Revisions				217235	C
LAL	Rev	Description	Chk	Date	Approved
	A	ENGRG RELEASE	BN	10-12-78	
	B	ADDED NOTE 3 (CUT ETCH & ADD JUMPER) ADDED DET. A (SH 5) ITEM 29 WAS: ASSY, LED (QTY 4 HLMP-6620P) QTY 1	BN	1-24-79	
X	C	MADE SEPERATE NOTES FOR LISTING 'CUT ETCH' INSTR (NOTE 3) AND 'ADD JUMPER' INSTR (NOTE 4)	BN	3-26-79	

ENGINEERING RELEASE

NTEP1-PWASSY.SIL (PNTEP-PWASSY.DM)

Dist Code SPG

Notes Unless Specified

1. Tolerances
   .xx ±.03
   .xxx ±.010
   Angular ±1/2°
2. Break All Sharp Edges .010 Approx
3. Mach. Surfaces
4. All Dim. In Inches

Drawn NISHIMURA

Check BN 3-26-79

Appr.

Material

Xerox Corporation
El Segundo, California

XEROX

ASSEMBLY, PRINTED WIRING-EMULATOR PROCESSOR (NOTETAKER)

Model No. / First Use	Finish	Code Ident	Size	Dwg. No.	Change Letter
NOTETAKER		18338	A	217235	C
Next Assy. / First Use 217684		Scale NONE	Do Not Scale Drawing	Sheet	1 OF 9

NOTES: UNLESS OTHERWISE SPECIFIED

1. ASSEMBLE PER MODULE ASSY SPEC, DWG NO. 216207.

2. DO NOT INSTALL I.C. SOCKETS IN 'SPARE' LOCATIONS.

3. THE FOLLOWING MODIFICATIONS ARE REQD USING 'A' REVISION PW BOARDS:

CUT ETCH

1) CUT ETCH TO EYELET NEXT TO B9 PIN 28 (COMP. SIDE).

2) CUT BOTH ETCHES TO F8 PIN 1 (COMP. SIDE).

3) CUT ETCH TO F7 PIN 1 (COMP. SIDE).

4) C3 PIN 9 (ETCH SIDE).

5) F8 PIN 2 (COMP. SIDE).

6) CUT ETCH TO F8 PIN 3 (COMP. SIDE).

7) CUT BOTH ETCHES TO F7 PIN 6 (COMP. SIDE & ETCH SIDE).

8) CUT ETCH TO A4 PIN 4 (ETCH SIDE).

9) C3 PIN 12 (ETCH SIDE).

10) C3 PIN 11 (COMP. SIDE).

11) C3 PIN 13 (COMP. SIDE).

12) C3 PIN 10 (ETCH SIDE).

13) B1 PIN 8 (COMP. SIDE).

14) B1 PIN 9 (COMP. SIDE).

15) A7 PIN 3 (COMP. SIDE).

16) A6 PIN 1 (ETCH SIDE).

17) F9 PIN 13 (ETCH SIDE).

18) F9 PIN 4 (ETCH SIDE).

19) F9 PIN 5 (ETCH SIDE).

20) F9 PIN 6 (ETCH SIDE).

21) CUT ETCH TO F9 PIN 4 (ETCH SIDE).

(NOTE 3 CONT'D ON SHEET 3)

NTEP2-PWASSY.SIL

Title

ASSY, PRINTED WIRNG-
EMULATOR PROCESSOR
(NOTETAKER)

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XEROX

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Sheet 2 Of 9

NOTE 3 CONT'D

CUT ETCH

22)	CUT ETCH TO	F9 PIN 5 (ETCH SIDE).
23)		F9 PIN 6 (ETCH SIDE).
24)		F9 PIN 13 (ETCH SIDE).
25)		A6 PIN 11 (ETCH SIDE ONLY).
26)		C5 PIN 8 (COMP. SIDE).
27)		EYELET NEXT TO F1 PIN 1 (COMP. SIDE ONLY).
28)		F6 PIN 7 (ETCH SIDE).
29)		F6 PIN 3 (ETCH SIDE).
30)		H6 PIN 9 (COMP. SIDE), CONNECTS TO RESISTOR PACK H6 PIN 7.
31)	CUT ETCH TO	H6 PIN 8 (ETCH SIDE).

4. THE FOLLOWING MODIFICATIONS ARE REQUIRED USING 'A' REVISION PW BOARDS:

ADD JUMPER (ETCH SIDE)

1)	ADD JUMPER FROM	EYELET LEFT OF A2 PIN 8 TO B4 PIN 3.
2)		B4 PIN 4 TO EYELET NEXT TO B9 PIN 28.
3)		F8 PIN 1 TO F4 PIN 28.
4)		F8 PIN 2 TO B4 PIN 8.
5)		F7 PIN 6 TO B1 PIN 12.
6)	ADD JUMPER FROM	F8 PIN 3 TO C3 PIN 10.

(NOTE 4 CONT'D OF SHEET 4)

Title: ASSY, PRINTED WIRNG-EMULATOR PROCESSOR (NOTETAKER)

Xerox Corporation
El Segundo, California

XEROX

217235 , C

Sheet 3 Of 9

NOTE 4 CONT'D (ADD JUMPER)

7) ADD JUMPER FROM C3 PIN 12 TO C3 PIN 7.

8) C3 PIN 11 TO F4 PIN 26.

9) C3 PIN 13 TO B3 PIN 1.

10) C3 PIN 9 TO F8 PIN 5.

11) C4 PIN 8 TO D4 PIN 8.

12) B1 PIN 13 TO B4 PIN 9.

13) F3 PIN 2 TO D9 PIN 10.

14) F3 PIN 5 TO E9 PIN 10.

15) F3 PIN 3 TO B5 PIN 6.

16) F3 PIN 6 TO B7 PIN 6.

17) F3 PIN 1 TO B1 PIN 9.

18) F3 PIN 4 TO B1 PIN 8.

19) H7 PIN 9 TO H8 PIN 11.

20) H7 PIN 8 TO C2 PIN 4.

21) C2 PIN 5 TO C3 PIN 3.

22) C2 PIN 6 TO A6 PIN 1.

23) A7 PIN 3 TO F4 PIN 27.

24) C5 PIN 12 TO A1 PIN 2.

25) F9 PIN 13 TO A1 PIN 3.

26) F6 PIN 11 TO CABLE CONN. PIN 47 (P2).

27) C4 PIN 9 TO F8 PIN 9.

28) C3 PIN 9 TO A4 PIN 4.

29) B1 PIN 11 TO C4 PIN 9.

30) ADD JUMPER FROM F7 PIN 1 TO C3 PIN 4.

NOTE 4 CONT'D ON SHEET 5

NTEP4-PWASSY.SIL

Title: ASSY,PRINTED WIRING-EMULATOR PROCESSOR (NOTETAKER)

Xerox Corporation
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XEROX

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Sheet 4 Of 9

NOTE 4 CONT'D (ADD JUMPER)

31) ADD JUMPER FROM F7 PIN 4 TO F4 PIN 32.

32) ADD JUMPER FROM A7 PIN 3 TO F4 PIN 27.

33) ADD JUMPER FROM C5 PIN 12 TO A1 PIN 2.

34) ADD JUMPER FROM MOTHERBD CONN PIN 7 (COMP. SIDE), ROUTE INSULATED WIRE THRU EYELET ON MOTHERBD CONN. (P1) PIN 6, TO F3 PIN 8 ON ETCH SIDE.

35) ADD JUMPER FROM F3 PIN 9 TO F3 PIN 7.

36) F3 PIN 10 TO F9 PIN 5.

37) C5 PIN 12 TO F9 PIN 4.

38) F9 PIN 6 TO A6 PIN 11.

39) C5 PIN8 TO MOTHERBD CONN.(P1) PIN 95.

40) H8 PIN 13 TO RESISTOR PACK H6 PIN 7.

41) EYELET ABOVE F1 PIN 1 TO F4 PIN 25.

42) F6 PIN 7 TO H9 PIN 9.

43) ADD JUMPER FROM F6 PIN 3 TO H6 PIN 5.

NTEP5-PWASSY.SIL

Title: ASSY, PRINTED WIRING- EMULATOR PROCESSOR (NOTETAKER)

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El Segundo, California
XEROX

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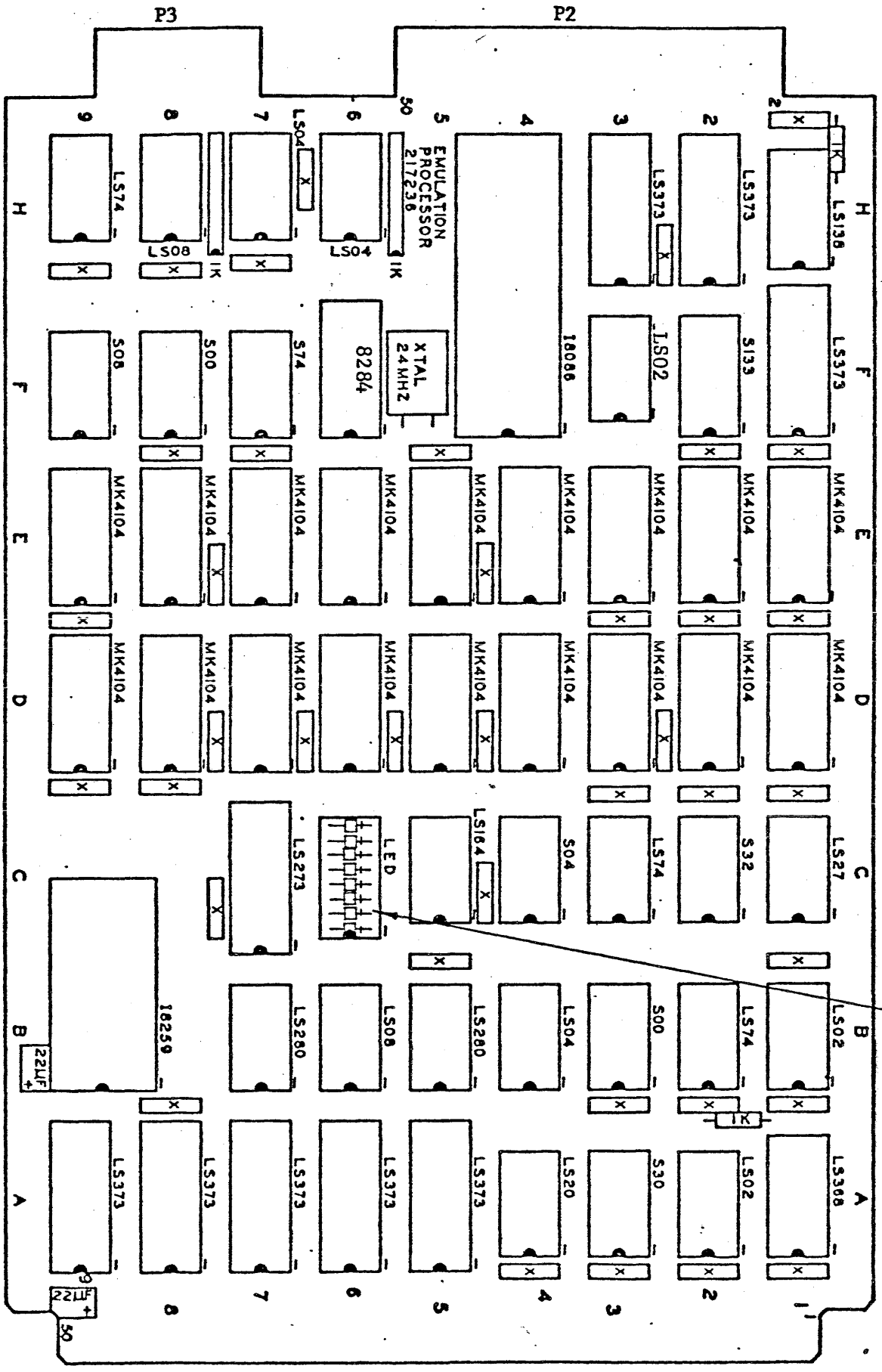
Sheet 5 of 9



Title

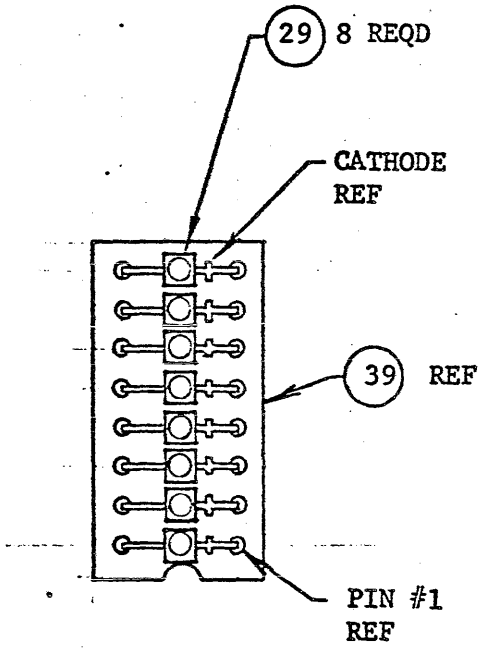
ASSY, PRINTED WIRING-
EMULATOR PROCESSOR

Xerox Corporation
El Segundo, California

XEROX

217235 C

Sheet 6 Of 9



LOC C6

DETAIL A
SCALE : 2/1

Title
ASSY,PRINTED WIRING-
EMULATION PROCESSOR

Xerox Corporation
El Segundo, California

XEROX

217235 C

Sheet 7 Of 9

Xerox Corporation
701 South Aviation Boulevard
El Segundo, California 90245

XEROX

MATERIAL LIST

ML	Drawing No.	Rev.
	217235	C

Rev. C

Drawing Title

ASSEMBLY, PRINTED WIRING-
EMULATOR PROCESSOR
(NOTETAKER)

NTEP8-PWASSY.SIL

Model No.	Date	Sheet
NOTETAKER 1	3/23/79	8 of 9

Eng. 217235

ML

Item No.	Drawing Title	Drawing No.	No. Req.	Remarks
1	BOARD, PW-EMULATOR PROCESSOR	217236	1	
2				
3	MICROCIRCUIT 8086 MICROPROCESSOR		1	F4
4	8284 CLOCK GEN.		1	F6
5	8259A INTRP CONTR.		1	B9
6	4104-3 RAM (4KX1)		18	D1-D9,E1-E9
7	74LS02		3	A2,B1,F3
8	74LS04		3	B4,H6,H7
9	74LS08		2	B6,H8
10	74LS138		1	H1
11	74LS164		1	C5
12	74LS20		1	A4
13	74LS27		1	C1
14	74LS273		1	C7
15	74LS280		2	B5,B7
16	74LS368		1	A1
17	74LS373		8	A5-A9,F1,H2,H3
18	74LS74		3	B2,C3,H9
19	74S00		2	B3,F8
20	74S04		1	C4
21	74S08		1	F9
22	74S133		1	F2
23	74S30		1	A3
24	74S32		1	C2
25	MICROCIRCUIT 74S74		1	F7
26				
27	RESISTOR NET SIP CTS #750-81-1K		2	H5,H7
28	CRYSTAL, 24 MHZ CTS #MP240		1	F5
29	LAMP, SUB-MIN HEWLETT PACKARD #HLMP-6620		8	C6 SEE DET. A (SH 5)
30				

701 South Aviation Boulevard
El Segundo, California 90245

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MATERIAL LIST

ML	Drawing No.	Rev.
	217235	C

Rev. C

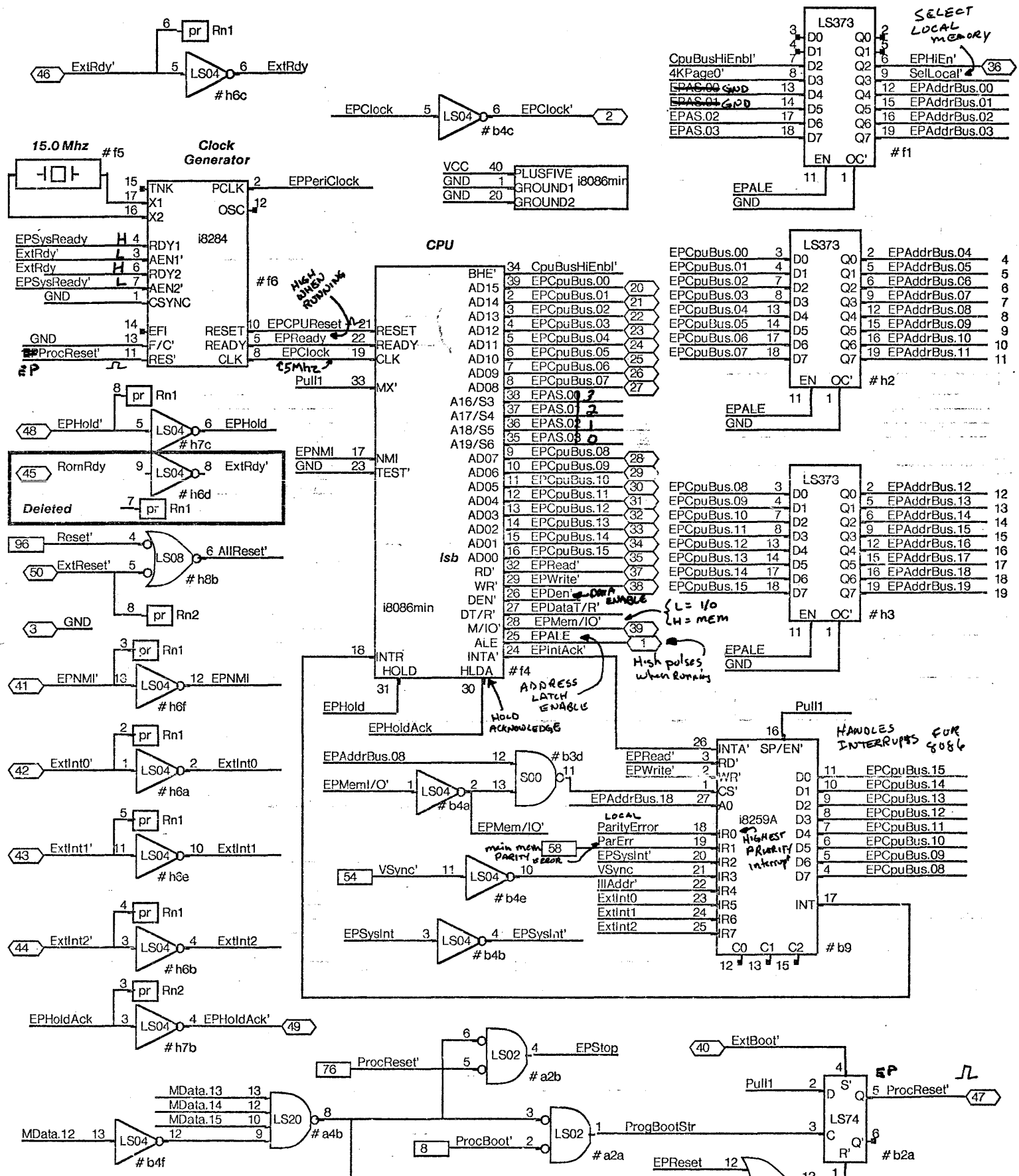
Drawing Title

ASSEMBLY, PRINTED WIRING- EMULATOR PROCESSOR . (NOTETAKER)

NTEP7-PWASSY.SIL

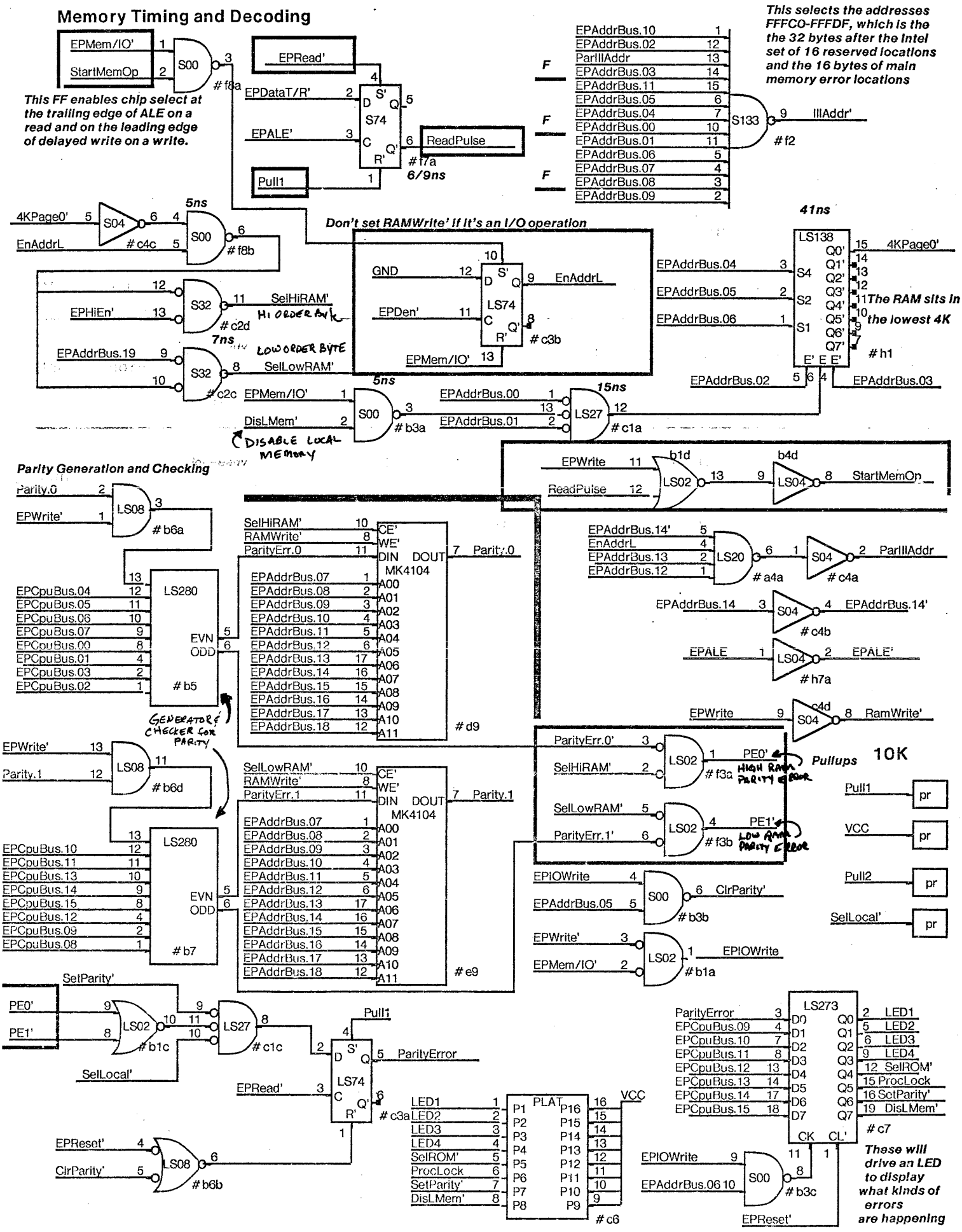
Model No.	Date	Sheet
NOTETAKER 1	3/23/79	9 of 9

Item No.	Drawing Title	Drawing No.	No. Req.	Remarks
31	RESISTOR, 1K, 5%, 1/4 W	116447-102	2	B2,H1
32				
33	CAPACITOR, .047 uF, CER (AVX # DG01SC473M)		39	LABELED "X"
34	CAPACITOR, TANT, 22uF	114491-226	2	A9,B9
35				
36				
37				
38	SOCKET, I.C. 14 PIN AUGAT # 514-AG11D		24	
39	16 PIN AUGAT # 516-AG11D		2	
40	18 PIN AUGAT # 518-AG11D		18	
41	20 PIN AUGAT # 520-AG11D		9	
42	28 PIN AUGAT # 528-AG11D		1	
43	SOCKET, I.C. 40 PIN AUGAT # 540-AG11D		1	
44				
45				

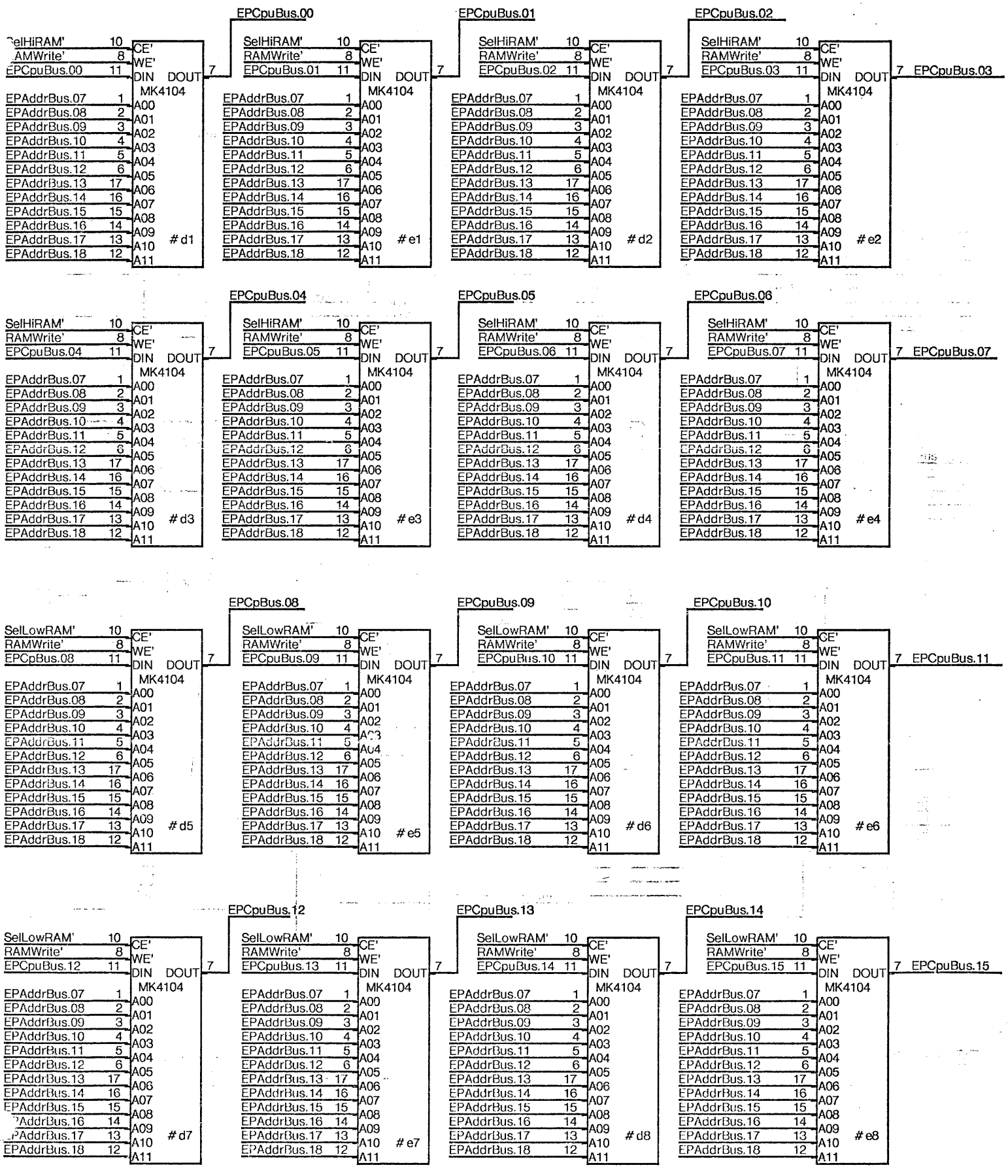


XEROX SSL	Project NoteTaker	Emulation Processor CPU Section	File pntep01-assy.sil	Designer Fairbairn	Rev D	Date 3/20/79	Page 01

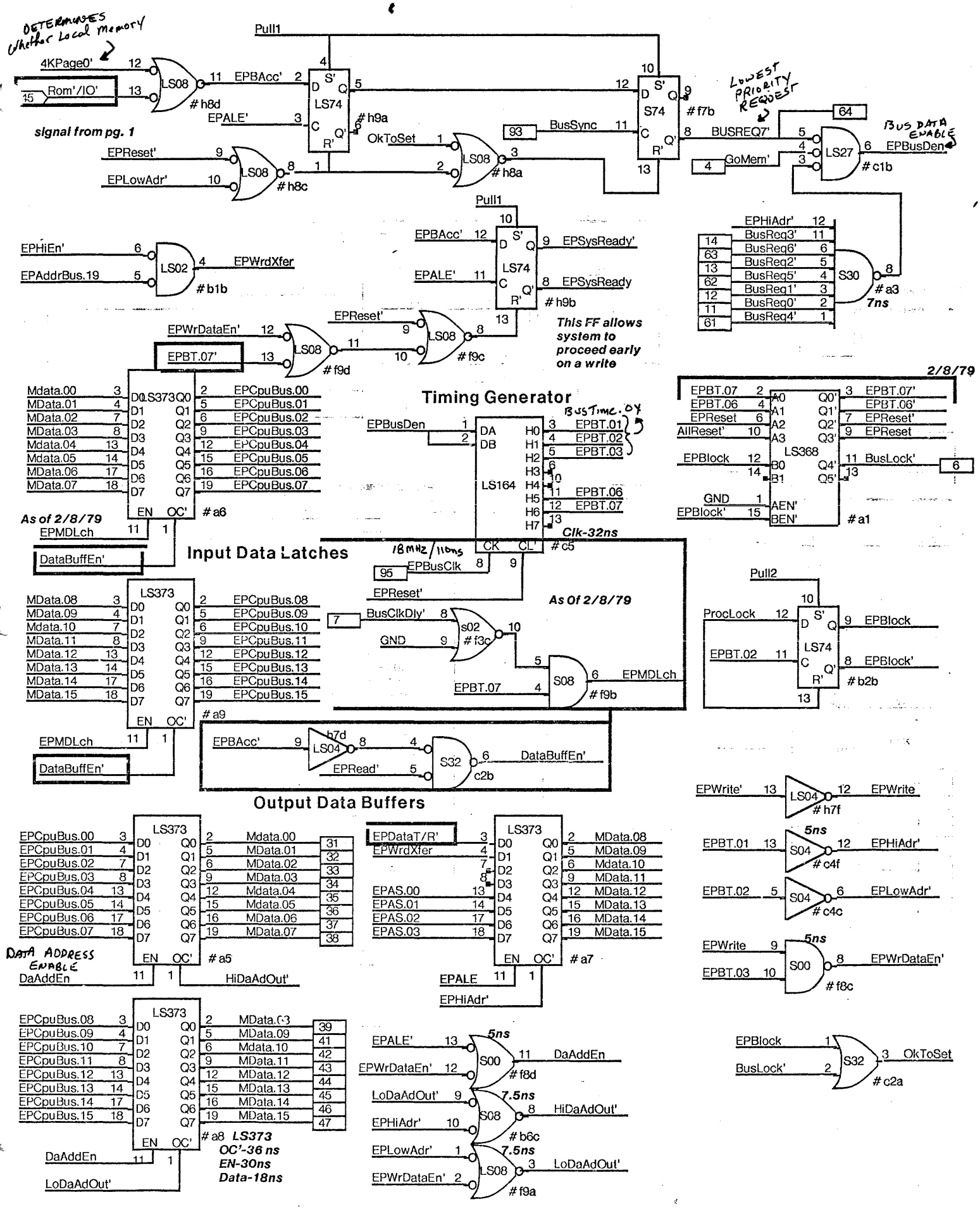
Memory Timing and Decoding



XEROX SSL	Project NT	Emulation Processor Memory Decode and Parity	File pntep02-assy.sil	Designer Fairbairn	Rev D	Date 3/20/79	Page 02



XEROX SSL	Project NT	Emulation Processor RAM - 4096x16	File pntep03-assy.sil	Designer Fairbairn	Rev A	Date 8/22/78	Page 03

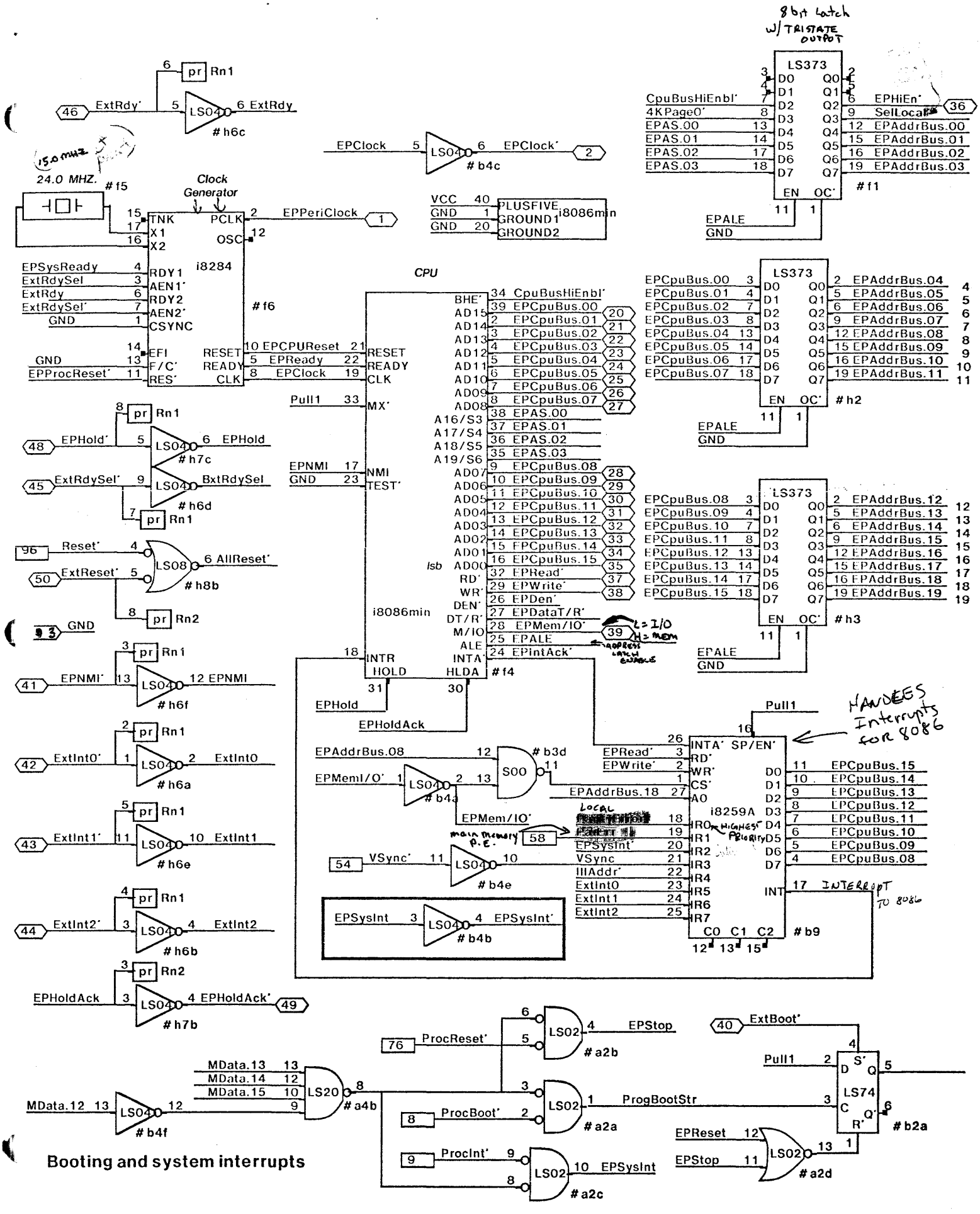


XEROX SSL	Project NoteTaker	Emulation Processor System Bus Interface	File pntep04-assy.sil	Designer Fairbairn	Rev D	Date 3/20/79	Page 04

Note:

EPReady = EPSysReady.IOReady' + IOReady.EPSysReady'

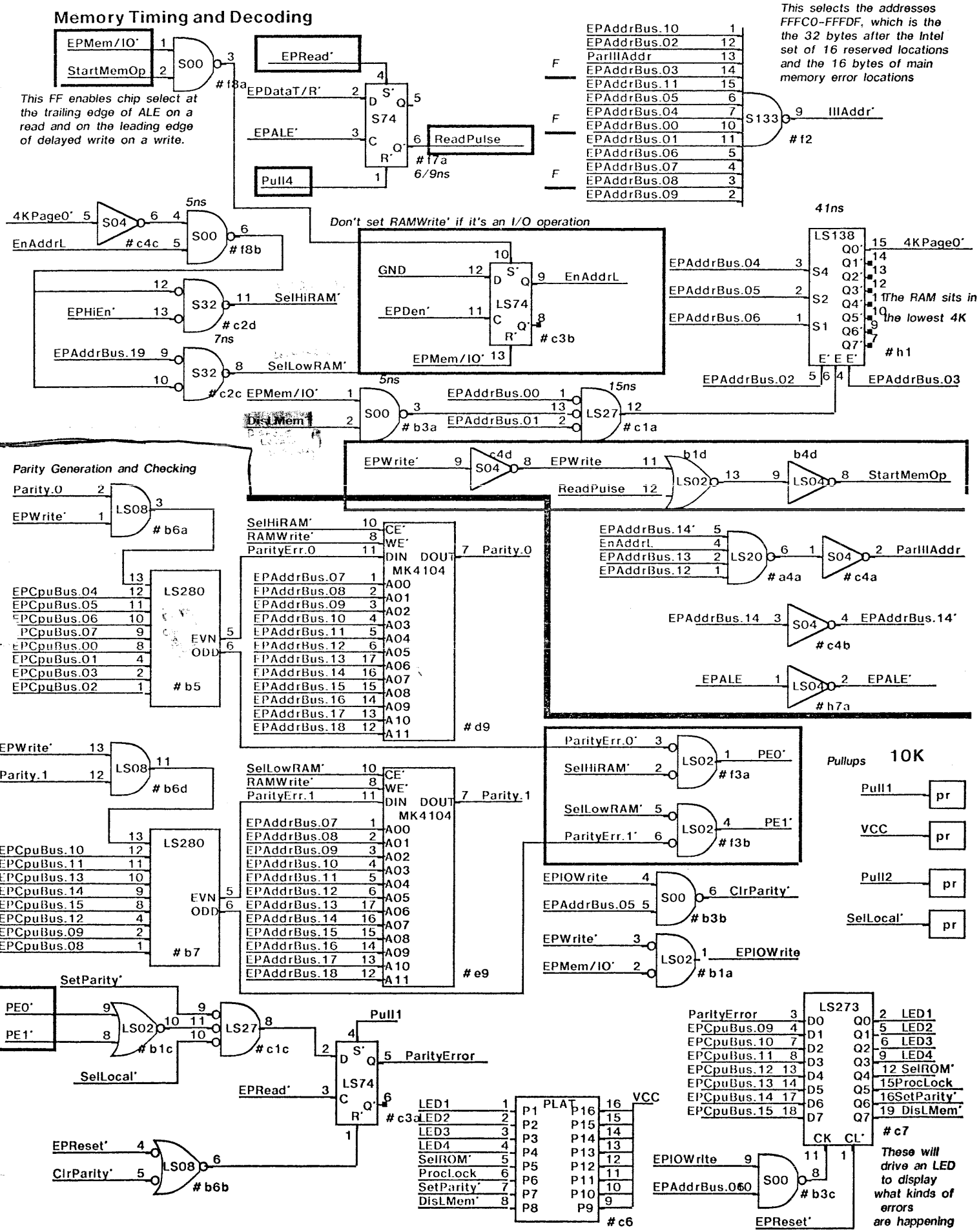
Internal Ram	*Ready*	1	·	0	1	·	0	
Main Memory	*Not Ready*	0	·	0	1	·	1	
	Ready	1	·	0	1	·	0	
Rom	*Not Ready*	1	·	1	0	·	0	
	Ready	1	·	0	1	·	0	



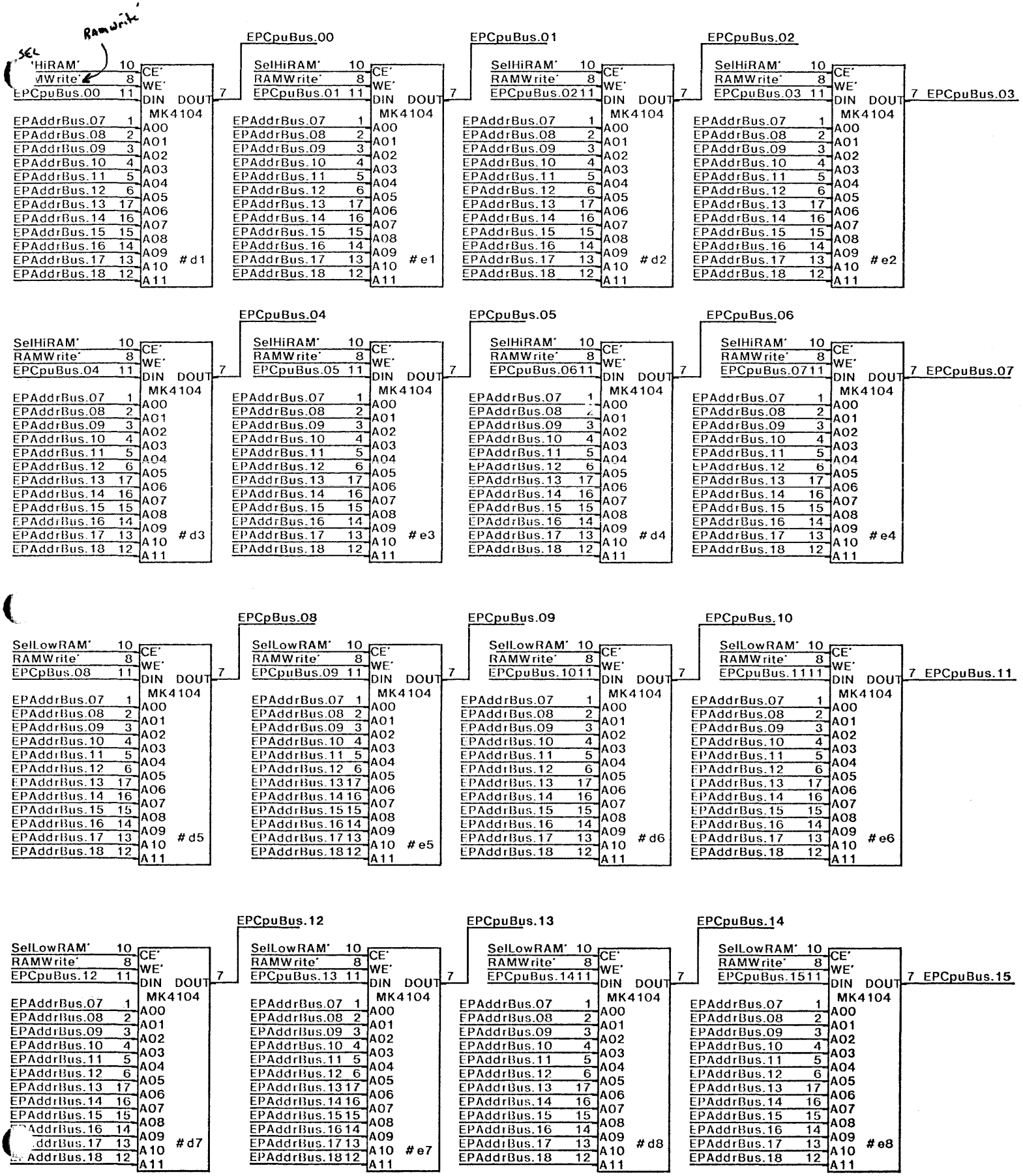
Booting and system interrupts

XEROX SSL	Project NoteTaker	Emulation Processor CPU Section	File pntep01-assy.sil	Designer Fairbairn	Rev C	Date 1/15/79	Page 01

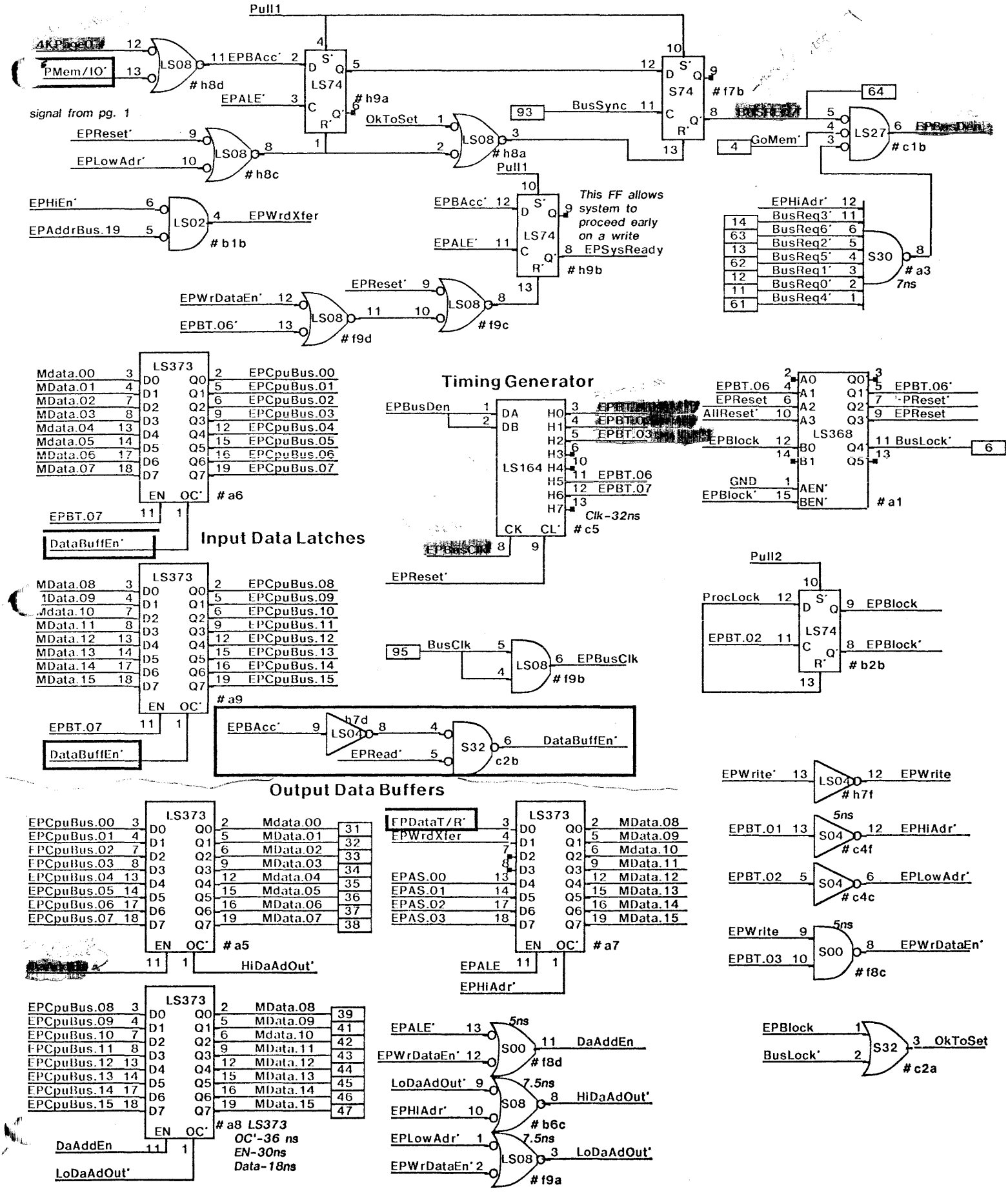
Memory Timing and Decoding



XEROX SSL	Project NT	Emulation Processor Memory Decode and Parity	File pntep02-assy.sil	Designer Fairbairn	Rev C	Date 1/15/79	Page 02



XEROX SSL	Project NT	Emulation Processor RAM - 4096x16	File pntep03-assy.sil	Designer Fairbairn	Rev A	Date 8/22/78	Page 03



XEROX SSL	Project NoteTaker	Emulation Processor System Bus Interface	File pntep04-assy.sil	Designer Fairbairn	Rev C	Date 1/15/79	Page 04