Appendix A Rigid Disk Subsystem

Appendix A: Rigid Disk Subsystem

Appendix A contains supplementary material for the rigid disk subsystem. Information is presented in the following order:

A.1 Disk Command Block (DCB) allowable commands, format, and operational errors.

A.2 State machine PROM contents

Schematics for the rigid disk subsystem are located in Appendix D.

A.1 Disk Command Block

A.1.1. DBC Commands

Table A.1 lists the operations provided by the disk command block.

Table A.1. Disk Operations

Operation	Function			Opcode in DCB
	header	label	data	
Restore-Recalibrate				0
Format Tracks	w	w	w	1
Read Data	v	v	r	2
Write Data	v	v	w	3
Write Label and Data	v	w	w	4
Read Label	v	r	n	5
Read Label and Data	v	r	r	6
Verify Data	v	v	v	7
Read Diagnostic*	r	r	r	10

* Not yet implemented.

w = write v = verify r = read n = ignore

A.1.2. DBC Format

In the Control Block, the rigid disk controller requires:

- Header image
- Label image

The rigid disk controller maintains: Current cylinder - 2 bytes

Table A.2 lists the header and label layout in the scratchpad and in FIFO. Information given in the table is subject to change.

Table A.2. Header and Label Layout in Scratchpad (SP) and FIFO

SP Loc	Contents of SP bit7 - bit0	Contents of FIFO bit15 - bit0 If (xxxx), then set to xx when sending If {xxxx}, then special case–see note
BC BD	DTACRC (+1)	CRC syndrome, Wd 1 (0000)
BE BF	(00) (00)	Reserved. Always 0
C0 C1	SECNTH SECNTL	-Number of sectors to transfer (two's complement)
C2 C3	0 SECPT	(Max sector number) + 1 (per track)
C4 C5	MCVRL HDSPC	Microcode revision level # # # (No of heads) + 1 per cylinder
C6 C7	CTLPDH CYLPDL	(No of cylinders) + 1 per drive
C9 C9	0 FSEC	Inv/Non-inv flag. See # # below. First sector number per track
CA CB #	WICYH WICYL	Reduce write current cylinder {FFFF}
CC CD	PCCYH PCCYL	Precomp cylinder
CE CF ##	0 WENDC	Sector length for diagnostics. Normal = -1 (FF)
D0 D1	0 HDRERT	Header error type (0000)
D2 0 D3	LBERT	Label error type (0000)
D4 D5	0 DTAERT	Data error type (0000)
D6 D7	0 LSTERT	Last error type (0000)
D8 D9	FCURCH FCURCL	Current cylinder ** (FFFF)
DA DB	0 1	Always 1
DC DD	CYL H CYL L	CYL Header image
DE DF	HD SEC	HD ! SEC Header image

– more –

Table A.2. Header and Label Layout (continued)

SP Loc	Contents of SP bit7 - bit0	Contents of FIFO bits15 - bit0	
E0 E1	RES1H RES1L	Reserved 1 (0000)	
E2 E3	RES2H RES2L	Reserved 2 (0000)	
E4 E5	DvSt CntSt	Drive and controller status	
E6 E7	0 OPER	Operation to be done	
E8 E9	TKFH TKFL	-No. of track to be formatted (two's complement)	
EA	*not used*		
EB EC	FID0 H FID0 L	FID0	Label Image
ED EE	FID1 H FID1 L	FID1	
EF F0	FID2 H FID2 L	FID2	
F1 F2	FID3 H FID3 L	FID3	
F3 F4	FID4 H FID4 L	1FID4	
F5 F6	FPLo H FPLo L	FP low	
F7 F8	FPHi&Flags H FPHi&Flags L	FPHi&Flags	
F9 FA	FT Hi FT Lo	FT	
FB FC	bootCLLo H bootCLLo L	bootCL Lo	
FD FE	bootCLHi H bootCLHi L	bootCl Hi	
FF	*not used*		

Notes for Table A.2

\# ReduceWrite Current Cyl: If the drive does not need this signal, then put FFFF in this location.

\#\# Sector Length: For normal length sectors, use -1. Some diagnostic operations will require longer data blocks, and they will use -2 here.

** Current cylinder: Load with FFFF. The value is a copy of the actual value. Between operations it is kept in a different location and copied here before it is sent to the FIFO. The value is the current cylinder number, with these exceptions:

- between the beginning of an operation and the end of the implied seek

- between the start and end of an implied seek occurring in the middle of an operation.

If the word content is FFFF, then the current cylinder is undefined. The contents are set to FFFF at the beginning of a seek and are set to the new value at the end of a seek.

Inv/Non-Inv Flag: The early pre-prototype IOP board inverted data (including the DCB data) between the IOP and the RDC. Production IOPs do not invert this data. The flag byte enables the IOP to tell the difference.

This byte, the most significant byte of FSec, is written to 0 when the command, LoadCommandBloc (put current status in the DiscCommandBlock), is executed by the RDC.

If the DCB is read without software inversion, then this byte indicates whether the hardware is non-inverting or inverting.

If read as 0, then the hardware is non-inverting.

If read as FF, then the hardware is inverting.

If an inverting RDC is read with software inversion, then this byte is 0.

Microcode revision level:

All microcode up to and including RDCENB = 0

Next microcode change that affects head and pilot = 1, and so forth.

The information sent to the RDC is sent back with appropriate changes.

A.1.3. DBC Errors

Errors are presented as one byte, the low order byte of the word, divided into two nibbles. Table A.3 lists the error codes.

Table A.3. Error Codes

High order nibble: 0 = FIFO protocol error 1 = Header error 2 = Label error 3 = Data error 8 or higher = error not encoded. Each number is a specific, not encoded, error type.
Low order nibble for types 1, 2, and 3 1 = Address Mark error: AM not found where expected 2 = ID error: wrong ID byte found 3 = Verify (compare) error: data was not what was expected 4 = CRC error 5 = Both verify and CRC/ECC errors
FIFO errors 01 = FIFO empty at GetCommandBlock command 03 = FIFO not empty at start of read from disk 04 = FIFO has been full for four revolutions of the disk during a read from disk 05 = FIFO has been empty for N revolutions of disk during a write to disk 07 = FIFO **not** empty at LoadCommandBlock command More To be defined
Other errors 81 = Sector not found 82 = Cylinder number too big during implied seek: no. of sectors went off top of disk 84 = Current cylinder unknown 85 = Write fault 8A = Illegal operation 8B = Illegal diagnostic operation 8C = Protocol sequence error: 2 (ExecuteCommandBlock) **not** preceded by 1 (GetCommandBlock) 8D = Not Ready&SeekComplete error: Not Ready&seekComp at beginning of data transfer operation
Contents of Drive Status Bit 0 = Lock detected 1 = Not Write fault 2 = Not Track 000 3 = Not Stored Index mark 4 = Address Mark out (AMdetected) 5 = always 0 6 = Not Seek completed 7 = Not Ready
Contents of Controller Status Bit 0 = FIFO full, synchronized 1 = FIFO empty, synchronized 2 = FIFO A1B1 same 3 = Not SP MA max count 4 = Not SP MA bit 3 5 = FIFO empty at read 6 = Not BDONE 7 = Read data found

A.2 State Machine PROM Contents

Table A.4 lists the PROM contents of the state machine.

Table A.4. States of the State Machine: PROM contents

	Address In						**Data Out**									
	External Inputs						PROM Outputs (after Lo-to-Hi clock edge)									
	RunSM	DHLDA	SARDY	FIFOOB'1	EOX'		ErrorTrap'	RDiskDmaintr	GateSLines'	ADDr' / Data	DMA Active	DRead / DWrite	RDCHoldReq	FIFOPreFetch		
Comments						StateNumber*										Next State*
WaitForHLDA	1	0	X	X	X	0010 ④	1	0	1	1	0	0	1	0		0010
GotHLDA	1	1	X	X	X	0010 ⑤	1	0	1	1	1	0	1	0		0111
T1State	1	X	X	X	X	0100 ⑥	1	0	0	0	1	1	1	1		0101
T2State	1	X	X	X	X	0101 ⑥	1	0	0	1	1	1	1	0		0110
T3State	1	X	X	X	X	0110 ⑥	1	0	1	1	1	1	1	0		0111
TwAndWait	1	X	0	X	X	0111 ⑦	1	0	1	1	1	1	1	0		0111
T4Normal	1	1	1	1	1	0111 ⑧	1	0	0	1	1	0	1	1		0100
T4AndEOXfer	1	X	1	X	0	0111 ⑧	1	0	1	1	1	0	1	0		1010
T4AndOutOfBnd	1	X	1	0	1	0111 ⑧	1	0	1	1	1	0	1	0		1000
T4AndEtherHld	1	0	1	X	1	0111 ⑧	1	0	1	1	1	0	1	0		1000
DropHLD	1	X	X	X	1	1000	1	0	1	1	1	0	0	0		1100
SendIntReq	1	X	X	X	0	1010	1	1	1	1	1	0	0	0		1100
WaitForFIFO	1	X	X	0	X	1100 ②	1	0	1	1	0	0	0	0		1100
SendHld	1	X	X	1	X	1100 ③	1	0	1	1	0	0	1	0		0010
DMA Disabled = (initial wait)	0	X	X	X	X	1100 ①	1	0	1	1	0	0	0	0		1100
ErrorEntryPoint (see note below)	1	X	X	X	X	1101	0	1	1	1	0	0	0	0		1100

* No explicit State Number or State ID exists within the State Machine PROM. These numbers are for identification only.

Note: The PROM area not covered in the table is programmed as Error condition (same as ErrorEntryPoint). The circled numbers correspond to the numbers on the state diagrams shown on Figures 5.15, 5.16, and 5.17.

Requirement: All external inputs other than SARDY must maintain their new logic level for at least two clock cycles.

IMPORTANT NOTE:

The State Machine marches through its states by means of an inherent pattern created by a combination of external inputs and the PROM outputs from the previous clock cycle. Therefore, changing the timing of the signals by manipulating the PROM contents is NOT advisable.

If such a change should become necessary, then a thorough analysis of the State Machine PROM behavior under all circumstances will be required. The timing of all the signals from the PROM as well as their derivative signals must be carefully analyzed and examined before any PROM commitment.