7. Floppy Disk Subsystem TABLE OF CONTENTS

7. Floppy Disk Subsystem

The floppy disk subsystem provides low cost, high density, removable storage media for the Dove workstation. Figure 7.1 illustrates the floppy disk subsystem as it applies to the overall IOP board. The number in parenthesis corresponds to the section in which the device is described.

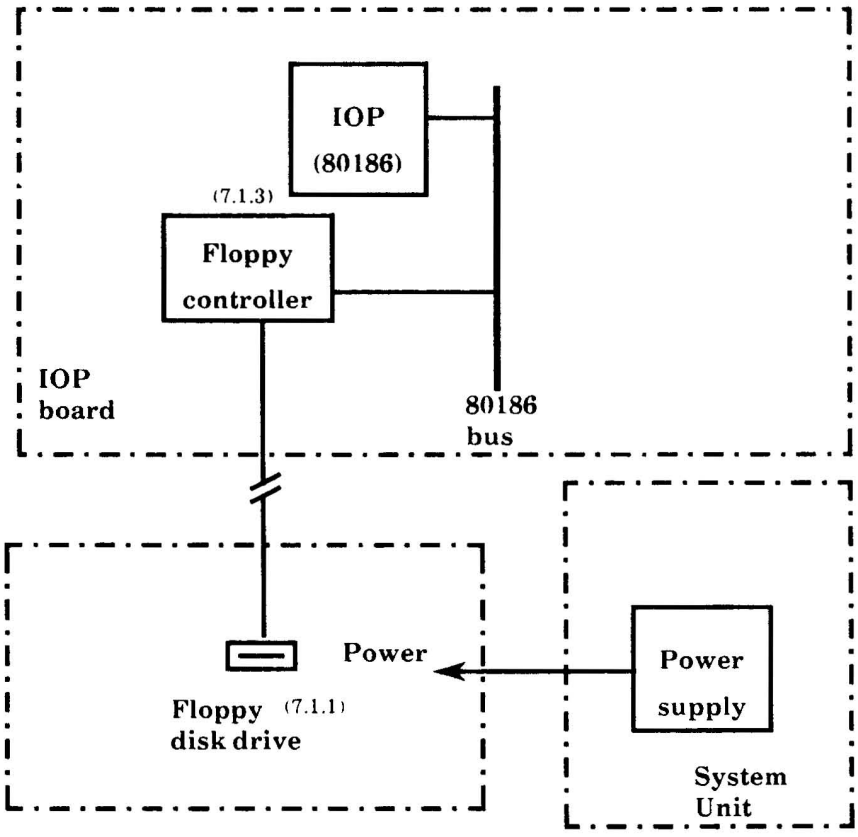

Figure 7.1. Floppy disk subsystem block diagram

7.1 Hardware

The floppy disk subsystem consists of the following components:

- Floppy disk drive (section 7.1.1)
- Floppy diskette (section 7.1.2)
- Floppy disk controller (section 7.1.3)

Together, these components constitute the floppy disk subsystem. The hardware is discussed in the following subsections. For schematic drawings, refer to appendix D.

7.1.1 Floppy Disk Drives

The floppy disk drive is a half-height device. The interface to the drive is compatible with the Shugart SA450 Standard Interface.

The floppy disk controller supports up to four $5\frac{1}{4}$-inch double-sided or single/double density floppy disk drives. The drives have a 250K bit/second or 500K bit/second transfer rate. The current packaging will allow only a single drive.

7.1.2 Diskettes

Figure 7.2 illustrates the diskette used with the disk drive. The diskette consists of a flexible magnetic disk enclosed in a protective jacket. The jacket cleans the diskette during normal operation or rotation (300/360 rpm). An opening in the jacket provides read/write/erase head access.

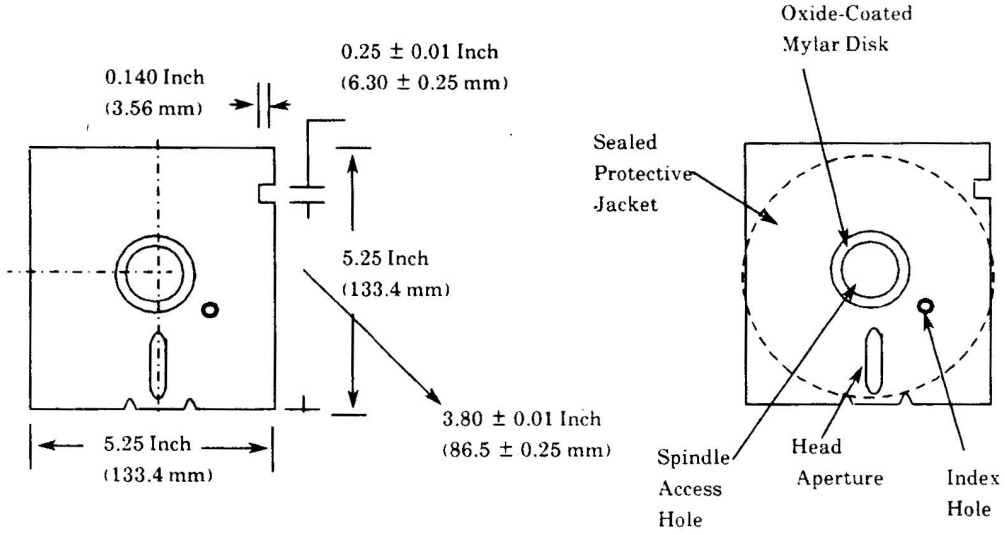

Figure 7.2. Diskettes

Two types of diskettes are supported: 48 TPI drives (IBM PC compatible) and 96 TPI drives (not IBM PC compatible). Table 7.1 summarizes the characteristics of both diskette types. Diskette format is discussed in section 7.3.4.

Table 7.1. Characteristics of Formatted Diskettes

Characteristic	48 TPI SA455	96 TPI SA465	96 TPI SA475
Diskette Size	5¼ inches	5¼ inches	5¼ inches
Sides	2	2	2
Tracks/Side	40	80	80
Sectors/Track	9	9	15
Bytes/Sector	512	512	512
Bytes/Track	4608	4608	7680
Bytes/Side	184.32K	368.64K	614.4K
Bytes/Diskette	368.64K	737.28K	1.2288M
Rotation Speed	300 RPM	300 RPM	360 RPM
Transfer Rate	250K bit/sec	250K bit/sec	500K bit/sec
Recording Method	MFM	MFM	MFM

7.1.3 Floppy Disk Controller

The Floppy Disk Controller (FDC) consists of an Intel 8272 chip and a Standard Microsystems 9229 chip. The 8272 chip serves as the IOP interface to the floppy disk; the 9229 chip acts as a data separator.

7.1.3.1. Controller Interface

The Intel 8272 floppy disk controller chip consists of two sections: the controller itself and the controller interface to the data separator and floppy disk drive.

The floppy disk controller interface to the IOP is a standard microprocessor interface; that is, it has a data bus, chip select, write strobe, and read strobe.

Figure 7.3 illustrates the pins and signals of the 8272 floppy disk controller. Table 7.2 lists the pins by name and number and explains their function in the controller system.

Note: The signal FDMaReq goes through logic that delays the DMA request by approximately 1 µs.

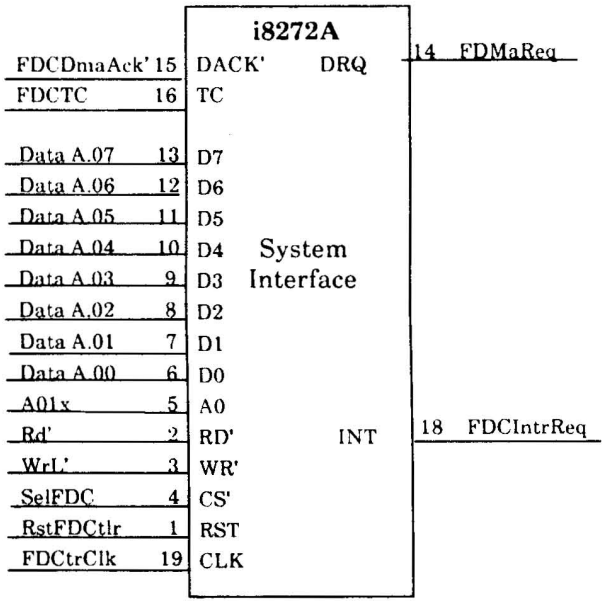

Figure 7.3. 8272 floppy disk controller pins and signals

Table 7.2. 8272 Pin Assignments
(reprinted by permission of Intel Corporation)

Symbol	Pin No.	Type	Connection To	Name and Function
A0	5	Input	µP	**Data Status Register Select:** Selects Data Reg (A0 = 1) or Status Reg (A0 = 0) contents to be sent to data bus.
CLK	19	Input		**Clock:** Single phase 8 MHz squarewave clock.
CS	4	Input	µP	**Chip Select:** IC selected when 0 (low) allowing RD' and WR' to be enabled.
D0-D7	6-13	I/O	µP	**Data Bus:** Bidirectional 8-bit data bus.
DACK'	15	Input	DMA	**DMA Acknowledge:** The DMA cycle is active when 0 (low) and controller is performing DMA transfer.
DRQ	14	Output	DMA	**Data DMA Request:** DMA request is being made by FDC when DRQ = 1.
INT	18	Output	µP	**Interrupt:** Interrupt request generated by FDC.
RD'	2	Input	µP	**Read Control:** Signal for transfer of data from FDC to Data Bus when 0 (low).
RST	1	Input	µP	**Reset:** Places FDC in idle state. Resets output lines to FDC to 0 (low). This does not clear the last specify command.
TC	16	Input	DMA	**Terminal Count:** This pin indicates the termination of a DMA transfer when 1 (high).
WR'	3	Input	µP	**Write:** Control signal for transfer of data to FDC via Data Bus when 0 (low).

The 8272 also has a floppy disk drive interface connecting the 9229 and the floppy disk drive. The drive interface is limited to a 10-foot maximum cable length. Figure 7.4 illustrates the pins and signals of the interface. Table 7.3 lists the pins by name and number and explains their function.

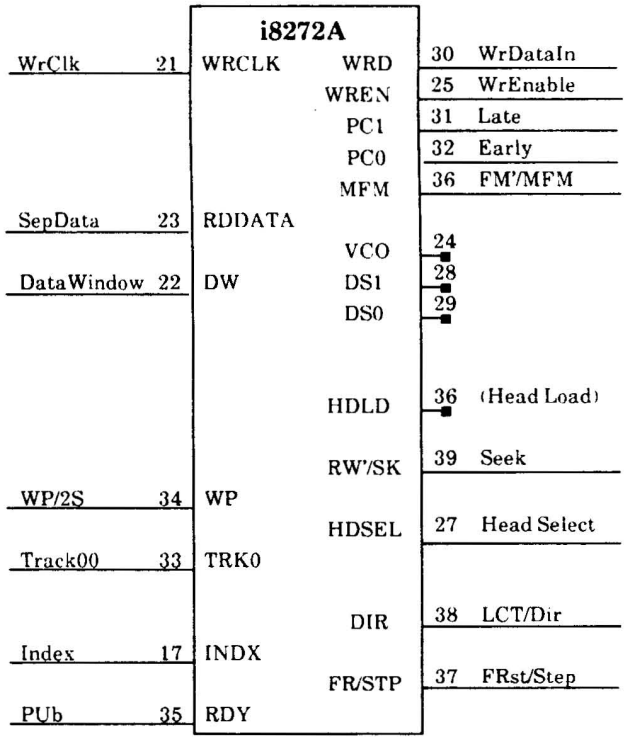

Figure 7.4. 8272 floppy disk controller interface pins and signals

Table 7.3. 8272 Interface Pin Assignments
(reprinted by permission of Intel Corporation)

Symbol	Pin No.	Type	Connection To	Name and Function
DW	22	Input	PLL	**Data Window:** Data sample signal from the phase-locked loop indicating that the FDC should sample input data from the disk drive.
DS_1, DS_0	28, 29	Output	Drive	**Drive Select:** Selects the disk drives.
FLT/TRK0	33	Input	Drive	**Fault/Track 0:** Senses the disk drive fault condition in the Read/Write mode and the Track 0 condition in the seek mode.
FR/STP	37	Output	Drive	**Fault Reset/Step:** Resets the fault flip-flop in the disk drive when operating in the Read/Write mode. Provides head step pulses (to move the head from one cylinder to another cylinder) in the Seek mode.
GND	20			**Ground:** dc power return.
HDLD	36	Output	Drive	**Head Load:** Loads the disk drive read/write head. (The head is placed in contact with the disk.)
HDSEL	27	Output	Drive	**Head Select** Selects head 0 or head 1 on a dual-sided disk.

- more -

Table 7.3. 8272 Interface Pin Assignments (continued)

Symbol	Pin No.	Type	Connection To	Name and Function
LCT/DIR	38	Input	Drive	**Low Current/Direction:** Signals that the recording head has been positioned over the inner cylinders (44-47) of the floppy disk in the Read/Write mode. (The write current must be lowered when recording on the physically shorter inner cylinders of the disk. Most drives do not track the actual head position and require that the FDC supply this signal. Determines the head step direction in the Seek mode. In the Seek mode, a high level on this pin steps the read/write head toward the spindle (step-in). A low level steps the head away from the spindle (step-out).
MFM	26	Output	PLL	**MFM Mode:** Active-high output used by external logic to enable MFM double-density recording mode. When the MFM output is low, single-density FM recording is indicated.
PC_1, PC_0	31, 32	Output	Drive	**Precompensation** (pre-shift) **Control**: Write precompensation output control during MFM mode. Specifies early, late, and normal timing signals.
RDDATA	23	Input	Drive	**Read Data:** FDC input data from the selected disk drive.
RDY	35	Input	Drive	**Ready:** Senses the disk drive ready status.
RW'/SEEK	39	Input	Drive	**Read, Write/Seek:** Mode Selector. A high level selects the Seek mode; a low level selects the Read/Write mode.
Vcc	40			+5V dc power.
VCO	24	Output	PLL	**VCO Sync:** Active-high signal indicating an 8272 interrupt service request.
WREN	25	Output	PLL	**Write Enable:** Active-high output that enables the disk drive write gate.
WP/TS	34	Input	Drive	**Write Protect/Two Sided:** Senses the disk write protect status in the Read/Write mode and the dual-sided media status in the Seek mode.
WRCLK	21	Input		**Write Clock:** 500 KHz (FM) or 1 MHz (FM) clock with a constant pulse width of 250 ns (for both FM and MFM recording). The write clock must be present at all times.
WRD	30	Output	Drive	**Write Data:** Serial data stream (combinations of clock and data bits) to be written on the disk.

7.1.3.2. Data Separator

Figure 7.5 illustrates the pins and signals of the 18-pin 9229 data separator. Table 7.4 lists the pins by name and number and explains their function.

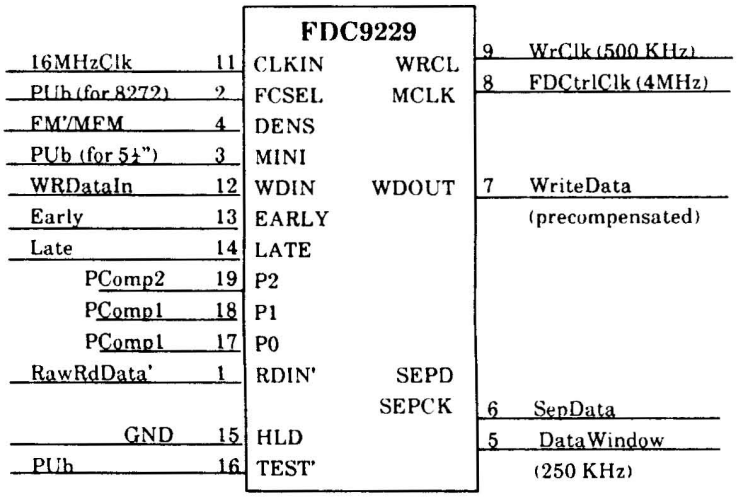

Figure 7.5. 9229 data separator pins and signals

Table 7.4. 9229 Pin Assignments

Symbol	Pin No.	Type	Connection To	Name and Function
CLKIN	11	Input	16 MHz Clock	**Clock In:** Connects to a 16 MHz crystal.
DENS	4	Input	FDC	**Density:** Indicates configuration for double density (MFM) floppy disk drive interfaces.
EARLY	13	Input	FDC	**Early Precompensation:** When high, writes WriteData pulse to the floppy disk.
FCSEL	2	Input	Pull-Up	**Floppy Controller Select:** Set high to indicate that data separator is programmed for 8272 controller.
HLD	15	Input	N/C	Not used.
LATE	14	Input	FDC	**Late Precompensation:** When high, the current WriteData pulse is written late to the disk. When both Early and Late are low, the current WriteData pulse is written early to the floppy disk.
MCLK	8	Output	FDC	**FDC Clock:** The 4 MHz master clock to the floppy disk controller.
MINI	3	Input	Control Register	**8 in./5¼ Select:** Indicates 5¼-inch FDC interface.
P0-P2	17-19	Input	Control Register	**Precompensation Value:** Sets 250 ns as amount of precompensation applied to the write data.
RDIN'	1	Input	Drive	**Read Data In:** (active low) Receives raw read data from the floppy disk drive.
SEPCK	5	Output	FDC	**Separated Clock:** Outputs a 250 KHz squarewave window clock signal.
SEPD	6	Output	FDC	**Separated Data:** Regenerated data pulse derived from the raw data input.
TEST'	16	Input	Pull-Up	**Test Mode:** Tied high for normal operation.
WRCLK	9	Output	FDC	**Write Clock:** Writes 500 KHz clock with 250 ns pulse width to the floppy disk controller.
WDOUT	7	Output	Drive	**Write Data Out:** Generates precompensated WriteData stream to the floppy disk drive.
WDIN	12	Input	FDC	**Write Data In:** Receives write data stream from the floppy disk controller.

7.2 Theory of Operations

The floppy disk controller (FDC) converts high level disk commands to the appropriate sequence of disk drive control signals.

Figure 7.6 illustrates the data paths of the floppy disk subsystem. The number in parentheses is the number of the subsection that discusses the component.

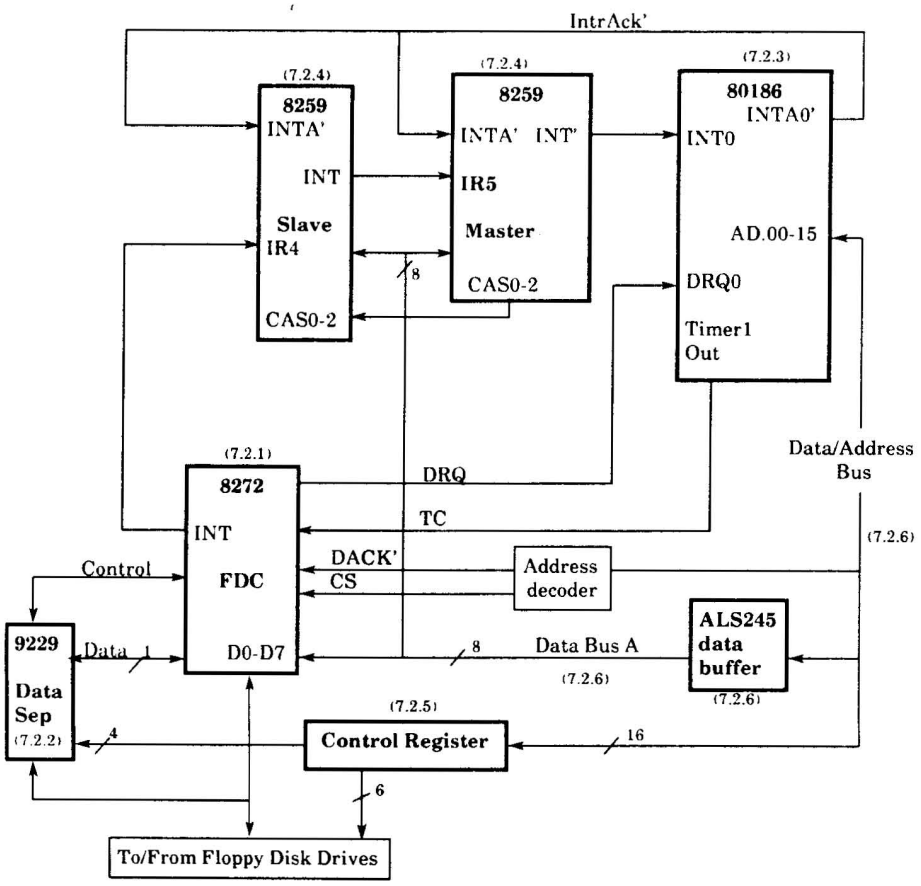

Figure 7.6. System interface

7.2.1 Floppy Disk Controller

The floppy disk controller translates IOP commands, such as format, read, and write, into the required control signals and sequences for the floppy disk. The controller is instructed by the IOP where, what, and how much to read.

Requests are exchanged by way of a DMA circuit consisting of a DMA request line, a terminal count line, and a DMA acknowledge line. The DMA request line is active only during data transfer.

When the floppy disk controller needs a byte for a write operation or holds a byte from a read operation, it activates the DMA request line. This signal (DRQ) notifies the 80186 that a DMA transfer is required.

When the DMA reads or writes the data byte to the floppy disk controller, the DMA acknowledge line is activated by the DMA. The floppy disk controller deactivates the FDC request line approximately 200 ns after the acknowledge signal is received. At the end of the transfer, the DMA deactivates the DMA acknowledge line.

7.2.2 Data Separator

The data separator helps complete data separation for the floppy disk drives. Incoming read data is separated into a data signal and a data window signal, as required by the 8272 for reading data.

The data separator also adjusts precompensation on the write data stream, under the control of the floppy disk controller.

7.2.3 80186 Processor (DMA and Timer)

The 80186 processor has two DMA channels: a DMA request and a DMA controller. When the floppy disk controller activates the DMA request line connected to the DMA channel 0 request line, the request goes directly to the 80186 DMA controller. The DMA controller then determines how many bytes to transfer, and sets up address pointers to store the data.

The DMA controller does not notify the floppy disk controller that the last byte has been transferred. Instead, the DMA acknowledge line from the floppy disk controller is also connected to an 80186 timer. The timer in the 80186 has an input line assigned to monitor the DMA and has a timer-in and timer-out pin. At each DMA acknowledge, the timer's count is incremented by 1. When the counter reaches a value preset in the max count register A, the timer outputs a pulse on the timer-out pin, which is connected to the floppy disk controller terminal-count pin. This output (TC) signals the floppy disk controller to end requests for further DMA cycles. TC is issued to the FDC interface approximately 18 µs after the last DmaAck signal.

7.2.4 Interrupt Controllers

The IOP contains three interrupt controllers: a slave interrupt controller, a master interrupt controller, and the 80186 interrupt controller. When an interrupt occurs, the floppy disk controller sends an interrupt signal to the slave interrupt controller; slave interrupts are then funneled into one interrupt line, which becomes one input to the 8259 master. All master interrupts are finally funneled into one interrupt pin on the 80186.

7.2.5 Control Register

Twelve bits in the IOP control register are used in the floppy disk subsystem. Seven bits control floppy disk drive signals; that is, drive motor function, the "in-use" line on the drive interface, and drive selection. Four bits control the data rate expected by the data separator and data separator precompensation. One bit (not indicated on the figure) enables timer 1 for TC signal generation.

7.2.6 Buses

Commands are written to the 8272 via the Data Bus A, which receives data through a data buffer from a data/address bus.

7.3 Programmer Interface

This section describes the floppy disk controller registers and associated registers, interrupts, and reset. Diskette format is described at the end of the section.

7.3.1 Registers

The floppy disk controller holds a status register and a data register. The status register provides information regarding the floppy controllers current status. The data register is the location for reading data, I/O result status, or writing data and commands.

The DMA data register accesses the floppy disk controller data register via the DMA channel. Timer registers hold preset count data and record DMA accesses. Finally, eleven bits on the IOP control register affect the floppy disk controller. The registers are discussed in the following subsections.

Table 7.5 lists the floppy disk controller registers and addresses. The registers listed in brackets are external to the floppy disk controller.

Table 7.5. Registers and Addresses

Register Name	Address
Status	50H
Data	52H
[DMA Data]	54H
[IOP Control]	[80H]

7.3.1.1. Floppy Disk Controller Registers

The floppy disk controller has a status register and a data register, selected by signal A0. A0 high designates a data register; A0 low designates a status register.

Status register

The floppy disk controller sets the status register bits prior to the command and result phase. Figure 7.7 illustrates the floppy disk controller status register. Each address is described below: the bit reference name is given in parentheses after each bit.

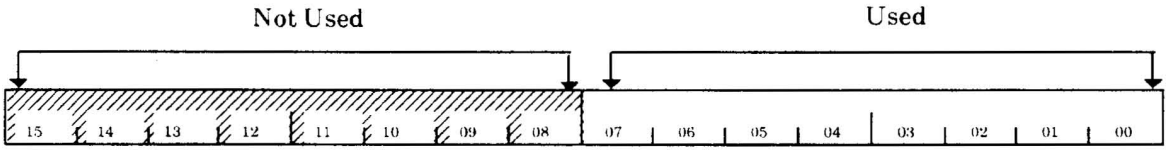

Figure 7.7. FDC status register (read only I/O Addr = 50 hex)

Bit 0 (D0B) When set, indicates Drive 0 is doing a seek.

Bit 1 (D1B) When set, indicates Drive 1 is doing a seek.

Bit 2 (D2B) When set, indicates Drive 2 is doing a seek.

Bit 3 (D3B) When set, indicates Drive 3 is doing a seek.

Bit 4 (CB) When set, indicates that the floppy disk controller is doing a read or write operation for the the floppy disk.

Bit 5 (NDM) When set, indicates that the floppy disk controller is in non-DMA mode. This bit is only valid during the execution phase of an operation.

Bit 6 (DIO) Indicates the direction of the next access of the data register, as follows:
0 = data is written to the data register. When a command byte is issued, the DIO bit is 0, indicating that a transfer occurred from the 80186 to the floppy disk controller data register.

1 = data is read from the data register. When a status byte is read, the DIO bit is 1, indicating that a transfer occurred from the floppy disk controller to the 80186. Note: In both cases, bit 7 (RQM) is 1.

Bit7 (RQM) When set, indicates that the floppy disk controller is ready to accept a byte from the 80186 or is ready to have a byte read by the 80186.

The status register may be read at any time. The operations necessary to obtain status are done by the floppy disk controller asynchronously to any processor functions. Therefore, the main status register should be checked prior to issuing any command byte or obtaining any result bytes for an I/O. Bits 6 and 7 (DIO and RQM) should also be checked to ensure that the floppy disk controller will move data in the correct direction.

If multiple reads or writes to the floppy disk controller are done in rapid succession, then a delay of at least 12 microseconds is necessary from the end of a command or result byte access. This delay allows the floppy disk controller to change the RQM bit from 1 to 0. The status register should not be read during this time because the RQM bit will erroneously indicate that the floppy disk controller is ready. After this delay, the software can continue to read the status register for the next access.

Data register

The 8-bit data register is the location for reading or writing commands, status, and data.

The floppy disk controller executes the following commands through this register:

Read: data, deleted data, a track, ID
Write: data, deleted data
Format a track
Scan: equal, low or equal, high or equal
Recalibrate
Sense: interrupt status, drive status
Specify
Seek
Invalid

Each command involves: 1) multi-byte transfers from the 80186 to the floppy disk controller for command information and 2) multi-byte transfers from the floppy disk controller to the 80186 for result information.

Each command can generally be considered as having three phases: command, execution, and result. However, not all operations have all three phases. For example, commands such as seek and recalibrate have only command and execution phases. Instead of a result phase, a sense interrupt status command must be issued to the floppy disk controller.

The execution phase always begins after the floppy disk controller receives the last command byte. The floppy disk controller then executes the requested command. When execution is completed, the

floppy disk controller interrupts the 80186 to indicate the beginning of the result phase.

Appendix B provides the command instruction sets and timing for the command phases.

7.3.1.2. DMA Registers

The 80186 integrated DMA controller handles all data transfers for read, write, or format operations. Channel 0 of the 80186 DMA controller is dedicated to the floppy disk subsystem.

Table 7.6 lists the name and address of the DMA registers that affect the floppy disk subsystem. Each register is word length and is located in the 80186 processor. The function and use of each register is discussed in Section 2, titled I/O Processor.

Table 7.6. DMA Registers

Register Name	Register Address
Control Word	$FFCAH
Transfer Count	$FFC8H
Destination Pointer (Upper 4 bits)	$FFC6H
Destination Pointer	$FFC4H
Source Pointer (Upper 4 bits)	$FFC2H
Source Pointer	$FFC0H

The DMA registers must be set up and enabled before command bytes are issued to the floppy disk controller. This initialization readies the DMA for the execution phase.

When the floppy disk controller begins a read or write operation, it requests DMA cycles until it reaches the end of the track or the cylinder. However, if the terminal count (TC) signal becomes active, the active signal is sent to the floppy disk controller to indicate that the required amount of data has been transferred. The floppy disk controller then halts activity.

Note: The 80186 DMA controller does not supply a TC signal. The DMA acknowledge line is connected to an 80186 integrated timer as well as to the DMA controller. When the requested number of DMA cycles have been completed, the 80186 timer 1 counts DMA cycles and provides a signal on the TC signal line.

7.3.1.3. Timer Registers

Timer 1 in the 80186 counts DMA cycles and provides the TC signal. Timer 1 must be initialized prior to starting the DMA or floppy disk controller.

The timer output line must also be enabled onto the floppy disk controller TC line. Enabling is done by setting bit 11 in the IOP control register to 1.

Maximum count register A is preprogrammed for the value that will stop DMA requests.

Table 7.7 lists the registers and addresses of the timer. The function and use of each register is discussed in Volume I in Intel's Microsystem Components Handbook.

Table 7.7. Timer Registers

Register Name	Register Address
Count Register	$FF58H
Max Count Register A	$FF5AH
Max Count Register B	$FF5CH
Control Register	$FF5EH

7.3.1.4. IOP Control Register

Several bits in the IOP control register (80H) must be set or reset prior to floppy disk operations. Since this write-only register may not be read, an image of what was written into the register should be maintained in memory.

Figure 7.8 illustrates the IOP control register as applied to floppy disk functions. The register bits are described below.

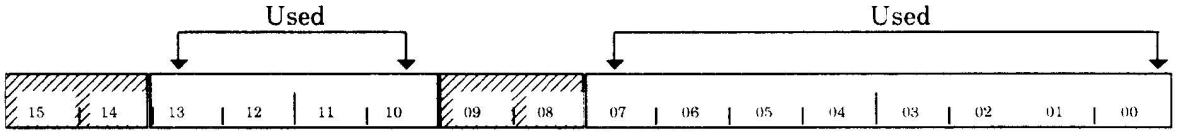

Figure 7.8. IOP control register (I/O write-only address = 80 hex)

Bit 13:
FddMotorOn — Turns on the floppy disk drive (FDD) drive motor for all drives, as follows:

0 = FDD drive motors for all drives are shut off
1 = FDD drive motors for all drives are turned on

A 500 ms delay must be allowed before reading and writing.

For maximum motor life, deactivate this line if immediate disk activity is required.

Bit 12:
FddInUse — Controls the "in use" interface line, as follows:

0 = in use to inactive
1 = in use to active

Bit 11:
AllowTmrTC — Enables timer 1 output so that it may be used to generate the TC signal to the floppy disk controller.

Bit 10:
High/Low' — Controls the speed of the floppy disk drive (for SA475 high-speed drives only), as follows:

0 = high speed (360 RPM)
1 = low speed (300 RPM)

Bits 7-4:
DriveSel4 - DriveSel1 — Control the drive select lines for the four possible drives. When a DriveSel bit is set to 1, the respective drive will be selected. These lines should be set prior to any disk operation, and should be reset after all disk activity is completed. Software should ensure that only one drive select is set active at any given time. More than one active drive select line will cause a conflict on the drive interface.

Bit 3:
5H/8L — Controls the data rate that the data separator will use on data transfers, as follows:

0 = 500 kb/s (SA475 at high speed only)
1 = 250 kb/s

Bits 2-0:
Precomp 2-0 — Control the amount of write precompensation that the data separator will use during write operations. Precomp2 is the most significant bit; Precomp0 is the least significant bit.

At high speed, precompensation can be set in increments of 62.5 ns. At low speed, precompensation can be set in increments of 125 ns.

For SA455, SA465, and SA475 (at low speed), precompensation should be set at 250 ns; that is, Precomp2-0 set to 0,1,0, respectively.

For SA475 at high speed, precompensation should be set to 125 ns; that is, Precomp2-0 set to 0,1, respectively.

7.3.2 Interrupts

Interrupts from the floppy disk controller are generated by:

1) completion of a read, write command at the beginning of the result phase;

2) the end of an asynchronous command (seek, recalibrate, etc);

3) an abnormal termination.

The two interrupt causes are differentiated by the floppy disk controller busy bit in the status register. If the bit is 0, then the interrupt was caused by an asynchronous event. If the bit is 1, then the interrupt was caused by the result phase of a read or write command. In either case, the 80186 continues issuing Sense Interrupt commands after the interrupt is serviced in order to search for any hidden interrupts.

The floppy disk controller is capable of stacking up several interrupts internally, thus requiring the repeated Sense Interrupt commands. The sense interrupt command should be repeated until invalid command code (ST0 = 80H) is received. This command code indicates that all interrupts have been serviced.

7.3.3 Reset

The reset signal for the floppy disk subsystem is connected to bit 2 of the reset control register (C0H). This bit is cleared to activate the reset line. The reset line in turn is held active for at least 4 microseconds.

After reset, the floppy disk controller updates the drive status for all four possible drives and asserts the interrupt line. The reset routine issues Sense Interrupt commands until the floppy disk controller indicates that all status addresses have been read (ST0 = 80H). The routine then initializes the floppy disk controller with the Specify command.

7.3.4. Diskette Format

New floppy diskettes must be written or formatted by the controller with a fixed data pattern or format before any data can be stored on them. The controller does the formatting track by track. Formatting destroys any information that was previously on the diskette.

Figure 7.9 illustrates the floppy diskette format, and subsections following the figure describe the format.

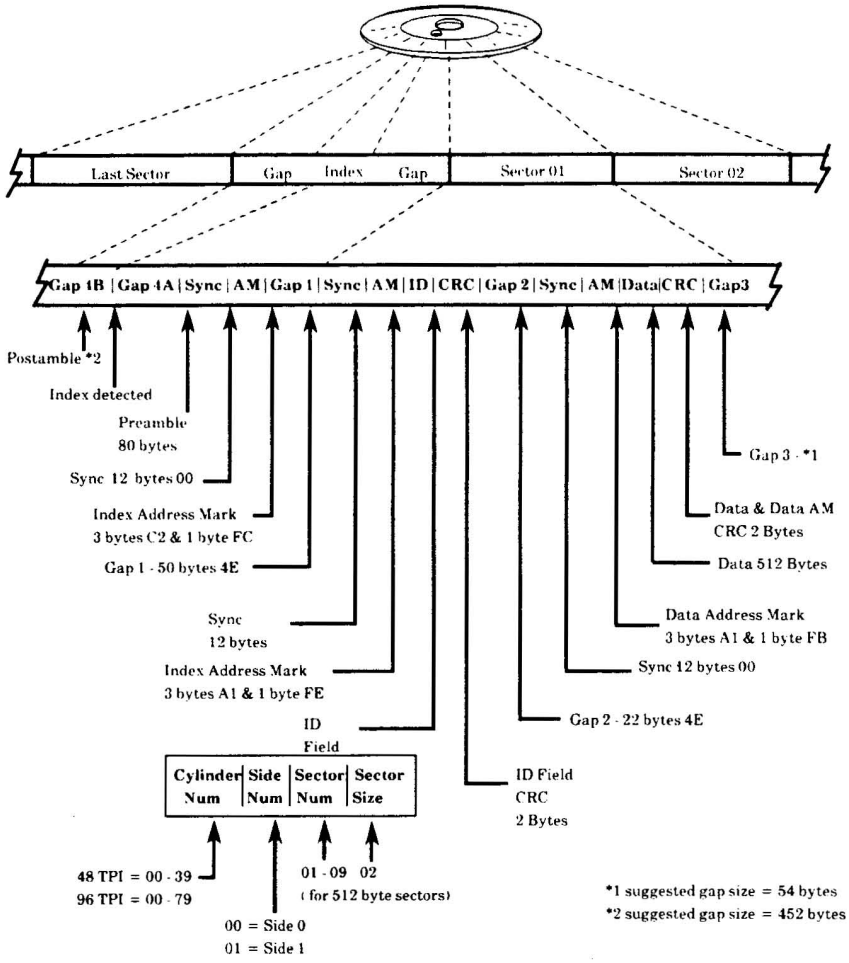

Figure 7.9. Floppy disk format

7.3.4.1. Preambles and Postambles

The sections of the diskette immediately before and after index hole detection are called the postamble and preamble, respectively. These diskette regions are written only at format time.

Preambles

The preamble gap begins at the index hole and consists of 80 bytes of 4EH. The gap is followed by 12 bytes of 00H that are collectively called the sync field. Data recovery circuits use this field to synchronize themselves for the upcoming address mark information.

The address mark immediately follows the sync field. Composed of three bytes of C2H and 1 byte of FCH, this address mark indicates the beginning of a data track. The address mark is followed by 50 bytes of 4EH that generate another gap.

Postambles

The postamble immediately follows the last sector, extends to the point where the index hole is first detected, and is filled with a 4EH pattern.

7.3.4.2. Sectors

A 360 Kbyte diskette has nine sectors/track; a 1.2 Mbyte disktte has 15 sectors/track. Each sector has the following ten divisions:

1) Each sector begins with twelve bytes of 00H as a sync field.

2) The sync field is followed by a 4 byte ID address mark that indicates the beginning of the sector ID information. The ID address mark is composed of three bytes of A1H and 1 byte of FEH. The address mark is followed by the ID field for that particular sector.

3) The ID field contains four bytes. The first byte indicates the cylinder on which the sector resides. The second byte indicates the side of the diskette on which the sector resides. The third byte indicates the sector number: 01H for sector 1, 02H for sector 2, and so on. The last byte indicates the number of data bytes in the sector. This byte is set to 02H to indicate 512 bytes per sector.

4) The ID field is followed by a two byte CRC field. These two bytes are the accumulated CRC over the ID field.

5) The ID field CRC is followed by a gap of 22 bytes of 4EH. The gap separates the ID information from the data information.

6) The sync field consists of 12 bytes of 00H. The field is used by the phase locked loop to synchronize itself for the upcoming data address mark information.

7) The address mark immediately follows the sync field and is composed of three bytes of A1H and 1 byte of FBH. The mark is used to indicate the beginning of the data section.

8) The next section is the actual data section.

9) A two-byte CRC follows. The CRC is accumulated over the data field and the data address mark.

10) Another gap follows the CRC field. This gap is 54 bytes of 4EH at format time and separates the end of the current sector from the beginning of the next sector.