2. I/O Processor
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2. I/O Processor and Related Components

The I/O processor is based on the 8 MHz Intel 80186 microprocessor and uses a traditional microprocessor bus architecture.

As discussed in section 1, the IOP subsystem includes a rigid disk controller and a floppy disk controller for file storage, an Ethernet controller and two serial channels for communication, and a keyboard/mouse controller. On-board memory consists of 16 Kbytes of EPROM and 16 Kbytes of RAM. An expansion bus is provided so that other workstation I/O requirements can be met by means of option boards. Figure 2.1 illustrates how the I/O processor relates to the overall IOP subsystem.

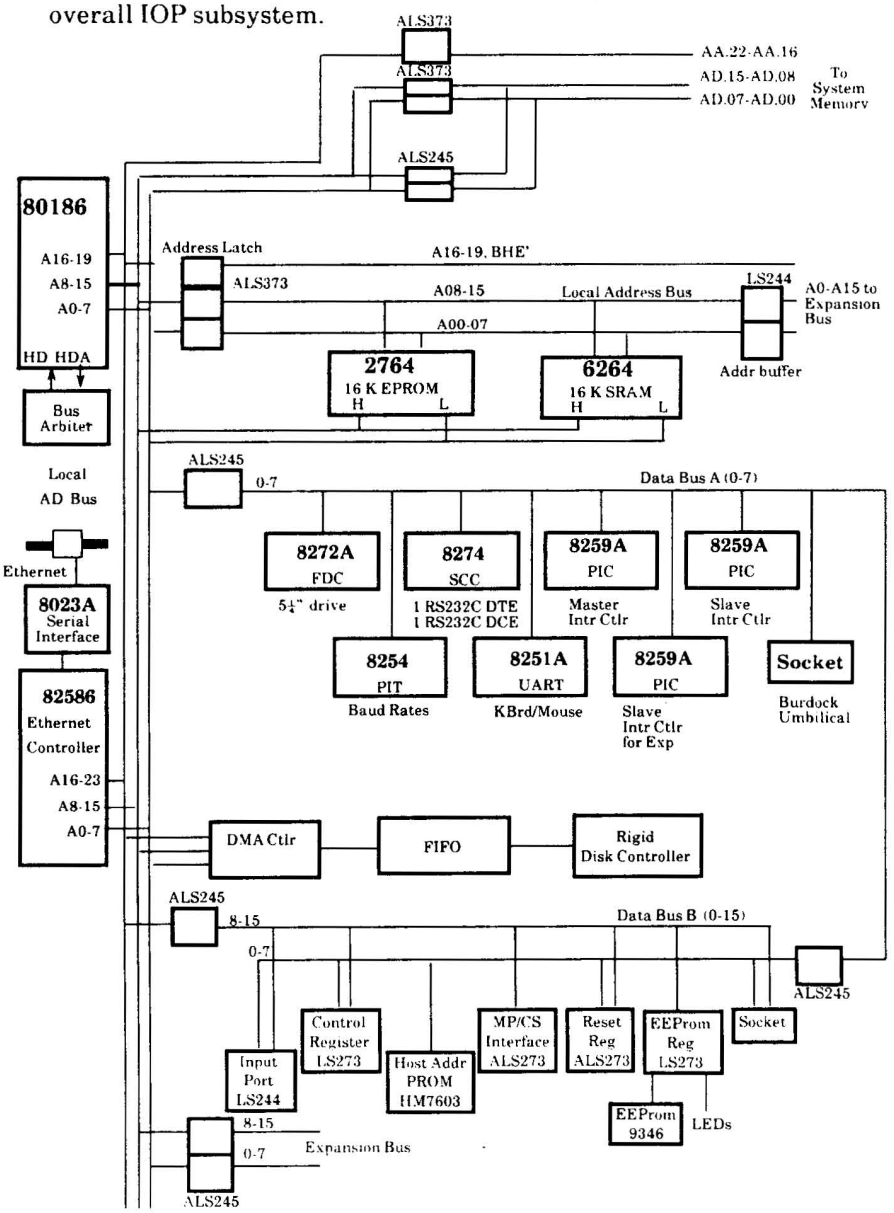

Figure 2.1. I/O subsystem block diagram

Other features of this subsystem:

- access to its local memory as well as to the main system memory via an external memory controller
- fully interrupt driven
- extended structure through additional option slots
- three external bus masters supported
- control and communication with the Mesa processor
- read and write of the Mesa processor programmable control store

2.1 Hardware

The I/O processor subsystem hardware consists of an 80186 microprocessor chip, buffers, local memory, interrupt controllers, and a non-maskable interrupt. The following subsections describe the physical hardware. For schematic drawings, refer to Appendix D.

2.1.1 Chip and Chip Socket

Figure 2.2 illustrates the top view of the 80186 chip. Because it is a 68-pin, leadless, JEDEC type chip carrier, it requires a special socket. Figure 2.3 illustrates the pin-outs of the socket.

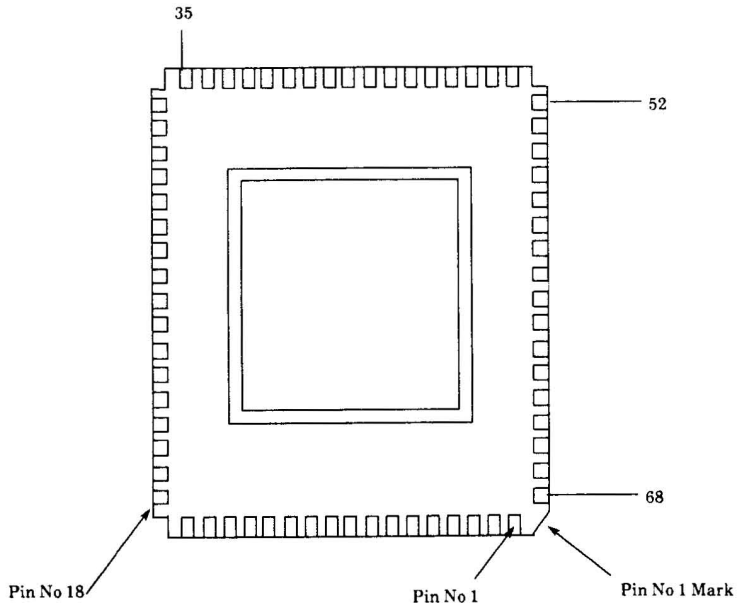

Figure 2.2. 80186 chip (top view)

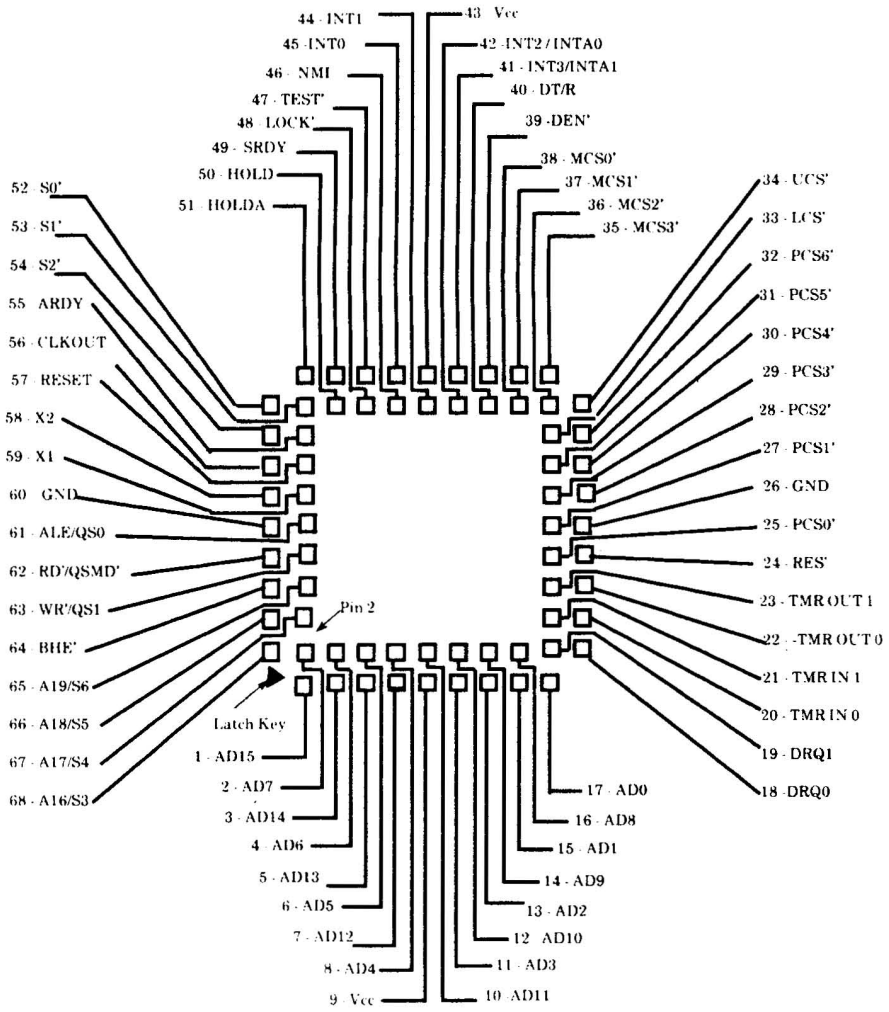

Figure 2.3. 80186 socket pin-outs (top view)

2.1.2 Pin Assignments and Description

Figure 2.4 illustrates the 80186 chip. For convenience, the chip is broken into five sections. The key in the left hand corner corresponds to the five blocks. Table 2.1 lists the pins and signals and describes their function.

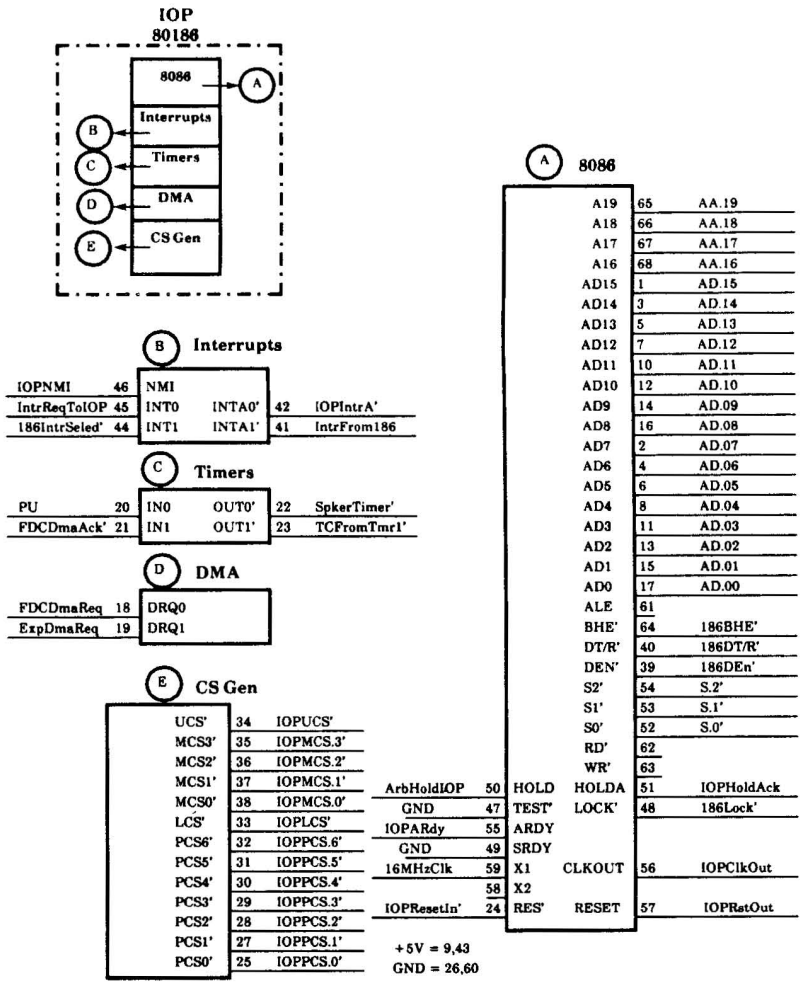

Figure 2.4. 80186 pins and signals

Table 2.1 80186 Pin Assignment

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Symbol	Function
RESET	Reset output indicates that the 80186 CPU is being reset, and can be used as a system reset. It is active high, synchronized with the processor clock and lasts an integer number of clock periods corresponding to the length of the RES' signal.
X1, X2	Crystal inputs, X1 and X2, provide an external connection for a fundamental mode parallel resonant crystal for the internal crystal oscillator. X1 interfaces to an external clock instead of a crystal. In this case, minimizes the capacitance on X2 or drive X2 with complemented X1. The input or oscillator frequency is internally divided by two to generate the clock signal (CLKOUT)
CLKOUT	Clock Output provides the system with a 50% duty cycle waveform. All device pin timings are specified relative to CLKOUT.
RES'	System Reset causes the 80186 to immediately terminate its present activity, clear the internal logic, and enter a dormant state. This signal may be asynchronous to the 80186 clock. The 80186 begins fetching instructions approximately seven clock cycles after RES' is returned high. RES is required to be low for greater than 4 clock cycles and is internally synchronized. For proper initialization, the low to high transition of RES' must occur no sooner than 50 microseconds after power up. This input is provided with a Schmitt-trigger to facilitate power-on RES' generation via an RC network. When RES' occurs, the 80186 will drive the status lines to an inactive level for one clock, and then tri-state them.

- more -

Table 2.1 80186 Pin Assignment (continued)

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Symbol	Function
TEST'	TEST' is examined by the wait instruction. If the TEST' input is high when wait execution begins, then instruction execution suspends. TEST' is resampled until it goes low, at which time execution will resume. If interrupts are enabled while the 80186 is waiting for TEST', then they are serviced. This input is synchronized internally.
TMR IN 0, TMR IN1	Timer inputs are used either as clock or control signals, depending upon the programmed timer mode. These inputs are active high (or low-to-high transitions are counted) and internally synchronized.
TMR OUT 0, TMR OUT1	Timer outputs provide single pulse or continuous waveform generation, depending upon the timer mode selected.
DRQ 0 DRQ 1	DMA Request is driven high by an external device when it desires a DMA channel (Channel 0 or 1) to perform a transfer. These signals are active high, level-triggered, and internally synchronized.
NMI	Non-Maskable interrupt is an edge-triggered input which causes a type 2 interrupt. NMI is not maskable internally. A transition from a low-to-high initiates the interrupt at the next instruction boundary. NMI is latched internally. An NMI duration of one clock or more will guarantee service. This input is internally synchronized.
INT0 INT1 INT2/INTA0' INT3/INTA1'	Maskable Interrupt Request are requested by strobing one of these pins. When configured as inputs, these pins are active high. Interrupt requests are synchronized internally. INT2 and INT3 may be configured via software to provide active-low interrupt-acknowledge output signals. All interrupt inputs may be configured via software to be either edge- or level-triggered. To ensure recognition, all interrupt requests must remain active until the interrupt is acknowledged. When iRMX mode is selected, the function of these pins changes (see section 2.3.1.4).
A19/S6, A18/S5, A17/S4, A16/S3	Address bus outputs (16-19) and bus cycle status (3-6) reflect the four most significant address bits during T1. These signals are active high during T2, T3, Tw, and T4. Status information is available on these lines as encoded below: **Low** **High** S6 Processor Cycle DMA Cycle S3, S4, and S5 are defined as low during T2-T4.
AD15-AD0	Address/Data Bus (0-15) signals constitute the time multiplexed memory or I/O address (T1) and data (T2, T3, TW, and T4) bus. The bus is active high. A0 is analogous to BHE' for the lower byte of the data bus, pins D7 through D0. It is low during T1 when a byte is to be transferred onto the lower portion of the bus in memory or I/O operations.
BHE'/S7	During T1, use the Bus High Enable signal to determine if data is to be enabled onto the most significant half of the data bus pins D15-D8. BHE' is low during T1 for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the higher half of the bus. The S7 status information is available during T2, T3, and T4. S7 is logically equivalent to BHE'. The signal is active low, and is tri-stated off during bus HOLD. **BHE' and A0 Encodings** BHE' Value / A0 Value / Function 0 / 0 / Word transfer 0 / 1 / Byte transfer on upper half of data bus (D15-D08) 1 / 0 / Byte transfer on lower half of data bus (D07-D00) 1 / 1 / Reserved
ALE/QS0	Address Latch Enable/Queue Status 0 is provided by the 80186 to latch the address into the address latches. ALE is active high. Addresses are guaranteed to be valid on the trailing edge of the ALE. The ALE rising edge is generated off the rising edge of the CLKOUT immediately preceding T1 of the associated bus cycle, effectively one-half clock cycle earlier than in the standard 8086. The trailing edge is generated off the CLKOUT rising edge in T1 as in the 8086. Note that ALE is never floated.
WR'/QS1	Not used.
RD'/QSMD'	Not used.

- more -

Table 2.1 80186 Pin Assignment (continued)

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Symbol	Function
ARDY	Asynchronous Ready informs the 80186 that the addressed memory space or I/O device will complete a data transfer. The ARDY input pin will accept an asynchronous input and is active high. Only the rising edge is internally synchronized by the 80186. This means that the falling edge of ARDY must be synchronized to the 80186 clock. If connected to Vcc, then no Wait states are inserted. Asynchronous ready (ARDY) must be active to terminate a bus cycle.
SRDY	Not used and tied low.
LOCK'	LOCK' output indicates that other system bus masters are not to gain control of the system bus while LOCK' is active low. The LOCK' signal is requested by the LOCK' prefix instruction and is activated at the beginning of the first data cycle associated with the instruction following the LOCK prefix. No prefetches occur while LOCK' is asserted. LOCK' is active low, is driven high for one clock during Reset, and then floated.
S0', S1', S2'	Bus cycle status S0'-S2' are encoded to provide bus transaction information, as follows: S2' S1' S0' Bus Cycle Initiated 0 0 0 Interrupt Acknowledge 0 0 1 Read I/O 0 1 0 Write I/O 0 1 1 Halt 1 0 0 Instruction Fetch 1 0 1 Read Data from Memory 1 1 0 Write Data to Memory 1 1 1 Passive (no bus cycle) The status pins float during HOLD. S2' may be used as a logical M/IO' indicator, and S1' as a DT/R' indicator. The status lines are driven high for one clock during reset, and then floated until a bus cycle begins.
HOLD (input) HLDA (output)	HOLD indicates that another bus master is requesting the local bus. The HOLD input is active high. HOLD may be asynchronous with respect to the 80186 clock. The 80186 issues a HLDA (high) in response to a HOLD request at the end of T4 or T1. Simultaneously with the issuance of HLDA, the 80186 floats the local bus and control lines. After HOLD is detected as being low, the 80186 lowers HLDA. When the 80186 needs to run another bus cycle, it again drives the local bus and control lines.
UCS'	Upper Memory Chip Select is an active low output whenever a memory reference is made to the defined upper portion (1K-256K block) of memory. This line is not floated during bus HOLD. The address range activating UCS' is software programmable.
LCS'	Lower Memory Chip Select is active low whenever a memory reference is made to the defined lower portion (1K-256K) of memory. This line is not floated during bus HOLD. The address ranges activating LCS' are software programmable.
MCS0'-3'	Mid-Range Memory Chip Select are active low when a memory reference is made to the defined mid-range portion of memory (8K–512K). These lines are not floated during bus HOLD. The address ranges activating MCS0'-3 are software programmable.
PCS0'-PCS3' PCS4'-PCS7'	Peripheral Chip Select signals 0-7 are active low when an I/O reference is made to the defined peripheral area (64 Kbyte I/O space). These lines are not floated during bus HOLD. The address ranges activating PCS0'-7' are software programmable.
DT/R'	Data Transmit/Receive controls the direction of data flow through the external data bus transceiver. When low, data is transferred to the 80186. When high, the 80186 places write data on the data bus.
DEN'	Data Enable is provided as a data bus transceiver output enable. DEN' is active low during each memory and I/O access. DEN' is high whenever DT/R' changes state.

2.2 Theory of Operations

The Intel 80186 shares a common base architecture with the 8086/88 and is completely object code compatible. Six other separate functional blocks are integrated into the 80186.

Figure 2.5 illustrates the basic components of the 80186 microprocessor; the number in the lower right hand corner of each block corresponds to the subsection in which the component is described.

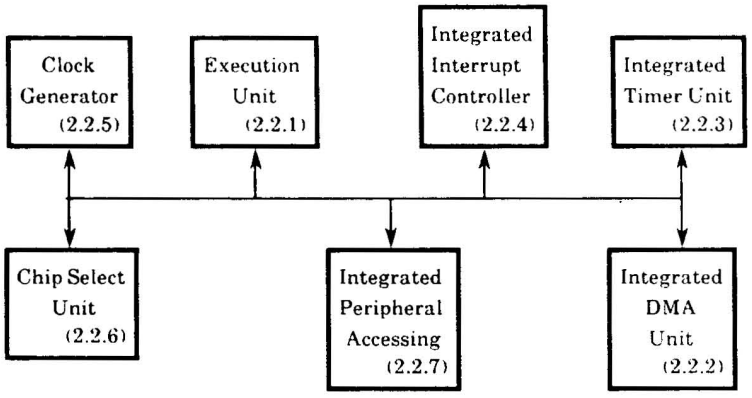

Figure 2.5. 80186 block diagram

2.2.1 Execution Unit

Architectural features of the 80186 CPU are:

- four 16-bit general purpose registers (AX, BX, CX, DX) which may be used as operands in most arithmetic operations in either 8 or 16 bit units.
- four 16-bit 'pointer' registers (SI, DI, BP, SP) which may be used in arithmetic operations and in accessing memory based variables.
- four 16-bit segment registers (CS, DS, SS, ES) which allow simple memory partitioning to aid construction of modular programs.
- one 16-bit instruction pointer and one 16-bit status register.
- one 16-bit ALU which performs 8- or 16-bit arithmetic and logical operations. The ALU makes data movement among registers, memory and I/O space possible.
- the CPU allows high speed data transfer from one area of memory to another, using string move instructions; and to or

from I/O ports and memory using block I/O instructions. The CPU also provides a wealth of conditional branches and other control instructions.

Figure 2.6 illustrates the layout of the 16-bit registers.

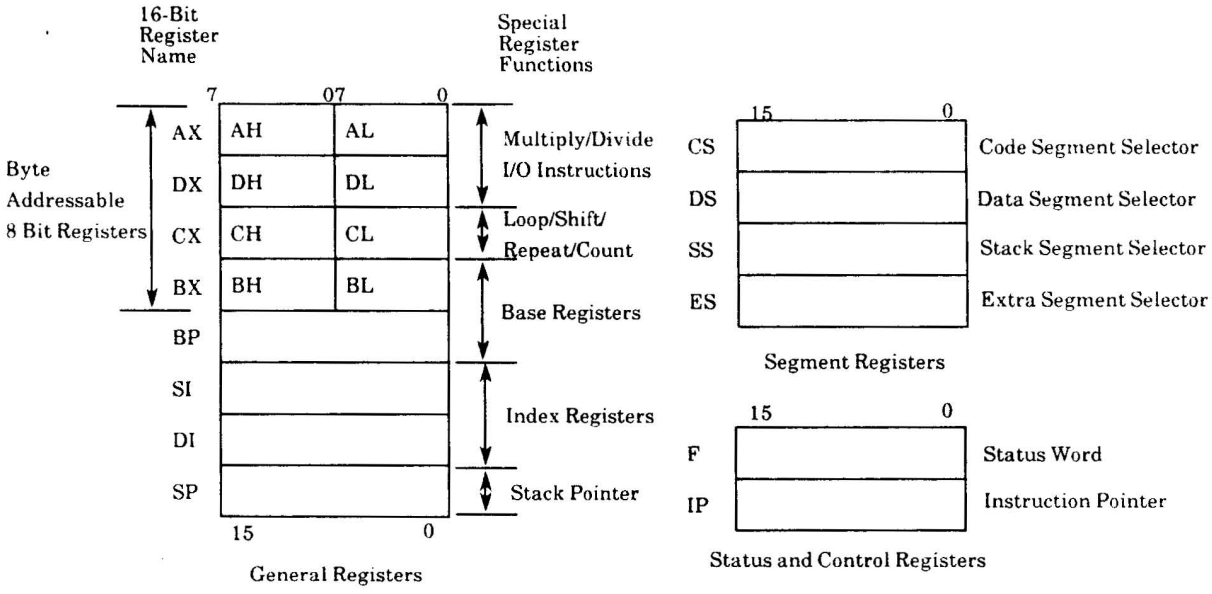

Figure 2.6. 80186 registers

2.2.2 Integrated DMA Unit

The DMA unit, as illustrated in Figure 2.7, provides two high speed DMA channels. In the IOP, DMA channel 0 is used for accessing the floppy disk. DMA channel 1 is provided to the expansion channel for option boards.

This unit performs transfers to or from any combination of I/O space and memory space in either byte or word units. Every DMA cycle requires two to four bus cycles: one or two to fetch the data to an internal register, and one or two to store the data. The cycles allow word data to be located on odd boundaries or byte data to be moved from odd locations to even locations.

Each DMA channel maintains independent 20-bit source and destination pointers that access the source and destination of the data transferred. The pointers may independently address either I/O or memory space. After each DMA cycle, the pointers are independently incremented, decremented, or maintained constant. Each DMA channel also maintains a transfer count that terminates a series of DMA transfers after a pre-programmed number of transfers.

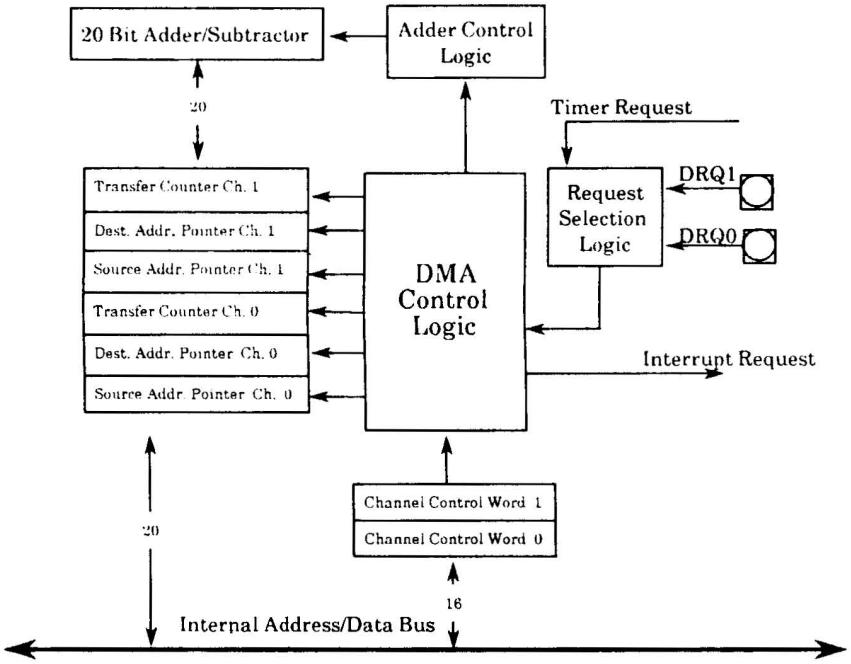

Figure 2.7. Integrated DMA unit

2.2.3 Integrated Timer Unit

The timer unit contains three independent 16-bit timer/counters. In the IOP, Timer 0 generates speaker waveforms. Timer 1 generates terminal count signals for the floppy disk DMA.

The third timer is reserved for operating system use and counts only CPU clocks. It interrupts the CPU after a programmable number of CPU clocks.

Figure 2.8 illustrates the timer unit.

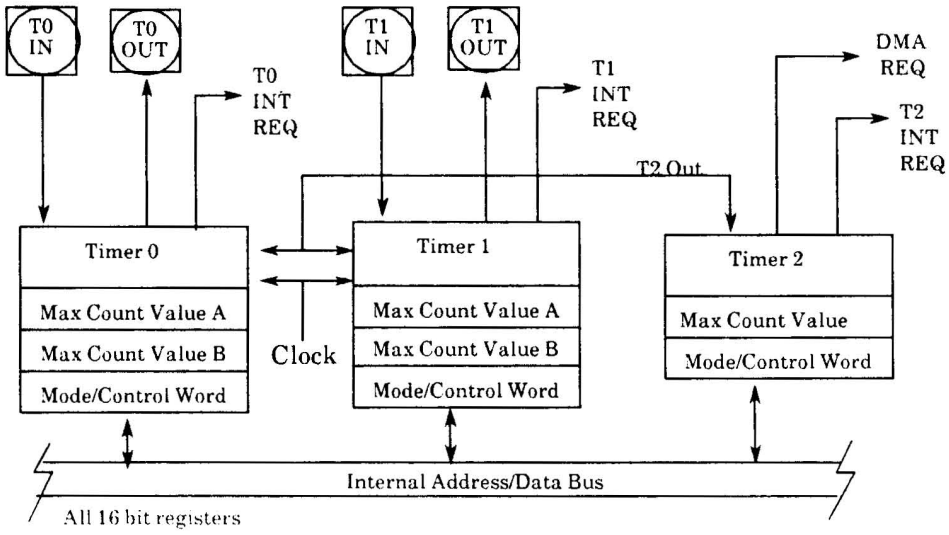

Figure 2.8. Timer unit block diagram

2.2.4 Integrated Interrupt Controller

The interrupt controller arbitrates interrupt requests among all internal and external sources. It is configured as a slave controller to an external interrupt controller; that is, it operates in iRMX mode. For further information on interrupts, see Section 3.

Figure 2.9 illustrates the interrupt controller.

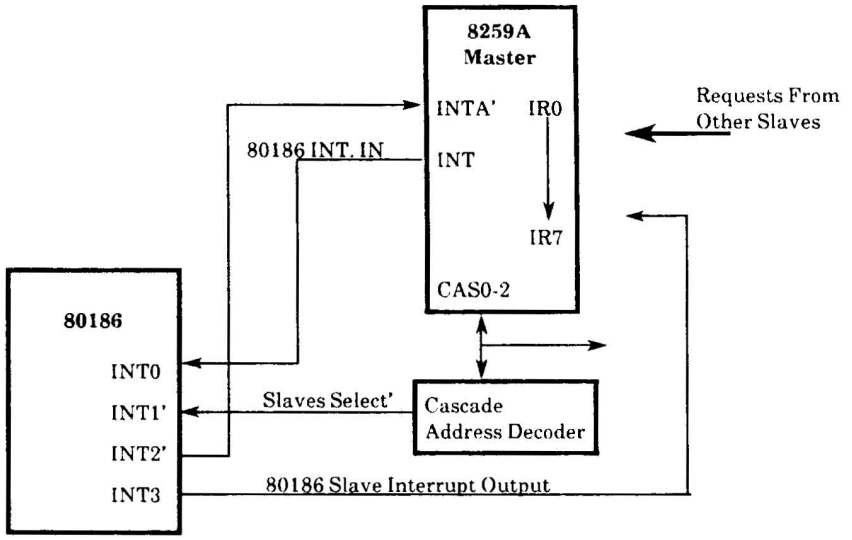

Figure 2.9. Integrated interrupt controller

2.2.5 Clock Generator

The 80186 has a built-in clock generator which includes an external 16 MHz oscillator as the input clock. The input clock signal is internally divided by two to provide the 50 percent duty cycle CPU clock from which all 80186 system timing derives.

All 80186 timing parameters are referenced to this externally available CPU clock. The clock generator also provides ready synchronization for the processor.

2.2.6 Chip Select Unit

Integrated chip select logic enables memory or peripheral devices. Six output lines address memory and seven output lines address peripherals.

The memory chip select lines are split into three groups for separately addressing the major memory areas in a typical 8086 system: upper memory for reset ROM, lower memory for interrupt vectors, and mid-range memory for program memory. The size of each of these regions is user programmable.

Seven peripheral select lines address one of the seven contiguous 128 byte blocks above a programmable base address. This base address is located at location 0 in I/O space.

The programmed chip select areas are associated with a set of programmable ready bits. The bits control an integrated wait state generator. The generator allows a programmable number of wait states (0 to 3) to be automatically inserted whenever an access is made to the area of memory associated with the chip select area. In addition, each set of ready bits includes a bit that determines whether the external ready signals (ARDY and SRDY) will be used or ignored.

2.2.7 Integrated Peripheral Accessing

The integrated peripheral and chip select circuitry is controlled by sets of 16-bit registers that are accessed using standard input, output, or memory access instructions. These peripheral control registers are located within a 256 byte block area called the peripheral control block. Because they are accessed exactly as if they were external devices, no new instruction types are required to access and control the integrated peripherals.

Figure 2.10 illustrates the integrated peripheral registers.

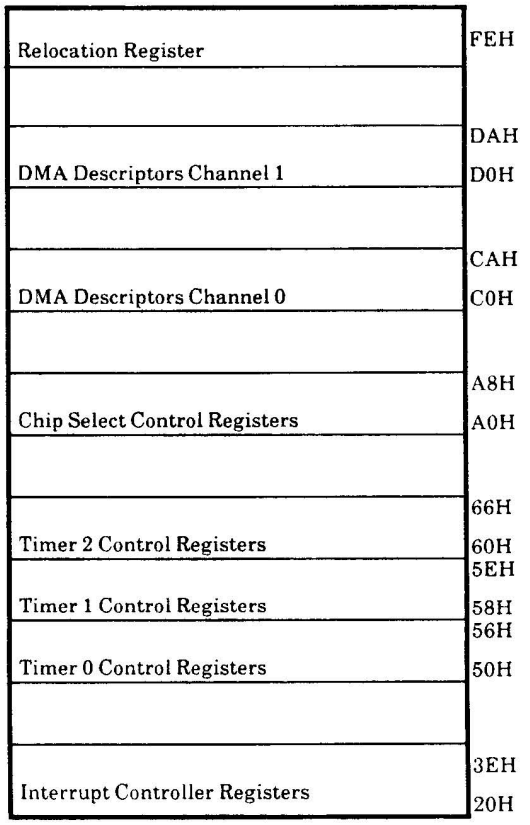

Figure 2.10. 80186 integrated peripheral control block

2.3 Programmer Interface

The following subsections describe the registers and internal programming of the 80186.

2.3.1 Processor Reset and Initialization

Processor initialization or startup begins when the RES' input pin is driven low. RES' forces the 80186 to terminate all execution and local bus activity. No instruction or bus activity occurs as long as RES' is active. After RES' becomes inactive and an internal processing interval elapses, the 80186 begins execution with the instruction at physical location FFFF0(H). RES' also sets some registers to predefined values, as shown in Table 2.2.

Table 2.2. 80186 Initial Register State after Reset

Name	Location
Status Word	F002(H)
Instruction Pointer	0000(H)
Code Segment	FFFF(H)
Data Segment	0000(H)
Extra Segment	0000(H)
Stack Segment	0000(H)
Relocation Register	20FF(H)
UMCS	FFFB(H)

The reset activities and initial states of various 80186 integrated controllers are described below.

2.3.1.1. Local Bus Controller and Reset

After receiving a reset pulse from the RES' input, the local bus controller performs the following actions:

1) Drives DEN', RD', and WR' high for one clock cycle, then floats. RD' is also provided with an internal pull-up device to prevent the processor from inadvertently entering queue status mode during reset.

2) Drives S0'-S2' to the passive state (all high) and then floats.

3) Drives LOCK' high and then float.

4) Tri-state AD0-15, A16-19, BHE' DT/R'.

5) Drives ALE low. ALE is never floated.

6) Drive HLDA low. If HOLD = H after RESET' = H, then HLDA will go high two clock cycles later.

2.3.1.2. Chip Select/Ready Logic and Reset

After reset occurs, the chip select/ready logic performs the following actions:

1) All chip select outputs are driven high.

2) After reset is cleared, the UCS' line is programmed to provide chip selects to a 1K block with the accompanying ready control bits at 011 to enable the maximum number (3) of internal wait states in conjunction with external Ready signal; that is, UMCS resets to FFFBH.

3) No other chip select or ready control registers have any predefined values after reset. They will not become active until the CPU accesses their control registers. Both the PACS and MPCS registers must be accessed before the PCS' lines become active.

2.3.1.3. DMA Channels and Reset

After reset occurs, the DMA channels perform the following actions:

1) The start/stop bit for each channel is reset to Stop.

2) Any transfer in progress is aborted.

2.3.1.4. Interrupt Controller and Reset

After reset occurs, the interrupt controller performs the following actions:

1) All special fully nested mode (SFNM) bits reset to 0, implying fully nested mode.

2) All priority bits (PR0-2) in the various control registers set to 1. This places all sources at the lowest priority. (level 111).

3) All level-trigger mode (LTM) bits reset to 0, resulting in edge-triggered mode.

4) All interrupt service bits reset to 0.

5) All interrupt request bits reset to 0.

6) All interrupt mask (MSK) bits set to 1 (mask).

7) All cascade (C) bits reset to 0 (non-cascade).

8) All priority mask (PRM) bits set to 1, implying no levels masked.

9) Initialized to non-iRMX 86 mode.

2.3.1.5. Timers and Reset

After reset, the timers perform the following actions:

1) All enable (EN) bits are reset, preventing timer counting.

2) All select (SEL) bits are reset to zero. This selects max count register A, resulting in the timer out pins going high upon reset.

2.3.2 Chip Select Address and Register Bit Maps

The IOP I/O controllers use the 80186 PCS lines. The PCS base addresses start at location 0H in the 80186 I/O space. Table 2.3 lists the addresses and shows the address contents.

Table 2.4 gives the IOP register bit maps. The table is self-explanatory.

Table 2.3. IOP I/O Controller Addresses: PCS0, PCS1, PCS4

The seven PCS lines are allocated as follows:

		Address	Uses
1 w.s.	PCS.0:	0 - 7FH	I/O Controllers
	PCS.1:	80 - FFH	Misc IOP I/O
	PCS.2:	100 - 17FH	PCE
	PCS.3:	180 - 1FFH	PCE
0 w.s.	PCS.4:	200 - 27FH	Rigid Disk/DMA
	PCS.5:	280 - 2FFH	unused
	PCS.6;	300 - 37FH	unused

Note :F8 to FFH reserved by Intel

PCS.0

Address (H)	Read (bits 7-0)	Write (bits 7-0)
8259A Master Intr Ctlr		
0	IRR,ISR	ICW1, OCW2, OCW3
2	IMR	ICW2, ICW3, ICW4, OCW1
8259A Slave Intr Ctlr		
10	IRR, ISR	ICW1, OCW2, OCW3
12	IMR	ICW2, ICW3, ICW4, OCW1
8254 Timer		
20	Timer Counter 0	Timer Counter 0
22	Timer Counter 1	Timer Counter 1
24	Timer Counter 2	Timer Counter 2
26	———	Timer mode
8251 Uart (Keyboard/Mouse)		
30	Uart Rx Data	Uart Tx Data
32	Uart Status	Uart Ctl Word
8274 RS232C Ctlr		
40	Ch A Rx Data	Ch A Tx Data
42	ChB Rx Data	Ch B Tx Data
44	Ch A Status	Ch A Cmd/Parm
46	Ch B Status	Ch B Cmd/Parm
8272A FDC		
50	FDC Main Status Reg	(illegal)
52	FDC Data Reg Stack	FDC Data Reg Stack
54	Dma Read from FDC	Dma Write to FDC
8259A Expansion Intr Ctlr		
60	IRR, ISR	ICW1, OCW2, OCW3
62	IMR	ICW2, ICW3, ICW4, OCW1
8255A-5 PIO	Debugger Interface	
70	PortA	Port A
72	Port B	Port B
74	Port C	Port C
76	(illegal)	Control Word

PCS.1

Address(H)	Read	Write
80	Input Port	Control Reg
90	Host Address PROM (90, 92, 94, 96, 98, 9A, 9C, 9EH)	Hex LED Display
A0	Clear Ring Latch	ENet Attn
B0	Clear Mesa Interrupt Latch	Mesa Processor /Control Store Reg
C0	Clear ENet Interrupt Latch	Reset Ctl Reg
D0	Clear Vertical Retrace Interrupt Latch	EEProm and LED Reg
E0	Reserved	Unused
F0	Arbiter Commands (F2H = HoldIOPCmd F4H = AllowRDCmd F8H = AllowPCCmd	Unused

PCS.4

200	NA	CR2-CR0 of 2942
202	CR2-CR0 of 2942	NA
204	DMA Word Counter* (Inside 2942)	NA
206	Addr Counter of 2942 (bits 8-1)	NA
208	NA	DMA Start Addr, bits 23-9, 0 and initialize 2942 counters
20A	NA	DMA start addr, bits 8-1 (counter inside 2942)
20C	NA	DMA Word Counter (counter inside 2942)
20E	NA	En Counters of 2942
210	DMA Status Reg	DMA Command Reg
212	unused	Preset FifoIn Bit 17
214	RDC Status Reg	RDC Control Reg
216	unused	Start DMA Command

NA = Not Available
* = in 2's complement form

Table 2.4. Register Bit Maps

	Read			Write				
	Input Port (80H)	Host Addr PROM (9xH)		Control Reg (80H)	LED (90H)	Mesa Proc/Control Store Reg (B0H)	Reset Control Reg (C0H)	EEProm Config Reg (D0H)
Bit 15				BlockSysMem'	LED digit 3	Control Store Wr Enable	Enable Ethernet Loopback	EEProm Data-in
Bit 14				EnSpker	LED digit 3	Control Store Load/Shift'	Enable Keyboard Loopback	
Bit 13	Data From Control Store (1 bit only)			FD Motor on	LED digit 3	ControlStore Buffer Enable	reserved	EEProm Clock
Bit 12				FD InUse	LED digit 3	Data To Control Store (1 bit only)	reserved	EEProm Enable
Bit 11	Data From Config EEProm (1 bit only)				LED digit 2	Control Store Shift Clock	reserved	reserved
Bit 10	RS232 Ch A DSR' (L active)			FD H = Low speed L = High Speed	LED digit 2	IOPRdNIA	Reset ExpansionChannel'	Diag LED3
Bit 9	RS232 Ch A Ring Indicator' (L active)			Sel RS232 DTE to use internal clock	LED digit 2	Halt Mesa Proc' (L active)	Reset Dma-FIFO'	Diag LED2
Bit 8	RS232 Ch B DTR' (Low active)			Enable RS232 Ch B to send clock signals	LED digit 2	Interrupt Mesa Processor	Reset RDC'	Diag LED1
Bit 7		↑		FD Drive Sel 3	LED digit 1		Reset PCE-80186'	
Bit 6	DBrk/Daisy	|		FD Drive Sel 2	LED digit 1		Reset Mesa Proc'	
Bit 5	SpareID'	Host Address		FD Drive Sel 1	LED digit 1		Reset Keyboard'	
Bit 4		PROM connected		FD Drive Sel 0	LED digit 1		Reset Burdock Ctlr 8255-5'	
Bit 3		to Bit 07-00		FD H = 5¼" L = 8"	LED digit 0		Reset Keyboard Uart 8251A'	
Bit 2		only		FD PreComp 2	LED digit 0		Reset FDCtlr 8272A'	
Bit 1		|		FD PreComp 1	LED digit 0		Reset RS232 Ctlr 8274'	
Bit 0		↓		FD PreComp 0	LED digit 0		Reset ENet Ctlr 82586'	