1. IOP Board
TABLE OF CONTENTS

1. IOP Board

The I/O subsystem is one of the major subsystems of the Dove workstation. The subsystem is common to both the Daisy and Daybreak implementations of the workstation.

1.1 Overview

Figure 1.1 illustrates the I/O subsystem, and shows its internal elements as well as its relationship to the system as a whole. This manual describes the elements that constitute the I/O subsystem.

The main functions of the I/O subsystem are:

- Controls all the I/O devices associated with the Dove workstation during system operation. With the exception of the bitmap display controller, all hardware associated with the peripheral devices is embodied in the I/O subsystem. All software that directly controls the I/O devices runs on the IOP. The display controller is programmed by the IOP, but most of the hardware associated with it is found outside the I/O subsystem.
- Controls the Mesa processor during power-up and initialization. The IOP is responsible for bringing the Mesa processor up to a functional state after the machine is powered up or booted. This process ensures that the various processor states are correctly initialized and then starts the Mesa processor.
- Writes and reads the Mesa processor control store. The write function initializes control store with microcode before the Mesa processor operates. The read function is primarily a diagnostic function that checks the correctness of control store.
- Provides the system booting function. This function is a multi-stage bring-up of the system using the boot files stored on one of several boot devices. The IOP runs the software that bootstraps from the raw machine to a fully-functional Dove workstation.
- Forms the basis of the diagnostic capability of the Dove workstation. Since the IOP can to some degree control all other subsystems, it can selectively exercise and diagnose problems in these subsystems.
- Provides the hardware and most of the software for the PC emulation function.
- Provides the framework by which optional devices can be attached to the Dove workstation. Control of the various options slots is exercised by the IOP.

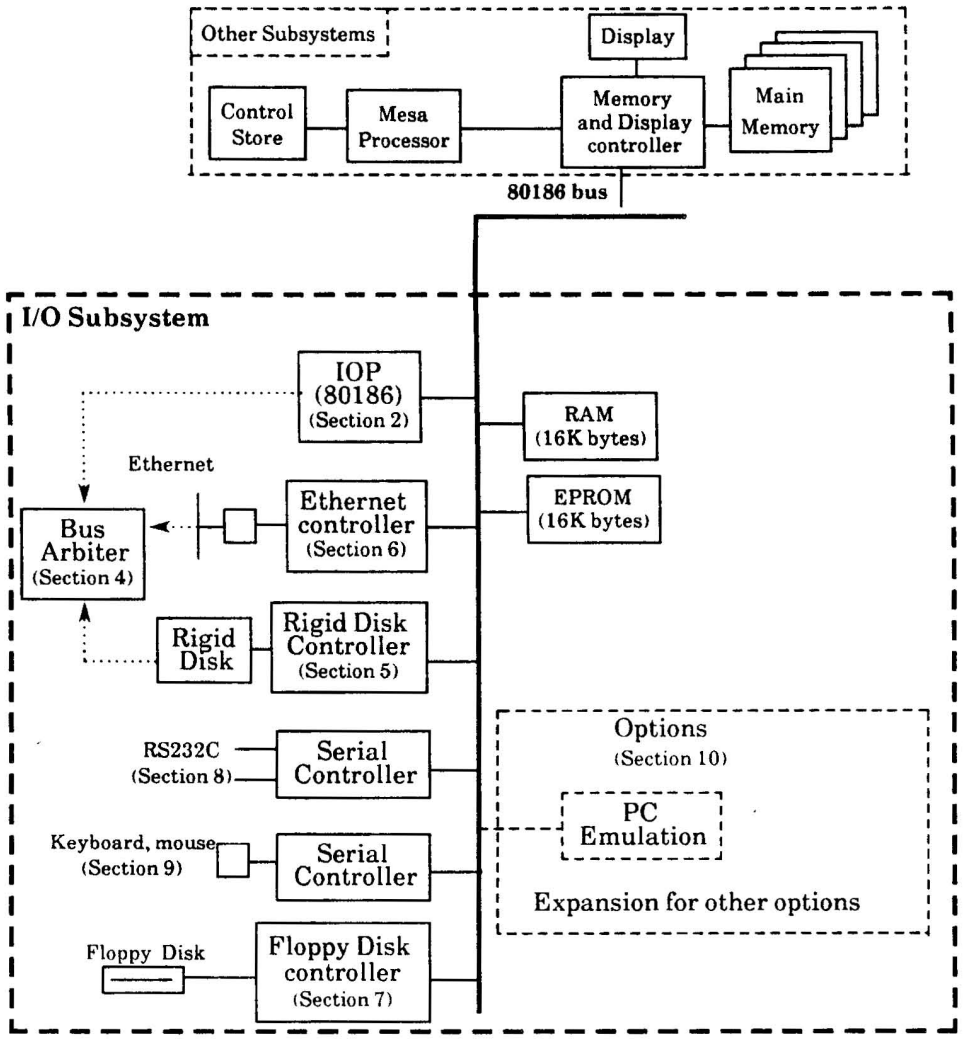


Figure 1.1. Dove workstation block diagram

The I/O subsystem is controlled by the I/O Processor (IOP), a commercial VLSI microprocessor. The subsystem has a traditional microprocessor bus architecture to which memory devices and I/O controllers can be connected. Except for the display controller, all Dove I/O devices interface to this bus. The devices include high speed devices like the Ethernet controller and rigid disk controller, medium speed devices like the floppy disk controller and serial communication controllers, and low speed devices like the keyboard and mouse controllers.

The microprocessor bus also extends to the Options slots, where additional peripheral controllers can be added.

The physical location of the IOP peripheral devices is as follows.

- The rigid disk drive is housed in the system unit.
- The floppy disk drive is located in a separate module on top of the system unit.

- The keyboard and mouse are located on the user's desktop near the display unit.
- The Ethernet transceiver is located at some remote distance from the system unit, typically in the area above the ceiling where the Ethernet cable is situated.
- The external I/O connections to the system unit are made at the rear of the system.

1.2 Hardware

All components of the I/O subsystem are common to both Daybreak and Daisy, and the board plugs into an identical backplane. The IOP electronics are housed in the system unit.

1.2.1 Printed Wiring Board Assemblies

I/O subsytem electronics are located on five printed wiring board assemblies (PWBAs): the 16" x 10.9" main IOP board with a 165-pin connector and a 96-pin connector; the 5" x 10.9" PCE Option board; and one to three 5" x 10.9" Options boards (Note: Daybreak supports only one option board). Figure 1.2 illustrates the locations of the I/O subsystem PWBAs on the backplane.

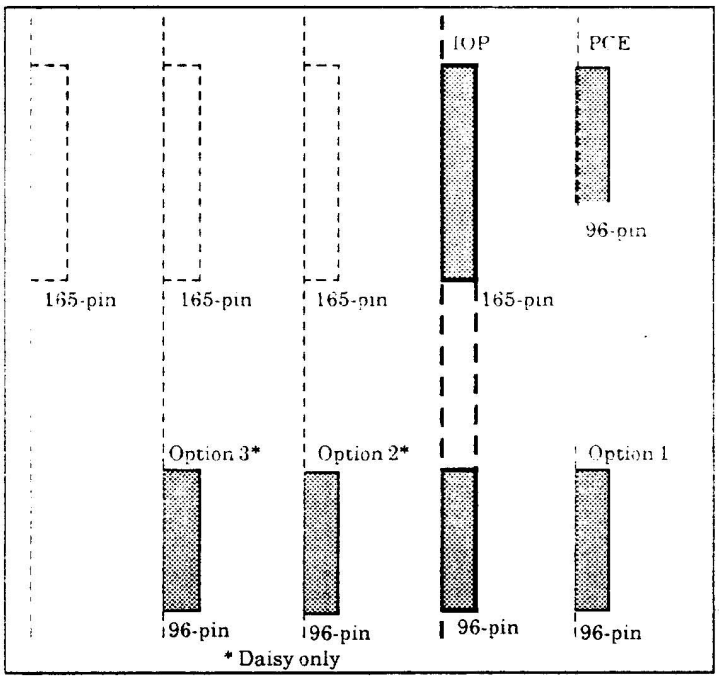


Figure 1.2. Locations of PWBAs on the backplane

Figure 1.3 illustrates the layout of the main IOP board. Note: The figure extends across two pages; the shaded areas indicate overlap.

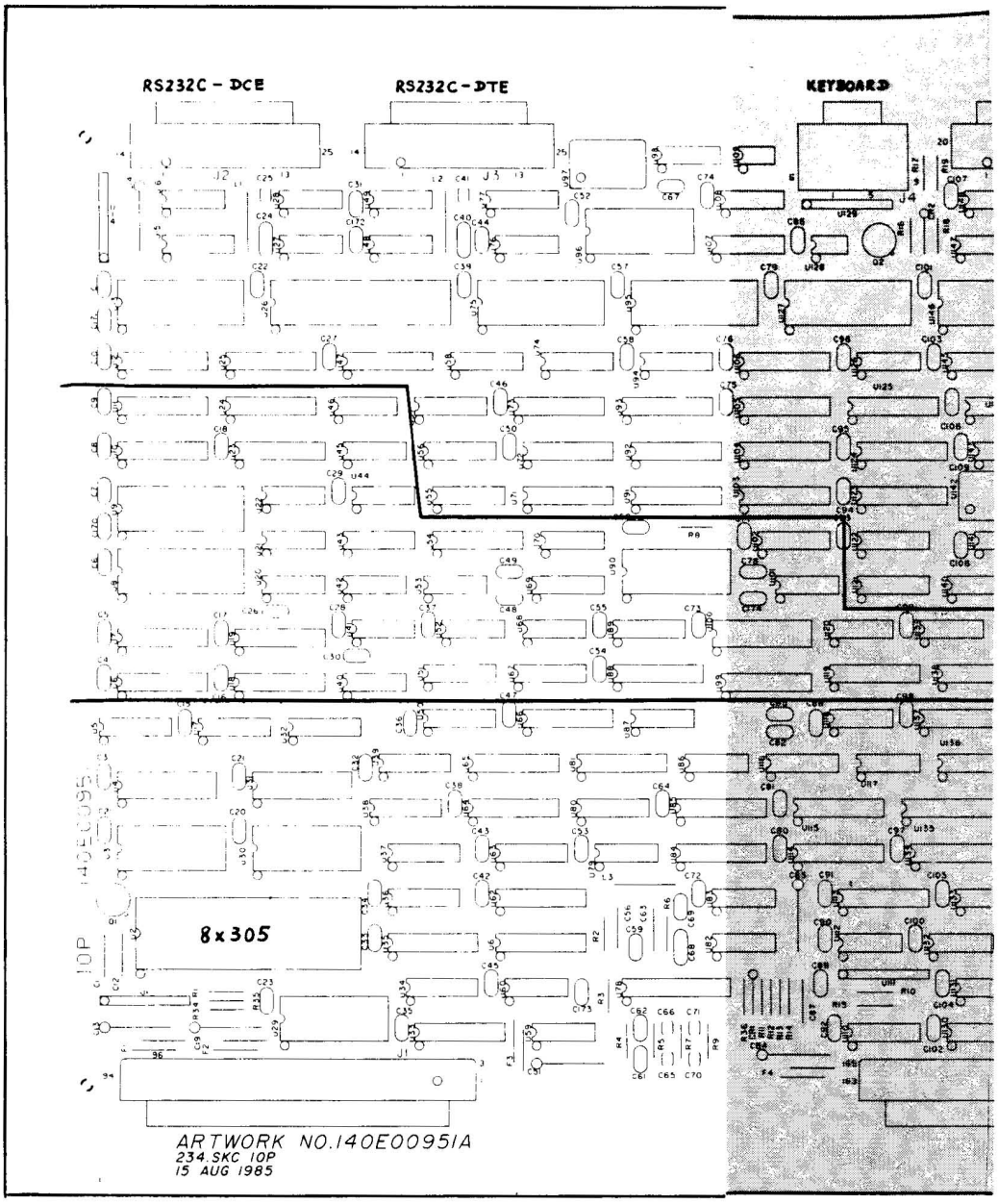
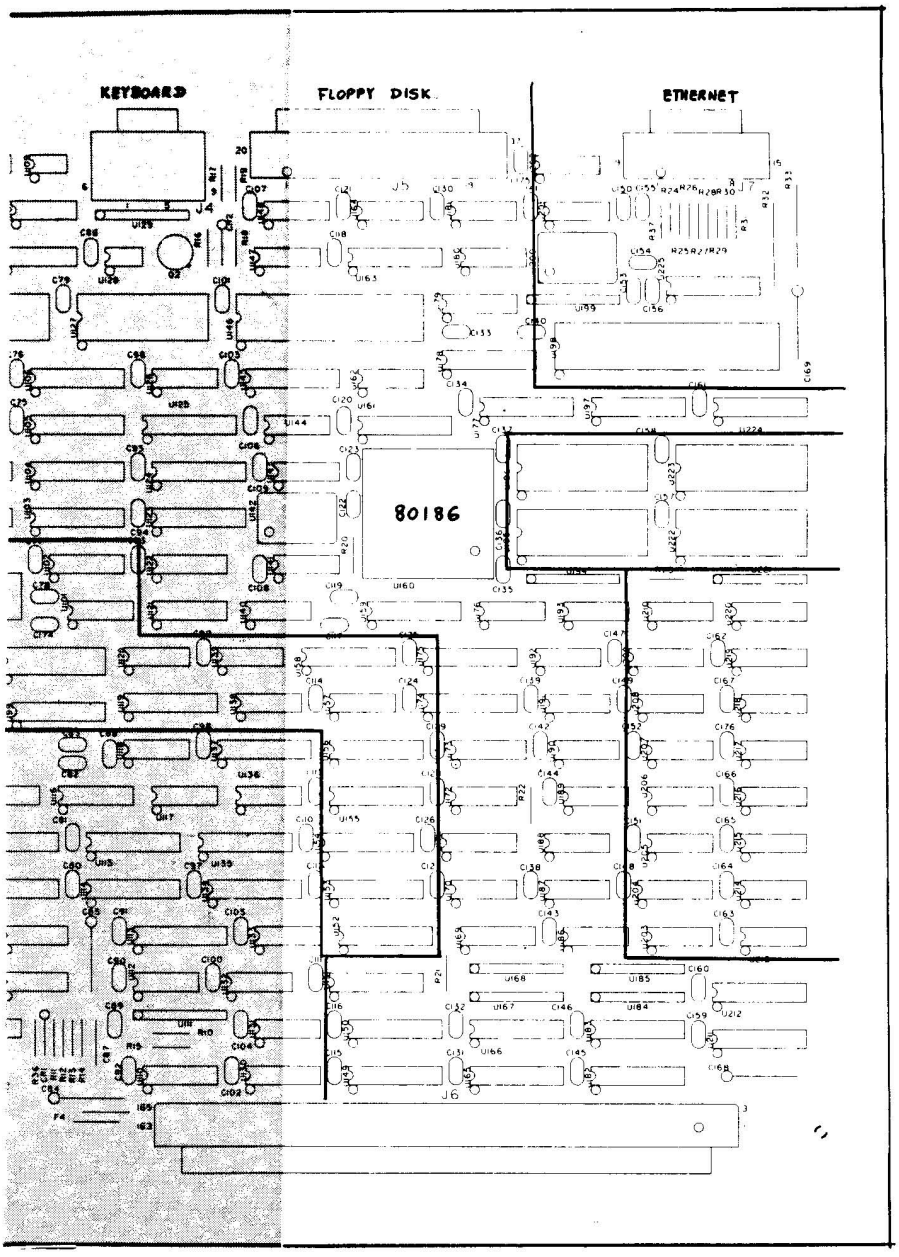


Figure 1.3. IOP board layout →



← **Figure 1.3.** IOP board layout

1.2.2 Interfaces to Backplane

Table 1.1 lists the IOP board 165-pin interface on the backplane. On the backplane, pins are grouped in six rows of three columns each. The table reflects the grouping, and is the front view of the backplane; that is the side from which the boards plug in.

Table 1.2 lists the 96-pin IOP expansion channel interface on the backplane. The table follows the same conventions as Table 1.1.

Backplane interfaces of the PCE and Options boards are presented in the manuals for those options.

Table 1.1. IOP Backplane Pin Assignment (Front View)

Outmost				Inmost	
Spare-1	J4.001	GND	J4.002	Spare-2	J4.003
A/AD.07	J4.004	A/DT/R'	J4.005	A/AD.15	J4.006
A/AD.06	J4.007	A/DEN'	J4.008	A/AD.14	J4.009
A/AD.05	J4.010	GND	J4.011	A/AD.13	J4.012
A/AD.04	J4.013	A/MemRdy	J4.014	A/AD.12	J4.015
A/AD.03	J4.016	A/ALE'	J4.017	A/AD.11	J4.018
A/AD.02	J4.019	A/IOPMemWr'	J4.020	A/AD.10	J4.021
A/AD.01	J4.022	Spare-3	J4.023	A/AD.09	J4.024
A/AD.00	J4.025	GND	J4.026	A/AD.08	J4.027
GND	J4.028	A/CLK	J4.029	VCC	J4.030
GND	J4.031	GND	J4.032	GND	J4.033
A/AA.19	J4.034	A/S.2'	J4.035	A/AA.23	J4.036
A/AA.18	J4.037	A/S.1'	J4.038	A/AA.22	J4.039
A/AA.17	J4.040	A/S.0'	J4.041	A/AA.21	J4.042
A/AA.16	J4.043	A/BHE	J4.044	A/AA.20	J4.045
A/EPromCs'	J4.046	GND	J4.047	A/IOR'	J4.048
Reserved - 0	J4.049	A/LocRamCS'	J4.050	Spare-4	J4.051
A/IOPLock	J4.052	GND	J4.053	A/IOW'	J4.054
A/PCHldAtoArb	J4.055	A/IOPMemRd'	J4.056	Spare	J4.057
-5V	J4.058	-5V	J4.059	-5V	J4.060
GND	J4.061	GND	J4.062	GND	J4.063
A/IORdy	J4.064	A/IOP-PCS2'	J4.065	A/IOPResetPC'	J4.066
Spare-7	J4.067	A/IOP-PCS3'	J4.068	GND	J4.069
SpareID'	J4.070	GND	J4.071	A/ArbHoldPC	J4.072
DBRK/Daisy'	J4.073	IOP-PCE-spare1	J4.074	Reserved-5	J4.075
A/PEINT'	J4.076	IOP-PCE-spare2	J4.077	A/PCEIntrIOP'	J4.078
A/MEBIntr'	J4.079	GND	J4.080	A/PCESpker'	J4.081
A/VREINT'	J4.082	RD1-RdData -	J4.083	RD1-WrData -	J4.084
GND	J4.085	RD1-RdData +	J4.086	RD1-WrData +	J4.087
A/RawCLK	J4.088	GND	J4.089	VCC	J4.090

- more -

Table 1.1. IOP Backplane Pin Assignment (continued)

Outmost				Inmost	
GND	J4.091	GND	J4.092	GND	J4.093
A/IOPIntMP'	J4.094	CSWREN	J4.095	RD1-DriveSeled'	J4.096
A/MPIntIOP	J4.097	CSLOAD/SHIFT'	J4.098	RD0-RdData-	J4.099
IOPRdNIA	J4.100	CSBUFFEREN	J4.101	RD0-RdData +	J4.102
A/HaltMP'	J4.103	CSDATAIN	J4.104	RD0-WrData -	J4.105
IOP-S-spare1	J4.106	CSSHIFTCLK	J4.107	RD0-WrData +	J4.108
A/ResetMPB'	J4.109	CSDATAOUT	J4.110	RD0-DrvSel'	J4.111
VCC	J4.112	VCC	J4.113	VCC	J4.114
VCC	J4.115	VCC	J4.116	VCC	J4.117
VCC	J4.118	VCC	J4.119	VCC	J4.120
GND	J4.121	GND	J4.122	GND	J4.123
GND	J4.124	GND	J4.125	GND	J4.126
GND	J4.127	GND	J4.128	GND	J4.129
RD/DirIn'	J4.130	RD/DrvSel2'	J4.131	RD/DrvSel1'	J4.132
RD/DrvSel0'	J4.133	RD/DrvSel3'	J4.134	RD/Step'	J4.135
RD/Ready'	J4.136	RD/Index'	J4.137	RD/HeadSel1'	J4.138
RD/HeadSel0'	J4.139	GND	J4.140	RD/WriteFault'	J4.141
RD/Track00'	J4.142	RD/SeekComp'	J4.143	RD/WriteGate'	J4.144
Rd/HeadSel2'	J4.145	GND	J4.146	RD/ReduceWrI'	J4.14
-12V	J4.148	-12V	J4.149	-12V	J4.150
GND	J4.151	GND	J4.152	GND	J4.153
GND	J4.154	GND	J4.155	GND	J4.156
+ 12V	J4.157	+ 12V	J4.158	+ 12V	J4.159
POWERNORMAL	J4.160	A/Reset'	J4.161	LED1	J4.162
BootButton	J4.163	LED3	J4.164	LED2	J4.165

Table 1.2. IOP Expansion Channel Pin Assignment

Outmost				Inmost	
A.15x	J13.01	Reset-x'	J13.02	A.07x	J13.03
A.14x	J13.04	GND	J13.05	A.06x	J13.06
A.13x	J13.07	IOPCLK-x	J13.08	A.05x	J13.09
A.12x	J13.10	GND	J13.11	A.04x	J13.12
A.11x	J13.13	IORd'-x	J13.14	A.03x	J13.15
A.10x	J13.16	GND	J13.17	A.02x	J13.18
A.09x	J13.19	IOWrH'-x	J13.20	A.01x	J13.21
A.08x	J13.22	Exp-spare1	J13.23	A.00x	J13.24
Exp-spare2	J13.25	ALE-x	J13.26	Exp-spare3	J13.27
VCC	J13.28	VCC	J13.29	VCC	J13.30
GND	J13.31	GND	J13.32	GND	J13.33
Datax.15	J13.34	IOPDEn-x'	J13.35	Datax.07	J13.36
Datax.14	J13.37	I/ORdy	J13.38	Datax.06	J13.39
Datax.13	J13.40	I/OWrL-x'	J13.41	Datax.05	J13.42
Datax.12	J13.43	GND	J13.44	Datax.04	J13.45
Datax.11	J13.46	IOPDT/R-x'	J13.47	Datax.03	J13.48
Datax.10	J13.49	ExpChanSel'	J13.50	Datax.02	J13.51
Datax.09	J13.52	GND	J13.53	Datax.01	J13.54
Datax.08	J13.55	XIntrReq1	J13.56	Datax.00	J13.57
+12V	J13.58	+12V	J13.59	VCC	J13.60
GND	J13.61	GND	J13.62	GND	J13.63
ExpDmaReq'	J13.64	XIntrReq2	J13.65	XIntrReq5	J13.66
Reserved	J13.67	XIntrReq3	J13.68	XIntrReq6	J13.69
XIntrReq0	J13.70	XIntrReq4	J13.71	XintrReq7	J13.72
-12V	J13.73	-12V	J13.74	-12V	J13.75
Exp-Spare4	J13.76	Exp-Spare5	J13.77	Reserved-1	J13.78
Exp-Spare6	J13.79	GND	J13.80	Reserved-2	J13.81
Exp-spare7	J13.82	Exp-spare8	J13.83	Reserved-3	J13.84
Exp-spare9	J13.85	GND	J13.86	Reserved-4	J13.87
-5V	J13.88	-5V	J13.89	VCC	J13.90
GND	J13.91	GND	J13.92	GND	J13.93
Exp-spare10	J13.94	Exp-spare11	J13.95	Exp-spare12	J13.96

1.2.3 Power

The system power supply is located at the rear of the system unit. It supplies the power necessary for the IOP board, as follows:

+5V ± 5% at 15.6 A
-5V ± 10% at 5mA
+12V ± 10% at 55mA
- 12V ± 10% at 50mA