

XEROX

Daybreak Technical Reference Manual

Version 1.0
December 1986

**Xerox Corporation
Information Systems Division
701 South Aviation Boulevard
El Segundo, California 90245**

**The information contained in this document is preliminary data
and is subject to change without notice.**

**Copyright ©1986, by Xerox Corporation. All rights reserved.
XEROX® is a trademark of XEROX CORPORATION.
Printed in the United States of America.**

Preface

P.1 Purpose

The Daybreak Technical Reference Manual describes the hardware that is specific to the Daybreak version of Dove. The manual describes the theory of operation of the components and presents information important for programmer interface.

P.2 Audience

The following groups are expected to refer to this publication:

- Engineers
- Field Service personnel
- Microprogrammers
- System designers

P.3 Organization

After a brief overview, each of the three Daybreak boards (Mesa Processor, Display Control and Memory, and Memory Expansion) is discussed in a separate section. Components are described as to hardware, theory of operations, and programmer interface.

Hardware describes board layout, interfaces to the backplane, power requirements, and external and internal signals of functional units.

Theory of Operations describes system operating modes.

Programmer Interface describes register assignments and timing.

Appendix A describes the standard cell Daybreak Display Controller.

Appendix B, printed in a separate volume, contains schematics for the three Daybreak boards and includes the Display Control and Memory board with the Daybreak Display Controller.

P.4 References

The following documents contain supplementary information.

Dandelion Hardware Manual (preliminary draft), version 2.2, March 1982.

Daybreak Microcode Reference Manual, Version 1.0, April 1986.

Dove IOP Board Technical Reference Manual, November 1985.

Dove PCE Board Technical Reference Manual, Version 1.0, January 1986.

Mesa Processor Principles of Operation, version 4.0, May 1985.

TABLE OF CONTENTS

1. Overview

1.1	Central Subsystem Components	1-2
1.1.2	Display controller and memory	1-2
1.1.2	System memory	1-3
1.2	Hardware: Backplane	1-3
1.3	Power	1-7
1.4	Notation	1-8
1.5	Glossary	1-8

2. Central Processor

2.1	General Board Hardware	2-2
2.1.1	Mesa processor board	2-2
2.1.2	Interfaces	2-3
2.1.3	Power	2-7
2.1.4	Clock generation	2-7
2.2	Microinstructions	2-8
2.2.1	Hardware	2-8
2.2.2	Theory of operations	2-8
2.2.3	Programmer interface	2-9
2.2.3.1	Microinstruction format	2-9
2.2.3.2	Microinstruction examples	2-11
2.3	Microinstruction Control Architecture	2-12
2.3.1	Hardware	2-14
2.3.1.1	Control store	2-14
2.3.1.2	Control store interface	2-14
2.3.1.3	Microinstruction decoder chip (MDC)	2-16
2.3.1.4	Microinstruction register (MIR)	2-18
2.3.2	Theory of operations: Mode control	2-19
2.3.2.1	Boot mode	2-19
2.3.2.2	Run mode	2-19
2.3.2.3	Stop mode	2-19
2.3.2.4	Mode control timing	2-20

2.3.3	Programmer interface	2-20
2.3.3.1	Conditional branching and dispatching	2-21
2.3.3.2	Instruction buffer dispatch	2-22
2.3.3.3	Interrupt register	2-23
2.3.3.4	Link registers	2-23
2.3.3.5	Microcode traps	2-24
2.4	Registers and Data Paths	2-26
2.4.1	Hardware	2-26
2.4.1.1	Arithmetic Logic Unit	2-26
2.4.1.2	Registers	2-29
2.4.1.3	Instruction buffer state machine	2-29
2.4.2	ALU theory of operations	2-31
2.4.2.1	External data paths	2-32
2.4.2.2	Internal data paths	2-33
2.4.2.3	Timing limitations	2-35
2.4.3	Programmer interface	2-38
2.4.3.1	2901C registers	2-38
2.4.3.2	Rotator	2-38
2.4.3.3	RH register	2-38
2.4.3.4	pc16 register	2-39
2.4.3.5	U register	2-40
2.4.3.6	stackP register	2-41
2.4.3.7	Instruction buffer registers	2-42
2.4.3.8	Constants	2-45
2.5	System Memory Addressing	2-45
2.5.1	Hardware	2-47
2.5.1.1	Mesa bus controller chip	2-47
2.5.1.2	Control logic	2-49
2.5.1.3	Memory address interfaces	2-51
2.5.1.4	Timer	2-53
2.5.2	Theory of operations: Mesa bus controller	2-54
2.5.2.1	States of the state machine	2-55
2.5.2.2	Interrupt control	2-64
2.5.2.3	Timer control	2-64

2.5.3	Programmer interface	2-66
2.5.3.1	Real address references	2-67
2.5.3.2	Virtual address references	2-68
2.5.3.3	Memory address register	2-69
2.5.3.4	Map reference	2-70
2.5.3.5	Memory data register	2-70
2.5.3.6	Memory data	2-70
3. Display Control		
3.1	General Information	3-1
3.1.1	Display parameters	3-2
3.1.2	Hardware	3-2
3.1.2.1	Display control and memory board	3-3
3.1.2.2	Interfaces	3-4
3.1.2.3	Power	3-7
3.2	Display Control	3-7
3.2.1	Hardware	3-9
3.2.2	Theory of operations	3-17
3.2.2.1	Display controller	3-18
3.2.2.2	Display initialization	3-24
3.2.2.3	Display line control	3-24
3.2.2.4	Display FIFO	3-29
3.2.3	Programmer interface	3-29
3.2.3.1	Vertical/Horizontal control store	3-29
3.2.3.2	Display data chip: registers and timing	3-30
3.2.3.3	Display cursor chip: registers	3-32
3.2.3.4	Display memory chip: registers and timing	3-32
3.2.3.5	Cursor	3-34
4. Memory		
4.1	Hardware	4-2
4.1.1	Memory on DCM board	4-2
4.1.2	Memory on MEB	4-5
4.1.2.1	Memory controller chip	4-6
4.1.2.2	Backplane interface	4-7

4.2	Theory of Operations	4-10
4.2.1	Read	4-10
4.2.2	Write	4-10
4.2.3	Refresh	4-11
4.3	Programmer Interface	4-11
4.3.1	Status registers	4-11
4.3.2	Memory timing	4-13
4.3.3	Functions	4-14
4.3.3.1	Full and page mode access	4-14
4.3.3.2	Row and column addressing	4-14

Appendices

Appendix A Daybreak Display Controller Chip

Software Differences

DDC Chip Functional and Timing Specification

Appendix B Representative Schematics (separate document)

Mesa Processor PWBA

Display Control and Memory PWBA

Memory Expansion PWBA

DCM Board with Standard Cell DDC

LIST OF FIGURES

Section 1	1.1	Daybreak architecture	1-1
	1.2	Backplane from logic board side	1-4
	1.3	Bus routing (logic board side)	1-5
	1.4	Signal flow of 165-pin connector (front view)	1-6
<hr/>			
Section 2	2.1	Mesa processor board logical blocks	2-1
	2.2	Mesa processor board layout	2-3
	2.3	Internally generated clocks	2-7
	2.4	Microinstruction format and subfield formats	2-10
	2.5	Microinstruction control architecture	2-13
	2.6	Writable control store pins and signals	2-14
	2.7	MDC pins and signals	2-16
	2.8	Mode (boot/run/stop) control timing	2-20
	2.9	I/O address space map	2-21
	2.10	2901C pins and signals	2-27
	2.11	IB state control pins and signals	2-30
	2.12	Daybreak central processor data paths	2-31
	2.13	ALU external data paths	2-32
	2.14	ALU internal block diagram	2-33
	2.15	ALU operations as a function of aS, aF, and Cin	2-34
	2.16	CP single-bit shifting	2-35
	2.17	Allowable X bus operations	2-37
	2.18	Rotator data paths	2-38
	2.19	RH register data paths	2-39
	2.20	U register data paths	2-40
	2.21	U register addressing modes	2-40
	2.22	stackP data paths	2-41
	2.23	Instruction buffer data paths	2-42
	2.24	Instruction buffer states	2-43
	2.25	Constants data paths	2-45
	2.26	Main memory addressing	2-46

	2.27	MBC pins and signals	2-47
	2.28	Mesa bus logic interface and control logic	2-50
	2.29	Mesa bus interface address/data paths	2-52
	2.30	Process timeout and interval timer pins and signals	2-53
	2.31	MBC functional block diagram	2-54
	2.32	State machine memory reference timing	2-56
	2.33	MBC state transitions	2-57
	2.34	Cycle 1: state machine flow	2-60
	2.35	Cycle 2: state machine flow	2-61
	2.36	Cycle 3: state machine flow (read)	2-62
	2.37	Cycle 3: state machine flow (write)	2-63
	2.38	Timer gate and clock timing	2-65
	2.39	Timer1 ripple carry clock	2-65
	2.40	Timer2 clock timing	2-66
	2.41	MAR address types	2-67
	2.42	Virtual-to-real address mapping	2-68
	2.43	Map address types	2-69
	2.44	Map entry format	2-69
	2.45	Memory Address Register (MAR) address generation	2-70
	2.46	Map← address generation	2-70
Section 3	3.1	DCM data paths	3-1
	3.2	DCM board layout	3-3
	3.3	Display controller block diagram	3-8
	3.4	Display Data Chip (DDC) pin-out	3-10
	3.5	Display Cursor Chip (DCC) pin-out	3-11
	3.6	Display Memory Chip (DMC) pin-out	3-12
	3.7	Horizontal and Vertical CS pins and signals	3-13
	3.8	Display FIFO pins and signals	3-13
	3.9	Cursor buffer pins and signals	3-14
	3.10	Display Data Chip I/O	3-18
	3.11	DDC internal data paths	3-19
	3.12	Display Cursor Chip I/O	3-20
	3.13	DCC internal data paths	3-21
	3.14	Display Memory Chip I/O	3-22

3.15	DMC internal data paths	3-23
3.16	Display line control flow	3-25
3.17	Control timing	3-27
3.18	Sync timing	3-28
3.19	Vertical control store registers	3-29
3.20	Horizontal control store registers	3-29
3.21	Display control registers: Write operations	3-30
3.22	DDC status register: Read operation	3-30
3.23	DDC timing	3-31
3.24	DCC control registers: Write operations	3-32
3.25	DCC status register: Read operation	3-32
3.26	DMC control registers: Write operations	3-33
3.27	DMC status register: Read operation	3-33
3.28	DMC timing	3-33
3.29	Memory access timing - nibble mode	3-34
3.30	Cursor pattern	3-35
3.31	Cursor buffer (32 x 8) registers	3-36

Section 4

4.1	Memory units	4-2
4.2	DCM memory controller chip	4-3
4.3	Memory Expansion Board (MEB) layout	4-6
4.4	MEB memory controller chip	4-7
4.5	IOP I/O address map for memory	4-11
4.6	Memory status register	4-12
4.7	Memory reference timing	4-13
4.8	Row and column addressing (from Dandelion)	4-14

LIST OF TABLES

Section 1	1.1	Total Daybreak dc power	1-7
Section 2	2.1	MPB backplane pin assignment	2-4
	2.2	Mesa (B) bus interface	2-6
	2.3	80186 (A) bus interface	2-6
	2.4	Power interface	2-7
	2.5	Control store interface signals	2-15
	2.6	MDC signal description	2-17
	2.7	Raw MIR interfaces	2-18
	2.8	Conditional branching and dispatching	2-22
	2.9	IB-refill traps	2-24
	2.10	Error types	2-25
	2.11	Stack pointer overflow or underflow	2-25
	2.12	ALU external signal description	2-29
	2.13	IB state interfaces	2-30
	2.14	Registers addressed by the central processor	2-32
	2.15	sh,,aD actions	2-34
	2.16	Effects of IB-related microinstruction functions	2-44
	2.17	MBC signal description	2-48
	2.18	B bus interface and control signals	2-51
	2.19	Timer signal description	2-53
Section 3	3.1	DCM backplane pin assignment	3-4
	3.2	Bus interface signals	3-6
	3.3	Display controller power consumption	3-7
	3.4	Power interface	3-7
	3.5	Display control external signal description	3-14
	3.6	Display subsystem internal signals	3-16
Section 4	4.1	Memory control chip (display) signal description	4-4
	4.2	MEB backplane pin assignment	4-8
	4.3	I/O write operation locations	4-12