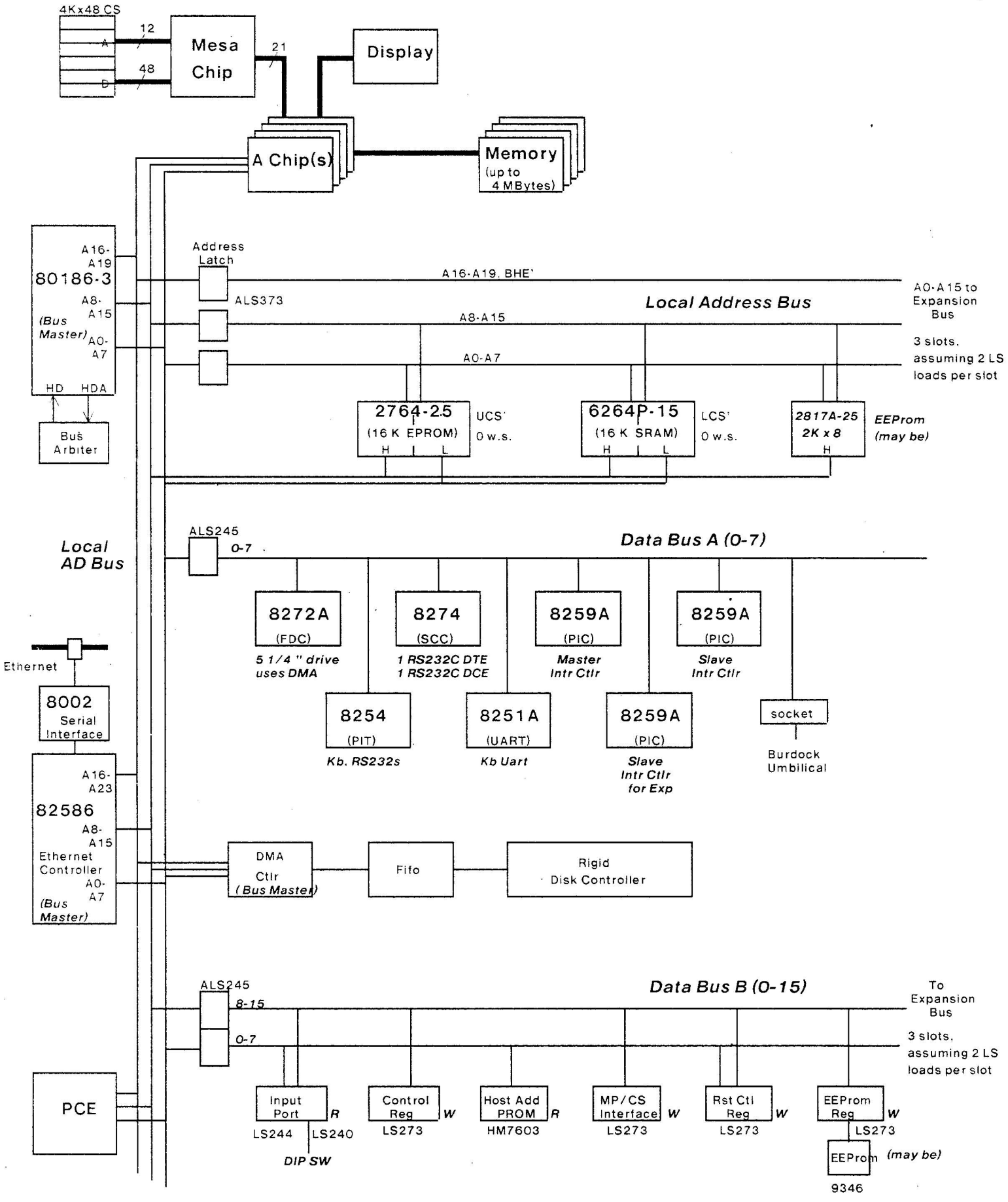
Daisy

IOP

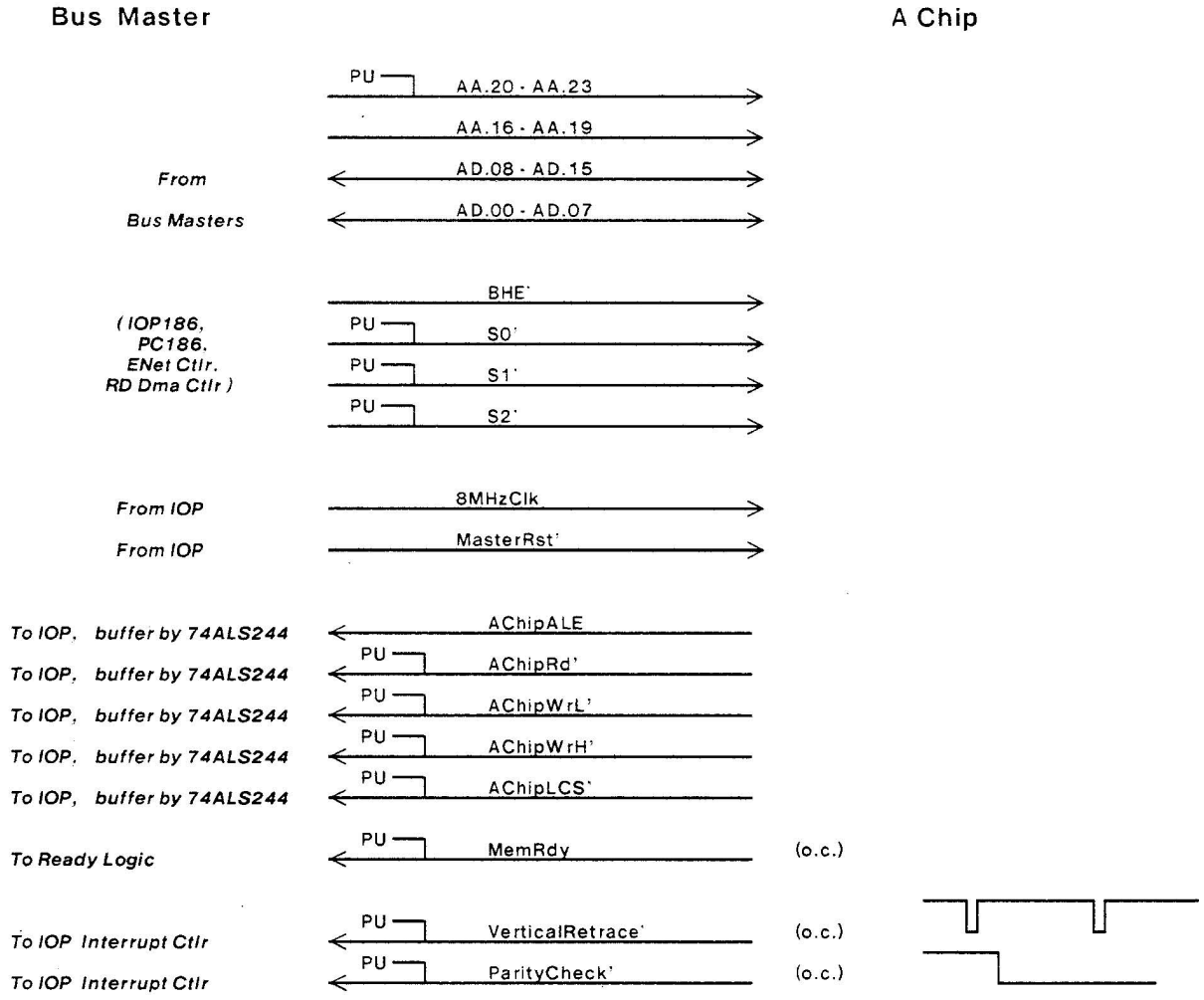
Notes

Rev : F
Date : 6/01/84
A. K. Tsang

File : [Ibis]<Daisy>IOP>DesignReview>Notes.press



XEROX SDD	Project Daisy	Daisy Block Diagram	File DIOP40.silx	Designer Tsang	Rev F	Date 6/01/84	Page 40



PU = 5.1K pull-up on IOP board.

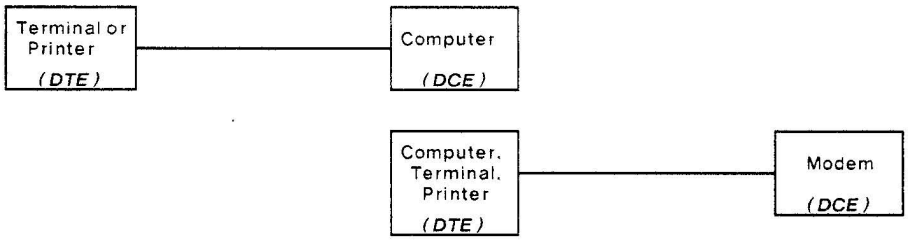
SelectA0', A1', A2' A3'
MapE'
MapF'

will be generated on Memory board(s).

Why A chip is used to generate some of the 80186 control signals instead of using those available from 80186 ?

1. When the 80186 relinquish the bus to other bus master device(s), it floats the bus control signals and deactivates ALE, memory-select, and peripheral-select signals. So if an ext. bus master wants to address memory & peripheral devices, discrete chip select and ready generation logic must be used. But by using the A chip to generate these signals (ALE, LCS', ARdy), this logic can be saved.
2. When 80186 is set up to operate in "Queue Status" mode, the RD' line is ext. grounded. ALE = QS0, WR' = QS1. That is, they are not available from 80186 any more. Queue status mode is used for 8087 NDP extension.

Typical Connections :



Interface Signals :

Connector Pin No [1]	Signal Name [2]		Direction of Flow	Signal Type	Active Level [3]
1	GND	*Chassis Ground*	DTE —— DCE		
2	TxD	*Transmitted Data*	DTE → DCE	Data	- 12 V
3	RxD	*Received Data*	DTE ← DCE	Data	- 12 V
4	RTS	*Request To Send*	DTE → DCE	Control	+ 12 V
5	CTS	*Clear To Send*	DTE ← DCE	Control	+ 12 V
6	DSR	*Data Set Ready*	DTE ← DCE	Control	+ 12 V
7	SG	*Signal Ground*	DTE —— DCE		
8	DCD	*Data Carrier Detect*	DTE ← DCE	Control	+ 12 V
15	TxC	*Transmitter Clock*	DTE ← DCE	Timing	
17	RxC	*Receiver Clock*	DTE ← DCE	Timing	
20	DTR	*Data Terminal Ready*	DTE → DCE	Control	+ 12 V
22	RI	*Ring Indicator*	DTE ← DCE	Control	+ 12 V

Note :

1. RS232C interface uses a 25-pin DB type connector.
   Typically, DTE uses a MALE connector,
   DCE uses a FEMALE connector.

2. RS232C signal names are w/r to DTE.

3. Signal voltages on the interface lines are nominally + 12v & -12v.
   * For Data signals, active => -12v = mark,
     inactive => + 12v = space.
   * For Control signals, active => + 12v = ON,
     inactive => -12v = OFF

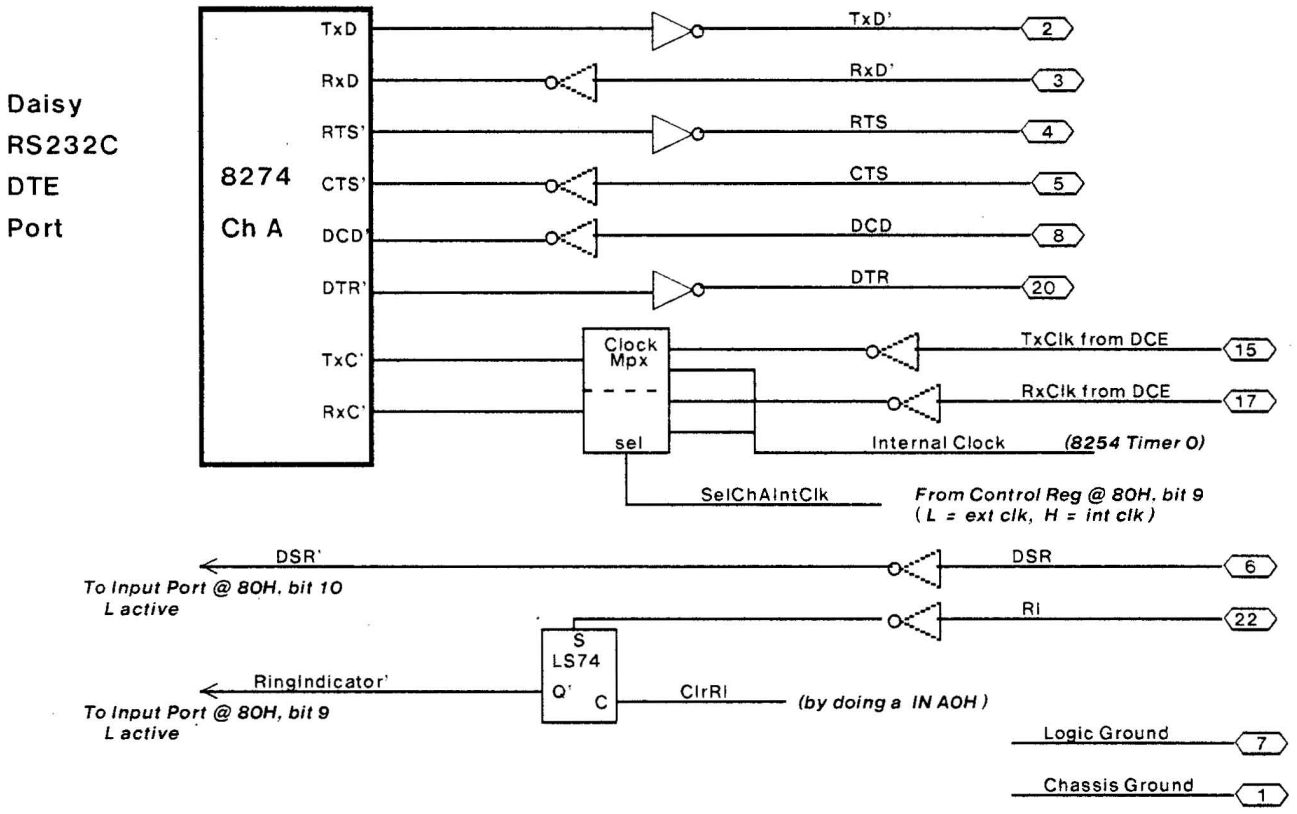
4. Some mfgers use pin 9 for + 12v,
   pin 12 for -12v.

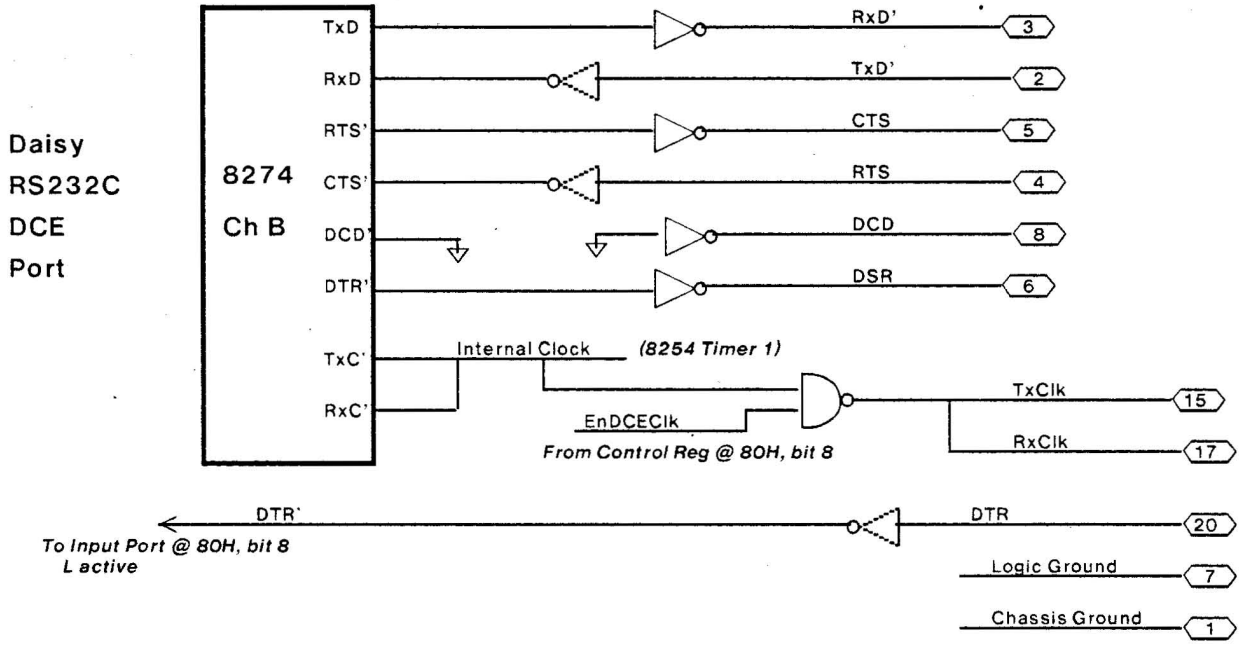
5. If a DTE were to be connected to another DTE (or a DCE to another DCE), the following pairs would have to be flipped :
   (2, 3)
   (4, 5)
   (6, 20)

6. In asynch mode, loopback w/i a single RS232C channel can be done by connecting
   2 to 3
   4 to 5 to 8 (and to 22 if implemented)
   20 to 6

7. Can convert RS422 signal levels for RS232C by picking up the the -ve side of the differential signal and ground the + ve side.

* In normal use, DTE brings up DTR, and DCE brings up DSR when they are powered on.
* In asynch, full duples environment, DTE then brings up RTS and awaits CTS from the DCE. (If the DCE is a modem, CTS is brought up along with DCD, once the incoming carrier has been detected).
* At this point, the DTE may transmit data to DCE over line 2, and the DCE may transmit data to DTE over line 3.
* In half-duplex system, RTS and CTS are used to determine which direction the data will be going over the wire, eg. the phone line.



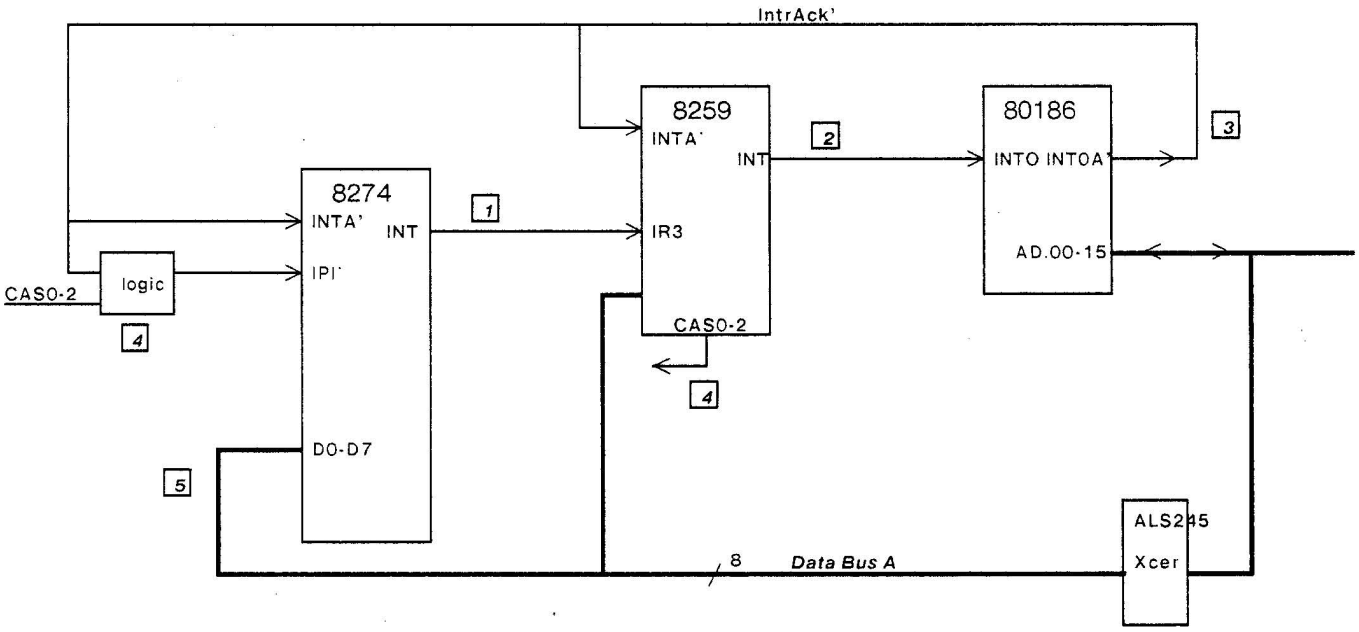


Features :

- Two independent full duplex channels
- Asynchronous, Byte Synchronous, & Bit Synchronous Operations
- Asyn transmission baud rate : up to 19.2K
- Synch transmission rate : up to 880K
- Interrupt driven operation, vector mode
- Internal Interrupt Priority : RxA, RxB, TxA, TxB, ExTA, ExTB
  or RxA, TxA, RxB, TxB, ExTA, ExTB

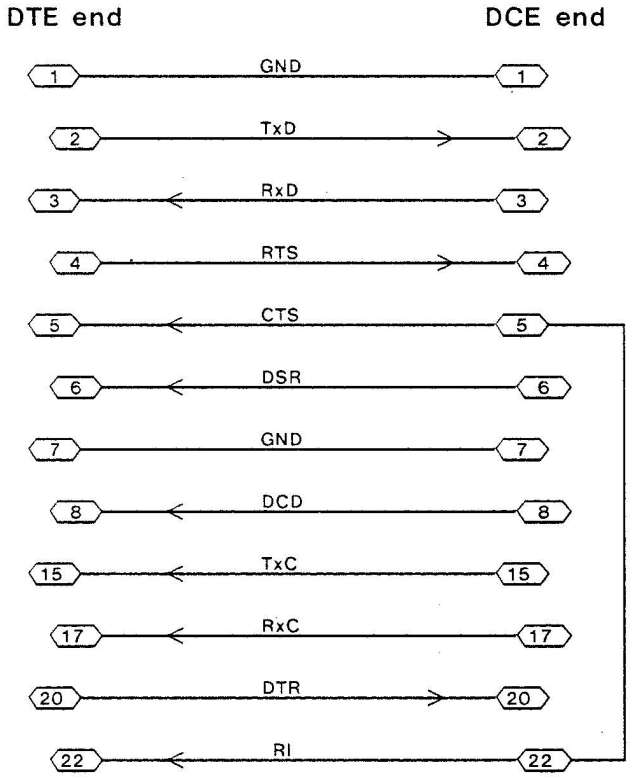
XEROX SDD	Project Daisy	Daisy RS232C Ports	File DIOP43.silx	Designer Tsang	Rev C	Date 4/23/84	Page 43

System Interface :



1. When an internal interrupt condition occurs (and if it is accepted), 8274 will cause an interrupt request to the Master Interrupt Controller 8259.
2. Upon receiving the interrupt request from 8274, and if it meets the conditions at that time, 8259 will generate an interrupt to the 80186 uP.
3. The uP will respond with two contiguous Interrupt ack cycles when it can service the interrupt.
4. Then, upon receiving the first INTA pulse, the 8259 will generate the Cascade signals, CAS0-2, which is then decoded.
5. If the CAS0-2 are decoded for 8274, the 8274 will then deliver the interrupt vector on the Data-Bus-A during the second INTA cycle.

DTE to DCE Connection for External Loopback :

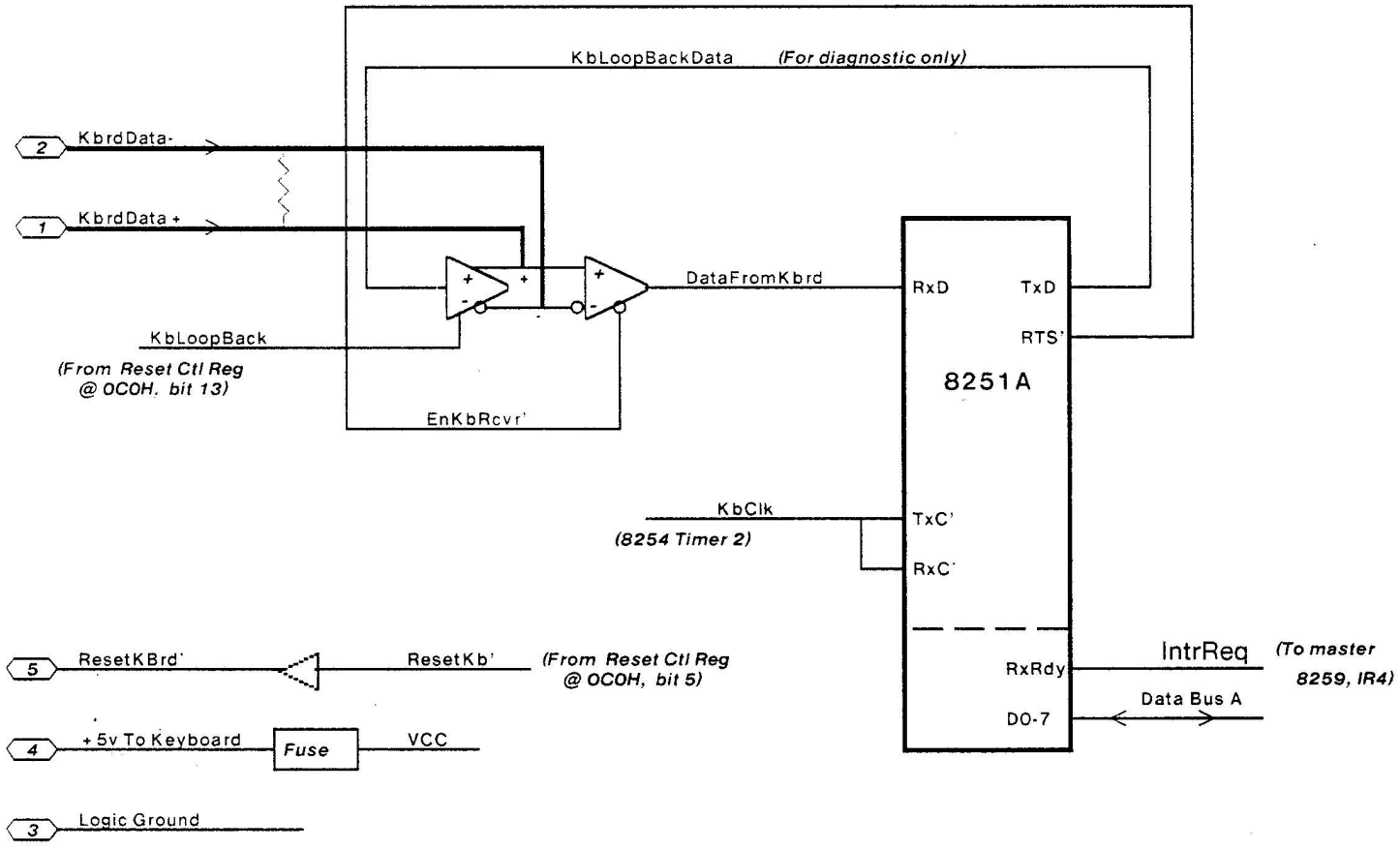


* If internal clock is used, loopback w/i a single RS232C channel can be performed by connecting :

TxD *to* RxD (2 to 3)
RTS *to* CTS (4 to 5)
DTR *to* DSR (20 to 6)

XEROX SDD	Project Daisy	Daisy RS232C Controller System Interface	File DIOP44.silx	Designer Tsang	Rev C	Date 5/1/84	Page 44

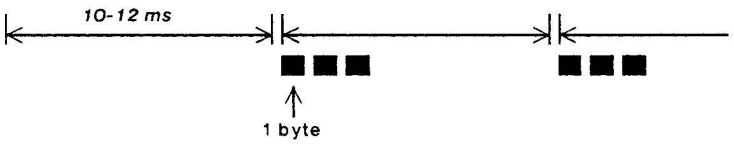
Keyboard/Mouse Interface :



Notes :

* Transmission rate : 9600 baud
* 1 start bit, 8 data bits, 1 stop bit.
  ~ 1 character per ms.
* kb takes ~ 10 - 12 ms per scan, then take
  ~ 5 ms to send 1 - 3 bytes of
  kb/mouse code to IOP.
* The receiver on the IOP is enabled by activating
  the RTS control signal of the 8274.
  Software must activate this signal in order to
  receive transmission from keyboard.

  The local driver should be disabled for
  normal operation.
* Transmission Picture :

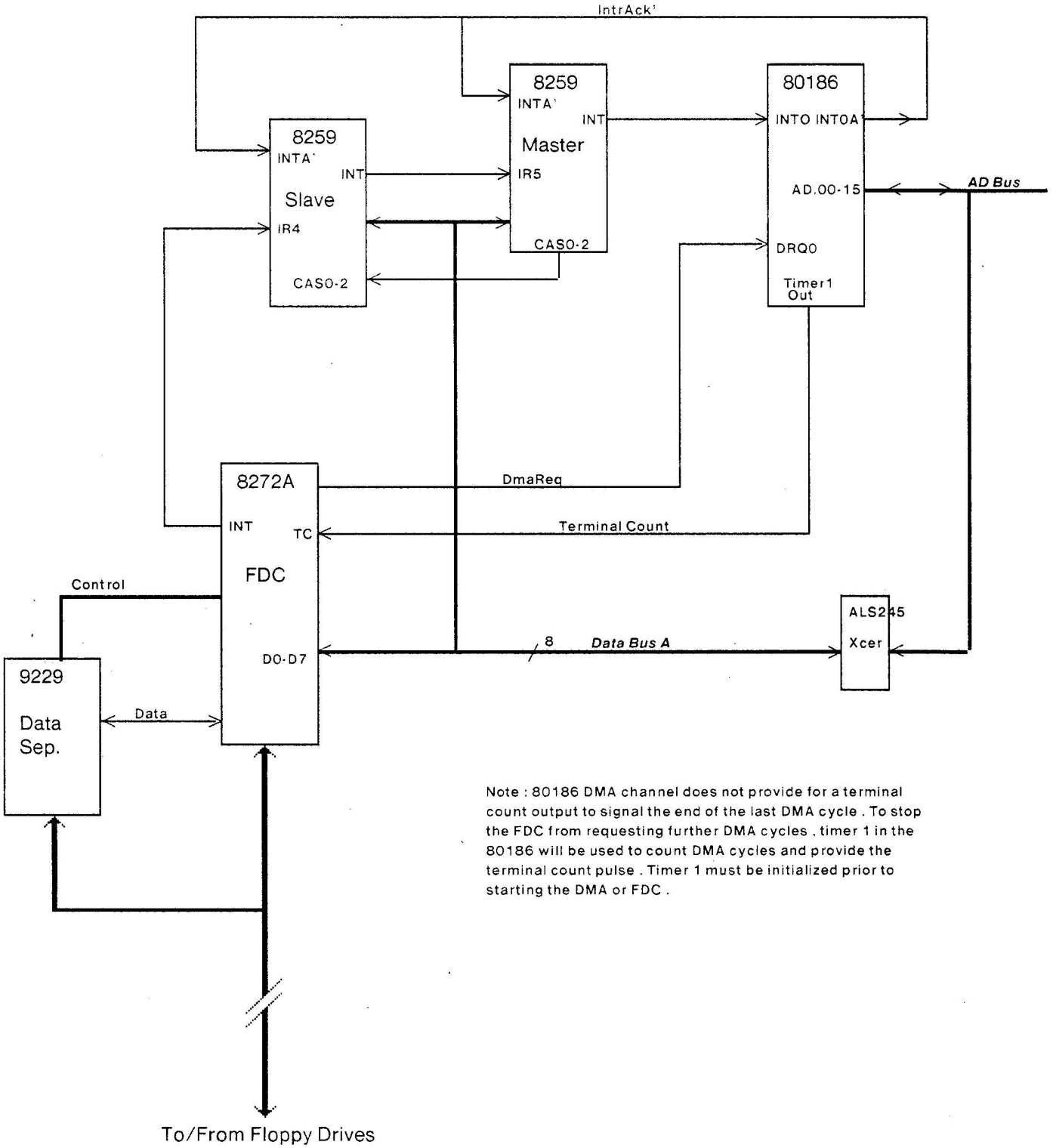


* When ResetKBrd' is active (ie. keyboard under
  reset), the driver at the keyboard end is disabled.
  So, if want to have local loopback for diagnostics
  without disconnecting the keyboard cable.
  MUST have the keyboard until reset.

  Then software can activate KbLoopBack signal to
  enable the local driver, and send TxD back to RxD.
* Only the receive channel (RxRdy) will generate
  interrupt upon receiving a character.
  When running diagnostic, should POLL TxRdy = H for
  transmission. TxRdy is not connected to intr ctlr.
* 6 wires connector,
  AMP DMP-R1A9S1A-xxx with right angle header.

  Connector :

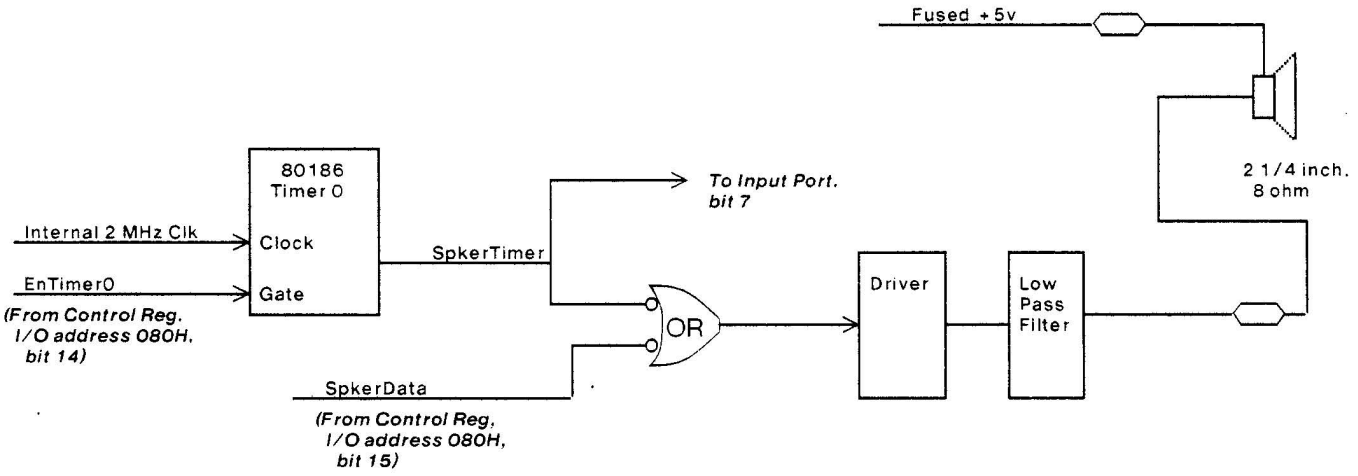
KbrdData +	1
KbrdData-	2
Gnd	3
Vcc	4
ResetKBrd'	5
unused	6



Note : 80186 DMA channel does not provide for a terminal count output to signal the end of the last DMA cycle . To stop the FDC from requesting further DMA cycles , timer 1 in the 80186 will be used to count DMA cycles and provide the terminal count pulse . Timer 1 must be initialized prior to starting the DMA or FDC .

XEROX SDD	Project Daisy	Floppy Disk Controller Interface	File DIOP46.silx	Designer Lopez	Rev F	Date 6/07/84	Page 46

Speaker Interface :



Two ways to generate sound from speaker :

1. Using the 80186 integrated Timer 0

   Set Control Reg. bit 14 = H, *(EnTimer0)*
   Control Reg. bit 15 = H, *(SpkerData)*

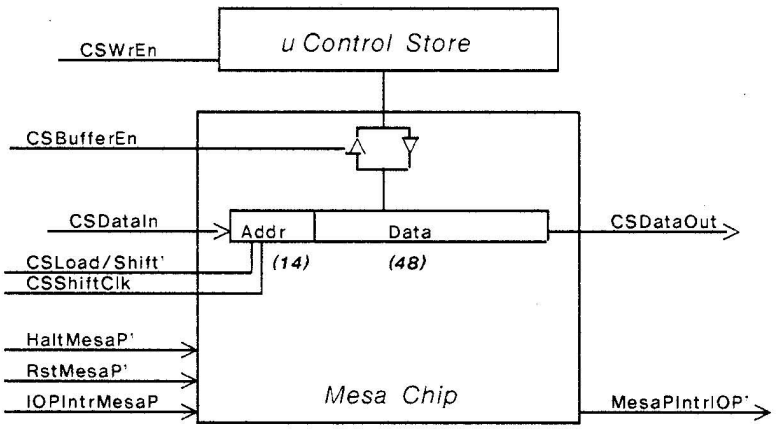
   Program the Timer 0 to generate the waveform desired.
   This method does not tie up the processor.

2. Use software to write to the speaker directly and use software loop to generate the waveform. This will tie up the processor.

   Set Control Reg. bit 14 = L to disable the timer.
   then toggle Control Reg. bit 15, as desired.

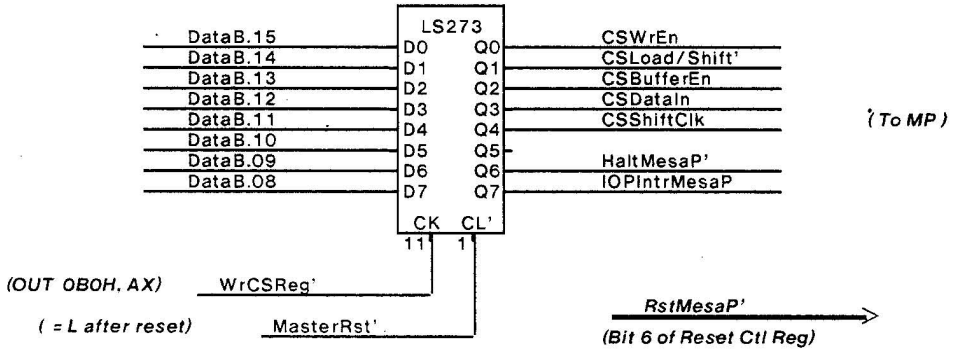
Mesa Processor & Control Store Interface

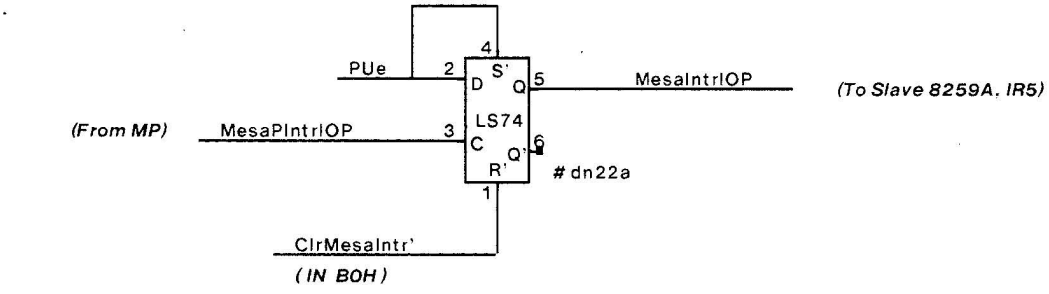
Model Only :

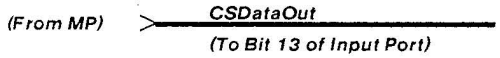


Note : Shift Reg shifts on L-to-H transition of clock.

8-bit Register

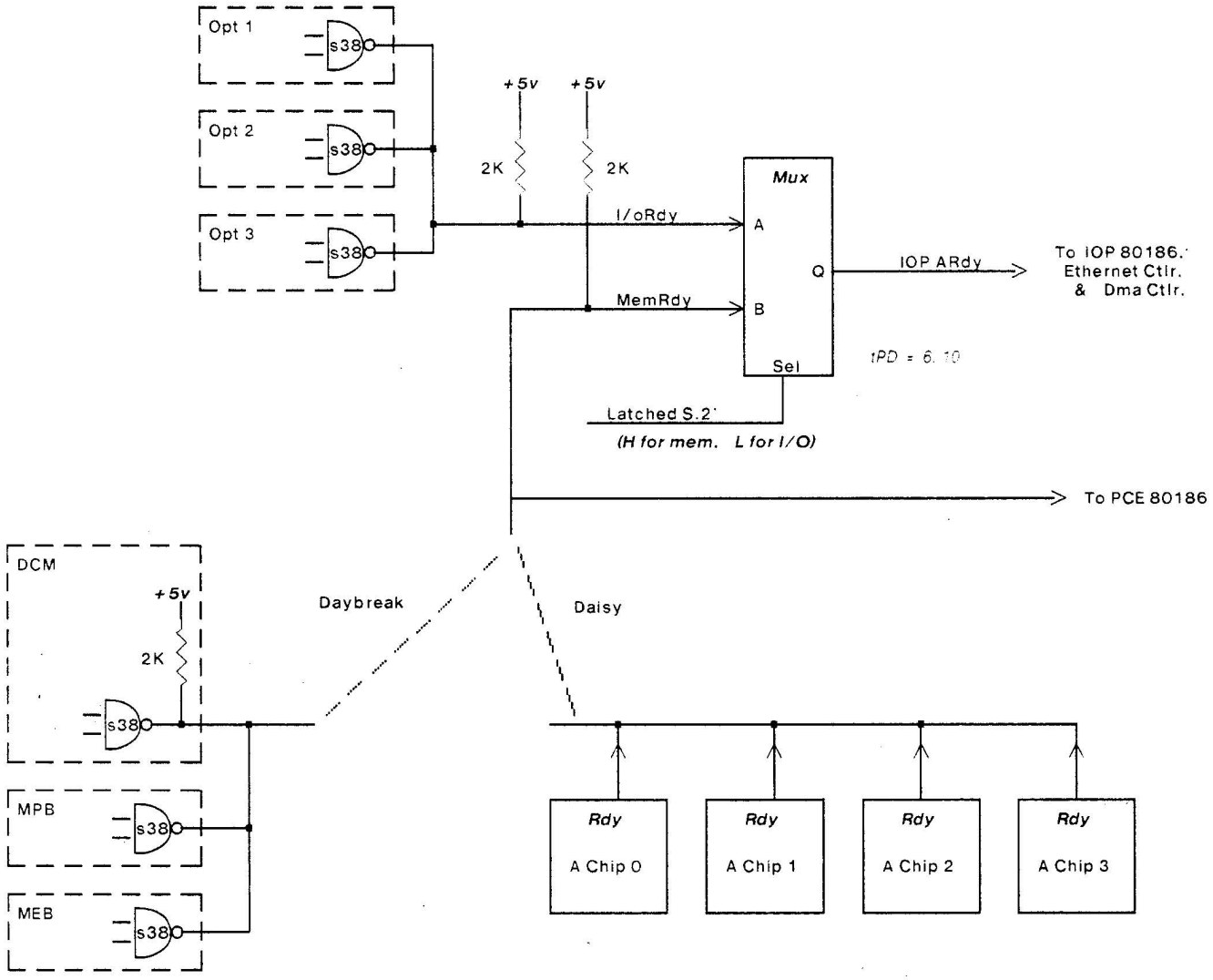






XEROX SDD	Project Daisy	Mesa Processor & Control Store Interface	File DIOP48.silx	Designer Tsang	Rev F	Date 6/07/84	Page 48

IOP 80186 Ready Logic :



Note :

* IOP is a NORMALLY-READY system.
* Only the ARdy of 80186 is used. SRdy is not used.
* ARdy is separated into MemRdy and I/ORdy in order to reduce loadings & faster rise time.
* I/ORdy is connected to Expansion Slots only.
  AChip internal registers, Daybreak Mono Display, Daybreak Color Display, and Mesa Processor I/O are also located in IOP 80186 I/O space. But because they require no wait state, they don't need to pull I/ORdy low. So I/ORdy is NOT connected to them.
* All expansion devices must be in I/O space. So MemRdy in not provided to Expansion Slots.

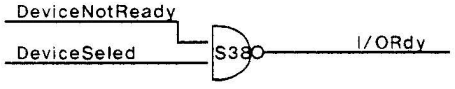
Expansion I/O Channel :

Signal Name	*Direction*	*Description*	*Loading Allowed Per Exp Slot*
A.15 - A.00	From IOP	Latch address bus. *(Not 20 bits because only I/O space).*	2 LS loads
Data.15 - Data .00	Bi-dir	Bi-directional 16-bit data bus.	2 LS loads
I/ORd'	From IOP	Read signal.	2 LS loads
I/OWrL'	From IOP	Write signal for Data.07 - .00 (low byte)	2 LS loads
I/OWrH'	From IOP	Write signal for Data.15 - .08 (high byte)	2 LS loads
ALE	From IOP	Address Latch Enable	2 LS loads
DEn'	From IOP	Data Enable. Used to enable Data Bus transceiver.	2 LS loads
DT/R'	From IOP	Data Bus direction signal. H for Transmit, L for Receive. For direction input of transceiver.	2 LS loads
I/ORdy	To IOP	Device Ready input signal to 80186. *See Note 1*	input
Reset'	From IOP	Reset signal. Low-level active. From 80186.	2 LS loads
8 MHz Clk	From IOP	Clock signal. 8 MHz, from 80186.	2 LS loads
IntrReq 0-7	To IOP	Interrupt Request inputs to 8259 Slave. Edge-triggered. *See Note 2*	input
ExpDmaReq'	To IOP	Dma Request input to 80186 integrated DMA Controller. Low-level active. *See Note 3*	input
ExpChanSel'	From IOP	Low if the address for 80186 I/O operations is within the range allocated for Expansion Slots. (4000H - 7FFFH)	2 LS loads

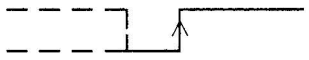
Notes :

* Three Expansion Slots for Daisy. One for Daybreak.
* All output signals are designed to drive 6 LS loads. two per Expansion Slots.
* All expansion devices lie in the 80186 I/O space. 16 KBytes of I/O addresses are allocated for expansion devices. From 4000H - 7FFFH.

1. Suggested implementation for *I/ORdy*

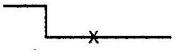


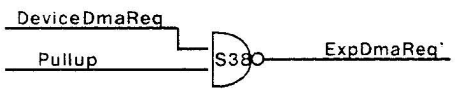
2. Interrupt Request inputs are edge-triggered

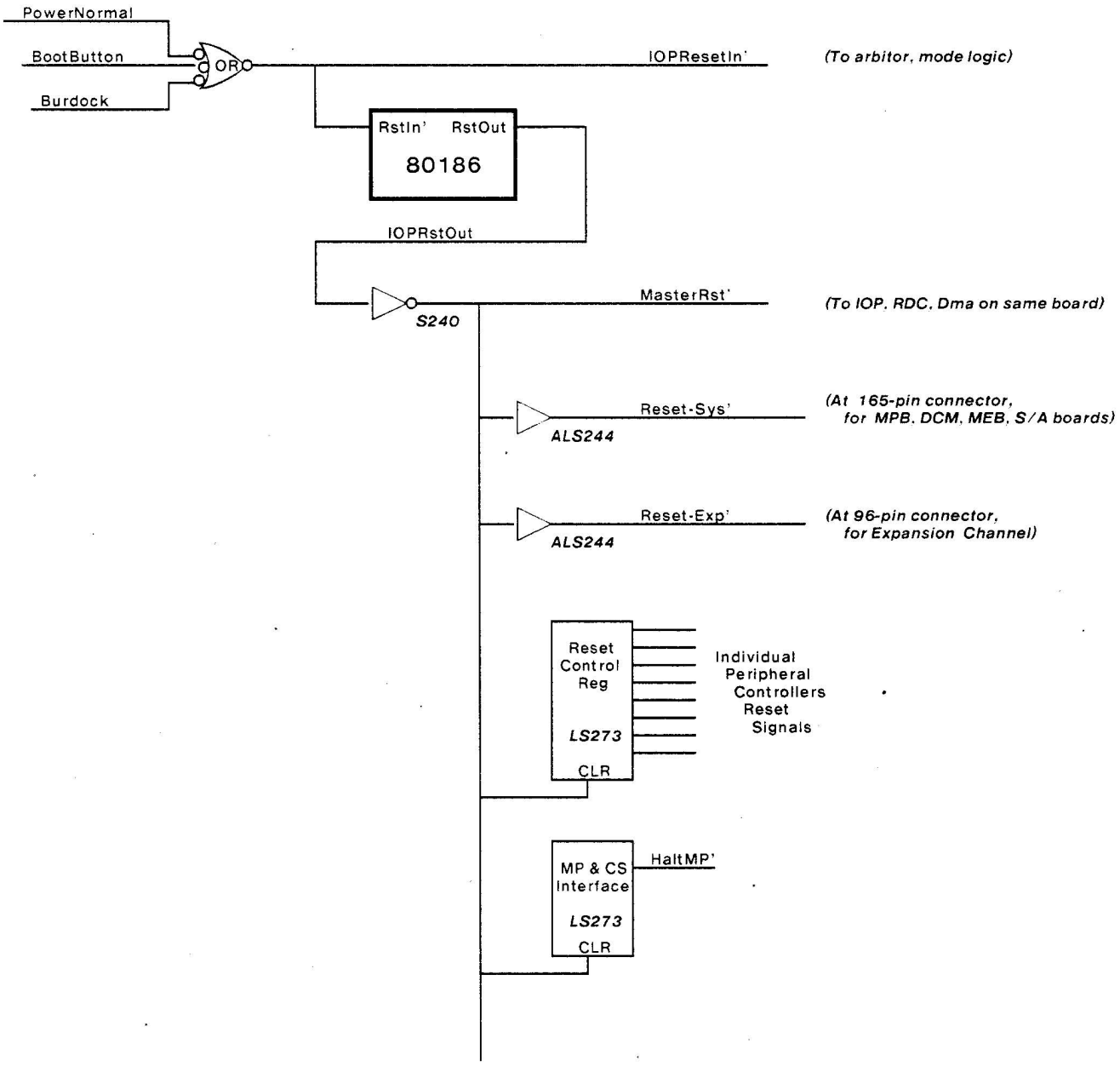


3. Suggested implementation for *ExpDmaReq'*

ExpDmaReq' is level triggered & sampled by 80186.

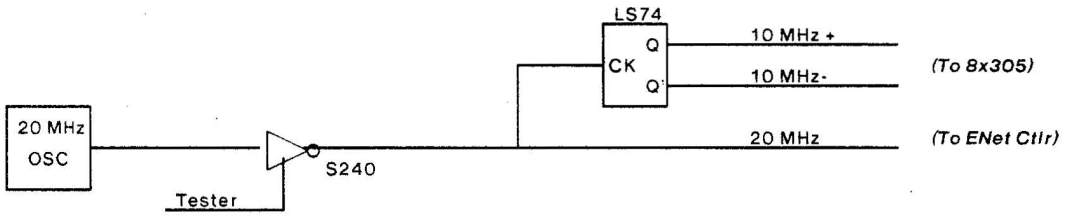


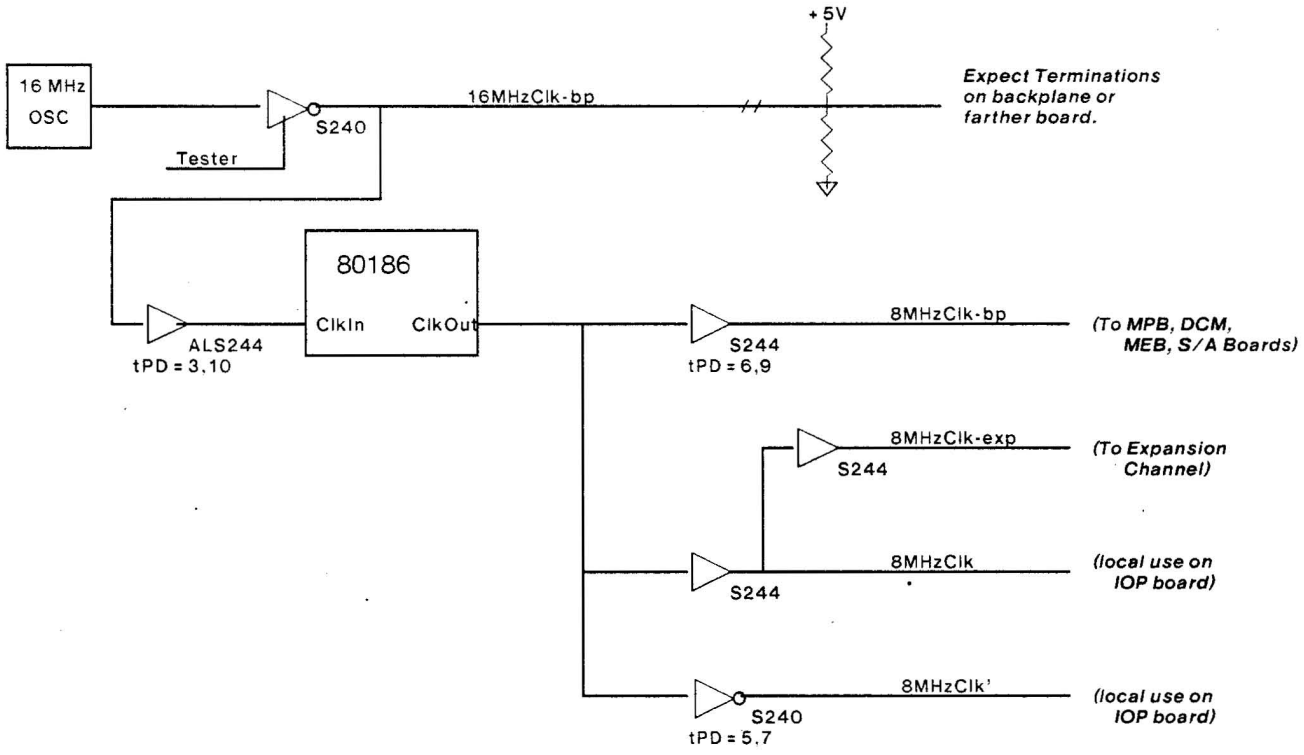




* PowerNormal becomes H btwn 50 - 250 ms after all power supply outputs have exceeded 94% of nominal.
* Pressing the Boot Button will generate a L pulse of ~ 0.5 s.
* Reset signal from Burdock must be at least 500 ns wide (80186 requirement).
* Software resets of peripheral controllers should be at least 20 us long (due to keyboard reset requirement).
* When floppy disk controller is reset or during machine power up, the Write Current is cut-off.
* When rigid disk controller is reset or during machine power up, the Write Current is cut-off.

XEROX SDD	Project: Daisy	Reset Logic	File: DIOP494.silx	Designer: Tsang	Rev: F	Date: 6/01/84	Page: 494



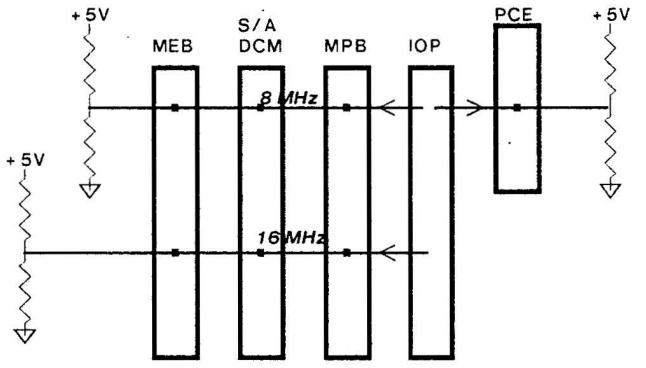


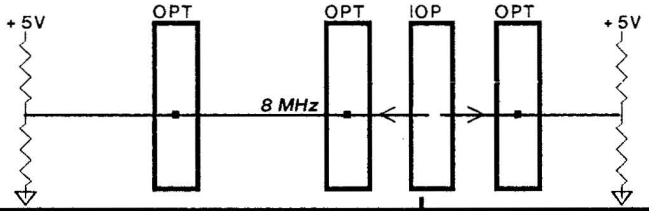
80186 ClkOut :

I_{OH} = 200 uA

I_{OL} = 2500 uA

Terminations :

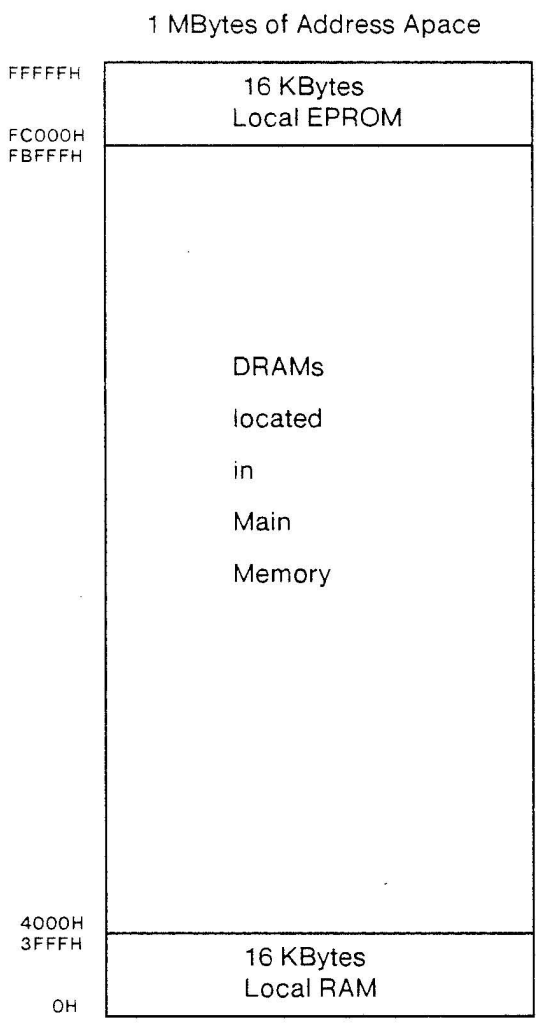




XEROX SDD	Project Daisy	Clock Distribution on IOP Board	File DIOP495.silx	Designer Tsang	Rev F	Date 6/01/84	Page 495x

IOP 80186 Memory Address Space

ms																			ls
A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1M	*512K*	*256K*	*128K*	*64K*	*32K*	*16K*	*8K*	*4K*	*2K*	*1K*	*512*	*256*	*128*	*64*	*32*	*16*	*8*	*4*	*2*



0 wait state
UCS'

at least
1 wait state

0 wait state
AChipLCS'

Function

* StartUp ROM
* IOP BIOS

* Local Memory
* Interrupt Vector Table
(max 1K)

16 KBytes of SRAM (temp only)
uses MCS0', 0 w.s.
located at 10000H -- 13FFFH

Base address of mid-range memory must be a integer multiple of total block size.

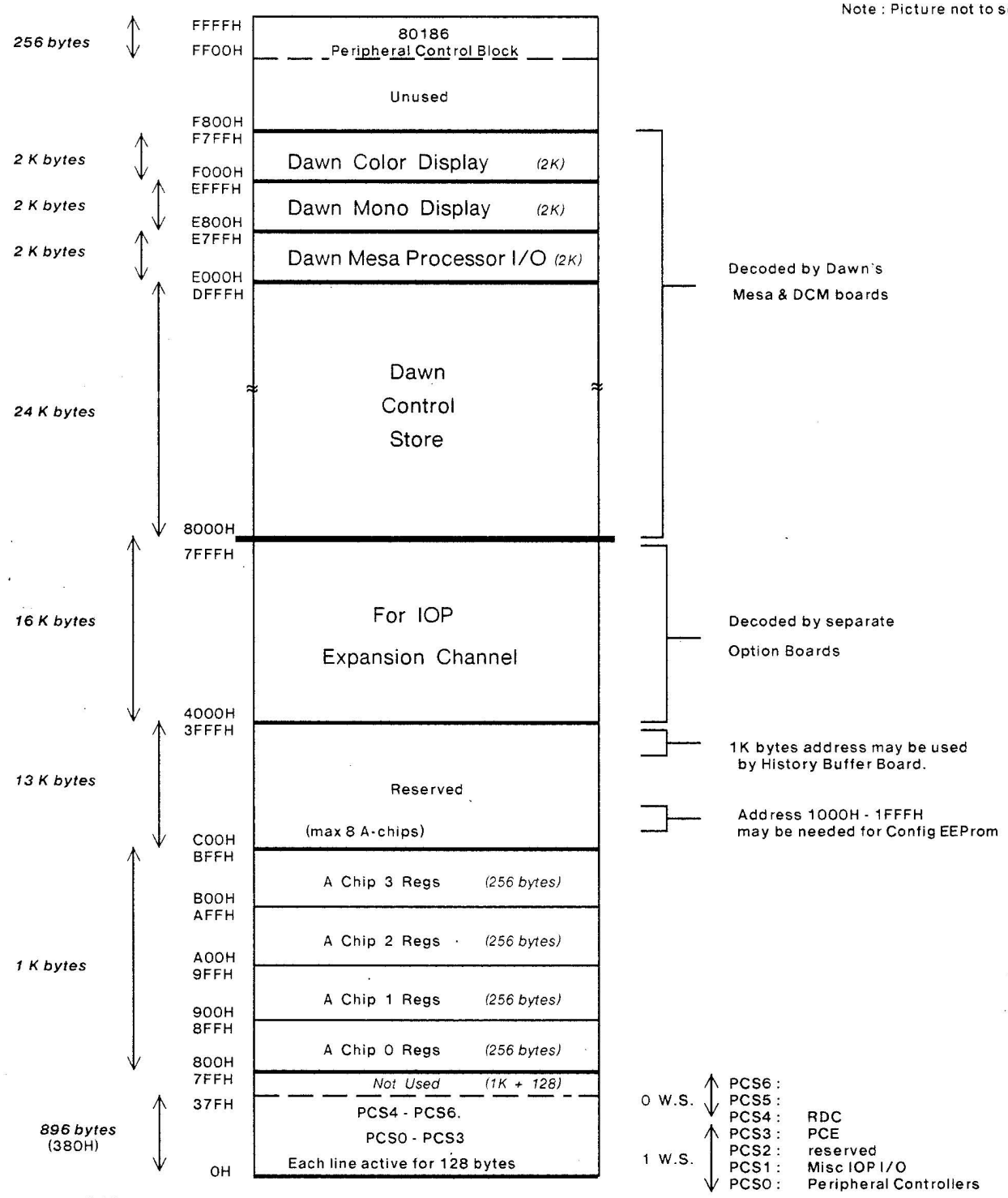
XEROX SDD	Project Daisy	80186 Memory Address Space	File DIOP50.silx	Designer Tsang	Rev A	Date 2/28/84	Page 50

IOP 80186 I/O Address Space

ms																ls			
A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
= 0				64K	32K	16K	8K	4K	2K	1K	512	256	128	64	32	16	8	4	2

64 KBytes of I/O Space

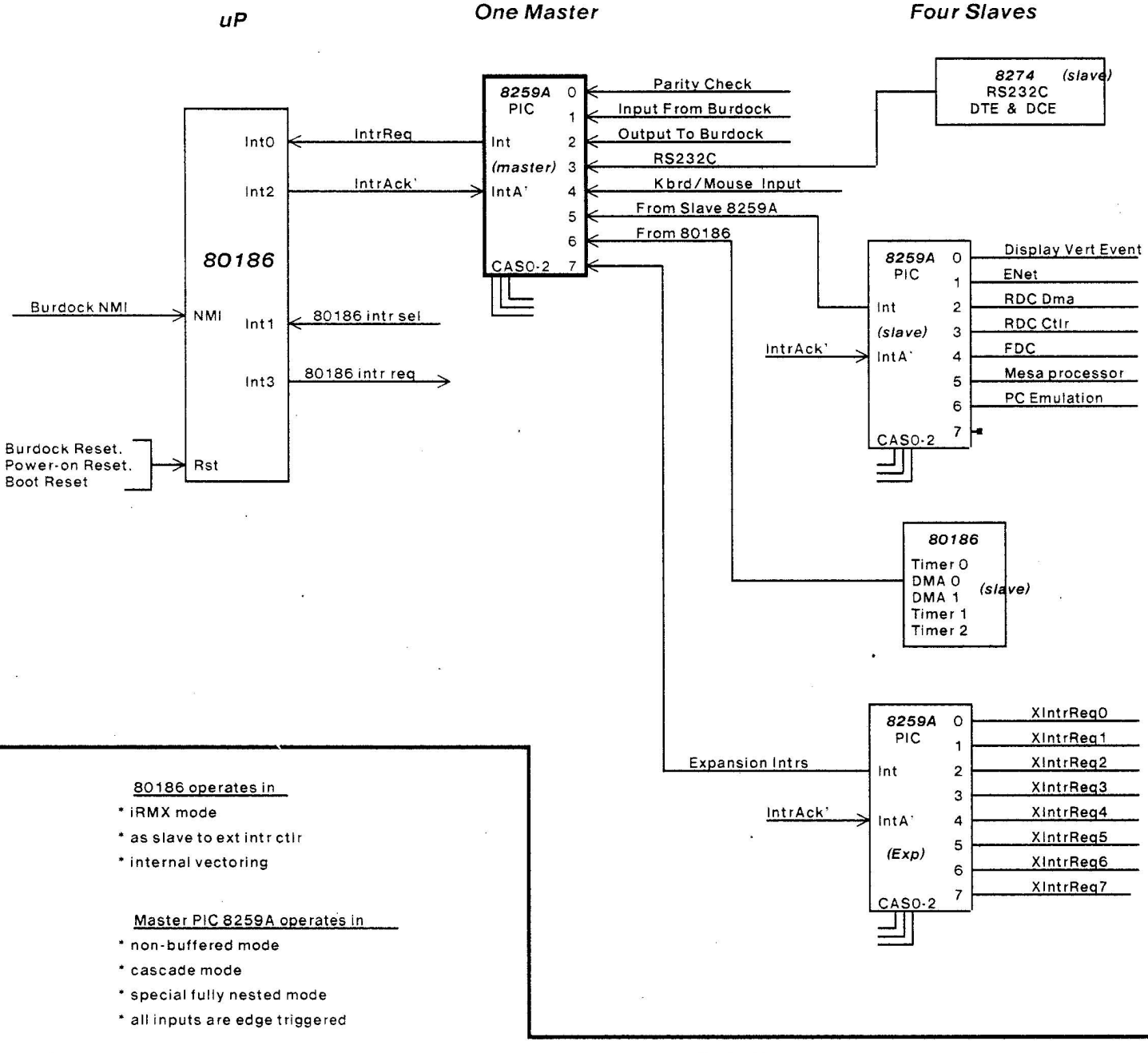
Note : Picture not to scale



Note : Base address of PCS's must be integer multiple of 1K.
Peripheral Control Block can be relocated to any 256 byte boundary.
0F8 to 0FF are reserved by Intel.
IBM PC I/O device addresses are located in the lowest 1K.

XEROX SDD	Project		File	Designer	Rev	Date	Page
	Daisy	80186 I/O Address Space	DIOP51.silx	Tsang	F	6/01/84	51

Interrupts



80186 operates in

* iRMX mode
* as slave to ext intr ctlr
* internal vectoring

Master PIC 8259A operates in

* non-buffered mode
* cascade mode
* special fully nested mode
* all inputs are edge triggered

Slave PIC 8259A operates in

* non-buffered mode
* cascade mode
* all inputs are edge triggered

Vector Types

* max 256 allowed (limited by 8 bits vector). including predefined and reserved ones.
* 0 - 19 pre-defined for 80186.
* 20 - 31 reserved by Intel.

IOP interrupt types should start at 32.

Advantage of RMX mode: Interrupt vectors for 80186 internal peripherals are programmable. (The 80186 Interrupt Vector Register specifies the 5 m.s. bits, the lower 3 sig. bits are determined by the priority level of the internal device causing the interrupt in iRMX mode).

Disadvantages: Take 55 c.c. to process an interrupt (internal or external vectoring).

XEROX SDD	Project Daisy	IOP Interrupts	File DIOP52.silx	Designer Tsang	Rev E	Date 5/22/84	Page 52x

IOP I/O Controllers use the 80186 PCS lines.
Base address of PCS's starts at 0H in 80186 I/O space.
The seven PCS lines are allocated as follows :

		Address	Usages	
1 w.s.	PCS.0 :	0 - 7FH	I/O Controllers	
	PCS.1 :	80 - FFH	Misc IOP I/O	(Note: F8 to FFH reserved by Intel)
	PCS.2 :	100 - 17FH	PCE	
	PCS.3 :	180 - 1FFH	PCE	
0 w.s.	PCS.4 :	200 - 27FH	Rigid Disk	
	PCS.5 :	280 - 2FFH	unused	
	PCS.6 :	300 - 37FH	unused	

PCS.0

Address (Hex)	Read	Write
8259A Master Intr Ctlr		
0	IRR, ISR	ICW1, OCW2, OCW3
2	IMR	ICW2, ICW3, ICW4, OCW1
8259A Slave Intr Ctlr		
10	IRR, ISR	ICW1, OCW2, OCW3
12	IMR	ICW2, ICW3, ICW4, OCW1
8254 Timer		
20	Timer Counter 0	Timer Counter 0
22	Timer Counter 1	Timer Counter 1
24	Timer Counter 2	Timer Counter 2
26	——	Timer Mode
8251A Uart (Keyboard/Mouse)		
30	Uart Rx Data	Uart Tx Data
32	Uart Status	Uart Ctl Word
8274 RS232C Ctlr		
40	Ch A Rx Data	Ch A Tx Data
42	Ch A Status	Ch A Cmd/Parm
44	Ch B Rx Data	Ch B Tx Data
46	Ch B Status	Ch B Cmd/Parm
8272A FDC		
50	FDC Main Status Reg	*(illegal)*
52	FDC Data Reg Stack	FDC Data Reg Stack
54	Dma Read from FDC	Dma Write to FDC
56	Terminal Count to FDC	*(for polling only)*
8259A Expansion Intr Ctlr		
60	IRR, ISR	ICW1, OCW2, OCW3
62	IMR	ICW2, ICW3, ICW4, OCW1
8255A-5 PIO Burdock Interface		
70	Port A	Port A
72	Port B	Port B
74	Port C	Port C
76	*(illegal)*	Control Word

PCS.1

Address (Hex)	Read	Write
80	Input Port	Control Reg
90	Host Address PROM (90,92,94,96,98,9A,9C,9EH)	LED
A0	Clear Ring Latch	ENet Attn
B0	Clear Mesa Interrupt Latch	Mesa Processor/ Control Store Reg
C0	Clear ENet Interrupt Latch	***Reserved (may be used for WrConfigReg')***
D0	X	
E0	X	AllowPCCmd'
F0	HoldIOPCmd'	AllowRDCCmd'

Note : address 0F8H -- 0FFH are reserved by Intel.

XEROX SDD	Project Daisy	IOP I/O Controller Addresses	File DIOP53.silx	Designer Tsang	Rev E	Date 5/22/84	Page 53

	READ			WRITE				
	Input Port *(80H)*			Control Reg *(80H)*	LED *(90H)*	Mesa Proc/ Control Store Reg *(B0H)*	Reset Control Reg *(C0H)*	EEProm Config Reg *(D0H) (may be)*
Bit 15	8272A FDC Interrupt Request			Speaker Data	LED digit 3	Control Store Wr Enable	Enable Ethernet Int Loopback	Serial EEProm Enable
Bit 14	8272A FDC Dma Request			Enable 186 Timer 0	LED digit 3	Control Store Load/Shift'	Enable Keyboard Int Loopback	*unused*
Bit 13	Data From Control Store (1 bit only)			FDD Motor On	LED digit 3	Control Store Buffer En	Allow to Access Byte-wide EEProm	*unused*
Bit 12	Daybreak/ Daisy' ID			FDD In Use	LED digit 3	Data To Control Store (1 bit only)	*unused*	Serial EEProm Data In
Bit 11	Data From Config EEProm (1 bit only) *(may be)*			Allow Timer 1 to generate 8272A TC in real Dma	LED digit 2	Control Store Shift Clock	*unused*	*unused*
Bit 10	RS232 Ch A DSR' *(L active)*			*unused*	LED digit 2	*unused*	*unused*	*unused*
Bit 9	RS232 Ch A Ring Indicator' *(L active)*			Sel RS232 Ch A to use internal clock	LED digit 2	Halt Mesa Proc' *(L active)*	Reset Dma-Fifo'	*unused*
Bit 8	RS232 Ch B DTR' *(L active)*			Enable RS232 Ch B to send clock signals	LED digit 2	Interrupt Mesa Proc	Reset PCE-80186'	Serial EEProm Clock
Bit 7	SpkerTimer				LED digit 1		Reset RDC'	
Bit 6	Serial EEPromRdy				LED digit 1		Reset Mesa Proc'	
Bit 5	DipSw.5				LED digit 1		Reset Keyboard'	
Bit 4	DipSw.4				LED digit 1		Reset Burdock Ctlr 8255-5'	
Bit 3	DipSw.3				LED digit 0		Reset Keyboard Uart 8251A'	
Bit 2	DipSw.2				LED digit 0		Reset FD Ctlr 8272A'	
Bit 1	DipSw.1				LED digit 0		Reset RS232 Ctlr 8274'	
Bit 0	DipSw.0				LED digit 0		Reset ENet Ctlr 82586'	

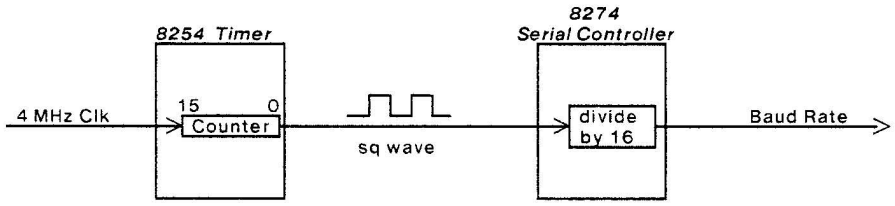
Timers

80186 : *(internal timers, 16 bits wide)*

Timer0 : Speaker Circuit (Clock-In = Internal 2 MHz clock)
Timer1 : FDC Terminal Count (Clock-In = 8272A FDC Dma Ack)
Timer2 : *Reserved for Operating System* (Clock-In = Internal 2 MHz clock, no ext output)

8254 : *(8 bits wide)*

Timer0 : RS232C DTE baud rate (clock in = 4.0 MHz)
Timer1 : RS232C DCE baud rate (clock in = 4.0 MHz)
Timer2 : Keyboard/Mouse baud rate (clock in = 4.0 MHz)

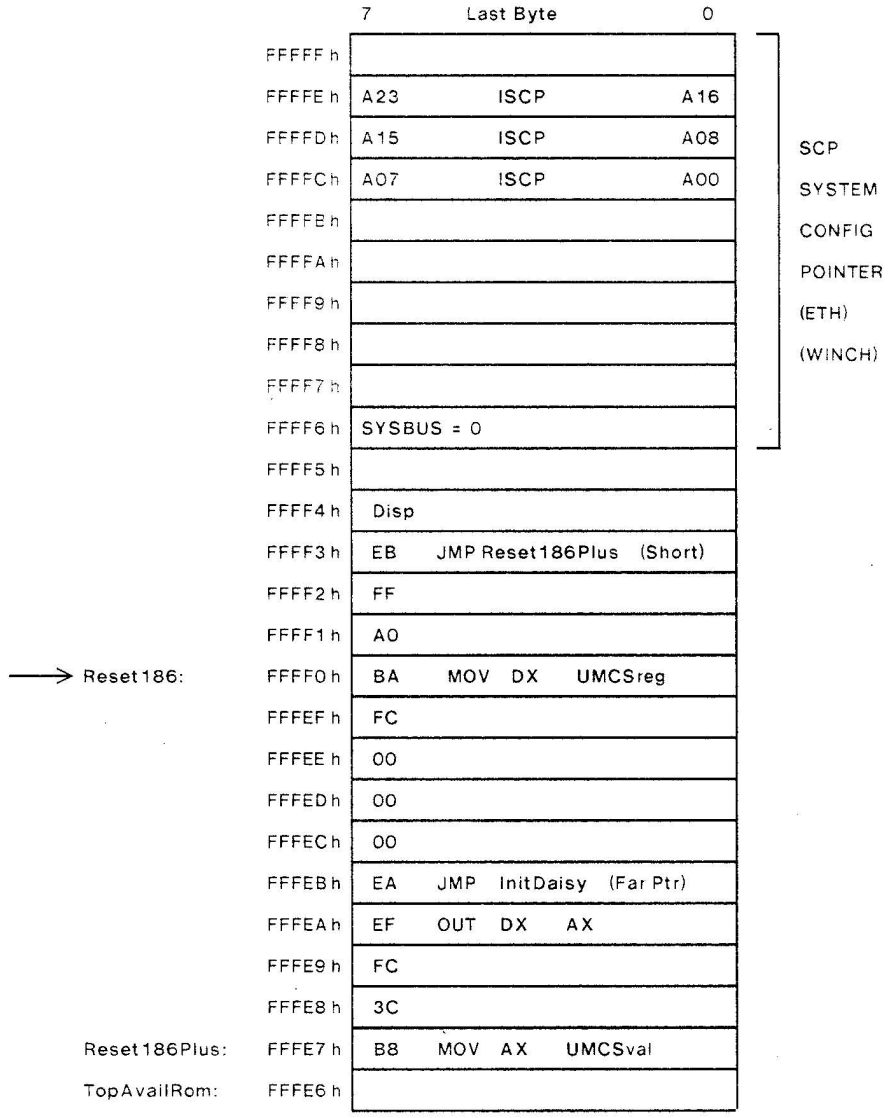


Baud Rate	*Time Const*	*Error*
19200	13	0.16 %
9600	26	0.16 %
7200	35	0.79 %
4800	52	0.16 %
3600	69	0.64 %
2400	104	0.16 %
2000	125	0 %
1800	139	0.08 %
1200	208	0.16 %
600	417	0.08 %
300	833	0.04 %
150	1667	0.02 %
134.5	1859	0.01 %
110	2272	0.03 %
75	3333	0.01 %
50	5000	0 %

$$\text{Time Constant} = \frac{4 \times 10^6}{(\text{baud rate}) \cdot (16)}$$

$$\%\,\text{Error} = \text{abs}\left[\frac{4 \times 10^6}{(\text{time const}) \cdot (\text{baud rate}) \cdot (16)} - 1\right] \times 100\%$$

XEROX SDD	Project		File	Designer	Rev	Date	Page
	Daisy	Timer Assignments	DIOP55.silx	Tsang	C	4/23/84	55



Note : This is the way the uppermost bytes of EProm is set up in order to support ENet & RDC before Memory with mapping is available.