XDF-50

OPERATION AND MAINTENANCE

MANUAL

XEBEC
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XEBEC SPECIFICATION NO. 200105

XEBEC MOVING HEAD DISK

FORMATTER

MODEL NO. XDF-50

OPERATION & MAINTENANCE MANUAL

Revision "B"
June 9, 1976

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SECTION I
INTRODUCTION

1.1 GENERAL

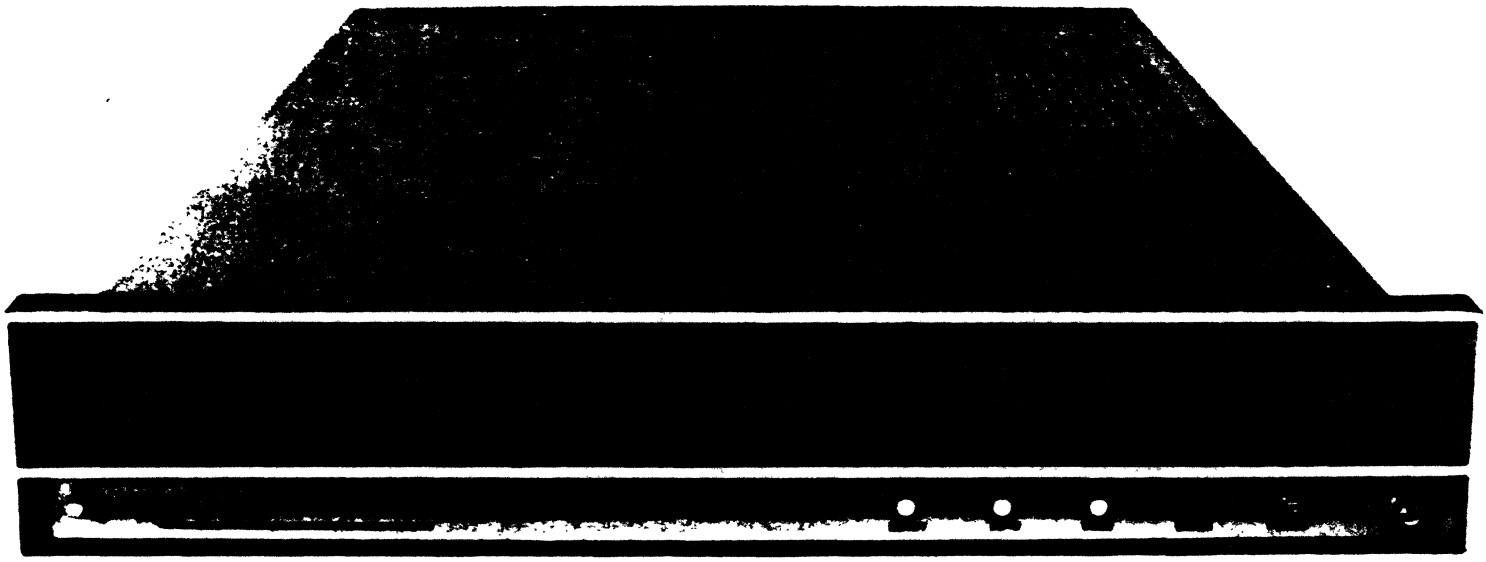
The Xebec Moving Head Disk Formatter (XDF-50) see Figure 1, described in this manual has been designed to be used with a wide variety of moving head disk drives manufactured by Microdata, CDC, Pertec and others.

The data conversion and control logic functions of this disk formatter significantly simplifies the logic design that is normally required to interface these Disk Drives to any modern mini-computer.

The XDF-50 design extensively utilizes medium scale integration (MSI) integrated circuits and incorporates conservative printed circuit design practices to produce a highly reliable, low cost piece of peripheral equipment.

1.2 SPECIFICATIONS

The specifications for the disk formatter are shown in Table 1.1.



XDF-50 XEBEC DISK FORMATTER
FIGURE 1.1

TABLE 1.1
DISK FORMATTER SPECIFICATION

	Parameter	Unit	Selected By
1.	Word Length	12 Bit Word 16 Bit Word	14 Pin DIP Program Plug
2.	Sector Size	32 Words 64 Words 96 Words 128 Words 160 Words 192 Words 224 Words 256 Words	14 Pin DIP Program Plug
3.	Sectors/Revolution	12 Sectors 16 Sectors 24 Sectors 32 Sectors	Automatically uses number of sector slots on disk pack.
4.	Size of Cylinder Address Register	9 Bits	
5.	Size of Command Register	12 Bits	
6.	Size of Status Register	12 Bits	
7.	Size of Word Count Register	9 Bits	
8.	Number of Disk Drives which may be connected.	4 Maximum	
9.	Spindle Speed	1500 RPM or 2400 RPM	
10.	Packing Density	2200 BPI	
11.	Words/Sector		

12	16	24	32	Number of Sectors
-	256	160	96	12 Bit Word
256	192	128	64	16 Bit Word

TABLE 1.1
DISK FORMATTER SPECIFICATION
(Continued)

Parameter

12. Words/Disk Drive (Single Platter) (Based on 207 Cylinders)

12	16	24	32	# of Sectors
-	1,695,744	1,589,760	1,271,808	12 Bit Word
1,271,808	1,271,808	1,271,808	1,271,808	16 Bit Word

13. Words/Disk Drive (Dual Platter) (Based on 203 Cylinders)

12	16	24	32	# of Sectors
-	3,325,952	3,118,080	2,494,464	12 Bit Word
2,494,464	2,494,464	2,494,464	2,494,464	16 Bit Word

14. Bit Transfer Rate — 1588.5 KHz at 1500 RPM*
2500.0 KHz at 2400 RPM

* A crystal change is required to change frequencies.

SECTION 2
SYSTEM DESCRIPTION

2.1 INTRODUCTION

When used in conjunction with various moving head drives, the XDF-50 provides all control and timing necessary to form a data storage/retrieval system suitable for use in small-to-medium scale data processing applications. Compatibility and interchangeability of disk packs is provided between disk drives and formatters.

2.2 FUNCTIONAL DESCRIPTION

The XDF-50 is designed to operate over a wide range of parameters. These variable parameters are:

1) 12 Bit or 16 Bit Word Lengths.
2) Number of Sectors per Revolution.
3) Number of Words per Sector.
4) 1500 RPM or 2400 RPM Disk Speed.
5) Manufacturer of Disk Drive.
6) Number of Disk Drives.

A maximum of four disk drives can be attached to each formatter. They must be of the same type with respect to the first five variable parameters, but may be any combination of single or dual platters.

2.3 MECHANICAL PACKAGING

2.3.1 Disk Formatter

The disk formatter is rack mountable in a standard EIA relay rack. Front access is accomplished by use of slides. Physical dimensions are as follows:

a)	Overall Depth:	29.0 Inches (includes cable bends and air flow)
b)	Unit Height:	3.5 Inches maximum
c)	Unit Width:	19.0 Inches maximum

d)	Weight:	30.0 Pounds maximum
e)	Mounting:	19 Inch EIA Rack Mounting Utilizing both Front and Back Rails
f)	Rack Space Required:	3.5 Inches maximum

2.4 POWER SUPPLY

The AC power requirements for the formatter are as follows:

115 ± 10% VAC, Single Phase
47 - 63 Hz, Fused at 1.5 Amperes
230 VAC Optional

2.5 SECTOR FORMAT

Each sector is divided as shown in Figure 2.1. As can be seen by this figure these divisions are as follows:

a) Zeros Field 1 - used for bit synchronization

b) Sync Word 1 - used for word synchronization

c) Preamble - identifies cylinder /sector/write protect/bad sector

d) Write Amplifier Turn-On Gap

e) Zeros Field 2 - used for bit synchronization

f) Sync Word 2 - used for word synchronization

g) Data Field

h) Cyclic Redundancy Checkwords

i) Write Amplifier Turn-Off Gap

j) Spare

The sector format is designed in this manner for the following reasons:

1) Positive checking of cylinder position.

2) Positive checking of sector and head selection.

3) Positive means of programming write protection into each individual sector.

4) A method of flagging bad sectors.

The write amplifier turn-on gap which follows the preamble allows time for the amplifiers to be turned on after the preamble has been read. This technique eliminates the need for rewriting the preamble each time a sector is updated, and also eliminates the need to wait one extra revolution to write a sector after checking the preamble.

The size of the initial gap has been chosen to allow full interchangeability between disk drives and disk drives between formatters.

2.6 FORMATTER COMMANDS

The formatter and disk commands that are available to the user are summarized below. A detailed description of these commands is contained in Section 3.

A. Load Cylinder Address Register

B. Load Microprogrammed Command Word Register

1. Select Unit

2. Select Sector

3. Select Head

4. Perform Operation

a. Write preamble and 1 sector

b. Check preamble and write 1 sector

c. Check preamble and read 1 sector

d. Read diagnostic mode

e. Ignore write protect and write 1 sector

f. Write diagnostic mode

g. Ignore Preamble and read 1 sector

C. Load Word Count Register

D. Read Status Register

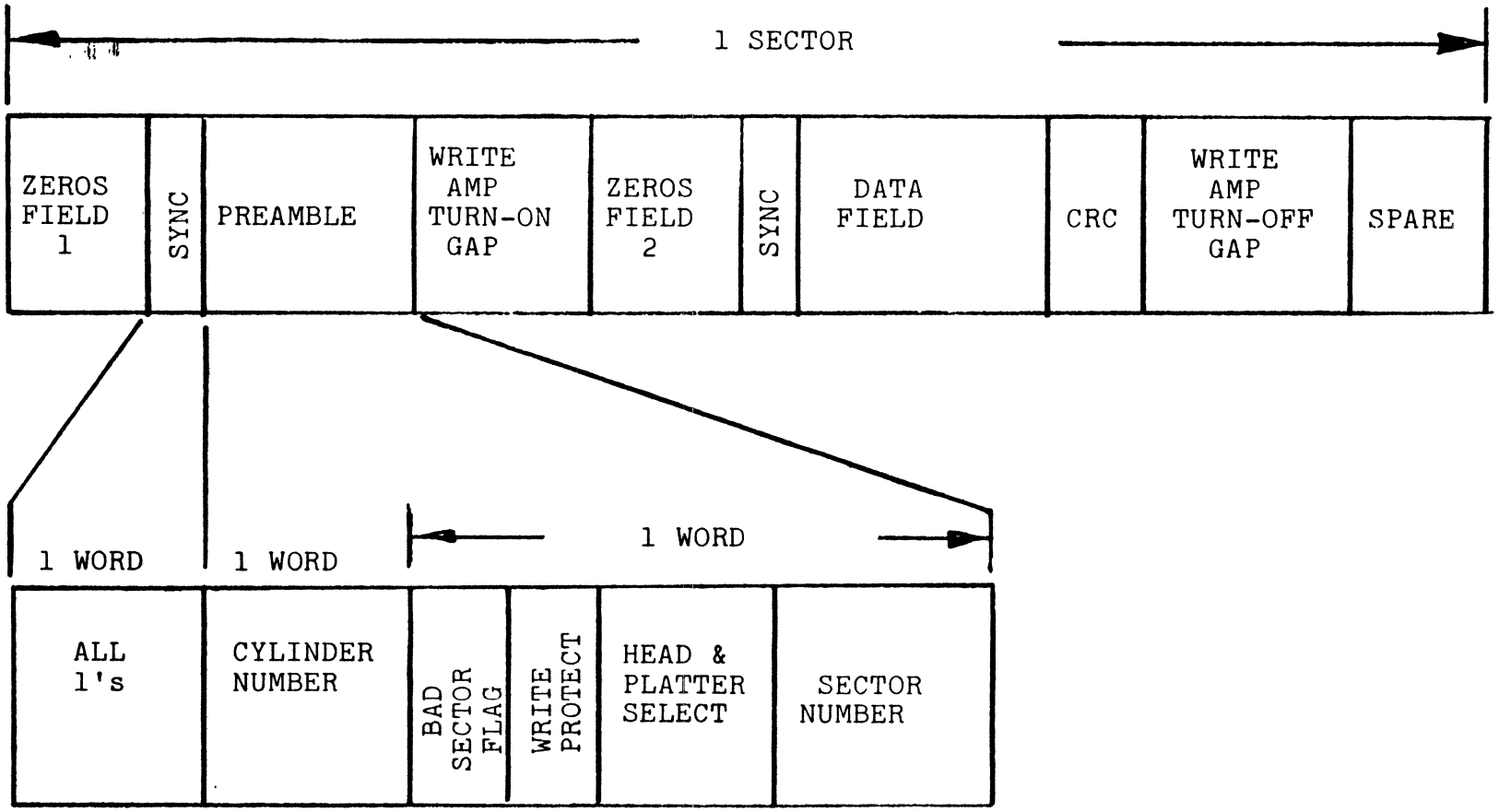

1 SECTOR
ZEROS FIELD 1
SYNC
PREAMBLE
WRITE AMP TURN-ON GAP
ZEROS FIELD 2
SYNC
DATA FIELD
CRC
WRITE AMP TURN-OFF GAP
SPARE
1 WORD
1 WORD
1 WORD
ALL 1's
CYLINDER NUMBER
BAD SECTOR FLAG
WRITE PROTECT
HEAD & PLATTER SELECT
SECTOR NUMBER

FIGURE 2.1

2.7 WRITE PROTECTION

Two levels of write protection are provided by the disk formatter. These are as follows:

1. Programmable write protection by use of a flag bit in the preamble, and

2. Absolute write protection by switch.

2.7.1 Write Protection Switch Location

On dual platter models the write protection switches located on the disk drive are sensed by the disk formatter.

The write protection switches are located behind the front panel of the formatter when the option is installed.

2.8 CONTROLS AND DISPLAYS

2.8.1 Controls

A. Power ON/OFF Switches

A toggle ON/OFF switch is provided on the front panel of the formatter. This toggle switch controls the AC power to the formatter power supply.

B. Write Protect Switches

Four write protect switches one for each drive unit are located behind the front panel of the formatter. These switches are provided when option is installed only.

2.8.2 Displays

A. Indicators

As can be seen by Figure 1.1, the front panel of the formatter has four indicators. These are:

1.	Read Indicator	The formatter is processing a read type instruction.
2.	Write Indicator	That the formater is processing a write type instruction.
3.	Error (Red Light)	The formatter has found an error during the last operation.
4.	Ready	The selected disk unit is on and ready to read or write.

2.9 ENVIRONMENT

2.9.1 Operating

Temperature:	+50° to +104°F, ambient
Humidity:	10% to 80% RH, 85°maximum wet bulb temperature.

2.9.2 Non-Operating and/or Storage

Temperature:	-40°F to +150°F
Humidity:	10% to 95% RH, non-condensing

SECTION 3
FUNCTIONAL OPERATION

3.1 INTRODUCTION

In this section there is a more detailed description of the commands which may be issued to the formatter. These commands are divided into two types:

1) Disk Commands which cause the disk to position to a specified cylinder, and

2) Formatter Commands which load or read registers in the formatter.

Neither disk commands nor formatter commands should be issued to the Formatter when it is Busy. See Figure 3-1 for a description of the proper sequence for issuing disk and formatter commands.

3.2 DISK COMMAND

The disk command, SEEK Cylinder, is routed through the formatter cylinder address register to the selected disk drive unit. This causes the positioner to move to the required cylinder address. This command does not cause the formatter to go Busy.

When an Output Strobe Pulse (OSP) is issued with the Register Address Bus (RAB)=011, the 9 bit formatter cylinder address register, Figure 3-2, is loaded from the Coupler Output Bus (CPOB) 0-8 lines. Loading this register causes a SEEK (on the drive unit selected by last command issued) to the Cylinder number loaded into the register. The disk drive performs a validity check on the address. A valid address causes the positioner to move to the required cylinder address.

After the SEEK has been initiated by the loading of this register, any other command (except SEEK) may be issued to the formatter immediately. Another SEEK cylinder command may be issued to a different disk unit after ten (10) microseconds. The 10 microseconds wait time is necessary to allow the disk drive to accept the SEEK address. On disk formatters which have more than one disk drive attached, the SEEK commands can be overlapped between drive units, i.e., two or more drive units may be seeking simultaneously while at the same time data transfers are taking place on another disk unit.

The cylinder address register must not be loaded if BUSY = 1, or if the SEEK bit of the status word = 1. Loading the cylinder address register leaves BUSY unchanged and does not effect DONE.

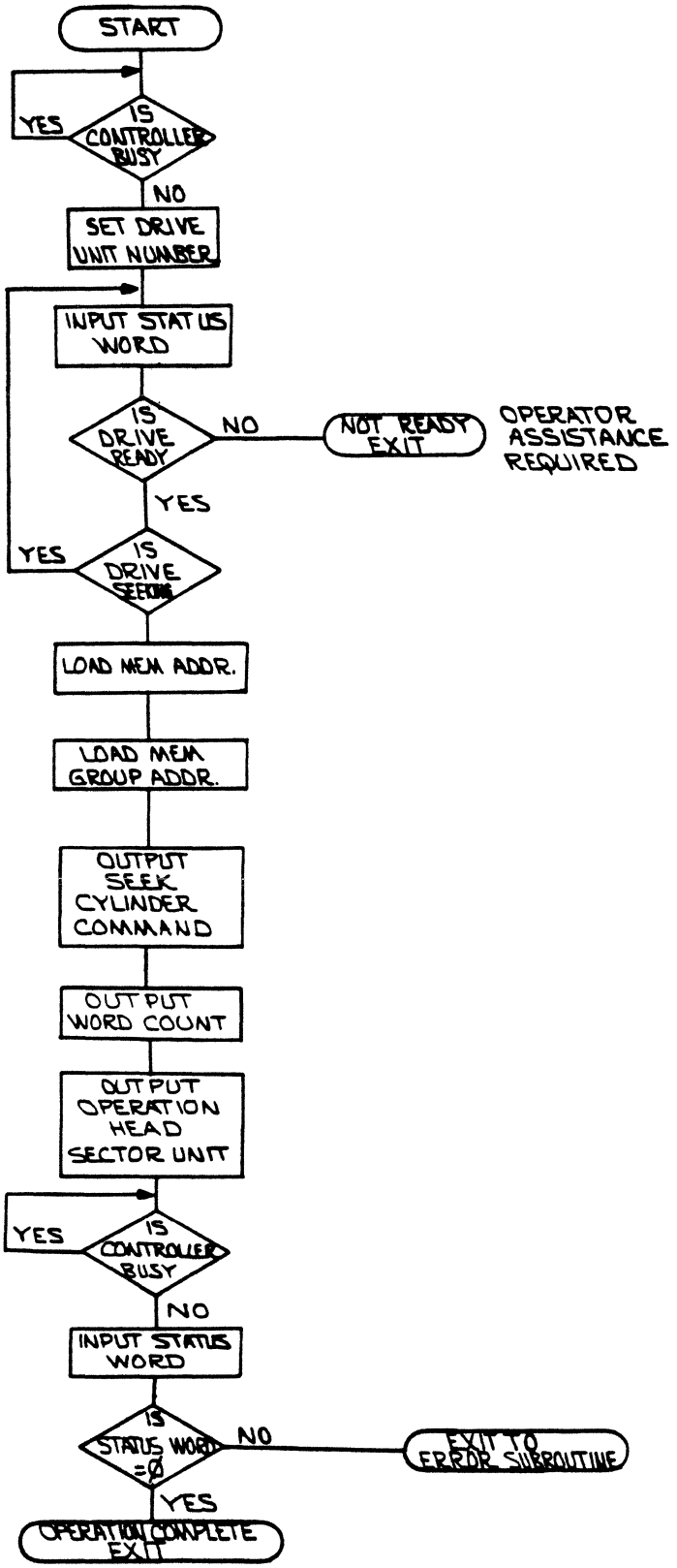
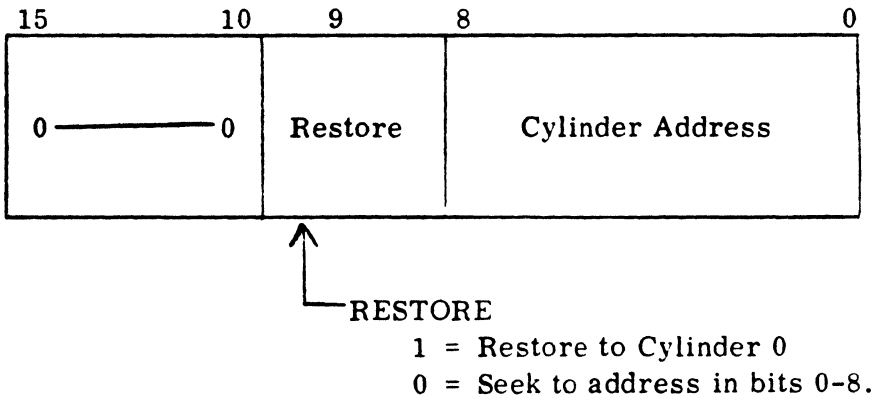

START
IS CONTROLLER BUSY
YES
NO
SET DRIVE UNIT NUMBER
INPUT STATUS WORD
IS DRIVE READY
NO
NOT READY EXIT
OPERATOR ASSISTANCE REQUIRED
YES
IS DRIVE SEEKING
YES
LOAD MEM ADDR.
LOAD MEM GROUP ADDR.
OUTPUT SEEK CYLINDER COMMAND
OUTPUT WORD COUNT
OUTPUT OPERATION HEAD SECTOR UNIT
IS CONTROLLER BUSY
YES
NO
INPUT STATUS WORD
IS STATUS WORD =Ø
NO
EXIT TO ERROR SUBROUTINE
YES
OPERATION COMPLETE EXIT

FIGURE 3.1



CYLINDER REGISTER

Figure 3.2

If the drive unit number has been changed since a SEEK command was initiated, the cylinder address register must be reloaded before the data transfer command can be issued. This is necessary so that the cylinder address portion of the preamble compares correctly.

Bit 9 of the cylinder address register is called the restore bit. A "1" in this bit causes the drive to seek to cylinder 0 without regard to the value of the bits in the rest of the register.

3.3 FORMATTER COMMANDS

These commands involve the transfer of data and control words to or from the disk and can be executed in either a single seek or seek overlap mode. As stated before, they may be issued while the disk is still engaged in a SEEK.

There are three basic formatter commands. All control functions and data conversion of signals from the disk are handled by these formatter commands. The user communicates with the disk formatter by sensing BUSY and DONE status and loading or reading registers.

3.3.1 Command Register

Issuing an OSP with the RAB=101 loads the 12 bit formatter command register from CPOB 0-11 lines. Loading this register causes BUSY to be set and initiates an operation. When the operation has been completed and BUSY goes off, a DONE pulse is issued.

NOTE: The register must not be loaded when BUSY = 1.

The format of the Command Register is as follows:

CPOB

15 14 13 12	11 10 9	8 7	6 5 4 3 2	1 0
0 ——— 0	Operation	Head Select Addr.	Sector Address	Unit Nbr.

Bits

15 - 12 Not Used = 00

11 - 9 OPR - Operation Code = Shown in Table 3.1.

TABLE 3.1

	OPERATION	ACCEPTABLE WORD COUNT	ERROR WHICH TERMINATED OPERATION BEFORE DATA TRANSFER OCCURS	ERROR WHICH MAY OCCUR AFTER DATA TRANSFER	COMMENTS
000	No-Operation	N.A	NRDY, CAE	NONE	No operation is performed. BUSY goes off immediately, DONE is generated. This operation is used to change the unit number without performing a data transfer.
001	Write Preamble and 1 Sector	2-(N+2) Inclusive	NRDY, WPE, CAE, TMO,	RATE, WCE, FTE	Write Preamble and Data up to 1 Sector in length depending upon value in word count register. The first two words transferred specify the preamble to be recorded as shown in Table II.
010	Check Preamble and Write 1 Sector	0 – N Inclusive	NRDY, WPE, CAE, PCE, BSEC, TMO, FTE	RATE, WCE	The previously recorded preamble is checked by the formatter, and data up to 1 sector in length is written on the disk. WC may be 0 N inclusive. If WC is less then N, the remaining words in the sector are filled with zeros.
011	Check Preamble and Read 1 Sector	0-N+2	NRDY, CAE, PCE, BSEC, TMO FTE	CRCE, RATE, WCE	The preamble previously recorded is checked by the formatter and data up to 1 sector in length are read from the disk. If WC is in the range 0 N inclusive, WC words will be transferred. If WC is N+1 or N+2, the entire data portion of sector is transferred plus the CRC word(s) will be input as the last word(s).
100	Read Diagnostic	N+4	NRDY, CAE, TMO, FTE,	CRCE, RATE, WCE	The preamble, 1 sector of data and the Cyclic Redundancy Check (CRC) words are read from the disk and tranferred through the formatter. The preamble words are the first two words input followed by N Data Words followed by two CRC words.
101	Check Preamble & Write a Sector but Ignore Write Protect Bit in Preamble.	0-N	NRDY, WPE, CAE, PCE, BSEC, TMO, FTE	RATE, WCE	This operation is identical to 010 except the transfer is not terminated if the write protect bit in the preamble is set. If write protect switch is on, or if the rest of the preamble does not check, writing will not occur.
110	Write Diagnostic	N+4	NRDY, WPE, CAE, TMO, FTE	RATE, WCE	The preamble 1 sector of data and the CRC words are transferred through the formatter and written on the disk. This instruction differs from 001 because the CRC words are transferred as data and are not generated by the formatter
111	Ignore Preamble and Read a Sector	0 – N Inclusive	NRDY, CAE, TMO, FTE	CRCE, RATE, WCE	The preamble is not checked and up to 1 sector of data is read.

Bits

8 - 7 Head - Head Select Address

The head selected to be used for reading or writing is assigned as follows:

Single Platter Drive

00 Upper Head
01 Lower Head

Dual Platter Drive

00 Upper Head - Removable Disk
01 Lower Head - Removable Disk
10 Upper Head - Non Removable Disk
11 Lower Head - Non Removable Disk

6 - 2 Sector - Sector Address

Data transfer will occur on the sector specified by this 5 bit number. The acceptable range is from $0-S_8$ where:

S_8 is
37_8 for 32 sector disks
27_8 for 24 sector disks
17_8 for 16 sector disks
13_8 for 12 sector disks

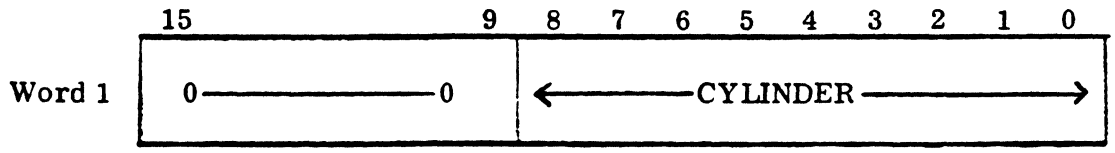
1 - 0 Unit - Unit Number

Unit selected for use by the formatter.

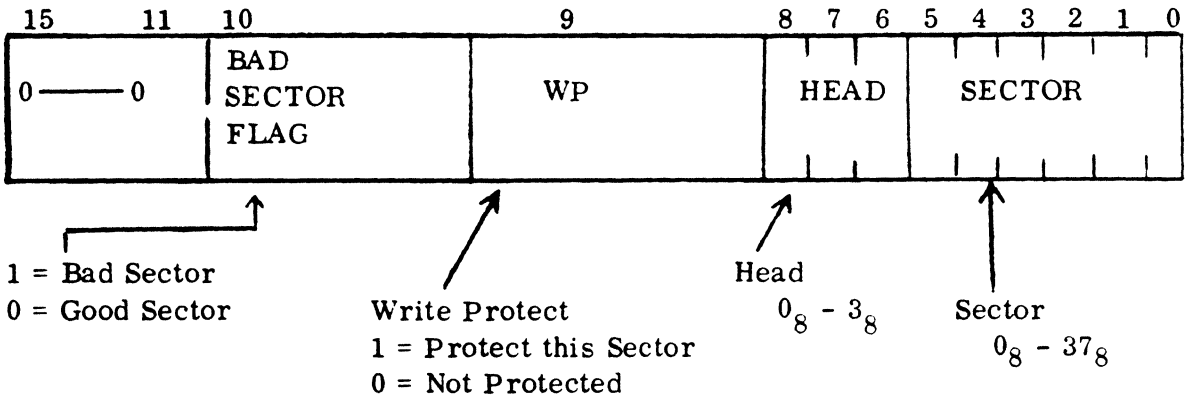
Code	Selected Unit
00	0
01	1
10	2
11	3

TABLE 3.2

PREAMBLE DATA FORMAT



Cylinder Values (0_8 - 624_8)



3.3.2 Word Count Register

Issuing an OSP with the RAB=111 loads the 9 bit formatter word count register from CPOB 0-8 lines. The word count register is used to determine how many words of data to transfer through the formatter for READ or WRITE operations. Although the word count register is a 9 bit register, the actual maximum number of bits that may be loaded into the register is a function of the sector size (N) hardwired into the disk formatter. See Table 3.3. If the specified word count is too large, an error flag is set in the Status Register at the end of the data transfer operation. This error flag indicates that the Word Count Register did not count down to zero.

Note: This register must not be loaded when BUSY=1. Loading the word count register leaves BUSY unchanged and does not affect DONE.

TABLE 3.3
SECTOR SIZE (N)
WORDS PER SECTOR

Decimal	N Octal
32_{10}	40_8
64_{10}	100_8
96_{10}	140_8
128_{10}	200_8
160_{10}	240_8
192_{10}	300_8
224_{10}	340_8
256_{10}	400_8

3.3.3 Status Register

Issuing an Input Strobe Pulse (ISP) with RAB=011 causes the status word of the formatter to be placed on Coupler Input Bus (CPIB) 0-11 lines.

NOTE: This register must not be accessed while BUSY=1.

The format of Status Register is as follows:

15 - 12	11	10	9	8	7	6	5	4	3	2	1	0
0—0	NRDY	WPE	CAE	PCE	TMO	FTE	CRCE	RATE	BSEC	WCE	0	SEEK

Bits

15 - 12 Not Used = 00

11 NRDY - Drive Not Ready

The currently selected unit is not connected, not turned on or not up to speed.

10 WPE - Write Protect Error

A write operation was attempted on a write protected sector or unit. No data transfer occurred.

9 CAE - Cylinder Address Error

A cylinder address which exceeded the range of the selected drive unit was loaded into the cylinder address register. No data transfer occurred.

8 PCE - Preamble Check Error

The cylinder or the sector portion of the preamble did not check. Data transfer did not occur.

7 TMO - Time Out Error

The unit did not go NOT BUSY within 2 seconds. No data transfer occurred. This error is usually caused by selecting a sector number which does not exist on the selected drive unit.

Bits	
6	FTE - Format Error Either a sector size too large for the disk drive connected to the formatter has been selected or no sync word was found in the specified sector indicating that the disk is not formatted. Data transfer may not have occurred.
5	CRCE - CRC Error The CRC word recorded at the end of the sector did not compare with the one calculated on the data in the sector. All specified data transfers occurred.
4	RATE - Rate Error The user did not clear the Data Flag within the specified length of time (by sending or accepting a new word.) Data transfer occurred up through the end of the sector but some words were missed.
3	BSEC - Bad Sector The Bad Sector Flag was set to 1. Data transfer did not occur.
2	WCE - Word Count Error The word count was greater than zero at the completion of the last operation. A full sector of data may have been transferred.
1	Not Used = 0
0	SEEK - Unit Seeking The disk unit last selected by a UNIT command is still executing a SEEK cylinder. If the user wishes to change the cylinder address on this unit, this bit must first go to zero.

SECTION 4
THEORY OF OPERATION

4.1 GENERAL

The heart of the Disk Formatter is the registers. All communications between the mini-computer and the Disk Formatter are accomplished by loading and reading of these registers. These registers are selected by a group of three lines called Register Address Bus (RAB) which address uniquely one of the registers to be loaded or read. In conjunction withRAB lines, there is an Output Strobe Pulse (OSP) or an Input Strobe Pulse (ISP) which strobes the data into registers or reads the data from register, respectively. In this manner, the registers are accessed.

The data is transmitted from the computer to the registers on Coupler Output (CPOB) lines, and from the registers back to the computer by means of Coupler Input Bus (CPIB) lines.

All diagrams shown in this section are provided as reference for the text which describes logic operation. In some cases, logic not pertinent to the discussion is blocked out of the drawing. A complete, up to date set of logics is included with each XDF-50 formatter. The user should refer to these logics for maintenance of his system since these prints describe the configuration of the XDF-50 as shipped.

4.2 REGISTERS

Before any data READ/WRITE operations can begin, the Disk Formatter registers must be loaded with data that describe cylinder positioning, number of data words to transfer, and what operations must be performed. The registers that must be loaded to perform these functions are in order of their loading sequence.

A. Cylinder Address Register

B. Word Count Register

C. Command Register

The mini-computer coupler transmits four signals to the formatter which are used to select the registers for loading. These are the three RAB signal lines mentioned previously which are decoded by the Disk Formatter and strobed by an Output Strobe Pulse. This loads the selected register. The balance of this section is concerned with a fuller explanation of these registers and their timing sequence.

4.2.1 Cylinder Address Register

The cylinder address register is shown in Figure 4.1. As can be seen by this figure, the cylinder address register is a 12-bit register. It is composed of three Quad Latches (SN7475) which drive a series of SN7438 power drivers. The SN7438 power drivers are used to drive the terminated cylinder address lines.

4.2.1.1 Loading Cylinder Address Register

The timing sequence for the loading of the cylinder address register is as shown in Figure 4.2. The pin numbers shown on Figure 4.2 refer to Figure 4.1.

Loading the cylinder address register causes a cylinder address strobe (CYL STROBE) to be generated to the disk unit. This strobe transfers the cylinder number from the cylinder register in the Disk Formatter to a like cylinder register in the disk drive. The disk unit performs a validity check on the address. A valid address causes the disk positioner to move to the required cylinder address. In case of an invalid address, a cylinder address error bit is returned by the disk unit.

After the SEEK has been initiated by the loading of this register, any other command (except SEEK) may be issued to the Disk Formatter. However, another SEEK command may be issued to a different disk drive within ten microseconds. As can be seen by Figure 4.2, this means that in a daisy chained disk configuration the Disk Formatter can cause SEEK's to be overlapped between disk drives.

4.2.2 Word Count Register

The word count register is shown in Figure 4.3. As can be seen by this Figure, the word count register is composed of two SN74193 up/down counter chips and two SN7474 D type flip flops, creating a 9 bit register. The purpose of this register is to tell the Disk Formatter how many words within a sector are to be transferred

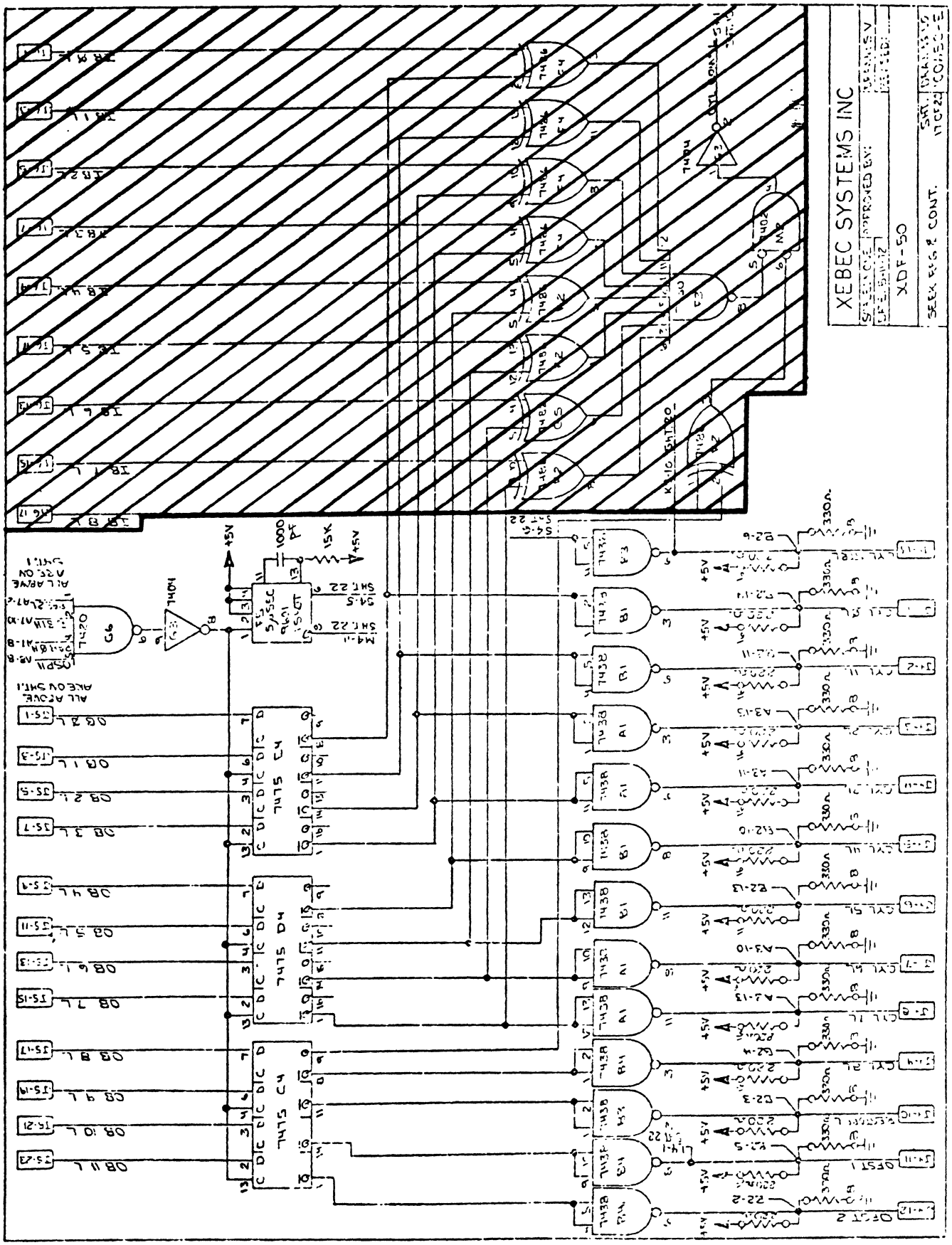


FIGURE 4'.1
Cylinder Address Register

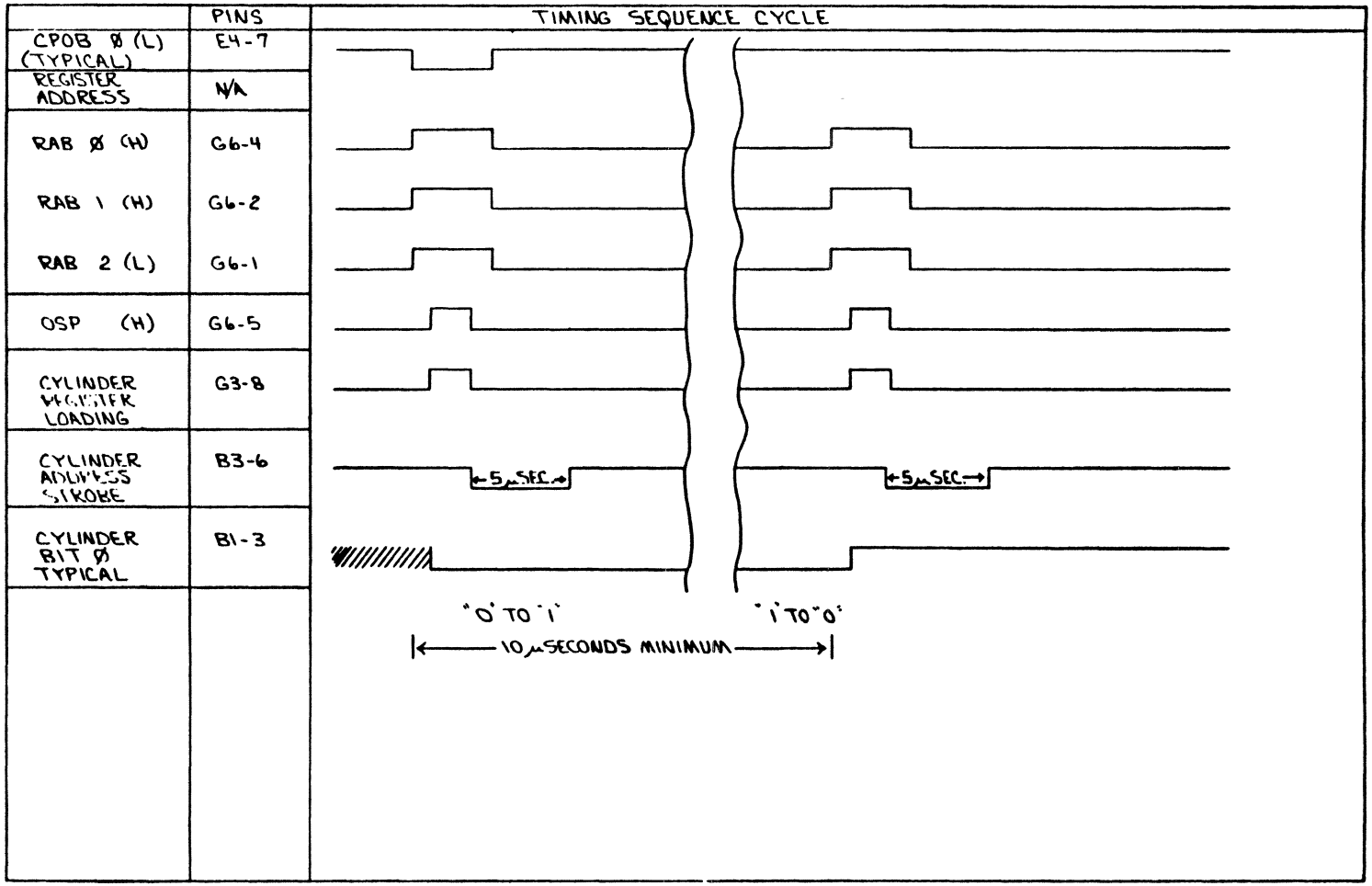


FIGURE 4.2

TIMING DIAGRAM FOR CYLINDER ADDRESS REGISTER

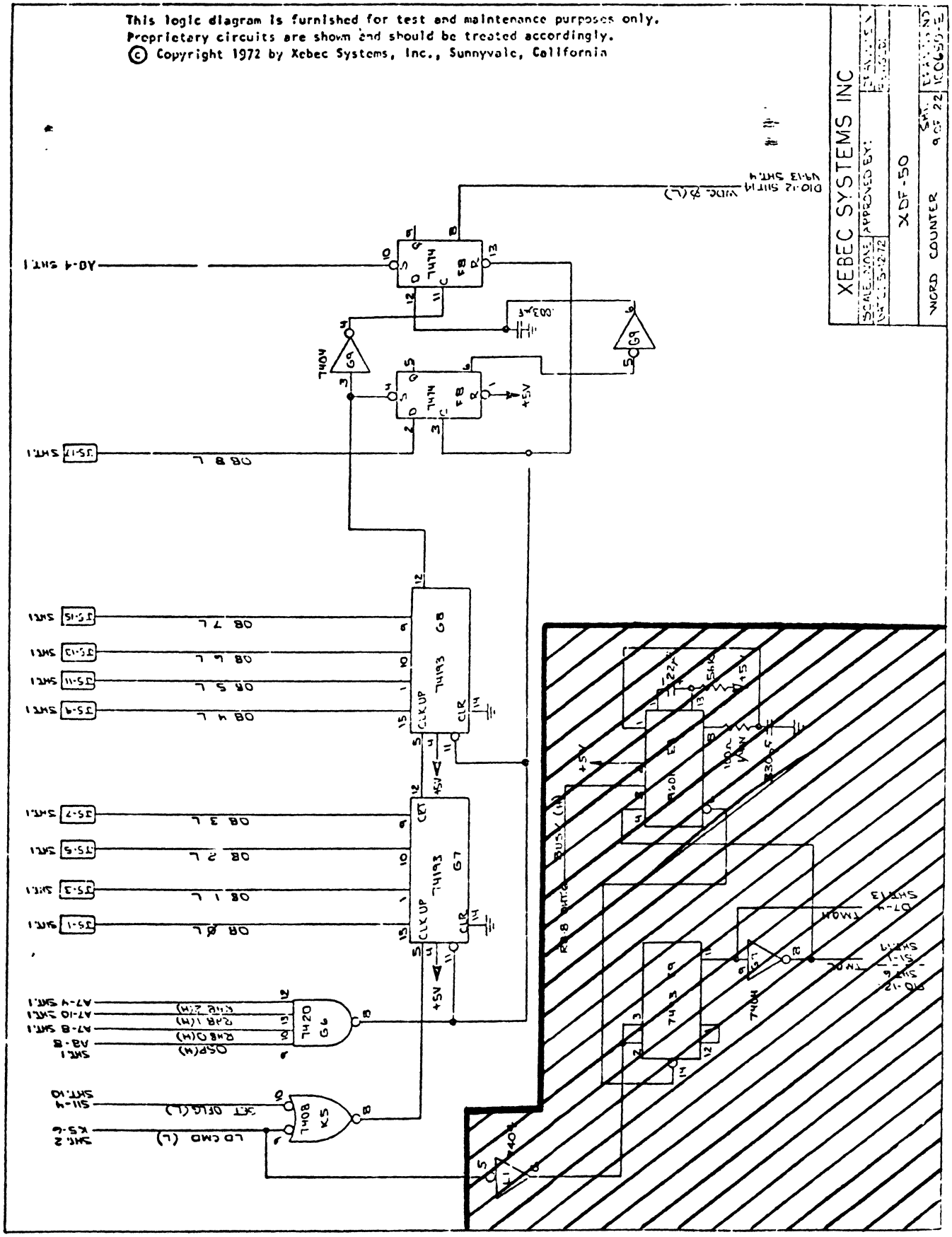


FIGURE 4.3
Word Count Register
4-5

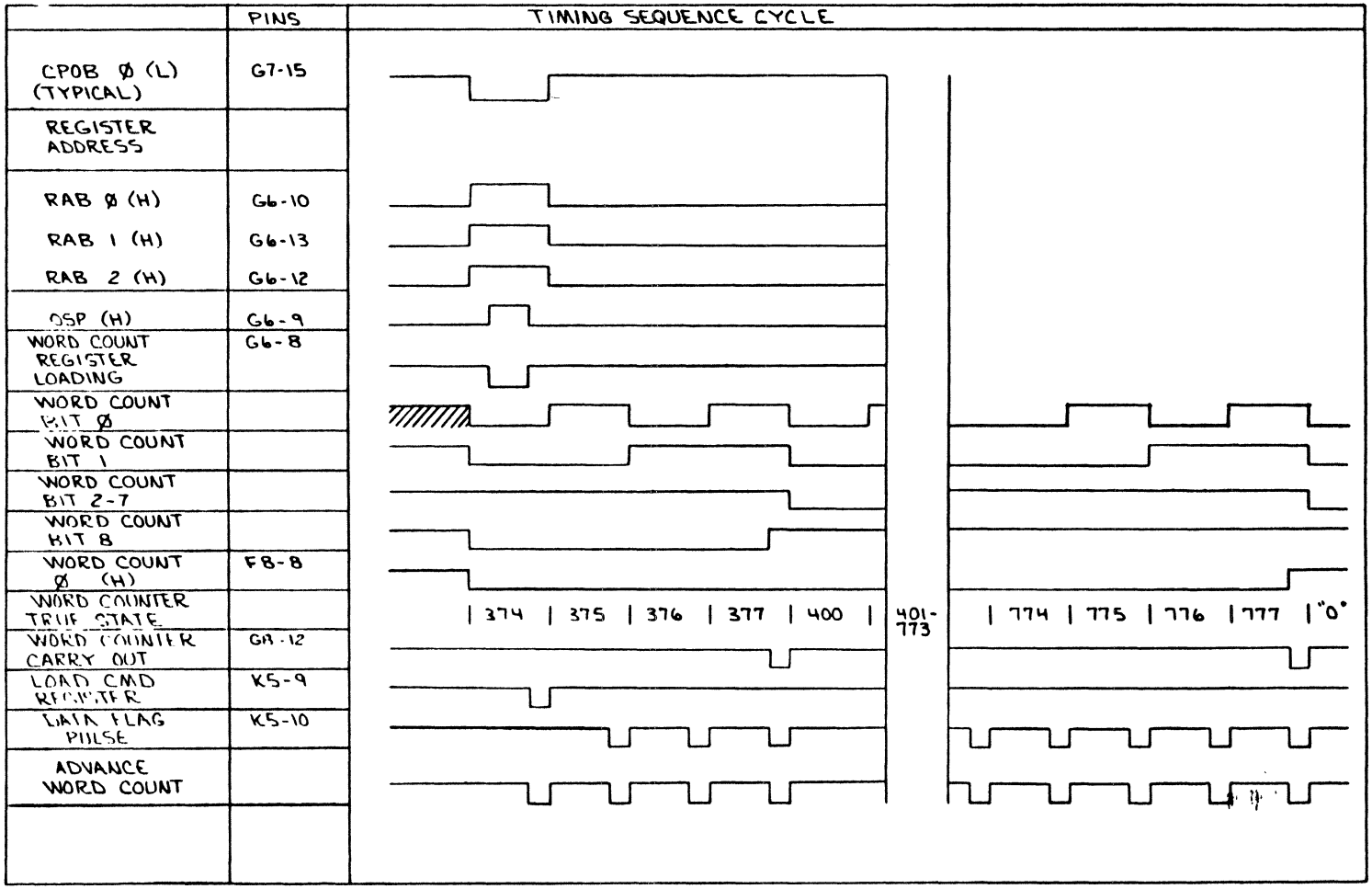


FIGURE 4-4

TIMING DIAGRAM FOR WORD COUNT REGISTER

4.2.2.1 Loading Word Count Register

The timing sequence for the loading of the word count register is as shown in Figure 4.4. The timing sequence shown is for a word count of "403_8".

Since the data on the CPOB is carried as low true, the "1's" complement of "403_8", is loaded into the word count register as a high true state. To change the "1's" complement into a "2's" complement, an initial advance of the word count register is accomplished by incrementing the counter when the command register (K5-9) is loaded. This assumes that the command register will only be loaded once following the loading of the word count register.

Therefore, each subsequent advance of the word count register is accomplished on the trailing edge of the Set Data Flag Pulse. When the word count register reaches "0" flip flop (F8-9) is set. This causes the Disk Formatter to quit generating Data Flag pulses.

As can be seen by Figure 4.4 the word counter "0" flip flop is not set on the first overflow of the Carry Out Signal in the example of "403_8" shown but is set on the second overflow. Whether F8-9 is set on first overflow or second overflow depends upon the value set in F8-5. Since F8-5 acts as the MSB of the counter it controls the setting of the word counter "0" flip flop.

The word counter "0" flip flop will remain set until a new value is loaded into the word count register.

4.2.3. Command Register

The command register is shown in Figure 4.5. As shown by this figure, the command register is a 12 bit register being composed of three SN7475 bistable latches. The register is loaded by data on the CPOB (0-11) lines. The register selection is accomplished by a RAB address of 101 and an OSP.

The most significant 3 bit outputs are decoded by the SN7442 binary decoder into 8 possible operations (0-7). Two bits go to a head select address (1 bit for platter select and 1 bit for head select), and 5 bits go to a comparator circuit where they are compared against a Sector Counter. The least significant 2 bits are decoded by a set of SN7438 drivers. These drivers are used to select 1 out of 4 possible disk units whose address are 0-3.

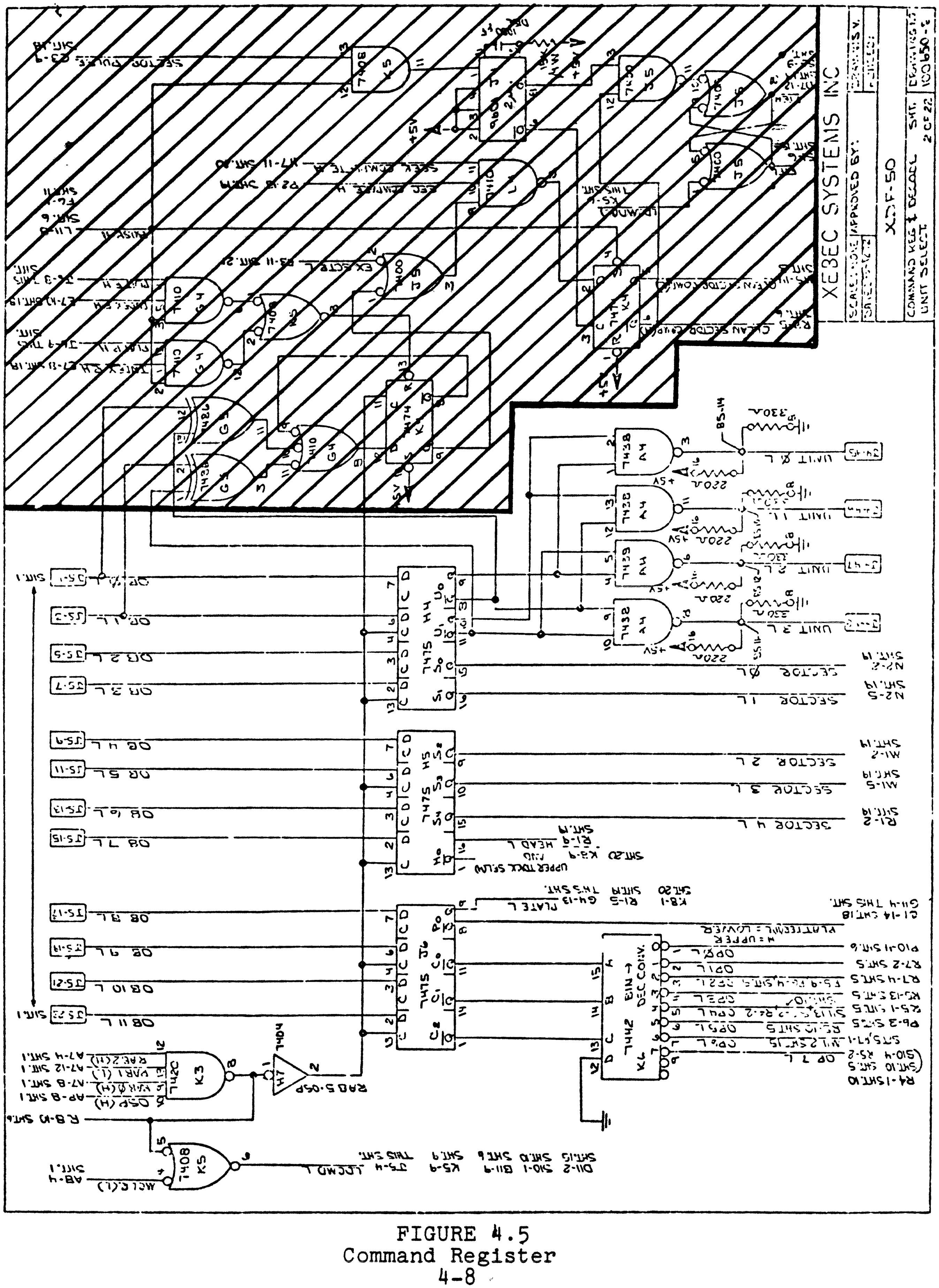


FIGURE 4.5
Command Register

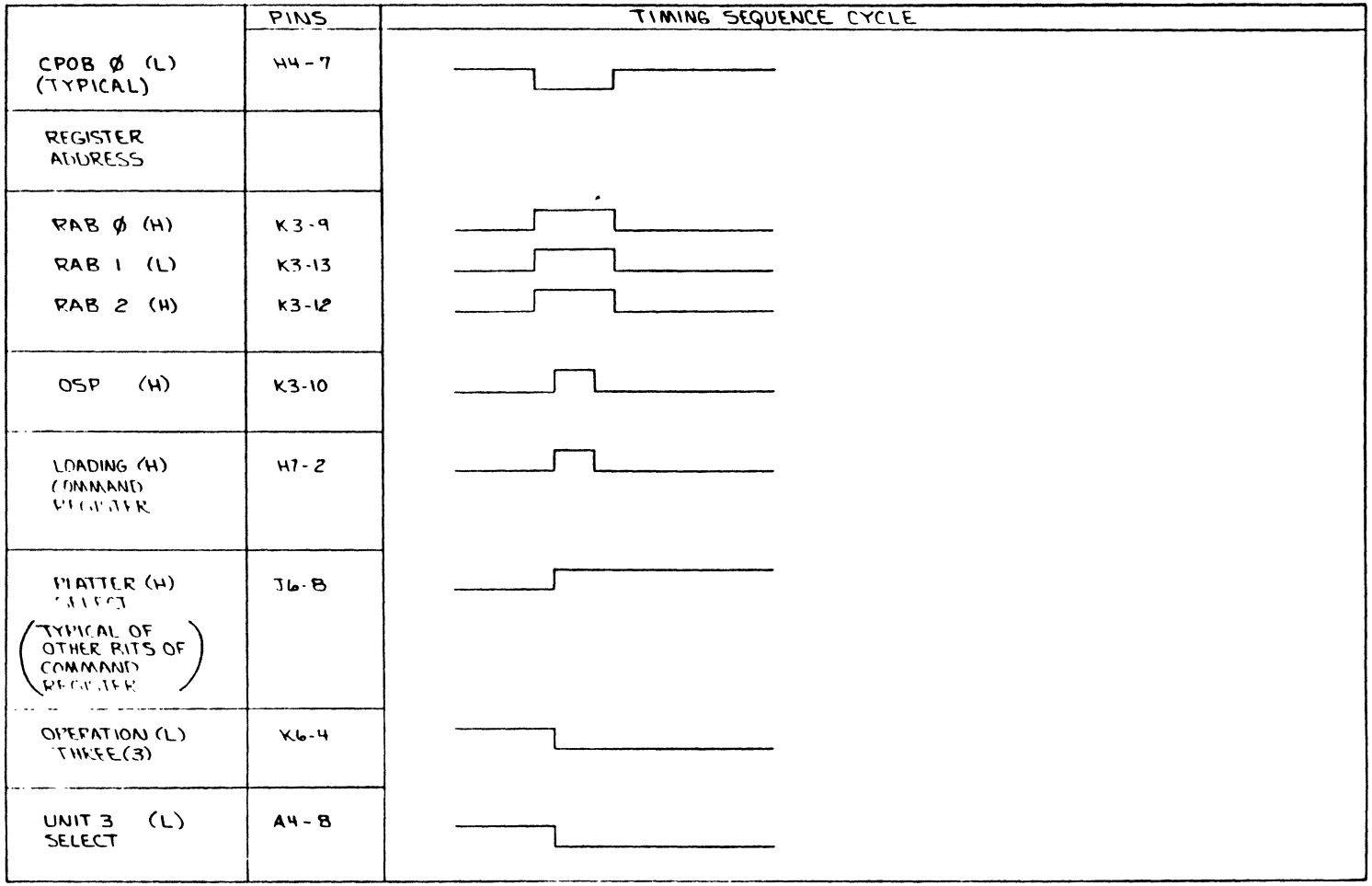


FIGURE 4.6

TIMING DIAGRAM FOR COMMAND REGISTER

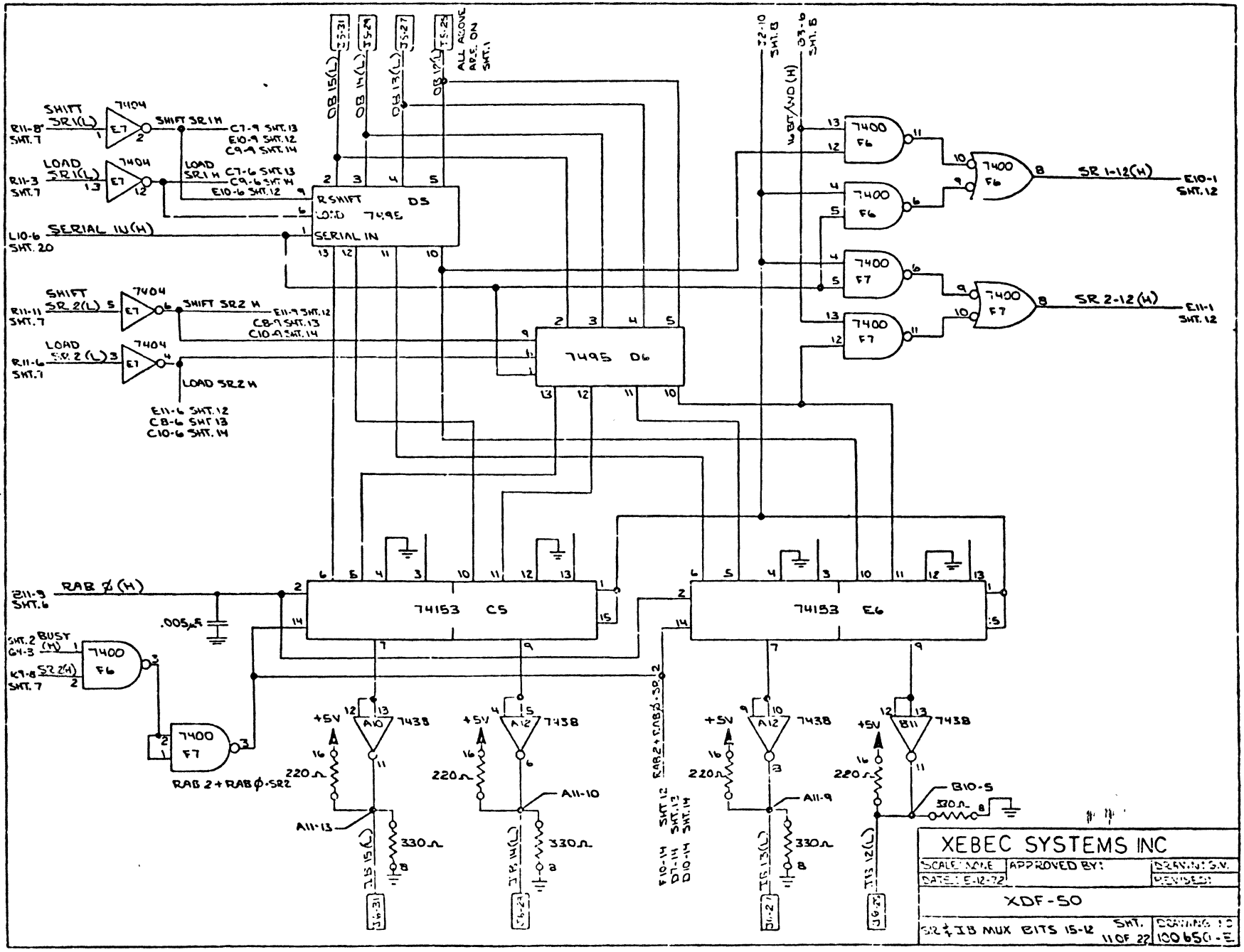


FIGURE #.7
Status Gating Logic
4-10

4.2.3.1 Loading the Command Register

The timing sequence for loading the command register is as shown in Figure 4.6. The timing sequence is an example of "3403_8" being loaded into the command register. Any time the command register is loaded with anything other than 000, the Disk Formatter unit goes BUSY, and the BUSY flip flop is set. For further discussion of BUSY, see paragraph 4.5.

4.2.4 Status Register

The status register is a 12 bit register. The status bits are placed on the CPIB lines any time that the formatter is not busy and RAB 0 = 1.

See figure 4-7 for logic of status gating. Detail descriptions of each of the status register bits is found in Section 3.3.3 and Section 4.4.

4.2.5 Shift Registers

A typical section of the shift register is shown in Figure 4.8. Each group of the SN7495 registers are four bit right shift registers that are loaded in parallel and shifted serially. They are not loaded from the mini-computer executed programs, but normally from the DMA channel only.

The shift registers have a RAB address of 000, and this address with an OSP causes the data on the CPOB lines to be loaded into the shift registers. The loaded shift registers are shifted serially and are used to provide the write data for the disk memory unit.

To determine which shift register is to be loaded in parallel and which shift register is to be shifted serially, the control logic steers the data by use of steering flip flop (K9 - Pin 8 & 9). See Figure 4.9. Initially, the control logic is set to select shift register 2 to be loaded in parallel and shift register 1 for data to be shifted serially. The timing of the shift registers and the steering logic is shown in Figure 4.10.

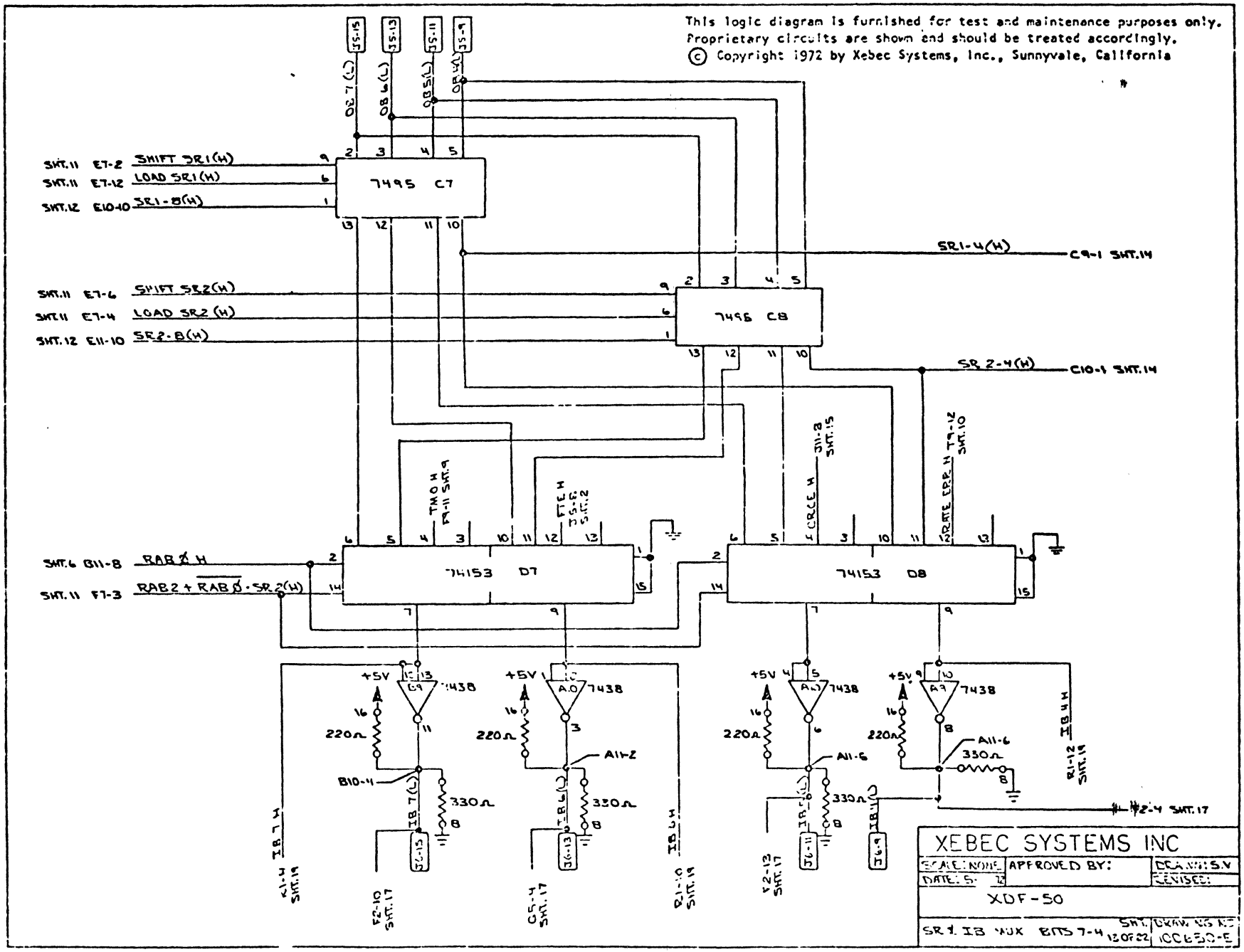


FIGURE 4.8
Shift Register
4-12

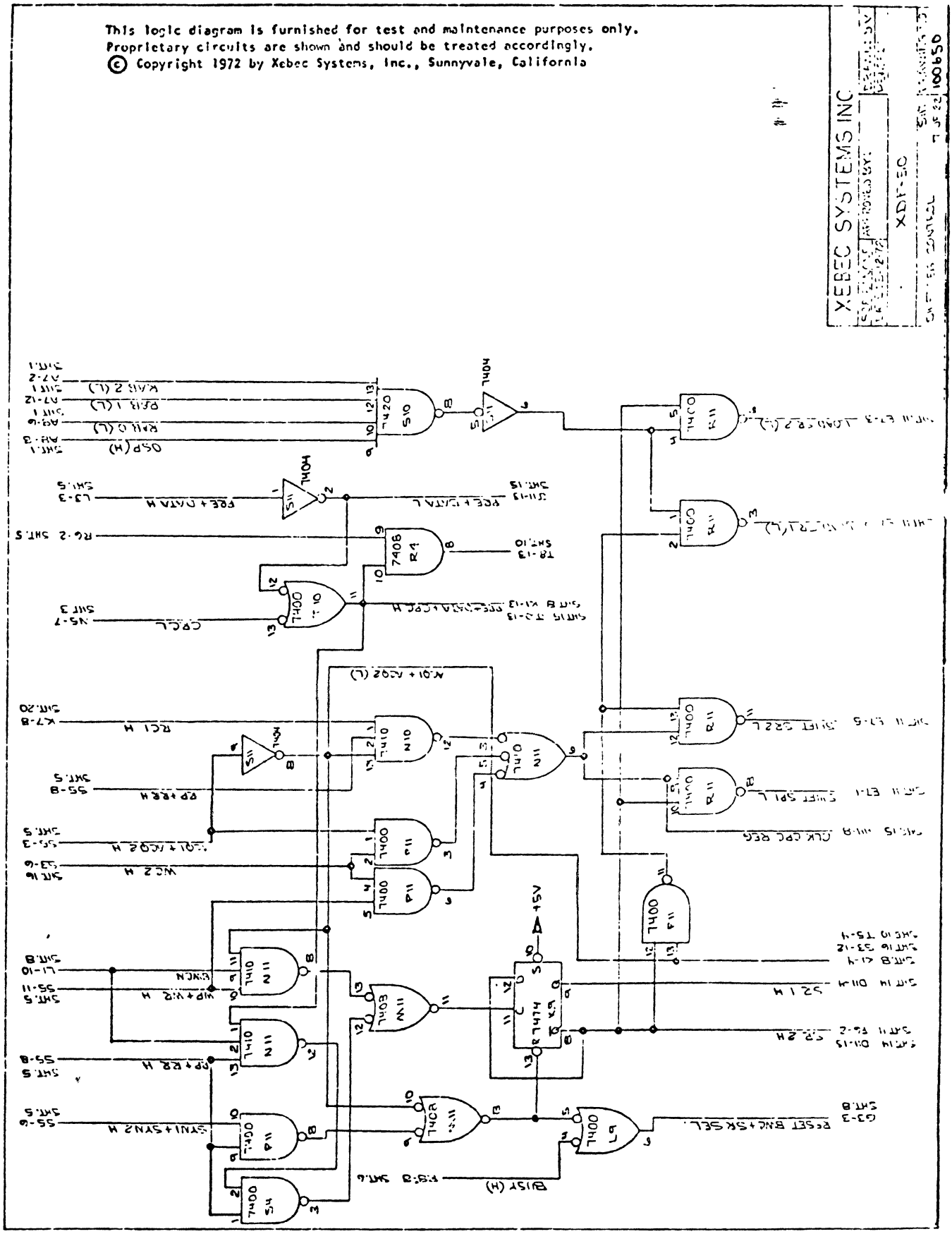


FIGURE 4.9
Steering Flip Flop
4-13

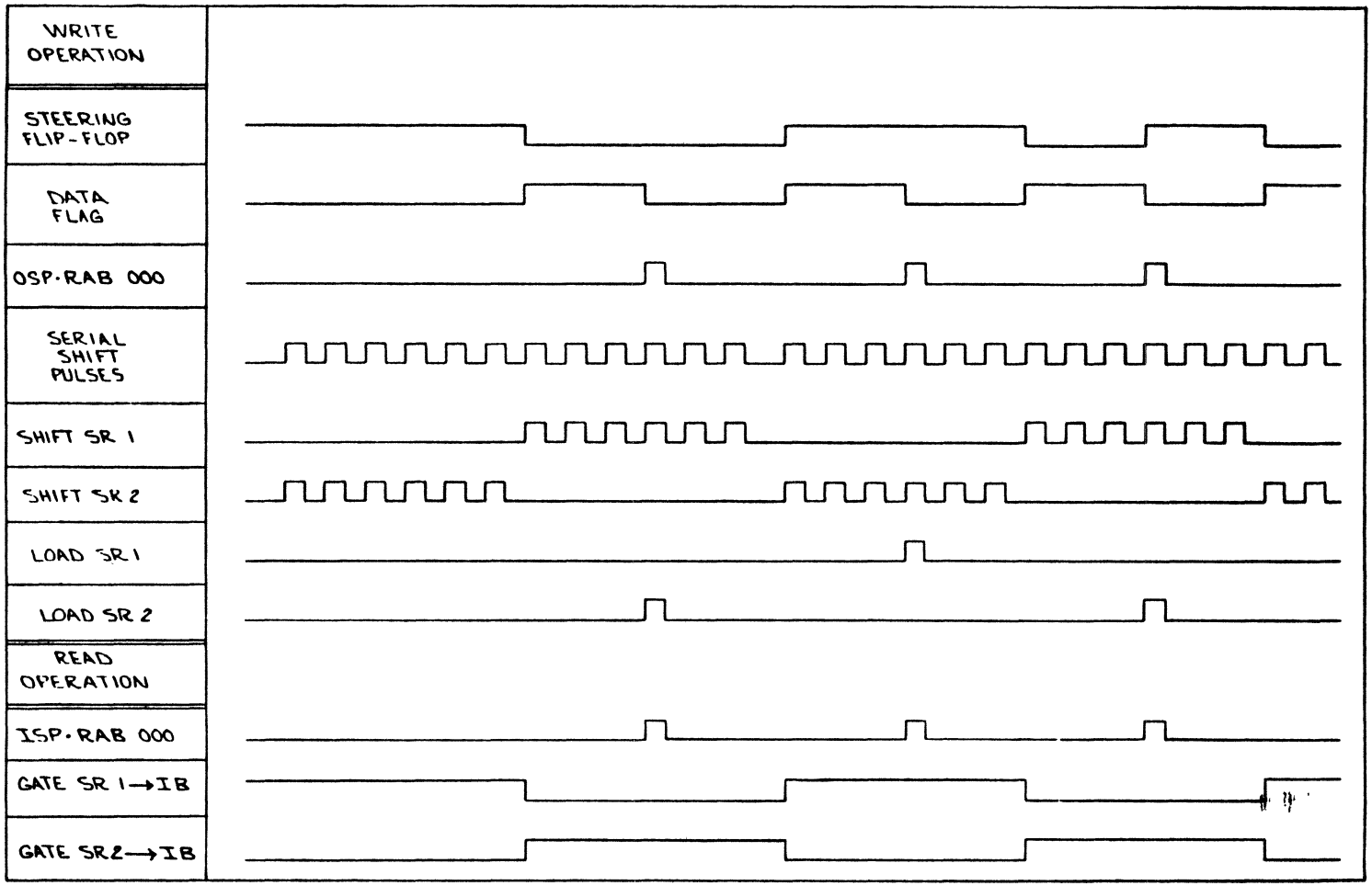


FIGURE 4.10

TIMING DIAGRAM FOR SHIFT REGISTER

4.3 CONTROL LOGIC

4.3.1 State Counter

The state counter is shown in Figure 4.11. It is composed of a SN74193 simultaneous advance counter and a SN7442 decoder. The output from the SN74193 counter is decoded by the SN7442 decoder into 1 of a possible 8 states.

The initial state as shown by Figure 4.11 is IDLE. The first signal input to the state counter is a Clean Sector Compare (H) signal which resets the state counter. This forces the counter to decode the output as 10_8 which is output on pin 10 (Idle State).

As soon as the Disk Formatter finds a sector compare the operation begins. The input on pin 12 of the SN7442 decoder is low so the counter is not advanced. This is decoded as "000" by the decoder, and a "0" on N5-12 forces the decoder to output the signal on N5-1 which is the ACQ-1 state.

Subsequent advances of the state counter are caused by an advance state counter pulse which comes from the SN 7451 AOI gate shown in Figure 4.12. This increment pulse causes the state counter to advance through its states which are decoded as ACQ1, SYN1, PRE, ACQ2, SYN2, DATA, CRC. The CRC state is the last state entered by the state counter. This state is terminated by resetting the BUSY flip flop. Resetting the BUSY flip flop also resets the Clean Sector Compare flip flop, which is decoded as the Idle State, terminating the Disk Formatter operation. See the Timing Diagram on Figure 4.13. The logic equation for the signals which advance the State Counter is shown in Table 4.1.

4.3.2 Sector Length Counter

The sector length counter is as shown on Figure 4.14. Initially, the sector length counter is in the zero state (SECL 0), it goes up through SECL 1, SECL 2, SECL 3, etc. up to SECL 7. When it reaches that point, the control logic sets the L3 flip flop. The setting of that flip flop prevents any further decodes from the SN 7442 decoder until the L3 flip flop is reset by SLC=N, indicating that the counter has counted one full sector. Sector length counter=N and SECL 0, SECL 0, SECL 1, SECL 2, and SECL 3 is used to decode into N+0, N+1, N+2, N+3.

The logic equations for the sector length counter as shown in Table 4.2, and the Timing Diagram is as shown in Figure 4.15.

This logic diagram is furnished for test and maintenance purposes only.
Proprietary circuits are shown and should be treated accordingly.

FIGURE 4.11
State Counter

FIGURE 4.12
Advance State Counter Pulse
4-17

TABLE 4.1
LOGIC EQUATIONS FOR ADVANCING STATE COUNTER

MODE OF OPERATION	LOGIC EQUATION
READ PREAMBLE (RP)	ACQ1•40μ•WC2+SYN1•SYNC•RC2 +PRE•SECL 3•BWCN•RC2
READ RECORD (RR)	ACQ2•60μ•WC2+SYN2•SYNC•RC2 +DATA•SECL(N)•BWCN•RC2
CRC MODE TO IDLE (READ TERMINATION) RESET BUSY (NORMAL TERMINATION) CRC BACK TO IDLE MODE	RR•(SECL N+3)•BWCN
WRITE PREAMBLE (WP)	ACQ1•100μ•WC2+SYN1•BWCN•WC2 +PRE•SECL 2•BWCN•WC2
WRITE RECORD (WR)	ACQ2•100μ•WC2+SYN2•BWCN•WC2 +DATA•SECL (N)•BWCN•WC2
CRC MODE TO IDLE (WRITE TERMINATION) RESET BUSY (NORMAL TERMINATION)	WR•(SECL N+4)•BWCN

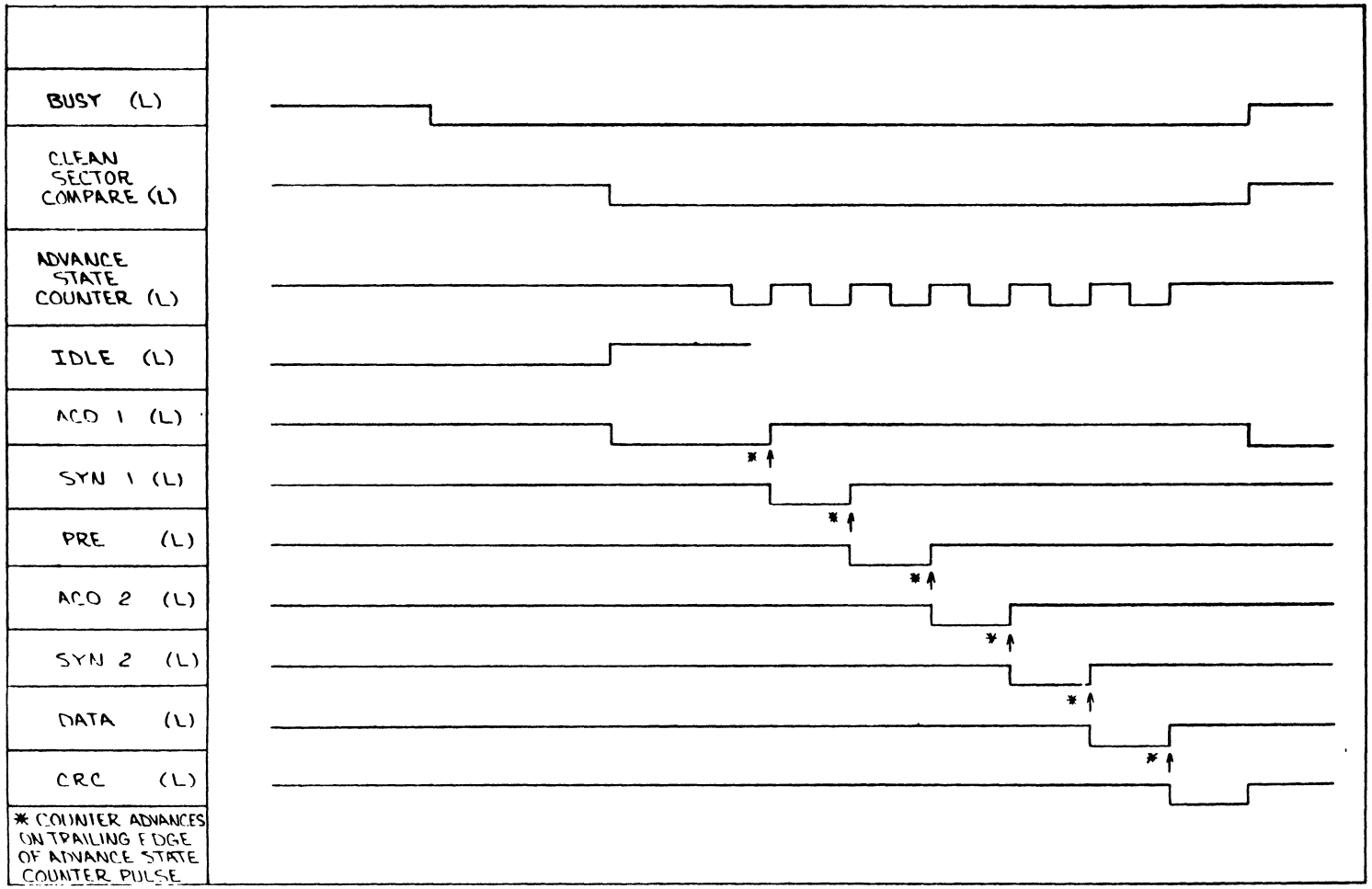


FIGURE 4.13

TIMING DIAGRAM FOR STATE COUNTER

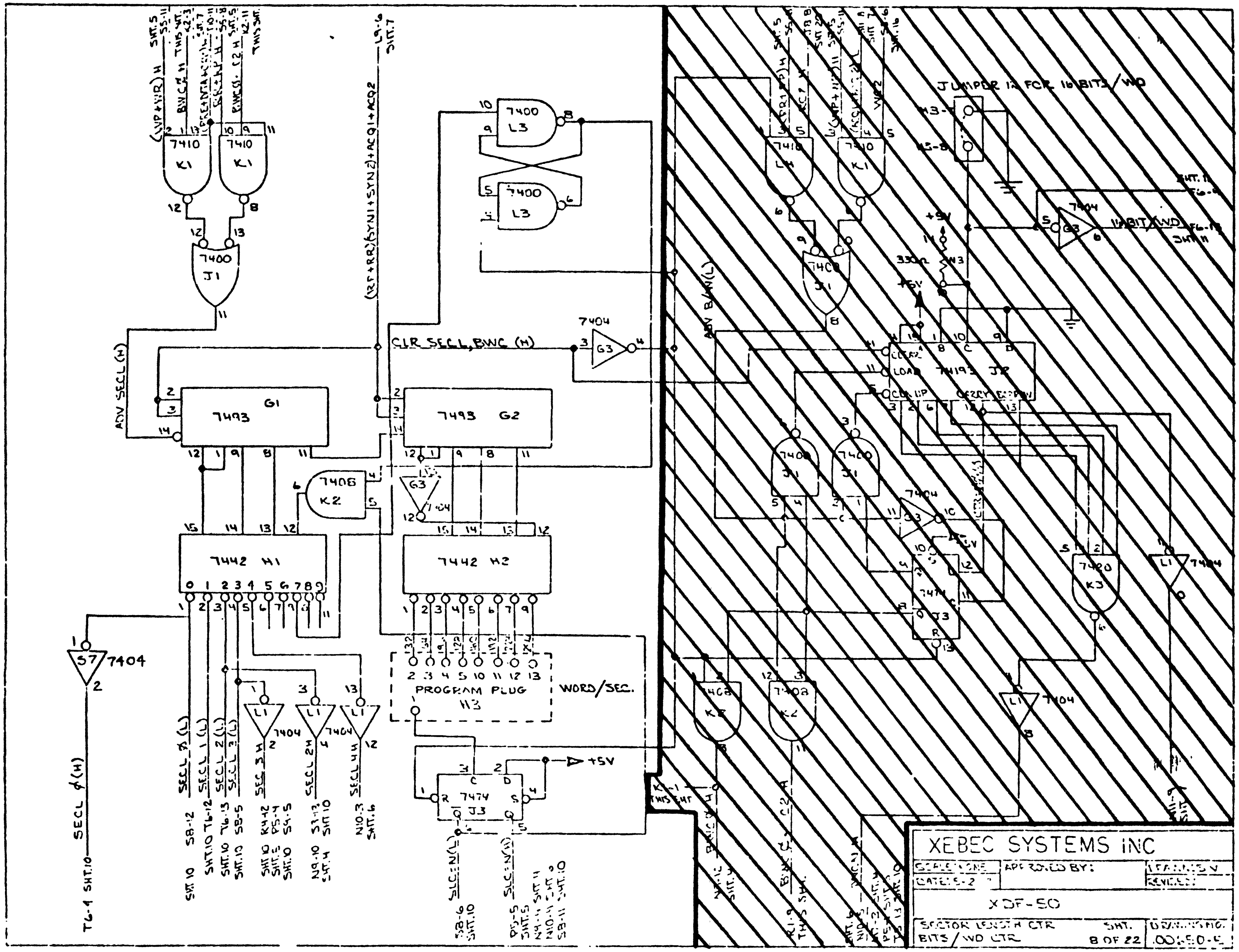


FIGURE 4.14
Sector Length Counter
4-20

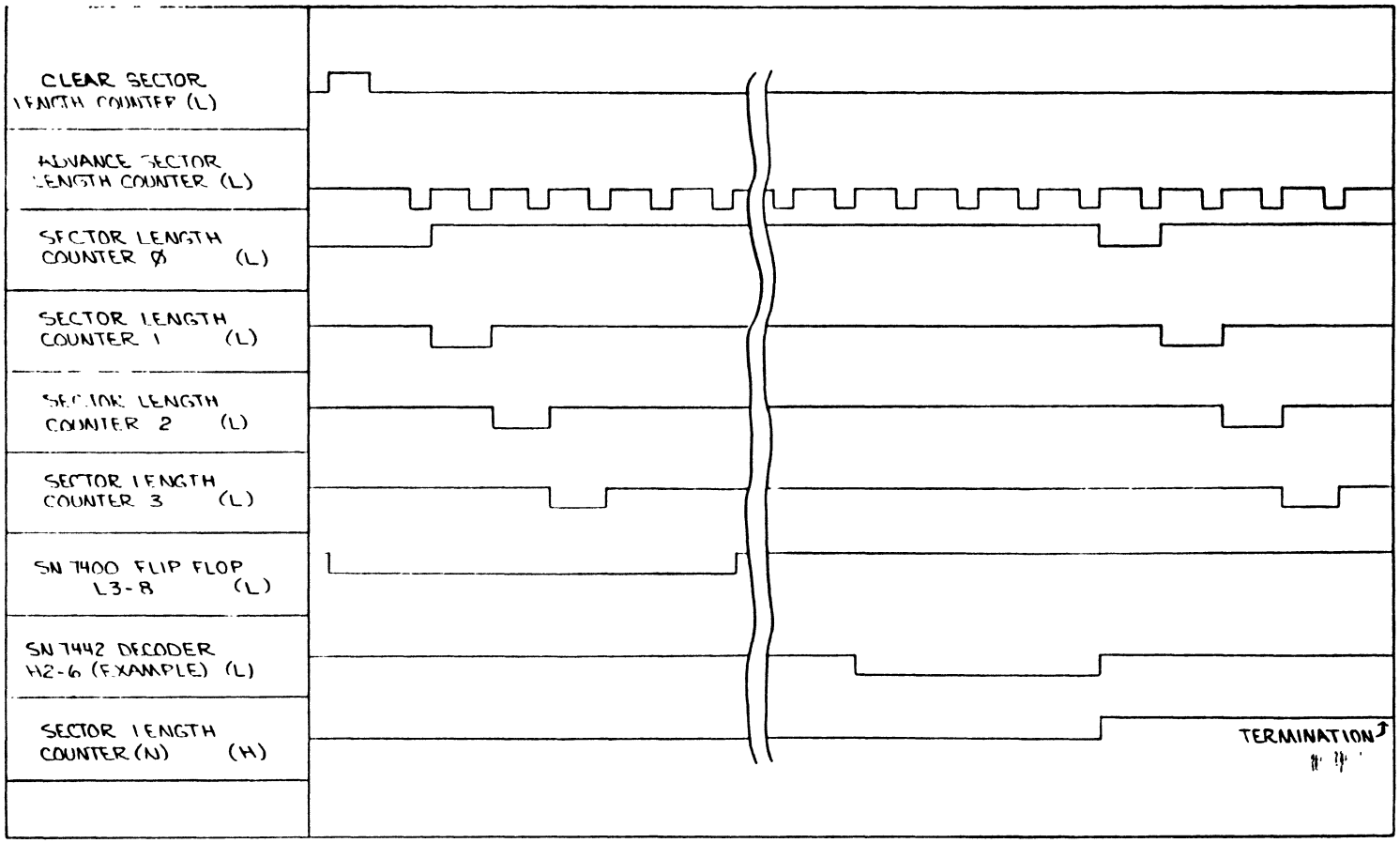


FIGURE 4.15

TIMING DIAGRAM FOR SECTOR LENGTH COUNTER

TABLE 4.2
LOGIC EQUATIONS FOR SECTOR LENGTH COUNTER

OPERATION MODE	LOGIC EQUATION TO INCREMENT COUNTER
READ PREAMBLE (RP)	PRE•BWC 0•RC2
READ RECORD (RR)	DATA•BWC 0•RC2 + CRC•BWC 0•RC2
WRITE PREAMBLE (WP)	PRE•BWC 0
WRITE RECORD (WR)	DATA•BWC 0 + CRC•BWC 0

RESET SECTOR LENGTH COUNTER

RP (ACQ1 + SNY1) + WP (ACQ1)
RR (ACQ2 + SYN2) + WR (ACQ2)

4.3.3 Sector Counter

The sector counters are shown in Figure 4.16. Sector pulses and index pulses come in from the disk, the index pulse once/revolution and sector pulse once/sector. The SN7474 E2 flip flop is used to determine when to reset the counter. If it gets set by the index pulse, then on the next sector pulse the counter will get reset.

When E2 is set, a pulse is generated on D2-3 which resets E2-13, an extension of the sector counter, to make the sector counter a 5 bit counter. Internally to the SN7493 sector counter on pins 2 and 3, an equivalent circuit is used. Pins 2 and 3 are inputs that will reset the counter when they are both high (H).

The sector pulse (E3-14) is inhibited when E2-5 is not set high. Therefore, no advance pulses enter the counter when it is being reset by index pulses. The timing diagram is shown in Figure 4.17.

The above describes the operation of the Sector Counter for the removable disk. An identical counter for the fixed disk is shown on the right hand side of Figure 4-24. The operation of this counter is the same. It should be noted, however, that entirely separate sets of pulses are used to drive the other sector counter, and the relationship of the value of the counters depends upon the orientation of the index mask on the fixed disk to the index mask on the removable disk.

4.3.4 Bits/Word Counter

The bits/word counter is shown in Figure 4.18. The bits/word counter can be configured to divide by 12 bits or 16 bits depending upon the jumper between H3-7 to H3-8.

When a 12 bits/word mini-computer is attached to the disk formatter, a "load pulse" is generated after count "0" to load a value of five into the counter.

When the counter reaches a value of 15, (BWCN), it resets itself automatically back to zero (BWC0) since it is a four bit counter. After count zero it jumps back to 5 as before. The net result is that 12 counter states are used.

In the case of a 16 bits/word mini-computer, the disk formatter generates a "load pulse" after count zero to load a value of "1" into the counter. The counter counts up to 15 (BWCN), and on the next count back to zero (BWC0) again. All 16 states of the counter are used.

The Timing Diagram for the bits/word counter is shown in Figure 4.19, and the logic equations for the operational modes are shown in Table 4.3.

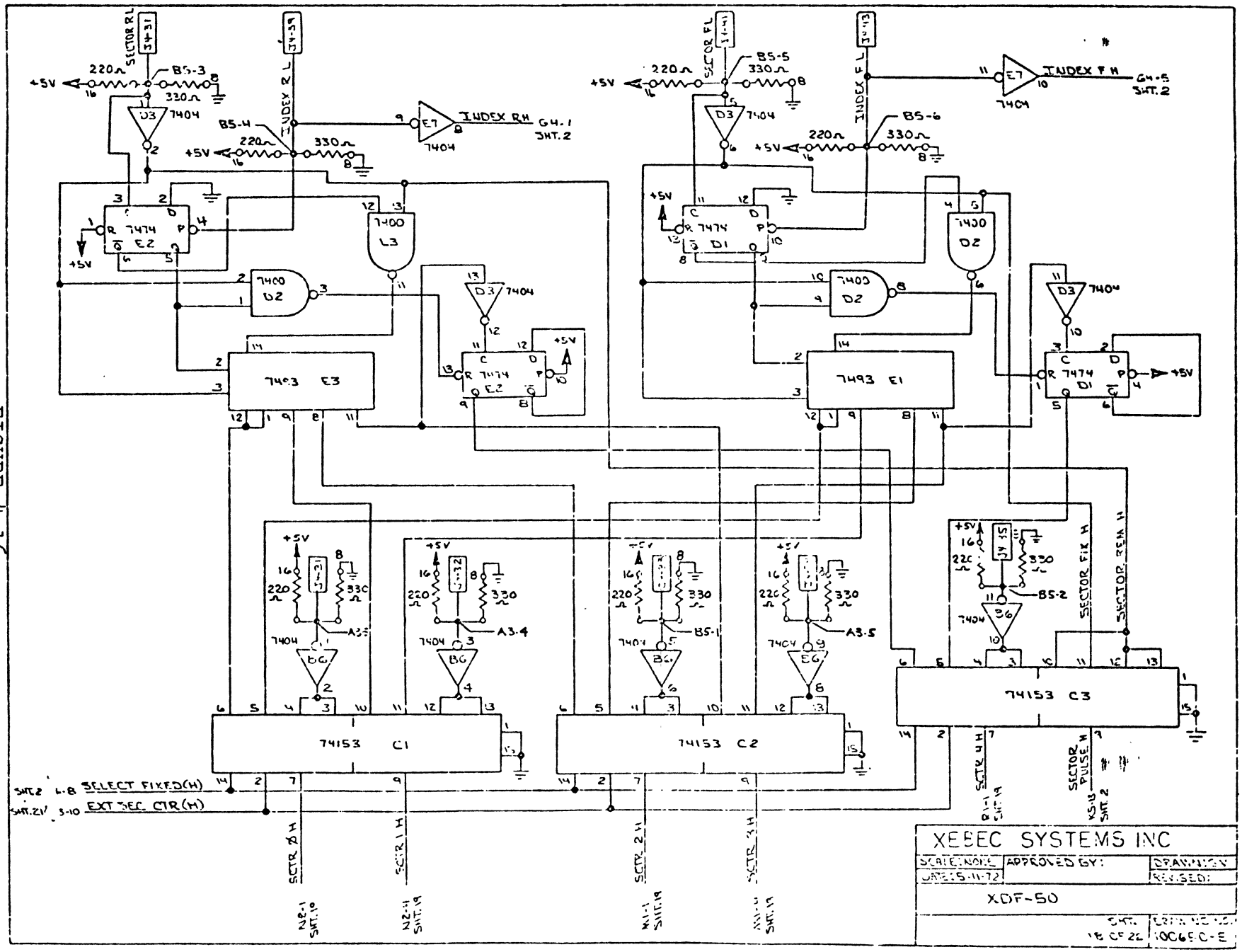


FIGURE 4.16
Sector Counter

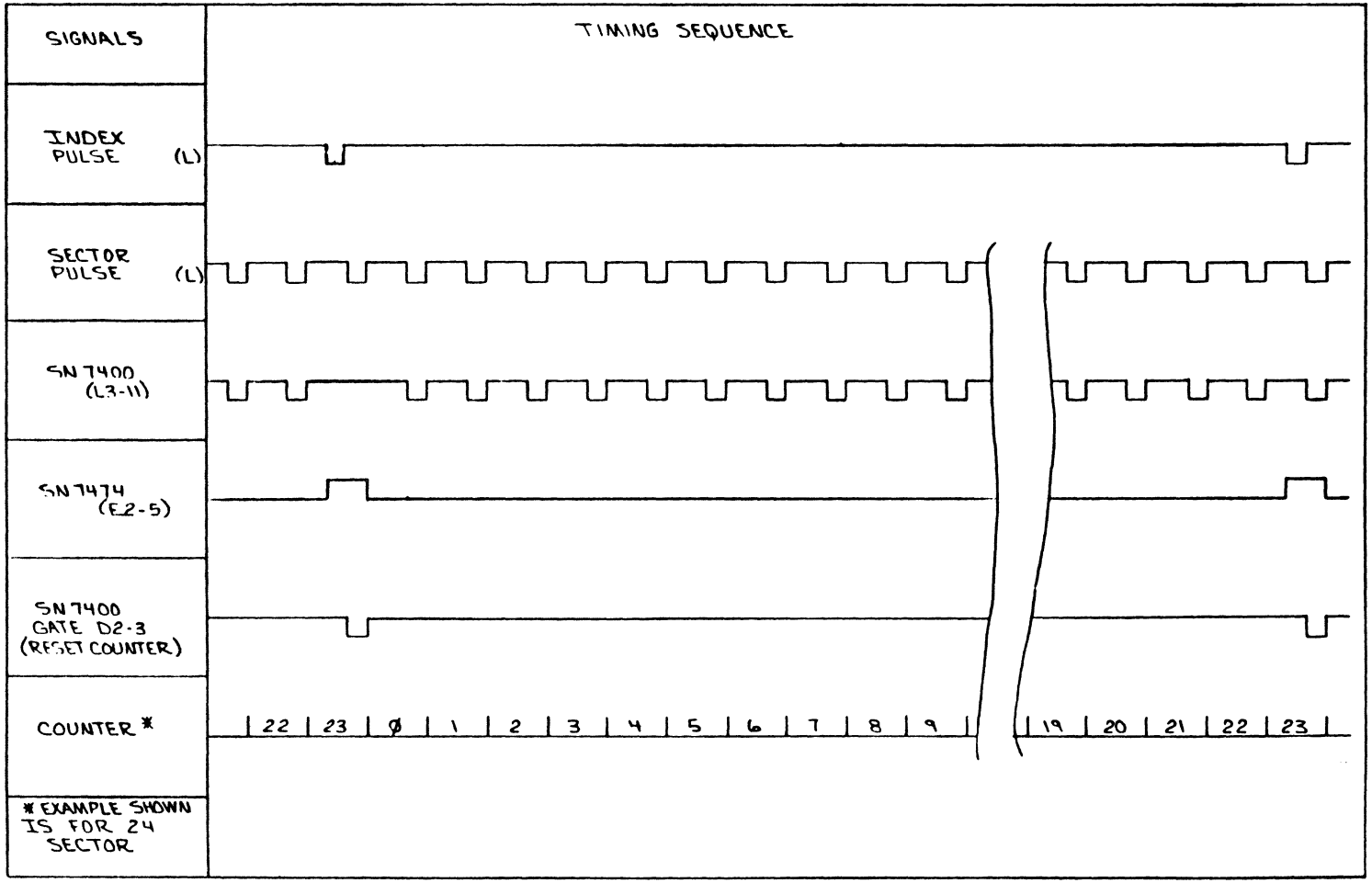


FIGURE 4.17

TIMING DIAGRAM FOR SECTOR COUNTER

FIGURE 4.18
Bits/Word Counter

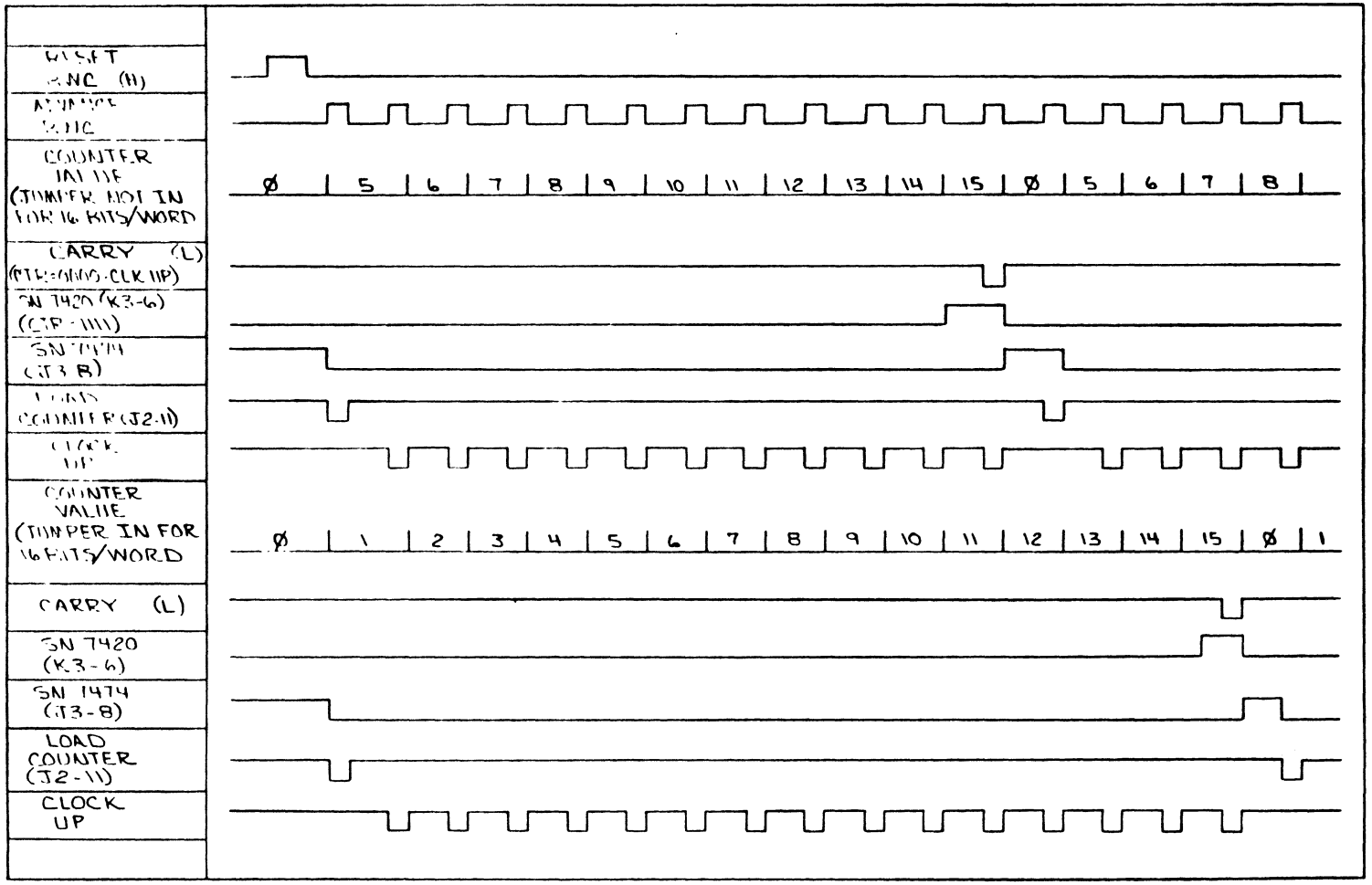


FIGURE 4.19

TIMING DIAGRAM FOR BITS/WORD COUNTER

TABLE 4.3
LOGIC EQUATION FOR BITS/WORD COUNTER

FUNCTION	OPERATION MODE	LOGIC EQUATION
RESET BITS/WORD COUNTER	READ PREAMBLE (RP)	(SYN1 + ACQ1)
		+
	WRITE PREAMBLE (WP)	(ACQ1)
		+
	READ RECORD (RR)	(SYN2 + ACQ2)
		+
	WRITE RECORD (WR)	(ACQ2)
ADVANCE BITS/WORD COUNTER	READ PREAMBLE (RP)	$\overline{(SYN1 + ACQ1)}$ RC2
	WRITE PREAMBLE (WP)	$\overline{(ACQ1\ WC2)}$
	READ RECORD (RR)	$\overline{(SYN2 + ACQ2)}$ RC2
	WRITE RECORD (WR)	$\overline{(ACQ2\ WC2)}$

4.3.5 Comparator Circuits

There are three (3) comparator circuits in the disk formatter. These are:

1) Cylinder Compare
2) Sector Compare
3) Preamble Sector Compare

These are briefly discussed in the balance of this section.

4.3.5.1 Cylinder Compare

Cylinder Compare circuit is shown in Figure 4.20. As can be seen by this girue, it is composed of SN7486 exclusive /OR gates feeding into an 8-input NAND flip flop. The output of this compare circuit is used to determine if the cylinder register matches the first preamble word (which identifies the cylinder address currently read).

4.3.5.2 Sector Compare

The sector compare flip flop is shown in Figure 4.21. When the command register is loaded, the BUSY flip flop is set. The disk formatter waits until SEEK is complete and then waits until the sector counter value is equal to the sector value loaded into the command register. This equality along with SEEK complete enables the sector pulse. The sector pulse is delayed approximately 2.0 microseconds to allow the counters to stabilize before comparison.

When these events have occurred the clean sector compare flip flop is set. This indicates the beginning of an operation in the addressed sector. The timing of these events is shown in Figure 4.22.

The comparison of the value in the sector register to the current value of the sector counter is shown in Figure 4.23. It is a series of SN7486 exlusive/OR gates whose output P2-13, is used to determine whether the sector counter value equals the command register sector value.

FIGURE 4.20
Preamble Cly Compare

FIGURE 4.21
Clean Sector Compare

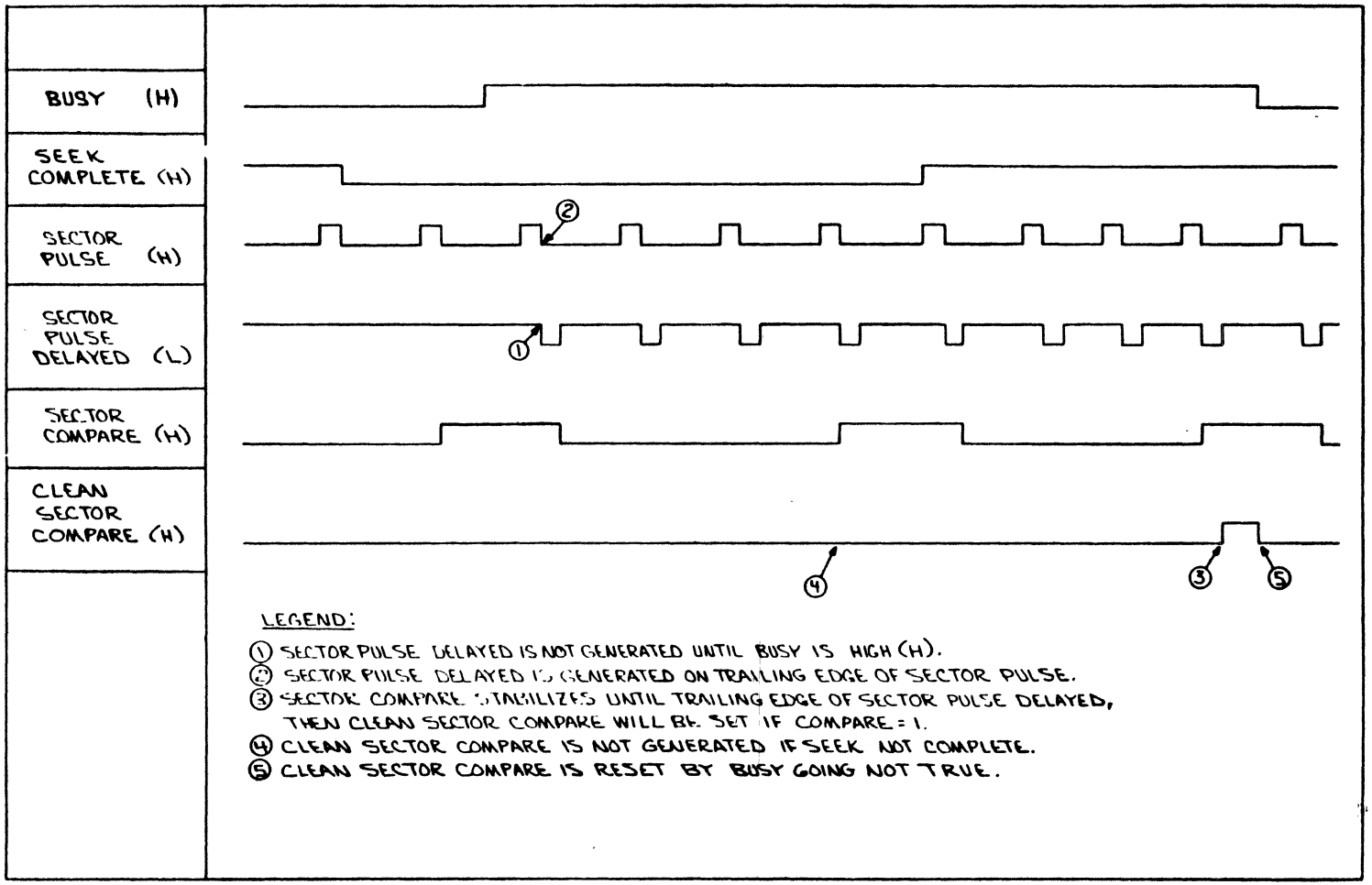
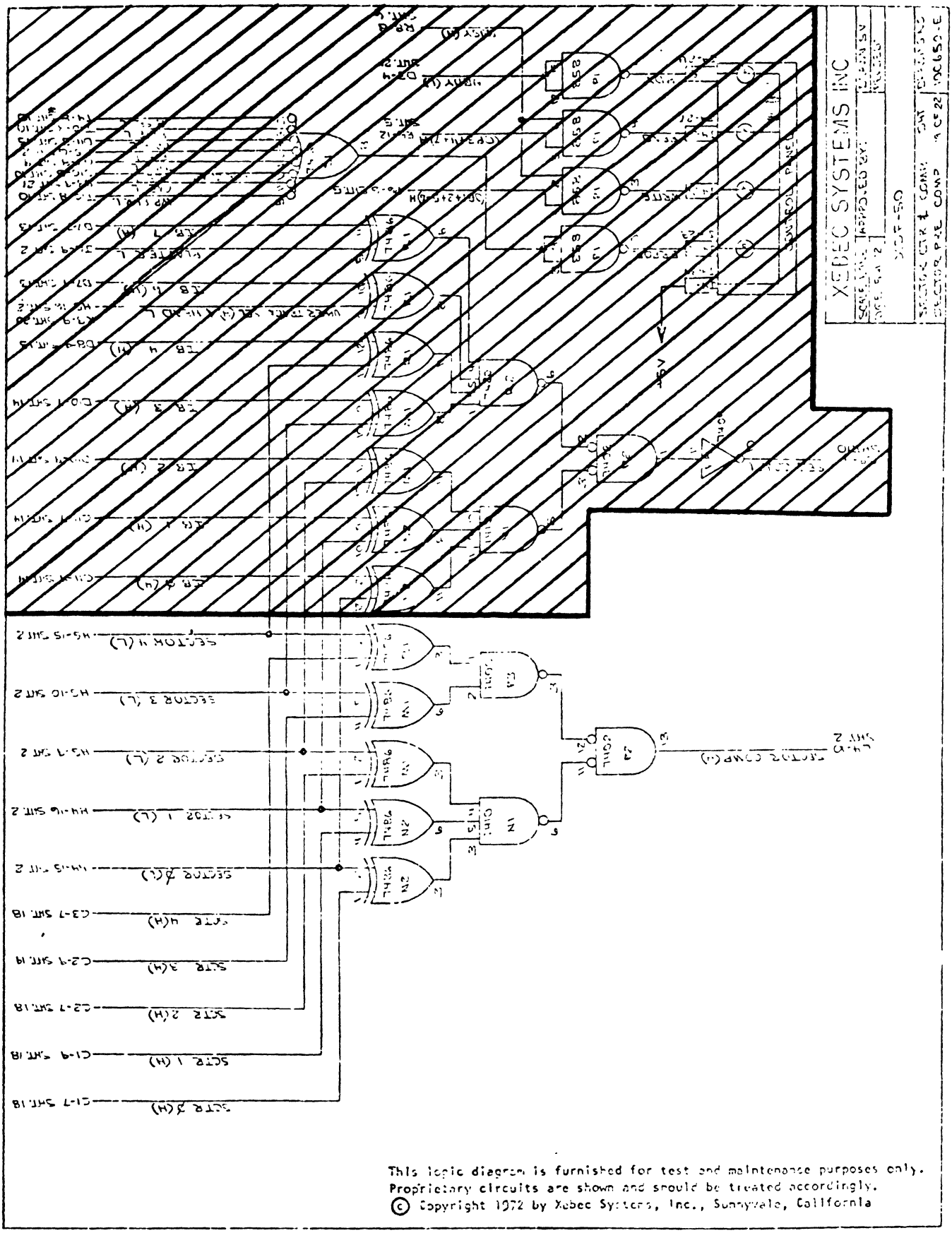


FIGURE 4.22

TIMING DIAGRAM FOR SECTOR COMPARE



This logic diagram is furnished for test and maintenance purposes only.
Proprietary circuits are shown and should be treated accordingly.

FIGURE 4.23
Sector Compare

4.3.5.3 Preamble Sector Compare

The preamble sector compare circuit is shown in Figure 4.24. It is composed of a series of SN7486 Exclusive /OR gates. The output of this compare circuit is used to determine if the sector register matches the 2nd word of the preamble (used to identify the sector currently being read.)

4.3.6 Timing Circuits

The timing circuit for the disk formatter is shown in Figure 4.25. This circuit is composed of two SN7493 4-bit binary counters, one SN7474 flip flop, and a series of SN7408 gates. The timing circuit shown utilizes jumpers between pins 6 and 8 for 2200 BPI density.

The outputs of the timing circuit are 40 microseconds, 60 microseconds, and 100 microseconds from the zero state of the counter. The logic equations for resetting and advancing the timer are as follows:

RESET TIMER $\overline{ACQ1 + ACQ2}$

ADVANCE TIMER WC1, $(ACQ1 + ACQ2)$

(Implied by reset, not actually in the logic for advancing timer)

4.3.7 Write Clock and Double Frequency Write Data Generation

The write clock circuit is shown in Figure 4.26. It is composed of two SN7474 counters and SN7408 decoders. These generate the write clocks used to create double frequency write data.

The write oscillator is the basic timing source and runs at one of the crystal controlled frequency values shown on Figure 4.26. The R3 inverter shapes the signal to a TTL compatible pulse

The TTL compatible signal is used to drive the SN7474 counter which is then decoded by the SN7408 gate. Two states of the counter are decoded as write clock 1 and write clock 2.

The disk formatter has thus generated a two (2) phase clock which are a quarter cell in duration and are spaced 1/2 cell apart. See Timing Diagram on Figure 4.27.

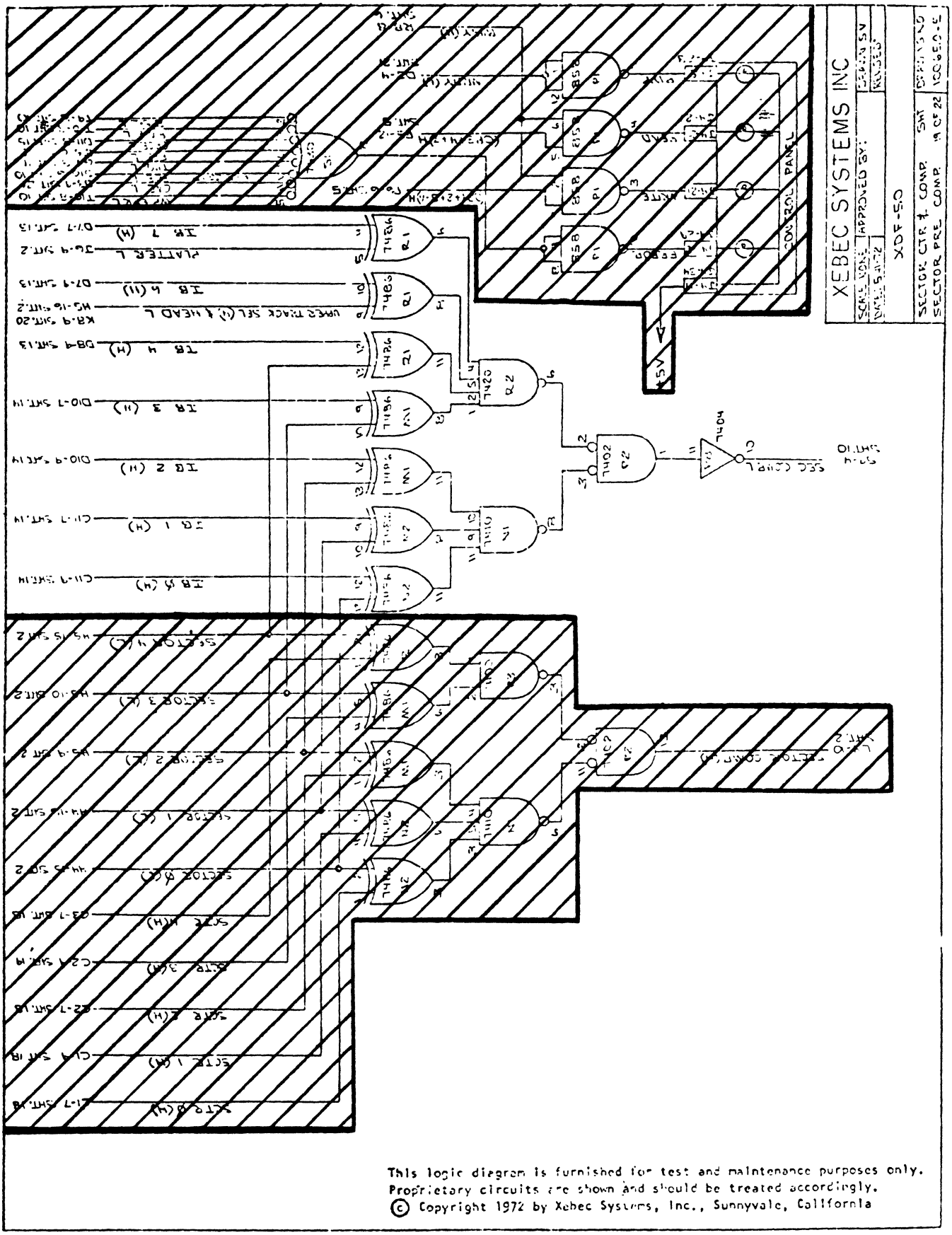


FIGURE 4.24
Preamble Sector Compare

This logic diagram is furnished for test and maintenance purposes only.
Proprietary circuits are shown and should be treated accordingly.

FIGURE 4.25
Timing Counter

The write clocks that are generated are used to create a double frequency (DF) encoded signal from the NRZ wirte data that is received from the shift registers. The timing for the DF signal is shown in Figure 4.27.

4.3.8 Read Gate

The read gate circuit is as shown in Figure 4.28. When a read operation is selected, the read gate circuit is enabled. This enables data from the disk memory unit to be read into the disk formatter.

The read gate flip flop is controlled as follows:

A) Set read gate = (RP·40 μ +RR·60 μ)

B) Reset read gate = OSP·RAB5 + PRE·ADV STATE CTR + MCLR

4.3.9 Read Clock Circuit

The read clock circuit is shown in Figure 4.29. A two phase set of internal read clocks is generated from the incoming read clock from the disk (Read CLKI).

Read Clock 1:	SHIFT-SHIFT REGISTERS
Read Clock 2:	CLOCK SECTOR LENGTH COUNTER CLOCK BITS/WORD COUNTER CLOCK STATE COUNTER

Read clock 1 and read clock 2 are pulses 50-100 NS wide, separated by a delay of 70 to 100 NS.

SRIN is generated from the read data input RDATA 1 and forms the serial read data input to the shift registers.

4.3.10 Write Enable

The write enable circuit is shown in Figure 4.30. The write enable flip flop is set when the clean sector compare signal pulse is enabled and write preamble operation is being performed, or when a write record operation is being performed. The write enable flip flop will remain set until 1) a write protect error is detected, or 2) until BUSY flip flop goes off indicating data transfer has been completed.

When the disk formatter detects a write protect error, the write enable flip flop is reset immediately. With a set and reset condition on the flip flop simultaneously, the disk formatter logic is designed so that signals enabling the reset side of any flip flop have first priority. The write enable circuit would be turned off, and an error bit would be returned to the status register.

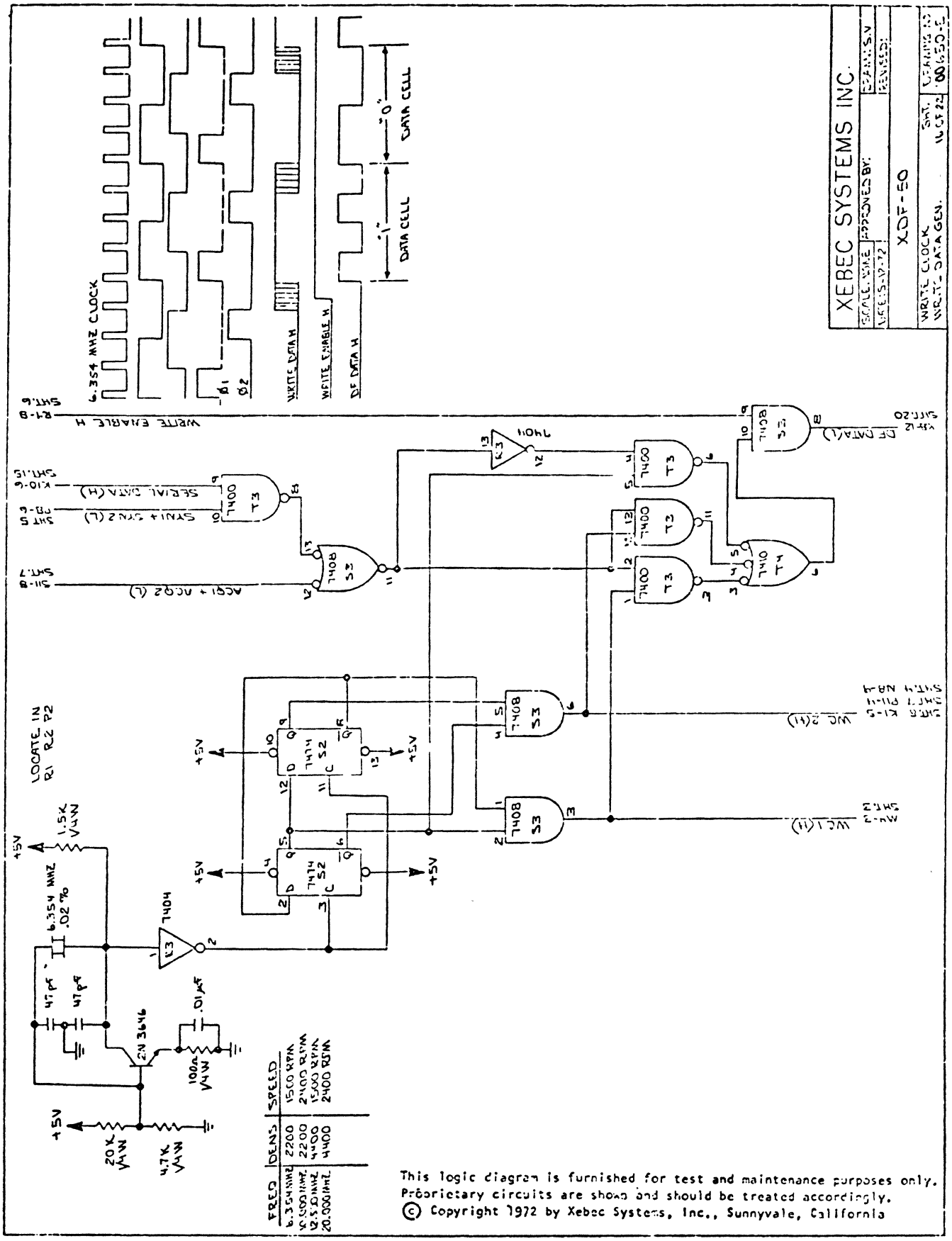


FIGURE 4.26
Write Clocks
4-38

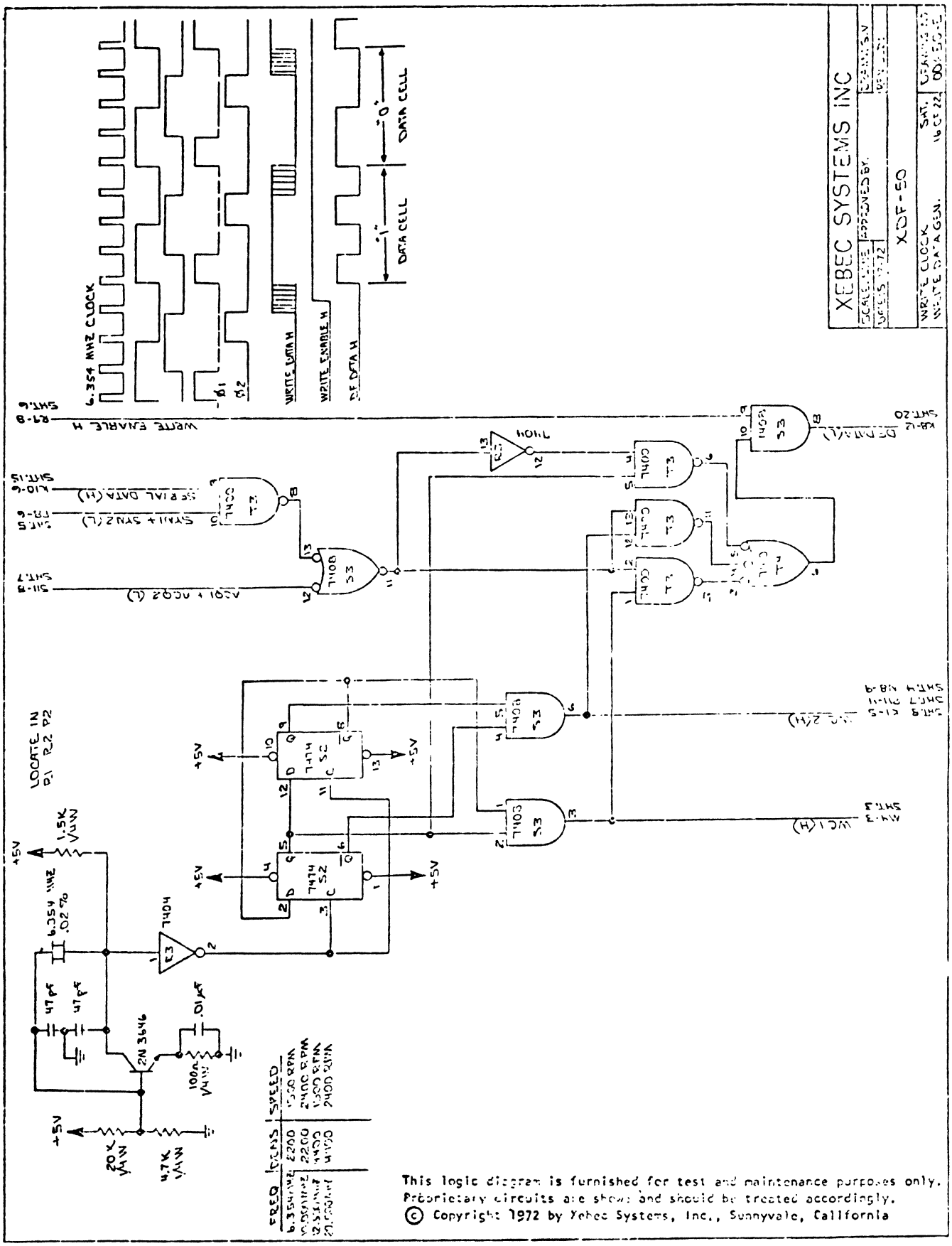


FIGURE 4.27
Write Clock/Data Timing

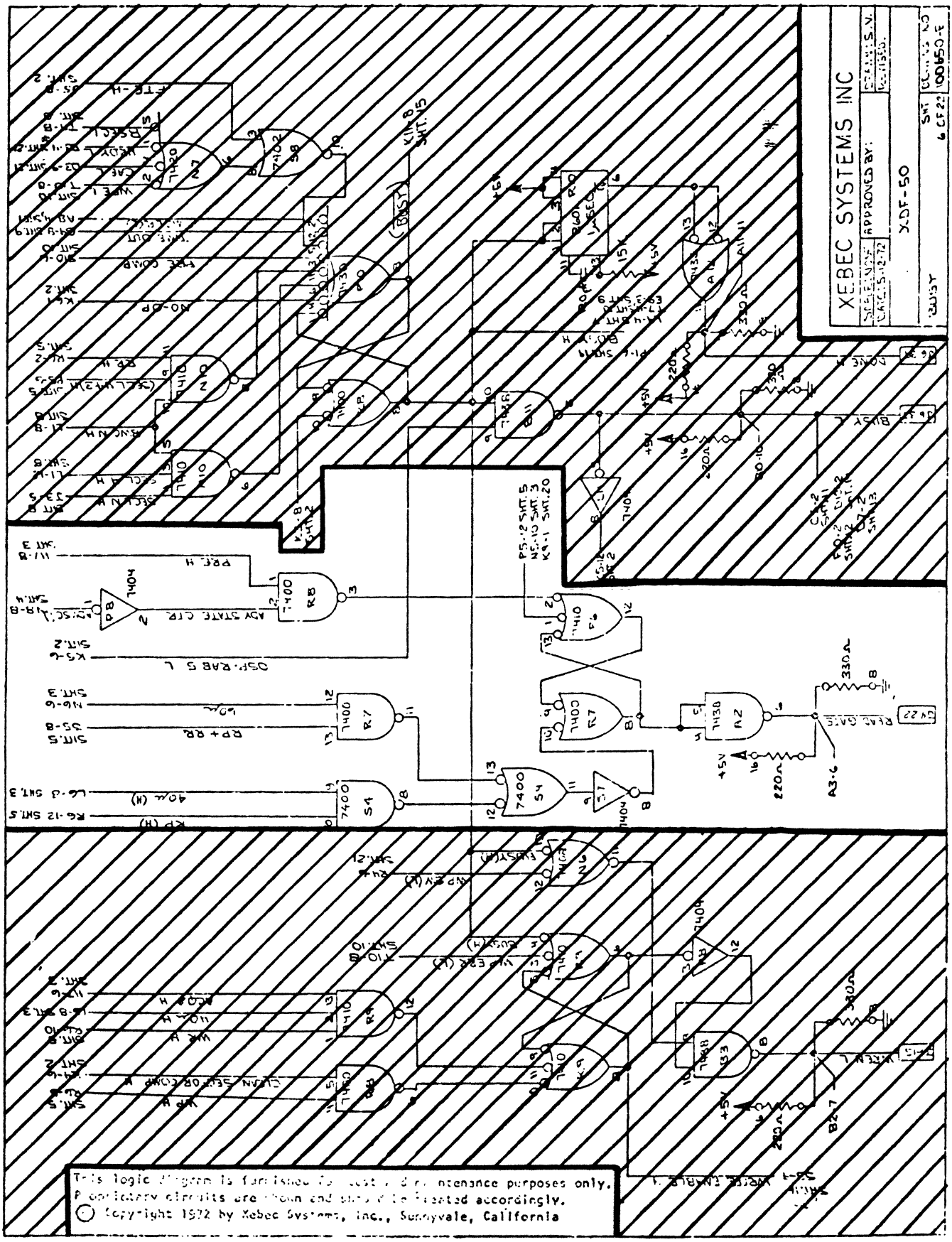


FIGURE 4.28
Read Gate Circuit
4-40

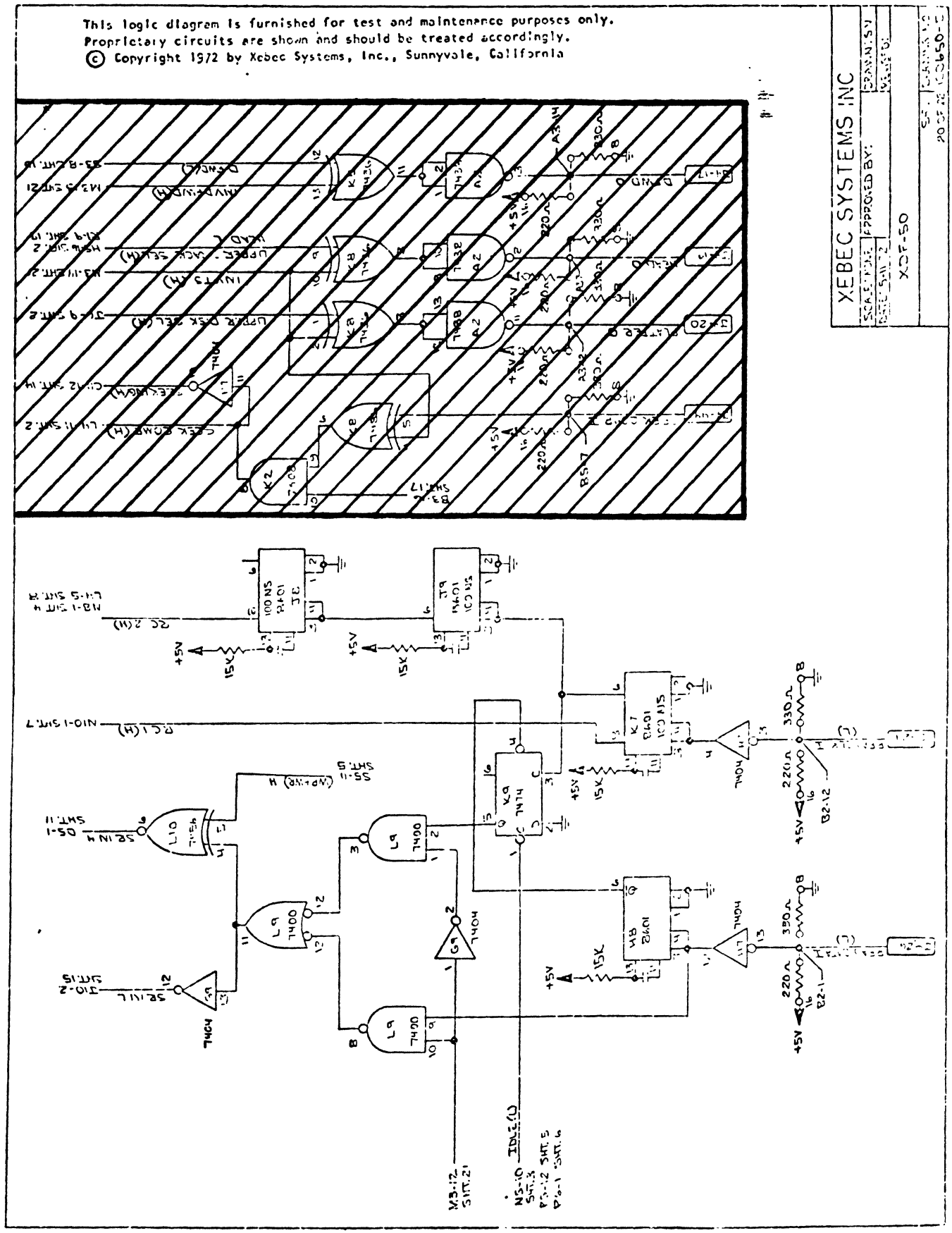


FIGURE 4.29
Read Clock Circuit

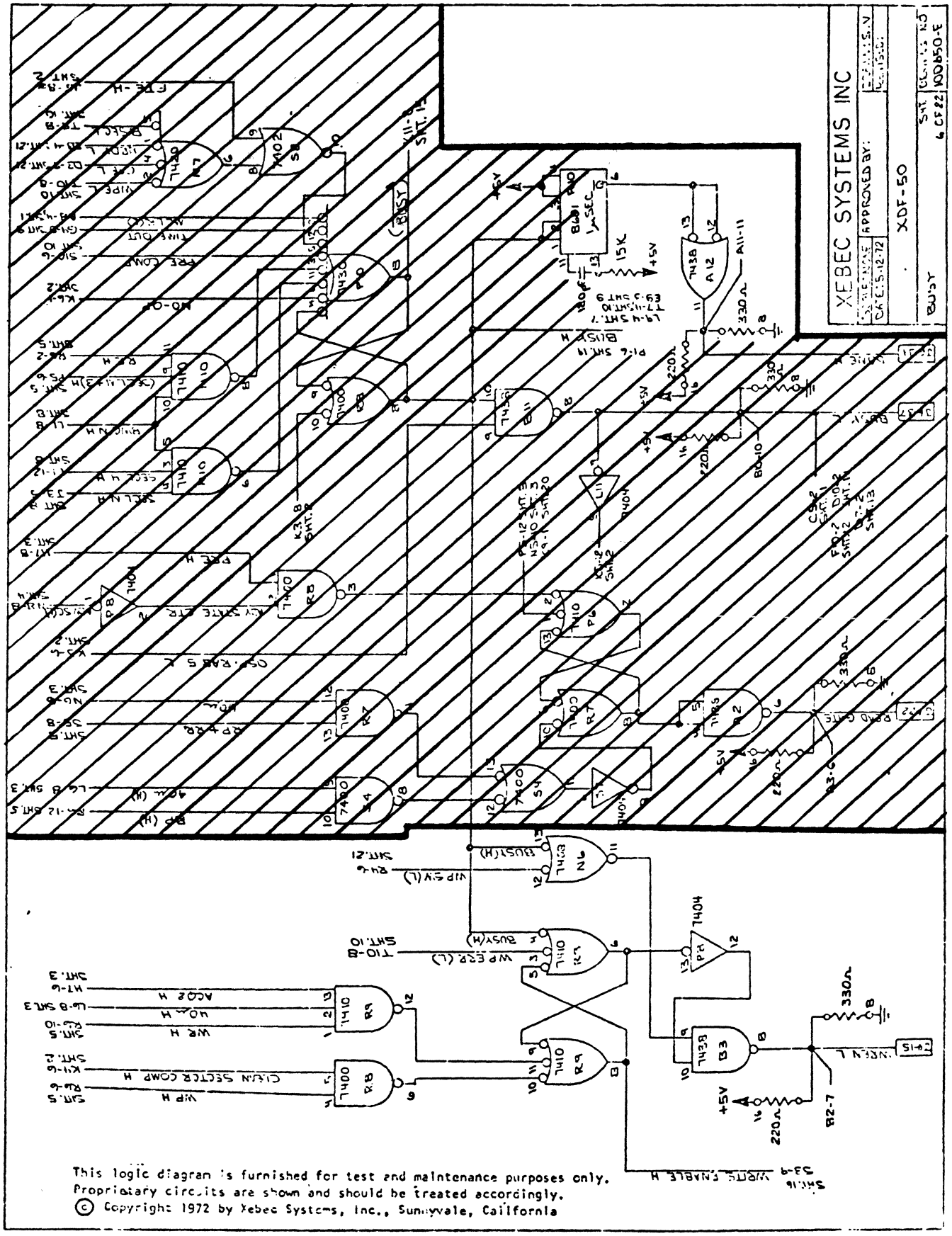


FIGURE 4.30
Write Enable
4-42

The logic equations for the write enable circuit are:

Set Write Enable FF = WP•CLEAN SECTOR COMPARE + WR• ACQ2 40 u

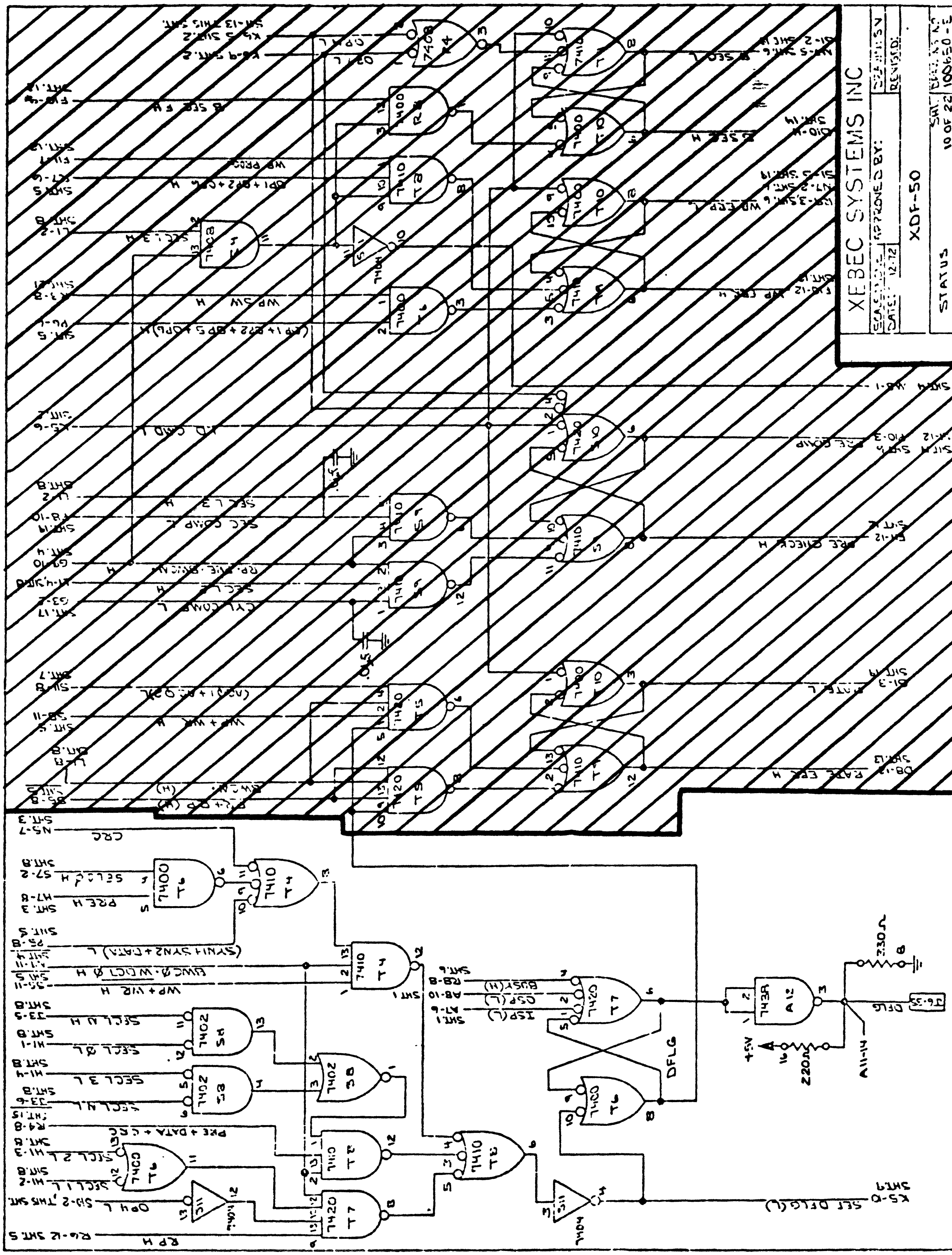
Reset Write Enable FF = WPERR + $\overline{\text{BUSY}}$

WREN = Write Enable FF•Busy•$\overline{WP_{SW}}$

4.3.11 Data Flag

The data flag circuit is shown in Figure 4.31. Data Flag (DFLG) is used to tell the mini-computer coupler that the formatter is ready to receive or send a word of data. DFLG is a flip flop controlled as follows:

Function	During Operation	Logic Equation
SET DFLG	READ PREAMBLE	$\overline{RP}$•$\overline{OP4}$•(SECL1+SECL2)•BWC0•$\overline{WDCT0}$
SET DFLG	READ RECORD	$\overline{RR}$•$\overline{(SECL0+SECLN3)}$•BWC0•$\overline{WDCT0}$
SET DFLG	WRITE PREAMBLE	WP•(SYN+PRE)•BWC0•$\overline{WDCT0}$
SET DFLG	WRITE RECORD	$\overline{WR}$•$\overline{(SYNC+DATA+CRC)}$•BWC0•$\overline{WDCT0}$
RESET DFLG	ALL WRITE OPERATIONS	OSP
RESET DFLG	ALL READ OPERATIONS	ISP
RESET DFLG	ALL OPERATIONS	$\overline{\text{BUSY}}$



FIGURE, 4.31
Data Flag Circuit

4.4 STATUS BITS

The status bits are shown in Figures 4.32 and 4.33. These status bits indicate the following error conditions within the disk formatter:

A) Rate Error

B) Preamble Compare Error

C) Write Protect Error

D) Bad Sector Flag

E) Format Error

F) Time Out Error

G) Cylinder Address Error

H) Not Operational

In addition, there is also a CRC error bit input to the status register, but that error condition is discussed under the CRC Register section of this manual.

4.4.1 Rate Error

A Rate Error is generated when the disk formatter does not receive a response to a data flag within one word time. If the reset signal is not received within the specified time, the disk unit will have missed a word and an error bit will be input to the status register. A Rate Error will not terminate the operation. The logic equations are:

Set Rate Error	All Read Operations	(RP+PR)•DFLG•BWCN
	All Write Operations	$\overline{(WP+WR)}$•$\overline{(ACQ1+ACQ2)}$•DFLG•BWCN
Reset Rate Error	All Operations	OSP•RAB5 + MCLR

FIGURE 4.32
Status Flip Flop

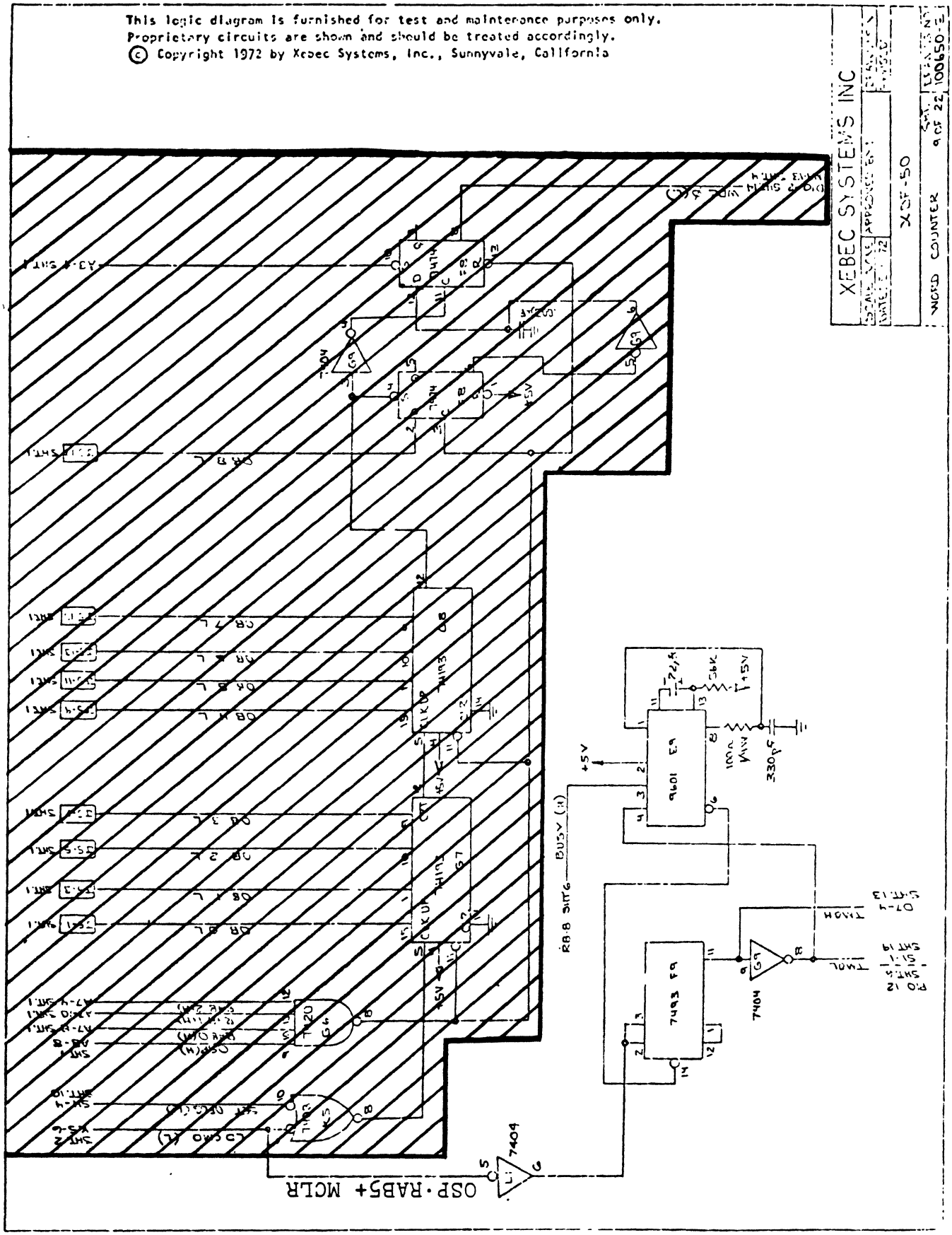


FIGURE 4.33
Timeout
4-47

4.4.2 Preamble Compare Error

A preamble compare error is generated when the cylinder or sector portion of the preamble do not compare with the values loaded into the cylinder address and command registers. This error terminates the operation. The logic equation for operation of this flip flop is as follows:

SET PREAMBLE COMPARE ERROR	$\overline{\text{CYL COMP}}$•SEC L2• RP•PRE•BWCN +
	$\overline{\text{SEC COMP}}$•SEC L3• RP PRE•BWCN
RESET PREAMBLE COMPARE ERROR	MCLR + LD CMD + OP4 + OP7

In case of simultaneous set and reset, reset has priority.

4.4.3 Write Protect Error

The write protect error flip flop is enabled when a write operation is attempted on a write protected sector or disk unit. The logic equation for the setting or resetting of this flip flop is as follows:

SET WRITE PROTECT ERROR	WPSW•(OP1 + OP2 + OP5 + OP6) + WPROG• (OP1 + OP2 + OP6)• SEC L3•RP•PRE•BWCN
RESET WRITE PROTECT ERROR	MCLR + LD CMD

4.4.4 Bad Sector Flag

A bad sector flag is generated when the bad sector flag bit is set in bit 10 of the second word of the preamble. An error bit is generated in the status register but the disk formatter operation is not terminated. The logic equation for the operation of this flip flop is as follows:

SET BAD SECTOR FLAG = BSECF•SECL3•RP•PRE•BWCN

RESET BAD SECTOR FLAG = OP7 + OP4 + LD CMD + MCLR

The bad sector flag logic is designed so that when a set and reset condition is on the flip flop simultaneously, the reset side has priority over the set side.

4.4.5 Format Error

A format error is generated anytime the clean sector compare flip flop is still set when the next sector pulse is generated. See Figure 4.21.

This is usually caused by reading a sector with no data written on it or having a pack in the disk with smaller sectors than the formatter is configured for (e.g., putting a 24 sector pack in a drive tied to a 16 sector formatter). A format error terminates operation in the formatter.

The logic equation for the set and reset condition of this flip flop is as follows:

SET FORMAT ERROR	BUSY•SEC PULSE•CLEAN SECTOR COMPARE
RESET FORMAT ERROR	MCLR + LD CMD

4.4.6 Time Out Error

A time out error is generated when an invalid sector number is selected or when the disk formatter does not go NOT BUSY within about two seconds and the operation is not complete. An error bit is input to the status register and the operation is terminated. The logic for the time out error is shown in Figure 4.33.

4.4.7 Cylinder Address Error

A cylinder address error is generated in the disk drive when a cylinder address that exceeds the selected disk unit is loaded into the cylinder address register. This error is gated through the formatter, and terminates the current operation. The only way this error can be cleared is by:

1) Unloading the disk drive with the load/unload switch, or

2) Issuing a legitimate cylinder address to the drive.

4.4.8 Not Operational

A not operational status is generated in the disk drive when 1) the unit is not selected, 2) not on, 3) not up to speed, or 4) malfunctioning. This error is gated through the formatter and terminates the current operation.

4.5 BUSY

The BUSY circuit is shown in Figure 4.34. The loading of the Command Register sets the BUSY flip flop. The setting of this flip flop causes the Disk Formatter to wait until SEEK is complete, then the operation begins.

The BUSY signal indicates that the Disk Formatter is busy with an operation. When BUSY=1 there can be no transfers other than data over the CPOB or CPIB data busses.

LOGIC EQUATIONS FOR BUSY FLIP FLOP

Function	Operation	Equation
Set BUSY	All Operations	LD CMD
Reset BUSY	Read Operations	RR•SECLN3•BWCN
Reset BUSY	Write Operations	SECLN4•BWCN
Reset BUSY	Premature Terminations caused by Errors	PRECOM+CAE+NRDY+BSEC+WPROT+TIMEOUT
Reset BUSY	All Others	MCLR+NO-OP

4.6 DONE

The DONE circuit is also shown in Figure 4.34. The DONE pulse is approximately 1 microsecond in duration, and indicates that the Disk Formatter has completed an operation. DONE occurs when BUSY goes from 1 to 0.

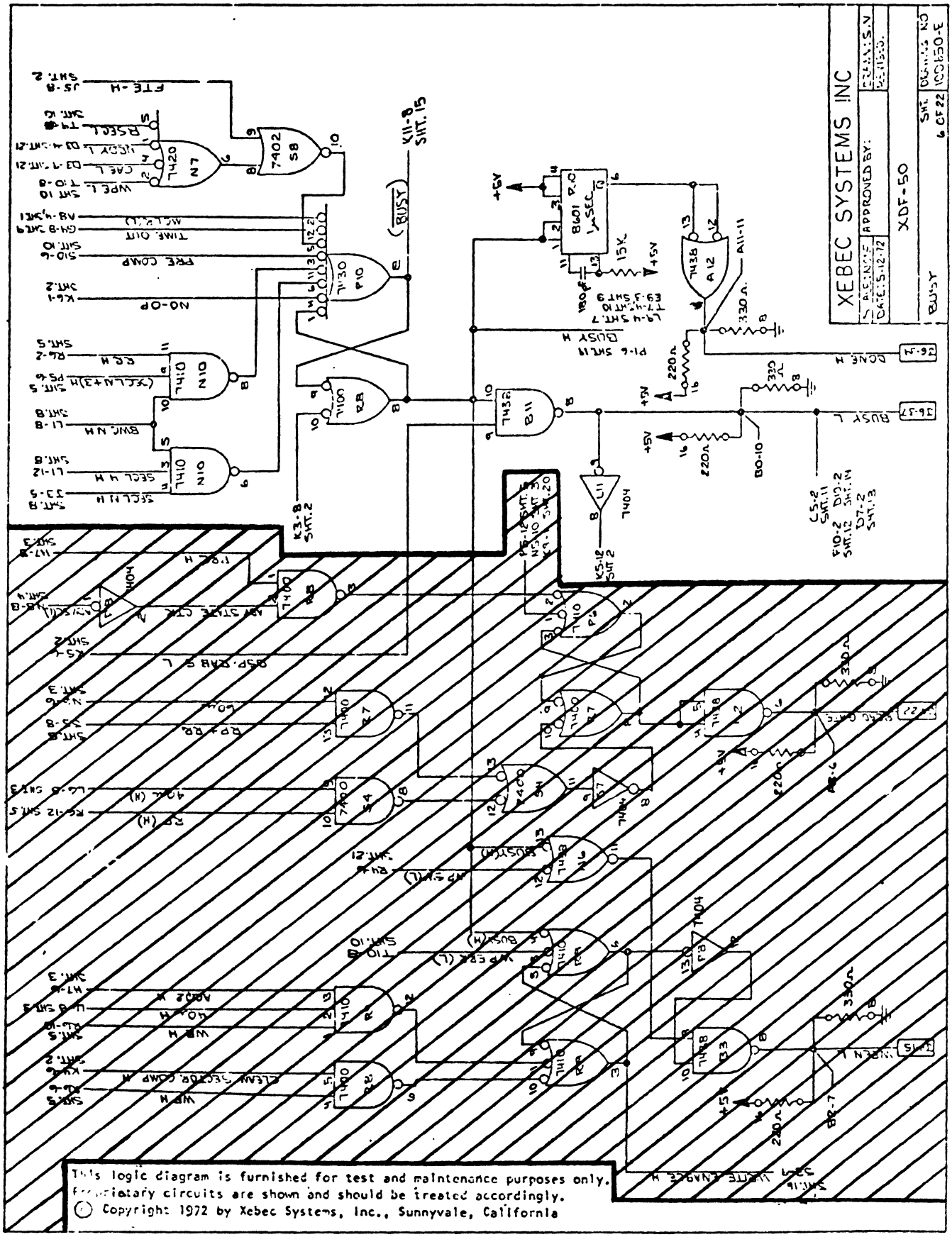


FIGURE 4.34
Busy and Done Circuit

4.7 FORMAT AND DISK OPTIONS

4.7.1 Format Options

The sector format of the number of words of data on the disk can be modified by placing jumpers on a program plug located in H3. The format parameters are:

# of Bit Per Word. (12 or 16)
# of Words Per Sector

The allowable number of words per sector is a function of the number of sectors per revolution and the number of bits per word.

	Max. # of Words per Sector				
Bits Per Word \ Sector Size	8	12	16	24	32
12	256	256	256	160	96
16	256	256	192	128	64

4.7.2 Disk Options

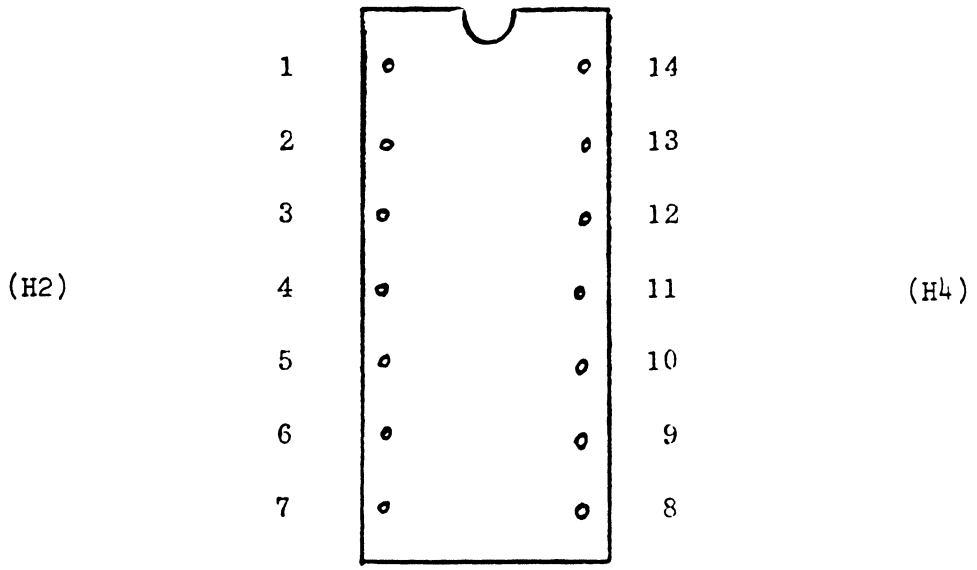
Various parameters of the disk interface signals are selectable by jumpers placed on program plugs located in M3.

These parameters are:

Output to Disk:

Polarity of disk select signal
Polarity of head select signal
Polarity of double frequency write data

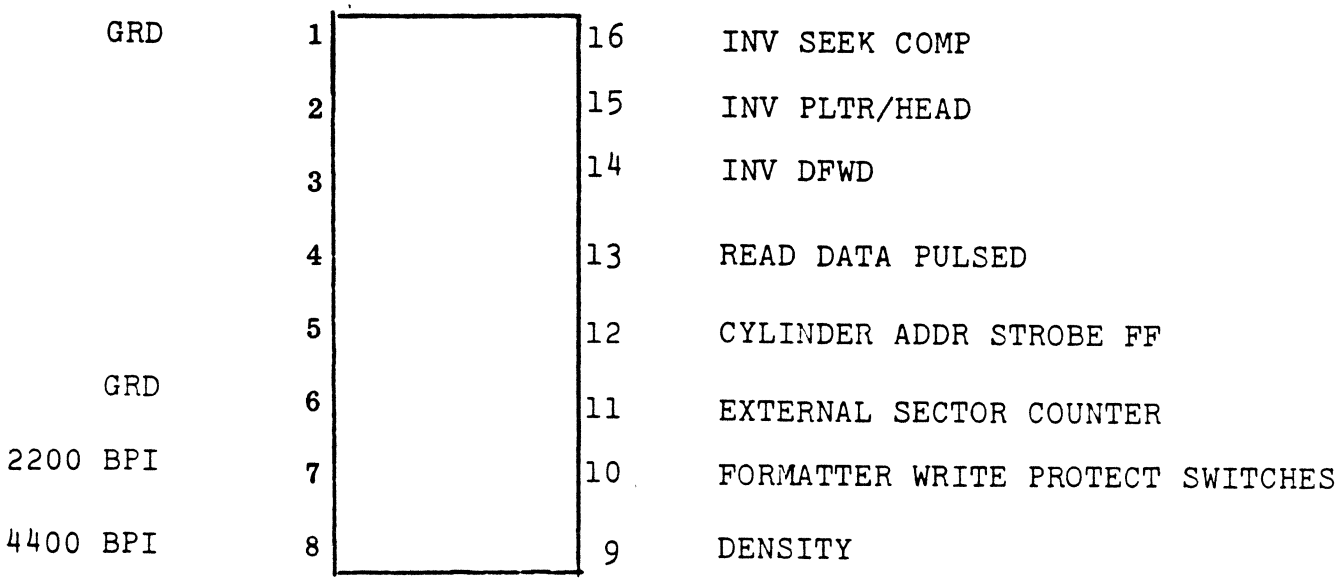
Orientation of Jumpers on Program Plug.
Located in H3.



Function		Jumper
Bits per Word	12	No jumper from pin 7-8
	16	Jumper in from pin 7-8
Words per Sector	32	1 - 2
	64	1 - 3
	96	1 - 4
	128	1 - 5
	160	1 - 10
	192	1 - 11
	224	1 - 12
	256	1 - 13

DISK OPTIONS
(XDF-50 Artwork Revision E and Above)

ORIENTATION OF JUMPERS ON PROGRAM PLUG LOCATED IN M 3



FUNCTION	JUMPERS
Disk Packing Density	6-8 Must Be On All XDF-50
Seek Select	
H=	
L=	
Platter/Head Select	
H=Upper	2-15
L=Lower	----
Double Freq. Write Data	
Pos. Edge	3-14
Neg. Edge	----
External Sector Counter	6-11
Internal Sector Counter	----
Read Data Pulsed	4-13
Read Data Level	----
Cyl Addr Strb Pulse	----
Cyl Addr Strb FF (Addr Ack)	5-12
Formatter Write Protect Sw	7-10

Input from Disks:

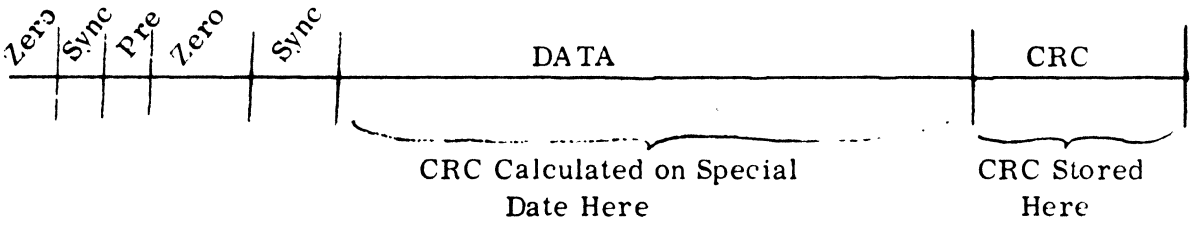
Polarity of SEEK complete
Select internal or external sector counter
Select type of read data - (Pulse or Level)
Type of cylinder address strobe (Pulse or flip flop)

Disk Speed - 1500 RPM or 2400 RPM - Selected by crystal frequency
6.354 Mhz = 1500 RPM
10.000 Mhz = 2400 RPM

4.8 CRC REGISTER

The Cyclic Redundancy Check (CRC) logic used to detect data errors within the XDF-50 Formatter is shown in Figure 4.35.

The CRC used is accumulated in a 16 bit shift register and is calculated on all data bits in the record portion of the sector. Note that the zero's fields, sync words, and preamble are excluded from the CRC calculation. It should also be noted that the CRC is maintained in a 16 bit register even if the data word is set to 12 bits or 16 bits in length. The CRC is actually calculated on the collection of serial data recorded on the disk and the resulting CRC stored serially after the data field.



The checking polynomial used is $1+x^2+x^{15}+x^{16}$.

For encoding, the serial data is entered at the high order end of the CRC register while the contents of the register is shifted toward the high order end. When the last bit of the serial data is entered, the calculated CRC is contained in the shift register. The data is shifted through the CRC register and then recorded on the disk.

When the data is read back, the CRC is calculated on the serial data from the disk as before. When the last data bit has been entered, the calculated CRC is again contained in the CRC register. The next 16 bits to be entered are the CRC calculated during the write cycle. As they are entered into the CRC register, the bits are compared one at a time to verify equality of the previously calculated and stored CRC to the currently calculated CRC. If equality exists, the CRC error flip flop is not set. If any set of bits differ, the CRC error flip flop is set and the error status reported through the status word.

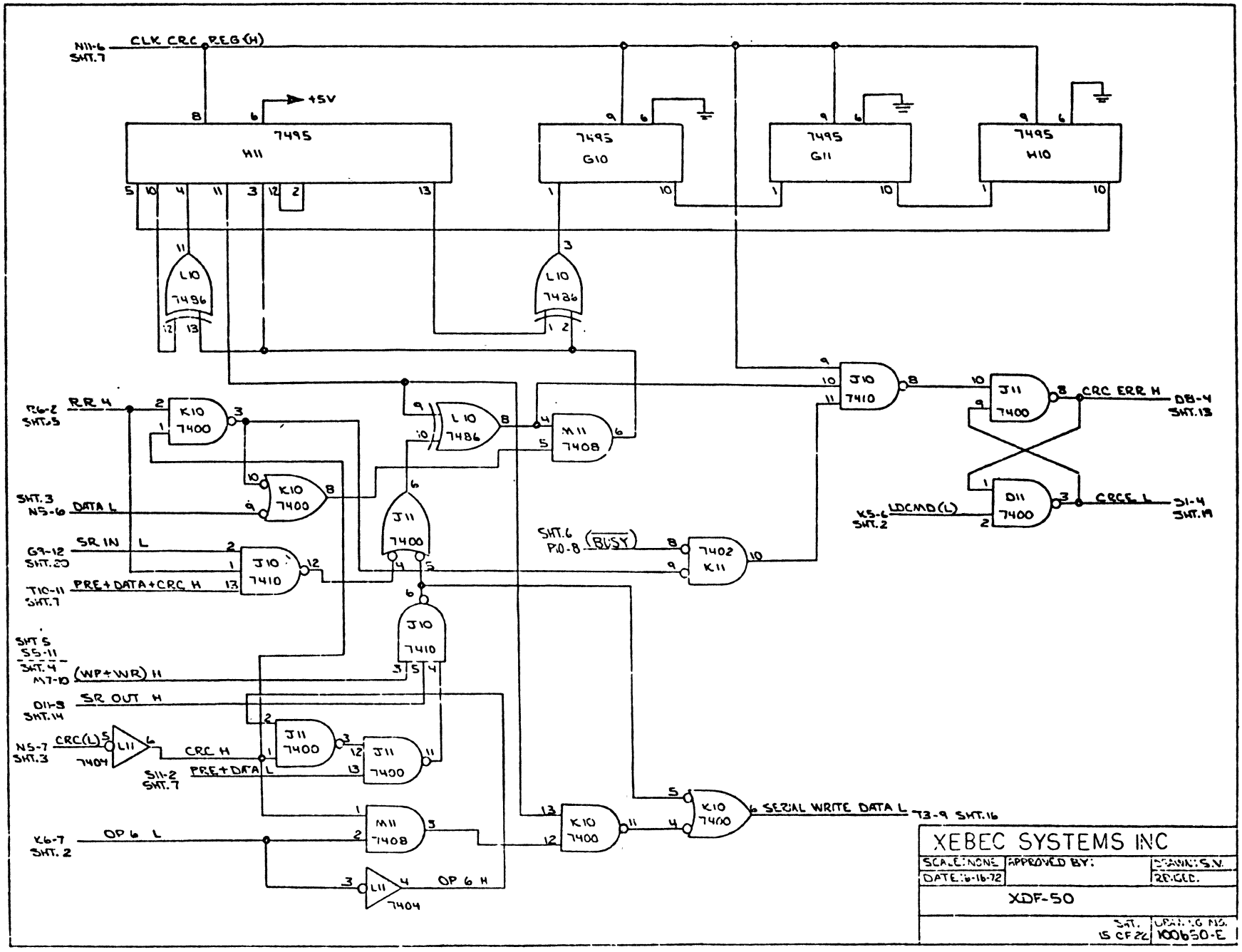


FIGURE 4.35
CRC Register
4-56

Table 4.4

Logic Equation For CRC Register

Condition (Figure 4.35)	
Serial Write Data	(WP + WR)• PRE + DATA) + (OP6• CRC)
	SR OUT + CRC Register (OP6• CRC)

SECTION 5
INSTALLATION/SHIPPING

This section describes the procedures for unpacking, setting up and connecting the XDF-50 Formatter. Also described is the procedure for packing the unit if it is to be shipped.

5.1 UNPACKING

A. Cut tape securing top end of box with a knife, being careful not to cut any deeper than is required to cut tape.

B. Remove and save manual which is taped to top of inner box.

C. Cut tape securing top of inner box with knife, being careful to cut only the tape and not the box.

D. Remove and save foam pad inside inner box.

E. Pull XDF-50 Formatter chassis by grasping edges of front panel casting and pulling straight up. It may be necessary to have someone else hold the box while the chassis is being removed.

F. Replace all foam pads, cardboard laminations, plastic sheets and other packing materials in the box and save. If unit is to be shipped again such as for factory service it must be shipped in this container to avoid shipping damage. See Section 5.7 for packing instructions.

5.2 INSPECTION

A. Remove formatter from plastic sack and visually inspect for shipping damage. If any shipping damage is noted, contact Shipping Carrier immediately to file insurance claim.

B. Remove top cover from formatter chassis by loosening screws on both sides. It is not necessary to remove these screws to lift cover.

C. Check inside of formatter to see that screws and standoffs securing P.C. card are snug that dc power connector is in place.

D. If unit is to be used on 115 VAC, the unit has been properly configured at factory. Replace cover and proceed to paragraph 5.4. If unit is to be used on 230V, change power strapping per paragraph 5.3.

5.3 230 VOLT OPERATION

The formatter is normally set for 115 volt operation at the factory. If 230 volt operation is required, the transformer taps must be changed. The diagrams below indicate the proper settings.

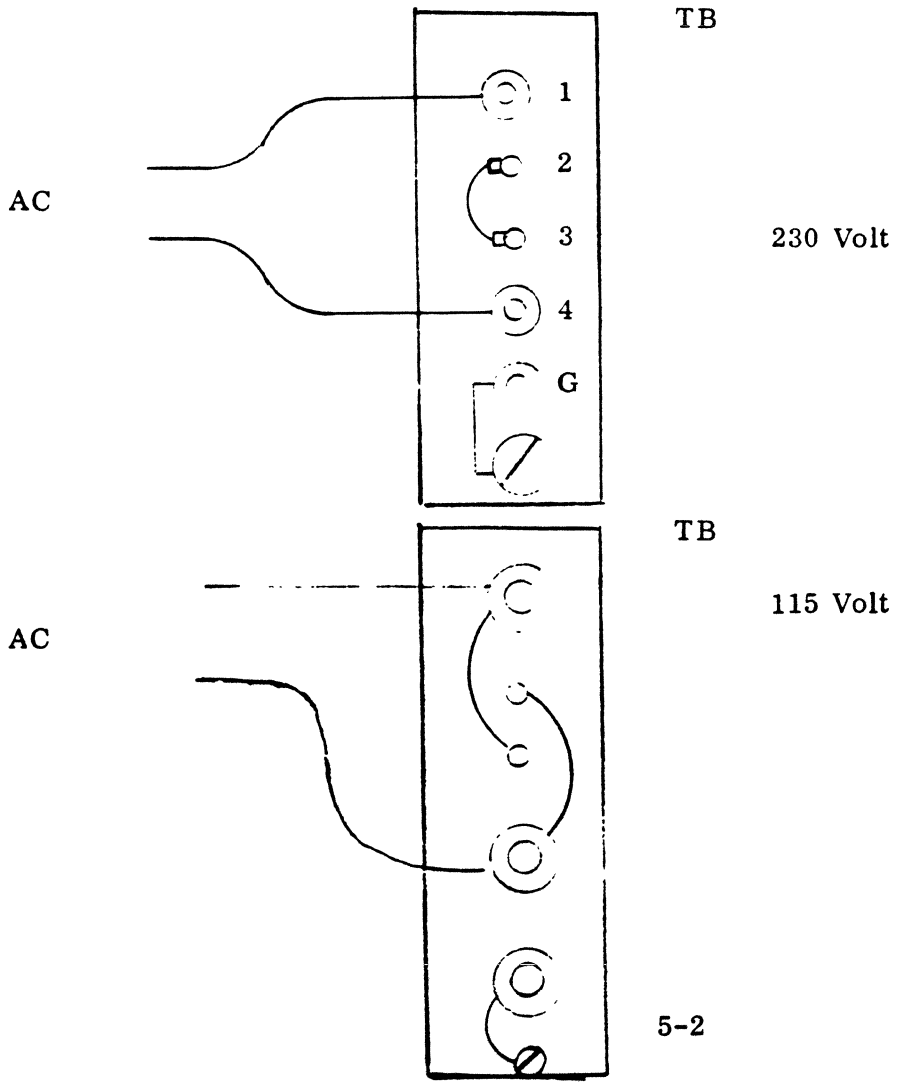
The procedure for setting transformer taps is:

A. Remove top cover of formatter.

B. Remove P.C. card(s) by removing screws and unplugging dc power connector.

C. Remove AC filter mounted over TB at rear of power supply.

D. Set jumpers on AC input connector at rear of power supply as below:



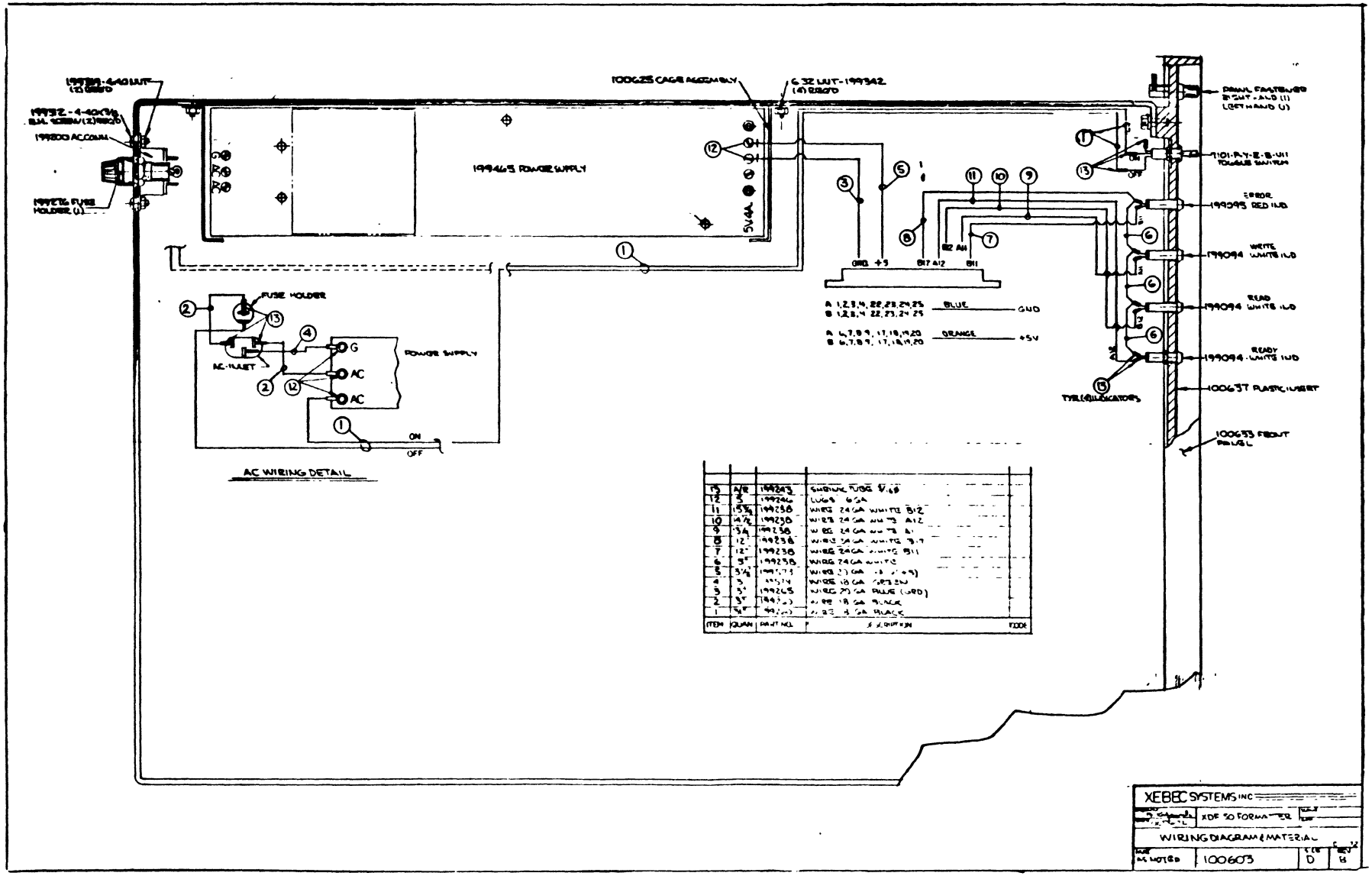


FIGURE 5.1
ASSEMBLY DETAIL
5-3

E. Replace P.C. Card(s) and DC Power Connector (s), tighten screws securing P.C. Card(s) finger tight.

F. Replace top cover.

5.4 PRELIMINARY TEST

This test verifies that the power supply is operational and that the DC is connected to the logic card.

After it has been ascertained that the power supply is configured for the correct AC voltage, plug in the power cord at the back of the formatter chassis, and connect the power plug to the appropriate AC outlet. Do not connect any other cables to the formatter. Switch on the AC power switch located on the front panel. The red error light should come on indicating that the power supply is operational. If the light does not come on, either:

A. AC fuse is blown (rear of chassis)

B. DC fuse is blown (internal to power supply)

C. DC connector not plugged onto card.

D. Lamp is defective.

E. Power supply is defective.

F. Power supply is out of adjustment (See 5.4.1 below)

5.4.1 DC Voltage Adjustment

The DC power output should be set to 5.0 $\pm$ .2 volts. A potentiometer which adjusts DC voltage is located on the regulator card. The voltage should be set initially with the connector disconnected from the card and the voltage measured at the DC terminal block.

If the voltage output is at about 1 volt, the overvoltage protect circuit has fired and the supply must be re-adjusted. First switch off the AC, then turn the potentiometer full CCW. Turn on AC, then slowly rotate potentiometer CW until voltage is at 5.0 $\pm$ .2 volts. Turn off AC, plug DC connector onto P.C. card then turn on AC and adjust to 5.0 $\pm$ .2 volts under load.

5.4.2 Current Limiting Adjustment

The power supply has a current limit adjustment. The current limit potentiometer is the one located on the power supply P.C. Board nearest the power supply fuse. The current limit pot is factory set and no adjustment is required.

5.5 RACK MOUNTING

If the optional slide mounting kit is provided, the unit is rack mounted as shown in Figure 5.2.

A. Select the location for the formatter to be mounted in the rack. It should be located near enough to the disk drive and computer to allow the cables to remain attached if the formatter is extended for service.

B. Separate chassis section slide and mount to chassis as shown in Figure 5.2. Use 10-32x3/8 screws supplied.

C. Connect rear extension bracket to back end of cabinet slide section using 10-32x3/8" screws and nuts, as shown in Figure 5.2.

D. Attach the slide mount brackets to the tapped rails. The center line of the bracket will be located 1.75" below the top of the formatter chassis when installed. Attach using 10-32x3/8 screws.

E. Extend cabinet slide sections to the full locked position (all the way out).

F. Slide chassis onto extended slide members, releasing locks as the unit is pushed to the rear of the rack.

G. Push unit to rear of rack until front panel contacts tapped rails. It may be necessary to loosen screws holding slides to tapped rails to allow unit to center. Be sure to tighten screws down again after centering.

5.6 INTERCONNECTING CABLING

Xebec Supplied Coupler/Drive

If the XDF-50 is supplied as part of a disk system which includes a computer coupler, the detailed interconnection instructions included as part of the coupler documentation should be followed.

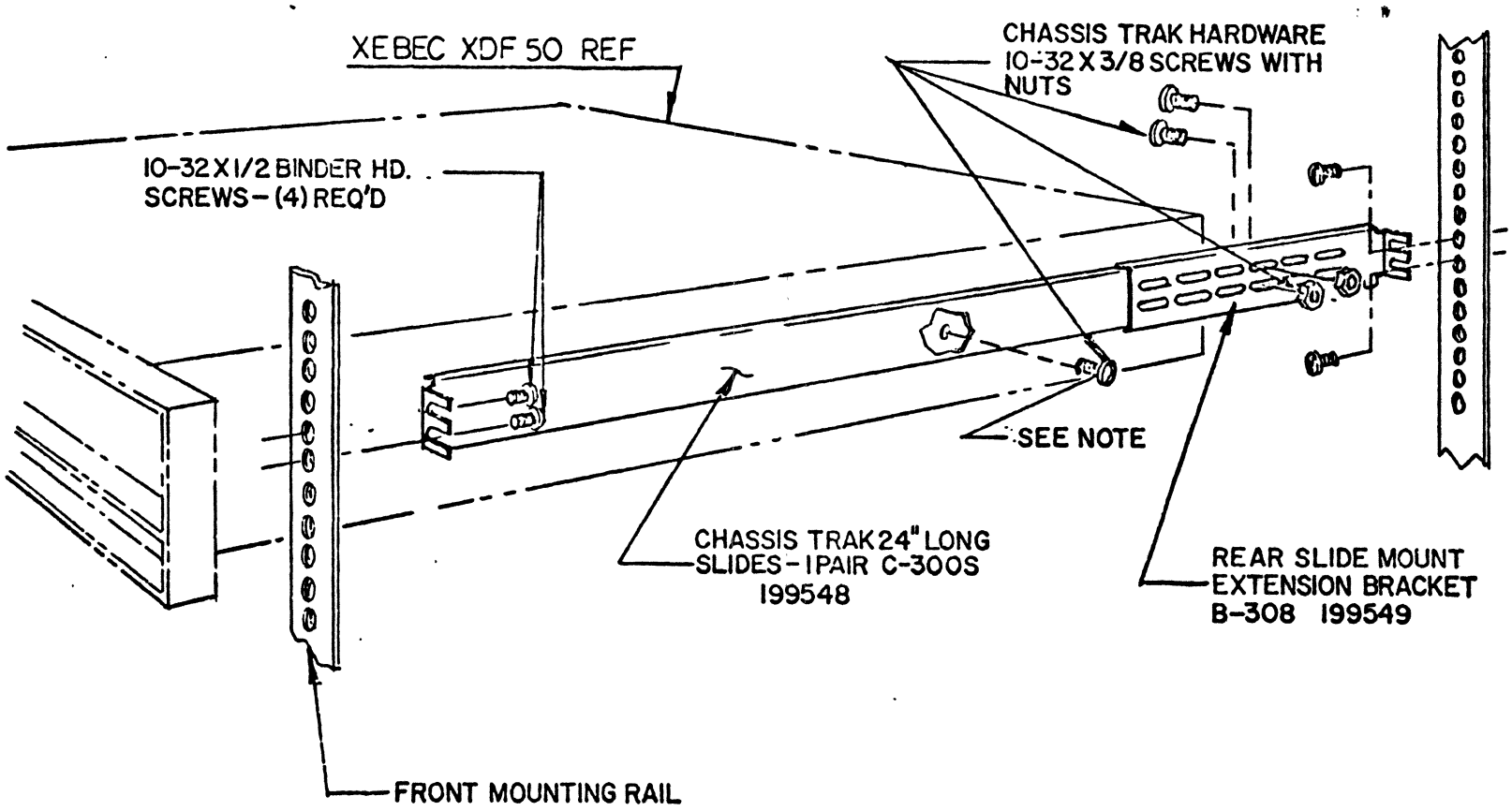


FIGURE 5.2
Slide Mounting

5-6

XDF-50/20/70

SLIDE KIT MOUNTING DETAIL

100602

NOTE

MOUNT CHASSIS SECTION OF SLIDES TO CHASSIS USING CHASSIS TRAK HARDWARE —

Customer Supplied Coupler/Drive

If the user is supplying his own interface and drive, the coupler will connect to J5 and J6, and the disk drive will connect to J4. See the interface specification Section 6 for description of the signals provided on these connectors.

5.7 PACKING INSTRUCTIONS

If the formatter must be shipped by common carrier, it should be packed in its original container according to the procedure below.

A. Wrap formatter in plastic sheet to prevent scratching in shipment. NOTE: Chassis half of slide rails must be removed prior to placing formatter in box.

B. Insert back of formatter in the styrofoam block with the smaller slot and slide this combination to the rear of the cardboard box.

C. Wrap manual and/or coupler cards in bubble pack and insert the bubble pack(s) into the space next to the top/bottom of chassis.

D. Fit the styrofoam block with the larger slot over the chassis front panel.

E. Insert cardboard tub next to styrofoam block. Place slide rails, mounting hardware and cables in the cardboard tub. Use sufficient packing material to prevent these items from moving during shipment.

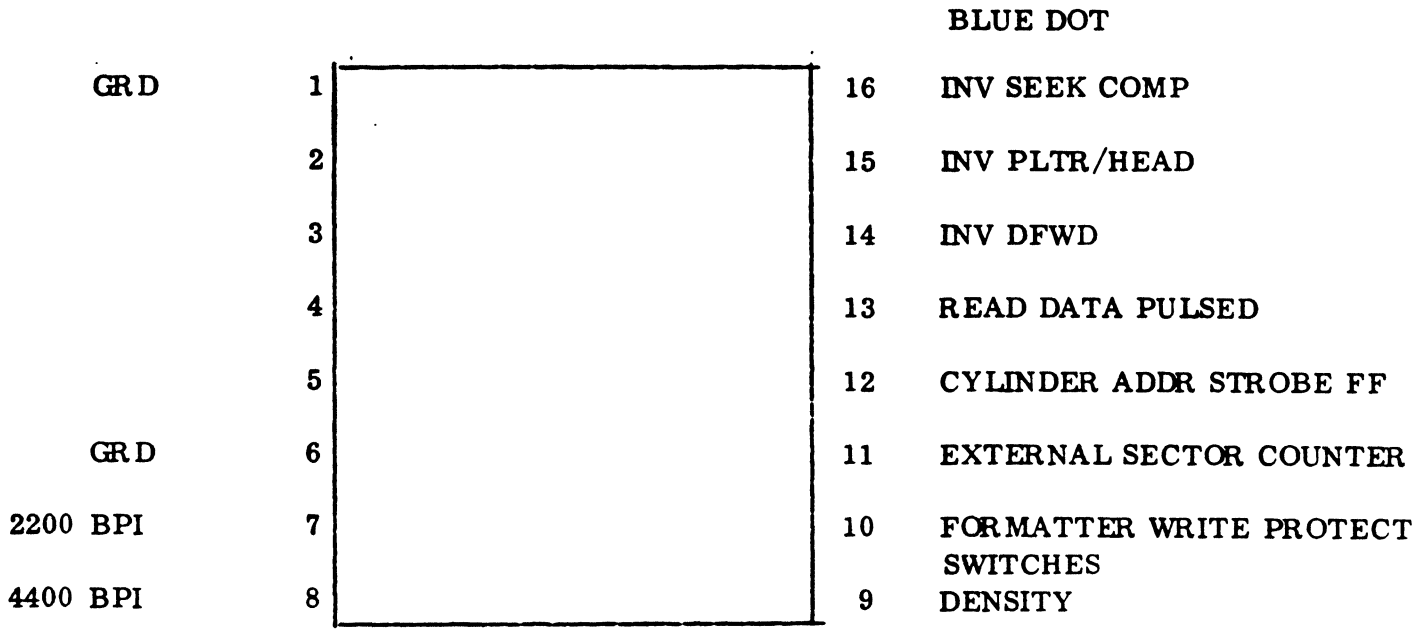
F. Close shipping container end flaps and seal with glass re-inforced tape.

PACKAGING DETAIL

PACKAGING DETAIL
FIGURE 5.3

DISK OPTIONS
(XDF-50 Artwork Revision E and Above)

ORIENTATION OF JUMPERS ON PROGRAM PLUG LOCATED IN M 3



FUNCTION	JUMPERS
Disk Packing Density	6-8 Must Be On All XDF-50
Seek Select	
H=	
L=	
Platter/Head Select	
H=Upper	2-15
L=Lower	----
Double Freq. Write Data	
Pos. Edge	3-14
Neg. Edge	----
External Sector Counter	6-11
Internal Sector Counter	----
Read Data Pulsed	4-13
Read Data Level	----
Cyl Addr Strb Pulse	----
Cyl Addr Strb FF (Addr Ack)	5-12
Formatter Write Protect Sw	7-10

SECTION 6
INTERFACE REQUIREMENTS

6.1 INTRODUCTION

The Xebec Moving Head Disk Formatter has two interfaces, one from the computer to formatter, and the other from the formatter to the Disk Cartridge Drive. However, from the coupler designer's point of view, the formatter interface logic that is required is reduced to loading and reading registers in the formatter. All timing and control of the disk memory is handled by the formatter.

6.2 INTERFACE SIGNALS

The signals between the formatter and interface coupler consist of 42 signal lines and associated ground. A block diagram of the disk formatter is shown in Figure 6.1. The signals at the interface coupler are described in greater detail in the balance of this section.

6.2.1 Register Selection

Five signals, which originate in the coupler, determine which register to select and whether to load it or read its contents. These signals are as follows:

A. RAB0, RAB1, RAB2	Three Register Address Bus lines that are decoded by the formatter into 8 possible states for register selection.
B. ISP	Input Strobe Pulse - A positive going pulse (0.500 usec to 1.5 usec) that is used to enable data onto CPIB 0-15 from a register specified by RAB0-2.
C. OSP	Output Strobe Pulse - A positive going pulse (0.5 usec to 1.5 usec) that is used to load the contents of CPOB 0-15 into a register selected by RAB0-2.

The assignment of the signals with respect to the registers in the formatter are as shown in Table 6.1.

The timing relationship of RAB0-2, ISP, OSP and the data on CPIB and CPOB buses is shown in Figure 6.2, Interface Signal Timing.

6.2.2 Coupler Output Bus

The Coupler Output Bus (CPOB) consists of 16 lines which contain data and commands that are to be transferred to the formatter. Tables 6.2 and 6.3 show the function of the bus for all bus addresses used.

6.2.2.1 CPOB Timing

Timing of the bus signals is shown in Figure 6.2. The CPOB must be stable within 400 nanoseconds before the leading edge of the output strobe pulse, and remain stable until 400 nanoseconds after the trailing edge of the output strobe pulse. Then the output bus must return to a high state (+2.4 to +5.0 volts) within 500 nanoseconds after the trailing edge of the output strobe pulse.

A quadruple 2-input positive NAND gate should be used to drive the CPOB. This logic device should be an open collector type such SN7438 or equivalent. No loads should be applied to the drivers in the coupler since the cable and controller require that the full fan out capability of the gate be used. The CPOB signals are low true (0.0 to +0.4 volts).

6.2.3 Coupler Input Bus

The coupler input bus (CPIB) is a 16 bit bus used to transfer data and status information from the formatter to the coupler. See Tables 6.2 and 6.3.

6.2.3.1 CPIB Timing

Timing of the bus signals is shown in Figure 6.2. The CPIB is stable within 400 nanoseconds after the leading edge of the input strobe pulse (ISP) and remains stable as long as the ISP is held to a "high" (+2.4 to +5.0 volts). The receiver for each bit of CPIB should be a single gate load such as SN 7400 or equivalent. The line should be terminated with the circuit shown in Figure 6.3. CPIB signals are low true (0.0 to +0.4 volts).

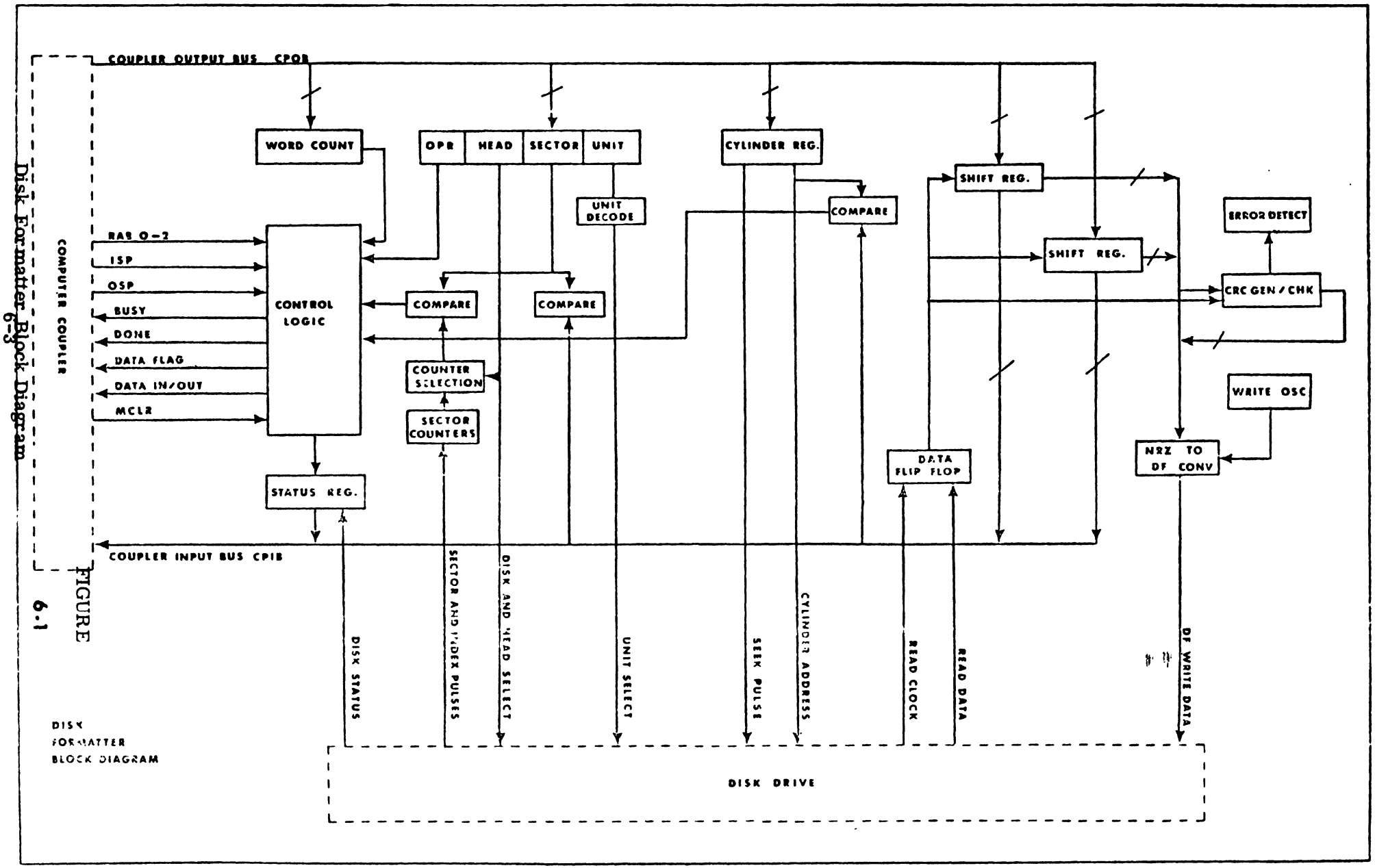


FIGURE 6-1

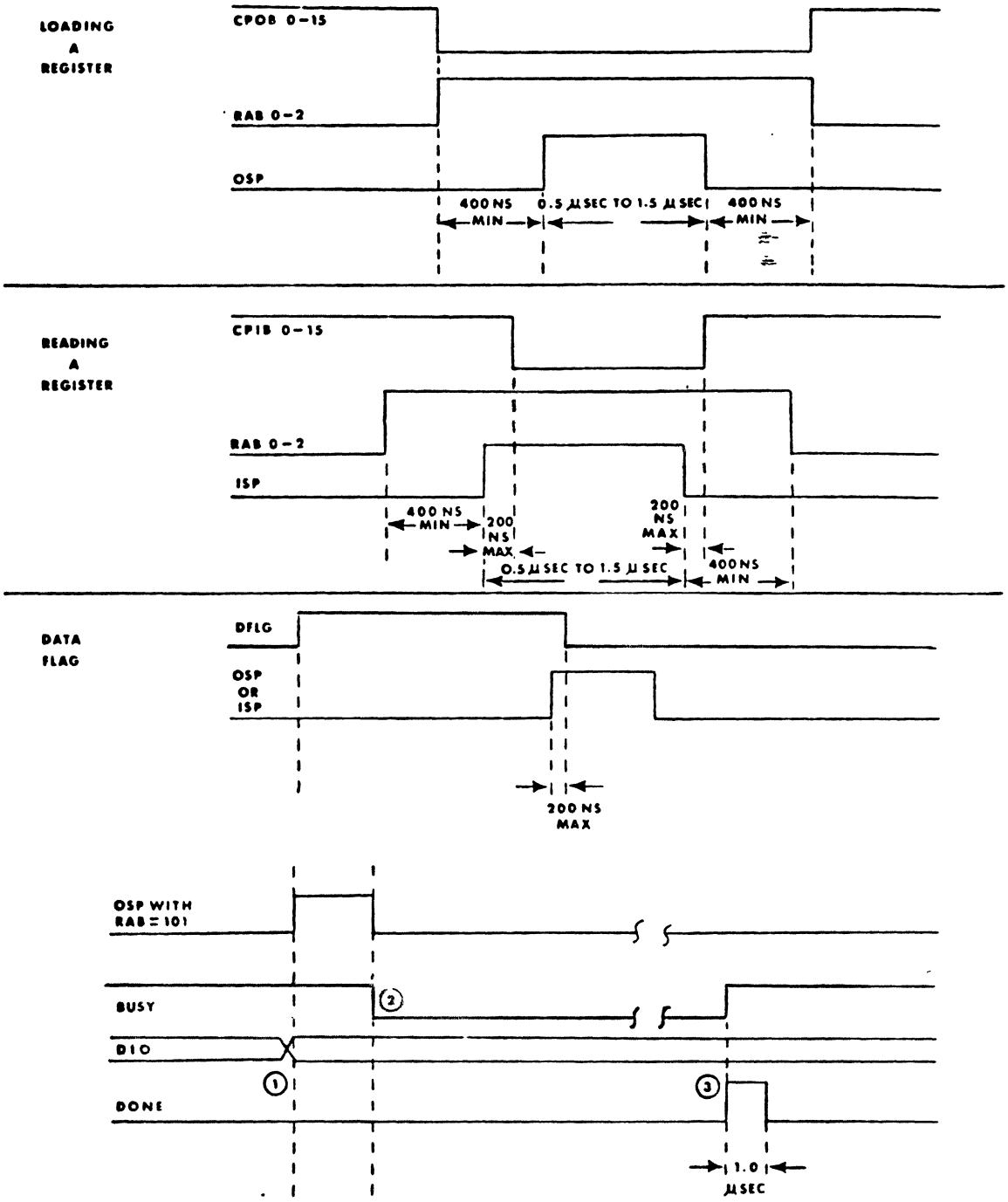
DISK FORMATTER BLOCK DIAGRAM

TABLE 6.1
REGISTER ADDRESS ASSIGNMENT

RAB2	RAB1	RAB	ISP	OSP	Register Name	Direction
0	0	0	0	P	Data Shift Register	To Formatter
0	1	1	0	P	Cylinder Address	To Formatter
1	0	1	0	P	Command	To Formatter
1	1	1	0	P	Word Count	To Formatter
0	0	1				
0	1	0	0	P	Unused	
1	0	0				
1	1	1				
0	0	0	P	0	Data Shift Register	From Formatter
0	1	1	P	0	Status Register	From Formatter
0	1	0				
1	0	0				
1	0	1	P	0	Unused	
1	1	0				
1	1	1				

LEGEND

P = Pulse (0.5 μsec to 1.5 μsec)



RELATIONSHIP OF BUSY AND DONE

(1) DIO IS STABLE WITHIN 300 NS AFTER LEADING EDGE OF (OSP).

(2) BUSY IS STABLE WITHIN 300 NS AFTER TRAILING EDGE OF (OSP).

(3) DONE IS FIRED ON TRAILING EDGE OF BUSY WITHIN 500 NS IF SEEK IS COMPLETE.

INTERFACE SIGNAL TIMING

6.2

TABLE 6.2
DRIVE CONNECTOR

Connector	Pin	Signal
J4	1	CYL0 (LSB)
J4	2	CYL1
J4	3	CYL2
J4	4	CYL3
J4	5	CYL4
J4	6	CYL5
J4	7	CYL6
J4	8	CYL7
J4	9	CYL8 (MSB)
J4	10	Restore
J4	11	Offset 1
J4	12	Offset 2
J4	13	Cylinder Strobe
J4	14	Ground
J4	15	Write Enable
J4	16	Ground
J4	17	Double Frequency Write Data
J4	18	Ground
J4	19	Head
J4	20	Platter
J4	21	Ground
J4	22	Read Gate
J4	23	Ground
J4	24	Read Clock
J4	25	Ground
J4	26	Read Data
J4	27	Ground
J4	28	Illegal Address/SEEK Incomplete
J4	29	Drive Ready
J4	30	Ground
J4	31	Sector 0
J4	32	Sector 1
J4	33	Sector 2
J4	34	Sector 3
J4	35	Sector 4
J4	36	Ground
J4	37	Sector Pulse Removable
J4	38	Ground
J4	39	Index Pulse Removable
J4	40	Ground

TABLE 6.2
DRIVE CONNECTOR
(Continued)

Connector	Pin	Signal
J4	41	Sector Pulse Fixed
J4	42	Ground
J4	43	Index Pulse Fixed
J4	44	Ground
J4	45	Unit Select 0
J4	46	Unit Select 1
J4	47	Unit Select 2
J4	48	Unit Select 3
J4	49	Seek Complete
J4	50	Write Protect External

TABLE 6.3
FORMATTER TO COUPLER CONNECTOR

Connector	Pin	Signal
J5	1	CPOB 0
J5	2	Ground
J5	3	CPOB 1
J5	4	Ground
J5	5	CPOB 2
J5	6	Ground
J5	7	CPOB 3
J5	8	Ground
J5	9	CPOB 4
J5	10	Ground
J5	11	CPOB 5
J5	12	Ground
J5	13	CPOB 6
J5	14	Ground
J5	15	CPOB 7
J5	16	Ground
J5	17	CPOB 8
J5	18	Ground
J5	19	CPOB 9
J5	20	Ground
J5	21	CPOB 10
J5	22	Ground
J5	23	CPOB 11
J5	24	Ground
J5	25	CPOB 12
J5	26	Ground
J5	27	CPOB 13
J5	28	Ground
J5	29	CPOB 14
J5	30	Ground
J5	31	CPOB 15
J5	32	Ground
J5	33	OSP
J5	34	Ground
J5	35	ISP
J5	36	Ground
J5	37	RAB 0
J5	38	Ground
J5	39	RAB 1
J5	40	Ground
J5	41	RAB 2
J5	43-50	Unused

TABLE 6.3
FORMATTER TO COUPLER CONNECTOR
(Continued)

Connector	Pin	Signal
J6	1	CPIB 0
J6	2	Ground
J6	3	CPIB 1
J6	4	Ground
J6	5	CPIB 2
J6	6	Ground
J6	7	CPIB 3
J6	8	Ground
J6	9	CPIB 4
J6	10	Ground
J6	11	CPIB 5
J6	12	Ground
J6	13	CPIB 6
J6	14	Ground
J6	15	CPIB 7
J6	16	Ground
J6	17	CPIB 8
J6	18	Ground
J6	19	CPIB 9
J6	20	Ground
J6	21	CPIB 10
J6	22	Ground
J6	23	CPIB 11
J6	24	Ground
J6	25	CPIB 12
J6	26	Ground
J6	27	CPIB 13
J6	28	Ground
J6	29	CPIB 14
J6	30	Ground
J6	31	CPIB 15
J6	32	Ground
J6	33	DIO
J6	34	Ground
J6	35	DFLG
J6	36	Ground
J6	37	Busy
J6	38	Ground
J6	39	Done
J6	40	Ground
J6	41	MCLR
J6	42	Ground
J6	43-50	Unused

6.2.4 DMA Data Control

Serial data to and from the disk drive unit is converted to a parallel data word by the formatter. The burst transfer rate of parallel data is as shown in Table 6.4.

TABLE 6.4

Disk Speed	Word Length	Average Word Transfer Rate	Maximum Time To * Respond to Data Flag
1500 RPM	16 Bit	99 KHz	9.2 usec
1500 RPM	12 Bit	132 KHz	6.7 usec
2400 RPM	16 Bit	158 KHz	5.7 usec
2400 RPM	12 Bit	211 KHz	4.2 usec

LEGEND *

Includes worst case frequency variation and formatter timing.

A direct memory access port is usually used to handle word rates in this range. The signals that are used to control the transfer rate are as follows:

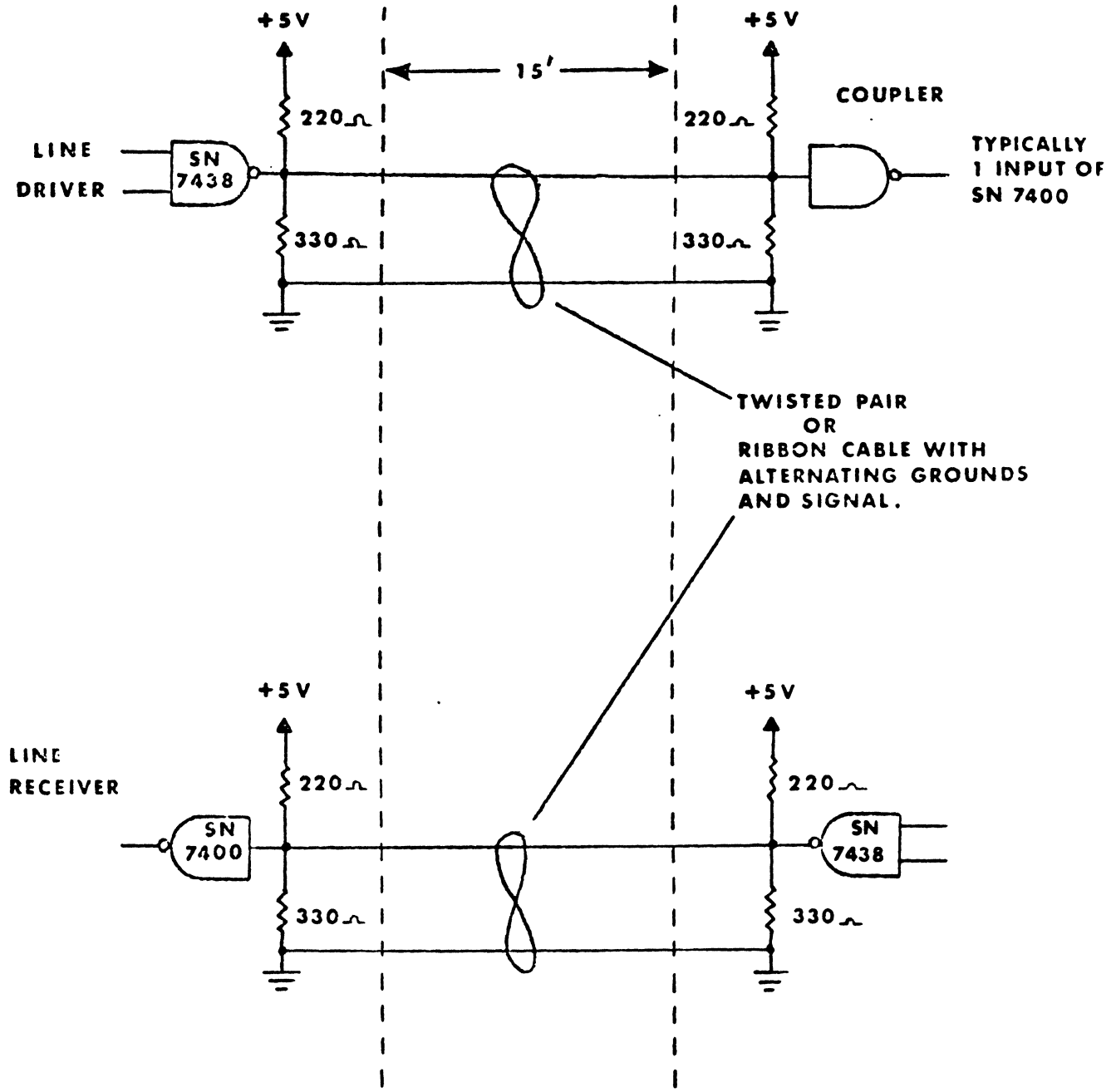
6.2.4.1 Data Flag

A high true level (+2.4 to +5.0 volts) indicates that the formatter is ready to receive another word in its output buffer (Write on Disk) or has assembled a word in its output buffer (Read from Disk).

The data flag is reset by issuing either:

ISP with RAB=000 for read from disk modes, or
OSP with RAB=000 for write on disk modes.

If this reset signal is not received within a specified time, the disk will have missed a word and a data rate error status bit will be set. The maximum allowable time to respond to a data flag is listed in Table 6.4.



SIGNAL TERMINATION

FIGURE 6.3

6.2.4.2 Data In/Out

The direction of data transfer is specified by the Data In/Out (DIO) line which originates in the formatter.

The convention for transfer is:

Logic 0 - Input to Coupler
Logic 1 - Output from Coupler

The timing of this signal is shown in Figure 6.2.

6.2.5 Basic Formatter Status

Two signals are provided by the formatter to indicate when it is BUSY with an operation and when it is DONE with an operation.

6.5.2.1 BUSY

BUSY indicates that the formatter is busy with an operation. If BUSY = 1 no transfers other than data may take place over the two data buses. RAB should be set to 000 during the entire interval when BUSY = 1.

The relationship of BUSY to RAB 101 and OSP is shown in Figure 6.2. It should be noted that BUSY is delayed until the trailing edge of OSP. This is done to prevent RAB from converting from 101 to 000 while OSP is still true, since the user normally will interlock BUSY with the logic used to generate the RAB signals. BUSY is a low true signal.

6.5.2.2 DONE

The DONE signal is a 1 usec pulse which occurs when the BUSY goes from 1 to 0. It is normally used to generate a computer interrupt to indicate completion of any operation. DONE is a high true signal.

6.2.6 Master Clear

Master Clear (MCLR) is a signal generated by the coupler to reset all control flip flops to idle state and reset BUSY. MCLR also resets, WPE, PCE, TMO, FTE, CRCE, RATE, and BSEC error flip flops. If it is set, MCLR should be a low pulse (0.0 to +0.4 volts) and a minimum of 500 nanoseconds long. MCLR is terminated in the controller by the network shown in Figure 6.3. It is recommended that MCLR be driven by a TTL gate such as SN7438 or equivalent.

6.3 INPUT/OUTPUT CONNECTORS

The I/O interface signals connect with the disk formatter by way of a set of two (2) adjacent edge connectors located at the rear of the chassis. The edge connectors are as shown in Table 6.5. Any edge connector selected should be compatible with flat cable or ribbon cable manufactured by 3M or Spectra Strip.

If flat cable or ribbon cable is not compatible for the user's application, then a standard edge connector with pierced posts for soldering may be substituted. Connectors of this type are available from a wide range of manufacturers.

6.4 CABLE DESIGN

6.4.1 Coupler Interface and Disk Drive

A. Coupler Interface

The cable may be manufactured using flat cable, ribbon cable or individual twisted pair. Flat cable or ribbon cable must have ground signals separating all signal lines. Twisted pair should have signal on one line of the pair and ground on the other. Maximum recommended length is 10 feet.

B. Disk Drive Interface

The disk drive may be fabricated using flat cable, ribbon cable or twisted pair. Maximum length is 15 feet. If the units are daisy chained, maximum recommended overall length of all cables is 15 feet.

TABLE 6.5
EDGE CONNECTOR SPECIFICATIONS

NAME	DIMENSION	UNIT
Card Thickness	0.054 - 0.071	inches
Number of Contacts	50 (25 dual)	pins
Contact Spacing	0.100 centers	inches
Width of Connector Throat	2.600	inches
Overall Width	3.90	inches

NOTE:

The connector type recommended by Xebec Systems, Inc. for use with this type of cable is 3M Part Number 3415-0000.