

Bell System Data Communications

TECHNICAL REFERENCE

●
Data Sets 201A and 201B

Interface Specifications

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September 1962
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PREFACE

This specification is specifically intended for designers of business machine equipment to be used with Bell System Data Sets 201A and 201B.

If additional details on the interface and its operation are needed, please contact:

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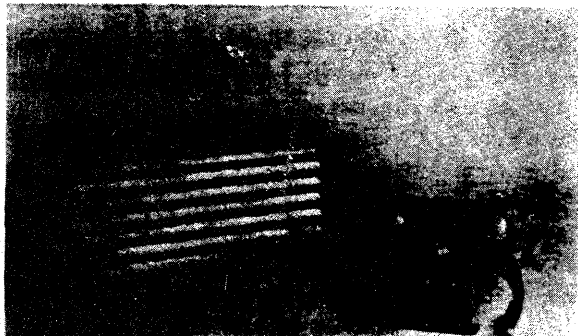
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DATA SETS 201A AND 201B - INTERFACE SPECIFICATION

This describes the operation and outlines the interface specifications of the Data Sets 201A and 201B. These sets, also known as "Four-Phase" sets, operate at fixed speeds. They accept binary data in serial form from the business machine at the transmitting end and deliver it in serial form to the business machine at the receiving end. The 201A operates at 2000 bits per second while the 201B is designed for 2400 bit per second operation. Each set provides timing signals at the transmitting end to "clock" the data out of the business machine equipment. (One version of these sets permits an external timing source to drive the transmitter.) At the receiving end the sets recover bit synchronism and provide a timing lead to the business machine equipment. The sets can be wired to operate either 2-wire or 4-wire. Automatic answering is also provided as a wiring option.

Both data sets measure 7-3/4"H x 17-1/2"W x 11-5/8"D and weigh approximately 35 pounds. The photograph shows the appearance of the 201A. The appearance of the 201B is similar.



Data Set 201A (or 201B)

1. INTRODUCTION

The Data Set 201A is designed to transmit and receive binary data at a fixed rate over a switched voice frequency telephone circuit or a private line. The 201B is designed primarily for private line use. Several unique features enable these sets to achieve a one bit per second data rate per cycle of bandwidth. These features include the way in which the data is encoded as a phase modulation, the stored reference in the receiver, and the method by which continuous timing synchronization is obtained in the receiver, directly from the line signal.

The transmission rate is fixed at 2000 bits per second for the 201A and 2400 bits per second for the 201B. The speed is determined by a crystal oscillator in the transmitter or by timing signals furnished by the business machine. The carrier frequency of the 201A is 1750 cps and the principal line signal spectrum covers the range from 750 cps to 2750 cps. The carrier frequency of the 201B is 1800 cps and the principal line signal spectrum ranges from 600 to 3000 cps.

The sets may be connected for two-wire operation, four-wire operation, and four-wire continuous operation. In two-wire operation the receiver is normally on and the transmitter is normally off. In four-wire operation the receiver is always on and for continuous operation the transmitter is always on. When a customer wishes to transmit, he must change the polarity on the "Request to Send" lead from negative to positive. When the set is ready to transmit data, it will return a "Clear to Send" signal to the customer. When carrier is established at the receiver, a "Carrier On" signal and clock signals will be supplied to the customer on the receiving end.

The customer must provide his own beginning and end of message codes and means for error detection or correction.

Transmitter

The data is encoded on a carrier wave as a succession of signal element phase shifts, each of which is an odd multiple of 45° (i.e., the phase may be shifted 1, 3, 5, or 7 times 45°), with respect to the previous signal element phase. In order to encode by means of these four phase shifts, the serial data, as received by the transmitter, is examined as pairs of binary digits, called "dibits." Since there are four possible dibit combinations (or codes) (i.e., 00, 01, 11, 10) each of the four phase shifts may be associated with one of the dibit codes. This means that the phase of the carrier for a particular dibit is shifted by some predetermined amount with respect to the phase just transmitted for the previous dibit. This is to be contrasted to phase modulation systems where the phase shift is in reference to a fixed phase reference. This scheme makes it unnecessary to transmit absolute phase information.

Receiver

The way that data is encoded, (and the relation between the data rate and the carrier frequency), provides a phase shift for each new dibit, regardless of what dibits, or succession of dibits, are received. The fact that the signal element phase is continually shifted enables the receiver to recover the necessary synchronization information. The operation of the bit synchronization recovery circuit which accomplishes this will be explained in detail in the text.

The data is determined by measuring the relative phase angle between the received signal element and the previous signal element delivered by a delay line (stored reference). The transmitter coding is such that one bit is determined by comparison to the delayed output while the other bit is determined by comparison to a delayed output, the phase of which is shifted by 90° . Pairs of bits are identified simultaneously, but delivered serially to the receiver data output circuit under control of the recovered timing synchronization signal. This clock signal also is supplied to the customer.

2. TRANSMITTER

While there are several ways in which data can be encoded into relative phase positions, the Bell System four-phase sets use the same basic method, differing only in details. As shown in Figure 1 (attached), the transmitter in each type of set has two separate sources of carrier, called Channel A and Channel B. These channels alternate in supplying the line signal, with the transfer from one channel to the other taking place gradually once each dibit. In other words, the signal from Channel A will be "on-line" for one dibit, Channel B the next, and so on. During the time the Channel A is supplying the line signal its phase is held constant, and it is during this time that the phase of Channel B (which is "off-line") is changed to the value that it will have during the next dibit interval.

The necessary phase changes, therefore, are made at a time when the channel being changed is not supplying the line signal. This technique produces a line signal which changes phase gradually as the signal from one channel takes over from the other. Abrupt phase changes, which would "splatter" energy over a wide frequency spectrum, are avoided.

As will be discussed later, the data will be recovered in the receiver by comparing the phase of the line signal corresponding to one dibit with the phase that existed during the previous dibit. This is called a "stored reference" system. This relative phase we will call the "epoch angle," and the relationship between it and the incoming data is shown in Figure 2. It is important not to confuse the epoch angle (change of carrier phase) with the absolute phase of the carrier; these are different parameters, although they are closely related.

Another parameter which is easy to confuse with the epoch angle is the shift in line signal phase that accompanies the transfer from one channel to the other. This shift is the difference in phase between the signal at the end of one dibit period and the new signal at the beginning of the next, and is known as the "tail-to-head" or "transition" angle. The epoch angle is the difference in phase between the line signals at the beginning of two successive dibit periods, or "head-to-head" angle. These are not the same because there are not an integral number of carrier cycles per dibit.

The circuit description in this section will be confined to the 201A data set with the internal timing option. While the basic principles of operation with external timing or of the other data sets in the four-phase family are the same, there are many differences in details.

As just discussed, the receiver compares the phase of the line signal with its phase one millisecond earlier in time (one dibit interval). This difference in phase is defined as the "Epoch Angle." The transmitter circuits produce the proper epoch angles in the line signal by controlling the INITIAL phase of the carrier generated for each dibit, i.e., the phase of the carrier at the beginning of the dibit interval.

With the "two-channel" technique and epoch angles that are odd multiples of 45° , it can be shown that there are only eight possible phases of line signal. Furthermore, these are divided into two families of four orthogonal phases, one for each channel, which are spaced 45° apart. This is shown in Figure 3.

For each dibit in the incoming data the transmitter circuits create the proper epoch angle in the line signal by (1) computing the new carrier phase to be transmitted, (2) setting the "off-line" channel to produce that phase of carrier until further instructed, and (3) switching channels.

In the 201A, all of these transmitter operations are locked to a crystal oscillator clock running at 14,000 cps, or eight times the carrier frequency. As shown in Figure 4A, the carrier frequency F_c is generated by binary counters that divide the clock signal by eight; details of these carrier generators are covered later, and are shown on another figure.

Another output from the clock is passed through successive stages of frequency division to produce the many timing signals used within the set and by the customer's equipment. The first stage is a division by seven, which produces the SCT signal, or "bit clock." This is a square wave at 2,000 cps, and is furnished to the customer for clocking his source of data at the precise rate required by the 201A. The next stage divides this signal by two, and produces the DCT signal, or "dibit clock." DCT is a square wave at the dibit rate of 1,000 cps and is used only for internal timing purposes, although it is present on the interface. The last stage again divides by two, producing the E signal, a 500 cps square wave also used for internal timing. The E signal produces two pairs of pulses (EP and EN, E'P and E'N) that control the flow of information within the data set. The interrelation of the SCT, DCT and E signals and these control pulses is shown in Figure 4B.

These two chains of frequency dividers fix the ratio of F_c to DCT at $1 \frac{3}{4}$ to 1 for the 201A. The 201B generates similar timing signals, but by different circuit arrangements. For this set the ratio of F_c to DCT is $1 \frac{1}{2}$ to 1.

Another major function of the E signal is controlling the gradual transfer from one channel to the other. The E signal passes through a filter that removes its higher components, leaving only a 500 cps sine wave, known as the ENV signal. The output of the Channel A carrier generator is then amplitude modulated by this ENV signal as shown in Figure 5A. The inverted E signal (called E') is also stripped of its harmonics to produce the ENV' signal, a 500 cps sine wave opposite in polarity to the ENV signal. The ENV' signal amplitude modulates the Channel B carrier so that it is at minimum level when Channel A is at its maximum.

After the carrier signals (which are square waves) are amplitude modulated, each is passed through a low pass filter to eliminate its out-of-band components (harmonics of 1,750 cps). These two signals are then added together to make up the line signal. As Figure 5B shows, the line

signal changes phase gradually as one channel decreases in level and the other increases. Figure 5C shows in another way how the phase changes occur. Proceeding from left to right, we see how at first the line signal L is dominated by Channel A. Then as A decreases in amplitude and B increases, the phase of the line signal swings smoothly around until it becomes that of Channel B.

As mentioned earlier, the carrier signals are generated by dividing the clock signal by eight, in a chain of three binary counters. The first stage of division (see Figure 6) is known as the "common binary;" after this stage, the circuit splits into Channel A and Channel B branches. The second and last stages of division in each channel are known as the "channel binaries." Note that the Channel A binaries are fed from the "1" output of the common binary, while the Channel B binaries are fed from the "0" output. As is evident from the waveform diagrams, this results in a 45° difference between the phase diagrams for the two channels. (In connection with Figure 3, this was shown to be necessary.)

The channel binaries in each channel make up a two-digit binary counter whose input is the signal from the common binary. At any instant the state of each counter can (and will, in this paper) be expressed as a two-digit binary number, referring to the state of the Channel A binary as "A" and to that of the Channel B binary as "B." Note, however, that the state of the last counter stage is the "most significant" digit in the number describing the channel binary state. Note also that the "carry" signal to the last counter stage is taken from the "1" output of the first; this makes each counter a "down-counter," following the sequence A (or B) = 11, 10, 01, 00, 11, 10, 01, 00, etc.

The waveforms in Figure 6 assume that the channel binaries of each channel start counting in the "00" state. Figure 7 shows the effect of starting the Channel A binaries in each of the four possible states. It is evident that one out of four carrier phases can be selected by setting the channel binaries into the correct initial starting condition. The dividers are then allowed to run freely (generating carrier) until the next change of phase is to be made. A similar set of waveforms could be drawn for Channel B.

Figure 8A shows a summary of the carrier phases produced by each channel if the various initial conditions are put into that channel's binaries. Comparison with Figure 3 shows that

the necessary carrier phases can all be produced. From this, it follows that any epoch angle can be generated in the line signal by starting the off-line channel binaries in the proper state. Figure 8B illustrates this point.

Figure 9 shows how the channel binaries are set into the proper starting condition, or "initialized." The incoming data are first processed by the "phase logic" circuits which produce pulses on a pair of leads connecting to the "phase register," whose contents at any instant we will call "C" (a two-digit binary number). This register acts as a subtractor. A pulse on one input lead causes 10 to be subtracted from the contents of the register and the remainder left in the register; a pulse on the other input lead subtracts 01. These pulses may be considered as a (binary) number " ΔC ," which is subtracted from the number "C" in the register.

Once each millisecond (at the end of each dibit in the incoming data) control pulses open the gates between the register and the off-line pair of channel binaries, and those channel binaries are set into a new initial condition. If Channel B is being initialized, the number contained in the register will be transferred to its channel binaries. That is, after the transfer is complete, the state of the Channel B binaries will be the same as the number contained in the register, or $B = C$. When Channel A is being initialized, the process is similar, but the "most significant" digit is inverted in the transfer ("1" becomes "0," and vice versa), or $A = C + 10$. The register contents are not affected by these transfers.

In Figure 10, the carrier phases are marked with the corresponding register contents, rather than the channel binary state. This figure is the same as Figure 8 except that it reflects the inversion that occurs in Channel A during the transfer.

We can find from Figure 10A what pulses must reach the register (ΔC) to produce each epoch angle. For example, if Channel B is "on-line" with the carrier phase corresponding to "00" in the register at the time it was set up one millisecond ago and if the data require that an epoch angle of 135° be generated, then we must somehow change the register to "01" before initializing Channel A. This is because inspection of Figure 10 shows that the phase this will produce corresponds to a change of 135° from the current "on-line" phase. Thus we must subtract "11" from the "00" left in the register when Channel B was initialized (00 -

11 = 01 in binary) requiring a pulse on each input lead, or $\Delta C = 11$. This is illustrated in Figure 10B.

However, Figure 10B illustrates only one way of producing a 135° epoch angle; all told there are eight ways, corresponding to the eight possible reference carrier phases. If we inspect all eight ways, two facts emerge; (1) as long as the reference is a Channel B phase as illustrated we get a uniform answer of $\Delta C = 11$, but (2) using a Channel A phase as reference produces a different answer, $\Delta C = 00$.

The results of this process for each epoch angle are tabulated in Figure 11. As shown, the results depend on which channel is being initialized. However, inspection shows that the difference between channels is a constant one. Each time we go to Channel B we must subtract an additional "01." This, of course takes place every other dibit.

Figure 12 shows how the ΔC pulses are computed. The data logic circuits develop directly from the incoming data what might be called the basic ΔC (i.e., the one needed when going to Channel A) in the form of pulses called "D180" and "D90." The data logic is such that a D180 pulse is generated if the first bit in the dibit is a "1" (dibits 10 and 11) and a D90 pulse is generated if the two bits in the dibit are different (dibits 01 and 10). Then an additional pulse on the "01" lead is generated every other dibit (by the "EP" signal) to subtract the extra "01" needed when Channel B is being set up.

These pulses are not coincident; they are spread over the dibit interval as diagrammed on Figure 13. As shown, the D180 pulse occurs when the first bit is sampled (if the data is a "1"), and the D90 pulse when the second bit is sampled (if it is unlike the first). Then two things happen in quick succession at the end of the dibit; first, the EP (or E'P) pulse sets the channel binaries to the "11" state. With the circuit arrangements used, this is a necessary prelude to transferring the information in the register to the channel binaries. This pulse also subtracts "01" from the contents of the register if Channel B is the one being initialized. Then about 5 microseconds later the EN (or E'N) pulse opens the gates between the register and the channel binaries to complete the transfer.

Let us now follow the transmitter through its operations for a few dibits, referring to

Figure 14. The assumed starting conditions are (1) the phase register contains the number C = 00, and (2) the Channel B binaries have just been set to the corresponding phase. This, of course, means that Channel A is "on-line."

When the first data bit is sampled, it turns out to be a "1," and a D180 pulse is generated. This subtracts 10 from the 00 in the register, leaving 10, as shown. Next, the second bit is sampled, and since it is unlike the first bit, a D90 pulse is generated. This subtracts 01 from the 10 in the register, leaving C = 01.

At the end of the dibit, the 01 is transferred to the Channel A binaries. Consulting Figure 10 (reproduced at the right of Figure 14), we find that the resulting new Channel A phase leads the Channel B phase by the desired epoch angle, 135°. Note that at this time Channel B is "on-line"; the 135° epoch angle will not appear in the line signal until the channels switch again, at the time labeled "T."

As dibit #2 appears, it also produces a D180 and a D90 pulse, causing the indicated arithmetic operations in the phase register. At the end of the dibit, however, the EP pulse subtracts an additional 01, leaving C = 01 to be transferred to the Channel B binaries. As shown, this produces another epoch angle of 135°. For dibit #3, the only pulse produced is D180 (since the bits are alike) and the resulting epoch angle is 45°.

Completion of this chart for dibits 4, 5, and 6 is left to the reader. As a check, however, the register contents at the end of the dibit #6 are C = 11. Also, the epoch angles produced can be checked against Figure 2 to see that they correspond to the assumed data.

3. LINE SIGNAL SPECTRUM

As discussed earlier, the signal consists of a phase shifted carrier containing an integral number of quarter cycles of carrier per dibit. The reason for this restriction will be discussed later. For random data the waveform is non-periodic in time and cannot be analyzed simply. However, for repeated dibits, the signals become periodic and will produce line spectra. It will be shown that the frequencies of the lines produced will depend upon the dibit code and the number of quarter cycles of carrier per dibit. These factors will determine the tail-to-head or transition angle between successive dibits which in turn controls the spectrum of the phase shifted line signal.

As an example, consider the repeated dibit 11. For the 201A, each dibit interval contains 1 3/4 cycles of the 1750 cps carrier. The transmitter circuits add +45° to the initial phase angle of the 1750 cps carrier for each succeeding dibit on the line, producing an epoch angle of +45°. If it is assumed that this is done abruptly (rather than gradually, as is actually the case) the resulting line signal would appear as in Figure 15. This signal has a period of 8 ms or a fundamental frequency of 125 cps, a frequency too low to appear as a significant component in the spectrum. The transition angle for this example is either +135° or -225°. This corresponds to the angle between the tail of the previous dibit and the head of the present dibit and is illustrated in Figure 16. Averaged over a long period of time, this is equivalent to adding 3/8 cycle (or subtracting 5/8 cycle) of a 1750 cps waveform to the carrier frequency each millisecond. Expressed another way, the average frequency is shifted upward by an amount:

$$\text{upward shift} = \frac{3/8 \text{ cycle}}{1/1000 \text{ second}} = \frac{3000}{8} = 375 \text{ cps}$$

The shifted carrier becomes:

$$1750 + 375 = 2125 \text{ cps}$$

Since this happens at the dibit frequency of 1000 cps, there will be significant sideband components of 2125 - 1000 = 1125 cps and 2125 + 1000 = 3125 cps. The 3125 cps component is very weak and is usually ignored. Averaged over a long period of time, the 1750 cps carrier is suppressed as a result of this phase shift modulation. Therefore, the significant frequency components in the repeated 11 dibit are 1125 cps and 2125 cps. The same result can be obtained by counting the number of zero crossings for the phase-shifted signal in Figure 15. There are 34 zero crossings in 8 ms for an average frequency of:

$$\frac{34 \text{ zero crossings}}{.008 \text{ sec.}} \times \frac{1 \text{ cycle}}{2 \text{ zero crossings}} = 2125 \text{ cps}$$

In four-phase modulation, where the coding is restricted to odd multiples of 45° for the epoch angle, the choice of an integral number of 1/4 cycle of carrier per dibit will assure a transition angle which is also some odd multiple of 1/8 cycle (45°) of the carrier waveform. This means that for repeated dibits, the carrier frequency shift will be restricted to odd multiples of a unit amount designated Δf corresponding to 1/8

cycle of the carrier per dibit interval. The unit amount becomes:

$$f = \frac{1/8 \text{ cycle}}{1/\text{dibit freq. sec.}} = \frac{\text{dibit freq.}}{8} \text{ cps}$$

Figure 17 shows how the line spectra for repeated dibits of all four codes are developed for a choice of 1 3/4 cycles of carrier per dibit (for the 201A). Figure 18 is a summary of the line spectra for repeated dibits for the 201A and 201B data sets. The 201B uses 1 1/2 cycles per dibit and as a result, the line spectra differ for the two sets even though they use the same epoch angle coding. Figure 19 shows the line spectra for the X301B(m-10) data set which also uses 1 1/2 cycles of carrier per dibit. This set is a model shop version of a 4 phase set developed for use at 40,800 bits per second over broadband facilities. The result of the coding and carrier frequency restrictions noted above is a line signal spectrum which contains pairs of frequencies separated by exactly the dibit frequency regardless of the data input. This fact will be made use of in the receiver sync recovery circuits which are discussed later.

The shape of the spectrum for random data can be determined by analyzing four-phase modulation as two double sideband AM suppressed carrier channels operating in quadrature. A single DSAMSC (DSB) system corresponds to 200% AM and for binary digital data becomes a phase-reversal system. Two phase-reversal systems in quadrature become a fixed reference four-phase system. For example, refer to Figure 2 and note that the dibit pair 11 and 00 form one phase-reversal channel and the pair 10 and 01 form the second channel in phase quadrature to the first. Each channel becomes a suppressed carrier AM system operating at the dibit frequency and will exhibit a continuous frequency spectrum corresponding to the impulse response of the transmitter shaping circuits. With true raised cosine shaping the spectrum would have zeroes corresponding to the carrier frequency plus or minus a frequency F corresponding to 1/T where T is the dibit interval. For the 201A:

$$T = 1 \text{ ms (dibit interval)}$$

$$\text{and } F = \frac{1}{1 \text{ ms}} = 1000 \text{ cps}$$

Then the spectrum to the first zeroes will be 1750 - 1000 = 750 cps to 1750 + 1000 = 2750 cps. The envelope modulators in the 201A data sets use a modified raised cosine shaping with a more abrupt cutoff as illustrated in Figure

5. As a result, the actual spectrum for the 201A contains zeroes at 2850 cps and 650 cps. Figure 20 shows spectrum oscillographs for the 201A data set.

4. RECEIVER

The receiver has two main circuit functions: (1) data recovery and (2) sync recovery. An over-all block diagram of the 201A receiver is shown in Figure 21; the 201B is similar. After compromise equalization (optional), amplification, and AVC, the line signal is simultaneously presented to the data and sync recovery circuits. The operation of each will be discussed separately.

Data Recovery

As discussed earlier, data recovery depends upon the epoch phase angle between the present and the previous dibit. The present dibit is applied simultaneously to one input of each of two product modulators (or demodulators in this usage). The other input to one of the modulators is the previous dibit or 0° reference obtained through a 1 ms broadband delay line. The second input to the other product demodulator is the delay line output shifted -90° in phase. The product modulator with the -90° phase-shifted reference input recovers the first (A) bit of the dibit. The product modulator with the 0° reference input recovers the second (B) bit of the dibit. Data recovery of both bits is done simultaneously (in parallel) and the second bit is delayed in a shift register (B DATA REGISTER) by one bit interval before being transferred to the A DATA REGISTER which produces the output serial data. It is important to note that A and B as used here has nothing to do with Channel A and B in the transmitter.

Figure 22 shows the 201A Data Recovery Circuits in more detail. The line signal is amplified and stabilized in amplitude before being applied to the recovery circuits as the line signal input LSI. This signal is then delayed one dibit interval by delay line R4 and R5. The 201A and 201B delay lines are shown schematically in Figure 23. There are two outputs labeled 0° and -90°; these provide the reference or previous dibit signals for the two data recovery modulators on cards R6 and R8.

The action of a product modulator is illustrated in Figure 24 for the case involving two inputs of the same frequency, but differing in phase by an angle θ . The product modulator

output contains a double-frequency term and a DC term. The double-frequency component is filtered out and the DC term is used to set the state of a sample amplifier in four-phase demodulation. The polarity of the DC term is sensitive to the phase difference angle θ between the two inputs. This angle is related to the epoch angle and therefore, contains the dibit code to be recovered. Polarity can be positive or negative and thus is a binary term. As each dibit contains two binary terms or "bits", two channels are necessary in the receiver to recover the two bits in each dibit. Thus the need for an in-phase (0°) and a quadrature (-90°) product demodulator.

As an example, consider the recovery of the dibit 11 in the 201A four-phase receiver. At the transmitter the carrier phase was advanced $+45^\circ$ relative to its phase 1 ms earlier. We can write an expression to represent the previous dibit as

$$\text{previous dibit} = \cos [wt + \phi]$$

where ϕ is an arbitrary phase angle. Then the expression representing dibit 11 becomes

$$\text{dibit 11} = \cos [(wt + \phi) + 45^\circ].$$

Both signals are presented simultaneously to the input of the 0° product modulator. The DC term in the output becomes

$$\text{DC term} = 1/2 \cos 45^\circ$$

the output polarity then is positive.

The previous dibit signal at the input to the -90° product modulator is

$$\text{previous dibit (shifted } -90^\circ) = \cos [(\omega t + \phi) - 90^\circ].$$

Then the DC term in the output becomes

$$\text{DC term} = 1/2 \cos [45^\circ - (-90^\circ)] = 1/2 \cos 135^\circ.$$

The output polarity of the -90° channel is negative. This is illustrated with waveforms in Figure 25. Again, abrupt phase transitions are assumed for simplicity. The DC output of the -90° modulator will be negative for epoch phase angles between 0° and $+180^\circ$. The DC output of the 0° modulator will be positive for epoch angles between $\pm 90^\circ$. Figure 26 contains a summary of these results. Note that data recovery is independent of the number of carrier cycles per dibit.

Figure 27 shows the circuit details of the data sample amplifiers. There is one data sample amplifier for each of the two demodulators. The output signal from the demodulators is coupled

(balanced to ground) to the input of the data sample amplifiers through low-pass filters. These filters effectively eliminate the double frequency product output of the demodulators. The resultant voltage on the base of transistors Q2 and Q3 represents the DC term of Figure 26 according to the dibit being detected. The voltage difference between the bases of Q2 and Q3 represents the recovered data signal before regeneration and serves as a point to observe the received "eye pattern." At the proper instant in the received dibit (approximately the middle of the eye pattern) this voltage difference is a maximum and a gate pulse on the SMP lead causes either Q2 or Q3 to conduct.

This results in a code pulse on either pin 14 or 5 in two-rail logic representing the properly associated code for bit A (-90° Demod) and bit B (0° Demod). The A bit pulse sets the state of the A REGISTER whose output appears as the Received Data or RD on the interface. The code pulse for the B bit is delayed one-half a dibit interval in the B REGISTER before a readout pulse transfers it to the A REGISTER as the second bit of the bit pair. The output data is then in serial form for use by the customer. At this point the RD signal has been re-timed and shaped so that it is essentially distortion-free.

Sync Recovery

Operation of the receiver logic and data sample circuits depends on an accurate clock signal. This clock signal can be extracted from the sidebands associated with each dibit code in the modulation spectrum. In the special case of repeated dibits, as shown in Figures 17-19, each dibit code generates a line spectrum pair with a constant separation corresponding to the dibit frequency. A detailed analysis can be used to show that these spectra pairs at the transmitter are also invariant in phase. Thus, by proper recovery technique, sync can be made available for all code combinations.

Figure 28 shows how this is accomplished. The frequencies shown are for the 201A data set and repeated dibits. The amplified and stabilized line signal is applied simultaneously to a pair of high and low pass band splitting filters which cut-off at the nominal carrier frequency. Since each dibit code contains a prominent frequency above and below the carrier frequency these are now separated and applied simultaneously to the two inputs of a balanced product demodulator.

The difference frequency output of the product demodulator is the separation frequency. As shown in Figure 28, this is the dibit frequency. This frequency is selected from the other modulation products by sharply tuned band pass filters. The recovered dibit frequency is shaped to provide clock and timing signals for the receiver circuits and it also is made available after conversion to bit frequency as SCR or Serial Clock Receive.

The stability of the sync recovery circuit is affected by delay distortion and to some extent amplitude distortion at the edges of the signal spectrum. Repeated dibit codes which produce a weak or delayed outer sideband; e.g., dibit 00 or 01 for the 201A, produce excessive jitter in the recovered sync signal and can cause data errors. For this reason, four-phase data sets are designed to "idle" with a code combination which produces a favorable line spectrum. This code is repeated dibit 11 for the 201A and 201B data sets.

5. INTERFACE

All voltages and impedances meet or exceed the minimums of the Electronic Industries Association Standard RS232. Positive and negative polarities of the order of six volts are used. A negative polarity represents a mark, one or off; a positive polarity represents a space, zero, or on. The connections between the data set and the business machine equipment are established by means of a 25 pin connector. The socket on the data set is a Cinch or Cannon receptacle per DB-19604-433. The business machine equipment should have a cable equipped with a cinch or Cannon plugger DB-19604-432 plus a DB-51226-1 hood (Cinch only) or the equivalent. Circuit terminations are as follows:

1. Frame Ground
2. Send Data
3. Receive Data
4. Send Request
5. Clear to Send
6. Interlock
7. Signal Ground
8. Carrier On-Off
9. + Power (For Testing)
10. - Power (For Testing)
11. Not Used
12. Not Used
13. Not Used

14. New Sync
15. Serial Clock Transmit or External Timing Input
16. Dibit Clock Transmit (not useable in set with external timing)
17. Serial Clock Receive
18. Dibit Clock Receive
19. Remote Release
20. Remote Control
21. Ready
22. Ring Indicator 1
23. Ring Indicator 2
24. External timing input (see note 2)
25. Not Used

Transmitter

The transmitter interface has six connections which connect the transmitter to the customers' equipment.

Interlock (IT)

This connection provides a positive 6 volt potential at all times during which the data set is prepared to send or receive data. A zero potential indicates that the set is not in an operating condition.

Request to Send (RS)

This connection is under the control of the customer's business machine. To send data, the customer applies a positive potential to this terminal and holds it during transmission. The Positive going transition of the RS lead should be made coincident with the Positive going transition of the D C T. When the customer has completed his transmission, he must apply a negative potential. When using two-wire operation this also transfers the set from the transmitting condition to the receiving condition. See Dibit Clock (Transmitter) (DCT). When the customer has completed his transmission, he must apply a negative potential. When using two-wire operation this also transfers the set from the transmitting condition to the receiving condition.

Clear to Send (CTS)

This terminal provides a negative potential at all times during which the set is activated but not in the transmitting state. A positive potential will appear at this terminal about 150 milliseconds after application of a positive potential at the RS terminal. This delay allows

sufficient time for line echo suppressor actuation and for the distant receiver to establish synchronization. In special cases (see note below) the delay may be reduced (by removing an internal strap) to about 8-1/2 milliseconds.

The CTS terminal will continue the positive potential until the RS terminal potential is made negative. A negative potential will then appear at the CTS terminal. Transmission of carrier will continue for 2 milliseconds. This allows data in the transmitter to be cleared before reverting to the transmitter "off" condition and enabling the receiver. *The business machine equipment should use the next positive transition of the SCT after the Clear to Send indication to gate in the first data bit.*

When the Data Set 201A is used on 2-wire lines, the set will be strapped for the "Echo Delay" option and for the 150 millisecond delay between the Request to Send Signal and the Clear to Send Signal. The Echo Delay option keeps the receiver turned off for about 100 milliseconds after the transmitter is turned off to permit echoes on the line to decay before the receiver is enabled.

Note 1: In special cases where very short 2-wire lines are used (hence no echo suppressors present and echoes not troublesome) both of the above options can be strapped out where fast turnaround time is desired.

Serial Clock (Transmitter) (SCT)

A square wave signal from the transmitter timing circuits appears on this terminal. This signal is to be used by the customer to synchronize his data with the transmitter timing. The customer must provide data bits at or about the time of the positive transition of this signal. Data is sampled by the data set for transmission at or near the negative transition of this signal. This lead is used to accept external timing from the business machine when the externally-timed version of the set is used. It is planned for the future (late 1963) to produce data sets that will be capable of operating as internally timed or externally timed sets by means of wiring options in the set. In these sets there will be two separate SCT pins assigned in the interface connector - one for the internally timed mode and the other for the externally timed mode of operation.

Note 2: Pin 15 and 24 is connected together in 201A's and 201B's manufactured subsequent to October 1962. Sets with this strapping can be recognized by the designation J1D201A-1 L1 --- B- or J1D201B-1 L1 --- B- stamped in ink on the underside of the data set. Earlier sets are designated J1D201A-1 L1, --- or J1D201B-1 L1 --- and have no electrical connection to pin 24. The reason for strapping is so that business machine manufacturers can start using the new external timing input (pin 24) now in anticipation of the future data sets as mentioned under SCT above.

When external timing sets are used, the customer must provide data bits at or about the time of the positive transition of his timing signal. Data is sampled by the data set at or near the negative transition of his timing signal. *The accuracy of the timing signal provided by the customer's business machine must be .01%. It should be a square wave with a duty cycle of $50\% \pm 1/2\%$.*

A high impedance input circuit is used on the SCT lead where external timing is accepted by the set from the customer's business machine. This permits up to about eight externally-timed sets to be "driven" from the timing of a single internally-timed set where this arrangement is desired by the customer. The business machine will also be bridged across this circuit and it should not load the circuit down excessively. If the impedance of the business machine timing input circuit is, say, 7,000 ohms or greater, excessive loading will not result.

Dibit Clock (Transmitter) (DCT)

The square wave signal on this terminal may be used by the customer for synchronization at the dibit rate if so desired. If the shortest delay is desired in the CTS circuit, the positive going polarity change on the RS terminal must be coincident with the positive going polarity change of this signal. The delay will then be $8-1/2 \pm 1/4$ milliseconds. This signal is not available for use on the externally-timed sets.

Send Data (SD)

The customer applies the data to be trans-

mitted to the SD terminal. A positive polarity at this terminal represents the binary "0" while a negative polarity represents the binary "1".

Receiver

The receiver interface has seven connections which connect the receiver to the customers' machine. These are described below.

Carrier On (CO)

The potential on this terminal will be negative when no carrier is present. The customer will receive a polarity change (negative to positive) on this terminal within 9 milliseconds of the time that carrier signal appears at the receiver input.

Serial Clock (Receiver) (SCR)

This square wave signal is similar to the SCT signal but is synchronized with the receiver timing circuits. Data bits are presented synchronously with the positive transitions of this signal and should be sampled by the customer at or near the negative transition.

Dibit Clock (Receiver) (DCR)

This square wave signal is similar to the DCT signal but is synchronized with the receiver timing. It may also be used for synchronization.

Received Data (RD)

The customer receives transmitted data from this terminal. Again a positive polarity indicates a binary 0, a negative polarity a binary 1.

New Sync (NS)

This terminal is provided to the customer for use for multiparty operation, so that he may effect a more rapid transition in synchronization between messages. A positive 1 millisecond pulse applied to the NS terminal at the end of a message will quench the existing synch signal. This allows the synchronization circuits to pick up within 8-1/2 milliseconds from a new transmitter for the next message. At all other times the voltage must be negative, and supplied from a low impedance source. If a customer does not wish to use this feature, internal strapping is provided to bypass it.

Ring Indicator 1 (RG1), Ring Indicator 2 (RG2)

These leads are connected together inside the data set during each ring when automatic

answering is used. The business machine equipment can make use of this feature to delay the automatic answer until ready to receive data. (See below)

Remote Release (RR), Remote Control (RC), Ready (RDY)

The business machine must close the Ready lead to the Remote Release lead to have unattended answering of "dialed-up" calls. If the loop is left open, the telephone will have to be answered manually in the usual way. Also, the business machine must normally close the Remote Release lead to the Remote Control lead and should open it momentarily (at least 150 milliseconds) only to end a telephone call made using automatic answering.

RC and RR leads must be permanently strapped in the business machine if Remote Release is not required; otherwise data set will not lock in data mode.

Grounds

In addition to these terminals, Data Ground (DG) and frame Ground (G) terminals are provided at the interface, and they are permanently connected together inside the data set power supply. The frame ground also is connected to the green third wire of the power cord. The customer must furnish a three-wire outlet to the data set location from the same AC service cabinet which serves the business machine equipment so that the same ground bus is used for both. This measure is necessary to prevent impulse noise potentials which might otherwise develop and cause data errors. Impulse noise measured between business machine ground and the data set ground should not exceed 1 volt peak of either polarity as measured on an oscilloscope with a bandwidth of a least 1 megacycle.

Test Switch

An external switch has been designed to connect the modulator of the 201A to the demodulator for local tests when used on 4-wire circuits. This permits the business machine to send to itself through the local data set. This arrangement will aid in isolating troubles. The switch terminates the telephone line and is intended to be connected so that when operated to the test position, it grounds the IT lead and thereby indicates to the business machine equipment that the data set is not conditioned to send data on the line.

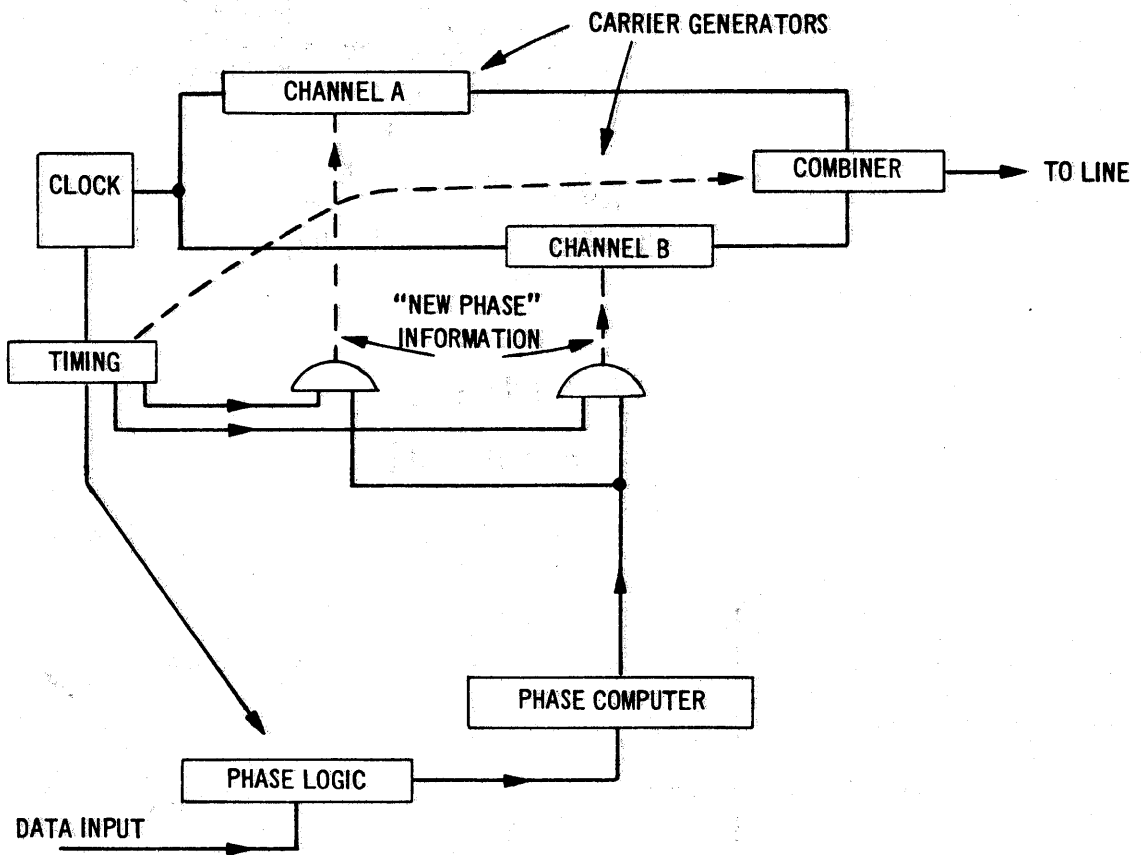


FIGURE 1
BLOCK DIAGRAM OF TRANSMITTER

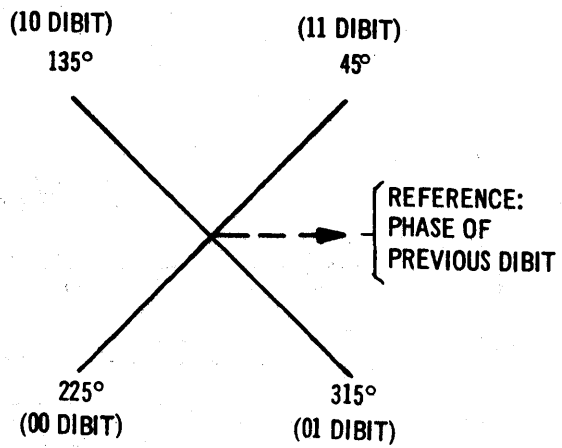
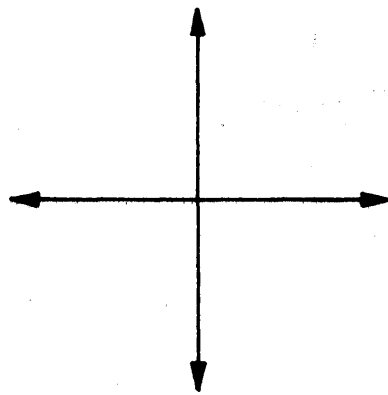
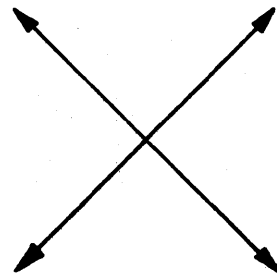


FIGURE 2
EPOCH ANGLES



PHASES OF CHANNEL A



PHASES OF CHANNEL B

FIGURE 3
EIGHT POSSIBLE CARRIER PHASES

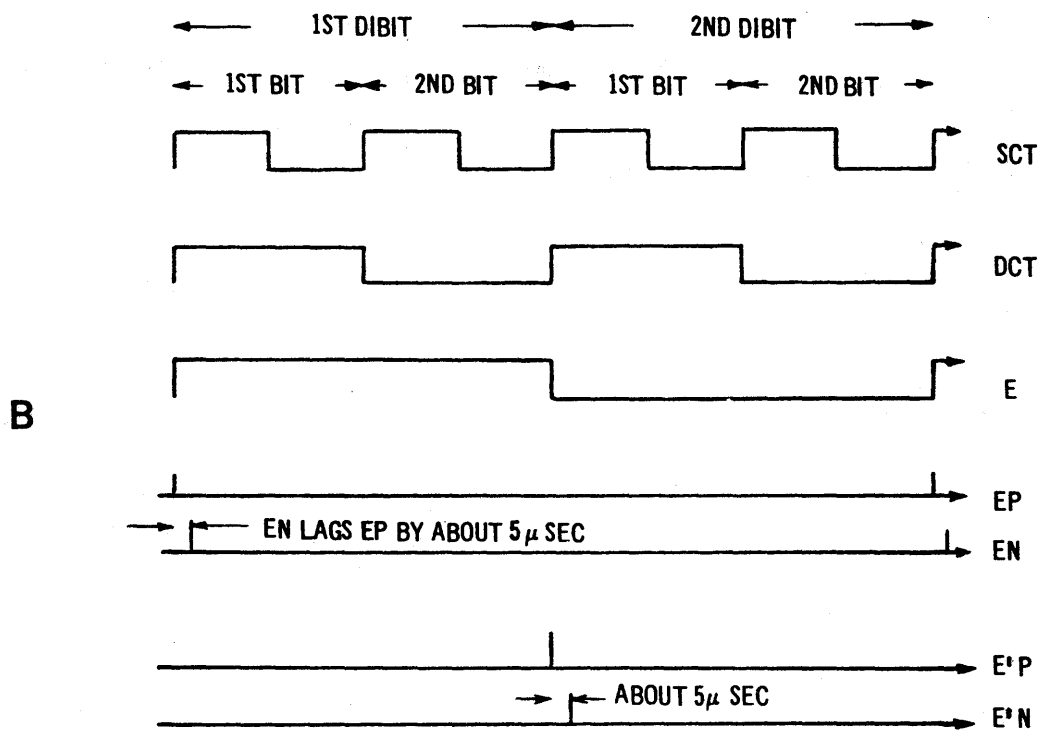
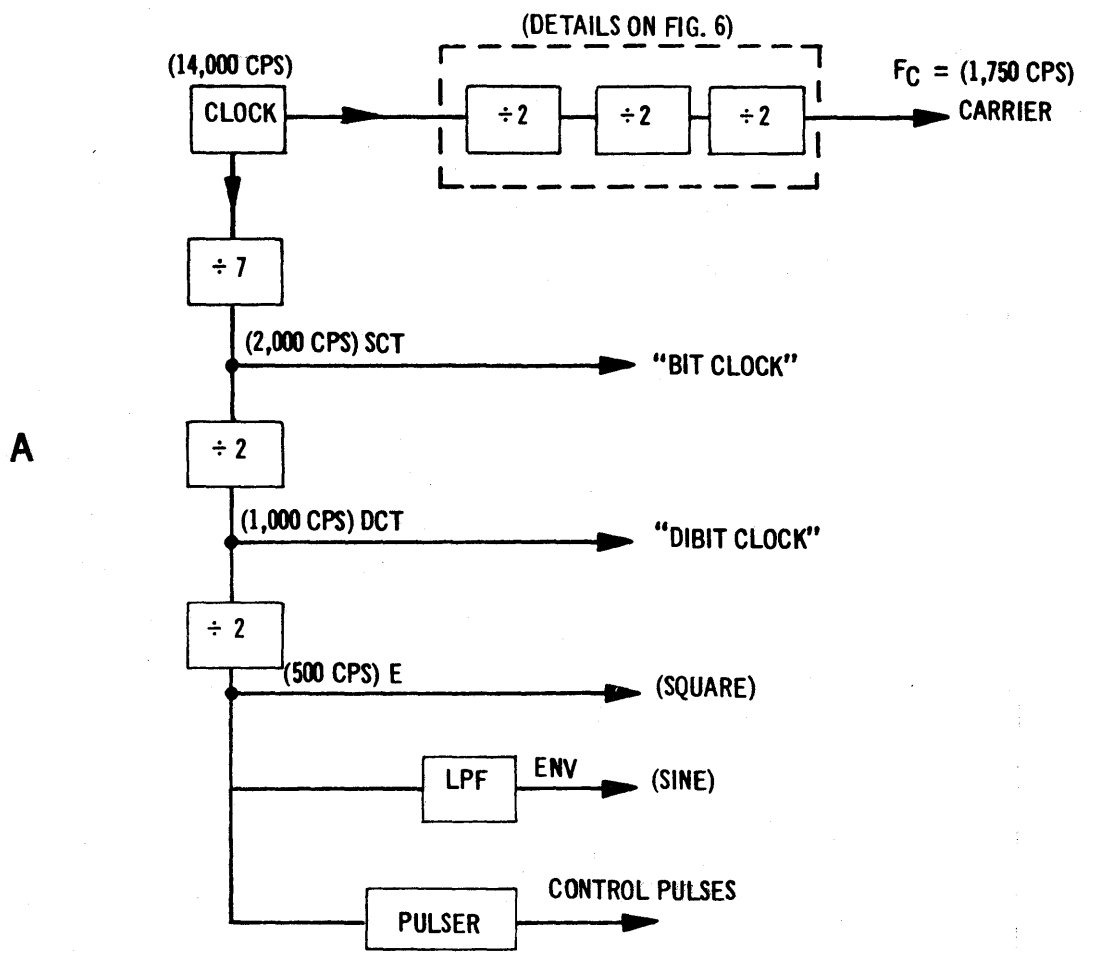


FIGURE 4
TIMING SIGNALS

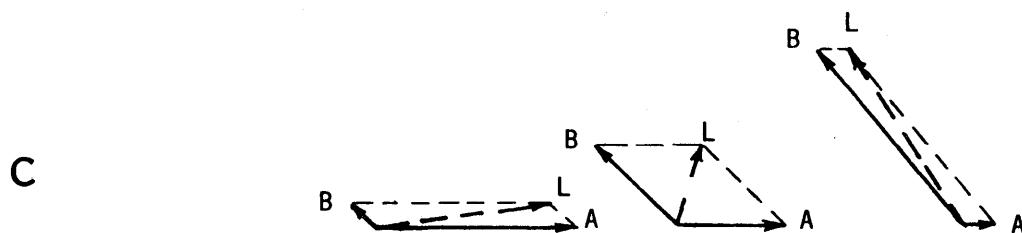
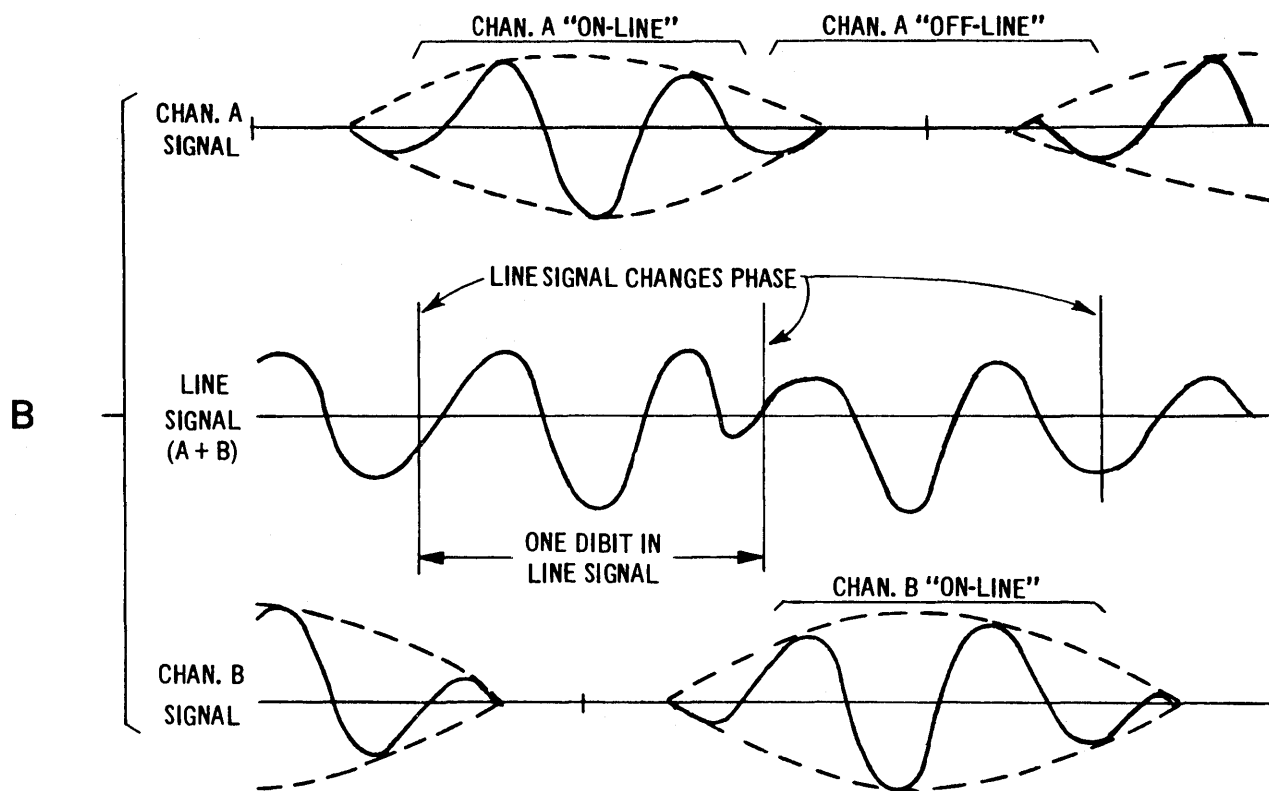
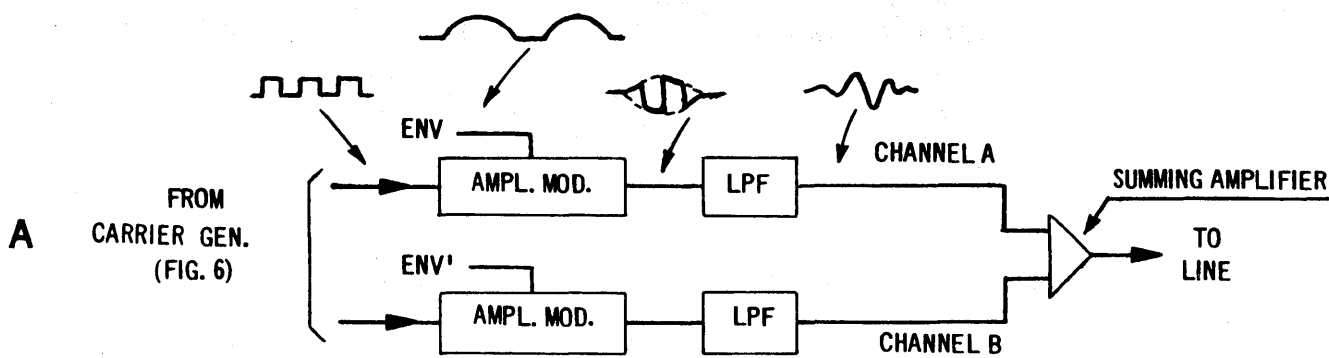


FIGURE 5
PRODUCTION OF LINE SIGNAL

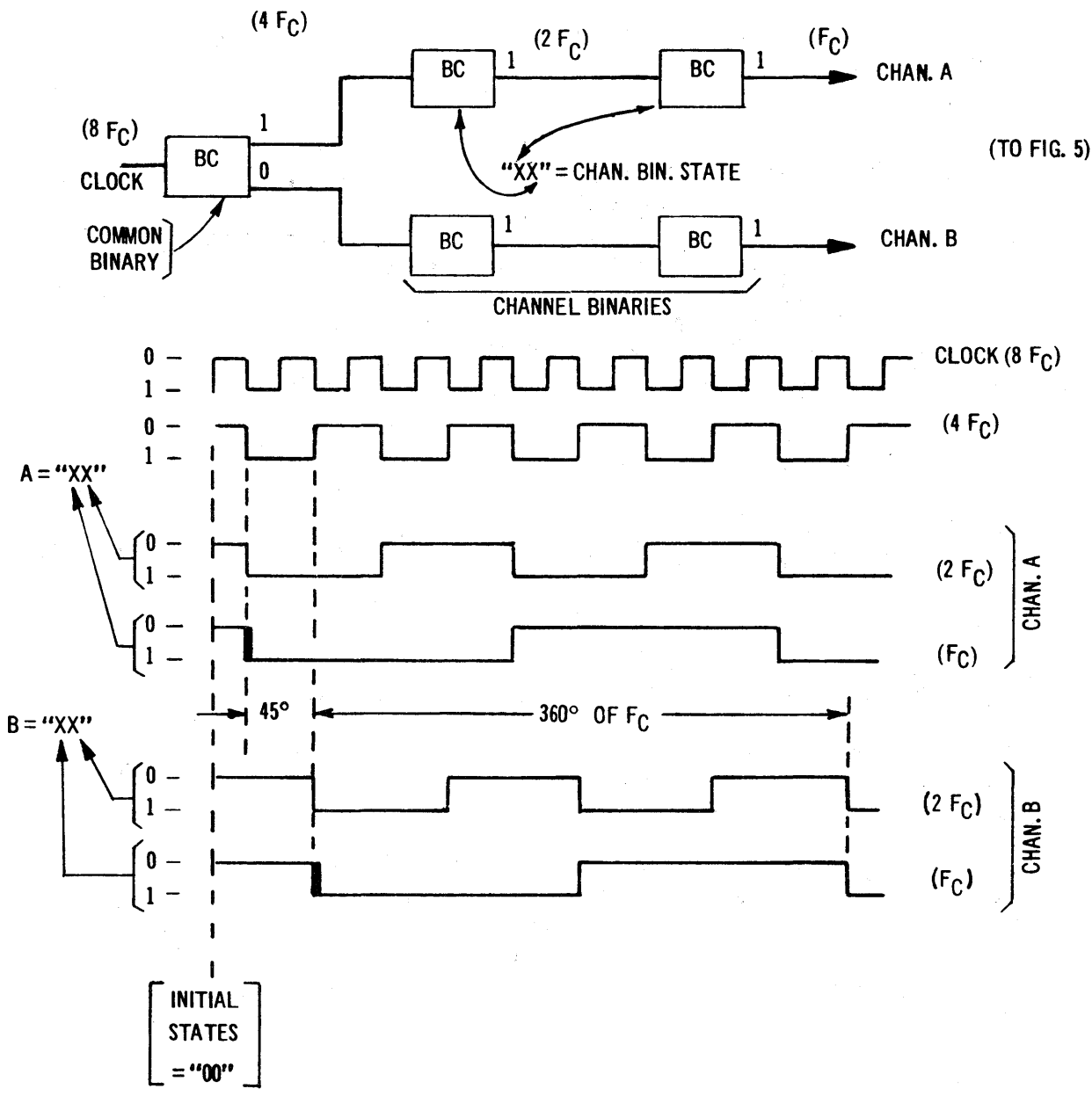


FIGURE 6
45° DIFFERENCE BETWEEN
CHANNELS A & B

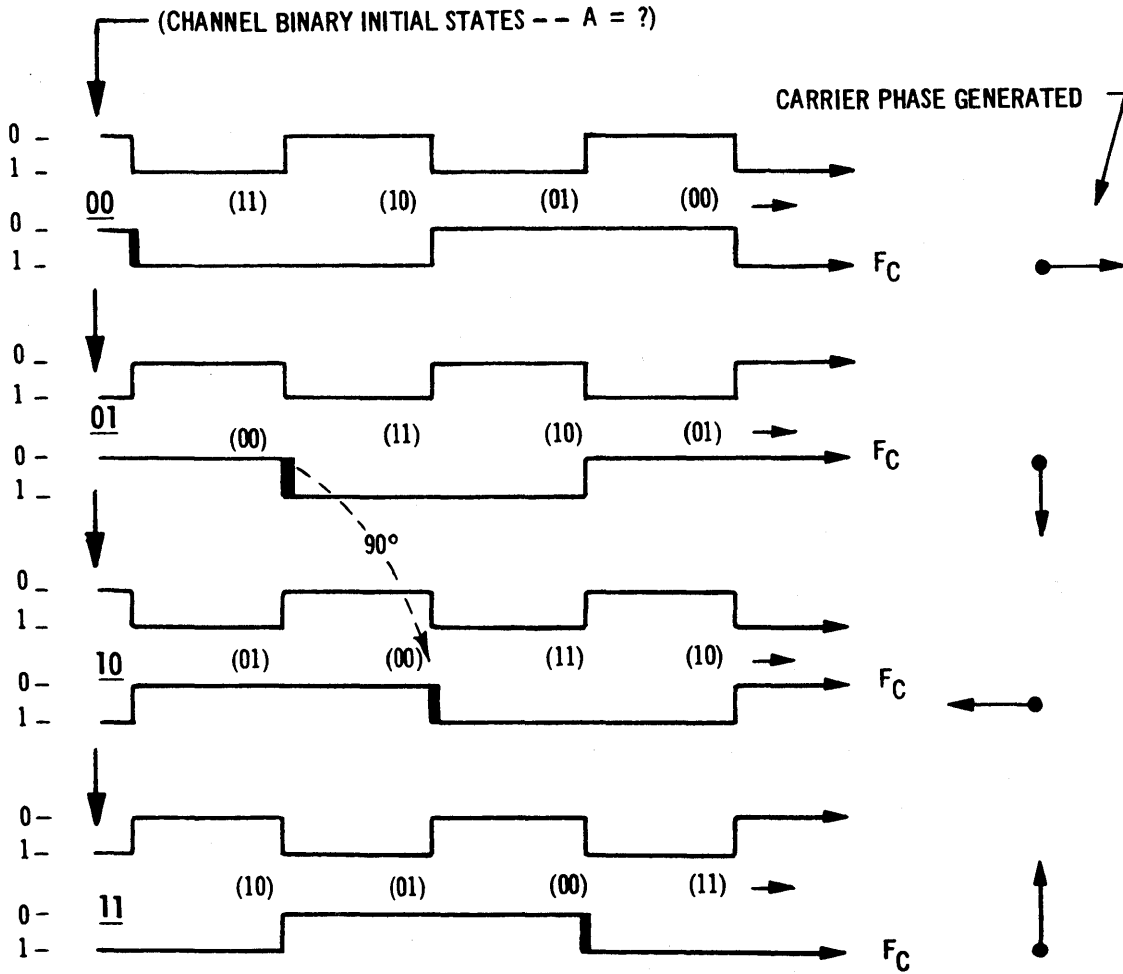
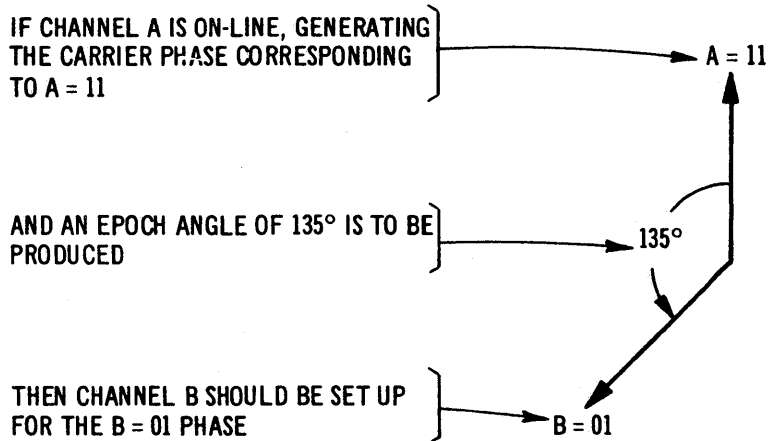
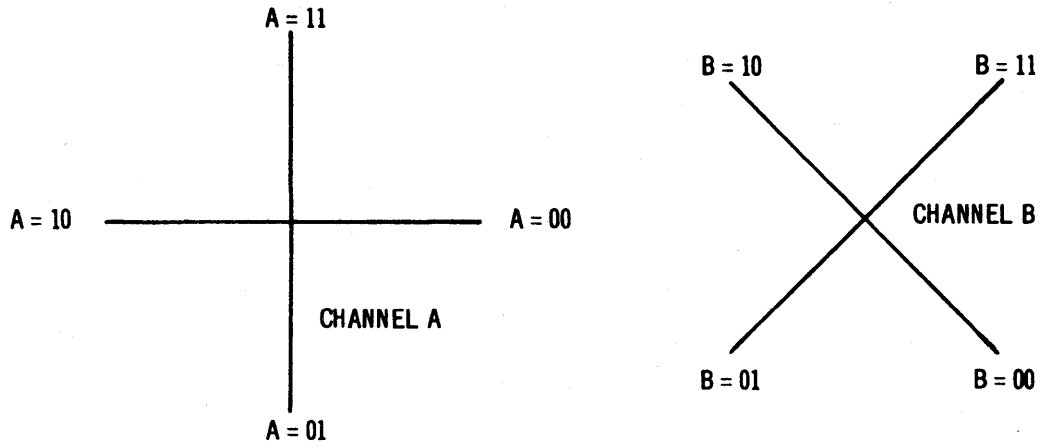


FIGURE 7
CARRIER PHASE VS. CHANNEL BINARY
INITIAL CONDITIONS

A



B

FIGURE 8
CARRIER PHASE VS CHANNEL BINARY INITIAL CONDITIONS

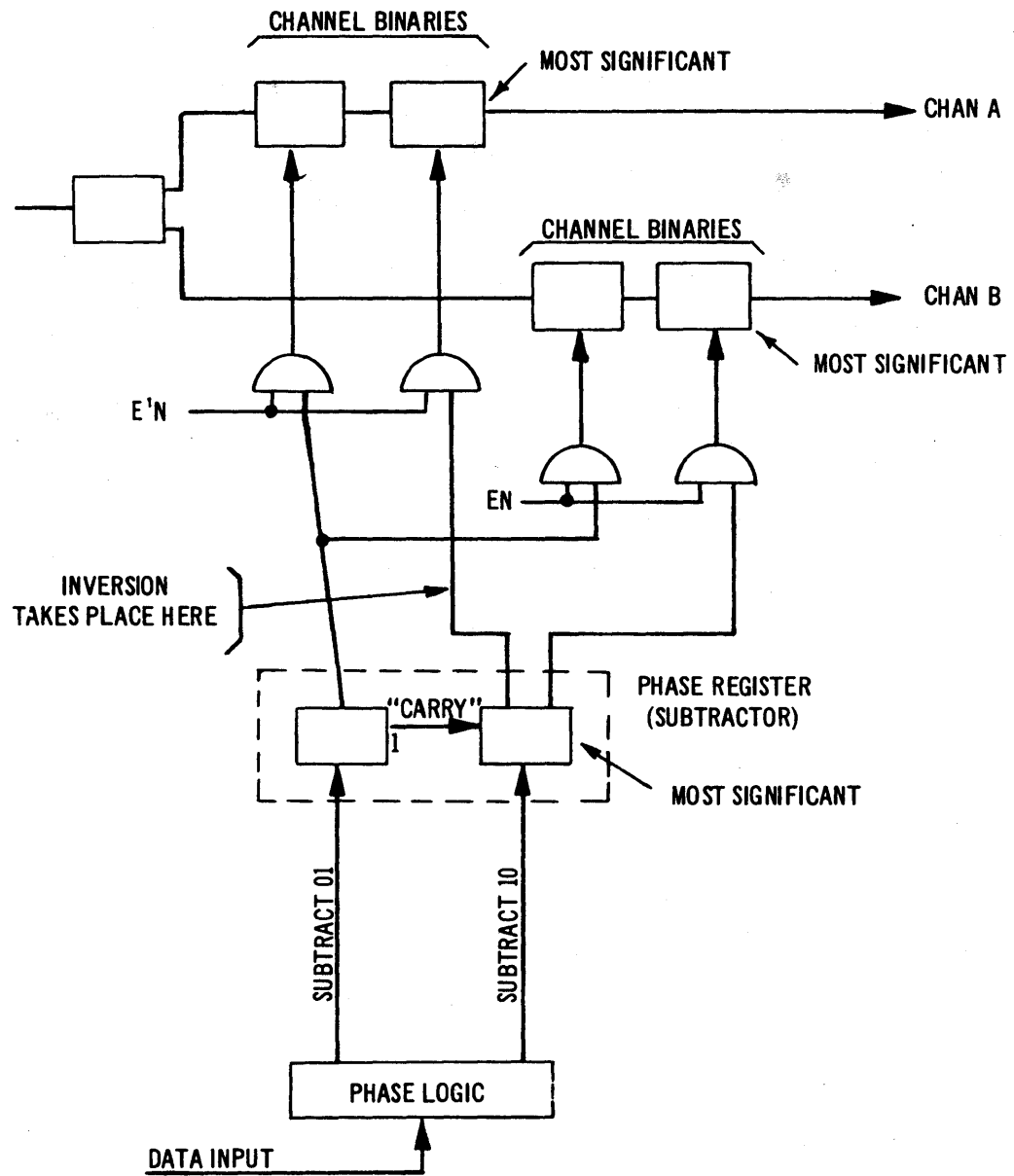


FIGURE 9
OPERATION OF PHASE REGISTER

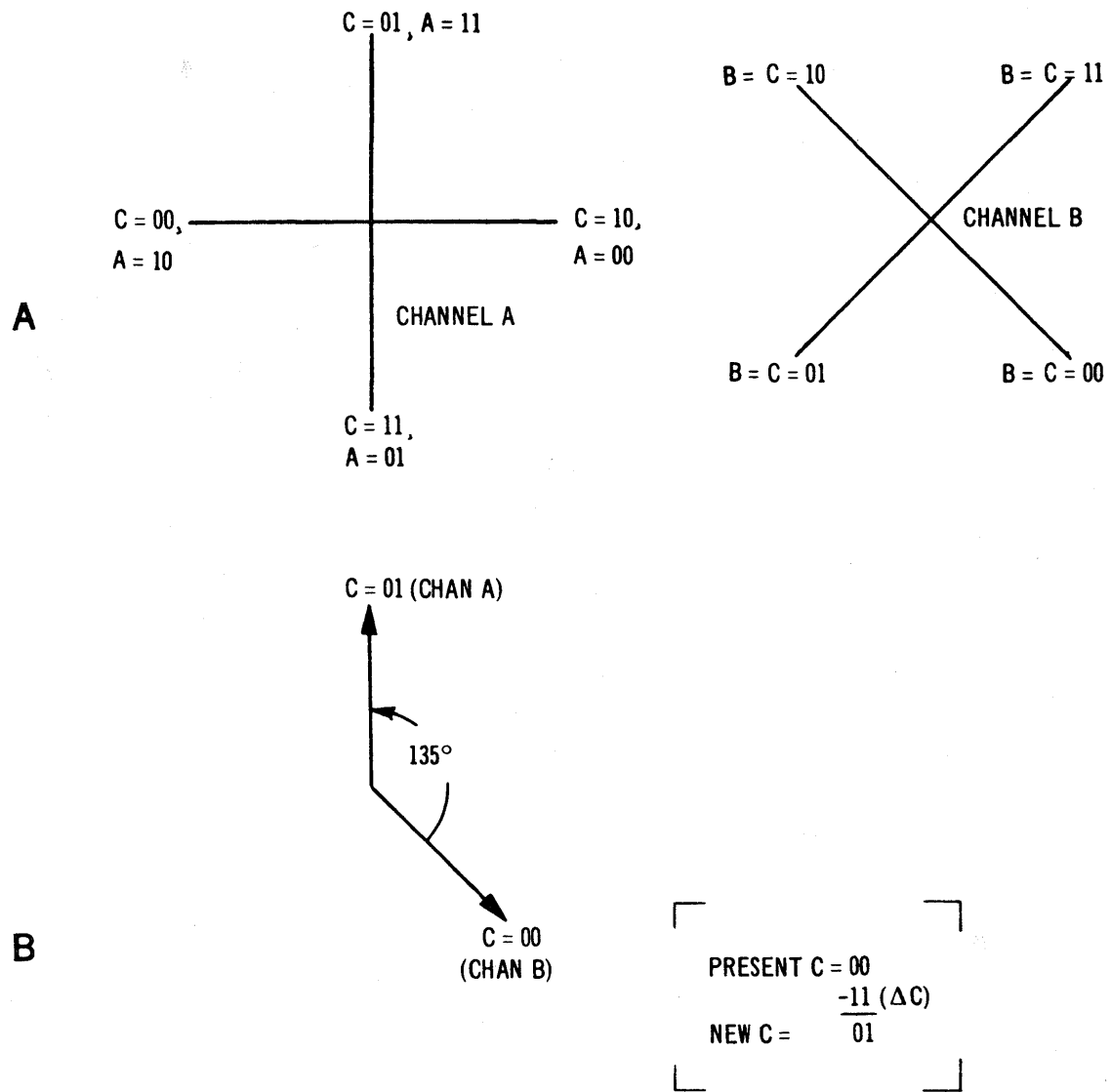
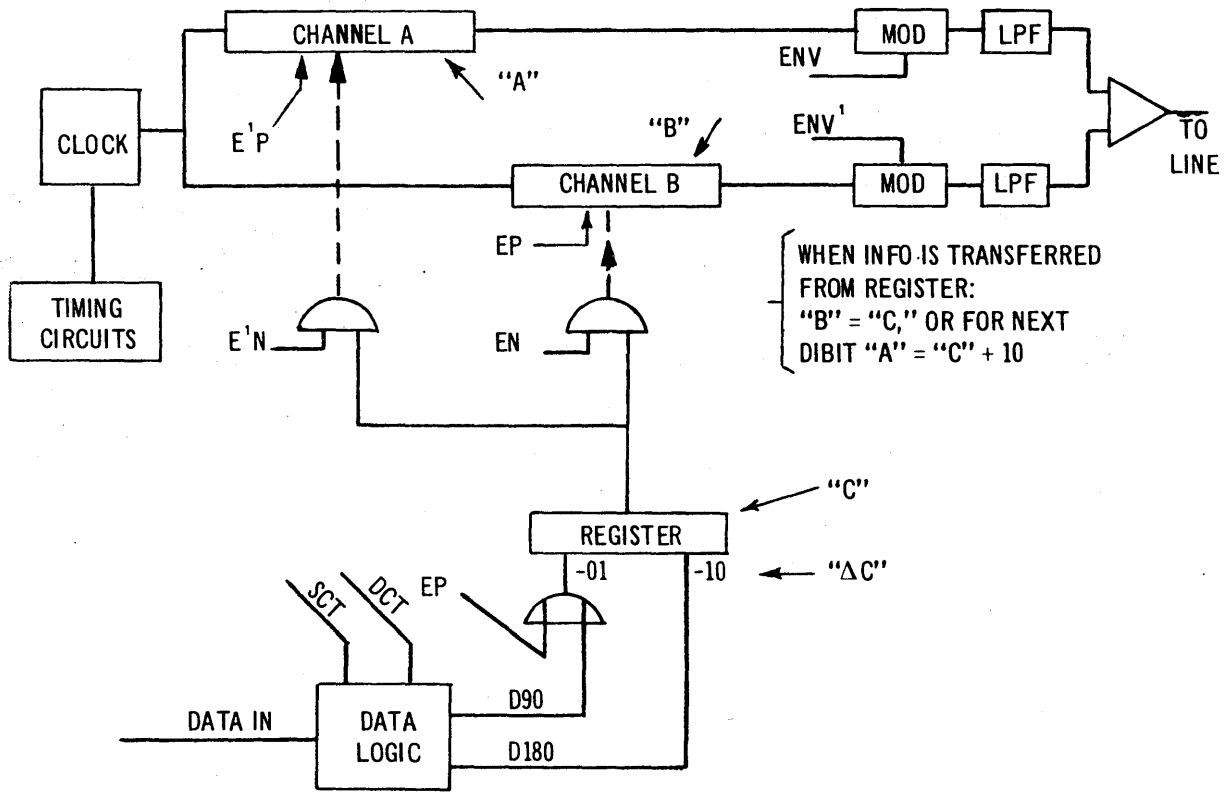


FIGURE 10
CARRIER PHASE VS. REGISTER CONTENTS

		ΔC SUMMARY			
		11	10	00	01
EPOCH ANGLE:		45°	135°	225°	315°
CHANNEL B ON-LINE, SETTING UP CHAN A	}	10	11	00	01
CHANNEL A ON-LINE, SETTING UP CHAN B	}	11	00	01	10
THE DIFFERENCE IS CONSTANT --- = 01	}	11 $\frac{-10}{01}$	00 $\frac{-11}{01}$	01 $\frac{-00}{01}$	10 $\frac{-01}{01}$

FIGURE 11
SUMMARY OF REQUIRED "ΔC" PULSES



CODE CONVERSION:

DIBIT CODE		EPOCH ANGLE	PHASE CODE	
1ST	2ND		D180	D90
1	1	45°	1	0
1	0	135°	1	1
0	0	225°	0	0
0	1	315°	0	1

FIGURE 12
 BLOCK DIAGRAM OF TRANSMITTER

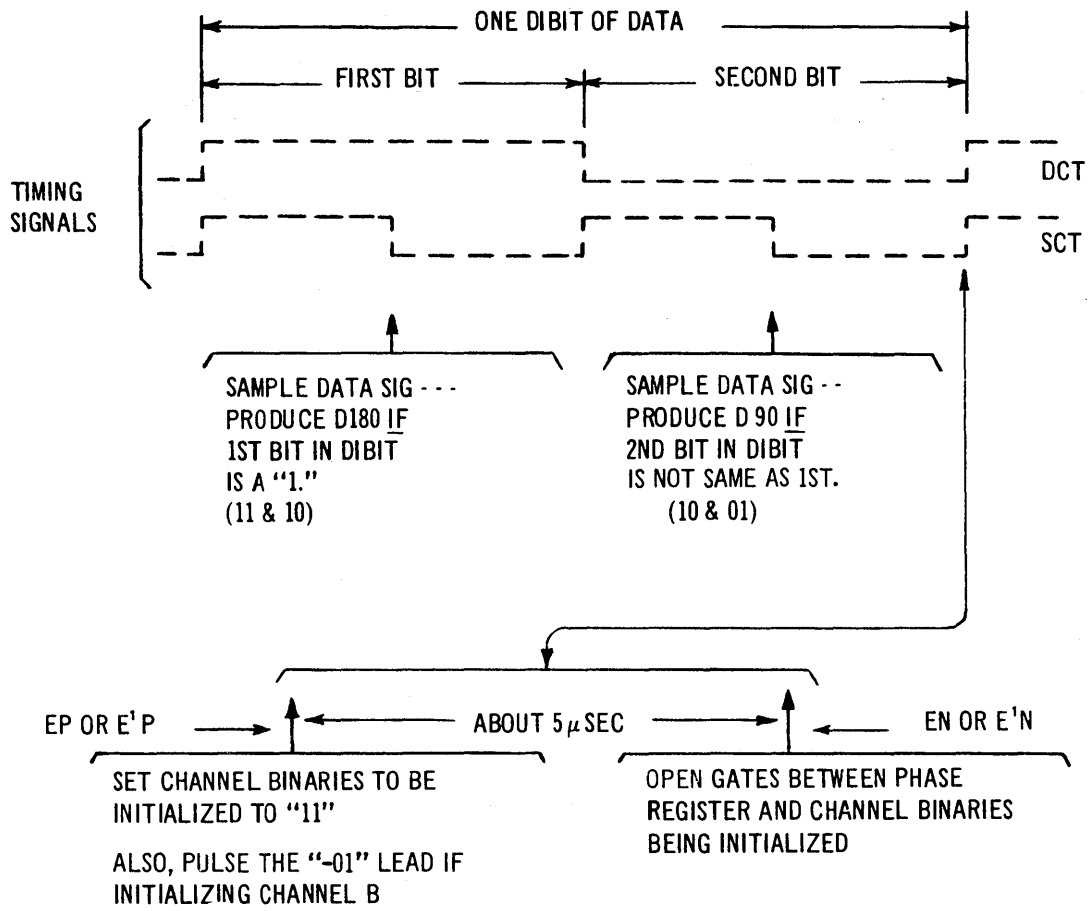
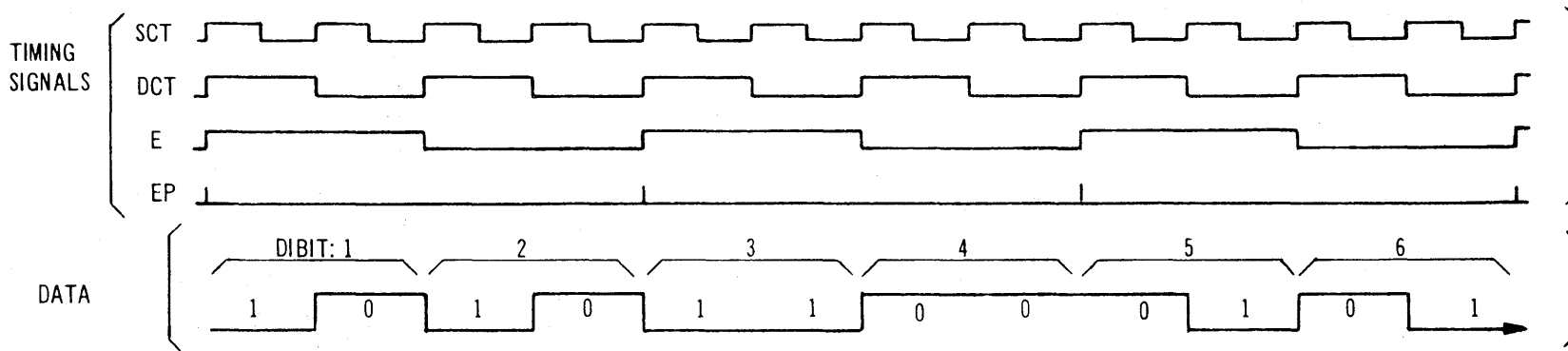


FIGURE 13
TIMING CHART



PHASE REGISTER -
CONTENTS &
ARITHMETIC
OPERATIONS

00
-10 (D180)
10
-01 (D90)
01

01
-10 (D180)
11
-01 (D90)
10
-01 (EP)
01

01
-10 (D180)
11

--

--

11

RULES:

D180 --
1ST BIT = 1
D90 --
1ST ≠ 2ND
EP ---

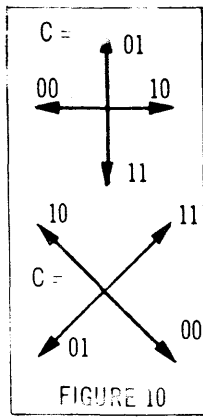
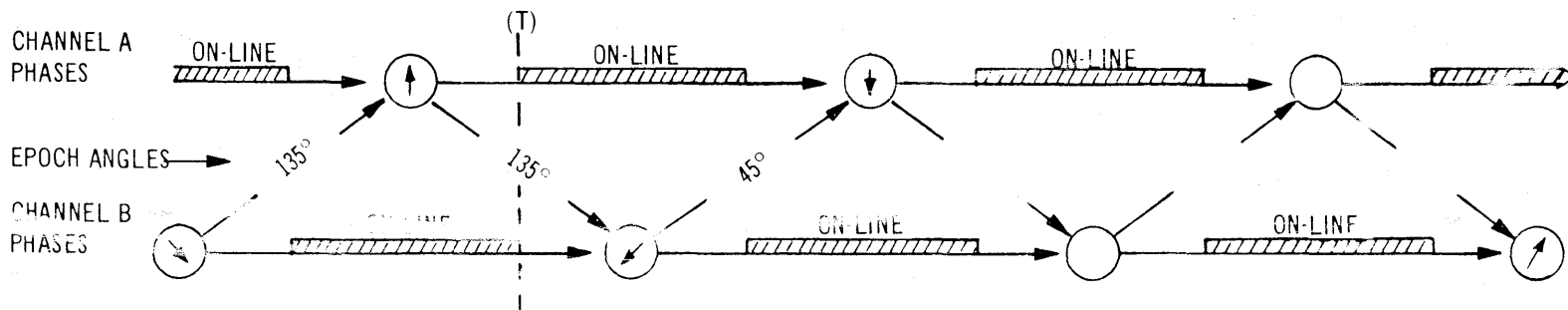


FIGURE 14
SEQUENCE CHART
201A DATA SET

201A DATA SET REPEATED 11 DIBITS

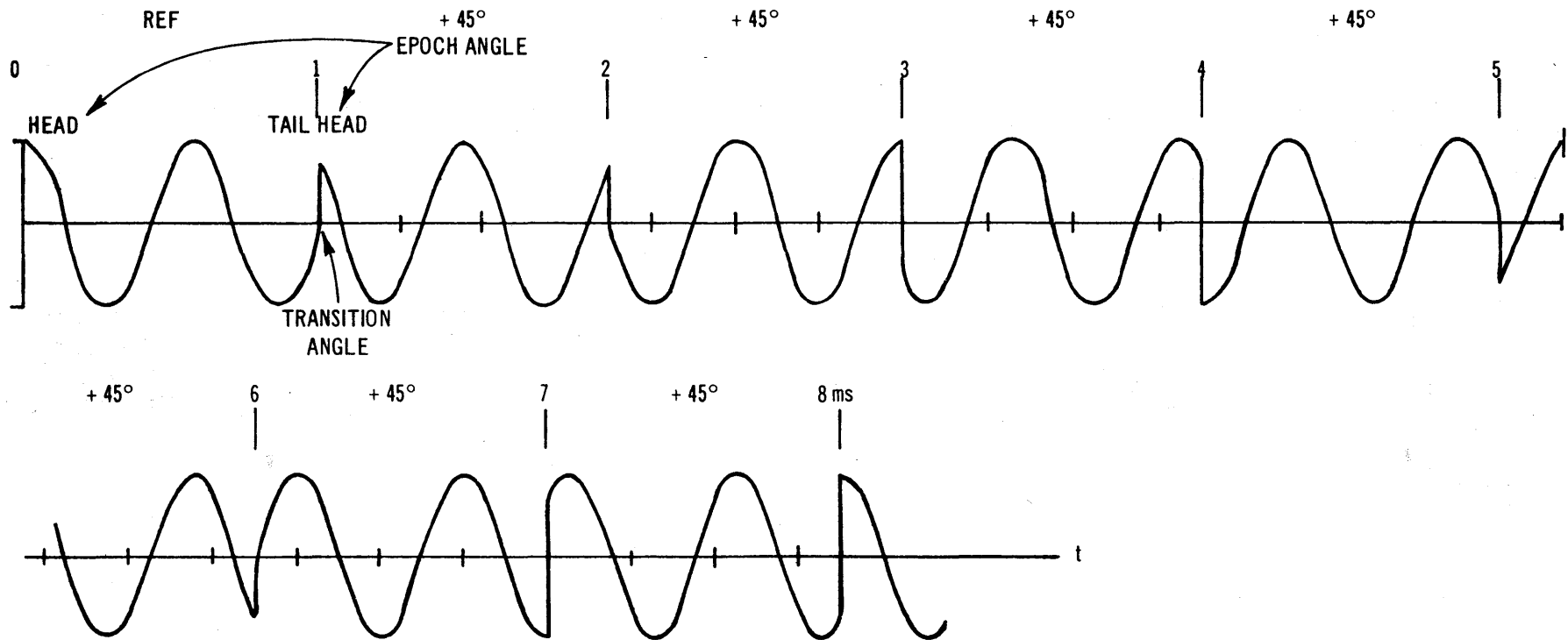


FIGURE 15

SIMPLIFIED LINE SIGNAL FOR REPEATED DIBITS

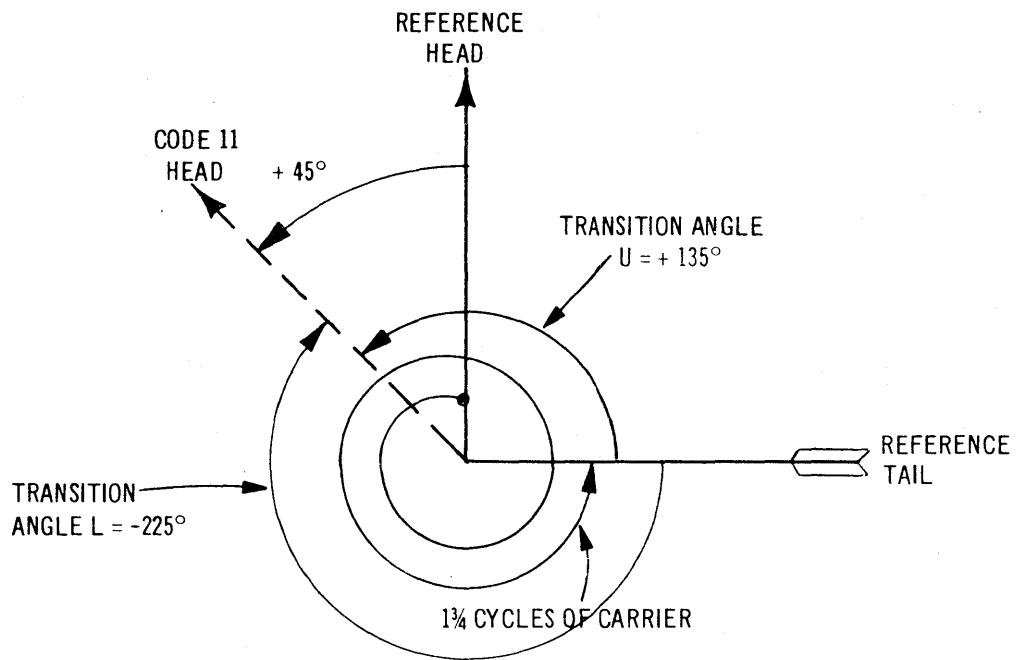
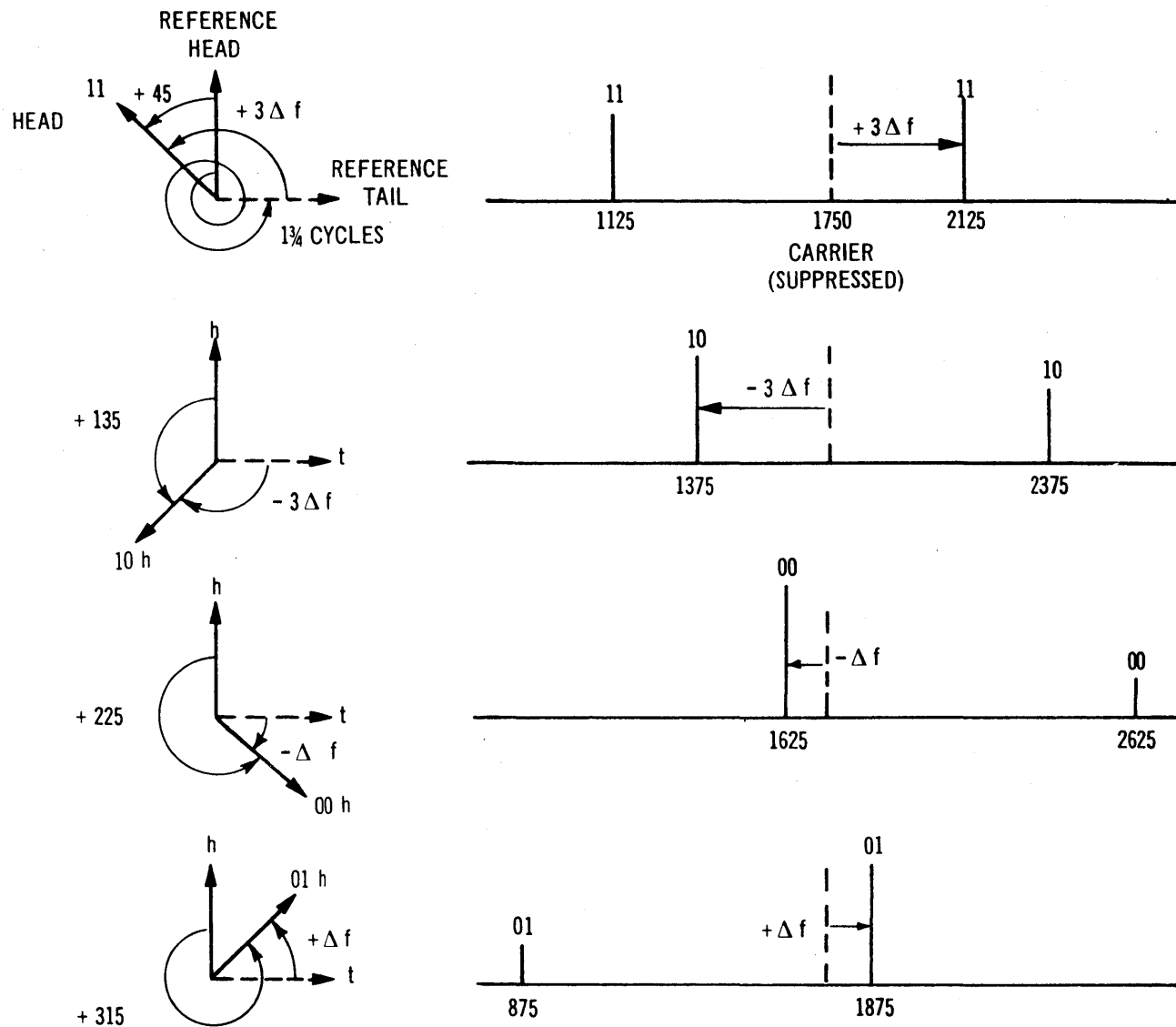


FIGURE 16
DETERMINING TRANSITION ANGLE

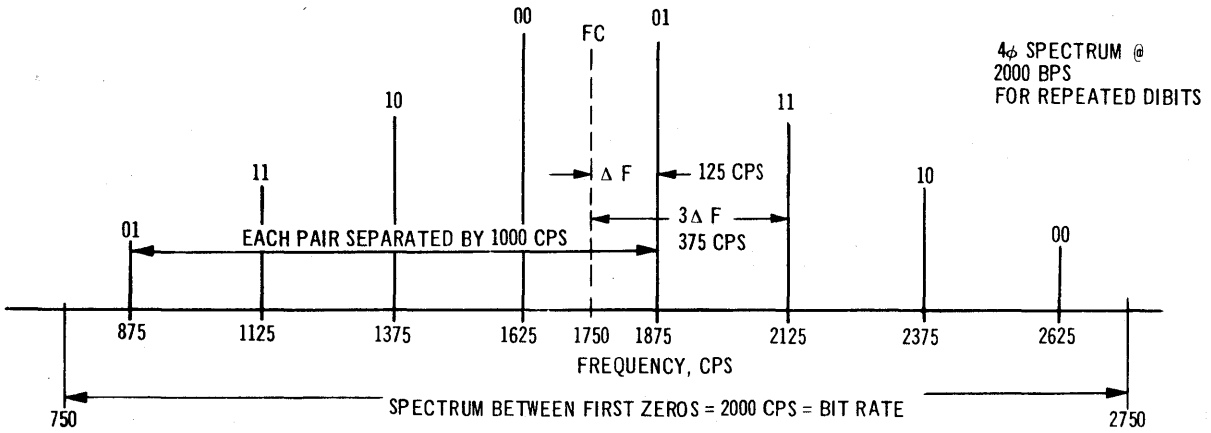
LINE SIGNAL SPECTRA DEPENDS ON TAIL-TO-HEAD ANGLES
 THESE DEPEND ON THE NUMBER OF CARRIER CYCLES/DIBIT

LINE SPECTRA FOR 2000 BPS AND 1¼ CYCLES/DIBIT



$$\Delta f = \frac{\text{DIBIT FREQ.}}{8} = \frac{1000 \text{ CPS}}{8} = 125 \text{ CPS}$$

FIGURE 17



$$\Delta F = \frac{\text{DIBIT RATE, CPS}}{8}$$

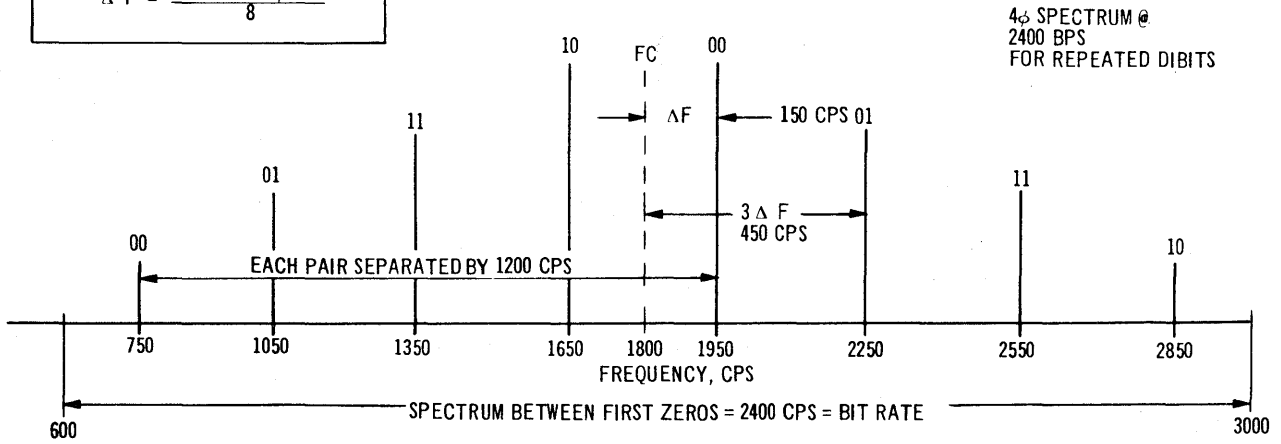


FIGURE 18

$$\Delta F = \frac{\text{DIBIT RATE, KCPS}}{8}$$

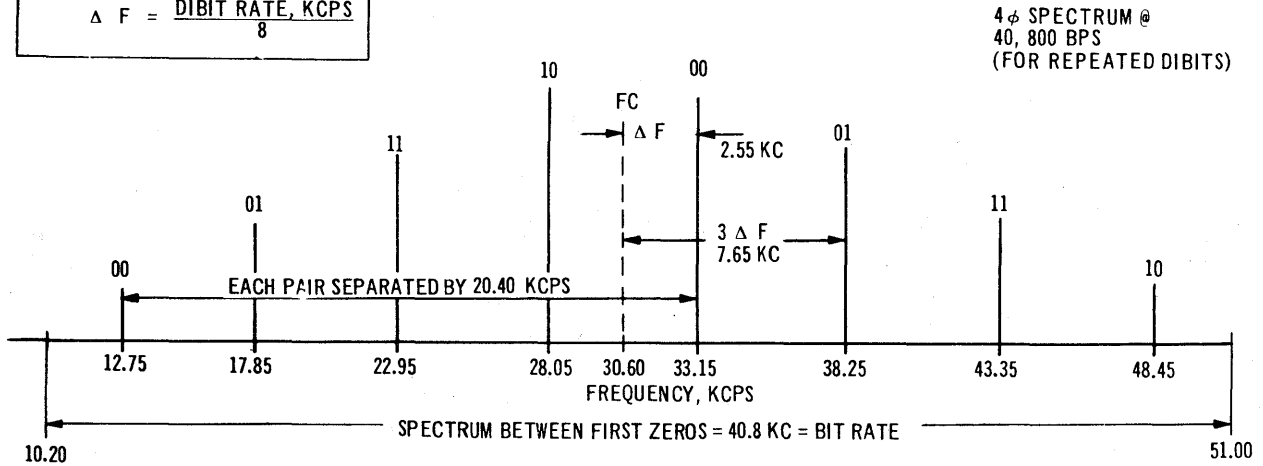
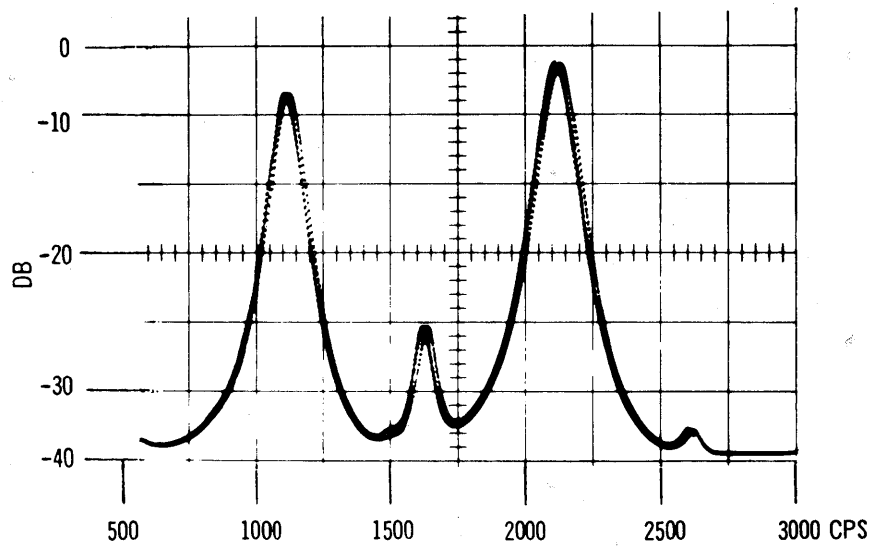
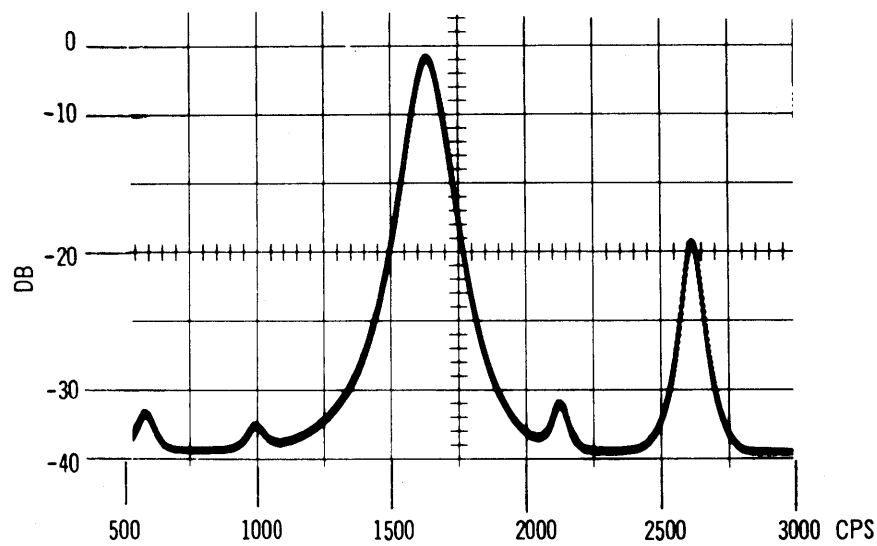


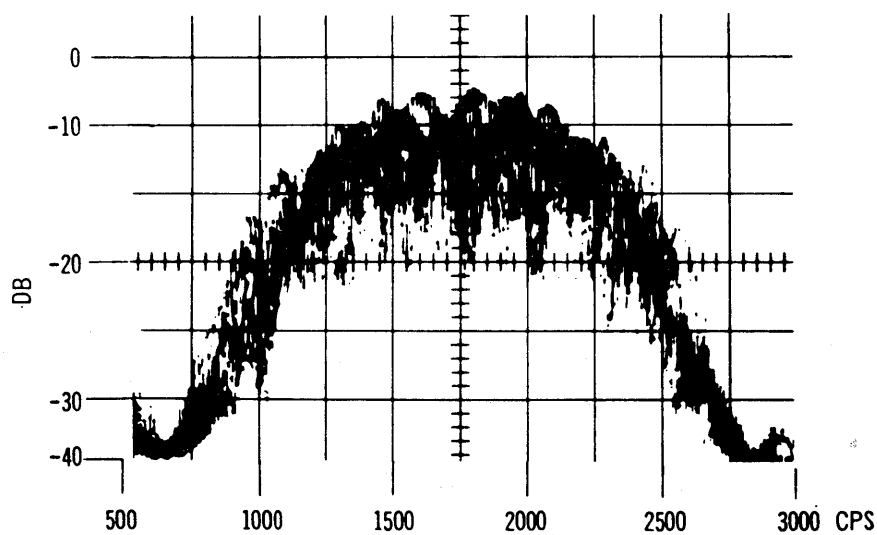
FIGURE 19



REPEATED 11 DIBITS



REPEATED 00 DIBITS



63 BIT RANDOM WORD

FIGURE 20

SPECTRUM ANALYSIS OF 201A DATA SET SIGNAL

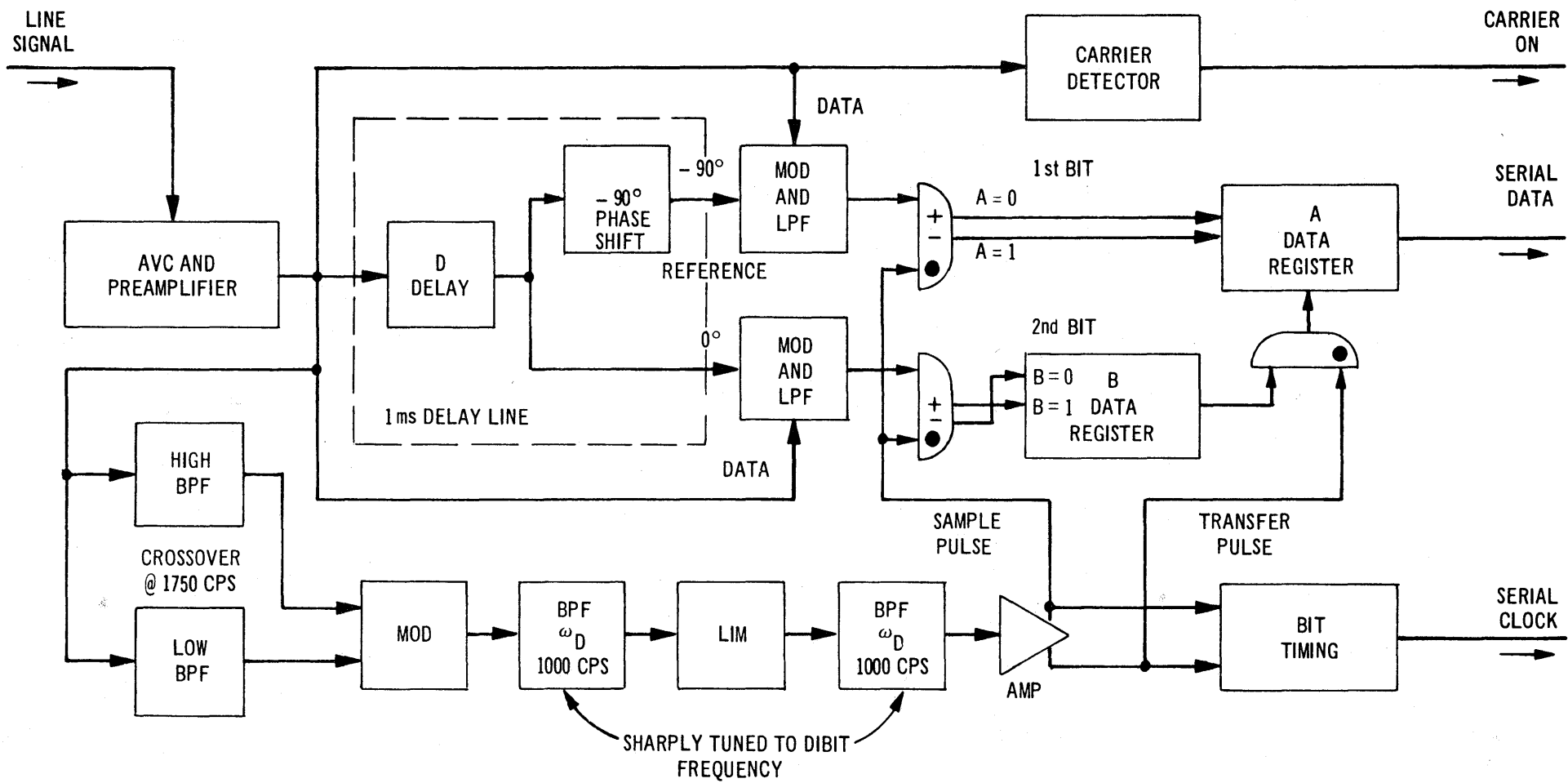


FIGURE 21
201A RECEIVER BLOCK DIAGRAM

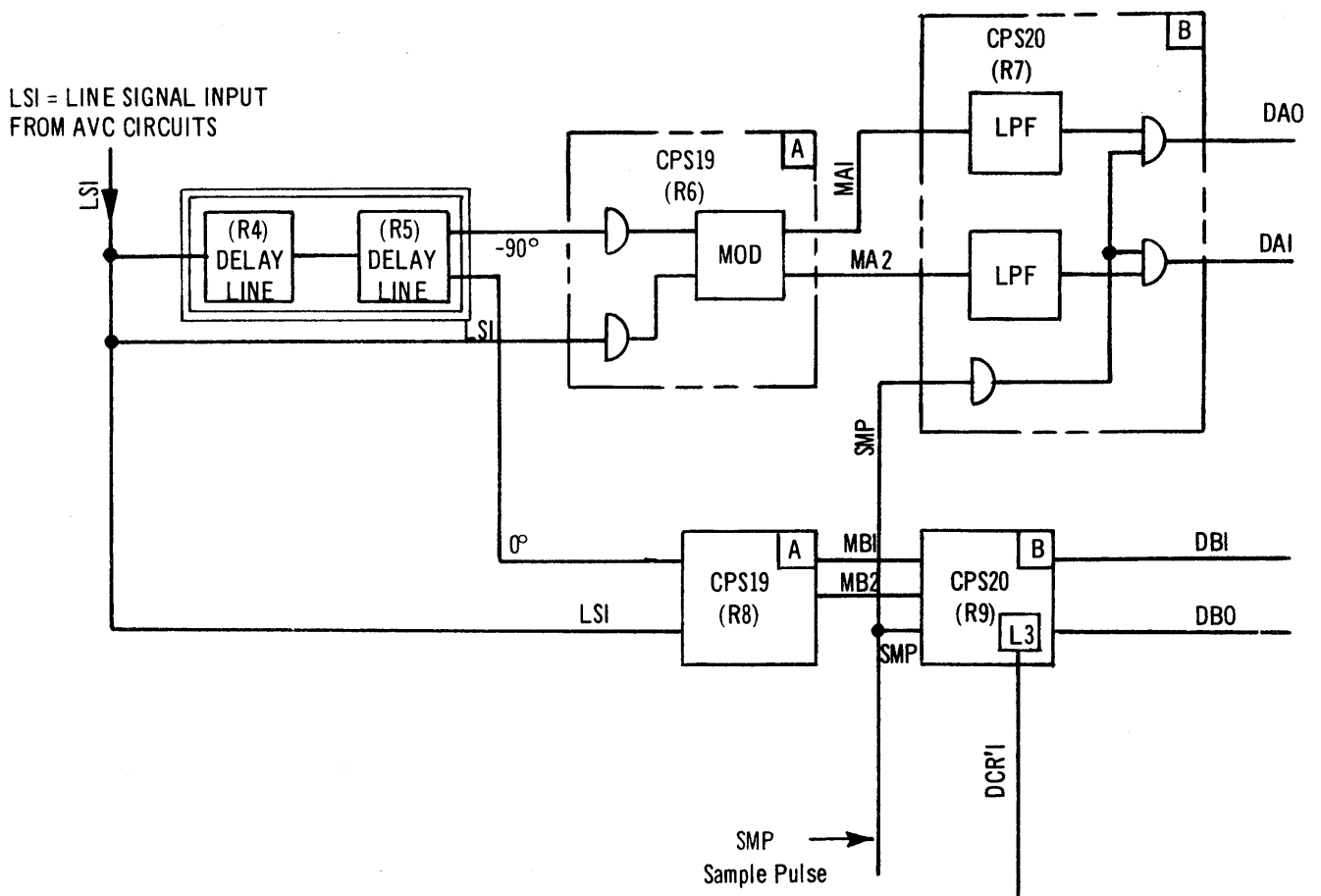


FIGURE 22
201A DATA RECOVERY CIRCUITS

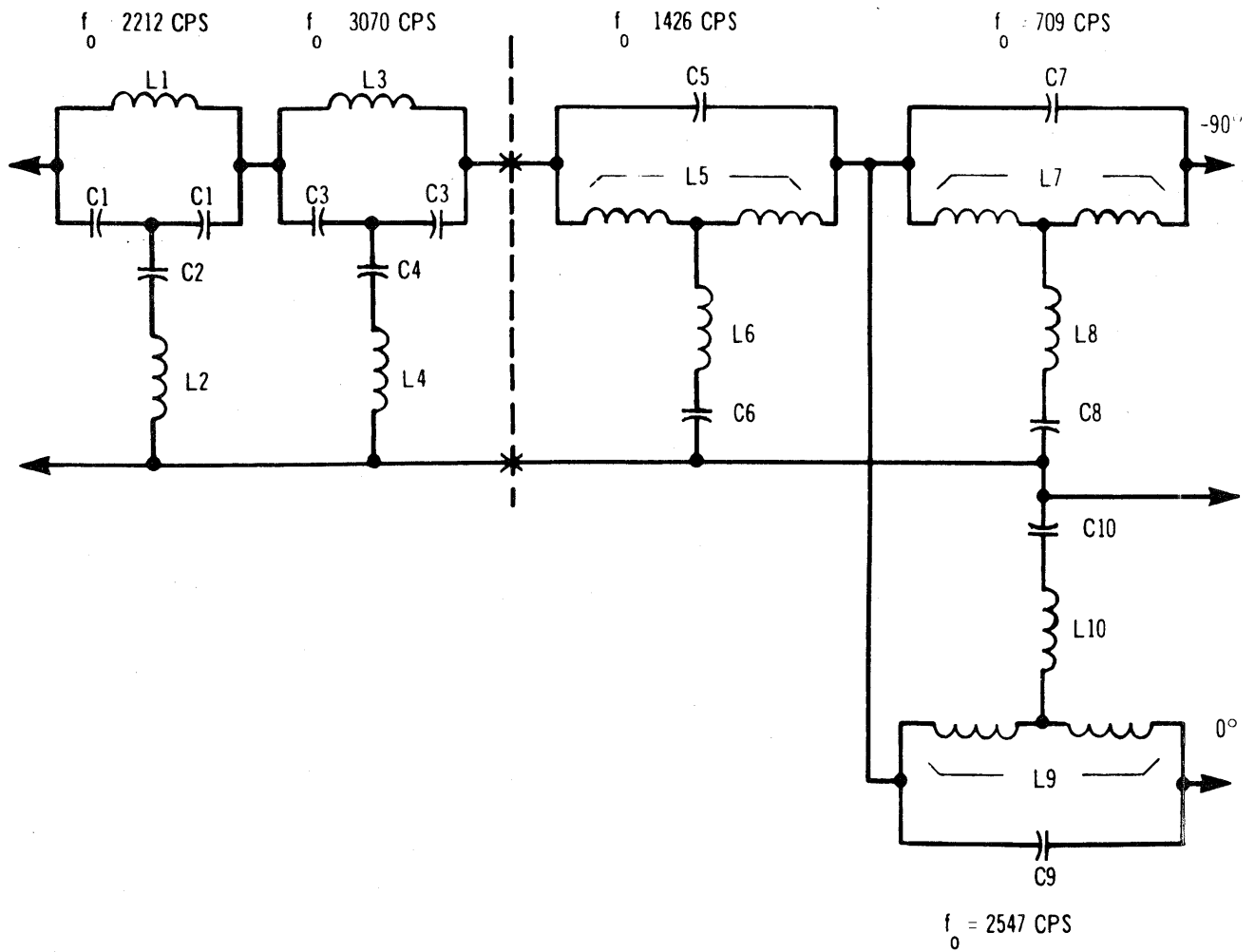


FIGURE 23
SKETCH OF R4 & R5 CIRCUIT 844A & 844B DELAY LINE
 201A 201B

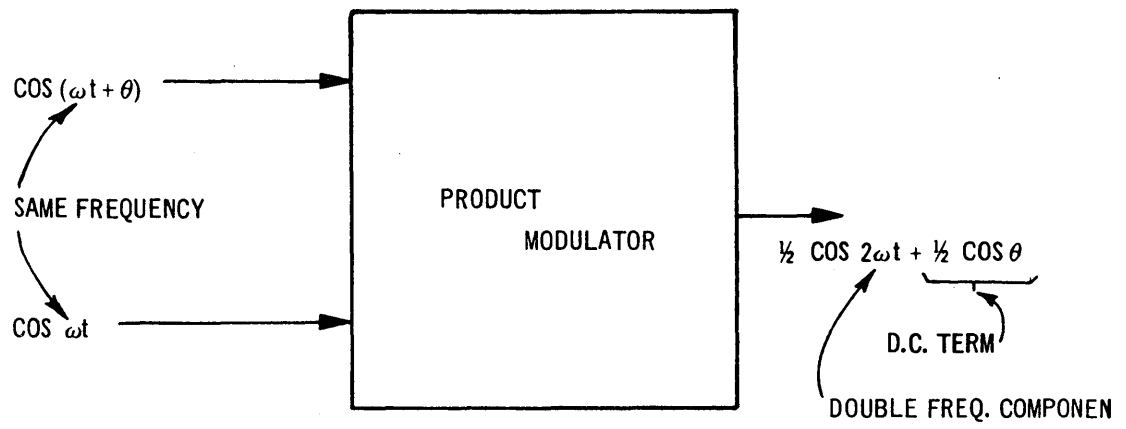
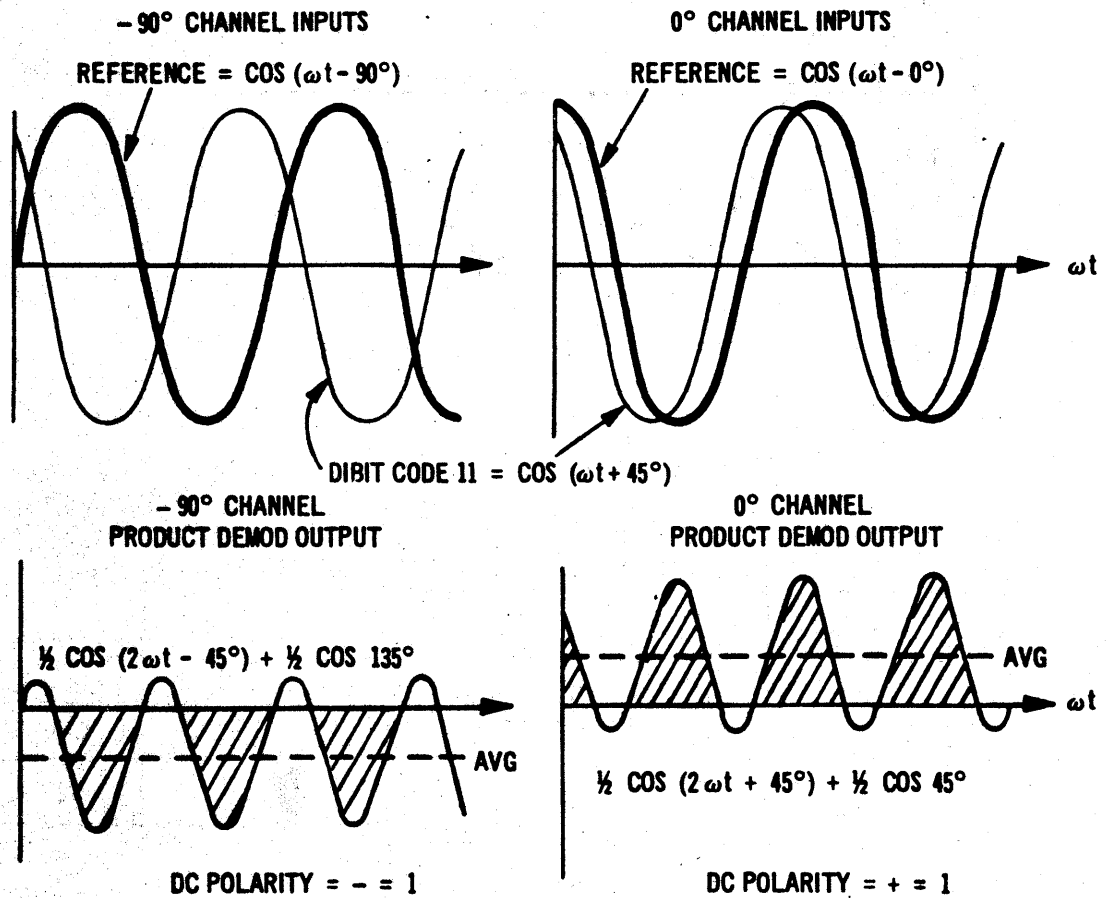


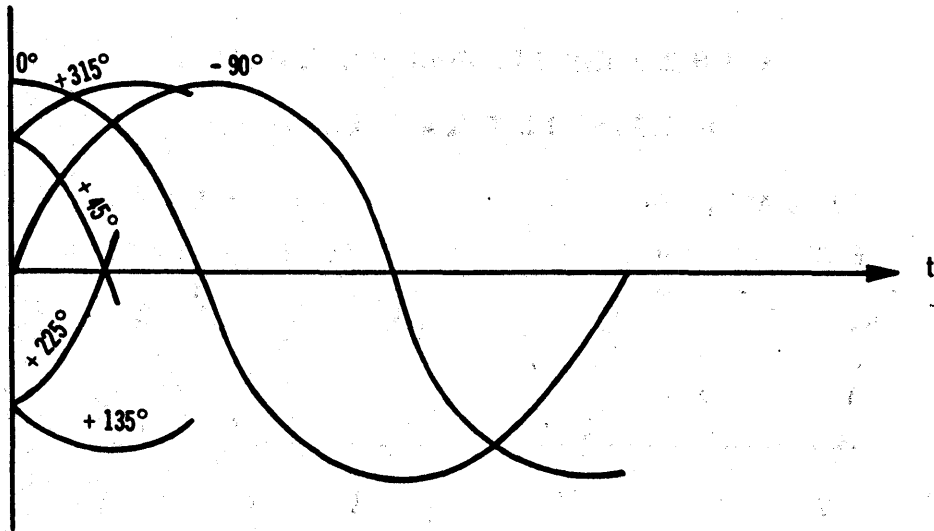
FIGURE 24
METHOD OF OPERATION FOR BALANCED PRODUCT MODULATOR

**DATA RECOVERY IN A FOUR-PHASE DATA SET
USING PRODUCT DEMODULATORS**



RECOVERED DATA = 11

FIGURE 25



EPOCH ANGLE	- 90°		0°	
	POLARITY	CODE	POLARITY	CODE
+ 45	-	1	+	1
+ 135	-	1	-	0
+ 225	+	0	-	0
+ 315	+	0	+	1

FIGURE 26

RELATIONSHIP BETWEEN EPOCH ANGLES
AND DC POLARITY FOR PRODUCT MODULATORS

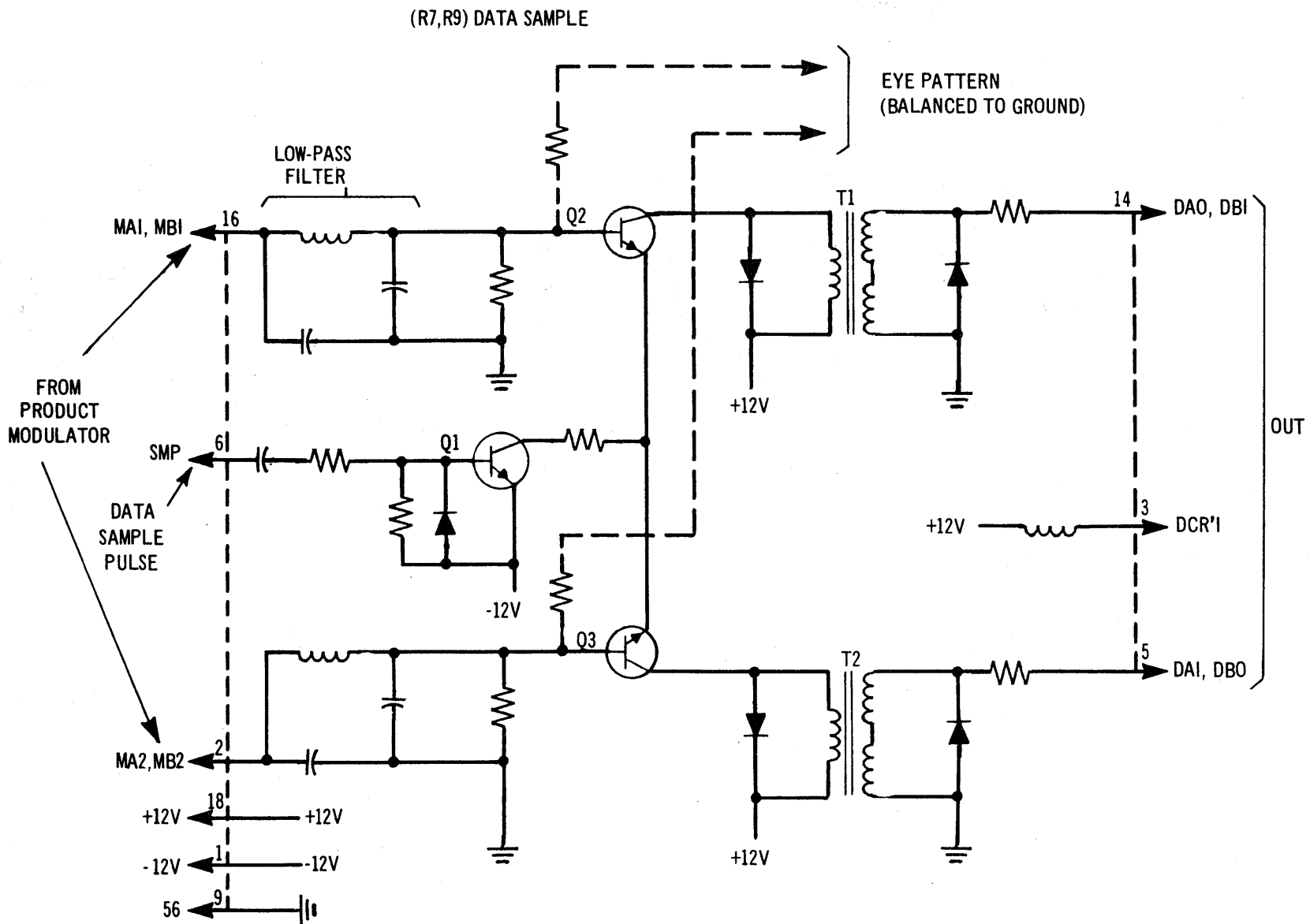
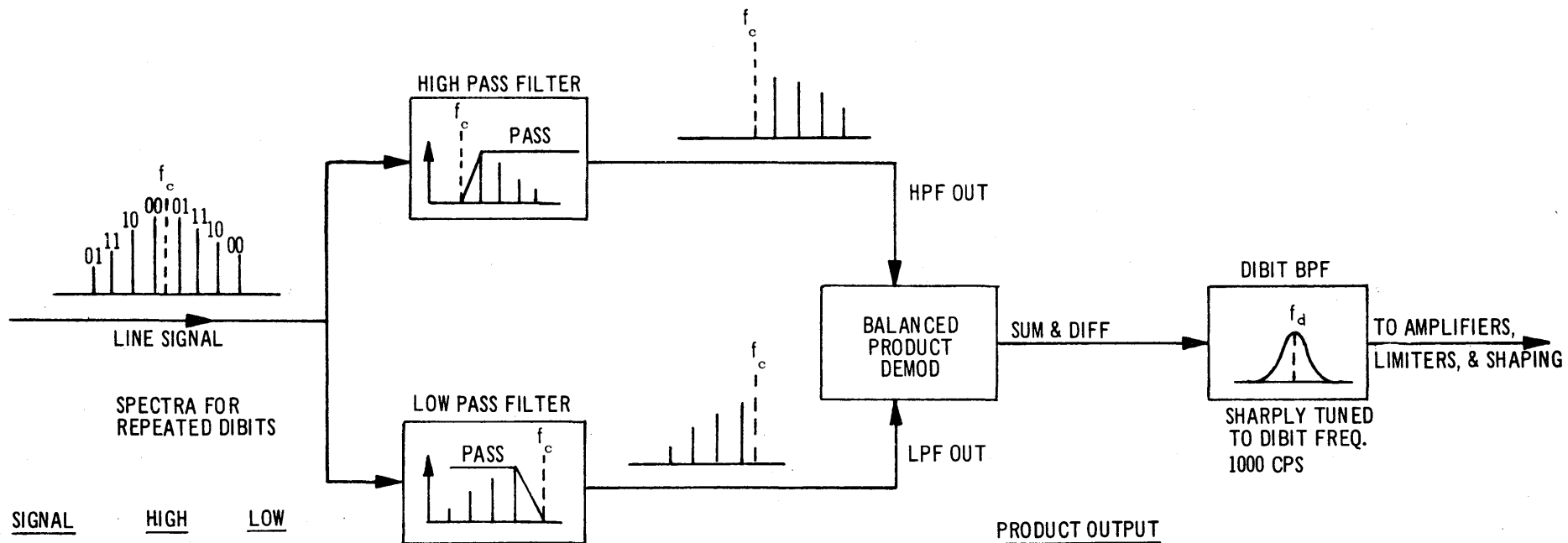


FIGURE 27 DATA SAMPLE CIRCUIT DETAILS



SPECTRA FOR REPEATED DIBITS

SIGNAL	HIGH	LOW
f_c	1750*	
01	1875	875
11	2125	1125
10	2375	1375
00	2625	1625

ABOVE ARE FOR 201A AT 2000 BPS

*SUPPRESSED CARRIER

PRODUCT OUTPUT		
CODE	SUM	DIFF
01	2750	1000
11	3250	1000
10	3750	1000
00	4250	1000

NOTE: THE BALANCED MODULATOR
BALANCES OUT THE HPF AND
LPF INPUT FREQUENCIES.

FIGURE 28
PRINCIPLE OF DIBIT SYNC RECOVERY