



Making the leading edge work for you

1981 PRODUCT
HANDBOOK

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WESTERN DIGITAL
C O R P O R A T I O N

**WESTERN DIGITAL
PRODUCT HANDBOOK**

Making The Leading Edge Work For You

This is our first complete Product Handbook and, naturally, we're proud of it. We're proud of the products detailed in these pages. We're proud of our people, who have taken these products from concept to market. And we're proud of the hundreds of Western Digital customers who have used these products to achieve a competitive advantage in their own markets.

The rate of innovation in this industry is breathtaking. And Western Digital has played an important role in the microelectronic revolution. Our guiding principle though, goes beyond extending the limits of the leading edge; we're dedicated to making the leading edge *work*. The proof is in our products.

And like our products, this handbook has been designed with you in mind. We've gone to great lengths to make it complete, accurate and useful. Now we would like your critical appraisal, to help us improve it. And our products. Let me hear from you directly. Or use the postcard at the back at this handbook.

A handwritten signature in black ink, appearing to read "Charles W. Missler". The signature is fluid and cursive, with a long horizontal stroke extending to the right.

Charles W. Missler
Chairman of the Board
President and Chief Executive Officer

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Introduction to

TELECOMMUNICATIONS

The Telecommunications Division of Western Digital has established a strong market leadership position by developing state-of-the-art standard and custom products which provide cost effective solutions for the complex needs of its customers in the rapidly growing field of digital communications.

GENERAL DATA COMMUNICATIONS

In the General Data Communications product line, our product offerings have been expanded to cover more advanced protocols such as the WD1933 for SDLC/HDLC and the WD1993 for the ARINC 429 which is for avionic use onboard aircraft. With these offerings, Western Digital now has the broadest line of protocol controllers in the industry. Future editions of this catalog will introduce dual devices with multiple system functions per package as well as complete board products.

SECURITY PRODUCTS

Western Digital has introduced the WD2001/2002, the first high-speed LSI implementation of the data encryption algorithm which has been standardized by the National Bureau of Standards. Because of this early market entry the WD2001 has been chosen by companies all over the world for use in their new designs. Future product offerings will include more advanced LSI devices with increased functionality as well as encryption system products.

NETWORK PRODUCTS

One of the most strategic products announced in this catalog is the X.25 Packet Switching Controller, the WD2501. Packet switching is an advanced form of digital network technology that is being heralded as one of the most strategic technologies of the 1980's, and Western Digital's visible leadership in this field will lead to significant growth opportunities in both public networks and "local network" markets such as the "office of the future" and advanced manufacturing applications. The Division is developing both standard proprietary products and custom versions.

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FUNCTIONALITY COMPATIBILITY GUIDE (PARTIAL LIST)

WD	SIGNETICS	FAIRCHILD	INTEL	MOTOROLA	AMI	SMC	HARRIS	ZILOG	MOSTEK
WD1931	2651								
	2661	6852	8251A	6852	6852	8251A		SIO	3884
WD1933		6854							
	2652	6856	8273	6854	6854	5025		SIO	3884
WD1993							429		
WD2001		9414 ¹	8294	6859	6894				
FR1502		33512							

PLEASE CONTACT FACTORY FOR APPLICATIONS ASSISTANCE.

NOTES: 1. Four chip set.

PIN COMPATIBLE REPLACEMENT GUIDE

WD	SMC	GI	NAT	TI	AMI	INTEL	SIGNETICS	HARRIS	INTERSIL
TR1402	COM2502	AY-5-1013A							
	COM2502H	AY-6-1013		TMS6010 ⁴	S1757		2536		
TR1602	COM2017								
	COM2017H			TMS6011 ⁴					
TR1863	COM1863								
	COM8017	AY-3-1014A						HM6402	IM6402
TR1865	COM8018	AY-3-1015D							
PR1472		AY-3-1472B ⁴							
PT1482		AY-3-1482B ⁴							
UC1671	COM1671		INS1671						
WD8250			INS8250						
WD1983 ¹			INS8251A			8251A			
BR1941 ²	COM5016								
	COM5036 ³								

PLEASE CONSULT FACTORY FOR MAXIMUM OPERATING FREQUENCIES AND HIGH-RELIABILITY SCREENING.

- NOTES: 1. WD1983 is ASYNC only.
 2. Many frequency selections available. Consult factory for details.
 Frequency selection is mask programmable—consult factory for details.
 3. Pin 10 on BR1941 is a "no connection".
 4. Discontinued product.

PRODUCT SELECTION CHART

9000-102-1

GENERAL DATA COMMUNICATIONS PRODUCTS	ARINC		UARTS			BOARTS			PSAR/PSAT		USART		DLC
	W	T	T	W	W	W	W	P	P	U	W	W	
	D	R	R	D	D	D	D	R	T	C	D	D	
	1	1	1	1	2	8	1	1	1	1	1	1	
	9	6	8	9	1	2	9	4	4	6	9	9	
	9	0	6	8	2	5	8	7	8	7	3	3	
	3	2	3/5	3	3	0	4	2	2	1	1	3	
PROTOCOL													
ARINC 429	o												
ASYNCH			o	o	o	o	o	o	o	o	o	o	
ISOCH			o	o	o	o		o	o	o			
SYNCH (BI-SYNCH)								o	o	o	o		
SDLC												o	
HDLG												o	
ADCCP												o	
FEATURES													
FULL DUPLEX	o	o	o	o	o	o	o			o	o	o	
MAXIMUM 100 kHz													
320 kHz			o									o	
500 kHz													
640 kHz	o			o				o	o				
1000 kHz			o		o	o	o			o	o	o	
1500 kHz			o										
2500 kHz			o									o	
3500 kHz			o										
SELECTABLE CLOCK													
BOTH TRANSMIT AND RECEIVE			o	o									
INDEPENDENT TRANSMIT AND RECEIVE	o			o	o	o	o	o	o	o	o	o	
1X				o	o	o	o	o	o	o	o	o	
4X	o						o						
16X			o	o	o	o	o	o	o			o	
32X								o	o	o		o	
64X				o	o	o		o	o	o	o		
128X												o	
256X												o	
WORD LENGTH SELECT													
5,6,7,8 BIT	o	o	o	o	o	o	o	o	o	o	o	o	
STOP BIT SELECT 1,1.5,2													
1	o	o	o	o	o	o	o	o	o	o	o	o	
PARITY SELECT ODD/EVEN													
ODD	o	o	o	o	o	o	o	o	o	o	o	o	
MATCH/SYN GENERATE													
MATCH/SYN DETECT								o		o	o	o	
BREAK DETECT													
BREAK DETECT	o			o	o	o	o						
DOUBLE BUFFERING													
DOUBLE BUFFERING	o	o	o	o	o	o	o	o	o	o	o	o	
TTL COMPATIBLE													
TTL COMPATIBLE	o	o	o	o	o	o	o	o	o	o	o	o	

PRODUCT SELECTION CHART

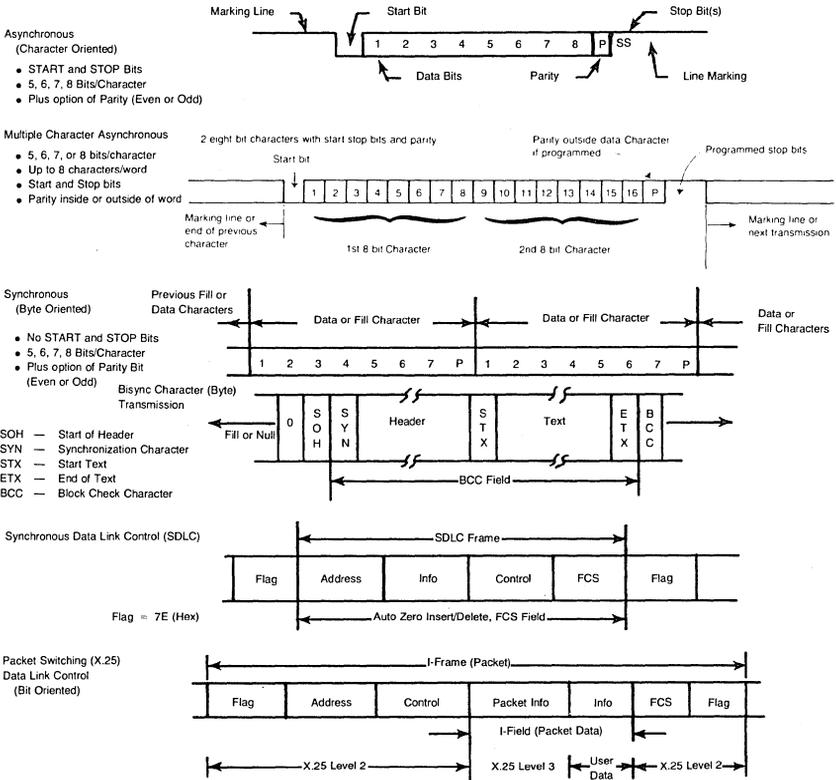
GENERAL DATA COMMUNICATIONS PRODUCTS	ARINC	UARTS		BOARTS			PSAR/PSAT		USART		DLC
	W D	T R	T R	W D	W D	W D	P R	P T	U C	W D	W D
	1	1	1	1	2	8	1	1	1	1	1
	9	6	8	9	1	2	9	4	4	6	9
	9	0	6	8	2	5	8	7	8	7	3
	3	2	³ / ₅	3	3	0	4	2	2	1	1
ERROR CHECKING											
FRAMING	•	•	•	•	•	•	•	•	•	•	•
OVERRUN	•	•	•	•			•	•			•
UNDERRUN	•						•			•	•
CRC GENERATE AND CHECK											•
PROCESSOR INTERFACE											
UNIDIRECTIONAL			•	•				•	•		
BIDIRECTIONAL	•				•	•	•	•		•	•
CONTROL PROGRAMMING											
DEVICE PINS			•	•				•	•		
BIDIRECTIONAL BUS	•				•	•	•	•		•	•
MODEM INTERFACE											
NUMBER OF SIGNALS	8										•
	6					•				•	•
	4		•								
	2				•						
SELF LOOP TEST											
	•					•	•			•	•
SPECIAL FEATURES											
NRZI OPTION											•
DIGITAL PHASE LOCK LOOP										•	•
ON BOARD BAUD RATE GENERATOR					•	•					
EXTENDED WORD SIZE	•						•				
TWO FULL DUPLEX CHANNELS						•					

General Data Communications Products

DATA COMMUNICATION FAMILIES

- UART — Universal Asynchronous Receiver-Transmitter
- PSAT — Programmable Synchronous/Asynchronous Transmitter
- PSAR — Programmable Synchronous/Asynchronous Receiver
- USART — Universal Synchronous/Asynchronous Receiver-Transmitter
- BOART — Bus Oriented Asynchronous Receiver-Transmitter
- DLC — Data Link Controller

PROTOCOL DEFINITIONS



TR1602/TR1402/TR1863/TR1865 Universal Asynchronous Receiver/Transmitter (UART)

FEATURES

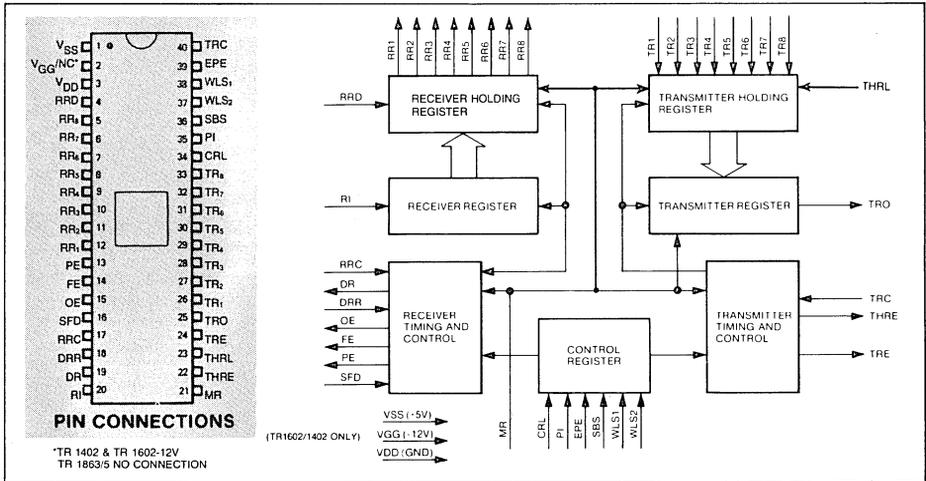
- DUAL POWER SUPPLY TR1602/TR1402
- SINGLE POWER SUPPLY — +5VDC ON TR1863/5
- D.C. TO 1 MHZ (64 KB) (STANDARD PART) TR1863/5
- FULL DUPLEX OR HALF DUPLEX OPERATION
- AUTOMATIC INTERNAL SYNCHRONIZATION OF DATA AND CLOCK
- AUTOMATIC START BIT GENERATION
- EXTERNALLY SELECTABLE
 - Word Length
 - Baud Rate
 - Even/Odd Parity (Receiver/Verification — Transmitter/Generation)
 - Parity Inhibit
 - One, One and One-Half, or Two Stop Bit Generation (1½ at 5 Bit Level for TR1602, TR1863/5)
- AUTOMATIC DATA RECEIVED/TRANSMITTED STATUS GENERATION
 - Transmission Complete
 - Buffer Register Transfer Complete
 - Received Data Available
 - Parity Error
 - Framing Error
 - Overrun Error

- BUFFERED RECEIVER AND TRANSMITTER REGISTERS
- THREE-STATE OUTPUTS
 - Receiver Register Outputs
 - Status Flags
- TTL COMPATIBLE
- TR1865 HAS PULL-UP RESISTORS ON ALL INPUTS

APPLICATIONS

- PERIPHERALS
- TERMINALS
- MINI COMPUTERS
- FACSIMILE TRANSMISSION
- MODEMS
- CONCENTRATORS
- ASYNCHRONOUS DATA MULTIPLEXERS
- CARD AND TAPE READERS
- PRINTERS
- DATA SETS
- CONTROLLERS
- KEYBOARD ENCODERS
- REMOTE DATA ACQUISITION SYSTEMS
- ASYNCHRONOUS DATA CASSETTES

MARCH, 1981



TR1602/TR1402/TR1863/TR1865 BLOCK DIAGRAM

GENERAL DESCRIPTION

The ASYNCHRONOUS RECEIVER/TRANSMITTER is a general purpose, programmable MOS/LSI device for interfacing an asynchronous serial data channel of a peripheral or terminal with parallel data of a computer or terminal. The transmitter section converts parallel data into a serial word which contains the data along with start/stop bits, and optional parity. The receiver section converts a serial word with start, data, optional parity, and stop bits, into parallel data, and it verifies proper code transmission by checking parity and receipt of a valid stop bit. Both

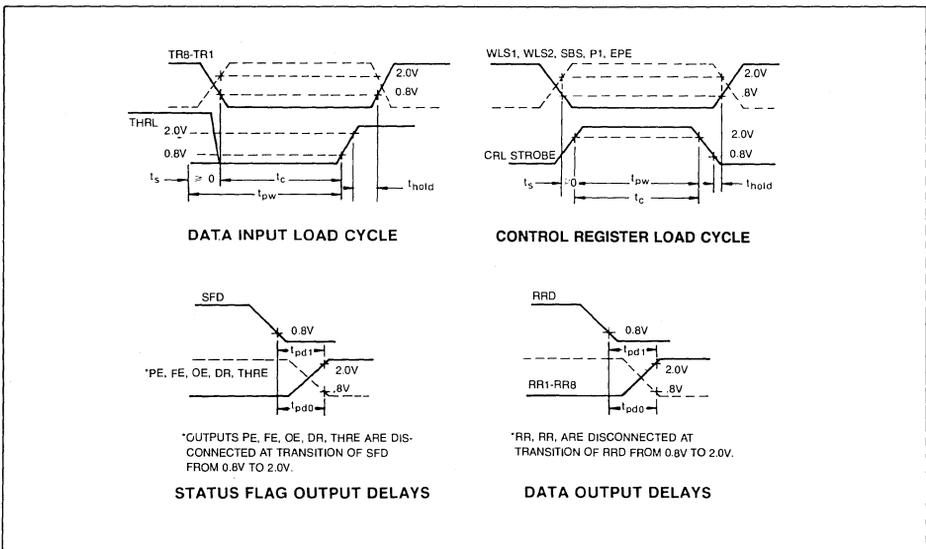
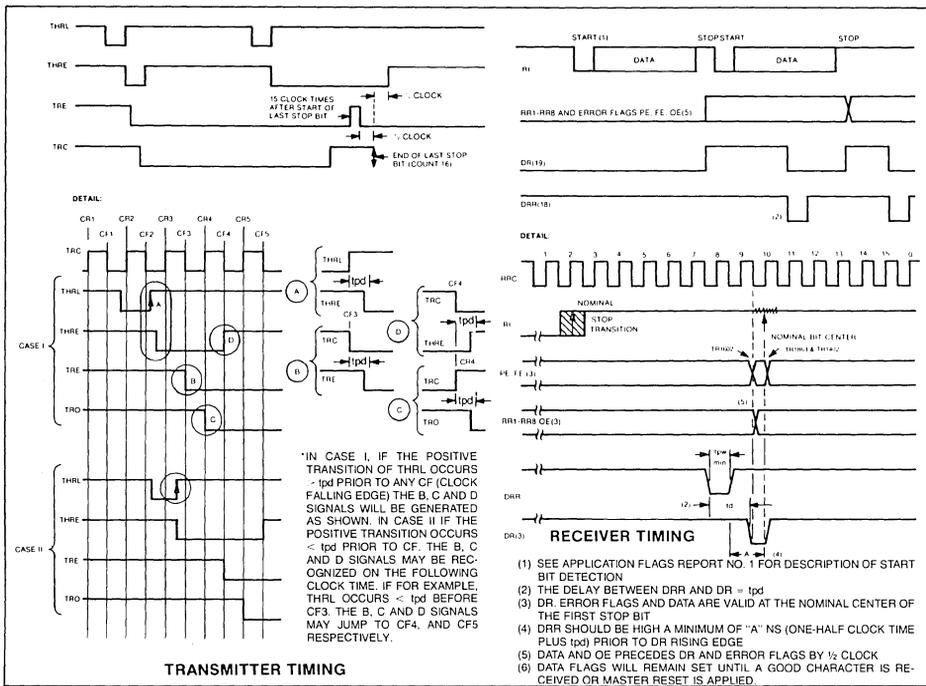
the receiver and the transmitter are double buffered. The array is compatible with bipolar logic. The array may be programmed as follows: The word length can be either 5, 6, 7, or 8 bits; parity generation and checking may be inhibited, the parity may be even or odd; and the number of stop bits may be either one or two, with one and one-half when transmitting a 5 bit code. The TR1863/5 is pin- and function-compatible to the TR1402 and TR1602 except that it is +5V only and can operate up to 3.5 MHz (218.75K Baud). The standard TR1863/5 operates at 1.0 MHz (62.5K Baud).

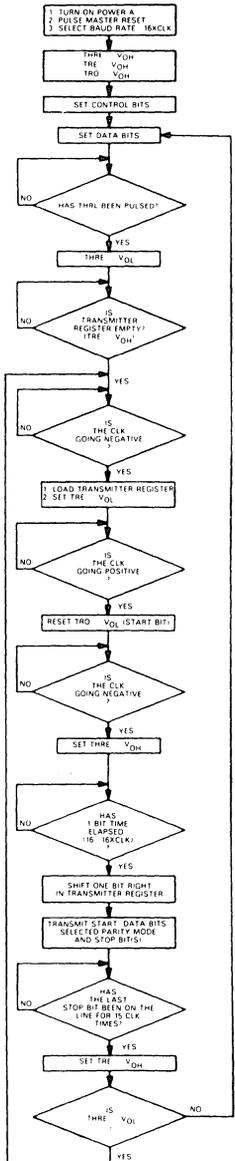
PIN DEFINITIONS

PIN NUMBER	NAME	SYMBOL	FUNCTION
1	V _{SS} POWER SUPPLY	VSS	+5 volts supply
2	V _{GG} — TR1602/TR1402 NC — TR1863/5	VGG NC	-12 volts supply No Connection (open)
3	V _{DD} POWER SUPPLY	GND	Ground = 0V
4	RECEIVER REGISTER DISCONNECT	RRD	A high level input voltage, V _{IH} , applied to this line disconnects the RECEIVER HOLDING REGISTER outputs from the RR ₁₋₈ data outputs (pins 5-12).
5-12	RECEIVER HOLDING REGISTER DATA	RR ₈₋₁	The parallel contents of the RECEIVER HOLDING REGISTER appear on these lines if a low-level input voltage, V _{IL} , is applied to RRD. For character formats of fewer than eight bits received characters are right-justified with RR1 (pin 12) as the least significant bit and the truncated bits are forced to a low level output voltage, V _{OL} .
13	PARITY ERROR	PE	A high level output voltage, V _{OH} , on this line indicates that the received parity does not compare to that programmed by the EVEN PARITY ENABLE control line (pin 39). This output is updated each time a character is transferred to the RECEIVER HOLDING REGISTER. PE lines from a number of arrays can be bussed together since an output disconnect capability is provided by Status Flag Disconnect line (pin 16).
14	FRAMING ERROR	FE	A high-level output voltage, V _{OH} , on this line indicates that the received character has no valid stop bit, i.e., the bit (if programmed) is not a high level voltage. This output is updated each time a character is transferred to the Receiver Holding Register. FE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
15	OVERRUN ERROR	OE	A high-level output voltage, V _{OH} , on this line indicates that the Data Received Flag (pin 19) was not reset before the next character was transferred to the Receiver Holding Register. OE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
16	STATUS FLAGS DISCONNECT	SFD	A high-level input voltage, V _{IH} , applied to this pin disconnects the PE, FE, OE, DR and THRE allowing them to be buss connected.

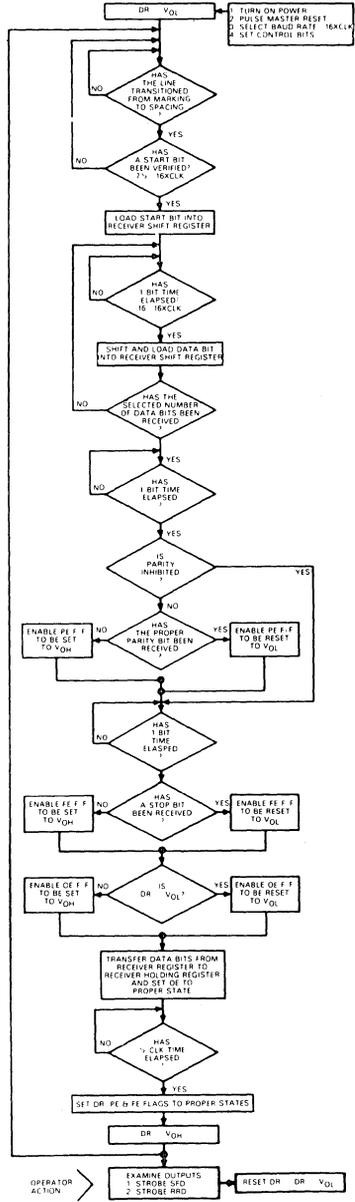
PIN NUMBER	NAME	SYMBOL	FUNCTION
17	RECEIVER REGISTER CLOCK	RRC	The receiver clock frequency is sixteen (16) times the desired receiver shift rate.
18	DATA RECEIVED RESET	DRR	A low-level input voltage, V_{IL} , applied to this line resets the DR line.
19	DATA RECEIVED	DR	A high-level output voltage, V_{OH} , indicates that an entire character has been received and transferred to the RECEIVER HOLDING REGISTER.
20	RECEIVER INPUT	RI	Serial input data received on this line enters the RECEIVER REGISTER at a point determined by the character length, parity, and the number of stop bits. A high-level input voltage, V_{IH} , must be present when data is not being received.
21	MASTER RESET	MR	This line is strobed to a high-level input voltage, V_{IH} , to clear the logic. It resets the Transmitter and Receiver Holding Registers, the Transmitter Register, FE, OE, PE, DR and sets TRO, THRE, and TRE to a high-level output voltage, V_{OH} .
22	TRANSMITTER HOLDING REGISTER EMPTY	THRE	A high-level output voltage, V_{OH} , on this line indicates the TRANSMITTER HOLDING REGISTER has transferred its contents to the TRANSMITTER REGISTER and may be loaded with a new character.
23	TRANSMITTER HOLDING REGISTER LOAD	THRL	A low-level input voltage, V_{IL} , applied to this line enters a character into the TRANSMITTER HOLDING REGISTER. A transition from a low-level input voltage, V_{IL} , to a high-level input voltage, V_{IH} , transfers the character into the TRANSMITTER REGISTER if it is not in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until its transmission is completed. Upon completion, the new character is automatically transferred simultaneously with the initiation of the serial transmission of the new character.
24	TRANSMITTER REGISTER EMPTY	TRE	A high-level output voltage, V_{OH} , on this line indicates that the TRANSMITTER REGISTER has completed serial transmission of a full character including STOP bit(s). It remains at this level until the start of transmission of the next character.
25	TRANSMITTER REGISTER OUTPUT	TRO	The contents of the TRANSMITTER REGISTER (START bit, DATA bits, PARITY bit, and STOP bits) are serially shifted out on this line. When no data is being transmitted, this line will remain at a high-level output voltage, V_{OH} . Start of transmission is defined as the transition of the START bit from a high-level output voltage V_{OH} , to a low-level output voltage, V_{OL} .
26-33	TRANSMITTER REGISTER DATA INPUTS	TR ₁ -TR ₈	The character to be transmitted is loaded into the TRANSMITTER HOLDING REGISTER on these lines with the THRL Strobe. If a character of less than 8 bits has been selected (by WLS ₁ and WLS ₂), the character is right justified to the least significant bit, RR1, and the excess bits are disregarded. A high-level input voltage, V_{IH} , will cause a high-level output voltage, V_{OH} , to be transmitted.

PIN NUMBER	NAME	SYMBOL	FUNCTION															
34	CONTROL REGISTER LOAD	CRL	A high-level input voltage, V_{IH} , on this line loads the CONTROL REGISTER with the control bits (WLS ₁ , WLS ₂ , EPE, PI, SBS). This line may be strobed or hard wired to a high-level input voltage, V_{IH} .															
35	PARITY INHIBIT	PI	A high-level input voltage, V_{IH} , on this line inhibits the parity generation and verification circuits and will clamp the PE output (pin 13) to V_{OL} . If parity is inhibited, the STOP bit(s) will immediately follow the last data bit of transmission.															
36	STOP BIT(S) SELECT	SBS	This line selects the number of STOP bits to be transmitted after the parity bit. A high-level input voltage V_{IH} , on this line selects two STOP bits, and a low-level input voltage, V_{IL} , selects a single STOP bit. The TR1602 and TR1863 generate 1½ stop bits when word length is 5 bits and SBS is High V_{IH} .															
37-38	WORD LENGTH SELECT	WLS ₂ -WLS ₁	<p>These two lines select the character length (exclusive of parity) as follows:</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>WLS₂</th> <th>WLS₁</th> <th>Word Length</th> </tr> </thead> <tbody> <tr> <td>V_{IL}</td> <td>V_{IL}</td> <td>5 bits</td> </tr> <tr> <td>V_{IL}</td> <td>V_{IH}</td> <td>6 bits</td> </tr> <tr> <td>V_{IH}</td> <td>V_{IL}</td> <td>7 bits</td> </tr> <tr> <td>V_{IH}</td> <td>V_{IH}</td> <td>8 bits</td> </tr> </tbody> </table>	WLS ₂	WLS ₁	Word Length	V_{IL}	V_{IL}	5 bits	V_{IL}	V_{IH}	6 bits	V_{IH}	V_{IL}	7 bits	V_{IH}	V_{IH}	8 bits
WLS ₂	WLS ₁	Word Length																
V_{IL}	V_{IL}	5 bits																
V_{IL}	V_{IH}	6 bits																
V_{IH}	V_{IL}	7 bits																
V_{IH}	V_{IH}	8 bits																
39	EVEN PARITY ENABLE	EPE	This line determines whether even or odd PARITY is to be generated by the transmitter and checked by the receiver. A high-level input voltage, V_{IH} , selects even PARITY and a low-level input voltage, V_{IL} , selects odd PARITY.															
40	TRANSMITTER REGISTER	TRC	The transmitter clock frequency is sixteen (16) times the desired transmitter shift rate.															





TRANSMITTER FLOW CHART



RECEIVER FLOW CHART

ABSOLUTE MAXIMUM RATINGS NOTE: These voltages are measured with respect to GND

Storage Temperature -55°C to +125°C (Plastic) -65°C to +150°C (Ceramic)
 V_{CC} Supply Voltage -0.3V to +7.0V
 Input Voltage at any pin -0.3V to +7.0V
 Operating Free-Air Temperature
 T_A Range 0°C to 70°C
 Lead Temperature (Soldering, 10 sec.) 300°C

ELECTRICAL CHARACTERISTICS

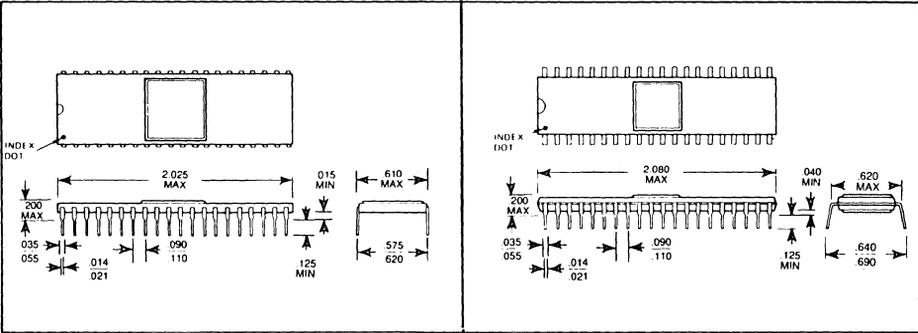
(V_{CC} = 5V ± 5%, V_{DD} = 0V, V_{GG} = -12V ± 5%, TR1602/TR1402) (V_{CC} = 5V ± 5% TR 1863/5)

SYMBOL	PARAMETER	TR1602/TR1402		TR1863/5		CONDITIONS
		MIN	MAX	MIN	MAX	
I _{CC} I _{GG}	OPERATING CURRENT					
	Substrate Supply Current Gate Supply Current		60 ma -10 ma		35 ma	V _{CC} = 5.25V V _{GG} = -12.6V
LOGIC LEVELS						
V _{IH} V _{IL}	Logic High Logic Low	V _{SS} - 1.5V		2.4V		V _{CC} = 4.75V
OUTPUT LOGIC LEVELS						
V _{OH} V _{OL}	Logic High Logic Low	V _{SS} - 1.0V		2.4V		V _{SS} = 4.75V, I _{OH} = 100 µa V _{SS} = 5.25V, I _{OL} = 1.6 ma
I _{OC} I _{IL} I _{IH}	Output Leakage Low Level Input Current High level Input Current		10 µa -1.6 ma		10ua -1.6ma 10 µa	V _{OUT} = 0V, SFD = RRD = V _{IH} V _{IN} = 0.4V V _{IN} = 3.75V, TR1865 only

SWITCHING CHARACTERISTICS

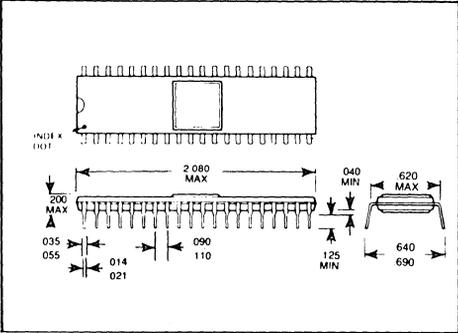
(See "Switching Waveforms")

SYMBOL	PARAMETER	MIN	MAX	CONDITIONS
f _{clock}	Clock Frequency			V _{CC} = 4.75V
	TR1402	DC	320 KHz	with internal pull-ups on all inputs
	TR1602	DC	320 KHz	with internal pull-ups on all inputs
	TR1863-00	DC	1.0 MHz	
	TR1863-02	DC	2.5 MHz	
	TR1863-04	DC	3.5 MHz	
	TR1865-00	DC	1.0 MHz	with internal pull-ups on all inputs
	TR1865-02	DC	2.5 MHz	with internal pull-ups on all inputs
	TR1865-04	DC	3.5 MHz	with internal pull-ups on all inputs
t _{pw}	Pulse Widths			
	CRL	200 ns		
	THRL	200 ns		
	DRR	200 ns		
	MR	500 ns		
t _c	Coincidence Time	200 ns		
t _{hold}	Hold Time	20 ns		
t _{set}	Set Time	0		
OUTPUT PROPAGATION DELAYS				
t _{pd0}	To Low State 1602/1402		650 ns	
t _{pd1}	To High State 1602/1402		650 ns	C _L = 20 pf, plus one TTL load
t _{pd0}	To Low State 1863/1865		250 ns	
t _{pd1}	To High State 1863/1865		250 ns	C _L = 20 pf, plus one TTL load
CAPACITANCE				
c _{in}	Inputs		20 pf	f = 1 MHz, V _{IN} = 5V
c _o	Outputs		20 pf	f = 1 MHz, V _{IN} = 5V



TR1602A, TR1402A, TR1863A, TR1865A
CERAMIC (HERMETIC) PACKAGE

TR1602B, TR1402B, TR1863B, TR1865B
PLASTIC PACKAGE



TR1602P, TR1402P, TR1863P,
TR1865P PLASTIC PACKAGE

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WESTERN DIGITAL CORPORATION

PR1472-01 (PSAR)

Programmable Synchronous & Asynchronous Receiver



FEATURES

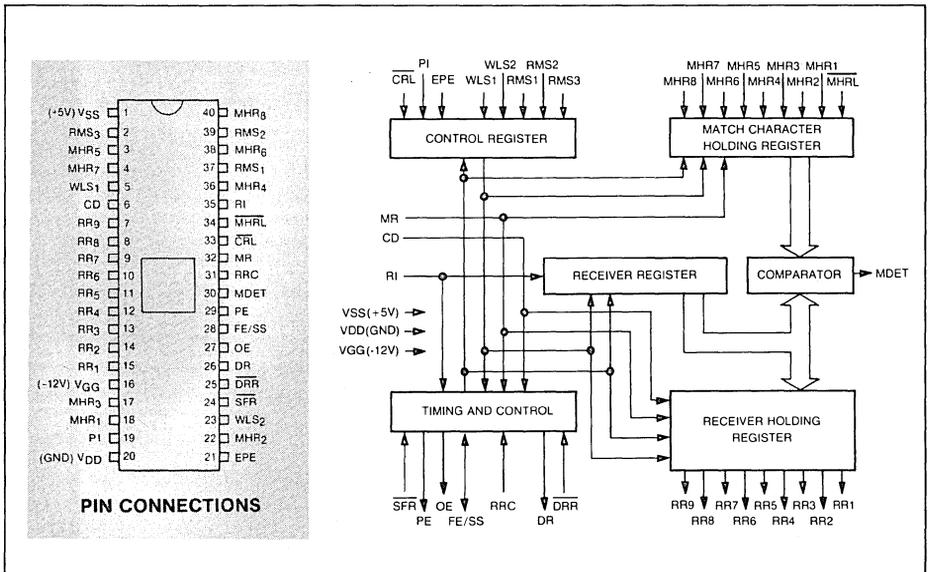
- SYNCHRONOUS, ASYNCHRONOUS OR ISOCHRONOUS OPERATION
- DC TO 640K BITS/SEC (1X CLOCK) PR1472-01; DC TO 100K BITS/SEC PR1472
- PROGRAMMABLE MATCH (FILL) CHARACTER WITH MATCH DETECT FLAG.
- INTERNAL OR EXTERNAL CHARACTER SYNCHRONIZATION
- NINE BIT WIDE RECEIVER HOLDING REGISTER
- SELECTABLE 5, 6, 7 OR 8 BITS PER CHARACTER
- EVEN/ODD OR NO PARITY SELECT
- PROGRAMMABLE CLOCK RATE; 1X, 16X, 32X OR 64X
- AUTOMATIC START AND STOP BIT STRIPPING
- AUTOMATIC CHARACTER STATUS AND FLAG GENERATION
- THREE STATE OUTPUTS — BUS STRUCTURE CAPABILITY
- DOUBLE BUFFERED
- TTL & DTL COMPATIBLE — INTERNAL ACTIVE PULLUP
- COMPATIBLE TRANSMITTER, PT1482

GENERAL DESCRIPTION

The Western Digital PR1472 (PSAR) is a programmable receiver that interfaces variable length serial data to a parallel data channel. The receiver converts a serial data stream into parallel characters with a format compatible with all standard Synchronous, Asynchronous, or Isochronous data communications media.

Contiguous synchronous serial characters are compared to a programmable Match-Character Holding Register, character synchronized and assembled. Programming the Asynchronous or Isochronous Mode provides assembly of characters with start and stop bit(s) which are stripped from the data. Four internal registers, in conjunction with Three-State Outputs provide full system versatility.

The PSAR is a TTL compatible device. The use of internal active pull-up devices and push-pull output drivers, provides direct compatibility with all forms of current sinking logic. Western Digital also offers a Compatible Transmitter, PT1482.



PR1472 BLOCK DIAGRAM

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION																												
1	V _{SS} POWER SUPPLY	V _{SS}	+5 Volt Supply																												
37, 39, 2	RECEIVER MODE SELECT	RMS ₁ , RMS ₂ , RMS ₃	<p>A low-level input voltage, V_{IL}, applied to CD (pin 6) enables RMS₁, RMS₂, and RMS₃ inputs. The Receiver Mode Select Inputs, in conjunction with the Control Register Load and Chip Disable, select the Receiver operating mode. RMS₁, RMS₂, and RMS₃ may be strobed or hard-wired to the appropriate input voltage.</p> <table border="1"> <thead> <tr> <th>RMS₃</th> <th>RMS₂</th> <th>RMS₁</th> <th>Selected Operating Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>ASYNCH OR ISOCH, 1X CLOCK</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>ASYNCH OR ISOCH, 16X CLOCK</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>ASYNCH OR ISOCH, 32X CLOCK</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>ASYNCH OR ISOCH, 64X CLOCK</td> </tr> <tr> <td>1</td> <td>X</td> <td>0</td> <td>SYNCH-EXTERNAL CHARACTER SYNCHRONIZATION</td> </tr> <tr> <td>1</td> <td>X</td> <td>1</td> <td>SYNCH-INTERNAL CHARACTER SYNCHRONIZATION</td> </tr> </tbody> </table> <p>NOTE: When operating in asynchronous or isochronous mode with 1X clock there is no protection against false start bits.</p> <p>A high-level input voltage, V_{IH}, applied to CD disables RMS₁, RMS₂ and RMS₃.</p>	RMS ₃	RMS ₂	RMS ₁	Selected Operating Mode	0	0	0	ASYNCH OR ISOCH, 1X CLOCK	0	0	1	ASYNCH OR ISOCH, 16X CLOCK	0	1	0	ASYNCH OR ISOCH, 32X CLOCK	0	1	1	ASYNCH OR ISOCH, 64X CLOCK	1	X	0	SYNCH-EXTERNAL CHARACTER SYNCHRONIZATION	1	X	1	SYNCH-INTERNAL CHARACTER SYNCHRONIZATION
RMS ₃	RMS ₂	RMS ₁	Selected Operating Mode																												
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1	X	0	SYNCH-EXTERNAL CHARACTER SYNCHRONIZATION																												
1	X	1	SYNCH-INTERNAL CHARACTER SYNCHRONIZATION																												
18,22 17, 36, 3, 38, 4, 40	MATCH-CHARACTER HOLDING REGISTER DATA	MHR ₁ , MHR ₂ , MHR ₃ , MHR ₄ , MHR ₅ , MHR ₆ , MHR ₇ , MHR ₈	<p>A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the inputs to the Match-Character Holding Register Load, MHRL. Parallel 8-bit characters are input into the Match-Character Holding Register with the MHRL Strobe (pin 34). If a character of less than 8 bits has been selected (by WLS₁ and WLS₂), only the least significant bits are accepted. These inputs may be strobed or hard-wired to the appropriate input voltage. A high-level input voltage, V_{IL}, applied to CD disables MHR₁ and MHR₈.</p>																												
5,23	WORD LENGTH SELECT	WLS ₁ , WLS ₂	<p>A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the inputs of the Control Register Load, CRL. Parallel 8-bit characters are input into the Control Register with the CRL Strobe (pin 4), WLS₁ and WLS₂ select the transmitted character length from five (5) to eight (8) bits defined by the Truth Table below:</p> <table border="1"> <thead> <tr> <th>WLS₂</th> <th>WLS₁</th> <th>Selected Word Length</th> </tr> </thead> <tbody> <tr> <td>V_{IL}</td> <td>V_{IL}</td> <td>5 BITS</td> </tr> <tr> <td>V_{IL}</td> <td>V_{IH}</td> <td>6 BITS</td> </tr> <tr> <td>V_{IH}</td> <td>V_{IL}</td> <td>7 BITS</td> </tr> <tr> <td>V_{IH}</td> <td>V_{IH}</td> <td>8 BITS</td> </tr> </tbody> </table> <p>WLS₁ and WLS₂ may be strobed or hard-wired to the appropriate input voltage. A high-level input voltage, V_{IH}, applied to CD disables WLS₁ and WLS₂.</p>	WLS ₂	WLS ₁	Selected Word Length	V _{IL}	V _{IL}	5 BITS	V _{IL}	V _{IH}	6 BITS	V _{IH}	V _{IL}	7 BITS	V _{IH}	V _{IH}	8 BITS													
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PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
24	STATUS FLAG RESET	SFR	A low-level input voltage, V_{IL} , applied to CD (pin 6) enables the SFR input. A low-level input voltage, V_{IL} , applied to this line resets the PE, FE and OE Status Flags.
25	DATA RECEIVED RESET	DRR	A low-level input voltage, V_{IL} , applied to CD (pin 6) enables the DRR input. A low-level input voltage, V_{IL} , applied to this line resets the DR Flag. A high-level input voltage, V_{IH} , applied to CD disables DRR.
26	DATA RECEIVED FLAG	DR	A high-level output voltage, V_{OH} , indicates that an entire character has been received and transferred to the Receiver Holding Register. When operating in the synchronous mode, the first SYN character, when located and transferred to the Receiver Holding Register, will not cause DR to go to a high-level output voltage, V_{OH} , but will cause MDET to go to a high-level output voltage. Character transfer to the Receiver Holding Register occurs in the center of the last bit of a synchronous character or the center of the first STOP element of an asynchronous or isochronous character at which time this flag is updated.
27	OVERRUN ERROR FLAG	OE	A low-level input voltage, V_{IL} , applied to CD (pin 6) enables the OE input. A high-level output voltage, V_{OH} , indicates that the previously received character was not read (DR line not reset) and was, therefore, lost before the present character was transferred to the Receiver Holding Register. This transfer occurs in the center of the last bit of a received synchronous character or in the center of the first STOP element of an asynchronous or isochronous character at which time this flag is updated. A high-level input voltage, V_{OH} , applied to CD disables OE.
28	FRAMING ERROR/ SYN SEARCH	FE/SS	FE/SS is a two-way (I/O) bus. If programmed for the ASYNCHRONOUS or ISOCHRONOUS MODE, a low-level input voltage, V_{IL} , applied to CD (pin 6) enables the FRAMING ERROR FLAG output which indicates the status of the STOP BIT detection circuit. A high-level output voltage, V_{OH} , indicates that the character transferred to the Receiver Holding Register has no valid STOP BIT; i.e., the bit following the PARITY BIT is not a high-level input voltage, V_{IH} . This transfer occurs in the center of the first stop element at which time this flag is updated. When programmed for the SYNCHRONOUS MODE, this line is an input and is not under control of CD. This line should be driven by a tri-state or an open collector device. If programmed for INTERNAL CHARACTER SYNCHRONIZATION, a transition from a low-level input voltage, V_{IL} , to a high-level input voltage, V_{IH} , initiates the automatic internal "SYN" CHARACTER search operation.

20-10ms
 1-20-10ms

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
28	FRAMING ERROR/ SYN SEARCH	FE/SS	<p>Prior to initiation of this operation, the Receiver Holding Register is "transparent" so that its contents are identical to that of the RECEIVER REGISTER. Upon receipt of a SYN character, (previously loaded into the Match-Character Holding Register during initialization), the Receiver Holding Register becomes non-transparent, the MATCH DETECT output (MDET) goes to a high-level output voltage, V_{OH}, but, the Data Received (DR) FLAG does not assume a high-level output voltage, V_{OH}. The P/SAR is now in character synchronization. Subsequent SYN or data character will be transferred to the RECEIVER HOLDING REGISTER as they are assembled (at the center of the last bit) and the DR FLAG will be raised. A transition from a high-level input voltage, V_{IH}, to a low-level input voltage, V_{IL}, causes the P/SAR to lose character synchronization and forces the Receiver Holding Register to become "transparent."</p> <p>If programmed for EXTERNAL CHARACTER SYNCHRONIZATION, the system external to the P/SAR examines the data stream for "SYN" characters when SYN SEARCH is a low-level input voltage, V_{IL}. The Receiver Holding Register is "transparent" which allows the contents of the RECEIVER REGISTER to be monitored as it ripples through the shift register. When the external logic locates a "SYN" CHARACTER, indicated by a high-level input voltage, V_{OH}, on MDET, the SYN SEARCH line is externally raised to a high-level input voltage, V_{IH}. This high-level input voltage causes character synchronization to be initiated, returns the Receiver Holding Register to a "non-transparent" condition, causing subsequent characters to be transferred to the RECEIVER HOLDING REGISTER (when the center of the last bit of a character is recognized) and raises the DR FLAG.</p>
30	MATCH DETECT FLAG	MDET	<p>A high-level output voltage, V_{OH}, indicates that the contents of the Transmitter Register are identical to the contents of the Match-Character Holding Register. This flag is set to a high-level output voltage, V_{OH}, at the center of the first STOP ELEMENT of an asynchronous or isochronous character.</p>
31	RECEIVER REGISTER CLOCK	RRC	<p>This fifty (50) percent duty cycle clock provides the basic receiver timing. The negative transition from a high-level input voltage, V_{IH}, to a low-level input voltage, V_{IL}, shifts data into the RECEIVER REGISTER at a rate determined by RMS_1, RMS_2 and RMS_3. Synchronous operation requires that this negative transition occur at the center of each data bit.</p>

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
32	MASTER RESET	MR	A high-level input voltage, V_{IH} , applied to this line resets timing and control logic to an idle state, sets the contents of the Receiver Holding Register to a high-level output voltage, V_{OH} , resets the contents of the Match-Character Holding Register, the MDET, DR, PE, FE, and OE outputs to a low-level output voltage, V_{OL} , but does not effect the contents of the control register.
33	<u>CONTROL REGISTER LOAD</u>	\overline{CRL}	A low-level input voltage, V_{IL} , applied to CD (pin 6) enables the \overline{CRL} input. A low-level input voltage, V_{IL} , applied to this line enables inputs to DC "D Type" Latches of the Control Register and loads it with Control Bits (EPE, PI, RMS ₁ , RMS ₂ , RMS ₃ , WLS ₁ , WLS ₂). A high-level input voltage, V_{IH} , applied to this line disables the Control Register. This line may be strobed or hard-wired to a low-level input voltage, V_{IL} . A high-level input voltage, V_{IH} , applied to CD disables CRL.
34	<u>MATCH CHARACTER HOLDING REGISTER LOAD</u>	\overline{MHRL}	A low-level input voltage, V_{IL} , applied to CD (pin 6) enables the \overline{MHRL} input. A low-level input voltage, V_{IL} , applied to this line enables input to DC "D Type" Latches of the Match-Character Holding Register and loads it with the Match-Character Holding Register. This line may be strobed or hard-wired to a low-level input voltage, V_{IL} . A high-level input voltage, V_{IH} , applied to CD disables \overline{MHRL} .
35	RECEIVER INPUT	RI	The serial input data stream received on this line enters the Receiver Register determined by the character length, parity and the number of stop bits programmed. A high-level input voltage, V_{IH} , must be present when no ASYNCHRONOUS data is being received.

ORGANIZATION

PR1472 block diagram is illustrated on page 1.

Control Register — Programming of the PSAR is accomplished by loading the 7 Bit Control register. Mode selection, clock division, word length, and parity are selected when the Control Register Load (CRL) signal is activated.

Receiver Register — The Receiver Register is used to store the incoming data stream. The contents of this register can be gated to the Holding register during the transparent mode, or compared with the Match Holding Register. When a character is assembled it is transferred to the Receiver Holding Register.

Receiver Holding Register — The Receiver Holding Register, a buffer register, is used to store the assembled character.

Match Holding Register — The Match Holding Register is used to store the match character. The contents of this register are compared with the

receiver register to establish character synchronization.

Timing & Control — The Timing and Control Logic generates the required control signals to assemble characters, match comparison, bit stripping, and generation of status/flag signals.

SYNCHRONOUS MODE OPERATION

Synchronous data appears as a continuous bit stream of contiguous characters at the input to the receiver with no Start or Stop bits. Character synchronization (the "framing" of this continuous bit stream into characters of a predetermined fixed length), must be accomplished by a comparison of this bit stream and a synchronization sequence. The P/SAR is designed to accommodate internal or external character synchronization by program control.

Referring to the Block Diagram of the Receiver, the Chip Disable (CD) enables or disconnects various in-

puts and outputs of the P/SAR. This feature provides the device with the capability of being disconnected from the system bus. The inputs to the Control Register and Match-Character Holding Register and their respective load strobes, CRL and MHRL are under CD control. In addition, DRR, SFR, PE, and OE and the outputs of the Receiver Holding Register, are also controlled by CD. It is necessary that CD enable these lines to allow strobing information in these registers and to allow examination of these output flags and data.

Device operation is programmed subsequent to being forced into its "idle" state. The P/SAR will enter a defined "idle" state when the Master Reset (MR) line is strobed to a high-level input voltage. In this state, all timing and control logic are reset, the contents of the Receiver Holding Register is set to a high-level output voltage and all output flags are reset to a low-level output voltage. The Master Reset also causes the contents of the Match-Character Holding Register to be reset to a low-level output voltage.

Enabled by CD, the Control Register is loaded by strobing CRL to a low-level input voltage which defines mode of operation and clock rate selection, character length and selected parity if required. Table 1 illustrates all programmable synchronous formats.

Character synchronization from the data stream requires Receiver recognition of specific bit pattern(s) which define the relative position of synchronous characters in the data stream and subsequent character assembly. The P/SAR programmably accommodates internal or external character synchronization.

Programmed for internal character synchronization, a high-level input voltage on the Sync Search line, the Receiver Holding Register is "transparent" and its contents are identical to the Receiver Holding Register. The data stream, gated into the Receiver Input (RI) by the negative transition of the Receiver Register Clock (RRC), shifts through the Receiver Register and is compared with the preprogrammed character in the Match-Character Holding Register. A match, indicated by a high-level output voltage on Match Detect (MDET), returns the Receiver Holding register to its non-transparent state and initializes timing and control logic but does not set the Data Received Flag to a high-level output voltage. The character following the match will be transferred to the Receiver Holding Register at the receipt of the center of its last bit and the Data Received Flag is set to a high-level output voltage. Depending on line discipline, this last character may also be a synchronizing character, in which case, Match Detect will continue to be a high-level output voltage when the Data Received Flag is set. Therefore, sequence verification can be performed by the system (additional hardware or software as desired).

Parity, if programmed, is verified upon receipt of the center of the parity bit which is the last bit of a synchronous character. If a parity error exists, the associated PE register is set to a high-level output voltage.

Transfer of a character to the Receiver Holding Register sets the associated Data Received Register Flag (DR) to a high-level output voltage. The transfer of a character to the Receiver Holding Register, if the Data Received Register Flag had already been set to a high-level output voltage, causes the previous character to be lost (written over) and is alerted by an Overrun Error Flag which is a high-level output voltage. In normal operation, the Data Received Flag is reset by DRR when the Receiver Holding Register is serviced (unloaded). The Status Flags, PE and OE, are also provided with an external reset SFR so that block status and character status may be (accumulated) verified. A low-level input voltage on Sync Search causes character synchronization to be lost and initiates transparency of the Receiver Holding Register.

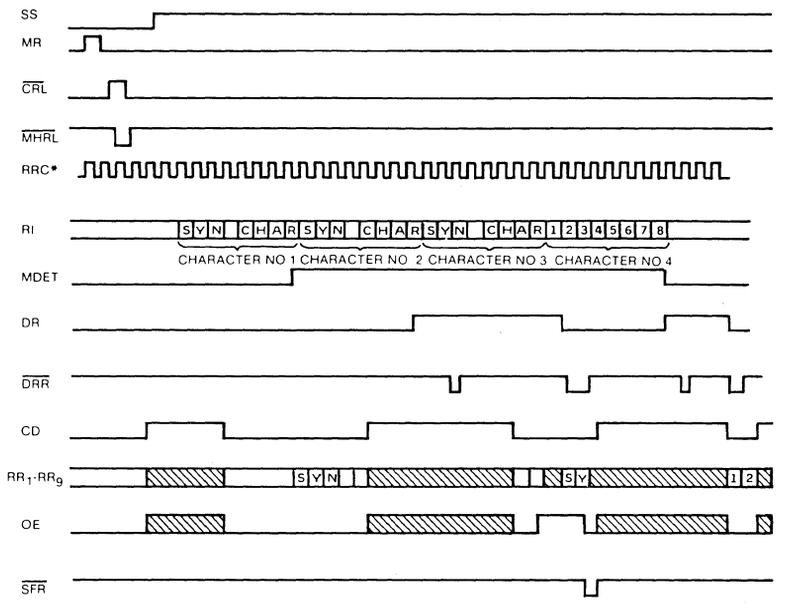
External character synchronization, programmed by the Control Register, is similar to the description above with the exception that the Sync Search line controls the nontransparency of the Receiver Holding Register directly and comparison is done externally. Upon recognition of the appropriate synchronizing pattern, the Sync Search line is set to a high-level input voltage prior to the end of the last bit. Raising the Sync Search line to a high-level input voltage causes the buffer to go "nontransparent", initializing timing and control circuitry to "frame" characters. The first bit received after a high-level input voltage is applied to Sync Search, defines the start of the "frame". Character length defined by the Control Register defines the end of the "frame".

Table 1. SYNC MODE CONTROL DEFINITION

CONTROL WORD					CHARACTER FORMAT	
R	W	W			DATA	PARITY BIT
M	L	L	E		BITS	CHECKED
S	S	S	P	P		
3	2	1	I	E		
1	0	0	0	0	5	ODD
1	0	0	0	1	5	EVEN
1	0	0	1	X	5	NONE
1	0	1	0	0	6	ODD
1	0	1	0	1	6	EVEN
1	0	1	1	X	6	NONE
1	1	0	0	0	7	ODD
1	1	0	0	1	7	EVEN
1	1	0	1	X	7	NONE
1	1	1	0	0	8	ODD
1	1	1	0	1	8	EVEN
1	1	1	1	X	8	NONE

↑ Sets to SYNC Mode

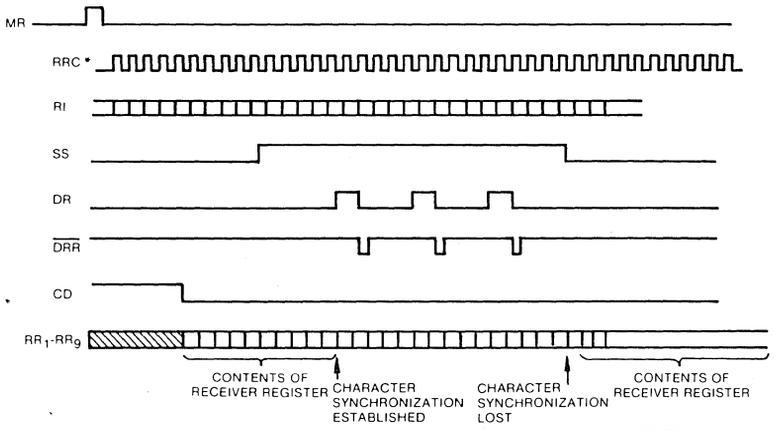
If RMS₁ = 1, the receiver operates in the internal character SYNC mode.
 If RMS₁ = 0, character SYNC must be externally provided.



*CLOCK SHOWN IS BIT RATE CLOCK (1X)

NOTE OUTPUTS FLOATING

(INTERNAL SYNCHRONIZATION)



*CLOCK SHOWN IS BIT RATE CLOCK (1X)

NOTE OUTPUTS FLOATING

(EXTERNAL SYNCHRONIZATION)

SYNCHRONOUS TIMING DETAIL

ASYNCHRONOUS & ISOCRONOUS MODE

The completed assembly of a parallel character, by the P/SAR, from a serial data stream and buffered by its Receiver Holding Register is indicated by the status of the Data Received (DR) Flag. The assembly of character from a serial data stream consisting of a start bit, data, parity (if programmed), and a stop interval is initiated by the Start bit transition.

Verification of parity and receipt of a valid stop bit is accomplished prior to the character transfer to the Receiver Holding Register. Simultaneously, this data is compared with a preprogrammed character in the Match-Character Holding Register.

Status Flags, Data Received, Parity Error, Framing Error, Overrun Error and Match Detect are loaded into status registers during character transfer to the Receiver Holding Register.

Referring to the Block Diagram of the Receiver, the Chip Disable enables or disconnects various inputs and outputs of the P/SAR. This feature provides the device with the capability of being disconnected from the system bus. The inputs to the Control Register and Match-Character Holding Register and their respective load strobes, CRL and MHR, are under CD control. In addition, DRR, SFR, PE, FE, OE and the outputs of the Receiver Holding Register are also controlled by CD. It is necessary that CD enable these lines to allow strobing information into these registers and to allow examination of these output data and flags.

Device operation is programmed subsequent to being forced into its "idle" state. The P/SAR will enter a defined "idle" state when the Master Reset (MR) line is strobed to a high-level input voltage. In this state, all timing and control logic are reset, the contents of the Receiver Holding Register is set to a high-level output voltage, and all output flags are reset to a low-level output voltage. The Master Reset also causes the contents of the Match-Character Holding Register to be reset to a low-level output voltage.

When the Receiver is enabled by CD, loading the Control Register by strobing the Control Register Load (CRL) line to a low-level input voltage defines the mode of operation and clock rate selection, character length and selected parity if required. Table 2 illustrates all the programmable asynchronous formats.

A mark to space transition on the receiver input initializes the clock counter causing it to count to the theoretical center of the start bit. At this time, the input is sampled. A high-level input voltage at the Receiver Input causes the first mark to space transition to be interpreted as a noise spike and resets all timing and control logic. This provides one-half data bit noise immunity on all clock selec-

tion rates except 1X. A low-level input voltage at the Receiver Input at the theoretical center of the start bit causes timing and control circuitry to sample the theoretical center of succeeding data bits. This data is shifted through the Receiver Register. When an entire character (as defined by the Control Register) is assembled in the Receiver Register, the line is "tested" for a valid stop bit at its theoretical center. This character is also compared with the contents of the Match-Character Holding Register at the center of the stop bit and its parity is verified. A parallel transfer occurs, loading the contents of the Receiver Register (less start and stop bits) into the Receiver Holding Register. The status of the parity verification, framing error, and overrun error circuitry are also loaded into their appropriate registers to provide output error flags when the Data Received Flag is set. If the Data Received Flag had not been reset prior to the assembly of the current character, the previous character is lost and this is indicated by a high-level output voltage on the Overrun Error Flag.

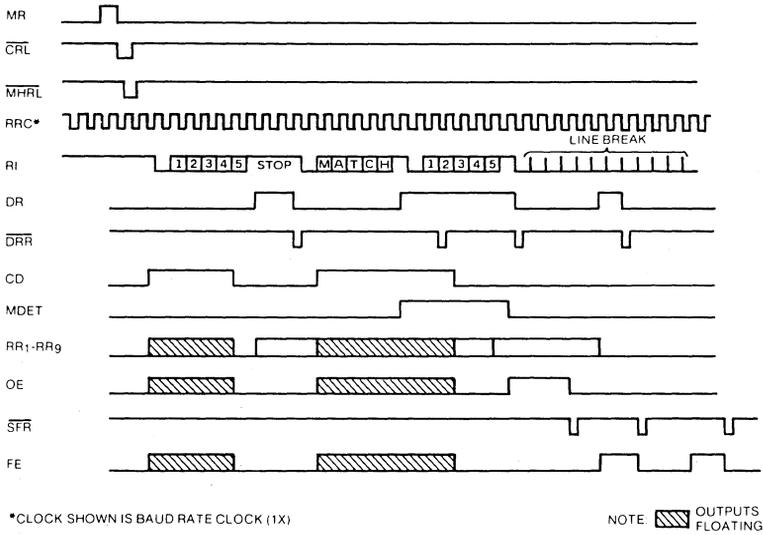
Table 2. ASYNCHRONOUS OR ISOCRONOUS MODE CONTROL DEFINITION

R	W	W				Added		
M	L	L	E			Parity	Stop	
S	S	S	P	Start	Data	Bit	Elements	
3	2	1	I	Bit	Bits			
0	0	0	0	1	5	Odd	1 or more	
0	0	0	0	1	5	Even	1 or more	
0	0	0	1	X	1	5	None	1 or more
0	0	1	0	0	1	6	Odd	1 or more
0	0	1	0	1	1	6	Even	1 or more
0	0	1	1	X	1	6	None	1 or more
0	1	0	0	0	1	7	Odd	1 or more
0	1	0	0	1	1	7	Even	1 or more
0	1	0	1	X	1	7	None	1 or more
0	1	1	0	0	1	8	Odd	1 or more
0	1	1	0	1	1	8	Even	1 or more
0	1	1	1	X	1	8	None	1 or more

↑ Set to ASYNC or ISOC Mode

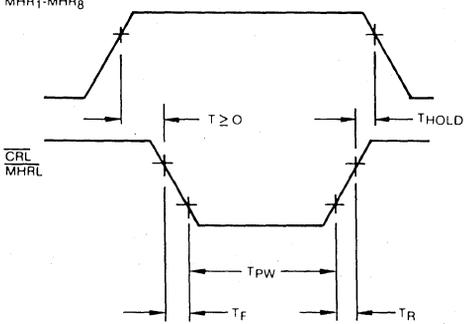
When RMS₂ is 0 (ASYNC or ISOC Mode), RMS₂ and RMS₃ determine the clock frequency according to the following table:

RMS ₂	RMS ₃	Clock Frequency
0	0	1X Baud Rate
0	1	16X Baud Rate
1	0	32X Baud Rate
1	1	64X Baud Rate

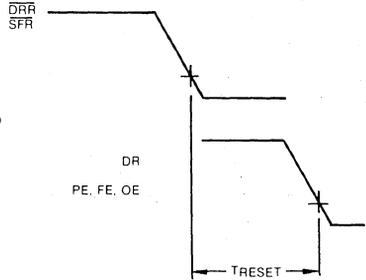


ASYNCHRONOUS & ISOCHRONOUS TIMING EXAMPLE

EPE, PI, WLS₁, WLS₂, RMS₁-RMS₃,
MHR₁-MHR₈

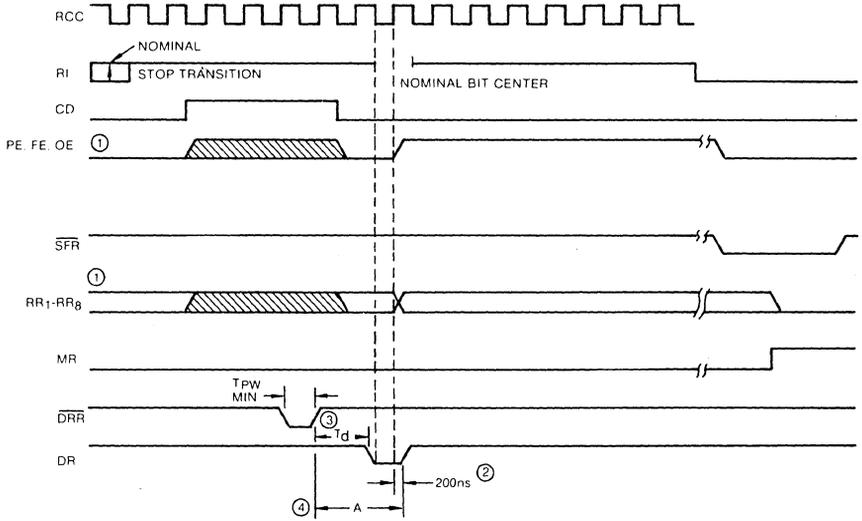


DATA INPUT LOAD CYCLE



RESET DELAY

SWITCHING WAVEFORMS



- 1 DATA AND ERROR FLAGS ARE VALID AT THE NOMINAL CENTER OF THE FIRST STOP BIT.
- 2 DR IS DELAYED 200ns FROM DATA AND ERROR FLAGS.
- 3 THE DELAY BETWEEN DRR AND DR = $T_d = 500\text{ns}$
- 4 DRR SHOULD BE HIGH A MINIMUM OF A ns ($T_d + 1/2 \text{ CLOCK} + 200\text{ns}$) PRIOR TO THE NEXT RISING EDGE OF DR

TIMING DETAIL

MAXIMUM RATINGS

V_{GG} Supply Voltage	+ 0.3V to - 20V
V_{DD} Supply Voltage	+ 0.3V to - 20V
Clock Input Voltage*	+ 0.3V to - 20V
Logic Input Voltage*	+ 0.3V to - 20V
Logic Output Voltage*	+ 0.3V to - 20V
Storage Temperature	Ceramic - 65°C to + 150°C Plastic - 55°C to + 125°C
Operating Free-Air Temperature T_A Range	0°C to + 70°C
Lead Temperature (Soldering, 10 sec)	300°C

* $V_{GG} = V_{DD} = 0V$

NOTE: These voltages are measured with respect to V_{SS} (Substrate).

ELECTRICAL CHARACTERISTICS

($V_{SS} = V_{CC} = 5V \pm 5\%$, $V_{DD} = 0V$, $V_{GG} = -12V \pm 5\%$, $T_A = 0^\circ C$ to + 70°C unless otherwise specified.)

SYMBOL	PARAMETER	MIN.	MAX.	CONDITIONS
V_{IL} V_{IH}	INPUT LOGIC LEVELS¹ Low-level Input Voltage High-level Input Voltage	$V_{SS}-1.5V$	0.8V	$V_{SS} = 4.75V$
V_{OL} V_{OH}	OUTPUT LOGIC LEVELS² Low-level Output Voltage High-level Output Voltage	$V_{SS}-1.0V$	0.4V	$V_{SS} = 5.25V$ $I_{OL} = 1.6mA$ $V_{SS} = 4.75V$ $I_{OH} = -100\mu A$
I_{IL}	INPUT CURRENT¹ Low-level Input Current (each input)		-1.6mA	$V_{SS} = 5.25V$ $V_{IN} = 0.4V$

** Not more than one output should be shorted at a time.

NOTE: 1) Inputs under Chip Disable control when disabled, (V_{IH} applied to CD), are logically disabled and appear as a single TTL Load.

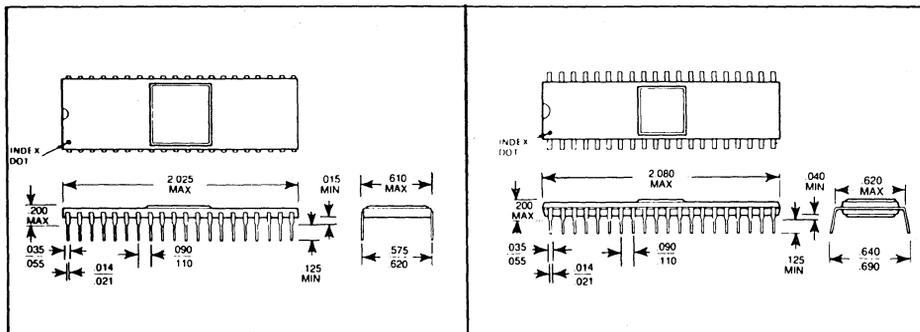
2) Outputs under Chip Disable control when disabled (V_{IH} applied to CD), are logically and electrically disconnected and caused to float. The Three-State Output has three stages;

(1) Low impedance to V_{CC} (2) Low impedance to GND (3) High impedance OFF ≈ 10 Megohm.

SWITCHING CHARACTERISTICS

($V_{SS} \cdot V_{CC} = 5V$, $V_{DD} = 0V$, $V_{GG} = -12V$, $T_A = 25^\circ C$, $C_L = 20$ pf)

SYMBOL	PARAMETER	MIN.	MAX.	CONDITIONS
F_C	Clock Frequency	DC	100 KHz	PR1472-00
	PULSE WIDTH	DC	640 KHz	PR1472-01
T_{HOLD}	Hold Time	20 nsec		
T_{CRL}	Control Register Load	250 nsec		
T_{MHRL}	Match-Character Holding Register Load	250 nsec		
T_{DRR}	Data Received Reset	200 nsec		
T_{SFR}	Status Flag Reset	200 nsec		
T_{MR}	Master Reset	500 nsec		
T_{PD}	Output Enable Delay	500 nsec		
T_R	Rise Time		150 nsec	
T_F	Fall Time		150 nsec	



PR1472A CERAMIC PACKAGE

PR1472B PLASTIC PACKAGE

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PT 1482-01 (PSAT)

Programmable Synchronous & Asynchronous Transmitter

FEATURES

- SYNCHRONOUS, ASYNCHRONOUS OR ISOCHRONOUS OPERATION
- DC TO 640K BITS/SEC, 1X CLOCK PT1482-01
- DC TO 100K BITS/SEC, 1X CLOCK PT1482
- PROGRAMMABLE MATCH (FILL) CHARACTER
- SELECTABLE 5,6,7, OR 8 BIT PER CHARACTER
- EVEN/ODD PARITY GENERATOR. PARITY INHIBIT
- PROGRAMMABLE CLOCK RATE 1X, 16X, 32X, OR 64X.
- AUTOMATIC START & STOP BIT GENERATION IN ASYNCHRONOUS & ISOCHRONOUS MODES
- PROGRAMMABLE 1 AND 2 STOP BITS, (1 1/2 IN 5 LEVEL MODE)
- AUTOMATIC CHARACTER STATUS AND DELIMITING SIGNAL GENERATION
- THREE STATE OUTPUTS — BUS STRUCTURE COMPATIBILITY
- DOUBLE BUFFERED
- TTL AND DTL COMPATIBLE — INTERNAL ACTIVE PULL UP
- COMPATIBLE RECEIVER, PR1472.

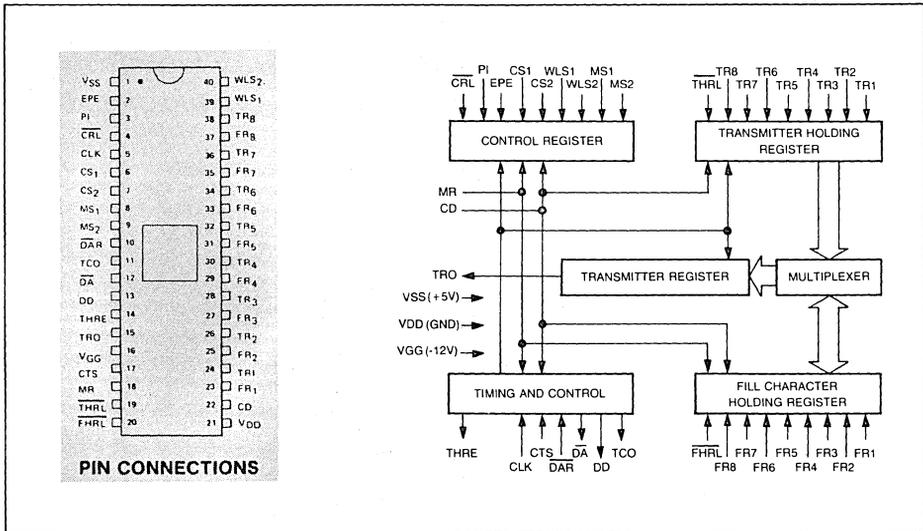
GENERAL DESCRIPTION

The Western Digital PT1482 (PSAT) is a programmable transmitter that interfaces variable length parallel data to a serial data channel. The transmitter converts parallel characters into a serial data stream with a format compatible with all standard Synchronous, Asynchronous or Isochronous data communications media.

Contiguous serial characters are transmitted in the Synchronous Mode with the automatic insertion of a programmable Fill (Idle) Character during the absence of parallel input data. Programming the Asynchronous Mode selects serial transmission with automatic insertion of Start and Stop Bits. Isochronous mode selects transmission with automatic fill character insertion during the absence of parallel input data. Four internal registers and a multiplexer, in conjunction with Three-State Output Lines, provide full system versatility.

The PSAT is a TTL compatible device. The use of internal active pull-up devices and push-pull output drivers, provides direct compatibility with all forms of current sinking logic. Western Digital also offers a compatible Receiver, PR1472.

AUGUST, 1980



PT1482 BLOCK DIAGRAM

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION																
1	V _{SS} POWER SUPPLY	V _{SS}	+ 5 Volt Supply																
2	EVEN PARITY ENABLE	EPE	A low-level input voltage, V _{IL} , applied to CD (pin 22) enables the EPE and PI Inputs.																
3	PARITY INHIBIT	PI	<p>The Even Parity Enable Input and the Parity Inhibit Input to the Control Register, in conjunction with the Control Register Load and Chip Disable, select even, odd or no parity to be generated by the Transmitter. A high-level input voltage, V_{IH}, applied to EPE selects even parity and a low-level input voltage, V_{IL}, selects odd parity if a low-level input voltage is applied to Parity Inhibit and Chip Disable.</p> <table border="1"> <thead> <tr> <th>PI</th> <th>EPE</th> <th>SELECTED PARITY</th> <th>COMMENTS</th> </tr> </thead> <tbody> <tr> <td>V_{IL}</td> <td>V_{IL}</td> <td>ODD</td> <td>CD = V_{IL}</td> </tr> <tr> <td>V_{IL}</td> <td>V_{IH}</td> <td>EVEN</td> <td>CD = V_{IL}</td> </tr> <tr> <td>V_{IH}</td> <td>X</td> <td>NONE</td> <td>CD = V_{IL}</td> </tr> </tbody> </table> <p>NOTE: IF CD = V_{IH}, NO PROGRAMMING IS PERFORMED SINCE INPUTS ARE DISABLED.</p> <p>X – either V_{IL} or V_{IH}. When programmed, the appropriate parity is generated following, and is contiguous with, the last data bit of a character, immediately preceding the stop element of asynchronous and isochronous characters.</p> <p>A high-level input voltage, V_{IH}, applied to CD disables EPE, PI, and CRL.</p>	PI	EPE	SELECTED PARITY	COMMENTS	V _{IL}	V _{IL}	ODD	CD = V _{IL}	V _{IL}	V _{IH}	EVEN	CD = V _{IL}	V _{IH}	X	NONE	CD = V _{IL}
PI	EPE	SELECTED PARITY	COMMENTS																
V _{IL}	V _{IL}	ODD	CD = V _{IL}																
V _{IL}	V _{IH}	EVEN	CD = V _{IL}																
V _{IH}	X	NONE	CD = V _{IL}																
4	CONTROL REGISTER LOAD	CRL	<p>A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the CRL input.</p> <p>A low-level input voltage, V_{IL}, applied to this line enables DC Latches of the Control Register and loads it with Control Bits (EPE, PI, CS₁, CS₂, MS₁, MS₂, WLS₁, WLS₂). A high-level input voltage, V_{IH}, applied to this line disables the Control Register. This line may be strobed or hard-wired to a low-level input voltage, V_{IL}. A high-level input voltage, V_{IH}, applied to CD, disables CRL.</p>																
5	TRANSMITTER REGISTER CLOCK	TRC	This is a fifty (50) percent duty cycle clock. The positive going edge of this Clock shifts data out of the Transmitter Register at a rate determined by the Control Bits CS ₁ and CS ₂ , and provides the basic time reference for all device functions.																
6-7	CLOCK RATE SELECT	CS ₁ -CS ₂	<p>A low-level input voltage, V_{IL}, applied to CD enables the CS₁ and CS₂ inputs. These two lines select the internal clock rate divider ratio to produce the transmitter bit rate defined by the Truth Table below:</p> <table border="1"> <thead> <tr> <th>CS₂</th> <th>CS₁</th> <th>SELECTED CLOCK INPUT RATE</th> </tr> </thead> <tbody> <tr> <td>V_{IL}</td> <td>V_{IL}</td> <td>1X BIT RATE</td> </tr> <tr> <td>V_{IL}</td> <td>V_{IH}</td> <td>16X BIT RATE</td> </tr> <tr> <td>V_{IH}</td> <td>V_{IL}</td> <td>32X BIT RATE</td> </tr> <tr> <td>V_{IH}</td> <td>V_{IH}</td> <td>64X BIT RATE</td> </tr> </tbody> </table>	CS ₂	CS ₁	SELECTED CLOCK INPUT RATE	V _{IL}	V _{IL}	1X BIT RATE	V _{IL}	V _{IH}	16X BIT RATE	V _{IH}	V _{IL}	32X BIT RATE	V _{IH}	V _{IH}	64X BIT RATE	
CS ₂	CS ₁	SELECTED CLOCK INPUT RATE																	
V _{IL}	V _{IL}	1X BIT RATE																	
V _{IL}	V _{IH}	16X BIT RATE																	
V _{IH}	V _{IL}	32X BIT RATE																	
V _{IH}	V _{IH}	64X BIT RATE																	

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION															
8-9	MODE SELECT	MS ₁ -MS ₂	<p>A high-level input voltage, V_{IH}, applied to CD disables CS₁ and CS₂.</p> <p>These lines may be strobed or hard-wired to the appropriate input voltage.</p> <p>A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the MS₁ and MS₂ inputs. These lines select the transmitter operating mode.</p> <table border="0" style="width: 100%;"> <tr> <td style="text-align: center;">MS₂</td> <td style="text-align: center;">MS₁</td> <td style="text-align: center;">MODE</td> </tr> <tr> <td>V_{IL}</td> <td>V_{IL}</td> <td>ASYNCHRONOUS — ONE STOP BIT</td> </tr> <tr> <td>V_{IL}*</td> <td>V_{IH}*</td> <td>ASYNCHRONOUS — TWO STOP BITS</td> </tr> <tr> <td>V_{IH}</td> <td>V_{IL}</td> <td>SYNCHRONOUS</td> </tr> <tr> <td>V_{IH}</td> <td>V_{IH}</td> <td>ISOCHRONOUS</td> </tr> </table> <p>*Selects 1.5 stop bits for 5-level codes.</p>	MS₂	MS₁	MODE	V _{IL}	V _{IL}	ASYNCHRONOUS — ONE STOP BIT	V _{IL} *	V _{IH} *	ASYNCHRONOUS — TWO STOP BITS	V _{IH}	V _{IL}	SYNCHRONOUS	V _{IH}	V _{IH}	ISOCHRONOUS
MS₂	MS₁	MODE																
V _{IL}	V _{IL}	ASYNCHRONOUS — ONE STOP BIT																
V _{IL} *	V _{IH} *	ASYNCHRONOUS — TWO STOP BITS																
V _{IH}	V _{IL}	SYNCHRONOUS																
V _{IH}	V _{IH}	ISOCHRONOUS																
10	DATA NOT AVAILABLE RESET	$\overline{\text{DAR}}$	<p>A high-level input voltage, V_{IH}, applied to CD disables MS₁ and MS₂.</p> <p>A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the $\overline{\text{DAR}}$ input. A low-level input voltage, V_{IL}, applied to this line resets the Data Not Available Flag. A high-level Input, V_{IH}, applied to CD disables $\overline{\text{DAR}}$. This input is not used during asynchronous operation.</p>															
11	TRANSMITTER CLOCK OUTPUT	TCO	<p>This output is a clock at the transmitted bit rate. The negative going edge of this clock corresponds to the center of each transmitted data bit. The positive going edge corresponds to the start of each data bit transmission. All waveforms in this specification are referenced to TCO.</p>															
12	DATA NOT AVAILABLE FLAG	$\overline{\text{DA}}$	<p>A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the $\overline{\text{DA}}$ input. A high-level output voltage, V_{OH}, on this line indicates that a Fill-Character has been transmitted, since a character was not loaded into the Transmitter Holding Register by the center of the last bit of a Synchronous Character or the center of the Stop Element of an Isochronous character. A high-level input voltage, V_{IH}, applied to CD disables $\overline{\text{DA}}$. This input is not used during asynchronous operation.</p>															
13	DATA DELIMIT/ END OF CHARACTER	DD/EOC	<p>During asynchronous operation, a high-level output voltage, V_{OH}, indicates data is being transmitted. A low-level output voltage, V_{OL}, indicates that a Start or Stop Element is being transmitted.</p> <p>A low-level output voltage during synchronous operation indicates that the last bit of a character is being transmitted.</p>															



PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
14	TRANSMITTER HOLDING REGISTER EMPTY	THRE	A low-level input voltage applied to CD (pin 22) enables the THRE input. A high-level output voltage, V_{OH} , on this line indicates the Transmitter Holding Register is empty and has transferred its contents to the Transmitter Register and may be loaded with a new character. This line goes to a low-level output voltage, V_{OL} , when THRL goes to a low-level input voltage, V_{IL} . A high-level input voltage, V_{IH} , applied to CD disables THRE.
15	TRANSMITTER REGISTER OUTPUT	TRO	The contents of the Transmitter Holding Register are serially shifted out as an NRZ waveform on this line provided that a character was loaded into the Transmitter Holding Register prior to \overline{DA} Flag (in Synchronous or Isochronous Modes). If a character was not loaded prior to a \overline{DA} Flag, the contents of the Fill-Character Register are transmitted as the next character.
16	V_{GG} POWER SUPPLY	V_{GG}	- 12 Volts Supply.
17	CLEAR-TO-SEND	CTS	The Clear-To-Send Control initiates or disables transmission as a function of the state of this line. A high-level input voltage, V_{IH} , initiates serial data transmission provided a character has been loaded into the Transmitter Holding Register. A low-level input voltage, V_{IL} , applied to this line during transmission allows completion of that character only, after which the output will continue to mark until a high-level input voltage is applied.
18	MASTER RESET	MR	The rising edge of a high-level input voltage, V_{IH} , applied to this line resets timing and control logic to an idle state, sets THRE, the contents of the Fill-Character Holding Register, and TRO to a high-level output voltage, V_{OH} .
19	<u>TRANSMITTER HOLDING REGISTER LOAD</u>	\overline{THRL}	A low-level input voltage, V_{IL} , applied to CD (pin 22) enables the \overline{THRL} input. A low-level input voltage, V_{IL} , applied to this line enables DC Latches of the Transmitter Holding Register and loads it with the Transmitter Holding Register data and forces THRE to a low-level output voltage, V_{OL} . A high-level input voltage, V_{IH} , applied to this line disables the Transmitter Holding Register. A high-level input voltage, V_{IH} , applied to CD disables \overline{THRL} .
20	<u>FILL-CHARACTER HOLDING REGISTER LOAD</u>	\overline{FHRL}	A low-level input voltage, V_{IL} , applied to CD (pin 22) enables the \overline{FHRL} input. A low-level input voltage, V_{IL} , applied to this line enables DC Latches of the Fill-Character Holding Register and loads it with the Fill-Character Register data FR_1 - FR_8 . A high-level input voltage, V_{IH} , applied to this line disables the \overline{FHRL} Register. This line may be strobed or hard-wired to a low-

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION																					
21	V _{DD} POWER SUPPLY	V _{DD}	<p>level input voltage, V_{IL}. This input is not used during asynchronous operation.</p> <p>A high-level input voltage, V_{IH}, applied to CD disables FHRL.</p> <p>Ground.</p>																					
22	CHIP DISABLE	CD	<p>This line controls the disconnect associated with busable inputs and Three-State outputs. A high-level input voltage, V_{IH}, applied to this line removes drive from push-pull outputs causing them to float. Drivers of disabled inputs are required to sink or source current. The I/O Lines controlled by Chip Disable are defined below:</p> <table border="0" data-bbox="516 557 932 703"> <thead> <tr> <th colspan="2" style="text-align: left;">INPUT LINES</th> <th style="text-align: left;">TRI-STATE OUTPUT LINES</th> </tr> </thead> <tbody> <tr> <td>CRL</td> <td>THRL</td> <td>DA</td> </tr> <tr> <td>EPE</td> <td>FHRL</td> <td>THRE</td> </tr> <tr> <td>PI</td> <td>FR₁-FR₈</td> <td></td> </tr> <tr> <td>CS₁-CS₂</td> <td>TR₁-TR₈</td> <td></td> </tr> <tr> <td>MS₁-MS₂</td> <td>WLS₁, WLS₂</td> <td></td> </tr> <tr> <td colspan="3">DAR</td> </tr> </tbody> </table>	INPUT LINES		TRI-STATE OUTPUT LINES	CRL	THRL	DA	EPE	FHRL	THRE	PI	FR ₁ -FR ₈		CS ₁ -CS ₂	TR ₁ -TR ₈		MS ₁ -MS ₂	WLS ₁ , WLS ₂		DAR		
INPUT LINES		TRI-STATE OUTPUT LINES																						
CRL	THRL	DA																						
EPE	FHRL	THRE																						
PI	FR ₁ -FR ₈																							
CS ₁ -CS ₂	TR ₁ -TR ₈																							
MS ₁ -MS ₂	WLS ₁ , WLS ₂																							
DAR																								
23, 25 27, 29 31, 33 35, 37	FILL-CHARACTER HOLDING REGISTER DATA INPUTS	FR ₁ -FR ₈	<p>A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the inputs of the Fill-Character Holding Register and associated Load Strobe, FHRL. Parallel 8-bit characters are input into the Fill-Character Holding Register with the FHRL Strobe (pin 20). If a character of less than 8 bits has been selected (by WLS₁ and WLS₂) only the least significant bits are accepted. These lines may be strobed or hard-wired to the appropriate input voltage. These inputs are not used during asynchronous operation.</p> <p>During Synchronous or Isochronous transmission, the Fill-Character is transmitted if a character was not loaded into the Transmitter Holding Register prior to a DA Flag; i.e., the Transmitter Holding Register did not contain a character at the center of the last bit being transmitted from the Transmitter Register. A high-level input voltage, V_{IH}, will cause a high-level output voltage, V_{OH}, to be transmitted, Least Significant Bit (FR₁) to Most Significant Bit (FR_n) order.</p> <p>A high-level input voltage, V_{IH}, applied to CD disables FR₁-FR₈.</p>																					
24, 26 28, 30 32, 34 36, 38	TRANSMITTER HOLDING REGISTER DATA INPUTS	TR ₁ -TR ₈	<p>A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the inputs to the Transmitter Holding Register and associated Load Strobe, THRL. If a character of less than 8 bits has been selected (by WLS₁ and WLS₂), only the least significant bits are accepted. A high-level input</p>																					

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION															
39-40	WORD LENGTH	WLS ₁ -WLS ₂	<p>voltage, V_{IH}, will cause a high-level output voltage to be transmitted, Least Significant Bit (TR₁) to Most Significant Bit (TR_n) order. A high-level input voltage, V_{IH}, applied to CD disables TR₁-TR₈.</p> <p>A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the inputs of the Control Register and Load, CRL. Parallel 8-bit characters are input into the Control Register with the CRL Strobe (pin 4), WLS₁ and WLS₂ select the transmitted character length from five (5) to eight (8) bits defined by the Truth Table below:</p> <table border="1"> <thead> <tr> <th>WLS₂</th> <th>WLS₁</th> <th>SELECTED WORD LENGTH</th> </tr> </thead> <tbody> <tr> <td>V_{IL}</td> <td>V_{IL}</td> <td>5 BITS</td> </tr> <tr> <td>V_{IL}</td> <td>V_{IH}</td> <td>6 BITS</td> </tr> <tr> <td>V_{IH}</td> <td>V_{IL}</td> <td>7 BITS</td> </tr> <tr> <td>V_{IH}</td> <td>V_{IH}</td> <td>8 BITS</td> </tr> </tbody> </table> <p>A high-level input voltage, V_{IH}, applied to CD disables WLS₁ and WLS₂, forcing them to float.</p>	WLS ₂	WLS ₁	SELECTED WORD LENGTH	V _{IL}	V _{IL}	5 BITS	V _{IL}	V _{IH}	6 BITS	V _{IH}	V _{IL}	7 BITS	V _{IH}	V _{IH}	8 BITS
WLS ₂	WLS ₁	SELECTED WORD LENGTH																
V _{IL}	V _{IL}	5 BITS																
V _{IL}	V _{IH}	6 BITS																
V _{IH}	V _{IL}	7 BITS																
V _{IH}	V _{IH}	8 BITS																

ORGANIZATION

PT1482 block diagram is illustrated on page 1.

Control Register — Programming of the PSAT is accomplished by loading the 8 Bit Control Register. Mode selection, clock divisor, word length, and parity are selected when the Control Register Load signal is activated.

Transmitter Register — The Transmitter Register is used to store the outgoing data stream. The contents of this register are derived from either the Transmitter Holding Register or the Fill (Match) Character Holding Register with the Control and Timing Logic automatically adding the required start and stop bits during Asynchronous and Isochronous Modes.

Transmitter Holding Register — The Transmitter Holding Register, a buffer register, is used to store the parallel character to be serially transmitted.

Fill Character Holding Register — The Fill Character Holding Register is used to store the Fill (Match) Character which is transmitted during the absence of characters in the Transmitter Holding Register.

Timing and Control — The Timing and Control Logic generates the required control signals to transmit Data and Fill Characters. Character transmission status signals are also derived from this logic.

SYNCHRONOUS MODE OPERATION

Synchronous transmission requires that characters

(programmably variable from 5 to 8 data bits plus parity) are contiguous with no start or stop bits. Since the requirement that characters are contiguous does not imply that the system servicing the transmitter always has ample time to load the Transmitter Holding Register, it is necessary that a character be transmitted when data has not been loaded into the Transmitter Holding Register. This character is defined as the Fill or Idle Character and a separate register has been provided to load this character upon initialization. The Fill-Character Holding Register is loaded by strobing the Fill-Character Holding Register Load (FHRL) line or hard-wiring it to a low-level input voltage.

Referring the Block Diagram of the Transmitter, it can be seen that the Chip Disable (CD) enables or disconnects various inputs and outputs of the P/SAT. The inputs to the Control Register, Transmitter Holding Register, Fill-Character Holding Register and their respective load strobes, CRL, THRL, and FHRL are under CD control. In addition, the Transmitter Holding Register Empty (THRE) Flag, Data Not Available (DA) Flag, and the Data Not Available Reset (DAR) are also controlled by CD. It is necessary that CD enable these lines to allow strobing information into these registers and to allow examination of these output flags. The P/SAT will enter a defined "idle" state when the Master Reset (MR) is strobed to a high-level input voltage. In this state, all timing and control logic are reset, the Transmitter Register Output continues to mark, the Transmitter Holding Register Flag is set to a high-level output voltage, the Data Delimit/End of Character (DD/EOC) Flag

is set to a low-level output voltage, and the contents of the Fill-Character Holding Register are forced to a high-level output voltage.

When the P/SAT is enabled by CD, loading the Control Register by strobing the Control Register Load (CRL) line to a low-level input voltage, defines the mode of operation, character length, selected parity if required, and the clock rate selection. Table 1 illustrates all the programmable synchronous character formats.

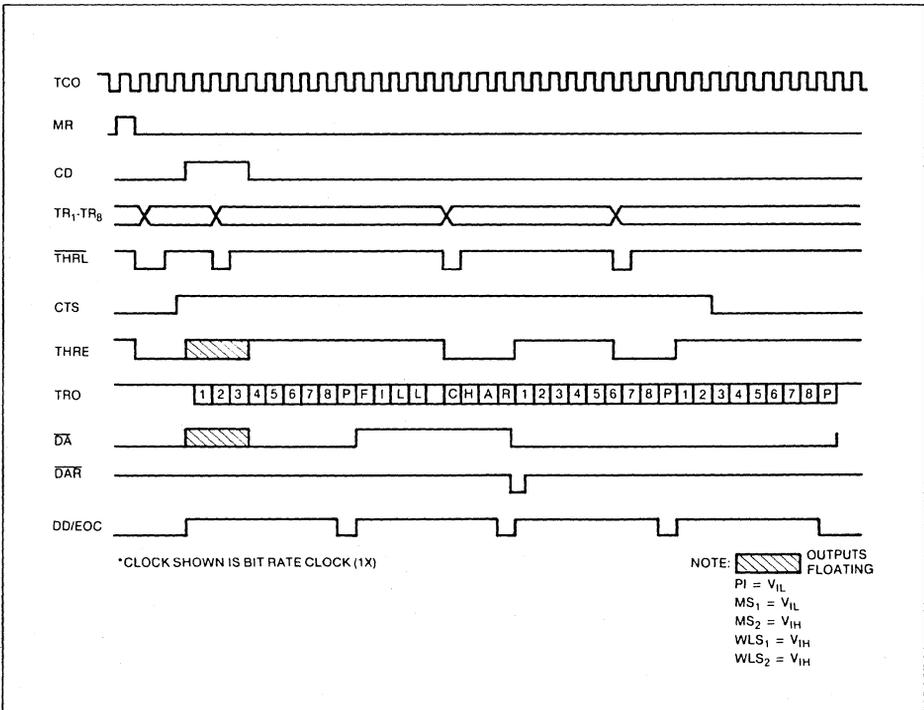
To initialize transmission the CTS signal must be set to a high state and the transmitter holding register must be loaded with a character to be transmitted. The transmitter will remain in an idle state until this is accomplished.

The character transferred into the Transmitter Register (from the Transmitter Holding Register or the Fill-Character Holding Register) is determined at the center of the last bit of the character being transmitted. If, at this time, no character has been loaded into the Transmitter Holding Register, the Fill-Character is loaded into the Transmitter Register at the end of the bit being transmitted

Table 1. SYNC MODE CONTROL DEFINITION

CONTROL WORD						CHARACTER FORMAT	
M	M	L	L	E		DATA	ADDED
S	S	S	S	P	P	BITS	PARITY
2	1	2	1	1	E		BIT
1	0	0	0	0	0	5	ODD
1	0	0	0	0	1	5	EVEN
1	0	0	0	1	X	5	NONE
1	0	0	1	0	0	6	ODD
1	0	0	1	0	1	6	EVEN
1	0	0	1	1	X	6	NONE
1	0	1	0	0	0	7	ODD
1	0	1	0	0	1	7	EVEN
1	0	1	0	1	X	7	NONE
1	0	1	1	0	0	8	ODD
1	0	1	1	0	1	8	EVEN
1	0	1	1	1	X	8	NONE

↑
Sets to SYNC Mode



SYNCHRONOUS TIMING EXAMPLE



and a Data Not Available ($\overline{\text{DA}}$) Flag is set to a high-level output voltage. This Fill-Character will be repeatedly transmitted until a character is loaded into the Transmitter Holding Register, at which time, the Data Not Available Flag is reset, the Fill-Character will be completed and the newly loaded synchronous character will follow contiguously.

A high-level output voltage, on the THRE Flag indicates that the Transmitter Holding Register is empty and may be loaded with a character. Data on the inputs of the Transmitter Holding Register is loaded when the Transmitter Holding Register Load (THRL) line is strobed to a low-level input voltage, forcing the THRE Flag to a low-level output voltage. This data must be stable prior to THRL going to a high-level input voltage since this register is a set of DC latches which are enabled by THRL.

If the Clear-To-Send (CTS) line is at a low-level input voltage, or if the Transmitter Register is in the process of transmitting a character, the character in the Transmitter Holding Register will not be transferred down to the Transmitter Register and the THRE Flag will remain at a low-level output voltage. Raising the CTS line to a high-level input voltage or completion of transmission of a character from the Transmitter Register causes the automatic transfer of the character in the Transmitter Holding Register to the Transmitter Register which forces the THRE Flag to be set to high-level output voltage. The selected parity is added to the data during the transfer to the Transmitter Register and serial transmission is initiated as an NRZ waveform. A low-level input voltage applied to CTS during transmission allows completion of that character only, after which the device enters the idle state and the output will continue to mark until a high-level input voltage is applied.

The Data Delimit/End of Character Flag has been provided to indicate the transmission of serial data on the Transmitter Register Output. The Data Delimit/End of Character Flag is defined as a low-level output voltage during transmission of the last bit of a synchronous character and when the P/SAT is in the "idle" state.

ASYNCHRONOUS MODE OPERATION

An asynchronous character consisting of a start bit, followed by data (programmably variable from 5 to 8 data bits), parity (if so programmed), and a stop "element" is serially transmitted, in that order, as an NRZ waveform by the P/SAT. The stop interval is referred to as an "element" since its minimum length is under program control and may be 1 or 2 bits in length. When programmed for 2 stop bits, a 5-level (bit) code will be transmitted with 1.5 stop bits.

Referring to the Block Diagram of the Transmitter, it can be seen that the Chip Disable enables or

disconnects various inputs and outputs of the P/SAT. The inputs to the Control Register, Transmitter Holding Register, Fill-Character Holding Register and their respective load strobes, $\overline{\text{CRL}}$, THRL and FHRL are under CD control. In addition, the Transmitter Holding Register Empty Flag (THRE), the Data Not Available Flag ($\overline{\text{DA}}$), and the Data Not Available Reset ($\overline{\text{DAR}}$) are also controlled by CD. It is necessary that CD enable these lines to allow strobing information into these registers and to allow examination of these output flags. It should be noted that the Fill-Character Holding Register and its associated load strobe, FHRL, the Data Not Available Flag and its associated reset, $\overline{\text{DAR}}$, play no role in asynchronous communications and are only mentioned here for completeness.

The P/SAT will enter a defined "idle" state when the Master Reset (MR) line is strobed to a high-level input voltage. In this state, all timing and control logic are reset, the Transmitter Register Output continues to mark, the Transmitter Holding Register Empty Flag is set to a high-level output voltage, V_{OH} , and the Data Delimit/End of Character (DD/EOC) Flag is reset to a low-level output voltage.

When the transmitter is enabled by CD, loading the Control Register by strobing the Control Register Load ($\overline{\text{CRL}}$) line to a low-level input voltage, V_{IL} , defines the mode of operation, character length, selected parity if required and the clock rate selection. Table 2 illustrates all the programmable asynchronous formats.

Continuous transmission, transmission of characters with the minimum number of stop bits programmed, is accomplished by loading the Transmitter Holding Register within a character time of when its "Empty Flag" becomes a high-level output voltage. A high-level output voltage, V_{OH} , on the Transmitter Holding Register Empty (THRE) Flag indicates that the Transmitter Holding Register is empty and may be loaded with a character. Data on the inputs of the Transmitter Holding Register is loaded when the Transmitter Holding Register Load (THRL) line is strobed to a low-level input voltage, V_{IL} , forcing the THRE Flag to a low-level output voltage, V_{OL} . This data must be stable prior to THRL going to a high-level input voltage since this register is a set of DC latches which are enabled by THRL. If the Clear-To-Send (CTS) line is at a low-level input voltage or if the Transmitter Register is in the process of transmitting a character, the character in the Transmitter Holding Register will not be transferred down to the Transmitter Register and the THRE Flag will remain at a low-level output voltage. Raising the CTS line to a high-level input voltage or completion of transmission of a character from the Transmitter Register causes the automatic transfer of the character in the Transmitter Holding Register to the Transmitter Register and the THRE flag will be set to a high-level output voltage.

The start bit, selected parity and stop bit(s), determined by the Control Register programming, are added to the data during the transfer to the Transmitter Register and serial transmission is initiated as an NRZ waveform.

A low-level input voltage, applied to GTS during transmission, allows completion of that character only, after which the output will continue to mark until a high-level input voltage is applied.

The Data Delimit/End of Character Flag has been provided to indicate the transmission of serial data on the Transmitter Register Output. Data Delimit is a low-level output voltage during start and stop bits and is a high-level output voltage during transmission of data and parity. Neither TRO, CTS nor DD/EOC is under control of Chip Disable.

Table 2. ASYNC MODE CONTROL DEFINITION

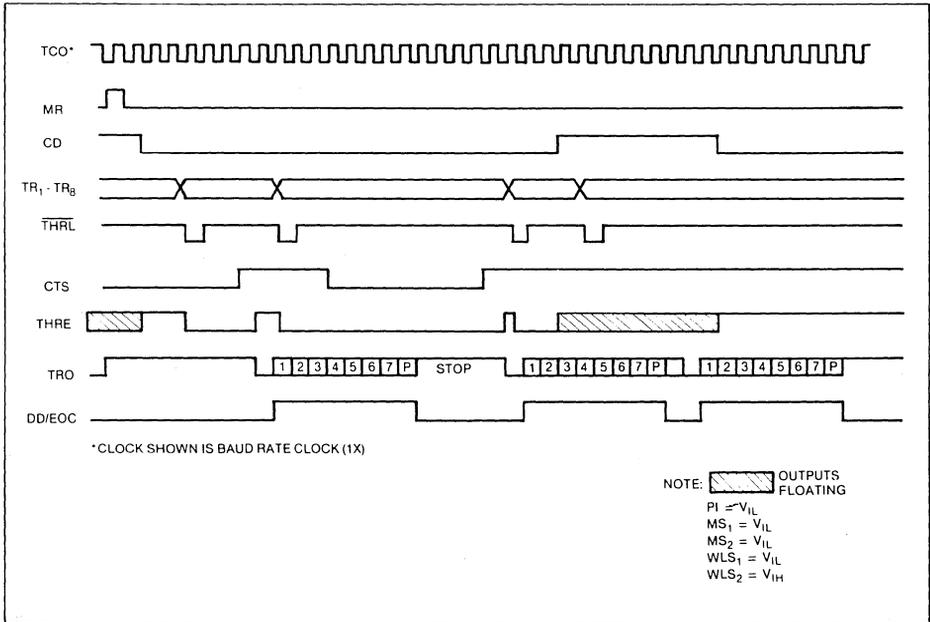
CONTROL WORD					CHARACTER FORMAT			
M	W	L	L	E	START BIT	DATA BITS	ADDED PARITY BIT	STOP ELEMENTS
S	S	S	S	P				
0	0	0	0	0	1	5	ODD	1
0	1	0	0	0	1	5	ODD	1.5
0	0	0	0	1	1	5	EVEN	1
0	1	0	0	1	1	5	EVEN	1.5
0	0	0	0	1X	1	5	NONE	1
0	1	0	0	1X	1	5	NONE	1.5
0	0	0	1	0	1	6	ODD	1
0	1	0	1	0	1	6	ODD	2
0	0	0	1	0	1	6	EVEN	1
0	1	0	1	0	1	6	EVEN	2
0	0	0	1	1X	1	6	NONE	1
0	1	0	1	1X	1	6	NONE	2
0	0	1	0	0	1	7	ODD	1
0	1	1	0	0	1	7	ODD	2
0	0	1	0	0	1	7	EVEN	1
0	1	1	0	0	1	7	EVEN	2
0	0	1	0	1X	1	7	NONE	1
0	1	1	0	1X	1	7	NONE	2
0	0	1	1	0	1	8	ODD	1
0	1	1	1	0	1	8	ODD	2
0	0	1	1	0	1	8	EVEN	1
0	1	1	1	0	1	8	EVEN	2
0	0	1	1	1X	1	8	NONE	1
0	1	1	1	1X	1	8	NONE	2

↑
Sets to ASYNC Mode

ISOCRONOUS MODE OPERATION

In the Isochronous Mode of operation all (Synchronous Mode) definitions apply with the exception of those for the Data Delimit/End of Character (DD/EOC) Flag and the Data Not Available Flag (DA).

This is the case since Isochronous Data Transmission requires contiguous characters with the addition of a start and a single stop bit added to each character.



ASYNCHRONOUS TIMING EXAMPLE

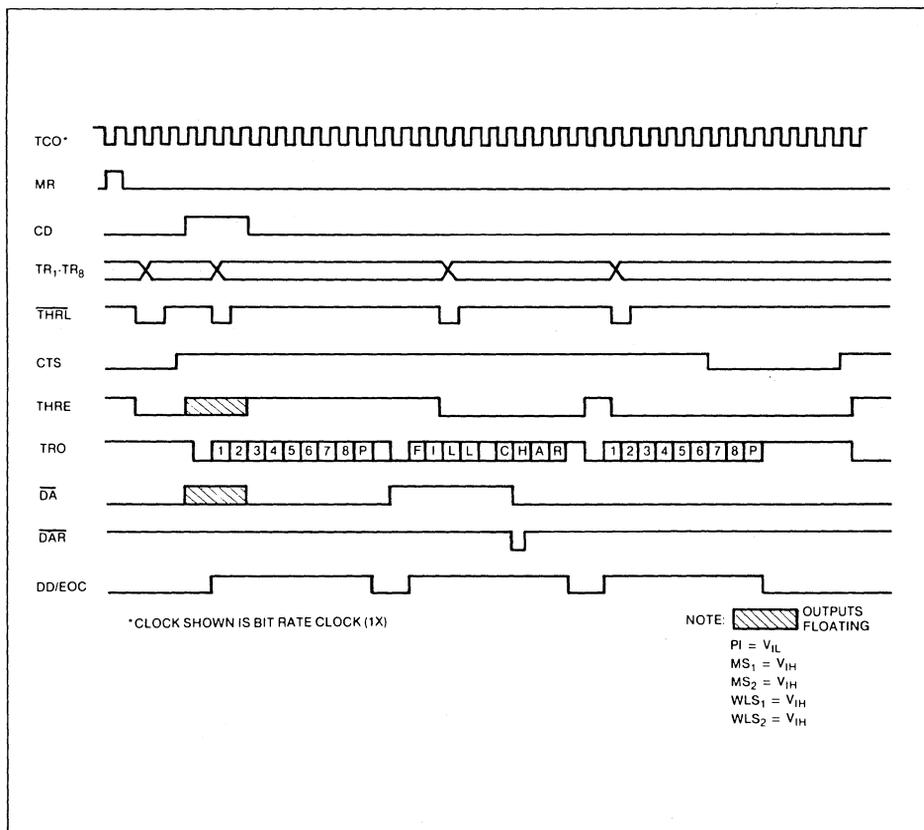
The Data Delimit/End of Character Flag is a low-level output voltage during start and stop bits and is a high-level output voltage during transmission of data and parity. The Data Not Available Flag (DA) is set to a high-level output voltage at the end of the stop bit if a character has not been loaded into the Transmitter Holding Register at the center of the stop bit. The contents of the Fill-Character Holding Register will be transferred into the Transmitter Register and repeatedly transmitted until a character is loaded into the Transmitter Holding Register. At this time, the Fill-Character will be completed and the newly loaded isochronous character will follow contiguously.

Table 3 illustrates all the programmable isochronous character formats.

Table 3. ISOC MODE CONTROL DEFINITION

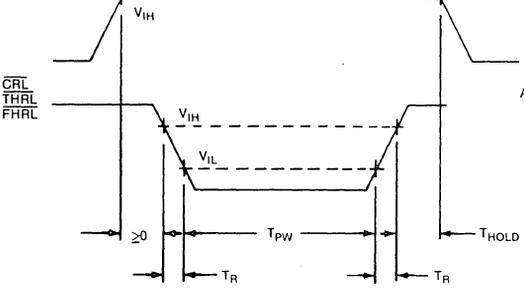
CONTROL WORD						CHARACTER FORMAT			
M	M	W	L	L	E	START BIT	DATA BITS	ADDED PARITY BIT	STOP ELEMENTS
S	S	S	S	P	P				
1	1	0	0	0	0	1	5	ODD	1
1	1	0	0	0	1	1	5	EVEN	1
1	1	0	0	1	X	1	5	NONE	1
1	1	0	1	0	0	1	6	ODD	1
1	1	0	1	0	1	1	6	EVEN	1
1	1	0	1	1	X	1	6	NONE	1
1	1	1	0	0	0	1	7	ODD	1
1	1	1	0	0	1	1	7	EVEN	1
1	1	1	0	1	X	1	7	NONE	1
1	1	1	1	0	0	1	8	ODD	1
1	1	1	1	0	1	1	8	EVEN	1
1	1	1	1	1	X	1	8	NONE	1

↑
Sets to ISOC Mode

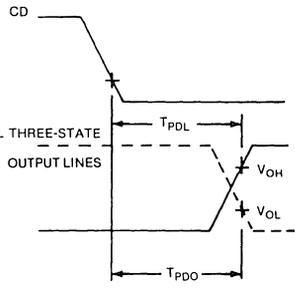


ISOCRONOUS TIMING EXAMPLE

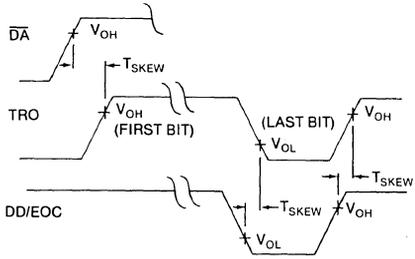
EPE, PI, CS₁, CS₂, MS₁, MS₂, WLS₁, WLS₂
 TR₁-TR₈
 FR₁-FR₈



DATA INPUT LOAD CYCLE

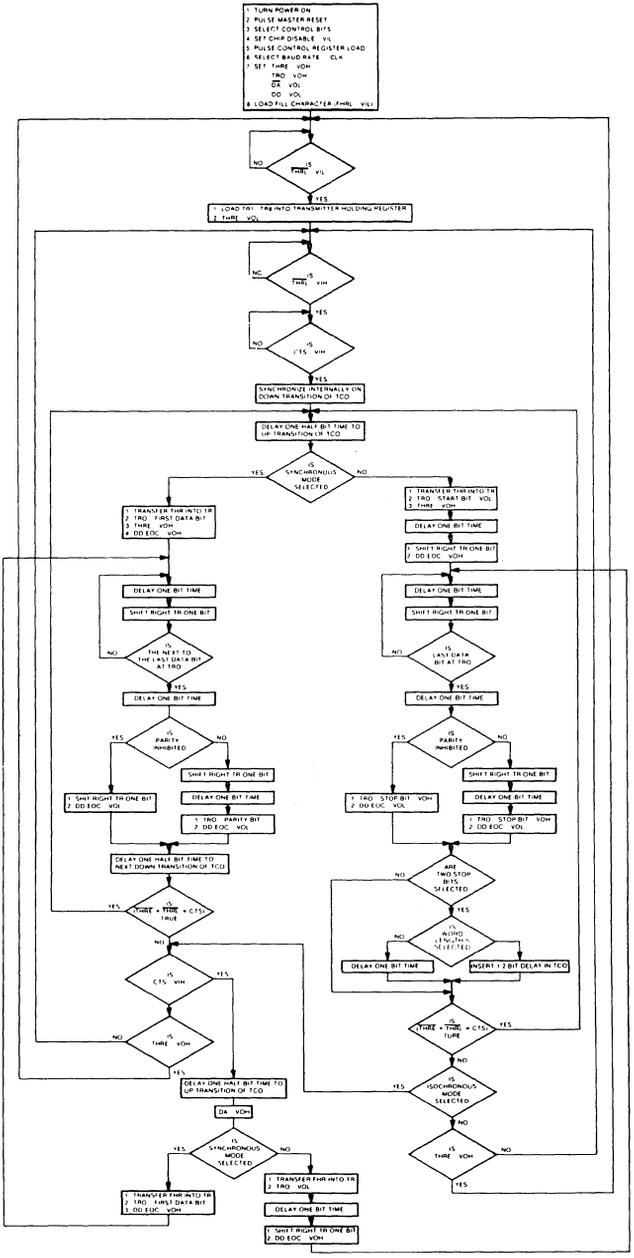


OUTPUT ENABLE DELAYS

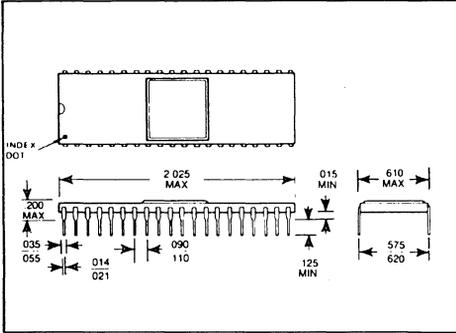


SKREW TIMES

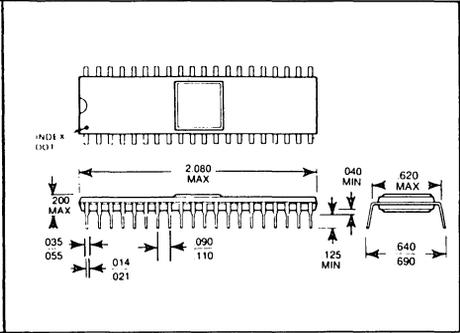
SWITCHING WAVEFORMS



PT1482 SYNCHRONOUS ASYNCHRONOUS TRANSMITTER FLOW CHART



PT1482A CERAMIC PACKAGE



PT1482B PLASTIC PACKAGE

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WESTERN DIGITAL
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3128 REDHILL AVENUE, BOX 2180
NEWPORT BEACH, CA 92663 (714) 557-3550, TWX 910-595-1139

FR1502 Series First-In/First-Out Buffer Register

FEBRUARY, 1981

FEATURES

- 40 CHARACTERS BY 9 BITS
- EXPANDABLE CHARACTER AND BIT SIZE (CASCADE CAPABILITY)
- DC TO 1 MHz ASYNCHRONOUS I/O ACCESS
- INPUT/OUTPUT READY STATUS FLAGS
- THREE STATE OUTPUTS
- SEPARATE INPUT AND OUTPUT ENABLES
- DIRECTLY TTL COMPATIBLE
- MASTER RESET
- NO EXTERNAL CLOCKS REQUIRED
- 28-PIN DIP PLASTIC OR CERAMIC PACKAGE

APPLICATIONS

- POINT OF SALE TERMINALS
- DATA TRANSMISSION BUFFER
- LINE PRINTER INPUT BUFFER
- KEY-TO-TAPE/KEY-TO-DISC EQUIPMENT
- CARD/TAPE READERS
- AUTO DIALERS
- CRT BUFFER MEMORY
- CONTROL STACK SILO ORIENTED MACHINES
- COMPUTER/TERMINALS I/O INTERFACE BUFFER
- TELEPRINTER BUFFER

GENERAL DESCRIPTION

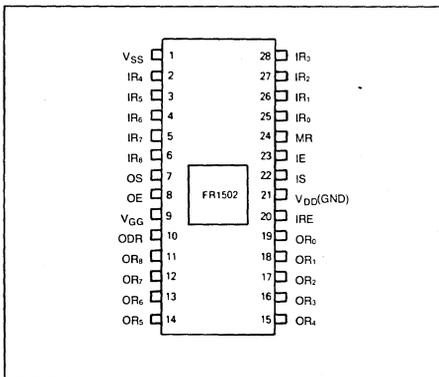
The FIFO (First-In/First-Out) Storage Chip is an asynchronous memory organized in a nine-bit by forty-character stack. Characters are loaded at the top of the stack and then "sink" to the bottom of the stack, or to the level of previously entered data, without external clocks being applied. As a character is taken from the bottom of the stack, all of the previously loaded characters will automatically propagate toward the output (bottom of stack).

Data can be entered whenever the INPUT REGISTER EMPTY line is high by strobing INPUT STROBE. The INPUT ENABLE line must also be high while strobing. The INPUT STROBE resets INPUT REGISTER EMPTY and latches the input data. As soon as this data is latched, INPUT REGISTER EMPTY will again go high and additional data can be loaded.

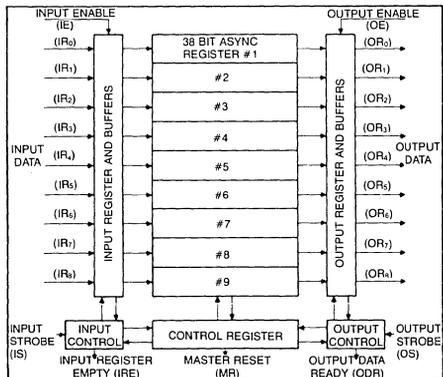
When data reaches the FIFO output, the OUTPUT DATA READY line will go high. The data is then valid at the outputs (providing the OUTPUT ENABLE line is high). The falling edge of the OUTPUT STROBE causes the OUTPUT DATA READY line to go low and to shift new data into the output register. When the new data is available, the OUTPUT DATA READY signal again goes high.

The FIFO output data lines are in high impedance state whenever the OUTPUT ENABLE line is low.

The logic conventions and internal delays designed into the FIFO allow direct expansion of the memory without external hardware (Cascade Mode).



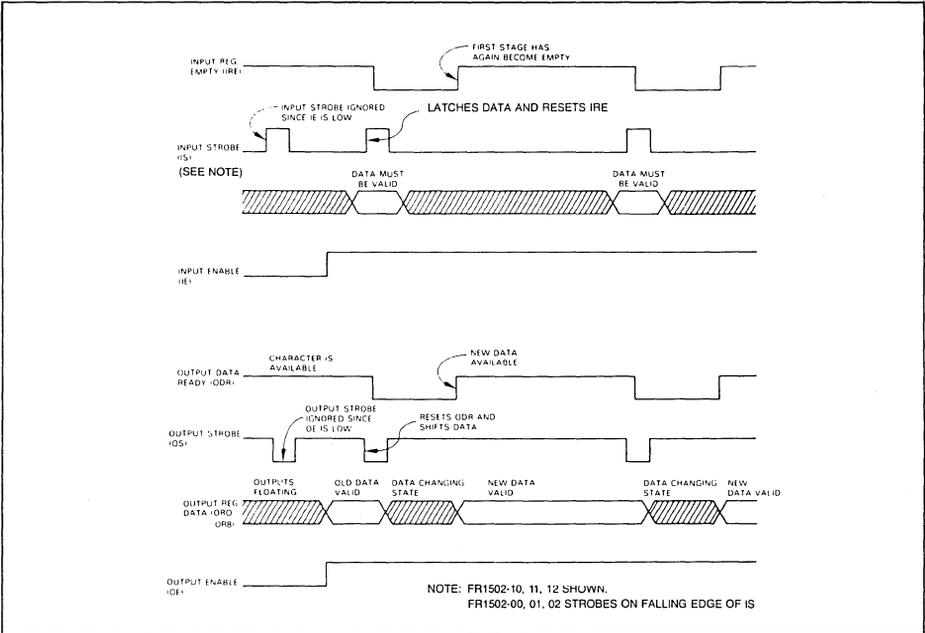
PIN CONNECTIONS



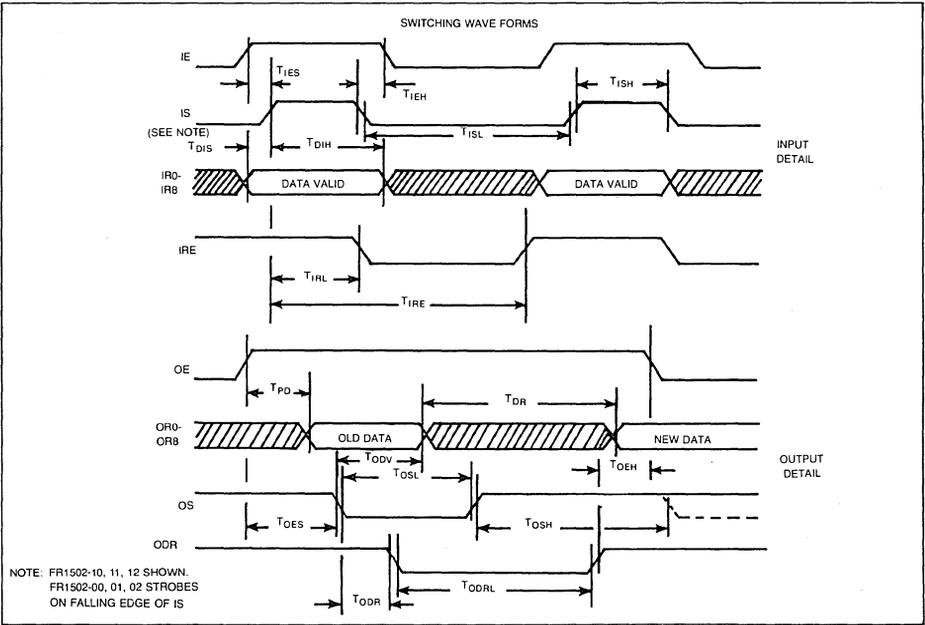
BLOCK DIAGRAM

INTERFACE SIGNALS DESCRIPTIONS

PIN NUMBER	SIGNAL NAME	SYMBOL	FUNCTION
25-28, 2-6	INPUT REGISTER FR1502-00 -01 -02	IR0- IR8	Input data lines. These are input (but not latched) to the FIFO when the Input Enable and Input Strobe are active (high).
	FR1502-10 -11 -12	IR0- IR8	Input data lines. These are input (but not latched) to the FIFO independently of the Input Enable or Input Strobe.
20	INPUT REGISTER EMPTY FR1502-00 -01 -02	IRE	When high, indicates that data can be loaded into the FIFO. It is reset to a low by falling edge of the Input Strobe.
	FR1502-10 -11 -12	IRE	When high, indicates that data can be loaded into the FIFO. It is reset to a low by a rising edge of the Input Strobe.
22	INPUT STROBE FR1502-00 -01 -02	IS	Latches input data in the FIFO on a falling edge.
	FR1502-10 -11 -12	IS	Latches input data in the FIFO on a rising edge.
24	MASTER RESET	MR	When high, clears the FIFO control registers. This leaves the OUTPUT REGISTER DATA (OR0-OR8) in an undefined state, sets INPUT REGISTER EMPTY (IRE) to high and resets OUTPUT DATA READY (ODR) to low.
19-11	OUTPUT REGISTER DATA	OR0- OR8	Three state data outputs. When OE is low, the outputs are in the high impedance state. When OE is high, these lines present the previous latched data in a first-in/first-out manner.
10	OUTPUT DATA READY	ODR	ODR is high when data is latched and available at the data output lines. Is reset to low by the falling edge of OUTPUT STROBE (OS) if OUTPUT ENABLE (OE) is high.
7	OUTPUT STROBE	OS	A falling edge of this signal resets the OUTPUT DATA READY (ODR) line and then shifts the data one step towards the output if OUTPUT ENABLE (OE) is high.
23	INPUT ENABLE FR1502-00 -01 -02	IE	When high, enables the Input Register and Input Control logic. When INPUT STROBE (IS) is high, the input data will be transferred into the FIFO. IS can then be used to latch the data.
	FR1502-10 -11 -12	IE	When high, enables the Input Control Logic. At any state of IE or IS, the input data will be transferred into the FIFO, but can not be latched unless IE is high.
8	OUTPUT ENABLE	OE	When low, OE puts the output lines (OR0-OR8) in high impedance state. When high, the output lines present the output data.
1	V _{SS} POWER SUPPLY	V _{SS}	+5VDC
21	V _{DD} POWER SUPPLY	V _{DD}	0 Volt—GND
9	V _{GG} POWER SUPPLY	V _{GG}	-12VDC



SWITCHING CHARACTERISTICS



SWITCHING WAVE FORMS

ABSOLUTE MAXIMUM RATINGS

V_{GG} Supply Voltage	+0.3V to -20V
V_{DD} Supply Voltage	+0.3V to -20V
Clock Input Voltage*	+0.3V to -20V
Logic Input Voltage*	+0.3V to -20V
Logic Output Voltage*	+0.3V to -20V
Storage Temperature (Ceramic)	-65°C to +150°C
Storage Temperature (Plastic)	-55°C to +125°C
* $V_{GG} = V_{DD} = 0V$	

NOTE: These voltages are measured with respect to V_{SS} (Substrate)

ELECTRICAL CHARACTERISTICS

($V_{SS} = +5V \pm 5\%$; $V_{DD} = 0V$; $V_{GG} = -12V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$ unless otherwise specified)

SYMBOL	PARAMETER	MIN	MAX	CONDITIONS
V_{IL}	INPUT LOGIC LEVELS Low-level Input Voltage	$V_{SS}-1.5V$	0.8V	$V_{SS} = 4.75V$ (NOTE 1)
V_{IH}	High-level Input Voltage			
V_{OL}	OUTPUT LOGIC LEVELS Low-level Output Voltage	$V_{SS}-1.0V$	0.4V	$V_{SS} = 5.25V$ (NOTE 2) $I_{OL} = -1.6mA$
V_{OH}	High-level Output Voltage			
I_{IL}	INPUT CURRENT Low-level Input Current (each pin)		-1.6mA	$V_{SS} = 5.25V$ $V_{IN} = 0.4V$
I_{SS}	SUBSTRATE SUPPLY CURRENT		65 mA	$V_{SS} = 5.25V$ $V_{GG} = -12.6V$
I_{GG}	GATE SUPPLY CURRENT		-30mA	$V_{IN} = 0.4V$

NOTE 1: All inputs have pull-up resistors. This allows unloaded TTL outputs of 2.0V to be connected and operate properly. When connected, this voltage (2.0V) will become $V_{SS} - 1.5V$.

NOTE 2: V_{OL} and V_{OH} when $OE = V_{IH}$ (low impedance output). High impedance ($OE = V_{IL}$) ≈ 10 Mohm.

SWITCHING CHARACTERISTICS — See “Switching Waveforms”

($V_{SS} = +5V$, $V_{DD} = 0V$, $V_{GG} = -12V$, $T_A = 0^\circ C$ to $+70^\circ C$, $C_{LOAD} = 10$ pf)

SYMBOL	PARAMETER	MIN	MAX	CONDITIONS
T_{IES}	Input Enable Setup Time	0 ns		
T_{IEH}	Input Enable Hold Time	0 ns		
T_{DIS}	Data Input Setup Time	0 ns		
T_{DIH}	Data Input Hold Time	250 ns		
T_{IRL}	Input Register Load Time		250 ns	
T_{IRE}	Input Register Empty Time		800 ns	
T_{ISL}	Input Strobe Low Time	450 ns		
T_{ISH}	Input Strobe High Time	150 ns		
T_{OES}	Output Enable Setup Time	50 ns		
T_{OEH}	Output Enable Hold Time	50 ns		
T_{OSL}	Output Strobe Low Time	150 ns		(NOTE 1)
T_{ODR}	Output Data Ready Time		200 ns	
T_{DR}	Data Reset Time		600 ns	
T_{PD}	Output Propagation Delay Time		250 ns	
T_{ODRL}	Output Data Ready Low		600 ns	
T_{OSH}	Output Strobe High Time	500 ns		
T_{ODV}	Output Data Valid Time		200 ns	
T_R	Maximum Ripple Time		10 μs	
T_B	Maximum Bubble Time		25 μs	
T_{MR}	Master Reset Pulse Time	500 ns		
f_D	Maximum Data Rate	250 kHz	1 MHz	(NOTE 4)

NOTE 1: $T_{rise} = T_{fall} = 10nS$.

NOTE 2: Ripple Time—time required for a single data character to propagate from the input to the output of an empty FIFO (IS strobing edge to ODR rising edge).

NOTE 3: Bubble Time—time required for a “hole” to propagate from the output to the input of a full FIFO (falling edge of OS to rising edge of IRE).

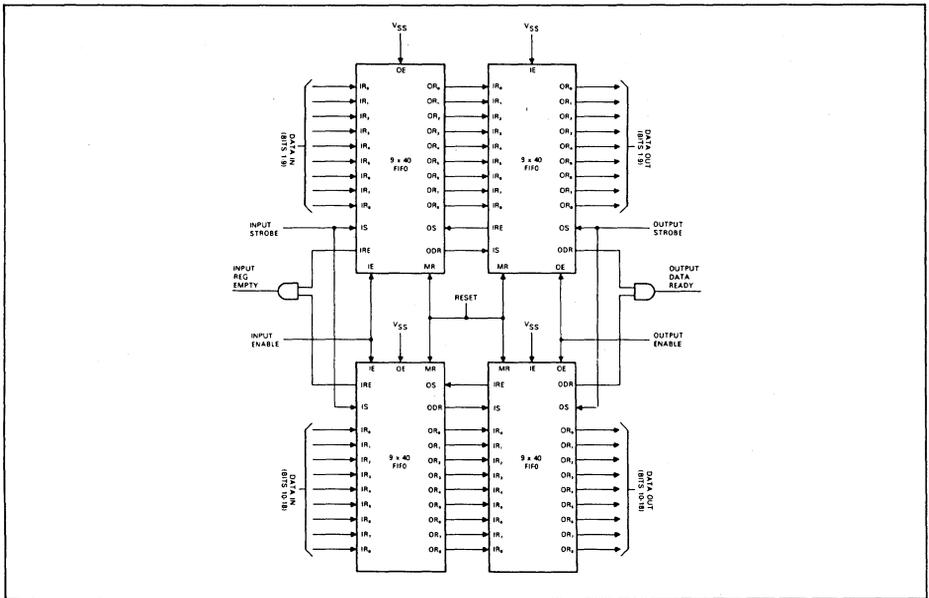
NOTE 4: The maximum data rates for a “single” FIFO (not cascaded) and for FIFO’s cascaded together are the same.

GENERAL NOTE: All A.C. test points are at 0.8V or 2.0V.

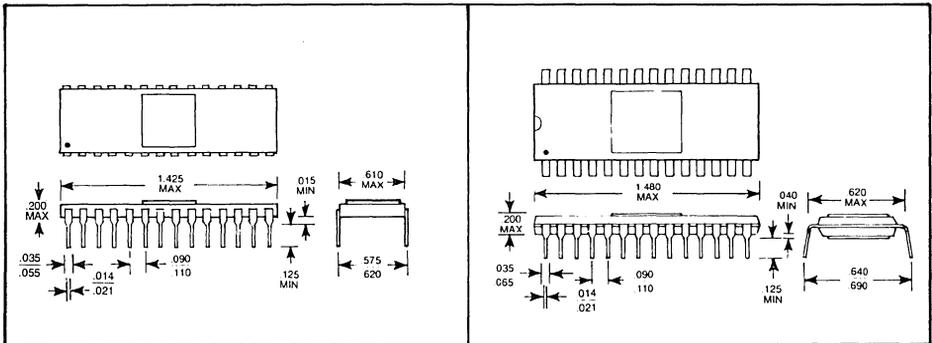
ORDERING INFORMATION

T_A = 0°C to +70°C

PART NO.	PACKAGE TYPE	CASCADABLE	INPUT STROBE EDGE	MAX. DATA RATE
FR1502E-00	CERAMIC	NO	FALLING	1.0 MHz
F-00	PLASTIC	NO	FALLING	1.0 MHz
E-01	CERAMIC	NO	FALLING	500 kHz
F-01	PLASTIC	NO	FALLING	500 kHz
E-02	CERAMIC	NO	FALLING	250 kHz
F-02	PLASTIC	NO	FALLING	250 kHz
E-10	CERAMIC	YES	RISING	1.0 MHz
F-10	PLASTIC	YES	RISING	1.0 MHz
E-11	CERAMIC	YES	RISING	500 kHz
F-11	PLASTIC	YES	RISING	500 kHz
E-12	CERAMIC	YES	RISING	250 kHz
F-12	PLASTIC	YES	RISING	250 kHz



EXPANSION EXAMPLE



FR1502E CERAMIC PACKAGE

FR1502F PLASTIC PACKAGE

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WD5869 Dynamic Shift Register

MARCH, 1981

FEATURES

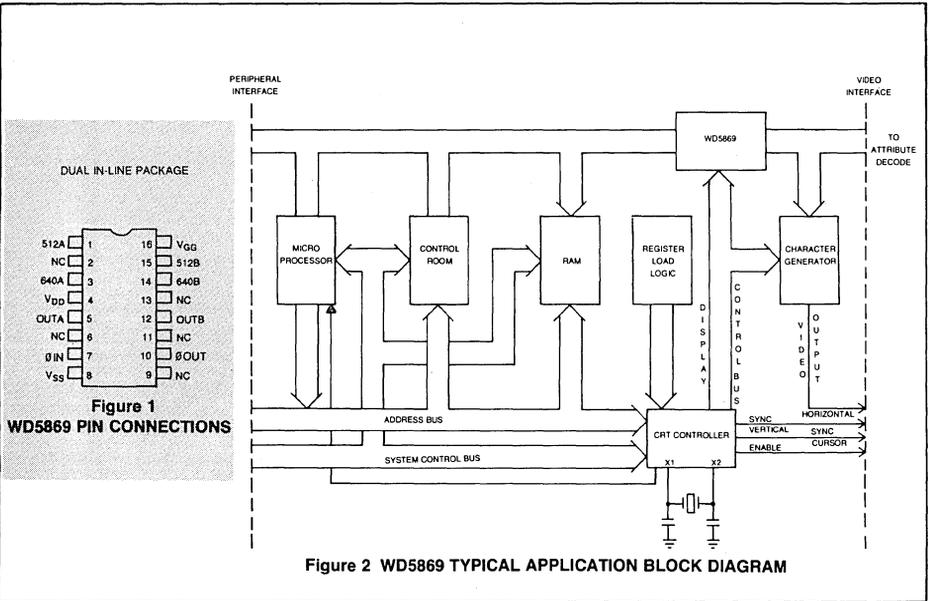
- DUAL 640 BIT
- ADDITIONAL TAPS AT 512 ON EACH REGISTER
- INTERNAL CLOCKING
- HIGH SPEED
- 3 STATE OUTPUT BUFFER

GENERAL DESCRIPTION

The WD5869 Dual 640 Bit Dynamic Shift Register is a monolithic MOS integrated circuit designed for use in computer display peripherals. The clocks and recirculate logic are internal to reduce system component count, and 3 state output buffers provide bus interface. The WD5869 is available in a 16 pin molded plastic package, or a 16 pin ceramic package.

APPLICATIONS

- CRT DISPLAYS
- COMPUTER PERIPHERALS
- CRYPTOGRAPHY



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Data and Clock Input Voltage and Supply Voltages with respect to VSS

+0.3V to -20V

Power Dissipation

800mW at TA = 25°C

Storage Temperature

-55°C to +125°C (Plastic Package)
-65°C to +150°C (Ceramic Package)

ELECTRICAL CHARACTERISTICS (DC)

TA = 0°C to + 50°C, VSS = +5V ± 5%, VDD = -5V + 5%, VGG = -12V ± 5%

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
I _{DD}	POWER SUPPLY CURRENT		-50	mA	
	DATA INPUT LEVELS				
V _{IL}	Logical Low Level	V _{SS} -17.9	V _{SS} -4.2	V	
V _{IH}	Logical High Level	V _{SS} -1.7	V _{SS} +0.3	V	
I _{IL}	DATA INPUT LEAKAGE		10	μA	V _{IN} = -5V; All other Pins GND
C _{di}	DATA INPUT CAPACITANCE		10	pf	V _{IN} = 0V; f = 1MHZ, All other Pins GND
	CLOCK INPUT LEVELS				
V _{OH}	Logical High Level	V _{SS} -1.0	V _{SS} +0.3	V	
V _{OL}	Logical Low Level	V _{SS} -17.9	V _{SS} -14.5	V	
I _{CL}	CLOCK INPUT LEAKAGE		10	μA	V _O = -17.9V; All other Pins GND
C _{ci}	CLOCK INPUT CAPACITANCE		200	pf	V _O = 0V; f = 1MHZ, All other Pins GND
	DATA OUTPUT LEVELS				
V _{OH}	Logical High Level	2.4		V	I Source = -50mA
V _{OL}	Logical Low Level		V _{SS} -0.4	V	I Sink = 1.6 mA

TABLE 1 D.C. PARAMETERS

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
	CLOCK FREQUENCY	10	2000	KHz	$\theta_{tr} = \theta_{tf} = 20 \text{ ns}$
$\theta_{pw \text{ in}}$	CLOCK PULSE WIDTH, In	0.15	1.0	μs	$\theta_{tf} + \theta_{pw} + \theta_{tr} \leq 3.0 \mu\text{s}$
$\theta_{pw \text{ out}}$	CLOCK PULSE WIDTH, Out	1	1	$\theta_{pw \text{ in}}$	
$\theta_{d \text{ rising}}$	CLOCK PHASE DELAY TIME, from rising edge	10		ns	
$\theta_{d \text{ falling}}$	CLOCK PHASE DELAY TIME, from falling edge	10		ns	
θ_{tr}	CLOCK TRANSITION TIME, rising edge		1.0	μs	$\theta_{tf} + \theta_{pw} + \theta_{tr} \leq 3.0 \mu\text{s}$
θ_{tf}	CLOCK TRANSITION TIME, falling edge		1.0	μs	
θ_{ds}	DATA INPUT SET-UP TIME	80		ns	
θ_{dh}	DATA INPUT HOLD TIME	40		ns	
θ_{pdL}	DATA OUTPUT PROPAGATION DELAY, to low level		200	ns	
θ_{pdH}	DATA OUTPUT PROPAGATION DELAY, to high level		200	ns	

TABLE 2 A.C. PARAMETERS

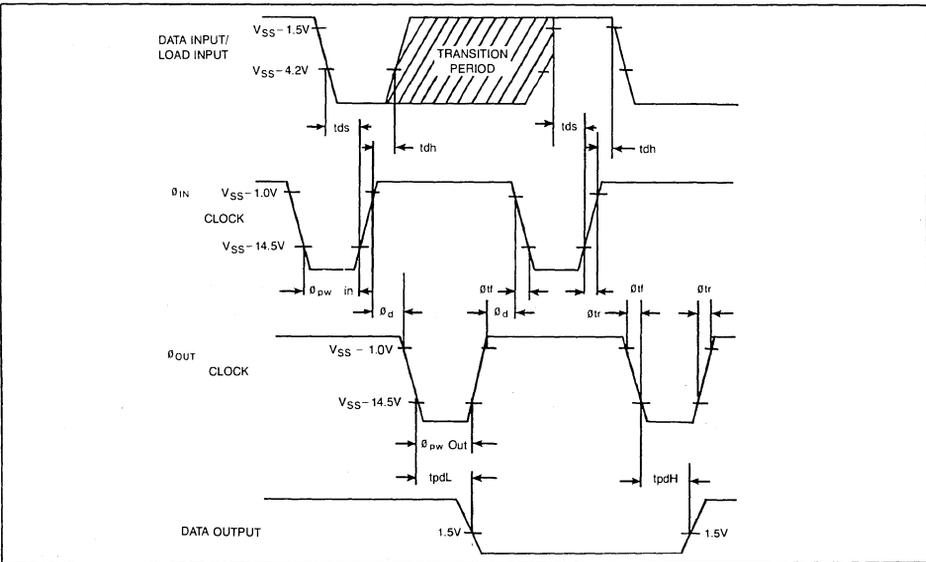
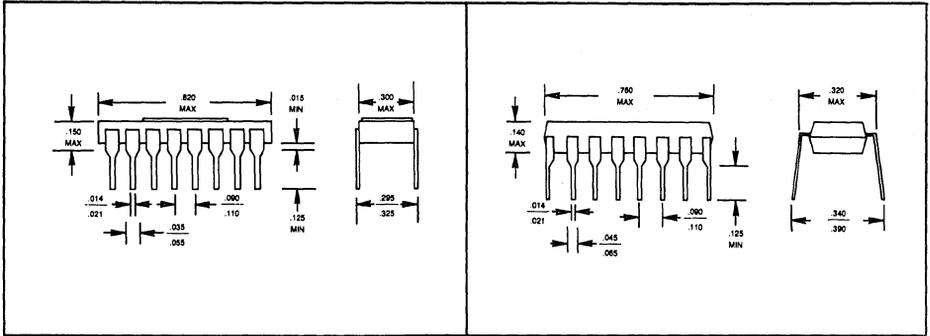


Figure 3 WD5869 TIMING DIAGRAM



WD5869J CERAMIC PACKAGE

WD5869K PLASTIC PACKAGE

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PIN OUTS

The device is packaged in a 40-pin plastic or ceramic cavity package. The interface signals are defined below with all input/output signals complemented to facilitate bussing and interfacing with TTL. The

Data Set controls and Status signals are also complemented to allow for an inversion when converting to EIA RS232C levels. The names and symbols assigned to the Data Set interface signals follows EIA standard nomenclature.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	POWER SUPPLIES	V _{BB}	- 5V
21		V _{CC}	+ 5V
40		V _{DD}	+ 12V
20		V _{SS}	Ground
23	MASTER RESET	MR	The Control and Status Registers and other controls are cleared when this input is low.
8-15	DATA ACCESS LINES	DAL0-DAL7	Eight-bit bi-directional bus used for transfer of data, control, status, and address information.
17,22,24,25,26	SELECT CODE	ID7-ID3	Five input pins which when hard-wired assign the device a unique identification code used to select the device when addressing and used as an identification when responding to interrupts.
3	CHIP SELECT	CS	The low logic transition of CS identifies a valid address on the DAL bus during Read and Write operations.
39	READ ENABLE	RE	This signal, when low, gates the contents of an addressed register from a selected ASTRO onto the DAL.
4	WRITE ENABLE	WE	This signal, when low, gates the contents of the DAL bus into the addressed register of a selected ASTRO.
7	INTERRUPT	INTR	This open drain output is made low when one of the communication interrupt conditions occur.
2	INTERRUPT ACKNOWLEDGE IN	IACKI	This input becomes low when polling takes place on the bus by the Controller to determine the interrupting source. When this signal is received, the ASTRO places its ID code on the DAL if it is requesting interrupt, otherwise it makes IACKO a low.
5	INTERRUPT ACKNOWLEDGE OUT	IACKO	This output is made a logic low in response to a low IACKI if the ASTRO receiving an IACKI input is not the interrupting device.
6	REPLY	RPLY	This open drain output is made low when the ASTRO is responding to being selected by an address on the DAL during read or write operations or in affirming that it is the interrupting source during interrupt polling.
30-33	CLOCK RATES	R1-R4	These four inputs accept four different local 32X data rate Transmit and Receive clocks. The input on R4 may be divided down into a 32X clock from a 32X, 64X, 128X, or 256X clock input. The clock used in the ASTRO is selected by the Control Register.
37	TRANSMITTED DATA	TDATA (BA)	This output is the transmitted serial data from the ASTRO. This output is held in a Marking condition when the transmitter section is not enabled.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
27	RECEIVED DATA	RDATA (BB)	This input receives serial data into the ASTRO.
38	REQUEST TO SEND	RTS (CA)	This output is enabled by the Control Register and remains in a low state during transmitted data from the ASTRO.
36	CLEAR TO SEND	CTS (CB)	This input, when low, enables the transmitter section of the ASTRO.
28	DATA SET READY	DSR (CC)	This input generates an interrupt when going On or Off while the Data Terminal Ready signal is On. It appears as a bit in the Status Register.
16	DATA TERMINAL READY	DTR (CD)	This output is generated by a bit in the Control Register and indicates Controller readiness.
18	RING INDICATOR	RING (CE)	This input from the Data Set generates an interrupt when made low with Data Terminal Ready in the "Off" condition.
29	CARRIER DETECTOR	CARR (CF)	This input from the Data Set generates an interrupt when going On or Off if Data Terminal Ready is On. It appears as a bit in the Status Register.
35	TRANSMITTER TIMING	IXTC (DB)	This input is the Transmitter 1X Data Rate Clock. Its use is selected by the Control Register. The transmitted data changes on the negative transition of this signal.
34	RECEIVER TIMING	IXRC (DD)	This input is the Receiver 1X Data Rate Clock. Its use is selected by the Control Register. The Received Data is sampled by the ASTRO on the positive transition of this signal.
19	MISCELLANEOUS	MISC	This output is controlled by a bit in the Control Register and is used as an extra programmable signal.

RECEIVER REGISTER — This 8-bit shift register inputs the received data at a clock rate determined by the Control Register. The incoming data is assembled to the selected character length and then transferred to the Receiver Holding Register with logic zeroes filling out any unused high-order bit positions.

RECEIVER HOLDING REGISTER — This 8-bit parallel buffer register presents assembled receiver characters to the DAL bus lines when requested through a Read operation.

COMPARATOR — The 8-bit comparator is used in the Synchronous mode to compare the assembled contents of the Receiver Register and the SYN register or DLE register. A match between the registers sets up stripping of the received character, when programmed, by preventing the data from being loaded into the Receiver Holding Register. A bit in the Status Register is set when stripping is performed. The comparator output also enables character synchronization of the Receiver on two successive matches with the SYN register.

SYN REGISTER — This 8-bit register is loaded from the DAL lines by a Write operation and holds the synchronization code used to establish receiver character synchronization. It serves as a fill character when no new data is available in the Transmitter Holding Register during transmission. This register cannot be read onto the DAL lines. It must be loaded with logic zeroes in all unused high-order bits.

DLE REGISTER — This 8-bit register is loaded from the DAL lines by a Write operation and holds the "DLE" character used in the Transparent mode of operation in which an idle transmit period is filled with the combination DLE-SYN pair of characters rather than a single SYN character. In addition the ASTRO may be programmed to force a single DLE character prior to any data character transmission while in the transmitter transparent mode.

TRANSMITTER HOLDING REGISTER — This 8-bit parallel buffer register holds parallel transmitted data transferred from the DAL lines by a Write operation. This data is transferred to the Transmitter Register when the transmitter section is enabled and the Transmitter Register is ready to send new data.

TRANSMITTER REGISTER — This 8-bit shift register is loaded from the Transmitter Holding Register, SYN register, or DLE register. The purpose of this register is to serialize data and present it to the transmitted Data output.

CONTROL REGISTERS — There are two 8-bit Control Registers which hold device programming signals such as mode selection, clock selection, interface signal control, and data format. Each of the Control Registers can be loaded from the DAL lines by a Write operation or read onto the DAL lines by a Read operation. The registers are cleared by a Master Reset.

STATUS REGISTER — This 8-bit register holds information on communication errors, interface data register status, match character conditions, and communication equipment status. This register may be read onto the DAL lines by a Read operation.

DATA ACCESS LINES — The DAL is an 8-bit bi-directional bus port over which all address, data, control, and status transfers occur. In addition to transferring data and control words the DAL lines also transfer information related to addressing of the device, reading and writing requests, and interrupting information.

ASTRO OPERATION

ASYNCHRONOUS MODE

Framing of asynchronous characters is provided by a Start bit (logic low) at the beginning of a character and a Stop bit (logic high) at the end of a character. Reception of a character is initiated on recognition of the first Start bit by a positive transition of the receiver clock, after a preceding Stop bit. The Start and Stop bits are stripped off while assembling the serial input into a parallel character.

The character assembly is completed by the reception of the Stop bit after reception of the last character bit. If this bit is a logic high, the character is determined to have correct framing and the ASTRO is prepared to receive the next character. If the Stop bit is a logic low the Framing Error Status flag is set and the Receiver assumes this bit to be the Start bit of the next character. Character assembly continues from this point if the input is still a logic low when sampled at the theoretical center of the assumed Start bit. As long as the Receive input is spacing, all zero characters are assembled and error flags and data received interrupts are generated so that line breaks can be determined. After a character of all zeroes is assembled along with a zero in the Stop bit location, the first received logic high is determined as a Stop bit and this resets the Receiver circuit to a Ready state for assembly of the next character.

In the Asynchronous mode the character transmission occurs when information contained in the Transmitter Holding Register is transferred to the Transmitter Register. Transmission is initiated by the insertion of a Start bit, followed by the serial output of the character least significant bit first with parity, if enabled, following the most significant bit; then the insertion of a 1-, 1.5-, or 2-bit length Stop condition. If the Transmitter Holding Register is full, the next character transmission starts after the transmission of the Stop bit of the present character in the Transmitter Register. Otherwise, the Mark (logic high) condition is continually transmitted until the Transmitter Holding Register is loaded.

In order to allow re-transmission of data received at a slightly faster character rate, means are provided for shortening the Stop bit length to allow transmission of characters to occur at the same rate as the reception of characters. The Stop bit is shortened by 1/16 of a bit period for 1-Stop bit selection and 3/16 of a bit period for 1.5-, or 2-Stop bit selection, if the next character is ready in the Transmitter Holding Register.

SYNCHRONOUS MODE

Framing of characters is carried out by a special Synchronization Character Code (SYN) transmitted at the beginning of a block of characters. The Receiver, when enabled, searches for two continuous characters matching the bit pattern contained in the SYN register. During the time the Receiver is searching, data is not transferred to the Receiver Holding Register, status bits are not updated, and the Receiver interrupt is not activated. After the detection of the first SYN character, the Receiver assembles subsequent bits into characters whose length is determined by contents of the Control Register. If, after the first SYN character detection, a second SYN character is present, the Receiver enters the Synchronization mode until the Receiver Enable Bit is turned off. If a second successive SYN character is not found, the Receiver reverts back to the Search mode.

In the Synchronous mode a continuous stream of characters are transmitted once the Transmitter is enabled. If the Transmitter Holding Register is not loaded at the time the Transmitter Register has completed transmission of a character, this idle time will be filled by a transmission of the character contained in the SYN register in the Non-transparent mode, or the characters contained in the DLE and SYN registers respectively while in the Transparent mode of operation.

DETAILED OPERATION

Receiver — The Receiver Data input is clocked into the Receiver Register by a 1X Receiver Clock

from a modem Data Set, or by a local 32X bit rate clock selected from one of four externally supplied clock inputs. When using the 1X clock, the Receiver Data is sampled on the positive transition of the clock in both the Asynchronous and Synchronous modes. When using a 32X clock in the Asynchronous mode, the Receive Sampling Clock is phased to the Mark-To-Space transition of the Received Data Start bit and defines, through clock counts, the center of each received Data bit within + 0%, - 3% at the positive transition 16 clock periods later.

In the Synchronous mode the Sampling Clock is phased to all Mark-To-Space transitions of the Received Data inputs when using a 32X clock. Each transition of the data causes an incremental correction of the Sampling Clock by 1/32nd of a bit period. The Sampling Clock can be immediately phased to every Mark-To-Space Data transition by setting Bit 4 of Control Register 1 to a logic high, while the Receiver is disabled.

When the complete character has been shifted into the Receiver Register it is then transferred to the Receiver Holding Register; the unused, higher number bits are filled with zeroes. At this time the Receiver Status bits (Framing Error/Sync Detect, Parity Error/DLE Detect, Overrun Error, and Data Received) are updated in the Status Register and the Data Received interrupt is activated. Parity Error is set, if encountered while the Receiver parity check is enabled in the Control Register. Overrun Error is set if the Data Received status bit is not cleared through a Read operation by an external device when a new character is ready to be transferred to the Receiver Holding Register. This error flag indicates that a character has been lost, as new data is lost and the old data and its status flags are saved.

The characters assembled in the Receiver Register that match the contents of the SYN or DLE register are not loaded into the Receiver Holding Register, and the DR interrupt is not generated, if Bit 3 of Control Register 2 (CR23 = SYN Strip) or Bit 4 of Control Register 1 (CR14 = DLE Strip) are set respectively, the SYN-DET and DLE-DET status bits are set with the next non SYN or DLE character. When both CR23 and CR14 are set (Transparent mode), the DLE-SYN combination is stripped. The SYN comparison occurs only with the character received after the DLE character. If two successive DLE characters are received only the first DLE character is stripped. No parity check is made while in this mode.

Transmitter — Information is transferred to the Transmitter Holding Register by a Write operation. Information can be loaded into this register at any time, even when the Transmitter is not enabled. Transmission of data is initiated only when the Request To Send bit is set to a logic one in the Control Register and the Clear To Send

input is a logic low. Information is normally transferred from the Transmitter Holding Register to the Transmitter Register when the latter has completed transmission of a character. However, information in the DLE register may be transferred prior to the information contained in the Transmitter Holding Register if the Force DLE signal condition is enabled (Bits 5 = Force DLE and 6 = TX Transparent of Control Register 1 set to a logic one). The control bit CR15 must be set prior to loading of a new character in the transmitter holding register to insure forcing the DLE character prior to transmission of the data character. The Transmitter Register output passes through a flip-flop which delays the output by one clock period. When using the 1X clock generated by the Modem Data Set, the output data changes state on the negative clock transition and the delay is one bit period. When using a local 32X clock the transmitter section selects one of the four selected rate inputs and divides the clock down to the baud rate. This clock is phased to the Transmitter Holding Register empty flag such that transmission of characters occurs within two clock times of the loading of the Transmitter Holding Register when the Transmitter Register is empty.

When the Transmitter is enabled, a Transmitter interrupt is generated each time the Transmitter Holding Register is empty. If the Transmitter Holding Register is empty when the Transmitter Register is ready for a new character the Transmitter enters an idle state. During this idle time a logic high will be presented to the Transmitted Data output in the Asynchronous mode or the contents of the SYN register will be presented in the Synchronous Non-transparent mode (CR16 = 0). In the Synchronous Transmit Transparent mode (enabled by Bit 6 of Control Register 1 = Logic 1), the idle state will be filled by a DLE-SYN character transmission in that order. When entering the Transparent mode the DLE-SYN fill will not occur until the first forced DLE.

If the Transmitter section is disabled by a reset of the Request to Send, any partially transmitted character is completed before the transmitter section of the ASTRO is disabled. As soon as the CTS goes high the transmitted data output will go high.

When the Transmit parity is enabled, the selected Odd or Even parity bit is inserted into the last bit of the character in place of the last bit of the Transmitted Register. This limits transfer of character information to a maximum of seven bits plus parity or eight bits without parity. Parity cannot be enabled in the Synchronous Transparency mode.

DEVICE PROGRAMMING

The two 8-bit Control Registers of the ASTRO determine the operative conditions of the ASTRO chip. Control Register 1 is shown in the following table.

BIT 7 7	6	5	4	3	2	1	0
SYNC/ASYNC 0—LOOP MODE 1—NORMAL MODE	ASYNC 0—NON BREAK MODE 1—BREAK MODE SYNC 0—NON TRANSMITTER TRANSPARENT MODE 1—TRANSMIT TRANSPARENT MODE	ASYNC (TRANS. ENABLED) 0—1 1/2 or 2 STOP BIT SELECTION 1—SINGLE STOP BIT ASYNC (TRANS. DISABLED) 0—MISC OUT = 1 1—MISC OUT = 0 SYNC (CR18 = 0) 0—NO PARITY GENERATED 1—TRANSMIT PARITY ENABLED SYNC (CR18 = 1) 0—NO FORCE DLE 1—FORCE DLE	ASYNC 0—NON ECHO MODE 1—AUTO ECHO MODE SYNC (CR12 = 1) 0—DLE STRIPPING NOT ENABLED 1—DLE STRIPPING ENABLED SYNC (CR12 = 0) 0—MISC OUT = 1 1—MISC OUT = 0	ASYNC 0—NO PARITY ENABLED 1—PARITY CHECK ENABLED ON RECEIVER PARITY GENERATION ENABLED ON TRANSMITTER SYNC 0—RECEIVER PARITY CHECK IS DISABLED 1—RECEIVER PARITY CHECK IS ENABLED	SYNC/ASYNC 0—RECEIVER DISABLED 1—RECEIVER ENABLED	SYNC/ASYNC 0—SETS RTS OUT = 1 1—SETS RTS OUT = 0	SYNC/ASYNC 0—SET DTR OUT = 1 1—SETS DTR OUT = 0

CONTROL REGISTER 1

Control Register 1

Bit 7 — A logic 0 configures the ASTRO into an Internal Data and Control Loop mode and disables the Ring interrupt. In this diagnostic mode the following loops are connected internally:

- The Transmit Data is connected to the Receive Data with the TD pin held in a Mark condition and the input to the RD pin disregarded.
- With a 1X clock selected, the Transmitter Clock also becomes the Receive Clock.
- The Data Terminal Ready (DTR) Control bit is connected to the Data Set Ready (DSR) input, with the DTR output in held in an Off condition (logic high), and the DSR input pin is disregarded.
- The Request to Send Control bit is connected to the Clear To Send (CTS) and Carrier Detector inputs, with the RTS output pin held in an Off condition (logic high), and the CTS and Carrier Detector input pins are disregarded.
- The Miscellaneous pin is held in an Off (logic high) condition.

A logic 1 on Bit 7 enables the Ring interrupt and returns the ASTRO to the normal full duplex configuration.

Bit 6 — In the *Asynchronous* mode a logic 1 holds the Transmitted Data output in a Spacing (Logic 0) condition, starting at the end of any current transmitted character, when the Transmitter is enabled. Normal Transmitter timing continues so that this Break condition can be timed out after the loading of new characters into the Transmitter Holding Register.

In the *Synchronous* mode a logic 1 sets the Transmitter in a transparent transmission which implies that idle transmitter time will be filled by DLE-SYN character transmission and a DLE can be forced ahead of any character in the Transmitter Holding

Register when CR15 is a logic one in the sync mode.

Bit 5 — In the *Asynchronous* mode a logic 1, with the Transmitter enabled, causes a single Stop bit to be transmitted. A logic 0 causes 2-Stop bit transmission for character lengths of 6, 7, or 8 bits and one-and-a-half Stop bits for a character length of 5 bits.

With the Transmitter disabled this bit controls the Miscellaneous output on Pin 19, which may be used for Make Busy on 103 Data Sets, Secondary Transmit on 202 Data Sets, or dialing on CBS Data Couplers.

In the *Synchronous* mode a logic 1 combined with a logic 0 on Bit 6 of Control Register 1 enables Transmit parity; if CR15=0 or CR15=1 no parity is generated. When set to a logic 1 with Bit 6 also a logic 1, the contents of the DLE register are transmitted prior to the next character loaded in the Transmitter Holding Register as part of the Transmit Transparent mode.

Bit 4 — In the *Asynchronous* mode a logic 1 enables the Automatic Echo mode when the receiver section is enabled. In this mode the clocked regenerated data is presented to the Transmit Data output in place of normal transmission through the Transmitter Register. This serial method of echoing does not present any abnormal restrictions on the transmit speed of the terminal. Only the first character of a Break condition of all zeroes (null character) is echoed when a Line Break condition is detected. For all subsequent null characters, with logic zero Stop bits, a steady Marking condition is transmitted until normal character reception resumes. Echoing does not start until a character has been received and the Transmitter is idle. The Transmitter does not have to be enabled during the Echo mode.

In the *Synchronous* mode a logic 1, with the Receiver enabled, does not allow assembled

Receiver data matching the DLE register contents to be transferred to the Receiver Holding Register; also, parity checking is disabled.

When the Receiver is not enabled this bit controls the Miscellaneous output on Pin 19, which may be used for New Sync on a 201 Data Set. When operating with a 32X clock and a disabled Receiver a logic 1 on this bit also causes the Receiver timing to synchronize on Mark-To-Space transitions.

Bit 3 — In the *Asynchronous* mode a logic 1 enables check of parity on received characters and generation of parity for transmitted characters.

In the *Synchronous* mode a logic 1 bit enables check of parity on received characters only. **Note:** Transmitter parity enable is controlled by CR15.

Bit 2 — A logic 1 enables the ASTRO to receive data into the Receiver Holding Register, update Receiver Status Bits 1, 2, 3, and 4, and to generate Data Received interrupts. A logic 0 disables the Receiver and clears the Receiver Status bits.

Bit 1 — Controls the Request To Send output on Pin 38 to control the CA circuit of the Data Set. The RTS output is inverted from the state of CR11. A logic 1 combined with a low logic Clear To Send input enables the Transmitter and allows THREE interrupts to be generated. A logic 0 disables the Transmitter and turns off the external Request To Send signal. Any character in the Transmitter Register will be completely transmitted before the Transmitter is turned off. The Request To Send output may be used for other functions such as "Make Busy" on 103 Data Sets.

Bit 0 — Controls the Data Terminal Ready output on Pin 16 to control the CD circuit of the Data Set. A logic 1 enables the Carrier and Data Set Ready interrupts. A logic 0 enables only the telephone line Ring interrupt. The DTR output is inverted from the state of CR10.

Control Register 2

Control Register 2, unlike Control Register 1, cannot be changed at any time. This register should be changed only while both the receiver and transmitter sections of the ASTRO are in the idle state.

Bits 7-6— These bits select the character length as follows:

Bits 7-6	Character Length
00	8 bits
01	7 bits
10	6 bits
11	5 bits

When parity is enabled it must be considered as a bit when making character length selection, i.e. 5 character bits plus parity = 6 bits.

Bit 5 — A logic 1 selects the Synchronous Character mode. A logic 0 selects the Asynchronous Character mode.

Bit 4 — A logic 1 selects odd parity and a logic 0 selects even parity, when parity is enabled by CR13 and/or CR15.

Bit 3 — In the *Asynchronous* mode a logic 0 selects the rate 1-32X clock input (pin 30) as the Receiver Clock rate and a logic 1 selects the same clock rate for the Receiver as selected by Bits 2-0 for the Transmitter. This bit must be a logic 1 for the 1X clock selection by Bits 2-0.

In the *Synchronous* mode a logic 1 causes all DLE-SYN combination characters in the Transparent mode when DLE strip CR14 is a logic 1, or all SYN characters in the Non-transparent mode to be stripped and no Data Received interrupt to be generated. The SYN Detect status bit is set with reception of the next assembled character as it is transferred to the Receiver Holding Register.

Bits 2-0 — These bits select the Transmit and Receive clocks. The Input Clock to the Rate 4 pin may be divided down to form the 32X clock from a multiple clock as shown:

Bits 2-0	Clock
000	1X clock for Transmit and Receive (Pins 35 and 34 respectively)
001	32X clock — Rate 1 input (Pin 30)
010	32X clock — Rate 2 input (Pin 31)
011	32X clock — Rate 3 input (Pin 32)
100	32X clock — Rate 4 input + 1 (Pin 33)
101	32X clock — Rate 4 input + 2 (Pin 33)
110	32X clock — Rate 4 input + 4 (Pin 33)
111	32X clock — Rate 4 input + 8 (Pin 33)

BIT 7 6	5	4	3	2 1 0
SYNC/ASYNC CHARACTER LENGTH SELECT 00 = 8 BITS 01 = 7 BITS 10 = 6 BITS 11 = 5 BITS	MODE SELECT 0—ASYNCHRONOUS MODE 1—SYNCHRONOUS MODE	SYNC/ASYNC 1—ODD PARITY SELECT 0—EVEN PARITY SELECT	ASYNC 1—RECEIVER CLOCK DETERMINED BY BITS 2-0 0—RECEIVER CLK = RATE 1 SYNC (CR14 = 0) 0—NO SYN STRIP 1—SYN STRIP SYNC (CR14 = 1) 0—NO DLE SYN STRIP 1—DLE SYN STRIP	SYNC/ASYNC CLOCK SELECT 000 1X CLOCK 001 RATE 1 CLOCK 010 RATE 2 CLOCK 011 RATE 3 CLOCK 100 RATE 4 CLOCK 101 RATE 4 CLOCK + 2 110 RATE 4 CLOCK + 4 111 RATE 4 CLOCK + 8

CONTROL REGISTER 2

Status Register

The data contained in the Status Register define Receiver and Transmitter data conditions and status of the Data Set. The Status word is shown and defined below.

Bit 7 — This bit is set to a logic 1 whenever there is a change in state of the Data Set Ready or Carrier Detector inputs while Data Terminal Ready (Bit 0 of Control Register 1) is a logic 1 or the Ring Indicator is turned on, with DTR a logic 0. This bit is cleared when the Status Register is read onto the Data Access Lines.

Bit 6 — This bit is the logic complement of the Data Set Ready input on Pin 28. With 202-type Data Sets it can be used for Secondary Receive.

Bit 5 — This bit is the logic complement of the Carrier Detector input on Pin 29.

Bit 4 — In the *Asynchronous* mode a logic 1 indicates that received data contained a log 0 bit after the last data bit of the character in the stop bit slot, while the Receiver was enabled. This indicates a Framing error. This bit is set to a logic 0 if the proper logic 1 condition for the Stop bit was detected.

In the *Synchronous* mode a logic 1 indicates that the contents of the Receiver Register matched the contents of the SYN Register. The condition of this bit remains for a full character assembly time. If SYN strip (CR23) is enabled this status bit is updated with the character received after the SYN character. In both modes the bit is cleared when the Receiver is disabled.

Bit 3 — When the DLE Strip is enabled (Bit 4 of Control Register 1) the Receiver parity check is disabled and this bit is set to a logic 1 if the *previous character* to the presently assembled character matched the contents of the DLE register; otherwise it is cleared. The DLE DET remains for one character time and is rest on the next character transfer or on a Status Register Read. If DLE Strip is not enabled this bit is set to a logic 1 when the Receiver is enabled, Receiver parity (Bit 3 of Control Register 1) is also enabled, and the last received character has a Parity error. A logic 0 on this bit indicates correct parity. This bit is cleared in either of the above modes when the Receiver is disabled.

Bit 2 — A logic 1 indicates an Overrun error which occurs if the previous character in the Receiver Holding Register has not been read and Data

Received is not reset, at the time a new character is to be transferred to the Receiver Holding Register. This bit is cleared when no Overrun condition is detected, i.e., the next character transfer time or when the Receiver is disabled.

Bit 1 — A logic 1 indicates that the Receiver Holding Register is loaded from the Receiver Register, if the Receiver is enabled. It is cleared to a logic 0 when the Receiver Holding Register is read onto the Data Access Lines, or the Receiver is disabled.

Bit 0 — A logic 1 indicates that the Transmitter Holding Register does not contain a character while the Transmitter is enabled. It is set to a logic 1 when the contents of the Transmitter Holding Register is transferred to the Transmitter Register. It is cleared to a 0 bit when the Transmitter Holding Register is loaded from the DAL, or when the Transmitter is disabled.

INPUT/OUTPUT OPERATIONS

All Data, Control, and Status words are transferred over the Data Access Lines (DAL 0-7). Additional input lines provide controls for addressing a particular unit, and regulating all input and output operations. Other lines provide interrupt capability to indicate to a Controller that an input operation is requested by the ASTRO. All input/output terminology below is referenced to the Controller so that a Read or Input takes data from the ASTRO and places it on the DAL lines, while a Write or Output places data from the DAL lines into the ASTRO.

Read

A Read Operation is initiated by the placement of an *eight-bit address* on the DAL by the Controller. When the Chip Select signal goes to a logic low state, the ASTRO compares Bits 7-3 of the DAL with its hard-wired ID code (Pins 17, 22, 24, 25, and 26) and becomes selected on a Match condition. The ASTRO then sets its REPLY line low to acknowledge its readiness to transfer data. Bits 2-0 of the address are used to select ASTRO registers to read from as follows:

Bits 2-0	Selected Register
000	Control Register 1
010	Control Register 2
100	Status Register
110	Receiver Holding Register

When the Read Enable (\overline{RE}) line is set to a logic low condition by the Controller the ASTRO gates

BIT 7	6	5	4	3	2	1	0
• DATA SET CHANGE	• DATA SET READY	• CARRIER DETECTOR	• FRAMING ERROR • SYN DETECT	• DLE DETECT • PARITY ERROR	• OVERRUN ERROR	• DATA RECEIVED	• TRANSMITTER HOLDING REGISTER EMPTY

STATUS REGISTER

the contents of the addressed register onto the DAL. The Read operation terminates, and the device becomes unselected, when both the Chip Select and Read Enable return to a logic high condition. Reading of the Receiver Holding Register clears the DR Status bit. Bit 0 must be a logic low in read or write operations.

Write

A Write operation is initiated by the placement of an eight-bit address or the DAL by the Controller. The ASTRO compares Bits 7-3 of the DAL with its ID code when the Chip Select input goes to a logic low state. If a Match condition exists, the device is selected and makes its RPLY line low to acknowledge its readiness to transfer data. Bits 2-0 of the address are used to select ASTRO registers to be written into as follows:

Bits 2-0	Selected Register
000	Control Register 1
010	Control Register 2
100	SYN and DLE Register
110	Transmitter Holding Register

When the Write Enable (WE) line is set to a logic low condition by the Controller the ASTRO gates the data from the DAL into the addressed register. If data is written into the Transmitter Holding Register, the THRE Status bit is cleared to a logic zero.

The 100 address loads both the SYN and DLE registers. After writing into the SYN register the device is conditioned to write into the DLE if followed by another Write pulse with the 100 address. Any intervening Read or Write operation with other addresses resets this condition such that the next 100 will address the SYN register.

Interrupts

The following conditions generate interrupts:

- 1. Data Received (DR)** — Indicates transfer of a new character to the Receiver Holding Register while the Receiver is enabled.
- 2. Transmitter Holding Register Empty (THRE)** — Indicates that the THR register is empty while the Transmitter is enabled. The first interrupt occurs when the Transmitter becomes enabled if there is an empty THR, or after the character is transferred to the Transmitter Register making the THR empty.
- 3. Carrier On** — Indicates Carrier Detector input goes low when DTR is on.

- 4. Carrier Off** — Indicates Carrier Detector input goes high when DTR is on.
- 5. DSR On** — Indicates the Data Set Ready input goes low when DTR is on.
- 6. DSR Off** — Indicates the Data Set Ready input goes high when DTR is on.
- 7. Ring On** — Indicates the Ring Indicator input goes low when DTR is off.

Each time an Interrupt condition exists the INTR output from the ASTRO is made a logic low. The following interrupt procedure is then carried out even if the interrupt condition is removed.

The Controller acknowledges the Interrupt request by setting the Chip Select (CS) and the Interrupt Acknowledge Input (IACKI) to the ASTRO to a Low state. On this transition all non-interrupting devices receiving the IACKI set their Interrupt Acknowledge Output (IACKO) low, enabling lower priority daisy-chained devices to respond to the Interrupt request. The highest priority device that is interrupting will then set its RPLY low. This device places its ID code on Bit Positions 7-3 of the DAL when a low RE signal is received. In addition Bit 2 is set to a logic one if any of the interrupt numbers 1 and 3-7 above occurred, and remains a logic low if the THRE has caused the interrupt (see note).

To reset the Interrupt condition (INTR) Chip Select (CS) and IACKI must be received by the ASTRO. A setup time must exist between CS and the RE or WE signals to allow chip selection prior to read/write operations and deselection control through the latter signals. The data is removed from the DAL when the RE signal returns to the logic high state.

MAXIMUM RATINGS

V _{DD} With Respect to V _{BB} (Ground)	+ 20 to - 0.3V
Max Voltage To Any Input With Respect to V _{BB}	+ 20 to - 0.3V
Operating Temperature	0°C to 70°C
Storage Temperature	Plastic -55°C to +125°C Ceramic -65°C to +150°C
Power Dissipation	1000 mW

NOTE:
The UC1671-1 places Data Received on DAL1 and THRE on DAL0 during interrupt servicing. The UC1671-0 places the DAL1 and DAL0 into a Three State Mode during interrupt.

OPERATING CHARACTERISTICS

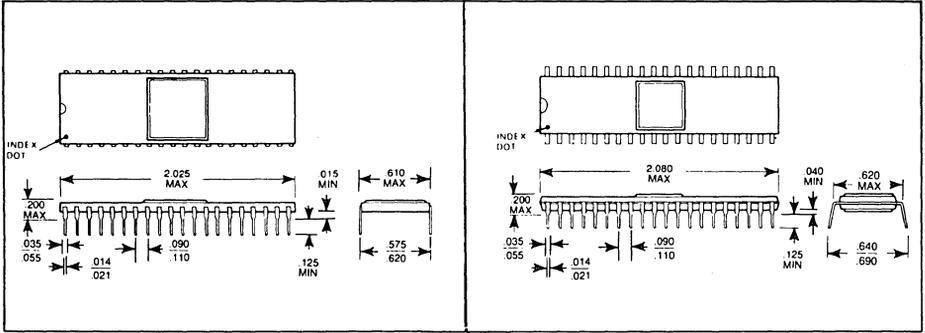
$T_A = 0^\circ\text{C to } 70^\circ\text{C}$, $V_{DD} = +12.0\text{V} \pm .6\text{V}$, $V_{BB} = -5.0 \pm .25\text{V}$, $V_{SS} = 0\text{V}$, $V_{CC} = +5\text{V} \pm .25\text{V}$

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
I _{LI}	Input Leakage			10	μA	V _{IN} = V _{DD}
I _{LO}	Output Leakage			10	μA	V _{OUT} = V _{DD}
I _{BB}	V _{BB} Supply Current			1	mA	V _{BB} = -5V
I _{CCAVE}	V _{CC} Supply Current			80	mA	
I _{DDAVE}	V _{DD} Supply Current			10	mA	
V _{IH}	Input High Voltage	2.4			V	
V _{IL}	Input Low Voltage (All Inputs)			.8	V	
V _{OH}	Output High Voltage	2.8			V	I _O = -100 μA
V _{OL}	Output Low Voltage			.4	V	I _O = 1.6 mA

AC CHARACTERISTICS

$T_A = 0^\circ\text{C to } 70^\circ\text{C}$, $V_{DD} = +12.0\text{V} \pm 0.6\text{V}$, $V_{BB} = -5.0\text{V} \pm 0.25\text{V}$, $V_{CC} = +5.0 \pm .25\text{V}$, $V_{SS} = 0\text{V}$
 $CL_{MAX} = 20\text{ pf}$

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
T _{AS}	Address Set-Up Time	0			ns	
t _{ah}	Address Hold Time	150			ns	
T _{ARL}	Address to R _{PLY} Delay			400	ns	
T _{CS}	$\overline{\text{CS}}$ Width	250			ns	
T _{CSRLF}	$\overline{\text{CS}}$ to Reply OFF Delay	0		250	ns	R _L = 2.7 KΩ
READ						
T _{ARE}	Address and $\overline{\text{RE}}$ Spacing	250			ns	
T _{RECSH}	$\overline{\text{RE}}$ and $\overline{\text{CS}}$ Overlap	20			ns	
T _{RECS}	$\overline{\text{RE}}$ to $\overline{\text{CS}}$ Spacing	250			ns	
T _{RED}	$\overline{\text{RE}}$ to Data Out Delay			180	ns	C _L = 20 pf
T _{RE}	$\overline{\text{RE}}$ Width	200		1000	ns	
WRITE						
T _{AWE}	Address to $\overline{\text{WE}}$ Spacing	250			ns	
T _{WECSH}	$\overline{\text{WE}}$ and $\overline{\text{CS}}$ Overlap	20			ns	
T _{WE}	$\overline{\text{WE}}$ Width	200		1000	ns	
T _{DS}	Data Set-Up Time	150			ns	
T _{DH}	Data Hold Time	100			ns	
T _{WECS}	$\overline{\text{WE}}$ to $\overline{\text{CS}}$ Spacing	250			ns	



UC1671A CERAMIC PACKAGE

UC1671B PLASTIC PACKAGE

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WD1931 Asynchronous/Synchronous Receiver/Transmitter

FEATURES

SYNCHRONOUS AND ASYNCHRONOUS

- Full Duplex Operations

SYNCHRONOUS MODE

- Selectable 5- to 8-Bit Characters
- Two Successive SYN Characters Sets Synchronization
- Programmable SYN and DLE Character Detection and Stripping
- Programmable SYN and DLE-SYN Fill
- Transparent BI-SYNC Operation

ASYNCHRONOUS MODE

- Selectable 5- to 8-Bit Characters
- Line Break Detection and Generation
- 1-, 1½-, or 2-Stop Bit Selection
- False Start Bit Detection
- Automatic Serial Echo Mode
- Overrun and Framing Error Detection

SYSTEM COMPATIBILITY

- Double Buffering of Data
- 8-Bit Bi-Directional Bus for Data, Status, and Control Words
- All Inputs and Outputs TTL Compatible
- Chip Select, RE, WE, A0, A1 Interface to CPU
- On-Line Diagnostic Capability
- Data Set, Carrier Detect, and Ring Interrupts

BAUD RATE — DC TO 1M BAUD/SEC

8 SELECTABLE CLOCK RATES

- Accepts 1X Clock and Up to Four Different 32X Baud Rate Clock Inputs
- Up to 47% Distortion Allowance with 32X Clock

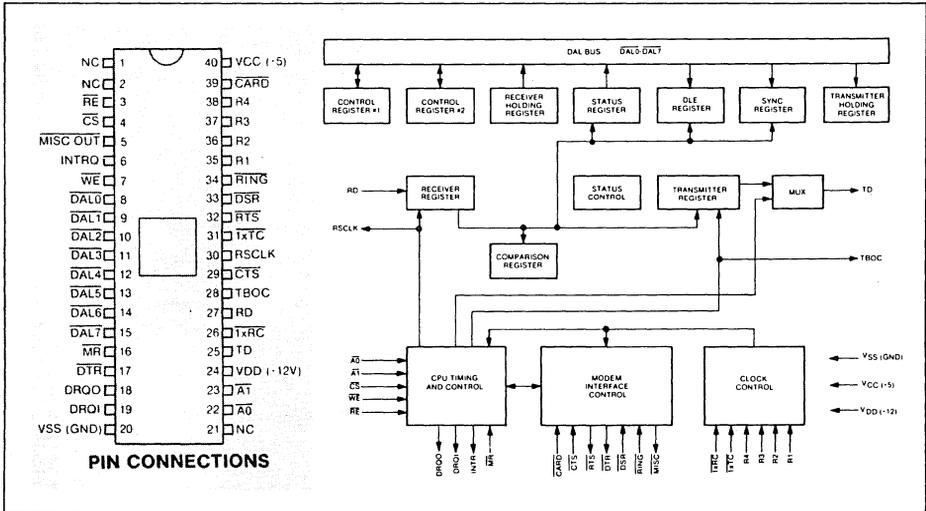
PINOUT COMPATIBLE TO SD1933 FOR MULTIPROTOCOL BOARD APPLICATIONS

APPLICATIONS

- ASYNCHRONOUS COMMUNICATIONS
- ASYNCHRONOUS COMMUNICATIONS
- SERIAL/PARALLEL COMMUNICATIONS

GENERAL DESCRIPTIONS

The WD1931 is a MOS/LSI device which performs the functions of interfacing a serial data communications channel to a parallel digital system. This device is capable of full duplex communications with asynchronous and/or synchronous systems. Western Digital has made device pin assignments for the WD1931 to make it compatible with the WD1933 (Synchronous Data Link Controller). This pin out allows the user to implement a one-board multiprotocol design. For character-oriented asynchronous and/or synchronous (bi-sync) protocols, the WD1931 is used, and for bit-oriented SDLC, HDLC and ADCCP protocols the WD1933 is used (see WD1933 data sheet).



WD1931 BLOCK DIAGRAM

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	—	NC	No connection; see Note 4.
2	—	NC	No internal connection.
3	$\overline{\text{READ ENABLE}}$	$\overline{\text{RE}}$	When this line is low the device, if selected, gates the contents of the addressed register on the DAL.
4	$\overline{\text{CHIP SELECT}}$	$\overline{\text{CS}}$	The chip is selected when this signal is low.
5	$\overline{\text{MISCELLANEOUS OUT}}$	$\overline{\text{MISC OUT}}$	This output is controlled by Bit 5 of Control Register 1 when in the Asynchronous mode and by Bit 4 when in the Synchronous mode. (See Note 1.)
6	INTERRUPT	INTRQ*	This output is made high when one of the interrupt conditions occurs. Reading the Status Register resets this signal.
7	$\overline{\text{WRITE ENABLE}}$	$\overline{\text{WE}}$	When this line is low the device, if selected, accepts the data on the DAL and gates it into the addressed register.
8-15	$\overline{\text{DATA ADDRESS LINES}}$	$\overline{\text{DAL0-DAL7}}$	Eight-bit Bi-directional bus for transfer of data, control and status information. Active low.
16	$\overline{\text{MASTER RESET}}$	$\overline{\text{MR}}$	The Control and Status Registers and other controls are cleared when this input is low.
17	$\overline{\text{DATA TERMINAL READY}}$	$\overline{\text{DTR}}$	This output is controlled by Bit 0 of Control Register 1 and is intended to control Circuit CD of the data set.
18	DATA REQUEST OUT	DRQO*	This output is made high when the THR is empty while the transmitter is enabled. Loading the THR resets this signal.
19	DATA REQUEST IN	DRQI*	This output is made high when the RHR is full while the receiver is enabled. Reading the RHR resets this signal.
20	POWER SUPPLY	V _{SS}	Ground
21	—	NC	No internal connection.
22	$\overline{\text{ADDRESS 0}}$	$\overline{\text{A0}}$	This input is the low-order address bit for register selection.
23	$\overline{\text{ADDRESS 1}}$	$\overline{\text{A1}}$	This input is the high-order address bit for register selection.
24	POWER SUPPLY	V _{DD}	+12V
25	TRANSMITTED DATA	TD	This output is the transmit serial data. This output is held in a MARKING condition when the transmitter is not enabled. It is intended to control Circuit BA of the data set.
26	$\overline{\text{RECEIVER TIMING}}$	$\overline{\text{1XRC}}$	This input is the receiver 1X clock, when used. It is intended to be derived from Circuit DC of the data set. The Received Data is sampled on the positive transition of this signal.
27	RECEIVED DATA	RD	This input is the receive serial data and is intended to be derived from Circuit BB of the data set.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
28	TRANSMITTER BYTE OUTPUT COMPLETE	TBOC	This output goes high after the last bit of a byte is transmitted including parity if enabled, and is valid for one bit period. See Note 2.
29	<u>CLEAR TO SEND</u>	<u>CTS</u>	This input enables the transmitter when low and is intended to be derived from Circuit CB of the data set.
30	RECEIVER CLOCK	RSCLK	This output goes high when the receiver data is sampled, and is valid for one clock period. See Note 2.
31	<u>TRANSMITTER TIMING</u>	<u>TXTC</u>	This input is the transmitter 1X clock when used. It is intended to be derived from Circuit DB of the data set. The Transmitter changes on the negative transition of this signal.
32	<u>REQUEST TO SEND</u>	<u>RTS</u>	This output is controlled by Bit 1 of Control Register 1 and is intended to control Circuit CA of the data set. If Bit 1 of Control Register 1 is reset during a transmission then RTS will go high on the falling edge of the transmitter clock that follows the last bit of the current transmission character.
33	<u>DATA SET READY</u>	<u>DSR</u>	This input appears as Status Bit 6 and generates interrupts when going on or off if DTR is on. It is intended to be derived from Circuit CC of the data set.
34	<u>RING INDICATOR</u>	<u>RING</u>	This input generates an interrupt when made low with DTR off. It is intended to be derived from Circuit CE of the data set.
35-38	RATES	R1-R4	These four rate inputs are used for 32X-256X Local Transmit and Receive clocks. The rate is selected by the Control Register. (See Note 3.)
39	<u>CARRIER DETECTOR</u>	<u>CARD</u>	This input appears as Status Bit 5 and generates interrupts when going on or off if DTR is on. It is intended to be derived from Circuit CF of the data set.
40	POWER SUPPLY	V _{CC}	+5V

* THE WD1931 OUTPUTS, INTRQ, DRQI, and DRQO ARE TRUE HIGH (TRUE = V_{OH}) OUTPUTS. ON THE UC1671, THESE OUTPUTS ARE TRUE LOW (TRUE = V_{OL}) AND OPEN DRAIN.

- NOTE 1:** If the system design does not make use of MISC IN on the WD1933, the user may tie this to +12V without harm or degradation to the WD1933. This has the same effect as a logic high input. If the system design does make use of MISC IN, then provisions must be made to select +12V when the WD1931 is in the socket or MISC IN when the WD1933 is in the socket. This may be accomplished by a small switch or by jumpers.
- NOTE 2:** The outputs TBOC and RSCLK on the WD1931 may be tied to ground or to +5 volts through a 10K pull-up without harm or degradation to the WD1931.
- NOTE 3:** If R1-R4 are not selected by the command word in the WD1931, then anything may be on these inputs. If RI and CD are tied high on the WD1933, then the inputs (pins 35-38) may have anything on them. When both the rate fields in the WD1931 and RI and CD on the WD1933 are used, the system designer must make provisions by an external switch or jumpers.
- NOTE 4:** Pin 1 of the device must **not** be connected in any way to any signal, power or ground line. This pin is the output of an internal Back Bias Generator, and is used for testing only.

ORGANIZATION

The WD1931 block diagram is illustrated on page 1. The primary sections include the control, buffer, status, receiver, transmitter, comparison and sync registers.

Control Registers.

There are two 8-bit Control Registers which hold device programming signals such as mode selection, clock selection, interface signal control, and data format. Each of the Control Registers can be loaded from the \overline{DAL} lines by a Write operation or read onto the DAL lines by a Read operation. The registers are cleared by a Master Reset.

Receiver Holding Register.

This 8-bit parallel buffer register presents assembled receiver characters to the \overline{DAL} bus lines when requested through a Read operation.

Status Register.

This 8-bit register holds information on communication errors, interface data register status, match character conditions, and communication equipment status. This register may be read onto the \overline{DAL} lines by a Read operation.

DLE Register.

This 8-bit register is loaded from the \overline{DAL} lines by a Write operation and holds the DLE character used in the Transparent mode of operation in which an idle transmit period is filled with the combination DLE-SYN pair of characters rather than a single SYN character. In addition the WD1931 may be programmed to force a single DLE character prior to any data character transmission while in the transmitter transparent mode. This register cannot be read onto the \overline{DAL} lines. It must be loaded with logic zeroes in all unused high-order bits.

SYN Register.

This 8-bit register is loaded from the \overline{DAL} lines by a Write operation and holds the synchronization code used to establish receiver character synchronization. It serves as a fill character when no new data is available in the Transmitter Holding register during transmission. This register cannot be read onto the \overline{DAL} lines. It must be loaded with logic zeroes in all unused high-order bits.

Transmitter Holding Register.

This 8-bit parallel buffer register holds parallel transmitted data transferred from the \overline{DAL} lines by a Write operation. This data is transferred to the Transmitter Register when the transmitter section is enabled and the Transmitter Register is ready to send new data.

Receiver Register.

This 8-bit shift register inputs the received data at a clock rate determined by the Control Register. This incoming data is assembled to the selected character length and then transferred to the Receiver Holding Register with logic zeroes filling out any unused high-order bit positions.

Transmitter Register.

This 8-bit shift register is loaded from the Transmitter Holding Register, SYN register, or DLE register. The purpose of this register is to serialize data and present it to the transmitted Data output.

Comparator.

The 8-bit comparator is used in the Synchronous mode to compare the assembled contents of the Receiver Register and the SYN register or DLE register. A match between the registers sets up stripping of the received character, when programmed, by preventing the data from being loaded into the Receiver Holding Register. A bit in the Status Register is set when stripping is performed. The comparator output also enables character synchronization of the Receiver on two successive matches with the SYN register.

Data Access Lines.

The \overline{DAL} is an 8-bit bi-directional bus port over which all data, control, and status transfers occur.

WD1931 OPERATION

Asynchronous Mode

Framing of asynchronous characters is provided by a Start bit (logic zero) at the beginning of a character and a Stop bit (logic one) at the end of a character. Reception of a character is initiated on recognition of the first Start bit after a preceding Stop bit. The Start and Stop bits are stripped off while assembling the serial input into a parallel character. If enabled, the parity bit is checked and then stripped off.

The character assembly is completed by the reception of the Stop bit after reception of the last character bit. If this bit is a logic one the character is determined to have correct framing and the WD1931 is prepared to receive the next character. If the Stop bit is a logic zero the Framing Error Status flag is set and the Receiver assumes this bit to be the Start bit of the next character. Character assembly continues from this point if the input is still a logic zero when sampled at the theoretical center of the assumed Start bit. As long as the Receive input is spacing, all zero characters are assembled and error flags and data received interrupts are generated so that line breaks can be determined. After a character of all zeroes is assembled along with a zero in the Stop bit location, the first received logic one is determined as

a Stop bit and this resets the Receiver circuit to a Ready state for assembly of the next character.

In the Asynchronous mode the character transmission occurs when information contained in the Transmitter Holding Register is transferred to the Transmitter Register. Transmission is initiated by the insertion of a Start bit, followed by the serial output of the character (least significant bit first) with parity, if enabled, following the most significant bit; then the insertion of a 1-, 1.5-, or 2-bit length Stop condition. If the Transmitter Holding Register is full the next character transmission starts after the transmission of the Stop bit(s) of the present character in the Transmitter Register. Otherwise, the Mark (logic one) condition is continually transmitted until the Transmitter Holding Register is loaded.

In order to allow re-transmission of data received at a slightly faster character rate, means are provided for shortening the Stop bit length to allow transmission of characters to occur at the same rate as the reception of characters. The Stop bit may be shortened a maximum of 1/16 of a bit period for 1-Stop bit selection and 3/16 of a bit period for 1.5-, or 2-Stop bit selection. To shorten the Stop bit the user must load the Transmitter Holding Register exactly $(X+2)$ 16ths of a bit period before the end of a stop bit transmission, where X = the number of 16ths the user wishes to strip. If $X+2$ exceeds the maximum then no shortening occurs. This feature does not work in 1X clocking mode.

***NOTE:** As a special case, the 1.5 stop bit mode can be shortened from 1/24 to 11/24 of the whole period if the Transmitter Holding Register is loaded $(X + 2)$ 24ths (of the whole period) before the end of the stop bit transmission.

Synchronous Mode

Framing of characters is carried out by a special Synchronization Character Code (SYN) transmitted at the beginning of a block of characters. The Receiver, when enabled, searches for two continuous characters matching the bit pattern contained in the SYN register. During the time the Receiver is searching, data is not transferred to the Receiver Holding Register, status bits are not updated, and the Receiver interrupt is not activated. After the detection of the first SYN character, the Receiver assembles subsequent bits into characters whose length is determined by contents of the Control Register. If, after the first SYN character detection, a second SYN character is present, the Receiver

enters the Synchronization mode until the Receiver Enable Bit is turned off. If a second successive SYN character is not found, the Receiver reverts back to the Search mode.

In the Synchronous mode a continuous stream of characters are transmitted once the Transmitter is enabled. If the Transmitter Holding Register is not loaded at the time the Transmitter Register has completed transmission of a character, this idle time will be filled by a transmission of the character contained in the SYN register in the Non-transparent mode, or the characters contained in the DLE and SYN registers respectively while in the Transparent mode of operation.

DETAILED OPERATION

Receiver

The Receiver Data input is clocked into the Receiver Register by a 1X Receiver Clock from a modem Data Set, or by a local 32X bit rate clock selected from one of four externally supplied clock inputs. When using the 1X clock, the Receiver Data is sampled on the positive transition of the clock in both the Asynchronous and Synchronous modes. When using a 32X clock in the Asynchronous mode, the Receive Sampling Clock is phased to the Mark-To-Space transition of the Received Data Start bit and defines, through clock counts, the center of each received Data bit within +0%, -3% at the positive transition 16 clock periods later.

In the Synchronous mode the Sampling Clock is phased to all Mark-To-Space transitions of the Received Data inputs when using a 32X clock. Each transition of the data causes an incremental correction of the Sampling Clock by 1/32nd of a bit period. The Sampling Clock can be immediately phased to every Mark-To-Space Data transition by setting Bit 4 of Control Register 1 to a logic one while the Receiver is disabled.

When the complete character has been shifted into the Receiver Register it is then transferred to the Receiver Holding register. The unused higher number bits are filled with zeroes. At this time the Receiver Status bits (Framing Error/Sync Detect, Parity Error/DLE Detect, Overrun Error, and Data Received) are updated in the Status Register and the Data Received interrupt is activated. Parity Error is set, if encountered, if the Receiver parity check is enabled in the Control Register. Overrun Error is set if the Data Received status bit is not cleared through a Read operation by an external device when a new character is ready to be transferred to the Receiver Holding Register. This error flag indicates that a character has been lost. New data is lost and the old data and its status flags are saved.

The characters assembled in the Receiver Register that match the contents of the SYN or DLE registers are not loaded into the Receiver Holding Register and the DR interrupt is not generated if Bit 3 of Control Register 2 (CR23= SYN Strip) or Bit 4 of Control Register 1 (CR14=DLE Strip) are set respectively. The SYN-DET and DLE-DET status bits are set with the next non-SYN or DLE character. When both CR23 and CR14 are set (Transparent mode), the DLE-SYN combination is stripped. The SYN comparison occurs only with the character received after the DLE character. If two successive DLE characters are received only the first DLE character is stripped. No parity check is made while in this mode.

Transmitter

Information is transferred to the Transmitter Holding Register by a Write operation. Information can be loaded into this register at any time, even when the Transmitter is not enabled. Transmission of data is initiated only when the Request To Send bit is set to a logic one in the Control Register and the Clear To Send input is a logic zero. Information is normally transferred from the Transmitter Holding Register to the Transmitter Register when the latter has completed transmission of a character. However, information in the DLE register may be transferred prior to the information contained in the Transmitter Holding Register if the Force DLE signal condition is enabled (Bits 5=Force DLE and 6=TX Transparent of Control Register 1 set to a logic one). The control bit CR15 must be set prior to loading of a new character in the transmitter holding register to ensure forcing the DLE character prior to transmission of the data character. The Transmitter Register output passes through a flip-flop which delays the output by one clock period. When using the 1X clock generated by the Modem Data Set the output data changes state on the negative clock transition and the delay is one bit period. When using a local 32X clock the transmitter section selects one of the four selected rate inputs and divides the clock down to the baud rate. This clock is phased to the Transmitter Holding Register empty flag such that transmission of characters occurs within two clock times of the loading of the Transmitter Holding Register when the Transmitter Register is empty.

When the Transmitter is enabled, a Transmitter interrupt is generated each time the Transmitter Holding Register is empty. If the Transmitter Holding Register is empty when the Transmitter Register is ready for a new character the Transmitter enters an idle state. During this idle time a logic one will be presented to the Transmitted Data output in the Asynchronous mode or the contents of the SYN reg-

ister will be presented in the Synchronous Non-transparent mode (CR16=0). In the Synchronous Transmit Transparent mode (enabled by Bit 6 of Control Register 1=Logic 1), the idle state will be filled by a DLE-SYN character transmission in that order. When entering the Transparent mode the DLE-SYN fill will not occur until the first forced DLE.

If the Transmitter section is disabled by a reset of the Request to Send, any partially transmitted character is completed before the transmitter section of the WD1931 is disabled. As soon as the CTS goes high the transmitted data output will go high.

When the Transmit parity is enabled, the selected Odd or Even parity bit is inserted into the last bit of the character in place of the last bit of the Transmitter Register. This limits transfer of character information to a maximum of seven bits plus parity or eight bits without parity. Parity cannot be enabled in the Synchronous Transparency mode.

CLOCKING

Two clocking schemes are used. In one case a 1X Receiver Timing and Transmitter Timing are input from a Data Set and are used to clock their respective data. In the second case a local 32X clock is phased to the data and used to clock the data. The device is capable of selecting from four externally supplied rates.

The use of the 1X clock is the same for the receiver and the transmitter in both the Synchronous and Asynchronous Character modes.

The use of the 32X clock in the receiver differs depending on mode. In the Asynchronous Character mode the receive sampling clock is phased to the mark-space transition of Received Data input at the beginning of the Start bit, causing the Sampling clock to be approximately in the middle of the bit. The accuracy of sampling is +0%, -3%. In the Synchronous Character mode the Receive Sampling clock is phased to all the mark-space transitions on the Received Data input. Each such transition of the data causes an incremental correction of the Sampling clock of 1/32 of the bit period. The Sampling clock can be immediately phased with the data transitions by setting Bit 4 of Control Register 1 to a 1 bit with the receiver disabled. As long as this bit is a one the Sampling clock is locked to every mark-space data transition.

The transmitter divides the selected rate input down to the baud rate. This clock is phased to the THRE flag so that character transmission starts within two clocks of the THR loading when the transmitter is idling.

AUTO ECHO FEATURE

The device is capable of serially echoing the received data with a one bit delay when in the Asynchronous mode and the Receiver on. This causes the clocked regenerated received data to be presented to the Transmit Data output rather than the output of the Transmitter Register or a steady marking. This serial method of echoing does not present any abnormal restrictions on the transmit speed of the terminal. Breaks are not echoed back. When the device detects a Zero Stop bit and a character of all zeroes, the echoing stops and a steady marking is transmitted until such time as normal character reception resumes. Because echoing is taking place during determination of a break condition, a single character of all zeroes (Null character) is echoed when a break is initiated at the terminal. The Echoing is enabled by setting Bit 4 of Control Register 1 to a 1 bit. Echoing does not start until the start of a receive character at a time when the transmitter is idle and \overline{CTS} is zero. If the Transmitter is forced out of the idle mode while a character is being echoed transmission of that character is halted. The Transmitter is idle when CR11 is a zero or the Transmitter is waiting for the THR to be loaded in the Asynchronous mode.

LOOP FEATURE

The device has on-line diagnostic capability. When the Loop Control bit is a zero the data and data set controls are appropriately looped as follows:

- Transmit Data is connected to Receive Data, with the TD output pin held in a MARK condition and the RD input pin disregarded.
- When a 1X clock is selected the TD clock becomes the Receive clock.
- The Data Terminal Ready Control bit is connected to the Data Set Ready input with the \overline{DTR} output pin held in an OFF condition and the \overline{DSR} input pin disregarded.
- The Request To Send Control bit is connected to the Clear To Send and Carrier inputs, with the \overline{CTS} output pin held in an OFF condition and the \overline{CTS} and \overline{CARD} input pins disregarded.
- MISCELLANEOUS Pin is held in an OFF condition.

INPUT/OUTPUT OPERATIONS

All data, control, and status information is transferred to DAL pins. Control and address lines provide for controlling the addressing, input and output operations. In addition other lines provide interrupt capability for alerting a controller that input/output is required. Input/output terminology is referenced to the controller; therefore, a Read or Input takes

data from the device and places it on the DAL, while a Write or Output places data from the DAL into the device.

READ

A read operation is initiated when \overline{CS} and \overline{RE} go low. When the Read Enable (\overline{RE}) line goes low, the device gates the contents of the addressed register onto the DAL. The device becomes unselected when the \overline{CS} and \overline{RE} are both high. When the Receiver Holding Register is read, the DR Status bit is cleared to zero.

WRITE

A Write operation is initiated when \overline{CS} and \overline{WE} go low. When the Write Enable (\overline{WE}) line goes low, the device gates the data from the DAL into the addressed register. When the \overline{CS} and \overline{WE} go high the device becomes unselected. If the Transmitter Holding Register is written into, the THRE Status bit is cleared to zero.

The 10 address is used to load both the SYN and DLE Registers. After writing into SYN the device is conditioned to write into DLE if followed by another Write to that address. Any intervening Read or Write to other addresses reset this condition so that SYN will be addressed with 10.

$\overline{A0}$ and $\overline{A1}$ address device registers for Read/Write operations are shown:

REGISTER ADDRESS FOR READ/WRITE OPERATIONS

A1	A0	Read	Write
F	F	Control Register 1	Control Register 1
F	T	Control Register 2	Control Register 2
T	F	Status Register	SYN & DLE Register
T	T	Receiver Holding Register	Transmitter Holding Register

T = V_{IL} at pin

F = V_{IH} at pin

DEVICE PROGRAMMING

Programming of the WD1931 is done via two Control Registers, one Status Register, a SYN/DLE Register, and the Transmitter and Receive Holding Registers. The two Control Registers are referred to as CR1 and CR2. The bits within CR1 are referred to as CR10 through CR17, and the bits within CR2 are referred to as CR20 through CR27. For any register bit 0 is the LSB.

Two general modes of operation exist for the WD1931, Asynchronous and Synchronous. Both modes of operation are discussed separately. BI-SYNC is a special case of Synchronous mode and is not treated separately.

Figures 4 through 6 show CR1, CR2, and the Status Register bit definitions. The meaning of each bit in each register is described twice: once for Asynchronous mode and again for Synchronous mode. The figures combine and summarize both modes.

ASYNCHRONOUS MODE

Control Register 1

Bit	Name	Function
0	DATA TERMINAL READY	Controls <u>DATA TERMINAL READY</u> output on Pin 17 for control of data set circuit CD. When set to a 1 bit, it enables Carrier and Data Set Ready interrupts. When set to a 0 bit, only the Ring interrupt is enabled.
1	REQUEST TO SEND	Controls <u>REQUEST TO SEND</u> output on Pin 32 for control of data set circuit CA. This bit must be a 1 bit, and the <u>CLEAR TO SEND</u> input must be low for the transmitter to be enabled and for <u>THRE</u> interrupts to be generated. When this bit is set to a 0 bit the Transmitter is disabled and the <u>RTS</u> output turned off, but not till the end of any current character being transmitted. The <u>RTS</u> output may be used for other functions such as "Make Busy" on 103 data sets.
2	RECEIVER ENABLE	When set to a 1 bit, it enables the receiver allowing received characters to be placed in the Receiver Holding Register, Status Bits 1, 2, 3 and 4 to be updated, and Data Received interrupt to be generated. When set to a 0 bit, the above status bits are cleared. After this bit is set, character reception starts with the first bit after a valid start bit.
3	PARITY ENABLE	When set to a 1 bit, it enables check of parity on received characters and generation of parity for transmitted characters.
4	ECHO MODE	When set to a 1 bit and the <u>RECEIVER</u> is enabled, the clocked regenerated data is presented to the Transmitted Data output. The transmitter does not have to be enabled.
5	STOP BIT SELECTION/MISCELLANEOUS	When set to a 1 bit with the transmitter enabled it causes a single stop bit to be transmitted. When set to a 0 bit, it causes two stop bits to be transmitted for character lengths of 6, 7, or 8 bits and 1.5 stop bits for a character length of 5 bits. When the transmitter is not enabled this bit controls the <u>MISCELLANEOUS</u> output on Pin 5 to be used for Make Busy on 103 Data Sets, Secondary Transmit on 202 Data Sets, or dialing on CBS Data Couplers.
6	BREAK	When set to a 1 bit and the transmitter is enabled the Transmitted Data is held in a spacing condition starting with the end of any current character. Normal transmitter timing continues so that the break can be timed out by loading characters into the <u>THR</u> , i.e., interrupts are generated and the transmitter operates normally except for the output which remains low while this bit is a one.
7	LOOP/NORMAL	When this bit is set to a 0 bit, the device is configured to provide an internal data and control loop and the Ring interrupt is disabled. When this bit is set to a 1 bit the device is in normal full duplex configuration and the Ring interrupt is enabled.

Control Register 2

Bit	Name	Function
2-0	CLOCK SELECT	Selects Transmit and Receive clock as follows: 0 — Transmit and Receive clock input (1X) 1 — Rate 1 (32X) 2 — Rate 2 (32X) 3 — Rate 3 (32X) 4 — Rate 4 (32X) 5 — Rate 4 ÷ 2 (32X) (64X) 6 — Rate 4 ÷ 4 (32X) (128X) 7 — Rate 4 ÷ 8 (32X) (256X)
3	ALTERNATE RX CLOCK	A 0 bit selects Rate 1 as the Receiver clock rate and a 1 bit provides the same rate as Transmit. This bit must be a 1 bit if 1X clocking is selected in bits 2-0.
4	PARITY ODD/EVEN	A 1 bit selects Odd Parity and a 0 bit selects Even Parity, when Parity is enabled.
5	CHARACTER MODE	A 0 bit selects Asynchronous Character Mode. A 1 bit selects Synchronous Character Mode.
7-6	CHARACTER LENGTH	Selects number of bits per character as follows: 0-8 bits 1-7 bits 2-6 bits 3-5 bits

SYNCHRONOUS MODE

Control Register 1

Bit	Name	Function
0	DATA TERMINAL READY	Controls <u>DATA TERMINAL READY</u> output on Pin 17 for control of data set circuit CD. When set to a 1 bit, it enables Carrier and Data Set Ready interrupts. When set to a 0 bit only the Ring interrupt is enabled.
1	REQUEST TO SEND	Controls <u>REQUEST TO SEND</u> output on Pin 32 for control of data set circuit CA. This bit must be a 1 bit and the <u>CLEAR TO SEND</u> input must be low for the transmitter to be enabled and for THREE interrupts to be generated. When this bit is set to a 0 bit the Transmitter is disabled and the <u>RTS</u> output turned off, but not till the end of any current character being transmitted. The <u>RTS</u> output may be used for other functions such as "Make Busy" on 103 data sets.
2	RECEIVER ENABLE	When set to a 1 bit, it enables the receiver allowing received characters to be placed in the Receiver Holding Register, Status Bits 1, 2, 3, and 4 to be updated, and the Data Received interrupt to be generated. When set to a 0 bit, the above status bits are cleared. After this bit is set, character reception starts with a Start bit when in the asynchronous mode, or with two matches to the contents of SYN Register when in the synchronous mode.

Control Register 1 (Sync Mode continued)

Bit	Name	Function
3	PARITY ENABLE	When set to a 1 bit, it enables check of parity on received characters only.
4	DLE STRIP/MISCELLANEOUS	When set to a 1 bit and the receiver is enabled, received characters which match the contents of the DLE Register are stripped out. Also parity checking is disabled. When the receiver is not enabled this bit controls the MISCELLANEOUS output on Pin 5 to be used for New Sync on a 201 Data Set. When operating with a 32X clock for 1 bit with the receiver not enabled causes the receiver bit timing to synchronize on mark-space transitions.
5	TX PARITY ENABLE/FORCE DLE	When set to a 1 bit with Bit 6 of Control Register 1 a 0 bit Transmit Parity is enabled, otherwise no parity is generated. When set to a 1 bit with Bit 6 a 1 bit, it causes the contents of the DLE Register to be transmitted prior to the next character loaded in the Transmitter Holding Register. (See description of Transparency below.)
6	TX TRANSPARENT	When a 1 bit of the transmitter is conditioned for transparent transmission which implies that idle fill will be DLE-SYN and a DLE can be forced ahead of any character in the THR by use of Bit 5. (See description of Transparency.)
7	LOOP/NORMAL	When this bit is set to a 0 bit, the device is configured to provide an internal data and control loop (see Loop feature) and the Ring interrupt is disabled. When this bit is set to a 1 bit the device is in normal full duplex configuration and the Ring interrupt is enabled.

Control Register 2

Bit	Name	Function
2-0	CLOCK SELECT	Selects Transmit and Receive clock as follows: 0 — Transmit and Receive clock input (1X) 1 — Rate 1 (32X) 2 — Rate 2 (32X) 3 — Rate 3 (32X) 4 — Rate 4 (32X) 5 — Rate 4 ÷ 2 (32X) (64X) 6 — Rate 4 ÷ 4 (32X) (128X) 7 — Rate 4 ÷ 8 (32X) (256X)
3	STRIP SYN	When set to a 1 bit and the receiver is enabled, received characters which match the contents of the SYN Register are stripped out. Also the SYN status bit is set with the next character. No SYN stripping occurs with a 0 bit.
4	PARITY ODD/EVEN	A 1 bit selects Odd Parity and a 0 bit selects Even Parity, when parity is enabled.
5	CHARACTER MODE	A 0 bit selects Asynchronous Character Mode. A 1 bit selects Synchronous Character Mode.
7-6	CHARACTER LENGTH	Selects number of bits per character as follows: 0-8 bits 1-7 bits 2-6 bits 3-5 bits

TRANSPARENCY

The Transmit Transparency mode causes Idle Fill to be the pair of characters DLE-SYN rather than a single SYN, and provides for preceding a character loaded into the THR with a DLE without the possibility of an intervening DLE-SYN fill. Transparency is enabled by Bit 6 of Control Register 1, which allows force DLE to be controlled by Control Register 1, Bit 5, but the DLE-SYN fill is not activated until after the first forced DLE. All aspects of Transparency are dis-

abled when Bit 6 is set to a 0 bit. When forcing transmission of a DLE, Bit 5 should be set to a 1 bit prior to loading the Transmitter Holding Register, otherwise the character in the Transmitter Holding Register may be transferred to the Transmitter Register prior to the setting of the Control Bit.

STATUS

The Status Register contains the following status information:

Bit	Name	Function
0	TRANSMITTER HOLDING REGISTER EMPTY (THRE)	This bit is a 1 bit when the Transmitter Holding Register does not contain a character and the transmitter is enabled. It is set to a 1 bit when the contents of the Transmitter Holding Register is transferred to the Transmitter Register. It is cleared to a 0 bit when the Transmitter Holding Register is loaded from the DAL, or when the transmitter is disabled.
1	DATA RECEIVED (DR)	This bit is set to a 1 bit when the Receiver Holding Register is loaded from the Receiver if the Receiver is enabled. It is cleared to a 0 bit when the Receiver Holding Register is read onto the DAL, or when the receiver is disabled.
2	OVERRUN ERROR (OE)	This bit is set to a 1 bit when the previous character in the Receiver Holding Register has <i>not</i> been read, causing DR to not be reset, at the time a new character is ready to be transferred to the Receiver Holding Register; otherwise the bit is cleared when a character is transferred to the Receiver Holding Register. It is cleared when the receiver is disabled.
3	PARITY ERROR/DLE DETECT	This bit is set to a 1 bit when the receiver and Receive parity are enabled and the last received character has a parity error, and is set to a 0 bit if the character has correct parity. When the DLE strip is enabled the Receive parity check is disabled and this bit is set to a 1 bit if the <i>previous character</i> matched the contents of the DLE Register and was stripped, otherwise it is set to a 0 bit. This bit is cleared when the receiver is disabled. When a SYN or DLE character is stripped this bit cannot be reset.
4	FRAMING ERROR (FE)/SYN DETECT (SD)	In the asynchronous mode this bit is set to a 1 bit if the bit after the last data bit of a synchronous character is a zero and the receiver is enabled. The Status bit is set to a 0 bit if the bit is a one. In the synchronous mode this bit is set to a 1 bit when the contents of the Receiver Register matches the contents of the SYN Register and SYN strip is not enabled. In both modes the bit is cleared when the receiver is disabled. If SYN strip is enabled this status bit is updated with the character received after the SYN character. When a SYN or DLE character is stripped this bit cannot be reset.
5	CARRIER DETECTOR	This bit is the complement of the Carrier Detector input on Pin 39.
6	DATA SET READY	This bit is the complement of the Data Set Ready input on Pin 33. With 202-type data sets it can be used for Secondary Receive.
7	DATA SET CHANGE	This bit is set to a 1 bit when there is a change in the state of the Data Set Ready or Carrier Detector inputs with DTR on, or the Ring indicator is turned on with DTR off. This bit is cleared when the Status Register is read onto the DAL.

**Control Registers 1, 2 and STATUS Bit Assignments for
TRUE DATA BUS, Invert for FALSE DATA BUS.**

BIT							
7	6	5	4	3	2	1	0
SYNC/ASYNC 0-LOOP MODE 1-NORMAL MODE	ASYNC 0-NON BREAK MODE 1-BREAK MODE SYNC 0-NON TRANSMITTER TRANSPARENT MODE 1-TRANSMIT TRANSPARENT MODE	ASYNC (TRANS. ENABLED) 0-1½ OR 2 STOP BIT SELECTION 1-SINGLE STOP BIT SELECTION ASYNC (TRANS. DISABLED) 0-MISC OUT = 1 1-MISC OUT = 0 SYNC (CR18 = 0) 0-NO PARITY GENERATED 1-TRANSMIT PARITY ENABLED SYNC (CR18 = 1) 0-NO FORCE DLE 1-FORCE DLE	ASYNC 0-NON ECHO MODE 1-AUTO ECHO MODE SYNC (CR12 = 1) 0-DLE STRIPPING NOT ENABLED 1-DLE STRIPPING ENABLED SYNC (CR12 = 0) 0-MISC OUT = 1 1-MISC OUT = 0	ASYNC 0-NO PARITY ENABLED 1-PARITY CHECK ENABLED ON RECEIVER. PARITY GENERATION ENABLED ON TRANSMITTER SYNC 0-RECEIVER PARITY CHECK IS DISABLED 1-RECEIVER PARITY CHECK IS ENABLED	SYNC/ ASYNC 0-RECEIVER DISABLED 1-RECEIVER ENABLED	SYNC/ ASYNC 0-SETS RTS OUT = 1 1-SETS RTS OUT = 0	SYNC/ ASYNC 0-SETS DTR OUT = 1 1-SETS DTR OUT = 0

CONTROL REGISTER 1

BIT								
7	6	5	4	3	2	1	0	
SYNC/ASYNC CHARACTER LENGTH SELECT 00 = 8 BITS 01 = 7 BITS 10 = 6 BITS 11 = 5 BITS		MODE SELECT 0-ASYNCHRONOUS MODE 1-SYNCHRONOUS MODE	SYNC/ASYNC 1-ODD PARITY SELECT 0-EVEN PARITY SELECT	ASYNC 1-RECEIVER CLOCK DETERMINED BY BITS 2,0 0-RECEIVER CLK = RATE 1 SYNC 0-NO SYN STRIP 1-SYN STRIP		SYNC/ASYNC CLOCK SELECT 000-1X CLOCK 001-RATE 1 CLOCK 010-RATE 2 CLOCK 011-RATE 3 CLOCK 100-RATE 4 CLOCK 101-RATE 4 CLOCK - 2 110-RATE 4 CLOCK - 4 111-RATE 4 CLOCK - 8		

CONTROL REGISTER 2

BIT							
7	6	5	4	3	2	1	0
DATA SET CHANGE	DATA SET READY	CARRIER DETECTOR	FRAMING ERROR SYN DETECT	DLE DETECT PARITY ERROR	OVERRUN ERROR	DATA RECEIVER	TRANSMITTER HOLDING REGISTER EMPTY

STATUS REGISTER

Reg	A1	A0	Read	Write
0	0	0	Control Register 1	Control Register 1
1	0	1	Control Register 2	Control Register 2
2	1	0	Status Register	SYN & DLE Register
3	1	1	Receiver Holding Register	Transmitter Holding Register

INTERRUPTS

The following interrupts can be generated.

Carrier On

The Carrier On interrupt occurs when the Carrier Detector input goes low and DTR is on.

Carrier Off

The Carrier Off interrupt occurs when the Carrier Detector input goes high and DTR is on.

DSR On

The DSR On interrupt occurs when the Data Set Ready input goes low and DTR is on.

DSR Off

The DSR Off interrupt occurs when the Data Set Ready input goes high and DTR is on.

Ring On

The Ring On interrupt occurs when the Ring input goes low and DTR is off.

When an interrupt condition exists the INTR output is made high. Reading the Status Register or MR will allow INTR to go high again.

DATA BUS CONTROLS

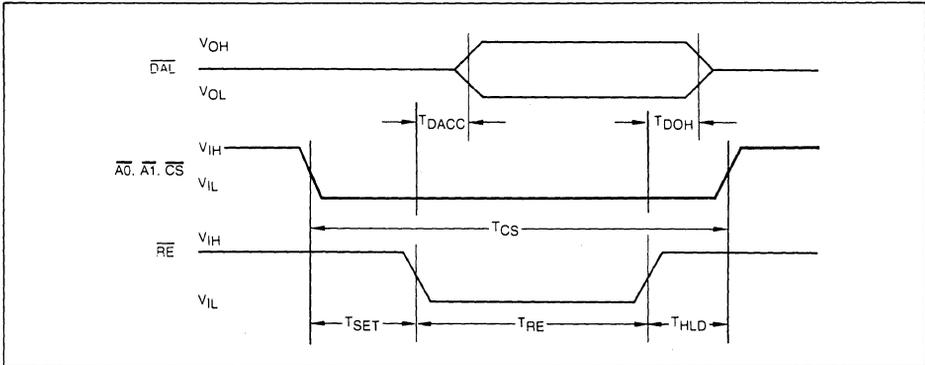
The following Data Bus controls can be generated.

Data Request Out

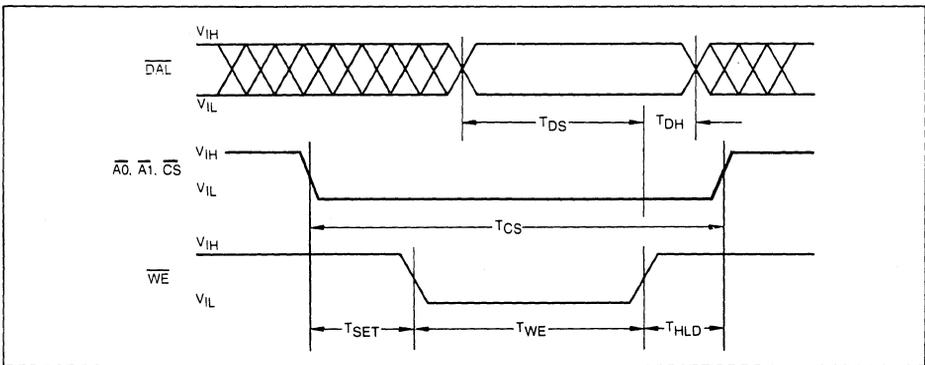
This control signal occurs when the THR is empty while the transmitter is enabled.

Data Request In

This control signal occurs when the RHR is full while the receiver is enabled.



READ TIMING



WRITE TIMING

MAXIMUM RATINGS

V_{DD} with Respect to V_{SS} (Ground)	+ 15 to -0.3V	Storage Temp. Ceramic	-65°C to +150°C
Max. Voltage to any Input with Respect to V_{SS}	+20 to -0.3V	Plastic	-55°C to +125°C
Operating Temperature	0°C to 70°C		
Power Dissipation	600 mW		

OPERATING CHARACTERISTICS

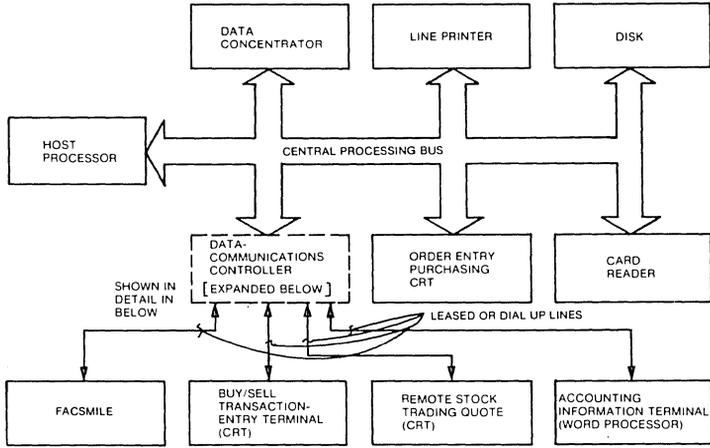
$T_A = 0^\circ\text{C to } 70^\circ\text{C}$, $V_{DD} = +12.0\text{V} \pm .6\text{V}$, $V_{CC} = +5.0\text{V} \pm .25\text{V}$, $V_{SS} = 0\text{V}$

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
I_{LI}	Input Leakage			10	μA	$V_{IN} = V_{DD}$
I_{LO}	Output Leakage			10	μA	$V_{OUT} = V_{CC}$
I_{CCAVE}	V_{CC} Supply Current			80	mA	
I_{DDAVE}	V_{DD} Supply Current			10	mA	
V_{IH}	Input High Voltage	2.4			V	
V_{IL}	Input Low Voltage (All Inputs)			.8	V	
V_{OH}	Output High Voltage	2.8			V	$I_O = -100 \mu\text{A}$
V_{OL}	Output Low Voltage			.45	V	$I_O = 1.6 \text{ mA}$

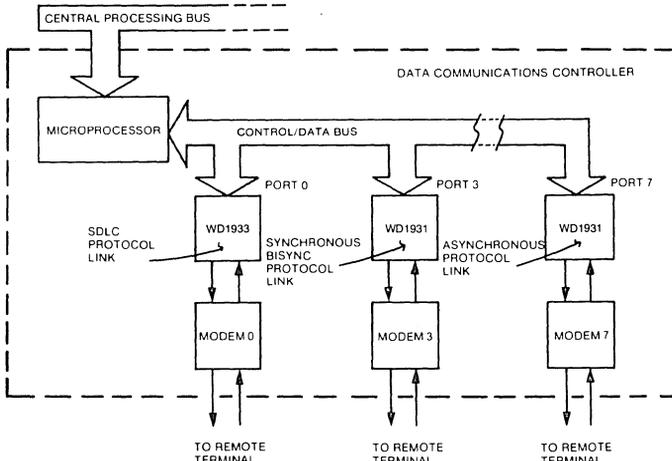
AC CHARACTERISTICS

$T_A = 0^\circ\text{C to } 70^\circ\text{C}$, $V_{DD} = +12.0\text{V} \pm 0.6\text{V}$, $V_{SS} = 0\text{V}$, $V_{CC} = +5.0 \pm .25\text{V}$

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
T_{HLD}	A0, A1 & CS Hold Time	5			ns	
T_{CS}	A0, A1 & CS Width	495			ns	
T_{SET}	A0, A1 & CS Set-Up Time	240			ns	
T_{CYCLE}	Cycle Time	1000			ns	
T_{LOW}	A0, A1 & CS Low Time	250			ns	
T_{MR}	MR Pulse Width	450			ns	
READ						
T_{RE}	\overline{RE} Width	250			ns	
T_{DACC}	Data Access from \overline{RE}			300	ns	$CL = 25 \text{ pf}$
T_{DOH}	Data Hold from \overline{RE}	50		150	ns	$CL = 25 \text{ pf}$
WRITE						
T_{WE}	\overline{WE} Width	250			ns	
T_{DS}	Data Set-Up Time	250			ns	
T_{DH}	Data Hold Time	100			ns	



DATA COMMUNICATIONS SYSTEMS FOR STOCK BROKERAGE FIRM

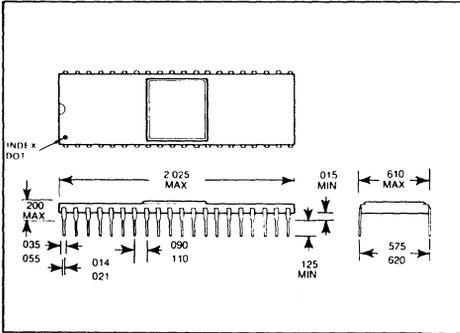


DETAIL OF DATA COMMUNICATION CONTROLLER

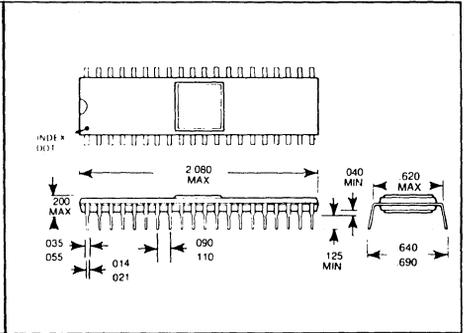
DIGITAL COMMUNICATIONS SYSTEM

The diagrams above illustrate a typical digital system employing several processing levels and digital protocols. It is flexible enough to satisfy several applications. For example, the host processor and remote terminals could be located respectively in airline reservation offices and ticket counters, travel centers and travel agencies, central bank offices and branch banks, or department stores and individual

cash registers. The exploded diagram of the Data-Communications Controller exemplifies the use of one common circuit board design with one 40-pin socket. When the Port requires a character-oriented protocol (synchronous, asynchronous, or synchronous-bisync), the WD1931 is plugged into the socket. For SDLC, HDLC or ADCCP, the WD1933 is used. In addition to storing the design cycle, system flexibility and cost savings are achieved.



WD1931A CERAMIC PACKAGE



WD1931B PLASTIC PACKAGE

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WESTERN DIGITAL

C O R P O R A T I O N

WD1933 Synchronous Data Link Controller

APRIL, 1981

FEATURES

- HDLC, SDLC, ADCCP AND CCITT X.25 COMPATIBLE
- LOOP DATA LINK CAPABILITY
- FULL OR HALF DUPLEX OPERATION
- DC TO 1.5 MBITS/SEC DATA RATE
- DC TO 1.0 MBITS/SEC DATA RATE (SDLC LOOP MODE)
- PROGRAMMABLE/AUTOMATIC FCS (CRC) GENERATION AND CHECKING
- PROGRAMMABLE NRZI ENCODE/DECODE
- FULL SET OF MODEM CONTROL SIGNALS
- DIGITAL PHASE LOCKED LOOP
- FULLY COMPATIBLE WITH MOST CPU'S
- MINIMUM CPU OVERHEAD
- ASYNCHRONOUS/SYNCHRONOUS MULTI-PROTOCOL BOARD CAPABILITY (PIN COMPATIBLE WITH WD 1931)
- FULLY TTL COMPATIBLE
- SINGLE +5V SUPPLY
- ERROR DETECTION: CRC, UNDERRUN, OVERRUN, ABORTED OR INVALID FRAME ERRORS.

- STRAIGHT FORWARD CPU INTERRUPTS
- PROGRAMMABLE MODEM CONTROL INTERRUPTS
- DOUBLE BUFFERING OF DATA
- DMA COMPATABILITY
- END OF BLOCK OPTION
- VARIABLE CHARACTER LENGTH (5, 6, 7 OR 8 BITS)
- RESIDUAL CHARACTER CAPABILITY
- ADDRESS COMPARE
- GLOBAL ADDRESS RECOGNITION
- EXTENDABLE ADDRESS FIELD
- EXTENDABLE CONTROL FIELD
- AUTOMATIC ZERO INSERTION AND DELETION
- MAINTENANCE MODE FOR SELF-TESTING
- 40-PIN PACKAGE

APPLICATIONS

- COMPUTER COMMUNICATIONS
- TERMINAL COMMUNICATIONS
- COMPUTER TO MODEM INTERFACING

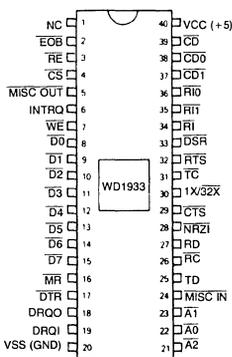


Figure 1 WD1933 PIN CONNECTIONS

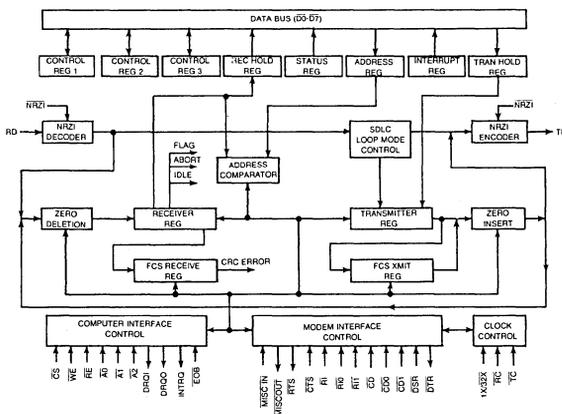


Figure 2 WD1933 BLOCK DIAGRAM

- LINE CONTROLLERS
- FRONT END COMMUNICATIONS
- NETWORK PROCESSORS
- TELECOMMUNICATION SWITCHING NETWORKS
- MESSAGE SWITCHING
- PACKET SWITCHING
- MULTIPLEXING SYSTEMS
- DATA CONCENTRATOR SYSTEMS
- LOOP DATA LINK SYSTEMS
- DMA APPLICATIONS
- COMMUNICATION TEST EQUIPMENT
- LOCAL NETWORKS
- MULTIDROP LINE SYSTEMS

GENERAL DESCRIPTION

The WD1933 is a MOS/LSI microcomputer peripheral device which performs the functioning of interfacing a parallel digital system to a synchronous serial data communication channel employing ISO's HDLC, IBM's SDLC or ANSI's ADCCP line protocol. These protocols are referred to as Bit-Oriented Protocols (BOP).

The chip is fabricated in N-channel depletion load MOS technology and is TTL compatible on all inputs and outputs. This controller requires a minimum of CPU software by supporting a comprehensive frame-level instruction set and by hardware implementation of the low level tasks associated with frame assembly/disassembly and data integrity. It can be programmed to encode/decode in NRZI code. The internal clock is then derived from the NRZI data using a digital phase locked loop.

The receiver and transmitter logic operate as two total independent sections with a minimum of common logic. The frames are automatically checked for errors during reception by verifying the Frame Check Sequence (FCS). In transmit mode, the FCS is automatically generated by this controller and sent before the final Flag. It also continuously checks for other errors. In a case of an error, the CPU is interrupted.

The controller recognizes and can generate Flag, Abort, Idle and GA characters. WD1933 can be used in a SDLC

Loop configuration. An End of Block option is supplied to minimize CPU time. A full set of modem control signals are supplied to minimize external hardware.

A BRIEF DESCRIPTION OF HDLC, SDLC AND ADCCP PROTOCOLS

The WD1933 is compatible with HDLC, SDLC and ADCCP standard communication Link Protocols. These are bit-oriented, code independent, and ideal for full duplex communication. A single communication element is called a FRAME, which can be used for both link control and data transfer purposes.

The elements of a frame are the beginning eight bit FLAG (F) consisting of one logical "0," six 1's and a 0, an eight bit ADDRESS-FIELD(A), an eight bit CONTROL-FIELD (C), a variable (N bits) INFORMATION-FIELD, a sixteen bit FRAME-CHECK-SEQUENCE (FCS), and an eight bit end FLAG (F), having the same bit-pattern as the beginning flag.

In HDLC, the address (A) and control (C) characters are extendable (more than one character). An important characteristic of a frame is that its contents are made code transparent by use of a zero bit insertion and deletion technique. Thus, the user can adapt any format or code suitable for his system. The frame is bit-oriented, meaning that, bits not characters in each field have specific meanings. The Frame Check Sequence (FCS) is an error detection scheme similar to the Cyclic Redundancy Checkword (CRC) widely used in magnetic disk storage devices. The frame format is shown in Figure 4.

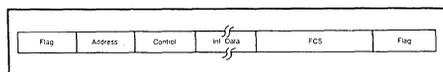


Figure 4 WD1933 HDLC FRAME FORMAT

Where:

FLAG = 01111110

Address field—One or more 8-bit characters defining the particular station

Control field—One or two 8-bit characters

Information field—Any number of bits (may be zero bits)

Frame Check Sequence—16-bit error checking field

The following features are also part of these protocols.

ZERO INSERTION/ZERO DELETION—Zero insertion/deletion is performed within the 2 Flags of a frame. If there are more than five 1's in a row, a 0 is automatically inserted after the fifth 1 and it is deleted upon reception by the receiver.

FRAME CHECK SEQUENCE (FCS)—A 16 bit cyclic redundancy check (CRC) calculation is performed during transmission of the data in between the 2 flags of the frame. The CRC is then transmitted after the I-field and before the final FLAG. Upon reception the receiver also performs a CRC calculation on the incoming data. If there were no transmission error, the Receiver CRC equals F0B8 (hex).

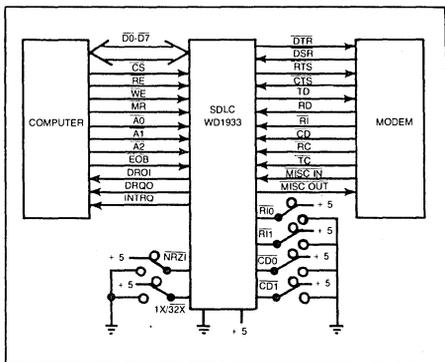


Figure 3 WD1933 TYPICAL SYSTEM INTERFACE

DESCRIPTION OF PIN FUNCTIONS

The WD1933 is packaged in a 40 pin DIP. The following is a functional description of each pin. A bar over a signal (SIGNAL), means active Low.

Table 1 DESCRIPTION OF WD1933 PIN FUNCTIONS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1		NC	No connection allowed to this pin. Used internally only.
2	End of Block	\overline{EOB}	This input, when low, function as an FCS command. Is independent of \overline{CS} .
3	Read Enable	\overline{RE}	This input, when low (and \overline{CS} is active), gates the content of addressed register onto the Data bus.
4	Chip Select	\overline{CS}	This input, when low, selects the WD1933 for a read or write operation to/from the Data bus.
5	Misc Output	$\overline{MISC\ OUT}$	This output is an extra programmable output signal for the convenience of the user. Is controlled by the CR10 bit.
6	Interrupt Request	INTRQ	The output is high whenever any of the interrupt register bits, IR7-IR3 are set.
7	Write Enable	\overline{WE}	This input when low (and \overline{CS} is active), gates the content of the Data bus into the addressed register.
8-15	Data Bus	$\overline{D0-D7}$	Bidirectional three-state Data Bus. Bit 7 is MSB.
16	Master Reset	\overline{MR}	This input, when low, initializes all the registers, and forces the WD1933 into an idle state. The WD1933 will remain idle until a command is issued by the CPU.
17	Data Terminal Ready	\overline{DTR}	Modem Control Signal. This output when low, indicates to the Data Communication Equipment (DCE) that the WD1933 is ready to transmit or receive data.
18	Data Request Output	DRQO	This output, when high, indicates that the Transmitter Holding Register (THR) is empty and ready to receive a data character from the Data bus for a transmit operation.
19	Data Request Input	DRQI	This output, when high, indicates that Receiver Holding Register (RHR) contains a newly received data character, available to be read onto the Data bus.
20	V _{SS}	V _{SS}	Ground
21,22,23	Address Lines	$\overline{A2}, \overline{A0}, \overline{A1}$	These inputs are used to address the CPU interface registers for read/write operations.
24	Misc Input	$\overline{MISC\ IN}$	This input is an extra input signal for the convenience of the user. The state is shown by the SR4 bit.
25	Transmitted Data	TD	This output transmits the serial data to the Data Communications Equipment/Channel.
26	Receive Clock	\overline{RC}	This input is used to synchronize the received data.
27	Received Data	RD	This input receives the serial data from the Data Communication Equipment/Channel.
28	NRZI	\overline{NRZI}	This input, when low, sets the WD1933 in NRZI mode.
29	Clear to Send	\overline{CTS}	Modem Control Signal. This input when low, indicates that the DCE is ready to accept data from the WD1933.
30	DPLL Select	$1X/32X$	This input controls the internal clock. When high (1X clock), the external clock has the same frequency as the internal clock. When low (32X clock), the external clock is 32 times faster than the internal clock and the DPLL Logic is enabled.
31	Transmit Clock	\overline{TC}	This input is used to synchronize the transmitted data.
32	Request to Send	\overline{RTS}	Modem Control Signal. This output, when low, indicates to the DCE that the WD1933 is ready to transmit data.
33	Data Set Ready	\overline{DSR}	Modem Control Signal. This input, when low, indicates that the DCE is ready to receive or transmit data.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
34	Ring Indicator	\overline{RI}	Modem Control Signal. This input, when low, indicates a ringing signal being received on the communication channel.
35,36	Ring Indicator Interrupt Control	$\overline{RI1}, \overline{RI0}$	These inputs are used to program Ring Indicator interrupts.
37,38	Carrier Detect Interrupt Control	$\overline{CD1}, \overline{CD0}$	These inputs are used to program Carrier Detect Interrupts.
39	Carrier Detect	\overline{CD}	Modem Control Signal. This input, when low, indicates there is a carrier signal received by the local DCE from a distant DCE.
40	V _{CC}	V _{CC}	+5VDC

Table 1 DESCRIPTION OF WD1933 PIN FUNCTIONS

TERMINOLOGY

TERM	DEFINITION/DESCRIPTION
BOP	Bit-oriented protocols: SDLC, HDLC, and ADCCP
ABORT	11111111 (seven or more contiguous 1's)
GA	Go-ahead pattern. 01111111 (0(LSB) followed by seven 1's)
LSB	First transmitted bit and first received bit. (Least significant bit)
MSB	Last transmitted bit and last received bit. (Most significant bit)
IDLE	11111111 11111111 (15 or more contiguous 1's)
FLAG	01111110. Starts and ends a Frame.
A-FIELD	Address-field in the Frame. Consists of one or more 8-bit characters. Defines the address of a particular station.
C-FIELD	Control field in the Frame. Consists of one or two 8-bit characters.
I-FIELD	Information field in the Frame. Consists of any number of bits.
FCS	Frame Check Sequence. A 16-bit error checking field sequence.
FRAME	A communication element, consisting of a minimum of 32 bits, and is always delimited by FLAGS.
GLOBAL ADDRESS	An A-field character of eight 1's. When this is compared and matched in the Address comparator, the DRQI will be set, indicating a valid address
RESIDUAL CHARACTER	The last I-field character, consisting of a lesser amount of bits than the other I-field characters in the Frame.
DATA SET	Data Communication Equipment (DCE). May be a modem.
BIT TIME	Length in time of a serial data bit.

Table 2 WD1933 TERMINOLOGY

HARDWARE ORGANIZATION

The WD1933 block diagram is illustrated in Figure 2 and described below.

CPU Interface Registers

All of these registers are addressable and to be read from and/or written into by the CPU via the Data bus. These are 8-bit registers and have to be enabled via Chip Select (CS) before any data transfer can be done.

CONTROL REGISTER 1, 2, 3 (CR1, 2, 3) Operations are initiated by writing the appropriate commands into these registers. CR1 should be programmed last.

RECEIVER HOLDING REGISTER (RHR) When Data Request Input is set (DRQI=1), contains received assembled character.

ADDRESS REGISTER (AR) Contains the address of this WD1933, which is to be compared to the received address character (A-field).

INTERRUPT REGISTER (IR) Contains the cause of the current interrupt request.

TRANSMITTER HOLDING REGISTER (THR) Is to be loaded with the next in line character to be transmitted, when Data Request Output is set (DRQO=1).

STATUS REGISTER (SR) Contains the overall status of the WD1933, plus some information of the last received frame.

Non-Addressable, Internal Registers

These registers are transparent to the user, but is mentioned in these data sheets to help the understanding of the WD1933.

TRANSMITTER REGISTER (TR) This 8-bit register functions as a buffer between the THR and the TD output. Is loaded from the THR (if Data Command) with the next character to be transmitted. An ABORT or FLAG character may also be loaded into this register under program control. This character is automatically shifted out to the Transmit Data output. When the last bit of the current transmitted character has left the TR register, a new character will be loaded into this register, setting DRQO (Data command) or INTRQ (Abort, Flag or FSC command). If at the time when only one bit remains left in the TR register, the THR is not loaded or a new command is not programmed (Data command), an underrun error will occur.

RECEIVER REGISTER (RR) The received data is, via the Zero-Deletion logic shifted into this 8-bit register. The data is here assembled to a 5, 6, 7 or 8-bit character length and then, under the right conditions, parallel transferred to the RHR register.

FCS RECEIVE REGISTER AND FCS XMIT REGISTER The WD1933 contains a 16-bit CRC check register (FCS REC. REG.) and a 16-bit CRC generation register (FCS XMIT REG.). The general polynomial is:

$$G(X) = X^{16} + X^{12} + X^5 + 1$$

The transmitter and receiver initialize the remainder value to all ones before CRC accumulation starts. The polynomial is multiplied by X^{16} and is divided by $G(X)$. Inserted 0's are not included in the accumulation. Under program control, the complement called the frame check sequence (FCS) is sent with high order bit first.

Various Internal Circuits

ADDRESS COMPARATOR This 8-bit comparator is used to compare the contents of the Address Register with the first address character of the incoming frame. This feature is enabled by a bit in the Command Register. If enabled and there is a match, the received frame is valid and DRQIs are generated for every character received (including the A-field). If enabled and there is not a match or there is no Global Address, the received frame is discarded. If not enabled, all received frames are valid and DRQIs are generated.

ZERO INSERTION The transmitted data stream is continuously monitored by this logic. A zero is automatically inserted following five contiguous 1 bits anywhere between the beginning FLAG and the ending FLAG of a frame. The insertion of the zero bit thus applies to the contents of the Address, Control, Information Data, and the FCS field.

ZERO DELETION The received data stream is continuously monitored by this logic. Upon receiving five contiguous 1 bits, the sixth bit is inspected. If the sixth bit is a 0, it is automatically deleted from the data stream. If the sixth bit is a 1, the seventh bit inspected; if it is a 0, a FLAG is recognized; if it is a 1 an ABORT or GO AHEAD is recognized.

DATA BUS (D7-D0) This is an inverted 8-bit bidirectional data bus.

SDLC LOOP-MODE CONTROL This logic supervises the WD1933 running in SDLC Loop mode. It monitors the received data for a GO-AHEAD pattern in the case when SDLC LOOP MODE bit (CR22) and ACT TRAN bit (CR16) are set. When GO-AHEAD pattern is received, this logic suspends the repeater function and initiates the transmitter function. For more details, see functional description of SDLC Loop Mode.

NRZI ENCODER/DECODER When this mode is selected, the NRZI Encoder encodes the "normal" transmitted data to NRZI formatted data and the NRZI Decoder decodes the received NRZI data to "normal" data.

A binary 1 for "normal data" is TD = high.

A binary 1 for NRZI data is TD = no change.

A binary 0 for "normal data" is TD = low.

A binary 0 for NRZI data is TD = change of state.

COMPUTER INTERFACE CONTROL This logic interfaces the CPU, to the WD1933. It supervises the read and write functions to the addressable registers, generates data requests and interrupts, decodes and initiates commands, monitors the status of WD1933 etc.

MODEM INTERFACE CONTROL This logic interfaces and supervises the modem control signals to/from the WD1933. It provides both dedicated (EIA Standard) and user defined control functions.

CLOCK CONTROL This logic interfaces the transmit and receive clocks to the WD1933. It converts the external clocks to the necessary internal clocks.

FUNCTIONAL DESCRIPTION

SDLC Loop Mode

The diagram below shows an SDLC LOOP Data Link System. WD1933 can be used in any of these stations.

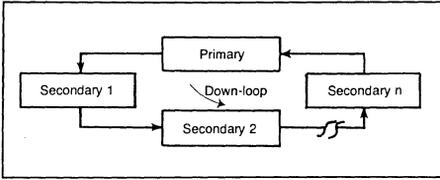


Figure 5 WD1933 SDLC LOOP DATA LINK

Each secondary station is normally a repeater in Receive mode. The primary station is the loop controller. Signals sent out on the loop by the primary station are relayed from station to station, then back to the Primary. Any secondary station finding its address in the A-field captures the frame for action at that station. All received frames are relayed to the next station on the loop.

If anyone of the secondary stations wants to transmit a message, it sets its ACT TRAN bit and waits for a GO-AHEAD (GA) pattern. The WD1933 recognizes seven or more contiguous logical 1's as a GO-AHEAD pattern. Until GA pattern is received, this secondary station continues operating as a repeater. When primary station is done transmitting, it may send a continuous stream of GA patterns down the Loop. This may be accomplished by going Idle. When the first in turn secondary station, with the ACT TRAN bit set, receives the GA pattern, it suspends the repeater function and immediately goes into transmit mode. It transmits its message and when completed, it resets the ACT TRAN bit. This converts the secondary station back to repeater mode. The GA-patterns still transmitted by the Primary Station, gets relayed down the Loop to the next secondary station. The next down-loop secondary station has the opportunity to transmit in the same manner. When the primary station receives the GA-pattern, all the secondary stations have been able to transmit their messages, and the

cycle is completed. The Primary Station may then transmit or initiate another cycle as described above. As a repeater, the transmitted data is delayed by 4 bits (NRZI=5 bits) relative to the received data.

1X/32X Clock Option

When 1X clock is selected, the data rate equals the external clock (receiver and transmitter).

When 32X clock is selected, the external clock rate is 32 times faster than the data rate.

Digital Phase Locked Loop (DPLL)

This feature is particularly useful in NRZI mode. The purpose of the DPLL is to synchronize the internal 1X clock to the received data, thus insuring that this data is sampled in the middle of the incoming serial bit. DPLL is automatically in operation when 32X clock is selected.

The DPLL Logic initiates at the first received data transition in a frame. Corrections, if needed, are then made for each received data transition. A 32-counter is used for this operation. At the beginning of each frame and at the first received data transition, this 32 counter is reset. From this time on, the counter increments with one count for each external clock pulse. At count 16 the internal 1X clock is forced to change state to high (this transition = sampling time). At count 32, the counter resets itself. This forces the internal 1X clock again to change state back to low.

At each received data transition, if the internal clock and the received data is out of synchronization, a correction is automatically made by ± 1 external clock period. See DPLL Timing Diagram in Figure 6.

End Of Block (EOB)

This is an FCS command. The main purpose of EOB is to allow the user to initiate FCS and FLAG without the need of

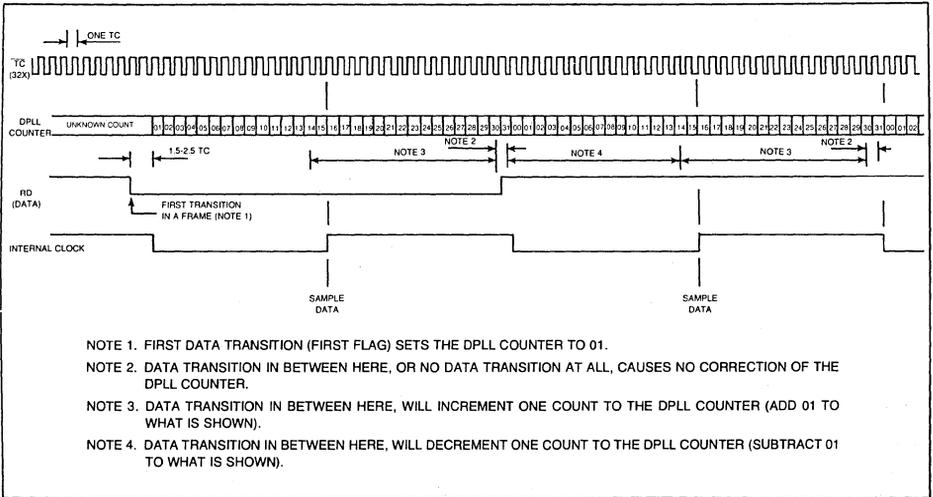


Figure 6 WD1933 DPLL TIMING DIAGRAM

using extra computer time. This is particularly practical in DMA applications. At the end of a frame, when the last information data character has already been loaded into the THR and once again DRQO is set, either a regular FCS command is written into CR1 Register, or EOB is to be activated. At the end of FCS, when INTRQ is set (XMIT OPCOM), the EOB if activated is to be reset again.

Serial Data Synchronization

The serial data is synchronized by the externally supplied Transmit Clock (TC) and Receive Clock (RC). When 1X clock is selected, the falling edge of TC generates new transmitted data and the rising edge of RC is used to sample the received data. When 32X clock is selected, a 32-counter (in the DPLL Logic) is used to synchronize the internal clock. At time 0, when the counter is reset to 0, the new transmitted data is generated. At time 16 (counter = 16) the received data is sampled, insuring that sampling is done in the middle of the received serial bit. At count 32, the counter is reset to 0 again.

Self Test (Diagnostic) Mode

This feature is a programmable Loop back of data, enabling the user to make a complete test of the WD1933 with a minimum of external circuitry. In this mode, transmitted data to the TD pin, is internally routed to the received data input circuitry, thus allowing a CPU to send a message to itself to verify proper operation of the WD1933. The modem control signals DTR and RTS are deactivated (off) to insure no interference to/from the Data Communication Equipment (DCE). DSR and CTS are internally activated for proper input conditions. TC and RC should be supplied by the same source if 1X clock is selected.

Auto Flag

If this is selected and Data Command is executed, continuous Flags will be sent between frames. This eliminates the need to execute the Flag Command. In DMA applications in particular, this is very practical.

Extended Addressing

This type of addressing means, that there is more than one address character in the A-field. In receive mode, the first address character is compared in the Address Comparator of the WD1933. The other address character/s is to be compared by the CPU. The last address character is recognized by the fact that the LSB (bit 2ⁿ) is a 1.

PROGRAMMING

Controlling Operation

Prior to initiating data transmission or reception, CONTROL REGISTER 1-3 (CR1-3) must be loaded with control information from the CPU. The contents of these registers will configure the WD1933 for the user's specific data communication environment. These registers should be loaded during power-on initialization and after a reset operation. They can be changed at any time that the respective transmitter or receiver is deactivated. The CR1-3 dictate what the transmitter will send: the type of character (DATA, ABORT, FLAG or FCS), the number of bits per character, and the number of bits in the residual character. Similarly, they tell the receiver the types of frames to look for: the number of bits per I-field character, whether to perform an address compare, and whether to watch for an extended address. The Control Register also control Data Terminal Ready (DTR), Misc Out and the activation of both the transmitter and the receiver. For more detailed information, see Register Formats.

Monitoring Operation

Monitoring is done by use of the Interrupt Register (IR) and Status Register (SR). The IR register indicates when a frame is completed (transmitted or received), if there was an error and if there is a Data Set Change. It also monitors the states of INTRQ, DRQO and DRQI.

The SR register indicates if an error is recognized by IR and what type of error. It also monitors the modem control signals; Ring Indicator (RI), Carrier Detect (CD), Data Set Ready (DSR) and Misc In.

Furthermore, the SR register monitors if the Receiver is idle, and also if in receive mode if the user has programmed the Receiver Character Length to be 8 bits per character, this register indicates the number of residual bits received. For more detailed information, see Register Formats.

Read/Write Control Of CPU Interface Registers

These registers are directly accessible from the CPU bus (D7-D0) by a read and/or write operation by the CPU.

The CPU must set up the WD1933 register address (A2-A0), Chip Select (CS), Write Enable (WE) or Read Enable (RE) before each data bus transfer operation.

During a write operation, the falling edge of WE will initiate a WD1933 write cycle. The addressed register will then be loaded with the content of the Data Bus (D7-D0). During a read operation, the falling edge of RE will initiate a WD1933 read cycle. The addressed register will then place its content

onto the Data Bus ($\overline{D7-D0}$). The read/write operation is completed, when \overline{CS} or $\overline{RE/WE}$ is brought high.

For more detailed information, timing, etc., see Read/Write Timing diagram.

For read and write operation, the CR1-3 registers need no external clock. To reset CR1-3, \overline{TC} clock is required. The AR and THR registers need no external clock, and can only be written into. The RHR, IR and SR registers need Transmit

Clock (\overline{TC}) or Receive Clock (\overline{RC}) to set various bits, and are read-only.

All these registers will get initialized by a Master Reset. A read operation of RHR resets the DRQI. A write operation to THR, resets the DRQO. A read operation of IR, resets IR bits 0 and 3-7. A read operation of SR, resets SR bits 0-2.

For addressing and external clocks needed, see figure below.

\overline{CS}	$\overline{A2}$	$\overline{A1}$	$\overline{A0}$	Read	Write	External Clock
L	H	H	H	CR1	CR1	None*
L	H	H	L	CR2	CR2	None*
L	H	L	H	CR3	CR3	None*
L	H	L	L	RHR	AR	RHR= \overline{RC} . AR=None
L	L	H	H	IR	THR	IR= \overline{TC} . THR=None
L	L	H	L	SR	—	SR0-3= \overline{RC} . SR4-7=None.
H	X	X	X	X	X	

L = VIL at pins
H = VIH at pins
X = Don't care

*Master Reset requires \overline{TC} .

REGISTER FORMATS

Below shows a short form register format.

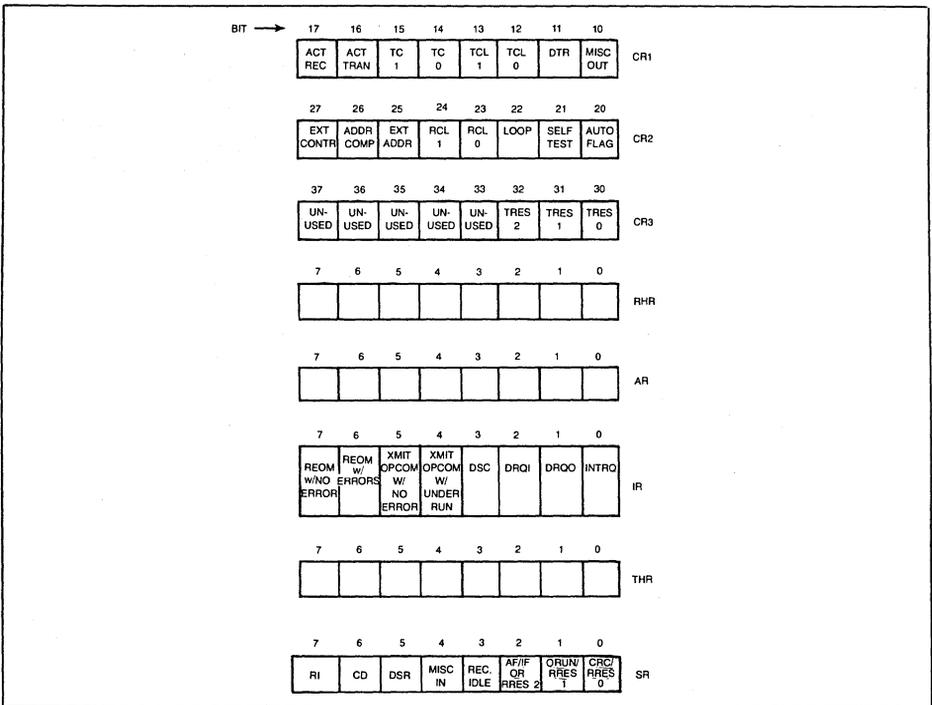


Figure 7 WD1933 BIT ASSIGNMENTS

A more detailed description is shown here of each bit location. It should be known, that because the Data Bus Lines (D7-D0) has inverted logic, a logic 1 (set) means low state. Also, a modem control signal which is inverted (example DTR), is in on-state (set) when low.

Control Register 1 (CR1)

When initiating a transmit/receive operation, this should be the last register programmed.

Miscellaneous Output (CR10) This bit controls the Miscellaneous Output signal to the data set. When CR10 is a logical 0, Misc Out is off, when it is a logical 1, Misc Out is on.

DTR Command (CR11) This bit controls the data Terminal Ready ($\overline{\text{DTR}}$) signal to the data set. When CR11 is a logical 0, $\overline{\text{DTR}}$ is off. When CR11 is a logical 1, $\overline{\text{DTR}}$ is on. When the Self-Test mode is selected, $\overline{\text{DTR}}$ signal is forced to an off state.

Transmitter Character Length (CR13, 12) These bits control the transmitted I-field data character length. The data character may be 5, 6, 7 or 8 bits long.

CR13 (TCL1)	CR12 (TCL0)	Bits Per Character
0	0	8
0	1	7
1	0	6
1	1	5

Transmitter Commands (CR15, 14) These bits control the transmission of DATA (A-field, C-field and I-field), ABORT, FLAG, and FCS (FCS plus FLAG). When these commands are programmed, the previous command currently still in progress, will complete the transmission of its character. When this is done, a new character generated by this new command, will be transmitted.

If DATA is programmed, the new character to be transmitted will be the character loaded (or still to be loaded) in the THR register. If ABORT is programmed, the new character will be eight logical 1's. If FLAG is programmed, the new character will be 01111110. If FCS is programmed, three new characters will be transmitted; first the 16-bit content of the FCS XMIT REGISTER, then a FLAG. One serial data bit time ahead of the first bit (LSB) of this new character (= FLAG character when FCS command) being transmitted, the CPU is signalled that the WD1933 is again ready to receive a new command. This signal is an INTRQ (XMIT OPCOM), if the now current command is ABORT, FLAG or FCS. This signal is a DRQO, if the current command is DATA. However, in this latter case (DATA), the user has two choices; 1. Change the command. 2. Keep the DATA command and load a new character into the THR register. For more information, please see the Transmission Timing diagram, Figure 8.

Programming, see figure below.

CR15 (TC1)	CR14 (TC0)	Command	Character/s Transmitted	Signal to CPU
0	0	DATA	Content of THR	DRQO
0	1	ABORT	1111 1111	INTRQ
1	0	FLAG	0111 1110	INTRQ
1	1	FCS	FCS + 01111110	INTRQ

Activate Transmitter (CR 16) This bit when set, enables the transmitter and sets RTS signal. If in SDLC Loop Mode (CR22 = set), the transmitter waits for a Go-Ahead pattern before the transmitter is enabled.

Activate Receiver (CR 17) This bit when set activates the receiver, which begins shifting in frames one character at a time into RR register for inspection.

CONTROL REGISTER 2 (CR2)

Auto Flag (CR20) When set, Flags (without INTRQs) will be continuously transmitted in between frames, when otherwise the transmitter would be in idle state.

Self-Test Mode (CR21) When set, the Transmitter Data Output is internally connected to the Receiver Data input circuitry. The modem control output signals are deactivated (off state). The modem control input signals are internally activated. This mode allows off-line diagnostic.

SDLC Loop Mode (CR22) When set, the WD1933 is conditioned to operate in an SDLC Loop Data Link system (see SDLC Loop Mode).

Receiver Character Length (CR24, 23) These bits indicate to the receiver how many bits per character there are to assemble for the I-field. The I-field characters may be 5, 6, 7 or 8 bits long. The unused bits read from RHR will be logical 0.

CR24 (RCL1)	CR23 (RCL0)	Bits Per Character
0	0	8
0	1	7
1	0	6
1	1	5

Extended Address (CR25) When set, this bit indicates to the receiver that there is more than one address character in the A-field. The receiver will expect another address character if the LSB in the current address character is a logical 0. The purpose of this bit: If a non-8-bit I-field character length is expected, the DRQIs will get out of synchronization if the WD1933 does not know exactly when the I-field will start. Not used in transmit mode.

Address Compare (CR26) When set, the first address character will be inspected in the Address Comparator. If there is a match with the AR register, or if the address compared is a Global Address (eight 1's) the frame is considered valid, causing DRQIs to be generated. Otherwise, the receiver does not react, and will continue comparing for a new valid address. If not set, all frames are considered valid.

Extended Control (CR27) When set, indicates that there are two control characters per frame. If not set, there is only one control character per frame. The purpose of this bit: If a non-8-bit I-field character length is to be received, the DRQIs will get out of synchronization if the WD1933 does not know when the I-field will start. Not used in transmit mode.

CR32 (TRES 2)	CR31 (TRES 1)	CR30 (TRES 0)	Residual Char. Length
0	0	0	No residual char. sent
0	0	1	1 bit
0	1	0	2 bits
0	1	1	3 bits
1	0	0	4 bits
1	0	1	5 bits
1	1	0	6 bits
1	1	1	7 bits

CONTROL REGISTER (CR3)

Transmit Residual Character Length (CR32, 31, 30) These bits inform the transmitter what bit-length the residual character will be. If no residual character is to be sent, these bits must be set to logical 0.

Unused (CR33-37) These bits are not used, and are always a logical 0.

INTERRUPT REGISTER (IR)

This register contains the information why an interrupt (INTRQ) was generated. An IR register read operation, will reset bits 0, and 3-7.

Loading the THR register, will reset DRQO (bit 1). Reading the RHR register, will reset DRQI (bit 2). A new interrupt will occur if one is pending.

If a new interrupt is generated while the CPU is reading the IR register, this new interrupt will set the respective bit in the IR register one bit time later (this to avoid losing any interrupt). The status of bits 3-7 will accumulate until the IR register is read by CPU.

INTRQ (IR0) When set, indicates an interrupt and that there are one or more bits set in positions 3 through 7 of this register. This bit is a mirror image of INTRQ signal (pin 6).

DRQO (IR1) When set, indicates a Data request output. This bit is a mirror image of DRQO signal (pin 18).

DRQI (IR2) When set, indicates a Data Request input. This bit is a mirror image of DRQI signal (pin 19).

Data Set Change (IR3) When set, indicates a change of state of the Data Set (Data Communication Equipment). This is a change of state of DSR, CD or RI. The type of change of CD and RI that this bit will react to, is programmed by use of input signals CD1/CD0 and RI1/RI0 and is shown below.

XMIT Operation Complete with Underrun Error (IR4) When set, indicates that the transmitter command has been completed and there was an Underrun error. An Underrun error occurs when the Data Request Output (DRQO) is set, but THR register is not loaded in time.

XMIT Operation with No Error (IR5) When set, indicates that the transmitter command has been completed and there was no error.

Received End of Message With Errors (IR6) When set, indicates that a Received End of Message is detected, and there was an error. Errors include CRC, Overrun, Invalid Frame and Aborted Frame.

The SR Register bits 0-2 will indicate the exact type of error.

Received End Of Message With No Error (IR7) When set, indicates that a Received End of Message is detected, and there was no error.

CD1	CD0	Interrupting edge of CD	RI1	RI0	Interrupting edge of RI
LO	LO	Rising and falling	LO	LO	Rising and falling
LO	HI	Falling	LO	HI	Falling
HI	LO	Rising	HI	LO	Rising
HI	HI	None	HI	HI	None

STATUS REGISTER (SR)

This register contains the status of the receiver and some modem control signals. It also indicates (if REOM w/Errors) exactly what type of errors. If the Receiver Character Length is 8 bits, this register indicates the amount of Residual bits that was received. A read operation will reset bits 0-2.

Received Error/Received Residual Character Length (SR 2-0) If REOM w/NO ERROR (IR7) is set, and the Receiver, Character Length (CR24, 23) is 8 bits, these bits (SR 2-0), indicate the number of residual bits received.

If REOM WITH ERROR (IR 6) is set, these bits indicate the type of error that occurred, as shown in figure below.

Bit Set	Error
SR0	CRC
SR1	Overrun
SR2	Aborted or Invalid frame

Receiver Idle (SR 3) When set, indicates that the receiver is currently IDLE.

Miscellaneous Input (SR4) This is a mirror image of MISC IN signal. When this signal is set, SR4 bit is set.

Data Set Ready (SR5) This is mirror image of $\overline{\text{DSR}}$ signal. When this signal is set, SR5 bit is set.

Carrier Detect (SR6) This is a mirror image of $\overline{\text{CD}}$ signal. When this signal is set, SR6 bit is set.

Ring Indicator (SR7) This is a mirror image of $\overline{\text{RI}}$ signal. When this signal is set, SR7 bit is set.

TRANSMITTER OPERATION

Prior to this operation, the programmable inputs and the transmit mode related register bits need to be programmed according to the user's specific data communications environment. The last bit to be set is always the ACT TRAN (CR16) bit.

Before this, the INTRQ has to be cleared, which can be done by reading the IR register. For more detailed information how to program the WD1933, see Programming.

As an example of how to program the WD1933, let's assume a 24-bit information is to be transmitted. The I-field would then consist of three 8-bit characters with no residual bits. CR3 should then be 00 (Hex).

If Auto Flag is selected, CR20 has to be set, CR21 and CR22 should be logical 0's, as this example is no Self-test and no SDLC Loop Mode.

Bits CR23-CR27 are for reception only (see Receiver Operation). The last register to be programmed is CR1. If MISC OUT is not used, this may be ignored. If a modem is used, DTR (CR11) is to be set. CR14 and CR12 should be logical 0's (8-bit char. length). CR15 and CR14 should be logical 0's (Data Command). ACT TRAN (CR16) bit is to be set. The ACT REC (CR17) is for reception only.

The DTR bit, when set, activates the $\overline{\text{DTR}}$ signal, indicating to the modem to prepare for communication. When the modem is ready, it sends back a Data Set Ready ($\overline{\text{DSR}}$) to the WD1933. This causes the DSC (IR3) bit to set, which in turn activates INTRQ. The IR register is now read. Simultaneously, when the ACT TRAN (CR16) bit is set, this activates the Request to Send ($\overline{\text{RTS}}$) signal, instructing the modem to enter into transmit mode. When the modem is ready to trans-

mit data, it responds by activating the Clear to Send ($\overline{\text{CTS}}$) signal.

The WD1933 is now conditioned to transmit. Now DRQO gets set, indicating to the CPU (or DMA) to load the first character (Address) into the THR. When this is done, DRQO will reset. As soon as the WD1933 is ready to be loaded with the next character to be transmitted, DRQO is again set. When the THR register is again loaded with a character, DRQO will again reset.

This same sequence continues until the last I-field character to be transmitted is loaded into the THR. If CRC checking is to be used, the next time when DRQO is set, an FCS command has to be programmed. This is accomplished by either setting CR15, 14 to both logical 1's or by activating the EOB signal.

At the end of the FCS being transmitted, INTRQ will set indicating XMIT Operation Complete. The IR register is to be read to find out whether the frame was sent with or without error. Also the FCS Command which was used as described above has to be changed. If CR15, 14 were set, these have to be reset (to Data Command), or if EOB was activated, this signal has to be deactivated. At this same time, the ACT TRAN bit is allowed to be reset, causing the TD output to go idle after the end Flag is sent. If the ACT TRAN bit is kept set, continuous Flags will be sent following the FCS.

If a new frame is to be sent right after this first frame, only one Flag is needed in between frames, meaning the frames have one common Flag character. In this case, the second frame Address character may be loaded at the same time the FCS command is programmed during the first frame. Also, the ACT TRAN bit should be kept set in between frames. Every time DRQO gets set, the user must load the THR register before the last loaded character only has 1.5 bits left to be transmitted. In other words, when DRQO gets set, the user may wait (if 8-bit characters) up to 7.5 serial data bits before loading the THR. If THR is not loaded within this time, an Underrun error will occur.

If Auto Flag is not selected (CR20 = logical 0) the sequence will be a little different than described below. When the first DRQO is set, and after the Address character is loaded into THR, a Flag command is also programmed (CR15, 14 = 10).

This will set an interrupt (INTRQ), which indicates that the IR register must be read. Now, the Data Command is reprogrammed (CR15, 14 = 00).

For more information, see Transmission Timing diagram.

ABORT CONDITIONS

The function of prematurely terminating a data link is called an "Abort." The transmitting station aborts by sending eight consecutive 1's. Unintentional Abort caused by 1's in the A-C- or I-field is prevented by zero insertion. Intentional Abort may be sent by programming an Abort command. Abort will also be sent in the case where THR is not loaded in time or FCS command is not programmed in time (=underrun). This means that after the DRWO is set, to avoid Abort; THR must be loaded, EOB activated or FCS command programmed before there is only 1.5 bits left of the last character to be transmitted.

If this is not done, INTRQ (XMIT OPCOM w/underrun) is set and Aborts are transmitted until, either the command is changed or the THR is loaded. If in this same case, Auto Flag was programmed, one Abort (with INTRQ) would be generated, and thereafter continuous Flags (with no INTRQs) will be sent.

RECEIVER OPERATION

Prior to this operation, the programmable inputs and the receive mode related register bits have to be programmed according to the user's specific data communication environment. Also, the INTRQ has to be cleared. The last bit to be set is always the ACT REC (CR17) bit.

For more detailed information how to program the WD1933, see Programming. As an example, let's assume a 26-bit information is to be received, and the I-field is made up by 8-bit characters. The CR3 register is only for transmit mode, and may be ignored here. CR20 and CR 12–16 bits are also for transmit mode only, and therefore may also be ignored. CR21 and CR22 are to be logical 0s (no Self-Test and no SDLC Loop Mode). CR24, 23 are to be logical 0's (8-bit character I-field). If only one A-field and one C-field character is expected, and this WD1933 has a specific address, CR25 should be a logical 0, CR26 should be a 1, and CR27 should be a 0. The address to which the A-field should compare should be loaded into the AR register.

The status of the modem is monitored by the SR register, and it may be useful to read it at this time. CR1 is loaded as the last register. CR10 (Misc In) bit is optional to the user. CR11 (DTR) is to be set if modem is used. CR17 (ACT REC) is now set, starting the input of frame characters into the Receiver Register (RR). When a Flag is detected, the next 8-bit character (address-character), when received, is compared to the character in the AR register. If these match, or if the received character is a Global address, this frame is valid, and the DRQI gets set. If the Address Comparator (CR26) bit is not set, all frames would be considered valid and generate DRQIs. When the RHR register is read, DRQI will be reset. All characters in a valid frame which are input into the RR register will set DRQI, and every time RHR is read by the CPU, DRQI will be reset.

During reception, the receiver also performs a CRC calculation on the incoming data. When the end Flag is received, INTRQ will get set, indicating Received End of Message. If the reception is completed with no error, IR7 (REOM w/no Error) bit will be set. When 8-bit characters are received SR 0-2 bits indicate the number of residual bits, in this case two. If IR6 (REOM w/Error) was set, SR 0-2 bits indicate the type

of errors (see Received Error Indication).

When all characters including the A-field and the FCS-field are read, and when the RE interrupt is recognized, it is up to the user to disassemble these mentioned characters from the received data. If non-8-bit characters are received, the amount of residual bits have to be calculated by the CPU after masking out the part of the ending Flag showing up in the last read character.

After end of frame, the receiver begins searching for a new frame.

For more information, see Reception Timing diagram.

RECEIVER ERROR INDICATION

When a frame is received, and REOM w/Error (IR6) is set, the type of error is indicated by the SR bits 0-2.

CRC Error (SR0) If the CRC calculation performed on the incoming data does not equal to F0B8 (HEX), this bit will be set.

Overrun Error (SR1) After DRQI is set, if the RHR is not read within one character minus one bit time, this bit will be set.

Aborted or Invalid Frame Error (SR2) If the frame is aborted, or it consists of less than 32 bits between flags, this bit will be set.

NOTES

1. TC—command—If two or more contiguous ABORTS of FLAGS are executed, the ACT TRAN (CR16) bit has to be reset before DATA-command can be executed.
2. Master Reset (\overline{MR})—Needs no clock during activation of MR. However, 2.5 clock pulses are required to reset the WD1933 after the falling edge of MR.
3. IR-register—Immediately when IR register is read, bit 0 will reset. Bits 3–7 are reset one bit time later.
4. SR-register—Bits 0–2 are reset one bit time after SR register being read.
5. SDLC Loop mode—Go-ahead pattern may be sent by either sending IDLE or ABORT.

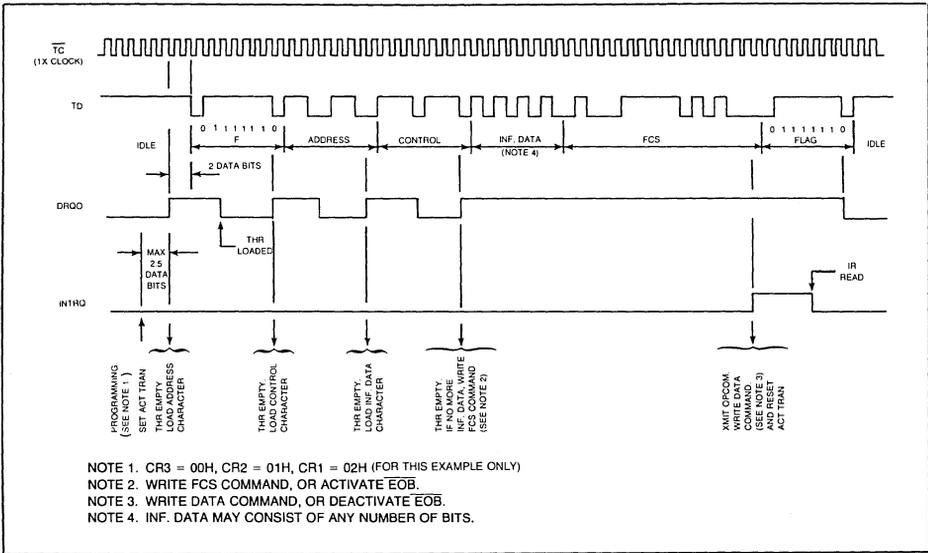


Figure 8 WD1933 TRANSMISSION TIMING DIAGRAM

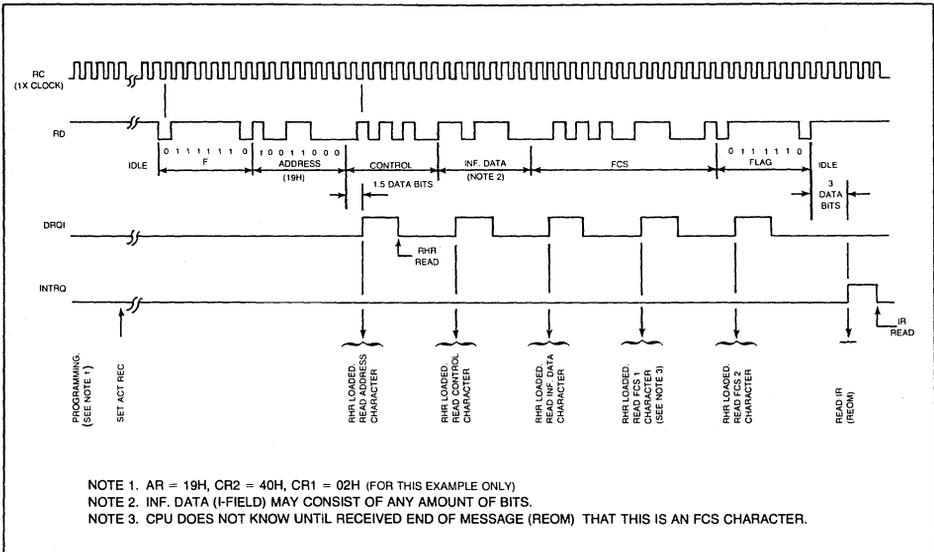


Figure 9 WD1933 RECEPTION TIMING DIAGRAM

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Storage Temperature	-55°C to +125°C (plastic package)
Storage Temperature	-65°C to +150°C (ceramic package)
Voltage on any pin with respect to GND (V _{SS})	-0.3 to +7.0V
Power Dissipation	1W

DC Characteristics

T_A = 0°C to +70°
V_{SS} = 0V, V_{CC} = +5 ± 0.25V

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I _{LI}	Input Leakage			10	uA	V _{IN} = V _{CC}
I _{LO}	Output Leakage			10	uA	V _{out} = V _{CC} or V _{SS}
V _{IH}	Input High Voltage	2.4			V	
V _{IL}	Input Low Voltage			0.8	V	All Inputs
V _{OH}	Output High Voltage	2.4			V	I _O = -100uA
V _{OL}	Output Low Voltage			0.4	V	I _O = 1.6mA
I _{CC}	Supply Current		40		ma	

Table 3 WD1933 DC CHARACTERISTICS

AC Characteristics

T_A = 0°C to +70°C
V_{SS} = 0V, V_{CC} = +5 ± 0.25V

Symbol	Parameter	Min	Typ	Max	Units	Conditions
						C _L = 50 pF
T _{AS}	READ AND WRITE Address Set-up	0			ns	
T _{AH}	Address Hold	0			ns	
T _{CSS}	Chip Select Set-up	0			ns	
T _{CSH}	Chip Select Hold	0			ns	
						C _L = 50pF
T _{RED}	READ Data Delay from \overline{RE}			240	ns	
T _{DV}	Data Valid from \overline{RE}			140	ns	
T _{DRQIR}	DRQI Reset Delay			280	ns	
T _{INTRQR}	INTRQ Reset Delay			280	ns	
T _{RE}	\overline{RE} pulse width	120			ns	
						C _L = 50pF
T _{DS}	WRITE Data Set-up	120			ns	
T _{DH}	Data Hold	0			ns	C _L = 50pF
T _{DRQOR}	DRQO Reset delay			330	ns	
T _{WE}	\overline{WE} pulse width	120			ns	
F _C	Input Clock	32X	DC	2.0	MHz	WD1933-00/10
		1X	DC	0.5	MHz	WD1933-00/10
		32X	DC	2.0	MHz	WD1933-01/11
		1X	DC	1.0	MHz	WD1933-01/11
		32X	DC	2.0	MHz	WD1933-02/12
		1X	DC	1.5	MHz	WD1933-02/12
		32X	DC	2.5	MHz	WD1933-03
		1X	DC	2.0	MHz	WD1933-03

Table 4 WD1933 AC CHARACTERISTICS

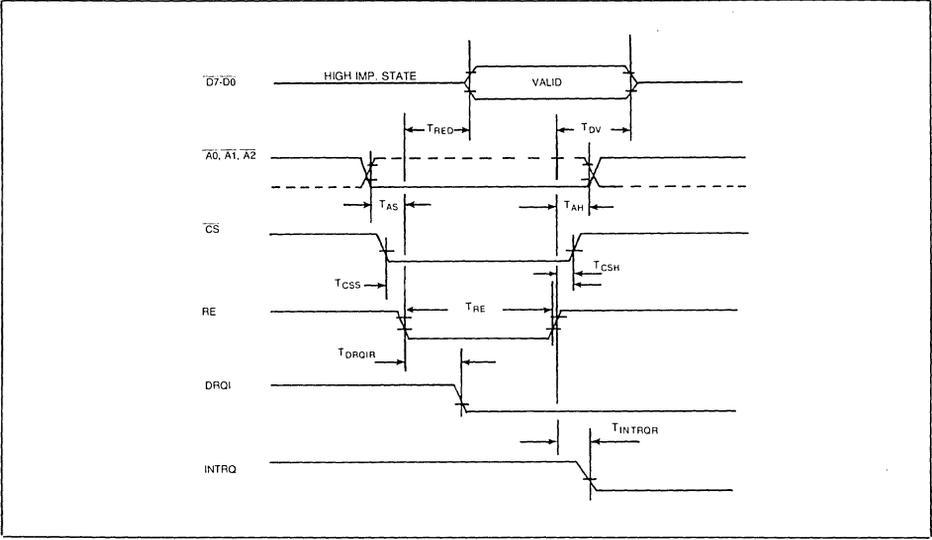


Figure 10 WD1933 READ TIMING DIAGRAM

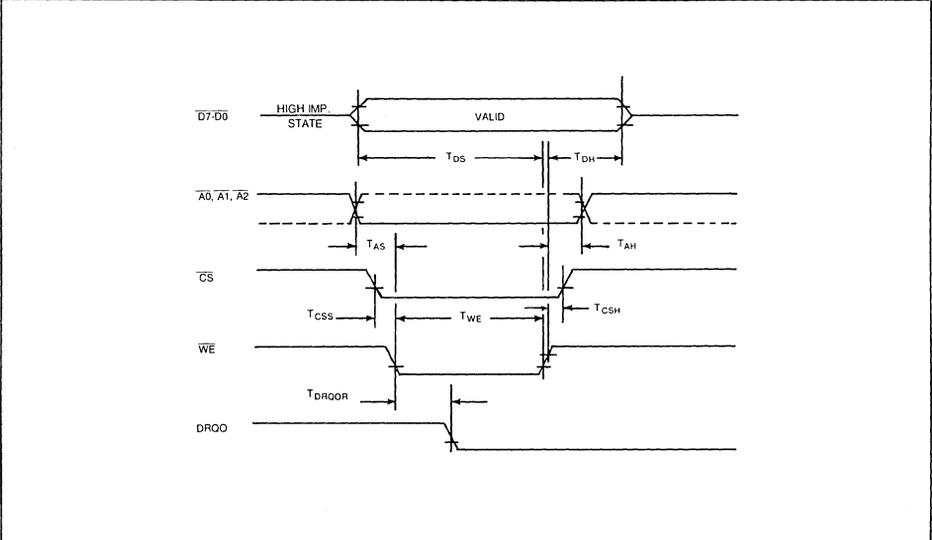
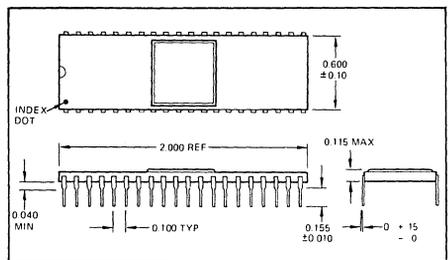


Figure 11 WD1933 WRITE TIMING DIAGRAM

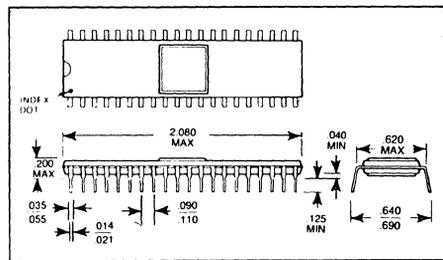
ORDERING INFORMATION

Part No.	Package Type	Loop Mode	Maximum Data Rate	Temp. Range
WD1933A-00	Ceramic	no	500KBPS	0°C to +70°C
WD1933A-10	Ceramic	yes	500KBPS	0°C to +70°C
WD1933B-00	Plastic	no	500KBPS	0°C to +70°C
WD1933B-10	Plastic	yes	500KBPS	0°C to +70°C
WD1933A-01	Ceramic	no	1.0MBPS	0°C to +70°C
WD1933A-11	Ceramic	yes	1.0MBPS	0°C to +70°C
WD1933B-01	Plastic	no	1.0MBPS	0°C to +70°C
WD1933B-11	Plastic	yes	1.0MBPS	0°C to +70°C
WD1933A-02	Ceramic	no	1.5MBPS	0°C to +70°C
WD1933A-12	Ceramic	yes	1.5MBPS	0°C to +70°C
WD1933B-02	Plastic	no	1.5MBPS	0°C to +70°C
WD1933B-12	Plastic	yes	1.5MBPS	0°C to +70°C
WD1933A-03	Ceramic	no	2.0MBPS	0°C to +70°C
WD1933B-03	Plastic	no	2.0MBPS	0°C to +70°C

Table 5 WD1933 ORDERING INFORMATION



WD1933A CERAMIC PACKAGE



WD1933B PLASTIC PACKAGE

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WESTERN DIGITAL

C O R P O R A T I O N

BR1941 Dual Baud Rate Clock

1 Z0-10100

FEBRUARY, 1981

FEATURES

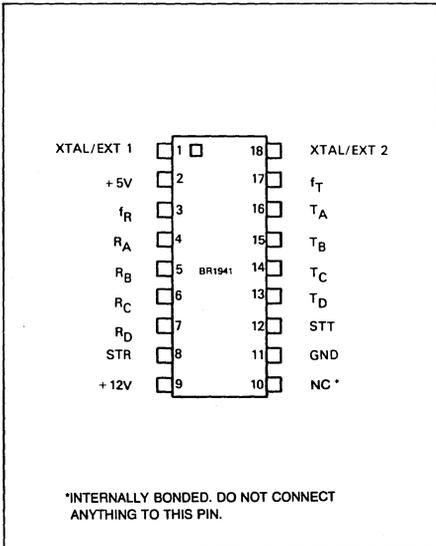
- 16 SELECTABLE BAUD RATE CLOCK FREQUENCIES
- DUAL SELECTABLE 16 X CLOCK OUTPUTS FOR FULL DUPLEX OPERATIONS
- OPERATES WITH CRYSTAL OSCILLATOR OR EXTERNALLY GENERATED FREQUENCY INPUT
- ROM MASKABLE FOR NON-STANDARD FREQUENCY SELECTIONS
- INTERFACES EASILY WITH MICRO-COMPUTERS
- OUTPUTS A 50% DUTY CYCLE CLOCK WITH 0.01% ACCURACY
- 18 PIN CERAMIC DIP PACKAGE
- 3 DIFFERENT FREQUENCY/DIVISOR PAIRS AVAILABLE

GENERAL DESCRIPTION

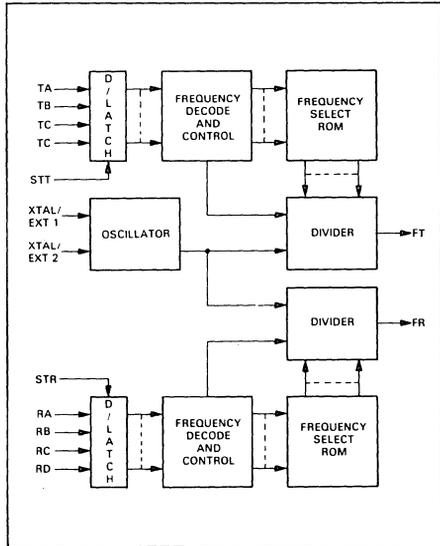
The BR1941 is a combination Baud Rate Clock Generator and Programmable Divider. It is manufactured in N-channel MOS using silicon gate technology. This device is capable of generating 16 externally selected clock rates whose frequency is determined by either a single crystal or an externally generated input clock. The BR1941 is a programmable counter capable of generating a division from 2 to $(2^{15}-1)$.

The BR1941 is available programmed with the most used frequencies in data communication. Each frequency is selectable by strobing or hard wiring each of the two sets of four Rate Select inputs. Other frequencies/division rates can be generated by reprogramming the internal ROM coding through a MOS mask change. Additionally, further clock division may be accomplished through cascading of devices. The frequency output is fed into the XTAL/EXT input on a subsequent device.

The BR1941 can be driven by an external crystal or by TTL logic.



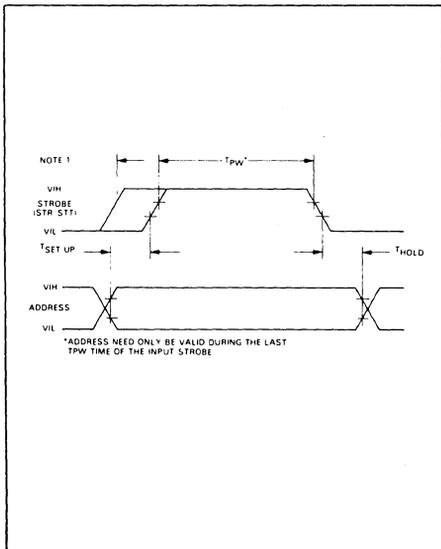
PIN CONNECTIONS



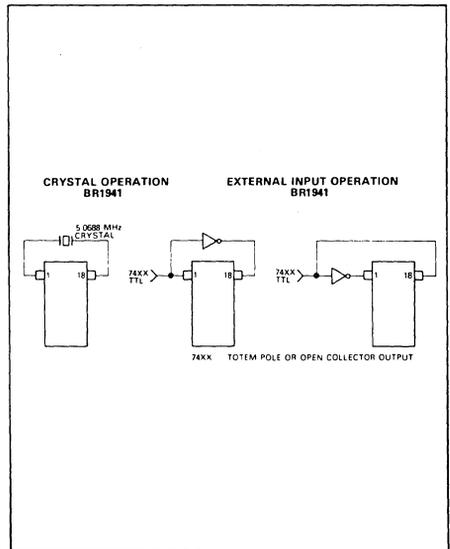
BR1941 BLOCK DIAGRAM

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	XTAL/EXT 1	Crystal or External Input 1	This input receives one pin of the crystal package or one polarity of the external input.
2	V _{CC}	Power Supply	+5 volt Supply
3	f _R	Receiver Output Frequency	This output runs at a frequency selected by the Receiver Address inputs.
4-7	R _A , R _B , R _C , R _D	Receiver Address	The logic level on these inputs as shown in Table 1, selects the receiver output frequency, f _R .
8	STR	Strobe-Receiver Address	A high-level input strobe loads the receiver address (R _A , R _B , R _C , R _D) into the receiver address register. This input may be strobed or hard wired to +5V.
9	V _{DD}	Power Supply	+12 volt Supply
10	NC	No Connection	Internally bonded. Do not connect anything to this pin.
11	GND	Ground	Ground
12	STT	Strobe-Transmitter Address	A high-level input strobe loads the transmitter address (T _A , T _B , T _C , T _D) into the transmitter address register. This input may be strobed or hard wired to +5V.
13-16	T _D , T _C , T _B , T _A	Transmitter Address	The logic level on these inputs, as shown in Table 1, selects the transmitter output frequency, f _T .
17	f _T	Transmitter Output Frequency	This output runs at a frequency selected by the Transmitter Address inputs.
18	XTAL/EXT 2	Crystal or External Input 2	This input receives the other pin of the crystal package or the other polarity of the external input.



CONTROL TIMING



CRYSTAL/CLOCK OPTIONS

ABSOLUTE MAXIMUM RATINGS

Positive Voltage on any Pin, with respect to ground	+20.0V
Negative Voltage on any Pin, with respect to ground	-0.3V
Storage Temperature	(plastic "M" package) -65°C to +125°C (ceramic "L" package) -65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+325°C

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and Functional Operation of the device at these or at any other condition above those indicated in the operational sections of this specification are not implied.

ELECTRICAL CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = +12V ± 5%, unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V _{IL}			0.8	V	excluding XTAL inputs
High-level, V _{IH}	V _{CC} -1.5		V _{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V _{OL}			0.4	V	I _{OL} = 3.2 mA I _{OH} = 100 μA
High-level, V _{OH}	V _{CC} -1.5	4.0		V	
INPUT CURRENT					
Low-level, I _{IL}			0.3	mA	V _{IN} = GND, excluding XTAL inputs
INPUT CAPACITANCE					
All inputs, C _{IN}		5	10	pf	V _{IN} = GND excluding XTAL inputs
POWER SUPPLY CURRENT					
I _{CC}		20		mA	
I _{DD}		20		mA	
AC CHARACTERISTICS					
T _A = +25°C					
CLOCK FREQUENCY		5.0688		MHz	XTAL/EXT inputs
PULSE WIDTH (T_{PW})					
Clock					50% Duty Cycle ± 10%
Receiver strobe	150		DC	ns	See Note 1
Transmitter strobe	150		DC	ns	See Note 1
INPUT SET-UP TIME (T_{SET-UP})					
Address	50			ns	See Note 1
OUTPUT HOLD TIME (T_{HOLD})					
Address	50			ns	

NOTE 1: Input set-up time can be decreased to >0 ns by increasing the minimum strobe width by 50 ns to a total of 200 ns.

All inputs except XTAL/EXT have internal pull-up resistors.

OPERATION

Standard Frequencies

Choose a Transmitter and receiver frequency from the table below. Program the corresponding address into TA-TD and RA-RD respectively using strobe pulses or by hard wiring the strobe and address inputs.

Non-Standard Frequencies

To accomplish non-standard frequencies do one of the following:

1. Choose a crystal that when divided by the BR1941 generates the desired frequency.
2. Cascade devices by using the frequency outputs as an input to the XTAL/EXT inputs of the subsequent BR1941.
3. Consult the factory for possible changes via ROM mask reprogramming.

FREQUENCY OPTIONS

TABLE 1 CRYSTAL FREQUENCY = 5.0688 MHZ

Transmit/Receive Address				Baud Rate	Theoretical Frequency 16X Clock	Actual Frequency 16X Clock	Percent Error	Duty Cycle %	Divisor
D	C	B	A						
0	0	0	0	50	0.8 KHz	0.8KHz	—	50/50	6336
0	0	0	1	75	1.2	1.2	—	50/50	4224
0	0	1	0	110	1.76	1.76	—	50/50	2880
0	0	1	1	134.5	2.152	2.1523	0.016	50/50	2355
0	1	0	0	150	2.4	2.4	—	50/50	2112
0	1	0	1	300	4.8	4.8	—	50/50	1056
0	1	1	0	600	9.6	9.6	—	50/50	528
0	1	1	1	1200	19.2	19.2	—	50/50	264
1	0	0	0	1800	28.8	28.8	—	50/50	176
1	0	0	1	2000	32.0	32.081	0.253	50/50	158
1	0	1	0	2400	38.4	38.4	—	50/50	132
1	0	1	1	3600	57.6	57.6	—	50/50	88
1	1	0	0	4800	76.8	76.83	—	50/50	66
1	1	0	1	7200	115.2	115.2	—	50/50	44
1	1	1	0	9600	153.6	153.6	—	48/52	33
1	1	1	1	19,200	307.2	316.8	3.125	50/50	16

BR1941-00

TABLE 2. CRYSTAL FREQUENCY = 4.9152 MHZ

Transmit/Receive Address				Baud Rate	Theoretical Frequency 16X Clock	Actual Frequency 16X Clock	Percent Error	Duty Cycle %	Divisor
D	C	B	A						
0	0	0	0	50	0.8 KHz	0.8 KHz	—	50/50	6144
0	0	0	1	75	1.2	1.2	—	50/50	4096
0	0	1	0	110	1.76	1.7598	-0.01	*	2793
0	0	1	1	134.5	2.152	2.152	—	50/50	2284
0	1	0	0	150	2.4	2.4	—	50/50	2048
0	1	0	1	300	4.8	4.8	—	50/50	1024
0	1	1	0	600	9.6	9.6	—	50/50	512
0	1	1	1	1200	19.2	19.2	—	50/50	256
1	0	0	0	1800	28.8	28.7438	-0.19	*	171
1	0	0	1	2000	32.0	31.9168	-0.26	50/50	154
1	0	1	0	2400	38.4	38.4	—	50/50	128
1	0	1	1	3600	57.6	57.8258	0.39	*	85
1	1	0	0	4800	76.8	76.8	—	50/50	64
1	1	0	1	7200	115.2	114.306	-0.77	*	43
1	1	1	0	9600	153.6	153.6	—	50/50	32
1	1	1	1	19,200	307.2	307.2	—	50/50	16

*When the duty cycle is not exactly 50% it is 50% ± 10%

BR1941-05

TABLE 3 CRYSTAL FREQUENCY = 5.0688 MHZ

Transmit/Receive Address				Baud Rate	Theoretical Frequency 32X Clock	Actual Frequency 32X Clock	Percent Error	Duty Cycle %	Divisor
D	C	B	A						
0	0	0	0	50	1.6 KHz	1.6 KHz	—	50/50	3168
0	0	0	1	75	2.4	2.4	—	50/50	2112
0	0	1	0	110	3.52	3.52	—	50/50	1440
0	0	1	1	134.5	4.304	4.303	.026	50/50	1178
0	1	0	0	150	4.8	4.8	—	50/50	1056
0	1	0	1	200	6.4	6.4	—	50/50	792
0	1	1	0	300	9.6	9.6	—	50/50	528
0	1	1	1	600	19.2	19.2	—	50/50	264
1	0	0	0	1200	38.4	38.4	—	50/50	132
1	0	0	1	1800	57.6	57.6	—	50/50	88
1	0	1	0	2400	76.8	76.8	—	50/50	66
1	0	1	1	3600	115.2	115.2	—	50/50	44
1	1	0	0	4800	153.6	153.6	—	*	33
1	1	0	1	7200	230.4	230.4	—	50/50	22
1	1	1	0	9600	307.2	298.16	2.941	*	17
1	1	1	1	19,200	614.4	633.6	3.125	50/50	8

*When the duty cycle is not exactly 50% it is 50% ± 10%

BR1941-06

APPLICATIONS INFORMATION

OPERATION WITH A CRYSTAL

The BR1941 Baud Rate Generator may be driven by either a crystal or TTL level clock. When using a crystal, the waveform that appears at pins 1 (XTAL/EXT 1) and 18 (XTAL/EXT 2) does not conform to the normal TTL limits of $V_{IL} \leq 0.8V$ and $V_{IH} \geq 2.0V$. Figure 1 illustrates a typical crystal waveform.

Since the D.C. level of the waveform causes the least positive point to typically be greater than 0.8V, the BR1941 is designed to look for an edge, as opposed to a TTL level. The XTAL/EXT logic triggers on a rising edge of typically 1V in magnitude. This allows the use of a crystal without any additional components.

OPERATION WITH TTL LEVEL CLOCK

With clock frequencies in the area of 5 MHz, significant overshoot and undershoot can appear at pins 1 and/or 18. The BR1941 may, at times, trigger on a rising edge of an overshoot or undershoot waveform, causing the device to effectively "double-trigger". This phenomenon may result as a twice expected baud rate, or as an apparent device failure. Figure 2 shows a typical waveform that exhibits the "ringing" problem.

The design methods required to minimize ringing include the following:

1. Minimize the P.C. trace length. At 5 MHz, each inch of trace can add significantly to overshoot and undershoot.

2. Match impedances at both ends of the trace. For example, a series resistor near the BR1941 may be helpful.
3. A uniform impedance is important. This can be accomplished through the use of:
 - a. parallel ground lines
 - b. evenly spaced ground lines crossing the trace on the opposite side of PC board
 - c. an inner plane of ground, e.g., as in a four layered PC board.

In the event that ringing exists on an already finished board, several techniques can be used to reduce it. These are:

1. Add a series resistor to match impedance as shown in Figure 3.
2. Add pull-up/pull-down resistor to match impedance, as shown in Figure 4.
3. Add a high speed diode to clamp undershoot, as shown in Figure 5.

The method that is easiest to implement in many systems is method 1, the series resistor. The series resistor will cause the D.C. level to shift up, but that does not cause a problem since the BR1941 is triggered by an edge, as opposed to a TTL level.

The BR1941 Baud Rate Generator can save both board space and cost in a communications system. By choosing either a crystal or a TTL level clock, the user can minimize the logic required to provide baud rate clocks in a given design.

CRYSTAL SPECIFICATIONS

User must specify termination (pin, wire, other)
Frequency—5.0688 MHz, or 4.9152 MHz
Temperature range 0°C to 70°C
Series resistance 50Ω
Series resonant
Overall tolerance ± .01%

Bulova Frequency Control Products

61-20 Woodside Avenue
Woodside, New York 11377
(212) 335-6000

CAL Crystal

1142 N. Gilbert Street
Anaheim, California 92801
(Available in HC-18 small can)
(714) 991-1580

CTS Knights Inc.

101 East Church Street
Sandwich, Illinois 60548
(815) 786-8411

CRYSTAL MANUFACTURERS (Partial List)

Northern Engineering Laboratories
357 Beloit Street
Burlington, Wisconsin 53105
(414) 763-3591

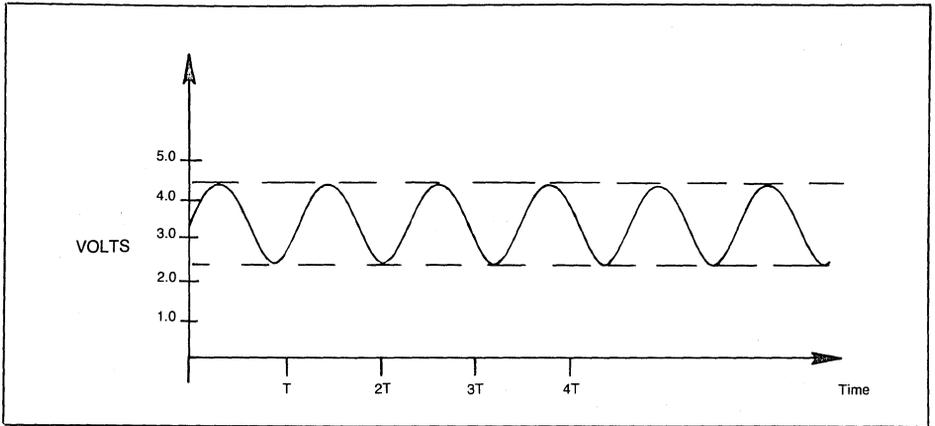


Figure 1 TYPICAL CRYSTAL WAVEFORM

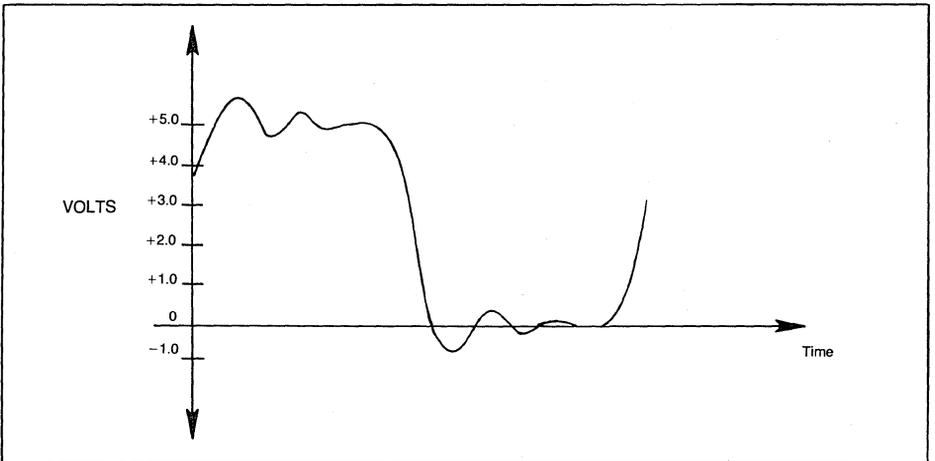


Figure 2 TYPICAL "RINGING" WAVEFORM

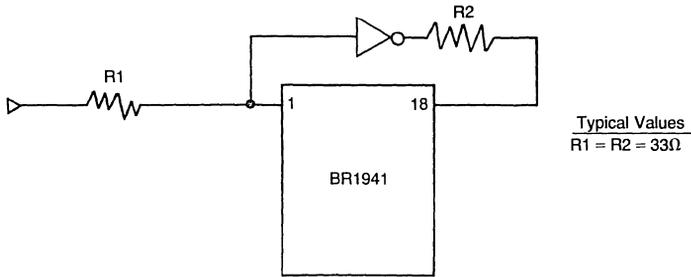


Figure 3 SERIES RESISTOR TO MATCH IMPEDANCE

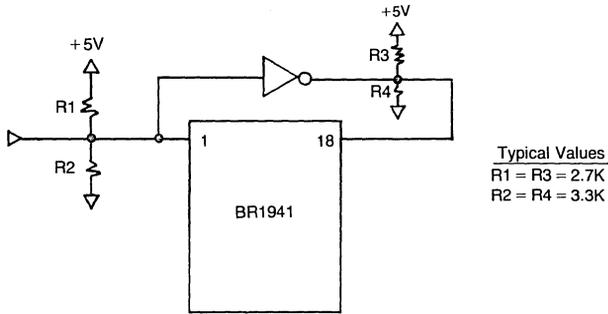


Figure 4 PULL-UP/PULL-DOWN RESISTORS TO MATCH IMPEDANCE

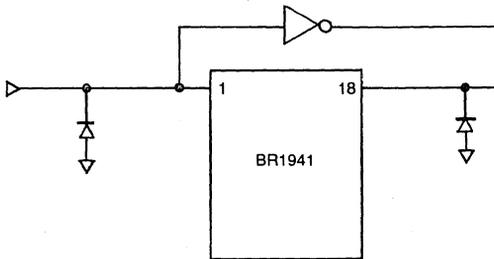
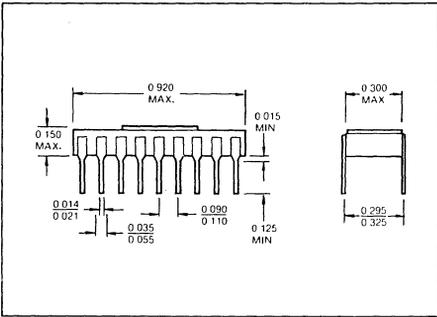
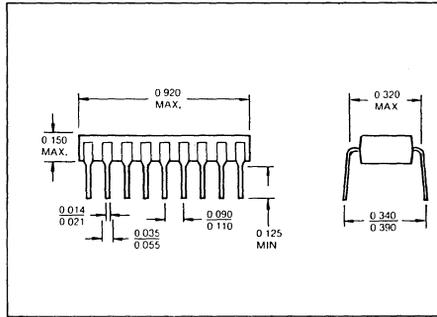


Figure 5 HIGH-SPEED DIODE TO CLAMP UNDERSHOOT



BR1941L CERAMIC PACKAGE



BR1941M PLASTIC PACKAGE

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NEWPORT BEACH, CA 92663 (714) 557-3550, TWX 910-595-1139

WD1983 (BOART)

BUS ORIENTED ASYNCHRONOUS RECEIVER/TRANSMITTER

FEBRUARY, 1981

FEATURES

ASYNCHRONOUS MODE

- FULL DUPLEX OPERATION
- SELECTABLE 5,6,7, & 8 BIT CHARACTERS
- LINE BREAK DETECTION AND GENERATION
- 1, 1½, or 2 STOP BIT SELECTION
- FALSE START BIT DETECTION
- OVERRUN AND FRAMING ERROR DETECTION
- DC TO 36K BITS/SEC (16X)
- DC TO 600K BITS/SEC (1X)
- 8251/8251A ASYNCHRONOUS ONLY REPLACEMENT
- REQUIRES NO ASYNCHRONOUS SYSTEM CLOCK
- 28 PIN PLASTIC OR CERAMIC
- +5 VOLT ONLY

SYSTEM COMPATIBILITY

- DOUBLE BUFFERING OF DATA
- 8 BIT BI-DIRECTIONAL BUS FOR DATA, STATUS, AND CONTROL WORDS
- ALL INPUTS AND OUTPUTS TTL COMPATIBLE
- CHIP SELECT, RE, WE, C/D INTERFACE TO CPU
- ON-LINE DIAGNOSTIC CAPABILITY
- THREE STATE DATA BUS

BAUD RATE-DC TO 36K BITS/SEC (16X) SELECTABLE CLOCK RATES

- 1X, 16X, 64X, BAUD RATE CLOCK INPUTS
- UP TO 47% DISTORTION ALLOWANCE WITH 64X CLOCK

APPLICATIONS

ASYNCHRONOUS COMMUNICATIONS
SERIAL/PARALLEL INTERFACE

GENERAL DESCRIPTION

The WD1983 is an N channel silicon gate MOS/LSI device that interfaces a digital asynchronous channel with a parallel channel. It is available in a ceramic or plastic standard 28 pin dual in line package.

The WD1983 is a fully programmable microprocessor I/O peripheral with two control registers and a status register. It is capable of full duplex operations.

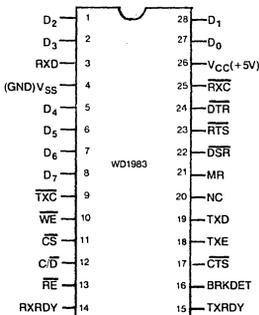


FIGURE 1 WD1983 PIN-OUT

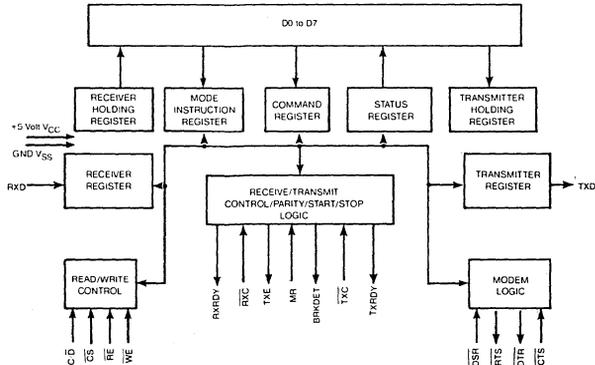


FIGURE 2 WD1983 BLOCK DIAGRAM

PIN. NO.	PIN NAME	SYMBOL	FUNCTION
4	POWER GND	VSS	Ground
26	POWER SUPPLY	VCC	+5 Volts
11	CHIP SELECT	\overline{CS}	This input, when low, enables READ or WRITE operations.
13	READ ENABLE	\overline{RE}	This input, when low, accesses the contents of the addressed register.
10	WRITE ENABLE	\overline{WE}	This input, when low, writes the data on the DATA BUS into the addressed register.
21	MASTER RESET	MR	This input, when high, initializes the device and clears the COMMAND and MODE REGISTERS.
12	CONTROL/DATA	C/\overline{D}	This input selects the CONTROL or DATA register. It is used in conjunction with a READ or WRITE enable.
19	TRANSMIT DATA	TXD	This output is the transmit serial data. When no data is being transmitted or after MASTER RESET, this output is high (a marking condition). COMMAND CONTROL word bit 3 is used to program a break condition by forcing the TXD output to a low (spacing condition).
9	TRANSMIT CLOCK	\overline{TXC}	This input is the source clock for transmission. MODE INSTRUCTION word bits MR0 & MR1, control 1X, 16X, or 64X, times the transmitted bit rate.
18	TRANSMIT EMPTY	TXE	This output is set high after MASTER RESET and is automatically reset when a character is written into the TRANSMITTER HOLDING REGISTER. It returns high at the end of a transmitted character indicating the end of transmission if the TRANSMIT HOLDING REGISTER has not been loaded.
15	TRANSMIT READY	TXRDY	This output is set high after MASTER RESET. It indicates that the transmitter is ready to accept a character and is automatically reset whenever a character is written into the TRANSMITTER HOLDING REGISTER.

170-10100
 170-10100

PIN NO.	PIN NAME	SYMBOL	FUNCTION
3	RECEIVE DATA	RXD	This input is the received serial data.
25	RECEIVE CLOCK	$\overline{\text{RXC}}$	This input is the receiver clock. MODE INSTRUCTION word bits MR0 & MR1 control whether this input is 1X, 16X or 64X times the received bit rate.
14	RECEIVER READY	RXRDY	This output is set low after MASTER RESET. When set high it indicates that the receiver has assembled a character and transferred it to the RECEIVER HOLDING REGISTER. It is automatically reset when the RECEIVER HOLDING REGISTER is read.
16	BREAK DETECT	BRKDET	This output is reset after MASTER RESET. It is set high when the receiver detects a string of zeros equal to the programmed character length including start, parity and stop bits. Upon detecting a valid one data bit it's reset. Assembly of the next character is begun after detecting a valid start bit.
17	CLEAR TO SEND	$\overline{\text{CTS}}$	This input is set low to enable the transmitter. When set high it disables transmission. If the transmitter is transmitting a character, it will terminate transmission after the TRANSMITTER REGISTER is empty.
24	DATA TERMINAL READY	$\overline{\text{DTR}}$	This is a general purpose output which is set and cleared by COMMAND word bit CR1. It is reset after MASTER RESET.
23	REQUEST TO SEND	$\overline{\text{RTS}}$	This is a general purpose output which is set and cleared by COMMAND word bit CR5. It is reset after MASTER RESET.
1, 2, 5, 6, 7, 8, 27, 28	DATA BUS	D0 THRU D7	These are input/output pins. Data on the DATA BUS is written into the selected register during a WRITE operation. During a READ operation, the DATA BUS is driven by data in the selected register. When not selected, ($\overline{\text{CS}}$ high), these pins are in a high impedance state.
22	DATA SET READY	$\overline{\text{DSR}}$	This is a general purpose input which is sensed in STATUS REGISTER bit #7.
20		NC	No internal connection, pin not used.

ORGANIZATION

The WD1983 Block Diagram is illustrated on Page 1. The WD1983 (BOART) is an eight bit bus-oriented device. Communication between the BOART and the controlling CPU occurs via the 8 bit DATA BUS. There are 2 accessible DATA REGISTERS, which buffer Transmit and Receive DATA. They are the TRANSMIT HOLDING REGISTER and the RECEIVE HOLDING REGISTER. There is a parallel-to-serial shift register (the TRANSMIT REGISTER) and a serial-to-parallel shift register (the RECEIVE REGISTER).

Operational control and monitoring of the BOART is performed by two CONTROL REGISTERS (the COMMAND INSTRUCTION REGISTER and the MODE INSTRUCTION REGISTER) and the STATUS REGISTER.

A READ/WRITE control circuit allows monitoring/programming or reading/loading in the CONTROL, STATUS or HOLDING REGISTERS by activating the appropriate control lines: Chip Select (\overline{CS}), Read Enable (\overline{RE}), Write Enable (\overline{WE}) and Control or Data Select (C/\overline{D}).

Internal control of the BOART is by means of two internal MICROCONTROLLERS: one for transmit and one for receive. The CONTROL REGISTERS, MODEM CONTROL LOGIC, READ/WRITE CONTROL LOGIC and various counters provide inputs to the MICROCONTROLLERS, which generate the necessary control signals to send and receive serial data according to the programmed asynchronous format.

READ/WRITE OPERATIONS

The WD1983 must be initialized after a MASTER RESET pulse by first writing the MODE INSTRUCTION word and then the COMMAND INSTRUCTION word. Thereafter, every control write to the device is interpreted as a COMMAND word. If it is desired to re-program the MODE REGISTER, a COMMAND REGISTER bit, INTERNAL RESET (CR6), allows the next control write data to be entered into the MODE REGISTER.

The WD1983 registers are accessed according to the following table:

\overline{CS}	C/\overline{D}	\overline{RE}	\overline{WE}	REGISTERS SELECTED
L	L	L	H	Read RECEIVE HOLDING REGISTER
L	L	H	L	Write TRANSMIT HOLDING REGISTER
L	H	L	H	Read STATUS REGISTER
L	H	H	L	Write CONTROL REGISTER
H	X	X	X	DATA BUS tri-stated

Note: "L" means V_{IL} at pins
 "H" means V_{IH} at pins
 "X" means don't care

OPERATING DESCRIPTION

The WD1983 (BOART) is primarily designed to operate in an 8 bit microprocessor environment, although other control logic schemes are easily implemented. The DATA BUS and the Interface Control Signals (\overline{CS} , C/\overline{D} , \overline{RE} and \overline{WE}) should be connected to the microprocessor's data bus and system control bus. The appropriate \overline{TXC} and \overline{RXC} clock frequencies should be selected for the particular application using a programmable baud rate generator such as the BR1941.

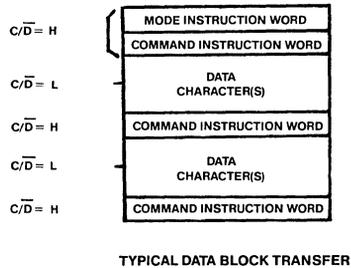
For typical data communication applications, the RXD and TXD input/outputs can be connected to RS-232C interface circuits or a modem.

The TXRDY, RXRDY, TXE and BRKDET Flags may be connected to the microprocessor system as interrupt inputs or the STATUS REGISTER can be periodically read in a polled environment to support BOART operations.

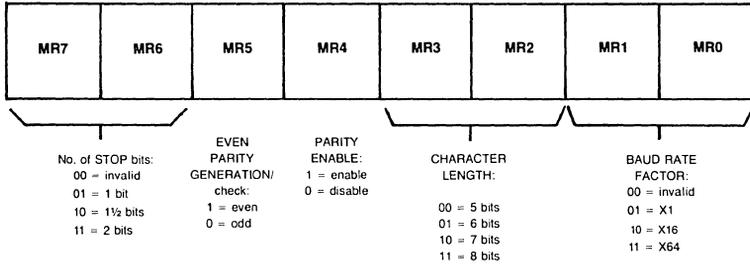
MODEM CONTROL SIGNALS can be configured several ways as the \overline{DTR} , \overline{RTS} and \overline{DSR} signals are controlled and sensed by the CPU through the COMMAND and STATUS REGISTERS. The \overline{CTS} input is used to synchronize the transmitter to external events.

The SBRK bit of the COMMAND REGISTER (CR3) is used to send a Break Character. (A break character is defined as a start bit, and all zero data, parity and stop bits). When the CR3 bit is set to a "1", it causes the transmitter output, TXD, to be forced low after the last word is transmitted.

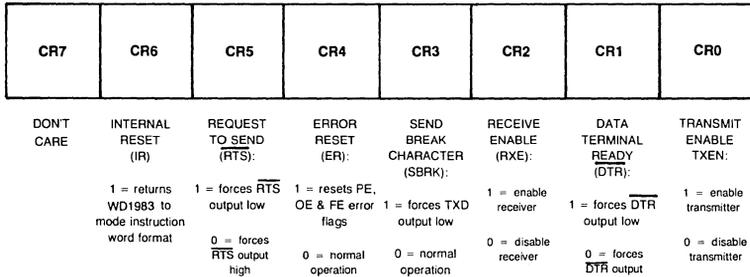
The receiver is equipped with logic to look for a break character. When a break character is received, the BREAK DETECT (BRKDET) FLAG and STATUS bit are set to logic "1". When the receiver input line goes high again for the least "one data bit time," the receiver resets the BREAK DETECT FLAG and resumes its search for a start bit.



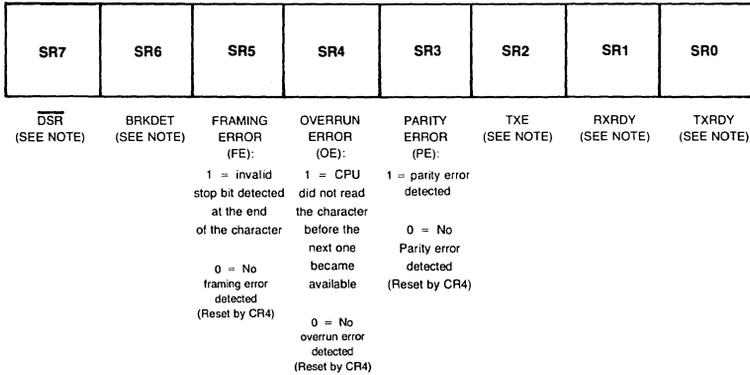
MODE INSTRUCTION CONTROL WORD FORMAT



COMMAND INSTRUCTION CONTROL WORD FORMAT



STATUS WORD FORMAT



FE, OE & PE FLAGS DO NOT INHIBIT OPERATION. THESE FLAGS ARE STATUS ONLY.

NOTE: SR0, SR1, SR2, SR6, and SR7 HAVE IDENTICAL MEANINGS AS THE EXTERNAL OUTPUT PINS.

ABSOLUTE MAXIMUM RATINGS

V_{DD} with Respect to V_{SS} (Ground) + 15 to -0.3V
 Max. Voltage to any Input with Respect to V_{SS} + 20 to -0.3V
 Power Dissipation 1000 MW

Storage Temp.

Ceramic -65°C to +150°C ('E' Package)
 Plastic -55°C to +125°C ('F' Package)

OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = + 5.0V ± .25V, V_{SS} = 0V

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
I _{LI}	Input Leakage			10	μA	V _{IN} = V _{CC}
I _{DL}	Data Bus Leakage			50	μA	Data Bus is in high impedance state
I _{CC_AVE}	V _{CC} Supply Current		45	80	mA	5.25 VDC/f _{CLK} = 600 kHz No Loads.
V _{IH}	Input High Voltage	2.4		0.8	V	
V _{IL}	Input Low Voltage (All Inputs)	-0.3			V	
V _{OH}	Output High Voltage	2.4			V	I _O = - 100μA (source)
V _{OL}	Output Low Voltage			0.45	V	I _O = 1.6 mA (sink)

TABLE 1 WD1983 DC CHARACTERISTICS

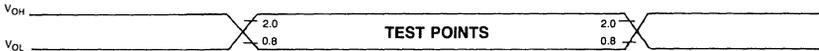


FIGURE 3 INPUT WAVEFORMS FOR AC TESTS

NOTE: ALL WAVEFORMS ARE MEASURED AT 2.0V IF RISING EDGE, AND 0.8V IF FALLING EDGE.

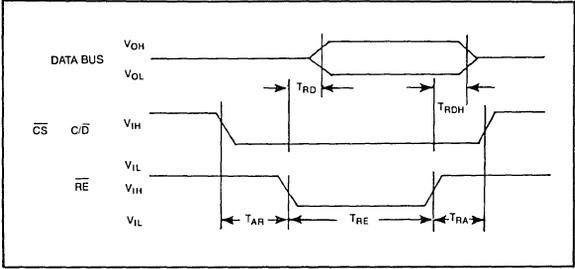


FIGURE 4 READ TIMING

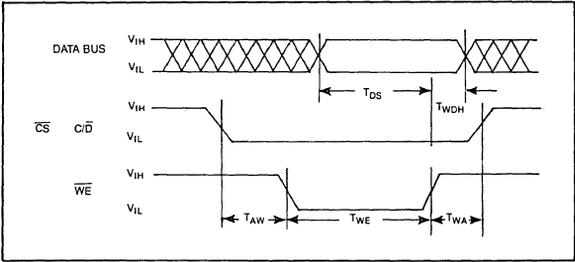


FIGURE 5 WRITE TIMING

NOTE:

8251A COMPATIBILITY

The WD1983 (BOART) is an asynchronous only device, which is compatible with the 8251A. However, in test evaluation and application, the following differences should be noted:

- (1) The WD1983 utilizes the transmit and receive baud clocks in their respective internal logic sections instead of the system clock normally applied to Pin 20 on the 8251A. This Pin on the WD1983 is not used.
- (2) As a result of the above condition, timings referenced to the system clock period in the 8251A specification are now specified in absolute time units or with respect to the transmit or receive baud clock.

AC Electrical Characteristics					
$T_A = 0^\circ\text{C to } +70^\circ\text{C}; V_{CC} = 5.0\text{ V} \pm 5\%; \text{GND} = 0\text{ V}$					
SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
BUS PARAMETERS					
READ CYCLE					
t_{AR}	Address Stable Before \overline{RE} ($\overline{CS}, C/\overline{D}$)	50		ns	
t_{RA}	Address Hold Time for \overline{RE} ($\overline{CS}, C/\overline{D}$)	5		ns	
t_{RE}	\overline{RE} Pulse Width	350		ns	
t_{RD}	Data Delay from \overline{RE}		200	ns	$C_L = 50\text{pF}$
t_{RDH}	\overline{RE} to Data Floating		200	ns	$C_L = 50\text{pF}$
		25		ns	$C_L = 15\text{pF}$
WRITE CYCLE					
t_{AW}	Address Stable Before \overline{WE}	20		ns	
t_{WA}	Address Hold Time for \overline{WE}	20		ns	
t_{WE}	\overline{WE} Pulse Width	350		ns	
t_{DS}	Data Set-Up Time for \overline{WE}	200		ns	
t_{WDH}	Data Hold Time for \overline{WE}	40		ns	
OTHER TIMINGS					
t_{DTX}	TXD Delay from Falling Edge of TXC		200	ns	$C_L = 100\text{pF}$
t_{SRX}	RX Data Set-Up Time to Sampling Pulse	200		ns	$C_L = 100\text{pF}$
t_{HRX}	RX Data Hold Time to Sampling Pulse	100		ns	$C_L = 100\text{pF}$
f_{TX}	Transmitter Input Clock Frequency				
	1X Baud Rate	DC	500	kHz	
	16X and 64X Baud Rate	DC	600	kHz	
t_{TPW}	Transmitter Input Clock Pulse Width				
	1X Baud Rate	1.0		μs	
	16X and 64X Baud Rate	500		ns	

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
t _{TPD}	Transmitter Input Clock Pulse Delay	1.0		μs	C _L = 50pF (16X)
	1X Baud Rate	800		ns	
f _{RX}	Receiver Input Clock Frequency	DC	500	kHz	
	1X Baud Rate	DC	600	kHz	
t _{RPW}	Receiver Input Clock Pulse Width	1.0		μs	
	1X Baud Rate	500		ns	
t _{RPD}	Receiver Input Clock Pulse Delay	1.0		μs	
	1X Baud Rate	800		ns	
t _{TX}	TXRDY Delay from Center of Data Bit		8	t _{RXC}	
t _{RX}	RXRDY Delay from Center of Data Bit		1/2	t _{RXC}	
t _{IS}	Internal BRKDET Delay from Center of Data Bit		1	t _{RXC}	
t _{TRD}	TXRDY Delay from Falling Edge of \overline{WE}		1	t _{TXC}	
t _{TOD}	TXD Output from Falling Edge of \overline{WE}		2	t _{TXC}	
t _{WC}	Control Delay from Rising Edge of \overline{WE} (DTR, RTS)		400	ns	
t _{CR}	Control to \overline{RE} Set-Up Time (\overline{DSR} , \overline{CTS})		500	ns	

TABLE 2 WD1983 AC CHARACTERISTICS

At $f_{TX}(\max)$, the duty cycle should be 50%. At less than $f_{TX}(\max)$, the minimum pulse width for the high or low half is

$$\frac{1}{2 \cdot f_{TX}(\max)}$$

Hence, at frequencies less than $f_{TX}(\max)$, the required duty cycle will be less stringent than 50%.

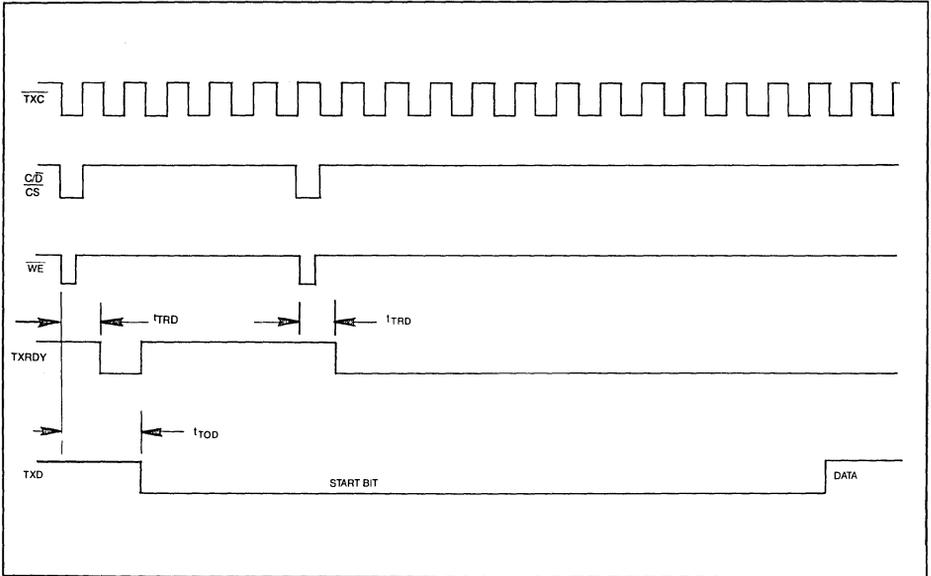


FIGURE 6

TRANSMITTER OUTPUT TIMINGS WITH RESPECT TO TRANSMIT CLOCK

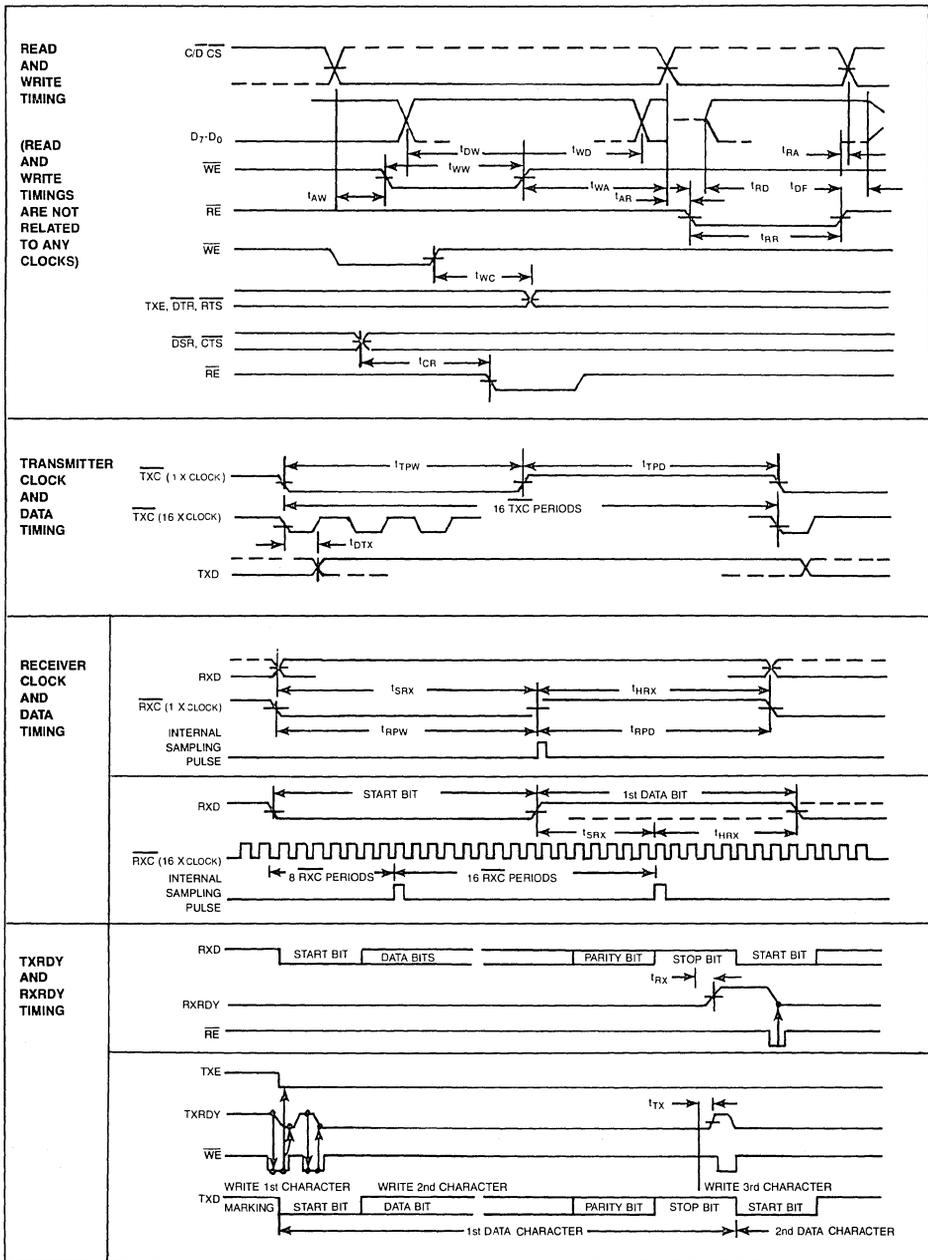
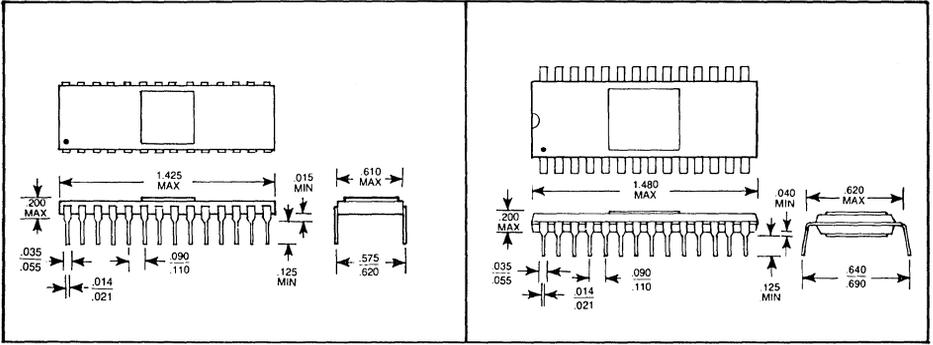


FIGURE 7 SYSTEM TIMING DIAGRAMS



WD1983 E CERAMIC PACKAGE

WD1983 F PLASTIC PACKAGE

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WD8250 Asynchronous Communications Element

FEATURES

- Designed to be Easily Interfaced to Most Popular Microprocessors (Z-80, 8080A, 6800, etc.)
- Adds or Deletes Standard Asynchronous Communication Bits (Start, Stop, and Parity) to or from Serial Data Stream
- Full Double Buffering Eliminates Need for Precise Synchronization
- Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts
- Programmable Baud Rate Generator Allows Division of Any Input Clock by 1 to $(2^{16} - 1)$ and Generates the Internal 16x Clock
- Independent Receiver Clock Input
- Fully Programmable Serial-Interface Characteristics
 - 5-, 6-, 7-, or 8-Bit Characters
 - Even, Odd, or No-Parity Bit Generation and Detection
 - 1-, 1½-, or 2-Stop Bit Generation
 - Baud Rate Generation (DC to 56K Baud)
- False Start Bit Detector
- Complete Status Reporting Capabilities
- THREE-STATE TTL Drive Capabilities for Bi-directional Data Bus and Control Bus
- Line Break Generation and Detection

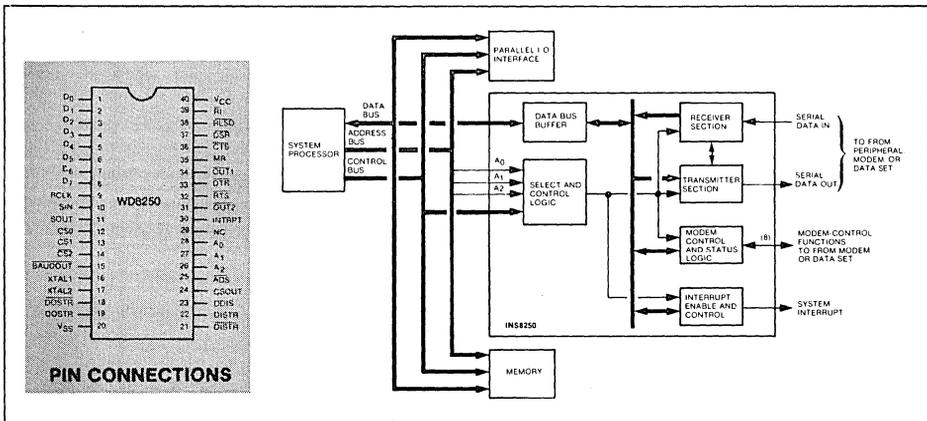
- Internal Diagnostic Capabilities
 - Loopback Controls for Communications Link Fault Isolation
 - Break, Parity, Overrun, Framing Error Simulation
- Full Prioritized Interrupt System Controls
- Single +5-Volt Power Supply

GENERAL DESCRIPTION

The WD8250 is a programmable Asynchronous Communications (ACE) chip contained in a standard 40-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate technology, functions as a serial data input/output interface in a microcomputer system. The functional configuration of the WD8250 is programmed by the system software via a THREE-STATE 8-bit bidirectional data bus.

The WD8250 performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the WD8250 at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the WD8250, as well as any error conditions (parity, overrun, framing, or break interrupt).

AUGUST, 1980



WD8250 GENERAL SYSTEM CONFIGURATION

In addition to providing control of asynchronous data communications, the WD8250 includes a programmable Baud Generator that is capable of dividing the timing reference clock input by divisors of 1 to $(2^{16} - 1)$, and producing a 16x clock for driving the internal transmitter logic. Provisions are also included to use this 16x clock to drive the receiver logic. Also included in the WD8250 is a complete MODEM-control capability, and a processor-interrupt system that may be software tailored to the user's requirements to minimize the computing time required to handle the communications link.

WD8250 FUNCTIONAL PIN DESCRIPTION

The following describes the function of all WD8250 input/output pins. Some of these descriptions reference internal circuits.

NOTE

In the following descriptions, a low represents a logic 0 (0 volt nominal) and a high represents a logic 1 (+2.4 volts nominal).

Input Signals

Chip Select (CS0, CS1, $\overline{CS2}$), Pins 12-14: When CS0 and CS1 are high and $\overline{CS2}$ is low, the chip is

selected. Chip selection is complete when the decoded chip select signal is latched with an active (low) Address Strobe (ADS) input. This enables communication between the WD8250 and the CPU.

Data Input Strobe (DISTR, \overline{DISTR}), Pins 22 and 21: When DISTR is high or \overline{DISTR} is low while the chip is selected, allows the CPU to read status information or data from a selected register of the WD8250.

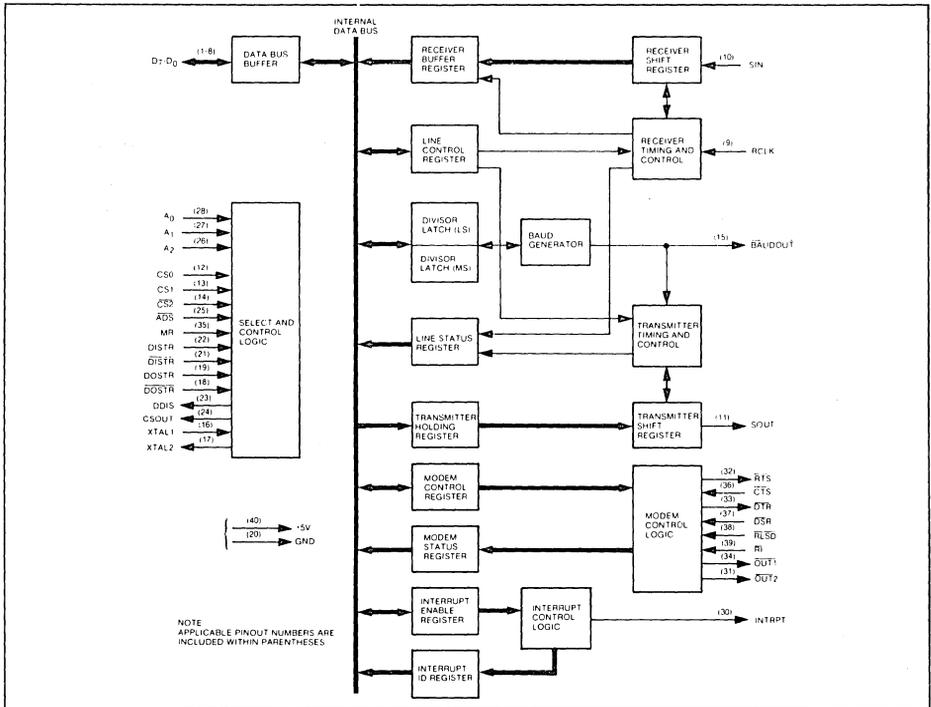
NOTE

Only an active DISTR or \overline{DISTR} input is required to transfer data from the WD8250 during a read operation. Therefore, tie either the DISTR input permanently low or the \overline{DISTR} input permanently high, if not used.

Data Output Strobe (DOSTR, \overline{DOSTR}), Pins 19 and 18: When DOSTR is high or \overline{DOSTR} is low while the chip is selected, allows the CPU to write data or control words into a selected register of the WD8250.

NOTE

Only an active DOSTR or \overline{DOSTR} input is required to transfer data to the WD8250 during a write operation. Therefore, tie either the DOSTR input permanently low or the \overline{DOSTR} input permanently high, if not used.



WD8250 BLOCK DIAGRAM

Address Strobe (ADS), Pin 25: When low, provides latching for the Register Select (A0, A1, A2) and Chip Select (CS0 CS1, CS2) signals.

NOTE

An active \overline{ADS} input is required when the Register Select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, tie the ADS input permanently low.

Register Select (A0, A1, A2), Pins 26-28: These three inputs are used during a read or write operation to select a WD8250 register to read from or write into as indicated in the table below. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain WD8250 registers. The DLAB is reset low when the Master Reset (MR) input is active (low); the DLAB must be set high by the system software to access the Baud Generator Divisor Latches.

DLAB	A2	A1	A0	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	None
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

Master Reset (MR), Pin 35: When high, clears all the registers (except the Receiver Buffer, Transmitter Holding, and Divisor Latches), and the control logic of the WD8250. Also, the state of various output signals (SOUT, INTRPT, OUT1, OUT2, RTS, DTR) are affected by an active MR input. (Refer to table 1.)

Receiver Clock (RCLK), Pin 9: This input is the 16x baud rate clock for the receiver section of the chip.

Serial Input (SIN), Pin 10: Serial data input from the communications link (peripheral device, MODEM, or data set).

Clear to Send (CTS), Pin 36: The \overline{CTS} signal is a MODEM control function input whose condition can be tested by the CPU by reading bit 4 (CTS) of the MODEM Status Register. Bit 0 (DCTS) of the MODEM Status Register indicates whether the \overline{CTS} input has changed state since the previous reading of the MODEM Status Register.

NOTE

Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if enabled.

Data Set Ready (DSR), Pin 37: When low, indicates that the MODEM or data set is ready to establish the communications link and transfer data with the

WD8250. The \overline{DSR} signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 5 (DSR) of the MODEM Status Register. Bit 1 (DDSR) of the MODEM Status Register indicates whether the \overline{DSR} input has changed state since the previous reading of the MODEM Status Register.

NOTE

Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if enabled.

Received Line Signal Detect (RLSD), Pin 38: When low, indicates that the data carrier has been detected by the MODEM or data set. The RLSD signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 7 (RLSD) of the MODEM Status Register. Bit 3 (DRLSD) of the MODEM Status Register indicates whether the RLSD input has changed state since the previous reading of the MODEM Status Register.

NOTE

Whenever the RLSD bit of the MODEM Status Register changes state, an interrupt is generated if enabled.

Ring Indicator (RI), Pin 39: When low, indicates that a telephone ringing signal has been received by the MODEM or data set. The RI signal is a MODEM-control function input whose condition can be tested CPU by reading bit 6 (RI) of the MODEM Status Register. Bit 2 (TERI) of the MODEM Status Register indicates whether the RI input has changed from a low to a high state since the previous reading of the MODEM Status Register.

NOTE

Whenever the RI bit of the MODEM Status Register changes from a high to a low state, an interrupt is generated if enabled.

VCC, Pin 40: +5-volt supply.

VSS, Pin 20: Ground (0-volt) reference.

Output Signals

Data Terminal Ready (DTR), Pin 33: When low, informs the MODEM or data set that the WD8250 is ready to communicate. The DTR output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. The DTR signal is set high upon a Master Reset operation.

Request to Send (RTS), Pin 32: When low, informs the MODEM or data set that the WD8250 is ready to transmit data. The RTS output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register. The RTS signal is set high upon a Master Reset operation.

Output 1 (OUT 1), Pin 34: User-designated output that can be set to an active low by programming bit 2 (OUT 1) of the MODEM Control Register to a high level. The OUT 1 signal is set high upon a Master Reset operation.

Output 2 (OUT 2), Pin 31: User-designated output that can be set to an active low by programming bit 3 (OUT 2) of the MODEM Control Register to a high level. The OUT 2 signal is set high upon a Master Reset operation.

Chip Select Out (CSOUT), Pin 24: When high, indicates that the chip has been selected by active CS0, CS1, and CS2 inputs. No data transfer can be initiated until the CSOUT signal is a logic 1.

Driver Disable (DDIS), Pin 23: Goes low whenever the CPU is reading data from the WD8250. A high-level DDIS output can be used to disable an external transceiver (if used between the CPU and WD8250 on the D7-D0 Data Bus) at all times, except when the CPU is reading data.

Baud Out (BAUDOUT), Pin 15: 16x clock signal for the transmitter section of the WD8250. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. The BAUDOUT may also be used for the receiver section by tying this output to the RCLK input of the chip.

Interrupt (INTRPT), Pin 30: Goes high whenever any one of the following interrupt sources has an active high condition: Receiver Error Flag; Received Data Available; Transmitter Holding Register Empty; and MODEM Status. The INTRPT signal is reset low upon a Master Reset operation.

Serial Output (SOUT), Pin 11: Composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Marking (logic 1) state upon a Master Reset Operation.

Input/Output Signals

Data (D7-D0) Bus, Pins 1-8: This bus comprises eight TRI-STATE input/output lines. The bus provides bidirectional communications between the WD8250 and the CPU. Data, control words, and status information are transferred via the D7-D0 Data Bus.

External Clock Input/Output (XTAL 1, XTAL 2), Pins 16 and 17: These two pins connect the main timing reference (crystal or signal clock) to the WD8250.

Table 1. Reset Control of Registers and Pinout Signals

Register/Signal	Reset Control	Reset State
Receiver Buffer Register	First Word Received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Master Reset	All Bits Low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High and Bits 1-7 Are Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, Except Bits 5 and 6 Are High
Modem Status Register	Master Reset MODEM Signal Inputs	Bits 0-3 Low Bits 4-7 — Input Signal
Divisor Latch (low order bits)	Writing into the Latch	Data
Divisor Latch (high order bits)	Writing into the Latch	Data
SOUT	Master Reset	High
BAUDOUT	Writing into either Divisor Latch	Low
CSOUT	ADS Strobe Signal and State of Chip Select Lines	High/Low
DDIS	DDIS = CSOUT · RCLK · DISTR (At Master Reset, the CPU sets RCLK and DISTR low.)	High
INTRPT	Master Reset	Low
OUT 2	Master Reset	High
RTS	Master Reset	High
DTR	Master Reset	High
OUT 1	Master Reset	High
D7-D0 Data Bus Lines	In THREE-STATE Mode, Unless CSOUT · DISTR = High or CSOUT · DOSTR = High	THREE-STATE Data (ACE to CPU) Data (CPU to ACE)

WD8250 ACCESSIBLE REGISTERS

The system programmer may access or control any of the WD8250 registers summarized in table 2 via the CPU. These registers are used to control WD8250 operations and to transmit and receive data.

WD8250 Line Control Register

The system programmer specifies the format of the asynchronous data communications exchange via

the Line Control Register. In addition to controlling the format, the programmer may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The contents of the Line Control Register are indicated and are described below.

Table 2. Summary of WD8250 Accessible Registers

Bit No.	Register Address									
	0DLAB=0	0DLAB=0	1DLAB=0	2	3	4	5	6	0DLAB=1	1DLAB=1
	Receiver Buffer Register (Read Only)	Holding Register (Write Only)	Interrupt Enable Register	Interrupt Identification Register	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Divisor Latch (LS)	Divisor Latch (MS)
0	Data Bit 0*	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OR)	Delta Data Set Ready (DDSR)	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	MODEM Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Receive Line Signal Detect (DSLSD)	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Shift Register Empty (TSRE)	Ring Indicator (RI)	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Received Line Signal Detect (RLSD)	Bit 7	Bit 15

*Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of stop bits in each transmitted or received serial character. If bit 2 is a logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, 1½ Stop bits are generated or checked. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 Stop bits are generated or checked.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (SOUT) is forced to the

Spacing (logic 0) state and remains there (until reset by a low-lever bit 6) regardless of other transmitter activity. This feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

WD8250 Programmable Baud Rate Generator

The WD8250 contains a programmable Baud Rate Generator that is capable of taking any clock input (DC to 3.1 MHz) and dividing it by any divisor from 1 to $(2^{16} - 1)$. The output frequency of the Baud Generator is 16x the Baud rate. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 3 and 4 illustrate the use of the Baud Generator with two different driving frequencies. One is referenced to a 1.8432 MHz crystal. The other is a 3.072 MHz crystal.

NOTE

The maximum operating frequency of the Baud Generator is 3.1 MHz. However, when using divisors of 5 and below, the maximum frequency is equal to the divisor in MHz. For example, if the divisor is 1, then the maximum frequency is 1 MHz. In no case should the data rate be greater than 56K Baud.

Table 3 Baud Rates Using 1.8432 MHz Crystal.

Desired Baud Rate	Divisor Used to Generate 16x Clock	Percent Error Difference Between Desired and Actual
50	2304	—
75	1536	—
110	1047	0.026
134.5	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.86

NOTE: 1.8432MHz is the standard 8080 frequency divided by 10.

Table 4 Baud Rates Using 3.072 MHz Crystal.

Desired Baud Rate	Divisor Used to Generate 16x Clock	Percent Error Difference Between Desired and Actual
50	3840	—
75	2560	—
110	1745	0.026
134.5	1428	0.034
150	1280	—
300	640	—
600	320	—
1200	160	—
1800	107	—
2000	96	—
2400	80	—
3600	53	0.628
4800	40	—
7200	27	1.23
9600	20	—
19200	10	—
38400	5	—
56000	3	14.285

Line Status Register

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated in table 2 and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 may be reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register or by writing a logic 0 into it from the CPU.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level).

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (Logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits).

NOTE

Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the WD8250 is ready to accept a new character for transmission. In addition, this bit causes the WD8250 to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Shift Register Empty (TSRE) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Shift Register is idle. It is reset to logic 0 upon a data transfer from the Transmitter

Holding Register to the Transmitter Shift Register. Bit 6 is a read-only bit.

Bit 7: This bit is permanently set to logic 0.

Interrupt Identification Register

The WD8250 has an on chip interrupt capability that allows for complete flexibility in interfacing to all popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the WD8250 prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and source of that interrupt are stored in the Interrupt Identification Register (refer to table 5). The Interrupt Identification Register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in table 2 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in table 5.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Interrupt Enable Register

This 8-bit register enables the four interrupt sources of the WD8250 to separately activate the chip Interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are indicated in table 2 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1. Bit 0 is reset to logic 0 upon completion of the associated interrupt service routine.

Table 5 Interrupt Control Functions.

Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

Bit 1: This bit enables the Receiver Line Status Interrupt when set to logic 1. Bit 2 is reset to logic 0 upon completion of the associated interrupt service routine.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1. Bit 3 is reset to logic 0 upon completion of the associated interrupt service routine.

Bits 4 through 7: These four bits are always logic 0.

MODEM Control Register

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in table 2 and are described below.

Bit 0: This bit controls the Data Terminal Ready (DTR) output. When bit 0 is set to a logic 1, the DTR output is forced to a logic 0. When bit 0 is reset to a logic 0, the DTR output is forced to a logic 1.

NOTE

The DTR output of the WD8250 may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send (RTS) output. Bit 1 affects the RTS output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 (OUT 1) signal, which is an auxiliary user-designated output. Bit 2

affects the OUT 1 output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 (OUT 2) signal, which is an auxiliary user-designated output. Bit 3 affects the OUT 2 output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a loopback feature for diagnostic testing of the WD8250. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control inputs (CTS, DSR, RLSD, and RI) are disconnected; and the four MODEM Control outputs (DTR, RTS, OUT 1, and OUT 2) are internally connected to the four MODEM Control inputs. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the WD8250.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

The WD8250 interrupt system can be tested by writing into the lower six bits of the Line Status Register

and the lower four bits of the MODEM Status Register. Setting any of these bits to a logic 1 generates the appropriate interrupt (if enabled). The resetting of these interrupts is the same as in normal WD8250 operation. To return to this operation, the registers must be reprogrammed for normal operation and then bit 4 must be reset to logic 0.

Bits 5 through 7: These bits are permanently set to logic 0.

MODEM Status Register

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in table 2 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the \overline{CTS} input to the chip has changed state since the last time it was read by the CPU.

Typical Applications

Figures 1 and 2 show how to use the WD8250 chip in an 8080A system and in a microcomputer system with a high-capacity data bus.

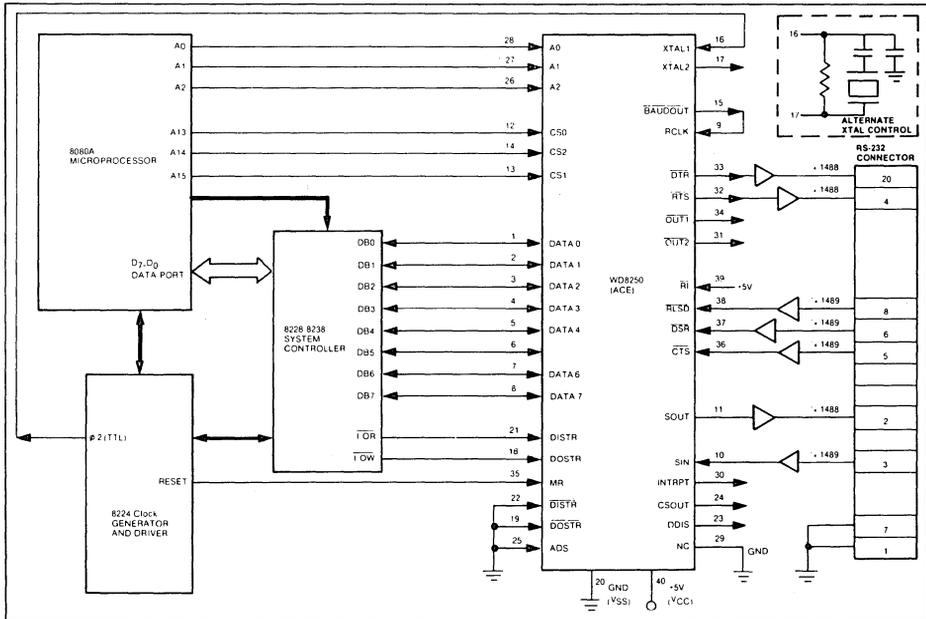


FIGURE 1 TYPICAL 8-BIT MICROPROCESSOR/RS-232 TERMINAL INTERFACE USING THE ACE.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the \overline{DSR} input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the \overline{RI} input to the chip has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the RLSD input to the chip has changed state.

NOTE

Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send (\overline{CTS}) input.

Bit 5: This bit is the complement of the Data Set Ready (\overline{DSR}) input.

Bit 6: This bit is the complement of the Ring Indicator (\overline{RI}) input.

Bit 7: This bit is the complement of the Received Line Signal Detect (RLSD) input.

Typical Applications (continued)

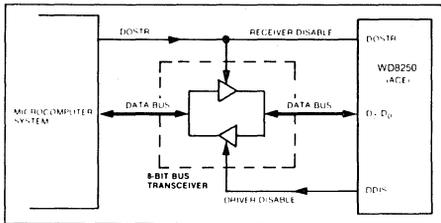


FIGURE 2 TYPICAL INTERFACE FOR A HIGH-CAPACITY DATA BUS.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias 0°C to +70°C
 Storage Temperature -65°C to +150°C (Ceramic)
 -50°C to +125°C (Plastic)
 All Input or Output Voltages with Respect to V_{SS} -0.5 V to +7.0 V
 Power Dissipation 750 mW

Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.

DC Electrical Characteristics

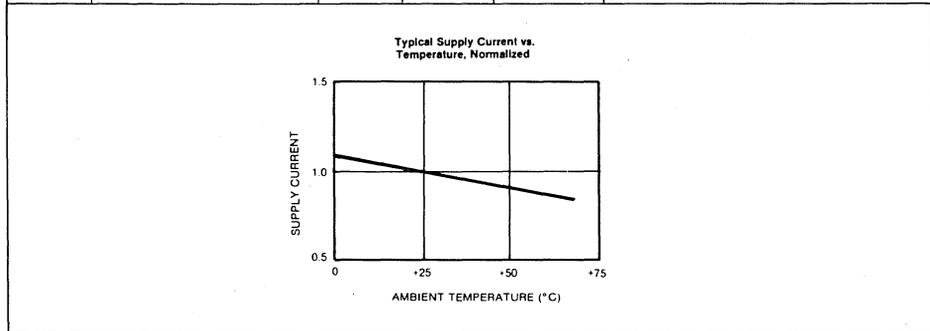
T_A = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{SS} = 0V, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V _{ILX}	Clock Input Low Voltage	-0.5		0.8	V	$I_{OL}=1.6\text{mA}$ on all outputs $I_{OH}=-100\ \mu\text{A}$
V _{IHX}	Clock Input High Voltage	2.0		V _{CC}	V	
V _{IL}	Input Low Voltage	-0.5		0.8	V	
V _{IH}	Input High Voltage	2.0		V _{CC}	V	
V _{OL}	Output Low Voltage			.45	V	
V _{OH}	Output High Voltage	2.4			V	
I _{CC(AV)}	Avg Power Supply Current (V _{CC})			150	ma	
I _{IL}	Input Leakage			± 10	μA	
I _{CL}	Clock Leakage			± 10	μA	

Capacitance

T_A = 25°C, V_{CC} = V_{SS} = 0V

Symbol	Parameter	Typ.	Max.	Units	Test Conditions
C _{XIN}	Clock Capacitance	10	15	pF	$f_c=1\ \text{MHz}$ Unmeasured pins returned to V _{SS}
C _{IN}	Input Capacitance	6	10	pF	
C _{OUT}	Output Capacitance	10	20	pF	



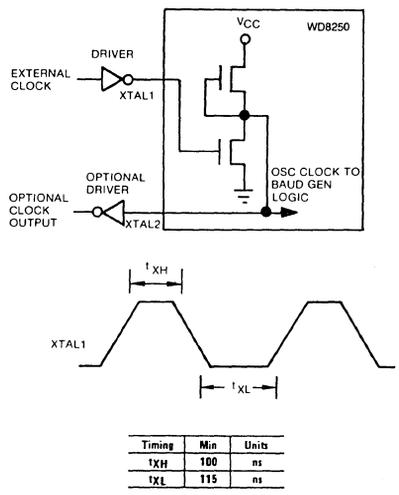
AC Electrical Characteristic TA = 0°C to +70°C, VCC = +5V ± 5%

1 Z0-CM10

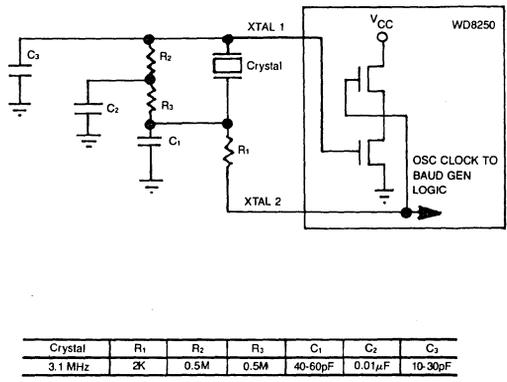
Symbol	Parameter	Units	Min	Max	Test Conditions
tAW	Address Strobe Width	ns	120		1TTL Load
tAS	Address Setup Time	ns	100		1TTL Load
tAH	Address Hold Time	ns	0		1TTL Load
tCSS	Chip Select Output Delay from Strobe	ns		160	1TTL Load
tDID	DISTR/DISTR Strobe Delay	ns	50		1TTL Load
tDIW	DISTR/DISTR Strobe Width	ns	300		1TTL Load
tRC	Read Cycle Delay	ns	655		1TTL Load
RC	Read Cycle=tAW + tDID + tDIW + tRC	ns	1000		1TTL Load
tDD	DISTR/DISTR to Driver Disable Delay	ns		200	1TTL Load
tDDD	Delay from DISTR/DISTR to Data	ns		300	1TTL Load
tHZ	DISTR/DISTR to Floating Data Delay	ns	60		1TTL Load
tDOD	DOSTR/DOSTR Strobe Delay	ns	20		1TTL Load
tDOW	DOSTR/DOSTR Strobe Width	ns	175		1TTL Load
tWC	Write Cycle Delay	ns	685		1TTL Load
WC	Write Cycle=tAW + tDOD + tDOW + tWC	ns	1000		1TTL Load
tDS	Data Setup Time	ns	100		1TTL Load
tDH	Data Hold Time	ns	20		1TTL Load
tCSC	Chip Select Output Delay from Select	ns		135	1TTL Load
tDIC	DISTR/DISTR Delay from Select	ns	50		1TTL Load
tDOC	DOSTR/DOSTR Delay from Select	ns	50		1TTL Load

*Applicable only when ADS input is not tied permanently low.

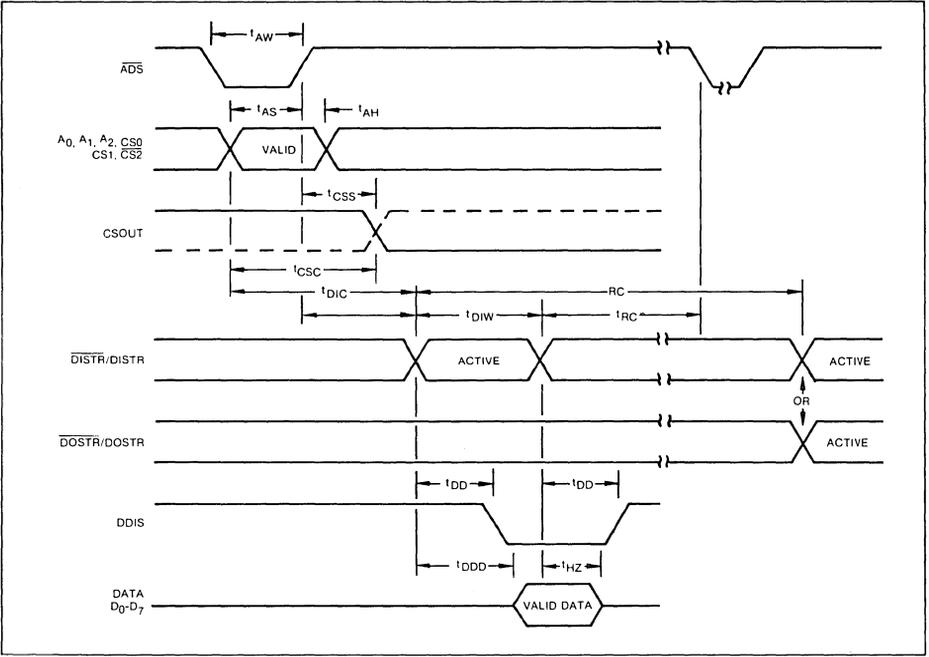
Symbol	Parameter	Min.	Max.	Units	Test Conditions
Baud Generator					
N	Baud Rate Divisor	1	2 ¹⁶ -1		
tBLD	Baud Output Negative Edge Delay		250 typ	ns	100pF Load
tBHD	Baud Output Positive Edge Delay		250 typ	ns	100pF Load
tLW	Baud Output Down Time	425 Typ		ns	100pF Load
tHW	Baud Output Up Time	330 Typ		ns	100pF Load
Receiver					
tSCD	Delay from RCLK to Sample Time		2 typ	μs	
tSINT	Delay from Stop to Set Interrupt		2 typ	μs	100pF Load
tRINT	Delay from DISTR/DISTR (RD RBR) to Reset Interrupt	.250	1 typ	μs	100pF Load
Transmitter					
tHR	Delay from DOSTR/DOSTR (WR THR) to Reset Interrupt	.250	1 typ	μs	100pF Load
tIRS	Delay from Initial INTR Reset to Transmit Start		16 typ	BAUDOUT Cycles	
tSI	Delay from Initial Write to Interrupt		24 typ	BAUDOUT Cycles	
tSS	Delay from Stop to Next Start	.250	1 typ	μs	
tSTI	Delay from Stop to Interrupt (THRE)		8 typ	BAUDOUT Cycles	
TIR	Delay from DISTR/DISTR (RD IIR) to Reset Interrupt (THRE)	.250	1 typ	μs	100pF Load
Modem Control					
tMDO	Delay from DOSTR/DOSTR (WR MCR) to Output	.250	1 typ	μs	100pF Load
tSIM	Delay to Set Interrupt from MODEM Input	.250	1 typ	μs	100pF Load
tRIM	Delay to Reset Interrupt from DISTR/DISTR (RD MSR)	.250	1 typ	μs	100pF Load



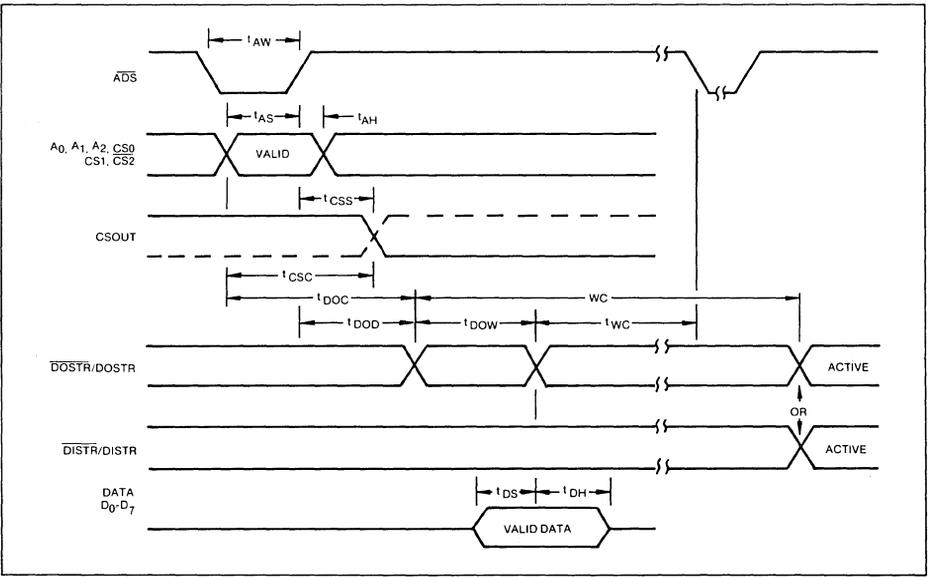
EXTERNAL CLOCK INPUT (3.1 MHz MAX.)



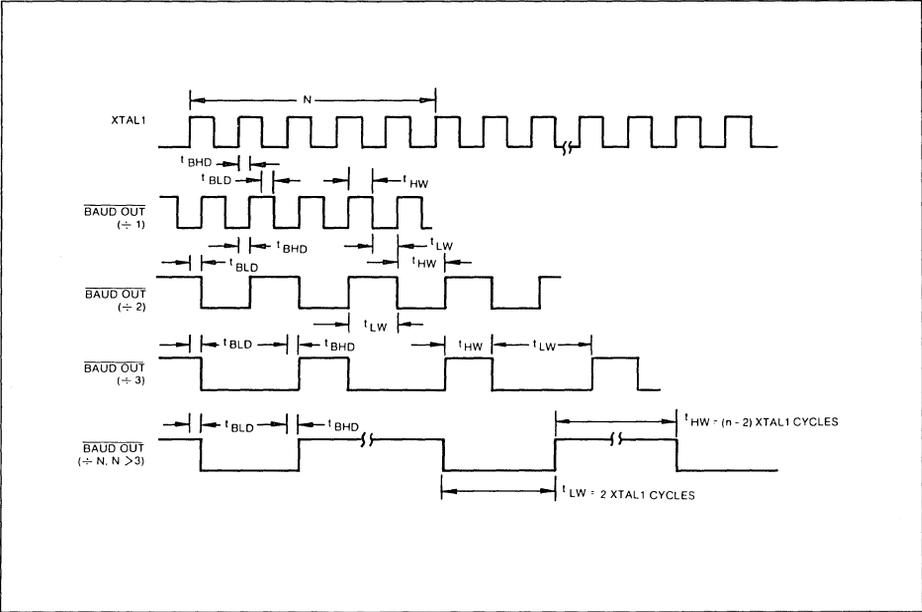
TYPICAL CRYSTAL OSCILLATOR NETWORK



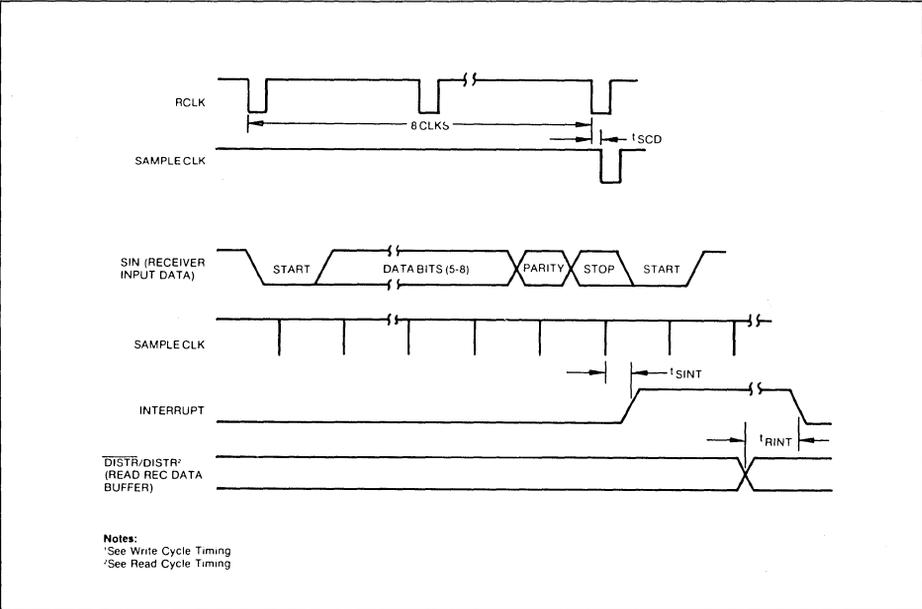
READ CYCLE TIMING



WRITE CYCLE TIMING

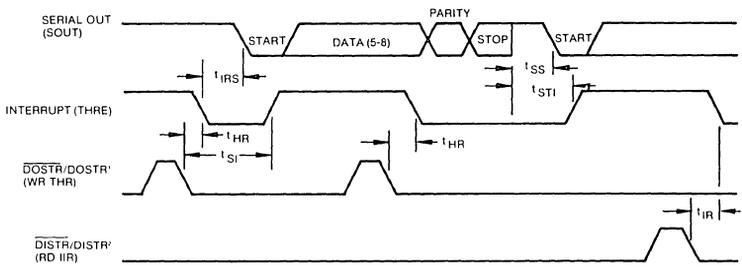


BAUDOUT TIMING



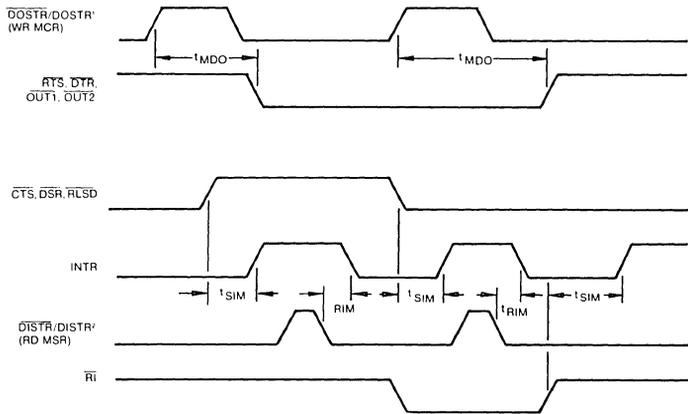
RECEIVER TIMING

Notes:
 *See Write Cycle Timing
 *See Read Cycle Timing



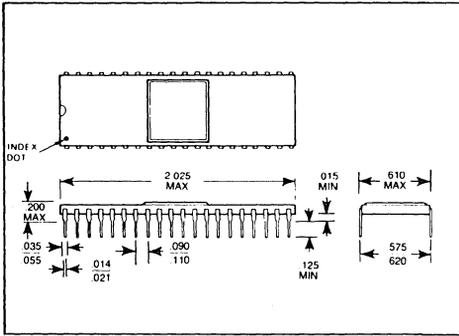
Notes:
¹See Write Cycle Timing
²See Read Cycle Timing

TRANSMITTER TIMING

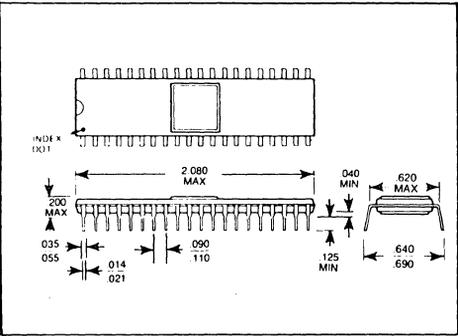


Notes:
¹See Write Cycle Timing
²See Read Cycle Timing

MODEM CONTROLS TIMING



WD8250 CERAMIC (HERMETIC)



WD8250 PLASTIC PACKAGE

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WD 2123 DEUCE DUAL ENHANCED UNIVERSAL COMMUNICATIONS ELEMENT

1-20-10100

MARCH, 1981

FEATURES

- TWO INDEPENDENT ASYNCHRONOUS FULL DUPLEX DATA COMMUNICATION CHANNELS (2 BOARDS)
- TWO INDEPENDENT BAUD RATE GENERATORS (ONE PER CHANNEL)
- EACH CHANNEL WITH FOLLOWING FEATURES:
 - SELECTABLE 5 TO 8 BIT CHARACTERS
 - 1X, 16X, 64X CLOCK RATES
 - 16 SELECTABLE BAUD RATE CLOCK FREQUENCIES (INTERNAL)
 - LINE BREAK DETECTION AND GENERATION
 - 1, 1½, OR 2 STOP BIT SELECTION
 - FALSE START BIT DETECTION
 - ODD OR EVEN PARITY GENERATE AND DETECTION
 - OVERRUN AND FRAMING DETECTION
 - DOUBLE BUFFERING OF DATA
 - TTL COMPATIBLE INPUTS AND OUTPUTS
 - COMPATIBLE WITH 8251A (ASYNC ONLY) AND WD1983 DEVICES

- DIAGNOSTIC LOCAL LOOP-BACK MODE
- RXD INITIALIZATION UPON MASTER RESET
- ON-BOARD OSCILLATOR FOR EASE OF USE WITH A CRYSTAL
- VERSATILE CLOCK SELECT OPTIONS FOR INDEPENDENT TRANSMIT AND RECEIVE RATES

INTRODUCTION

The Western Digital WD2123 Dual Enhanced Universal Communications Element (DEUCE) is a single chip MOS/LSI Data Communications Controller Circuit that contains two independent full-duplex asynchronous RECEIVER/TRANSMITTER CHANNELS and two independent BAUD RATE GENERATORS. The WD2123 is fabricated in N-Channel silicon gate technology and is packaged in a 40 pin plastic or ceramic package. All inputs and outputs are TTL compatible.

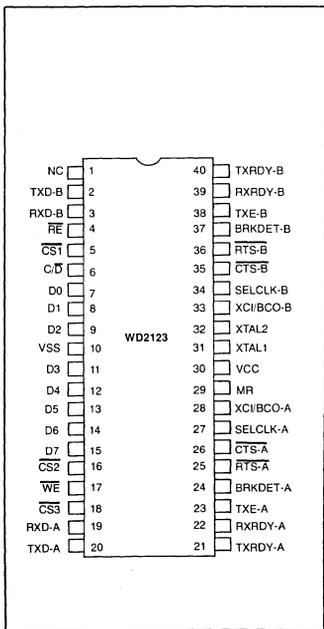


Figure 1 WD2123 PINOUT DIAGRAM

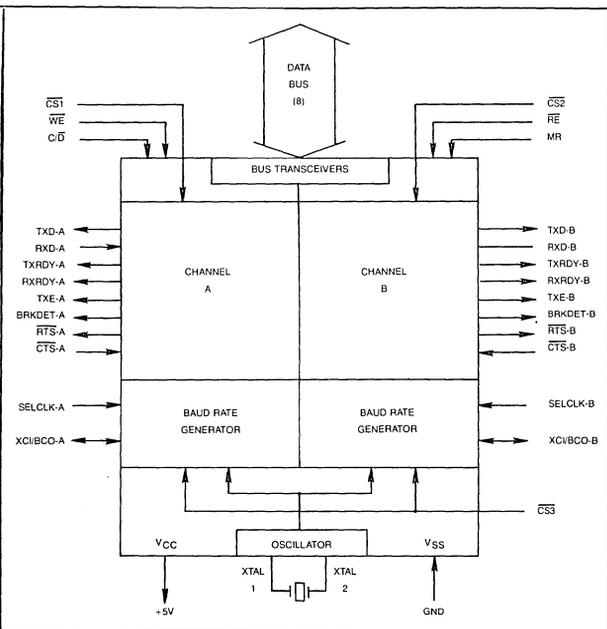


Figure 2 WD2123 BLOCK DIAGRAM

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
10	GROUND	VSS	Ground
30	POWER SUPPLY	VCC	+5VDC power supply input.
7	DATA BUS	D0	This is the 8 bit Bidirectional Data Bus. It is the means of communication between the WD2123 and the CPU. Data, control, mode and status registers are accessed via this bus.
8		D1	
9		D2	
11		D3	
12		D4	
13		D5	
14		D6	
15		D7	
5	CHIP SELECT ONE	$\overline{CS1}$	V_{IL} on this input selects Channel A and enables computer communications with Channel A Data, control and status registers.
16	CHIP SELECT TWO	$\overline{CS2}$	V_{IL} on this input selects Channel B and enables computer communications with Channel B Data, control and status registers.
18	CHIP SELECT THREE	$\overline{CS3}$	V_{IL} on this input select the Baud Rate registers for programming.
6	CONTROL or DATA SELECT	C/\overline{D}	This input is used in conjunction with the appropriate Chip Select and an active read or write operation to determine register access via the Data Bus.
4	READ ENABLE	\overline{RE}	V_{IL} on this input allows the CPU to read data, or status information from the selected register.
17	WRITE ENABLE	\overline{WE}	V_{IL} on this input allows the CPU to write data or control information into the selected register.
29	MASTER RESET	MR	V_{IH} on this input resets both channels to the idle state and resets the status, command, mode and Data registers.
31	CRYSTAL OSCILLATOR INPUT	XTAL1	This is the input side of the on-chip oscillator. It can also be driven by an external clock source.
32	CRYSTAL OSCILLATOR OUTPUT	XTAL2	This is the output side of the on-chip oscillator.
27	SELECT CLOCK (Channel A)	SELCLK-A	This input is used in conjunction with the Clock Select bit (CR1) in the command register to determine the baud clock source for Channel A.
34	SELECT CLOCK (Channel B)	SELCLK-B	This input is used in conjunction with the Clock Select bit (CR1) in the command register to determine the baud clock source for Channel B.
28	EXTERNAL CLOCK INPUT/BAUD CLOCK OUTPUT-(Channel A)	XCI/BCO-A	This is a bidirectional port, which is used as the externally applied baud clock input or the internal baud rate generator output depending on the states of SELCLK and CR1 command bit. (Channel A)
33	EXTERNAL CLOCK INPUT/BAUD CLOCK OUTPUT-(Channel B)	XCI/BCO-B	This is a bidirectional port, which is used as the externally applied baud clock input or the internal baud rate generator output depending on the states of SELCLK and CR1 command bit. (Channel B)
26	CLEAR-TO-SEND (Channel A)	$\overline{CTS-A}$	V_{IL} on this input enables Channel A to transmit serial data if the Transmitter is enabled.
35	CLEAR-TO-SEND (Channel B)	$\overline{CTS-B}$	V_{IL} on this input enables Channel B to transmit serial data if the Transmitter is enabled.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
20	TRANSMIT DATA (Channel A)	TXD-A	This is the Serial Data Output from Channel A.
2	TRANSMIT DATA (Channel B)	TXD-B	This is the Serial Data Output from Channel B.
19	RECEIVE DATA (Channel A)	RXD-A	This is the Serial Data Input for Channel A.
3	RECEIVE DATA (Channel B)	RXD-B	This is the Serial Data Input for Channel B.
21	TRANSMITTER READY (Channel A)	TXRDY-A	This output, when high (V_{OH}), alerts the CPU that Channel A is ready to accept a new data character. The TXRDY output is automatically reset whenever a character is written into the Transmit Holding Register and can be used as an interrupt to the system.
40	TRANSMITTER READY (Channel B)	TXRDY-B	This output, when high (V_{OH}), alerts the CPU that Channel B is ready to accept a new data character. The TXRDY output is automatically reset whenever a character is written into the Transmit Holding Register and can be used as an interrupt to the system.
22	RECEIVER READY (Channel A)	RXRDY-A	This output, when high (V_{OH}), alerts the CPU that Channel B contains a data character that is ready to be input. This output is automatically reset whenever the new character is read from the Receive Holding Register and can be used as an interrupt to the system.
39	RECEIVER READY (Channel B)	RXRDY-B	This output, when high (V_{OH}), alerts the CPU that Channel B contains a data character that is ready to be input. This output is automatically reset whenever the new character is read from the Receive Holding Register and can be used as an interrupt to the system.
23	TRANSMITTER EMPTY (Channel A)	TXE-A	This output, when high (V_{OH}), indicates that Channel A Transmitter has no new characters to send and is waiting in an idle state.
38	TRANSMITTER EMPTY (Channel B)	TXE-B	This output, when high (V_{OH}), indicates that Channel B Transmitter has no new characters to send and is waiting in an idle state.
24	BREAK DETECT (Channel A)	BRKDET-A	This output, when high (V_{OH}), indicates that the Receiver for Channel A has detected a break condition.
37	BREAK DETECT (Channel B)	BRKDET-B	This output, when high (V_{OH}), indicates that the Receiver for Channel B has detected a break condition.
25	REQUEST-TO-SEND (Channel A)	$\overline{\text{RTS-A}}$	A general purpose output that is controlled by the command register bit CR5 for Channel A.
36	REQUEST-TO-SEND (Channel B)	$\overline{\text{RTS-B}}$	A general purpose output that is controlled by the command register bit CR5 for Channel B.
1		NC	No Internal Connection.

Table 1 WD2123 PIN DESCRIPTIONS

GENERAL DESCRIPTION

The WD2123 Block Diagram is shown in Figure 2. The WD2123 is a merger of two WD1983s and one WD1941 from WDC's line of communications devices on one piece of silicon. The 1983 is an asynchronous only version of the 8251A and the 1941 is a baud rate generator. In this manner, 8251A compatibility is maintained with the WD2123 with the added features of 2 channels and 2 baud rate generators on a single chip.

As depicted from the block diagram, the channels are referred to as CHANNELS A and B. CHANNEL A, which is an asynchronous 8251A, is addressed or controlled by the input signal $\overline{CS1}$. CHANNEL B is similarly controlled by $\overline{CS2}$. Finally, the BAUD RATE GENERATORS are controlled by $\overline{CS3}$.

Each channel of the WD2123 can be programmed to receive and transmit asynchronous serial data. The WD2123 performs serial-to-parallel conversion on data characters received from an input/output device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the status of either channel at any time. Status information on a per channel basis reported includes the type and the condition of the transfer operations being performed by the WD2123 as well as any transmission error conditions (parity, overrun, or framing). Programming the WD2123 is identical to the 8251A in the asynchronous mode, remembering that $\overline{CS1}$, when low, selects CHANNEL A and when $\overline{CS2}$ is low, selects CHANNEL B.

The WD2123 BAUD RATE GENERATORS may be selected either internally or externally. The clock select logic includes a clock select control bit CR1 (CS) in each COMMAND INSTRUCTION REGISTER. This control bit allows selection of the internal baud clock or an externally applied clock and works in conjunction with the select clock pin, "SELCLK" and the external clock input/baud clock output pin, "XCI/BCO". When CS is logic 1, the external clock select mode is selected. This means that the transmit and receive clocks (TXC and RXC) are internally tied together and the select clock pin, SELCLK, will determine whether those clocks are driven from the internal baud rate generator (SELCLK is high) or from the external clock input pin, "XCI/BCO", (SELCLK is low).

If the internal BRG clock is selected, (SELCLK is high) then the external clock input pin becomes a BRG clock output. Hence, the mnemonic, "XCI/BCO".

When CR1 (CS) is logic 0, then internal clock select mode is selected. The transmit clock (TXC) is driven by the internal BRG clock and the receive clock is driven by the select clock pin, (SELCLK). The XCI/BCO pin becomes the baud clock output (the same signal that is being applied to TXC).

The WD2123 also provides a local loop-back test mode of operation for each channel. This diagnostic mode is independently controlled via the LB(CR7) bit of the COMMAND REGISTER. When LB is logic 1, the channel is programmed

for Local Loop-Back. In this diagnostic mode, the TXD output is set to the marking (logic "1") state; the output of the TRANSMIT REGISTER is "looped-back" into the RECEIVER REGISTER input; RTS output is held high; the CTS and RXD inputs are ignored. An additional requirement is that the TEN(CR0) command bit and the REN(CR2) be logic 1. The status and output flags operate normally.

Each channel is also provided with break character generation and detection. (A break character is defined as all zero data bits, parity bit and stop bits after a valid start bit.) For break character generation, SBRK (CR3) command bit is set to a logic 1. This causes the TXD output to be forced low (spacing) for as long as SBRK is programmed high. The break detect output and status bit (SR6) is set to logic 1, indicating that the receiver has detected a break character. The framing error flag is also set to 1 for this condition.

ORGANIZATION

The WD2123 is an eight bit bus-oriented device. Communication between the controlling CPU and the two RECEIVER/TRANSMITTER CHANNELS or the two BAUD RATE GENERATORS occurs via the 8 bit data bus through a common set of bus transceivers.

A diagram of one of the two communication controllers is shown in Figure 3. There are two accessible data registers, which buffers transmit and receive data. They are the TRANSMIT HOLDING REGISTER and the RECEIVE HOLDING REGISTER. There is a parallel-to-serial shift register, the TRANSMIT REGISTER and a serial-to-parallel shift register, the RECEIVE REGISTER.

Operational Control and monitoring of the CHANNEL is performed by two CONTROL REGISTERS (the COMMAND INSTRUCTION REGISTER and the MODE INSTRUCTION REGISTER) and the STATUS REGISTER.

A read/write control circuit allows programming/monitoring or loading/reading of data in the CONTROL, STATUS and HOLDING REGISTERS by activating the appropriate control lines: Chip Select ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$), READ ENABLE (\overline{RE}), WRITE ENABLE (\overline{WE}) and CONTROL or DATA SELECT ($\overline{C/D}$).

Internal control of each channel is by means of two internal microcontrollers: one for transmit and one for receive. The control registers, various counters and external signals provide inputs to the microcontrollers, which generate the necessary control signals to send and receive serial data according to the programmed protocol.

A diagram of one of the two BAUD RATE GENERATORS is shown in Figure 4. The 4 low order DATA BUS bits, DO-D3, are used to program the desired rate by loading the RATE REGISTER. Control signals $\overline{CS3}$, \overline{WE} and $\overline{C/D}$ are used to select and load the appropriate register.

The contents of the RATE REGISTER is decoded and addresses a FREQUENCY SELECT ROM for the proper frequency, which is generated by the DIVIDER circuitry and the control logic.

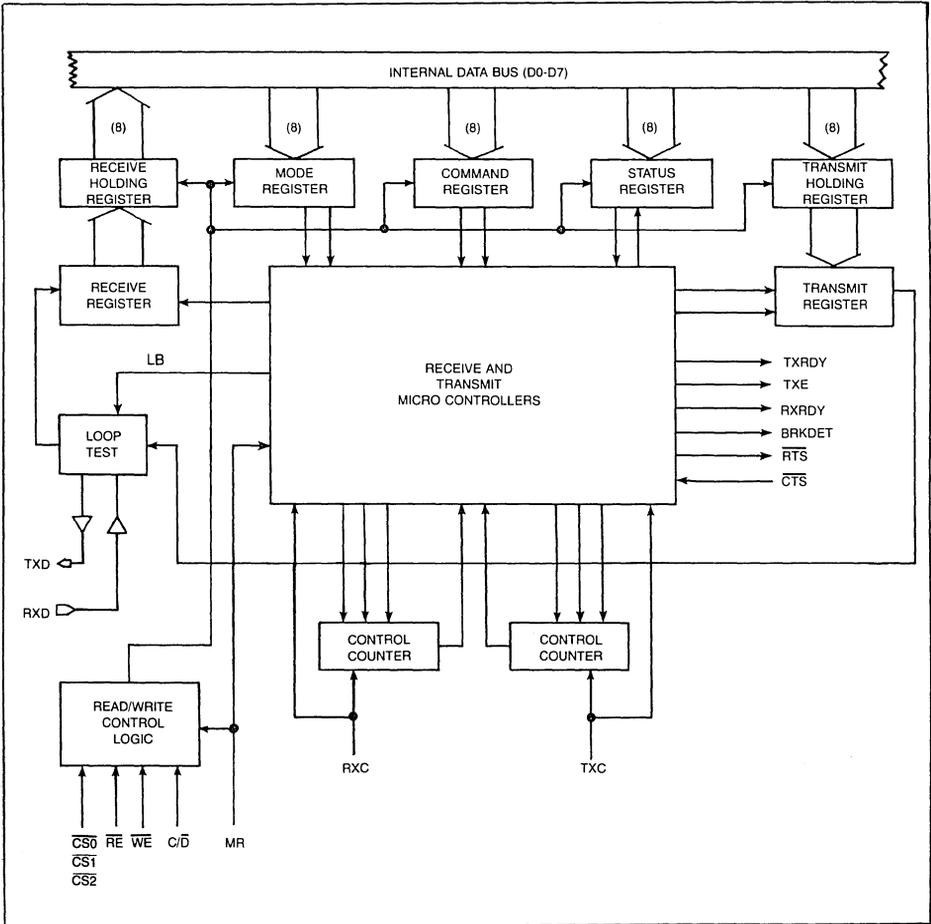


Figure 3 RECEIVE/TRANSMIT COMMUNICATIONS CONTROLLER DIAGRAM

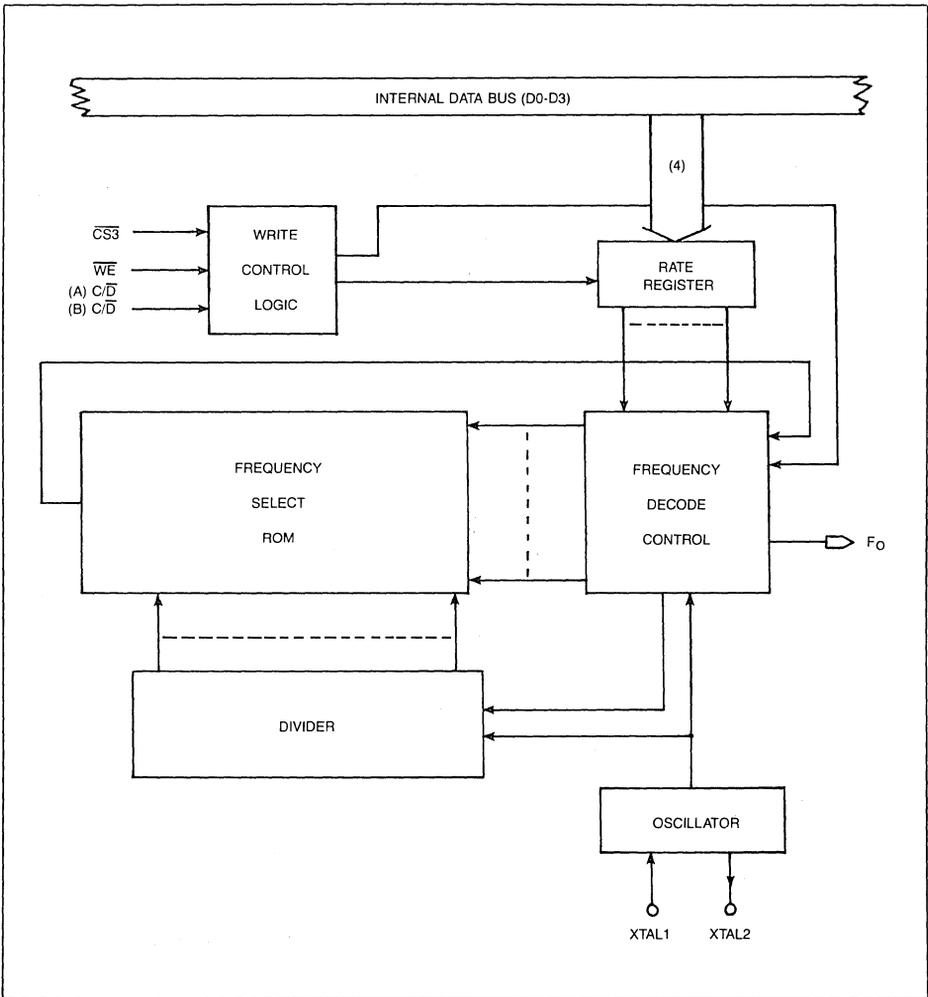


Figure 4 WD2123 BAUD RATE GENERATOR DIAGRAM

The WD2123 registers are addressed by the following table:

C/D	\overline{RE}	\overline{WE}	$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	REGISTER SELECTED
L	L	H	L	H	H	RECEIVE HOLDING REG. — CHA
L	H	L	L	H	H	TRANSMIT HOLDING REG. — CHA
H	L	H	L	H	H	STATUS REG. — CHA
H	H	L	L	H	H	MODE AND COMMAND REG. — CHA
L	L	H	H	L	H	RECEIVE HOLDING REG. — CHB
L	H	L	H	L	H	TRANSMIT HOLDING REG. — CHB
H	L	H	H	L	H	STATUS REG. — CHB
H	H	L	H	L	H	MODE and COMMAND REG. — CHB
L	H	L	H	H	L	RATE REG. — CHA
H	H	L	H	H	L	RATE REG. — CHB
X	X	X	H	H	H	DATA BUS IN HIGH IMPEDANCE MODE

Table 2 WD2123 REGISTER ADDRESSING

Note:

"L" means V_{IL} at pins.

"H" means V_{IH} at pins.

"X" means don't care.

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The WD2123 contains two MODE REGISTERS—one for each channel. The format and definition of the MODE REGISTERS are shown below:

MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
S2	S1	EP	PEN	L2	L1	B2	B1

B2	B1	BAUD RATE FACTOR
0	0	Undefined
0	1	1X
1	0	16X
1	1	64X
L2	L1	CHARACTER LENGTH
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits
PEN	PARITY ENABLE	
0	Disable Parity	
1	Enable Parity	
EP	PARITY SELECT	
0	Odd Parity	
1	Even Parity	
S2	S1	NUMBER OF STOP BITS
0	0	Invalid
0	1	1 Bit
1	0	1½ Bits
1	1	2 Bits

Table 3 WD2123 MODE REGISTERS

The WD2123 contains two COMMAND REGISTERS—one per channel. The format and definition of the COMMAND REGISTERS are shown below:

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
LB	IR	RTS	ER	SBK	REN	CS	TEN

TEN	TRANSMIT ENABLE
1	Enable
0	Disable
CS	CLOCK SELECT
1	External Clock Select Mode
0	Internal Clock Select Mode
REN	RECEIVE ENABLE
1	Enable
0	Disable
SBK	SEND BREAK CHARACTER
1	Force TXD Low
0	Normal Operation
ER	ERROR RESET
1	Reset Error Flags
0	No Reset
RTS	REQUEST TO SEND
1	Force $\overline{\text{RTS}}$ pin = 0 (V_{OL})
0	Force RTS pin = 1 (V_{OH})
IR	INTERNAL RESET
1	Returns WD2123 to Mode Instruction Format
LB	LOOP BACK ENABLE
0	Normal Operation Mode
1	Local Loop-Back Mode

Table 4 WD2123 CONTROL REGISTERS

The WD2123 contains two STATUS REGISTERS—one per channel. The STATUS REGISTER is a read-only register. The format and definition of the STATUS REGISTERS are shown below:

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
CTS	BRK DET	FE	OE	PE	TXE	RX RDY	TX RDY

TXRDY	TRANSMITTER READY
1	Denotes THR is empty and ready for a new character
0	THR not empty. (Reset when THR is loaded by CPU)
RXRDY	RECEIVER READY
1	Denotes that the RHR contains a valid character
0	RHR does not contain a valid character. (Reset when the CPU reads the RHR)
TXE	TRANSMITTER EMPTY
1	Denotes that the TR is empty
0	Denotes that the TR is not empty
PE	PARITY ERROR
1	Denotes Parity Error
0	No Parity Error. (Reset by ER bit of command register)
OE	OVERRUN ERROR
1	Denotes Overrun Error
0	No Overrun Error. (Reset by ER bit of command register)
FE	FRAMING ERROR
1	Denotes Framing Error
0	No Framing Error. (Reset by ER bit of command register)
BRKDET	BREAK DETECT
1	Indicates that the receiver has detected a line break condition. (FE will also be set)
0	No Break Condition detected for at least one bit time
CTS	CLEAR-TO-SEND
1	Indicates that the $\overline{\text{CTS}}$ pin is active (V_{IL})
0	Indicates that the $\overline{\text{CTS}}$ pin is not active (V_{IH})

Table 5 WD2123 STATUS REGISTERS

OPERATING DESCRIPTION

The WD2123 is primarily designed to operate in an 8 bit microprocessor environment, although other control logic schemes are easily implemented. The DATA BUS and the interface control signals ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$, $\overline{C/D}$, \overline{RE} , \overline{WE}) should be connected to the microprocessor's data bus and system control bus. A 1.8432 MHz crystal should be connected to the WD2123 as shown in figure 5. The appropriate TXC (RXC) clock frequencies should be programmed via system software. Different Baud clock configurations are possible, such as separate transmit and receive frequencies, and are outlined in the general description.

For typical data communication applications, the RXD and TXD input/outputs can be connected to RS-232C interface circuits. Interface control signals, \overline{CTS} and \overline{RTS} , are controlled and sensed by the CPU through the COMMAND and STATUS REGISTERS and can be configured in several ways. The \overline{CTS} input can be used to synchronize the transmitter to external events.

The TXRDY, RXRDY, TXE and BRKDET FLAGS may be connected to the microprocessor system as interrupt inputs or the STATUS REGISTER can be periodically read in a polled environment to support data communication control operations.

The SBRK bit of the COMMAND REGISTER (CR3) is used to send a Break Character. (A Break Character is defined as a start bit, and all zero data, parity and stop bits.) When the CR3 bit is set to a "1", it causes the transmitter output, TXD, to be forced low after the last bit of the last character is transmitted.

The Receiver is equipped with logic to look for a break character. When a break is received, the BREAK DETECT (BRKDET) FLAG and STATUS bit are set to "1". When the receiver input line goes high (V_{IH}) for at least one clock period, the receiver resets the BRKDET FLAG and resumes its search for a start bit.

PROGRAMMING PROCEDURE

The programming sequence of the two channels will be different, depending on whether it is an initialization sequence (that is, one performed right after a hardware master reset occurs) or a re-programming sequence (that is, one performed to change the protocol characteristics (Parity, rate, character length, etc.) after the device has been previously operating in the system). The programming sequence differs, in that, after a master reset, the chip is set to expect the first control write operation ($\overline{C/D}=1$) to contain a *mode instruction*. Any subsequent control write operations will be transferred to the *command instruction register*.

Now when it is desired to *change the mode instruction register contents*, the following re-programming sequence should be performed. A Command Control word of "40" Hex is written to the Chip. This turns off the Receiver and Transmitter and sets the IR (Internal Reset) bit. This bit causes the read/write control logic to expect the *next control write operation* to be a *new mode instruction*. After the *new mode instruction* is written to the chip, all subsequent control write operations will again be interpreted as *command instructions*. Therefore, after the *new mode instruction* is performed, the next command would turn the receiver and transmitter back on and resume normal Data operations.

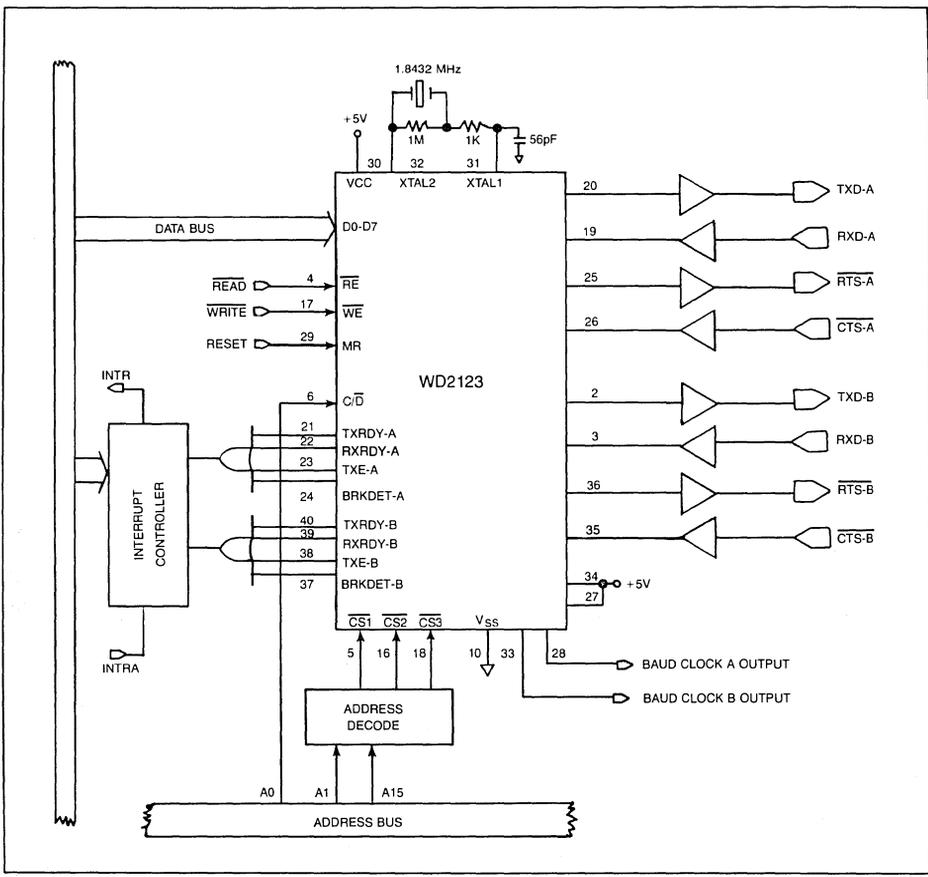


Figure 5 WD2123 MICROPROCESSOR APPLICATION

ABSOLUTE MAXIMUM RATINGS

V_{DD} with respect to V_{SS}	0.5V to +12V
Voltage on Any Pin with Respect to Ground	−0.5V to +7V
Power Dissipation	500mW.

STORAGE TEMPERATURE:

Ceramic: −65°C to +150°C
Plastic: −55°C to +125°C

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

DC ELECTRICAL CHARACTERISTICS

$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$; $V_{CC} = 5.0\text{V} \pm 5\%$; $\text{GND} = 0\text{V}$

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	−0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 1.6\text{ mA}$
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -100\text{ }\mu\text{A}$
I_{DL}	Data Bus Leakage (High Impedance State)			−50 10	μA	$V_{OUT} = 0.45\text{V}$ $V_{OUT} = V_{CC}$
I_{IL}	Input Leakage			10	μA	$V_{IN} = V_{CC}$
I_{CC}	Power Supply Current		50	100	mA	$V_{CC} = 5.25\text{V}$ No Load

Table 7 WD2123 D.C. PARAMETERS

CAPACITANCE

$T_A = 25^\circ\text{C}$; $V_{CC} = \text{GND} = 0\text{V}$

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	$f_C = 1\text{MHz}$
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND.

Table 8 WD2123 CAPACITANCE LEVELS

AC ELECTRICAL CHARACTERISTICS

 $T_A = 0^\circ\text{C to } +70^\circ\text{C}; V_{CC} = 5.0\text{V} \pm 5\%; \text{GND} = 0\text{V}$

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
BUS PARAMETERS					
Read Cycle					
t_{AR}	Address Stable Before READ (CS,C/D)	50		ns	
t_{RA}	Address Hold Time for READ (CS,C/D)	5		ns	
t_{RE}	READ Pulse Width	350		ns	
t_{RD}	Data Delay from READ		200	ns	$C_L = 50 \text{ pF}$
t_{RDH}	READ to Data Floating		200	ns	$C_L = 50 \text{ pF}$
		25		ns	$C_L = 15 \text{ pF}$
Write Cycle					
t_{AW}	Address Stable Before WRITE	20		ns	
t_{WA}	Address Hold Time for WRITE	20		ns	
t_{WE}	WRITE Pulse Width	350		ns	
t_{DS}	Data Set-Up Time for WRITE	100		ns	
t_{WDH}	Data Hold Time for WRITE	100		ns	
OTHER TIMINGS					
t_{TXC}	Transmit Clock Period	1.6		us	
t_{DTX}	TxD Delay from Falling Edge of TxC		200	ns	$C_L = 100 \text{ pF}$
t_{SRX}	Rx Data Set-Up Time to Sampling Pulse	200		ns	$C_L = 100 \text{ pF}$
t_{HRX}	Rx Data Hold Time to Sampling Pulse	100		ns	$C_L = 100 \text{ pF}$
f_{TX}	Transmitter Input Clock Frequency 1x Baud Rate 16x and 64x Baud Rate	DC DC	500 600	kHz kHz	$C_L = 100 \text{ pF}$
t_{TPW}	Transmitter Input Clock Pulse Width 1x Baud Rate 16x and 64x Baud Rate	1.0 800		us ns	
t_{TPD}	Transmitter Input Clock Pulse Delay 1x Baud Rate 16x and 64x Baud Rate	1.0 800		us ns	

Table 9 WD2123 A.C. PARAMETERS

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
f _{RX}	Receiver Input Clock Frequency 1x Baud Rate 16x and 64x Baud Rate	DC DC	500 600	kHz kHz	
t _{RPW}	Receiver Input Clock Pulse Width 1x Baud Rate 16x and 64x Baud Rate	1.0 800		us ns	
t _{RPD}	Receiver Input Clock Pulse Delay 1x Baud Rate 16x and 64x Baud Rate	1.0 800		us ns	
t _{TX}	TxRDY Delay from Center of Stop Bit		8	t _{RXC}	C _L = 50pF (16X)
t _{RX}	RxRDY Delay from Center of Stop Bit		½	t _{RXC}	
t _{IS}	Internal BRKDET Delay from Center of Data Bit		1	RXC	
t _{TRD}	TxRDY Delay from Falling Edge of WRITE		450	ns	
t _{TOD}	TXD Output from Falling Edge of WRITE		1½	t _{TXC}	
t _{WC}	Control Delay from Rising Edge of WRITE (RTS)		200	ns	
t _{CR}	Control to READ Set-Up Time (CTS)		1	t _{TXC}	

Table 9 WD2123 A.C. PARAMETERS

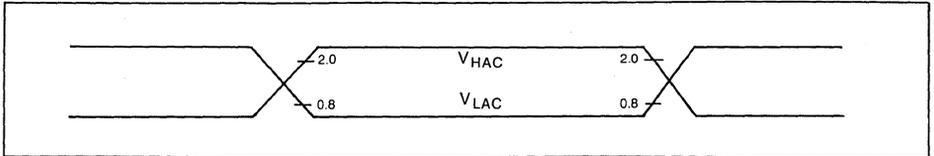


Figure 6 A.C. TEST POINTS

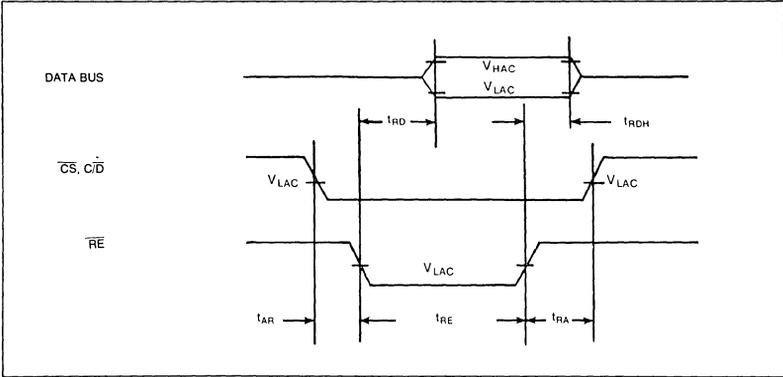


Figure 7 WD2123 READ TIMING

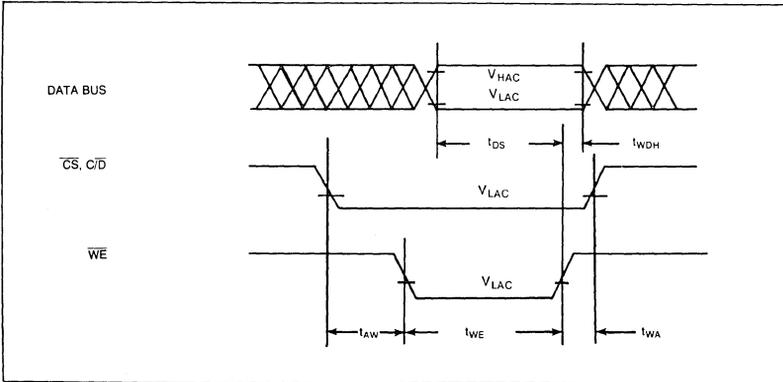


Figure 8 WD2123 WRITE TIMING

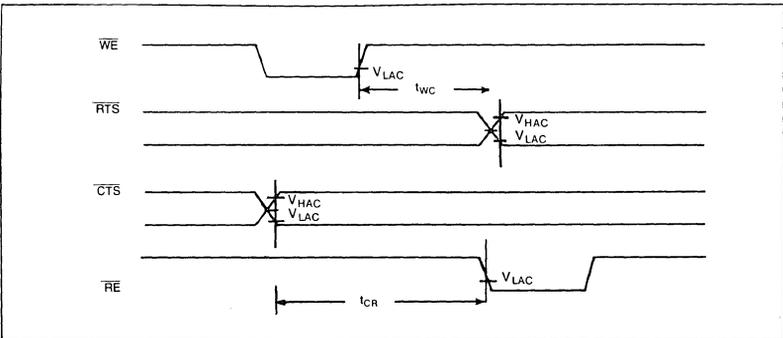


Figure 9 WD2123 INTERFACE CONTROL TIMING

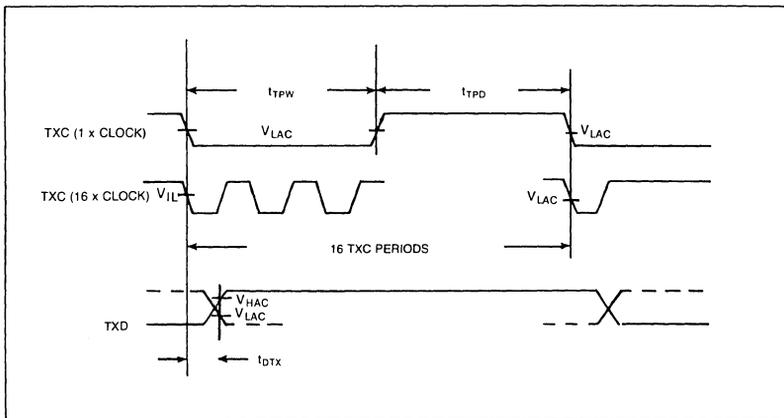


Figure 10 WD2123 TRANSMITTER CLOCK AND DATA TIMING

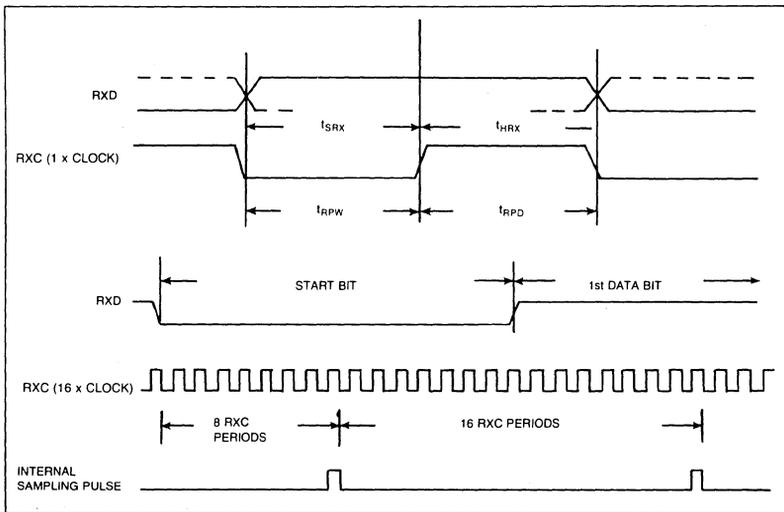


Figure 11 WD2123 RECEIVER CLOCK AND DATA TIMINGS

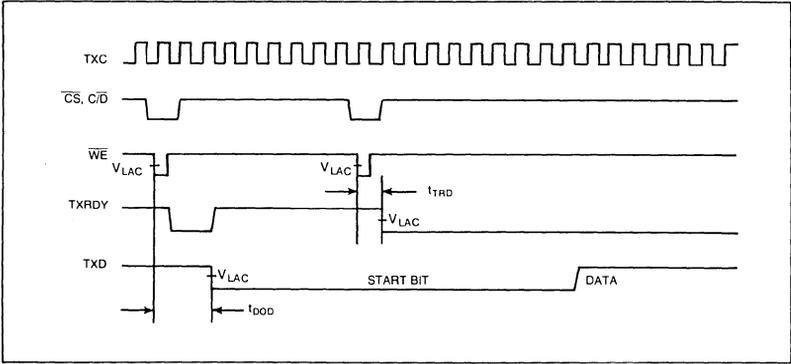


Figure 12 WD2123 TRANSMITTER OUTPUT TIMINGS WITH RESPECT TO TRANSMIT CLOCK

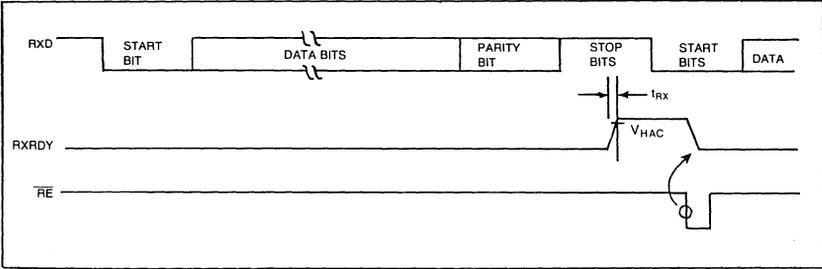


Figure 13 WD2123 RXRDY TIMING

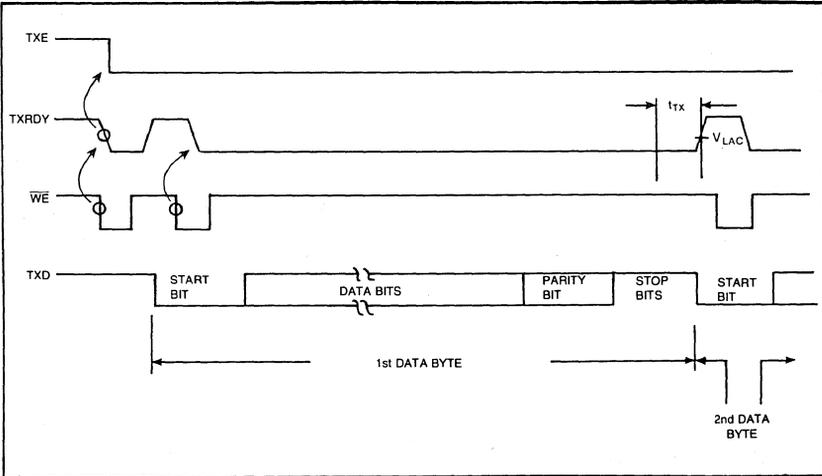
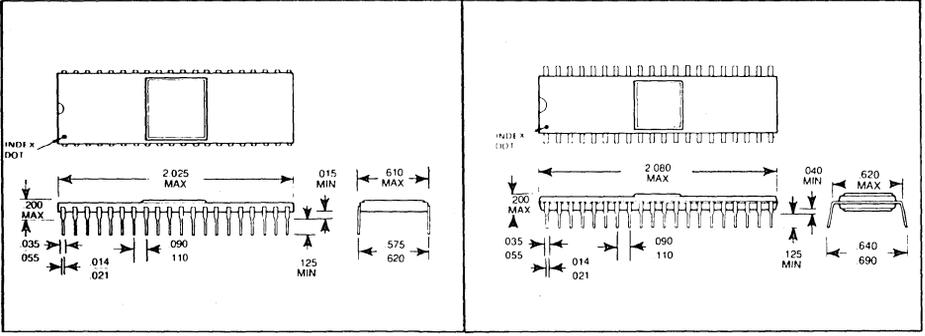


Figure 14 WD2123 TXRDY TIMING



WD2123A CERAMIC PACKAGE

WD2123B PLASTIC PACKAGE

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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WESTERN DIGITAL

C O R P O R A T I O N

WD1993 ARINC 429 RECEIVER/TRANSMITTER AND MULTI-CHARACTER RECEIVER/TRANSMITTER

SECTION
1

FEATURES

- PRESENT UPON MASTER RESET FOR ARINC 429 PROTOCOL
- PROGRAMMABLE WORD LENGTH FROM 1 CHARACTER TO 8 CHARACTERS
- PROGRAMMABLE CHARACTER LENGTH, 5, 6, 7, OR 8 BITS
- RETURN TO ZERO (RZ) OUTPUT
- AUTO SPACE GENERATION
- DOUBLE BUFFERED RECEIVER AND TRANSMITTER
- UNDERRUN ERROR DETECTION FOR TRANSMISSION
- OVERRUN, FRAMING AND PARITY ERROR DETECTION ON RECEIVER
- WORD ERROR FLAG FOR COMPREHENSIVE ERROR REPORTING
- FIRST CHARACTER OF WORD FLAG FOR SINGLE INTERRUPT APPLICATIONS
- DIAGNOSTIC LOCAL LOOP-BACK TEST MODE
- DC TO 200 KILOBITS PER SECOND OPERATION
- TTL COMPATIBLE INPUTS AND OUTPUTS

- SINGLE +5 VOLT SUPPLY
- 28 PIN CERAMIC OR PLASTIC PACKAGE
- TEMPERATURE RANGES 0°C to 70°C, -40°C to +85°C, or -55°C to +125°C

INTRODUCTION

The Western Digital WD1993 Avionic Receiver/Transmitter is designed to handle digital data transmission, according to the Avionic Arinc 429 protocol. Also, the word length is programmable from one to eight characters of 5, 6, 7, or 8 bits. Parallel data is converted into a serial data stream during transmission and serial to parallel during reception. The WD1993 is packaged in a 28 pin plastic or ceramic package and is available in three temperature ranges: Commercial, Industrial and Military.

GENERAL DESCRIPTION

The WD1993 is a bus-orientated MOS/LSI device designed to provide the Avionics Arinc 429 Data Communication Protocol, along with programmable character length capabilities.

Also, the WD1993 contains a local loop-back test mode of operation, which is controlled by the Loop Test Enable (LTE) bit in the command register. In this diagnostic mode, the transmitter output is "looped-back" into the receiver input. The REN and TEN control bits must also be active ("1") and the CTS input must be low. The status and output flags operate normally.

MARCH, 1981

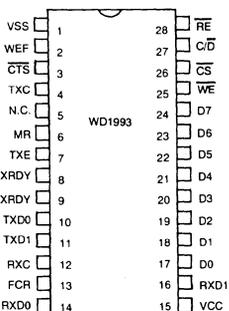


Figure 1 PIN DIAGRAM

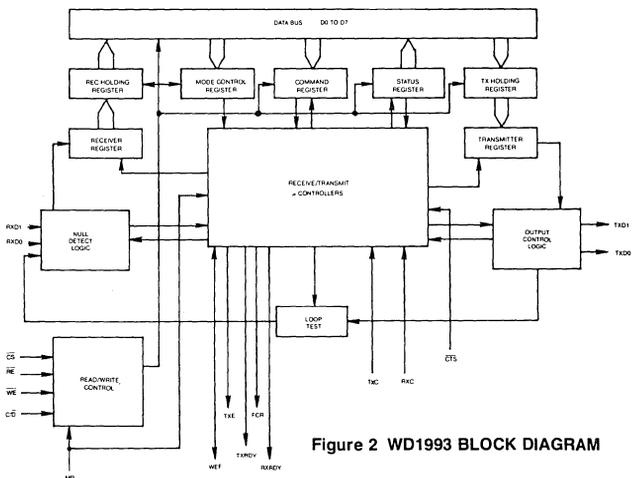


Figure 2 WD1993 BLOCK DIAGRAM

PIN NO.	SYMBOL	SIGNAL NAME	FUNCTION
1	VSS	GROUND	Ground
15	VCC	POWER SUPPLY	+5V DC
26	\overline{CS}	CHIP SELECT	When active (V_{IL}), the device is selected. This enables communication between the WD1993 and a micro-processor.
27	C/\overline{D}	CONTROL/DATA	This input is used in conjunction with an active read or write operation to determine register access via the DATA BUS.
28	\overline{RE}	READ ENABLE	When active (V_{IL}), allows the CPU to read data or status information from the WD1993.
25	\overline{WE}	WRITE ENABLE	When active (V_{IL}), allows the CPU to write into the selected register.
6	MR	MASTER RESET	When active (V_{IH}), presets the WD1993 mode and command registers to the ARINC protocol. Master Reset also resets the data registers and places the WD1993 transmitter and receiver into idle states. After MR, the command register is set to 00100101 and the mode register is set to 00111100.
4	TXC	TRANSMIT CLOCK	This input is the source clock for transmission. The data rate is a function of this clock frequency. ARINC MODE = 4 × bit rate
12	RXC	RECEIVE CLOCK	This input is the source clock for reception. The data rate characteristics are the same as the transmit clock.
3	\overline{CTS}	CLEAR-TO-SEND	This input is activated (V_{IL}) to enable the transmitter logic.
16	RXD1	RECEIVE DATA ONE	The RXD1 input is driven by the V/Z line receiver. Each time the V/Z circuit detects a logic one, a TTL level logic one (active for one-half bit time) is provided to this input.
14	RXD0	RECEIVE DATA ZERO	RXD0 is driven by the line V/Z receiver circuit. When the V/Z circuit detects a logic zero, a TTL logic one (active for one-half bit time) is provided to the WD1993.
11	TXD1	TRANSMIT DATA ONE	This output drives the V/Z circuit when a logic one is to be transmitted and is active for one-half bit time.
10	TXD0	TRANSMIT DATA ZERO	This output drives the V/Z circuit when a logic zero is to be transmitted and is active for one-half bit time.

PIN NO.	SYMBOL	SIGNAL NAME	FUNCTION
7	TXE	TRANSMITTER EMPTY	This output goes high to indicate the end of a transmit operation. TXE is automatically reset after the Transmit Holding Register is loaded.
8	RXRDY	RECEIVER READY	This output, when high, alerts the CPU that the Receiver Holding Register contains a data character that is ready to be input. This output is automatically reset whenever a character is read from the WD1993. RXRDY is enabled unless inhibited by setting command bit CR3 (RXRDYIN) to a logic "1". It is automatically enabled again after a receive sequence is completed.
9	TXRDY	TRANSMITTER READY	This output, when high, alerts the CPU that the Transmit Holding Register is ready to accept a data character. The TXRDY output is automatically reset whenever a character is written into the WD1993 and can be used as an interrupt to the system.
13	FCR	FIRST CHARACTER READY	This output goes high after the receiver has completed reception of the first character in a multi-character sequence.
2	WEF	WORD ERROR FLAG	This pin is an output, which when active indicates an error in either the transmitter or receiver has been detected. It reflects an underun, overrun, parity or framing (receive word) error and is intended as an error interrupt. The Status Register should be read to determine the specific error.
17 18 19 20 21 22 23 24	D0 D1 D2 D3 D4 D5 D6 D7	DATA BUS	This is the bi-directional data bus. It is the means of communication between the WD1993 and the CPU. Control, Mode, Data and Status Registers are accessed via this bus.
5	N.C.		No Internal Connection

ORGANIZATION

A block diagram of the WD1993 is shown in figure 2.

As mentioned, the WD1993 is an eight bit bus-oriented device. Communication between the WD1993 and the controlling CPU occurs via the 8 bit data bus through the bus transceivers. There are 2 accessible data registers, which buffer transmit and receive data. They are the Transmit Holding Register and the Receive Holding Register. There is a parallel-to-serial shift register (parallel in-serial out), the transmit register and a serial-to-parallel shift register (serial in-parallel out), the receive register.

Operational control and monitoring of the WD1993 is performed by two control registers (the command instruction register and the mode instruction register) and the status register.

A read/write control circuit allows programming/monitoring or loading/reading of data in the control, status or holding registers by activating the appropriate control lines: Chip Select (\overline{CS}), Read Enable (\overline{RE}), Write Enable (\overline{WE}), and Control or Data Select ($\overline{C/D}$).

Internal control of the WD1993 is by means of two internal microcontrollers; one for transmit and one for receive. The control registers, null detect logic and various counters, provide inputs to the microcontrollers which generate the necessary control signals to send and receive serial data according to the Arinc 429-1 protocol, along with the programmable multicharacter capabilities.

OPERATION

Upon master reset (\overline{MR}), the device is programmed to transmit and receive four 8-bit contiguous characters with the 32nd bit odd parity. (ARINC protocol.)

A minimum four bit time space is automatically inserted after the character transmission. Two receiver inputs, RXD1/RXD0 and two transmitter outputs, TXD1/TXD0, are provided to interface with voltage—impedance (V/Z) circuits to translate ± 10 volt ARINC line levels to 5 volt TTL logic levels. The transmit clock (TXC) and receive clock (RXC), in ARINC mode, are four times (4X) the bit rate desired.

The receiver monitors the received data input to detect a four bit time null, which delimits the word. If the communications link is broken during a word reception, the receiver will generate a word error flag to (WEF) to notify the CPU to request retransmission. When a null is detected, the receiver logic is reset and returned to an idle state awaiting the next word.

The WD1993 may also be programmed to support a multiple character word consisting of from one to eight characters. Also, the character length is programmable from 5 to 8 bits, and the parity bit if parity is used, may be either inside or outside the word.

The Command Register is used to select features such as parity options, loop test capability, RXRDY flag enabling, transmitter and receiver enabling, and may also cause the WD1993 to return to the Mode instruction.

The Mode Register is used to select features such as bits/character and characters/word.

The Status Register contains information such as Transmitter Ready, Transmitter Empty, Receiver Ready, error conditions, and First Character Ready.

OPERATING DESCRIPTION

The WD1993 is primarily designed to operate in an 8 bit micro-processor environment, although other control logic schemes are easily implemented. The DATA BUS and the Interface Control Signals (\overline{CS} , \overline{RE} , \overline{WE} and $\overline{C/D}$) should be connected to the microprocessor's data bus and system control bus.

The appropriate TXC and RXC clock frequencies should be selected for the particular application, using a programmable baud rate generator such as a BR1941. A master reset pulse initializes the WD1993 and presets the control registers to the ARINC protocol.

The RXD1/RXD0 inputs are interfaced to the DITS data line via external level translators that provide TTL (5V) logic levels to the WD1993. The TXD1/TXD0 outputs are connected to high voltage ($\pm 10V$) driver circuits. Figures 16 and 17 show some typical $\pm 10V$ translator and driver circuits.

The TXRDY, RXRDY, FCR and WEF Flags may be connected to the microprocessor system as interrupt inputs. The status register can be periodically read in a polled environment to support WD1993 operations.

The \overline{CTS} input can be used to synchronize the transmitter to external events.

The WD1993 is designed such that a control register write operation accesses the command instruction register.

The RXRDYIN bit of the command register is used to inhibit the RXRDY output pin for ARINC operations.

MULTI-CHARACTER OPERATIONS

As discussed above, the WD1993 is equipped with a multi-character option which provides the user with the means of transmitting and receiving multiple contiguous characters of data within one set of delimiters—4 bit nulls for ARINC 429. Since the WD1993 is an 8 bit bus-oriented device, the controlling processor must read the WD1993 data from its holding register before the subsequent characters are assembled. This situation also exists on the transmit side, i.e., the Transmit Holding Register must be loaded before the previous 8 bits are completely shifted out of the transmit register.

Several "flags" are provided for interrupt purposes so that continuity is maintained and data integrity is preserved. These flags are First Character Ready (FCR), Receiver Ready (RXRDY), Transmitter Ready (TXRDY) and Transmitter Empty (TXE).

The Transmitter operates as follows:

- a) With the mode and command registers programmed as desired, the transmitter is enabled, TEN (CR0) = "1".
- b) The TXE and TXRDY flags are "1" (active).
- c) The external $\overline{\text{CTS}}$ signal = "0".
- d) The CPU loads data into the Transmitter Holding Register, TXE and TXRDY go Low.

- e) The data is loaded into the transmit register and TXRDY goes high. This indicates the first data word is being sent and a character can be loaded into the holding register. If the WD1993 is programmed for more than one character (multi-character) then an underrun error will be generated if the next character is not loaded before the previous word is completely shifted out, unless the current character is the last character in a sequence.
- f) If the last character is transmitted and no more new data is to be sent, the transmitter will indicate its status by raising the TXE flag. (No error is generated as a result of this condition.)

The Receiver operates similarly:

- a) With the control registers suitably programmed, the receiver is enabled, REN (CR2) = "1".
- b) The RXRDY and FCR flags are "0". (Inactive).
- c) The incoming data word activates the receive logic and the data begins to be assembled in the receive register.
- d) When the first character is completely assembled, the data is loaded into the Receive Holding Register, the FCR (First Character Ready) and RXRDY (Receiver Ready) flags become active, "1". The CPU should read the data prior to the reception of the next character or an overrun error will be generated as the receiver will overwrite the old data with the new data character just received.

The exception to this is in the ARINC mode, where the first character in the ARINC protocol contains a label. The FCR and RXRDY Flags become active to indicate the reception of the first character of data. The CPU reads the first character and decides whether or not it wants to acquire the subsequent characters. If not, then the CPU performs a "control write" to the COMMAND REGISTER, setting the RXRDYIN (CR3) bit to a "1". This bit in ARINC mode, inhibits the RXRDY flag from interrupting the CPU during the reception of the 3 remaining characters. The RXRDYIN bit is then automatically reset upon completion of the receive sequence and RXRDY is enabled again.

LOOP TEST MODE

As mentioned, the WD1993 is equipped with a diagnostic test mode, local loop-back. This mode is activated by setting the LTE command bit to a "1". The TEN and REN bits should be "1" and CTS should be "V_{IL}". The receiver inputs are ignored and the transmitter outputs are sending nulls. The transmitter is internally "looped-back" to the receiver and the error and status flags operate normally.

For basic testing, failing to reload the Transmit Holding Register in the middle of a data send sequence will cause an underrun error in the transmitter and a word error in the receiver. Failure to read the Receive Holding Register after a FCR or RXRDY flag will cause an overrun error to be generated.

For Loop-Back test operations, the user should be sure that the TXC and RXC clock frequencies are the same. This is normally implemented by placing the same clock signal on both pins (TXC and RXC).

ARINC BACKGROUND

Aeronautical Radio Inc. (ARINC) publishes the ARINC 429 specification. This document defines the air transport industries standards for the transfer of digital data between avionics systems elements. This specification was adopted by The

Airlines Electronic Engineering Committee April 11, 1978. By the adoption of this specification the foundation is set for a standard protocol governing all intersystems equipment (Line Replaceable Units).

MARK 33 DIGITAL INFORMATION TRANSFER SYSTEM (DITS)

Basic Philosophy

Transmit from a designated output port over a single twisted and shielded pair of wires to designated receiver.

Bidirectional data flow not permitted on a given pair.

Data Transfer

- Numeric
- Iso Alphabet #5
- Graphic

Data Format

32 bits or less (unused bit positions should be filled with binary zeros or valid data pad bits).

Bit #32 is assigned to parity.

Modulation

Return to Zero (RZ)

Transmit Voltage Levels

high	+10	±0.5V
null	0	±0.5V
low	-10	±0.5V

Receiver Voltage Levels:

	(in absence of noise)	(noisy environment)
high	+6.0V to +10V	+5.0V to +13V
low	-6.0V to +10V	-5.0V to -13V

No damage to receiver up to 20 vac rms between A & B; +28, A to Gnd; -28, B to Gnd.

Data Rate

100 kilo bit per second ± 1%

Low speed 12 to 14.5 kilo bit per second ± 1%

Word Synchronization

All zero gap of a minimum of 4 bit times

The format and definition of the Mode Register is shown below:

MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
X	N3	N2	N1	CLS2	CLS1	X	X

<u>CLS2</u>	<u>CLS1</u>	<u>Character Length Select</u>	
0	0	5 bits	
0	1	6 bits	
1	0	7 bits	
1	1	8 bits	
<u>N3</u>	<u>N2</u>	<u>N1</u>	<u>Characters Per Word Select</u>
0	0	0	1 character
0	0	1	2 characters
0	1	0	3 characters
0	1	1	4 characters
1	0	0	5 characters
1	0	1	6 characters
1	1	0	7 characters
1	1	1	8 characters

The WD1993 registers are addressed according to the following table:

\overline{CS}	C/\overline{D}	\overline{RE}	\overline{WE}	<u>Registers Selected</u>
L	L	L	H	Read Receive Holding Register
L	L	H	L	Write Transmit Holding Register
L	H	L	H	Read Status Register
L	H	H	L	Write Control Registers
H	X	X	X	Data Bus Tri-Stated

L = V_{IL} at pins
H = V_{IH} at pins
X = don't care

The format of the Status Register is shown below:

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
UE	FCR	WEF	OE	PE	TXE	RXRDY	TXRDY

<u>TXRDY</u>	<u>Transmitter Ready</u>
1	Active (THR can be reloaded)
0	Inactive (transmitter is busy)
<u>RXRDY</u>	<u>Receiver Ready</u>
1	Active (RHR should be read)
0	Inactive
<u>TXE</u>	<u>Transmitter Empty</u>
1	Transmitter idle
0	Transmitter active
<u>PE</u>	<u>Parity Error</u>
1	Error reported
0	No error
<u>OE</u>	<u>Overrun Error</u>
1	RHR has been overwritten
0	No error
<u>WEF</u>	<u>Word Error Flag</u>
1	Indicates improper receive sequence (word error), overrun error, parity error or underrun error.
0	No error
<u>FCR</u>	<u>First Character Ready</u>
1	This bit indicates the receiver has just completed assembly of the 1st character in a multi-character sequence and that the data is contained in the RHR.
0	First character not ready.
<u>UE</u>	<u>Underrun Error</u>
1	Indicates that the THR has not been loaded with a new character in time for a contiguous data transmission sequence.
0	No error

ABSOLUTE MAXIMUM RATINGS

Storage Temperature -55°C to +125°C (Plastic Package)
 -65°C to +150°C (Ceramic Package)

Voltage on any Pin with Respect to Ground .. -0.3V to +7V

Power Dissipation 400 MW

Note: Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Electrical Characteristics.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = 5.0V ± 5%; GND = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
V _{IL}	Input Low Voltage	-0.3		0.8	V	
V _{IH}	Input High Voltage	2.0		V _{CC}	V	
V _{OL}	Output Low Voltage			0.45	V	I _{OL} = 1.6mA
V _{OH}	Output High Voltage	2.4			V	I _{OH} = -100µA
I _{DL}	Data Bus Leakage			50	µA	Data Bus is in High Impedance State
I _{IL}	Input Leakage			10	µA	V _{IN} = V _{CC}
I _{CC}	Power Supply Current		45	80	mA	V _{CC} = 5.25V No Load

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C _{IN}	Input Capacitance			10	pF	f _C = 1MHz
C _{I/O}	I/O Capacitance			20	pF	Unmeasured pins returned to GND

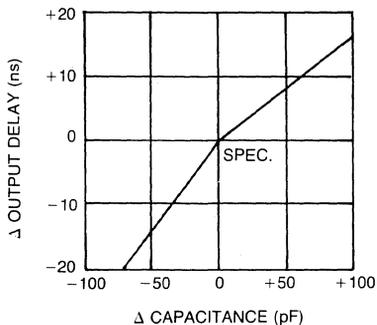


Figure 3 OUTPUT DELAY vs CAPACITANCE

A.C. TIMING PARAMETERS

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
BUS PARAMETERS					
Read Cycle (Reference Figure 6)					
t_{AR}	Address Stable before \overline{RE} , (\overline{CS} , C/D)	50		ns	
t_{RA}	Address Hold Time for \overline{RE} , (\overline{CS} , C/D)	5		ns	
t_{RE}	\overline{RE} Pulse Width	350		ns	
t_{RD}	Data Delay from \overline{RE}		200	ns	$C_L = 50\text{ pF}$
t_{RDH}	\overline{RE} to Data Floating		200	ns	$C_L = 50\text{ pF}$
		25		ns	$C_L = 15\text{ pF}$

WRITE CYCLE (Reference Figure 7)					
t_{AW}	Address Stable before \overline{WE}	20		ns	
t_{WA}	Address Hold Time for \overline{WE}	20		ns	
t_{WE}	\overline{WE} Pulse Width	350		ns	
t_{DS}	Data Set-Up Time for \overline{WE}	200		ns	
t_{WDH}	Data Hold Time for \overline{WE}	40		ns	

OTHER TIMINGS (Reference Figures 8, 9)					
t_{DTX}	TXD Delay from Falling Edge of TXC		500	ns	$C_L = 100\text{ pF}$
t_{SRX}	Rx Data Set-up Time to Sampling Pulse	200		ns	$C_L = 100\text{ pF}$
t_{NRX}	Rx Data Hold Time to Sampling Pulse	100		ns	$C_L = 100\text{ pF}$
t_{TX}	Transmitter Input Clock Frequency				
	1 × Baud Rate	DC	500	kHz	
	4 ×, 16 × Baud Rate	DC	750	kHz	
t_{TPW}	Transmitter Input Clock Pulse Width				
	1 × Baud Rate	1.0		us	
	16 × Baud Rate	500		ns	
t_{TPD}	Transmitter Input Clock Pulse Delay				
	1 × Baud Rate	1.0		us	
	16 × Baud Rate	500		ns	
t_{RX}	Receiver Input Clock Frequency				
	1 × Baud Rate	DC	500	kHz	
	4 ×, 16 × Baud Rate	DC	750	kHz	
t_{RPW}	Receiver Input Clock Pulse Width				
	1 × Baud Rate	1.0		us	
	16 × Baud Rate	500		ns	
t_{RPD}	Receiver Input Clock Pulse Delay				
	1 × Baud Rate	1.0		us	
	16 × Baud Rate	500		ns	
t_{TX}	TXRDY Delay from center of Data Bit		½	t_{TXC}	(1x or 16x)

A.C. TIMING PARAMETERS

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
t_{TX}	TXRDY Delay from Center of Data Bit	200 ns	2	t_{TXC}	(4x)
t_{RX}	RXRDY Delay from Center of Data Bit (FCR Delay from Center of Data Bit)		$\frac{1}{2}$	R_{RXC}	
	TXE Delay from Center of Data Bit		$\frac{1}{2}$	t_{TXC}	$C_L = 50 \text{ pF}$ (1 × Rate)

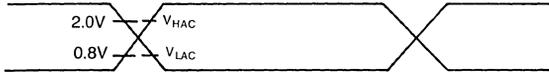


Figure 4 TEST POINTS FOR A.C. TIMING

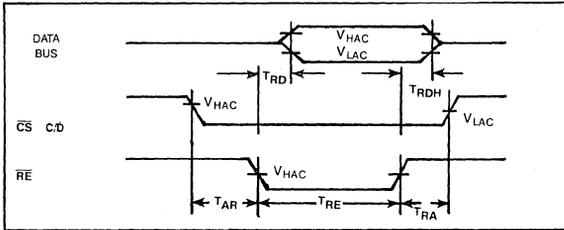


Figure 5 READ CYCLE TIMING

Note: AC timings measured at $V_{OH} = 2.0V$, $V_{OL} = 0.8V$ and with test load circuit.

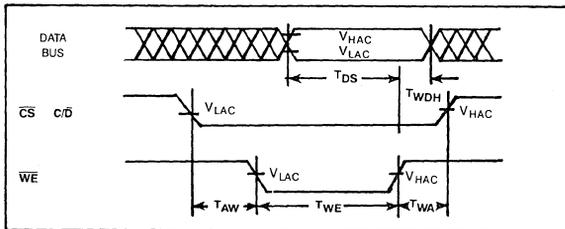


Figure 6 WRITE CYCLE TIMING

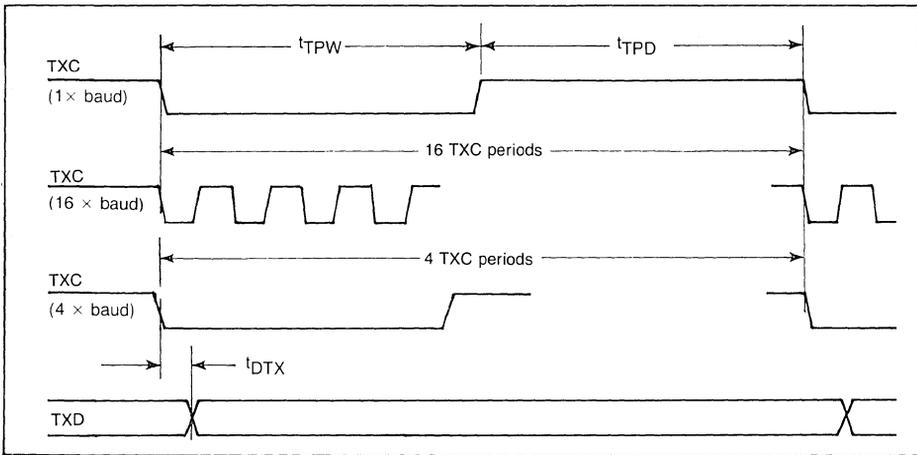


Figure 7 TRANSMITTER CLOCK AND DATA TIMINGS

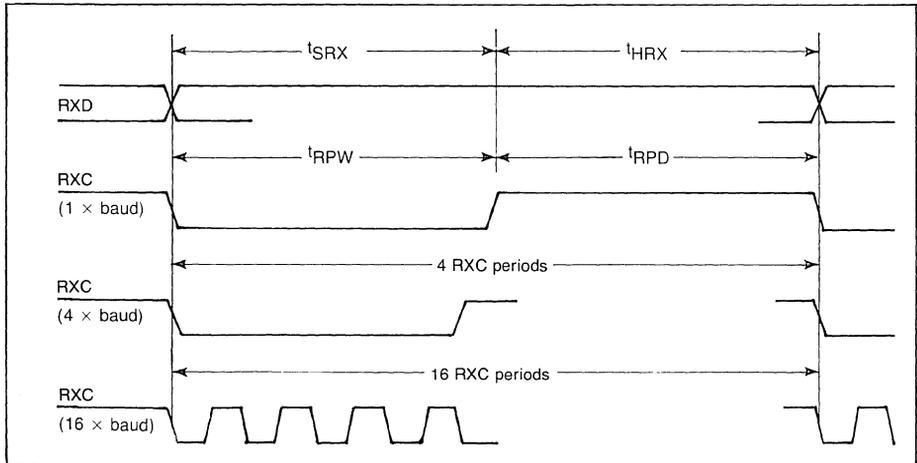


Figure 8 RECEIVER CLOCK AND DATA TIMINGS

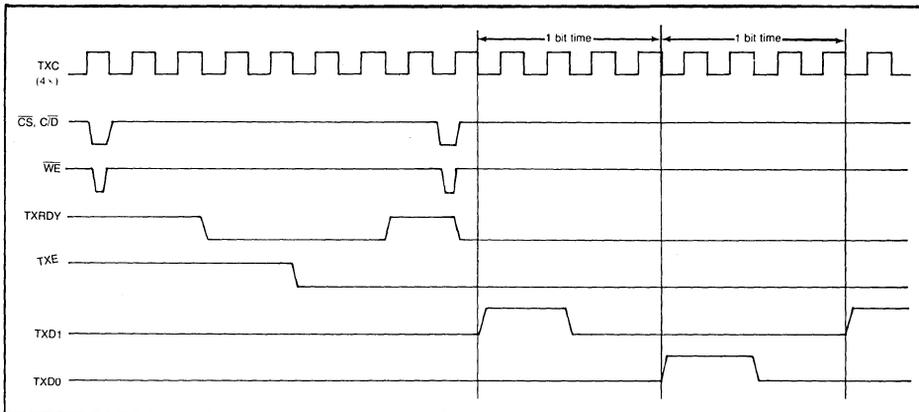


Figure 9 TRANSMITTER TIMINGS (ARINC MODE)

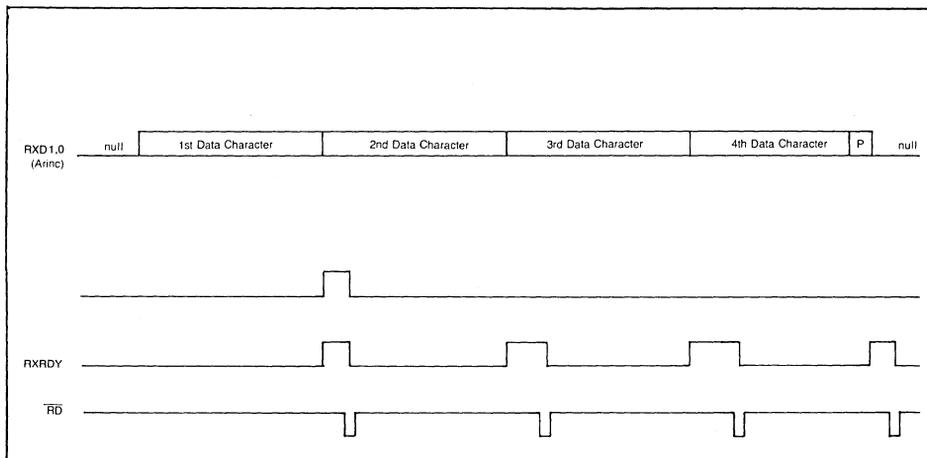


Figure 10 RXRDY AND FCR TIMING

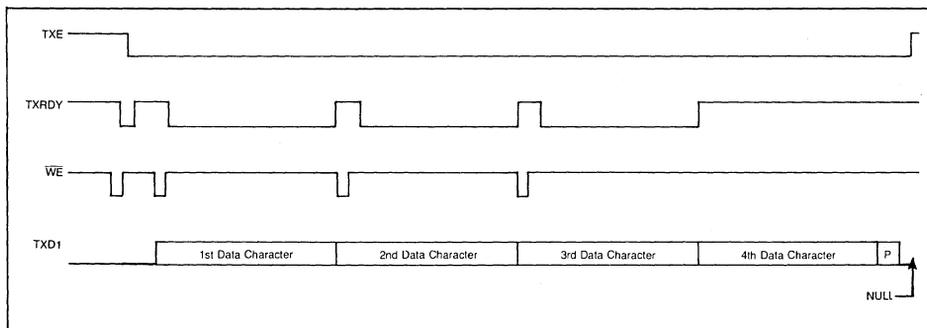


Figure 11 TXRDY AND TXE TIMINGS (4 Character Sequence)

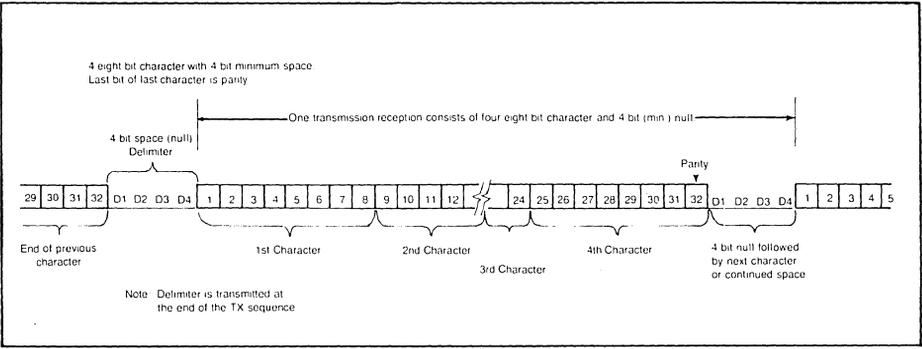


Figure 12 ARINC 429

The V/Z Receiver converts ± 10 volt levels to TTL logic levels. It is composed of logic one and zero comparators. A logic one (RXD1) TTL output is derived when voltage rising to 1 (VR1) threshold is crossed and terminated at voltage falling to 1 (VF1). A logic zero (RXD0) TTL output is generated between voltage falling to zero (VFO) and voltage rising from zero (VRO). When input thresholds are not exceeded, neither output is active. The V/Z output can drive one TTL input.

The return to zero (RZ) format is shown below

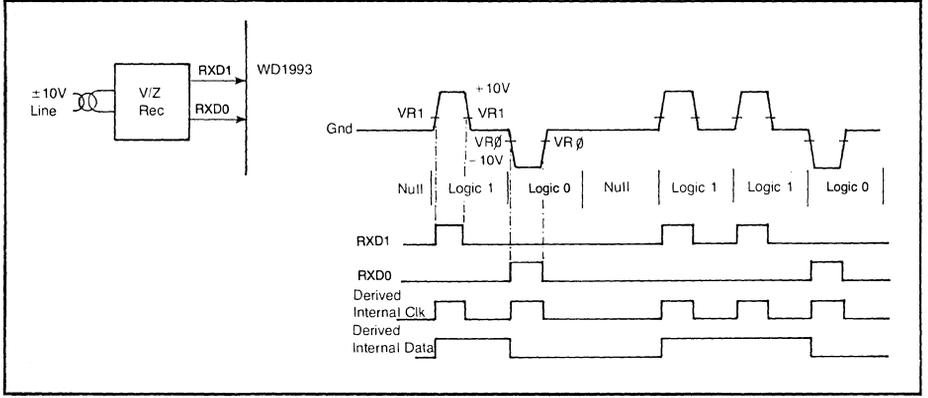


Figure 13 ARINC RECEIVER CIRCUIT

The V/Z Driver convert TTL logic levels into ± 10 volt levels. The TXD1 and TXD0 outputs of the WD1993 are used to drive the line drivers. Each output can drive one TTL load. When the outputs are not active, the line Driver should return to zero.

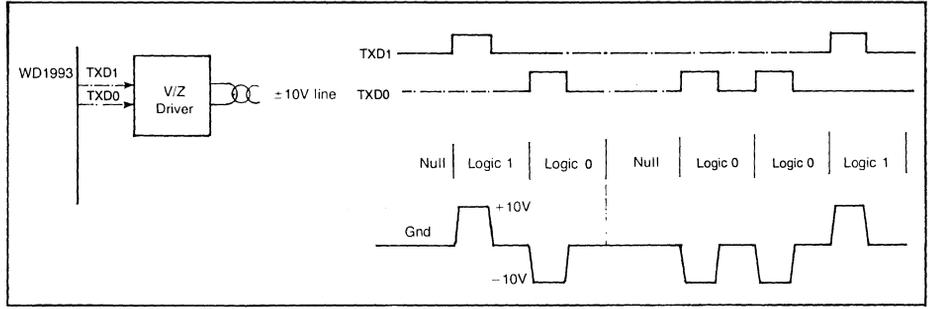


Figure 14 ARINC DRIVER CIRCUIT

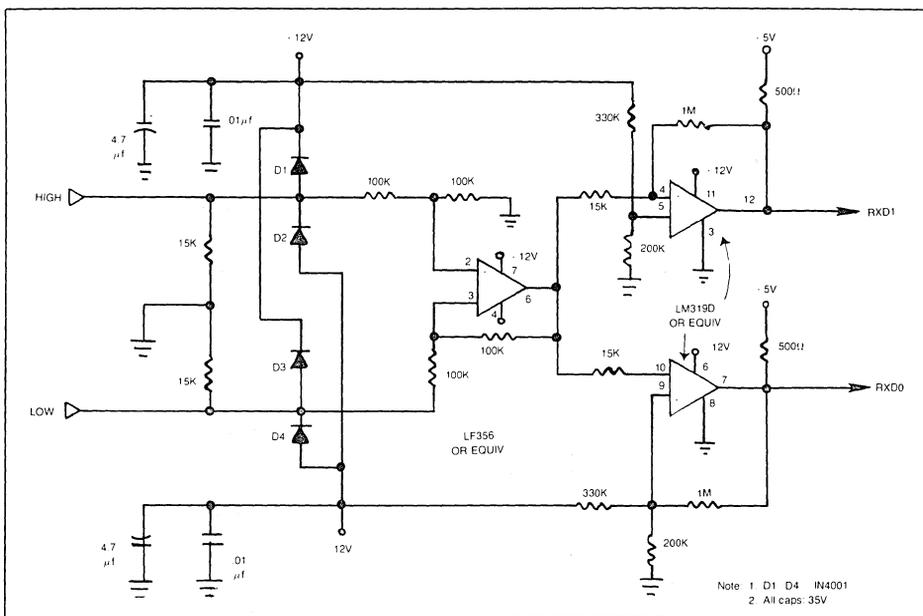


Figure 15 ARINC 429 LINE LEVEL TRANSLATOR (RECEIVER)

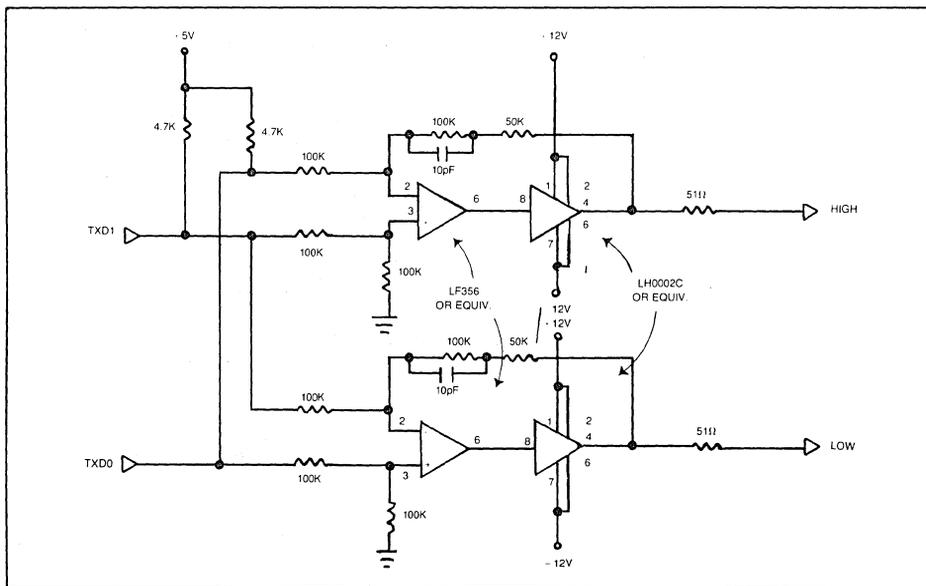
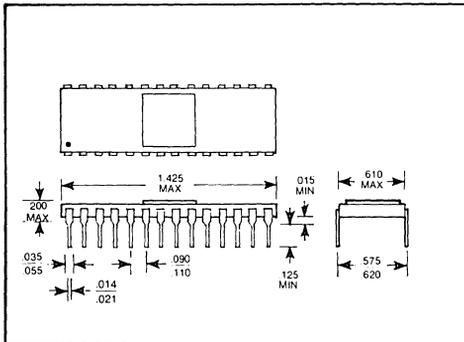
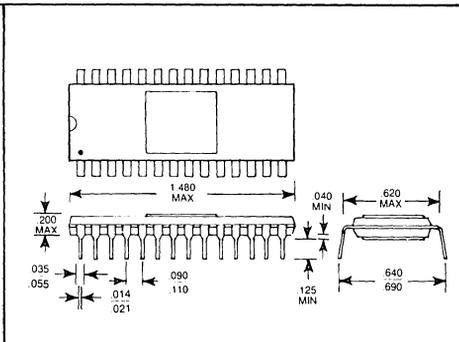


Figure 16 ARINC 429-1 LINE DRIVER



WD1993E CERAMIC PACKAGE



WD1993F PLASTIC PACKAGE

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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WESTERN DIGITAL CORPORATION

WD1984 MULTI-CHARACTER SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER

SECTION 1

MARCH, 1981

FEATURES

- TWO OPERATING MODES: SYNCHRONOUS & ASYNCHRONOUS
- 1 TO 8 CHARACTERS OF 5, 6, 7, OR 8 BITS PER CHARACTER TRANSMISSION
- SELECTABLE PARITY INSERTION IN OR AFTER LAST BIT OF WORD
- EVEN/ODD PARITY SELECT OR NO PARITY
- DOUBLE BUFFERED RECEIVER & TRANSMITTER
- ASYNCHRONOUS SELECTABLE CLOCK RATES (1x,16x)
- UNDERRUN ERROR DETECTION FOR TRANSMISSION
- OVERRUN, FRAMING AND PARITY ERROR DETECTION ON RECEIVER
- LINE BREAK GENERATION AND DETECTION (ASYNC MODE)
- FIRST CHARACTER OF WORD FLAG FOR SINGLE INTERRUPT APPLICATIONS

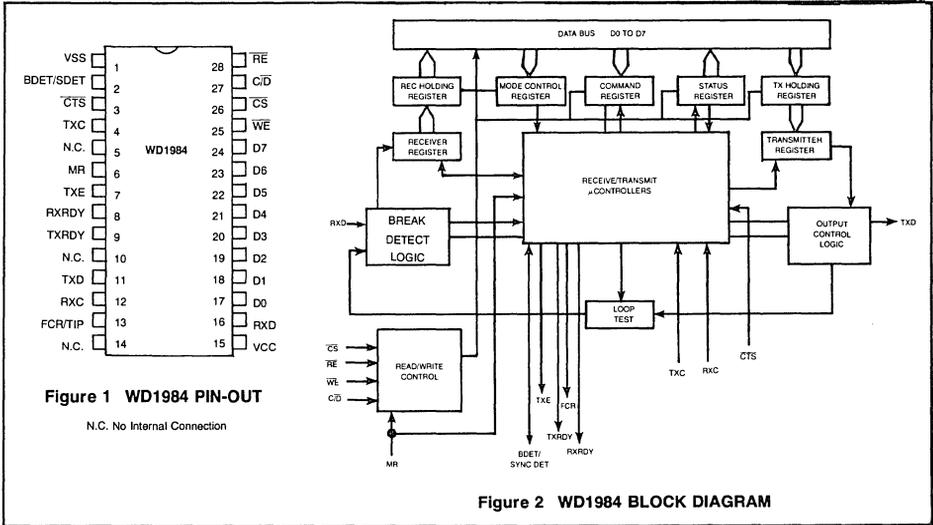
- DIAGNOSTIC LOCAL LOOP-BACK TEST MODE

- DC TO 1M BITS/SEC (1x) OPERATION
- TTL COMPATIBLE INPUTS AND OUTPUTS
- SINGLE +5 VOLT SUPPLY
- 28 PIN CERAMIC OR PLASTIC PACKAGE
- TEMPERATURE RANGES 0°C to 70°C, -40°C TO +85°C

INTRODUCTION

The Western Digital WD1984 is designed to handle digital data transmission, according to two protocols. These are the Synchronous and Asynchronous protocols. Parallel data is converted into a serial data stream during transmission and serial to parallel during reception.

The device can be programmed to transmit and receive words that are 1 to 8 characters in length; 5, 6, 7 or 8 bits per character. Error flags and control signals have been provided to broaden the application range of the device. The WD1984 is packaged in a 28 pin plastic or ceramic package and is available in two temperature ranges: Commercial and Industrial.



PIN NO.	SYMBOL	SIGNAL NAME	FUNCTION
1	VSS	GROUND	Ground
2	BDET/ SDET	BREAK DETECT/ SYNC DETECT	This pin is a bi-directional port. In ASYNC, it is an output, which goes high when the receiver logic detects a break character. In the SYNC mode, it is an input which causes the receiver to begin assembling data bytes as programmed.
3	$\overline{\text{CTS}}$	CLEAR-TO-SEND	This input is activated (V_{IL}) to enable the transmitter logic.
4	TXC	TRANSMIT CLOCK	This input is the source clock for transmission. The data rate is a function of this clock frequency. ASYNC MODE = $1 \times$ or $16 \times$ bit rate SYNC MODE = $16 \times$ bit rate
5	N.C.		No internal connection.
6	MR	MASTER RESET	When high (V_{IH}), presets the WD1984. The command register is set to 00100101 and the mode register is set to 00111100.
7	TXE	TRANSMITTER EMPTY	This output goes high to indicate the end of a transmit operation. TXE is automatically reset after the Transmit Holding Register is loaded.
8	RXRDY	RECEIVER READY	This output, when high, alerts the CPU that the Receiver Holding Register contains a data character that is ready to be input. This output is automatically reset whenever a character is read from the WD1984.
9	TXRDY	TRANSMITTER READY	This output, when high, alerts the CPU that the Transmit Holding Register is ready to accept a data character. The TXRDY output is automatically reset whenever a character is written into the WD1984 and can be used as an interrupt to the system.

PIN NO.	SYMBOL	SIGNAL NAME	FUNCTION
10	N.C.		
11	TXD	TRANSMIT DATA ONE	This output is the serial data output.
12	RXC	RECEIVE CLOCK	This input is the source clock for reception. The data rate characteristics are the same as the transmit clock.
13	FCR/TIP	FIRST CHARACTER READY/TRANSMISSION IN PROGRESS	In the ASYNC mode, this output goes high after the receiver has completed reception of the first character in a multi-character sequence.
14	N.C.		
15	VCC	POWER SUPPLY	+5V DC
16	RXD	RECEIVE DATA ONE	This input is the serial data input.
17	D0	DATA BUS	This is the bi-directional data bus. It is the means of communication between the WD1984 and the CPU. Control, Mode, Data and Status Registers are accessed via this bus.
18	D1		
19	D2		
20	D3		
21	D4		
22	D5		
23	D6		
24	D7		
25	\overline{WE}	WRITE ENABLE	When low (V_{IL}), allows the CPU to write into the selected register.
26	\overline{CS}	CHIP SELECT	When low (V_{IL}), the device is selected. This enables communication between the WD1984 and a microprocessor.
27	C/\overline{D}	CONTROL/DATA	This input is used in conjunction with an active read or write operation to determine register access via the DATA BUS.
28	\overline{RE}	READ ENABLE	When low (V_{IL}), allows the CPU to read data or status information from the WD1984.

GENERAL DESCRIPTION

The WD1984 is a bus-oriented MOS/LSI device designed to provide two data communication protocols:

1. Asynchronous
2. Synchronous

The control registers are used to select the desired protocol and provide programmable format options within each protocol, as outlined below.

The WD1984 contains two control registers needed to specify format options within each protocol. These registers are the command instruction register and the mode instruction register.

The format options available to the user are:

- 1) Parity Enable (PEN)
- 2) Parity Position (PIA)
The Parity bit (when enabled) can either be appended to the data word after the data bits or it can be inside the data word in the last bit position.
- 3) Odd or Even Parity Select (EPS)
- 4) Character Length Select 5, 6, 7 or 8 Bits/Character (CLS2 and CLS2)

The Asynchronous mode has the option of selecting the number of contiguous characters per transmission and receive sequence. This multicharacter option may facilitate data handling between peripheral devices with a non-standard number of data bits. Therefore, the user can change the mode register to transmit and receive any combination of one to eight characters per word and 5, 6, 7 or 8 bits per character.

Additionally, the Asynchronous mode has two options which determine the operational characteristics of the protocol:

- 1) Stop Bit Selection—(SPS)
This control bit selects 1 or 2 stop bits (1 or 1½ bits in 5 bit characters) at the end of the word, which is part of the character delimiting definition.

- 2) Asynchronous clock rate select (1× or 16× clock rate), which describes resolution and bit rate characteristics.

The WD1984 also contains a local loop-back test mode of operation, which is controlled by the Loop Test Enable (LTE) bit in the command register. In this diagnostic mode, the transmitter output is "looped-back" into the receiver input. The REN and TEN control bits must also be active ("1") and the CTS input must be low ("0"). The status and output flags operate normally.

ORGANIZATION

A block diagram of the WD1984 is shown in figure 1.

As mentioned, the WD1984 is an eight bit bus-oriented device. Communication between the WD1984 and the controlling CPU occurs via the 8 bit data bus through the bus transceivers. There are 2 accessible data registers, which buffer transmit and receive data. They are the Transmit Holding Register and the Receive Holding Register. There is a parallel-to-serial shift register (parallel in-serial out), the transmit register and a serial-to-parallel shift register (serial in-parallel out), the receive register.

Operational control and monitoring of the WD1984 is performed by two control registers (the command instruction register and the mode instruction register) and the status register.

A read/write control circuit allows programming/monitoring or loading/reading of data in the control, status or holding registers by activating the appropriate control lines: Chip Select (\overline{CS}), Read Enable (\overline{RE}), Write Enable (\overline{WE}) and Control or Data Select ($\overline{C/D}$).

Internal control of the WD1984 is by means of two internal microcontrollers; one for transmit and one for receive. The control registers, null detect logic and various counters, provide inputs to the microcontrollers which generate the necessary control signals to send and receive serial data according to the programmed protocols.

REGISTER DEFINITIONS

The format and definition of the Command Register is shown below:

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
EPS	IR	PEN	LTE	TXSM	REN	PIA	TEN

TEN

1
0

Transmit ENable

Enabled
Disabled

PIA

1
0

Parity Inside or After

After the data word
Inside (the last data bit) of word

REN

1
0

Receive ENable

Enabled
Disabled

TXSM

1
0

Transmit Space or Mark

Send break character (force TXD low)
Normal transmitter operation

LTE

1
0

Loop Test ENable

Local loop-back mode
Normal Operation

PEN

1
0

Parity ENable

Enabled
Disabled

IR

1
0

Internal Reset

Returns WD1984 to mode instruction format

EPS

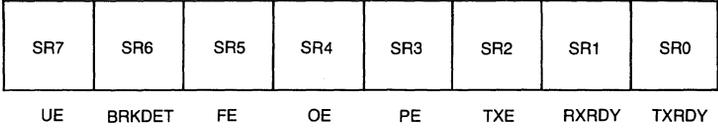
1
0

Even Parity Select

Even parity
Odd parity

*Internally disabled in Synchronous mode.

The format of the Status Register is shown below:



<u>TXRDY</u>		<u>Transmitter Ready</u>
1		Active (THR can be reloaded)
0		Inactive (transmitter is busy)
<u>RXRDY</u>		<u>Receiver Ready</u>
1		Active (RHR should be read)
0		Inactive
<u>TXE</u>		<u>Transmitter Empty</u>
1		Transmitter idle
0		Transmitter active
<u>PE</u>		<u>Parity Error</u>
1		Error reported
0		No error
<u>OE</u>		<u>Overrun Error</u>
1		RHR has been overwritten
0		No error
<u>FE</u>		<u>Framing Error</u>
1		Indicates a framing error has been detected.
0		No error
<u>BRKDET</u>		<u>Break Character Detect</u>
1		In ASYNC mode, this bit indicates the receiver has detected a break character.
0		Inactive
<u>UE</u>		<u>Underrun Error</u>
1		In multi-character transmissions, indicates that the THR has not been loaded with a new character in time for a contiguous data transmission sequence.
0		No error

The format and definition of the Mode Register is shown below:

MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
SBS	N3	N2	N1	CLS2	CLS1	MS2	MS1

<u>MS2</u>	<u>MS1</u>	<u>Mode Selected</u>
X	X	Undefined
0	0	Asynchronous mode (16X)
0	1	Asynchronous mode (1X)
1	X	Synchronous mode (16X)

<u>CLS2</u>	<u>CLS1</u>	<u>Character Length Select</u>
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

<u>N3</u>	<u>N2</u>	<u>N1</u>	<u>Characters Per Word Select</u>
0	0	0	1 character
0	0	1	2 characters
0	1	0	3 characters
0	1	1	4 characters
1	0	0	5 characters
1	0	1	6 characters
1	1	0	7 characters
1	1	1	8 characters

<u>SBS</u>	<u>Stop Bit Select</u>
1	2 stop bits (1-1/2 bits in 5 bit characters)
0	1 stop bit

The WD1984 registers are addressed according to the following table:

<u>CS</u>	<u>C/D</u>	<u>RE</u>	<u>WE</u>	<u>Registers Selected</u>
L	L	L	H	Read Receive Holding Register
L	L	H	L	Write Transmit Holding Register
L	H	L	H	Read Status Register
L	H	H	L	Write Control Registers
H	X	X	X	Data Bus Tri-States

L = V_{IL} at pins
H = V_{IH} at pins
X = don't care

A.C. TIMING PARAMETERS

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
t_{RX}	RxRDY Delay from Center of Data Bit (FCR Delay from Center of Data Bit)		1/2	R_{RXC}	$C_L = 50 \text{ pF}$ (1 × Rate)
	Internal BRKDET Delay from Center of Data Bit		1	t_{RXC}	
	External SynDet Set-up time before rising edge of RXC	200		ns	
	TXEMPTY Delay from Center of Data Bit		1/2	t_{TXC}	

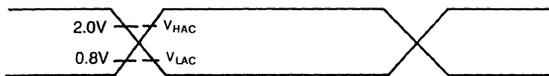


Figure 4 TEST POINTS FOR A.C. TIMING

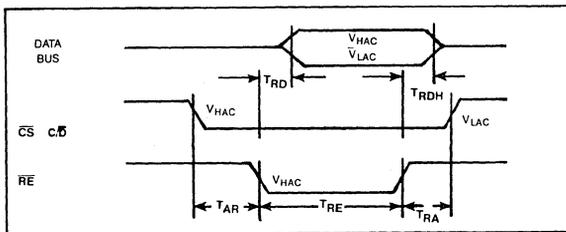


Figure 5 READ CYCLE TIMING

Note: AC timings measured at $V_{OH} = 2.0V$, $V_{OL} = 0.8V$

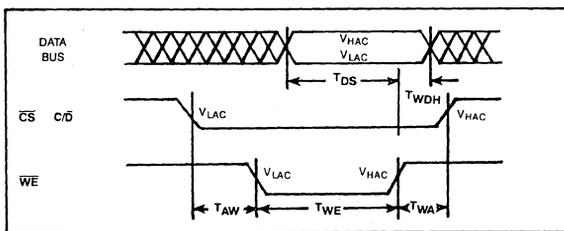


Figure 6 WRITE CYCLE TIMING

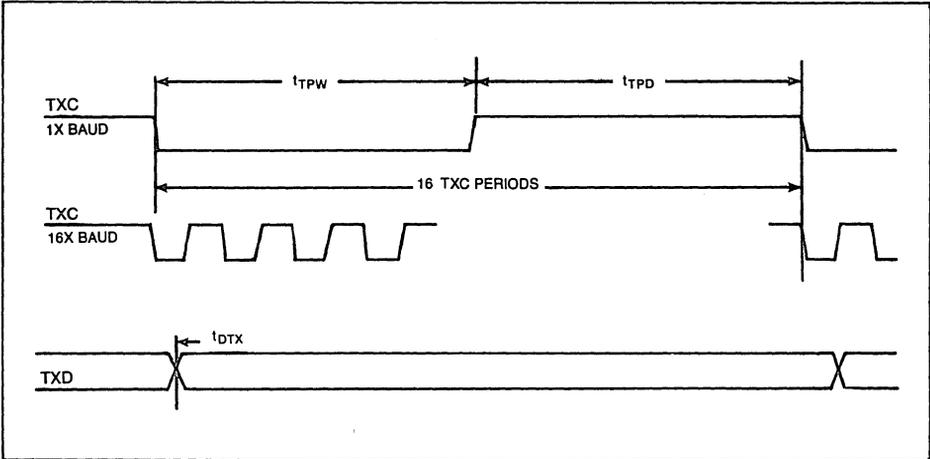


Figure 7 TRANSMITTER CLOCK AND DATA TIMINGS

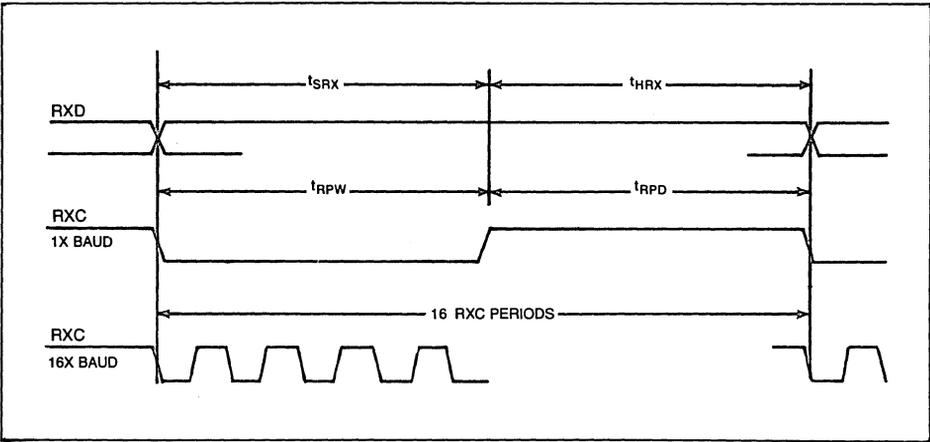


Figure 8 RECEIVER CLOCK AND DATA TIMINGS

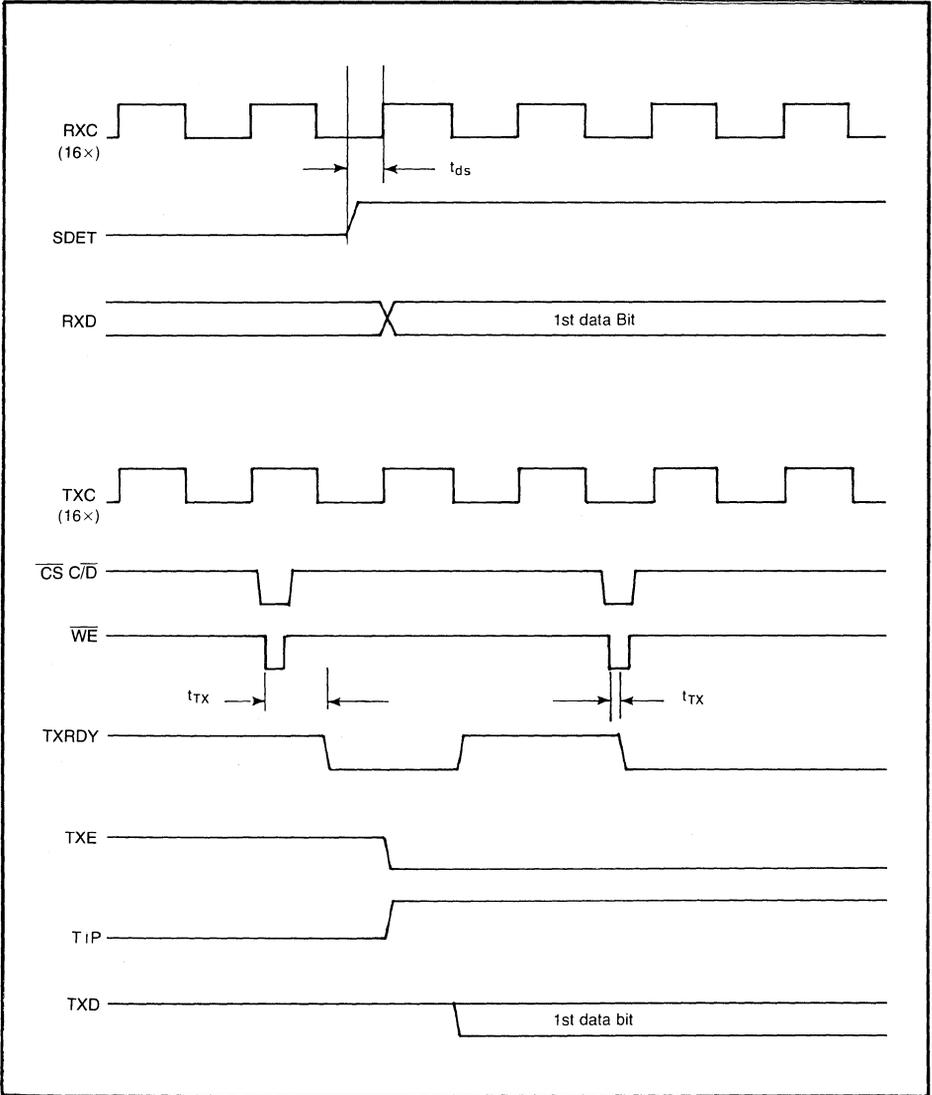


Figure 9 SYNCHRONOUS MODE TIMINGS

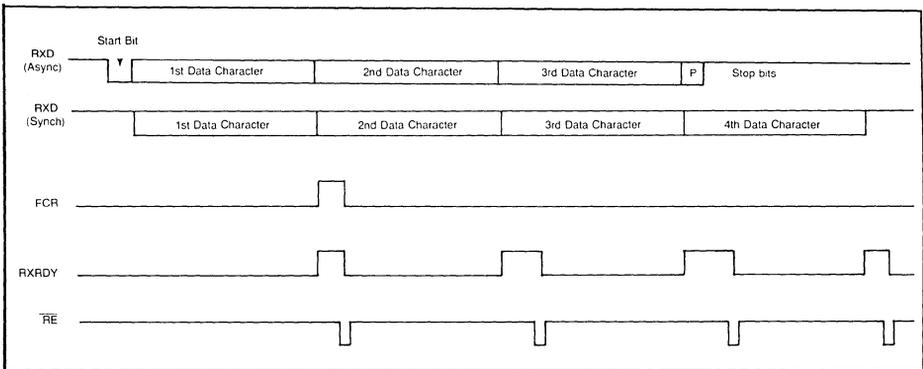


Figure 10 RXRDY AND FCR TIMING

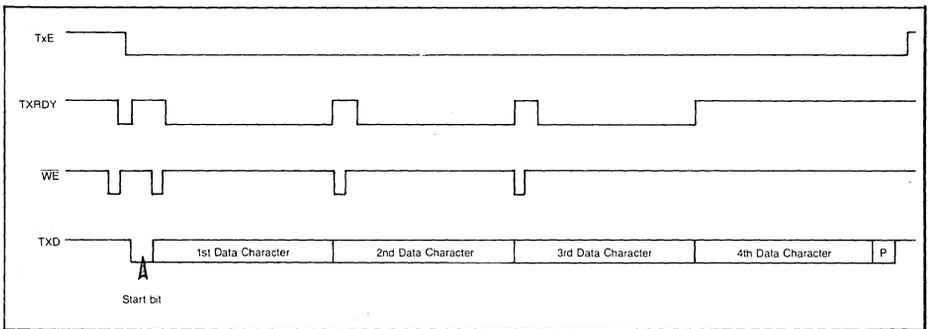


Figure 11 TXRDY AND TXE TIMINGS (4 CHARACTERS SEQUENCE)

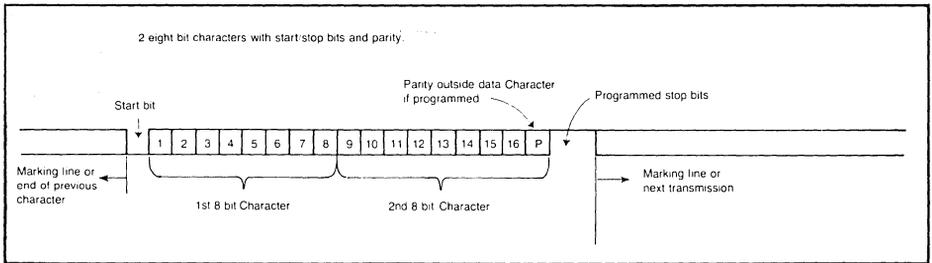


Figure 12 16 BIT ASYNCHRONOUS

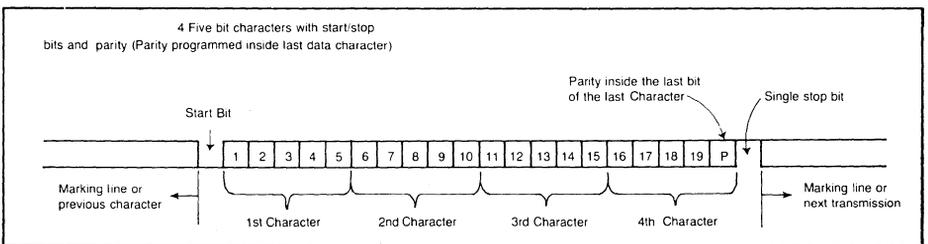


Figure 13 20 BIT ASYNCHRONOUS

ASYNCHRONOUS OPERATION

When the Asynchronous mode is selected, start, stop and parity bits are inserted as programmed. The receiver and transmitter clocks can be programmed as 1X or 16X. The transmitter output, TXD line will mark or space after transmission depending on command register programming. A line break condition can be programmed by setting the TXSM bit (command register bit CR3) to a logic "1". The TXD line will be forced to a low as long as this bit is logic "1". When the receiver detects the input line (RXD) low for a period equal to the word length including start, parity and stop bits, the break detect flag will become active.

The multi-character option is available to the Asynchronous protocol. The user can select any combination of one to eight characters per word and 5, 6, 7 or 8 bits per character. This allows a minimum word length of 5 bits and a maximum of 64 bits, plus parity, if enabled.

SYNCHRONOUS OPERATION

When the Synchronous mode is selected, start and stop bits are not transmitted. Parity is not available in Synchronous mode. The multi-character option is not available; however, the transmitter will continuously shift out data as long as the transmit holding register is buffered by the CPU. Two I/O signals are provided for synchronization, TIP (transmission in progress), an output which indicates that the transmitter is actively sending data and SYNCDET (SYNC detect), an input which notifies the receiver logic when to begin assembling characters.

Synchronization is obtained when the TIP signal from the transmitter is brought to the SYNCDET input of the associated receiver. Completion of a data transmission sequence occurs when the last character in the transmit register is sent and no further data is loaded into the transmit holding register. The TIP signal goes low. The receiver monitors the SYNCDET line and assembles data characters until it goes low, at which time it goes to an idle state.

PARITY MODES

The WD1984 is provided with some unique parity options as discussed above. If parity is enabled and the word length is eight bits, the parity is added to the transmitted word and stripped from the received word. When programmed for 5, 6 or 7 bits per character, the receiver checks and makes available the parity bit on the bus next to the MSB of data. Unused bits in an assembled character are zero when the receive holding register is read.

For example, in Asynchronous mode when two 8 bit characters are programmed with parity after the Data Word and two stop bits, 20 bits are transmitted. These are the Start bit, 16 Data bits, Parity and the 2 Stop bits. The Parity will be stripped off at the receiver since the character length is 8.

In Synchronous mode, Parity is not available and it is suggested the user provide his own software CRC as the last characters of his transmission.

OPERATING DESCRIPTION

The WD1984 is primarily designed to operate in an 8 bit micro-processor environment, although other control logic schemes are easily implemented. The DATA BUS and the Interface Control Signals (\overline{CS} , \overline{RE} , \overline{WE} and C/D) should be connected to the microprocessor's data bus and system control bus. The appropriate TXC and RXC clock frequencies should be selected for the particular application, using a programmable baud rate generator such as a BR1941. A master reset pulse initializes the WD1984 and presets the control registers to transmit and receive four 8-bit contiguous characters with the 32nd bit odd parity. If other protocols are desired, then the mode and command registers should be programmed as discussed previously.

For typical data communication applications, the RXD and TXD input/outputs can be connected to RS-232C interface circuits or a modem.

The TXRDY, RXRDY, FCR and FE/BRKDET Flags may be connected to the microprocessor system as interrupt inputs. The status register can be periodically read in a polled environment to support operations.

The \overline{CTS} input can be used to synchronize the transmitter to external events.

The WD1984 is designed such that a control register write operation accesses the command instruction register. The mode instruction register is accessed by performing a control write operation setting the internal reset bit high, which allows the next control write operation to program the mode register. Subsequent control write operations will again access the command register until another internal reset is performed. Internal reset commands should also disable the receiver and transmitter until the new mode instruction is programmed. The next command should then reactivate the receiver and transmitter to resume operations. This minimizes any errors that may be generated as a result of an active receive line during reprogramming.

The TXSM bit of the command register causes the transmitter output to be forced low after the last word is transmitted. This is also used in Asynchronous mode to send a break character (all zero data and parity bits).

The receiver is equipped with logic to look for a break character in the Asynchronous mode. When a break character is received, the receiver activates the break detect flag and status bit. When the receiver input line goes high again for at least "one bit time", the receiver resets the break detect flag and resumes its search for a start bit.

MULTI-CHARACTER OPERATIONS

As discussed above, the WD1984 is equipped with a multi-character option which provides the user with the means of transmitting and receiving multiple contiguous characters of data within one set of start and stop bits. Since the WD1984 is an 8 bit bus-oriented device, the controlling processor must read the WD1984 data from its holding register before the subsequent characters are assembled. This situation also exists on the transmit side, i.e., the Transmit Holding Register must be loaded before the previous 8 bits are completely shifted out of the transmit register.

Several "flags" are provided for interrupt purposes so that continuity is maintained and data integrity is preserved. These flags are First Character Ready (FCR), Receiver Ready (RXRDY), Transmitter Ready (TXRDY) and Transmitter Empty (TXE).

The Transmitter operates as follows:

- a) With the mode and command registers programmed as desired, the transmitter is enabled, TEN (CR0) = "1".
- b) The TXE and TXRDY flags are "1" (active).
- c) The external $\overline{\text{CTS}}$ signal = "0".
- d) The CPU loads data into the Transmitter Holding Register, TXE and TXRDY go Low.
- e) The data is loaded into the transmit register and TXRDY goes High. This indicates the first data word is being sent and the character can be loaded into the holding register. If the WD1984 is programmed for more than one character (multi-character) then an underrun error will be generated if the next character is not loaded before the previous word is completely shifted out, unless the current character is the last character in a sequence.
- f) If the last character is transmitted and no more new data is to be sent, the transmitter will indicate its status

by raising the TXE flag. (No error is generated as a result of this condition.)

The Receiver operates similarly:

- a) With the control registers suitably programmed, the receiver is enabled, REN (CR2) = "1".
- b) The RXRDY and FCR flags are "0". (Inactive).
- c) The incoming data word activates the receive logic and the data begins to be assembled in the receive register.
- d) When the first character is completely assembled, the data is loaded into the Receive Holding Register, the FCR (First Character Ready) and RXRDY (Receiver Ready) flags become active, "1". The CPU should read the data prior to the reception of the next character or an overrun error will be generated as the receiver will overwrite the old data with the new data character just received.

LOOP TEST MODE:

As mentioned, the WD1984 is equipped with a diagnostic test mode, local loop-back. This mode is activated by setting the LTE command bit to a "1". The TEN and REN bits should be "1" and CTS should be "0". The receiver inputs are ignored and the transmitter outputs are held high V_{OH} . The transmitter is internally "looped-back" to the receiver and the error and status flags operate normally.

It is possible to program a test routine using the loop-back mode so that one can simulate "line breaks" and parity errors. This can be done using the TXSM command to interrupt a transmit sequence in "mid-stream", since setting the TXSM bit to a "1" while the transmitter is currently sending data will immediately cause zeroes to be sent until the TXSM bit is reprogrammed to a "0". This can only be done when in the loop-test mode, else the TXSM command is recognized only after the current transmission is complete.

For multicharacter operations, failing to reload the Transmit Holding Register in the middle of a data send sequence will cause an underrun error in the transmitter and a word error in the receiver. Failure to read the Receive Holding Register after a FCR or RXRDY flag will cause an overrun error to be generated.

For Loop-Back test operations, the user should be sure that the TXC and RXC clock frequencies are the same. This is normally implemented by placing the same clock signal on both pins (TXC and RXC).



ABSOLUTE MAXIMUM RATINGS

Storage Temperature	
Plastic ("F" package)	-55°C to +125°C
Ceramic ("E" package)	-65°C to +150°C
Voltage on any Pin with respect to ground	-0.5V to +7V
Power Dissipation	.400MW

Absolute ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Electrical Characteristics.

DC ELECTRICAL CHARACTERISTICS

$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$; $V_{CC} = 5.0\text{V} \pm 5\%$; $\text{GND} = 0\text{V}$

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITION
V_{IL}	Input Low Voltage	-0.5		.08	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 1.6\text{mA}$
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -100\mu\text{A}$
I_{DL}	Data Bus Leakage			-50	μA	$V_{OUT} = 0.45\text{V}$
				10	μA	$V_{OUT} = V$
I_{IL}	Input Leakage			10	μA	$V_{IN} = V_{CC}$
I_{CC}	Power Supply Current		45	80	mA	

CAPACITANCE

$T_A = 25^\circ\text{C}$; $V_{CC} = \text{GND} = 0\text{V}$

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITION
C_{IN}	Input Capacitance			10	pF	$f_C = 1\text{MHz}$
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND

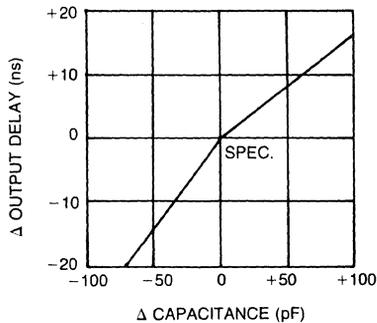


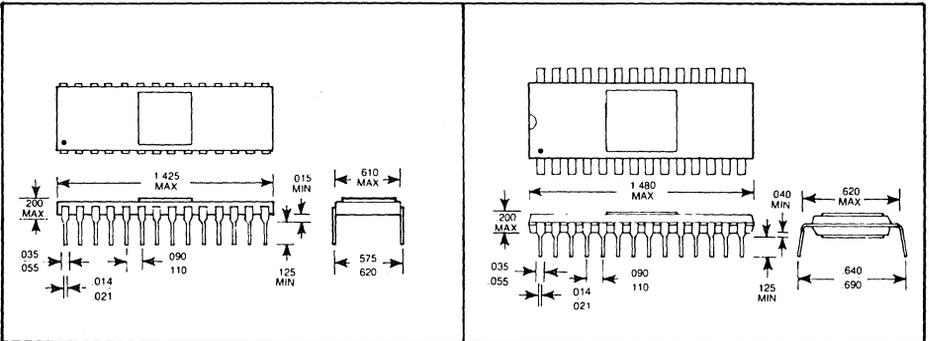
Figure 3 OUTPUT DELAY VS CAPACITANCE

A.C. TIMING PARAMETERS

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITIONS
BUS PARAMETERS					
Read Cycle (Reference Figure 5)					
t_{AR}	Address Stable before \overline{RE} , $(\overline{CS}, C/\overline{D})$	50		ns	
t_{RA}	Address Hold Time for \overline{RE} , $(\overline{CS}, C/\overline{D})$	5		ns	
t_{RE}	\overline{RE} Pulse Width	350		ns	
t_{RD}	Data Delay from \overline{RE}		200	ns	$C_L = 50\text{pF}$
t_{RDH}	\overline{RE} to Data Floating		200	ns	$C_L = 50\text{pF}$
		25		ns	$C_L = 50\text{pF}$

WRITE CYCLE (Reference Figure 6)					
t_{AW}	Address Stable before \overline{WE}	20		ns	
t_{WA}	Address Hold Time for \overline{WE}	20		ns	
t_{WE}	\overline{WE} Pulse Width	350		ns	
t_{DS}	Data Set-Up Time for \overline{WE}	200		ns	
t_{WDH}	Data Hold Time for \overline{WE}	40		ns	

OTHER TIMINGS (Reference Figure 7, 8, 9)					
t_{DTX}	TXD Delay from Falling Edge of TXC		500	ns	$C_L = 100\text{pF}$
t_{SRX}	RX Data Set-Up Time to Sampling Pulse	200		ns	$C_L = 100\text{pF}$
t_{NRX}	RX Data Hold Time to Sampling Pulse	100		ns	$C_L = 100\text{pF}$
t_{TX}	Transmitter Input Clock Frequency				
	1× Baud Rate	DC	500	kHz	
	4×, 16× Baud Rate	DC	750	kHz	
t_{TPW}	Transmitter Input Clock Pulse Width				
	1× Baud Rate			us	
	16× Baud Rate	500		ns	
t_{TPD}	Transmitter Input Clock Pulse Delay				
	1× Baud Rate	1.0		us	
	16× Baud Rate	700		ns	
t_{Rx}	Receiver Input Clock Frequency				
	1× Baud Rate	DC	500	kHz	
	4×, 16× Baud Rate	DC	750	kHz	
t_{RPW}	Receiver Input Clock Pulse Width				
	1× Baud Rate	1.0		us	
	16× Baud Rate	500		ns	
t_{RPD}	Receiver Input Clock Pulse Delay				
	1× Baud Rate	1.0		us	
	16× Baud Rate	700		ns	
t_{TX}	TXRDY Delay from center of Data Bit	200 ns	$\frac{1}{2}$	t_{TXC}	(1x or 16x)



WD1984E CERAMIC PACKAGE

WD1984F PLASTIC PACKAGE

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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General Data Communications Technical Notes

WESTERN DIGITAL

C O R P O R A T I O N

TECHNICAL NOTE

Using The New Data Link Control Chips

By Geary Leger

MARCH, 1981

- A NEW GENERATION OF LSI DEVICES FOR DATA LINK CONTROL HAS ARRIVED. WHAT ARE THE ADVANTAGES? PITFALLS? TRADE-OFFS?
- THE TECHNOLOGY OF LARGE-SCALE-INTEGRATION (LSI) HAS BROUGHT ABOUT A VARIETY OF NEW DATA COMMUNICATIONS DEVICES WHICH HANDLE BOTH EXISTING CHARACTER-ORIENTED PROTOCOLS AND THE RELATIVELY NEW BIT-ORIENTED PROTOCOLS. THE MOST WIDELY PUBLICIZED ARE THE MULTI-PROTOCOL CHIPS, AND THEIR ADVANTAGES HAVE BEEN DOCUMENTED. HOWEVER, THESE CHIPS MAY NOT OFFER THE OPTIMUM SOLUTION. A COMBINATION OF CHARACTER-ORIENTED AND BIT-ORIENTED PLUG-COMPATIBLE ICs MAY OFFER PERFORMANCE ADVANTAGE AND A COST-EFFECTIVE ALTERNATIVE TO THE MULTI-PROTOCOL CHIPS.

BIT AND CHARACTER-ORIENTED PROTOCOLS

A data link is a communications channel established between two or more locations for the purpose of information transfer. A protocol is a set of rules controlling the orderly exchange of that information.

Data exchanged across a data link contains both user information and control data. Satisfying the need to exchange the user information is the whole reason for the data link: the sole justification for the existence of the data link. The control (or supervisory) data assures the reliable and orderly information exchange. Insertion, separation, and interpretation of the control data is the responsibility of the protocol. A protocol must also provide link initialization, termination, and error recovery. Among the rather wide variety of protocols which have been used, there are only two types: character-oriented and bit-oriented.

Character-oriented refers to the method whereby both control data and text data have a fixed character length. This length is often 8 bits but may also appear as 5, 6, or 7 bits. Two types of synchronization are used. These are character synchronization, which resyncs at each character by the use of start/stop bits, and bit synchronization, which maintains a bit rate clock synchronized between transmitter and receiver. Character synchronization is commonly referred to as "asynchronous", and bit synchronization is usually called "synchronous".

In character-oriented protocol, control data and user information both have the same format and use the same character set, such as ASCII or EBCDIC. Therefore, it is necessary to have a means to distinguish the control data from the user information.

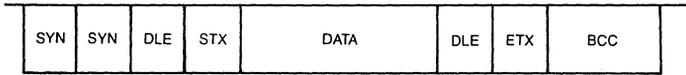
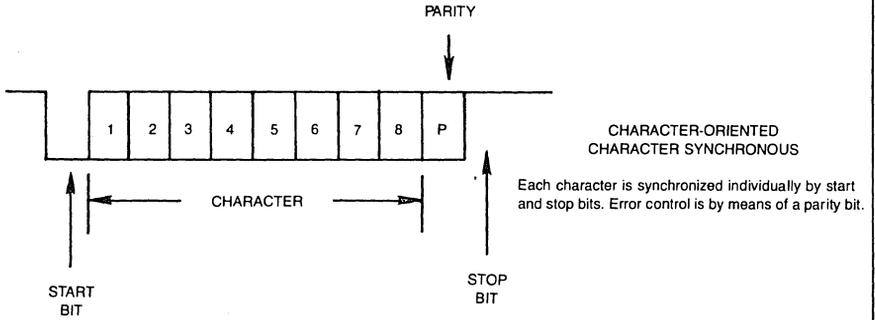
The character-oriented protocols have been in existence since the early 60's, which is considerably longer than the bit-oriented versions, and thus have a more widespread usage. The most popular has been "Bi-sync" (BSC).*

In the relatively new bit-oriented method, data are divided into frames which are preceded and ended by a unique flag pattern (01111110). Within the frame are all control and text data, and a 0 is inserted after each sequence of five contiguous 1's which provides data transparency. The only type of synchronization used is bit synchronization.

The bit-oriented protocols offer a number of improvements as shown in TABLE II. The standards for the bit-oriented are primarily High-Level Data Link Control (HDLC), Synchronous Data Link Control (SDLC), and Advanced Data Communication Control Procedure (ADCCP).

Initial work on the bit-oriented protocols began about 1969, with the first applications available in about 1974.

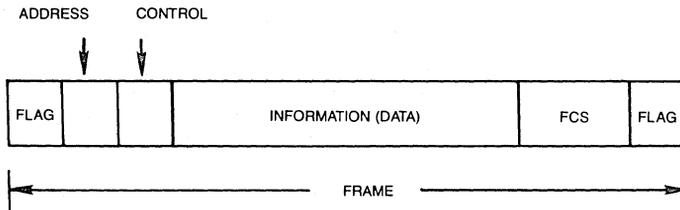
*BSC = Binary Synchronous Communications



CHARACTER-ORIENTED
BIT SYNCHRONOUS

This particular example is BSC, transparent.

Each bit is synchronized by a bit clock locked to the transmitter clock. Character synchronization is achieved by a beginning synchronizing (SYN) character. Error control is by a 16-bit block check character (BCC) which is generated by a cyclic redundancy check (CRC) polynomial $X^{16} + X^{15} + X^2 + 1$.



Each bit is synchronized by a bit clock locked to the transmitter clock. Each frame is synchronized by a unique beginning and trailing Flag (01111110). In between flags, all sequences of 5 contiguous 1's are followed by a 0. Since a Flag contains 6 contiguous 1's, it is not possible to misinterpret a Flag or Data. Error control is by the Frame Check Sequence (FCS) which is the 16 bits preceding the trailing flag. The FCS is generated by CRC polynomial $X^{16} + X^{12} + X^5 + 1$.

CHARACTER ORIENTED		BIT ORIENTED
ASYNCHRONOUS	SYNCHRONOUS	SYNCHRONOUS
Interactive devices such as teletypes and keyboard display devices ASR-33, T1 Silent 700, GE Terminent, etc.	BSC (BISYNC) DDCMP	HDLC, SDLC, ADCCP, CCITT X.25

Table I: APPLICATIONS OF CHARACTER-ORIENTED AND BIT-ORIENTED PROTOCOLS

CHARACTER ORIENTED PROTOCOLS	BIT ORIENTED PROTOCOLS
<ul style="list-style-type: none"> * Code Set Shared Between Data And Control Functions * Transparency Achieved Only Through Use Of Escape Mechanisms * Device, Message, And Link Control Intermixed * Error Checking On Text * Two-Way Alternate In Nature (i.e. half-duplex) * Relatively Rigid In Structure 	<ul style="list-style-type: none"> * Use Of Fields For Control Frees Code Set For Data * Naturally Code Transparent * Unambiguous As To Link Control Separates Link From Device And Message Control. * Error Checking On Text And Supervision * Two-Way Simultaneous Capability Provides Efficient Utilization Of Full Duplex Link. * Very Flexible And Modular. Provides For Wide Range Of Application.

Table II: COMPARISON OF CHARACTER AND BIT-ORIENTED PROTOCOLS.

IMPLEMENTATION PROBLEM

Since the character-oriented protocols have been in existence for some time, there is already a large amount of equipment installed world-wide which are established as character-oriented terminals. Herein also lies a problem that manufacturers and users of data communication equipment face with character-oriented terminals. The bit-oriented may represent the protocols of the future, but the character-oriented styles will stay for some time because of the enormous economic investment they represent. Thus, how does one plan for the future by providing bit-oriented capability, without prematurely obsoleting character-oriented equipment?

One solution is to use a multi-protocol-style chip; such as the Signetic 2652, the Zilog SIO or the Fairchild 3846. Basically, these chips provide both character-oriented and bit-oriented capabilities on the same chip.

One application for the multi-protocol chips is CCITT Recommendation X.21. X.21 defines three levels of data link control. Level 1 is the physical interface and specifies a mechanical connection of a 15-pin connector. Levels 2 and 3 are the link initialization and call establishment phases. The call establishment is specified as character-oriented, and is followed by the data transfer phase which the user is free to define as either character- or bit-oriented, but is bit-oriented in probably all applications.

However, in non-X.21 applications, only one protocol will be

used throughout that particular application. Therefore, a cost effective solution is to design a printed circuit (or socket) to accept either a character-oriented or a bit-oriented chip. To reach this end, Western Digital Corporation has developed a pin-for-pin compatible family, the WD1931 and WD1933. Therefore, a single P/C board could satisfy both existing character-oriented protocols and the newer bit-oriented protocols without the expense of a multi-protocol-style chip.

The WD1931 is a versatile character-oriented chip. This chip has automatic idle fill for both transparent and non-transparent BSC. Idle-fill is one desirable feature of BSC for transmitter processors which are slow with respect to the data rate. A SYN (non-transparent) or a DLE-SYN (transparent) may be inserted without affecting the integrity of the data, and the CS ASTRO may be programmed for either SYN fill or DLE-SYN fill.

The WD1933 is a universal bit-oriented data link controller which will handle HDLC, ADCCP, or SDLC. Bit rates up to 1.5M bps may be achieved. A digital phase locked-loop may be used with a 32X clock to facilitate usage modems without timing clocks. Also, the WD1933 may be used for SDLC loop applications such as the IBM 3650 Retail Stores System.

Table III shows a comparison of the combination 1931/1933 with two popular multi-protocol chips.

Figure I details the compatibility of the 1931/1933 pins.

Table III. COMPARISON OF 1931/1933 COMBINATION WITH TWO POPULAR MULTI-PROTOCOL CHIPS

FEATURE	WESTERN DIGITAL		SIGNETICS 2652 or SMC 5025	ZILOG SIO
	1931	1933		
Maximum Data Rate (bps)	1M	1.5M	1M/2M	550K/880K
Bit-Oriented Protocol		Yes	Yes	Yes
SDLC Loop Mode Operation (e.g. IBM 3650)		Yes	No	No
Bit-Oriented Short Frame Detection		Yes	Yes	No
Bit-Oriented NRZI		Yes	No	No
Digital Phase-Locked Loop		Yes	No	No
Character-Oriented Protocol Synchronous	Yes		Yes	Yes
Automatic SYN Fill/Strip on BSC	Yes		Yes	Yes
Automatic DLE-SYN Fill/Strip on BSC Transparent	Yes		No	No
Asynchronous	Yes		No	Yes
Shortened STOP Bit Capability	Yes		N.A.	No
Asynchronous AUTO ECHO	Yes		N.A.	No
Loop Test Diagnostic Feature	Yes	Yes	Yes	No
CRC for HDLC		Yes	Yes	Yes
CRC for Bisync	No		No	Yes***
CRC for DDCMP**	No		Yes	Yes
Miscellaneous I/O Pins	OUT,ONLY	Yes	No	No

N. A. = Not Applicable

** DDCMP is Digital Equipment Corporation's protocol, "Digital Data Communication Message Protocol".

*** Only if DMA is not used.

Figure 1. PIN ASSIGNMENTS FOR THE 1931/1933

PIN #	1931	1933	COMMENTS
1	IC	IC	IC = Internal Connection
2	NIC	EOB	NIC = No Internal Connection
3	RE	RE	Same
4	CS	CS	Same
5	MISC OUT	MISC OUT	Same
6	INTRQ	INTRQ	Same
7	WE	WE	Same
8	DAL0	DAL0	Same
9	DAL1	DAL1	Same
10	DAL2	DAL2	Same
11	DAL3	DAL3	Same
12	DAL4	DAL4	Same
13	DAL5	DAL5	Same
14	DAL6	DAL6	Same
15	DAL7	DAL7	Same
16	MR	MR	Same
17	DTR	DTR	Same
18	DRQ0	DRQ0	Same
19	DRQ1	DRQ1	Same
20	GND	GND	Same
21	NIC	A2	NIC = No Internal Connection
22	A0	A0	Same
23	A1	A1	Same
24	+12V	MISC IN	See Note 1
25	TD	TD	Same
26	IXRC	RC	Same
27	RD	RD	Same
28	TBOC	NRZ1	See Note 2
29	CTS	CTS	Same
30	RSCLK	IX/32X	See Note 2
31	1XTC	TC	Same
32	RTS	RTS	Same
33	DSR	DSR	Same
34	RING	RI	Same
35	RI	RI1	See Note 3
36	R2	RI0	See Note 3
37	R3	CD1	See Note 3
38	R4	CD0	See Note 3
39	CARD	CD	Same
40	+5V	+5V	Same

Note 1: If the system design does not make use of MISC IN on the 1933, the user may tie this to +12V without harm or degradation to the 1933. This has the same effect as a logic input. If the system design does make use of MISC IN, then provisions must be made to select +12V when the 1931 is in the socket or MISC IN when the 1933 is in the socket. This may be accomplished by a small switch or by jumpers.

Note 2: The outputs TBOC and RSCLK on the 1931 may be tied to ground or to +5 volts through a 10K pull-up without harm or degradation to the 1931.

Note 3: If R1-R4 are not selected by the command word in the 1931, then anything may be on these inputs. If RI and CD are tied high in the 1933, then the inputs (pins 35-38) may have anything on them. When both the rate fields in the 1931 and RI and CD in the 1933 are used, the system designer must make provisions by an external switch or jumpers.

Note 4: The reader should also consult the data sheets for the 1931 and 1933.

ZC-10m6
1

BI-SYNC'S CRC: AN INHERENT APPLICATION PITFALL

Implementation of the Cyclic Redundancy Check (CRC) for the BSC (bi-sync) poses a problem with no easy solution. By contrast, the CRC application in the bit-oriented styles is more straightforward.

This is why all the bit-oriented chips handle the CRC automatically, but the character-oriented chips have difficulty with the bi-sync CRC.

TABLE IV shows the differences between the two computations. However, the most significant problem with the bi-sync CRC is the lack of continuity of the computation throughout the data stream. The bit-oriented CRC includes all data between the opening flag and the first bit of the Frame Check Sequence (FCS) field which just precedes the closing flag. However, the rule for the bi-sync (CRC-16) is: CRC is initialized by, but does not include, the beginning STX (Start of Text) or SOH (Start of Heading) and includes all data up to and including ETX (End of Text), except for DLE's (Data Link Escape) inserted for transparency, and except for SYN's (Synchronization character) if non-transparent, or except for DLE-SYN sequences not preceded by an odd number of DLE's if transparent.

Also, bi-sync may use one of two other error checking codes: CRC-12 or LRC (Longitudinal Redundancy Check), but the CRC-16 is most widely used.

Thus, it is clear as to why the Bi-sync CRC is a problem. There are a number of solutions.

The Zilog SIO performs the bi-sync CRC and allows the user to turn-on or turn-off the CRC for each character. This has only one draw-back in that this method cannot be easily used with Direct Memory Access (DMA).

Another popular solution is to perform the CRC in software. Then the CRC is turned on or off either by calling or not calling the CRC computation subroutine. Several routines are available, but are too numerous to mention here. One example of bi-sync CRC routine is shown in Figure 2, using the assembly language of the 8080 microprocessor. The disadvantage of any software CRC is the time-consuming software overhead. Higher bit rates can be achieved by computing CRC before transmission, or after reception, of a text frame. However, a time delay is still present, and system throughput could be impaired.

A third solution is to use a hardware CRC generator which is external to the data link control chip. This can offer the advantage of speed over the software approach, but has the disadvantage of added hardware costs.

To summarize, because of the nature of the bi-sync CRC, there is no "clean" solution to the problem of bi-sync CRC implementation.

Table IV. COMPARISON OF CRC'S
FOR BSC AND HDLC/SDLC.

FUNCTION	HDLC/SDLC	BSC (CRC-16)
Length	16 Bits*	16 Bits
Transmitted Order	High Order Bit First	High Order Bit First
Transmitted Polarity	Inverted	Non-Inverted
Pre-Set Value	All 1's	All 0's
ERROR-Free Detection Pattern	1111000010111000	All 0's
Include All Contiguous Data In Computation?	YES	NO
Polynomial	$X^{16} - X^{12} - X^5 + 1$	$X^{16} + X^{15} + X^2 + 1$

*Some Federal Government products require a 32 bit FCS.

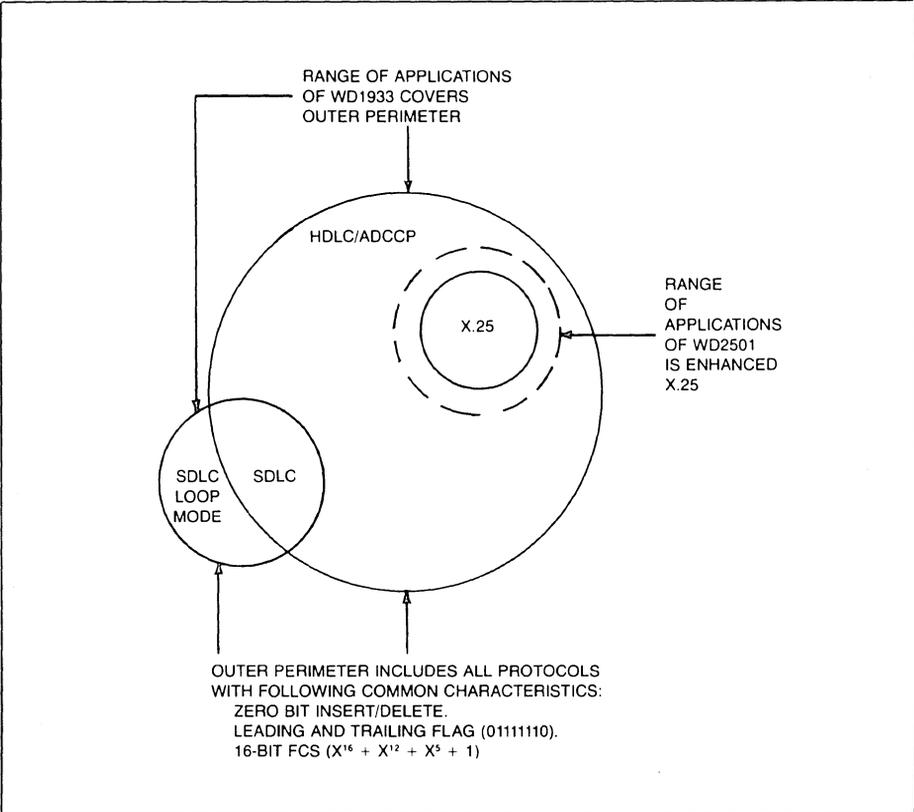


Figure 2 THE "WORLD" OF BIT-ORIENTED PROTOCOLS.

A DATA LINK CONTROLLER FOR PACKET NETWORKS

In addition to the 1933, Western Digital manufactures an LSI device for bit-oriented protocols used in Packet-Switching Networks. The WD2501 is called the Micro Packet Network Interface (uPAC) and is compatible² with CCITT X.25 with programmable enhancements. The 2501 is mentioned here only briefly, and the reader should consult the Data Sheet for more detail.

Both the 1933 and 2501 are bit-oriented devices aimed at different application areas. The 1933 handles the widest possible range of bit-oriented protocols. The 2501 is limited to applications at or near X.25, but does more work within this area. Figures 2 and 3 are aids to assist a user in selecting the bit-oriented controller that best fits his particular needs.

Figure 3 COMPARISON OF 1933 AND 2501 BIT-ORIENTED CONTROLLER

1933	2501
Handles all bit-oriented protocols HDLC, ADCCP, SDLC Complete modem control (DTR, DSR, RI, CD, RTS, CTS, etc.)	More specialized. Handles super-set of X.25, level 2. Limited modem control (RTS and CTS, only).
Zero-bit insertion/deletion, Flag appending and detection, and FCS included.	Zero-bit insertion/deletion, Flag appending and detection, and FCS included.
DMA compatible.	DMA included.
Retransmission control by external CPU decision.	Retransmission control included in the 2501.
Link set-up and disconnect controlled by external CPU thru 1933.	Link set-up and disconnect included in the 2501.
40-pin package.	48-pin package.

REFERENCES

1. "General Purpose Interface Between Data Terminal Equipment (DTE) and Data Circuit-Terminating Equipment (DCE) for Synchronous Operation Over Public Data Networks"; CCITT Recommendation X.21.
2. "Interface Between Data Terminal Equipment (DTE) and Data Circuit-Terminating Equipment (DCE) for Terminals Operating in the Packet Mode on Public Data Networks"; CCITT Recommendation X.25.

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Data-link control chip supports all three bit-oriented protocols

Ability to handle newer control procedures increases flexibility in designing data-communications systems

□ As with any form of communication, rules, whether implicit or explicit, are necessary if messages are to be received and interpreted properly. In the case of data communications, the increasing capability and complexity of equipment and rapidly rising software costs have called forth the development of more efficient sets of rules, or protocols. The recent protocols for data-link control have therefore switched from a character- to a bit-oriented approach.

This approach uses position instead of control characters to define the various parts of a message, thereby boosting throughput and greatly simplifying implementation. In addition, the newer protocols provide advanced error-checking techniques, data transparency, and full-duplex capability.

Western Digital Corp.'s SD1933 (and the version soon to be produced as a second source by National Semiconductor Corp.) is the first data-link control chip to fully support all three bit-oriented protocols: IBM Corp.'s Synchronous Data Link Control (SDLC), the International Standards Organization's High-Level Data Link Control (HDLC), and the American National Standards Institute's Advanced Data Communications Control Procedure (ADCCP), which is almost identical to HDLC (see "Lots of protocols," p. 142, and "Data-link control chips: bringing order to data protocols," *Electronics*, June 8, p. 104).

The SD1933 generates modem-controlling signals for total link control. It interfaces a parallel digital system with a serial data-communications channel. To understand how this is done, the basic unit of information transfer for the three bit-oriented protocols—the frame—has to be examined.

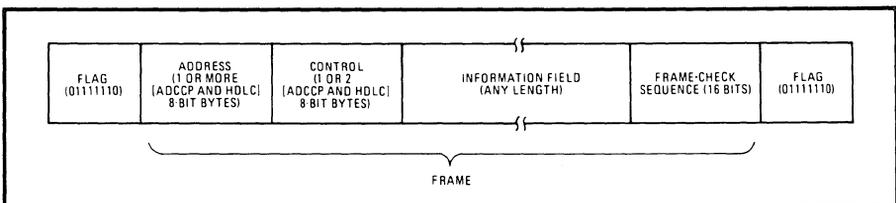
The frame consists of an address field, a control field, the information field, and a frame-check sequence (FCS) and is bounded at each end by a flag (Fig. 1). The flag sequence is 01111110.

Picturing the frame

There are two addressing modes: the basic address mode, which uses a single address byte (8 bits) and may be an individual, group, or global address; and the extended address mode (ADCCP and HDLC protocols only), in which the field is one or more bytes. In the latter, if the first (2⁰) bit of an address byte is a 0, then the next byte is an extension of the address field. The field is terminated by putting a 1 in the first bit of the last byte. In this way, the address field may be extended to any number of bytes.

The control field, for encoding commands and responses required to control the data link, is one (all three protocols) or two (ADCCP and HDLC) bytes long. Three types exist. They are: supervisory, used to convey ready or busy conditions and possibly to report frame sequence errors; information transfer, used to send sequenced information frames; and nonsequenced (un-numbered), for data-link management, which includes initializing or activating secondary stations, controlling the response mode of secondary stations, and reporting procedural errors.

The frame-check sequence provides error detection. It uses the CCITT's 16-bit error-checking algorithm to perform a cyclic redundancy check on the address, control, and information fields. The transmitter first presets its 16-bit frame-check sequence to all 1s. Next, the binary value of the transmission to be sent is multi-



1. Information transfer. The frame is made up of groups, or fields, of bytes that contain all the required data control information, as well as the data itself. It is always bounded by flag sequences. The flags contain no information; they act as start and stop signals.

Data-link control: a glossary

Abort	a sequence of 7 to 14 consecutive binary 1s that terminates a frame and also the continuity of the data link	Flag	a bit sequence (01111110) used to delimit frames
ADCCP	Advanced Data Communications Control Procedure: the American National Standards Institute's version (BSR X3.66) of SDLC	Full-duplex	simultaneous independent transmission of information in both directions
Address field	the field that defines the source or destination of a frame; it follows the opening flag of a frame	Global address	an address of all 1s, indicating that the frame is intended to be received by all stations
Asynch	any asynchronous data-communications protocol: transmission in which each character is individually synchronized by the use of start and stop bits; the length of the gap between characters is not necessarily fixed	Go-ahead mode	a special SDLC mode in which the link is configured as a loop with one primary and n secondary stations
Bisync	Binary Synchronous Communications: a character-oriented synchronous data-communications protocol developed by IBM; the predecessor of SDLC	Go-ahead pattern	a bit pattern of one 0 followed by seven 1s, which is recognized by secondary stations as permission to transmit
Control field	a one- or two-byte (ADCCP and HDLC only) field that follows the address field and is used for sending commands and responses required to control the data link	HDLC	High-Level Data Link Control: the International Standards Organization's (ISO 3309) version of SDLC
CRC	cyclic redundancy check: an error-checking technique that uses a sophisticated mathematical algorithm	Idle	a sequence of 15 or more consecutive 1s, indicating that the data link is to be idled
Extended address	feature of ADCCP and HDLC that allows the address field to be more than one byte long	l-field	information field
FCS field	frame-check sequence field: a 16-bit error-checking field to validate transmission accuracy; it uses CRC	NRZI	nonreturn-to-zero-inverted coding: a coding method in which the output remains in the same state to send a binary 1 and changes state to send a binary 0
		SDLC	Synchronous Data Link Control: IBM's most recent synchronous data-communications protocol (GA27-3093)
		STR	Synchronous Transmit and Receive: IBM's earliest synchronous data-communications protocol; predecessor of Bisync
		Zero insertion and deletion	an encoding and decoding method used within a frame to guarantee that there are no more than five 1s in a row, thereby ensuring data transparency

plied and divided by appropriate polynomials. The integer quotient is then ignored and the complement of the remainder is transmitted. The receiver performs a similar computation on each incoming frame, including

the frame-check sequence. If there are no errors, the receiver's FCS equals F0B8 (hexadecimal).

The information field may be any length, including zero. Thus the minimum frame, not counting flags, is 32 bits long. In SDLC, the information field length must be a multiple of 8 bits; consequently, the SD1933 can generate and receive a residual byte of 1 to 7 bits.

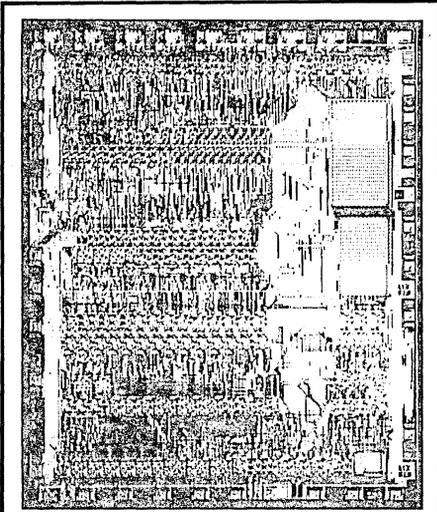
SYNCHRONOUS DATA-LINK CONTROL CHIP FUNCTIONS	
Transmitter	Receiver
Zero insertion	Zero deletion
CRC generation	CRC check
Abort generation	Aborted frame detection
Residual byte transmission	Residual byte detection
Variable-byte-length transmission	Variable-byte-length reception
Go-ahead (loop) mode	Go-ahead (loop) mode
NRZI encoding	NRZI decoding
Flag generation	Idle detection
	Invalid frame detection
	Address comparison
	Address extension

Aborting the frame

Besides flags, two other bit sequences have meaning, and both are important features of the three bit-oriented protocols. A transmitting station may end a frame by sending an abort—a sequence of 7 to 14 1s. The receiving station will then ignore the frame, and it may not send another frame until it receives a command from the primary station.

The third bit sequence triggers the idle state provided for by the three protocols. The data link is idled when a station receives 15 or more 1s in a row. It remains idled until a 0 is detected.

Another attribute of these protocols is zero insertion



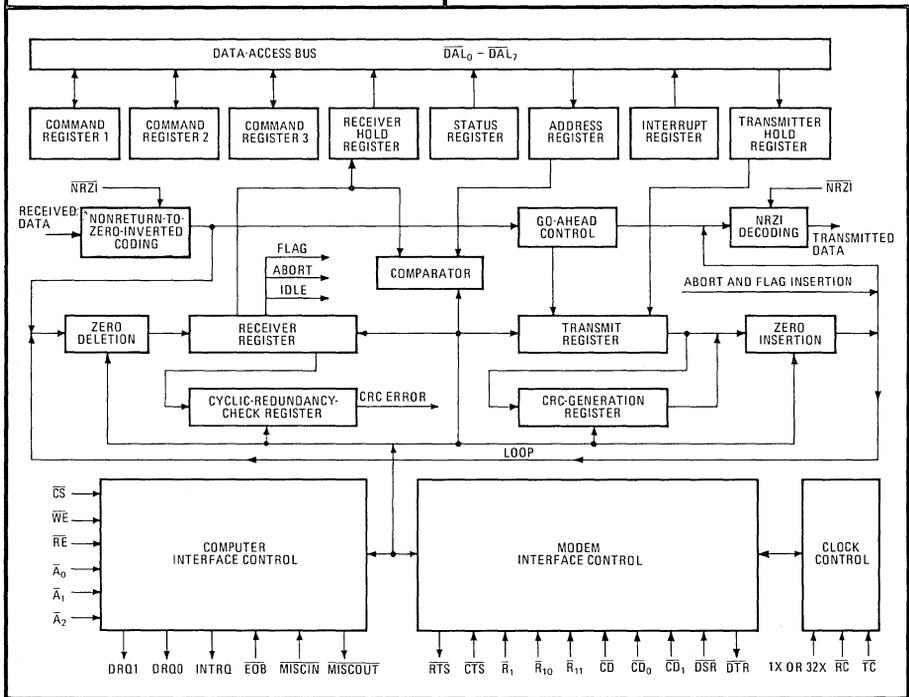
and deletion, which ensures data transparency. Within the two flags of a frame, a 0 is automatically inserted during transmission after five 1s and deleted on reception. Therefore no bit sequence in a frame can be misinterpreted as a flag, an idle, or an abort.

In addition, SDLC features a loop mode, called go-ahead. In this mode, each secondary station becomes a repeater. Transmissions from the primary are relayed from station to station and then back to the primary. Any secondary station finding its address in the address field of a frame captures that frame for action. All received frames are then relayed to the next station down the loop.

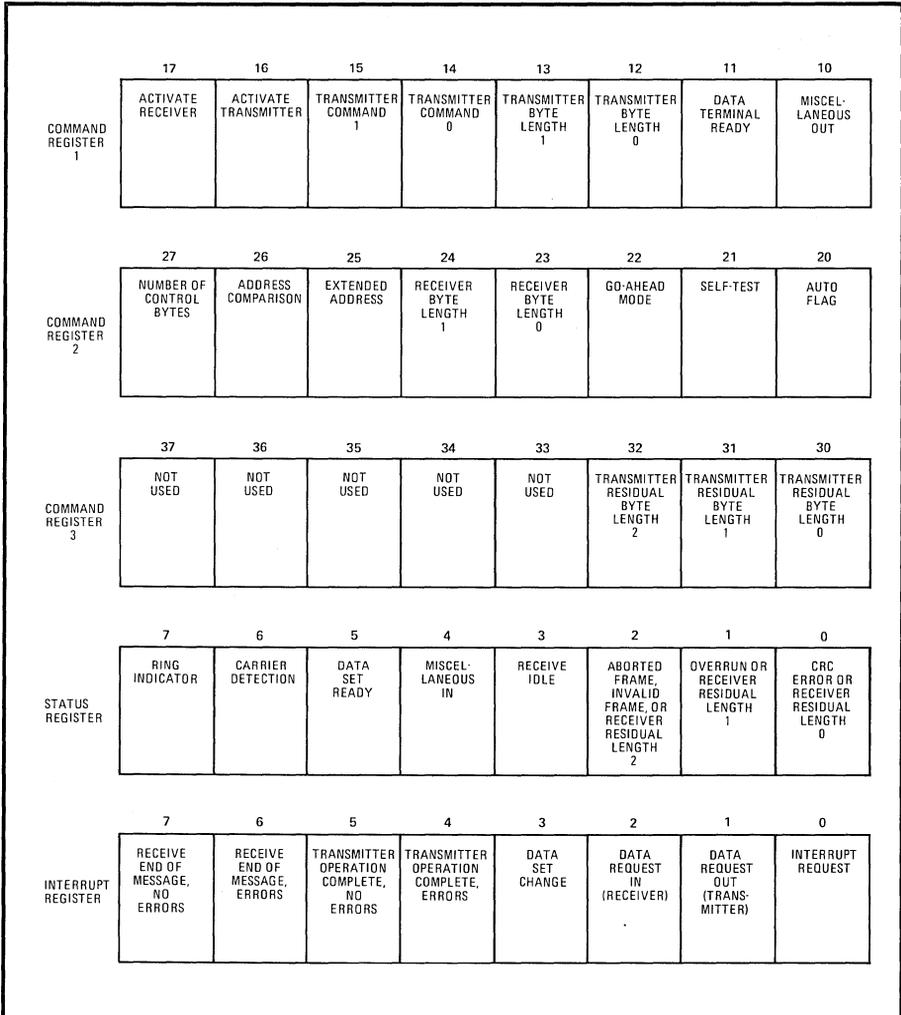
Whenever a secondary station receives the go-ahead pattern (a 0 followed by seven or more consecutive 1s), it may, at its option, suspend repeating and put its own transmission on the line. When it is finished, it sends a go-ahead pattern, deactivates its transmitter, and again becomes a repeater.

Performing the functions

The SD1933 performs all the functions required by the SDLC, ADCCP, and HDLC protocols (see the table). Built with n-channel metal-oxide-semiconductor technology, it uses a single 5-volt supply and is transistor-



2. **Layout.** The architecture of the SD1933 data-link control chip is fabricated on a chip 300 mils by 300 mils (top). Internal interconnections (bottom) use 40 external pins for interfacing a parallel digital system with a synchronous serial-data channel.



3. Registers. The SD1933 exercises system control through the command registers and monitoring through the status and interrupt registers. Command-register functions include specifying the type of information to be transmitted and received and the number of bits per byte.

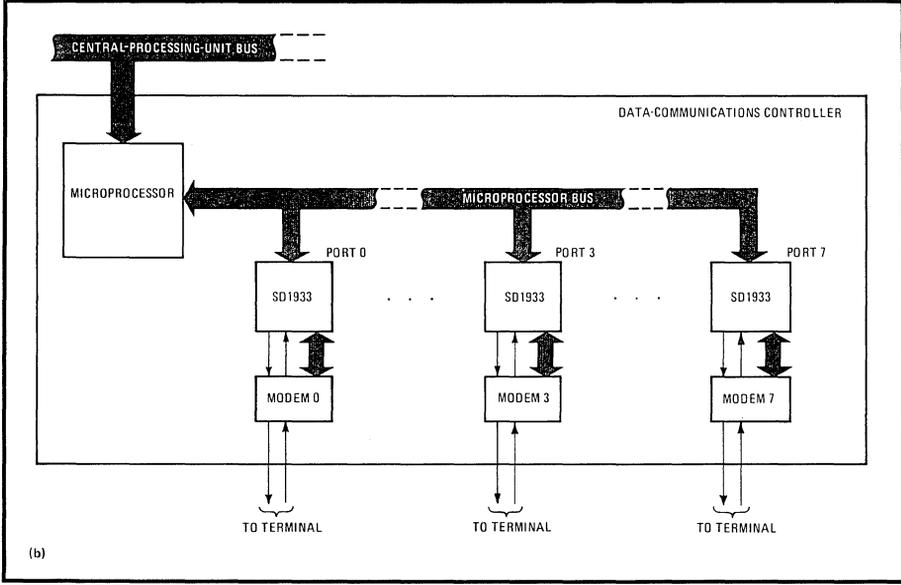
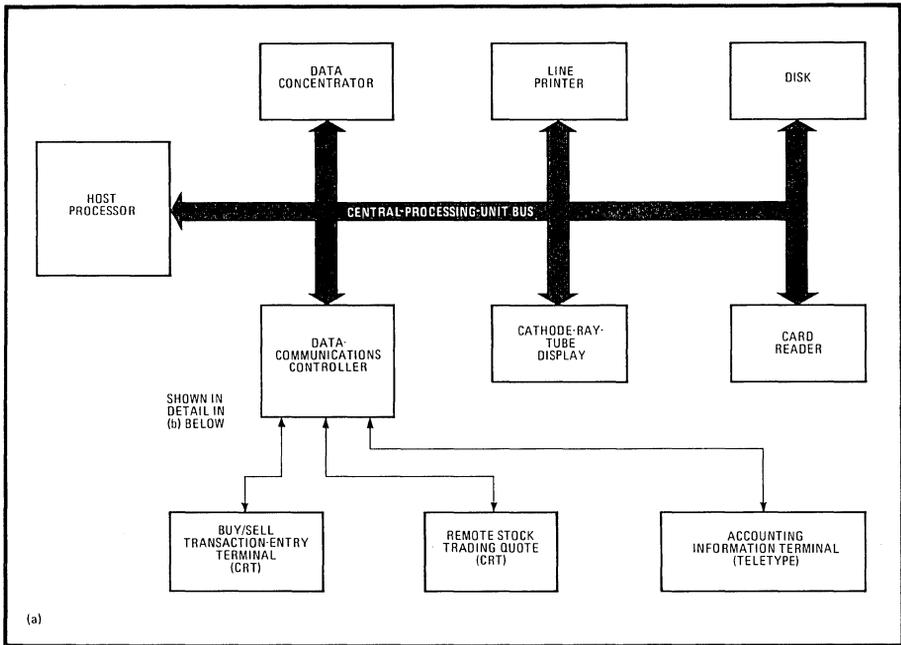
transistor-logic-compatible on all inputs and outputs. It comes in a 40-pin dual in-line package.

The SD1933 operates at 1.5 MHz in full-duplex operation, and the SD1933-03 at 2.05 MHz. Its basic read and write signals are: chip select (CS), read enable (RE), write enable (WE), register-address select (A₀-A₂), and data-access (DAL₀-DAL₇).

Read and write operations are initiated by placing signals on the appropriate lines. For example, a write

operation is initiated by placing a 3-bit address on the A₂-A₀ lines. CS and WE must then be activated. The data on the data-access lines are then locked into the registers when either CS or WE is deactivated. A read operation is initiated by placing the register address on the A₂-A₀ lines. Next, CS and RE must be activated. Data is then valid on the data-access lines and remains valid until either CS or RE is deactivated.

System control is done through the command regis-



4. Location. A basic data-communications system for a stock brokerage firm (a) uses Western Digital's SD1933 data-link control chip to connect a microprocessor to each modem in the line (b). Other applications include tellers' terminals and cash register terminals.

ters, and monitoring is accomplished by use of the status and interrupt registers (Fig. 3). The command registers dictate what the transmitter will send: the type of information (abort, flag, FCS, or data), the number of bits per byte, and the number of bits in the residual byte. Similarly, they tell the receiver the types of frames to look for, the number of bits per byte, whether to perform an address comparison, and whether to watch for an extended address.

Monitoring the signals

The status and interrupt registers perform monitoring. The status register indicates if an aborted or invalid frame has been received, whether an idle was received, and so on. The interrupt register indicates if end-of-message signals have been received and if frame transmission is complete. It also monitors the status of the interrupt signals.

Various modems are readily accommodated, as the SD1933 has a full complement of modem interface signals. These signals include data set ready (DSR), ring indicator (RI), carrier detect (CD), clear to send (CTS), request to send (RTS), and data terminal ready (DTR). An interrupt is generated if DSR, RI, or CD changes state (the latter two if so programmed). RI and CD may be programmed to interrupt on the rising edge, on the falling edge, or on both edges. The interrupt source is determined by reading the interrupt and status registers. The DTR output is set by a bit in the command register and RTS is set when the transmitter is activated.

Still more choices

When the nonreturn-to-zero-inverted code is chosen (a data transition when a 0 is sent and no transition when a 1 is sent), the transmitter encodes the transmitted data with the NRZI code before shifting it out. Similarly, the receiver expects NRZI-encoded data and will decode it before assembling data bytes.

In the 1X mode, the SD1933 requires the clock and data signals to be phase-synchronized in order to ensure link integrity. In the 32X mode, it uses a digital phase-locked loop to provide the synchronization, thus allowing connection to asynchronous modems as well. However, the loop requires data transitions to do this. Zero insertion and deletion guarantees transitions for long strings of 1s within a frame. To provide transitions for long strings of 0s, the nonreturn-to-zero-inverted option should be used.

The end-of-data-block (EOB) option allows easy transfer of blocks of memory by direct memory access. Activated at the end of the data block, it causes automatic transmission of the frame-check sequence and a flag.

Putting the chip to work

In a typical data-communications application (Fig. 4) such as might be found in a stock brokerage firm, the host and its peripherals are located at the main office. Terminals are also located in remote offices, with connection to the host via data-communications controllers. The terminals provide up-to-the-minute stock prices, entry of customers' buy and sell orders, and companies' financial statements, as well as the firm's

Lots of protocols

Since the advent of synchronous data communications, a wide variety of protocols has been developed by various military agencies, universities, and companies. The most widely used have been those generated by IBM Corp.

The earliest were the Synchronous Transmit and Receive (STR) and Binary Synchronous Communications (Bisync) protocols. However, the increased sophistication of processing equipment called for more efficient procedures.

Synchronous Data Link Control (SDLC), announced in 1973, was developed to permit accurate full-duplex transmissions with a high throughput. Some of the advantages of SDLC over STR and Bisync are independence of code structure, full information transparency without the use of control characters, a single standard-frame format, and full-duplex operation.

After the introduction of SDLC, several national and international organizations issued their own versions. The International Standards Organization's High-Level Data Link Control (HDLC) is described in the ISO 3309 specification. The American National Standards Institute's version, called Advanced Data Communications Control Procedure (ADCCP), is described in ANSI BSR X3.66. The ISO and the ANSI specs are very similar and both are supersets of SDLC (except for its loop mode).

accounting and billing information.

Such a system is general enough to be configured for a wide variety of applications. For example, the host processor and remote terminals could be located respectively in airline reservation offices and ticket counters, travel centers and travel agencies, central bank offices and branch banks, or department stores and individual cash registers.

The host processor performs high-level data-processing tasks such as accounting, bookkeeping, and input and output to the cathode-ray-tube terminal, line printer, card reader, or disk. Usually, a large portion of the data processing is dedicated to sending or accepting data to or from the data concentrator. Sending large blocks of data to the remote terminals via the data concentrator relieves the host of time-consuming I/O chores, freeing it for other processing tasks.

The data concentrator processes and formats data to allow for more orderly and efficient information transfer between the host and the data-communications controller. It is modified for each application to enable it to translate the data received from the controller into a format acceptable to the host, and vice versa. Other functions include setting priorities for the controller's channels, processing interrupts, and holding data until the host is ready to accept it.

The data-communications controllers interface remote terminals via modems (if necessary) with the data concentrator. Each controller uses a microprocessor to manage eight serial data-communications ports. Each port contains a printed-circuit board with a 40-pin socket filled with the chip appropriate for SDLC or Bisync communications. A DIP switch on each pc board programs it to expect the right one. □

General Data Communications Applications Notes

TR1602/TR1863 MOS/LSI APPLICATION NOTES ASYNCHRONOUS RECEIVER/TRANSMITTER

120-101MS

AUGUST, 1980

INTRODUCTION

The transfer of digital data over relatively long distances is generally accomplished by sending the data in serial form thru a single communications channel using one of two general transmission techniques; *asynchronous* or *synchronous*. Synchronous data transmission requires that a clock signal be transmitted with the data in order to mark the location of the data bits for receiver. A specified clock transition (either rising or falling) marks the start of each data bit interval as shown in Figure 1. In addition, special synchronization data patterns are added to the start of the transmission in order for the receiver to locate the first bit of the message. With synchronous transmission, each data bit must follow contiguously after the sync word, since one data bit is assumed for every clock period.

With asynchronous transmission, a clock signal is not transmitted with the data and the characters need not be contiguous. In order for the receiver to properly recover the message, the bits are grouped into data characters (generally from 5 to 8 bits in

length) and synchronizing start and stop elements are added to each character as shown in Figure 2.

The start element is a single logic zero (space) data bit that is added to the front of each character. The stop element is a logic one (mark) that is added to the end of each character. The stop element is maintained until the next data character is ready to be transmitted. (Asynchronous transmission is often referred to as start-stop transmission for obvious reasons). Although there is no upper limit to the length of the stop element, there is a lower limit that depends on the system characteristics. Typical lower limits are 1.0, 1.42 or 2.0 data bit intervals, although most modern systems use 1.0 or 2.0. The negative going transition of the start element defines the location of the data bits in one character. A clock source at the receiver is reset by this transition and is used to locate the center of each data bit.

The rate at which asynchronous data is transmitted is usually measured in *baud*, where a baud is defined to be the reciprocal of the shortest signal element (usually one data bit interval). It is interesting to note

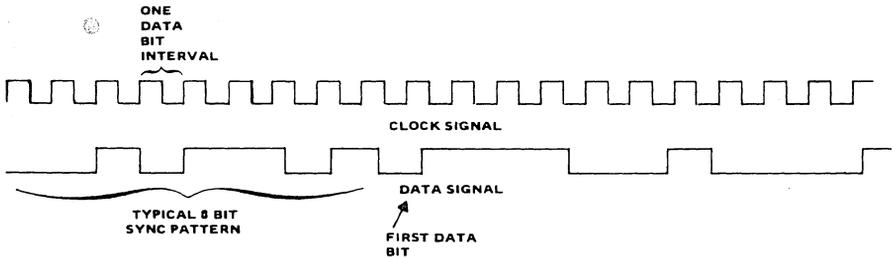


Figure 1 Synchronous Data

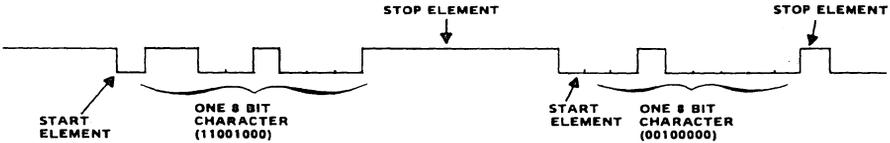


Figure 2 Asynchronous Data

that the variable stop length is what makes the baud rate differ from the bit rate. For synchronous transmission, each element is one bit in length so that the baud rate equals the bit rate. The same is true for asynchronous transmission if the stop element is always one bit in duration (this is referred to as *isochronous* transmission). However, when the stop code is longer than one bit, as shown in Figure 3, the baud rate differs from the bit rate.

Each character in Figure 3 is 11 data bit intervals in length, and if 15 characters are transmitted per second, then the shortest signal element (one data bit interval) is $66.6 \text{ ms}/11 = 6.06 \text{ ms}$; giving a rate of $1/6.06 \text{ ms} = 165 \text{ baud}$. However, since only 10 bits of information (8 data bits, one start bit and 1 stop bit) are transmitted every 66.6 msec, the bit rate is 150 bit/sec. (Even though the stop element lasts for two data intervals, it still is only one bit of information)

There are several reasons for using asynchronous transmission. The major reason is that since a clock signal need not be transmitted with the data, transmission equipment requirements are greatly simplified. (Note, however, that an independent clock source is still required at both the transmitter and receiver). Another advantage of asynchronous transmission is that characters need not be contiguous in time, but are transmitted as they become available. This is a very valuable feature when transmitting data from manual entry devices such as a keyboard. The major disadvantage of asynchronous transmission is that it requires a very large portion of the communication channel bandwidth for the synchronizing start and stop elements (a much smaller portion of the bandwidth is required for the sync words used in synchronous transmission).

Asynchronous transmission over a simple twisted wire pair can be accomplished at moderately high baud rates (10K baud or higher depending on the length of the wire, type of line drivers, etc.) while it is generally limited to approximately 2K baud over the telephone network. When operating over the telephone network, a modem is required to convert the data pulses to tones that can be transmitted through the network.

One of the major limiting factors in the speed of asynchronous transmission is the distortion of the signal elements. Distortion is defined as the time displacement between the actual signal level transition and the nominal transition (Δt), divided by the nominal data bit interval (See Figure 4).

The nominal data bit interval is equal to the reciprocal of the nominal transmission baud rate and all data transitions should ideally occur at an integer number of intervals from the start bit negative going transition. Actual data transitions may not occur at these nominal points in time as shown in the lower waveform of Figure 4. The distortion of any bit transition is equal to $\Delta t \times \text{NOMINAL BAUD RATE}$.

This distortion is generally caused by frequency jitter and frequency offset in the clock source used to generate the actual waveform as well as transmission channel, noise, etc. Thus, the amount of distortion that can be expected on any asynchronous signal depends on the device used to generate the signal and the characteristics of the communication channel over which it was sent. Electronic signal generators can be held to less than 1% distortion while electromechanical devices (such as a teletype) typically generate up to 20% distortion. The transmission channel may typically add an additional 5% to 15% distortion.

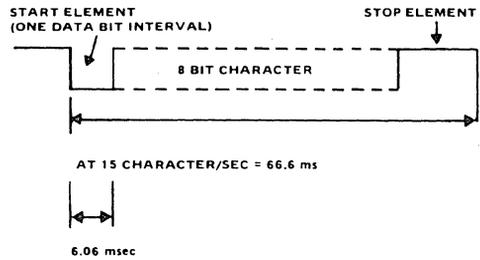


Figure 3

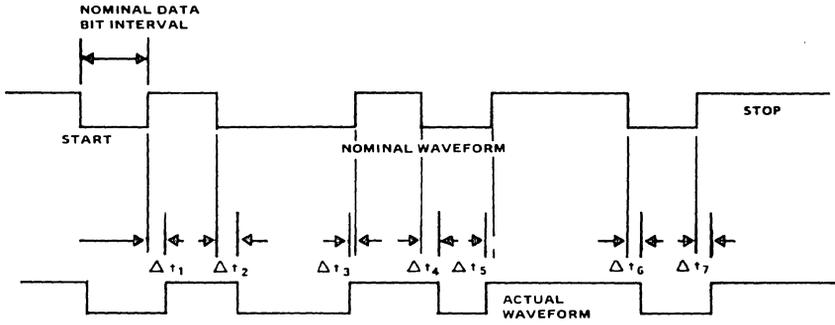


Figure 4A

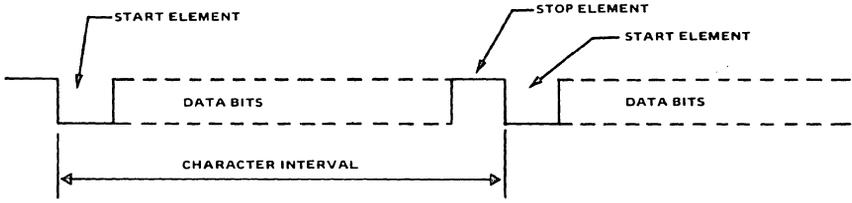


Figure 4B

The distortion previously described referred only to a single character as all measurements were referenced to the start element transition of that character. However, there may also be distortion between characters when operating at the maximum possible baud rate (i.e., stop elements are of minimum length). This type of distortion is usually measured by the minimum character interval as shown in Figure 4B.

The minimum character interval distortion is generally specified as the percentage of a nominal data bit interval that any character interval may be shortened from its nominal length. Since many of the same parameters that cause distortion of the data bits are also responsible for the character length distortion, the two distortions are often equal. However, some systems may exhibit character interval distortions of up to 50% of a data bit interval. This parameter is important when operating at the maximum baud rate since the receiver must be prepared to detect the

next start bit transition after the minimum character interval.

Asynchronous receivers operate by locating the nominal center of the data bits as measured from the start bit negative going transition. However, due to receiver inaccuracies, the exact center may not be properly located. In electromechanical devices such as teletypes, the inaccuracy may be due to mechanical tolerances or variations in the power line frequency. With electronic receivers, the inaccuracies are due to frequency offset, jitter and resolution of the clock source used to find the bit centers. (The bit centers are located by counting clock pulses). For example, even if the receiver clock had no jitter or offset, and it was 16 times the baud rate, then the center of the bit could only be located within 1/16 of a bit interval (or 6.25%) due to clock resolution. However, by properly phasing the clock, this tolerance can be adjusted so that the sample will always be within $\pm 3.125\%$ of the bit center. Thus,

signals with up to 46.875% distortion could be received. This number (the allowable receiver input distortion) is often referred to as the receiver distortion margin. Electromechanical receivers have distortion margins of 25 to 30%. The receiver must also be prepared to accept a new character after the minimum character interval. Most receivers are specified to operate with a minimum character interval distortion of 50%.

TR1602 Operation**

The WDC TR1602 is designed to transmit and receive asynchronous data as shown in Figure 5. Both the transmitter and the receiver are in one MOS CHIP, packaged in a 40 lead ceramic DIP. The array is capable of full duplex (simultaneous transmission and reception) or half duplex operation.

The transmitter basically assembles parallel data characters into a serial asynchronous data system. Control lines are included so that the characters may be 5, 6, 7 or 8 bits in length, have an even or odd parity bit, and have either one or two* stop bits. Furthermore, the baud rate can be set anywhere between DC and 20K baud by providing a transmit clock at 16 times the desired baud rate.

*1-1/2 with 5 bit code

**All references to the TR1602 operation also apply to the TR1863 operation.

The receiver disassembles the asynchronous characters into a parallel data character by searching for the start bit of every character, finding the center of every data bit, and outputting the characters in a parallel format with the start, parity and stop bits removed. Three error flags are also provided to indicate if the parity was in error, a valid stop bit was not decoded or the last character was not unloaded by the external device before the next character was received (and therefore the last character was lost). The receiver clock is set at 16 times the transmitter baud rate.

Both the transmitter and receiver have double character buffering so that at least one complete character interval is always available for exchange of the characters with the external devices. This double buffering is especially important if the external device is a computer, since this provides a much longer permissible interrupt latency time (the time required for the computer to respond to the interrupt).

The status of the transmitter buffer and the receiver buffer (empty or full) is also provided as an output.

Another feature of the TR1602 is that the control information can be strobed into the transmitter and receiver and stored internally. This allows a common bus from a computer to easily maintain the controls for a large number of transmitter/receivers.

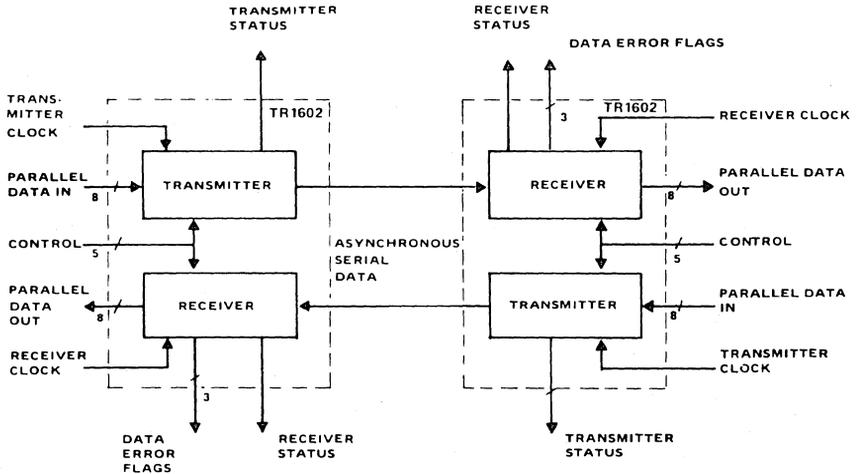


Figure 5

The TR1602 data and error flag outputs are designed for direct compatibility with bus organized systems. This feature is achieved by providing completely TTL compatible Three-state outputs (no external components are required). Three-state outputs may be set to a logic one or logic zero when enabled, or set to an open circuit (very high impedance) when disabled. A separate control line is provided to enable the data outputs and another one to enable the error flags so that the data outputs can be tied to a separate bus from the flag outputs.

The TR1602 inputs are also directly compatible with TTL logic elements without any external components.

TR1602 Description

Figure 6 is a block diagram of the transmitter portion of the TR1602. Data can be loaded into the Transmitter Holding Register whenever the Transmitter Holding Register Empty (THRE) line is at a logic one, indicating that the Transmitter Holding Register is empty. The data is loaded in by strobing the Transmitter Holding Register Load (THRL) line to a logic zero. The data is automatically transferred to the Transmitter Register as soon as the Transmitter Register becomes empty. The desired start, stop and parity bits are then added to the data and serial transmission is started. The number of stop bits and the type of parity bit is under control of the Control Register. The state of the control lines is loaded into the Control Register when the Control Register Load (CRL) line is strobed to a logic one. The 5 control lines allow 24 different character formats as shown in Table 1. These 24 formats cover almost all of the transmission schemes presently in use.

A Master Reset (MR) input is provided which sets the transmitter to the idle state whenever this line is strobed to a logic one. In addition, a Status Flag Disconnect (SFD) line is provided. When this signal is at a logic one, the THRE output is disabled and goes to a high impedance. This allows the THRE outputs of a number of arrays to be tied to the same data bus.

Figure 7 illustrates the relative timing of the transmitter signals. After power turn-on, the master reset should be strobed to set the circuits to the idle state. The external device can then set the transmitter register data inputs to the desired value and after the data inputs are stable, the load pulse is applied. The data is then automatically transferred to the Transmitter Register where the start, stop and parity (if required) bits are added and transmission is started. This process is then repeated for each subsequent character as they become available. The only timing requirement for the external device is that the data

TABLE 1
CONTROL DEFINITION

CONTROL WORD					CHARACTER FORMAT			
W	W				START	DATA	PARITY	STOP
L	L	P	E	S	BIT	BITS	BIT	BITS
S	S	I	P	B				
2	1	E	S					
0	0	0	0	0	1	5	ODD	1
0	0	0	0	1	1	5	ODD	1.5
0	0	0	1	0	1	5	EVEN	1
0	0	0	1	1	1	5	EVEN	1.5
0	0	1	x	0	1	5	NONE	1
0	0	1	x	1	1	5	NONE	1.5
0	1	0	0	0	1	6	ODD	1
0	1	0	0	1	1	6	ODD	2
0	1	0	1	0	1	6	EVEN	1
0	1	0	1	1	1	6	EVEN	2
0	1	1	x	0	1	6	NONE	1
0	1	1	x	1	1	6	NONE	2
1	0	0	0	0	1	7	ODD	1
1	0	0	0	1	1	7	ODD	2
1	0	0	1	0	1	7	EVEN	1
1	0	0	1	1	1	7	EVEN	2
1	0	1	x	0	1	7	NONE	1
1	0	1	x	1	1	7	NONE	2
1	1	0	0	0	1	8	ODD	1
1	1	0	0	1	1	8	ODD	2
1	1	0	1	0	1	8	EVEN	1
1	1	0	1	1	1	8	EVEN	2
1	1	1	x	0	1	8	NONE	1
1	1	1	x	1	1	8	NONE	2

inputs be stable during the load pulse (and 20 nsec after).

The TR1602 Transmitter output will have less than 1% Distortion at baud rates of up to 20K baud (assuming the Transmitter Register Clock is perfect) and is, therefore, compatible with virtually all other asynchronous receivers.

Figure 8 is a block diagram of the Receiver portion of the TR1602. Serial asynchronous data is provided to the Receiver Input (RI). A start bit detect circuit continually searches for a logic one to logic zero transition while in the idle state. When this transition is located, a counter is reset and allowed to count until the center of the start bit is located. If the input is still a logic zero at the center, the signal is assumed to be a valid start bit and the counter continues to count to find the center of all subsequent

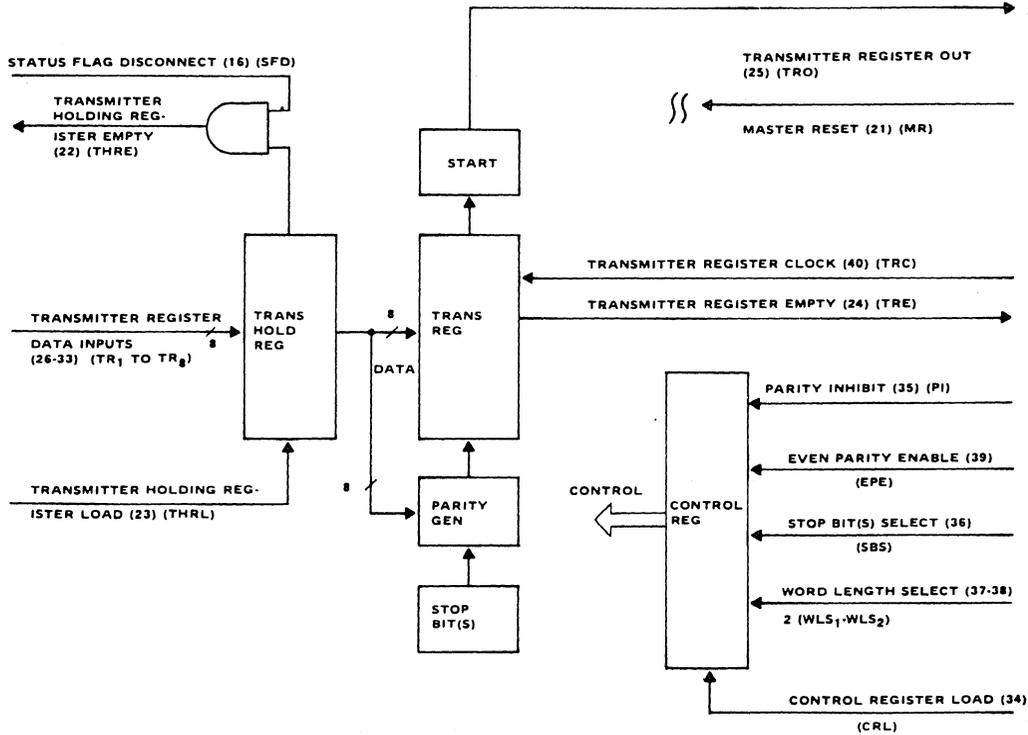


Figure 6 Transmitter Block Diagram

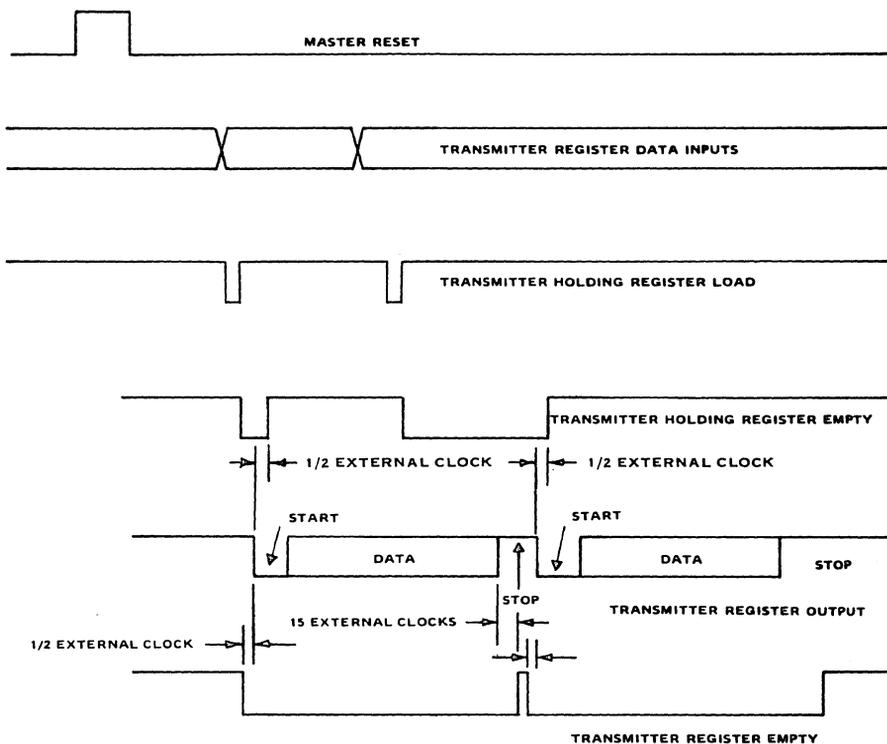


Figure 7 Transmitter Timing Diagram

data and stop bits. (Verification of the start bit prevents the receiver from assembling an erroneous data character when a logic zero noise spike is presented to the Receiver Input). The Receiver is under control of the Control Register described in the previous paragraph. This register controls the number of data bits, number of stop bits, and the type of parity as described in Table 1. The word length gating circuit adjusts the length of the Receiver Register to match the length of the data characters. A parity check circuit checks for even or odd parity if parity was added by the Transmitter. If parity does not check a Parity Error signal will be set to a logic one and this signal will be held until the next character is transferred to the Holding Register. A circuit is also provided that checks the first stop bit of each character. If the stop bit is not a logic one, the Framing Error line will be set to a logic one and held until the next

character is transferred to the Holding Register. This feature permits easy detection of a break character (null character with no stop element). As each received character is transferred to the Holding Register, the Data Received (DR) line is set to a logic one indicating that the external device may sample the data output. When the external device samples the output, it should strobe the Data Received Reset (DRR) line to a logic zero to reset the DR line. If the DR line is not reset before a new character is transferred to the Holding Register (i.e., a character is lost) the Overrun Error line will be set to a logic one and held until the next character is loaded into the Holding Register. The timing for all of the Receiver functions is obtained from the external Receiver Register Clock which should be set at 16 times the baud rate of the transmitter.

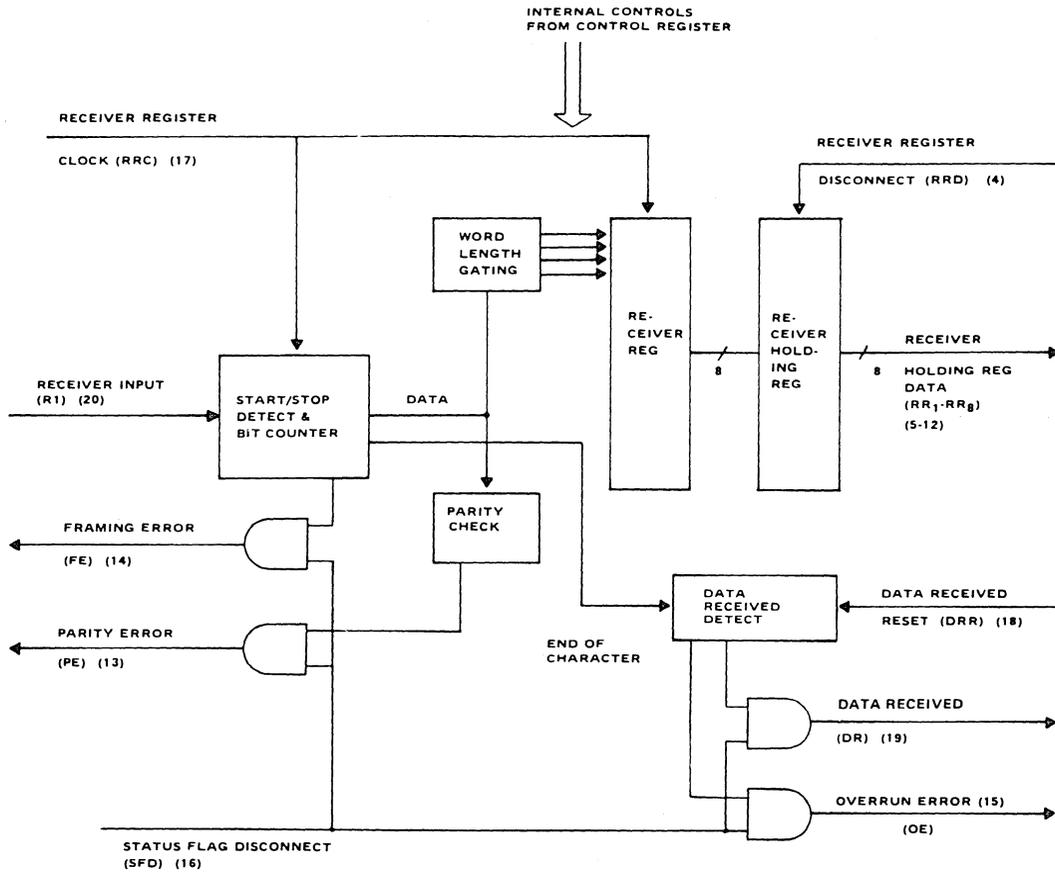


Figure 8 Receiver Block Diagram

Figure 9 illustrates the relative timing of the Receiver signals. A Master Reset strobe places the unit in the idle mode and the Receiver then begins searching for the first start bit. After a complete character has been decoded, the data output and error flags are set to the proper level and the Data Received (DR) line is set to a logic one. Although it is not apparent in Figure 9, the data outputs are set to the proper level one half clock period before the DR and error flags, which are set in the center of the first stop bit. The Data Received Reset pulse resets the DR line to a logic zero. Data can be strobed out at any time before the next character has been disassembled.

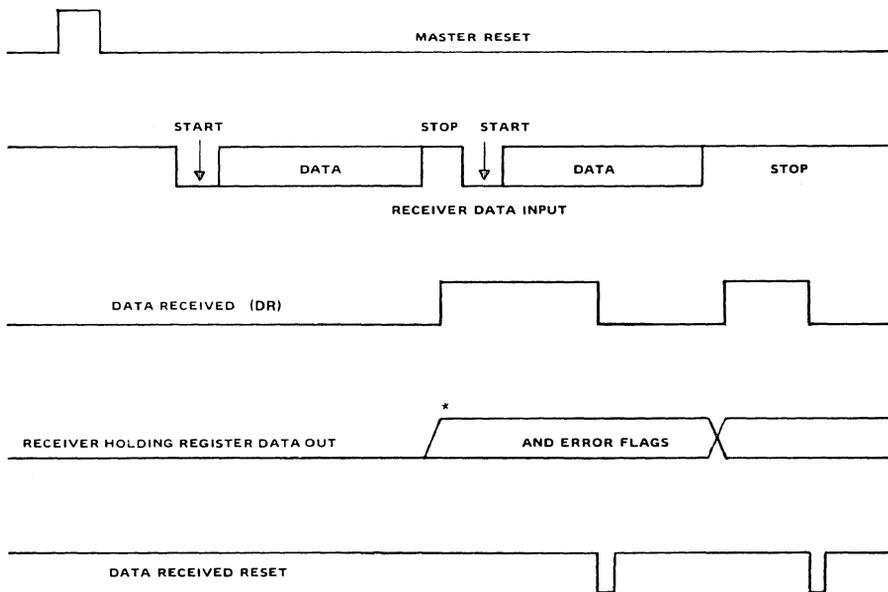
The TR1602 Receiver uses a 16X clock for timing purposes. Furthermore, the center of the start bit is defined as clock count 7-1/2. Therefore, if the receiver clock is a symmetrical square wave as shown in Figure 10, the center of the bits will always be located within $\pm 3.125\%$ (assuming a perfect input clock) thus giving a receiver margin of 46.875%.

In Figure 10, the start bit could have started as much as one complete clock period before it was detected, as indicated by the shaded area of the negative going transition. Therefore, the exact center is also unknown by the shaded area around the sample point. This turns out to be $\pm 1/32 = \pm 3.125\%$.

If the receiver clock is not perfect, then the receiver distortion margin must be further reduced. For example, if the clock had 1.0% jitter, 0.1% offset and the positive clock pulse was only 40% of the clock cycle; then, for a 10 element character, the clock would add:

$$1.0\% \text{ (Jitter)} + (0.1\% \times 10) \text{ (Offset)} + 0.1 \text{ (1/16) (Non-symmetrical Clock)} = 2.3\% \text{ Distortion}$$

(The frequency offset was multiplied by the number of elements per character since the offset is cumulative on each element).



*NOTE: DATA OUT AND OVER-RUN ERROR PRECEDES DR & ERROR FLAGS BY 1/2 CLOCK

Figure 9 Receiver Timing Diagram

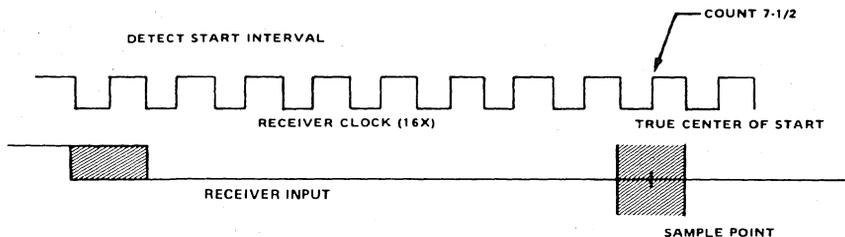


Figure 10

Since a clock with these characteristics is very easy to obtain, it is apparent that a receiver operating margin of slightly over 45% is very easy to achieve when using the TR1602. Furthermore, this margin is sufficient for virtually all existing transmitters and modems presently in use.

The TR1602 also begins searching for the next start bit exactly in the center of the first stop bit so that minimum character distortions of up to 50% can be accepted.

A break character (null character without a stop bit) will lock the receiver up since it will not begin looking for the next start bit until a stop bit has been received.

TYPICAL TR1602 APPLICATION

The TR1602 is ideally suited for use in distributed computer networks such as is illustrated in Figure 11. One of the primary purposes of the communications controller is to assemble and disassemble the asynchronous characters (required for communication with the data terminals) into the parallel data format required by the host computer. Often the communications controller is a minicomputer and character assembly/disassembly is performed by the software. When this is the case, the minicomputer must be interrupted at a rate equal to 8 to 16 times the baud rate of all terminals being handled by the controller. (The actual interrupt rate depends on the amount of distortion that can be experienced on the received characters). When the number of terminals exceeds 8 to 16, even the most powerful minicomputers become overloaded due to the high interrupt rate and the complex algorithms required by the software.

The TR1602 greatly reduces this problem by performing the character assembly/disassembly functions in external hardware as shown in a typical configuration in Figure 12. This solution not only reduces the interrupt rate by a factor of up to 176, but it also greatly

reduces the minicomputer load, thus freeing it for other functions.

Since the TR1602 inputs and outputs are TTL compatible, the TR1602 interface directly with virtually all minicomputer I/O busses. In Figure 12, the minicomputer Data Output Bus is connected to the Transmitter Register (TR) inputs and the Control Register inputs. When the minicomputer has a character to transmit, the character is placed on the Data Output bus and the address of the appropriate TR1602 is placed on the Device Address Bus. The Address Decode circuit will output a THRL load pulse under control of the Data Out Strobe from the mini. When the control register should be changed, a new 5 bit control word is placed on the Data Output Bus and along with an appropriate device address which is converted to a CRL load pulse in the Address Decode circuits, again under control of the Data Out Strobe. A THRE Pulse to the Interrupt Request circuit will notify the mini when a new character may be provided to the TR1602 for transmission.

When a character has been received, a DR signal to the Interrupt Request circuit will request an interrupt from the mini. The mini will respond by setting the proper device address and provide a Data in Strobe pulse. The Address-Decode circuit then sets the RRD line and SFD line to the appropriate receiver to enable the Data Outputs onto the mini Data Input Bus. The Data in Strobe from the mini then resets the DR signal with a DRR pulse from the Address Decode circuit.

The TR1602 Transmitter Output (TRO) and Receiver Input (RI) must generally be converted to RS232 levels if they interface with a modem as shown in Figure 12. RS232 is a standard that has been established by the Electronic Industries Association for the interface between data terminals and data communications equipment. RS232-C defines a space as greater than 3 volts and a mark as less than negative 3 volts at the Receiver input. A transmitter output of

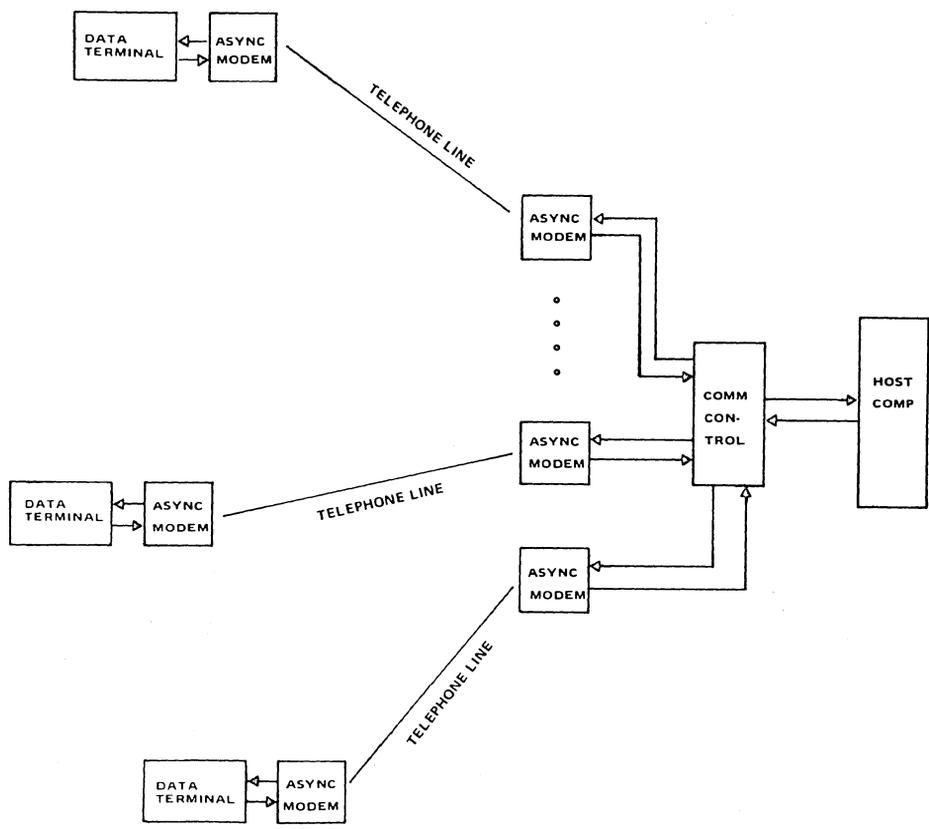


Figure 11

between 5 and 15 volts is a space while a level between -5 and -15 is a mark. The input/output impedances and signal rise and fall times are also specified by RS232. Fairly simple discrete level translators can be used to convert from the TTL levels to the RS232 levels, or monolithic IC's are also available.

It should be noted that the typical application illustrated in Figure 12 is only one of many and it does not take advantage of many of the TR1602 features. For example, the Status Flags could be tied to a separate interrupt request bus or the TRE output could be used to implement half-duplex operation.

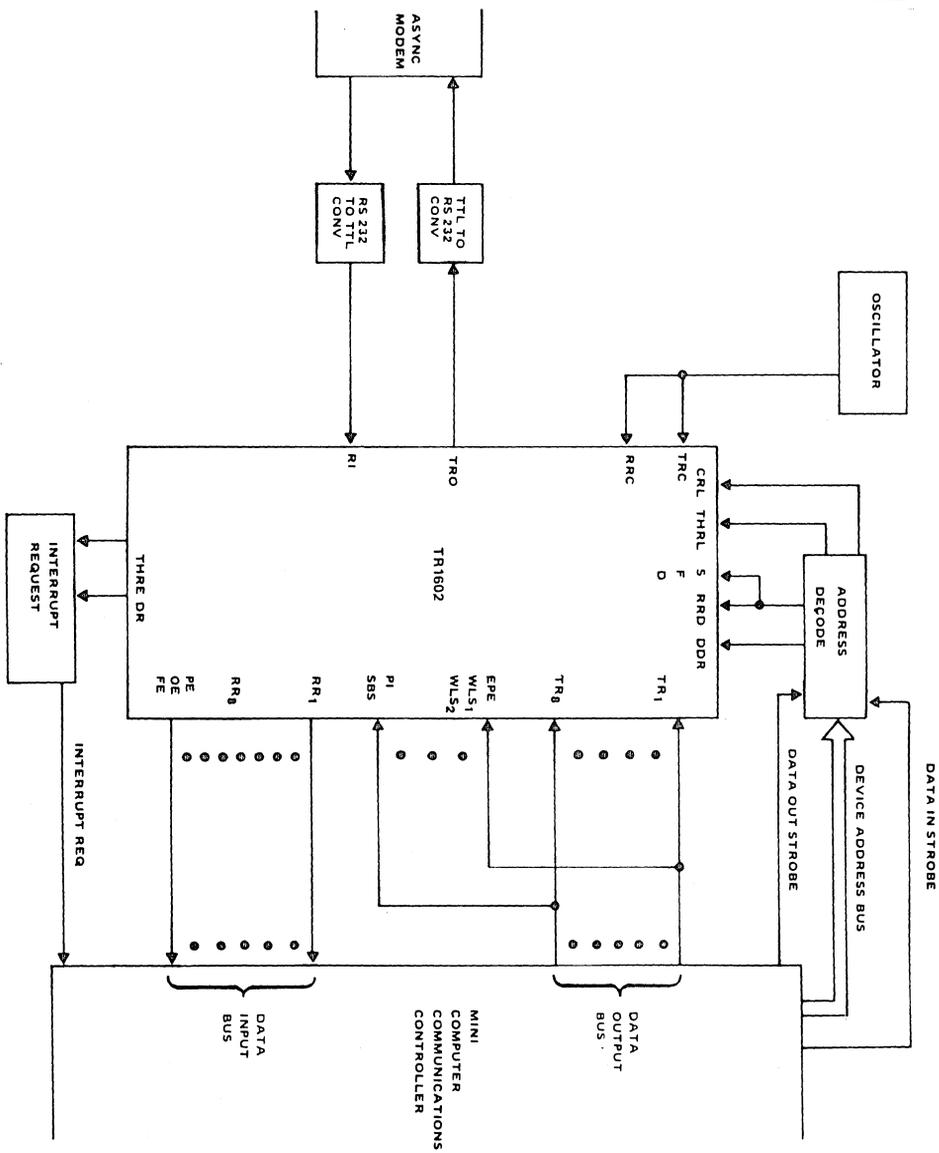


Figure 12 Typical Minicomputer Interface

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C O R P O R A T I O N

WD1931/WD1933 COMPATIBILITY APPLICATION NOTES

By Jan E. Rovall

SECTION 1

MARCH, 1981

INTRODUCTION

The purpose of this document is to provide the reader with information about the WD1931 and WD1933 devices, and how to take advantage of their compatibility. Various applications examples are given showing flowcharts and timing diagrams. As the devices are designed for use in a very large range of applications, many different features are described and illustrated for the benefit of the reader.

For detailed product information such as A.C. and D.C. parameters, please refer to the respective data sheets.

GENERAL DESCRIPTION

The WD1931 and the WD1933 are MOS/LSI devices which interface a parallel digital system to a serial data communication channel (and vice versa). Both circuits are capable of simplex, duplex, and full duplex operation.

The WD1931 is designed for character-oriented asynchronous and/or synchronous (BI-SYNC) protocols. The WD1933 is designed for bit-oriented SDLC, HDLC and ADCCP protocols. The devices are programmable and compatible to most 8-bit microcomputers on the market. The pin assignments of these two devices have been chosen to allow the user to implement a one-board multiprotocol design. This board may then be used for any of the above mentioned protocols, by choosing the proper device (WD1931 or WD1933) and connecting some jumpers (see paragraph entitled "Multiprotocol Board Design"). The purpose of these circuits are to convert parallel data from a computer or terminal to a serial data stream at one end of a communication channel. At the other end of the channel, the data is converted back to the original parallel data.

Serial data communications minimizes the number of physical channels required to transfer data and therefore reduces the cost to send data between two (or more) distant points. A microcomputer could perform the same serial/parallel conversion function as these devices, but at much slower speeds. However, using the WD1931 and WD1933 devices to do this function is much more efficient. This makes the computer free to perform other tasks during transmission

and reception. The only work that the computer is required to do is to initialize the WD1931 or WD1933, and the devices take care of the serialization or deserialization of data, plus control and timing.

Some control signals on the computer side of the devices are needed for read, write, and control purposes. Additional signals can also be used for special purposes or modes for the convenience of the user. Typically, these other control signals are used to enable communication with a modem or DCE (Data Communications Equipment).

Interrupt outputs are provided to inform the microcomputer when to retrieve from, or to provide data to the holding registers. Also, interrupts can be generated to provide status information such as changes in modem control lines, or that events such as Transmission Complete or Received End of Message have occurred.

SYSTEM APPLICATIONS

WD1931/33 may be used in the following applications:

- Switched network
- Multipoint network
- Non-switched point to point network
- Simplex, half-duplex, or full duplex
- Asynchronous or synchronous communication
- Message switching
- Multiplexing systems
- Data concentrator systems
- Loop data link systems
- DMA applications
- Parallel to serial data conversion (and vice versa)
- Local Networks
- Packet Switching
- X.25
- Multidrop line systems

A typical block diagram of a data link is shown in Figure 1. The communication media used could be a direct communication channel (such as a leased telephone line), a switched telephone line, or one of many other possibilities. Typically these applications would require the use of a modem.

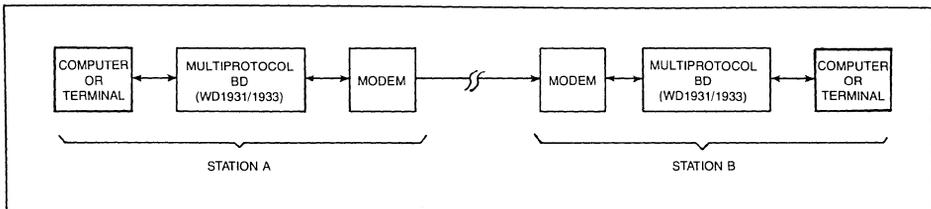


Figure 1 DATA LINK BLOCK DIAGRAM

The applications that these devices could be used in would be a combination of the previously mentioned. A modem would be needed for long distance communication lines. For shorter distance, line drivers/receivers may be sufficient. In some very well controlled environments, such as a laboratory, two devices may be connected without line drivers and receivers.

The WD1931 or WD1933 may be connected directly to a microcomputer bus, but buffers would normally be recommended. Figure 2 shows a typical schematic of an interface

between a Z80 microcomputer and a modem. This is called a multiprotocol board, which is described later in this document.

Some examples of various WD1931/WD1933 systems are shown here by use of block diagrams. The station shown in Figure 3 consists of a computer or terminal, a multiprotocol board, and a modem. A station may consist of only the computer or terminal, and one WD1931 or WD1933 device. Whether the modem, line drivers and receivers, or CPU buffers are needed depends on the details of the particular design situation.

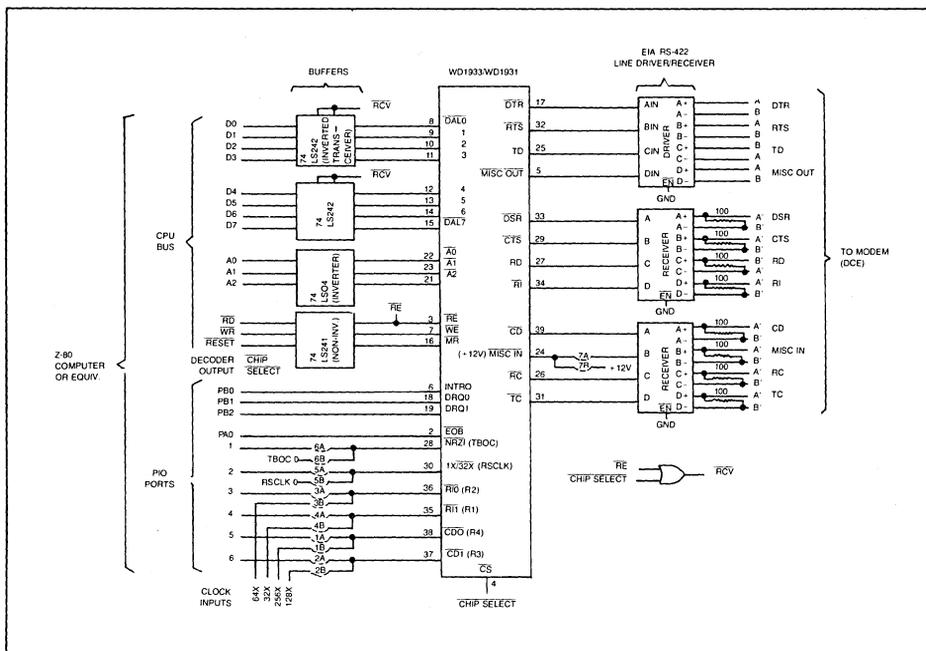
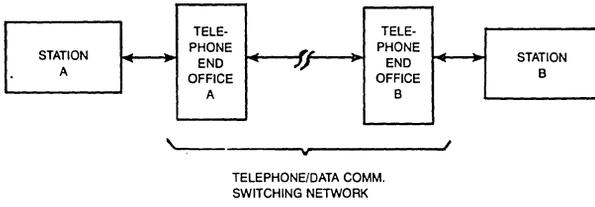
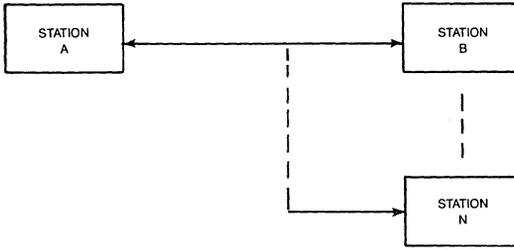


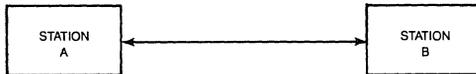
Figure 2 WD1931/1933 AND MICROCOMPUTER. (MULTIPROTOCOL BOARD)



SWITCHED NETWORK



MULTIPOINT NETWORK



NONSWITCHED POINT TO POINT NETWORK

Figure 3 TYPICAL NETWORKS

LOOP DATA LINK SYSTEM

The Loop Mode is used in SDLC only. A loop data link system consists of one primary station (Loop Controller), and a number of secondary stations all functioning normally as repeaters. Figure 4 illustrates a typical Loop Data Link system.

Any secondary station finding its address in the address field captures the frame for action at that station. All received frames are relayed to the next station down the loop.

A secondary station is allowed to suspend the repeater function and initiate its transmission when a Go-Ahead pattern is received.

DATA COMMUNICATIONS EXAMPLE NO. 1

The diagrams below (Figures 5 and 6) illustrate a typical digital system employing several processing levels and digital communications protocols. It is flexible enough to satisfy several applications. For example, the host processor and remote terminals could be located in airline reservation offices and ticket counters, travel centers and travel agencies, central bank offices and branch banks, or department stores and individual cash registers. The exploded diagram of the Data Communications Controller exemplifies the use of one common circuit board design with eight multiprotocol circuits. When one port requires a character-oriented protocol (asynchronous, character oriented synchronous, or bisync), the WD1931 is installed into the appropriate socket. For SDLC, HDLC or ADCCP, the WD1933 is used.

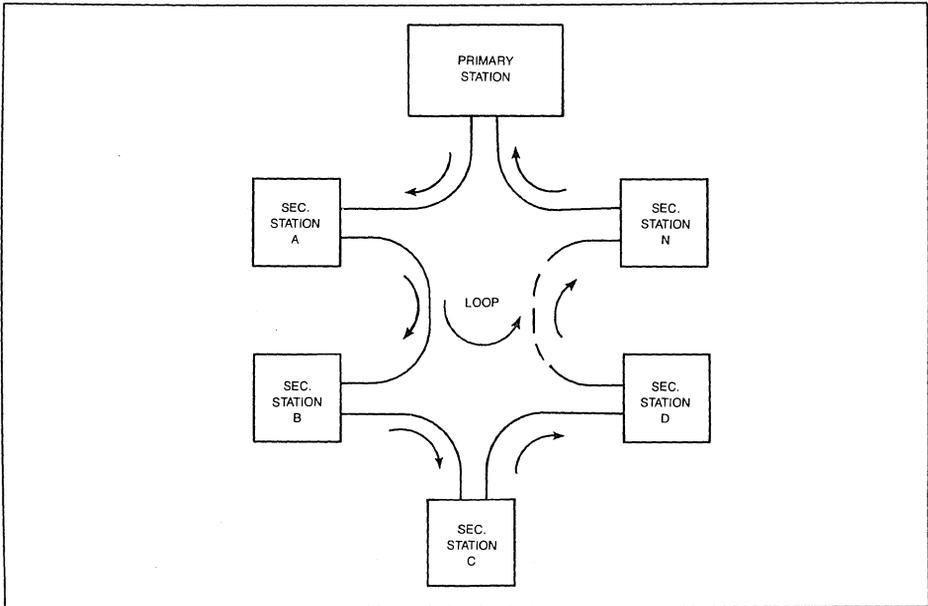


Figure 4 LOOP DATA LINK SYSTEM

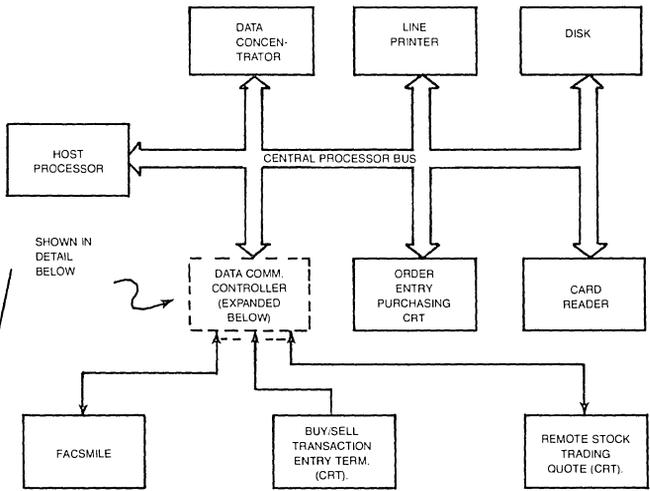


Figure 5. STOCK BROKERAGE SYSTEM

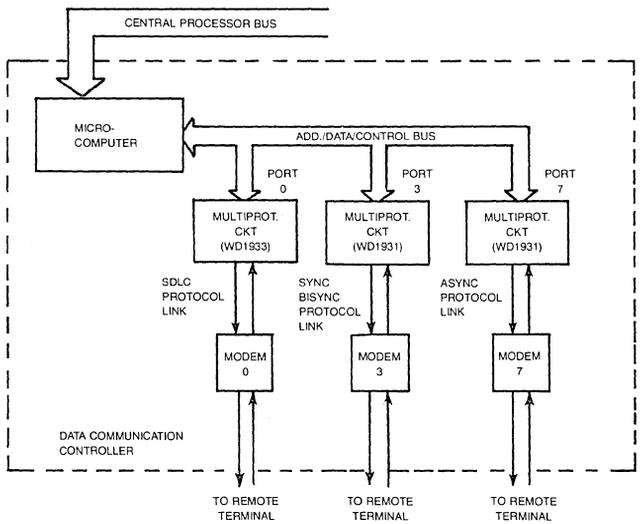


Figure 6 DATA COMMUNICATION CONTROLLER

DATA COMMUNICATIONS EXAMPLE NO. 2

Figure 7 illustrates a Host Computer that communicates through modems to a multiprotocol board. This in turn collects information from many remote stations through a Data Concentrator.

DATA COMMUNICATIONS EXAMPLE NO. 3

A simplified HDLC point to point connection is shown in Figure 8. In this example, no buffers or line drivers and receivers are used.

Figure 9 represents a more "real world" application with the use of modems through a communications channel.

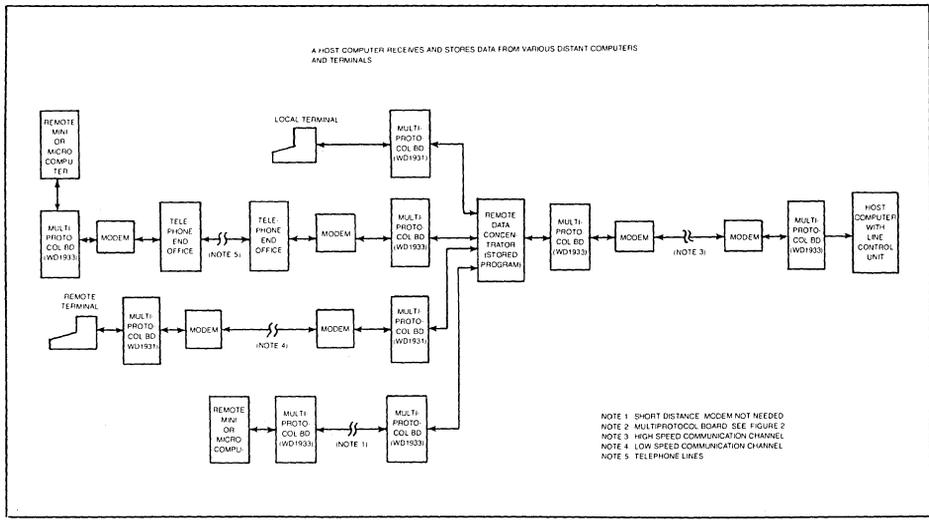


Figure 7 DATA CONCENTRATOR

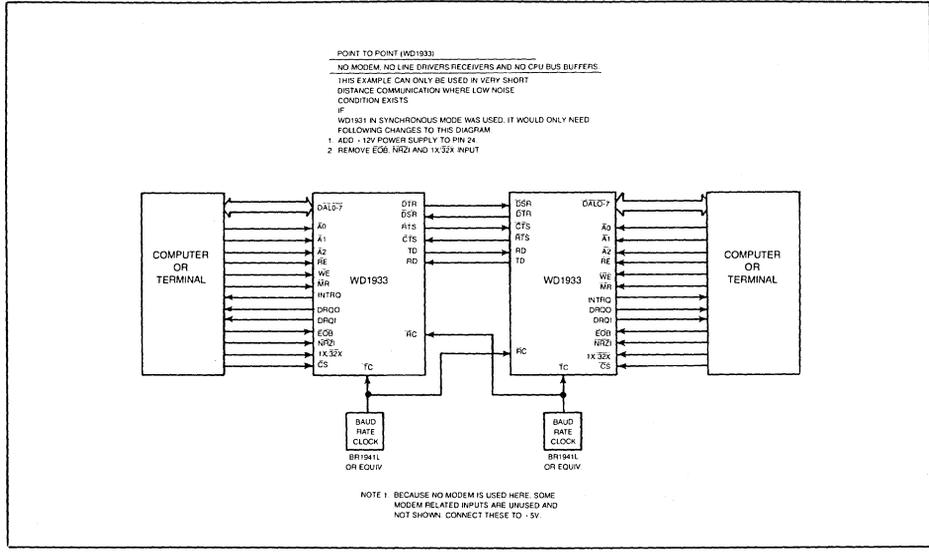


Figure 8 HDLC POINT TO POINT

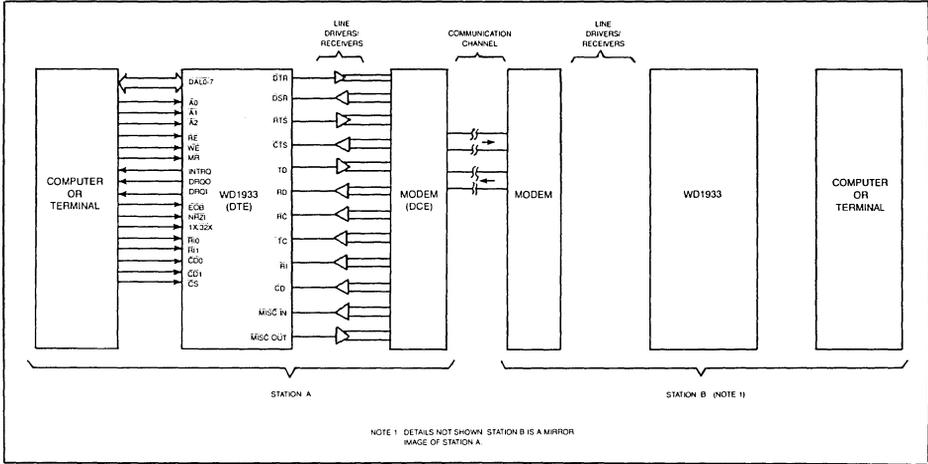


Figure 9 HDLC POINT TO POINT WITH MODEM

WD1931 AND WD1933 TECHNICAL DESCRIPTIONS

The WD1931 and WD1933 devices have been designed to provide a high degree of compatibility and interchangeability. The pin-outs are similar, and the register operations are software compatible. This feature allows for the use of either device in a given socket.

WD1931 PIN-OUTS AND BLOCK DIAGRAM

The WD1931 pin assignments and the block diagram are shown in Figure 10.

WD1933 PIN-OUTS AND BLOCK DIAGRAM

The WD1933 pin assignments and the block diagram are shown in Figure 11.

SHORT FORM REGISTER FORMAT AND ADDRESSING

Information concerning operating modes and status conditions are passed to and from the WD1931 or WD1933 device through I/O addressable registers. Each register contains eight bits, where each bit represents a specific function and has its own mnemonics.

The state of each bit is represented by a "1" for TRUE and a "0" for FALSE. This may or may not correlate to a measurable voltage level at a pin, since some pins are TRUE when they are at 0 volts (this is indicated by a bar over the name, or a slash immediately preceding the name).

The WD1931 registers are shown in Figure 12. Note that some bits are affected by the transmit clock (\overline{TC}) rate or the receive clock (\overline{RC}) rate.

The WD1933 registers are shown in Figure 13. Note that some bits are affected by the transmit clock (\overline{TC}) rate or the receive clock (\overline{RC}) rate.

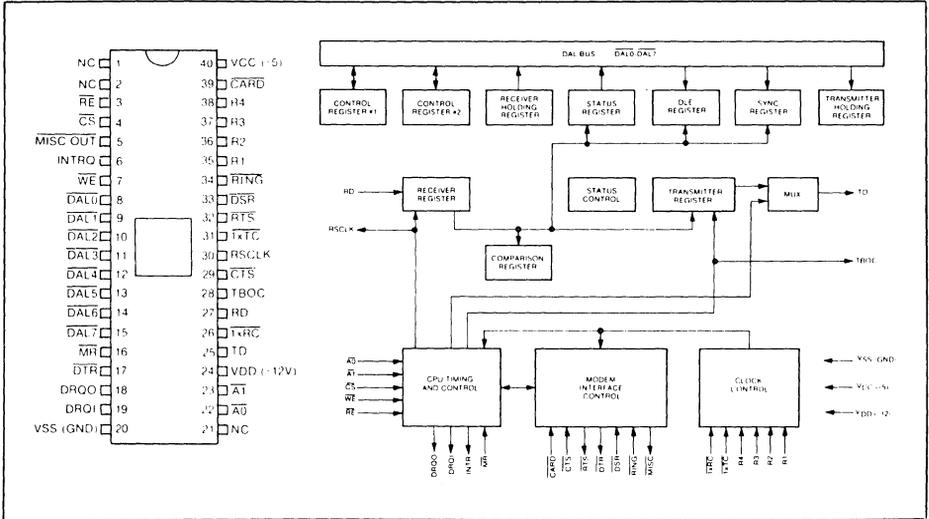


Figure 10 WD1931 PIN CONNECTIONS AND BLOCK DIAGRAM

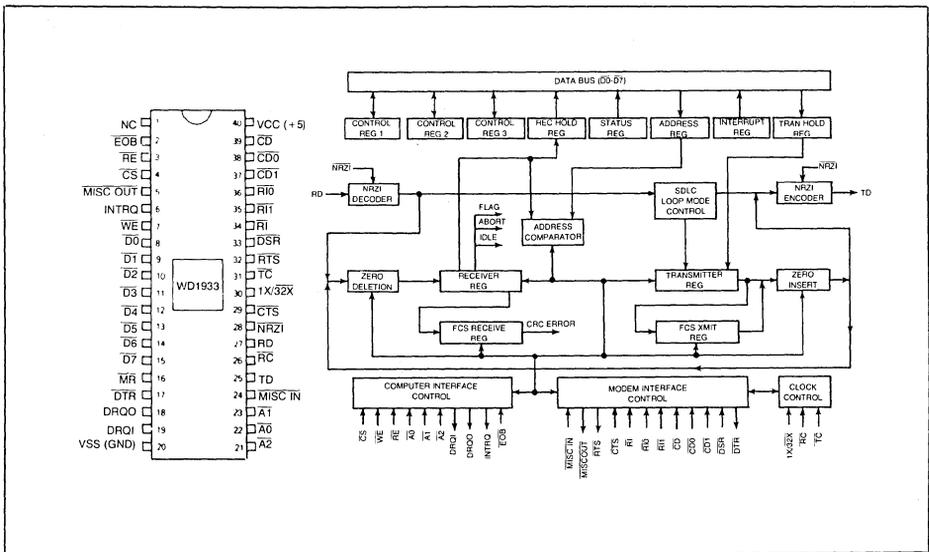
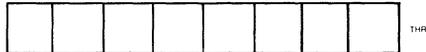
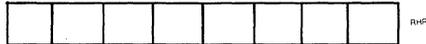
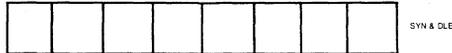
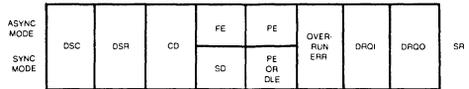
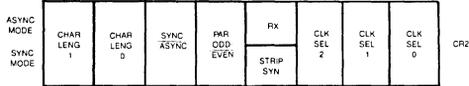
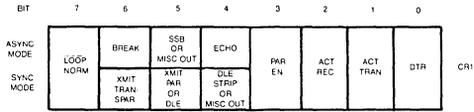


Figure 11 WD1933 PIN CONNECTIONS AND BLOCK DIAGRAM

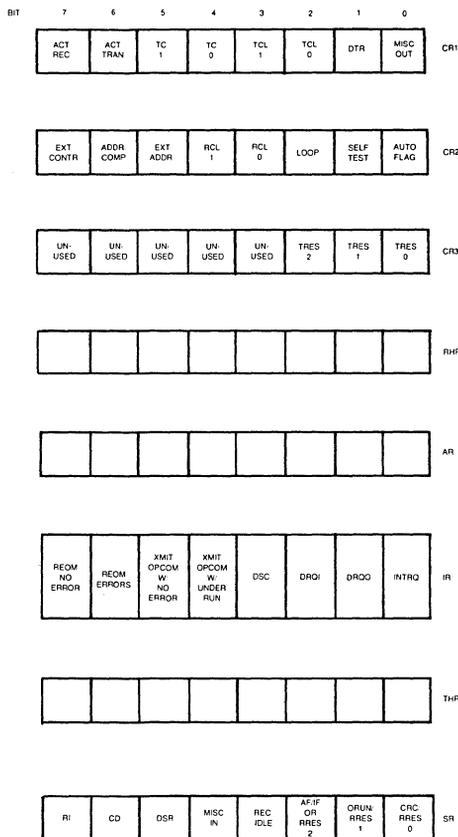


WD1931 BIT ASSIGNMENTS

$\overline{A1}$	$\overline{A0}$	READ	WRITE	CLOCK
LO	LO	CR1	CR1	NONE
LO	HI	CR2	CR2	NONE
HI	LO	SR	SYN & DLE	SR0 = \overline{TC} . SR1-4 = \overline{RC} . SR5-7, SYN, DLE = NONE
HI	HI	RHR	THR	RHR = \overline{RC} . THR = NONE

WD1931 REG. ADDRESSES AND CLOCKS

Figure 12 WD1931 REGISTERS



WD1933 BIT ASSIGNMENTS

$\overline{A2}$	$\overline{A1}$	$\overline{A0}$	READ	WRITE	CLOCK
HI	HI	HI	CR1	CR1	NONE
HI	HI	LO	CR2	CR2	NONE
HI	LO	HI	CR3	CR3	NONE
HI	LO	LO	RHR	AR	$RHR = \overline{RC}$. AR = NONE
LO	HI	HI	IR	THR	$IR = \overline{TC}$. THR = NONE
LO	HI	LO	SR	—	$SR0-3 = \overline{RC}$. SR4-7 = NONE

WD1933 ADDRESSES AND CLOCKS

Figure 13 WD1933 REGISTERS

MULTIPROTOCOL BOARD DESIGN

The WD1931 and WD1933 pin assignments were chosen so that a circuit board designer may use only one 40-pin socket, but have the choice of using either device on that board. Depending on the application, a few jumper wires may be needed, or perhaps none at all. Figure 2 shows a typical example of a multiprotocol board. This board may be designed with even less components and jumpers, dependent on the particular application it is intended for.

Jumpers 1A-7A are to be connected when WD1933 and all its options are used. Jumpers 1B-7B are to be connected when WD1931 and all its options are used.

For example, if the user does not need the NRZI signal mode, the 1X clock is only used, no Ring or Carrier Detect indication is needed, TBOC, RSCLK and MISC IN are not used, and then no jumpers are needed in the design. In this case, pin 24 may be permanently connected to +12V. Pins

28 and 30 may be connected to +5V via a 10K resistor, and pins 35 through 38 may be connected directly to +5V.

TRANSMISSION AND RECEPTION EXAMPLES

TRANSMISSION EXAMPLE 1 (ONE FRAME)

A typical sequence of events is shown here to transmit a message from computer A to another computer (or terminal) B. Through a switched network the message to be sent is a synchronous SDLC protocol frame as shown below in Figure 14. For simplicity, the message sent in this example is very straightforward and short.

Line drivers and receivers are used, permitting transmission to a remote DCE or modem (see schematic in Figure 2). As the SDLC frame is sent, the WD1933 is used. The jumpers required are 1A-7A. Figure 15 illustrates the functional flow, and Figure 16 details the timing of the transmitted frame. Note that the device can be programmed in several different ways to allow for various requirements.

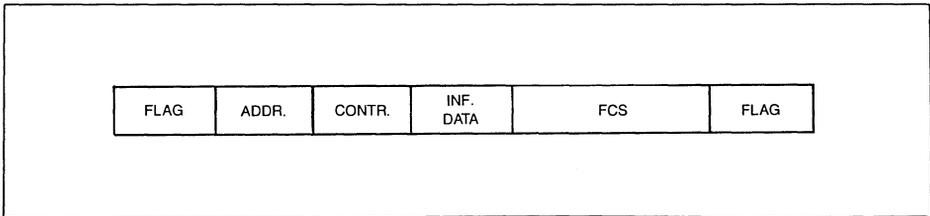


Figure 14 SDLC FRAME FORMAT

FLOW CHART

INTERRUPT MODE

AUTO FLAG

INF. DATA = 8 BITS (8-BIT CHARACTER WITH NO RESIDUAL BITS)

TC COMMAND IS USED TO INITIATE FCS.

INITIATE

TRANSMIT MODE

DTE AND DCE IDLE

PORT A = OUTPUT
PORT B = INTERRUPT
INPUT

AUTO FLAG
DATA TERM. READY

COMPUTER DOING
OTHER TASKS

DATA SET READY
INTERRUPT NO. 1

DATA SET CHANGE
A

START

ACTIVATE
MR MOMENT.
CONFIGURE
PIO.

SET AUTO
FLAG AND
DTR

WAIT

INTERRUPT

READ IR.
ENABLE INT.

DSC = 1
?

ERROR

PA_{7:0} = 0111 1111
PBO/PB1 (INTRQ/DRQO) = INTERRUPTS

CR_{3:0} = 0000 0000
CR_{2:0} = 0000 0001
CR_{1:0} = 0000 0010

Figure 15 FLOW DIAGRAM OF FRAME TRANSMISSION

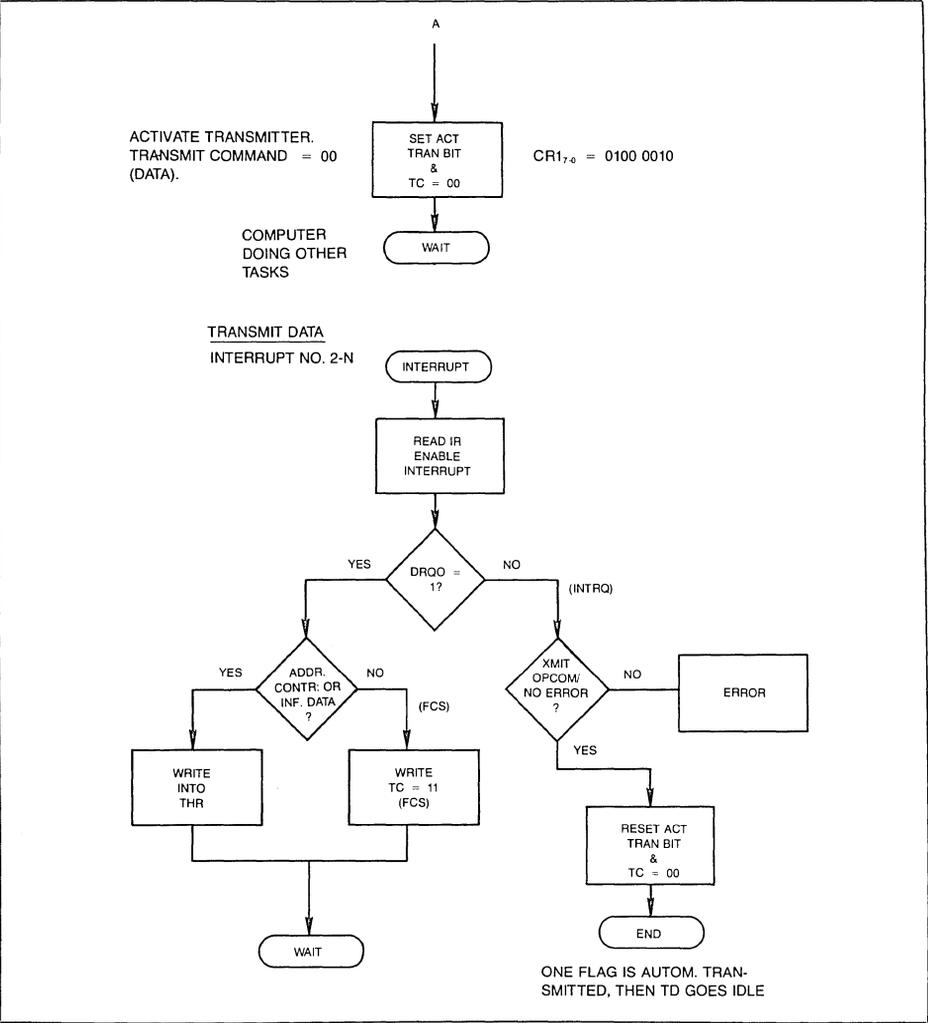


Figure 15 FLOW DIAGRAM OF FRAME TRANSMISSION

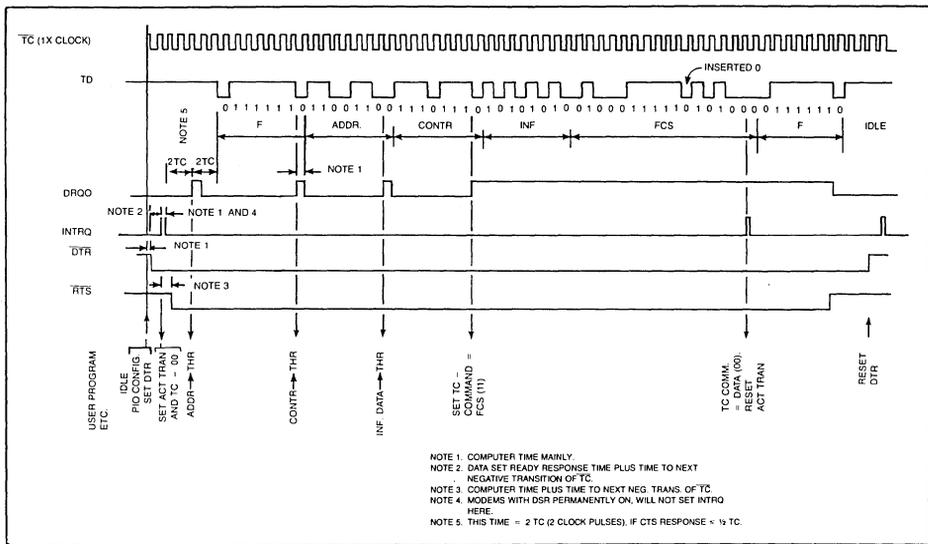


Figure 16 TIMING DIAGRAM OF FRAME TRANSMISSION

WD1933 TRANSMISSION EXAMPLE 2 (DMA APPLICATION)

The WD1933 is very efficient for DMA applications. The control registers are loaded to initiate the WD1933 for DMA mode in the same way as in Transmission Sample 1. The Auto Flag bit is set, and the Transmitter Command is "DATA" (CR14 and CR15 bits = 00). The procedure to set up the link (initiate transmit mode and data set ready) is the same as in Transmission Sample 1. When INTRQ is set and the Transmitter is activated, the DMA Controller Board takes over control. From this time on, the DMA Controller Board responds on every DRQO (Data Request Out). When the last

character is transmitted, the INTRQ is received, and the control is switched back over to the CPU.

A very important feature of the WD1933 is the EOB (End of Block) input. Instead of using the normal (time-consuming) method of writing into a control register to start the FCS (Frame Check Sequence), the EOB input is activated at this time. At the next occurrence of INTRQ the EOB signal is deactivated.

An example of a schematic/block diagram is shown in Figure 17, and a timing diagram is shown in Figures 18 through 20.

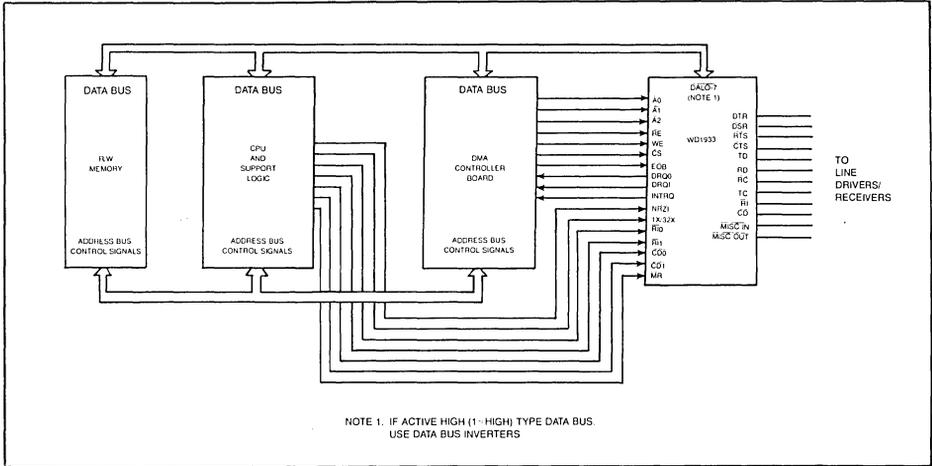


Figure 17 BLOCK DIAGRAM OF DMA APPLICATION

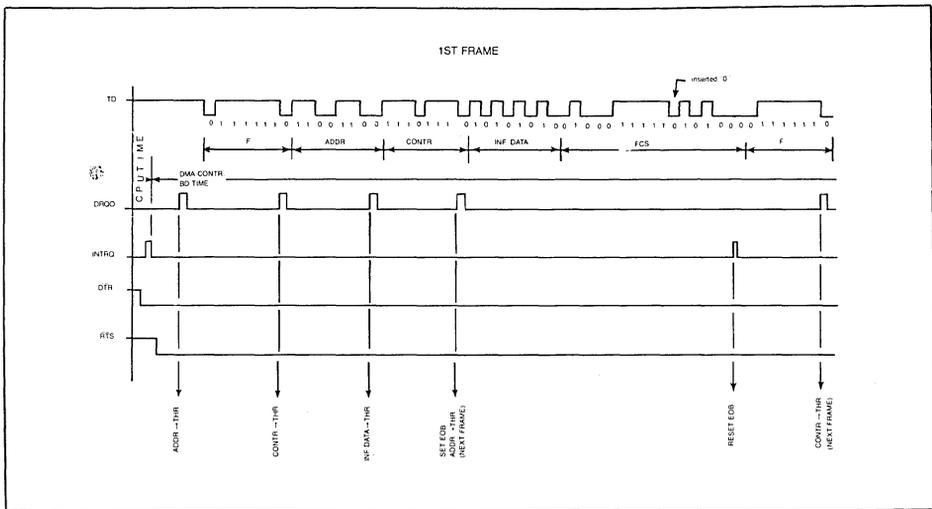


Figure 18 DMA TIMING OF FIRST FRAME

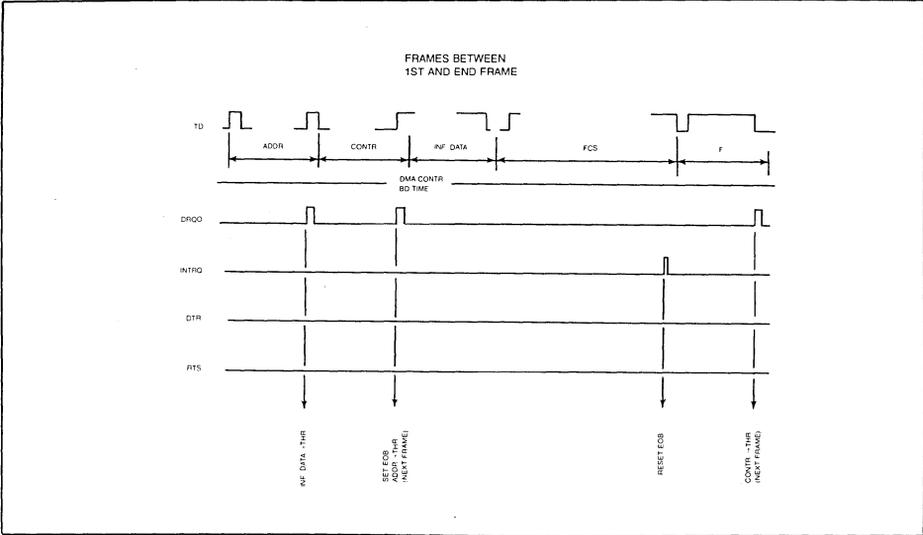


Figure 19 DMA TIMING OF MIDDLE FRAMES

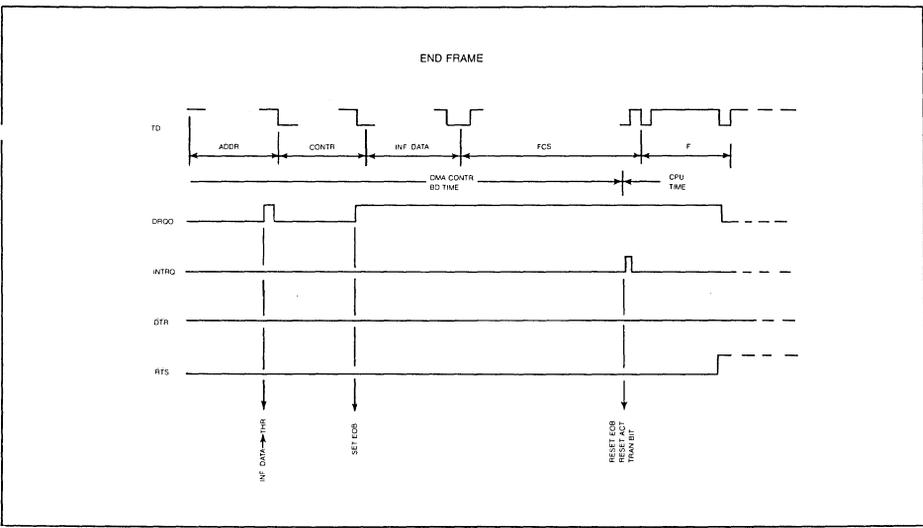


Figure 20 DMA TIMING OF LAST FRAME

WD1933 RECEPTION EXAMPLE 1

A sequence of events is shown in illustrating how to receive a message with the WD1933 device. For simplicity, the same SDLC frame structure is used as in Transmission Example 1. Also, please refer to the same interface circuitry shown in Figure 2.

Figure 21 illustrates the functional flow, and Figure 22 contains the timing information.

WD1933 RECEPTION EXAMPLE 2

This example shows a frame with two ADDRESS characters, two CONTROL characters, one 5-bit INFORMATION DATA

character, and two residual bits. This example may not be a typical frame, but it shows how the WD1933 works in a wide range of frame structures.

The first FLAG and FCS are not shown in detail, and are not critical to this example.

Figure 23 illustrates the functional flow, and Figure 24 contains the timing information.

WD1933 LOOP DATA LINK EXAMPLE

This example shows how to program a secondary station to function in Loop mode. The functional flow is illustrated in Figure 25, and the interface circuit is shown in Figure 2.

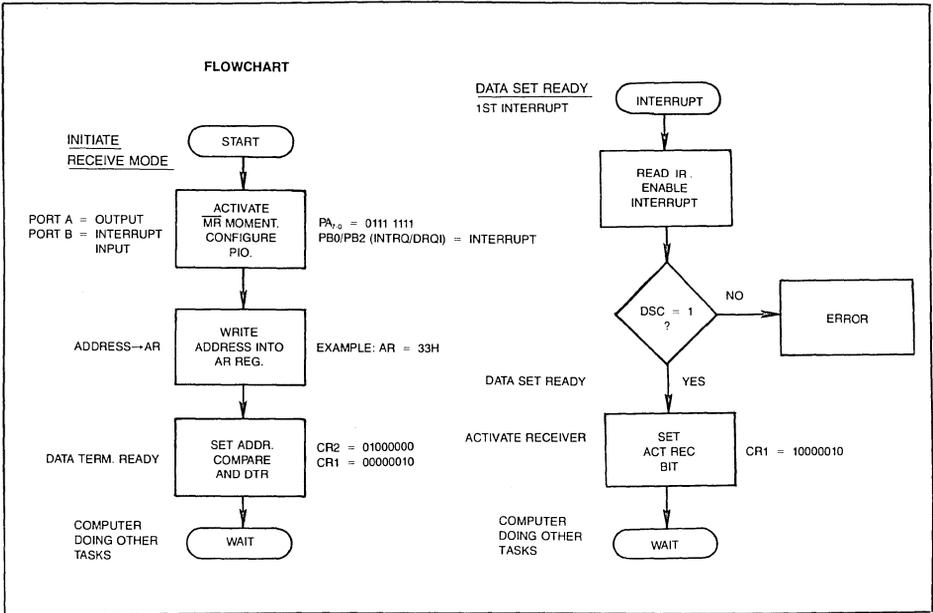


Figure 21 FLOW DIAGRAM OF FRAME RECEPTION (EXAMPLE NO. 1)

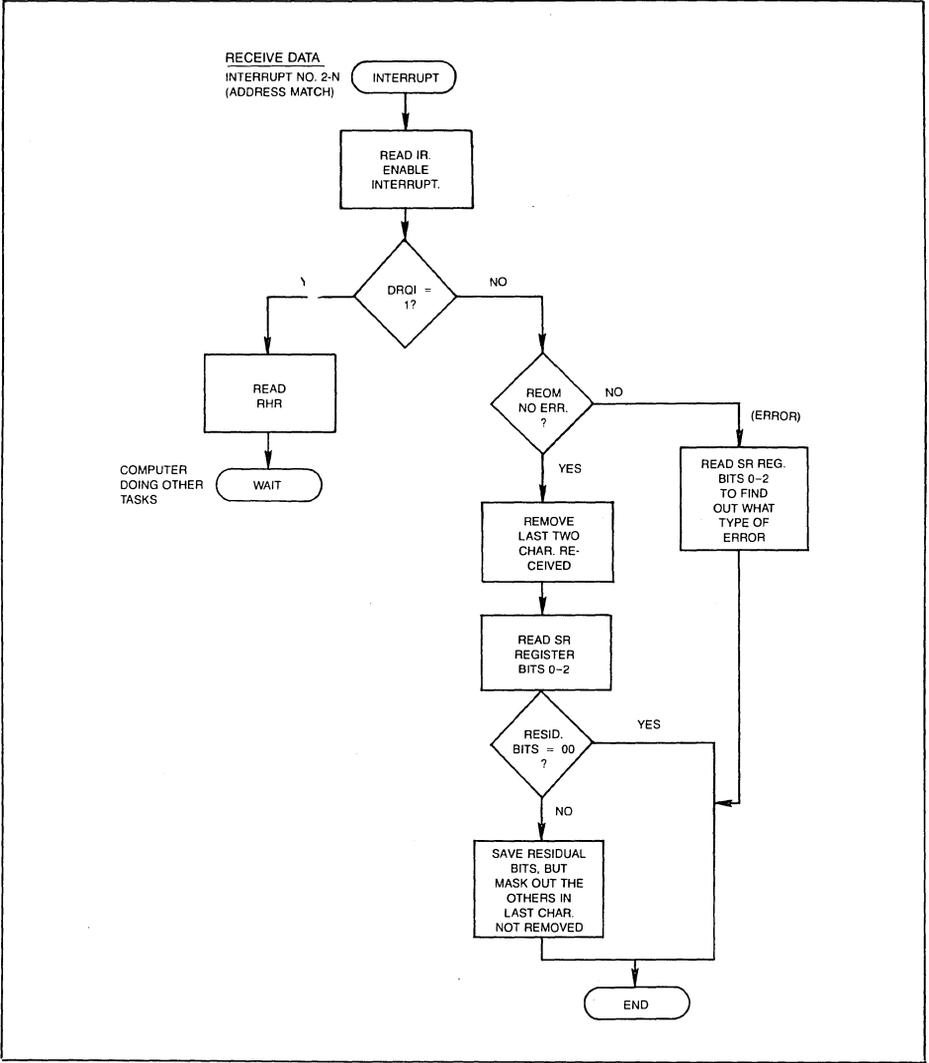


Figure 21 FLOW DIAGRAM OF FRAME RECEPTION

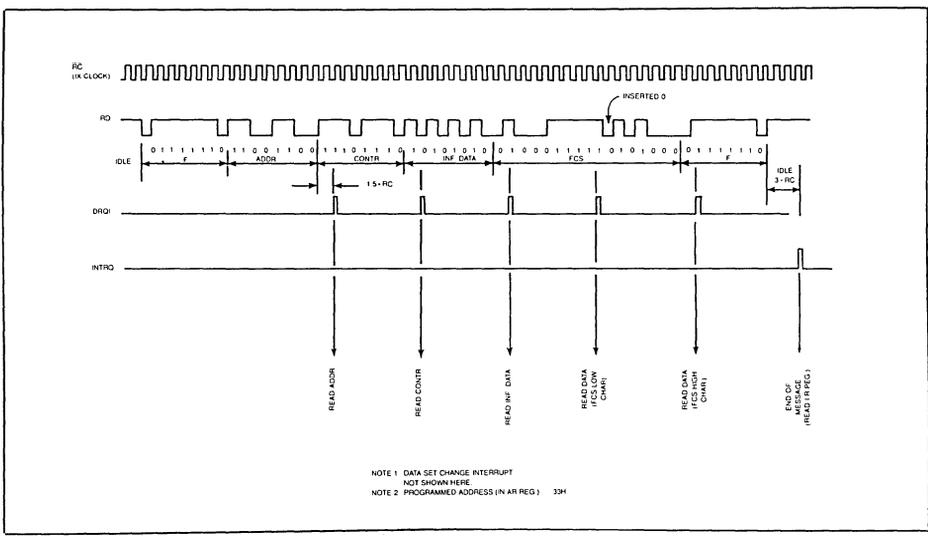


Figure 22 TIMING DIAGRAM OF FRAME RECEPTION (EXAMPLE NO. 1)

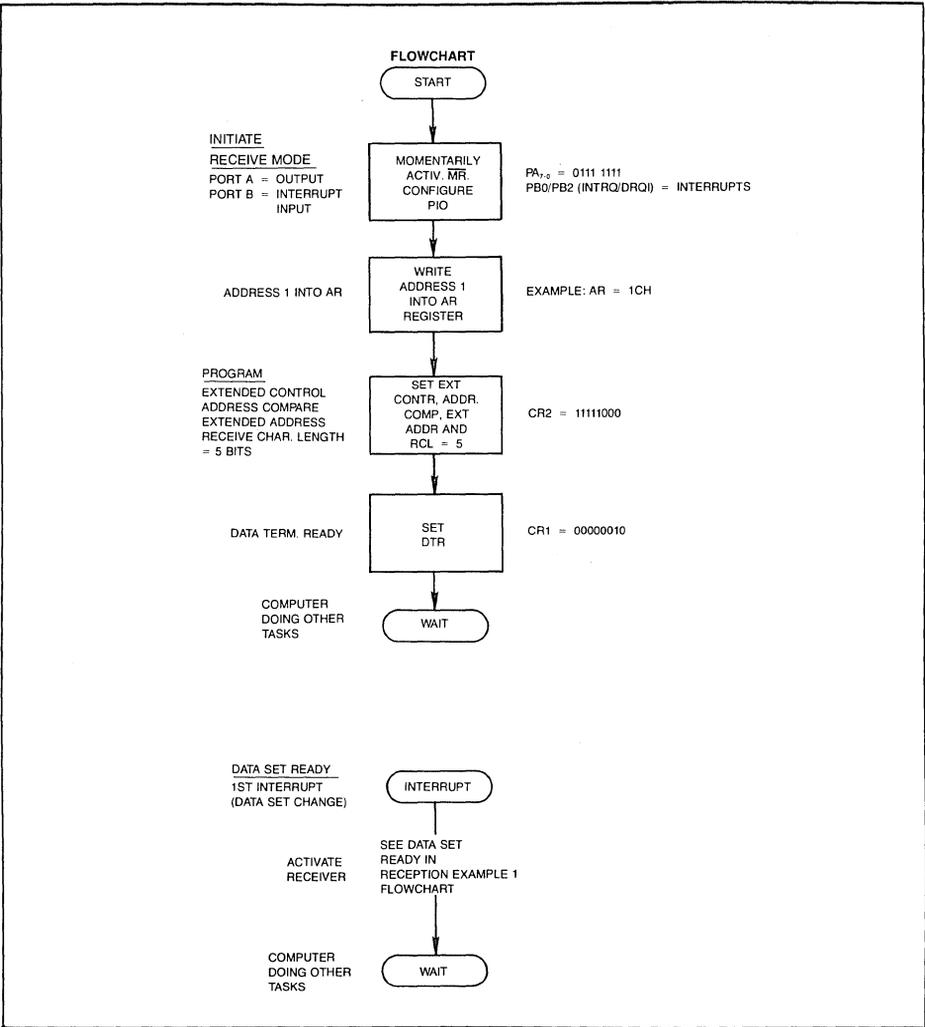


Figure 23 FLOW DIAGRAM OF FRAME RECEPTION (EXAMPLE NO. 2)

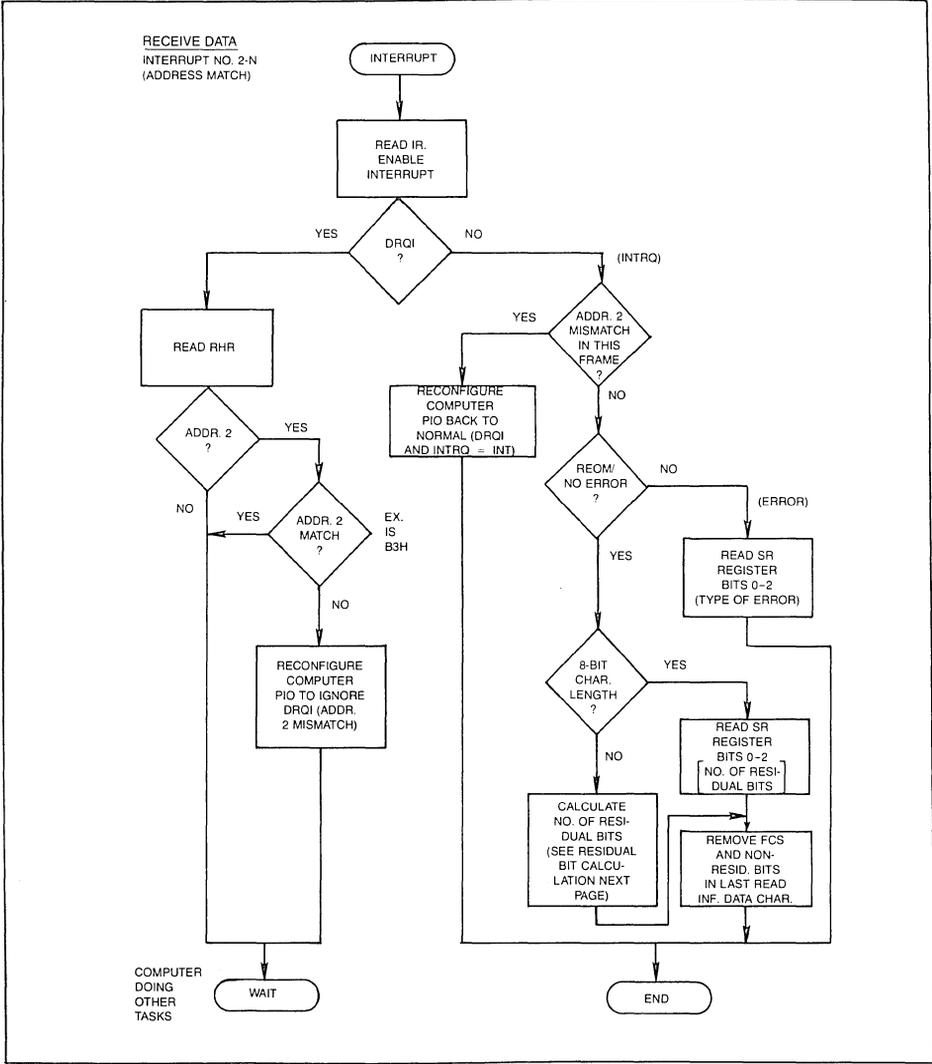


Figure 23 FLOW DIAGRAM OF FRAME RECEPTION

RESIDUAL BIT CALCULATION
 THIS CALCULATION
 NEEDED ONLY WHEN
 RESIDUAL BITS MAY BE
 RECEIVED IN A
 NON-8-BIT CHARACTER

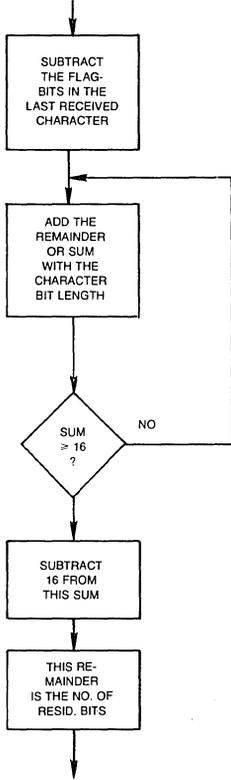


Figure 23 FLOW DIAGRAM OF FRAME RECEPTION

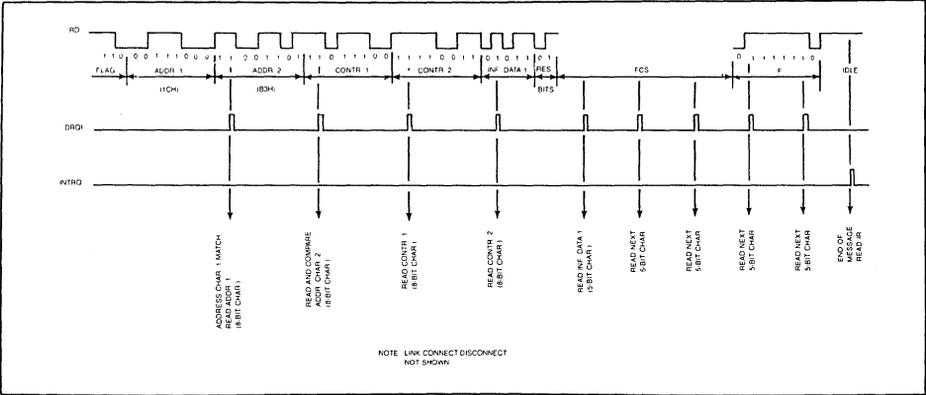


Figure 24 TIMING DIAGRAM OF FRAME RECEPTION (EXAMPLE NO. 2)

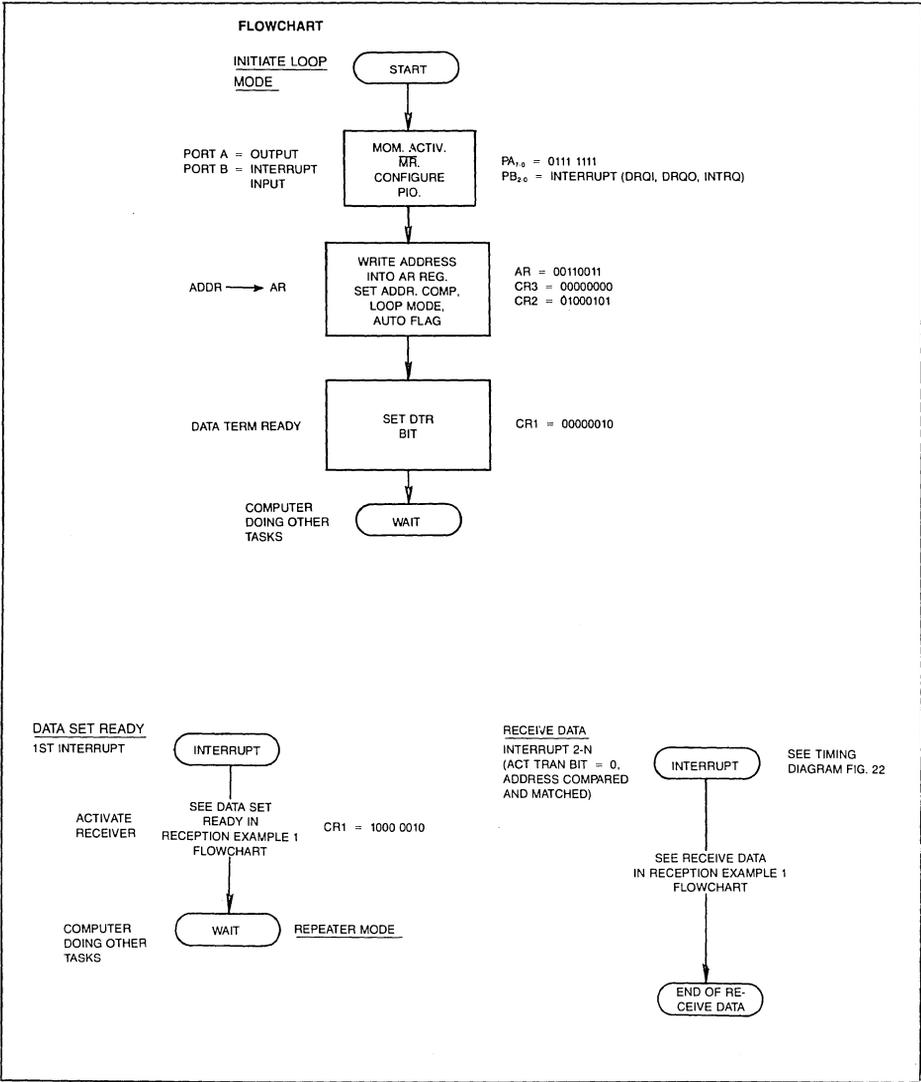


Figure 25 FLOW DIAGRAM OF LOOP MODE OPERATION

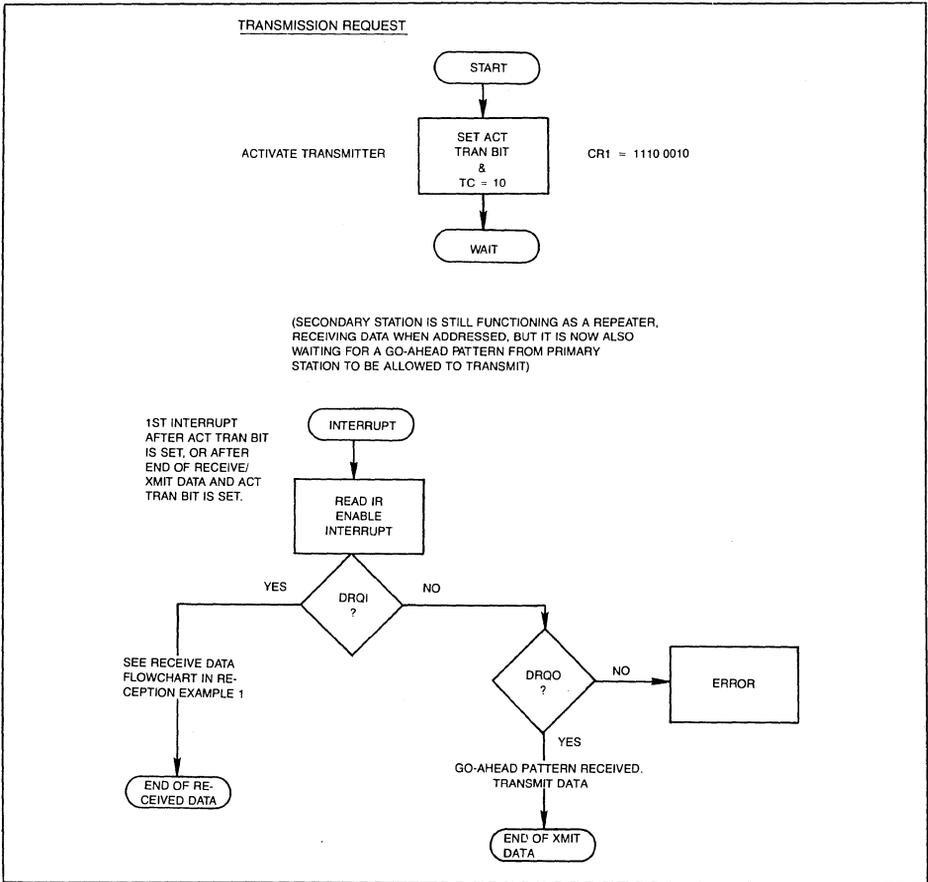


Figure 25 FLOW DIAGRAM OF LOOP MODE OPERATION

CONCLUSION

The WD1931 and WD1933 devices are highly compatible, which allows the design of a multiprotocol communications board. This compatibility allows the use of asynchronous, character oriented synchronous, and bit oriented synchronous communications protocols with the same 40 pin socket.

APPENDIX

RELATED DOCUMENTS

- WD1931 Data Sheet, Western Digital Corporation
- WD1933 Data Sheet, Western Digital Corporation

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CORPORATION

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Security Products Data Sheets

WD2001/WD2002 Data Encryption Devices

WESTERN DIGITAL

AUGUST, 1980

FEATURES

- CERTIFIED BY NATIONAL BUREAU OF STANDARDS.
- TRANSFER RATE: 1.3M BITS/SEC (2 MHz CLOCK) (HIGHER SPEEDS AVAILABLE)
- ENCRYPTS/DECRYPTS 64 BIT DATA WORDS USING 56 BIT KEY WORD
- SINGLE PORT 28 PIN PACKAGE WD2001 OR DUAL PORT 40 PIN PACKAGE WD2002
- COMMAND BIT PROGRAMMING VIA DAL BUS OR INPUT PINS
- DMA COMPATIBLE (SEE WESTERN DIGITAL DM1883)
- PARITY CHECK ON KEY WORD LOADING
- STANDARD 8 BIT MICROPROCESSOR INTERFACE
- INPUTS AND OUTPUTS TTL COMPATIBLE
- KEY STORED ON CHIP IS NOT EXTERNALLY ACCESSIBLE
- SEPARATE CLEAR AND CIPHER BUS STRUCTURE ON WD2002

APPLICATIONS

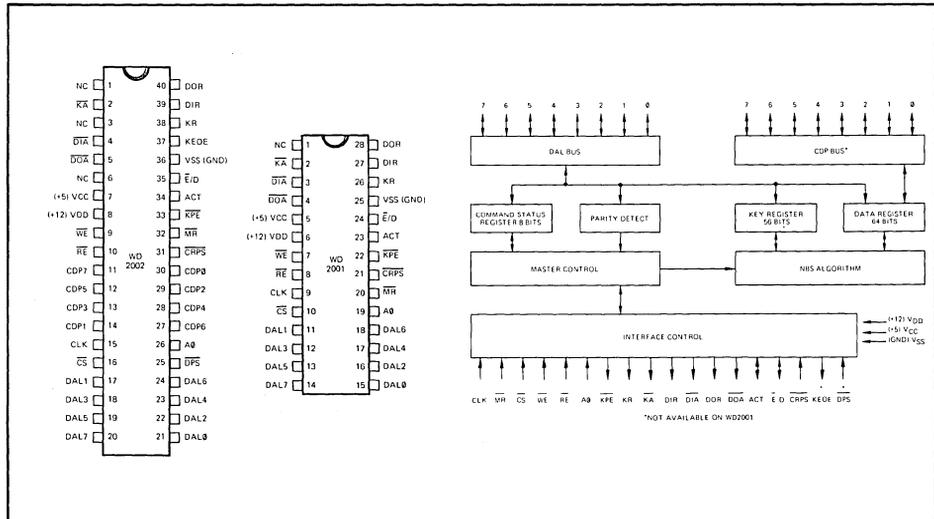
- SECURE BROKERAGE TRANSACTIONS
- ELECTRONIC FUNDS TRANSFERS
- SECURE BANKING/BUSINESS ACCOUNTING
- MAINFRAME COMMUNICATIONS

- REMOTE AND HOST COMPUTER COMMUNICATIONS
- SECURE A/D
- SECURE DISK OR MAG TAPE DATA STORAGE
- SECURE PACKET SWITCHING TRANSMISSION

GENERAL DESCRIPTION

The Western Digital WD2001 and WD2002 Data Encryption/Decryption devices are designed to encrypt and decrypt 64-bit blocks of data using the algorithm specified in the Federal Information Processing Data Encryption Standard (#46). These devices encrypt a 64-Bit clear text word using a 56-Bit user-specified key to produce a 64-Bit cipher text word. When reversed, the cipher text word is decrypted to produce the original clear text word.

The DE2001/2 are fabricated in N-channel silicon gate MOS technology and are TTL compatible on all inputs and outputs.



WD2001/WD2002 BLOCK DIAGRAM

PIN OUTS

PIN NO.		PIN NAME	SYMBOL	FUNCTION
WD2001	WD 2002			
11-18	17-24	DATA LINES	DAL \emptyset → DAL 7	Eight active true three-state bi-directional I/O lines used for information transfer to and from the DES chip's registers. During single port operation, all COMMAND/STATUS, KEY WORD and DATA WORD transfers are via this bus. During dual port operation, all COMMAND/STATUS, KEY WORD and <u>clear</u> DATA WORD transfers are via this bus. (<u>Cipher</u> DATA WORD transfers are via the CIPHER DATA PORT (CDP) bus.)
N/A	11-14 27-30	CIPHER DATA PORT	CDP \emptyset → CDP 7	Eight active true three-state bi-directional I/O lines used <u>only</u> in dual port operation. <u>Cipher</u> DATA WORD transfers are via this bus. These pins are available on the WD2002 40 pin package version <u>only</u> .
6	8	POWER SUPPLY	VDD	+ 12v
5	7	POWER SUPPLY	VCC	+ 5v
25	36	GROUND	VSS	GROUND
9	15	CLOCK	CLK	System clock input.
21	32	MASTER RESET	MR	MR active low resets the COMMAND/STATUS REGISTER and resets internal circuitry. (Requires active clock for reset operation.)
10	16	CHIP SELECT	\overline{CS}	\overline{CS} is made low to access registers within the device.
8	10	READ ENABLE	\overline{RE}	The contents of the selected register are placed on the DAL (or CDP) bus lines when \overline{CS} and \overline{RE} are made low.
7	9	WRITE ENABLE	\overline{WE}	Information on the DAL (or CDP) bus lines is written into the selected DES register when \overline{CS} and \overline{WE} are made low.
19	26	A \emptyset	A \emptyset	When this input is active high (during \overline{CS} active) the COMMAND/STATUS REGISTER is addressed. (A \emptyset active high will override internally generated addressing of the KEY and DATA REGISTERS as described on page 6.) This input is ignored when \overline{CRPS} is active.
26	38	KEY REQUEST	KR	This output is active high when the DES chip is requesting that a byte of the KEY WORD be written into the KEY REGISTER. (The KEY REGISTER is automatically addressed when KR is active, unless overridden by A \emptyset .)
2	2	KEY ACKNOWLEDGE	\overline{KA}	This output is active low when \overline{WE} is made low while the KEY REGISTER is addressed. (Can be used for handshake.)
27	39	DATA-IN REQUEST	DIR	This output is active high when the DES chip is requesting that a byte of the DATA WORD be written into the DATA REGISTER. (The DATA REGISTER is automatically addressed when DIR is active, unless overridden by A \emptyset .)
3	4	DATA-IN ACKNOWLEDGE	\overline{DIA}	This output is active low when \overline{WE} is made low while the DATA REGISTER is addressed. (Can be used for handshake.)

PIN NO.		PIN NAME	SYMBOL	FUNCTION
WD2001	WD2002			
28	40	DATA-OUT REQUEST	DOR	This output is active high when the DES chip is requesting that a byte of the DATA WORD be read from the DATA REGISTER. (The DATA REGISTER is automatically addressed when the DOR is active, unless overridden by A β .)
4	5	$\overline{\text{DATA-OUT}} \overline{\text{ACKNOWLEDGE}}$	$\overline{\text{DOA}}$	This output is active low when $\overline{\text{RE}}$ is made low while the DATA REGISTER is addressed. (Can be used for handshake.)
22	33	$\overline{\text{KEY PARITY ERROR}}$	$\overline{\text{KPE}}$	This output is active low when enabled via the COMMAND/STATUS REGISTER BIT 2 (KEOE) and a parity error has been detected during loading of the KEY REGISTER.
21	31	$\overline{\text{COMMAND REGISTER PIN SELECT}}$	$\overline{\text{CRPS}}$	This input selects DAL bus or input pin programming of the COMMAND/STATUS REGISTER. $\overline{\text{CRPS}}$ high or open selects DAL bus programming. $\overline{\text{CRPS}}$ low selects input pin programming.
23	34	ACTIVATE	ACT	When $\overline{\text{CRPS}}$ is high or open, this pin is an output reflecting the status of the ACTIVATE bit (bit 1) of the COMMAND/STATUS REGISTER. When $\overline{\text{CRPS}}$ is low, this pin is an input that overrides the ACTIVATE bit of the COMMAND/STATUS REGISTER.
N/A	37	KEY ERROR OUTPUT ENABLE	KEOE	This output indicates the status of the KEY ERROR OUTPUT ENABLE bit (bit 2) of the COMMAND/STATUS REGISTER. This output is active when input pin programming is selected ($\overline{\text{CRPS}}$ low). This pin is available on the WD2002 40 pin package version only.
24	35	$\overline{\text{ENCRYPT/DECRYPT}}$	$\overline{\text{E/D}}$	When $\overline{\text{CRPS}}$ is high or open, this pin is an output reflecting the status of the $\overline{\text{ENCRYPT/DECRYPT}}$ bit (bit 3) of the COMMAND/STATUS REGISTER. When $\overline{\text{CRPS}}$ is low, this pin is an input pin that overrides the $\overline{\text{ENCRYPT/DECRYPT}}$ bit of the COMMAND/STATUS REGISTER.
N/A	25	$\overline{\text{DUAL PORT SELECT}}$	$\overline{\text{DPS}}$	When this input is high or open, single port operation is selected and all DES chip transfers are via the DAL bus. When $\overline{\text{DPS}}$ is low, dual port operation is selected and both the DAL bus and the CDP bus are used [separate busses for clear data (DAL bus) and cipher data (CDP bus)]. This pin is available on the WD2002 40 pin package version only.

NOTE: The WD2001 28 pin package version does not have the following pins:
 The 8 CDP pins, the KEOE pin, and the $\overline{\text{DPS}}$ pin.



ORGANIZATION

The Data Encryption Standard chip consists of a 56-bit KEY REGISTER, a 64-bit DATA REGISTER, an 8-bit COMMAND/STATUS REGISTER, plus the necessary logic to check KEY parity and implement the NBS algorithm. A typical system implementation is shown on page 10 and the block diagram is shown on page 1. Although the DES chip interfaces to a wide variety of processors including mini-computers, the interface is tailored to the 8080A class microprocessor.

GENERAL OPERATING DESCRIPTION

The user programs the DES chip for encryption or decryption, and single or dual port operation.* Data is encrypted/decrypted with a 64-bit user defined KEY WORD. Data encrypted with a given KEY WORD can be decrypted only using that KEY WORD. The KEY REGISTER is loaded by the computer with eight successive 8-bit bytes. Parity is checked on each byte of the KEY WORD as it is loaded into the KEY REGISTER (The 8th bit (DALØ) of each 8-bit byte is reserved for odd parity for that byte and is not used in the algorithm calculation.) Similarly the DATA REGISTER is loaded with eight successive 8-bit bytes. The DATA REGISTER is read by reading eight successive 8-bit bytes.

When the DES chip is programmed for encryption, the DATA REGISTER is loaded with eight bytes of plain or clear text. The DES chip encrypts the data, then the encrypted data may be read from the DATA REGISTER (64-bits of encrypted text). When the DES chip is programmed for decryption, the DATA REGISTER is loaded with eight bytes of encrypted or cipher text. The DES chip decrypts the data, then the plain text may be read from the DATA REGISTER (64-bits of plain text). Note that all transfers to and from the KEY REGISTER and/or DATA REGISTER must occur in eight successive 8-bit bytes.

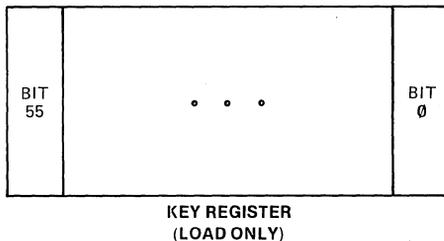
*Note: Dual port operation available with WD2002 40 pin package version only. (Single and dual port operation is described in detail under PART V. OPERATION.)

REGISTER DESCRIPTION

The following describes the KEY, DATA, and COMMAND/STATUS REGISTERS of the DES chip.

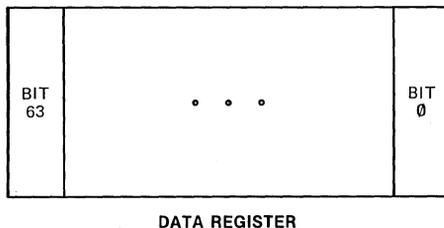
Key Register

This 56-bit register contains the KEY by which the Data Encryption Algorithm operates. Eight successive bytes are needed to load the KEY REGISTER. The KEY REGISTER can be loaded only when there is a KEY REQUEST (Status bit and output). THIS REGISTER IS LOAD ONLY AND CANNOT BE READ.



Data Register

This 64-bit register contains plain or cipher text. When in the encrypt mode, the DATA REGISTER is loaded with plain text, and when read contains cipher text. When in the decrypt mode, the DATA REGISTER is loaded with cipher text, and when read contains plain text. The DATA REGISTER is always read or loaded with eight successive byte transfers. The DATA REGISTER can be loaded only when there is a DATA-IN REQUEST (status bit and output); similarly the DATA REGISTER can be read only when there is a DATA-OUT REQUEST (status bit and output).



Command/Status Register (C/S R)

This 8-bit register controls the operation of the DES chip and monitors its status. Bits 7, 6, 5 and 4 are status-only bits (read only). Bits 3, 2 and 1 are COMMAND/STATUS bits (read/write). Bit 0 is not used. The COMMAND/STATUS bits (bits 3, 2, and 1) are normally loaded only once for an entire encrypt or decrypt process.

7	6	5	4	3	2	1	0
DOR	DIR	KPE	KR	E/D	KEOE	ACT	N/U
STATUS BITS (READ ONLY)				COMMAND/STATUS BITS [READ] [WRITE]			

COMMAND/STATUS REGISTER

COMMAND/STATUS REGISTER (C/S R)

Bit	Name	Function
C/S R0	NOT USED	
C/S R1	ACTIVATE	This bit must be set from '0' to '1' to initiate loading the KEY REGISTER. This bit must be '1' for encrypt/decrypt operation. This is a read/write bit.
C/S R2	KEY ERROR OUTPUT ENABLE (KEOE)	When '0', the KEY PARITY ERROR output pin (\overline{KPE}) remains inactive regardless of the status of the KEY PARITY ERROR bit (bit 5). When '1', the KEY PARITY ERROR output pin is active when the KPE bit (bit 5) is '1'. This bit is set to '1' upon a MASTER RESET. This is a read/write bit.
C/S R3	ENCRYPT/DECRYPT (E/D)	When '0' data is to be encrypted. When '1' data is to be decrypted. This is a read/write bit.
C/S R4	KEY REQUEST (KR)	This bit is set one clock period after the ACTIVATE bit is set (from '0' to '1'). It is reset upon loading of the 8th and final byte of the KEY REGISTER. This is a read only bit.
C/S R5	KEY PARITY ERROR (KPE)	This bit is set internally upon detection of a parity error during loading of the KEY REGISTER. It is reset when the ACTIVATE bit is programmed from '1' to '0' (i.e., chip is deactivated). This is a read only bit.
C/S R6	DATA-IN REQUEST (DIR)	This bit is set upon either: a) Completion of KEY REGISTER loading - or - b) Completion of DATA REGISTER reading, (ie, the last DATA-OUT REQUEST has been serviced by an 8-byte read and the DATA REGISTER is now empty and ready to be loaded with the next DATA WORD). It is reset upon loading of the 8th and final byte of the DATA REGISTER. This is a read only bit.
C/S R7	DATA-OUT REQUEST (DOR)	This bit is set upon completion of the internal encrypt/decrypt calculation of a DATA WORD. It is reset upon reading of the 8th and final byte of the DATA REGISTER. This is a read only bit.

Note: All bits of the COMMAND/STATUS REGISTER are reset to '0' upon MASTER RESET, except bit 2 (KEOE) which is set to '1' and bit 0 (not used) which will read '1' by default during a COMMAND/STATUS REGISTER read.

DETAILED OPERATING DESCRIPTION

The DES chip is initiated by programming a '1' in the ACTIVATE bit of the COMMAND/STATUS REGISTER. The DES chip will respond by activating the KEY REQUEST (KR) bit (bit 4) of the STATUS REGISTER and the KEY REQUEST output.

The user must deactivate $A\emptyset$ (allowing the chip to internally address the KEY REGISTER), and load the KEY REGISTER with the 64-bit KEY WORD. The KEY REGISTER is loaded with 8 consecutive 8-bit bytes by activating \overline{WE} 8 times (with \overline{CS} active).

When \overline{WE} is made active, the DES chip deactivates the KR output. When \overline{WE} is deactivated, the KR output is again activated. The DES chip will activate 8 KEY REQUESTs in this fashion until the KEY REGISTER is full.

Also, when \overline{WE} is made active, the DES chip responds by activating the KEY ACKNOWLEDGE (\overline{KA}) output. Thus, 8 \overline{KA} activations will be made.

The KR and \overline{KA} outputs can be used for asynchronous handshaking (as in DMA control) or further activations following the first KR can be ignored and the KEY REGISTER can be loaded in a synchronous (programmed I/O) manner via 8 successive activations of \overline{WE} .

Each byte of the KEY WORD is checked for odd parity as it is loaded. If a parity error is found, the chip will set the KEY PARITY ERROR (KPE) bit (bit 5) of the COMMAND/STATUS REGISTER. If the KEY ERROR OUTPUT ENABLE bit (bit 2) of the COMMAND/STATUS REGISTER has been set, the DES chip will also activate the KPE output. The KPE bit will be reset when the ACTIVATE bit is re-programmed to a '0'.

After loading the last (8th) byte of the KEY WORD into the KEY REGISTER, the DES chip will set the DATA-IN REQUEST bit (bit 6) of the STATUS REGISTER and activate the DATA-IN REQUEST (DIR) output. The 64-bit DATA WORD must then be loaded into the DATA REGISTER. The DATA REGISTER is loaded in the same manner as the KEY REGISTER via 8 successive activations of DATA-IN REQUEST (DES output), \overline{WE} (DES input, and DATA-IN ACKNOWLEDGE (DES output).

After the last (8th) byte of the DATA WORD has been loaded, the chip begins the internal calculation of the NBS algorithm. Upon completion of the calculation, the new data is internally loaded into the DATA REGISTER, and the DES chip sets the DATA-OUT REQUEST bit (bit 7) of the STATUS REGISTER and activates the DATA-OUT REQUEST (DOR) output. The DATA WORD must then be read from the DATA REGISTER. The DATA REGISTER is read in the same manner as it was loaded via 8 successive activations of DATA-OUT REQUEST (DES output), \overline{RE} (DES input), and DATA-OUT ACKNOWLEDGE (DES output).

Again, for both data-in and data-out, further activations of the DIR, DOR and \overline{DIA} , \overline{DOA} outputs, after the first request, can be ignored and the DATA REGISTER loaded (read) by 8 successive activations of \overline{WE} (\overline{RE}).

After the last (8th) byte of the DATA REGISTER has been read, the DES chip will reactivate the DATA-IN REQUEST. This cycle of loading the DATA REGISTER, internal algorithm calculation, and reading the new data from the DATA REGISTER can continue indefinitely until all desired data has been encrypted or decrypted with the current KEY WORD.

After all desired data has been encrypted/decrypted with the current KEY WORD, the ACTIVATE bit of the COMMAND/STATUS REGISTER should be programmed to '0'. When the ACTIVATE bit has been reset to '0', an unauthorized user will not have access to the last KEY loaded into the DES chip since to resume operation, the ACTIVATE bit must be programmed to '1' which activates KEY REQUEST and a new KEY must be loaded before access to the DATA REGISTER is possible.

To encrypt plain data, plain data is loaded into the DATA REGISTER, and encrypted data is read from the DATA REGISTER. (The ENCRYPT/DECRYPT bit (bit 3 of the COMMAND/STATUS REGISTER) must have been previously programmed to '0'.)

To decrypt encrypted data, encrypted data is loaded into the DATA REGISTER, and plain data is read from the DATA REGISTER. (The ENCRYPT/DECRYPT bit must have been previously programmed to '1'.)

Note: If it is desired to switch from encrypt to decrypt (or vice versa) under the same KEY WORD, this can be accomplished before a DATA WORD transfer is initiated. By making $A\emptyset$ high, the DES chip will override the internal addressing of the DATA REGISTER, and address the COMMAND/STATUS REGISTER. The COMMAND/STATUS REGISTER can be re-programmed. When $A\emptyset$ is returned to a low state, the DES chip will internally address the DATA REGISTER awaiting loading of the next DATA WORD.

DUAL PORT OPTION

(Available on WD2002 40 Pin Version Only)

When the $\overline{DUAL\ PORT\ SELECT}$ (\overline{DPS}) input is high or left open (i.e., single port operation is selected), all transfers to/from the DES chip are via the DAL bus. The CDP bus is not used and remains three-stated.

When \overline{DPS} is made low (i.e., dual port operation is selected), all transfers to/from the COMMAND/STATUS REGISTER, and transfers to the KEY REGISTER are still via the DAL bus. Clear DATA WORDS are also transferred via the DAL bus. However, cipher DATA WORDS are now transferred via the CDP bus. This provides separate busses for clear and ciphered text.

Encryption during dual port operation requires loading clear data via the DAL bus, and reading cipher data via the CDP bus.

Decryption during dual port operation requires loading cipher data via the CDP bus, and reading clear data via the DAL bus.

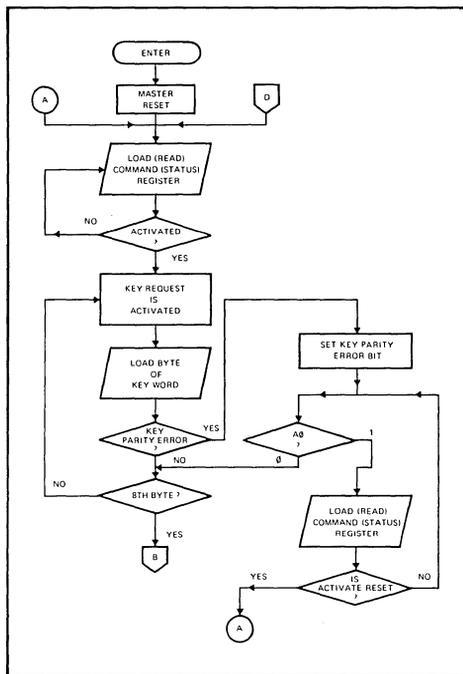
COMMAND SELECT OPTION

When the COMMAND REGISTER PIN SELECT (CRPS) input is made low, the ACT and \bar{E}/D pins are enabled as inputs. These inputs override bits 1 and 3 (respectively) of the COMMAND/STATUS REGISTER. This allows input pin control of the DES chip. The KE0E bit (bit 2) of the COMMAND/STATUS REGISTER will be held to '1'.

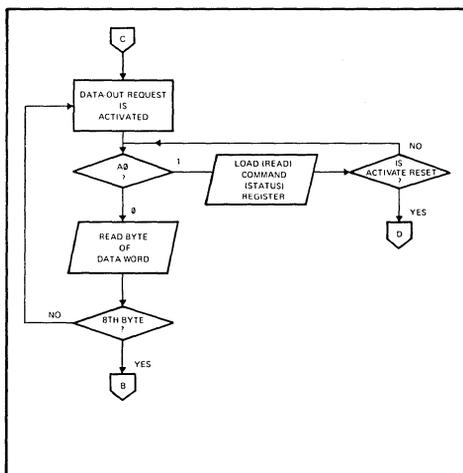
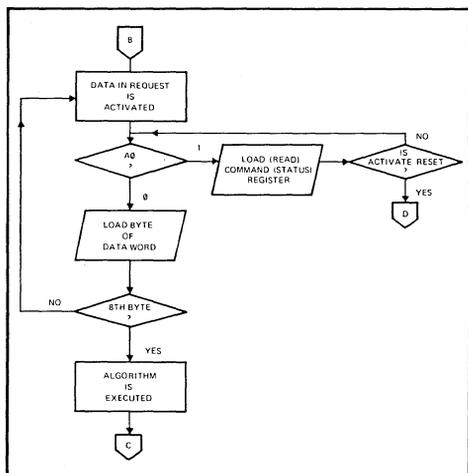
Input A0 will be disregarded in this mode of operation, and the COMMAND/STATUS REGISTER cannot be accessed via the DAL lines.

Note that the ACT pin must be toggled from '1' to a '0' to clear a parity error detection in this mode of operation.

All other operation remains as described previously.



WD2001/WD2002 FLOW CHARTS



MAXIMUM RATINGS

V_{DD} with Respect to V_{SS} (Ground) +15 to -0.3V
 Max. Voltage to any Input with Respect to V_{SS} +15 to -0.3V
 Operating Temperature 0°C to 70°C
 Power Dissipation 1 W

Storage Temp. Ceramic -65°C to +150°C
 Plastic -55°C to +125°C

OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12.0V ± .6V, V_{CC} = +5.0V ± .25V, V_{SS} = 0V

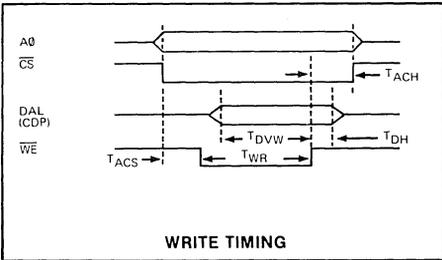
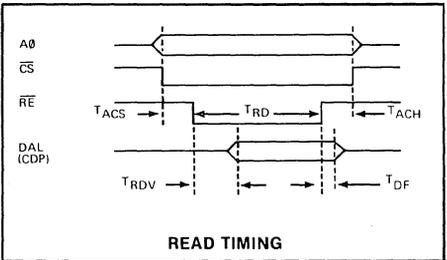
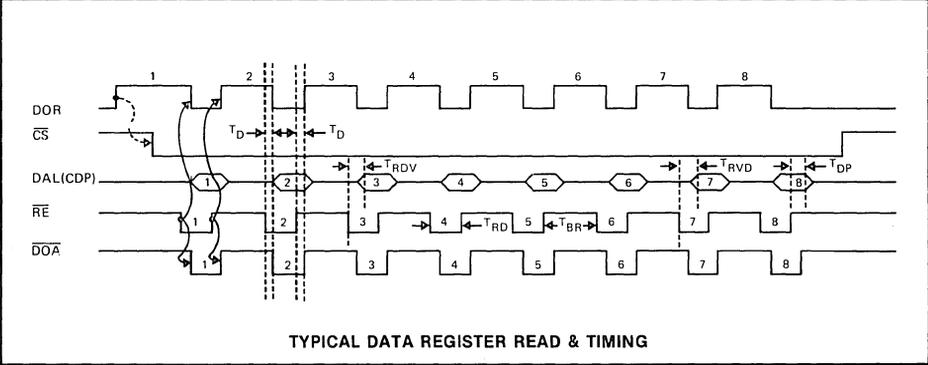
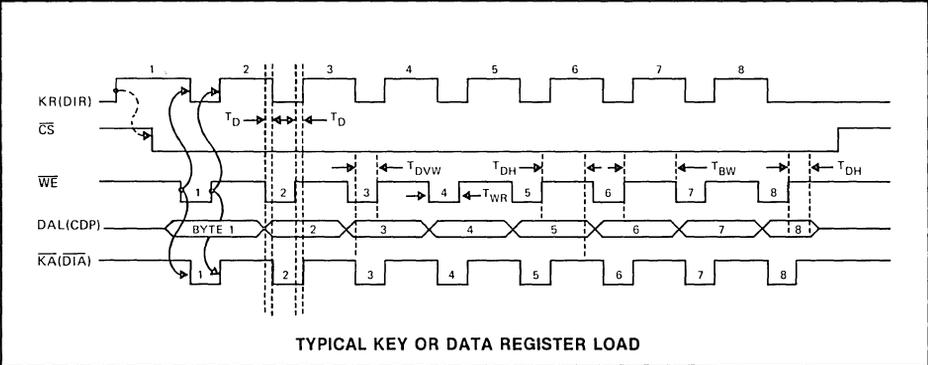
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
I _{LI}	Input Leakage			10	µA	V _{IN} = V _{DD}
I _{LO}	Output Leakage			10	µA	V _{OUT} = V _{CC}
I _{CCA}	V _{CC} Supply Current		68	100	mA	
I _{DDA}	V _{DD} Supply Current		17	25	mA	
V _{IH}	Input High Voltage	2.4			V	
V _{IL}	Input Low Voltage (All Inputs)			.8	V	
V _{OH}	Output High Voltage	2.0			V	I _O = -100µA
V _{OL}	Output Low Voltage			.4	V	I _O = 1.6 mA

AC CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12.0V ± 0.6V, V_{SS} = 0V, V_{CC} = +5.0 ± .25V

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
READ						
T _{ACS}	A ₀ , \overline{CS} Set up to $\overline{RE} \downarrow$	80			ns	C _{LOAD} = 50PF
TR _{DV}	$\overline{RE} \downarrow$ to DAL (CDP) Valid			330	ns	
TR _D	\overline{RE} Pulse Width	330			ns	
T _{DF}	$\overline{RE} \uparrow$ to DAL Float	30		200	ns	
T _{ACH}	A ₀ , \overline{CS} Hold From $\overline{RE} \uparrow$	0			ns	
WRITE						
T _{ACS}	A ₀ , \overline{CS} Set up to $\overline{WE} \downarrow$	80			ns	C _{LOAD} = 50PF
T _{DVW}	DAL (CDP) Set up to $\overline{WE} \uparrow$	200			ns	
T _{WR}	\overline{WE} Pulse Width	200			ns	
T _{DH}	DAL (CDP) Hold From $\overline{WE} \uparrow$	80			ns	
T _{ACH}	A ₀ , \overline{CS} Hold From $\overline{WE} \uparrow$	0			ns	
HAND-SHAKE						
T _D	KR (DIR) \downarrow , \overline{KA} (\overline{DIA}) \downarrow From $\overline{WE} \downarrow$ KR (DIR) \uparrow , \overline{KA} (\overline{DIA}) \uparrow From $\overline{WE} \uparrow$ DOR \downarrow , \overline{DOA} \downarrow From $\overline{RE} \downarrow$ DOR \uparrow , \overline{DOA} \uparrow From $\overline{RE} \uparrow$		300	450	ns	C _{LOAD} = 50PF

NOTE: All output timing specifications reflect the following: High Output 2.0V
 Low Output 0.8V



MISCELLANEOUS TIMING

1. CLOCK INPUT
 FREQUENCY: 2 MHZ (MAX); 100 KHZ (MIN).
 PULSE WIDTH: 250 nsec MIN.
2. MASTER RESET PULSE WIDTH: 10 Clock Periods
3. Time between consecutive \overline{RE} or \overline{WE} pulses:
 $T_{BR} = T_{BW} = 2 \text{ CLOCK PERIODS MINIMUM}$
4. ACT, $\overline{E/D}$, KEQOE OUTPUTS
 These pins will be valid within $2 \text{ CLK} \downarrow + 450 \text{ nsec}$ from $\overline{WE} \uparrow$ of a COMMAND REGISTER write operation.
5. \overline{KFE} OUTPUT
 This pin will be active within $2 \text{ CLK} \downarrow + 450 \text{ nsec}$ from $\overline{WE} \uparrow$ of a write of a KEY WORD byte that results in a parity error.
6. \overline{CRPS} , \overline{DPS} , $\overline{E/D}$ INPUTS require a 300 ns set-up time.
7. The initial KR activation will be valid within $3 \text{ CLK} \downarrow + 450 \text{ nsec}$ from $\overline{WE} \uparrow$ of a write operation that programs a '1' into the COMMAND REGISTER ACTIVATE bit (or $2 \text{ CLK} \downarrow + 450 \text{ nsec}$ from ACT input \uparrow , if $\overline{CRPS} = 0$).
8. The initial DIR activation will be valid within $2 \text{ CLK} \downarrow + 450 \text{ nsec}$ from $\overline{WE} \uparrow$ of the 8th write into the KEY REGISTER.
9. The initial DOR activation will be valid within 49

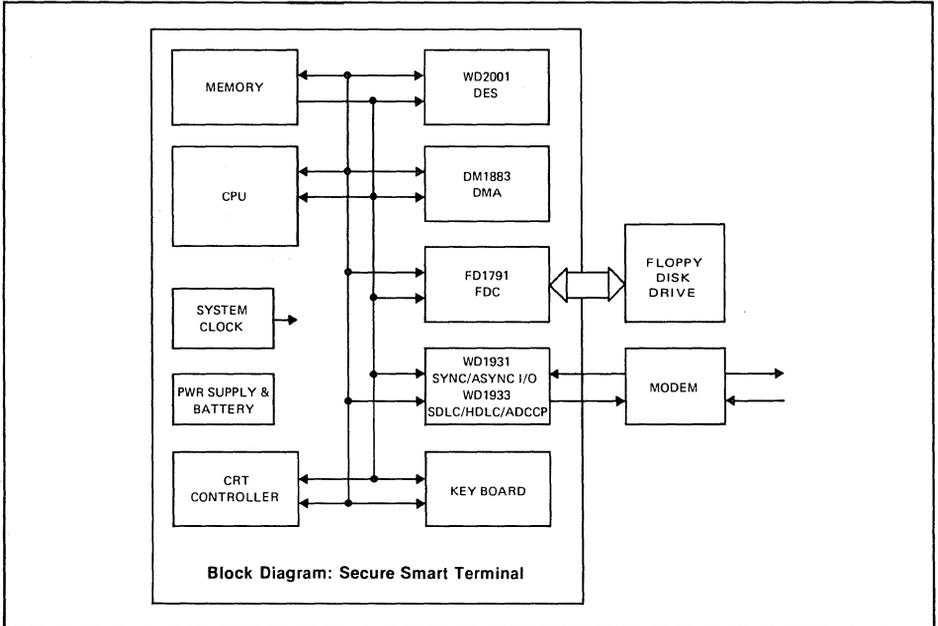
$\text{CLK} \downarrow + 450 \text{ nsec}$ from $\overline{WE} \uparrow$ of the 8th write into the DATA REGISTER.

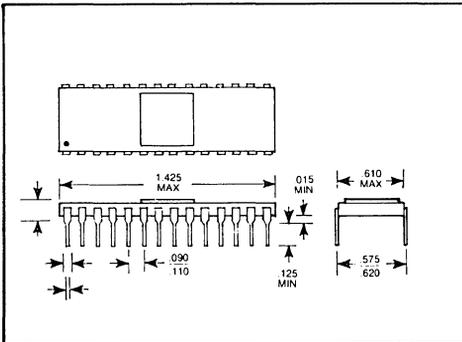
10. When reading the DATA REGISTER (in response to DOR), subsequent data bytes are made available internally to the DAL (CDP) output buffers within $2 \text{ CLK} \downarrow + 450 \text{ nsec}$ from $\overline{RE} \uparrow$

NOTE: All output timings assume CLOAD = 50 PF

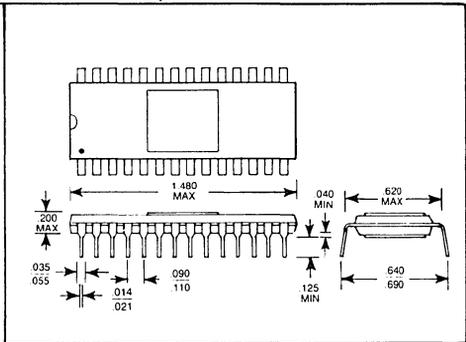
TYPICAL APPLICATION

Shown below is a block diagram for a floppy disk based DES secure smart terminal. The Direct Memory Access (DMA) controller optimizes data transfer operations for not only the floppy but also for file encryption and decryption operations. Secure features for the terminal include: secure file storage on floppy disks, optical clear/secure transmission via the communications I/O and battery backup of the Terminal ID key. Tampering with the Terminal by unauthorized persons either through the key board power supply interrupt interlock or attempting to open the service panel results in memory scrambling and terminal ID key destruction. Finally, a hardware option was also included to allow the use of the pin compatible WD1933 device in place of the WD1931 for bit oriented SDLC, HDLC, or ADCCP protocols.

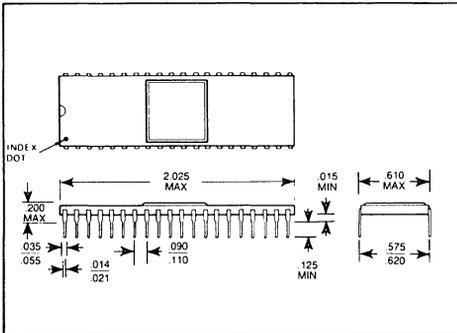




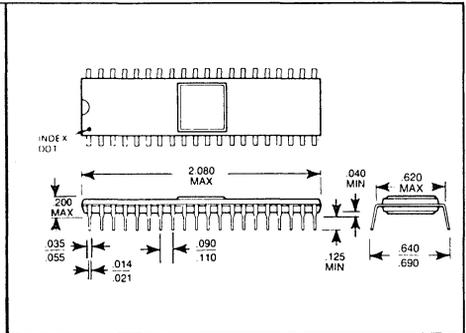
WD2001E CERAMIC PACKAGE



WD2001F PLASTIC PACKAGE



WD2002A CERAMIC PACKAGE



WD2002B PLASTIC PACKAGE

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WDK20001-XA CRYPTOGRAPHIC PRIMER KIT

MARCH, 1981

FEATURES

- RS-232 COMPATIBLE CRYPTOGRAPHIC UNIT WITH:
 - WD2002 CERTIFIED IMPLEMENTATION OF THE NATIONAL BUREAU OF STANDARDS DATA ENCRYPTION STANDARD
 - SELECTABLE BAUD RATE (50BPS to 19.2KBPS)
 - CABLE TO HOOK DIRECTLY TO AN RS-232 COMPUTER PORT
 - LED DISPLAY FOR CRYPTOGRAPHIC STATUS AND ERROR CONDITIONS
 - CRYPTOGRAPHIC PROTOCOL
- USER MANUAL FOR HARDWARE
- MANUAL DESCRIBING CRYPTOGRAPHIC TECH-

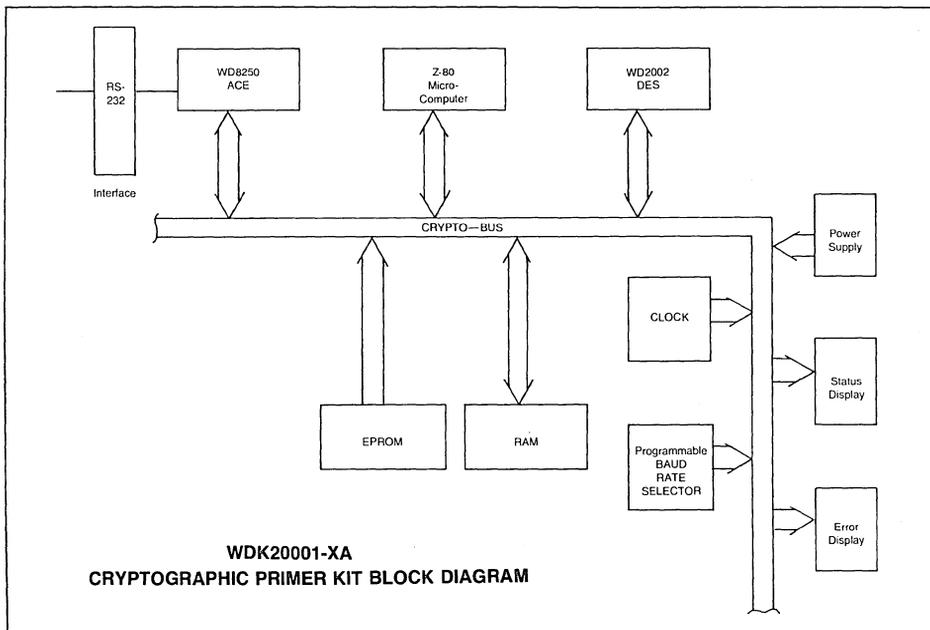
NIQUES AND HOW TO IMPLEMENT THEM

- EXAMPLES TO HELP CHECK OUT USER SOFTWARE
- THE "CODEBREAKERS" BY DAVID KAHN

GENERAL DESCRIPTION

The WDK20001-XA provides a basic cryptographic unit with a standard RS-232 I/O interface. The user accesses the cryptographic unit as a programmed I/O device operating at a switch selectable baud rate between 50bps and 19.2Kbps.

Guidance for writing applications programs to communicate with the cryptographic unit through a cryptographic protocol and for using it to perform cipher feedback and other cryptographic implementations is included in the Cryptographic Primer manual. Specific examples of matched key, plaintext and ciphertext are included to help debug the users application programs.



Security Products Technical Notes

1 ZO-10ms

WESTERN DIGITAL
C O R P O R A T I O N
CIPHER FEEDBACK CRYPTOGRAPHY
TECHNICAL NOTE

by Ken Cohen

SYSTEM
1

CIPHER FEEDBACK CRYPTOGRAPHY

The United States Government in proposed Federal Standard 1026 describes three different approved ways of using the National Bureau of Standard's Data Encryption Standard (DES): Electronic Codebook; Cipher Feedback; and Cipher Block Chaining. Western Digital's WD2001 and WD2002, as delivered, implement the DES in Electronic Codebook Mode. This Technical Note will describe how to build an "N" bit Cipher Feedback (CFB) circuit using the WD2001.

WHAT IS CIPHER FEEDBACK?

Cipher feedback cryptography produces, as a function of previous cipher text, a pseudorandom bit stream which is added modulo 2 to the plain text to produce the next cipher text.

DES IN CIPHER FEEDBACK (CFB)

Obviously, both the receiver and transmitter must start their cryptographic operation with the same cryptographic keys to be able to acquire and maintain cryptographic synchronization, i.e. produce the same pseudorandom bit stream at the same point in time.

For DES this means that both the 64 bit cryptographic variable (56 bit key) and the initial input to the algorithm must be identical at both ends. The initial input to DES in CFB is called the Initializing Vector (IV). Its format and generation are described in detail in Federal Standard 1026.

The functional description of using the WD2001 in CFB mode below assumes that communication synchronization has been achieved; that identical decrypted IV's and cryptographic keys are available to both the transmit and receive ends of the link; that encryption is to be a 1 bit cipher feedback; and that the plain text character size (1 in the example) equals the transmitted character size (Method A in proposed Federal Standard 1026).

ENCRYPTION

At time 0, the 64 bit cryptographic variable is loaded into the WD2001 with the key load sequence. A 64 bit block consisting of not more than 16 leading 0's and the 48 bit (or longer) IV is loaded into a 64 bit shift register (R) and into the input register, as if it were data, and encrypted. The WD2001 will automatically encrypt the IV under control of the cryptovariable and present a 64 bit block, 8 bits at a time as output.

This output is stored in a shift register(S) with the most significant bit (MSB), to the left and the least significant bit on the right.

The MSB of S is added modulo 2 to the first bit of plain text to produce the first cipher bit. The contents of R are shifted 1 bit to the left and the just created cipher bit is inserted as the least significant bit (LSB) in R. The cipher bit is now available for buffering, transmission, etc.

The new contents of R are now loaded into the WD2001 as data, encrypted, and the new output placed in S.

The above procedure is repeated until the entire message text is encrypted, one bit at a time.

DECRYPTION

Decryption is accomplished in a similar manner: the IV is stored in R; loaded into the WD2001 as data; ENCRYPTED (even though the operation on the message text is to be decrypted); the results stored in S; and R shifted 1 bit to the left. Now, because the unit is receiving cipher rather than creating it, the first received bit is placed in the LSB of R. This cipher bit is also added, modulo 2, to the leftmost bit in S to reproduce the original plain text.

NOTES

Of particular significance is that the DES chip is in the ENCRYPT mode for CFB cryptography regardless whether the operation is to be performed to create cipher text or to recreate plain text. This is because the DES is being used to generate a pseudorandom bit stream. It is the exclusive OR operating on that bit stream and the received text which accomplishes the actual encryption/decryption of data.

S was nominally defined to be 64 bits long. It need be no longer than the number of text bits to be exclusive OR'd at one setting of the pseudorandom stream. In the example it was one bit. In reality it could be any character or block size from 1 to 64 bits long.

The convention used in this note is to organize a shift register with the MSB to the left. In practice, what is important is to use the MSB of S for the MOD 2 addition and to shift the R register content, so that the MSB is dropped and the cipher bit becomes the LSB. It is also important to perform the shift and generate a new pseudorandom block after each character has been encrypted or decrypted.

FEBRUARY, 1981

OTHER CIPHER FEEDBACK METHODS

Cipher Feedback can be done for any feedback size of 1 through 64 bits. One bit cipher feedback has the overall advantage of being transparent to the data being protected.

CHARACTERISTICS OF CFB

CFB has two properties which must be considered when selecting it for data encryption: 1) error extension and 2) self synchronization. Both of these properties exist because the encryption process synchronizes on the received cipher to produce the pseudorandom bit stream.

In the case of DES in one bit CFB, a one bit error in the received cipher message will affect the next 64 pseudorandom blocks—it will take 64 iterations to shift the one "bad" bit out of the 64 bit register above. If 8 bit CFB is used, then only 8 blocks will be affected, but that will still represent 64 bits used to decrypt incoming data.

In the same way, receiving 64 consecutive good bits of cipher will have filled the data-in register on the receiver end with the same 64 bits of data as in the transmit unit and proper decryption can again take place, assuming both ends have the same cryptographic key. This is what is meant by self-synchronizing.

APPLICATIONS OF CFB

In the data communications world error extension and self-synchronization are not important because of the excellent conditions of the lines and the protocols and error correcting codes used to insure proper receipt of data. In some applications, these properties of CFB cryptography can be turned to the user's benefit. This is especially true in situations where the data stream contains highly redundant information, where an incorrect recovery of 64 bits is hardly noticed—particularly when compared with the overall communications benefit of having the cryptography automatically resynchronize itself.

WD2001 CHARACTERISTICS IN CFB

The WD2001 is rated as having 1.304 megabits per second throughput when driven by a 2 MHz clock. This figure is based on processing 64 bits of data at each operation. Using the WD2001 in an 8 bit cipher feedback circuit will reduce that to 163 kilobits per second. A 1 bit cipher feedback circuit would further reduce effective throughput to 20,385 kilobits per second. This is true of any DES implementation. The algorithm is designed to process 64 bits of plain (cipher) text at a time to produce 64 bits of cipher (plain) text; cipher feedback is designed to operate on a basic character size and shift after that character has been encrypted. In the 1 bit case, the user "throws away" 63/64ths throughput capacity for each encryption.

Security Product Applications Note

- Zo-omó

WESTERN DIGITAL C O R P O R A T I O N

WD2001/2 APPLICATIONS NOTE

"ONE BIT CIPHER FEEDBACK IN A SYNCHRONOUS SYSTEM"

By Michael D. Garvey

INTRODUCTION

The WD2001/2 Data Encryption device interfaces easily to both microcomputer and hard-wired logic circuits. This Applications Note provides suggestions for the implementation of a synchronous circuit to perform system timing in a one bit cipher feedback application.

SYSTEM TIMING CONSIDERATIONS

The synchronous operation of a digital circuit often leads to both minimal hardware count and simple, easy to understand timing relationships. In addition, the concern over individual device characteristics become non-critical through the use of a worst case design approach. Common problems such as race conditions and temperature sensitivity can be virtually eliminated by synchronizing all logical events to a well defined clock edge.

WD2001/2 TIMING REQUIREMENTS

The WD2001/2 may be operated from a 2 MHz clock. This provides a fundamental time period of 500 nSec that easily fits into the timing requirements for the device. For example, the minimum pulse width for a read (RD) or write (WR) pulse is 450 nSec.

Generation of the RD or WR pulse can be directly obtained from a synchronous device that transitions at each edge of the synchronous clock (SYNCLK). Figure 1 illustrates the timing relationship between SYNCLK and RD or WR.

Once the timing relationship is understood, the implementation becomes quite straightforward. The circuit of Figure 2 suggests a possible method of RD or WR generation.

FEBRUARY, 1981

WD 2001/2

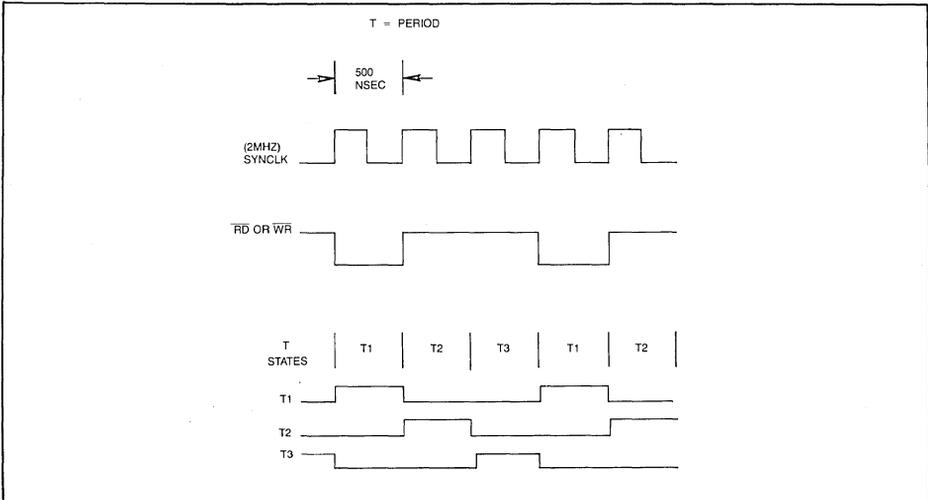


Figure 1 SYNCLK, RD, AND WR TIMING RELATIONSHIPS.

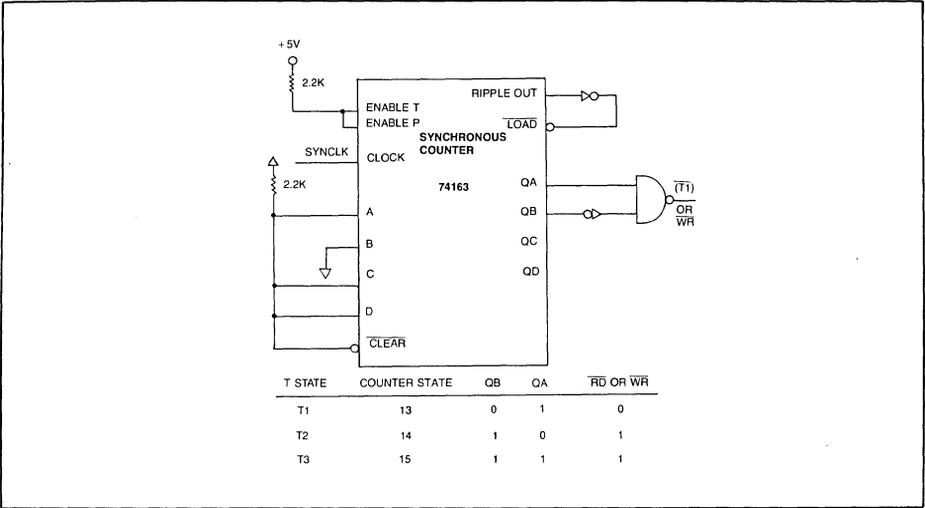


Figure 2 RD AND WR TIMING GENERATION

FUNDAMENTAL TIMING SEQUENCES

Any cryptographic implementation using the Data Encryption Standard (DES) can be broken down into four fundamental timing sequences. First, the key is loaded into the WD2001/2 (Load Key). Second, the data to be encrypted or decrypted is loaded into the device (Load Data). Next, the DES is executed. Finally, the result of the DES is unloaded from the WD2001/2 (Unload Data). Figure 3 lists the timing requirements for each timing sequence.

The Load Key, Load Data, and Unload Data sequences are highly similar. Figure 4 shows the logical flow associated with the Key Load or Data Load, or Data Unload. The Data Encryption Algorithm sequence can be derived from the timing associated with the other three sequences. For simplicity, the DES timing is accomplished by counting groups of three clock periods in a fashion similar to the method shown in Figure 4. The logical flow for the DES timing is shown in Figure 5.

SEQUENCE	NUMBER OF CLOCK PERIODS	TOTAL
Load Key	8 bytes × 3 clocks	24
Load Data	8 bytes × 3 clocks	24
DES	17 × 3 clocks	51
Unload Data	8 bytes × 3 clocks	24

Figure 3 FUNDAMENTAL TIMING SEQUENCES

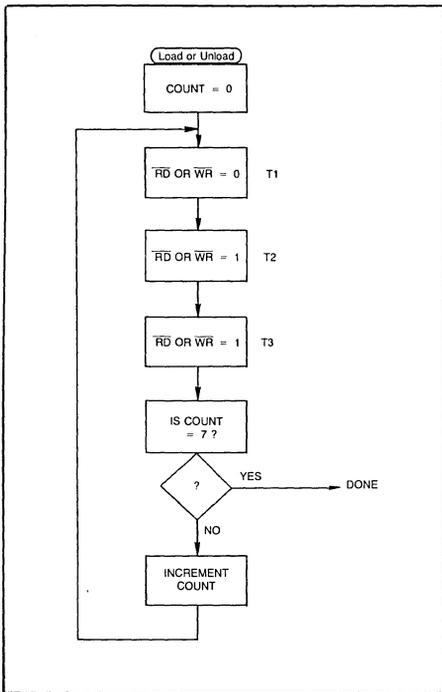


Figure 4 KEY LOAD, DATA LOAD, AND DATA UNLOAD FLOW

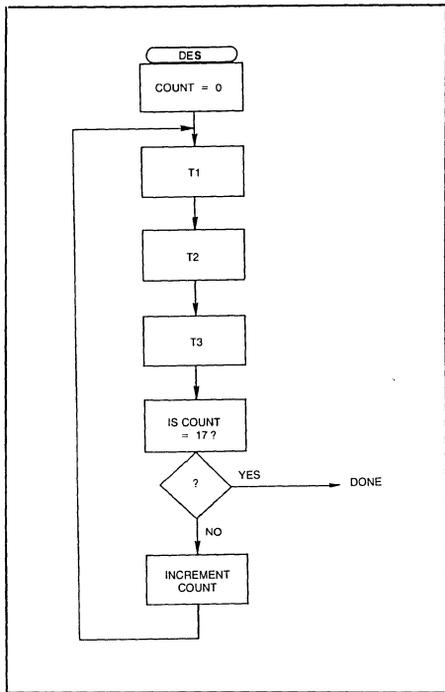


Figure 5 DES LOGICAL FLOW

SYSTEM TIMING OVERVIEW

The normal operation of a cryptographic system would require three classes of input/output (I/O) operations with the WD2001/2. First, the key is loaded (Key Load) through eight consecutive write cycles. Second, the data to be encrypted or decrypted is loaded (Load Data) in a similar fashion. After the Data Encryption standard is completed, the data is unloaded (Unload Data) through eight consecutive read cycles. Typically, the Key Load sequence would occur much less frequently than the Load Data or Unload Data sequences.

The flow diagram of Figure.6 shows the relationship between the four fundamental timing sequences defined previously,

and also highlights the three I/O operations. Note that the Key Load sequence is outside of the tight loop.

Using the four fundamental timing sequences as logical building blocks, a functional block diagram of system timing can be designed. Figure 7 illustrates the overall system timing functions.

An implementation of the functions shown in Figure 7 is suggested in Figure 8. Note that all timing transitions are synchronous with the rising edge of SYNCLK.

Figure 9 details the timing of the Load Key sequence, and is similar to the Load Data, Unload Data, and DES_i sequences also.

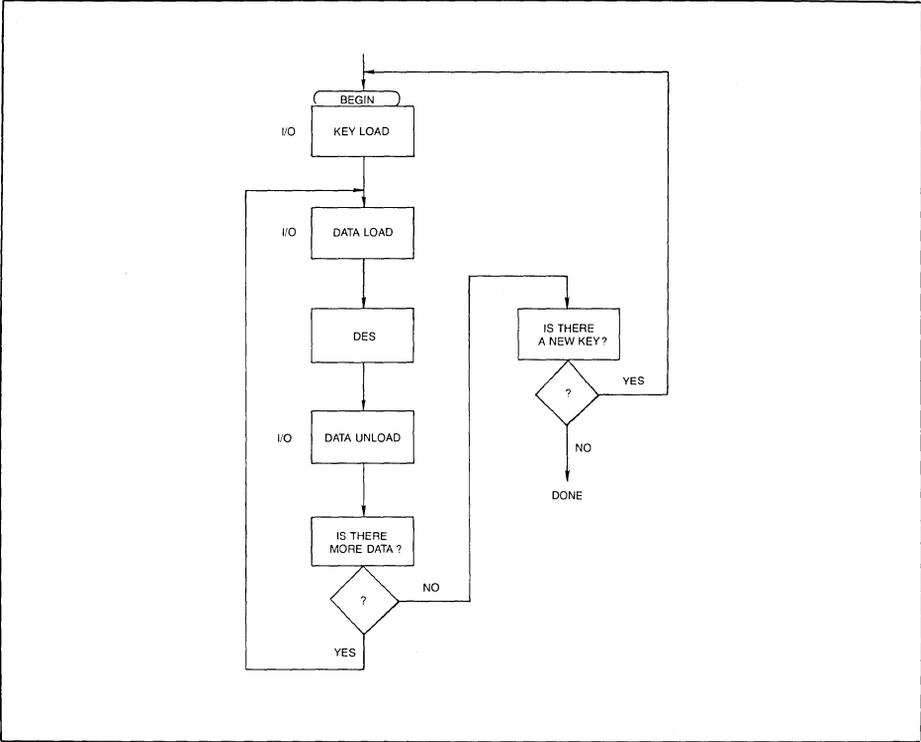


Figure 6 FUNDAMENTAL TIMING SEQUENCES INTERRELATIONS

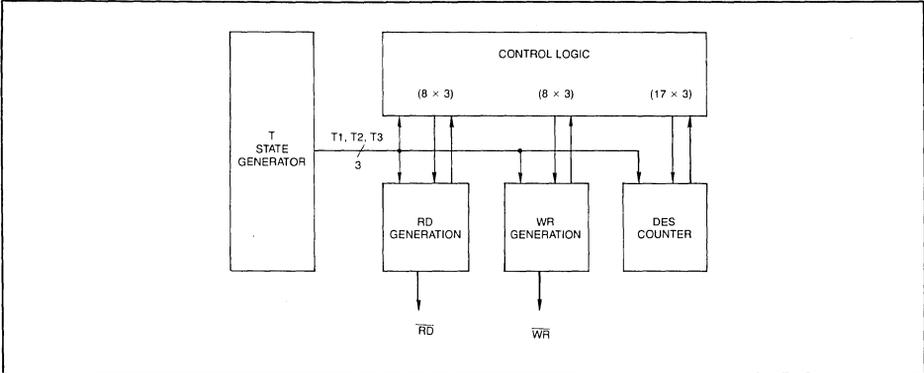


Figure 7 SYSTEM TIMING BLOCK DIAGRAM

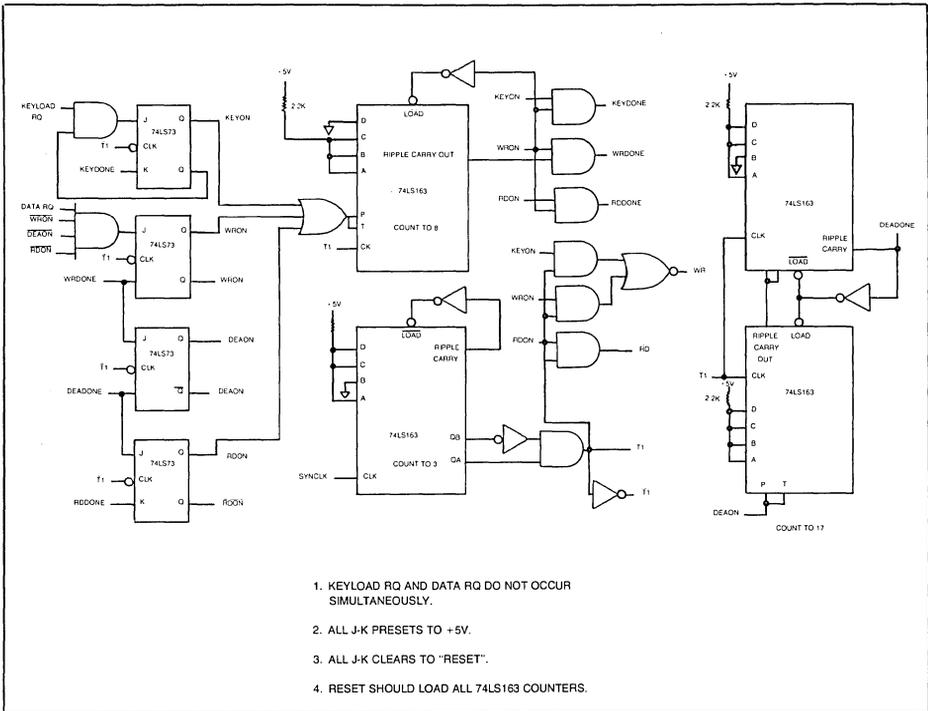


Figure 8 SYSTEM TIMING IMPLEMENTATION

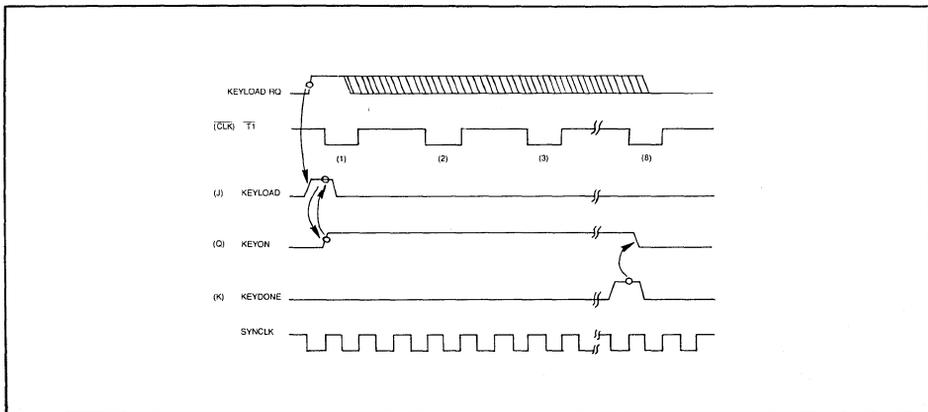


Figure 9 SINGLE KEYLOAD SEQUENCE

ONE BIT CIPHER FEEDBACK

The one bit cipher feedback (OBCFB) architecture is widely used in Data Communications. The WD2001/2 device, when operated with a 2 MHz clock, will run at an effective bit rate of over 19,200 bits/second, which is the practical upper limit of many communications links.

FUNDAMENTAL LOGICAL COMPONENTS OF OBCFB

A one bit cipher feedback system can be broken down into nine logical components, as listed in Figure 10.

NAME	DESCRIPTION
KEY	56 bit number that maps INV to OV
IV	Initialization Vector
INV	Input Vector
DES	Data Encryption Standard
OV	Output Vector
SDI	Serial Data In
SDO	Serial Data Out
SR	Shift Register (used with INV)
MOD2	Modulo 2 Adder

Figure 10

NINE FUNDAMENTAL COMPONENTS OF OBCFB

FUNCTIONAL DESCRIPTION OF OBCFB

The OBCFB algorithm operates on a one bit wide data input, hence it is ideally suited to serial Data Communications applications. In encryption mode, the serial data in is added modulo 2 with the most significant bit (msb) of the 64 bit output vector. The result of this operation is then fed into the least significant bit (lsb) of a 64 bit shift register, and also is used as the serial data output. The shift register is then shifted from the lsb to the msb, and the result becomes the next input vector. After the Data Encryption Standard is completed, the process is repeated again for the next single bit of serial input data. Because each serial data bit requires an entire 64 bit INV and OV, the effective bit rate of this operation is 64 times less than that of a operation which uses all 64 bits of the OV, such as Code Book. Figure 11 shows a block diagram of a OBCFB circuit operating in encryption mode.

To decrypt, the operation is changed in one way. Instead of feeding the result of the modulo 2 adder to the shift register, the unmodified serial data is used. All other operations are identical. Figure 12 shows a circuit which supports both encryption and decryption.

Because the OBCFB algorithm uses a 64 bit shift register on the INV, each SDO bit is a function of its corresponding SDI bit and the 64 previous operations. This implies that the past history of the encryption operation is necessary to initialize a system. The IV is used to supply the history required to allow immediate use of the OV from the DEA. Typically, the IV is either a predefined value, or the last 64 SDO bits from the data stream being encrypted or decrypted. This allows the

encryption process to be accomplished with discrete blocks of data, and hence the WD2001/2 can be used in a multi-channel communications environment.

In OBCFB, the WD2001/2 is always set to encrypt mode. The selection of either the SDI as the feedback element to the shift register, or the SDO as the feedback element, determines whether the incoming data is encrypted or decrypted.

Another factor involved with OBCFB is the propagation of errors through a 64 bit block of data. Because of the 64 bit shift register that feeds the INV, a single bit error will cause the following 63 bits to be in error also. After the last bit of the 64 erred bits, the data will become resynchronized and the effect of the shift register will no longer cause bad data.

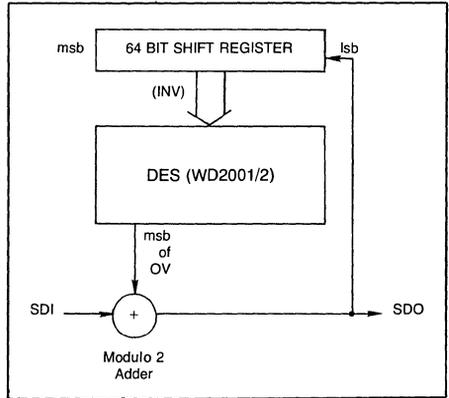


Figure 11 OBCFB ENCRYPTION BLOCK DIAGRAM

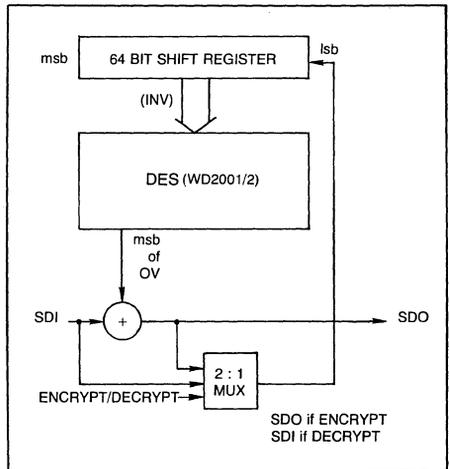


Figure 12

OBCFB ENCRYPTION/DECRYPTION BLOCK DIAGRAM

ONE BIT CIPHER FEEDBACK IMPLEMENTATION

Since the WD2001/2 is a byte input/output oriented device, the implementation of a OBCFB circuit can be accomplished without the 64 bit shift register shown in Figures 11 and 12. Through the use of a 9 bit wide FIFO, a "virtual" 64 bit shift register can be built. Figure 13 illustrates this with a Western

Digital FR1502 FIFO and some common TTL logic.

Once the modulo 2 adder, the encrypt/decrypt selector, and the shift register are defined, the overall circuit can be generated by combining these pieces along with the logic shown in Figure 8. The overall block diagram of the one bit cipher feedback system is given in Figure 14.

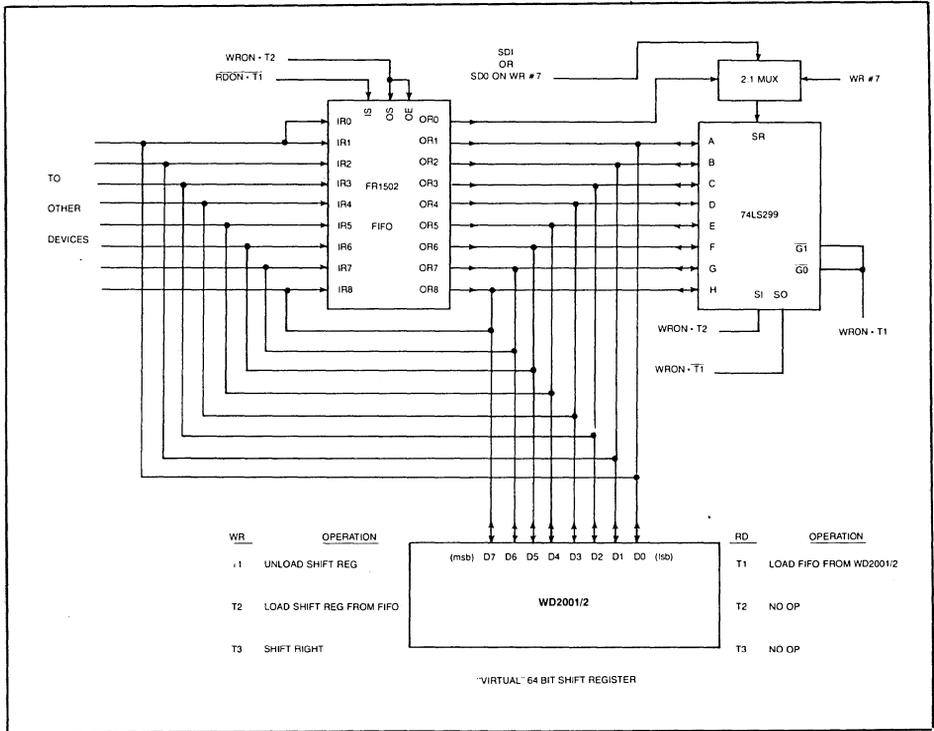


Figure 13 "VIRTUAL" 64 BIT SHIFT REGISTER

1-20-10100

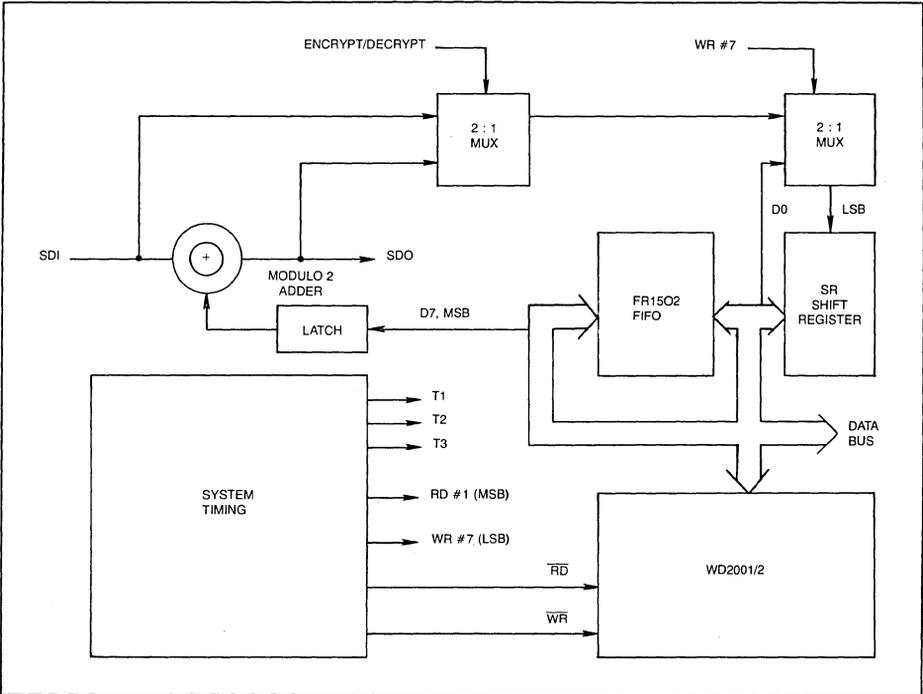


Figure 14 OBCFB SYSTEM BLOCK DIAGRAM

CONCLUSION

The WD2001/2 device lends itself readily to the most common of all Data Communications encryption techniques. The one bit cipher feedback algorithm can be implemented easily through the use of synchronous timing generation and circuit design techniques.

RELATED DOCUMENTS

- WD2001/2 Data Sheet, Western Digital Corporation
- FIPS 46
Federal Information Processing Standard
National Bureau Of Standard
Department of Commerce

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Network Products Data Sheets

WESTERN DIGITAL CORPORATION

PRELIMINARY

LSI PACKET NETWORK INTERFACE WD2501/11 SHORT FORM DATA SHEET

SECTION 1

September, 1980

FEATURES

- Packet Switching Controller Compatible with CCITT Recommendation X.25, Level 2, LAP.
- Programmable Primary Timer (T1) And Retransmission Counter (N2)
- Programmable A-Field Which Provides A Wider Range Of Applications Than Defined By X.25. These Include: DTE-To-DTE Connection, Multipoint, And Loop-Back Testing
- Direct Memory Access (DMA) Transfer: Two Channels; One For Transmit And One For Receive. Send/Receive Data Accessed By Indirect Addressing Method. No External Address Latches Required. Sixteen Output Address Lines.
- Zero Bit Insert And Delete
- Automatic Appending and Testing Of FCS Field
- Computer Bus Interface Structure: 8 Bit Bi-Directional Data Bus. CS, WE, RE-Four Input Address Lines
- DC To *1.6M Bits/SEC Baud Rate

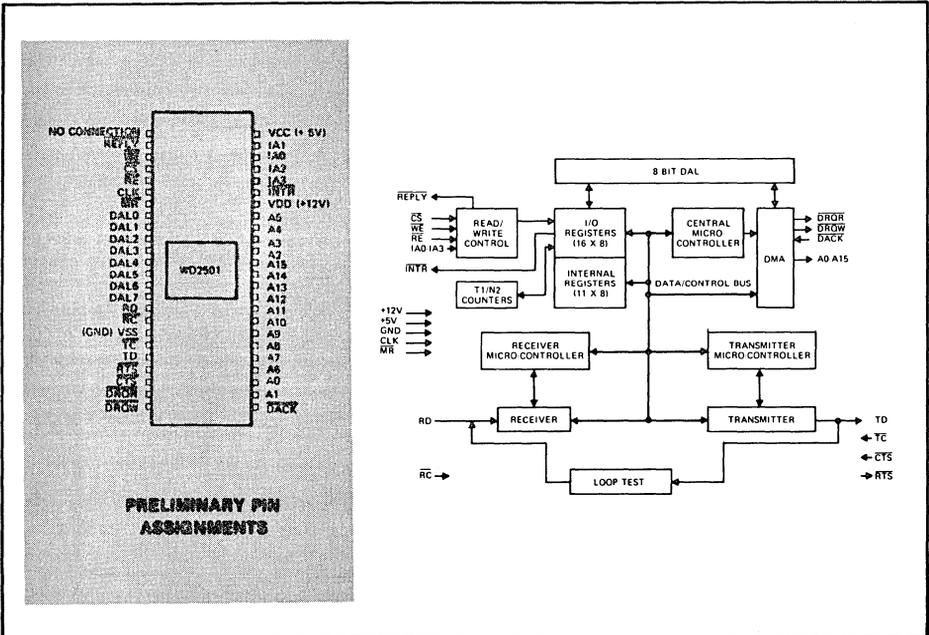
- TTL Compatible
- 48 Pin Dual In-Line Packages
- Pin-for-pin compatible with WD2511 (LAPB.)
- Higher Baud Rates Available By Special Order

APPLICATIONS

X.25 PACKET SWITCHING CONTROLLER
PART OF DTE OF DCE
PRIVATE PACKET NETWORKS

GENERAL DESCRIPTION

The WD2501 is a MOS/LSI device which handles bit-oriented, full-duplex serial data communications with DMA, which conforms to CCITT X.25 with programmable enhancements. The device is fabricated in N-Channel silicon gate MOS technology and is TTL compatible on all inputs and outputs.



*A detailed long form data sheet for this product is available from your local Western Digital Representative.

INTERFACE SIGNAL DESCRIPTION

*PIN NUMBER	SYMBOL	NAME	FUNCTION
48	VCC	Power Supply	+ 5VDC power supply input
42	VDD	Power Supply	+ 12VDC power supply input
18	VSS	Ground	Ground
6	CLK	Clock	Clock input used for internal timing. Must be square wave from 1.0 to 3.0 mHz.
7	$\overline{\text{MR}}$	Master Reset	Initialize on active low. All registers reset to zero, except control bits MDISC and LINK are set to 1. DACK must be stable high before MR goes high.
4	$\overline{\text{CS}}$	Chip Select	Active low chip select for CPU control of I/O registers.
8-15	DAL0-DAL7	Data Access Lines	An 8 bit bi-directional three-state bus for CPU and DMA controlled transfers.
5	$\overline{\text{RE}}$	Read Enable**	The contents of the selected register are placed on DAL when CS and RE are low.
3	$\overline{\text{WE}}$	Write Enable	The data on the DAL are written into the selected register when CS and WE are low. RE and WE must not be low at the same time.
2	$\overline{\text{REPLY}}$	Reply	An active low output to indicate that either a CS•WE or CS•RE input is present.
43	$\overline{\text{INTR}}$	Interrupt Request	An active low interrupt service request output, and returns high when Status Register #1 is read.
47-44	IA0-IA3	Address Lines In	Four address inputs to the 2501 for CPU controlled read/write operation with registers in the 2501. If ADRV = 0, these may be tied to A0 - A3.
26-41	A0-A15	Address Lines Out	Sixteen address outputs from the 2501 for DMA operation. If the control bit ADRV is 1, the outputs are TTL drives at all times. If ADRV is 0, the outputs are 3-state, and are HI-Z whenever DACK is high. (ADRV is in Control Register #1.)
23	$\overline{\text{DRQR}}$	DMA Request Read	An active low output signal to initiate CPU bus request so the 2501 can output onto the bus.

*PIN NUMBER	SYMBOL	PIN NAME	FUNCTION
24	$\overline{\text{DRQW}}$	DMA Request Write	An active low output signal to initiate CPU bus request so that data may be written into the 2501. $\overline{\text{DRQW}}$ and $\overline{\text{DRQR}}$ cannot be low at the same time.
25	$\overline{\text{DACK}}$	DMA Acknowledge	An active low input from the CPU in response to $\overline{\text{DRQR}}$ or $\overline{\text{DRQW}}$. $\overline{\text{DACK}}$ must not be low if $\overline{\text{CS}}$ and $\overline{\text{RE}}$ are low or if $\overline{\text{CS}}$ and $\overline{\text{WE}}$ are low.
20	TD	Transmit Data	Transmitted serial data output
16	RD	Receive Data	Receive serial data input
19	$\overline{\text{TC}}$	Transmit Clock	A 1X clock input. TD changes on the falling edge of $\overline{\text{TC}}$.
17	$\overline{\text{RC}}$	Receive Clock	This is a 1X clock input, and RD is sampled on the rising edge of $\overline{\text{RC}}$. Adjustment of the sample is by quadrant. The sampling may be monitored by the $\overline{\text{RCO}}$ output.
21	$\overline{\text{RTS}}$	Request-To-Send	An open collector (drain) output which goes low when the 2501 is ready to transmit either flags or data. May be hard-wired to ground.
22	$\overline{\text{CTS}}$	Clear-To-Send	An active low input which signals the 2501 that transmission may begin. If high, the TD output is forced high. May be hard-wired to ground.

* PIN NUMBERS ARE PRELIMINARY

** Throughout this document, the term "read" refers to data out of the 2501 and "write" refers to data going into the 2501.

CONTROL, STATUS, ERROR REGISTERS

REGISTER	7	6	5	4	3	2	1	0
CR0	0	0	0	ACTIVE/ PASSIVE	LOOP TEST	0	RECR	MDISC
CR1	0	0	0	ADRV	RRT1	0	0	SEND
SR0	NA2	NA1	NA0	RNRR	NB2	NB1	NB0	RNRX
SR1	¹ PKR	¹ XBA	¹ ERROR		NE2	NE1	NE0	
SR2	T1OUT	$\overline{\text{IRTS}}$	REC IDLE				RANC	$\overline{\text{LINK}}$
ER0	ER07	ER06	ER05	ER04	ER03	ER02	ER01	ER00

¹Causes Interrupt ($\overline{\text{INTR}}$ Goes Low).

BIT	DESCRIPTION
CR07	Unused control bits, like CR07, should be 0.
CR04	This bit will cause the 2501 to initiate link set-up if CR04 = 1, or to wait for a link set-up from the remote device if CR04 = 0.
CR03	The LOOP TEST bit will connect the transmitted data output to the receiver input. The receiver input pin, RD, is gated-out. The "E" and "F" registers of the A-field should be equal.
CR01	This bit is RECR which defines the CPU's receiver buffer as Ready (CR01 = 1) or as Not Ready (CR01 = 0). If RECR = 0, this bit indicates that the CPU has a temporary inability to accept more I-frames, or packets, and the 2501 will transmit an RNR S-frame.
CR00	MDISC is a mandatory disconnect command. MDISC will cause a logical disconnect in the DTE/DCE link. No DMA accessed data may be transferred as long as MDISC = 1. After Master Reset ($\overline{\text{MR}}$ pin transition from low to high), MDISC will be set. The 2501 will neither transmit nor accept received data until MDISC = 0.
CR14	The ADRV bit (CR14) is the control for the 16 bit output addresses (A0-A15). If ADRV = 0, the outputs are 3-state and are in HI-Z, except when $\overline{\text{DACK}}$ goes low. If ADRV = 1, the outputs are always low impedance (TTL), and are high when $\overline{\text{DACK}}$ is high.

BIT	DESCRIPTION
CR13	RRT1 will cause the 2501 to transmit an RR (RECR = 1) or RNR (RECR = 0) at T1 intervals provided the 2501 is not sending a command or waiting for an acknowledgement.
CR10*	The SEND bit (CR10) is used to command the 2501 to send the next packet or packets. If SEND = 1, the 2501 will read from TLOOK the BRDY bit of the next segment for transmission. If BRDY = 0, the 2501 will clear SEND and no action occurs. If BRDY = 1, the 2501 will then read TSADR and TCNT, followed by the transmission of that buffer. After transmission, the 2501 clears BRDY of the segment just transmitted, and reads BRDY of the next segment. If 1, the next segment is transmitted. If 0, the SEND bit is cleared, and transmission of packets is stopped.
SR07-SR05*	NA2-NA0. Next block of transmitted data to be Acknowledged.
SR04	RNRR. An RNR has been received.
SR03-SR01*	NB2-NB0. Next block to be transmitted.
SR00	RNRX. As a result of RECR (CR01) = 0, an RNR has been transmitted.
SR17	<p>The PKR bit stands for Packet Received. This means that a packet has been received error-free and in correct sequence according to the received N (S) count. The data (I-field) has been placed in the CPU's RAM memory. NE is advanced.</p> <p>The three interrupt-causing bits are SR17, SR16, and SR15. Any of the three will cause an interrupt request (INTR goes low) when that bit goes to a 1. After SR1 is read, all three bits are reset to 0, and INTR returns high.</p>
SR16	The XBA bit means that a previously transmitted Block, or Blocks, have been acknowledged by the remote device. Upon acknowledgement, the ACK'ED bit is set to "1" for each segment in TLOOK which was acknowledged.
SR15	<p>The ERROR bit indicates: 1) An error has occurred which is not recoverable by the 2501, or 2) A significant event has occurred. The "significant events" are: change in link status (link-up or down), the 2501 is progressing to the next segment in a chained receive buffer, or one direction of the link has been reset.</p> <p>The exact nature of the reason for the ERROR bit is given in ER0.</p>
SR13-SR11*	NE2-NE0. Next Expected packet segment number of RLOOK.
SR27	T1OUT bit means that timer T1 has timed-out. This bit returns to 0 when T1 is re-started.
SR26	IRTS stands for the Internal Request-To-Send bit, and indicates that the transmitter is attempting (successful or not) to send either data or flags. If the RTS pin is not tied to ground or WIRE-ORED with another signal, then IRTS = RTS.
SR25	REC IDLE indicates that the 2501 has received at least 15 contiguous 1's.
SR21	<p>RANC means that the Received Address field is Not Correct. Either the A-field was from "E" but should have been "F" or vice versa. A CMDR will be transmitted if link was in the information transfer phase.</p> <p>NOTE: If an A-field is neither "E" nor "F", the entire packet is disregarded and not brought into memory by DMA. No action is taken.</p>
SR20	If the link is established, LINK = 0. If the link is logically disconnected, LINK = 1.

*See "Memory Access Method" Section

ERROR REGISTER (ER0)

ER07	ER06	ER05						
0	0	0	ER00 - NOSFR ER01 - ROR ER02 - TUIR ER03 - RPKNR ER04 - RLNR					
0	0	1	ER04	ER03	ER02	ER01	ER00	LINK is up. (Was down) Received DISC while LINK up. DISC sent, sent SARM sent N2 times without UA. DISC sent, REC IDLE for T1xN2.
0	1	0	CHAIN STATUS ER00 - GNCS ER01 - CNR					
1	0		LINK RESET RECEIVED if ER05 - ER00 = 000000 LINK RESET TRANSMITTED if ER05 - ER00 = non-zero ER00 similar to W ER01 similar to X ER02 similar to Y ER03 similar to Z ER05 means received F = 1, but did not send P = 1 ER04 means I-frame was sent N2 times without acknowledge					
1	1		COMMAND REJECT RECEIVED if ER05 - ER00 = 000000 TRANSMITTED if ER05 - ER00 = non-zero ER00 = W ER01 = X ER02 = Y ER03 = Z ER04 = Z1					

- NOTES:**
- Whenever a command reject (CMDR) is received, the I-field will have been placed in appropriate memory by DMA, and a link reset SARM will be transmitted. The NB is not advanced.
 - Definitions of W,X,Y,Z as stated in CCITT X.25. Z1 indicates received N(S) is invalid (not part of X.25).

TERMS USED IN ERROR REGISTER

GNCS Going to Next Chain Segment

ROR Receiver Over-Run. The Receiver Register (RR) had a character to load into the FIFO, but the FIFO was full.

RLNR RLOOK Not Ready. REC RDY bit of next segment is 0.

RPKNR Received Packet but Memory Block was Not Ready.

TUR Transmitter Under-Run. The Transmitter Register (TR) needed a character from the Transmitter Holding Register (THR), but the THR was not ready.

NOSFR No S-frame received for T1 x N2. Used only if RRT1 = 1.

MEMORY ACCESS METHOD

The memory access method, which includes DMA, is designed to take full advantage of the bit-oriented protocol which allows up to 7 I-frames to be outstanding (i.e., unacknowledged) in each direction of a communications link. The memory access method used two "look-up" tables: One for transmit and one for receive. These tables contain addresses and control for the individual send/receive packets. Thus, packet data are DMA addressed indirectly. This method is best suited for most software applications.

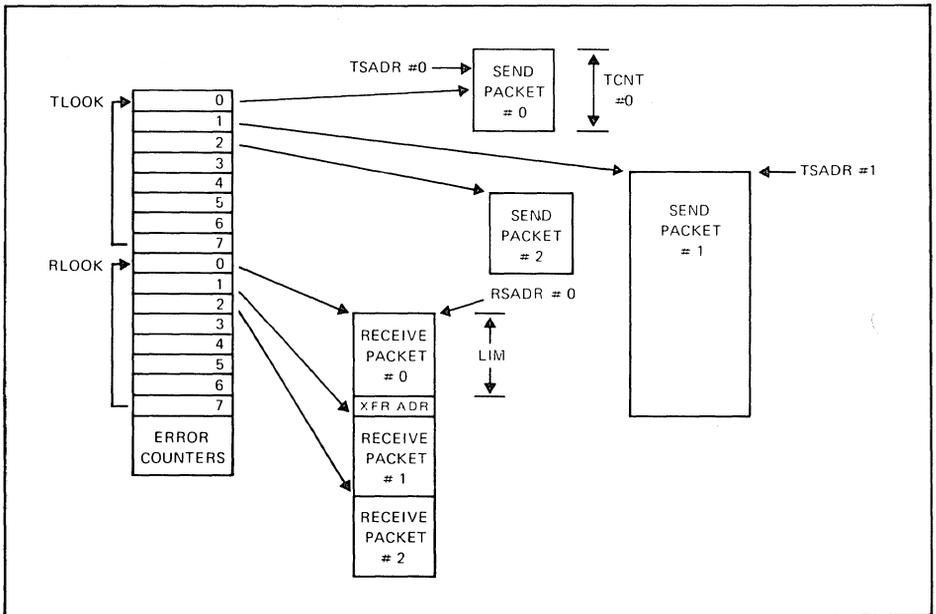
The 16 bit starting address for the look-up table TLOOK is loaded into the 2501 by the CPU. (I/O Registers "A" and "B"). RLOOK must immediately follow TLOOK in contiguous fashion. TLOOK and RLOOK are in the RAM memory external to the 2501. There are a total of 8 segmented control sections for each table. Each segment contains eight bytes. Four bytes are used for

data memory starting address and length, two bits of one byte are used for control, one byte defines variable bit length and residual, and the other two bytes are open for user definition.

In transmit, the 2501 will have read from TLOOK the starting address and length of the first packet to be transmitted. The 2501 will automatically transmit the flag, address, and control fields. Next, the information field data will be transmitted using DMA from the "SEND #0 PACKET" memory. At the end of the information field, the 2501 will automatically send the FCS and closing Flag. The 2501 will then move on to the next packet.

If retransmission of one or more (up to seven) packets becomes necessary, the 2501 will automatically retrace the previous transmissions through the TLOOK table. The user's CPU software does not become involved in the retransmission. However, an ERROR COUNTER is incremented. (See Error Counter Section.)

To receive, each frame is checked for correct address and FCS fields and for type of control field. If the frame is a packet, the information field is placed in the assigned memory location in a method similar to that used in transmit. After the packet is received error-free and in proper N(S) sequence count, an interrupt is generated, and the 2501 is ready for the next packet which will be placed in the next location.



MEMORY ACCESS SCHEME

"DEADLY EMBRACE" PREVENTION

A "deadly embrace" can occur when two processors reach a state where each is waiting for the other. In this case, the two processors are the user's CPU and the micro-controller inside the 2501. Therefore, to prevent the "deadly embrace", the following rule is obeyed by the 2501 and should also be obeyed by the user's CPU. This rule applies to TLOOK, RLOOK, and to the I/O registers. The Error Counters do not apply to this rule.

RULE: If a bit is set by the CPU, it will not be set by the 2501, and vice versa. If a bit is cleared by the 2501, it will not be cleared by the CPU, and vice versa.

As an example, the BRDY bit in the TLOOK segment is set by the CPU, only, but cleared by the 2501, only.

ERROR COUNTERS

Following contiguously after RLOOK is ten 8 bit error counters. The 2501 will increment each counter at

the occurrence of the defined event. However, the 2501 will not increment past 255 (all 1's). The CPU has the responsibility of clearing each counter. The first counter past RLOOK is #1, etc.

ERROR COUNTER	COUNT
1	Received Frames with FCS Error
2	Received Short Frames (less than 32 bits)
3	Number of times T1 ran-out (completed)
4	Number of I-Frame Retransmissions
5	REJ Frames Received
6	REJ Frames Transmitted
7	Invalid Commands Received
8	Invalid Responses Received
9	Number of frames which I-field exceeded total Limit.
10	Number of Null Packets Received

BYTE # IN SEGMENT	7	6	5	4	3	2	1	0
1	ACK'ED	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	BRDY
2	TSADR HI							
3	TSADR LO							
4	SPARE				TCNT HI			
5	TCNT LO							
6*	SBL2	SBL1	SBL0	BL1	RES2	RES1	RES0	BL0
7	SPARE FOR USER DEFINITION							
8	SPARE							

TLOOK SEGMENT

BYTE # IN SEGMENT	7	6	5	4	3	2	1	0
1	FRCML	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	REC RDY
2	RSADR HI							
3	RSADR LO							
4					RCNT HI			
5	RCNT LO							
6*	SBL2	SBL1	SBL0	BL1	RES2	RES1	RES0	BLO
7	SPARE FOR USER DEFINITION							
8	SPARE							

*Byte #6 defines variable bit length and residual bits.

RLOOK SEGMENT

BRDY means that the transmit buffer is ready. The 2501 will send the block only after the CPU makes BRDY = 1. (BRDY is used in conjunction with the SEND bit.) At the completion of the transmission, the 2501 will make BRDY = 0, and then read the BRDY of the next segment.

After transmitting a packet, an acknowledgement must be received from the remote device. The acknowledgement is contained in the received N (R) count of an I-frame, RR frame, or RNR frame. Upon acknowledgement, the 2501 will make ACK'ED = 1, and generate a block-acknowledged interrupt. Before assigning a new block to a segment in TLOOK, the CPU must make sure that the previous block which used that segment number has been acknowledged.

REC RDY informs the 2501 that the receive buffer is ready. The 2501 will not receive a packet into a buffer referenced by a particular segment until REC RDY = 1. If the 2501 progresses to a segment which has REC RDY = 0, an error interrupt will be generated.

After receiving an error-free packet in proper sequence, the 2501 will set FRCML, clear REC RDY, and generate a Packet Received Interrupt. The 2501 will also write the value of the binary length of the received packet in RCNT HI and RCNT LO. The NE count is advanced. The 2501 will acknowledge received packets at the first opportunity. This will be in either the next transmitted I-frame, or by an RR frame if RECR = 1, or by an RNR

frame if RECR = 0. (RECR is in CRO.)

In the address bytes, HI represents the upper 8 bits and LO represents the lower 8 bits. In the count bytes, HI represents the upper 4 bytes.

TSADR is the starting address of the buffer to transmit, and TCNT is the binary count of the number of characters in the I-field.

RSADR is the starting address of the receive buffer. After successfully receiving the packets, the 2501 will write the value of RCNT which is the binary count of the number of characters in the I-field.

Whether the 2501 accesses a look-up table or a memory block, a DMA Cycle is required for each access.

TLOOK AND RLOOK POINTERS

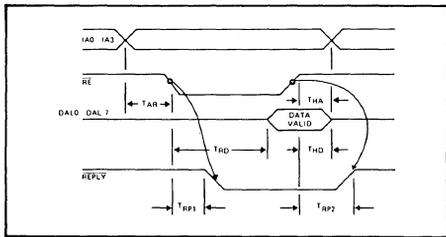
There are three 3-bit counters for the status of the segments in TLOOK and RLOOK. Status Register #0 (SRO) contains counters NA and NB which are used in conjunction with TLOOK. NB is the segment number of the next block to be transmitted, and is advanced at the end of each DMA transmission. NA is the value of the segment of the next block which will be acknowledged. If all transmitted blocks have been acknowledged, then NA = NB.

In SR1 is a 3-bit counter, NE, used with RLOOK. NE is the value of the segment number where the next received packet will be placed.

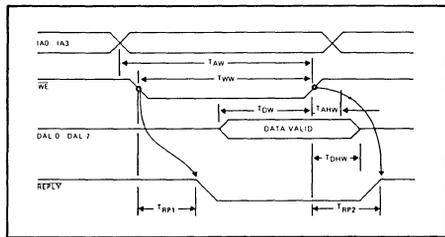


PRELIMINARY TIMING SPECIFICATIONS

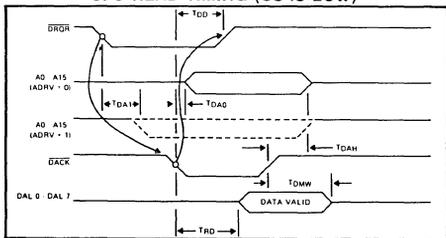
SYMBOL	PARAMETER	MIN. (NS)	MAX. (NS)	COMMENT
T _{AR}	Input Address Valid to \overline{RE}	0		
T _{RD}	Read Strobe (or \overline{DACK} Read) to Data Valid	200		C (DAL) = 50 pf C (DAL) = 100 pf
T _{HD}	Data Hold Time from Read Strobe		80	
T _{HA}	Address Hold Time from Read Strobe	80		
T _{AW}	Input Address Valid to Trailing Edge of \overline{WE}	200		
T _{WW}	Minimum \overline{WE} Pulse	200		
T _{DW}	Data Valid to Trailing Edge of \overline{WE} or Trailing Edge of \overline{DACK} for DMA Write	100		
T _{AHW}	Address Hold Time after \overline{WE}	80		
T _{DHW}	Data Hold Time after \overline{WE} or after \overline{DACK} for DMA Write	80		
T _{DA1}	Time from \overline{DRQR} (or \overline{DRQW}) to Output Address Valid if ADRV = 1		80	C (ADDRESS) = 100 pf
T _{DA0}	Time from \overline{DACK} to Output Address Valid if ADRV = 1		360	C (ADDRESS) = 100 pf
T _{DD}	Time from Leading Edge of \overline{DACK} to Trailing Edge of \overline{DRQR} (or \overline{DRQW})		200	C (\overline{DRQ}) = 50 pf
T _{DAH}	Output Address Hold Time from \overline{DACK}		120	
T _{DMW}	Data Hold Time from \overline{DACK} for DMA Read		80	
T _{RP1}	\overline{REPLY} Response Leading Edge		160	C _{LOAD} = 50 pf
T _{RP2}	\overline{REPLY} Response Trailing Edge		240	C _{LOAD} = 100 pf
			200	C _{LOAD} = 50 pf
			260	C _{LOAD} = 100 pf



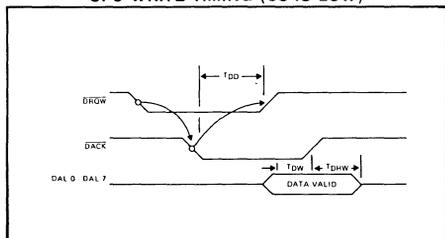
CPU READ TIMING (\overline{CS} IS LOW)



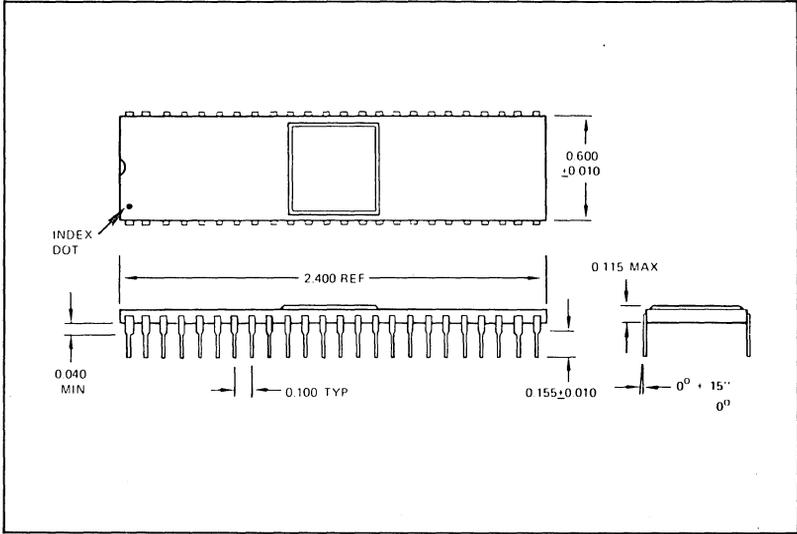
CPU WRITE TIMING (\overline{CS} IS LOW)



DMA READ TIMING



DMA WRITE (A0-A15 SAME AS DMA READ)



WD2501 CERAMIC PACKAGE

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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WDK25001-XC PAC KIT

FEATURES

- WD2501 X.25 PACKET NETWORK INTERFACE CHIP
- RS-423 INTERFACE
- CRYSTAL AND BAUD RATE GENERATOR INCLUDED
- DMA MEMORY INTERFACE
- INCLUDES ASSEMBLY AND OPERATIONS MANUAL
- RAM/ROM/EPROM SOCKETS PROVIDED
- LARGE WIRE-WRAP AREA ON BOARD FOR PROTOTYPING

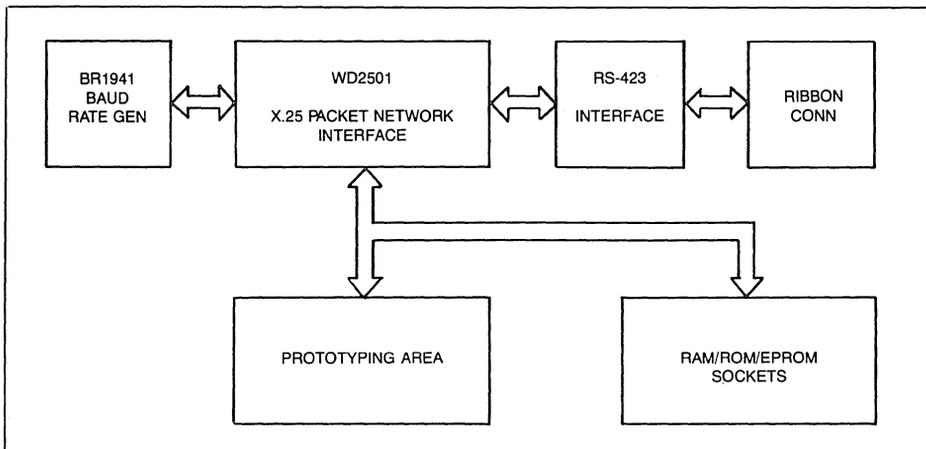
APPLICATIONS

- X.25 DEVELOPMENT
- PACKET NETWORK EDUCATIONAL COURSES
- SYSTEM PROTOTYPING

GENERAL DESCRIPTION

The Western Digital Corporation WDK25001 XC PAC-KIT is a X.25 development kit featuring the WD2501 Packet Network Interface chip. The PAC KIT provides for easy interface to a local microcomputer or a Host System bus, along with a RS-423 serial Communications interface.

FEBRUARY, 1981



WDK25001-XC BLOCK DIAGRAM

1 2011-01-01



A MCGRAW-HILL PUBLICATION

Electronics

SEMICONDUCTORS

WD2511 LSI circuit simplifies packet-network connection

by Geary L. Leger, *Western Digital Corp., Newport Beach, Calif.*



Chip
opens door
to packet
switching

Technical articles

LSI ready to make a mark on packet-switching networks

New chip's link-control capabilities ease connection to terminals: Part I

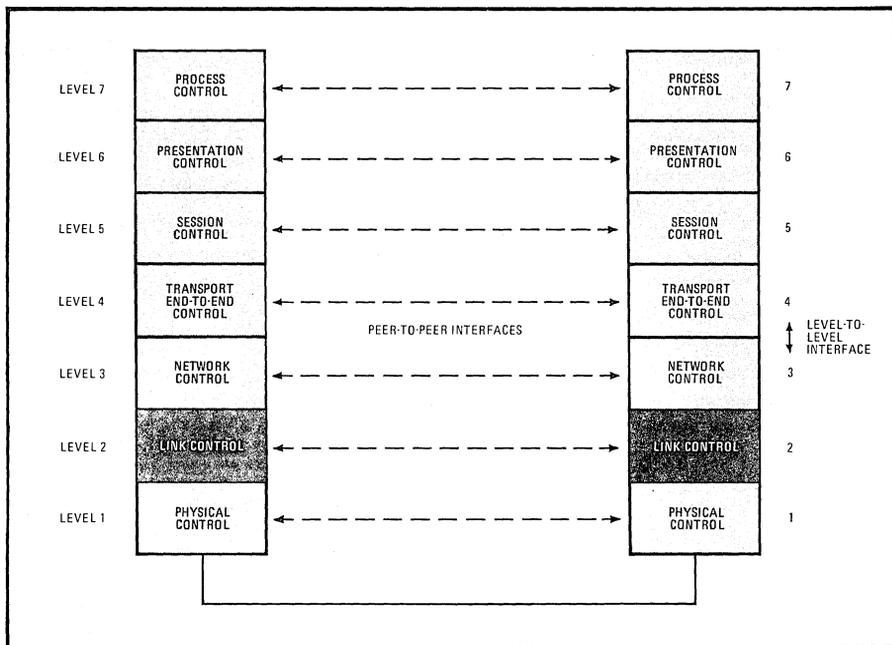
by Geary L. Leger, Western Digital Corp., Newport Beach, Calif.

□ Packet-switching networks are prime targets for the application of large-scale-integrated circuit technology. In fact, sometime during the first quarter of next year, this useful and expanding approach to data communica-

tions will have its first dedicated LSI circuit, one designed to take advantage of LSI's potential for lower cost and greater reliability.

The circuit is the Micro Packet Interface chip, or μ PAC, being developed by Western Digital. It will handle Level 2 control of the link between a data terminal and a network node as set forth in the X.25 protocol established by the Consultative Committee for International Telephony and Telegraphy (CCITT). Because these

This is the first of two articles. It deals with the overall characteristics of packet-switching networks. Part 2, which starts on page 95, describes an LSI chip being developed for Level 2 control per the X.25 protocol for packet networks.



1. Layered architecture. Independence among system levels allows changes to be made to one level without disrupting the operation of other levels; and adjacent level is affected only if the changes affect the interface to that level. Standards apply to peer-to-peer interfaces.

Recent efforts in packet switching

The security, survivability, and economic advantages of packet-switching data-communications networks have not gone unnoticed in either the military or the corporate sectors. Though still in its infancy, this type of communication is growing rapidly.

According to Defense Advanced Research Project Agency director Eugene H. Kopf, the latest military packet effort aims to find the optimum architecture for a command and control network of 5,000 to 10,000 small packet radio relay terminals whose purpose would be to insure survivable control over strategic weapons. The network voice and data-packet radios would provide line-of-sight communications throughout the continental U. S. after an attack.

The civilian sector has continued the development of packet networks from their modest beginnings. In 1972, Bolt Beranek & Newman Inc. founded Telenet, a public packet-switching network taken over this year by General Telephone & Electronics Corp. GTE Telenet Communications Corp., Vienna, Va., completed installation this month of a packet-switching exchange in San Juan, Puerto Rico, for ITT World Communications Inc. The new service allows businesses and industrial organizations to link to the ITT gateway and transmit and receive data over shared transmission lines to data terminals or computers on the U. S. mainland.

Tymnet Inc., Cupertino, Calif., is the largest public packet-switching network in the U. S. It has so many customers that it issues a 34-page directory describing 200 data bases accessible through its network. Tymnet now serves 250 computers in the U. S.; it recently added New Zealand

to its list of countries served, bringing the total to 26.

The Japanese have not been idle in adapting packet technology to their needs. Nippon Telegraph and Telephone Public Corp. started work on its digital data-exchange system in 1971 and had installed packet-network equipment in seven cities by late 1978. This commercial packet-switching network (called D50) is expected to go into full service this year. D50 conforms fully to Recommendation X.25 of the Consultative Committee for International Telephony and Telegraphy.

The packet network industry has come a long way since the first operational system (Arpanet) was installed by the Defense Advanced Research Projects Agency in 1969. In 1976, the CCITT adopted X.25 as a standard three-level protocol for interfacing terminals to public packet networks—a major step for the industry. Even though it has been criticized as being too complicated, X.25 has stimulated interest in packet networks.

However, packet switching is not the answer to all data and voice communications problems, as some have claimed. Gino J. Coviello of the Defense Communications Agency in Arlington, Va., concluded in a recent study that the number of channels traversing a particular transmission link and the network topology and architecture have a significant impact on the cost-effectiveness of a packet-switching network. Ray W. Sanders, president of Computer Transmission Corp., says, "Packet switching will take its rightful place alongside circuit switching." A hybrid approach combining features of both circuit and packet switching "provides the best of all possible worlds," according to Sanders. **-Harvey J. Hindin**

networks are relatively new, familiarity with the Level 2 link control and other details of their operations is not widespread. Yet the purpose of the μ PAC is intelligible only in the context of such an understanding.

To date, most data-communications systems use circuit-switching techniques. A physical circuit is assigned either permanently (a private, leased line) or for the duration of the call (a dial-up line). But of a given line's total available time, only a small percentage is actually taken up by data transmission. A system for dynamic allocation of the physical circuits, in contrast to static circuit-switching allocation, requires the logic and memory capabilities of computers.

Prior to the late 1960s, static circuit allocation was more economical than using computers in a dynamic allocation system. The low cost of today's minicomputers and microprocessors and the dramatic drop in the cost of memory, however, make dynamic allocation more economically feasible in many cases. It is most suitable in multipurpose applications—digital communications systems linking various types of data terminals such as facsimile machines, computerized data bases, interactive keyboard printers, or cathode-ray-tube terminals.

Historically, communications systems have been developed to satisfy one application at a time. The wide variety of computers, terminals, and technologies has led to the development of many incompatible networks. A time-sharing network may connect many asynchronous interactive keyboard printers on dial-in lines at 110 or

300 bits per second. A clustered CRT application such as IBM's 3270 may operate synchronously at 1,200, 2,400, or 4,800 b/s.

The incompatibility of different types of equipment and the protocols they use for communicating greatly reduces the reliability and efficiency of data communications as a whole. A single corporation may, for example, use several incompatible networks.

Security and survivability

The technique of sending a digital data in short packets, rather than in a continuous stream, was first suggested by Paul Baran of the Rand Corp. more than a decade ago. The packets are transmitted between intermediate points in the network, called nodes, or DCEs, for data-circuit-terminating equipment (see table).

This dynamic-allocation technique has two major inherent advantages over circuit-switching methods. It increases data security, since the message is broken up: all the packets would have to be picked up and combined by an intruder before he could use the data. And system survivability and reliability are enhanced by the large number of linked nodes. Alternate routes will get a message through if some of the nodes or links are malfunctioning or destroyed. The security and survivability are of great interest to the military. The commercial sector is also developing this type of system (see "Recent efforts in packet switching," above).

The problem of equipment and communication-proto-

col incompatibility is an international one, since data communications is international. This question is addressed at the global level by the CCITT (see "Setting the standard," p. 93).

The difficulty of expanding, modifying, or upgrading existing data-communications networks is another problem that is tackled by the new packet-switching systems. Any communications system represents a large capital investment, and down time can be disastrously expensive. A user cannot simply tear down an old network and substitute a new one with the latest advances. New terminals and technologies must be phased into the existing structure without interrupting operation. This calls for a degree of system flexibility.

Layered architecture

Packet-switching networks achieve this flexibility through layered (or multilevel) architecture [*Electronics* May 24, 1979, p. 111]. Several standards organizations have been working on the specifics of this concept.

The importance of layered structure is easy to understand. Suppose Mr. Jones, an executive, wishes to talk to Ms. Smith, another executive. Jones (level 4) tells his secretary (level 3) to get Smith on the line. Jones' secretary dials the number (level 2). An electromechanical switching mechanism connects the two phones (level 1). Smith's phone rings (level 2). The two secretaries converse (level 3) and pass on the information that the call is ready to their bosses. Smith and Jones now communicate (level 4).

Jones was never concerned with the electromechanical switching mechanism, nor with Smith's telephone number; he was primarily concerned with talking to Smith (peer to peer) and secondarily with talking to his secretary to get the call set up.

Multilevel communications systems are structured in a similar fashion. The protocol standards are prepared for connection in the peer-to-peer layer. Standards do not define the interface between adjacent layers. This is intentional: terminal manufacturers are thus left free to design the adjacent-layer interface in their own way. This enhances system flexibility. If a layer is changed or upgraded, nonadjacent layers are not affected.

X.25 defines and standardizes three levels. There are as many as four more definable levels (Fig. 1), but much work remains to be done to standardize these higher levels. Level 1 may be viewed as a data-exchange mechanism serving Level 2. Level 2 is a data-exchange mechanism serving Level 3, and so on.

Three standardized levels

Level 1 concerns itself with the link's physical interfaces. Level 2 deals with link control. It includes setting up and disconnecting a link, the control of flow between data generators and data receivers, and bit-oriented frame structure. The μ PAC from Western Digital is designed to perform the Level 2 functions. Level 3, network control, includes the procedures for establishing and disconnecting the virtual circuit and for controlling the flow of data packets in the network.

In a packet network, the sender or receiver has a terminal (commonly called DTE, for data-terminal equip-

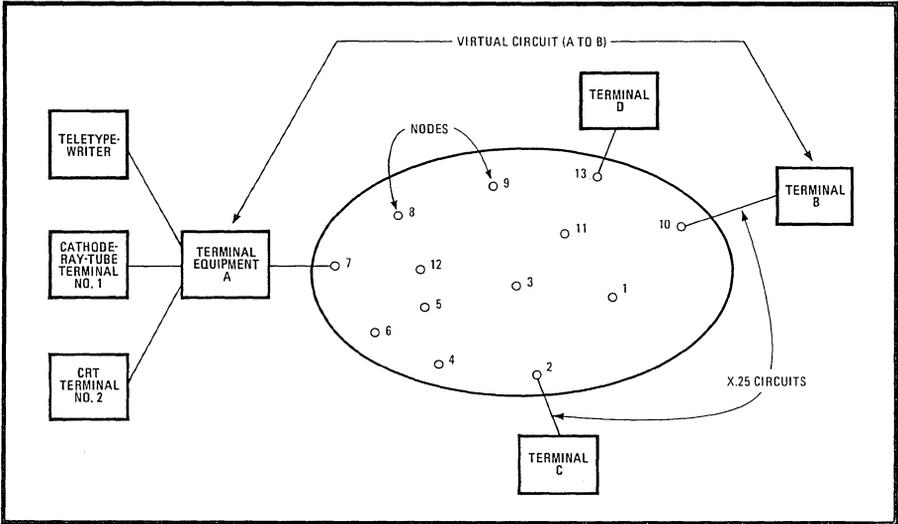
PACKET-SWITCHING NETWORK TERMINOLOGY

ADCCP	Advanced Data-Communications Control Procedure (ANSI X3.66)
ANSI	American National Standards Institute
ATDM	asynchronous time-division multiplexing
BOP	bit-oriented protocol
CCITT	Consultative Committee for International Telephony and Telegraphy
DCE	data-circuit-terminating equipment (network node)
DTE	data-terminal equipment (user's terminal)
FCS	frame check sequence
HDLC	High-level Data-Link Control protocol (ISO 3309)
ISO	International Standards Organization
ITU	International Telecommunications Union
I frame	information frame, known as a packet under X.25
LAP	Link-Access Procedure (X.25)
LAPB	Link-Access Procedure, Balanced (X.25)
Link control	X.25 Level 2 control for linking DTE and DCE, including link initialization, establishment, and disconnection, and control of data flow on the link
Network control	X.25 Level 3 control of virtual circuits in network, including circuit establishment, disconnection, and reset, and the control of packet flow
N1	maximum number of bits in a packet
N2	maximum number of command retransmissions
PAD	Packet Assembly/Disassembly facility (defined in CCITT recommendations X.3, X.28, and X.29)
Physical interface	X.25 Level 1 specifications for the physical connection of DTE and DCE, including electrical parameters and transmission rate
S frame	supervisory frame
SDLC	Synchronous Data-Link Control protocol
T1	t time minimum before retransmission of unacknowledged command
U frame	unnumbered frame
X.25	CCITT recommendation for packet-switching network protocols (others include X.3, X.28, and X.29)

ment) with a distinct address. Part of the gear at a network node might also be called data-terminal equipment. The packets of data are transferred from node to node and finally to the receiver's terminal.

When a node receives a packet, it stores the packet, decides where and when to forward it on the basis of the packet's destination and priority and the load conditions of the network, and then does so. This store-and-forward facility is the key to the network's ability to allocate circuits dynamically. Packets going from terminal A to terminal B, in Fig. 2 could follow the node path 7-12-11-10, 7-5-3-1-10, or any of a number of others.

Dynamic routing within the network is transparent to the users at their terminals. The path data takes is called a virtual circuit between A and B; the terminals communicate as if a dedicated circuit joined them. In order to



2. Many possible paths. The user of a packet-switching network at his terminal sees no difference between the virtual circuit and an ordinary physical link. Network control may send the data packets through a changing series of nodes as system traffic conditions change.

establish a virtual circuit, terminal A transmits a call-request packet that includes the caller's address and the address of terminal B, the destination. Terminal B accepts the request by returning a call-accepted packet to A, and the virtual circuit is set up.

Circuit sharing

Several simultaneously active virtual circuits can be set up by interleaving packets. This asynchronous time-division multiplexing (ATDM) exploits the fact that a typical virtual circuit carries data for only a small percentage of the time it is set up. It differs from other time-division multiplexing schemes in that a dedicated

time slot is not provided for each virtual circuit being multiplexed.

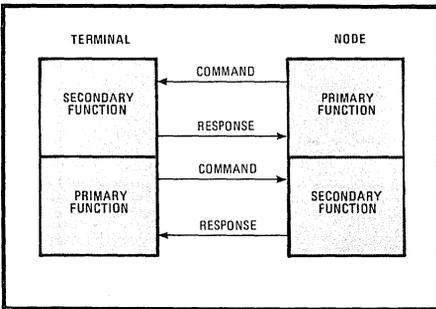
In the multilevel packet-switching architecture, Level 2 (also known as the link level or the frame level) involves the point of contact between the subscriber's terminal and the network node it is linked to directly.

Each station, be it terminal or node, has two logical functions needed for addressing and signal implementation, called primary and secondary (Fig. 3). The primary function transmits commands and receives responses; the secondary function does the reverse—it receives commands and transmits responses.

The structure of the data frames used for this communication is common to all bit-oriented protocols (BOPs)—High-level Data-Link Control (HDLC), the essentially similar Advanced Data-Communication Control Procedures (ADCCP), and the Synchronous Data-Link Control (SDLC) protocol worked out by IBM [*Electronics*, Jan. 18, 1979, p. 137]. The Level 2 protocol defined by X.25 is an outgrowth of HDLC.

The frame is simply a block of serial data exchanged between two terminals or a terminal and a node. It consists of a flag, an address field (or A field), a control field (or C field), an information field (or I field), a frame-check sequence (FCS), and another flag. Depending on the frame type, the information field may or may not be included.

There is a flag at either end of a frame; a single flag may close one frame and open the next. Data transparency is provided within the frame by the transmitting station: a logic 0 is inserted after all sequences of 5 contiguous logic 1 bits, so that no transmitted data is inadvertently read as a flag, which has the binary form



3. Addressable functions. A terminal or node has a primary function that sends commands and receives responses. Its secondary function, which has a different address, responds to received commands. Arrows represent system logic, not physical wires.

Setting the standard

International interface standards are vital to the development and growth of packet-switching networks. Standards lead to lower costs for equipment bought by network users, since this equipment can be manufactured in much larger quantities. The user also benefits from the interchangeability of gear from different vendors. Manufacturers reap the rewards of a global market rather than a local one, and network organization is made vastly easier.

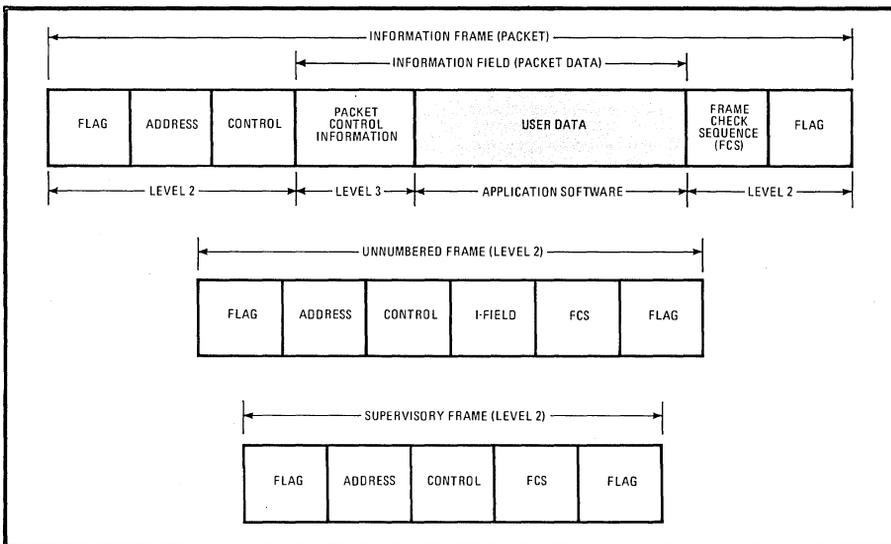
A number of U. S. and international standards organizations are working together to set up interface rules. The International Telecommunications Union (ITU), formed in 1865, operates under the auspices of the United Nations. Under the ITU is the Consultative Committee for International Telegraphy and Telephony (CCITT), which is primarily an organization of carriers.

Study Group VII is a CCITT organization that handles

public data networks. SG VII is responsible for publishing a number of standards or recommendations for packet-switching networks. The best known of these is Recommendation X.25.

The International Standards Organization (ISO), which is composed of representatives from the manufacturing and user community, works closely with the CCITT; the ISO also has a group under its wing with responsibility for public data networks.

In the U. S., the American National Standards Institute (ANSI) is a clearinghouse that coordinates activity for voluntary standards. Its X3S37 committee, which has the responsibility for public data networks, does liaison work as well as coordination. This committee represents a cross section of U. S. industry: manufacturers, users, and carriers. It offers inputs to both the ISO and the CCITT.



4. Standard frames. Three types of data frames may be sent over a packet network. All data except the user data in the information field of an information frame is system overhead required for synchronization, data checking, verification, and bookkeeping functions.

0111110. The receiving station automatically deletes the inserted 0s from the data.

The frame-check sequence is the last 16 bits before the closing flag. They are produced by a calculation that checks all data between the opening flag and the first bit of the FCS. The logic 0s inserted for data transparency are not checked.

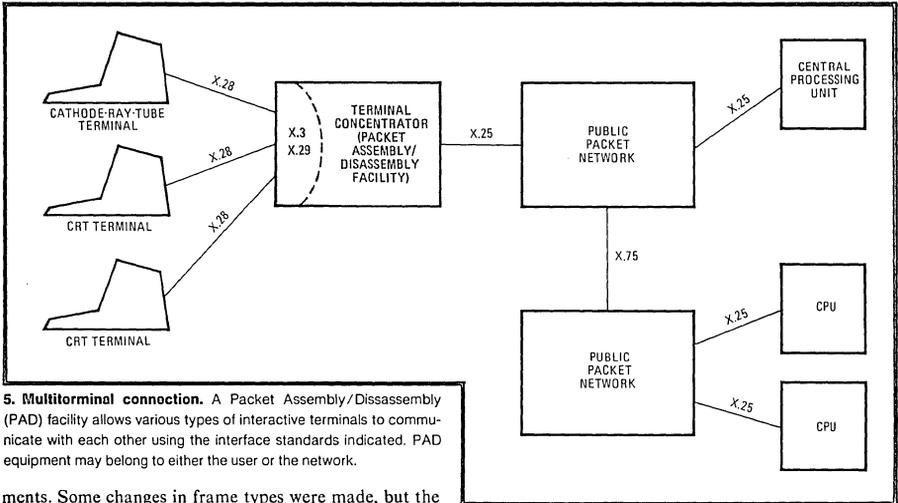
A frame may be one of three types (Fig. 4): a supervisory frame (or S frame), an unnumbered frame (or U frame), or an information frame (or I frame).

Level 2 control does not involve itself with the data within the information field of an information frame. It

simply encloses the packet data in an HDLC frame and sends it out onto the network.

Supervisory frames are used to perform supervisory control of a link, such as acknowledging packets, requesting retransmission of packets, and requesting temporary suspension of transmission. Unnumbered frames are used to set up, disconnect, and reset links.

The Level 2 protocol may take one of two forms: Link-Access Procedure (LAP) and Link-Access Procedure, Balanced (LAPB). When it was originally written in 1976, Recommendation X.25 contained LAP only. LAPB has been added since that time, offering some improve-



5. Multiterminal connection. A Packet Assembly/Disassembly (PAD) facility allows various types of interactive terminals to communicate with each other using the interface standards indicated. PAD equipment may belong to either the user or the network.

ments. Some changes in frame types were made, but the primary differences between LAP and LAPB are in the functions that set up, disconnect, and reset links. (Two models of the μ PAC, the WD 2501 and the WD 2511, are geared to the LAP and the LAPB, respectively.)

There are four system parameters defined by the X.25 Level 2 protocol: T1, N2, N1, and k. T1 is the time limit set for the primary timer; when T1 runs out, an unacknowledged command may be retransmitted. N2 is the limit set for a counter that is incremented each time a command is retransmitted because time T1 ran out without its being acknowledged. N1 is the maximum number of bits in a packet; it depends on the maximum length of the information field. And k is the maximum number of sequential packets that a terminal or node may have outstanding (transmitted but unacknowledged) at any given time. In the μ PAC, T1, N2, and N1 are programmable. The number k can never exceed seven under X.25, and it is fixed at seven in the μ PAC.

Multiplexing terminals

Since each user of the packet network typically has many different types of data generators and receivers, multiplexers must connect the network to the existing equipment. This multiplexer has been defined by the CCITT as the Packet Assembly/Disassembly (PAD) circuit (Fig. 5). The PAD is specifically for use with asynchronous terminals; it combines or separates the multiple signals that are sent to or received from the network.

CCITT protocol standards X.3, X.28, and X.29 are used together to define a PAD interface. A PAD facility may be viewed as a terminal concentrator that connects several asynchronous terminals to a single X.25 link. The PAD circuit is sometimes called an interactive-terminal interface because in practice most terminals connected to PAD interfaces require human interaction via keyboards and CRT displays or printing equipment.

When a PAD interface is used between the packet network and the terminals, two stations that are incompatible by themselves can communicate. They need only be able to talk to the PAD. The μ PAC chips will allow them to do this. Another advantage of this approach is that new types of equipment added at a terminal are transparent to the network.

On the other hand, changes and improvements within the packet network are transparent to the user. These improvements could include increasing node-to-node communication speed, increasing the number of nodes, and changing node-to-node connections to fiber optics.

Variations on the theme

Many packet systems are available; they vary according to the network organization. Several networks, such as Montreal-based Bell Canada's Datapac, offer (in addition to the standard virtual circuit) a permanent virtual circuit that requires no call for link establishment and is continually available.

Another possible service, Datagram, when made available, will not require the initial establishment of a virtual circuit. In this approach a packet is merely put out on the line—typically by users of so-called transaction-based networks. There is no call procedure, and duration of connection is not of concern for billing purposes. Users may, for example, pay a flat fee. Short, independent data bursts will ultimately work their way through the network to their destinations.

A closed user group, available from Datapac and others, is like a private network. Users in a group, actually connected to a public network, can communicate with one another, but access is barred to and from all other users of the network. AT&T's proposed Advanced Communications Service includes this feature; the company calls it a virtual subnetwork. □

WD2511 LSI circuit simplifies packet-network connection

48-pin chip replaces entire board
and thousands of lines of software

by Geary L. Leger, *Western Digital Corp., Newport Beach, Calif.*

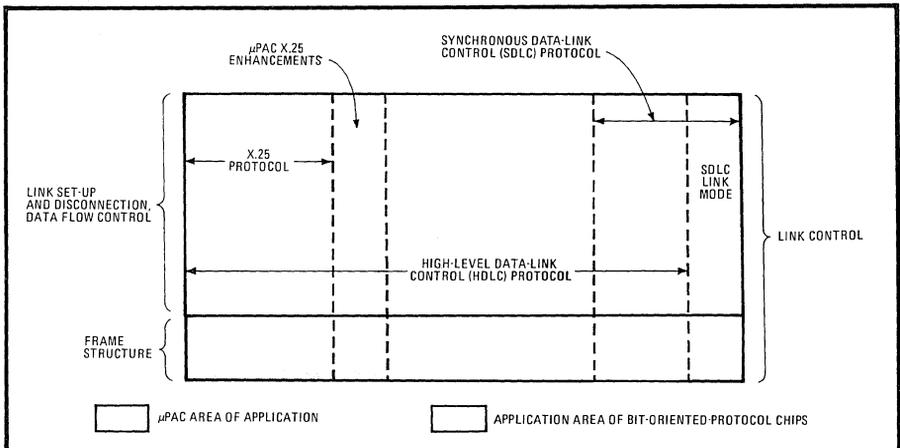
□ Packet-switching data-communications technology can now claim its first dedicated large-scale integrated circuit. Called the Micro Packet Network Interface chip, or μ PAC for short, it is a complete X.25 Level 2 controller with on-chip bidirectional direct-memory-access facilities. This n-channel silicon-gate MOS chip in a 48-pin package replaces a board full of electronics.

The μ PAC goes way beyond the functions performed by the bit-oriented-protocol (BOP) control chips currently in widespread use. It includes the circuitry of a BOP chip. But it handles many other operations, eliminating the need for separate DMA circuits and associated address latches, timing chips, and the system software (more than 1,000 lines of code) required until now to perform Level 2 control of the link between a data terminal and a node of a packet-switching network. It has an 11-K read-only memory and the equivalent of three microprocessors: one to handle data-transmission operations, another for dealing with received data, and a third central processor to coordinate all chip functions. Sample quantities of the controller will be available from

Western Digital Corp. in the first quarter of 1980.

The data-link controllers already on the market (Western Digital 1933, Signetics 2652, Intel 8273, Zilog SIO, and others) handle BOP frame structure in a broad range of applications. For example, the WD 1933 can be used with the High-level Data Link Control (HDLC) and Synchronous Data-Link Control (SDLC) protocols, including the SDLC loop mode. This chip and others like it handle zero-bit insertion and deletion, the frame-check sequence (FCS), and the flags that define the beginning and end of a data frame.

The μ PAC trades some of this protocol flexibility for the sake of greatly enhanced usefulness within its area of application (Fig. 1). It is restricted to the Level 2 packet-switching protocol defined in Recommendation X.25 from the Consultative Committee for International Telephony and Telegraphy (CCITT), a protocol developed from HDLC. But other BOP chips do not set up, disconnect, or reset the link; they do not automatically retransmit up to seven information frames (I frames); nor do they have a timer for retransmission control. These are



1. Targeted. The Micro Packet Interface (μ PAC) chip is the first large-scale integrated circuit designed specifically for packet-switching applications. The application range of other chips that handle bit-oriented frame structure is wider, but the μ PAC does much more in its area.

TABLE 1: COMPARISON OF FEATURES OF BIT-ORIENTED-PROTOCOL CHIPS

HDLC/ADCCP protocol feature	X.25 Level 2	Bit-oriented-protocol chips	μ PAC
Basic bit-oriented frame structure	yes	yes	yes
Retransmission of up to 7 I frames (modulo 8)	yes	no	yes
Asynchronous response mode	yes, LAP	no	yes, 2501
Asynchronous balanced mode	yes, LAPB	no	yes, 2511
Control of S, U frames	yes	no	yes
Link set-up, disconnect, and reset procedures	yes	no	yes
Time-out recovery	yes, T1/N2	no	yes, T1/N2
Multipoint operation	no	no	yes
Normal response mode (NRM)	no	no	no
Level 2 modulo 128	FS	no	no

FS = item for further study by the CCITT

all features of the μ PAC chip (see Table 1).

Two versions of the μ PAC will be made available. One, the WD 2501, uses the Link-Access Procedure (LAP) defined in the first version of X.25. The WD 2511 is for networks using the Link-Access Procedure, Balanced (LAPB) added to X.25 subsequently. The two chips differ only in the program stored in ROM. They are pin-compatible and interchangeable without hardware or software modifications. Both may be used either in a terminal (DTE, data-terminal equipment) or in a network node (DCE, data-circuit-terminating equipment).

Direct memory access

Because of the HDLC feature that allows up to seven packets (I frames) to be outstanding (transmitted but unacknowledged) at any time, the μ PAC has information-field data (the I field of an information frame) buffered for up to eight packets both when transmitting and when receiving. In other words, the μ PAC may have to retransmit up to seven packets. It must therefore be able to retrace its steps through as many as seven of its eight buffers.

DMA circuitry, included in the μ PAC, is the best way to achieve this. A number of other control chips (floppy-disk controllers and data-link controllers) are DMA-compatible, but they do not actually include DMA. General-purpose microprocessors that have their own DMA, such as the Intel 8089, are not in the same category as the μ PAC.

DMA control on the μ PAC is simple, requiring only three pins (\overline{DRQ} , \overline{DROR} , and \overline{DACK}) for handshaking with the central processing unit's bus (Fig. 2.). There are 16 address-output pins (A0 through A15) that are separate from the eight data pins (DAL0 through DAL7). This means that the DMA transfers are fast—they occur in a single cycle. Unlike the μ PAC, DMA chips such as Western Digital's 1883 or Intel's 8257 require external address latches. This means that some or all of the address must come through the data bus and two or three cycles are required for data transfer.

In general, DMA control is either of the block-transfer type or the transparent type. In block-transfer DMA control, the DMA controller transfers several bytes of

data while the CPU is disabled from using the bus. If transparent, the DMA control is imbedded in the CPU's clock cycle in such a way that the transfers are invisible, or transparent, to the CPU. Since the μ PAC must be able to transmit and receive data on two DMA channels at once (for full-duplex operation), the only logical choice for the μ PAC is transparent DMA, since block-transfer DMA would restrict operation to half-duplex.

All Level 2 data is appended and checked automatically by the μ PAC. The I-field data is accessed via DMA channel. All supervisory frames (S frames) and unnumbered frames (U frames) are automatically transmitted and checked by the μ PAC. The user's CPU operates only on the I field of I frames.

Keeping track of packets

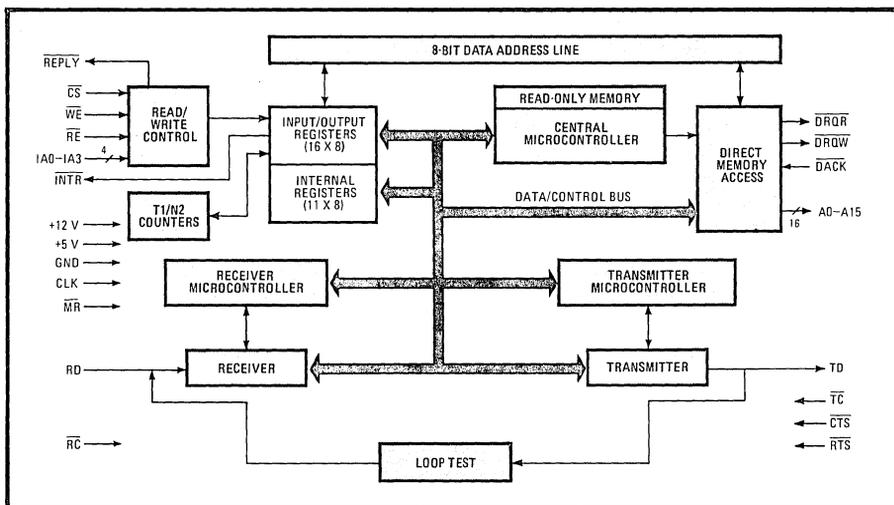
The DMA uses two lookup tables—one for transmitted frames (TLOOK) and another for received frames (RLOOK). These contain addresses and control bytes for the individual packets. Thus packet data is addressed indirectly. This method is best suited for most software applications.

The 16-bit starting address for TLOOK is loaded into the μ PAC by the CPU. RLOOK must follow immediately, and both TLOOK and RLOOK are stored in random-access memory external to the μ PAC.

There are a total of eight segmented control sections for each table. Each section contains 8 bytes, 4 of which are used for memory starting address and length. The rest are for control.

In the transmit mode, the μ PAC reads (from TLOOK) the starting address and length of the first packet to be transmitted. The chip then automatically transmits the flag, address, and control fields. Next, the information-field data is transmitted using DMA and the memory location called "send #0 packet." At the end of the information field, the μ PAC automatically sends the FCS and closing flag. It then moves on to the next packet.

If retransmission of one or more (up to seven) packets becomes necessary, the chip automatically retraces the previous transmissions through the TLOOK table. The user's CPU software does not become involved in the retransmission. An error counter is incremented.



2. Inside the μ PAC. The Level 2 controller has its own timer and direct-memory-access circuitry and is the logical equivalent of three microprocessors. Routines stored on the chip allow it to relieve the network user's central processor of a large software overhead burden.

Each received frame is checked for correct address and FCS fields and for type of control field. If the frame is an I frame, the I field is placed in the assigned memory location using a method similar to that used in transmission. After the packet is received error-free and in proper sequence, an interrupt is generated and the μ PAC is ready for the next packet, which will be placed in the next location.

Ten 8-bit error counters follow RLOOK in the external RAM. These counters do not cause an error interrupt, but maintain a running count of error activity. The contents of the counters include: the number of frames received with FCS error; the number of times T1 (the time minimum set for a timer that allows retransmission of an unacknowledged packet) ran out; and the number of packet retransmissions.

Control bits are included in TLOOK, RLOOK, and the μ PAC to ensure orderly transfer of data blocks. For example, the control bits are designed to prevent what is known as "deadly embrace," a situation in which the μ PAC and the user's computer are waiting for one another to start.

Self-testing

Self-testing features are critical to proper operation. The μ PAC does a comparison test, an internal RAM register test, and a loop-back test. All three are suitable for use during manufacturing and inspection. The internal RAM and loop-back tests are also useful for system diagnostics and troubleshooting.

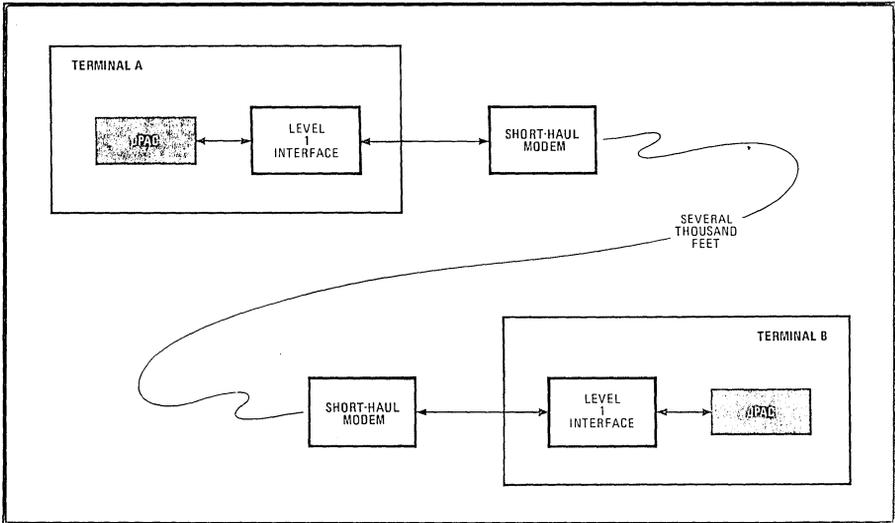
The comparison test requires a device known to be good or a stored list of known good responses. The program location counter (PLC) for the main ROM is halted so it may be incremented under external control.

TABLE 2: MICRO PACKET INTERFACE CHIP (μ PAC) TERMINOLOGY	
ABM	asynchronous balanced mode
ARM	asynchronous response mode
CMDR	command reject (U frame, LAP only)
DISC	disconnect (U frame)
DM	disconnect mode (U frame, LAPB only)
FRMR	frame reject (U frame, LAPB only)
REJ	reject (S frame)
RNR	receiver not ready (S frame)
RR	receiver ready (S frame)
SABM	set asynchronous balanced mode (LAPB only)
SARM	set asynchronous response mode (LAP only)
UA	unnumbered acknowledgement (U frame)

All jumps stored in ROM are disabled so that each location of the PLC may be counted. As the PLC is incremented, the responses of the output pins and status registers are compared to the known good responses.

There are 11 8-bit registers in the μ PAC that are not directly accessible by the user's CPU, which complicates testing somewhat. The internal RAM register test provides a means of checking these registers. The contents of register A are placed in six even internal registers and the contents of register B in five odd internal registers. The 11 registers are then added together without carry and the result is placed in status registers. This test is initiated by a control bit in the μ PAC. The loop-back test is discussed later.

For the purposes of discussing link establishment procedures, it will be assumed that there is a 2501 μ PAC at each end of the link. In practice, the 2501 can



3. Off the network. The μ PAC is also useful in non-network applications that use bit-oriented protocols. It provides full-duplex capability, does error detection and recovery, and gives systems the option of hooking directly to a packet-switching network at some future date.

communicate with any device meeting X.25 Level 2 specifications.

When a link is set up, it is said to be in the information-transfer phase. This means that the terminal and node will accept and transmit I and S frames. When a link is logically disconnected, only U frames—DISC, SARM, or UA (disconnect, set asynchronous response mode, and unnumbered acknowledge; see Table 2)—will be accepted or transmitted.

Link supervision

A link-connect frame is not the same as a link-reset frame. A link in the information-transfer phase may be reset in one direction by a SARM transmission. A link is up after both ends send a SARM command and receive a UA response.

Since a SARM can be either a command to reset or set up a link, misinterpretation by the receiver of a SARM is possible. This could happen when a link is established if one end momentarily loses power. When that end tries to bring the link up by sending a SARM, the other end may interpret the command as a link-reset.

There are two ways to get around this problem. Suppose a terminal or node attempting to bring a link up sends a SARM command and receives a UA. After time T1, if the station does not receive SARM, it assumes that the other end considered the link up. It will then disconnect the link by sending DISC and receiving a UA, and attempt to set up a link a second time.

The other way around the problem is the method used by the 2501. The 2501 will always send DISC and receive a UA before attempting to bring the link up. This will assure a logically disconnected link so that it may

attempt to set one up. Immediately after the link is up, the 2501 generates an interrupt.

It is possible to recover a single error on a packet with μ PAC control. The error makes the received FCS bad, so B does not recognize A's first transmission of frame 1. When B receives frame 2, something is wrong since the last successfully received packet was frame 0. Thus, at the next opportunity, B sends a REJ (reject—an S frame) asking A to retransmit frame 1. This opportunity comes after B completes sending its frame 2.

When A receives the REJ frame, it is sending frame 3. There is no need to continue with frame 3, so A aborts transmission of frame 3 and goes back and retransmits frame 1. After retransmitting frame 1, A will retransmit frames 2 and 3. Finally, A will continue transmitting other frames.

Loop-back

A loop-back condition exists when a station receives the same serial information it has transmitted. In the loop-back test, the serial-transmit output is connected to the serial-receive input in order to test the transmitter and receiver channels. Each station has both primary and secondary functions, so there are two logical primary-to-secondary associations on a terminal-to-node link, and each association is identified by a different address field. This makes loop-back testing impossible when a strict X.25 connection is made. Commands will have the A field of a response and vice versa. One way around this is to make the A fields of the two associations equal for the duration of the loop-back test. (The A fields are programmable in the μ PAC.)

Another problem with loop-back testing is the actual

detection of the condition and the detection of the condition's removal. There is no simple way around this problem, and the μ PAC gives only limited assistance.

First, detecting the existence of a loop-back condition is the responsibility of the CPU driving the μ PAC. If the CPU sees that a link cannot be brought up, or if a link is up and suddenly has excessive link resets and CMDRs (command reject, a U frame), the CPU could assume the presence of a loop-back condition. After making the two A fields the same, if a disconnected link is successfully brought up, then the loop-back condition exists.

To detect the removal of this condition, a particular control bit (RRT1) in the μ PAC may be used. It causes the μ PAC to send an RR (receiver ready, an S frame) or an RNR (receiver not ready, also an S frame). These frames are sent at T1 intervals as long as the μ PAC is not commanded to send a packet. As long as the μ PAC receives those S frames, the loop-back condition exists. However, if the μ PAC fails to receive an S frame for a time equal to $T1 \times N2$, an interrupt is generated, signaling that the loop-back condition has been removed.

Modified X.25

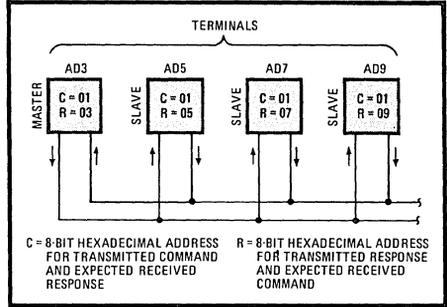
The original design intention was to use the μ PAC in a strict X.25 terminal-to-node application, the only application covered by X.25. However, by taking advantage of the terminal-node symmetry of the μ PAC (the fact that it can be used in both DTE and DCE), other applications are possible that use its built-in features.

For instance, the user does not need to develop the software for error recovery since this is a μ PAC feature. For another, using a μ PAC makes it possible to connect a non-packet terminal to an X.25 link at a future time. And lastly, the chip's protocol is bit-oriented. It has a number of advantages over older, character-oriented protocols, such as code transparency, full-duplex capability, flexibility, and modularity [*Electronics*, Jan. 18, 1979, p. 137].

One possible application is the connection of two terminals at Levels 1 and 2 (Fig. 3). How much of Level 3 is used would depend upon the individual application; the more of Level 3 used, the better standardized the interface is. One of the terminals in Fig. 3 could be a terminal concentrator (a Packet Assembly/Disassembly facility, or PAD, as defined by Recommendations X.3, X.28, and X.29) on a factory floor, and the other could be a host computer in a data-processing center.

Modified X.25 could also be used in a multipoint system (Fig. 4). Idle terminals in this type of system must transmit an "idle" sequence, not continuous flags. The terminal addresses (AD3, AD5, AD7, and so on) correspond to the transmitted response A field. The transmitted command A field is the same for all terminals and is chosen to be hexadecimal 01 in this case. All A fields are selected with odd values (least-significant bit transmitted first) to conform to the extended-address format of the Advanced Data-Communication Control Procedures (ADCCP).

Two terminals on the multipoint line may establish and discontinue communications by exercising X.25 procedures for setting up and disconnecting a link. But only two terminals can communicate at any one time.



4. **Multipoint line.** The programmed features of the μ PAC chip enhance the flexibility of a system comprising one master terminal and up to 128 slave terminals. Hardware and software savings are possible when the μ PAC is used in this off-network context.

Suppose that AD3 wishes to communicate with AD7. AD3 will first make sure that its receiving line is idle (a status bit in the μ PAC). Next, AD3 will change its transmitted command and response A fields to be the reverse of AD7 (command field is set to 07, response field is set to 01). Then AD3 will initiate link establishment by setting a control bit, called "active," in the μ PAC. Once the link has been established (the μ PAC generates an interrupt when the link is first set up), AD3 and AD7 may exchange I frames. To discontinue the session, either AD3 or AD7 will set the mandatory-disconnect control bit in its μ PAC. This will cause that terminal to initiate a logical-disconnect procedure.

Contention and roll-call methods

The multipoint system may be implemented by either contention or roll-call polling. In the roll-call method, the master terminal will initiate link establishment with one of the slave terminals, communicate with that slave, discontinue the session (disconnecting the link), and go on to the next slave. This process continues until all slaves are polled and then starts over. One advantage of the roll-call method is that the master has tight control over the line for efficient operation.

A disadvantage is that slaves must be queried (polled) before sending data, and the more slaves on the line, the longer it takes for the master to poll them. Therefore it is essential that each slave be designed to exchange a relatively small amount of data with the master in a single session, lest it tie up the line for long periods. Large amounts of data should be broken up and exchanged in more than one session. This method is suited to applications where the multipoint line has a high usage.

In the contention method, any terminal may initiate a session at any time. This is similar to a party telephone line and is suited to applications where line usage is low. All sessions are between the master and one of the slaves, but unlike the roll-call method, a slave may initiate the session. The terminal that initiates a session must send an I frame with its unique address immediately after the link is set up. □

Board Product Numbering System

TELECOMMUNICATIONS BOARD LEVEL PRODUCT NUMBERING

GENERAL DESCRIPTION: WD A XXXXX — A A A
1 2 3 4 5 6

1. WD — WESTERN DIGITAL.
2. A — A letter to be designated. This field may be missing. Values assigned to date: K — KIT.
3. XXXXX — An expanded version of the number of the featured WESTERN DIGITAL LSI device on the board.
4. A — A letter designating BUS OPTION. This field will never be blank. Values assigned to date:
 - A — UNIBUS™
 - B — Q BUS™
 - D — MULTIBUS™
 - E — "STANDARD" BUS
 - X — No BUS interface
5. A — A letter designating I/O Channel interface. This field will never be blank. Values assigned to date:
 - A — RS 232
 - B — RS 422
 - C — RS 423
 - D — RS 449
 - E — Fiber Optic
 - X — No I/O channel
6. A — A letter, function to be designated later.

- EXAMPLES: WDK 2001-XA — WESTERN DIGITAL Cryptographic Kit using the WD2001. The board has an RS 232 I/O Channel interface.
- WD 25001-AC — WESTERN DIGITAL Packet Switching board using the WD 2501. The board has a UNIBUS™ computer interface and an RS-423 I/O Channel interface.

Introduction to

COMPUTER PRODUCTS DIVISION

The Computer Products Division of Western Digital is an established leader in File Management Devices. We are currently the leading supplier of floppy disk and Winchester disk controller products. We provide our customers with a standard line of MOS/LSI controller devices, support circuits, custom devices and board level products.

Winchester Products

Western Digital recently announced and began shipping the WD1000 fixed disk controller and WD1100 chip set. These products dramatically reduce the cost and circuit board area required to interface with the popular Winchester technology devices.

Floppy Disk Products

The Computer Products Division is the world's leading supplier of MOS/LSI floppy disk devices. Our 1700 Series Controllers support single and double density, IBM compatible and non-standard 5¼ inch and 8 inch drives.

Specialty Products

The Computer Products Division supplies specialty devices and board level products which support data management activities. These include standard, semi-custom, and custom products, and a family of semi-custom logic arrays.

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COMPUTER PRODUCTS DIVISION

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**ADVANCE
INFORMATION**

WESTERN DIGITAL

C O R P O R A T I O N

WD1000 WINCHESTER CONTROLLER

FEATURES

- ST500/SA1000 INTERFACE
- 256 BYTE BUFFER
- AUTOMATIC CRC CHECKING/VERIFICATION
- 5 MBITS/SEC TRANSFER RATE
- DMA OR PROGRAMMED I/O TRANSFERS
- CONTROL UP TO 4 DRIVES
- CONTROL UP TO 8 R/W HEADS
- GENERAL PURPOSE 8 BIT INTERFACE
- SINGLE 5-VOLT SUPPLY
- MULTIPLE SECTOR READ AND WRITE COMMANDS
- FORMATTING AND SECTOR INTERLEAVE CAPABILITY
- BUILT IN DATA SEPARATOR/WRITE PRECOMPENSATION LOGIC
- SIX POWERFUL MACRO-COMMANDS
- "BAD BLOCK" MARK AND DETECTION

SPECIFICATIONS

INSTRUCTION SET

RESTORE
READ SECTOR
WRITE SECTOR
AUTO FORMAT
SEEK

POWER SUPPLY

+5 VDC

CONTROLLER/INTERFACE

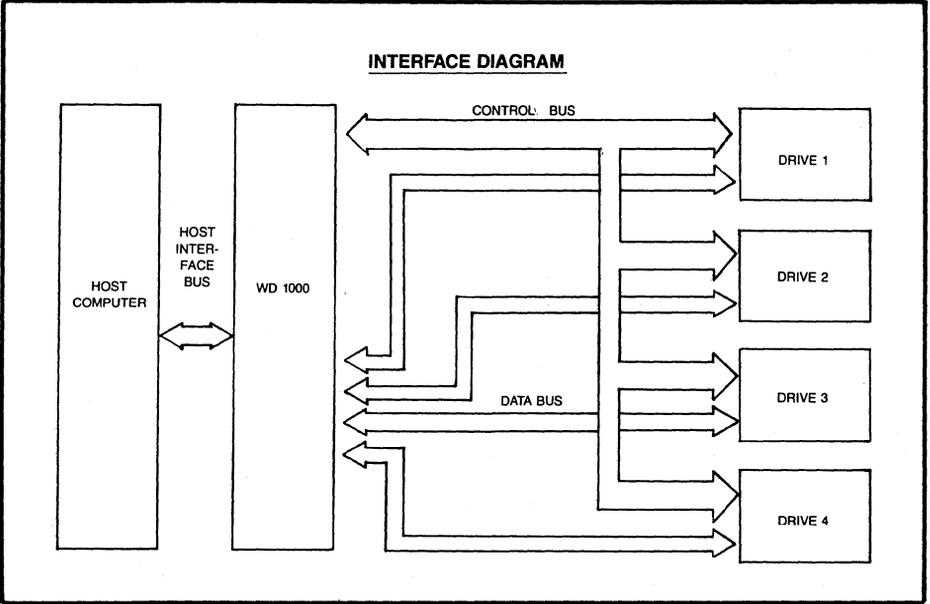
8 DATA LINES
3 ADDRESS LINES
MASTER RESET
DATA REQUEST
INTERRUPT REQUEST
READ ENABLE
WRITE ENABLE

GENERAL DESCRIPTION

The WD1000 WINCHESTER CONTROLLER BOARD provides the user with a low-cost alternative for interfacing any ST500 compatible Winchester disk drive to a host computer. The processor interface consists of an 8-bit bi-directional bus for data, status and control word transfers. The controller board includes data separation and write precompensation circuitry. Data being written to or read from the drive is stored in an on-board buffer memory, simplifying the DMA or programmed I/O interface. The controller will read or write MFM data at rates up to 5M bits per second.

Reading and writing of sectors, along with motor control is accomplished via a powerful set of macro-commands. Programming the WD1000 controller board is similar to programming the Western Digital FD179X floppy disk controller.

The WD1000 is based upon a proprietary Chip Set specifically designed for Winchester control. The WD1000 Chip Set is also available for OEM design.



Host Interface Signals

- Data Access 0
- Data Access 1
- Data Access 2
- Data Access 3
- Data Access 4
- Data Access 5
- Data Access 6
- Data Access 7
- Write Enable
- Read Enable
- Address 0
- Address 1
- Address 2
- Interrupt Request
- Data Request
- Chip Select
- Write Clock
- Timing Clock

Control Signals

- Reduce Write Current
- Write Gate
- Seek Complete
- Track 000
- Write Fault
- Head Select 0
- Head Select 1
- Head Select 2
- Index
- Ready
- Step
- Direction
- Drive Select 0
- Drive Select 1
- Drive Select 2
- Drive Select 3

Data Signals

- + Write Data
- Write Data
- + Read Data
- Read Data
- + Timing Clock
- Timing Clock

WD1100 WINCHESTER CONTROLLER CHIP SET

DESCRIPTION

The WD1100 Chip Set provides a low cost alternative for developing a Winchester Controller. These five devices have been designed to read and convert an MFM data stream into 8-bit parallel bytes. During a write operation, parallel data is converted back into MFM to be written on the disk. Address Marks are generated and detected while CRC bytes can be appended on the data stream. The WD1100 is fabricated in N-channel silicon gate and technology and is available in a 20 pin Dual-In-Line package.

- WD1100-01 Ser/Parallel Converter
- WD1100-02 MFM Generator
- WD1100-03 AM Detector
- WD1100-04 CRC Generator/Checker
- WD1100-05 Par/Serial Converter

FEATURES

- SA1000/ST506 COMPATIBLE
- SINGLE 5V SUPPLY
- TRI-STATE DATA LINES
- 5 MBITS/SEC TRANSFER RATE

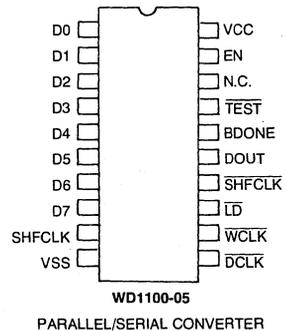
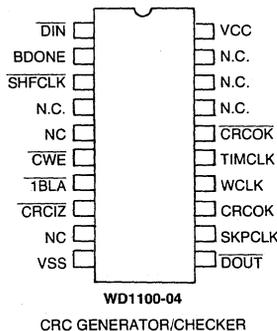
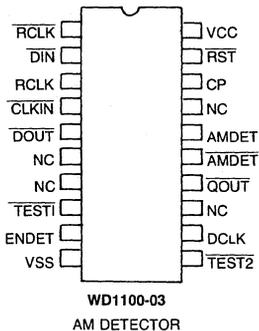
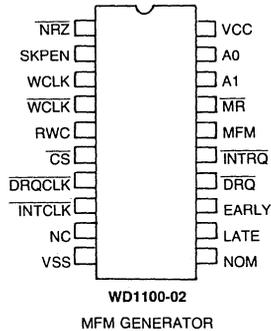
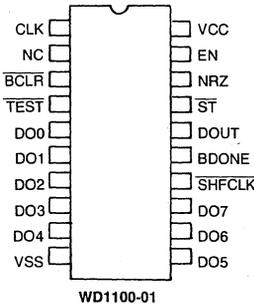
APPLICATIONS

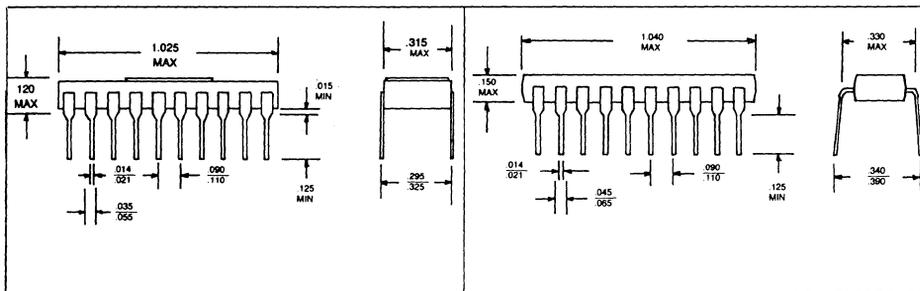
Winchester Controllers For:

- Shugart Associates—SA1004
- Seagate Technology—ST506
- Quantum Corp.—Q2000

MARCH, 1981

ZC-10m6
2





1100U CERAMIC PACKAGE

1100V PLASTIC PACKAGE

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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WESTERN DIGITAL

C O R P O R A T I O N

FD 179X-02 Floppy Disk Formatter/Controller Family

FEATURES

- TWO VFO CONTROL SIGNALS
- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
IBM 3740 Single Density (FM)
IBM System 34 Double Density (MFM)
- READ MODE
Single/Multiple Sector Read with Automatic Search or Entire Track Read
Selectable 128 Byte or Variable length Sector
- WRITE MODE
Single/Multiple Sector Write with Automatic Sector Search
Entire Track Write for Diskette Formatting
- SYSTEM COMPATIBILITY
Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
DMA or Programmed Data Transfers
All Inputs and Outputs are TTL Compatible
On-Chip Track and Sector Registers/Comprehensive Status Information

- PROGRAMMABLE CONTROLS
Selectable Track to Track Stepping Time
Side Select Compare
- WRITE PRECOMPENSATION
- WINDOW EXTENSION
- INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY
- FD1792/4 IS SINGLE DENSITY ONLY
- FD1795/7 HAS A SIDE SELECT OUTPUT

MAY 1980

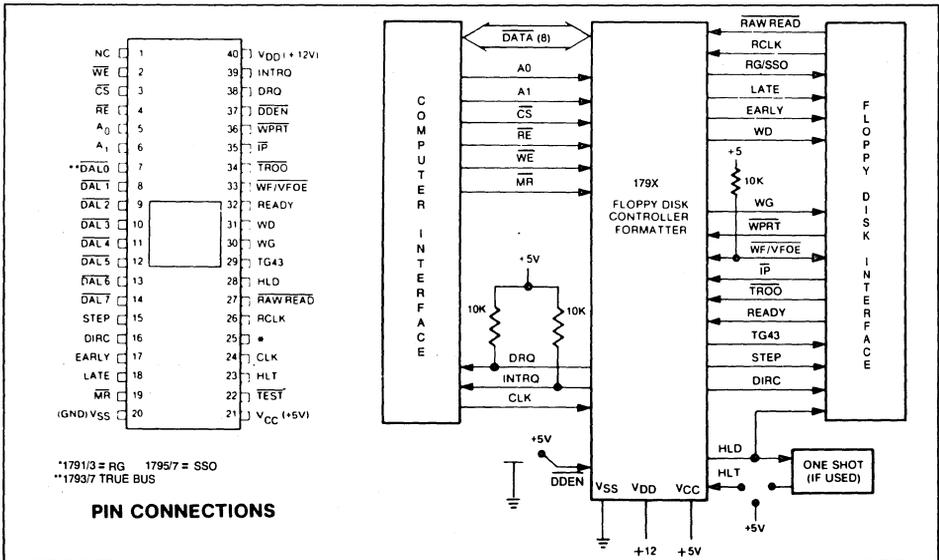
SECTION 2

179X-02 FAMILY CHARACTERISTICS

FEATURES	1791	1793	1795	1797
Single Density (FM)	X	X	X	X
Double Density (MFM)	X	X	X	X
True Data Bus		X		X
Inverted Data Bus	X		X	
Write Precomp	X	X	X	X
Side Selection Output			X	X

APPLICATIONS

FLOPPY DISK DRIVE INTERFACE
SINGLE OR MULTIPLE DRIVE CONTROLLER/
FORMATTER
NEW MINI-FLOPPY CONTROLLER



FD179X SYSTEM BLOCK DIAGRAM

GENERAL DESCRIPTION

The FD179X are MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The FD179X, which can be considered the end result of both the FD1771 and FD1781 designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The FD179X contains all the features of its predecessor the FD1771, plus the added features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation. In order to maintain compatibility, the FD1771, FD1781, and FD179X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load

control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The FD179X is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD179X is fabricated in N-channel Silicon Gate MOS technology and is TTL compatible on all inputs and outputs. The 1793 is identical to the 1791 except the DAL lines are TRUE for systems that utilize true data busses.

The 1795/7 has a side select output for controlling double sided drives, and the 1792 and 1794 are "Single Density Only" versions of the 1791 and 1793. On these devices, DDEN must be left open.

PIN OUTS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION																				
1	NO CONNECTION	NC	Pin 1 is internally connected to a back bias generator and must be left open by the user.																				
19	MASTER RESET	\overline{MR}	A logic low on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during \overline{MR} ACTIVE. When \overline{MR} is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.																				
20	POWER SUPPLIES	V_{SS}	Ground																				
21		V_{CC}	+5V \pm 5%																				
40		V_{DD}	+12V \pm 5%																				
COMPUTER INTERFACE:																							
2	WRITE ENABLE	\overline{WE}	A logic low on this input gates data on the DAL into the selected register when \overline{CS} is low.																				
3	CHIP SELECT	\overline{CS}	A logic low on this input selects the chip and enables computer communication with the device.																				
4	READ ENABLE	\overline{RE}	A logic low on this input controls the placement of data from a selected register on the DAL when \overline{CS} is low.																				
5,6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive/transfer data on the DAL lines under \overline{RE} and \overline{WE} control: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>A1</th> <th>A0</th> <th>\overline{RE}</th> <th>\overline{WE}</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Status Reg</td> <td>Command Reg</td> </tr> <tr> <td>0</td> <td>1</td> <td>Track Reg</td> <td>Track Reg</td> </tr> <tr> <td>1</td> <td>0</td> <td>Sector Reg</td> <td>Sector Reg</td> </tr> <tr> <td>1</td> <td>1</td> <td>Data Reg</td> <td>Data Reg</td> </tr> </tbody> </table>	A1	A0	\overline{RE}	\overline{WE}	0	0	Status Reg	Command Reg	0	1	Track Reg	Track Reg	1	0	Sector Reg	Sector Reg	1	1	Data Reg	Data Reg
A1	A0	\overline{RE}	\overline{WE}																				
0	0	Status Reg	Command Reg																				
0	1	Track Reg	Track Reg																				
1	0	Sector Reg	Sector Reg																				
1	1	Data Reg	Data Reg																				
7-14	DATA ACCESS LINES	DAL0-DAL7	Eight bit inverted Bidirectional bus used for transfer of data, control, and status. This bus is receiver enabled by \overline{WE} or transmitter enabled by \overline{RE} .																				
24	CLOCK	CLK	This input requires a free-running square wave clock for internal timing reference, 2 MHz for 8" drives, 1 MHz for mini-drives.																				

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion of any command and is reset when the STATUS register is read or the command register is written to. Use 10K pull-up resistor to +5.
FLOPPY DISK INTERFACE:			
15	STEP	STEP	The step output contains a pulse for each step.
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.
17	EARLY	EARLY	Indicates that the WRITE DATA pulse occurring while Early is active (high) should be shifted early for write precompensation.
18	LATE	LATE	Indicates that the write data pulse occurring while Late is active (high) should be shifted late for write precompensation.
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	This input is used for testing purposes only and should be tied to +5V or left open by the user unless interfacing to voice coil actuated motors.
23	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged.
25	READ GATE (1791/3)	RG	A high level on this output indicates to the data separator circuitry that a field of zeros (or ones) has been encountered, and is used for synchronization.
25	SIDE SELECT OUTPUT (1795, 1797)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When S = 1, SSO is set to a logic 1. When S = 0, SSO is set to a logic 0. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.
26	READ CLOCK	RCLK	A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not.
27	$\overline{\text{RAW READ}}$	$\overline{\text{RAW READ}}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
31	WRITE DATA	WD	A 250 ns (MFM) or 500 ns (FM) pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	<u>WRITE FAULT</u> VFO ENABLE	<u>WF/VFOE</u>	This is a bi-directional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When $WG = 1$, Pin 33 functions as a WF input. If $WF = 0$, any write command will immediately be terminated. When $WG = 0$, Pin 33 functions as a VFOE output. VFOE will go low during a read operation after the head has loaded and settled ($HLT = 1$). On the 1795/7, it will remain low until the last bit of the second CRC byte in the ID field. VFOE will then go high until 8 bytes (MFM) or 4 bytes (FM) before the Address Mark. It will then go active until the last bit of the second CRC byte of the Data Field. On the 1791/3, VFOE will remain low until the end of the Data Field.
34	<u>TRACK 00</u>	<u>TR00</u>	This input informs the FD179X that the Read/Write head is positioned over Track 00.
35	<u>INDEX PULSE</u>	<u>IP</u>	This input informs the FD179X when the index hole is encountered on the diskette.
36	<u>WRITE PROTECT</u>	<u>WPRT</u>	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	<u>DOUBLE DENSITY</u>	<u>DDEN</u>	This pin selects either single or double density operation. When $DDEN = 0$, double density is selected. When $DDEN = 1$, single density is selected. This line must be left open on the 1792/4

ORGANIZATION

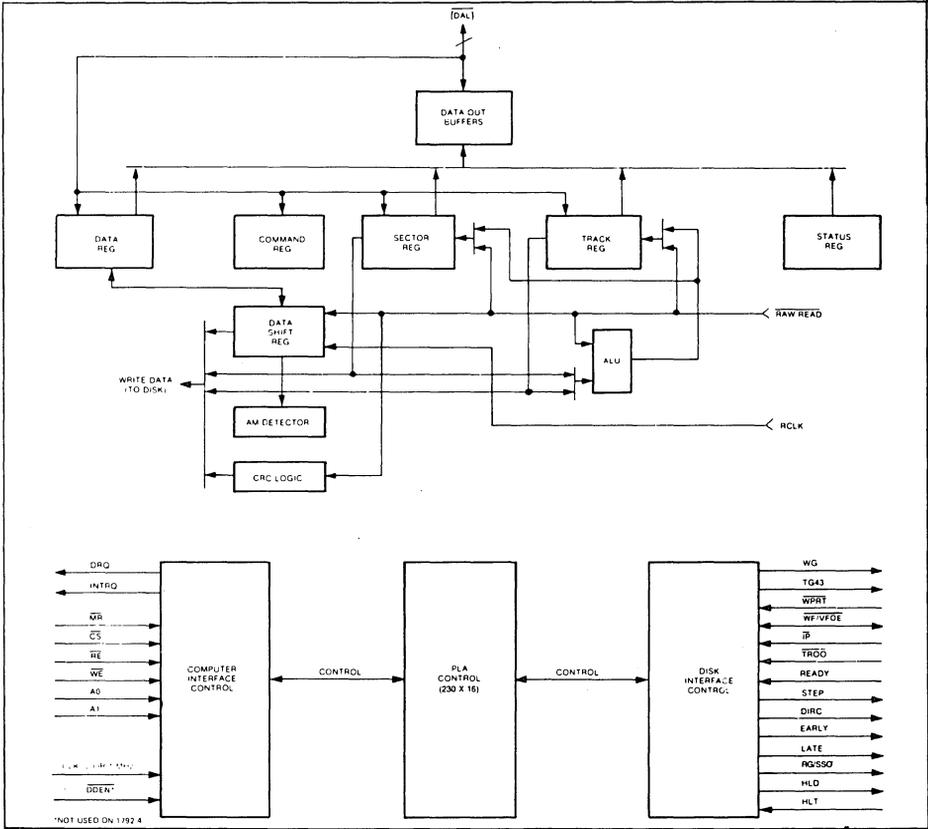
The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register—This 8-bit register assembles serial data from the Read Data input (RAW READ) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register—This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register—This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.



FD179X BLOCK DIAGRAM

Sector Register (SR)—This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR)—This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR)—This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic—This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU)—The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control—All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

The FD1791/3 has two different modes of operation according to the state of DDEN. When DDEN = 0 double density (MF) is assumed. When DDEN = 1, single density (FM) is assumed.

AM Detector—The address mark detector detects ID, data and index address marks during read and write operations.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the FD179X. The DAL are three state buffers that are enabled as output drivers when Chip Select (CS) and Read Enable (\overline{RE}) are active (low logic state) or act as input receivers when \overline{CS} and Write Enable (\overline{WE}) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and \overline{CS} is made low. The address bits A1 and A0, combined with the signals \overline{RE} during a Read operation or \overline{WE} during a Write operation are interpreted as selecting the following registers:

A1-A0	READ (\overline{RE})	WRITE (\overline{WE})
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD179X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

FLOPPY DISK INTERFACE

The 179X has two modes of operation according to the state of \overline{DDEN} (Pin 37). When $\overline{DDEN} = 1$, single density is selected. In either case, the CLK input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density. When the clock is at 2 MHz, the stepping rates of 3, 6, 10, and 15 ms are obtainable. When CLK equals 1 MHz these times are doubled.

HEAD POSITIONING

Five commands cause positioning of the Read-Write head (see Command Section). The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. If $\overline{TEST} = 0$, there is zero settling time. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

The rates (shown in Table 1) can be applied to a Step-Direction Motor through the device interface.

Step—A 2 μ s (MFM) or 4 μ s (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output.

Direction (DIRC)—The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12 μ s before the first stepping pulse is generated.

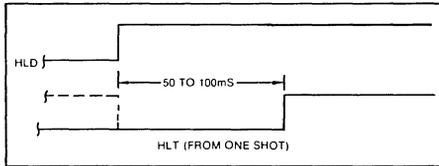
When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 ($V = 1$) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. The FD179X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated.

Table 1. STEPPING RATES

CLK	2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
\overline{DDEN}	0	1	0	1	x	x
R1 R0	$\overline{TEST}=1$	$\overline{TEST}=1$	$\overline{TEST}=1$	$\overline{TEST}=1$	$\overline{TEST}=0$	$\overline{TEST}=0$
0 0	3 ms	3 ms	6 ms	6 ms	184 μ s	368 μ s
0 1	6 ms	6 ms	12 ms	12 ms	190 μ s	380 μ s
1 0	10 ms	10 ms	20 ms	20 ms	198 μ s	396 μ s
1 1	15 ms	15 ms	30 ms	30 ms	208 μ s	416 μ s

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set ($h = 1$), at the end of the Type I command if the verify flag ($V = 1$), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with ($h = 0$ and $V = 0$); or if the FD179X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load Timing (HLT) is an input to the FD179X which is used for the head engage time. When HLT = 1, the FD179X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the FD179X.



HEAD LOAD TIMING

When both HLD and HLT are true, the FD179X will then read from or write to the media. The "and" of HLD and HLT appears as a status bit in Type I status.

In summary for the Type I commands: if $h = 0$ and $V = 0$, HLD is reset. If $h = 1$ and $V = 0$, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If $h = 0$ and $V = 1$, HLD is set near the end of the command, an internal 15 ms occurs, and the FD179X waits for HLT to be true. If $h = 1$ and $V = 1$, HLT is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the FD179X then waits for HLT to occur.

For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, \overline{DDEN} should be placed to logical "1." For MFM formats, \overline{DDEN} should be placed to a logical "0." Sector lengths are determined at format time by a special byte in the "ID" field. If this Sector length byte in the ID field is zero, then the sector length is 128 bytes. If 01 then 256 bytes. If 02, then 512 bytes. If 03, then the sector length is 1024 bytes. The number of sectors per track as far as the FD179X is concerned can be from 1 to 255 sectors. The number of tracks as far as the FD179X is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with 8 sectors/track. (See Sector Length Table.)

For read operations, the FD179X requires \overline{RAW} READ Data (Pin 27) signal which is a 250 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not it may be

derived externally by Phase lock loops, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM, RG is made true when 2 bytes of zeroes are detected. The FD179X must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the FD179X is deriving any useful information from the data stream. Similarly for MFM, RG is made active when 4 bytes of "00" or "FF" are detected. The FD179X must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

During read operations ($WG = 0$), the \overline{VFOE} (Pin 33) is provided for phase lock loop synchronization. \overline{VFOE} will go active when:

- Both HLT and HLD are True
- Settling Time, if programmed, has expired
- The 179X is inspecting data off the disk

If $\overline{WF}/\overline{VFOE}$ is not used, leave open or tie to a 10K resistor to +5.

DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD179X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{Write Protect}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD179X terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The Write Fault input should be made inactive when the Write Gate output becomes inactive.

For write operations, the FD179X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM ($\overline{DDEN} = 1$) and 250 ns pulses in MFM ($\overline{DDEN} = 0$). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written early. LATE is active true when the WD pulse is to be written LATE. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the FD179X. The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.

Whenever a Read or Write command (Type II or III) is received the FD179X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated.

COMMAND DESCRIPTION

The FD179X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 2.

Table 2 COMMAND SUMMARY

TYPE COMMAND	BITS							
	7	6	5	4	3	2	1	0
I Restore	0	0	0	0	h	v	r ₁	r ₀
I Seek	0	0	0	1	h	v	r ₁	r ₀
I Step	0	0	1	u	h	v	r ₁	r ₀
I Step In	0	1	0	u	h	v	r ₁	r ₀
I Step Out	0	1	1	u	h	v	r ₁	r ₀
II Read Sector	1	0	0	m	F ₂	E	F ₁	0
II Write Sector	1	0	1	m	F ₂	E	F ₁	a ₀
III Read Address	1	1	0	0	0	0	0	0
III Read Track	1	1	1	0	0	0	0	0
III Write Track	1	1	1	1	0	0	0	0
IV Force Interrupt	1	1	0	1	l ₃	l ₂	l ₁	l ₀

Note: Bits shown in TRUE form.

Table 3 FLAG SUMMARY

TYPE I COMMANDS
<u>h = Head Load Flag (Bit 3)</u>
h = 1, Load head at beginning
h = 0, Unload head at beginning
<u>V = Verify flag (Bit 2)</u>
V = 1, Verify on destination track
V = 0, No verify
<u>r₁r₀ = Stepping motor rate (Bits 1-0)</u>
Refer to Table 1 for rate summary
<u>u = Update flag (Bit 4)</u>
u = 1, Update Track register
u = 0, No update

Table 4 FLAG SUMMARY

TYPE II & III COMMANDS
<u>m = Multiple Record flag (Bit 4)</u>
m = 0, Single Record
m = 1, Multiple Records
<u>a₀ = Data Address Mark (Bit 0)</u>
a ₀ = 0, FB (Data Mark)
a ₀ = 1, F8 (Deleted Data Mark)
<u>E = 15 ms Delay (2MHz)</u>
E = 1, 15 ms delay
E = 0, no 15 ms delay
(F ₂) <u>S = Side Select Flag (1791/3 only)</u>
S = 0, Compare for Side 0
S = 1, Compare for Side 1
(F ₁) <u>C = Side Compare Flag (1791/3 only)</u>
C = 0, disable side select compare
C = 1, enable side select compare
(F ₁) <u>S = Side Select Flag</u>
(Bit 1, 1795/7 only)
S = 0 Update SSO to 0
S = 1 Update SSO to 1
(F ₂) <u>b = Sector Length Flag</u>
(Bit 3, 1975/7 only)

Sector Length Field				
	00	01	10	11
b = 0	256	512	1024	128
b = 1	128	256	512	1024

Table 5 FLAG SUMMARY

TYPE IV COMMAND
<u>li = Interrupt Condition flags (Bits 3-0)</u>
l0 = 1, Not-Ready to Ready Transition
l1 = 1, Ready to Not-Ready Transition
l2 = 1, Index Pulse
l3 = 1, Immediate Interrupt
l ₃ -l ₀ = 0, Terminate with no Interrupt

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contains a rate field (r₀r₁), which determines the stepping motor rate as defined in Table 1.

The Type I Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If $h = 1$, the head is loaded at the beginning of the command (HLD output is made active). If $h = 0$, HLD is deactivated. Once the head is loaded, the head will remain engaged until the FD179X receives a command that specifically disengages the head. If the FD179X is idle (busy = 0) for 15 revolutions of the disk, the head will be automatically disengaged (HLD made inactive).

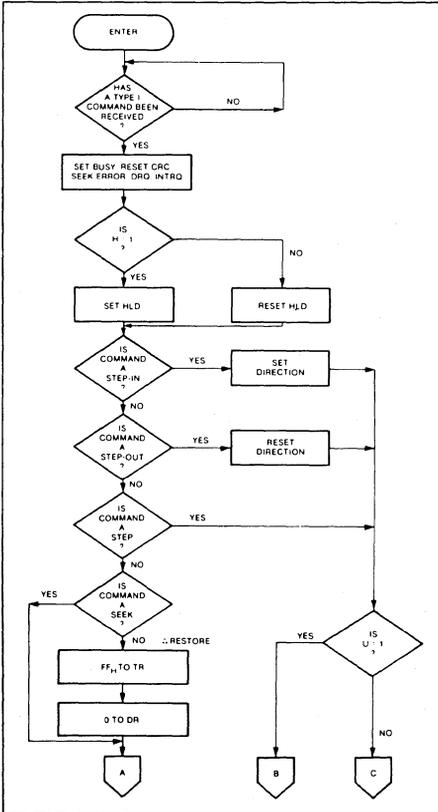
The Type I Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If $V = 1$, a verification is performed, if $V = 0$, no verification is performed.

During verification, the head is loaded and after an internal 15 ms delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field is read off the disk. The track address of the

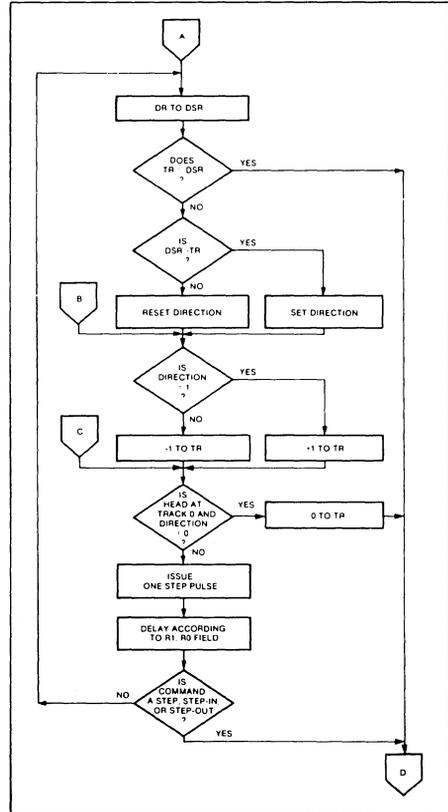
ID field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the Busy status bit is reset. If there is not a match but there is valid ID CRC, an interrupt is generated, and Seek Error Status bit (Status bit 4) is set and the Busy status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after four revolutions of the disk, the FD179X terminates the operation and sends an interrupt, (INTRQ).

The Step, Step-In, and Step-Out commands contain an Update flag (U). When $U = 1$, the track register is updated by one for each step. When $U = 0$, the track register is not updated.

On the 1795/7 devices, the SSO output is not affected during Type 1 commands, and an internal side compare does not take place when the (V) Verify Flag is on.



TYPE I COMMAND FLOW



TYPE I COMMAND FLOW

RESTORE (SEEK TRACK 0)

Upon receipt of this command the Track 00 ($\overline{\text{TROO}}$) input is sampled. If $\overline{\text{TROO}}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{\text{TROO}}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the r_{1r0} field are issued until the $\overline{\text{TROO}}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{\text{TROO}}$ input does not go active low after 255 stepping pulses, the FD179X terminates operation, interrupts, and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when MR goes from an active to an inactive state.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD179X will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP

Upon receipt of this command, the FD179X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_{1r0} field, a verification takes place if the V flag is on. If the u flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 76. If the u flag is on, the Track Register is incremented by one. After a delay determined by the r_{1r0} field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

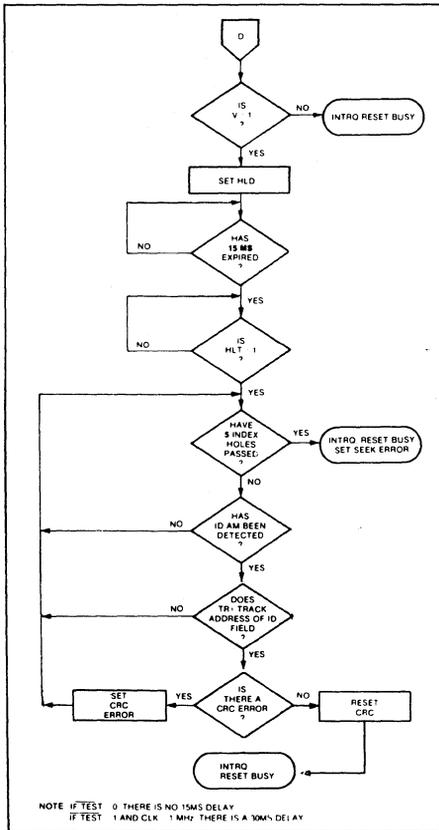
STEP-OUT

Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 0. If the u flag is on, the Track Register is decremented by one. After a delay determined by the r_{1r0} field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

TYPE II COMMANDS

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLT is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15 msec delay. The ID field and Data Field format are shown on page 13.

When an ID field is located on the disk, the FD179X compares the Track Number on the ID field with the Track Register. If there is not a match, the next en-



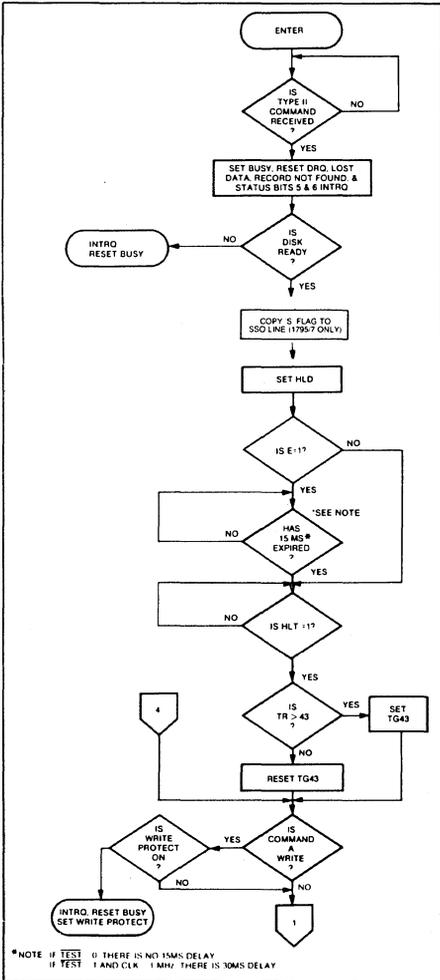
TYPE I COMMAND FLOW

countered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FD179X must find an ID field with a Track number, Sector number, side number, and CRC within four revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.

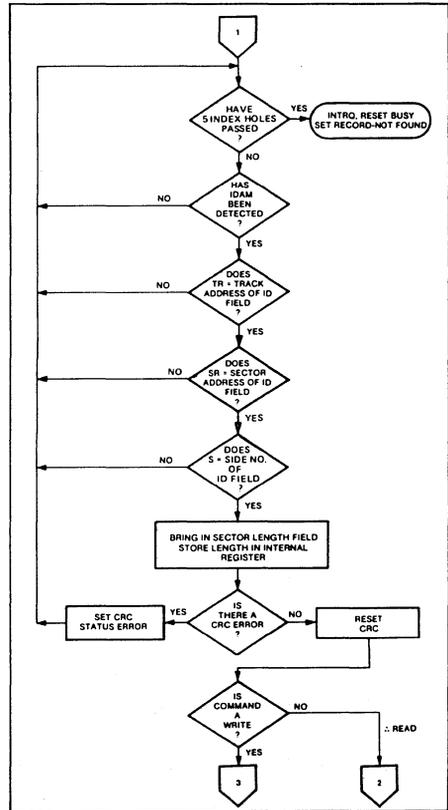
Sector Length Table	
Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If $m = 0$, a single sector is read or written and an interrupt is generated at the completion of the command. If $m = 1$, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FD179X will continue to read or write multiple records and update the sector register until the sector regis-

SECTION 2



TYPE II COMMAND



TYPE II COMMAND

ter exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

If the Sector Register exceeds the number of sectors on the track, the Record-Not-Found status bit will be set.

The Type II commands also contain side select compare flags. When C = 0, no side comparison is made. When C = 1, the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag. If the S flag compares with the side number recorded in the ID field, the 179X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

The 1795/7 READ SECTOR and WRITE SECTOR commands include a 'b' flag. The 'b' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatibility, the 'b' flag should be set to a one. The

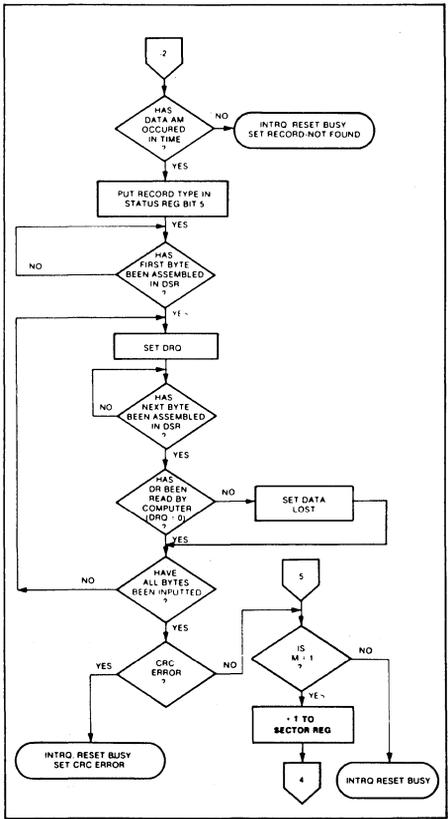
's' flag allows direct control over the SSO Line (Pin 25) and is set or reset at the beginning of the command, dependent upon the value of this flag.

READ SECTOR

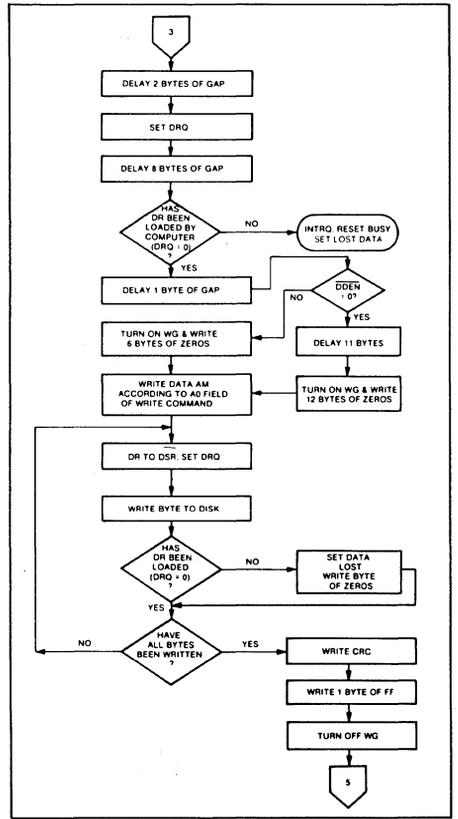
Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the Record Not Found status bit is set and the operation is terminated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and

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TYPE II COMMAND



TYPE II COMMAND

the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown below:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The FD179X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a_0 field of the command as shown below:

a_0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

The FD179X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated.

TYPE III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The

next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the FD179X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register. At the end of the operation an interrupt is generated and the Busy Status is reset.

READ TRACK

Upon receipt of the Read Track command, the head is loaded and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. The accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated. RG is not activated during the Read Track Command. An internal side compare is not performed during a Read Track.

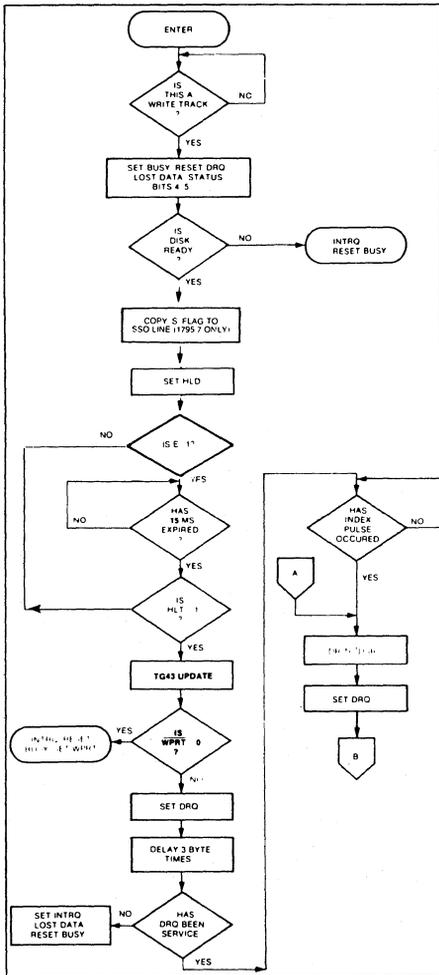
WRITE TRACK

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM.

GAP III	ID AM	TRACK NUMBER	SIDE NUMBER	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP II	DATA AM	DATA FIELD	CRC 1	CRC 2
ID FIELD										DATA FIELD		

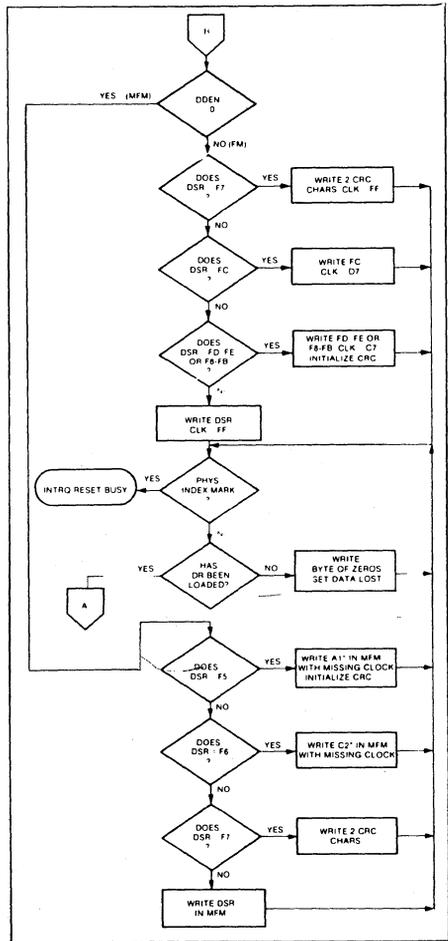
In MFM only, IDAM and DATA AM are preceded by three bytes of A1 with clock transition between bits 4 and 5 missing.

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TYPE III COMMAND WRITE TRACK

CONTROL BYTES FOR INITIALIZATION

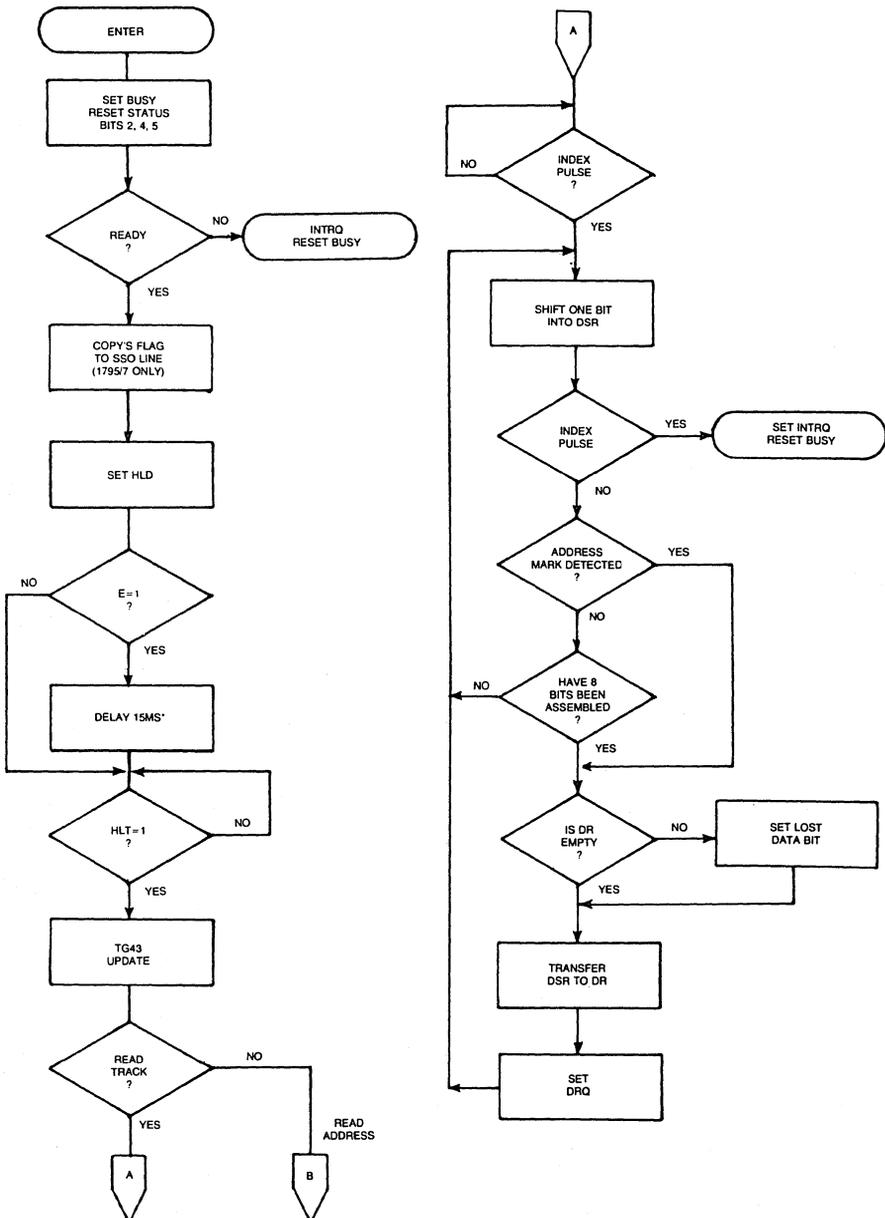


TYPE III COMMAND WRITE TRACK

DATA PATTERN IN DR (HEX)	FD179X INTERPRETATION IN FM (DDEN = 1)	FD1791/3 INTERPRETATION IN MFM (DDEN = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Preset CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, Clk = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with Clk = D7	Write FC in MFM
FD	Write FD with Clk = FF	Write FD in MFM
FE	Write FE, Clk = C7, Preset CRC	Write FE in MFM
FF	Write FF with Clk = FF	Write FF in MFM

*Missing clock transition between bits 4 and 5

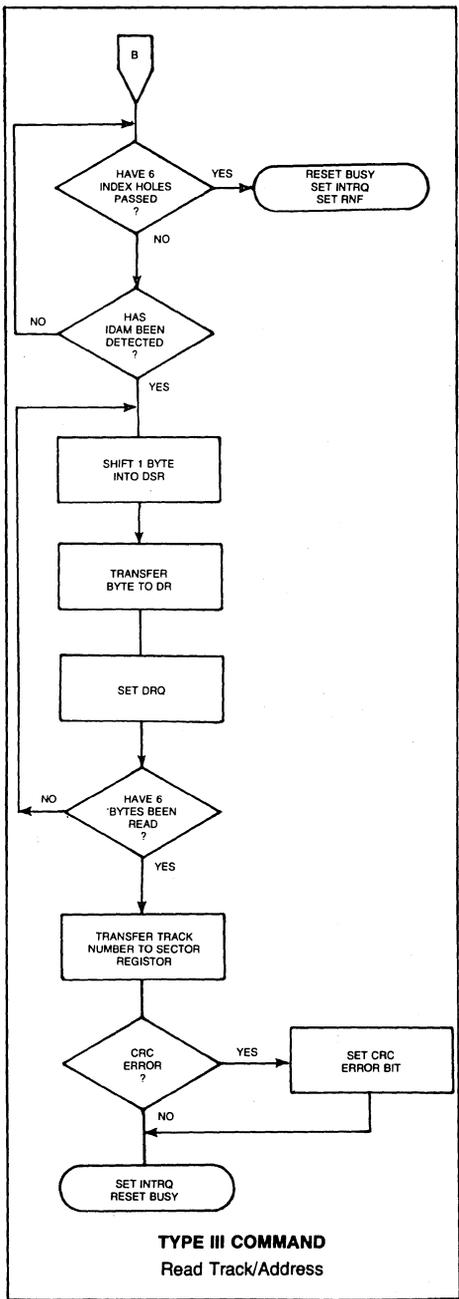
**Missing clock transition between bits 3 & 4



*If TEST = 0, NO DELAY

If TEST = 1 and CLK = 1 MHZ, 30 MS DELAY

TYPE III COMMAND
Read Track/Address



TYPE IV COMMAND

FORCE INTERRUPT

This command can be loaded into the command register at any time. If there is a current command under execution (Busy Status Bit set), the command will be terminated and an interrupt will be generated when the condition specified in the I_0 through I_3 field is detected. The interrupt conditions are shown below:

- I_0 = Not-Ready-To-Ready Transition
- I_1 = Ready-To-Not-Ready Transition
- I_2 = Every Index Pulse
- I_3 = Immediate Interrupt (requires reset, see Note)

NOTE: If $I_0 - I_3 = 0$, there is no interrupt generated but the current command is terminated and busy is reset. This is the only command that will enable the immediate interrupt to clear on a subsequent Load Command Register or Read Status Register.

STATUS DESCRIPTION

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 6.

FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command. Upon receipt of the Write Track command, the FD179X raises the Data Request signal. At this point in time, the user loads the data register with desired data to be written on the disk. For every byte of information to be written on the disk, a data request is generated. This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the FD179X detects a data pattern of F5 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation. For instance, in FM an FE pattern will be interpreted as an ID address mark (DATA-FE, CLK-C7) and the CRC will be initialized. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

IBM 3740 FORMAT—128 BYTES/SECTOR

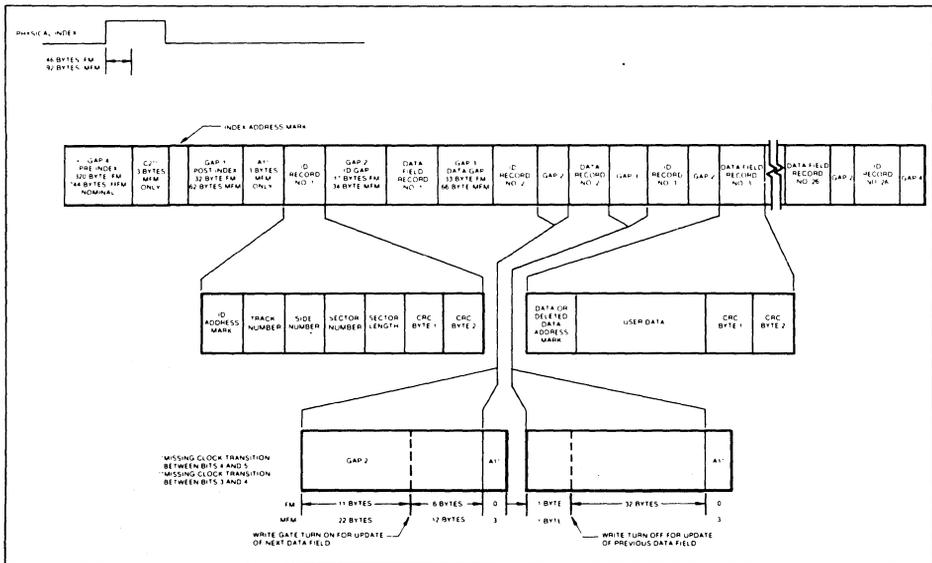
Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	FF (or 00) ¹
6	00
1	FC (Index Mark)
26	FF (or 00)
6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 thru 1A)
1	00
1	F7 (2 CRC's written)
11	FF (or 00)
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
27	FF (or 00)
247**	FF (or 00)

*Write bracketed field 26 times

**Continue writing until FD179X interrupts out. Approx. 247 bytes.

1-Optional '00' on 1795/7 only.



IBM TRACK FORMAT

SECTION 2

IBM SYSTEM 34 FORMAT- 256 BYTES/SECTOR

Shown below is the IBM dual-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
80	4E
12	00
3	F6
1	FC (Index Mark)
50*	4E
12	00
3	F5
1	FE (ID Address Mark)
1	Track Number (0 thru 4C)
1	Side Number (0 or 1)
1	Sector Number (1 thru 1A)
1	01
1	F7 (2 CRCs written)
22	4E
12	00
3	F5
1	FB (Data Address Mark)
256	DATA
1	F7 (2 CRCs written)
54	4E
598**	4E

* Write bracketed field 26 times
 **Continue writing until FD179X interrupts out.
 Approx. 598 bytes.

1. NON-IBM FORMATS

Variations in the IBM format are possible to a limited extent if the following requirements are met: sector size must be a choice of 128, 256, 512, or 1024 bytes; gap size must be according to the following table. Note that the Index Mark is not required by the 179X. The minimum gap sizes shown are that which is required by the 179X, with PLL lock-up time, motor speed variation, etc., adding additional bytes.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
*	6 bytes 00	12 bytes 00 3 bytes A1
Gap III	10 bytes FF	24 bytes 4E 3 bytes A1
**	4 bytes 00	8 bytes 00
Gap IV	16 bytes FF	16 bytes 4E

*Byte counts must be exact.

**Byte counts are minimum, except exactly 3 bytes of A1 must be written.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

V_{DD} With Respect to V_{SS} (Ground) = 15 to -0.3V

Operating Temperature

0°C to 70°C

Max. Voltage to Any Input With Respect to V_{SS} = 15 to -0.3V

Storage Temperature

-55°C to +125°C

V_{DD} = 10 ma Nominal V_{CC} = 35 ma Nominal

OPERATING CHARACTERISTICS (DC)

TA = 0°C to 70°C, V_{DD} = + 12V ± .6V, V_{SS} = 0V, V_{CC} = + 5V ± .25V

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS	CONDITIONS
I _{IL}	Input Leakage		10	μA	V _{IN} = V _{DD}
I _{OL}	Output Leakage		10	μA	V _{OUT} = V _{DD}
V _{IH}	Input High Voltage	2.6		V	
V _{IL}	Input Low Voltage		0.8	V	
V _{OH}	Output High Voltage	2.8		V	I _O = -100 μA
V _{OL}	Output Low Voltage		0.45	V	I _O = 1.6 mA
P _D	Power Dissipation		0.5	W	

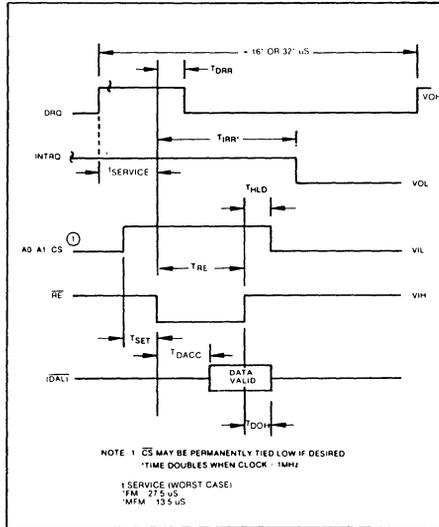
TIMING CHARACTERISTICS

$T_A = 0^\circ\text{C}$ to 70°C , $V_{DD} = +12\text{V} \pm .6\text{V}$, $V_{SS} = 0\text{V}$, $V_{CC} = +5\text{V} \pm .25\text{V}$

READ ENABLE TIMING

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{\text{RE}}$	50			nsec	
THLD	Hold ADDR & CS from $\overline{\text{RE}}$	10			nsec	
TRE	$\overline{\text{RE}}$ Pulse Width	400			nsec	$C_L = 50\text{ pf}$
TDRR	DRQ Reset from $\overline{\text{RE}}$		400	500	nsec	
TIRR	INTRQ Reset from $\overline{\text{RE}}$		500	3000	nsec	See Note 5
TDACC	Data Access from $\overline{\text{RE}}$			350	nsec	$C_L = 50\text{ pf}$
TDOH	Data Hold From $\overline{\text{RE}}$	50		150	nsec	$C_L = 50\text{ pf}$

SECTION 2



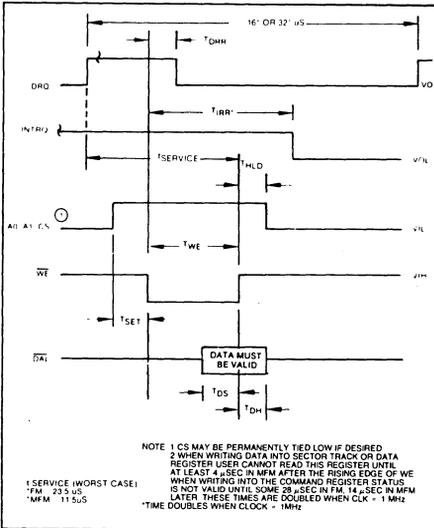
READ ENABLE TIMING

WRITE ENABLE TIMING

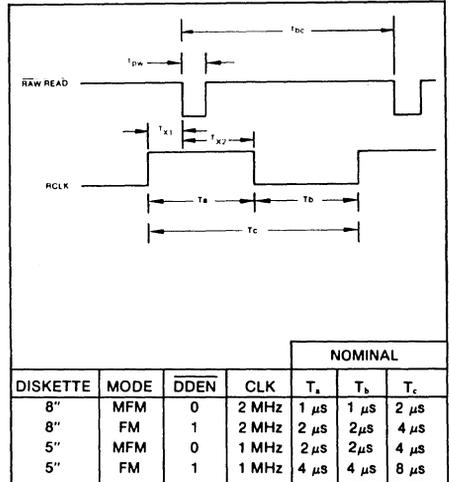
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to \overline{WE}	50			nsec	See Note 5
THLD	Hold ADDR & CS from \overline{WE}	10			nsec	
TWE	\overline{WE} Pulse Width	350			nsec	
TDRR	DRQ Reset from \overline{WE}		400	500	nsec	
TIIR	INTRQ Reset from \overline{WE}		500	3000	nsec	
TDS	Data Setup to \overline{WE}	250			nsec	
TDH	Data Hold from \overline{WE}	70			nsec	

INPUT DATA TIMING:

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T_{pw}	$\overline{Raw Read}$ Pulse Width	100	200		nsec	See Note 1
t_{bc}	$\overline{Raw Read}$ Cycle Time		1500		nsec	1800 ns @ 70°C
T_c	RCLK Cycle Time		1500		nsec	1800 ns @ 70°C
T_{x1}	RCLK hold to $\overline{Raw Read}$	40			nsec	See Note 1
T_{x2}	$\overline{Raw Read}$ hold to RCLK	40			nsec	



WRITE ENABLE TIMING

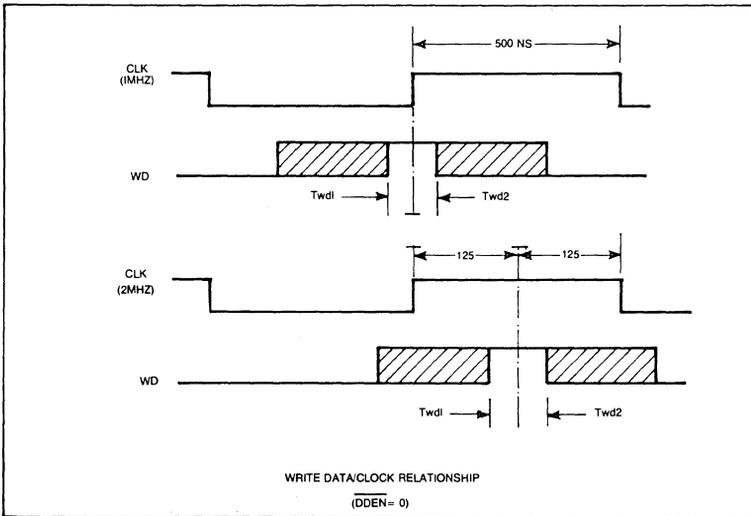


INPUT DATA TIMING

WRITE DATA TIMING: (ALL TIMES DOUBLE WHEN CLK = 1 MHz)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Twp	Write Data Pulse Width	450	500	550	nsec	FM
		150	200	250	nsec	MFM
Twg	Write Gate to Write Data		2		μ sec	FM
			1		μ sec	MFM
Tbc	Write data cycle Time		2,3, or 4		μ sec	\pm CLK Error
Ts	Early (Late) to Write Data	125			nsec	MFM
Th	Early (Late) From Write Data	125			nsec	MFM
Twf	Write Gate off from WD		2		μ sec	FM
			1		μ sec	MFM
Twd1	WD Valid to Clk	100			nsec	CLK=1 MHZ
		50			nsec	CLK=2 MHZ
Twd2	WD Valid after CLK	100			nsec	CLK=1 MHZ
		30			nsec	CLK=2 MHZ

SECTION 2

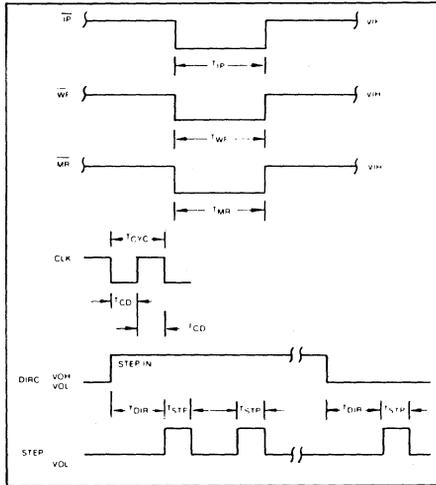


WRITE DATA TIMING

MISCELLANEOUS TIMING:

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TCD ₁	Clock Duty (low)	230	250	20000	nsec	See Note 5 ± CLK ERROR
TCD ₂	Clock Duty (high)	200	250	20000	nsec	
TSTP	Step Pulse Output	2 or 4			μsec	
TDIR	Dir Setup to Step		12		μsec	See Note 5
TMR	Master Reset Pulse Width	50			μsec	
TIP	Index Pulse Width	10			μsec	
TWF	Write Fault Pulse Width	10			μsec	

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MISCELLANEOUS TIMING

NOTES:

1. Pulse width on RAW READ (Pin 27) is normally 100-300 ns. However, pulse may be any width if pulse is entirely within window. If pulse occurs in both windows, then pulse width must be less than 300 ns for MFM at CLK = 2 MHz and 600 ns for FM at 2 MHz. Times double for 1 MHz.
2. A PPL Data Separator is recommended for 8" MFM.
3. tbc should be 2 μs, nominal in MFM and 4 μs nominal in FM. Times double when CLK = 1 MHz.
4. RCLK may be high or low during RAW READ (Polarity is unimportant).
5. Times double when clock = 1 MHz.

Table 6 STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

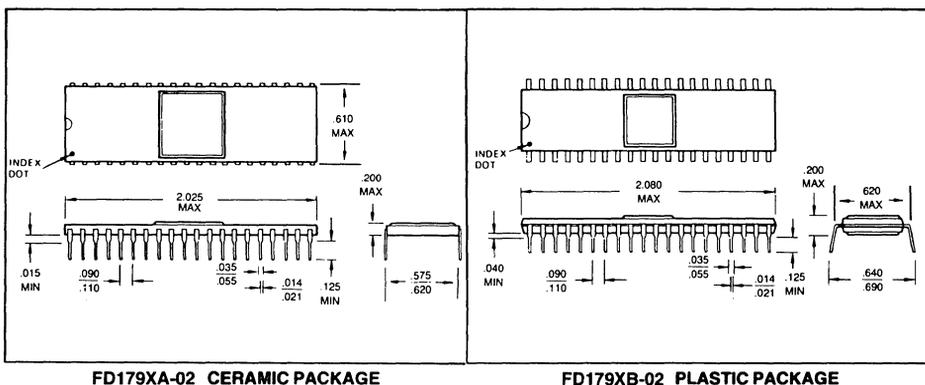
STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of WRPT input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the TROO input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the IP input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

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This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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FD179X Application Notes

NOVEMBER, 1980

2 Z0-10ms

INTRODUCTION

Over the past several years, the Floppy Disk Drive has become the most popular on-line storage device for mini and microcomputer systems. Its fast access time, reliability and low cost-per-bit ratio enables the Floppy Disk Drive to be *the* solution in mass storage for microprocessor systems. The drive interface to the Host system is standardized, allowing the OEM to substitute one drive for another with minimum hardware/ software modifications.

Since Floppy Disk Data is stored and retrieved as a self-clocking serial data stream, some means of separating the clock from the data and assembling this data in parallel form must be accomplished. Data is stored on individual Tracks of the media, requiring control of a stepper motor to move the Read/Write head to a predetermined Track. Byte synchronization must also be accomplished to insure that the parallel data is properly assembled. After all the design considerations are met, the final controller can consist of 40 or more TTL packages.

To alleviate the burden of Floppy Disk Controller design, Western Digital has developed a Family of LSI Floppy Disk controller devices. Through its own set of macro commands, the FD179X Controller Family will perform all the functions necessary to read and write data to the drive. Both the 8" standard and 5¼" mini-floppy are supported with single or double density recording techniques. The FD179X is compatible with the IBM 3740 (FM) data format, or the System 34 (MFM) standards. Provisions for non-standard formats and variable sector lengths have been included to provide more storage capability per track. Requiring standard +5, +12 power supplies the FD179X is available in a standard 40 pin dual-in-line package.

The FD179X Family consists of 6 devices. The differences between these devices is summarized in Figure 1. The 1792 and 1794 are "single density only" devices, with the Double Density Enable pin (DDEN) left open by the user. Both True and inverted Data bus devices are available. Since the 179X can only drive one TTL Load, a true data bus system may use the 1791 with external inverting buffers to arrive at a true bus scheme. The 1795 and 1797 are identical to the 1791 and 1793, except a side select output has been added that is controlled through the Command Register.

SYSTEM DESIGN

The first consideration in Floppy Disk Design is to determine which type of drive to use. The choice ranges from single-density single sided mini-floppy to the 8" double-density double-sided drive. Figure 2 illustrates the various drive and data capacities associated with each type. Although the 8" double-density drive offers twice as much storage, a more complex data separator and the addition of Write Precompensation circuits are mandatory for reliable data transfers. Whether to go with 8" double-density or not is dependent upon PC board space and the additional circuitry needed to accurately recover data with extreme bit shifts. The byte transfer time defines the nominal time required to transfer one byte of data from the drive. If the CPU used cannot service a byte in this time, then a DMA scheme will probably be required. The 179X also needs a few microseconds for overhead, which is subtracted from the transfer time. Figure 3 shows the actual service times that the CPU must provide on a byte-by-byte basis. If these times are not met, bytes of data will be lost during a read or write operation. For each byte transferred, the 179X generates a DRQ (Data Request) signal on Pin 38. A bit is provided in the status register which is also set upon receipt of a byte from the Disk. The user has the option of reading the status register through program control or using the DRQ Line with DMA or interrupt schemes. When the data register is read, both the status register DRQ bit and the DRQ Line are automatically reset. The next full byte will again set the DRQ and the process continues until the sector(s) are read. The Write operation works exactly the same way, except a WRITE to the Data Register causes a reset of both DRQ's.

RECORDING FORMATS

The FD179X accepts data from the disk in a Frequency-Modulated (FM) or Modified-Frequency-Modulated (MFM) Format. Shown in Figures 4A and 4B are both these Formats when writing a Hexidecimal byte of 'D2'. In the FM mode, the 8 bits of data are broken up into "bit cells." Each bit cell begins with a clock pulse and the center of the bit cell defines the data. If the data bit = 0, no pulse is written; if the data = 1, a pulse is written in the center of the cell. For the 8" drive, each clock is written 4 microseconds apart.

In the MFM mode, clocks are decoded into the data stream. The byte is again broken up into bit cells, with the data bit written in the center of the bit cell if data = 1. Clocks are only written if both surrounding data bits are zero. Figure 4B shows that this occurs only once between Bit cell 4 and 5. Using this encoding scheme, pulses can occur 2, 3 or 4 microseconds apart. The bit cell time is now 2 microseconds; twice as much data can be recorded without increasing the Frequency rate due to this encoding scheme.

The 179X was designed to be compatible with the IBM 3740 (FM) and System 34 (MFM) Formats. Although most users do not have a need for data exchange with IBM mainframes, taking advantage of these well studied formats will insure a high degree of system performance. The 179X will allow a change in gap fields and sector lengths to increase usable storage capacity, but variations away from these standards is not recommended. Both IBM standards are soft-sector format. Because of the wide variation in address marks, the 179X can only support soft-sectored media. Hard sectored diskettes have continued to lose popularity, mainly due to the unavailability of a standard and the limitation of sector lengths imposed by the physical sector holes in the diskette.

PROCESSOR INTERFACE

The Interface of the 179X to the CPU consists of an 8-bit Bi-directional bus, read/write controls and optional interrupt lines. By selecting the device via the CHIP SELECT Line, each of the five internal registers can be accessed.

Shown below are the registers and their addresses:

PIN 3 CS	PIN 6 A ₁	PIN 5 A ₀	PIN 4 RE=Ø	PIN 2 WE=Ø
0	0	0	STATUS REG	COMMAND REG
0	0	1	TRACK REG	TRACK REG
0	1	0	SECTOR REG	SECTOR REG
0	1	1	DATA REG	DATA REG
1	X	X	H1-Z	H1-Z

Each time a command is issued to the 179X, the Busy bit is set and the INTRQ (Interrupt Request) Line is reset. The user has the option of checking the busy bit or use the INTRQ Line to denote command completion. The Busy bit will be reset whenever the 179X is idle and awaiting a new command. The INTRQ Line, once set, can only be reset by a READ of the status register or issuing a new command. The MR (Master Reset) Line does not affect INTRQ.

The A₀, A₁, Lines used for register selections can be configured at the CPU in a variety of ways. These lines may actually tie to CPU address lines, in which case the 179X will be memory-mapped and addressed like RAM. They may also be used under Program Control by tying to a port device such as the 8255, 6820, etc. As a diagnostic tool when checking out the CPU interface, the Track and Sector registers should respond like "RAM" when the 179X is idle (Busy = INTRQ = 0).

Because of internal synchronization cycles, certain time delays must be introduced when operating under Programmed I/O. The worst case delays are:

OPERATION	NEXT OPERATION	DELAY REQ'D
WRITE TO COMMAND REG	READ STATUS REGISTER	MFM = 14µs* FM = 28µs.
WRITE TO ANY REGISTER	READ FROM A DIFFERENT REG	NO DELAY

*NOTE: Times Double when CLK = 1MHz (5¼" drive)

Other CPU interface lines are CLK, \overline{MR} and \overline{DDEN} . The CLK line should be 2MHz (8" drive) or 1MHz (5¼" drive) with a 50% duty cycle. Accuracy should be ±1% (crystal source) since all internal timing, including stepping rates, are based upon this clock.

The \overline{MR} or Master Reset Line should be strobed a minimum of 50 microseconds upon each power-on condition. This line clears and initializes all internal registers and issues a restore command (Hex '03') on the rising edge. A quicker stepping rate can be written to the command register after a \overline{MR} , in which case the remaining steps will occur at the faster programmed rate. The 179X will issue a maximum of 255 stepping pulses in an attempt to expect the \overline{TROO} line to go active low. This line should be connected to the drive's \overline{TROO} sensor.

The \overline{DDEN} line causes selection of either single density (DDEN = 1) or double density operation. DDEN should not be switched during a read or write operation.

FLOPPY DISK INTERFACE

The Floppy Disk Interface can be divided into three sections: Motor Control, Write Signals and Read Signals. All of these lines are capable of driving one TTL load and not compatible for direct connection to the drive. Most drives require an open-collector TTL interface with high current drive capability. This must be done on all outputs from the 179X. Inputs to the 179X may be buffered or tied to the Drives outputs, providing the appropriate resistor termination networks are used. Undershoot should not exceed -0.3 volts, while integrity of V_{IH} and V_{OH} levels should be kept within spec.

MOTOR CONTROL

Motor Control is accomplished by the STEP and DIRC Lines. The STEP Line issues stepping pulses with a period defined by the rate field in all Type I commands. The DIRC Line defines the direction of steps (DIRC = 1 STEP IN/DIRC = 0 STEP OUT).

Other Control Lines include the IP or Index Pulse. This Line is tied to the drives' Index L.E.D. sensor and makes an active transition for each revolution of the diskette. The TROO Line is another L.E.D. sensor that informs the 179X that the stepper motor is at its furthest position, over Track 00. The READY Line can be used for a number of functions, such as sensing "door open", Drive motor on, etc. Most drives provide a programmable READY Signal selected by option jumpers on the drive. The 179X will look at the ready signal prior to executing READ/WRITE commands. READY is not inspected during any Type I commands. All Type I commands will execute regardless of the Logic Level on this Line.

WRITE SIGNALS

Writing of data is accomplished by the use of the WD, WG, WF, TG43, EARLY and LATE Lines. The WG or Write Gate Line is used to enable write current at the drive's R/W head. It is made active prior to writing data on the disk; The WF or WRITE FAULT Line is used to inform the 179X of a failure in drive electronics. This signal is multiplexed with the VFOE Line and must be logically separated if required. Figure 5 illustrates three methods of demultiplexing.

The TG43 or "TRACK GREATER than 43" Line is used to decrease the Write current on the inner tracks, where bit densities are the highest. If not required on the drive, TG43 may be left open.

WRITE PRECOMPENSATION

The 179X provides three signals for double density Write Precompensation use. These signals are WRITE DATA, EARLY and LATE. When using single density drives (eighth 8" or 5 1/4"), Write Precompensation is not necessary and the WRITE DATA line is generally TTL Buffered and sent directly to the drive. In this mode, EARLY and LATE are left open.

For double density use, Write Precompensation is a function of the drive. Some manufacturers recommend Precompensating the 5 1/4" drive, while others do not. With the 8" drive, Precompensation may be specified from TRACK 43 on, or in most cases, all TRACKS. If the recommended Precompensation is not specified,

check with the manufacturer for the proper configuration required.

The amount of Precompensation time also varies. A typical value will usually be specified from 100-300ns. Regardless of the parameters used, Write Precompensation must be done external to the 179X. When DDEN is tied low, EARLY or LATE will be activated at least 125ns. before and after the Write Data pulse. An Algorithm internal the 179X decides whether to raise EARLY or LATE, depending upon the previous bit pattern sent. As an example, suppose the recommended Precomp value has been specified at 150ns. The following action should be taken:

EARLY	LATE	ACTION TAKEN
0	0	delay WD by 150ns (nominal)
0	1	delay WD by 300ns (2X value)
1	0	do not delay WD

There are two methods of performing Write Precompensation:

- 1) External Delay elements
- 2) Digitally

Shown in Figure 6 is a Precomp circuit using the Western Digital 2143 clock generator as the delay element. The WD pulse from the 179X creates a strobe to the 2143, causing subsequent output pulses on the $\delta 1$, $\delta 2$ and $\delta 3$ signals. The 5K Precomp adjust sets the desired Precomp value. Depending upon the condition of EARLY and LATE, $\delta 1$ will be used for EARLY, $\delta 2$ for nominal (EARLY = LATE = 0), and $\delta 3$ for LATE. The use of "one-shots" or delay line in a Write Precompensation scheme offers the user the ability to vary the Precomp value. The $\delta 4$ output resets the 74LS175 Latch in anticipation of the next WD pulse. Figure 7 shows the WD-EARLY/LATE relationship, while Figure 8 shows the timing of this write Precomp scheme.

Another method of Precomp is to perform the function digitally. Figure 9 illustrates a relationship between the WD pulse and the CLK pin, allowing a digital Precomp scheme. Figure 10 shows such a scheme with a preset Write Precompensation value of 250ns. The synchronous counter is used to generate 2MHz and 4MHz clock signals. The 2MHz clock is sent to the CLK input of the 179X and the 4MHz is used by the 4-bit shift register. When a WD pulse is not present, the 4MHz clock is shifting "ones" through the shift register and maintaining Q_0 at a zero level. When a WD pulse is present, a zero is loaded at either A, B, or C depending upon the states of LATE, EN PRECOMP and EARLY. The zero is then shifted by the 4MHz clock until it reaches the Q_0 output. The number of shift operations determines whether the WRITE DATA pulse is written early, nominal or late. If both FM and MFM operations is a system requirement, the output of this circuit should be disabled and the WD pulse should be sent directly to the drive.



DATA SEPARATION

The 179X has two inputs (RAW READ & RCLK) and one output (VFOE) for use by an external data separator. The RAW READ input must present clock and data pulses to the 179X, while the RCLK input provides a "window" or strobe signal to clock each RAW READ pulse into the device. An ideal Data Separator would have the leading edge of the RAW READ pulse occur in the exact center of the RCLK strobe.

Motor Speed Variation, Bit shifts and read amplifier recovery circuits all cause the RAW READ pulses to drift away from their nominal positions. As this occurs, the RAW READ pulses will shift left or right with respect to RCLK. Eventually, a pulse will make its transition outside of its RCLK window, causing either a CRC error or a Record-not-Found error at the 179X.

A Phase-Lock-Loop circuit is one method of achieving synchronization between the RCLK and RAW READ signals. As RAW READ pulses are fed to the PLL, minor adjustments of the free-running RCLK frequency can be made. If pulses are occurring too far apart, the RCLK frequency is *decreased* to keep synchronization. If pulses begin to occur closer together, RCLK is *increased* until this new higher frequency is achieved. In normal read operations, RCLK will be constantly adjusted in an attempt to match the incoming RAW READ frequency.

Another method of Data Separation is the Counter-Separator technique. The RCLK signal is again free-running at a nominal rate, until a RAW READ pulse occurs. The Separator then denotes the position of the pulse with respect to RCLK (by the counter value), and counts down to increase or decrease the current RCLK window. The next RCLK window will occur at a nominal rate and will continue to run at this frequency until another RAW READ pulse adjusts RCLK, but only the present window is adjusted.

Both PPL and Counter/Separator are acceptable methods of Data Separation. The PPL has the highest reliability because of its "tracking" capability and is recommended for 8" double density designs.

As a final note, the term "Data Separator" may be misleading, since the physical separation of clock and data bits are not actually performed. This term is used throughout the industry, and can better be described as a "Data Recovery Circuit" rather than a Data Separator.

The VFOE signal is an output from the 179X that signifies the head has been loaded and valid data pulses are appearing on the RAW READ line. It can be used to enable the Data Separator and to insure clean RCLK transitions to the 179X. Since some drives will output random pulses when the head is disengaged, VFOE can prevent an erratic RCLK signal during this time. If the Data Separator requires synchronization during a known pattern of one's or zero's, then RG (READ GATE) can be used. The RG signal will go active when the 179X is currently over a field of zeros or ones. RG is not available on the 1795/1797 devices, since this signal was replaced with the SSO (Side Select Output) Line.

Shown in Figure 11 is a 2½ IC Counter/Separator. The 74LS193 free runs at a frequency determined by the CRYCLK input. When a RAW READ pulse occurs, the counter is loaded with a starting count of '5'. When the RAW READ Line returns to a Logic 1, the counter counts down to zero and again free runs. The 74LS74 insures a 50% duty cycle to the 179X and performs a divide-by-two of the Q₀ output.

Figure 12 illustrates another Counter/Separator utilizing a PROM as the count generator. Depending upon the RAW READ phase relationship to RCLK, the PROM is addressed and its data output is used as the counter value. A 16MHz clock is required for 8" double density, while an 8MHz clock can be used for single density.

Figure 13 shows a Phase-Lock-Loop data recovery circuit. The phase detector (U2, Figure 2) compares the phase of the SHAPED DATA pulse to the phase of VFO CLK ÷ 2. If VFO CLK ÷ 2 is lagging the SHAPED DATA pulse an output pulse on #9, U2 is generated. The filter/amplifier converts this pulse into a DC signal which increases the frequency of the VCO. If, correspondingly, CLK ÷ 2 is leading the SHAPED DATA pulse, an output pulse on #5, U2 is generated. This pulse is converted into a DC signal which decreases the frequency of the VCO. These two actions cause the VCO to track the frequency of the incoming READ DATA pulses. This correction process to keep the two signals in phase is constantly occurring because of spindle speed variation and circuit parameter variations.

The operating specifications for this circuit are as follows:

Free Running Frequency	2MHz
Capture Range	± 15%
Lock Up Time	50 microsec. "1111" or "0000" Pattern 100 Microsec "1010" Pattern

The RAW READ pulses are generated from the falling edge of the SHAPED DATA pulses. The pulses are also reshaped to meet the 179X requirements. VFO CLK ÷ 2 OR 4 is divided by 2 once again to obtain VFO CLK OUT whose frequency is that required by the 179X RCLK input. RCLK must be controlled by VFOE so VFOE is sampled on each rising edge of VFO CLK OUT. When VFOE goes active EN RCLK goes active in synchronization with VFO CLK OUT preventing any glitches on the RCLK output. When VFOE goes inactive EN RCLK goes inactive in synchronization with VFO CLK OUT, again preventing any glitches on the RCLK output.

Figure 14 illustrates a PPL data recovery circuit using the Western Digital 1691 Floppy Support device. Both data recovery and Write Precomp Logic is contained within the 1691, allowing low chip count and PLL reliability. The 74S124 supplies the free-running VCO output. The PUMP UP and PUMP DOWN signals from the 1691 are used to control the 74S124's frequency.

COMMAND USAGE

Whenever a command is successfully or unsuccessfully completed, the busy bit of the status register is reset and the INTRQ line is forced high. Command termination may be detected either way. The INTRQ can be tied to the host processor's interrupt with an appropriate service routine to terminate commands. The busy bit may be monitored with a user program and will achieve the same results through software. Performing both an INTRQ and a busy bit check is not recommended because a read of the status register to determine the condition of the busy bit will reset the INTRQ line. This can cause an INTRQ from not occurring.

RESTORE COMMAND

On some disk drives, it is possible to position the R/W head outward past Track 00 and prevent the TROO line from going low unless a STEP IN is first performed. If this condition exists in the drive used, the RESTORE command will never detect a TROO. Issuing several STEP IN pulses before a RESTORE command will remedy this situation. The RESTORE and all other Type I commands will execute even though the READY bit indicates the drive is not ready (NOT READY = 1).

READ TRACK COMMAND

The READ TRACK command can be used to manually inspect data on a hard copy printout. Gaps, address marks and all data are brought in to the data register during this command. The READ TRACK command may be used to inspect diskettes for valid formatting and data fields as well as address marks. Since the 179X does not synchronize clock and data until the Index Address Mark is detected, data previous to this ID mark will not be valid. READ GATE (RG) is not actuated during this command.

READ ADDRESS COMMAND

In systems that use either multiple drives or sides, the read address command can be used to tell the host processor which drive or side is selected. The current position of the R/W head is also denoted in the six bytes of data that are sent to the computer.

TRACK	SIDE	SECTOR	CRS LENGTH	CRC 1	CRC 2
-------	------	--------	------------	-------	-------

The READ ADDRESS command as well as all other Type II and Type III commands will not execute if the READY line is inactive (READY = 0). Instead, an interrupt will be generated and the NOT READY status bit will be set to a 1.

FORCED INTERRUPT COMMAND

The Forced Interrupt command is generally used to terminate a multiple sector command or to insure Type I status in the status register. The lower four bits of the command determine the conditional interrupt as follows:

1_0	=	NOT-READY TO READY TRANSITION
1_1	=	READY TO NOT-READY TRANSITION
1_2	=	EVERY INDEX PULSE
1_3	=	IMMEDIATE INTERRUPT

Regardless of the conditional interrupt set, any command that is currently being executed when the Forced Interrupt command is loaded will immediately be terminated and the busy bit will be reset indicating an idle condition.

Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred.

The conditional interrupt is enabled when the corresponding bit positions of the command ($1_3 - 1_0$) are set to a 1. If $1_3 - 1_0$ are all set to zero, no interrupt will occur, but any command presently under execution will be immediately terminated upon receipt of the Force Interrupt command (HEX DO).

As usual, to clear the interrupt a read of the status register or a write to the command register is required. The exception is when using the immediate interrupt condition ($1_3 = 1$). If this command is loaded into the command register, an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt; another forced interrupt command with $1_3 - 1_0 = 0$ must be loaded into the command register in order to reset the INTRQ from this condition.

More than one condition may be set at a time. If for example, the READY TO NOT-READY condition ($1_1 = 1$) and the Every Index Pulse ($1_2 = 1$) are both set, the resultant command would be HEX "DA". The "OR" function is performed so that either a READY TO NOT-READY or the next Index Pulse will cause an interrupt condition.

DATA RECOVERY

Occasionally, the R/W head of the disk drive may get "off track", and dust or dirt may get trapped on the media. Both of these conditions will cause a RECORD NOT FOUND and/or a CRC error to occur. This "soft error" can usually be recovered by the following procedure:

1. Issue the command again
2. Unload and load the head and repeat step
3. Issue a restore, seek the track, and repeat step 1

If RNF or CRC errors are still occurring after trying these methods, a "hard error" may exist. This is usually caused by improper disk handling, exposure to high magnetic fields, etc. and generally results in destroying portions or tracks of the diskette.

FIGURE 1 DEVICE CHARACTERISTICS

DEVICE	SNGL DENSITY	DBLE DENSITY	INVERTED BUS	TRUE BUS	DOUBLE-SIDED
1791	X	X	X		
1792	X		X		
1793	X	X		X	
1794	X			X	
1795	X	X	X		X
1797	X	X		X	X

FIGURE 2 STORAGE CAPACITIES

SIZE	DENSITY	SIDES	UNFORMATTED CAPACITY (NOMINAL)		BYTE TRANSFER TIME	FORMATTED CAPACITY	
			PER TRACK	PER DISK		PER TRACK	PER DISK
5¼"	SINGLE	1	3125	109,375*	64µs	2304**	80,640
5¼"	DOUBLE	1	6250	218,750	32µs	4608***	161,280
5¼"	SINGLE	2	3125	218,750	64µs	2304	161,280
5¼"	DOUBLE	2	6250	437,500	32µs	4608	322,560
8"	SINGLE	1	5208	401,016	32µs	3328	256,256
8"	DOUBLE	1	10,416	802,032	16µs	6656	512,512
8"	SINGLE	2	5208	802,032	32µs	3328	512,512
8"	DOUBLE	2	10,416	1,604,064	16µs	6656	1,025,024

*Based on 35 Tracks/Side

**Based on 18 Sectors/Track (128 byte/sec)

***Based on 18 Sectors/Track (256 bytes/sec)

FIGURE 3 NOMINAL VS. WORSE CASE SERVICE TIME

SIZE	DENSITY	NOMINAL TRANSFER TIME	WORST-CASE 179X SERVICE TIME	
			READ	WRITE
5 1/4"	SINGLE	64μs	55.0μs	47.0μs
5 1/4"	DOUBLE	32μs	27.5μs	23.5μs
8"	SINGLE	32μs	27.5μs	23.5μs
8"	DOUBLE	16μs	13.5μs	11.5μs

FIGURE 4A. FM RECORDING

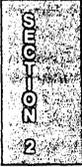
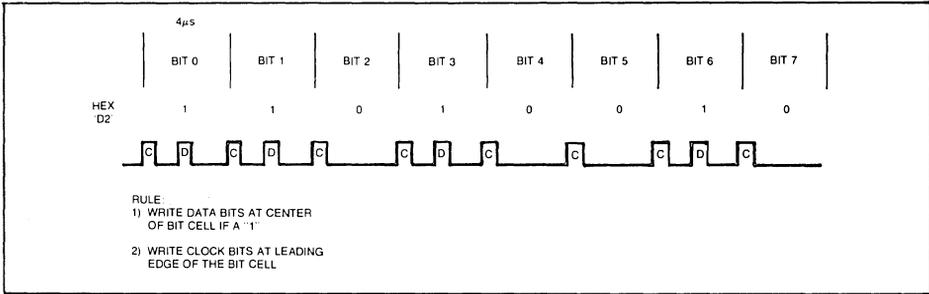


FIGURE 4B. MFM RECORDING

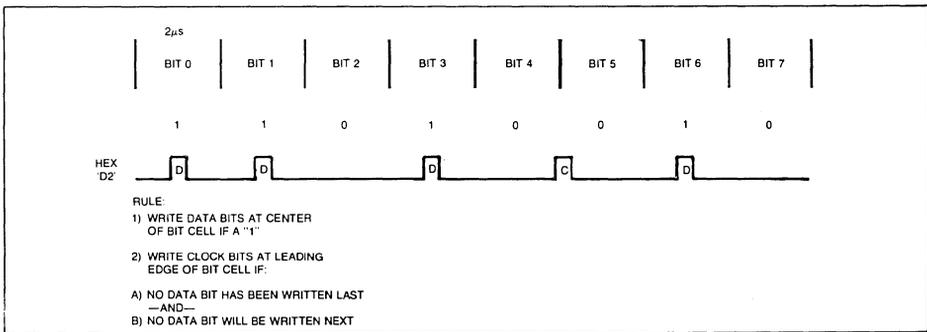
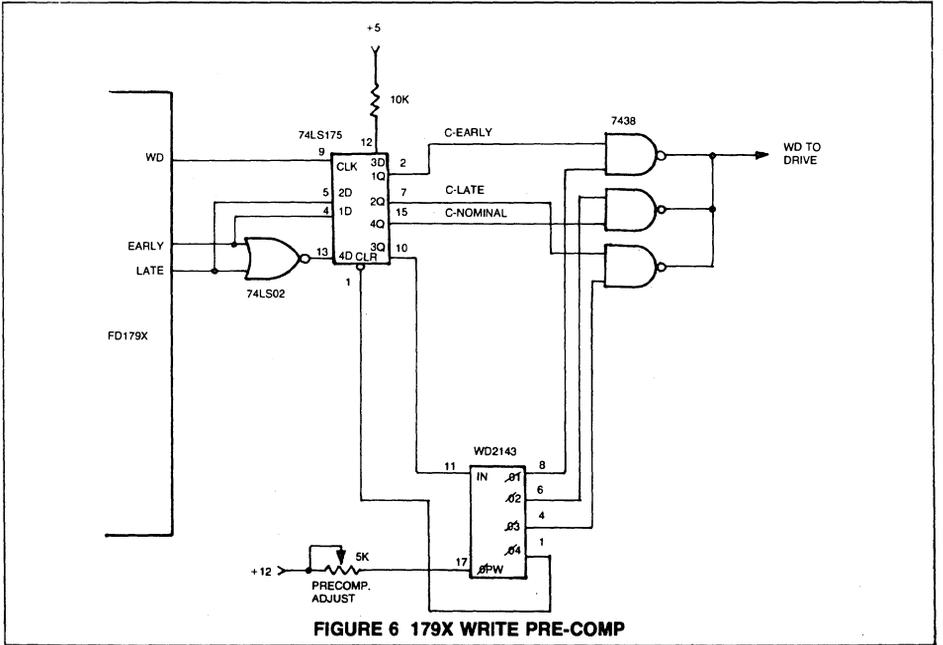
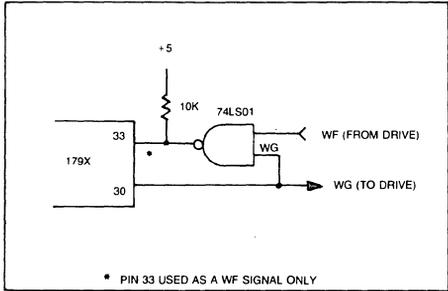
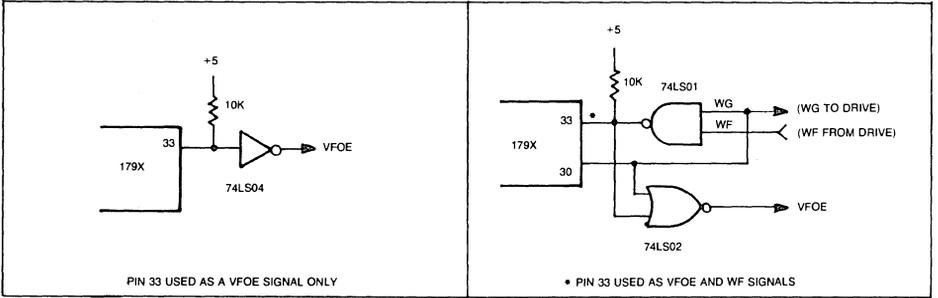


FIGURE 5 WF/VFOE DEMULTIPLEXING CIRCUITRY



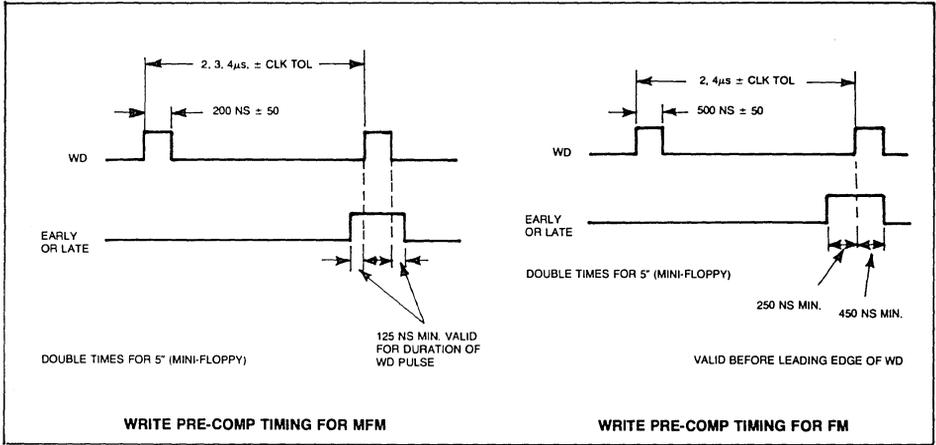


FIGURE 7 WRITE PRE-COMP TIMING

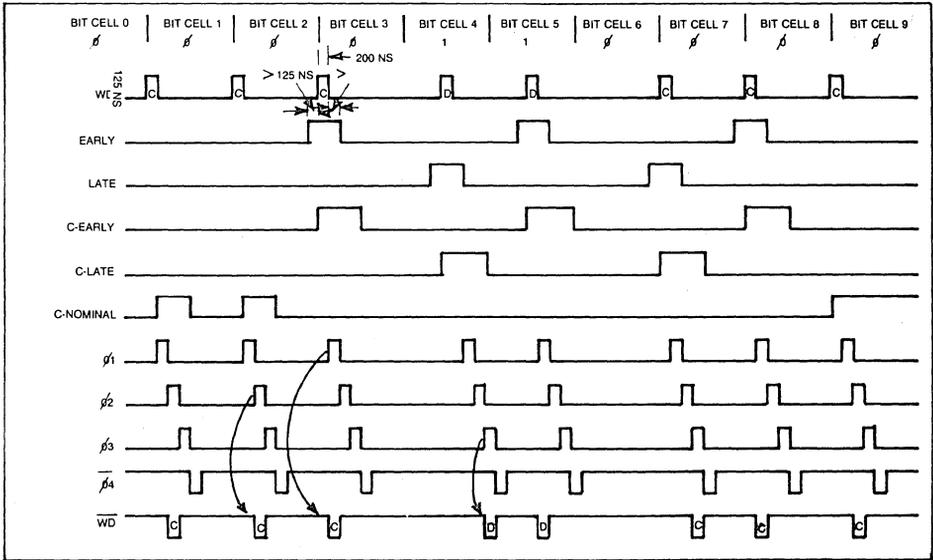


FIGURE 8 PRECOMP TIMING FOR CIRCUIT IN FIGURE 6

SMT-10ZS

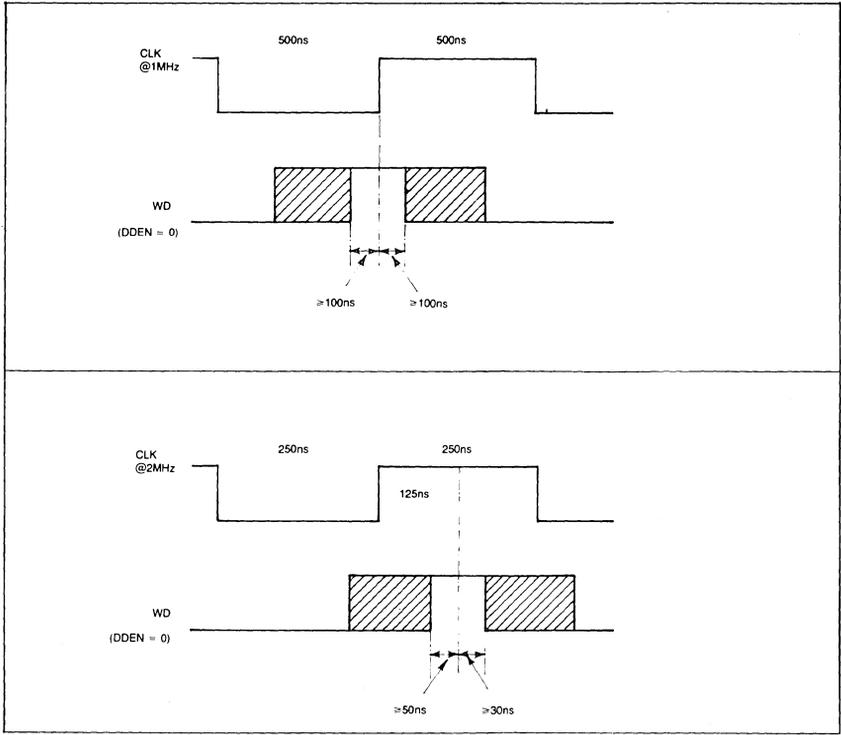


FIGURE 9 WD/CLK RELATIONSHIP FOR WRITE PRECOMP USE

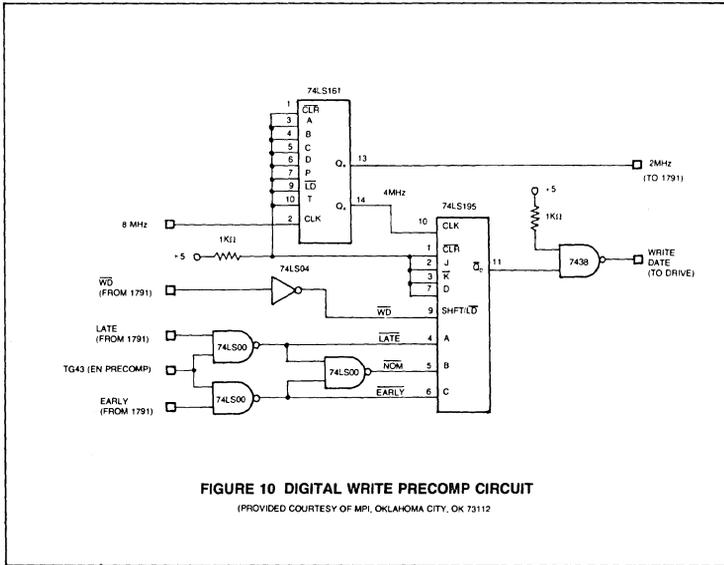
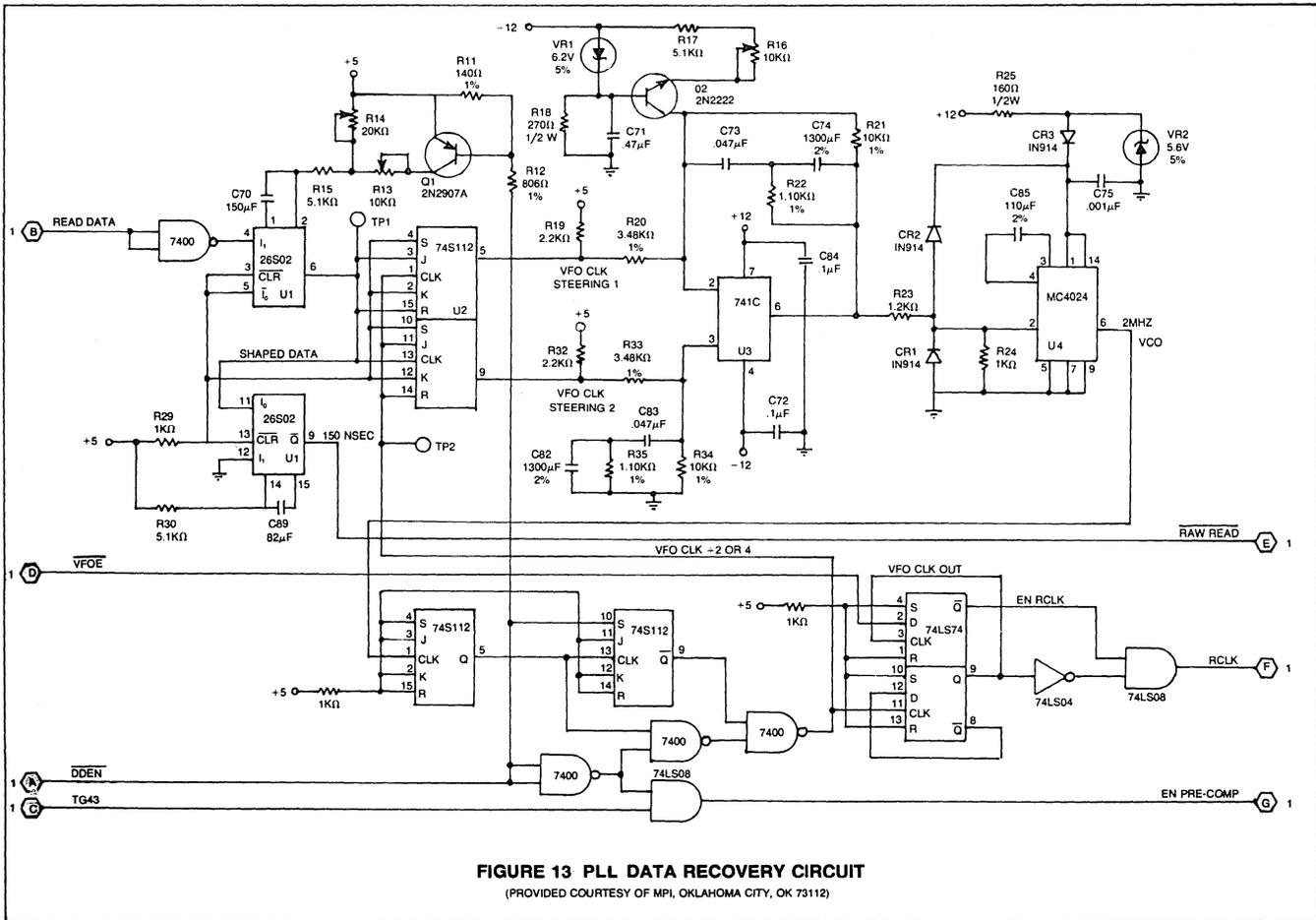


FIGURE 10 DIGITAL WRITE PRECOMP CIRCUIT

(PROVIDED COURTESY OF MPI, OKLAHOMA CITY, OK 73112)



COMMAND SUMMARY

		BITS							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r ₁	r ₀
I	Seek	0	0	0	1	h	V	r ₁	r ₀
I	Step	0	0	1	u	h	V	r ₁	r ₀
I	Step In	0	1	0	u	h	V	r ₁	r ₀
I	Step Out	0	1	1	u	h	V	r ₁	r ₀
II	Read Sector	1	0	0	m	S	E	C	0
II	Write Sector	1	0	1	m	S	E	C	a ₀
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrupt	1	1	0	1	l ₃	l ₂	l ₁	l ₀

Note: Bits shown in TRUE form.

STEPPING RATES

CLK	2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
DDEN	0	1	0	1	X	X
R ₁ , R ₀	TEST=1	TEST=1	TEST=1	TEST=1	TEST=0	TEST=0
0 0	3 ms	3 ms	6 ms	6 ms	184 μs	368 μs
0 1	6 ms	6 ms	12 ms	12 ms	190 μs	380 μs
1 0	10 ms	10 ms	20 ms	20 ms	198 μs	396 μs
1 1	15 ms	15 ms	30 ms	30 ms	208 μs	416 μs

FLAG SUMMARY

TYPE I COMMANDS

h = Head Load Flag (Bit 3)

- h = 1, Load head at beginning
- h = 0, Unload head at beginning

V = Verify flag (Bit 2)

- V = 1, Verify on destination track
- V = 0, No verify

r₁, r₀ = Stepping motor rate (Bits 1-0)

Refer to Table 1 for rate summary

u = Update flag (Bit 4)

- u = 1, Update Track register
- u = 0, No update

FLAG SUMMARY

TYPE II & III COMMANDS

m = Multiple Record flag (Bit 4)

- m = 0, Single Record
- m = 1, Multiple Records

a₀ = Data Address Mark (Bit 0)

- a₀ = 0, FB (Data Mark)
- a₀ = 1, F8 (Deleted Data Mark)

E = 15 ms Delay (2MHz)

- E = 1, 15 ms delay
- E = 0, no 15 ms delay

S = Side Select Flat

- S = 0, Compare for Side 0
- S = 1, Compare for Side 1

C = Side Compare Flag

- C = 0, disable side select compare
- C = 1, enable side select compare

FLAG SUMMARY

TYPE IV COMMAND

li = Interrupt Condition flags (Bits 3-0)

- l₀ = 1, Not-Ready to Ready Transition
- l₁ = 1, Ready to Not-Ready Transition
- l₂ = 1, Index Pulse
- l₃ = 1, Immediate Interrupt
- l₃ - l₀ = 0, Terminate with no Interrupt

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WESTERN DIGITAL

C O R P O R A T I O N

FD1771-01 Floppy Disk Formatter/Controller

FEATURES

- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- READ MODE
Single/Multiple Sector Write with Automatic Sector Search or Entire Track Read
Selectable 128 Byte or Variable Length Sector
- WRITE MODE
Single/Multiple Sector Write with Automatic Sector Search
Entire Track Write for Diskette Formatting
- PROGRAMMABLE CONTROLS
Selectable Track-to-Track Stepping Time
Selectable Head Settling and Head Engage Times
Selectable Three Phase or Step and Direction and Head Positioning Motor Controls

SYSTEM COMPATIBILITY

- Double Buffering of Data 8-Bit Bi-Directional Bus for Data, Control and Status
- DMA or Programmed Data Transfers
- All Inputs and Outputs are TTL Compatible

APPLICATIONS

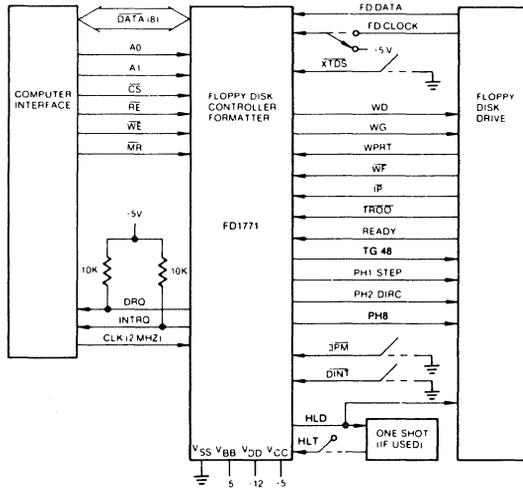
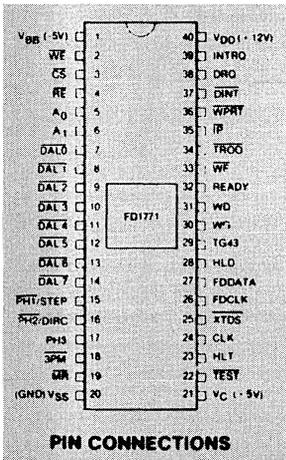
- FLOPPY DISK DRIVE INTERFACE
- SINGLE OR MULTIPLE DRIVE CONTROLLER/FORMATTER
- NEW MINI-FLOPPY CONTROLLER

GENERAL DESCRIPTION

The FD1771 is a MOS/LSI device that performs the functions of a Floppy Disk Controller/Formatter. The device is designed to be included in the disk drive electronics, and contains a flexible interface

JUNE, 1980

DISC-02-2



FD1771 SYSTEM BLOCK DIAGRAM

organization that accommodates the interface signals from most drive manufacturers. The FD1771 is compatible with the IBM 3740 data entry system format.

The processor interface consists of an 8-bit bidirectional bus for data, status, and control word

transfers. The FD1771 is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD1771 is fabricated in N-channel Silicon Gate MOS technology and is TTL compatible on all inputs and outputs. The A and B suffixes are for ceramic and plastic packages, respectively.

PIN OUTS

Pin No.	Pin Name	Symbol	Function																				
1	Power Supplies	V_{BB}/NC	-5V																				
19	MASTER RESET	\overline{MR}	A logic low on this input resets the device and loads "03" into the command register. The Not Ready (Status bit 7) is reset during \overline{MR} ACTIVE. When \overline{MR} is brought to a logic high, a Restore Command is executed, regardless of the state of the Ready signal from the drive.																				
20		V_{SS}	Ground																				
21		V_{CC}	+5V																				
40		V_{DD}	+12V																				
Computer Interface																							
2	$\overline{WRITE\ ENABLE}$	\overline{WE}	A logic low on this input gates data on the DAL into the selected register when \overline{CS} is low.																				
3	$\overline{CHIP\ SELECT}$	\overline{CS}	A logic low on this input selects the chip and enables computer communication with the device.																				
4	$\overline{READ\ ENABLE}$	\overline{RE}	A logic low on this input controls the placement of data from a selected register on the DAL when \overline{CS} is low.																				
5, 6	REGISTER SELECT LINES	A_0, A_1	These inputs select the register to receive/transfer data on the DAL lines under \overline{RE} and \overline{WE} control: <table border="0"> <tr> <td>A_1</td> <td>A_0</td> <td>\overline{RE}</td> <td>\overline{WE}</td> </tr> <tr> <td>0</td> <td>0</td> <td>Status Register</td> <td>Command Register</td> </tr> <tr> <td>0</td> <td>1</td> <td>Track Register</td> <td>Track Register</td> </tr> <tr> <td>1</td> <td>0</td> <td>Sector Register</td> <td>Sector Register</td> </tr> <tr> <td>1</td> <td>1</td> <td>Data Register</td> <td>Data Register</td> </tr> </table>	A_1	A_0	\overline{RE}	\overline{WE}	0	0	Status Register	Command Register	0	1	Track Register	Track Register	1	0	Sector Register	Sector Register	1	1	Data Register	Data Register
A_1	A_0	\overline{RE}	\overline{WE}																				
0	0	Status Register	Command Register																				
0	1	Track Register	Track Register																				
1	0	Sector Register	Sector Register																				
1	1	Data Register	Data Register																				
7-14	$\overline{DATA\ ACCESS\ LINES}$	$\overline{DAL0-DAL7}$	Eight bit inverted bidirectional bus used for transfer of data, control, and status. This bus is a receiver enabled by \overline{WE} or a transmitter enabled by \overline{RE} .																				
24	CLOCK	CLK	This input requires a free-running 2 MHz \pm 1% square wave clock for internal timing reference.																				
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operation, respectively. Use 10K pull-up resistor to +5.																				
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion or termination of any operation and is reset when a new command is loaded into the command register. Use 10K pull-up resistor to +5.																				
Floppy Disk Interface:																							
15	Phase 1/Step	$\overline{PH1}/STEP$	If the $\overline{3PM}$ input is a logic low the three-phase motor control is selected and $\overline{PH1}$, $\overline{PH2}$, and $\overline{PH3}$ outputs																				

N 20-Cont'd

Pin No.	Pin Name	Symbol	Function
16	Phase 2/Direction	$\overline{\text{PH2}}/\text{DIRC}$	form a one active low signal out of three. $\overline{\text{PH1}}$ is active low after MR. If the 3PM input is a logic high the step and direction motor control is selected. The step output contains a 4 usec high signal for each step and the direction output is active high when stepping in; active low when stepping out.
17	Phase 3	PH3	
18	3-Phase Motor Select	3PM	
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	This input is used for testing purposes only and should be tied to +5V or left open by the user.
23	HEAD LOAD TIMING	HLT	The HLT input is sampled after 10 ms. When a logic high is sampled on the HLT input the head is assumed to be engaged.
25	$\overline{\text{EXTERNAL DATA SEPARATION}}$	$\overline{\text{XTDS}}$	A logic low on this input selects external data separation. A logic high or open selects the internal data separator.
26	FLOPPY DISK CLOCK (External Separation)	FDCLOCK	This input receives the externally separated clock when $\overline{\text{XTDS}} = 0$. If $\overline{\text{XTDS}} = 1$, this input should be tied to a logic high.
27	FLOPPY DISK DATA	FDDATA	This input receives the raw read disk data if $\overline{\text{XTDS}} = 1$, or the externally separated data if $\overline{\text{XTDS}} = 0$.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	Track Greater than 43	TG43	This output informs the drive that the Read-Write head is positioned between tracks 44-76. This output is valid only during Read and Write commands.
30	WRITE GATE	WG	This output is made valid when writing is to be performed on the diskette.
31	WRITE DATA	WD	This output contains both clock and data bits of 500 ns duration.
32	Ready	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low, the Read or Write operation is not performed and an interrupt is generated. A Seek operation is performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{\text{WRITE FAULT}}$	$\overline{\text{WF}}$	This input detects wiring faults indications from the drive. When $\text{WG} = 1$ and $\overline{\text{WF}}$ goes low, the current Write command is terminated and the Write Fault status bit is set. The $\overline{\text{WF}}$ input should be made inactive (high) when WG becomes inactive.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the FD1771 that the Read-Write head is positioned over Track 00 when a logic low.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	Input, when low for a minimum of 10 usec, informs the FD1771 when an index mark is encountered on the diskette.
36	$\overline{\text{WRITE PROTECT}}$	$\overline{\text{WPRT}}$	This input is sampled whenever a Write command is received. A logic low terminates the command and sets the Write Protect status bit.
37	$\overline{\text{DISK INITIALIZATION}}$	$\overline{\text{DINT}}$	The input is sampled whenever a Write Track command is received. If $\overline{\text{DINT}} = 0$, the operation is terminated and the Write Protect status bit is set.

ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated on page 4. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register: This 8-bit register assembles serial data from the Read Data input (FDDATA) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register: This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command, the Data Register holds the address of the desired Track position. This register can be loaded from the DAL and gated onto the DAL under processor control.

Track Register: This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be

loaded from or transferred to the DAL. This Register should not be loaded when this device is busy.

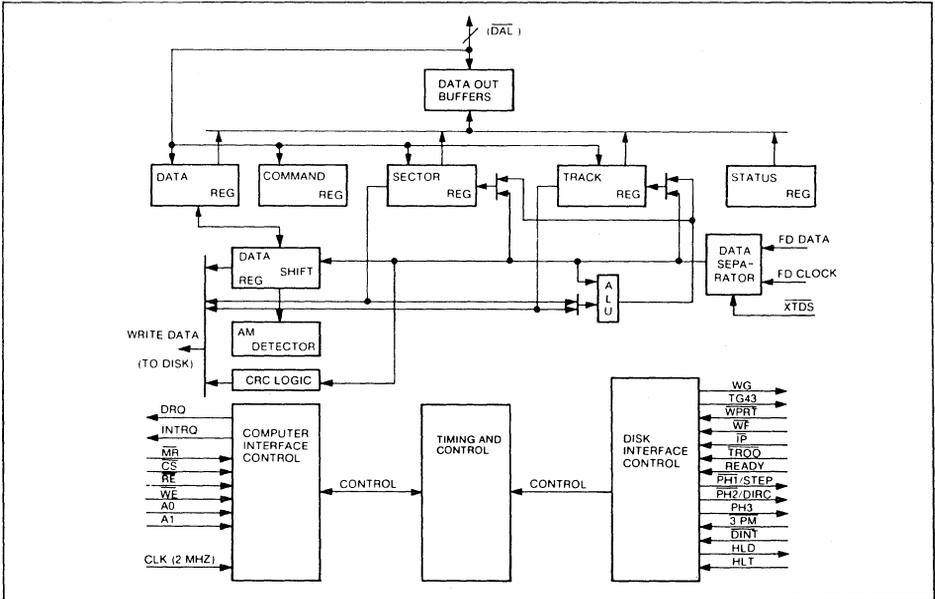
Sector Register (SR): This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR): This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the execution of the current command is to be overridden. This latter action results in an interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR): This 8-bit register holds device Status information. The meaning of the Status bits are a function of the contents of the Command Register. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic: This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.



FD1771 BLOCK DIAGRAM

20-01015

Arithmetic/Logic Unit (ALU): The ALU is a serial comparator, incrementer, and decremter and is used for register modification and comparisons with the disk recorded ID field.

AM Detector: The Address Mark detector is used to detect ID, Data, and Index address marks during Read and Write operations.

Timing and Control: All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from a 2.0 MHz external crystal clock.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the FD1771. The DAL are three-state buffers that are enabled as output drivers when Chip Select (CS) and Read Enable (RE) are active (low logic state) or act as input receivers when CS and Write Enable (WE) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and CS is made low. The least-significant address bits A1 and A0, combined with the signals RE during a Read operation or WE during a Write operation are interpreted as selecting the following registers:

A1-A0	READ (\overline{RE})	WRITE (\overline{WE})
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD1771 and the Processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded

at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

The Lost Data bit and certain other bits in the Status Register will activate the interrupt request (INTRQ). The interrupt line is also activated with normal completion or abnormal termination of all controller operations. The INTRQ signal remains active until reset by reading the Status Register to the processor or by the loading of the Command Register. In addition, the INTRQ is generated if a Force Interrupt command condition is met.

FLOPPY DISK INTERFACE

The Floppy Disk interface consists of head positioning controls, write gate controls, and data transfers. A 2.0 MHz \pm 1% square wave clock is required at the CLK input for internal control timing (may be 1.0 MHz for mini floppy).

HEAD POSITIONING

Four commands cause positioning of the Read-Write head (see Command Section). The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step, an additional 10 milliseconds of head settling time takes place. The four programmable stepping rates are tabulated below.

The rates (shown in Table 1) can be applied to a Three-Phase Motor or a Step-Direction Motor through the device interface. When the $\overline{3PM}$ input is connected to ground, the device operates with a three-phase motor control interface, with one active low signal per phase on the three output signals PH1, PH2, and PH3. The stepping sequence, when stepping in, is Phases 1-2-3-1, and when stepping out, Phases 1-3-2-1. Phase 1 is active low after Master Reset. Note: PH3 needs an inverter if used.

The Step-Direction Motor Control interface is activated by leaving input $\overline{3PM}$ open or connecting it to +5V. The Phase 1 pin PH1 becomes a Step pulse of 4 microseconds width. The Phase 2 pin PH2 becomes a direction control with a high voltage on this pin indicating a Step In, and a low voltage indicating a Step Out. The Direction output is valid a minimum of 24 μ s prior to the activation of the Step pulse.

When a Seek, Step or Restore command is executed, an optional verification of Read-Write head position can be performed by setting bit 2 in the command word to a logic 1. The verification operation begins at the end of the 10 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete. If track comparison is not



made but the CRC checks, an interrupt is generated, the Seek Error status (Bit 4) is set and the Busy status bit is reset.

Table 1 STEPPING RATES

r ₁	r ₀	1771-X1 CLK=2 MHz TEST=1	1771-X1 CLK=1 MHz TEST=1	1771 or -X1 CLK=2 MHz TEST=0	1771 or -X1 CLK=1 MHz TEST=0
0	0	6ms	12ms	Approx. 400us*	Approx. 600us*
0	1	6ms	12ms		
1	0	10ms	20ms		
1	1	20ms	40ms		

*For exact times consult WDC.

The Head Load (HLD) output controls the movement of the read/write head against the disk for data recording or retrieval. It is activated at the beginning of a Read, Write (E Flag On) or Verify operation, or a Seek or Step operation with the head load bit, h, a logic one remains activated until the third index pulse following the last operation which uses the read/write head. Reading or Writing does not occur until a minimum of 10 msec delay after the HLD signal is made active. If executing the type 2 commands with the E flag off, there is no 10 msec delay and the head is assumed to be engaged. The delay is determined by sampling of the Head Load Timing (HLT) input after 10 msec. A high state input, generated from the Head Load output transition and delayed externally, identifies engagement of the head against the disk. In the Seek and Step commands, the head is loaded at the start of the command execution when the h bit is a logic one. In a verify command the head is loaded after stepping to the destination track on the disk whenever the h bit is a logic zero.

DISK READ OPERATION

The 2.0 MHz external clock provided to the device is internally divided by 4 to form the 500 kHz clock rate for data transfer. When reading data from a diskette this divider is synchronized to transitions of the Read Data (FDDATA) input. When a transition does not occur on the 500 kHz clock active state, the clock divider circuit injects a clock to maintain a continuous 500 kHz data clock. The 500 kHz data clock is further divided by 2 internally to separate the clock and information bits. The divider is phased to the information by the detection of the address mark.

In the internal data read and separation mode the Read Data input toggles from one state to the opposite state for each logic one bit of clock or information. This signal can be derived from the amplified, differentiated, and sliced Read Head signal, or by the output of a flip-flop toggling on the Read Data pulses. This input is sampled by the 2 MHz clock to detect transitions.

The chip can also operate on externally separated data, as supplied by methods such as Phase Lock loop, One Shots, or variable frequency oscillators. This is accomplished by grounding the External Data Separator ($\overline{\text{XTDS}}$) INPUT. When the Read Data input makes a high-to-low transition, the information input to the FDDATA line is clocked into the Data Shift Register. The assembled 8-bit data from the Data Shift Register are then transferred to the Data Register.

The normal sector length for read or Write operations with the IBM 3740 format is 128 bytes. This format or binary multiples of 128 bytes will be adopted by setting a logic 1 in Bit 3 of the Read and Write commands. Additionally, a variable sector length feature is provided which allows an indicator recorded in the ID Field to control the length of the sector. Variable sector lengths can be read or written in Read or Write commands, respectively, by setting a logic 0 in Bit 3 of the command word. The sector length indicator specifies the number of 16 byte groups or $16 \times N$, where N is equal to 1 to 256 groups. An indicator of all zeroes is interpreted as 256 sixteen byte groups.

DISK WRITE OPERATION

After data is loaded from the processor into the Data Register, and is transferred to the Data Shift Register, data will be shifted serially through the Write Data (WD) output. Interlaced with each bit of data is a positive clock pulse of 0.5 μ sec duration. This signal may be used to externally toggle a flip-flop to control the direction of Write Current flow.

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing, the first data byte must be loaded into the Data Register in response to a Data Request from the FD1771 before the Write Gate signal can be activated.

Writing is inhibited when the Write Protect input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD1771 terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The Write Fault input should be made inactive when the Write Gate output becomes inactive.

Whenever a Read or Write command is received the FD1771 samples the READY input. If this input is logic low the command is not executed and an interrupt is generated. The Seek or Step commands are performed regardless of the state of the READY input.

COMMAND DESCRIPTION

The FD1771 will accept and execute eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault-free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 2.

TYPE 1 COMMANDS

The Type 1 Commands include the RESTORE, SEEK, STEP, STEP-IN, and STEP-OUT commands. Each of the Type 1 Commands contain a rate field (r_0r_1), which determines the stepping motor rate as defined in Table 1, page 4.

The Type 1 Commands contain a head load flag (h) which determines if the head is to be loaded at the

Table 2. COMMAND SUMMARY

TYPE	COMMAND	BITS							
		7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Command	1	0	0	m	b	E	0	0
II	Write Command	1	0	1	m	b	E	a_1a_0	
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	1	0	\bar{s}
III	Write Track	1	1	1	1	0	1	0	0
IV	Force Interrupt	1	1	0	1	l_3	l_2	l_1	l_4

Note: Bits shown in TRUE form.

Table 3 FLAG SUMMARY

TYPE I
<u>h = Head Load flag (Bit 3)</u> h = 1, Load head at beginning h = 0, Do not load head at beginning
<u>V = Verify flag (Bit 2)</u> V = 1, Verify on last track V = 0, No verify
<u>r_1r_0 = Stepping motor rate (Bits 1-0)</u> Refer to Table 1 for rate summary
<u>u = Update flag (Bit 4)</u> u = 1, Update Track register u = 0, No update

Table 4 FLAG SUMMARY

TYPE II
<u>m = Multiple Record flag (Bit 4)</u> m=0, Single Record m=1, Multiple Records
<u>b = Block length flag (Bit 3)</u> b=1, IBM format (128 to 1024 bytes) b=0, Non-IBM format (16 to 4096 bytes)
<u>a_1a_0 = Data Address Mark (Bits 1-0)</u> a_1a_0 = 00, FB (Data Mark) a_1a_0 = 01, FA (User defined) a_1a_0 = 10, F9 (User defined) a_1a_0 = 11, F8 (Deleted Data Mark)

Table 5 FLAG SUMMARY

TYPE III
<u>s = Synchronize flag (Bit 0)</u> \bar{s} =0, Synchronize to AM \bar{s} =1, Do Not Synchronize to AM
TYPE IV
<u>li = Interrupt Condition flags (Bits 3-0)</u> l_0 =1, Not Ready to Ready Transition l_1 =1, Ready to Not Ready Transition l_2 =1, Index Pulse l_3 =1, Immediate interrupt
<u>E = Enable HLD and 10 msec Delay</u> E=1, Enable HLD, HLT and 10 msec Delay E=0, Head is assumed Engaged and there is no 10 msec Delay

beginning of the command. If h=1, the head is loaded at the beginning of the command (HLD output is made active). If h=0, HLD is deactivated. Once the head is loaded, the head will remain engaged until the FD1771 receives a command that specifically disengages the head. If the FD1771 does not receive any commands after two revolutions of the disk, the head will be automatically disengaged (HLD made inactive). The Head Load Timing Input is sampled after a 10 ms delay, when reading or writing on the disk is to occur.

The Type 1 Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V=1, a verification is performed; if V=0, no verification is performed.

During verification, the head is loaded and after an internal 10 ms delay, the HLT input is sampled. When

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HLT is active (logic true), the first encountered ID field is read off the disk. The track address of the ID Field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the BUSY status bit is reset. If there is not a match but there is valid ID CRC, an interrupt is generated, the Seek Error status bit (Status Bit 4) is set and the BUSY status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status Bit 3), and the next encountered ID Field is read from the disk for the verification operation. If an ID Field with a valid CRC cannot be found after two revolutions of the disk, the FD1771 terminates the operation and sends an interrupt (INTRQ).

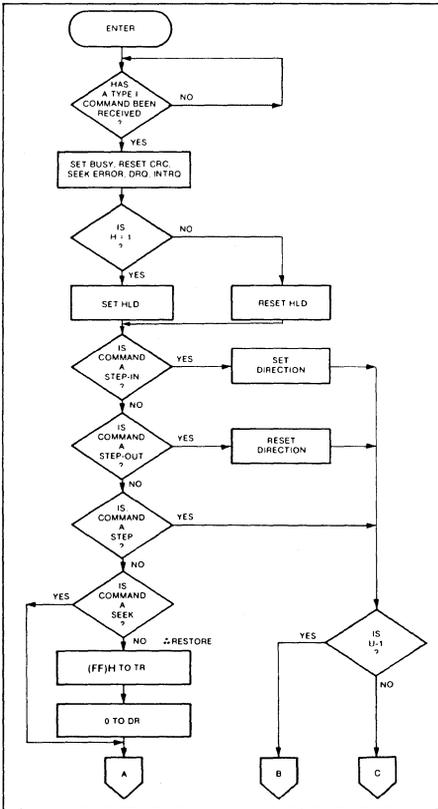
The STEP, STEP-IN, and STEP-OUT commands contain an UPDATE flag (U). When U=1, the track register is updated by one for each step. When U=0, the track register is not updated.

RESTORE (SEEK TRACK 0)

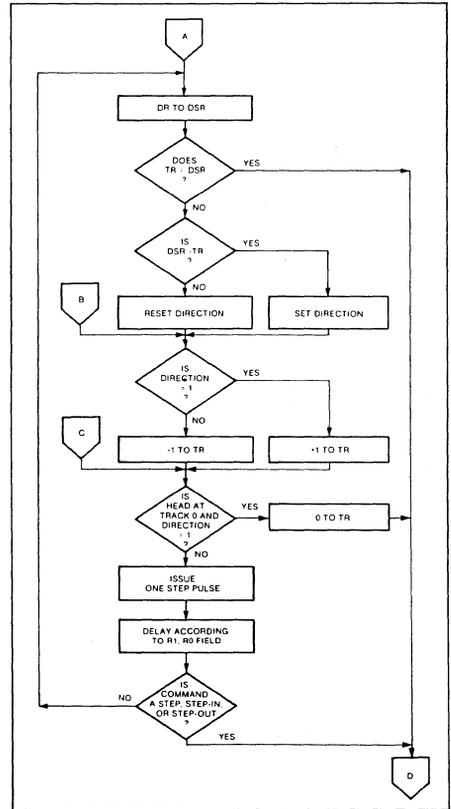
Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 17) at a rate specified by the r_{10} field are issued until the $\overline{TR00}$ input is activated. At this time the TR is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the FD1771 terminates operation, interrupts, and sets the Seek error status bit. Note that the RESTORE command is executed when \overline{MR} goes from an active to an inactive state. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command.

SEEK

This command assumes that the Track Register contains the track number of the current position of the



TYPE I COMMAND FLOW



TYPE I COMMAND FLOW

Read-Write head and the Data Register contains the desired track number. The FD1771 will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the data register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP

Upon receipt of this command, the FD1771 issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_{1r0} field, a verification takes place if the V flag is on. If the u flag is on, the TR is updated. The h bit allows the head to be loaded at the start of the command. An

interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the FD1771 issues one stepping pulse in the direction towards track 76. If the u flag is on, the Track Register is incremented by one. After a delay determined by the r_{1r0} field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the FD1771 issues one stepping pulse in the direction towards track 0. If the u flag is on, the TR is decremented by one. After a delay determined by the r_{1r0} field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

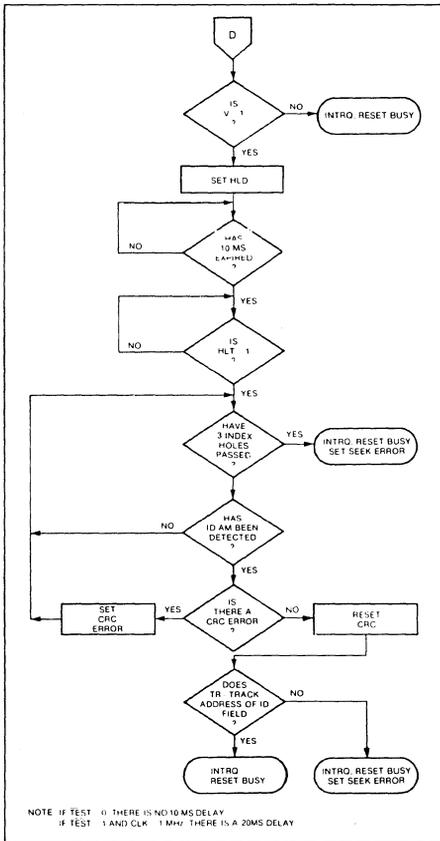
TYPE II COMMANDS

The Type II Commands include the Read Sector(s) and Write Sector(s) commands. Prior to loading the Type II command into the COMMAND REGISTER, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the Busy status bit is set. If the E flag=1 (this is the normal case), HLD is made active and HLT is sampled after a 10 msec delay. If the E flag is 0, the head is assumed to be engaged and there is no 10 msec delay. The ID field and the Data Field format are shown below.

When an ID field is located on the disk, the FD1771 compares the track number of the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending on the command. The FD1771 must find an ID field with a track number, Sector number, and CRC within two revolutions of the disk; otherwise, the Record Not Found status bit is set (Status bit 3) and the command is terminated with an interrupt.

Each of the Type II Commands contain a (b) flag which in conjunction with the sector length field contents of the ID determines the length (number of characters) of the Data field.

For IBM 3740 compatibility, the b flag should equal 1. The numbers of bytes in the data field (sector) is then 128×2^n where $n = 0, 1, 2, 3$.



NOTE: IF TEST 0: THERE IS NO 10 MS DELAY
 IF TEST 1 AND CLK 1 MHz: THERE IS A 20MS DELAY

TYPE I COMMAND FLOW

GAP	ID AM	TRACK NUMBER	ZERO	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP	DATA AM	DATA FIELD	CRC 1	CRC 2
ID FIELD									DATA FIELD			

IDAM ID Address Mark -- DATA (FE)₁₆ CLK (C7)₁₆

Data AM Data Address Mark -- DATA (F8, F9, FA, or FB). CLK (C7)₁₆

For b 1

Sector Length Field (Hex)	Number of Bytes in Sector (Decimal)
00	128
01	256
02	512
03	1024

When the b flag equals zero, the sector length field (n) multiplied by 16 determines the number of bytes in the sector or data field as shown below.

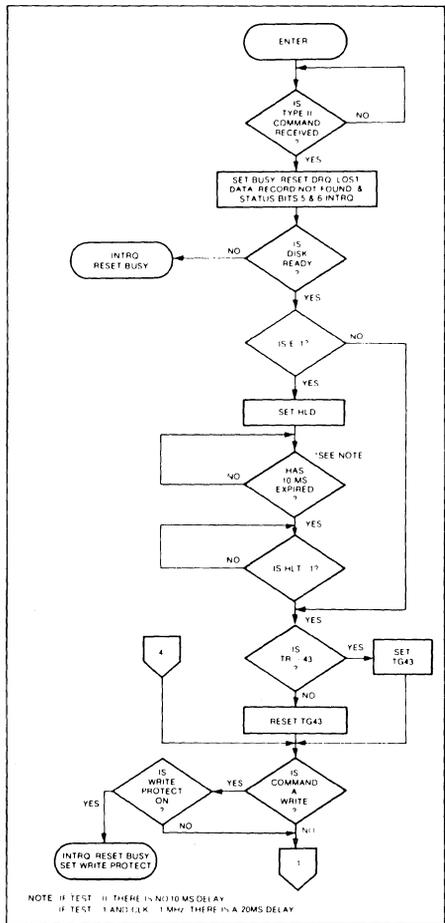
For b 0

Sector Length Field (Hex)	Number of Bytes in Sector (Decimal)
01	16
02	32
03	48
04	64
.	.
.	.
.	.
FF	4080
00	4096

Each of the Type II commands also contain a (m) flag which determines if the multiple records (sectors) are to be read or written, depending upon the command. If m=0 a single sector is read or written and an interrupt is generated at the completion of the command. If m=1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FD1771 will continue to read or write multiple records and update the sector register until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the command register, which terminated the command and generates an interrupt.

READ COMMAND

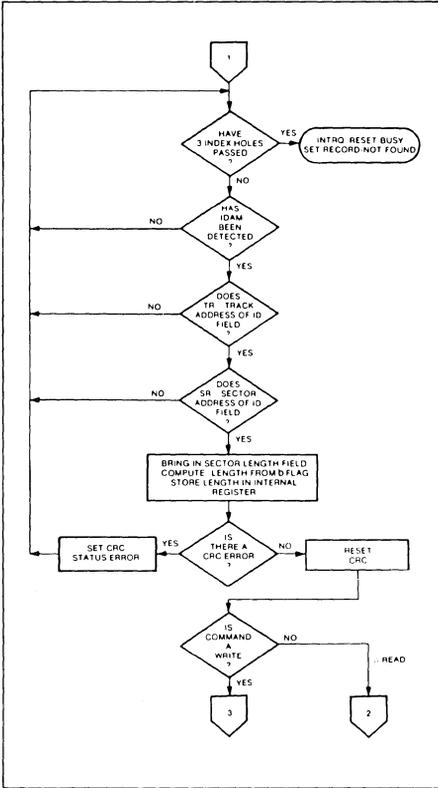
Upon receipt of the Read command, the head is loaded, the BUSY status bit set, and when an ID field is encountered that has the correct track number, correct sector number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 28 bytes of the correct field; if not, the Record Not Found status bit is set and the operation is terminated. When



TYPE II COMMAND FLOW

the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the computer has not read the previous contents of the DR before a new character is transferred that character is lost and the

SECTION 2

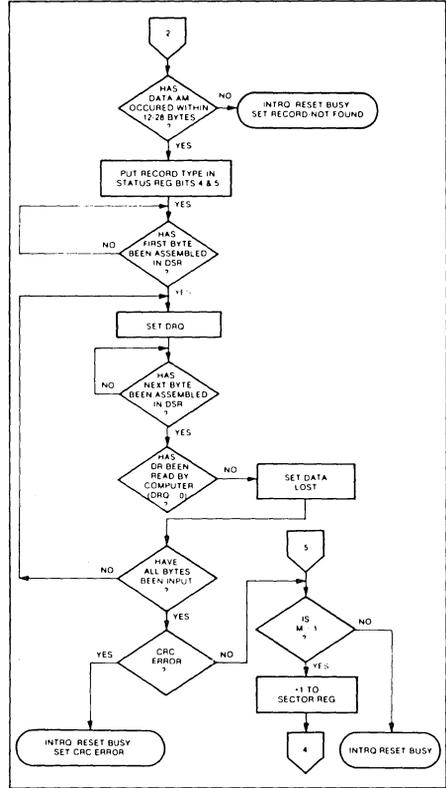


TYPE II COMMAND FLOW

Lost Data status bit is set. This sequence continues until the complete data field has been input to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bits 5 and 6) as shown below.

Status Bit 5	Status Bit 6	Data AM (Hex)
0	0	FB
0	1	FA
1	0	F9
1	1	F8



TYPE II COMMAND FLOW

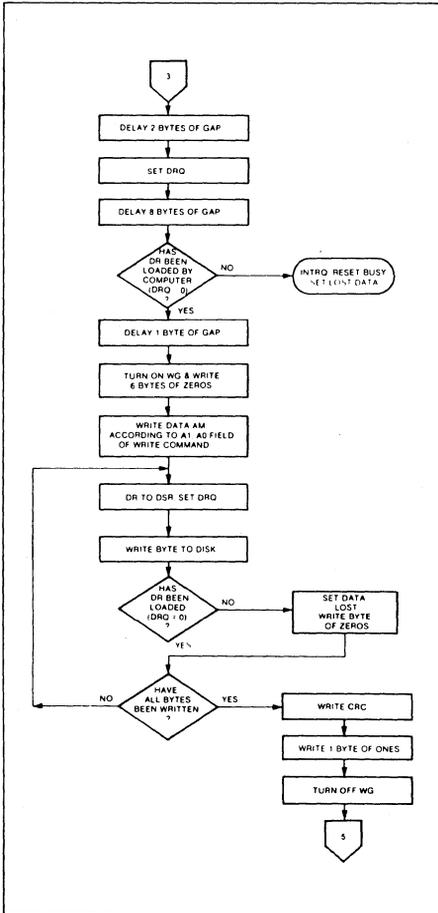
WRITE COMMAND

Upon receipt of the Write command, the head is loaded (HLD active) and the BUSY status bit is set. When an ID field is encountered that has the correct track number, correct sector number, and correct CRC, a DRQ is generated. The FD1771 counts off 11 bytes from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the $a_1 a_0$ field of the command as shown on next page.

The FD1771 then writes the data field and generates DRQs to the computer. If the DRQ is not serviced in

a ₁	a ₀	Data Mark (Hex)	Clock Mark (Hex)
0	0	FB	C7
0	1	FA	C7
1	0	F9	C7
1	1	F8	C7

time for continuous writing the Lost Data status bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte gap of logic ones. The WG output is then deactivated.



TYPE II COMMAND FLOW

TYPE III COMMANDS

READ Address

Upon receipt of the Read Address command, the head is loaded and the BUSY Status bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below.

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

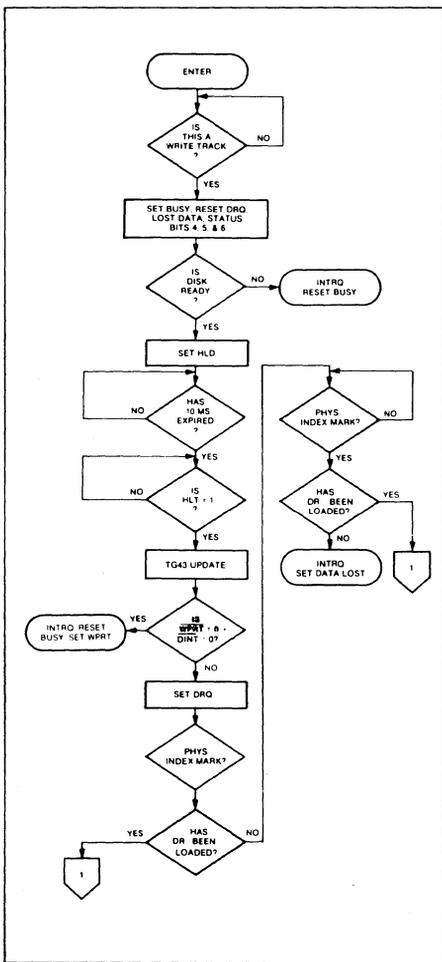
Although the CRC characters are transferred to the computer, the FD1771 checks for validity and the CRC error status bit is set if there is a CRC error. The Sector Address of the ID field is written into the Sector Register. At the end of the operation an interrupt is generated and the BUSY Status is reset.

READ TRACK

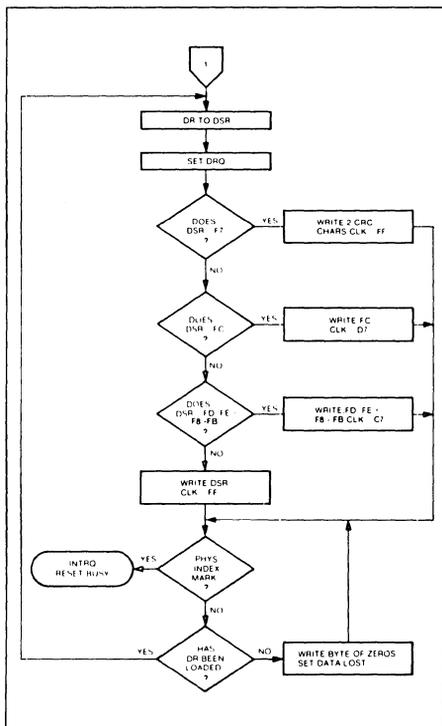
Upon receipt of the Read Track command, the head is loaded and the BUSY status bit is set. Reading starts with the leading edge of the first encountered index mark and continues until the next index pulse. As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. If bit 0(S) of the command is a 0, the accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated.

WRITE TRACK

Upon receipt of the Write Track command, the head is loaded and the BUSY status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data status bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR.



TYPE III COMMAND WRITE TRACK



TYPE III COMMAND WRITE TRACK

The Write Track Command will not execute if the DINT input is grounded; instead, the Write Protect status bit is set and the interrupt is activated. Note that one F7 pattern generates two CRC characters.

TYPE IV COMMAND

Force Interrupt

This command can be loaded into the command register at any time. If there is a current command under execution (BUSY status bit set), the command will be terminated and an interrupt will be generated when the condition specified in the I₀ through I₃ field is detected. The interrupt conditions are shown below:

- I₀ = Not-Ready-To-Ready Transition
- I₁ = Ready-To-Not-Ready Transition
- I₂ = Every Index Pulse
- I₃ = Immediate Interrupt (Requires reset, see Note)

NOTE: If I₀ - I₃ = 0, there is no interrupt generated but the current command is terminated and busy is reset. This is the only command that will clear the immediate interrupt.

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN (HEX)	INTERPRETATION	CLOCK MARK (HEX)
F7	Write CRC Character	FF
F8	Data Address Mark	C7
F9	Data Address Mark	C7
FA	Data Address Mark	C7
FB	Data Address Mark	C7
FC	Index Address Mark	D7
FD	Spare	
FE	ID Address Mark	C7

STATUS DESCRIPTION

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is

reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The format of the Status Register is shown below.

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 6.

Table 6 STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ	READ TRACK	WRITE	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	RECORD TYPE	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD ENGAGED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	ID NOT FOUND	RECORD NOT FOUND	0	RECORD NOT FOUND	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT	NAME	MEANING
S7	NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the READY input and logically "ored" with MR.
S6	PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of WRPT input.
S5	HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4	SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3	CRC ERROR	When set, there was one or more CRC errors encountered on an unsuccessful track verification operation. This bit is reset to 0 when updated.
S2	TRACK 00	When set, indicates Read-Write head is positioned to Track 0. This bit is an inverted copy of the TR00 input.
S1	INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the IP input.
S0	BUSY	When set, command is in progress. When reset, no command is in progress.

STATUS BITS FOR TYPE II AND III COMMANDS

BIT	NAME	MEANING
S7	NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the READY input and "ored" with MR. The TYPE II and III Commands will not execute unless the drive is ready.
S6	RECORD TYPE/WRITE PROTECT	On Read Record: It indicates the MSB of record-type code from data field address mark. On Read Track: Not Used. On any Write Track: It indicates a Write Protect. This bit is reset when updated.
S5	RECORD TYPE/WRITE FAULT	On Read Record: It indicates the LSB of record-type code from data field address mark. On Read Track: Not Used. On any Write Track: It indicates a Write Fault. This bit is reset when updated.
S4	RECORD NOT FOUND	When set, it indicates that the desired track and sector were not found. This bit is reset when updated.
S3	CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2	LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1	DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0	BUSY	When set, command is under execution. When reset, no command is under execution.

SECTION 2

FORMATTING THE DISK (Refer to section on Type III Commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA control with a large amount of memory. When operating under DMA with limited amount of memory, formatting is a more difficult task. This is because gaps as well as data must be provided at the computer interface.

Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command. Upon receipt of the Write Track command, the FD1771 raises the Data Request signal. At this point in time, the user loads the Data Register with desired data to be written on the disk. For every byte of information to be written on the disk, a Data Request is generated. This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the Data Register is written on the disk with a clock mark of (FF)₁₆. However, if the FD1771 detects a data pattern on F7 through FE in the Data

Register, this is interpreted as data address marks with missing clocks or CRC generation. For instance, an FE pattern will be interpreted as an ID address mark (DATA-FE, CLK-C7) and the CRC will be initialized. An F7 pattern will generate two CRC characters. As a consequence, the patterns F7 through FE must not appear in the gaps, data fields, or ID fields. Also, CRCs must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 formats with sector lengths of 128,256,512, or 1024 bytes, or may be formatted in non-IBM format with sector lengths of 16 to 4096 bytes in 16-byte increments. IBM 3740 at the present time only defines two formats. One format with 128 bytes/sector and the other with 256 bytes/sector. The next section deals with the IBM 3740 format with 128 bytes/sector followed by a section of non-IBM formats.

IBM 3740 Formats — 128 Bytes/Sector

The IBM format with 128 bytes/sector is depicted in the Track Format figure on the following page. In order to create this format, the user must issue the

Write Track command, and load the data register with the following values. For every byte to be written, there is one data request.

Number of Bytes	Hex Value of Byte Written
40	00 or FF
6	00
1	FC (Index Mark)
* 26	00 or FF
6	00
1	FE (ID Address Mark)
1	Track Number (0 through 4C)
1	00
1	Sector Number (1 through 1A)
1	00
1	F7 (two CRCs written)
11	00 or FF
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (two CRCs written)
27	00 or FF
247**	00 or FF

*Write bracketed field 26 times.

**Continue writing until FD1771 interrupts out. Approximately 247 bytes.

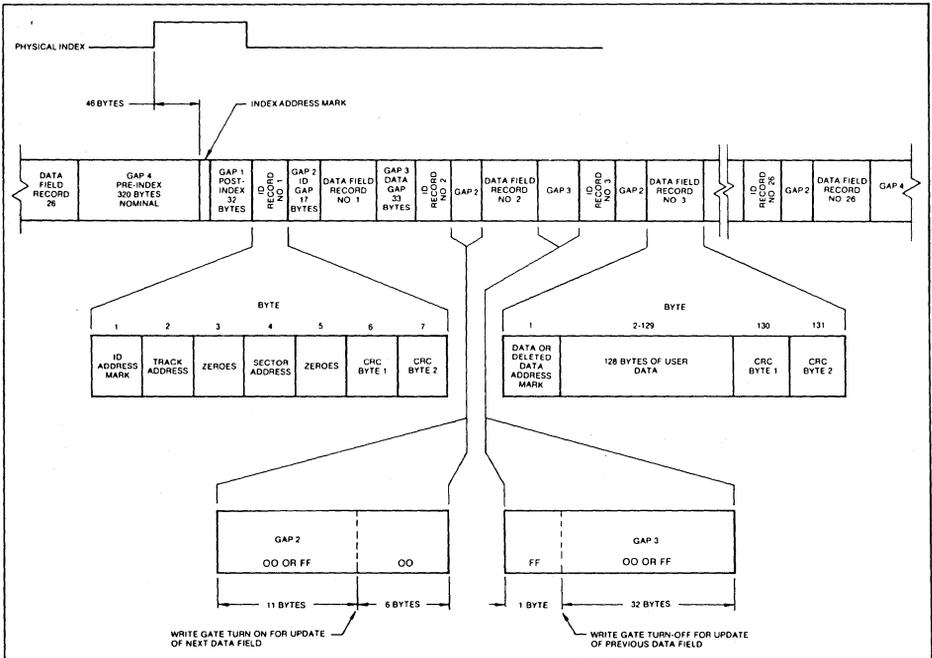
Non-IBM Formats

Non-IBM formats are very similar to the IBM formats except a different algorithm is used to ascertain the sector length from the sector length byte in the ID field. This permits a wide range of sector lengths from 16 to 4096 bytes. Refer to Section V, Type II commands with b flag equal to zero. Note that F7 through FE must not appear in the sector length byte of the ID field.

In formatting the FD1771, only two requirements regarding GAP sizes must be met. GAP 2 (i.e., the gap between the ID field and data field) must be 17 bytes of which the last 6 bytes must be zero and that every address mark be preceded by at least one byte of zeros. However, it is recommended that every GAP be at least 17 bytes long with 6 bytes of zeros. The FD1771 does not require the index address mark (i.e., DATA = FC, CLK = D7) and need not be present.

References:

- 1) IBM Diskette OEM Information GA21-9190-1.
- 2) SA900 IBM Compatibility Reference Manual — Shugart Associates.



TRACK FORMAT

ELECTRICAL CHARACTERISTICS

Maximum Ratings

V _{DD} with respect to V _{BB} (Ground)	+20 to -0.3V
Max Voltage to any input with respect to V _{BB}	+20 to -0.3V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C

OPERATING CHARACTERISTICS (DC)

T _A = 0°C to 70°C, V _{DD} = +12.0V ± .6V,
V _{BB} = -5.0 ± .5V, V _{SS} = 0V, V _{CC} = +5V ± .25V
I _{DD} = 10 ma Nominal, I _{CC} = 30 ma Nominal,
I _{BB} = 0.4 μA Nominal

Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
I _{LJ}	Input Leakage			10	μA	V _{IN} = V _{DD}
I _{LO}	Output Leakage			10	μA	V _{OUT} = V _{DD}
V _{IH}	Input High Voltage	2.6			V	
V _{IL}	Input Low Voltage (All Inputs)			0.8	V	
V _{OH}	Output High Voltage	2.8			V	I _O = -100 μA
V _{OL}	Output Low Voltage			0.45	V	I _O = 1.0 mA

TIMING CHARACTERISTICS

TA = 0°C to 70°C, V _{DD} = +12V ± .6V,
V _{BB} = -5V ± .25V, V _{SS} = 0V, V _{CC} = +5V ± .25V

NOTE: Timings are given for 2 MHz Clock. For those timings noted, values will double when chip is operated at 1 MHz. Use 1 MHz when using mini-floppy.

Read Operations

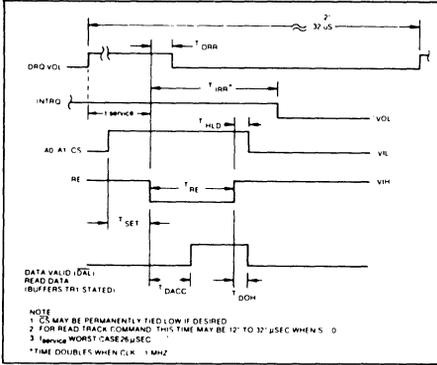
Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
TSET	Setup ADDR and CS to \overline{RE}	100			nsec	C _L = 25 pf
THLD	Hold ADDR and CS from \overline{RE}	10			nsec	
TRE	\overline{RE} Pulse Width	500			nsec	
TDRR	DRQ Reset from \overline{RE}			750	nsec	
TIRR	INTRQ Reset from \overline{RE}			3000	nsec	
TDACC	Data Access from \overline{RE}			450	nsec	
TDOH	Data Hold from \overline{RE}	50		150	nsec	C _L = 25 pf

Write Operations

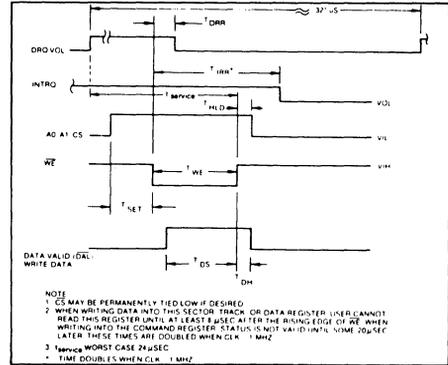
Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
TSET	Setup ADDR and CS to \overline{WE}	100			nsec	See Note
THLD	Hold ADDR and CS from \overline{WE}	10			nsec	
TWE	\overline{WE} Pulse Width	450	300		nsec	
TDRR	DRQ Reset from \overline{WE}			750	nsec	
TIRR	INTRQ Reset from \overline{WE}			3000	nsec	
TDS	Data Setup to \overline{WE}	250			nsec	
TDH	Data Hold from \overline{WE}	150			nsec	

External Data Separation (XTDS = 0)

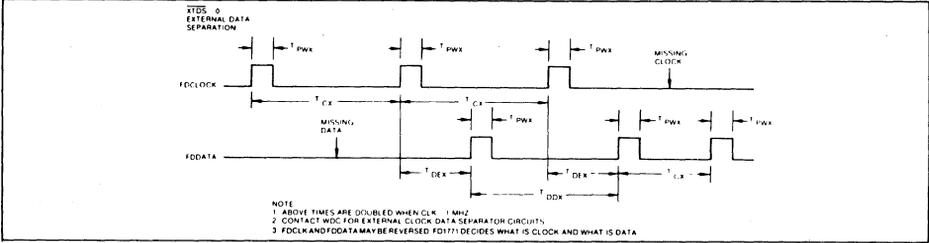
Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
TPWX	Pulse Width Read Data & Read Clock	150		350	nsec	
TCX	Clock Cycle External	2500			nsec	
TDEX	Data to Clock	500			nsec	
TDDX	Data to Data Cycle	2500			nsec	



READ ENABLE TIMING



WRITE ENABLE TIMING



READ TIMING (XTDS = 0)

Internal Data Separation (XTDS = 1)

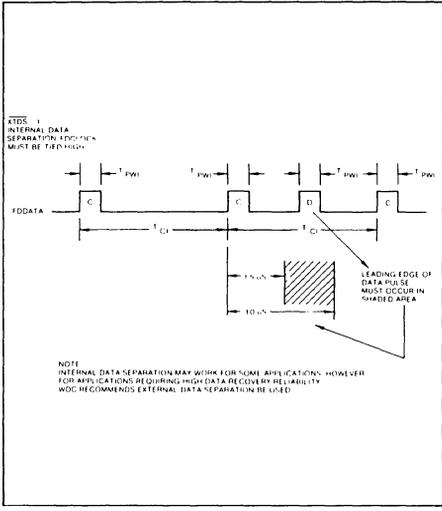
Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
TPWI	Pulse Width Data and Clock	150		1000	nsec	
TCl	Clock Cycle Internal	3500		5000	nsec	

Write Data Timing

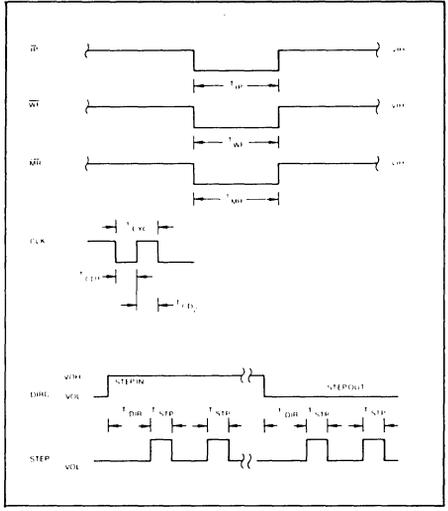
Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
TWGD	Write Gate to Data		1200		nsec	300 nsec ± CLK tolerance
TPWW	Pulse Width Write Data	500		600	nsec	
TCDW	Clock to Data		2000		nsec	± CLK tolerance
TCW	Clock Cycle Write		4000		nsec	± CLK tolerance
TWGH	Write Gate Hold to Data	0		100	nsec	

Miscellaneous Timing

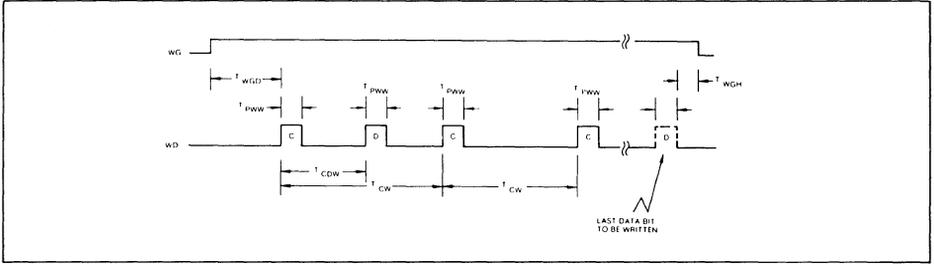
Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
TCD ₁	Clock Duty	175			nsec	These times doubled when CLK = 1 MHz
TCD ₂	Clock Duty	210			nsec	
TSTP	Step Pulse Output	3800		4200	nsec	
TDIR	Direct Setup to Step	24			usec	
TMR	Master Reset Pulse Width	10			usec	
TIP	Index Pulse Width	10			usec	
TWF	Write Fault Pulse Width	10			usec	



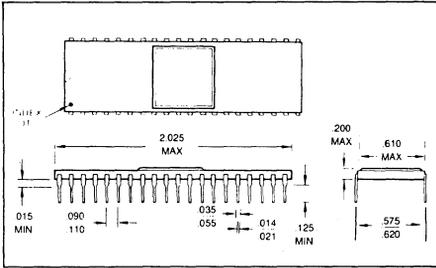
READ TIMING ($\overline{XTDS} = 1$)



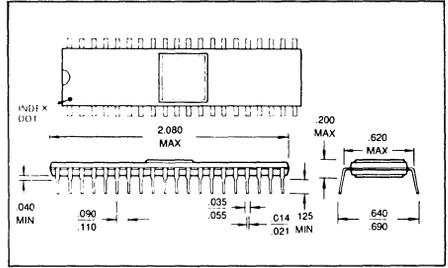
MISCELLANEOUS TIMING



WRITE DATA TIMING



FD1771A CERAMIC PACKAGE



FD1771B PLASTIC PACKAGE

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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WESTERN DIGITAL

C O R P O R A T I O N

1771-01 Application Notes

MAY 1980

SECTION 2

INTRODUCTION

The FD1771-01 Floppy Disk Formatter/Controller is a MOS/LSI device designed to ease the task of interfacing the 8" or 5¼" (mini-floppy) disk drive to a host processor. It is ideally suited for a wide range of microprocessors, providing an 8-bit bi-directional interface to the CPU for all control and data transfers. Requiring standard +12, ±5V power supplies, the 1771 is available in ceramic or plastic 40 pin dual-in-line packages.

The 1771 has been designed to be compatible with the IBM 3740 standard. This single-density Frequency Modulated (FM) recording technique, records a clock bit between a data bit serially on each track. Figure 1 illustrates how a HEX "D2" is recorded. Note that when the data bit to be written is zero, no pulse or flux transition is recorded. For the 8" drive, there are 77 tracks, with 26 sectors on each track. Each sector contains 128 bytes of data. Although there is no "standard" format for the mini-floppy, most manufacturers utilize either 35 or 40 tracks per side, with 16 sectors of 128 bytes each per track. Both the 8" and 5¼" formats must be soft-sectored, i.e., there are no physical holes to denote sector locations. The hard-sectored disk has been losing popularity, mainly due to the fact that the sector lengths cannot be increased.

Being soft-sector compatible, the 1771 must know where each sector begins on the track. This is performed by using Address Marks. These bytes are recorded on the disk with certain clock pulses missing, and are unique from all other data and gap bytes recorded on the track. Six distinct Address Marks can be used:

Description	Data	Clock Pattern
Index Address Mark	FC	D7
ID Address Mark	FE	C7
Data Address Mark	FB	C7
User defined	FA	C7
User Defined	F9	C7
Deleted Address Mark	F8	C7

The two "User Defined" Address Marks are unique to the 1771, and do not appear in the IBM 3740 standard. These Address Marks can be used to

define the type of data i.e., "object" or "text" data, alternate sector data, or any other purpose the user chooses.

PROCESSOR INTERFACE

The 1771 contains five internal registers that can be accessed via the 8-bit DAL lines by the CPU. These registers are used to control the movement of the head, read and write sectors, and perform all other functions at the drive. Regardless of the operation performed, it must be initiated through one or more of these registers. They are selected by a proper binary code on the A0, A1 lines in conjunction with the \overline{RE} and \overline{WE} lines when the device is selected. The registers and their addresses are:

CS	A ₁	A ₀	$\overline{RE} = 0$	$\overline{WE} = 0$
0	0	0	STATUS REG	COMMAND REG
0	0	1	TRACK REG	TRACK REG
0	1	0	SECTOR REG	SECTOR REG
0	1	1	DATA REG	DATA REG
1	X	X	Deselected	Deselected

Command Register: This is a write-only register used to send all commands to the 1771.

Status Register: This is a read-only register that must be read at the completion of every command to determine whether execution was successful. It may also be used to monitor command execution, and to sense when data is required by the drive for read or write operations.

Track Register: This R/W register holds the current position of the R/W head.

Sector Register: This R/W register holds the desired sector number for read and write commands.

Data Register: This R/W register contains the data to be read or written to a particular sector.

INTERRUPTS

There are two INTERRUPT lines for CPU use. These are the DRQ (Data Request) and INTRQ (Interrupt Request). These are active high, open drain outputs and require a pull-up resistor of 10K or greater to +5V. Both of these signals also appear in the status register as the Busy (INTRQ) and the data request (DRQ) bits. The user has the option of utilizing these hardware lines for system interrupts, or through

software by polling the status register. The choice is dependent upon the particular microprocessor and support hardware of the system.

INTRQ: This line is used to signify the completion of any command. It is reset low when a new command is loaded into the command register, or when the status register is read.

DRQ: This line is active high whenever the data register requires servicing. During a read command, it signifies that the data register contains a byte of data from the disk and may be read by the CPU. During a write command, it signifies that the data register is empty and may be loaded with the next byte to be written on the disk. The DRQ line is reset whenever the data register is read or written to. It is also reset when a new command is loaded into the command register, providing the new command is not a Forced Interrupt, and the 1771 is not busy (Busy Bit = 0).

WRITE SECTOR

With the use of the WRITE SECTOR command, the CPU can access any desired sector(s) in a track. Prior to loading this command, the R/W head of the drive must be positioned over the specific track. This can be first accomplished with the use of any of the Type I commands. Once positioned, the CPU must load the desired sector number into the sector register, then issue the command. The head will load, and the 1771 will begin searching for the correct ID field. If the correct sector and track is not found within 2 revolutions of the disk, the RECORD-NOT-FOUND bit will be set in the status register, and the command will be terminated. Once found, the 1771 will issue a DRQ in request of the first data byte to be written. Once the data register is loaded, the 1771 will issue a DRQ for each byte to be recorded, until the entire sector is written. For the 8" drive, the user must load the data register 24 microseconds after a DRQ is generated. Failure to meet this time will cause the lost data bit to be set, and a byte of zeros substituted and written on the disk.

READ SECTOR

The READ SECTOR command functions in much the same way as the WRITE SECTOR command. The sector register must again be loaded with the desired sector number, before the read command can be loaded. After the ID field has been found, the 1771 will begin generating DRQ's, with the data register being loaded with each byte of the sector field. For the 8" drive, the user must read the data register at least 26 microseconds after the DRQ is generated. Failure to meet this time will cause the lost data bit to be set in the status register, while the next assembled byte will overwrite the contents of the data register.

Both the Read and Write sector commands also

contain an "m" flag for accessing multiple sectors. The sector register is incremented internally after each sector is read or written to. Eventually the sector register will exceed the physical number of sectors on the track. The user can either issue the Forced Interrupt command after the last sector, or wait for the 1771 to interrupt out. In the latter case, the RECORD-NOT-FOUND status bit will be set.

FLOPPY DISK INTERFACE

For the most part, the actual Floppy Disk Interface will consist mainly of Buffer/Drivers. Most drives manufactured today require an open collector TTL interface, with appropriate resistor terminal networks. Figure 2 shows the interface of the 1771 to a Shugart SA400 Drive. Aside from the data separator, the interface consists mainly of 7438's and 7414 TTL gates. A 9602 one-shot is used for the desired head load delay. In this illustration, the 6800 microprocessor is used via a 6820 Peripheral Interface Adapter to control all functions of the 1771. Similarly, other parallel port devices (such as the 8255 for 8080 systems) can be used for the interface, or the 1771 may simply be tied directly to the systems data bus and control lines, providing TTL loading factors are observed.

DATA SEPERATION

The internal DATA SEPERATOR of the 1771 can be used by tying the XTDS line high, and supplying the combined clock and data pulses on the FD data line. In order to maintain an error rate better than 1 in 10⁶, and external data separator is recommended.

Since the 1771 system clock is at 2 MHz, this allows for a 500 ns resolution. The internal data window will move 500 ns with respect to the incoming data bit. On the inner tracks of the drive, the bit shift is more severe and may occasionally cause a data or clock bit to fall outside of this data window. Since the 1771 will perform up to 5 retries, this error rate may be acceptable for some applications.

When the XTDS line is forced low, the 1771 will accept separated clock and data on the FDCLOCK and FDDATA lines. Figure 3 illustrates the timing of these signals. The actual FDCLOCK and FDDATA lines may be reversed; the 1771 will determine which line is clock and which is data when an Address Mark is detected. This feature greatly simplifies the design of the data separator.

Figure 4 illustrates the Phase-Lock Loop method for data separation. The circuit operates at 8 MHz, or 32 times the frequency of a received bit cell. The MC4024 VCO is used to supply the nominal clock frequency. The first 74LS161 counter provides a divide by 16 frequency and a carry to one side of the MC4044 phase detector. The other input of the MC4044 is tied to another 74LS161 counter which is affected by the incoming data stream. The output of

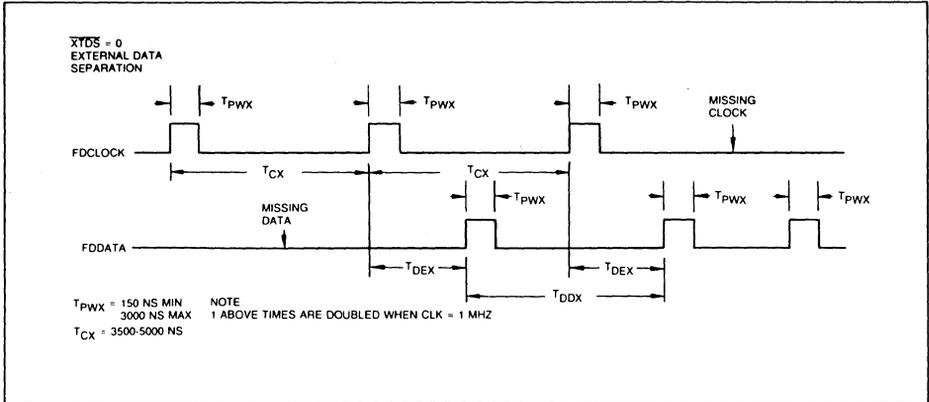


FIGURE 3 EXTERNAL DATA SEPERATOR TIMING.

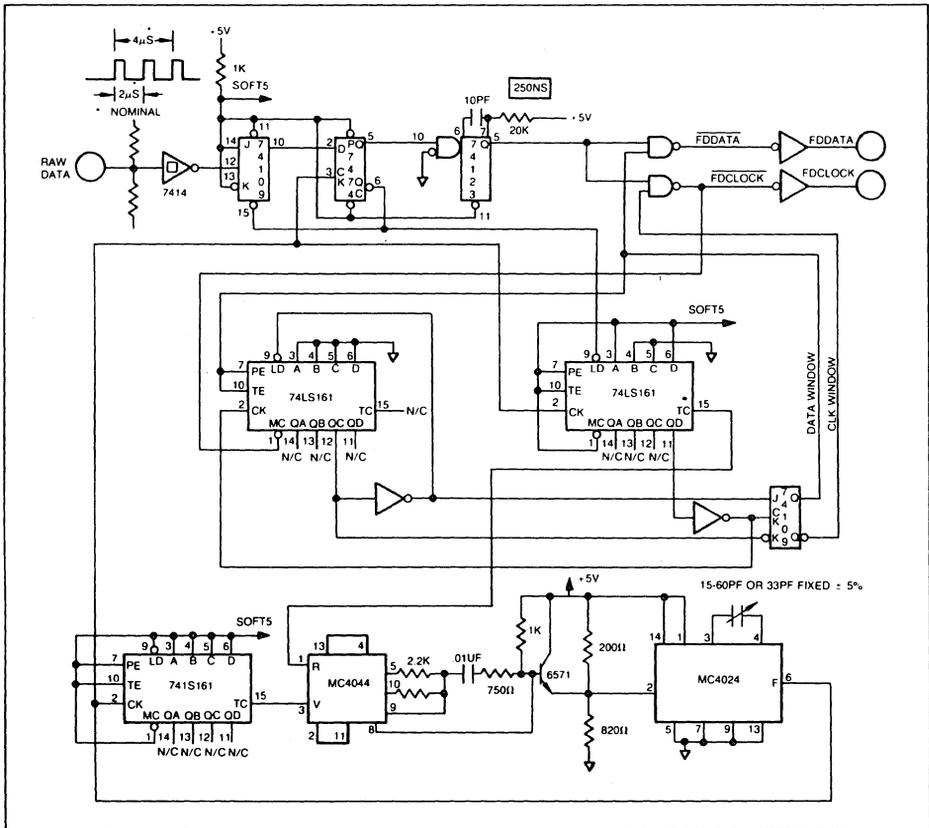


FIGURE 4 CIRCUIT PROVIDED COURTESY OF MOTOROLA AND ICOM CORPS.

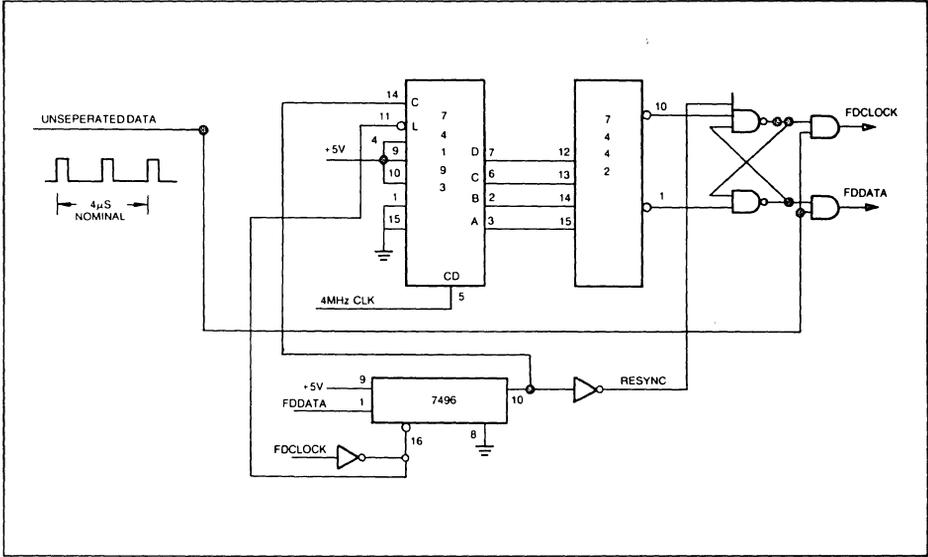


FIGURE 5 CIRCUIT PROVIDED COURTESY OF PROCESSOR APPLICATIONS LTD.

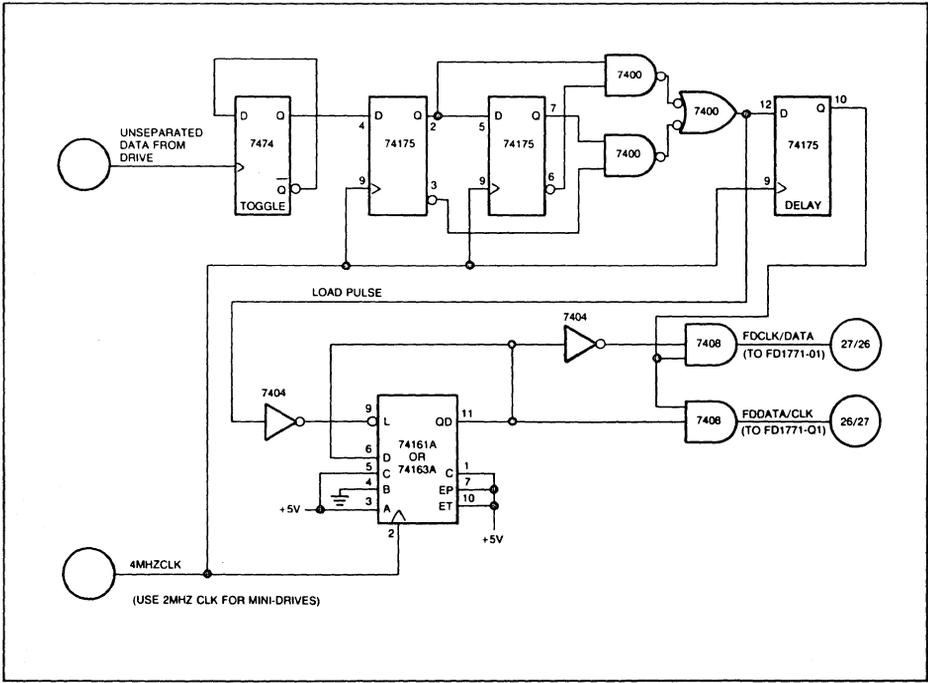


FIGURE 6

2 ZO-10110

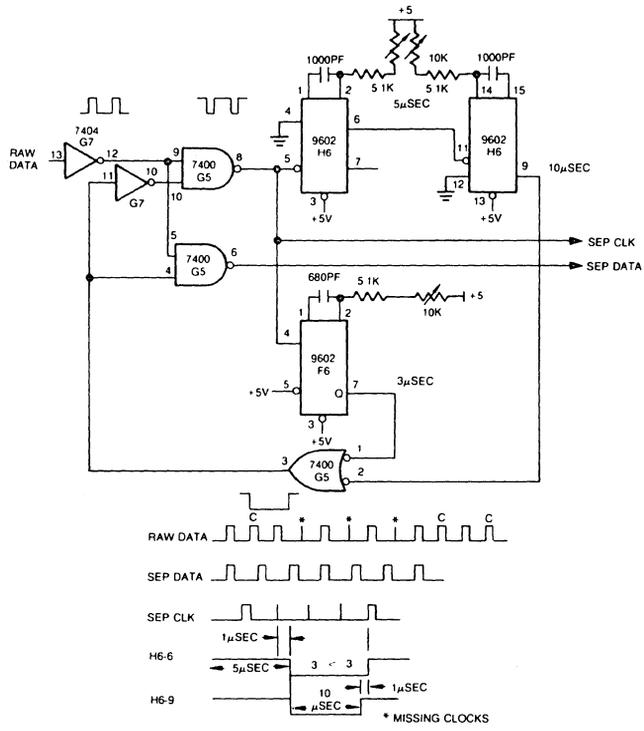


FIGURE 7 CIRCUIT PROVIDED COURTESY OF ACUTEST CORP.

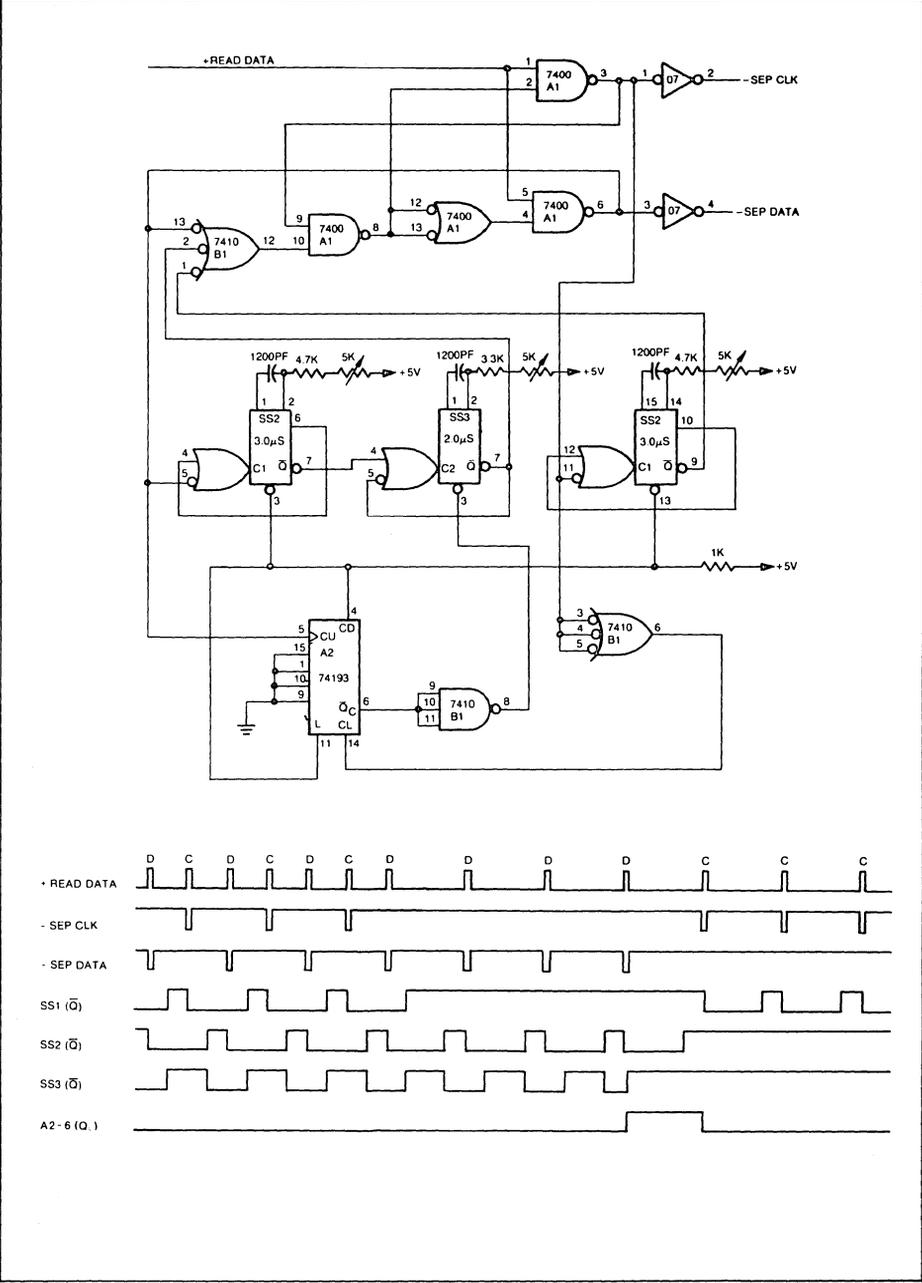


FIGURE 8 CIRCUIT PROVIDED COURTESY OF SHUGART ASSOCIATES.

All diagrams within this applications note are shown for illustrative purposes and may not necessarily reflect the total logic for implementation.

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C O R P O R A T I O N

WD1691 FLOPPY SUPPORT LOGIC (F.S.L.)

FEATURES

- Direct interface to the FD179X
- Eliminates external FDC Logic
- Data Separation/RCLK GENERATION
- Write Precompensation Signals
- VFOE/WF Demultiplexing
- Programmable Density
- 8" or 5.25" Drive Compatible
- All inputs and outputs TTL Compatible
- Single +5V Supply

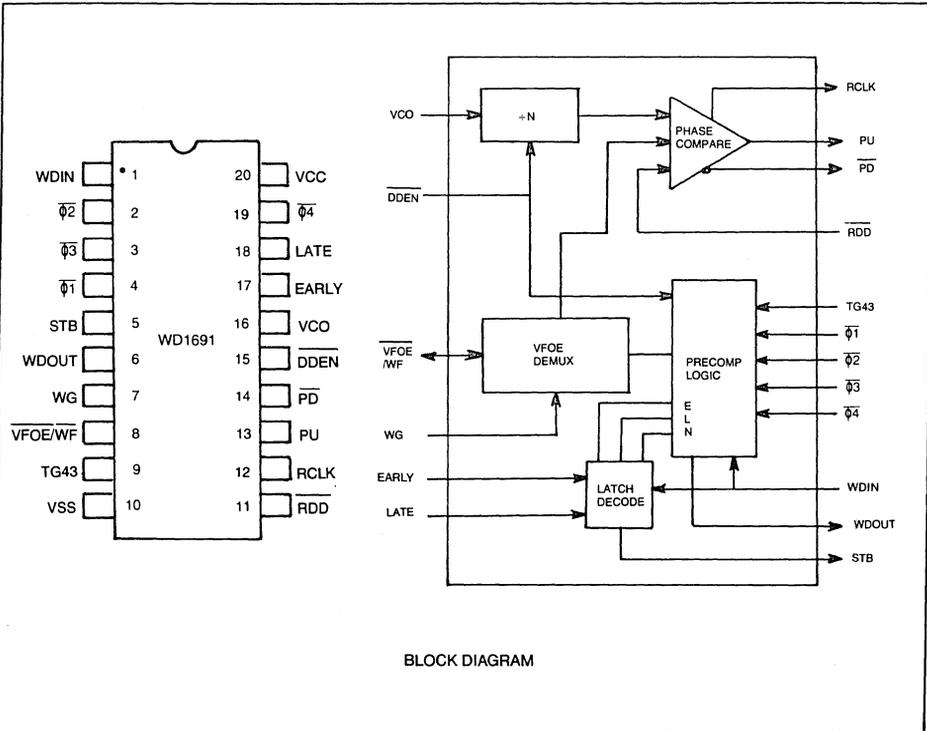
GENERAL DESCRIPTION

The WD1691 F.S.L. has been designed to minimize the external logic required to interface the 179X Family of Floppy Disk Controllers to a drive. With the use of an external VCO, the WD 1691 will generate the RCLK signal for the WD179X, while providing an adjustment pulse (PUMP) to control the VCO frequency. VFOE/WF de-multiplexing is also accomplished and Write Precompensation signals have been included to interface directly with the WD2143 Clock Generator.

The WD1691 is implemented in N-MOS silicon gate technology and is available in a plastic or ceramic 20 pin dual-in-line package.

October, 1980

SECTION 2



PIN	NAME	SYMBOL	FUNCTION
1	WRITE DATA INPUT	WDIN	Ties directly to the FD179X WD pin.
2, 3, 4, 19	PHASE 2, 3, 1, 4	$\overline{02}$ $\overline{03}$ $\overline{01}$ $\overline{04}$	4 Phase inputs to generate a desired Write Precompensation delay. These signals tie directly to the WD2143 Clock Generator.
5	STROBE	STB	Strobe output from the 1691. Strobe will latch at a high level on the leading edge of WDIN and reset to a low level on the leading edge of 04.
6	WRITE DATA OUTPUT	WDOUT	Serial, pre-compensated Write data stream to be sent to the disk drive's WD line.
7	WRITE GATE	WG	Ties directly to the FD179X WG pin.
8	VFO ENABLE/ WRITE FAULT	$\overline{\text{VFOE/WF}}$	Ties directly to the FD179X $\overline{\text{VFOE/WF}}$ pin.
9	TRACK 43	TG43	Ties directly to the FD179X TG43 pin, if Write Precompensation is required on TRACKS 44-76.
10	V _{ss}	V _{ss}	Ground
11	READ DATA	$\overline{\text{RDD}}$	Composite clock and data stream input from the drive.
12	READ CLOCK	RCLK	RCLK signal generated by the WD1691, to be tied to the FD179X RCLK pin.
13	PUMP UP	PU	Tri-state output that will be forced high when the WD1691 requires an increase in VCO frequency.
14	PUMP DOWN	$\overline{\text{PD}}$	Tri-state output that will be forced low when the WD1691 required a decrease in VCO frequency.
15	Double Density Enable	$\overline{\text{DDEN}}$	Double Density Select input. When Inactive (High), the VCO frequency is internally divided by two.
16	Voltage Controlled Oscillator	VCO	A nominal 4.0MHz (8" drive) or 2.0MHz (5.25" drive) master clock input.
17, 18	EARLY LATE	EARLY LATE	EARLY and LATE signals from the FD179X, used to determine Write Precompensation.
20	V _{cc}	V _{cc}	+ 5V ± 10% power supply

DEVICE DESCRIPTION

The WD1691 is divided into two sections:

- 1) Data Recovery Circuit
- 2) Write precompensation Circuit

The Data Separator or Recovery Circuit has four inputs: \overline{DDEN} , VCO, RDD, and $\overline{VFOE/WF}$; and three outputs: PU, \overline{PD} and RCLK. The $\overline{VFOE/WF}$ input is used in conjunction with the Write Gate signal to enable the Data recovery circuit. When Write Gate is high, a write operation is taking place, and the data recovery circuits are disabled, regardless of the state on any other inputs.

When $\overline{VFOE/WF}$ and WRITE GATE are low, the data recovery circuit is enabled. When the RDD line goes Active Low, the PU or PD signals will become active. If the RDD line has made its transition in the beginning of the RCLK window, PU will go from a HI-Z state to a Logic 1, requesting an increase in VCO frequency. If the RDD line has made its transition at the end of the RCLK window, PU will remain in a HI-Z state while PD will go to a logic zero, requesting a decrease in VCO frequency. When the leading edge of RDD occurs in the center of the RCLK window, both PU and PD will remain tri-stated, indicating that no adjustment of the VCO frequency is needed. The RCLK signal is a divide-by-16 ($\overline{DDEN}=1$) or a divide-by-8 ($\overline{DDEN}=0$) of the VCO frequency.

WG	VFOE/WF	RDD	PU+PD
1	X	X	HI-Z
0	1	X	HI-Z
0	0	1	HI-Z
0	0	0	Enable

The Write Precompensation circuit has been designed to be used with the WD2143-01 clock generator. When the WD1691 is operated in a "single density only" mode, write precompensation as well as the WD2143-01 is not needed. In this case, $\overline{\Phi 1}$, $\overline{\Phi 2}$, $\overline{\Phi 3}$, $\overline{\Phi 4}$, and STB should be tied together, \overline{DDEN} left open, and TG43 tied to ground.

In the double-density mode ($\overline{DDEN}=0$), the signals Early and Late are used to select a phase input ($\overline{\Phi 1} - \overline{\Phi 4}$) on the leading edge of WDIN. The STB line is latched high when this occurs, causing the WD2143-01 to start its pulse generation. $\overline{\Phi 2}$ is used as the write data pulse on nominal (Early=Late= $\overline{\Phi}$), $\overline{\Phi 2}$ is used for early, and $\overline{\Phi 3}$ is used for late. The leading edge of $\overline{\Phi 4}$ resets the STB line in anticipation of the next write data pulse. When TG43=0 or $\overline{DDEN}=1$, Precompensation is disabled and any transitions on the WDIN line will appear on the WDout line. If write precompensation is desired on all tracks, leave TG43 open (an internal pull-up will force a Logic 1) while $\overline{DDEN}=0$.

The signals, \overline{DDEN} , TG43, and RDD have internal pull-up resistors and may be left open if a logic 1 is desired on any of these lines.

The minimum Voh level on PU is specified at 2.4V, sourcing 200ua. During PUMP UP time, this output will "drift" from a tri-state to .4V minimum. By tying PU and PD together, a PUMP signal is created that will be forced low for a decrease in VCO frequency and forced high for an increase in VCO frequency. To speed up rise times and stabilize the output voltage, a resistor divider can be used to set the tri-state level to approximately 1.4V. This yields a worst case swing of $\pm 1V$; acceptable for most VCO chips with a linear voltage-to-frequency characteristic.

Both PU and PD signals are affected by the width of the RAW READ (RDD) pulse. The wider the RAW READ pulse, the longer the PU or PD signal (depending upon the phase relationship to RCLK) will remain active. If the RAW READ pulse exceeds 250ns. ($VCO = 4MHz$, $\overline{DDEN} = 0$) or 500ns. ($VCO = 4MHz$, $\overline{DDEN} = 1$), then both a PU and PD will occur in the same window. This is undesirable and reduces the accuracy of the external integrator or low-pass filter to convert the PUMP signals into a slow moving D.C. correction voltage.

Eventually, the PUMP signals will have corrected the VCO input to exactly the same frequency multiple as the RAW READ signal. The leading edge of the RAW READ pulse will then occur in the exact center of the RCLK window, and ideal condition for the FD179X internal recovery circuits.

SAMSUNG

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias -25° to 70°C
 Voltage on any pin with respect to Ground (vss) -0.2 to +7V
 Power Dissipation 1W

Storage Temp.—Ceramic—65°C to +150°C
 Plastic—55°C to +125°C

NOTE: Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

DC ELECTRICAL CHARACTERISTICS

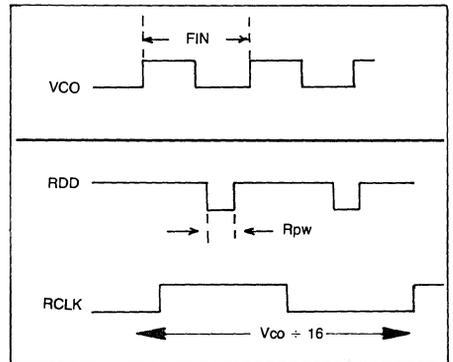
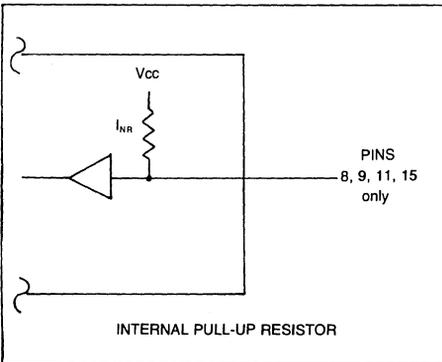
T_A = 0 to 70°C; V_{CC} = 5.0V±10%; V_{SS}=0V

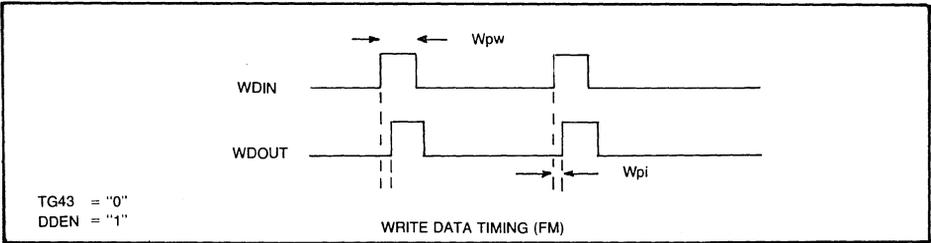
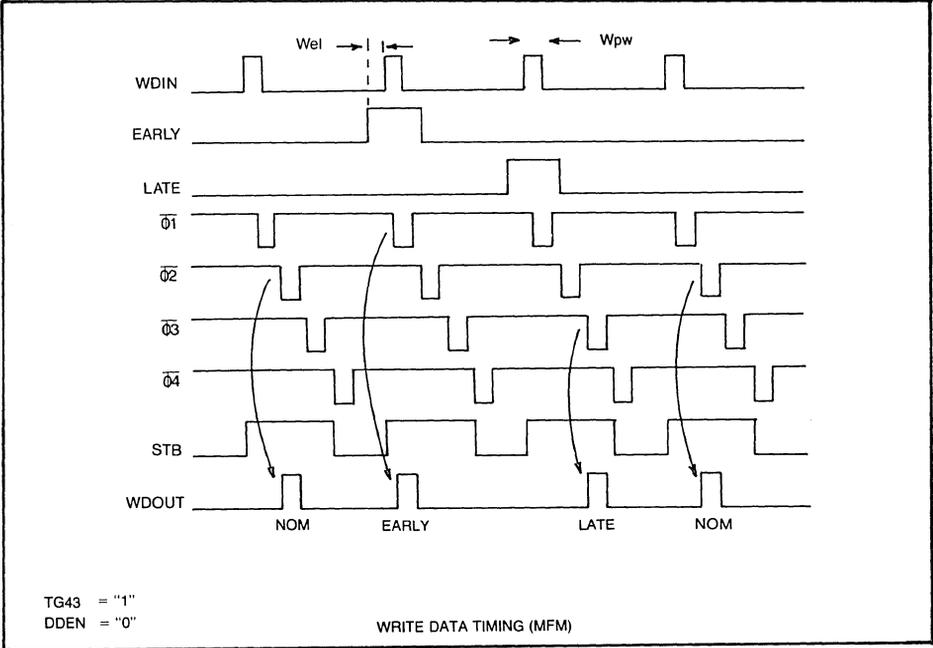
SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
V _{IL}	Input Low Voltage	-0.2		+0.8	V	
V _{IH}	Input High Voltage	2.0			V	
V _{OL}	Output Low Voltage			0.45	V	I _{OL} =3.2MA
V _{OH}	High Level Output Voltage	2.4			V	I _{OH} =-200µa
V _{CC}	Supply Voltage	4.5	5.0	5.5	V	
I _{CC}	Supply Current		40	100	MA	All outputs open

AC ELECTRICAL CHARACTERISTICS

T_A = 0° to 70°C; V_{CC} = 5V±10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
FIN	VCO Input Frequency	.5	4	6	MHz	$\overline{\text{DDEN}}=0$
		.5	2	6	MHz	$\overline{\text{DDEN}}=1$
R _{pw}	$\overline{\text{RDD}}$ Pulse Width	100	200		ns.	
W _{el}	EARLY (LATE) to WDIN	100			ns.	
P _{on}	PUMP UP/DN Time	0		250	ns.	
W _{pi}	WDIN to WDOU			80	ns.	$\overline{\text{DDEN}}=1$
I _{NR}	Internal Pull-up Resistor	4.0	6.5	10	KΩ	





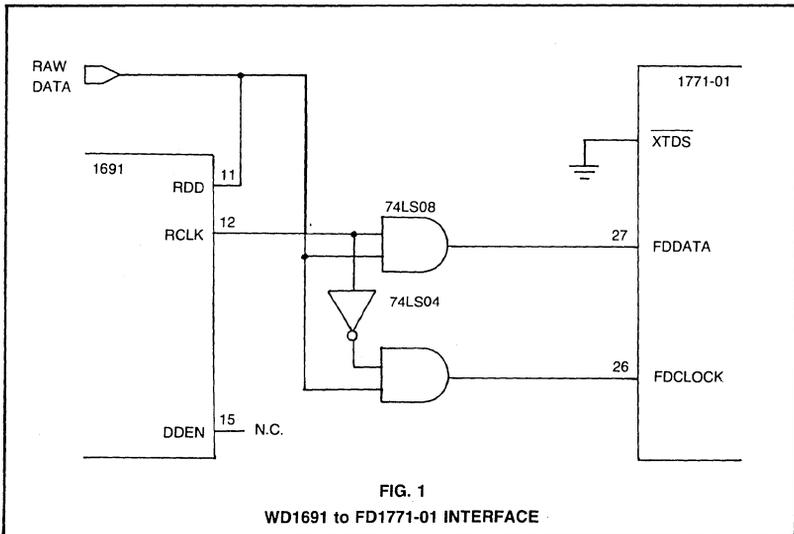
TYPICAL APPLICATIONS

Figure 1 illustrates the 1691 to FD1771-01 floppy disk controller. The RCLK signal is used to gate the RAW data pulses which are inverted by the 74LS04 inverter. Since RCLK will be high during data and low during clock a 74LS08 is used to switch the proper clock or data pulse to the FD1771.

Shown in Figure 2 is a Phase-Lock Loop data separator and the support logic for a single and double-density 8" drive. The raw data (Both clock and data bits) are fed to the WD1691 and FD179X. The WD1691 outputs its PU or PD signal, which is integrated by the .33uf capacitor and 33ohm resistor to form a control voltage for the 74S124 VCO device. The 4.0MHZ nominal output of the VCO then feeds back to the WD1691 completing the loop. The WD2143-01 is also used, providing write precompensation when in double-density, from tracks 44-77. The DDEN line can either be controlled by a toggle switch or a logic level from the host system.

To adjust write precompensation, issue a command to the FD179X so that write data pulses are present. This can be done with a 'WRITE TRACK' command and the IP line open, or a continuous 'WRITE SECTOR' operation. With a scope on pin 4 of the WD1691, adjust the precomp pot for the desired value. This will range from 100 to 300 ns typically. The pulse width set on pin 4 (01) will be the desired precomp delay from nominal.

The data separator must be adjusted with the $\overline{\text{RDD}}$ or VFOE/WF line at a Logic 1. Adjust the bias voltage potentiometer for 1.4V on pin 2 of the 74S124. Then adjust the range control to yield 4.0MHZ on pin 7 of the 74S124.



SUBSTITUTING VCO's

There are other VCO circuits available that may be substituted for the 74S124. The specifications required are:

- 1) The VCO must free run at 4.0MHz with a 1.4V control signal. The WD1691 will force this voltage 1 Volt in either direction (i.e., .4V = decrease frequency, 2.4V = increase frequency). If a $\pm 15\%$ capture range is desired, then a 1 Volt change on the VCO input should change the frequency by 15%. Capture range should be limited to about $\pm 25\%$, to prevent the VCO from breaking into oscillation and/or losing lock because of noise spikes (causing abnormally quick adjustments of the VCO frequency). Jitter in the VCO output frequency may further be reduced by increasing the integration capacitor/resistor, but this will also decrease the final capture range and lock-up time.

- 2) The sink output current of the WD1691 is 3.2ma minimum. The source output current is $-200\mu\text{a}$. Therefore, source current is the limiting factor. Insure that the input circuitry of the VCO does not require source current in excess of $-200\mu\text{a}$.

Another alternative is to use a voltage follower/level shifter circuit to match the input requirements of the VCO chosen. A more complex filter can be used to convert the PUMP UP/PUMP DOWN pulses to the varying DC voltage signal required by the VCO, achieving an optimum condition between lock-up time and high frequency rejection.

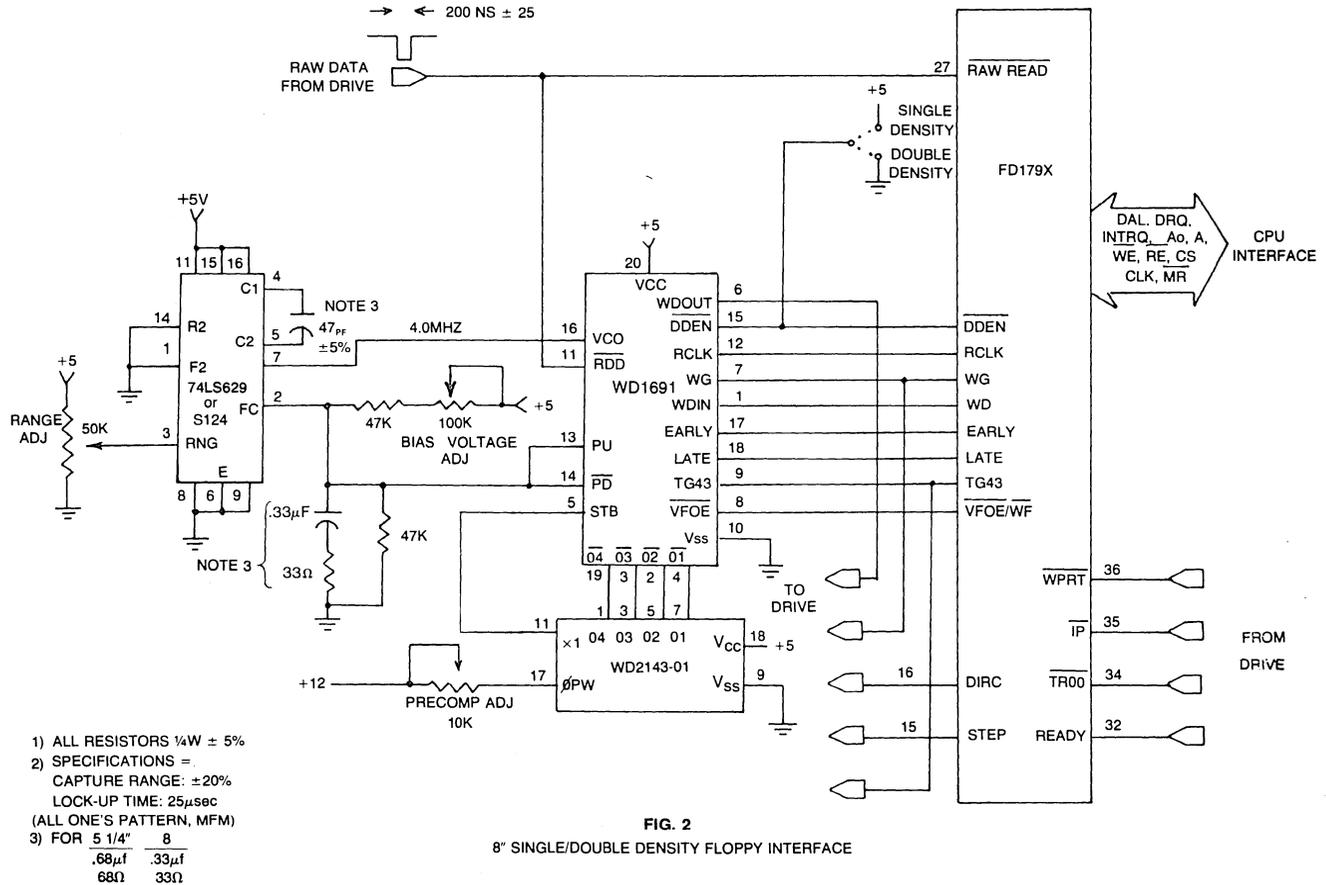
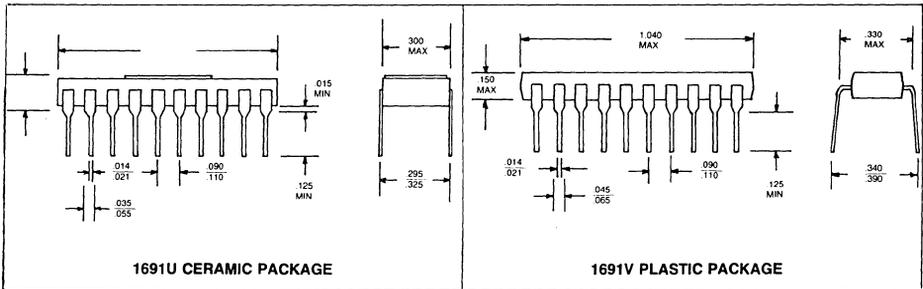


FIG. 2
8" SINGLE/DOUBLE DENSITY FLOPPY INTERFACE

2 ZO-10m6



This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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C O R P O R A T I O N

DM1883A/B Direct Memory Access Controller

AUGUST, 1980

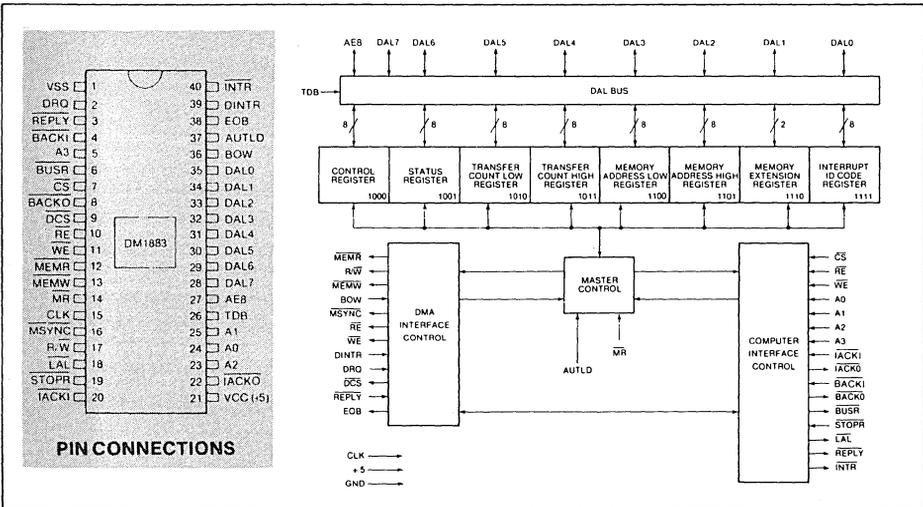
FEATURES

- AUTOMATIC DAISY CHAINING OF BUS AND INTERRUPT ACKNOWLEDGE SIGNALS
- AUTO LOAD OPTION
- SINGLE +5 VDC POWER SUPPLY
- 8 BIT BI-DIRECTIONAL DATA BUS
- TRUE OR COMPLEMENT DATA BUS
- 8 CPU ADDRESSABLE DMAC REGISTERS
- 8 CPU ADDRESSABLE DEVICE REGISTERS
- AUTOMATIC GENERATION OF DEVICE CS DURING DMA AND CPU DEVICE ACCESSES
- 256K MEMORY ADDRESSING
- 64K PROGRAMMABLE PAGE PROTECTION
- BYTE OR WORD DMA TRANSFERS
- INTERRUPT AND BUS REQUEST CAPABILITIES
- END-OF-BLOCK SHUT OFF BY DMAC
- TIME-OUT INTERRUPT CAPABILITY
- SINGLE CLOCK INPUT
- CS, RE, WE, A0-A3 ADDRESSING
- STOP REQUEST INPUT TO DELAY INTERRUPT OR BUS REQUESTS
- COMPATIBLE WITH OUR FLOPPY DISC CONTROLLERS
- 8 BIT PROGRAMMABLE INTERRUPT ID CODE

GENERAL DESCRIPTION

The DM1883 Direct Memory Access Controller (DMAC) is packaged in a 40 pin standard dual in-line package. The chip requires a single +5 power supply input and a single clock input. The device contains 8 CPU addressable registers, and allows for up to 8 CPU addressable device registers if the automatic device chip select feature is used. Byte or word transfers can be programmed, and all memory DMA operations are handshaked for compatibility with a variety of bus structures. Up to 256K bytes of memory can be accessed directly with 64K page protection and nonexistent memory interrupt as options. Bus and Interrupt Acknowledge signals are internally daisy chained, and a STOP REQUEST input prevents new requests while a current request is active. Device accesses are not handshaked, and a BUS HOLD feature is present for high speed devices. Device interrupt input, end-of-block output, and I/O read/write output pins simplify hardware interfacing to the device and the CPU bus. The AUTO LOAD feature allows automatic boot-loading of up to 64K bytes or words into memory starting at location zero. An 8 bit interruptID code is also provided.

2 NO-10M9



DM1883 BLOCK DIAGRAM

INTERFACE SIGNALS DESCRIPTIONS

PIN NUMBER	SIGNAL NAME	SYMBOL	FUNCTION
1	GROUND	VSS	Ground
2	DATA REQUEST	DRQ	Data service request input from the peripheral device. A DMA transfer is initiated when this signal goes high.
3	REPLY	REPLY	Active low bi-directional handshake signal for both CPU and DMA transfers.
4	BACK IN	BACKI	Bus acknowledge in. An active low input signal from the CPU or a previous device in the BACK daisy chain. When low this signal will initiate a DMA transfer if the DMAC was requesting a DMA cycle.
5, 23, 24, 25	REGISTER SELECTS	A0-A3	These inputs select one of eight DMAC registers or one of eight device registers. When A3 is high the DMAC is selected. When A3 is low the DMAC is deselected and DCS is made low by the DMAC to activate device transfers. CS input to the DMAC must be made low before either the DMAC or the device may be selected by the CPU.
6	BUS REQUEST	BUSR	Active low output signal to initiate a CPU bus request and to latch A8-A15, A17 of the 18 bit DMA transfer address from DAL0-DAL7, AE8 into an external register.
7	CHIP SELECT	CS	Active low chip select input signal for CPU controlled operations.
8	BACK OUT	BACKO	Bus acknowledge out. An active low output signal used to pass BACKI along the daisy chain when the DMAC is not requesting a DMA cycle. This output is not affected by STOPR.
9	DEVICE SELECT	DCS	Active low device chip select output signal for CPU and DMAC controlled operations.
10	READ ENABLE	RE	Active low bi-directional read enable for the DMAC and the device.
11	WRITE ENABLE	WE	Active low bi-directional write enable for the DMAC and the device. RE and WE are inputs during CPU controlled operations, and outputs to the device during DMAC controlled operations.
12	MEMORY READ	MEMR	Active low output to initiate a memory read during DMA transfers to the peripheral device.
13	MEMORY WRITE	MEMW	Active low output to initiate a memory write during DMA transfers from the peripheral device.
14	MASTER RESET	MR	Active low master reset signal to initialize the DMAC.
15	CLOCK	CLK	Clock input
16	MEMORY SYNC	MSYNC	Active low memory sync output to initiate a memory access during DMA transfers.
17	READ/WRITE	R/W	This output indicates the direction of transfer for the peripheral device. High for device-to-memory transfers (READ), and low for memory to device transfers (WRITE). Tied directly to Control Register bit 4.
18	LOAD ADDRESS LOW	LAL	Active low output signal to latch A0-A7, A16 of the 18-bit DMA transfer address from DAL0-DAL7, AE8 into an external register. BUSR and LAL are compatible with INTEL 8212 devices.

2
 10-1000
 2

PIN NUMBER	SIGNAL NAME	SYMBOL	FUNCTION
19	$\overline{\text{STOP REQUEST}}$	$\overline{\text{STOPR}}$	Active low input that prevents $\overline{\text{INTR}}$ and $\overline{\text{BUSR}}$ from going low even if a request becomes active. An active $\overline{\text{INTR}}$ or $\overline{\text{BUSR}}$ request will not be affected by this input going low. This signal is used to speed up daisy chaining of bus and interrupt acknowledge inputs, and to prevent new requests while some other request is in the process of being serviced.
20	$\overline{\text{IACK IN}}$	$\overline{\text{IACKI}}$	Interrupt acknowledge in. An active low input signal from the CPU or a previous device in the IACK daisy chain. The DMAC is selected when $\overline{\text{INTR}}$ is low and this signal goes low. If $\overline{\text{RE}}$ also goes low while the DMAC is selected via this signal then the interrupt ID code is gated onto DAL0-DAL7.
21	POWER SUPPLY	V_{CC}	+5 VDC power supply input
22	$\overline{\text{IACK OUT}}$	$\overline{\text{IACKO}}$	Interrupt acknowledge out. An active low output signal used to pass IACKI along the daisy chain when the DMAC is not requesting an interrupt. This output is not affected by STOPR.
26	TRUE DATA BUS	TDB	This input selects a true data bus on the DAL lines when high or open, and a complemented data bus on the DAL lines when low.
27	ADDRESS EXTENSION	AE8	Address extension bit output. Used during DMA operations to extend the address to 18 bits. This bit is true if TDB is high and complemented if TDB is low.
28-35	DATA ACCESS LINES	DAL0-DAL7	An 8-bit bi-directional three-state bus for CPU and DMAC controlled transfers to and from the DMAC. These signals remain in a three-state mode if the peripheral device is selected via A3 instead of the DMAC.
36	BYTE OR WORD	BOW	Byte or word DMA transfer mode input. When high memory addresses are incremented by one after every DMA transfer. When low memory addresses are incremented by two after every DMA transfer and the LSB of the memory address is forced to zero.
37	AUTO LOAD	AUTLD	Active high input to initiate a non-programmed 64K device to memory data transfer.
38	END OF BLOCK	EOB	Active high output to shut off the peripheral device when the transfer count goes to zero.
39	DEVICE INTERRUPT	DINTR	Interrupt service request input from the peripheral device. An interrupt request is generated by the DMAC if this input is high and the device interrupt enable bit in the command register is also set.
40	$\overline{\text{INTERRUPT REQUEST}}$	$\overline{\text{INTR}}$	Active low interrupt service request output. This output goes low if: 1) Any one of the three interrupt conditions is active, and 2) The $\overline{\text{STOPR}}$ input is high, and 3) The corresponding interrupt enable bit for the interrupting condition is set.

NOTE: The following pins float when not active low and require an external pull-up resistor of 10 K Ω (or greater) to +5 VDC:

$\overline{\text{INTR}}$, $\overline{\text{REPLY}}$, $\overline{\text{RE}}$, $\overline{\text{WE}}$, $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{MSYNC}}$

The following pins have internal 10 K Ω pull-up resistors to +5 VDC:

TBD, DRQ, DINTR

WIRE-ORABLE SIGNALS

The following output signals can be wired together with a single common pull-up resistor if multiple DMAC chips exist on the same board:

MSYNC, MEMR, MEMW, INTR

REGISTER SELECTION

A 4-bit address input (A0, A1, A2, A3) is used to select one of 8 internal DMAC registers or to generate a device chip select (DCS) output signal for selection of up to 8 peripheral device registers. The following table details the selection process.

INPUTS					OUTPUT	SELECTED REGISTER
CS	A3	A2	A1	A0	DCS	
L	L	X	X	X	L	One of 8 peripheral device registers
L	H	L	L	L	H	DMAC control register (0)
L	H	L	L	H	H	DMAC status register (1)
L	H	L	H	L	H	DMAC TC low register (2)
L	H	L	H	H	H	DMAC TC high register (3)
L	H	H	L	L	H	DMAC MA low register (4)
L	H	H	L	H	H	DMAC MA high register (5)
L	H	H	H	L	H	DMAC MA ext. register (6)
L	H	H	H	H	H	DMAC ID code register (7)

NOTE: L = Low voltage level, H = High voltage level, X = don't care.

TRANSFER COUNT REGISTER (TCR)

A 16-bit counter register that holds the two's complement of the transfer count (words or bytes) for DMA transfer operations. The low order 8 bits are in TC low, and the high order 8 bits are in TC high. The count is incremented by one after every DMA transfer. When the count reaches zero bit 3 of the Status Register is set to a one. If bit 3 in the Command Register is also a one then INTR will go low (providing STOPR is also high). TCR is set to a one on a MASTER RESET to allow a 64K transfer count during auto load.

MEMORY ADDRESS REGISTER (MAR)

An 18-bit counter register that occupies 3 DMA registers. Bits 0-7 are in MA low, bits 8-15 are in MA high, and bits 16-17 are in MA ext. The carry from bit 15 to 16 is enabled if and only if bit 6 of the Command Register is set to a one. If the BOW input pin is high then the MAR is incremented by one after every DMA transfer. If the BOW input pin is low then the MAR is incremented by two after every transfer and bit 0 is forced to a zero. This register is cleared to all zeros on a MASTER RESET.

During a DMA operation the DMA address is gated onto the DAL lines in two 9-bit bytes. The first byte out contains MAR 8-15 on DAL 0-7 and MAR 17 or AE8. The second byte out contains MAR 0-7 on DAL 0-7 and MAR 16 on AE8. The first byte is valid on the trailing edge of BUSR, and the second byte is valid on the trailing edge of LAL. Note that the address can easily be extended to 24 bits by decoding the address of the 2-bit extension register externally and gating the 6 unused bits into an external latch. This would give the system 16Mbytes of addressing with either 65K or 256K bytes of paging.

REGISTER DEFINITIONS

DMAC CONTROL REGISTER (CR)

	7	6	5	4	3	2	1	0
	N/A	AECE	HBUS	IOM	TCIE	TOIE	DIE	RUN
BIT	SYMBOL		FUNCTION					
0	RUN	Run/stop bit. A 1 places the DMAC in the run mode. A 0 terminates DMAC operation.						
1	DIE	Device interrupt enable. A 1 allows a high input on DINTR to set the INTR output low.						
2	TOIE	Time-out interrupt enable. A 1 allows the time-out one-shot to set the INTR output low. The time-out interrupt is set during a DMA transfer if REPLY does not go low within 5 usec of MSYNC going low.						
3	TCIE	Transfer count zero interrupt enable. A 1 allows a zero in the transfer count register to set the INTR output low.						
4	IOM	Input or output mode. A 1 sets READ mode (from the peripheral device to memory), and a 0 sets WRITE mode (from memory to the peripheral device). This bit also appears as an ungated output on the R/W pin.						
5	HBUS	Hold bus. A 1 informs the DMAC to hold onto the bus for the entire block instead of releasing the bus after each byte or word transfer.						

BIT	SYMBOL	FUNCTION
6	AECE	Address extension carry enable. A 1 allows a carry from DMA address bit 15 to propagate into bit 16.
7	N/A	Not used.

NOTE: Bits 1, 2, 3 set $\overline{\text{INTR}}$ low on an active condition if and only if the $\overline{\text{STOPR}}$ input is high.

DMAC STATUS REGISTER (SR)

		7	6	5	4	3	2	1	0
		BUSY	AECE	HBUS	IOM	TCZI	TOI	DINT	BOW
BIT	SYMBOL	FUNCTION							
0	BOW	Byte or word data channel. A read only bit that indicates the status of the BOW input pin. A 1 bit indicates byte mode, and the DMA memory address is incremented by one after each DMA transfer. A 0 bit indicates word mode, and the DMA memory address is incremented by two (bit 0 is forced to a 0) after every DMA transfer.							
1	DINT	If set a device interrupt has occurred. This is a read/write bit. Resetting this bit to a zero will reset $\overline{\text{INTR}}$.							
2	TOI	If set a time-out interrupt has occurred. This is a read/write bit. Resetting this bit to a zero will reset $\overline{\text{INTR}}$.							
3	TCZI	If set a transfer count equals zero interrupt has occurred. A read only bit. Sets EOB output when set.							
4	IOM	Input-output mode. This bit reflects the status of bit 4 in the Command Register. A read only bit.							
5	HBUS	Hold bus. This bit reflects the status of bit 5 in the Command Register. A read only bit.							
6	AECE	Address extension carry enable. This bit reflects the status of bit 6 in the Command Register. A read only bit.							
7	BUSY	Busy (data transfer not completed). A read only bit that reflects the status of bit 0 (RUN) in the Command Register.							

NOTE: Bits 1, 2, 3 are set if the corresponding condition occurs. The enable bits in the CR affect only the $\overline{\text{INTR}}$ output, and not the Status Register.

ID CODE REGISTER (IDR)

An 8-bit programmable interrupt ID code register that gives the system an efficient way to establish a jump or vector address during a DMAC interrupt. The register is cleared to all zeros during a MASTER RESET, and must be loaded by the program during system initialization. If $\overline{\text{INTR}}$ is low, and $\overline{\text{IACK1}}$ and $\overline{\text{RE}}$ go low then the contents of this register are gated onto DAL 0-7. $\overline{\text{IACK1}}$ and $\overline{\text{CS}}$ must not be allowed to be low at the same time.

MASTER RESET

All register bits are reset to a zero during a MASTER RESET except the following which are set to ones: TCR bit 0, CR4, CR5, CR6, SR4, SR5, and SR6. This sets up the DMAC for a 64K transfer from the peripheral device to memory starting at address 0. The hold bus mode is also enabled. Execution of an Auto Load will begin DMA transfers under the above conditions.

AUTO LOAD

If the AUTLD input is made active after a MASTER RESET then bits CR3, CR1, and CR0 are also set. This places the DMAC in run mode, and enables two of the interrupt conditions. The DMAC will initiate data transfers, and will continue until either the transfer count reaches zero or a device interrupt occurs. Either event will terminate transfers and generate an interrupt.

WRITE PROTECT FEATURE

During CPU controlled transfers to the DMAC, if the RUN bit is set then any attempt to write into any of the Memory Address or Transfer Count registers will result in a NOP. $\overline{\text{REPLY}}$ will be made low in any case.

CPU CONTROLLED DATA TRANSFERS

During a CPU controlled transfer the CPU must have control of the system bus. When a CPU cycle is

initiated the system decodes the address on the bus. If the DMAC or its associated peripheral device is selected then \overline{CS} to the DMAC is made low. The DMAC looks at the A3 input. If A3 is low the peripheral device is selected, and \overline{DCS} is made low. The DMAC will not respond to an active \overline{RE} or \overline{WE} if A3 is low, and the DAL bus will stay in a high impedance state. This allows the DMAC DAL bus and the device DAL bus to be tied together if the device DAL bus is also in a high impedance state when the device is not selected.

If A3 is high when \overline{CS} is low then the DMAC is selected and will respond to an active low \overline{RE} or \overline{WE} . A0-A2 selects the DMAC as described under the REGISTER SELECTION section. If \overline{RE} goes low the DMAC places the contents of the selected register on the DAL bus and activates \overline{REPLY} to inform the CPU that valid data is on the bus. If \overline{WE} goes low the DMAC gates the contents of the DAL bus into the selected register and activates \overline{REPLY} to inform the CPU that data has been accepted.

If the peripheral device has more than 8 registers, or the device has fewer than 8 registers and there are one or more auxiliary registers external to the device, then it may be easier for the user to separate DMAC and device chip selects. In this mode \overline{CS} to the DMAC is activated if and only if the DMAC is selected and A3 is tied to +5 VDC. The chip select to the device from a CPU controlled data transfer is ORed with \overline{DCS} out of the DMAC. In this mode \overline{DCS} will go low if and only if a DMA transfer is in effect and can be used by the controller as a "DMA ACTIVE" signal. Note that in any case actual data transfers to and from the CPU and the peripheral device are done by way of the device's DAL bus, not the DMAC's DAL bus.

DMAC CONTROLLED DATA TRANSFERS

When the DMAC is in RUN mode (CR0=1) it waits for a Data Request (DRQ) input from the peripheral device. When DRQ becomes active the DMAC requests the bus from the CPU by activating \overline{BUSR} . If \overline{STOPR} was active when DRQ went active then the DMAC would wait until \overline{STOPR} went high before activating \overline{BUSR} . When \overline{BACKI} goes low in response to an active \overline{BUSR} the request has been granted and the DMAC controls data transfers between the peripheral device and memory. The direction of the transfer is determined by the status of the $\overline{READ/WRITE}$ (R/W) output pin. Note that R/W is tied directly to CR4.

1.) DEVICE-TO-MEMORY DMA TRANSFERS (CR4=1)

Once the DMAC has been granted the bus the following occurs:

- A.) The DMAC places the high byte of the memory address on the DAL lines, activates \overline{DCS} , and then raises \overline{BUSR} . The trailing edge of

\overline{BUSR} can be used to latch the address into an external buffer.

- B.) The DMAC places the low byte of the memory address on the DAL lines while activating \overline{LAL} , and then activates \overline{MSYNC} . The trailing edge of \overline{LAL} can be used to latch the address into an external buffer
- C.) The DAL lines are placed into a high impedance state in anticipation of a data transfer across the bus.
- D.) The DMAC activates \overline{RE} and then activates \overline{MEMW} .
- E.) The DMAC waits for \overline{REPLY} to go low. When \overline{REPLY} is active the DMAC deactivates \overline{MEMW} and then deactivates \overline{RE} .
- F.) If the DMAC is *not* in hold bus mode (CR5=1) then the DMAC deactivates \overline{DCS} and gives up control of the bus. If the DMAC is in hold bus mode then \overline{DCS} remains low until after the completion of the final data transfer. Note that \overline{BUSR} still cycles for every transfer.
- G.) After the completion of every data transfer the memory address register is incremented by one in byte mode or two in word mode.
- H.) After the completion of every data transfer the transfer count is incremented by one. Transfers are considered to be completed when the transfer count equals zero.

2.) MEMORY-TO-DEVICE DMA TRANSFERS (CR4=0)

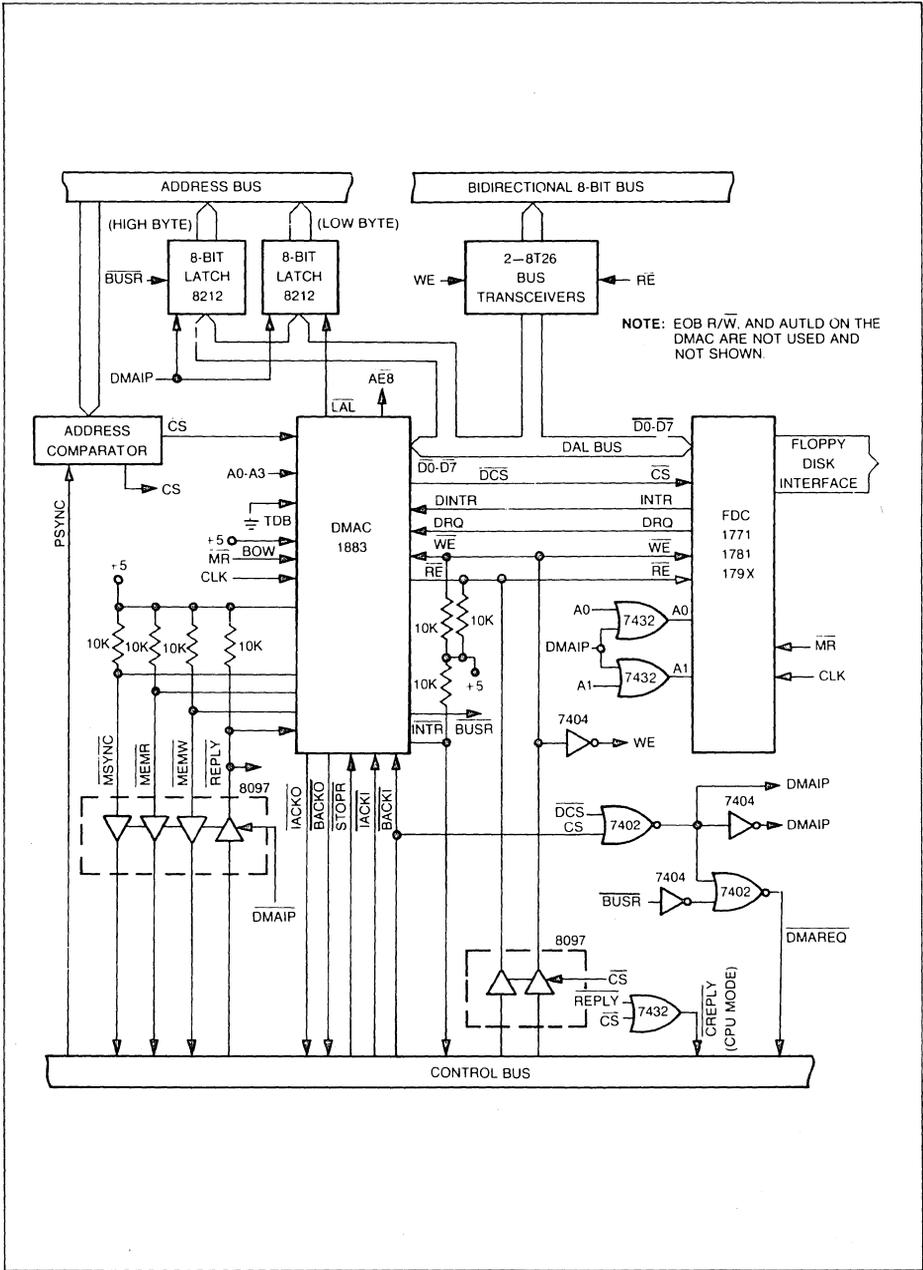
Once the DMAC has been granted the bus it goes through the same steps as in the DEVICE-TO-MEMORY mode with the exception of steps "D" and "E" which are as follows:

- D.) The DMAC activates \overline{MEMR} and then activates \overline{WE} .
- E.) The DMAC waits for \overline{REPLY} to go low. When \overline{REPLY} is active the DMAC deactivates \overline{WE} and then deactivates \overline{MEMR} .

In either mode \overline{BACKI} will be gated out to \overline{BACKO} as soon as the DMAC deactivates \overline{DCS} . This allows other devices in the chain to gain access to the bus immediately.

INTERRUPTS

There are three individually enabled interrupt conditions. If any of the conditions occurs it will set its corresponding bit in the Status Register. If the appropriate enable bit in the Command Register is set then \overline{INTR} is also activated. Note that these are independent functions. When \overline{INTR} is active then the DMAC can be selected by an active \overline{IACKI} instead of an active \overline{CS} . \overline{CS} and \overline{IACKI} must not both be active at the same time.



TYPICAL DMAC TO FDC APPLICATION

Once an interrupt condition sets its corresponding bit in the status register the bit stays set until a CPU write to the status register occurs with a zero in the bit position.* If any one (or more) of the three interrupt condition bits in the Status Register is set then IACKI will not be gated out to IACKO even if the interrupt is *not* enabled.

NOTE: For a transfer-count-equals-zero interrupt condition to be cleared the Transfer Count Register must be loaded with a non-zero count.

The three interrupt conditions are as follows:

1.) DEVICE INTERRUPT (DINT)

A device interrupt condition occurs when the DINTR input is made high. This sets SR1 and, if CR1 is set, it activates INTR. The RUN bit is also reset thus terminating all subsequent DMA transfers. A device interrupt could be generated by a number of causes, and the program will have to test the device's Status Register to determine the cause of the interrupt. The DINT status bit in the DMAC Status Register must be cleared by the program as a part of the interrupt service routine.

2.) TRANSFER COUNT EQUALS ZERO INTERRUPT (TCZI)

When the TCR is incremented to zero after a DMA transfer the TCZI status bit (SR3) is set and the RUN bit (CR0) is reset. This terminates all DMA operations and, if CR3 is set, activates INTR. SR3 can be cleared only by loading a non-zero value into the TCR. The EOB output pin is high whenever SR3 is set.

3.) TIME-OUT INTERRUPT (TOI)

During any DMA transfer the leading edge of MSYNC triggers an internal time delay of approximately 5 microseconds. If the DMAC does not receive an active low REPLY input within that time delay then the DMA operation is terminated, the RUN bit is reset, and the TOI status bit (SR2) is set. If CR2 is set then INTR is activated. SR2 can only be cleared by writing a zero into that position of the Status Register.

INTERLUPT OPERATION

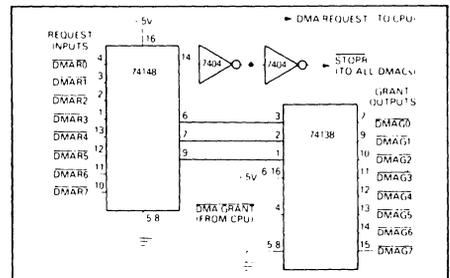
When the DMAC activates INTR the CPU responds by activating IACKI. This signal can be daisy chained through all devices. The first device in the chain that has any bit in SR1-SR3 set will block the gating of IACKI out to IACKO. In addition, if INTR is active an IACKI will select the DMAC. An active RE after an IACKI select will gate the contents of the interrupt ID code register onto the DAL lines. The ID code stays active on the DAL lines as long as IACKI and RE are active. This code, which is cleared to zero by a MASTER RESET and loaded by the program during system initialization, can be used by the system to create a JUMP or VECTOR address for the

device interrupt routine. Note that an active CS during a DMAC select via an active IACKI will cause unspecified results. Note also that no condition can activate INTR unless its corresponding enable bit is set and STOPR is high. If STOPR is active when the interrupt condition occurs then the DMAC will hold INTR inactive until STOPR goes inactive. At that time the DMAC will activate INTR automatically.

DMA PRIORITY SYSTEMS

Fixed Priority

A fixed priority can be established in two ways: through a parallel request-grant system or through a CPU controlled daisy chain system. A typical asynchronous parallel DMA priority system is shown. In this system any request generates an active STOPR, which is gated to all devices, and an active DMA request to the CPU. The CPU DMA grant generates a grant to the requesting device with the highest priority. If more than one request is received at the same time then the grants are honored from the highest to the lowest priority. In most cases, however, grants are not received simultaneously. The highest priority devices, therefore, will receive most of the immediate grants with the others being delayed by an active STOPR.



ASYNCHRONOUS PARALLEL DMA PRIORITY SYSTEM

Establishing a fixed priority system through a daisy chain approach requires the CPU monitor a "DMA IN PROGRESS" signal on the bus. This signal can be generated from DCS during a DMA transfer (i.e., DCS-CS). In this mode the CPU activates BACKI and STOPR in response to some bus request. STOPR is tied to all DMA controllers to prevent new bus requests while BACKI is propagating through all non-requesting DMAC devices. When the requesting DMAC gains control over the bus and activates DCS the CPU drops BACKI*. When DCS is deactivated the CPU deactivates STOPR to allow new requests. In this manner the device physically closest to the CPU on the daisy chain has highest priority for all request cycles.

NOTE: BACKI and STOPR can be dropped at the same time with no effect on the priority scheme, but the CPU may have to capture new requests until DCS goes high.

Rotating Priority

This is a daisy chain approach that prevents one device from getting most of the bus grants if multiple devices are active at the same time. In this mode any device requesting the bus causes the CPU to activate BACKI. This signal is tied to the BACKI and STOPR inputs of the first DMAC. The BACKO output of the first DMAC goes to the BACKI and STOPR inputs of the second DMAC, and so on. The BACKO output of the last DMAC in the chain goes back to the CPU to reset its BACKI output. In this mode the first device cannot request again until all other requesting devices in the chain have also been serviced.

In any case, if the CPU has to have the DMA request held active throughout the DMA cycle then the user will have to create this signal on the controller thusly: $DMAREQ = BUSR + (DCS \cdot \overline{CS})$. If the device and DMAC chip selects are generated on the controller separately then the \overline{CS} can be eliminated from the equation. It is needed only to distinguish a CPU chip select from a DMA cycle chip select. Note that in either case the second term in the equation is equivalent to "DMA CYCLE IN PROGRESS" (DMAIP).

SPECIFICATIONS

Absolute Maximum Ratings

Ambient Temperature Under Bias... 0°C to +70°C
 Voltage on Any Pin with Respect to Ground -0.5V to +7V
 Power Dissipation 0.6 Watt

NOTE: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

DC Electrical Characteristics

$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$; $V_{CC} = 5.0\text{V} \pm 5\%$; $GND = 0\text{V}$

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.4		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 1.6\text{ mA}$
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -100\ \mu\text{A}$
I_{DL}	Data Bus Leakage			-50	μA	$V_{IN} = 0.45\text{V}$
				10	μA	$V_{IN} = V_{CC}$
I_{IL}	Input Leakage			10	μA	$V_{IN} = V_{CC}$
I_{CC}	Power Supply Current		45	90	mA	

NOTE: $V_{OL} \leq 0.4\text{V}$ when interfacing with low power Schottky parts ($I_{OL} < 1\text{ mA}$).

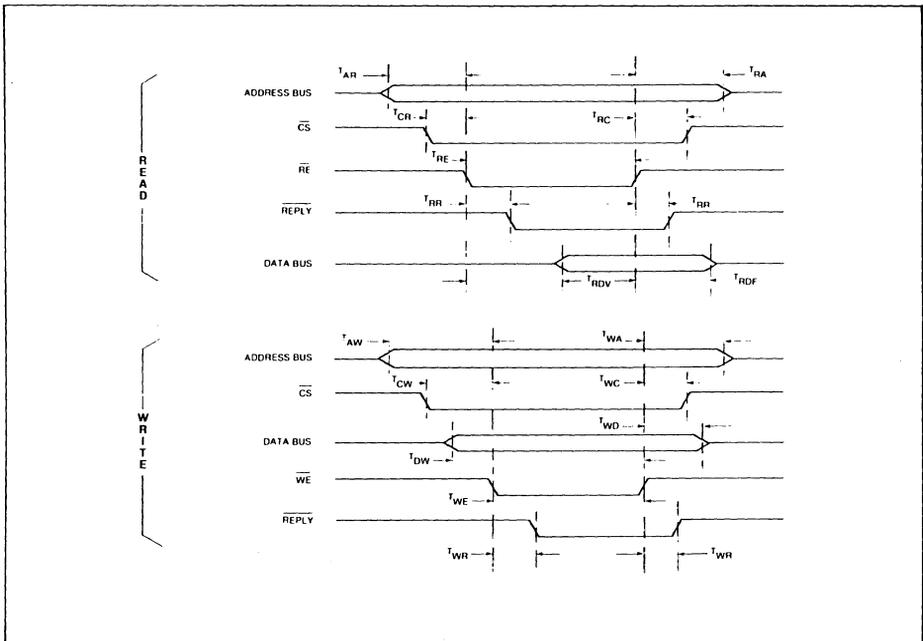
Capacitance

$T_A = 25^\circ\text{C}$; $V_{CC} = GND = 0\text{V}$

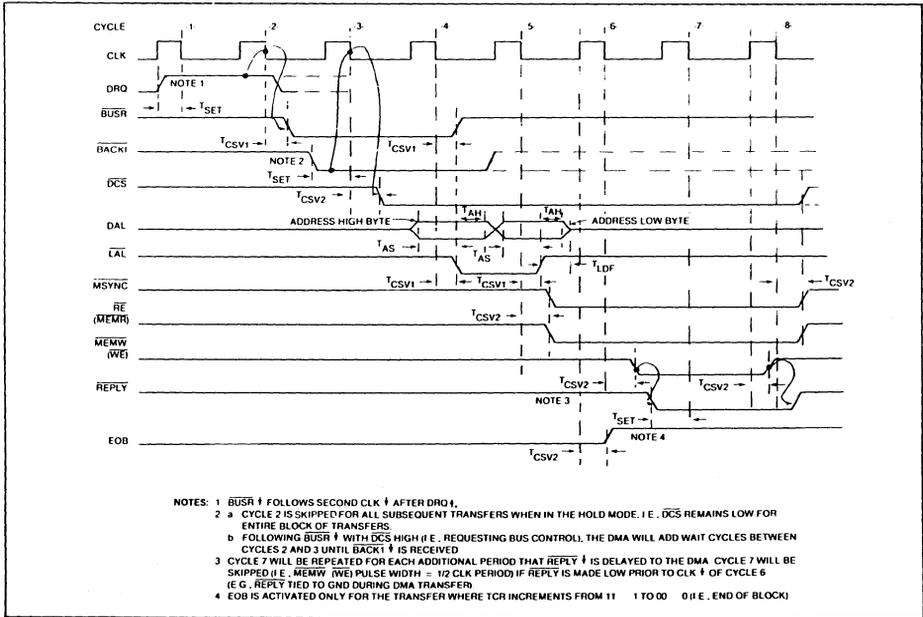
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	$f_C = 1\text{ MHz}$
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND.

System Clock (CLK) Characteristics

Maximum Frequency	2.0 MHz
Minimum Pulse Width	250 ns
Maximum Pulse Width	50% of duty cycle



CPU CONTROLLED TRANSFER



- NOTES:**
- 1 BUSR \uparrow FOLLOWS SECOND CLK \uparrow AFTER DRQ \uparrow .
 - 2 a CYCLE 2 IS SKIPPED FOR ALL SUBSEQUENT TRANSFERS WHEN IN THE HOLD MODE, I.E. DCS REMAINS LOW FOR ENTIRE BLOCK OF TRANSFERS.
b FOLLOWING BUSR \uparrow WITH DCS HIGH IF E. REQUESTING BUS CONTROL, THE DMA WILL ADD WAIT CYCLES BETWEEN CYCLES 2 AND 3 UNTIL BACK# \uparrow IS RECEIVED.
 - 3 CYCLE 2 WILL BE REPEATED FOR EACH ADDITIONAL PERIOD THAT REPLY \uparrow IS DELAYED TO THE DMA. CYCLE 7 WILL BE SKIPPED IF E. MEMW (WE) PULSE WIDTH = 1/2 CLK PERIOD IF REPLY IS MADE LOW PRIOR TO CLK \uparrow OF CYCLE 6 (E.G. REPLY TIED TO GND DURING DMA TRANSFER).
 - 4 EOB IS ACTIVATED ONLY FOR THE TRANSFER WHERE TCR INCREMENTS FROM 11 1 TO 00 0 I.E. END OF BLOCK.

DMA CONTROLLED TRANSFER TIMING

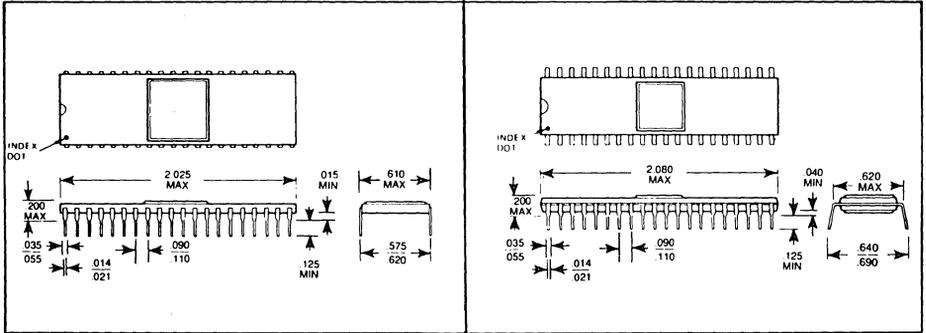
AC Electrical Characteristics

T_A = 0°C to +70°C; V_{CC} 5.0V ±5%; GND 0V

SYMBOL	DESCRIPTION	MIN	MAX.	UNIT	COND	
CPU CONTROLLED TRANSFER TIMING - READ						
T _{AR}	Address Valid to $\overline{RE} \downarrow$	80		ns		
T _{CR}	$\overline{CS} \downarrow$ to $\overline{RE} \downarrow$	0		ns		
T _{RE}	\overline{RE} Pulse Width	300		ns		
T _{RDV}	$\overline{RE} \downarrow$ to Data Valid		375	ns	CL = 50 pF	
T _{RR}	$\overline{RE} \downarrow$ (4) to $\overline{REPLY} \downarrow$ (4)	50	350	ns	CL = 50 pF	
T _{RA}	Address Hold from $\overline{RE} \downarrow$	30		ns		
T _{RC}	\overline{CS} Hold from $\overline{RE} \downarrow$	0		ns		
T _{RDF}	Data Float from $\overline{RE} \downarrow$		200	ns		
CPU CONTROLLED TRANSFER TIMING - WRITE						
T _{AW}	Address Valid to $\overline{WE} \downarrow$	80		ns		
T _{CW}	$\overline{CS} \downarrow$ to $\overline{WE} \downarrow$	0		ns		
T _{DW}	Data Valid to $\overline{WE} \downarrow$	300		ns	CL = 50 pF	
T _{WE}	\overline{WE} Pulse Width	300		ns		
T _{WR}	$\overline{WE} \downarrow$ (4) to $\overline{REPLY} \downarrow$ (4)	50	350	ns	CL = 50 pF	
T _{WA}	Address Hold from $\overline{WE} \downarrow$	30		ns		
T _{WC}	\overline{CS} Hold from $\overline{WE} \downarrow$	0		ns		
T _{WD}	Data Hold from $\overline{WE} \downarrow$	30		ns		
SYMBOL	DESCRIPTION	MIN	TYP	MAX.	UNIT	COND
DMA CONTROLLED TRANSFER TIMING						
T _{C5V1}	Indicated CLK Edge to Indicate Signal Valid		150	250	ns	CL = 50 pF
T _{C5V2}	Indicated CLK Edge to Indicated Signal Valid		250	400	ns	CL = 50 pF
T _{AS}	DAL Set Up to $\overline{BUSR} \downarrow$ or $\overline{LAL} \downarrow$ (4)	80			ns	CL = 50 pF
T _{AH}	DAL Hold from $\overline{BUSR} \downarrow$ or $\overline{LAL} \downarrow$ (4)	50			ns	CL = 50 pF
T _{LDF}	$\overline{LAL} \downarrow$ to DAL Float			250	ns	CL = 50 pF
T _{SET}	Indicated Signal Setup to Indicated CLK Edge	80			ns	
MISCELLANEOUS TIMING (τ 1 CLOCK PERIOD)						
$\overline{CS} \downarrow$ (4) To $\overline{DCS} \downarrow$ (4) Propagation Delay (for A3 low)			150	250	ns	CL = 50 pF
$\overline{IACK} \downarrow$ (4) to $\overline{IACKO} \downarrow$ (4) Propagation Delay when Not Requesting Interrupt			150	250	ns	CL = 50 pF
$\overline{BACK} \downarrow$ (4) to $\overline{BACKO} \downarrow$ (4) Propagation Delay when Not Requesting Bus			150	250	ns	CL = 50 pF
\overline{MR} Pulse Width		2 τ				
DINTR, AUTLD, DRQ, \overline{REPLY} Pulse Width		1 τ				
BOW \downarrow (4) or TDB \downarrow (4) Set Up		500			ns	
Waiting INTR \downarrow or $\overline{BUSR} \downarrow$ from STOPR \downarrow				1 τ + 400	ns	CL = 50 pF
INTR \downarrow from DINTR \downarrow				1.5 τ + 400	ns	CL = 50 pF

NOTE: A 1 TTL load is assumed on all output signals

SECTION 2



DM1883 CERAMIC PACKAGE

DM1883 PLASTIC PACKAGE

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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WESTERN DIGITAL

C O R P O R A T I O N

WD2143-01 Four Phase Clock Generator

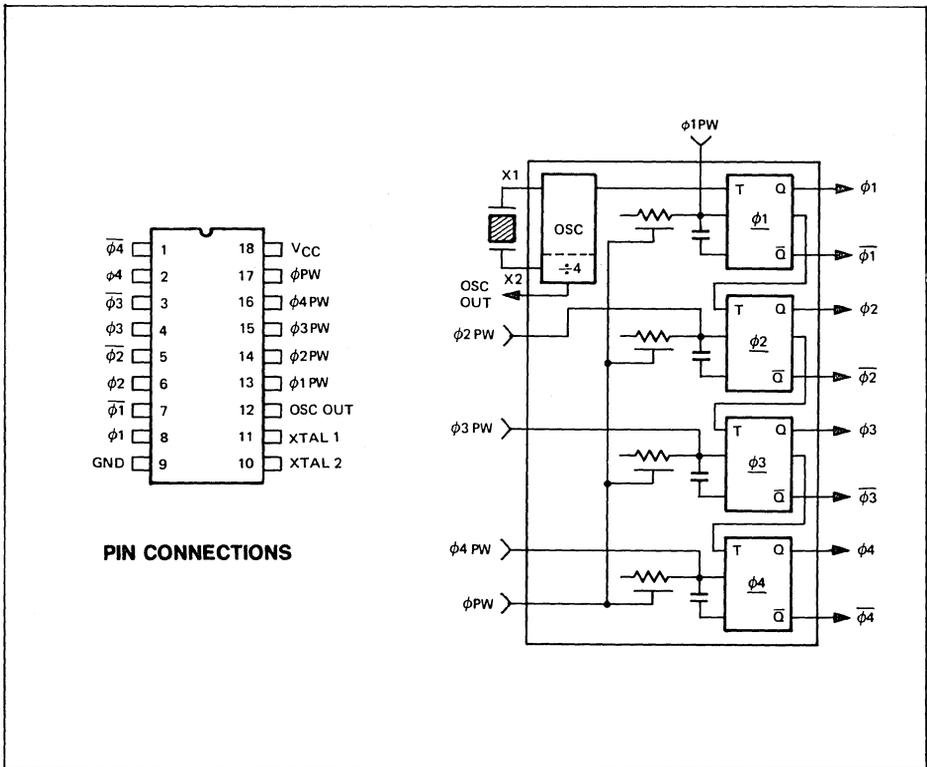
FEATURES

- TRUE AND INVERTED OUTPUTS
- SINGLE 5 VOLT SUPPLY
- TTL COMPATIBLE
- ON CHIP OSCILLATOR
- XTAL OR TTL CLOCK INPUTS
- 3 MHz OPERATION
- TTL CLOCK OUTPUT
- PROGRAMMABLE PULSE WIDTHS
- PROGRAMMABLE PHASE WIDTHS
- NO EXTERNAL CAPACITOR
- NON-OVERLAPPING OUTPUTS

GENERAL DESCRIPTION

The WD2143-01 Four-Phase Clock Generator is a MOS/LSI device capable of generating four non-overlapping clocks. The output pulse widths are controlled by tying an external resistor to the proper control inputs. All pulse widths may be set to the same width by tying the ϕPW line through an external resistor. Each pulse width can also be individually programmed by tying a resistor through the appropriate $\phi 1PW - \phi 4PW$ control inputs. In addition, the OSC OUT line provides a TTL square wave output at a divide-by-four of the crystal frequency.

Z01-10ms 2



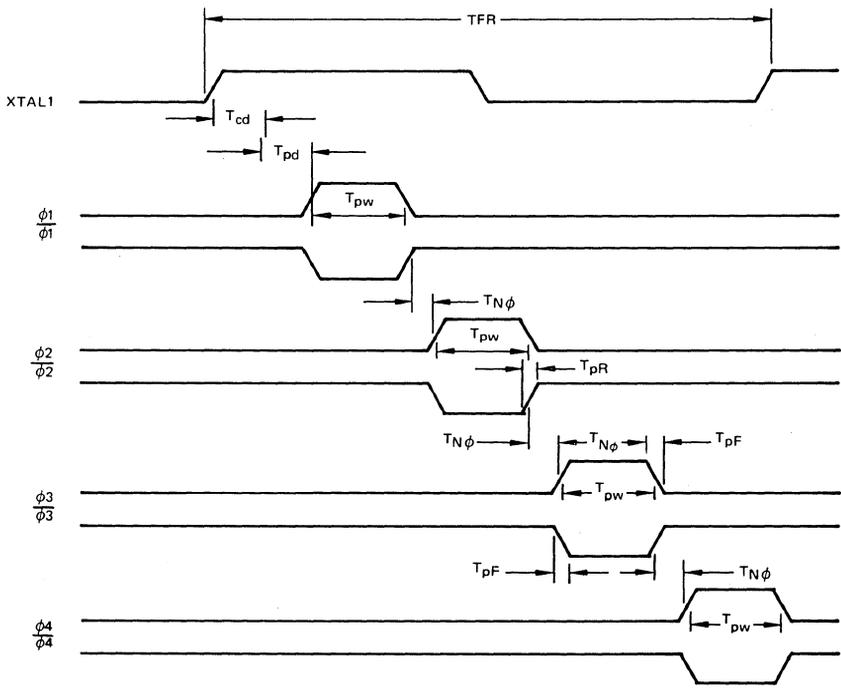
WD2143-01 BLOCK DIAGRAM

PIN NUMBER	SYMBOL	DESCRIPTION
1, 3, 5, 7	$\overline{01}-\overline{04}$	Four phase, non-overlapping outputs. These outputs are inverted (active low).
2, 4, 6, 8	01-04	Four Phase, non-overlapping outputs. These outputs are true (active high).
9	GND	Ground
10, 11	XTAL1 XTAL2	External XTAL connections. An external crystal tied to these pins will cause the oscillator to oscillate at the crystal frequency.
12	OSC OUT	A TTL compatible output that is a divide-by-four of the crystal frequency.
13-16	01PW-04PW	External resistor inputs to control the individual pulse widths of each output. These pins can be left open if 0PW is used.
17	0PW	External resistor input to control all phase outputs to the same pulse widths.
18	V _{CC}	+5V ± 5% power supply input

DEVICE OPERATION

Each of the phase outputs can be controlled individually by tying an external resistor from 01PW-04PW to a +5V supply. When it is desired to have 01 through 04 outputs the same width, the 01PW-04PW inputs should be left open and an external resistor tied from the 0PW (Pin 17) input to +12V.

XTAL1 and XTAL2 can be connected directly to a series-resonant crystal, forcing the internal oscillator to oscillate to the crystal frequency. XTAL2 (pin 11) may also be driven by a TTL square wave with XTAL1 (pin 10) left open. Each of the four phase outputs provide both true and inverted signals, capable of driving 1 TTL load each.



NOTES:
 T_{cd} MEASURED FROM 90% V_{OH} POINTS
 T_{pw} MEASURED FROM 50% V_{OH} POINTS

WD2143-01 TIMING DIAGRAM

SPECIFICATIONS

Absolute Maximum Ratings		Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to the DC electrical characteristics specified.
Operating Temperature	0° to $+70^{\circ}$ C	
Voltage on any pin with respect to Ground	-0.5 to +7V	
Power Dissipation	1 Watt	
Storage Temperature	-55° to $+125^{\circ}$ C	

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = +5V \pm 5\%$ R(\emptyset NPW) or R(\emptyset PW) = 5K, GND = 0V $T_A = 0^\circ$ to 70° C

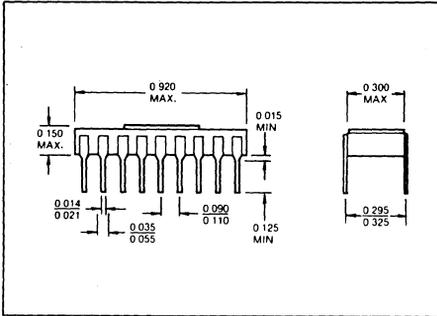
SYMBOL	PARAMETER	MIN.	MAX.	UNITS	CONDITIONS
V_{ol}	TTL low level output		0.4	V	$I_{ol} = 1.6$ ma.
V_{oh}	TTL high level output	2.4		V	$I_{oh} = 100$ ua.
V_{il}	XTAL in low voltage		0.8	V	
V_{ih}	XTAL in high voltage	2.4		V	
I_{cc}	Supply Current		80	ma	All outputs open

SWITCHING CHARACTERISTICS

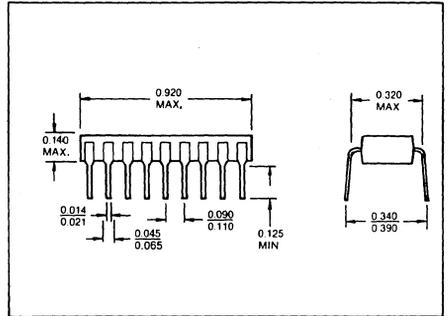
$V_{CC} = 5V \pm 5\%$, GND = 0V $T_A = 0^\circ$ to 70° C

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	CONDITIONS
T_{cd}	XTAL in to OSC out (\uparrow)		100	NS	
T_{pd}	OSC out to $\emptyset 1$		100	NS	

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	CONDITIONS
T_{pw}	Pulse Width (any output)	100		NS	$CL = 30$ pf $\emptyset PW = 5K$
$T_{n\phi}$	Non-Overlap Time	20		NS	
T_{pr}	Rise Time (any output)		30	NS	$CL = 30$ pf
T_{pf}	Fall Time (any output)		25	NS	$CL = 30$ pf
TFR	OSC in Frequency External Resistor		3 100	mHz k.Ω	$\emptyset PW$ or $\emptyset NPW$
T_{pw}	Pulse Width Differential		5	%	$\emptyset PW = 5K$



WD2143L-01 CERAMIC PACKAGE



WD2143M-01 PLASTIC PACKAGE

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WESTERN DIGITAL

C O R P O R A T I O N

WD1510-00, 01 LIFO/FIFO BUFFER REGISTER

FEATURES

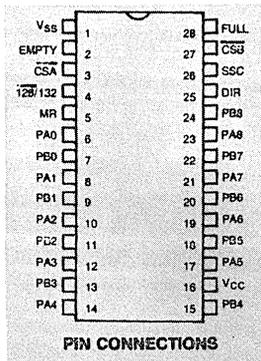
- WORD LENGTH SELECTABLE: 128 OR 132
- 9 BIT WORD WIDTH
- DC TO 650 KHZ (-00), 1 MHz (-01)
- EMPTY AND FULL FLAGS
- THREE-STATE DATA LINES
- 5-VOLT ONLY
- NO EXTERNAL CLOCKS REQUIRED
- TTL COMPATIBLE ON ALL INPUTS AND OUTPUTS
- 28 PIN PLASTIC OR CERAMIC DIP
- MASTER RESET

GENERAL DESCRIPTION

The WD1510 is an MOS/LSI Memory Buffer which is organized as a 9-bit by 128 or 132 word stack. The chip has 2 bidirectional data ports and may be read from or written into either port. Thus, the chip can function as a LIFO from either port or it can function as a FIFO, with data flow from either port A to port B or vice versa. The DIRECTION input pin is used to specify the data flow direction. The WD1510 is fabricated in 5-volt only N-channel technology.

APPLICATIONS

- POINT OF SALE TERMINALS
- COMPUTER-TO-PERIPHERAL BUFFER
- CRT BUFFER MEMORY
- LINE PRINTER BUFFER
- INTERRUPT STACK (LIFO MODE)

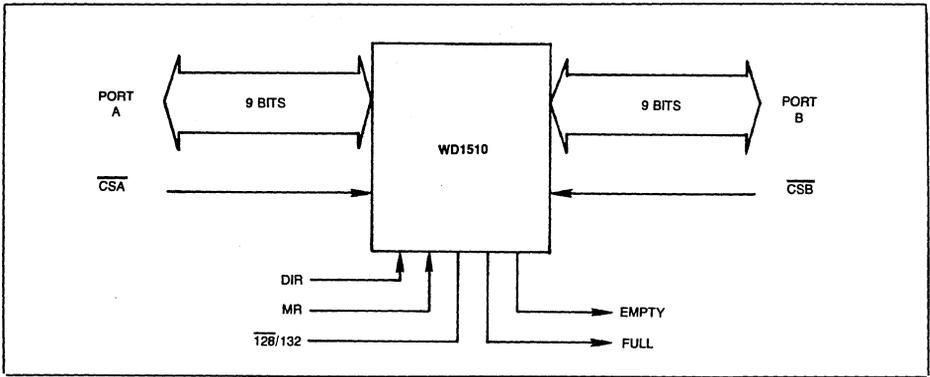


PIN DEFINITIONS

PIN NUMBER	NAME	SYMBOL	FUNCTION
1	VSS	VSS	Ground
2	EMPTY	EMPTY	Indicates when there is no data in the buffer
3	CHIP SELECT PORT A	CSA	Used to select Port A for either a Read or Write operation
4	128 OR 132	128/132	Used to set word length. When low word length = 128, when high word length = 132
5	MASTER RESET	MR	When pulsed will clear the buffer and set the EMPTY pin
6,8,10,12,14,17,19,21,23	PORT A DATA LINES	PA0-PA8	Bidirectional DATA Port for reading or writing data
7,9,11,13,15,18,20,22,24	PORT B DATA LINES	PB0-PB8	Bidirectional DATA Port for reading or writing data
16	V _{CC}	V _{CC}	+5 volts ±.25V
25	DIRECTION	DIR	When low DIR specifies that Port A may be read from and Port B may be written into. When high DIR specifies that Port A may be written into and Port B may be read from
26	SYSTEM SENTINEL™ CHECKOUT	SSC	No connection (For future use)
27	CHIP SELECT PORT B	CSB	Used to select Port B for either a Read or Write Operation
28	FULL	FULL	Indicates that all 132 or 128 words of memory are loaded with data

FEBRUARY, 1981





OPERATION

The WD1510 contains a 132×9 buffer which may be programmed for 128×9 operation. Setting the 128/132 pin to a Logic 0 enables the EMPTY and FULL lines to be activated when 128 bytes are read or written. When the 128/132 line is set to a Logic 1 or left open, the 132 byte operation is enabled. This line contains an internal pull-up resistor of approximately $5K\Omega$.

When the Master Reset Line (pin 5) is set to a Logic 1, all internal counters are reset and the EMPTY Flag is set. Prior to reading or writing data, the DIRECTION Line (pin 25) must be set to select the desired operation:

DIR	PORT A	PORT B
1	WRITE	READ
0	READ	WRITE

To operate the device in the FIFO mode, both Ports must be used. If the DIRECTION Line is set to a Logic 1, then data

is written into Port A and read out of Port B. Reading/Writing to the two ports can be done asynchronously.

In the LIFO mode only one port is used. For example, if using Port A, the DIRECTION Line is set to a Logic 1 to enter data, and is reset to a Logic 0 to read data.

Reading or writing is performed by setting the appropriate \overline{CS} (Chip Select) Line to a Logic 0. After the specified hold time has expired, data may be entered or read on the rising edge of CSA or CSB. In a Read mode, data is valid as long as \overline{CS} remains active. Both Ports return to the high impedance state when \overline{CS} is returned to a Logic 1.

The EMPTY Line (Pin 2) and the FULL Line (Pin 28) are used as status or interrupt lines to determine the status of the buffer. When both EMPTY and FULL are at a Logic 0, the buffer contains 1 thru 127 bytes ($128/132 = 0$) or 1 thru 131 bytes ($128/132 = 1$).

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

V_{CC} with respect to V_{SS} (Ground)	= +7V
Max Voltage on any Pin with respect to V_{SS}	= -0.5V to +7V
Operating Temperature	= 0°C to 70°C
Storage Temperature	= -55°C to +125°C

Operating Characteristics (DC)

$$TA = 0^{\circ}C \text{ to } 70^{\circ}C, V_{SS} = 0V, V_{CC} = +5V \pm .25V$$

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
I_{LI}	Input Leakage			10	μA	$V_{IN} = V_{CC}$ $V_{OUT} = V_{CC}, V_{SS}$
I_{LO}	Output Leakage			10	μA	
V_{IH}	Input High Voltage	2.4			V	$I_O = -40\mu A$ $I_O = 1.6 \text{ mA}$ All outputs open
V_{IL}	Input Low Voltage			.7	V	
V_{OH}	Output High Voltage	2.4			V	
V_{OL}	Output Low Voltage			.4	V	
I_{CC}	Power Supply Current		125	200	mA	

A.C. TIMING CHARACTERISTICS

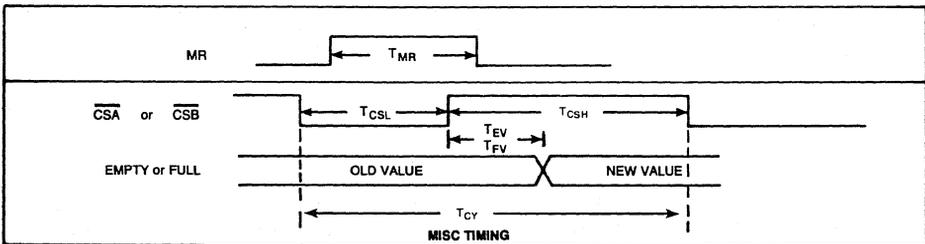
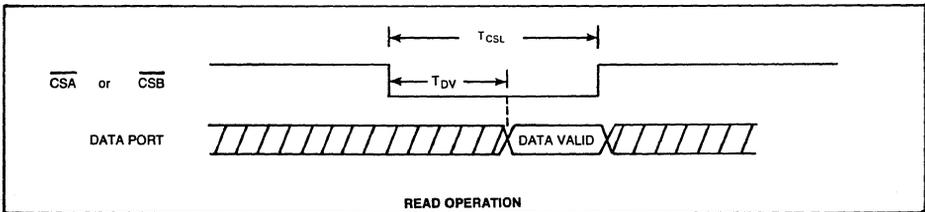
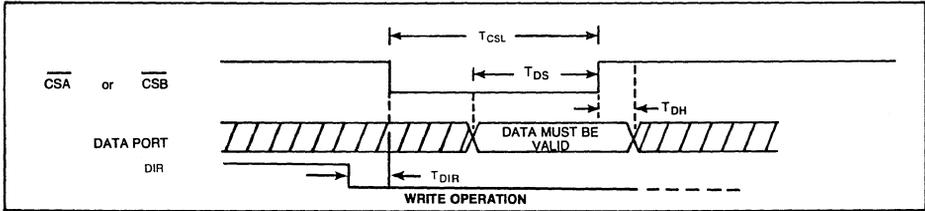
TA = 0°C to 70°C, V_{SS} = 0V, V_{CC} = +5V ± .25V, V_{OH} = 2.0V, V_{OL} = 0.8V

WD1510-00

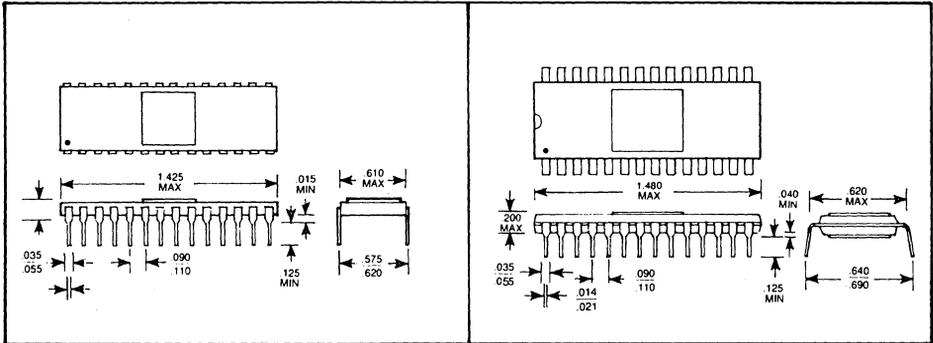
SYMBOL	CHARACTERISTICS	MIN	TYP	MAX	UNITS	CONDITIONS
T _{MR}	Master Reset Time	400			NS.	
T _{DV}	Data Valid from CS			550	NS.	
T _{DH}	Data Hold from CS	150			NS.	
T _{DIR}	DIR Setup Time	1500			NS.	
T _{EV}	EMPTY Valid from CS			550	NS.	
T _{FV}	FULL Valid from CS			550	NS.	
T _{CSL}	CS Pulse Width Low	600			NS.	
T _{CSH}	CS Pulse Width High	600			NS.	
T _{CY}	CS Cycle Time	1540			NS.	
T _{DS}	Data Setup Time	80			NS.	
F _{MAX}	Data Transfer Rate			650	KHZ	

WD1510-01

T _{MR}	Master Reset Time	250			NS.	
T _{DV}	Data Valid from CS			350	NS.	
T _{DH}	Data Hold from CS	100			NS.	
T _{DIR}	DIR Setup Time	1000			NS.	
T _{EV}	EMPTY Valid from CS			350	NS.	
T _{FV}	FULL Valid from CS			350	NS.	
T _{CSL}	CS Pulse Width Low	500			NS.	
T _{CSH}	CS Pulse Width High	500			NS.	
T _{CY}	CS Cycle Time	1000			NS.	
T _{DS}	Data Setup Time	50			NS.	
F _{MAX}	Data Transfer Rate			1	MHZ	



S-T-O-N 2



WD1510E-XX CERAMIC PACKAGE

WD1510F-XX PLASTIC PACKAGE

XX

00 650kHz, version 1

01 1.0 MHz version

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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Introduction to

ADVANCED SYSTEMS DIVISION

The Advanced Systems Division markets a complete line of microcomputer system products. These products combine file management, telecommunications, high level language, and microprocessor expertise into complete computer systems.

In 1974 Western Digital developed the first 16 bit microprocessor, the LSI-11* for Digital Equipment Corporation, and in 1976 developed the WD16 for Alpha Micro Corporation, both of which are still in volume production.

The Pascal MICROENGINE, announced in 1978, signalled Western Digital's entry into the sophisticated Microcomputer Systems Marketplace. The MICROENGINE was the first microcomputer designed exclusively to maximize performance of Pascal high level language software programs. Pascal has rapidly become one of the most popular computer languages.

In 1980 the Modular MICROENGINE was introduced. This product is implemented with one function per board (processor, memory, disk controller etc.) to maximize versatility, expandability, and maintainability. It continues the tradition of architecture optimized to high level language execution.

The Advanced Systems Division is operating its future product strategy around continued use of Pascal, and use of the new programming language, Ada. Ada is a language originally defined by the US Department of Defense as part of its Standardization program. Functionally a superset of Pascal, Ada** extends Pascal in four major areas: error recovery with exception handling; separately compiled packages; multi task synchronization via rendezvous; and strongly enforced user defined data types.

Advanced System Division products will significantly improve programmer and user productivity in the 80's.

* LSI-11 is a trademark of Digital Equipment Corporation.

**Ada is a trademark of the U.S. Department of Defense.



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ADVANCED SYSTEMS DIVISION

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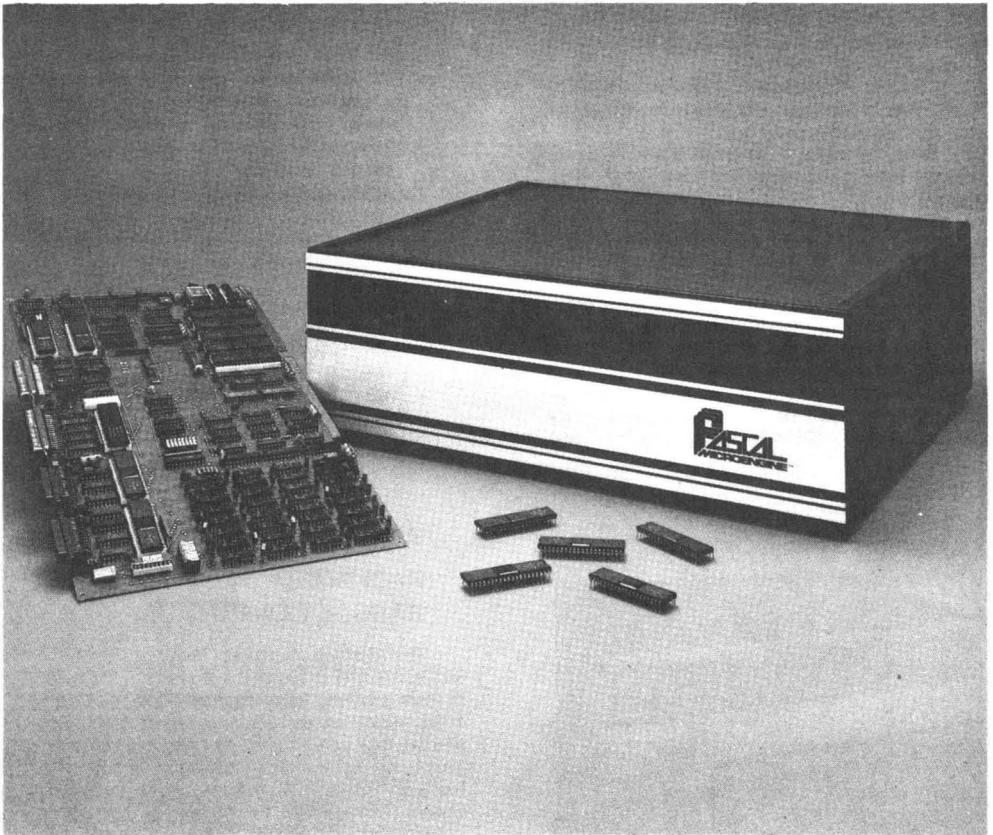


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WESTERN DIGITAL
CORPORATION

PASCAL **MICROENGINE™**

MICROCOMPUTER PRODUCT LINE



SOLUTIONS
3

THE PASCAL MICROENGINE CONCEPT

Western Digital's Pascal MICROENGINE™-M Product Family is the only Microcomputer specifically designed to optimize execution of modern, high order language programs.

Thus, the Pascal MICROENGINE user enjoys the benefits of speed and ease of use in developing and maintaining systems in a universally recog-

nized, block structured language, plus the memory efficiency and performance advantages normally available only in assembly language.

The machine language of the Pascal MICROENGINE is P-code, the "ideal" Pascal intermediate language, and thus the MICROENGINE is the ideal Pascal machine.

WD/9000

MICROPROCESSOR CHIP SET

The WD/9000 Pascal MICROENGINE Microprocessor is a 16 bit, MOS/LSI chip set that executes Pascal programs at speeds five to ten times faster than equivalent systems using conventional architecture.

The chip set consists of five 40-pin dual-in-line LSI components:

ARITHMETIC COMPONENT contains ALU, micro-instruction decode, register file and paths to control processor operation.

CONTROL PROCESSOR contains control circuitry, macro-instruction decode, micro-instruction counters, and I/O control logic.

THREE MICROM'S (each 22 bits × 512) contain the high speed microcode which implements P-code.

MICROENGINE chip set features include 16-bit user-defineable I/O and data paths; single—and mult—byte instruction formats; direct addressing to 128k bytes of memory; stack architecture for reentrant and recursive programs; four-level nested interrupt structure; hardware multiply/divide (16 bit integer) and floating point (IEEE single precision standard) instructions; memory mapped input/output capability; and TTL-compatible three-state interface. The MICROENGINE uses +5v, -5v, and +12v power supply voltages.

WD/900

SINGLE BOARD COMPUTER

The Pascal MICROENGINE is also available on a Single Board Computer, the WD/900. This implementation reduces end product design and development costs in many applications where a standard configuration can be employed. The WD/900 contains the following:

Pascal MICROENGINE CPU

64K Bytes of RAM Memory

Two RS-232 asynchronous/synchronous ports (110-19.2K baud-full duplex). Synchronous or asynchronous operation, odd or even parity, SYN stripping enabled/disabled, character length (5 to 8 bits), and switch selectable for baud rate

Two 8-bit parallel ports (500 KHz maximum data rate)

Floppy disk controller with direct memory access (DMA), switch selectable for:

Single or double density 8" floppy

Single or double sided operation

1 to 4 drives

Compatible with most standard floppy models

IBM soft sectored format

Up to 4MB floppy disk storage

A 64KB memory expansion board is also available

WD/90

PACKAGED PASCAL COMPUTER

The desktop computer features the 16-bit MICROENGINE processor, 32K words (64K bytes) of RAM memory, fully-integrated floppy disk controller, two RS-232 asynchronous/synchronous ports, and two 8-bit parallel ports all on a single 8" × 16" board, plus a power supply, packaged in a low-profile (5¼" high × 16¼" × 13½") enclosure; UCSD Pascal Software System (Version III.O) on floppy diskette; and the WD/90 Pascal MICROENGINE Reference Manual.



PASCAL

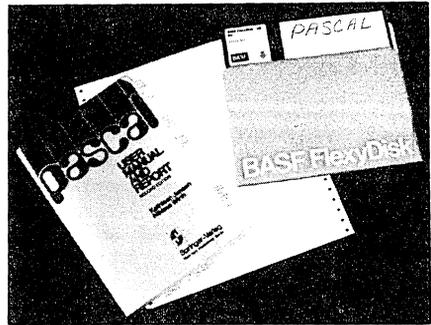
Pascal is a universally used structured programming language developed by Niklaus Wirth and defined in the Pascal User Manual and Report. The language is suited to a broad range of applications: systems programming, real-time control, data communication, business systems, education, and most other applications. It encourages increased programmer productivity and more reliable, maintainable, and transportable programs. Pascal combines the data structuring capabilities of Cobol, the block structuring of PL/I, and the expression handling of Fortran into a concise, efficient language.

The Pascal MICROENGINE family is built around the UCSD Pascal compiler and System Software—the most widely used Pascal system for small computers. UCSD's compiler contains the Jensen-Wirth nucleus plus additional features which extend Pascal's capabilities. Some of these language extensions include:

- Long integers (up to 36 characters)
- Data file access
- Automatic loading of program segments from disk storage
- Separate compilation and linking of Pascal modules
- I/O and interrupt programming in Pascal
- Program synchronization via SIGNAL and WAIT ON SEMAPHORE instructions

System design engineers using the Pascal MICROENGINE family for Pascal-based system development realize the performance benefits of assembly language system development and the cost benefits of Pascal systems. These include:

HIGH PERFORMANCE direct execution of



P-code on the 16-bit MICROENGINE processor provides high system throughput.

LOWER SOFTWARE DEVELOPMENT COST as a high-level language with strong data typing, extensive error checking, and automatic reentrancy and recursion, Pascal increases programmer productivity.

SHORTENED DEVELOPMENT SCHEDULES critical software schedules are shortened.

LOWER UPDATE/MODIFICATION COSTS Pascal programs cost less to change than those programmed in alternative languages.

EFFICIENT MEMORY UTILIZATION P-machine efficiency means that programs written in Pascal for the MICROENGINE family often use less memory than even assembly language programs for other architectures.

TRANSPORTABILITY programs written in the widely used UCSD Pascal system may be executed on the other Pascal-based systems.

IMPROVED RELIABILITY since Pascal programs are simpler statements of the algorithm to be executed, they are less likely to fail in costly field situations.

SECTION 3

COMPARISON OF DIRECT P-CODE EXECUTION TO OTHER TECHNIQUES

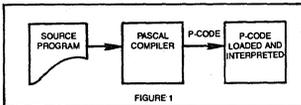


FIGURE 1 Most microprocessor Pascal compilers are interpretive: the Pascal compiler produces P-code which is then decoded and executed by a software interpreter. Interpretation of each P-code instruction requires execution of multiple processor instructions.

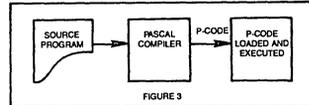


FIGURE 3 The Pascal MICROENGINE microprocessor does not use the approaches listed. Instead the Pascal compiler converts programs to P-code which the MICROENGINE microprocessor directly executes as its native instruction set.

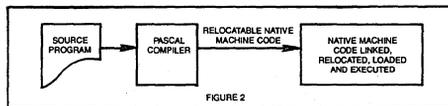


FIGURE 2 Other Pascal compilers convert Pascal source programs into the target processor's machine language. Thus Pascal programs are force fit onto architectures not efficient for Pascal, resulting in execution of more instructions for a given function.

WESTERN DIGITAL'S UCSD PASCAL SOFTWARE SYSTEM

Western Digital's UCSD Pascal Software System is a complete software development and program execution system that runs on the "ideal" Pascal P-code machine, as defined by the University of California at San Diego (UCSD).

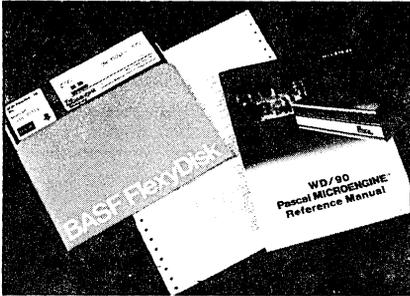
This "ideal" Pascal P-code machine has been implemented in hardware as the Western Digital Pascal MICROENGINE. Because Pascal programs run directly on a stack machine designed for Pas-

cal, the system is very efficient, has low memory requirements, and out performs equivalent machines with conventional architecture.

In addition to an operating system the Pascal Software System provides software tools to support program development, debug, and execution; manipulation of files; and data and text processing.

Western Digital's UCSD Pascal Software System includes:

- Operating System
- Pascal Compiler
- Multi-tasking, concurrency primitives, and interrupts
- Screen and line oriented editors
- File handler
- Library and Linker systems
- Software debugger
- Utilities
- Efficient execution of Pascal programs and minimal memory requirements
- Supports up to two serial devices, one parallel device, up to four single or double sided and single or double density drives, and 64K bytes of memory
- Can be configured for specific CRT or TTY terminals



WESTERN DIGITAL CORPORATION

Western Digital is an industry leader in the fields of high order languages, mass storage controllers, telecommunications subsystems, and energy management devices. We serve over 1300 customers in 23 countries through 100 sales representatives.

In addition to Pascal Microprocessors and Mi-

crocomputers, our sophisticated products include custom microprocessors; floppy and Winchester disk controllers; gate arrays; X.25, SDLC/HDLC/ADCCP, Async/Bisync and ARINC avionics communications controllers, UARTS, and USARTS; custom industrial controllers, digital thermostats, and industrial timers.

WESTERN DIGITAL
CORPORATION

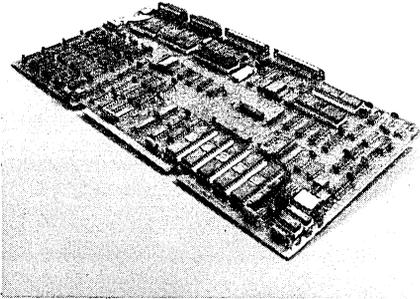
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NOVEMBER, 1980

WESTERN DIGITAL

C O R P O R A T I O N

Pascal MICROENGINE™ Product



PASCAL MICROENGINE™ 16 BIT PASCAL MICROCOMPUTER

FEATURES

- DIRECT EXECUTION OF PASCAL P-CODE.
- 16 BIT STACK ORIENTED ARCHITECTURE
- UP TO 128K BYTES OF MEMORY
- 1 TO 4 DISK DRIVES
- UP TO 4 MB DISK STORAGE
- SINGLE OR DOUBLE DENSITY DISKETTES
- SINGLE OR DOUBLE SIDED DISKETTES
- TWO FULL DUPLEX SERIAL I/O PORTS (50-19.2K BAUD)
- TWO PARALLEL I/O PORTS (500K BYTE/SEC MAX DATA RATE)
- INTERRUPT DRIVEN DISC AND I/O
- HARDWARE FLOATING POINT
- HARDWARE MULTIPLY/DIVIDE
- 2.5 MHZ FOUR PHASE CLOCK

DESCRIPTION

The PASCAL MICROENGINE is the first microcomputer specifically designed to optimize performance of high order languages. The machine language of the MICROENGINE is Pascal P-code.

Thus the user enjoys the benefits of developing and maintaining systems in a modern, universally recognized high order language; plus the performance and memory efficiency advantages of machine language.

The MICROENGINE is available as a single board microcomputer with the 16 bit, stack oriented processor, 64K bytes of memory, a floppy disk controller, two full duplex serial and two parallel I/O ports.

An expansion card is also available which provides an additional 64K bytes of memory for more user program space and faster execution.

Both the MICROENGINE and expanded MICROENGINE are also available in a desk top cabinet with power supply.

NO-TOMS
3

SPECIFICATIONS

PROCESSOR

Stack Architecture

All operations are performed on the hardware stack

Instructions (P-code operators)

The machine language of the PASCAL MICROENGINE™ is the Pascal P-Code operator set.

All instructions are one byte long, followed by zero to three parameters.

Constant One Word Loads

SDLC Short Load Word Constant
LDCN Load Constant Nil
LDCB Load Constant Byte
LDCI Load Constant Word
LCA Load Constant Address

Local One Word Loads and Store

SLDLI . . 16 Short Load Local Word
LDL Load Local Word
LLA Load Local Address
STL Store Local Word

Global One Word Loads and Stores

SLDOI . . 16 Short Load Global Word
LDO Load Global Word
LAO Load Global Address
SRO Store Global Word

Intermediate Store

LOD Load Intermediate Word
LDA Load Intermediate Address
STR Store Intermediate Word

Indirect One-Word Loads and Store

STO Store Indirect

Extended One Word Loads and Store

LDE Load Word Extended
LAE Load Address Extended
STE Store Word Extended

Multiple Word Loads and Stores (Sets & Reals)

LDC Load Multiple Word Constant
LDM Load Multiple Words
STM Store Multiple Words

Byte Arrays

LDB Load Byte
STB Store Byte

Record and Array Indexing Assignment

MOV Move Words
SINDO . . 7 Short Index and Load Word
IND Static Index and Load Word
INC Increment Field Pointer
IXA Index Array
IXP Index Packed Array
LDP Load a Packed Field
STP Store into a Packed Field

Logicals

LAND Logical AND
LOR Logical OR
LNOT Logical NOT
LEUSW Compare Unsigned Words less than or Equal
GEUSW Compare Unsigned Words Greater than or Equal
BNOT Bit Not

Integers

ABI Absolute Value of Integer
NGI Negate Integer
DUP1 Copy Integer
ADI Add Integers
SBI Subtract Integers
MPI Multiply Integers
DVI Divide Integers
MODI Modulo Integers
CHK Check Against Subrange Bounds
EQUI Compare Integers Equal
NEQI Compare Integers Not Equal
LEQI Compare Integers less than or equal to
GEQI Compare Integers Greater than or equal

Reals

FLT Float top of Stack
TNC Truncate Real
RND Round Real
ABR Absolute Value of Real
NGR Negate Real
DUP2 Copy Real
ADR Add Reals
SBR Subtract Reals
MPR Multiply Reals
DVR Divide Reals
EQUREAL Compare Reals Equal
LEQREAL Compare Real Less than or Equal
GEQREAL Compare Real Greater than or Equal

Sets

ADJ	Adjust Set
SRS	Build Subrange set
INN	Set Membership
UNI	Set Union
INT	Set Intersection
DIF	Set Difference
EQUWPWR	Set Compare Equal
LEQPWR	Set Compare Less than or Equal (Subset of)
GEQPWR	Set Compare Greater than or Equal (Superset of)

Byte Arrays

EQUBYT	Byte Array Compare Equal
LEQBYT	Byte Array Compare Less Than or Equal
GEQBYT	Byte Array Compare Greater than or Equal

Jumps

UJP	Unconditional Jump
FJP	False Jump
EFJ	Equal False Jump
NFJ	Not Equal False Jump
UJPL	Unconditional Long Jump
FJPL	False Long Jump
XJP	Case Jump

Procedure & Function Calls & Returns

CPL	Call Local Procedure
CPG	Call Global Procedure
CPI	Call Intermediate Procedure
CXL	Call Local External Procedure
CXG	Call Global External Procedure
CXI	Call Intermediate External Procedure
CPF	Call Formal Procedure
RPV	Return from User Procedure
LSL	Load Static Link On To Stack

System Control

SIGNAL	Signal Semaphore
WAIT	Wait on Semaphore
LPR	Load Processor Register
SPR	Store Processor Register

Debugger

BPT Break Point

Miscellaneous

NOP	No Operation
SWAP	Swap Word Top of Stack with Word Top of Stack -1

MEMORY

Size 64K or 128K Bytes
Cycle Time: 1200 ns

SERIAL I/O PORTS

Baud Rates: 50-19,200 baud
Character Size: 5-11 bits
Full Duplex
Interfaces any RS232 compatible device

PARALLEL I/O PORTS

8 bits In
8 bits Out
Data Rate: Up to 500 K Bytes/sec.

Interfaces to Following Line Printers:

Centronics 700,701, 737 or equivalent

FLOPPY DISK

DMA Operation
Up to 4 drives, switch selectable for

Single or dual sided, and
Single or dual density

Up to 4 MB capacity
Interfaces to Following Drives: Shugart 800 and 850
series, and all compatible drives such as
REMEX 4000 series, Qume Datatrak 8, CDC 9406-
1,9406-3, 9404-B

MECHANICAL

Single board computer 8" × 16"
Expansion Card 8" × 16"
Desk Top Computer 5¼" H × 16¼" W × 13" D

ENVIRONMENT

Operating Range 0-50° C
Humidity 0-95%

ELECTRICAL

Power Requirements	+5V	-5V	+12V	-12V
Single Board Computer	2.0A	.5mA	500mA	100mA

CONNECTORS

Serial Ports: DB-25S 25 Pin right angle con-
nector

Parallel and Floppy Disk Ports: DC-375 37 Pin
right angle connector



ORDER INFORMATION

WD900 (X) * PASCAL MICROENGINE Single Board Computer

WD90 (X) * PASCAL MICROENGINE Desk Top Computer 110V

WD95 (X) * PASCAL MICROENGINE Desk Top Computer 220 V

* (X) indicates diskette option:

- a = 8" Single Density Single Sided
- b = 8" Single Density Double Sided
- c = 8" Double Density Single Sided
- d = 8" Double Density Double Sided

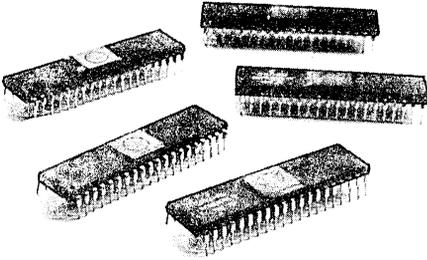
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WESTERN DIGITAL

C O R P O R A T I O N

Pascal MICROENGINE™ Product



THE WD9000 CHIP SET 16 BIT Pascal MICROPROCESSOR

FEATURES

- DIRECT EXECUTION OF PASCAL INTERMEDIATE CODE (P-CODE)
- HIGH LEVEL LANGUAGE PROGRAMMING DEVELOPMENT SPEED AND EASE
- ASSEMBLY LANGUAGE EXECUTION EFFICIENCY
- HIGH PERFORMANCE 16 BIT MICROPROCESSOR
- STACK-BASED ARCHITECTURE FOR REENTRANT AND RECURSIVE PROGRAMS
- EXECUTES FULL UCSD PASCAL, VERSION III.0
- PROGRAM TRANSPORTABILITY
- PROGRAM SIZE TO 128K BYTES
- 3.0 MHZ FOUR-PHASE CLOCK
- FOUR-LEVEL INTERRUPT STRUCTURE
- IEEE HARDWARE MULTIPLY/DIVIDE
- HARDWARE FLOATING POINT
- SINGLE AND MULTI-BYTE INSTRUCTIONS
- TTL COMPATIBLE THREE-STATE INTERFACE
- MEMORY MAPPED I/O

DESCRIPTION

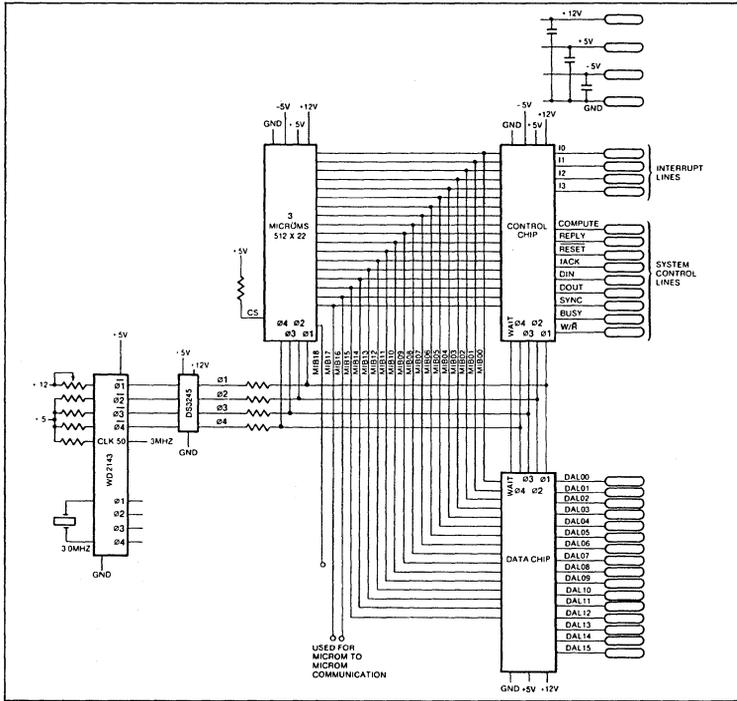
The WD9000 PASCAL MICROENGINE™ Microprocessor is a 16 bit MOS/LSI chip set that executes programs written in Pascal at speeds five or more times greater than equivalent systems using conventional architectures. This is because the MICROENGINE chip set is designed to be the ideal P-code (Pascal Psuedo code) machine. Its machine language is the P-code produced by the UCSD Pascal compiler.

The Chip Set consists of five LSI components:

- Arithmetic Component — contains the arithmetic logic unit, microinstruction decode, register file, and paths to control processor operation.
- Control Processor — contains macroinstruction decode, portions of the control circuitry, microinstruction counters, and I/O control logic.
- MICROM Components — three high-speed, 512 × 22 bit, custom MICROMS, microcoded for direct execution of UCSD Pascal Version III.0 P-Code.

The MICROENGINE Microprocessor chip set is ideal for all applications requiring 16 bit performance, assembly language efficiency and high level language speed of program development and ease of use.





PIN ASSIGNMENTS The following are pin assignments for the Pascal MICRO-ENGINE™ Microprocessor Chip Set:

DATA CHIP PIN ASSIGNMENTS

PIN NO.	SIGNAL	PIN NO.	SIGNAL	PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	ø3	11	DAL08	21	ø2	31	MIB07
2	V _{BB}	12	DAL09	22	WAIT	32	MIB06
3	DAL00	13	DAL10	23	MIB15	33	MIB05
4	DAL01	14	DAL11	24	MIB14	34	MIB04
5	DAL02	15	DAL12	25	MIB13	35	MIB03
6	DAL03	16	DAL13	26	MIB12	36	MIB02
7	DAL04	17	DAL14	27	MIB11	37	MIB01
8	DAL05	18	DAL15	28	MIB10	38	MIB00
9	DAL06	19	V _{SS}	29	MIB09	39	V _{DD}
10	DAL07	20	ø4	30	MIB08	40	ø1

MICROM CHIP PIN ASSIGNMENTS

PIN NO.	SIGNAL						
1	ø3	11	MIB16	21	ø2	31	MIB06
2	V _{BB}	12	MIB17	22	V _{CC}	32	MIB05
3	NC	13	MIB18	23	CS	33	MIB04
4	NC	14	NC	24	NC	34	MIB03
5	NC	15	NC	25	NC	35	MIB02
6	NC	16	NC	26	MIB11	36	NC
7	MIB15	17	NC	27	MIB10	37	MIB01
8	MIB14	18	NC	28	MIB09	38	MIB00
9	MIB13	19	V _{SS}	29	MIB08	39	V _{DD}
10	MIB12	20	ø4	30	MIB07	40	ø1

CONTROL CHIP PIN ASSIGNMENTS

PIN NO.	SIGNAL						
1	ø3	11	MIB16	21	ø2	31	MIB07
2	V _{BB}	12	REPLY	22	V _{CC}	32	MIB06
3	I3	13	WAIT	23	MIB16	33	MIB05
4	I2	14	DOUT	24	MIB14	34	MIB04
5	I1	15	W/R	25	MIB13	35	MIB03
6	I0	16	IACK	26	MIB12	36	MIB02
7	MIB17	17	SYNC	27	MIB11	37	MIB01
8	BUSY	18	DIN	28	MIB10	38	MIB00
9	COMPUTE	19	V _{SS}	29	MIB09	39	V _{DD}
10	RESET	10	ø4	30	MIB08	40	ø1

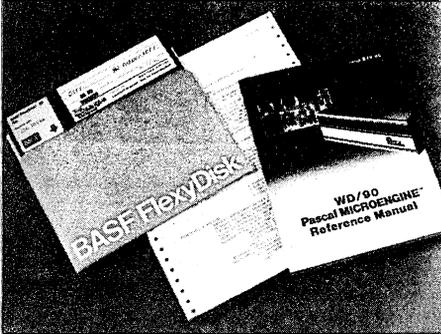
SIGNAL DESCRIPTIONS

DAL	DATA/ADDRESS LINES
MIB	MICRO INSTRUCTION BUS
NC	NO CONNECTION
CS	CHIP SELECT
IO-3	INTERRUPT LEVELS
W/R	WRITE/READ
ø	CLOCK PHASES
V _{DD} , V _{BB} , V _{SS} , V _{CC}	VOLTAGE LINES
IACK	INTERRUPT ACKNOWLEDGE
SYNC	I/O SYNCHRONIZATION
DIN	DATA IN
BUSY	INHIBIT I/O OPERATIONS
COMPUTE	SINGLE INSTRUCTION MODE
W/R	CONTROL TO DATA CHIP INTERFACE
DOUT	DATA OUT
REPLY MEMORY	I/O ACKNOWLEDGE
RESET	MASTER RESET

WESTERN DIGITAL

C O R P O R A T I O N

Pascal MICROENGINE™ Product



PASCAL SYSTEM SOFTWARE

UCSD LEVEL III.0
COMPATIBLE TEXT PROCESSING,
SOFTWARE DEVELOPMENT,
AND PROGRAM EXECUTION SYSTEM

FEATURES

- OPERATING SYSTEM
- PASCAL COMPILER
- MULTI-TASKING, CONCURRENCY PRIMITIVES, AND INTERRUPTS
- SCREEN AND LINE ORIENTED EDITORS
- FILE HANDLER
- LIBRARY AND LINKER SYSTEMS
- SOFTWARE DEBUGGER
- UTILITIES
- EFFICIENT EXECUTION OF PASCAL PROGRAMS AND MINIMAL MEMORY REQUIREMENTS
- SUPPORTS UP TO TWO SERIAL DEVICES, ONE PARALLEL DEVICE, UP TO FOUR SINGLE OR DOUBLE SIDED AND SINGLE OR DOUBLE DENSITY DRIVES, AND 64K OR 128K BYTES OF MEMORY
- CAN BE CONFIGURED FOR SPECIFIC CRT OR TTY TERMINALS

DESCRIPTION

Western Digital's UCSD Pascal Software System is a complete software development and program execution system that runs on the "ideal" Pascal P-code machine, as defined by the University of California at San Diego (UCSD).

This "ideal" Pascal P-code machine has been implemented in hardware as the Western Digital Pascal Microengine™. Because Pascal programs run directly on a stack machine designed for Pascal, the system is efficient, has low memory requirements, and out performs equivalent machines with conventional architecture.

In addition to an operating system the Pascal software system provides software tools to support program development, debugging, and execution, manipulation of files, and data and text processing.

3
Z-O-T-C-M-G

Pascal Compiler

The Pascal compiler compiles Pascal source programs into P-code that is directly executed by the MICROENGINE. The UCSD Pascal language contains the Niklaus Wirth nucleus with additional features to extend its capabilities. Some of the language extensions are:

- strings
- long integers (up to 36 decimal digits)
- random file access
- automatic loading of program segments from disk storage
- separate compilation and linking of Pascal modules
- I/O and interrupt programming
- program synchronization via SIGNAL and WAIT on semaphores
- multi-tasking via START of a Pascal process

Operating System

The operating system is a single user system that supports the capabilities provided by the level III.0 UCSD Pascal compiler. The operating system allows multiple tasks to be operating concurrently based on priority. It supports type ahead queues for the serial ports. Sequential and random access to files is provided.

File Handler

The file handler allows manipulation of the workfile, maintenance of files and diskettes, and transfer of files to diskette, printer, and terminals.

Screen Editor

The screen oriented editor is designed for use with video display terminals to insert, delete, and modify text. It is well suited to program development and text processing. Some of the features provided are:

- insert text
- delete text
- change text
- margin paragraphs
- find a target string
- replace a target string with another string
- move text in a file

- make copies of text
- include any portion of the text from another file
- conveniently move through the file
- set and jump to markers in a file

Line Editor

The line oriented editor is provided for systems that do not have a video terminal or where the video terminal runs at a slow baud rate. Its capabilities are similar to the screen oriented editor.

Debugger

The debugger provides interactive settings and removal of breakpoints at user specified positions in the program. It may be invoked upon detection of a run time error for inspection of program status. The debugger performs memory and I/O register inspection, stack and dynamic linkage chaining, and program dump capabilities.

Library and Linker Systems

With the Library and Linker systems the user can make libraries of frequently used subroutines. The subroutines are then linked into the program before run time. Also, programs can be divided into modules that are separately compiled and then linked.

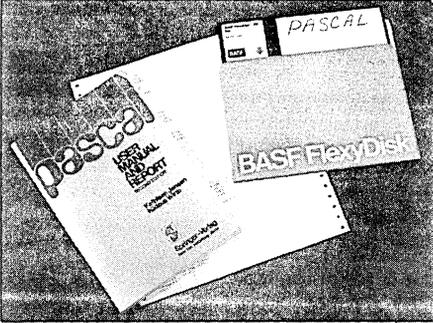
Utilities

A number of utilities are provided including utilities to:

- configure a system to a particular terminal
- list the linker information in a library or code file
- disassemble a program to list the P-code it contains
- copy the system boot to a new diskette
- maintain duplicate directories on a diskette for backup purposes
- dump and/or patch any file in hex or ASCII
- format a single or double density, single or double sided diskette.

WESTERN DIGITAL C O R P O R A T I O N

Pascal MICROENGINE™ Product



PASCAL COMPILER UCSD LEVEL III.0 COMPATIBLE PASCAL COMPILER

FEATURES

- HIGH LEVEL STRUCTURED PROGRAMMING LANGUAGE
- EFFICIENT EXECUTION AND MEMORY UTILIZATION ON THE PASCAL MICROENGINE
- LOWER PROGRAM DEVELOPMENT AND UPDATE/MODIFICATION COSTS
- STANDARDIZATION PROVIDES TRANSPORTABILITY
- ENCOURAGES SELF-DOCUMENTING PROGRAMS AND TOP DOWN DESIGN
- POWERFUL DATA TYPES
- EXTENSIVE ERROR CHECKING
- SEVERAL CONTROL STRUCTURES
- MULTI-TASKING, CONCURRENCY PRIMITIVES, AND INTERRUPTS
- PROGRAMMATIC ACCESS TO I/O PORTS
- PROGRAM SEGMENTATION FOR MEMORY OVERLAYS
- MODULARITY
- EXPANDED I/O CAPABILITIES

DESCRIPTION

Pascal is a universally used structured programming language developed by Niklaus Wirth and defined in the Pascal User Manual and Report.

The language is suited to a broad range of applications: systems programming, real-time control, data communication, business systems, education, and most other applications. Its use encourages increased programmer productivity and more reliable, maintainable, and transportable programs.

Pascal combines the data structuring capabilities of Cobol, the block structuring of PL/1, and the expression handling of Fortran into a concise, efficient language.

Western Digital's Pascal Microengine Supports all features of level III.0 UCSD (University of California at San Diego) Pascal.

3 ZONE

SPECIFICATIONS

Variables and Data Types

Pascal has extensive data types. Type checking helps to ensure correct programs. Several pre-defined types for variables are available. These include real, integer, boolean, character, string, and long integer (up to 36 decimal digits). The user can define his own types such as arrays of a certain type, enumerated types (an ordered set of values), subrange of a scalar type, sets, and records made up of one or more fields of different types. Identifiers with constant values can also be defined. Each variable must be declared before its first use to allow for extensive type checking and error detection and to encourage self-documenting programs. Identifier names of any length are allowed although only 8 characters are significant.

Procedures and Functions

Procedures and functions are provided to facilitate structured programming, and programs that are easier to understand and debug. Procedures allow the user to group Pascal declarations and statements together and give this grouping a descriptive name by which it will be invoked. Functions provide the same capability, but will return a value when called. Procedures and functions can be nested several layers deep. Recursion (a procedure or function calling itself) is allowed.

Control Structures

Several control structures are provided. They include:

- IF <condition> THEN ... ELSE ...
- CASE <selector> OF ...
- REPEAT ... UNTIL <condition>
- WHILE <condition> DO ...
- FOR <variable> := <starting value> TO <ending value> DO ...
- WITH <record> DO ...

File Handling and I/O Capabilities

With UCSD Pascal, files can be programmatically named, opened, closed, read, and written. Sequential and random access to files is provided. Files on all I/O devices, including disk files, terminals, and printers are treated identically. Low level I/O for direct physical access to I/O devices is provided.

Memory Mapped I/O

UCSD Pascal's ability to access any memory location through case variant records combined with the MICROENGINE's memory mapped I/O allows programmatic access to I/O ports.

Multi-tasking, Concurrency Primitives, and Interrupts

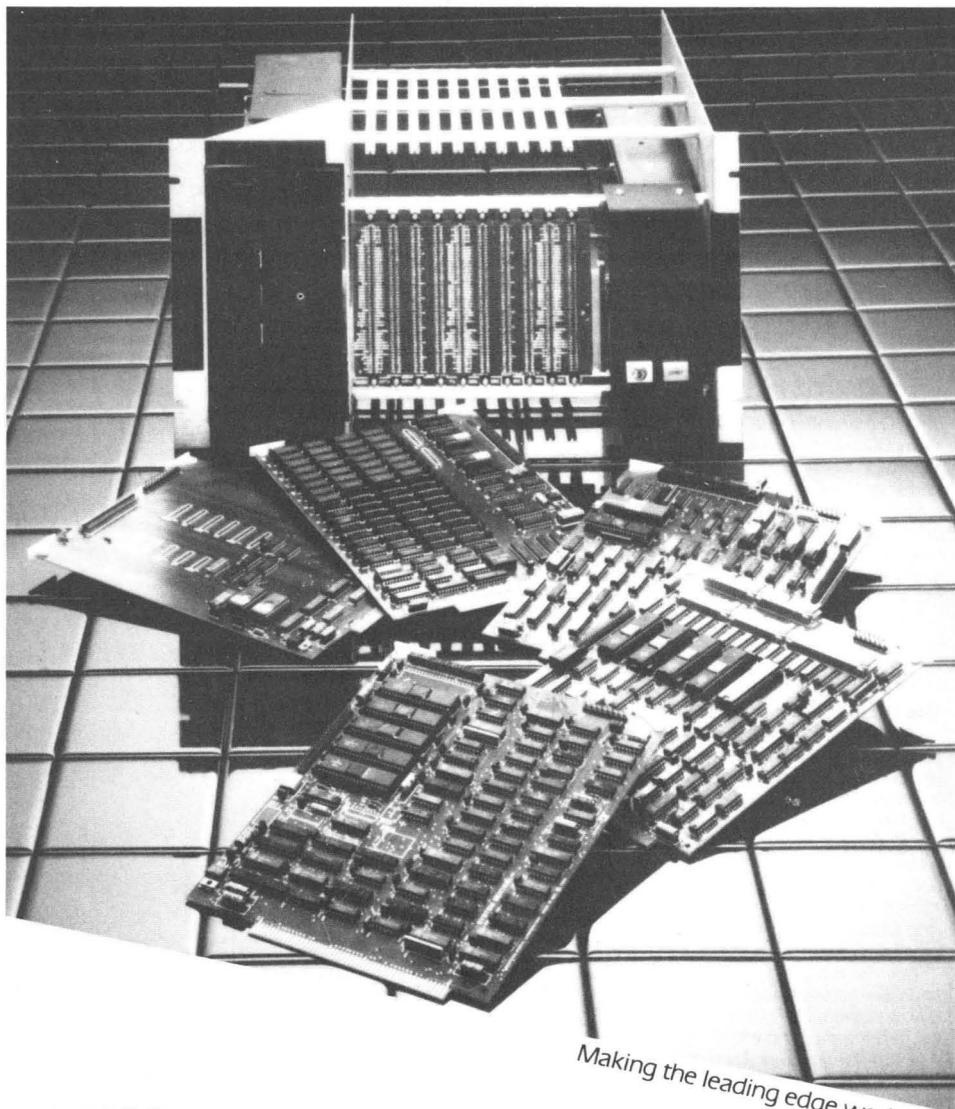
Multi-tasking is provided to the user with the PROCESS declaration and the START statement. The start statement invokes a process from within the program as an asynchronous task. SIGNAL and WAIT (like Dijkstra's V and P) on a semaphore allow synchronization of tasks and allow tasks to wait on a hardware interrupt such as an I/O complete.

Program Segmentation

Segment procedures provide automatic loading of program code from disk storage. Segment procedures and memory overlaying in the operating system allows programs to run that would use more than the amount of memory available.

Modularity

The unit capability allows large programs to be broken into smaller modules to be separately compiled and linked together. It also allows frequently used subroutines to be linked into programs so that the source of the subroutines does not need to be included in each program that uses it. All linking is done before the program is executed.



ME 1600
MODULAR MICROENGINE™

Making the leading edge work for you

WESTERN DIGITAL
CORPORATION

ME1600 Modular MicroEngine™

Software, not hardware, has become the key to system efficiency in the Eighties. To this end, Western Digital has innovated the Micro-Engine™. It's a unique concept, designed to blaze the P-code trail, making Pascal and Ada™ eminently accessible. In fact, it executes these high-order, block structured languages directly, as its own native instruction set.

Now, to optimize usability and flexibility, we've expanded this concept to the Modular Micro-Engine. It's modular in choice of languages—Pascal or MicroAda™, our microprocessor-based subset of DoD mandated Ada™. And it's modular in system function, for expansion freedom and service simplicity.

Specifically, each board in the system implements a distinct function: processing, storage, file management, I/O, and user access to the Sentinel/24™ bus.

Such modularity facilitates maintenance. And it puts the system configuration decisions squarely in the hands of the OEM designer.

The ideal P-code machine.

Our Modular MicroEngine is based on the universally-embraced UCSD Pascal compiler and System Software. The result is incredibly efficient program compilation. Unlike conventional processors, which must interpret Pascal instructions in their own language, the MicroEngine executes its internalized Pascal P-code directly; it is the processor's native language.

This "software in hardware" approach provides system designers with a powerful combination: the performance and efficiency of assembly language programming and the time-saving simplicity of the most advanced languages.

P-code was designed to run most efficiently on stack-oriented processors, such as our Micro-

Engine. So programmer efficiency is optimized. And there's no better vehicle for developing fluency with Pascal and Ada.

Speedier software development—with flexibility.

As high level languages with strong data typing, extensive error-checking, and automatic reentrancy and recursion, Pascal and Ada are designed to produce extremely reliable code.

And the resulting programs are easy to live with. They're less costly to update and modify than programs in other common languages.

And they're fully transportable since Pascal and Ada are such highly standardized languages.

Because algorithmic languages allow simpler statements of the program to be executed, they're less likely to fail in the field.

The Modular MicroEngine's UCSD Pascal Software System includes: Operating System • Pascal Compiler • Multi-tasking concurrency primitives and interrupts • Screen and line-oriented editors • Library and Linker systems • Software debugger • File management utilities.

ME1601 Pascal & MicroAda Processor

16-bit stack oriented processor
• Software-driven architecture • Four interrupt levels • Hardware multiply and divide, with floating point • Memory-mapped I/O • Real-time clock • DMA control logic • Power-fail detection with auto restart • System Sentinel™ protection for bus "time-out."

ME1610 128K Byte Memory Module

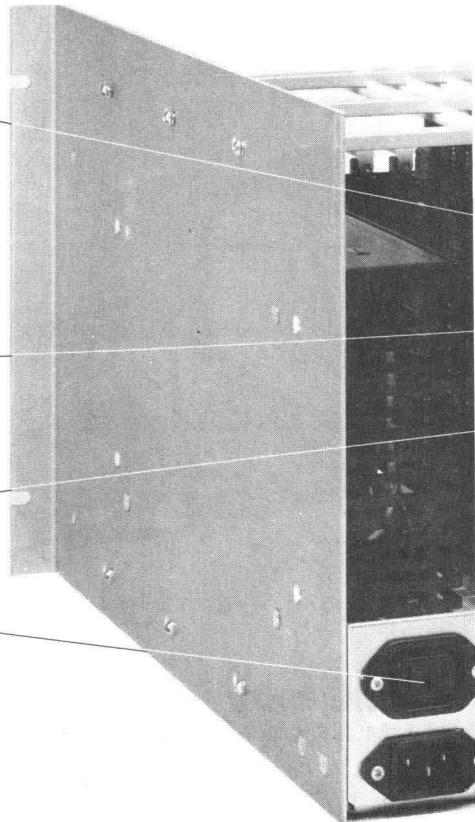
16K dynamic RAMs with 350ns cycle time • Read/write access: 610ns • 16-bit word length • Memory refresh interleaved with bus access for minimum memory latency.

ME1620 Floppy Disk Controller

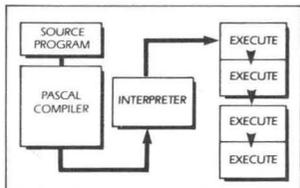
Controls up to four floppy disk drives • DMA operation • Supports 8" drives • Single or double density, single or double sided • Diskettes may be preformatted, or formatted under program control.

ME1650/1651 Chassis/Power Supply

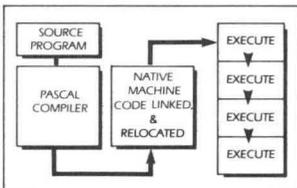
10-slot Sentinel/24 card cage
• 15 or 25 amp power supply
• Sentinel/24 bus motherboard



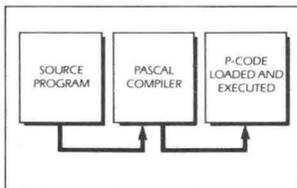
COMPARISON OF DIRECT P-CODE EXECUTION TO OTHER TECHNIQUES



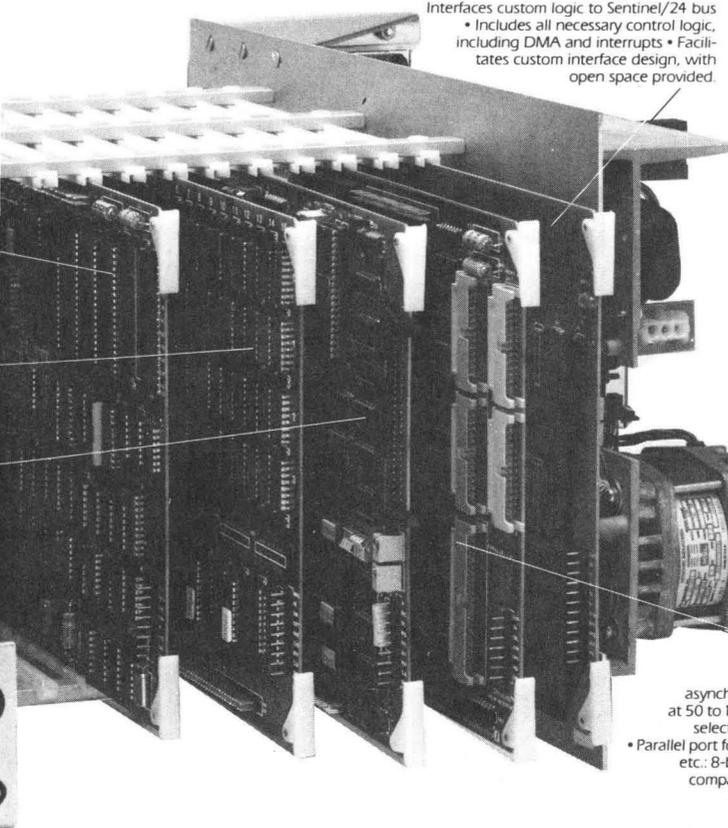
Most microprocessor Pascal compilers are interpretive: the compiler produces intermediate code which is decoded and executed by software interpreter. Each P-code instruction requires multiple processor instructions, taking more time and using more memory.



Other Pascal compilers convert Pascal source programs into the processor's machine language. This force-fits programs onto architectures not efficient for Pascal, resulting in execution of more instructions per function.



The Modular MicroEngine takes a direct approach. The Pascal compiler produces P-code which the MicroEngine is able to execute directly as its own native instruction set.



ME1639 General Purpose Interface Controller

Interfaces custom logic to Sentinel/24 bus
 • Includes all necessary control logic, including DMA and interrupts • Facilitates custom interface design, with open space provided.

System Configurations ME1660 Subsystem

Includes: ME1601 Pascal/MicroAda Processor • ME1610 128 KB Dynamic RAM Memory Module • ME1620 Floppy Disk Controller • ME1630 Serial/Parallel I/O Controller • ME1609 Boot/Terminator Module • ME1651 10-slot Chassis with 25 amp Power Supply

ME1665 System

Includes: ME1660 Subsystem, plus: One Double Density, Double Sided Floppy Disk Drive

ME1670 Packaged System

Includes: ME1660 Subsystem, plus: One additional Double Density, Double Sided Floppy Disk Drive (two total); Desk Top Enclosure

ME1675 Packaged System

Includes: ME 1670 Packaged System, plus: Centronics 737 Line Printer; 80 Character by 24 line CRT Terminal

ME1630 Serial/Parallel I/O Controller

Four RS-232-C full duplex I/O channels: supports asynchronous I/O; data transmission at 50 to 19,200 baud; interrupts may be selectively enabled for each channel
 • Parallel port for interfacing printers, plotters, etc.; 8-bit input/output configuration; compatible with Centronics printers.

SECTION 3

Pascal

Pascal is a universally used structured programming language. With appropriate library support, it is suited to a broad range of applications: systems programming, real-time control, data communication, business systems, education, and most other applications. Pascal combines the data structuring capabilities of COBOL, the block structuring of PL/I, and the expression handling of FORTRAN into a concise, efficient language.

The modular MicroEngine family is built around the UCSD Pascal compiler and System Software — the most widely used Pascal system for small computers. UCSD's compiler contains the Jensen-Wirth nucleus plus additional features which extend Pascal's capabilities. Some of these language extensions include:

- Long integers (up to 36 characters)
- Data file access
- Automatic loading of program segments from disk storage

- Separate compilation and linking of Pascal modules
- I/O and interrupt programming
- Pascal program synchronization via SIGNAL and WAIT on SEMAPHORE instructions.

MicroAda

Ada is a new language defined by the US Department of Defense, as a standard language for all new DoD systems. It is a modular, algorithmic language with strong data typing and is primarily intended for real time applications.

Functionally Ada provides all the capabilities of Pascal, with extensions in four major areas:

- Exception handling for error recovery
- Separately compiled packages
- Multi-task synchronization
- Primitives for encapsulating and implementing of special I/O interfaces.

Western Digital's MicroAda is a subset of the full Ada language, and is designed to operate on our MicroEngine with 128KB of memory. The initial release of MicroAda will support most features of Ada packages and separate compilation, tasks and exceptions, but generics, representation specifications and the more complex exception handling features will not be included.

Western Digital intends to support the full Ada language in upcoming products.

For more information, contact your sales representative at:

Western Digital Corporation
3128 Red Hill Avenue, Box 2180
Newport Beach, CA 92663
(714) 557-3550 • TWX 910-595-1139

MicroAda, MicroEngine, Sentinel/24 and System Sentinel are trademarks of Western Digital Corporation. Ada is a trademark of the U.S. Department of Defense.



WESTERN DIGITAL
C O R P O R A T I O N

April, 1981 ASD-001-4/81-10K

Introduction to

CONTROL SYSTEMS DIVISION

The Control Systems Division offers a complete spectrum of products and services, ranging from single-chip PMOS and NMOS microcomputers for dedicated control applications to complete boards and finished products. In addition, the Division is charged with developing and marketing products for use in energy conservation and environmental control, including thermostats, furnace, heat pump, and air conditioning controls, as well as lighting and irrigation controllers and new sensor technology which are designed to conserve and control all forms of energy in business and residential environments. Another major thrust of the Division is the application of microelectronic engineering services to supplement and improve upon existing mechanical and electromechanical controls. From components to finished products, Control Systems offers a complete spectrum of product support.



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CONTROL SYSTEMS DIVISION

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4 BIT MICROCOMPUTERS

Western Digital Control Systems Division offers both PMOS and NMOS single chip microcomputers for dedicated controller applications. Both of these families are true microcomputers in that they have on-chip mask ROM, RAM, I/O, and clock generation—all of the elements required to implement a programmable microcontroller solution for your dedicated control problem.

Worldwide, the 4-bit microcomputer market is estimated to be approximately 20 million units in 1980 with a growth rate of approximately 30% annually. Due to the fact that they normally have very few if any external support circuits, their cost effectiveness makes possible a wide diversity of applications such as:

CONSUMER APPLIANCES

- Microwave ovens
- Washers and dryers
- Garage-door openers
- House heating/cooling systems
- Gas/electric ranges
- Dishwashers
- Lawn sprinklers
- Water softeners

CONSUMER ELECTRONIC PRODUCTS

- Electronic games
- Telephone answering machines
- TV tuning synthesizer
- CB radio synthesizer
- Tape deck transports
- Time zone clocks
- Photographic timers/controllers
- Electronic toys
- Telephone dialer/memory
- Telephone call-diverters
- Hi-fi turntables
- Hi-fi system controller
- 7-day alarm clocks
- Automated slide projectors

OFFICE MACHINES

- Printing calculators
- Postage machines
- Small printing machines

- Specialty calculators
- Copy machines
- Dictation equipment

COMMERCIAL APPLIANCES

- Electronic cash registers
- Vending machines
- Gasoline pumps
- Elevator controllers
- Printing presses
- Cookers/fryers
- Electronic weighing/marketing scales
- Copy equipment
- Automated "ticketing" machines
- Weather monitors
- Ice cream machines

SECURITY SYSTEMS

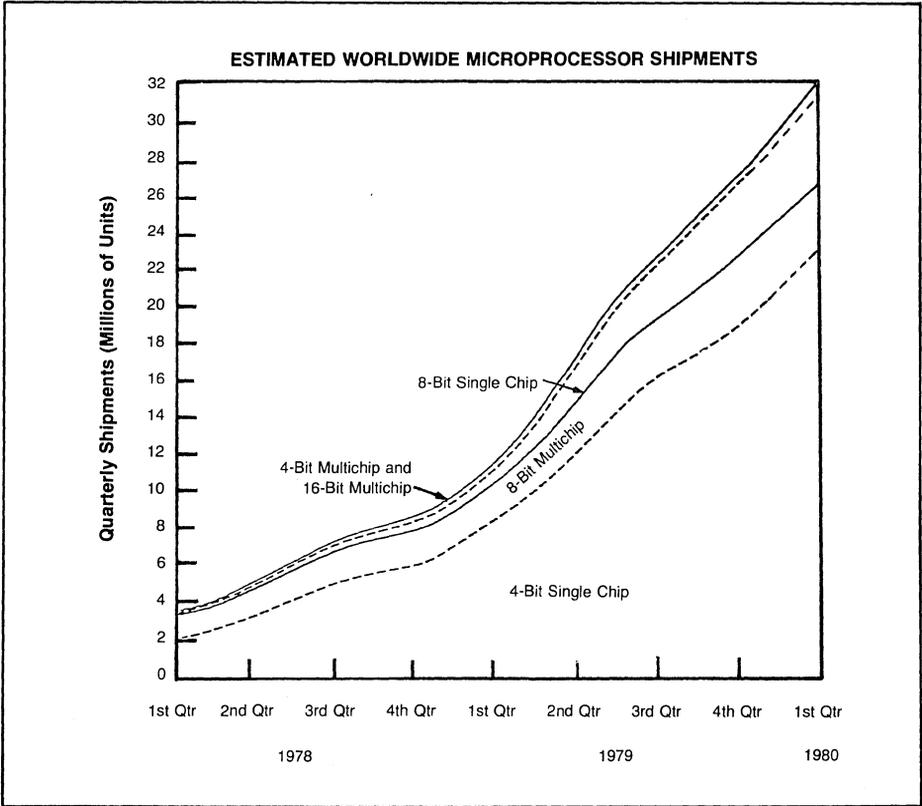
- Intrusion alarms
- Fire alarms
- Water/flood alarms
- Identification systems
- Personnel counters
- Electronic door locks
- Violent weather alarms

AUTOMOTIVE/MARINE

- Anti-skid braking system
- Dashboard control
- Systems status monitor
- Fuel consumption/MPG computer
- Anti-theft systems
- Marine navigational calculator

INDUSTRIAL APPLICATIONS

- Simple machine control
- Simple process control
- Special counters/timers
- Molding presses
- Cooking equipment



Source DATAQUEST, Inc.

SUBMISSION OF MASK ROM CODE

To submit mask ROM code for the WD4200/4210, two items need to be received:

- (1) Completed I/O options list (see page) describing the desired configured of the mask-programmable options.
- (2) The object code itself.

The object code may be in the form of a diskette containing the XXX.TRT and XXX.LM files generated by a COP400 PDS development system, or EPROMS (5204, 2708, 2716, etc.), paper tape, etc. (we prefer the diskette or EPROMS), and a hard copy printout of the object code. Western Digital will review and dupli-

cate the media submitted and will return copies to the customer.

Upon written confirmation as to the correctness of the data, masks are generated and an engineering pilot run is commenced. At the completion of the pilot run, approximately 10 devices are submitted to the customer for verification and approval. Upon written verification by the customer, the remainder of the pilot run (usually several hundred devices) are shipped as part of a pre-production delivery, and the production wafers are started for predetermined, scheduled delivery.

MASK OPTION CONFIGURATION TABLE FOR WD4200/4210

(Reference WD4200 Data Sheet, Pg. 13)

MASK OPTION	SELECTED OPTION	COMMENT	MASK OPTION	SELECTED OPTION	COMMENT
1		Ground Pin	21		G0 I/O Port
2		CKO Pin	22		G1 I/O Port
3		CKI Input	23		G2 I/O Port
4		RESET Pin	24		G3 I/O Port
5		L7 Driver	25		D3 Output
6		L6 Driver	16		D2 Output
7		L5 Driver	27		D1 Output
8		L4 Driver	28		D0 Output
9		IN ₁ Input NA 4210	29		Function
10		IN ₂ Input NA 4210	30		Bonding
11		Vcc Pin			
12		L3 Driver			
13		L2 Driver			
14		L1 Driver			
15		L0 Driver			
16		SI Input			
17		SO Driver			
18		SK Driver			
19		IN ₀ Input NA 4210			
20		IN ₃ Input NA 4210			

Customer: _____

WDC P/N: _____

Customer P/N: _____

SECTION 4

PREPROGRAMMED MICROCONTROLLERS

Control Systems Division offers several preprogrammed microcontrollers which were developed by the Division to solve timing and control problems which previously had been implemented by electromechanical systems consisting of motors, cam switches, levers, etc. or for which a large number of random-logic IC's were required. Several more devices are being developed; for customized versions of these standard products, please contact the factory.

WD-51 IRRIGATION CONTROLLER

The WD-51 performs all of the timing and control functions required by a 6-station irrigation (sprinkler) control system for residential and commercial applications.

The only support circuitry required is a simple power supply, display, keyboard/switch matrix, and triac or other high-current solenoid driver. The device is fully programmable for a 7-day week and each station output is programmable from 0 to 99 minutes duration. Up to 3 complete watering cycles per 24 hour period are available, as well as a pump/master valve output and a rain-inhibit switch input.

WD-55 TIMER/CONTROLLER

The WD-55 is a general purpose timing element for use as a dark room timer, process sequencer, appliance timer, time-delay relay, recycling timer, etc. It may be configured for two different modes of operation: one mode utilizes a conventional matrix keyboard for data entry, in conjunction with a 4-digit LED or V-F display for generating up to seven timed sequential outputs. Another mode allows data entry through BCD-encoded switches for triggered or continuous control of 2 outputs.

WD4200/4210

These devices are fabricated using N-channel technology, and are hardware and software compatible with National Semiconductor's COP 420/421 devices. The WD4200 is available in a 28-pin package and features 23 I/O lines. The WD4210 is a bonding option which deletes the 4-bit IN-port and is available in a 24-pin package. They both feature $1K \times 8$ ROM, 64×4 RAM, a $4.0\mu s$ instruction cycle time, 4.5 to 6.3V operation, a 3-level subroutine stack, single-level interrupt, serial I/O plus sync, on-chip counter/timer, and a high current 8-bit bidirectional port capable of directly driving LED displays.

WD4020

This is a ROMless version of the WD4200. It is available in a 40-pin package and has all of the I/O lines

of the WD4200 but in addition has a multiplexed address/data bus to interface with external EPROM or PROM memory. It is hardware and software compatible with the WD4200 and thus may be used for in-circuit emulation of the mask-ROM part for hardware/software debugging. Also, since it requires only an off-chip latch and PROM, it may be used to implement a low cost 3-chip microcomputer for low-volume, cost sensitive applications.

CR2272/2282

These devices are fabricated using P-channel technology and are available in a 40-pin package. The CR2272 has 512×10 words of ROM, while the CR2282 features 640×10 words of ROM. Both have 32×4 words of RAM, 16 latched outputs, 2 latched inputs, 8 scan outputs, and direct LED of V-F display drive capability.

PRODUCT/SYSTEM DESIGN CAPABILITY

Control System's technical staff has in-depth experience in applying microcomputer technology to consumer and industrial applications. This experience includes:

- (1) Electronic circuit design
- (2) Software (programming) design
- (3) System integration
- (4) Complete product design, development, and testing.

In addition, Western Digital's Controlled Energy Division, located in Riverside, California, has extensive capabilities for the assembly and test of PCB's ranging from prototype to high volume production.

A typical development cycle for a complete product is shown in Figure 1. The initial starting point of a product hinges on the availability of a functional specification. The functional specification describes in detail the function which the end product is supposed to perform. If this is not available, WDC has the capability of working with the customer in developing mutually acceptable specifications based on our experience and the customers' wishes or ideas for a product.

Upon completion of the functional specification, the preliminary hardware and software phase is entered. During this timeframe, the electronic circuit design is performed and a prototype, usually consisting of a handmade wire-wrapped breadboard, is produced. During this same time, the software design is being performed and is mated with the prototype hardware by means of an emulator board containing the software in EPROM. This prototype is then available for customer checkout. At this stage, changes can be made relatively easily since the prototype can be reprogrammed and rebuilt with minimal expenditures of

time and effort. However, with attention given to the initial specification development, these changes can be minimized to a great extent.

It is important to note that the circuit design can incorporate any part the design engineer and customer feel is best, even though that part may not be made by Western Digital.

When the customer is satisfied with the performance of the hardware and software, a hard tooling phase is entered in which the program information is converted to mask ROM single-chip microcomputers and the hardware design is converted to a printed circuit board

assembly. At the completion of this phase usually a field trial with these preproduction systems is performed. Hopefully, the changes required as a result of the field trial are minimal at this time, since significant changes can become very costly during this phase, due to the fact that software is now in mask ROM form.

If no changes are required, a pilot run is then performed to allow WDC or other producers to smoothly move into a volume production phase.

If you wish further information on these capabilities, please contact the Control Systems Division to discuss your product in detail.

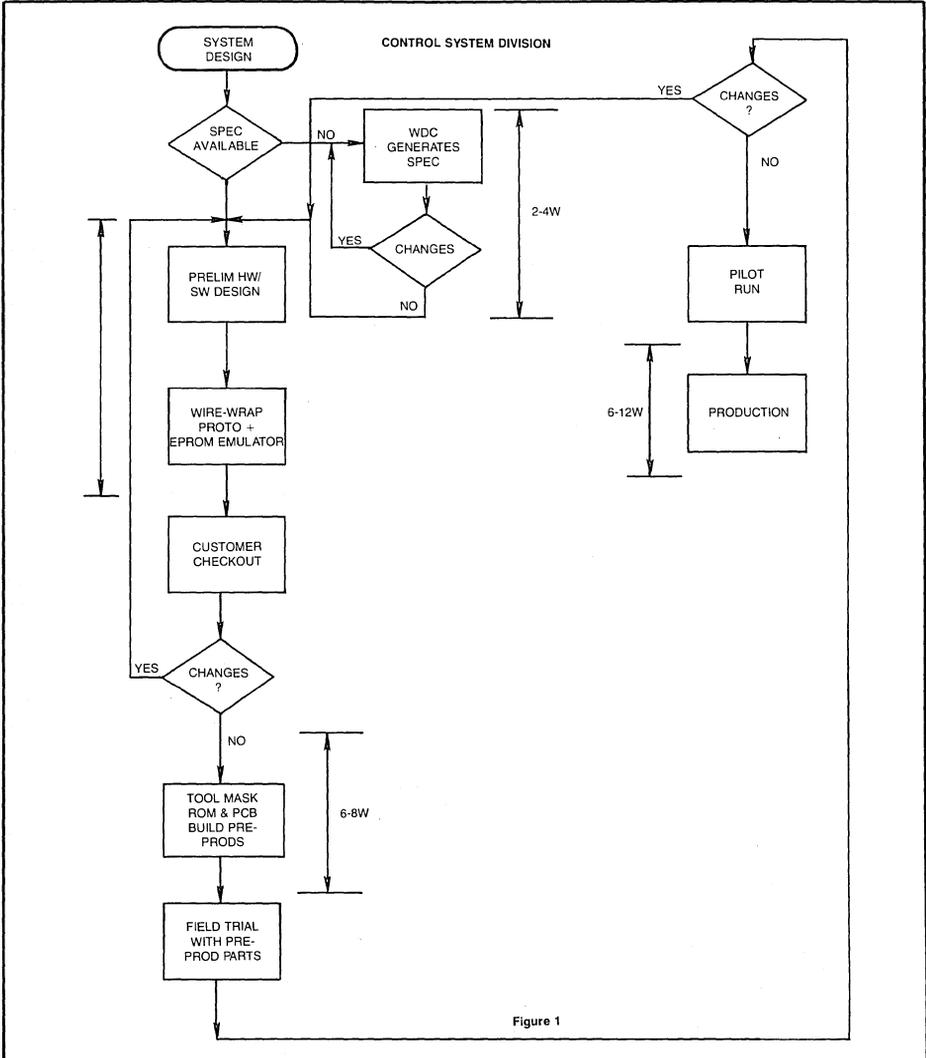


Figure 1

4-ZO-1010

DESIGN NEWS

Reprinted from
February 5, 1979

Designing With Electronics

One approach is to let the electronics supplier do some, of all, the work
Bill McDonough, Applications Manager, Western Digital Corp., Newport Beach, CA

How long have design engineers been talking about integrated circuits (ICs), medium-scale integration (MSI) and large-scale integration (LSI)? Five, maybe ten years? Compared to gears, detents, motors, bearings, pulleys, levers and the like, that's a relatively short time in which to provide case histories pertinent to every situation.

Although it's natural for engineers and designers to wonder how to apply these electronic technologies to their own products, there are many unanswered questions and nebulous answers floating around. Lower cost, part-count reduction, increased efficiency, improved performance and better reliability are hinted at in discussions of LSI application to mechanical systems. But why would a designer who's been doing his job right, and who has a good, reliable design, be motivated to change to electronics?

It is almost anecdotal, but too often the design engineer doesn't determine that he needs a specially designed circuit or LSI chip until his competition announces a new product using this technology. When the need to follow suit becomes apparent, he basically has one of two choices to make. Will he attempt to bring electronics expertise in-house or will he seek assistance from an outside source?

There are several things to consider if the designer opts for the first choice. First, simply hiring bright, young electrical engineers with microprocessor and LSI technology backgrounds will not solve the problem. Although these engineers probably will be the best-qualified in the company technically, most often they are grossly unqualified to make necessary decisions because they lack understanding of company and market needs.

Second, bringing the design work in-house requires a system design team—electronics assembly problems must be addressed, the design must be tested and the reliability must be proven. Companies literally enter a whole new business when they choose to develop their own electronics. The large companies of this world can afford to design, assemble, test, and prove, but many companies cannot afford to work this way. Sometimes company profit margins are so thin that they will remain mechanical even if the time is right for the application of electronics.

The design engineer does, however, have another alternative—he can have chips specially designed by an outside firm. And this is where he runs into many unanswered questions. Where does one go to get this type of help? Are specially designed "subsystem chips"

available? What is included with this custom service? Would it be a proprietary chip? And finally, what does it cost—not only the end-cost, but what will it cost to find out whether LSI application is feasible for the product?

WHERE TO GET THIS HELP

One of the primary reasons that companies are reluctant to seek outside assistance is that they simply do not know where to turn. The semiconductor supplier market is not clearly defined. Certainly there are the large semiconductor suppliers who will gladly ship custom chips in 100,000-piece volumes. But unless the design engineer is able to seek help from his tried-and-proven industrial control suppliers, the only answer for the low-volume buyer has been the circuit board assembler—a middleman firm specializing in custom work.

Typically, one of these "board stuffers" assembles functional PC boards using designs furnished by the engineer. Some of these firms may also be able to aid in the board design, but often another middleman in the form of a consultant may be required to help the designer decide what to stuff on the board.

There is, however, another option available to the second-level, low-volume buyer seeking outside help. Some semiconductor suppliers, like Western Digital, recognizing the "hole" in the market, are now willing to provide as little or as much assistance as required for quantities as low as 10,000 units. Yes, the cost per unit will be more than for the 100,000 order, but at least now more companies are able to consider electronics. Services such as these will open the door to a lot of business that might otherwise be forced to remain mechanical or use some standard semiconductor product that can't provide all the desired features.

WHAT KIND OF HELP TO EXPECT

There are four major stages the potential chip-user goes through to arrive at his end product. Depending on his level of electronics expertise, he can seek help at any or all of these stages from the semiconductor manufacturer.

Step 1: The design engineer must compile a list of product requirements and desired features. This can take the form of detailed specifications or just general function specifications. Basically, what does the product have to do?

A semiconductor supplier will sit down with the de-

Typical development schedule for a custom circuit

Task \ Month	MARCH	APRIL	MAY	JUNE	JULY	AUG	SEPT	OCT	NOV	DEC	JAN	FEB
LOGIC DESIGN (Upsized Schem.)												
RAM Address Controller	▼▼											
Control Logic	▼		▼									
Check			▼▼	▼								
CIRCUIT DESIGN (Sized Schem.)	▼			▼								
Layout Design			▼			▼						
CAD Conversion					▼		▼					
Masks							▼▼	▼	▼		▼	▼
Fab							▼	▼	▼	▼	▼	▼
Debug								▼▼		▼▼		

signer and help him draw up his specification, if necessary. There is normally no charge for this service if a predetermined volume is involved.

Carried to the next logical step, a parts list can be drawn up from the spec and a development cost estimated. The manufacturer can also estimate a competitive production price at this point.

By considering cost/volume trade-offs at the start, the designer benefits from these new services right up front. Based on a particular product volume, the designer will know whether his \$100 product will now sell for \$90 or \$110 with electronics. Designers can decide fairly early whether it's the right move to make.

As a part of the initial proposal, this is a service for which a fee is generally charged. But it may also identify unconsidered advantages: additional selling features, a better display, increase reliability, and fewer moving parts.

It's not unlikely that the main issue will be shown to be features, and not strictly cost. And that has to help any product proposal's chances of success during the marketing and financial review process. The important thing to remember is that it is not simply a substitution of electronics for mechanics. The electronics will allow the addition of more features now, and later will make it easier to make further modifications.

Step 2: The design engineer must select a semiconductor product to fulfill his specification. When he seeks assistance from a semiconductor firm he has basically three options open to him.

The programmable solution. With the semiconductor manufacturer's help, the design engineer can determine if his application will be satisfied with a standard manufacturer-supplied chip, or microcontroller. Functions such as timing control, temperature control, set point control, special purpose computation and appliance control can often be accomplished electronically with a standard chip. For example, Western Digital has standard chips programmed to replace logic in vending machines and the timers in sprinkling systems.

Depending on the design engineer's expertise, he may elect to program the standard chip himself, or he may have the manufacturer do it for him.

If the designer elects to do his own programming, he can expect free application help from the semiconductor manufacturer and enough literature to tell him how to do the job. For the chip supplier, this is the simplest way of doing business; in this case, the designer should be able to order for a nominal program charge.

If the supplier will be programming the chip, he will expect a typical order to be in the 10,000-to-100,000-unit range over the first year. Programming costs might be expected to run anywhere from \$7000 to \$20,000, depending on the complexity of the application. Typically, this process takes 12 weeks from spec to single-chip programmed device.

Programming costs, in the case of Western Digital, can be kept reasonably low because complete display timing and control functions are built into the chip hardware, as opposed to being written into the program. This design eliminates customization or program time usually involved with the display loop and initially saves 100 to 150 instruction words.

The custom circuit approach is the second option open to the design engineer. The programmable solution is not always feasible, especially if the intended application is complex. In this case, a manufacturer can build a custom circuit from scratch to perform the required functions. The typical product development time in this case is nine months and development costs will run approximately \$50,000. The design engineer should be considering between 50,000 and 250,000 units per year to justify this development cost.

The integrated hardware solution is the third option available to the design engineer. Here the semiconductor manufacturer does the system design and provides a PC board with components already mounted and tested and ready to plug into the end product. This route will cost out anywhere from \$25,000 to \$100,000.

Step 3: The designer must now decide how he is going

SOLUTION 4

to design and assemble his product to do the job required. Unless the design engineer has chosen the integrated hardware solution, he buys his chip, whether standard or custom, programs it himself or has the manufacturer program it and is then responsible for putting that chip on a board. At this point, he must also select and design a display, a keyboard and an interface, integrate them all together and add plugs.

Step 4: The designer has to decide whether he's going to produce the board himself or have someone else produce it in volume. If the designer has elected to go with a standard chip, he can seek bids for the board production from several manufacturers or he can produce the board himself.

If the designer has commissioned a specially designed subsystem chip, he can opt for the designing manufacturer to handle the board production, or again, he can handle it himself.

A TYPICAL CASE

Let's take a hypothetical situation from start to finish to illustrate how this process would take place.

XYZ Company manufactures electromechanical irrigation system controllers. Their competition suddenly comes out with an electronic device that does a more efficient job. XYZ's marketing people inform their president that, to stay ahead in the market, XYZ's product will now have to offer a better resolution of the time cycle: one-minute increments (instead of standard five to ten minutes) and multiple cycles (previously unavailable) to compensate for terrain differences. And, it must remain at a competitive cost.

XYZ's president promptly hands the problem to his design team. From a marketing timetable standpoint, we would hope the conclusion is quickly reached that outside help will be necessary. At that point, contact is made with the applications department of a semiconductor manufacturer. The applications people sit down with the XYZ's designers, evaluate the product's requirements and write an objective specification.

After a suitable microcontroller has been selected,

XYZ will then decide whether the software program will be written in-house or by the semiconductor manufacturer—a service generally priced between \$7000 and \$13,000. If XYZ chooses to have the supplier do the programming, the semiconductor maker typically will require a production commitment before taking on the assignment.

Let's say XYZ opts have the supplier do the programming. The company then supplies the semiconductor firm with an order for a predetermined minimum number of chips to be used over the first year. XYZ is now committed to pay a developmental fee for programming and tooling the chip; typically a 50% deposit will be made to the manufacturer at this point.

Four to eight weeks later, XYZ can expect a system prototype. In effect, the manufacturer supplies the equivalent of a three-chip solution, with the program resident in PROM to allow modification of the program during prototype evaluation.

Meanwhile, XYZ is designing a board to accept this part. The three-chip system is put on the board, it is plugged in and field testing begins. XYZ will pinpoint problems and change features, and the manufacturer will make the changes accordingly until XYZ feels they have a system that works and are ready to go with it.

The manufacturer will then pick up the rest of the developmental fee and build a single-chip part. This process can take three to six weeks. Under these conditions, XYZ owns the program and the part—it is their proprietary chip. The company has paid in the neighborhood of \$7000 to \$13,000 but has done its own board work.

If XYZ did not have the capability to do the board work, the supplier could do this also, and would supply the board assembly work and design to XYZ, well documented. In this case, XYZ would not necessarily end up with a proprietary product.

So, when the design challenge or problem-solution first indicates you should "go electronic," talk to a semiconductor manufacturer and see how they can help you. You may be pleasantly surprised at the very personalized treatment.



WESTERN DIGITAL

C O R P O R A T I O N

WD-51 IRRIGATION CONTROLLER

AUGUST, 1980

FEATURES

- CONTROLS UP TO 6 IRRIGATION STATIONS
- PUMP CONTROL/MASTER VALVE OUTPUT
- USER PROGRAMMABLE FOR UP TO 3 WATERING CYCLES DURING A 24 HOUR DAY
- USER PROGRAMMABLE RUN TIMES OF 1 TO 99 MINUTES FOR EACH STATION
- USER SELECTION OF WATERING DAYS OF 0 TO 7 DAYS PER WEEK
- TIME OF DAY AND DAY OF WEEK CONTINUOUSLY DISPLAYED
- RAIN INHIBIT MODE
- EASY TO DESIGN IN

GENERAL DESCRIPTION

Preprogrammed Controller for Irrigation Applications.

The WD-51 is a single-chip controller preprogrammed to operate a 6 station irrigation system. It is implemented using P-channel silicon gate MOS/LSI technology and requires minimal support circuitry. All program and data storage are on-chip, as well as input switch matrix scan, 7 segment display decode and drive, and output control logic.

FUNCTIONAL DESCRIPTION

The logic symbol and block diagram of the WD-51 is shown in Figure 1.

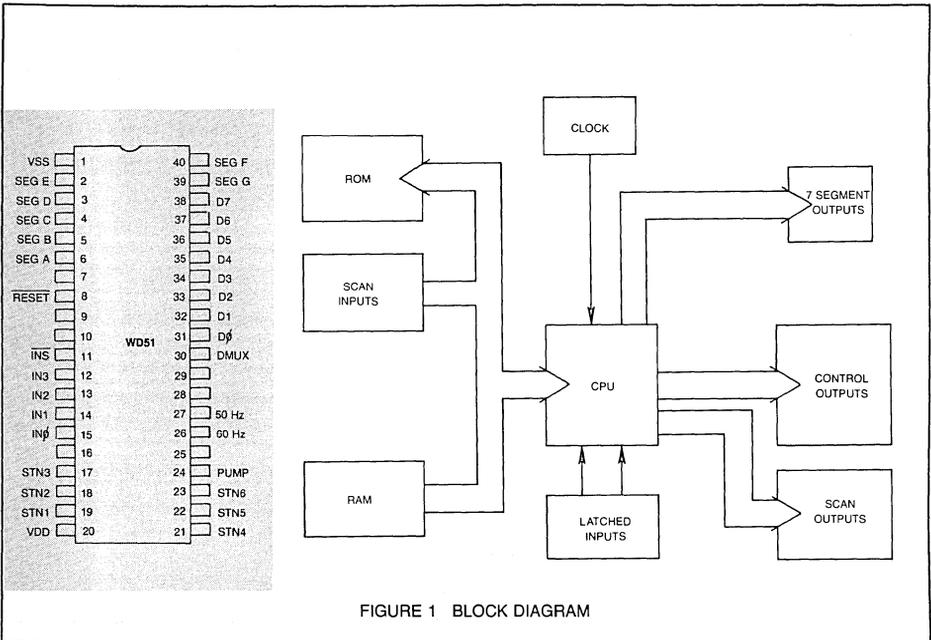
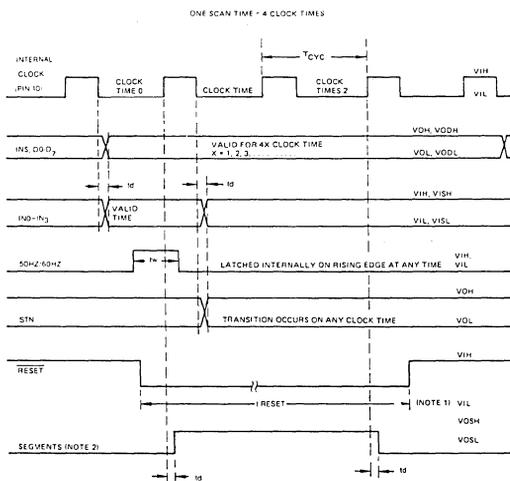


FIGURE 1 BLOCK DIAGRAM

WD-51-02 4

PIN DESCRIPTION

SYMBOL	PIN NO.	FUNCTION
V _{SS}	1	Positive Supply voltage
V _{DD}	20	Negative Supply voltage
Seg A,B,C, D,E,F,G	2-6, 39-40	Decoded 7-Segment Multiplexed outputs, 15 mA source.
<u>RESET</u>	8	A low-level input voltage resets internal logic and initializes RAM data.
INO, 1N1, 1N2, 1N3	12-15	Scanned inputs, 1N3 is MSB
STN 1,2,3, 4,5,6	17-19, 21-23	Station Output control for solenoid drivers.
PUMP	24	Pump control output- a high-level output indicates a manual or automatic cycle is in progress.
60HZ	26	60 HZ time base input
50HZ	27	50 HZ time base input
DMUX	30	4-digit display control output
D0-D7	31-38	Digit scan outputs, (D7=MS _D , D0=LS _D)



NOTE 1: RISING EDGE OF RESET GENERATES SCAN TIME 0 WITHIN 4 CLOCK TIMES
 NOTE 2: SEGMENT OUTPUTS ARE VALID DURING CLOCK TIMES 1 TO 3 ONLY
 THEY ARE LOW AT TIME 0

FIGURE 2
TIMING DIAGRAM

INPUTS

INPUT SWITCH MATRIX—The WD-51 may be used with any switch configuration which is matrix compatible, such as a keyboard, rotary switch, slide switch, or combinations of both. All multiplexing and decoding is performed on-chip, thus requiring no external components, other than the switch matrix.

SETTING DAY OF WEEK—If SET DAY is depressed in conjunction with ADVANCE, the Day digit (D4) will increment, with rollover from 7 to 1. Note that since the day is numerically displayed (as opposed to alphanumeric), the numbering is arbitrary, i.e., if Sunday is considered to be "1", then Wednesday is "4", Friday is "6", etc.

		DIGIT SCAN TIME OUTPUTS							
		D7 (38)	D6 (37)	D5 (36)	D4 (35)	D3 (34)	D2 (33)	D1 (32)	D0 (31)
SCANNED INPUTS	IN0 (15)	ADVANCE	3-STATION STRAP	SET MINUTES	ACTIVE DAY 4	ACTIVE DAY 1	START TIME #1	RUN TIME #4	RUN TIME #1
	IN1 (14)			SET HOURS	ACTIVE DAY 5	ACTIVE DAY 3	START TIME #1	RUN TIME #5	RUN TIME #2
	IN2 (13)			SET DAY	ACTIVE DAY 6	ACTIVE DAY 3	START TIME #3	RUN TIME #6	RUN TIME #3
	IN3 (12)			SKIP -A-DAY	ACTIVE DAY 7		MANUAL OFF	MANUAL ON	RUN

FIGURE 3 INPUT SWITCH MATRIX

The basic functions of the Irrigation Controller are selected by one or more switches as defined in Figure 2. Inputs IN0-IN3 form a 4 bit wide input port which is scanned by the Digit Scan Outputs D0-D7, forming an 8 × 4 matrix which connects to the user-supplied keyboard/switches.

SWITCH FUNCTIONS—The switch functions shown in Figure 3 are defined as follows:

ADVANCE—For all setting operations, a common key is used to increment the selected data (time, day, start-time, or run-time). Immediately after the detection of the advance switch, the data increments by 1, waits 1½ seconds, then begins incrementing at the rate of 3 per second. This allows the operator to move rapidly to the desired value without "overshooting" and then "tapping" the advance key when close to the find value.

SETTING TIME OF DAY—Two separate switch inputs for setting hours and minutes in conjunction with the ADVANCE key. If SET MINUTES is selected while ADVANCE is depressed, the minutes digits (D0 & D1) will increment. Minutes rollover is from 59 to 00 with no carry into the hours. If SET HOURS is selected while ADVANCE is depressed, the hours digits (D2 & D3) will advance. Hours rollover is from 24 to 01, with midnight equal to 2400.

SETTING START TIMES—There are up to 3 automatic watering cycle times available in a 24 hour period. To examine them, START TIME 1, 2, or 3 is selected and displayed in hours on digits D7 and D6. If it is desired to change the data, the ADVANCE key is depressed. The rollover is from 24 to 00, with 00 being a start-time "skip" value. Thus 1, 2, or 3 cycles per day may be selected.

SETTING RUN-TIMES—Each one of 6 stations may be set to a run time of 0 to 99 minutes, with 00 being a "skip station" value. To examine the stored data, the desired station RUN TIME key (1-6) is selected with the time in minutes being displayed on digits D7 and D6. To change the data, the ADVANCE key is depressed. The selected run time will then increment with rollover from 99 to 00 minutes.

SETTING ACTIVE DAYS—The WD51 reads active day information from the switch matrix, with typically slide, toggle, or "DIP" switches being used. An automatic watering cycle may be set for 0 to 7 days a week simply by closing the switch for the respective day. An ALTERNATE DAY switch position is provided, which, when activated, causes the controller to ignore the 7 active-day switches and to run an automatic cycle every other day.

MANUAL ON—This switch position immediately activates a timed watering cycle beginning with station No. 1, regardless of the setting of the start-times or active days. The run times programmed for stations 1-6 are automatically run.

WITH
 4 20-1-10110

The cycle may be terminated anytime with the **MANUAL OFF** key. If it is desired to start with a specific station other than station No. 1, that station **ONE-TIME**-key should be depressed *first*, then the manual key. The cycle will then begin at the selected station and continue through station No. 6.

RUN MODE—This is the normal automatic operating mode of the Irrigation Timer. When in this mode, the **START** and **RUN-TIME** data cannot be displayed or modified, preventing accidental erroneous entry of data.

RAIN INHIBIT (MANUAL OFF)—This switch is used to cancel or prevent a watering cycle, either manual or automatic. When activated during a current cycle, it immediately turns off all station outputs and returns to a time-keeping mode only. With external signal conditioning circuitry, this input could be used to interface with a moisture or rain sensor. This function is normally implemented by paralleling a toggle switch ("rain") with a momentary key ("manual off").

3 STATION OPTION—By connecting IN3 to D5 through a diode, run times for Stations 4, 5 and 6 will be continuously set to zero, thus they will always be skipped. Also, if switch positions for Run Times 4, 5 and 6 are not provided to the user, these stations cannot be examined.

RESET—This is the reset input of the micro-controller. An external capacitor of approximately 2 μ f is recommended between 8 and VDD to generate a reset signal when power is first applied.

OUTPUTS

DISPLAY SEGMENT OUTPUTS (SEG A-SEG F)—The WD-51 is designed to directly drive vacuum fluorescent (V-F) displays or common-cathode LED displays up to 0.3

The selected station (1–6) is shown in digit D5. The station number is displayed when a **RUN-TIME** key is depressed or the controller is active during a manual or automatic watering cycle; otherwise a zero is displayed.

The start time and run times are displayed in digits D6 and D7. When any of the start-time switches are selected, the D6 and D7 digits display the hour of the day the watering cycle is to start. If a run-time switch is activated, the selected station run-time is displayed in a minutes format. During a manual or automatic watering cycle, the time remaining for the currently active station is displayed in minutes. Otherwise, 00 is displayed.

STN1-STN6—The station outputs are latched logic outputs designed to control the solenoid drives in an irrigation system. These outputs are normally a low-level voltage (solenoid drive is off). When a manual or automatic watering cycle occurs, the appropriate station output goes to a logic "high" voltage for the selected run-time interval. Station-to-station switching is essentially instantaneous. It is recommended that these outputs be buffered by a current driver to supply sufficient current for triacs, relays, or other high-power switching devices.

PUMP CONTROL OUTPUT—This output is a latched logic output which is normally a logic "low" voltage for the pump off condition. It goes to a logic "high" voltage at the beginning of a watering cycle, either manual or automatic, and remains high until the last station goes off. With suitable buffering, this output may be used to turn a pump motor on and off when needed or simply to drive a "cycle on" LED status indicator, or to act as a "master valve" output.

DMUX OUTPUT—This output, in conjunction with minimal external logic, provides a means of using a 4 digit display with the WD51. It is a logic high when a **RUN-TIME**, **START-**

DIGIT SCAN TIME

D7	D6	D5	D4	D3 D2 D1 D0			
START/RUN TIME (MSD)	START/RUN TIME (LSD)	STATION NUMBER	DAY OF WEEK	T	I	M	E
				10's HOURS	HOURS	10's MINUTES	MINUTES

FIGURE 4 DISPLAY REGISTER

inches. The seven segment outputs are high current outputs and are multiplexed in synchronization with D0 - D7 with sufficient interdigit blanking to prevent "ghosting". The display register is shown in Figure 4.

The time of day is displayed as a four digit number in 24 hour format (9AM = 0900, 5PM = 1700, MIDNIGHT = 2400, etc.) and the day of the week is displayed as a number between 1 and 7. The time and day are continuously displayed regardless of the mode selection. Zero blanking is not provided for any of the digits.

TIME, or **SET-DAY** key is depressed and a logic low voltage at all other times, hence it may be used to externally select digit times D4–D7 when high and D0–D4 when low.

DEFAULT INITIALIZATION—Upon the occurrence of a **RESET** the micro-controller defaults to the following: Time of day to 12:00; day to 1; start time 1 to 0200 hours; start times 2 and 3 to 00; and run time 1–6 to 10 minutes each. Thus if power is lost to the microcomputer, a default program will be executed without user intervention.



SPECIFICATIONS

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

ABSOLUTE MAXIMUM RATINGS

Operating Free-Air Temperature	
T _A Range	0°C to 70°C
Lead Temperature (Soldering, 10 sec.)	300°C
Storage Temperature	-65°C to +150°C (Ceramic) -55°C to +125°C (Plastic)

Power Dissipation 2.5 Watt at 25°C
 Positive Voltage on any Pin with Respect to V_{SS}: +0.3V
 Negative Voltage on any Pin with Respect to V_{SS}: -20.0V

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{SS}-V_{DD} = 13.2V unless noted otherwise

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage (V _{SS} -V _{DD})	All inputs and outputs open	11.5	13.2	14.5	V
Operating Current		6		15	mA
Input Voltage Levels					
All Inputs Except IN0-IN3	Note 1	V _{SS} -1.0		V _{SS}	V
Logic High (V _{IH})		V _{DD}		V _{SS} -4.2	V
Logic Low (V _{IL})	Note 2	V _{SS} -3.75		V _{SS}	V
Inputs IN0-IN3		V _{DD}		V _{SS} -9.0	V
Logic High (V _{ISH})					V
Logic Low (V _{ISL})					V
Output Voltage Levels					
All Outputs Except D0-D7 and SEG A-SEG G					
Logic High (V _{OH})	I _{OH} = +100 μA Min.	V _{SS} -1.0		V _{SS}	V
Logic Low (V _{OL})	I _{OL} = -1.6 mA Min.	V _{DD}		V _{SS} -4.6	V
D0-D7 Outputs					
Logic High (V _{ODH})	I _{ODH} = 1.5 mA+1 Input (IN0-IN3)	V _{SS} -1.5		V _{SS}	V
	I _{ODH} = 5.0 mA+1 Input	V _{SS} -3.0		V _{SS}	V
V _{ODL}	Note 3	V _{SS} -3.5		V _{SS}	V
Seg Outputs Seg A-G	I _{OSH} = 16 mA			V _{SS} -6.0	V
Segment Output Current	Note 3	10	15	40	mA
Seg A-G I _{OSH}					
AC Electrical					
TCYC			10		μsec
Instruction Cycle Time					μsec
t _d /t _w		5.0			μsec
t _{RESET}		15			msec
TBase		0	60	500	HZ

Note 1: Internal Pullup Resistors of Approximately 6K to V_{SS} Across Each Input.

Note 2: Internal Pulldown Resistors of Approximately 12K to V_{DD} Across Each Input.

Note 3: Single Transistor to V_{SS} Output Only.



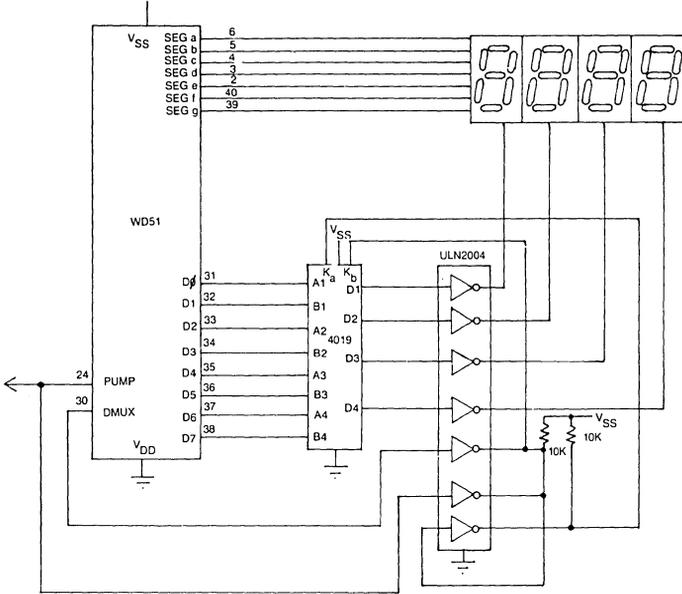


FIGURE 6 WD51 WITH 4-DIGIT DISPLAY OPTION

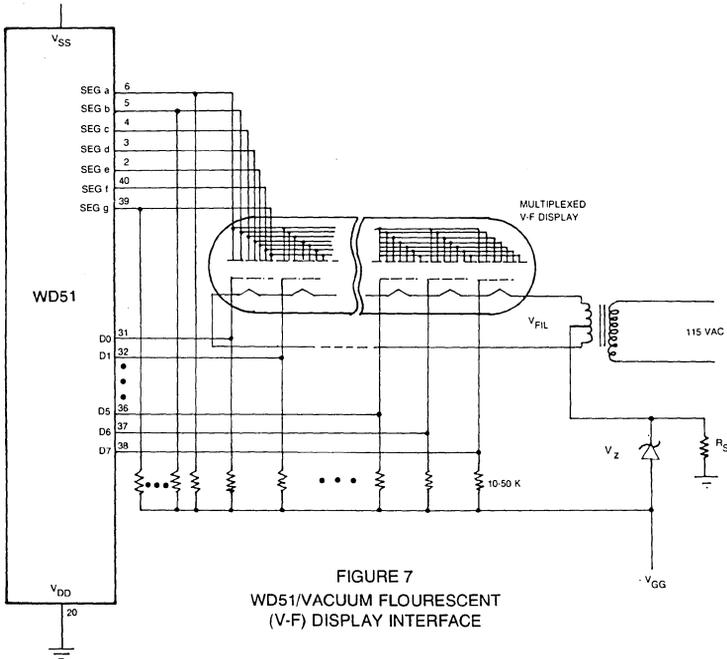
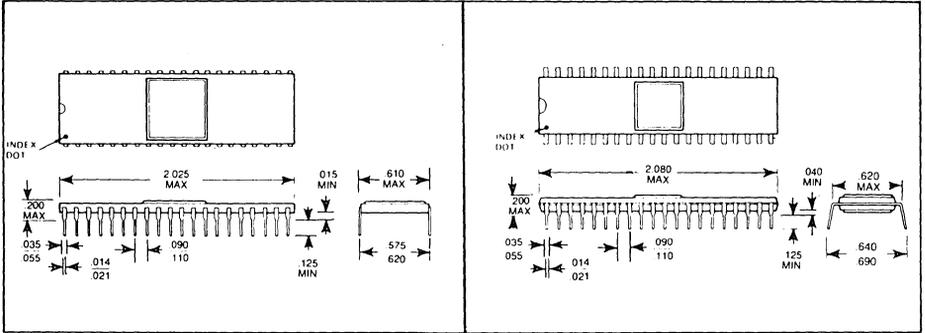


FIGURE 7
WD51/VACUUM FLOURESCENT
(V-F) DISPLAY INTERFACE

4 ZO-CMUP

MECHANICAL

40 Pin DIP Package available in plastic or ceramic packages.



WD51A CERAMIC PACKAGE

WD51B PLASTIC PACKAGE

SUPPORT:

Application and Design support is available from Western Digital.

ORDERING INFORMATION:

Specify upon ordering

WD51A for 40 pin ceramic package

WD51B for 40 pin plastic package

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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WESTERN DIGITAL C O R P O R A T I O N

WD 55 Industrial Timer/Controller

FEATURES:

- o LOW COST PREPROGRAMMED MICROCONTROLLER
- o USEABLE WITH KEYBOARD OR DISCRETE SWITCHES
- o HIGH CURRENT LED OUTPUTS OR DIRECT DRIVE OF VACUUM FLUORESCENT (V-F) DISPLAYS
- o UP TO 7 SEQUENTIAL OUTPUTS
- o SYNCHRONIZED WITH 50/60 HZ TIME BASE OR EXTERNAL OSCILLATOR
- o SINGLE TIME OPTION
- o CONTINUOUS OR SEMI-AUTOMATIC OPTION
- o DEDICATED TIMER OPTION-WORKS WITHOUT KEYBOARD OR DISPLAY
- o RESOLUTIONS OF FROM 0.1 SEC. TO 999 HOURS WITH DIGITAL ACCURACY
- o ALARM OUTPUT FOR AUDIBLE BUZZER
- o RELAY AND TRIAC OUTPUTS
- o AUDIBLE FEEDBACK FOR USE WITH MEMBRANE SWITCHES
- o 100 MW TYPICAL POWER CONSUMPTION

GENERAL DESCRIPTION

The WD-55 is a versatile, self-contained digital timer/controller/sequencer designed to replace many of the timing and control functions currently being performed by gears, cams, levers, and motors. It is another in a series of "silicon software" preprogrammed microcontrollers based on the WD40 family of 4-bit microprocessors. The WD-55 may be used in conjunction with a matrix keyboard and numeric display to implement a programmable timer/sequencer or with suitable "strap" options, may be used as a dedicated, stand-alone on/off controller. It is implemented in P-channel Silicon Gate MOS and is available in 40 pin plastic and ceramic DIP packages.

APPLICATIONS:

- o DARKROOM TIMER
- o PROCESS CONTROLLER
- o PROCESS SEQUENCER
- o TIME DELAY RELAY
- o APPLIANCE TIMERS
- o DEFROST CONTROLLERS
- o "DRIP" AND "MIST" IRRIGATION CONTROLLERS
- o ON/OFF TIMER
- o DIGITALLY CONTROLLED TIME DELAY
- o TRAFFIC LIGHT SEQUENCER
- o SECURITY SYSTEMS
- o LIGHTING CONTROL
- o INTERVAL TIMER
- o RECYCLING TIMER

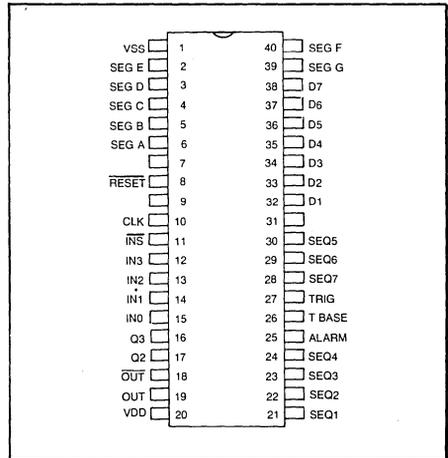


FIGURE 1.
WD-55 PIN CONNECTION

OPTION 4

WD-55 PIN DESCRIPTION

PIN NO.	SYMBOL	FUNCTION
1	VSS	+V
2	SEG E	One of 7 high current (20 MA source) outputs for direct LED drive
3	SEG D	One of 7 high current (20 MA source) outputs for direct LED drive
4	SEG C	One of 7 high current (20 MA source) outputs for direct LED drive
5	SEG B	One of 7 high current (20 MA source) outputs for direct LED drive
6	SEG A	One of 7 high current (20 MA source) outputs for direct LED drive
8	$\overline{\text{RESET}}$	Power turn-on reset input, active low
10	CLK	Internal RC clock oscillator output, approx. 100 KHZ
11	INS	Input select, not used in this application
12	IN3	Scanned input, MSB
13	IN2	Scanned input
14	IN1	Scanned input
15	IN0	Scanned input, LSB
16	Q3	Latched output, not used in this application
17	Q2	Latched output, not used in this application
18	$\overline{\text{OUT}}$	Timer output, active low
19	OUT	Timer output, active high
20	VDD	-V
21	SEQ1	One of 7 sequencer outputs, active high during preset timing interval 1
22	SEQ2	One of 7 sequencer outputs, active high during preset timing interval 2
23	SEQ3	One of 7 sequencer outputs, active high during preset timing interval 3
24	SEQ4	One of 7 sequencer outputs, active high during preset timing interval 4
25	ALARM	Audible alarm control output, active high
26	TBASE	Time base input, used as reference for all timing modes
27	TRIG	Trigger input, used in on/off mode, rising edge sensitive
28	SEQ7	One of 7 sequencer outputs, active high during preset timing interval 7
29	SEQ6/TIM2	One of 7 sequencer outputs, active high during preset timing interval 6

4 ZO-10m0

WD-55 PIN DESCRIPTION (Continued)

PIN NO.	SYMBOL	FUNCTION
30	SEQ5/TIM1	One of 7 sequencer outputs, active high during preset timing interval 5
31	D0	Digit output, LSD
32	D1	Digit output
33	D2	Digit output
34	D3	Digit output
35	D4	Digit output
36	D5	Digit output
37	D6	Digit output
38	D7	Digit output, MSD
39	SEG F	One of 7 high current (20 MA source) outputs for direct LED drive
40	SEG G	One of 7 high current (20 MA source) outputs for direct LED drive

FUNCTIONAL DESCRIPTION

The WD-55 is a versatile digital timing element designed to replace mechanical timing devices of the synchronous motor, cams, and lever variety. It is a preprogrammed mask-ROM single chip 4-bit microcontroller with different features determined by external strap options. It has essentially two distinct modes of operation: a keyboard programmable timer/sequencer using on-chip RAM for data storage and a 4-digit 7-segment display for data recall, or as an on/off timer which uses thumbwheel switches or even diodes for data storage and recall and does not require a display. These two different modes are selected by the absence or presence of a diode between the D7 digit output (38) and the IN0 scanned input (15). If the diode is absent, upon the occurrence of a reset pulse at pin (8), the device enters the keyboard programmable timer/sequencer mode. If the diode is present, a reset forces the device into the on/off timer mode.

In the timer/sequencer mode, the WD-55 operates with a matrix keyboard and a 4 digit numeric display to form a simple but flexible digital timing device for use in applications such as a dark room timer or programmable sequencer. The configuration table shown in Figure 1 provides the definition of keys, display digits, and strap options.

Keyboard: The WD-55 is useable with a standard 4x4 matrix keyboard (or 3x4 with two off-board switches) of the electromechanical or "membrane" type; audible feedback through the alarm output is provided for use with membrane or other switches which have little or no tactile feel. The bounce time is approximately 100 ms using a 60HZ timebase.

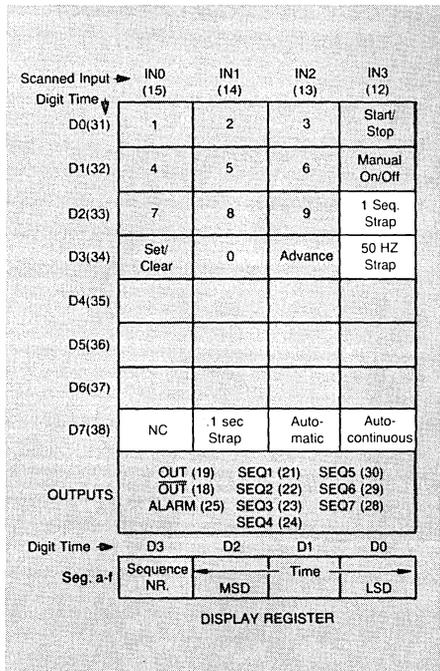


FIGURE 1. CONFIGURATION TABLE PROGRAMMABLE TIMER/SEQUENCER

KEY DEFINITIONS

ADVANCE: The key is used to access the 7 storage locations in RAM. Each time this key is depressed, the sequence number (digit 3) is incremented by one and the current value of the respective sequence is fetched and displayed in digits D0-D2 (least to most significant). If the current sequence number is 7, depressing the advance key will rollover to sequence #1. If the "1 sequence" strap is present (see strap options), this key is not required.

SET/ CLEAR: This key enables the entry of data into the RAM location currently being displayed by digit 3. When depressed, it enables the "SET" mode and clears display digits D0-D2 to zero as well as the respective memory location. Successive entry of data with the numeric keys (0 through 9) is then allowed. The set mode is terminated by depressing any non-numeric key. Note that there is no need for an "enter" or "store" key since the data displayed on digits D0-D2 is always automatically stored. If "SET/CLEAR" has not been depressed prior to a numeric key, the numeric key is ignored, preventing the accidental or unwanted entry of data.

MANUAL ON/OFF: This key acts as a push on/ push off switch to manually force the output pins (OUT (19) and $\overline{\text{OUT}}$ (18)) to toggle. This is used to manually force an output on, such as in a darkroom timer application where the enlarger needs to be turned on and adjusted before proceeding with a timed interval. These outputs will remain in their current state indefinitely until either the manual key is depressed again or a timed interval is initiated. It has no effect on any of the sequencer outputs, SEQ1-7.

START/STOP: This key is used to initiate or terminate a timed sequence. If a timing cycle is not being performed, depressing this key will initiate a cycle beginning with the sequence currently being displayed in digit 3. If a cycle is currently running, it will terminate it, returning the two complementary outputs (OUT and $\overline{\text{OUT}}$) to their normal state and incrementing the sequence digit by 1. In fact, when a timing sequence is currently active, this is the only key which is scanned. This key may be paralleled with an external start/stop or footswitch if dictated by the application.

NUMERIC KEYS (0-9): These keys are used to enter numeric data when in the "SET" mode. Data entry is accomplished by right to left entry; that is, digits 0 to 2 are left-shifted by 1 digit (with the old value of digit 2 discarded) and the most recently depressed numeric key data entered into digit zero. There is no limit to the number of numeric keys which are entered, but only the most recent 3 are displayed and stored. If the "SET/CLEAR" key has not been previously depressed, these keys are ignored.

STRAP CONFIGURATION

Considerable versatility is accomplished with the WD-55 by the use of strap options in the form of diodes to select or delete specific functions. In the timer/sequencer mode, the following options are available.

50 HZ STRAP: The WD55 uses an external time base to accomplish its timing functions. It is optimized for use with 50 or 60 HZ AC line applications. For operation with 60HZ, no strap is necessary. For 50HZ applications, a diode should be connected between D3(34) and IN3(12).

1 SEQ STRAP: This strap (a diode between D2(33) and IN3(12)) forces the device to operate as though it had only 1 time available. At the end of the timed sequence, the SEQ digit does not advance and the SEQ1 data is restored to digits 0-2. When this strap is employed, the advance key should not be used and the sequence digit (Digit 3) is always a "1" and hence could be eliminated.

.1 SEC STRAP: Without this strap, the basic resolution of the 7 sequences is 1 sec. That is, intervals of from 1 to 999 seconds are possible. With a diode (or diode plus SPST switch for variable applications) between D7(38) and IN1(14), the minimum resolution is decreased to .1 seconds; that is, the intervals are now from .1 to 99.9 seconds.

"AUTOMATIC" STRAP: With a diode between D7(38) and IN2(13), the automatic mode is enabled. In this mode, once the START key is depressed, sequences 1 through 7 are executed without further intervention. The cycle stops at the conclusion of sequence 7; that is, SEQ 1 data is being displayed and the keyboard is again being scanned. This is useful when the WD-55 is being used as a sequencer to cycle a complete 7-event sequence.

"AUTOCONTINUOUS" STRAP: This is used in conjunction with the "automatic" strap mentioned previously. If a diode is connected between D7(38) and IN3(12), the device will operate continuously once triggered by the start/stop key. This strap must be connected through a switch, since there is no means of terminating the sequence once initiated. Sequence 7 will be followed immediately by sequence 1. Depressing the start/stop key during the cycle will only terminate the current sequence in progress and begin execution of the next. This mode would typically be used in process control, machine sequencer, "moving lights" displays, etc.

INITIALIZATION

A low going pulse of sufficient duration (see Electrical Data) on the RESET pin (8) will force an initialization state, usually as the result of a power-turn-on reset. All 7 sequence times are set to zero and the sequence number digit (Digit 3) is set to "1". The complementary outputs OUT and $\overline{\text{OUT}}$ are set to logic LOW and logic HIGH respectively, and all sequencer outputs are logic LOW.

STOPWATCH/ELAPSED TIME CONTROLLER: If a nonzero time is entered into any sequence location, the WD-55 will count that time down to zero before advancing to the next sequence. However, if the stored data is already zero, depressing the START/STOP key will initiate an "UP" count mode starting from zero. The outputs (OUT and SEQ) function as before. If the START/STOP key is activated during this count cycle, the count will stop, the elapsed time will be displayed, the outputs will return to their "off" state, but the sequence number will not advance. This allows the WD55 to act as a "stopwatch" with a cumulative time capability and as an elapsed time controller to time and control a variable event.

ALARM OPERATION

The alarm output (Pin 25) serves several functions in the timer/sequencer mode. First, it provides a .1 sec pulse, active HIGH ("BEEP") whenever a valid key closure is detected. This provides audio feedback for use with non-tactile membrane keyboards. When counting down in a sequence mode, a single "BEEP" is enabled when the count reaches 10.0 seconds, giving an early warning of the end of cycle. When the count reaches zero, two "BEEPS" are output to give audible indication of end of cycle. This output can be buffered and used with self contained buzzers such as a Mallory Sonalert or may be used in conjunction with piezoelectric transducers (see Figure 9).

ON/OFF TIMER MODE

In the ON/OFF timer mode, the WD-55 is programmed to act as a digital programmable timer with one or two time periods which may vary from .1 sec to 999 hours. The data is input to the device by means of switches, thumbwheels, or even diodes. The use of a display is optional, which if employed, will show the current time remaining during each timing cycle. The timebase reference is again externally provided, usually from the 50 or 60 HZ AC line. Strap options are available to instruct the device as to whether it is to run one or two times, whether it is to be operated continuously or in the triggered mode, and whether the BCD switch data is to be interpreted as hours, minutes, or seconds. This mode is intended for use as a digital time delay relay, on/off timer/controller, set point timer, digital one-shot, etc. The timing is performed with digital accuracy and repeatability; it is not dependent upon bulky resistor/capacitor components and their inherent tolerance and temperature problems. For example, the WD-55 can generate a time delay of 999 hours with an accuracy of a fraction of a second with only a handful of diodes as external components, over a temp range of 0 to 55°C, a difficult feat to accomplish by analog means.

The configuration table shown in Figure 2 defines the strap and switch options required in this mode of operation.

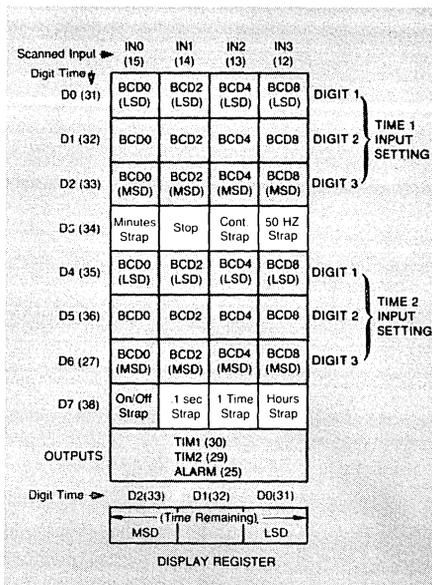


FIGURE 2 CONFIGURATION TABLE ON/OFF TIMER MODE

ON/OFF STRAP: A diode MUST be connected between D7(38) and IN0(15) to inform the WD-55 that it is to operate in this mode. This strap is scanned at the time a reset occurs and causes the microprocessor to access the ON/OFF timer program. Without the strap, the WD-55 will operate as a programmable timer/sequencer as described before.

50 HZ STRAP: As described before, the WD-55 is optimized to use a 50 or 60 HZ timebase. No strap is required for 60 HZ operation. If 50HZ is used, a diode should be connected between D3(34) and IN3(12).

.1 SEC STRAP: If this strap is present (diode between D7(38) and IN1(14)), the input data is evaluated as XX.X secs; that is, times of from .1 to 99.9 seconds are attainable. If this strap is absent and there are no minutes or hours straps present, the data is evaluated as XXX. seconds.

MINUTES STRAP: If a diode is connected between D3(34) and IN0(15), the data is evaluated as XXX minutes. That is, times of from 1 to 999 minutes are attainable.

NO. 4

HOURS STRAP: If a diode is connected between D7(38) and IN3(12), the data is evaluated as XXX hours. That is, times of from 1 to 999 hours are attainable.

TIME 1 STRAP: There are normally two time periods available with the WD-55 which are executed in sequence. If a diode is present between D7(38) and IN2(13), the device will act on only time 1. In other words, when triggered it will count down time 1 to zero, stop, and reload time 1 rather than advancing and loading time 2.

CONTINUOUS STRAP: If this strap is not present, the WD-55 will operate in the "triggered mode". A rising edge (low to high transition) at the trigger input (Pin 27) will initiate a timing cycle beginning with the current time (one or two). At the end of the cycle, the outputs return to their active low state, the next time is loaded and displayed, and the device waits for another trigger input. If a diode is connected between D3(34) and IN2(13), continuous operation is selected. Here the trigger input is ignored. This strap allows the WD-55 to operate as a dedicated purpose timer, such as a defrost controller, which begins operation upon application of power.

STOP INPUT: If an input is detected between D3(34) and IN1(14) during a timing cycle, the cycle will terminate immediately. This can allow a manual override to stop a cycle in progress. However, if the "CONTINUOUS" strap is present, this input serves only to stop the current timing cycle and cause an advance to the next time.

DATA INPUTS: The time data is input during digit times D0 to D2 (LSD to MSD) for time 1 and during D4 to D6 (LSD to MSD) for time 2 (if used), as shown in the configuration table. The data may be input by means of encoded switches, thumbwheels, or even discrete diodes. The WD-55 has on-chip pull-down resistors across inputs IN0-IN3, so that with the absence of an input during a given digit time is interpreted as a "0". Thus it would be possible to set a time of 080 hours by using only one diode. The data format must be 8421 BCD, with BCD8 connected to IN3 and BCD1 connected to IN0.

TRIGGER (PIN27): If the triggered mode is selected, a positive going transition at this input will initiate a timing cycle. This input is edge sensitive and has an internal pull-up resistor so that a momentary pushbutton switch may be used to manually trigger an event. Since this is not a scanned input, interface to other external logic is simple.

OUTPUTS

TIM1 (30): This output is active HIGH when timing cycle 1 is active, and LOW otherwise.

TIM2 (29): This output is active HIGH when timing cycle 2 is active, and LOW otherwise.

ALARM (25): This output is logic LOW when a timing cycle (1 or 2) is in progress and is logic HIGH otherwise. It may be buffered to drive an audible alarm or it may be used as a third timing output to turn a single device on for two different intervals.

INITIALIZATION

A logic low of sufficient duration on Pin 8 (RESET) will cause initialization of the WD55. In the on/off timer mode, TIM1, TIM2, and alarm will be logic low, and the first time (TIME 1) data is loaded into the display register. If the CONTINUOUS mode is selected, the device will immediately begin counting down time 1, else it will wait for a trigger pulse to occur.

APPLICATIONS CIRCUITS

The following are several circuits designed to give the user an idea of the range of applications that the WD-55 is capable of being utilized.

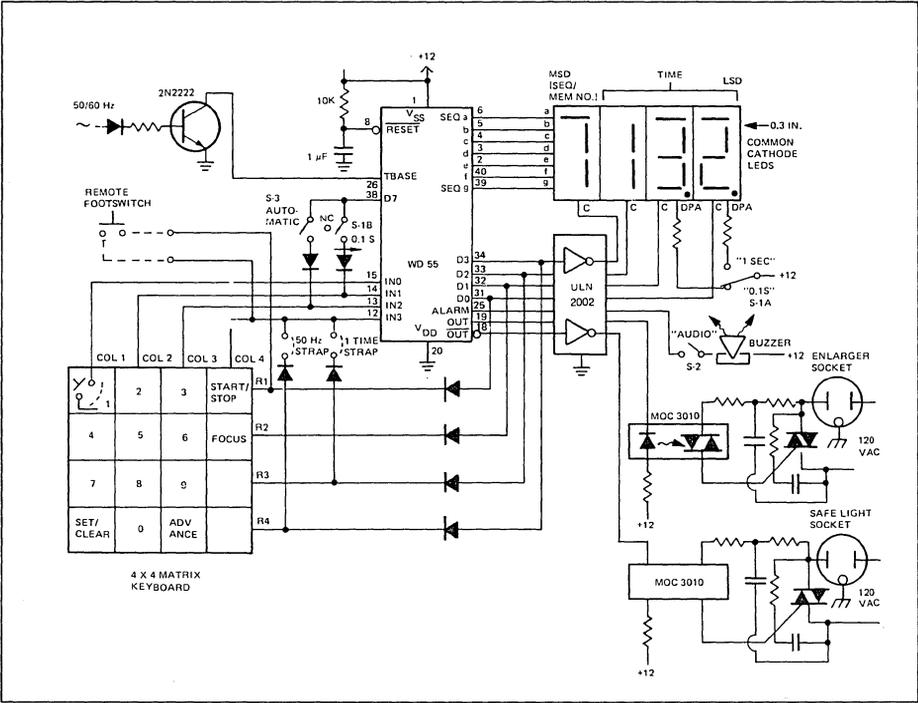


FIGURE 3 DARKROOM TIMER

DARKROOM TIMER

Figure 3 shows a complete schematic (except for power supply) of a dark room timer/controller using the WD-55. Note that the only external components required are a display, a digit driver, keyboard, and output switching devices. A 4-digit common-cathode LED display is used since their inherently red radiation is desirable for dark room environments. Note that the high current sourcing capability of the WD-55 segment outputs allows easy drive of instrument-size LEDs. The time base is provided by shaping up the 50/60HZ AC line input to Pin 26 (TBASE). A complete matrix keyboard is used to allow access to all 7 memory locations. A DPDT switch (S1) is used to select a resolution of .1 or 1 seconds and to simultaneously move the decimal point.

A good dark room timer/controller normally has two switched AC outlets, one for the enlarger and one for the "safe" light. They are the complements of each other in that the safe light is "on" when the enlarger

is not active and is "off" when the enlarger is printing. The circuit shown makes use of the complementary outputs OUT (19) and OUT (18) to allow solid-state switching in the form of optically-isolated triacs by buffering them through two unused sections of the high-current digit driver. The value of "snubber" components depends upon the load, which in the case of enlargers and safe lamps is often inductive. If desired, a single SPDT relay may be used in place of the triacs and opto-isolators shown.

The buzzer shown is of the self-contained oscillator variety and operates with DC drive. The WD-55 may also be used with piezoelectric elements (see Figure 9). A switch is provided to disable the beeper when not desired. Another switch (S-3) is used to enable the automatic mode for making up to 7 sequential timed prints by depressing the start key only once. If the possibility of depressing two keys exists, the keyboard should be diode isolated to avoid "sneak" paths.

SECTION
4

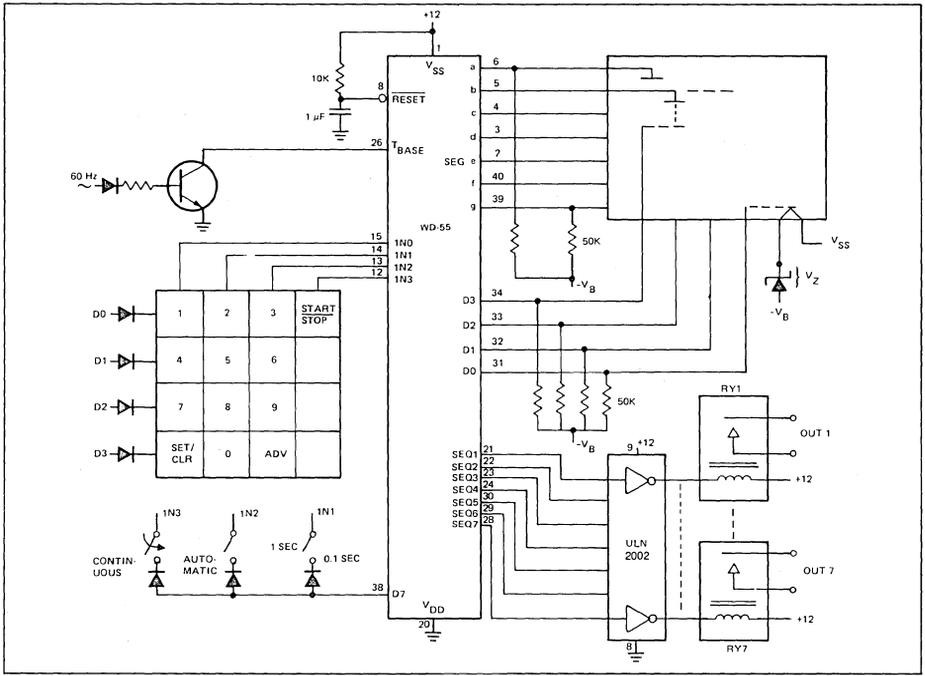


FIGURE 4 SEQUENCER WITH V-F DISPLAY

Figure 4 shows the WD-55 used to implement a keyboard programmable sequencer with 7 outputs. It features a vacuum-fluorescent (V-F) display which takes advantage of the fact that the WD-55 can drive it directly with no high voltage buffers — only external pull-down resistors are required. A conventional matrix keyboard is used as in the dark room timer

application. Toggle switches are provided to allow strap options for .1 sec resolution and user-selectable continuous operation. In the auto-continuous mode, once set up, the 7 sequencer outputs will operate in succession to cycle up to 7 processes. The sequencer outputs are buffered by a high current driver interface to 7 relays which perform the output switching task.

20-1010

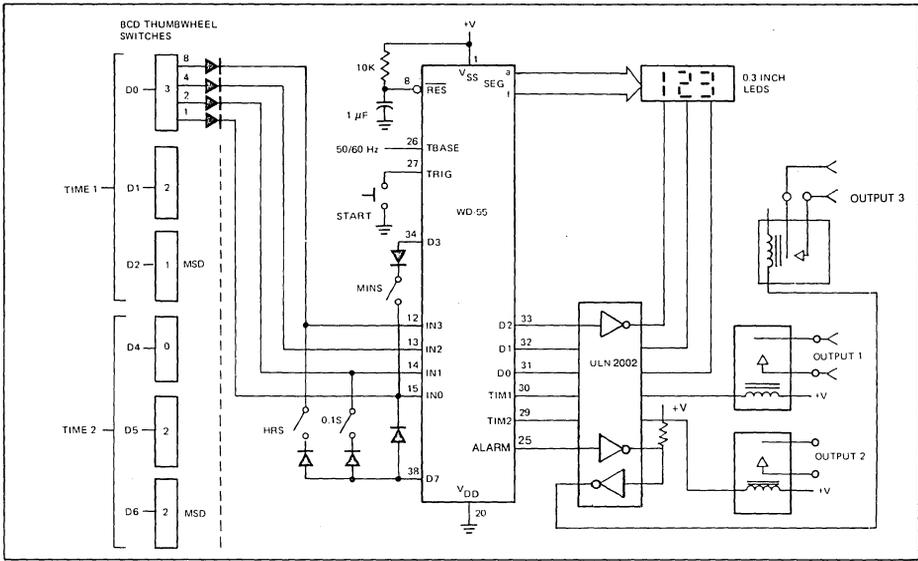


FIGURE 5 THUMBWHEEL PROGRAMMABLE INTERVAL TIMER

Figure 5 shows the WD-55 in its second mode of operation, that of a switch programmable on/off or interval timer. The circuit shown has three relay switched outputs, labelled one, two, and three. Output one is active for the duration of time 1, output two is active for the duration of time 2, and output three is active for the duration of both one and two.

Timing data is input through 6 BCD-encoded thumbwheel switches. Three SPST switches inform

the WD-55 to interpret this data as NN.N seconds, NNN seconds, NNN minutes, or NNN hours. The LED display will show the time remaining and the countdown when operating. Since the data is input through switches, the display may be deleted if this feature is not desired. Also, since the timing information is read from switches, the data is non-volatile and no battery backup would be required of the device.

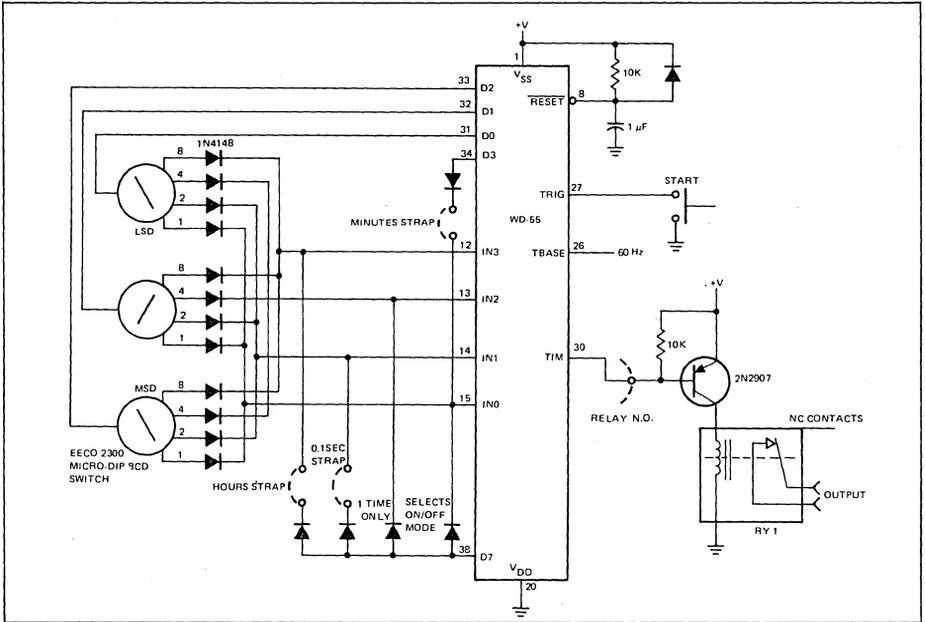


FIGURE 6 DIGITAL TIME DELAY RELAY

Figure 6 shows a digital programmable time delay relay using the WD-55 to give "ON" or "OFF" time delays of from .1S to 999 hours. the "Time 1 only" strap option is used here so that when triggered, the device loads and counts down only one time and

then resets. Simple screw-driver slot programmable DIP switches are used here for low cost. Note that a display is not required, but could be added to produce a unique time delay relay with digital readout of time remaining.

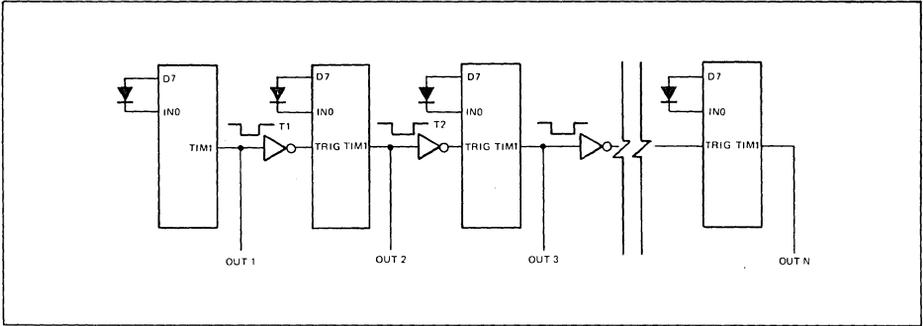


FIGURE 8 DAISY-CHAIN N-SEQUENTIAL INTERVAL CONTROLLER

Finally, Figure 8 shows how multiple, independent WD-55's may be configured for triggered mode operation may operate in daisy chain fashion to produce an N-sequential programmable interval controller.

These are but a few of the many applications for the WD-55. For custom versions, please contact the factory.

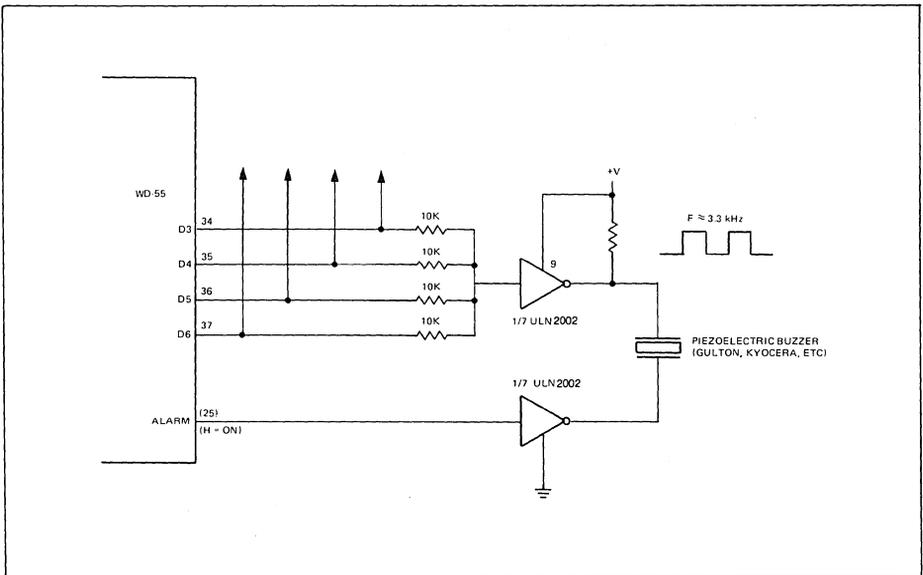


FIGURE 9 WD-55 USED WITH PIEZOELECTRIC BUZZER

SOLUTIONS 4

ABSOLUTE MAXIMUM RATINGS

Storage Temperature -65°C to +150°C Ceramic
 -55°C to +125°C Plastic
 Operating Free-Air Temperature
 T Range 0°C to 70°C
 Lead Temperature (Soldering, 10 sec.) 300°C
 Power Dissipation 2.5 Watt at 25°C
 Positive Voltage on any Pin with Respect to
 V_{SS}: +0.3V

Negative Voltage on any Pin with Respect to
 V_{SS}: 20.0V

Absolute maximum ratings indicate limits beyond
 which damage to the device may occur. DC and AC
 electrical specifications are not ensured when operat-
 ing the device at absolute maximum ratings.

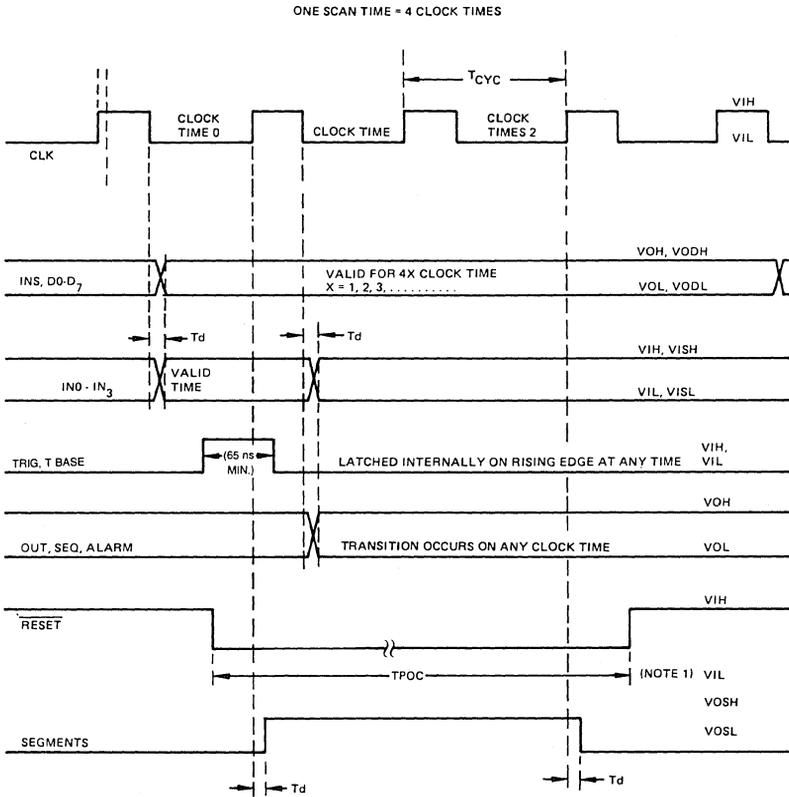
ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{SS}-V_{DD} = 13.2V unless noted otherwise

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage (V _{SS} -V _{DD})		11.5	13.2	14.5	V
Operating Current	All inputs and outputs open	6		15	mA
Input Voltage Levels All Inputs Except IN0-IN3 Logic High (V _{IH}) Logic Low (V _{IL}) Inputs IN0-IN3 Logic High (V _{ISH}) Logic Low (V _{ISL})	Note 1 Note 2	V _{SS} -1 V _{DD} V _{SS} -3.75 V _{DD}		V _{SS} V _{DD} -4.2 V _{SS} V _{SS} -9.0	V V V V
Output Voltage Levels All Outputs Except D0-D7 and SA-SG Logic High (V _{OH}) Logic Low (V _{OL}) D0-D7 Outputs Logic High (V _{ODH}) V _{ODL} Seg Outputs Seg a-f	I _{OH} =+100 μA Min. I _{OL} =-1.6 mA Min. I _{ODH} =1.5 mA I _{ODH} =1.5 mA+I Input (IN0-IN3) I _{ODH} =5.0 mA+1 Input Note 3 I _{OSH} =16 mA	V _{SS} -2 V _{DD} V _{SS} -1.5 V _{SS} -3.0 V _{SS} -3.5		V _{SS} V _{SS} -4.6 V _{SS} V _{SS} V _{SS} 1.0	V V V V V V
Segment Output Current Seg a-f I _{OSH}	Note 3	10	15	40	mA
AC Electrical T _{cYC}			10		μs
Reset T _{Base} Timing error (TOUT)	Note 4	15 0	60	500 ±1	msec HZ ms

- Note 1: Internal Pullup Resistors of Approximately 6K to V_{SS} Across Each Input.
- Note 2: Internal Pulldown Resistors of Approximately 12K to V_{DD} Across Each Input.
- Note 3: Single Transistor to V_{SS} Output Only.
- Note 4: T_{Base} = 60.000 HZ.

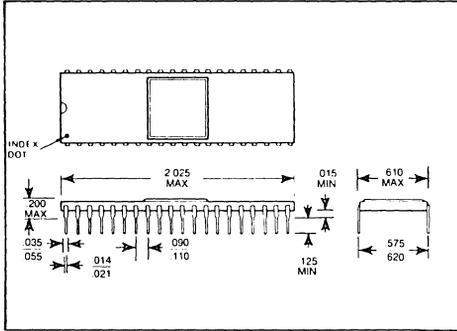
4 20-10ms



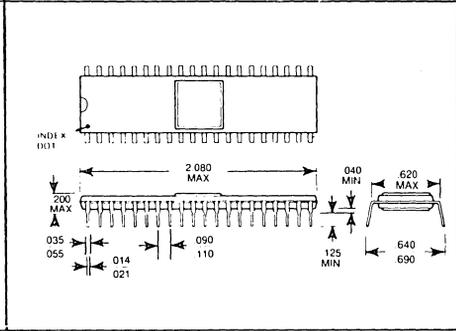
NOTE 1: RISING EDGE OF RESET GENERATES SCAN TIME 0 WITHIN 4 CLOCK TIMES

Note 2: $t_d = \mu s$ MAX

WD-55 TIMING DIAGRAM



WD55A CERAMIC PACKAGE



WD55B PLASTIC PACKAGE

SUPPORT: Application and Design Support is available from Western Digital Corporation

ORDERING INFORMATION: WD55A for 40 Pin Ceramic Package
WD55B for 40 Pin Plastic Package

SECTION 4

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WESTERN DIGITAL CORPORATION

WD4020 ROMless N-Channel Microcontrollers

September, 1980

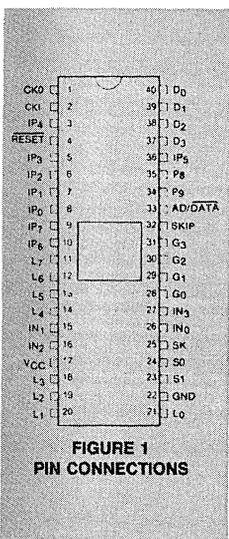
FEATURES

- LOW COST
- EXACT CIRCUIT EQUIVALENT OF WD4200
- STANDARD 40-PIN DUAL-IN-LINE PACKAGE
- INTERFACES WITH STANDARD PROM OR ROM
- 64 x 4 RAM, ADDRESSES UP TO 1K x 8 ROM
- POWERFUL INSTRUCTION SET
- TRUE VECTORED INTERRUPT, PLUS RESTART
- THREE-LEVEL SUBROUTINE STACK
- 4.0 μ s INSTRUCTION TIME
- SINGLE SUPPLY OPERATION (4.5 V TO 6.3 V)
- INTERNAL TIME-BASE COUNTER FOR REALTIME PROCESSING
- INTERNAL BINARY COUNTER REGISTER WITH SERIAL I/O CAPABILITY

- SOFTWARE/HARDWARE COMPATIBLE WITH OTHER MEMBERS OF WD4000 FAMILY

GENERAL DESCRIPTION

The WD4020 ROMless Microcontrollers are members of the Control Oriented Processor (COP) family, fabricated using N-channel, silicon gate MOS technology. Each part contains CPU, RAM and I/O, and is identical to a WD4200 device, except the ROM has been removed; pins have been added to output the ROM address to input ROM data. In a system, the WD4020 performs exactly like the WD4200; this important benefit facilitates development and debug of a WD4200 program prior to masking the final part. These devices are also appropriate in low volume applications, or when the program may require changing.



**FIGURE 1
PIN CONNECTIONS**

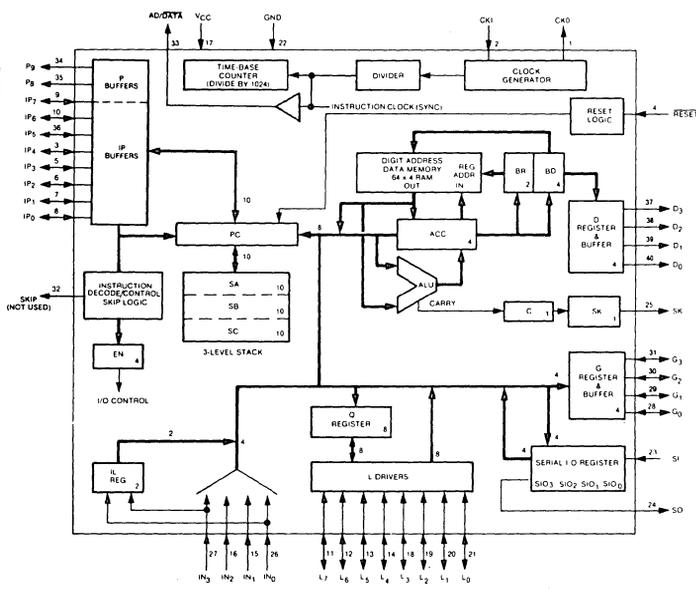


FIGURE 2 WD4020 BLOCK DIAGRAM

SECTION 4

Pin No.	Symbol	Description
1	CKO	System oscillator output
2	CKI	System oscillator input
3,5,6,7,8, 9,10,36	IP ₀ - IP ₇	8 bidirectional ROM address and data ports
4	$\overline{\text{RESET}}$	System reset input
11,12,13,14, 18,19,20,21	L ₀ - L ₇	8 bidirectional I/O ports with TRI-STATE [®]
15,16,26,27	IN ₀ - IN ₃	4 general purpose inputs
17	V _{CC}	Power supply
22	GND	Ground
23	SI	Serial input (or counter input)
24	SO	Serial output (or general purpose output)
25	SK	Logic-controlled clock (or general purpose output)
28,29,30,31	G ₀ - G ₃	4 bidirectional I/O ports
32	SKIP	Instruction skip output
33	AD/ $\overline{\text{DATA}}$	Address out/data in flag
34, 35	P ₈ - P ₉	2 ROM address outputs
37,38,39,40	D ₀ - D ₃	4 general purpose outputs

Absolute Maximum Ratings

Voltage at Any Pin Relative to GND:	-0.5V to + 7V
Ambient Operating Temperature	0°C to +70°C
WD4020A,B	
WD4020AE, BE:	-40°C to +85°C
Ambient Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	0.75 Watt at 25°C
	0.4 Watt at 70°C

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +70°C, 4.5V ≤ V_{CC} ≤ 6.3V unless otherwise noted.

Parameter	Conditions	Min	Max	Units
Operating Voltage (V _{CC})		4.5	6.3	V
Operating Supply Current	V _{CC} = 5V, T _A = 25°C (all inputs and outputs open)		30	mA
Input Voltage Levels				
CKI Input Levels				
Logic High (V _{IH})		2.0		V
Logic Low (V _{IL})			0.4	V
RESET Input Levels				
Logic High		0.7 V _{CC}		V
Logic Low			0.6	V
RESET Hysteresis		1.0		V
SO Input Level (Test mode)		2.0	3.0	V
All Other Inputs				
Logic High	V _{CC} = max	3.0		V
Logic High	V _{CC} = 5V ± 5%	2.0		V
Logic Low			0.8	V
Output Voltage Levels (Note 2)				
TTL Operation				
Logic High (V _{OH})	V _{CC} = 5V ± 5%	2.4		V
Logic Low (V _{OL})	I _{OH} = 100µA I _{OL} = -1.6mA		0.4	V
CMOS Operation				
Logic High (V _{OH})	I _{OH} = 10µA	V _{CC} - 1		V
Logic Low (V _{OL})	I _{OL} = -10µA		0.2	V
Output Current Levels				
LED Direct Drive Output				
Logic High (I _{OH})	V _{CC} = 6V V _{OH} = 2.0V	2.5	14	mA
TRI-STATE* Output		-10	+10	µA
Leakage Current				



AC ELECTRICAL CHARACTERISTICS $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 6.3\text{V}$ unless otherwise noted.

Parameter	Conditions	Min	Max	Units
Instruction Cycle Time— t_c CKI Using Crystal Input Frequency— f_1 Duty Cycle (Note 2)	figure 3a +16 mode figure 3a	4 1.6 30	10 4 55	μs MHz %
INPUTS: $\text{IN}_3\text{--}\text{IN}_0$, $\text{G}_3\text{--}\text{G}_0$, $\text{L}_7\text{--}\text{L}_0$ t_{SETUP} t_{HOLD} SI , $\text{IP}_7\text{--}\text{IP}_0$ t_{SETUP} t_{HOLD}		1.7 100 0.3 100		μs ns μs ns
OUTPUTS: COP TO CMOS PROPAGATION DELAY SK as a Logic-Controlled Clock t_{PD1} t_{PD0} SO, SK as a Data Output t_{PD1} t_{PD0} t_{PD1} $\text{D}_3\text{--}\text{D}_0$, $\text{G}_3\text{--}\text{G}_0$ t_{PD1} t_{PD0} $\text{L}_7\text{--}\text{L}_0$ (LED Direct Drive) t_{PD1} t_{PD0}	$4.5\text{V} \leq V_{CC} \leq 6.3\text{V}$, $C_L = 50\text{pF}$, $V_{OH} = 0.7 V_{CC}$, $V_{OL} = 0.3 V_{CC}$ $V_{OH} = 2\text{V}$ $V_{OH} = 2\text{V}$		1.1 0.3 1.4 0.3 0.7 1.6 0.6 2.4 0.4	μs μs μs μs μs μs μs μs μs
COP TO TTL PROPAGATION DELAY AD/DATA t_{PD1} t_{PD0} SKIP t_{PD1} t_{PD0}	fanout = 1 Standard TTL Load $V_{CC} = 5\text{V} \pm 5\%$, $C_L = 50\text{pF}$, $V_{OH} = 2.4\text{V}$, $V_{OL} = 0.4\text{V}$		0.5 0.5 0.6 0.6	μs μs μs μs
SK as a Logic-Controlled Clock t_{PD1} t_{PD0} SK as a Data Output, SO t_{PD1} t_{PD0}			0.8 0.8 1.0 1.0	μs μs μs μs

AC ELECTRICAL CHARACTERISTICS (continued) $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 6.3\text{V}$ unless otherwise noted.

Parameter	Conditions	Min	Max	Units
OUTPUTS (cont.):				
D ₃ -D ₀ , G ₃ -G ₀				
t _{PD1}			1.3	μs
t _{PD0}			1.3	μs
L ₇ -L ₀				
t _{PD1}			1.4	μs
t _{PD0}			0.4	μs
IP ₇ -IP ₀ , P ₉ , P ₈				
t _{PD1}			1.5	μs
t _{PD0}			1.5	μs
CKO (figure 3b)				
t _{PD1}			0.2	μs
t _{PD0}			0.2	μs

Note 1: Duty Cycle = $t_{WI}/(t_{WI} + t_{WO})$.

Note 2: See WD4200 data sheet for additional I/O characteristics and instruction set description

Note 3: I/O options on WD4020 are: CKI/CKO = "xtal osc," L-PORT = "LED direct drive," IN-PORT, SI, RESET = "pullup," G, D-PORTS, SO, SK = "standard out," FUNCTION = "non-microbus™."

*TRI-STATE, MICROBUS are copyrighted by National Semiconductor Corporation

SMT-1015

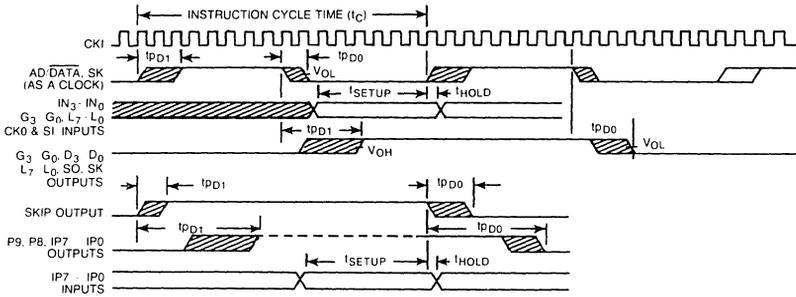


Figure 3a. Input/Output Timing Diagrams (Crystal \div 16 Mode)

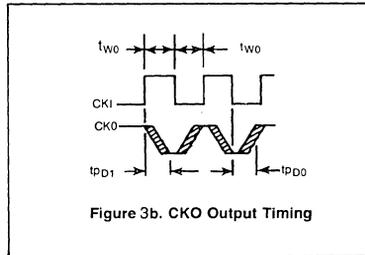
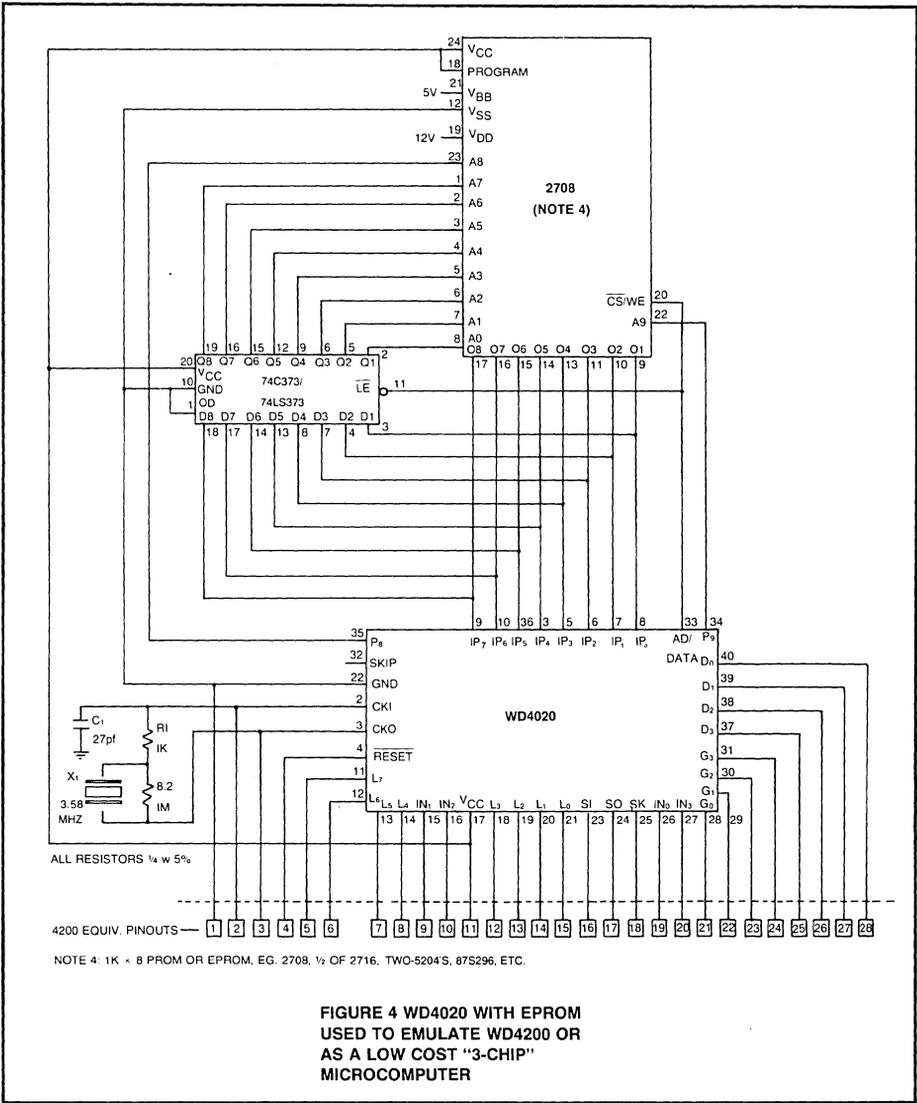


Figure 3b. CKO Output Timing



**FIGURE 4 WD4020 WITH EPROM
USED TO EMULATE WD4200 OR
AS A LOW COST "3-CHIP"
MICROCOMPUTER**

WESTERN DIGITAL

C O R P O R A T I O N

WD4200/WD4210 Single-Chip N-Channel Microcontrollers

FEATURES

- Low cost
- Powerful instruction set
- 1K x 8 ROM, 64 x 4 RAM
- 23 I/O lines (WD4200)
- True vectored interrupt, plus restart
- Three-level subroutine stack
- 4.0 μ s instruction time
- Single supply operation (4.5V to 6.3V)
- Internal time-base counter for real-time processing
- Internal binary counter register with serial I/O capability
- General purpose and TRI-STATE[®] outputs
- TTL/CMOS compatible in and out
- LED direct drive outputs
- MICROBUS[™] compatible
- Software/hardware compatible with other members of WD4200 family
- Extended temperature range device available (-40°C to +85°C)

GENERAL DESCRIPTION

The WD4200 and WD4210 Single-Chip N-Channel Microcontrollers are members of the Control Oriented Processor family, fabricated using N-channel, silicon gate MOS technology. They are complete microcomputers containing all system timing, internal logic, ROM, RAM and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture and I/O scheme designed to facilitate keyboard input, display output and BCD data manipulation. The WD4210 is identical to the WD4200, except with 19 I/O lines instead of 23. They are an appropriate choice for use in numerous human interface control environments. Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized Control Oriented Processor at a low end-product cost.

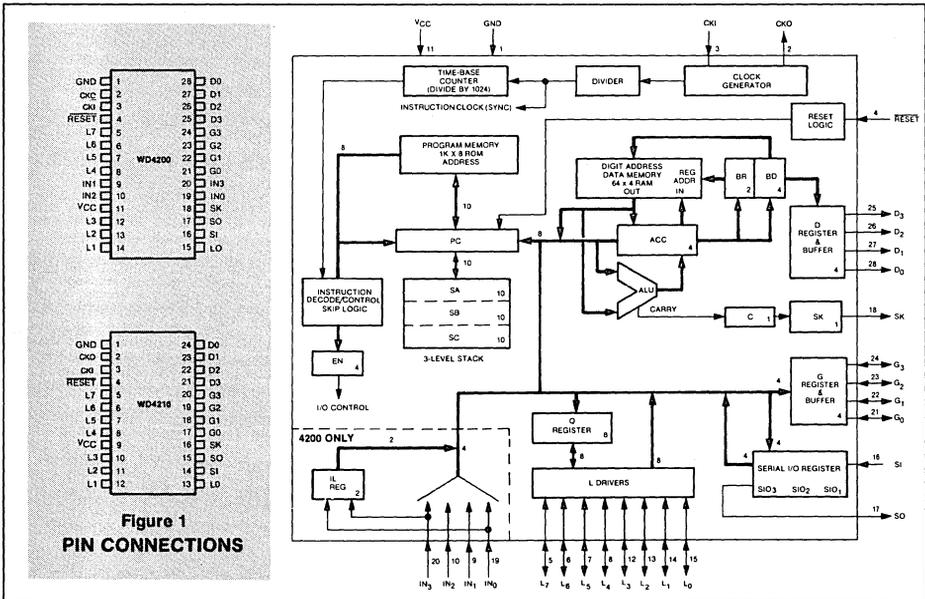


Figure 2 WD4200/4210 BLOCK DIAGRAM

PIN DESCRIPTION	
L7-L0	8 bidirectional I/O ports with TRI-STATE®
G3-G0	4 bidirectional I/O ports
D3-D0	4 general purpose outputs
IN3-IN0	4 general purpose inputs (WD4200 only)
SI	Serial input (or counter input)
SO	Serial output (or general purpose output)
SK	Logic-controlled clock (or general purpose output)
CKI	System oscillator input
CKO	System Oscillator output (or general purpose input or RAM power supply)
RESET	System reset input
VCC	Power supply
GND	Ground

FUNCTIONAL DESCRIPTION

A block diagram of the WD4200 is given on page 1. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. Positive logic is used. When a bit is set, it is logic "1" (greater than 2 volts). When a bit is reset, it is a logic "0" (less than 0.8 volts).

Program Memory

Program Memory consists of a **1,024-byte ROM**. As can be seen by an examination of WD4200/4210 instruction set, these words may be program instructions, program data or ROM addressing data. Because of the special characteristics associated with the JP, JSRP, JID and LQID instructions, ROM must often be thought of as being organized into 16 pages of 64 words each.

ROM addressing is accomplished by a **10-bit PC register**. Its binary value selects one of the 1,024 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential 10-bit binary count value. Three levels of subroutine nesting are implemented by the **10-bit subroutine save registers, SA, SB and SC**, providing a last-in, first-out (LIFO) hardware subroutine stack.

ROM instruction words are fetched, decoded and executed by the Instruction Decode, Control and Skip Logic circuitry.

Data Memory

Data Memory consists of a **256-bit RAM**, organized as four data registers of 16 4-bit digits. RAM addressing is implemented by a **6-bit B register** whose upper two bits (Br) select one of four data registers and lower 4 bits (Bd) select one of 16 4-bit digits in

the selected data register. While the 4-bit contents of the selected **RAM digit (M)** is usually loaded into or from, or exchanged with, the A register (accumulator), it may also be loaded into or from the Q latches or loaded from the L ports. RAM addressing may also be performed directly by the LDD and XAD instructions based upon the 6-bit contents of the operand field of these instructions. The Bd register also serves as a source register for 4-bit data sent directly to the D outputs.

Internal Logic

The 4-bit **A register** (accumulator) is the source and destination register for most I/O, arithmetic, logic and data memory access operations. It can also be used to load the Br and Bd portions of the B register, to load and input four bits of the 8-bit Q latch data, to input four bits of the 8-bit L I/O port data and to perform data exchanges with the SIO register.

A **4-bit adder** performs the arithmetic and logic functions of the WD4200/4210, storing its results in A. It also outputs a carry bit to the 1-bit **C register**, most often employed to indicate arithmetic overflow. The C register, in conjunction with XAS instruction and the EN register, also serves to control the SK output. C can be outputted directly to SK or can enable SK to be a sync clock each instruction cycle time (see XAS instruction and EN register description below).

Four **general-purpose inputs, IN₃-IN₀**, are provided; IN₁, IN₂ and IN₃ may be selected, by a mask-programmable option, as Read Strobe, Chip Select and Write Strobe inputs, respectively, for use in MICROBUS™ applications.

The **D register** provides four general-purpose outputs and is used as the destination register for the 4-bit contents of Bd.

The **G register** contents are outputs to four general-purpose bidirectional I/O ports. G₀ may be mask-programmed as an output for MICROBUS™ applications.

The **Q register** is an internal, latched, 8-bit register, used to hold data loaded to or from M and A, as well as 8-bit data from ROM. Its contents are output to the L I/O ports when the L drivers are enabled under program control (see LEI instruction). With the MICROBUS™ option selected, Q can also be loaded with the 8-bit contents of the L I/O ports upon the occurrence of a write strobe from the host CPU.

The **eight L drivers**, when enabled, output the contents of latched Q data to the L I/O ports. Also, the contents of L may be read directly into A and M. As explained above, the MICROBUS™ option allows L I/O port data to be latched into the Q register. L I/O ports can be directly connected to the segments of a multiplexed LED display (using the LED Direct Drive output configuration option) with

Q data being outputted to the Sa-Sg and decimal point segments of the display.

The **SIO register** functions as a 4-bit serial-in/serial-out shift register or as a binary counter depending on the contents of the EN register (see EN register description below). Its contents can be exchanged with A, allowing it to input or output a continuous serial data stream. SIO may also be used to provide additional parallel I/O by connecting SO to external serial-in/serial-out shift registers. For example of additional parallel output capacity, see Application No. 2.

The **EN register** is an internal 4-bit register loaded under program control by the LEI instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register (EN₃-EN₀).

1. The least significant bit of the enable register, EN₀, selects the SIO register as either a 4-bit shift register or a 4-bit binary counter. With EN₀ set, SIO is an asynchronous binary counter, *decrementing* its value by one upon each low-going pulse ("1" to "0") occurring on the SI input. Each pulse must be at least two instruction cycles wide. SK outputs the value of C upon execution of XAS and remains the same until the execution of another XAS instruction. The SO output is equal to the value of EN₃. With EN₀ reset, SIO is a serial shift register shifting left each instruction cycle time. The data present at SI goes into the least significant bit of SIO. SO can be enabled to output the most significant bit of SIO each cycle time (see 4 below). The SK output becomes a logic-controlled clock, providing a SYNC signal each instruction time. It will start outputting a SYNC pulse upon the execution of an XAS instruction with C = 1, stopping upon the execution of a subsequent XAS with C = 0.
2. With EN₁ set the IN₁ input is enabled as an interrupt input. Immediately following an interrupt, EN₁ is reset to disable further interrupts.

3. With EN₂ set, the L drivers are enabled to output the data in Q to the L I/O ports. Resetting EN₂ disables the L drivers, placing the L I/O ports in a high-impedance input state. If the MICROBUS™ option is being used, EN₂ does not affect the L drivers.
4. EN₃, in conjunction with EN₀, affects the SO output. With EN₀ set (binary counter option selected) SO will output the value loaded into EN₃. With EN₀ reset (serial shift register option selected), setting EN₃ enables SO as the output of the SIO shift register, outputting serial shifted data each instruction time. Resetting EN₃ with the serial shift register option selected disables SO as the shift register output; data continues to be shifted through SIO and can be exchanged with A via an XAS instruction but SO remains reset to "0". The table below provides a summary of the modes associated with EN₃ and EN₀.

Interrupt

The following features are associated with the IN₁ interrupt procedure and protocol and must be considered by the programmer when utilizing interrupts.

- a. The interrupt, once acknowledged as explained below, pushes the next sequential program counter address (PC + 1) onto the stack, pushing in turn the contents of the other subroutine-save register to the next lower level (PC+1 → SA → SB → SC). Any previous contents of SC are lost. The program counter is set to hex address OFF (the last word of page 3) and EN₁ is reset.
- b. An interrupt will be acknowledged only after the following conditions are met:
 - 1) EN₁ has been set.
 - 2) A low-going pulse ("1" to "0") of at least two instruction cycles wide occurs on the IN₁ input.
 - 3) A currently executing instruction has been completed.

ENABLE REGISTER MODES — BITS EN₃ AND EN₀

EN ₃	EN ₀	SIO	SI	SO	SK AFTER XAS
0	0	Shift Register	Input to Shift Register	0	If C = 1, SK = SYNC If C = 0, SK = 0
1	0	Shift Register	Input to Shift Register	Serial Out	If C = 1, SK = SYNC If C = 0, SK = 0
0	1	Binary Counter	Input to Binary Counter	0	If C = 1, SK = 1 If C = 0, SK = 0
1	1	Binary Counter	Input to Binary Counter	1	If C = 1, SK = 1 If C = 0, SK = 0



- 4) All successive transfer of control instructions and successive LBIs have been completed (e.g., if the main program is executing a JP instruction which transfers program control to another JP instruction, the interrupt will not be acknowledged until the second JP instruction has been executed.
- c. Upon acknowledgement of an interrupt, the skip logic status is saved and later restored upon the execution of a subsequent RET instruction. For example, if an interrupt occurs during the execution of ASC (Add with Carry, Skip on Carry) instruction which results in carry, the skip logic status is saved and program control is transferred to the interrupt servicing routine at hex address 0FF. At the *end* of the interrupt routine, a RET instruction is executed to "pop" the stack and return program control to the instruction following the original ASC. *At this time*, the skip logic is enabled and skips this instruction because of the previous ASC carry. Since, as explained above, it is the RET instruction which enables the previously saved status of the skip logic, subroutines should not be nested within the interrupt servicing routine since their RET instruction will enable any previously saved main program skips, interfering with the orderly execution of the interrupt routine.
- d. The first instruction of the interrupt routine at hex address 0FF must be a NOP.
- e. A LEI instruction can be put immediately before the RET to re-enable interrupts.

MICROBUS™ Interface

The WD4200 has an option which allows it to be used as a peripheral microprocessor device, inputting and outputting data from and to a host microprocessor (μ P). IN_1 , IN_2 , and IN_3 general purpose inputs become MICROBUS™ compatible read-strobe, chip-select, and write-strobe lines, respectively. IN_1 becomes \overline{RD} — a logic "0" on this input will cause Q latch data to be enabled to the L ports for input to the μ P. IN_3 becomes \overline{CS} — a logic "0" on this line selects the WD4200 as the μ P peripheral device by enabling the operation of the \overline{RD} and \overline{WR} lines and allows for the selection of one of several peripheral components. IN_3 becomes \overline{WR} — a logic "0" on this line will write bus data from the L ports to the Q latches for input to the WD4200. G_0 becomes \overline{INTR} a "ready" output, reset by a write pulse from the μ P on the \overline{WR} line, providing the "hand-shaking" capability necessary for asynchronous data transfer between the host CPU and the WD4200.

This option has been designed for compatibility with National's MICROBUS™ — a standard interconnect system for 8-bit parallel data transfer between MOS/LSI CPUs and interfacing devices. (See MICROBUS™, National Publication.) The functioning and timing

relationships between the WD4200 signal lines affected by this option are as specified for the MICROBUS™ interface, and are given in the AC electrical characteristics and shown in the timing diagrams (figures 11 and 12). Connection of the WD4200 to the MICROBUS™ is shown in MICROBUS™ Option interconnect illustration.

Initialization

The Reset Logic, internal to the WD4200/4210 will initialize (clear) the device upon power-up if the power supply rise time is less than 1 ms and greater than 1 μ s. If the power supply rise time is greater than 1 ms, the user must provide an external RC network and diode to the \overline{RESET} pin as shown below. The \overline{RESET} pin is configured as a Schmitt trigger input. If not used it should be connected to V_{CC} . Initialization will occur whenever a logic "0" is applied to the \overline{RESET} input, provided it stays low for at least two instruction cycle times.

Upon initialization, the **PC register is cleared to 0** (ROM address 0) and the **A, B, C, D, EN, and G registers are cleared**. The **SK output is enabled as a SYNC output**, providing a pulse each instruction cycle time. **Data Memory (RAM) must be cleared by the user's program**. The first instruction at address 0 must be a CLRA.

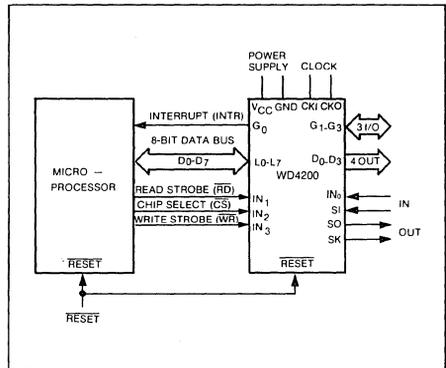


Figure 3 MICROBUS™ OPTION INTERCONNECT

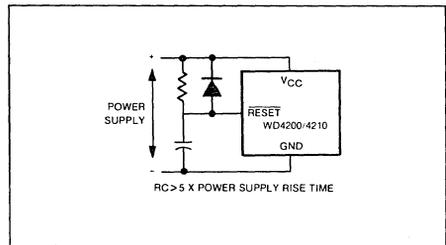


Figure 4 POWER-UP CLEAR CIRCUITS

Oscillator

There are four basic clock oscillator configurations available as shown below.

- Crystal Controlled Oscillator.** CKI and CKO are connected to an external crystal. The instruction cycle time equals the crystal frequency divided by 16 (optional by 8).
- External Oscillator.** CKI is configured as a TTL compatible input accepting an external clock signal. The external frequency is divided by 16 (optional by 8 or 4) to give the instruction cycle time. CKO is now available to be used as the RAM power supply (V_R) or as a general purpose input.
- RC Controlled Oscillator.** CKI is configured as a single pin RC controlled Schmitt trigger oscillator. The instruction cycle equals the oscillation frequency divided by 4. CKO is available for non-timing functions.
- Externally Synchronized Oscillator.** Intended for use in multi-WD systems, CKO is programmed to function as an input connected to the SK out-

put of another WD4200/4210 with CKI connected as shown. In this configuration, the SK output connected to CKO must provide a SYNC (instruction cycle) signal to CKO, thereby allowing synchronous data transfer between the WDs using only the SI and SO serial I/O pins in conjunction with the XAS instruction. Note that on power-up SK is automatically enabled as a SYNC output (see Functional Description, Initialization, above).

CKO Pin Options

In a crystal controlled oscillator system, CKO is used as an **output to the crystal network**. As an option CKO can be a **general purpose input**, read into bit 2 of A (accumulator) upon execution of an INIL instruction. As another option, CKO can be a **RAM power supply pin (V_R)**, allowing its connection to be a standby/backup power supply to maintain the integrity of RAM data with minimum power drain when the main supply is inoperative or shut down to conserve power. Using either option is appropriate in applications where the WD4200/4210 system timing configuration does not require use of the CKO pin.

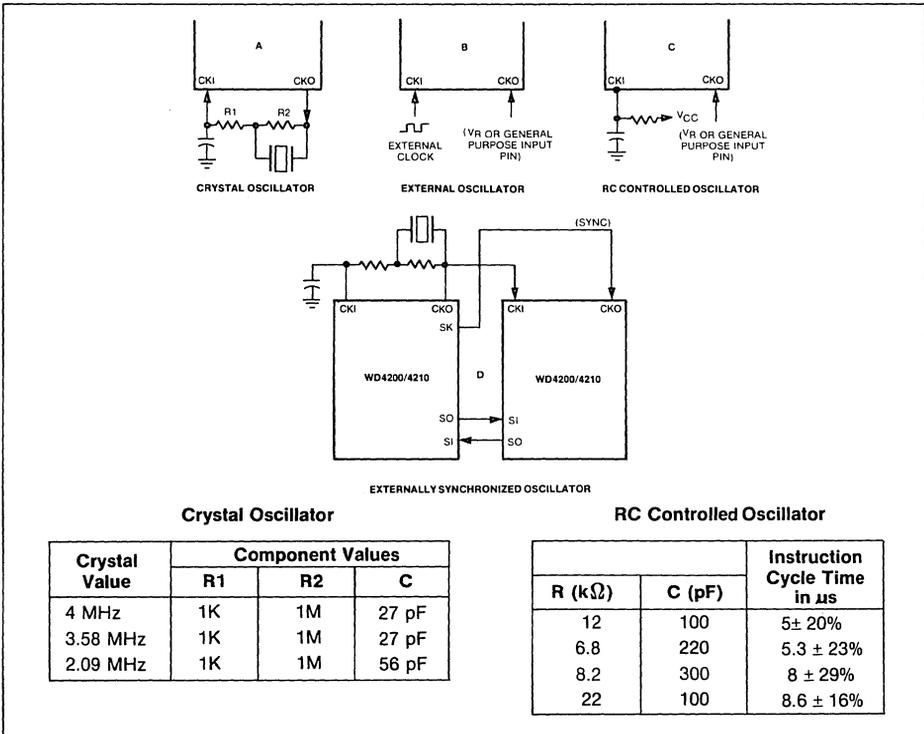


Figure 5 WD4200/4210 OSCILLATOR

I/O Options

WD4200/4210 outputs have the following optional configurations, illustrated below.

- Standard.** An enhancement-mode device to ground in conjunction with a depletion-mode device to V_{CC} compatible with TLL and CMOS input requirements.
- Open-Drain.** An enhancement-mode device to ground only, allowing external pull-up as required by the user's application.
- Push-Pull.** An enhancement-mode device to ground in conjunction with a depletion-mode device paralleled by an enhancement-mode device to V_{CC} . This configuration has been provided to allow for fast rise and fall times when driving capacitive loads.
- LED Direct Drive.** An enhancement-mode device to ground and to V_{CC} , meeting the typical current sourcing requirements of the segments of an LED display. The sourcing device is clamped to limit current flow. These devices may be turned off under program control (see Functional Description, EN Register), placing the outputs in a high-impedance state to provide required LED segment blanking for a multiplexed display.
- TRI-STATE® Push-Pull.** An enhancement-mode device to ground and V_{CC} intended to meet the requirements associated with the MICROBUS™ option. These outputs are TRI-STATE® outputs, allowing for connection of these outputs to a data bus shared by other bus drivers.

WD4200/4210 inputs have the following optional configurations:

- An on-chip depletion load device to V_{CC} .
- A Hi-Z input** which must be driven to a "1" or "0" by external components.

The above input and output configurations share common enhancement-mode and depletion-mode devices. Specifically, all configurations use one or more of six devices (numbered 1-6, respectively). Minimum and maximum current (I_{OUT} and V_{OUT}) curves are given on figure 7 for each of these devices to allow the designer to effectively use these I/O configurations in designing a WD4200/4210 system.

The SO, SK outputs can be configured as shown in A, B, or C. The D and G outputs can be configured as shown in A or B. Note that when inputting data to the G ports, the G outputs should be set to "1". The L outputs can be configured as A, B, D, or E.

An important point to remember if using configuration A or D with the L drivers is that even when the L drivers are disabled, the depletion load device will source a small amount of current.

WD4210

If the WD4200 is bonded as a 24-pin device, it becomes the WD4210, illustrated in figure 1, WD4200/4210 Connection Diagrams. Note that the WD4210 does not contain the four general purpose IN inputs (IN_3 - IN_0). Use of this option precludes, of course use of the IN options, interrupt feature, and the MICROBUS™ option which uses IN_1 - IN_3 . All other options are available for the WD4210.

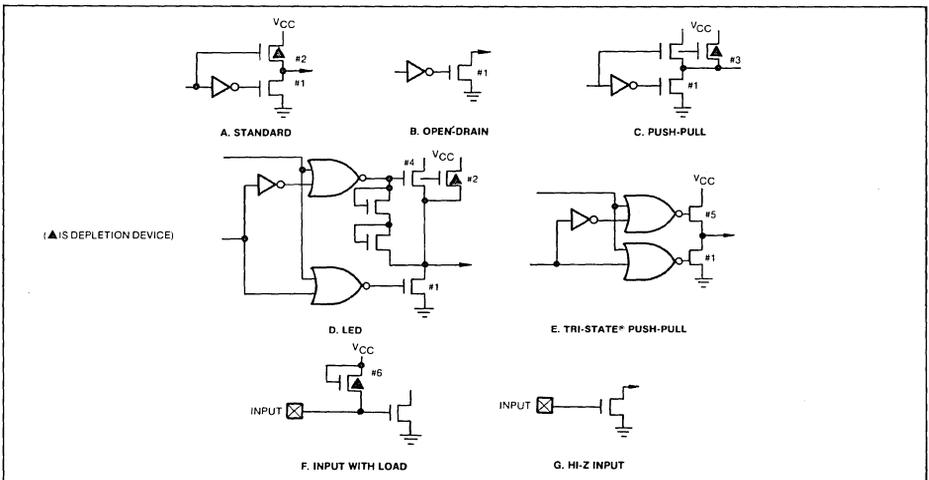


Figure 6 OUTPUT CONFIGURATIONS

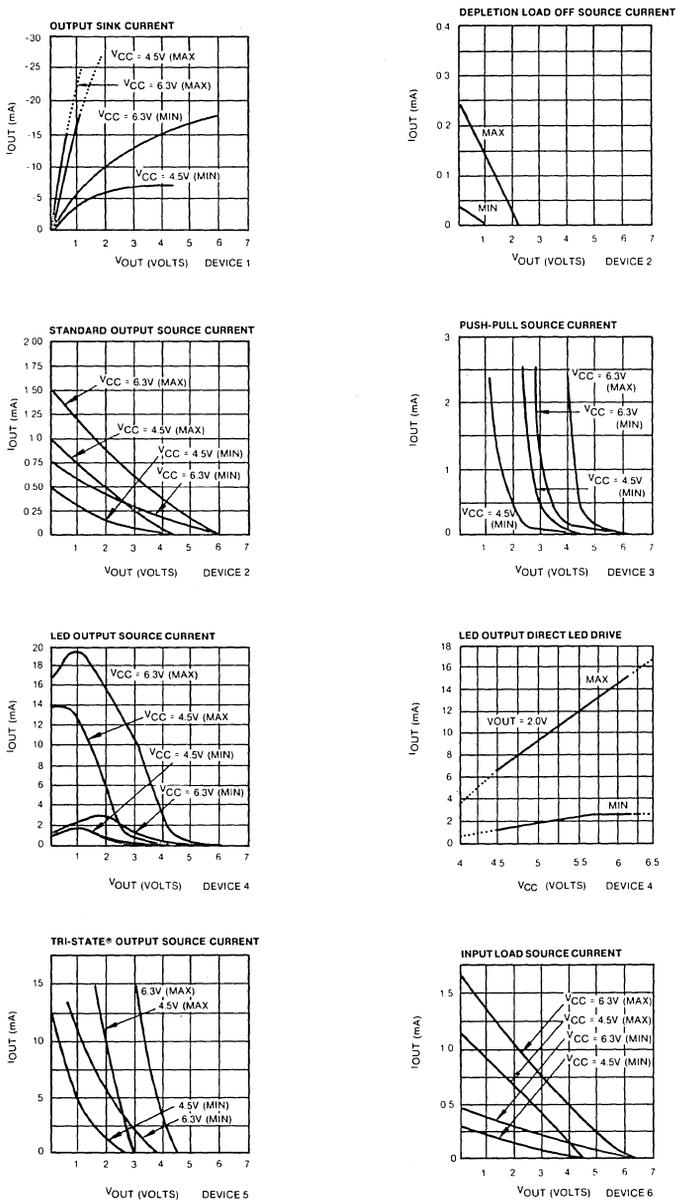


Figure 7 OUTPUT CHARACTERISTICS



WD4200/4210 INSTRUCTION SET

Table 1 is a symbol table providing internal architecture, instruction operand, and operational symbols used in the instruction set table.

Table 2 provides the mnemonic, operand, machine code, data flow, skip conditions, and description associated with each instruction in the WD4200/4210 instruction set.

TABLE 1. WD4200/4210 INSTRUCTION SET TABLE SYMBOLS

Symbol	Definition	Symbol	Definition
INTERNAL ARCHITECTURE SYMBOLS		INSTRUCTION OPERAND SYMBOLS	
A	4-bit Accumulator	d	4-bit Operand Field, 0-15 binary (RAM Digit Select)
B	6-bit RAM Address Register	r	2-bit Operand Field, 0-3 binary (RAM Register Select)
Br	Upper 2 bits of B (register address)	a	10-bit Operand Field, 0-1023 binary (ROM Address)
Bd	Lower 4 bits of B (digit address)	y	4-bit Operand Field, 0-15 binary (Immediate Data)
C	1-bit Carry Register	RAM(s)	Content and RAM location addressed by s
D	4-bit Data Output Port	ROM(t)	Content and ROM location addressed by t
EN	4-bit Enable Register	OPERATIONAL SYMBOLS	
G	4-bit Register to latch data for G I/O Port	+	Plus
IL	Two 1-bit Latches associated with the IN ₃ or IN ₀ Inputs	-	Minus
IN	4-bit Input Port	→	Replaces
L	8-bit TRI-STATE® I/O Port	↔	Is exchanged with
M	4-bit contents of RAM Memory Pointed to by B Register	=	Is equal to
PC	10-bit ROM Address Register (program counter)	\bar{A}	The ones complement of A
Q	8-bit Register to latch data for L I/O Port	⊕	Exclusive-OR
SA	10-bit Subroutine Save Register A	:	Range of values
SB	10-bit Subroutine Save Register B		
SC	10-bit Subroutine Save Register C		
SIO	4-bit Shift Register and Counter		
SK	Logic-Controlled Clock Output		

TABLE 2. WD4200/4210 INSTRUCTION SET TABLE (Note 1)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
ARITHMETIC INSTRUCTIONS						
ASC		30	0 0 1 1 0 0 0 0	A + C + RAM(B) → A Carry → C	Carry	Add with Carry, Skip on Carry
ADD		31	0 0 1 1 0 0 0 1	A + RAM(B) → A	None	Add A to RAM
ADT		4A	0 1 0 0 1 0 1 0	A + 10 ₁₀ → A	None	Add Ten to A
AISC	y	5-	0 1 0 1 y	A + y → A	Carry	Add Immediate, Skip on Carry (y ≠ 0)
CASC		10	0 0 0 1 0 0 0 0	\bar{A} + RAM(B) + C → A Carry → C	Carry	Complement and Add with Carry, Skip on Carry
CLRA		00	0 0 0 0 0 0 0 0	0 → A	None	Clear A
COMP		40	0 1 0 0 0 0 0 0	\bar{A} → A	None	Ones complement of A to A
NOP		44	0 1 0 0 0 1 0 0	None	None	No Operation
RC		32	0 0 1 1 0 0 1 0	"0" → C	None	Reset C
SC		22	0 0 1 0 0 0 1 0	"1" → C	None	Set C
XOR		02	0 0 0 0 0 0 1 0	A ⊕ RAM(B) → A	None	Exclusive-OR A with RAM

SAMSUNG

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
TRANSFER OF CONTROL INSTRUCTIONS						
JID		FF	$\boxed{1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1}$	ROM (PC9:8, A, M) → PC7:0	None	Jump Indirect (Note 3)
JMP	a	6_	$\boxed{0\ 1\ 1\ 0\ 0\ 0\ a_9\ a_8}$	a → PC	None	Jump
		--	$\boxed{a_7:0}$			
JP	a	--	$\boxed{1\ a_6:0}$	a → PC6:0	None	Jump within Page (Note 4)
			(Pages 2, 3 only) or			
		--	$\boxed{1\ 1\ a_5:0}$	a → PC5:0		
			(all other pages)			
JSRP	a	--	$\boxed{1\ 0\ a_5:0}$	PC + 1 → SA → SB → SC 0010 → PC9:6 a → PC5:0	None	Jump to Subroutine Page (Note 5)
JSR	a	6_	$\boxed{0\ 1\ 1\ 0\ 0\ 1\ 0\ a_9\ a_8}$	PC + 1 → SA → SB → SC	None	Jump to Subroutine
		--	$\boxed{a_7:0}$	a → PC		
RET		48	$\boxed{0\ 1\ 0\ 0\ 1\ 0\ 0\ 0}$	SC → SB → SA → PC	None	Return from Subroutine
RETSK		49	$\boxed{0\ 1\ 0\ 0\ 1\ 0\ 0\ 1}$	SC → SB → SA → PC	Always Skip on Return	Return from Subroutine then Skip
MEMORY REFERENCE INSTRUCTIONS						
CAMQ		33	$\boxed{0\ 0\ 1\ 1\ 1\ 0\ 0\ 1\ 1}$	A → Q7:4	None	Copy A, RAM to Q
		3C	$\boxed{0\ 0\ 1\ 1\ 1\ 1\ 1\ 0\ 0}$	RAM(B) → Q3:0		
CQMA		33	$\boxed{0\ 1\ 1\ 0\ 0\ 1\ 1\ 1\ 1}$	Q7:4 → RAM(B)	None	Copy Q to RAM, A
		2C	$\boxed{0\ 0\ 1\ 0\ 1\ 1\ 1\ 0\ 0}$	Q3:0 → A		
LD	r	_5	$\boxed{0\ 0\ r\ 0\ 1\ 0\ 1}$	RAM(B) → A BR [®] r → Br	None	Load RAM into A, Exclusive-OR Br with r
LDD	r, d	23	$\boxed{0\ 0\ 1\ 0\ 0\ 0\ 1\ 1}$	RAM(r,d) → A	None	Load A with RAM pointed to directly by r, d
		--	$\boxed{0\ 0\ r\ d}$			
LQID		BF	$\boxed{1\ 0\ 1\ 1\ 1\ 1\ 1\ 1\ 1}$	ROM(PC9:8, A, M) → Q SB → SC	None	Load Q Indirect (Note 3)
RMB	0	4C	$\boxed{0\ 1\ 0\ 0\ 1\ 1\ 0\ 0}$	0 → RAM(B) ₀	None	Reset RAM Bit
	1	45	$\boxed{0\ 1\ 0\ 0\ 0\ 1\ 0\ 1}$	0 → RAM(B) ₁		
	2	42	$\boxed{0\ 1\ 0\ 0\ 0\ 0\ 0\ 1}$	0 → RAM(B) ₂		
	3	43	$\boxed{0\ 1\ 0\ 0\ 0\ 0\ 0\ 1}$	0 → RAM(B) ₃		
SMB	0	4D	$\boxed{0\ 1\ 0\ 0\ 1\ 1\ 0\ 1}$	1 → RAM(B) ₀	None	Set RAM Bit
	1	47	$\boxed{0\ 1\ 0\ 0\ 0\ 1\ 1\ 1}$	1 → RAM(B) ₁		
	2	46	$\boxed{0\ 1\ 0\ 0\ 0\ 1\ 1\ 0}$	1 → RAM(B) ₂		
	3	4B	$\boxed{0\ 1\ 0\ 0\ 1\ 0\ 1\ 1}$	1 → RAM(B) ₃		

SECTION 4

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
MEMORY REFERENCE INSTRUCTIONS (Continued)						
STII	y	7 ₋	$\boxed{0\ 1\ 1\ 1\ \ y}$	y → RAM(B) Bd + 1 → Bd	None	Store Memory Immediate and Increment Bd
X	r	6 ₋	$\boxed{0\ 0\ \ r\ \ 0\ 1\ 1\ 0}$	RAM(B) ↔ A Br ⊕ r → Br	None	Exchange RAM with A, Exclusive OR Br with r
XAD	r, d	23 --	$\boxed{0\ 0\ 1\ 0\ \ 0\ 0\ 1\ 1}$ $\boxed{1\ 0\ \ r\ \ d}$	RAM(r, d) ↔ A	None	Exchange A with RAM pointed to directly by r, d
XDS	r	7 ₋	$\boxed{0\ 0\ \ r\ \ 0\ 1\ 1\ 1}$	RAM(B) ↔ A Bc - 1 → Bd Br ⊕ r → Br	Bd decrements past 0	Exchange RAM with A and Decrement Bd, Exclusive-OR br with r
XIS	r	4 ₋	$\boxed{0\ 0\ \ r\ \ 0\ 1\ 0\ 0}$	RAM(B) ↔ A Bd + 1 → Bd Br ⊕ r → Br	Bd increments past 15	Exchange RAM with A and Increment Bd, Exclusive-OR Br with r
REGISTER REFERENCE INSTRUCTIONS						
CAB		50	$\boxed{0\ 1\ 0\ 1\ \ 0\ 0\ 0\ 0}$	A → Bd	None	Copy A to Bd
CBA		4E	$\boxed{0\ 1\ 0\ 0\ \ 1\ 1\ 1\ 0}$	BD → A	None	Copy Bd to A
LBI	r, d	-- 33 --	$\boxed{0\ 0\ \ r\ \ (d)}$ (d = 0, 9:15) or $\boxed{0\ 0\ 1\ 1\ \ 0\ 0\ 1\ 1}$ $\boxed{1\ 0\ \ r\ \ d}$ (any d)	r, d → B	Skip until not a LBI	Load B Immediate with r, d (Note 6)
LEI	y	33 6 ₋	$\boxed{0\ 0\ 1\ 1\ \ 0\ 0\ 1\ 1}$ $\boxed{0\ 1\ 1\ 0\ \ y}$	y → EN	None	Load EN Immediate (Note 7)
XABR		12	$\boxed{0\ 0\ 0\ 1\ \ 0\ 0\ 1\ 0}$	A ↔ Br (0, 0 → A ₃ , A ₂)	None	Exchange A with Br
TEST INSTRUCTIONS						
SKC		20	$\boxed{0\ 0\ 1\ 0\ \ 0\ 0\ 0\ 0}$	1st byte 2nd byte	C = "1"	Skip if C is True
SKE		21	$\boxed{0\ 0\ 1\ 0\ \ 0\ 0\ 0\ 1}$		A = (RAM(B))	Skip if A Equals RAM
SKGZ		33	$\boxed{0\ 0\ 1\ 1\ \ 0\ 0\ 1\ 1}$		G _{3:0} = 0	Skip if G is Zero (all 4 bits)
SKGBZ		21	$\boxed{0\ 0\ 1\ 0\ \ 0\ 0\ 0\ 1}$		G ₀ = 0 G ₁ = 0 G ₂ = 0 G ₃ = 0	Skip if G Bit is Zero
		33	$\boxed{0\ 0\ 1\ 1\ \ 0\ 0\ 1\ 1}$			
	0	01	$\boxed{0\ 0\ 0\ 0\ \ 0\ 0\ 0\ 1}$			
	1	11	$\boxed{0\ 0\ 0\ 1\ \ 0\ 0\ 0\ 1}$			
SKMBZ		2	$\boxed{0\ 0\ 0\ 0\ \ 0\ 0\ 1\ 1}$		RAM(B) ₀ = 0 RAM(B) ₁ = 0 RAM(B) ₂ = 0 RAM(B) ₃ = 0	Skip if RAM Bit is Zero
		3	$\boxed{0\ 0\ 0\ 1\ \ 0\ 0\ 1\ 1}$			
	0	01	$\boxed{0\ 0\ 0\ 0\ \ 0\ 0\ 0\ 1}$			
	1	11	$\boxed{0\ 0\ 0\ 1\ \ 0\ 0\ 0\ 1}$			
SKT		2	$\boxed{0\ 0\ 0\ 0\ \ 0\ 0\ 0\ 1}$	A time-base counter carry has occurred since last test	Skip on Timer (Note 3)	
		3	$\boxed{0\ 0\ 0\ 1\ \ 0\ 0\ 0\ 1}$			
		41	$\boxed{0\ 1\ 0\ 0\ \ 0\ 0\ 0\ 1}$			

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
INPUT/OUTPUT INSTRUCTIONS						
ING		33	$[0\ 0\ 1\ 1\ 0\ 0\ 1\ 1\]$	G → A	None	Input G ports to A
		2A	$[0\ 0\ 1\ 0\ 1\ 0\ 1\ 0\]$			
ININ		33	$[0\ 0\ 1\ 1\ 0\ 0\ 1\ 1\]$	IN → A	None	Input IN inputs to A (Note 2)
		28	$[0\ 0\ 1\ 0\ 1\ 0\ 0\ 0\]$			
INIL		33	$[0\ 0\ 1\ 1\ 0\ 0\ 1\ 1\]$	IL3, CKO, "0", IL ₀ → A	None	Input IL Latches to A (Notes 2 and 3)
		29	$[0\ 0\ 1\ 0\ 1\ 0\ 0\ 1\]$			
INL		33	$[0\ 0\ 1\ 1\ 0\ 0\ 1\ 1\]$	L7:4 → RAM(B)	None	Input L Ports to RAM, A
		2E	$[0\ 0\ 1\ 0\ 1\ 1\ 1\ 0\]$	L3:0 → A		
OBD		33	$[0\ 0\ 1\ 1\ 0\ 0\ 1\ 1\]$	Bd → D	None	Output Bd to D Outputs
		3E	$[0\ 0\ 1\ 1\ 1\ 1\ 1\ 1\]$			
OGI	y	33	$[0\ 0\ 1\ 1\ 0\ 0\ 1\ 1\]$	y → G	None	Output to G Ports Immediate
		5-	$[0\ 1\ 0\ 1\ \quad y \quad]$			
OMG		33	$[0\ 1\ 1\ 0\ 0\ 1\ 1\ 1\]$	RAM(B) → G	None	Output RAM to G Ports
		3A	$[0\ 0\ 1\ 1\ 1\ 0\ 1\ 0\]$			
XAS		4F	$[0\ 1\ 0\ 0\ 1\ 1\ 1\ 1\]$	A ↔ SIO, C → SK	None	Exchange A with SIO (Note 3)

Note 1: All subscripts for alphabetical symbols indicate bit numbers unless explicitly defined (e.g., Br and Bd are explicitly defined). Bits are numbered 0 to N where 0 signifies the least significant bit (low-order, right-most bit). For example, A₃ indicates the most significant (left-most) bit of the 4-bit A register.

Note 2: The ININ and INIL instructions are not available on the 24-pin WD4210 since this device does not contain the IN inputs.

Note 3: For additional information on the operation of the XAS, JID, LQID, INIL, and SKT instructions, see below.

Note 4: The JP instruction allows a jump, while in subroutine pages 2 or 3, to any ROM location within the two-page boundary of page 2 or 3. The JP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.

Note 5: A JSRP transfers program control to subroutine page 2 (0010 is loaded into the upper 4 bits of P). A JSRP may not be used when in pages 2 or 3. JSRP may not jump to the last word in page 2.

Note 6: LBI is a single-byte instruction if d = 0, 9, 10, 11, 12, 13, 14, or 15. The machine code for the lower 4 bits equals the binary view of the "d" data minus 1, e.g., to load the lower four bits of B (Bd) with the value 9 (1001₂), the lower 4 bits of the LBI instruction equal B (1000₂). To load 0, the lower 4 bits of the LBI instruction should equal 5 (1111₂).

Note 7: Machine code for operand field y for LEI instruction should equal the binary value to be latched into EN, where a "1" or "0" in each bit of EN corresponds with the selection of deselection of a particular function associated with each bit (see Functional Description, EN Register).

The following information is provided to assist the user in understanding the operation of several unique instructions and to provide notes useful to programmers in writing WD4200/4210 programs.

XAS Instruction

XAS (Exchange A with SIO) exchanges the 4-bit contents of the accumulator with the 4-bit contents of the SIO register. The contents of SIO will contain serial-in/serial-out shift register or binary counter data, depending on the value of the EN register. An XAS instruction will also affect the SK output, providing a logic controlled clock if SIO is selected as a shift register or C → SK if SIO is selected as a bi-

nary counter. (See Functional Description, EN Register, above). If SIO is selected as a shift register, an XAS instruction must be performed once every 4 instruction cycles to effect a continuous data system.

JID Instruction

JID (Jump Indirect) is an indirect addressing instruction, transferring program control to a new ROM location pointed to indirectly by A and M. It loads the lower 8 bits of the ROM address register PC with the contents of ROM addressed by the 10-bit word, PC_{9:8}, A, M. PC₉ and PC₈ are not affected by this instruction.

Note that JID requires two instruction cycles.



INIL Instruction

INIL (Input IL Latches to A) inputs two latches, IL3 and IL0 (see figure 8) and CKO into A. The IL3 and IL0 latches are set if a low-going pulse ("1" to "0") has occurred on the IN3 and IN0 inputs since the last INIL instruction, provided the input pulse stays low for at least two instruction times. Execution of an INIL inputs IL3 and IL0 into A3 and A0 respectively, and resets these latches to allow them to respond to subsequent low-going pulses on the IN3 and IN0 lines. If CKO is mask programmed as a general purpose input, an INIL will input the state of CKO into A2. If CKO has not been so programmed, a "1" will be placed in A2. A "0" is always placed in A1 upon the execution of an INIL. The general purpose inputs IN3—IN0 are input to A upon the execution of an ININ instruction (see table 2, ININ Instruction). INIL is useful in recognizing pulses of short duration or pulses which occur too often to be read conveniently by an ININ instruction.

LQID Instruction

LQID (Load Q Indirect) loads the 8-bit Q register with the contents of ROM pointed to by the 10-bit word PC9, PC8, A, M. LQID can be used for table look-up or code conversion such as BCD to seven-segment. The LQID instruction "pushes" the stack (PC + 1 → SA → SB → SC) and replaces the least significant 8 bits of PC as follows: A → PC7:4, RAM(B) → PC3:0, leaving PC9 and PC8 unchanged. The ROM data pointed to by the new address is fetched and loaded into the Q latches. Next, the stack is "popped" (SC → SB → SA → PC), restoring the saved value of PC to continue sequential program execution. Since LQID pushes SB → SC, the previous contents of SC are lost. Also, when LQID pops the stack, the previously pushed contents of SB are left in SC. The net result is that the contents of SB are placed in SC (SB → SC). Note that LQID takes two instruction cycle times to execute.

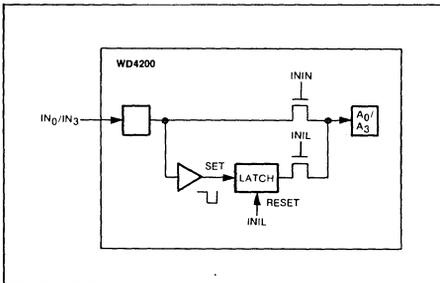


Figure 8 INIL HARDWARE IMPLEMENTATION

SKT Instruction

The SKT (Skip on Timer) instruction tests the state of an internal 10-bit time-base counter. This counter divides the instruction cycle clock frequency by 1024 and provides a latched indication of counter overflow. The SKT instruction tests this latch, executing the next program instruction if the latch is not set. If the latch has been set since the previous test, the next program instruction is skipped and the latch is reset. The features associated with this instruction, therefore, allow the WD4200/4210 to generate its own time-base for real-time processing rather than relying on an external input signal.

For example, using a 2.097 MHz crystal as the time-base to the clock generator, the instruction cycle clock frequency will be 131 kHz (crystal frequency ÷ 16) and the binary counter output pulse frequency will be 128 Hz. For time-of-day or similar real-time processing, the SKT instruction can call a routine which increments a "seconds" counter every 128 ticks.

Instruction Set Notes

- The first word of a WD4200/4210 program (ROM address 0) must be a CLRA (Clear A) instruction.
- Although skipped instructions are not executed, one instruction cycle time is devoted to skipping each byte of the skipped instruction. Thus all program paths take the same number of cycle times whether instructions are skipped or executed.
- The ROM is organized into 16 pages of 64 words each. The Program Counter is a 10-bit binary counter, and will count through page boundaries. If a JP, JSRP, JID, or LQID instruction is located in the last word of a page, the instruction operates as if it were in the next page. For example: a JP location in the last word of a page will jump to a location in the next page. Also, a LQID or JID located in the last word of pages 2, 7, 11, or 15 will access data in the next group of four pages.

OPTION LIST

The WD4200/4210 mask-programmable options are assigned numbers which correspond with the WD4200 pins.

TABLE 3 is a list of WD4200 options. When specifying a WD4210 chip, Options 9, 10, 19, 20, and 29 must all be set to zero. The options are programmed at the same time as the ROM pattern to provide the user with the hardware flexibility to interface to various I/O components using little or no external circuitry.

TABLE 3 WD4200 MASK OPTIONS

Option 1 = 0: Ground Pin — no options available	Option 15: L ₀ Driver Same as Option 5
Option 2: CKO Pin = 0: clock generator output to crystal = 1: pin is RAM power supply (V _R input) = 2: general purpose input, load device to V _{CC} = 3: multi-COP SYNC input = 4: general purpose input, Hi-Z input	Option 16: SI Input Same as Option 9
Option 3: CKI Input = 0: crystal input divided by 16 = 1: crystal input divided by 8 = 2: TTL external clock input divided by 16 = 3: TTL external clock input divided by 8 = 4: single-pin RC controlled oscillator	Option 17: SO Driver = 0: Standard output (Figure 6A) = 1: Open-Drain output (Figure 6B) = 2: Push-Pull output (Figure 6C)
Option 4: $\overline{\text{RESET}}$ Pin = 0: load devices to V _{CC} = 1: Hi-Z input	Option 18: SK Driver Same as Option 17
Option 5: L ₇ Driver = 0: Standard output (Figure 6A) = 1: Open-Drain output (Figure 6B) = 2: LED direct drive output (Figure 6D) = 3: TRI-STATE® push-pull output (Figure 6E)	Option 19: IN ₀ Input Same as Option 9
Option 6: L ₆ Driver Same as Option 5	Option 20: IN ₃ Input Same as Option 9
Option 7: L ₅ Driver Same as Option 5	Option 21: G ₀ I/O Port = 0: Standard output (A) = 1: Open-Drain output (B)
Option 8: L ₄ Driver Same as Option 5	Option 22: G ₁ I/O Port Same as Option 21
Option 9: IN ₁ Input = 0: load device to V _{CC} (Figure 6F) = 1: Hi-Z input	Option 23: G ₂ I/O Port Same as Option 21
Option 10: IN ₂ Input Same as Option 9	Option 24: G ₃ I/O Port Same as Option 21
Option 11 = 0: V _{CC} Pin — no options available	Option 25: D ₃ Output = 0: Standard output (A) = 1: Open-Drain output (B)
Option 12: L ₃ Driver Same as Option 5	Option 26: D ₂ Output Same as Option 25
Option 13: L ₂ Driver Same as Option 5	Option 27: D ₁ Output Same as Option 25
Option 14: L ₁ Driver Same as Option 5	Option 28: D ₀ Output Same as Option 25
	Option 29: COP Function = 0: normal operation = 1: MICROBUS™ option
	Option 30: COP Bonding = 0: WD4200 (28-pin device) = 1: WD4210 (24-pin device)

TEST MODE (Non-Standard Operation)

The SO output has been configured to provide for standard test procedures for the custom-programmed WD4200. With SO forced to logic "1", two test modes are provided, depending upon the value of SI:

- a. RAM and Internal Logic Test Mode (SI = 1)
- b. ROM Test Mode (SI = 0)

These special test modes should not be employed by the user; they are intended for manufacturing test only.



APPLICATION NO. 1: WD4200 General Controller

The diagram below shows an interconnect diagram for a WD4200 used as a general controller. Operation of the system is as follows:

1. The L7-L0 outputs are configured as LED Direct Drive outputs, allowing direct connection to the segments of the display.
2. The D3-D0 outputs are buffered by transistors to drive the digits of the multiplexed display and to scan the columns of the 4x4 keyboard matrix rows.
3. The IN3-IN0 inputs are used to input the four drives of the keyboard matrix. Reading the IN lines in conjunction with the current value of the D outputs allows detection, debouncing, and decoding of any one of the 16 keyswitches.
4. CKI is configured as a single-pin oscillator input allowing system timing to be controlled by a single pin RC network. CKO is therefore available for use as a VR RAM power supply pin. RAM data integrity is thereby assured when the main power supply is shut down.
5. SI is selected as the input to a binary counter input. With SIO used as a binary counter, SO and SK may be used as general purpose outputs.
6. The four bidirectional G I/O ports (G3-G0) are available for use as required by the user's application.

APPLICATION NO. 2

Provides an interconnect diagram for a versatile application of the WD4200 as a keyboard/display interface to a microprocessor (μP). Generally, operation of the WD4200 in this configuration is as follows:

1. The MICROBUS™ option has been selected.
2. System timing is provided by an external crystal. The time base for the real-time (counter and clock) modes is provided by the internal time-base counter, tested by the SKT instruction.
3. The SIO register is used as a serial-in/serial-out shift register. In this configuration, however, SI is shifted into SIO to be tested as one of the four row lines tied to the keyboard matrix. SO is used to output display segment data (loaded into SIO with an XAS instruction) to the cascaded 74C164s (8-bit parallel out serial shift registers). SK functions as a logic-controlled clock, sending a SYNC signal to clock serial data into the 74C164s.
4. The 16 bits of data shifted into the 74C164s are buffered through the DS8867s (8-segment LED drivers) to the 16 segments of the alphanumeric LED displays.
5. The D0-D1 outputs are decoded by the DS8664 (14-digit decoder/driver) and used to select one of the 14 digits of the multiplexed display as well as to scan the 13 columns of the keyboard matrix and the strap switch scan line (D14).

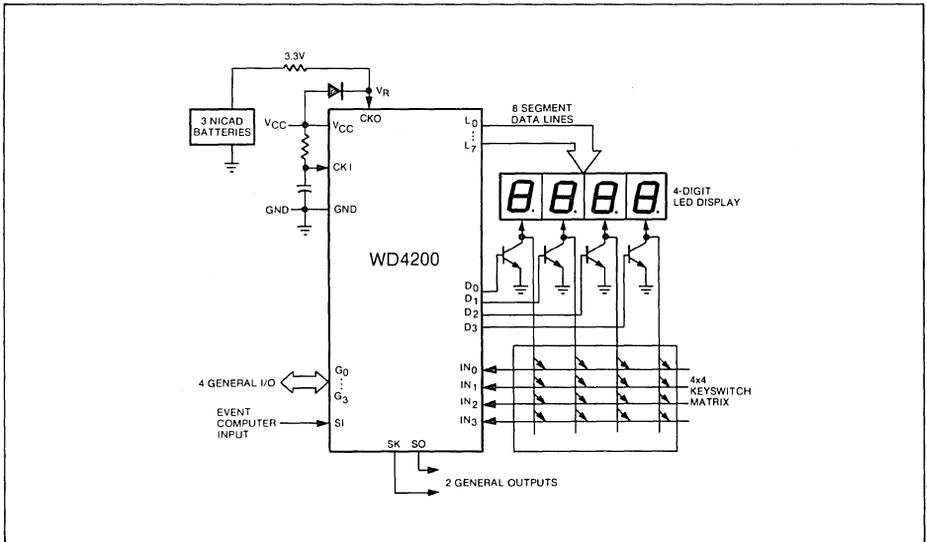


Figure 9 WD4200 KEYBOARD/DISPLAY INTERFACE

6. The G₁-G lines together with SI are connected to the four rows of the keyboard matrix and the four strap switch lines to input key or strap switch data to the WD4200.
7. The L₀-L₇ TRI-STATE® bidirectional I/O ports are connected to the microprocessor data bus to allow for input or output of data to and from the microprocessor and the WD4200.
8. The various operations which can be performed by the system include the following "handshaking" and WD4200 "stand-alone" modes:
 - a. keyboard to μP (7-bit ASCII)
 - b. keyboard to WD4200 buffer to μP (7-bit ASCII)
 - c. μP to display
 - d. display to μP
 - e. μP to clock
 - f. clock to μP
 - g. μP to timer
 - h. timer to μP
 - i. keyboard to display
 - j. clock to display
 - k. timer to display

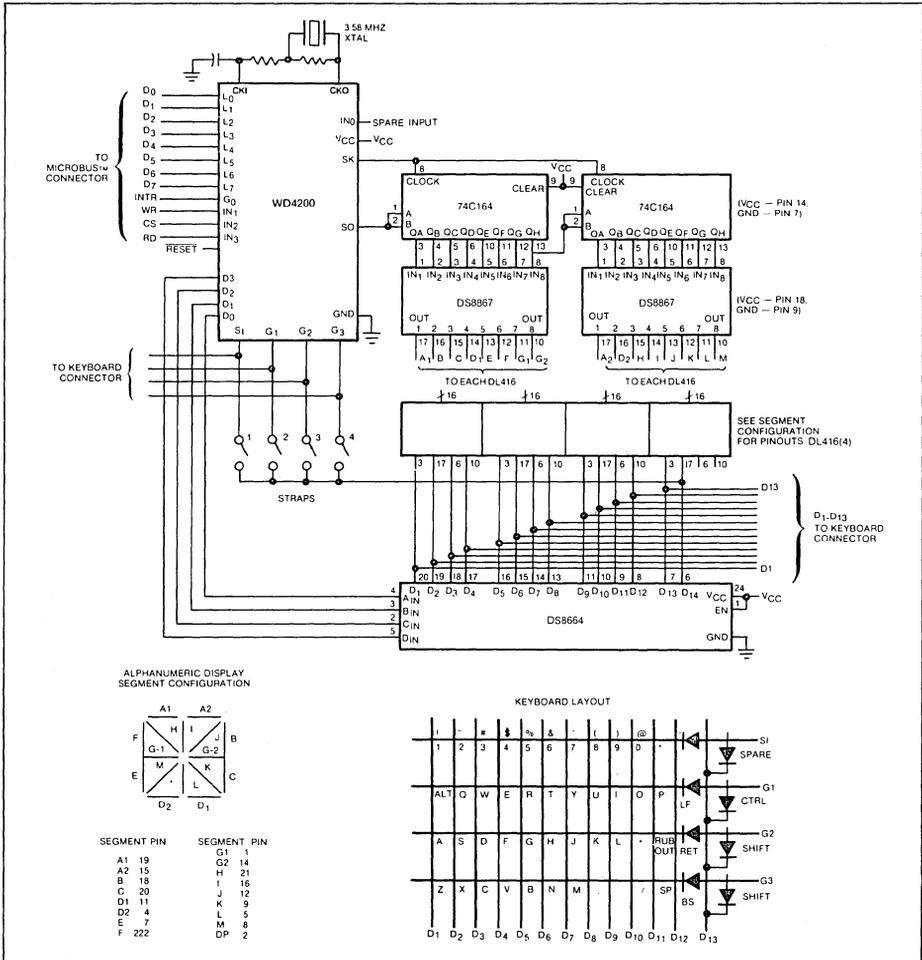


Figure 10 WD4200 KEYBOARD/DISPLAY INTERFACE

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin Relative to GND -0.5V to +7V
Ambient Operating Temperature (Note 1)

0°C to +70°C

Ambient Storage Temperature -65°C to +150°C

Lead Temperature (Soldering, 10 sec.) 300°C

Power Dissipation 0.75 Watt at 25°C

0.4 Watt at 70°C

TABLE 4

DC ELECTRICAL CHARACTERISTICS

0°C ≤ TA ≤ +70°C, 4.5V ≤ VCC ≤ 6.3V unless otherwise noted.

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

PARAMETER	CONDITIONS	MIN	MAX	UNITS
Operating Voltage (VCC)		4.5	6.3	V
Operating Supply Current	VCC = 5V, TA = 25°C (all inputs and outputs open)		30	mA
Input Voltage Levels				
CKI Input Levels				
Crystal Input				
Logic High (VIH)		2.0		V
Logic Low (VIL)			0.4	V
TTL Input	VCC = 5V ± 5%			
Logic High (VIH)		2.0		V
Logic Low (VIL)			0.8	V
Schmitt Trigger Input				
Logic High (VIH)		0.7 VCC		V
Logic Low (VIL)			0.6	V
RESET Input Levels				
Logic High		0.7 VCC		V
Logic Low			0.6	V
RESET Hysteresis		1.0		V
SO Input Level (Test Mode)		2.0	3.0	V
All Other Inputs				
Logic High	VCC = Max	3.0		V
Logic High	VCC = 5V ± 5%	2.0		V
Logic Low			0.8	V
Output Voltage Levels				
Standard Output				
TTL Operation	VCC = 5V ± 5%			
Logic High (VOH)	IOH = 100 μA	2.4		V
Logic Low (VOL)	IOL = -1.6 mA		0.4	V
CMOS Operation				
Logic High (VOH)	IOH = 10 μA	VCC-1		V
Logic Low (VOL)	IOL = -10 μA		0.2	V
Output Current Levels				
LED Direct Drive Output				
Logic High (IOH)	VCC = 6V VOH = 2.0V	2.5	14	mA
TRI-STATE® Output		-10	+10	μA
Leakage Current				
CKO Output				
VR Power Saving Option	VR = 3.3V			
Power Requirements			3	mA

TABLE 5

AC Electrical Characteristics

0°C ≤ TA ≤ +70°C, 4.5V ≤ VCC ≤ 6.3V unless otherwise stated.

PARAMETER	CONDITIONS	MIN	MAX	UNITS
Instruction Cycle Time — tC	figure 13a	4	10	μs
CKI Using Crystal (figure 5A)				
Input Frequency — f1	÷16 mode	1.6	4	MHz
	÷ 8 mode	0.8	2	MHz
Duty Cycle (Note 2)	figure 13b	30	55	%
CKI Using External Clock (figure 5B)				
Input Frequency	÷16 mode	1.6	4	MHz
	÷ 8 mode	0.8	2	MHz
Duty Cycle (Note 2)		30	60	%
Rise Time	f1 = 4 MHz		60	ns
Fall Time	f1 = 4 MHz		40	ns
CKI Using RC (figure 5C)				
Frequency	R = 15K ± 5%, C = 100 pF ± 10%	0.5	1.0	MHz
Instruction Cycle Time		4	8	μs
CKO as SYNC Input (figure 5D)				
tSYNO	figure 13b	50		ns
Inputs (figure 13a):				
IN3-IN0, G3-G0, L7-L0				
tSETUP		1.7		μs
tHOLD		100		ns
SI				
tSETUP		0.3		μs
tHOLD		100		ns
Outputs:				
COP to CMOS Propagation Delay	4.5V ≤ VCC ≤ 6.3V, CL = 50 pF, VOH = 0.7 VCC, VOL = 0.3 VCC			
SK as a Logic-Controlled Clock			1.1	μs
tPD1			0.3	μs
tPD0				
S0, SK as a Data Output			1.4	μs
tPD1			0.3	μs
tPD0			0.7	μs
	VOH = 2V			
D3-D0, G3-G0			1.6	μs
tPD1			0.6	μs
tPD0				
L7-L0 (Standard)			1.4	μs
tPD1			0.3	μs
tPD0				
L7-L0 (LED Direct Drive)			2.4	μs
tPD1	VOH = 2V		0.4	μs
tPD0				
COP to TTL Propagation Delay	fanout = 1 Standard TTL Load VCC = 5V ± 5%, CL = 50 pF, VOH = 2.4V, VOL = 0.4V			
SK as a Logic-Controlled Clock			0.8	μs
tPD1			0.8	μs
tPD0				
SK as a Data Output, S0			1.0	μs
tPD1			1.0	μs
tPD0				

SECTION 4

PARAMETER	CONDITIONS	MIN	MAX	UNITS
Outputs (continued):				
D3-D0, G3-G0				
t _{PD1}			1.3	μs
t _{PD0}			1.3	μs
L7-L0				
t _{PD1}			1.4	μs
t _{PD0}			0.4	μs
L7-L0 (Push-Pull)				
t _{PD1}			0.4	μs
t _{PD0}			0.3	μs
CKO (figure 13C)				
t _{PD1}			0.2	μs
t _{PD0}			0.2	μs
MICROBUS™ Timing		CL = 50 pF, V _{CC} = 5V ± 5%		
Read Operation (figure 11)				
Chip Select Stable Before \overline{RD} - t _{CSR}		50		ns
Chip Select Hold Time for \overline{RD} - t _{RCS}		5		ns
\overline{RD} Pulse Width - t _{RR}		300		ns
Data Delay from \overline{RD} - t _{RD}			250	ns
\overline{RD} to Data Floating - t _{DF}			200	ns
Write Operation (figure 12)				
Chip Select Stable Before \overline{WR} - t _{CSW}		20		ns
Chip Select Hold Time for \overline{WR} - t _{WCS}		20		ns
\overline{WR} Pulse Width - t _{WW}		300		ns
Data Set-Up Time for \overline{WR} - t _{DW}		200		ns
Data Hold Time for \overline{WR} - t _{WD}		40		ns
INTR Transition Time from \overline{WR} - t _{WI}			700	ns

Note 1: An extended temperature range WD4200/4210 is available which will operate within an ambient temperature range of -40°C to +85°C.

Note 2: Duty Cycle = $t_{W1} / (t_{W1} + t_{W0})$.

Note 3: See figure 7 for additional I/O characteristics.

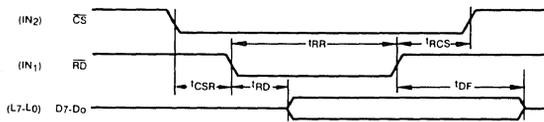


Figure 11 MICROBUS™ READ OPERATION TIMING

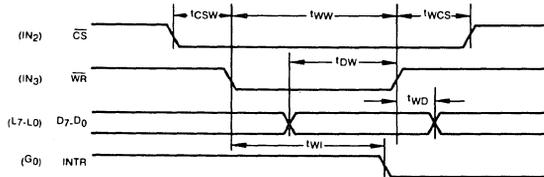


Figure 12 MICROBUS™ WRITE OPERATION TIMING

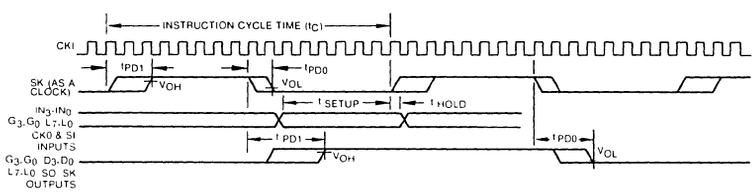


Figure 13A INPUT/OUTPUT TIMING DIAGRAM (CRYSTAL + 16 MODE)

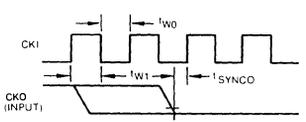


Figure 13B SYNCHRONIZATION

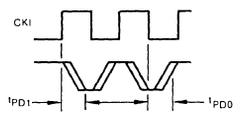
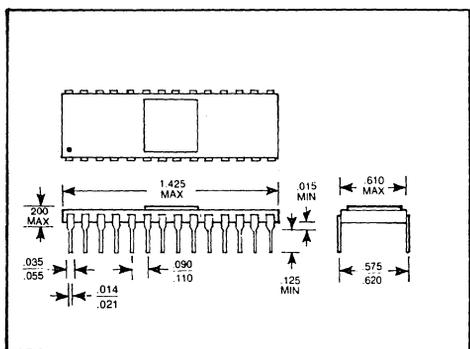
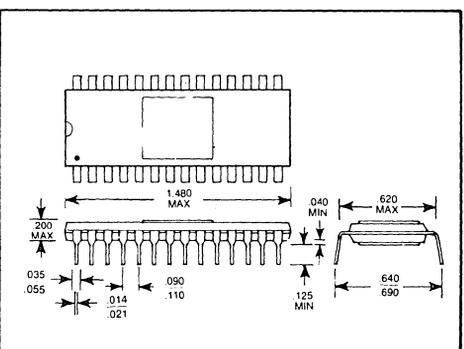


Figure 13C CKO OUTPUT TIMING

Figure 13 TIMING



WD4200E CERAMIC PACKAGE



WD4200F PLASTIC PACKAGE

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GENERAL INFORMATION

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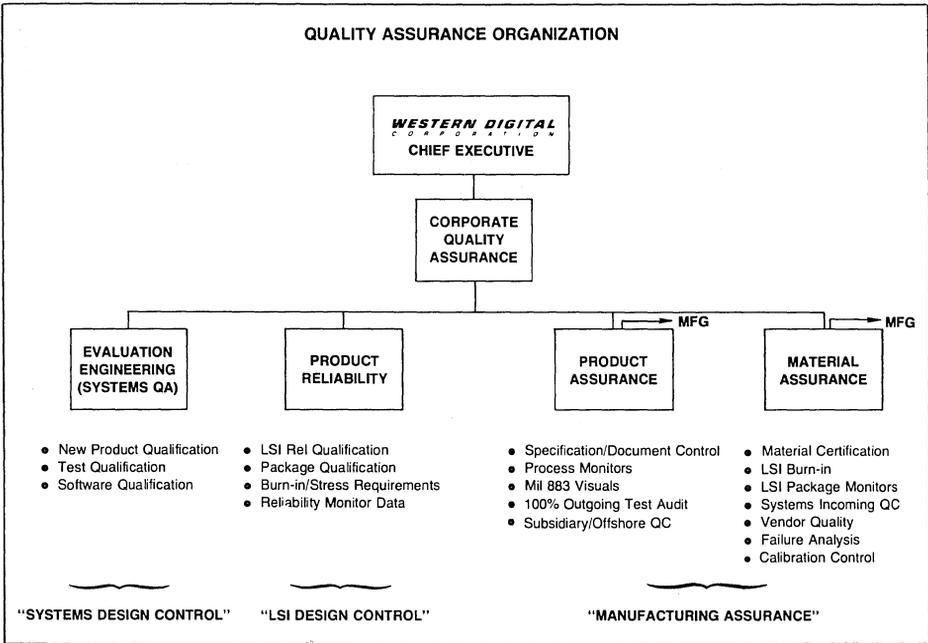
CORPORATE QUALITY ASSURANCE

It is the policy of *Western Digital Corporation* that every employee be committed to quality excellence in producing products/processes which conform to acceptable requirements.

The total quality program is managed and monitored by the quality assurance organization. Quality assurance is chartered to review marketing product requirements, qualify hard-

ware and software designs, certify manufacturing operations and monitor performance/control conformance to product specifications.

Primary responsibility for execution of the quality program rests with functional organizations to design, produce, and market high quality and high reliability products specified to our customers.



QUALITY ASSURANCE PROGRAM HIGHLIGHTS

- All process chemicals used in the Mask/Wafer fabrication operations are monitored by the process control section of QA.
- Document control is an integral part of quality assurance. All specifications are issued and controlled by this activity.
- All Western Digital devices are 100% tested by manufacturing and, in addition, must pass a 1.0% AQL sample test performed by QA.
- All devices are tested on either state-of-the-art MOS/LSI Spartan test systems designed and built by Western Digital or on industry standard test systems such as Megatest or Fairchild.
- Receiving inspection maintains a very thorough check of incoming material and has developed unique "use/stress tests" (look ahead sample build acceptance) which critical material must pass before acceptance by Western Digital.
- The Quality Assurance Department continuously monitors the manufacturing operations and issues weekly process control reports displaying detailed data and trends for the associated areas.
- *The Western Digital Malaysian assembly operation uses*

the same specifications as the Newport Beach operation. All specifications are controlled at Newport Beach.

- All new devices and proposed process changes must pass a thorough reliability qualification before incorporation into production.
- The Western Digital HI-REL "K" program is designed to provide high reliability comparable to the requirements of MIL-STD-883B, Method 5004-4, Class B.

OUTGOING QUALITY/RELIABILITY

This brochure should answer questions brought up by various W.D.C. customers throughout the years. In the following pages we have outlined the quality conformance and qualification tests that all devices must meet prior to delivery to our customers.

PRODUCT STABILIZATION

W.D.C. subjects all products to 100% stabilization bake and temperature cycling prior to final testing. The adherence to a single high quality level device, reduces the field maintenance problems frequently found by *many customers*. Device Designs have built in static protection on all devices.

QUALIFICATION AND QUALITY CONFORMANCE INSPECTION

Table I. GROUP A 100% OUTGOING ELECTRICAL AUDIT

Subgroups	AQL
Subgroup 1 — Final Electrical Test @ 25°C	1.0 AQL
Subgroup 2 — Final Electrical Test @ 70°C	1.0 AQL

Refer to the specific device data sheet specifications for min./max. parameters, definition and limits.

Table II. GROUP B REL QUALIFICATION MONITOR

Test	Method	Conditions	LTPD
Subgroup 1 Physical dimensions	2016		15
Subgroup 2			
a. Resistance to solvents	2015		3 devices (no failures)
b. Internal Visual and Mechanical	2014		1 device (no failures)
c. Bond Strength—Aluminum Wire— Ultrasonic	2011	Test Condition D	
Subgroup 3 Solderability	2033	Soldering Temp of 260°C ± 10°C. 95% coverage, void concentration not to exceed 5% of area.	15
Subgroup 4			
a. Lead Fatigue	2004	Test condition B ₂ : 8 oz., #1 direction. 3 bends, 90° each.	15
b. Gross Leak	—	Flouorocarbon detection 10 ⁻³ atm/cc/sec.	
Subgroup 5			
a. Steady State Life Test	1005	HTRB, temperature—125°C, 1,000 hrs.	5
b. Electrical Parameters	—	Final electrical @ 25°C	

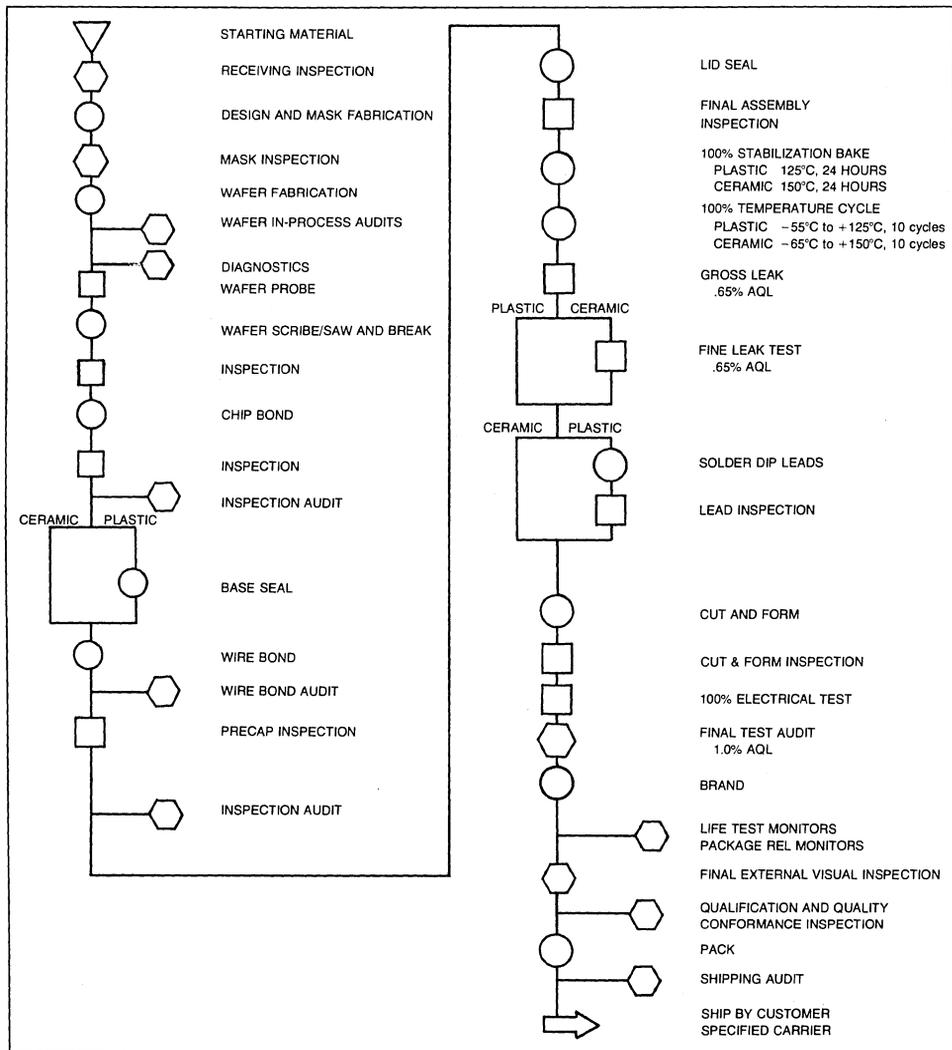
Table III. Group C Tests

Test	Method	Conditions	LTPD
group 1			
Thermal Shock	1011	Test method B: Liquid to liquid, 125°C to -55°C to 125°C, 15 cycles	15
Temperature cycling	1010	Test condition B: air to air -55°C to 125°C, 100 cycles	
Moisture resistance	1004	Omit initial conditioning	
Gross Leak	—	Fluorocarbon detection 10 ⁻³ atm/cc/sec	
Electrical parameters	—	Final electrical @ 25°C	
group 2			
Mechanical shock	2002	Test condition B: 5 shock pulses, 6 orientation directions; 1,500 F	15
Vibration variable frequency	2007	Test condition A: 20 Hz-2 KHz; 20G, X, Y, Z orientation	
Constant acceleration (Centrifuge)	2001	Test condition E: 30 KG centrifugal acceleration	
Gross Leak	—	Fluorocarbon detection 10 ⁻³ atm/cc/sec	
Electrical parameters	—	Final electrical @ 25°C	
group 3			
Salt atmosphere (Corrosion)	1009	Test condition A: 24 hrs	15
Gross Leak	—	Fluorocarbon detection 10 ⁻³ atm/cc/sec	
Visual examination	—	Per visual criteria of method 1009	
group 4			
High temperature storage	1008	Test condition B: 125°C storage, 1,000 hours	15
Gross Leak	—	Fluorocarbon detection 10 ⁻³ atm/cc/sec	
Electrical parameters	—	Final electrical @ 25°C	

Groups A, B, and C sampling plans are based on standard LTPD tables of MIL-M-38510.

Product/Process Assurance

... Quality audits and gates are located throughout the manufacturing process in order to assure a stable process and thus, a quality product to our customers. The following manufacturing/screening/inspection flow diagram identifies the steps as they relate to the production of Western Digital plastic and ceramic MOS/LSI packages.



RELPAK PLASTIC PACKAGE SPECIFICATION

FEATURES

- COST ADVANTAGES OF TOTAL ENCAPSULATED PACKAGES.
- RELIABILITY ADVANTAGES OF A CERAMIC PACKAGE.
- SUPERIOR MECHANICAL QUALITIES
- OUTSTANDING ELECTRICAL CHARACTERISTICS.
- CONSTRUCTION MATERIALS ELIMINATE SOURCES OF RUST AND CORROSION.
- ELIMINATES HOT INTERMITTANT OPEN PROBLEMS.
- ELIMINATES DEVICE INSTABILITY DUE TO IONIC CONTAMINATION.
- MOISTURE PENETRATION DRAMATICALLY REDUCED.

AVAILABILITY

WDC has been supplying satisfied customers for over nine years with this package. Because this package was developed in-house, we have a completely self-sustained production line with very little dependence on suppliers. The package was developed alongside the ceramic package, which means equipment interchangeability on the assembly line. This production versatility has enabled WDC customers to benefit from quick turn around times.

We patented this package in 1973 and, because of its similarities to the ceramic packages, WDC has the unique distinction of possessing the only industry available plastic E-Prom package. With slight material changes, WDC can assemble 24 lead E-Prom devices in the Standard RELPAK Packages for customer evaluation and use.

RELIABILITY AT LOW COST

Western Digital Corporation's RELPAK Plastic Package is unique to the industry in that it contains many of the cost advantages of the industry accepted total encapsulated package while it also contains many of the reliability advantages of a ceramic package.

CONSTRUCTION DETAILS

The RELPAK is a cavity approach which allows the use of aluminum wire for cost purposes, while the plastic will never come in contact with the active circuit and wires. This eliminates the Hot Intermittant Open HIO problems associated with industry standard plastic packages and also eliminates device instability due to ionic contamination caused by plastic being in direct contact with the device.

The die is attached to its metal base separately from the

plastic package body. This allows for a true AuSi Eutectic die attachment prior to the marriage with the plastic body. This process design again eliminated the chance for ionic contamination upon the active circuit areas.

The package structure is such that 95% of the internal surface area is composed of metal. The possible paths for moisture penetration are confined to the parameters of the cavity, thereby increasing the mean distance of moisture paths to its maximum.

This package is constructed using a proprietary copper lead frame material, which eliminates sources of rust or corrosion. Our proprietary molding process allows WDC to mold without the lead frame bonding surface ever making contact with the molding material, again eliminating possible sources for ionic contamination.

We use an Ortho Creasol Novolac Epoxy resin and a Phenolic Novolac curing agent as the base transfer molding compound. Together with our proprietary lead frame material we have achieved a true chemical mechanical bond during the molding process. This bond is so strong, we are able to place a device prior to lid seal upside down on a helium leak detector and pass a 1×10^{-8} std cc/sec open face leak test.

Using standard stress acceleration factors, the projected life expectancy of the WDC RELPAK Package is well in excess of 100 years.

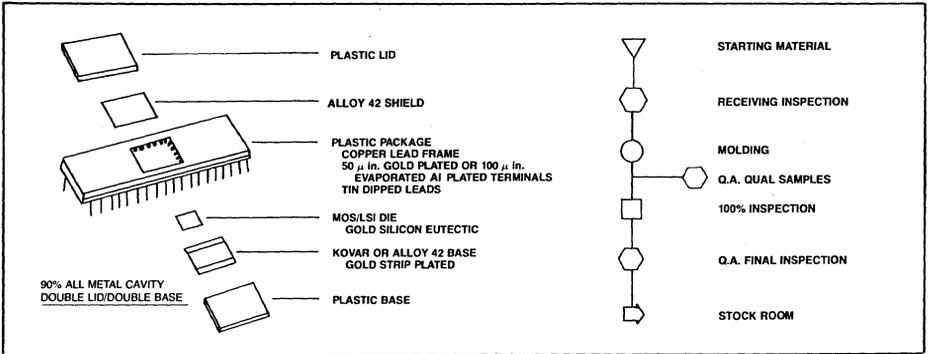
The basic RELPAK design employs a "see thru" construction. The lead frames are stamped from 10 mil thick sheets of copper into strips of four, which are then spot Ni spot Au plated. The quality levels of the lead frames and molding powders are rigorously controlled by incoming Q.C. The lead frames and molding powders are controlled by lot numbers. Each incoming lot is individually increased by W.D.C. material assurance.

ADVANTAGES OF THE RELPAK

The most obvious is its lower cost compared to its ceramic counterpart without any reduction in reliability—by retaining the premolded cavity package concept, essentially all the problems of a total encapsulated package are avoided such as work damage to the bonding wires during the molding operation, concern for adverse effects from direct contact of the molding epoxy with the die surface, and the hot intermittent open reliability problem. The use of a solid metal lead frame coupled with the gold plated Kovar (or Alloy 42) base to which the die is eutectically attached provide more than adequate thermal paths for power dissipation, a primary reliability consideration.

Careful adherence to sound engineering design practices during package development coupled with the use of a metallurgical bond at chip bond and conventional aluminum wire bonding has resulted in a plastic cavity package which can be subjected to the same product assurance screening operations as its ceramic counterparts without adversely affecting the package or device parameters.

... The Western Digital plastic "cavity" package is a unique package offering most of the advantages of ceramic. The quality assurance and reliability department maintains a thorough inspection program during production of the plastic packages. An overview of the plastic package (RELPAK) program is illustrated below.



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C O R P O R A T I O N

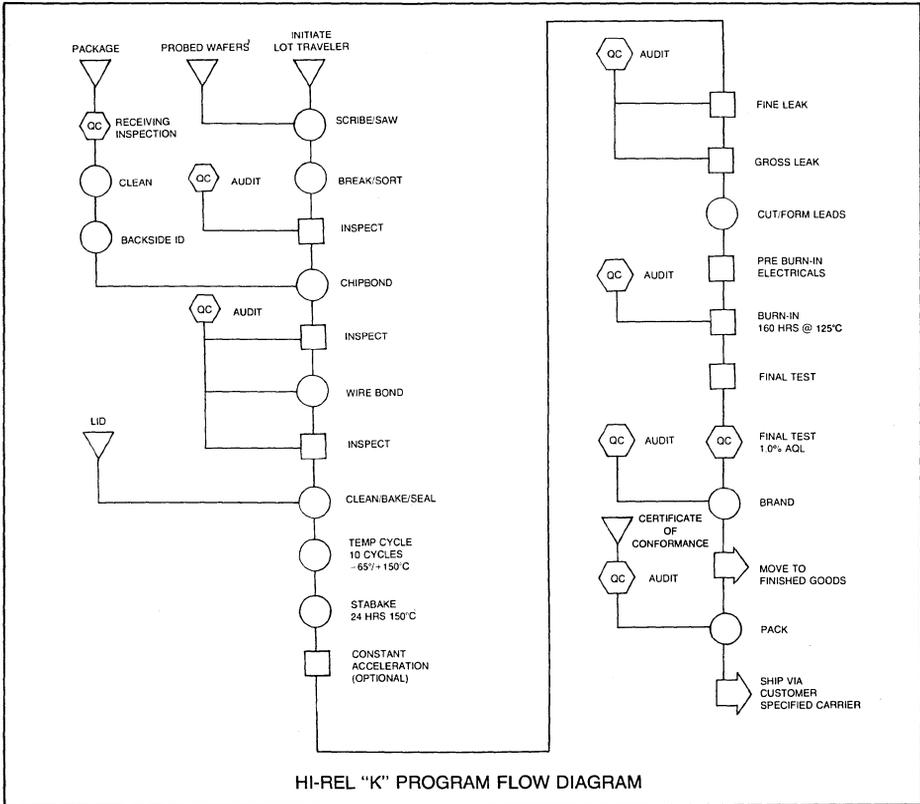
HI-REL "K" TESTING PROGRAM

FEATURES

- GENERAL CONFORMANCE TO MIL-STD-883B, METHOD 5004.4, CLASS B
- INCLUDES:
 - PRECAP VISUALS
 - SEAL INTEGRITY
 - POWER CONDITIONING
 - ENHANCEMENT OPTIONS

GENERAL DESCRIPTION

Western Digital's Hi-Rel "K" program is designed to provide high reliability devices for extended temperature environments. Individual enhancements may be selected to meet your particular environmental needs.



HI-REL "K" PROGRAM FLOW DIAGRAM

51011-02
5

3.1.1 Internal Visual

Method 2010.3
Test condition B

All Hi-Rel "K" devices receive 100% inspections prior to lid seal. These inspections together comprise criteria comparable to Mil-Std-883, method 2010.3, test condition B.

3.1.2 Stabilization Bake

Method 1008.1
Test condition C
24 hours at 150°C

Same

3.1.3 Temperature Cycling

Method 1010.2, Test condition C
-65°C to 150°C for 10 cycles, with 10 minutes dwell,
and 5 minutes maximum transfer time

Same

3.1.4 Constant Acceleration

Method 2001.2, Test condition E. 30,000 G stress
level

Optional

3.1.5 Visual Inspection

Visual inspection for catastrophic failures after screens

Same

3.1.6 Seal Method 1014.2

- (a) Helium fine leak — Test condition A₁. Bomb condition 2 hours at 60 psig. Reject limit 5×10^{-8} torr
- (b) Fluorocarbon gross leak — Test condition C

Same

Same

3.1.9 Interim (pre-burn-in) Electricals

Per applicable device specification

Preburn-in at 25°C. Must meet requirements of device data sheets.

3.1.10 Burn-in Test

Method 1015.2, 160 hours @ 125°C

Same

3.1.13 Interim (Post burn-in) electricals

Per applicable device specification

Final Test

3.1.15 Final Electrical Test

(a) Static Tests

Same

(1) 25°C

(2) Minimum and Maximum Operating
Temperatures

(b) Dynamic and Switching Tests at 25°C

(c) Functional Tests at 25°C

**3.1.17 Qualification or Quality Conformance
Inspection and Test Sample Selection**

To be agreed upon

3.1.18 External Visual

Method 2009.2

Same

WESTERN DIGITAL RELIABILITY ENHANCEMENT OPTIONS

100% Temperature Testing

Level —40° to +85°C
—55° to +125°C

Thermal, Shock (Liquid to Liquid)

Level 0° to +100°C, 15 cycles
—55° to +125°C
—65° to +150°C

Extended High Temperature Storage

+150°C for 24 hours standard, other time/temperature storage requirements available as required.

Abbreviations and acronyms

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A/D	Analog/digital	BSC	Binary synchronous communications
ACCT	Ad Hoc Committee for Competitive Telecommunications	BTAM	Basic telecommunications access method (IBM)
ACF	Advanced communications function	BTU	Basic transmission unit
ACK	Acknowledgement, positive	CATV	Community antenna television
ACM	Association for Computing Machinery	CAI	Computer assisted instruction
ACU	Automatic calling unit	CBEMA	Computer Business Equipment Manufacturers Association
ADCCP	Advanced data communications control procedure	CBT	Computer-based terminal
ADP	Automatic data processing	CBX	Computerized private branch exchange
AFIPS	American Federation of Information Processing Societies	CCB	Common Carrier Bureau
ALU	Arithmetic logic unit	CCDN	Corporate consolidated data network (IBM)
ANSI	American National Standards Institute	CCF	Communications control field
APL	A programming language	CCIA	Computer and Communications Industry Association
Arinc	Aeronautical Radio Inc. (airlines network)	CCIS	Common channel interoffice system (AT&T)
ARPA	Advanced Research Project Agency (Department of Defense)	CCITT	International Consultative Committee for Telegraphy and Telephony
Arpanet	ARPA network (Department of Defense)	CCL	Communications control language
ARQ	Automatic request for repetition (IBM)	CCT	Coupler cut through
ASCII	American standard code for information interchange (7 level)	CCU	Communications control unit
ASR	Automatic send/receive (teleprinters)	CDCCP	Control Data communications control procedure (Control Data Corp.)
ATSU	Association of Time-Sharing Users	CDF	Communications-data field
Autodin	Automatic digital network (Department of Defense)	CEPT	Conference of European Postal and Telecommunications Administrations
AVD	Alternate voice/data	CICS	Customer information control system
Basic	Beginners all symbolic instruction code	CMOS	Complementary metal oxide semiconductor
Baudot	Teletypewriter code (5 level)	CPH	Characters per hour
BCC	Block check character	CPODA	Contention priority-oriented demand assignment (protocol)
BCD	Binary coded decimal	CPU	Central processing unit
BDLC	Burroughs data link control	Coax	Coaxial cable
BDN	Bell data network (planned)	Cobol	Common business-oriented language
BER	Bit error rate	COM	Computer output microfilm
BERT	bit-error-rate-test (set)	Comsat	Communications Satellite Corp.
Bit	Binary digit	CPOL	Communications procedure-oriented language
Bit/s	Bits per second	CR	Carriage return
BLU	Basic link unit	CRC	Cyclic redundancy checking
		CRT	Cathode ray tube

CTAK	Cipher text auto key	EIA	Electronic Industries Association
CTS	Communications Technology Satellite or clear to send	EIES	Electronic Information Exchange System (New Jersey Institute of Technology)
Cybernet	Control Data Corp. network	EOA	End of address
DA	Data available	EOM	End of message
DAA	Data access arrangement (AT&T)	EOT	End of text or end of transmission
DAL	Data access line	EPROM	Erasable programmable read only memory
DAP	Data access protocol	ESS	Electronic switch system
Darpa	Defense Advanced Research Project Agency (See ARPA)	FAX	Facsimile
DASD	Direct access storage device	FCC	Federal Communications Commission
Dataset	Synonym for modem (see modem)	FDX	Full-duplex transmission
Datel II	RCA Global Communications data service in conjunction with Telenet	FDM	Frequency-division multiplexer
dB, db	Decibel	FEC	Forward error correction
DBMS	Database management system	FED-STD	Federal standard
DBS	Database service (WUI)	-1001	High-speed synchronous signaling rates between data terminal equipment and data circuit- terminating equipment
DCE	Data circuit-terminating equipment	-1003	Bit-oriented data link control procedures
DCF	Distributive computing facility (Bank of America)	-1005	2.4 kbit/s modems
DCS	Distributed computing system	-1010	ASCII bit sequencing for serial-by- bit transmission
DDCMP	Digital Data communications message protocol (Digital Data Corp.)	-1011	Character structure for serial-by- bit ASCII transmission
DDP	Distributed data processing	-1012	Character structure for parallel-by- bit ASCII transmission
DDS	Dataphone digital service (AT&T)	-1013	Data terminal equipment to data circuit-terminating equipment synchronous signaling rates using 4 Hz circuits
Decnet	Digital Equipment Corp. network	-1020	Electrical characteristics of unbalanced voltage digital interface circuits
DES	Data encryption standard	-1030	Electrical characteristics of balanced voltage digital interface circuits
DLC	Data link control	FF	Form feed
DLCF	Data link control field	FHD	Fixed-head disk
DMA	Direct memory access	FIPS	Federal Information Processing Standards
DMEP	Data-network modified emulator program (Cambridge Telecommunications Inc.)	FIGS	Figures shift (teleprinters)
DNA	Digital network architecture (Digital Equipment Corp.)	FMTP	File management transaction processor (Bank of America)
Domsat	Domestic satellite service	FOC	Fiber optics communications
DOS	Disk operating system	Fortran	Formula translation
DRS	Data rate selector	Fox message	Test message (The quick brown fox jumped over the lazy dog)
DSC	Direct satellite communications	FSK	Frequency-shift keying
DSDS	Dataphone switched digital service (AT&T)	FX	Foreign exchange
DSE	Distributed system environment	GPD	General purpose discipline (first IBM data link control)
DSU	Data service unit	HASP	Houston automatic spooling priority
DTE	Data terminal equipment		
DTS	Digital tandem switch		
EBCDIC	Extended binary coded decimal interchange code (8 level)		
ECOS	Extended communications operating system (Harris Corp.)		
EDP	Electronic data processing		
EFT	Electronic funds transfer		

HDLC	High-level data link control		complements
HDX	Half-duplex transmission	IS 2629-1973	Basic mode control procedures— conversational information message transfer
HID/LoD	High-density/low-density tariff		
HN	Host to network		
Hz	Hertz (cycles per second)	IS 3309-1976	Data communications—high-level data link control procedures— frame structure
IBM TSS	Timesharing system (IBM network)		
ICA	International Communications Association	IS 4335-1977	Data communications—high-level data link control procedures— elements of procedures (independent numbering)
ICST	Institute for Computer Science and Technology		
IDCMA	Independent Data Communications Manufacturers Association	ISO	International Standards Organization
IEEE	Institute of Electrical and Electronic Engineers	IT	Intelligent terminal
IFIPS	International Federation of Information Processing Societies	ITDM	Intelligent time-division multiplexer
IMP	Interface message processor	ITS	Invitation to send
IMS	Information management system (IBM)	ITU	International Telecommunications Union
Infonet	Computer Science Corp. network	JCL	Job control language
Intelsat	International satellite service	KAK	Key-auto-key
I/O	Input/output	KAU	Keystation adapter unit
IPL	Initial program load	KDS	Keyboard display station
IPN	Instant private network	KSR	Keyboard send/receive
IRC	International record carrier	LED	Light-emitting diode
IS	International standard	LF	Line feed
IS-646-1973	Bit-coded character set for information processing interchange	LDM	Limited-distance modem
IS 1155-1973	Information processing—use of longitudinal parity to detect errors in information messages (included in V.4 and X.4)	LIU	Line interface unit
IS 1177-1973	Information processing—character structure for start/stop and synchronous transmission (included in V.4 and X.4)	LIM	Line interface module
IS 1745-1975	Information processing—basic mode control procedures for data communications systems	LO	Line occupancy
IS 2110-1972	Data communication—data terminal and data communication equipment— interchange circuits. Assignment of connector pin numbers (being revised—DIS 2110 is being balloted)	LRC	Longitudinal redundancy check
IS 2111-1972	Data communication—basic mode control procedures—code independent information transfer	LSD	Line-sharing device or line signal detector
IS 2593-1973	Connector pin allocations for use with high-speed data terminal equipment	LSI	Large-scale integrated (circuit)
IS 2628-1973	Basic mode control procedures—	LTRS	Letters shift (teletypewriters)
		Mark III	General Electric Co. Information Services network
		MD	Multiple dissemination
		MDS	Multiple dataset system
		Merit	Michigan network among three largest universities
		MHD	Moving-head disk
		MHP	Message-handling processor (Bank of America)
		MICR	Magnetic ink character recognition
		MIU	Multistation interface unit
		MNCS	Multipoint network-control system
		Modem	Modulator-demodulator
		MOS	Metal oxide semiconductor
		MPCC	Multiprotocol communications controller
		MPL	Multischedule private line
		MSI	Medium-scale integrated (circuit)
		MT	Measured time
		MTBF	Mean time between failures
		MTS	Message telecommunications service (AT&T)
		MTTR	Mean time to repair

MUX	Multiplexer	RMS	Root mean square
MVS	Multiple virtual storage	RO	Receive only
NAK	Negative acknowledgement	ROM	Read only memory
NAM	Network access method (Control Data Corp.)	ROTR	Receive-only typing reperforation
Naruc	National Association of Regulatory Utility Commissioners (state agencies)	RPC	Registered protective circuit
NBS	National Bureau of Standards	RPG	Report program generator
NC	Network connect	RPQ	Request for price quotation
NCP	Network control program (IBM)	RS	Recommended standard (EIA)
NCR-DNA	NCR Corp.-distributed network architecture	RS-232-C	Interface between data terminal equipment and data communication equipment employing serial binary data interchange (August 1969)
NCS	National communications system (Department of Defense)	RS-269-B	Synchronous signaling rates for data transmission (January 1976; identical to ANS IX3.1-1976)
NDT	Net data throughput	RS-334	Signal quality at interface between data processing terminal equipment and synchronous data communication equipment for serial data transmission (Also adopted as ANSI X3.24-1967; new revision being balloted)
NMC	Network management center	RS-357	Interface between facsimile terminal equipment and voice frequency data communication terminal equipment (June 1968)
NRZ	Non-return to zero (waveform)	RS-363	Standard for specifying signal quality for transmitting and receiving data processing terminal equipment using serial data transmission at the interface with non-synchronous data communication equipment (May 1969)
NSP	Network services protocol (Digital Equipment Corp.)	RS-366	Interface between data terminal equipment and automatic calling equipment for data communication (August 1969)
NTPF	Number of terminals per failure	RS-404	Standard for start/stop signal quality between data terminal equipment and non-synchronous data communication equipment (March 1973)
NYPSC	New York Public Service Commission	RS-410	Standard for electrical characteristics of Class A closure interchange circuits (April 1974)
OCR	Optical character recognition	RS-422	Electrical characteristics of balanced voltage digital interface circuits (April 1975)
Octopus	Control Data Corp. network	RS-423	Electrical characteristics of unbalanced voltage digital interface circuits (April 1975)
OS	Operating system		
OSWS	Operating system workstation		
PABX	Private automatic branch exchange		
PAD	Packet assembler/disassembler		
PAM	Pulse amplitude modulation		
PBX	Private branch exchange		
PCM	Pulse-code modulation		
PFEP	Programmable front-end processor		
PIU	Path information unit		
PL/1	Programming language one (IBM)		
PMS	Public message service (WU)		
PMX	Packet multiplexer		
PSC	Public Service Commission		
PSE	Packet-switching exchange		
PROM	Programmable read only memory		
PRTM	Printing response-time monitor		
PTT	Postal Telegraph and Telephone agencies (Europe)		
PUC	Public Utilities Commission		
QAM	Quadrature amplitude modulation		
QTAM	Queued telecommunications access method (IBM)		
RAD	Random access device		
RAM	Random access memory		
RCAC	Remote computer access communications service		
RCD	Receiver-carrier detector		
RDC	Remote data concentrator		
RLSD	Received line signal detector		
RJE	Remote job entry		

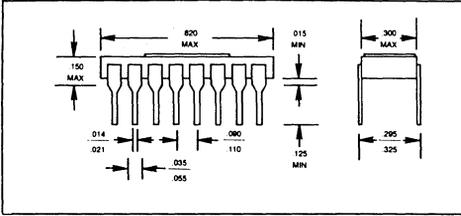
RTS	Request to send	UART	Universal asynchronous receiver/transmitter
RU	Request/response unit		
SDC	Satellite communications controller or specialized common carrier	USASCII	United States of America standard code for information interchange (identical to ASCII)
SCPC	Single channel per carrier	USITA	United States Independent Telephone Association
SDLC	Synchronous data link control (IBM)	V.	CCITT code designation
SID	Swift (see below) interface device	V.1	Equivalence between notation symbols and the significant conditions of a two-condition code
SIMP	Satellite information message protocol		
SMRT	Single message rate timing		
SNA	Systems network architecture (IBM)	V.2	Power levels for data transmission over telephone lines
SNAP	Standard network access protocol		
SNR	Signal/noise ratio	V.3	International alphabet No. 5
SOH	Start of header	V.4	General structure of signals of international alphabet No. 5
SOM	Start of message		
SP	Space character		
Spool	Simultaneous peripheral operation on line (now an accepted term)	V.10 (X.26)	Electrical characteristics for unbalanced double-current interchange circuits for general use with integrated circuit equipment in the field of data communications (and provisional amendments, May 1977)
SQD	Signal quality detector		
STR	Synchronous transmit/receive (4 level code, IBM)		
STX	Start of text		
SU	Signaling unit		
SVD	Simultaneous voice/data		
Swift	Society for Worldwide Interbank Financial Telecommunications (banking network)	V.11 (X.27)	Electrical characteristics for balanced double-current interchange circuits for general use with integrated circuit equipment in the field of data communications (and provisional amendments, May 1977)
Sysgen	System generation		
TAC	Telenet access controller (Telenet Corp.)		
TC	Terminal controller		
TCAM	Telecommunications access method		
TCU	Transmission control unit	V.15	Use of acoustic coupling for data transmission
TDM	Time-division multiplexer		
TDMA	Time-division multiple access	V.19	Modems for parallel data transmission using telephone signaling frequencies
Telex	Teletypewriter exchange service (WU)		
TIMS	Transmission impairment measuring set (Hewlett-Packard)	V.20	Parallel data transmission modems standardized for universal use in the general switched telephone network
TIP	Terminal interface package		
TMS	Telecommunications message switcher	V.21	200-bit/s modem standardized for use in the general switched telephone network
TMU	Transmission message unit		
TNS	Transaction network service (AT&T)	V.22	Standardization of data signaling rates for synchronous data transmission in the general switched telephone network
TSO	Timesharing option		
TTL	Transistor-to-transistor logic		
TTY	Teletypewriter	V.22bis	Standardization of data signaling rates for synchronous data transmission on leased telephone-type circuits
TUCC	Triangle University Computing Center		
TWX	Teletypewriter exchange service		
Tymnet	Timeshare Inc. network	V.23	600/1.2K bit/s modem

	standardized for use in the general switched telephone network		computing (IBM)
V.24	List of definitions for interchange circuits between data terminal equipment and data circuit terminating equipment (and provisional amendments, May 1977)	VTAM	Virtual telecommunications access method (IBM)
V.25	Automatic calling and/or answering equipment on the general switched telephone network, including disabling of echo suppressors on manually established calls	WATS	Wide area telecommunications service (AT&T)
V.26	2.4K/1.2K bit/s modem standardized for use on four-wire leased circuits	WPM	Words per minute
V.26bis	2.4K/1.2K bit/s modem standardized for use in the general switched telephone network	WRU	Who-are-you? character
V.27	4.8 kbit/s modem standardized for use on leased circuits	WUI	Western Union International
V.27bis	4.8 kbit/s modem with automatic equalizer standardized for use on the leased circuits	X-off	Transmitter off
V.27ter	4.8K/2.4K bit/s modem standardized for use in the general switched telephone network	X-on	Transmitter on
V.28	Electrical characteristics for unbalanced double-current interchange circuits	X.	CCITT recommendation designation
V.29	9.6 kbit/s modem for use on leased circuits	X.1	International user classes of service in public data networks
V.31	Electrical characteristics for single-current interchange circuits controlled by contact closure	X.2	International user facilities in public data networks
V.35	Data transmission at 48 kbit/s using 60-to-108 kHz group-bit/s circuits	X.3	Packet assembly/disassembly facility (PAD) in a public data network
V.36	Modems for synchronous data transmission using 60-to-108 kHz group-bit/s circuits	X.4	General structure of signals of international alphabet No. 5 code for data transmission over public data networks
V.41	Code independent control system	X.20	Interface between data terminal equipment and data circuit-terminating equipment for start/stop transmission services on public data networks
V.54	Loop test devices for modems (and provisional amendments, May 1977)	X.20bis (V.21)	Compatible interface between data terminal equipment and data circuit-terminating equipment for start/stop transmission services on public data networks
VAC	Value added carrier	X.21	General purpose interface between data terminal equipment and data circuit-terminating equipment for synchronous operation on public data networks
VAN	Value added network	X.21bis	Use on public data networks of data terminal equipment which is designed for interfacing to synchronous V-series modems
VIP	Visual information projection	X.24	List of definitions of interchange circuits between data terminal equipment and data circuit-terminating equipment on public data networks
VM	Virtual memory	X.25	Interface between data terminal equipment and data circuit-terminating equipment for terminals operating in the packet mode on public data networks (and provisional amendment, April 1977)
V+TU	Voice plus teleprinter unit		
VS	Virtual storage		
VSPC	Visual storage personal		

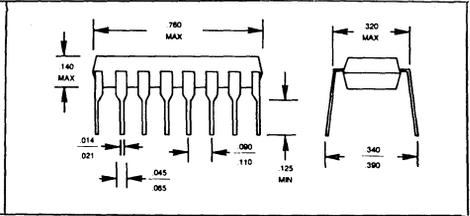
S E C R E T - Z O N E

X.26	Electrical characteristics for unbalanced double-current interchange circuits for general use with integrated circuit equipment in the field of data communications (identical to V.10)		accordance with international alphabet No. 5
		X.92	Hypothetical reference connections for public synchronous data networks
		X.95	Network parameters in public data networks
X.27	Electrical characteristics for balanced double-current interchange circuits for general use with integrated circuit equipment in the field of data communications (identical to V.11)	X.96	Call progress signals in public data networks
		X3.1-1976	Synchronous signaling rates for data transmission
		X3.15-1976	Bit sequencing of the American national standard code for information interchange in serial-by-bit transmission
V.28	DTE/DCE interface for start/stop mode data terminal equipment accessing the packet assembly/disassembly facility (PAD) on a public network situated in the same country	X3.16-1976	Character structure and character parity sense for serial-by-bit data communication in the American national standard code for information interchange
X.29	Procedures for exchange of control information and user data between a packet-mode DTE and a packet assembly/disassembly facility (PAD)	X3.25-1976	Character structure and character parity sense for parallel-by-bit communication in the American national standard code for information interchange
X.30	Standardization of basic model page-printing machine in accordance with international alphabet No. 5	X3.28-1976	Procedures for the use of communication control characters of American national standard code for information interchange in specified data communications links
X.31	Characteristics, from the transmission point of view, at the interchange point between data terminal equipment and data circuit-terminating equipment in a 200 bit/s start/stop data terminal	X3.36-1977	Synchronous high-speed data signaling rates between data terminal equipment and data communication equipment
X.32	Answer-back units for 200 bit/s start/stop machines in accordance with international alphabet No. 5	X3.44-1977	Determination of the performance of data communication systems
		X3.57-1977	Message heading formats for information interchange using ASCII for data communication system control
X.33	Standardization of an international text for the measurement of the margin of start/stop machines in	XTC	External transmit clock

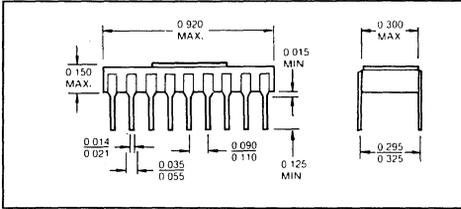
PACKAGE DESCRIPTION



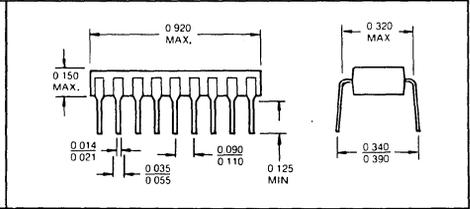
"J" CERAMIC PACKAGE—16 LEADS



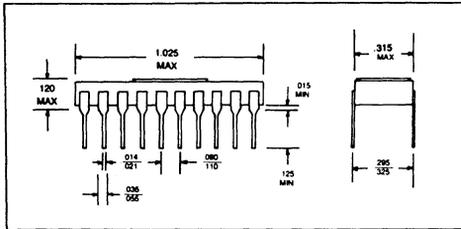
"K" PLASTIC PACKAGE—16 LEADS



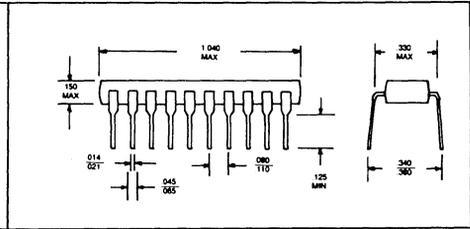
"L" CERAMIC PACKAGE—18 LEADS



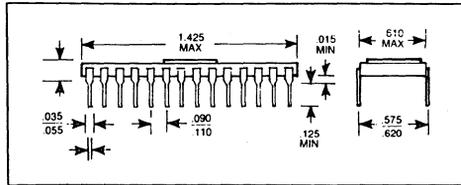
"M" PLASTIC PACKAGE—18 LEADS



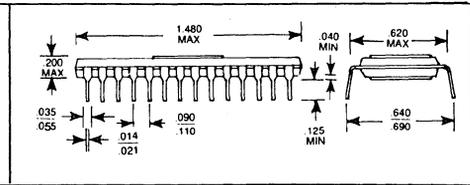
"U" CERAMIC PACKAGE—20 LEADS



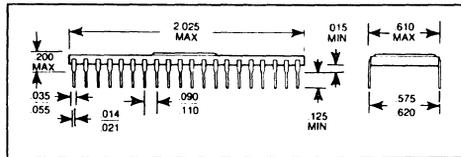
"V" PLASTIC PACKAGE—20 LEADS



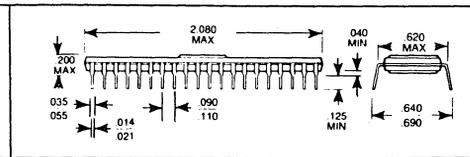
"E" CERAMIC PACKAGE—28 LEADS



"F" PLASTIC PACKAGE—28 LEADS



"A" CERAMIC PACKAGE—40 LEADS



"B" PLASTIC PACKAGE—40 LEADS

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	KIERULFF ELECT.	13 FORTUNE DR. BILLERICA, MA 01821	(617) 667-8331	BOB GREEN
	TIME NEW ENG.	400 NEW BOSTON PARK WOBURN, MA 01801	(617) 935-8080	BOB GREEN
MICHIGAN	GREINER ASSOC.	15324 E. JEFFERSON GROSSE POINT, MI 48230	(313) 499-0188	LEN STRONG
	DIPLOMAT ELECT. (MI)	32708 W. 8 MILE RD. FARMINGTON, MI 48924	(313) 477-3200	LEN STRONG
MINNESOTA	MEL FOSTER TECH. SALES	7389 BUSH LAKE RD. BOX 35216 EDINA, MN 55435	(612) 835-2252	LEN STRONG
	KIERULFF ELECT.	5289 W. 74TH ST. EDINA, MN 55435	(612) 835-4388	LEN STRONG
	DIPLOMAT (MN)	3816 CHANDLER DR. MINNEAPOLIS, MN 55421	(612) 788-8601	LEN STRONG
MISSOURI	NEVCO	1715 BALTIMORE AVE. KANSAS CITY, MO 64108	(816) 421-1751	LEN STRONG
	NEVCO	10132 GLENFIELD TER. CRESTWOOD, MO 63126	(314) 843-7406	LEN STRONG
MISSISSIPPI	MURCOTA CORP.	1106 BURKE ST. WINSTON SALEM, NC 27101	(919) 722-9445	BOB GREEN
MONTANA	KIERULFF ELECT.	3695 W. 1987 S. SALT LAKE CITY, UT 84104	(801) 973-6913	BOB GREEN
NEVADA	EL REPCO	55 SURREY DR. RENO, NV 89511	(702) 849-2899	E. ZITTLE
	BELL IND.	1161 N. FAIROAKS AVE. SUNNYVALE, CA 94086	(408) 734-8570	E. ZITTLE
	KIERULFF ELECT.	3969 E. BAYSHORE RD. PALO ALTO, CA 94303	(415) 968-6292	E. ZITTLE
NEBRASKA	NEVCO	1715 BALTIMORE AVE. KANSAS CITY, MO 64108	(816) 421-1751	LEN STRONG
	DIPLOMAT (MO)	2721 MERCANTILE DR. ST. LOUIS, MO 63144	(314) 645-8558	LEN STRONG
NEW HAMPSHIRE	COMPONENT TECH.	155-U NEW BOSTON #172 WOBURN, MA 01801	(617) 933-5390	BOB GREEN
	KIERULFF ELECT.	13 FORTUNE DR. BILLERICA, MA 01821	(617) 935-8331	BOB GREEN
	TIME NEW ENG.	400 NEW BOSTON PARK WOBURN, MA 01801	(617) 935-8080	BOB GREEN

STATE	COMPANY	ADDRESS	PHONE	AREA MGR
NEW JERSEY	E.R.A.	354 VETERANS MEMORIAL HWY. COMMACK, NY 11725	(516) 543-0510 NJ) 800-645-5500-5501	BOB GREEN
	GCM ASSOC.	1014 BETHLEHEM PIKE ERDENHEIM, PA 19118	(215) 785-1830	BOB GREEN
	DIPLOMAT	490 S. RIVERVIEW DR. TOTOWA, NJ 07512	(201) 785-1830	BOB GREEN
	MID ATLANTIC ELECTRONICS	INTERSTATE INDUSTRIAL PARK KOR-CENTER, EAST H-1 BELL MAWR, N.J. 08031	(609) 931-5303	BOB GREEN
	TIME MID ATL.	359 E. MADISON AVE. CLIFTON HTS., PA 19018	(215) 622-2500	BOB GREEN
	KIERULFF ELECT.	3 EDISON PLACE FAIRFIELD, NJ 07006	(201) 575-6750	BOB GREEN
NEW YORK	OSSMANN COMP. SALES	154 PICKARD BLDG. SYRACUSE, NY 13211	(315) 455-6611	BOB GREEN
	OSSMANN COMP.	280 METRO PARK ROCHESTER, NY 14623	(716) 424-4460	BOB GREEN
	E.R.A.	354 VETERANS MEMORIAL HWY. COMMACK, NY 11725	(516) 543-0510 NJ) 80-645-5500-5501	BOB GREEN
	DIPLOMAT	110 MURCUS DRIVE MELVILLE, NY 11747	(516) 454-6334	BOB GREEN
	KIERULFF ELECT.	3 EDISON PLACE FAIRFIELD, NJ 07006	(201) 575-6750	BOB GREEN
	TIME NEW ENG.	400 NEW BOSTON PARK WOBURN, MA 01801	(617) 935-8080	BOB GREEN
	ZEUS COMPONENTS	500 EXECUTIVE BLVD. ELMSFORD, NY 10523	(914) 593-4120	BOB GREEN
NORTH CAROLINA	MURCOTA CORP.	1106 BURKE ST. WINSTON SALEM, NC 27101	(919) 722-9445	BOB GREEN
	DIPLOMAT (FL)	2120 CALUMET ST. CLEARWATER, FL 33515	(813) 443-4514	BOB GREEN
NORTH & SOUTH DAKOTA	MEL FOSTER TECH. SALES	7389 BUSH LAKE RD. EDINA, MN 55435	(612) 835-2252	LEN STRONG
	DIPLOMAT (MN)	3816 CHANDLER DR. MINNEAPOLIS, MN 55421	(612) 788-8601	LEN STRONG
NEW MEXICO	DAR-C INC.	14425 N. SCOTTDALE RD. #500 SCOTTSDALE, AZ 85254	(602) 948-2240	JOE MADER
OHIO	EMA	35 COMPARK RD. BOX 449 CENTERVILLE, OH 45459	(513) 433-2800	LEN STRONG
	EMA	337 GARFIELD RD. BOX 275 AURORA, OH 44202	(216) 562-6104	LEN STRONG
	DEECO INC.	2500 S.W. 16TH AVE CEDERS RAPIDS, OH 52406	(319) 365-7551	LEN STRONG
	IND'L PRODUCTS	35 COMPARK RD. CENTERVILLE OH 45459	(513) 435-2086	LEN STRONG
	IND'L PRODUCTS	337 GARFIELD RD. AURORA, OH 44202	(216) 562-8113	LEN STRONG
OKLAHOMA	COMPONENT SPEC.	7920 E. 40TH ST TULSA, OK 74145	(918) 664-2820	LEN STRONG

REPRESENTATIVE DISTRIBUTOR

STATE	COMPANY	ADDRESS	PHONE	AREA MGR
OREGON	COMPONENTS WEST	13540 N.W. MILL CREEK PORTLAND, OR 97229	(503) 643-5588	E. ZITTE
	KIERULFF ELECT.	1005 ANDOVER PK E. TUKWILA, WA 98188	(206) 575-4420	E. ZITTE
PENNSYLVANIA	GCM	1014 BETHLEHEM PIKE ERDENHEIM, PA 19118	(215) 233-4600	BOB GREEN
	EMA	35 COMPARK RD. BOX 449 CENTERVILLE, OH 45459	(513) 433-2800	BOB GREEN
	KIERULFF ELECT.	3 EDISON PLACE FAIRFIELD, NJ 07006	(201) 575-6750	BOB GREEN
	TIME MID ATL	359 MADISON AVE. CLIFTON HTS. PA 19018	(215) 622-2500	BOB GREEN
	MACK ELECTRONIC	1014 BETHLEHEM PIKE ERDENHEIM, PA 19118	(215) 233-4650	BOB GREEN
RHODE ISLAND	COMPONENT TECH.	155-U NEW BOSTON PK. #172 WOBURN, MA 01801	(617) 933-5390	BOB GREEN
	TIME NEW ENG.	400 NEW BOSTON PARK WOBURN, MA 01801	(617) 935-8080	BOB GREEN
SOUTH CAROLINA	MURCOTA CORP.	1106 BURKE ST. WINSTON SALEM, NC 27101	(919) 722-9445	BOB GREEN
	DIPLOMAT (FL)	2120 CALLUMET ST. CLEARWATER, FL 33515	(813) 443-4514	BOB GREEN
TENNESSEE	MURCOTA CORP.	1106 BURKE ST. WINSTON, SALEM, NC 27101	(919) 722-9445	BOB GREEN
TEXAS	DAR-C	14425 N. SCOTTSDALE #500 SCOTTSDALE, AZ 85254	(602) 948-2240	LEN STRONG
	WEST ASSOC.	4300 ALPHA RD. #106 DALLAS, TX 75234	(214) 661-9400	LEN STRONG
	WEST ASSOC.	9730 TOWN PARK #101 HOUSTON, TX 77036	(713) 777-4108	LEN STRONG
	WEST ASSOC.	4515 MANCHACA RD. # 105 AUSTIN, TX 78745	(512) 441-6973	LEN STRONG
	COMPONENT SPEC.	10907 SHADY TRAIL DALLAS, TX 75220	(214) 357-6511	LEN STRONG
	COMPONENT SPEC.	8222 JAMESTOWN RD. AUSTIN, TX 78758	(512) 837-8922	LEN STRONG
	COMPONENTS SPEC.	8181 COMMERCE PARK DR. HOUSTON, TX 77036 SUITE 700	(713) 771-7237	LEN STRONG
	QUALITY COMPONENTS	1020 McKALLA #D AUSTIN, TX 78758	(512) 835-0220	LEN STRONG
	QUALITY COMPONENTS	4257 KELLWAY CIRCLE ADDISON, TX 75001	(214) 387-4949	LEN STRONG
	QUALITY COMPONENTS	6126 WESTLINE HOUSTON, TX 77036	(713) 772-7100	LEN STRONG

STATE	COMPANY	ADDRESS	PHONE	AREA MGR
UTAH	COMPONENT SALES	2520 S. STATE ST. #102 BOX 15084 SALT LAKE CITY, UT 84115	(801) 485-0363	E. ZITTLER
	BELL INDUSTRIES	3639 W. 2150 SOUTH SALT LAKE CITY, UTAH 84120	(801) 972-6969	E. ZITTLER
	DIPLOMAT (UT)	3007 S.W. TEMPLE SALT LAKE CITY, UT 84115	(801) 486-4134	E. ZITTLER
	DIPLOMAT	7100 BROADWAY-BLDG 6 DENVER, CO 80221	(303) 427-5544	E. ZITTLER
	KIERULFF ELECT.	3695 W. 1987 S. SALT LAKE CITY, UT 84104	(801) 973-6913	E. ZITTLER
VERMONT	COMPONENT TECH.	155-U NEW BOSTON PK #172 WOBURN, MA 01801	(617) 933-5390	BOB GREEN
VIRGINIA	NEW ERA SALES	7310 RITCHIE HWY. #407 EMPIRE TOWERS GLEN BURNIE, MD 21061	(301) 768-6666	BOB GREEN
	TIME MID ATL.	359 E. MADISON AVE. CLIFTON HTS. PA 19018	(215) 622-2500	BOB GREEN
WASHINGTON	COMPONENTS WEST	451 S.W. 10TH ST. #109 RENTON, WASH. 98055 BOX 58006, TUKWILA, WA 98188	(206) 271-5252	E. ZITTLER
	KIERUIFF	1005 ANDOVER PK. E. TUKWILA, WA 98188	(206) 575-4420	E. ZITTLER
WASHINGTON DC	NEW ERA SALES	7310 RITCHIE HWY. #407 EMPIRE TOWERS GLEN BURNIE, MD 21061	(301) 768-6666	BOB GREEN
	TECHNICO	9051 RED BRANCH RD. COLUMBIA, MD 21044	(301) 995-1995	BOB GREEN
	TIME MID ATL.	359 MADISON AVE. CLIFTON HTS. PA 19018	(215) 622-2500	BOB GREEN
WEST VIRGINIA	NEW ERA SALES	7310 RITCHIE HWY. #407 EMPIRE TOWERS GLEN BURNIE, MD 21061	(301) 768-6666	BOB GREEN
WISCONSIN	MEL FOSTER TECH. SALES	7389 BUSH LAKE RD. EDINA, MN 55435	(612) 835-2252	LEN STRONG
	JANUS INC.	3166 DES PLAINES DES PLAINES, IL 60018	(312) 298-9330	LEN STRONG
	KIERULFF ELECT.	2212 E. MOORELAND AVE. WAUKESTA, WI 53186	(414) 784-8160	LEN STRONG
	DIPLOMAT (MN)	3816 CHANDLER DR. MINNEAPOLIS, MN 55421	(612) 788-8601	LEN STRONG
	DIPLOMAT (ILL)	1071 JUDSON BENSENVILLE, IL 60106	(312) 595-1000	LEN STRONG
WYOMING	COMPONENT SALES	5925 E. EVANS AVE. #204B DENVER, CO 80222	(303) 759-1666	E. ZITTLER
	DIPLOMAT (UT)	3007 S.W. TEMPLE SALT LAKE CITY, UT 84115	(801) 486-4134	E. ZITTLER

FOREIGN REP/DIST QUICK REFERENCE BY COUNTRY

COUNTRY	COMPANY	ADDRESS	PHONE NO.	TELEX NO.
AUSTRALIA	DANEVA CONTROLS	70 BAY ROAD, SANDRIGHAM 3191 VICTORIA, AUSTRALIA	(3) 598-9207	79034439
AUSTRIA	INTRACO AF-SYSTEME GMBH	AM BRUNNER 19 D-8011 HEIMSTETTEN POST KIRCHHEIM, WEST GERMANY	(089) 90 36 191	8415216329
BELGIUM	ETS JP LEMAIRE	RAMPE GAULOISE 1A 1020 BRUXELLES BELGIUM	479-8690	84624610
BRAZIL	EXIMEL IMPORTACAO	E EXPORTACAO LTDA RUA AURORA 171/CJ2 SAO PAULO BRAZIL CEP 01209	(011) 222-4170 (011) 223-7388	3911131298
CANADA	WEBER ELECTRONIC	105 BRISBANE ROAD DOWNSVIEW, ONTARIO M3J 2K6	(416) 663-5650	6104223048
DIST	SEMAD ELECTRONIC OTTAWA OFFICE:	864 LADY ELLEN PLACE OTTAWA, ONTARIO KLZ 5L5		6104921337
	SEMAD ELECTRONIC DORVAL OFFICE	620 MELOCHE AVENUE DORVAL, QUEBEC H9P 2P4		6104921337
DENMARK	C-88	ULDVRJEN 10 DK-2970 HORSHOLM, DENMARK	02-5708-88	85537578
ENGLAND	PRONTO	466-478 CRANBROOK ROAD, GANTS HILL, ILFORD, ESSEX. IG2 6LE	01-599-3041	(851) 8954213
FINLAND	KOMDEL OY	VANHA FINNOONTIE 4 02270 ESPOO 27, FINLAND BOX 32, 02271 ESPOO 27, FINLAND	90-885001	857121926
FRANCE	TECHNOLOGY RESOURCES	27-29 RUE DES POISSONNIERS 92200 NEUILLY-SUR-SEINE, FRANCE	747-4717 747-7051	842610657
W. GERMANY	INTRACO SYSTEME GMBH	AM BRUNNER 19 D-8011 HEIMSTETTEN POST KIRCHHEIM, WEST GERMANY	(089) 90 36 191	8415216329
DIST.	ELECTRONIC 2000 VERTRIEBS CMBM	8000 MUNCHEN 80 NEUMARKTER STRASSE 75 WEST GERMANY	(089) 43 40 61	841522561
HOLLAND	DIODE	HOLLAND LAAN NO. 22 UTRECHT, HOLLAND	030884214	(846) 47388
HONG KONG	WHITE & ALLCOCK	TOPPAN BUILDING, 6TH FLOOR 22 WESTLANDS ROAD QUARRY BAY, HONG KONG	5-632113-8 5-644312 5-644332	78083640
INDIA	KRYONIX	KOWDAIR, TRIVANDRUM PIMCODE: 695003, SOUTH INDIA	63805	953884307
U.S. OFFICE	MIRCO AIDS INT'L	778 BLUE SAGE DRIVE SUNNYVALE, CALIF 94086	(408) 738-2295	

COUNTRY	COMPANY	ADDRESS	PHONE NO.	TELEX NO.
ISRAEL	VECTRONICS LTD	69 DORDONS ST. BOX 16335 TEL AVIV, ISRAEL	(010) 23 44 24 (010) 22 84 72 (010) 24 63 12	92232396
ITALY	COMPREL S.R.L.	20092 CINSELLO B. (MI) — V. LE ROMAGNA, ITALY	(02) 61206412	843332484
JAPAN	PANETRON DIV. TOKYO ELECTRON LIMITED	38 FL. SHINJUKU NOMURA BD. 1-26-2, NISHI-SHINJUKU SHINJUKU-KU, TOKYO 160 JAPAN	03-343-4411	781-2322220
U.S. OFFICE:	PAN ELECTRON INCORPORATED	465 S. MATHILDA AVE SUNNYVALE, CALIF. 94086	(408) 735-8731	346342
NEW ZEALAND	DANEVA CONTROL	70 BAY ROAD, SANDRIGHAM 3191 VICTORIA, AUSTRALIA	(03) 598-9207	79034439
NORWAY	HANS H. SCHIVE A/S ELECTRONIC COMPONENTS	GUSTAV VIGELANDS vei 5, BOX 250 SKOYEN OSLO 2 NORWAY	(010) 475754655	85619124
REP. OF IRELAND	NELTRONIC LTD	JOHN F. KENNEDY ROAD NAAS ROAD DUBLIN 12, REP. OF IRELAND	DUBLIN 501845	8524837
SINGAPORE	TOTAL COMPUTER SYSTEMS (S) PTE LTD.	20/237, 6TH FLOOR BLOCK 12 50, KALLANG BAHRU. SINGAPORE 12	(786) 293-4401	78623910
SOUTH AFRICA	SOUTH CONTINENTAL DEVICES	5TH FLOOR, RANDOVER HOUSE DOVER ST. 960 RANDBURG, S. AFRICA	(011) 789-2400	9604-24849
SPAIN	INTERFACE S.A.	RDA SAN PEDRI 22, 30 BARCELONA, 10 SPAIN	93-456-31-51	83151508
SWEDEN	TELEIMPORT AB	BOX 5071 S 162 05 VALLINGBY, SWEDEN	VX 08-89-0435	85413033
SWITZERLAND	STOLZ AG	TAFERNSTRASSE 15 5405 BADEN-DATTWIL, SWITZERLAND	056/84 01 51	84554070
TAIWAN (REP/CHINA)	TAIWAN AUTOMATION CO.	8TH FLOOR 270 NANKING E. RD SECTION 3, TAIPEI TAIWAN, R.O.C.	(02) 771-0940-3	78511942
NEW JERSEY OFFICE:	SST TRADE & DEVELOPMENT	1101 SLOCUM AVE RIDGEFIELD, NEW JERSEY 07657	(201) 941-3333	135197

**2445 McCABE WAY, POST OFFICE BOX 2180
IRVINE, CALIFORNIA 92714
(714) 557-3550, TWX 910-595-1139**

**2445 McCABE WAY, POST OFFICE BOX 2180
IRVINE, CALIFORNIA 92714
(714) 557-3550, TWX 910-595-1139**