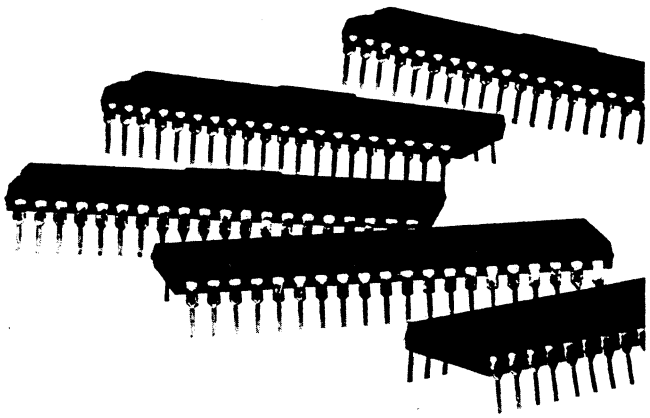
The MICROENGINE Company

The WD9000 Pascal MICROENGINE™ Microprocessor Chip Set

FEATURES

- Direct Execution of Pascal Intermediate Code (P-Code)
- High Level Language Programming with Assembly Language Efficiency
- 16-Bit Stack-Based Architecture
- Executes Full USCD Pascal, Version III.0
- Program Size to 128K Bytes
- 3.0 MHz Four-Phase Clock
- Four-Level Interrupt Structure
- Hardware Multiply/Divide
- Hardware Floating Point
- Single and Multi-Byte Instructions
- TTL Compatible Three-State Interface
- Memory Mapped I/O



Pascal MICROENGINE™ Five Chip Set

DESCRIPTION

The WD9000 Microprocessor is a 16-bit MOS/LSI Chip Set that directly executes programs written in the Pascal programming language at speeds five or more times greater than equivalent systems using interpreters. The Chip Set consists of five LSI components:

- *Arithmetic Component* — contains the arithmetic logic unit, microinstruction decode, register file, and paths to control processor operation.
- *Control Processor* — contains macroinstruction decode, portions of the control circuitry, microinstruction counters, and I/O control logic.
- *MICROM Components* — three high-speed, 512 x 22 bit, custom MICROMs implement P-Code instructions.

The MICROENGINE™ Microprocessor Chip Set is designed for a large range of applications which could gain from 16-bit throughput and/or direct Pascal execution. Pascal is a high-level programming language which provides an environment conducive to structured software development. The WD9000 Microprocessor Chip Set directly executes the University of California at San Diego (UCSD) Pascal System, Version III.0, which is widely used throughout the industry on eight- and sixteen-bit processors.

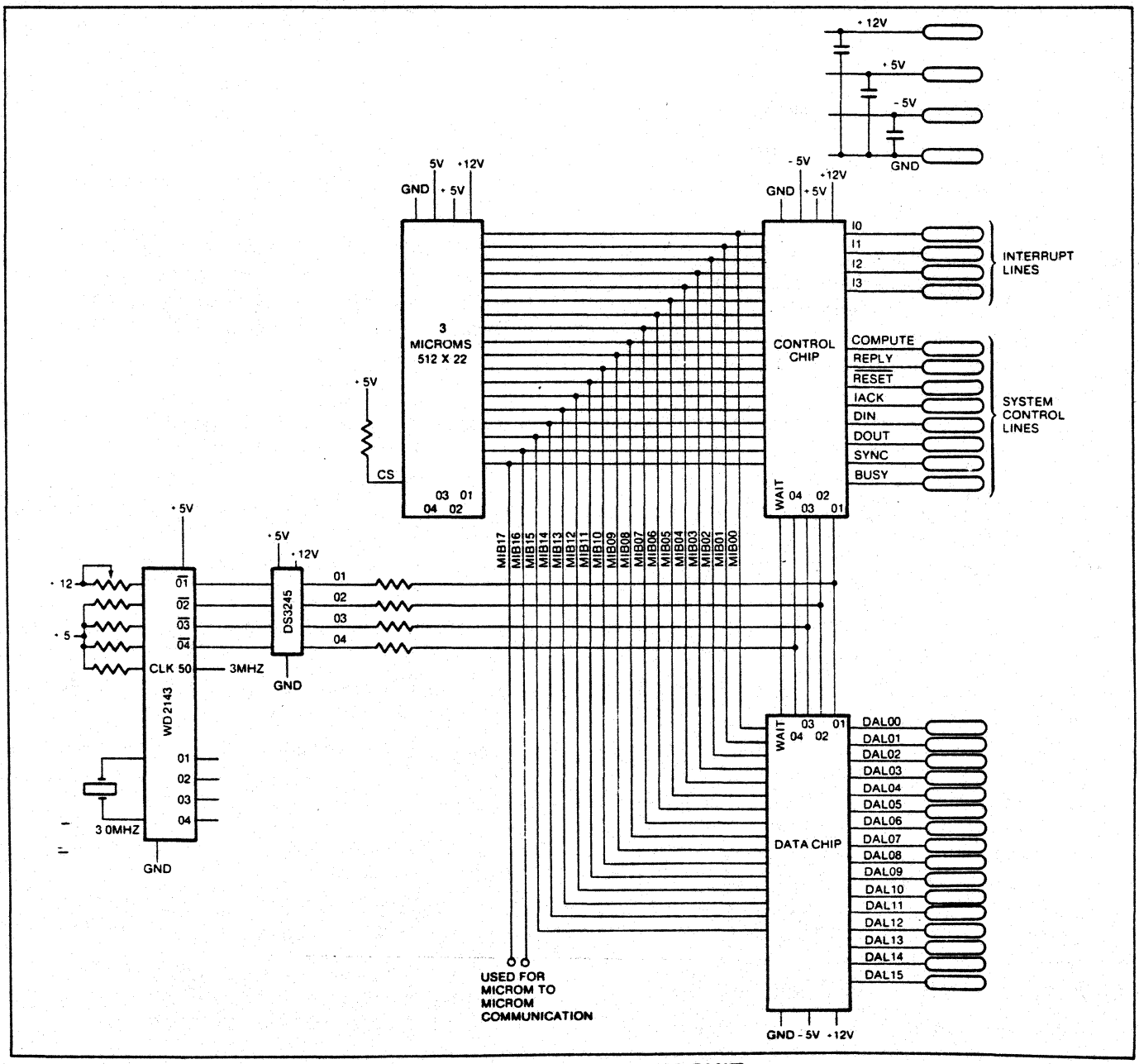
The WD9000 Microprocessor includes:

- *P-Machine Architecture* — implements the UCSD Version III.0 P-Machine, an ideal architecture (stack oriented) for execution of Pascal programs. This approach replaces the alternative of software interpreters or compilation to architectures less suited for Pascal.
- *Sixteen-Bit I/O and Data Paths for High Throughput* — all address, data and I/O paths are sixteen bits wide.
- *Stack Architecture for Reentrant and Recursive Programs* — all Pascal programs are reentrant and recursive with no performance penalty
- *High-Level Language Programming of I/O and Interrupts* — simple access to device and system control provided in the Pascal language.
- *Hardware Multiply/Divide* — 16-bit multiply and divide instructions.
- *Floating Point Hardware* — instructions provide execution of floating point instructions using the proposed IEEE standard.
- *Four-Level Interrupt Structure* — each level represents an interrupt priority.
- *TTL Compatible Three-State Interface* — standard parts may be used to interface to the Chip Set.
- *Memory Mapped I/O* — the language and Chip Set support memory mapped I/O, where I/O devices are accessed as memory locations.

BENEFITS

Use the WD9000 Pascal MICROENGINE™ Microprocessor Chip Set has significant benefits for the system designer:

- *High Performance* — throughput of the 16-bit CPU provides processing power needed for many applications.
- *Lower Software Development Cost* — use of Pascal increases programmer productivity, decreasing software development costs over alternative approaches. These productivity increases are the result of the language's high-level nature, extensive error checking, automatic reentrancy and recursion.
- *Shortened Development Schedules* — critical software development schedules are shortened.
- *Transportability* — programs written in the industry standard UCSD Pascal may be executed on other Pascal-based systems.
- *Efficient Memory Utilization* — Since the P-Machine is an ideal architecture for Pascal execution, memory utilization is equivalent to that of software programmed in assembly language on other processors and less than on systems using interpreters or compilers operating on architectures not optimized for Pascal.
- *System Reliability* — reliability, the probability that programs will perform their intended function, is improved by extensive compiler error checking. In addition, since Pasçal programs are simpler statements of the algorithm to be executed than the alternative tools, reliability is further enhanced.



TYPICAL WD9000 CPU CIRCUIT

PIN ASSIGNMENTS

The following are pin assignments for the Pascal MICRO-ENGINE™ Microprocessor Chip Set:

DATA CHIP PIN ASSIGNMENTS

PIN NO.	SIGNAL	PIN NO.	SIGNAL	PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	ø3	11	DAL08	21	ø2	31	$\overline{\text{MIB07}}$
2	V_{BB}	12	DAL09	22	WAIT	32	$\overline{\text{MIB06}}$
3	DAL00	13	DAL10	23	$\overline{\text{MIB15}}$	33	$\overline{\text{MIB05}}$
4	DAL01	14	DAL11	24	$\overline{\text{MIB14}}$	34	$\overline{\text{MIB04}}$
5	DAL02	15	DAL12	25	$\overline{\text{MIB13}}$	35	$\overline{\text{MIB03}}$
6	DAL03	16	DAL13	26	$\overline{\text{MIB12}}$	36	$\overline{\text{MIB02}}$
7	DAL04	17	DAL14	27	$\overline{\text{MIB11}}$	37	$\overline{\text{MIB01}}$
8	DAL05	18	DAL15	28	$\overline{\text{MIB10}}$	38	$\overline{\text{MIB00}}$
9	DAL06	19	V_{SS}	29	$\overline{\text{MIB09}}$	39	V_{DD}
10	DAL07	20	ø4	30	$\overline{\text{MIB08}}$	40	ø1

CONTROL CHIP PIN ASSIGNMENTS

PIN NO.	SIGNAL	PIN NO.	SIGNAL	PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	ø3	11	$\overline{\text{MIB16}}$	21	ø2	31	$\overline{\text{MIB07}}$
2	V_{BB}	12	REPLY	22	V_{CC}	32	$\overline{\text{MIB06}}$
3	I3	13	WAIT	23	$\overline{\text{MIB15}}$	33	$\overline{\text{MIB05}}$
4	I2	14	DOUT	24	$\overline{\text{MIB14}}$	34	$\overline{\text{MIB04}}$
5	I1	15	NC	25	$\overline{\text{MIB13}}$	35	$\overline{\text{MIB03}}$
6	I0	16	IACK	26	$\overline{\text{MIB12}}$	36	$\overline{\text{MIB02}}$
7	$\overline{\text{MIB17}}$	17	SYNC	27	$\overline{\text{MIB11}}$	37	$\overline{\text{MIB01}}$
8	BUSY	18	DIN	28	$\overline{\text{MIB10}}$	38	$\overline{\text{MIB00}}$
9	COMPUTE	19	V_{SS}	29	$\overline{\text{MIB09}}$	39	V_{DD}
10	$\overline{\text{RESET}}$	10	ø4	30	$\overline{\text{MIB08}}$	40	ø1

MICROM CHIP PIN ASSIGNMENTS

PIN NO.	SIGNAL	PIN NO.	SIGNAL	PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	ø3	11	$\overline{\text{MIB16}}$	21	ø2	31	$\overline{\text{MIB06}}$
2	V_{BB}	12	$\overline{\text{MIB17}}$	22	V_{CC}	32	$\overline{\text{MIB05}}$
3	NC	13	NC	23	CS	33	$\overline{\text{MIB04}}$
4	NC	14	NC	24	NC	34	$\overline{\text{MIB03}}$
5	NC	15	NC	25	NC	35	$\overline{\text{MIB02}}$
6	NC	16	NC	26	$\overline{\text{MIB11}}$	36	NC
7	$\overline{\text{MIB15}}$	17	NC	27	$\overline{\text{MIB10}}$	37	$\overline{\text{MIB01}}$
8	$\overline{\text{MIB14}}$	18	NC	28	$\overline{\text{MIB09}}$	38	$\overline{\text{MIB00}}$
9	$\overline{\text{MIB13}}$	19	V_{SS}	29	$\overline{\text{MIB08}}$	39	V_{DD}
10	$\overline{\text{MIB12}}$	20	ø4	30	$\overline{\text{MIB07}}$	40	ø1

PIN FUNCTIONS

The following describes the function of each pin:

BUSY (TTL)
The BUSY is a Control signal from an external unit to the Processor requesting access to the bus. The signal can be used by a DMA unit to access the memory. The BUSY signal is interrogated at ø3 by the Processor every time READ or WRITE instructions are taking place. Whenever the BUSY signal is found to be on, the Processor enters a WAIT state inhibiting any access operation from taking place. The Processor will resume normal operation as soon as BUSY is turned off.

CS
CS (Chip Select) is always connected to +5 Volts.

ø1-ø4 CLOCK CYCLES

These cycles may be generated by the CP 2143 Clock Chip or by external user supplied circuitry. Cycles occur every 83 nanoseconds, yielding a 333 nanosecond interval between each occurrence of a given clock.

COMPUTE (TTL)

The processor examines COMPUTE during every ø1 to determine whether or not it should execute the present microinstruction. In the case of a two cycle instruction, COMPUTE need be high only during ø1 of the first cycle. Among other things, COMPUTE may be used to control single stepping of microinstructions. This line should not be confused with the WAIT signal on the MIB bus.

DAL 00-DAL 15 (TTL)

Data/Address Lines, used to transfer addresses and data from the processor and receive data into the processor. Signals are logical true data.

DIN (TTL)

The DATA-IN (DIN) is a Control signal from the Processor to cause the address unit to gate its Read data on the Data lines. It is made high at the time the address is removed from the lines, or one cycle after the SYNC is made high (the second ø2 of the INPUT) and is a function of the READ instruction. The DATA-IN is made low at the end of the Input Byte or Input Word instruction or when SYNC is made low. This signal can be used to control the enabling of external TTL Tri-State Bus Driver/Receivers.

DOUT (TTL)

The DATA-OUT (DOUT) is a Control signal from the Processor which is made high at the same time as the Write data (ø1 following the OUTPUT) is placed on the DAL bus by the Processor. It remains high for the duration of the OUTPUT instruction, dropping one phase before the data is taken off the DAL bus.

IACK (TTL)

The IACK is a Control signal from the Processor

which signifies that the Processor is responding to an Interrupt. This signal is made high at the same time the SYNC is made high as a result of either 'RA' or 'WA' instructions, and stays high as long as SYNC is high.

I0-I3

I0-I3 provide four interrupt request levels to the chip set. Interrupts are tested by priority from I0 to I3. If an Interrupt is pending on any line the chip set will execute an Interrupt Acknowledge sequence. This sequence presents a 4 bit code on the DAL lines which provides mask capability to disable other interrupt levels.

MIB00-MIB10

These lines carry data bidirectionally between MICROM's and the Data and Control Chips. They are unconditionally precharged Hi at ø4 by the MICROM's attached to the bus. At the following ø1 they may have two different meanings, depending upon whether the Microinstruction presently being executed is a one cycle or a two cycle instruction.

If the Microinstruction executes one cycle, then the next ø1 conveys the next microinstruction from the Microinstruction ROM to the Data Chip and Control Chip.

If the Microinstruction takes two cycles, the second occurrence of ø1 may result in data being transferred from the Data Chip to the Control Chip. At ø2, address data is transferred from the Location Counter in the Control Chip to the MICROM. At ø3 the address data remains valid on the bus. The processor cycle is completed by an unconditional precharge of these lines by the MICROM at ø4.

MIB11-MIB14

These lines serve to convey Microinstruction data from the MICROM to the Data and Control Chips in much the same fashion as the preceding lines do. These lines are unconditionally precharged Hi by the MICROM at ø4. At ø1 of a single cycle they are conditionally discharged to represent Micrinstruction Data from the MICROM to the Data Chip and the Control Chip.

If the preceding Microinstruction was of the 2-cycle variety, the second occurrence of ø1 on these lines can carry data from the Data Chip to the Control Chip. These lines have no other significance during ø2 and ø3.

MIB15

MIB15 is used to carry Microinstruction data from the MICROM to the Data Chip and Control Chip and also to transfer the results of conditional jump tests from the Data Chip to the Control Chip.

This line is precharged Hi unconditionally by the MICROM at ø3. At ø4 it can be conditionally discharged by the results of a conditional jump test.

At ø1 this line conveys the microinstruction data from the MICROM to the Data and Control Chip. In the case of a microinstruction whose execution takes two cycles, the second occurrence of ø1 may serve to convey data from the Data Chip to the Control Chip. The contents of MIB15 are not significant at ø2. The cycle is completed by an unconditional precharge of MIB15 at ø3.

MIB16

This control line conveys data from the ROM to the Control and Data Chips and from the Control Chip to the MICROM. It is unconditionally precharged HI at ø2 and ø4. At ø1 following ø4 it may conditionally discharge low by the MICROM in which case the signal is interpreted by the Control Chip as a command to load the subroutine Return Register with the incremented content of the Location Counter. On ø2 the lines are unconditionally precharged Hi. At ø3, the Control Chip may conditionally discharge this line. If it does so, this is an instruction to the selected MICROM to disable its outputs at the next ø1. In this fashion, 2 cycle instructions inhibit the transfer of new microinstructions from the MICROM to the Control Chip and the Data Chip.

MIB17

MIB17 conveys the READ NEXT INSTRUCTION imperative from the MICROM to the Control Chip. This line is unconditionally precharged by the MICROMs attached to the Microinstruction Bus and conditionally discharged at ø1. A discharge indicates that the RNI imperative is required.

REPLY (TTL)

The REPLY is a Control signal used by the addressed unit to respond to the Processor's Data Access signals.

The REPLY signal must be high during ø3 of the INPUT or OUTPUT microinstruction execution cycle in order for this operation to complete. The REPLY signal is also interrogated by READ and WRITE microinstructions and it must be low during ø3 in order for these operations to take place.

RESET (TTL)

Activation of the RESET line causes the Microprocessor to force 001 into the Location Counter.

A NOP is also forced into the MIR and the MI registers. SYNC and DATA-IN are both reset. The RESET line can be wired to a POWER ON reset or it may be used by the program for its own purposes.

SYNC (TTL)

The SYNC is a Control signal used to initiate and signify the length of a Data Access operation. SYNC is made high as soon as an address becomes valid. This occurs at ø2 following a READ or WRITE. It remains high until the termination of the operation.

V_{BB}
−5 Volt Supply

V_{CC}
+5 Volt Supply

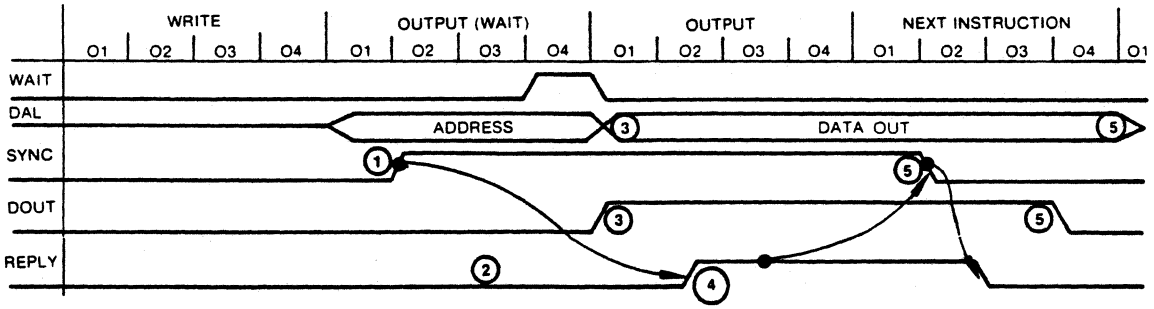
V_{DD}
+12 Volt Supply

V_{SS}
Logic Ground

WAIT

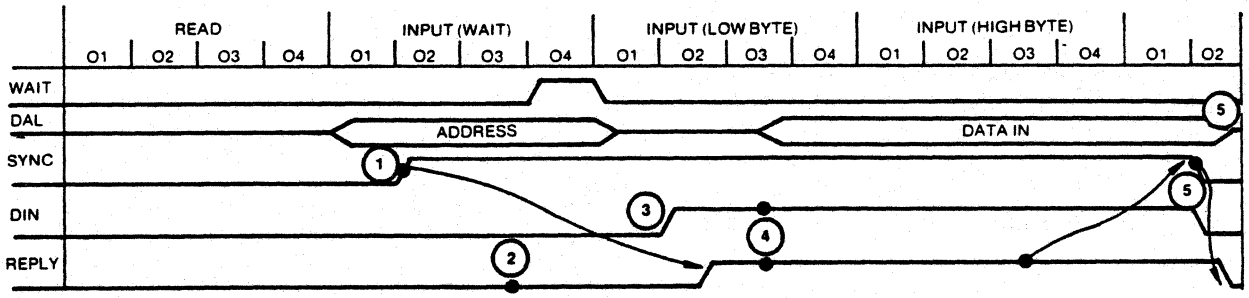
The WAIT Line from the Control Chip to the Data Chip establishes whether or not the Data Chip is in the RUN or WAIT mode. Whenever the WAIT control line is in the Low state, the Data Chip is in the RUN mode and the Microinstruction will be loaded into the MIR register and executed. This line is normally Low and must be driven Hi during ø4 to cause the Data Chip to enter the WAIT state. It always returns to Low when the beginning edge of the ø1 clock appears.

WAVE FORMS



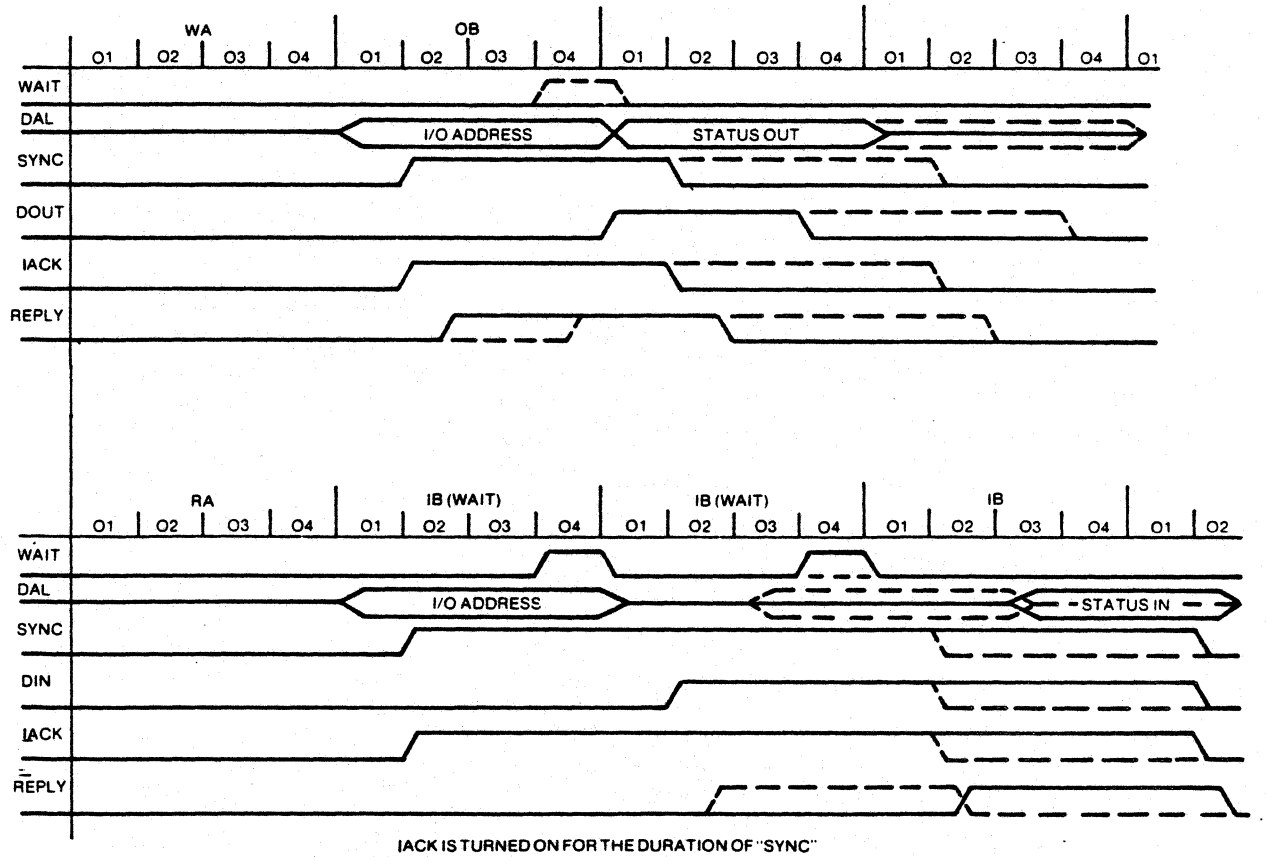
1. "SYNC" IS MADE HIGH AS SOON AS A VALID ADDRESS IS ON THE BUS (02)
2. "REPLY" BEING LOW ON 03 CAUSES THE OUTPUT SEQUENCE TO BE REPEATED
3. "DOUT" IS MADE HIGH ON 01 AS "DATA OUT" IS PLACED ON THE BUS
4. "OUTPUT" OPERATION IS TERMINATED BY RAISING "REPLY" BEFORE 03
5. "SYNC" IS MADE LOW ON 02, "DOUT" IS MADE LOW ON 04, AND "DAL-- IS TRI-STATED ON 01. REPLY CAN BE TURNED OFF AS SOON AS "SYNC" IS MADE LOW.

WRITE/OUTPUT SEQUENCE



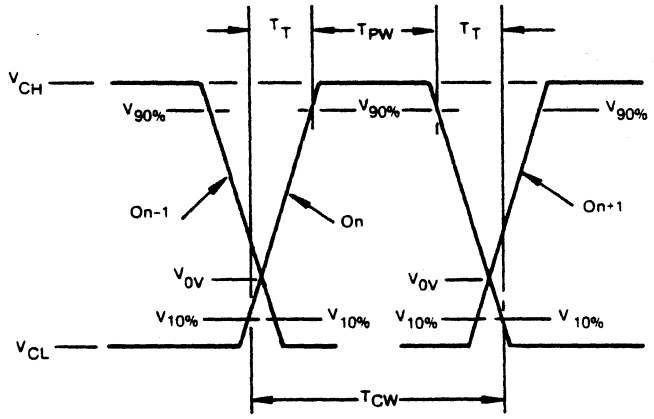
1. "SYNC" IS MADE HIGH AS SOON AS A VALID ADDRESS IS ON THE BUS (02)
2. "REPLY" BEING LOW ON 03 CAUSES THE INPUT SEQUENCE TO BE REPEATED
3. "DIN-- IS MADE HIGH AS SOON AS THE ADDRESS IS TAKEN OFF THE BUS (02) AS FUNCTION OF READ MICROINSTRUCTION
4. "REPLY" AND "DIN" MUST BE HIGH ON 03 IN ORDER FOR "INPUT" OPERATION TO TAKE PLACE
5. UPON TERMINATION OF "INPUT" SEQUENCE, "SYNC" AND "DIN" ARE MADE LOW ON 02

READ/INPUT SEQUENCE



IACK IS TURNED ON FOR THE DURATION OF "SYNC"

INTERRUPT ACKNOWLEDGE SEQUENCE



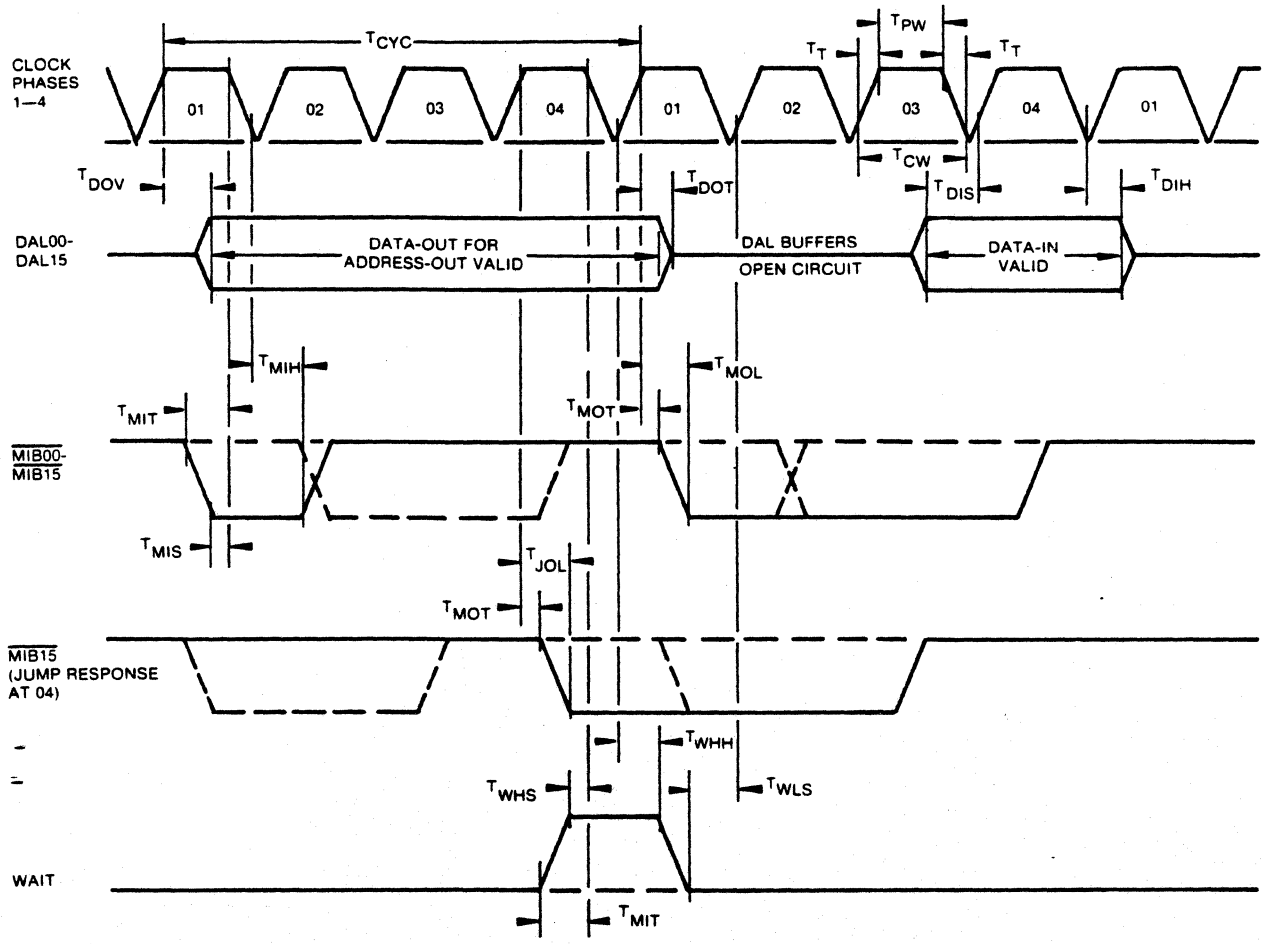
DEFINITION OF 10% AND 90% VOLTAGE POINTS FOR CLOCK, INPUTS AND OUTPUTS

$$V_{10\%} = V_{LOW\ (MAX)} + 0.1\ [V_{HIGH\ (MIN)} - V_{LOW\ (MAX)}]$$

$$V_{90\%} = V_{LOW\ (MAX)} + 0.9\ [V_{HIGH(MIN)} - V_{LOW\ (MAX)}]$$

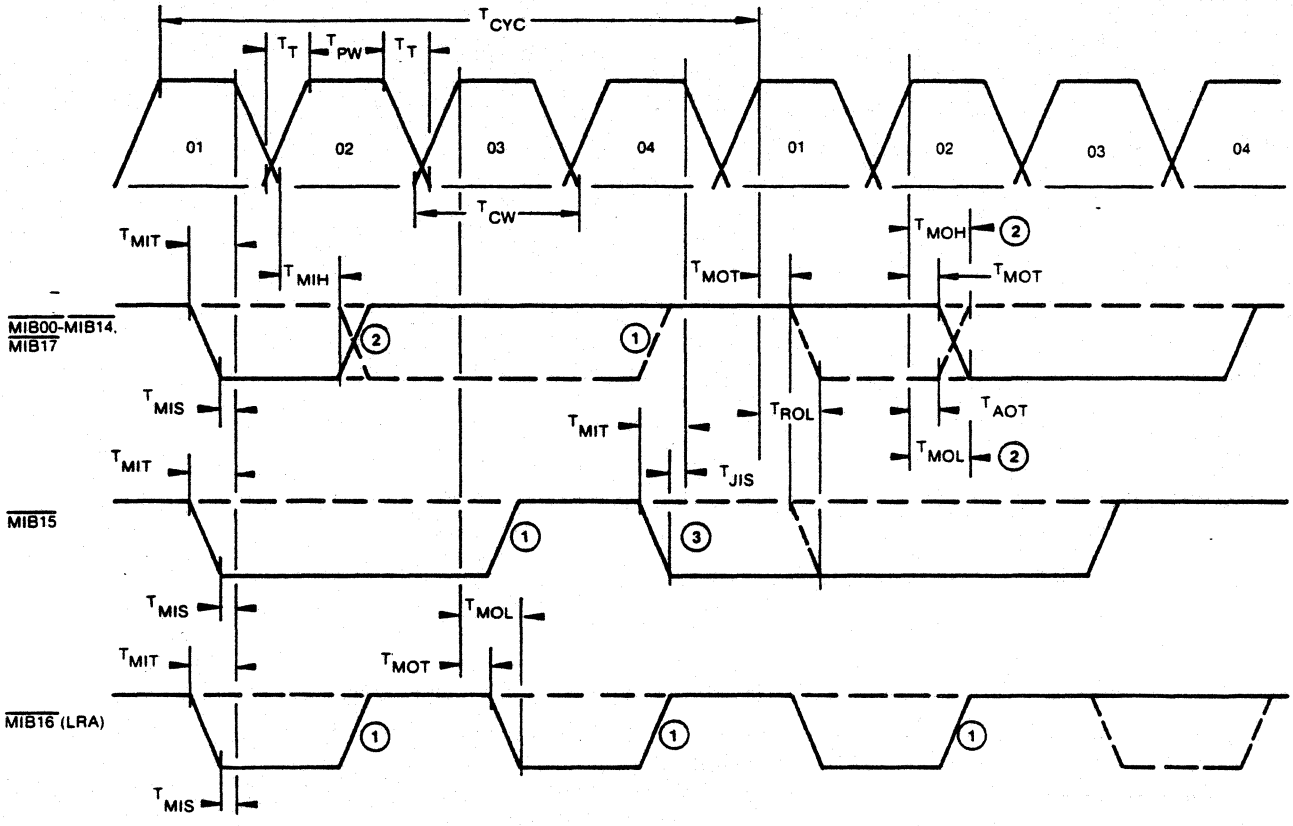
THIS DEFINITION APPLIES TO CLOCK, INPUT AND OUTPUT PINS

WD9000 CLOCK DIAGRAM



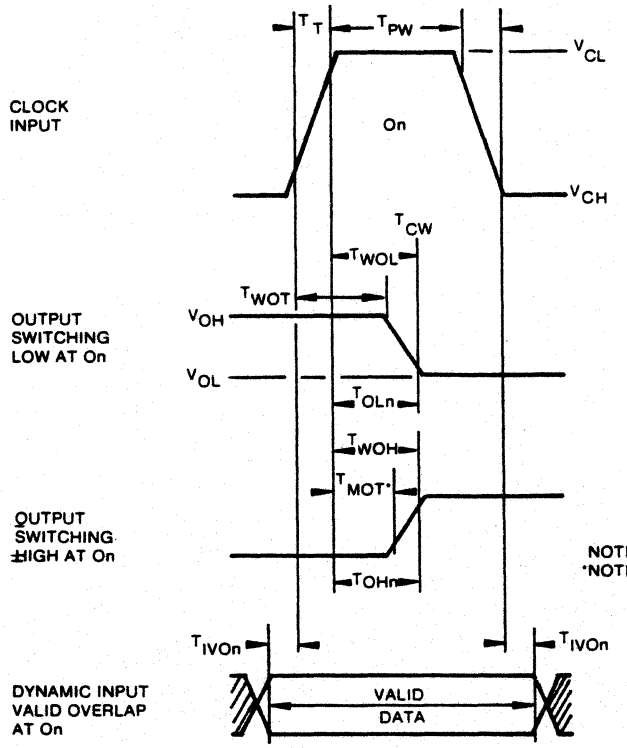
NOTE: SWITCHING TIMES ARE MEASURED AT 10% AND 90% OF SPECIFIED LEVELS

DATA CHIP INTERFACE TIMING



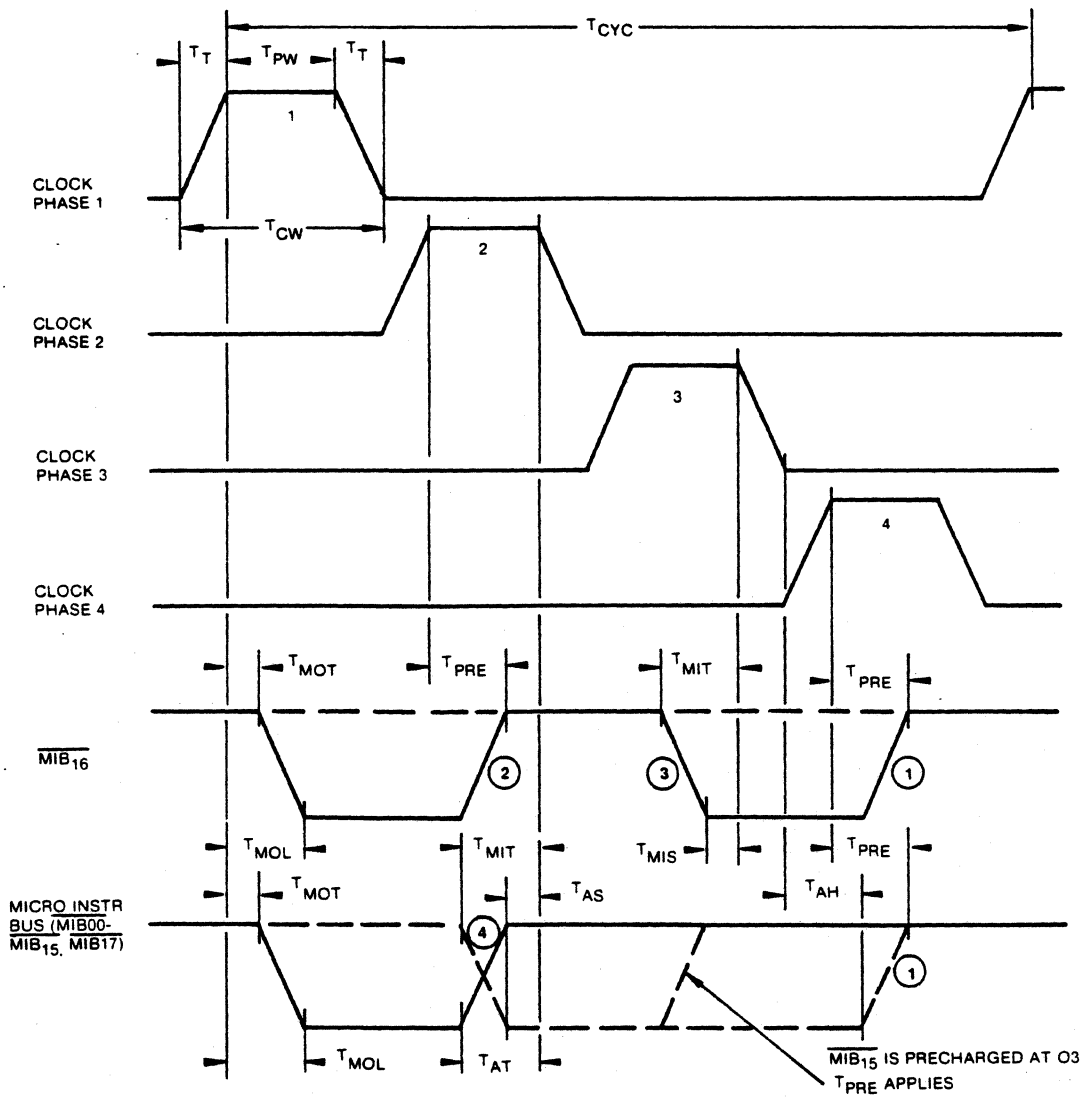
NOTES:
1. BUS PRECHARGING IS PERFORMED BY THE MICROM
2. ADDRESS OUTPUT SWITCHING TIME (TMOH AND TMOL) APPLIES TO $\overline{MIB00}$-$\overline{MIB10}$ ONLY
3. JUMP RESPONSE FROM DATA CHIP
4. SWITCHING TIMES ARE MEASURED AT 10% AND 90% OF SPECIFIED LEVELS

MICROM MICRO INSTRUCTION BUS



NOTE: SWITCHNG TIMES ARE MEASURED AT 10% AT 90% OF SPECIFIED LEVELS
*NOTE: T_{MOT} ONLY APPLIES TO THE WAIT SIGNAL IN THESE DRAWINGS

CONTROL SIGNALS TIMING



NOTES:
1. $\overline{MIB}$ LINES EXCEPT $\overline{MIB15}$ ARE PRECHARGED HIGH AT PHASE 4
2. $\overline{MIB16}$ IS ALSO PRECHARGED HIGH AT PHASE 2
3. $\overline{MIB16}$ IS DISCHARGED TO DISABLE THE $\overline{MIB00}$-$\overline{MIB15}$ AND $\overline{MIB18}$-$\overline{MIB21}$ OUTPUTS AT PHASE 1 FROM DISCHARGING LOW
4. ADDRESS INPUT TRANSITIONS OCCUR ONLY ON $\overline{MIB00}$-$\overline{MIB10}$ LINES AND CHIP SELECT
5. SWITCHING TIMES ARE MEASURED AT 10% AND 90% OF SPECIFIED LEVELS

MICROM TIMING DIAGRAM

Pascal MICROENGINE™ Instruction Set Format

Instructions are one byte long, followed by zero to four parameters. Most parameters specify one word of information, and are one of five basic types.

UB Unsigned byte: high order byte of parameter is implicitly zero.

SB Signed byte: high order byte is sign extension of bit 7.

DB Don't care byte: can be treated as SB or UB, as value is always in the range 0...127.

B Big: this parameter is one byte long when used to represent values in the range 0...127, and is two bytes long when representing values in the range 128...32767. If the first byte is in 0...127, the high byte of the parameter is implicitly zero. Otherwise, bit 7 of the first byte is cleared and it is used as the high order byte of the parameter. The second byte is used as the low order byte.

W Word: the next two bytes, low byte first, are the parameter value.

More detailed information on the Pascal MICROENGINE™ instructions (P-Code) is contained in the Pascal Operations Manual.

These mnemonics are intended only for further understanding of P-code. Neither the Microengine Company nor the University of California at San Diego provide P-code assembler software.

Mnemonic	Instruction Code	Parameters	Description
Constant One Word Loads			
SLDC	0...31		Short Load Word Constant (Value 0-31)
LDCN	152		Load Constant Nil
LDCB	128	UB	Load Constant Byte
LDCI	129	W	Load Constant Word
LCA	130	B	Load Constant Address
Local One Word Loads and Store			
SLDL1...16	32...47		Short Load Local Word
LDL	135	B	Load Local Word
LLA	132	B	Load Local Address
STL	164	B	Store Local
Global One Word Loads and Store			
SLDO1...16	48...63		Short Load Global Word
LDO	133	B	Load Global Word
LAO	134	B	Load Global Address
SRO	165	B	Store Global Word
Intermediate One-Word Loads and Store			
LOD	137	DB, B	Load Intermediate Word
LDA	136	DB, B	Load Intermediate Address
STR	166	DB, B	Store Intermediate Word
Indirect One-Word Loads and Store			
STO	196		Store Indirect
Extended One-Word Loads and Store			
LDE	154	UB, B	Load Word Extended
LAE	155	UB, B	Load Address Extended
STE	217	UB, B	Store Word Extended
Multiple Word Loads and Stores (Sets and Reals)			
LDC	131	B, UB	Load Multiple Word Constant
LDM	208	UB	Load Multiple Words
STM	142	UB	Store Multiple Words
Byte Arrays			
LDB	167		Load Byte
STB	200		Store Byte

Mnemonic	Instruction Code	Parameters	Description
Record and Array Indexing and Assignment			
MOV	197	B	Move Words
SIND0..7	120..127		Short Index and Load Word
IND	230	B	Static Index and Load Word
INC	231	B	Increment Field Pointer
IXA	215	B	Index Array
IXP	216	UB_1, UB_2	Index Packed Array
LDP	201		Load A Packed field
STP	202		Store Into A Packed Field
Logicals			
LAND	161		Logical And
LOR	160		Logical Or
LNOT	229		Logical Not
LEUSW	180		Compare Unsigned Word <=
GEUSW	181		Compare Unsigned Word >=
Integers			
ABI	224		Absolute Value of Integer
NGI	225		Negate Integer
ADI	162		Add Integers
SBI	163		Subtract Integers
MPI	140		Multiply Integers
DUP1	226		Copy Integer
DVI	141		Divide Integers
MODI	143		Modulo Integers
CHK	203		Check Against Subrange Bounds
EQUI	176		Compare Integer =
NEQI	177		Compare Integer <>
LEQI	178		Compare Integer <=
GEQI	179		Compare Integer >=
Reals (All Over/Underflows Cause a Run-Time Error)			
FLT	204		Float Top-of-Stack
TNC	190		Truncate Real
RND	191		Round Real
ABR	227		Absolute Value of Real
ADR	192		Add Reals
NGR	228		Negate Real
SBR	193		Subtract Reals
MPR	194		Multiply Reals
DUP2	198		Copy Real
DVR	195		Divide Reals
EQUREAL	205		Compare Real =
LEQREAL	206		Compare Real <=
GEQREAL	207		Compare Real >=
Sets			
ADJ	199	UB	Adjust Set
SRS	188		Build Subrange Set
INN	218		Set Membership
UNI	219		Set Union
INT	220		Set Intersection
DIF	221		Set Difference
EQUPWR	182		Set Compare =
LEQPWR	183		Set Compare <= (Subset of)
GEQPWR	184		Set Compare >= (Superset of)

Mnemonic	Instruction Code	Parameters	Description
Byte Arrays			
EQUBYT	185	B	Byte Array Compare =
LEQBYT	186	B	Byte Array Compare <=
GEQBYT	187	B	Byte Array Compare >=
Jumps			
UJP	138	SB	Unconditional Jump
FJP	212	SB	False Jump
EFJ	210	SB	Equal False Jump
NFJ	211	SB	Not Equal False Jump
UJPL	139	W	Unconditional Long Jump
FJPL	213	W	False Long Jump
XJP	214	B	Case Jump
Procedure and Function Calls and Returns			
CPL	144	UB	Call Local Procedure
CPG	145	UB	Call Global Procedure
CPI	146	DB, UB	Call Intermediate Procedure
CXL	147	UB_1, UB_2	Call Local External Procedure
CXG	148	UB_1, UB_2	Call Global External Procedure
CXI	149	UB_1, DB, UB_2	Call Intermediate External Procedure
CPF	151		Call Formal Procedure
RPU	150	B	Return From User Procedure
LSL	153	DB	Load Static Link Onto Stack
NOP	156		No Operation
SIGNAL	222		Signal
WAIT	223		Wait on Semaphore
LPR	157		Load Processor Register
SPR	209		Store Processor Register
BPT	158		Break Point
RBP	159		Return From Breakpoint
SWAP	189		Swap Top-of-Stack with Next to Top-of-Stack

ABSOLUTE MAXIMUM RATINGS OVER FREE AIR TEMPERATURE RANGE (Unless Otherwise Noted)*

Supply Voltage V_{DD} (See NOTE)	−0.5V to 15V
Supply Voltage V_{CC} (See NOTE)	−0.5V to 15V
Supply Voltage V_{BB} (See NOTE)	−10V to 1.0V
Clock Voltage (See NOTE)**	−1.0V to 15V
All Other Pin Voltages (See NOTE)	−1.0V to 15V
Operating Free Air Temperature Range	0°C to 125°C
Storage Temperature Range	−55°C to 125°C

NOTE: These voltage values are with respect to V_{SS} Supply Voltage. If V_{BB} is more positive than any other voltage, then I_{BB} must be limited to 10 ma.

*Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum-rating conditions for extended periods may affect device reliability.

**The other three clock voltages must be between 0.5V and −0.6V except for switching overlaps. Not more than one clock may be high at any one time.

Applying power to the part may be any sequence of conditions that do not violate the maximum ratings specified on this sheet.

OPERATING CHARACTERISTICS

T_{CASE} = 0°C to 70°C, V_{DD} = +12.0 ± .6V, V_{BB} −3.9 ± .25V, V_{SS} = 0V, V_{CC} = +5V ± .25V

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	COMMENTS AND CONDITIONS
I_L	Leakage Current for any Pin Other than Clock or Power			±10	μA	V_{IN} = 5.25V/0V
I_{BB}	V_{BB} Supply Current			−500	μA	V_{BB} = −5.25V
I_{LC}	Clock Leakage Current			±100	μA	V_{CLOCK} = 13.7V/0V
$I_{CC_{AVE}}$	Average V_{CC} Operating Current*		10.0	20.0	mA	T_{CYC} = 300 nsec C_L = 25 pf
$I_{DD_{AVE}}$	Average V_{DD} Operating Current		10.0	20.0	mA	T_{CYC} = 300 nsec C_L = 50 pf
V_{IHM}	Input High Voltage (All Inputs)	4.0	V_{CC}	V		
V_{ILM}	Input Low Voltage (All Inputs)	0.0	0.8	V		
V_{OHM}	Output High Voltage (MOS)	4.35	V_{CC}	V	I_O = −30 μA	
V_{OHT}	Output High Voltage (TTL)	2.4	V_{CC}	V	I_O = −50 μA	
V_{OLM}	Output Low Voltage (MOS)	V_{SS}	0.4	V	I_O = 100 μA	
V_{OLT}	Output Low Voltage (TTL)	0.0	0.4	V	I_O = 1.8 ma	
V_{OV}	Overlap Voltage of Any Two Adjacent Clock Phases	0.0	3.0	V		
V_{CH}	Clock High Voltage (SEE NOTE)	11.8 12.0	13.0 13.7	V	V_{DD} = 11.4 V_{DD} = 12.6	
V_{CL}	Clock Low Voltage (SEE NOTE)	−0.6	0.5	V		

NOTE: Linear interpolation applies for V_{CH} when V_{DD} is between 11.4V and 12.6V. No overshoot or undershoot allowable.

*Note: The majority of this current is used to precharge the output capacitance, C_L; and therefore, is proportional to the C_L precharged by the MICROM and the frequency of discharge.

AC CHARACTERISTICS

T_{CASE} = 0°C to 70°C, V_{DD} = +12V ± .6V, V_{BB} = −3.9V ± .25V, V_{SS} = 0V, V_{CC} = +5.0V ± 0.25V

SYMBOL	CHARACTERISTICS	MIN	TYP	MAX	UNITS	CONDITIONS
T_{PW}	Clock Width High (All Phases)	55		240	nsec	
T_{CW}	Clock Width Low (All Phases)	75		300	nsec	
T_T	Clock Transition Time (All Phases)	5			nsec	
T_{CYC}	Clock Period (All Phases)	300		1000	nsec	
T_{MOL}	Output Propagation Delay from Ø1 Clock			35	nsec	C_L = 50 pf
T_{PRE}	Time to Precharge Outputs High			55	nsec	C_L = 25 pf
T_{MIS}	Input Set-Up Time on $\overline{MIB16}$ at Phase 3	20			nsec	
T_{TOL}	TTL Out Switching Low			55	nsec	
T_{AS}	Address Set-Up Time	5			nsec	
T_{AH}	Address Hold Time	0			nsec	
T_{MOT}	Output Transition Start Delay Time			20	nsec	C_L = 50 pf
T_{MIT}	Input Transition Start Set-Up Time	35			nsec	
T_{AT}	Address Transition Start Set-Up Time	25			nsec	

CAPACITANCE

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$C_{\phi 1}$	Clock Phase 1 Capacitance		20	50	pf	V_{IN} = OV
$C_{\phi 2}$	Clock Phase 2 Capacitance		40	60	pf	V_{SS} = OV,
$C_{\phi 3}$	Clock Phase 3 Capacitance		20	50	pf	V_{DD} = C
$C_{\phi 4}$	Clock Phase 4 Capacitance		50	100	pf	V_{BB} = −3.9V
C_b	Data Input/Output Pin Capacitance		5.0	8.0	pf	f = 1 MHz
C_c	Clock to Clock Capacitance		3.0	6.0	pf	

RELATED PRODUCTS

MICROENGINE™ company products include:

- WD900 Pascal MICROENGINE™ Single Board Computer — MICROENGINE™ CPU, 64K Bytes of RAM, 2 Parallel Ports (110-19.2K Band), 2 Serial Ports, Floppy (Single or Double Density, Standard or Mini) Disk Controller with DMA.
- WD90 — Pascal MICROENGINE™ Computer — Pascal MICROENGINE™ Single Board Enclosed in Low Profile Housing With Power Supply.

Western Digital Corporation supplies other components useful in designing systems based on the Pascal MICROENGINE™. These include:

- FD1700 Series Floppy Controllers. — For mini and standard floppy diskettes, single and double densities, IBM and non-IBM compatible. Also, Z80/8080 bus-compatible versions.
- DM1883 Direct Memory Access Controller.
- WD 2143 System Clock for MICROENGINE™ Chip Set.
- Communication products including UART, PSAT/PSAR, ASTRO/USART, BOART, SDLC, and Data Encryption.

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

The MICROENGINE Company is a wholly-owned subsidiary of Western Digital Corporation

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