OEM MANUAL

IBM PC TO QIC-36 INTERFACE

PC-36 TAPE DRIVE CONTROLLER

wangtek

PC-36 CONTROLLER OEM MANUAL

Part Number 20593-001

NOTICE

This document is intended to provide the user with detailed information adequate for the efficient installation, operation, and service of the equipment involved.

However, while every effort has been made to keep the information contained herein current and accurate as of the date of publication, no guarantee is given or implied as to its accuracy. Wangtek reserves the right to make changes, for the purpose of product improvement, at any time.

WANGTEK, INC.
41 Moreland Road
Simi Valley, CA 93065
Telex 650450

(818) 704-7113
TWX 910-494-1926

(805) 583-5255
FAX 805-522-1576

DECEMBER 1986

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OPERATING AND SERVICE MANUAL NO. 63149-001 Rev. 1

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FORWARD

This manual provides operating and service information for the PC-36, Manufactured by Wangtek Incorporated, 41 Moreland Road, Simi Valley, California.

The content includes a detailed product description, specifications, installation and operation instructions. Also included are theory of operation, maintenance, troubleshooting, and parts removal and replacement instructions.

TECHNICAL SUPPORT

If for any reason you require product technical support, please contact the OEM or Distributor where you first purchased your equipment. If they cannot help you or at their direction, Wangtek Technical Support can be reached at:

WANGTEK Incorporated
41 Moreland Road
Simi Valley, CA. 93065

(805) 583-5255
Telex 650450
FAX (805) 583-8249

WANGTEK-Europe
Unit 1A, Apollo House
Calleva Industrial Park
Aldermaston, Reading
RG7 4QW England
44-7356-77746
Telex 851-848135
FAX 44-7356-6076

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This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause interference to radio communications. It has been tested and found to comply with the limits for Class B computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial or residential environment. This equipment is a Class B digital apparatus which complies with the Radio Interference Regulations, CRC c.1374.

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1.0 INTRODUCTION

The purpose of this document is to provide a functional description of the Wangtek PC-36 Controller, detailing specific host commands implemented in the manner in which the tape drive is controlled, monitored, the method of the status and error reporting to the host, and the diagnostic capabilities of the controller.

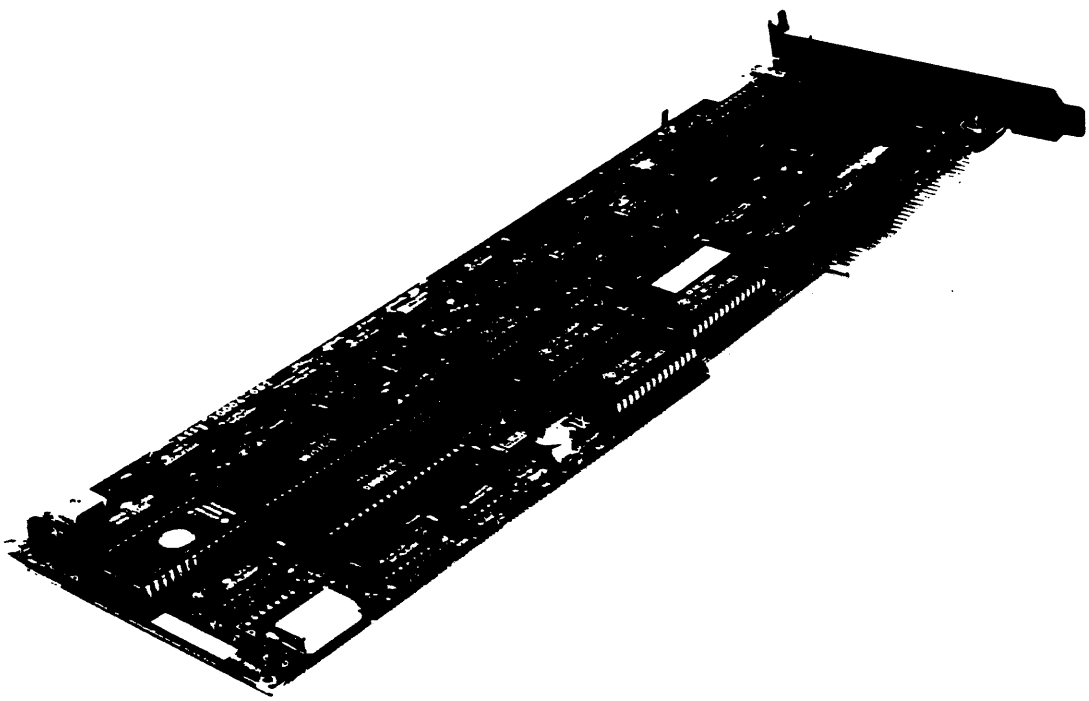
The Wangtek PC-36 Controller is designed to interface with the Wangtek Series 5000E and the Wangtek Series 5125E Basic Drives via the QIC-36 basic streaming tape drive interface. The Series 5000E interface signals are described in Section 4.4.4 and the Series 5125E interface signals are described in Appendix "A". The controller provides for the implementation of standard set of QIC-02 defined streaming commands with the IBM PC interface. However, most of the functional characteristics of the controller are under firmware control; therefore, other optional commands can be implemented by simply upgrading the firmware.

2.0 DEFINITIONS

The following is a definition of the terminology used throughout this document for further reference.

block	A group of 512 consecutive bytes of data which are transferred as a unit.
BOM	Beginning of Media, the start of recordable area of tape on the initial track (Track 0).
BOT	Beginning of Tape, a marker indicating the beginning of tape.
cartridge	Refer to ANSI Specification X3.55-1982.
command	The instruction byte which specifies the operation to be performed.
continuable	Any error after which an operation can be continued by issuing another command.
device	The controller as described herein.
drive	A device used to store and recover data onto and from magnetic tape.
EOT	End of Tape, the marker indicating the end of tape.
erase	To remove magnetically recorded data from the tape.
EW	Early Warning, a marker indicating the approaching end of the permissable recording area.

FIGURE 1.0 PC-36 CONTROLLER



exception condition	Any condition which prevents the performance of a potential command or the continuance of the current operation.
fatal	An error which causes an operation to be aborted and requires that operation to be started over.
file mark	A magnetically recorded identification mark.
host	An IBM PC, PC XT or PC AT interfaced to the controller.
LP	Load Point, a marker indicating the beginning of the permissable recording area.
search	A Read operation that logically repositions the tape and does not transfer data to the controller.
status	Bytes transmitted indicating the current condition of a device.
streaming drive	A tape drive that is designed to maintain continuous tape motion without the requirement to start and stop within an inter-record gap. If tape motion is interrupted for any reason, the drive must re-position the tape by moving far enough in the reverse direction to allow the tape to be brought up to speed in the forward direction before it reaches the point at which the preceding operation was terminated.
underrun	A condition developed when the controller transmits or receives data at a rate less than that required by the device to maintain streaming operation.

3.0 SPECIFICATION SUMMARY

Table 1.0 lists specification summary of the PC-36 Controller.

TABLE 1.0 SPECIFICATION SUMMARY

CHARACTERISTIC	TYPE/VALUE
Host Interface	IBM PC (Technical Reference 6025005, 6936808)
Drive Interface	QIC-36 Standard Interface
Data Interchange Format	QIC-24 Standard for Data Interchange or QIC-11 (Archive 8")
Tape Drives Controlled	Four (4) maximum
Transfer Rate	90 Kbytes per second
Recording Tracks/Format	9 track serpentine
Recording Code	(0,2) Run length limited (GCR encoding)
Data Buffering	Three (3) x 512-byte blocks, or 15 x 512-byte blocks (optional)
Write Re-tries	16 maximum
Read Re-tries	16 maximum
Error Detection	CRC (standard)
Soft Error Rate (Read)	1 in 10^8 bits
Hard Error Rate (Read)	1 in 10^{10} bits
MTBF	25,000 power-on hours
MTTR	Less than 30 minutes
Temperature	
Operating	+5°C to 45°C (+41° to +113°F)
Non-Operating	-30°C to +60°C (-22° to +140°F)
Relative Humidity	20 to 80% non-condensing
EMI	Compliance with FCC class B
Power Requirements	+12 VDC @ 0.2 amps +5 VDC @ 2.0 amps
Power Dissipation	12.5 Watts
Physical Characteristics:	
Width (inches/cm)	13.5/34.29
Height (inches/cm)	4.2/10.67
Weight	0.6 pounds

NOTE: In general, the PC-36 controller shall meet the IBM PC operating environment specification.

4.0 INTERFACE

This section defines the electrical interface between the PC-36 controller and the host computer, the basic streaming tape drive interface and the controller power requirements. The controller is contained on a single 13.5" X 4.2" board. Connectors are provided for the host and drive. The board is designed to mount in a full length expansion slot in an IBM PC, XT or AT.

4.1 INPUT POWER

The input power for the controller is provided from the host through the J1 I/O connector.

4.2 CONTROLLER POWER REQUIREMENTS

The voltages and currents required to operate the Controller are shown in Table 2.0 along with the applicable pin numbers of the J1 I/O connector.

TABLE 2.0 CONTROLLER POWER REQUIREMENTS

PIN NUMBER	PIN NAME	VOLTAGE MINIMUM	VOLTAGE MAXIMUM	CURRENT OPER.	COMMENTS REFERENCE NOTES
B9	V12+	11.6	12.4	0.2A	+12VDC (See Note 2)
B1, 10, 31	GND				+5VDC/+12VDC Return
B3, 29	V5+	4.85	5.25	2.0A	+5VDC (See Note 2)

NOTE 1. Must be tied together and to ground at one point in power supply.
NOTE 2. All voltages measured at J1 I/O connector.

4.3 HOST INTERFACE

The host computer interface to the controller is via card edge connector J1 to the 62-pin host computer bus. The board utilizes one of the long slots in the card cage. Operational parameters required to interface with the controller are described in Section 5.1.

4.3.1 Host Interface Signal Levels

All signals to the host are standard Tri-State TTL levels as follows:

False = High = 2.4 to 5.25 VDC
True = Low = 0 to 0.8 VDC
Off = High impedance state

Voltages shall be measured at the controller connector.

4.3.2 Signal Loading

Signals from the host to the controller are loaded by not more than 2.0ma. Command, address, DMA and interrupt request lines drive into not more than two PAL1628A inputs. The data lines drive into a single LS245 input.

4.3.3 I/O Channel

The I/O channel is an extension of the 8088 microprocessor bus. It is, however, demultiplexed, repowered, and enhanced by the addition of interrupts and direct memory access (DMA) functions.

The I/O channel contains an 8-bit, bi-directional data bus, 20 address lines, 6 levels of interrupt, control lines for memory and I/O read or write, clock and timing lines, 3 channels of DMA control lines, memory refresh timing control lines, a channel-check line, and power and ground for the adapters. Four voltage levels are provided for I/O cards: +5 Vdc, -5 Vdc, +12 Vdc, and -12 Vdc. These functions are provided in a 62-pin connector with 100-mil card tab spacing.

For additional information refer to IBM PC Technical Reference Manual.

4.3.4 I/O Channel Description

The following is a description of the IBM Personal Computer XT I/O Channel. All lines are TTL-compatible. Signal pinouts are shown in Table 3.0. IBM PC I/O channel signal orientation is shown in Figure 2.0.

SIGNAL	I/O	DESCRIPTION
OSC	O	Oscillator: High-speed clock with a 70-ns period (14.31818 MHz). It has a 50% duty cycle.

SIGNAL	I/O	DESCRIPTION
CLK	O	System clock: It is a divide-by-three of the oscillator and has a period of 210 ns (4.77 MHz). The clock has a 33% duty cycle.
RESET DRV	O	This line is used to reset or initialize system logic upon power-up or during a low line voltage outage. This signal is synchronized to the falling edge of clock and is active high.
A0-A19	O	Address bits 0 to 19: These lines are used to address memory and I/O devices within the system. The 20 address lines allow access of up to 1 megabyte of memory. A0 is the least significant bit (LSB) and A19 is the most significant bit (MSB). These lines are generated by either the processor or DMA controller. They are active high.
D0-D7	I/O	Data Bits 0 to 7: These lines provide data bus bits 0 to 7 for the processor, memory, and I/O devices. D0 is the least significant bit (MSB). These lines are active high.
ALE	O	Address Latch Enable: This line is provided by the 8288 Bus Controller and is used on the system board to latch valid addresses from the processor. It is available to the I/O channel as an indicator of a valid processor address (when used with AEN). Processor addresses are latched with the failing edge of ALE.
I/O CH CK*	I	-I/O Channel Check: This line provides the processor with parity (error) information on memory or devices in the I/O channel. When this signal is active low, a parity error is indicated.

SIGNAL	I/O	DESCRIPTION
I/O CH RDY	I	I/O Channel Ready: This line, normally high (ready), is pulled low (not ready) by a memory or I/O device to lengthen I/O or memory cycles. It allows slower devices to attach to the I/O channel with a minimum of difficulty. Any slow device using this line should drive it low immediately upon detecting a valid address and a read or write command. This line should never be held low longer than 10 clock cycles. Machine cycles (I/O or memory) are extended by an integral number of CLK cycles (210 ns).
IRQ2-IRQ7	I	Interrupt Request 2 to 7: These lines are used to signal the processor that an I/O device requires attention. They are prioritized with IRQ2 as the highest priority and IRQ7 as the lowest. An Interrupt Request is generated by raising an IRQ line (low to high) and holding it high until it is ackowledged by the processor (interrupt service routine).
IOR*	O	-I/O Read Command: This command line instructs an I/O device to drive its data onto the data bus. It may be driven by the processor or the DMA controller. This signal is active low.
IOW*	O	-I/O Write Command: This command line instructs an I/O device to read the data on the data bus. It may be driven by the processor or the DMA controller. This signal is active low.
MEMR*	O	Memory Read Command: This command line instructs the memory to drive its data onto the data bus. It may be driven by the processor or the DMA controller. This signal is active low.
MEMW*	O	Memory Write Command: This command line instructs the memory to store the data present on the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

SIGNAL	I/O	DESCRIPTION
DRQ1-DRQ3	I	DMA Request 1 to 3: These lines are asynchronous channel requests used by peripheral devices to gain DMA service. They are prioritized with DRQ3 being the lowest and DRQ1 being the highest. A request is generated by bringing a DRQ line to an active level (high). A DRQ line must be held high until the corresponding DACK line goes active.
DACK0*-DACK3*	O	-DMA Acknowledge 0 to 3: These lines are used to acknowledge DMA requests (DRQ1-DRQ3) and to refresh system dynamic memory (DACK0). They are active low.
AEN	O	Address Enable: This line is used to de-gate the processor and other devices from the I/O channel to allow DMA transfers to take place. When this line is active (high), the DMA controller has control of the address bus, data bus, read command lines (memory and I/O), and the write command lines (memory and I/O).
T/C	O	Terminal Count: This line provides a pulse when the terminal count for any DMA channel is reached. This signal is active high.
CARD SLCTD*	I	-Card Selected: This line is activated by cards in expansion slot J8. It signals the system board that the card has been selected and that appropriate drivers on the system board should be directed to either read from, or write to, expansion slot J8. Connectors J1 through J8 are tied together at this pin, but the system board does not use their signal. This line should be driven by an open collector device.

The following voltages are available on the system board I/O channel:

+5 Vdc ±5%, located on 2 connector pins (B3, B29)
-5 Vdc ±10%, located on 1 connector pin (B5)
+12 Vdc ±5%, located on 1 connector pin (B9)
-12 Vdc ±10%, located on 1 connector pin (B7)
GND (Ground), located on 3 connector pins (B1, B10, B31)

TABLE 3.0. SIGNAL PINOUTS

J1 Pin #	Name	Signal Description
A1	I/O CH CK*	I/O Channel Check
A2	D7	
A3	D6	
A4	D5	
A5	D4	Data Bits 0 to 7
A6	D3	
A7	D2	D0 = LSB
A8	D1	D7 = MSB
A9	D0	
A10	I/O CH RDY	I/O Channel Ready
A11	AEN	Address Enable
A12	A19	
A13	A18	
A14	A17	
A15	A16	
A16	A15	
A17	A14	
A18	A13	
A19	A12	Address Bits 0-19
A20	A11	
A21	A10	A0 = LSB
A22	A9	A19 = MSB
A23	A8	
A24	A7	
A25	A6	
A26	A5	
A27	A4	
A28	A3	
A29	A2	
A30	A1	
A31	A0	
B1	GND	Ground
B2	RESET DRIVE	Reset or Initialize
B3	+5V DC	
B4	IRQ2	Interrupt Request #2
B5	-5V DC	
B6	DRQ2	DMA Request #2
B7	-12V DC	
B8	CAND SELECT*	Card Selected
B9	+12V DC	

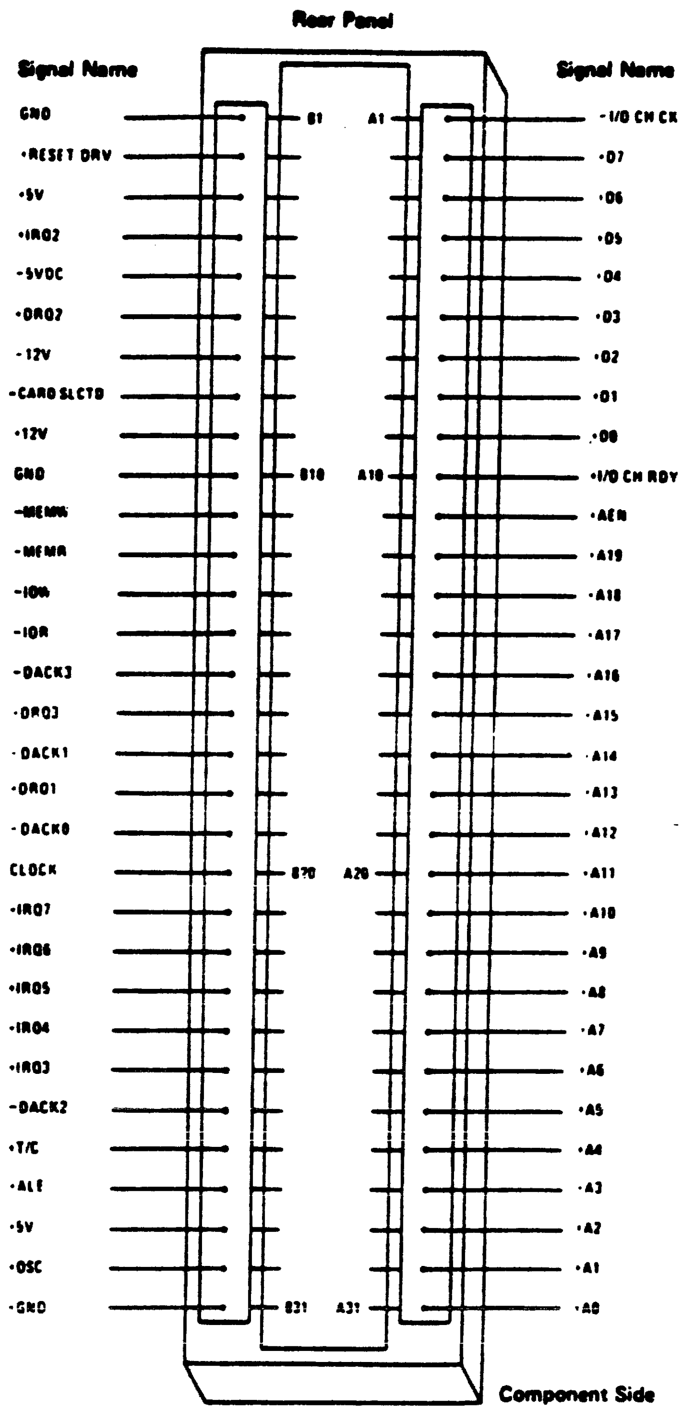
*Negative True

TABLE 3.0. SIGNAL PINOUTS
(Continued)

J1 Pin #	Name	Signal Description
B10	GND	Ground
B11	MEMU*	Memory Write Command
B12	MEMR*	Memory Read Command
B13	IOW*	I/O Write Command
B14	IOR*	I/O Read Command
B15	DACK 3*	DMA Acknowledge #3
B16	DRQ 3	DMA Request #3
B17	DACK 1*	DMA Acknowledge #1
B18	DRQ 1	DMA Request #1
B19	DACK 0*	DMA Acknowledge #0
B20	CLOCK	System Clock
B21	IRQ7	
B22	IRQ6	
B23	IRQ5	Interrupt Request 3 to 7
B24	IRQ4	
B25	IRQ3	
B26	DACK 2*	DMA Acknowledge #2
B27	TIC	Terminal Count
B28	ALE	Address Latch Enable
B29	+5VDC	
B30	OSC	Oscillator=High-Speed Clock
B31	GND	Ground

*Negative True

FIGURE 2.0 IBM PC I/O CHANNEL SIGNAL ORIENTATION



4.4 TAPE DRIVE INTERFACE

The interface of the PC-36 controller to the tape drive is accomplished via card edge connector J2 on the controller board. A 50-wire ribbon cable with 3M-type 3415-0001 connector (or equivalent) or a 62-pin D-Series connector AMP P/N 211139-1 (or equivalent) is required for connection between the controller and the tape drive. The maximum cable length is 3 meters.

4.4.1 Interface Signal Levels

All interface signals between the basic tape drive and the PC-36 controller are TTL logic levels as defined below:

SIGNAL TRUE = LOGIC 1 (low) 0.00 to 0.55 VDC

SIGNAL FALSE = LOGIC 0 (high) 2.40 to 5.25 VDC

4.4.2 Signal Loading

All signals from the PC-36 controller to the tape drive are capable of driving one standard TTL load in addition to the signal terminator.

All signals from the tape drive to the controller must be capable of driving at least one standard TTL load (1.6ma) in addition to the 23ma required by the tape drive interface terminations. Refer to the following documents:

1) Model 5000E series 1/4" streaming cartridge tape drives OEM manual.

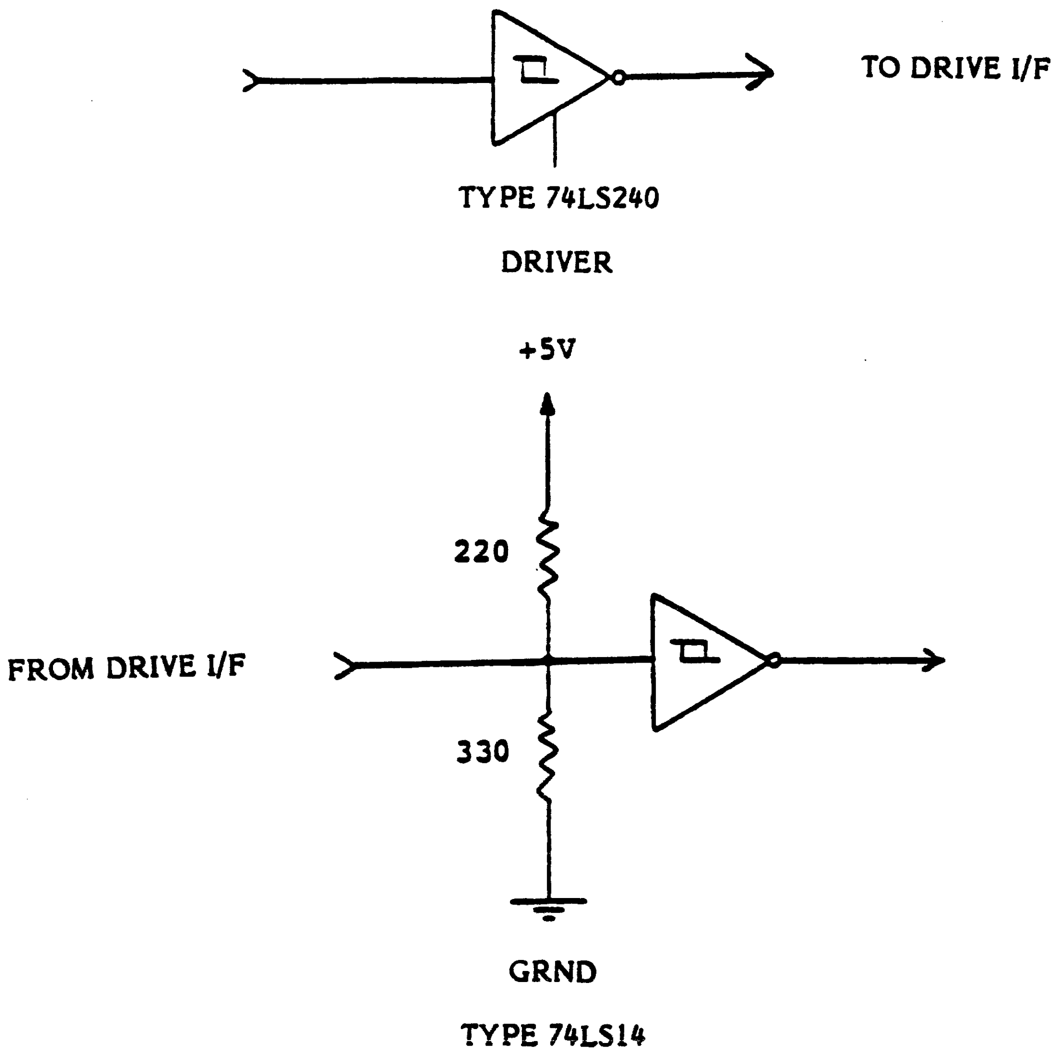
2) Operational Description Chapter 5 of this specification.

4.4.3 Drive Signal Terminations

All signals between the PC-36 controller and the tape drive should be terminated with 330 ohms to ground and 220 ohms to 5 Vdc.

Signal inputs to the controller are terminated at the controller. Signal outputs from the controller must be terminated in the tape drive; or in the last tape drive when more than one tape drive is daisy chained to the controller. Figure 3.4 shows the signal termination scheme.

FIGURE 3.0 INTERFACE SIGNAL TERMINATION



4.4.4 Tape Drive Interface Signal Descriptions

This section describes the electrical interface between the streaming cartridge tape drive and the PC-36 controller. The controller signal interface to the tape drive consists of three (3) basic signal groups. They include:

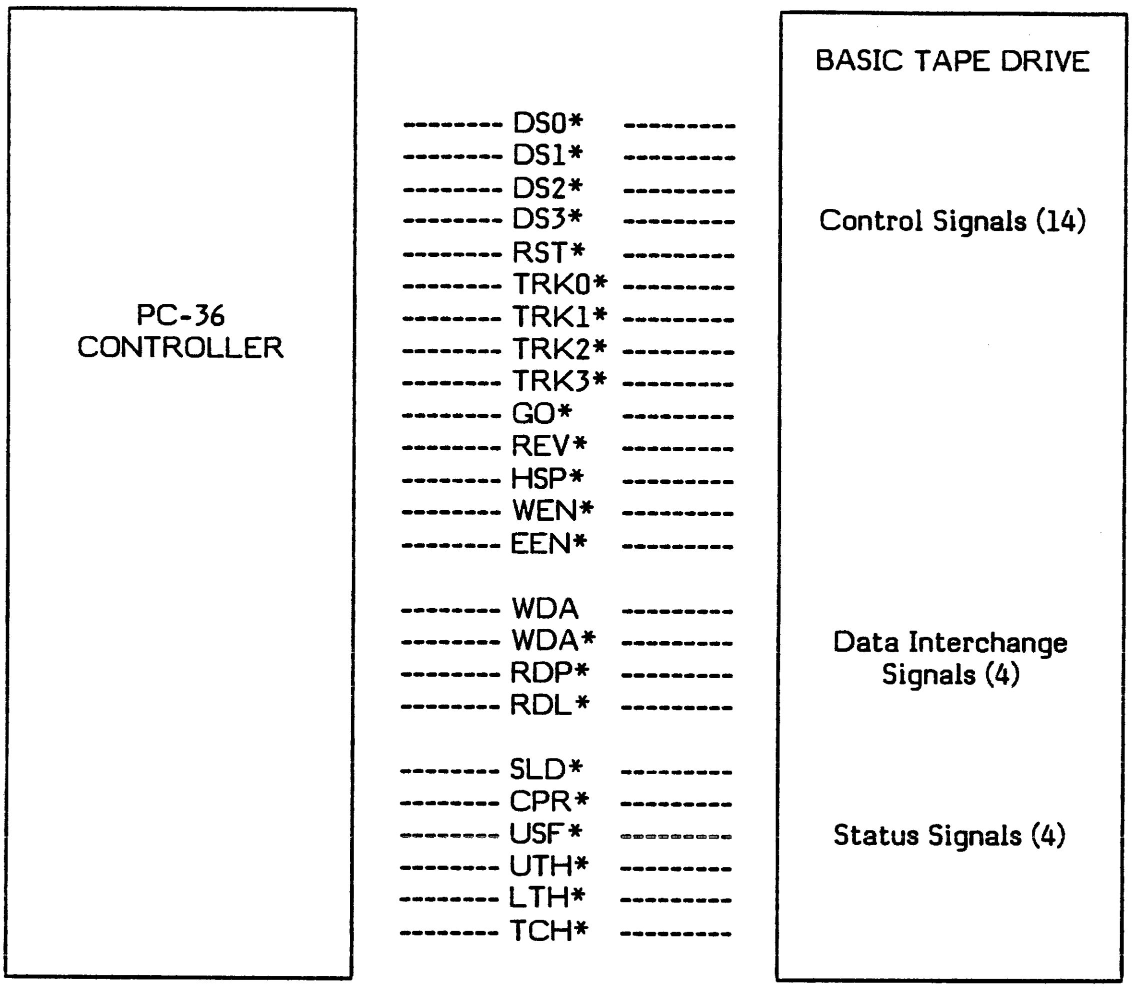
1. Tape Drive Control Signals
2. Tape Drive Status Signals
3. Data Interchange Signals

There are fourteen (14) tape drive control signals, four (4) data signal lines, and six (6) tape drive status output signals. Figure 3.2 identifies the tape drive/controller interface signals. This signal interface is pin and plug compatible with the QIC-36 interface standard.

For additional information of the drive, refer to Series 5000E OEM Manual, Wangtek P/N 200363-001.

FIGURE 4.0
TAPE DRIVE/CONTROLLER INTERFACE SIGNAL GROUPS

J2A or B



* Indicates low true.

TABLE 4.0 CONTROLLER/TAPE DRIVE INTERFACE SIGNALS

J2A Pin #	J2B Pin #	Name	Signal Description
02	1	GO*	Go Control for Capstan Motor
04	2	REV*	Direction Control for Capstan Motor
06	3	TR3*	Track Select Bit 3
08	4	TR2*	Track Select Bit 3
10	5	TR1*	Track Select Bit 3
12	6	TR0*	Track Select Bit 3
14	7	RST*	Reset
18	9	DS2*	Drive 2 Select Control (Not Used)
20	10	DS1*	Drive 1 Select Control
22	11	DS0*	Drive 0 Select Control
24	12	RDL*	Read Level Output-a digitized derivative of the Analog Output Signal
26	13	RDP*	Read Pulse Output - A Pulse per Flux Transition
28	14	UTH*	Upper Tape Position Code
30	15	LTH*	Lower Tape Position Code
32	16	SLD*	Selected Response from Selected Drive
34	17	CIN*	Cartridge In Place
36	18	USF*	Unsafe - Cartridge Safe plug is in the "unsafe" position (i.e., writing is enabled)
38	19	TCH*	Capstan Tachometer Pulses - each pulse Equals 0.145 $\pm$3% inches of tape movement
40	20	WDA-*	Write Data Signal
42	21	WDA+*	Inverse Write Data Signal
44	44	RES	Reserved
46	46	HSD*	High Speed Select Control
48	48	WEN*	Write Enable Control
50	50	EEN*	Erase Enable Control

NOTE: All pins not listed on each connector are signal grounds.

* Indicates low true.

4.4.4.1 Control Signals to Tape Drive

The QIC Controller signal outputs to the tape drive consist of the following signals:

SIGNAL	DESCRIPTION
RST*	RESET: This signal, when active low, initializes the tape drive and causes the magnetic recording head to go to the track position closest to the lower edge of tape.
DSO* thru DS2*	DRIVE SELECT 0 through 2: These signals are used to select any one of three tape drive units for operation. (DS2 is not used.)
GO*	GO: This signal, when active low, enables the tape drive motor if the tape drive is selected. Tape motion will not be enabled, however, if REV* is high and the tape is at the EOT (end-of-tape) position or if REV* is low and the tape is at the BOT (beginning-of-tape) position.
REV*	REVERSE: This signal output, when high, enables the tape to move from the beginning-of-tape to the end-of-tape; when low, tape movement is in the opposite direction.
TRK0* thru TRK3*	TRACK SELECT 0 through 3: These signals are binary-encoded track addressing outputs to the tape drive. These signals are used to position the recording head over logically adjacent tracks and enable writing and/or reading the selected track. Tracks 0 through 8 are valid address codes for 9-track drives.
WEN*	WRITE ENABLE: This signal, when active low, allows transitions on the write data inputs WDA/WDA* to be recorded on the selected track.
EEN*	ERASE ENABLE: This signal, when active low, causes the tape drive erase bar to be enabled. All tracks are simultaneously erased.

4.4.4.2 Status Signals From Tape Drive

The QIC Controller receives the following status inputs from the tape drive.

SIGNAL	DESCRIPTION
CPR*	CARTRIDGE:PRESENT: This signal input, when active low, indicates that a cartridge is inserted in the tape drive.
SLD*	SELECTED: This signal input, when active low, indicates the selected tape drive is powered up and ready for operation.
USF*	UNSAFE: This signal input, when active low, indicates that the installed tape cartridge is not write protected (cartridge not set to SAFE position).
UTH* and LTH*	UPPER TAPE HOLE and LOWER TAPE HOLE: This inputs to the QIC controller provides an indication of the current tape position as indicated below. These status signals are indicated below. These status signals are not valid upon initial insertion of tape cartridge until such time that the tape drive is reset or the tape is moved to the EOT or BOT positions.

UTH*	LTH*	Interpretation
L	L	Beginning-of-tape position.
L	H	Warning Zone (between load point and early warning hole and BOT)
H	H	In Recording Zone (between load point and early warning hole) if a BOT or EOT was detected since cartridge insertion; otherwise this code means "tape position unknown".
H	L	End-of-tape position.

SIGNAL	DESCRIPTION
TCH*	TACHOMETER: This signal is a pulse input to the QIC controller whose frequency is proportional to the speed of the tape drive motor. Each TCH* pulse represents a movement of approximately 0.14 ($\pm$8%) inches of tape past the magnetic recording head. This signal can be usd by the controller to determine the current tape speed, how much tape was used, or for other diagnostic purposes.

4.4.4.3 Data Signals

The data interchange signals consist of a pair of write data output lines and two (2) independent read data inputs to the tape drive. The data interchange signals are described below:

SIGNAL	DESCRIPTION
WDA- WDA+	WRITE DATA: These signals ae differential signal lines containing the information to be recorded on magnetic tape. Data appearing on these signal lines will only be recorded if the write enable (WEN*) signal line is active. Each change of state in the WDA-/WDA+ signal line recorded as a flux transition on tape.
RDP*	READ DATA PULSE: This signal input from the tape drive contains the data read from magnetic tape during either a read only or read-after-write operation. Each negative-going edge of the RDP* signal line represents a flux transition recorded on magnetic tape.
RDL*	READ DATA LEVEL: This signal input from the tape drive contains the data read from magnetic tape during a read-only or read-after-write operation. Each transition of the RDL* signal represents a flux transition recorded on magnetic tape. This signal is not used on the PC36 controller.

5.0 FUNCTIONAL DESCRIPTION

The PC-36 controller provides an interface between an IBM PC, XT or AT and a Series 5000E 1/4-inch cartridge streaming tape drive. Its input conforms to the IBM PC I/O channel requirements described by IBM Technical Reference 6025005. Its output is compatible with the QIC-36 interface, the industry standard basic streaming tape drive interface.

The PC-36 controller performs the function of an intelligent streaming tape controller. In the write mode, it accepts data from the host, formats it into blocks, appends CRC, GCR encodes the data and writes it to tape. The controller performs a read after write data check using the appended CRC to insure data integrity. In the read mode, the controller reads data from tape, GCR decodes the data, checks the CRC and sends the data to the host.

The PC-36 controller is microprocessor based. Therefore, most of its operating characteristics are a function of the firmware installed. Further information as to the format of the data blocks, tape format and the interpretation an execution of commands will be found in the subsequent sections.

As shown in Figure 5.0, the PC-36 controller consists of the following functional blocks.

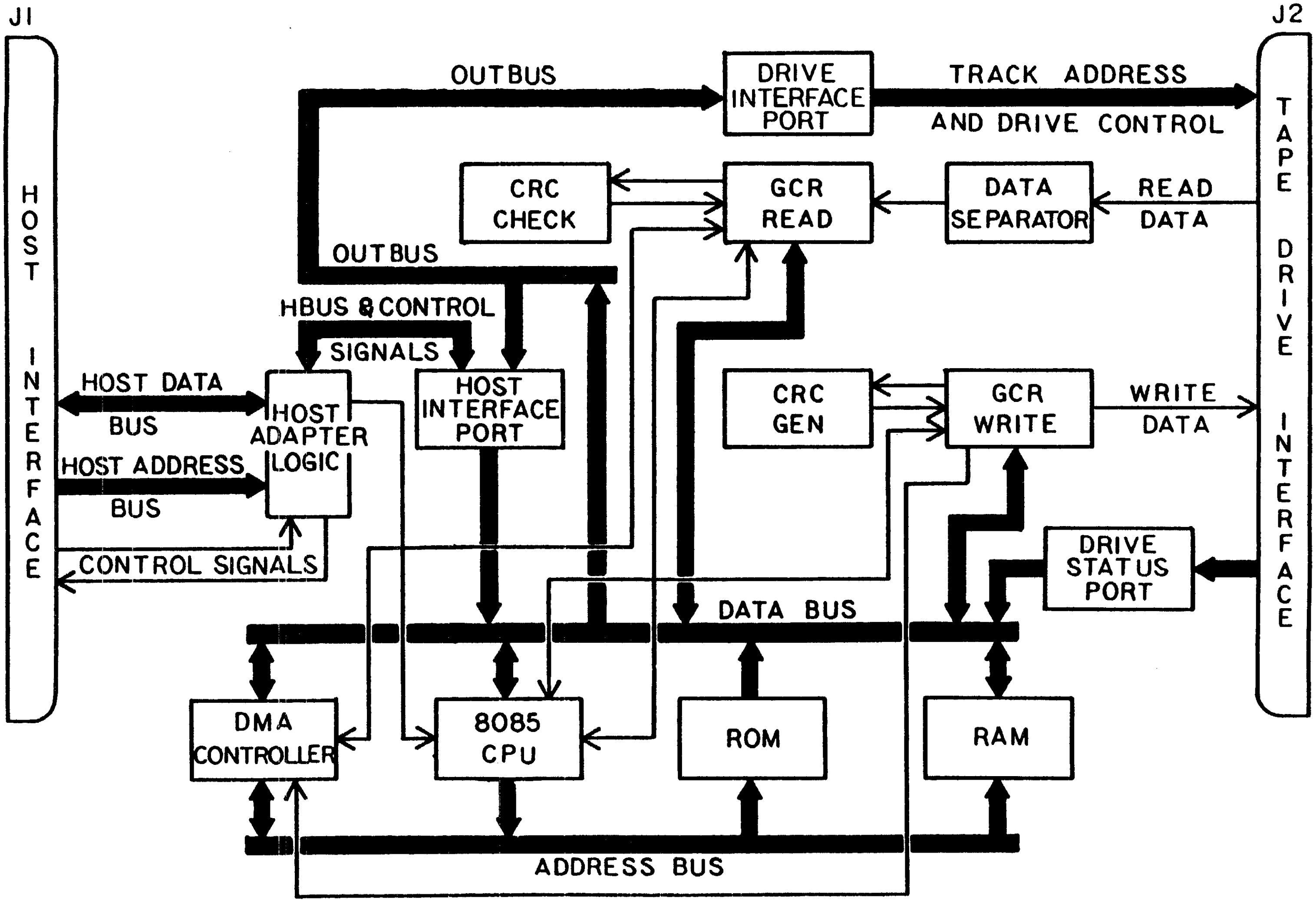
Host Interface
Basic Tape Drive Interface
Microprocessor
DMA Controller
ROM
RAM
GCR Read
GCR Write
CRC Generator
Data Separator

Each of these functional blocks will be described in the following paragraphs.

5.1 HOST INTERFACE

This section provides the electrical interface between the PC-36 Controller and the host computer. The host adaptor logic controls data transfers to and from the host bus. It uses three custom PAL's to decode the address in order to execute the various system commands. It also includes the various switches and jumpers used to determine the device address, the DMA channel, and the interrupt request level.

FIGURE 5.0 PC-36 CONTROLLER BLOCK DIAGRAM



PC-36 CONTROLLER- BLOCK DIAGRAM

5.1.1 I/O Channel Interface

The controller conforms to IBM PC I/O channel requirements described by IBM Technical Reference 6025005. The controller provides manually selectable: a) 10 bit I/O Port Address (even addresses only), b) request/acknowledge selection for DMA channels 1, 2 or 3 and c) interrupt selection for levels 2 through 7.

5.1.1.1 Controller Port Address Selection

The controller port address is dip-switch positions of SW-1 on the PC-36 controller board. Switch positions relative to port addressing are shown below.

ADDRESS BIT	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
SW-1 POSITION	9	8	7	6	5	4	3	2	1	N/A
000 (HEX)	ON	ON	ON	ON	ON	ON	ON	ON	ON	N/A
2AC (HEX)	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	ON	N/A
300 (HEX)	OFF	OFF	ON	ON	ON	ON	ON	ON	ON	N/A
3F6 (HEX)	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	N/A
338 (HEX)	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	ON	N/A

Switch Positions: ON - Logical False (0)
OFF - Logical True (1)

Position 10 not used - off (normal).
Address Bit A0 not used.

5.1.1.2 DMA Data Transfer

The controller utilizes the host PC's DMA channel which is jumper addressable to address 1, 2, or 3. Additional DMA information is described in Programming Guide, Section 11.0.

5.1.1.3 Interrupt Addressing

Interrupt addresses are jumper selectable from 2 to 7. The default address is 2.

5.1.2 I/O Address Interface

Interfacing to the PC-36 controller board is accomplished by addressing two default ports as shown below:

NAME	ADDRESS (HEX)	READ/WRITE FUNCTION
Status Port	300	Read Only
Control Port	300	Write Only
Command Port	300	Write Only
Data Port	301	Read/Write

5.1.2.1 Status Port

Reading from the selected I/O port address shall input the following QIC-02 operational status as defined by the QIC-02 specification to the computer (Refer to Section 6.0):

Bit	0	Ready
	1	Exception
	2	Direction
	3	Reserved
	4-7	Not Used

The controller generates Interrupt (if enabled) when status bits 0 or 1 become active low.

5.1.2.2 Control Port

Writing to the selected I/O port address sends the following control directives to the controller (Refer to Section 6.0):

Bit	0	ONLINE
	1	RESET
	2	REQUEST
	3	Enable selected DMA Channel (1 or 2) and Interrupt
	4	Enable DMA Channel 3 and Interrupt
	5-7	Not Used

5.1.2.3 Command Port

Writing to the selected I/O port address plus 1 transfers the standard QIC-02 commands as defined by the QIC-02 specification to the controller (Refer to Section 7.1).

5.1.2.4 Data Port

Writing to or Reading from the selected I/O port address plus 1 shall transfer data between the host computer and the controller. Reading from the selected I/O port address plus 1 shall also input the six (6) status byte descriptions of the controller to the host computer. (Refer to Section 7.2 for description of status bytes).

5.2 BASIC TAPE DRIVE INTERFACE

The PC-36 controller provides an interface to a Series 5000E tape drive which is compatible with the QIC-36 industry standard interface. For additional information, refer to Section 4.4

5.3 MICROPROCESSOR

The PC-36 controller is controlled by an 8085A-2 microprocessor running at 7.2 MHz input clock frequency. Many of the operating characteristics of the controller are controlled by the microprocessor. Therefore, it is possible for configure the controller to write different tape formats or respond differently to host commands by changing the firmware running on the 8085A-2.

5.4 DMA CONTROLLER

The PC-36 controller uses a 8257 DMA controller to handle data transfers to and from the controller RAM and the host or basic interface. Three of the four DMA channels available on the 8257 are used. DMA Channel 0 is used to transfer data from RAM to tape via the GCR write gate array. DMA Channel 1 is used to transfer data from tape, via the GCR read gate array, to RAM. DMA Channel 2 is used to transfer data between RAM and the host interface.

5.5 ROM

The PC-36 controller is designed to accept any of the plug compatible ROMS (JEDEC Approved) from 16K (2Kx8) to 128K (16Kx8) in size. No jumpers are required for change in ROM size. EPROM configuration - One socket is provided for using EPROM chips. The currently used EPROM types are shown (equivalent types may be used).

EPROM Type	8 X 4K	Intel 2732
	8 X 8K	Intel 2764 (Standard)
	8 X 16K	Intel 27128

The firmware program executed by the 8085A-2 is contained within the EPROM. Additionally, QIC-24 data format described in Section 9.0 is controlled by the EPROM.

5.6 RAM

The PC-36 controller is designed to accept either 2K or 8K RAM chips. A jumper change is required to accommodate the different RAMS.

RAM configuration - One socket is provided for using byte-wide static RAM chips. The currently used RAM types are shown below (equivalent types may be used).

RAM Type	8 X 2K	AMD 9128-20 (Standard)
	8 X 8K	Hitachi 6264-15P

RAM serves as on-board data buffer and a scratch pad memory storage for the 8085A-2 microprocessor. 2Kx8 and 8Kx8 RAM's provide 3x512 and 15x512 data block buffers, respectively.

5.7 GCR READ GATE ARRAY

The GCR Read gate array is a semi-custom chip. It performs the GCR decode and serial to parallel conversion necessary to interface with the basic tape drive.

The GCR read gate array is designed to interface with both the microprocessor and the DMA controller. The Hold Acknowledge output from the microprocessor is used to differentiate between command and status transfers with the microprocessor and data transfers with the DMA controller. Communication with the microprocessor is via I/O Port BX. Communication with the DMA controller is on DMA Channel 1.

The GCR read gate array also interfaces with one of the two CRC/ECC gate arrays on the PC-36 controller. It passes GCR decoded data to the CRC/ECC and latches the state of the error output at the end of the block.

5.8 GCR WRITE GATE ARRAY

The GCR Write gate array is a semi-customer LSI device. It performs the GCR encode and parallel to serial conversion necessary to interface with the basic tape drive. This device is designed to interface with both the microprocessor and the DMA controller. The Hold Acknowledge output from the microprocessor is used to differentiate between microprocessor initiated operations and DMA transfers.

The microprocessor communicates with the GCR Write gate array via I/O Port 71X. The DMA controller communicates via DMA Channel 0.

Like the GCR Read array, the GCR Write array interfaces with a CRC/ECC gate array to calculate the CRC on ECC that is appended to data written to tape.

5.9 CRC GATE ARRAYS

The CRC gate arrays are semi-custom LSI devices. They are capable of calculating a Cyclic Redundancy Check (CRC) character on a serial data stream. Two of these devices are used on the PC-36 controller. One is used to append CRC to the data written to tape. The second is used to check the integrity of data read from tape.

The device used to append CRC to data written is interfaced to the GCR Write gate array. At the beginning of each data block, this CRC gate array is initialized, via its INIT* input, by the GCR Write array. Data is then shifted serially through the device. At the end of a data block, the GCR Write array signals the device to begin outputting the calculated CRC on its Data Out output. This is shifted out, serially by the GCR, write array's CRC clock.

The device used to check the integrity of data read from tape is interfaced to the GCR Read gate array. At the beginning of each data block read, it is initialized via its INIT* input. Data and the CRC (appended during the write operation) are then shifted serially through the device. After the last bit of CRC has been passed to the device, its ERROR* output is true (Low) at this time, an error condition has been detected.

5.10 DATA SEPARATOR

The data separator is a high performance phase lock loop (PLL) with the necessary additional logic to track the incoming read data and convert it back into a NRZ data stream and clock. This data stream is then decoded by the GCR Read Gate Array. The data separator utilized a 4046 PLL chip and various other CMOS FET switches, flip-flops, and other logic elements to perform this function.

6.0 CONTROL LINES

6.1 $\overline{\text{RESET}}$

This signal is generated by the host. Controller connected to the bus is reset and operating parameters are initialized. After RESET, the drive with unit address 0 takes command of the bus and activates EXCEPTION.

6.1.1 No device with unit address 0. The bus stays in a nonactive state and no indication is given to the host. After a time-out, the host may issue a select command to select another drive.

6.2 EXCEPTION

This signal is generated by the controller to indicate that the controller has information for the host. After a RESET, EXCEPTION is always asserted by the selected device. EXCEPTION may be asserted during an operation and should be treated with priority. After EXCEPTION, the only legal command that should be transmitted to the device is Read Status.

6.3 ONLINE

This signal is generated by the host and is true when the device is either writing, reading or searching. In all other operations, the state of this signal is not relevant. Deasserting the ONLINE signal terminates a write or read operation and rewinds the tape to BOT. During deselection and selection of the device while at position, care must be taken to avoid unwanted rewind as a result of the ONLINE signal. Following a write or read operation, the device does not perform rewind when deselected with ONLINE asserted. When reselected the device will sample the state of ONLINE. A rewind does not occur if selection is made with ONLINE asserted or deasserted. However, the host must assert ONLINE prior to any subsequent read or write operations.

6.4 REQUEST

This signal is generated by the host to initiate and execute command transfers. REQUEST is also used to handshake with READY when transferring status information from the controller to the host. This signal should only be asserted when an EXCEPTION or READY is asserted.

6.5 READY

This signal is generated by the controller to indicate one of the following conditions:

1. The controller is available to receive and execute a new command.

2. A new block is ready for transfer during a read or write operation.

3. The controller is ready to receive a new block during write operation.

4. The controller is ready to transfer status information to the host when REQUEST is asserted.

6.6 TRANSFER

This signal is generated by the host and decoded by the Pal on the host adaptor logic to indicate that data is being placed on the data bus in write mode or that data has been taken from the bus in read mode. TRANSFER is used in conjunction with ACKNOWLEDGE to move data between the controller and host.

6.7 ACKNOWLEDGE

This signal is generated by the controller to indicate that data has been accepted from the data bus in write mode or that data is being placed on the bus in read mode. ACKNOWLEDGE is used in conjunction with TRANSFER to move data between the controller and host.

6.8 DIRECTION

This signal is generated by the controller to indicate the direction of the bus. The asserted state of DIRECTION indicates that transfers are from the controller to the host.

7.0 COMMAND/STATUS

The controller includes firmware implementation of all standard QIC-02 commands as follows, including the corresponding 8-bit OP Code:

COMMAND	OP CODE			HEX	
	BIT	7654	3210		
Select Drive "0"		0000	0001	01	
Select Drive "1"		0000	0010	02	
Select Drive "2"		0000	0100	04	(Not Used)
Rewind to BOT		0010	0001	21	
Erase Tape		0010	0010	22	
Initialize (Retension) Tape		0010	0100	24	
Write Data		0100	0000	40	
Write File Mark		0110	0000	60	
Read Data		1000	0000	80	
Read File Mark		1010	0000	A0	
Read Status		1100	0000	C0	
Select QIC-11 Format		0010	0110	26	
Select QIC-24 Format		0010	0111	27	
Power-On/Reset					

All unimplemented, reserved, and unassigned commands will return a illegal command status from the controller.

7.1 COMMAND DESCRIPTIONS

This section defines the commands which are implemented by the controller.

7.1.1 Select (Device N) Command.

The SELECT command selects one of up to three drives. The drives remains selected until changed by either a RESET or another SELECT command.

Before a new device is selected, the currently selected drive's tape must be rewound to BOT; otherwise, the controller will return an illegal command status to the host.

In the case where no drive is selected due to a RESET (NO DRIVE PRESENT) or the attempted selection of a nonexistent drive, the host may then issue a SELECT command to identify another drive.

7.1.2 Rewind Command

The REWIND command positions the tape in the drive at BOT. The normal completion of this command causes READY to be asserted.

7.1.3 Erase Command

The ERASE command completely erases the tape in the drive. The command moves the tape in the selected drive to BOT, activates the erase head and moves to EOT, deactivates the erase head and moves the tape back to BOT. In addition, this command performs all the functions of the INITIALIZATION command. The normal completion of this command causes READY to be asserted.

7.1.4 Initialization Command

The INITIALIZATION command conditions the tape in the drive according to the recommendations of the media manufacturer. The command moves the tape in the selected drive to BOT, then to EOT and then back to BOT. The normal completion of this command causes READY to be asserted.

7.1.5 Write Command

The WRITE command causes data to be written on the tape in the drive. The host must assert ONLINE before issuing the WRITE command. Then, the device transfers data. The READY line is asserted when the device is ready for a data block transfer. When the READY line is asserted, the host can terminate transfer of write data by alternatively issuing a WRITE FILE MARK command or deactivating ONLINE. Deactivating ONLINE causes a file mark to be written (if not preceded by a WRITE FILE MARK command) and the tape is rewound to BOT. Note: A WRITE command following cartridge insertion, RESET, or any command which positions the tape at BOT will commence recording at BOM. Otherwise, recording will commence at the current tape position. If, between blocks, the host starts data transfer by asserting TRANSFER before the device asserts READY, then the behavior of the READY signal is device dependent. The device will, regardless of the way READY is handled, continue the TRANSFER and ACKNOWLEDGE handshaking correctly so that no data is lost.

When EW is detected while recording on the last track, the device ceases to transfer additional data blocks from the host. The device completes writing the current write block in progress, terminates the WRITE command, and reports EOM by means of an EXCEPTION and READ STATUS. The device allows the transfer of two additional blocks of data with a WRITE command after the receipt of EOM. However, EXCEPTION is asserted for each block transferred. The controller will accept the READ STATUS and WRITE FILE MARK commands after detection of EOM.

7.1.6 Write File Mark Command

The WRITE FILE MARK command causes a FILE MARK to be written on the tape in the drive. A WRITE FILE MARK command following cartridge insertion, RESET, or any command which positions the tape at BOT commences recording from BOM. Otherwise, recording commences from the current tape position. The normal completion of this command causes READY to be asserted. Deasserting ONLINE causes the tape to rewind to BOT.

7.1.7 Read Command

The READ command causes data to be read from the tape in the drive. The host must assert ONLINE before issuing the READ command. Then, device transfers data. The READY line is activated when the device is ready for a data block transfer. The READ command is terminated by the device if a file mark is detected. The host is informed of file mark detection by means of an EXCEPTION and a read status sequence. When READY is asserted, the host may terminate the READ command by either:

(a) Deactivating ONLINE, which causes the tape to rewind to BOT; or

(b) Issuing another command.

A READ command following cartridge insertion, RESET, or any command which positions the tape at BOT commences reading at BOM. Otherwise, the READ command commences from the current tape position. If the host starts a data transfer between blocks, before READY is asserted READY may not occur.

7.1.8 Read File Mark Command

The READ FILE MARK command causes the tape in the drive to move to the EOM side of the next file mark. No data is transferred to the host. A READ FILE MARK command following cartridge insertion, RESET, or any command which positions the tape at BOT commences reading from BOM. Otherwise, reading commences from the current tape position. The normal completion of this command causes EXCEPTION to be asserted with FMD asserted.

7.1.9 Read Status Command

The READ STATUS command causes the device to transfer to the host information about itself. The device transfers six bytes of status information. The normal completion of this command causes READY to be asserted. The READ STATUS command must be issued in response to an EXCEPTION condition. Any other command will be rejected by the controller if an EXCEPTION condition exists.

7.1.10 Select QIC-11 Format

If the controller being used has a firmware with default data format of QIC-24, then the SELECT QIC-11 FORMAT command will cause the controller to write or read data in the QIC-11 (Archive 8-inch) format.

This command should be issued only when the selected drive is READY and the inserted cartridge is at BOT. The controller will accept the command if the cartridge is not inserted; however, it will then assert EXCEPTION, informing the host of no cartridge in place. If the command is given during a READ or WRITE operation, the controller will reject it as an illegal command, and the tape will rewind to BOT.

7.1.11 Select QIC-24 Format

If the controller being used has a firmware with default data format of QIC-11, then the SELECT QIC-24 FORMAT command will cause the SBF to write or read data in QIC-24 format.

This command should be issued only when the selected drive is READY and the inserted cartridge is at BOT. The controller will accept the command if a cartridge is not inserted; however, it will then assert EXCEPTION, informing the host of no cartridge in place. If the command is given during a READ or WRITE operation, the controller will reject it as an illegal command, and the tape will rewind to BOT.

7.1.12 Power-On/Reset

The POWER-ON/RESET sequence provides the host with the information on power on occurrences in the device. It also provides a convenient mechanism for initializing the device during hardware and software debugging of the host interface.

A power-on condition or a pulse on the reset line resets the device, and forces it to assert EXCEPTION. When the power on reset times out or when the reset pulse terminates, the device initializes operating parameters and defaults to drive 0 for subsequent commands. The device waits for the host to issue a command. If the command issued was a READ STATUS command, the device now executes the command by transferring the six required status bytes, and sets bit 0 of byte 1 (the second byte) to indicate that power-up or a reset occurred.

7.2 STATUS DESCRIPTION

All DEVICE STATUS is contained in 6 byte groups as defined in the following sections.

7.2.1 Status Byte Summary

Table 3.0 presents a summary of the 6 status bytes returned by the Read Status command.

7.2.2 Status Byte Description

Bytes 0 and 1 contain exception status (EXC) to define the reason that the device asserted EXCEPTION. A description of each status bit is as follows:

<u>STATUS</u> <u>BYTE 1</u>

BIT 0: POR - The Power On/Reset bit is set after the host asserts RESET or when the controller is powered up. The bit is reset by a Read Status Sequence.

BIT 1: RES - Reserved

BIT 2: RES - Reserved

BIT 3: BOM - Beginning of Media bit is set whenever the cartridge is logically at beginning of tape, Track 0. The bit is reset when the tape moves away from beginning of tape. This is the only bit in this byte that does not set EXCEPTION when it goes true, nor is it reset by the Read Status Sequence.

BIT 4: MBD - The Marginal Block Detected bit is set when the controller takes more than eight but less than sixteen retries to read a block with correct CRC. This status bit warns the host that the tape is marginal and should be replaced. This bit is reset by the READ STATUS sequence.

BIT 5: NDT - No Data Detected bit is set when an unrecoverable data error occurs due to lack of recorded data. Absence of recorded data is the failure to detect a data block within 20 inches of tape after three consecutive retries. This bit is reset by a Read Status Sequence.

BIT 6: ILL - Illegal command bit is set if any of the following occurs. The bit is reset by a Reset Status sequence.

a. SELECT command is issued with no drives or more than one drive indicated.

b. ONLINE not asserted when a WRITE, WRITE FILE MARK, READ or READ FILE MARK command is issued.

c. A command other than WRITE or WRITE FILE MARK is issued during the execution of a Write Data sequence.

d. A command other than READ or READ FILE MARK is issued during the execution of a Read Data sequence.

e. A command to select a new drive is issued when the current drive's tape is not at BOT.

BIT 7: ST1 - Status Byte 1 bit is set if any other bit in Status Byte 1 is set.

TABLE 5.0 STATUS BYTES

```
     BYTE 0        BYTE 1         ACRONYM               DESCRIPTION
                                   (EXS)

BIT 76543210      76543210
    !!!!!!!!      !!!!!!!+-------  POR    power on/reset occurred
    !!!!!!!!      !!!!!!!+-------  POR    power on/reset occurred
    !!!!!!!!      !!!!!!+--------  RES    reserved for end of recorded media
    !!!!!!!!      !!!!+----------  RES    reserved for bus parity
    !!!!!!!!      !!!!                    error
    !!!!!!!!      !!!+-----------  BOM    beginning of media
    !!!!!!!!      !!+------------  MBD    marginal block detected
    !!!!!!!!      !+-------------  NDT    no data detected
    !!!!!!!!      !+-------------  ILL    illegal command
    !!!!!!!!      +--------------  ST1    status byte 1 bits

    !!!!!!!+-------------------  FIL    file mark detected
    !!!!!!+--------------------  BNL    bad block not located
    !!!!!+---------------------  UDA    unrecoverable data error
    !!!!+----------------------  EOM    end of media
    !!!+-----------------------  WRP    write protected cartridge
    !!+------------------------  DFF    device fault flag
    !+-------------------------  CNI    cartridge not in place
    +--------------------------  ST0    status byte 0 bits
```

MSB	LSB		
BYTE 2	BYTE 3	DEC	data error counter
BYTE 4	BYTE 5	URC	underrun counter

STATUS BYTE 0

BIT 0: FIL - File Mark detected bit is set when a File Mark is detected during a Read Data or Read File Mark sequence. The bit is reset by a Read Status sequence.

BIT 1: BNL - Block in error Not Located bit is set when an unrecoverable read error occurs and the controller can not confirm that the last block transmitted was the block in error. The bit is reset by a Read Status sequence.

BIT 2: UDA - Unrecoverable Data Error bit is set when the controller cannot read a block after sixteen retries and cannot obtain a correct CRC. The UDA bit is also set when the controller cannot correctly write a block within sixteen retries or when the controller cannot locate a block. The UDA bit is reset by a READ STATUS sequence.

BIT 3: EOM - End of Media bit is set when the logical early warning hole of the last track is detected during a write operation. This bit will remain set as long as the drive is at logical end of media. The EOM bit will not be reset by a Read Status sequence.

BIT 4: WRP - Write Protected bit is set if the cartridge write protect plug is set in the file protect "safe" position. Operator must change the write protect plug position before the status bit will reset.

BIT 5: DFF - Device Fault Flag bit is set when the device detects a problem other than data errors during command execution. RESET or READ STATUS sequences will reset this bit.

BIT 6: CNI - Cartridge Not in Place bit is set if a cartridge is not fully inserted into the drive. Operator must correct the condition before the status bit will reset.

BIT 7: ST0 - Status Byte 0 bit is set if any other bit in Status Byte 0 is set.

Refer to EXCEPTION STATUS SUMMARY and EXCEPTION STATUS DESCRIPTION for further explanation.

Bytes 2 and 3 contain the data error counter (DEC) which accumulates the number of blocks rewritten for WRITE operations and the number of soft read errors during READ operations. These bytes are cleared by a Read Status sequence.

Bytes 4 and 5 contain the underrun counter (URC) which accumulates the number of times that streaming was interrupted because host failed to maintain minimum throughput rate. These bytes are cleared by a Read Status sequence.

7.2.3 Exception Status Summary

	Byte 0	Byte 1	Description
1.	110X0000	00000000	No Cartridge
2.	00100000	00000000	Device Fault Flag
3.	10010000	X000X000	Write Protected
4.	10001000	00000000	End of Media
5.	100X0100	10001000	Read or Write Abort
6.	100X0100	00000000	Read Error, Bad Block Xfer
7.	100X0110	00000000	Read Error, Filler Block Xfer
8.	100X0110	10100000	Read Error, No Data
9.	100X1110	10100000	Read Error, No Data & EOM
10.	100X0001	00000000	Read a Filemark
11.	XXXX0000	1100X000	Illegal Command
12.	XXXX0000	1000X001	Power On/Reset
13.	100X0001	00010000	Marginal Block Detected (Not Used)

NOTE: "X" denotes either 0 or 1 condition.

7.2.4 Exception Status Description

1. NO CARTRIDGE - Selected drive did not contain a cartridge when BOT, RET, ERASE, WRITE, WFM, READ or RFM was issued or cartridge was removed while the drive is selected. FATAL.

2. DEVICE FAULT FLAG - The drive detected a problem other than data errors during command execution. FATAL.

3. WRITE PROTECTED - Selected drive contained write protected (safe) cartridge when ERASE, WRITE, or WFM was issued. FATAL.

4. END OF MEDIA - Tape has passed the logical early warning hole of the last track during WRITE command. CONTINUABLE.

5. READ OR WRITE ABORT - The maximum limit of same block rewrites occurred during a WRITE or WFM command or unrecoverable reposition error occurred during a WRITE, WFM, READ, or RFM command... Tape has returned to BOT. FATAL.

6. READ ERROR, BAD BLOCK XFER - The maximum limit of same block retrys failed to recover block without CRC error, last block transferred contained data from the erroneous data block for off line reconstruction. CONTINUABLE.

7. READ ERROR, FILLER BLOCK XFER - The maximum limit of same block retrys failed to recover block without CRC error, last block transferred contained filler data to keep total block count correct. CONTINUABLE.

8. READ ERROR, NO DATA - No recorded data found on tape for 20 inches. CONTINUABLE.

9. READ ERROR, NO DATA & EOM - The maximum limit of same block retries failed to recover the next or subsequent blocks and the logical end of tape holes on the last track were encountered. CONTINUABLE.

10. FILEMARK READ - A filemark block was read during a READ or RFM command. CONTINUABLE.

11. ILLEGAL COMMAND - One of the following events occurred:

a. Attempt to select other than one drive.

b. Attempt to change drive selection when tape has been moved away from BOT by a read or write operation.

c. Attempt to BOT, RETENSION, or ERASE simultaneously.

d. Attempt to WRITE, WFM, READ, or RFM with ONLINE not asserted.

e. Attempt to issue a command other than WRITE or WFM during a WRITE command. FATAL.

f. Attempt to issue a command other than READ or RFM during a READ command. FATAL.

g. Attempt to issue any command not implemented.

12. POWER ON/RESET - A power on/reset or a reset by the host has occurred. FATAL.

13. MARGINAL BLOCK DETECTED - A data block was detected by the device after more than eight but less than sixteen retries. CONTINUABLE.

8.0 COMMAND TIMING

The PC-36 controller has two distinct logical sections: the host adaptor section and the formatter section. The host adapter section communicates with the IBM PC/XT/AT and their compatibles via the IBM I/O channel and with the formatter section via the QIC-02 interface. The QIC-02 interface resides within the PC-36 controller itself. The following command signal timing specifications reflect signal activity at the QIC-02 interface level.

8.1 RESET TIMING

Figure 6.0 presents the timing diagram which results from the assertion of RESET. As indicated in the diagram the host is required to maintain reset assertion for at least 25 microseconds.

8.2 READ STATUS TIMING

A hardware reset or a power on reset (generated by the drive) will generate an Exception condition, indicated by the assertion of EXCEPTION from the controller. The host clears Exception by performing a Read Status command. Figure 7.0 shows the timing for the Read Status command.

8.3 SELECT COMMAND TIMING

The controller will respond to the Select Command as defined by the QIC specification. The controller will produce an Exception condition if a drive other than 0 is selected. Timing for the Select Command sequence is shown in Figure 8.0

8.4 POSITION COMMAND TIMING

Figure 9.0 illustrates timing for the Rewind, Erase, and Retension commands.

8.5 WRITE DATA TIMING

One of the two major commands of the controller is Write Data. This is the mechanism by which user data is recorded on the tape media. Figure 10.0 shows the Timing Diagrams associated with this command.

8.6 READ DATA TIMING

Once data has been recorded on tape it is recovered by the Read Data command, the second major command. Figure 11.0 presents the timing for the Read Data command.

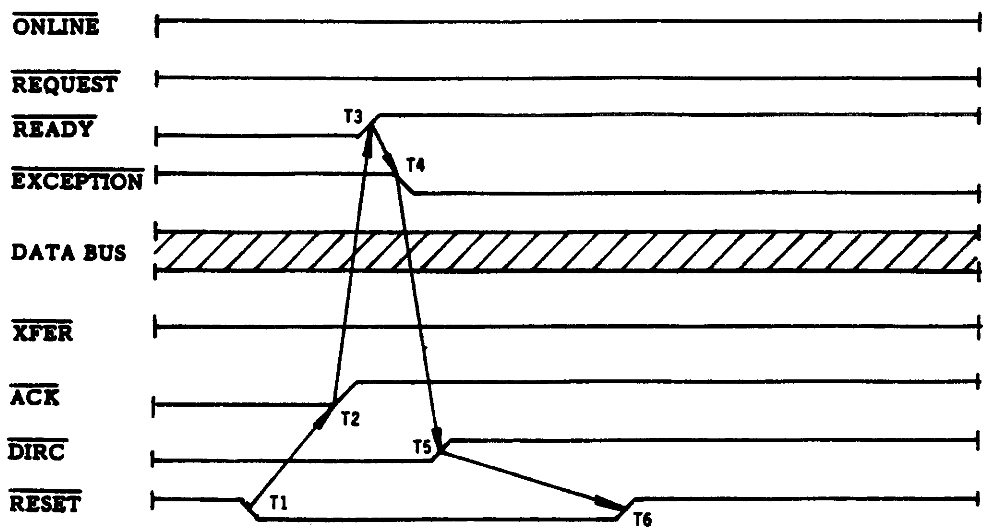
8.7 WRITE FILE MARK COMMAND TIMING

The File Mark is a method by which the user can separate logical or physical records on the tape. The Write File Mark Command Timing diagram is shown in Figure 12.0.

8.8 READ FILE MARK COMMAND TIMING

To position the tape at a file mark a Read File Mark Command is issued. Figure 13.0 shows the timing for this command.

FIGURE 6.0 RESET TIMING DIAGRAM

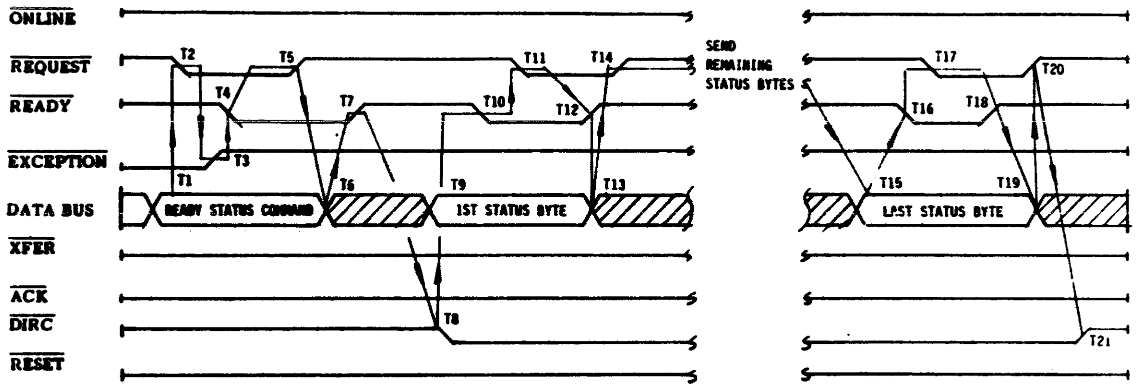


RESET TIMING

ACTIVITY	CRITICAL TIMING
T1 - HOST ASSERTS RESET	N/A
T2 - CONTROLLER DE-ASSERTS ACK	T1 — T2 < 1 Usec
T3 - CONTROLLER DE-ASSERTS READY	T1 — T3 < 1 Usec
T4 - CONTROLLER ASSERTS EXCEPTION	T1 — T4 < 3 Usec
T5 - CONTROLLER DE-ASSERTS DIRC	T1 — T5 < 3 Usec
T6 - HOST DE-ASSERTS RESET	T1 — T6 > 25 Usec

X - DON'T CARE

FIGURE 7.0 READ STATUS COMMAND TIMING



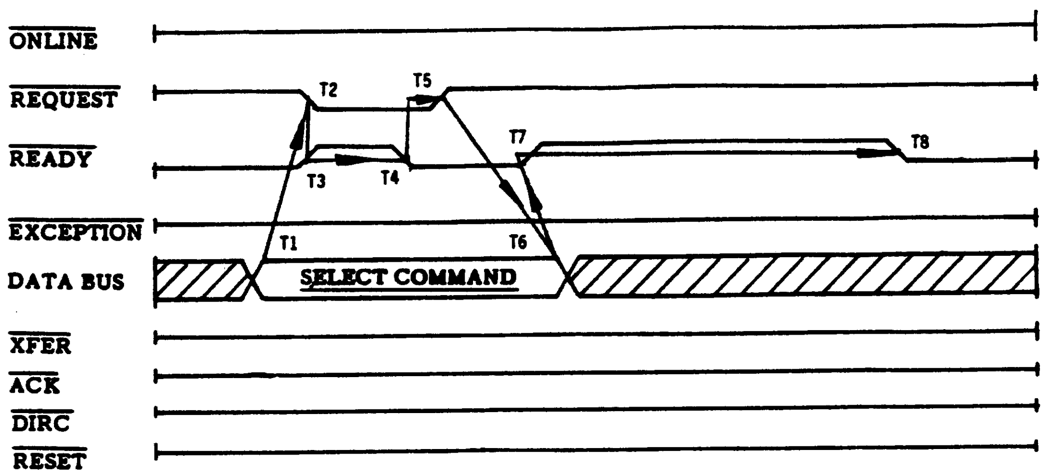
READ STATUS COMMAND

ACTIVITY	CRITICAL TIMING
T1 - HOST COMMAND TO BUS	N/A
T2 - HOST ASSERTS REQUEST	T1 — T2>Usec
T3 - CONTROLLER DE-ASSERTS EXCEPTION	T3 — T4>10Usec
T4 - CONTROLLER ASSERTS READY	T2 — T4>20Usec (500 Usec nominal)
T5 - HOST DE-ASSERTS REQUEST	T4 — T5>0Usec
T6 - BUS DATA INVALID	T4 — T6>0Usec
T7 - CONTROLLER DE-ASSERTS READY	20 < T5— T7<100 Usec
T8 - CONTROLLER CHANGES BUS DIRECTION	N/A
T9 - 1ST STATUS BYTE TO BUS	N/A
T10- CONTROLLER ASSERTS READY	T7 — T10>20 Usec
T11- HOST ASSERTS REQUEST	T10— T11>500 N.S
T12- CONTROLLER DE-ASSERTS READY	T11— T12<1 Usec
T13- BUS DATA INVALID	T11— T13>0 Usec
T14- HOST DE-ASSERTS REQUEST	T11— T14>20 Usec

ACTIVITY	CRITICAL TIMING
T15-LAST STATUS BYTE TO BUS	N/A
T16-SAME AS T10	SAME AS T10
T17-SAME AS T11	SAME AS T11
T18-SAME AS T12	SAME AS T12
T19-SAME AS T13	SAME AS T13
T20-SAME AS T14	SAME AS T14

X - DON'T CARE

FIGURE 8.0 SELECT COMMAND TIMING



SELECT COMMAND

ACTIVITY

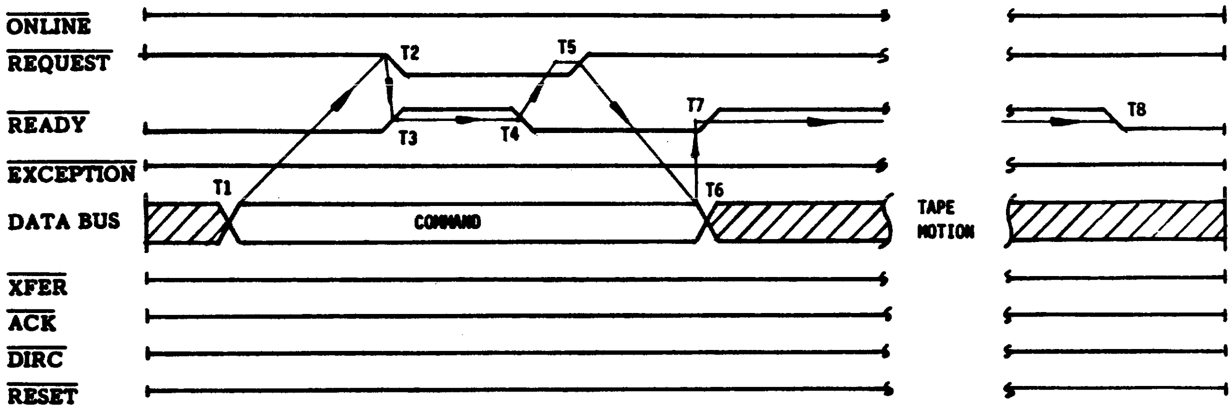
T1 - HOST COMMAND TO BUS
T2 - HOST ASSERTS REQUEST
T3 - CONTROLLER DE-ASSERTS READY
T4 - CONTROLLER ASSERTS READY
T5 - HOST DE-ASSERTS REQUEST
T6 - BUS DATA INVALID
T7 - CONTROLLER DE-ASSERTS READY
T8 - CONTROLLER ASSERTS READY

X - DON'T CARE

CRITICAL TIMING

N/A
T1 — T2 > Ø Usec
T2 — T3 < 1 Usec
T3 — T4 > 50 Usec (500 Usec nominal)
T4 — T5 > Ø Usec
T4 — T6 > Ø Usec
20 < T5 — T7 < 100 Usec
T7 — T8 > 20 Usec

FIGURE 9.0 POSITION COMMAND TIMING

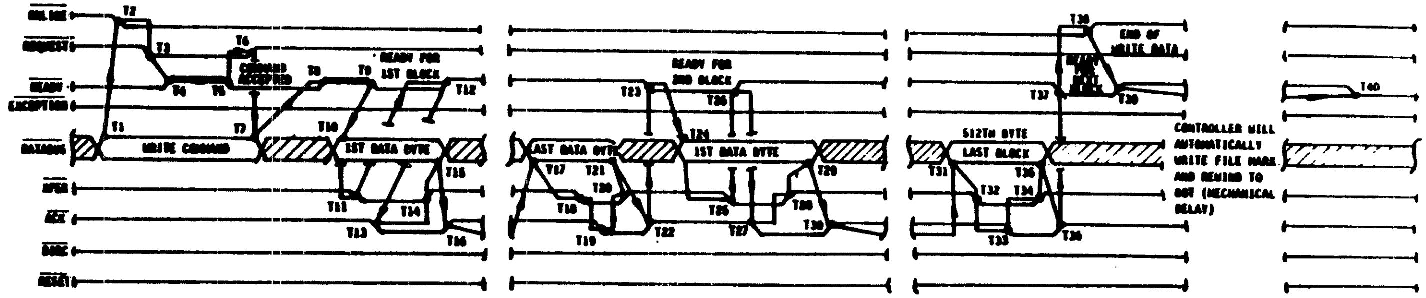


BOT, RETENSION OR ERASE COMMAND

ACTIVITY	CRITICAL TIMING
T1 - HOST BUS DATA VALID	N/A
T2 - HOST ASSERTS REQUEST	T1 — T2 > Ø Usec
T3 - CONTROLLER DE-ASSERTS READY	T2 — T3 < 1 Usec
T4 - CONTROLLER ASSERTS READY	T3 — T4 > 20 Usec (500 Usec nominal)
T5 - HOST DE-ASSERTS REQUEST	T4 — T5 > Ø Usec
T6 - BUS DATA INVALID	T4 — T6 > Ø Usec
T7 - CONTROLLER DE-ASSERTS READY	20 < T5 — T7 < 100 Usec
T8 - CONTROLLER ASSERTS READY	T7 — T8 > 20 Usec

X - DON'T CARE

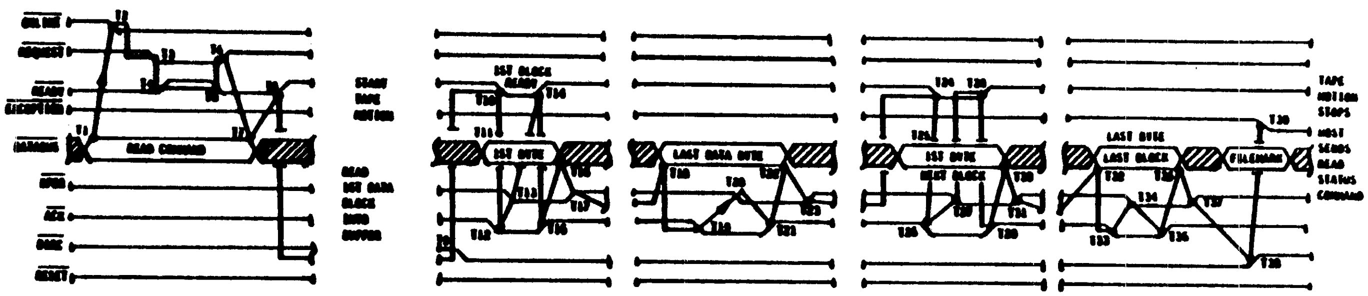
FIGURE 10.0 WRITE DATA COMMAND TIMING



WRITE DATA COMMAND

ACTIVITY	CRITICAL TIMING	ACTIVITY	CRITICAL TIMING	ACTIVITY	CRITICAL TIMING
T1-HOST COMMAND TO BUS	N/A	T15-BUS DATA INVALID	T13-T15>0 U Sec	T28-HOST DE-ASSERTS XFER	SAME AS T14
T2-HOST ASSERTS ONLINE	N/A	T16-CONTROLLER DE-ASSERTS ACK	0<T14-T16<3 U Sec	T29-BUS DATA INVALID	SAME AS T15
T3-HOST ASSERTS REQUEST	T2-T3>0 U Sec	T17-HOST DATA TO BUS	N/A	T30-CONTROLLER DE-ASSERTS ACK	SAME AS T16
T4-CONTROLLER DE-ASSERTS READY	T3-T4<1 U Sec	T18-SAME AS T11	SAME AS T11	T31-HOST DATA TO BUS	N/A
T5-CONTROLLER ASSERTS READY	T4-T5>20 U Sec (500 U sec nominal)	T19-SAME AS T13	SAME AS T13	T32-HOST ASSERTS XFER	SAME AS T18
T6-HOST DE-ASSERTS REQUEST	T5-T6>0 U Sec	T20-SAME AS T14	SAME AS T14	T33-CONTROLLER ASSERTS ACK	SAME AS T19
T7-BUS DATA INVALID	T5-T7>0 U Sec	T21-SAME AS T15	SAME AS T15	T34-HOST DE-ASSERTS XFER	SAME AS T20
T8-CONTROLLER DE-ASSERTS READY	20<T6-T8<100 U Sec	T22-SAME AS T16	SAME AS T16	T35-BUS DATA INVALID	N/A
T9-CONTROLLER ASSERTS READY	T8-T9>20 U Sec	T23-CONTROLLER ASSERTS READY	T22-T23>100 U Sec	T36-CONTROLLER DE-ASSERTS ACK	SAME AS T22
T10-HOST DATA TO BUS	N/A	T24-HOST DATA TO BUS	N/A	T37-CONTROLLER ASSERTS READY	SAME AS T23
T11-HOST ASSERTS XFER	T10-T11>40 NANO Sec	T25-HOST ASSERTS XFER	SAME AS T11	T38-HOST DE-ASSERTS ONLINE	N/A
T12-CONTROLLER DE-ASSERTS READY	T11-T12<1 U Sec	T26-CONTROLLER DE-ASSERTS READY	SAME AS T12	T39-CONTROLLER DE-ASSERTS READY	N/A
T13-CONTROLLER ASSERTS ACK	0.5<T11-T13<100 U Sec	T27-CONTROLLER ASSERTS ACK	SAME AS T13	T40-CONTROLLER ASSERTS READY	N/A
T14-HOST DE-ASSERTS XFER	T13-T14>0 U Sec				

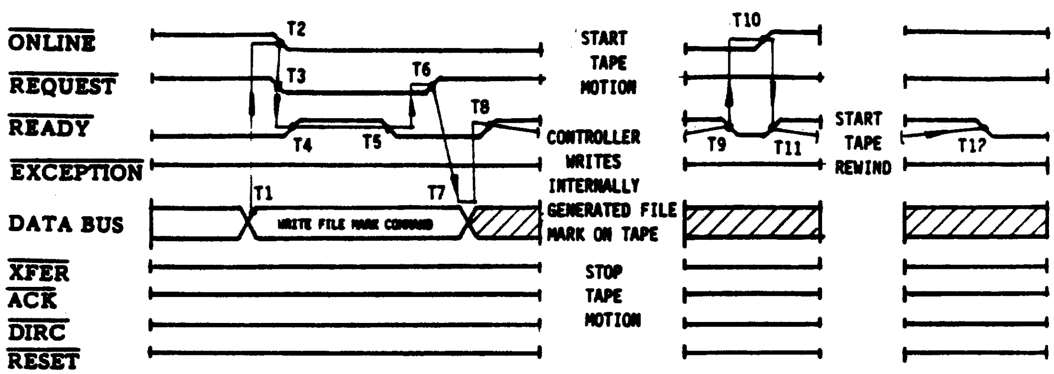
FIGURE 11.0 READ DATA COMMAND TIMING



ACTIVITY	CRITICAL TIMING	ACTIVITY	CRITICAL TIMING	ACTIVITY	CRITICAL TIMING
T1-HOST COMMAND TO BUS	N/A	T14-CONTROLLER DE-ASSERTS READY	T13-T14<1 U Sec.	T27-HOST ASSERTS XFER	SAME AS T13
T2-HOST ASSERTS ONLINE	N/A	T15-CONTROLLER DE-ASSERTS ACK	0.5<T13-T15<3 U Sec	T28-CONTROLLER DE-ASSERTS READY	SAME AS T14
T3-HOST ASSERTS REQUEST	T2-T13>0 U Sec	T16-BUS DATA INVALID	T13-T16>0 U Sec	T29-CONTROLLER DE-ASSERTS ACK	SAME AS T15
T4-CONTROLLER DE-ASSERTS READY	T3-T4<1 U Sec	T17-HOST DE-ASSERTS XFER	T16-T17>0 U Sec	T30-BUS DATA INVALID	SAME AS T16
T5-CONTROLLER ASSERTS READY	T4-T5>20 U Sec (500 U Sec nominal)	T18-BUS DATA VALID		T31-HOST DE-ASSERTS XFER	SAME AS T17
T6-HOST DE-ASSERTS REQUEST	T5-T6>0 U Sec	N/A		T32-LAST BYTE TO BUS	N/A
T7-BUS DATA INVALID	T5-T7>0 U Sec	T19-CONTROLLER ASSERTS ACK	SAME AS T12	T33-CONTROLLER ASSERTS ACK	SAME AS T12
T8-CONTROLLER DE-ASSERTS READY	20<T6-T8<100 U Sec	T20-HOST ASSERTS XFER	SAME AS T13	T34-HOST ASSERTS XFER	SAME AS T13
T9-CONTROLLER CHANGES DIRC	N/A	T21-CONTROLLER DE-ASSERT ACK	SAME AS T15	T35-CONTROLLER DE-ASSERTS ACK	SAME AS T15
T10-1ST DATA BYTE TO BUS	N/A	T22-BUS DATA INVALID	SAME AS T16	T36-BUS DATA INVALID	SAME AS T16
T11-CONTROLLER ASSERTS READY	N/A	T23-HOST DE-ASSERTS XFER	SAME AS T17	T37-HOST DE-ASSERTS XFER	SAME AS T17
T12-CONTROLLER ASSERTS ACK	T11-T12>40 NANO Sec	T24-CONTROLLER ASSERTS READY	N/A	T38-CONTROLLER CHANGES BUS DIRECTION	N/A
T13-HOST ASSERTS XFER	T12-T13>0 U Sec	T25-1ST BYTE TO BUS	N/A	T39-CONTROLLER ASSERTS EXCEPTION	N/A
		T26-CONTROLLER ASSERTS ACK	SAME AS T12		

NOTE: T12 can precede T11 by 40 Nano Seconds.

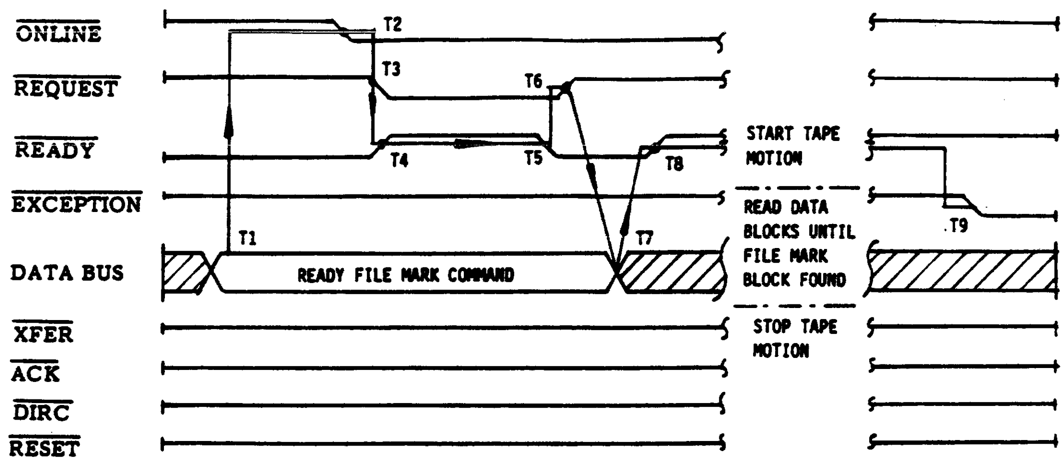
FIGURE 12.0 WRITE FILE MARK COMMAND TIMING



WRITE FILE MARK COMMAND

ACTIVITY	**CRITICAL TIMING**
T1 - HOST COMMAND TO BUS	N/A
T2 - HOST ASSERTS ONLINE	T1 — T2 > Ø Usec
T3 - HOST ASSERTS REQUEST	T2 — T3 > Ø Usec
T4 - CONTROLLER DE-ASSERTS READY	T3 — T4 < 1 Usec
T5 - CONTROLLER ASSERTS READY	T4 — T5 > 20 Usec (500 Usec nominal)
T6 - HOST DE-ASSERTS REQUEST'	T5 — T6 > Ø Usec
T7 - BUS DATA INVALID	T5 — T7 > Ø Usec
T8 - CONTROLLER DE-ASSERTS READY	20 < T6 — T8 < 100 Usec
T9 - CONTROLLER ASSERTS READY	N/A
T10-HOST DE-ASSERTS ONLINE	T9 — T10 > Ø Usec
T11-CONTROLLER DE-ASSERTS READY	N/A
T12-CONTROLLER ASSERTS READY (AT BOT)	N/A

FIGURE 13.0 READ FILE MARK COMMAND TIMING



READ FILE MARK COMMAND

ACTIVITY	CRITICAL TIMING
T1 - HOST COMMAND TO BUS	N/A
T2 - HOST ASSERTS ONLINE	T1 — T2 > ∅ Usec
T3 - HOST ASSERTS REQUEST	T2 — T3 > ∅ Usec
T4 - CONTROLLER DE-ASSERTS READY	T3 — T4 < 1 Usec
T5 - CONTROLLER ASSERTS READY	T4 — T5 > 20 Usec (500 Usec nominal)
T6 - HOST DE-ASSERTS REQUEST	T5 — T6 > ∅ Usec
T7 - BUS DATA INVALID	T4 — T7 > ∅ Usec
T8 - CONTROLLER DE-ASSERTS READY	20 < T6 — T8 < 100 Usec
T9 - CONTROLLER ASSERTS EXCEPTION	N/A

*SYSTEM MUST ISSUE READ STATUS COMMAND

9.0 DATA FORMAT

9.1 QIC-11 DATA FORMAT

This section defines the requirements necessary to ensure interchange at acceptable performance levels when data is written in QIC-11 (8-inch Archive) data format.

9.1.1 Definitions

azimuth - the angular deviation, in minutes of arc, of the mean flux transition line from the normal to the cartridge reference plane.

bit - a single digit in the binary number system.

bit cell - a length of magnetic recording tape within which the occurrence of a flux transition signifies a "one" bit and the absence signifies a "zero" bit.

block - a group of 512 consecutive bytes transferred as a unit.

BOT - beginning of tape marker indicating beginning of tape.

byte - a group of 8 binary (10 GCR) bits operated on as a unit.

cartridge - a four by six inch enclosure containing 0.250 in (6.30 mm) wide magnetic tape wound on two coplanar hubs and driven by an internal belt which is coupled by an internal belt capstan to the external drive (ref. ANSI X3.55-1977).

cyclical redundancy check - a two byte code derived from information contained in the data block and block number byte and recorded after the data block and block number byte for read after write check and read only check.

density - the maximum allowable flux transitions per unit length for a specific recording standard.

early warning - early warning marker indicating the approaching end of the permissible recording area.

EOT - end of tape marker indicating the end of tape.

erase - to remove all magnetically recorded information from the tape.

file mark - an identification mark following the lst block in a file.

flux transition - a point on the magnetic tape which exhibits maximum free space flux density normal to the tape surface.

flux transition spacing - the distance on the magnetic tape between flux reversals.

group code recording - (GCR) a data encoding method where a 4-bit group of data bits is encoded into a 5-bit group for recording on magnetic tape (ref. ANSI X3.54-1976).

load point - load point marker indicating the beginning of the permissible recording area.

magnetic tape - an oxide coated mylar base tape capable of accepting and retaining magnetically recorded information.

nibble - a group of 4 binary (5 GCR) bits operated on as a unit.

postamble - guard information recorded after the data block.

recorded block - a group of consecutive bits comprising preamble, data block marker, data block, block number, GCR and postamble.

reference tape cartridge - a magnetic tape cartridge selected for a specific property to be used as a reference.

retension - an operation which restores normal tension to the tape wound on the hubs of a cartridge.

streaming - a method of recording on magnetic tape where the tape is continuously moving and data blocks are continuously recorded.

track - a recording strip parallel to the edge of the magnetic tape containing recorded information.

underrun - a condition developed when host transmits or receives data at a rate less than that required by the device or streaming operation.

9.1.2 Recording

9.1.2.1 Method

The method of recording is the "non-return to zero, change on one" (NRZI) where a "one" is represented by a flux transition occurring in the bit cell and a "zero" is represented by the absence of a flux transition in the bit cell.

9.1.2.2 Code

Each 8-bit data byte is separated into two 4-bit groups (nibbles). Each 4-bit data nibble is encoded into a 5-bit GCR nibble for recording on the streaming magnetic tape cartridge. The most significant nibble is recorded first. The encoded data has the property that no more than two consecutive "zeros" occur. The translation table for data nibbles (B3, B2, B1, B0) and GCR nibbles (G4, G3, G2, G1, G0) are as follows:

HEX	B3	B2	B1	B0		G4	G3	G2	G1	G0	HEX
0	0	0	0	0	----	1	1	0	0	1	19
1	0	0	0	1	----	1	1	0	1	1	1B
2	0	0	1	0	----	1	0	0	1	0	12
3	0	0	1	1	----	1	0	0	1	1	13
4	0	1	0	0	----	1	1	1	0	1	1D
5	0	1	0	1	----	1	0	1	0	1	15
6	0	1	1	0	----	1	0	1	1	0	16
7	0	1	1	1	----	1	0	1	1	1	17
8	1	0	0	0	----	1	1	0	1	0	1A
9	1	0	0	1	----	0	1	0	0	1	09
A	1	0	1	0	----	0	1	0	1	0	0A
B	1	0	1	1	----	0	1	0	1	1	0B
C	1	1	0	0	----	1	1	1	1	0	1E
D	1	1	0	1	----	0	1	1	0	1	0D
E	1	1	1	0	----	0	1	1	1	0	0E
F	1	1	1	1	----	0	1	1	1	1	0F

9.1.2.3 Nominal Density

The maximum nominal recording density (flux transitions in every bit cell) is 10,000 flux transitions per inch (394 flux transitions per millimeter).

9.1.2.4 Nominal Bit Cell Length

The nominal bit cell length is 100 microinches (2.54 micrometers).

9.1.2.5 Average Bit Cell Length

The average bit cell length is the sum of distances between flux transitions over N bit cells divided by N. Any continuously recorded group code pattern may be used to measure the average bit cell.

9.1.2.6 Long Term Average Bit Cell Length

The long term average bit cell length is the average bit cell length taken over a minimum of 900,000 bit cells. The long term average bit cell length is within ±4% of the nominal bit cell length.

9.1.2.7 Medium Term Average Bit Cell Length

The medium term average bit cell length is the average bit cell length taken over a minimum of 126 and a maximum of 130 bit cells. The medium term average bit cell length is within ±7% of the long term average bit cell length.

9.1.2.8 Short Term Average Bit Cell Length

The short term average bit cell length is the average bit cell length taken over a minimum of 39 and a maximum of 43 bit cells.

9.1.2.9 Short Term Average Cell Center Length

The short term average bit cell center is located at a point 1/2 the short term average bit cell length from either egde.

9.1.2.10 Reference Bit Cell

The reference bit cell is the center bit cell in the bit cell group used to measure the short term average bit cell length. Bit cell centers of the bit cell group are positioned such distanced between flux transitions and bit cell centers are minimized ignoring missing flux transitions.

9.1.2.11 Data Amplitude

The data amplitude is measured at a point 1/2 the short term average bit cell length after each flux transition and will be greater than 25% of the average standard reference amplitude for all flux transitions in each non-rewritten block.

9.1.2.12 Erasure

The magnetic tape cartridge is AC erased (demagnetized) prior to recording such that no remaining signal amplitude is greater than 3% of the lowest data amplitude.

9.1.2.13 Azimuth

The angular deviation of the mean flux transition line from a normal to the magnetic tape cartridge reference base is less than or equal to 5 minutes of arc.

9.1.3 Tracks

9.1.3.1 Number and Use of Tracks

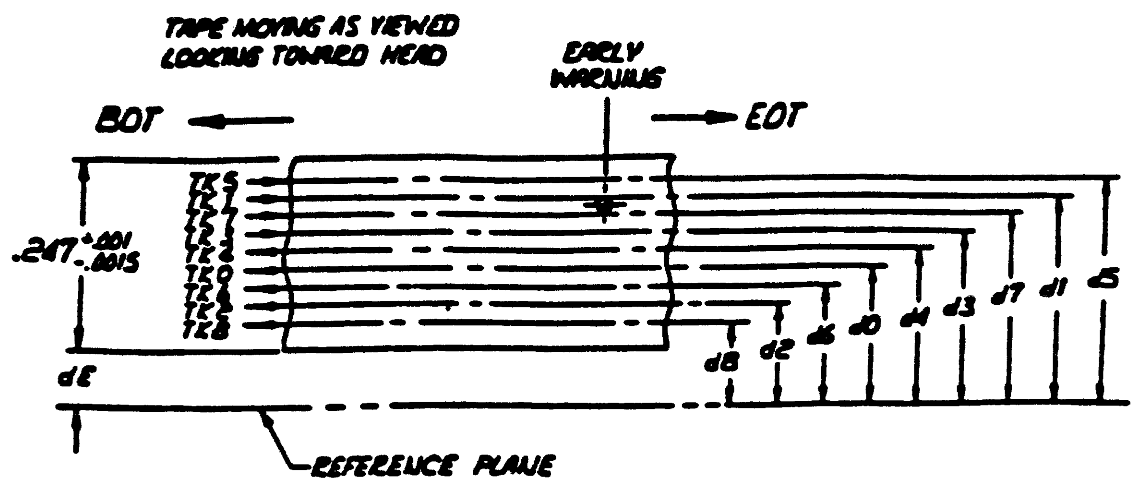
There are a maximum of nine tracks numbered 0 through 8 as shown in Figure 11. Even numbered tracks are recorded serially in the forward direction of tape movement. Odd numbered tracks are recorded serially in the reverse direction of tape movement. On even tracks, all data for interchange is recorded after the load point marker and before the end of tape marker. On odd tracks 3 and 5, all data for interchange is recorded after the early warning marker and before the beginning of tape marker. However, on tracks 1 and 7, all data for interchange is recorded between the early warning marker and the load point marker. Tracks are recorded sequentially in the order, 0, 1, 2, ..., 8.

9.1.3.2 Reference Plane

The top surface of the magnetic tape cartridge base is the reference plane.

9.1.3.3 Track Center Line Locations

The track center lines are located as indicated below:



d0 = 0.172 $\pm$0.001 in
d1 = 0.268 $\pm$0.001 in
d3 = 0.124 $\pm$0.001 in
d4 = 0.220 $\pm$0.001 in
d5 = 0.196 $\pm$0.001 in
d6 = 0.292 $\pm$0.001 in
d7 = 0.244 $\pm$0.001 in
d8 = 0.100 $\pm$0.001 in
dE = 0.070 in reference

FIGURE 14.0 TRACK CENTER LINE LOCATIONS

9.1.3.4 Track Width for 0.048 in Track Spacing

When an 0.048 in track spacing is used, the number of recorded tracks are limited to a maximum four tracks. The width of the recorded track is 0.036 $\pm$0.002 inches. Th width of the verified recorded track (read after write) is 0.020 $\pm$0.001 inches.

9.1.3.5 Track Width for 0.024 in Track Spacing

When an 0.024 in track spacing is used, all nine tracks may be recorded. The width of the recorded track is 0.0135 $\pm$0.0005 inches. The width of the verified recorded track is 0.0165 $\pm$0.0005 inches.

9.1.3.6 Interchange Between 0.048 and 0.024 in Track Spacing

Magnetic tape cartridges recorded with the 0.048 in track spacing provides data interchange with magnetic tape cartridges with the 0.024 in track spacing where the recording has been limited to tracks 0 through 3 subject to the condition that nominal signal amplitudes may be reduced to 70% of normal.

9.1.4 Data Block

The data block format shall be as follows:

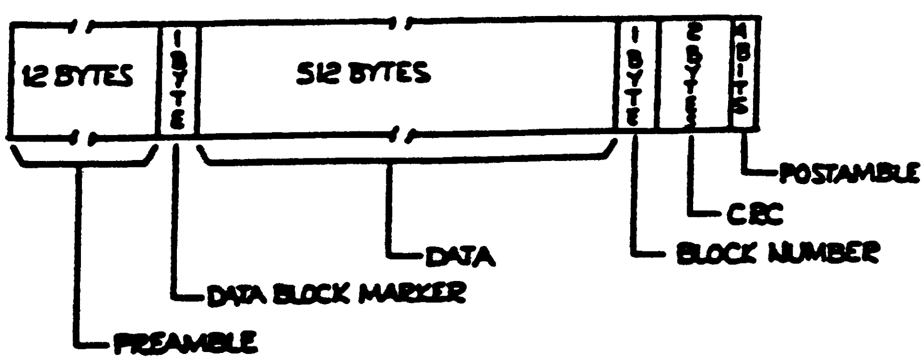


FIGURE 15.0 DATA BLOCK FORMAT

9.1.4.1 Preamble

The preamble contains 120 flux transitions (12 bytes) recorded at the maximum nominal recording density of 10,000 flux transitions per inch (394 flux transitions per millimeter). The preamble is used to synchronize the phase locked loop in the read electronics to the data frequency. The preamble is also used to measure the average preamble amplitude.

A long preamble is used preceding the first data block recorded after an underrun (7.2) and preceding the first data block for interchange recorded at the beginning of a track (8.0).

9.1.4.2 Data Block Marker

The data block marker identifies the start of data and consists of the following GCR pattern:

G4	G3	G2	G1	G0	G4	G3	G2	G1	G0
1	1	1	1	1	0	0	1	1	1
MS nibble					LS nibble				

9.1.4.3 Data Block

The data block contains 512 bytes of data for interchange encoded into GCR bytes in accordance with the CODE.

9.1.4.4 Block Number

The block number uniquely identifies a block over a group of 256 blocks and is used in error detection and tape positioning. The block number is encoded into GCR bytes in accordance with the CODE. The first block on the tape is block 1 and subsequent blocks are numbered sequentially.

9.1.4.5 Cyclical Redundancy Check

The cyclical redundancy check (CRC) consists of two bytes calculated over the 512 bytes of interchange data and the 1 byte block number starting with all ones CRC initial value and using the CRC generating polynominal:

$$X^{16} + X^{12} + X^{5} + 1$$

The CRC is encoded into GCR bytes in accordance with the CODE.

9.1.4.6 Postamble

A five flux transition postamble recorded at the maximum nominal flux density is recorded following the CRC as a guard band.

9.1.5 File Mark

The file mark block format is identical to the data block format except that the data field contains 512 bytes consisting of the following GCR pattern:

G4	G3	G2	G1	G0	G4	G3	G2	G1	G0
0	0	1	0	1	0	0	1	0	1
MS nibble					LS nibble				

The GCR nibble (00111) is converted to the HEX nibble (1111) to form the data field for CRC generation and checking.

9.1.6 Rewritten Blocks

Data for interchange is rewritten such that requirements for data interchange are met. Each data and file mark block that do not meet the requirements for interchange is rewritten. A data block is tested for interchange requirements during the read after write check. Writing of block N + 1 begins before the read after write check of block N is completed. If block N satisfies the requirements for interchange, the read after write check of block N + 1 is begun. However, if block N does not satisfy the requirements for interchange, it is rewritten after the writing of block N + 1 is completed. Block N + 1 is also rewritten after block N in order to preserve the sequential order of records. Block N is written up to 16 times before the recording operation is aborted. A sequence of rewritten blocks is shown below.

... N-1 | N | N+1 | N | N+1 | N+2 ...

9.1.6.1 Underrun, End of File or End of Track

Streaming operation is normally terminated when underrun, end of file or end of track conditions exist. The normal sequence of recording of blocks N, N + 1, etc. is replaced by the sequence of blocks N, N, etc. until the recording of block N meets the requirements for interchange. When block N is recorded such that the requirements of interchange are met, the associated rewriting of block N is completed and a postamble of 0.354 inches minimum, 0.508 maximum is written as follows:

... N-1 N N

Long Postamble
.354" Min.
.508" Max.

Recording in the long postamble begins at 0.309 inches minimum, 0.358 inches maximum from the end of the block preceding the long postamble. A long preamble of 0.209 inches minimum, 0.72 inches maximum is recorded before recording any other field in the block.

Long Postamble

... N-1 N N

Overlap

.309" Min.
.358" Max.
.722" Max.

Long Preamble
.209" Min.

9.1.6.2 Forced Streaming

Termination of streaming operation due to underrun may optionally be prevented by continued recording of the last block until end of file or end of track occurs. Standard length format fields are used during forced streaming operation.

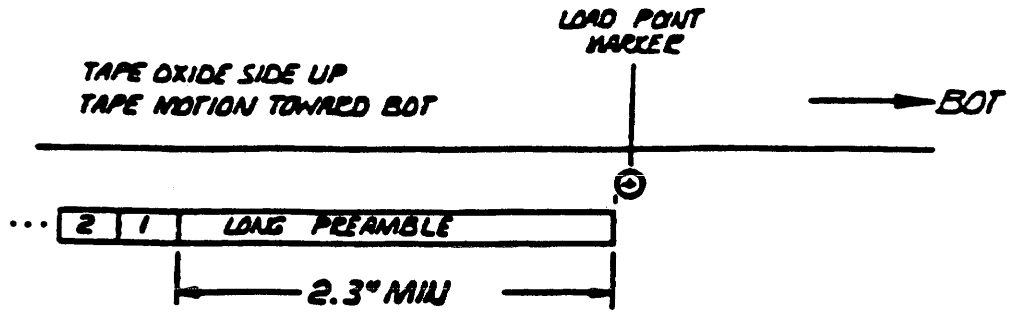
... N-1 N N ... N N ...

9.1.7 Beginning of Tracks

9.1.7.1 Even Tracks

A long preamble of 2.3 in minimum length is recorded after the load point marker and before the first data block for interchange on all even numbered tracks. It is permissible to substitute redundant data blocks for long preamble.

FIGURE 16.0 EVEN TRACKS



9.1.7.2 Odd Tracks

A long preamble of 4.0 in minimum length is recorded before the early warning marker on odd numbered tracks. A long preamble of 0.3 in minimum length is recorded after the early warning marker and before the first data block for interchange on odd tracks. It is permissible to substitute redundant data blocks for long preamble.

9.2 QIC-24 DATA FORMAT

9.2.1. Scope and Introduction

This section defines the QIC-24 format and recording standard for the streaming 0.250 in (6.30 mm) wide magnetic tape cartridge to be used for information interchange among information processing systems, communications systems and associated equipment. Compliance with the standard for the unrecorded magnetic tape cartridge (ref. ANSI X3.55-1977) is a requirement for information interchange.

9.2.2 Definitions

See Section 9.1.1

9.2.3 Recording

9.2.3.1 Method

See Section 9.1.2.1

9.2.4 Tracks

9.2.4.1 Number and Use of Tracks

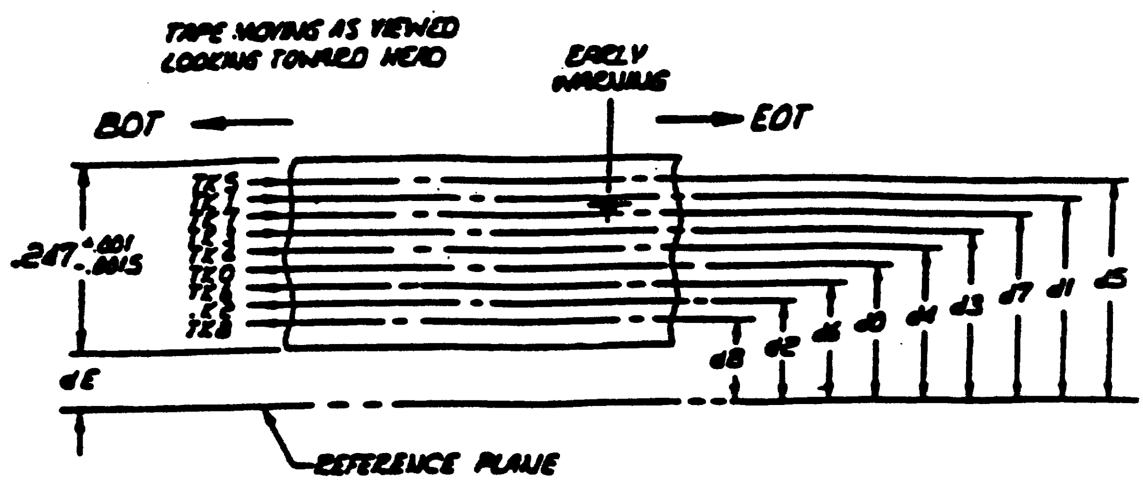
There are a maximum of nine tracks numbered 0 through 8 as specified in 9.2.4.3. Even numbered tracks are recorded serially in the forward direction of tape movement. Odd numbered tracks are recorded serially in the reverse direction of tape movement. On even tracks, all data for interchange is recorded after the load point marker and before the end of tape marker. On odd tracks 3 and 5, all data for interchange is recorded after the early warning marker and before the beginning of tape marker. However, on tracks 1 and 7, all data for interchange is recorded between the early warning marker and the load point marker. Tracks are recorded sequentially in the order, 0, 1, 2, . . . 8.

9.2.4.2 Reference Plane

The reference plane of the magnetic tape cartridge base is the datum for track location.

9.2.4.3 Track Center Line Locations

Track center lines are located as indicated below:



d0 = 0.172 ±.0042 in
d1 = 0.268 ±.0042 in
d3 = 0.124 ±.0042 in
d4 = 0.220 ±.0042 in
d5 = 0.196 ±.0042 in
d6 = 0.292 ±.0042 in
d7 = 0.244 ±.0042 in
d8 = 0.100 ±.0042 in
dE = 0.070 in reference

FIGURE 17.0 TRACK CENTER LINE LOCATIONS

9.2.4.4 Track Width for 0.048 In Track Spacing

When an 0.048 in track spacing is used, the number of recorded tracks is limited to a maximum of four tracks. The width of the recorded track is 0.036 $\pm$0.002 inches. The width of the verified recorded track (read after write) is 0.020 $\pm$0.001 inches.

9.2.4.5 Track Width for 0.024 in Track Spacing

When an 0.024 in track spacing is used, all nine tracks may be recorded. The width of the recorded track is 0.0135 $\pm$0.0005 inches. The verified recorded track width (read after write) is 0.0165 $\pm$0.0005 inches.

9.2.4.6 Interchange Between 0.048 and 0.024 in Track Spacing

Magnetic tape cartridges recorded with the 0.048 in track spacing provide data interchange with magnetic tape cartridges with the 0.024 in track spacing where the recording has been limited to tracks 0 through 3.

NOTE: Nominal signal amplitudes may be reduced due to narrower track width.

9.2.5 Data Block

The data block format is as follows:

```
+----/ /----+---+--------/ /-------+-------+---+---------+
!           ! 1 !                  !   4   ! 2 !         !
! See       !   !                  !       !   ! See     !
!           ! B !                  !   B   ! B !         !
! Section   ! Y !    512 BYTES     !   Y   ! Y ! Section !
!           ! T !                  !   T   ! T !         !
! 5.1       ! E !                  !   E   ! E ! 5.6     !
!           !   !                  !   S   ! S !         !
+----/ /----+---+--------/ /-------+-------+---+---------+
!___________! ! !__________________!   !      !      !
      !       !           !            !      !      !
      !       !           !--DATA      !      !   POSTAMBLE
      !       !                        !      !
      !       !--DATA BLOCK MARKER     !      !--CRC
      !                                !
      !--PREAMBLE                      !--BLOCK ADDRESS
```

FIGURE 18.0 DATA BLOCK

FIGURE 19.0 BLOCK ADDRESS

```
         0                1                        2              3
 ____________________________________________________________________
 :               :              :           :            :          :
 :     Track     :   Control    :           :            :          :
 :    Address    :   Nibble     :           :            :          :
 :               :              :           :            :          :
 ____________________________________________________________________
                                :                                   :
                                :- - - - - - -  Block Address  - - -:
```

BYTE	BITS	FUNCTION
0	7	Track Number Bit 7 (MSB)
	6	Track Number Bit 6
	5	Track Number Bit 5
	4	Track Number Bit 4
	3	Track Number Bit 3
	2	Track Number Bit 2
	1	Track Number Bit 1
	0	Track Number Bit 0 (LSB)
1	7	Control Nibble Bit 3 (MSB)
	6	Control Nibble Bit 2
	5	Control Nibble Bit 1
	4	Control Nibble Bit 0 (LSB)
	3	Block Address Bit 19 (MSB)
	2	Block Address Bit 18
	1	Block Address Bit 17
	0	Block Address Bit 16
2	7	Block Address Bit 15
	6	Block Address Bit 14
	5	Block Address Bit 13
	4	Block Address Bit 12
	3	Block Address Bit 11
	2	Block Address Bit 10
	1	Block Address Bit 9
	0	Block Address Bit 8
3	7	Block Address Bit 7
	6	Block Address Bit 6
	5	Block Address Bit 5
	4	Block Address Bit 4
	3	Block Address Bit 3
	2	Block Address Bit 2
	1	Block Address Bit 1
	0	Block Address Bit 0 (LSB)

9.2.5.1 Preamble

9.2.5.1.1 Normal

The preamble contains a minimum of 120 and a maximum of 300 flux transitions recorded at the maximum normal recording density of 10,000 flux transitions per inch (394 flux transitions per millimeter). The preamble is used to synchronize the phase locked loop in the read electronics to the data frequency. The preamble is also used to measure the average preamble amplitude.

9.2.5.1.2 Elongated

An elongated preamble contains a minimum of 3500 and a maximum of 7000 flux transitions and precedes the first data block recorded after an underrun (7.2).

9.2.5.1.3 Long

A long preamble contains a minimum of 15,000 and a maximum of 30,000 flux transitions, and precedes the first data block for interchange recorded at the beginning of a track.

9.2.5.2 Data Block Marker

The data block marker identifies the start of data and consists of the following GCR pattern:

G4	G3	G2	G1	G0	G4	G3	G2	G1	G0
1	1	1	1	1	0	0	1	1	1
MS nibble					LS nibble				

9.2.5.3 Data Block

The data block contains 512 bytes of data for interchange encoded into GCR bytes in accordance with the CODE.

9.2.5.4 Block Address

The block address consists of 4 bytes which uniquely identify a block recorded on tape. The block address is encoded into GCR bytes in accordance with the CODE, and as defined in Figure 12.0.

9.2.5.4.1 Track Number

The track number as specified in Section 9.2.4.3 is recorded in byte 0.

9.2.5.4.2 Control Block

Definition of control block is as follows:

Control Nibble 3 2 1 0	Value	Meaning
0 0 0 0	0	The current block contains user data or file mark.
0 0 0 1	1	The current block contains control information.
0010-1111	2-15	Reserved

NOTE: The use of control blocks as defined herein is an optional feature. It is permissible for a device to recognize and process only blocks with control nibble=0 and to ignore all blocks with control nibble=1 and still meet the requirements for data interchange as specified herein.

9.2.5.4.3 Address of Block

The first block on the tape is block 1, and subsequent blocks are numbered sequentially. The block address does not reset at the end of a track.

9.2.5.4.4 Control Block Data Field (Optional)

When the control nibble equals 1, the current 512-byte date block contains control information. This control information is defined as follows:

BYTE	MEANING
0 (M.S.)	Drive Type 04H = 4-track device 09H = 9-track device

BYTE	MEANING
1	Type of Control Block 00H = None 01H = First block on a track. 02H = Last block on a track. This block may be used to terminate a completed track. 03H = Extended file marks. 04H = Partial block count. This indicates that bytes 2 and 3 specify the number of valid data bytes in the following data block. In the data block, the valid data bytes are recorded first, followed by filler characters. 05-1FH = Reserved. 20-FFH = Not defined.
2	File Mark Number (MSB), or number of data bytes (MSB) in the partial block.
3	File Mark Number (LSB), or number of data bytes (LSB) in the partial block.
4-OF	Reserved (Set to 00H)
10-1FF	Not defined in this document.

NOTE: The use of the partial block option will generate a recorded tape which does not meet the requirements for data interchange at the minimum machine level (QIC-24 with no options).

9.2.5.5 Cyclical Redundancy Check

The cyclical redundancy check (CRC) consists of two bytes calculated over the 512-bytes of interchange data and the 4-byte block address starting with all ones CRC initial value and using the CRC generating polynominal:

$$X^{16} + X^{12} + X^{5} + 1$$

The CRC is encoded into GCR bytes in accordance with Code.

9.2.5.6 Postamble

9.2.5.6.1 Normal

A normal postamble with a minimum of 5 and a maximum of 20 flux transitions, recorded at the maximum nominal flux density is recorded following the CRC as a guard band.

9.2.5.6.2 Elongated

An elongated postamble with a minimum of 3,500 and a maximum of 7,000 flux transitions, recorded at the maximum nominal flux density, is recorded following an underrun sequence.

9.2.6 File Mark Block

The file mark block format is identical to the data block format except that the data field contains 512 bytes consisting of the following GCR pattern:

G4	G3	G2	G1	G0	G4	G3	G2	G1	G0
0	0	1	0	1	0	0	1	0	1
MS nibble					LS nibble				

The GCR nibble (00101) is converted to the HEX nibble (1111) to form the data field for CRC generation and checking.

9.2.7 Rewritten Blocks

9.2.7.1 Error

Data for interchange, if written such that all requirements for interchange are not met, is rewritten such that requirements for data interchange are met. Each data and file mark block that do not meet the requirements for interchange is rewritten. A data and file mark block is tested for interchange requirements during the read after write check. Writing of block N + 1 begins before the read after write check of block N is completed. If block N satisfies the requirements for interchange, the read after write check of block N + 1 is begun. However, if block N does not satisfy the requirements for interchange, it is rewritten after the writing of block N + 1 is completed. It shall be permissible to truncate the writing of block N + 1 with postamble before rewriting block N. Block N + 1 is alsorewritten after block N in order to preserve the sequential order of records. During error processing of block N, it is permissible to rewrite block N without rewriting block N + 1. A Block in Error shall be written up to 16 times before the recording operation is aborted. Various sequences of rewritten blocks are shown below.

... N-1 N N+1 N N+1 N+2 ...

... N-1 N N N N+1 ...

... N-1 N N+1 N N N+1 N+2 ...

9.2.7.2 Underrun, End of File, or End of Track

Streaming operation is normally terminated when underrun, end of file, or end of track conditions exist. The normal sequence of recording of blocks N, N + 1, etc., is replaced by the sequence of blocks N, N, etc., until the recording of block N meets the requirements for interchange. When block N is recorded such that the requirements of interchange are met, the associated rewriting of block N is completed or truncated. An elongated postamble (Section 8.2.5.6.2) is written as shown below.

```
...   N-1   N    N    ///////
                         :
                         :--Elongated Postamble
```

Recording in the elongated postamble at 3000 flux transitions minimum, 3500 flux transitions maximum from the end of the block preceding the elongated postamble. An elongated preamble is recorded before recording any other field in the block.

```
                                   : --Elongated Postamble
                                   :
                                   :
                                   :
...   N-1   N    N    ////   X   \\\\   ...
                       :     :
                       :     :
                       :     :--Overlap
                       :
                       :           :
                       :           :
3000 Flux Transitions MIN.-- :     :
3500 Flux Transitions MAX.         : --Elongated Preamble
```

9.2.7.3 Forced Streaming

Termination of streaming operation due to underrun may optionally be prevented by continued recording of the last block until end of file or end of track occurs. Standard length format fields are used during forced streaming operation.

9.2.7.4 End of Recorded Data

On other than the last track, the end of recorded data is indicated by a valid file mark block and optional control blocks followed by a minimum of 45 inches of erased track.

9.2.8 Recorded Tracks at Beginning and End of Tape

9.2.8.1 Reference Burst

A Track reference burst recorded at the maximum nominal recording density of 10,000 flux transitions per inch (394 flux transitions per millimeter) is written between the BOT holes and recorded data on Track 0. The reference burst starts a minimum of 0 inches and a maximum of 15 inches from the BOT hole and extends past the load point hole for a minimum of 3 inches and a maximum of 4 inches. A long preamble precedes the first data block.

9.2.8.2 Even Tracks

All even tracks start a minimum of 3 inches and a maximum of 4 inches past the load point hole. A long preamble precedes the first data block for interchange. On even tracks, no data for interchange is recorded beyond a point 36 inches past the early warning hole.

9.2.8.3 Odd Tracks

All odd tracks start a minimum of 1 inch and a maximum of 2 inches past the early warning hole. A long preamble precedes the first data block for interchange. On tracks 1 and 7, no data for interchange is recorded past the load point hole. The last block of data for interchange written on these tracks prior to track switching to the next sequential track ends a maximum of 4 inches and a minimum of 0.1 inch before the load point hole is measured from the center line of the hole. On tracks 3 and 5 it is permissible to record data for interchange past the load point hole. No data for interchange is recorded beyond a point 27 inches past the load point hole.

10.0 COMMAND SEQUENCE DESCRIPTION

All commands are initiated by the host, and share the same initial sequence of events. The events following acceptance of the command depend upon the specific command issued, and the current status of the controller and drive. This section should also be referred to Command Timing, Section 8.0.

10.1 COMMON COMMAND SEQUENCE

The following commands must be preceded by asserting ONL- (Online):

Read Data
Read File Mark
Write Data
Write File Mark

ONL- must remain asserted until all operation with the selected drive is completed. Deassertion of the ONL- signal during any of the above commands will result in the drive being deselected, and the tape being rewound to BOT.

Errors and completion of the Read Data and Read File Mark commands are indicated by the assertion of EXC- signal in place of the RDY-.

The sequence which takes place in response to a command is as follows:

1. The controller is in a state waiting for a command, and RDY- is asserted. If the "at-position" flag is set, and ONL- is not asserted, then the controller will deassert RDY-, and perform a BOT sequence described in Section 10.18 prior to reasserting RDY-.

2. If a Write Data, Write File Mark, Read Data, or Read File Mark command is issued, the host asserts ONL-.

3. The host places the command on the data bus and asserts REQ-.

4. The controller deasserts RDY-, reads the command, and reasserts RDY-to indicate that it has read the command.

5. The host removes the command from the data bus, and deasserts REQ-.

6. The controller deasserts RDY-.

7. The controller performs the command.

8. If the command is not valid, or if an error occurs, then the controller aborts the command, sets the appropriate status bits, and asserts EXC- to notify the host to initiate a Read Status command.

9. When the command is successfully completed, the controller asserts RDY.

The tape can be at either of two locations at the start of any operational sequences: at logical BOT, or "at-position" point where the tape was stopped by a previous operation.

In the "at-position" case, the controller firmware sets the "at-position" flag to indicate that any subsequent write or read operation should start with a repositioning sequence to locate the end of the data that has already been written, or read. The "at-position" flag is cleared if the cartridge is at BOT. Current status of the "at-position" flag is not included in the status information returned to the host in response to a Read Status command.

10.2 POWER-ON/RESET SEQUENCE

The power-on/reset sequence provides the host with information relating to power-on conditions with the controller. It also provides a convenient mechanism for initializing the controller during hardware, and software debugging of the host interface. The sequence is as follows:

1. The host applies power to the controller, or applies a pulse to the controller reset line.

2. The controller hardware asserts EXC-, and deasserts RDY-, DIR-, and ACK-.

3. Diagnostics are performed on ROM (checksum test), and RAM (read/write test). If either test fails, the controller will not proceed beyond the diagnostics. It is recommended that the host provide a long timeout (at least 1 second) to detect this failure.

5. Reset is applied to all drives and the controller waits a sufficient interval for them to initialize.

6. The controller initializes all internal parameters, sets default tape drive to Drive 0, and clears the "AT POSITION" flag.

7. The Power-on/Reset flag (POR) is set in the status bytes, and the controller waits for the host to issue a Read Status command. The above steps may require as long as a second to complete. The host should be prepared to wait for a status command response delay of this length.

10.3 SELECT COMMAND SEQUENCE

This command allows the host to select one of the maximum of four drives connected to the controller. Prior to selection of a new drive, the currently selected drive must be at BOT. Selection of a drive turns on the drive select LED. The light remains on until the drive is deselected through completion of one of the following operations; rewinding to BOT, or selection of another drive.

Once a drive has been selected, it will be remembered by the controller, even after it has been deselected. Operations following deselection will automatically default to the previously selected drive, unless another drive has been selected, and will reselect the drive. Reset will set the default unit to drive 0. The sequence of operation is as follows:

1. The host issues the Select command.

2. The controller checks to determine if the drive being deselected has its cartridge at BOT; otherwise selection is aborted by setting the Illegal command flag (ILL), and asserting EXC- to notify the host of the error. The BOM flag remains reset.

3. The controller asserts RDY- to indicate it has completed the command.

10.4 READ STATUS COMMAND SEQUENCE

This command provides the host with information about the controller and the selected drive. The sequence of operation is as follows:

1. If the controller has requested that the host read status, then EXC- will be asserted; otherwise RDY- is asserted.

2. The host issues the Read Status command.

3. The controller deasserts EXC-.

4. The controller selects the drive, and obtains the drive status.

5. The controller asserts DIR- and transfers six status bytes to the host using RDY-, and REQ- handshaking.

6. If the drive was selected when this command was issued, then it remains selected; otherwise, it is deselected.

7. The exception status flags, error counter, and underrun counter are cleared.

8. The controller deasserts DIRECTION and asserts READY.

10.5 REWIND TO BOT COMMAND SEQUENCE

This command allows the host to position the cartridge tape in the selected drive to the BOT position.

The sequence of operations is as follows:

1. The host issues the Rewind to BOT command.
2. If a drive is not already selected, then the last addressed drive is selected.
3. If the drive is not operational with a cartridge present then the operation is aborted. CNI-, and USL status is set and EXC- is asserted.
4. The controller selects Track 0, sets REV-, clears the at-position flag, and enables the tape drive motor.
5. The controller waits for an indication from the tape drive that the tape is at BOT.
6. When the BOT hole is detected, the tape is stopped. The drive then moves the tape back between the BOT, and LP holes.
7. The at-position flag is cleared.
8. The controller deselects the drive to turn its LED off. The BOM status is set. The controller indicates command completion to the host by asserting READY.

10.6 INITIALIZE (RETENSION) COMMAND SEQUENCE

This command is used by the host to retension a tape cartridge by winding the tape on the takeup reel and rewinding it to the supply reel at high speed.

Retensioning is recommended by cartridge tape manufacturers prior to writing or reading a cartridge that has been subjected to a change in environment, or not used for a prolonged period of time, or when drives are used in frequent start/stop applications. The sequence of operations is as follows:

1. The host issues the Initialization command.
2. If the drive is not already selected, then the last addressed drive is selected.
3. If a cartridge is not present, then the operation is aborted. The CNI status is set, and EXC- is asserted.

4. The at-position flag is cleared and the cartridge is positioned to BOT. This is accomplished by reversing tape motion until the BOT hole is detected.

5. The controller selects Track 0, HSD-, and REV for forward tape motion until it is positioned at EOT.

6. The controller selects HSD-, and REV- for reverse tape motion until the tape is positioned at BOT.

7. The tape is stopped, and the drive then positions the tape between the BOT, and LP holes.

8. The controller deselects the drive to turn its select LED off. Upon the completion of the command, BOM status is set, and RDY- is asserted to the host.

10.7 ERASE COMMAND SEQUENCE

This command is used to completely erase the tape before writing on it. It also performs a "retension" function. The sequence of operations is as follows:

1. The host issues the Erase command.

2. If the drive is not already selected, then the last addressed drive is selected.

3. If a cartridge is not present, or is present and write protected, then the operation is aborted, the CNI or WRP status bit is set accordingly, and EXC- is asserted.

4. The at-position flag is cleared and the cartridge is positioned to BOT. This is accomplished by reversing tape motion until the BOT hole is detected.

5. The controller selects Track 0, HSD-, and REV for forward direction, enables the erase head (EEN-), and positions to EOT.

6. The controller selects HSD-, REV- for reverse direction, disables the erase head, and positions the tape to BOT.

7. The tape is stopped, and the drive then positions the tape between the BOT, and LP holes.

8. The controller deselects the drive to turn the select LED off. Command completion is indicated to the host by the setting of the BOM status, and asserting of RDY-.

10.8 WRITE DATA COMMAND SEQUENCE

This command provides for the writing of sequential blocks of data to the tape. Blocks are transferred by the host to the controller where there are buffered, an then written to the selected drive. The sequence of operations is as follows:

1. The host asserts ONL-, and issues the Write Data command.

2. RDY- is asserted, indicating to the host that the controller is ready for data transfers from the host to the controller buffer.

3. The controller checks the at-position flag. If it is not set, a BOT sequence without deselection is performed. If the cartridge is write protected the WRP status is set, then the operation is aborted with EXC- asserted.

4. If the at-position flag is set, the Write Reposition sequence (described in section 10.11) is performed, and the recording of data begins at step #7 below. Otherwise, the controller enables the erase bar to erase the tape ahead of recording new data, initializing at Track 0.

5. The controller records the reference burst from the BOT hole to approximately 3.5-inches beyond LP hole on Track 0.

6. The controller records approximately 2.175-inches of long preamble.

7. The controller begins recording blocks of data on the tape, adding gap, sync, block, address, and CRC. Blocks are numbered sequentially beginning with one. The controller attempts to keep all buffers filled by initiating a block transfer as soon as a buffer becomes available.

8. As each block reaches the read head, it is checked for errors.

9. After a block has been read without error, its buffer is released for further data reception from the host.

10. Steps 7 through 9 are repeated until the EW hole (in forward) and the LP hole (in reverse) is detected. The controller then completes writing the current block and writes one more block of data.

11. The controller performs the Last Block sequence (described in section 9.10), turns the write head off, and continues until it reaches either EOT or BOT. The tape motion is stopped, and if writing Track 0, the erase bar is disabled. The data transfers from host to the controller are allowed during track turnaround.

12. The controller requests the transfer of the next three (or fifteen) data blocks, switches to the next track, resumes motion in the opposite direction, and positions to approximately 3.5-inches beyond LP (in forward), or 1.5-inches beyond EW (in reverse). Writing is then continued at step 7.

13. The host concludes the write data sequence at a block boundry when RDY- is asserted by issuing a Write File Mark command or asserting ONL-. These actions will result in the controller writing and checking the remaining blocks it has buffered, and then peforming a Write File Mark sequence (described in section 10.9). If ONL-was deassserted, then the controller will also perform a BOT sequence after writing the file mark, which will leave the current drive deselected.

14. If the host does not discontinue writing before the end of the last track is encountered, then the controller performs an End-of-Media sequence as follows:

    a. The EW hole on Track 8 is encountered since the tape is positioned at the end of the last track.

    b. The controller ceases to accept additional data blocks from the host and completes writing the current block.

    c. The controller set EOM, asserts EXC- to alert the host, and returns to a command state to wait for the host to issue a Read Status.

    d. After reading the status, the host can issue a WRITE or WRITE FILE MARK command. The controller will write two additional blocks of data (or Filemark) after detecting EOM. However, it will assert EXCEPTION after each block.

15. It is the responsibility of the host to keep the controller streaming by supplying it with data at an appropriate rate. If a full block is not available when it is time to start writing a new block, then the following steps occur:

    a. The buffer underrun counter is incremented.

    b. The controller concludes writing by performing a Last Block sequence. If a full buffer is available before the conclusion of checking the last block, then writing continues at step #7 with a single block having been written.

c. If tape motion is stopped, the controller waits for the host to send it three (or fifteen) data blocks. When they have been received, a Write Reposition sequence is performed.

10.9 WRITE FILE MARK COMMAND SEQUENCE

This command will generate a standard length data block with unique codes in the user data field. The sequence of operations is as follows:

1. The host asserts ONL- and issues the Write File Mark command.

2. The controller checks the at-position flag. If it is set, a Write Reposition sequence without deselection is performed. Otherwise, a BOT sequence without deselection is performed.

3. The controller generates a file mark block, and writes it to tape.

4. A Last Block sequence is performed, which again writes the file mark, an extended postamble, and if on Track 0, erases 45-inches of tape.

5. The host is notified of the command completion by the controller asserting RDY-, and returning to the command state.

10.10 LAST BLOCK SEQUENCE

The last block sequence is performed by the controller during Write Data and Write File Mark commands to record the final data block (or file mark) on the tape. The sequence of operations is as follows:

1. The read channel is read, checking the last block.

2. The write channel finishes writing the last block, and commences to rewrite the last block.

3. The read channel finishes re-checking the last block. If the block is in error, then the block must be rewritten. This involves incrementing the rewritten block counter. If less than 16 retries have been made, then repeat step 2 to rewrite the block again; otherwise, the writing is aborted.

4. The read channel commences to read, but not to check the final block.

5. The write channel finishes writing the rewritten last block and starts writing the postamble.

6. The read channel finishes reading the rewritten block and reads two milliseconds of postamble, the write head is turned off.

7. If a file mark is being written on Track 0, then the erase bar is left enabled and 45-inches of tape is erased (or EOT is reached).

8. Unless recording the last block at the end of other than the last track, the at-position flag is set, the erase bar is disabled, and the tape is stopped.

10.11 WRITE REPOSITION SEQUENCE

This sequence is performed during execution of Write Data and Write File Mark commands to continue writing after the tape has been stopped and the at-position flag is set. The sequence of operations is as follows:

1. The controller causes the tape to reverse direction, and tape is moved 20-inches (80-inches for more than two consecutive repositions) or to the upper warning hole at the start of the track.

2. The controller selects the original direction, starts the tape motion, and delays approximately 4.0-inches of tape movement.

3. The controller searches for block N-1 (last block rewritten) as follows:

   a. Each block is read and its CRC is checked. If it contains a valid CRC, then its address is checked. Reading continues until a record with an address equal to N-1 is located, or until 20-inches of tape passes without reading data.

   b. If no data is detected, then two additional attempts are made to locate block N-1 by returning to step 1 above.

   c. If the block cannot be located, a write abort is performed by initiating a BOT sequence, setting the BNL flag, asserting EXC-, and returning to the command state.

4. The controller searches for the extended postamble written by the Last Block sequence. If 20-inches of tape pass without detecting a gap, return to step 1 above.

5. When the controller detects 1 millisecond of postamble, the write head is enabled. If recording on Track 0, then the erase head is enabled.

6. An extended postamble of .58-inches is written.

7. The controller resumes writing.

10.12 WRITE ERROR SEQUENCE

Due to the excessive time it takes to reposition a tape, write errors are corrected "on-the-fly", by rewriting the data until it is written and read correctly. Since the read head follows the write head by 0.3-inches, and the inter-record gap is only 0.013-inches, the controller must begin writing the next record (N+1) prior to the preceding record (N) can be checked. When an error is detected, both records N and N+1 must be rewritten. Read-after-write check error is processed as follows:

1. The read channel finishes reading block N, and it has a CRC error.

2. The rewritten blocks count is incremented by 2.

3. If 16 attempts have been made to rewrite this block, then the write operation is aborted. This is accomplished by disabling the erase bar, write head, and stopping tape. A BOT sequence is then performed. The UDA flag is set, EXC- is asserted, and the controller returns to the command state waiting for the Read Status command.

4. The controller begins reading, but not checking block N+1.

5. The controller finishes writing block N+1 and begins rewriting block N.

6. The read channel finishes reading block N+1 and starts reading and checking block N.

7. The controller completes writing and begins rewriting block N+1.

8. The read channel finishes reading block N. If the error occurs again, the above procedure is repeated until the 16 retry limit is exceeded, or a successful read occurs.

9. A successful read enables the continuation of the process. If an end of track is detected during the process it is ignored, and is processed normally upon successful completion of this procedure.

10.13 READ DATA COMMAND SEQUENCE

This command provides for the reading of sequential blocks of data from tape. Data is read from the selected drive, checked, and buffered by the controller. The host then transfers the data to its memory for processing.

The sequence of operations for the Read Data command is as follows:

1. The host asserts ONL-, and issues the Read Data command.

2. The controller checks the at-position flag. If it is set, then a Read Reposition sequence (section 10.15) is performed, and the reading of data commences. Otherwise, a BOT sequence without deselection is performed.

3. The controller causes the tape to move forward, until it passes LP, and then begins searching for the first data block.

4. The controller reads the entire data block to the read buffer, and checks the CRC, and block address. CRC and sequence errors are processed (as described in section 10.17). If the controller does not read data within 20-inches of tape, it performs a No Data sequence (described in section 10.16).

5. If the CRC and block address are good, then the block is stored in the FIFO queue, and RDY- is asserted to initiate the transfer to the host. After each block is transferred, its buffer is made available for reading. The controller can retrieve two (or fourteen) whole blocks ahead of the host.

6. Steps 4 and 5 are repeated until either the EOT hole, on even tracks, or BOT hole, on odd tracks are encountered, at which point the following procedure is initiated:

   a. The tape is stopped, and direction is reversed.

   b. Tape is advanced past the LP on even tracks, or the EW hole on odd tracks.

   c. Search for the first block on the track is initiated.

   d. Operation resumes at step 4 above.

7. Reading is terminated when a File Mark is detected. At this point, tape motion is stopped, and the at-position flag is set. Any remaining blocks of data buffered by the controller are transferred to the host. The controller then sets FIL status flag, asserts EXC- to alert the host, and returns to the command state.

8. When the controller is at a block transfer boundary, and RDY- is asserted, the host may terminate the Read Data command by deactivating ONL-. In this case, the controller terminates data transfer immediately. Any remaining buffers are ignored. RDY- is deasserted and a BOT sequence is performed. RDY- is reasserted and the controller returns to the command state for further direction from the host.

9. The host may alternatively terminate the Read Data command by issuing a Read File Mark command at the beginning of a data block transfer sequence when RDY- is asserted. In this case, the controller terminates data transfer on the next block boundary. No further data will be transferred. A Read File Mark sequence (described in section 10.14) is then performed.

10. The host must accept transfer of blocks fast enough to keep the tape streaming or it will stop. This occurs when the host falls two (or fourteen) blocks behind. If this occurs, the buffer underrun counter is incremented, and the tape is stopped. The controller then waits for the host to complete transfer of all blocks it has queued. The controller then performs a Read Reposition sequence, and resumes at step 5.

10.14 READ FILE MARK COMMAND SEQUENCE

The Read File Mark command is used to position the tape to the next file mark. The sequence of operation is as follows:

1. The host asserts ONL- and issues the Read File Mark command.

2. The controller checks the at-position flag. If it is set and the previous operation was a Read Data sequence, then a Read Reposition sequence is performed, and processing skips to step 4 below. Otherwise, a BOT sequence without deselection is performed.

3. The controller then starts forward, waits for the LP hole to pass, and searches for the first data block.

4. The controller reads the entire data block to the read buffer, and checks the CRC and block address. If the controller does not read data within 20-inches of tape, it performs a No Data sequence. CRC and block address sequence errors are processed by a Read Repositioning sequence until a successful read is attained, or until it reaches the 16 retry limit, at which point it aborts the read operation.

5. If the CRC and block are good, then the block is checked to determine if it is a file mark. Data is not transferred to the host.

Reading is terminated by the controller when a file mark is detected by stopping the tape and setting the at-position flag. The controller then sets the FIL status flag, asserts EXC- to alert the host, and returns to the command state to await a Read Status command.

6. Steps 4 and 5 are repeated until the EOT hole (even tracks), or BOT hole (odd tracks) are encountered. The sensing of either of the holes causes the tape to be stopped, and direction reversed. Then the tape is advanced past the LP (even tracks), or EW (odd tracks) in search of the first data block on the track. Operation then resumes at step 4.

7. The host may terminate the Read File Mark command at any time by deasserting ONL-. A BOT sequence will be performed and the controller will assert RDY-, and return to the command state.

10.15 READ REPOSITION SEQUENCE

The Read Reposition sequence is initiated during Read Data or Read File Mark operations to restart reading a tape with block N after the tape has been stopped. Block N-1 is the last block read. This requires the tape to be backed-up and rereading the last block processed. The sequence of operations is as follows:

1. Tape motion is started in the reverse direction.

2. Tape is reversed 20-inches (80-inches if two or more consecutive retries or a no data timeout have occurred) or until EOT or BOT holes are sensed.

3. Tape is stopped and restarted in its normal read direction, 0.7-inches of tape is skipped (or until warning holes are sensed), and reading is enabled.

4. Blocks are read and checked. If the block contains a valid CRC, then its address is checked. If block N+2 is found, control is returned to the calling sequence with block N+2 in the read buffer. This will result in a read error sequence being performed. CRC errors are ignored. If a block is not read within 20-inches of tape motion, then a No Data sequence is initiated. Reading continues until block N is read.

5. After block N is found, control is returned to the calling sequence with block N in its buffers.

10.16 NO DATA SEQUENCE

The No Data sequence is initiated by the Read Data and Read file Mark command sequences whenever 20-inches of tape have passed while waiting to read without recovering a block. The sequence of operations is as follows:

1. The controller has failed to recover a block within 20-inches of tape motion.

2. The controller causes the tape to be moved back an additional 80-inches (or to a warning hole), and reverses the tape motion in an attempt to read again. If successful, then control is returned to the calling sequence.

3. The controller then asserts the NDT flag, assert EXC- to alert the host, and returns to the command state awaiting the Read Status command.

10.17 READ ERROR SEQUENCE

The Read Error sequence is invoked by the Read Data and Read File Mark command sequences when a block is read with an invalid CRC, or block address.

The control nibble of the data format must be 0 for all data blocks and file marks. Blocks with a non-zero control nibble will be ignored, but must contain a valid track and block address.

If block N contains an error, 15 retries will be made to read this block. If the block cannot be read with 16 retries, then a "hard" error indication is returned to the host. Data written to tape may be in error repeatedly, thus causing a search for a valid block N, until block N+2 is read. When block N+2 is encountered, tape motion is reversed, and then again read forward searching for a valid block N.

The sequence of operations is as follows:

1. The controller reads the next data block. If a data block is not read within 20-inches, skip to step 4.

2. If the data block contains a valid CRC and the correct block address, and if the retry counter is less than 16, then control is returned to the calling sequence without error.

3. If the data block is in error or is block N+1, then it is skipped and step 1 is repeated.

4. If the block address is greater than N+1, or a no data timeout has occurred, than a retry is initiated as follows:

a. If the retry counter is at 15, the operation is concluded by skipping to step 5.

b. If this is the first retry, then the Error Counter status bytes are incremented.

c. Tape is repositioned by reversing 20-inches (80-inches if two or more consecutive retries have occurred). If BOT or EOT is sensed, tape is again reversed, and moved 1.75-inches beyond LP (even tracks), or 4.35-inches beyond EW (odd tracks).

d. The balance of the 20-inches (or 80) are backed up. Control is then transferred to step 1 above.

5. After 16 retries to read a block in error, a "hard" read error is returned to the host. This is done by first stopping the tape. The last block read in error is buffered by the controller (unless this sequence was entered from a Read File command in which case the UDA flag is set, and EXC- is asserted). The UDA and BIE flags are set and EXC- is asserted to notify the host. The controller returns to the command state awaiting a Read Status command.

10.18 BEGINNING-OF-TAPE SEQUENCE

The BOT sequence allows the host to position the tape in the selected drive at the start of Track 0. The sequence of operations is as follows:

1. The host verifies that RDY- is true, places the rewind to BOT command on the bus, then asserts REQ-.

2. Drive reset RDY- and after reading the command, again sets RDY- to its true state to indicate the completion of the command.

3. Host resets REQ-, and removes the command from the bus. The drive completes the handshake by reasserting RDY-.

4. When the command has been validated the drive selects HSD-, sets reverse direction, clears the at-position flag, enables the capstan motor, and rewinds the cartridge to BOT.

5. The drive asserts RDY- to the host indicating completion of the command.

6. Drive is deselected if the select command selects another device.

11.0 PROGRAMMING GUIDE

This section describes programming tips to interface to the PC-36 controller. Prior to proceeding with this section, the user should thoroughly review Sections 5.1, 6.0, 7.0, 8.0 and 10.0.

11.1 Command Transfer

Commands are transferred by sending a desired command to the command port. However, prior to issuing a command, the host must first check for READY to be true. After READY is checked and the command is written to the command port, the host issues a REQUEST. REQUEST indicates to the controller that a command is on the bus, and the host now waits for the controller process. READY becomes deasserted and asserted again to indicate that the controller has accepted the command and that the host should remove REQUEST. Next READY will depend upon what command is being processed, but is typically remains deassetted until a command is completed. Refer to Section 8.0 for various command timings. Also, refer to "command" procedure in the following sample code.

11.2 Write/Read Operation

Sending a write/read operation is the same as the above, however, there are additional parameters to consider. Refer to "write/read data" in the sample code.

1. ONLINE must be asserted prior to sending a command and it must remain asserted until read/write operation is completed. Refer to "comwtrd" in the sample code.

2. The DMA must be set and started after the command has been sent. Refer to "writedata" and "readdata" in the sample code.

3. The DMA must be disabled when the DMA operation is completed or an EXCEPTION occurs before reading the status or issuing another command.

11.3 DMA Operation

The DMA must be set and started prior to any data transfer operation. The procedure is as follows. Refer to "setdma" in the sample code.

1. Get the address of the memory where data is stored, then generate a twenty bit address for the starting location.

2. Output the low 16 bits order of the address to the address port on the DMA chip, and then the high 4 bits order of the address to the page register.

3. Output the write/read mode to the mode register.

4. Output the number of bytes to be transferred to the count register. The number should be 512 bytes.

5. Enable the DMA bit of the channel 1 on the PC-36 controller by sending the bit 3 on the control port to be true. Refer to Section 5.1.2.2.

6. Reset the status register by reading the status port on the DMA chip.

7. Enable DMA channel 1 by sending the channel 1 number to the mask register on the DMA chip.

11.4 SAMPLE CODE

(Pages 84 through 90.)

```
###########################################################################
##  SAMPLE PROCEDURES TO DO MAJOR TAPE DRIVE COMMANDS                   ##
##  COPY RIGHT WANGTEK INC.                                              ##
###########################################################################

#define S_RDY 0x01                /* ready     status bit          */
#define S_EXC 0x02                /* exception status bit          */
#define S_DIR 0x04                /* direction status bit          */

#define ONL     0x01              /* offset for online  line output */
#define RESET   0x02              /* offset for reset line output   */
#define REQ     0x04              /* offset for request line output */
#define DMA12   0x06              /* offset for dma request 1 & 2   */
#define DMA3E   0x08              /* offset for dma request 3       */
#define CLR     0x00

#define STATUSREG    0x300        /* offset for status port         */
#define CONTROLREG   0x300        /* offset for control port        */
#define DATAREG      0x301        /* offset for data port           */
#define COMMANDPORT 0x301         /* offset for command port        */

#define READ_STAT 0xc0            /* read status command byte       */
#define REWIND    0x21            /* position BOT command byte      */
#define ERASE     0x22            /* erase command byte             */
#define RETENSION 0x24            /* retension command byte         */
#define SELECT    0x01            /* select command byte            */
#define WRITE     0x40            /* write command byte             */
#define WRITEFM   0x60            /* write file mark command byte   */
#define READ      0x80            /* read command byte              */
#define READFM    0xa0            /* read file mark command         */

#define DMAWT     0X49            /* write command on the dma chip  */
#define DMARD     0x45            /* read command on the dma chip   */

#define TRUE      1
#define FALSE     0
#define ESCAPE    0x1b

extern int online;              /* variable to idicate if only is on or off */
extern int cmd;                 /* the command that is being procced        */
extern int srb[6] ;             /* 6 status bytes                           */


/**************************************************************************.
/** Routine name:        command                                        **.
/** Description:         put the specified command on the bus and send it **.
/**************************************************************************.
command()
{
rdy_0();                              /* wait for ready                  */
outportb(CONTROLREG,CLR+online);      /* keep online and clear the other */
outportb(COMMANDPORT,cmd);            /* put command on bus              */
outportb(CONTROLREG,REQ+online);      /* set request                     */
rdy_0();                              /* wait ready                      */
outportb(CONTROLREG,CLR+online);      /* reset request                   */
rdy_1();                              /* wait not ready                  */
do                                    /* wait for ready or exception     */
  {
  if (chkrdy())
    break;
  if (chkexc())
    break;
   }
```

```
while(TRUE);
}

/*************************************************************************
/** Routine name:       comwtrd                                          **
/** Description:        put the specified write or read command on the bus **
/**                     and send it to the drive and keep online true.   **
/*************************************************************************
comwtrd()
{
rdy_0();                                /* wait for ready               */
online=ONL;                             /* set online                   */
outportb(CONTROLREG,online);            /* output online                */
outportb(COMMANDPORT,cmd);              /* put command on bus           */
outportb(CONTROLREG,REQ+online);        /* set request and add online   */
rdy_0();                                /* wait ready                   */
outportb(CONTROLREG,online);            /* reset request but keep online */
rdy_1();                                /* wait not ready               */
}

/*************************************************************************
/** Routine name:       reset                                            **
/** Description:        reset the tape drive                             **
/*************************************************************************
reset()
{
int i;
cmd=RESET;
online=CLR;
outportb(CONTROLREG,cmd);          /* reset line true      */
for (i=0; i<100; i++);             /* delay at least 25us */
rdy_1();                           /* wait for not ready   */
do                                 /* wait fo rexception   */
  {}
while(!chkexc());
outportb(CONTROLREG,online+CLR);   /* reset line false     */
}

/*************************************************************************
/** Routine name:       readstatus                                       **
/** Description:        read the status and display it                   **
/*************************************************************************
readstatus()
{
int  i;
cmd=READ_STAT;                          /* set the read status command  */
outportb(COMMANDPORT,cmd);              /* put command on bus           */
outportb(CONTROLREG,REQ+online);        /* set request and add online   */
rdy_0();                                /* wait ready                   */
outportb(CONTROLREG,online);            /* reset request but keep online */
rdy_1();                                /* wait not ready               */
do
   {}
while(!chkrdy());
for (i=0; i<6; i++)
   {
    rdy_0();                            /* wait ready     */
    srb[i]=inportb(DATAREG);            /* set the status */
    outportb(CONTROLREG,REQ+online);    /* set request    */
    rdy_1();                            /* wait not ready */
    outportb(CONTROLREG,online);        /* reset request  */
    }
}
```

```
/*****************************************************************************
/** Routine name:        rdp                                                **
/** Description:         read status port and return the value              **
/*****************************************************************************
rdp()
{
int sport;                                  /* variable to return the status */
sport=inportb(STATUSREG) & 0x0f;            /* status port value             */
return(sport);
}

/*****************************************************************************
/** Routine name:        retension                                          **
/** Description:         send the retantion command                         **/
/*****************************************************************************
retension()
{
cmd=RETENSION;              /* set the retension command */
command();                  /* send the command          */
}

/*****************************************************************************
/** Routine name:        erase                                              **
/** Description:         send the erase command                             **
/*****************************************************************************
erase()
{
cmd=ERASE;                  /* set the erase command  */
command();                  /* send the command       */
}

/****************************************************************************/
/** Routine name:        rewind                                             **/
/** Description:         send the rewind command                            **
/*****************************************************************************
posbot()
{
cmd=REWIND;                 /* set the rewind command */
command();                  /* send the command       */
}

/****************************************************************************/
/** Routine name:        select                                             **/
/** Description:         send the select command                            **/
/****************************************************************************/
select()
{
cmd=SELECT;                 /* set the select command  */
command();                  /* send the command        */
}

/****************************************************************************/
/** Routine name:        writefm                                            **/
/** Description:         send the write file mark command                   **/
/*****************************************************************************
writefm()
{
cmd=WRITEFM;                /* set the write file mark command */
online=ONL;                 /* set online                      */
command();                  /* send the command                */
}
```

```
/*****************************************************************************
/** Routine name:        readfm                                              *
/** Description:         send the read file mark command                     **
/*****************************************************************************
readfm()
{
cmd=READFM;              /* set the read file mark command */
online=ONL;              /* set online                     */
command();               /* send the command               */
}

/*****************************************************************************
/** Routine name:        writedata                                           **
/** Description:         write the given data on the tape                    **
/*****************************************************************************
writedata()
{
unsigned long *buffptr;  /* a pointer to the buffer area        */
cmd=WRITE;               /* set the write command               */
comwtrd();

setdma(DMAWT,buffptr);   /* set the dma to write and start it   */
 do                      /* cheak for termal count or exception */
  {}
 while (!(chkwci() || chkexc()));
 disabledma();           /* diable the dma                      */
 if (chkexc())           /* if there is exception then quit     */
  {
   break;
  }
}

/*****************************************************************************
/** Routine name:        readdata                                            **
/** Description:         read the specified data from the tape               **
/*****************************************************************************
readdata()
{
 unsigned long *buffptr; /* pointer to a buffer area */
 cmd=READ;               /* set the read command     */
 comwtrd();              /* send the read command    */
 setdma(DMARD,buffptr);  /* set the dma for read operation and start the dma *
   do                    /* wait for termal count or exception               *
     {}
   while (!(chkwci() || chkexc()));
   disabledma();         /* disable the dma                                  *
   if    (chkexc())      /* if there is exception then quit                  *
    {
     break;
    }
}

/*****************************************************************************
/** Routine name:        chkrdy                                              **
/** Description:         check if the ready bit is on                        **
/*****************************************************************************
chkrdy()
{
return(!(inportb(STATUSREG) & S_RDY));
}

/*************************/
/*** wait for not ready ***/
```

```
/***************************/
rdy_1()
{
 do
  {}
 while (chkrdy());
}

/***********************/
/*** wait for ready  ***/
/***********************/
rdy_0()
{
 do
  {}
 while (!chkrdy());
}

/*************************************************************************
/** Routine name:       chkexc                                          **
/** Description:        check if the exception bit is on                **
/*************************************************************************
chkexc()
{
return(!(inportb(STATUSREG) & S_EXC));
}

/*************************************************************************
/** Routine name:       chkdir                                          **
/** Description:        check if the direction bit is on                **
/*************************************************************************
chkdir()
{
return(!(inportb(STATUSREG) & S_DIR));
}

/*************************************************************************
/** Routine name:       Chkwci                                          **
/** Description:        Read the status resister on the 8237 and return **
/**                     true if the bit in channal 1 is set.            **
/*************************************************************************
chkwci()
{
return(inportb(0x8) & 0x2);
}

/*************************************************************************
/** Routine name:       Disabledma                                      **
/** Description:        disable the dma chip (8237) and the everex board **
/**                     dma bit.                                        **
/*************************************************************************
disabledma()
 {
 outportb(0xa,5);                     /* Disable dma channal 1 on 8237 */
 outportb(CONTROLREG,online);         /* Disable dma but keep online */
 }
```

```
data     segment word public
         public  setdma
mode     db      0
data     ends

channal  equ     1h
pageres  equ     83h
statres  equ     8h
addport  equ     2h
cntport  equ     3h
strport  equ     0ah
cmdport  equ     0bh
initport equ     0ch

code     segment byte public
         org     100h
         assume  cs:code,ds:data
         public  setdma

setdma   proc    near
         pop     di                 ;pop return address
         pop     cx                 ;pop the mode
         pop     bx                 ;pop the address offset

         cli                        ;disable interupt
         mov     mode,cl            ;save the mode
         mov     al,5               ;set the mask reg
         out     strport,al         ;disable dma
         out     initport,al        ;set the first/last f/f

         mov     ax,ds              ;get current segment address
         mov     cl,4
         rol     ax,cl              ;multiply by 16
         mov     ch,al              ;move the high order in the CH register
         and     al,0f0h            ;zero out the low four bits

         add     ax,bx              ;add the buffer offset to the data segment
         jnc     no_high_increment
         inc     ch                 ;increment the page register

no_high_increment :
         out     addport,al         ;output low address
         mov     al,ah
         out     addport,al         ;output high address
         mov     al,ch
         out     pageres,al         ;output high 4 bits to the page reg

         mov     al,mode
         out     cmdport,al         ;output the mode byte
;determine count
         mov     ax,511             ;each block is 512 bytes
         out     cntport,al         ;output low byte of count
         mov     al,ah
         out     cntport,al         ;output high byte of count

         mov     dx,300h            ;address for the control port on the pc 36
         mov     al,9h              ;enable dma channel 1 and keep online
         out     dx,al

         in      al,statres         ;reset the status register on the dma chip
         mov     al,chan            ;set dma operation to channel 1
         out     strport,al         ;enable channel 1 command to dma
```

```
        sti                             ;enable interupt

        push    bx                      ;push the offset address
        push    cx                      ;push the mode
        push    di                      ;push the return address
        ret

setdma  endp
code    ends
        end
```

12.0 ADJUSTMENTS AND JUMPER CONFIGURATIONS PC-36 CONTROLLER

12.1 PHASE-LOCK-LOOP ADJUSTMENT

This procedure is designed to optimize the Phase Lock Loop operating points and test for acceptable limits. If a "PC-36 controller" is adjusted per and meets the test limits of this specification, it will be able to function with a reasonable level of confidence.

12.2 EQUIPMENT

Oscilloscope and two 10X probes
Digital frequency counter
Two I.C. clips and a miniature clip lead
Power source and power cable (or IBM Extender Card) for PCBA
Digital Voltmeter with .3% DC accuracy or better

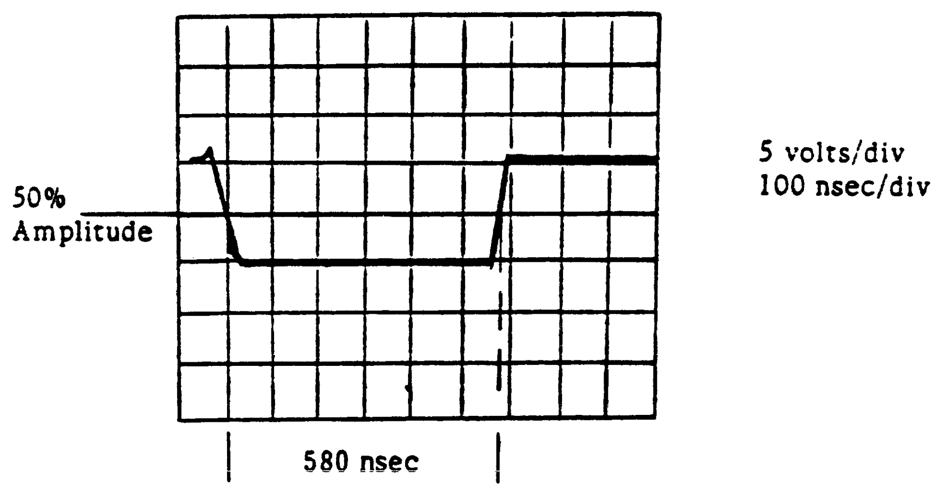
12.3 SET-UP

Connect the power cable or IBM Extender Card (5V and 12V) to J1 interface connector. Be sure that the pins on the power cable connector and the PCBA interface connector match up. Turn the power switch on.

12.4 ADJUSTMENT PROCEDURE

12.4.1 Install an I.C. clip on U21, then connect Pin 1 to Pin 7 (ground). This will supply a 900 KHZ signal to the Phase Lock Loop input circuitry.

12.4.2 Connect the oscilloscope probe to TP1 (U12 Pin 2) and adjust the trim-pot R18 for a negative pulse width of 580 nsec (see Figure below). (Measure at the 50% amplitude points.) Apply glyptol to the trim-pot and verify that the pulse width does not change.



NOTE: Prior to starting this adjustment, insure your adjustment tool is made of plastic. **No screwdrivers!**

12.4.3 Using a calibrated DVM, connect the positive lead to TP3 (U18 Pin 9) and the negative lead to the ground test point. (It is preferred that DVM probes have miniature clip leads.) Adjust the trimming capacitor (C16) for a 5.00 volt reading. Apply glyptol to the variable capacitor (C16). Insure that the voltage setting does not change (by monitoring the reading on DVM).

NOTE: Glyptol is only used as an indicator to insure the trimmers are not touched after alignment. Avoid using excessive amounts of glyptol.

Use a Q.A. approved glyptol. **Do not use "torque seal" glpt!**

12.5 TESTS AND FINAL ADJUSTMENT

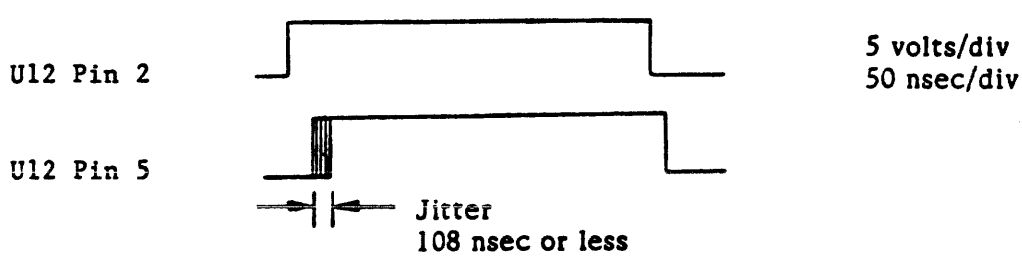
12.5.1 Connect TP3 or U18 Pin 9 (VCO input) to ground. Connect the frequency counter to the VCO output TP2 (U15 Pin 5), and measure the frequency (should be 650 KHZ or less). Then connect TP3 (U18 Pin 9) to +10V (CR4 cathod) and measure the frequency. See table below for the frequency limits.

VCO INPUT	FREQUENCY	
Ground 0V	650 KHZ or less	Range $\geq$370 KHz
(CR4 cathode) +10V	1.02 MHz or greater	

12.5.2 If the range of 370 KHZ minimum cannot be achieved, check R4 and R5 for proper values. If the values are correct, suspect a low gain PLL chip (U18).

12.5.3 Check static jitter by connecting both scope probes, one to TP1 (U12 Pin 2) and the other to U12 Pin 5.

12.5.4 Trigger the scope on positive edge of the signal on U12 Pin 2 (TP1). Compare the positive going edge of U12 Pin 5 as shown in the figure below. (The jitter should be less than or equal to 108 nsec.) If the jitter is excessive, suspect U18, U7, U12, C19, R6, or R7.



12.6 JUMPER CONFIGURATIONS

The PC-36 controller board allows for various jumper configurations. Jumper pins are designated as E1 thru E18, T11 to T12 and W1. The following descriptions define the functions of each jumper setting.

12.6.1 Tape Drive Speed Select

Jumpers E1 thru E6 are used to select the PC-36 controller configuration for proper tape drive speed.

Jumper	Tape Drive Speed
E1 to E6	30 IPS (inches per second)
E2 to E5	60 IPS
E3 to E4	90 IPS - Normal

12.6.2 RAM Select

Jumpers E7 thru E10 are used to define RAM size installed in the socket located at U-25.

Jumper	Setting
E8 to E9	2K byte RAM (standard)
E7 to E10	8K byte RAM

12.6.3 Clock Select

Jumper E11 to E12 is used for selecting the clock input for the microprocessor. This jumper is provided for test purposes only.

Jumper	Setting
E11 to E12	IN - Normal mode
	OUT - Test mode (allows external clock use)

12.6.4 Track Format Select

Jumpers E13 thru E16 are used to select 9 track or 12 track format. The controller is configured for 9 track format only, therefore, no jumper is required.

12.6.5 Read Level (RDL) Select

Jumper E17 to E18 provides Read Level (RDL) input to the controller, if required.

Jumper	Setting
E17 to E18	IN - RDL input
	OUT -Normal mode

12.6.6 PC Oscillator Select

Jumper T11 to T12 is used to select the PC oscillator clock frequency which is divided down by 2. This jumper is not used as the controller provides an internal 7.2 Mhz oscillator.

12.6.7 Microprocessor Software Reset Select

Jumper W1 is used to provide software reset via QIC-02 command (refer to Section 6.1) to 8085A-2 microprocessor. The jumper should always be connected.

12.6.8 DMA Request Jumpers

DRQ1 through DRQ3 jumpers are used to select DMA channel requests. DRQ1 has the highest priority and DRQ3 has the lowest priority.

Jumper	Setting
DRQ1	Installed - standard
DRQ2	Optional
DRQ3	Optional
DRQ3EN	Installed - standard

(Installed for backward compatibility only. Can be removed at customer's discretion.)

12.6.9 DMA Acknowledge Jumpers

DACK1 through DACK3 jumpers are used to select the DMA acknowledge lines.

Jumper	Setting
DACK1	Installed - standard
DACK2	Optional
DACK3	Optional
DACK3EN	Installed - standard

(Installed for backward compatibility only. Can be removed at customer's discretion.)

12.6.10 Interrupt Request Jumpers

IRQ2 through IRQ7 jumpers are used to select the interrupt request lines. IRQ2 has the highest priority and IRQ7 has the lowest priority.

Jumper	Setting
IRQ2	Optional
IRQ3	Installed - standard
IRQ4-IRQ7	Optional

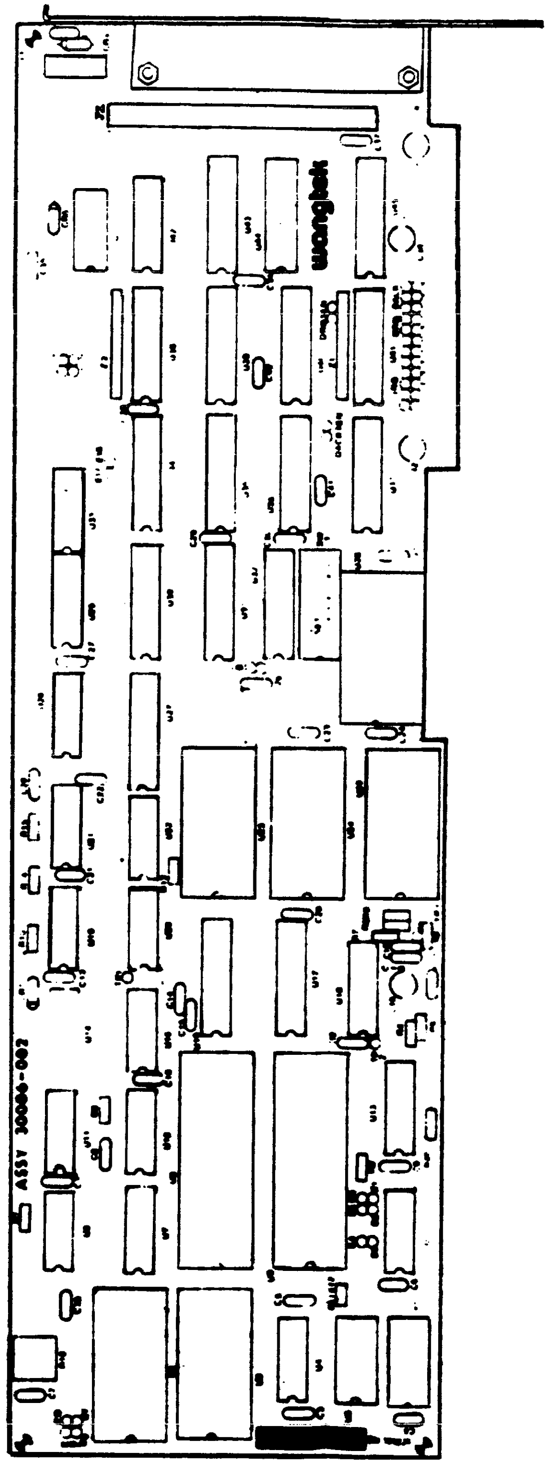
13.0 PARTS LIST

Item No.	Parts	Wangtek Part No.	Qty	Reference Designator
1	74LS02-IC	50056	1	U22
2	74LS04-IC	50020	2	U4, U33
3	74LS08-IC	50021	1	U11
4	74LS32-IC	50024	2	U1, U26
5	74LS25-IC	55182	1	U21
6	74LS74-IC	50026	3	U5, U6, U19
7	74LS92-IC	55172	1	U10
8	74LS138-IC	50077	1	U14
9	74LS174-IC	55188	2	U29, U42
10	74LS240-IC	50030	5	U27,U31,U32,U35,U38
11	74LS244-IC	50031	2	U39, U43
12	74LS245-IC	55188	1	U45
13	74LS257-IC	55169	1	U13
14	74LS373-IC	50033	3	U16, U17, U44
15	74LS374-IC	50034	3	U30, U34, U40
16	4013B-IC	55185	2	U7, U12
17	4046B-IC	55180	1	U18
18	4066B-IC	55193	1	U20
19	4070B-IC	55189	1	U15
20	IC, Gate Array - CRC/ECC	55157	2	U24, U28
21	IC, Gate Array - Write	55159	1	U23
22	IC, Gate Array - Read	55158	1	U25
23	IC, 8257-5 DMA Controller	55194	1	U8
24	IC, 8085-A-2 Microprocessor	55192	1	U9
25	IC, Erasable PROM	55176	1	U3
26	IC, Static RAM	55206	1	U2
27	IC, PAL-Programmed	55187	1	U36
28	IC, PAL-Programmed	55190	1	U37
29	IC, PAL-Programmed	55191	1	U41
30				
31				
32				
33				
34	Resistor, 68, 5%, 1W	55060-680	1	R21
35	Resistor, 1K, 5%, ¼W	50001-102	1	R14
36	Resistor, 3.3K, 5%, ¼W	50001-332	7	R1, R2, R3, R8, R9, R10, R13
37	Resistor, 5.6K, 5%, ¼W	50001-562	1	R20
38	Resistor, 9.1K, 5%, ¼W	50001-912	1	R15
39	Resistor, 10K, 5%, ¼W	50001-103	1	R7
40	Resistor, 14.7K, 1%, 1/8W	55061-1472	1	R4
41	Resistor, 24.9K, 1%, 1/8W	55061-2492	1	R5
42	Resistor, 33K, 5%, ¼W	50001-333	1	R6
43	Resistor, VAR., 10K, ½W	55184-103	1	R18
44	Resistor, SIP, 220/330	50553-002	1	Z2
45	Resistor, SIP, 4.7K	50015-472	1	Z1

13.0 PARTS LIST

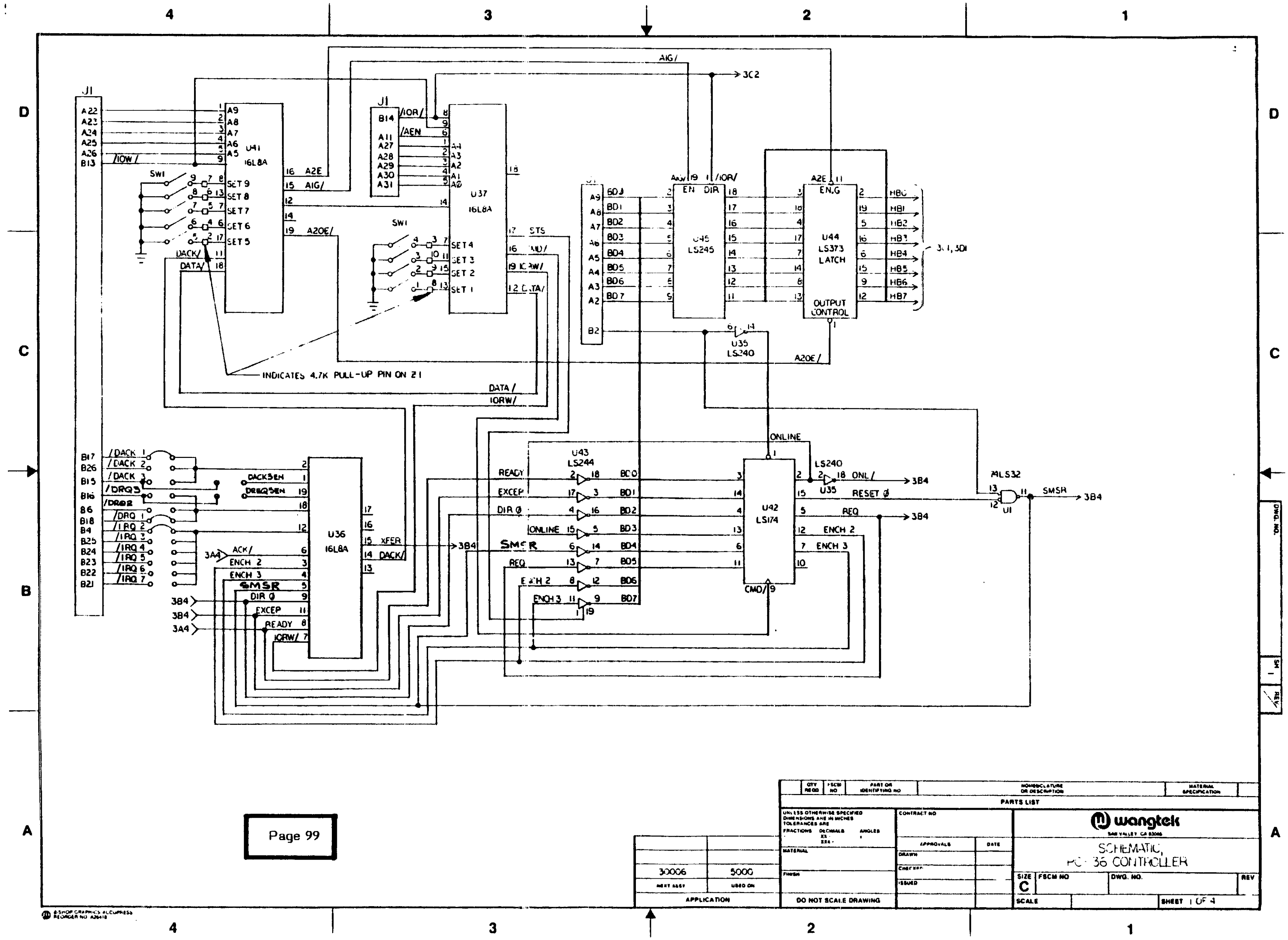
Item No.	Parts	Wangtek Part No.	Qty	Reference Designator
46				
47				
48				
49				
50	DIODE, 1N914	50092	1	CR1
51	DIODE, ZENER, ¼W, 10V, 2%	55199	1	CR4
52	DIODE, DJ1655	55200	1	CR5
53				
54	Capacitor, CER, .1MF, +80%/-20%	55195-104	27	C1-6, 10, 12-15, 20-24, 26, 27, 29-31, 33, 34, 37, 39, 35
55				
56	Capacitor, TANT, 10MF, 20%	55032-102	2	C32, 38
57	Capacitor, TANT, 15MF, 20%	55032-152	1	C36
58	Capacitor, CER., 47PF, 10%, NPO	55196-470	3	C8, 19, 28
59	Capacitor, CER., 430PF, 5%, NPO	55197-431	1	C18
60	Capacitor, CER., 27PF, 5%, NPO	55197-270	1	C17
61	Capacitor, VAR., 15-60 PF	55198	1	C16
62				
63				
64				
65				
66	Oscillator, 7.2 MHZ	55201	1	Y1
67	Switch, DIP, 10 Pos.	55202-010	1	SW1
68	Jumper, .10 Centers	55045-001	10	DRQ, DACK, E17-18, E8-9, E7-10, E1-6, E2-5, E3-4, E11-12, W1
69				
70	Header, DBL Row, 12 Pin	55203-012	1	1RQ
71	Header, DBL Row, 50 Pin	55203-050	1	J2
72	Conn., 62 Pin Sub D	55207-062	0	J3
73	Bracket	20545-002	1	
74	Bracket	20545-001	0	
75	Screw Lock Assy, Female	55208	0	
76	Screw, 4-40 X .38, CR PH	55137-206	2	
77	Washer, Nylon	55209-001	2	
78	Washer, Lock #4	55109-200	2	
79	Nut, Hex, 4-40	55104-200	2	
80				
81	Socket, DIP, 28 Pin	50008-028	6	U2, 3, 23-25, 28
82	Socket, DIP, 20 Pin	50008-020	3	U36, 37, 41
83	Socket, DIP, 40 Pin	50008-040	2	U8, 9
84				

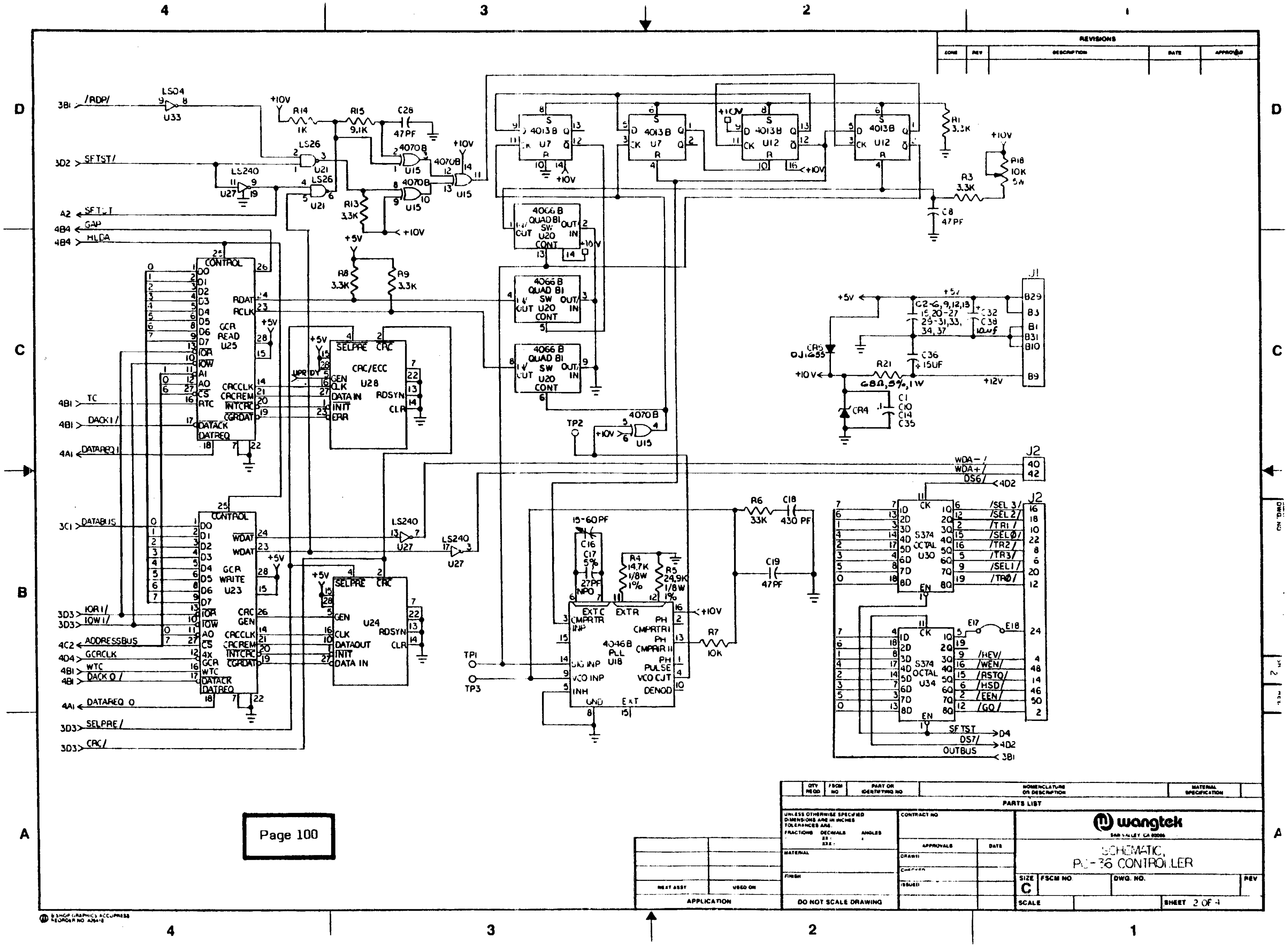
FIGURE 20.0 PC-36 CONTROLLER LAYOUT



14.0 SCHEMATIC - PC36 CONTROLLER

This section contains the schematics for the PC-36 controller (Assembly No. 30006-XXX). Schematics for the PC-36-II controller (Assembly No. 30422-XXX) are shown in Section 16.0.


J1
U41
16L8A
U37
16L8A
SW1
INDICATES 4.7K PULL-UP PIN ON Z1
U45
LS245
U44
LS373
LATCH
OUTPUT CONTROL
U35
LS240
U36
16L8A
U43
LS244
U42
LS174
74LS32
U1
SMSR
ONLINE
READY
EXCEP
DIR Ø
REQ
ENCH 2
ENCH 3
RESET Ø
ONL/
XFER
DACK/
DATA/
IORW/
A2E
A1G/
A2OE/
STS
/IOR/
/AEN
/IOW/
DACKSEN
DREQSEN
3B4
3A4
3C2
wangtek
SCHEMATIC,
PC-36 CONTROLLER
30006
5000
NEXT ASSY
USED ON
APPLICATION
DO NOT SCALE DRAWING
PARTS LIST
SIZE
C
SHEET 1 OF 4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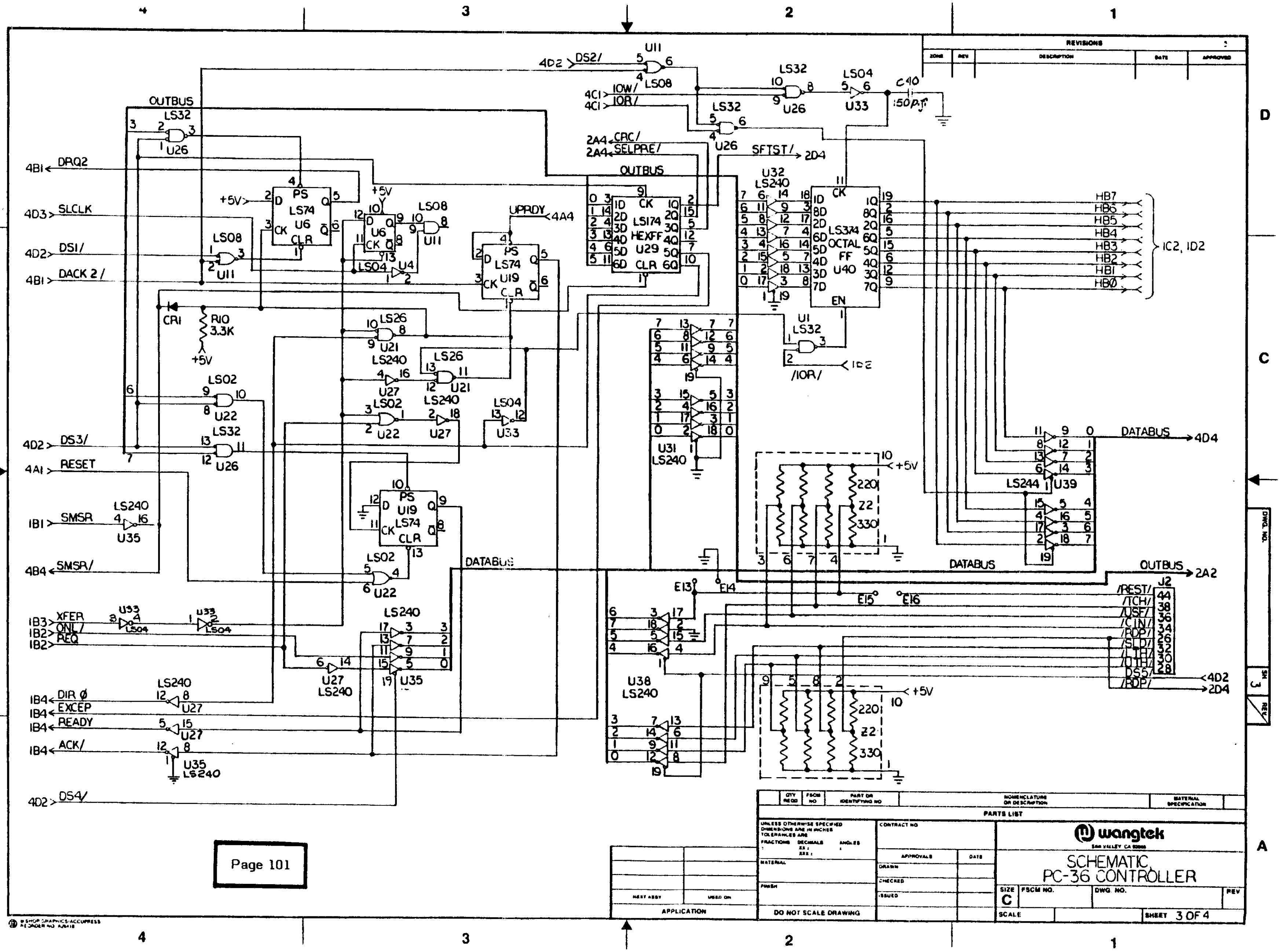
SCHEMATIC, PC-36 CONTROLLER
SIZE C
SHEET 2 OF 4
Page 100



OUTBUS
DATABUS
DRQ2
SLCLK
DS1/
DACK 2 /
DS2/
DS3/
DS4/
RESET
SMSR
SMSR/
XFER
ONL/
REQ
DIR Ø
EXCEP
READY
ACK/
IOW/
IOR/
CRC/
SELPRE/
SFTST/
UPRDY
LS74 U6
LS74 U19
LS174 HEXFF U29
LS374 OCTAL FF U40
U32 LS240
U31 LS240
U38 LS240
LS244 U39
CR1
R10 3.3K
C40 150PF
HB7
HB6
HB5
HB4
HB3
HB2
HB1
HBØ
IC2, ID2
/REST/
/TCH/
/USF/
/CIN/
/RDP/
/SLD/
/LTH/
/UTH/
DS5/
/RDP/
J2
E13
E14
E15
E16
REVISIONS
PARTS LIST
DO NOT SCALE DRAWING
APPLICATION
wangtek
SCHEMATIC, PC-36 CONTROLLER
SIZE C
SHEET 3 OF 4

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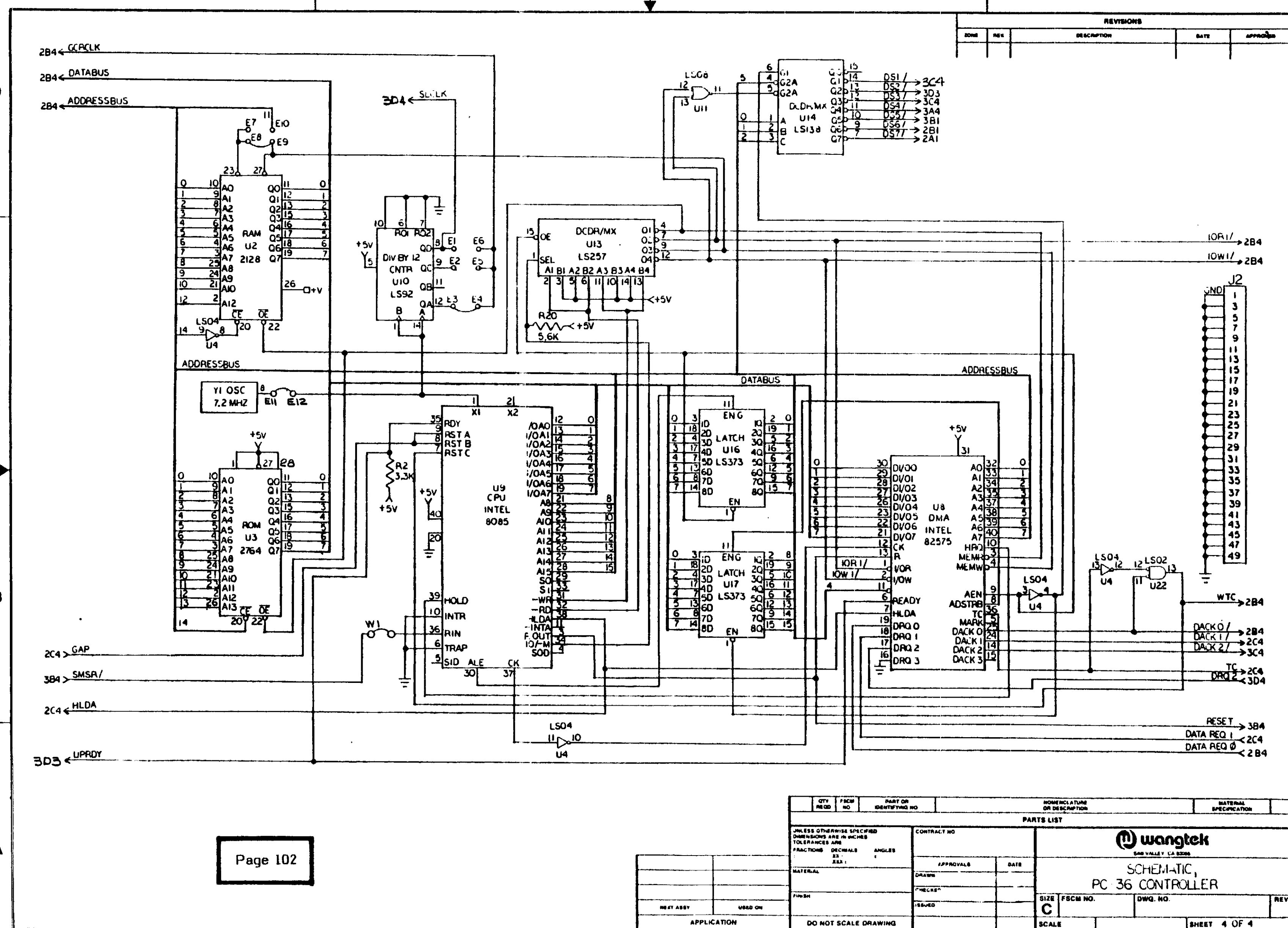

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SCHEMATIC, PC 36 CONTROLLER

SIZE C

SHEET 4 OF 4

DO NOT SCALE DRAWING

15.0 PLL ADJUSTMENT PROCEDURE AND JUMPER CONFIGURATION - PC36-II CONTROLLER

This procedure is designed to optimize the Phase Lock Loop operating points and test for acceptable limits. If a PC-36-II controller board is adjusted per and meets the test limits of this specification, it will be able to function with a reasonable level of confidence.

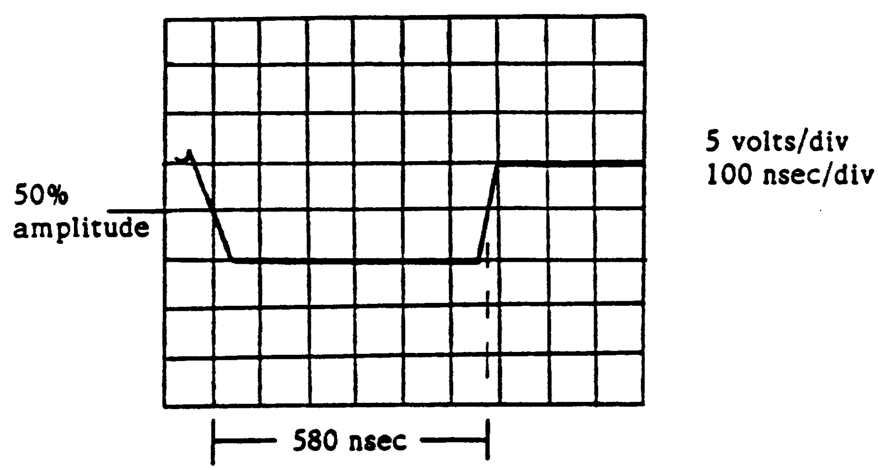
15.1 EQUIPMENT

Oscilloscope and two 10X probes
Digital frequency counter
Two I.C. clips and a miniature clip lead
Temperature chamber
Digital voltmeter

15.2 ADJUSTMENT

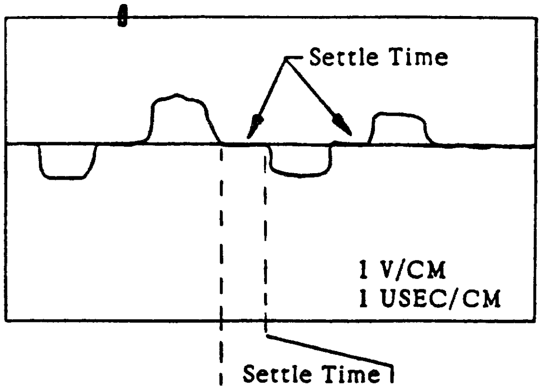
15.2.1 Install an I.C. clip on U20, then connect Pin 1 to Pin 7 (ground). This will supply a 900 KHZ signal to the Phase Lock Loop input circuitry.

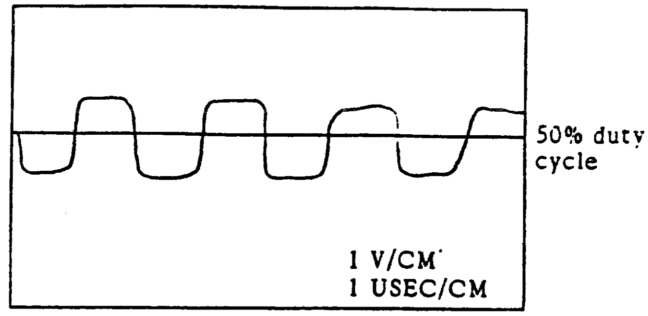
15.2.2 Connect one channel of the oscilloscope to TP1 (U2 Pin 12) and adjust the trim-pot R9 for a negative pulse width of 580 nsec. (Measure at the 50% amplitude points.)



NOTE: Prior to starting this adjustment, insure your adjustment tool is made of plastic. **No screwdrivers!**

15.2.3 Connect the scope to TP3 (U7 Pin 9). Synchronize scope to obtain a steady, single trace display. Adjust the trimming capacitor (C9) for 5 volts at the settle time of the waveform or at the 50% duty cycle, according to the appropriate waveform. Apply glyptol to the capacitor. Insure that the voltage setting does not change.





(If 5 volts DC cannot be set, C9, C8, R13, or R14 may be the wrong value or defective.)

15.3 TESTS AND FINAL FREQUENCY ADJUSTMENT

15.3.1 With frequency counter on the VCO output TP2 (U4 Pin 8), measure the frequency range of the VCO.

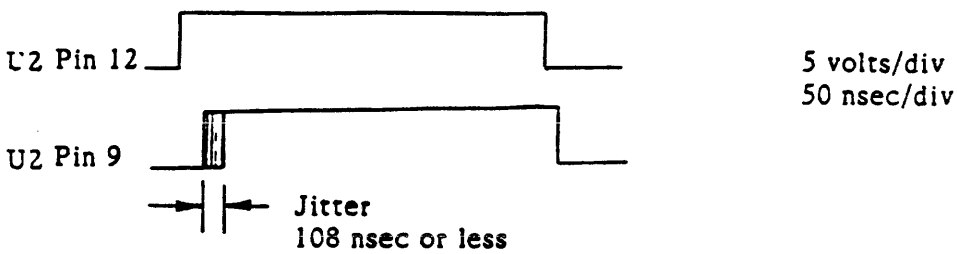
15.3.2 Connect TP3 or U7 Pin 9 (VCO input) to ground and measure the frequency. Then connect TP3 or U7 Pin 9 to +10V (U8 Pin 1) and measure the frequency. (See table for the frequency limits.)

VCO INPUT	FREQUENCY	
Ground 0V	650 KHZ or less	Range $\geq$370 KHz
(U8 Pin 1) +10V	1.02 MHz or greater	

15.3.3 If the frequency limits are not met but the range of maximum-minimum is at least 370 KHZ, re-tweek trimming capacitor C9 to center the VCO frequencies to meet the frequency limits of "650 KHZ or less" to "1.02 MHZ or greater". If the range of 370 KHZ minimum cannot be achieved, check R14 and R13 for proper value. If the values are correct, suspect a low gain PLL chip (U7).

15.3.4 Check static jitter. Connect both scope probes, one to TP1 (U2 Pin 12) and the other to U2 Pin 9.

15.3.5 Trigger the scope on the positive edge of the signal on U2 Pin 12 (TP1). Compare the positive going edge of U2 Pin 9 as shown in the picture.



If jitter is excessive, suspect U7, U1, U2, C11, C12, R16, or R15.

15.4 JUMPER CONFIGURATION - PC-36-II

15.4.1 Tape Drive Speed Selection

Jumpers E1 through E6 are used to select the PC-36-II controller configuration for proper tape drive speed.

Jumper	Tape Drive Speed
E1-E6	30ips (inches per second)
E2-E5	60ips
E3-E4	90ips

15.4.2 RAM Selection

Jumpers E7 through E10 are used for addressing the different RAM's that can be used on the PC36-II controller.

Jumper	RAM Size
E8-E9	2-Kbyte RAM - standard
E7-E10	8-Kbyte RAM

15.4.3 8085 CPU Clock Input Jumper

Jumper E11 to E12 allows an external clock input to the microprocessor on the PC36-II controller for test purposes.

Jumper	Setting
E11-E12	Installed - normal mode
	Not installed - test mode (allows external clock input)

15.4.4 Track Format Option Jumper

Jumper E13 to E14 allows the PC36-II controller firmware to use Bit 6 of the drive status port as a track format option bit for 12-track drives. This jumper is for Wangtek internal use only. Normally, it is not installed.

15.4.5 Threshold Selection Jumper

Jumper E15 to E16 allows an external control for the threshold selection in the drive electronics. This jumper is for Wangtek internal use only. Normally, it is not installed.

15.4.6 High Coercivity Select Jumper

Jumper E17 to E18 allows an externally generated high-coercivity signal input at Pin 24 of the QIC-36 basic drive interface.

Jumper	Setting
E17-E18	Not installed - standard

Installed - optional (requires special firmware)

15.4.7 PC36-II Controller Power Status Jumper

When installed, Jumper W1 pulls up the drive SEL-3 signal at Pin-16 of the QIC-36 interface to +5V upon power up.

Jumper	Setting
W1	Not installed - standard

Installed - optional (for vendors who wish to monitor this signal to determine if the PC36-II controller is powered up.)

15.4.8 DMA Request Jumpers

DRQ1 through DRQ3 jumpers are used to select DMA channel requests. DRQ1 has the highest priority and DRQ3 has the lowest priority.

Jumper	Setting
DRQ1	Installed - standard
DRQ2	Optional
DRQ3	Optional
DRQ3EN	Installed - standard

(Installed for backward compatibility only. Can be removed at customer's descretion.)

15.4.9 DMA Acknowledge Jumpers

DACK 1 through DACK3 jumpers are used to select the DMA acknowledge lines.

Jumper	Setting
DACK1	Installed - standard
DACK2	Optional
DACK3	Optional
DACK3EN	Installed - standard

(Installed for backward compatibility only. Can be removed at customer's descretion.)

15.4.10 Interrupt Request Jumpers

IRQ2 through IRQ7 jumpers are used to select the interrupt request lines. IRQ2 has the highest priority and IRQ7 has the lowest priority.

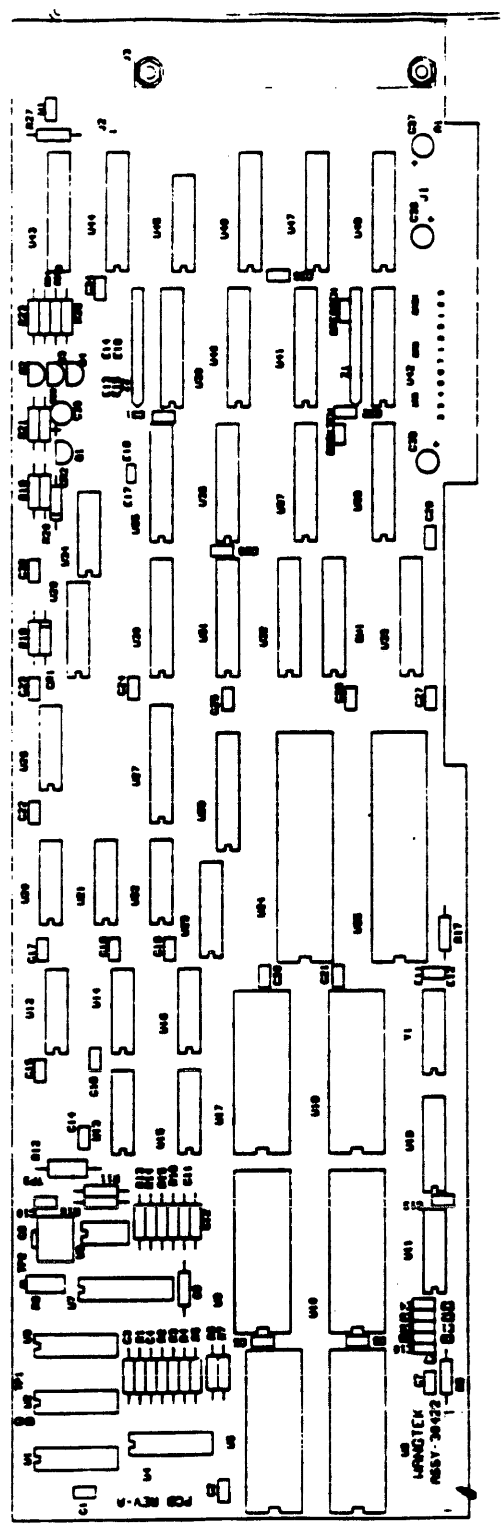
Jumper	Setting
IRQ2	Optional
IRQ3	Installed - standard
IRQ4-IRQ7	Optional

16.0 PARTS LIST - PC36-II CONTROLLER

Item No.	Parts	Wangtek Part No.	Qty	Reference Designator
1	I.C. 74LS00	50019	1	U14
2	I.C. 74LS02	50056	1	U22
3	I.C. 74LS04	50020	2	U21, 26
4	I.C. 74LS08	50021	1	U16
5	I.C. 74LS32	50024	2	U15, 34
6	I.C. 74LS26	55182	1	U20
7	I.C. 74LS74	50026	2	U12, 13
8	I.C. 74LS92	55172	1	U11
9	I.C. 74LS138	50077	1	U23
10	I.C. 74LS174	55171	2	U29, 45
11	I.C. 74LS240	50030	5	U27,31,32,U36, 39
12	I.C. 74LS244	50031	2	U40, 46
13	I.C. 74LS244	55229	2	U43, 44
14	I.C. 74LS245	55188	1	U48
15	I.C. 74LS257	55169	1	U19
16	I.C. 74LS373	50033	3	U28, 33, 47
17	I.C. 74LS374	50034	1	U41
18	I.C. 74S374	55170	2	U30, 35
19	I.C. 4013B	55185	2	U1, 2
20	I.C. 4046B,PLL	55180	1	U7
21	I.C. 5066B	55193	1	U3
22	I.C. 4070B	55189	1	U5, 6
23	I.C. Gate Array - CRC/ECC CF40100BN	55157	2	U5, 6
24	I.C. Gate Array - Write CF40101N	55159	1	U10
25	I.C. Gate Array - Read CR40102N	55158	1	U9
26	I.C. 8257-5 DMA Controller	55194	1	U24
27	I.C. 8085A-2 Microprocessor	55192	1	U25
28	I.C. Static RAM (2K)	55206	1	U18
29	I.C. Pal Programmed	55187	1	U37
30	I.C. Pal Programmed	55190	1	U38
31	I.C. Pal Programmed	55191	1	U42
32	I.C. EPROM Programmed	20597	1	U17
33	Voltage Regulator TL431CP	55227	1	U8
34				
35				
36	Oscillator 7.2 MHz	55201	1	Y1
37				
38				
39	Transistor 2N3904	50223	4	Q1, 2, 3, 4
40				
41				
42	Diode 1N914	50092	1	CR2
43	Diode 1N270	55220	1	CR1

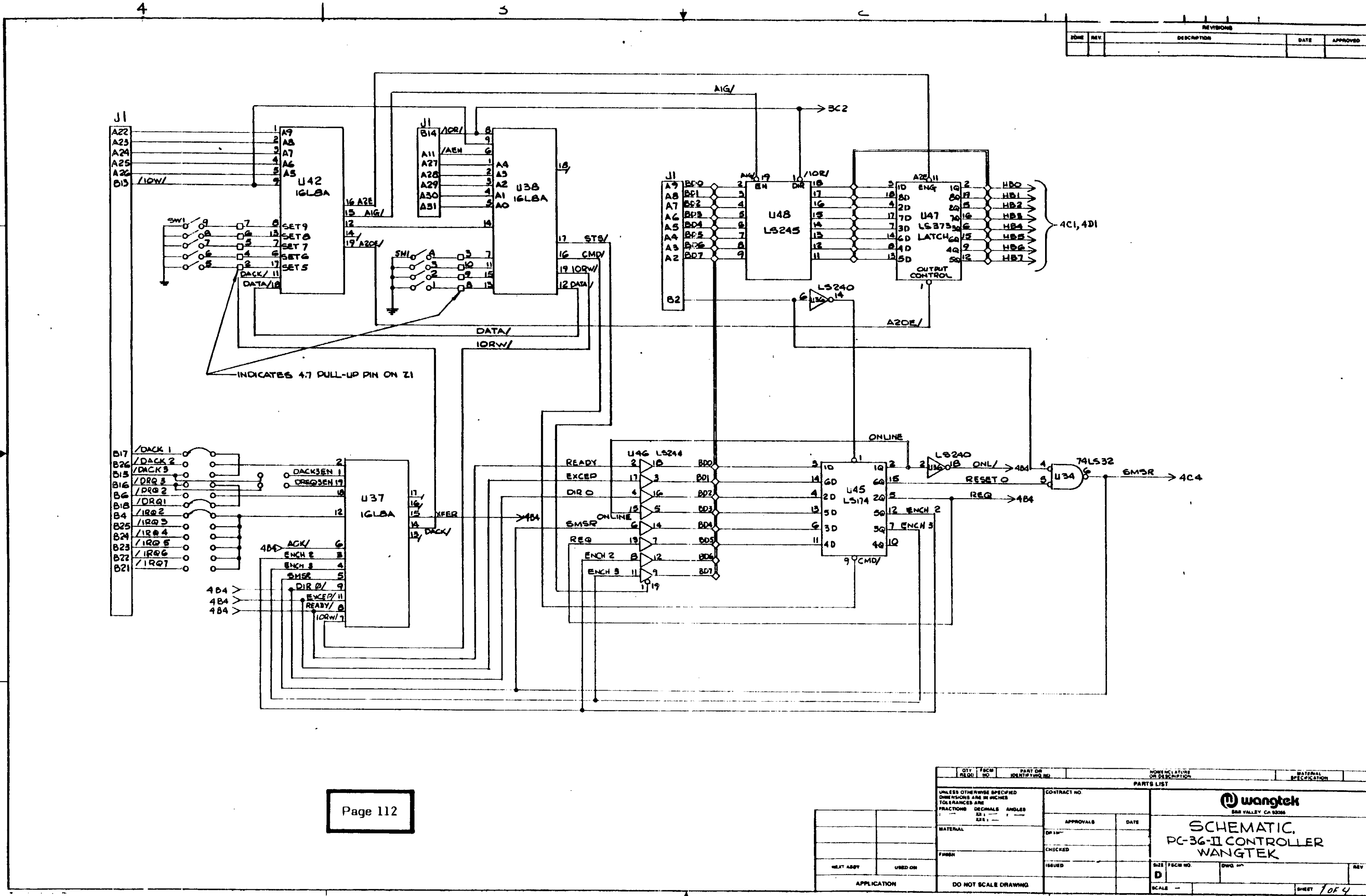
Item No.	Parts	Wangtek Part No.	Qty	Reference Designator
44	Capacitor, 0.1MF Radial	55246-001	28	C1, 2, 5-7, 10, C13-29, 31, 32, C34, 35, 38
45	Capacitor, 2.2MF Tant Radial	55032-221	1	C30
46	Capacitor, 10MF Tant Radial	55032-102	2	C33, 37
47	Capacitor, 15MF Tant Radial	55032-152	1	C36
48	Capacitor, 27PF 1% Axial	55250-001	1	C8
49	Capacitor, 47PF 1% Axial	55249-001	1	C12
50	Capacitor, 47PF 5% Axial	55248-001	2	C3, 4
51	Capacitor, 430PF 1% Axial	55253-001	1	C11
52	Capacitor, Rt. Angle 15-60PF	55238	1	C9
53				
54				
55				
56	Resistor, 68 ohms 5% 1/2 W	55239	1	R12
57	Resistor, 150 ohms 5% 1/4 W	50001-151	1	R21
58	Resistor, 750 ohms 5% 1/4 W	50001-751	1	R23
59	Resistor, 470 ohms 5% 1/4 W	50001-471	1	R22
60	Resistor, 499 ohms 1% 1/8 W	55061-4900	1	R11
61	Resistor, 1K 5% 1/4 W	50001-102	3	R3, 25, 27
62	Resistor, 1.5K 1% 1/8 W	55061-1501	1	R10
63	Resistor, 3.3K 5% 1/4 W	50001-332	8	R1, 2, 4-7, R17, 18
64	Resistor, 4.7K 5% 1/4 W	50001-472	3	R20, 24, 26
65	Resistor, 5.6K 5% 1/4 W	50001-562	1	R8
66	Resistor, 9.1K 5% 1/4 W	50001-912	1	R2
67	Resistor, 10K 5% 1/4 W	50001-103	1	R15
68	Resistor, 14.7K 1% 1/8 W	55061-1472	1	R14
69	Resistor, 24.9K 1% 1/8 W	55061-2492	1	R13
70	Resistor, 33K 5% 1/4 W	50001-333	1	R16
71	Resistor, 100K 5% 1/4 W	50001-104	1	R19
72	Resistor, SIP 220/330, 10 Pin	55247-001	1	Z2
73	Resistor, SIP 4.7K, 10 Pin	50015-472	1	Z1
74	Resistor, Rt Angle Var 10K1/2 W	55240	1	R9
75	Jumper	55045-001	5	IRD2, DRQ1, DACK 1, E3, E4, E8, E9
76	Header, Double Row, 24 Pin	55203-024	1	IRQ2-7, DRQ1-3 DACK1-3
77	Header, Double Row, 50 Pin	55203-050	1	J2
78	Pin, Test Point	55207-001	26	E1-18, W1, Gnd, TP1-3, DRQ3EN
79	Switch, Dip, 10 Position	55202-010	1	SW1
80	Bracket	20545-002	1	
81	Screw 4-40 x .38 CR, PH	55137-206	2	
82	Washer, Nylon	55209-001	3	
83	Washer, Lock #4	55109-200	2	
84	Nut, Hex 4-40	55104-200	2	

FIGURE 21.0 PC36-II CONTROLLER LAYOUT

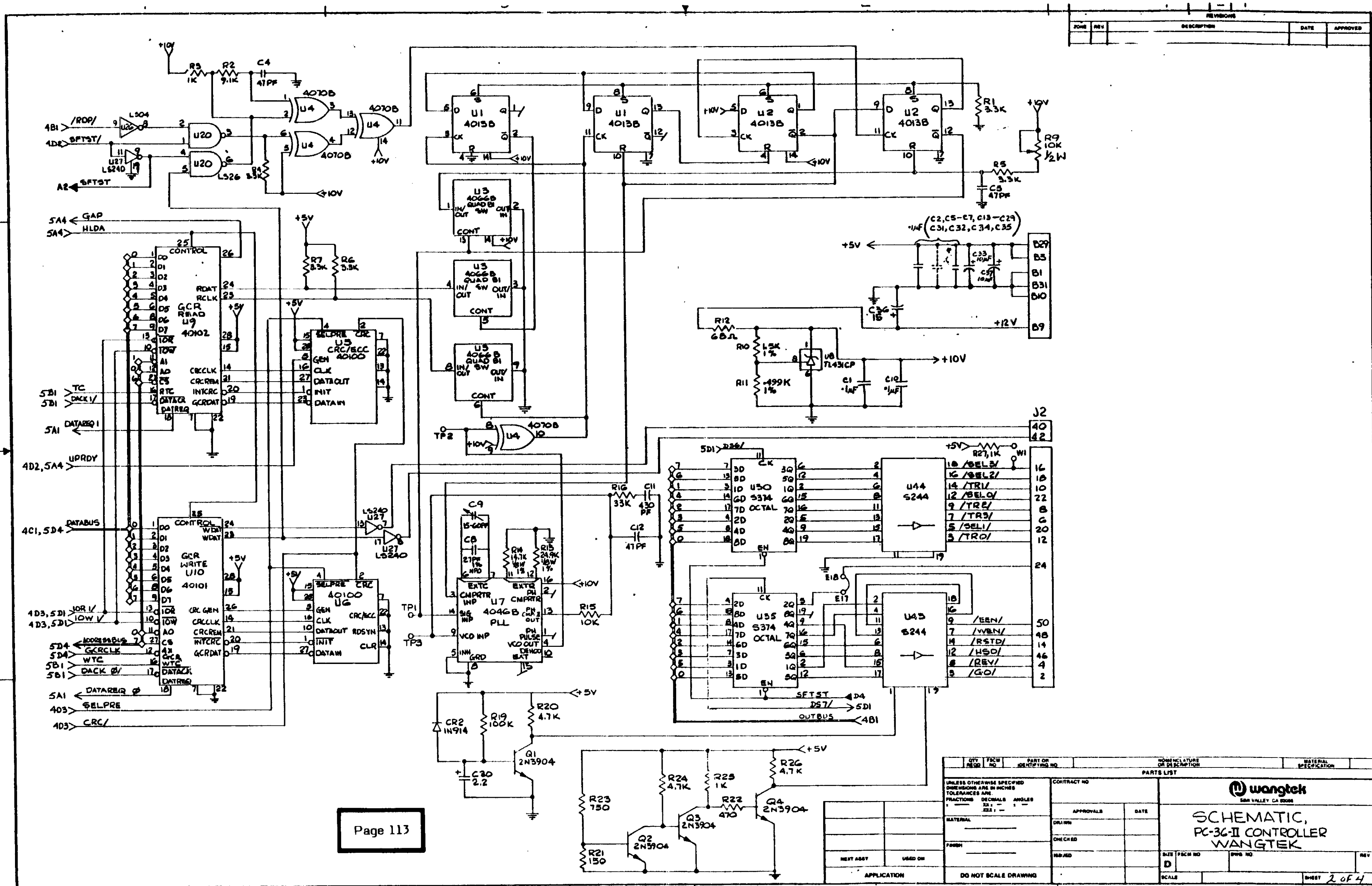


17.0 SCHEMATIC - PC36-II CONTROLLER

This section contains the schematics for the PC36-II controller (Assembly No. 30422-XXX). Schematics for the PC-36 controller (Assembly No. 30006-XXX) are given in Section 14.0.



U42 16L8A
U38 16L8A
U48 LS245
U47 LS373 LATCH
OUTPUT CONTROL
U37 16L8A
U46 LS244
U45 LS174
74LS32
LS240
INDICATES 4.7 PULL-UP PIN ON Z1
4C1, 4D1
SMSR
4C4
wangtek
SCHEMATIC,
PC-36-II CONTROLLER
WANGTEK
DO NOT SCALE DRAWING
APPLICATION
1 OF 4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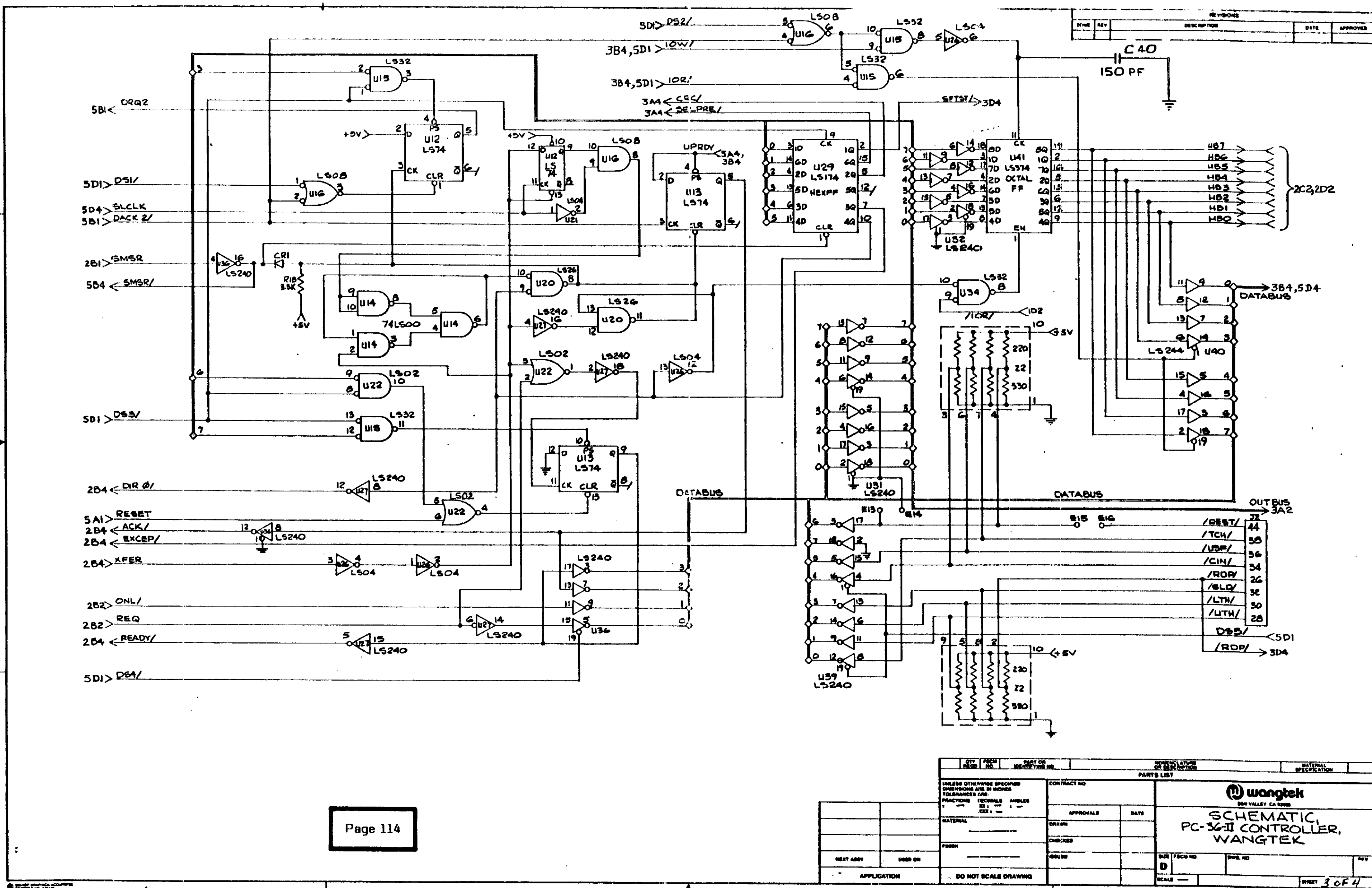
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wangtek
C40 150 PF
DATABUS
OUTBUS 3A2
5D1 > DS1/
5D1 > DS2/
3B4,5D1 > IOW/
3B4,5D1 > IOR/
3A4 < CSC/
3A4 < SEL PRE/
SFTST/ > 3D4
5B1 < DRQ2
5D4 > SLCLK
5B1 > DACK 2/
2B1 > SMSR
5B4 < SMSR/
5D1 > DS3/
2B4 < DIR Ø/
5A1 > RESET
2B4 < ACK/
2B4 < EXCEP/
2B4 > XFER
2B2 > ONL/
2B2 > REQ
2B4 < READY/
5D1 > DS4/
UPRDY < 3A4, 3B4
/IOR/ < ID2
HB7 HB6 HB5 HB4 HB3 HB2 HB1 HB0
2C2,2D2
3B4,5D4 DATABUS
/RESET/ 44
/TCH/ 38
/USF/ 36
/CIN/ 34
/RDP/ 26
/BLD/ 32
/LTH/ 30
/UTH/ 28
DS5/ < 5D1
/RDP/ > 3D4
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U29 LS174 HEXFF
U12 LS74
U13 LS74
74LS00
SHEET 3 OF 4

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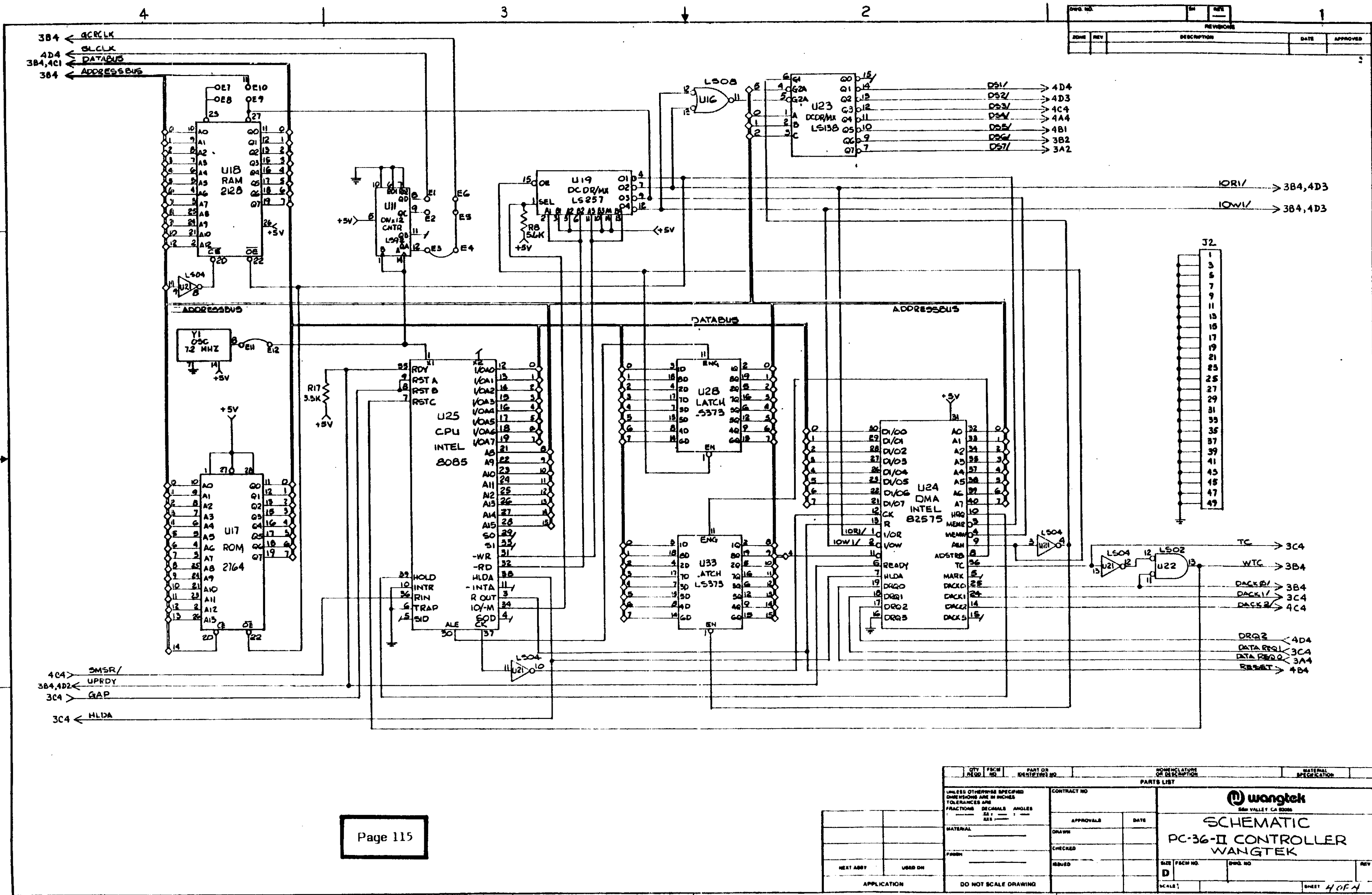

U18 RAM 2128
U17 ROM 2764
U11 CNTR LS93
U19 DCDR/MX LS257
U16 LS08
U23 DCDR/MX LS138
U25 CPU INTEL 8085
U28 LATCH LS373
U33 LATCH LS375
U24 DMA INTEL 82575
U22 LS02
U21 LS04
Y1 OSC 7.2 MHZ
R17 3.5K
R8 5.6K
J2
ADDRESSBUS
DATABUS
GCRCLK
SLCLK
SMSR/
UPRDY
GAP
HLDA
IORI/
IOWI/
DS1/
DS2/
DS3/
DS4/
DS5/
DS6/
DS7/
TC
WTC
DACK0/
DACK1/
DACK2/
DRQ3
DATA REQ1
DATA REQ0
RESET
SCHEMATIC
PC-36-II CONTROLLER
WANGTEK
wangtek
PARTS LIST
DO NOT SCALE DRAWING
APPLICATION
SHEET 4 OF 4

18.0 WANGTEK PC-36-III CONTROLLER

18.0.1 INTRODUCTION

The Wangtek PC-36-III Controller (Assembly No. 30850-XXX) is an enhanced version of the Wangtek PC-36 Controller. Some of the enhancements include the following. Major portions of the controller logic have been consolidated into one gate array chip. Also, the four gate arrays (Read, Write, CRC) have been combined into one gate array chip. Ground layouts have been reinforced to enhance PLL performance. The power glitch protection circuitry has also been improved to prevent accidental erasure of tape during sudden loss of power.

18.1 ADJUSTMENTS AND JUMPER CONFIGURATION

18.1.0 PLL ADJUSTMENT PROCEDURE

This procedure is designed to optimize the Phase Lock Loop operating points and test for acceptable limits. If a PC-36 III Controller Board is adjusted per and meets the test limits of this specification, it will be able to function with a reasonable level of confidence.

18.1.1 EQUIPMENT

Oscilloscope and two 10X probes.
Digital frquency counter.
Two I.C. clips and a minature clip lead.
Power source and power cable (or IBM Extender Card) for PCBA.
Digital voltmeter with .3% DC accuracy or better.

18.1.2 SET-UP

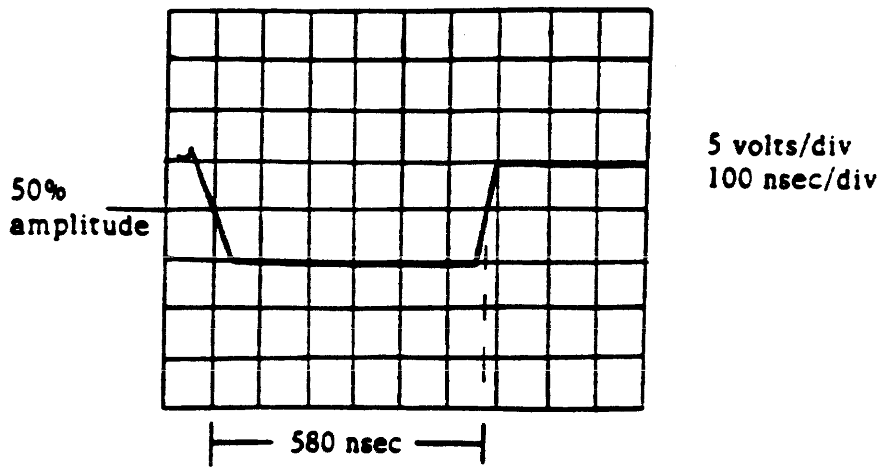
Connect the power cable or IBM Extender Card to J1 interface connector. Turn the power switch on.

18.1.3 ADJUSTMENT

18.1.3.1 Remove the jumper from W6.

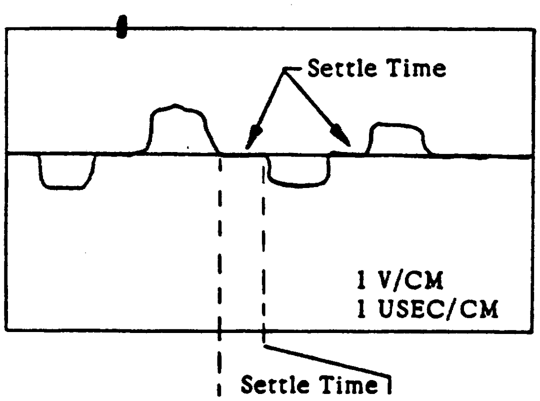
18.1.3.2 Install a jumper on W7. This will supply a 900 KHZ signal to the Phase Lock Loop input circuitry.

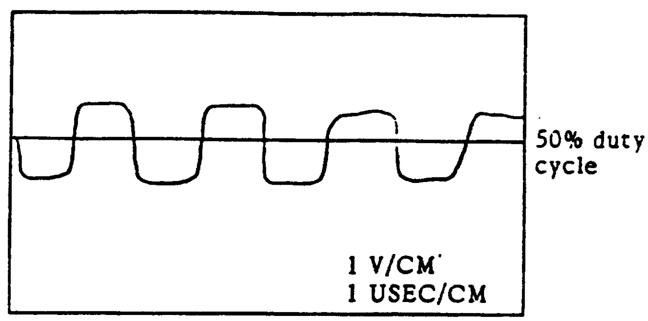
18.1.3.3 Connect one channel of the oscilloscope to TP1 (U2 Pin 12) and adjust the trim-pot R9 for a negative pulse width of 580 nsec. (Measure at the 50% amplitude points.)



Note: Prior to starting this adjustment insure your adjustment tool is made of plastic. No screw drivers.

18.1.3.4 Connect the scope to TP3 (U5 Pin 9). Synchronize scope to obtain a steady, single trace display. Adjust the trimming capacitor (C14) for 5 volts at the settle time of the waveform or at the 50% duty cycle, according to the appropriate waveform. Apply glpt to the capacitor. Insure that the voltage setting does not change.





(If 5 volts DC cannot be set, C13, C14, R10 or R11 may be the wrong value or defective.)

18.1.4 TESTS AND FINAL ADJUSTMENT

18.1.4.1 With frequency counter on the VCO output TP2 (U4 Pin 8), measure the frequency rate of the VCO.

18.1.4.2 Connect TP3 or U5 Pin 9 (VCO input) to ground and measure the frequency. Then connect TP3 or U5 Pin 9 to +10V (U6 Pin 1) and measure the frequency. (See the table for the frequency limits).

VCO INPUT	FREQUENCY	
Ground 0V	650 KHZ or less	Range $\geq$370 KHz
U6 Pin 1 +10V	1.02 MHz or greater	

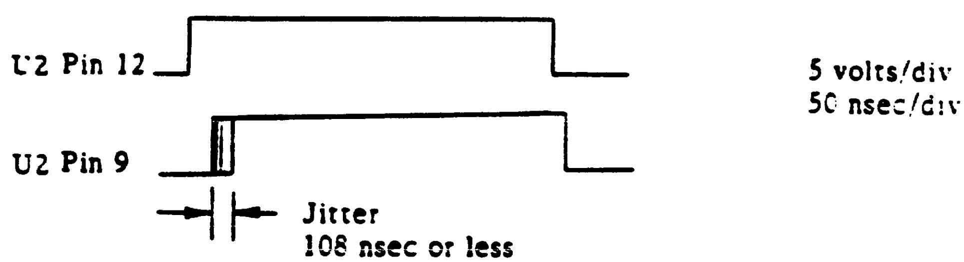
18.1.4.3 If the frequency limits are not met, but the range of maximum - minimum is at least 370 KHz, re-tweek trimming capacitor C9 to center of the VCO frequencies to meet the frequency limits of "650 KHz or less" to "1.02 MHz or greater".

If the range of 370 KHz minimum cannot be achieved, check R10 and R11 for the proper value.

If the values are correct, suspect a low gain PLL chip (U5).

18.1.4.4 Check static jitter. Connect both scope probes, one to TP1 (U2 Pin 12) and the other to U2 Pin 9.

18.1.4.5 Trigger the scope on the positive edge of the signal on U2 Pin 12 (TP1). Compare the positive going edge of U2 Pin 9 as shown in the picture. If jitter is excessive, suspect U5, U1, U2 or C11, C12, R12, R13.



18.1.4.6 Remove the jumper from W7 and install it on W6.

18.1.5 JUMPER CONFIGURATIONS

18.1.5.1 8085 CPU Clock Input Jumper

Jumper W1 allows an external clock input to the 8085 micro-processor on the PC-36-III Controller for test purposes.

Jumper	Setting
W1	Installed-normal mode. Not installed-test mode (allows external lock input).

18.1.5.2 RAM Selection Jumpers

Jumpers W2 and W3 are used for addressing the different RAMs that can be used on the PC-36-III Controller.

Jumper	RAM Size
W2	W2 installed, W3 not installed. (2K byte RAM-standard).
W3	W3 installed, W2 not installed for 8K byte RAMs.

18.1.5.3 Threshold Selection Jumper

Jumper W4 allows an external control for the threshold selection in the drive electronics. This jumper is for Wangtek internal use only. Normally it is not installed.

18.1.5.4 Track Format Option Jumper

Jumper W5 allows the formatter firmware to use bit 6 of the drive status port as a track format option bit for 12 track drives. This jumper is for Wangtek internal use only. Normally it is not installed.

18.1.5.5 PLL Adjustment Jumpers

Jumpers W6 and W7 are used for PLL adjustment on the PC-36 III Controller.

Jumper	Setting
W6	Installed - Standard.
W7	Install only for PLL adjustment.

18.1.5.6 PC-36 III Controller Power Status Jumper

Jumper W8, when installed, pulls up the drive/DS3* signal at pin 16 of the QIC-36 interface to +5V upon power up.

Jumper	Setting
W8	Not installed - standard. Installed - optional (for vendors who wish to monitor this signal to determine if the PC-36 III controller is powered up.)

18.1.5.7 High Coercivity Select Jumper

Jumper W9 allows an externally generated high coercivity signal input at pin 24 of the QIC-36 basic drive interface.

Jumper	Setting
W9	Not installed - standard.
	Installed - optional (requires special firmware).

18.1.5.8 Chassis to Logic Ground Jumper

Jumper W10 allows the PC-36 III logic ground to be connected to chassis ground.

Jumper	Setting
W10	Installed - standard.
	Not Installed - optional.

18.1.5.9 DMA Request Jumpers

DRQ1 through DRQ3 jumpers are used to select DMA channel requests. DRO1 has the highest priority and DRQ3 has the lowest priority.

Jumper	Setting
DRQ1	Installed - standard.
DRQ2	Optional.
DRQ3	Optional.
DRQ3EN	Installed - standard (installed for backward compatibility only. Can be removed at Customer's discretion).

18.1.5.10 DMA Acknowledge Jumpers

DACK1 through DACK3 jumpers are used to select the DMA acknowledge lines.

Jumper	Setting
DACK1	Installed - standard.
DACK2	Optional.
DACK3	Optional.

18.1.5.11 Interrupt Request Jumpers

IRQ2 through IRQ7 jumpers are used to select the interrupt request lines. IRQ2 has the highest priority and IRQ7 has the lowest.

Jumper	Setting
IRQ3	Installed - standard.
IRQ2	Optional.
IRQ4-IRQ7	Optional.

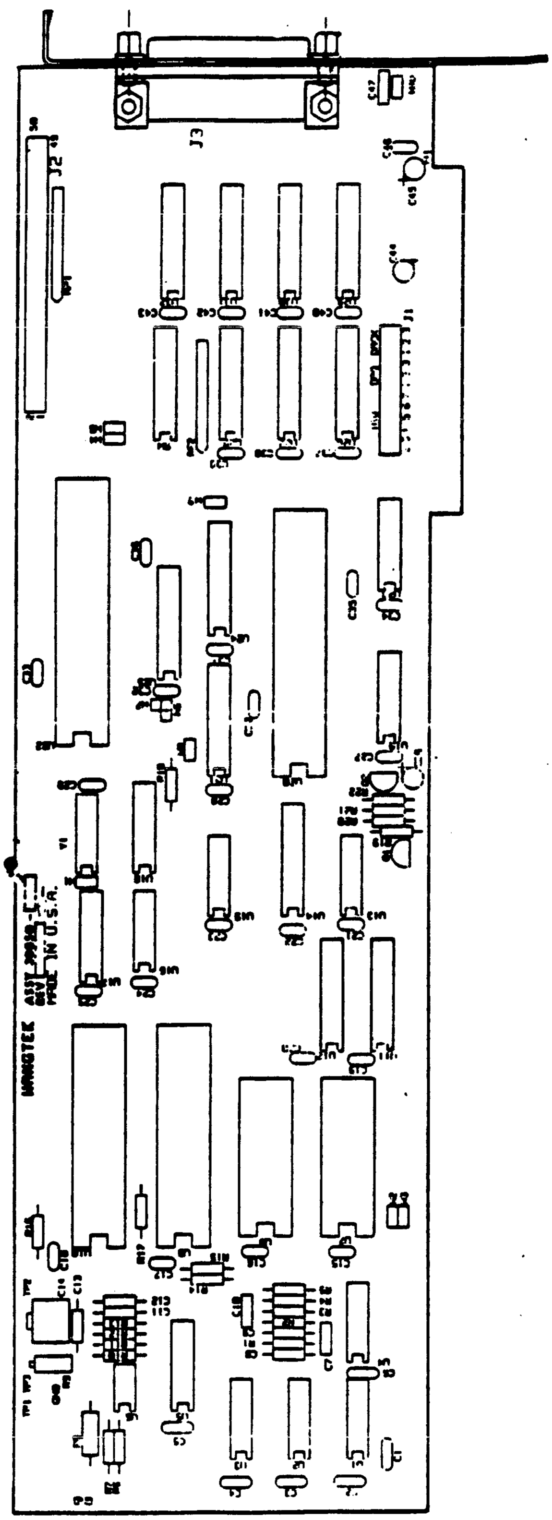
18.1.6 PARTS LIST PC-36-III

Item No.	Part	Wangtek P/N	Qty.	Remarks
1	Header, Single Row, 1 Pin	50004-002	6	TP1,TP2,TP3,GND(2),W7
2	Header, Double Row, 2 Pin	55203-002	9	W1-6,W8,W11,W12
3	Header, Double Row, 24 Pin	55203-024	1	IRQ2-7,DRQ1-3,DACK1-3
4	Header, Double Row, 50 Pin	55023-050	1	J2
5	Socket, Dip, 20 Pin	50008-020	3	U26, U27, U28
6	Socket, Dip, 28 Pin	50008-028	2	U7, U8
7	Socket, Dip, 48 Pin	50008-048	2	U20, U22
8	IC, Gate Array, R/W	20790-001	1	U20
9	IC, Gate Array, Glue Logic	20791-001	1	U22
10	IC, 8085A, Microprocessor	55192	1	U9
11	IC, 8257-5 DMA Controller	55194	1	U10
12	IC, TL431CP Volt. Reg.	55227	1	U6
13	IC, 4070B	55189	1	U4
14	IC, 4066B	55193	1	U3
15	IC, 4013B	55185	2	U1, U2
16	IC, 4046B, PLL	55180	1	U5
17	IC, 74LS373	50033	2	U11, U12
18	IC, 74LS240	50030	2	U14, U15
19	IC, 74LS257	55169	1	U17
20	IC, 74LS26	55182	1	U13
21	IC, 74S244	55229	2	U21, U24
22	IC, 74LS02	50056	1	U16
23	IC, 74LS245	55188	1	U32
24	IC, 74LS640	55383-001	1	U30
25	IC, 74LS174	55171	1	U23
26	IC, 74LS374	50034	1	U31
27	IC, 74LS00	50019	1	U15
28	IC, DS3487	55396-001	1	U19
29	IC, 74LS244	50031	1	U29
30	IC, PAL, Programmed	55187-003	1	U26
31	IC, PAL, Programmed	55191-003	1	U27
32	IC, PAL, Programmed	55190	1	U28
33	Switch, Dip, 10 Position	55202-010	2	SW1
34	Oscillator, 7.2 MHz	55201	1	Y1
35	Transistor, 2N3904	50223	2	Q1, Q2
36	Recept. Assy.-Conn. 25 Pin	55384-006	1	J3
37	Capacitor, 0.1 UF Radial	55246-001	35	C2-4, C6-7, C15-25, C27-43, C46-47
38	Capacitor, 2.2 UF ±10% 20 Volt Radial	55242-221	1	C26
39	Capacitor, 4.7 UF, ±10% 20 Volt Radial	55242-471	1	C45

18.1.6 PARTS LIST PC-36-III (Continued)

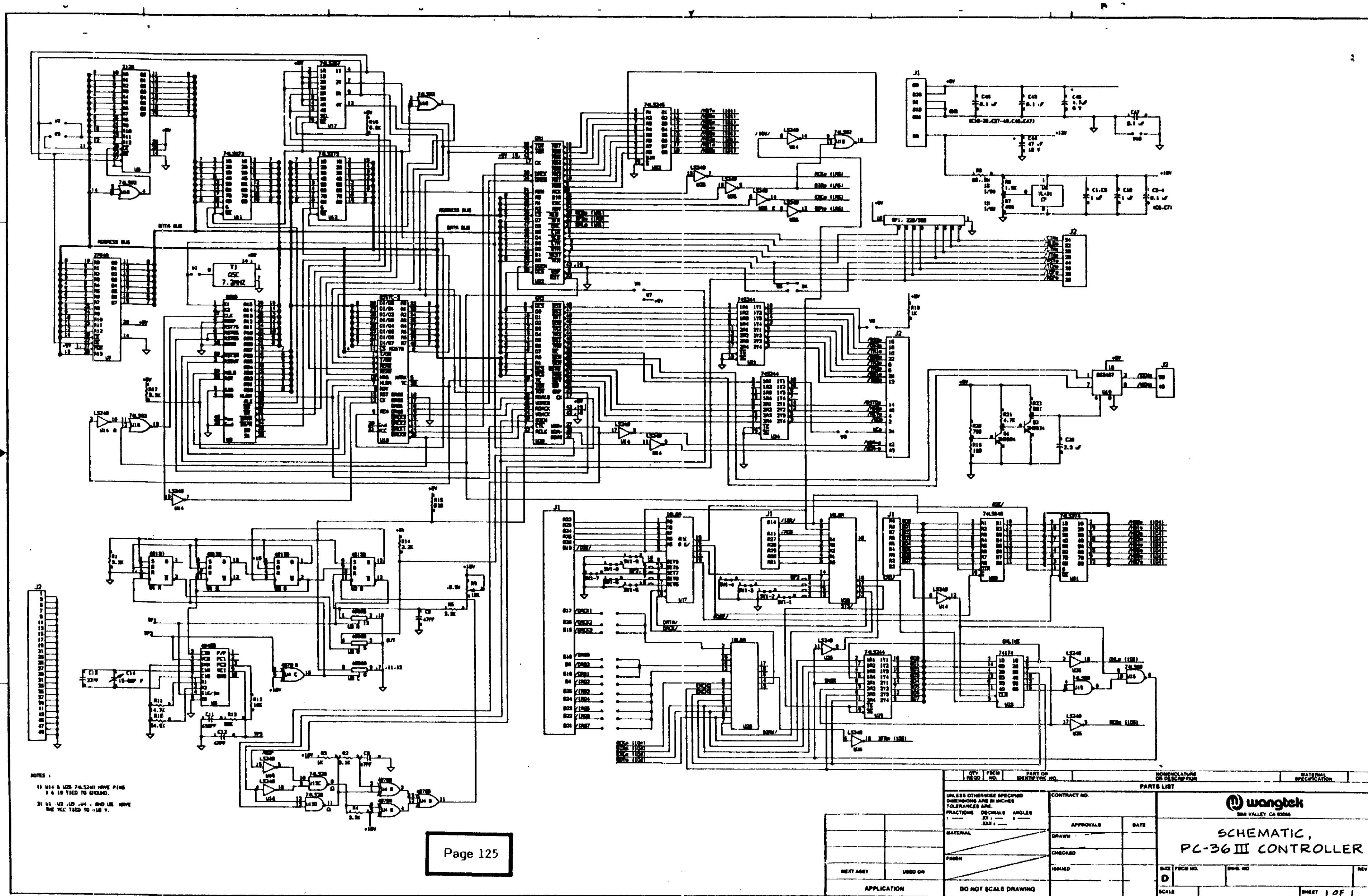
Item No.	Part	Wangtek P/N	Qty.	Remarks
40	Capacitor, 47 UF, ±10% 20 Volt Radial	55242-472	1	C44
41	Capacitor, Var. 15-60PF	55238	1	C14
42	Capacitor, 27PF, 5% Axial	55250-001	1	C13
43	Capacitor, 47PF, 5% Axial	55248-001	3	C12, C8, C9
44	Capacitor, 430PF, 5% Axial	55253-001	1	C11
45	Capacitor, 1UF, 50V, ±10%	55279-001	3	C1, C5, C10
46	Resistor, 68, 5%, ½W	55239-001	1	R8
47	Resistor, 150, 5%, ¼W	50001-151	1	R19
48	Resistor, 56K, 5%, ¼W	50001-563	1	R22
49	Resistor, 750, 5%, ¼W	50001-751	1	R20
50	Resistor, 4.7K, 5%, ¼W	50001-472	1	R21
51	Resistor, 1K, 5%, ¼W	50001-102	2	R3, R18
52	Resistor, 6.8K, 5%, ¼W	50001-682	1	R16
53	Resistor, 3.3K, 5%, ¼W	50001-332	4	R1, R4, R5, R17
54	Resistor, 9.1K, 5%, ¼W	50001-912	1	R2
55	Resistor, 33K, 5%, ¼W	50001-333	1	R13
56	Resistor, 2.2K, 5%, ¼W	50001-222	1	R14
57	Resistor, 820, 5%, ¼W	50001-821	1	R15
58	Resistor, 24.9K, 1%, 1/8W	55061-2492	1	R10
59	Resistor, 14.7K, 1%, 1/8W	55061-1472	1	R11
60	Resistor, 10K, 1%, 1/8W	55061-1002	1	R12
61	Resistor, 1.5K, 1%, 1/8W	55061-1501	1	R6
62	Resistor, 0.499K, 1%, 1/8W	55061-4990	1	R7
63	Resistor, Var. 10K, ½W	55240-001	1	R9
64	Resistor, 220/330,10 Pin SIP	55247-001	1	RP1
65	Resistor, 4.7K,10Pin,UP SIP	50015-471	1	RP2
66	Bracket, Mounting	20706-001	1	
67	Screw, 4-40 X .38 PH	55137-206	2	
68	Washer, Nylon	55209-001	2	
69	Washer, Lock	55109-200	2	
70	Nut, Hex, 4-40	55104-200	2	
71	Standoff, Male, Female Threaded	55342-001	2	

FIGURE 22.0. PC-36-III CONTROLLER LAYOUT



19.0 SCHEMATIC - PC-36-III CONTROLLER

This section contains the schematics for the PC-36-III Controller (Assembly Number 30850-XXX). Schematics for the PC-36-III Controller (Assembly Number 30422-XXX) and the PC-36 Controller (Assembly Number 30006-XXX) are given in Sections 17.0 and 14.0 respectively.



SCHEMATIC,
PC-36 III CONTROLLER
wangtek
PARTS LIST
DO NOT SCALE DRAWING
APPLICATION
NEXT ASSY
USED ON
SIZE D
SHEET 1 OF 1

APPENDIX "A"

The following describes signals and their definitions for the Wangtek Series 5125E, 125 Megabyte Tape Drive Interface.

INPUT SIGNAL DESCRIPTION. The input signals to the drive are as follows:

PIN 2 - GO. The GO line is used to start and stop the tape drive. A low signal level at this line will initiate tape motion. A High level signal will terminate tape motion.

PIN 4 - REV. The REV line is used to determine tape direction. A low level at this line will cause tape motion in the reverse (EOT to BOT) direction. A high level at this line will cause tape motion in the forward (BOT to EOT) direction.

PIN 6 - TR3.
PIN 8 - TR2.
PIN 10 - TR1.
PIN 12 - TR0.
PIN 18 - TR4. These lines are used to determine the head positioning with the respect to the track location. TR4 is the Most Significant Bit while TRO is the Least Significant Bit. TR1 through TR3 signal lines are used to determine head positioning. TRO is used to switch between the two write/read heads on the head assembly. TR4 is used for off track seek and is defined as shown in the following table.

Track Location	TR4	TR3	TR2	TR1	TR0
0	H	H	H	H	H
1	H	H	H	H	L
2	H	H	H	L	H
3	H	H	H	L	L
4	H	H	L	H	H
5	H	H	L	H	L
6	H	H	L	L	H
7	H	H	L	L	L
8	H	L	H	H	H
9	H	L	H	H	L
10	H	L	H	L	H
11	H	L	H	L	L
12	H	L	L	H	H
13	H	L	L	H	L
14	H	L	L	L	H
OFF TK (UP)	L	L	L	L	H
OFF TK (DN)	L	L	L	H	H

APPENDIX "A"

PIN 14 - RST. The RST line initiates a Reset pulse to the microprocessor. A low level signal to this line will initiate a reset to the microprocessor, which positions the head to the recalibration position and terminates any operation being performed.

PIN 20 - DS1. The DS1 line is used to select drive #1 when the drive is jumpered for Select #1. A low level signal at this line selects drive #1.

PIN 22 - DS0. The DS0 line is used to select drive #0. This is the standard select configuration for the drive. A low level signal at this line will select the drive for operation.

PIN 24 - HC. The HC line is used to select high write current for use with the high coercivity tapes. A low signal at this line selects the high write current to the write amplifier. This function is normally performed with the basic drive microrprocessor.

PIN 40 - WDA-. The WDA- line is used to supply digital write data information to the write amplifier circuitry.

PIN 42 - WDA+. The WDA+ line is used to supply digital write data information to the write amplifier circuitry. This signal is the inverse of the WDA- signal.

PIN 44 - THD. The THD line is used to select either the read or write threshold level. A low signal at this line will select the write threshold level, which is 25% higher than the read level. This function is normally carried out in the basic drive microprocessor.

PIN 46 - HSD. The HSD line is used to select high speed (90 IPS) rewind and fast forward operations. A low level signal at this line enables the high speed operation. This function is normally carried out in the basic drive microrprocessor.

PIN 48 - WEN. The WEN line is used to enable the drive to write data to the tape. Alow level signal to this line enables the drive to write data to the tape.

PIN 50 - EEN. The EEN line is used to enable the drive to erase data from the tape. A low level signal to this line enables the drive to erase the tape cartridge, but only if the drive is selecting Track 0 and moving forward from BOT.

OUTPUT SIGNAL DESCRIPTION. The output signal descriptions are as follows:

PIN 16 - RDP. The RDP signal line is used to transmit the read data pulse information to the formatter. This line will be at a low signal level when the read data level is true.

APPENDIX "A"

PIN 28 - UTH. The UTH line is used to transmit tape position status information regarding the upper tape hole status to the formatter.

PIN 30 - LTH. The LTH line is used to transmit tape position information to the formatter regarding the lower tape hole status. A low signal level at this line indicates that the lower tape hole has been detected.

PIN 32 - SLD. The SLD line is used to inform the formatter that the tape drive has been selected. A low level signal at this line indicates that the drive is selected.

PIN 34 - CIN. The CIN line is used to inform the formatter that a cartridge has been inserted in the drive. A low level signal at this line indicates that a cartridge is inserted in the drive.

PIN 36 - USF. The USF line is used to inform the formatter that the tape cartridge inserted in the drive is not write protected. A low level signal at this line indicates that it is safe to write data to the cartridge.

PIN 38 - TCH. The TCH line is used to transmit the tachometer information to the formatter.