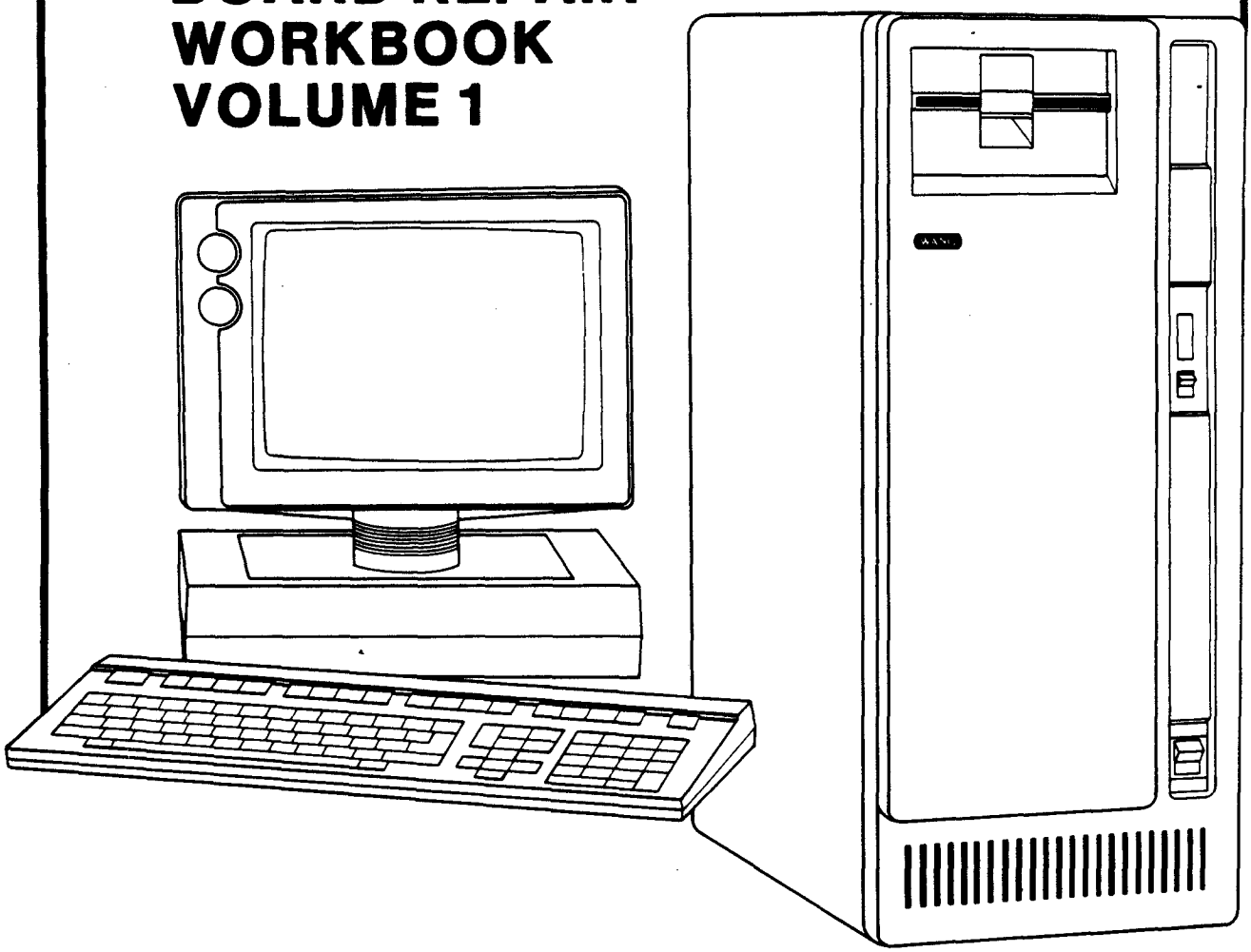
WANG

1403

OIS 40/50/60

BOARD REPAIR WORKBOOK VOLUME 1



CUSTOMER ENGINEERING
TRAINING AND DOCUMENTATION

741-9034

WANG

CUSTOMER ENGINEERING TRAINING CENTER

OIS 40/50/60
BOARD REPAIR WORKBOOK VOLUME 1

PREFACE

This document is intended to be used for TRAINING PURPOSES only. The material contained in this document, while accurate during the developement of this workbook, may not reflect the latest developments or changes to the OIS 40/50/60 system.

TECHNICAL SUPPORT DOCUMENTS

OIS 50 INTERNAL PRINTER CONTROLLER HARDWARE SPECIFICATIONS HM-60
OIS 40/50 RESOURCE MANAGEMENT UNIT THEORY OF OPERATION 751-0902
OIS 40/50 RESOURCE CONTROL UNIT THEORY OF OPERATION 751-0911
OIS 40/50 IWS FULL MATRIX CONTROLLER SPECIFICATION HM-67
WL-2630 OIS/VS COLLECTIVE GATE ARRAY SPECIFICATION HM-37
OIS-50 INTERNAL WISE SPECIFICATION REVISION 3 HM-85
OFFICE INFORMATION SYSTEMS OIS 40/50/60 741-1267
OIS SYSTEM ADMINISTRATION GUIDE 700-5562E

First Edition - December, 1985

OUTLINE OF WORKBOOK

TABLE OF CONTENTS VOL I

CHAPTER Page

SECTION 5
APPENDICIES

TABLE OF CONTENTS VOL II

CHAPTER Page

SECTION 6
Internal Printer Controller (IPC)

SECTION 7
Internal WISE Controller (IWISE)

CHAPTER Page

SECTION 7 (cont.)

SECTION 8
DIAGNOSTICS

CHAPTER Page

SECTION 9
APPENDICIES

LIST OF ILLISTRATIONS

SECTION 3
Resource Control Unit (RCU)

SECTION 4
Internal Workstation Controller (IWS)

LIST OF ILLISTRATIONS (cont.)

LIST OF TABLES

LIST OF TABLES (cont.)

SECTION 4
Internal Workstation Controller (IWS)

LIST OF TABLES (cont.)

SECTION I
INTRODUCTION

SECTION 1

OIS 40/50/60 WORKBOOK INTRODUCTION

This board repair workbook is comprized of two volumes. In the first volume the overall system will be covered in general. Then the reader will be presented with theory of operation for the three main circuit boards within the system, the Resource Management Unit (RMU), the Resource Control Unit (RCU), and the Internal Workstation Controller (IWS). Each of these sections will include a detailed description of the circuit board with limited bit chasing. The reader will be referred to Figures and Tables, along with references to the schematics to help him or her understand the operation of the unit. At the end of each section there is a quiz covering the information that was presented. After answering the questions in the quiz the reader can check his or her answers by referring to the answers in Appendix G.

In the second volume the reader will be presented with a detailed description of the theory of operation for the Internal Printer Controller (IPC), and the Internal WISE Controller (IWISE) circuit boards. The organization of the second volume is similar to that of the first as far as type of content and objectives.

Both volumes contain Appendices that provide relitive infromation about the circuit boards within that volume. Also located in the rear of the each volume is a master index that covers both volumes, this should provide the reader with a quick reference to just about any circuit operation.

If after you read this book you have any further questions or are interrested in learning more about the operation of the system, a list of reference books is provided in Appendix A of volume 1.

If while you are reading this workbook you come accross any errors that you feel need correcting, fill out the form provided at the back of the book and subbmit it to you supervisior. This feed back will help us improve the quality of the books that we produce and improve the quality of training that you receive.

1.1 OIS 40/50/60 SYSTEM INTRODUCTION

The OIS 40/50/60 system is a smaller version of the OIS 140 system that is contained in one package. The OIS 50 is capable of supporting up to four non-intelligent workstations and one or two non-intelligent printers. The logic providing the intelligence of these workstations and printers resides within the OIS 50 Master Processor. In addition the system will support up to four OIS 928 type serial devices, including intelligent workstations, image printers, phototypesetters, and telecommunication devices. The OIS 50 may be connected in a network configuration to more powerful Office Information Systems through the use of a Wang Inter-System Exchange Unit (WISE).

The OSI 40 is essentially a subset of the more versitile OIS 50. It was designed to be used as a stand alone system, capable of supporting one non-intelligent workstation along with one non-intelligent printer. As an option the OIS 40 may be configured to support one 928 type serial intelligent workstation or device. Like the OIS 50, it may be connected in an office system network via WISE, and has optional telecommunications capability.

The OIS 60 system represents the latest design in the OIS family of WANG Office Information Systems. In addition to the features of the OIS 40/50 configurations the OIS 60 provides four additional standard 928-type serial data link ports enabling the system to support a total of 12 peripheral devices, eight of these could be workstations. To support the additional ports the Resource Management Unit (RMU) and the Resource Control Unit (RCU) PCA's have been modified. The applicable theory and maintenance information (differences) for each will be covered as the RMU and RCU boards are discussed.

All three system contain an onboard 5 1/4 inch floppy archive drive, and either a 10 Meg or 30 Meg Winchester disk drive. The OIS 40 and 50 contain 10 Meg Winchester drives while the OIS 60 has a 30 Meg Winchester drive. In addition the OIS 60 has a hinged rear panel for easier access to the internal cabling for troubleshooting purposes.

The front panel of each of the units contains a rocker switch used for selecting which drive the unit will IPL from, (i.e. the Winchester or the Floppy). Directly above the IPL switch is located a LED status display. When the system is first powered on the unit will run an onboard BIT diagnostic. If an error is detected during the BIT test the status display will reflect the type of problem found. Refer to Appendix zzz for a complete list of error codes and their meaning.

1.2 SYSTEM OPERATION

In the OIS 40/50/60 system there are six printed circuit board that reside in the Master Processor, they are:

BOARD #	DESCRIPTION	SYSTEM
210-8266-A	Resource Management Unit (RMU)	((OIS 40/50))
210-8490-A	Resource Management Unit (RMU)	((OIS 60))
210-8267-A	Resource Control Unit (RCU)	((OIS 40/50))
210-8267-B	Resource Control Unit (RCU)	((OIS 60))
210-8274-A	Internal Workstation Controller (IWS)	((OIS 40/50/60))
210-8280-A	Internal Printer Controller (IPC)	((OIS 40/50/60))
210-8270-A	Internal WISE Controller (IWISE)	((OIS 40/50/60))
210-8269	OIS 50 Motherboard	((OIS 40/50/60))

The OIS motherboard is designed to hold a total of seven printed circuits boards, two of these boards must be the RMU and RCU boards. These two board contain all the Central Processing Logic for the Master unit. The five remaining slots accommodate the different peripheral controller boards in various combinations. Four of these slot may contain Internal Workstation Controllers (IWS), while the last slot may contain either an Internal WISE Controller (IWISE) or Internal Printer Controller (IPC). Depending on the system configuration, an additional IPC board may be substituted for one of the IWS controllers. FIGURE 1-1 shows a simplified block diagram of the OIS 40/50/60 system depicting the RMU, RCU, IWS,IPC and IWISE controllers, floppy and Winchester storage, and various peripheral devices. The flow of information between the various devices and PC boards occurs on the 50BUS. This bus is comprised of 40 signals representing address, data, select, and control information.

All of the Central Processing Logic for the OIS 40/50/60 is contained on the Resource Management Unit (RMU) and the Resource Control Unit (RCU) circuits boards. The Resource Management Unit (RMU) as its name implies, is responsible for the overall management of system operations. It runs the Operating System code and contains the system's main memory. The Resource Control Unit (RCU) shares the processing burden by controlling some of the more cumbersome tasks. In this way the RCU relieves the RMU of certain time-consuming operations, thus freeing the RMU to concentrate on overall system management. The net result is a system that runs faster and more efficiently than single-processor systems.

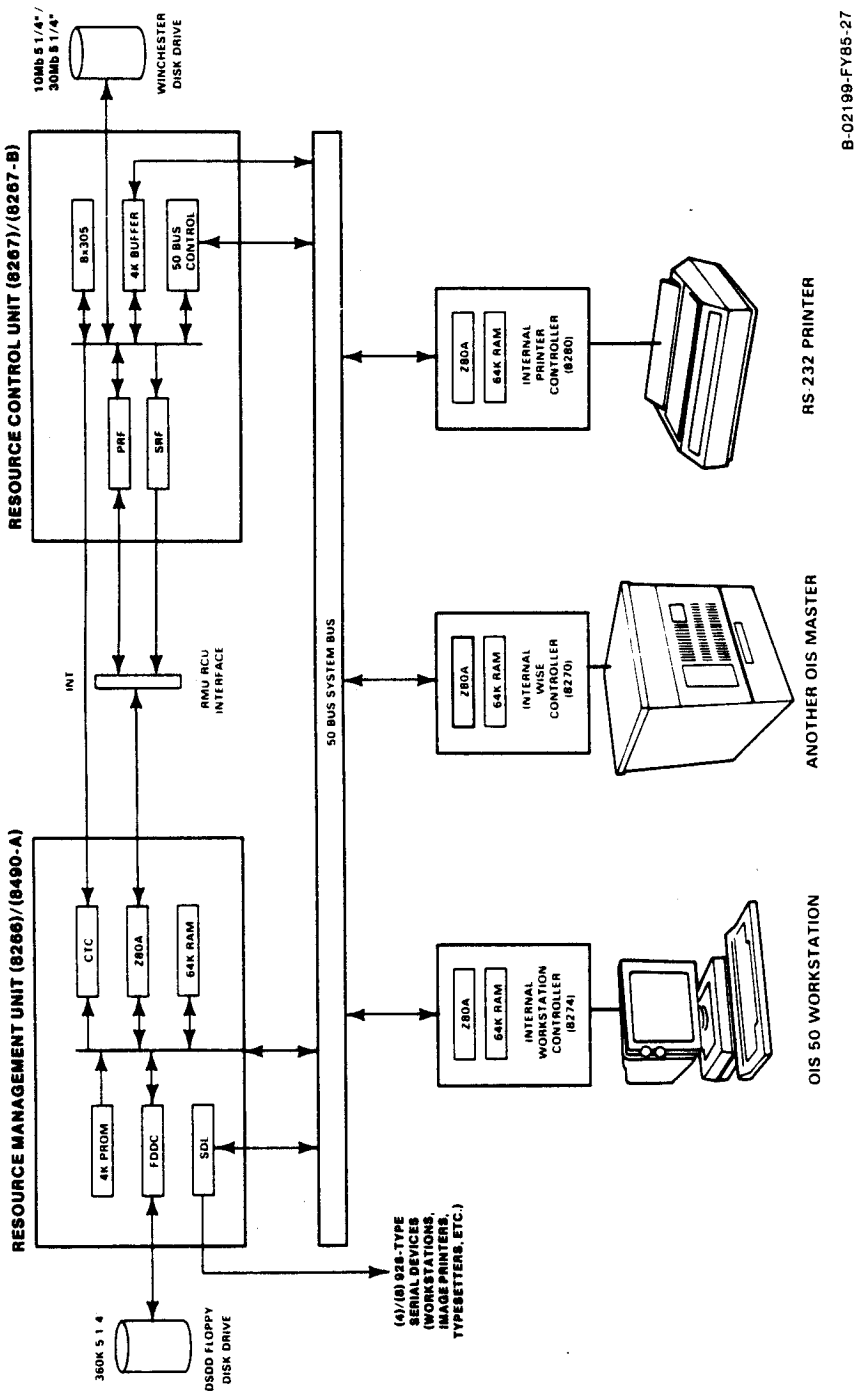


FIGURE 1-1
OIS 40/50/60 Simplified Block Diagram

1.2.1 Resource Management Unit (RMU)

The RMU contains a Z80 microprocessor that executes the system operating code, also on the RMU is located 64K of RAM overlayed by 4K of PROM memory. The RAM functions as main memory for the system, while the PROM contains the BIT power-up diagnostics and bootstrap loader code. The upper 256 bytes of memory is reserved Memory Mapped I/O. A Z80 Counter/Timer Chip (CTC) handles the various interrupts that the Z80 must respond to. The RMU is also responsible for controlling all operation involving the system's mini-floppy disk drive. An LSI Floppy Disk Controller chip (FDDC) resides on the RMU for this purpose. Finally, the RMU also contains all transmit and receive logic for all the external Serial Data Link (SDL) ports that connect the OIS 40/50/60 to 928-type serial peripherals. Although this SDL logic resides on the RMU board the RCU is actually responsible for its control.

1.2.2 Resource Control Unit (RCU)

The RCU board is designed around a Signetics 8X305 Microcontroller chip. It relieves the RMU's Z80 of a good deal of overhead by assuming the processing duties in four main areas:

1. Control and execution of all operations involving the 5 1/4" Winchester Disk Drive.

2. Execution of all block data transfers.

3. Control and arbitration of the 50BUS System Bus.

4. Control and execution of the Serial Data Link (SDL).

The 8X305 Microcontroller is the heart of the RCU board, and operates from instructions stored in firmware. A 4K Data Buffer is located on the RCU, and is involved in any operation that requires the transfer of block data. Logic on the RCU board generates commands and control signals that governs the operation of the 50BUS. Finally, all Serial Data Link (SDL) operations are under direct control of the 8X305 Microcontroller and additional support logic, even though the actual SDL transmit and receive circuitry is on the RMU.

In a multi-processor system such as this, communication between the two microprocessors is an important aspect of the system design. The RMU's Z80A and the RCU's 8X305 Microcontroller communicate with one another through the use of shared memory and interrupt signals. Two special memory areas are present on the RCU board. Both the Z80A and the 8X305 Microcontroller can access these locations. One area is called the Parameter Register File (PRF) while the other is labeled the Status Register File (SRF). When the Z80A of the RMU encounters and instruction that is the responsibility of the RCU, it will instruct the RCU to perform the task. To do this the RMU will write commands and parameter information into the Parameter Register File. The RCU then reads the (PRF) and interprets and executes the commands. When the RCU completes the task it writes status information into the Status Register File. The RMU reads the status information from the (SRF) to determine the outcome of the operation. For lengthy RCU operations such as block transfers the RMU will attend to other management duties while the RCU carries out the operation. When the RCU completes the task it will generate an interrupt to the Z80A indicating that the operation is complete.

As mentioned earlier, the 50BUS is the system's internal bus network comprised of 40 signals representing address, data, select, and control information. All information exchanged between the OIS 40/50/60 Central Processing Logic (RMU, RCU) and the various peripheral controllers (IWS, IPC, IWIS) travel on the 50BUS. The RCU initiates and governs all 50BUS transactions. Via the 50BUS the RCU is able to exchange information with a total of eight logical devices, called 50BUS Devices. Three of these logical devices reside on the RMU board:

1. Main Memory
2. The Floppy disk drive controller
3. The Serial Data Link transmit and receive logic

The remaining five logical devices correspond to the five Motherboard slots which house the various peripheral controller boards (IWS, IPC, IWISE).

A typical 50BUS transaction between the RCU and a 50BUS Device usually involves the transfer of block data. Consider the following example: While running the operating system, the RMU determine that it needs to read a portion of the workstations memory. Since the operation involves use of the 50BUS, and the RCU is responsible for operation of the 50BUS then the RMU instruct the RCU to perform the task and supplies the RCU with the particulars (which IWS, what portion of memory to read from, etc.) by writing to the (PRF). The RMU then goes about doing other housekeeping duties while the RCU performs the task. Using the 50BUS, the RCU selects the desired slave and places the slaves Z80A into a Bus-Request state so a DMA operation can take place. Then the RCU reads the desired slaves memory and transfers it byte for byte into the 4K Data Buffer on the RCU board via the 50BUS. When the operation is complete the RCU notifies the RMU by an interrupt. The RMU will then read the (SRF) to determine the results of the operation.

Three type of peripheral controller boards may be included in an OIS 40/50/60 system. They are; the Internal Workstation Controller (IWS), Internal Printer Controller (IPC), and the Internal WISE Controller (IWISE). Each of these controller boards contain a Z80A microprocessor along with 64K bytes of RAM used as slave memory. The following paragraphs contain a brief description of each board's responsibilities.

1.2.3 The Internal Workstation Controller (IWS)

The OIS 40/50/60 Master is capable of supporting up to four OIS 40/50/60 non-intelligent display terminals. The workstation is termed non-intelligent because the hardware and software that control the logical functions reside within the OIS 40/50/60 Master, on an (IWS) Controller board. The IWS Controller is responsible for providing:

1. The interface signals to the monitor electronics.
2. The interface logic to the serial keyboard.
3. The CRT, font, and main memory storage.
4. Interface logic required to communicate with the 50BUS.

1.2.4 The Internal Printer Controller (IPC)

The Internal Printer Controller (IPC) is designed to control a single RS-232C printer. The IPC receives commands and data from the RCU board via the 50BUS and communicates with the printer through an RS-232C serial interface. It is designed around a Z80A microprocessor running at 4 Mhz, and contains:

1. 50BUS interface logic.
2. RS-232C interface logic.
3. Printer control interface logic.
4. 64K of Dynamic RAM

1.2.5 The Internal WISE Controller (IWISE)

The internal WISE board provides a high speed communication path between the OIS 40/50/60 and any other WANG system that employs the standard 928-type Serial Data Link. The IWISE enables the OIS 40/50/60 to be used as clustered system, providing a communication link to a higher level Master Processor, such as the OIS 145 shown in FIGURE 1-1. Like the other controller devices attached to the 50BUS, the IWISE board depends on a Z80A running at 4 Mhz, and also contains:

1. Serial Data Link protocol logic.
2. 50BUS protocol logic.
3. 64K of Dynamic RAM and memory access arbitration logic.
4. DMA logic.

A complete theory of operation, and detailed circuit description for each of the circuit boards in the OIS 40/50/60 system is discussed in the following sections. Appendix A gives a complete list of all related documents for the OIS 40/50/60 system.

SECTION 1 QUIZ

1) What are the major differences between an OIS 50 and an OIS 60?

2) Name the five PCA assemblies that can reside in the main unit of either of the systems?

3) What two controller circuits reside on the RMU but are primarily controlled by the RCU?

4) In what four main areas does the RCU assume processing duties for the RMU?

5) What two memory areas do the Z80A and the 8X305 use to communicate with each other?

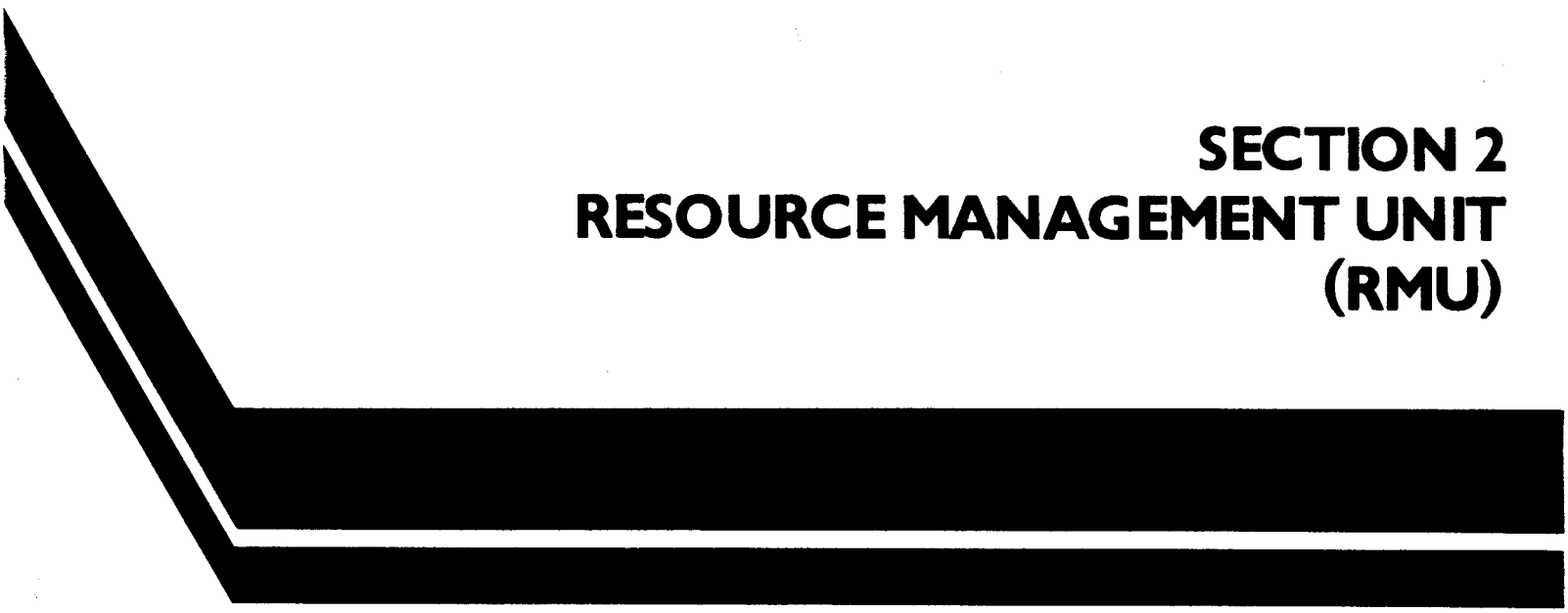
6) Who initiates and governs all 50BUS transactions?

7) What four items is the Internal Workstation Controller (IWS) responsible for?

8) How many printers can be connected to an Internal Printer Controller (IPC)?

9) What type of interface does the Internal WISE Controller (IWISE) require to communicate with other units?

10) Which Appendix contains a listing of reference materials that may be read to provide a better understanding of the OIS 40/50/60 system.



SECTION 2
RESOURCE MANAGEMENT UNIT (RMU)

SECTION 2

Resource Management Unit (RMU)

2.1 Resource Management Unit (RMU)

In this section we will discuss the theory of operation and circuit description for the Resource Management Unit (RMU). In lue of the fact that the RMU can not operate completely by itself, parts of the RCU circuits will also be discussed throughout this section.

While reading this section you should refer to the schematics in Appendix E so that you can follow along with the descriptions given. All circuit components will be referred to by their chip number and schematic location; Example L4 (1B2) indicates chip L4 located on sheet 1 row B column 2. If you are unfamiliar with a pectular type of chip that is being discussed you should refer to either the manufactures specification sheet or to the TTL Data Book by Texas Instruments. A quick reference of all the chips in the OIS 40/50/60 system is located in appendix C, each chip is listed by number and a brief description of its operation in the circuit is given. This Appendix is divided into parts representing each of the circuit boards located in the OIS 40/50/60. I recommend that you turn to Appendix C now and take a quick look at the listings.

Throughout the description of the circuits I will be using mnemonics to describe different signals that are generated. A complete listing of the meaning of these mnemonics are given in Appendix B. Any mnemonics that are active low and are indicated in the schematics by having a bar over the top will be prefixed in this document be an ampersand (&). Some signal have dual functions, such a R/W which when active low indicates a read operation and when active high indicates a write operation. To indicate which part of the mnemonic is active low I will place an additional ampersand next to the portion of the mnemonic that is active low, (i.e. &&R/W will represent the above description whereas R/W&& would indicate the reverse situation).

The 8266 Resource Management Unit used in the OIS 40/50/60 processor-based data processing system contains the 4-MHz Z80A Processor; the Counter Timer Chip, which generates interrupts and acts as a time-of-day clock; and the NEC765 Floppy Disk Controller (FDC), which manages operations involving the system's Floppy Disk Drive (FDD). (The 8X305 Microcontroller, the second processor of the OIS 50 multiprocessor system, is located on the 210-8267 Resource Control Unit board.) FIGURE 2.1-1 is a block diagram of the Resource Management Unit, and FIGURE 2.1-2 illustrates the Resource Management Unit's relation to the OIS 40/50/60 system.

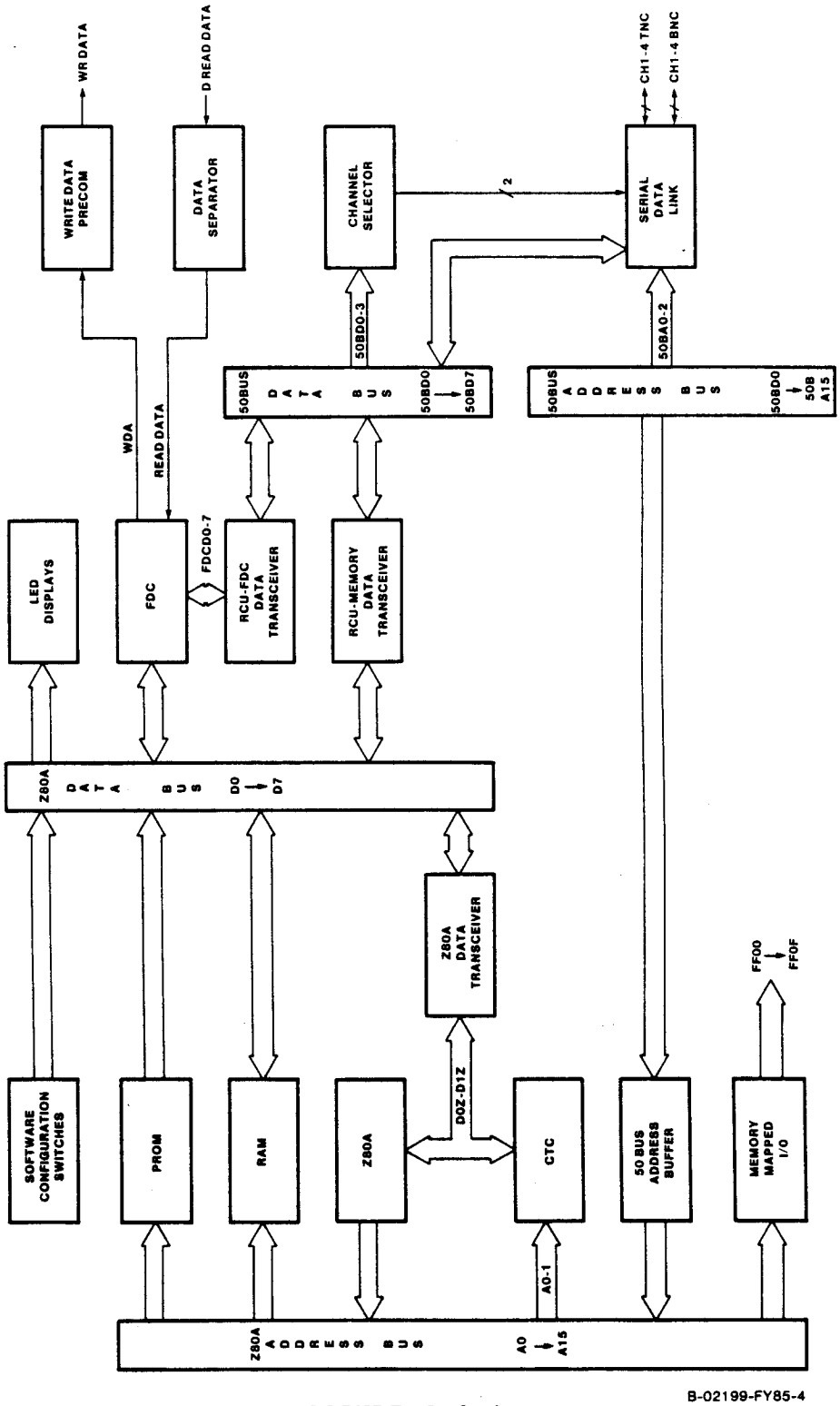


FIGURE 2.1-1
Block Diagram of the Resource Management Unit

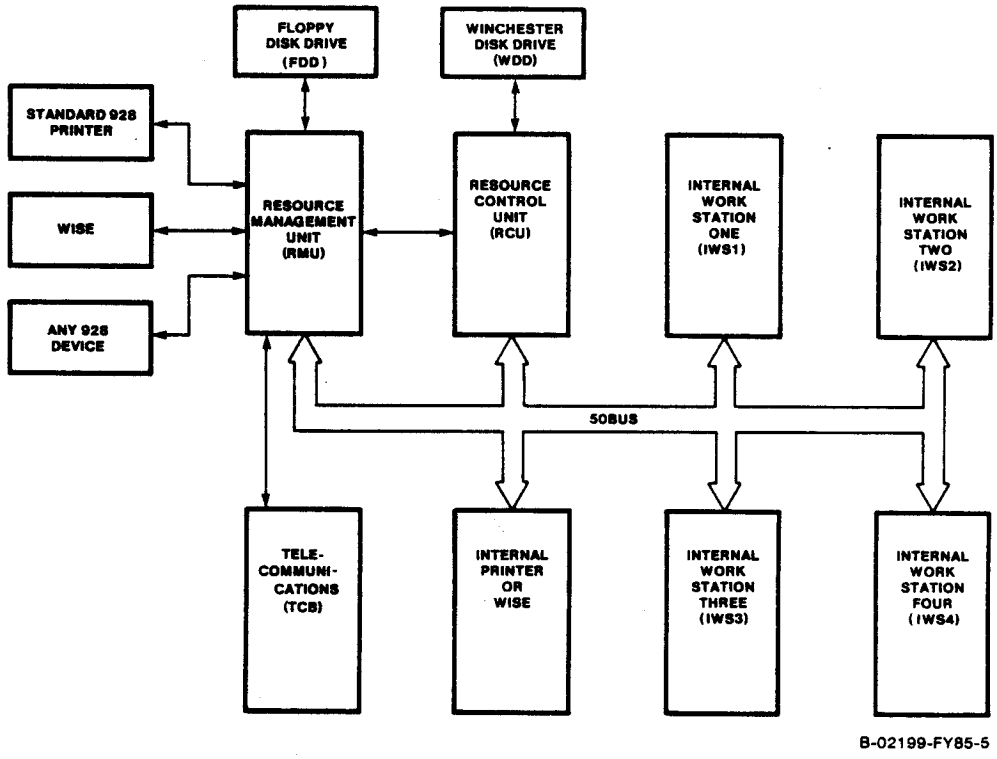


FIGURE 2.1-2
OIS 50 Block Diagram

Memory support for the OIS 40/50/60 is located on the Resource Management Unit (RMU) and is divided among RAM, PROM, and Memory Mapped Input/Output (MMI/O). Sixty-four kilobytes of RAM and 4k bytes of PROM are available for power-up diagnostics and Initial Program Load (IPL). Memory addresses from 1000-FF00 are used as random access memory, with the lower 4k bytes (0000-0FFF) overlayed by PROM. Memory addresses from FF00-FFFF are reserved for MMI/O.

The RMU board also contains serial transmit and receive logic for external Data Link ports 1-4. However, the 8X305 Microcontroller on the Resource Control Unit (RCU) board maintains control of these ports.

RMU-RCU Interaction

RMU-RCU communication involves shared memory, a Command Notification Bit (CNB), and the 8X305 Microcontroller interrupts that assert the Z80A. Two memory areas on the RCU board are shared between the Z80A and the 8X305: the 16-byte Parameter Register File (PRF) and the 12-byte Status Register File (SRF). Both the Z80A and the 8X305 can read from or write to the PRF; they cannot, however, access the PRF simultaneously. Only the Z80A can read the SRF, and only the 8X305 can write to it.

The RCU decodes RMU requests via the Parameter Register File. The Z80A microprocessor in the RMU loads the PRF with the command codes and data that the RCU needs to perform a specific operation. When the Z80A sets the Command Notification Bit, the 8X305 operates on the PRF as needed to complete the command. (Generally, the 8X305 moves the PRF data to its scratchpad RAM and then releases the PRF.) The PRF must be released quickly because the Z80A is suspended (ie, held in a bus request state) while the 8X305 uses the PRF.

PRF byte assignments depend upon the function requested (see Appendix G). Typically, the Z80A issues the FF20 (Command Request) byte and the FF22 (Specify Command) byte to the PRF. The RCU reads the bytes and defines the remaining bytes according to specific command requirements and then returns the FF21 (Command Acknowledge) byte to the PRF for the Z80A to read. To avoid invalid parameter errors, unused or undefined bytes should always be cleared to zero.

To perform a function that involves the RCU, the Z80A loads the command code and necessary data into the PRF. The Z80A then writes to address FF30 to issue the Command Notification Bit that initiates the command. Normally, the 8X305 is polling, waiting for the Command Notification Bit to be set. When the RMU issues a command, the 8X305 can perform one of two routines. If the command is an immediate command, the Z80A is awaiting command completion and the RCU must, therefore, execute the command immediately. If, however, the command is a non-immediate command, the RCU defers the command until it has completed any immediate operation in progress.

Upon receiving an immediate command, the RCU validates the command code, copies the PRF to its scratchpad RAM, completes the requested operation, and releases the RMU. Upon receipt of a non-immediate command, the RCU validates the command code, copies the PRF to its scratch RAM, sets RCU Busy status in the SRF, releases the RMU, completes the requested operation, and issues either an interrupt request or a Control Unit Busy (CUBUSY) signal to the RMU when the operation has been completed.

When the 8X305 Microcontroller performs a 1-byte operation, it does not immediately release the PRF. The Microcontroller holds the Z80A in a suspended state for a maximum of 1 ms (otherwise the lack of dynamic RAM refresh could cause a memory data loss). When the 8X305 releases the Z80A, the data and/or status from the 1-byte operation is immediately available to the Z80A via the SRF.

Status and error information returns to the RMU via the dual-ported SRF. When the 8X305 is busy, RCU Busy status information is set in byte FF10 of the SRF. Status information concerning Data Link block operations resides in SRF bytes FF11 and FF12. SRF bytes FF13-FF15 contain status information about the 1-byte Data Link opera- tions, and bytes FF16-FF1B contain status information concerning the Winchester Disk Drive (WDD).

2.1.1 Controls and Indicators

Two 7-segment displays (L3 and L4, located on the top edge of the RMU board and visible through the front bezel of the OIS 40/50/60 cabinet) indicate various errors. Error codes are displayed to indicate errors detected during power-up diagnostics or system errors (such as operator errors) detected after the operating system has taken control. Inverted data bits /D0-7 drive the LEDs, the data bits are inverted through L8 (1G3) and then supplied to drivers L5 (1G2) (activated by /FF08 write command) and L6 (1G1) (activated by /FF09 write command). L5 drives the L4 (1B2) lower display, and L6 drives the L3 (1B1) upper display.

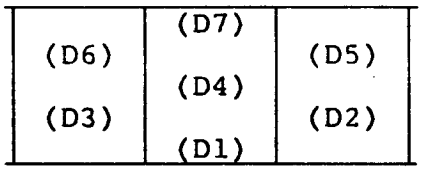
All seven display segments light up momentarily when power is applied to the OIS 40/50/60. The LEDs do not remain on long enough to be seen, however, and their lighted condition can be verified only with a Zebug (to establish that all LEDs are functioning correctly). Power-up LED illumination is created by the trailing edge of the /MR signal as it clocks the L4 and L5 drivers via L26 (1F3) while bits D0-7 are high.

Table 2.1-1 shows the codes used on bits D0-7 to create each hexadecimal symbol on the display. Table 2.1-2 lists the display error codes for power-up diagnostics and the error condition indicated by each symbol. Table 2.1-3 lists the display error codes for system errors and the error condition indicated by each code.

Switch SW2 is a pushbutton Restart Control Switch located on the interior of the OIS 40/50/60 cabinet on the front edge of the RMU board. If the operating system has control, activating SW2 generates a Non-Maskable Interrupt (NMI) to the Z80A. The NMI traps the Z80A to the Master Debugger routine (if the system is configured with the Master Debugger). The Master Debugger routine is used exclusively as a development tool.

Activating the Restart Control Switch during Test 1 (the LED Test) of the power-up diagnostics causes the tests following Test 1 to be skipped and initiates the bootstrap routine. To prevent error message generation, bit 7 of the Software Configuration Switches should be open prior to activating SW2 during Test 1. Activating SW2 with bit 7 open normally allows a smooth transition into the bootstrap routine.

In Table 2.1-2, "fatal*" next to an error indicates that the program cannot "continue on error" (not even when using the special DIP switch settings described in Table 2.1-4). "Fatal**" indicates that the encountered error halts the power-up sequence; however, tests can continue with the use of the DIP switch settings shown in Table 2.1-4. The test number is shown on the upper display, and the error number is shown on the lower display.



(D0) = decimal point

DISPLAY	CODE (HEX, without decimal point)	CODE (HEX, with decimal point
0	EE	EF
1	48	49
2	BA	BB
3	B6	B7
4	74	75
5	D6	D7
6	DE	DF
7	A4	A5
8	FE	FF
9	F4	F5
A	FC	FD
B	4E	4F
C	CA	CB
D	3E	3F
E	DA	DB
F	D8	D9

Table 2.1-1: LED DISPLAY CODES

Table 2.1-2: POWER-UP DIAGNOSTIC DISPLAY ERROR CODES

TEST NUMBER	TEST NAME	ERROR NUMBER
0	LED SEGMENT DISPLAY TEST Visual Feedback for Error Detection	
1	CTC TEST Read/Write Miscompare Down Count Failure	 (fatal**) 1 (fatal**) 2
2	UPPER RAM TEST Data Error (fatal**) Parity Error (fatal**) Parity Status Register Error Non-Maskable Interrupt (NMI) Error	 0-7 P (fatal**) PS (fatal**) P8
3	PRF TEST RCU Busy (loops until ready) RCU Command Response to RMU Command Not Accepted Command Invalid Incomplete Command Accepted None of the Above PRFs Affected	 (fatal*) .d (fatal*) .0 (fatal*) .1 (fatal*) .2 (fatal*) .3 (fatal*) .P

Table 2.1-2: POWER-UP DIAGNOSTIC DISPLAY ERROR CODES (cont.)

4	CTC TEST		
	CTC Not Interrupting (Channels 0-3)	(fatal**)	1
	Incorrect Vector	(fatal**)	2
.4	FDD DEADMAN TIMER TEST		
	No Interrupt (fatal**)	1	
	Incorrect Vector	(fatal**)	2
	Interrupt Not Caused by Deadman Timer	(fatal**)	3
	Floppy Disk Controller Has Interrupt Pending	(fatal**)	4
5	RCU INTERRUPT TEST		
	RCU Busy (loops until ready)	(fatal*)	.d
	RCU Response Bad on Block Write Command	(fatal**)	1
	Vector Error (fatal**)	2	
	No Interrupt Created	(fatal**)	3
.5	WINCHESTER DEADMAN TIMER TEST		
	RCU Busy (loops until ready)	(fatal*)	.d
	No Interrupt Requested	(fatal**)	1
	Vector Error	(fatal**)	2
	Drive Not Selected	(fatal**)	3
	Indexing Stuck Off	(fatal**)	4
	Indexing Stuck On	(fatal**)	5
6	SET SLAVE LIST		
	RCU Busy (loops until ready)	(fatal*)	.d
	RCU Command Response to RMU		
	Command Not Accepted	(fatal*)	.0
	Command Invalid	(fatal*)	.1
	Incomplete Command Accepted	(fatal*)	.2
	None of the Above	(fatal*)	.3
7	MAP SLAVE STATUS		
	RCU Busy (loops until ready)	(fatal*)	.d
	RCU Command Response to RMU		
	Command Not Accepted	(fatal*)	.0
	Command Invalid	(fatal*)	.1
	Incomplete Command Accepted	(fatal*)	.2
	None of the Above	(fatal*)	.3

Table 2.1-2: POWER-UP DIAGNOSTIC DISPLAY ERROR CODES (cont.)

	The following error numbers are displayed for about one second, but do not prevent continuation of testing.		
	1-Byte Data Link Status (DLS) 1-Byte Slave Status (SS) CPE Detected by DLS and SS CPE Detected Only by SS MPE Detected by DLS and SS MPE Detected Only by SS Detected by Data Link Status Received Parity Error No Data Timeout Check Power-Up State If slaves are not available, display error and loop on test.		.4 .5 .6 .7 .8 .9 .P .F
8	SLAVE CONTROL WRITE SECTION RCU Busy (loops until ready) RCU Command Response to RMU Command Not Accepted Command Invalid Incomplete Command Accepted None of the Above	 (fatal*) (fatal*) (fatal*) (fatal*) (fatal*)	 .d .0 .1 .2 .3
	The following error numbers are displayed for about one second, but do not prevent continuation of testing.		
	1-Byte Data Link Status (DLS) 1-Byte Slave Status (SS) CPE Detected by DLS and SS CPE Detected Only by SS MPE Detected by DLS and SS MPE Detected Only by SS Detected by Data Link Status Received Parity Error No Data Timeout Check Power-Up State		 .4 .5 .6 .7 .8 .9 .P
.8	READ SECTION RCU Busy (loops until ready) RCU Command Response to RMU Command Not Accepted Command Invalid Incomplete Command Accepted None of the Above	 (fatal*) (fatal*) (fatal*) (fatal*) (fatal*)	 .d .0 .1 .2 .3

Table 2.1-2: POWER-UP DIAGNOSTIC DISPLAY ERROR CODES (cont.)

	The following error numbers are displayed for about one second, but do not prevent continuation of testing.	
	1-Byte Data Link Status (DLS) 1-Byte Slave Status (SS) CPE Detected by DLS and SS CPE Detected Only by SS MPE Detected by DLS and SS MPE Detected Only by SS Detected by Data Link Status Received Parity Error No Data Timeout Check Power-Up State Compare Data to Correct Data	 .4 .5 .6 .7 .8 .9 .P .E
	If slaves are not available, a loop back to Test 7 is performed until a slave passes the test.	
	COMPARE DATA ERROR Register Contents: H - Data Received C - Data Expected D - XOR Data E - Slave Number L - Low Address	
9	IPL TEST FLOPPY DISK DRIVE I/O Error Addressed Drive Is Not Ready (loops on drive if not ready) WINCHESTER DISK DRIVE I/O Error Addressed Drive Is Not Ready (loops on drive if not ready)	 (fatal*) 1 2 (fatal*) .1 .2
	"UP" is displayed for approximately 1 s after successful completion of all power-up tests. Control then passes to bootstrap program.	

Table 2.1-3: SYSTEM DISPLAY ERROR CODES

Display Error Code (Hex)	Error Condition
FF	Parity
FE	Restart
FD	Software Debugger
FC	Hardware Debugger
FB	I/O Error Reading Master or Volume Label
FA	Illegal PROM Address
F9	Parity and Illegal PROM Address
DC	PROM Revision Levels Not Compatible
DD	No RCU Response
DE	XMM Configured for 64k Master
DF	Data Link Error During I/D Transfer (XMM)
E0	Invalid Volume Label (Hash Code)
E1	Not System Disk
E2	Bad Configuration - Too Little Memory
E3	Bad Configuration - System Disk Excluded
E4	Insufficient Memory for Control Blocks (TCB)
E5	Insufficient Memory for Control Blocks (VCB)
E6	Insufficient Memory for Control Blocks (DCB)
E7	Insufficient Memory for Control Blocks (FCB)
E8	Unsupported Disk Type
E9	Insufficient Memory for Buffers (VAU Map)
EA	Insufficient Memory for Buffers (Catalog)
EB	Incorrect PROM Installed
EC	Unsupported Timer Interval
ED	Cannot Mount System Disk
EE	Invalid SMD/CMD Characteristic Switches
EF	Invalid IPL Sector

IPL Device Select Switch SW1 is a rocker switch located on the OIS 40/50/60 control panel. When read by the /FF04 command, SW1 selects either the Floppy Disk Drive or the Winchester Disk Drive as the system drive for initial program loading. When SW1 is in position 3, D7 is cleared to 0 and the Floppy Disk Drive is selected to IPL the system; when SW1 is in position 1, D7 is set to 1 and the Winchester Disk Drive is used to IPL the system.

SW3 is an 8-bit switch bank used to select various software configurations during the power-up sequence. SW3 switch settings define, via data bits D0-7, which software configurations run on the OIS 40/50/60. Switch settings are passed through the L49 Software Configuration Switch Buffer when the /FF05 command is activated. The SW3 Software Configuration Switches, used only during power-up diagnostics, are sensed in the order listed in Table 2.1-4.

Table 2.1-4: SOFTWARE CONFIGURATION SWITCH SETTINGS

Switch Number	Function
7	Software configuration switch settings are of no significance to the built-in test unless this bit is set (ie, D7 = 1).
0	When cleared (D0 = 0), causes program to loop on power-up diagnostics.
1	When cleared (D1 = 0), causes program to stop on error.
2	When cleared (D2 = 0), causes program to loop on error.
3	When cleared (D3 = 0), causes program to continue on error.
4-6	Ignored by diagnostics.

Power-Up Protection

Power-Up protection circuitry (L131 (2F3-8), composed of four comparators) monitors the 5-V (pin 9), -5-V (pin 4), and 12-V (pin 7) power levels to ensure that the proper voltages are reached before the Z80A is released to place the OIS 40/50/60 into an operative mode. When the voltages are at their correct levels, the active &AUTO RESET signal from L131 pin 13 is deactivated, allowing the Z80A to begin operation. The &AUTO RESET signal is converted into the Master Reset (&MRC) signal and sent to the other boards of the OIS 40/50/60 system. &MRC holds each OIS 40/50/60 board reset until proper voltage levels are reached.

2.1.2 Clock Generation

Y1 generates the 16-MHz base timing signal (CK) from which the clock generation circuitry (L31 (1K2) and L32 (1I3/4), shown in FIGURE 2.1-3) creates all other clock signals used on the RMU board. L32 gate 1 divides the 16-MHz signal to create the 8-MHz 1/2Phi signal that synchronizes the generation of Z80A Data Bus direction control signals and the RAS signal. L32 gate 2 divides the 8-MHz signal to create the 4-MHz Phi-Z and Phi-ZC signals that drive the CTC and the Z80A processors. L31 gate 2 generates the /Phi-A signal used for FDC write timing and for the Z80A wait circuit. FIGURE 2.1-4 illustrates the relationship of the various clocking signals.

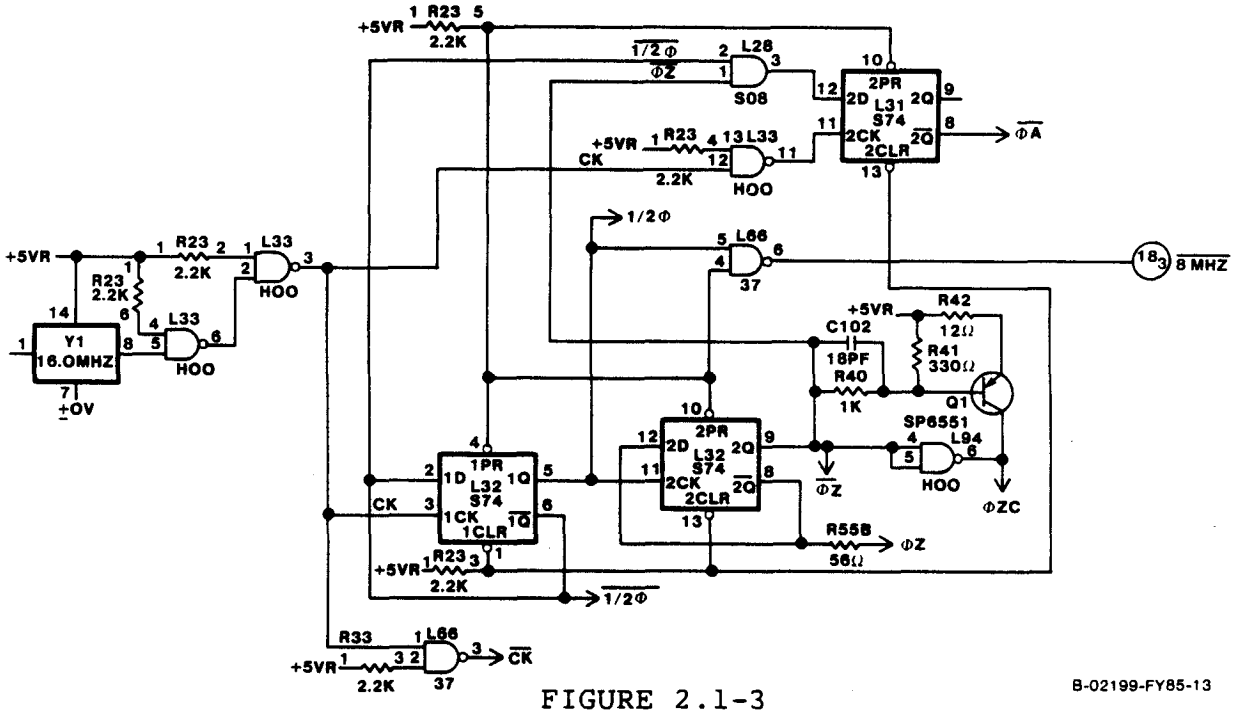


FIGURE 2.1-3
RMU CLOCK LOGIC

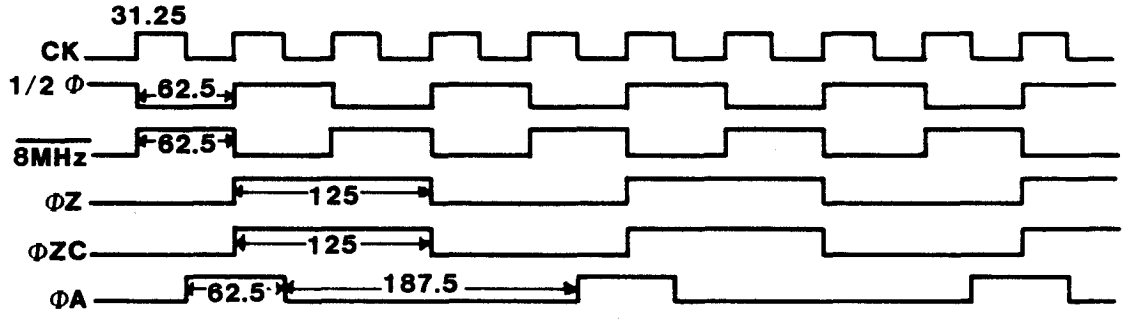


FIGURE 2.1-4
RMU TIMING

2.1.3 Memory Mapped Input/Output

Memory addresses FF00-FFFF are reserved for Memory Mapped I/O (MMI/O) operations. FF00-FF0F are decoded on the RMU board, and FF10-FF40 are decoded on the RCU board. MMI/O Decoder L80 on the RMU board decodes address bits A0-3 into I/O Port Commands /FF00-/FF0F (defined in Table 2.1-5). Address bits A4-15 are decoded through gates L64 (1J10) and L95 (1K11) to enable the MMI/O Decoder L80 (1J/K9). MMI/O Logic is shown in FIGURE 2.1-5.

The RMU MMI/O Decoder is enabled when address bits A8-15 are high and address bits A4-7 are low: A8-15 select a memory mapped operation, and A4-7 enable decoding of the RMU Memory Mapped I/O operation. Address bits A8-15 assert L95 to generate the Port Address (&PORTAD) signal from pin 8. The combination of &PORTAD and the &MREQ signal (which is active for any memory request operation) asserts L63 (1K10) to generate the &MMI/O enabling signal that asserts L80 pin 18. During MMI/O operations BUSAK is low on pin 5 of L63 to gate the &MMI/O signal through. BUSAK is applied at L63 to prevent an incorrect DMA address from generating an MMI/O operation. Low-order address bits A4-7 assert L64 to generate the second MMI/O Decoder enabling signal, which asserts L80 pin 19. If A4-7 are low, ports FF00-FF0F on the RMU board are decoded from A0-3; if A4-7 are high and the &MMI/O signal is active, ports FF10-FF2F on the RCU board are decoded.

During Memory Mapped I/O operations the Wait State Insert Flipflop (L31 (1K6)) generates the PWAIT signal to delay the Z80A by one complete WAIT State. The WAIT state allows time for propagation delays and for ports that have slow response times. PWAIT generation is initiated when the &MMI/O signal asserts L11 (1K6) to generate a signal that asserts L31 pin 2. When L31 is clocked by the /Phi-A signal it generates &PWAIT from pin 6. &PWAIT asserts the Z80A's &WAIT pin to insert the necessary WAIT state. PWAIT from pin 5 is fed back to hold L31 latched for one complete WAIT state.

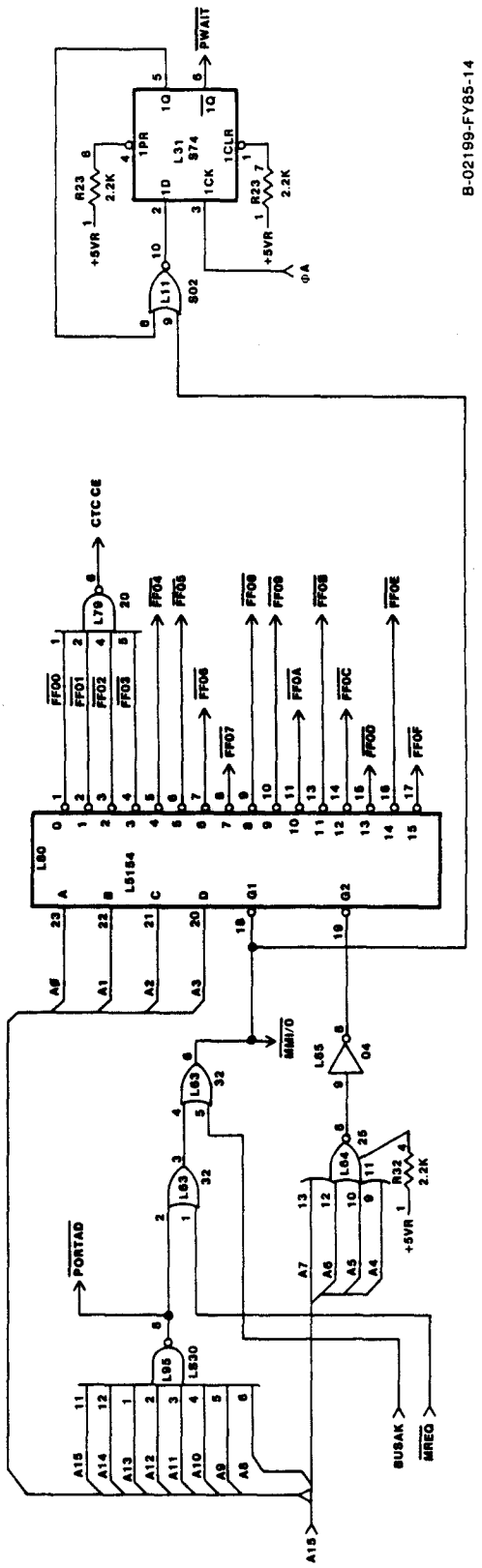


FIGURE 2.1-5
MMI/O Logic

When a command such as &FF0B is issued, it can be used to perform either a read or a write operation. To create individual signals for read and write operations the &FF0B signal is gated with the &RD1 and &WR signals at L108 (1F8), &FF0B asserts pins 9 and 13 of L108. In read operations, &FF0B is gated through L108 by the active &RD1 signal asserting pin 12 to create the &RFF0B signal from pin 11. In write operations, &FF0B is gated through L108 by the active &WR signal asserting pin 10 to create the &WFF0B signal from pin 8.

Table 2.1-5: RMU MEMORY MAPPED I/O COMMANDS

PORT COMMAND	DEFINITION
&FF00-&FF03	Writes Counter Timer Chip channels. Also writes interrupt vector, control word, and time constant assignments as follows: COMMAND CHANNEL &FF00 00 &FF01 01 &FF02 02 &FF03 03 Read CTC internal down counter of one of the four CTC channels.
&FF04	Read IPL Device Select Switch (SW1), which determines Disk Drive to be used for IPL. D7 = 0 - Floppy Disk Drive D7 = 1 - Winchester Disk Drive
&FF05	Read Software Configuration Switches (SW3) to define running software configurations.
&FF06	Read Floppy Disk Controller Status Register.
&FF07	Read Floppy Disk Controller Data Register (&RFF07). Write data to Floppy Disk Controller (&WFF07).

Table 2.1-5: RMU MEMORY MAPPED I/O COMMANDS (cont.)

&FF08	Write lights lower Error LED Display (see Tables 1-1, 1-2, and 1-3).
&FF09	Write lights upper Error LED Display (see Tables 1-1, 1-2, and 1-3).
&FF0A	Write resets Floppy Disk Controller Chip. Two &FF0A writes must be performed to software-specify a 10-us reset pulse. The first &FF0A issued turns the reset pulse on and the second &FF0A turns the pulse off. Reset pulse width must be at least 10 us.
&FF0B	Read Floppy Disk Drive Status Register (/RFF0B). D0 = 1 - File Ready. D1 = 1 - Disk Selected. D2 = 1 - Door Disturbed. (Cleared by &RFF0B when door is closed.) D3 = 1 - Deadman Timer Interrupt Pending. D4 = 0 - DMA Request Pending. D5 = 0 - Interrupt Request Pending. D6 = 0 - Not Used. D7 = 0 - Not Used. Write Floppy Disk Drive Motor Control and Drive Select (&WFF0B) data . D0 = 1 - Turn Floppy Disk Drive Motor On. D1 = 1 - Select Floppy Disk. D6 = 1 - Terminal Count Asserts Floppy Disk Controller. D7 = 1 - DMA Acknowledge Asserts Floppy Disk Controller.
&FF0C	Issued immediately after an FDD operation is sent to the FDC. Write sets the deadman timer and trips a 540-ms timeout that determines whether FDC is "frozen." Timeouts issue a Floppy Interrupt (FINT) signal to the CTC.

Table 2.1-5: RMU MEMORY MAPPED I/O COMMANDS (cont.)

&FF0D	Primarily used in diagnostics. Write controls parity (even or odd) written to memory. D6 = 1 - Prevents a memory error (&ME) from generating an NMI to the Z80A. D7 = 0 - Even Parity. D7 = 1 - Odd Parity.
&FF0E	Reads memory parity bit (&RFF0E). D7 = 1 - Parity Error. Write enables or disables access to diagnostic /IPL PROM (&WFF0E). PROM is mapped into memory locations 0000-0FFF. D7 = 0 - PROM Disabled. D7 = 1 - PROM Enabled.
&FF0F	Write clears RAM Parity Error Bit.

2.2 Z80A CENTRAL PROCESSOR UNIT

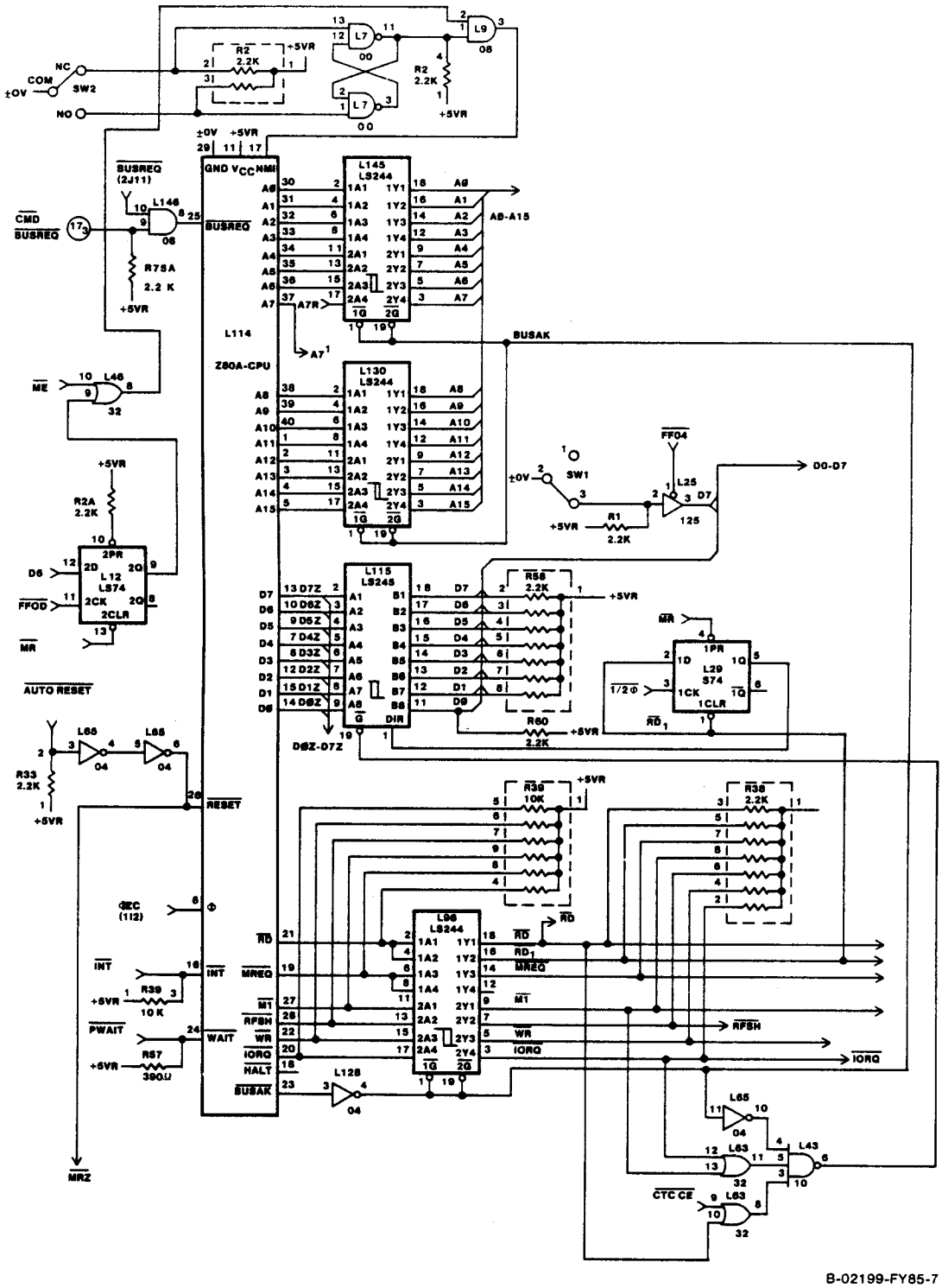
The Z80A Central Processor Unit (L114 (1E-J13)) resides on the 8266 Resource Management Unit board. When power is first applied, the active &AUTO RESET signal on L114 pin 26 automatically resets the Z80A. When the voltages are at their correct levels, &AUTO RESET is deactivated to allow the Z80A to begin operation.

Address lines from the Z80A are supplied to the L145 and L130 (1I/J13) Address Bus Drivers. When enabled by the inactive BUSAK signal, L145 and L130 gate the Z80A address lines onto the A0-15 Address Bus. Separate enabling and direction control logic controls Data Transceiver L115 (1G13), which controls the data flow to and from the Z80A. When enabled by an inactive &BUSAK signal, Control Line Driver L96 (1E12) drives the Z80A control signal outputs. Z80A access logic is shown in FIGURE 2.2-1.

2.2.1 Z80A CONTROL LINES

a. &BUSREQ (input)

The Z80A can be halted momentarily by either an active &BUSREQ (Bus Request) or &CMD BUSREQ (Command Bus Request) signal asserting pin 25. Requesting the Z80A bus forces the Z80A to relinquish bus control and, therefore, allows the RCU to gain control of the Z80A Data and Address Buses. The RCU generates two signal to the RMU when it requires the Z80A data and address bus, they are &5ØBSLCTØ and &5ØBUSREQ. These enter at 2K12 and are ORed together to generate &BUSREQ to the Z80A, and &BUSREQ also removes the preclear from L127 (2K10) so that the Z80A can generate a &5Ø BUSAK (bus acknowledge). Once the Z80A receives the bus request it will complete the operation that it is doing and then activate &BUSAK at pin 23 of the Z80A. This signal is then sent to L127 at 2K10 where it is placed on the "D" input. Then on the next phase Z clock L127 will set and generate &5Ø BUSAK to the RCU. When the Z80A activated the &BUSAK on pin 23 it also tristated its data and address bus. The Z80A can also be placed into this type of condition by the &CMDBUSREQ signal. The RCU generates the &CMDBUSREQ signal at 1J14 to directly request the Z80A buses after the Z80A has issued a command to the RCU.



B-02199-FY85-7

FIGURE 2.2-1
Z80A Access Logic

b. Interrupts (input)

The Z80A can be interrupted by non-maskable interrupt (NMI) requests arriving on pin 17 or by maskable interrupt requests asserting pin 16. NMIs result either from memory errors or from activation of the Restart Switch. Maskable interrupts are generated by the CTC in response to either active &CUBUSY, &WSKCMP, or &FINT (&DMI) signals, or the programmable time-of-day clock.

1. NON-MASKABLE INTERRUPTS (input)

If during the reading of the RMU's main memory a parity error is detected the &ME will be sent to L46 at (1I14). This will be passed through as long as the system is not doing a MMI/O operation &FF0D with D6 high, (usually done during diagnostics). The active &ME signal will then be placed on pin 17 of the Z80A after it passes through L9 at (1K12).

The other source of nonmaskable interrupt is from SW2 the Restart Switch. Them SW2 located at 1K14 is depressed ground will be placed on the NO contact and force latch L7 (1K13) to place a zero pin 17 of the Z80A after passing through L9 (1K12). When SW2 is released latch L7 will change states and clear the MNI.

When the Z80A receives a NMI request on pin 17 it will ignore the next instruction that it fetches an jump directly to its hardware default address of ØØ66H. At this location there will be a restart routine that will determine where the interrupt came from. This will be discussed in more detail in the section on parity checking.

2. MASKABLE INTERRUPTS (input)

The Z80A receives maskable interrupts on pin 16 from the CTC (Counter Timer Chip) at 3J3. The CTC generates this interrupt in response to either active &CUBUSY, &WSKCMP, or &FINT (&DMI) signals, or the programmable time-of-day clock. When the CTC generates an interrupt to the Z80A it will also place a vector corresponding to the location of the interrupt routine on the Z80A data bus. The Z80A will then jump to this location and perform the required task. A further discussion on the workings of the CTC can be found in the section covering the CTC.

c. WAIT (input)

During Memory Mapped I/O operations, &PWAIT asserts the Z80A's &WAIT pin to delay the Z80A by one complete WAIT state. The &PWAIT signal is generated by L31 (1J6), the Wait State Insert Flipflop, whenever the flipflop is driven by the &MMI/O signal, which is asserted during all MMI/O operations.

d. CONTROL OUTPUTS

Z80A control outputs are supplied to L96 (1E12), the Control Line Driver, when the inactive &BUSAK signal enables the driver. (&BUSAK is inactive when the Z80A has bus control.)

The &RD and &MREQ are the only control signals generated by the RCU during DMA operations. They are generated when the RCU needs to access memory (the Z80A is held inactive until the &50BBUSREQ signal from the RCU is deactivated).

&M1 is active on Z80A pin 27 during op-code fetch cycles. When a memory read or write is about to occur, the &MREQ signal from pin 19 is activated. When a read operation is about to occur, &RD goes active on pin 21, and when a memory or I/O write operation is about to occur, &WR goes active on pin 22. The Input/Output Request (&IORQ) signal from pin 20 is active only during interrupt acknowledge cycles.

The Refresh signal (&RFSH) travels to the Refresh Multiplexer Logic and the Memory Request Logic to generate the RAS-only refresh operation. Pin 28 of the Z80A generates &RFSH during the last two "T" states of an op-code fetch.

During diagnostic operations, the &FFOD command can be asserted on L12 (1H14) pin 11 with D6 = 1 on pin 12 to prevent a memory error from interrupting the Z80A with an NMI. L12 will then generate a high signal from pin 9 that prevents the Memory Error (&ME) signal from being gated through L46 (1I14).

2.2.2 ADDRESS BUS

Address lines from the Z80A are supplied to Address Bus Drivers L145 and L130 (1I/J12). L145 drives the low address byte and L130 drives the high address byte. When the inactive &BUSAK signal asserts pins 1 and 19 of both L145 and L130, the drivers place the addresses onto the A0-15 Address Bus. &BUSAK is inactive while the Z80A has bus control.

L145 does not drive address bit A7 directly from the Z80A. Rather, this bit is sent to the A7 Refresh Bit Multiplexer where it is multiplexed with a synthetic A7 bit used for RAM refresh purposes. The multiplexed result, A7R, is driven by L145 (1J13) as the A7 address bit. (Section 2.4.3 provides a detailed explanation of the refresh operation.)

L129 and L144 located at (2I/K13), are address buffers between the 50BUS and the Z80A's A0-15 Address Bus. The RCU uses these RCU-Memory Address Buffers when it provides an address for a memory access operation. The buffers move the address from the 50BA Bus when the enabling signal, which is generated by L127 (1K10) in response to an RCU bus request, is present. (Sections 2.5.1 and 2.5.2 provide a detailed explanation of the RCU memory access operation.)

2.2.3 DATA BUS

Data lines to and from the Z80A pass through Data Transceiver L115 (1G13), which produces outgoing data or accepts incoming data depending on enable and direction control inputs. When the Data Transceiver is disabled, the CTC has access to the Z80A via the D0Z-D7Z bus. The Data Transceiver is disabled (ie, tristated) when a high signal generated by L43 (pin 6), located at (1F8), asserts L115 pin 19. Only the CTC has access to the Z80A via the D0Z-D7Z Bus when the Data Transceiver is disabled.

Three operations can disable the Data Transceiver. When the Z80A does not have bus control (eg, in a DMA operation) the active &BUSAK signal asserts L43 (1F8) pin 4 to disable the Data Transceiver. While the CTC is being read via the D0Z-D7Z Bus, the CTC Chip Enable (&CTC CE) signal and the &RD signal assert L63 (1F9) pins 9 and 10, respectively. L63 then generates a signal that asserts L43 to disable the transceiver. When the Z80A is in an interrupt-acknowledged service routine, active &IORQ and &M1 signals assert L63 (pins 12 and 13, respectively). L63 then generates a signal that causes L43 to disable the transceiver. The CTC can then access the Z80A via the D0Z-D7Z Bus.

L29 (1G10), the Data Transceiver Control Flipflop, governs the direction of data flow to and from the Z80A. During a read from memory operation, the active &RD1 signal asserts the clear pin (pin 1) of L29, driving the pin 5 output low. (&RD1 is used through L29 to prevent bus contention problems.) The low signal from L29 pin 5 places the transceiver in the read from memory direction (B to A) by asserting pin 1. Write operations are performed when the &RD1 signal is inactive. The inactive &RD1 signal asserts pin 2 of flipflop L29. Then, when clocked by the &1/2Phi clock, L29 issues a high signal from pin 5 to place the transceiver in the write direction (A to B).

L89 (2I10) is a Data Transceiver between the 50BUS and the Z80A's D0-7 Data Bus. During RCU memory access operations, when the necessary enabling and direction control signals are present, the L89 RCU-Memory Data Transceiver moves data to and from the 50BD Bus. The control signals are generated in response to RCU bus request and Read/Write signals. (Sections 2.5.1 and 2.5.2 provide a detailed explanation of the RCU memory access operation.)

2.3. COUNTER TIMER CHIP

The Counter Timer Chip (CTC), L82 (3J3) is a programmable, 4-channel device that generates maskable interrupts and provides a time-of-day clock. The chip has an 8-bit data bus, eight control outputs, and 10 control inputs (including the clock input). Counter Timer Chip interrupts have the highest priority after non-maskable interrupts; therefore, the Enable Interrupt input (pin 13) is held in a high, enabled state at all times. The Counter Timer Chip Data Bus (D0-7Z) provides an all-purpose, free access path between the Z80A and the Counter Timer Chip. To reset the Counter Timer Chip, the Master Reset (&MRZ) signal asserts pin 17. (FIGURE 2.3-3 shows the Counter Timer Chip access logic.)

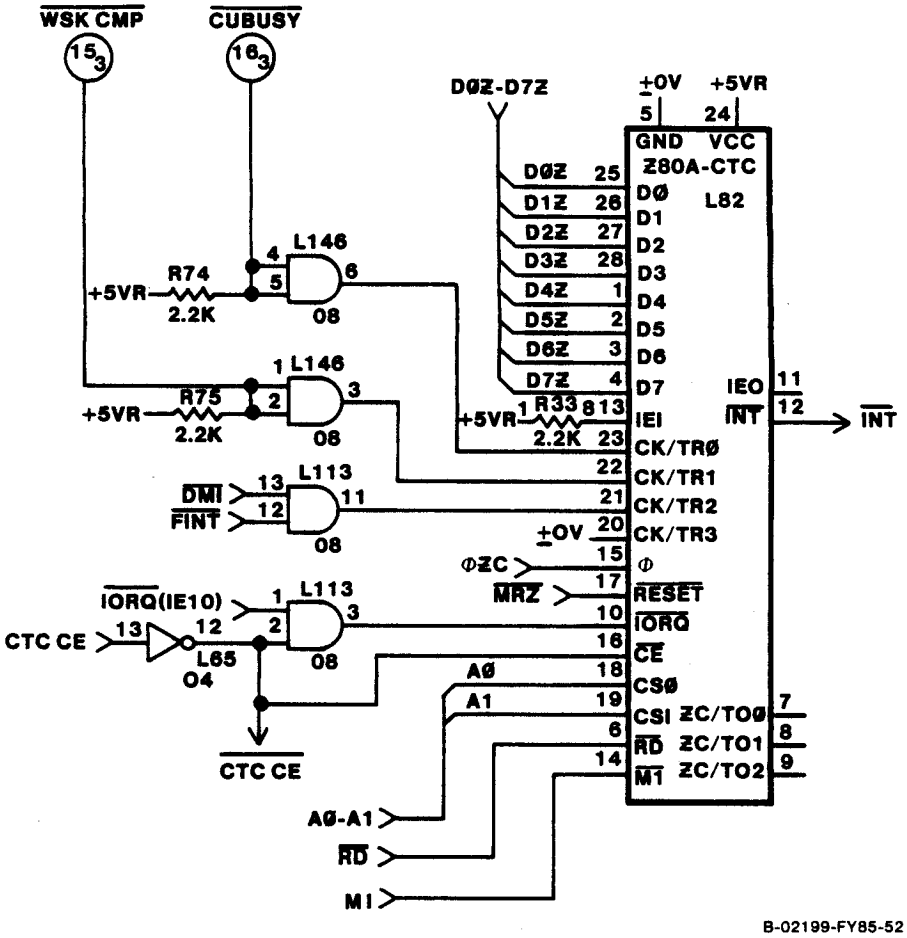


FIGURE 2.3-1
Counter Timer Chip Access Logic

When the Counter Timer Chip issues the Interrupt (&INT) signal from pin 12, it also places a unique vector on the data bus. The CTC-generated vector combines with information programmed in the Z80A Instruction (I) Register to provide a pointer to a table. This table contains a list of interrupt service routine addresses that direct the Z80A to the proper service routine.

CTC channels 0, 1, and 2 are set in the counter mode and are used to prioritize Z80A interrupt requests received by the Counter Timer Chip. Channel 0 generates an interrupt request when the RCU has completed an operation and is, therefore, no longer busy (&CUBUSY, pin 23). Channel 1 generates an interrupt request when the Winchester Disk Drive (WDD)completes a seek operation (&WSKCMP, pin 22), and channel 2 provides interrupt support for Floppy Disk Drive (FDD) functions such as the deadman timer (&DMI, pin 21 via L113 (3J5)) and Floppy Disk Controller Interrupt (&FINT, pin 21 via L113). Channel 3 is programmed to operate in the timer mode for use as a time-of-day clock.

Buffered address bits A0B and A1B (on pins 18 and 19 of L82) provide the channel selection signals to the CTC. A0B and A1B select one of the four CTC channels (channel numbers are coincident with A0B and A1B's hex values) to generate prioritized interrupts. The CTC Chip Enable (&CTC CE) signal asserts L82 pin 16 to enable the CTC for operation. The Z80A issues the &RD, &IORQ, and &M1 control signals to the CTC. &RD is active on pin 6 when a read operation is pending, &IORQ is active on pin 10 during interrupt acknowledge cycles, and &M1 is active on pin 14 during op-code fetch and interrupt acknowledge cycles.

2.4. MEMORY

Memory support for the OIS 40/50/60 processors is divided among RAM, PROM, and Memory Mapped Input/Output (MMI/O). Sixty-four kilobytes of RAM and 4k bytes of PROM are available on the RMU board for power-up diagnostics and Initial Program Load (IPL). Memory addresses from 1000-FF00 are assigned to RAM, with the lower 4k bytes (0000-0FFF) overlayed by PROM for power-up diagnostics and initial bootstrap. Memory addresses from FF00-FFFF are reserved for MMI/O.

The Resource Management Unit provides 64k bytes of RAM (with parity) in nine 64k-bit dynamic memory chips. PROM-resident programs normally overlay memory addresses 0000-0FFF. RAM addresses 0000-0FFF are not normally available but can be accessed under software control (via the MMI/O &FF0E command) following the power-up sequence and during diagnostics. A 2-position switch on the OIS 40/50/60 control panel selects either the Floppy Disk Drive (FDD) or the Winchester Disk Drive (WDD) as the device to be used for initial program loading. After the IPL and diagnostics, RAM can be banked in from 0000-0FFF.

During the power-up routine, memory is loaded with data carrying bad (ie, odd) parity bits. This data will cause a parity error if it is read from memory that has not been initialized (ie, loaded with valid data). The Memory Parity Bit Control Flipflop (L30 (1D3), gate 2Q) controls the parity of the data loaded into memory. Upon receipt of an &FF0D command with D7 = 1, L30 generates signals that cause the gating logic of L26 and L46 (1D1) to issue an odd PARIN signal, loading all bad parity bits upon power up. During normal operation (due to power-up default), L30 allows the even parity bit from L27 into memory.

2.4.1 Z80A and Direct Memory Access Paths

Either the Z80A or the RCU can access RAM via the A0-15 Address Bus and the D0-7 Data Bus as shown in FIGURE 2.4-1 . (The actual memory access circuitry appears in FIGURE 2.4-2.) The Z80A accesses memory directly (through buffers) from its data and address output pins. The RCU gains Z80A bus control for a DMA operation by issuing either an active Command Bus Request (&CMD BUSREQ) or an active 50BUS Bus Request (&50BBUSREQ) signal. The Z80A responds with an active &BUSAK (Bus Acknowledge) signal to release bus control to the RCU.

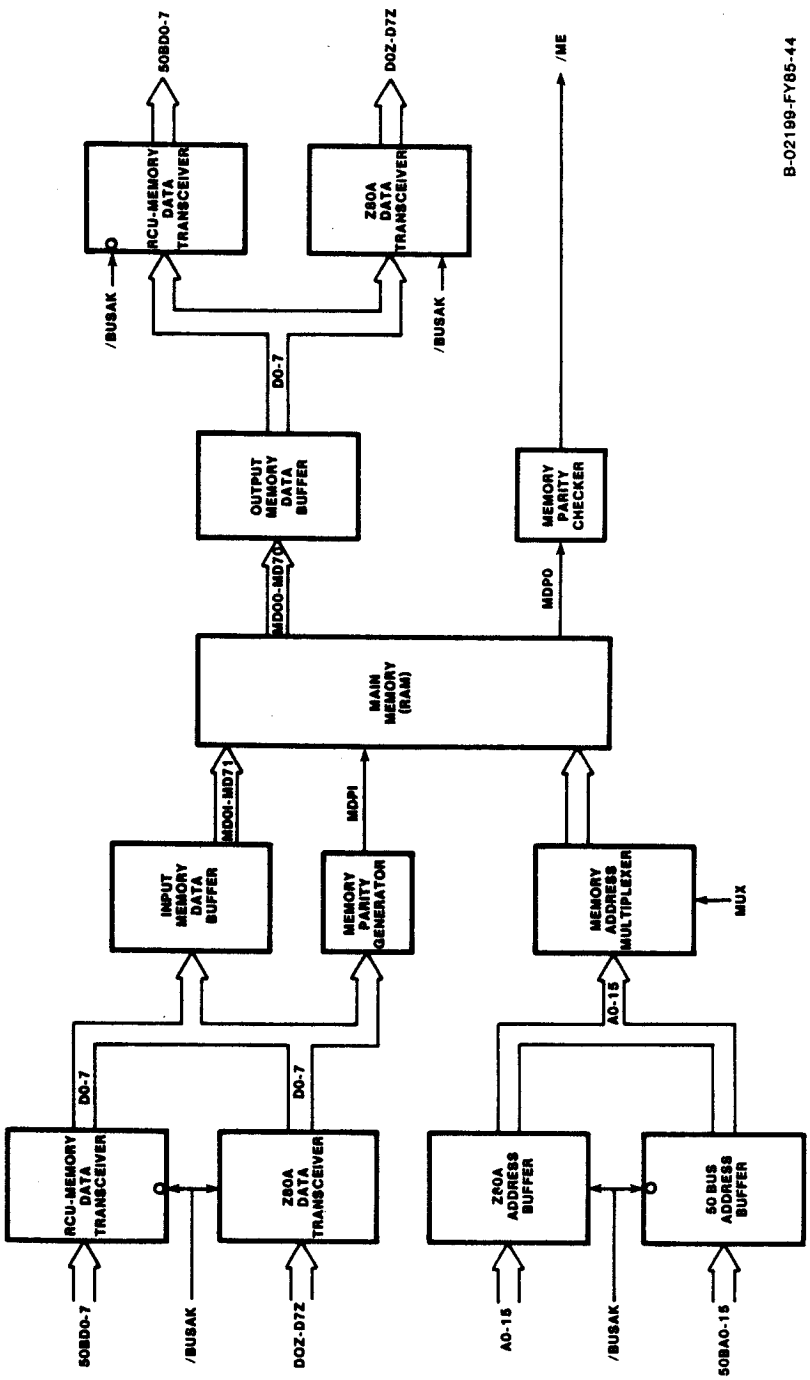
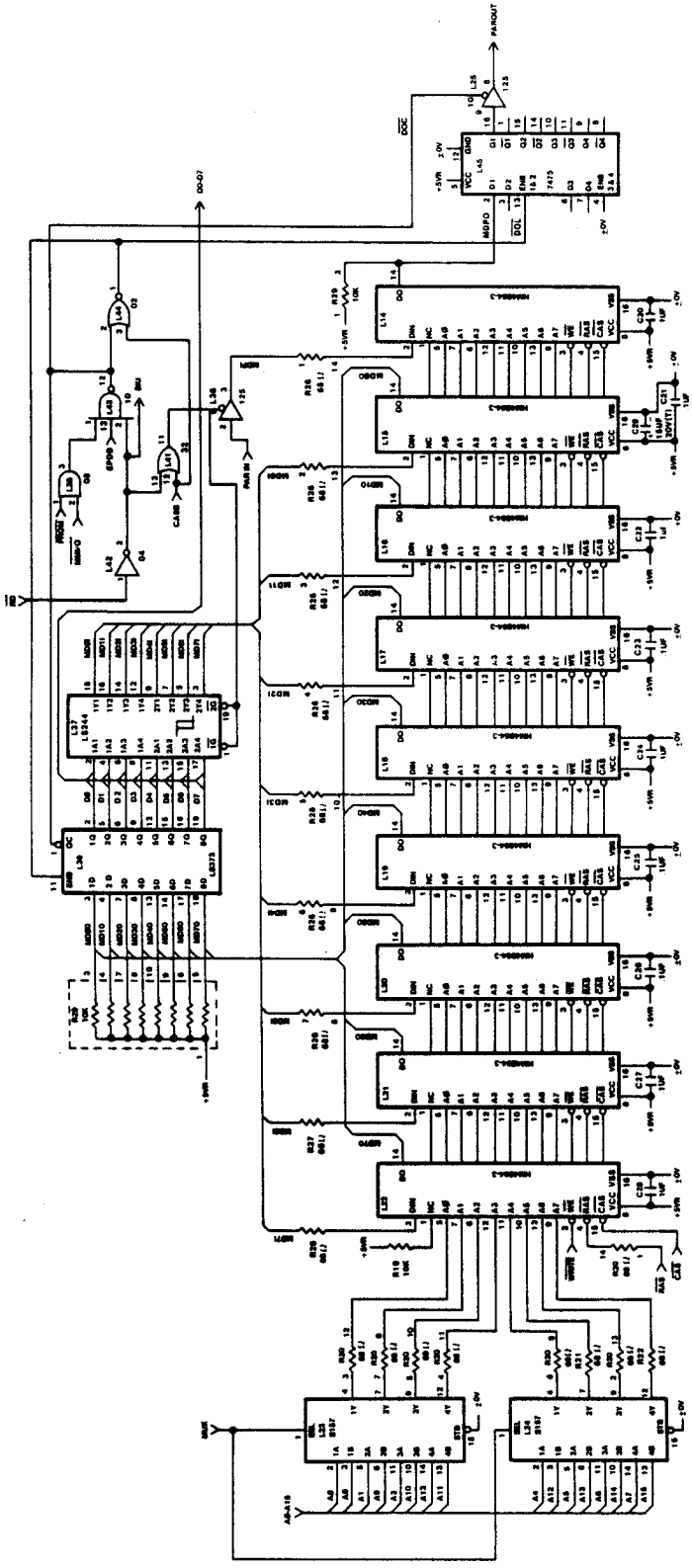


FIGURE 2.4-1
Memory Access Block Diagram



B-02199-FY85-60

FIGURE 2.4-2
Memory Access Circuitry

Direct Memory Access (DMA) occurs under RCU control via the D0-7 Data Bus and the A0-15 Address Bus. The RCU initially moves data between the 50BD Bus and the RCU's data buffer. Upon receipt of the proper enabling and direction control signals, RCU-Memory Data Transceiver (L89 (2I10)) moves data between the 50BD Bus and the D0-7 Bus. The RCU sends addresses for read and write operations to the A0-15 Address Bus via the 50BUS Address Bus and Address Buffers L129 and L144. (2I/J13)

When performing a DMA transfer, the RCU-Memory Operation Enabling Flipflop (L127 (2K10)) issues a signal from pin 6 that enables Address Buffers L129 and L144 and Data Transceiver L89 to move data between the RCU and memory via the 50BUS. BUSAK is clocked through L127 by the Phi-Z (8-MHz) clock to generate the &50B BUSAK (50BUS Bus Acknowledge) signal from pin 6. BUSAK is active whenever the RCU has Z80A bus control. &50B BUSAK asserts the enabling pins of the address buffers and data transceiver.

The direction of data flow through RCU-Memory Data Transceiver L89 is controlled by gating the 50BR/W (50BUS Read/Write) signal through L141 (2H13) to create a synthetic &RD (simulated Z80 Read) signal. If the synthetic &RD signal is active, L89 passes data from the D0-7 Bus to the 50BD Bus as the RCU reads the memory.

In a Z80A or DMA memory access, data is buffered from the D0-7 Bus to the MD0I-MD7I (Memory Data Input) Bus by Input Memory Data Buffer L37 (1D9). Outgoing data is buffered from the MD0O-MD7O (Memory Data Output) Bus to the D0-7 Bus by Output Memory Data Latch L39 (1D10).

Upon receipt of a low enabling signal on pins 1 and 19, L37, the Input Memory Data Buffer, allows data to enter memory. L41 (1D8) generates the enabling signal for L37 from pin 11 when it receives inactive &RD and active &CASB (Buffered Column Address Strobe) signals on pins 13 and 12, respectively. RD is inactive during memory write operations, and &CASB is active near the end of memory access operations.

When the main memory is to be read, the Output Memory Data Latch L39 (1D10) receives an active Data Out Control (&DOC) signal on pin 1 and an active Data Out Load (&DOL) signal on pin 11. Gate L43 (1D7) generates the &DOC signal when all of the gate's inputs are high. Generally, L43 generates &DOC when PROM and MMI/O are not being accessed (inactive &PROM and inactive &MMI/O on pins 1 and 2 of L38), the read signal is active (active RD on L43 pin 2), and the processor Data Bus is enabled (active EPDB on L43 pin 13). The &DOC signal generated from L43 pin 12 asserts L44 pin 2 and then is gated with &CASB. If &CASB is active (as it should be at the end of a memory access cycle), L44 generates the &DOL signal. &DOL asserts pin 11 of the Output Memory Data Latch (L39) to send the data from memory to the D0-7 Data Bus. Upon receipt of &DOL and &DOC, the transparent Memory Parity Bit Buffer (L45 (1B6)) creates the PAROUT (Parity Out) signal from the Memory Data Parity Out (MDPO) signal.

2.4.2 Memory Parity Generator/Checker

In Z80A-controlled read and write operations, the Parity Generator/Checker (L27 (1E4)) and its associated circuitry generate and check data parity (see FIGURE 2.4-3). L27 also generates a parity bit during RCU-controlled write operations. However, since the 50BUS does not have the capacity to carry a parity bit, the RCU does not check parity during read operations. The parity bit generated during RCU-controlled write operations is checked when the Z80A reads RCU-generated data.

During memory write operations, the Parity Generator/Checker establishes even parity for RCU or Z80A data entering on the D0-7 Data Bus. L27 issues the even parity bit from pin 5 to assert L26 pin 5 (1C2). Normally, the even parity bit is gated through L26, since the signal on L26 pin 4 is low (pin 4 is high only while running diagnostics). The even parity bit from L26 pin 6 is gated through L46 to create the PARIN (Parity In) signal. PARIN is gated through L36 (1C7) to create the MDIP (Memory Data In Parity) signal that enters RAM via L14 (1B7) pin 2.

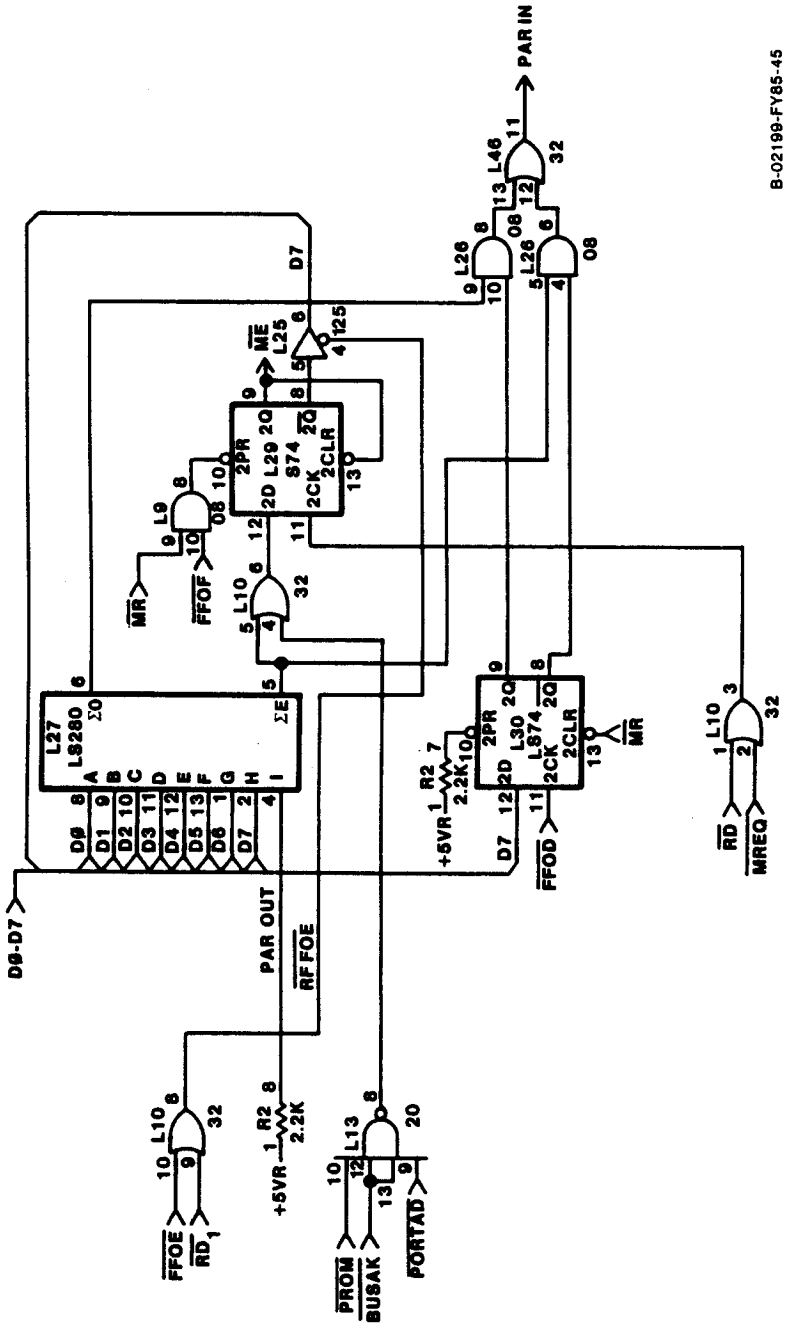


FIGURE 2.4-3
Parity Generator/Checker Logic

L27 also checks data parity in Z80A-controlled memory read operations. MDPO, the parity bit from memory, is issued from L14 pin 14 and used by Parity Buffer L45 to create the PAROUT signal. PAROUT along with data on the D0-7 Bus asserts the inputs of the Parity Generator/Checker (L27). If L27 detects odd parity (ie, an error has occurred), it issues a low signal from pin 5 that drives low pin 12, (via L10, see next paragraph below) of the Memory Parity Error Flipflop (L29). The trailing edge of the &RD signal clocks the low signal on L29 pin 12 through L29 to create the Memory Error (&ME) signal on pin 9. &ME asserts the Z80A to generate a non-maskable interrupt.

Parity can be checked only when the Z80A reads data from memory. Parity is not checked if &PROM (PROM operation), &BUSAK (RCU-controlled DMA operation), or &PORTAD (MMI/O operation) prevents L29 from checking parity bits. When asserted by any of these signals, L13 generates a high signal from pin 8 that prevents generation of the &ME signal by holding L29 pin 12 high.

By issuing the &FF0E command and reading the D7 bit, software can determine whether an NMI was caused by a memory error or the Restart Switch (SW2). &FF0E from L80 (1J9) pin 14 is gated with the &RD signal to create the &RFF0E signal on L10 (1E5) pin 8. &RFF0E asserts L25 pin 4, which allows software to read the ME signal via the D7 bit to determine if a memory error caused the NMI. If ME is inactive, the Restart Switch caused the interrupt; if it is active, a memory error caused the NMI.

Diagnostic routines test the Parity Generator/Checker by issuing the &FF0D command with D7 = 1. In response to &FF0D, L30 (gate 2Q (1D4)) generates signals that cause the gating logic of L26 and L46 to issue an odd PARIN signal, establishing the odd parity bit in memory. As data is retrieved from memory, L27 checks for even parity and detects odd parity. (L27 always checks for even parity.) L29 then generates the Memory Error (&ME) signal.

2.4.3 Memory Refresh

Memory Refresh of the RMU dynamic RAM chips must be completed every 2-4 ms, depending on RAM type. To begin the memory refresh process, the Z80A activates the Z80A Refresh Control (&RFSH) signal at the end of an op-code fetch cycle. At the same time, the Z80A presents to memory the row address of the memory space to be refreshed. (See FIGURE 2.4-4.) The Z80A can provide a 7-bit refresh address, yielding a total of 128 row addresses for refresh. Some of the RMU's 64k-byte RAMs require 256-row address refresh capability. This capability is produced by toggling and multiplexing a synthetic Refresh A7 bit into the A7R bit of the Z80A Address Bus.

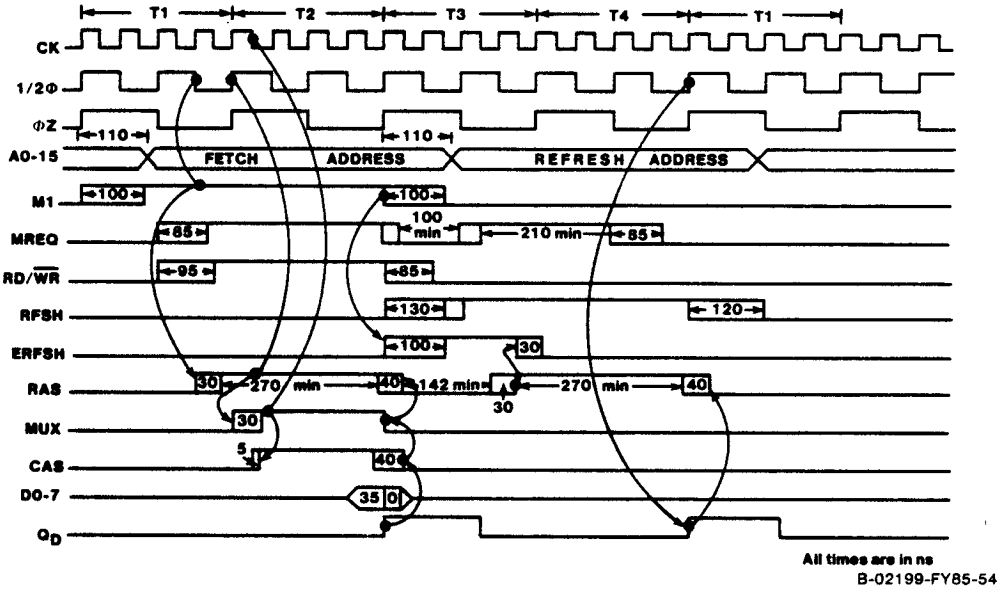


FIGURE 2.4-4
Op-Code Fetch / Memory Refresh Timing Diagram

Z80A refresh memory request logic is centers around the Refresh Request Flipflop (L35 (3J12)), which generates the Early Refresh (&ERFSH) signal. L35 produces &ERFSH at the end of each &M1 op-code fetch cycle as the rising edge of &M1 clocks L35 pin 3. The signal ERFSH from pin 5 asserts the RAS Generating Flipflop (L54 (3K10)) via L51 to begin the RAS generation cycle for refresh (see Section 2.4.4). &ERFSH from pin 6 travels to the L52 (3I11) Refresh A7 Bit Control Flipflop to cause it to select the synthetic Refresh A7 bit needed to perform a RAS-only refresh operation. L35 is cleared when the &RAS signal asserts pin 1.

The Refresh A7 Bit Control Flipflop L52, is preset to select the synthetic Refresh A7 bit during refresh by the active &ERFSH signal. The synthetic Refresh A7 bit is produced by L69 (3I13) and latched by the synthetic Refresh A7 Bit Latch L40 (3I12) during a row address refresh. Active &MREQ and &RFSH signals assert L69 (via L71) to clock the A6 bit through to L40.

In a 256-row refresh operation, the Z80A issues A6 low for the first 128-row refresh and high for the second 128-row refresh. In a 256-row refresh, the high signal from L69 (generated as a result of the high A6 signal) clocks L40 to generate the high A7R bit needed for the second 128-row refresh. Both A7R and A6 are low for the first 128-row refresh and high for the second 128-row refresh. The Refresh A7 Bit Control Flipflop is reset (to feed the A7' bit) at the end of each refresh operation by the rising trailing edge of the &RFSH signal that clocks pin 3.

2.4.4 RAS/CAS Signal Generator

Row Address Strobe (RAS) and Column Address Strobe (CAS) signals strobe data to and from the memory array. (FIGURE 2.4-5 shows the RAS/CAS and WRITE generating logic.) The memory address must be present on the Memory Address Bus prior to RAS or CAS strobe activation. RAS uses the low-order address byte to provide the row location of the data cell to be strobed, and CAS uses the high-order address byte to provide the column location of the data cell to be strobed.

The RAS/CAS generation cycle begins differently in memory data access operations and refresh operations. During a request for memory data transfer, the RAS/CAS cycle is initiated by either an active &M1 (Z80A in Fetch Cycle) signal on L34 (3K12) pin 4, or an active &MREQ (Memory Request) signal on L51 (3K14) pin 1 and an inactive RFSH (Z80A Refresh Control) signal on L51 pin 2. When the active &M1 signal or the active &MREQ and inactive &RFSH signals assert L34 and L51, output pin 6 of L34 generates the Enable Processor Data Bus (EPDB) signal. EPDB clocks L35 (3K12) (gate 2) to initiate the generation of memory data transfer request signals. The Memory Access Operation Pending Latch (L35, gate 2) issues a high signal from pin 9 that asserts pin 12 of L54 (3K10), the RAS Generating Flipflop.

During refresh operations, the Early Refresh (ERFSH) signal is generated at the end of all op-code fetch cycles (ie, when &M1 is active) to begin the RAS-only cycle. ERFSH from L35 pin 5 asserts L54 via L51 to initiate the RAS-generating cycle.

RAS/CAS generation during refresh or memory access begins with a high signal asserting pin 12 of L54, the RAS Generating Flipflop. The &1/2Phi (8-MHz) signal clocks L54's 2Q output to begin the generation of synchronized RAS signals. The &RAS signal from L54 pin 8 proceeds to memory to provide the row address strobe, and RAS from pin 9 travels to the RAS/CAS Timing Shift Register (L53 (3I8)) to begin the RAS/CAS timing chain. RAS from pin 9 also asserts L38 (3K9) pin 10 to begin the MUX-CAS cycle. An inactive &RFSH signal on pin 9 of L38 indicates that the current operation is not a refresh operation. The combination of active RAS on L38 pin 10 and inactive &RFSH on L38 pin 9 causes pin 8 to go high. This high signal asserts pin 2 of MUX Flipflop L50 (3J8) to generate MUX from pin 5 when the 1/2Phi clock signal asserts pin 3.

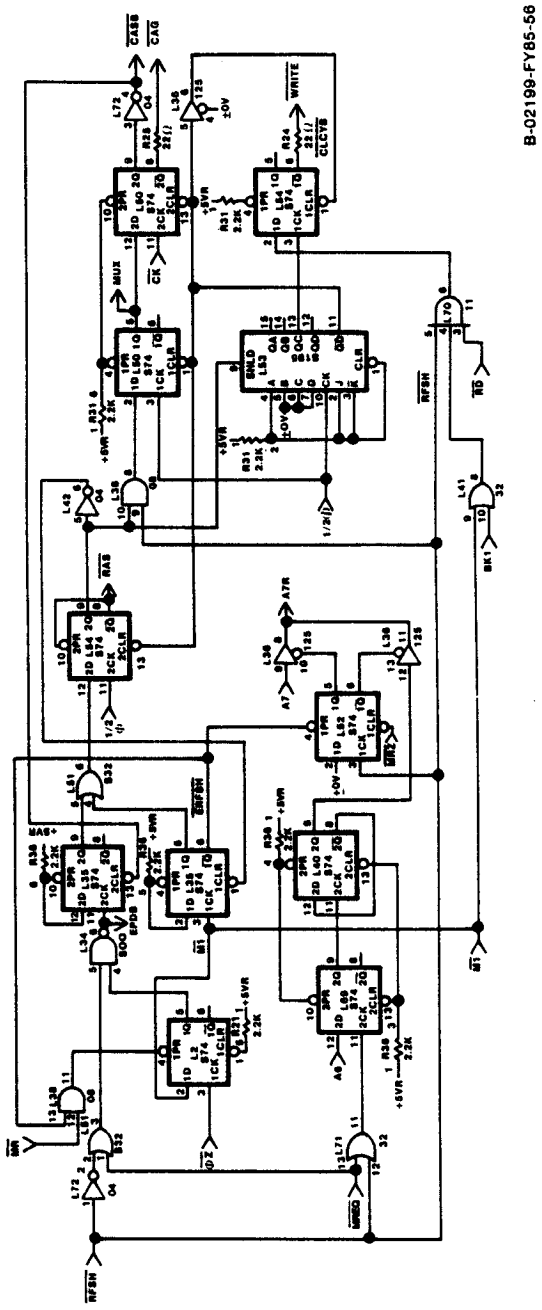


FIGURE 2.4-5
RAS/CAS and WRITE Generating Logic

MUX asserts the Memory Address Multiplexer (L23 and L24 (1A-C14)) to switch to the high-order address containing the column address. MUX also asserts pin 12 of CAS Flipflop L50 to generate CAS signals upon receipt of the &CK 16-MHz clock. &CAS from pin 8 proceeds to memory to provide the Column Address Strobe; it also indicates that the end of the memory access cycle is near. &CASB from L50 pin 9 clears the L35 Operation Pending Flipflop and aids in memory read/write control.

2.4.5 RAS/CAS Timing

RAS/CAS timing logic generates the timing sequence (shown in FIGURE 2.4-6) for memory access operations. The RAS/CAS Timing Shift Register (L53) is preset to 01H. When the RAS signal arrives on pin 9 of L53, it places the Shift Register into the shift mode of operation. The 1/2Phi clock signal on pin 10 of L53 shifts the bit through the register upon the receipt of each clock pulse. After two clock pulses, the QC output generates a high signal that clocks Write Flipflop L54 to generate the &WRITE signal. The &WRITE signal will only be activated if L70 (3H8) has all highs on its inputs, indicating a write operation. Upon the arrival of the third clock pulse at the end of the memory access cycle, the &QD output of L53 goes high on pin 11. The &Qd signal clears the RAS/CAS signal generation logic directly, and then clears the write logic via L36 and the &CLCYB signal.

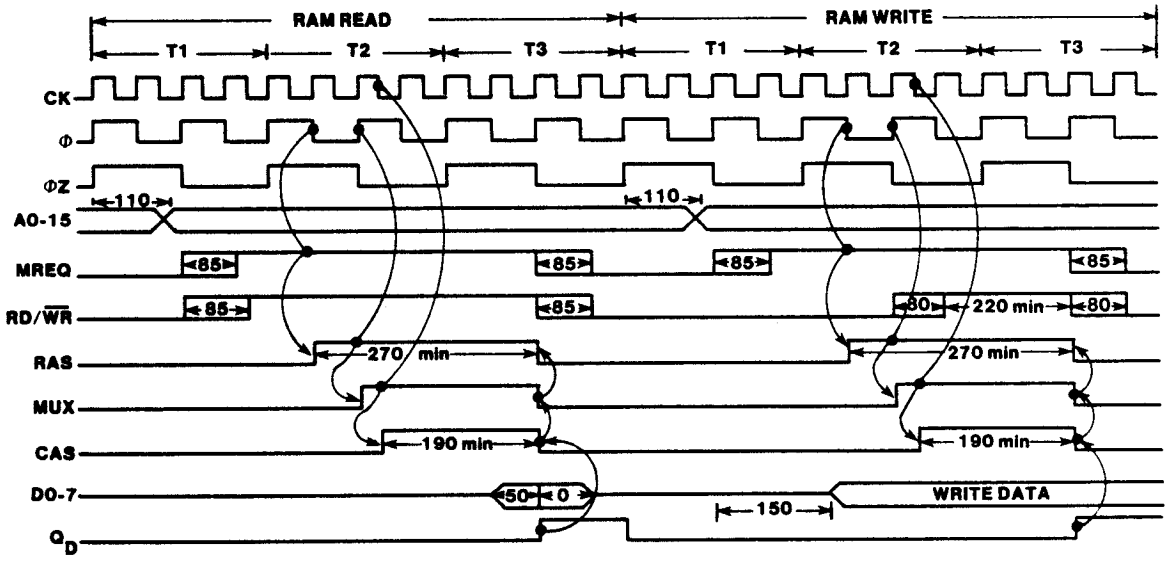


FIGURE 2.4-6
Memory Read Write Timing

2.4.6 Read/Write Signal Generator

During read and write operations, the Read/Write Signal Generator (L54 (3I7)) produces an active or inactive &WRITE signal on pin 6. The &WRITE signal from L54 is low if a write operation is required, and high if a read operation is required. When clocked by the Qc bit from the RAS/CAS Timing Shift Register, the Read/Write Flipflop samples its pin 2 input. If pin 2 is high, L54 generates an active &WRITE signal, and if pin 2 is low, L54 generates an inactive &WRITE signal.

Read/Write signal generation logic monitors the &M1, &RFSH, and &RD (respectively, Z80A in Fetch Cycle, Z80A Refresh Control, and Z80A or 8X305 Memory Read) signals via L54 pin 2 to detect read or write operations. When the inputs of L70 are high, a write operation is pending, and a signal from the output of L70 asserts L54 pin 2. &M1, &RFSH, and &RD are normally inactive during write operations; these signals, therefore, cause the output of L70 to go high to generate the WRITE signal from L54. &M1 and RD are gated into L41 to prevent L54 from generating WRITE during interrupt acknowledge operations when &M1 goes active.

2.4.7 Programmable Read Only Memory

L47 (1H6), a 2732A-2 PROM, contains 4k bytes of power-up (ie, IPL) and diagnostic programs that are addressed by bits A0-11. (FIGURE 2.4-7 diagrams the PROM Access Logic.) PROM-resident programs overlay the lower 4k bytes (0000-0FFFH) of RAM. PROM is enabled to overlay RAM when pins 9 and 10 of L7 (1G6) both are held high. L7 pin 9 normally is held high by a signal from the PROM Diagnostic Control Flipflop (L30 (1E5), gate 1Q). L7 pin 10 is held high by low address bits A12-15 driving the output of L64 (1G6) high. This combination of high signals on the inputs of L7 generates the low enabling signal from pin 8 that asserts the PROM's command enable and output enable pins via L46 (1G6). L46 monitors the &M1 and &MREQ signals (from L9 (1F6)) on its pin 4 input to ensure that either one or both signals are active during PROM access.

Data from the enabled PROM is placed on the D0-7 Bus and then buffered into the D0-7 Data Bus via Data Buffer L48 (1G5). L48's output is enabled when the &RD signal (from L96 (1E12)) and the low PROM enabling signal (from L7) assert L46 pins 1 and 2 to generate the low enabling signal from pin 3. The low signal from L46 pin 3 enables data output from PROM by driving pins 1 and 19 of L48 low.

To make more RAM space available as needed, diagnostic and operating system programs can retain control of the lower 4k bytes of RAM and, therefore, prevent PROM from overlaying the 0000-0FFF RAM space. Applying the &FF0E signal, via L10, to pin 3 of L30 (gate 1Q) with D7 = 0 on pin 2 causes L30 to generate a low signal from pin 5. This low signal asserts pin 9 of L7 to prevent the generation of the PROM enabling signal and, therefore, disabling PROM from the lower 4k bytes of RAM. When PROM is disabled, the lower 4k bytes of RAM are available for diagnostic testing.

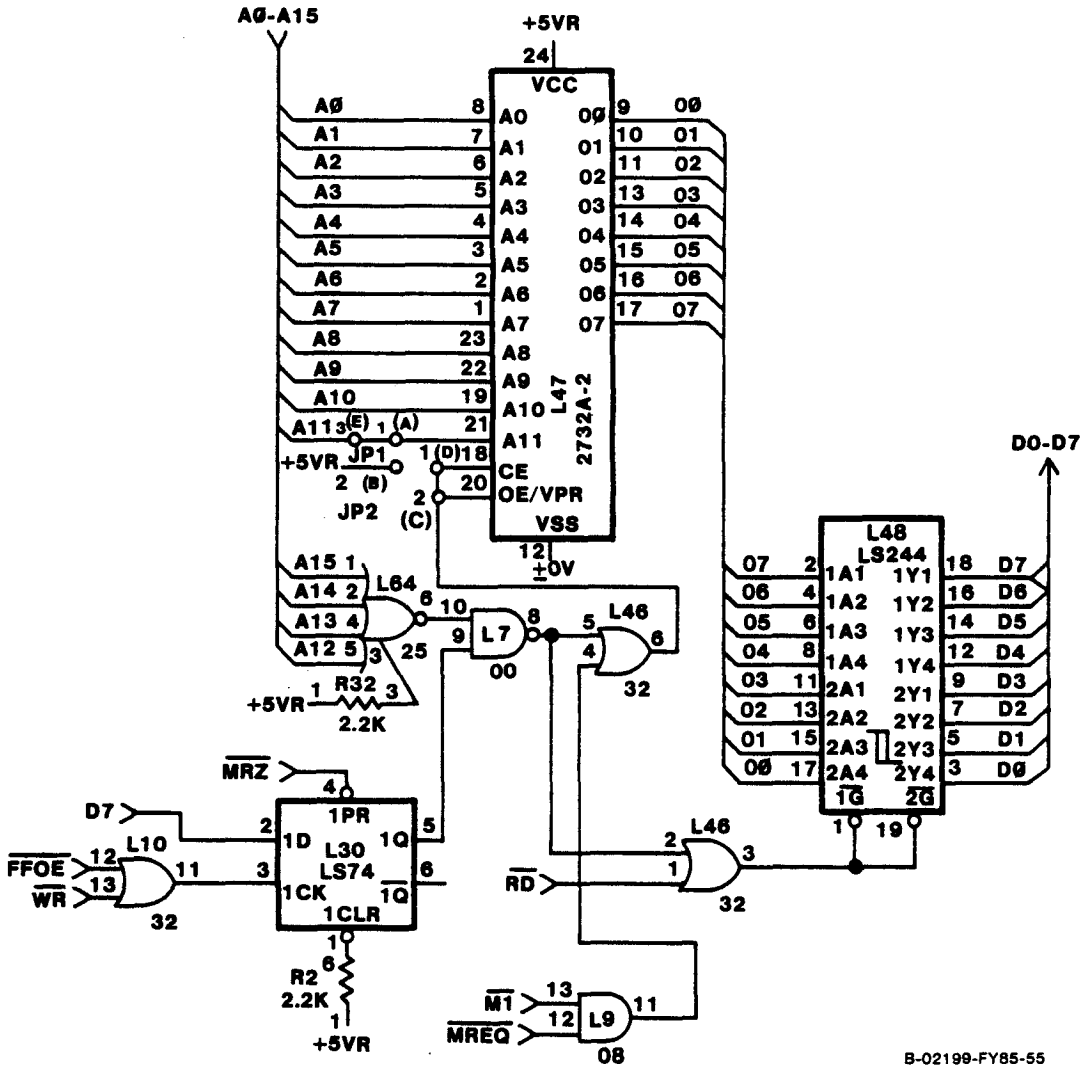


FIGURE 2.4-7
Prom Access Logic

2.5. FLOPPY DISK CONTROLLER

The Resource Management Unit's Floppy Disk Controller can execute ten different commands, each is initiated by a multibyte transfer from the Z80A processor. Command execution can result in a multibyte transfer back to the Z80A processor. Because of this multibyte interchange of information between the Floppy Disk Controller and the Z80A, it is convenient to consider each command as consisting of three phases:

1. Command phase: The Floppy Disk Controller (FDC, L101) receives all the information it needs to perform a particular operation.

2. Execution phase: The FDC performs the operation as instructed by the command.

3. Result phase: After completing the operation, the FDC makes status information available.

The FDC, when used in an OIS 50 system, can execute ten of the 15 available FDC commands: Read Data, Read ID, Read a Track, Specify, Write Data, Format a Track, Seek, Recalibrate, Sense Interrupt Status, and Sense Drive Status. Each of these commands require a multiple byte transfer of commands to specify the operation to be performed. The FDC receives and decodes the command in the command phase and executes it in the execution phase. At the end of the execution phase, the FDC issues an interrupt to the Z80A processor. The FDC must then complete the result phase, by reading all of the FDC internal status registers before the FDC can accept new commands.

2.5.1 Read/Write Operation

During the command phase of Floppy Disk Drive (FDD) operation, data is sent, via the D0-7 Bus, from the Z80A to the FDC Data Transceiver (L87 (2D7)). (FIGURE 2.5-1 shows FDC data access routes, and FIGURE 2.5-2 and 2.5-3 show the FDC access and data path logic.) The command is sent through the Data Transceiver to the Floppy Disk Controller Data (FDCD) Bus and into the FDC. The FDC interprets the command and enters the execution phase to perform the operation.

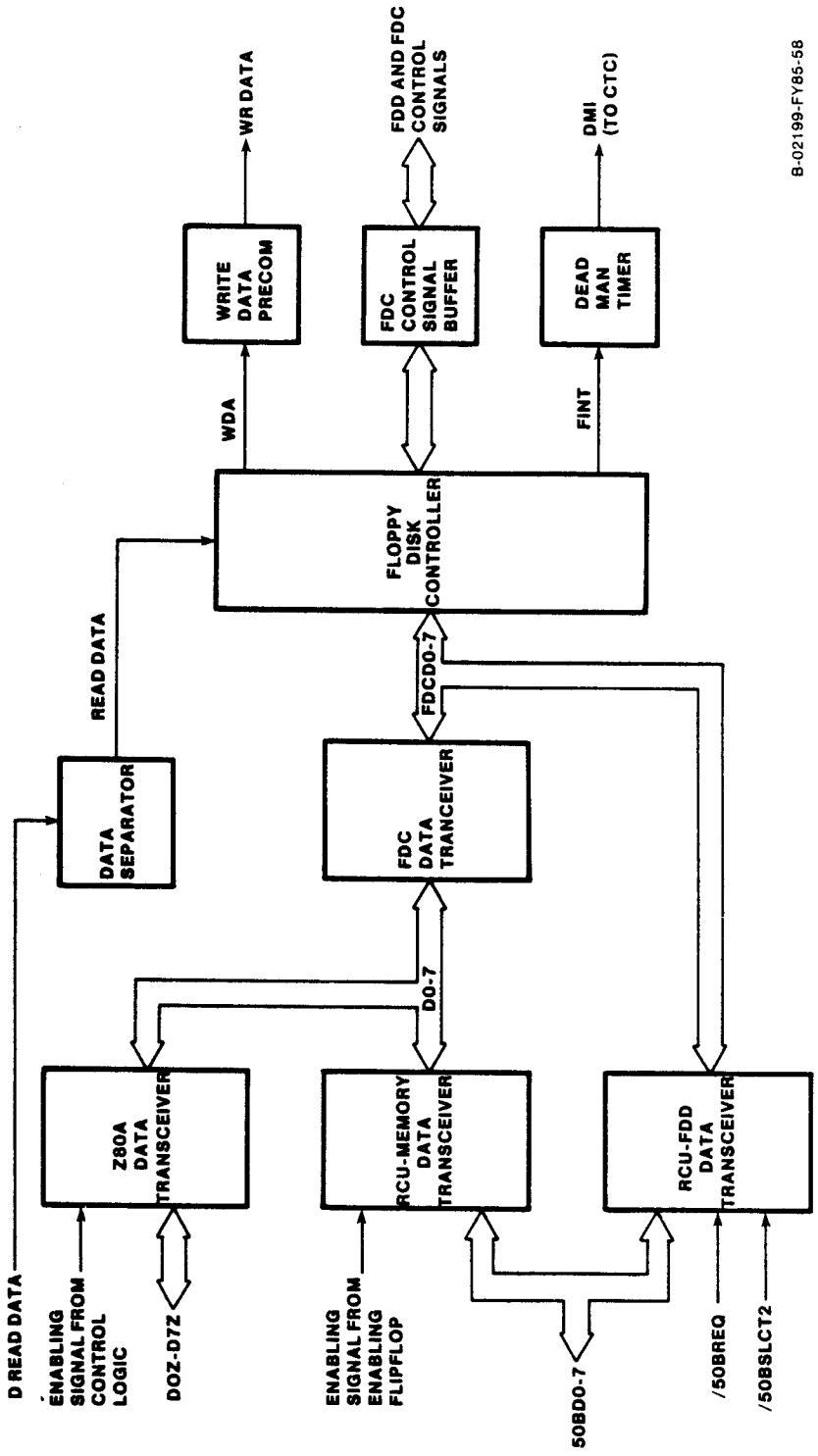


FIGURE 2.5-1
FDC Access Block Diagram

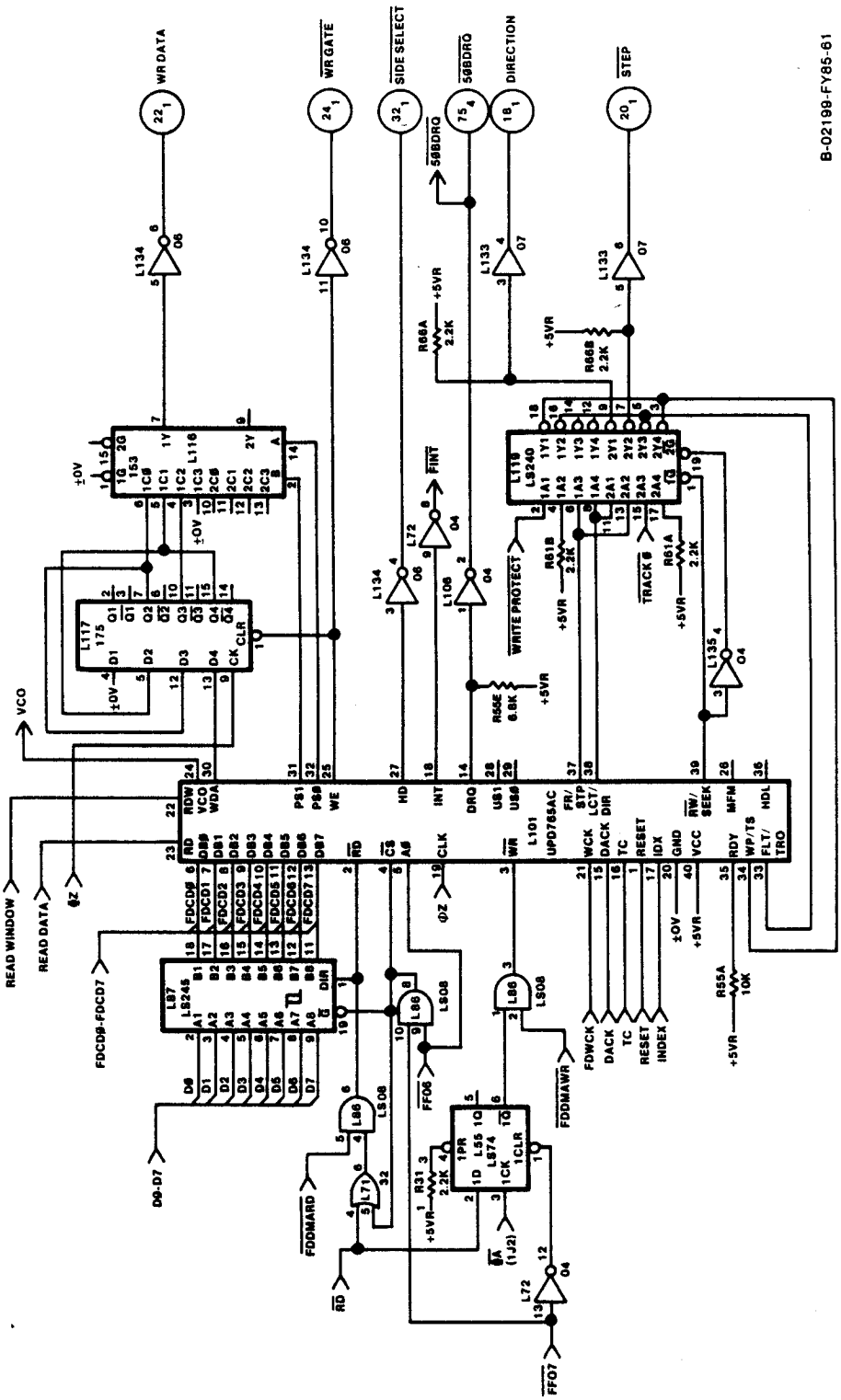


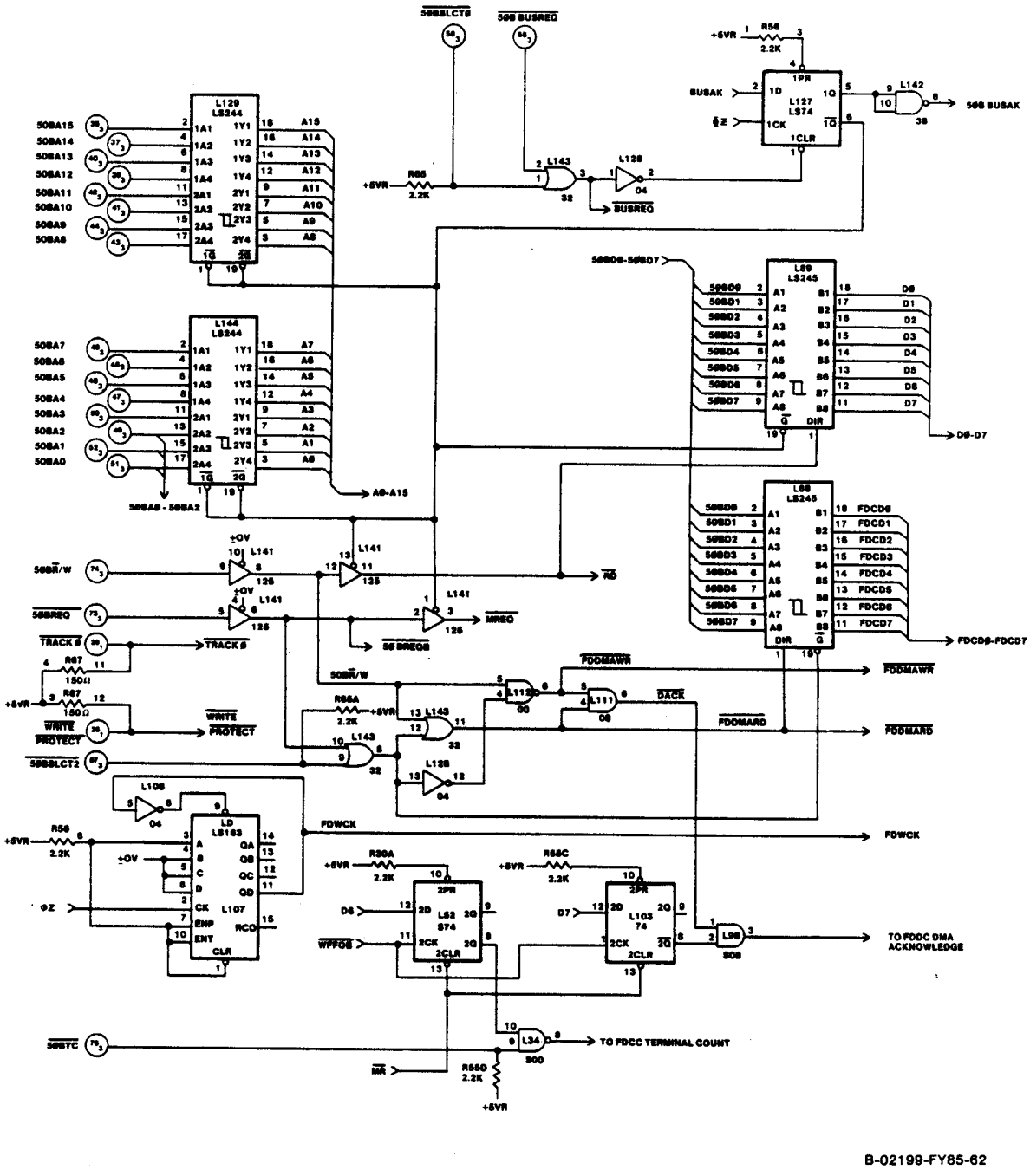
FIGURE 2.5-2
FDC Access Logic

During FDD read operations, control signals allow data to be read from the Floppy Disk Drive. The FDD Controller receives this data on pin 23, assembles it into a parallel format, and sends it, via the FDCD Bus, to the RCU-FDC Data Transceiver (L88 (2H10)). Enabling and direction control signals allow the data to pass through L88 and onto the 50BD (50 Bus Data) Bus. The RCU board then reads the data from the 50BD Bus into its data buffer. The FDD-originated data is written from the RCU back onto the 50BD Bus, and, simultaneously, the data's memory address is written onto the 50Bus Address (50BA) Bus. When the necessary enabling and direction control signals are present, the RCU-Memory Data Transceiver (L89 (2I10)) reads the data from the 50BD Bus onto the D0-7 Bus. At the same time, the RCU-Memory Address Buffers (L129 and L144 (2I-J13)) place the data address onto the A0-15 Bus. The data is then stored in memory at the address provided on the A0-15 Bus. (Section 2.5.2 explains the enabling and control signals used in this operation.)

During FDD write operations, the data to be written to the Floppy Disk Drive is retrieved from memory under RCU control via the D0-7 Data Bus. The RCU provides the data address via the 50BUS Address Bus and Address Buffers L129 and L144. Upon receipt of the proper enabling and direction control signals, the RCU-Memory Data Transceiver (L89) places the data on the 50BD Bus. The RCU reads the data from the 50BD Bus into its data buffer. When the RCU-FDC Data Transceiver (L88) is properly enabled, the data is written from the RCU onto the 50BD Bus and passed through L88 onto the FDCD0-7 Bus. The FDC reads the data from the FDCD Bus, serializes it for transmission, and sends the serial data to the Floppy Disk Drive from pin 30. At the same time, the FDC issues the appropriate control signals from other pins.

2.5.2 Read/Write Enabling

The RCU generates the &50BRW signal to place the DMA operation in either the read or write direction (see FIGURE 2.5-3). During RCU read operations, &&50BR/W is low; the low &&50BR/W signal is gated through L143 (2G12), with &50BSLCT2 and &50BREQ to create the active FDD DMA Read (&FDDMARD) signal. During RCU write operations, &&50BR/W is high; the high &&50BR/W signal asserts L112 (2G12) pin 5 to generate an active FDD DMA Write (&FDDMAWR) signal from pin 6. &FDDMARD and &FDDMAWR assert the appropriate buffers and control logic to control read and write operations.



B-02199-FY85-62

FIGURE 2.5-3
FDC Data Path Logic

The chip select signal, which is generated by L86 (2C7) pin 8 as a result of the Read FDC Status (&FF06) or Read/Write FDD Data (&FF07) command asserting pins 9 and 10, enables FDC Data Transceiver L87 (2D7). The &RD and &FDDMARD signals control the direction of data flow through L87. If &FDDMARD is active on L86 pin 5 or an active &RD signal is gated onto L86 pin 4 (via L71), L86 generates a low signal from pin 6 that places the transceiver in the read direction. If &RD or &FDDMARD is inactive (high) and the FDC is selected, L87 is placed in the write direction.

L127 (2K10), the RCU-Memory Operation Enabling Flipflop, issues a signal from pin 6 that enables Address Buffers L129 and L144 and Data Transceiver L89 to move data (via the 50 Bus) between the RCU and memory. The BUSAK signal is clocked through L127 by the Phi-Z clock to generate the &50B BUSAK signal from pin 5. (BUSAK is active whenever the RCU has Z80A Bus Control.) &50B BUSAK asserts the enabling pins of the address buffers and data transceiver.

To control the direction of data flow through the RCU-Memory Data Transceiver (L89), the &&50BR/W signal is gated through L141 to create a synthetic &RD (simulated Z80 Read) signal. If the synthetic &RD signal is active, L89 passes data from the D0-7 Bus to the 50BD Bus when memory is read by the RCU.

Gating the RCU-generated &50BREQ (50BUS Byte Request) signal on pin 10 with the &50BSLCT2 (FDD Bus Select) signal on pin 9 creates a low signal from L143 pin 8. This low signal enables L88, the RCU-FDC Data Transceiver. &50BREQ is active whenever the RCU reads or writes a byte of data to the disk, and &50BSLCT2 is active during all FDD operations. The &50BREQ signal from the RCU is interpreted on the RMU board, via L141 (2H13), to create the synthetic &MREQ (Z80A Memory Request) signal.

The direction of data flow through the RCU-FDC Data Transceiver (L88) is controlled by the Floppy Disk Drive DMA Read (&FDDMARD) signal asserting L88 pin 1. When &FDDMARD is active on pin 1, data passes from the FDCD Bus to the 50BD Bus as data is read from the FDD. An inactive &FDDMARD signal places L88 in the opposite (ie, write to the FDD) direction. &FDDMARD is created from L143 pin 11 by the &&50BR/W (50 Bus Read/Write) signal being gated through pin 13 to pin 11. L143 pin 12 monitors the active &50BSLCT2 and &50BREQ signals (via L143 pins 9 and 10) to ensure that the FDD is selected and the RCU is prepared to read or write a byte of data.

2.5.3 Control Signal Generator

The Read-Write/Seek (&&RW/SEEK) signal on pin 39 of the FDC determines the flow of signals through L119 (2B4), the FDC Control Signal Buffer (FIGURE 2.5-2). When the FDC performs a read or write operation, pin 39 is low to allow the 1Y1-1Y4 outputs of L119 to follow the inputs on pins 1A1-1A4. When the FDC performs seek operations, pin 39 is high to allow the 2Y1-2Y4 outputs to follow the inputs on pins 2A1-2A4.

During Floppy Disk Drive read or write operations, L101 pin 39, the FDC, produces a low Read/Write (&RW) signal that enables the 1Y outputs of Control Signal Buffer L119. These outputs generate the signals required for read or write operations to occur. L119 passes the &WRITE PROTECT and Fault (FLT) signals from the FDD to the FDD Controller. The &WRITE PROTECT signal defines, to the FDC, the status of the recording media (ie, write protected or not write protected). The signal from 1Y2 (pin 16) of L119 is held low to create an inactive FLT (Fault) signal. The FDC's FLT input is not used and, therefore, is held inactive during read or write operations.

During Floppy Disk Drive Seek operations, L101 pin 39 produces a high SEEK signal that enables the Control Signal Buffer's 2Y outputs to generate the signals needed to perform a seek operation. L119 passes the &STEP, DIRECTION, TRACK 0, and TWO-SIDED MEDIA signals. &STEP asserts the Floppy Disk Drive to move the head of the drive to another cylinder, and DIRECTION controls the direction in which the drive moves the head when the STEP signal is generated. TRACK 0 signals the FDC that the drive is at Track 0. The TWO-SIDED MEDIA signal is held active on pin 34 of the FDC (since this is the only medium used during seek operations).

The following FDC-generated control signals are not buffered through L119: Floppy Interrupt (FINT), 50BUS DMA Request (50BDRQ), SIDE SELECT, and Write Gate (WR GATE). When the FDC finishes command execution, the FDC (L101, pin 18) sends a Floppy Interrupt to the RMU. L101 pin 14 sends 50BDRQ to the RCU when a byte of data is ready to be transferred. SIDE SELECT is generated by pin 27 and sent to the FDD to select a disk surface to be used in the FDD operation, and WRITE GATE is generated from pin 25 to command the FDD to prepare for a write operation.

2.5.4 Write Data Precompensation

Write data precompensation circuitry (FIGURE 2.5-2) defines the timing sequence of the data pattern to be written onto the Floppy Disk Drive. Data can be written in one of three different timing sequences, early, nominal, or late, to prevent data errors from being created when the data is written. Writing data early means that each data bit is written 250 ns earlier then normally expected. Nominal data is written at the time that it would normally be written, and late data is written 250 ns after it would normally be written on the disk. Writing data at alternate times prevents data crowding and, therefore, prevents frequent data errors as data is read from near the center of the disk.

L117 (2E5), the Write Data Precompensation Sequencer, is enabled during FDD write operations by the WRITE GATE signal from FDC pin 25. When enabled, L117 receives data from the FDC via pin 13 and then transmits that data via pin 15. The data from pin 15 is fed back into pin 5 of L117 and then fed back again from the pin 7 output to the pin 12 input. This feedback cycle creates the 250-ns delay between each data bit as a result of the Phi-Z (4-MHz) clock asserting the clocking pin of L117. Early data is fed from L117 pin 15, nominal data from pin 7, and late data from pin 10.

L116 (2E4), the Write Data Precompensation Data Selector, chooses either early (input pin 5), nominal (input pin 6), or late (input pin 4) data depending on the PS1 and PS0 signals it receives on pins 2 and 14. The data, in the selected timing sequence, is transmitted to the Floppy Disk Drive as the WR DATA signal from L116 pin 7. Table 2.5-1 illustrates the timing sequences selected by the PS0 and PS1 signals from the FDC.

Table 2.5-1: WRITE DATA/PRECOMPENSATION SELECT SIGNALS

PS0	PS1	TIMING SEQUENCE
0	0	Nominal
0	1	Early
1	0	Late

2.5.5 Motor Control

On/off motor control circuitry protects against excessive disk wear if the drive motor is left running continuously (since the heads are loaded when the disk drive door is closed). To turn on the drive motor, the Z80A issues &WFF0B with D0 = 1. In response, Motor Control Flipflop L118 ((2C13) gate 1) issues the MOTOR ON signal to the disk drive. To turn off the drive motor, the Z80A issues &WFF0B with D0 = 0, and L118 responds with the inactive MOTOR ON signal. The FDD motor is shut off automatically under Z80A program control if the FDD is not accessed for 1 s.

The &FF0A MMI/O command asserts L55, the FDC Reset Flipflop, to generate a signal from pin 5 which asserts the reset pin of the NEC765 Floppy Disk Controller. Reset pulse width must be at least 10 us (see Section 2.5.9).

2.5.6 Terminal Count

For Z80A-Floppy Disk Drive DMA operations, Terminal Count and DMA Acknowledge handshaking signals are generated by flipflops L52 and L103, respectively (see FIGURE 2.5-3). The RCU board generates Terminal Count and DMA Acknowledge signals for 8X305-Floppy Disk Drive DMA operations.

During Z80A-Floppy Disk Drive DMA operations, Terminal Count Flipflop L52 provides the active Terminal Count handshaking signal. This signal is sent to the FDC during Z80A DMA data transfers either when all the data has been sent or when all the data has been received by the Z80A. L52 (2F12) generates a high Terminal Count signal from pin 8 upon receipt of the &WFF0B command with D6 = 1. This signal is gated through L34 (2E12) to generate a signal that asserts FDC pin 16. During 8X305-FDD DMA operations, the RCU board provides the Terminal Count signal to FDC pin 16 via the 50 Bus Terminal Count (&50BCT) signal on pin 9 of L34.

2.5.7 DMA Acknowledge

The DMA Acknowledge (&DACK) handshaking signal is used in all Floppy Disk Drive DMA transfers. The RCU returns this signal, on a byte-by-byte basis, in response to a DMA Request from the FDC. During normal DMA operations (8X305-Floppy Disk Drive), L111 (2G11) generates &DACK in response to the RCU-generated &50BREQ signal (as shown in FIGURE 2.5-3). L143 pins 9 and 10 monitor the &50BSLCT2 (50BUS Select Channel 2) and &50BREQ (50BUS Byte Request) signals. &50BSLCT2 is active throughout any FDD operation, and &50BREQ pulses each time a byte is transferred in a DMA operation. As &50BREQ is activated, it is gated through the L143 (2G13) gates into input pin 4 of L111. L111 then generates &DACK upon receipt of the gated &50BREQ signal (since L111 pin 5 is low as a result of the inverted &50BREQ signal asserting L112 pin 4).

During diagnostics the Z80A (rather than the RCU) can perform DMA operations. In this case, the necessary &DACK signal is generated on the RMU board by the Z80A DMA Acknowledge Flipflop (L103, pin 8 (2F11)) in response to the &WFF0B command with D7 = 1. &DACK from L103 pin 8 is gated through L98 to assert pin 15 of the Floppy Disk Controller.

2.5.8 Deadman Timer

Deadman timer logic prevents errors from causing both Floppy Disk Drive operation and Floppy Disk Controller operation to be frozen or "hung". The Z80A, after issuing a command to the FDC, sends the &FF0C signal to the deadman timer to begin a 540-ms timeout period. The deadman timer logic then monitors the FDC for the presence of the &FINT signal. (&FINT normally is sent to the Z80A from the FDC when command execution is completed.) If the active &FINT signal does not assert the deadman timer logic within 540 ms, the deadman timer logic issues a Deadman Interrupt (&DMI) signal to the Z80A. Also, the Z80A can read the status of the DMI signal via FDC Status Register bit D3 (&RFF0B).

After the FDC receives a command during any Floppy Disk Drive operation, L80 (1J9) issues &FF0C to pin 11 of the Deadman Timer 1-Shot (L100, gate 2 (2D12)). If L100 is not cleared by a low signal on pin 13 prior to the 540-ms timeout, it issues a signal that clocks L69 (2D11), the Deadman Timer Flipflop. L69, when clocked, issues the Deadman Interrupt (&DMI) signal from pin 6. &DMI asserts pin 12 of the CTC (via L13), and the CTC, in turn, issues an interrupt to the Z80A. Upon receiving the interrupt, the Z80A executes a routine to determine whether the Floppy Disk Drive or the deadman timer generated the interrupt. The Z80A then proceeds with other routines to correct the error situation or to retry the Floppy Disk command.

Three signals can clear the deadman timer logic to prevent the generation of the &DMI signal. The &FINT (Floppy Interrupt) signal goes active whenever the FDC completes an operation. &FINT asserts L70 (2D13) pin 13 to generate a low signal from pin 12 that clears the deadman timer logic. &MRFD (Master Reset Floppy Disk) also asserts L70 to clear the deadman timer logic. &RFF0B from L108 reads the FDC Status Registers and clears the deadman timer logic via L70.

2.5.9 Floppy Disk Controller Reset

Either the Z80A processor or the &MRFD (Master Reset Floppy Disk) signal can reset the Floppy Disk Controller. The Z80A resets the FDC by issuing &FF0A commands through L80, the Memory Mapped I/O Decoder. L80 (1J9) issues two &FF0A write commands to reset the FDC: the first &FF0A command turns on the Reset Flipflop and the second turns it off. (Reset pulse width must be at least 10 us.) &FF0A asserts pin 11 of the Reset Flipflop (L55 (2E14), gate 2Q) to generate a high signal from pin 9 that is gated through L71 (2E13) to reset the FDC. The active &MRFD signal resets the FDC by asserting pin 1 of the FDC via pin 9 of L71. (&MRFD is generated as a result of the &AUTO RESET signal.)

2.5.10 Floppy Disk Drive and Controller Status

The Z80A uses the &RFF0B command to read the status of the Floppy Disk Drive and Controller. &RFF0B asserts the clock pins of Status Registers L101A (2D9) and L105 (2C11) to clock the Status Byte onto the D0-7 Data Bus. Table 2.5-2 lists and defines the status signals, and FIGURE 2.5-4 illustrates the logic that generates the status signals.

Table 2.5-2: FLOPPY DISK DRIVE STATUS BYTE

BIT	SIGNAL	DEFINITION
D0	True File Ready	Generated by True File Ready 1-Shot (L100, gate 1). Indicates that Floppy Disk Drive is ready to perform an operation (ie, disk is loaded and spinning, FDD door is closed, and FDD is selected).
D1	Select Line	Generated by Floppy Disk Drive Select Flipflop (L118, gate 2). Indicates that Floppy Disk Drive is selected to perform an operation.
D2	Door Disturbed	Generated by Door Disturbed Flipflop (L120, gate 2). Indicates that door to Floppy Disk Drive is open.
D3	Deadman Timer	Generated by Deadman Timer Flipflop L69. Indicates that deadman timer has generated an interrupt.
D4	50BUS Data Request	Generated by Floppy Disk Controller (L101) when FDC makes a DMA request for data. Signal is of primary significance during diagnostic testing of FDC logic.
D5	Floppy Interrupt	Generated by Floppy Disk Controller. Indicates that received command has been executed. Signal is of primary significance during diagnostic testing of FDC logic.
D6	Not Used	
D7	Not Used	

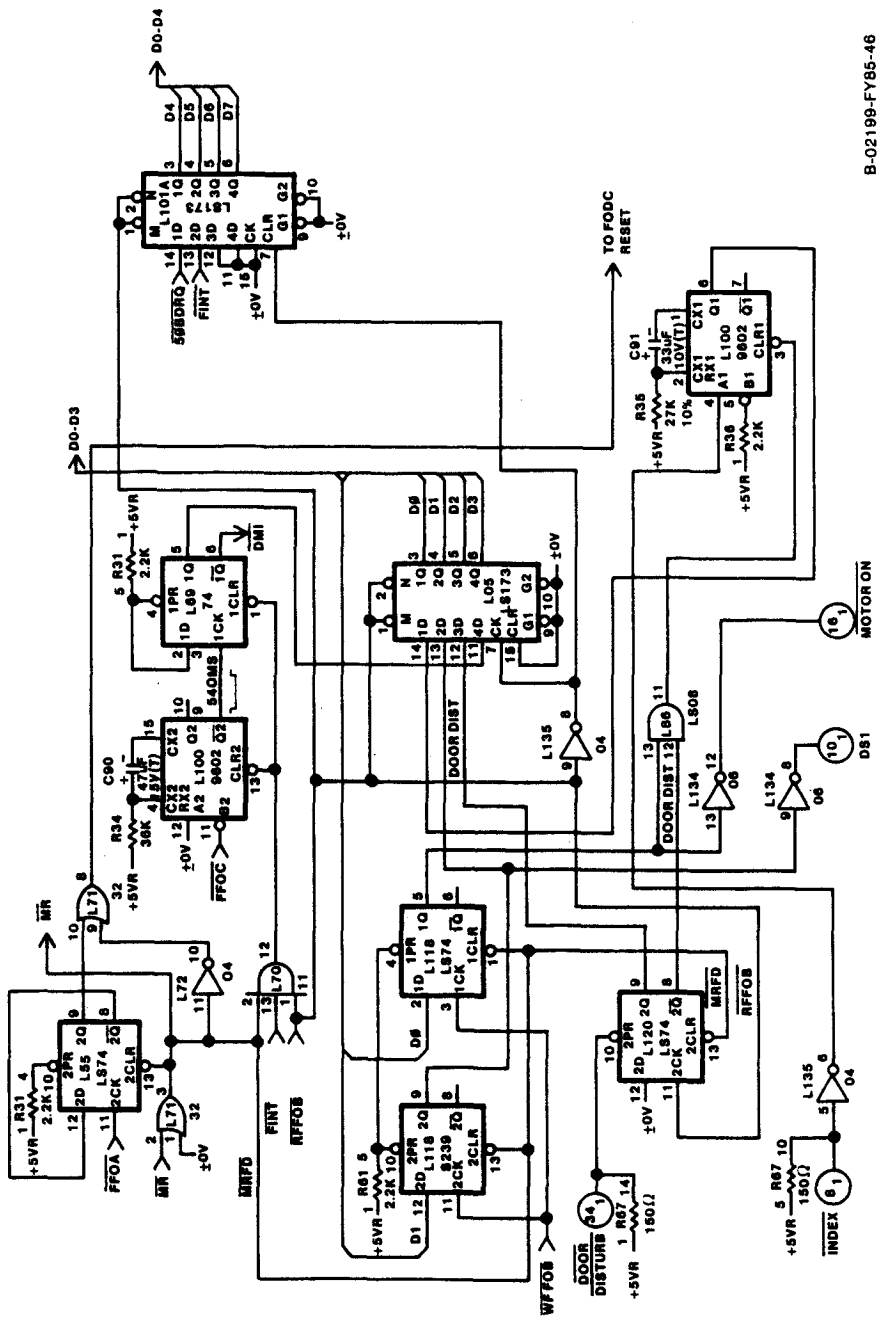


FIGURE 2.5-4
FDC Status Logic

L100 (2A10) (gate 1) generates the True File Ready status signal from pin 6 to indicate that the disk is loaded and spinning, the FDD door is closed, and the FDD is selected. The inactive &DOORDIST signal (door has not been disturbed) and the active MOTOR ON signal (motor is on) assert L86 to generate a high signal from pin 11 that asserts the clear pin of L100. L100 can then generate the True File Ready signal when it receives the INDEX signal from the FDD. The INDEX pulses from the FDD assert pin 4 of L100 when the disk is loaded and spinning. If either the MOTOR ON signal or the &DOORDIST signal on the inputs of L86 changes state, L100 is cleared and the True File Ready signal is deactivated.

The Floppy Disk Drive Select Flipflop (L118 (2C14), gate 2) responds to &WFF0B and D1 by issuing the Disk Select #1 (DS1) signal that controls FDD selection. The Z80A selects the Floppy Disk Drive for operation by issuing the &WFF0B with D1 = 1; &WFF0B with D0 = 0 de-selects the FDD.

L120 (2A13), the Door Disturbed Flipflop, latches the &DOOR DISTURB signal from the FDD to inform the Z80A that the drive door has been opened (even if the door is closed at the time of the Status Read). The Z80A issues the &RFF0B command to read the FDC Status Register. If the door is closed, &RFF0B clears the Door Disturbed Flipflop by clocking a zero through the flipflop.

When a diagnostic routine tests the FDC logic, the Z80A must verify the generation of &50BDREQ (50BUS DMA Request) and &FINT (Floppy Interrupt). &50BDRQ is generated by L101, the Floppy Disk Controller, when L101 makes a DMA request for data. &FINT is generated by the Floppy Disk Controller to indicate that execution of the received command has been completed. Status Register L101A provides &50BDRQ and &FINT to the Z80A via data bits D4 and D5.

2.5.11 Data Recovery

FDD data recovery logic accepts and synchronizes the data signal (D READ DATA) from the Floppy Disk Drive and converts this signal into a form (READ DATA) that the FDC can easily use. (FIGURE 2.5-5 diagrams the data recovery operation.) The data recovery logic recognizes data bits from the FDD only as phase/frequency transitions, which then are converted into a standard digital data stream. Voltage Regulator VR1 provides an isolated 5 V to the data recovery logic (since the recovery logic can operate correctly only in an environment with a minimal amount of electronic noise).

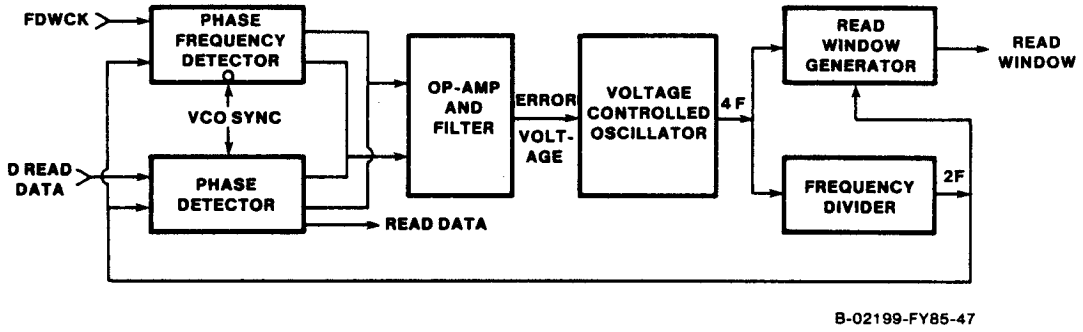


FIGURE 2.5-5
Data Recovery Block Diagram

When the FDD data recovery logic shown in FIGURE 2.5-6 is not reading data, it is locked into use as a free-running frequency generator to hold the recovery logic at the center frequency of operation. The phase locked loop portion of the recovery logic generates a free-running center frequency by locking the phase and frequency of the FDD Write Clock (FDWCK) signal and the VCO-generated feedback signal into the same phase and frequency. (&FDWCK is a 1-MHz signal generated by Floppy Disk Timing Generator L107.)

Phase/Frequency Detector L85 (2J6) detects FDWCK on pin 1 and compares FDWCK's phase and frequency with the phase and frequency of the signal generated by the Voltage Controlled Oscillator (VCO, L83 (2J2)). If the signals' phases and/or frequencies differ, L85 produces error signals on pins 2 and 13. The two L99 gates, sum these signals and send them to Op Amp L84, which creates an error voltage output relative to the signals it receives. The error voltage issued from L84 asserts pin 2 of VCO L83. In response, L83 generates a frequency (from pin 7) that is dependent on the error voltage applied to pin 2. The VCO-generated frequency asserts L97, which then halves the frequency and issues it from pin 5. The frequency from pin 5 again asserts the Phase/Frequency Detector to continue the loop and generate a predictable center frequency until a read operation occurs.

During read operations, the FDC issues a high VCO Synchronizing signal from pin 24. This signal prevents the Phase/Frequency Detector from generating a free-running center frequency by holding pins 11 and 3 of L99 high. The VCO Synchronizing signal drives L103 (2I8) pin 2 high, enabling L103 to receive the D READ DATA signal from the FDD. Data from the FDD can then be accepted, via L103, for conversion into a digital data stream.

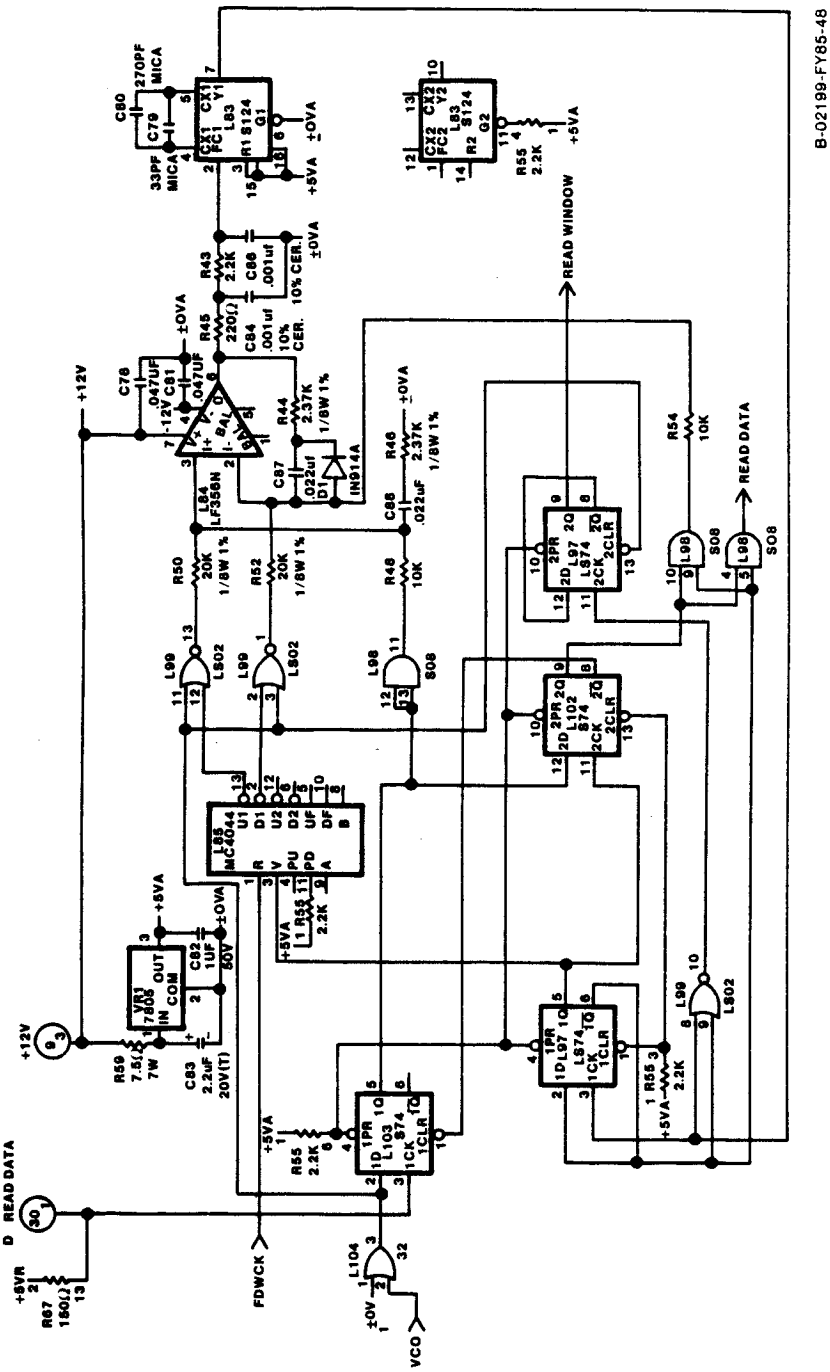


FIGURE 2.5-6
Data Recovery Logic

The data recovery logic recognizes data from the FDD as phase transitions; therefore, during read operations, only the data's phase is significant. L103, when clocked by D READ DATA, issues a signal (from pin 5) containing the phase information the recovery logic needs to convert the FDD data into digital form. The FDD data is gated through L98 (2I5) to assert pin 3 of Op Amp L84. The data also asserts L102 (2H5) pin 12 to generate the READ DATA signal, which is sent to the positive input of the Op Amp. L84 the OP Amp compares the data on its input pins 2 and 3 and issues an error voltage relative to those inputs. This error voltage asserts the VCO, and the VCO, in turn, produces an error frequency that reflects the error voltage. L97 halves the error frequency and transmits it to L102 pin 11 to clock data in.

The synchronized READ DATA signal from L102 pin 9 is fed to the FDC via L98. READ DATA is continually fed back through the loop to reduce the phase error and, therefore, keep the frequency from the VCO within the correct range to separate the data. The FDC reads data when the READ WINDOW signal created by L97 is active (ie, the read window is open).

2.6 SERIAL DATA LINK

2.6.1 Command Decoder

The RCU activates &50BSLCT1 (50BUS Device Select 1) on the 50BUS to select the Serial Data Link I/O ports. Seven commands (see Table 2.6-1) allow the RCU to communicate with a Serial Data Link port on the RMU board. The Serial Data Link Command Decoder (L110 (3G13), see FIGURE 2.6-1) decodes RCU-generated commands from the 50BUS address lines when the Serial Data Link is selected and 50BREQ (50BUS Byte Request) is strobed on pin 6. 50BUS Address Bits 50BA0-2 assert L110 pins 1-3 to select the commands that control the Serial Data Link ports. Appendix D Part 1 describes the 8X305 instruction sequences used to complete the Serial Data Link commands.

During transmit and receive operations, the 8X305 issues the necessary commands and then halts and waits for a response from the Serial Data Link (SDL) logic. After executing a transmit or receive command, the SDL logic deactivates the Clear Halt (&CL HALT) signal to clear the Microcontroller halt. The SDL logic deactivates &CL HALT in response to an active Serial Data Link Byte Request (&BYTE REQ), Serial Data Link Byte Received (&BYTE REC), or &NO DATA signal. In one of the final steps of all SDL operations, the Microcontroller senses SDL Status Register L126 (3G10) to determine which signal cleared the halt state.

A combination of the Channel Select (&CHAN SLCT) signal and the 50BD0-1 Data Bits controls channel selection during SDL receive and transmit operations. (Channels always are selected before the receive or transmit operation is performed.) The Channel Select Flipflops (L125 (3G6-7)) are loaded with the proper channel code via 50BD0-1. &CHAN SLCT then clocks the flipflops to present 50BD0-1 to either the Receive or Transmit Channel Selector. The selected channel number equals the hexadecimal code of 50BD0-1 (eg, hex code 0 selects Channel 0). After the channel is selected, the 8X305 issues instructions and data to begin the receive (1H on 50BA0-3) or transmit (0H on 50BA0-3) operation.

Table 2.6-1: SERIAL DATA LINK COMMANDS

COMMAND	50BA0-2 (HEX)	DEFINITION
&TRANSMIT	0	Transmit (pin 15). Enables Serial Data Link transmit logic.
&RECEIVE	1	Receive (pin 14). Enables Serial Data Link receive logic.
&CHAN SLCT	2	Channel Select (pin 13). Selects channel for upcoming transmit or receive operation. Channels are selected from 50BUS Data Bits 50BD0-3 as follows: 50BD0-3 (Hex) Channel 00 0 01 1 02 2 03 3
&XMIT DATA	3	Transmit Data (pin 12). Moves data from 50BUS Data Bus into Serial Data Link transmit logic.
&RECD DATA	4	Receive Data (pin 11). Moves data from Serial Data Link receive logic onto 50BUS Data Bus.
&STATUS READ	5	Status Read (pin 10). Places Serial Data Link Status Nibble on 50BUS bits 50BD0-4. Data is interpreted as follows: 50BD0 = 0 - Received data byte 50BD1 = 0 - Received data parity error 50BD2 = 0 - Byte requested for transmit 50BD3 = 0 - No data timeout detected
DIAGNOSTIC	6	Diagnostic (pin 9). Allows diagnostic routine from RCU to check Serial Data Link logic on RMU board.
SPARE	7	Not Used (pin 7).

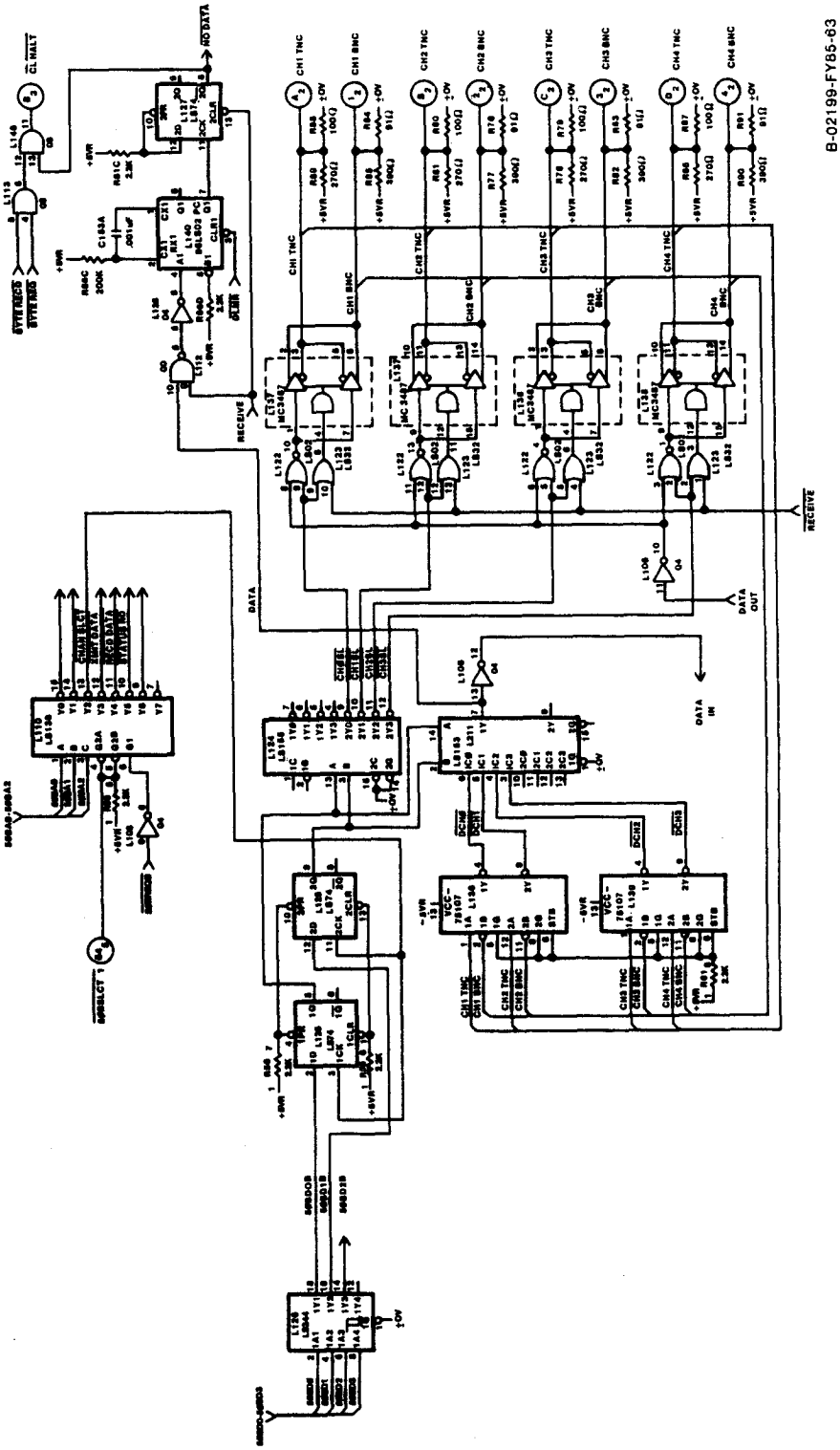


FIGURE 2.6-1
SDL Operation Control Logic

Loopback Control Flipflop L120 (3E9) places the SDL into a loopback mode for diagnostic testing. L110 issues a diagnostic command with 50BD2B = 1, causing L120 to generate the Receive Enable (REC ENB) signal. REC ENB enables the Receive Timing logic, but does not enable the receive logic to accept data from the 50BUS. ENABLE SAMPLE and &RECD DATA enable the SDL receive logic to receive data from the SDL transmit logic. (The loopback capability can be implemented as needed, but is not currently used in any diagnostic routines.)

2.6.2 Receive Operation

Serial Data Link Receive operations are initiated when the 8X305 Microcontroller issues a 1H code on Address Bits 50BA0-3 and &50BSLCT1 (50BUS Device Select 1) and &50BREQ (50BUS Byte Request) are active. In response, Command Decoder L110 issues the Receive signal on pin 14 to assert Receive Latch L109 (gate 2 (3F9)) to hold the receive condition active. L109, in turn, issues RECEIVE to the SDL receive logic to instruct and enable the logic to receive data. RECEIVE from L109 is gated through L108 to create the REC ENB signal. REC ENB deactivates the clear pins of Start Bit Detector L78 (3F13) and Enable Sample Flipflop L91 (3E11), allowing these chips to function when the Start Bit is detected. FIGURE 2.6-2 and 2.6-3 show the SDL Receive Block Diagram and the SDL Receive Logic. FIGURE 2.6-4 illustrates receive operation timing signal interaction.

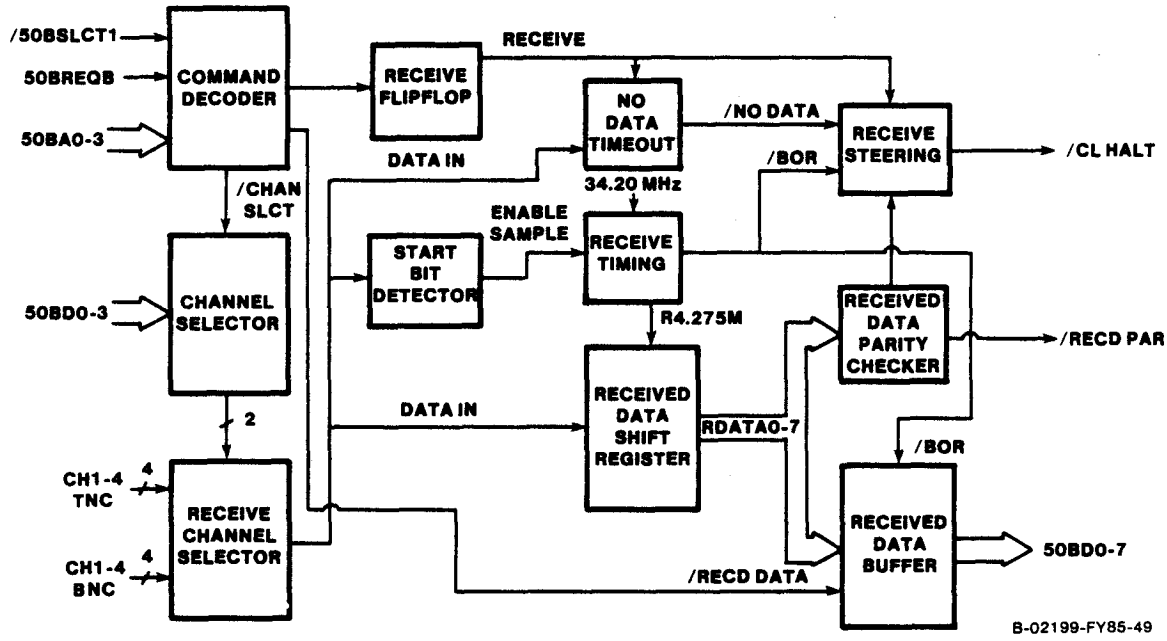


FIGURE 2.6-2
SDL Receive Block Diagram

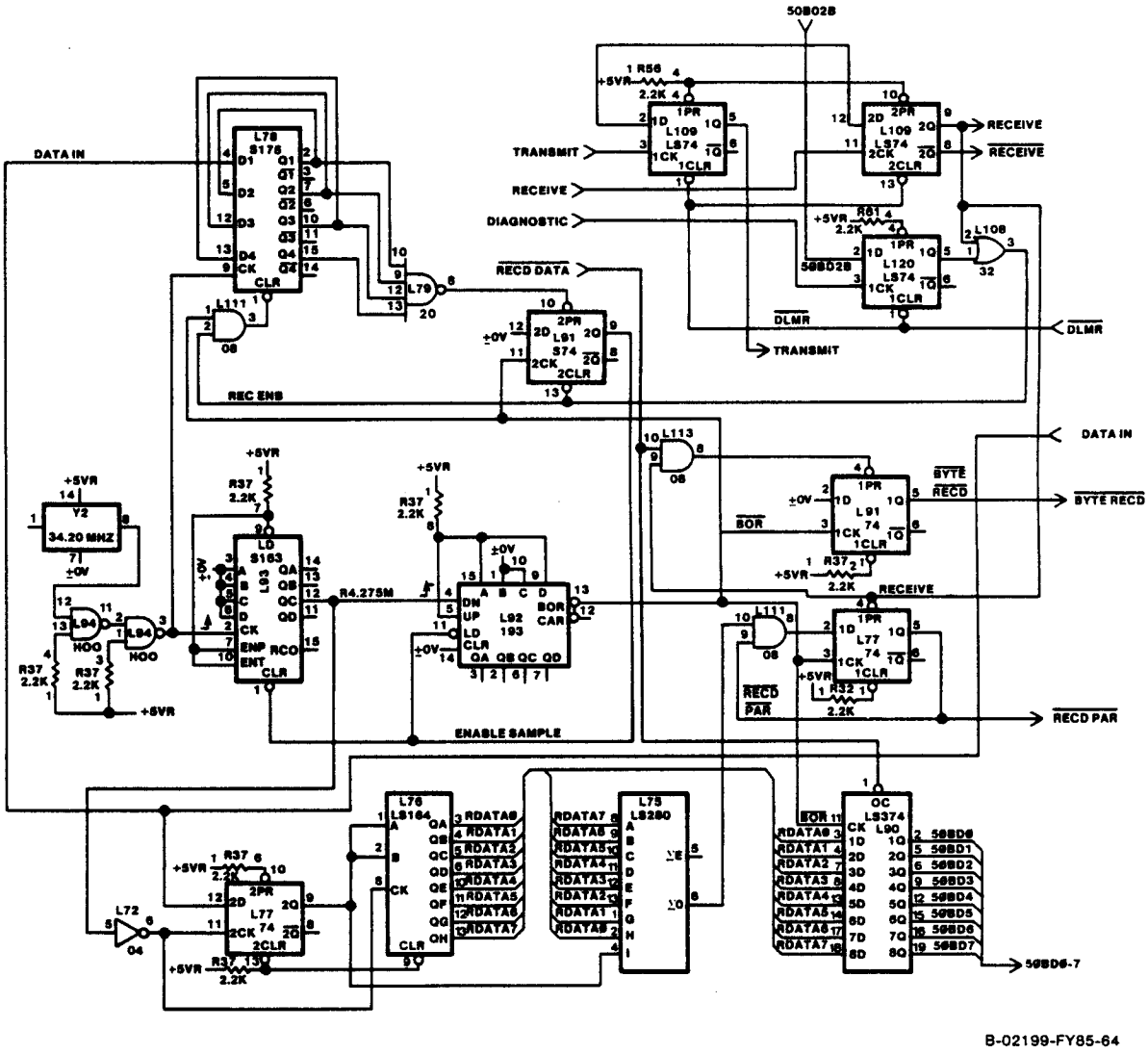


FIGURE 2.6-3
SDL Receive Logic

Data enters the RMU board via Serial Data Link Receivers L136 and L139 (3E-F7). Each 11-bit data word contains a start bit, eight data bits, a parity bit, and a stop bit. Data from the Serial Data Link channels is supplied to Receive Channel Selector L121 (3F6), which selects a data channel according to the signals (on its input pins 2 and 14) from the Channel Select Flipflops (L125). L121 transmits (on pin 7) data from the selected channel as the DATA IN signal.

L78 (3F12), the Start Bit Detector, samples the data stream (DATA IN) from the Receive Channel Selector at a 34.20-MHz rate to detect the Start Bit and to determine that the received word is legal. Upon detecting a legal Start Bit, L78 causes L79 to issue a low signal that presets Enable Sample Flipflop L91 (3E11). When the preset of L91 is held low and the clear pin of L91 is held high by an active REC ENB signal, L91 generates the Enable Sample signal. ENABLE SAMPLE asserts the Receive Shift Frequency Generator (L93 (3C12), pin 1) and the Receive Bit Counter (L92 (3C13), pin 11) to initiate their timing functions.

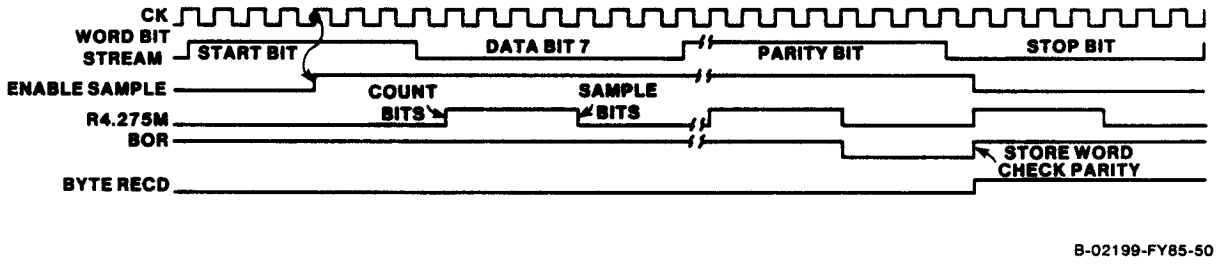


FIGURE 2.6-4
SDL Receive Timing

Serial Received Data Shift Register L76 (3A12) receives (via L77) eight of the 11 bits in a data word, assembles these bits into an 8-bit word, and then places this word onto Data Bus RDATA0-7. L75 (3A11), the 9-bit Serial Received Data Parity Checker, examines the received data's parity bit; if the data has the correct (ie, odd) parity, L75 issues a high signal to Parity Latch L77 (3C9). Upon receipt of the Received Data (&RECD DATA) enabling signal and the Serial Data Link Receive Borrow Strobe (&BOR) clocking signal, Received Data Bus Buffer L90 (3A9) places RDATA0-7 onto the 50BUS.

Receive Shift Frequency Generator L93 and Receive Bit Counter L92 derive the receive logic timing signals from the 34.20-MHz signal generated by SDL Clock Generator Y2. L93 uses the 34.20-MHz signal to generate a 233-ns (4.275-MHz) signal that asserts L77 (3A13) pin 11 to clock data in. L92 counts the nine bits (eight data bits plus a parity bit) contained in each word it receives and generates &BOR upon receipt of each complete word. &BOR then clocks the Receive Parity Flipflop (L77 (3C9)) and the Receive Control Flipflop (L91 (3D9)), causing them to generate the Received Parity (&RECD PAR) and Byte Received (&BYTE RECD) signals. &RECD PAR is fed to the SDL Status Register, and &BYTE RECD clears the &CL HALT (Clear Halt) signal via L113 and L146 (3I2) to inform the Microcontroller that the Serial Data Link has completed the receive operation.

2.6.3 Transmit Operations

Serial Data Link transmit operations are initiated when the 8X305 Microcontroller issues a 0H code on Address Bits 50BA0-3 and &50BSLCT1 (50BUS Device Select 1) and &50BREQ (50BUS Byte Request) are active. Command Decoder L110 responds by issuing the Transmit Data (&XMIT DATA) signal. &XMIT DATA clocks the data to be transmitted from the 50BUS (50BD0-7) onto the TDATA bus via Transmit Data Bus Buffer L74 (3A7). FIGURE 2.6-5 and 2.6-6 show the SDL Transmit Block Diagram and the SDL Transmit Logic. FIGURE 2.6-7 illustrates transmit operation timing signal interaction.

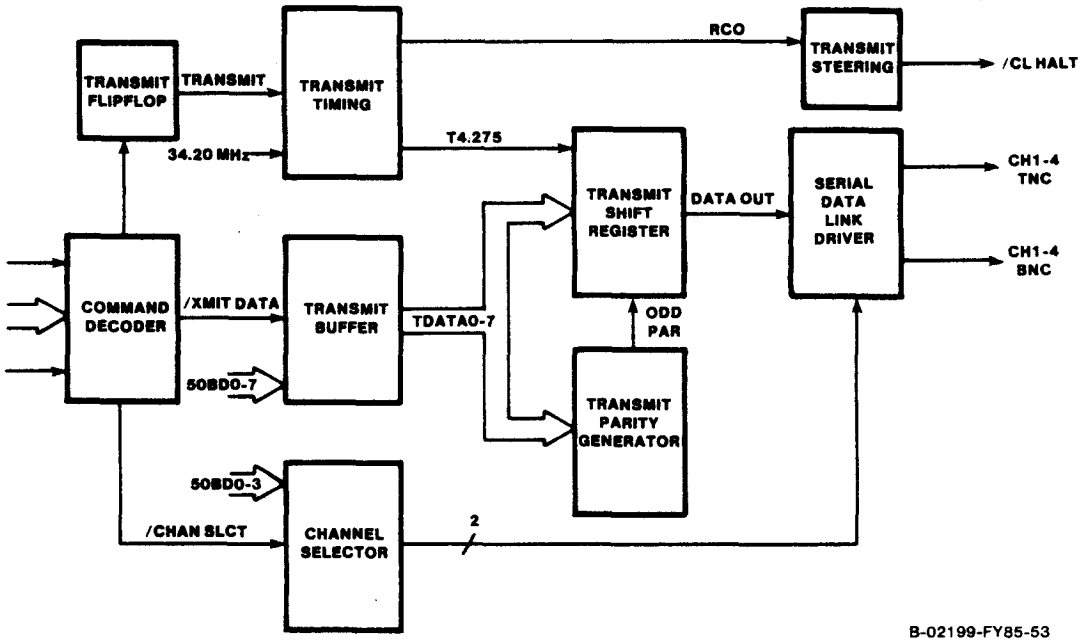


FIGURE 2.6-5
SDL Transmit Block Diagram

After issuing the &XMIT DATA signal, Command Decoder L110 issues the Transmit signal (in response to instructions from the RCU). TRANSMIT from L110 pin 15 asserts Transmit Latch L109 (gate 1 (3F10)) to hold the transmit condition active. L109, in turn, issues TRANSMIT to enable the Serial Data Link transmit logic by deactivating (via L111) the signals that assert the clear pins of L56-59 (3B1-4 and 3C7). When TRANSMIT is activated, the transmit logic begins processing the data that was loaded by &XMIT DATA. Shift Control Flipflop L40 (3C6), which is enabled when the Transmit signal deactivates its preset pin, generates a Shift signal from pin 5 that follows the T4.275 input on L40 pin 3. The Shift signal asserts (via L44) the shift/load pins of the Transmit Shift Registers, L56-58, placing the registers in the shift mode.

Transmit Data Parity Generator L73 (3B5) generates odd parity for received data bits TDATA0-7. Transmit Serial Data Shift Registers L56, L57, and L58 shift the data in response to the 4.275-MHz transmit clock. The serial data stream is shifted to the SDL Drivers (via L56, pin 14) as the DATA OUT signal.

Data is transmitted out of the Serial Data Link logic by gating the DATA OUT signal through one of the four SDL Drivers (two each on L137 and L138). The Channel Select (&CH0-3SL) signals from Transmit Channel Selector L124 enable the driver for transmission.

Transmit Shift Frequency Generator L60 (3C8) and Transmit Bit Counter L59 derive the transmit logic timing signals from the 34.20-MHz signal generated by SDL Clock Generator Y2. After being enabled by the TRANSMIT signal, L60 converts the 34.20-MHz signal into a 233-ns (4.275-MHz) clock signal that is used to shift data out. Shift Control Flipflop L40 generates a signal from pin 6 that asserts L62 to introduce a 233-ns delay in the generation of the &BYTE REQ signal. This delay prevents &BYTE REQ from being generated too early and causing a race condition.

Transmit Bit Counter L59 counts each clock pulse from L60 to count the 11 bits (Start bit, eight Data Bits, Parity Bit, and Stop Bit) contained in each transmitted word. Upon counting the 11th bit, L59 generates the Carry Out (RCO) signal. When clocked by RCO, Byte Request Flipflop L61 (3C3) generates the &BYTE REQ signal to deactivate the Clear Halt (&CL HALT) signal. &BYTE REQ clears the &CL HALT signal via L113 and L146 (3I2) to inform the Microcontroller that the SDL has completed the transmit operation.

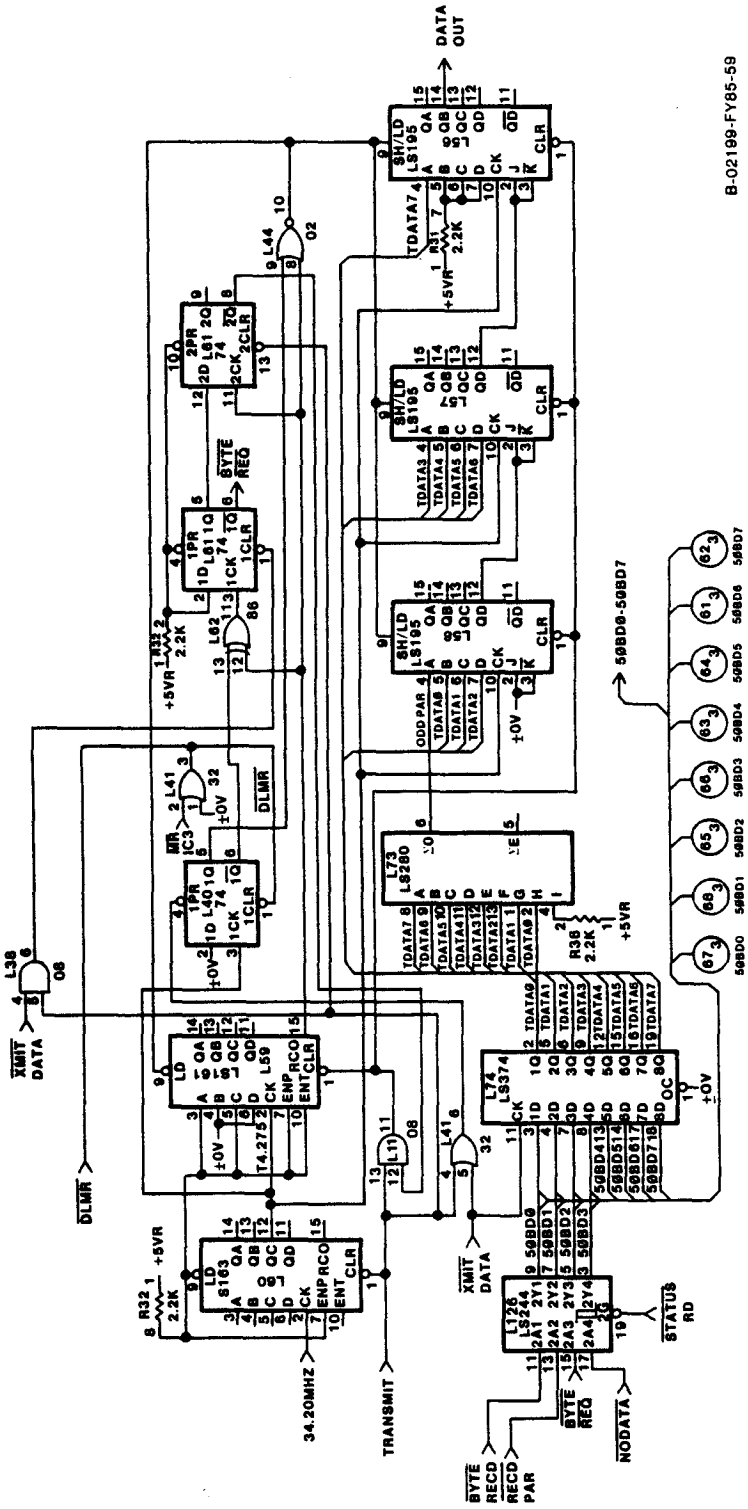


FIGURE 2.6-6
SDL Transmit Logic

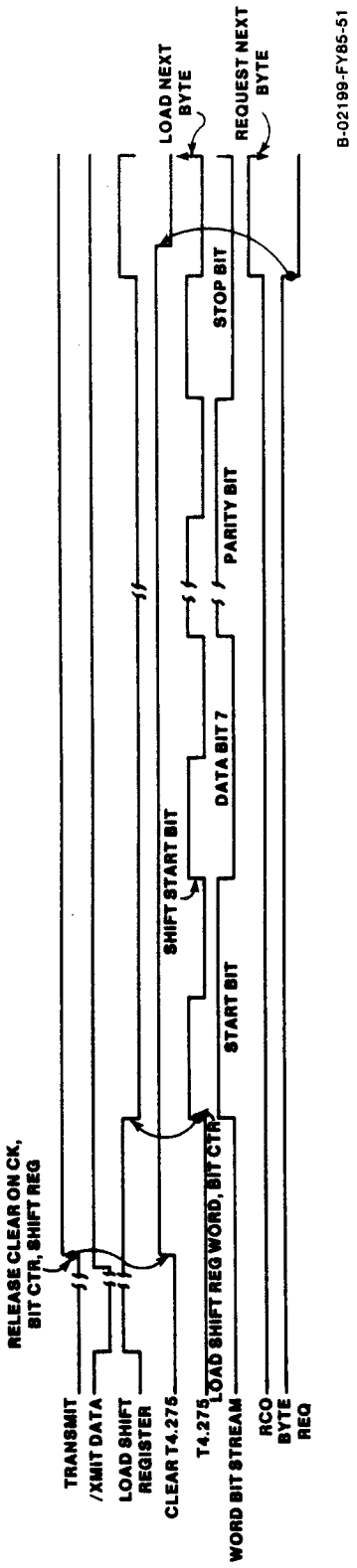


FIGURE 2.6-7
SDL Transmit Timing Diagram

&XMIT DATA clears Byte Request Flipflop L61 via L38 (3D6) as each new byte is loaded into the transmit logic; &XMIT DATA does not clear L61 at the end of the transmit operation, however, because no new bytes are being loaded into the transmit logic. If the Transmit signal is still active, L59 continues to count bits from the Transmit Shift Frequency Generator. When L59 generates the next RCO signal, L61 (3C2) generates a low signal (from pin 8) that clears the Shift Registers (via L111, pin 11 (3B11)) by activating the clear pins of the Shift Registers and the Bit Counter. A continuous data stream of zeros is shifted out of the Shift Registers until TRANSMIT is deactivated. Deactivating the Transmit signal at any time during the transmit operation also causes L111 to generate a signal (from pin 11) that clears the transmit logic.

2.6.4 Status Register

Four status bits and the 50BD0-3 Data Bus report the status of the SDL Transmit or receive logic to the 8X305. The Microcontroller accesses the SDL Status Nibble via SDL Status Register L126 (3A8) and the &STATUS RD command. Table 2.6-2 lists and defines the Status Bits.

Table 2.6-2: SERIAL DATA LINK STATUS BYTE

BIT	SIGNAL	DEFINITION
50BD0	&BYTE RECD	Generated by L91 to indicate that the Serial Data Link has received a data byte. Also clears the 8X305 halt condition.
50BD1	&RECD PAR	Generated by L77. Indicates that the Serial Data Link has received a data byte containing a parity error.
50BD2	&BYTE REQ	Generated by L61 to indicate that the Serial Data Link has transmitted a data byte. Also clears the 8X305 halt condition.
50BD3	&NO DATA	Generated by L127. Indicates that a Serial Data Link Receive operation was commanded, but either no data was received or the data was interrupted.

During receive operations, Receive Parity Flipflop L77 and Byte Received Flipflop L91 generate the Received Parity (&RECD PAR) and Byte Received (&BYTE RECD) signals (see Section 2.6.2). &BYTE RECD functions as a status signal and also deactivates the &CL HALT signal via L113 and L146 (Section 2.6.1). &RECD PAR from L77 functions only as a status signal.

L61 generates the &BYTE REQ signal to indicate that a byte of data is needed for transmission (see Section 2.6.3). &BYTE REQ functions as a status signal and also deactivates the &CL HALT signal via L113 and L146 (Section 2.6.1).

No Data Flipflop L127 (3H1) generates the &NO DATA signal to indicate that an SDL receive operation was commanded and initiated, but either no data was received or the data was interrupted. The No Data Timeout 1-Shot (L140 (3H2)) is activated when RECEIVE is active and DATA is inactive on the inputs of gate L112. L112 then generates a signal that triggers the 1-Shot via L128. If no data is received, the 1-Shot times out for 86 us and generates a signal from pin 7 to clock L127. If the No Data Flipflop is cleared by the inactive Receive signal within 86 us (prior to the clocking signal), it does not generate the &NO DATA signal. If, however, RECEIVE is still active when the clock signal arrives, L127 issues the &NO DATA signal from pin 8 to deactivate the Clear Halt (&CL HALT) signal via L146. Deactivating &CL HALT causes the 8X305 to function as if SDL command execution had proceeded normally. The 8X305 detects the no data condition when it reads SDL Status Register L126 at the completion of the receive command.

This concludes the theory of operation section for the RMU circuit board. Refer to Section 8 for troubleshooting tips for the Resource Management Unit (RMU).

SECTION 2 QUIZ

1) What two ways does the RCU have to inform the RMU that a non-immediate command has been completed?

2) If SW1 is depressed during TESt 1 of the BIT what will happen?

3) What purpose does the AUTO RESET signal provide?

4) Why is the signal PWAIT generated during MMI/O operations?

5) What two way does the RCU have to request the Data and Address busses of the RMU?

6) What are the two sources of Non-Maskable interrupts for the Z80A on the RMU?

7) Which bit of the Address bus is used as a synthetic refresh bit?

8) The PROM enabling flipflop performs what function?

9) What are the three phases of a floppy drive access?

10) If the dead-man timer is not reset after 540 nsec what happens?

11) How many commands are used to communicate between the RCU and the SDL?

12) What do the four bit of the SDL status register indicate?

SECTION 3
RESOURCE CONTROL UNIT (RCU)

SECTION 3

Resource Control Unit (RCU)

3.1.1 GENERAL INFORMATION

The 8267 Resource Control Unit (RCU) used in the OIS 40 and OIS 50 multiprocessor-based data processing systems contains the 4K x 8 Data Buffer, 1K-byte Scratchpad RAM, 16-byte Parameter Register File (PRF), 12-byte Status Register File (SRF), Winchester Disk Drive Interface, 50BUS Interface, and 10-MHz 8X305 Microcontroller. The 4K x 8 Data Buffer on the RCU board is a 4K-byte buffer used as a data storage area during all block data moves between any two boards in the OIS system. Scratchpad RAM is a temporary storage area for tables and program variables. The PRF is used as a common area for data moving between the Resource Management Unit (RMU) and the RCU. Status information sent from the RCU to the RMU uses the Status Register File as a intermediary storage area. The 50BUS is an internal bus that connects all devices within the OIS 50. The 8X305 Microcontroller maintains control over most RCU operations. FIGURE 3.1-1 is a block diagram of the Resource Control Unit.

The Microcontroller generates two control signals, called the Left Bank (LB) and Right Bank (RB) signals, to optimize its data accessing capabilities. By providing left and right bank I/O options, the Microcontroller can access a total of 512 ports. The Microcontroller in the RCU maintains 256 x 8 bytes of Scratchpad RAM on its left bank as a temporary storage area for tables and program variables. The RCU's right bank contains I/O port commands to control major RCU functions.

The RCU's 4K x 8 Data Buffer serves as a temporary storage area for data passing between the RCU and the Winchester or floppy disk drives. The Microcontroller uses 4K x 16 bytes of RCU-resident PROM to store its instruction code. Addresses for PROM-resident instructions are generated by the Microcontroller and sent to the PROM via the XA0-12 bus. XA1, the control bit of the XA0-12 bus, selects high-order (active XA1) or low-order (inactive XA1) PROM.

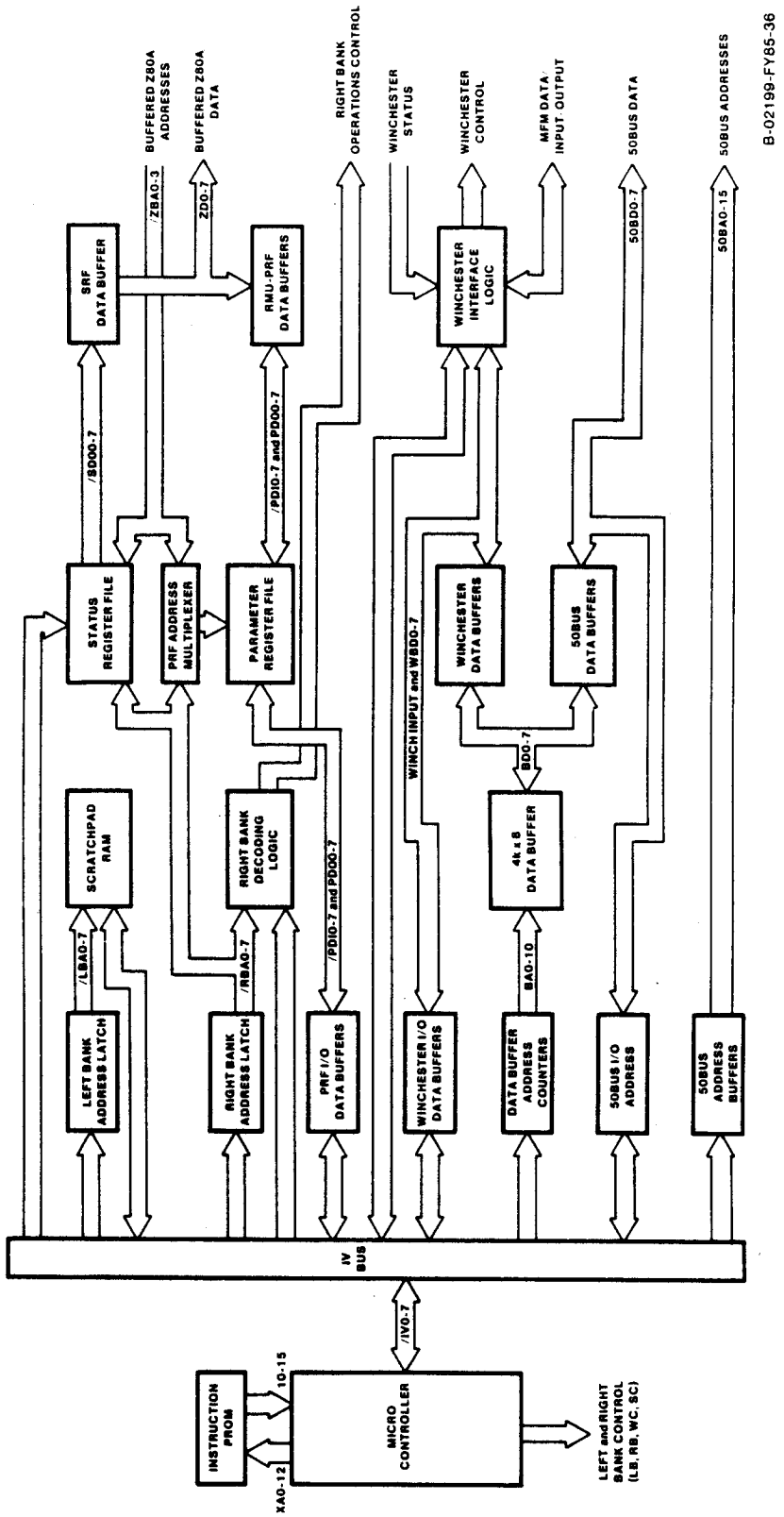


FIGURE 3.1-1
Block Diagram of the Resource Control Unit

During Winchester read/write operations, the Microcontroller controls the Winchester disk drive and loads or empties the 4K x 8 Data Buffer. When the Winchester access operation has been completed, the Microcontroller presents status information (via the Status Register File) and the Control Unit Not Busy (&CUBUSY) interrupt to the Z80A. The Winchester Seek Complete (WSKCMP) interrupt is generated by the Winchester disk drive and sent directly to the Counter Timer Chip (CTC, channel 2) on the RMU board.

3.1.2 RMU-RCU Interaction

RMU-RCU communication involves shared memory, a Command Notification (&CMD) bit, and the 8X305 Microcontroller interrupts that assert the Z80A. Two memory areas on the RCU board are shared between the Z80A and the Microcontroller: the 16-byte Parameter Register File (PRF) and the 12-byte Status Register File (SRF). Both the Z80A and the Microcontroller can read from or write to the PRF; however, they cannot access the PRF simultaneously. Only the Z80A can read the SRF, and only the Microcontroller can write to it.

The RCU receives RMU requests via the Parameter Register File. The Z80A microprocessor on the RMU loads the PRF with the command codes and data that the RCU needs to perform a specific operation. When the Z80A sets the Command Notification bit, the Microcontroller operates on the PRF as needed to complete the command. (Generally, the Microcontroller moves the PRF data to its Scratchpad RAM and then releases the PRF.) The PRF must be released quickly because the Z80A is suspended (ie, held in a bus request state) while the Microcontroller controls the PRF. If the Z80A is suspended for too long a time, the RAM on the RMU board will decay due to the lack of Z80A-generated refresh cycles.

PRF byte assignments depend upon the function requested (see Appendix G). Typically, the Z80A issues the FF20 (Command Request) byte and the FF22 (Specify Command) byte to the PRF. The RCU reads the bytes, defines the remaining bytes according to specific command requirements, and then returns the FF21 (Command Acknowledge) byte to the PRF for the Z80A to read. To avoid invalid parameter errors, unused or undefined bytes should always be cleared to zero.

To perform a function that involves the RCU, the Z80A loads the command request and necessary data into the PRF. The Z80A then writes to address FF30 to issue the Command Notification bit that initiates the command. Normally, the Microcontroller is polling, waiting for the Command Notification bit to be set. When the RMU issues a command, the Microcontroller can perform one of two routines. If the command is an immediate command, the Z80A is awaiting command completion and the RCU must, therefore, execute the command immediately. If, however, the command is a non-immediate command, the RCU releases the Z80A after moving the data from the PRF to the scratchpad. The RCU then executes the command and notifies the Z80A upon completion.

Upon receiving an immediate command, the RCU checks to see that the command code is valid, copies the PRF to its scratchpad RAM, completes the requested operation, and releases the RMU. When the 8X305 Microcontroller performs a 1-byte operation, for example, it does not immediately release the PRF. The Microcontroller holds the Z80A in a suspended state for a maximum of 1 ms (otherwise the lack of dynamic RAM refresh could cause a memory data loss). When the Microcontroller releases the Z80A, the data and/or status information from the 1-byte operation is immediately available to the Z80A via the SRF.

Upon receipt of a non-immediate command, the RCU checks to see that the command code is valid, copies the PRF to its scratch RAM, sets RCU Busy status in the SRF, releases the RMU, completes the requested operation, and issues either an interrupt request or a Control Unit Not Busy (&CUBUSY) signal to the RMU when the operation has been completed.

Status and error information returns to the RMU via the dual-ported SRF. When the Microcontroller is busy, RCU Busy status information is set in byte FF10 of the SRF. Status information concerning Data Link block operations resides in SRF bytes FF11 and FF12. SRF bytes FF13-FF15 contain status information concerning the 1-byte Serial Data Link operations, and bytes FF16-FF1B contain status information concerning the Winchester Disk Drive.

3.1.3 RMU-RCU Interface

The interface between the Resource Control Unit (RCU) and the Resource Management Unit (RMU) resides on the RCU board. FIGURE 3.1-2 shows a block diagram of this interface. Data passing to and from the Z80A on the RMU must pass through L149 (1I10), a data transceiver. The direction of the data flow is determined by the decoding of the MMI/O signals sent from the RMU. Table 3.1-1 lists the MMI/O commands generated by the Z80A. L98 (1J13) decodes the commands by looking at the upper nible of the lower byte of the Z80A port address (A4-7). Looking at Table 3.1-1 you can see that the upper nible of the lower byte only changes from a 1 through a 4, thus selecting the command. The lower nible of the lower byte selects the address in either the (PRF) or (SRF) that the data is to transferred. The upper byte of the port address is always FF for MMI/O operations.

There are three buffers connected to the B side of L149. Two of these buffers are use to transfer data to and from the (PRF), while the other buffer allows the (SRF) to sent data to the Z80A. The selection of these buffers is either from decoding of the Z80A MMI/O signals or form the 8X305 Microcontroller.

The (SRF) is comprized of six LS670's, these are 4-by-4 register files with each containing separate read and write address inputs. When the Z80A wishes to read the status of an operation the address is decoded using L98 (1J13), L99 (1H13) and L103 (1I12). This decoded address is sent to pin 4, 5 and 11 of each of the chips. Pins 4 and 5 select the location within the chip while pin 11 selects the chip for a read operation. The actual chip selection is determined by L103 through address bits BA2-3. L103 also selects the (SRF) data buffer through L86 (1G11) thus allowing the selected data to pass to the data transceiver. The status information in the (SRF) was written into it by the 8X305 Microcontroller. The data was presented to each of the chips from the IV0-7 data bus, while the address was sent to pin 12, 13 and 14. Pins 13 and 14 did the selection of the location within the chip, while pin 12 selected the chip. Chip selection was generated from dacoder L79 (2F6). This information is decoded from the data generated by the 8X305.

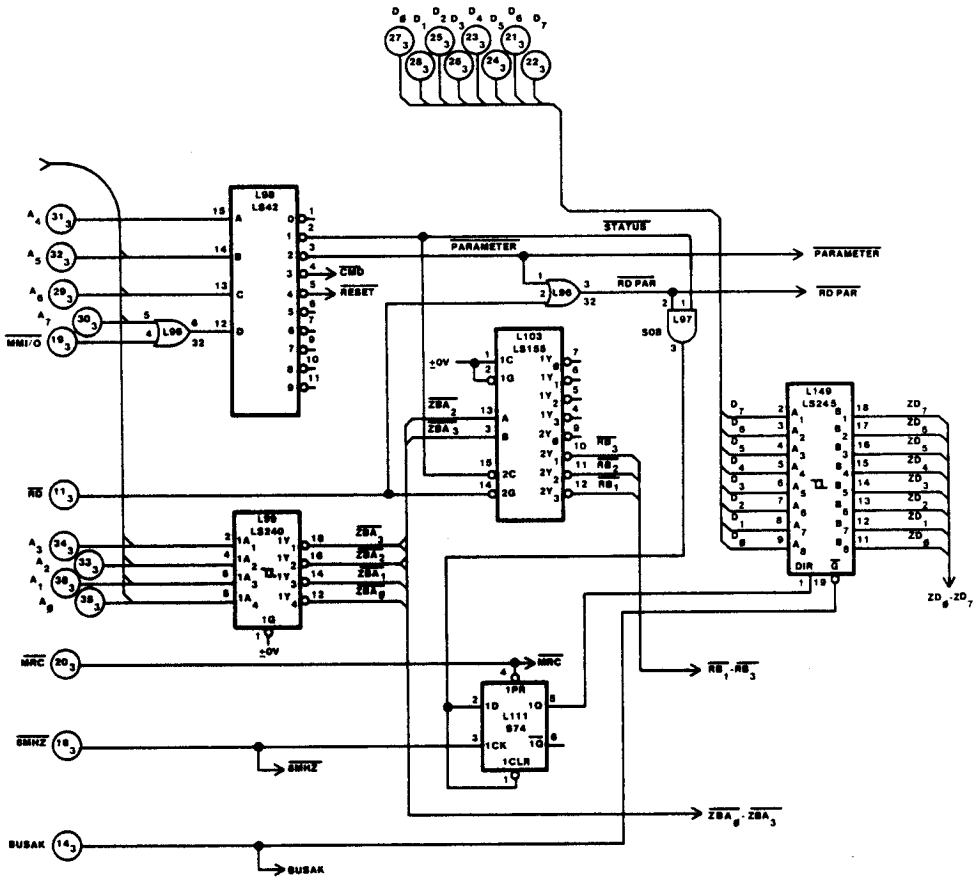


FIGURE 3.1-2
RMU/ RCU Interface Block Diagram

The Parameter Register File can be written to by the Z80A to instruct the RCU to perform an operation. The parameters are passed through the data transceiver and on to the inputs of L116 (1F9) the (PRF) Input Data Buffer. At this time the Z80A generates a write to the paramter register which is decoded by L98 (1J13). L98 will generate &PARAMETER which will enable L116 the (PRF) Input Data Buffer and both L100 and L101 (1B8-10), the (PRF). Since the Z80A is writing to the (PRF) it will also generate &WR, entering at (1A14). &WR is gated with &PARAMETER through L64 (1A11) and L97 (1A10) to activate the write enbale of the (PRF). After all of the parameters are stored in the (PRF) the Z80A will then set the CMD bit, informing the RCU that a command is pending.

The (PRF) can also be read by the Z80A. This is accomplished by the Z80A reading MMI/O loaction FF20-FF2F. The Z80A issues a &RD along with the address within the (PRF) that it wishes to read. The &RD signal is gated with &PARAMETER through L76 (1J12) to generate &RD PAR. &RD PAR has two functions, first it is gated through L97 (1J11) to the Data Direction Control Flipflop. On the next clock pulse from the 8Mhz clock the data transceiver will be placed in the B-to-A mode. The second function of &RD PAR is two fold, first it enables the (PRF) Data Out Buffer and second it enables the (PRF) memory chips by driving pin 2 of L00 and L101 low.

The location within the (PRF) that the data is to be transfered to or from is selected by L102 (1D10). This data selector selects addresses from either the Z80A or the 8X305 Microcontroller. The Z80A address come from the same circuits that generated the address for the (SRF), while the address from the 8X305 Microcontroller are generated by L85 (2G8) (more on this later). L102 receives its select signal from L25 the Command Bus Request Flipflop. This flipflop is normaly in the reset state, thus deactivating CMDBUSREQ causing the select input of L102 to select the A inputs. If this were a write operation to the (PRF) the Z80A would issues a CMD command after all the data had been transferred, thus causing L25 to set causing the RCU to start the its operation.

The Z80A set L25 by issuing FF30-FF3F MMI/O instruction, this forces L98 to activate &CMD. &CMD is placed directly on the preset input of L25 forcing it set. The Q output of L25 will go high activating CMDBUSREQ causing L102 to select the RCU address information. At the same time the &Q output will go low, causing several things to happen. First this low is sent back to the RMU notifing the Z80A that the RCU is performing an operation. Secondly this low is sent to L133 the IV Bus to (PRF) Input Data Bus Buffer. Here it activates L133 allowing the 8X305 the ability to write data into the (PRF) if needed during the operation. Lastly the low on the 2Q output of L25 is sent to L94 (1B7).

Table 3.1-1: Z80A-GENERATED I/O COMMANDS

Z80A Port Address	I/O Command	Function
FF10-FF1F (R)	&STATUS	Read the 12-byte Status Register File. Data located in FF10-FF1B are the result of a previously executed Microcontroller command. FF1C-FF1F are not used.
FF20-FF2F (W/R)	&PARAMETER	Read or write the 16-byte Parameter Register File. The read or write operation is specified by the condition of the Z80A Read Request (&RD) signal from the RMU board.
FF30-FF3F (W)	&CMD	After the Z80A writes to any location in the (PRF) it will set Command Bus Request Flipflop. The &CMD bit generates the Command Bus Request (&CMDBUSREQ) signal to notify the Microcontroller that a command has been loaded in the PRF and the Z80A has surrendered bus control.
FF40-FF4F (W)	&RESET	Accessing any one of the 16 PRF locations generates a Z80A Reset (&RESET) signal that resets the Microcontroller and, therefore, the RCU board.

The 8X305 Microcontroller is normaly in a poling mode of operation, and during this operation it will activate &RD INPUT DATA and &COMMAND. These two signals will activate the trystate input of L94, thus allowing the low on pin 2 to be placed on IV7 of the 8X305 bus. The 8X305 Microcontroller will check this bit, looking for it to be low (which it is). Once the 8X305 find this bit low it will start reading the (PRF) to determine what operation it is to perform.

3.2: 8X305 MICROCONTROLLER

The RCU's 8X305 Microcontroller (see FIGURE 3.2-1 and 3.2-2) controls most of the OIS 50's functions. Instructions for the Microcontroller arrive from the 4K x 16 PROM storage area via the 16-bit I0-15 instruction bus. Addresses for PROM-resident instructions are generated by the Microcontroller's address bus (XA0-12). Designed to operate with a 200-ns instruction execution cycle, the Microcontroller controls a series of peripheral devices attached to it by means of the 8-bit Interface Vector (IV) bus. The IV bus issues signals to Microcontroller Data Transceiver L69 which, in turn, generates the &IV0-7 Interface Vector bus. The Microcontroller does not use typical conventions for bit identification: on all of its buses (I0-15, XA0-12, and IV0-7), a subscript of "0" denotes the most significant bit (MSB) and the highest subscript denotes the least significant bit (LSB). The Microcontroller sends control signals to L38, the Control Signal Decoder, to create the necessary peripherals control signals.

Five control signals generated by the Microcontroller indicate the direction in which the IV bus is being driven and the type of data on the bus. Any one of up to 256 addresses (per bank) can be selected in a single instruction cycle when the Microcontroller places a unique address on the IV bus and asserts the Select Command (SC) signal. Once selected, the address normally remains selected until the SC signal is again asserted with a different address on the IV bus. The direction of data flow is indicated by the Write Command (WC) signal. The WC signal is asserted when data is being placed on the IV bus, and is not asserted when data is read from the IV bus. An IV bus read is indicated when both the SC and WC signals are inactive.

Two control signals, the Left Bank (LB) and Right Bank (RB) signals, optimize the Microcontroller's data accessing capabilities. Either of these signals is asserted concurrently with other control signals based on the contents of the instruction word. The LB and RB signals allow 512 addresses (256 on each bank) to be accessed during a single microcontroller instruction cycle. Timing on the bus is synchronized with the Master Clock (MCLK) signal. Together with the other control signals, MCLK enables access to the IV bus at the correct time in the Microcontroller's instruction cycle. The left bank reads or writes 256 bytes of Scratchpad RAM, and the right bank issues I/O Port commands, which control many OIS 50 functions.

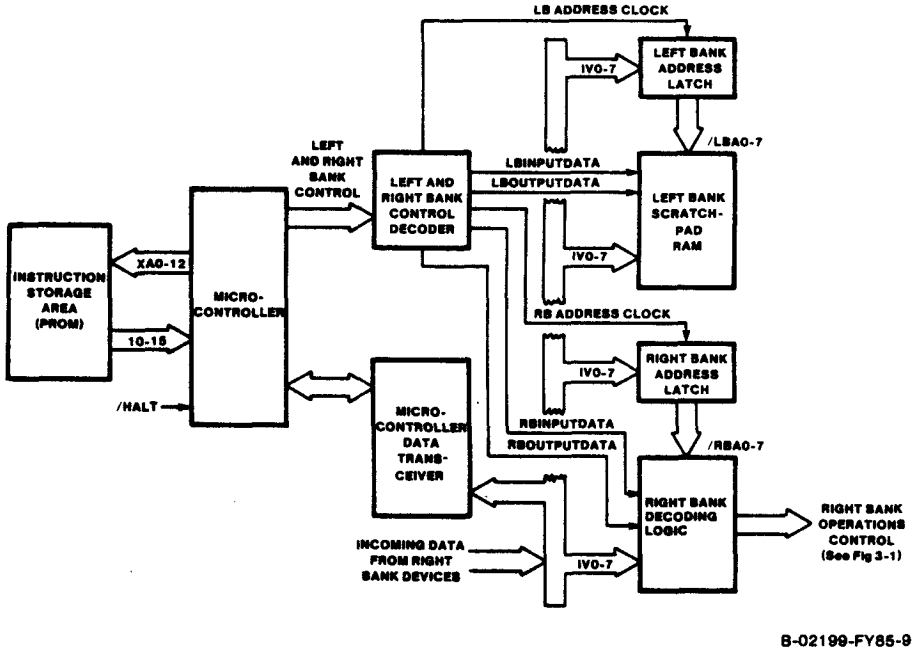


FIGURE 3.2-1

8X305 Microcontroller Block Diagram.

Control Signal Decoder L38 receives four of the five primary control signals as inputs (barring the Master Clock). The signals issued from L38 depend, of course, on the status of the incoming signals. Table 3.2-1 lists the outputs generated by the various input combinations.

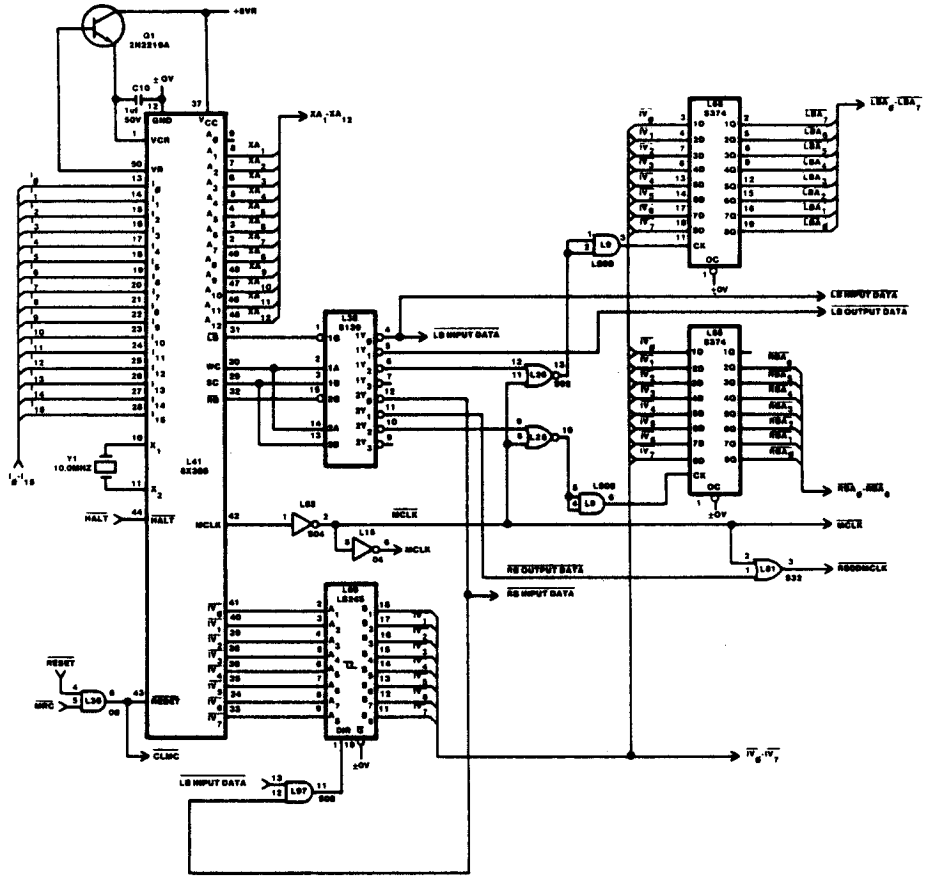
The Left Bank Input Data (&LBINPUTDATA) and Right Bank Input Data (&RBINPUTDATA) signals are used throughout the logic to enable either left or right bank read operations. The Left Bank Output Data (&LBOUTPUTDATA) and Right Bank Output Data (&RBOUTPUTDATA) signals enable either left or right bank write operations. The direction of the Microcontroller's Data Transceiver, L69, is controlled by either the active &RBINPUTDATA or the active &LBINPUTDATA signal asserting L69 pin 1 (via L97), depending on which bank has control of the read or write operation.

Table 3.2-1: MICROCONTROLLER CONTROL SIGNAL DECODER

Control Signals Active	Decoder Output Signals Active
WC, &LB	&LBOUTPUTDATA and WC (from pin 6)
SC, &LB	&LBINPUTDATA
SC, WC, &RB	&RBOUTPUTDATA and WC (from pin 10)
SC, &RB	&RBINPUTDATA

If either &RBINPUTDATA or &LBINPUTDATA is active, L97 generates a low signal that asserts pin 1 of Microcontroller Data Transceiver L69 to place the transceiver in the input direction (B-to-A). An inactive &RBINPUTDATA or &LBINPUTDATA signal places the data transceiver in the output direction (A-to-B). &RBOUTPUTDATA is synchronized with the Microcontroller's Master Clock (MCLK) signal at L81 to generate the &RBODMCLK signal. &RBODMCLK is used by all of the right bank decoders to synchronize write operations. &LBOUTPUTDATA is gated with &MCLK at L64 to generate a synchronized signal which asserts the write enable pin of the left bank scratchpad memory.

The Write Command (WC) signal is decoded from Control Signal Decoder L38 for use as an address write control signal for either the left or right bank (whichever is being asserted by the Microcontroller). If the left bank address is being accessed, L38 pin 6 asserts L26 pin 12, driving it low, which allows the &MCLK signal through to the output of L26 pin 13. From L26 pin 13, the left bank &MCLK signal then clocks L68, the Left Bank Address Latch, to store left bank addresses &LBA0-7. &LBA0-7 address 256 bytes of scratchpad RAM. If the right bank is being accessed, L38 pin 10 asserts L26 pin 9, driving it low, which allows the &MCLK signal through to the output of L26 pin 10. From L26 pin 10, the right bank &MCLK signal then clocks Right Bank Address Latch L85 to store right bank addresses &RBA0-7. &RBA0-7 are sent to decoders throughout the right bank circuitry to decode the I/O ports that control the primary RCU functions.



B-02199-FY85-10

FIGURE 3.2-2
8X305 Microcontroller Access Logic

3.2.2 Microcontroller Instruction Storage Area

Four 2K x 8 PROMs provide the 4K x 16 storage area needed for the Microcontroller's instructions set. These PROMs are addressed by a 13-bit address generated by the Microcontroller's address bus (XA0-12). The PROM places the 16-bit addressed instruction onto the I0-15 instruction bus, where it is sent to the Microcontroller for execution. L40 and L54 contain the low-order (from 0 to 2k) addressed PROM, as addressed by XA0-12. When accessing low-order PROM, L54 provides the high byte (I0-7) of the 16-bit instruction, and L40 provides the low byte (I8-15). (As explained earlier in this chapter, the Microcontroller uses an atypical convention for bit identification.) L39 and L53 contain high-order addressed PROM, from 2 to 4k, as addressed by XA0-12. When accessing high-order PROM, L53 provides the high byte (I0-7) of the 16-bit instruction, and L39 provides the low byte (I8-15). High or low order PROM is specified by the XA1 bit of the Microcontroller's address bus. Inactive XA1 asserts the low enabling pin 20 of the low-order PROM chips (L40 and L54) to enable these chips when low-order PROM is accessed. High-order PROM is enabled by the active XA1 signal asserting enabling pin 18 of L39 and L53.

3.2.3 Left Bank Scratchpad Memory

The Microcontroller uses 256 x 8 bytes of scratchpad RAM (in two 256 x 4 chips, L66 and L67) on its left bank as a temporary storage area for tables and program variables . Table 3.2-2 displays the memory map configuration of the scratchpad.

Table 3.2-2: SCRATCHPAD MEMORY MAP

Memory Location (Hex)	Memory Contents
00-0F	Parameter Register File data supplied by the RMU. Parameters are typically retrieved and decoded from the scratchpad copy of the PRF, not directly from the PRF. Some diagnostic support routines directly access and decode parameters from the PRF without copying the PRF in the scratchpad.
10-19	Physical to logical slave address mapping table. This table is created by the set slave list command.
1A-23	Hardware select code for each slave type. Slave's physical addresses are used to index this table for select codes. Slave — Physical Address — Select Code Master Memory — 00 — 01 IWS 1 — 01 — 08 IWS 2 — 02 — 10 IWS 3 — 03 — 20 IWS 4 — 04 — 40 IWISE — 05 — 80 Serial Port 1 — 06 — 02 Serial Port 2 — 07 — 02 Serial Port 3 — 08 — 02 Serial Port 4 — 09 — 02
80	Start of variable area which ends at location FF. The variable area is cleared upon power on.

Table 3.2-2: SCRATCHPAD MEMORY MAP (cont.)

80	1-byte cell devoted to serial device status Operations.
81	1-byte cell devoted to the control byte for Winchester operations.
82-83	Working storage used to count the number of headers that have passed since the beginning of the Winchester read or write operation. Currently, this number is only an 8-bit number, with location 83 reserved for expansion.
84-86	ECC syndrome or check bytes from the previous read or diagnostic read operation. The first ECC byte resides at location 84.
87	1-byte flag indicating the condition of the Winchester to slave memory chaining operation.
88-8A	Desired header bytes when chaining a Winchester write to slave read. Location 88 contains a copy of the value of FF24. Location 89 contains a copy of the value of FF25. Location 8A contains a copy of the value of FF26.
8B	1-byte flag indicating an error in a slave memory read operation. Data read is intended to be written to the Winchester.
8C-8F	32-bit count of ECC errors since power on. Byte 8C is the least significant byte. The count is not cleared when the RMU resets the RCU.
90-93	32-bit count of Winchester sector read operations since power on. Byte 90 is the least significant byte. The count is not cleared when the RMU resets the RCU.
94-97	32-bit count of Winchester sector write operations since power on. Byte 94 is the least significant byte. The count is not cleared when the RMU resets the RCU.

Table 3.2-2: SCRATCHPAD MEMORY MAP (cont.)

98-9B	32-bit count of parameter errors since power on. Byte 98 is the least significant byte. The count is not cleared when the RMU resets the RCU. One byte to master memory operations are not counted.
9C-9F	32-bit count of serial receive data parity errors since power on. Byte 9C is the least significant byte. The count is not cleared when the RMU resets the RCU.
A0-A3	32-bit count of header not found errors since power on. Byte A0 is the least significant byte. The count is not cleared when the RMU resets the RCU.
A4-A7	32-bit count of header LRC errors since power on. Byte A4 is the least significant byte. The count is not cleared when the RMU resets the RCU.
A8-AB	32-bit count of RCU resets (by the RMU) since power on. Byte A8 is the least significant byte. The count is not cleared when the RMU resets the RCU.
AC-AF	Not used.
B0	Constant number (96 decimal) initialized at power on. This constant provides three disk revolutions during which the maximum number of headers is examined before declaring that a requested sector cannot be found (i.e. header not found error). Diagnostics may change this value in order to tighten the sector-finding window.
B1-B3	24-bit test pattern, initialized at power on. When reset, the Microcontroller checks for the initialized pattern. If the pattern is present, the Microcontroller executes a reset sequence. If the pattern is absent, the Microcontroller generates the pattern and initiates the power-on sequence.

A primary function of the scratchpad is to act as a temporary storage area for data moving between the Microcontroller and the PRF or SRF. Typically the Microcontroller accepts data from the PRF and places this data into the scratchpad. The Microcontroller accesses data in the scratchpad to perform an RMU-requested operation and then returns the necessary data to the scratchpad. Data from the scratchpad is then read again by the Microcontroller (via a left bank operation) in order to place the data into either the PRF or the SRF (via a right bank operation). PRF- or SRF-based data is available to be read by the the Z80A on the RMU board.

The Microcontroller provides addresses to the scratchpad for the scratchpad access operation via the &IV0-7 bus as shown in FIGURE 3.2-3. Addresses from the &IV bus are buffered through L68, the Left Bank Address Latch, onto the left bank address bus (&LBA0-7). The bit weights of the addressed data on the &IV bus are reversed at the output of L68. Therefore, IV0, which is the most significant bit on the &IV bus, becomes &LBA7, the most significant bit on the &LBA bus. The &LBA addresses from L68 assert the address pins of scratchpad chips L66 and L67. Data to be stored at the &LBA addresses comes into the scratchpad directly from the Microcontroller's &IV bus. Scratchpad chip L67 handles the high-order data nibble (&IV0-3), and L66 handles the low-order nibble (&IV4-7). Data is read from the scratchpad through the Scratchpad Data Output Buffer (L83) and onto the &IV bus.

Under the control of the 8X305 Microcontroller, data is read from the PRF via the right bank and then loaded into the scratchpad on the left bank. Data is drawn from the PRF through the PRF Data Output Buffer (L84), onto the &IV bus, and then to the Microcontroller. The Microcontroller then transfers the data to the scratchpad on the left bank.

Scratchpad data destined for the PRF or SRF is first read from the scratchpad (into the Microcontroller) via Scratchpad Output Buffer L83 when &LBINPUTDATA is active on the buffer's enabling pins. The Microcontroller then writes the outgoing data from the &IV bus to the PRF via L133, the PRF Data Input Buffer. Scratchpad data destined for the SRF is read by the Microcontroller and then written to the SRF directly from the &IV bus. The Microcontroller provides addresses for the PRF and SRF via its right bank ports. Control of PRF Data Input (L133) and Output (L84) Buffers is also maintained by a right bank I/O command.

Scratchpad read and write operations are controlled by the &LBOUTPUTDATA and &LBINPUTDATA signals generated by Control Signal Decoder L38. During a scratchpad write operation, &LBOUTPUTDATA is active on L64 pin 1. Since L64 pin 1 is low, the &MCLK signal from the Microcontroller controls the output of L64 (pin 2), which clocks the Write Enable (&WE) pin (pin 20) of scratchpad chips L66 and L67 to perform a write operation. The Microcontroller reads scratchpad data via Scratchpad Output Buffer L83 and then passes that data to the SRF or PRF by means of a right bank operation. Since the output enable pin of the scratchpad is always enabled, data is read from the scratchpad onto the &IV bus when the enabling pins of Scratchpad Output Buffer L83 are driven low by the active &LBINPUTDATA signal.

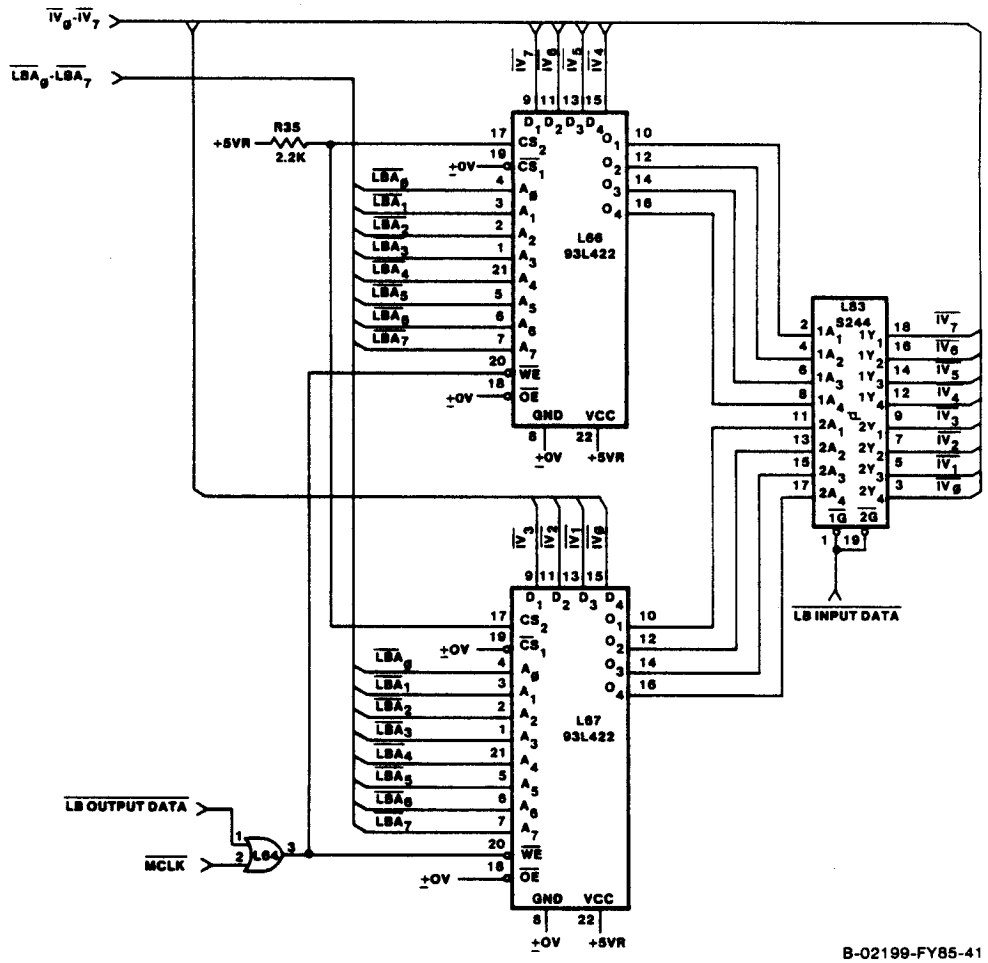


FIGURE 3.2-3
Scratchpad Memory Logic

3.2.4 Right Bank I/O Decoder Operations

The right bank generates I/O port commands which control the primary RCU functions. The right bank controls Status and Parameter Register File access, 4K x 8 Data Buffer access, 50BUS access, Winchester Disk Drive access, the Control Unit Busy interrupt, and reading and clearing the Command Bus Request bit.

The Microcontroller places the addresses of selected right bank ports on the &IV bus via Microcontroller Data Transceiver L69. At the proper time the Microcontroller issues active Right Bank (&RB) and Select Command (&SC) control signals to Control Signal Decoder L38 to select the appropriate right bank port. L38 then issues &RBINPUTDATA from pin 12 and an inverted WC signal from pin 10. The signal from L38 pin 10 drives pin 9 of L26 low, allowing the &MCLK signal to pass through to the output of L26 (pin 10). From L26 pin 10, &MCLK then clocks Right Bank Address Latch L85 to generate right bank addresses &RBA0-7. The bit weights of the &IV bus address on the inputs of L85 are reversed (ie, &IV0, the MSB of the &IV bus, becomes &RBA7, the MSB of the &RBA bus). The &IV address bus is and then issued from L85 as the &RBA address bus. The &RBA0-7 addresses are decoded to create I/O command control signals. There is one primary right bank I/O decoder and seven secondary right bank I/O decoders.

L80, the Right Bank I/O Decoder, decodes addresses &RBA4-6 into seven I/O command groups. Each of these groups enables one of the seven I/O port functions. L80 is always held enabled and, therefore, generates I/O commands when it receives an address on its input pins. Table 3.2-3 lists right bank RCU port addresses, the corresponding command, and the function of that command. In Table 3.2-3 and following tables, "W" indicates that the commands are used for write-only operations, "R" indicates that the commands are used for read-only operations, and "W/R" indicates that the some of the commands in the address range are used for both write and read operations. Each specific right bank command function is broken down in greater detail in Section 3.3

Table 3.2-3: RCU RIGHT BANK I/O DECODER COMMANDS

RCU Port Address (Hex)	I/O Command	Function
00-0B (W)	&STREGFILE	Status Register Functions Strobe. Write status information to the 12-byte Status Register File. Status information is read from the SRF by the RMU.
0C-0F	Not Used	
10-1F (W/R)	&PARREGFILE	Parameter Register File Functions Strobe. Write or read data to or from the 16-byte Parameter Register File. The Parameter Register File passes commands and parameters between the RMU and the RCU.
20 (W/R)	&COMMAND	Command. Write or read the Command Notification (&CMD) bit. The &CMD bit is generated by the RMU to issue a Command Bus Request (&CMDBUSREQ) to the RCU. Writing to 20H clears &CMDBUSREQ. Reading 20H reads the status of the &CMDBUSREQ signal.
21-2F	Not Used	
30-3B (W/R)	&BUFFER	Buffer Memory Functions Strobe. Write or read data to or from the 4K x 8 Data Buffer. The 4K x 8 Data Buffer is used as an interim data storage area during Winchester write or read operations.
34-3F	Not Used	
40-47 (W/R)	&50BUS	50BUS Functions Strobe. Write or read generates 50BUS control signals. These control signals control all 50BUS operations.
48-4F	Not Used	

Table 3.2-3: RCU RIGHT BANK I/O DECODER COMMANDS (cont.)

RCU Port Address (Hex)	I/O Command	Function
50-57 (W/R)	&WINCH	Winchester Functions Strobe. Write or read controls Winchester write, read, and format operations.
58-6F	Not Used	
70 (W)	&INTERRUPT	Interrupt Functions Strobe. Write issues the Control Unit Not Busy (&CUBUSY) signal. &CUBUSY notifies the RMU when the Microcontroller has completed an operation.
71-7F	Not Used	

3.3. RIGHT BANK OPERATIONS

The right bank generates I/O port commands, which control the primary RCU functions. The right bank also controls Status and Parameter Register File access, 4K x 8 Data Buffer access, 50BUS access, Winchester disk drive access, issuing the Control Unit Busy interrupt, and reading or clearing the Command Bus Request bit. There is one primary right bank I/O decoder and seven secondary I/O decoders on the right bank, as shown in FIGURE 3.3-1. L80, the Right Bank I/O Decoder, decodes addresses &RBA4-6 into seven I/O functions. Each of the seven functions enables the respective I/O port's command decoder. Table 3.2-3 shows the relationship between the RCU port addresses and the right bank I/O functions. Each specific right bank command function is broken down in greater detail in the following text.

3.3.1 Status Register File Control I/O Commands

When the Microcontroller selects the Status Register File (locations 00-0BH), Right Bank I/O Decoder L80 issues the active Status Register Functions Strobe (&STREGFILE) signal from pin 7. &STREGFILE first is synchronized with &RBODMCLK (&RBODMCLK is the &MCLK signal synchronized with the Right Bank Data Output signal, &RBOUTPUTDATA) at L81. &STREGFILE then enables Status Register File Decoder L79 by asserting L79 pin 1. When enabled, L79 decodes addresses &RBA2-3 into one of three address spaces: Write SRF Bank One, Two, or Three (WB1, WB2, or WB3). Each of these signals asserts enabling pins on two Status Register File chips. The SRF chips must be enabled in pairs since each chip contains half (ie, four bits) of a complete word. Six 4 x 4 Status Register File chips provide twelve SRF bytes. Table 3.3-1 illustrates the relationship of the address bits to the command, and the function of each command.

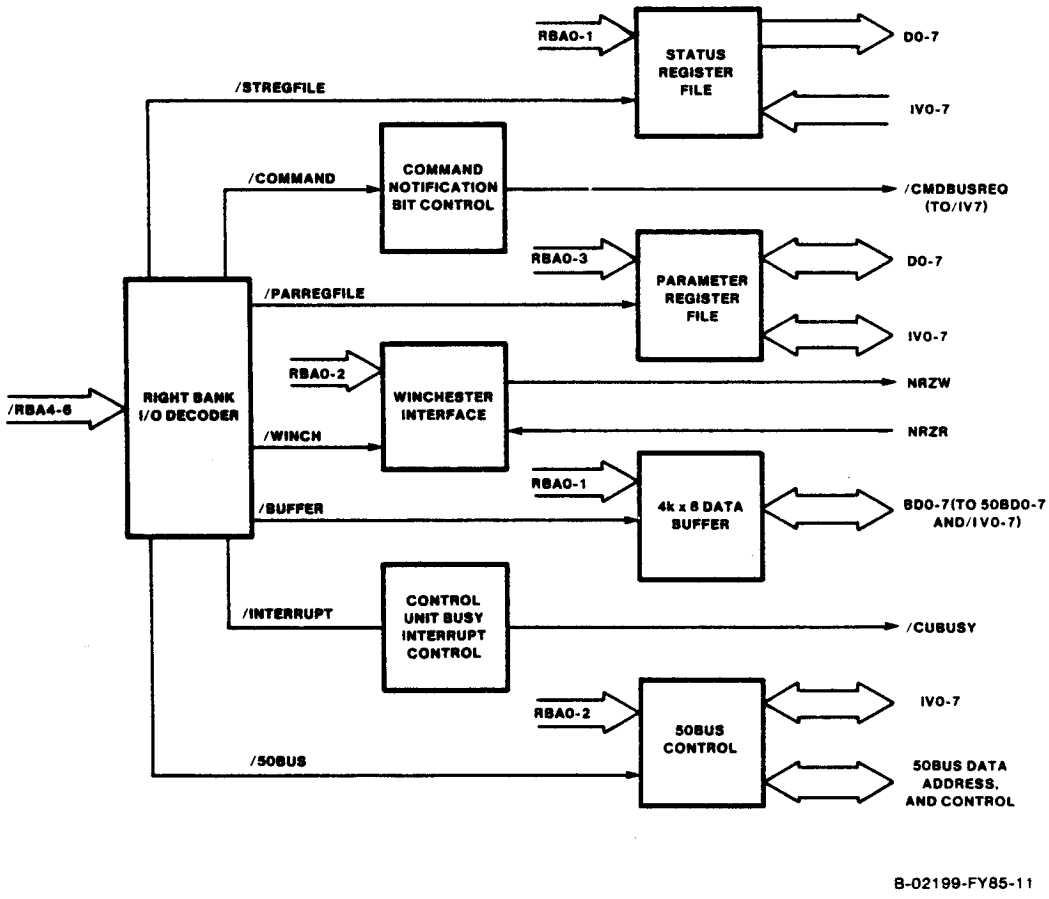


FIGURE 3.3-1
Right Bank Decoding Block Diagram

Table 3.3-1: STATUS REGISTER FILE I/O COMMANDS

RCU Port Address (Hex)	I/O Command	Function
00-03	WB1 (W)	Write enables data to be written into the L151 and L152 SRF chips.
04-07	WB2 (W)	Write enables data to be written into the L134 and L135 SRF chips.
08-0B	WB3 (W)	Write enables data to be written into the L117 and L118 SRF chips.

3.3.2 Parameter Register File Control I/O Commands

When the Microcontroller writes or reads data to or from the Parameter Register File (locations 10-1FH), Right Bank I/O Decoder L80 issues the Parameter Register File Functions Strobe (&PARREGFILE) signal from pin 9. &PARREGFILE is gated through L97 (pin 5 to pin 6) to assert the select pin of Parameter Register File chips L100 and L101. During PRF write operations, &PARREGFILE asserts L64 pin 9, where it is synchronized with &RBODMCLK on pin 10. The output of L64 is gated through L97 to generate a low signal that instructs the PRF to write data by asserting pin 3 of the PRF chips. During read operations, &RBODMCLK is inactive; therefore, pin 10 of L97 is high. Since the Z80A Write Request (&WR) signal is also inactive, pin 9 of L97 is high, which creates a high signal on the PRF's write pin, placing the PRF in the read direction. At the same time, &PARREGFILE asserts L64 pin 6, allowing the Right Bank Input Data (&RBINPUTDATA) signal to enable PRF Data Output Buffer L84 (via L64 pin 5). PRF read and write operations are explained in detail in Section 3.5. Section 3.5 also provides detailed information about Parameter Register File access.

3.3.3 Command Notification Bit Issuance I/O Command

To clear the Command Notification bit (write port 20H), Right Bank I/O Decoder L80 issues the &COMMAND signal from pin 10. After being synchronized with the active &RBODMCLK signal through L26, &COMMAND asserts the clock pin of Command Bus Request Flipflop L25 as shown in FIGURE 3.3-2. When clocked by the synchronized output from L26 pin 4, L25 deactivates the Command Bus Request (&CMDBUSREQ) signal from pin 8. The inactive &CMDBUSREQ signal is sent to the RMU to release the Z80A from its bus-requested state. The Microcontroller cuts off its access to the PRF by disabling PRF Input Data Buffer L133 with the inactive &CMDBUSREQ signal. At the same time, the inactive CMDBUSREQ signal from L25 pin 9 asserts the select pin of PRF Address Multiplexer L102 to select the Z80A-generated bank address bits (&ZBA0-3) for an impending Z80A-controlled PRF read or write operation.

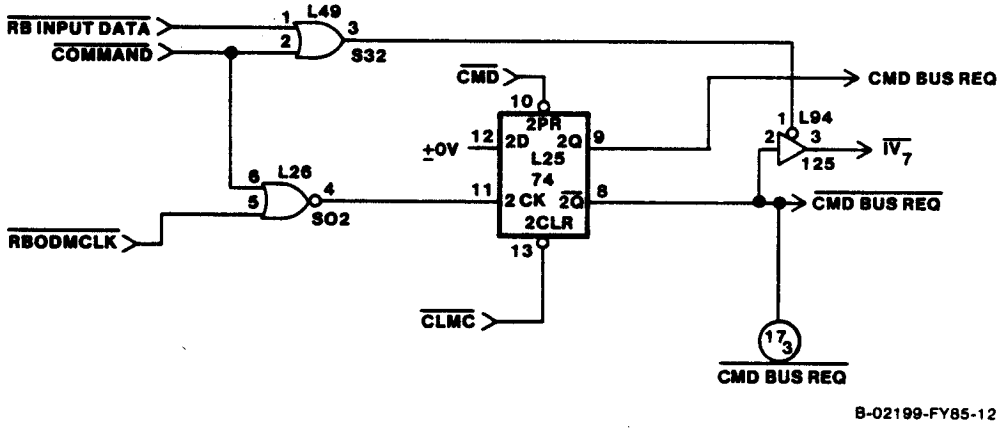


FIGURE 3.3-2
Command Bus Request Bit Control

The Microcontroller reads the status of the CMDBUSREQ signal by reading port 20H. The active &COMMAND signal asserts L94 (via L49), allowing the Microcontroller to read the status of the &CMDBUSREQ signal via the &IV7 bit.

3.3.4 4K x 8 Data Buffer Control I/O Commands

When the Microcontroller commands a 4K x 8 Data Buffer read or write operation (ports 30H-3FH), Right Bank I/O Decoder L80 issues the Buffer Memory Functions Strobe (&BUFFER) signal from pin 11. &BUFFER is synchronized with the active &RBODMCLK signal to generate a low synchronized output from L49 pin 11 which enables 4K x 8 Data Buffer Decoder L77 by asserting pin 1.

When enabled, the 4K x 8 Data Buffer Decoder responds to address bits &RBA0-1 by generating one of four possible I/O commands. Table 3.3-2 shows the relationship of the address bits to the command, and the function of each command. Section 3.4 provides detailed information about 4K x 8 Data Buffer access.

Table 3.3-2: 4K x 8 DATA BUFFER I/O COMMANDS

RCU Port Address (Hex)	I/O Command	Function
30 (W)	Load Low-Order Address	Write loads low-order address bits from the &IV bus through the 4K x 8 Data Buffer Low-Order Address Counter (L125 and L126) onto Buffer Address Bus bits BA0-7.
31 (W)	Load High-Order Address	Write loads high-order address bits from the &IV bus through the 4K x 8 Data Buffer High-Order Address Counter (L143) onto Buffer Address Bus bits BA8-10. Only four bits are needed; therefore, the low-order nibble (&IV4-7) of the IV bus is used.

Table 3.3-2: 4K x 8 DATA BUFFER I/O COMMANDS (cont.)

RCU Port Address (Hex)	I/O Command	Function
32 (W)	READ	Write generates the Data Buffer Read (READ) signal which commands a 4K x 8 Data Buffer read operation. Two consecutive writes to port 32H must be performed to read data. The first write turns on the 4K x 8 Data Buffer Read (&BUFFRD) strobe to the Data Buffer, and the second write turns it off (creating a 200-ns duration READ signal).
33 (W)	WRITE	Write generates the Data Buffer Write (WRITE) signal, which commands a 4K x 8 Data Buffer write operation. Two consecutive writes to port 33H must be performed to write data. The first write turns on the 4K x 8 Data Buffer Write (&BUFFWR) strobe to the Data Buffer, and the second write turns it off (creating a 200-ns duration WRITE signal).
34-3F	Not Used	

3.3.5 50BUS Control I/O Commands

When the Microcontroller initiates a 50BUS operation (ports 40-4FH), Right Bank I/O Decoder L80 issues the 50BUS Functions Strobe (&50BUS) signal from pin 12. The &50BUS signal asserts 50BUS Decoders L78 (1G7) and L114 (1F7) (via L81) to enable a 50BUS read or write operation. L78, the 50BUS Read Control Decoder, decodes addresses &RBA0-1 into one of two I/O commands. L114, the 50BUS Write Control Decoder, decodes addresses &RBA0-2 into one of eight 50BUS control commands.

When &RDINPUTDATA is active at L81 pin 9, the &50BUS signal from the Right Bank I/O Decoder is passed through L81 to enable L78, the 50BUS Read Control Decoder. L78 decodes addresses &RBA0-1 into one of two commands. (Table 3.3-3 illustrates the relationship of the address bits to the command, and the function of each command.) When &RBODMCLK is active at L81 pin 12, the &50BUS signal from the Right Bank I/O Decoder is synchronized through L81 to enable L114, the 50BUS Write Control Decoder. L114 decodes addresses &RBA0-2 into one of eight commands. Section 3.4 provides a detailed explanation of the 50BUS Control I/O command functions.

Table 3.3-3: 50BUS I/O COMMANDS

RCU Port Address (Hex)	I/O Command	Function
40 (R)	&RP40H	Read data from the 50BUS data bus onto the &IV data bus.
40 (W)	&SLAVESLCT	Select a slave on the 50BUS. The relationship of the data on the &IV bus to the device selected is shown below. &IV0-&IV7 — Device Selected 01H — 0 - Master memory 02H — 1 - Serial data link 04H — 2 - FDC DMA 08H — 3 - IWS 10H — 4 - IWS 20H — 5 - IWS 40H — 6 - IWS 80H — 7 - IWISE
41 (R)	Unnamed	Read the status of the 50BUS Acknowledge (&50BBUSAK) and 50BUS DMA Request (&50BDRQ) signals from the 50BUS. If &IV7 (the LSB) is set to 1, &50BBUSAK is active; if &IV6 is set to 1, &50BDRQ is active.

Table 3.3-3: 50BUS I/O COMMANDS (cont.)

RCU Port Address (Hex)	I/O Command	Function
41 (W)	&WP41H	Write to load low-order address from the &IV bus onto the 50BUS address bus.
42 (W)	&ADDHIGH	Write to load high-order address from the &IV bus onto the 50BUS address bus.
43 (W)	&WP43H	Write data onto the 50BUS data bus.
44 (W)	&DATA ENABLE	Write selects data path to the 50BUS as follows: IV7 = 1 - Microcontroller data is sent to 50BUS IV6 = 1 - Data from 4K x 8 Data Buffer is sent to the 50BUS
		NOTE: Only one can be selected at a time.
45 (W)	&CNTRL	Write generates both 50BUS Bus Request (&50BBUSREQ) and 50BUS read/write signals as follows: IV1 = 0 - Write operation IV1 = 1 - Read operation IV2 = 0 - Turn off &50BBUSREQ IV2 = 1 - Turn on &50BBUSREQ

Table 3.3-3: 50BUS I/O COMMANDS (cont.)

RCU Port Address (Hex)	I/O Command	Function
46 (W)	&SPFUNC	Write generates the following 50BUS signals: Status 50BUS (STATUS50B) IV4 = 1 - Turn on status IV4 = 0 - Turn off status Reset 50BUS Device (RESET50B) IV3 = 1 - Turn on reset IV3 = 0 - Turn off reset Terminal Count (TC) IV5 = 1 - Turn on terminal count IV5 = 0 - Turn off terminal count
47 (W)	&REQ	Write generates the 50BUS Byte Request (&50BREQ) signal.
47-4F	Not Used	

3.3.6 Winchester Control I/O Commands

When the Microcontroller commands a Winchester read or write operation (ports 50-57H), Right Bank I/O Decoder L80 issues the Winchester Functions Strobe (&WINCH) signal from pin 13. &WINCH, after being gated through L35, asserts the Winchester Read and Write Decoders (L78 and L62 (2B4 & 2D4)). During Winchester write operations, the Right Bank Output Data Master Clock (&RBODMCLK) signal is active on L35 pin 12, synchronizing the &WINCH signal through L35 to enable Winchester Write Decoder L62. During Winchester read operations, &RBINPUTDATA is active on L35 pin 5, allowing the &WINCH signal through L35 to enable Winchester Read Decoder L78.

When enabled, Winchester Write Decoder L62 responds to address bits &RBA0-2 by generating one of eight possible I/O write commands. Winchester Read Decoder L78, when enabled, responds to address bits &RBA0-1 by generating one of three possible I/O read commands. (Table 3.3-4 illustrates the relationship of the address bits to the command, and the general function of each command.) Chapter 6 provides a detailed explanation of the Winchester I/O command functions.

Table 3.3-4: WINCHESTER I/O COMMANDS

RCU Port Address (Hex)	I/O Command	Function
50 (R)	&READDSKDATA	Read a byte of data from the Winchester.
50 (W)	&DSKWRITEDATA	Write a byte of data to the Winchester.
51 (R)	&READDSKSTATUS	Read the Winchester status byte. IV7 = 1 - Track 0 has been detected. IV6 = 1 - A write fault has been detected. IV5 = 1 - The Winchester is ready to perform an operation. IV4 = 1 - A command seek operation has been completed. IV3 = 1 - The Winchester has been selected for an operation. IV2 - Unused IV1 - Unused IV0 = 1 - An index mark has been detected (ie, located at the beginning of a track).

Table 3.3-4: WINCHESTER I/O COMMANDS (cont.)

RCU Port Address (Hex)	I/O Command	Function
51 (W)	&WRITEDRPRG	Program the Winchester. Write a control byte to the Winchester and controller. IV7 = 1 - Select a write operation. IV6 = 1 - Select a read operation. IV5 = 1 - Select reduced write current for write precompensation. IV4 = 1 - Select the direction of head movement. IV3 = 1 - Select the drive for a read, write, or seek operation. IV2 - 1 - Select head 2 for read or write operation. IV1 = 1 - Select head 1 for read or write operation. IV0 = 1 - Select head 0 for read or write operation.

Table 3.3-4: WINCHESTER I/O COMMANDS (cont.)

RCU Port Address (Hex)	I/O Command	Function
52 (R)	&READCNTRLSTATUS	Read Winchester controller status. IV7-IV4 - Four switched bits that define Winchester characteristics. IV3 = 1 - Parallel to Serial Converter L141 has sent a byte of data to the Winchester and requires another byte for serialization. IV2 = 1 - Serial to Parallel Converter L107 has assembled a byte of data and requires the host to accept the data byte. IV1 = 1 - The minimum amount of zeros (8 bytes) needed prior to address mark detection has been encountered. IV0 = 1 - An address mark has been detected. The header or data field should follow.

Table 3.3-4: WINCHESTER I/O COMMANDS (cont.)

RCU Port Address (Hex)	I/O Command	Function
52 (W)	&WRITELOGICCNTRL	Write Winchester control signals. IV7, IV2, IV1 - Unused. IV6 = 1 - Enable ECC time. IV5 = 1 - Generate reset. IV4 = 1 - Enable skip (for address mark generation). IV3 = 1 - Enable write gate. IV0 = 1 - Enable write precompensation.
53 (W)	&WRITELOTSC	Write the low-order track step counter with eight bits (&IV7-&IV0).
54 (W)	&WRITEHOTSC	Write the high-order track step counter with four bits (&IV7-&IV4).
55 (W)	&LOADDSKWD	Write to clear byte request from Winchester controller (data irrelevant).
56 (W)	&WP56H	Write to enable or disable the Microcontroller Halt circuit.
57 (W)	Unnamed	Enable or disable data movement. IV7 = 1 - Enable data from 4K x 8 Data Buffer to the Winchester.

Table 3.3-4: WINCHESTER I/O COMMANDS (cont.)

RCU Port Address (Hex)	I/O Command	Function
		IV7 = 0 - Disable data from 4K x 8 Data Buffer to the Winchester. IV6 = 1 - Enable Winchester data to 4K x 8 Data Buffer. IV6 = 0 - Disable Winchester data to 4K x 8 Data Buffer. IV5 = 1 - Enable 50BUS data to 4K x 8 Data Buffer. IV5 = 0 - Disable 50BUS data to 4K x 8 Data Buffer.
58-5F	Not Used	

3.3.7 Interrupt Issuance I/O Command

When the Microcontroller issues an interrupt (port 70H), Right Bank I/O Decoder L80 issues the Interrupt Functions Strobe (&INTERRUPT) signal from pin 15. &INTERRUPT, together with the active &RBODMCLK signal (&RBODMCLK is the &MCLK signal synchronized with the &RBOUTPUTDATA signal), asserts L35 (2E5). Together these signals generate a low output from L35 pin 8 which, via L65, fires Control Unit Not Busy 1-Shot L34 by asserting pin 11. L34's firing issues the Control Unit Not Busy (&CUBUSY) pulse to inform the RMU that the RCU has completed an operation and is no longer busy. When the Microcontroller is hung in a Winchester read or write operation (see Section 3.5.7), a signal from the carry pin of the Dead Man Timer can also assert L34 via L65 to generate the &CUBUSY signal. When interrupted, the Z80A performs interrupt service routines which determine the cause of the active &CUBUSY signal by examining various status bits in the Status Register File.

3.4 4K x 8 DATA BUFFER and 50BUS INTERFACE

3.4.1 4K x 8 Data Buffer

The 4K x 8 Data Buffer on the RCU board serves as a temporary storage area for data passing between the RCU and the Winchester or floppy disk drive (see FIGURE 3.4-1). Two 2K x 8 Static RAM chips (L110 and L109 (1H7 & 1J7)) comprise the 4K x 8 Data Buffer (as shown in FIGURE 3.4-2). Therefore, if data moves between one slave's memory and another slave's memory, the data passes through the 4K x 8 Data Buffer. In addition, if data moves between the RCU and any slave, the data passes through the 4K x 8 Data Buffer.

Addresses are provided to the 4K x 8 Data Buffer by the 4K x 8 Data Buffer Address Counters (L125, L126, and L143 (1H/K8)). The Microcontroller generates the initial address and sends it to the data buffer via the &IV bus. The 11-bit address is then sent into the 4K x 8 Data Buffer via the BA0-10 address bus when the address counter load pins are asserted by signals from the 4K x 8 Data Buffer Decoder (L77). The address is then incremented by either an active &BUFFRD or &BUFFWR signal issued via the L76 flipflops.

Data moves to and from the 4K x 8 Data Buffer via the BD0-7 data bus. Data is moved between the BD0-7 bus and the 50BD0-7 (50BUS Data) bus through the 50BD0-7 to BD0-7 Bus Data Buffer (L127) and the BD0-7 to 50BD0-7 Bus Data Latch (L28). Data moves between the BD0-7 bus and the Winchester via the BD0-7 to WBD0-7 Bus Data Latch (L142) and the Winchester to BD0-7 Bus Data Buffer (L108).

The 4K x 8 Data Buffer Bank Select Flipflop (L93, 1Q output) selects and synchronizes (with the Master Clock, MCLK) the bank select signal which chooses either L109 or L110 for the 4K x 8 Data Buffer read or write operation. The &IV4 signal is forwarded through L143 to the input of L93 to specify L93's output. L109 is selected for the read or write operation if L93 generates an active signal from pin 6 (ie, input &IV4 is inactive). L110 is selected for the read or write operation if L93 generates an active signal from pin 5 (ie, input &IV4 is active).

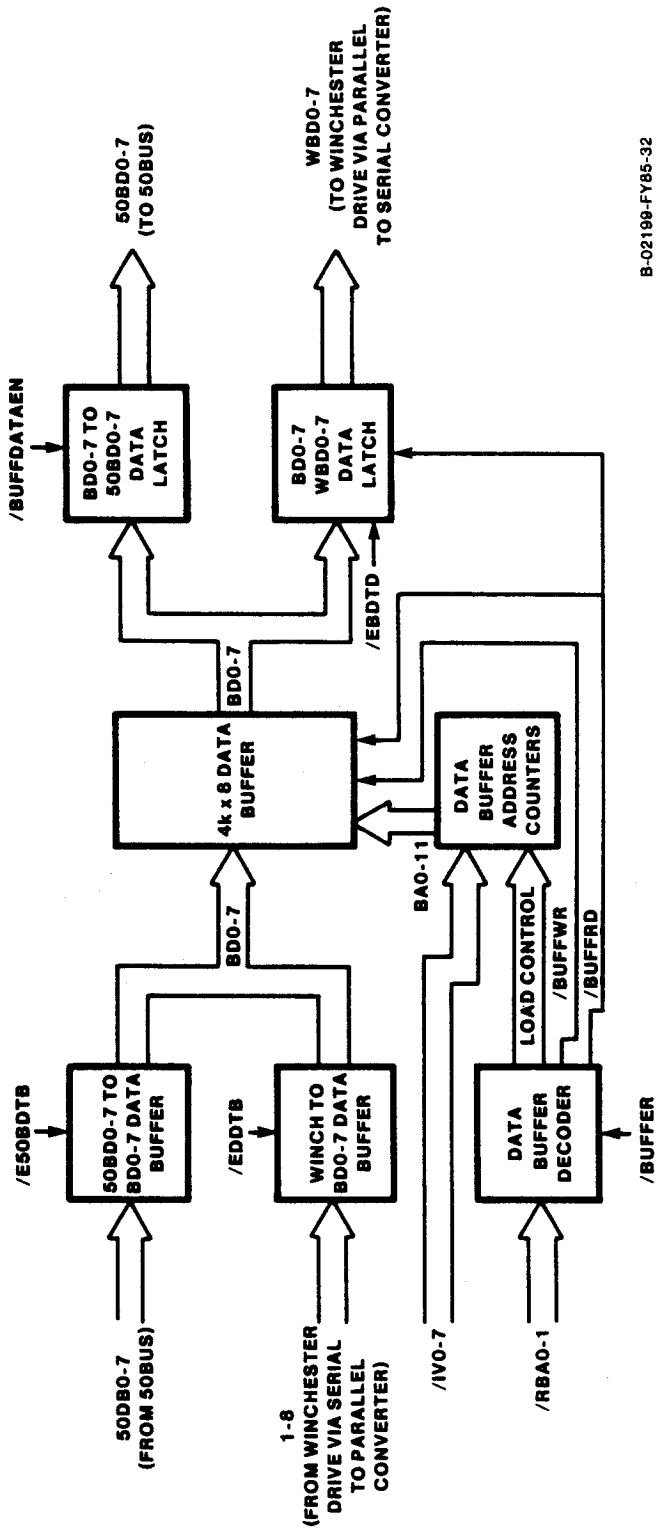


FIGURE 3.4-1
4K x 8 Data Buffer Block Diagram

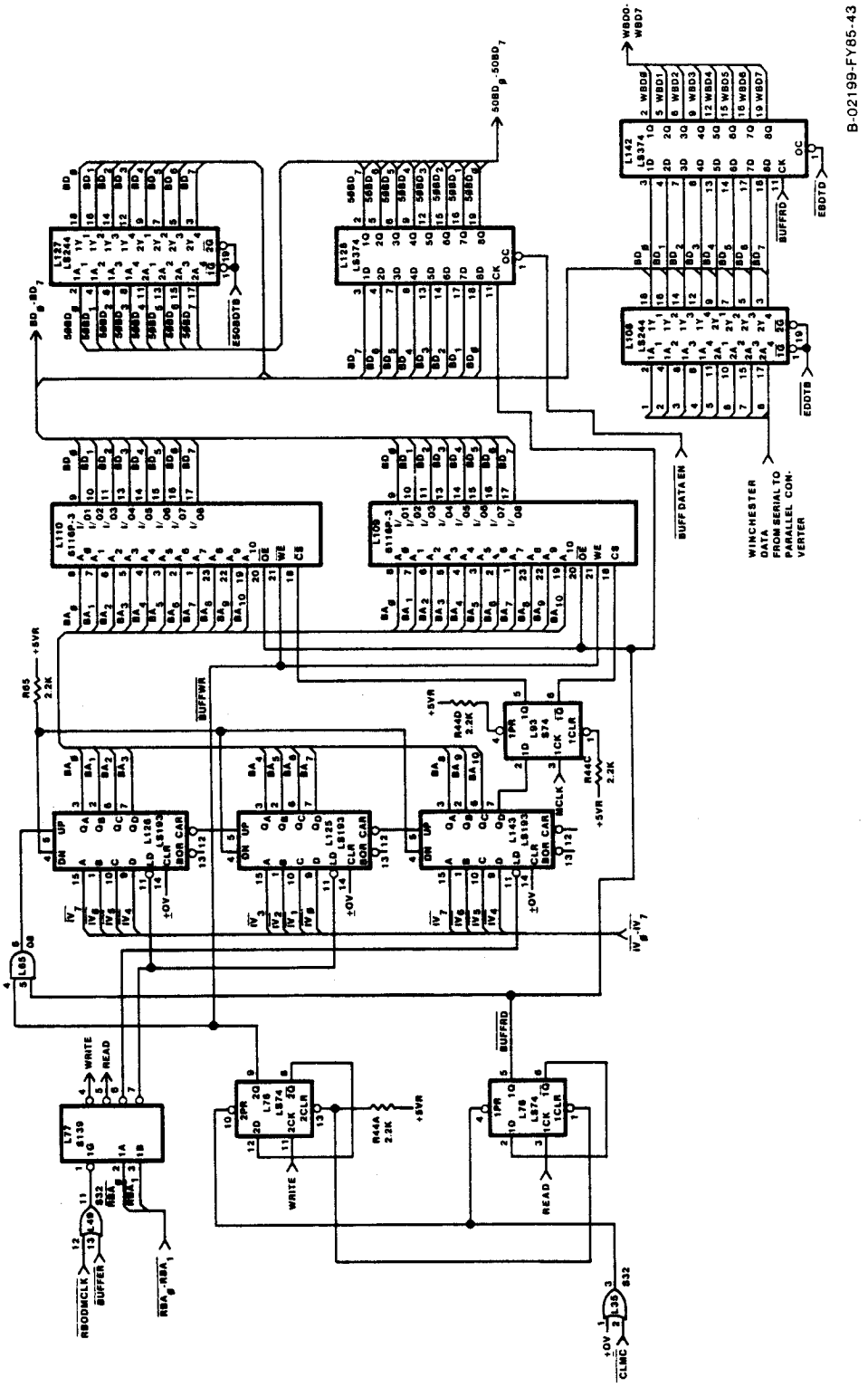


FIGURE 3.4-2
4K x 8 Data Buffer Access Logic

3.4.2 Data Buffer I/O Command Functions

When the Microcontroller commands a 4K x 8 Data Buffer read or write operation (ie, it issues 30-3BH), Right Bank I/O Decoder L80 issues the Buffer Memory Functions Strobe (&BUFFER) signal from pin 11. &BUFFER is synchronized with the active &RBODMCLK (Right Bank Output Data Synchronized with Master Clock) signal to generate a low synchronized output from L49 pin 11 which enables 4K x 8 Data Buffer Decoder L77 by asserting pin 1. When enabled, L77 responds to address bits &RBA0-1 by generating one of four possible I/O commands (see Table 3.3-2).

In response to the 30H write command, 4K x 8 Data Buffer Decoder L77 issues a signal from pin 7 which asserts the load pins of 4K x 8 Data Buffer Low-Order Address Counters L125 and L126 to pass the initial address from the &IV bus onto the &BA0-7 bus outputs. The address counters are incremented to provide additional addresses by the active 4K x 8 Data Buffer Read (&BUFFRD) or 4K x 8 Data Buffer Write (&BUFFWR) signal asserting L126 pin 5 via L65. &BUFFWR and &BUFFRD are latched versions of the active Data Buffer Write (&WRITE) and Data Buffer Read (&READ) signals issued from L77 pins 4 and 5.

In response to the 31H write command, L77 issues a signal from pin 6 that asserts the load pin of 4K x 8 Data Buffer High-Order Address Counter L143 to pass the initial address from the &IV bus onto the &BA8-10 bus outputs. The High-Order Address Counter is incremented to provide additional addresses when the carry signal from Low-Order Address Counter L125 asserts pin 5 of L143.

In response to the 32H write command, 4K x 8 Data Buffer Decoder L77 issues a signal from pin 5 that initiates a data buffer read operation. The Microcontroller actually generates the read strobe to the data buffer by writing to port 32H. Two consecutive port 32H writes are issued to perform a read operation: the first turns the Read signal on, and the second turns it off. This procedure results in an active &BUFFRD strobe of 200-ns duration (200-ns is the lenght of one instruction cycle for the 8X305 Microcontroller). The Read signal from L77 generates the &BUFFRD signal directly through Data Buffer Read Control Flipflop L76 (2H3). READ asserts L76's clock input to latch the &BUFFRD signal active from pin 5. &BUFFRD is turned off 200 ns later when the READ signal is activated again on the clock input of L76.