VARIAN DATA 520/i SYSTEM REFERENCE MANUAL

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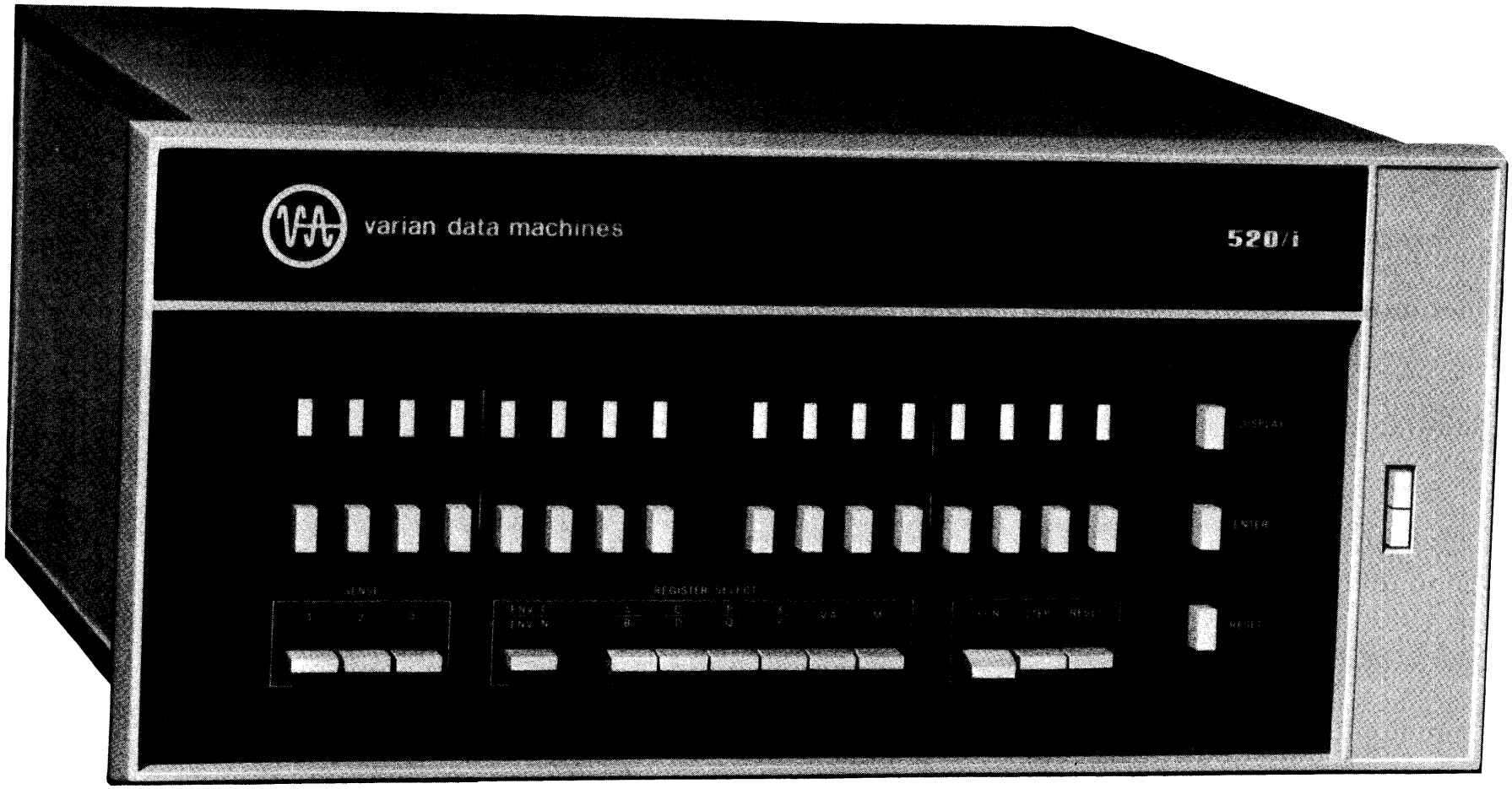


Figure 1-1. Varian Data 520/i Computer

1.1 GENERAL

The Varian Data 520/i (Figure 1-1) is a system-oriented, general-purpose digital computer designed for use as the controlling element in data acquisition, process control, communications and other real-time applications. The 520/i features powerful computing ability, easy interfacing, integrated circuit reliability, compact size and low cost.

A versatile register structure offers two complete processing capabilities. This system allows the servicing of input/output operations without affecting the main program, or allows two programs to be processed concurrently; one in the foreground using I/O and the other in the background.

General characteristics of the 520/i are:

Variable operand precision of 8, 16, 24 or 32 bits.
Two hardware register sets (environments) including 32-bit accumulators, 16-bit program counters and 16-bit index registers.
Two's complement arithmetic.
Direct addressing to 4,096 bytes.
Indirect and indexed addressing.
Comprehensive instruction set.
Memory expandable from 4,096 bytes (8 bits each) to 32,768 bytes.
1.5- microsecond memory cycle time.
Addressing reference to 8, 16, 24 or 32-bit level.
High-speed direct input/output channel.
Four priority interrupts included in the standard machine.
Optional direct memory access.

1.2 SPECIFICATIONS

Specifications	Characteristics
Type	General-purpose digital, designed for on-line data systems.
Memory	Magnetic core, 8 bits, 1.5 microseconds full cycle, 500 nanoseconds access time, 4096 bytes minimum, expandable to 32,768 bytes.
Arithmetic	Parallel, binary, fixed point, 2's complement.
Operand Word Length	8, 16, 24 or 32 bits.
Addressing	Direct addressing to 4096 bytes. Index with X register in hardware, does not add to execution time. Multi-level indirect addressing.
Instructions	Over 50 basic instructions with over 500 useful register to register operations.

Number	Type
1	Load
1	Store
2	Arithmetic
3	Logical
14	Skip
3	Branch
4	Input/Output

Specifications	Characteristics
	Number / **Type** 8 — Register Change 8 — Logical Shift 16 — Control
Registers available to the programmer	P Register: Program counter in current environment, 16 bits X Register: Index register in current environment, 16 bits. A Register: Most-significant accumulator in current environment, 16 bits. C Register: Least-significant accumulator in current environment, 16 bits. OPC Register: Operand precision (word length) register in current environment, 2 bits. OVC Register: Overflow register in current environment, 1 bit. Q Register: Program counter in noncurrent environment, 16 bits. Y Register: Index register in noncurrent environment, 16 bits. B Register: Most-significant accumulator in noncurrent environment, 16 bits. D Register: Least-significant accumulator in noncurrent environment, 16 bits. OPN Register: Operand precision register in noncurrent environment, 2 bits. OVN Register: Overflow register in noncurrent environment, 1 bit. Z Register: Pseudo-register containing only ZEROs. F Register: I/O channel register in optional peripheral controller, 16 bits.
Registers not available to the programmer	I Register: Instruction register, 8 bits. S Register: Temporary operand storage register, 8 bits.

Specifications	Characteristics
	MB Register: Memory buffer, temporary operand storage register, 8 bits.
	MA Register: Memory address register, 15 bits.
Features	Dual environment: two sets of hardware registers (program counter, index register, accumulator, control registers) eliminate the necessity to save and restore register contents when transferring between program routines in different environments.
INPUT/OUTPUT	
Processor	Programmed data transfer: single word to/from accumulator External control lines External sense lines
Automatic Data Transfer	Direct-memory-access facility with data rates up to 666,000 bytes per second.
Priority Interrupts	Eleven interrupts are standard with group enable/disable and individual arm/disarm.
Console	Display and data entry switches for all operational registers and memory, single step control.
PHYSICAL	
Dimensions	Main frame: 8-3/4 inches high, 19 inches wide, 20-3/4 inches deep.
Weight	Main frame with internal power supply: 48 pounds.
Power	115 vac ± 10 vac, 60 Hz, 2-6 amps. Power supplies are regulated. Additional regulation is not required with normal commercial power sources. Conversion for European power available at added cost.
Expansion	Main frame contains provisions and space for 8,192 bytes of memory, teletype controller, paper tape system controller and 16-bit I/O channel.
Installation	Mounts in standard 19-inch cabinet. No air conditioning, sub-flooring, special wiring or site preparation are required.
Environment	0°C to 50°C, 0 to 90% relative humidity.
Mainframe	Integrated circuit, 8-MHz clock, logic levels are 0 vdc false (ZERO) and +5 vdc true (ONE).

1.3 OPTIONS

Available hardware options for the 520/i are grouped into main frame options and peripheral options. Main frame options include:

a. Teletype controller.
b. Punched-tape system controller.
c. Peripheral adapter for program-controlled 16-bit I/O channel.
d. Memory parity.

Peripheral options include:

a. Expansion chassis.
b. Magnetic tape controller (seven and nine track).
c. Rotating memory controller.
d. Card reader controller.
e. Digital plotter controller.
f. Punched-tape system controller.

1.3.1 Teletype Controller

This main-frame option controls the transfer of commands and data between the central processor and a model ASR-33 teletypewriter. One teletype can be accommodated by this controller. The first teletype controller comprises 27 integrated circuit chips and wiring that are part of the central processor module. This option is installed only at the factory.

1.3.2 Punched-Tape-System Controller

This main-frame option controls the transfer of commands and data between the central processor and a high-speed punched-tape system comprising a Tally punch (60 cps) and a Remex reader (300 cps). One punched-tape system can be accommodated by this controller.

1.3.3 Memory Parity

This main-frame option generates even-bit parity for all words stored in the memory and checks for correct parity in all words accessed from memory. If a parity error is detected, an interrupt to memory location 004 is generated. The parity-error interrupt has a fixed priority (hard wired) one level higher than external interrupt line 0. This option may be used with only the nine-bit memory modules.

1.3.4 Peripheral Adapter

This main-frame option enables the 520/i central processor to communicate with external devices requiring a 16-bit interface. As many as 31 devices can be controlled through the peripheral adapter.

The following standard peripheral options may be used with the peripheral adapter:

a.	620/i-23	Card reader, 200 cpm.
b.	620/i-30	Magnetic tape, seven track (with 620/i-30A or 620/i-30B; may be used with 620/i-30C at 556 bpi only).
c.	620/i-31	Magnetic tape, nine track (with 620/i-31A or 620/i-31B).
d.	620/i-40	Disc memory, 32,768 words, 30 kHz.
e.	620/i-41	Disc memory, 65,536 words, 30 kHz.
f;	620/i-42	Disc memory, 131,072 words, 30 kHz.
g.	620/i-43	Disc controller, 262,144 words, 30 kHz.
h.	620/i-50	Paper-tape punch, 60 Hz.
i.	620/i-51	Paper-tape reader, 300 Hz.
j.	620/i-52	Punched-tape system, 60 Hz punch, 300 Hz reader

1.3.5 Expansion Chassis

The expansion chassis provides the required frame and mounting hardware for optional memory modules (up to four per expansion frame with a total of six external memory modules possible) or peripheral controllers. Space is provided in each chassis for optional expansion power supplies.

1.3.6 Magnetic Tape Controller

A master controller for up to four tape transports. This option controls seven- or nine-track transports and includes a data assembly/disassembly register. Transports are available with recording densities of 200,556 and 800 bpi at a speed of 25 ips. This option requires the 520/i peripheral adapter.

1.3.7 Rotating Memory Controller

This option provides control and data interface between the 520/i peripheral adapter and a 30 kHz fixed-head magnetic disc. Disc packs are available with storage capacities of 32,768, 65,536, 131,072 and 262,144 words (16 or 18 bits per word).

1.3.8 Card Reader Controller

This option provides control and data interface between the 510/i peripheral adapter and a 1000 cpm reader.

1.3.9 Digital Plotter Controller

This option provides control and data interface between the 520/i peripheral adapter and a Cal Comp 565 digital plotter with a recording rate of 300 steps per second.

1.3.10 Punched Tape System Controller

This option provides control and data interface between the 520/i peripheral adapter and a punched tape system that may include a 60 cps punch and 300 cps reader.

1.4 PROGRAMMING SYSTEM

A comprehensive package of operational programs is available with the Varian Data 520/i. These include a symbolic assembly system, debugging aids, library of mathematical subroutines and maintenance test package. Each of these groups is described in the following paragraphs.

1.4.1 Symbolic Assembly System

The 520/i assembly system consists of an assembly program and a symbolic language that assists in program preparation. The assembly program interprets instructions written in the symbolic language to produce object programs suitable for use by the 520/i. The assembly system is designed to operate in a minimum hardware system consisting of an ASR-33 teletype and a 520/i with 4,096 bytes of memory and a teletype controller option.

1.4.2 Debugging Aids

The debugging package consists of basic and general debugging programs that assist the programmer in displaying and altering memory and hardware registers, punching selected areas of memory, and branching to selected user programs.

1.4.3 Subroutine Library

The comprehensive subroutine library includes the most commonly used subroutines needed in systems applications. The library includes routines for number conversions, fixed and floating-point arithmetic, logarithmic, trigonometric and exponential functions, and for operating standard peripheral equipment.

1.4.4 Test Programs

The 520/i test package is designed to check instructions, memory and input/output devices, and to help isolate errors. Maintenance tests can be used in either the preventive or corrective mode of operation. In the preventive mode, the system is checked before operation. If a malfunction occurs, the test program indicates the error and provides information that helps determine the trouble. The corrective mode is used when a malfunction is known to exist but the trouble is not decisively known. Proper application of the test programs can reduce repair time to minutes. The test programs are assembled in a modular package that can be easily expanded to accommodate special equipment.

1.5 APPLICATIONS

The Varian Data 520/i computer is ideally suited to such systems applications as process control, data storage and retrieval, data buffering, input/output media conversion, data compression, and other broad uses.

As a self-contained tool, the 520/i finds application in research and development, instruction and training, and as a variable precision calculator.

1.6 DOCUMENTATION

Documentation supplied with the 520/i computer includes drawings and manuals for use and maintenance of the equipment, and software programs with written descriptions of operation and typical use.

Manuals available for the Varian Data 520/i include:

a. System reference manual.
b. Programming reference manual.
c. System installation and integration manual.

Programs available for the 520/i include:

a. Basic bootstrap program.
b. Binary loader program.
c. Symbolic assembler program.
d. Basic debugging aid program.
e. General debugging aid program.
f. Source tape correction program.
g. Maintenance test programs.
h. Mathematical subroutines.
i. Peripheral device service programs.

2.1 GENERAL

The 520/i main frame includes a basic chassis with modular front panel, circuit cards and power supply. Overall views of the main frame, with dimensions, are shown in Figure 2-1. Detailed drawings showing construction of the front panel, a typical circuit card module and the power supply are shown in Figures 2-2 through 2-4.

2.2 CONTROLS AND INDICATORS

The front-panel controls and indicators of the 520/i are shown in Figure 2-5. A description of these switches and displays is given in the following paragraphs.

2.2.1 Data Display Indicators

The 16 binary indicators that constitute the data display are switched between several sources. It is possible to display contents of memory, memory address register, accumulators, index registers and program counters.

2.2.2 Data Entry Switches

Sixteen binary switches that load an associated register (switch register) for data entry to the memory or one of the operational registers.

2.2.3 RESET Display Switch

The RESET display switch clears the switch register to all zeros.

2.2.4 Overflow Indicators 01 and 02

These indicators reflect the status of the arithmetic overflow flip-flops in each environment.

2.2.5 RUN Indicator and Switch

The RUN indicator illuminates when the machine is actively executing an instruction. The RUN switch starts the machine executing from the current program counter location.

2.2.6 STEP Indicator and Switch

The STEP indicator illuminates when the machine is not running and indicates that front-panel controls and indicators are active and may be used for register display and entry. The STEP switch causes the machine to leave the run condition. It is used to single step instructions for program or hardware check.

2.2.7 RESET Switch

Momentary activation of the RESET switch returns all control flip-flops in the machine to an initialized condition. The environmental status is returned to interruptable (environment 1). The operand precisions are set to eight bits.

2.2.8 REGISTER SELECT Switches

The seven REGISTER SELECT switches determine which register is being actively displayed or which register will accept manual entry from the switch register.

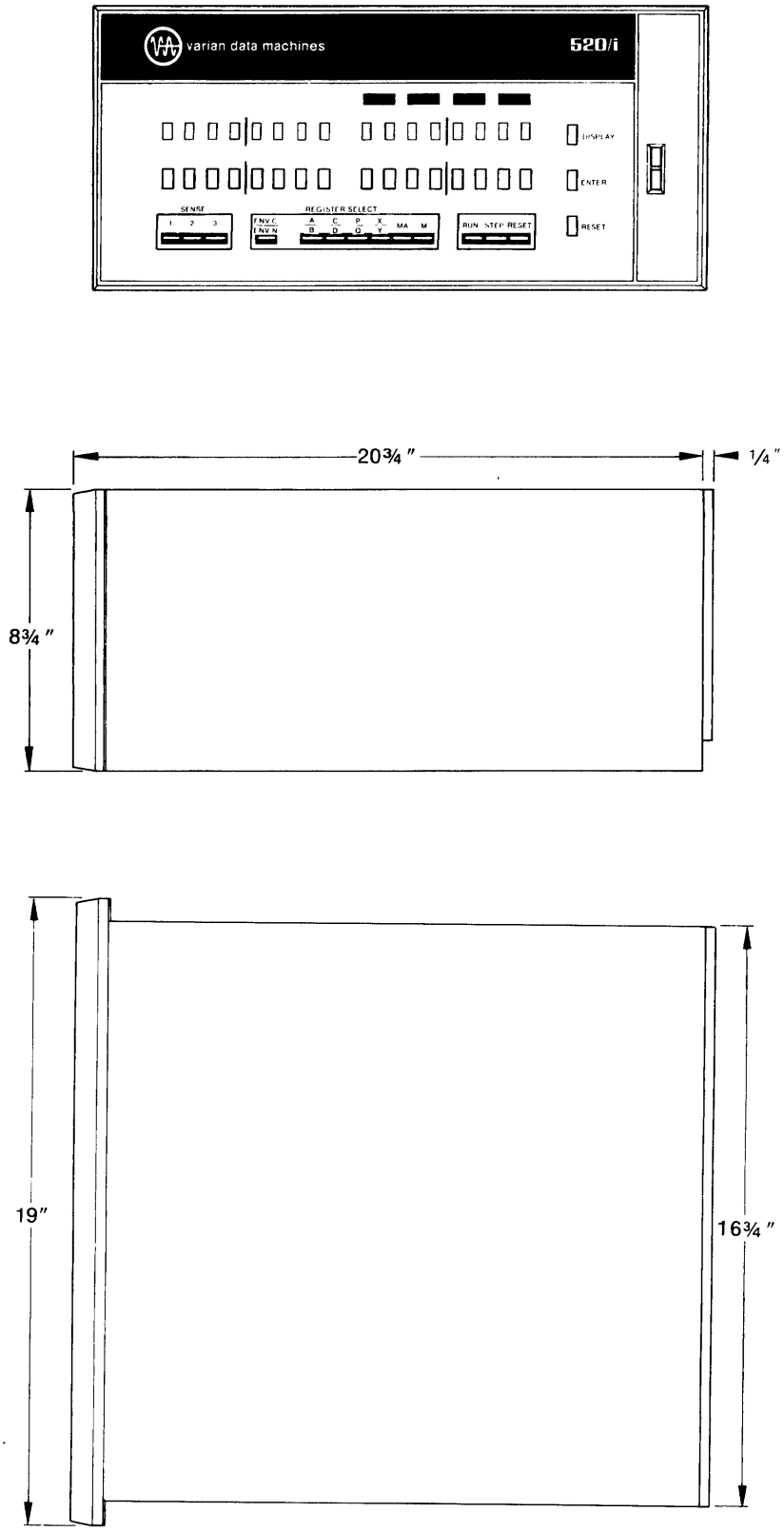


Figure 2-1. 520/i Outline Drawing

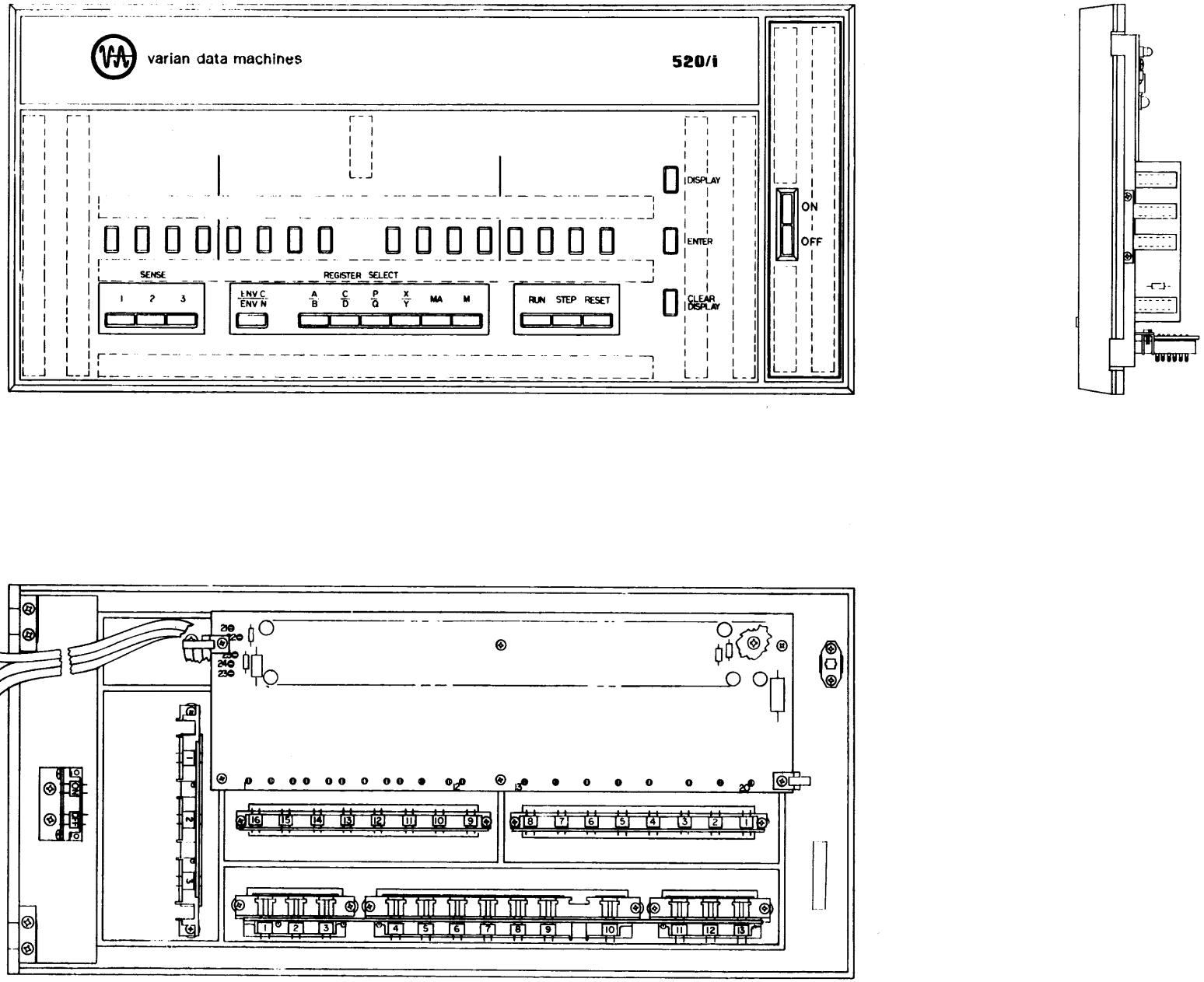


Figure 2-2. 520/i Front-Panel Construction

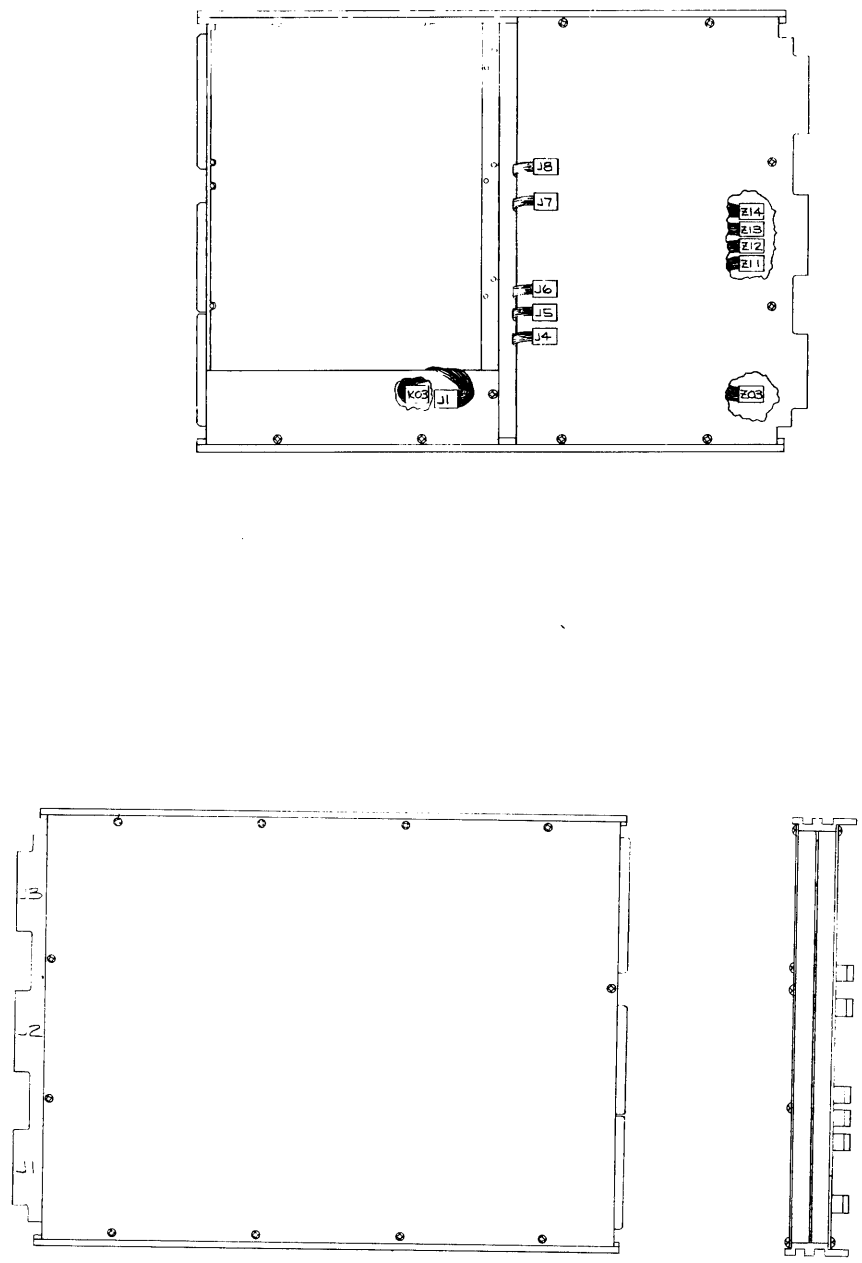


Figure 2-3. Typical Module Construction 520/i Circuit Cards

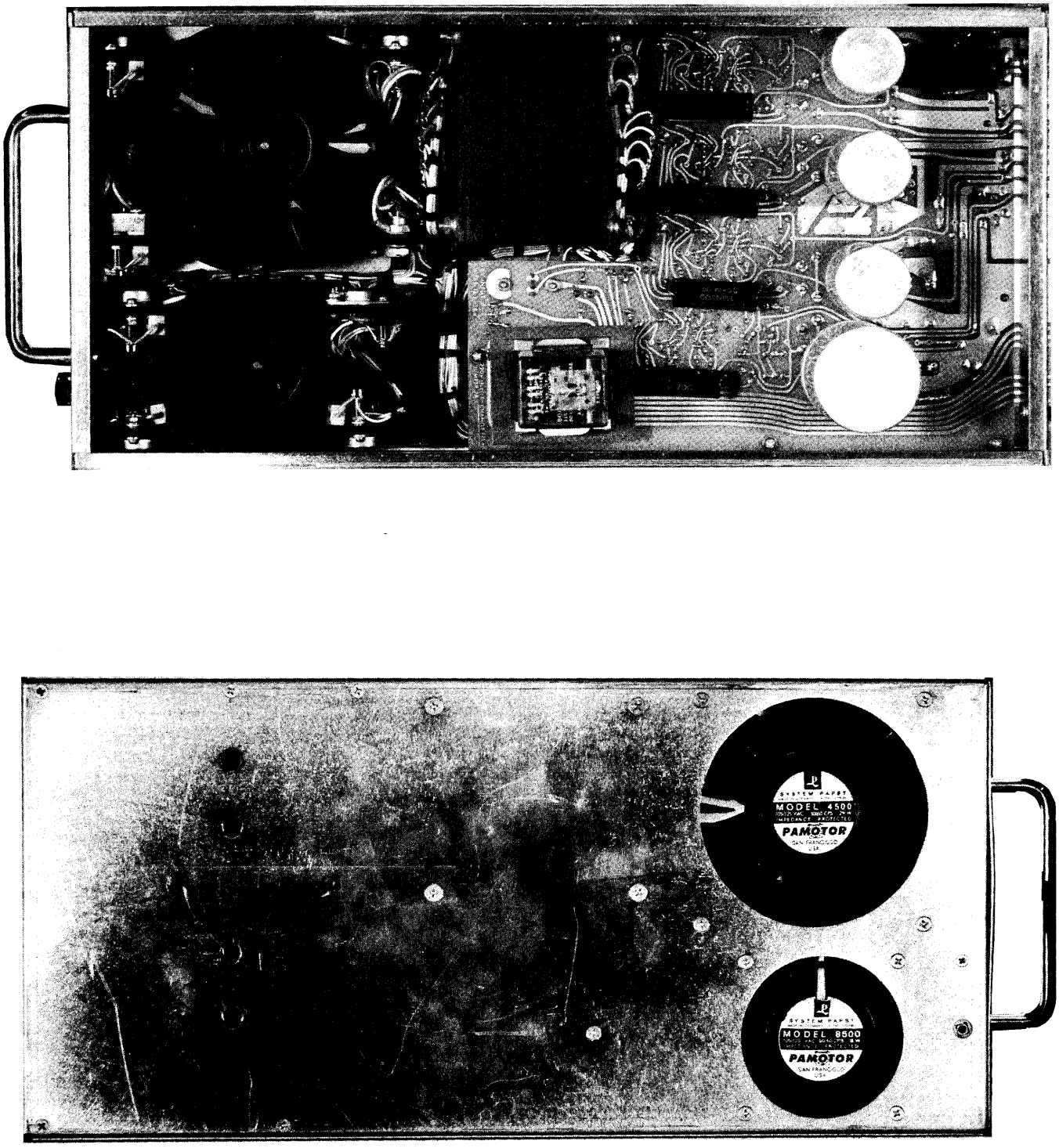


Figure 2-4. 520/i Power Supply Construction

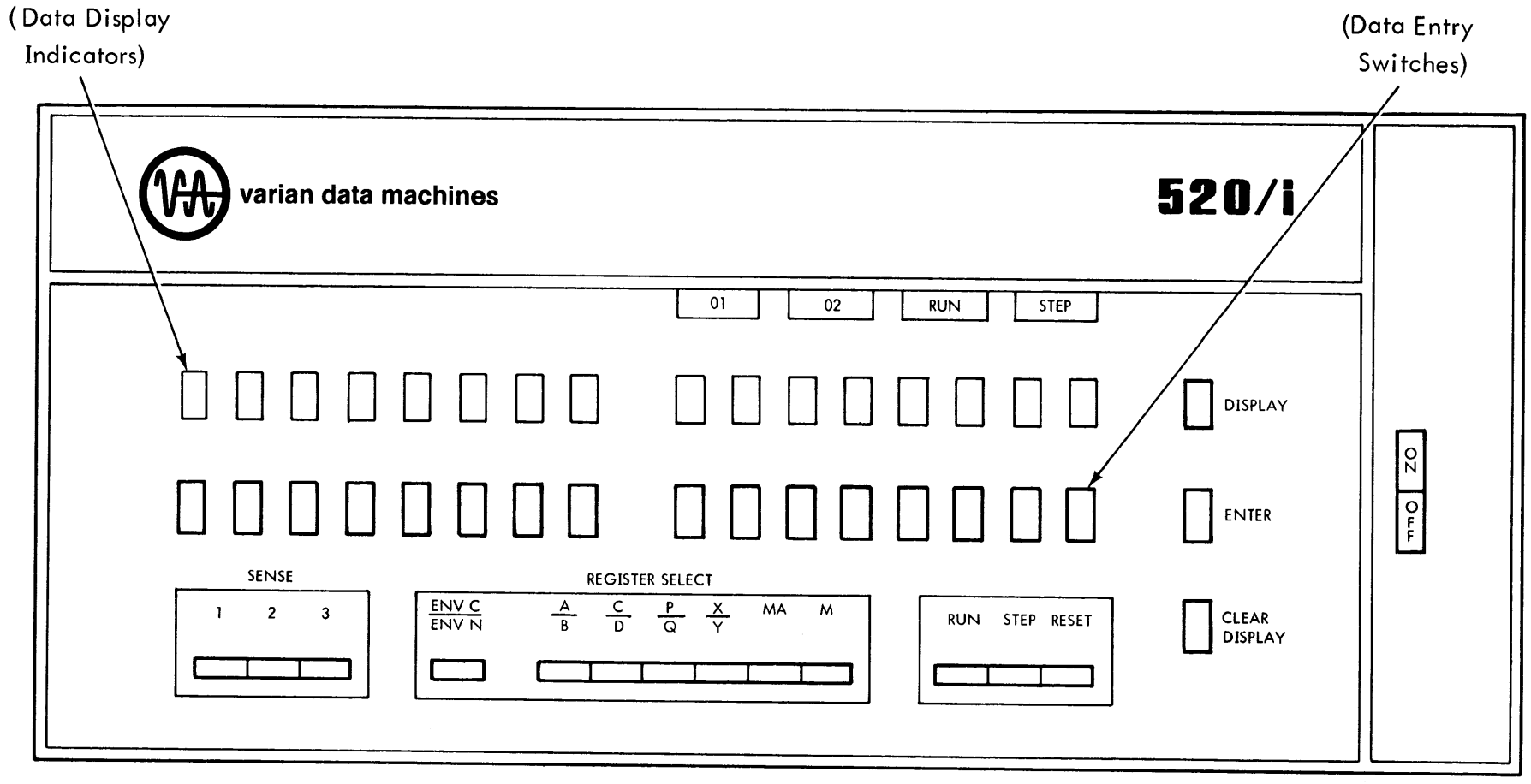


Figure 2-5. 520/i Front Panel

The switches are:

ENV C/ENV N	Determines whether the accumulator, index register or program counter selected (by the switches described below) is for the current or noncurrent environment.
A/B	Selects upper accumulator (current/noncurrent, determined by setting of ENV C/ENV N switch).
C/D	Selects lower accumulator (current/noncurrent).
P/Q	Selects program counter (current/noncurrent).
X/Y	Selects index register (current/noncurrent).
MA	Selects memory address register (cannot be displayed).
M	Selects memory data register.

When a register switch is down, the contents are displayed by pressing the DISPLAY switch. The contents are altered by clearing the display and keying in the new data. Pressing the ENTER switch routes the data to the selected register.

2.2.9 ENTER Switch

When a register is selected for entry, the data entry switches set the switch register with the desired contents. Pressing the ENTER switch transfers the contents of the switch register to the selected register.

2.2.10 SENSE Switches 1, 2 and 3

The three SENSE switches allow program branches and decisions to be made by operator action. The condition of each switch can be interrogated and decisions made in the program based on SENSE switch settings.

2.2.11 Power ON/OFF Switch

The power ON/OFF switch controls the application of ac power to the power supplies in the 520/i. Pressing the ON button resets the 520/i to an initialized condition.

3.1 ORGANIZATION

The standard 520/i computer divides into five major functional areas. These are:

a. Central processor.
b. Memory.
c. Direct-memory-access port.
d. Eight-bit input/output channel.
e. Control panel.

These areas are separately described in Sections 3.4 through 3.8. The relationship between functional areas is shown in Figure 3-1. The figure includes the optional 16-bit input/output channel described in paragraph 1.3.4. To aid in understanding the 520/i functional areas, Section 3.2 describes word formats for all types of data found in the 520/i. Section 3.3 describes the addressing modes possible with 520/i instructions.

3.2 WORD FORMATS

There are three types of words used in the 520/i. These are:

a. Data words.
b. Instructions.
c. Input/output words.

In the following description of word formats, bit positions are numbered from right to left with the highest-numbered bit being the most significant and bit 0 the least significant.

3.2.1 Data Words

Data may occupy as few as eight bits or as many as 32 bits in memory and in the accumulator. Precision of the data may be varied by eight-bit bytes as shown in Figure 3-2. All quantities are represented in two's complement form. The most-significant bit is ZERO for positive numbers and ONE for negative numbers.

3.2.2 Instruction Words

Instructions occupy as few as eight or as many as 24 bits in memory. Instructions are either memory-reference or nonmemory-reference types as shown in Figure 3-3. In the figure,

i	is a binary code that indicates the instruction type,
m	is a binary code that indicates the addressing mode,
y	is a binary operand address that may be modified to obtain the effective address,
f	is a binary code that indicates a particular function to be performed,
f1	is a binary code that indicates a function class modified by f2 and f3,
f2 and f3	are binary codes that specify a particular function within class f1.

3.2.3 Input/Output Words

Input/output words communicate information on the eight-bit I/O channel and on the optional 16-bit I/O channel. As shown in Figure 3-4, the formats of these words are different for each channel.

Basic communication with the 520/i utilizes an eight-bit data word, an eight-bit address word, and individual control and interrupt signals. Optional 16-bit communication with the 520/i is through a peripheral adapter that time-shares 16 lines for output functions and bidirectional data.

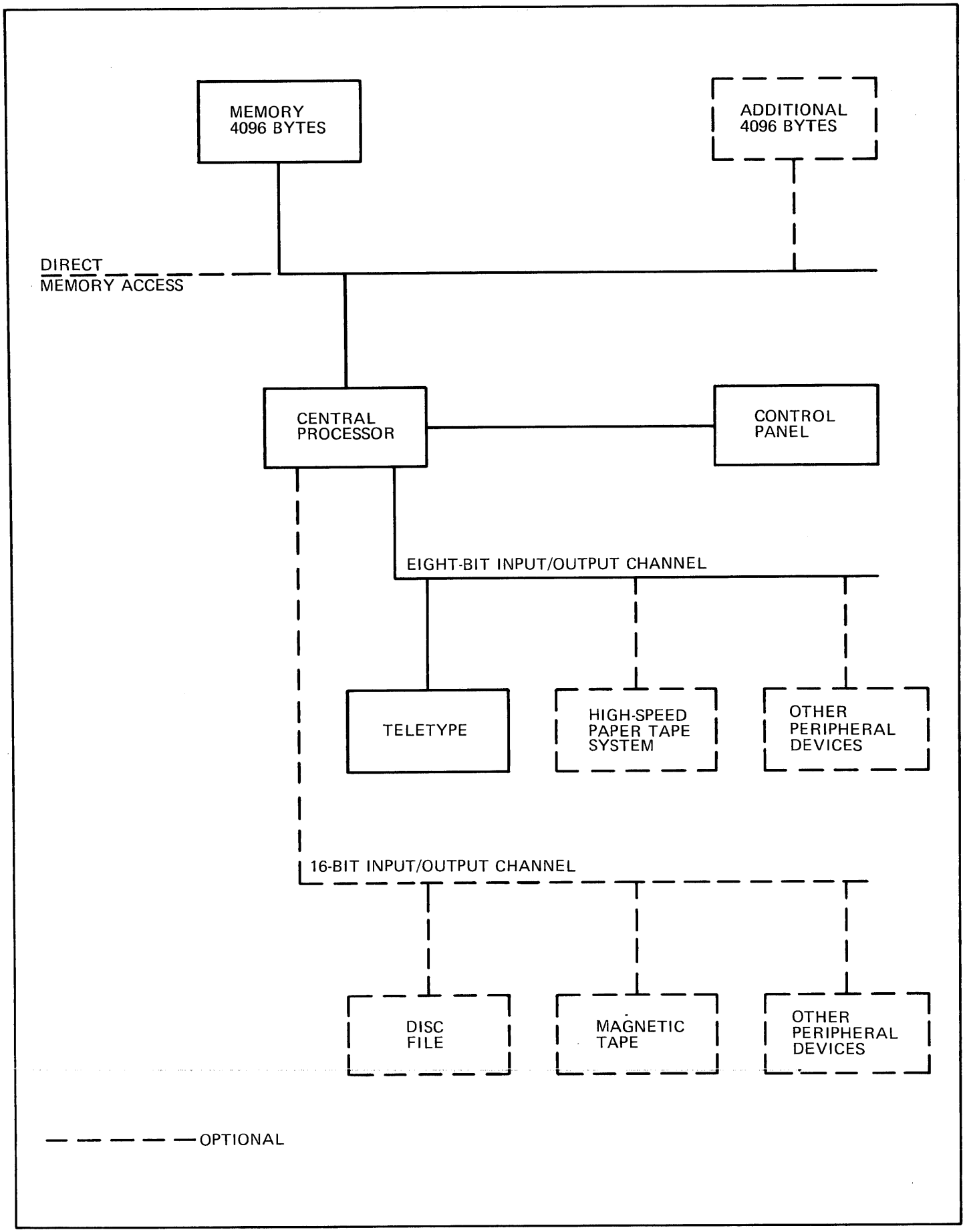
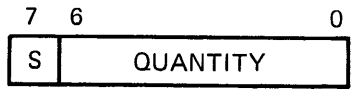


Figure 3-1. 520/i Simplified Block Diagram

BIT 0 = LEAST SIGNIFICANT BIT

S = SIGN BIT

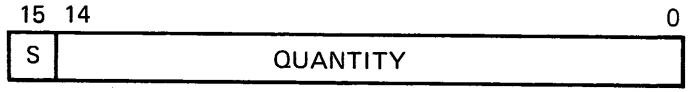
EIGHT-BIT FORMAT



NUMBER RANGE: FRACTIONAL = $-1 \leq N < +1$

INTEGER = $-2^7 \leq N < +2^7$

16-BIT FORMAT



NUMBER RANGE: FRACTIONAL = $-1 \leq N < +1$

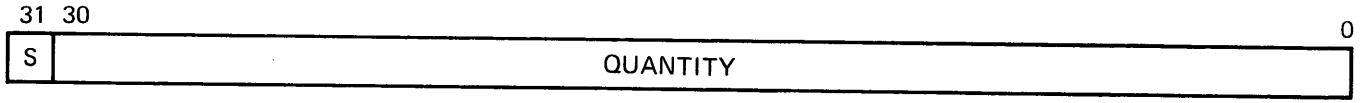
INTEGER = $-2^{15} \leq N < +2^{15}$

24-BIT FORMAT

NUMBER RANGE: FRACTIONAL = $-1 \leq N < +1$

INTEGER = $-2^{23} \leq N < +2^{23}$

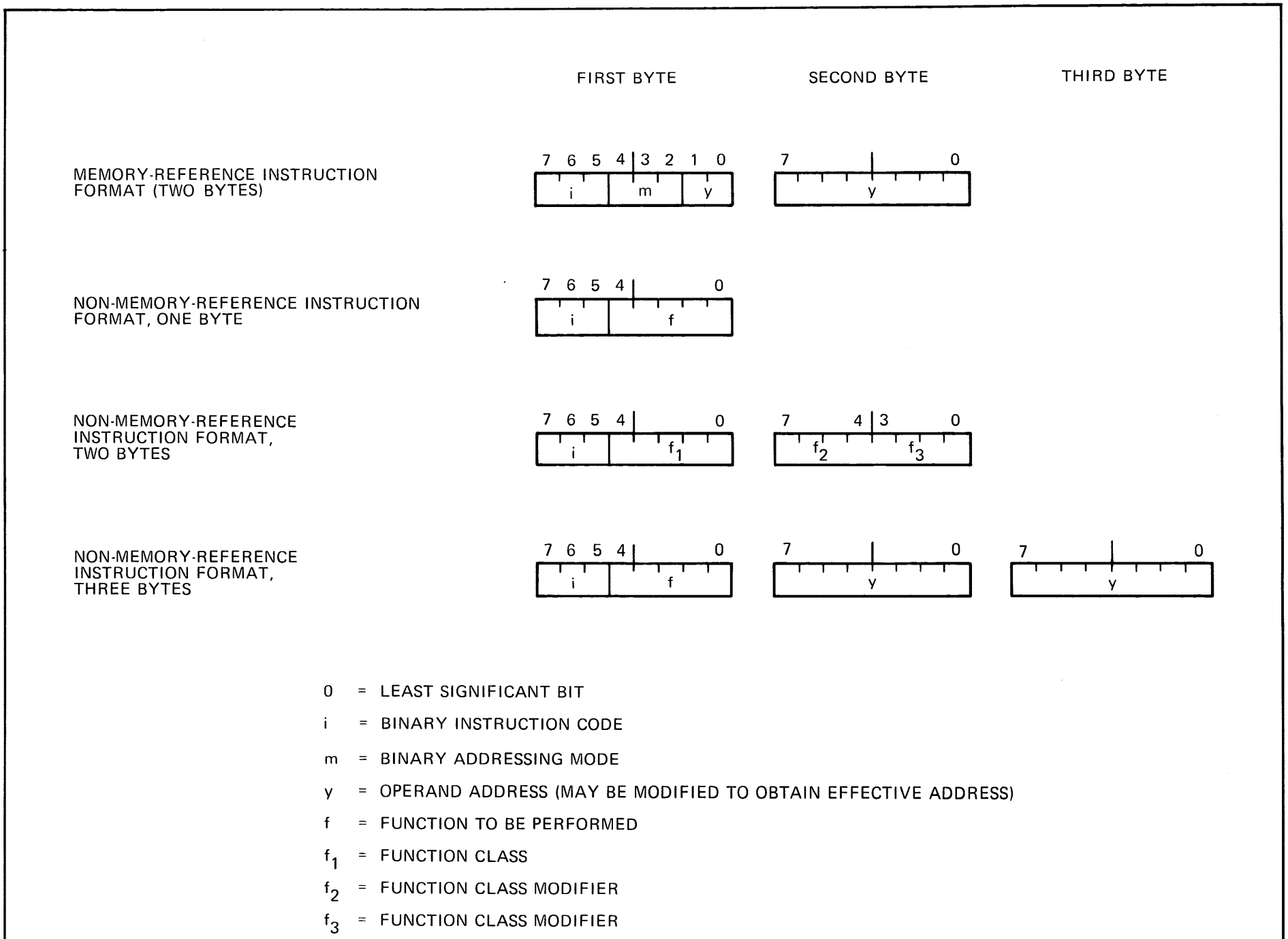
32-BIT FORMAT



NUMBER RANGE: FRACTIONAL = $-1 \leq N < +1$

INTEGER = $-2^{31} \leq N < +2^{31}$

Figure 3-2. Word Formats 520/i Data



0 = LEAST SIGNIFICANT BIT

i = BINARY INSTRUCTION CODE

m = BINARY ADDRESSING MODE

y = OPERAND ADDRESS (MAY BE MODIFIED TO OBTAIN EFFECTIVE ADDRESS)

f = FUNCTION TO BE PERFORMED

f_1 = FUNCTION CLASS

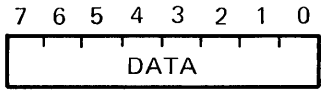
f_2 = FUNCTION CLASS MODIFIER

f_3 = FUNCTION CLASS MODIFIER

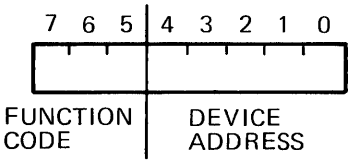
Figure 3-3. 520/i Instruction Formats

EIGHT-BIT INPUT/OUTPUT

DATA WORD (DATA BUS)

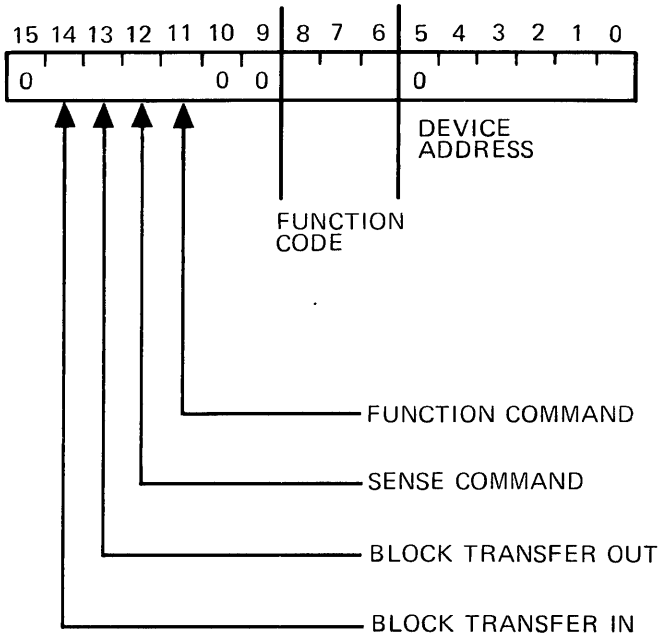


ADDRESS WORD (ADDRESS BUS)



16-BIT INPUT/OUTPUT

FUNCTION WORD (E BUS)



DATA WORD (E BUS)

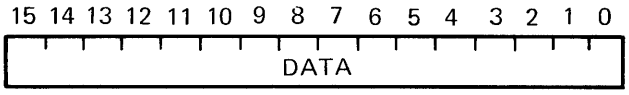


Figure 3-4. 520/i Input/Output Word Formats

3.3 ADDRESSING MODES

Addressing the contents of memory is a function of the current operand and accumulator word length. Word length (precision) is program selectable. The memory is addressed at the byte level. If the current data precision is one byte, the operand address is the only address for that eight bits of data. If the current data precision is two, three or four bytes, the operand address refers to the memory location of the most-significant byte. The accessing of multiple bytes of memory occurs automatically in the correct order for execution.

Address modification is defined by the m field of the instruction word. These three bits specify direct, indirect or indexed addressing. The bits are decoded into eight address conditions defined in Table 3-1.

A sector is 1024 bytes. The basic 520/i has four sectors, with a maximum of 32 sectors possible through optional memory expansion. The division is illustrated in Figure 3-5.

3.3.1 Direct Addressing

There are two forms of direct addressing used in the 520/i:

a. Direct to lower four sectors; enables direct addressing to 4096 bytes of memory. For the standard computer this is total direct addressing
b. Direct to current sector; gives access to 1024 bytes in the sector determined by the most-significant bits of the program counter.

3.3.2 Indirect Addressing

Indirect addressing uses the address y to obtain another operand address contained as a 16-bit word in address y and y + 1. A 16-bit address is always assumed when indirect addressing is specified. The most-significant bit specifies further indirect addressing.

The 520/i uses two modes of indirect addressing:

a. Indirect addressing to zero. Regardless of current sector location, the addressing mechanism returns to the lowest 1024-byte sector of memory to find the effective address. This allows pointers for public routines to be accessible from all sectors.
b. Indirect addressing in current sector. Address y designates the least-significant part of the address while the program counter specifies the most-significant part. This enables the use of 16-bit indirect pointers within the current operating sector.

Table 3-1. Address Bit Decoding

Bit 12	Bit 11	Bit 10	Address Condition
0	0	0	Direct to lower four sectors.
0	0	1	
0	1	0	
0	1	1	
1	0	0	Direct to current sector.
1	0	1	Indirect through current sector.
1	1	0	Indexed.
1	1	1	Indirect through zero sector.

Location	Sector	Comment
0000 ↓ 1023	0	Standard memory module accessible by direct address from anywhere in memory.
1024 ↓ 2047	1	
2048 ↓ 3071	2	
3072 ↓ 4095	3	
4096 ↓ 5119	4	Optional memory modules (4096 bytes each).
5120 ↓ 32,767	5-31	

Figure 3-5. Memory Sector Allocation

3.3.3 Indexing

The 10-bit operand address y may be modified by the addition of the contents of the index register. This yields a 16-bit address that allows addressing of any location in the maximum 32,768-word memory.

3.4 CENTRAL PROCESSOR

The DATA 520/i central processor employs parallel arithmetic and parallel word transfers for maximum speed. Accumulator operations such as add and store are performed with variable word lengths from eight bits to 32 bits. This allows the programmer to utilize the precision required by the data rather than fitting the data to the precision of the machine.

The DATA 520/i central processing unit block diagram is shown in Figure 3-6.

The following operational registers are accessible by the programmer:

a. Two program counters; 16-bits each.
b. Two index registers; 16-bits each.
c. Two accumulators; 32-bits each.

The registers are divided into two functional environments. Environment 1 is interruptable; environment 2 is not interruptable. Either environment may be current or noncurrent.

When environment 1 is interrupted, the program counter, index register and accumulator contents are left unchanged while the processor services the demand of a priority interrupt using the hardware of environment 2. A single instruction (1.5-microsecond execution time) returns the processor to environment 1 to resume the interrupted program. In this way, an I/O subroutine, with separate computation, can be alternated with a background program. If the registers of environment 1 are used for general purpose processing, the programmer has full use of two 32-bit accumulators, two index registers and two program counters.

Additional registers not available to the programmer are:

I Eight-bit instruction register that holds the current instruction and address modification.
MB Eight-bit temporary storage for accessing memory and for control panel display and entry.
S Eight-bit temporary storage for presenting data to the arithmetic unit and for control panel display and entry.
MA 16-bit address register that holds the current operand address.

3.5 MEMORY

The 520/i incorporates a high-speed, random-access memory of modular construction. The memory uses magnetic cores with coincident current read and write control. Each memory module has a capacity of 4096 words of eight or nine bits each. Up to two memory modules may be accommodated in the 520/i main frame. The memory may be expanded to a maximum of 32,768 bytes using expansion chassis.

The memory operates asynchronously with a full-cycle time of 1.5 microseconds and an access time of 500 nanoseconds. Waveforms and timing for a full-cycle operation are shown in Figure 3-7.

3.5.1 Stack Temperature Compensation

The 520/i memory does not require a core-stack heater (with inconvenient warm-up period). The memory allows stack temperature to follow ambient temperature, but compensates by controlling drive currents with an electronic servo. This servo senses stack temperature and automatically adjusts drive and inhibit currents to optimum values.

3.6 DMA PORT

The direct-memory-access (DMA) port of the 520/i computer provides a means for external equipment to interrupt the central processor and initiate a memory operation without the need to execute an interrupt subroutine and without disturbing the operational registers. At the conclusion of the DMA data transfer, the interrupted program continues from where it was interrupted.

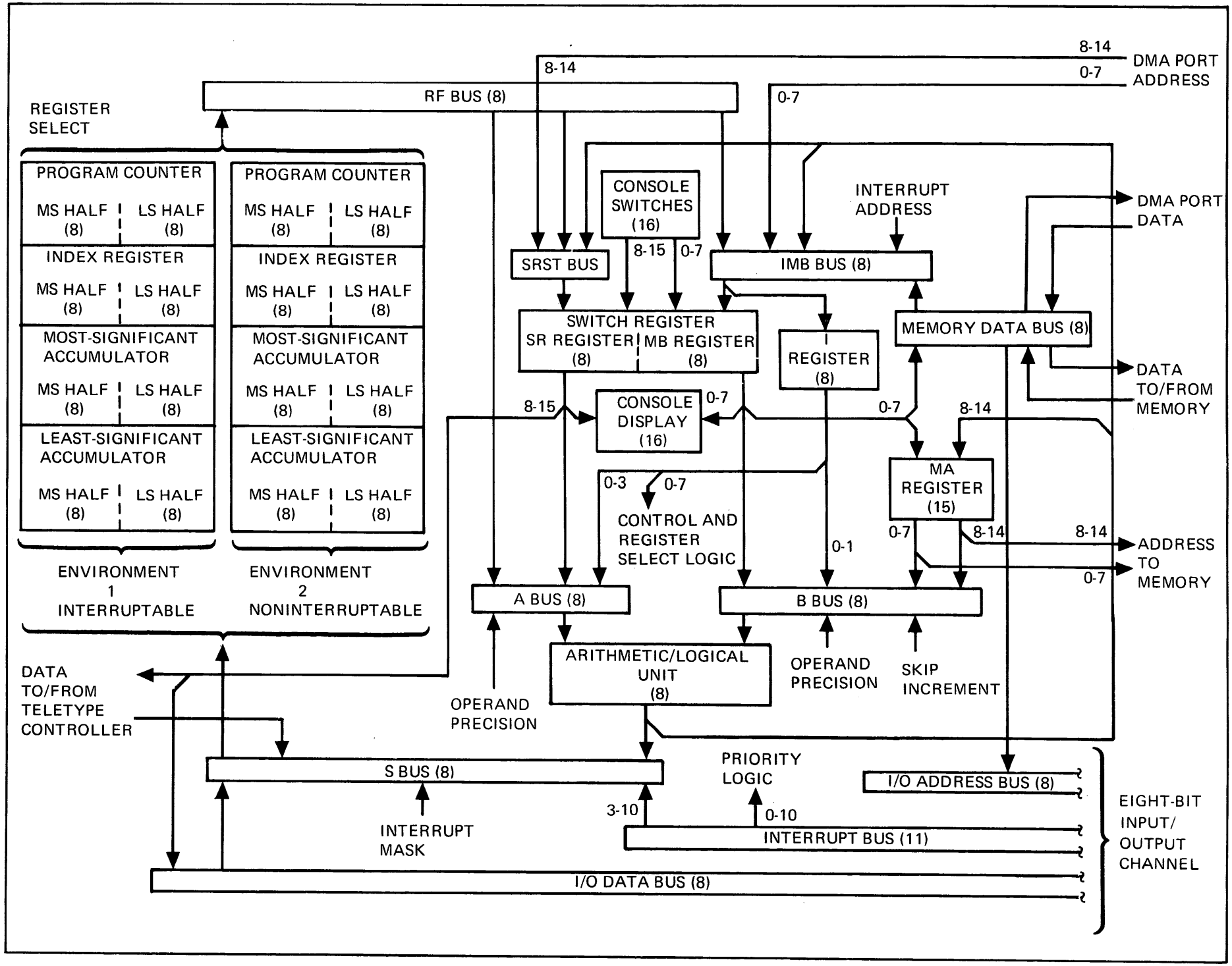


Figure 3-6. 520/i Central Processor Register and Bus Structure

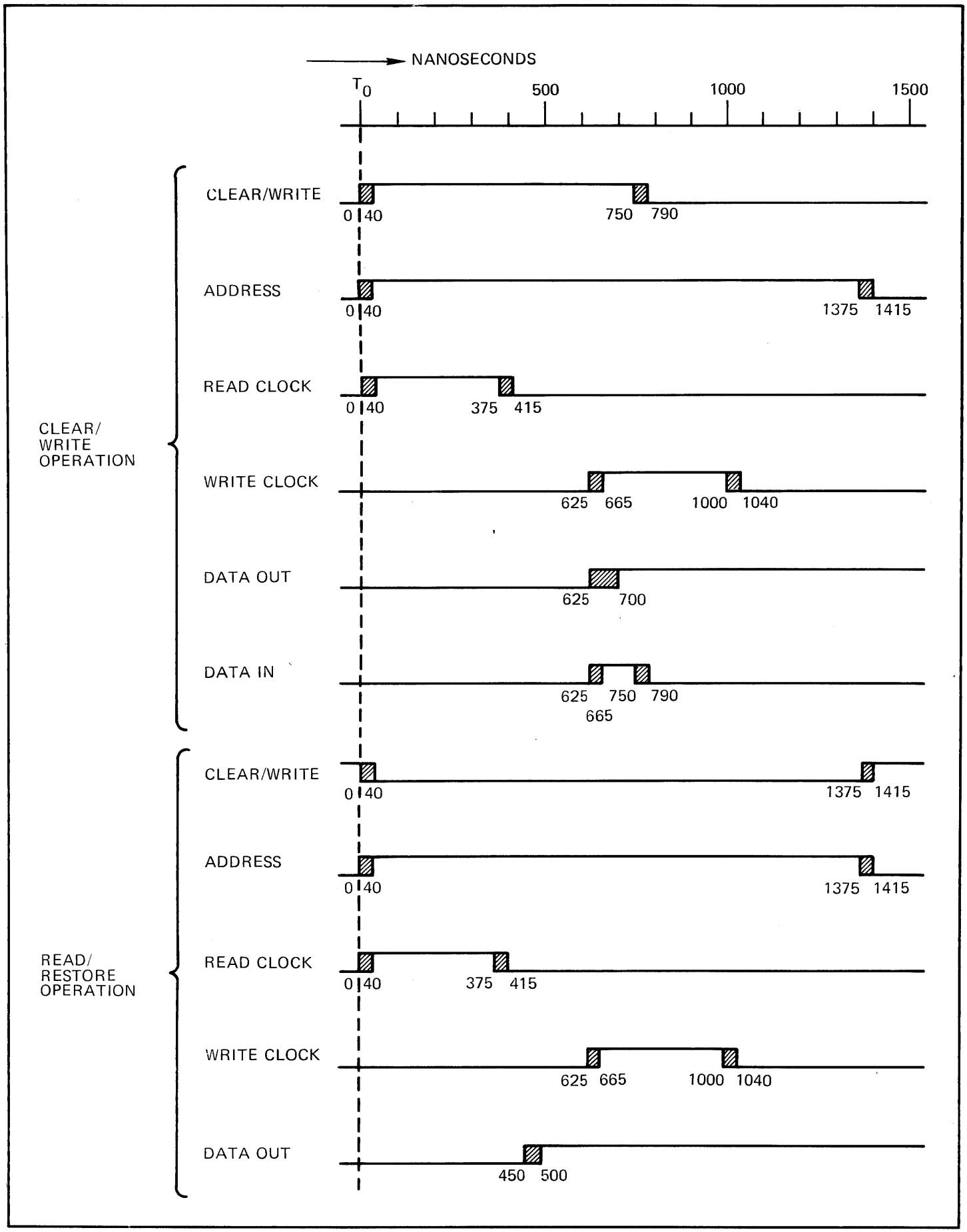


Figure 3-7. 520/i Full-Cycle Memory Timing

The DMA port permits data transfers to and from external equipment at rates up to 666,000 bytes per second. This operation is ideally suited for high-speed data transfers by magnetic tape or disc units, or from data sampling units.

3.7 EIGHT-BIT INPUT/OUTPUT CHANNEL

The eight-bit I/O channel provides efficient and flexible communications with peripheral equipment. Numerous external devices can be controlled with a minimum of control logic.

The eight-bit I/O channel communicates with external equipment over a data bus and an address bus. The data bus comprises eight bidirectional data lines. Each line can be connected to up to ten line drivers or receivers. The address bus comprises three control lines that specify one of eight control functions or sense inquiries, and five device address lines that specify one of 31 possible devices to communicate with the central processor. Each signal can drive up to ten line receivers.

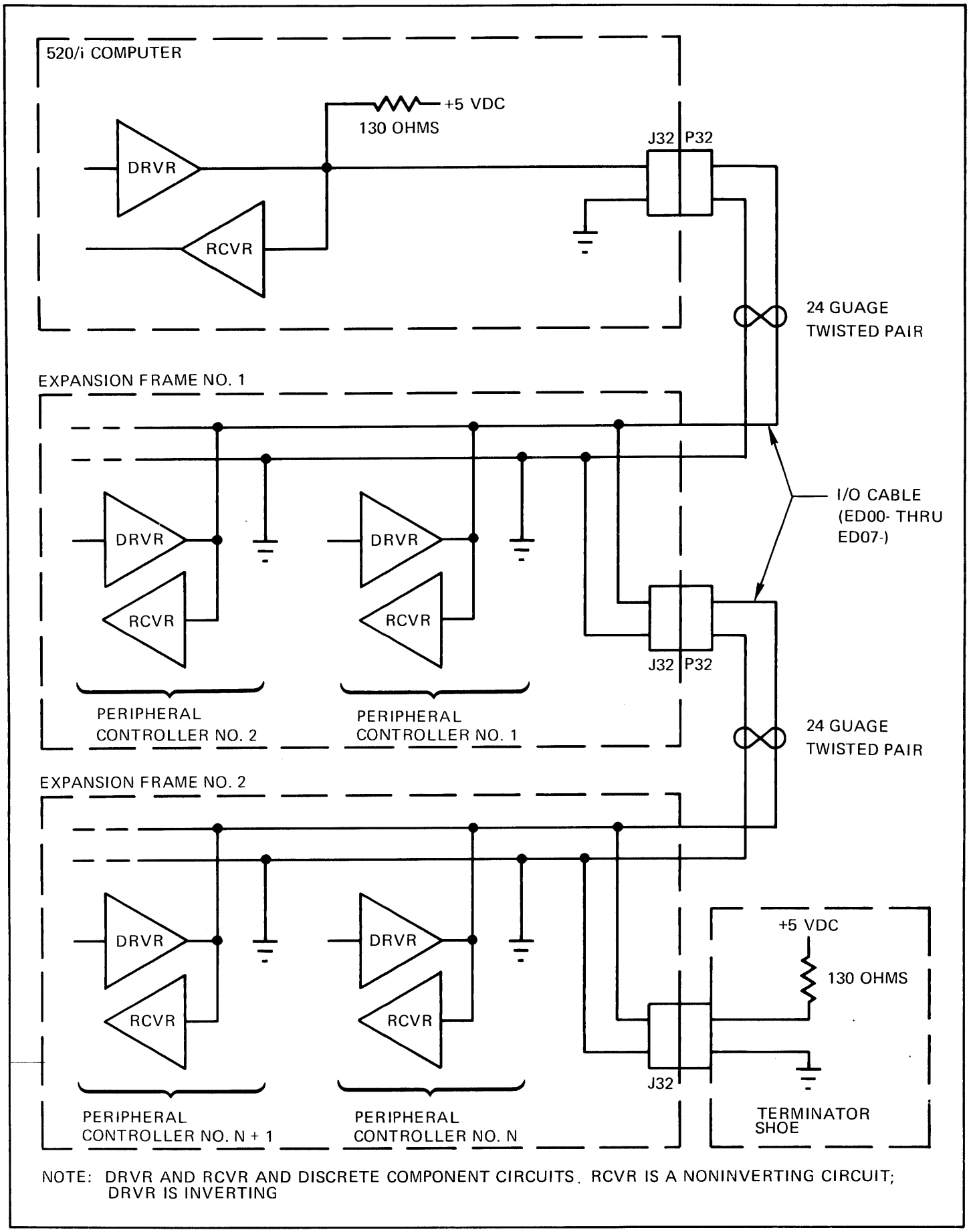
Figures 3-8 through 3-10 show typical data and address line circuits.

3.8 CONTROL PANEL

The control panel houses all switches and displays intended for use by the system operator. These include:

a. Register select switches.
b. Data entry switches.
c. Data display switch and indicators.
d. Data reset switch.
e. Mode select switches and indicators.
f. Sense switches.
g. Power switches and indicators.
h. Accumulator overflow indicators.

From the control panel, the operator can direct and monitor every function of the system.



NOTE: DRVR AND RCVR AND DISCRETE COMPONENT CIRCUITS. RCVR IS A NONINVERTING CIRCUIT; DRVR IS INVERTING

Figure 3-8. Typical 520/i Data Bus Line

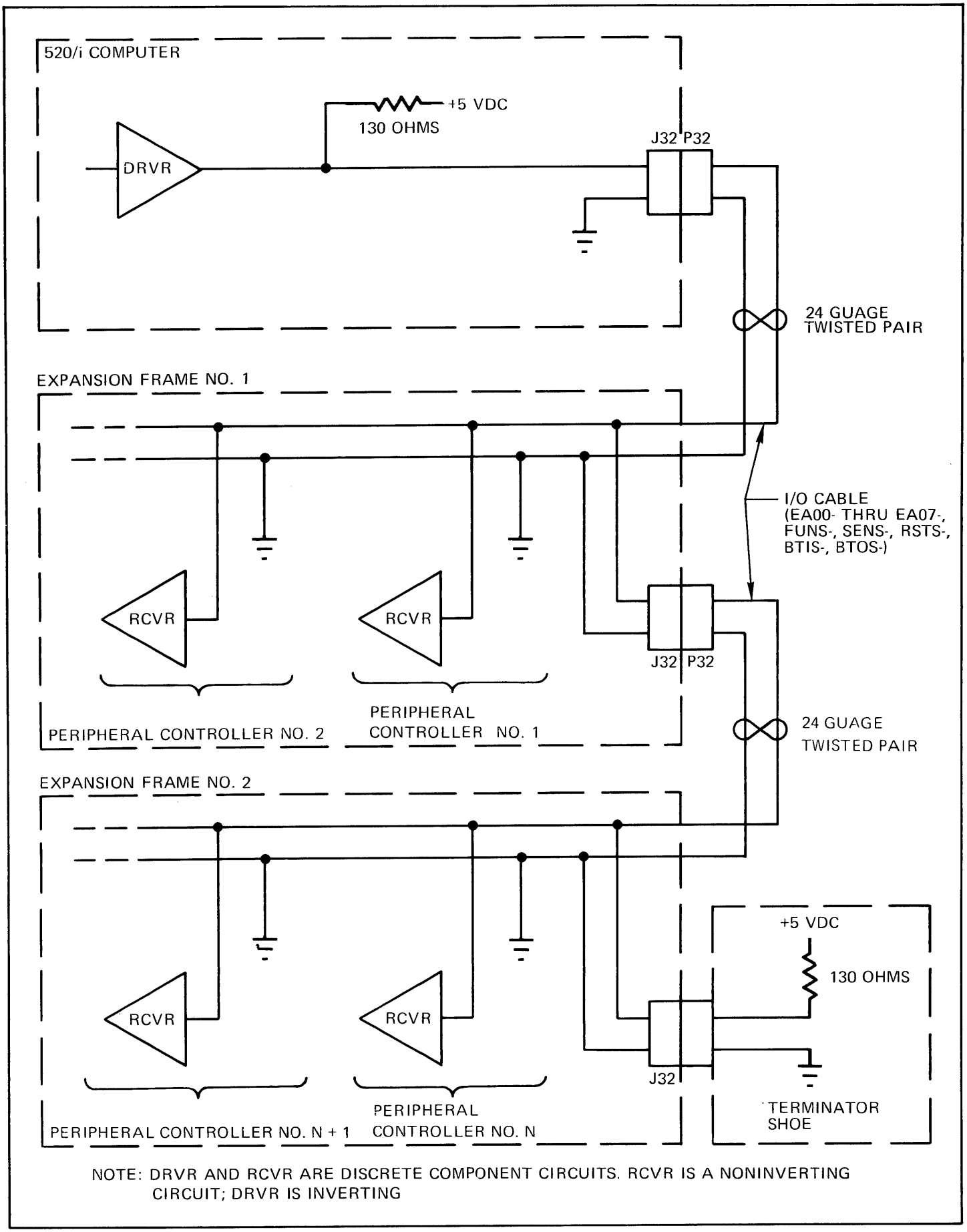


Figure 3-9. Typical Control Line from the 520/i

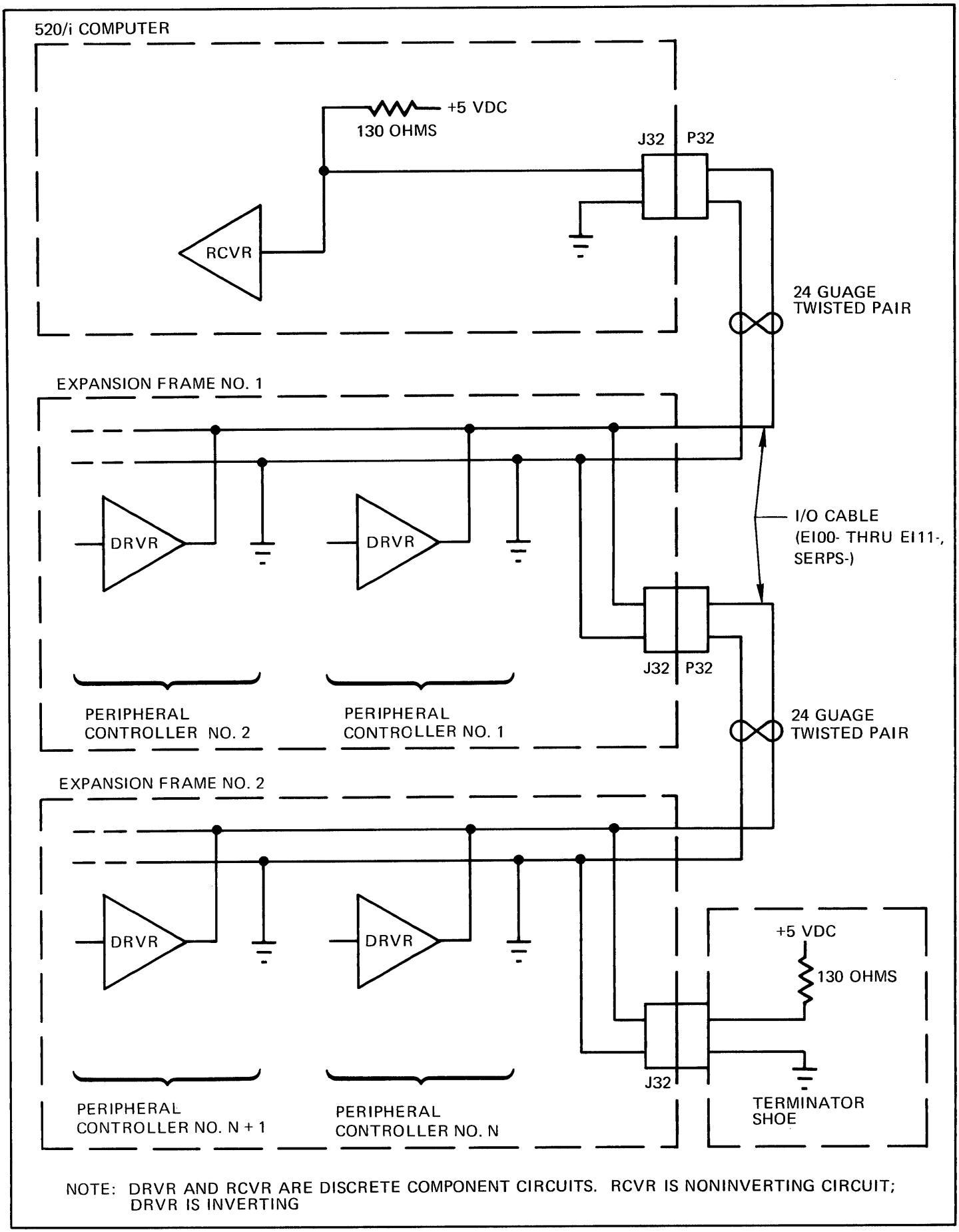


Figure 3-10. Typical Control Line to the 520/i

4.1 GENERAL

This section defines each instruction for the 520/i.

The following table of abbreviations defines symbols used in the instruction descriptions.

Table 4-1. Index of Symbolic Terms

Term	Definition
()	Contents of a register or memory location.
$\overline{()}$	Inverse or one's complement of the contents of a register or memory location.
$\overline{x}$	Inverse or one's complement of expression x.
+	Arithmetic sum (where 0 + 0 = 0, 0 + 1 = 1, 1 + 0 = 1 and 1 + 1 = 10).
−	Arithmetic difference (where 0 − 0 = 0, 0 − 1 = −1, 1 − 0 = 1 and 1 − 1 = 0).
∩	Logical AND (where 0 ∩ 0 = 0, 0 ∩ 1 = 0, 1 ∩ 0 = 0 and 1 ∩ 1 = 1).
∪	Logical OR (where 0 ∪ 0 = 0, 0 ∪ 1 = 1, 1 ∪ 0 = 1 and 1 ∪ 1 = 1).
⊕	Logical exclusive OR (where 0 ⊕ 0 = 0, 0 ⊕ 1 = 1, 1 ⊕ 0 = 1 and 1 ⊕ 1 = 0).
(A) ← (P)	Contents of A are replaced by the contents of P.
OP	Current operand-precision in bytes (1, 2, 3 or 4).
OPC	Two-bit operand precision counter in the current environment.
OVC	Overflow indicator in the current environment.
OPN	Two-bit operand-precision counter in the noncurrent environment.
OVN	Overflow indicator in the noncurrent environment.
Z	16-bit pseudoregister containing all binary ZEROs.
(Acc)	Contents of the entire accumulator in the current environment with an operand precision equal to that of current environment (may be one, two, three or four bytes).
A	Most-significant 16 bits of the accumulator in the current environment.
C	Least-significant 16 bits of the accumulator in the current environment.
X	16-bit index register in the current environment.

Term	Definition
P	16-bit program counter in the current environment.
B	Most-significant 16 bits of the accumulator in the noncurrent environment.
D	Least-significant 16 bits of the accumulator in the noncurrent environment.
Y	16-bit index register in the noncurrent environment.
Q	16-bit program counter in the noncurrent environment.
F	16-bit input/output register in the peripheral adapter.
Y	Operand address in a memory-reference instruction.
s	Source register in a register-change instruction.
d	Destination register in a register-change instruction.
o	Order code in an input/output instruction.
a	Device address in an input/output instruction.
m	Addressing mode of an instruction.
[ ]	Brackets enclose explanatory comments relating to the expression immediately preceding the brackets. For example, y + 2 [if Acc_{MSBit} = 1] means that two is added to y if the most-significant bit of the current accumulator contains a binary ONE.

4.2 MEMORY REFERENCE INSTRUCTIONS

There are two types of memory reference instructions for the 520/i:

a. Those that specify the location of one operand where the other is assumed (e.g., in the accumulator).
b. Those that specify a location to begin a new sequence.

The length of the accumulator may vary from eight to 32 bits, under program control. Whenever an accumulator operation references memory, it does so relative to the current accumulator length. If the accumulator length is eight bits, the operand reference to memory is only eight bits. If the accumulator length is 16, 24 or 32 bits, the operand reference to memory corresponds.

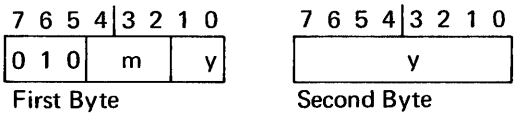
The operand address actually points to the first byte of a two, three or four-byte string when the accumulator length is greater than eight bits. The first byte in memory is always the most-significant byte of the operand. Accessing multiple bytes is automatic according to accumulator length.

Instruction: LOD Load accumulator

Description: (Acc) ← (y)

The contents of the memory location(s) specified by the effective address are placed in the accumulator. The contents of memory are unaffected.

Coding:



Timing:

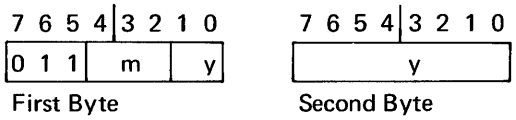
Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	3	4	5	6

Instruction: STO Store accumulator

Description: (y) ← (Acc)

The contents of the accumulator are placed in the memory location(s) specified by the effective address. The accumulator is unaffected.

Coding:



Timing:

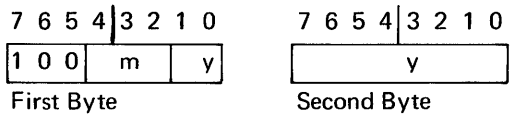
Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	3	4	5	6

Instruction: SUM Add to accumulator

Description: (Acc) ← (Acc) + (y)

The arithmetic sum of the contents of the accumulator and the contents of the memory location(s) specified by the effective address are placed in the accumulator. The contents of memory are unaffected. The overflow indicator is set if the result is less than -2^{AL-1} or greater than $2^{AL-1} - 1$, where AL is the accumulator length in bits.

Coding:



Timing:

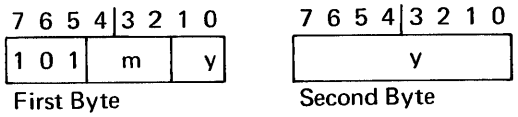
Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	3	4	5	6

Instruction: SUB Subtract from accumulator

Description: (Acc) ← (Acc) − (y)

The arithmetic difference between the contents of the accumulator and the contents of the memory location(s) specified by the effective address are placed in the accumulator. The contents of memory are unaffected. The overflow indicator is set if the result is less than -2^{AL-1} or greater than $2^{AL-1} - 1$, where AL is the accumulator length in bits.

Coding:



Timing:

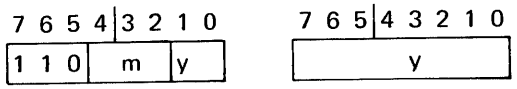
Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	3	4	5	6

Instruction: AND AND to accumulator

Description: (Acc) ← (Acc) ∩ (y)

The logical product of the contents of the accumulator and the contents of the memory location(s) specified by the effective address are placed in the accumulator. The contents of memory are unaffected.

Coding:



Timing:

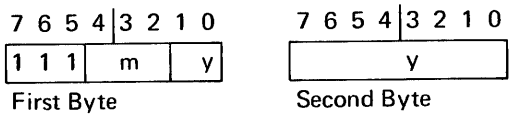
Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	3	4	5	6

Instruction: BRU Branch unconditionally

Description: (P) ← y

The effective address (after any address modification) is placed in the current program counter.

Coding:



Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	2	2	2	2

4.3 NON-MEMORY-REFERENCE ONE-BYTE INSTRUCTIONS

4.3.1 Register-Operate Instructions

Instruction: CLA Clear accumulator

Description: (Acc) ← 0

The contents of the current accumulator are set to zero. The accumulator is affected only to the set precision.

Coding:

7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	0

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	1	2	2	2

Instruction: CMA Complement accumulator

Description: (Acc) ← $\overline{(Acc)}$

The contents of the current accumulator are inverted (one's complement). The accumulator is affected only to the set precision.

Coding:

7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	1

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	1	2	2	2

Instruction: IAR Increment accumulator

Description: (Acc) ← (Acc) + 1

The contents of the current accumulator are incremented by one. The accumulator is affected only to the set precision. If the result is greater than $2^{AL-1} - 1$, where AL is the accumulator length in bits, the overflow indicator is set.

Coding:

7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	0

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	1	2	2	2

Instruction CIA Complement and increment accumulator

Description: (Acc) ← $\overline{(Acc)}$ + 1

The contents of the current accumulator are inverted and incremented (two's complement). The accumulator is affected only to the set precision. If the result is less than -2^{AL-1}, where AL is the accumulator length in bits, the overflow indicator is set.

Coding:

7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	1

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	1	2	2	2

Instruction: IXO Increment index register by the operand precision.

Description: (X) ← (X) + (OPC)

The current operand precision (in bytes) is added to the contents of the current index register.

Coding:

7	6	5	4	3	2	1	0
0	0	0	1	0	1	1	1

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	2	2	2	2

4.3.2 Control Instructions

Instruction: SP1 Set operand precision to 1 byte

Description: OP = 1 byte

The accumulator and operand length is adjusted to eight bits.

Coding:

7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	0

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	1	1	1	1

Instruction: SP2 Set operand precision to 2 bytes

Description: OP = 2 bytes

The accumulator and operand length is adjusted to 16 bits.

Coding:

7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	1

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	1	1	1	1

Instruction: SP3 Set operand precision to 3 bytes

Description: OP = 3 bytes

The accumulator and operand length is adjusted to 24 bits.

Coding:

7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	0

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	1	1	1	1

Instruction: SP4 Set operand precision to 4 bytes

Description: OP = 4 bytes

The accumulator and operand length is adjusted to 32 bits.

Coding:

7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	1

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	1	1	1	1

Instruction: HLT Halt

Description: The machine halts with the program counter containing the next location in sequence.

Coding:

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	1	1	1	1

Instruction: NOP No operation

Description: No execution activity takes place during this instruction.

Coding:

7	6	5	4	3	2	1	0
0	0	0	1	0	1	1	0

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	1	1	1	1

Instruction: SOF Set overflow indicator

Description: (OVC) ← 1

The current overflow indicator is set.

Coding:

7	6	5	4	3	2	1	0
0	0	0	1	0	1	0	0

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	1	1	1	1

Instruction: ROF Reset overflow indicator

Description: (OVC) ← 0

The current overflow indicator is reset.

Coding:

7	6	5	4	3	2	1	0
0	0	0	1	0	1	0	1

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	1	1	1	1

4.3.3 Skip Instructions

All skip instructions cause the next instruction in sequence to be executed if the skip condition tested for is false. If the skip condition tested for is true, P increments twice to jump over an intervening two-byte instruction.

Instruction: SAN Skip if accumulator is negative

Description: (P) ← (P) + 1 + 2 [if (Acc) < 0]

If the contents of the current accumulator are less than zero, the next two bytes in sequence are skipped. The accumulator is tested only to the set precision.

Coding:

7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	0

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	1	1	1	1

Instruction: SANN Skip if accumulator is not negative

Description: (P) ← (P) + 1 + 2 [if (Acc) ⩾ 0]

If the contents of the current accumulator are not less than zero, the next two bytes in sequence are skipped. The accumulator is tested only to the set precision.

Coding:

7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	1

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	1	1	1	1

Instruction: SAZ Skip if accumulator is zero

Description: (P) ← (P) + 1+2 [if (Acc) = 0]

If the contents of the current accumulator are zero, the next two bytes in sequence are skipped. The accumulator is tested only to the set precision.

Coding:

7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	0

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	1	2	2	2

Instruction: SAZN Skip if accumulator is not zero

Description: (P) ← (P) + 1 + 2 [if (Acc) ≠ 0]

If the contents of the current accumulator are not zero, the next two bytes in sequence are skipped. The accumulator is tested only to the set precision.

Coding:

7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	1

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	1	2	2	2

Instruction: SXZ Skip if index register is zero

Description: (P) ← (P) + 1 + 2 [if (X) = 0]

If the contents of the current index register are zero the next two bytes in sequence are skipped.

Coding:

7	6	5	4	3	2	1	0
0	0	0	0	1	0	1	0

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	2	2	2	2

Instruction: SXZN Skip if index register is not zero

Description: (P) ← (P) + 1 + 2 [if (X) ≠ 0]

If the contents of the current index register are not zero, the next two bytes in sequence are skipped.

Coding:

7	6	5	4	3	2	1	0
0	0	0	0	1	0	1	1

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	2	2	2	2

Instruction: SOV Skip on accumulator overflow

Description: (P) ← (P) + 1 + 2 [if (OVC) = 1]

(OVC) ← 0

If the overflow indicator of the current accumulator has been set by a previous operation, the next two bytes in sequence are skipped. The current overflow indicator is reset regardless of the test outcome.

Coding:

7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	1	1	1	1

Instruction: SOVN Skip on no accumulator overflow

Description: (P) ← (P) + 1 + 2 (if (OVC) = 0]

If the overflow indicator of the current accumulator has not been set by a previous operation, the next two bytes in sequence are skipped. The current overflow indicator is reset regardless of the test outcome.

Coding:

7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	1	1	1	1

Instruction: SOD Skip if accumulator is odd

Description: (P) ← (P) + 1 + 2 [if (Acc_{LSBit}) = 1]

If the least-significant bit of the current accumulator is a ONE, the next two bytes in sequence are skipped.

Coding:

7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	1	1	1	1

Instruction: SODN Skip if accumulator is not odd

Description: $(P) \leftarrow (P) + 1 + 2$ [if $(Acc_{LSBit}) = 0$]

If the least-significant bit of the current accumulator is not a ONE, the next two bytes in sequence are skipped.

Coding:

7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	1

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	1	1	1	1

4.3.4 Shift Instructions

Instruction: SR1 Shift right 1 bit

Description: $(Acc_n) \leftarrow (Acc_{n+1})$

$(Acc_{MSBit}) \leftarrow 0$

The current accumulator is shifted one bit to the right. ZERO is shifted into the most-significant bit. The accumulator is affected only to the set precision.

Coding:

7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	0

First Byte

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	1	2	2	2

Instruction: SR8 Shift right 8 bits (1 byte)

Description: $(Acc_n) \leftarrow (Acc_{n+8})$

$(Acc_{MSByte}) \leftarrow 0$

The current accumulator is shifted eight bits to the right. ZEROs are shifted into the most-significant byte. The accumulator is affected only to the set precision.

Coding:

7	6	5	4	3	2	1	0
0	0	0	1	1	0	0	1

First Byte

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	1	2	2	2

Instruction: RR1 Rotate right 1 bit

Description: $(Acc_n) \leftarrow (Acc_{n+1})$

$(Acc_{MSBit}) \leftarrow (Acc_{LSBit})$

The current accumulator is rotated one bit to the right. The least-significant bit replaces the most-significant bit. The accumulator is affected only to the set precision.

Coding:

7	6	5	4	3	2	1	0
0	0	0	1	1	0	1	0

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	2	2	2	3

Instruction: RR8 Rotate right 8 bits (1 byte)

Description: $(Acc_n) \leftarrow (Acc_{n+8})$

$(Acc_{MSByte}) \leftarrow (Acc_{LSByte})$

The current accumulator is rotated eight bits to the right. The least-significant byte replaces the most-significant byte. The accumulator is affected only to the set precision.

Coding:

7	6	5	4	3	2	1	0
0	0	0	1	1	0	1	1

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	1	2	2	2

Instruction: SL1 Shift left 1 bit

Description: $(Acc_n) \leftarrow (Acc_{n-1})$

$(Acc_{LSBit}) \leftarrow 0$

The current accumulator is shifted one bit to the left. ZERO is shifted into the least-significant bit. The accumulator is affected only to the set precision.

Coding:

7	6	5	4	3	2	1	0
0	0	0	1	1	1	0	0

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	1	2	2	2

Instruction: SL8 Shift left 8 bits (1 byte)

Description: $(Acc_n) \leftarrow (Acc_{n-8})$

$(Acc_{LSByte}) \leftarrow 0$

The current accumulator is shifted eight bits to the left. ZEROs are shifted into the least-significant byte. The accumulator is affected only to the set precision.

Coding:

7	6	5	4	3	2	1	0
0	0	0	1	1	1	0	1

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	1	2	2	2

Instruction: RL1 Rotate left 1 bit

Description: $(Acc_n) \leftarrow (Acc_{n-1})$

$(Acc_{LSBit}) \leftarrow (Acc_{MSBit})$

The current accumulator is rotated one bit to the left. The most significant bit replaces the least-significant bit. The accumulator is affected only to the set precision.

Coding:

7	6	5	4	3	2	1	0
0	0	0	1	1	1	1	0

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	2	2	2	3

Instruction: RL8 Rotate left 8 bits (1 byte)

Description: $(Acc_n) \leftarrow (Acc_{n-8})$

$(Acc_{LSByte}) \leftarrow (Acc_{MSByte})$

The current accumulator is rotated bits to the left. The most-significant byte replaces the least-significant byte. The accumulator is affected only to the set precision.

Coding:

7	6	5	4	3	2	1	0
0	0	0	1	1	1	1	1

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	1	2	2	2

4.3.5 Environmental Control Instructions

Switching between environments is always under program control even when initiated by hardware interrupt. The actual change in environmental status is accomplished by executing a change-status (CST) instruction or a load-Q-and-change-status (CSQ) instruction. These are the only ways to transfer the program from one program sequence to the alternate sequence.

In general-purpose use, the transfer is programmed to make full use of two accumulators and two index registers.

When using the I/O interrupt system to switch modes, the CST instruction is programmed into the memory location associated with the desired interrupt. Other interrupts may occur, but they must be processed by programming a BRM (branch and mark) instruction in the associated interrupt cells.

While in environment 2 (noninterruptable), whether for general-purpose use or high-rate I/O servicing, external interrupts are ignored. The CST instruction from environment 1 to environment 2 disables any interrupts. When preceded by an IBE instruction, the CST instruction from environment 2 back to environment 1 reenables the interrupt capability.

Instruction: CST Change environmental status

Description: The environment is changed. The noncurrent environment becomes the current operating environment. Instruction execution begins with the instruction at the location in the new location counter. Accumulator precision is unchanged from the last time in the new environment. The old location counter, accumulator and index register are unaffected.

Coding:

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	1	1	1	1

4.4 NON-MEMORY REFERENCE TWO-BYTE INSTRUCTIONS

4.4.1 Register-Operate Instructions

The eight 16-bit registers used in maintaining a foreground and background process may also be used as general-purpose registers.

The registers are treated as separate 16-bit values without regard to accumulator precision. The register status (current or noncurrent) is always relative to the current environment (1 or 2).

Register codes for these instructions are given in Table 4-2.

Instruction: T Transfer source register to destination register

Description: (d) ← (s)

The contents of the source register are placed in the destination register. The source register is unaffected.

Coding:

7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	0

First Byte

7	6	5	4	3	2	1	0
s				d			

Second Byte

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	3	3	3	3

Table 4-2. Register Codes

Register	Binary Code
Z	0000
A	0001
C	0010
X	0011
P	0100
B	0110
D	0111
Y	0111
Q	1000
F*	1001

Instruction: C Complement source register and transfer to destination register

Description: (d) ← $\overline{(s)}$

The contents of the source register are inverted and placed in the destination register. The source register is unaffected unless it is also the destination register.

Coding:

7 6 5 4	3 2 1 0
0 0 1 0 0 0 0 1	

First Byte

7 6 5 4	3 2 1 0
s	d

Second Byte

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	3	3	3	3

Instruction: I Increment source register and transfer to destination register

Description: (d) ← $\overline{(s)}$ + 1

The contents of the source register are incremented by one and placed in the destination register. The source register is unaffected unless it is also the destination register.

Coding:

7 6 5 4	3 2 1 0
0 0 1 0 0 0 1 0	

First Byte

7 6 5 4	3 2 1 0
s	d

Second Byte

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	3	3	3	3

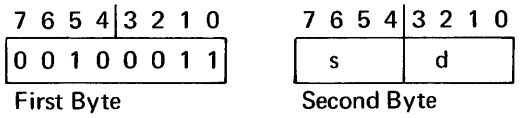
*The only permissable instruction in which this register may be used is T (transfer).

Instruction: D Decrement source register and transfer to destination register

Description: (d) ← (s) − 1

The contents of the source register are decremented by one and placed in the destination register. The source register is unaffected unless it is also the destination register.

Coding:



Timing:

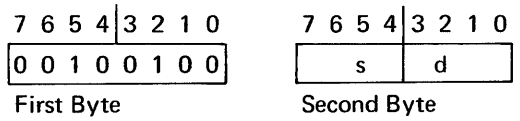
Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	3	3	3	3

Instruction: M AND source register into destination register

Description: (d) ← (d) ∩ (s)

The logical product of the contents of the source register and the destination register is placed in the destination register. The source register is unaffected.

Coding:



Timing:

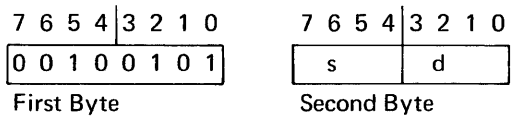
Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	3	3	3	3

Instruction: O Inclusive OR source register into destination register

Description: (d) ← (d) ∪ (s)

The logical sum of the contents of the source register and the destination register is placed in the destination register. The source register is unaffected.

Coding:



Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	3	3	3	3

Instruction: E Exclusive OR source register into destination register

Description: (d) ← (d) ⊕ (s)

The logical exclusive OR of the contents of the source register and the destination register is placed in the destination register. The source register is unaffected unless it is also the destination register.

Coding:

7 6 5 4	3 2 1 0
0 0 1 0	0 1 1 0

First Byte

7 6 5 4	3 2 1 0
s	d

Second Byte

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	3	3	3	3

Instruction: A Add source register to destination register

Description: (d) ← (d) + (s)

The artihmetic sum of the contents of the source register and the destination register is placed in the destination register. The source register is unaffected unless it is also the destination register. The overflow indicator is not set by this instruction.

Coding:

7 6 5 4	3 2 1 0
0 0 1 0	0 1 1 1

First Byte

7 6 5 4	3 2 1 0
s	d

Second Byte

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	3	3	3	3

4.4.2 Input/Output Instructions

Instruction: BTO Byte transfer out

Description: I/O data bus ← (Acc_{LSByte})

I/O address bus ← o, a

The order code and device address are placed on the I/O address bus. The least-significant eight bits of the current accumulator are placed on the I/O data bus.

Coding:

7 6 5 4	3 2 1 0
0 0 1 1	0 0 0 0

First Byte

7 6 5 4	3 2 1 0
o	a

Second Byte

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	2	2	2	2

Instruction: BTI Byte transfer in

Description: $(Acc_{LSByte}) \leftarrow$ I/O data bus

I/O address bus ← o, a

The order code and device address are placed on the I/O address bus. A byte of data from the addressed device is placed in the least-significant eight bits of the current accumulator.

Coding:

7 6 5 4	3 2 1 0
0 0 1 1	0 0 0 1

First Byte

7 6 5 4	3 2 1 0
o	a

Second Byte

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	2	2	2	2

Instruction: SEN Sense and skip

Description: I/O address bus ← o, a

(P) ← (P) + 2 + 2 [if sense response true]

The order code and device address are placed on the I/O address bus. The next two bytes in sequence are skipped if the sense response line on the I/O bus is true. The device being interrogated uses the order code to condition its response to various inquiries.

Coding:

7 6 5 4	3 2 1 0
0 0 1 1	0 0 1 0

First Byte

7 6 5 4	3 2 1 0
o	a

Second Byte

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	3	3	3	3

Instruction: FUN Function out

Description: I/O data bus ← (Acc_{LSByte})

I/O address bus ← o, a

The order code and device address are placed on the I/O address bus. The least-significant eight bits of the current accumulator are placed on the I/O data bus (may be used as a special BTO instruction or may be ignored). The device being commanded interprets the order code and executes the indicated function (e.g., rewind tape).

Coding:

7 6 5 4	3 2 1 0
0 0 1 1	0 0 1 1

First Byte

7 6 5 4	3 2 1 0
o	a

Second Byte

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	2	2	2	2

4.4.3 Assigned Input/Output Instructions

Device address 00 is decoded internally by the 520/i to execute special instructions.

Instruction: MIN Modify interrupts (0 to 3)

Description: Interrupt enable n = 1 [if (Acc_n) = 1]

Interrupt enable n = 0 [if (Acc_{n+4}) = 1]

The interrupts are selectively enabled or disabled by this instruction.

The least significant bits of the accumulator are used to modify the enable/disable status of the four interrupts lines. Binary ONEs in bits 0 to 3 of the current accumulator enable interrupts 0 to 3. Binary ONEs in bits 4 to 7 of the current accumulator disable interrupts 0 to 3.

If the enable bit in the accumulator is a ZERO and the disable bit is a ZERO, the interrupt status is unaffected. If both enable and disable bits are ONE, the interrupt status is complemented.

Coding:

7 6 5 4	3 2 1 0
0 0 1 1	0 0 0 0

First Byte

7 6 5 4	3 2 1 0
0 0 0 0	0 0 0 0

Second Byte

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	2	2	2	2

Instruction: SS1 Skip if sense switch 1 is off

Description: (P) ← (P) + 2 + 2 [if sense switch 1 = 0]

If the front-panel SENSE switch 1 is not set, the next two bytes in sequence are skipped.

Coding:

7 6 5 4	3 2 1 0
0 0 1 1	0 0 1 0

First Byte

7 6 5 4	3 2 1 0
0 0 1 0	0 0 0 0

Second Byte

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	3	3	3	3

Instruction: SS2 Skip if sense switch 2 if off

Description: (P) ← (P) + 2 + 2 [if sense switch 2 = 0]

If the front-panel SENSE switch 2 is not set, the next two bytes in sequence are skipped.

Coding:

7 6 5 4	3 2 1 0
0 0 1 1	0 0 1 0

First Byte

7 6 5 4	3 2 1 0
0 1 0 0	0 0 0 0

Second Byte

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	3	3	3	3

Instruction: SS3 Skip if sense switch 3 is off

Description: (P) ← (P) + 2 + 2 [if sense switch 3 = 1]

If the front-panel SENSE switch 3 is not set, the next two bytes in sequence are skipped.

Coding:

7 6 5 4	3 2 1 0
0 0 1 1	0 0 1 0

First Byte

7 6 5 4	3 2 1 0
1 0 0 0	0 0 0 0

Second Byte

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	3	3	3	3

Instruction: SIE Skip on interruptable environment

Description: (P) ← (P) + 2 + 2 [if machine is in environment 1]

If the machine is in the interruptable environment (environment 1), the next two bytes in sequence are skipped.

Coding:

7 6 5 4	3 2 1 0
0 0 1 1	0 0 1 0

First Byte

7 6 5 4	3 2 1 0
0 0 0 0	0 0 0 0

Second Byte

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	3	3	3	3

Instruction: SSH Skip on halt-mode power failure

Description: (P) ← (P) + 2 + 2 [if machine is in halt-mode during power-fail interrupt]

If the machine is in the halt-mode and a power-fail interrupt (optional) is detected, the next two bytes in sequence are skipped.

Coding:

7 6 5 4	3 2 1 0
0 0 1 1	0 0 1 1

First Byte

7 6 5 4	3 2 1 0
0 1 1 0	0 0 0 0

Second Byte

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	3	3	3	3

Instruction: CIS Copy interrupt status

Description: (Acc_0 to Acc_7) ← interrupts 3 to 10

The eight interrupt lines that share priority interrupt 3 are placed in the least-significant bits of the current accumulator.

Coding:

7 6 5 4 | 3 2 1 0	7 6 5 4 | 3 2 1 0
0 0 1 1 0 0 0 1	0 0 0 0 0 0 0 0
First Byte	Second Byte

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	2	2	2	2

Instruction: CIM Copy interrupt mask

Description: (Acc_0 to Acc_3) ← Interrupt Mask

The four interrupt mask lines are placed in the least-significant bits of the current accumulator.

Coding:

7 6 5 4 | 3 2 1 0	7 6 5 4 | 3 2 1 0
0 0 1 1 0 0 0 1	0 0 1 0 0 0 0 0
First Byte	Second Byte

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	2	2	2	2

Instruction: IBD Interrupt block disable

Description: The interrupt system is disabled as a block.

Coding:

7 6 5 4 | 3 2 1 0	7 6 5 4 | 3 2 1 0
0 0 1 1 0 0 1 1	0 0 0 0 0 0 0 0
First Byte	Second Byte

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	2	2	2	2

Instruction: IBE Interrupt block enable

Description: The interrupt system is enabled as a block.

Coding:

7 6 5 4 | 3 2 1 0	7 6 5 4 | 3 2 1 0
0 0 1 1 0 0 1 1	0 0 1 0 0 0 0 0
First Byte	Second Byte

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	2	2	2	2

4.4.4 Teletype Controller Reserved Instructions

Device address 01 is reserved for the teletype controller.

Instruction: FUN Reset teletype controller

Description: I/O data bus ← (Acc_{LSByte})

The instruction places the teletype controller in the output buffer ready condition, halts the paper tape reader of the teletype and disables both teletype controller interrupt masks.

Coding:

7 6 5 4	3 2 1 0
0 0 1 1	0 0 1 1

First Byte

7 6 5 4	3 2 1 0
0 0 1 0	0 0 0 1

Second Byte

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	2	2	2	2

Instruction: FUN Start teletype paper tape reader

Description: I/O data bus ← (Acc_{LSByte})

Continuous paper tape motion is initiated in the paper tape reader of the teletype.

Coding:

7 6 5 4	3 2 1 0
0 0 1 1	0 0 1 1

First Byte

7 6 5 4	3 2 1 0
0 1 0 0	0 0 0 1

Second Byte

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	2	2	2	2

Instruction: FUN Enable teletype read interrupt

Description: I/O data bus ← (Acc_{LSByte})

The teletype controller read interrupt is enabled.

Coding:

7 6 5 4	3 2 1 0
0 0 1 1	0 0 1 1

First Byte

7 6 5 4	3 2 1 0
0 1 1 0	0 0 0 1

Second Byte

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	2	2	2	2

Instruction: FUN Enable teletype write interrupt

Description: I/O data bus ← (Acc_{LSByte})

The teletype controller write interrupt is enabled.

Coding:

7 6 5 4	3 2 1 0
0 0 1 1	0 0 1 1

First Byte

7 6 5 4	3 2 1 0
0 0 0 0	0 0 0 1

Second Byte

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	2	2	2	2

Instruction: FUN Read one character

Description: I/O data bus ← (Acc_{LSByte})

The paper tape reader of the teletype is advanced one character and stops on the following character.

Coding:

7 6 5 4	3 2 1 0
0 0 1 1	0 0 1 1

First Byte

7 6 5 4	3 2 1 0
1 1 0 0	0 0 0 1

Second Byte

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	2	2	2	2

Instruction: BTI Transfer teletype controller buffer to the C register

Description: (C_{LSByte}) ← (Teletype Controller Buffer)

The contents of the teletype controller buffer are transferred to the least-significant bits of the current accumulator.

Coding:

7 6 5 4	3 2 1 0
0 0 1 1	0 0 0 1

First Byte

7 6 5 4	3 2 1 0
0 0 0 0	0 0 0 1

Second Byte

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	2	2	2	2

Instruction: BTO Transfer C register to the teletype controller buffer

Description: (Teletype Controller Buffer) ← (C_{LSByte})

The contents of the least-significant bits of the current accumulator are transferred to the teletype controller buffer.

Coding:

7 6 5 4	3 2 1 0
0 0 1 1	0 0 0 0

First Byte

7 6 5 4	3 2 1 0
0 0 0 0	0 0 0 1

Second Byte

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	2	2	2	2

Instruction: SEN Sense teletype output buffer ready

Description: (P) ← (P) + 2 + 2 [if WRDY = 1]

If the teletype output-buffer-ready signal is true, the next two bytes in sequence are skipped.

Coding:

7 6 5 4	3 2 1 0
0 0 1 1	0 0 1 0

First Byte

7 6 5 4	3 2 1 0
0 0 1 0	0 0 0 1

Second Byte

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	3	3	3	3

Instruction: SEN Sense teletype input buffer ready

Description: (P) ← (P) + 2 + 2 [if RRDY = 1]

If the teletype input-buffer-ready signal is true, the next two bytes in sequence are skipped.

Coding:

7 6 5 4	3 2 1 0
0 0 1 1	0 0 1 0

First Byte

7 6 5 4	3 2 1 0
0 1 0 0	0 0 0 1

Second Byte

Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	3	3	3	3

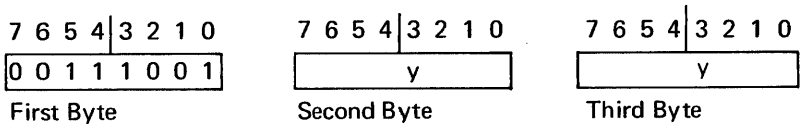
4.5 NON-MEMORY-REFERENCE, THREE-BYTE INSTRUCTIONS

Instruction: CSQ Change environmental status and load the noncurrent program counter

Description: (Q) ← y

The environment is changed. The noncurrent environment becomes the current operating environment. The last two bytes of the CSQ instruction are loaded into the location counter of the environment just becoming current.

Coding:



Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	3	3	3	3

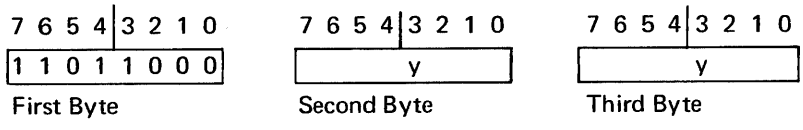
Instruction: BRM Branch and mark

Description: (y), (y + 1) ← (P) + 3

(P) ← y + 2

The program counter, after being incremented to the next instruction location, is placed in memory locations y and y + 1 specified by the BRM instruction. The address y + 2 is placed in the program counter.

Coding:



Timing:

Operand Precision	1 byte	2 bytes	3 bytes	4 bytes
Machine Cycles	6	6	6	6

5.1 INITIAL SETUP

Very little preparation of the 520/i is required before running an object program. Assuming that the system is properly installed and peripheral devices are correctly set for the required functions, perform the following steps:

a. Apply ac power to the computer.
b. Press the power ON switch on the control panel.
c. Manually load the basic bootstrap program from the control panel.
d. From the teletype punched-tape reader, load the binary loader program.
e. From the teletype punched-tape reader, load the required binary object program(s).
f. Press the RUN switch on the control panel.

5.2 OPERATING STEPS

This section presents summaries of operating steps for loading various programs into the 520/i memory. These include:

a. Basic bootstrap program, Table 5-1.
b. Binary loader program, Table 5-2.
c. Binary object program, Table 5-3.

The computer operator must decide the memory sector (1024 bytes) in which to load each program.

Where the operator is required to select a sector, an S character is shown in the address code. All codes are hexadecimal. Codes for S characters are given below:

Memory Sector	S Character Code
0	03
1	07
2	0B
3	0F
4	13
etc.	etc.

Many of the steps in Tables 5-1 through 5-3 require the operator to enter data into various registers of the 520/i using the control panel. Section 2.2 describes all front-panel controls and indicators.

Table 5-1. Summary of Basic Bootstrap Program Loading Steps

Step	Description
1	Set P register to S97.
2	Manually load 14 memory bytes:

Set MA register	Set M register
S97	31
S98	01
S99	78

Step	Description	
	Set MA register	Set M register
	S9A	FF
	S9B	23
	S9C	33
	S9D	33
	S9E	41
	S9F	32
	SA0	41
	SA1	F3
	SA2	9F
	SA3	F3
	SA4	97

Table 5-2. Summary of Binary Loader Program Loading Steps

Step	Description
1	Set P register to S9D.
2	Set X register to X00.
3	Position binary loader tape with first character over read station.
4	Press RUN switch.
5	Verify computer halt with P register set to SA8.

Table 5-3. Summary of Binary Object Program Operating Steps

Step	Description
1	Set Q register to SF6.
2	Set B register to 0000 to load and halt; to a positive value to load and execute.
3	Set P register to SA8.
4	Position object-tape blank leader over read station.
5	Press RUN switch.
6	Verify that computer does not halt with P register set to SE0 due to a check-sum error. If a check-sum error occurs, perform steps 7 and 8.
7	Reposition beginning of present tape record over read station.
8	Press RUN switch.

6.1 GENERAL

The 520/i has three basic methods for transferring data to and from external devices:

a. Eight-bit program-controlled data transfer to and from the accumulator.
b. Sixteen-bit program-controlled data transfer to and from the accumulator.
c. Eight-bit direct memory access.

The standard 520/i is equipped with the eight-bit program-controlled data-transfer capability and the ability to accommodate direct-memory-access devices. The 16-bit program controlled channel is optional.

6.2 PRIORITY INTERRUPTS

The priority-interrupt system of the 520/i computer permits rapid response to a variety of external stimuli.

System devices can use the interrupt system to signal alarm conditions, to mark time of day or to alert the central processor for data transfers. In this way, central processor time is used more efficiently than if a program is used to sense device readiness.

6.2.1 Priority Levels

There are eleven interrupt lines in the I/O cable as shown in Figure 6-1. Line 0 has the highest priority.

Lines 3 to 10 all have the same hardware priority, and comprise external interrupt number 3. The programmer assigns priorities within this group by copying the eight interrupt lines into the accumulator (by a copy-interrupt-status command) and determining the interrupting device.

The interrupt system is disabled as a block when power is first applied, when the RESET switch on the front panel is activated, when the central processor executes a CST or CSQ instruction changing modes into the noninterruptable environment, or when the processor executes an IBD instruction disabling the interrupt system.

Individual interrupts are enabled or disabled with the execution of a modify-interrupt instruction (BTO with device address 00).

6.2.2 Central Processor Response

An interrupt, if enabled and if no interrupt of higher priority is present, is acted upon when the central processor completes the current instruction. The interrupt causes the program sequence to be modified by directing the central processor to a fixed memory location where a single instruction is located.

Memory locations for the hard-wired interrupts are given in Table 6-1.

6.3 EIGHT-BIT PROGRAM-CONTROLLED INPUT/OUTPUT

The basic machine provides five types of I/O operations:

a. Sense – The status of a selected peripheral controller sense line is interrogated by the 520/i under program control.
b. Function control – A control code is transferred under program control to a peripheral controller.
c. Byte transfer in – A single byte of data is transferred under program control from a peripheral controller to the least-significant eight bits of the current accumulator.
d. Byte transfer out – A single byte of data is transferred under program control to a peripheral controller from the least-significant eight bits of the current accumulator.
e. Interrupt – A peripheral controller transmits an interrupt request to the 520/i to initiate special program subroutines.

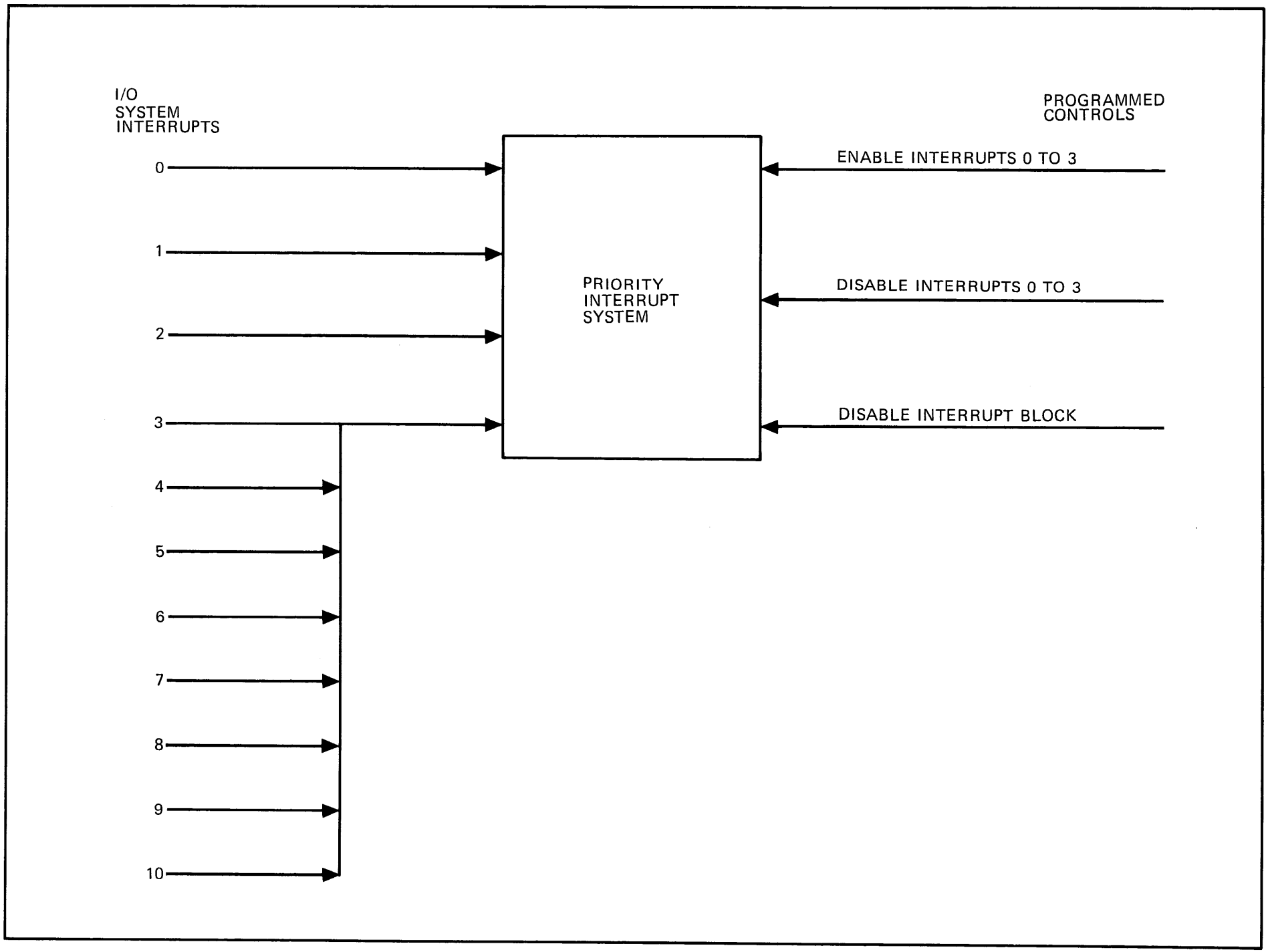


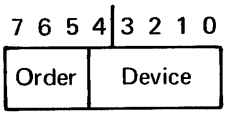
Figure 6-1. Interrupt Configuration.

Table 6-1. Central Processor Interrupt Addresses

Interrupt	Address (Hexadecimal)
Internal power-fail interrupt (optional)	000
Internal parity-error interrupt (optional)	004
External interrupt line 0	008
External interrupt line 1	00C
External interrupt line 2	010
External interrupt lines 3 to 10	014

All of the I/O instructions have an associated order code and device address that are transmitted on an eight-bit address bus to the external devices.

The format is:



Each device uses a unique device address, bits 0 to 4, with up to 32 device addresses possible. Bits 0 to 7 identify the function to be performed or in some other way qualify the I/O command.

6.3.1 Interface

The standard I/O bus consists of a data bus, address bus, interrupt bus and six control lines.

The data bus is an eight-bit, parallel, bidirectional I/O channel. It is used to transmit data from the computer to peripheral devices. In turn the bus is used by these devices to transmit data to the computer. A total of 10 drivers and 10 receivers may be connected to each output. Data bus mnemonics are ED00 to ED07.

The address bus is an eight-bit output bus. It is used to transmit device address and order code to the peripheral device. Five bits determine device address and three bits specify up to eight control functions or sense inquiries. A total of 10 receivers may be connected to each output. Address bus mnemonics are EA00- to EA07-.

The interrupt bus consists of 11 interrupt lines. Highest priority is assigned by hardware to three lines (EI00-, EI01-, and EI02-). The eight remaining lines are assigned priority by software. Interrupt receivers may be driven by up to 10 drivers. Interrupt bus mnemonics are EI00- to EI11-.

Control signals FUNS-, SENS-, BTIS- and BTOS- are generated during computer-initiated I/O functions. They are mutually exclusive and determine which of four operations is in process. Internal gating provides a nominal signal duration of 500 nanoseconds. The four signals are defined as follows:

FUNS-	Functional control.
SENS-	Sense external device.
BTIS-	Byte transfer in.
BTOS-	Byte transfer out.

Control signal SERPS- is an affirmative sense response. The receiver for this signal may be driven by up to 10 drivers.

Control signal RSTS- is true during the period in which the console RESET switch is pressed. This signal may drive up to 10 receivers.

The line drivers and receivers used on the 520 i I/O bus enable a "wired-OR" interconnection. This feature is functional only if negative logic is used at the "wired-OR" junction. Negative logic in this sense refers to a signal with a ONE value near ground and a ZERO value in excess of 2.4 volts. Consequently, all signals on the I/O bus are complements of signals used in the 520/i and the peripheral equipment. For example, if two sense responses are to be combined to notify the computer that a sense response has occurred, they are first inverted:

Sense Response 1 becomes $\overline{\text{Sense Response 1}}$

Sense Response 2 becomes $\overline{\text{Sense Response 2}}$

Then they are connected to the I/O bus:

$\overline{\text{Sense Response 1}} \cdot \overline{\text{Sense Response 2}}$

(In positive logic, interconnection performs a logical AND operation.)

Finally, they are reinverted in the 520/i:

$\overline{\overline{\text{Sense Response 1}} \cdot \overline{\text{Sense Response 2}}}$

This is equivalent to:

Sense Response 1 + Sense Response 2

This results in the desired function.

Logic sense in 520/i conventions is represented by the use of "+" and "-" signs. A logic ONE signal is represented as: SIGNAL+ or SIGNAL. Its complement is represented as SIGNAL-

Since all signals on the I/O bus are complements, their mnemonics are followed by a "-" sign.

6.3.2 Applications

The 520/i eight-bit I/O channel is designed to provide efficient and flexible communications with peripheral equipment. Numerous external devices can be controlled with a minimum of control logic.

The application examples that follow depict typical situations encountered in the control of peripheral devices. It is assumed that the device controllers interface with the 520/i eight-bit I/O channel using drivers and receivers compatible with those found in the 520/i.

In the illustrations following, all line drivers are driven by open-collector TTL NAND gates. Other logic elements may be DTL circuits if the number of gate delays does not exceed those shown in the examples. If a design requires more gate delays, it is suggested that TTL circuits be used.

All timing requirements stated assume a 30-foot cable is to be driven. If shorter cables are used, minimum times may be increased by 3.3 nanoseconds per foot for each foot of cable length less than 30 feet.

Sense status of external device. The status of an external device is interrogated by the use of a SEN instruction. The least-significant part of the address portion of the instruction determines which of 31 devices is to be interrogated. One of the eight sense functions is selected by coding the most-significant part of the address portion of the instruction.

The logic for the sense function for a typical controller is shown in Figure 6-2. The address portion of the instruction precedes the SENS- signal by at least 125 nanoseconds at the output of the receivers. The SENS- signal has a minimum duration of 400 nanoseconds and a maximum duration of 600 nanoseconds at the output of the receiver. The sense response (SERPS-) must be applied to the NAND gate feeding the driver within 750 nanoseconds of the receipt of SENS- signal from the receiver. The sense response must have a minimum duration of 200 nanoseconds with a maximum duration of 1 microsecond.

Timing requirements are shown in Figure 6-4.

The circuit of Figure 6-2 satisfies these conditions by using SENS+ to strobe the sense response. This provides a minimum delay and controls the sense response duration.

Figure 6-2 also shows the decoding of a typical address. This function, ADDR, is used in other illustrations.

External control function. Control signals are applied to external devices using the FUN instruction. The least significant part of the address portion of the instruction determines which of 3 external devices is to receive the control signal. One of eight control functions can be selected by coding the most-significant part of the address portion of the instruction.

The logic for a typical control function is shown in Figure 6-3. The address portion of the instruction precedes the FUNS- signal by at least 125 nanoseconds at the output of the receivers. The FUNS- signal has a minimum duration of 400 nanoseconds and a maximum duration of 600 nanoseconds.

The circuit of Figure 6-3 uses the FUNS- signal to control the duration of the control signal. If a greater duration is required, the FUNS- signal may be used to set a flip-flop.

Timing requirements are shown in Figure 6-5.

Data transfer output operations. Data are transferred from the computer to a peripheral device by means of a BTO instruction. Data are transmitted along data bus lines ED00- to ED07-. The operation is recognized as an output transfer by the presence of the BTOS- signal. The address portion of the instruction determines the peripheral device to receive the data. The most-significant three bits of the address portion of the instruction may be used to distinguish several types of output bytes to a single device.

The logic to implement a data transfer for a typical situation is shown in Figure 6-6. The address portion of the instruction precedes the BTOS- signal by at least 125 nanoseconds at the output of the receivers. Data are present at the receivers at least 140 nanoseconds before BTOS-. The BTOS- signal is at least 400 nanoseconds but not more than 600 nanoseconds in duration. Data are present at the receivers for a minimum of 900 nanoseconds. These timing conditions are shown in Figure 6-8.

The circuit of Figure 6-6 applies the data directly into the inputs of "type D" flip-flops. BTOS- is gated with the address and is used as a clock. In this configuration, the flip-flops present the new data within 240 nanoseconds of the receipt of BTOS- (assuming TTL flip-flops). The complement of the clock may be used as a data ready signal.

A typical application of the RSTS- signal is shown in Figure 6-8. The signal can be "ORed" with a signal from the peripheral device. This enables the register to be reset by the 520/i or by the peripheral device.

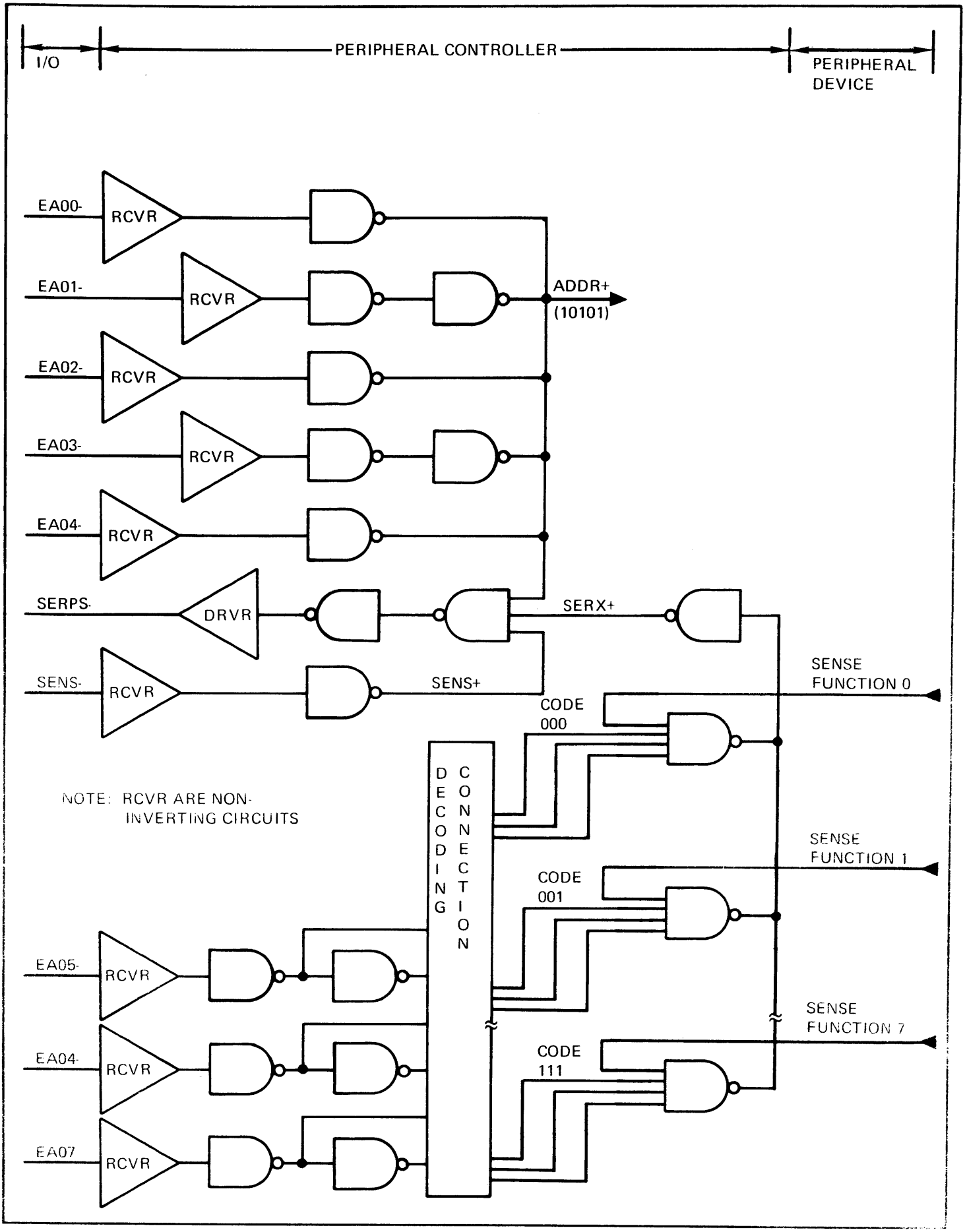


Figure 6-2. Typical Sense Logic

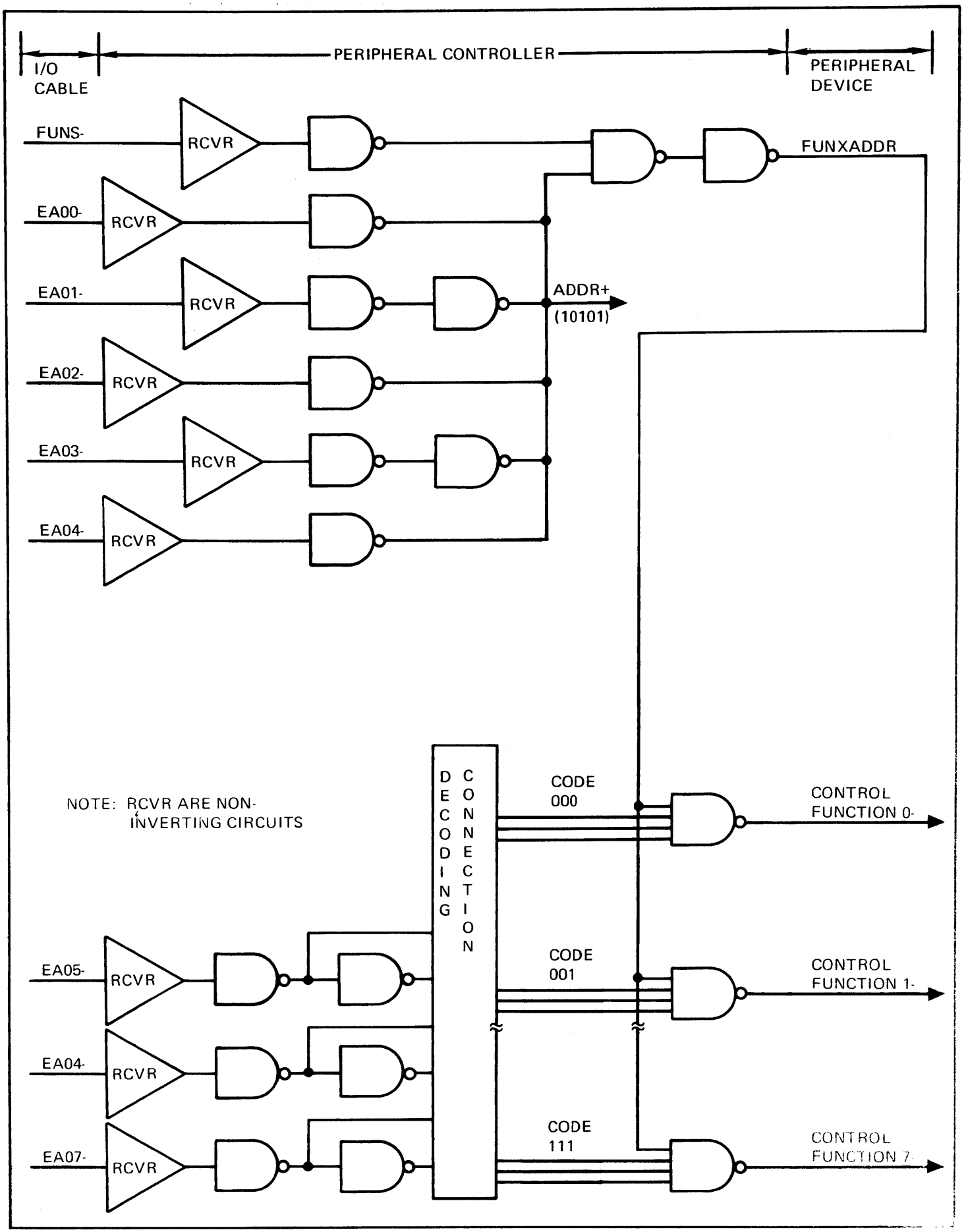


Figure 6-3. Typical Function Control Logic

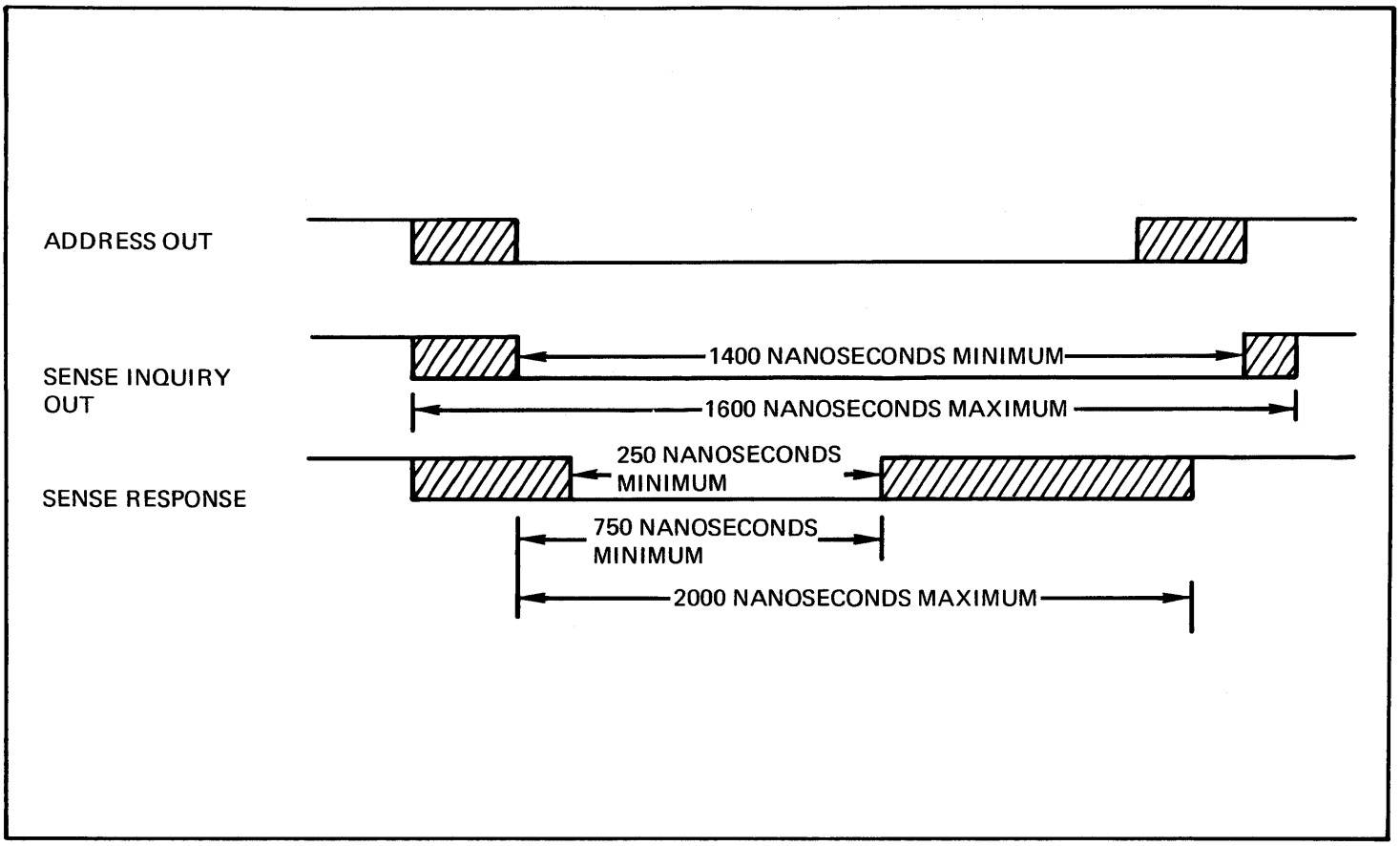


Figure 6-4. External Sense Timing

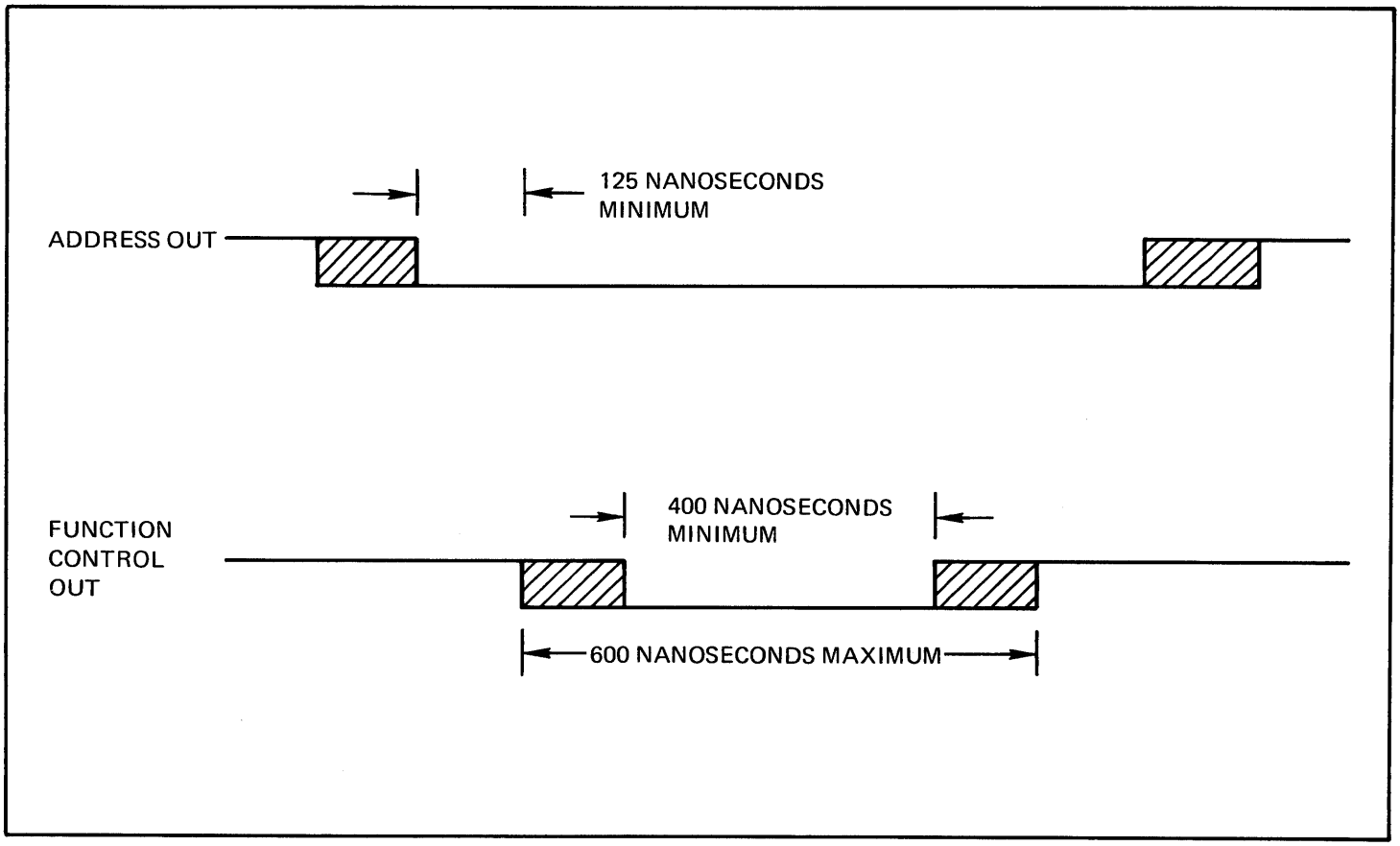


Figure 6-5. External Function Control Timing

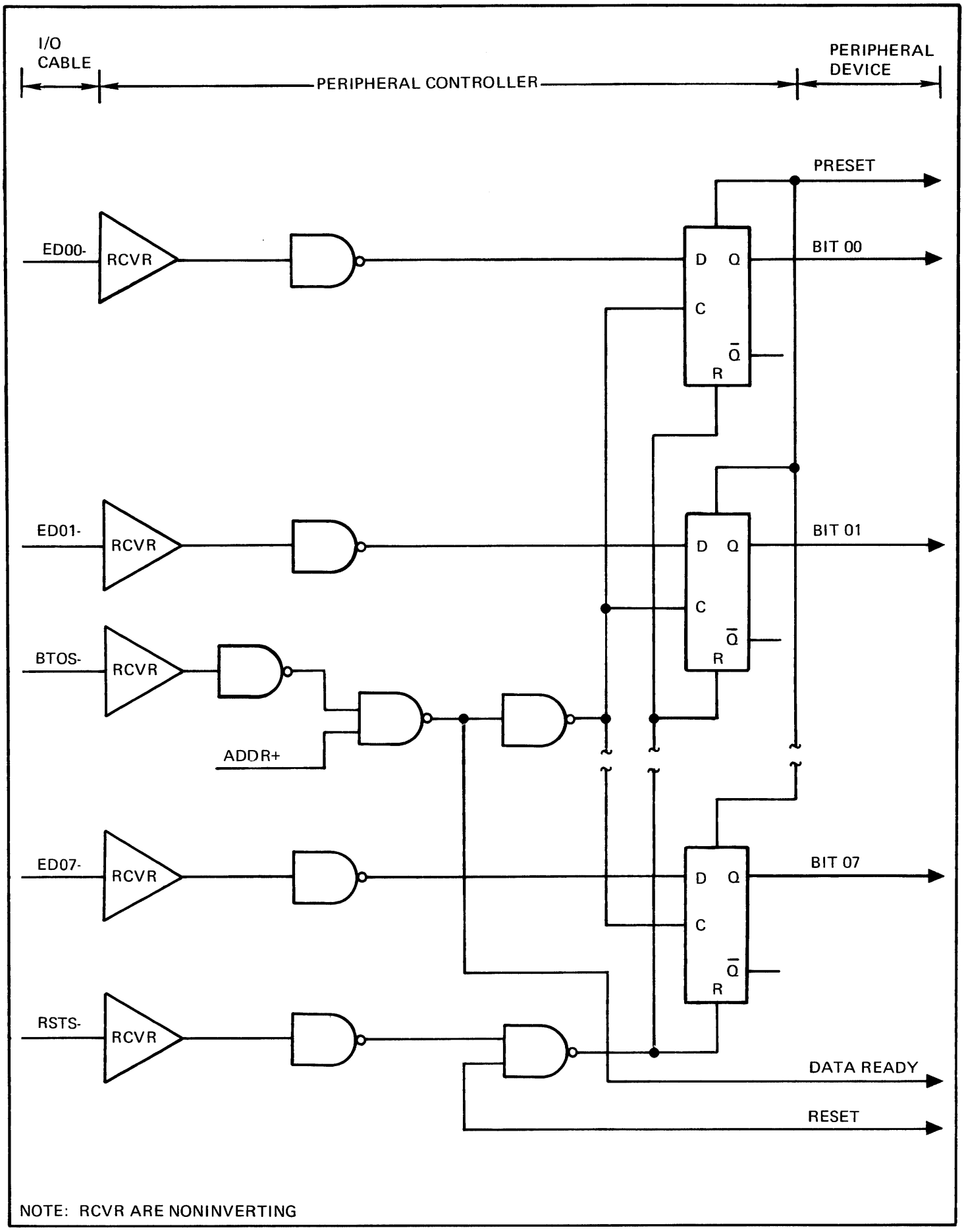


Figure 6-6. Typical Data Transfer Output Logic

Data transfer input operations. Data are transferred from a peripheral device to the computer by means of a BTI instruction. Data are transmitted along data bus lines ED00- to ED07-. The operation is recognized as an input transfer by the presence of the BTIS- signal. The address portion of the instruction determines the peripheral device to send the data. The most-significant three bits of the address portion of the instruction may be used to distinguish several types of input bytes from a single device.

The logic to implement a data transfer for a typical situation is shown in Figure 6-7. The address portion of the instruction precedes the BTIS- signal by at least 125 nanoseconds at the output of the receivers. The BTIS- signal is at least 400 nanoseconds but not more than 600 nanoseconds in duration. Data must be present at the drivers until the end of the BTIS- signal. The leading edge of data at the drivers should occur no later than 110 nanoseconds after the leading edge of BTIS.

Timing requirements are shown in Figure 6-9.

The logic of Figure 6-7 presumes that data were ready in the peripheral devices before the BTI instruction. Either the computer was informed that data were ready by an affirmative sense response or an interrupt, or the computer readied the data by means of a function control instruction. The timing requirements are satisfied by using the BTIS+ signal as a strobe.

Interrupt operations. Eleven interrupts are available on the 520/i I/O bus. Three of these (EI00-, EI01-, EI02-) are assigned priority by hardware with EI00- having the highest priority. The remaining eight interrupts (EI03- to EI10-) have been assigned equal priority by hardware but with a priority status lower than EI02-. Priority among the eight low-priority interrupts is assigned by software.

Figure 6-10 shows typical uses of interrupts. Interrupt A is the usual connection with the interrupt driver connected directly to the interrupt source.

The NAND gate used at the input to the driver provides an opportunity to logically OR two interrupt sources as shown at B. Interrupt C is the logical AND of two interrupt sources. The interrupt shown at D is a logical OR of two interrupt sources from two separate controllers.

Interrupts may be raised at any time but must persist until reset by a response from the computer in the form of a FUN, BTO or BTI instruction.

6.4 SIXTEEN-BIT PROGRAM CONTROLLED INPUT/OUTPUT

The basic block diagram, Figure 1-1, shows the use of the optional 16-bit I/O channel. The 16-bit channel includes a buffer register that is loaded from the accumulator for output and unloaded into the accumulator for input as shown in Figure 6-11. A register-change instruction recognizes the 16-bit buffer as a source or destination register for data transfers.

Once a word is transferred into the accumulator, it may be stored, modified or transferred to another device. For store or modify operations, the accumulator precision must be adjusted to 16 bits.

6.4.1 Sense-Loop Transfer

The maximum 16-bit transfer rate is 37,000 words per second. Sense loop transfer with 16-bit devices is like that with the eight-bit I/O, except for additional register transfer and two-byte precision in the accumulator.

6.4.2 Interface

The following lines are found on the 16-bit I/O channel:

16 bidirectional data and address lines.

1 control line out.

1 sense response.

Timing on the 16-bit I/O channel is shown in Figure 6-12.

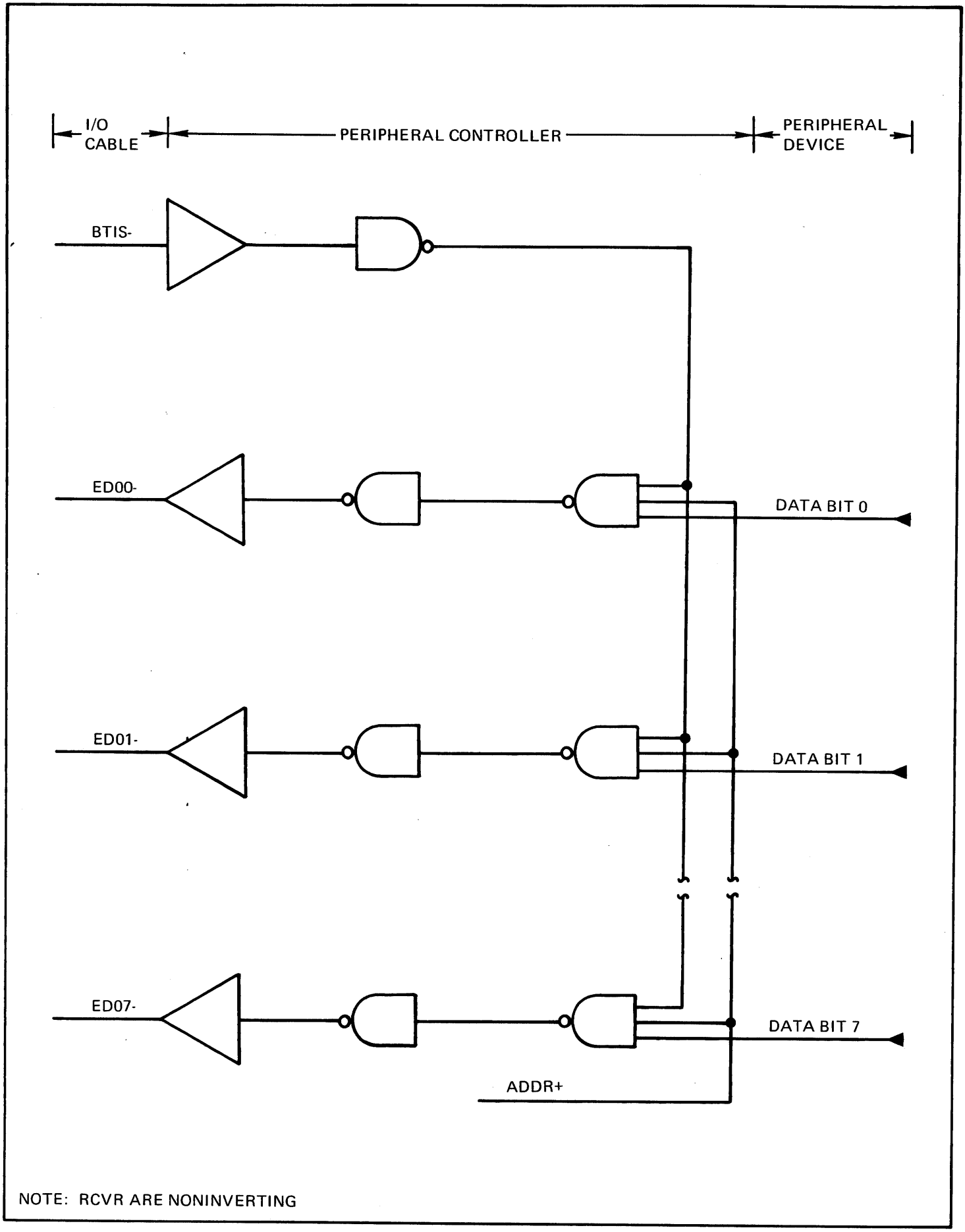


Figure 6-7. Typical Data Transfer Input Logic

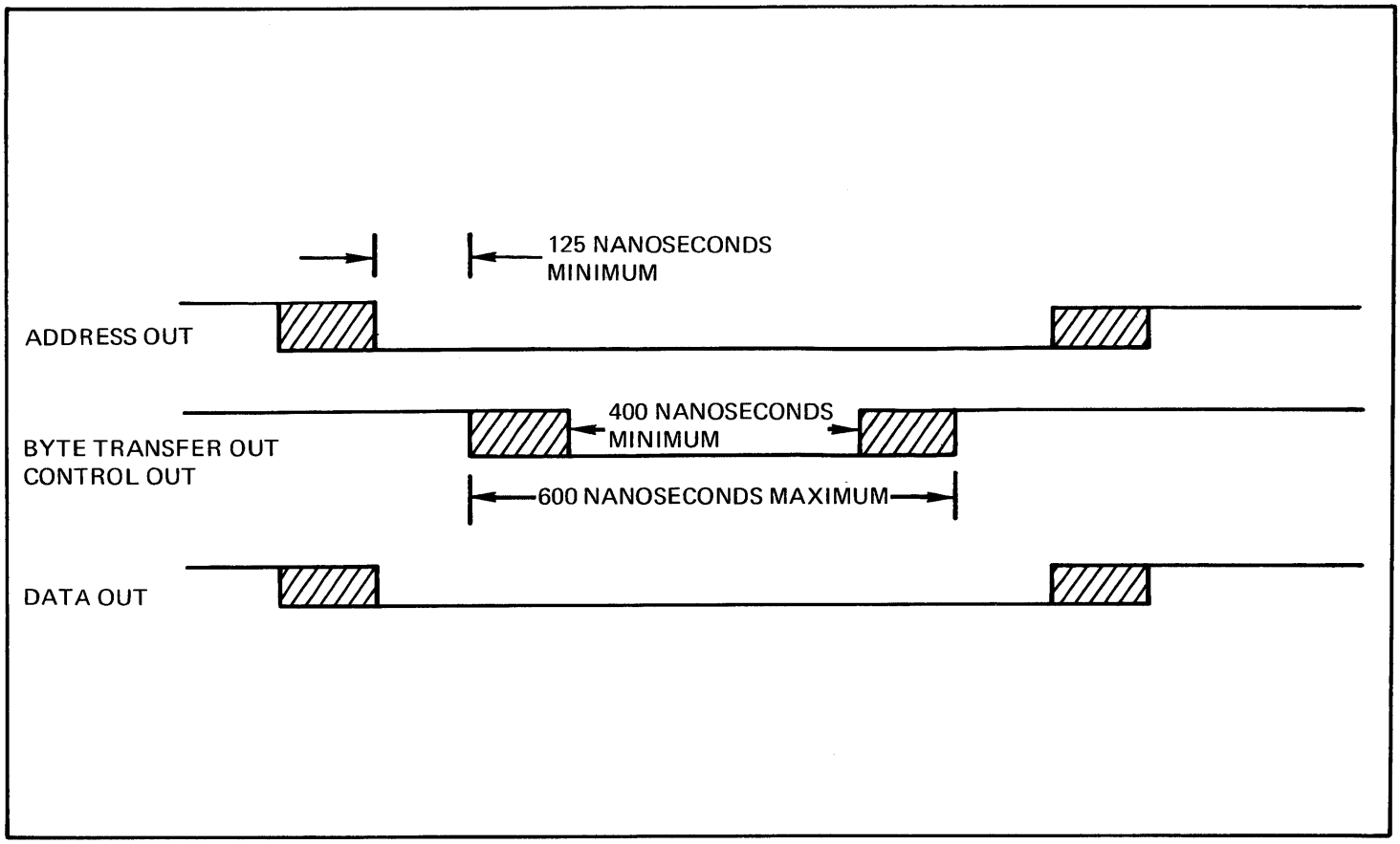


Figure 6-8. Data Transfer Output Timing

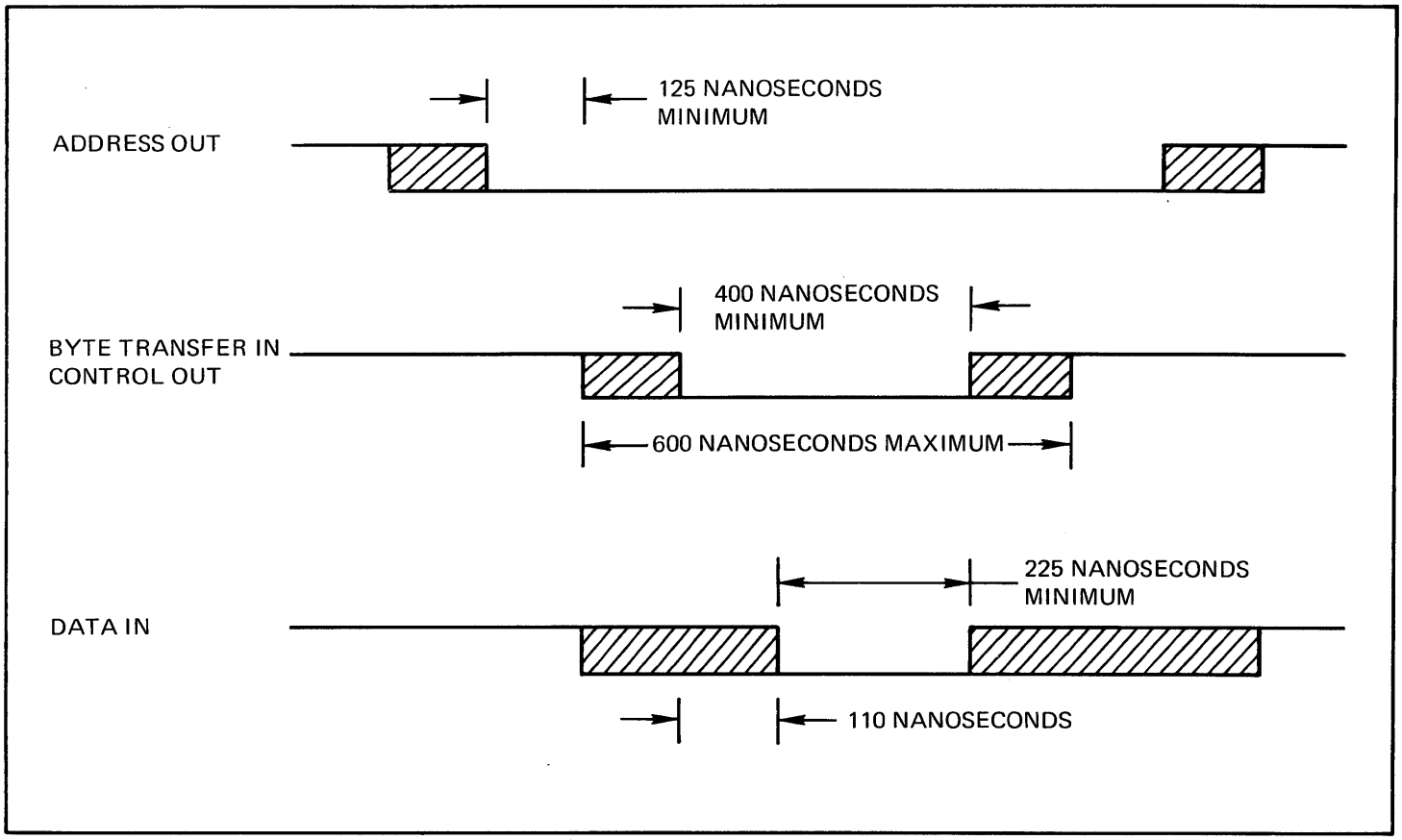


Figure 6-9. Data Transfer Input Timing

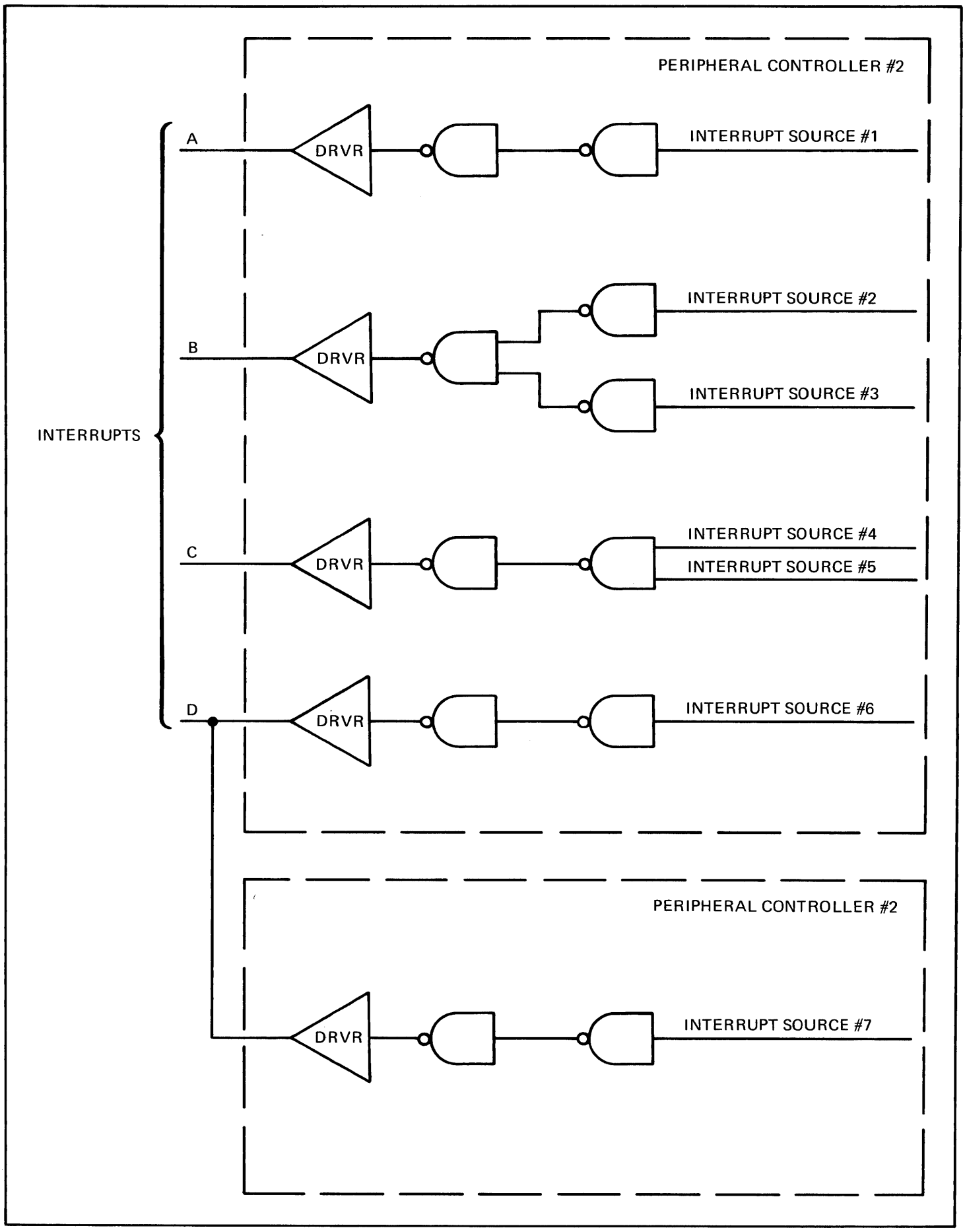


Figure 6-10. Typical Interrupt Applications

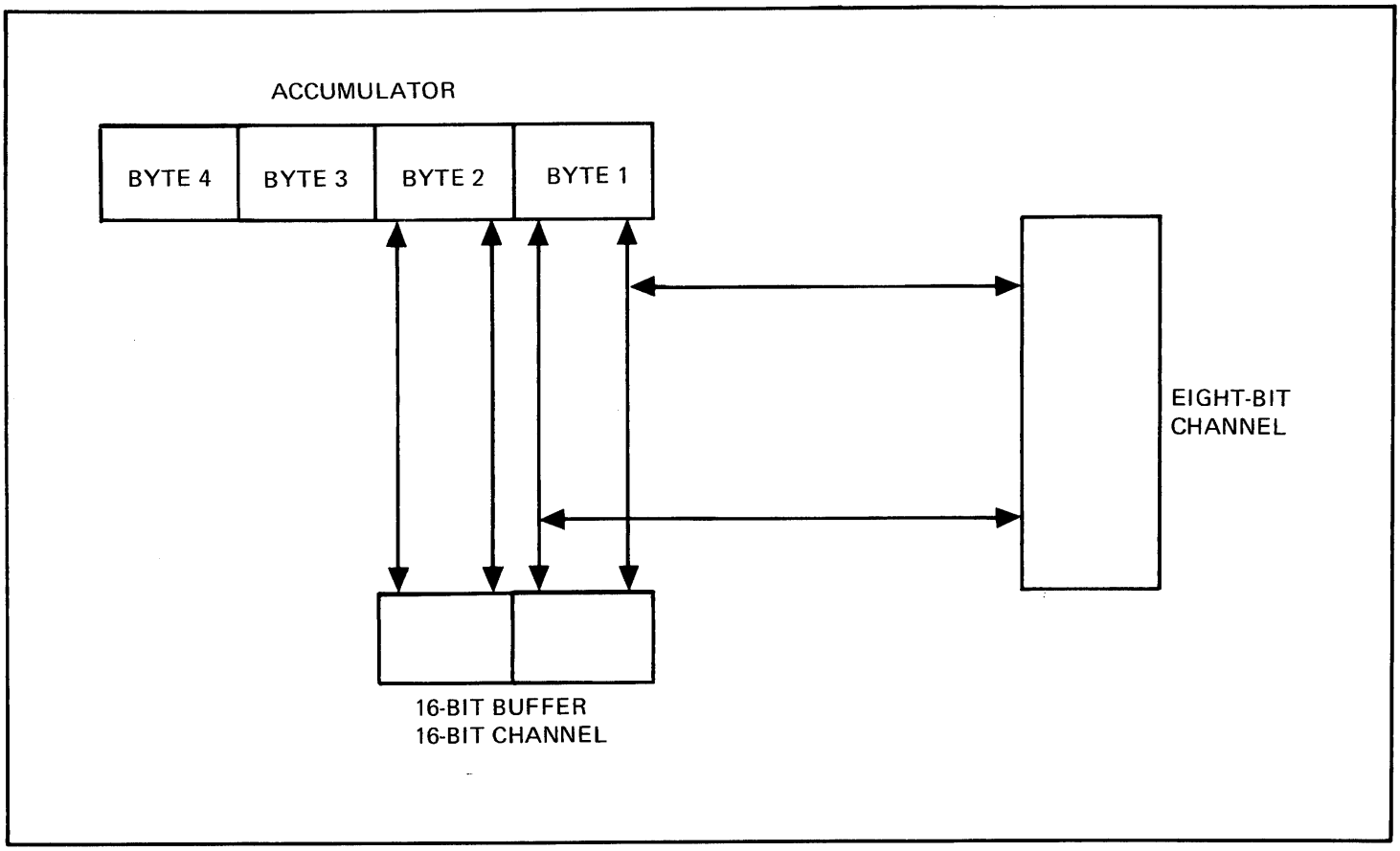
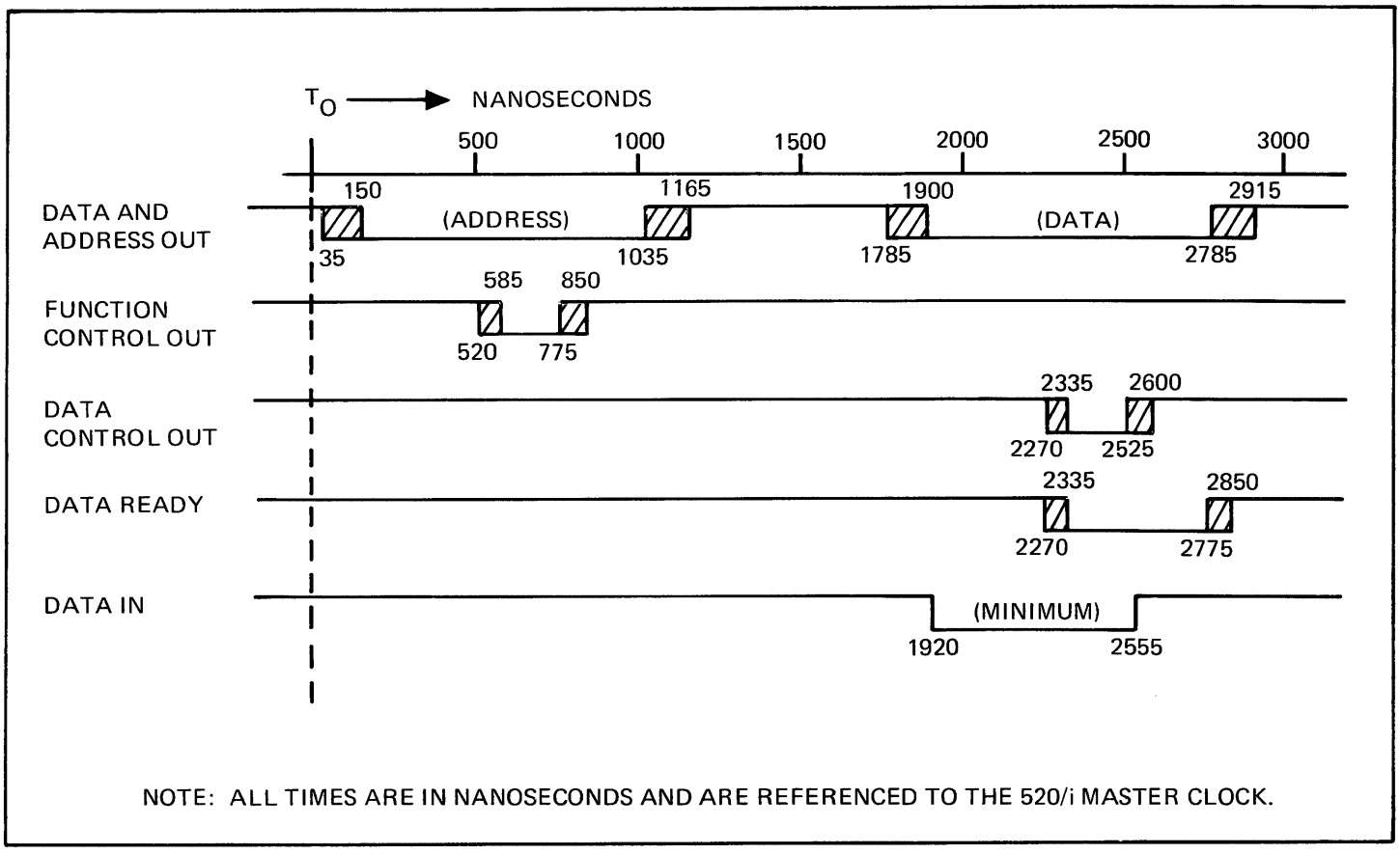


Figure 6-11. Simplified 16-Bit I/O Channel



NOTE: ALL TIMES ARE IN NANOSECONDS AND ARE REFERENCED TO THE 520/i MASTER CLOCK.

Figure 6-12. Timing on the 16-Bit I/O Channel

6.5 DIRECT MEMORY ACCESS PORT

The direct memory access (DMA) port of the 520/i computer provides a means for external equipment to interrupt the central processor and initiate a memory operation without disturbing the operational registers. The interrupted program continues at the conclusion of the DMA data transfer.

The DMA port permits data transfers to and from external equipment at rates up to 666,000 bytes per second. This operation is ideally suited for high-speed data transfers by magnetic tape or disc units, or from data sampling units.

Characteristics of the DMA port are:

a. The external mechanism using this facility can operate asynchronously with feedback control signals.
b. The external mechanism provides memory addresses.
c. The external mechanism can use consecutive memory cycles for a high data-burst rate.

There are three options available to the customer as to how to use the DMA port:

a. The customer uses the vacant slot in the computer to build his own DMA requesting logic on his own logic board. Varian Data Machines provides information as to the capabilities, restrictions and limitations of connecting directly to the internal computer bus structure.
b. The customer purchases from Varian Data Machines a general-purpose socket board that plugs into the vacant slot. Varian Data Machines provides the same information as in option a.
c. The customer purchases the 520/i DMA port line driver and receiver required to locate the customer's DMA requesting device external to the 520/i option module main frame. Varian Data Machines provides information on how to connect to these drivers and receivers.

6.5.1 Operation

An external device using the DMA port must provide address, data and control signals compatible with the 520/i logic.

The DMA port may operate in one of two modes, depending on the data transfer rate of external equipment. For external equipment operating at less than 93,000 bytes per second, a DMA request sent to the 520/i is acknowledged at the completion of the instruction in process. The external device then provides address and data words (if required). Either the external data word is then stored or an accessed word is transferred to the external device. The maximum access rate is determined by the instruction with the longest execution time. For most programs, the worst-case instruction execution time is about nine microseconds, giving the following maximum access rates:

One external device	= 93,000 bytes per second.
Two devices operating together	= 81,500 bytes per second.
Three devices operating together	= 73,000 bytes per second.
Four devices operating together	= 65,500 bytes per second.

For external equipment operating at greater than 93,000 bytes per second, an I/O command from the 520/i is sent to the requesting external device before data transfer is started. The I/O command sustains the DMA request signal throughout the data transfer. At the completion of the data transfer, the DMA request signal is made inactive allowing the interrupted program to continue. In this way, every memory cycle during the data transfer is reserved for DMA, giving the following maximum access rates:

One external device	= 660,000 bytes per second.
Two devices operating together	= 333,000 bytes per second.
Three devices operating together	= 222,000 bytes per second.
Four devices operating together	= 167,000 bytes per second.

When a DMA request and an interrupt require a response from the 520/i at the completion of the same instruction, the following holds true:

a. A power-fail interrupt has priority over a DMA request. In addition, a DMA data transfer is always interrupted by a power-fail interrupt at the end of the data access in process.
b. A DMA request has priority over all interrupts other than power fail. A DMA data transfer in process cannot be interrupted by interrupts other than power fail. If the 520/i includes a parity option, parity error detection is inhibited during a DMA operation. Parity is formed when writing data into memory, but is not checked when accessing memory.

Binary numbers in the 520/i may have a precision of eight bits, 16 bits, 24 bits or 32 bits. In each case, the most-significant bit is the sign bit. A sign bit of ZERO denotes a positive number; a sign bit of ONE denotes a negative number. The negative of a positive number is represented in 2's-complement form.

The 2's complement of a number may be found in either of two ways:

a. Take the 1's complement of the number (complement each bit) and add 1 to the result. Example:

number	0 0 0 0 1 0 0 1	(+9)
1's complement	1 1 1 1 0 1 1 0	
	+ 1	
2's complement	1 1 1 1 0 1 1 1	(-9)

b. For an n-bit number (including the sign bit), subtract the number from $2^{(n+1)}$. Example:

$2^{(n+1)}$	1 0 0 0 0 0 0 0 0
-(+9)	- 0 0 0 0 1 0 0 1
-9	1 1 1 1 0 1 1 1

It is generally convenient to express binary numbers by their hexadecimal equivalent. This conversion is easily performed by grouping the binary bits in fours, starting with the least-significant bit. In this way, numbers with an eight-bit precision may be expressed by only two hexadecimal digits (0 0 to F F). For the maximum machine precision, only eight hexadecimal digits are required.

The range of numbers in the 510/i is from $-2^{(31)}$ to $2^{(31)}$ -1. The numbers zero, minus 1, and plus and minus full scale are shown below.

Decimal	Hexadecimal
2,147,483,647 (+full scale)	7 F F F F F F F
0	0 0 0 0 0 0 0 0
-1	F F F F F F F F
-2,147,483,648 (-full scale)	8 0 0 0 0 0 0 0

In performing addition or subtraction, it is possible for the result to exceed the full-scale range of the machine. For example:

Decimal	Hexadecimal
83	53
+79	+4F
162	A2 (-94)

The negative hexadecimal result is in error. The same type of error occurs when the sum of two negative numbers exceeds the negative full-scale range:

Decimal	Hexadecimal
-83	AD
(+)-79	+B1
-162	(1) 6E (+110)

The carry bit out of the most significant data position is lost; however, to inform the programmer that the result of the operation is outside the range of the set precision, an overflow indicator is provided (in each environment). The overflow indicator is set if the sign bit changes when two numbers of the same sign are added.

Table B-3 presents direct conversions between hexadecimal integers 0 0 0 to F F F and decimal integers 0 0 0 0 to 4 0 9 5. For conversion of larger integers, Table B-2 presents values that may be added to those of Table B-3. Table B-4 presents direct conversions between hexadecimal and decimal fractions.

Table B-2. Hexadecimal/Decimal Large Integer Conversions

Hexadecimal	Decimal	Hexadecimal	Decimal
01 000	4 096	20 000	131 072
02 000	8 192	30 000	196 608
03 000	12 288	40 000	262 144
04 000	16 384	50 000	327 680
05 000	20 480	60 000	393 216
06 000	24 576	70 000	458 752
07 000	28 672	80 000	524 288
08 000	32 768	90 000	589 824
09 000	36 864	A0 000	655 360
0A 000	40 960	B0 000	720 896
0B 000	45 056	C0 000	786 432
0C 000	49 152	D0 000	851 968
0D 000	53 248	E0 000	917 504
0E 000	57 344	F0 000	983 040
0F 000	61 440	100 000	1 048 576
10 000	65 536	200 000	2 097 152
11 000	69 632	300 000	3 145 728
12 000	73 728	400 000	4 194 304
13 000	77 824	500 000	5 242 880
14 000	81 920	600 000	6 291 456
15 000	86 016	700 000	7 340 032
16 000	90 112	800 000	8 388 608
17 000	94 208	900 000	9 437 184
18 000	98 304	A00 000	10 485 760
19 000	102 400	B00 000	11 534 336
1A 000	106 496	C00 000	12 582 912
1B 000	110 592	D00 000	13 631 488
1C 000	114 688	E00 000	14 680 064
1D 000	118 784	F00 000	15 728 640
1E 000	122 880	1 000 000	16 777 216
1F 000	126 976	2 000 000	33 554 432

Table B-1. Binary/Hexadecimal/Decimal Conversions

Binary	Hexadecimal	Decimal
0000	0	0
0001	1	1
0010	2	2
0011	3	3
0100	4	4
0101	5	5
0110	6	6
0111	7	7
1000	8	8
1001	9	9
1010	A	10
1011	B	11
1100	C	12
1101	D	13
1110	E	14
1111	F	15

Table B-3. Hexadecimal/Decimal Integer Conversions

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
000	0000	0001	0002	0003	0004	0005	0006	0007	0008	0009	0010	0011	0012	0013	0014	0015
010	0016	0017	0018	0019	0020	0021	0022	0023	0024	0025	0026	0027	0028	0029	0030	0031
020	0032	0033	0034	0035	0036	0037	0038	0039	0040	0041	0042	0043	0044	0045	0046	0047
030	0048	0049	0050	0051	0052	0053	0054	0055	0056	0057	0058	0059	0060	0061	0062	0063
040	0064	0065	0066	0067	0068	0069	0070	0071	0072	0073	0074	0075	0076	0077	0078	0079
050	0080	0081	0082	0083	0084	0085	0086	0087	0088	0089	0090	0091	0092	0093	0094	0095
060	0096	0097	0098	0099	0100	0101	0102	0103	0104	0105	0106	0107	0108	0109	0110	0111
070	0112	0113	0114	0115	0116	0117	0118	0119	0120	0121	0122	0123	0124	0125	0126	0127
080	0128	0129	0130	0131	0132	0133	0134	0135	0136	0137	0138	0139	0140	0141	0142	0143
090	0144	0145	0146	0147	0148	0149	0150	0151	0152	0153	0154	0155	0156	0157	0158	0159
0A0	0160	0161	0162	0163	0164	0165	0166	0167	0168	0169	0170	0171	0172	0173	0174	0175
0B0	0176	0177	0178	0179	0180	0181	0182	0183	0184	0185	0186	0187	0188	0189	0190	0191
0C0	0192	0193	0194	0195	0196	0197	0198	0199	0200	0201	0202	0203	0204	0205	0206	0207
0D0	0208	0209	0210	0211	0212	0213	0214	0215	0216	0217	0218	0219	0220	0221	0222	0223
0E0	0224	0225	0226	0227	0228	0229	0230	0231	0232	0233	0234	0235	0236	0237	0238	0239
0F0	0240	0241	0242	0243	0244	0245	0246	0247	0248	0249	0250	0251	0252	0253	0254	0255

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
100	0256	0257	0258	0259	0260	0261	0262	0263	0264	0265	0266	0267	0268	0269	0270	0271
110	0272	0273	0274	0275	0276	0277	0278	0279	0280	0281	0282	0283	0284	0285	0286	0287
120	0288	0289	0290	0291	0292	0293	0294	0295	0296	0297	0298	0299	0300	0301	0302	0303
130	0304	0305	0306	0307	0308	0309	0310	0311	0312	0313	0314	0315	0316	0317	0318	0319
140	0320	0321	0322	0323	0324	0325	0326	0327	0328	0329	0330	0331	0332	0333	0334	0335
150	0336	0337	0338	0339	0340	0341	0342	0343	0344	0345	0346	0347	0348	0349	0350	0351
160	0352	0353	0354	0355	0356	0357	0358	0359	0360	0361	0362	0363	0364	0365	0366	0367
170	0368	0369	0370	0371	0372	0373	0374	0375	0376	0377	0378	0379	0380	0381	0382	0383
180	0384	0385	0386	0387	0388	0389	0390	0391	0392	0393	0394	0395	0396	0397	0398	0399
190	0400	0401	0402	0403	0404	0405	0406	0407	0408	0409	0410	0411	0412	0413	0414	0415
1A0	0416	0417	0418	0419	0420	0421	0422	0423	0424	0425	0426	0427	0428	0429	0430	0431
1B0	0432	0433	0434	0435	0436	0437	0438	0439	0440	0441	0442	0443	0444	0445	0446	0447
1C0	0448	0449	0450	0451	0452	0453	0454	0455	0456	0457	0458	0459	0460	0461	0462	0463
1D0	0464	0465	0466	0467	0468	0469	0470	0471	0472	0473	0474	0475	0476	0477	0478	0479
1E0	0480	0481	0482	0483	0484	0485	0486	0487	0488	0489	0490	0491	0492	0493	0494	0495
1F0	0496	0497	0498	0499	0500	0501	0502	0503	0504	0505	0506	0507	0508	0509	0510	0511
200	0512	0513	0514	0515	0516	0517	0518	0519	0520	0521	0522	0523	0524	0525	0526	0527
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7E0	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031
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BB0	2992	2993	2994	2995	2996	2997	2998	2999	3000	3001	3002	3003	3004	3005	3006	3007
BC0	3008	3009	3010	3011	3012	3013	3014	3015	3016	3017	3018	3019	3020	3021	3022	3023
BD0	3024	3025	3026	3027	3028	3029	3030	3031	3032	3033	3034	3035	3036	3037	3038	3039
BE0	3040	3041	3042	3043	3044	3045	3046	3047	3048	3049	3050	3051	3052	3053	3054	3055
BF0	3056	3057	3058	3059	3060	3061	3062	3063	3064	3065	3066	3067	3068	3069	3070	3071
C00	3072	3073	3074	3075	3076	3077	3078	3079	3080	3081	3082	3083	3084	3085	3086	3087
C10	3088	3089	3090	3091	3092	3093	3094	3095	3096	3097	3098	3099	3100	3101	3102	3103
C20	3104	3105	3106	3107	3108	3109	3110	3111	3112	3113	3114	3115	3116	3117	3118	3119
C30	3120	3121	3122	3123	3124	3125	3126	3127	3128	3129	3130	3131	3132	3133	3134	3135
C40	3136	3137	3138	3139	3140	3141	3142	3143	3144	3145	3146	3147	3148	3149	3150	3151
C50	3152	3153	3154	3155	3156	3157	3158	3159	3160	3161	3162	3163	3164	3165	3166	3167
C60	3168	3169	3170	3171	3172	3173	3174	3175	3176	3177	3178	3179	3180	3181	3182	3183
C70	3184	3185	3186	3187	3188	3189	3190	3191	3192	3193	3194	3195	3196	3197	3198	3199
C80	3200	3201	3202	3203	3204	3205	3206	3207	3208	3209	3210	3211	3212	3213	3214	3215
C90	3216	3217	3218	3219	3220	3221	3222	3223	3224	3225	3226	3227	3228	3229	3230	3231
CA0	3232	3233	3234	3235	3236	3237	3238	3239	3240	3241	3242	3243	3244	3245	3246	3247
CB0	3248	3249	3250	3251	3252	3253	3254	3255	3256	3257	3258	3259	3260	3261	3262	3263
CC0	3264	3265	3266	3267	3268	3269	3270	3271	3272	3273	3274	3275	3276	3277	3278	3279
CD0	3280	3281	3282	3283	3284	3285	3286	3287	3288	3289	3290	3291	3292	3293	3294	3295
CE0	3296	3297	3298	3299	3300	3301	3302	3303	3304	3305	3306	3307	3308	3309	3310	3311
CF0	3312	3313	3314	3315	3316	3317	3318	3319	3320	3321	3322	3323	3324	3325	3326	3327

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
D00	3328	3329	3330	3331	3332	3333	3334	3335	3336	3337	3338	3339	3340	3341	3342	3343
D10	3344	3345	3346	3347	3348	3349	3350	3351	3352	3353	3354	3355	3356	3357	3358	3359
D20	3360	3361	3362	3363	3364	3365	3366	3367	3368	3369	3370	3371	3372	3373	3374	3375
D30	3376	3377	3378	3379	3380	3381	3382	3383	3384	3385	3386	3387	3388	3389	3390	3391
D40	3392	3393	3394	3395	3396	3397	3398	3399	3400	3401	3402	3403	3404	3405	3406	3407
D50	3408	3409	3410	3411	3412	3413	3414	3415	3416	3417	3418	3419	3420	3421	3422	3423
D60	3424	3425	3426	3427	3428	3429	3430	3431	3432	3433	3434	3435	3436	3437	3438	3439
D70	3440	3441	3442	3443	3444	3445	3446	3447	3448	3449	3450	3451	3452	3453	3454	3455
D80	3456	3457	3458	3459	3460	3461	3462	3463	3464	3465	3466	3467	3468	3469	3470	3471
D90	3472	3473	3474	3475	3476	3477	3478	3479	3480	3481	3482	3483	3484	3485	3486	3487
DA0	3488	3489	3490	3491	3492	3493	3494	3495	3496	3497	3498	3499	3500	3501	3502	3503
DB0	3504	3505	3506	3507	3508	3509	3510	3511	3512	3513	3514	3515	3516	3517	3518	3519
DC0	3520	3521	3522	3523	3524	3525	3526	3527	3528	3529	3530	3531	3532	3533	3534	3535
DD0	3536	3537	3538	3539	3540	3541	3542	3543	3544	3545	3546	3547	3548	3549	3550	3551
DE0	3552	3553	3554	3555	3556	3557	3558	3559	3560	3561	3562	3563	3564	3565	3566	3567
DF0	3568	3569	3570	3571	3572	3573	3574	3575	3576	3577	3578	3579	3580	3581	3582	3583
E00	3584	3585	3586	3587	3588	3589	3590	3591	3592	3593	3594	3595	3596	3597	3598	3599
E10	3600	3601	3602	3603	3604	3605	3606	3607	3608	3609	3610	3611	3612	3613	3614	3615
E20	3616	3617	3618	3619	3620	3621	3622	3623	3624	3625	3626	3627	3628	3629	3630	3631
E30	3632	3633	3634	3635	3636	3637	3638	3639	3640	3641	3642	3643	3644	3645	3646	3647
E40	3648	3649	3650	3651	3652	3653	3654	3655	3656	3657	3658	3659	3660	3661	3662	3663
E50	3664	3665	3666	3667	3668	3669	3670	3671	3672	3673	3674	3675	3676	3677	3678	3679
E60	3680	3681	3682	3683	3684	3685	3686	3687	3688	3689	3690	3691	3692	3693	3694	3695
E70	3696	3697	3698	3699	3700	3701	3702	3703	3704	3705	3706	3707	3708	3709	3710	3711
E80	3712	3713	3714	3715	3716	3717	3718	3719	3720	3721	3722	3723	3724	3725	3726	3727
E90	3728	3729	3730	3731	3732	3733	3734	3735	3736	3737	3738	3739	3740	3741	3742	3743
EA0	3744	3745	3746	3747	3748	3749	3750	3751	3752	3753	3754	3755	3756	3757	3758	3759
EB0	3760	3761	3762	3763	3764	3765	3766	3767	3768	3769	3770	3771	3772	3773	3774	3775
EC0	3776	3777	3778	3779	3780	3781	3782	3783	3784	3785	3786	3787	3788	3789	3790	3791
ED0	3792	3793	3794	3795	3796	3797	3798	3799	3800	3801	3802	3803	3804	3805	3806	3807
EE0	3808	3809	3810	3811	3812	3813	3814	3815	3816	3817	3818	3819	3820	3821	3822	3823
EF0	3824	3825	3826	3827	3828	3829	3830	3831	3832	3833	3834	3835	3836	3837	3838	3839
F00	3840	3841	3842	3843	3844	3845	3846	3847	3848	3849	3850	3851	3852	3853	3854	3855
F10	3856	3857	3858	3859	3860	3861	3862	3863	3864	3865	3866	3867	3868	3869	3870	3871
F20	3872	3873	3874	3875	3876	3877	3878	3879	3880	3881	3882	3883	3884	3885	3886	3887
F30	3888	3889	3890	3891	3892	3893	3894	3895	3896	3897	3898	3899	3900	3901	3902	3903
F40	3904	3905	3906	3907	3908	3909	3910	3911	3912	3913	3914	3915	3916	3917	3918	3919
F50	3920	3921	3922	3923	3924	3925	3926	3927	3928	3929	3930	3931	3932	3933	3934	3935
F60	3936	3937	3938	3939	3940	3941	3942	3943	3944	3945	3946	3947	3948	3949	3950	3951
F70	3952	3953	3954	3955	3956	3957	3958	3959	3960	3961	3962	3963	3964	3965	3966	3967
F80	3968	3969	3970	3971	3972	3973	3974	3975	3976	3977	3978	3979	3980	3981	3982	3983
F90	3984	3985	3986	3987	3988	3989	3990	3991	3992	3993	3994	3995	3996	3997	3998	3999
FA0	4000	4001	4002	4003	4004	4005	4006	4007	4008	4009	4010	4011	4012	4013	4014	4015
FB0	4016	4017	4018	4019	4020	4021	4022	4023	4024	4025	4026	4027	4028	4029	4030	4031
FC0	4032	4033	4034	4035	4036	4037	4038	4039	4040	4041	4042	4043	4044	4045	4046	4047
FD0	4048	4049	4050	4051	4052	4053	4054	4055	4056	4057	4058	4059	4060	4061	4062	4063
FE0	4064	4065	4066	4067	4068	4069	4070	4071	4072	4073	4074	4075	4076	4077	4078	4079
FF0	4080	4081	4082	4083	4084	4085	4086	4087	4088	4089	4090	4091	4092	4093	4094	4095

Table B-4. Hexadecimal/Decimal Fraction Conversions

Hexadecimal	Decimal	Hexadecimal	Decimal	Hexadecimal	Decimal	Hexadecimal	Decimal
.00 00 00 00	.00000 00000	.40 00 00 00	.25000 00000	.80 00 00 00	.50000 00000	.C0 00 00 00	.75000 00000
.01 00 00 00	.00390 62500	.41 00 00 00	.25390 62500	.81 00 00 00	.50390 62500	.C1 00 00 00	.75390 62500
.02 00 00 00	.00781 25000	.42 00 00 00	.25781 25000	.82 00 00 00	.50781 25000	.C2 00 00 00	.75781 25000
.03 00 00 00	.01171 87500	.43 00 00 00	.26171 87500	.83 00 00 00	.51171 87500	.C3 00 00 00	.76171 87500
.04 00 00 00	.01562 50000	.44 00 00 00	.26562 50000	.84 00 00 00	.51562 50000	.C4 00 00 00	.76562 50000
.05 00 00 00	.01953 12500	.45 00 00 00	.26953 12500	.85 00 00 00	.51953 12500	.C5 00 00 00	.76953 12500
.06 00 00 00	.02343 75000	.46 00 00 00	.27343 75000	.86 00 00 00	.52343 75000	.C6 00 00 00	.77343 75000
.07 00 00 00	.02734 37500	.47 00 00 00	.27734 37500	.87 00 00 00	.52734 37500	.C7 00 00 00	.77734 37500
.08 00 00 00	.03125 00000	.48 00 00 00	.28125 00000	.88 00 00 00	.53125 00000	.C8 00 00 00	.78125 00000
.09 00 00 00	.03515 62500	.49 00 00 00	.28515 62500	.89 00 00 00	.53515 62500	.C9 00 00 00	.78515 62500
.0A 00 00 00	.03906 25000	.4A 00 00 00	.28906 25000	.8A 00 00 00	.53906 25000	.CA 00 00 00	.78906 25000
.0B 00 00 00	.04296 87500	.4B 00 00 00	.29296 87500	.8B 00 00 00	.54296 87500	.CB 00 00 00	.79296 87500
.0C 00 00 00	.04687 50000	.4C 00 00 00	.29687 50000	.8C 00 00 00	.54687 50000	.CC 00 00 00	.79687 50000
.0D 00 00 00	.05078 12500	.4D 00 00 00	.30078 12500	.8D 00 00 00	.55078 12500	.CD 00 00 00	.80078 12500
.0E 00 00 00	.05468 75000	.4E 00 00 00	.30468 75000	.8E 00 00 00	.55468 75000	.CE 00 00 00	.80468 75000
.0F 00 00 00	.05859 37500	.4F 00 00 00	.30859 37500	.8F 00 00 00	.55859 37500	.CF 00 00 00	.80859 37500
.10 00 00 00	.06250 00000	.50 00 00 00	.31250 00000	.90 00 00 00	.56250 00000	.D0 00 00 00	.81250 00000
.11 00 00 00	.06640 62500	.51 00 00 00	.31640 62500	.91 00 00 00	.56640 62500	.D1 00 00 00	.81640 62500
.12 00 00 00	.07031 25000	.52 00 00 00	.32031 25000	.92 00 00 00	.57031 25000	.D2 00 00 00	.82031 25000
.13 00 00 00	.07421 87500	.53 00 00 00	.32421 87500	.93 00 00 00	.57421 87500	.D3 00 00 00	.82421 87500
.14 00 00 00	.07812 50000	.54 00 00 00	.32812 50000	.94 00 00 00	.57812 50000	.D4 00 00 00	.82812 50000
.15 00 00 00	.08203 12500	.55 00 00 00	.33203 12500	.95 00 00 00	.58203 12500	.D5 00 00 00	.83203 12500
.16 00 00 00	.08593 75000	.56 00 00 00	.33593 75000	.96 00 00 00	.58593 75000	.D6 00 00 00	.83593 75000
.17 00 00 00	.08984 37500	.57 00 00 00	.33984 37500	.97 00 00 00	.58984 37500	.D7 00 00 00	.83984 37500
.18 00 00 00	.09375 00000	.58 00 00 00	.34375 00000	.98 00 00 00	.59375 00000	.D8 00 00 00	.84375 00000
.19 00 00 00	.09765 62500	.59 00 00 00	.34765 62500	.99 00 00 00	.59765 62500	.D9 00 00 00	.84765 62500
.1A 00 00 00	.10156 25000	.5A 00 00 00	.35156 25000	.9A 00 00 00	.60156 25000	.DA 00 00 00	.85156 25000
.1B 00 00 00	.10546 87500	.5B 00 00 00	.35546 87500	.9B 00 00 00	.60546 87500	.DB 00 00 00	.85546 87500
.1C 00 00 00	.10937 50000	.5C 00 00 00	.35937 50000	.9C 00 00 00	.60937 50000	.DC 00 00 00	.85937 50000
.1D 00 00 00	.11328 12500	.5D 00 00 00	.36328 12500	.9D 00 00 00	.61328 12500	.DD 00 00 00	.86328 12500
.1E 00 00 00	.11718 75000	.5E 00 00 00	.36718 75000	.9E 00 00 00	.61718 75000	.DE 00 00 00	.86718 75000
.1F 00 00 00	.12109 37500	.5F 00 00 00	.37109 37500	.9F 00 00 00	.62109 37500	.DF 00 00 00	.87109 37500
.20 00 00 00	.12500 00000	.60 00 00 00	.37500 00000	.A0 00 00 00	.62500 00000	.E0 00 00 00	.87500 00000
.21 00 00 00	.12890 62500	.61 00 00 00	.37890 62500	.A1 00 00 00	.62890 62500	.E1 00 00 00	.87890 62500
.22 00 00 00	.13281 25000	.62 00 00 00	.38281 25000	.A2 00 00 00	.63281 25000	.E2 00 00 00	.88281 25000
.23 00 00 00	.13671 87500	.63 00 00 00	.38671 87500	.A3 00 00 00	.63671 87500	.E3 00 00 00	.88671 87500
.24 00 00 00	.14062 50000	.64 00 00 00	.39062 50000	.A4 00 00 00	.64062 50000	.E4 00 00 00	.89062 50000
.25 00 00 00	.14453 12500	.65 00 00 00	.39453 12500	.A5 00 00 00	.64453 12500	.E5 00 00 00	.89453 12500
.26 00 00 00	.14843 75000	.66 00 00 00	.39843 75000	.A6 00 00 00	.64843 75000	.E6 00 00 00	.89843 75000
.27 00 00 00	.15234 37500	.67 00 00 00	.40234 37500	.A7 00 00 00	.65234 37500	.E7 00 00 00	.90234 37500
.28 00 00 00	.15625 00000	.68 00 00 00	.40625 00000	.A8 00 00 00	.65625 00000	.E8 00 00 00	.90625 00000
.29 00 00 00	.16015 62500	.69 00 00 00	.41015 62500	.A9 00 00 00	.66015 62500	.E9 00 00 00	.91015 62500
.2A 00 00 00	.16406 25000	.6A 00 00 00	.41406 25000	.AA 00 00 00	.66406 25000	.EA 00 00 00	.91406 25000
.2B 00 00 00	.16796 87500	.6B 00 00 00	.41796 87500	.AB 00 00 00	.66796 87500	.EB 00 00 00	.91796 87500
.2C 00 00 00	.17187 50000	.6C 00 00 00	.42187 50000	.AC 00 00 00	.67187 50000	.EC 00 00 00	.92187 50000
.2D 00 00 00	.17578 12500	.6D 00 00 00	.42578 12500	.AD 00 00 00	.67578 12500	.ED 00 00 00	.92578 12500
.2E 00 00 00	.17968 75000	.6E 00 00 00	.42968 75000	.AE 00 00 00	.67968 75000	.EE 00 00 00	.92968 75000
.2F 00 00 00	.18359 37500	.6F 00 00 00	.43359 37500	.AF 00 00 00	.68359 37500	.EF 00 00 00	.93359 37500
.30 00 00 00	.18750 00000	.70 00 00 00	.43750 00000	.B0 00 00 00	.68750 00000	.F0 00 00 00	.93750 00000
.31 00 00 00	.19140 62500	.71 00 00 00	.44140 62500	.B1 00 00 00	.69140 62500	.F1 00 00 00	.94140 62500
.32 00 00 00	.19531 25000	.72 00 00 00	.44531 25000	.B2 00 00 00	.69531 25000	.F2 00 00 00	.94531 25000
.33 00 00 00	.19921 87500	.73 00 00 00	.44921 87500	.B3 00 00 00	.69921 87500	.F3 00 00 00	.94921 87500
.34 00 00 00	.20312 50000	.74 00 00 00	.45312 50000	.B4 00 00 00	.70312 50000	.F4 00 00 00	.95312 50000
.35 00 00 00	.20703 12500	.75 00 00 00	.45703 12500	.B5 00 00 00	.70703 12500	.F5 00 00 00	.95703 12500
.36 00 00 00	.21093 75000	.76 00 00 00	.46093 75000	.B6 00 00 00	.71093 75000	.F6 00 00 00	.96093 75000
.37 00 00 00	.21484 37500	.77 00 00 00	.46484 37500	.B7 00 00 00	.71484 37500	.F7 00 00 00	.96484 37500
.38 00 00 00	.21875 00000	.78 00 00 00	.46875 00000	.B8 00 00 00	.71875 00000	.F8 00 00 00	.96875 00000
.39 00 00 00	.22265 62500	.79 00 00 00	.47265 62500	.B9 00 00 00	.72265 62500	.F9 00 00 00	.97265 62500
.3A 00 00 00	.22656 25000	.7A 00 00 00	.47656 25000	.BA 00 00 00	.72656 25000	.FA 00 00 00	.97656 25000
.3B 00 00 00	.23046 87500	.7B 00 00 00	.48046 87500	.BB 00 00 00	.73046 87500	.FB 00 00 00	.98046 87500
.3C 00 00 00	.23437 50000	.7C 00 00 00	.48437 50000	.BC 00 00 00	.73437 50000	.FC 00 00 00	.98437 50000
.3D 00 00 00	.23828 12500	.7D 00 00 00	.48828 12500	.BD 00 00 00	.73828 12500	.FD 00 00 00	.98828 12500
.3E 00 00 00	.24218 75000	.7E 00 00 00	.49218 75000	.BE 00 00 00	.74218 75000	.FE 00 00 00	.99218 75000
.3F 00 00 00	.24609 37500	.7F 00 00 00	.49609 37500	.BF 00 00 00	.74609 37500	.FF 00 00 00	.99609 37500

Hexadecimal	Decimal	Hexadecimal	Decimal	Hexadecimal	Decimal	Hexadecimal	Decimal
.00 00 00 00	.00000 00000	.00 40 00 00	.00097 65625	.00 80 00 00	.00195 31250	.00 C0 00 00	.00292 96875
.00 01 00 00	.00001 52587	.00 41 00 00	.00099 18212	.00 81 00 00	.00196 83837	.00 C1 00 00	.00294 49462
.00 02 00 00	.00003 05175	.00 42 00 00	.00100 70800	.00 82 00 00	.00198 36425	.00 C2 00 00	.00296 02050
.00 03 00 00	.00004 57763	.00 43 00 00	.00102 23388	.00 83 00 00	.00199 89013	.00 C3 00 00	.00297 54638
.00 04 00 00	.00006 10351	.00 44 00 00	.00103 75976	.00 84 00 00	.00201 41601	.00 C4 00 00	.00299 07226
.00 05 00 00	.00007 62939	.00 45 00 00	.00105 28564	.00 85 00 00	.00202 94189	.00 C5 00 00	.00300 59814
.00 06 00 00	.00009 15527	.00 46 00 00	.00106 81152	.00 86 00 00	.00204 46777	.00 C6 00 00	.00302 12402
.00 07 00 00	.00010 68115	.00 47 00 00	.00108 33740	.00 87 00 00	.00205 99365	.00 C7 00 00	.00303 64990
.00 08 00 00	.00012 20703	.00 48 00 00	.00109 86328	.00 88 00 00	.00207 51953	.00 C8 00 00	.00305 17578
.00 09 00 00	.00013 73291	.00 49 00 00	.00111 38916	.00 89 00 00	.00209 04541	.00 C9 00 00	.00306 70166
.00 0A 00 00	.00015 25878	.00 4A 00 00	.00112 91503	.00 8A 00 00	.00210 57128	.00 CA 00 00	.00308 22753
.00 0B 00 00	.00016 78466	.00 4B 00 00	.00114 44091	.00 8B 00 00	.00212 09716	.00 CB 00 00	.00309 75341
.00 0C 00 00	.00018 31054	.00 4C 00 00	.00115 96679	.00 8C 00 00	.00213 62304	.00 CC 00 00	.00311 27929
.00 0D 00 00	.00019 83642	.00 4D 00 00	.00117 49267	.00 8D 00 00	.00215 14892	.00 CD 00 00	.00312 80517
.00 0E 00 00	.00021 36230	.00 4E 00 00	.00119 01855	.00 8E 00 00	.00216 67480	.00 CE 00 00	.00314 33105
.00 0F 00 00	.00022 88818	.00 4F 00 00	.00120 54443	.00 8F 00 00	.00218 20068	.00 CF 00 00	.00315 85693
.00 10 00 00	.00024 41406	.00 50 00 00	.00122 07031	.00 90 00 00	.00219 72656	.00 D0 00 00	.00317 38281
.00 11 00 00	.00025 93994	.00 51 00 00	.00123 59619	.00 91 00 00	.00221 25244	.00 D1 00 00	.00318 90869
.00 12 00 00	.00027 46582	.00 52 00 00	.00125 12207	.00 92 00 00	.00222 77832	.00 D2 00 00	.00320 43457
.00 13 00 00	.00028 99169	.00 53 00 00	.00126 64794	.00 93 00 00	.00224 30419	.00 D3 00 00	.00321 96044
.00 14 00 00	.00030 51757	.00 54 00 00	.00128 17382	.00 94 00 00	.00225 83007	.00 D4 00 00	.00323 48632
.00 15 00 00	.00032 04345	.00 55 00 00	.00129 69970	.00 95 00 00	.00227 35595	.00 D5 00 00	.00325 01220
.00 16 00 00	.00033 56933	.00 56 00 00	.00131 22558	.00 96 00 00	.00228 88183	.00 D6 00 00	.00326 53808
.00 17 00 00	.00035 09521	.00 57 00 00	.00132 75146	.00 97 00 00	.00230 40771	.00 D7 00 00	.00328 06396
.00 18 00 00	.00036 62109	.00 58 00 00	.00134 27734	.00 98 00 00	.00231 93359	.00 D8 00 00	.00329 58984
.00 19 00 00	.00038 14697	.00 59 00 00	.00135 80322	.00 99 00 00	.00233 45947	.00 D9 00 00	.00331 11572
.00 1A 00 00	.00039 67285	.00 5A 00 00	.00137 32910	.00 9A 00 00	.00234 98535	.00 DA 00 00	.00332 64160
.00 1B 00 00	.00041 19873	.00 5B 00 00	.00138 85498	.00 9B 00 00	.00236 51123	.00 DB 00 00	.00334 16748
.00 1C 00 00	.00042 72460	.00 5C 00 00	.00140 38085	.00 9C 00 00	.00238 03710	.00 DC 00 00	.00335 69335
.00 1D 00 00	.00044 25048	.00 5D 00 00	.00141 90673	.00 9D 00 00	.00239 56298	.00 DD 00 00	.00337 21923
.00 1E 00 00	.00045 77636	.00 5E 00 00	.00143 43261	.00 9E 00 00	.00241 08886	.00 DE 00 00	.00338 74511
00 1F 00 00	.00047 30224	.00 5F 00 00	.00144 95849	.00 9F 00 00	.00242 61474	.00 DF 00 00	.00340 27099
.00 20 00 00	.00048 82812	.00 60 00 00	.00146 48437	.00 A0 00 00	.00244 14062	.00 E0 00 00	.00341 79687
.00 21 00 00	.00050 35400	.00 61 00 00	.00148 01025	.00 A1 00 00	.00245 66650	.00 E1 00 00	.00343 32275
.00 22 00 00	.00051 87988	.00 62 00 00	.00149 53613	.00 A2 00 00	.00247 19238	.00 E2 00 00	.00344 84863
.00 23 00 00	.00053 40576	.00 63 00 00	.00151 06201	.00 A3 00 00	.00248 71826	.00 E3 00 00	.00346 37451
.00 24 00 00	.00054 93164	.00 64 00 00	.00152 58789	.00 A4 00 00	.00250 24414	.00 E4 00 00	.00347 90039
.00 25 00 00	.00056 45751	.00 65 00 00	.00154 11376	.00 A5 00 00	.00251 77001	.00 E5 00 00	.00349 42626
.00 26 00 00	.00057 98339	.00 66 00 00	.00155 63964	.00 A6 00 00	.00253 29589	.00 E6 00 00	.00350 95214
.00 27 00 00	.00059 50927	.00 67 00 00	.00157 16552	.00 A7 00 00	.00254 82177	.00 E7 00 00	.00352 47802
.00 28 00 00	.00061 03515	.00 68 00 00	.00158 69140	.00 A8 00 00	.00256 34765	.00 E8 00 00	.00354 00390
.00 29 00 00	.00062 56103	.00 69 00 00	.00160 21728	.00 A9 00 00	.00257 87353	.00 E9 00 00	.00355 52978
.00 2A 00 00	.00064 08691	.00 6A 00 00	.00161 74316	.00 AA 00 00	.00259 39941	.00 EA 00 00	.00357 05566
.00 2B 00 00	.00065 61279	.00 6B 00 00	.00163 26904	.00 AB 00 00	.00260 92529	.00 EB 00 00	.00358 58154
.00 2C 00 00	.00067 13867	.00 6C 00 00	.00164 79492	.00 AC 00 00	.00262 45117	.00 EC 00 00	.00360 10742
.00 2D 00 00	.00068 66455	.00 6D 00 00	.00166 32080	.00 AD 00 00	.00263 97705	.00 ED 00 00	.00361 63330
.00 2E 00 00	.00070 19042	.00 6E 00 00	.00167 84667	.00 AE 00 00	.00265 50292	.00 EE 00 00	.00363 15917
.00 2F 00 00	.00071 71630	.00 6F 00 00	.00169 37255	.00 AF 00 00	.00267 02880	.00 EF 00 00	.00364 68505
.00 30 00 00	.00073 24218	.00 70 00 00	.00170 89843	.00 B0 00 00	.00268 55468	.00 F0 00 00	.00366 21093
.00 31 00 00	.00074 76806	.00 71 00 00	.00172 42431	.00 B1 00 00	.00270 08056	.00 F1 00 00	.00367 73681
.00 32 00 00	.00076 29394	.00 72 00 00	.00173 95019	.00 B2 00 00	.00271 60644	.00 F2 00 00	.00369 26269
.00 33 00 00	.00077 81982	.00 73 00 00	.00175 47607	.00 B3 00 00	.00273 13232	.00 F3 00 00	.00370 78857
.00 34 00 00	.00079 34570	.00 74 00 00	.00177 00195	.00 B4 00 00	.00274 65820	.00 F4 00 00	.00372 31445
.00 35 00 00	.00080 87158	.00 75 00 00	.00178 52783	.00 B5 00 00	.00276 18408	.00 F5 00 00	.00373 84033
.00 36 00 00	.00082 39746	.00 76 00 00	.00180 05371	.00 B6 00 00	.00277 70996	.00 F6 00 00	.00375 36621
.00 37 00 00	.00083 92333	.00 77 00 00	.00181 57958	.00 B7 00 00	.00279 23583	.00 F7 00 00	.00376 89208
.00 38 00 00	.00085 44921	.00 78 00 00	.00183 10546	.00 B8 00 00	.00280 76171	.00 F8 00 00	.00378 41796
.00 39 00 00	.00086 97509	.00 79 00 00	.00184 63134	.00 B9 00 00	.00282 28759	.00 F9 00 00	.00379 94384
.00 3A 00 00	.00088 50097	.00 7A 00 00	.00186 15722	.00 BA 00 00	.00283 81347	.00 FA 00 00	.00381 46972
.00 3B 00 00	.00090 02685	.00 7B 00 00	.00187 68310	.00 BB 00 00	.00285 33935	.00 FB 00 00	.00382 99560
.00 3C 00 00	.00091 55273	.00 7C 00 00	.00189 20898	.00 BC 00 00	.00286 86523	.00 FC 00 00	.00384 52148
.00 3D 00 00	.00093 07861	.00 7D 00 00	.00190 73486	.00 BD 00 00	.00288 39111	.00 FD 00 00	.00386 04736
.00 3E 00 00	.00094 60449	.00 7E 00 00	.00192 26074	.00 BE 00 00	.00289 91699	.00 FE 00 00	.00387 57324
.00 3F 00 00	.00096 13037	.00 7F 00 00	.00193 78662	.00 BF 00 00	.00291 44287	.00 FF 00 00	.00389 09912

Hexadecimal	Decimal	Hexadecimal	Decimal	Hexadecimal	Decimal	Hexadecimal	Decimal
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.00 00 01 00	.00000 00596	.00 00 41 00	.00000 38743	.00 00 81 00	.00000 76889	.00 00 C1 00	.00001 15036
.00 00 02 00	.00000 01192	.00 00 42 00	.00000 39339	.00 00 82 00	.00000 77486	.00 00 C2 00	.00001 15633
.00 00 03 00	.00000 01788	.00 00 43 00	.00000 39935	.00 00 83 00	.00000 78082	.00 00 C3 00	.00001 16229
.00 00 04 00	.00000 02384	.00 00 44 00	.00000 40531	.00 00 84 00	.00000 78678	.00 00 C4 00	.00001 16825
.00 00 05 00	.00000 02980	.00 00 45 00	.00000 41127	.00 00 85 00	.00000 79274	.00 00 C5 00	.00001 17421
.00 00 06 00	.00000 03576	.00 00 46 00	.00000 41723	.00 00 86 00	.00000 79870	.00 00 C6 00	.00001 18017
.00 00 07 00	.00000 04172	.00 00 47 00	.00000 42319	.00 00 87 00	.00000 80466	.00 00 C7 00	.00001 18613
.00 00 08 00	.00000 04768	.00 00 48 00	.00000 42915	.00 00 88 00	.00000 81062	.00 00 C8 00	.00001 19209
.00 00 09 00	.00000 05364	.00 00 49 00	.00000 43511	.00 00 89 00	.00000 81658	.00 00 C9 00	.00001 19805
.00 00 0A 00	.00000 05960	.00 00 4A 00	.00000 44107	.00 00 8A 00	.00000 82254	.00 00 CA 00	.00001 20401
.00 00 0B 00	.00000 06556	.00 00 4B 00	.00000 44703	.00 00 8B 00	.00000 82850	.00 00 CB 00	.00001 20997
.00 00 0C 00	.00000 07152	.00 00 4C 00	.00000 45299	.00 00 8C 00	.00000 83446	.00 00 CC 00	.00001 21593
.00 00 0D 00	.00000 07748	.00 00 4D 00	.00000 45895	.00 00 8D 00	.00000 84042	.00 00 CD 00	.00001 22189
.00 00 0E 00	.00000 08344	.00 00 4E 00	.00000 46491	.00 00 8E 00	.00000 84638	.00 00 CE 00	.00001 22785
.00 00 0F 00	.00000 08940	.00 00 4F 00	.00000 47087	.00 00 8F 00	.00000 85234	.00 00 CF 00	.00001 23381
.00 00 10 00	.00000 09536	.00 00 50 00	.00000 47683	.00 00 90 00	.00000 85830	.00 00 D0 00	.00001 23977
.00 00 11 00	.00000 10132	.00 00 51 00	.00000 48279	.00 00 91 00	.00000 86426	.00 00 D1 00	.00001 24573
.00 00 12 00	.00000 10728	.00 00 52 00	.00000 48875	.00 00 92 00	.00000 87022	.00 00 D2 00	.00001 25169
.00 00 13 00	.00000 11324	.00 00 53 00	.00000 49471	.00 00 93 00	.00000 87618	.00 00 D3 00	.00001 25765
.00 00 14 00	.00000 11920	.00 00 54 00	.00000 50067	.00 00 94 00	.00000 88214	.00 00 D4 00	.00001 26361
.00 00 15 00	.00000 12516	.00 00 55 00	.00000 50663	.00 00 95 00	.00000 88810	.00 00 D5 00	.00001 26957
.00 00 16 00	.00000 13113	.00 00 56 00	.00000 51259	.00 00 96 00	.00000 89406	.00 00 D6 00	.00001 27553
.00 00 17 00	.00000 13709	.00 00 57 00	.00000 51856	.00 00 97 00	.00000 90003	.00 00 D7 00	.00001 28149
.00 00 18 00	.00000 14305	.00 00 58 00	.00000 52452	.00 00 98 00	.00000 90599	.00 00 D8 00	.00001 28746
.00 00 19 00	.00000 14901	.00 00 59 00	.00000 53048	.00 00 99 00	.00000 91195	.00 00 D9 00	.00001 29342
.00 00 1A 00	.00000 15497	.00 00 5A 00	.00000 53644	.00 00 9A 00	.00000 91791	.00 00 DA 00	.00001 29938
.00 00 1B 00	.00000 16093	.00 00 5B 00	.00000 54240	.00 00 9B 00	.00000 92387	.00 00 DB 00	.00001 30534
.00 00 1C 00	.00000 16689	.00 00 5C 00	.00000 54836	.00 00 9C 00	.00000 92983	.00 00 DC 00	.00001 31130
.00 00 1D 00	.00000 17285	.00 00 5D 00	.00000 55432	.00 00 9D 00	.00000 93579	.00 00 DD 00	.00001 31726
.00 00 1E 00	.00000 17881	.00 00 5E 00	.00000 56028	.00 00 9E 00	.00000 94175	.00 00 DE 00	.00001 32322
.00 00 1F 00	.00000 18477	.00 00 5F 00	.00000 56624	.00 00 9F 00	.00000 94771	.00 00 DF 00	.00001 32918
.00 00 20 00	.00000 19073	.00 00 60 00	.00000 57220	.00 00 A0 00	.00000 95367	.00 00 E0 00	.00001 33514
.00 00 21 00	.00000 19669	.00 00 61 00	.00000 57816	.00 00 A1 00	.00000 95963	.00 00 E1 00	.00001 34110
.00 00 22 00	.00000 20265	.00 00 62 00	.00000 58412	.00 00 A2 00	.00000 96559	.00 00 E2 00	.00001 34706
.00 00 23 00	.00000 20861	.00 00 63 00	.00000 59008	.00 00 A3 00	.00000 97155	.00 00 E3 00	.00001 35302
.00 00 24 00	.00000 21457	.00 00 64 00	.00000 59604	.00 00 A4 00	.00000 97751	.00 00 E4 00	.00001 35898
.00 00 25 00	.00000 22053	.00 00 65 00	.00000 60200	.00 00 A5 00	.00000 98347	.00 00 E5 00	.00001 36494
.00 00 26 00	.00000 22649	.00 00 66 00	.00000 60796	.00 00 A6 00	.00000 98943	.00 00 E6 00	.00001 37090
.00 00 27 00	.00000 23245	.00 00 67 00	.00000 61392	.00 00 A7 00	.00000 99539	.00 00 E7 00	.00001 37686
.00 00 28 00	.00000 23841	.00 00 68 00	.00000 61988	.00 00 A8 00	.00001 00135	.00 00 E8 00	.00001 38282
.00 00 29 00	.00000 24437	.00 00 69 00	.00000 62584	.00 00 A9 00	.00001 00731	.00 00 E9 00	.00001 38878
.00 00 2A 00	.00000 25033	.00 00 6A 00	.00000 63180	.00 00 AA 00	.00001 01327	.00 00 EA 00	.00001 39474
.00 00 2B 00	.00000 25629	.00 00 6B 00	.00000 63776	.00 00 AB 00	.00001 01923	.00 00 EB 00	.00001 40070
.00 00 2C 00	.00000 26226	.00 00 6C 00	.00000 64373	.00 00 AC 00	.00001 02519	.00 00 EC 00	.00001 40666
.00 00 2D 00	.00000 26822	.00 00 6D 00	.00000 64969	.00 00 AD 00	.00001 03116	.00 00 ED 00	.00001 41263
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.00 00 35 00	.00000 31590	.00 00 75 00	.00000 69737	.00 00 B5 00	.00001 07884	.00 00 F5 00	.00001 46031
.00 00 36 00	.00000 32186	.00 00 76 00	.00000 70333	.00 00 B6 00	.00001 08480	.00 00 F6 00	.00001 46627
.00 00 37 00	.00000 32782	.00 00 77 00	.00000 70929	.00 00 B7 00	.00001 09076	.00 00 F7 00	.00001 47223
.00 00 38 00	.00000 33378	.00 00 78 00	.00000 71525	.00 00 B8 00	.00001 09672	.00 00 F8 00	.00001 47819
.00 00 39 00	.00000 33974	.00 00 79 00	.00000 72121	.00 00 B9 00	.00001 10268	.00 00 F9 00	.00001 48415
.00 00 3A 00	.00000 34570	.00 00 7A 00	.00000 72717	.00 00 BA 00	.00001 10864	.00 00 FA 00	.00001 49011
.00 00 3B 00	.00000 35166	.00 00 7B 00	.00000 73313	.00 00 BB 00	.00001 11460	.00 00 FB 00	.00001 49607
.00 00 3C 00	.00000 35762	.00 00 7C 00	.00000 73909	.00 00 BC 00	.00001 12056	.00 00 FC 00	.00001 50203
.00 00 3D 00	.00000 36358	.00 00 7D 00	.00000 74505	.00 00 BD 00	.00001 12652	.00 00 FD 00	.00001 50799
.00 00 3E 00	.00000 36954	.00 00 7E 00	.00000 75101	.00 00 BE 00	.00001 13248	.00 00 FE 00	.00001 51395
.00 00 3F 00	.00000 37550	.00 00 7F 00	.00000 75697	.00 00 BF 00	.00001 13844	.00 00 FF 00	.00001 51991

Hexadecimal	Decimal	Hexadecimal	Decimal	Hexadecimal	Decimal	Hexadecimal	Decimal
.00 00 00 00	.00000 00000	.00 00 00 40	.00000 00149	.00 00 00 80	.00000 00298	.00 00 00 C0	.00000 00447
.00 00 00 01	.00000 00002	.00 00 00 41	.00000 00151	.00 00 00 81	.00000 00300	.00 00 00 C1	.00000 00449
.00 00 00 02	.00000 00004	.00 00 00 42	.00000 00153	.00 00 00 82	.00000 00302	.00 00 00 C2	.00000 00451
.00 00 00 03	.00000 00006	.00 00 00 43	.00000 00155	.00 00 00 83	.00000 00305	.00 00 00 C3	.00000 00454
.00 00 00 04	.00000 00009	.00 00 00 44	.00000 00158	.00 00 00 84	.00000 00307	.00 00 00 C4	.00000 00456
.00 00 00 05	.00000 00011	.00 00 00 45	.00000 00160	.00 00 00 85	.00000 00309	.00 00 00 C5	.00000 00458
.00 00 00 06	.00000 00013	.00 00 00 46	.00000 00162	.00 00 00 86	.00000 00311	.00 00 00 C6	.00000 00461
.00 00 00 07	.00000 00016	.00 00 00 47	.00000 00165	.00 00 00 87	.00000 00314	.00 00 00 C7	.00000 00463
.00 00 00 08	.00000 00018	.00 00 00 48	.00000 00167	.00 00 00 88	.00000 00316	.00 00 00 C8	.00000 00465
.00 00 00 09	.00000 00020	.00 00 00 49	.00000 00169	.00 00 00 89	.00000 00318	.00 00 00 C9	.00000 00467
.00 00 00 0A	.00000 00023	.00 00 00 4A	.00000 00172	.00 00 00 8A	.00000 00321	.00 00 00 CA	.00000 00470
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.00 00 00 0C	.00000 00027	.00 00 00 4C	.00000 00176	.00 00 00 8C	.00000 00325	.00 00 00 CC	.00000 00474
.00 00 00 0D	.00000 00030	.00 00 00 4D	.00000 00179	.00 00 00 8D	.00000 00328	.00 00 00 CD	.00000 00477
.00 00 00 0E	.00000 00032	.00 00 00 4E	.00000 00181	.00 00 00 8E	.00000 00330	.00 00 00 CE	.00000 00479
.00 00 00 0F	.00000 00034	.00 00 00 4F	.00000 00183	.00 00 00 8F	.00000 00332	.00 00 00 CF	.00000 00481
.00 00 00 10	.00000 00037	.00 00 00 50	.00000 00186	.00 00 00 90	.00000 00335	.00 00 00 D0	.00000 00484
.00 00 00 11	.00000 00039	.00 00 00 51	.00000 00188	.00 00 00 91	.00000 00337	.00 00 00 D1	.00000 00486
.00 00 00 12	.00000 00041	.00 00 00 52	.00000 00190	.00 00 00 92	.00000 00339	.00 00 00 D2	.00000 00488
.00 00 00 13	.00000 00044	.00 00 00 53	.00000 00193	.00 00 00 93	.00000 00342	.00 00 00 D3	.00000 00491
.00 00 00 14	.00000 00046	.00 00 00 54	.00000 00195	.00 00 00 94	.00000 00344	.00 00 00 D4	.00000 00493
.00 00 00 15	.00000 00048	.00 00 00 55	.00000 00197	.00 00 00 95	.00000 00346	.00 00 00 D5	.00000 00495
.00 00 00 16	.00000 00051	.00 00 00 56	.00000 00200	.00 00 00 96	.00000 00349	.00 00 00 D6	.00000 00498
.00 00 00 17	.00000 00053	.00 00 00 57	.00000 00202	.00 00 00 97	.00000 00351	.00 00 00 D7	.00000 00500
.00 00 00 18	.00000 00055	.00 00 00 58	.00000 00204	.00 00 00 98	.00000 00353	.00 00 00 D8	.00000 00502
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.00 00 00 1C	.00000 00065	.00 00 00 5C	.00000 00214	.00 00 00 9C	.00000 00363	.00 00 00 DC	.00000 00512
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.00 00 00 1F	.00000 00072	.00 00 00 5F	.00000 00221	.00 00 00 9F	.00000 00370	.00 00 00 DF	.00000 00519
.00 00 00 20	.00000 00074	.00 00 00 60	.00000 00223	.00 00 00 A0	.00000 00372	.00 00 00 E0	.00000 00521
.00 00 00 21	.00000 00076	.00 00 00 61	.00000 00225	.00 00 00 A1	.00000 00374	.00 00 00 E1	.00000 00523
.00 00 00 22	.00000 00079	.00 00 00 62	.00000 00228	.00 00 00 A2	.00000 00377	.00 00 00 E2	.00000 00526
.00 00 00 23	.00000 00081	.00 00 00 63	.00000 00230	.00 00 00 A3	.00000 00379	.00 00 00 E3	.00000 00528
.00 00 00 24	.00000 00083	.00 00 00 64	.00000 00232	.00 00 00 A4	.00000 00381	.00 00 00 E4	.00000 00530
.00 00 00 25	.00000 00086	.00 00 00 65	.00000 00235	.00 00 00 A5	.00000 00384	.00 00 00 E5	.00000 00533
.00 00 00 26	.00000 00088	.00 00 00 66	.00000 00237	.00 00 00 A6	.00000 00386	.00 00 00 E6	.00000 00535
.00 00 00 27	.00000 00090	.00 00 00 67	.00000 00239	.00 00 00 A7	.00000 00388	.00 00 00 E7	.00000 00537
.00 00 00 28	.00000 00093	.00 00 00 68	.00000 00242	.00 00 00 A8	.00000 00391	.00 00 00 E8	.00000 00540
.00 00 00 29	.00000 00095	.00 00 00 69	.00000 00244	.00 00 00 A9	.00000 00393	.00 00 00 E9	.00000 00542
.00 00 00 2A	.00000 00097	.00 00 00 6A	.00000 00246	.00 00 00 AA	.00000 00395	.00 00 00 EA	.00000 00544
.00 00 00 2B	.00000 00100	.00 00 00 6B	.00000 00249	.00 00 00 AB	.00000 00398	.00 00 00 EB	.00000 00547
.00 00 00 2C	.00000 00102	.00 00 00 6C	.00000 00251	.00 00 00 AC	.00000 00400	.00 00 00 EC	.00000 00549
.00 00 00 2D	.00000 00104	.00 00 00 6D	.00000 00253	.00 00 00 AD	.00000 00402	.00 00 00 ED	.00000 00551
.00 00 00 2E	.00000 00107	.00 00 00 6E	.00000 00256	.00 00 00 AE	.00000 00405	.00 00 00 EE	.00000 00554
.00 00 00 2F	.00000 00109	.00 00 00 6F	.00000 00258	.00 00 00 AF	.00000 00407	.00 00 00 EF	.00000 00556
.00 00 00 30	.00000 00111	.00 00 00 70	.00000 00260	.00 00 00 B0	.00000 00409	.00 00 00 F0	.00000 00558
.00 00 00 31	.00000 00114	.00 00 00 71	.00000 00263	.00 00 00 B1	.00000 00412	.00 00 00 F1	.00000 00561
.00 00 00 32	.00000 00116	.00 00 00 72	.00000 00265	.00 00 00 B2	.00000 00414	.00 00 00 F2	.00000 00563
.00 00 00 33	.00000 00118	.00 00 00 73	.00000 00267	.00 00 00 B3	.00000 00416	.00 00 00 F3	.00000 00565
.00 00 00 34	.00000 00121	.00 00 00 74	.00000 00270	.00 00 00 B4	.00000 00419	.00 00 00 F4	.00000 00568
.00 00 00 35	.00000 00123	.00 00 00 75	.00000 00272	.00 00 00 B5	.00000 00421	.00 00 00 F5	.00000 00570
.00 00 00 36	.00000 00125	.00 00 00 76	.00000 00274	.00 00 00 B6	.00000 00423	.00 00 00 F6	.00000 00572
.00 00 00 37	.00000 00128	.00 00 00 77	.00000 00277	.00 00 00 B7	.00000 00426	.00 00 00 F7	.00000 00575
.00 00 00 38	.00000 00130	.00 00 00 78	.00000 00279	.00 00 00 B8	.00000 00428	.00 00 00 F8	.00000 00577
.00 00 00 39	.00000 00132	.00 00 00 79	.00000 00281	.00 00 00 B9	.00000 00430	.00 00 00 F9	.00000 00579
.00 00 00 3A	.00000 00135	.00 00 00 7A	.00000 00284	.00 00 00 BA	.00000 00433	.00 00 00 FA	.00000 00582
.00 00 00 3B	.00000 00137	.00 00 00 7B	.00000 00286	.00 00 00 BB	.00000 00435	.00 00 00 FB	.00000 00584
.00 00 00 3C	.00000 00139	.00 00 00 7C	.00000 00288	.00 00 00 BC	.00000 00437	.00 00 00 FC	.00000 00586
.00 00 00 3D	.00000 00142	.00 00 00 7D	.00000 00291	.00 00 00 BD	.00000 00440	.00 00 00 FD	.00000 00589
.00 00 00 3E	.00000 00144	.00 00 00 7E	.00000 00293	.00 00 00 BE	.00000 00442	.00 00 00 FE	.00000 00591
.00 00 00 3F	.00000 00146	.00 00 00 7F	.00000 00295	.00 00 00 BF	.00000 00444	.00 00 00 FF	.00000 00593

Table B-5. Hexadecimal Arithmetic

Addition

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
2	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11
3	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12
4	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
5	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14
6	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15
7	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16
8	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17
9	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18
A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19
B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A
C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B
D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C
E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D
F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E

Multiplication

1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
2	04	06	08	0A	0C	0E	10	12	14	16	18	1A	1C	1E
3	06	09	0C	0F	12	15	18	1B	1E	21	24	27	2A	2D
4	08	0C	10	14	18	1C	20	24	28	2C	30	34	38	3C
5	0A	0F	14	19	1E	23	28	2D	32	37	3C	41	46	4B
6	0C	12	18	1E	24	2A	30	36	3C	42	48	4E	54	5A
7	0E	15	1C	23	2A	31	38	3F	46	4D	54	5B	62	69
8	10	18	20	28	30	38	40	48	50	58	60	68	70	78
9	12	1B	24	2D	36	3F	48	51	5A	63	6C	75	7E	87
A	14	1E	28	32	3C	46	50	5A	64	6E	78	82	8C	96
B	16	21	2C	37	42	4D	58	63	6E	79	84	8F	9A	A5
C	18	24	30	3C	48	54	60	6C	78	84	90	9C	A8	B4
D	1A	27	34	41	4E	5B	68	75	82	8F	9C	A9	B6	C3
E	1C	2A	38	46	54	62	70	7E	8C	9A	A8	B6	C4	D2
F	1E	2D	3C	4B	5A	69	78	87	96	A5	B4	C3	D2	E1

Table B-6. Mathematical Constants

Constant	Decimal Value	Hexadecimal Value
π	3.14159 26535 89793	3.243F 6A89
π^{-1}	0.31830 98861 83790	0.517C C1B7
$\sqrt{\pi}$	1.77245 38509 05516	1.C5BF 891C
$\ln \pi$	1.14472 98858 49400	1.250D 048F
e	2.71828 18284 59045	2.B7E1 5163
e^{-1}	0.36787 94411 71442	0.5E2D 58D9
$\sqrt{e}$	1.64872 12707 00128	1.A612 98E2
$\log_{10} e$	0.43429 44819 03252	0.6F2D EC55
$\log_2 e$	1.44269 50408 88963	1.7154 7653
γ	0.57721 56649 01533	0.93C4 67E4
$\ln \gamma$	-0.54953 93129 81645	-0.8CAE 9BC1
$\sqrt{2}$	1.41421 35623 73095	1.6A09 E668
$\ln 2$	0.69314 71805 59945	0.B172 17F8
$\log_{10} 2$	0.30102 99956 63981	0.4D10 4D42
$\sqrt{10}$	3.16227 76601 68379	3.298B 075C
$\ln 10$	2.30258 50929 94046	2.4D76 3777

Table B-7. Powers of Two, Base 10

2^n	n	2^{-n}
1	0	1.0
2	1	0.5
4	2	0.25
8	3	0.125
16	4	0.062 5
32	5	0.031 25
64	6	0.015 625
128	7	0.007 812 5
256	8	0.003 906 25
512	9	0.001 953 125
1 024	10	0.000 976 562 5
2 048	11	0.000 488 281 25
4 096	12	0.000 244 140 625
8 192	13	0.000 122 070 312 5
16 384	14	0.000 061 035 156 25
32 768	15	0.000 030 517 578 125
65 536	16	0.000 015 258 789 062 5
131 072	17	0.000 007 629 394 531 25
262 144	18	0.000 003 814 697 265 625
524 288	19	0.000 001 907 348 632 812 5
1 048 576	20	0.000 000 953 674 316 406 25
2 097 152	21	0.000 000 476 837 158 203 125
4 194 304	22	0.000 000 238 418 579 101 562 5
8 388 608	23	0.000 000 119 209 289 550 781 25
16 777 216	24	0.000 000 059 604 644 775 390 625
33 554 432	25	0.000 000 029 802 322 387 695 312 5
67 108 864	26	0.000 000 014 901 161 193 847 656 25
134 217 728	27	0.000 000 007 450 580 596 923 828 125
268 435 456	28	0.000 000 003 725 290 298 461 914 062 5
536 870 912	29	0.000 000 001 862 645 149 230 957 031 25
1 073 741 824	30	0.000 000 000 931 322 574 615 478 515 625
2 147 483 648	31	0.000 000 000 465 661 287 307 739 257 812 5
4 294 967 296	32	0.000 000 000 232 830 643 653 869 628 906 25
8 589 934 592	33	0.000 000 000 116 415 321 826 934 814 453 125
17 179 869 184	34	0.000 000 000 058 207 660 913 467 407 226 562 5
34 359 738 368	35	0.000 000 000 029 103 830 456 733 703 613 281 25
68 719 476 736	36	0.000 000 000 014 551 915 228 366 851 806 640 625
137 438 953 472	37	0.000 000 000 007 275 957 614 183 425 903 320 312 5
274 877 906 944	38	0.000 000 000 003 637 978 807 091 712 951 660 156 25
549 755 813 888	39	0.000 000 000 001 818 989 403 545 856 475 830 078 125

Table B-8. Powers of 16, Base 10

16^n	n	16^{-n}
1	0	0.10000 00000 00000 00000 × 10
16	1	0.62500 00000 00000 00000 × 10^{-1}
256	2	0.39062 50000 00000 00000 × 10^{-2}
4 096	3	0.24414 06250 00000 00000 × 10^{-3}
65 536	4	0.15258 78906 25000 00000 × 10^{-4}
1 048 576	5	0.95367 43164 06250 00000 × 10^{-6}
16 777 216	6	0.59604 64477 53906 25000 × 10^{-7}
268 435 456	7	0.37252 90298 46191 40625 × 10^{-8}
4 294 967 296	8	0.23283 06436 53869 62891 × 10^{-9}
68 719 476 736	9	0.14551 91522 83668 51807 × 10^{-10}
1 099 511 627 776	10	0.90949 47017 72928 23792 × 10^{-12}
17 592 186 044 416	11	0.56843 41886 08080 14870 × 10^{-13}
281 474 976 710 656	12	0.35527 13678 80050 09294 × 10^{-14}
4 503 599 627 370 496	13	0.22204 46049 25031 30808 × 10^{-15}
72 057 594 037 927 936	14	0.13877 78780 78144 56755 × 10^{-16}
1 152 921 504 606 846 976	15	0.86736 17379 88403 54721 × 10^{-18}

Table B-9. Powers of 10, Base 16

10^n	n	10^{-n}
1	0	1.0000 0000 0000 0000
A	1	0.1999 9999 9999 999A
64	2	0.28F5 C28F 5C28 F5C3 × 16^{-1}
3E8	3	0.4189 374B C6A7 EF9E × 16^{-2}
2710	4	0.68DB 8BAC 710C B296 × 16^{-3}
1 86A0	5	0.A7C5 AC47 1B47 8423 × 16^{-4}
F 4240	6	0.10C6 F7A0 B5ED 8D37 × 16^{-4}
98 9680	7	0.1AD7 F29A BCAF 4858 × 16^{-5}
5F5 E100	8	0.2AF3 1DC4 6118 73BF × 16^{-6}
3B9A CA00	9	0.44B8 2FA0 9B5A 52CC × 16^{-7}
2 540B E400	10	0.6DF3 7F67 5EF6 EADF × 16^{-8}
17 4876 E800	11	0.AFEB FF0B CB24 AAFF × 16^{-9}
E8 D4A5 1000	12	0.1197 9981 2DEA 1119 × 16^{-9}
918 4E72 A000	13	0.1C25 C268 4976 81C2 × 16^{-10}
5AF3 107A 4000	14	0.2D09 370D 4257 3604 × 16^{-11}
3 8D7E A4C6 8000	15	0.480E BE7B 9D58 566D × 16^{-12}
23 8652 6FC1 0000	16	0.734A CA5F 6226 F0AE × 16^{-13}
163 4578 5D8A 0000	17	0.B877 AA32 36A4 B449 × 16^{-14}
DE0 B6B3 A764 0000	18	0.1272 5DD1 D243 ABA1 × 16^{-14}
8AC7 2304 89E8 0000	19	0.1D83 C94F B6D2 AC35 × 16^{-15}

Character	ASCII Binary	ASCII Hexadecimal	Hollerith
@	1 1 0 0 0 0 0 0	C0	0-2-8
A	1 1 0 0 0 0 0 1	C1	12-1
B	1 1 0 0 0 0 1 0	C2	12-2
C	1 1 0 0 0 0 1 1	C3	12-3
D	1 1 0 0 0 1 0 0	C4	12-4
E	1 1 0 0 0 1 0 1	C5	12-5
F	1 1 0 0 0 1 1 0	C6	12-6
G	1 1 0 0 0 1 1 1	C7	12-7
H	1 1 0 0 1 0 0 0	C8	12-8
I	1 1 0 0 1 0 0 1	C9	12-9
J	1 1 0 0 1 0 1 0	CA	11-1
K	1 1 0 0 1 0 1 1	CB	11-2
L	1 1 0 0 1 1 0 0	CC	11-3
M	1 1 0 0 1 1 0 1	CD	11-4
N	1 1 0 0 1 1 1 0	CE	11-5
O	1 1 0 0 1 1 1 1	CF	11-6
P	1 1 0 1 0 0 0 0	D0	11-7
Q	1 1 0 1 0 0 0 1	D1	11-8
R	1 1 0 1 0 0 1 0	D2	11-9
S	1 1 0 1 0 0 1 1	D3	0-2
T	1 1 0 1 0 1 0 0	D4	0-3
U	1 1 0 1 0 1 0 1	D5	0-4
V	1 1 0 1 0 1 1 0	D6	0-5
W	1 1 0 1 0 1 1 1	D7	0-6
X	1 1 0 1 1 0 0 0	D8	0-7
Y	1 1 0 1 1 0 0 1	D9	0-8
Z	1 1 0 1 1 0 1 0	DA	0-9
[	1 1 0 1 1 0 1 1	DB	12-5-8
\	1 1 0 1 1 1 0 0	DC	0-6-8
]	1 1 0 1 1 1 0 1	DD	11-5-8
↑	1 1 0 1 1 1 1 0	DE	7-8
←	1 1 0 1 1 1 1 1	DF	2-8

Character	ASCII Binary	ASCII Hexadecimal	Hollerith
blank	1 0 1 0 0 0 0 0	A0	no punch
!	1 0 1 0 0 0 0 1	A1	11-2-8
"	1 0 1 0 0 0 1 0	A2	0-5-8
#	1 0 1 0 0 0 1 1	A3	0-7-8
$	1 0 1 0 0 1 0 0	A4	11-3-8
%	1 0 1 0 0 1 0 1	A5	11-7-8
&	1 0 1 0 0 1 1 0	A6	12-7-8
'	1 0 1 0 0 1 1 1	A7	4-8
(	1 0 1 0 1 0 0 0	A8	0-4-8
)	1 0 1 0 1 0 0 1	A9	12-4-8
*	1 0 1 0 1 0 1 0	AA	11-4-8
+	1 0 1 0 1 0 1 1	AB	12
'	1 0 1 0 1 1 0 0	AC	0-3-8
–	1 0 1 0 1 1 0 1	AD	11
.	1 0 1 0 1 1 1 0	AE	12-3-8
/	1 0 1 0 1 1 1 1	AF	0-1
0	1 0 1 1 0 0 0 0	B0	0
1	1 0 1 1 0 0 0 1	B1	1
2	1 0 1 1 0 0 1 0	B2	2
3	1 0 1 1 0 0 1 1	B3	3
4	1 0 1 1 0 1 0 0	B4	4
5	1 0 1 1 0 1 0 1	B5	5
6	1 0 1 1 0 1 1 0	B6	6
7	1 0 1 1 0 1 1 1	B7	7
8	1 0 1 1 1 0 0 0	B8	8
9	1 0 1 1 1 0 0 1	B9	9
:	1 0 1 1 1 0 1 0	BA	5-8
;	1 0 1 1 1 0 1 1	BB	11-6-8
<	1 0 1 1 1 1 0 0	BC	12-6-8
=	1 0 1 1 1 1 0 1	BD	3-8
>	1 0 1 1 1 1 1 0	BE	6-8
?	1 0 1 1 1 1 1 1	BF	12-2-8

This appendix gives the mnemonic representation, hexadecimal code, definition and reference page in the text for each valid instruction. Instructions are grouped by programming type, as follows:

D-1 One-byte non-memory reference.

D-2 Two-byte non-memory reference.

D-3 Three-byte non-memory reference.

D-4 Two-byte memory reference.

D-5 Two-byte input/output.

D-6 Teletype controller reserved.

D-7 Punched-tape system reserved.

Table D-1. One-Byte Non-Memory-Reference Instructions

Mnemonic	Hexadecimal Code	Definition	Execution Cycles				Text Page
			OP 1	OP 2	OP 3	OP 4	
HLT	00	Halt with program counter at next location	1	1	1	1	35
CST	01	Change environmental status	1	1	1	1	42
SOV	02	Skip on current accumulator overflow and reset overflow indicator	1	1	1	1	38
SOVN	03	Skip on no current accumulator overflow and reset overflow indicator	1	1	1	1	38
SOD	04	Skip if current accumulator is odd	1	1	1	1	38
SODN	05	Skip if current accumulator is not odd	1	1	1	1	39
SAN	06	Skip if current accumulator is negative	1	1	1	1	36
SANN	07	Skip if current accumulator is positive	1	1	1	1	36
SAZ	08	Skip if current accumulator is zero	1	2	2	2	36
SAZN	09	Skip if current accumulator is not zero	1	2	2	2	37
SXZ	0A	Skip if current index register is zero	2	2	2	2	37
SXZN	0B	Skip if current index register is not zero	2	2	2	2	37
CLA	0C	Clear current accumulator to the set precision	1	2	2	2	32
CMA	0D	Complement current accumulator to the set precision	1	2	2	2	32

Table D-1. One-Byte Non-Memory-Reference Instructions (Continued)

Mnemonic	Hexadecimal Code	Definition	Execution Cycles				Text Page
			OP 1	OP 2	OP 3	OP 4	
IAR	0E	Increment current accumulator to the set precision	1	2	2	2	32
CIA	0F	Complement and increment current accumulator to the set precision	1	2	2	2	33
SP1	10	Set current operand precision to 1 byte	1	1	1	1	33
SP2	11	Set current operand precision to 2 bytes	1	1	1	1	34
SP3	12	Set current operand precision to 3 bytes	1	1	1	1	34
SP4	13	Set current operand precision to 4 bytes	1	1	1	1	34
SOF	14	Set current overflow indicator	1	1	1	1	35
ROF	15	Reset current overflow indicator	1	1	1	1	35
NOP	16	No operation	1	1	1	1	35
IXO	17	Increment current index register by the set precision	2	2	2	2	33
SR1	18	Shift current accumulator right one bit to the set precision	1	2	2	2	39
SR8	19	Shift current accumulator right eight bits to the set precision	1	2	2	2	39
RR1	1A	Rotate current accumulator right one bit to the set precision	2	2	2	3	40
RR8	1B	Rotate current accumulator right eight bits to the set precision	1	2	2	2	40
SL1	1C	Shift current accumulator left one bit to the set precision	1	2	2	2	40
SL8	1D	Shift current accumulator left eight bits to the set precision	1	2	2	2	41
RL1	1E	Rotate current accumulator left one bit to the set precision	2	2	2	3	41
RL8	1F	Rotate current accumulator left eight bits to the set precision	1	2	2	2	41

Table D-2. Two-Byte Non-Memory-Reference Instructions

Mnemonic	Hexadecimal Code	Definition	Execution Cycles				Text Page
			OP 1	OP 2	OP 3	OP 4	
Z	0=s, d	Nonexistent zeros register					
A	1=s, d	Current accumulator most-significant 16 bits					
C	2=s, d	Current accumulator least-significant 16 bits					
X	3=s, d	Current index register					
P	4=s, d	Current program counter					
B	5=s, d	Noncurrent accumulator most-significant 16 bits					
D	6=s, d	Noncurrent accumulator least-significant 16 bits					
Y	7=s, d	Noncurrent index register					
Q	8=s, d	Noncurrent program counter					
F	9=s, d	Peripheral adapter input/output register					
T	20 s d	Transfer source register to destination register	3	3	3	3	42
C	21 s d	Complement source register and transfer to destination register	3	3	3	3	43
I	22 s d	Increment source register and transfer to destination register	3	3	3	3	43
D	23 s d	Decrement source register and transfer to destination register	3	3	3	3	44
M	24 s d	AND source register into destination register	3	3	3	3	44
O	25 s d	OR source register into destination register	3	3	3	3	44
E	26 s d	Exclusive OR source register into destination register	3	3	3	3	45
A	27 s d	Add source register to destination register	3	3	3	3	45
MIN	3000	Modify interrupts according to current accumulator	2	2	2	2	47
CIS	3100	Copy interrupt status into current accumulator	2	2	2	2	49

Table D-2. Two-Byte Non-Memory-Reference Instructions (Continued)

Mnemonic	Hexadecimal Code	Definition	Execution Cycles				Text Page
			OP 1	OP 2	OP 3	OP 4	
CIM	3120	Copy interrupt mask into current accumulator	2	2	2	2	49
SIE	3200	Skip if in interruptable environment	3	3	3	3	48
SSH	3260	Skip on power-fail interrupt in halt mode	3	3	3	3	48
SS1	3220	Skip if SENSE switch 1 is off	3	3	3	3	47
SS2	3240	Skip if SENSE switch 2 is off	3	3	3	3	47
SS3	3280	Skip if SENSE switch 3 is off	3	3	3	3	48
IBD	3300	Interrupt system disable	2	2	2	2	49
IBE	3320	Interrupt system enable	2	2	2	2	49

Table D-3. Three-Byte Non-Memory-Reference Instructions

Mnemonic	Hexadecimal Code	Definition	Execution Cycles				Text Page
			OP 1	OP 2	OP 3	OP 4	
BRM	38- - - -	Branch and mark (store) current program counter	6	6	6	6	53
CSQ	39- - - -	Change environmental status and load noncurrent program counter	3	3	3	3	53

Table D-4. Two-Byte Memory-Reference Instructions

Mnemonic	Hexadecimal Code	Addressing Mode	Definition	Execution Cycles				Text Page
				OP 1	OP 2	OP 3	OP 4	
LOD	40- -	Direct	Load the	3	4	5	6	30
	50- -	Direct, current sector	current	3	4	5	6	
	54- -	Indirect, current sector*	accumulator	5	6	7	8	
	58- -	Indexed	from memory	3	4	5	6	
	5C- -	Indirect, zero sector*		5	6	7	8	
STO	60- -	Direct	Store the	3	4	5	6	30
	70- -	Direct, current sector	current	3	4	5	6	
	74- -	Indirect, current sector*	accumulator	5	6	7	8	
	78- -	Indexed	in memory	3	4	5	6	
	7C- -	Indirect, zero sector*		5	6	7	8	

*Two machine cycles are required for each additional level of indirect addressing

Table D-4. Two-Byte Memory-Reference Instructions (Continued)

Mnemonic	Hexadecimal Code	Addressing Mode	Definition	Execution Cycles OP 1	OP 2	OP 3	OP 4	Text Page
SUM	80 - -	Direct	Add memory	3	4	5	6	30
	90 - -	Direct, current sector	to the	3	4	5	6	
	94 - -	Indirect, current sector*	current	5	6	7	8	
	98 - -	Indexed	accumulator	3	4	5	6	
	9C - -	Indirect, zero sector*		5	6	7	8	
SUB	A0 - -	Direct	Subtract	3	4	5	6	31
	B0 - -	Direct, current sector	memory	3	4	5	6	
	B4 - -	Indirect, current sector*	from the	5	6	7	8	
	B8 - -	Indexed	current	3	4	5	6	
	BC - -	Indirect, zero sector*	accumulator	5	6	7	8	
AND	C0 - -	Direct	AND	3	4	5	6	31
	D0 - -	Direct, current sector	memory to	3	4	5	6	
	D4 - -	Indirect, current sector*	the current	5	6	7	8	
	D8 - -	Indexed	accumulator	3	4	5	6	
	DC - -	Indirect, zero sector*		5	6	7	8	
BRU	E0 - -	Direct	Branch un-	2	2	2	2	31
	F0 - -	Direct, current sector	conditionally	2	2	2	2	
	F4 - -	Indirect, current sector*		4	4	4	4	
	F8 - -	Indexed		3	3	3	3	
	FC - -	Indirect, zero sector*		4	4	4	4	

*Two machine cycles are required for each additonal level of indirect addressing.

Table D-5. Two-Byte Input/Output Instructions

Mnemonic	Hexadecimal Code	Definition	Execution Cycles OP 1	OP 2	OP 3	OP 4	Text Page
BTO	30 - -	Byte transfer out of current accumulator	2	2	2	2	45
BTI	31 - -	Byte transfer into current accumulator	2	2	2	2	46
SEN	33 - -	Sense device and ship if sense true	3	3	3	3	46
FUN	34 - -	Transfer function out and transfer a byte out of the current accumulator	2	2	2	2	46

Table D-6. Teletype Controller Reserved Instructions

Mnemonic	Hexadecimal Code	Definition	Execution Cycles				Text Page
			OP 1	OP 2	OP 3	OP 4	
BTO 01	3001	Transfer least-significant byte of current accumulator to the teletype controller input buffer	2	2	2	2	52
BTI 01	3101	Transfer teletype controller buffer to the least-significant byte of the current accumulator	2	2	2	2	51
SEN 21	3221	Sense for teletype controller output buffer readiness and skip if ready	3	3	3	3	52
SEN 41	3241	Sense for teletype controller input buffer readiness and skip if ready	3	3	3	3	52
FUN 01	3301	Enable teletype controller write interrupt	2	2	2	2	51
FUN 31	3321	Reset teletype controller	2	2	2	2	50
FUN 41	3341	Start teletype punched-tape reader	2	2	2	2	50
FUN 61	3361	Enable teletype controller read interrupt	2	2	2	2	50
FUN C1	33C1	Read one character on the teletype punched-tape reader	2	2	2	2	51

Table D-7. Punched-Tape System Reserved Instructions

Mnemonic	Hexadecimal Code	Definition	Execution Cycles			
			OP 1	OP 2	OP 3	OP 4
BTO 02	3002	Punch least-significant byte of current accumulator	2	2	2	2
BTI 02	3102	Read one tape character into least-significant byte of current accumulator	2	2	2	2
SEN 02	3202	Sense for punched-tape transfer readiness and skip if ready	3	3	3	3
FUN 22	3322	Start punched-tape reader	2	2	2	2
FUN 42	3342	Enable punched-tape interrupt	2	2	2	2
FUN A2	33A2	Stop punched-tape reader	2	2	2	2
FUN C2	33C2	Disable punched-tape interrupt	2	2	2	2

Character	Definition
O	Invalid operation mnemonic
U	Undefined symbol
M	Multiply defined symbol
P	Invalid operand precision
N	Invalid numerical operand
I	Invalid operation code addition
A	Addressing error