UNIVAC
Solid-State
COMPUTER

TYPE 7900 CENTRAL PROCESSOR 90
THEORY OF OPERATION
Service Manual No. 1

Remington Rand Univac
DIVISION OF SPERRY RAND CORPORATION

Copy No.

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"COMPANY CONFIDENTIAL

REGISTERED CIRCULATION

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SECTION I

INTRODUCTION

The purpose of this manual is to provide the reader with the fundamentals of computer logic and to apply these fundamentals to the theory of operation of the New Univac® Type 7900 Central Processor. Similar manuals have been prepared to acquaint the reader with the operating principles of the peripheral equipment of the system: the High-Speed Printer (or HSP); the Card-Sensing Punch Unit, 90 Column, or read-punch unit (RPU); and the Card-Sensing Unit, 90 Column, or card reader.

It is not within the scope of this manual to detail all of the logical operations carried out by the central processor. Section II, however, enables the reader to grasp the basic concepts of logical circuitry. Sections III and IV apply the knowledge of logical circuitry to detailed explanations of computer circuits and some of the more complex functions of the processor. Section V explains the operation of all of the types of instructions, except those few which control the input-output devices. In section VI, the basic theory of the major electronic circuit components, diodes, transistors, and magnetic amplifiers, is explained to enable the reader to analyze the circuits using these components.

1-1. FUNCTIONAL DESCRIPTION

The New Univac® system is composed of the processor, the card reader, the read-punch unit, and the printer.

The first step in processing is to store the program for the problem. Punched tabulating cards, bearing input information to be processed, then are placed in the card reader (figure 1-1). The card reader reads or senses the information represented by punched holes on the cards. The information is transferred from the card reader to the processor where the program stored previously in the magnetic storage drum controls the processing and computation of the input information.

A program, compiled by a programmer, is a sequence of instructions punched on tabulating cards. The instructions on the program cards are read by the card reader and transferred to the computer storage unit. The program automatically specifies and controls the operations required to solve a given problem.

The computed results or data processed in the processor are sent, as output, to the printer and to the read-punch unit. The output information may be printed on paper by the printer or punched on other tabulating cards in the read-punch unit or both. The cards placed in the input bin of the read-punch unit can be either prepunched with information or blank. In either case the input card is read at a read station before being punched with computer output at the punch station. The card is read again for checking purposes at a second read station and transferred to one of two output stackers.

Figure 1-1 shows a typical functional arrangement of the system. Variations of this arrangement are possible through program control. The programming and applications manuals on the system cover the many other possible arrangements. Table 1-1 lists the major characteristics of the New Univac ® system. Complete information on the input-output units can be found in the manuals which accompany these equipments.

1-2. PROCESSOR

The processor consists of the computing and processing circuitry, the storage drum, the operator's control panel and keyboard, and the system power supplies. The storage device is a cylindrical, magnetically coated drum with a capacity of 5000 computer words. In addition to this 5000-word capacity, which is known as main storage, other areas of the drum are set aside for timing purposes and input-output buffer storage. The buffer storage areas store information coming from or going to the input-output devices. Buffer storage enables the slower input-output devices to keep pace with the faster speeds of the processor and also allows the units of the system to operate in parallel.

All of the computing and processing circuitry explained in this manual is compactly contained on printed wiring boards, known as packages, within the processor cabinet. Arithmetic, control, and processing operations take place within the magnetic amplifier, transistor, diode, and miscellaneous circuitry on these packages. The clock circuits, which synchronize the operation of the magnetic amplifier components, and most of the system power supplies also are located in the processor cabinet.

Three of the four logical units necessary to a data-processing system are contained in the processor. These units, shown in figure 1-2, are: the control unit, the storage unit and the arithmetic unit. A general description of each of the three units follows; detailed descriptions of the units can be found in section III.

1-3. CONTROL UNIT. The control unit controls all of the operations of the system including the input-output unit. The major components of the control unit are: register C, the static register, the instruction decoder, the function encoder, and the operator's control panel.

Complete instruction words read from storage are stored in register C. Parts of these words are compared with storage addresses in the adder and comparator circuits in order to locate stored information or other instruction words. The two instruction code digits of the instruction word stored in register C are also stored in the static register. These digits are interpreted by the instruction decoder and converted into a function signal. This function signal is converted into a number of other function signals by the function encoder. The function signals control various computer circuits which cause the stored instruction to be executed.

The operator's control panel contains pushbutton switches and indicators which enable the operator to control manually the automatic operation of the system. Abnormal conditions in any of the four units also are indicated at the operator's panel. A keyboard on the panel enables the operator to type information into the processor or to alter the stored program.

1-4. STORAGE UNIT. The main component of the storage unit is the magnetic storage drum. Instructions or data are stored magnetically on the drum. Instructions are read from the drum to control calculations or processing; data is read from the drum to be operated upon by the instruction. The read-write circuits of the drum control reading from or writing onto the drum. Permanently recorded signals on the drum go to the timing circuits which synchronize and time all computer operations.

1-5. ARITHMETIC UNIT. Although the arithmetic unit has many components, the most important components are the three arithmetic registers and the adder and comparator circuits. All arithmetic and comparison operations are performed in the arithmetic unit. Each of the three registers, A, L, and X stores temporarily the ten digits of a word, which is usually the operand in an arithmetic instruction. The operands are operated upon in the adder

and comparator circuits, and the results are returned to one of the three registers.

1-6. CARD READER

The card reader reads information from punched input cards and transfers the information to the processor at a maximum rate of 450 cards per minute. The input cards are placed in the input bin. From the input bin, cards are automatically transported through the read stations to the output stackers. Each card is read by brush sensing at two read stations. The second read station enables the programmer to check the accuracy of the information read at the first read station. After the two readings the cards are transported to one of three output stackers. The program determines which stacker is used.

1-7. READ-PUNCH UNIT

The read-punch unit also reads information from input cards, but it is not a normal method of input to the system. The cards inserted into the read-punch input bin are usually blank cards or cards punched with a small amount of information. Under the control of the program the card is read by pin sensing at the first read station and is sent to the punch station where processed or computed information is punched into the card. The card moves to a second read station where the information on the card originally and the information added by punching are checked. The card is then transferred to one of two output stackers as determined by the program. The read-punch unit reads and punches cards at a rate of 150 per minute.

1-8. PRINTER

The information computed by the processor can be printed by the printer on many types of continuous forms at a speed of 600 lines per minute. Each line of print can contain a maximum of 130 characters. The number of spaces between lines is specified by the program. The printer contains 65 print wheels. Each wheel contains all of the characters available for printing. All of the characters to be printed on any one line are printed during the time necessary for one complete revolution of the print wheels. Under control of the program the paper is spaced before the printing of each line.

1-9. COMPUTER LANGUAGE

The purpose of this section is to familiarize the reader with the basic language of the computer.

1-10. COMPUTER WORDS

Information is processed by the computer in units known as computer words. A computer word is a group of digits constituting the smallest unit of information which can be processed or stored. Each computer word, which consists of ten digits and a sign, is presented in a space 12 digits long. The twelfth position is used as the spacing between words and is included as part of the word. Each digit of a word consists of four bits (refer to section 1-14). A bit is a binary character (either 0 or 1) which, when combined with other bits in a certain order, can represent a numeric digit. The bits of a digit are transferred in parallel and the digits themselves are transferred in series. To facilitate identification of every digit of a computer word, the following method of naming the digits is used throughout this manual:

Computer Word

Position Number	p11	p10	p9	p8	p7	p6	p5	p4	p3	p2	p1	p0
Digit	SBW	10	9	8	7	6	5	4	3	2	1	0

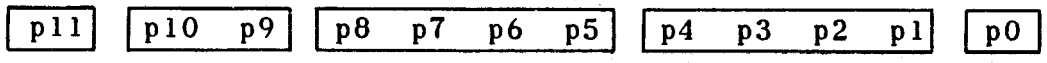
In this method, the 12 digit positions of a computer word are designated p0 through p11. The digits of a word are transferred throughout the computer with the least-significant digit (LSD) first, which is the reason for placing digit 1 or p1 at the right end of the word and the most-significant digit (MSD), digit 10 or p10, at the left end of the word.

Computer words are divided into two distinct groups: data words and instruction words. Data words contain information to be processed; instruction words contain instructions and addresses of data words to be used in the instruction. Instruction words, therefore, control processing and computations; data words are part of the information processed or computed. The difference between the data word and instruction word is a programming consideration only. The computer does not differentiate between the two types.

1-11. DATA WORD. A data word consists of a number of information digits which are to be processed or computed. The 12 digit positions of a data word contain ten digits, an algebraic sign, and a space between words (SBW). In the computer word given as an example above, the p0 digit position contains the sign of the data word; the p1 through p10 digit positions contain the numeric digits of the word (even though they may be zero digits); and the p11 digit position is the space between words (SBW) and contains a zero digit. The p10 digit is usually the most significant of the ten numeric digits; the p1 digit is the least significant of the ten digits.

1-12. INSTRUCTION WORDS. An instruction word consists of ten numeric digits and a space between words. The p0 digit of an instruction word is always a zero. The digits of an instruction word are divided into three groups as shown:

Instruction Word



SBW instruction code | m address | c address

Digits p10 and p9 are the instruction code digits. Every instruction given by the programmer consists of two digits. For example, when the programmer wishes to insert an add instruction into the program he places the digits 7 and 0 in the p10 and p9 digit position of the instruction word.

Digits p8 through p5 comprise the m address, which is the storage address of the operand to be used in executing the instruction. For example, when the programmer inserts an addition instruction into the program the operand must be read from the m address in the processor storage before the addition can take place. The programmer inserts the numerical address of the term which is to be read in the m address position of the instruction word. Digits p4 through p1 make up the c (control) address, which is the address of the next instruction. To construct a continuous program, in which the programmer programs one instruction after another in the desired order, each instruction word must contain the address in the processor storage of the next instruction word to be processed. The address of this next instruction word is known as the c address. The unused sign position of the instruction word always contains a zero.

1-13. SYSTEM CODES

The computer employs two types of coding for numeric (and alphabetic) information processed within the system: computer (UCT) code and Remington Rand (RR) card code. The punched tabulating cards used as the main method of input and output of the system are punched in the card code, in which digits are represented by six bits. The information in card code on the input cards is read from the cards under control of the program and transferred to the translator circuits of the processor. These circuits translate the six-bit card code into four-bit UCT code for internal use in the processor. When processing of the input information is complete, the four-bit UCT code is translated back into six-bit card code which can be punched on the output tabulating cards.

1-14. UCT CODE. The UCT code is a biquinary, four-bit code. Decimal digits 0 through 9 are represented as shown:

Decimal Value	Bit Position 4	3	2	1	
0	0	0	0	0	[a]
1	0	0	0	1	[b]
2	0	0	1	0	
3	0	0	1	1	
4	0	1	0	0	
5	1	0	0	0	
6	1	0	0	1	
7	1	0	1	0	
8	1	0	1	1	
9	1	1	0	0	
Decimal Value	5	4	2	1	
	Decimal Weight				

The four bits of this code are assigned weights from left to right of 5, 4, 2, and 1. For example, the decimal digit 4 is 0100, or 0 + 4 + 0 + 0. Examination of the code shows that the last three bits or lowest order bits of the digits 0 through 4 are repeated for the digits 5 through 9. The most significant bit of the combinations determines whether the digit lies in the 0 through 4 range or the 5 through 9 range. In the sign position of the word the 0000 combination denotes a + sign, and the 0001 combination denotes a minus sign.

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[a] Represents + when used in the sign position, p0.

[b] Represents - when used in the sign position, p0.

Six non-numeric code combinations in UCT code are available to the programmer. The non-numeric codes also can be processed through the computer but no value or weights are assigned to the bits of these combinations. These special codes are represented as shown:

Code
0101
0110
0111
1101
1110
1111

The method for manually inserting these non-numeric combinations into the computer is described in section 4-48.

1-15. REMINGTON RAND CARD AND CODE. The Remington Rand card shown in figure 1-3 is divided into two parts: the upper field and the lower field. Each field has six rows of punching positions and is 45 columns wide. Because there are 45 columns in each of the two fields, this card is referred to as a 90-column card. The 90 columns are numbered in the figure from 1 through 45 for the upper field and from 46 through 90 for the lower field. Each card, therefore, has 540 punching positions (90 columns times 6 rows).

The six rows of the upper field and the six rows of the lower field are numbered 0, 1, 3, 5, 7, and 9 as shown at the right of the card. In the figure, the punch in the 0 row of column 4 indicates a decimal value of 0, and a single punch in row 1 of column 2 indicates a decimal value of 1. Examination of table 1-2 shows that 0 and all of the odd decimal numbers are indicated by a single punch in the proper row. The even numbers are indicated by two punches: one punch in one of the 1, 3, 5, or 7 rows and also one punch in the 9 row of the same column. For example, punches in rows 1 and 9 of a column

represent a decimal 2, punches in rows 3 and 9 of a column represent a 4. Because the 1, 3, 5, 7, and 9 rows can indicate an odd or even number, depending upon whether or not there is also a punch in the 9 row of the same column, each of the 540 punch positions is marked with a notation (1_2, 3_4, etc.) which indicates the two possibilities.

Table 1-2 lists the decimal values, the rows to be punched in a column to represent each decimal value, and the bit-codes of the various punched-hole patterns. For example, if a hole is punched in row 0 of a column, the LSB of the card code is a 1 bit, or if a hole is punched in row 9, the MSB of the card code combination is a 1 bit. The least significant bit of the card code refers to row 0, the next lowest order bit refers to row 1 and so forth. A punched hole represents a 1 bit; no hole represents a 0 bit.

Table 1-1. Characteristics of the New Univac® System

Input-output characteristics are listed in the individual input-output manuals.

INSTRUCTIONS			
(A repertory of 32 instructions is available for the programmer. This table lists the seven types of instructions.)			
Arithmetic		Translate	
Comparison		Shift	
Transfer		Input Output	
Miscellaneous			

ARITHMETIC SPEEDS	
Addition	85 microseconds (addition of two 10-digit numbers)
Subtraction	85 microseconds (subtraction of two 10-digit numbers)
Multiplication	119 microseconds (minimum) 1785 microseconds (maximum)
Division	425 microseconds (minimum) 1955 microseconds (maximum)

COMPUTER WORDS	
Data word	12 digit positions (ten digit positions, one sign position and a space-between-words position)
Instruction word	12 digit positions (ten digit positions, unused sign position, and a space between words)

INFORMATION FLOW			
Bits	In parallel	Words	Serial-parallel
Digits	In series	Speed	707,000 digits per second

CODES			
UCT	Four bit binary coded biquinary	Card	Six bit Remington Rand code

Table 1-1. Characteristics of the New Univac® System (cont)

STORAGE	
Total Capacity	5000 words (main storage)
Capacity per band	200 words
Total number of bands	25
Normal-access bands	20 (one head per track)
Capacity Access time	4000 words 3400 microseconds, maximum (200 word times)
Fast-access bands	5 (4 heads per track)
Capacity Access time	1000 words 850 microseconds, maximum (50 word times)
Speed	17,670 rpm
Timing band	Provides channel addresses and synchronizes generation of timing pulses
Sprocket tracks (2)	Provide basic half pulse time frequency for clock
HSP (printer) buffer tracks (2)	Store 13 words, which constitute a printed line, from memory
HSR (card reader) buffer tracks (4)	Store 20 words (two complete input card readings)
RPU (read-punch unit) buffer tracks (4)	Store 30 words (two complete input card readings and one output card reading)

INPUT KEYBOARD			
Keys	0 through 9	Signs	Plus and minus keys
Non-numeric	Typed by simultaneous operation of numeric keys	Control	Control keys

Table 1-1. Characteristics of the New Univac ® System (cont)

TIMING	
Half pulse time	0.707 microseconds (time for a signal to be transferred through a magnetic core)
Pulse time	1.414 microseconds (time for passage of one digit)
Word time	17 microseconds (time for passage of one word)

Table 1-2. Card Code Combinations

Decimal Value	Row Punches	Card Codes
0	0	0 0 0 0 0 1
1	1	0 0 0 0 1 0
2	1 + 9	1 0 0 0 1 0
3	3	0 0 0 1 0 0
4	3 + 9	1 0 0 1 0 0
5	5	0 0 1 0 0 0
6	5 + 9	1 0 1 0 0 0
7	7	0 1 0 0 0 0
8	7 + 9	1 1 0 0 0 0
9	9	1 0 0 0 0 0

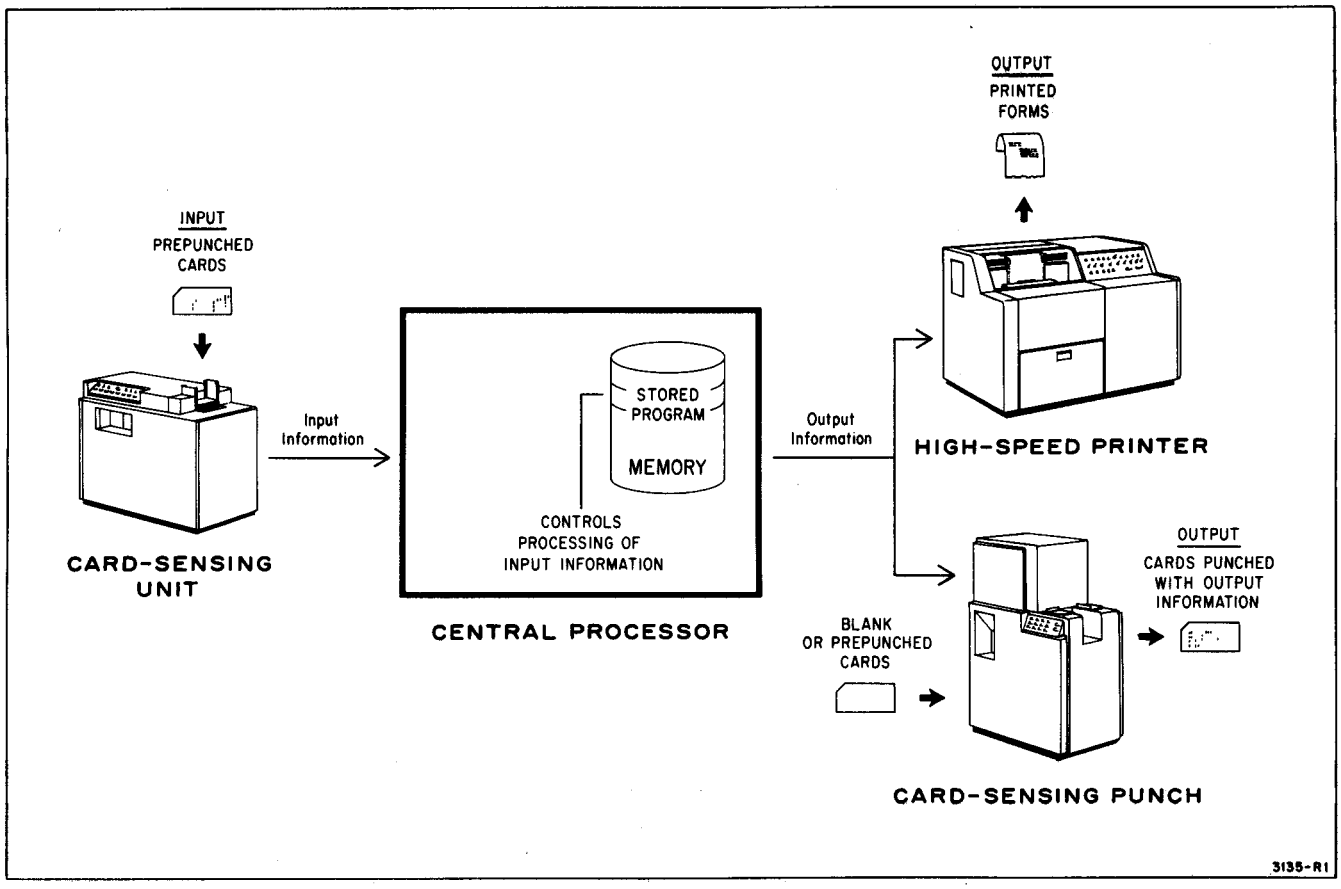


Figure 1-1. Typical Arrangement of New Univac® System

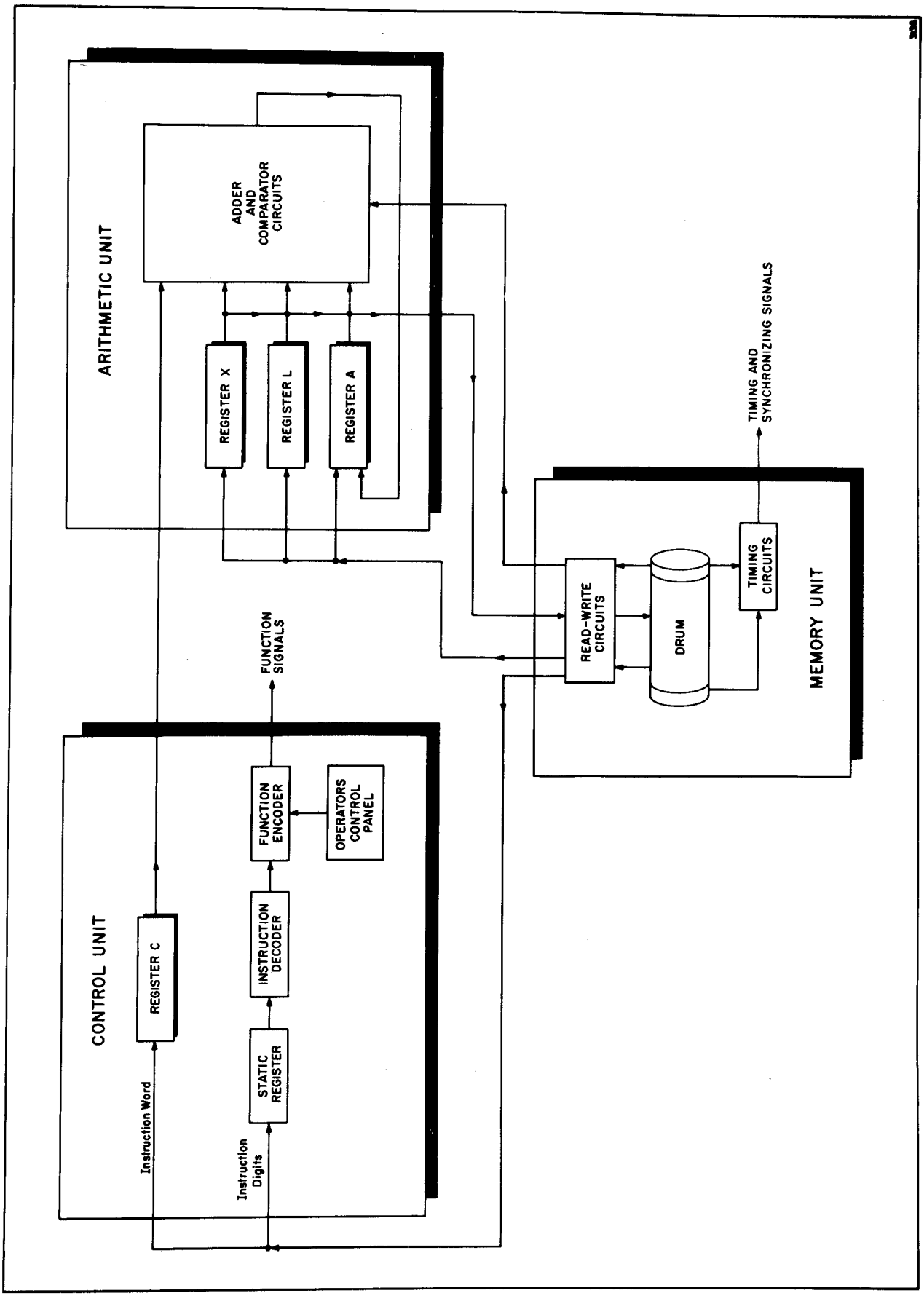


Figure 1-2. Central Processor Units

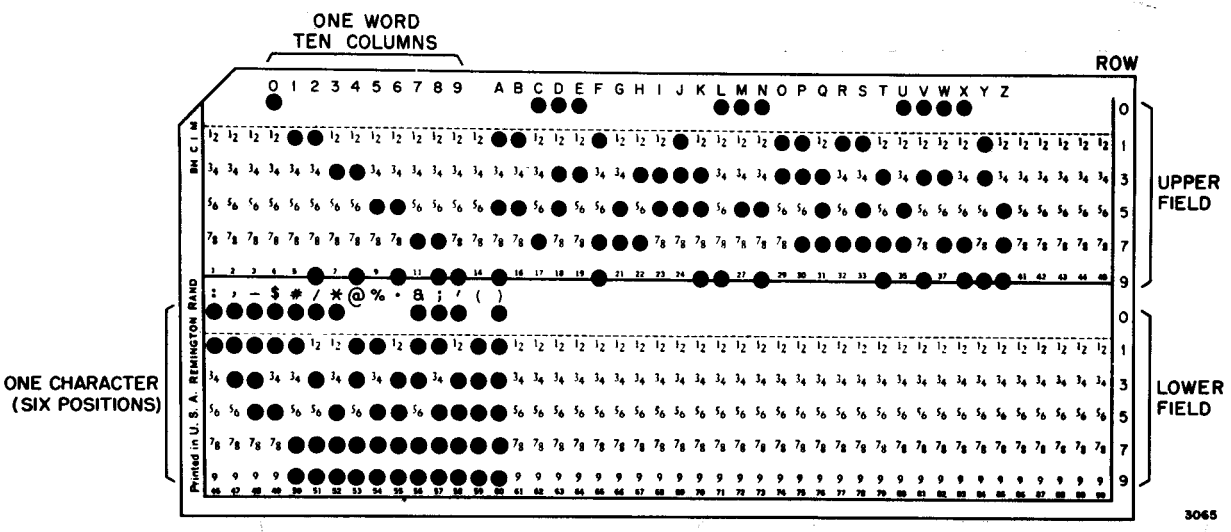


Figure 1-3. Remington Rand Tabulating Card

SECTION II

LOGICAL CIRCUITRY

2-1. INTRODUCTION

This section gives the reader the necessary background for understanding processor operations that are described in later sections of the manual. It also enables him to extract from the logical drawings detailed information not specifically supplied in the manual.

Whenever possible, the description is related to the logical drawings by examples of actual circuits. In certain instances, however, simplified versions of typical logical circuits are described as an introduction to the actual circuits shown on the drawings.

2-2. GENERAL

The logical drawings represent the actual processor circuitry in symbolic form. Because most of the processor circuitry consists of magnetic amplifiers and diodes, the logical drawings consist principally of diode and magnetic amplifier symbols connected by lines. Signals are indicated on the drawings by abbreviated reference designations or numbers.

This section explains the meaning of the symbols on the logical drawings and describes how the elements that the symbols represent are used to form the basic processor circuits. It also describes the different types of signals and the way they are represented on the drawings. In addition, the method by which timing signals are generated and used to synchronize operations throughout the processor is described.

Only the logical functions of the circuit elements are described here. The electronic theory and operation of magnetic amplifiers and other circuit elements are described in section VI, Electronic Circuitry.

2-3. SIGNAL POLARITY

Information is represented in circuitry by high signals or low signals. In this section, high and low signal conditions are distinguished from one another for illustrative purposes as shown in figure 2-1a.

A high signal is a definite positive voltage. A low signal is a zero voltage condition. A high signal may be thought of as representing a "pulse condition" and a low signal as representing a "no-pulse condition". Actually, a low signal is not negative, as suggested in figure 2-1a. It is illustrated as negative only to avoid the confusion that might result if the zero voltage condition were represented by a straight line.

2-4. DIODE CIRCUITS

The basic logical element in the circuitry is the diode circuit. A diode circuit is symbolized on a logical drawing as a segment of a circle (figure 2-1b). A diode circuit performs the logical functions of a gate (figure 2-1b, 1), or a buffer (figure 2-1b, 2), or when used as a connecting diode (figure 2-1b, 3), it performs no logical function at all.

Diodes transmit current in one direction but oppose current flow in the opposite direction. They prevent any signal from affecting the source of any other.

2-5. GATES

A gate is a circuit designed to produce a prescribed output signal only when every one of its input lines is in a prescribed state. A gate is represented by the diode symbol with a dot in the center. Gating is accomplished when low signals are present on all the input lines (figure 2-1c).

The gate produces a low output signal only when every one of its input lines is low. If one or more of the input signals is high, the output signal is high. High signals cannot be used to perform the gating function since the same high output would be produced whether only one or all of the input signals were high.

2-6. BUFFERS

A buffer is a circuit designed to produce a prescribed output signal when any one of its input lines is in a prescribed state. A buffer is represented by the diode symbol with a plus sign in the center. The buffer output is high when any one of its input lines is high (figure 2-1d).

2-7. DIFFERENCES

The difference between a gate and a buffer is a difference of logical definition. The same circuit that serves as a gate for low signals also serves as a buffer for high signals. The important point is that the necessary definitions have been made on the logical drawing. A diode circuit is represented as a gate if its essential function is to perform a gating function; otherwise, it is represented as a buffer or a connecting diode.

2-8. CONNECTING DIODE

A connecting diode (figure 2-1b, 3) is represented by a diode symbol with no dot or plus sign in its center. A connecting diode has only one input line and one output line. It has no logical significance other than to prevent the interaction of signals. Connecting diodes are shown on the logical drawings, however, to prevent the magnetic amplifiers that they connect from being confused with another type of magnetic amplifier which does not require a connecting diode (section 2-43).

2-9. MAGNETIC AMPLIFIERS

The basic symbol for the magnetic amplifier is a triangle. The point of the triangle indicates the direction of signal flow. Additional notation shows amplifiers as belonging to one of two electronic categories, and one of two logical categories.

2-10. ELECTRONIC DIFFERENCES

A central sine-wave clock circuit supplies power pulses to all the magnetic amplifiers. The magnetic amplifiers retime and reshape the input signals. Magnetic amplifiers can be divided electronically into two groups: those that receive A-phase power pulses, and those that receive B-phase power pulses.

The generation of power pulses is synchronized with the revolving storage drum by sprocket tracks on the drum (figure 2-3). Each sprocket track contains 2400 permanently recorded pulses. These pulses are read continually from the drum at the rate of one every 1.414 microseconds. This is the basic pulse rate of the computer. The sprocket pulses are fed to the sine wave clock which generates an A-phase and a B-phase power pulse for each sprocket pulse it receives. These power pulses differ by half a pulse time

and are 180 degrees out of phase. The letter A or B inside the triangle indicates the phase of the power pulse that drives the amplifier.

All the A-phase amplifiers in the computer receive an A-phase power pulse simultaneously. One-half pulse time later, all the B-phase amplifiers receive a B-phase power pulse. Amplifiers connected in series must alternate in phase so that an A-phase amplifier always precedes and follows a B-phase amplifier. Each power pulse has a positive half cycle and a negative half cycle (figure 2-3). During the half-pulse time that the power pulse is negative, the magnetic amplifier receives an input signal. For example, an A-phase amplifier receives an input signal during the half-pulse time that its A-phase power pulse is negative. During the next half-pulse time, the A-phase amplifier delivers an output signal to the B-phase amplifier next in line at the time the B-phase amplifier is receiving the negative half of its B-phase power pulse. This sequence of operation entails a delay of one half-pulse time in the passage of a pulse through an amplifier or one full-pulse time through both an A-phase and B-phase amplifier. The operation of the magnetic amplifier circuits is discussed in detail in section VI.

2-11. LOGICAL DIFFERENCE

Logically there are two types of magnetic amplifiers, complementers and non-complementers. A non-complementer produces an output signal of the same polarity as the input signal. The complementer inverts the input signal from high to low, or low to high.

A complementer is distinguished from a non-complementer on the logical drawings by a dot added to the basic amplifier symbol (figure 2-1e).

2-12. DECODING AND ENCODING MATRIXES

To simplify their presentation, it is often convenient to represent large gating and buffing arrays as decoding and encoding matrixes. Representing a gating or buffing array in this form does not change its logical significance.

2-13. DECODING MATRIX

A decoding matrix is an array of gates that convert a combination of several signals into one signal. A typical decoding matrix is the instruction decoder shown in

figure A3. The dots at the intersections of the lines of the instruction decoder represent diodes in the actual circuitry and each of the vertical lines represents a single gating circuit. For example, the vertical line labelled 26(B) represents a gating circuit with input signals STR1, $\overline{\text{STR2}}$, STR4, $\overline{\text{STR5}}$, STR6 and $\overline{\text{STR8}}$. The output of the circuit after inversion by the A-phase complementer is the 6A signal. The same circuit is redrawn in figure 2-2a to illustrate that it is a standard gating circuit. When all the inputs to the gate are low, the complemented output signal 6A is high; if one or more of the input signals is high, the output signal 6A is low. Each of the vertical lines in the decoding matrix of figure A3 represents a gating circuit such as is shown in figure 2-2a.

2-14. ENCODING MATRIX

Whereas a decoding matrix is an array of gates that convert a combination of several signals into one signal, an encoding matrix is an array of buffers that convert one signal into a combination of several signals. A typical encoding matrix is the function encoder in figure A4. As with the decoding matrix, the dots at the intersection of the lines represent diodes in the actual circuitry.

The 6A signal generated by the instruction decoder described in the preceding section is one of the many inputs to the function encoder. The 6A input line is connected by diodes to the lines which produce output signals 6, 55+, 67, 77, and 82A.

To illustrate how function signal outputs are generated, part of the function encoder is redrawn as an array of buffers in figure 2-2b. The high 6A signal from the instruction decoder generates low function signals 6, 67, 77, and high function signals 55+ and 82A. When signal 6A is high, the other inputs to the buffers are low.

Other A-phase signals from the instruction decoder also can generate some of the function signals that are generated by the 6A signal. For example, a high 9A signal would generate function signals 67, 77, and 82A. However, it would not generate signals 6 and 55+. In the actual circuitry, A-phase signals, other than those shown in figure 2-2b, can generate function signals 6, 55+, 67, 77, and 82A. To simplify the example, these are not shown.

2-15. COMPUTER TIMING

All processor operations are precisely synchronized. The movement of information within the processor or between the processor and the three input-output devices is synchronized by timing signals generated by the cycling unit. It is, therefore, necessary to understand computer timing in order to understand the operations of the computer.

2-16. PULSE TIME

The basic unit of computer timing is the pulse time. This is the time required for a pulse to pass a given point in the circuitry. A pulse is delayed one half-pulse time in passing through a magnetic amplifier or one full-pulse time in passing through both an A-phase and a B-phase magnetic amplifier. Because the four pulses that represent the four bits of a decimal digit are transmitted in parallel (section 2-35), one pulse time is also the time necessary for a digit to pass a given point in the circuitry.

2-17. WORD TIME

The basic unit of processor information is the 12-digit word, which requires 12 pulse times to pass a point in the circuitry. These 12 pulse-time intervals, hereafter referred to as one word time, are designated t0 to t11 (figure 2-4). Each of the 12 pulse-time intervals corresponds to the time necessary for a pulse to pass an A-phase and a B-phase amplifier in the circuitry. Each pulse time interval is, therefore, divided into two parts, an A-phase and a B-phase. Consequently, there are 24 distinct time intervals, each of one half-pulse time duration, to each word time. The timing signals that synchronize the operations of the processor are based on the 24-time intervals of a word time. During every word time, the cycling unit generates timing signals for each of the 24 time intervals.

The generation of the timing signals by the cycling unit is synchronized with the revolving storage drum. In addition to the 25 main memory bands, the storage drum has a timing band that contains 200 locations. The timing band locations are, however, not addressable by the programmer but contain permanently recorded pulses that perform various synchronizing functions. One of the functions of the timing band is to synchronize the generation of the timing signals with the revolving memory drum. For this purpose a special code combination (1101) is recorded in one of the 12 digit spaces in each of the 200 locations of the timing band. This special combination is read from the timing band once each word time of a drum revolution and then is fed to the cycling unit to begin the generation of timing signals.

2-18. TIMING SIGNALS

The cycling unit (figure A16) consists of a string of magnetic amplifiers connected by diodes. This circuit constitutes a one word-time delay; that is, a word time is necessary for a pulse to travel through the entire circuit. Such a pulse must pass through 24 magnetic amplifiers, each of which causes a delay of one-half pulse time.

The special code combination that initiates the generation of the timing signals is fed into gate 102 on the TS1, $\overline{TS2}$, TS3 and TS4 lines. (The notation TS1, $\overline{TS2}$, is explained in section 2-41.) Once each word time, the code combination 1101 is read from the timing bands to produce low signals on all of the input lines of gate 102. Thus a gating action takes place and once each word time the A-phase amplifier following gate 102 generates a high signal. This high signal is the t7A+ timing signal which is high for only a half-pulse time; at all other time intervals it is low. The plus sign following the signal designation indicates that it is a high signal only during the half-pulse time interval t7A.

The high t7A+ signal is an input to a B-phase complementer and a B-phase non-complementer so that a half-pulse time later, the B-phase timing signals (t7B+ and t7B-) of the t7 time interval are generated. The plus or minus sign following each t7B signal indicates that it is a high or low signal, respectively, only during the half-pulse time interval t7B. As the signal that is generated by the A-phase amplifier at the output of gate 102 progresses through the cycling unit, it generates A-phase and B-phase timing signals for each of the 24 half-pulse time intervals.

In addition to generating A-phase and B-phase signals for each time interval, the cycling unit generates complemented and non-complemented versions of the A- and B-phase signals during many of the 24 time intervals. For example, during the t0 time interval, the cycling unit generates signals t0A-, t0A+, t0B+, and t0B-.

In certain instances, timing signals, such as the t0B+ signal, are generated on two output lines. Logically, the two signal outputs are identical. They come from two sources to satisfy an engineering requirement for additional driving power, because the signals are needed to synchronize an unusually high number of operations throughout the processor. To distinguish between the two signal outputs, one is written primed (t0B'+) and the other is written unprimed (t0B+).

2-19. RELATION BETWEEN TIMING SIGNALS AND WORD TIME

One of the 200 locations of the timing band is shown in detail in the upper left corner of figure 2-5. The permanently recorded pulses in this location can be read by the timing-band read heads in one word time. Consequently, the special code combination (1101), in the digit position corresponding to the t6 time interval, is read once every word time or 200 times per drum revolution. Because the code combination 1101 is located in the t6 digit space, the timing signals for the t7A time interval are the first generated by the cycling unit after the 1101 combination is read. Then, for one word time, the timing signals for the remaining time intervals are generated by the cycling unit. At the end of one word time the combination 1101 in the next timing band location begins the cycle again.

2-20. SIGNAL NOTATION

In addition to the timing signals described above, there are three other types of signals in the processor: function signals, control signals, and information signals. Function and control signals control the execution of instructions in accordance with the program. Information signals represent information processed by the processor. The notations used to designate these three types of signals distinguish them from one another and from the timing signals. The use of the function, control, and information signals is described in detail in section IV, Theory of Operation. Only the notations used to designate these signals are described here.

2-21. FUNCTION SIGNALS

Most function signals (FS) are designated by numbers: FS1, FS6, FS77, etc. Some function signals have a plus sign following the number. The plus sign after the number indicates that it is a high signal during the execution time of an instruction which has this signal as one of its function signals. At all other times it is a low signal. The opposite is true for signals without a plus sign. Although most of the function signals are B-phase signals generated by B-phase amplifiers, there are a few A-phase function signals generated by A-phase amplifiers. These are distinguished by an A placed after the signal designation (FS14A, FS20A). On the logical drawings, all function signals are placed inside circles (figure 2-6).

2-22. CONTROL SIGNALS

A control signal is designated by an alphabetic notation that is usually an abbreviation of the name of the signal. As examples, EP is the abbreviation for the ending pulse signal, CT for conditional transfer, TS for time selection, and CP for complement.

2-23. INFORMATION SIGNALS

An information signal represents an information bit. (See the explanation of the biquinary code in section 1-14.) Because one decimal digit is made up of four bits, four information signals represent a digit. Each of the four bits of a decimal digit is assigned a bit position number. Bit 1 is always the least significant bit (LSB) of a digit, bit 2 is the next higher order bit, etc. Bit 4 is the most significant bit (MSB).

Information signals transferred within the processor are designated by an alpha-numeric notation. A letter or letters indicate the source of the signal and a number indicates the bit position of the signal. For example, information leaves register A on the A1, A2, A3 and A4 lines. The letter A identifies the output lines of register A while the number identifies the bit position.

2-24. LOGICAL FUNCTIONS

In the logical circuitry, the gating function is usually performed by a diode circuit and an amplifier in series. A typical gating circuit is shown in figure 2-6. The output signal from the A-phase complementer is high only when all of the input signals to the gate are low.

The gating circuit in figure 2-6 is typical of many of the gating circuits within the processor in that the input signals include a timing signal plus one or more signals of another type. In addition to the timing signal t11B-, this circuit has as inputs, function signal 1 and two control signals, OF and TS. The meaning of these function and two control signals is explained in section IV, Theory of Operation. The polarity of the timing signal t11B- is known for any time interval of any word time. The signal is high except for the half-pulse time interval t11B, when it is low. The polarities of the function signal and the two control signals do not change in accordance with any regular time sequence but depend on the program being processed.

In descriptions of gating circuits in this manual the following three expressions are often used: making a gate permissive, alerting a gate, and blocking a gate. The meaning of each of these expressions is described in the following three sections, with reference to figure 2-6.

2-25. MAKING A GATE PERMISSIVE

Most of the gating functions in the computer are performed at a definite time interval. The gating circuit in figure 2-6, for example, can perform the gating function only during the half-pulse time t11B when this signal is low. During any other time interval, the high timing signal prevents a gating function regardless of the polarities of FS1 and control signals TS and OF. If these signals are low at t11B, a gating action takes place and the gate is said to be made permissive. The term making a gate permissive means that a circuit which is designated a gate operates as a gate at some definite time.

2-26. ALERTING A GATE

Function signal 1 is normally high, but goes low during the execution time of an instruction which has FS 1 as one of its function signals. Assuming that such an instruction is being executed, FS 1 goes low at t0B, the beginning of some word time. The timing signal t11B-, however, does not go low until 11 pulse times later so that a gating action cannot take place before t11B. Whether gating takes place depends on the polarities of the signals on the OF and TS lines at t11B. When FS 1 goes low, it is said to alert the gate. In this manual, the expression alerting a gate means that a function or control signal input to a gate goes low one or more pulse times earlier than the time interval of a possible gating action and remains low until the interval ends.

2-27. BLOCKING A GATE

The gating circuit in figure 2-6 can perform the gating function only during the time interval t11B, when the t11B- signal is low. At any other time interval, the timing signal blocks the gate since it is then high, preventing the gate from performing the gating function regardless of the polarities of the other input signals. The term blocking a gate is used in this manual to mean that either a timing, control, or function signal input to a gate is high and, therefore, blocks any gating action.

2-28. BASIC LOGICAL CIRCUITS

The basic functions of buffing and gating circuits and the types of signals that pass through these circuits have been explained. Gates and buffers are used to build the flip-flop, a circuit used for a variety of purposes. This section explains the basic flip-flop and describes a few of its uses.

2-29. THE BASIC FLIP-FLOP

The flip-flop is a storage element that can maintain either of two stable states. It remains in one state until an input signal causes it to change to the other state. The two possible states of a flip-flop are the set state and the restored state. A simple flip-flop is shown in the set state in figure 2-7b and in the restored state in figure 2-8b. The notation used to designate the two outputs of this particular flip-flop, S and $\overline{S}$, means that the two signals are always opposite in polarity; that is, if $\overline{S}$ is low, S is high and if $\overline{S}$ is high, S is low. The unbarred and barred notation is used to identify the outputs of many of the flip-flops in the circuitry. For example, the complement flip-flop (CP FF) has two output signals, CP and $\overline{CP}$; the conditional transfer flip-flop has outputs CT and $\overline{CT}$. The fact that one signal is unbarred and the other barred indicates that they are always opposite in polarity. The use of the barred and unbarred notation for circuits other than flip-flops is discussed in section 2-41.

2-30. SETTING THE FLIP-FLOP

The flip-flop in figure 2-7a is set when gate 1, the set gate of the flip-flop, is made permissive by low signals A and B at time interval tOB. The timing signal tOB- to gate 1 is low and the timing signal tOB+ to gate 2 is high only during the time interval tOB. One pulse time later, signal S goes low and the signal $\overline{S}$ goes high. The flip-flop is kept in the set state by the circulating low S signal which is gated with the normally low timing signal into gate 2. Gate 2 is made permissive therefore so that a high signal into buffers 3 and 4 keeps signal S low and $\overline{S}$ high for at least the remainder of the word time as shown in figure 2-7b.

At the end of the word time, the flip-flop can remain in the set state or it can be restored. If signals A and B are still low at the next t0B time interval, gate 1 is made permissive again and the flip-flop remains set for another word time. During this same t0B time interval, the t0B+ signal into gate 2, the restore gate of the flip-flop, does not restore the flip-flop because the high signal into buffers 3 and 4 overrides the low signal from the restore gate into these same buffers. This action illustrates an important property of the flip-flops in the UCT circuitry. If a flip-flop receives a set and a restore signal at the same time interval, the set signal always takes precedence.

2-31. RESTORING THE FLIP-FLOP

To restore the flip-flop, set gate 1 must not be permissive at t0B, that is, signals A, or B, or both must be high at t0B. The timing signal into restore gate 2 goes high at t0B. Figure 2-8a shows how a flip-flop is restored by the timing signal into restore gate 2. One pulse time later, at t1B, signal S is high and signal $\overline{S}$ is low. Figure 2-8b shows the flip-flop in the restored state for one word time by the circulating high S signal into gate 2 and the normally high timing signal into gate 1. At the next t0B time interval, the flip-flop will be set only if both signals A and B into gate 1 are low. Otherwise, it will remain in the restored state.

2-32. THE SET AND THE RESTORED STATES

The set and the restored states are easily distinguished. The flip-flop in figure 2-7b is in the set state; S is low and $\overline{S}$ is high. The same flip-flop is shown in the restored state in figure 2-8b; S is high and $\overline{S}$ is low. The state of this flip-flop, therefore, indicates the polarity of the output signals. This is true of all the flip-flops in the logical circuits which have output signals with unbarred and barred notation. For example, the polarities of the two output signals of the complement flip-flop are indicated by the state of the flip-flop. When the CP flip-flop is set, CP is low and $\overline{CP}$ is high; when it is restored, CP is high and $\overline{CP}$ is low. In all the flip-flops that have a barred and an unbarred output, the flip-flop is set when the unbarred signal is low, and the barred signal is high. The flip-flop is restored when the barred signal is low, and the unbarred signal is high.

2-33. THE READ FLIP-FLOP

The flip-flop shown in figures 2-7 and 2-8 does not actually exist in the logical circuitry, although its logic is the same as that of any of the flip-flops in the system. A description of the read flip-flop on figure A19, for example, will show the similarity between this actual flip-flop and the typical flip-flop described in sections 2-29 through 2-32. The read flip-flop is so called because it controls the reading of information from the main storage.

The read flip-flop is similar to the flip-flop in figures 2-7 and 2-8 in that its state can be changed once every word time and it stays in one state for at least one word time. The read flip-flop, however, has three set gates, 42A, 42B, and 42C, only one of which operates at any time. Another important difference is that there is only one output signal, RD, from the read flip-flop, although this signal goes to two different circuits, gates 45A, 45B, and gate 47. There is no $\overline{RD}$ output signal because it is not logically necessary.

If any one of the set gates has all low input signals at t8B, the read flip-flop is set for one word-time; RD goes low at t9B and remains low for at least one word time. At the end of this word time, the t8B+ signal into restore gate 43 restores the flip-flop, provided that none of the three set gates has all low input signals. If the flip-flop is restored, it remains in this state until a later t8 time interval, when it can be set by all low input signals on one of the three set gates.

2-34. COUNTERS

The read flip-flop illustrates one use of a single flip-flop. Two or more flip-flops can be used to perform other logical functions such as that of a counter.

A counter is a circuit that counts the number of times a repeated operation is performed. For example, a row counter counts the rows of a card being read. Because there are 12 rows on a card, such a component must be able to count from 1 to 12.

A typical counter is shown in figure 2-9. It can count from 1 to 4 but is set to an initial reading of count 1 only by a jamming pulse which is an input to buffer 2 of flip-flop 1. The counter is counting 1 if flip-flop 1 is set, that is, if output signal 1 is low; it is counting 2 if flip-flop 2 is set, and so forth. The counter is stepped to counts of 2, 3, and 4 by successive stepping pulses which are inputs to the two connecting diodes. The counter can be stepped to the next count only if it has been counting the previous count.

The complete operating sequence of the counter is as follows: Initially the four flip-flops of the counter are reading zero, that is, all four flip-flops are in a restored state in which output lines 1, 2, 3, and 4 are high. First, a high jamming pulse into buffer 2 jams the counter to the 1 count by setting flip-flop 1 (output line 1 goes low). The first high stepping pulse is complemented by B-phase complementer 12 (figure 2-9) so that it is a low input to gate 3 where it is gated with the low output of flip-flop 1. Gate 3 is made permissive and sets flip-flop 2. The same stepping pulse goes through B-phase non-complementer 13 (figure 2-9), the output of which is a high input to gate 1. Flip-flop 1 is restored.

The low output signal from flip-flop 2 is gated with the next low stepping pulse at gate 6 to set flip-flop 3. The high stepping pulse to gate 4 restores flip-flop 2. The next low stepping pulse to gate 9 is gated with the low output of flip-flop 3 and sets flip-flop 4. The high stepping pulse to gate 7 restores flip-flop 3. Flip-flop 4 is restored by the next high stepping pulse to gate 10. The initial jamming pulse plus three stepping pulses enables the counter to count from 1 to 4.

If the counter had additional flip-flops, it could be made to count from 1 to any desired number. In the logical circuitry, counters similar to the one shown in figure 2-9 are used to count from 1 to 4, 1 to 10 and other series.

2-35. SHIFT REGISTER

A shift register is a circuit that consists of a number of flip-flops connected in series. Physically, the flip-flops of a shift register are similar to those

of the counter circuit (section 2-34). A shift register, however, does not count the number of times an operation is performed, but temporarily stores information. The shift registers in UCT consist of ten flip-flops connected in series. These ten flip-flops can store ten information bits, one bit per flip-flop.

A shift register converts information from parallel to serial form. Such an operation is necessary because information on a punched card is read by the input-output devices in parallel. For example, the ten least significant bits of a word are read in parallel. However, these ten bits must be written serially on the main storage drum. A shift register is the intermediary storage device that makes the conversion from parallel to serial form.

A typical shift register is shown in figure 2-10. It consists of ten flip-flops. The individual flip-flops are similar to those which make up the counter circuit (figure 2-9). The flip-flops of the shift register circuit differ from those of the counter circuit in that each flip-flop has an information input line to its buffer and the output of each flip-flop goes only to the set gate of the next flip-flop in line.

In a typical operation, ten bits of information enter the ten flip-flops in parallel on the ten information lines. A high signal on an information line is a binary 1 that sets the flip-flop to which it is an input. The output line of any of the flip-flops, therefore, is low if it is storing a binary 1. When the ten bits of information have been stored in the ten flip-flops, each flip-flop is storing a 0 or a 1, according to what was on its information line. Each flip-flop continues to store its pulse until a shifting pulse moves each bit of information one flip-flop to the right, so that if flip-flop 1 had a low pulse, flip-flop 2 now has a low pulse, and so forth. One pulse time after the first shifting pulse, the pulse that was circulating in FF 10 is shifted to the SR 1 (shift register 1) line and is sent eventually to the memory drum. The shifting operation for the shift register is identical with the stepping operation of the counter circuit (section 2-34).

After ten shifting pulses (assume one pulse time between each shifting pulse) all ten pulses originally stored in the ten flip-flops have been shifted to the SR 1 line. Thus, ten bits of information that were available in parallel before they entered the shift register are put on the SR 1 line serially, one pulse each pulse time, the rate at which they are written on the drum.

2-36. TIMING REFERENCE

Most of the logical drawings are marked in one or more places with timing references. These references make it possible to determine the location of any of the 12 digits of a word in the circuitry during any of the 24 intervals of a word time.

For convenient reference to the 12 digits of a word, each digit is assigned a position number. The notation used to indicate the 12 positions of a computer word is shown in figure 2-11. The six-digit number 0000781325 is assigned digit position numbers. When p0 is referred to, the reader knows that this is the sign (plus or minus) of the word, whereas p1 is the least significant digit, a 5 in this example, and so forth. Although this is only a six-digit number, it always moves in the computer as a complete word. The p7 to p10 digit positions of figure 2-11, therefore, contain zeros.

A typical timing reference notation is p0 = t0B. This notation is placed on a drawing so that it indicates the exact location in the circuitry where p0 (the sign of the word) is at the time interval t0B. Knowing this and knowing that a pulse is delayed half a pulse time in passing through a magnetic amplifier, the time at which p0 arrives at any point in the circuitry can be calculated. Reference timing is discussed further in the next section, which describes one of the circuits in detail.

2-37. CIRCULATING REGISTERS

The four circulating registers (the registers C, A, X, and L) are basically similar in that each can store one computer word. They are called circulating registers because the word of information is stored dynamically; that is, it constantly circulates in the register. The plus or minus sign associated with each computer word is stored not in the register but in flip-flops provided for this purpose (except for register C, for which there is no sign flip-flop). A computer word circulating in a register occupies 12 digit positions, counting the sign position and the space-between-words position, but only ten of these positions are occupied by information digits.

The uses of a circulating register are discussed in sections 3-13 through 3-50. In this section, register L is discussed in detail to show how information enters, circulates and leaves a circulating register.

In figure A10, register L consists of four subregisters, numbered 4 through 1 from top to bottom. Each subregister stores ten bits: subregister 1 stores the ten least-significant bits, subregister 2 stores the ten next higher-order bits, etc. For example, if the number 0000871342 were stored in register L, the distribution of the bits would be as shown in the diagram in figure 2-12.

2-38. INPUT GATES

A new word of information can enter register L through one of two sets of input gates. One group of input gates is numbered 2A, 2B, 2C, and 2D. Each of these gates has an input from the M buffer circuit: M1 goes to sub-register 1, M2 goes to sub-register 2, etc. The gates numbered 3A, 3B, 3C, and 3D are also input gates of register L and function in the same manner as the input gates just mentioned, except that the word of information which enters by these gates comes from the S buffer as indicated by the input lines, S1, S2, S3, and S4.

2-39. RECIRCULATING GATES OF REGISTER L

Gates 1A, 1B, 1C, and 1D are the recirculating gates of register L. A word of information in the register continues to circulate until cleared by the 57+ signal on the recirculating gates. Function signal 57+ is normally low, but during the execution step of an instruction that has 57+ as one of its function signals, 57+ goes high. The high 57+ signal blocks the recirculation gates so that the word of information in the register is prevented from circulating.

The notation p0 = t0B above gate 1D (figure A10) is the timing reference for the drawing. This notation means that p0, the sign of the word, is an input to the recirculating gates or either set of input gates at time t0B. Although the sign actually is blocked by timing signal t0B+, it is present as an input to the gates at t0B. With the aid of timing reference, the timing of a digit at any point in the register can be established. For example, digit p1 is an input to gates 1A, 1B, 1C, and 1D at t1B; p2 is an input at t2B, and so forth. Because it takes one pulse time for a pulse to travel through an A-and B-phase amplifier, the timing notation p0 = t0B in front of gate 1D (figure A10) is in agreement with the notation p0 = t11B after gate 6A.

One of the simplest instructions performed by UCT is the 30 (L) instruction which is: transfer the contents of the memory location designated by m to register L. The function signals for the 30 (L) instruction are 8, 57+, and 67. Only FS 8 and 57+ are considered here since FS 67 does not appear on figure A10. During the execution of the 30 (L) instruction, function signals 8 and 57+ allow a new word from the M buffer to enter register L. Function signal 57+ goes high for one word time and clears the information circulating in the register. When 57+ goes high, FS 8 goes low for one word time so that a new information word on the M1, M2, M3, and M4 lines can enter the register through input gates 2A, 2B, 2C, and 2D.

Information entering the register on the M lines is made up of 1 bits and 0 bits. A 1 on any of the M lines is a low signal that is gated with low function signal 8. The output of the gate goes through two complementers so that a binary 1 in a sub-register is a low signal. A binary 0 on the M lines is a high signal that circulates in a sub-register as a high signal. The biquinary code for a decimal 7, for example, is 1010. On the M lines a biquinary 7 would be: M1 high, M2 low, M3 high, and M4 low, in this way:

1	0	1	0
M4	M3	M2	M1
(low)	(high)	(low)	(high)

It takes one word time for a computer word to enter register L. At the end of this word time, FS 57+ goes low so that the new word of information can circulate in the register, and FS 8 goes high to block the input gates.

The fact that 57+ and 8 are function signals of the 30 (L) instruction is indicated on the logical drawings by the letter L which is placed next to function signals 57+ and 8. All letters next to function signals on the logical drawings indicate the instructions with which the function signal is associated. For example, figure A10 shows that the 57+ is also a function signal of the 77(K) instruction as is FS 16 on the other set of input gates. The 77(K) instruction is: transfer the contents of register A to register L.

2-40. OUTPUT GATES OF REGISTER L

The output gates of register L are gates 4A, 4B, 4C, and 4D, each of which has function signal 66 as an input signal. During most operations, the information word in register L is not being sent out to the L1, L2, L3, and L4 lines because FS 66 is usually a high signal and blocks gates 4A, 4B, 4C, and 4D. This signal goes low during the execution of an instruction which has FS 66 as a function signal so that the information word in register L is gated out to the L lines. The information word continues to circulate in the register after it is read out. Function signal 66 is a function signal of instructions 82(Q), 87(T), 85(M), and 55(D). This is indicated on the logical drawings by the presence of Q, T, M, and D near FS 66.

2-41. INFORMATION GATING CIRCUIT

The timing signals used throughout the computer are generated by the cycling unit which is activated each word time by a special code combination (1101) (section 2-18). The 1101 combination must be gated at the input gate of the cycling unit. This gating action is explained in detail in the following paragraphs.

Figure 2-13a shows the timing-band read amplifiers which are also shown on logical drawing A17. This circuit is always active; that is, the timing band read amplifiers are always reading the timing band signals. One of the digit spaces in each of the 200 locations of the timing band contains the special code combination 1101 which is read by the read amplifiers once each word time.

As illustrated in figure 2-13a, a high signal coming off the drum has a binary value of one; a low signal coming off the drum has a binary value of zero. One pulse time later, these signals become the TS1 to TS5 and $\overline{TS1}$ to $\overline{TS5}$ output signals. The TS5 and $\overline{TS5}$ signals, the check bit signals, are shown as outputs from the timing band read amplifiers, but are not inputs to the cycling unit input gate.

Figure 2-13a shows that the signals for each of the bits of the special code combination are available in two forms: a complemented form (TS1 to TS4) and a non-complemented form ($\overline{TS1}$ to $\overline{TS4}$). Figure 2-13b shows that the input gate to the cycling unit, which also is shown in drawing A16, has input signals TS1, $\overline{TS2}$, TS3, and TS4. When the combination 1101 is present on the TS lines, the gate shown

in figure 2-13b has all low signals on its input lines. The result is a high signal following the A-phase amplifier. This high signal is one of the timing signals generated for each of the 24 time intervals of a word time. Any code combination other than the special code combination results in a low output signal following the A-phase amplifier.

The gating action described in this section illustrates the important point that a signal can be inverted electronically without logically losing its identity. The zero of the special code combination is represented by a high signal coming off the drum. To put all low signals on the gate in figure 2-13a, it is necessary to make the $\overline{TS2}$ and not the TS2 signal an input to the gate. This low signal still represents a zero because it is the complement-version of the original signal. Electronically, the original high zero signal has been inverted; logically it still represents a zero.

2-42. SPECIAL CIRCUIT ELEMENTS

Special circuit elements are discussed in this section to aid the reader in interpreting the logical drawings. A detailed electronic discussion of these circuits is included in section VI, Electronic Circuitry.

2-43. ARITHMETIC AMPLIFIERS

The arithmetic amplifiers (figure 2-14a) are non-complementers and can be either A-phase or B-phase. The letter S (in the triangle with letter A or B) designates a special type of amplifier which is simpler and more economical to build than the standard amplifier. It is not necessary to put connecting diodes between arithmetic amplifiers. A special amplifier can drive only another special amplifier or a transition amplifier, designated by the letter T in the triangle with the letter A or B. The transition amplifier can drive only a standard non-complementer. Neither the special nor the transition type amplifiers can drive gating or buffing circuits.

The special and transition type amplifiers are used in the recirculation loops of the arithmetic registers. The main loop is made up of a series of special amplifiers. Near the output of each of the subregisters, a transition amplifier and a standard non-complementer precede the output line to provide the necessary driving force.

2-44. TRANSISTOR DRIVING AMPLIFIERS

The outputs of transistor driving amplifiers go to transistor circuits rather than to standard amplifiers. Transistor driving amplifiers perform the same logical functions as the standard complementers and non-complementers. The symbols for transistor driving amplifiers are shown in figure 2-14b. The difference between the square symbol and the triangle within the square in figure 2-14b indicates an electronic difference, not a logical difference.

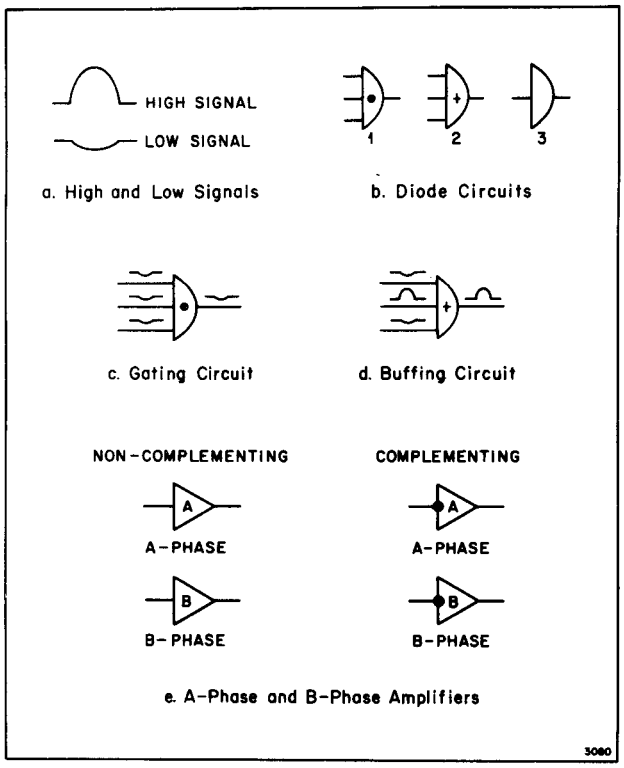


Figure 2-1. Basic Logical Circuit Elements

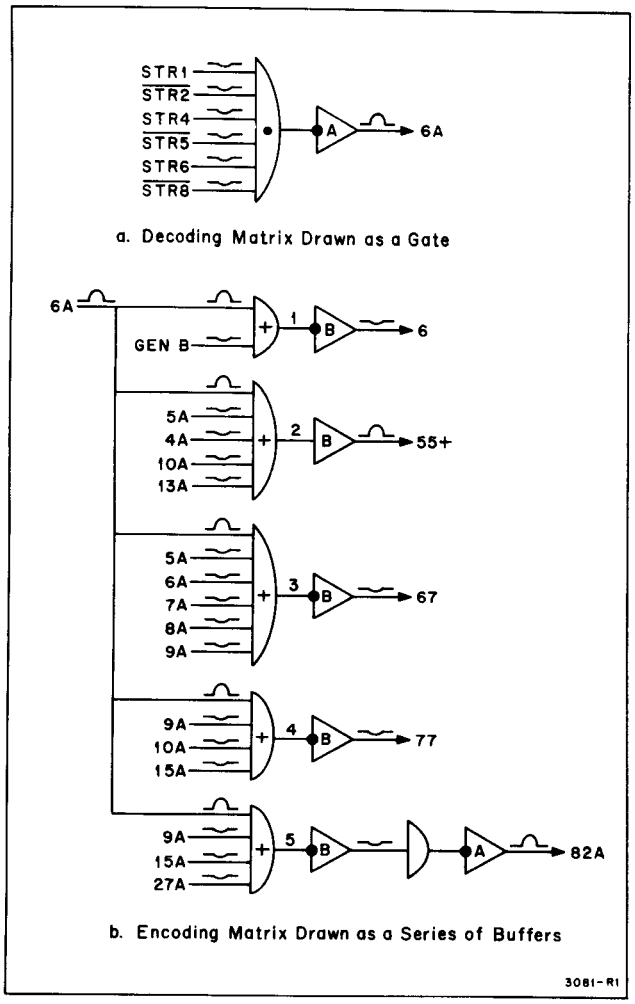


Figure 2-2. Decoding and Encoding Matrices

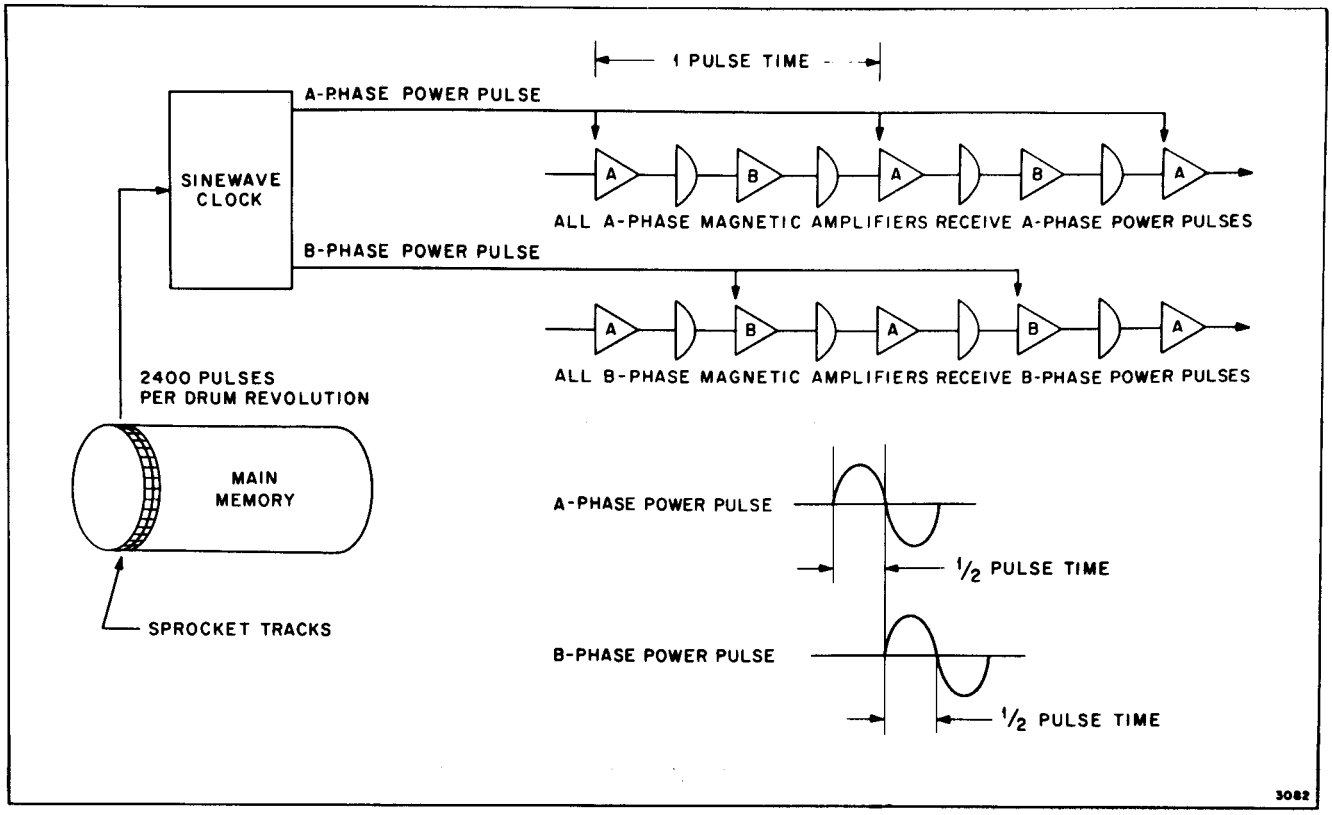


Figure 2-3. A-Phase and B-Phase Power Pulses

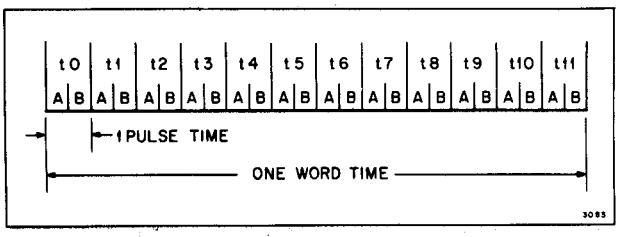


Figure 2-4. Twenty-Four Time Intervals of a Word Time

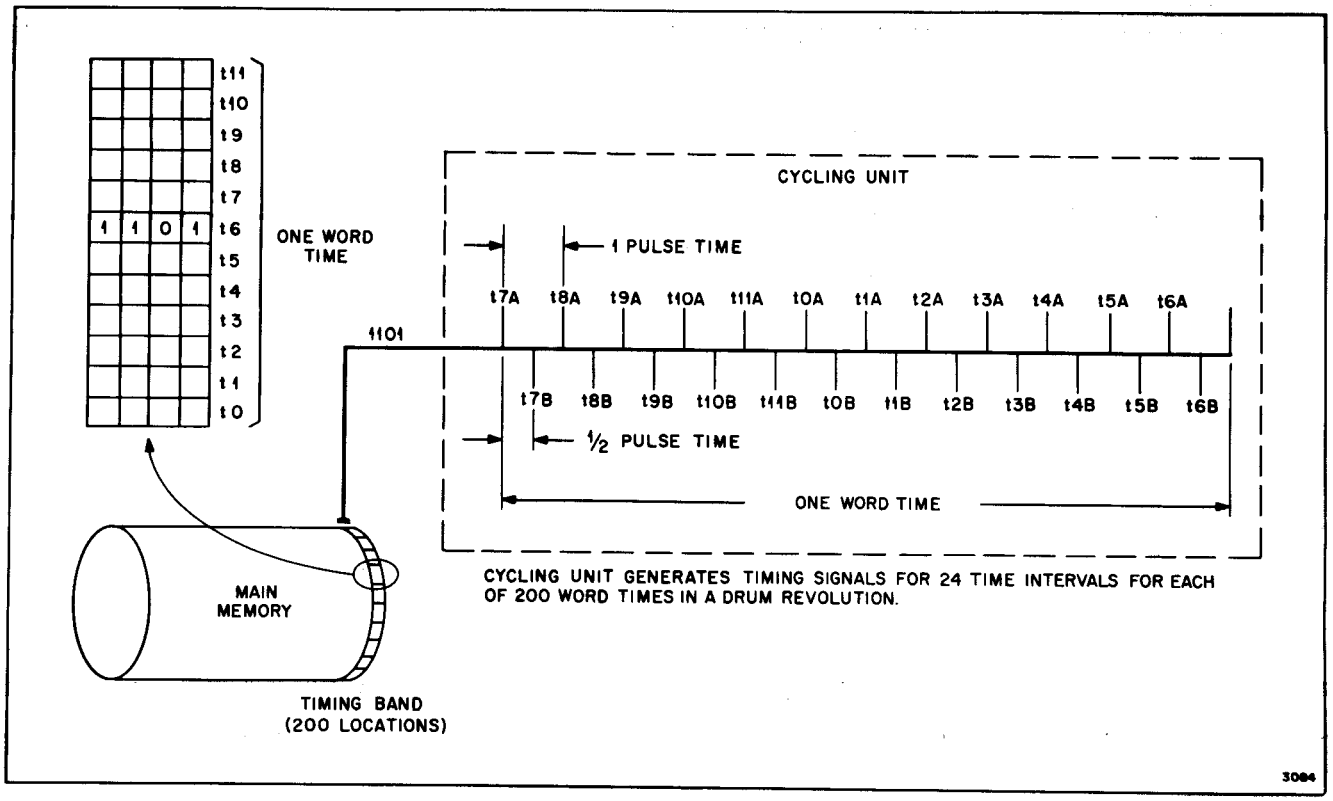


Figure 2-5. Relation Between Timing Signals and Word Time

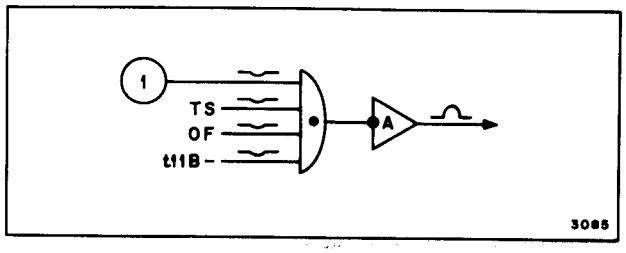


Figure 2-6. Typical Gating Circuit

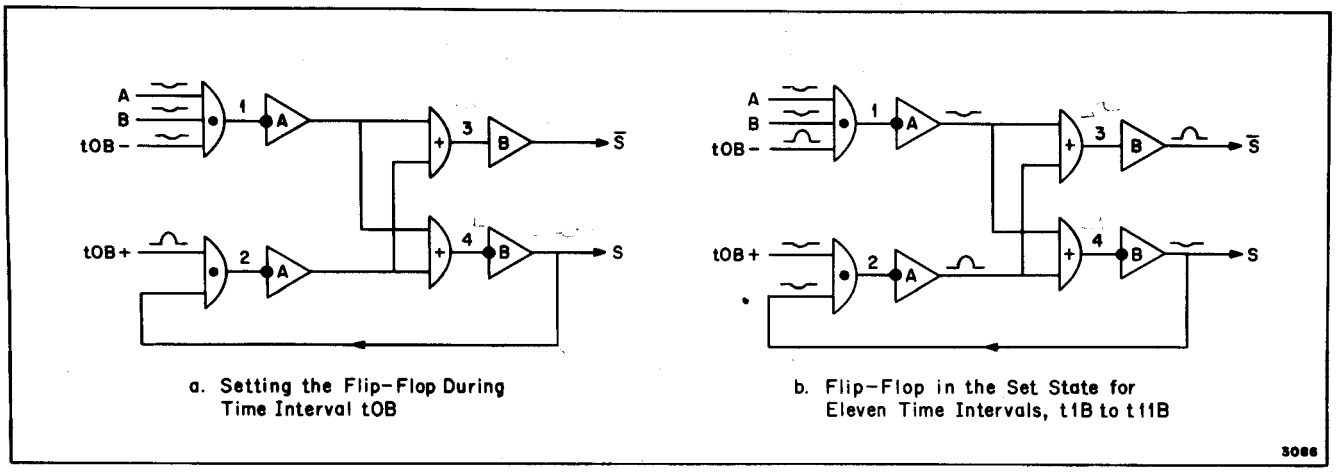


Figure 2-7. Setting a Typical Flip-Flop

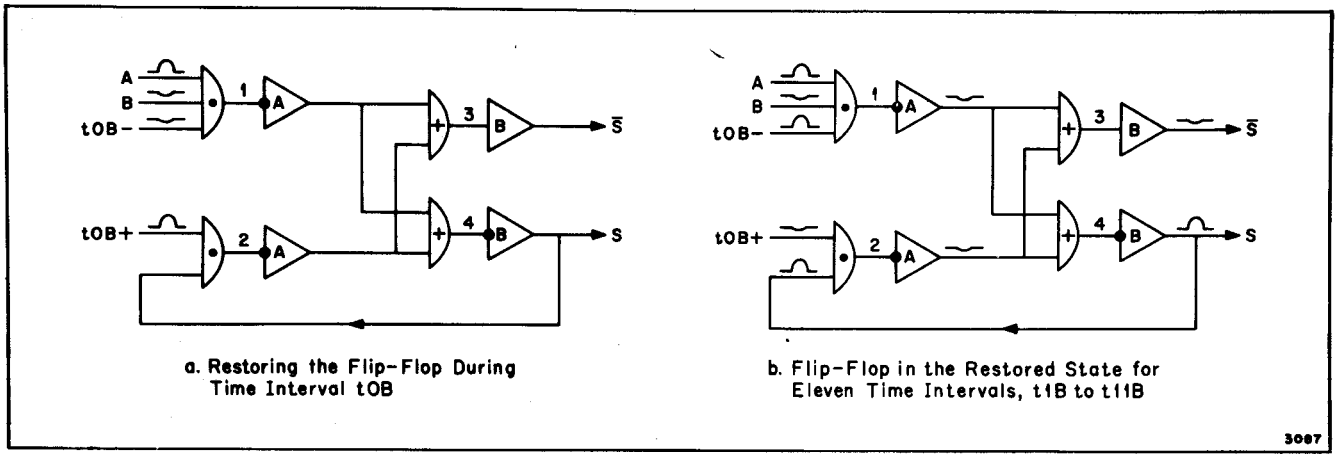


Figure 2-8. Restoring a Typical Flip-Flop

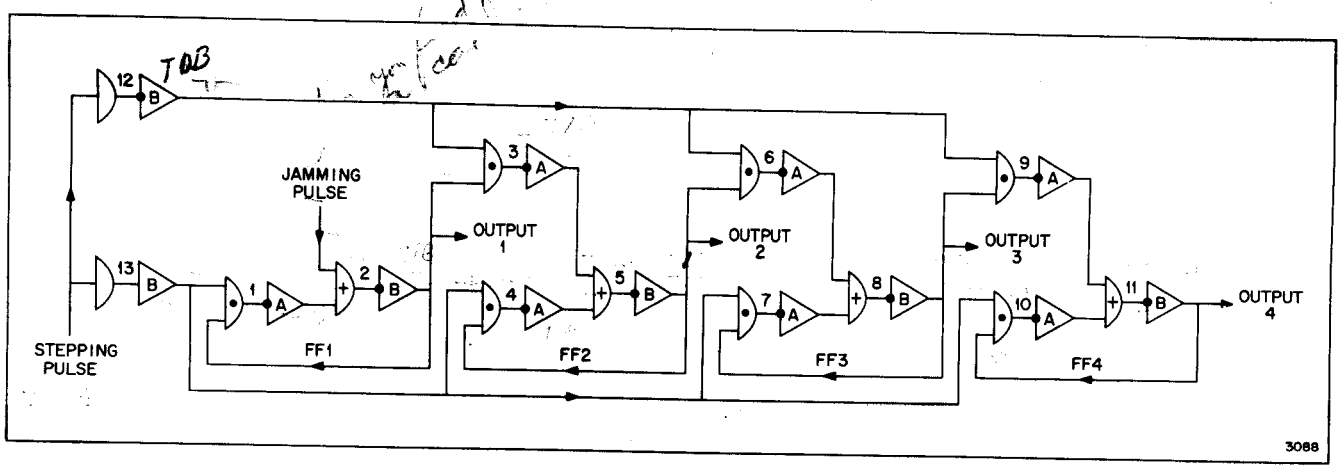


Figure 2-9. Typical Counter Circuit

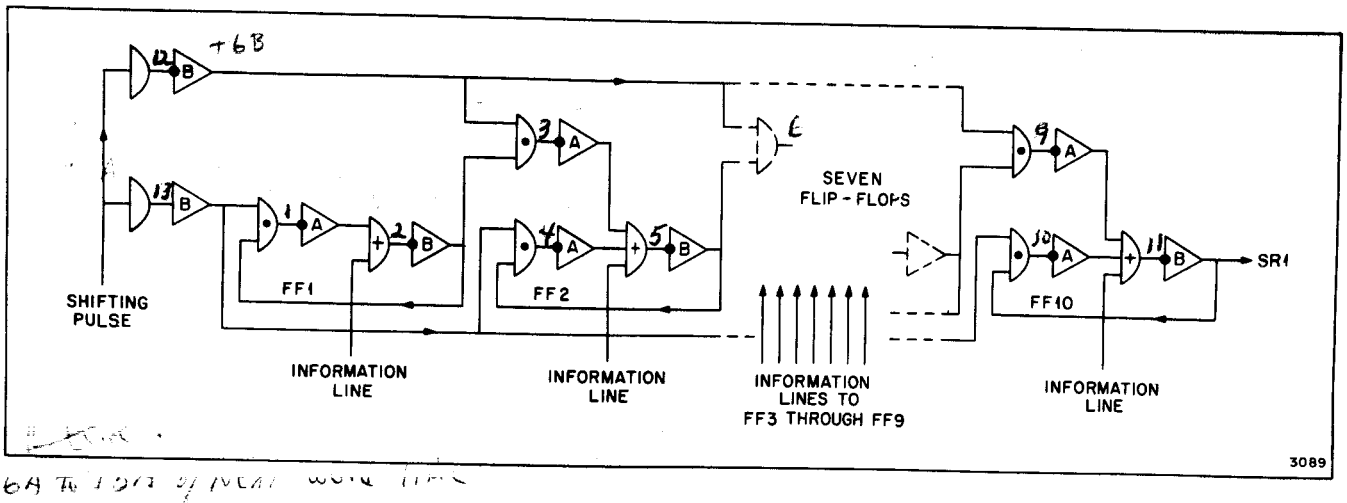
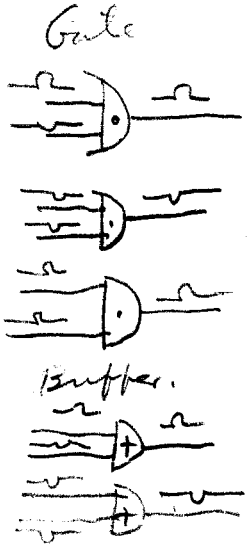


Figure 2-10. Typical Shift Register



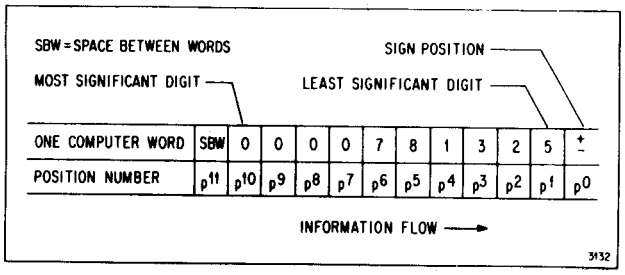


Figure 2-11. Digit Position Number of a Computer Word

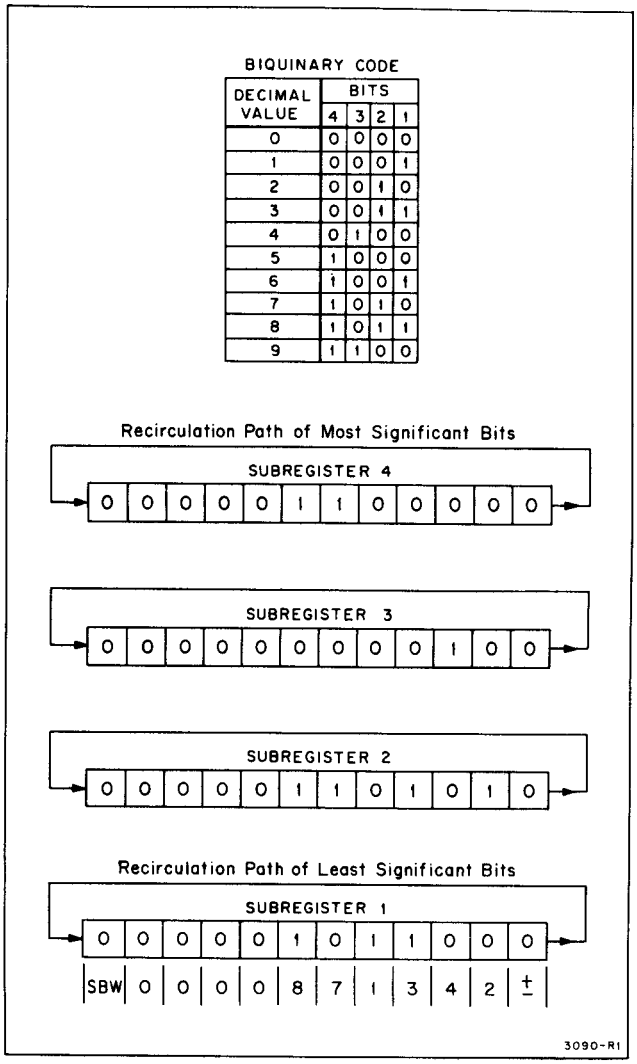


Figure 2-12. Distribution of Bits in a Circulating Register

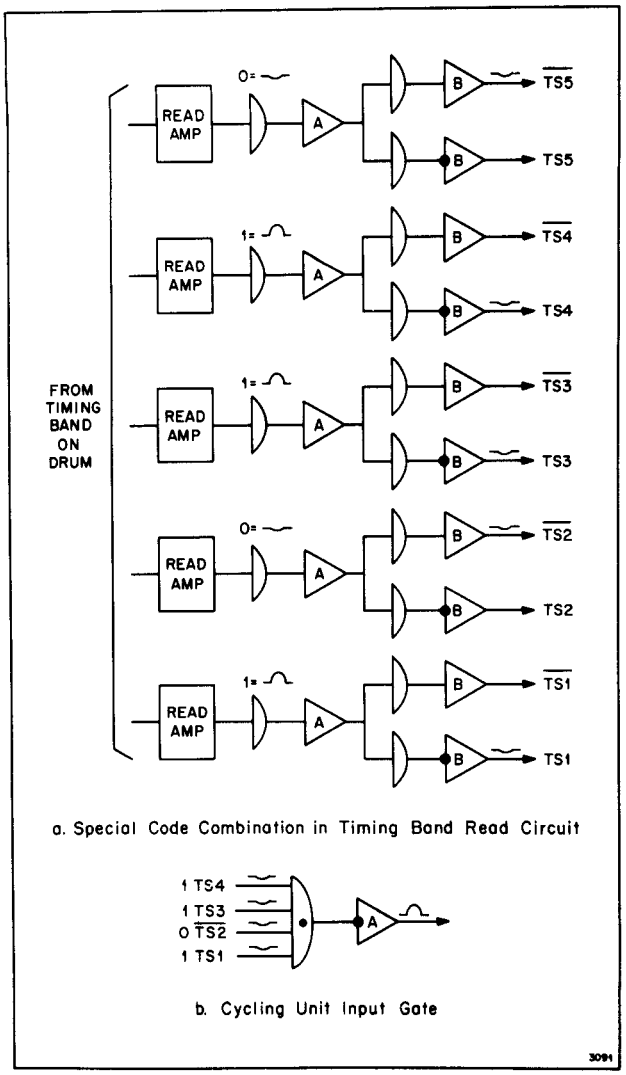


Figure 2-13. Special Code Combination in Timing Band Read Circuit

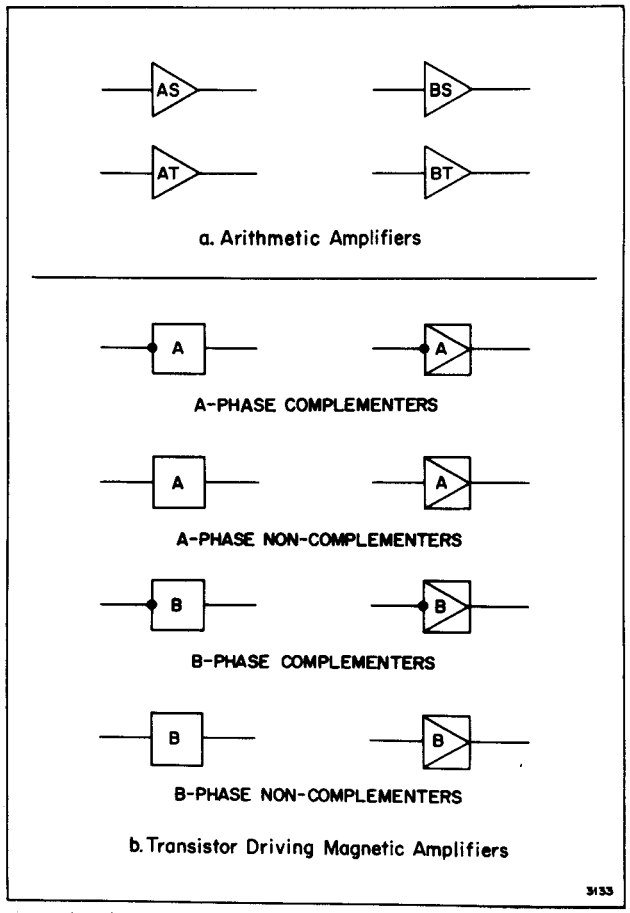


Figure 2-14. Special Amplifiers

SECTION III

DESCRIPTION OF CENTRAL PROCESSOR COMPONENTS

The purpose of this section is to familiarize the reader with the processor components, excluding the input-output synchronizers. Knowledge of the components, however slight, is necessary for the understanding of section IV, in which these components are referred to frequently within the more complex operations of the system. The reader should use this chapter not only as a preparation for section IV, but also as a reference. All of the text in this chapter is associated with the logical drawings in appendix A.

3-1. GENERAL

The processor system consists of four logical units: control, arithmetic, storage, and input-output. The input-output unit consists of the input-output devices and synchronizing circuits, which are treated in the input-output manuals. Section III deals only with the control, arithmetic and storage units which are shown in general block diagram form in figure 1-2.

3-2. CONTROL UNIT

The control unit interprets programmed or manually inserted instructions and controls the operations necessary to perform the instructions. Programs enter into the computer storage unit from punched cards or from the operator's keyboard. Each program instruction is transferred from the storage, in the sequence specified by the program, to the control unit. Elements of the control unit translate the biquinary representation of each instruction into signals which control the internal operations of the computer in performing the instruction.

The major components of the control unit are: the static register, the instruction decoder, the function encoder, register C, and the operator's control panel.

3-3. STATIC REGISTER

The static register (figure A2) consists of the following circuits: static register flip-flops, stepping gate, ending pulse buffer, D3 flip-flop, and I/O abnormal condition flip-flop (section 4-41).

3-4. STATIC REGISTER FLIP-FLOPS. The seven static register flip-flops statically store the seven bits of the two instruction digits. Because the third bit of the least significant digit is unnecessary for the staticizing operation, the flip-flops are numbered 1, 2, 4, 5, 6, 7, and 8. Each of the seven bits of the two instruction digits is stored in its respective flip-flop until the ending pulse restores all of the flip-flops.

An instruction word is read from storage into the M buffers. Prior to read-in of the M bits, an ending pulse restores the flip-flops. The seven bits of the two instruction digits (p10 and p9) of the instruction word become the M output signals of the buffers and go to the input gates of the seven static register flip-flops. The three bits of the least-significant digit, p9, of the two instruction digits enter flip-flops 1, 2, and 4 at gates 5A, 5B, and 5D. One pulse time later, the four bits of the most-significant digit, p10, of the two instruction digits enter flip-flops 5, 6, 7, and 8 at gates 6A, 6B, 6C, and 6D. A 0-bit on the M lines (a high M signal is a 0-bit) keeps the flip-flop restored, generating a low $\overline{\text{STR}}$ output. A 1-bit on the M lines (a low M signal is a 1-bit) sets the flip-flop, which then generates the low STR output. In this way, a 7-bit combination is stored in the seven flip-flops. A low $\overline{\text{STR}}$ output indicates a 0-bit; a low STR output indicates a 1-bit. The outputs of the seven flip-flops drive the instruction decoder and function encoder to generate signals to execute the instruction. The character "X" shown in any output combination of the static register flip-flops, such as 0X10, is used to balance a four-bit combination, or to indicate that the bit can be either a 1 or a 0. In all output combinations, the p3 bit is shown as an X because only three bits are required for the p9 digit.

The condition of the flip-flops can be changed by the input signals to each flip-flop and by the stepping gate or ending pulse buffer.

3-5. STEPPING GATE. The stepping gate steps flip-flops 1 and 2 to 1-outputs to advance the staticized instruction to the execution steps. During the arithmetic, shift, input-output test, and zero suppress instructions, function signal 64 (FS64) alerts gate 26, the stepping gate. If the ending pulse (EP) is low, meaning that the instruction is not yet completed, the gate is permissive. The high

output of the complementer steps flip-flops 1 and 2 to STR1 and STR2 outputs. This steps the static register to the second step of the instruction previously staticized. For example, the right circular shift instruction is staticized in the flip-flops as: 0011 0X10 (STR8 is the most-significant bit; STR1 is the least-significant bit) which is the combination for 32. In the first step (N1) of the instruction, FS 64 is generated. The stepping gate sets flip-flop 1, which was restored to $\overline{\text{STR1}}$, to an STR1 output. The stepping gate steps flip-flop 1 and flip-flop 2 unless one of these is in the set condition, as is flip-flop 2, in this case. The staticized combination is therefore stepped to 0011 0X11 (33) which drives the encoder and decoder to execute the second step of the instruction (N2).

3-6. ENDING PULSE BUFFER. The ending-pulse gates sample various circuits of the computer for indications that the execution of an instruction is complete. When these indications are present at one of the ending pulse gates as low signals, the ending pulse buffer generates a high EP signal. The EP signal goes to the restore gates of all seven static register flip-flops. A high at the restore gates restores each flip-flop to the barred outputs, such as $\overline{\text{STR1}}$ (0), clearing the seven flip-flops so that the next instruction digits can be staticized.

3-7. BLOCK READ FLIP-FLOPS. The two block read flip-flops block the storage read circuits during a search operation (either m or c address search) in which the contents of an arithmetic register have been called for rather than the contents of a storage address. The programmer addresses one of the registers by placing one of the following bit combinations in either the p1 (for c address) or p5 (for m address) position of the instruction word: 0101, 0111, or 0110. The 0101 combination causes readout from rA; 0111 causes readout from rX; and 0110 causes readout from rL.

During a search step the contents of rC are on the S lines. Gate 120 samples the S1 and S3 signals which, if low, indicate that either of registers A or X has been addressed. When gate 120 is permissive to these signals, the BRD1 flip-flop is set to a high block RD1 output. Gate 122 samples the S2 and S3 signals which, if low, indicate that either of registers L or X has been addressed. When gate 122 is permissive, the BRD2 flip-flop is set to a high block RD2 output. The high block RD1 and block RD2

signals block circuits which normally permit a readout from storage, generate function signals, and alert the output gates of the arithmetic registers for readout. When STR FF1 is stepped to a 1, indicating that the appropriate (m or c) search is complete, the STR1 signal makes gate 124 permissive, restoring both block read flip-flops.

3-8. RUN FLIP-FLOPS. In a normal search-for-next-instruction operation, the static register contains all zeros. When the next instruction is found, the static register is changed to a combination other than all zeros. This search operation can take up to 200 word times to complete. Under normal conditions, then, the longest period of time that the STR contains all zeros is 200 word times, in the search-for-next-instruction operation. Under abnormal, or computer stop conditions, however, the STR can contain zeros for a longer period because no instruction is staticized until the condition is remedied. The run flip-flops ensure that a computer stop condition does not turn off the RUN lights on the control panels before the 200 word times have elapsed. As a result, a normal search operation does not turn off the RUN lights to indicate a computer stop.

Only one TS1 at t11B- sentinel is recorded on the drum timing band; therefore, it is read from storage once every 200 word times. This sentinel sets the first run flip-flop once every drum revolution. A high ending pulse (EP) restores the flip-flop under normal conditions after every instruction. If no instruction is processed EP remains low during the 200 word times, and the flip-flop remains set. The next time the sentinel is read from the drum, it sets the second run flip-flop if EP is still low. The set output of the second flip-flop turns off the RUN lamps, indicating a computer stop.

Also associated with the static register are the D3 and I/O abnormal condition flip-flops (section 4-37). The D3 FF (section 4-36) initiates the third execution step of the divide instruction (D3). The D3 flip-flop is the only circuit, other than the instruction decoder, which generates function signals. It generates FS 32 and FS 32A which control the third step of division.

3-9. INSTRUCTION DECODER

The instruction decoder (figure A3) is a network of diode gates which receive the pulse combination outputs of the static register flip-flops and convert these outputs into function signals. Each flip-flop of the static register produces either of two possible outputs.

For example, static register (STR) flip-flop 1 produces either an $\overline{\text{STR1}}$ or an STR1 output. The overscored output signifies a zero. The output which is not overscored signifies a one when it is low. Seven such outputs from the static register make permissive only one of the diode gates in the instruction decoder.

If, for instance, the 50 instruction is staticized in the static register, the pulse combination sent to the instruction decoder is: STR8 (1), $\overline{\text{STR7}}$ (0), $\overline{\text{STR6}}$ (0), $\overline{\text{STR5}}$ (0) — $\overline{\text{STR4}}$ (0), $\overline{\text{STR2}}$ (0) and $\overline{\text{STR1}}$ (0). The pulse combination for the first digit of the instruction is 1000, for the decimal 5. The combination for the second digit is 0X00, for the decimal 0 ("X" indicating the unused third bit). Only the gate line labeled 50 is permissive to this 1000 0X00 combination, generating function signal 23A.

The signals generated by the instruction decoder are always sent to the function encoder, where the function signals that control the internal operations of the computer are generated. In addition, some of the signals generated by the instruction decoder are sent in parallel to other circuits, which they control. Therefore all signals generated by either the instruction decoder or function encoder are known as function signals.

The origin of a function signal usually can be determined by its phase. Signals originating in the instruction decoder are A-phase signals; those originating in the function encoder are B-phase signals. (Function signals 38A and 82A, generated by the function encoder, are the only exceptions.) When function signals are referred to, the presence of an A, following the signal number (such as FS12A), denotes an A-phase signal; the absence of an A (such as FS76) denotes a B-phase signal. All of the signals produced by the decoder to execute a specific instruction are high signals, with the exception of low signal 60A.

In addition to the STR outputs of the static register, three other signals affect the instruction decoder gates. These are control signals OR+, IER+, and $\overline{\text{SP}}$. The OR+ and IER+ signals from the computing circuits are present during the divide and multiply instructions to block the generation of certain function signals (sections 4-30,2; 4-35). The $\overline{\text{SP}}$ signal, which indicates a computer stop condition, also blocks the generation of any function signals when it is present on the instruction decoder.

3-10. FUNCTION ENCODER

In the normal execution of an instruction the function encoder (figure A4) receives an A-phase function signal from the instruction decoder and encodes this signal into a number of function signal outputs for use throughout the computer. The instruction decoder performs the logical function of a gate because a number of low inputs are necessary to generate a single output signal. The function encoder, although it is shown in figure A4 as a diode matrix similar to the instruction decoder matrix, performs the logical function of a buffer because any high input produces one or more output signals. A buffer on the function encoder is a vertical diode line on the matrix and every diode (shown as a dot) on that line is an input to the buffer. The high 1A signal, for example, goes to four buffers, which generate function signals 1, 58+, 74 and 63. In order for any buffer to operate and generate a function signal, one high input must be applied to it. In this example, high signal 1A is the signal presently being produced by the instruction decoder, therefore all other outputs of the instruction decoder to the function encoder are low. The low-signal inputs to the four buffers have no effect on the function encoder.

The function encoder receives inputs from sources other than the instruction decoder. Input signals from the control panel, the IER, OR and D3 flip-flops, and the printer control circuit, also generate function signals from the encoder.

3-11. REGISTER C

Register C (figure A1) stores the ten digits of the instruction word read from storage during a search-for-instruction operation. Four parallel subregisters store the two digits of the instruction, the four digits of the m address, and the four digits of the c address. When the instruction word is stored in register C, the p9 and p10 digits, which make up the instruction code, are also sent to the static register for storage. Storage of the same two digits in register C is for control panel display purposes.

Three output gates on each subregister of register C permit readout of part of the instruction word. The register display gates operate when the operator depresses the C button on the REGISTER SELECTOR on the control panel, generating signal RSC. This signal makes permissive the output display gates of rC, sending the contents of register C to the register display circuits. The instruction digits, m address, and c address are then visible, in biquinary form, on the control panel. The register contents are sent in parallel to the display circuits, and continue to recirculate in the register.

When the operator selects one of the arithmetic registers A, L, and X at the REGISTER SELECTOR, the output display circuits of these registers transmit the contents of their respective registers (signals A1$\overline{0}$D through A4$\overline{0}$D, X1$\overline{0}$D through X4$\overline{0}$D, and L1$\overline{0}$D through L4$\overline{0}$D) into the register display circuit of register C. The contents of the selected register are then sent to the control panel display lights. Controlling signals on the m address output gates and the c address output gates determine which address is to be sent to the comparison circuits of the arithmetic units (section 3-61). All outputs from register C, except the register display outputs, go to the S buffer and the memory selection circuits. The only inputs to the four subregisters are from the M buffer. Information stored in register C, as in the arithmetic registers, recirculates until a clear signal blocks the recirculation gates.

3-12. OPERATOR'S CONTROL PANEL

The operator's control panel, on the processor cabinet, contains the switches and indicators necessary for manual control of the computer. The engineer's panel (concealed) on the same cabinet is primarily for troubleshooting purposes and is therefore discussed in the maintenance manual. Each of the three input-output devices has a separate panel for controlling the operations of the individual device. These panels are treated in the manuals for each device. The descriptions of the major operator-controlled operations are listed in section 4-42.

3-13. ARITHMETIC UNIT

The arithmetic unit consists of the logical circuits which perform the various computing functions of the system. Components of the arithmetic unit also process all of the non-computing processor instructions and some of the input-output instructions.

3-14. REGISTER A

Register A and the two other arithmetic registers, L and X, are circulating registers. The logical operation of a circulating register is described in section 2-37. Register A (figure A8) stores the ten decimal digits of a computer word in four 12-bit subregisters. The gates and buffers that control input to and output from register A are described in this section.

3-15. INPUT GATES. The input gates, when alerted by function signal 77, permit information from the M buffers and S buffers to enter register A. When the outputs of the M buffers are to be read into register A, a blocking signal is applied to the S buffers. The blocking signal keeps the S inputs to register A low so that the M inputs can enter. In other instructions the M buffers are similarly blocked to enable the S buffer outputs to enter the input gates of register A.

3-16. LEFT SHIFT GATES. During either a left shift instruction or a left shift in division, lengthening the recirculation loop shifts left the contents of register A. The lengthened recirculation path for the first three bits of each digit is through the S buffers (figure A7) and the complementer circuit (figure A11). The outputs of the complementer are the S1C, S2C and S3C signals which go to the left shift gates of register A. Because the complementer circuit can accommodate only three inputs, the recirculation path for the fourth bit of each digit is lengthened within the register and becomes the A"4 signal, which goes to the left shift gates at the same time as the complementer outputs. Alerting signals, when present, make the left shift gates permissive to the left-shifted contents of register A.

3-17. RIGHT SHIFT GATES. During either a right shift instruction or a right shift in multiplication shortening the recirculation path shifts right the contents of register A. This is done by blocking the normal recirculation path and reading out of register A one pulse time early. These early outputs, labeled A'1, A'2, A'3 and A'4, are returned to register A through the right shift gates. Function signal 59 alerts the gates to the early outputs of the register.

3-18. QUOTIENT INPUT GATES. In the division instruction, the quotient digits are computed in the multiplier/quotient counter (MQC) (section 3-74). Each computed quotient digit is stored in register X. In the final step of division (D3), the quotient is transferred from register X, through the multiplier quotient counter to register A. It enters the register by way of the quotient input gates. Function signal 32 alerts the gates to the quotient-digit signals Q1 through Q4.

3-19. MULTIPLIER SENTINEL GATE. In the first step of multiplication a sentinel is inserted automatically into register A. The sentinel stops the process after the multiplicand has been multiplied by the last multiplier digit. Function signal 13 alerts the multiplier sentinel gate which jams ones into the A1 and A3 subregisters while zeroes remain in the A2 and A4 subregisters. As a result a bit combination of 0101, which will be decoded later as the multiplier sentinel, is placed in register A.

3-20. LSD COMPLEMENTER GATE. Alerted by a control signal OR, the least-significant digit (LSD) complementer gate complements the digit contained in the space-between-words position (SBW) of register X during division. The complemented digit becomes the LSD of register A. The contents of the SBW position of register X can be either zero or a nine in the division process. The $\overline{X4D}$ signal is an output of the most-significant bit (X4) subregister and, as can be seen in the code, the $\overline{X4D}$ output of register X does indicate whether the contents of the space-between-words position is a 0 or a 9. If a nine (1100) occupies the SBW position of rX, the $\overline{X4D}$ signal from register X is high. The LSD complementer complements the signal to a low and sends a zero combination (0000) into register A. If a zero occupies the SBW position of register X the $\overline{X4D}$ signal from that register is low. The LSD complementer complements the signal to a high, placing a 1100 (9) combination into register A (section 4-35,1).

3-21. RECIRCULATION GATES. The recirculating signals of the four subregisters of register A are A1, A2, A3 and A4. These signals go from the last amplifier of the subregisters into the recirculation gates, where they reenter the register. The recirculation gates are normally permissive to the recirculating signals. When function signal 55+ is high, however, it blocks the recirculation gates and the contents of the register read out to the S buffers and to whatever circuit is presently permissive to the S buffer outputs. Thus the register is cleared when the high blocking pulse is applied. Another input to the recirculation gates is the output of the zero suppress gate.

3-22. ZERO SUPPRESS GATE. When FS 38A is present during a zero suppress instruction, the zero suppress gate samples the Z1 through Z10 outputs of register X. If any of the Z signals is high, the gate permits the normal recirculation of the register to continue. When all Z signals become low, however, the zero suppress gate places a high, blocking signal on recirculation gates 27 and 28, suppressing the code combinations for both zeros and commas. The card-code combination for zero is 00 0001; the combination for comma is 00 0011. As a result, only A1 and A2 subregisters need be cleared to suppress both punching and printing zeros and commas.

3-23. REMINGTON RAND TO UCT TRANSLATOR GATES. The RR to UCT translator gates translate the Remington Rand (RR) card code into UCT computer code, the only code that can be processed by the computer. Only numeric characters can be translated correctly into computer code. The six bits of the card code are stored, four bits in register A and two in register X. On a translate instruction, that part of the code stored in register A is transferred through the S buffers to the S lines. The part of the code stored in register X is transferred through the M buffers to the M lines. The code combination on the M and S lines goes to the translator gates which, when alerted by function signal 17, convert the six-bit code to four-bit code. The four-bit code is stored within register A. Table 3-1 shows the gates of the translator, the six-bit code signals received from the M and S lines, and the resulting four-bit code. The first two columns show the contents of register X and register A in card code. The third column shows the row positions on the cards which must be punched for each decimal digit. The fourth column lists the input code-bits received by each gate. The four-bit codes resulting from the translation are listed in the last column. (See section 5-10.)

3-24. UCT TO RR TRANSLATOR GATES. These gates translate the UCT computer code into RR card code, the only code acceptable to the output devices. In the instruction associated with this translation, the information to be translated is stored in register A. Function signal 18 alerts the translator gates to the S lines, which contain the contents of register A. Since the translation is from four-bit code to six-bit code and register A can hold only four bits, the contents of rA on the S lines also goes to register X where the two most significant bits of the code are produced.

In UCT code, a 4 is represented by 0100 with a 1 in the A3 position of register A. After translation, a 4 in RR code is represented by two punches—one in the 3 row and one in the 9 row. Therefore, a 4 after translation would show a 1 bit in A3 (register A) and a 1 bit in X2 (register X): 0010 (rX) 0100 (rA) = 4.

Table 3-2 shows the UCT-RR translator gates, the four-bit code signals received from the S lines, and the translated six-bit card code. The second column shows the contents of register A in UCT code. The next two columns show the translate gates of register A and register X. The inputs and outputs of each gate are shown, together with the number of the gate in parenthesis. The fourth and fifth columns show the results of the translation in register X and register A and the last column shows the representation of numbers 0 through 9 in RR card punches. Note in column three that two gates, 6 and 7, are required to translate an 8 from UCT code into RR code. **(See section 5-11.)**

3-25. CIRCULAR SHIFT GATES. These gates function on right circular shift and divide instructions to permit the shifted outputs of register X to be transferred into register A. The gates, alerted by function signal 22, are permissive to the X'1 through X'4 early outputs of register X.

3-26. SUM INPUT BUFFERS. During the arithmetic instructions, the sum of any addition is present on the 0 lines from the binary and quinary adders (sections 3-53 and 3-65). In these instructions, the sum of additions is transferred from the quinary and binary adder gates to the sum input buffers of register A.

3-27. OUTPUT DISPLAY GATES. Use of the REGISTER SELECTOR on the operator's control panel enables the operator to type into or view the contents of a register. If the operator selects register A by depressing the REGISTER SELECTOR button A, the RSA control signal is generated. This signal makes the four output display gates of register A permissive to the contents of the four subregisters. The resulting A1-$\overline{0}$D, A2-$\overline{0}$D, A3-$\overline{0}$D and A4-$\overline{0}$D signals are sent to buffers shown on the register C drawing, A1 (section 3-11). From register C, the contents of register A go to the control panel display circuits.

3-28. OUTPUT CIRCUITS. Four cutputs of the register A are common to all four subregisters. All four outputs normally read out of the register to various circuits. Whether these signals are used at their destinations depends on the presence of controlling signals. For example, A1M through A4M outputs always read out of the register A to the M buffer input gates. If the gates are permissive to the signals, the contents of the register are allowed to enter the M buffers and the M lines. If the recirculation gates of the register A are blocked, however, the A1M through A4M signals continue to go to the M buffer input gates but are blocked from entering the M buffers. The A1 through A4 output signals go to the recirculation gates (section 3-21). The A'1 through A'4 signals go to the right shift gates of the register A and the register X. The A11, A21, A31, A41 outputs normally go to the S buffers and onto the S lines. However, during a number of instructions, function signal 58+ is high. This signal blocks the outputs to the S buffers so that the buffers can be used for other purposes. The A"4 and $\overline{A"4}$ output signals are generated only by the fourth bit subregister. One of these signals goes to the left shift gates during a left shift instruction (section 3-16).

3-29. REGISTER X

The register X (figure A9) also stores the ten decimal digits of a computer word in four 12-bit subregisters. The 13 gates described in the following sections control input to and output from register X.

3-30. INPUT GATES. The input gates of the register X receive the outputs of the M buffers, when alerted by function signal 76. In both instructions involving the input gates, the contents of a storage location are on the M lines and enter register X through the input gates.

During the PRY step of the print instruction, FS 42+ blocks input gates 19C and 19D to place 0 bits in subregisters X3 and X4. At the same time, FS 76 makes gates 19A and 19B permissive to the primed part of the print word from storage.

3-31. RIGHT SHIFT GATES. The right shift gates of register X operate in the same manner as the right shift gates of register A (section 3-17). During either a right shift instruction or a right shift in multiplication, the outputs of register X (X'1 through X'4) are returned to register X one pulse time earlier than in normal recirculation. Function signal 59 alerts the gates to the early output.

3-32. ZERO SUPPRESS GATE. During a zero suppress instruction, this gate complements the $\overline{S1}$ bits of the digits being transferred from the S buffers to register A and places the complemented bit in subregister X3. Function signal 36 alerts the gate during the first step of the zero suppress instruction. The $\overline{S1}$ signal, when low, indicates a zero in the least-significant bit (LSB) position of the card code digit. Examination of the RR card code shows that the only digit having a one in the LSB position is a decimal zero (00 0001). Wherever a zero is present in the LSB position, the digit entering register A is a non-zero digit. In the zero suppress instruction, a 1 bit is placed into register X whenever a non-zero digit is present in register A. The $\overline{S1}$ bit indicates a non-zero character; therefore the low $\overline{S1}$ signal is complemented to a high signal. The high signal produces a one in the proper position of subregister X3.

3-33. COMMA SUPPRESS GATES. The comma suppress gates operate in conjunction with the zero suppress gate during a zero suppress instruction to replace commas with non-punching zeroes. The card code combination for a comma is 00 0011. Gates 25D and C sample the two highest order bits of the unprimed part of the word from rA. Gates 25A and B sample the two bits of the primed portion of the word from the X1 and X2 subregisters of rX. If the X1, X2, S3 and S4 inputs are high, indicating zeroes and the zero suppress gate is blocked by a high $\overline{S1}$ signal, a comma is present and a 0 bit is placed in the X3 subregister. This 0 bit will indicate the presence of a punching zero and commas in the second step of the zero suppress instruction. Examination of the six bit card code shows that the only combinations which contain 1's in the LSB position and 0's in the four highest order bits are a zero, 00 0001, and a comma, 00 0011. It is unnecessary to test the second lowest order bit (S2).

3-34. RECIRCULATION GATES. The recirculating signals of the four subregisters of register X are X1, X2, X3 and X4. These signals are the outputs of the last amplifier of the subregisters and they reenter register X at the recirculation gates. The recirculation gates are normally permissive to the recirculating signals. During a number of instructions, however, function signal 56+ blocks the path of recirculation, clearing the register. During the second step of a zero suppress instruction, function signal 37+ blocks recirculation of the X3 bit to clear subregister X3 of the 1 bits which were inserted during the first step.

Table 3-1. Translating from Remington Rand to UCT Code

Decimal Digit	RR Code M (rX)	RR Code S (rA)	Row Positions	Translator Gates of rA*	UCT Code (rA)
0	0000	0001	0		0000 = 0
1	0000	0010	1	(24) $\overline{M2}$ S2 ⟶ A1	0001 = 1
2	0010	0010	1,9	(23) M2 S2 ⟶ A2	0010 = 2
3	0000	0100	3	(22) $\overline{M2}$ S3 ⟶ A1 A2	0011 = 3
4	0010	0100	3,9	(17) M2 S3 ⟶ A3	0100 = 4
5	0000	1000	5	(20) S4 ⟶ A4	1000 = 5
6	0010	1000	5,9	(19) M2 S4 ⟶ A1 (20) S4 ⟶ A4	1001 = 6
7	0001	0000	7	(18) M1 ⟶ A2 A4	1010 = 7
8	0011	0000	7,9	(21) M1 M2 ⟶ A1 (18) M1 ⟶ A2 A4	1011 = 8
9	0010	0000	9	(16) $\overline{S2}$ $\overline{S3}$ $\overline{S4}$ $\overline{M1}$ M2 ⟶ A3 A4	1100 = 9

*Gate numbers appear in parentheses

Table 3-2. Translating from UCT to Remington Rand Code*

Decimal Digit	UCT Code (rA)	Translator Gates of rA	Translator Gates of rX	RR Code (rX)	RR Code (rA)	Row Positions
0	0000	(5) $\overline{S1}$ $\overline{S2}$ $\overline{S3}$ $\overline{S4}$ ⟶ A1		0000	0001	(0) = 0
1	0001	(6) S1 $\overline{S2}$ $\overline{S4}$ ⟶ A2		0000	0010	(1) = 1
2	0010	(7) $\overline{S1}$ S2 $\overline{S4}$ ⟶ A2, X2		0010	0010	(1,9) = 2
3	0011	(3) S1 S2 $\overline{S4}$ ⟶ A3		0000	0100	(3) = 3
4	0100	(4) S3 $\overline{S4}$ ⟶ A3	(5) S3 ⟶ X2	0010	0100	(3,9) = 4
5	1000	(8) $\overline{S2}$ $\overline{S3}$ S4 ⟶ A4		0000	1000	(5) = 5
6	1001	(8) $\overline{S2}$ $\overline{S3}$ S4 ⟶ A4	(6) S4 S1 ⟶ X2	0010	1000	(5,9) = 6
7	1010		(7) S2 S4 ⟶ X1	0001	0000	(7) = 7
8	1011		(6) S4 S1 ⟶ X2 (7) S2 S4 ⟶ X1	0011	0000	(7,9) = 8
9	1100		(5) S3 ⟶ X2	0010	0000	(9) = 9

*Gate numbers appear in parentheses

3-35. QUOTIENT-COMPLEMENTING GATES. When alerted by an OR control signal, the quotient-complementing gates complement the division sentinel and quotient digits in the divide instruction. The Q1 through Q4 and $\overline{Q1}$ through $\overline{Q4}$ signals represent the quotient digits which are computed in the multiplier/quotient counter (sections 3-74 and 4-35,1).

3-36. DIVISION SENTINEL GATE. In the first step of the divide instruction, function signal 15 alerts the division sentinel gate, which jams a one into subregister X1 of register X. This places the division sentinel combination, 0001, into the least significant digit position of register X. Later, this sentinel will signal the end of division. (See section 4-34.)

3-37. REMAINDER INPUT GATES. In the third step of the divide instruction (D3), the final quotient in register A and the final remainder in register X must be interchanged. The contents of register A normally read onto the S lines. Function signal 32 alerts the remainder input gates. The remainder, which was stored in register A is transferred on the S lines to register X. (See section 4-36.)

3-38. UCT TO RR TRANSLATOR GATES. The translator gates of register X operate in conjunction with the UCT to RR translator gates of register A (table 3-2). The translate gates of register A convert the four bits of UCT code into the four lowest-order bits of the six-bit card-code. The translate gates of register X translate the four bits of UCT code into the two highest-order bits of the card-code. Function signal 18 alerts the gates to the S lines, which carry the four-bit code to be converted.

3-39. CHECK-BIT STORAGE GATE. In the print instruction, the six bits of a digit are transferred from main storage, through registers A and X, to the print buffer band. Four of the six bits are sent through register A, two through register X. The check bit for the unprimed four bits sent through register A is stored in subregister X4 of register X. Function signal 43 alerts the check-bit storage gate to the DM5 check-bit signal.

3-40. CHECK-BIT COMPUTER GATES. The check-bit computer gates also operate during the print instruction to sample the primed part of the digit coming from storage on the M1 and M2 lines and the check bit of the unprimed part of the digit already stored in rX, indicated by the X4 signal. The gates, alerted by FS 65, compute a single check bit for the two parts of the digit, primed and unprimed. If any one of these four gates operates, a 1 bit is stored in the fourth subregister of rX because the digit contains an even combination of 1 bits and requires a 1 bit to make it odd. If none of the gates operates, a 0 bit is computed and stored because the digit contains the necessary odd combination of 1 bits.

3-41. CIRCULAR SHIFT GATES. During either a right shift or a divide instruction, a circular shift takes place between registers A and X. The output of register A goes to register X through the circular shift gates of register X and the output of register X goes to register A through the circular shift gates of register A. Function signal 59 alerts the gates to the A'1 through A'4 outputs of register A.

3-42. OUTPUT DISPLAY GATES. The output display gates of register X function in the same way as those of register A (section 3-27). When the operator selects register X by depressing the REGISTER SELECTOR button X, the RSX control signal is generated. This signal makes the output display gates permissive to the contents of register X. The outputs of the four gates, signals X1 $\underline{OD}$, X2 $\underline{OD}$, X3 $\underline{OD}$, and X4 $\underline{OD}$, go to the register display circuit shown on register C (section 3-11). From register C, the contents of register X go to the control panel display circuits.

3-43. OUTPUT CIRCUITS. Four outputs of register X are common to the four subregisters. Signals X1M thru X4M go to the M buffers (figure A6). Signals X'1 through X'4 go to the right shift gates of registers A and X, and also to the M buffers. The recirculating signals X1 through X4, in addition to returning to the recirculation gates of register X go to the multiplier quotient counter (figure A14)

during the multiply and divide instructions. These signals go to the input gates of the MQC flip-flops. In division the MQC provides a one-pulse delay for shifting left the contents of register X. In multiplication, the MQC stores the digits of the multiplier (sections 4-35,1; 4-30,1). Z1 through Z10 outputs of subregister X3 are used in the zero suppress instruction and go to the zero suppress gate of register A.

In the print operation, subregister X4 contains the check bit for the part of a digit contained in register A. The $\overline{X4}$ and X4 outputs of subregister X4 are sampled by the check bit computer gates in the computing of a new check bit. In operations other than printing, X4 is also a normal recirculating signal. Another output of subregister X4 is the $\overline{X4D}$ signal, which goes to the LSD complementer gate of register A, during a divide instruction.

3-44. REGISTER L

Each of the four subregisters of register L (figure A10) has three input gates and two output gates. The five gates controlling input to and output from register L are described in this section.

3-45. RECIRCULATION GATES. The upper gate of each subregister in figure A10 is the recirculation gate. Information normally recirculates from the output of the subregister into the recirculation gates. During most instructions function signal 57+ is low, making the gate permissive to the recirculating signals. During the storage-to-register L and register A-to-register L transfer instructions, however, function signal 57+ goes high, blocking the gate. This clears the register because there is no path for normal readout of the contents of the register during these instructions. The subregisters of register L are cleared so that new information can enter through either the M or S input gates.

3-46. M GATES. The outputs of the M buffers (section 3-52) on the M lines enter the M input gates during the storage-to-register L transfer instruction. The M gates are shown as the center gate of each subregister in figure A10. Function signal 8 makes the M gates permissive to information on the M lines (M1 to M4). At the end of the instruction, blocking signal 57+ is removed from the recirculation gates and the information begins to recirculate.

3-47. S GATES. The outputs of the S buffers (section 3-51) on the S lines enter the S input gates during the register A-to-register L transfer instruction. The S gates are shown as the lower gate of each subregister in figure A10. Function signal 16 alerts the S gates to information on the S lines (S1 to S4). At the end of the instruction, the recirculation path is opened as the blocking signal goes low, and the information begins to recirculate.

3-48. OUTPUT DISPLAY GATES. When the operator depresses the REGISTER SELECTOR for register L, the control signal RSL is generated. This signal makes the output display gates of register L permissive to the contents of the register. Output signals L1 $\underline{O}$D, L2 $\underline{O}$D, L3 $\underline{O}$D and L4 $\underline{O}$D go to the output display circuit shown on register C, which controls the control panel display circuit.

3-49. OUTPUT GATES. The output gates are permissive to the contents of register L on the multiply, divide, and comparison instructions. Alerted by function signal 66 on these instructions, the output of the gates are the L1 through L4 signals. These four signals, which represent the contents of the four subregisters of register L, go to the M buffer.

In the second step of division, control signal OR+ is high, blocking the output gates even though function signal 66 has alerted them. As soon as signal OR+ goes low, the gates again are permissive to the contents of the register.

3-50. OUTPUTS. The signals L1M and L4M are normal outputs of the register to the M buffers. The M buffers, however, are permissive to these signals only during a register L-to-storage transfer instruction. At all other times, the input gates of the M buffers are not permissive to the signals from register L.

3-51. S BUFFERS

The S buffers (figure A9) transfer the outputs of registers A and C to various circuits throughout the central processor. The output signals of the two registers are ungated inputs to the buffers. The outputs of the buffers are the S1 through S4 and $\overline{S1}$ through $\overline{S4}$ signals, which are frequently referred to as the S lines. The S1 through S4 unbarred outputs are forced low during the divide, storage-to-register A transfer, print, and superimpose instructions, by high function signal 82A. Of these instructions, only the unbarred (non-complemented) outputs are used so that when 82A is high, the S lines are low. This enables the M lines, which are not forced low, to enter the input gates of register A.

3-52. M BUFFERS

The M buffers (figure A6) normally transfer the contents of register L and the storage drum to other central processor circuits. The signals from register L, L1 through L4, and the DM memory outputs are ungated inputs to the buffers. Therefore, they are transferred to the M lines whenever they are present at the M buffer. All other inputs to the M buffers are from the input gates, which are permissive during the instructions listed for each gate in figure A6. A permissive gate allows information signals from various computer elements to enter the M buffers and the M lines. During the input-output test instruction, function signals 27 and 27A are high inputs to the buffers. They force the unbarred M outputs low so that the S lines can read into the input gates of register A.

3-53. COMPARATOR

The circuits of the comparator (figure A12) perform four major functions: comparison, addition of binary bits, determination of carry, and control. The comparator performs these functions in the arithmetic and comparison instructions and in the search for instructions or operands in the memory. Because certain components of the comparator operate differently for each of the four functions, the description of each component includes separate treatment for each of its functions. (In the computer code, the three lowest order bits of a digit are the quinary bits. The most significant is the binary bit. References made in this section to quinary and binary bits pertain to this order of significance.)

3-54. QUINARY EQUALITY CIRCUIT. In the search for either an instruction or an operand from storage, the code combinations for the many addresses on the storage drum are transferred serially to the M buffer and the M lines. The address of the instruction or operand being searched for is stored in register C and also reads into the S buffers and the S lines. The quinary equality circuit compares the quinary bits of the addresses on the M lines with the quinary bits of the address on the S lines. When the circuit finds equality between the two lowest order digits of the two addresses, and the correct band is chosen (section 3-97), the desired storage address has been located and the instruction or operand contained in that location can be read out. The input gates of the circuit are controlled by the A, C and CP control signals, which are generated during any function involving the quinary equality circuit, to make the gates permissive. When all of the M and S

inputs to a quinary equality gate are low, a condition which can occur only when the inputs are equal, a high K signal is generated. The K signal generates low signal EQ and high signal $\overline{EQ}$, both of which indicate equality of the input quinary bits. The $\overline{EQ}$ signal controls the time selection (TS) flip-flop. The EQ signal controls the conditional transfer (CT) flip-flop.

In the conditional transfer instruction (87), the contents of register L and register A are present at the M and S inputs, respectively. Information in the two registers is compared in the comparator to determine whether the contents of register A is greater than the contents of register L. The presence of low signals A and C at the input gates indicates that the contents of register A is not greater than the contents of register L. Control signals A, C and CP alert the quinary equality input gates to the M and S inputs. Once again, equality at any one of the gates produces a high K signal, which in turn produces high $\overline{C}$ and low C signals. The $\overline{C}$ and C signals control gates 13 and 14 of the CT flip-flop.

In the Q conditional transfer instruction, the gates test for equality in the same manner as the T instruction. However, the A, C, and CP signals act only as alerting signals in the Q instruction.

During the subtraction process, the quinary equality gates compare the minuend and subtrahend. If the two are equal, the result of the subtraction, zero, must be given a plus sign (section 3-67). The CP signal, which indicates that subtraction is taking place, and the A and C signals, alert the gates to the M and S inputs. Equality produces the K signal and also the high $\overline{EQ}$ signal which keeps the TS flip-flop from being restored. If the inputs to the gates are not equal, the $\overline{EQ}$ signal becomes a low signal which restores the TS flip-flop.

3-55. QUINARY CARRY CIRCUIT. The quinary carry circuit consists of all of the comparator gates that generate R signals and the three output circuits which generate C, $\overline{C}$, and C'.

The quinary carry gates alerted by the $\overline{CP}$ signal from the complement (CP) flip-flop (section 3-63) are used during the four arithmetic instructions. In the addition process for any of these instructions, the quinary bits of the two digits being added go to the quinary carry gates. When the addition of quinary bits results in a carry, the indication of carry is sent to the binary addition circuits, to be introduced into the addition of the binary bits. Similarly,

decimal carry from a previous addition is indicated to the quinary carry gates by the presence of both the A and C signals. In the arithmetic instructions, the operand from memory is on the M lines, and the contents of register A on the S lines. The quinary carry gates alerted by the CP signal sample specific bits of the two digits being added. For instance, gate 45 samples the M3 and S1 bits. If both bits are 1's, the quinary combination of the two digits is 1XX XX1. A 1 in the M3 bit position indicates that one of the digits being added is a 4 or greater. A 1 in the S1 bit position indicates that the other digit is a one or greater. In adding the digits 1 and 4, a carry to the binary bits occurs. Gate 45, then, generates a high R signal, which in turn generates low signals C and C' and high signal $\overline{C}$. The C' and $\overline{C}$ signals go to the binary adder; the $\overline{C}$ signal, together with the C signal, also goes to the decimal carry adder.

During a subtraction process (addition with unlike signs or subtraction with like signs) the group of quinary carry gates alerted by the CP signal is used to sample for quinary carry. In the subtraction process, the contents of register A on the S lines are complemented in the complementer gates of the quinary adder (section 3-65). In parallel, the S lines and the M lines go to the quinary carry gates. One of the gates alerted by the CP signal generates a K signal when the combination of M and S inputs is low. Control signal CP indicates that the S line inputs are presently being complemented (nine's complement). The quinary carry gates for subtraction differ from those for addition in that the nine's complement of the S inputs to these gates must be added to the M inputs to determine quinary carry. To illustrate this, the combination at gate 46 is: M = 001X, S = X00X. Referring to the computer code, the digit on the S lines can be any digit with zero in the S2 and S3 bit position. Four possibilities exist for this combination: 0, 1, 5, and 6. Because the S bits are being complemented in the quinary adder, the same S bits at the quinary carry gates represent the complemented version of the S digit. The nine's complement of 0, 1, 5 and 6 are: 9, 8, 4 and 3 respectively. Following are additions of the quinary bits of the four possible S combinations, after complementing, to the quinary bits of the M combination, at gate 46:

M: X/01X = (2)	M: X/01X = (2)	M: X/01X = (2)	M: X/01X = (2)
S: 1/100 = (4)	S: 1/011 = (3)	S: 0/011 = (3)	S: 0/100 = (4)
sum 6	sum 5	sum 5	sum 6

The digit on the M lines is described above as a 2, because, with a 1 in the M2 bit position, the digit can be no less than a 2. If the addition of 2 to the S digit requires a quinary carry, it follows that any digit larger than 2 also requires a quinary carry. The first quinary addition is of the S combination for 9 (the nine's complement of 0) to the M bits. Only the quinary bits of the digit are sampled; therefore in quinary code a 2 is added to a 4. The sum is 6 and, because any digit larger than 4 necessitates a quinary carry to the binary addition, a quinary carry is indicated. This holds true for the other three possible S combinations, all of which result in a quinary digit larger than 4. Any such combination present at the quinary carry gates during subtraction causes a C signal to be generated. The number in parentheses in each addition is the digit formed by the quinary bits.

Gate 51 of the quinary carry circuit is the only one that operates on both the addition and subtraction processes. This gate is permissive to a combination of M and S inputs, common to both addition and subtraction. In either process, the presence of this combination generates an R signal.

The group of quinary carry gates, which are alerted by the CP signal, is used also during the T comparison instruction to compare the quantities in registers A and L. If the contents of register L, on the M lines, is greater than the contents of register A, on the S lines, a high R signal is generated. The R signal generates low C and high $\overline{C}$ signals to control the CT flip-flop. Some of the comparisons made by these gates are of non-numeric combinations (denoted by the alpha symbol). The combinations 0101, 0110, and 0111 are less than zero; the combinations 1101, 1110, and 1111 are greater than nine. Non-numeric symbols in card code also can be compared during the T instruction by these gates. Sections 1-14 and 1-15 explain computer and card codes.

3-56. FORCE DECIMAL-CARRY GATES. The comparator gates labeled force decimal carry generate the two indications of decimal carry, A and C, when the proper controlling signals are applied.

On the T comparison instruction, function signal 20 alerts gate 32 to the A+ signal. The A+ signal comes from the register A sign flip-flop (section 3-66) and indicates that the sign of the contents of register A is a plus. If the A+ signal is low it becomes a high signal output of the amplifier and is sent to the binary carry and quinary carry circuits to generate the A and C signals. In this instruction, the A and C signals are used to alert the quinary equality circuit. If the A+ signal is high, the A and C signals are not generated and the quinary equality circuit is blocked.

Gate 31 also operates during the T instruction to compare the binary bits of information from registers L and A. If the $\overline{S4}$ bit from register A and the M4 bit from register L are present the digit in register L is greater than the digit in register A. The A and C signals are generated by the gate to control the CT flip-flop (section 3-61). The CP signal, present during this instruction, alerts the gate.

Gates 30 and 31 of the force decimal-carry circuit operate during the arithmetic instructions. They generate the A and C signals to indicate decimal carry regardless of whether the quinary-carry signal, C, is present. In adding certain digits, addition of the quinary bits generates no quinary carry (C) to the binary adder. However, in many such additions, a decimal carry to the next digit is necessary. To ensure that the A and C signals are present at the decimal-carry adder (section 3-64), the force decimal-carry gates generate both A and C to add a carry of one, whenever the binary bits show a decimal carry. When both the M4 and S4 bits are 1's, as when either gate is permissive, a decimal carry is generated. The CP and $\overline{CP}$ control signals alert the gates. The $\overline{CP}$ signal indicates that the $\overline{S4}$ bit is being complemented in the quinary-adder complementer gates and will therefore become a 1 bit. The same two gates also operate as part of the binary equality gates during the search operation.

3-57. BINARY EQUALITY GATES. The binary equality gates compare the binary bits of digits on the M and S lines during search and various other instructions.

In the search for either an instruction or an operand, the code combinations for the storage addresses are on the M lines. The address of the instruction or operand being searched for is stored in register C and is present on the S lines. While the quinary equality gates are comparing the quinary bits of each address digit, the binary equality gates are comparing the binary bits of the same digit. Only the gates alerted by the CP signal operate during search operations. If the M4 and S4 bits are equal (M4 and S4 or $\overline{M4}$ and $\overline{S4}$), the binary-carry circuit generates signals which control the memory selection circuits (figure A18), and the TS flip-flop (section 3-62).

The binary equality gates alerted by the CP signal are used during both the Q and T comparison instructions to sample for equality of digits being compared on the M and S lines. If the bits are equal, the binary carry circuit generates signals which control the CT flip-flop.

Any of the binary equality gates, and gates 30 and 31, can operate during the arithmetic instructions. If a subtraction process is involved, those gates alerted by the CP signal operate. If an addition process is involved, those gates alerted by the $\overline{CP}$ signal operate. In the subtraction process (CP present), the binary equality gates send a high signal to the binary carry and adder circuits to produce a 1 whenever the input bits are alike. When the input bits are unlike, a low signal is sent to the carry circuit and the adder to produce a 0. In the addition process ($\overline{CP}$ present), the binary equality gates send a high signal to the carry circuit and adder to produce a 1 when the input bits are unlike. Whenever the input bits are alike the equality gates send a low signal to the carry and adder circuits to produce a 0.

3-58. INITIAL FORCE DECIMAL-CARRY CIRCUIT. This circuit operates during the search, add, subtract, or Q comparison instructions. The CP flip-flop generates one of the following high signals: CP1, CP2, CP3, CP4 and CP5. These high signals go to the initial force decimal-carry buffer to force the outputs of the binary and quinary carry circuits to A and C, respectively. The A and C signals are generated initially in the instructions and search to alert various comparison gates.

3-59. BINARY-CARRY CIRCUIT. The binary-carry circuit converts inputs from the initial force decimal-carry, force decimal carry, and binary equality circuits into the A', $\overline{A'}$, A and $\overline{A}$ binary carry signals. The latter three signals control the memory selection circuits (figure A18) and the CT flip-flop of the comparator. The A and $\overline{A}$ signals, which indicate the presence or absence of binary carry, go to the decimal-carry adder, (section 3-64). The A' and $\overline{A'}$ signals go to the binary adder and indicate binary carry or the value of the binary bit. The signal flow chart accompanying figure A12 illustrates other uses of the binary-carry outputs.

3-60. BINARY ADDER GATES. The binary adder gates are alerted by function signal 50 during all of the arithmetic instructions. The adder adds the outputs of the quinary and binary carry circuits and sends the sum to register A. The output 0 signal is the binary or fourth bit of the sum. The quinary bits of the sum are present on the 0 output lines of the quinary adder.

3-61. CONDITIONAL TRANSFER FLIP-FLOP. The conditional transfer flip-flop (CT FF) is used primarily during the search step and the Q and T comparison instructions to determine whether the computer takes the next instruction from the m address or the c address.

In the Q instruction, the m address is chosen if the two words from registers A and L are equal; if they are unequal, the c address is chosen. In the T instruction, the m address is chosen if the contents of register A are greater than the contents of register L; if not, the c address is chosen. The CT signal controls readout of the m address from register C; the $\overline{CT}$ signal controls readout of the c address from register C.

In the staticize step of any instruction, set gate 12 of the CT FF samples the $\overline{STR2}$ signal, which indicates whether the instruction involves a search for the m address. If the $\overline{STR2}$ signal is low, indicating a zero in the STR2 bit position, the CT FF is set and the CT signal is generated to control readout of the m address. If the $\overline{STR2}$ signal is high, indicating a 1 in the STR2 bit position, the flip-flop is restored, generating the $\overline{CT}$ signal to control readout of the c address. Function signal 2 makes the gate permissive to the $\overline{STR2}$ signal.

At the beginning of the execution step of the Q and T instructions, FS 60A makes gate 1 permissive, setting the flip-flop to CT. When the CP signal is generated, the m address will be read unless comparison operations restore the flip-flop to $\overline{CT}$ thereby choosing the c address.

During the second stages of any of the three input-output test instructions, FS 27 alerts set gate 11 of the flip-flop. If the Jam I2B input signal is high, indicating that an abnormal condition is present in one of the input-output units, the flip-flop is restored to $\overline{CT}$, causing the program to go to the c address for the next instruction. If the input-output units are operating normally, the Jam I2B signal is low. The low signal sets the flip-flop to generate CT and read out the m address.

During the T instruction, gates 13, 14, and 15 control the restore circuit of the CT FF. Function signal 20 alerts all three gates which sample the sign of the contents of registers L and A (signals A- and L+) and the outputs of the binary and quinary carry circuits (signals A, C, $\overline{A}$ and $\overline{C}$). The A and C signals on gate 13 indicate that the A+ signal is present at the force decimal-carry gate, 32. Table 3-3 lists the gates (figure A12) which operate to restore the CT FF to $\overline{CT}$ under the various conditions in the T instruction. The conditions, or signals, in the first column of table 3-3 are the sign combinations possible for the contents of registers A and L. The conditions listed at the top of the table are the absolute values of the contents of both registers, as determined by the comparison circuits. The CT FF remains set to generate CT under those conditions marked by X in the table.

Table 3-3. Conditional Transfer Flip-Flop Gate Inputs

	A > L	A = L	A < L
A+ L+	X	Gate 13	Gate 13
A+ L-	X	X	X
A- L+	Gates 14 15	Gates 14 15	Gate 13
A- L-	Gates 14 15	Gates 14 15	X

In the Q comparison instruction, gates 16 and 17 control the restore circuit of the CT FF. Function signal 75 alerts the gates which sample the indications of equality between the contents of registers A and L. If either the $\overline{EQ}$ or $\overline{A'}$ signal is low, one of the gates sends a high signal to buffers 77 and 78 to restore the flip-flop.

The $\overline{EQ}$ signal, when low, indicates inequality of the quinary bits of the two registers. The $\overline{A'}$ signal indicates inequality of the binary bits of the two registers. If the contents of the registers are equal, the $\overline{EQ}$ and $\overline{A'}$ signals are high. The high signals block gates 16 and 17 and the CT FF remains in the set condition.

During the Q instruction, gates 18 and 19 sample the signs of registers A and L which are stored in the sign and control circuits. If the signs are unequal, A+ and L-, or A- and L+, one of the gates is permissive. The permissive gate sends a high signal to buffer 77, restoring the flip-flop. If the signs are equal, one of the inputs to both gates is high. The high signals block both gates and the flip-flop remains in the set condition. Function signal 75 alerts the gates to the sign signals.

The CT FF is also controlled by the NEXT ADDRESS switch on the operator's control panel. The result of any comparisons made during the Q or T instructions is indicated by the m address and the c address lights on the control panel. If the CT FF has been set, the m lamp is lit; if it is restored, the c lamp is lit. The NEXT ADDRESS switch enables the operator to override the results of the instructions. If the m switch is energized, a high signal goes to buffer 76, which sets the flip-flop and generates CT. If the c switch is energized, a high signal goes to buffer 77, which restores the flip-flop and generates $\overline{CT}$.

3-62. TIME SELECTION FLIP-FLOP. The time selection flip-flop (TS FF) is used in controlling memory search operations, and during the add and subtract instructions to control the sign of the sum.

In the search for a storage location, the two lowest-order digits of the instruction address, p1 and p2, or operand address, p5 and p6, and the least significant bit of the third digit, p3 or p7, are compared to address digits from the storage circuits in the comparator equality circuits. The TS FF is initially set to TS, at buffer 82, before search operations begin. The flip-flop in the set condition indicates equality of the address digits being compared. Inequality of the digits restores the flip-flop. Function signal 1 alerts the flip-flop input gates 20 and 21 during search. These gates sample the $\overline{EQ}$ and $\overline{A'}$ outputs of the quinary and binary comparison circuits. If both inputs are high, indicating equality, the gates are blocked and the TS FF remains set. If either of the signals goes low, indicating inequality of the digits being compared, the flip-flop is restored and a new search operation begins (section 4-3). Gate 22 operates to restore the TS FF under certain conditions of the search operations (section 4-5).

The CT FF restore gates 16 and 17 also control the TS FF during the subtraction process. When two quantities involved in the subtraction process are equal, the sign of the zero result must be plus. As in the Q instruction, gates 16 and 17 are alerted by FS 75 to sample for equality of digits being compared in the binary and quinary equality circuits. If equality exists between the two, the gates are blocked and the TS FF remains set. The TS output of the flip-flop goes to the register A sign flip-flop to force the sign of the sum to plus (section 3-67). Outputs of the TS FF also go to the memory selection circuits, the static register, and the read-write circuits.

3-63. COMPLEMENTER

The complementer circuit (figure A11) operates during the arithmetic instructions to complement, if necessary, the quinary bits of information on the S lines. In the subtraction process, the minuend on the S lines must be complemented. Under such conditions the complement flip-flop (CP FF) is set, generating the CP control signal. With CP present, the complementer gates generate the quinary bits of the nine's complement of the input S bits. For example, if the quinary bits of the digit one (001) are to be complemented, the input to the complementer circuit is: $\overline{S3}$, $\overline{S2}$, S1, and CP. Gate 1 is permissive to the low S1 signal, generating low S1C.

Gate 2 is blocked by the high $\overline{CP}$ signal, and gate 4 is blocked by the high $\overline{S1}$ signal. Gate 3, however, is permissive to $\overline{S2}$, S1, and CP, generating low S2C. Gate 5 is blocked by the high $\overline{CP}$ signal and gate 6 is blocked by the $\overline{S1}$ signal. Because both gates 5 and 6 are blocked, the $\overline{S3C}$ signal is low. The outputs of the complementer, then, are $\overline{S3C}$, S2C, and S1C, or the combination 011. This is the quinary combination for either a 3 or an 8. The binary circuits determine the binary bit of the combination, which in this case is a 1. Because the nine's complement of 1 is 8, the complementer and binary adder circuits produce the biquinary code combination for 8, which is 1011. Section 3-60 gives details of the function of the binary adder circuits.

In an addition, complementing is unnecessary; therefore the $\overline{CP}$ signal alerts the complementer gates so that the input bits pass unchanged through the circuit. The outputs of the complementer circuit are low signals and are applied to the quinary adder gates, (section 3-65).

3-64. DECIMAL-CARRY ADDER

The decimal-carry adder (figure A11) operates during either or both steps of any subtraction process to add a 1 to the subtrahend on the M lines. The design of the computer calls for the use of the nine's complement in arithmetic operations. However, when a subtrahend is to be added to a minuend, adding the nine's complement of the minuend to the subtrahend does not produce a correct difference. Adding the ten's complement of the minuend to the subtrahend does produce the correct difference. The unit adder simulates the use of the ten's complement by adding a one to the subtrahend. This has the same effect as adding the ten's complement of the minuend to the subtrahend.

The A and C signals from the comparator add a one to the subtrahend on the M lines. During a subtraction process, the CP signal is generated by the complement flip-flop in the set condition and causes the initial force decimal-carry circuit to generate signals A and C. These signals alert the decimal-carry adder gates to the subtrahend bits on the M lines. Each gate is permissive to a specific input combination. For example, if the quinary combination on the M lines is 010 (2), the inputs

are $\overline{M3}$, M2, $\overline{M1}$, A, and C. Gates 14, 15, and 16 are blocked to this combination, generating $\overline{M3U}$. Gate 13 is permissive to the $\overline{M1}$ and M2 signals, generating M2U. Gate 9 is also permissive, generating M1U. The output combination of the decimal-carry adder is: $\overline{M3U}$, M2U, M1U. This signifies the quinary combination of 011 (3). Thus the adder has added a 1 to a quinary 2 for a quinary sum of 3.

During an addition, the decimal-carry adder adds a decimal carry from a previous addition to the quantity on the M lines. At the beginning of the process, the CP FF is restored and the initial force decimal-carry circuit generates $\overline{A}$ and $\overline{C}$. However, if a decimal carry exists from a previous addition, the carry circuits override the $\overline{A}$ and $\overline{C}$ signals to produce the A and C signals which indicate decimal carry. The decimal-carry adder adds the decimal carry of 1 to information on the M lines. The outputs of the decimal-carry adder go to the quinary adder.

3-65. QUINARY ADDER

The quinary adder consists of 18 gates, arranged in a matrix in figure A11. The circuit adds the three quinary M bits from the decimal-carry adder to the three quinary S bits from the complementer. Function signal 50 alerts the gates, one or two of which can be permissive to a single combination of low inputs. The permissive gates generate high $\underline{0}$ signals; the blocked gates generate low $\underline{0}$ signals. A high output signal indicates a 1 bit; a low output signal indicates a 0 bit. The three major outputs of the quinary adder are $\underline{01}$, $\underline{02}$, and $\underline{03}$ signals. These form the quinary portion of the sum of addition and go to register A for storage.

3-66. SIGN AND CONTROL CIRCUIT

The sign and control circuit, figure A13, consists of three sign flip-flops, three control flip-flops, and a control circuit for display of the register signs on the operator's panel. The sign flip-flops compute and store the signs of the contents of register A, X, and L. The control flip-flops generate signals that control various operations in the computer.

3-67. REGISTER A SIGN FLIP-FLOP. The register A sign flip-flop computes and stores the sign of the contents of register A and the sign of the result in the arithmetic instructions.

Gates 1 and 2, alerted by FS 86 during multiplication and division, determine the sign of the product in multiplication and the sign of the quotient in division. The flip-flop is initially set to A- by FS 13A during multiply and FS 15A during divide. Gates 1 and 2 sample the signs of registers X and L from the sign flip-flops of these registers. If the signs are alike, one of the gates is permissive and the flip-flop is restored to A+. If the signs are unlike, both gates are blocked and the flip-flop remains in the set condition, generating A-.

Gate 3 is alerted by FS 4 during either the add or subtract instruction to compute the sign of the sum or difference. The presence of the A and C inputs to the gate indicates that the quantity in register A is equal to the word from storage. The CP signal indicates that a subtraction process is taking place. The A- signal is the output of the register A sign flip-flop prior to sign computation. If gate 3 is permissive to these signals, the flip-flop is restored to A+; if not, the flip-flop remains in the set condition and stores the A- signal.

Gate 7 receives the same inputs as gate 3 except that it is permissive when the sign of the word in register A is positive, and is equal to the word from memory. When the gate is made permissive, it sets the flip-flop and stores a minus sign, A-.

Gate 6 is alerted by FS 4, during the subtraction process, to force the flip-flop to A+ if the quantities being subtracted are equal. The TS signal indicates equality of the first nine digits of the two quantities; the EQ and A' signals indicate equality of the tenth digits of the two quantities. If both quantities are equal, the gate is permissive and the flip-flop is restored to A+. This ensures that a zero result always has a plus sign.

In a transfer of information from memory to register A (B instruction), the sign of the information being transferred is received by gate 4.

The flip-flop is initially set to A- by FS 6. The $\overline{M1}$ signal on the M lines represents the sign position of the word from storage. If $\overline{M1}$ is low, indicating a plus sign, the flip-flop is restored to A+; if $\overline{M1}$ is high, it blocks gate 4. Function signal 6, however, makes gate 5 permissive and the flip-flop remains in the set condition (A-).

3-68. REGISTER L SIGN FLIP-FLOP. The register L sign flip-flop stores the sign of the contents of register L during the two transfer instructions involving the register. In both instructions, the flip-flop is set initially to L+ by FS 8 and 16. If the input sign to the flip-flop is plus, the flip-flop remains set; if the input is minus, the flip-flop is restored to L-.

3-69. REGISTER X SIGN FLIP-FLOP. The register X sign flip-flop stores the sign of the contents of register X during the multiply and transfer instructions. In the divide instruction, the flip-flop stores the sign of the dividend. The dividend is stored in register A. In the multiply, divide, and Y transfer instructions, FS 78 sets the flip-flop to X+ and alerts gates 34 and 35 to the M1 signal.

At the beginning of the multiply and divide instructions, the sign of the multiplier or dividend is on the M lines (M1). In the Y instruction, the M1 bit indicates the sign of the word being transferred from storage. If the M1 signal is low, the flip-flop is restored to X- ; if M1 is high, the flip-flop is set to X+.

In the second step of the multiply instruction, FS 14-1A at gate 37 jams the flip-flop to X+. The IER signal from the IER-OR flip-flop (section 3-78) alerts gate 33 to the output of the rA sign FF, A-. The product of a multiplication is stored in both register A and register X. Therefore, the sign of rX must be identical to that of rA. If the sign of rA is minus, as indicated by the A- signal, the flip-flop is restored to X- ; if the sign of rA is plus, gate 33 is blocked and the flip-flop remains set.

3-70. SIGN DISPLAY CIRCUIT. The four REGISTER SELECTOR switches on the operator's control panel enable the operator to view the contents and the sign of any of the four circulating registers. The input gates of the register display circuit are alerted by the signals

generated by these selector switches, and cause the proper sign indicator lamp to be lit. For example, if the operator energizes the switch for rA, the RSA signal is generated. The signal alerts gate 101 of the sign display circuit. The gate samples the A- output of the rA sign flip-flop. If the sign of rA is minus, the A- signal is low and a high signal is sent to light the minus lamp on the control panel. If A- is high, indicating that the sign of rA is plus, the gate is blocked and a high signal is sent to light the plus lamp on the control panel.

3-71. COMPLEMENT FLIP-FLOP. Although the program specifies either an add or a subtract instruction, the complement flip-flop determines from the magnitudes and signs of the quantities involved whether an addition or subtraction is required. If a subtraction is required, one of the quantities involved must be complemented; therefore the CP control signal is generated to control the complementing and additions. If an addition is required, complementing is unnecessary; therefore the $\overline{CP}$ signal is generated to control circuits which perform the addition.

The add and subtract instructions are distinguished at the input of the CP FF by the STR4 output of the static register (section 3-3). The $\overline{STR4}$ signal, if low at gates 8 and 9, indicates that an add instruction is staticized in the static register. The STR4 signal, if low at gates 10 and 11, indicates that a subtract instruction is staticized in the static register. The four gates for add and subtract are alerted by FS 4.

When the $\overline{STR4}$ signal is low, gates 8 and 9 sample the M1 bit, which is the sign bit of the word from memory. A low M1 signal indicates that the sign is minus; a low $\overline{M1}$ signal indicates a plus sign. These signals are compared with the A+ or A- signal which is the sign of the contents of register A. Either of the two gates is permissive only to unlike signs from storage and register A. The flip-flop is restored initially to $\overline{CP}$ at buffer 19 by the t'11B+ timing signal. If the signs are unlike, the flip-flop is set to CP. If the signs are alike, the gates are blocked and the flip-flop remains restored to $\overline{CP}$.

If the subtract instruction has been staticized, the STR4 signal is low at gates 10 and 11, which also sample the signs of the word from storage and register A. When the signs of the two words are alike, the gates are permissive and the flip-flop is set to CP. Unlike signs block the gate to keep the flip-flop restored.

If complementing takes place in the first step of the add or subtract instructions, the result of the first step may be complemented in the second step of these instructions. When complementing is required during the second step of the instructions, FS 74 is generated to alert gate 12 which sets the flip-flop to CP. During a storage search operation or 0 instruction, FS 74 alerts gate 12 to set the flip-flop to CP.

3-72. OVERFLOW FLIP-FLOP. The overflow (OF) flip-flop receives signals which indicate that overflow conditions are present in various computer circuits. The flip-flop is used in the add, subtract, divide, and test instructions.

In the second step of the divide instruction, the OR control signal alerts gate 27. The gate samples the X1 bit of register X which, if low, is the indication of the division sentinel in the most significant digit position (MSD) of register X. When the sentinel is present, the gate is permissive and the flip-flop is set to OF. The OF signal controls the starting of the final stage of division.

Improper division occurs when the MQC countdown circuit counts below zero, indicating that the problem was programmed improperly or that an error is present.

The OF FF input gate 28, alerted by FS 31, samples the Q2 and Q3 outputs of the MQC FFs. The presence of Q2 and Q3 indicates a combination other than zero through ten, which means that the divisor was subtracted more than ten times from the dividend. Such a combination makes the gate permissive, generating the improper division signal (DI) and setting the overflow flip-flop to OF. The DI signal generates an ending pulse in the static register. This clears the STR FFs to zero and initiates a search for the c+1 address. The third step of division does not take place when improper division occurs.

When the sum of two ten-digit quantities exceeds the capacity of register A, the programmer must provide for the storage of the extra sum digit. When this condition is present, the A, C, $\overline{CP}$, and t11B signals are low at gate 29. The A and C signals signify decimal carry at the end of addition. Function signal 4 alerts the gate during the addition process. When the gate is permissive to its input signals, the flip-flop is set to OF and a high AO signal is generated.

Control signal Jam I2A is a high output of the I/O abnormal condition flip-flop in figure A2. The signal sets the overflow flip-flop to OF. The OF signal controls the overflow delay flip-flop which in turn controls the reading of the c+1 address. The overflow flip-flop is restored to $\overline{OF}$ by the OF2+ and GCB+ control signals. Signal OF2+ is the output of the overflow delay flip-flop; GCB+ is generated when the operator presses the GENERAL CLEAR button on the control panel.

3-73. OVERFLOW DELAY FLIP-FLOP. After overflow results from an addition or an abnormal condition, the program continues normally into a search for the next instruction. The programmer anticipates overflow by programming into memory location c+1 (the next storage location on the memory after the specified c address) the instruction he wants the computer to follow when overflow occurs. When the next instruction is located by the comparison operation, the TS FF is set. The overflow delay flip-flop generates a signal (OF2+) which keeps the TS FF set to $\overline{TS}$ to delay for one word time the reading of the selected address. As a result, the next address is read from the address following that specified by the register C contents.

During the third step of division, D3, the OF2+ signal is generated by FS 32A. The OF2+ signal in turn restores the overflow flip-flop to the normal $\overline{OF}$ condition.

3-74. MULTIPLIER/QUOTIENT COUNTER

The multiplier/quotient counter (MQC) operates during five instructions: circular shift, left shift, select stacker, multiply, and divide. The counter consists of four flip-flops, a countdown circuit, and a clear circuit (figure A14).

3-75. MQC FLIP-FLOPS. In the left or circular shift instructions, the flip-flops store the p7 digit of the instruction word. This digit designates the number of places that information is to be shifted. The countdown circuit counts down to zero from the number of shifts specified by the digit stored in the flip-flops. In the staticize step of either shift instruction, FS 2 alerts the input gates of the flip-flops. The input gates are permissive to inputs from the M lines only at the time interval t7B-. The four bits of the p7 digit of the instruction word from storage enter the flip-flops during this time interval. The outputs of the flip-flops are the Q1 through Q4 signals which go to the gates of the countdown circuit.

In the multiply instruction, the flip-flops are cleared initially to zero by a high signal from the clear MQC circuit, so that a multiplier digit can be read into the circuit from register X. If the multiplier contains five digits, they will be stored, one by one, in the MQC FFs. The least significant multiplier digit from register X is the first digit of the multiplier to be stored in the flip-flops. The four bits of the digit, X1 through X4, enter the flip-flops at gates 4A, 4B, 4C, and 4D, all of which are alerted by the IER-OR control signal (section 3-78). A low X signal denotes a 1 bit, a high X denotes a 0 bit. The four bits become the Q outputs of the flip-flops. In the second stage of multiplication, FS 61 alerts the gates of the countdown circuit. Table 3-4 shows the operation of the gates and their effect on the flip-flops. When the MQC has counted down to zero for each multiplier digit, the Q outputs of the flip-flops initiate a new phase of the multiplication process at the IER FF. (See section 4-30.)

At the beginning of the divide instruction, in the D1 step, the clear-MQC circuit clears the flip-flops to zero so that they can be used as a left shift path for the contents of register X. When the IER-OR signal alerts gates 4A, 4B, 4C, and 4D in the second and third steps of division, the X1 through X4 outputs of register X enter the MQC FFs to be stored for one pulse time. Then, the X input bits become the Q outputs and return to register X. In this way, the entire contents of register X are left-shifted. (See section 4-35,1.)

During the second step of division, the flip-flops and the countdown circuit monitor the number of divisor-to-dividend additions, and these numbers become the final quotient digits. In preparation for this quotient-counting operation, the four flip-flops are set initially to a count of ten. The OR control signal from the OR FF makes gate 1 permissive, jamming 1 bits into flip-flops 1, 2, and 4. The output of the four flip-flops, then, is 1101, the combination for the digit ten. The ten combination is stored in the flip-flops until the first divisor-to-dividend addition is accomplished, when the countdown circuit places the combination for 9 in the flip-flops. The countdown circuit reduces by a count of one the digit stored in the flip-flops with each ensuing addition. After the final addition of each add step takes place, the Q outputs of the MQC go to register X and become the final quotient digits.

In the select stacker instruction, 57, the number of the stacker which is to receive the card is programmed into the p7 digit of the instruction word. In the staticize step of the instruction the p7 digit on the M lines is stored in the MQC flip-flops just as in the shift instructions. The Q outputs of MQC which result from the p7 digit are sampled in the synchronizer circuits to select the specified stacker.

3-76. COUNTDOWN CIRCUIT. The countdown circuit consists of a group of gates which reduce by one the digit stored in the flip-flops. The circuit outputs are returned to the flip-flops, where the new digit (the original digit from the flip-flops minus one) is stored. This counting procedure continues as long as FS 61 alerts the gates of the countdown circuit. The circuit is used during the shift, multiply, and divide instructions. Function signal 61 alerts the gates which sample for a specific combination for the digit stored in the flip-flops. Table 3-4 shows the various Q input combinations to the gates from the flip-flops, the gates which are permissive to the input combinations, the output signals of the gates and their destination, and the output combination of the flip-flops. The information in table 3-4 is applicable to all four instructions involving the circuit.

Table 3-4. MQC Countdown Gates

UCT Code	Gate	Inputs	Outputs	Output Code of MQC
10 = $\frac{Q4}{1}$ $\frac{Q3}{1}$ $\frac{Q2}{0}$ $\frac{Q1}{1}$	17	Q1	N2B → FF1	1100 = 9
9 = 1 1 0 0	15	Q3 $\overline{Q1}$	N4 → FF1+FF2 N4B → FF3	1011 = 8
8 = 1 0 1 1	17	Q1	N2B → FF1	1010 = 7
7 = 1 0 1 0	16	Q2 $\overline{Q1}$	N3 → FF1 N3B → FF2	1001 = 6
6 = 1 0 0 1	17	Q1	N2B → FF1	1000 = 5
5 = 1 0 0 0	18	$\overline{Q1}$ $\overline{Q2}$ $\overline{Q3}$	N1 → FF3 N1B → FF4	0100 = 4
4 = 0 1 0 0	15	Q3 $\overline{Q1}$	N4 → FF1+FF2 N4B → FF3	0011 = 3
3 = 0 0 1 1	17	Q1	N2B → FF1	0010 = 2
2 = 0 0 1 0	16	Q2 $\overline{Q1}$	N3 → FF1 N3B → FF2	0001 = 1
1 = 0 0 0 1	17	Q1	N2B → FF1	0000 = 0
0 = 0 0 0 0	14	$\overline{Q4}$ $\overline{Q3}$ $\overline{Q2}$ $\overline{Q1}$	N5 → FF2	0110 = Count below zero (indicates improper division)
	18	$\overline{Q1}$ $\overline{Q2}$ $\overline{Q3}$	N1 → FF3 N1B → FF4	

3-77. CLEAR MQC CIRCUIT. The clear MQC circuit generates a signal that clears the flip-flops to zero. The CLQ output of the circuit is generated during the staticize step of any instruction, and during the multiply and divide instruction. During the first step of multiplication, FS 62 at gate 19 generates the CLQ signal. In the second, (D2) step of division, the CLQ signal is generated by control signal ORA+ at buffer 42. In the final step of division (D3), the signal is generated by FS 32A at buffer 42. The high CLQ signal blocks gates 5, 6, 7, and 8 of the flip-flops to restore the four flip-flops to $\overline{Q1}$, $\overline{Q2}$, $\overline{Q3}$, and $\overline{Q4}$ outputs. The flip-flops are thus cleared to zero to enable new information to enter.

3-78. IER-OR FLIP-FLOPS

The IER and OR flip-flops (figure A15) control the phases of the multiplication and division process. (IER is from the suffix of "multiplier"; OR is from the suffix of "divisor".) The IER FF is set initially during the first step of multiplication at gate 11, which samples for input signals indicating that the first step of the instruction (M1) is complete and that the second step (M2) is ready to begin. The STR inputs to the gate, when low, indicate that the static register has sequenced to the M2 step of the instruction. The $\overline{Q1}$ through $\overline{Q4}$ signals indicate that the MQC flip-flops have been cleared to zero. During future add steps of the same multiply instruction, the same $\overline{Q}$ inputs indicate that the countdown circuit has counted down to zero from the specified number of additions for each multiplier digit. As soon as the MQC counts to zero, as indicated at gate 11, the IER FF is set, generating high signals IER A1+, IER A2+, and IER+, and low signals IER-OR, and IER. These signals control the operations of the multiply instruction **(section 4-30)**.

During the divide instruction the OR FF provides control signals for the division process. In the first step of division, D1, FS 15 makes gate 9 permissive to set the flip-flop and generate high signals ORA+ and OR+, and low signals OR and IER-OR. These signals initiate the first phase (complementing and left shift phase) of the D2 step. At the end of the complementing and shift phase, timing signal t11B+ restores the OR FF, generating low ORA+, OR+, and IER-OR, and high OR, which initiate the add phase of the D2 step. All complement and shift phases thereafter are initiated at gate 10 which is alerted by FS 31 and is made permissive by input signals indicating decimal carry.

The MULTIPLY-DIVIDE ENDING TEST switch on the engineer's panel is intended for maintenance purposes primarily. When it is energized, a low output from the switch makes gates 100 and 101 permissive. The STR inputs arrive at gate 100 when the second step of multiplication, M2, is in progress. The TS1 and t'11B- signals indicate a specific storage location. In troubleshooting the multiply or divide instruction, the instruction is placed in a specific storage location so that the last phase of the second step coincides with the OpO pulse. This pulse, generated by the cycling unit, always synchronizes the maintenance oscilloscope with a specific storage location. The programmed instruction should end at the same time as the OpO pulse is generated, that is, at t'11B- which is the time when the TS1 signal from storage should occur. In the second step of division gate 101 is also alerted by FS 31. The gate is made permissive by energizing the MULTIPLY-DIVIDE ENDING TEST switch. Signals TS1 and t'11B- also alert the gate. When gate 101 is permissive, it generates the DEB and DEA control signals. Signal DEB jams the OR FF to the add phase at gate 12. Signal DEA initiates the third and final step of division by setting the D3 FF (section 3-3).

The final step of a multiply-end operation is a right-circular shift of the contents of registers A and X. The final step of a divide-end operation is an interchange of the contents of the two registers. In this interchange, the contents of register X are shifted through the MQC FFs. The final quotient digit, computed in MQC, is placed in the p1 position of register A.

3-79. STORAGE UNIT

The storage unit performs two major functions, word storage and computer timing. The storage unit stores instruction words and data words which process input data from punched cards or the manual keyboard. The stored information can be read from the drum for use in the processor or input-output synchronizers. The storage unit sends various types of timing pulses to the control, arithmetic, and input-output units to time the internal operations of the system.

3-80. STORAGE DRUM

The major component of the storage unit is the rotating storage drum. Figure 3-1 shows, from a theoretical standpoint, the simplified, functional arrangement of the storage drum.

Information is stored on the surface of the drum in the form of magnetized areas which are written and read by read-write heads. The four bits of a digit are written in parallel across the drum. A check bit is written in the fifth bit position. The digits of an information word are written serially around the surface of the drum. A recorded word, therefore, consists of 12 digit positions around the drum, each digit consisting of five bits across the drum. The main storage area of the drum can store 5000 of these 12-digit information words.

The main storage area is divided into 25 areas known as bands, around the circumference. Each band has 200 word-storage locations. Each band consists of five tracks, in which are stored the bits of a digit.

Of the 25 main storage bands, 20 are designated normal-access bands (locations 0000-3999); and five are designated fast-access bands (locations 4000-4999). Each fast-access band is serviced by four read-write heads per track (20 heads per band), which are 90 degrees apart. Figure 3-1 shows only three of the four heads of a fast-access track; the fourth head is on the underside of the drum. The use of four heads makes any storage location on a fast-access band available within a maximum of 50 word times, or one-quarter of a drum revolution. Each normal-access track is serviced by only one read-write head per track (five heads per band). Any storage location on a normal-access band is available within a maximum of 200 word times, or one complete drum revolution.

Figure 3-2 illustrates the bit pattern formed by a stored computer word. A computer word consists of 12 digits--ten information digits, one digit for the sign, and one digit position for the space between words. The stored word in the figure is: - 6187203459_. Tracks 1 through 4, with biquinary bits weighted 1, 2, 4, and 5 (in that order) store the bits of the digits. Track 5 stores the check bit (section 3-90). The example shows the serial-parallel method of storage. That is, the digits of a word are written serially, while the bits of each digit are written in parallel across the drum.

The storage locations for the 25 bands follow this paragraph. Bands 1 to 20 are the normal-access bands with a total capacity of 4000 words; bands 21 to 25 are the fast-access bands with a total capacity of 1000 words.

NORMAL-ACCESS BANDS

Band 1	0000-0199	Band 11	2000-2199
Band 2	0200-0399	Band 12	2200-2399
Band 3	0400-0599	Band 13	2400-2599
Band 4	0600-0799	Band 14	2600-2799
Band 5	0800-0999	Band 15	2800-2999
Band 6	1000-1199	Band 16	3000-3199
Band 7	1200-1399	Band 17	3200-3399
Band 8	1400-1599	Band 18	3400-3599
Band 9	1600-1799	Band 19	3600-3799
Band 10	1800-1999	Band 20	3800-3999

FAST-ACCESS BANDS

Band 21	4000-4199
Band 22	4200-4399
Band 23	4400-4599
Band 24	4600-4799
Band 25	4800-4999

In figure 3-1, the normal-access band containing the stored word example is band number 6, reading from right to left and excluding the timing band. The stored word is in the next to the last location of band 6 which contains storage locations 1000 to 1199, or address 1198. The addressing system is explained in detail in section 4-4.

3-81. BUFFER STORAGE AREAS. In addition to the 5000-word capacity of the main storage bands, a complete band and two tracks are used for input-output buffer storage. Figure 3-1 shows that the print buffer area consists of two tracks and that four tracks are divided between the high-speed-reader buffer (locations 000-099) and the read-punch-unit buffer (locations 0100-0199).

The buffer storage areas compensate for differences in the speed of operation between the relatively slow input-output devices and the fast rate of computation. For example, the time necessary for the printer to advance and print one line of information is approximately equal to the time necessary for 30 drum revolutions. If the information to be printed were available to the printer only from main storage locations, the processor could not process other instructions for nearly 30 drum revolutions, because the read-write heads which serve main storage would be occupied with the transfer of information for three drum revolutions and actual printing would take an additional 27. To avoid wasting computer time, information to be printed first is transferred from main storage to a buffer storage area. Once the transfer to the buffer areas of information to be printed is complete, the read-write heads which serve main storage are free to transfer data and instruction words as specified by the program.

Buffer storage areas are provided also for information processed by the card reader and the read-punch device. Information read from punched cards by either the card reader or the read-punch unit is transferred to a buffer storage area and then to main storage. Information which is to be punched on cards first is transferred from main storage to a buffer storage area and then to the read-punch device.

The print buffer area consists of two tracks which store information sufficient to print one line on the printer. Eight read-write heads serve the two print buffer tracks. Each track is served by heads mounted at 90-degree intervals around the circumference of the drum. For more detailed treatment of the print buffer area, see the New Univac® Type 7901 High-Speed Printer manual.

The card buffer storage area consists of four tracks which are hereafter referred to as the card buffer band. The card buffer band is divided into two parts; one half serves the card reader while the other half serves the read-punch device. The card buffer band is served by eight read-write heads, two for each of the four tracks. The heads are mounted at 180-degree intervals around the circumference of the drum. For more detailed explanation of the card buffer areas, see the manuals New Univac® Type 7902 Card-Sensing Punch Unit, 90 Column and New Univac® Type 7904 Card-Sensing Unit, 90 Column.

3-82. TIMING BAND. The timing band, five tracks wide, controls the addressing of storage locations and the generation of timing signals in the cycling unit.

Each of the 200-word storage locations around the drum is identified by a combination of digits stored permanently in the timing band. The expanded view of the timing band (figure 3-3) shows the code combinations stored in a section of the timing band. When a storage search takes place, the recorded combinations on the timing band are read from the drum. The 200 unique timing band addresses are read, one by one, by the timing band read circuits. The TS signals, indicating storage addresses, are transferred to the M lines and are compared with the desired address. When the desired address corresponds to the address being read by the timing band heads, the proper channel is selected and the information is read from that location.

A time selection address is located on the word channel directly preceding the word with which it is associated. This allows one word time of delay for the addressed word to be read by the read-write heads.

Only five timing-band word areas are shown in figure 3-3. The three lowest-order digit positions of each word area contain the three digits indicating a channel across the drum. Because the timing band addresses differ by one word time from the main storage addresses, the digits 197, stored in the uppermost word area in the figure, indicate that any word stored across the drum in the associated channel is located in the 196th position in one of the bands. The band is selected in the band selection circuits (section 4-6). The time-selection addresses stored in the timing band are numbered 000 through 199.

A 1 bit is contained in track 5 for any digit containing an even number of 1 bits. For example, the code combination for time selection address 000 does not contain any 1 bits. To ensure that an odd number of 1 bits is read from the drum for any stored character, a 1 bit is added in the fifth bit position of the digits. Because the addresses can be numbered only from 000 to 199, the most-significant digit of an address can be only a 0 or a 1. For this reason, the most-significant digit of the channel address is identified by a single bit, the bit in the track 1 position.

The timing combination shown in figures 3-1 and 3-3 is recorded permanently in the t6 position of every timing-band word. The combination, 1101, is read by the timing-band read circuits and goes to the cycling unit to generate the signals used to time the internal operations of the system (sections 3-84, 3-85).

Signals that control the three input-output synchronizers are also stored permanently in the timing band. These signals are known as input-output sentinels (section 3-86) and are stored in the bit positions which are shown as empty in figures 3-1 and 3-3.

3-83. SPROCKET TRACK. In a single track around the drum, there are 2400 bit positions. In the two sprocket tracks, a permanent bit is stored in each of the 2400 positions. Two heads per track read the sprocket bits to ensure that at least one is properly read every pulse time. The sprocket signals go to the sine wave clock circuits which generate synchronized A- and B-phase power pulses. The power pulses control the magnetic amplifier elements throughout the computer circuitry.

3-84. TIMING BAND READ CIRCUITS

The timing band read circuits (figure A17) consist of five amplifier circuits, which convert the combinations stored on the timing band into time selection signals, the timing band flip-flop, and the timing error flip-flop. The TS signal outputs of the read circuits can be grouped into three categories: storage address signals, timing-combination signals, and control signals.

The storage address signals, which are the three lowest order digits of each word in the timing band, go to the comparator of the arithmetic unit, via the M buffers, to be used in the search operations. These signals are stored in the t0, t1, and t2 positions of the timing band.

Once every word time, the timing combination is read from the t6 position of every timing band word into the cycling unit. The cycling unit uses the 1101 combination from the timing band to generate signals which time internal computer operations.

The TS outputs of the timing band read circuits also work in conjunction with the timing signals from the cycling unit as input-output sentinels. The sentinels, which are used in controlling the input-output synchronizers, are explained in section 3-86.

The timing band flip-flop ensures that the t2 position of location 199 of the timing band contains a zero because the next storage address is 000. During the initial recording of the timing band, t2 of location 199 is recorded first and t1 of location 199 is recorded last. Since the recording is stopped at t1, it may overlap into the t2 position, causing extraneous information to be

recorded. To prevent the reading of this extraneous information, readout of the 000 combination is simulated by the timing band flip-flop.

The flip-flop is set at gate 20 by the A sentinel in location 198. The setting of the flip-flop causes the timing band read circuits to indicate 0 bits on the TS1 through TS4 tracks and a 1 bit (check bit) on the TS5 track.

The timing error flip-flop, also shown in figure A17, is explained in the error circuits section, section 4-39.

3-85. CYCLING UNIT

The cycling unit (figure A16), controlled by the timing combination from the timing band, generates the timing signals used to synchronize all computer operations. The cycling unit consists of the delay line which produces the timing signals, the cycling-unit error flip-flop (section 4-40) and the even word flip-flop.

Every word time the timing combination TS4, TS3, $\overline{TS2}$ and TS1 (1101) is transferred from the timing band, through the timing band read circuits, to the cycling unit. The combination is present at gate 102 at t6B, making the gate permissive and generating high signal t7A+. One half pulse-time later, high t7B+ and low t7B- signals are generated. The input signal continues through the cycling unit, which is actually a delay line, generating the many variations of timing signals. The A- and B-phases of signals t0 through t11 are generated in high (+) and low (-) states. Generally, a high signal is used as a blocking signal and a low signal is used as an alerting signal on gates throughout the system.

The every-other-word flip-flop (EW FF) generates signals which synchronize signals from the control panel or input-output devices with the timing of the processor. Control signal Quad+, generated by RPU drum revolution counter (figure A26) sets the flip-flop, generating low signal EW and high signal $\overline{EW}$. These conditions exist until time interval t11B, when the high t11B+ signal at gate 48 overrides low EW, changing the state of the flip-flop (EW high and $\overline{EW}$ low). The flip-flop remains in this state for one word time until low signals t11B- and $\overline{EW}$ at gate 47 set it again. The flip-flop thus changes state every word time.

Most external signals (generated by manually or mechanically operated switches) are sent to the set gates of synchronizing flip-flops under the control of one of the three output signals of the EW flip-flop. The output signal of the synchronizing flip-flops is sent to another gate that is also under the control of the same output signal from the EW flip-flop. A timing signal alerts both gates. Since the low output of the EW flip-flop and the timing signal occur together only once every other word time, the external signal must recirculate in the synchronizing flip-flop for two word times. During these two word times, if the signal is a weak or partial signal it will build up or die out. If it dies out, that flip-flop is set again the next time the EW flip-flop output signal and the timing signal occur together because switch signals last for more than two word times.

3-86. INPUT-OUTPUT SENTINELS

The input-output sentinels control the transfer of information between the input-output devices and the buffer storage areas, and between the buffers and main storage. The sentinels are 0 bits or 1 bits recorded on tracks of the timing band in specific positions of one or more word locations, and are identified by one or more alphabetic, and sometimes numeric, characters.

As shown in table 3-5, each timing-band word location contains a timing band address (section 3-82), a timing combination (section 3-85), and may also contain one or more sentinels. The timing band address requires nine bit positions, as indicated by X's in table 3-5 and the timing combination, 1101, requires four bit positions. The remaining bit positions of each timing band word are available for the recording of input-output sentinels. Table 3-5 is a composite of all 200 word locations of the timing band, and shows the position of each sentinel in the location or locations in which it is recorded.

Some sentinels are recorded in only one location of the timing band. For example, the A sentinel is recorded as a 1 bit on track 1 at the t9 position of location 198 of the timing band. The gates controlled by the A sentinel require low TS1 and t9B signals, which occur together only in the 198 location and restrict the operation of the gate to once a drum revolution. The F sentinel is typical of sentinels which are recorded in more than one location around the band, and is recorded as a 1 bit on track 4 at the t10 position of 14 word locations: 004, 013, 022, 045, 054, 066, 085, 098, 107, 129, 138, 151, 169, and 182. The gates controlled by the F sentinel require low TS4 and t10B signals, which occur together 14 times during one drum revolution.

Table 3-5. Input-Output Sentinel Chart

Timing Signals	Timing Band Combination Signals			
	TS4	TS3	TS2	TS1
t11	Q4	Q5	Q6	
t10	F	E	D	C
t9			BT1	A
t8	X	PS	B	OW
t7	M3	M2	M1	Y
t6	1	1	0	1
t5	R6	R5	K	TO
t4		Q3	Q2	Q1
t3	J	ST	I	H
t2	G3	G2	G1	X
t1	X	X	X	X
t0	X	X	X	X

Sentinels	Produce Sentinel
M1 $\overline{M2}$ $\overline{M3}$	P1
$\overline{M1}$ M2 $\overline{M3}$	P2
M1 M2 $\overline{M3}$	P3
$\overline{M1}$ $\overline{M2}$ M3	P4
$\overline{G1}$ G2 $\overline{G3}$	R1
G1 G2 $\overline{G3}$	R2
$\overline{G1}$ $\overline{G2}$ G3	R3
G1 $\overline{G2}$ G3	R4

Some sentinels are made up of unique combinations of other sentinels. For example, the P1 sentinel is a combination of the sentinels M1, $\overline{M2}$, and $\overline{M3}$, and is therefore recorded as a 1 bit on track 2, a 0 bit on track 3, and a 0 bit on track 4 at the t7 position of five word locations: 107, 127, 147, 167, and 187. A barred sentinel, such as $\overline{M2}$, is recorded as a 0 bit.

A more detailed explanation of the sentinels, their locations and function is found in the synchronizer sections of the three input-output manuals.

3-87. WRITE CIRCUIT

The components of the write circuit (figures A18 and A19) enable information from the computer to be written on the drum. Information is transferred from the M buffers of the arithmetic unit into the write circuits and converted into the form necessary for recording. All information to be written into storage from the processor must be transferred from the arithmetic registers by transfer instructions. Information to be written into storage from the input-output buffers is sent directly to the M buffers and the write circuits by buffer-to-storage transfer instructions. The components of the write circuit are described in this section.

3-88. WRITE PEDESTAL GENERATOR. Before the write circuits can be used for writing on the drum, the read circuits must be deenergized. During any instruction which involves writing information into storage, a high signal is applied to buffer 104 and the write pedestal generator. The output of the generator is a write pedestal which disconnects the read amplifiers of the normal access heads. The IR (inhibit read) output of the generator disconnects the read amplifiers of the fast access heads.

3-89. WRITE INPUT CIRCUITS. The four bits of each digit to be written are transferred on the M lines into the write input circuits. The barred M inputs ($\overline{M1}$ through $\overline{M4}$) go to the write input circuits of the normal access write circuits and into the phase modulation coder. The $\overline{W1}$ through $\overline{W4}$ outputs of the circuits go to the phase modulation coder of the fast access write circuits (figure A20).

3-90. CHECK-BIT CIRCUIT. The check-bit circuit checks the accuracy of information written on and read from the drum. The check is made to ensure that no bits have been affected by failure of any of the transmitting elements. When a digit to be written contains an even number of 1 bits, a 1 check bit is added. When a digit contains an odd number of bits a 0 check bit is added. Because all

digits contain an odd number of bits when recorded on the drum, they should also contain an odd number of digits when read from the drum. The read circuit maintains a check on the number of bits read from the drum.

The digits of a word to be written are sent in parallel on the M lines into the write input circuits and the check-bit circuit. An even number of bits in a combination generates a high $\overline{CK}$ signal. An odd combination of bits causes the $\overline{CK}$ signal to be low. The $\overline{CK}$ signal controls the writing of a check bit in the phase modulation coder. For example, if the combination for 7 (1010) is applied to the check-bit circuit, the inputs are M4, $\overline{M3}$, M2, $\overline{M1}$. Only diode gate 26F is permissive to the input signals, and it generates a high $\overline{CK}$ signal. The $\overline{CK}$ signal causes a 1 bit to be written in the fifth bit position of the digit on the drum. The check-bit circuit is used also to check the number of bits when information is read from the drum.

3-91. WRITE FLIP-FLOP. The write flip-flop controls the write operation by alerting or blocking the input gates of the phase modulation coder. In the register-to-storage and buffer-to-storage transfer instructions, function signals 3, 72, and 98 alert the flip-flop input gates. Control signals RSC2 (gate 5A) and RSC5 (gates 100, 101) set the write flip-flop and indicate that the read flip-flop of the input-output buffer read circuits is set. Information then can be read out of the input-output buffer band and be written onto the main storage. The set output of the write flip-flop is a low signal which alerts input gates 20 through 25 of the phase modulation coder. If the flip-flop is restored the input gates are blocked. The W6 signal from the flip-flop, when low, alerts the phase-modulation-coder input gates of the fast access write circuits.

3-92. PHASE MODULATION CODER. The phase modulation coder receives an input pulse and transforms it into two positive sine waves one of which is delayed one-half pulse time. The phase of the two output pulses determines whether a 1 or a 0 is written on the drum.

Figure 3-4 shows a typical phase modulation circuit with a 1 input (a 1 is a high input signal). The high input pulse is complemented to a low by the input complementer 1. Gates 2 and 2A, alerted by the set output of the write flip-flop, are permissive to the low pulse. Complementing amplifier 2 complements the signal to a high pulse, which goes through a buffer to one end of the write transformer. Complementer 2A complements the low input signal to a high pulse which

goes to amplifier 3. Amplifier 3 delays the pulse for one-half pulse time, and sends it to the opposite end of the write transformer. The first output of the transformer occurs one-half pulse time earlier than the second output. The first pulse draws current in a positive direction at the center-tapped write-head winding, supplying the positive portion of the current waveshape. The second pulse draws current in a negative direction at the head winding to supply the negative portion of the waveshape. The current waveshape of a 1 recorded on the drum is shown in figure 3-5a.

A 0 input to the coder (a 0 is a low input signal) also produces two high outputs to the write transformer, but with reversed timing. The low input is complemented to a high by the input complementer 1. The high signal blocks gates 2 and 2A but is buffed into amplifiers 4 and 4A. The output of amplifier 4 goes directly to one end of the write transformer. The output of amplifier 4A goes to the opposite end of the transformer via amplifier 5 which delays the pulse for one-half pulse time. The input to both ends of the write transformer is a high pulse, but the first input precedes the delayed input by one-half pulse time. When the first output precedes the second, the negative portion of the current waveshape on the drum precedes the positive portion (figure 3-5b). A 011 combination would appear on the drum as a low-high, high-low, high-low configuration (figure 3-5c).

The check bit is also phase-modulated, at gate 25. The $\overline{CK}$ signal is high when a 1 bit is to be added in the fifth bit position and low when a 0 is to be written.

The outputs of the write transformers of the normal access read-write circuits (figure A19) are the WD signals which go to the memory switches. The write transformer outputs of the fast-access circuits are the WF signals. They also go to the memory switch.

3-93. READ CIRCUIT

The components of the read circuit (figures A18 and A19) enable information to be read from the storage drum. The major components of the read circuit are the read flip-flop, the read output circuits, the check bit circuit, the check-timing flip-flop, and the memory-check flip-flop. The latter two components are explained in section 4-38. The check-bit circuit, which functions in both the read and write operations, is explained in section 3-90.

3-94. READ FLIP-FLOP. The read flip-flop controls readout from the drum. When the flip-flop is set, a low output signal makes the gates of the read output circuits permissive to output from the drum. When the flip-flop is in the restored condition, a high signal blocks the gates to prevent the read circuits from reading from the drum.

The flip-flop can be set at gate 42C during a print instruction. In this instruction, information is read from main storage and transferred into the print buffer storage. The gate is alerted by FS 42, and $\overline{\text{STR4}}$ indicates that the print instruction, and not a paper advance instruction, is taking place. The TS2 and t8B- signals constitute a B sentinel (section 3-86).

During a storage-to-card buffer transfer instruction, the read flip-flop is set at gate 42B so that information can be read from storage. Function signal 30 alerts the gate to set the flip-flop if the OW sentinel (TS1 and t8B-) is present.

In a search operation the flip-flop is set so that information can be read from a selected address. Function signal 1 alerts gate 42A and the TS and $\overline{\text{OF}}$ signals indicate that the search operation was successful. This gate is blocked by high Block RD1 and Block RD2 signals during a register search operation.

The set output of the flip-flop alerts gates 45A and 45B, one of which is made permissive by FM (fast memory) or NM (normal memory) signals. The FM signal indicates that the information is to be read from the fast storage bands, therefore by the fast access read write heads. If FM is present, gate 45B operates to generate the RGF signal. This signal alerts the read output gates of the fast access read circuits (figure A20). This allows the fast access read heads to read information from the fast access bands.

If the NM_f signal is present, rather than the FM signal, (only one can be present at a time) gate 45A operates to alert the output gates of the normal storage circuits. The NM signal indicates that information is to be read from the normal access bands of main storage.

3-95. READ OUTPUT CIRCUIT. The four information bits read from the normal access bands of the drum become the DM'1 through DM'4 signals. The four bits read from the fast access bands of the drum become the DM15 through DM45 signals. These signals go directly to the M buffers and onto the M lines. The M lines transfer the outputs

of the read circuit to the components specified by the instruction presently being processed. The M lines also return the read outputs to the check bit circuit. Here the information digits are checked for an even number of 1 bits just as they were in the write operation. Section 4-38 explains the operation of the check-bit circuit, the check timing flip-flops, and the memory-check flip-flop in reading erroneous combinations from the drum.

3-96. MEMORY SELECTION CIRCUITS

The memory selection circuits control the memory switches, which energize a specific read-write head for reading or writing. Head selection, band selection and switch selection are accomplished by the memory selection circuits (figure A18).

3-97. BAND SELECTION FLIP-FLOPS. The band selection flip-flops are divided into two groups, those which determine the hundreds digit (p3) of the desired storage address, and those which determine the thousands digit (p4) of the address. For example, if the location to be written into or read from is 3689, the p3 band selection flip-flops generate signals which indicate the 6 digit of the address and the p4 flip-flops generate signals which indicate the 3 digit. Digits 8 and 9 are determined in the comparator (section 3-53).

Register C contains the desired address. Its outputs are on the S lines during memory selection. The bits of the p3 digit of the address are sampled by the five p3 band selection flip-flops (table 3-6). The table shows that if the p3 digit of the address is, for instance, 2 or 3, the MS2 flip-flop is set generating signal MS2. The MS2 signal goes to the switch-selection gate matrix to control the selection of the proper memory switch.

The p4 digit of the storage address determines the thousands digit of the desired storage location. Only the two lowest-order bits of p4 are required to determine the thousands digit because the digit ranges from only zero to four. The two bits are read directly from register C (signals C13, C14, C23, and C24) into the MS 10 and MS 20 flip-flops. The flip-flops are set or restored by the signals from register C. Their outputs (MS 10 and MS 20) indicate the fourth, or thousands digit of the address. These output signals also go to the switch-selection gate matrix.

Table 3-6. Band Selection Flip-Flops (p3)

p3 Digit	p3 Bits				Flip-Flop Output
	S4	S3	S2	S1	
0	0	0	0	0	MS0
1	0	0	0	1	MS0
2	0	0	1	0	MS2
3	0	0	1	1	MS2
4	0	1	0	0	MS4
5	1	0	0	0	MS4
6	1	0	0	1	MS6
7	1	0	1	0	MS6
8	1	0	1	1	MS8
9	1	1	0	0	MS8

The fast/normal flip-flop determines whether the desired location is the fast or normal access area of storage. The C33 and C44 signals from register C indicate whether the third bit of the p4 digit is a 1 or a 0. If it is a 0, the p4 digit is less than 4; therefore the desired address is in locations 0000-3999. These are normal locations and as a result the NM signal is generated. If the third bit of p4 is a 1, the p4 digit is a 4, therefore the desired address is in locations 4000-4999. Because these are fast access locations, the FM signal is generated by the fast/normal flip-flop. The FM or NM outputs also go to the switch-selection gate matrix.

3-98. CLEAR BAND SELECTION CIRCUIT. The band selection flip-flops, which process the p3 and p4 digits, operate in parallel with and at the same time as the time selection circuits which process the p1 and p2 digits. If the comparison circuits determine that the p1 and p2 digits are unequal, the TS FF generates $\overline{TS}$. The $\overline{TS}$ signal indicates that there is no need for further band selection. Function signal 1 alerts the gate which samples the $\overline{TS}$ signal. If $\overline{TS}$ is low, the circuit generates a high output to restore the eight band selection flip-flops before the outputs of the flip-flops can affect the switch selection circuits. The FS 30+ signal on gate 62 is low during all instructions except those involving the input-output buffers. Therefore, the gate is permissive at all other times. During the instructions which involve the input-output buffers, a specific band must be chosen but not a specific location in that band. Therefore, FS 30+ blocks gate 62 so that the band selection flip-flops are not cleared. The flip-flops can, as a result, continue to select a band within main storage until they are restored.

Although FS 1A is high during a search operation, the effect of FS1 overrides that of FS 1A at gate 64. However, when any instruction other than Sc is in process, FS 1A is low. As a low signal, FS 1A generates a high output which clears the band selection flip-flops.

3-99. HEAD SELECTION FLIP-FLOPS. The two lowest-order digits of the desired address are compared with the same two digits of the timing band addresses in the comparator circuits. These two digits narrow the search to four possible channels. The desired location then is in one of four quadrants of the drum. Head selection 1 FF and head selection 2 FF determine which of the four quadrants contains the desired information. The outputs of the flip-flops go to the memory-switch selection matrix. More detailed information on the two flip-flops can be found in section 4-5, in which is explained the complete memory selection operation.

3-100. SWITCH SELECTION CIRCUITS. The switch selection gates, shown as a matrix in figure A18, sample the outputs of the band and head selection flip-flops to determine which memory switch is to be energized. Only one of the switches can be energized by the 13 inputs to the gates, and the output of the gates goes to a switch driver. The elements of a switch driver are shown within the left driver in the figure. The outputs of the switch drivers are the FS 0 through FS 38 signals, one of which energizes the proper memory switch. The numbers within the switch driver blocks on figure A18 signify the bands controlled by each driver.

If the storage location is within the 1000-1199 normal access band, gate 6A is permissive to the NM, MS0, MS 10, and $\overline{\text{MS 20}}$ low input signals. The switch driver output is the FS 10 signal which energizes the proper switch to read from the chosen band. The same switch driver also serves the fast memory switches. In addition, the driver selects a switch which energizes one of the four heads of a fast access band. The FS 10 signal can be generated also by input signals FM, MS2, $\overline{\text{QS2}}$, and QS1 at gate 6B. The 4203 designation refers to band 4200, head 3. The top number in each switch driver block refers to the normal access band, the lower number refers to both the fast access band and the head of that band.

3-101. MEMORY SWITCH. The memory switches (figure A21) select a specific group of ten heads as dictated by the FS signal inputs. The ten selected heads include five normal access heads which record the five information bits, and five fast access heads which also record five information bits. The read and write circuits determine which five of the ten heads are selected. For example, if the FS 10 signal energizes switch 1000, ten heads are chosen. However, the FS 10 signal was generated with the help of the low FM signal, indicating fast access storage. In reading from the drum the NM signal is therefore high and blocks the normal read circuits from reading, while the low FM signal allows the fast read circuits to read. As a result, the NM signal blocks the transistor flip-flops of the read units to block readout to the DM' line, while the FM signal makes the transistor flip-flops permissive, allowing information from fast access read heads to enter the DM lines. In writing on the drum, the NM and FM signals block the input gates of the phase modulation coders of either the normal or fast circuits (figures A19 and A20).

The WF (fast storage) and WD (normal storage) signals are the inputs to the selected heads when writing, or the outputs of the heads when reading from the drum. Section VI includes circuit descriptions of the read and write circuits.

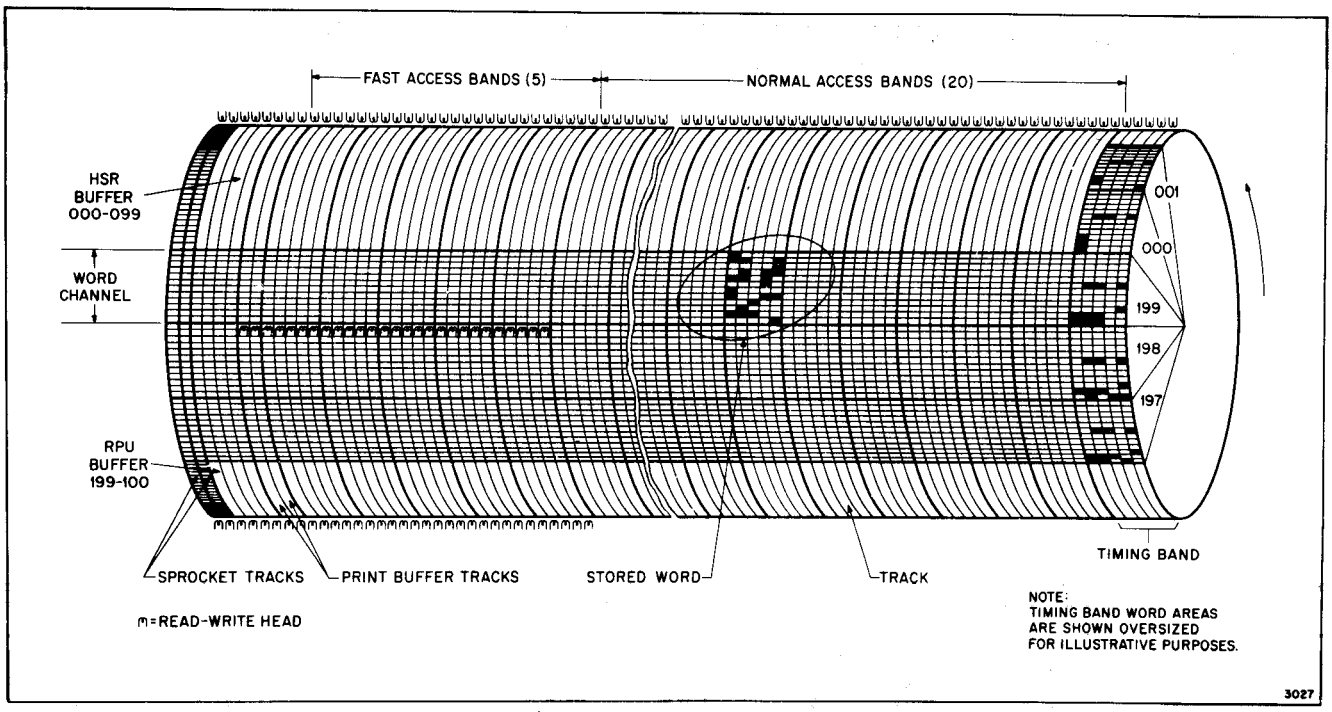


Figure 3-1. Storage Drum Showing Computer Characteristics

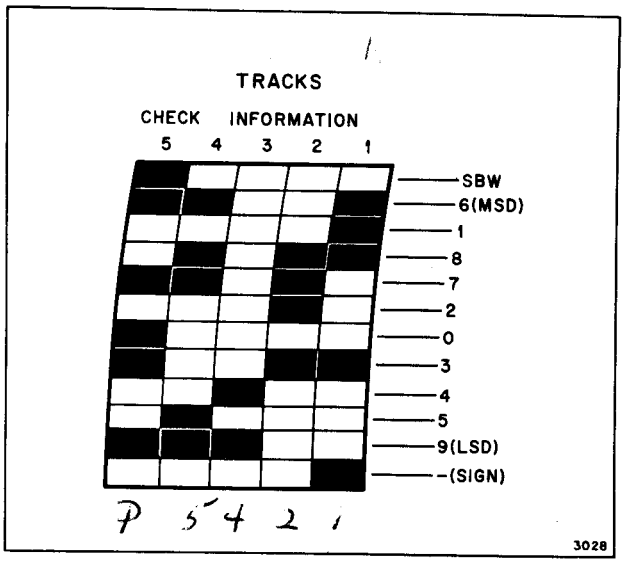


Figure 3-2. Word-Storage Pattern

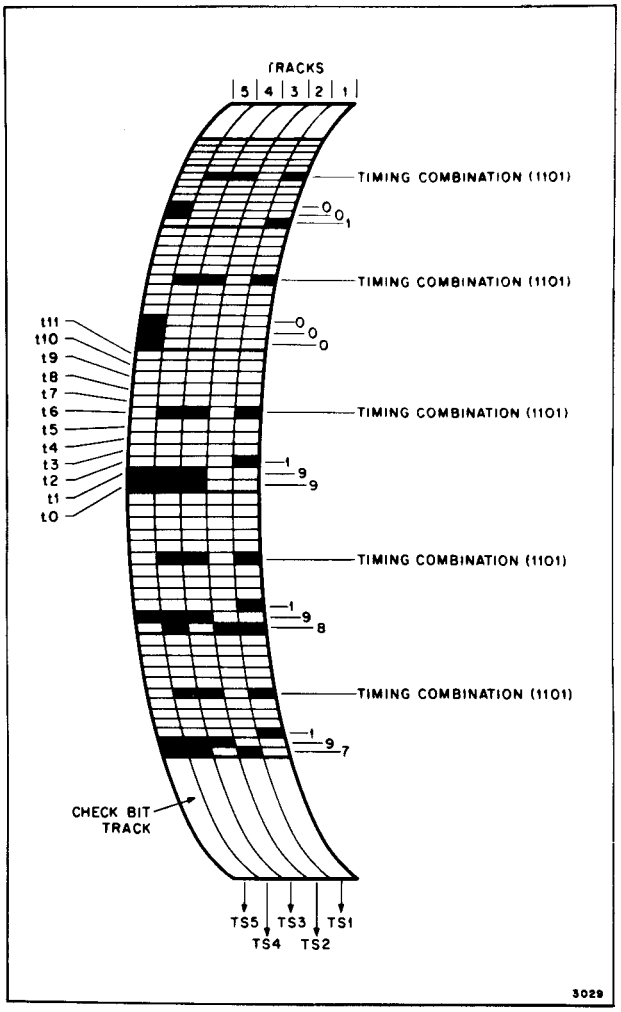


Figure 3-3. Timing Band, Expanded View

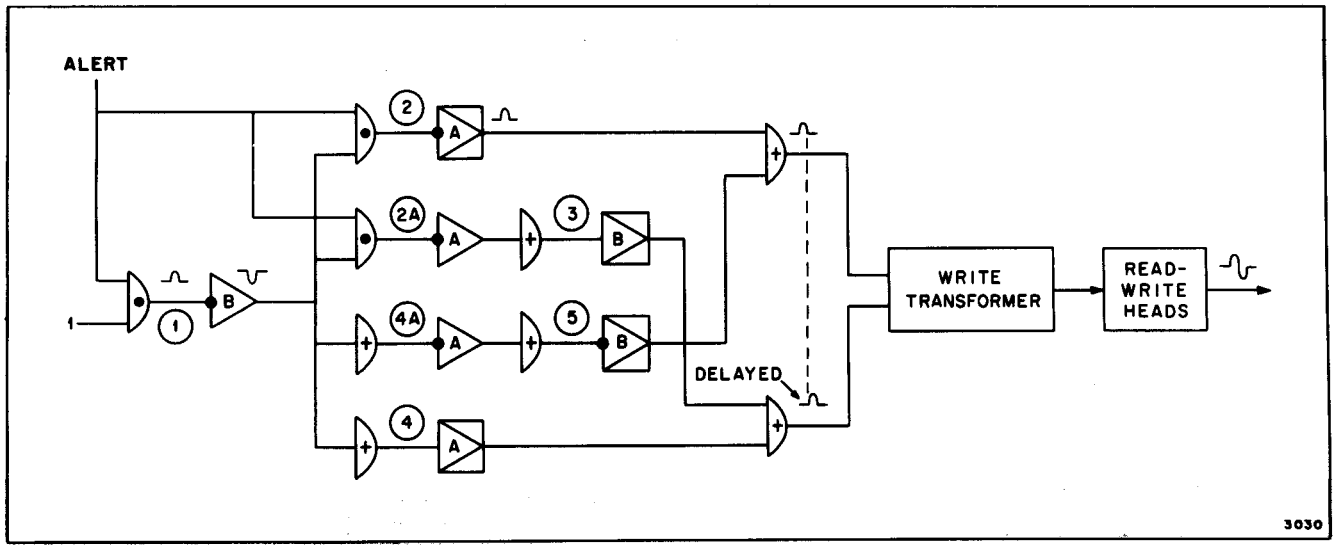


Figure 3-4. Phase Modulation Coder

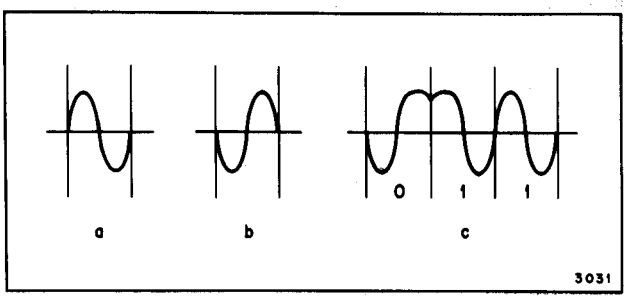


Figure 3-5. Phase Modulation Waveshapes

SECTION IV

THEORY OF OPERATION

4-1. INTRODUCTION

Section II, by explaining the use of logical symbols and elements, enables the reader to interpret the logical circuitry of the processor. Section III, by describing the logical components of the processor, familiarizes the reader with the specific circuits encountered in this section, section IV, and in the Analysis of Instructions manual. The purpose of this section is to apply the knowledge gained in the foregoing sections to actual computer operations in which more than just an understanding of the logical circuits is necessary. Types of instructions not described in section IV are treated on the more general level in section V. All instructions are treated in complete detail in the Analysis of Instructions manual.

4-2. BASIC OPERATION CYCLE

The basic operation cycle consists of the steps necessary to perform any instruction completely. All instructions require at least three basic steps. Instructions requiring only three steps are those in which no operand is involved, such as a simple register-to-register transfer. Most instructions, however, require four basic steps because of the need for an operand. For this reason, a basic operation cycle consists of four steps. In instructions requiring only three steps the third or search-for-operand step is bypassed. The four steps of the normal cycle, with the search for the instruction as the starting point, are:

(1) Search for the instruction (Sc).

(2) Staticize the instruction (Sz).

(3) Search for the operand (Sc-m).

(4) Execute the instruction (Ex).

When an instruction is completed, an ending pulse is generated which clears the static register and starts the next cycle by initiating a search for the next instruction in the program (search for the instruction).

When an instruction has been located on the drum it is read from storage by the read circuits and is stored in the static register and register C (rC) (staticize the instruction). If the instruction requires an operand another search is made for this quantity (search for the operand). When the operand is located, the first step of the instruction is executed (execute the instruction). Any further steps in the instruction are executed in order after the first execution step. At the completion of the execution of the instruction, an ending pulse is produced to start the sequence once more.

4-3. SEARCH-FOR-INSTRUCTION STEP

After an instruction has been completed a signal is applied to the ending-pulse buffer of the static register. As shown in figure 4-1, the ending-pulse buffer generates the EP signal which is applied to the restore gates of the seven static-register flip-flops. The high EP signal restores all seven flip-flops to their barred outputs, which indicate 0 bits at t11B of the execute step of the preceding instruction. The new outputs of the static register drive the instruction decoder.

Only the search (Sc) gateline of the instruction decoder is permissive to the 0 bits. The search gate interprets the two 0's in the two lowest-order bit positions, STR1 and STR2, and generates the 1A function signal. Function signal (FS) 1A drives the function encoder and generates function signals 1, 58+, 63 and 74. These four function signals and FS 1A control the search-for-instruction step.

In the search-for-instruction step, the storage address specified by the c address in rC must be located, the specified band selected, and the storage-read circuits alerted to read the instruction word contained in the address.

4-4. LOCATING THE STORAGE ADDRESS. In the search for a storage address the following must be determined: the word channel and drum quadrant containing the desired address, the proper band, and the read-write head which is to be energized to read the contents of the location. One of four heads must be selected in reading from a fast-access band. In normal access, however, only one head can be

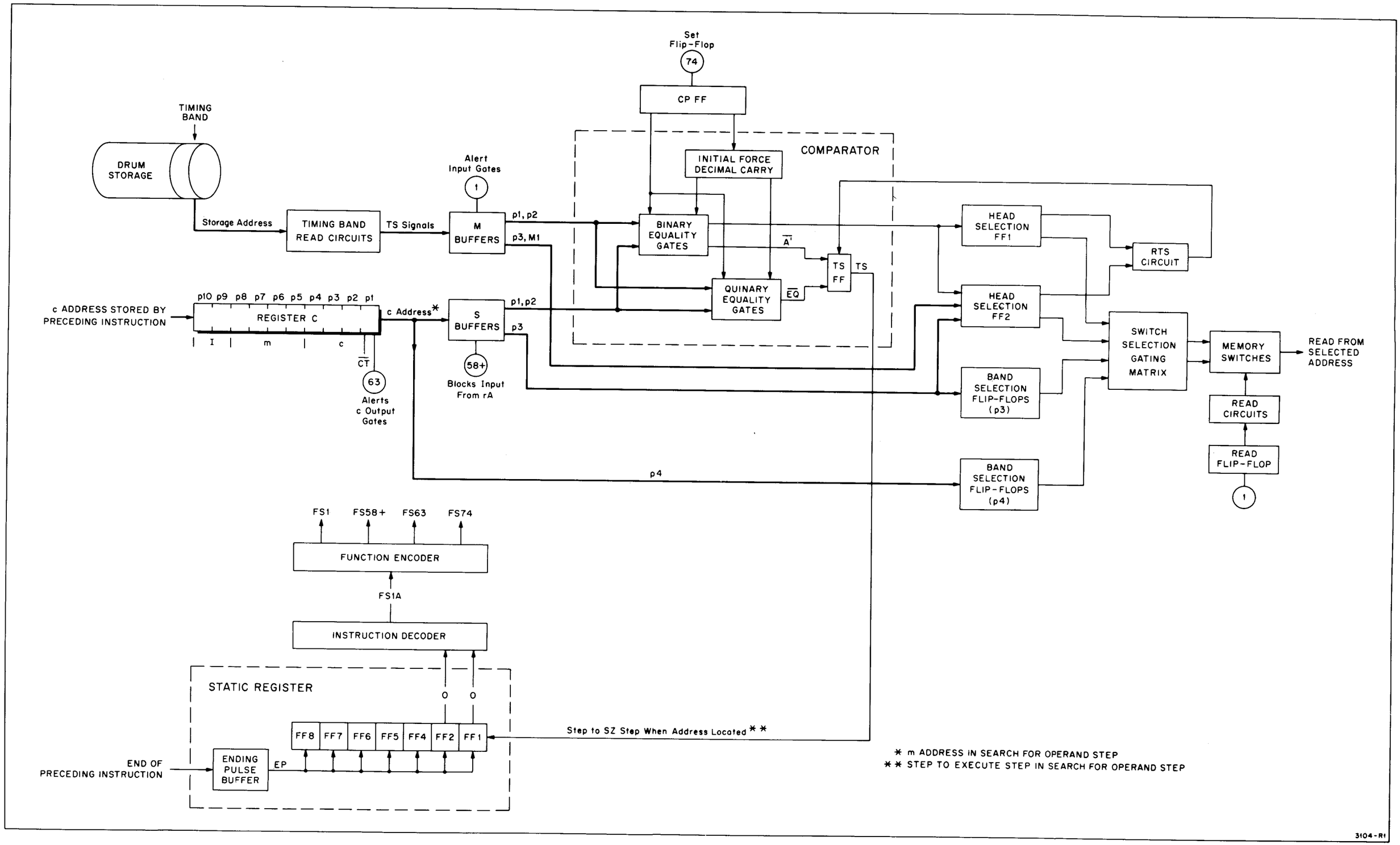
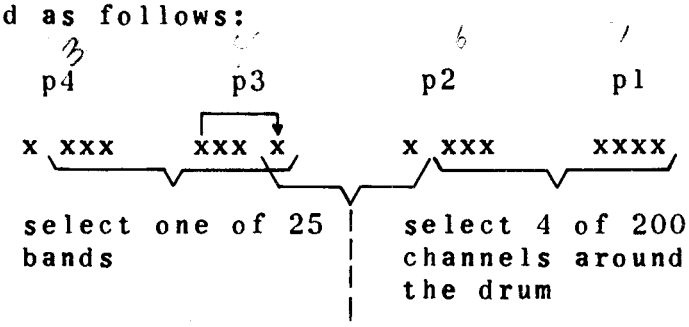


Figure 4-1. Search Step of Basic Operation Cycle

selected since there is only one head per track. In a search for an address, the bits of the four c-address digits stored in rC are used as follows:



Because there are four heads spaced at 90-degree intervals around the drum in fast-access storage, it is necessary to theoretically divide the surface or circumference of the drum into quadrants. It is necessary to refer to quadrants in normal access because both types of access storage use the same circuits. One of the four fast-access heads must be energized to read or write at the time the quadrant containing the desired storage address is approaching that head, minimizing the time required to read from or write onto the drum.

The p1 digit and the three lowest order bits of p2 partially represent the channel across the drum in which the correct address is found. If the complete address is 4469, p1 represents the 9 digit. However, the three lowest order bits of p2 do not fully represent the 6 digit; they merely show that the digit is either 1 or 6. Since addresses 000 through 199 are found within a band, the word can be in any one of channels 019, 069, 119, or 169. These four possible combinations for the time selection bits are shown in figure 4-2. The most significant bit (MSB) of p2 and the MSB and least significant bit (LSB) of p3 choose one of the quadrants, completing the selection of a channel and also selecting the head to be energized for reading. The remaining bits of digit p3 and the three lowest order bits of digit p4 select the proper band.

Digit p2 of 4469 is 6, or 1001 in biquinary code. The three lowest order bits, 001, are common to both 1 and 6 in biquinary code. Therefore if the MSB of p2 is a 0, the address is either 019, or 119; if it is a 1, the address is either 069 or 169. In address 4469 the MSB of p2 is 1; therefore the address is in either quadrant 01 or 11 (addresses 169 or 069) as shown in figure 4-2.

Address 069 has an even hundreds digit; address 169 has an odd hundreds digit. The least significant bit of p3 designates one of the two quadrants selected by the MSB of p2. Selection is accomplished by combining the LSB of p3 with the MSB of p3 to ascertain the evenness or oddness of p3.

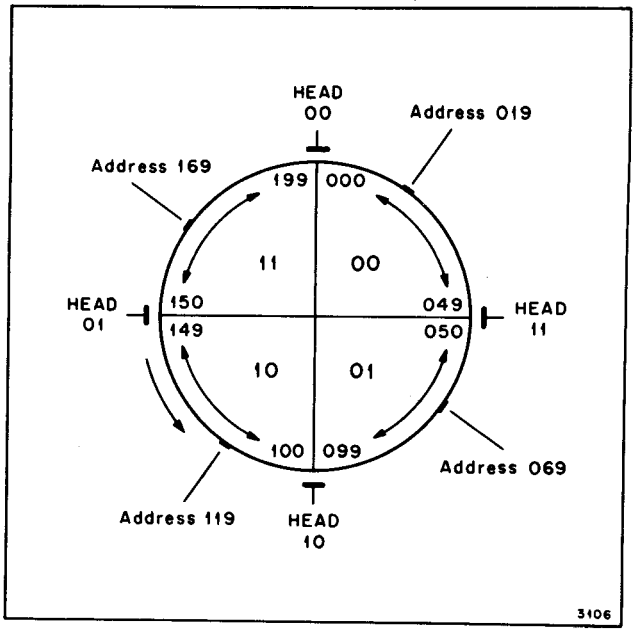


Figure 4-2. Drum Quadrants

This combination of the MSB and LSB of p3 is necessary because the least significant bits of the biquinary code do not form a pattern by which the oddness or evenness of a digit can be determined. The first column of table 4-1 shows that 0, the LSB of p3, if taken alone could indicate either an odd or even decimal digit. The last column shows that combining the LSB and MSB of each digit forms a pattern. When the combined bits equal 0, the digit is even; when they equal 1, the digit is odd.

In the 4469 address, digit p3 is 4, or 0100, which is an even-digit combination (0). Therefore digit p3 signifies that the address is contained in a location having an even hundreds digit, such as 069, 269, 469, 669, or 869. The MSB of p2 already has designated either the 169 or 069 channel. The p3 digit, being even, specifies the 069 channel and therefore quadrant 01.

The MSB of p2 and the LSB of p3, both of which determined the correct quadrant, also select one of the four heads in a fast-access band. With the 000 address in a band under the 00 head, the four quadrants and four heads are as shown in figure 4-2. To determine the head to be energized, the MSB of p2 and the LSB of p3 from rC and the timing combination from storage are quarter added. Table 4-2 lists the possible combinations of these bits. The four conditions shown under table 4-2a refer to the drum position in figure 4-3a; that is, quadrant 00 is under head 00. The conditions under table 4-2b refer to the possible conditions when quadrant 01 is approaching head 00. Similarly, table 4-2c and

Table 4-1. Oddness and Evenness of Biquinary Combinations

	Biquinary Code MSB LSB	Decimal Equivalent	Even or Odd[a] MSB LSB
	0 0 0 0	0	0 and 0 = 0
	0 0 0 1	1	0 and 1 = 1
	0 0 1 0	2	0 and 0 = 0
	0 0 1 1	3	0 and 1 = 1
p3 →	0 1 0 0	4	0 and 0 = 0
	1 0 0 0	5	1 and 0 = 1
	1 0 0 1	6	1 and 1 = 0
	1 0 1 0	7	1 and 0 = 1
	1 0 1 1	8	1 and 1 = 0
	1 1 0 0	9	1 and 0 = 1

[a] 0 = even; 1 = odd

Table 4-2. Head Selection

Timing Band Combinations p3 M1 p2 M4	c Address p3 S1 S4 p2 S4	Head Selected	Table Section
0 0	0 0	00	a
0 0	0 1	11	
0 0	1 0	10	
0 0	1 1	01	
0 1	0 0	01	b
0 1	0 1	00	
0 1	1 0	11	
0 1	1 1	10	
1 0	0 0	10	c
1 0	0 1	01	
1 0	1 0	00	
1 0	1 1	11	
1 1	0 0	11	d
1 1	0 1	10	
1 1	1 0	01	
1 1	1 1	00	

figure 4-3c show the possible conditions when quadrant 10 is approaching head 00; table 4-2d shows the possible conditions when quadrant 11 is approaching head 00.

The cutaway view of the drum in figure 4-3a shows the conditions specified in table 4-2a. It must be remembered that the quadrant called for in the c address is represented by the two quadrant selection bits of rC; that is, the MSB of p2 and the LSB of p3. If the 00 quadrant is under the 00 head, as in all four cases of table 4-2a, and the 00 quadrant is called for by rC, combination of the two quadrants results in selection of the 00 head. If the desired address is X in quadrant 00, the 00 head must be selected as the drum rotates in a counterclockwise direction. If the drum quadrants are in the same position and quadrant 11 is specified in the c address, the 01 head must be selected.

With any of the other three quadrants under the 00 head, as in figure 4-3a, 4-3b and 4-3c, head selection again depends on the quadrant to be read. For example, in figure 4-3c, the 10 quadrant is under the 00 head. Therefore, if the 11 quadrant is to be read, the 11 head, which is most immediately in the path of counterclockwise rotation of the drum and quadrant 11, is selected. The same conditions in table 4-2c (last line) verify the head selected in figure 4-3c.

Thus far, digits p1, p2, and part of p3 have selected the proper storage channel, the quadrant containing the address, and one of four heads to be energized in reading that address. Digit p3 and the three LSB's of p4 determine which of five fast-access bands contain the address. Digit p3 determines the third digit, the hundreds digit, of the address; the three lowest order bits of p4 determine the fourth, or thousands digit of the address. A detailed explanation of the memory search process is given in the following section.

4-5. COMPARISON AND HEAD SELECTION. The comparison operation (figure 4-1) begins with the comparison of the timing band channel addresses with the address contained in rC. As shown in the figure, the timing band signals enter the comparator on the M lines from the M buffers; the c-address signals from rC enter on the S lines from the S buffers. (Figure 4-1 and the logical diagrams in appendix A are pertinent throughout this description.)

Function signal 63 alerts the c-address output gates of rC. The gates are made permissive by the $\overline{CT}$ signal from the conditional transfer flip-flop (CT FF). The CT FF is restored to $\overline{CT}$ by the RCT outputs of the static register at the end of every search operation. Digits p1, p2, and p3 of the c address in rC are transferred, through the permissive output gates, to the S buffers. The p4 digit goes directly from rC to the band-selection flip-flops. The output signals of the four output gates of rC (figure A1) are C12, C22, C32, and C42. The c address from rC can enter the S buffers and the S lines because FS 58+ has blocked the outputs of rA which normally enter the S buffers. The p1 and p2 digits of the c address are transferred on the S lines into the quinary and binary equality gates of the comparator.

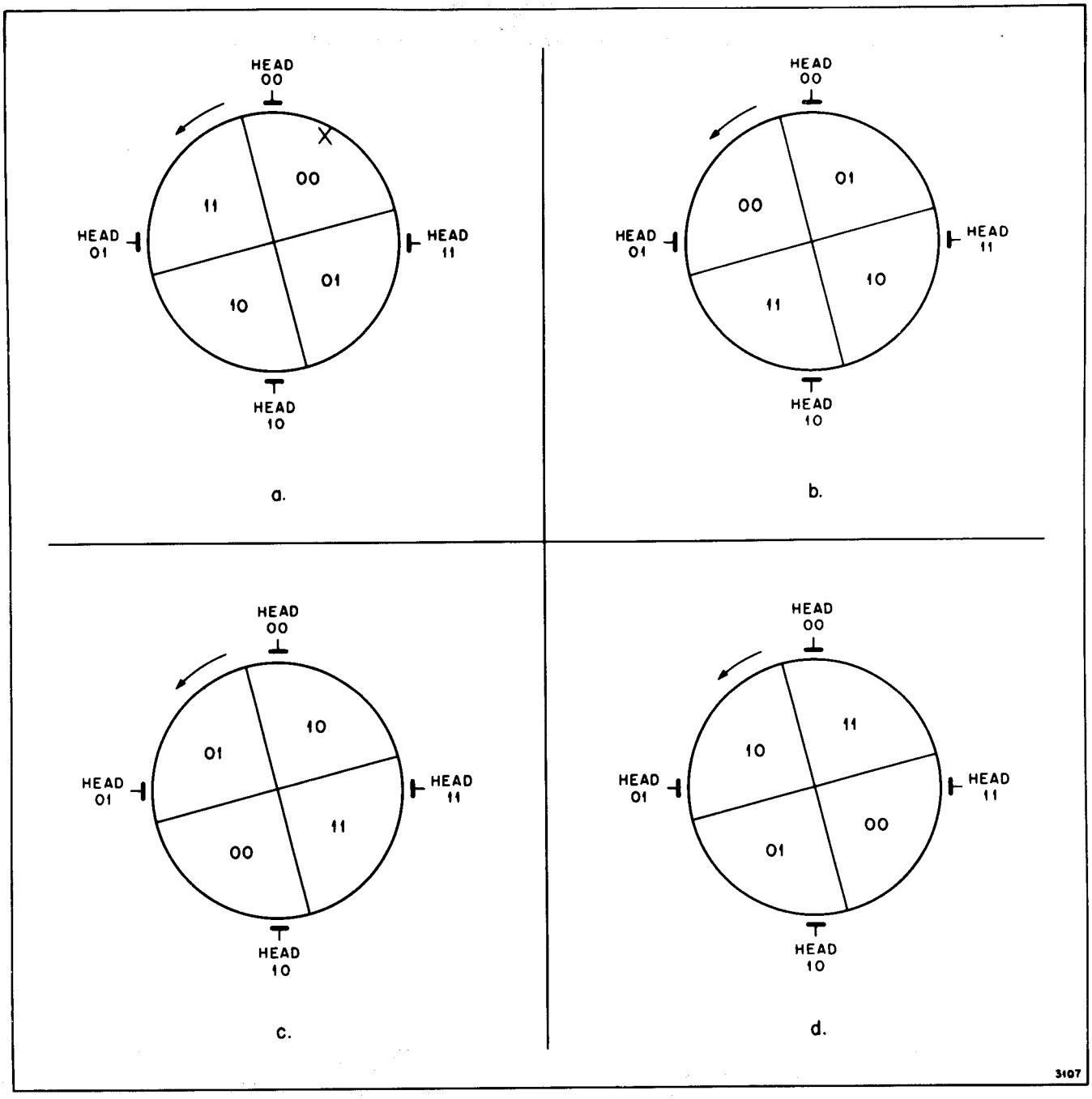


Figure 4-3. Drum Quadrants under Fast-Access Heads

Function signal 1 alerts the input gates of the M buffers from t0 to t2B. The timing band combinations signals TS1 through TS4 from the timing-band read circuit enter the M buffers and the M lines.

Function signal 74 sets the complement flip-flop of the sign-and-control circuit to produce a complement (CP) signal for the comparison operation. The CP signal alerts the binary and quinary equality gates of the comparator. Function signal 74 also generates a CP5 signal from the CP FF for use in the comparison operation. The CP5 signal drives the initial force-decimal-carry circuit which generates the A and C decimal-carry signals. These signals alert the quinary equality gates and binary carry gates of the computer.

The p1 digits from rC and storage arrive on the M and S lines at time t1B. The quinary bits of p1 (M1, M2, M3, and S1, S2, S3) are compared in the quinary equality gates of the comparator. Equality between the three M bits and the three S bits makes one of the eight gates permissive and causes a high output from one of the quinary equality gates. The high output goes to a noncomplementing amplifier which produces a high $\overline{EQ}$ output at t2B.

Before the comparison operation at t11B of the previous word time the time selection flip-flop (TS FF) (figure 4-1) was set. The set state of the TS FF indicates equality of the M and S bits. Inequality of the M and S bits restores the TS FF, indicating that the timing-band address under the TS head at that instant does not match the c address in rC. At various times the TS output is sampled to see whether a match has been obtained. Restoring the TS FF causes another search cycle to be initiated at the time TS is sampled. If the flip-flop remains set, it indicates equality of the timing address bits with the c-address bits. The TS FF input gate 21 (figure A12) restores the flip-flop to $\overline{TS}$ only when $\overline{EQ}$ is low at time t2B or t3B. The $\overline{EQ}$ output is low only when the quinary bits are unequal, resulting in a low output from the quinary equality gates. The high $\overline{EQ}$ signal blocks input gate 21 to keep the TS FF set.

The binary bits of p1 also are compared in the binary equality gates of the comparator at the same time (t1B) as the quinary bits are compared. Equality of bits M4 and S4 in the gates alerted by CP produces a high output signal which is buffed into a noncomplementing

amplifier to generate a high $\overline{A'}$ at t2B. This indication of equal binary bits goes to gate 20, an input gate of the TS FF. The high $\overline{A'}$ signal blocks the gate and the TS FF remains set.

Inequality of M4 and S4 causes the binary equality circuit to produce a low output to the noncomplementing amplifiers. The output of the amplifiers is a low $\overline{A'}$ signal. Input gate 20 of the TS FF is permissive to low signals at time t2B, and the low $\overline{A'}$ signal restores the TS FF to indicate inequality.

At time t2B, the quinary bits of digit p2 are compared for equality in the quinary equality gates. The comparison is accomplished in the same manner as for the quinary bits of p1. The high $\overline{EQ}$ signal, indicating equality of the quinary bits of p2, occurs at t3B and keeps the TS FF set.

The binary bits of digit p2, M4 and S4, are compared in the binary equality gates which are alerted by the low $\overline{CP}$ signal at t2B. Equality of the bits produces a high $\overline{A'}$ signal. The most significant bit of p2 indicates whether the desired address is above or below 50; it therefore contributes to head selection.

The high $\overline{A'}$ signal goes to the head selection 1 flip-flop (HS1 FF) of the memory selection circuit (figure A18). The signal blocks gate 33 of the HS1 FF, keeping the flip-flop restored to a low $\overline{HS1}$ output. The low $\overline{HS1}$ output indicates a 0 in the $\overline{LSB}$ of the quadrant address: either 00 or 10. If the $\overline{A'}$ signal on gate 33 is low at time St3B, the gate operates to set the flip-flop to a low HS1 output. The HS1 signal indicates a 1 in the LSB of the quadrant address: either 01 or 11. The HS1 FF output goes to the switch-selection gating matrix.

Also at St3B, the input gates of the HS2 FF sample the conditions which affect the selection of the MSB of the quadrant address. The output of the HS2 FF is the MSB of the two-digit head address shown in table 4-2.

All of the input gates of HS2 FF logically quarter add their inputs. For example, gate 37E of the flip-flop is permissive only to low signals $\overline{S4}$, S1, M1, and $\overline{A}$ (figure 4-4). The $\overline{S4}$ and S1 signals are the MSB and LSB

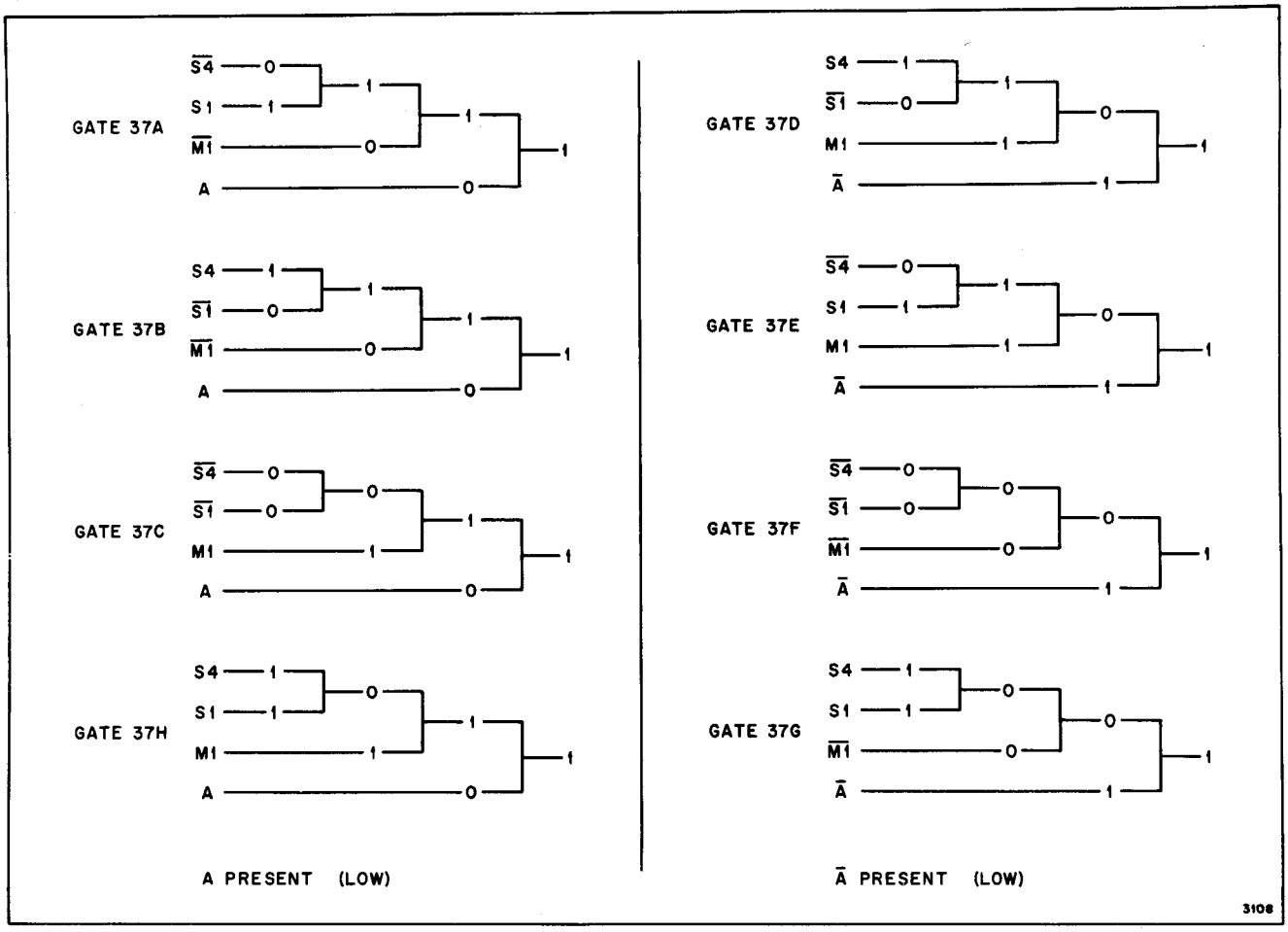


Figure 4-4. Quarter Addition of HS2 FF Inputs

of the p3 digit. Quarter addition of these two bits produces a 1. The M1 signal indicates a 1 bit, and it is quarter added to the result of the quarter addition of $\overline{S4}$ and S1 bits. Quarter addition of a 1 bit ($\overline{S4}$, S1) to a 1 bit (M1) again produces a 0 bit. The $\bar{A}$ signal, which has a value of 1, is quarter added to the previous bit result to produce a final result of 1. As a result, the HS2 FF is set to an HS2 output to select a quadrant address with an MSB of 1. If either bit of the quadrant address selected by the head selection flip-flops is a 1, the fast-access bands are involved. If the 00 quadrant is selected, normal-access bands may be involved.

The low $\bar{A}$ signal has a value of 1 when the p2 digit from the timing band is less than 5 and the p2 digit of rC is 5 or larger. The low A signal has a value of 0 under all conditions except those associated with the $\bar{A}$ signal. Gates 28, 29 and 31 of the comparator (figure A12) determine from comparison of the MSB's of p2 whether the A or the $\bar{A}$ signal is low. If one of the inputs to each one of these gates is high, the $\bar{A}$ signal is low. This can occur only when the M4 bit is

a 0 and the S4 bit is a 1. If this condition is not present, one of the gates is permissive to the low inputs, generating a low A signal. The low A signal is present when the MSB of the timing-band p2 digit is equal to the MSB of the rC p2 digit or if the MSB of the timing-band p2 digit is a 1 and the MSB of the rC p2 digit is a 0.

The conditions necessary to set the HS2 FF to an HS2 output (1) are shown in figure 4-4. If none of the eight gates is permissive, the flip-flop is restored to an $\overline{HS2}$ output (0). The outputs of the HS1 and HS2 FF's go to the memory switch selection matrix together with the outputs of the band-selection flip-flops.

If the quadrant address selected by the outputs of HS1 FF and HS2 FF is 10, 01, or 11, the input gate which produced the 1 output (a high output) also causes a high signal to go to amplifier 39 to generate a low RTS signal. The low RTS signal goes to gate 22 of the TS FF (figure A12).

The signals which make gate 22 permissive are low $\overline{S3}$ and $\overline{S4}$ which indicate 0 bits in the S3 and S4 bit positions of p4. When S3 and S4 are 0, addresses 0000 through 3999 (normal access) are involved; when S3 is 1, addresses 4000 through 4999 (fast access) are involved.

If either of the head selection flip-flops has, by generating RTS, indicated a fast-access head and the low $\overline{S3}$ and $\overline{S4}$ bits indicate a normal-access location, gate 22 (figure A18) restores the TS FF. When the HS1 and HS2 flip-flops select a 00 head, the RTS signal is high. The high RTS signal blocks gate 22, keeping the TS FF set so that the selected head can be energized to read or write.

When the search operation is unsuccessful, a high TS signal is generated by the restored TS FF and sent to input gate 7 of static register flip-flop 1 (STR FF1). The high input blocks the gate to keep the flip-flop set to a 0 bit. The flip-flop cannot be stepped to a 1 bit output until the TS input is low at t5B or t10B.

During instructions H, X, and J, which involve writing on the drum because they are transfer-to-storage instructions, the TS signal is sampled at gate 8 of static-register flip-flop 1. A low TS signal indicates that the timing band combination matches that of the c or m address in rC.

4-6. BAND SELECTION. The final step in locating an address is the selection of the band specified by the p3 and p4 digits in rC. The correct band is selected by digit p3 and the three lowest-order bits of p4. These

seven bits indicate the hundreds and thousands digits of the address and whether the address is in fast- or normal-access storage.

The band is selected by the band selection flip-flops. See figures 4-1 and A18. The operation of these flip-flops is explained in detail in section 3-97. The input gates of the band selection p3 and p4 flip-flops are alerted at St3B, the same time as the quadrant selection flip-flops are alerted. At this time, the three highest-order bits of the p3 digit from rC are on the S lines. The S inputs to the p3 flip-flops generate MS signals which indicate one of five possible band addresses specified by the hundreds digit of the address. Digit p3 specifies one of the following band addresses: 000 through 199, 200 through 399, 400 through 599, 600 through 799, 800 through 999. The head selection circuits determine, at the same time, a specific quadrant of such a band address.

The band selection p4 flip-flops sample the two lowest-order bits of digit p4 to determine the thousands digit of the address. At time St3B, direct outputs of rC are sampled by the MS10 and MS20 flip-flops. The C signals are sent directly to the flip-flops without being delayed at the S buffers so that all of the band and head selection operations are initiated at time St3B.

The fast/normal flip-flop determines whether the desired address is in fast- or normal-access storage. At St3B, the third lowest-order bit of digit p4 is sampled by the input gates of the flip-flop. The C33 and C34 signals from rC indicate whether the desired address is in normal-access locations 0000 to 3999 or fast-access locations 4000 to 4999. For normal-access selection the flip-flop generates the NM signal; for fast-access selection the flip-flop generates the FM signal. These signals go to the switch selection matrix and to the read-write circuits to control reading and writing by fast- or normal-access heads.

The outputs from all the band selection and head selection circuits appear at the switch selection matrix at t4B. The clear band selection circuit, which is explained in detail in section 3-98, clears all of the band selection flip-flops and also the head selection flip-flops if the p1 and p2 digits are found to be unequal.

If the search operation has located the correct address, as indicated by a low TS signal, FS1 makes gate 42A (figure A19) of the read flip-flop permissive at t8B. The permissive gate sets the flip-flop, the output of which goes to gates 45A and 45B. One of these gates is made permissive at t9B by the FM or NM signal from the fast/normal selection flip-flop (figure A18). If

gate 45B is made permissive, the low RGF signal alerts the fast-access read output gates (figure A20) so that the instruction word in the specified fast-access storage location can be read from the drum onto the DM lines. If gate 45A is made permissive, a low signal (figure A19) alerts the normal-access read-output gates so that the instruction word can be read from normal-access storage onto the DM' lines. The instruction word thus is read from storage to be stored in the static register and rC, during the staticize step. (See section 6-75 for a discussion of read circuits in detail.)

Sections 3-100 and 3-101 explain switch selection and the operation of the memory switch circuits.

4-7. STATICIZE-INSTRUCTION STEP

The primary function of the staticize step (figure 4-5) is to store the two instruction digits of the instruction word so that they can control the execution of the instruction. Other functions of the staticize step (SZ) are to store the entire ten digits of the instruction word in rC and to store the p7 digit of the instruction word in the multiplier/quotient counter (MQC). The word stored in rC, in addition to containing the two instruction digits, contains the storage address of the operand to be used in the instruction (m address) and the address of the next instruction word (c address). The p7 digit of the instruction word specifies the number of shifts necessary in a shift instruction and the number of the output stacker to be selected in the card reader in a select stacker instruction. It is stored in the MQC on every instruction so that no special preparation is necessary if a shift instruction is called for by the program.

At t10B of the search step, the output of the TS FF is sampled to make certain that the search step was successful. If the search was successful, the TS signal is low at gate 7 of STR FF1 (figure A2). Function signal 1 alerts this gate which also samples the $\overline{OF}$ output of the overflow FF at t10B of the search step. Because the conditions necessary to generate a high $\overline{OF}$ signal are explained in section 3-72, it is sufficient to say here that the low $\overline{OF}$ signal indicates that no abnormal conditions are present. When gate 7 is permissive to these signals, it sets FF 1 to a low STR1 output, which indicates a 1 bit, and generates a high RCT1 signal which restores the CT FF (figure A12).

Every staticize step causes the CT FF to be restored to $\overline{CT}$. This condition causes the c address to be read unless at a later time the CT FF is set to CT. As a result, an instruction which requires an operand sets the CT FF at the end of the staticize step; otherwise the next search is for the c address.

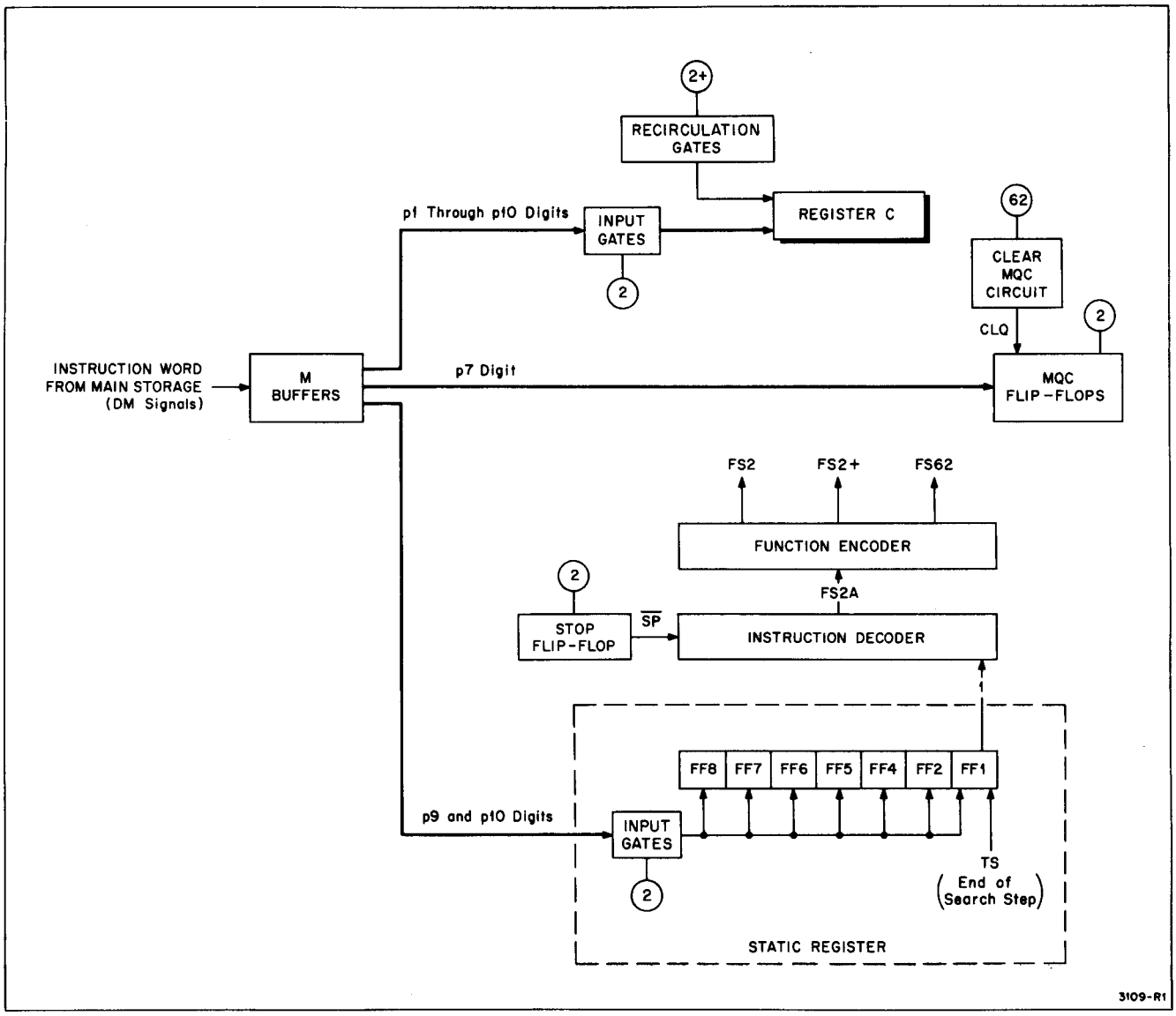


Figure 4-5. Staticize Step

When FF1 is set to a 1 output (figure 4-5), the input to the instruction decoder is 0000 0X01, since only that flip-flop has changed. The decoder converts this combination into FS 2A, which drives the function encoder to generate function signals 2, 2+, and 62. These signals control the functions of the staticize step.

4-8. STORING THE p7 DIGIT. Before storing the p7 digit in the four flip-flops of the MQC, the flip-flops must be cleared of previous information. At t0B of the staticize step, FS 62 at gate 19 of the clear-MQC circuit (figures 4-5 and A14) generates the CLQ signal. The CLQ signal restores the four flip-flops to 0 at gates 5, 6, 7, 8.

Function signal 2 alerts the input gates of the flip-flops at t7B, the time interval during which digit p7 is on the M lines. The four bits of digit p7 enter the flip-flops to be stored for future use if the staticized instruction is a shift or select stacker instruction.

4-9. STORING THE INSTRUCTION WORD. At t0A of the staticize step, the p0 digit of the instruction word from memory is present on the DM or DM' lines of the read-output circuits (figures A19 and A20). These signals go directly to the M buffer and are on the M lines at t0B. Function signal 2+ blocks the recirculation gates of the four subregisters of rC, clearing the register. Thus, at t0B of the staticize step, the p0 digit of the instruction word enters the permissive input gates of rC. Function signal 2 alerts the input gates to the digits of the instruction word on the M lines.

4-10. STATICIZING THE INSTRUCTION. Once they have performed their functions, the function signals generated by the staticize step must be removed. At t8B of the staticize step, FS 2 is low at gate 114 of the static register (figure A2). This restores STR FF1 to a 0 output, which causes the function signals of the staticize step to be lost at t11B.

At t9B the p9 digit of the instruction word is present on the M lines as shown in figure 4-5. Function signal 2 alerts the input gates of FF1, FF2, and FF4 at t9B so that the p9 digit can enter. (Only three bits of the p9 digit are of use in the processor.) To make certain that no function signals are generated in the one pulse time between the time digit p9 is staticized (t9B) and digit p10 is staticized (t10B), the high $\overline{SP}$ signal blocks the instruction decoder for one pulse time. At t9B, function signal 2 sets the stop flip-flop; gate 20 of the stop flip-flop generates a high $\overline{SP}$ signal (figure A5). The high $\overline{SP}$ signal blocks the instruction decoder.

At t10B, the p10 digit is present on the M lines. Function signal 2 also alerts the input gates of flip-flop 5, flip-flop 6, flip-flop 7 and flip-flop 8 at t10B so that the p10 digit can enter. By t11B the two instruction digits are completely staticized in the static register. Function signals required to execute the staticized instruction are available from the instruction decoder at t0A, and from the function encoder at t0B.

4-11. SEARCH-FOR-OPERAND STEP

In the search for an operand step, the storage address designated by the m address of the instruction word is searched for in the same manner as in the search-for-instruction step. When located, the operand is read from storage in time to be used in the execution step of the instruction. In some instructions, the m address does not contain an operand. It may instead contain one of the following: a location to which information must be transferred, the number of shifts in a shift instruction, a stacker number in a select stacker instruction, or the number of lines to be advanced in the print instruction.

The search-for-operand step is not required for all instructions. It is necessary only in instructions which require one of the following: an operand from main storage, a storage location or band to be read from or written onto, or the number of lines to advance paper. The arithmetic instructions require an operand as do the instructions which transfer information from or to main storage.

4-12. INSTRUCTION CODE CHARACTERISTICS. Instructions requiring operands can be identified by their instruction code. When the LSD (digit p9) of a staticized instruction is a decimal 0, 1, 5 or 6, a search for operand step is necessary. The two lowest-order bits, 00 for decimals 0 and 5, 01 for decimals 1 and 6, indicate to the control unit that the storage location designated by the m address of the instruction word in rC either contains an operand or is the location into which information is to be transferred. The least-significant digits of instructions which do not involve an operand or storage location are other than 0, 1, 5 or 6; therefore the two lowest-order bits of such instructions are not 00 or 01, but 10 or 11. Table 4-3 shows the characteristic codes of instructions requiring a search for operand step.

The search process required to locate an operand to be used for input-output instructions is explained along with the instructions in the input-output manuals. The input-output instructions involving a search for operand are those with an LSD of 1 or 6. The search process for processor instructions, those with an LSD of 0 or 5, is explained in the next paragraph.

4-13. LOCATING THE OPERAND. The search process required to locate an operand in storage is identical to the search-for-instruction process. Control of the operand search, however, differs from control of the instruction search. Figure 4-1 is also a block diagram of the search-for-operand step. Differences between the instruction search and operand search in the figure are indicated by the notes. In locating an instruction, the c address in rC is compared with the timing band addresses; in locating an operand, the m address in rC is compared with the timing band addresses.

Although FS 63 alerts both the m-address output gates and the c-address output gates of rC, the CT FF determines which address is to be read out and compared. When an instruction is staticized, the output of STR FF2 determines whether an operand is necessary. Table 4-3 shows that the STR2 position of the staticized instruction is always 0 when a search for operand is required.

The $\overline{\text{STR2}}$ output of the static register is sampled by gate 12 of the CT FF (figure A12) at t10B of the staticize step. If the $\overline{\text{STR2}}$ signal is low, indicating that a search must be made for the m address, the gate is permissive. When gate 12 is permissive the CT FF is set to CT, which controls readout of the m address from rC. When gate 12 is blocked by high signal $\overline{\text{STR2}}$, the CT FF is restored to $\overline{\text{CT}}$, which controls readout of the c address. The staticized instruction, however, has generated new function signals for executing the instruction so that the $\overline{\text{CT}}$ signal has no effect on rC until after the execution step.

The CT output of the CT FF is available at the m-address output gates of rC at t0B. The LSD of the m address, p5, goes from rC to the S buffers and the S lines and is available at the quinary and binary equality gates of the comparator (figure A12) at t1B. The comparison and memory selection processes for the search-for-operand step are the same as those of the search-for-instruction step (section 4-3).

The H, X, and J transfer instructions require a search-for-operand step, but the operand is a storage location into which information must be written. Because these three instructions entail writing in storage, time must be allowed for the write circuits to be prepared. For this reason, the H, X, and J instructions generate FS 3 for use in the search operation in addition to the normal search (Sc) function signals. Function signal 3 alerts gate 8 of STR FF1 to sample the TS signal at t5B. (In normal search, the TS signal is sampled three pulse times later, at t8B.) Sampling at t5B allows the write circuits to prepare for writing by the time the execute step begins. If the TS signal is low at t5B, the STR FF1 is set to a 1, initiating the execute step of the instruction stored in the static register.

4-14. EXECUTE-INSTRUCTION STEP

The execute-instruction step is initiated when the seven bits of the two instruction digits are staticized in the static register and either of the two lowest-order bits of the p9 digit is a 1 (search-for-operand step is unnecessary), or when the search for-operand step has been completed and the STR FF1 has been stepped to a 1 output. In both cases the combination of bits stored in the STR represents a specific instruction and can be decoded by the instruction decoder. The combination in the static register goes to the instruction decoder and function encoder to generate one or more function signals which execute the staticized instruction.

The Analysis of Instructions manual lists the function signals generated for each instruction and the purpose of each of these signals. Section 4-21, Arithmetic Operations, and the input-output manuals explain the details of the execution steps of typical instructions. The instructions not covered in detail in that section and the input-output manuals are treated in functional block diagram form in section V.

4-15. INSTRUCTIONS WITH TWO EXECUTION STEPS. Many instructions involve two execution steps. The add instruction (70), for example, adds two quantities in the first execution step and complements if necessary the sum of the addition in the second execution step. The function signals generated for the first step (A1) of the add instruction include FS 64. At t10B of the A1 step FS 64 at the stepping gate of the STR (figure A2) restores FF1 and FF2. Flip-flop 1 had been previously set to a 1 to accomplish the A1 step. Setting FF2 to a 1 output sets up the combination in the static register for step A2; as a result, a new set of function signals is generated to control the A2 step. The stepping gate similarly controls FF1 and FF2 during many other instructions.

Table 4-3 shows the code combinations for the steps of all instructions. The table is divided into instructions which require only one execution step and those which require more than one. It is subdivided further into instructions which require a search-for-operand step and those which do not. The third column, STR code, lists the code combinations for each step of each instruction after it has been staticized in the static register. The code positions marked by X are bits which are unnecessary to the staticize step. The X in the STR3 position of the LSD is included only to balance each combination with the eight bits of the biquinary code.

4-16. TIMING OF THE BASIC OPERATION CYCLE

The four steps of the basic operation cycle require a minimum of four word times to complete. Instructions requiring no search-for-operand step take only three word times. Instructions with more than one execution step require more than four word times. The timing of the basic operation cycle with and without a search-for-operand step is shown in figure 4-6. The timing of the various operations of the search-for-operand step is identical to that of the search-for-instruction step. Therefore the search-for-operand step shows only the timing of operations unique to it. Although many other operations occur during each word time, only the ones necessary to explain the timing of the whole cycle are included.

4-17. PROCESSING A TYPICAL INSTRUCTION

This section applies the principles of the basic operation cycle to the processing of a typical instruction, the H(60) instruction. In the discussion of the search-for-instruction step, the operation of the storage read circuits was explained. The storage write circuits can be explained with the H(60) instruction, which requires a transfer of information from a register to a storage location.

In the search-for-instruction step, the H(60) instruction is located in storage. In the staticize step the instruction word is stored in rC, and the two instruction digits, 60, are staticized in the static register. In the H instruction the contents of rA must then be transferred to a storage location. The address of that location is the operand in the instruction. The execution step of the H instruction controls the writing of the word from rA into the specified storage location on the drum.

Table 4-3. Instruction Code Combinations

Instruction	Biquinary Code	STR Code 8 7 6 5 4 3 2 1	Steps
INSTRUCTIONS WITH ONE EXECUTION STEP (SEARCH)			
05 (Y): (m) ⟶ rX	0 0 0 0 1 0 0 0	X X X X X X 0 0 0 0 0 0 1 X 0 1	Sc 00 Y 06
20 (P): Superimpose (m) and (rA) ⟶ rA	0 0 1 0 0 0 0 0	X X X X X X 0 0 0 X 1 0 0 X 0 1	Sc 00 P 21
25 (B): (m) ⟶ rA	0 0 1 0 1 0 0 0	X X X X X X 0 0 0 X 1 0 1 X 0 1	Sc 00 B 26
30 (L): (m) ⟶ rL	0 0 1 1 0 0 0 0	X X X X X X 0 0 0 X 1 1 0 X 0 1	Sc 00 L 31
35 (E): Logically multiply (m) and (rA) ⟶ rA	0 0 1 1 1 0 0 0	X X X X X X 0 0 0 X 1 1 1 X 0 1	Sc 00 E 36
50 (J): (rL) ⟶ m	1 0 0 0 0 0 0 0	1 0 0 0 0 X 0 0 1 0 0 0 0 X 0 1	J-Sc 50 J-Ex 51
60 (H): (rA) ⟶ m	1 0 0 1 0 0 0 0	1 X 0 1 X X 0 0 1 X 0 1 0 X 0 1	H-Sc 60 H-Ex 61
65 (X): (rX) ⟶ m	1 0 0 1 1 0 0 0	1 X 0 1 X X 0 0 1 X 0 1 1 X 0 1	X-Sc 65 X-Ex 66
INSTRUCTIONS WITH ONE EXECUTION STEP (NO SEARCH)			
12 (G): RR ⟶ UCT (rA) + (rX) ⟶ rA	0 0 0 1 0 0 1 0	0 X 0 1 0 X 1 0	G 12
17 (R): UCT ⟶ RR (rA) ⟶ rA + rX	0 0 0 1 1 0 1 0	0 X 0 1 1 X 1 0	R 17
47 (Z2): Select output stacker of fast reader	0 1 0 0 1 0 1 0	0 1 0 0 1 X 1 0	Z2 47
67 Stop	1 0 0 1 1 0 1 0	1 X 0 1 1 X 1 0	Stop 67
72 (CC): Feed one card (fast reader)	1 0 1 0 0 0 1 0	1 X 1 0 0 X 1 0	CC 72
77 (K): (rA) ⟶ rL	1 0 1 0 1 0 1 0	1 X 1 0 1 X 1 0	K 77

82 (Q): (rA) : (rL)
If (rA) = (rL), go to m
If (rA) ≠ (rL), go to c
	1 0 1 1 0 0 1 0	1 X 1 0 0 X 1 0	Q 82

Table 4-3. Instruction Code Combination (cont)

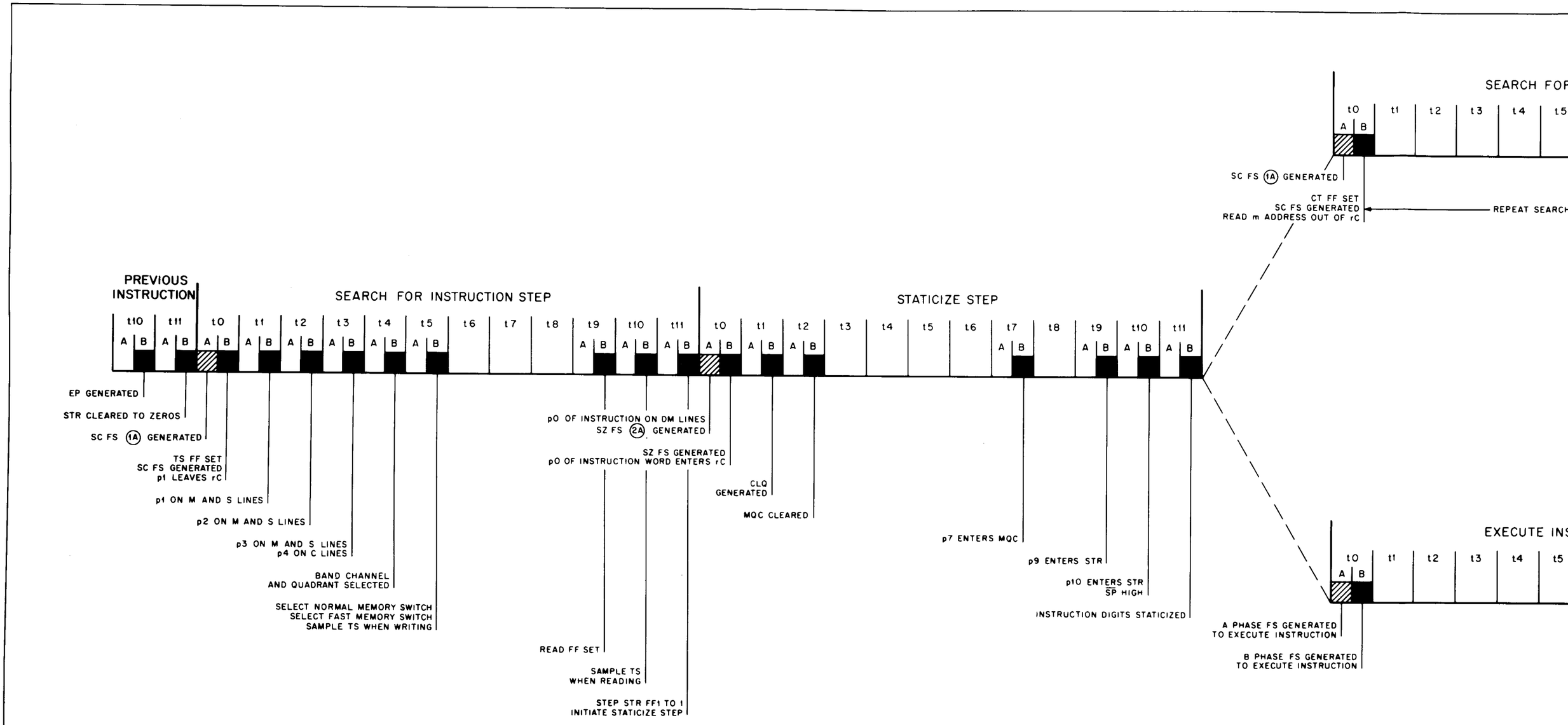
INSTRUCTIONS WITH ONE EXECUTION STEP (NO SEARCH) (cont)			

87 (T): (rA) : (rL)
If (rA) > (rL), go to m
If (rA) ≤ (rL), go to c
	1 0 1 1 1 0 1 0	1 X 1 1 1 X 1 0	T 87

INSTRUCTIONS WITH TWO OR MORE EXECUTION STEPS (SEARCH)			
55 (D): (m) ÷ (rL) ⟶ rA; remainder ⟶ rX	1 0 0 0 1 0 0 0	X X X X X X 0 0 1 0 0 0 1 X 0 1 1 0 0 0 1 X 1 1 1 0 0 1 1 X 1 1	Sc 00 D1 56 D2 58 D3 68
70 (A): (m) + (rA) ⟶ rA	1 0 1 0 0 0 0 0	X X X X X X 0 0 1 X 1 0 X X 0 1 1 X 1 0 X X 1 1	Sc 00 A1 71 A2 73
75 (S): (rA) - (m) ⟶ rA	1 0 1 0 1 0 0 0	X X X X X X 0 0 1 X 1 0 X X 0 1 1 X 1 0 X X 1 1	Sc 00 S1 76 S2 78
85 (M): (m) x (rL) ⟶ rA + rX	1 0 1 1 1 0 0 0	X X X X X X 0 0 1 X 1 1 1 X 0 1 1 X 1 1 1 X 1 1	Sc 00 M1 86 M2 88
INSTRUCTIONS WITH TWO OR MORE EXECUTION STEPS (NO SEARCH)			
11 (PR1): Storage ⟶ print buffer	0 0 0 1 0 0 0 1	0 X 0 1 X X 0 1 0 X 0 1 X X 1 1	PR1 11 PR2 13
16 (PF1): Paper advance	0 0 0 1 1 0 0 1	0 X 0 1 X X 0 1 0 X 0 1 X X 1 1	PF1 16 PF2 18
22 (I11): Test card buffer (read punch) If loaded, go to m If not loaded, go to c	0 0 1 0 0 0 1 0	0 X 1 0 0 X 1 0 0 X 1 0 X X 1 1	I11 22 I12 23
27 (I21): If printing or paper feeding, go to c If not printing or paper feeding, go to m; (rC) ⟶ rA	0 0 1 0 1 0 1 0	0 X 1 0 1 X 1 0 0 X 1 0 X X 1 1	I21 27 I12 28
32 (N): Right circular shift rA ⟶ rX; rX ⟶ rA n places	0 0 1 1 0 0 1 0	0 X 1 1 X X 1 0 0 X 1 1 0 X 1 1	N1 32 N2 33

Table 4-3. Instruction Code Combination (cont)

INSTRUCTIONS WITH TWO OR MORE EXECUTION STEPS (NO SEARCH) (cont)			
37 (V): Left shift (rA) n places Lose MSD; place 0 in LSD	0 0 1 1 1 0 1 0	0 X 1 1 X X 1 0 0 X 1 1 1 X 1 1	V1 37 V2 38
42 (I31): Test card buffer (fast reader) If loaded, go to m If not loaded, go to c	0 1 0 0 0 0 1 0	0 1 0 0 0 X 1 0 0 X 1 0 X X 1 1	I31 42 I12 23
46 (W11): Card buffer (read punch) ⟶ main storage	0 1 0 0 1 0 0 1	0 1 0 0 1 X 0 1 0 1 0 0 1 X 1 1	W11 46 W12 48
62 (ZS1): Zero suppress RR word in rA	1 0 0 1 0 0 1 0	1 X 0 1 0 X 1 0 1 X 0 1 0 X 1 1	ZS1 62 ZS2 63
81 (W21): Start read punch unit and main storage ⟶ card buffer (read punch)	1 0 1 1 0 0 0 1	1 X 1 1 0 X 0 1 1 X 1 1 0 X 1 1	W21 81 W22 83
96 (W31): Card buffer (fast reader) ⟶ main storage	1 1 0 0 1 0 0 1	1 1 0 0 1 X 0 1 1 1 0 0 1 X 1 1	W31 96 W32 98


PREVIOUS INSTRUCTION
SEARCH FOR INSTRUCTION STEP
STATICIZE STEP
t10 t11 t0 t1 t2 t3 t4 t5 t6 t7 t8 t9 t10 t11 t0 t1 t2 t3 t4 t5 t6 t7 t8 t9 t10 t11
A B
EP GENERATED
STR CLEARED TO ZEROS
SC FS (1A) GENERATED
TS FF SET
SC FS GENERATED
p1 LEAVES rC
p1 ON M AND S LINES
p2 ON M AND S LINES
p3 ON M AND S LINES
p4 ON C LINES
BAND CHANNEL
AND QUADRANT SELECTED
SELECT NORMAL MEMORY SWITCH
SELECT FAST MEMORY SWITCH
SAMPLE TS WHEN WRITING
pO OF INSTRUCTION ON DM LINES
SZ FS (2A) GENERATED
SZ FS GENERATED
pO OF INSTRUCTION WORD ENTERS rC
CLQ GENERATED
MQC CLEARED
READ FF SET
SAMPLE TS WHEN READING
STEP STR FF1 TO 1
INITIATE STATICIZE STEP
p7 ENTERS MQC
p9 ENTERS STR
p10 ENTERS STR
SP HIGH
INSTRUCTION DIGITS STATICIZED
SEARCH FOR
t0 t1 t2 t3 t4 t5
SC FS (1A) GENERATED
CT FF SET
SC FS GENERATED
READ m ADDRESS OUT OF rC
REPEAT SEARCH
EXECUTE INS
A PHASE FS GENERATED
TO EXECUTE INSTRUCTION
B PHASE FS GENERATED
TO EXECUTE INSTRUCTION

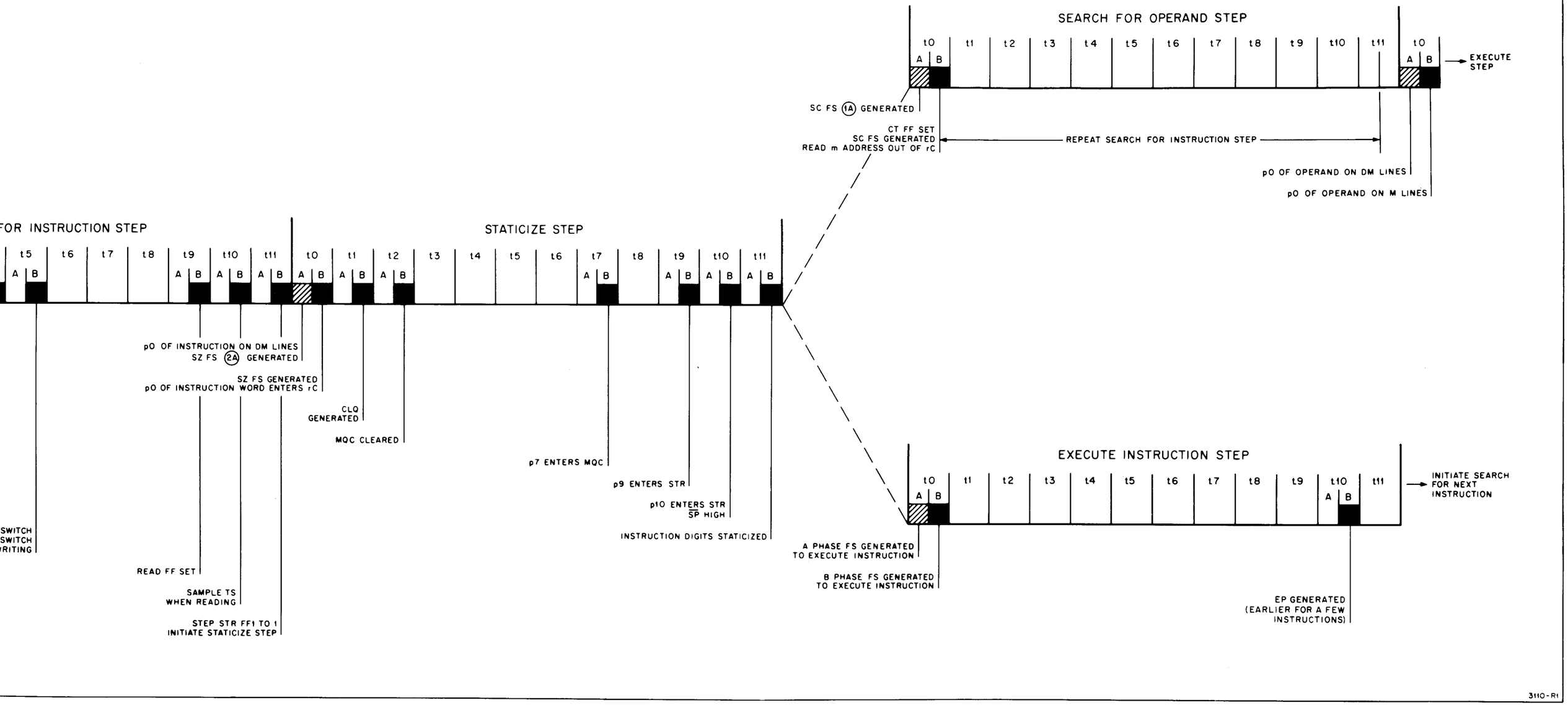


Figure 4-6. Timing of Basic Operation Cycle

4-18. SEARCH FOR OPERAND

The H(60) instruction is staticized in the static register flip-flops by the staticize step as 1001 0X00. The two lowest-order bits of the p9 digit are 0's, indicating a search. This combination is picked up by the H-X-J-Sc and Sc gate lines of the instruction decoder and generates FS 1A and FS 3A. (The search steps of the H, X, and J instruction require the same function signals; therefore, all are on a common instruction decoder gate line.)

Function signal 1A generates FS 58+, FS 74, FS 63 and FS 1. Function signal 58+ blocks readout from rA onto the S lines. Function signal 74 sets the CP FF to produce a CP signal. Function signal 63, in conjunction with the CT signal, causes readout of the m address from rC onto the S lines. Function signal 1 alerts the input gates of the M buffer to enable the timing band signals from the drum to enter the M lines.

The 1001 0X00 STR output combination also generates FS 3A (H-X-J Sc gate) which generates FS 3 to alert the STR FF1 stepping gate. At t5B of the search-for-operand step, the output of the TS FF is sampled by gate 8 of FF1. A low TS signal and FS 3 make gate 8 permissive and step FF1 from a 0 output to a 1 output. The new STR output combination of 1001 0X01 (61) is present at the instruction decoder at t6B.

At t6B, FS 3 sets the write FF (figure A19) at gate 5B to prepare the write circuits for the execute step of the instruction.

When gate 8 of STR FF1 is permissive at t6A, a high RCT2 signal is generated which goes to the input gates of the CT FF and to buffer 104 of the write circuits. The high RCT2 signal restores the CT FF, generating the low $\overline{CT}$ signal which controls readout of the c address from rC and generates the write pedestal (section 6-77). The new STR combination causes the function signals for search to end at t7A. The search-for-operand step has located the operand, which is the storage location designated by the m address.

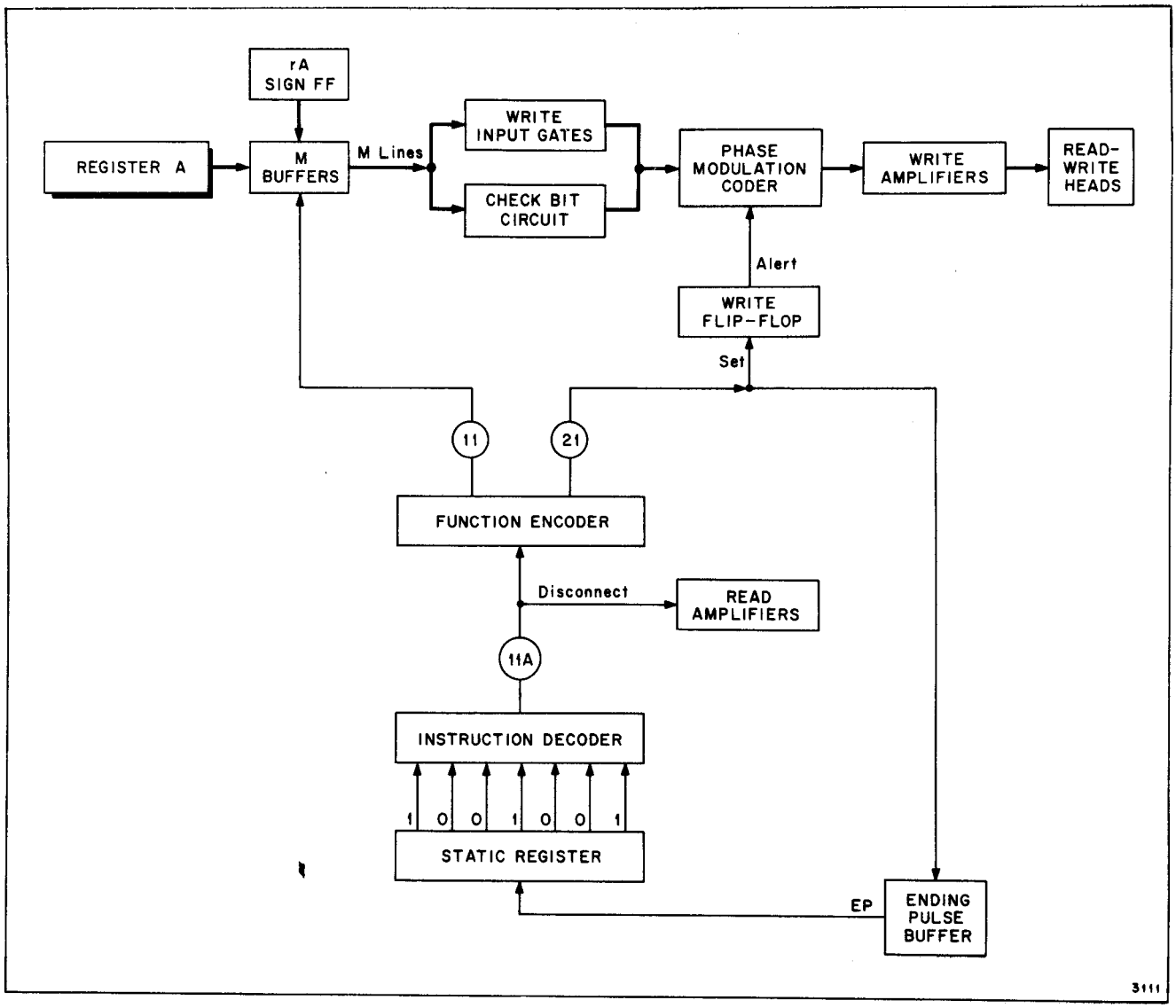


Figure 4-7. Execution Step of H (60) Instruction

4-19. EXECUTE THE H(60) INSTRUCTION

In the execute step of the H(60) instruction (figure 4-7), the contents of rA is recorded in the storage address located by the search-for-operand step. During the execution step, certain function signals are generated by the new combination in the static register. These signals control the transfer of the contents of rA onto the M lines and into the storage write circuits, the preparation of the write circuits to record on the drum, and eventually the ending of the instruction.

At t7A of the search step the H gate line of the instruction decoder generates FS 11A which generates FS 11 and FS 21. These signals control the writing of the contents of rA onto the drum.

Function signal 11 alerts input gates 7A, 7B, 7C, and 7D of the M buffers (figure A6). These gates are permissive to the four bits of the p0 digit (A1M, A2M, A3M, and A4M) from rA at t7B, and the contents of rA enters onto the M lines. Gate 6 of the M buffers, also alerted by FS 11, also is permissive at t7B to a low A- signal. This condition indicates that the sign of the contents of rA, which has been stored in the rA sign flip-flop, is minus. If the sign of rA is plus, low A- is absent from gate 06. The sign position of the word (t7B) on the A1M lines contains 0, indicating a plus sign. The word and its sign are sent from rA onto the M lines and into the write circuits (figures A19 and A20).

At t4B of the execute step FS 21 operates gate 19 of the static register to generate the EP and Reset-TS signals. Because the H, X, and J instructions involve writing on the drum and therefore require less time for execution than most instructions, the EP signal is generated early. The function signals for the instruction are lost at t7B. The TS FF is restored so that the set output of the flip-flop, TS, cannot set the read flip-flop. Normally, at t8B, the read flip-flop (figure A19) is set by FS 1, TS and $\overline{OF}$. All these signals will be present at t8B because the function signals for search will be available at t7B. To keep the read flip-flop restored until reading is required, the Reset-TS signal restores the TS FF, keeping the TS signal high. High TS blocks gate 42A of the read flip-flop, keeping it restored. The zero combination in the STR initiates a search for the next instruction.

4-20. MEMORY WRITE OPERATION

During a write operation, information and check bits are sent on the M lines to the phase-modulation coder where each input signal is coded into a phase-modulated pulse representation for recording. The resulting pulse is amplified in the write amplifier and drives the write heads.

At t7A, FS 11A electronically disconnects the read amplifiers from the write circuits by generating the write pedestal (section 6-77). Control signal RCT2, present for only one pulse time, has generated the write pedestal from t6A until t7A. For writing on the fast-access bands the IR output of the write-pedestal generator disconnects the read amplifiers of the fast-access heads.

The bits of each digit to be written are sent in parallel to the check-bit circuit and to the write input circuits. The check-bit circuit is explained in section 4-38. Each of the four bits of the digit to be written is delayed a pulse time by two complementing amplifiers before going to the input gates of the phase-modulation coder, so that the check bit and the information bits can be written simultaneously. Computing the check bit requires a full pulse time. At t9B the information bits and a check bit are present at the input gates to the phase-modulation coder. The write flip-flop output alerts the input gates at t8B and for a full word time thereafter. The operation of the phase-modulation coder is explained in section 3-92. The bits are converted into a phase-modulated waveshape which goes directly to the read-write heads and is written on the drum in the location specified by the m address.

4-21. ARITHMETIC OPERATIONS

4-22. ADDITION AND SUBTRACTION

4-23. ADD INSTRUCTION. The functions of the add instruction are: add algebraically the quantity in the storage location designated by m to the contents of rA, store the result in rA, compute the sign of the sum, and store the sign in the rA sign flip-flop. The quantity in storage is the addend; the quantity in rA is the augend.

The following preparations for addition have taken place before the A1 step:

(1) The search-for-instruction step has been completed.

(2) The add instruction (70) has been staticized.

(3) The staticized instruction has initiated a search for the operand (m address), which in this instruction is the addend.

(4) The augend has been stored in rA by a previous instruction and its sign has been stored in the A sign flip-flop.

The add instruction requires two execution steps, A1 and A2.

(1) A1 Step. In the first step of addition, A1, (figure 4-8a), the signs of the augend and addend are compared at the input gates of the complement flip-flop (CP FF). The gates determine from the two signs whether the augend is to be complemented (CP) or not complemented ($\overline{CP}$) before addition. This information controls the complementing circuit of the quinary adder. The sign of the augend is compared with the CP output of the complement flip-flop at the input gates of the rA sign flip-flop to determine the sign of the sum. Once determined, the sign of the sum is stored in the rA sign flip-flop. The augend in rA is sent on the S lines into the binary and quinary adders. The addend from the location designated by the m address is sent on the M lines into the binary and quinary adders. The adders add the two quantities digit by digit and transfer the sum on the 0 lines into rA.

The staticized digits of the A1 step (71) generate function signals 4, 50, 55+, 64, and 75 at t0B to execute the A1 step. Function signal 4 alerts the input gates of the CP FF. Gates 8 and 9 of the CP FF (section 3-71) operate during the add instruction to sample the signs of the two quantities. If the signs are unlike, one of the gates operates to set the CP FF to CP, which will cause the augend digits to be complemented. If the signs are alike, gates 8 and 9 are blocked, the flip-flop remains restored to $\overline{CP}$, and the augend is not complemented.

Function signal 55+ blocks the recirculation gates of rA, and the digits of the augend go to the S buffers and the S lines. Function signal 50 alerts the quinary and binary adder gates at t0B.

The quinary bits of the p1 digit of the addend (M1, M2, and M3) go to the input gates of the decimal carry adder (figure A11) and the quinary carry gates (figure A12). The input gates of the decimal carry adder sample the A and C signals from the binary and quinary circuits to determine whether a carry bit is to be added to the two digits being added. Because the p1 digits are the first to be added there can be no carry, and the A or $\overline{C}$ signal, or both, will be low. The outputs of the decimal carry adder go to the quinary adder. They represent the quinary bits of each digit of the addend.

The quinary bits of the p1 digit of the augend (S1, S2, and S3) go to the input gates of the complementing circuit (figure A11). If the CP (complement) signal alerts the

gates, the circuit produces the complement of the input bits. If the CP (no complement) signal alerts the gates, the quinary S bits pass through the circuit unchanged.

The quinary S bits and M bits also are sent in parallel to the quinary carry circuit. Any combination of quinary bits which indicates the need for quinary carry generates C and C' signals from the quinary carry circuit. The gates are blocked by combinations which require no quinary carry, generating the low $\overline{C}$ signal. The low C signal, if generated, is used in conjunction with the A signal to indicate a decimal carry into the addition of the next two digits. The low C' signal indicates the presence of quinary carry and causes a carry bit to be added in the addition of the binary bits in the binary adder.

The quinary outputs of the decimal carry adder and those of the complementing circuit are added in the quinary adder gates. One (or two) of the adder gates is permissive to the input combinations, producing a high $\underline{O}$ output signal.* A high $\underline{O}$ output signal indicates a 1 bit, a low $\underline{O}$ output signal indicates a 0 bit.

The binary bits of the two quantities are added in the binary adder (figure A12) at the same time as the quinary bits. Initially, the M4 and S4 binary bits are compared in the binary equality gates. The gates, alerted by $\overline{CP}$, sample the two binary bits during a normal addition. If either bit is a 1, a signal indicating the 1 bit goes to the binary carry circuit to generate a binary carry signal A, which will be used with the C signal, if present, in the addition of the next two digits. The carry circuit also sends the A' signal to gate 6 of the binary adder. If the $\overline{C}$ signal is low, gate 6 is permissive to the A' signal and the $\underline{O}42$ output is high, indicating a 1 bit in the MSB of the sum digit. No decimal carry will be generated if the $\overline{C}$ signal is low.

If the M4 and the S4 bits both have a value of 1, gate 30 of the force decimal carry circuit is permissive and the A and C signals are generated to force an indication of a decimal carry to the next addition.

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*Throughout the manual, $\underline{O}$ signifies the letter, as an abbreviation for output, not zero.

If the M4 and the S4 bits both have a value of 0, the binary equality gates are blocked, generating low signals $\underline{A}$ and $\underline{A}'$ which indicate no binary carry. The low $\underline{A}'$ signal goes to gate 7 of the binary adder which is permissive only if quinary carry is present, a condition indicated by the low C' signal. If the gate is permissive, the $\underline{0}41$ output is high, indicating a 1 in the MSB position of the sum digit. If quinary carry is absent, the C' signal is high blocking gate 7 and producing a low $\underline{0}41$ bit. A low $\underline{0}41$ output signal indicates a 0 in the MSB of the sum digit. The $\underline{0}$ signal outputs of the quinary adder and the binary adder are sent to the sum input buffers of rA. The sum digits are stored in rA during the A1 step.

If the sum of two quantities with unlike signs is zero, the sign of that sum must be forced to plus. The TS FF is used as a control circuit to indicate this condition to the rA sign flip-flop. Function signal 75 alerts restore gates 16 and 17 of the TS FF during the A1 step. If the signs of the two quantities being added are unlike, the CP FF is set to CP. The CP, A, and C signals are present during addition when the signs are unequal. These signals alert the quinary-equality gates, which compare for equality the digits being added in the adders. The CP signal alerts the binary-equality gates which also compare for equality. If the first nine digits of the quantities being added are equal, the TS FF remains set to TS. The TS signal goes to the rA sign flip-flop to force the sign of the sum to plus if the sum of the quantities is zero.

At t11B, FS 4 alerts the input gates of the rA sign flip-flop and the overflow flip-flop. Gates 3, 6, and 7 of the rA sign FF compute the sign of the sum (section 3-67) and store it in the flip-flop. During addition, the overflow flip-flop (OF FF) is set at gate 29 when the input signals indicate that the sum has exceeded the capacity of rA. When this possibility is expected, the programmer provides for it by programming a routine in the c+1 address, to be used only if overflow occurs. The set output of the OF FF, OF, sets the overflow delay flop to OF2+ during the next search-for-instruction step. The OF2+ signal keeps the TS FF set at buffer 82 to delay for one word time the reading of the selected instruction word address. This causes the c+1 address to be read instead of the c address.

Function signal 64 alerts the STR stepping gate at t10B of the A1 step. If the EP signal is low, the gate steps FF1 and FF2 to 1 outputs. At this point, however, FF1 is already generating a 1 bit output, so that, in effect, only FF2 is stepped. The new 11 reading in the lowest order STR bits is converted into function signals for the A2 step by the instruction decoder and function encoder. The function signals generated for the A2 step are 50, 55+ and 67.

(2) A2 Step. If the sum determined during A1 is the complement of the true sum, it must be complemented to its true form in the A2 step (figure 4-8). The sum determined during A1 and stored in rA reads out onto the S lines. Register A is cleared by FS 55+ to make room for the true sum which will be determined in the A2 step.

Function signal 50 alerts the gates of the binary and quinary adders. The sum on the S lines goes to the complementing circuit and the binary equality gates for complementing if necessary. If complementing is unnecessary (section 3-71), the $\overline{CP}$ signal is present and the sum merely passes through the complementing circuit. It also passes through the quinary and binary adders, as in the A1 step, and returns to rA. No addition takes place in the adders because there is no quantity on the M lines to be added. (In subtraction, however, a 1 is automatically added to the quantity from rA in the decimal carry adder.)

Function signal 67 operates gate 17 of the ending-pulse buffer circuit at t9B. At t10B the EP signal is generated to clear the static register of the add instruction and initiate a search for the next instruction.

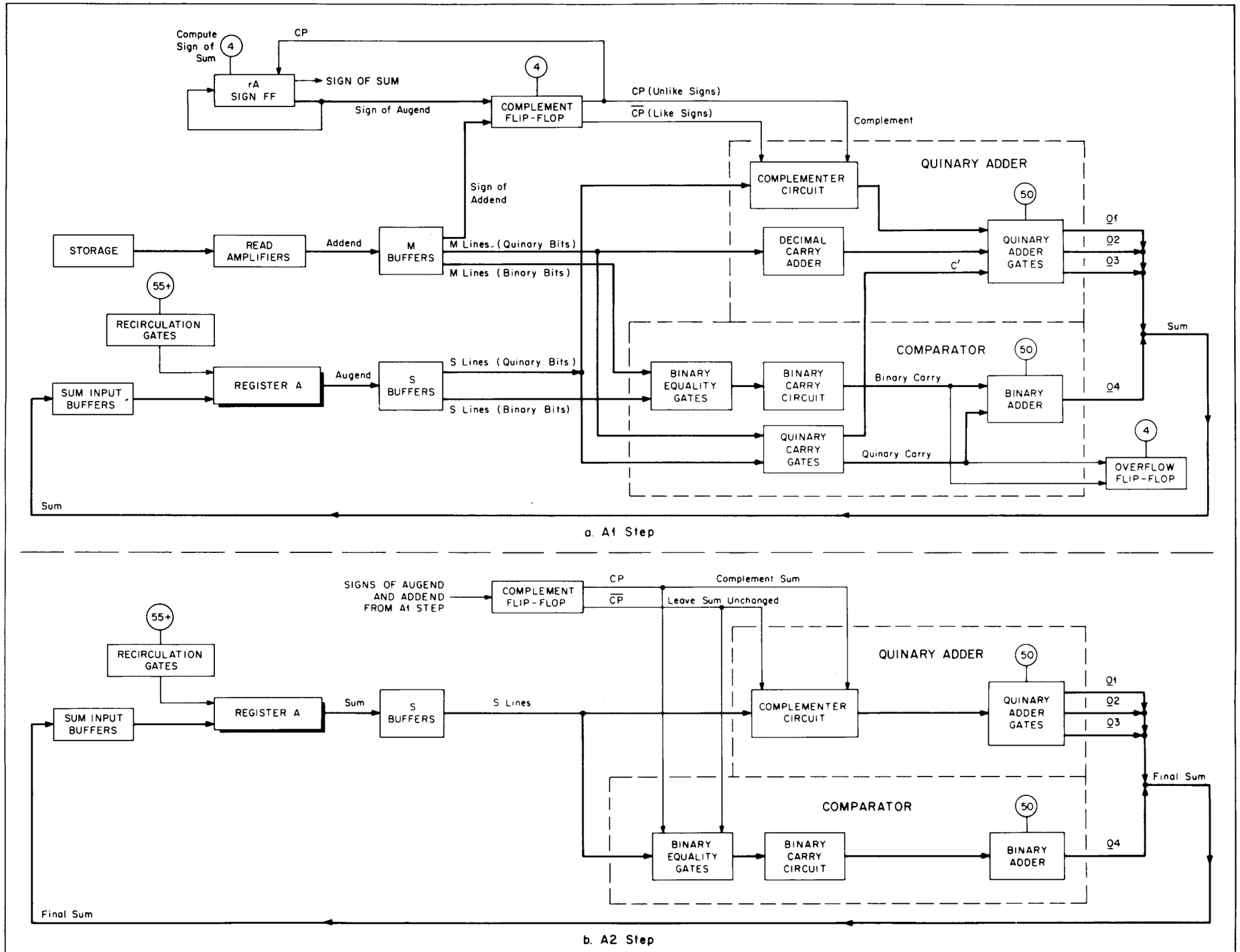

Figure 4-8. Add Instruction

4-24. SUBTRACT INSTRUCTION. The execution of add and subtract instructions is identical; the two instructions differ only in control functions. The function of the subtract instruction is to subtract algebraically the contents of the storage location designated by the m address from the contents of rA, store the difference in rA, compute the sign of the difference and store it in the rA sign flip-flop. The quantity in storage is the subtrahend; the quantity in rA is the minuend. The subtract instruction also requires two execution steps, S1 and S2.

Although the instruction code for subtract is 75, the staticized digits cause the same function signals to be generated as those generated for the staticized add instruction. The STR FF4 output for subtract is an STR4 signal. As a result, gates 10 and 11 of the CP FF operate during subtraction to determine whether the subtrahend is to be complemented.

When quantities with unlike signs are subtracted, the process is the same as when quantities with like signs are added. The sign of the subtrahend is changed, and the two quantities are added. These conditions cause the CP FF to be restored to $\overline{CP}$ so that no complementing takes place.

A special circuit in the function encoder operates during addition and subtraction to control the CP FF and complementing in the A2 or S2 step. The operation of this circuit is described below.

4-25. SAMPLE PROBLEMS. The many similarities and the few dissimilarities of addition and subtraction may be illustrated by two sample problems. In the examples two digits are first added and then subtracted.

(1) Addition. In this sample addition problem column (A) indicates the digits, (B) indicates their biquinary equivalents, (C) indicates the bits of the digits as signals on the M and S lines, and (D) represents the outputs of the decimal-carry adder and complementing circuits. The M4 and S4 bits are not included because they are added within the binary adder. The addend is the contents of m, and the augend the contents of rA.

EXAMPLE OF ADDITION

(A)	(B)	(C)					(D)		
+2 (m)	= 0010 =	$\overline{M4}$	$\overline{M3}$	M2	$\overline{M1}$	= $\overline{M3U}$	M2U	$\overline{M1U}$	
+1 (rA)	= 0001 =	$\overline{S4}$	$\overline{S3}$	$\overline{S2}$	S1	= $\overline{S3C}$	$\overline{S2C}$	S1C	
		LOW	LOW	HIGH	HIGH				
SUM AFTER A1 and A2:		$\underline{0}4$	$\underline{0}3$	$\underline{0}2$	$\underline{0}1$	= 0011 or +3			

Like signs in the add instruction restore the CP FF to $\overline{CP}$. The quinary bits of the augend, $\overline{M3}$, M2, and $\overline{M1}$, go to the decimal-carry adder, which does not change their value. The outputs of the circuit are $\overline{M3U}$, M2U, and $\overline{M1U}$, which have the same quinary value (010) as the inputs. The quinary bits of the addend, $\overline{S3}$, $\overline{S2}$, and S1 go to the complementer circuit, which does not complement because the $\overline{CP}$ signal is low. The outputs of the complementer circuit, $\overline{S3C}$, $\overline{S2C}$, and S1C, have the same value (001) as the inputs. The binary bits of the two digits, M4 and $\overline{S4}$, go to the binary-carry circuit. These two bits and $\overline{CP}$ generate a low $\underline{0}4$ output from the binary adder. A low output signal on the $\underline{0}$ lines is a 0 bit, which goes to the A4 subregister of rA. The outputs of the decimal-carry adder and complementer circuits go to the quinary adder. Only gate 34 of the adder is permissive to the input combination. Gate 34 produces a high $\underline{0}12$ output which goes to the A1 and A2 subregisters of rA. Hence the two lowest order bits of the sum are 1 bits. Because only gate 34 is permissive,

the other gates are blocked. As a result, inputs to the A3 subregister from the quinary adder are low $\underline{0}$ signals, indicating a 0 bit. The sum determined during the A1 step, therefore, is 0011, or 3. In the A2 step this sum recirculates unchanged through the complementer circuit because the CP FF remains restored to $\overline{CP}$. The rA sign flip-flop determines from the signs of the two quantities that the sign of the sum is plus.

(2) Subtraction. In the first step of subtraction, S1, the input M and S bits indicated by (C) which go to the decimal-carry adder and the complementer are the same as in addition. In subtraction, however, the decimal-carry adder adds a 1 to the subtrahend and the complementer produces the 9's complement of the minuend if the CP signal is present. (Complementing is explained later in this section.)

The minuend is the contents of rA, and the subtrahend the contents of m.

EXAMPLE OF SUBTRACTION

S1 STEP

	(A)	(B)	(C)		(D)
+2	(rA) = 0010 =	$\overline{S4}$ $\overline{S3}$ S2 $\overline{S1}$	⟶ complement ⟶		$\overline{S3C}$ S2C $\overline{S1C}$
+1	(m) = 0001 =	$\overline{M4}$ $\overline{M3}$ $\overline{M2}$ M1	⟶ add 1 ⟶		$\overline{M3U}$ M2U $\overline{M1U}$

	HIGH	HIGH	LOW	LOW		
SUM AFTER S1:	$\underline{0}$4	$\underline{0}$3	$\underline{0}$2	$\underline{0}$1	=	1100 or 9

S2 STEP

	(E)	(F)		(G)
1100 (from rA)	= S4 S3 $\overline{S2}$ $\overline{S1}$	⟶ complement ⟶		$\overline{S3C}$ $\overline{S2C}$ $\overline{S1C}$
0000 (on M lines)	= $\overline{M4}$ $\overline{M3}$ $\overline{M2}$ $\overline{M1}$	⟶ add 1 ⟶		$\overline{M3U}$ $\overline{M2U}$ M1U

	LOW	LOW	LOW	HIGH		
SUM AFTER S2:	$\underline{0}$4	$\underline{0}$3	$\underline{0}$2	$\underline{0}$1	=	0001 or 1

At t0B of the first step of subtraction (S1) the plus signs of the two digits and the STR4 signal set the CP FF to CP at gate 11. At t1A, high signal CP4 is generated for one pulse time. Signal CP4 goes to the initial force-decimal-carry circuit to force generation of the decimal-carry signals, A and C. The A and C signals represent the 1 bit which is to be added to the subtrahend in the decimal-carry adder. Signals A and C, because they were generated by the CP4 signal, last for only one pulse time. The quinary M inputs to the decimal-carry adder represent a decimal 1; the outputs (D) represent a 2.

Complementing of the S input combination to the complementing circuit is not evident from the output combination (D) which retains the same quinary value. The result of complementing, however, is evident at the outputs of the adders. Only gate 46 of the adder is permissive to the outputs of the decimal-carry adder and complementer circuits; it produces a high $\underline{O}3$ output and low $\underline{O}2$ and $\underline{O}1$ outputs. The $\overline{M4}$ and $\overline{S4}$ bits, with CP, send a low signal to gate 6 of the binary adder. None of the quinary carry gates alerted by $\underline{C}P$ is permissive to the M and S inputs. As a result, a low $\overline{C}$ signal alerts gate 6 to produce a high $\underline{O}4$ output, indicating a binary 1 bit. The $\underline{O}$ input bits to rA at the end of the S1 step therefore have a value of 1100 or 9. The decimal 9 is the 10's complement of the true answer.

Because addition of the two combinations in the S1 step produced no decimal carry, the $\overline{A}$ and $\overline{C}$ signals from the comparator (figure A12) are low at t11B of the S1 step. Gates 62 and 63 of the function encoder (figure A4), alerted by the CP signal to the low $\overline{A}$ and $\overline{C}$ signals are permissive at t11B of the S1 step. When the gates are permissive, low FS 74 is generated. This function signal keeps the CP FF set to CP and also generates the CP5 signal for one pulse time. The CP5 signal forces decimal-carry signals A and C to low from t1B until t2B of the S2 step.

In the S2 step, the 1100(E) combination returns to the S lines from register A as S4, S3, $\overline{S2}$, $\overline{S1}$ (F). The three lowest order S bits go to the complementer which produces a $\overline{S3C}$, $\overline{S2C}$, $\overline{S1C}$ (G) output combination.

During the S2 step there is no information on the M lines, and the barred M signals are all low (F). The A and C signals, which are present for one pulse time, cause a

decimal 1 to be added to the 0 value of the M bits. The resulting output of the decimal-carry adder is M3U, M2U, M1U (G).

The outputs of the decimal-carry adder and complementer go to the quinary adder. Only gate 32 is permissive to the input combination. Gate 32 produces a high 01 output, while the 02 and 03 outputs of the quinary adder and the 04 output of the binary adder are low. The output combination of the quinary and binary adders, 0001 or one, returns to the sum input gates of rA. The plus sign of the result is computed by the rA sign flip-flop (section 3-67).

4-26. MULTIPLICATION

Multiplication in the system is accomplished by iterative additions and shifts of the multiplicand. The multiplicand is added to itself the number of times specified by each digit of the multiplier. The multiplication process has two steps, M1 and M2. The processor can multiply a ten-digit multiplicand by a ten-digit multiplier. In such a case the 20-digit product will be stored in rA and rX. The least significant part of the product is stored in rX; the most significant part of the product is stored in rA.

Before multiplication, the multiplicand is placed in rL by a programmed transfer instruction. In the first step of multiplication (M1) the multiplier is transferred from its storage location to rX. A code combination, the multiplier sentinel, is placed in the LSD position of rA. The sentinel will signal the end of multiplication and cause the multiplication process to end.

In the second step, M2, the multiplicand in rL is added to itself in the adder the number of times indicated by the LSD of the multiplier. The LSD of the multiplier is stored in the multiplier/quotient counter (MQC) which counts the number of additions. The sum of these additions is returned to rA. The contents of rA and rX are next shifted right one digit position, placing the LSD of rA in the MSD position of rX. The LSD in rA before each shift becomes the LSD of the product. This process of adding and shifting continues until the LSD of the product is the LSD of rX.

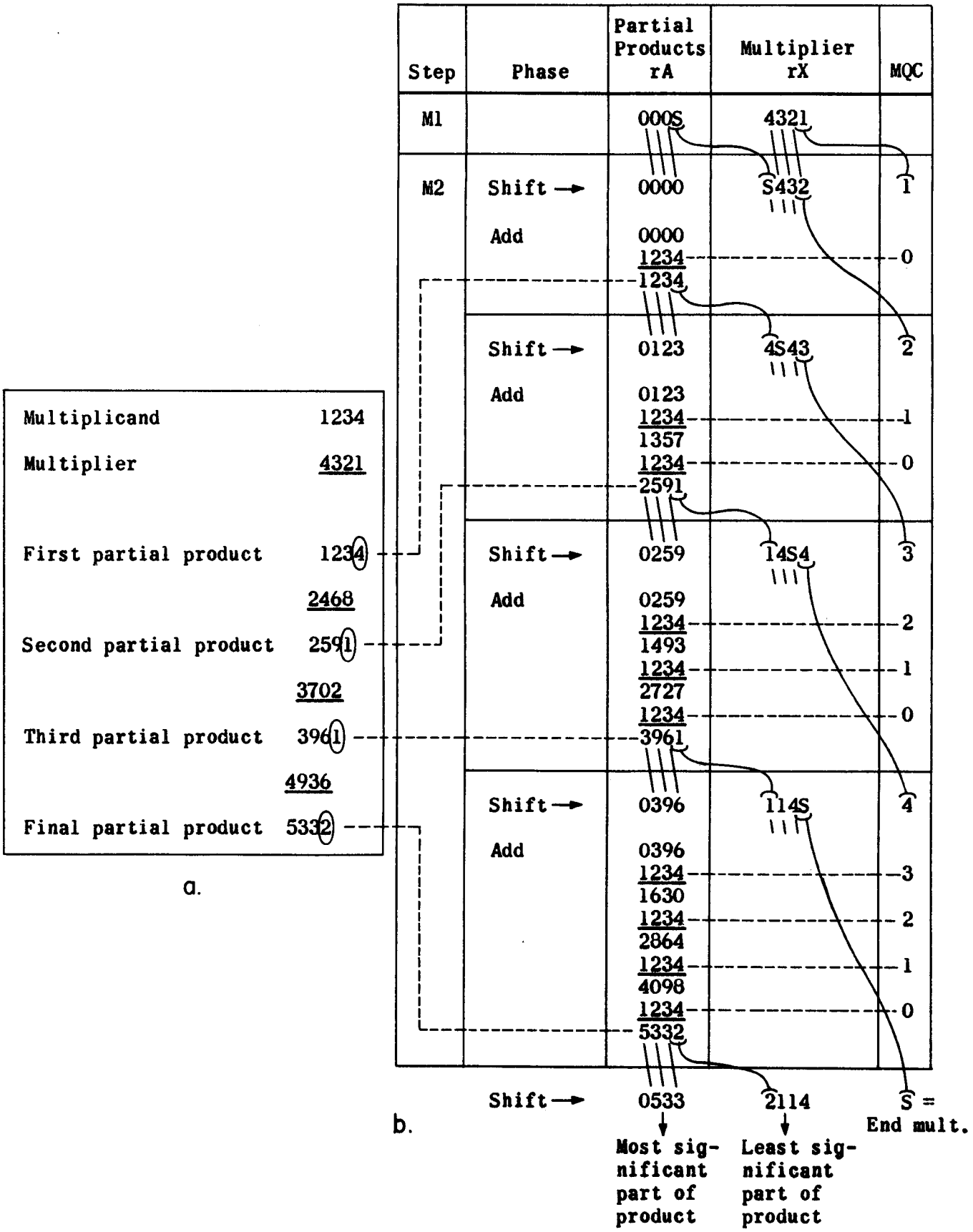

Figure 4-9. Multiplication Process

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The sentinel also is shifted during the shift operations. Initially it is shifted from the LSD position in rA to the MSD position of rX. Every ensuing shift operation shifts the sentinel one more place to the right until it reaches the LSD position of rX. It is then shifted into the MQC where it ends the multiplication process.

The M2 step consists of two phases, designated IER and $\overline{\text{IER}}$.

During each IER (shift) phase, the contents of rA and rX are shifted one place to the right, the sentinel is shifted one place, and the LSD of rX, which contains the multiplier, is shifted into the MQC to control the number of additions.

During the $\overline{\text{IER}}$ (add) phase, the multiplicand is added to the sum of additions from the previous IER phase the number of times specified by the multiplier digit in MQC. The new sum is returned to rA for the next IER phase.

4-27. GENERAL DESCRIPTION. The multiplication method used in the processor is illustrated by the sample problem in figure 4-9. In the problem, the number 1234 is multiplied by 4321. Although the processor can multiply two ten-digit numbers, the sample problem is confined to two four-digit numbers. Figure 4-9a shows the method used by the computer; figure 4-9b shows the method as used in the processor circuits. The circled digits and the final four digits in figure 4-9a are the product digits. The first computed product digit is 4 and it is the LSD of the final product.

During the M1 step, the multiplication sentinel (S) is placed in the LSD of rA, and the multiplier is placed in rX. The M2 step begins with a shift phase in which the sentinel is shifted from rA to the MSD position of rX. The multiplier in rX is also shifted right, causing the LSD, 1, to be transferred to the MQC. The next phase of M2 is the add phase in which the multiplicand from rL is added to the contents of rA the number of times specified by the digit stored in MQC. The MQC digit is 1; therefore the multiplicand 1234 is added to the contents of rA, which at this point is 0000. The sum of the addition, 1234, is returned to rA. The MQC counts down to 0 after the necessary number of additions has occurred, and a zero digit in MQC initiates the next shift phase.

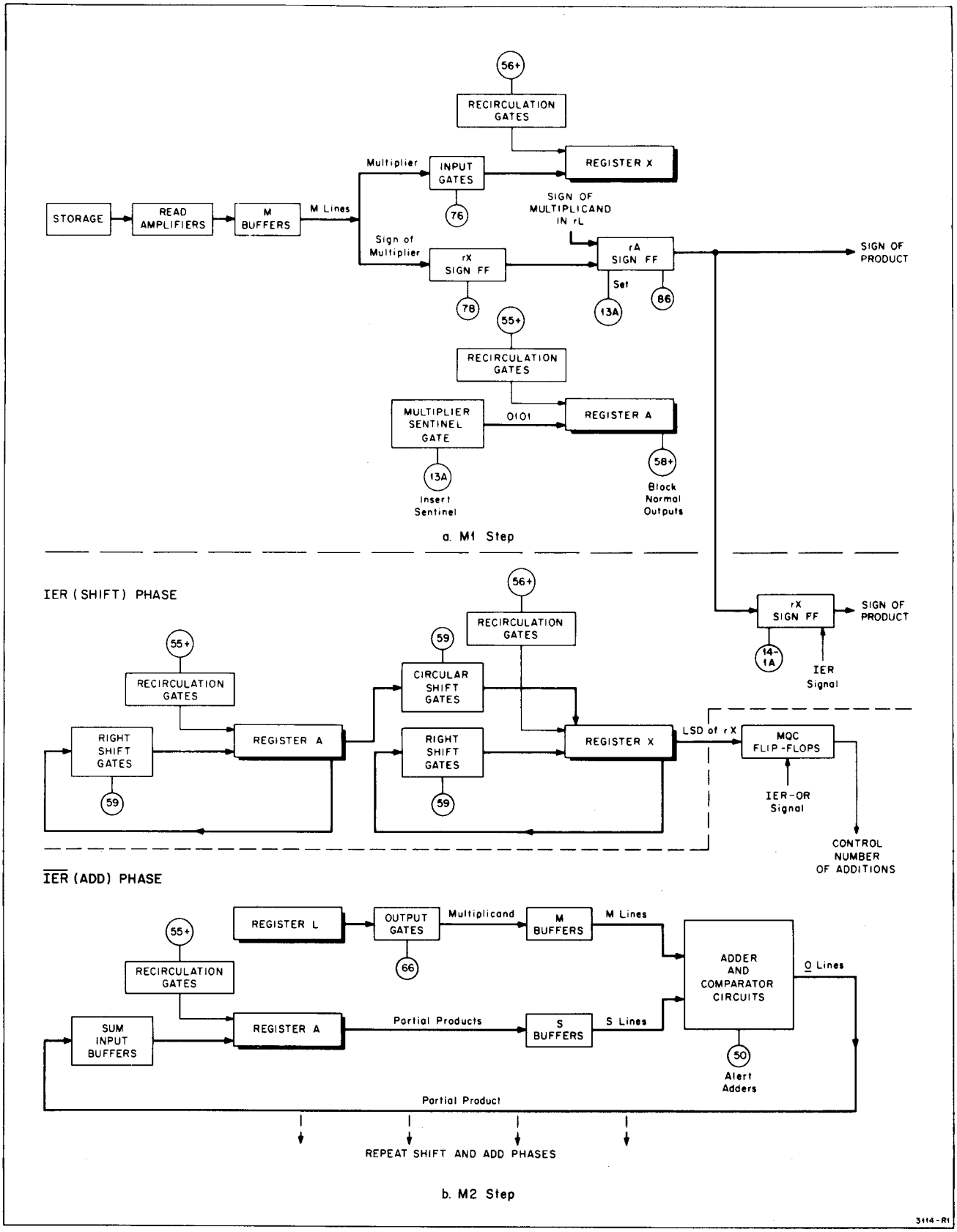


Figure 4-10. Multiply Instruction

In the next shift phase, the contents of rA (1234) is shifted to the right, causing the LSD of the first partial product, 4, to be shifted into rX. At the same time that rA and rX are shifted, the sentinel advances to the right one more place. The LSD of the multiplier in rX, 2, is shifted into MQC to control the number of additions in the next add phase. The multiplicand, 1234, is added to the shifted contents of rA, 0123, twice as specified by the MQC. The two additions produce the second partial product, 2591. The second partial product is also shifted, the LSD, 1, becoming the second quotient digit when placed in the MSD of rX. The product digits and sentinel in rX again shift to the right, creating the MSD vacancy into which the partial product digit, 1, is placed. The LSD of rX, 3, is transferred to the MQC. The MQC therefore permits three additions of the multiplicand, after which a zero reading starts the next shift phase. This process of alternating shift and add phases continues until the sentinel reaches the LSD position of rX and is shifted into MQC. The sentinel combination in MQC ends the multiplication with the most significant part of the product in rA and the least significant part in rX.

4-28. INITIAL CONDITIONS. The following preparations for multiplication take place before the M1 step:

(1) A transfer instruction places the multiplicand in rL and its sign in the rL sign flip-flop.

(2) The instruction word is located in the search-for-instruction step.

(3) The multiply instruction (85) is staticized in the static register.

(4) The multiplier in the storage location designated by m is read from the drum in the search-for-operand step.

(5) STR FF1 is jammed to 1. The combination in the STR is 1011 1X01, which generates function signals at t0A and t0B to carry out the M1 step.

4-29. M1 STEP. The sign of the final product in multiplication is determined during the M1 step (figure 4-10a) by the rA sign flip-flop, which compares the signs of the multiplier and multiplicand. The sign of the multiplicand already has been stored in the rL sign flip-flop during the transfer instruction. The sign of the multiplier enters the

rX sign flip-flop at t0B at gates 34 and 35, which are alerted by function signal 78. At t0A, the rA sign flip-flop is set to A- by FS 13A to prepare for the comparison of the signs of the multiplier and multiplicand. At t11B of the M1 step, FS 86 alerts gates 1 and 2 of the rA sign flip-flop. If the signs of the multiplier and multiplicand are alike (X+ and L+, or X- and L-), the flip-flop is restored to A+. If the signs are unlike, gates 1 and 2 are blocked and the flip-flop remains set to A-.

At t0B, FS 62 operates gate 19 of the clear-MQC circuit. At t1A the CLQ signal clears the MQC flip-flops, which receive the LSD of the multiplier in the M2 step. At t0B, FS 56+ blocks the recirculation gates of rX, and FS 76 alerts the input gates to the multiplier which enters on the M lines.

Register A is cleared during the M1 step so it can receive the partial products during the M2 step. At t0B, FS 55+ blocks the recirculation gates of rA. At t1B, FS 13 operates the multiplier sentinel gate of rA. When this gate operates, it jams 1's into the A1 and A3 subregisters. As a result, the LSD of rA is the multiplier sentinel combination, 0101. Register A now contains the sentinel and nine zero digits. Function signal 58+ blocks the normal output gates of rA so that the sentinel remains within the register.

At t10B of the M1 step, FS 64 alerts the STR stepping gate which jams STR FF2 to a 1 output to initiate the M2 step. Function signals for the M2 step are generated at t0A and t0B of the M2 step.

At t11B, gate 11 of the IER FF samples the STR output signals which indicate that the M2 step has been staticized, and the $\overline{Q}$ (0) outputs of the MQC flip-flops, which indicate that the circuit has been cleared. If these two conditions are met, the IER FF is set at t0B to initiate the IER phase of the M2 step. The flip-flop generates low control signals IER at t0B and IER-OR at t1B, high control signals IERA1+ from t0A to t0B only, IERA2+ at t1A, and IER+ at t0B. These signals control the IER phase of the M2 step.

4-30. M2 STEP. The M2 step staticized in the static register generates FS 55+ and $\overline{\text{FS}}$ 66. These signals are present during both the IER and $\overline{\text{IER}}$ phases of M2. Other function signals, however, are generated during each of the two phases by the outputs of the IER FF.

(1) IER Phase. At the beginning of the IER shift phase, control signal IERA1+ generates FS 59 for one pulse time from t0B to t1B. Beginning at t1B, control signal IERA2+ is high, and it generates FS 59 and 56+.

At t0A of the IER phase, FS 14-1A jams the rX sign flip-flop to X+. At t0B of the IER phase, the low IER control signal alerts rX sign flip-flop, gate 33, which samples the sign of rA from the rA sign flip-flop. If the sign of rA is minus, the rX sign flip-flop is restored to X-; if it is plus, the flip-flop remains set to X+. Thus the signs of both parts of the final product will be identical.

Function signal 59 alerts the right-shift gates of rA and rX and the circular-shift gates of rX so that a right shift of both registers can take place. Function signal 56+ blocks the recirculation gates of rX; function signal 55+ blocks the recirculation gates of rA. During the first IER phase, the right-shift operation causes the multiplication sentinel, in the LSD position of rA, to be shifted into the MSD position of rX. At the same time, the LSD of the multiplier in rX is shifted into the MQC flip-flops. Control signal IER-OR alerts the input gates of the four MQC flip-flops to the outputs of the rX subregisters.

Function signal 66 alerts the output gates of rL, which stores the multiplicand during multiplication. The multiplicand in rL is transferred to the M lines and into the adder circuits in preparation for the add phase ($\overline{\text{IER}}$). The partial product stored in rA after each shift phase is on the S lines and is also an input to the adder circuits.

During every IER shift phase, the IER control signal alerts gate 18 of the ending-pulse circuit to sample for the 0101 sentinel in MQC. When the sentinel is present in the MQC flip-flops, the gate is permissive and the EP signal is generated to end multiplication.

(2) $\overline{\text{IER}}$ Phase. During this phase the contents of rA is added in the adder to the multiplicand from rL. The $\overline{\text{IER}}$ add phase is initiated at t11B of the IER phase by the t11B+ timing signal at gate 40 of the IER FF. The signal restores the flip-flop at t0A, and the polarities of the signals generated by the flip-flop during the IER phase are reversed for the $\overline{\text{IER}}$ phase. The IER+ output, which is now low, goes to the instruction decoder. If the staticized M2 signals are present and the IER+ signal is low, FS 14-2A is generated. Function signal 14-2A in turn generates FS 50 and 61. Function signal 50 alerts the binary and quinary adders. Function signal 61 alerts the countdown gates of the multiplier-quotient counter.

After each shift phase, the multiplicand is added to the partial product in the binary and quinary adders, just as in addition (section 4-23). The sum of each addition is returned to rA. The MQC countdown circuit counts down to zero from the multiplier digit stored in it during the shift phase. When the reading in the MQC flip-flops is zero, the IER FF is set to initiate the IER shift phase again.

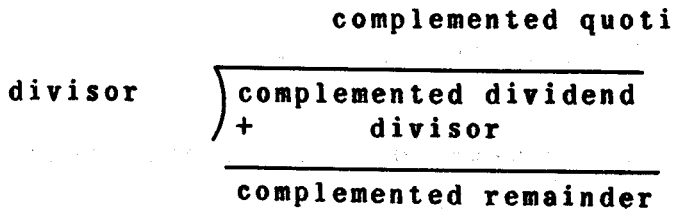
After the last multiplier digit has been processed and the necessary additions have been performed, the sentinel is shifted into the MQC flip-flops. In the next shift phase, the IER signal alerts the ending-pulse gate 18. If the sentinel (0101) is stored in MQC, the Q1 and Q3 signals from the MQC flip-flops are low. Only the sentinel has 1 bits in these positions. The EP is generated and, at t0B, a search for the next instruction is initiated.

4-31. DIVISION

In the method of non-restoring division used in the system the programmer scales the dividend so that it will be smaller than the divisor. Within the processor the dividend is logically multiplied by ten and complemented. The divisor is added to this new form of the dividend until addition produces an overflow carry. The remainder is complemented and multiplied by ten (shifted left), and the divisor is again added to this new dividend.

The number of divisor-to-dividend additions is monitored for each step and these numbers (or their complements) become the final quotient digits. The end of the division process is signaled by a sentinel that has been stored in the least significant digit position of a register and is shifted with each step toward the most significant digit position. When the sentinel becomes the most significant digit, the division process ends.

4-32. GENERAL DESCRIPTION. In the first phase of the division process, the dividend is shifted left and complemented. In the next phase, the divisor is added to the complemented dividend. Because the dividend is in its complemented form, the resulting quotient digit is also in complemented form. The quantity which remains after the divisor-to-complemented-dividend additions is the complemented remainder as shown:



The complemented remainder becomes the dividend of the next phase in which the next quotient digit will be determined. Before being used as the next dividend, however, this complemented remainder is complemented again to return it to its original or true form as shown:

```
                    quotient
                  ___________
        divisor  )dividend
                  + divisor
                  _________
                  remainder
```

In the next succeeding phase the dividend, quotient, and remainder again become the complemented form of their actual value. The cycles of the shift and complement phases alternate throughout the division process, and are differentiated as even cycles and odd cycles.

The odd cycles of the shift and complement phase always precede the even cycles. In the odd cycles the dividend, the quotient, and the remainder less the divisor are the 9's complement of their real value. In the even cycles the three quantities are represented in their uncomplemented form.

It must be remembered that although the quantity contained in rA at the end of every add phase is the remainder of that phase it becomes the new dividend necessary for the determination of the next quotient digit. Therefore, to arrive at a five-digit quotient, there must be five dividends, each dividend being the remainder of the previous division.

The quotient digits derived from each cycle are stored in rX, the contents of which is left shifted and complemented until division ends. The quotient digit derived during an odd cycle is complemented an odd number of times so that when it is transferred to rA it is in its true form. The quotient digit derived during an even cycle is complemented in rX an even number of times so that when transferred to rA it too is in its true form.

In the sample division problem (figure 4-11) the divisor, 0.133, is divided into the dividend, 0.032. The MQC column shows the state of the MQC countdown circuit at each successive addition. The Phase column shows whether the computer is in the shift-complement phase (OR) or the add phase ($\overline{OR}$). The distinction between odd and even OR phases is explained later in this section.

Step	MQC	Phase	rA	rX	rL
D1	0		003200	000001	013300
D2	10	OR odd	//// 967990	///// 999980	013300
	9	$\overline{OR}$	+ 133 981290		
	8		+ 133 994590		
	7		+ 133 C007890	999980	
			////	////	
	10	OR even	921000	000120	
	9	$\overline{OR}$	+ 133 934300		
	8		+ 133 947600		
	7		+ 133 960900		
	6		+ 133 974200		
	5		+ 133 987500		
	4		+ 133 C000800	000120	
			////	////	
	10	OR odd	991990	998750	
	9	$\overline{OR}$	+ 133 C005290	998750	
			////	////	
	10	OR even	947000	012400	
	9	$\overline{OR}$	+ 133 960300		
	8		+ 133 973600		
	7		+ 133 986900		
	(6)		+ 133 C000200	012400	
D3	0		024060	000200	013300
			Final Quotient	Carry	Divisor

OR = shift and complement phase $\overline{OR}$ = add phase

```
        .2406
.133:  .0320000
         266
          540
          532
            800
            798
             02
```

Figure 4-11. Division Process

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For simplification the division process described is for a six-digit register rather than the 12-digit register used in the system. The least significant digit position in each register is the sign position and remains unchanged throughout the process. The most significant digit is the SBW position.

The divide instruction consists of the three steps D1, D2, and D3. In the D1 step the following takes place:

(1) MQC is cleared to 0.

(2) The dividend is placed in rA.

(3) The division sentinel (0001) is stored in LSB position of rX.

The first phase of D2 is the odd OR phase, in which the contents of rA and rX are individually shifted left and complemented. The 003200 combination in rA therefore becomes the quantity 967990. Similarly, the 1 sentinel and the contents of rX become the quantity 999980.

In the next phase, the $\overline{OR}$ phase, the divisor is added to the dividend. The 133 divisor can be added to the complemented dividend three times before a decimal carry occurs. Meanwhile, the MQC counts down from ten to seven. This ends the $\overline{OR}$ phase with a 7 digit in MQC, the remainder in rA, and the rX sentinel shifted one digit position to the left.

In the next phase, the even OR, the remainder is shifted left and complemented to the quantity 921000, which becomes the new dividend for the computation of the next quotient digit. In the left shift operation, a 0 replaces, in the LSD position, the MSD shifted to the left out of the register. The quotient digit 7, stored in MQC, is placed in the LSD position of rA after the sentinel is shifted left, and both are complemented. The quantity in rA becomes 000120, of which the 1 is the sentinel and 2 is the first quotient digit. At the end of the OR phase the MQC is jammed to ten.

In the next $\overline{OR}$ phase a count of the divisor is again added to the dividend. Six such additions take place before a decimal carry occurs. As a result, the MQC counts down to 4 and the $\overline{OR}$ phase ends.

The next OR phase causes the remainder, 000800, to

be complemented and shifted, the sentinel to be shifted, the digit 4 from MQC to be placed in rX, and the contents of rX to be complemented. The MQC is again jammed to ten.

Addition of divisor to dividend (remainder) again takes place in the $\overline{OR}$ phase. Only one addition takes place before decimal carry occurs; thus, the digit in MQC is 9.

In the next OR phase, the remainder 005290 is shifted and complemented to a quantity of 947000, the new dividend for the last add phase. The sentinel is shifted into the next MSB position. The quotient digit 9, computed in previous add phase, enters the MSB position of rX, and the contents of rX is complemented. The quantity in rX is now 012400. The 0 is the SBW, 1 is the sentinel, 2 is the first final quotient digit, 4 is the second final quotient digit, and 0 is the sign position.

The final addition phase, $\overline{OR}$, steps MQC down to 6 and leaves a remainder in rA of 000200.

In the previous OR phase the 1 sentinel was shifted to the MSB position of rX, signifying the end of division. The $\overline{OR}$ add phase takes place as described, but the sentinel has begun to initiate the D3 step, which starts as $\overline{OR}$ ends.

In the D3 step, the contents of rA and rX are interchanged; the final quotient is stored in rA and the final remainder in rX. The quotient digit, 6, derived from the last set of additions, goes uncomplemented to the LSD position of rA to become part of the quotient. The sign of the quotient also is computed during D3 in the rA sign flip-flop.

Examination of the problem shows that the quotient digits resulting from an odd OR phase are complemented an odd number of times; the quotient digits resulting from an even OR phase are complemented an even number of times. This process ensures that the final quotient, transferred to rA, is the true quotient.

4-33. INITIAL CONDITIONS. The following preparations for division have taken place brfore the D1 step:

(1) The search-for-instruction step has been completed.

(2) The divide instruction (55) has been staticized.

(3) The dividend (operand) has been located by the second search step.

(4) The divisor has been placed in rL by a previous instruction, either an L or a K instruction.

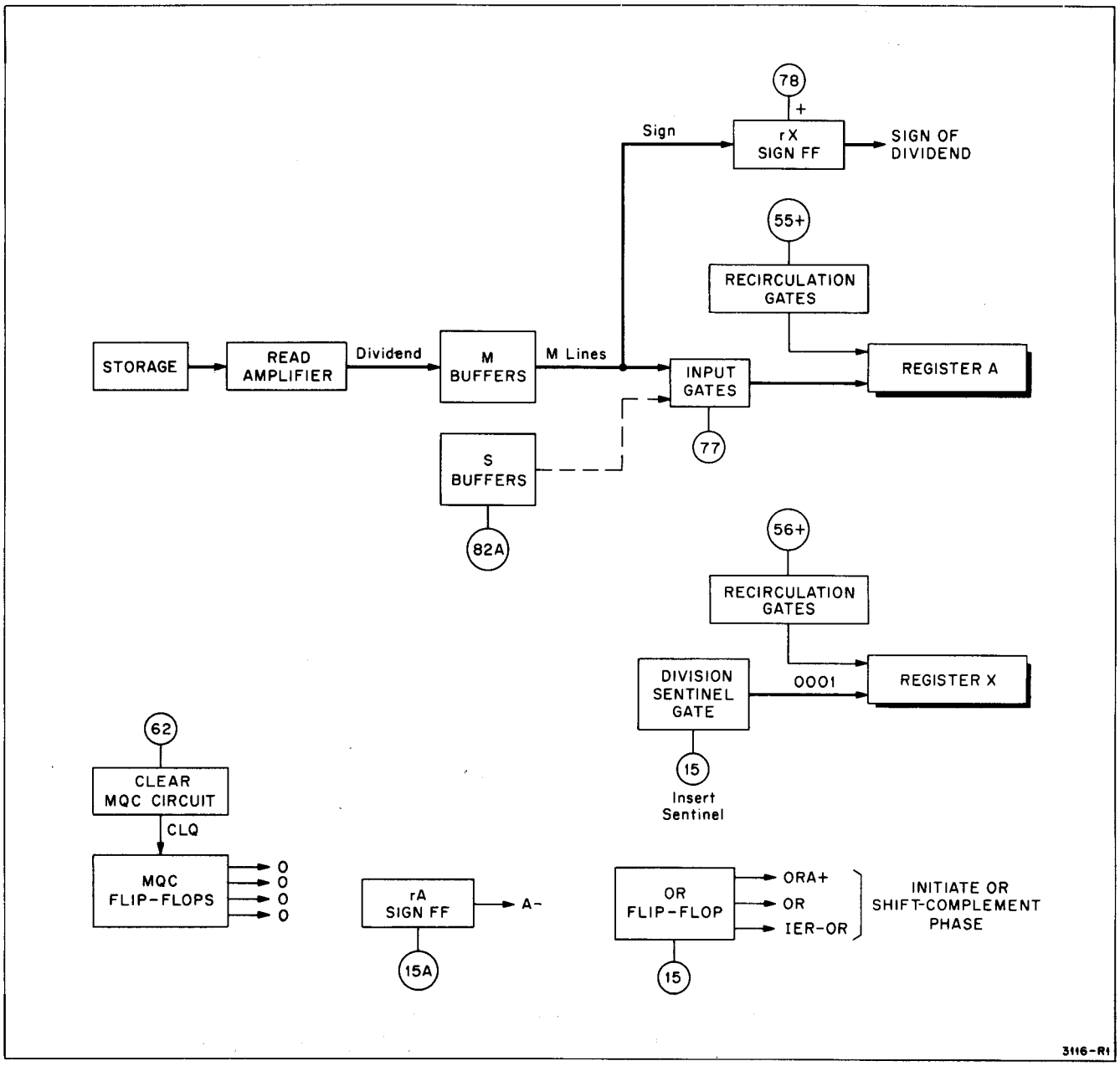


Figure 4-12. D1 Step of Division

4-34. D1 STEP. In the first execution step of division, D1 (figure 4-12), registers A and X are prepared for division, the rX and rA sign flip-flops are prepared for the computation of the sign of the quotient and the sign of the remainder, MQC is cleared, the division sentinel is placed in rX, and at the end of D1 the static register is stepped to D2. The divisor has been stored in rL by a previous instruction.

Function signal 55+ blocks the recirculation gates of rA to clear the register of its contents. Function signal 77 alerts the input gates of rA, making them permissive to the M and S lines. However, since only the dividend on the M lines is to be read into rA at this time, FS 82A holds the outputs of the S buffers low so that the S lines cannot read into rA.

Function signal 56+ blocks the recirculation gates of rX to clear the register. The division sentinel is generated by FS 15 at the division sentinel gate to place an 0001 combination in the LSD position of rX.

Function signal 62 alerts gate 19 of the clear MQC circuit at t0B to generate the CLQ signal at t1B. The CLQ signal clears the MQC flip-flops to zeros.

The sign of the divisor has been stored in the rL sign flip-flop by a previous instruction. At the beginning of D1, the rX sign flip-flop is set to X+ at t0B by FS 78 at gate 35. If the sign of the dividend is minus, gate 34 is permissive, causing an X- to be stored. The signs of the divisor and dividend are sampled in the D3 step to determine the sign of the quotient.

At t11B of the D1 step FS 15 alerts gate 9 to set the OR FF, (figure A15), initiating the first OR cycle of D2 at t0B. The flip-flop generates the IER-OR, ORA+, and OR control signals.

At t10B of D1, FS 64 alerts the STR stepping gate to step STR FF1 and STR FF2 to outputs STR1 and STR2. The combination in STR is now 1000 1X11 which generates the D2 function signals.

4-35. D2 STEP. The D2 step consists of alternating shift and complement phases (OR) and add phases ($\overline{OR}$). The first phase of D2 is always the OR phase and is followed by the $\overline{OR}$ phase.

(1) OR Phase. The OR phase (figure 4-13) is initiated by the setting of the OR FF at the end of D1 (figure 4-12). The D1 function signal 15 sets the flip-flop at t11B at gate 9.

The ORA+ control signal, generated during D1, is a high signal which sets the CP FF, producing a low CP output. Signal ORA+ also generates a CLQ signal at the clear-MQC circuit at buffer 42. The CLQ signal clears the MQC flip-flops.

(a) Complementing and Left Shift of rA. The contents of rA (dividend) normally reads onto the S lines; when normal recirculation of the register is blocked by FS 55+, the register is cleared. The first three bits of the dividend (S1, S2, and S3) on the S lines are read into the quinary-adder complementer circuit. The CP signal, which alerts the complementing gates, causes the first three bits of the dividend to be complemented. The quinary bits (S1C, S2C, and S3C) return to rA at the left shift gates. In recirculating through the complementer circuit the first three bits are delayed one pulse time, the time necessary to effect a left shift of rA. The fourth bit of rA is delayed (shifted left) within rA and recirculated to the left shift gates as an A"4 signal. The fourth bit is complemented by gate 42 which is alerted by the CP signal. Function signal 71 alerts the rA left-shift gates, and the left-shifted, complemented dividend enters and is stored.

(b) Complementing and Left Shift of rX. Function signal 56+ blocks the recirculation gates of rX, and the contents of the register including the sentinel enters the input gates of the MQC flip-flops. The IER-OR control signal, generated during D1, alerts these gates. The MQC flip-flops, which have been cleared by the CLQ signal, supply one pulse time of delay for the X1, X2, X3, and X4 outputs of rX. One pulse time after entering the flip-flops the X input bits become the Q outputs of the flip-flops and return to rX at the quotient complementing gates. The OR control signal alerts these gates, which complement the Q inputs from MQC. In the first OR cycle only the sentinel is stored in rX whereas in succeeding OR cycles the sentinel and quotient digits are stored in rX. The entire contents of rX is complemented and shifted left.

(c) Complementing the LSD of rA. In the first OR phase the original dividend is complemented and left shifted.

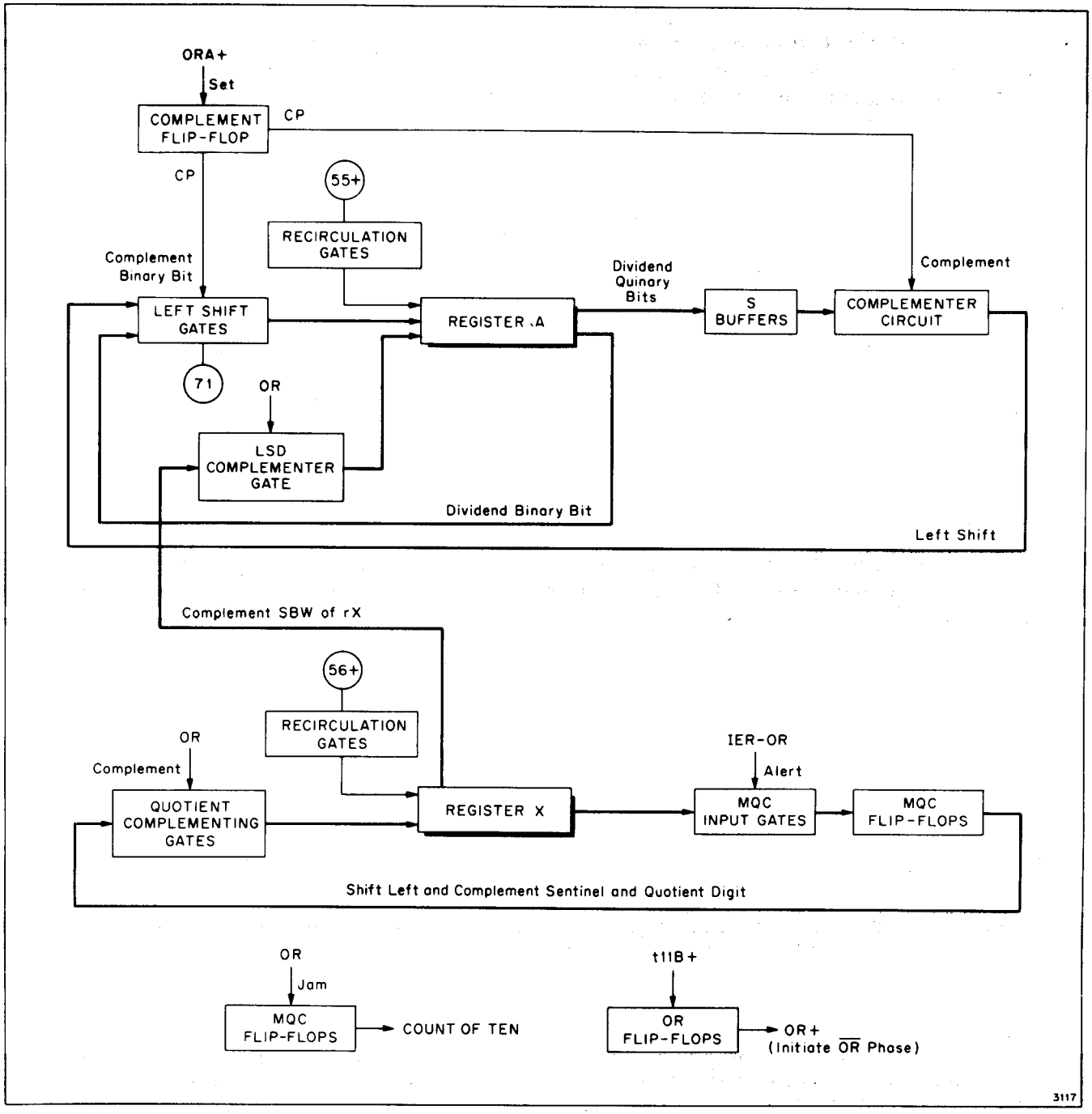


Figure 4-13. D2 Step, OR Phase

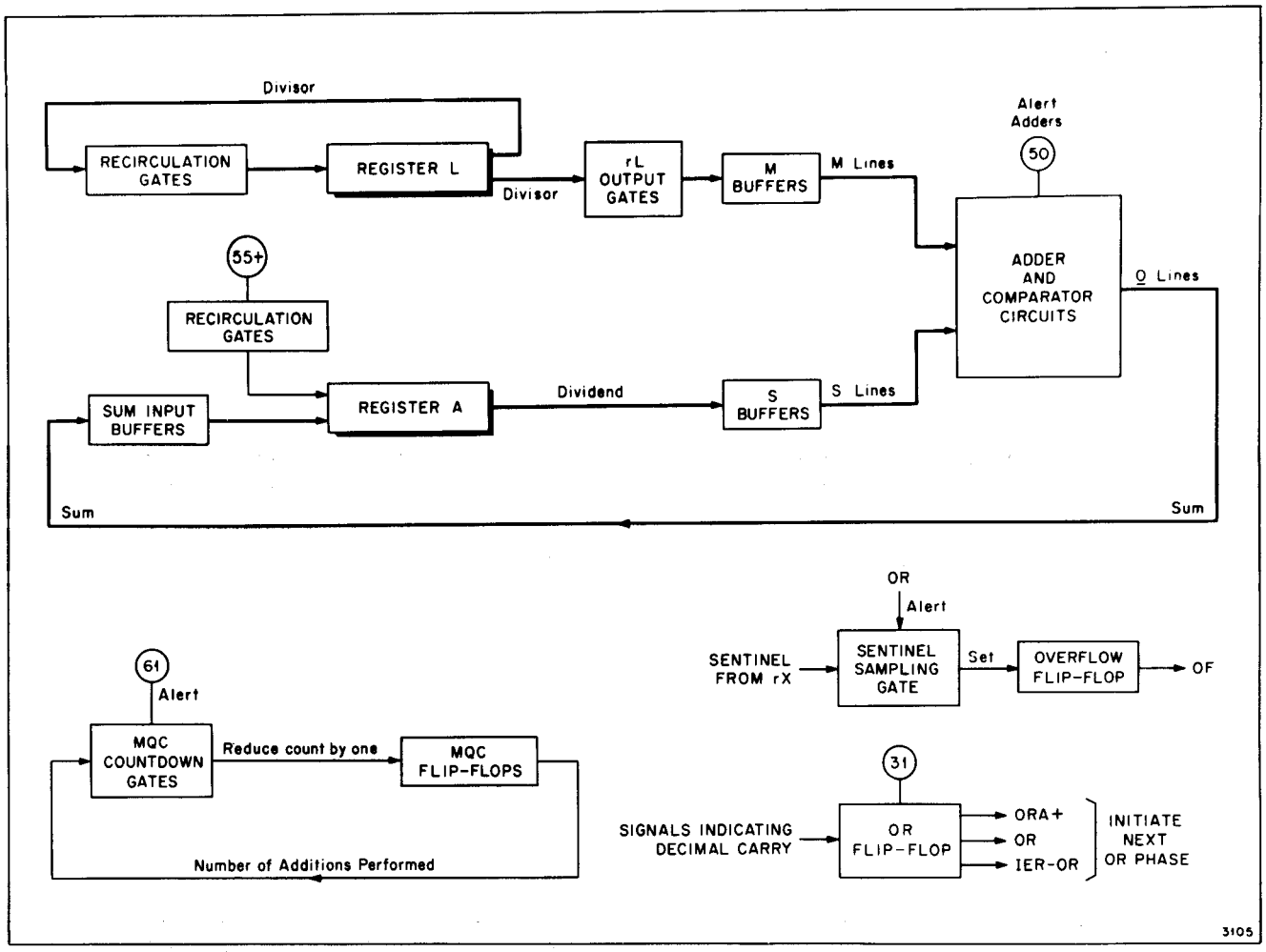


Figure 4-14. D2 Step, $\overline{OR}$ Phase

In an ordinary left-shift-of-rA instruction, the vacancy created in the LSD position is filled with a zero. In division, however, the dividend is complemented, and the digit which becomes the LSD must also be complemented. On alternate phases, therefore, the LSD of rA is either nine or zero. During the odd OR phases (shift and complement) the LSD of rA is nine. During the even OR phases (complement and shift) the LSD of rA is zero.

The LSD complementer gate of rA is alerted by the OR output of the OR FF. At t1B the gate samples the X4D output of rX, which is the SBW position. Only the X4D bit is necessary to determine whether a nine digit or a zero digit is stored in rX. If the SBW of rX is zero, it is complemented to a nine in the LSD of rA; if the SBW of rX is nine, it is complemented to a zero in the LSD of rA.

(d) Jam MQC. At t11B of each OR phase the OR signal makes gate 1 permissive, jamming ones into MQC flip-flops 1, 3, and 4. This action stores a ten combination in MQC to allow countdown during the $\overline{OR}$ phase.

(e) Initiate $\overline{OR}$ Phase. At the end of the OR phase a t11B+ high signal restores the OR FF to an output of OR+, initiating the $\overline{OR}$ phase.

(2) $\overline{OR}$ Phase. During the $\overline{OR}$ phase (figure 4-14) the divisor from rL and the dividend from rA go to the quinary and binary adder circuits where the two quantities are added. The MQC countdown circuit monitors the number of additions. The sum of the divisor-to-dividend additions returns to rA for temporary storage.

(a) Addition. The divisor, already placed in rL by a previous instruction, is recirculating within rL. Function signal 66 and the OR FF output, OR+, which is low at this time, make the rL output gates permissive. The contents of rL continues to recirculate but also reads onto the L lines to the M buffer and the M lines. The M lines go to the quinary and binary adders. Function signal 55+ blocks recirculation of rA, and the dividend reads into the S buffers and the S lines. The S4 bits of the dividend on the S lines read into the binary adder circuit. The three lowest order bits read into the quinary-adder circuit, as in the addition process (section 4-23). Function signal 50 alerts the quinary and binary adders to the M and S inputs. The divisor and dividend are added and the sum emerges on the $\underline{O}$ lines. With each addition, the MQC countdown gates, alerted by FS 61,

reduce the number stored in the MQC flip-flops by one every t1B of the OR phase. When decimal carry occurs, the remainder is still on the Q lines and the MQC contains the number of additions performed. Function signal 31 alerts gate 10 of the OR FF throughout the D2 step to sample the OF, A, C, S3, and S4 signals. The A and C signals at t11B indicate that the addition of the p10 digit has produced a decimal carry to the p11 digit. The S3 and S4 signals (1100=9) indicate that the p11 digit is a nine. If a decimal carry is added to the final digit to be added, a nine, a carry condition will occur. The OF FF is restored during the add phases, generating low OF. If present, these signals set the flip-flop to the OR phase by generating the OR, ORA+, and IER-OR control signals.

(b) End of D2 Step. During every OR phase of D2, the division sentinel advances toward the MSD position of rX. At t9B of the tenth OR cycle the sentinel sampling gate 27 examines the X1 bit of rX which, if present, indicates the sentinel in the MSB position of rX. If the gate is alerted by OR, indicating that the last addition has ended, the OF FF is set, generating OF. The OF signal makes it possible to step to D3, if the last OR phase is complete.

4-36. D3 STEP. In the D3 step (figure 4-15) the contents of rA and rX are interchanged, placing the final quotient in rA and the remainder (carry) in rX. The sign of the quotient also is computed during D3 and the instruction is ended.

(1) Interchanging rA and rX. Function signal 31 alerts input gate 001 of the D3 FF (figure A2) throughout the D2 step. When the following signals are present on the gate, the D3 FF is set, initiating the third step of division, D3:

(a) OF, indicating that the sentinel is the MSD of rX.

(b) A and C, which indicate that a carry or remainder is present.

(c) S3 and S4, which indicate the presence of the digit nine in the SBW of rA.

(d) STR8 which indicates that improper division has not occurred. (Improper division generates EP, which clears all STR flip-flops to zero.)

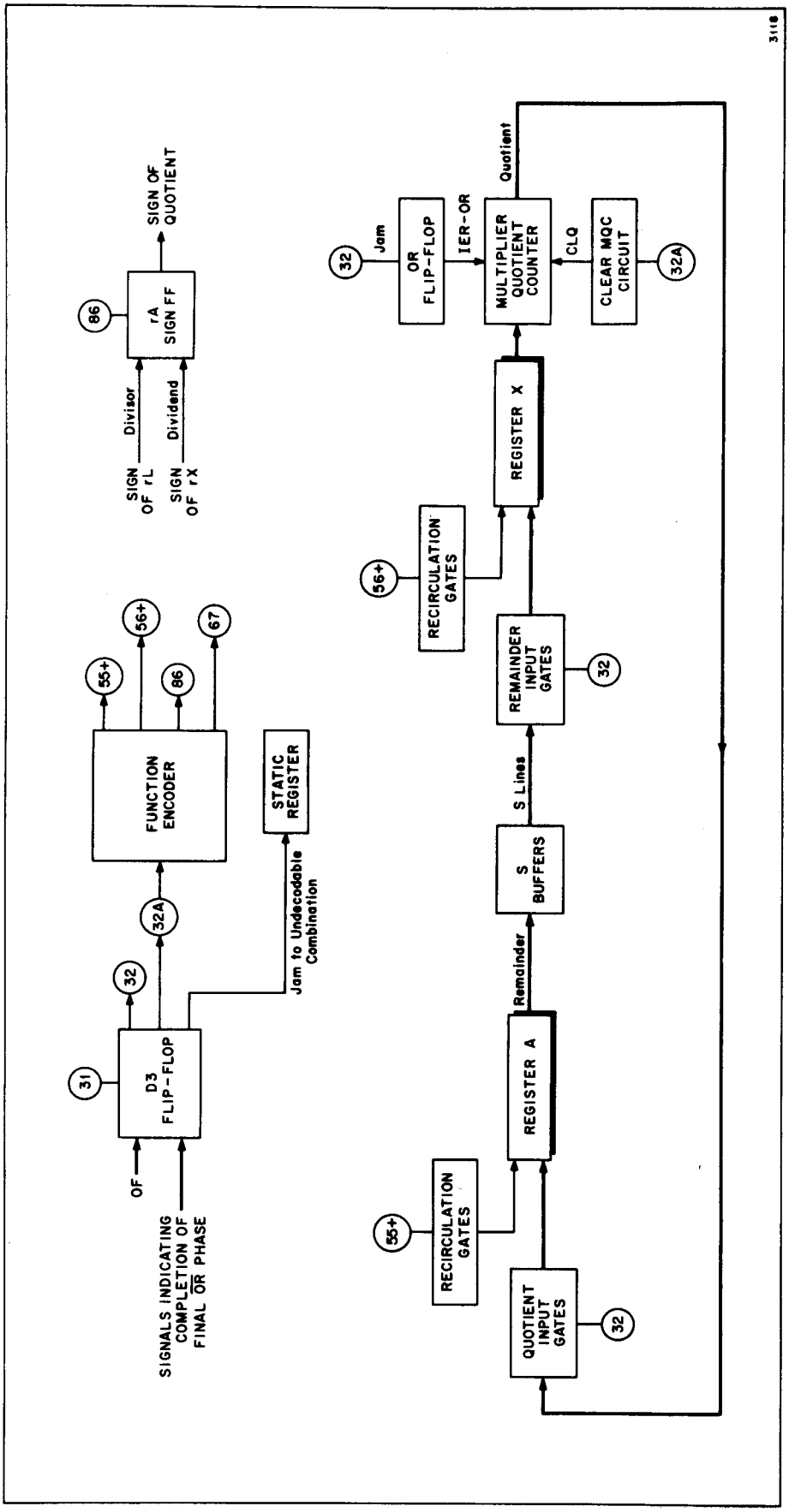


Figure 4-15. D3 Step

Because OF is low, $\overline{OF}$ is high, blocking gate 10 of the OR FF, so that the flip-flop remains restored. Coincidence of these signals at t11B of the tenth OR phase sets the D3 FF, which generates FS 32 at t0B. Function signal 32A is generated at t1A. When the D3 FF is set, it also steps FF5 to a 1 output, resulting in a combination that cannot be decoded by the instruction decoder. As a result, no function signals are generated by the instruction decoder and the D3 FF now generates its own function signals. The flip-flop is restored every word time by the t11B+ signal.

Function signal 32A drives the function encoder to generate FS 55+, 56+, 86, and 67. Function signal 55+ blocks recirculation of rA. The remainder, from rA, goes to the S buffer and the S lines. Function signal 32 alerts the remainder of rX input gates to the S inputs. (Function signal 56+ blocks recirculation in rX. Function signal 32 also generates the IER-OR control signal which alerts the input gates of the MQC flip-flops to the X lines from rX. Function signal 32A clears the MQC flip-flops every pulse time by generating the CLQ clear signal at the clear MQC circuit.)

As the quotient in rX is shifted during the one pulse time of delay supplied by the MQC flip-flops, the remainder on the S lines reads into rX. The outputs of rX are read through the MQC flip-flops. Function signal 32 alerts the quotient input gates of rA to the quotient on the Q lines. Thus the remainder is transferred into rX and the quotient is transferred into rA. Function signal 67 ends the instruction at t11B of the D3 step by generating the EP signal at t9B.

(2) Sign of the Quotient. During the D3 step the sign of the quotient is computed at gates 01 and 02 of the rA sign flip-flop. Function signal 86 alerts these gates to sample the sign of the divisor, which is stored in the rL sign flip-flop, and the sign of the dividend, which is stored in the rX sign flip-flop. The rA sign flip-flop already has been set to A-. If the X and L signs signify a minus sign for the quotient, the rA sign flip-flop remains set to A-. If the X and L outputs signify a plus sign, the flip-flop is restored to store an A+ for the sign of the quotient.

4-37. ERROR CIRCUITS

A constant check on system errors or abnormal conditions in the input-output devices is maintained by four flip-flops: the memory-read error flip-flop, the timing-error flip-flop, the cycling-unit error flip-flop, and the

input-output (I/O) abnormal-condition flip-flop. The signals produced by the setting of any of these flip-flops, except the I/O abnormal-condition flip-flop, set the stop flip-flop. The signal generated by the stop flip-flop blocks the gates of the instruction decoder so that the next instruction staticized in the static register will not be executed until the cause of the condition is remedied and the operator restarts the computer. An error or abnormal condition which develops in one of the input-output devices sets the I/O abnormal-condition flip-flop.

4-38. MEMORY-CHECK FLIP-FLOP

When information is written into main storage the check-bit computer (figure A19) ensures that an odd number of 1 bits is recorded on the drum for each digit. The check-bit computer performs the same check on information read from storage. If the digit read from storage contains an even number of 1 bits, a low CK signal is generated. If the digit contains an odd number of 1 bits, a low $\overline{CK}$ signal is generated. The CK and $\overline{CK}$ signals go to the memory-check flip-flop to indicate whether a 0 or a 1 check bit was necessary when the bit was written on the drum. The value of the check bit being read from the drum is indicated by the DM5 signal output of the read circuits. The check bit is found on the DM55 line during the fast-storage read operation. The memory-check flip-flop is set to a high MRE output (memory read error) to indicate an error under two conditions:

(1) If a 0 checkbit is present, as indicated by the low $\overline{CK}$ signal, and there is a 1 check bit being read as indicated by the low DM5 signal, or

(2) if a 1 check bit is present as indicated by a low CK signal and a 0 check bit indicated by the low DM5 signal.

The memory-check flip-flop can be set to a high MRE output only if the check-timing flip-flop is set. This check-timing flip-flop is set at t0B if the RD signal is present, indicating that the main storage read flip-flop is set. The low output of the check-timing flip-flop alerts gates 53A and 53B of the memory-check flip-flop to sample for check bit error condition.

The high MRE signal lights the MAIN STORAGE and PROCESSOR OFF NORMAL indicators on the control panel and sets the stop flip-flop (figure A5). The high $\overline{SP}$ output of the stop flip-flop goes to the instruction decoder

to block the generation of function signals for the execution of the next instruction until the error condition is remedied. The operator must press the start button generating a high ST (start) signal. This signal restores the memory read error flip-flop to a low MRE output and the stop flip-flop to a low $\overline{SP}$ output. The low $\overline{SP}$ signal enables the instruction decoder to generate function signals which enable the processor to resume operations.

4-39. TIMING-ERROR FLIP-FLOP

The timing-error flip-flop (figure A17) samples the output digits of the timing band read circuits. When originally recorded on the timing band of the drum, each permanent timing combination contains an odd number of 1 bits. The timing-error flip-flop maintains a constant check on the digit outputs of the timing-band read circuits to ensure that each digit contains an odd number of 1 bits. Thus, the operation of the drum and of the read circuits is constantly checked.

Gates 2, 3, 4, and 5 of the timing-error flip-flop test the TS1, TS2, and TS3 outputs of the timing band read circuits. Gates 6 and 7 test the TS4 and TS5 outputs. An even combination of 1 bits alerts two of the gates, setting the flip-flop to a high TE (timing error) output. For example, gates 2 and 6 operate if the TS combination is 0 0000. This combination contains an even number (zero) of 1 bits; therefore an error exists. Gate 2 operates to send a high signal to buffer 14 and then a low signal to gate 9. Gate 6 operates to send a high signal to buffer 16 and then a low signal to gate 9. Both inputs to gate 9 are therefore low, setting the flip-flop to a high TE output.

The timing-error flip-flop is set to a high TE output, indicating an error, under two conditions:

(1) If each of the two groupings of gates receives an even combination, (even + even = even) or,

(2) if each of the two groupings receives an odd combination (odd + odd = even).

A normal-odd input combination in one grouping plus an even input combination in the other grouping (odd + even = odd) puts a high on both set gates and the timing error flip-flop output, TE, remains low. If an error exists the high TE signal lights the TIMING ERROR and PROCESSOR OFF NORMAL indicators on the control panel and sets the stop flip-flop.

4-40. CYCLING-UNIT ERROR FLIP-FLOP

The cycling unit error flip-flop (figure A16) constantly checks the synchronization of the timing combination input to the cycling unit. This combination, TS4, TS3, $\overline{TS2}$ and TS1, must be present at t6B of every word time to properly synchronize processor and input-output operations. If this combination is absent at t6B, the cycling unit error flip-flop generates a signal that stops the processor and indicates the condition on the control panel for remedial action.

Gate 3 of the flip-flop is blocked by the high t6B+ signal at t6B, which is the exact time that the timing combination should be present. At any time other than t6B, the t6B+ signal is low. Therefore, if the bits of the timing combination are low at the gate at any time other than t6B, the gate is permissive, setting the flip-flop. Gates 4, 5, 6, and 7 check the individual bits of the timing combination for synchronization. These gates are alerted by the t6B- signal at t6B. A malfunction is present if any one of the $\overline{TS1}$, TS2, $\overline{TS3}$, and $\overline{TS4}$ signals is low at t6B, since only the timing combination signals should be low at that time. If the input signal to one of these gates is low at t6B, the gate is permissive. This condition again sets the flip-flop to a high CUE output. The low output signal from buffer 11 lights the CYCLING UNIT ERROR and PROCESSOR OFF NORMAL indicators on the control panel and the high CUE signal sets the stop flip-flop.

4-41. INPUT-OUTPUT ABNORMAL-CONDITION FLIP-FLOP

Any abnormal operation of one of the three input-output devices produces a signal that goes to one of the three set gates of the master I/O abnormal-condition flip-flop (figure A2). On the next card cycle or print instruction, the flip-flop is set by the function signal generated by the instruction and the signal that indicates the abnormal condition. For example, abnormal operation of the printer causes a low AOP (Abnormal Operation Printer) signal to be generated. The next print instruction (16 or 11) in the program generates FS 41, which alerts gate 100 to the AOP indication. The permissive gate sets the I/O abnormal-condition flip-flop, generating high Jam I2A and Jam I2B signals. The Jam I2A signal sets FF 1, 2, and 6, to 1 outputs. The Jam I2B signal restores FF 5 and 8 to 0 outputs. This staticizes the second step of a test instruction. The abnormal condition signals, AOT and AOR,

from the read punch and card reader respectively, similarly affect the I/O abnormal-condition flip-flop when the instruction involving these devices is staticized. These signals set the flip-flop, which in turn, jams the STR FF's to the second stage of a test instruction.

This new reading generates function signals that transfer the unexecuted instruction still in rC to rA for storage. The second stage of a test instruction normally transfers the contents of rC to rA and also sets the CT FF so the next instruction is taken from m instead of c. (See I12, under instruction 22, Analysis of Instructions manual.) This setting of the CT FF is prevented by an inhibiting Jam I2B signal which blocks the gate.

The contents of rC is transferred to rA for future use by the programmer. This transfer takes place without clearing rC. Jam I2A ensures that the next instruction is taken from c+1 address by setting the OF FF and restoring the CT FF. The assumption is made that the programmer has stored, in the c+1 address, a routine which brings the computer to a stop.

4-42. MANUALLY-CONTROLLED OPERATIONS

The computer can operate either on a continuous or a noncontinuous basis. Although the computer normally functions in the continuous mode, facilities are provided, mainly for troubleshooting and testing procedures, to operate the computer in the noncontinuous or step-by-step mode.

The operator controls the mode of operation of the computer by depressing one of the six pushbutton lights on the control panel under OPERATION. These buttons light when pushed and are mechanically interlocked so that only one can be pushed at a time. When the CONTINUOUS button is pushed, the computer operates continuously until a programmed stop instruction is staticized in the static register, until an error occurs, or until the operator stops computation by pushing the STOP button. To place the computer in a noncontinuous mode one of the five buttons marked ONE LINE PRINT, ONE CARD RPU, ONE CARD HSR, ONE INSTRUCTION, or COMPARISON STOP must be pushed. The logical operation of the noncontinuous modes is described in the following paragraphs.

4-43. ONE LINE PRINT

When the ONE LINE PRINT button is pushed, the computer stops on the first step of the next advance-and-print instruction. When this button is pushed an EPR signal is generated and sent to buffer 101 of the abnormal-operation-printer flip-flop (figure A35).

When any one of the noncontinuous pushbutton switches is energized, the NC (noncontinuous) signal is generated. The NC signal is used to synchronize the control panel input signal with internal computer signals. It alerts gate 1 of the synchronizing flip-flop which is permissive at t0B if an EW signal is present. Because the NC signal is generated by a manually controlled switch, it may be a weak or partial signal at t0B. The synchronizing flip-flop stores the NC signal for two word times, during which the signal either dies out or builds up into a strong signal.

If the original NC signal dies out, the synchronizing flip-flop is restored and then set again with a strong signal when the next EW signal is available. At the end of the two word times, the signal goes to gate 9 of the IOS FF. Gate 9 is alerted by the EW signal and is permissive at t0B if the input signal is low, setting the flip-flop. The IOS FF generates an IOS signal which is sent to set gates 19, 22, 23, 24, and 25 of the stop flip-flop. Setting the IOS FF generates a high $\overline{\text{IOS}}$ signal which restores the synchronizing flip-flop.

When gate 25 is permissive, it sets the stop flip-flop to low SP and high $\overline{\text{SP}}$ outputs. The $\overline{\text{SP}}$ signal blocks the instruction decoder so that no function signals are generated. When the operator pushes the START button a high ST signal is generated to restore the stop flip-flop.

4-44. ONE CARD RPU

When the ONE CARD RPU button is pushed, the computer stops on the first step of the next card-cycle instruction involving the read-punch unit. When this button is pushed, a TECC signal is generated and sent to buffer 40 of the abnormal-operation-RPU flip-flop (figure A26).

4-45. ONE CARD HSR

When the ONE CARD HSR button is pushed, the computer stops on the first step of the next card-cycle instruction for the card reader. When this button is pushed, an RECC signal is generated and is sent to buffer 73 of the abnormal-operation-reader flip-flop (figure A25).

4-46. ONE INSTRUCTION

When the ONE INSTRUCTION button is pushed, the computer stops after the next instruction is staticized. The operator uses this mode of operation to type information into the computer from the keyboard. When this button is pushed, a staticize-every-minus (SZE-) signal is generated and sent to gate 23 of the stop flip-flop. Function signal 2 alerts gate 23 during the staticize step of the next instruction. When the gate is permissive the stop flip-flop is set.

4-47. COMPARISON STOP

The fifth noncontinuous button, COMPARISON STOP, differs from the other four in that it stops the computer after a Q or T instruction has been executed but before the computer searches for the next instruction. The function of both the Q and T instructions is to compare two quantities and, on the basis of this comparison, to determine whether the next instruction should be taken from the m or the c address. Two illuminated pushbutton switches on the control panel indicate to the operator whether the next instruction to be searched for will be

in the m or c address. When the operator has depressed the COMPARISON STOP button, the computer stops after the comparison is made and the next address has been selected. If the operator wishes to override the address determined by the comparison he pushes the appropriate button. The m or c button changes the state of the CT FF and lights the lamp associated with the chosen address. The RUN button is then pushed and the computer searches for the next instruction.

When the COMPARISON STOP button is pushed a QT Stop signal is generated and sent to gate 24 of the stop flip-flop. The STR signals that make gate 24 permissive are common only to the Q and T comparison instructions. If the inputs to gate 24 are low, the gate is permissive at t10B, setting the stop flip-flop. The t10B signal ensures that the comparison instruction will be completed before the stop flip-flop is set.

4-48. KEYBOARD INPUT

The control panel keyboard enables the operator to change the contents of the arithmetic registers (A, X, or L) by typing in new information. An instruction word also is typed into rC at the keyboard to load the program into the memory at the c address specified in the instruction word. The keyboard consists of ten keys (0 through 9), a KEYBOARD ALERT pushbutton to energize the keyboard, a KEYBOARD READY light, which indicates that the keyboard is ready for use, and two WORD RELEASE pushbuttons labeled + and -. With the latter two pushbuttons, the sign of the word is inserted and the typed word is released from temporary storage into the selected register.

4-49. MANUAL OPERATION

At all times during computation, the contents of one of the four registers, A, C, X, or L, is displayed in lights on the control panel. Forty lights labelled REGISTER CONTENTS display the biquinary combinations of each of the ten digits contained in the register. Two sign lights (+ and -) directly below these 40 lights indicate the sign of the word in the register. The operator selects the register to be displayed by pushing one of four illuminated pushbuttons on the control panel labelled REGISTER SELECTOR. These four buttons, C, A, X, and L, light when depressed and are mechanically interlocked so that only one can be operated at a time.

To type either instruction or data information into the computer, the operator selects a register and stops the computer by pushing the STOP button. When the computer stops, the operator pushes the ONE INSTRUCTION and KEYBOARD ALERT buttons. After a delay of approximately one second, the KEYBOARD READY lamp lights to signal the operator that the keyboard is ready for use. The operator can now type in the word, MSD first. When the complete word is typed, the operator pushes one of the word-release buttons, either + or -. The word is shifted into the selected register and its sign is placed in the proper sign flip-flop. The operator then pushes the CONTINUOUS button and the RUN button.

If a typing error is made, the operator can push one of the word-release buttons to release the word into the register, push the KEYBOARD ALERT button once again, and retype the word.

The operator can depress two keys at the same time to form bit combinations for characters not represented by keys on the keyboard. An alternate method is to type in two complete words. The operator then depresses one of the word-release buttons and the combination of the first and second shifts into the selected register. Here is a list of key combinations that the operator can use:

Biquinary Code	Key Combinations
0101	1 + 4
0110	2 + 4
0111	3 + 4
1101	9 + 1
1110	9 + 2
1111	4 + 8

The word typed into the computer is stored temporarily in four shift registers: read-punch shift register, card-reader shift register, card-reader group counter, and read-punch group counter (figure 4-16.) Each shift register stores 10 bits of the typed 40-bit word. The LSD of the word reads out of the shift registers first, although the operator types in the MSD of the word first. A CLIA-signal, which clears all four shift registers, is generated when the (keyboard alert) button is pushed. Signals necessary to shift the word are generated every time a key is released. When the entire word is typed and stored in the shift registers, the operator pushes one of the two word-release keys to supply the sign of the word and open the path into the selected registers.

4-50. DEPRESSING A KEY

Each time the operator depresses a key to place a digit in the four shift registers, the four-bit code for the desired digit is generated by the keyboard encoder matrix shown in figure A5. The four bits of each digit are distributed onto four output lines. The SCI1 line goes into the read-punch shift register, the SCI2 line goes to the read-punch group counter, the SCI3 line goes to the card-reader shift register, and the SCI4 line goes to the card-reader group counter. Each bit is stored in the first flip-flop of a register. Table 4-4 shows the outputs of the keyboard encoder, which is controlled by the keyboard keys.

Table 4-4. Keyboard Encoder

Keyboard Key	Card-Reader Group Counter SCI_4	Card-Reader Shift Register SCI_3	Read-Punch Group Counter SCI_2	Read-Punch Shift Register SCI_1	UCT Code
0					0000
1				x	0001
2			x		0010
3			x	x	0011
4		x			0100
5	x				1000
6	x			x	1001
7	x		x		1010
8	x		x	x	1011
9	x	x			1100

A high SCI+ signal is generated from the beginning to the end of the keyboard input. The SCI+ signal goes to the card-reader group counter to block the setting of the sample-pulse 1 flip-flop and to the read-punch group counter to block the stepping of the row counter.

4-51. RELEASING A KEY

Each time a key is released a sprocket signal is generated. This signal is synchronized with the timing of computer signals by the EW and t4B- signals which set the sprocket-synchronizing flip-flop. This flip-flop generates a low SPR signal. This SPR signal sets the keyboard input flip-flop (figure A27) at t4B, gate 218 when the EW signal is present. Three signals are generated: a low SCISB, a high SCISA, and a high RSP. The SCISA signal is available for 9 pulse times (t6A to t3A) and in all four registers it shifts each bit of information nine places to the right. The SCISB signal supplies a recirculation path to the two group counters. The other two shift registers are already recirculating. The RSP signal restores the sprocket synchronizing flip-flop.

As a result of the operation of a key the four bits of the first digit stored in the four registers are shifted nine places to the right in all shift registers by the SCISA signal. This signal sends a high signal to the restore gates and a low to the set gates of the ten flip-flops of each register. Section 2-35 explains the operation of a shift register. As a result of this shifting, the four bits of the first digit are placed in the LSD position of the four registers. When the next key is depressed, the four bits of the next digit are stored in the first flip-flop of each register. When the key is released the SCISA signal again shifts the new bits nine places to the right and shifts the previously inserted bits the same number of places. The SCISB signal, sent to the group counters, permits the first bit in each counter to recirculate and become the second lowest order bit of the register. All ten digits of a word are read into the registers and shifted in the same manner. As a result, all digits of the word are in position in the register to be read out LSD first. See table 4-4.

4-52. SIGNING AND RELEASING THE WORD

After all ten digits of a word have been typed, the operator provides the word with a sign and releases the word into the previously selected register by depressing either of the two word-release buttons, labeled + and -. If the plus button is depressed, a WR+ signal is generated. If the minus button is depressed, a WR- signal is generated. The WR+ or WR- signal is stored temporarily in the word-release initial storage flip-flop and then is synchronized with computer timing by the setting of the word-release synchronizing flip-flop. The synchronized signal generated from this flip-flop sets the word-release flip-flop. When set, this flip-flop generates two signals, a high WRA and a low WRB. The WRB signal generates function signals that will open up the path into the selected register on the M lines and gate the information stored in all four registers onto the M lines. The WRA signal supplies the shift pulses needed to shift information out of the four registers.

The WRB signal alerts the DM gates 56A, 56B, 56C, and 56D (figure A5) so the four output lines of shift registers read the contents onto the DM and M lines as follows:

Register	Output	DM line	M line
Read-punch shift register	SR2	DM11	M1
Read-punch group counter	TG10	DM21	M2
Card-reader shift register	SR1	DM31	M3
Card-reader group counter	G10	DM41	M4

The WRB signal also goes to the generate-instruction gates 57, 58, 59 and 60 (figure A5), only one of which has been alerted. One of the RSC, RSA, RSL, or RSX signals alerts one of the gates, depending on which register has been selected by the operator. If the RSC signal has been generated, a generate-beta signal is produced. If the RSX signal has been generated, a generate-Y signal is produced. If the RSL signal has been generated, a generate-L signal is produced and if RSA signal has been generated, a generate-B signal is produced.

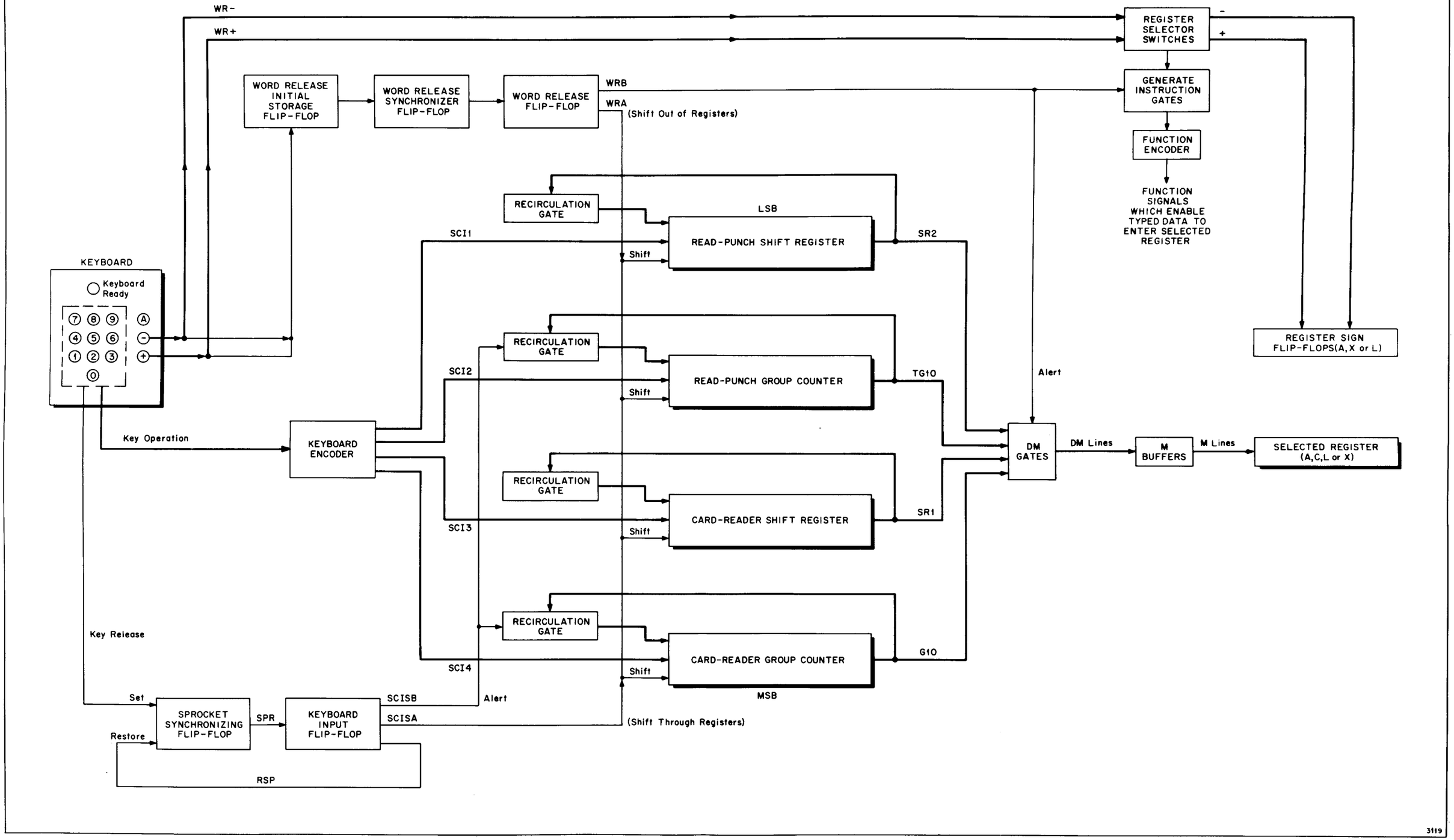


Figure 4-16. Keyboard Input Operation

One of these four signals is sent to the function encoder to generate function signals that perform the instruction required to store the input data in the selected register. (Function signal 67, however, is not generated because the static register is not involved.) The WRB signal also is sent to gate 15 on the static register to generate an ending pulse if FS 2 is present.

The WRA signal is sent to all four shift registers to place a high signal on the restore gates and a low on the set gates to shift the contents out of the registers. The WRA signal also is sent to the keyboard input flip-flop to generate an RSP signal which restores the word-release initial-storage and word-release synchronizing flip-flops.

The signal generated when an arithmetic register is selected (RSA, RSX, or RSL) is combined with either the WR+ or WR- signal to generate one of the following signals: WRA-, WRA+, WRX-, WRX+, WRL-, WRL+. These signals go directly to the rA, rX, or rL sign flip-flops to store the correct sign in the correct flip-flop. If rC is selected to receive the word typed in, no sign is involved.

SECTION V

INSTRUCTIONS

5-1. INTRODUCTION

There are 32 instructions in the repertoire. Eight are input-output instructions described in other manuals. The remaining instructions, concerned with operations internal to the processor, are described in this section and in section IV of this manual. Appendix C lists all the instructions numerically.

The descriptions of instructions in this section are arranged as follows:

(1) Input-output instructions

(2) Arithmetic instructions

(3) Transfer instructions

(4) Translate instructions

(5) Miscellaneous instructions

(6) Comparison instructions

(7) Test instructions

Section IV of this manual, Theory of Operation, describes in detail the search and staticize instruction steps that are common to all instructions. Section IV also explains the execution steps of the 60(H) transfer instruction, and the arithmetic instructions: 70(A), add; 75(S), subtract; 85(M), multiply; and 55(D), divide. A thorough knowledge of the five instructions and the basic search and staticize sequence should provide the reader with the necessary background for understanding the less detailed descriptions in this section. The execution sequence for the remaining six transfer instructions and the translation, comparison, miscellaneous, and input-output test instructions are described in this section at a block diagram level. The reader may assume that the initial search and staticize instruction steps have been completed and that both the text and the figures in this section refer to the execution sequences.

To trace in detail the execution of the instructions described in this section, refer to Analysis of Instructions, a manual which describes briefly the steps in each instruction and the effect of the control signals generated by the instructions. Section III of this manual, Description of Central Processor Components, gives a functional description of the logical circuits that are mentioned both in this section and in the manual Analysis of Instructions.

Instructions are designated in this manual by both an alphabetic notation, used on the logical drawings, and a numeric notation, used chiefly in programming; for example, instructions are designated: 70(A), 85(M).

5-2. INPUT-OUTPUT INSTRUCTIONS

Input-output instructions are used to control the transfer of information to and from the input-output devices, as well as to control the movement of cards, the selection of output stackers, and so forth. Because a thorough understanding of these instructions requires knowledge of the input-output devices, each input-output instruction is described in detail in the separate manual for the device with which it is associated, as follows:

Type 7902 Card-Sensing Punch Unit, 90 Column

46(W11) instruction
57(Z1) instruction
81(W21) instruction

Type 7904 Card-Sensing Unit, 90 Column

47(Z2) instruction
72(CC) instruction
96(W31) instruction

Type 7901 High-Speed Printer

11(PR1) instruction
16(PF1) instruction

For convenience, these instructions are listed numerically in appendix C of this manual.

5-3. ARITHMETIC INSTRUCTIONS

The four arithmetic instructions, 70(A), 75(S), 85(M), and 55(D), are described in detail in section IV of this manual.

5-4. TRANSFER INSTRUCTIONS

There are seven transfer instructions that are internal to the processor. They are the 60(H), 65(X), 50(J), 25(B), 05(Y), 30(L), and 77(K) instructions.

5-5. THE 60(H), 65(X), AND 50(J) INSTRUCTIONS

These instructions transfer information from a register in the processor to a main storage location. The 60(H) instruction, which transfers the contents of register A to a main storage location, is described in detail in section IV. The 65(X) and 50(J) instructions are similar to the 60(H) instruction except that they transfer the contents of register X and register L, respectively, to main storage locations.

5-6. THE 25(B), 05(Y), AND 30(L) INSTRUCTIONS

These instructions transfer information from a main storage location to a register in the processor. The 25(B) instruction transfers the contents of a main storage location to register A. The 05(Y) and 30(L) instructions are similar to the 25(B) instruction except that they transfer the contents of a main storage location to register X and register L, respectively.

5-7. THE 25(B) INSTRUCTION. During the execution step of the 25(B) instruction (figure 5-1), the recirculation gates of register A are blocked so that the new word from storage can enter the register. The word from storage is read by the read amplifiers, goes through the M buffers, and enters the register-A input gates. A blocking signal into the S buffers forces the S lines low so that the input gates are permissive to information on the M lines only. The sign of the word from storage enters the rA sign flip-flop as shown in figure 5-1. When the entire word from storage is in the register, the blocking signal on the recirculation gates is removed so that the word can recirculate in the register.

5-8. THE 77(K) INSTRUCTION

The 77(K) instruction transfers the contents of register A to register L and is the only register-to-register transfer instruction. Because this instruction does not involve a search for an operand, the m-address portion of the instruction is ignored.

5-9. TRANSLATE INSTRUCTIONS

There are two translate instructions. The 12(G) instruction translates one word from card code to UCT code, and the 17(R) instruction translates one word from UCT code to card code. The input-output devices operate with card code, while the processor performs arithmetic operations only with UCT code. See section I, Introduction, for details about the codes.

5-10. THE 12(G) INSTRUCTION

The 12(G) instruction translates the contents of registers A and X from card code to UCT code. If it is desired to perform arithmetic operations on information read by the card reader or read-punch device, the 12(G) instruction must first be given in order to translate the information from the card code used by the input-output devices to the UCT code used by the processor.

Information read in card code from punched cards by the card reader or read-punch device is eventually stored in main storage. Each word of information in the 6-bit card code must be divided into two parts, called the primed and unprimed parts, in order to store it on the storage drum, which normally stores the 4-bit UCT code. The unprimed part is stored in one location which normally stores a complete UCT-coded word, and the primed part is stored in another location. The division of each word in card code into primed and unprimed parts is accomplished automatically when the programmer transfers the information from the card-buffer band to main storage. This operation is described in detail in the read-punch manual and in the card reader manual.

In order to translate a word from card code to UCT code, the programmer gives the appropriate transfer instructions to transfer the unprimed part of the word to be translated from its main storage location to register A and the primed part from its main storage location to register X. When a 12(G) instruction is given, the unprimed part of the word in register A is sent to the S buffer and then to the translation gates of rA; this information does not recirculate in rA because the recirculation gates are blocked. At the same time, the primed part of the word in rX is sent to the M buffers and then to the translation gates of rA. The recirculation gates of rX are also blocked. See figure 5-2.

After the complete card-coded word is translated into UCT code, the blocking signal on the recirculation gates of rA is removed to allow the newly formed UCT-coded word to recirculate in rA. Register X remains cleared to all zeros. The sign of the UCT-coded word in rA after translation is the sign of the unprimed part of the card-coded word that was in rA before translation.

5-11. THE 17(R) INSTRUCTION

The 17(R) instruction translates the contents of register A from UCT code to card code. The programmer places the UCT-coded word which is to be translated in register A. When a 17(R) instruction is given, the word is sent to the S buffers and then to the translation gates of registers A and X (figure 5-3), but it does not recirculate in register A because the recirculation gates are blocked. The unprimed part of the translated word goes to register A; the primed

part of the translated word goes to register X. After the complete word is translated, the blocking signals on the recirculation gates of both registers are removed so that the unprimed and primed parts of the word can circulate in rA and rX respectively. The programmer then transfers the primed and unprimed parts of the word to main storage by giving the appropriate transfer instructions. During the translation process, both the rA and rX sign flip-flops are forced to a plus condition.

5-12. MISCELLANEOUS INSTRUCTIONS

Six instructions have been grouped in the miscellaneous category. These are: the 20(P) superimpose instruction; the 35(E) extract instruction; the 32(N) shift-right instruction; the 37(V) shift-left instruction; the 62(ZS) zero suppress instruction; and the 67(STOP) instruction.

5-13. THE 20(P) SUPERIMPOSE INSTRUCTION

The 20(P) instruction superimposes the 1 bits of the word in the m-address location on the word in register A. The result is a new word in register A containing a 1 bit where either the original word in rA or the word from storage had a 1 bit. The sign of the original word in rA is not changed.

This instruction is used when it is desired to combine the information in one word with the information in another word so that the new word contains the information of both. Often the information in one word must be combined with many other words, so that the information to be superimposed is placed in storage as a constant.

As shown in the block diagram of the 20(P) instruction (figure 5-4), the word of information in rA is allowed to circulate in register A through the recirculation gates. At the same time, the word from storage enters rA on the M lines from the M buffers through the input gates of rA. The S buffers are blocked so that the rA input gates are permissive to information on the M lines only. Thus, the 1 bits in register A are allowed to recirculate into the register through the recirculation gates and the 1 bits in the word from storage are allowed to enter the register through the input gates.

5-14. THE 35(E) EXTRACT INSTRUCTION

The 35(E) instruction changes 1 bits to 0 bits in each decimal digit of the word in register A whenever there is a 0 bit in the corresponding bit position of the word in the main storage location designated by the m address. The sign of rA is not changed.

This instruction is referred to as the extract instruction because it is used to extract certain digits from a word in rA. In the extract word placed in storage by the programmer, each bit of each digit contains a 1 bit where the corresponding digit in rA is to be unchanged, and a 0 bit where it is to be changed to 0.

For example, to extract the five most significant digits of the word in rA by changing the five least significant digits to zeros, the programmer places the extract word .....00000 in storage. When an extract instruction that contains this extract word as the m address is given, the 0 bits in each bit position of the five least significant digit positions change these digits to zeros in the word in rA. Since the UCT code for a period is 1111, or four 1 bits, there are no 0 bits in the five most significant digit positions of the extract word, and the corresponding digits in the original word in rA remain unchanged.

As figure 5-5 shows, this instruction is similar to the 20(P) instruction. In the 35(E) instruction, however, the word in rA does not recirculate because the recirculation gates are blocked. Instead, it is sent to the S buffer, so that it is on the S lines at the same time that the extract word from storage is on the M lines. Corresponding digits of both words, therefore, are at the input gates of register A at the same time. (See section 3-15.) The new word formed in rA as a result of this instruction contains 1 bits only in the bit positions where the S and M lines had 1 bits in corresponding bit positions.

5-15. THE 32(N) SHIFT-RIGHT INSTRUCTION

The 32(N) instruction shifts the contents of register A to the right a designated number of places into rX and at the same time shifts the contents of rX to the right into register A. The number of places shifted can vary from zero through ten. A single digit in the p7 digit position of the m address of the instruction word indicates the number of places to be shifted. (The p7 position is the next to most significant digit of the m address.) The bit-code combination 1101 is used to indicate 10 in this instruction.

During the staticize step of every instruction, the p7 digit of the m address is placed in the multiplier-quotient counter (MQC), so that it is available if the instruction is a shift instruction.

There are two execution steps in the 32(N) instruction: N1 and N2. During the N1 step (figure 5-6), the digit in MQC (the p7 digit of the m address) is examined. If the digit in MQC is a zero, an ending pulse clears the static register to all zeros so that there is a search for the next instruction. If the digit in MQC is not a zero, the static register is stepped to the N2 step of the 32(N) instruction.

During the N2 step of this instruction, the contents of rA and rX are shifted to the right by blocking the normal recirculation gates of rA and rX, and circulating the contents of rA and rX through a shortened loop. During the N2 stage the contents of rA and rX are circulated through the shortened loop the number of times indicated by the digit in MQC. During each circulation, the contents of both rA and rX are shifted one place to the right (figure 5-6). A circular shift operation also takes place: the least significant digit (LSD) of rA becomes the most significant digit (MSD) of rX and the LSD of rX becomes the MSD of rA. During each shift operation the count-down gates of MQC count down one until the digit in MQC is zero. A zero in MQC generates an ending pulse.

5-16. THE 37(V) SHIFT-LEFT INSTRUCTION

The 37(V) instruction shifts the contents of rA to the left a designated number of places. The most significant digits are lost and zeros are placed in the least significant digit places. The number of places shifted can vary from zero through ten. The code combination 1101 is used to indicate 10 in this instruction.

There are two steps to the 37(V) instruction: V1 and V2. During the V1 step (figure 5-7), the digit in MQC is examined. The digit in MQC is the p7 digit of the m address, placed in MQC during every staticize instruction step. If the digit in MQC is a zero, an ending pulse clears the static register so that there is a search for the next instruction. If the digit in MQC is not a zero, the static register is stepped to the V2 step of the 37(V) instruction.

During the V2 step, the normal recirculation gates of rA are blocked and the contents of rA is shifted to the left by circulating it through a lengthened loop. The contents of rA is delayed one pulse time in the loop before it reaches the left shift gates, so that the entire contents of rA shifts one place to the left each time it circulates. The binary bit of each digit is delayed by adding one pulse time in subregister 4 of rA. The quinary bits are delayed one pulse time by sending them through the S buffers and the complementing circuit, and then back into rA. (The bits are only delayed in the complementing circuit, not complemented.) As a result of each left shift of one digit position, the most significant digit is lost and a zero appears in the least significant digit position. During each shift operation the count-down gates of MQC count down one until the digit in MQC is zero. A zero in MQC generates an ending pulse.

5-17. THE 62(ZS) ZERO SUPPRESS INSTRUCTION

The 62(ZS) instruction suppresses all the card-coded punching or printing zeros and commas (and only zeros and commas) to the left of the most significant digit and replaces them with non-punching or non-printing zeros. The m portion of the instruction word is ignored because there is no search for an operand in this instruction. Suppressing means that a code combination which would cause a zero or comma to be punched on a card or printed by the printer is changed so that the code combination causes a space on the card or the printed paper.

All output information which is to be printed by the printer or punched by the read-punch device must be in card code. When information is translated from UCT code to card code before going to the input-output devices, all UCT-coded zeros are translated into card-coded punching or printing zeros. The card code for a punching or printing zero is 000001. (See section 1-15 for an explanation of the card code.) The combination 000001 causes a hole to be punched in the zero row of the card, or causes the printer to print a zero. The zero suppress instruction changes the binary one of the combination 000001 to zero, creating the non-printing and non-punching combination 000000.

In addition to suppressing all zeros to the left of the most significant digit, the 62(ZS) instruction suppresses all commas to the left of the most significant digit. The instruction changes 000011, the code combination for a comma, to 000000. Since a result may have a large number of digits, commas are often programmed into words. For example, 75875875 is printed or punched as 75,875,875. However, if the number 00,000,875 is to be printed or punched, a zero suppress instruction removes the five zeros and two commas to the left of the most significant digit, and 875 is printed or punched.

During a zero suppress instruction, the unprimed part of the word to be suppressed must be in register A. Since each digit of the unprimed part consists of the four lower order bits, the unprimed part of the word fills register A. However, each digit of the primed part consists only of the two higher order bits and these occupy subregisters 1 and 2 of rX. Because subregister 3 is not used to circulate information, it is used temporarily as a special storage device during the execution of the zero suppress instruction. Register X, therefore, should contain only the primed part of the word.

Figure 5-8 shows the two steps of the zero suppress instruction: ZS1 and ZS2. During ZS1, the unprimed part of the word in rA is sent through the zero suppress and comma suppress gates of rX. The gates, which are connected only to subregister 3 of rX, place a binary zero in subregister 3 wherever there is a punching or printing zero (000001) or comma (000011) in the corresponding digit position of rA. They place a binary one in subregister 3 for every character other

than a zero or a comma. When the entire contents of rA has been examined, the static register is stepped to ZS2.

During the ZS2 step, the word in rA recirculates through the normal recirculation gates. Subregister 3 of rX is designed so that the outputs of each of the ten bits in the subregister are available in parallel. These ten outputs are inputs to the zero suppress gate of rA. The output of the rA zero suppress gate is an input to two of the normal recirculation gates of rA. As long as a binary one in subregister 3 of rX indicates that there are still significant digits to enter rA, the zero suppress gate of rA is blocked so that the output of this gate keeps the normal recirculation of rA permissive to the recirculating digits. A blocking signal on the normal recirculation gate of subregister 3 of rX prevents the bits from reentering the subregister. When there are no longer any binary ones in the subregister, the zero suppress gate of rA is made permissive and its output blocks the normal recirculation gates of rA so that all the 1 bits of the remaining digits of the word in rA (which are zeros or commas) are changed to 0 bits. That is, all remaining zeros and commas are suppressed.

5-18. THE 67(STOP) INSTRUCTION

The 67(STOP) instruction stops the processor. When this instruction is in the static register, it generates a signal which sets the stop flip-flop and clears the static register to zeros. The stop flip-flop generates a signal which is sent to the instruction decoder and prevents the generation of any function signals.

With the static register cleared to zeros and no function signals being generated, the 67 instruction word (which includes the m and c address) continues to circulate in register C. The processor is started again by pressing the RUN button, one of the two COMPUTATION buttons on the control panel. The next instruction is at the m address if the NEXT ADDRESS button for the m address is lit; at the c address if that NEXT ADDRESS button is lit. The operator may select the next address by pressing either NEXT ADDRESS button, however. The buttons control the conditional-transfer (CT) flip-flop.

5-19. COMPARISON INSTRUCTIONS

There are two comparison instructions which compare the contents of register A and register L and, as a result of the comparison, direct the processor either to the m address or to the c address. The 82(Q) instruction compares for the equality or inequality of the contents of registers A and L. The 87(T) instruction compares for greater-than and less-than conditions.

The processor can be stopped after the execution of an 82(Q) or an 87(T) instruction by pressing the COMPARISON STOP button on the control panel. When this button is pressed, one of the NEXT ADDRESS pushbuttons lights to indicate whether the next instruction is to be taken from the main storage location indicated by the m address or the c address. The operator can change the address determined by the comparison, by pushing the other NEXT ADDRESS button. The comparison stop operation is explained in detail in section 4-47.

5-20. THE 82(Q) INSTRUCTION

The 82(Q) instruction compares the contents of register A with the contents of register L. If (rA) and (rL) are algebraically equal, the next instruction is in the storage location designated by the m address. If (rA) and (rL) are not algebraically equal, the next instruction is in the storage location designated by the c address.

Figure 5-9 is a block diagram of the 82(Q) instruction. The state of the conditional-transfer (CT) flip-flop determines which address is to be read from storage. If the CT flip-flop is set, the m address is read from storage; if the CT flip-flop is restored, the c address is read from storage. At the beginning of the instruction, the CT flip-flop is set. If (rA) and (rL) are equal, the CT flip-flop remains set at the end of the comparison and the m address is read from storage. If, however, (rA) and (rL) are not equal, the CT flip-flop is restored and the c address is read from storage.

As shown in figure 5-9, (rA) and (rL) are sent to the binary and quinary equality gates on the M and S lines, (rA) on the S lines and (rL) on the M lines. The binary equality gates sample for the equality of the binary bits of each digit on the M and S lines, while the quinary equality gates sample for equality of the quinary bits of each digit on the M and S lines. See sections 3-54 and 3-57 for a detailed explanation of these circuits.

In addition to the M and S lines, the binary and quinary equality circuits of the comparator have, as an input, the CP signal from the complement flip-flop. The complement flip-flop is set at the beginning of the comparison operation so that the CP signal alerts the binary and quinary equality gates during the word time that (rA) and (rL) are compared.

The quinary equality gates also have the A and C signals as inputs. When the complement flip-flop is set at the beginning of the comparison operations, it generates a CP5 signal for one pulse time. The CP5 signal is sent to the initial force-decimal-carry circuit (section 3-58), where it initially generates the A and C signals so that the quinary equality gates are permissive to the bits of the first digit to be compared for equality on the M and S lines. For example, suppose the words being compared are as follows:

(rL) on M lines 0000006917

(rA) on S lines 0000006917

The initial generation of the A and C signals by the initial force-decimal-carry circuit makes the quinary equality gates permissive to the two sevens, the first two digits to be compared. Because they are equal, the comparison of the two seven digits results in the generation of the A and C signals again. Because all succeeding digits are equal, the A and C signals continue to be generated and are present at the end of the comparison.

There are four gates which can restore the CT flip-flop during the 82(Q) instruction. (See Analysis of Instructions for gate numbers.) The outputs of the binary and quinary equality circuits (the $\overline{EQ}$ and $\overline{A'}$ signals) are sent to two of the four restore gates, to restore the CT flip-flop if either the binary or the quinary part is not equal. During this instruction, the other two restore gates of the CT flip-flop have as inputs the outputs of the rA and rL sign flip-flops, to restore the CT flip-flop if the signs of (rL) and (rA) are not the same.

5-21. THE 87(T) INSTRUCTION

The 87(T) instruction compares the contents of registers A and L. If the contents of register A is algebraically greater than the contents of register L, the next instruction is in the storage location designated by the m address. If (rA) is algebraically less than or equal to (rL), the next instruction is in the storage location designated by the c address.

Figure 5-10 is a block diagram of the 87(T) instruction. The condition of the CT flip-flop determines which address is read from storage. If the CT flip-flop is set, the m address is read from storage; if the CT flip-flop is restored, the c address is read from storage. The CT flip-flop is set at the beginning of the comparison operation. If (rA) is greater than (rL), the CT flip-flop remains set at the end of the comparison and the storage location designated by the m address is read. If, however, (rA) is less than or equal to (rL), the CT flip-flop is restored and the storage location designated by the c address is read from storage.

The contents of rA and rL are compared during the 87(T) instruction in the quinary equality gates (section 3-54), the binary equality gates (section 3-57), the force-decimal-carry gates (section 3-56) and part of the quinary carry circuit (section 3-55). The M and S lines are inputs to all of these circuits. During the T instruction, the contents of rA is sent to the circuits on the S lines and the contents of rL is sent on the M lines. Several of the circuits have the CP signal as an input. Since the CP flip-flop is set at the

beginning of the comparison operation, the circuits which have CP as an input are permissive to information on the M and S lines.

The binary and quinary equality gates sample for the equality of digits on the M and S lines in this instruction as they do in the 82(Q) instruction. Gate 31 of the force-decimal-carry circuit (figure A12) samples for whether the binary bit on the M line is greater than the binary bit on the S line. The part of the quinary circuit consisting of gates 33, 34, and 46 through 56 samples for whether the digit on the M lines is greater than the digit on the S lines.

Table 5-1 shows all conditions for comparing (rA) and (rL). Whether the CT flip-flop remains set or is restored depends upon whether the A and C signals are present at the completion of the comparison. The restore gates of the CT flip-flop during the 87(T) instruction have as inputs the $\overline{A}$ and C signals (gate 13) or the $\overline{C}$ signal (gate 14) or the $\overline{A}$ signal (gate 15). (See Analysis of Instructions.) Table 3-3 shows which gate operates to restore the CT flip-flop under each of the conditions in table 5-1.

As indicated in table 5-1, gate 32 of figure A12 initially generates the decimal-carry signals (A and C) if the sign of (rA) is plus. If (rA) is minus the A and C signals are not initially generated. The initial generation of the A and C signals when (rA) is plus but not when (rA) is minus affects the conditions under which the CT flip-flop remains set or is restored.

As shown in table 5-1, there are two conditions under which the CT flip-flop is restored when rA is plus: when (rA) equals (rL), and when (rA) is less than (rL). If (rA) equals (rL), the binary and quinary equality gates continue to generate the A and C signals, which restore the CT flip-flop at the end of the comparison.

If (rA) is less than (rL), the A and C signals are again present at the end of the comparison, but they are generated by the gates which indicate (rA) is less than (rL) (section 3-55). For example, suppose the two words being compared are as follows:

(rL) on M lines 0000007809

(rA) on S lines 0000007431

When the nine and the one are compared, A and C signals are generated because rA is less than rL. When the zero and the three are compared, the A and C signals are lost because rA is greater than rL and there are no gates to generate A and C signals under this condition. When the two most significant non-equal digits, the eight and four, are compared, A and C signals are again generated by the gates of the

Table 5-1. State of Conditional-Transfer Flip-Flop After Comparison Operation

When the flip-flop is set, the m address is read. When the flip-flop is restored, the c address is read.

Sign*		Absolute Value		
(rA)	(rL)	(rA) > (rL)	(rA) = (rL)	(rA) < (rL)
+	+	set	restored	restored
+	-	set	set	set
-	+	restored	restored	restored
-	-	restored	restored	set

*When the sign of (rA) is plus, gate 32 generates initial decimal-carry signals. When the sign of (rA) is minus, no initial decimal-carry signals are generated.

quinary-carry circuit which indicate rA is less than rL. The A and C signals thus generated make the quinary equality gates permissive so that the succeeding digits, which are all equal, continue to generate the A and C signals, which restore the CT flip-flop at the end of the comparison.

Table 5-1 shows that when (rA) is minus, there is only one condition for which the CT flip-flop remains set: when both (rA) and (rL) are minus, and (rA) is less than (rL). When (rA) is less than (rL), the gates which indicate the contents of rA is less than the contents of rL generate the A and C signals and the CT flip-flop is not restored. For example, suppose the two words being compared are as follows:

(rL) on M lines 0000005924

(rA) on S lines 0000005384

The A and C signals are not generated until the two most significant non-equal digits, the nine and the three, are compared, when the gates which indicate that rA is less than rL generate the signals. Because the A and C signals are not initially generated, the equality gates are blocked and the A and C signals are not generated when the two fours are compared. They are not generated when the eight and the two are compared, because there are no gates which indicate (rA) is greater than (rL). However, when the nine and the three generate the A and C signals, the biquinary equality gates are made permissive and the A and C signals continue to be

generated because all remaining digits of this example are equal.

5-22. TEST INSTRUCTIONS

Three input-output test instructions are provided, one for each of the three input-output devices. The programmer uses these instructions to determine whether a particular input-output device is available or whether it is still processing a previous instruction. For example, the input-output test for the printer tests to determine if the printer is free to accept a print order or is still processing a previous print order. If the printer is not available to process a print order, the processor is free to continue the main program, instead of waiting until the printer is available. This is a saving in computing time. The instructions are distributed throughout the program to test the availability of the input-output devices at convenient intervals.

Each of the three input-output instructions has two stages. The first stage tests whether the device is available. If it is not available, an ending pulse is generated and the processor goes to the c address, the address of the next instruction. Because each of the three instructions tests a different device, the first stage of each instruction is different.

If the test performed during the first stage shows that the device is available, the static register is stepped to the second stage. The second stage of each test instruction is identical. (See figure 5-11.) During this stage, the contents of register C is transferred to register A, and the next instruction is read from the m address. Register C contains the c address, the address of the next instruction of the main program. It is put in register A because the processor must return to it in order to continue to process the program. The m address to which the processor is directed can contain a subroutine which transfers the c address of the test instruction from register A to storage, gives one of the input-output instructions, and returns the processor to the main program.

5-23. THE 22 (I 11) INSTRUCTION

The 22 (I 11) instruction tests to determine whether the card buffer band is loaded with information from the read-punch device. If the card buffer band is not loaded from the read-punch device, the next instruction is in the storage location designated by the c address. If the card buffer band is loaded from the read-punch unit, the next instruction is in the storage location designated by the m address, and the contents of register C is transferred to register A.

Item 1 of the instruction analysis for the 22 (I 11) instruction lists the signals in the first stage, during which the test is made to determine whether or not the buffer is loaded from the read-punch device. If the buffer band is not loaded from the read-punch device, an ending pulse is generated. If the buffer band is loaded from the read-punch device, the static register is stepped to the second stage of the instruction (items 2 through 9 of the instruction analysis). The second stage of this instruction, which is common to all the input-output test instructions, is shown in block diagram form in figure 5-11.

5-24. THE 27 (I 21) INSTRUCTION

The 27 (I 21) instruction tests to determine whether the printer is printing or feeding paper. If the printer is printing or feeding paper, the next instruction is in the storage location designated by the c address. If the printer is not printing or feeding paper, the next instruction is in the storage location designated by the m address and the contents of register C is transferred to register A.

Item 1 of the instruction analysis of the 27 (I 21) instruction lists the signals in the first stage, during which the test is made to determine whether or not a printing or paper feeding operation is taking place. If the printer is occupied, an ending pulse is generated. If the printer is available, the static register is stepped to the second stage of the instruction (items 2 through 9 of the instruction analysis). The second stage, which is common to all the input-output test instructions, is shown in block diagram form in figure 5-11.

5-25. THE 42 (I 31) INSTRUCTION

The 42 (I 31) instruction tests to determine whether the card buffer is loaded with information read by the card reader. If the buffer band is not loaded from the card reader, the next instruction is in the storage location designated by the c address. If the card buffer band is loaded from the card reader, the next instruction is in the storage location designated by the m address and the contents of register C is transferred to register A.

Item 1 of the instruction analysis lists the signals in the first stage, during which the test is made to determine whether or not the buffer band is loaded from the card reader. If the buffer band is not loaded from the card reader, an ending pulse is generated. If the card buffer band is loaded, the static register is stepped to the second stage of the instruction (items 2 through 9 of the instruction analysis). The second stage, which is common to all the input-output instructions, is shown in block diagram form in figure 5-11.

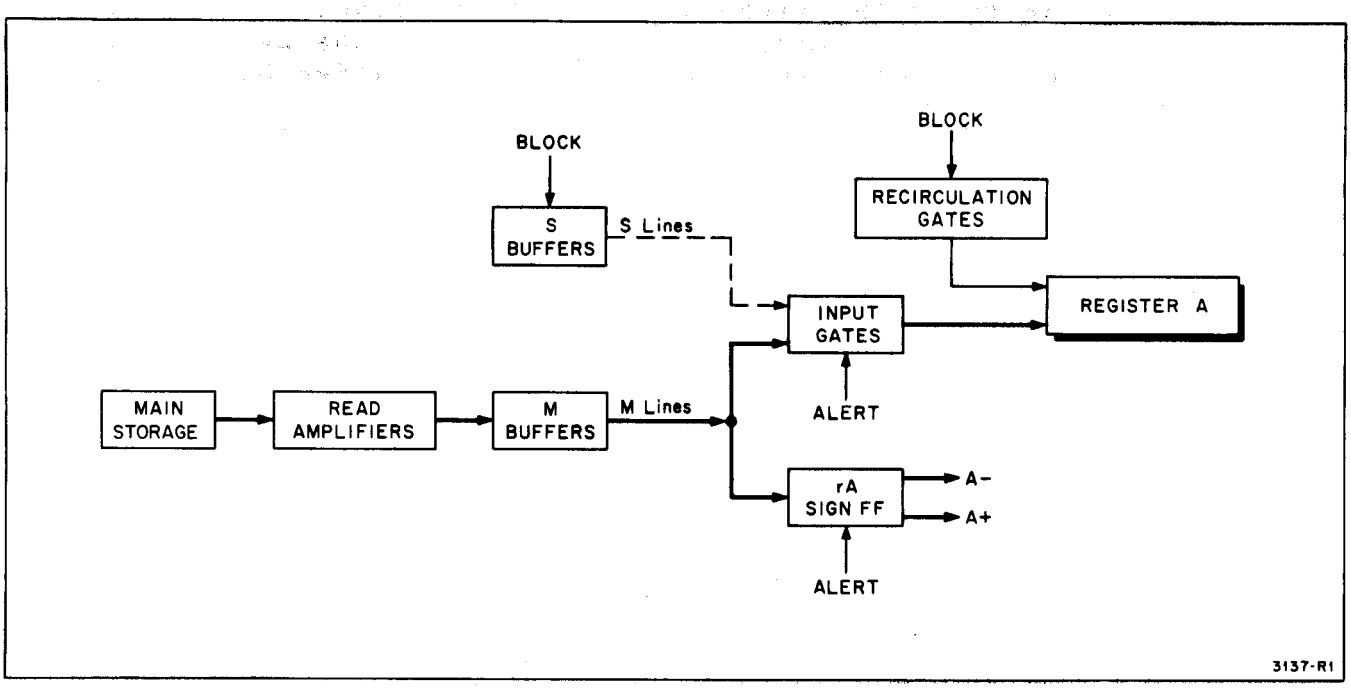


Figure 5-1. The 25(B) Transfer Instruction ((m)--->rA)

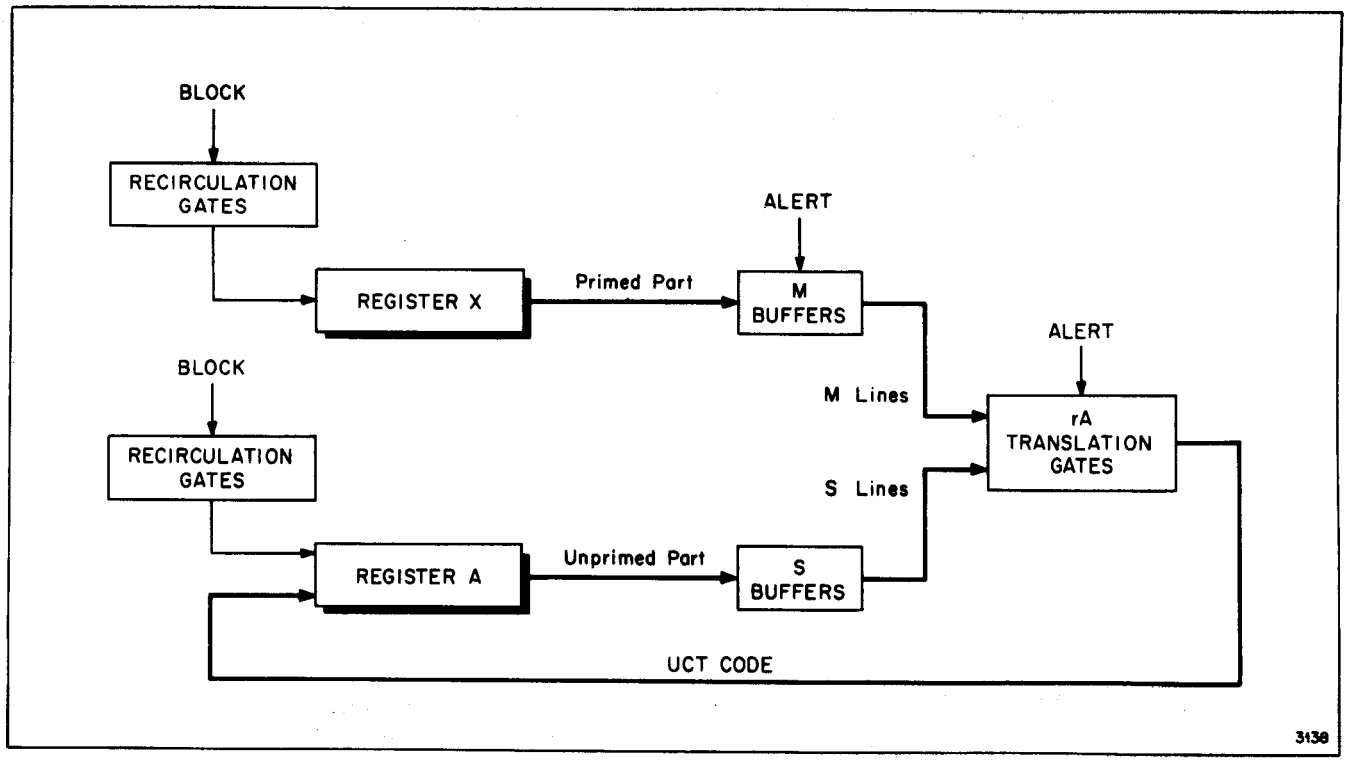


Figure 5-2. The 12(G) Translate Instruction (Card Code to UCT Code)

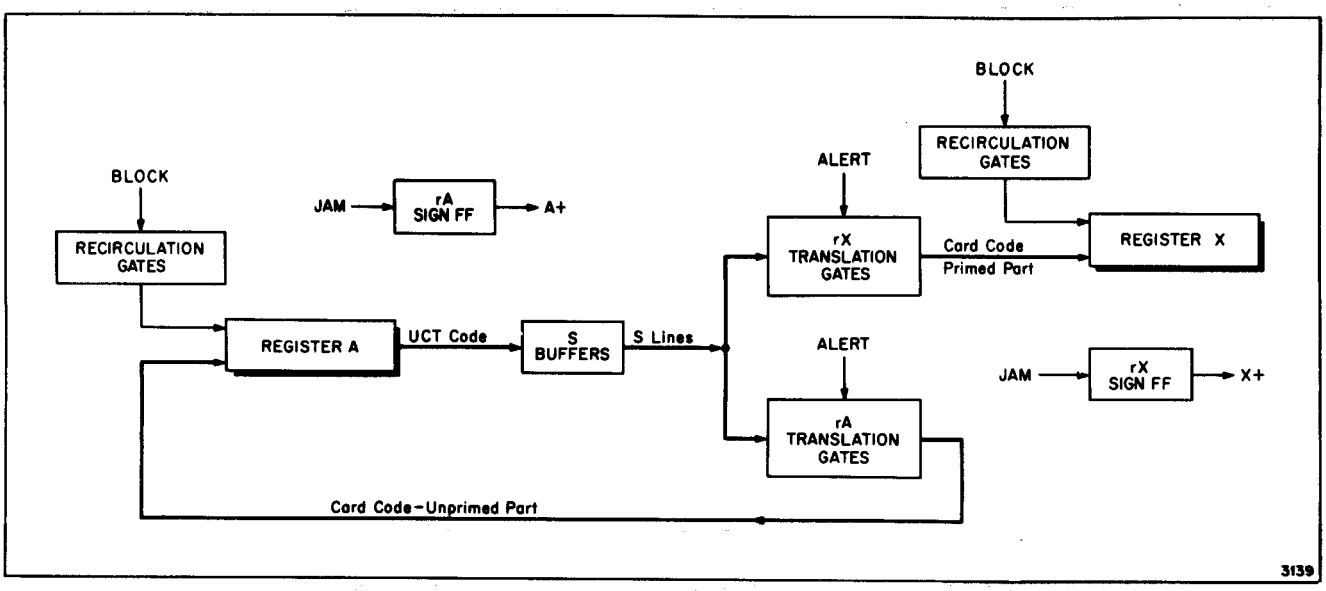


Figure 5-3. The 17(R) Translate Instruction (UCT Code to Card Code)

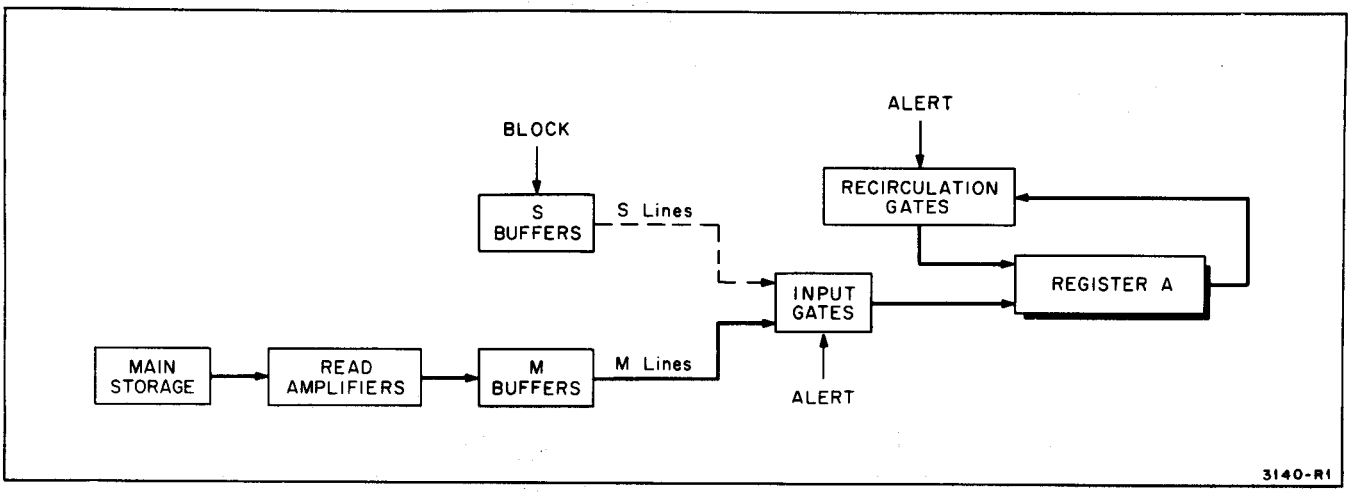


Figure 5-4. The 20(P) Superimpose Instruction

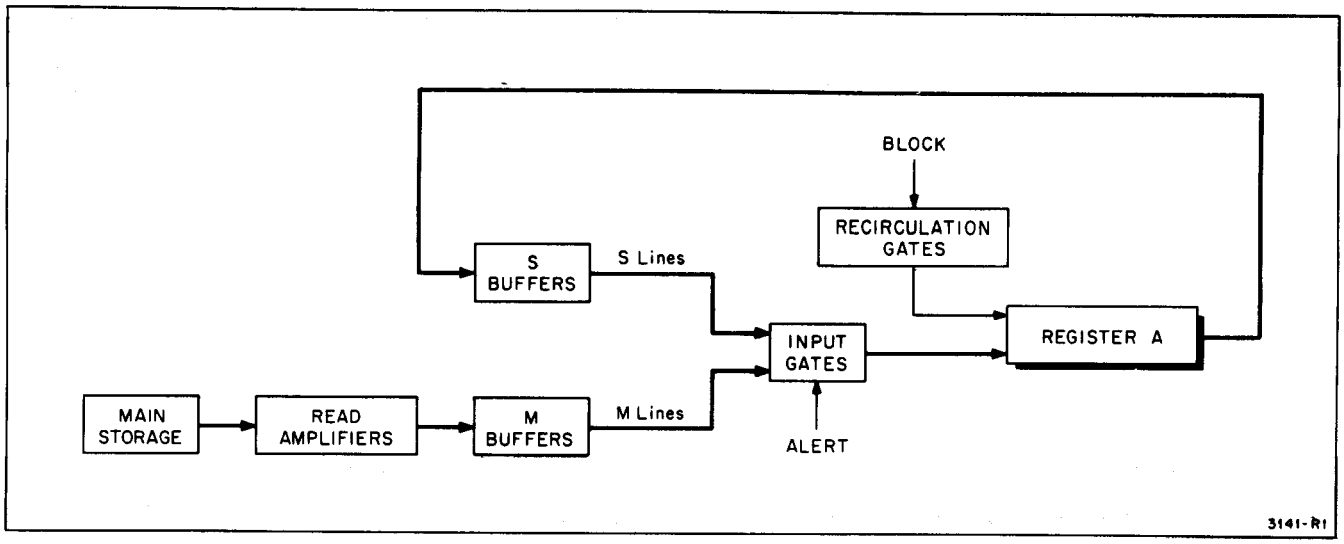


Figure 5-5. The 35(E) Extract Instruction

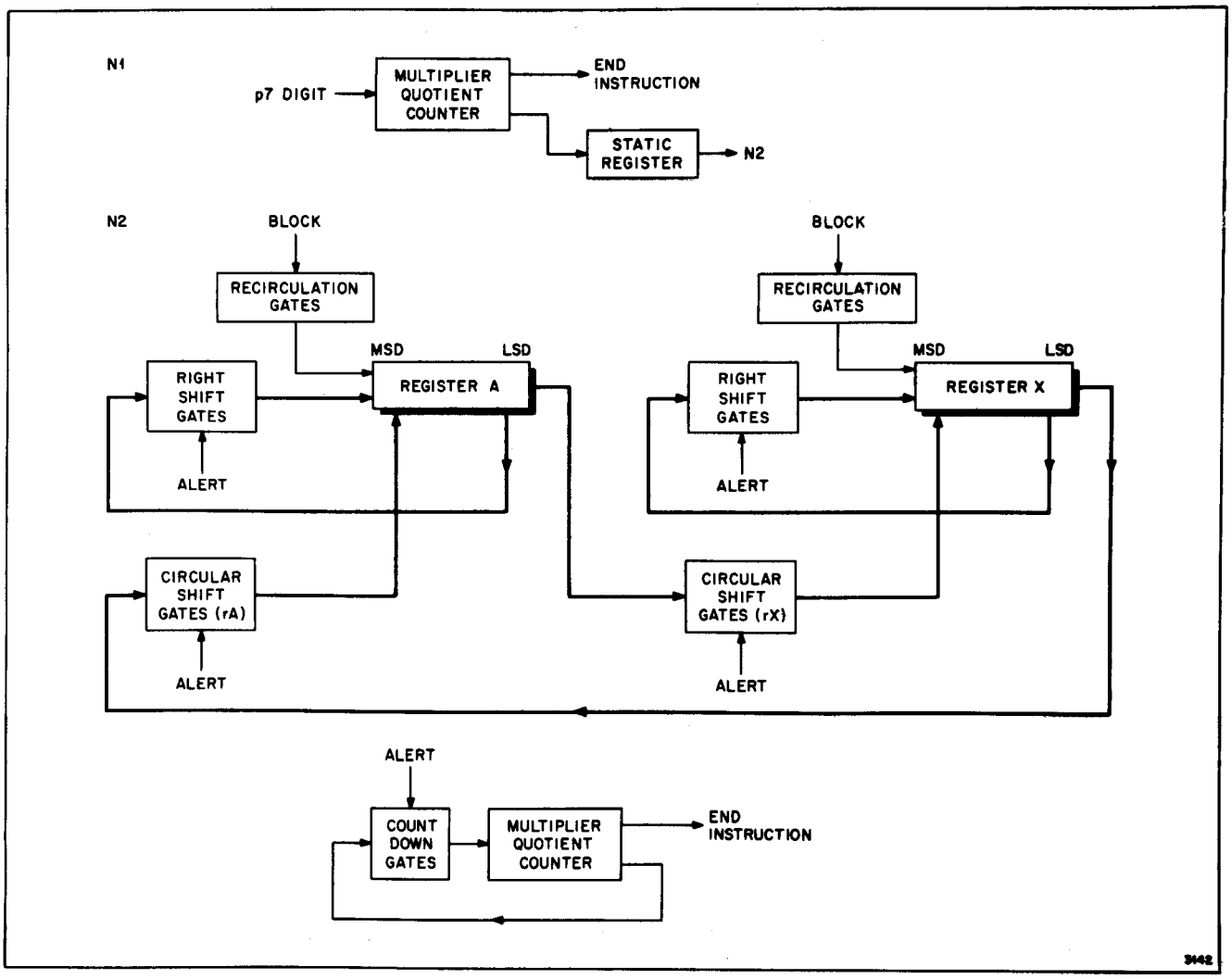


Figure 5-6. The 32(N) Right-Shift Instruction

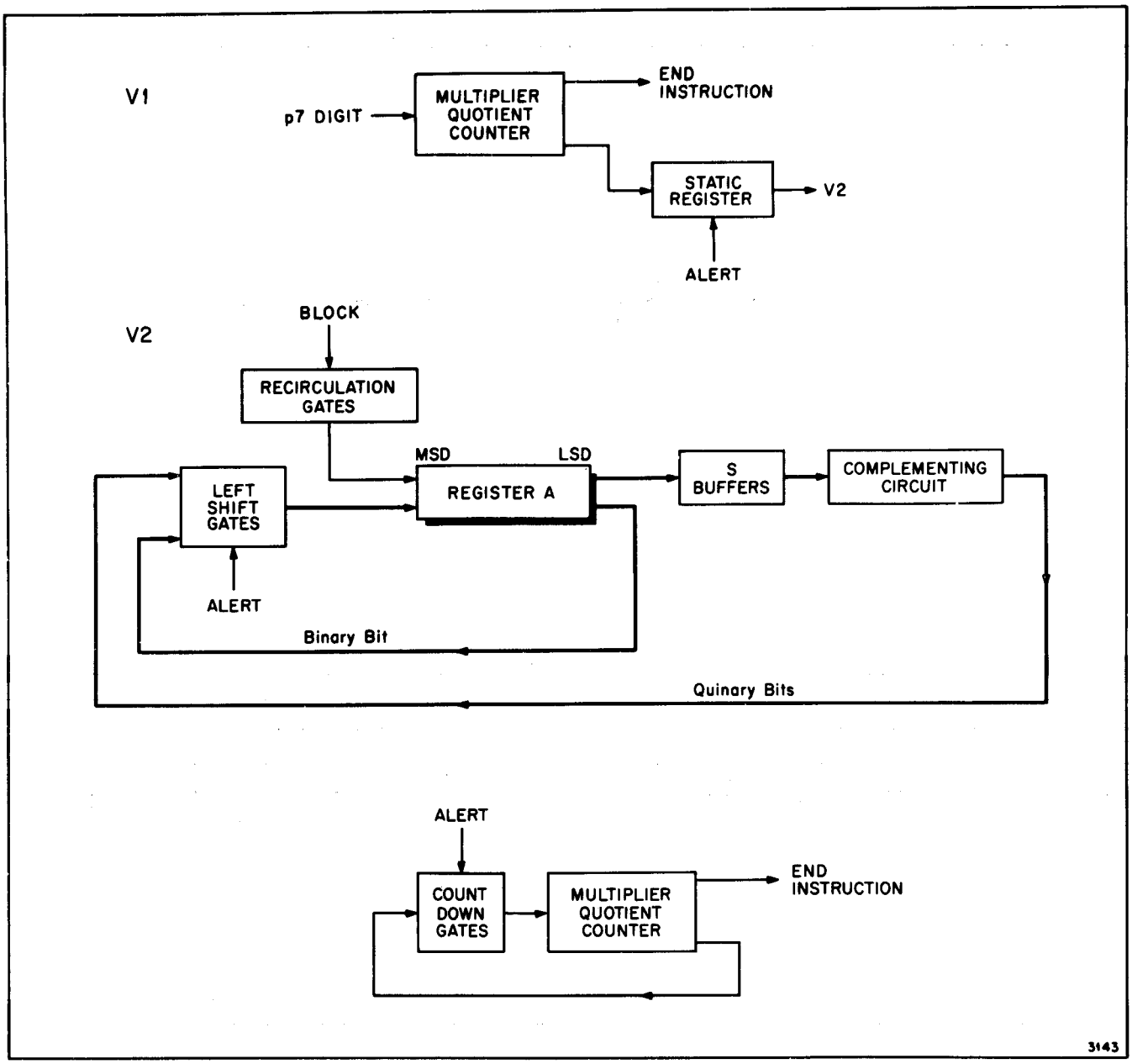


Figure 5-7. The 37(V) Left-Shift Instruction

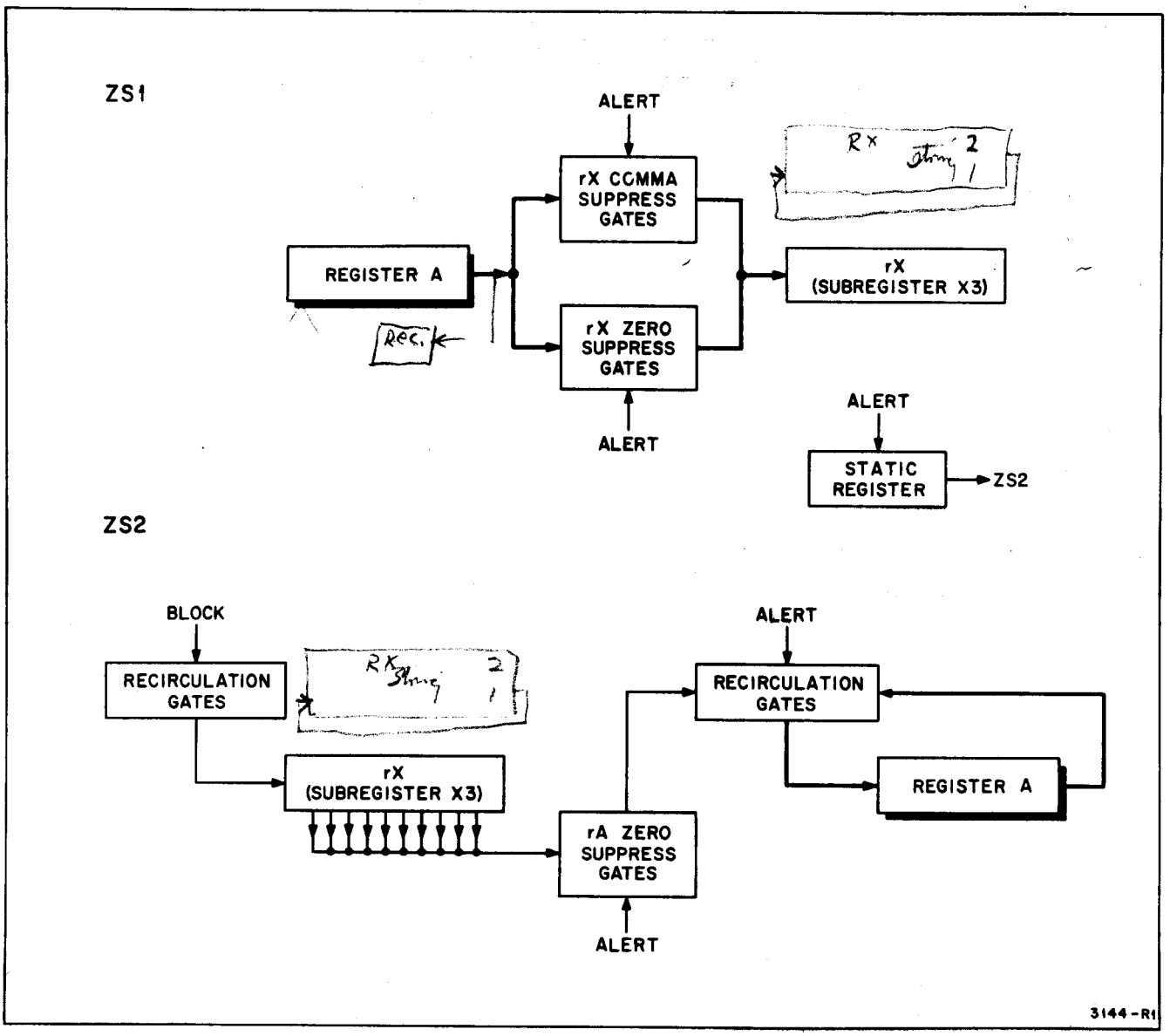


Figure 5-8. The 62(ZS1) Zero-Suppress Instruction

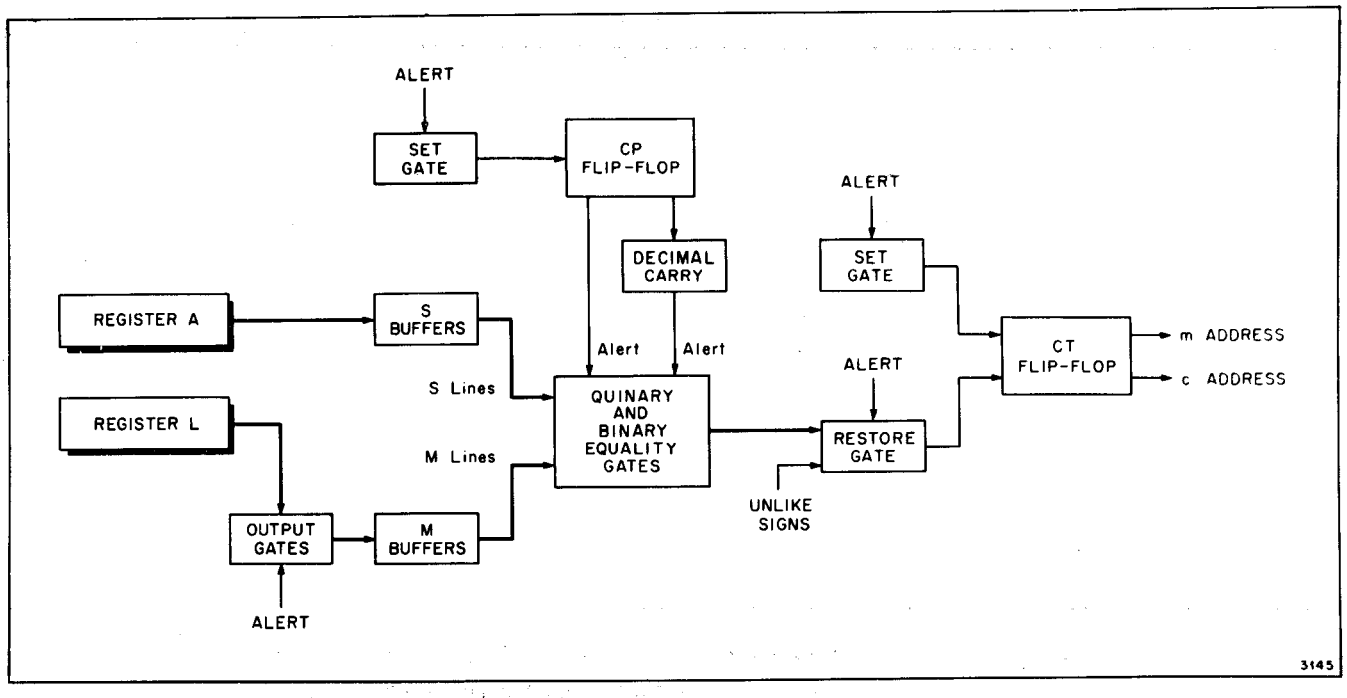


Figure 5-9. The 82(Q) Equality-Comparison Instruction

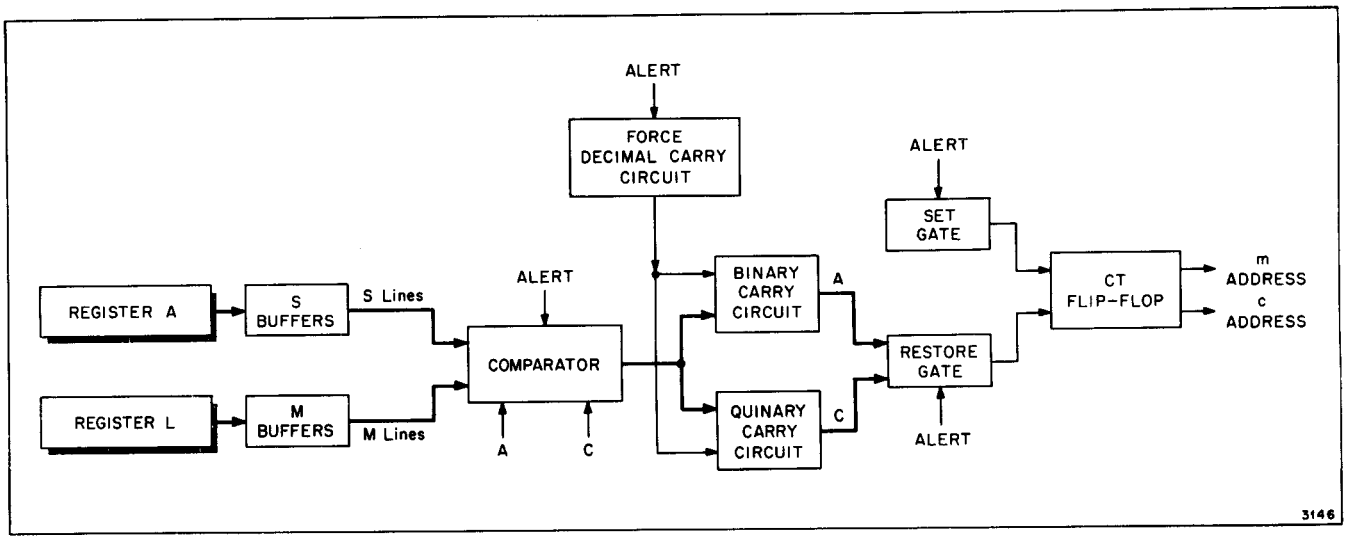


Figure 5-10. The 87(T) Comparison Instructions

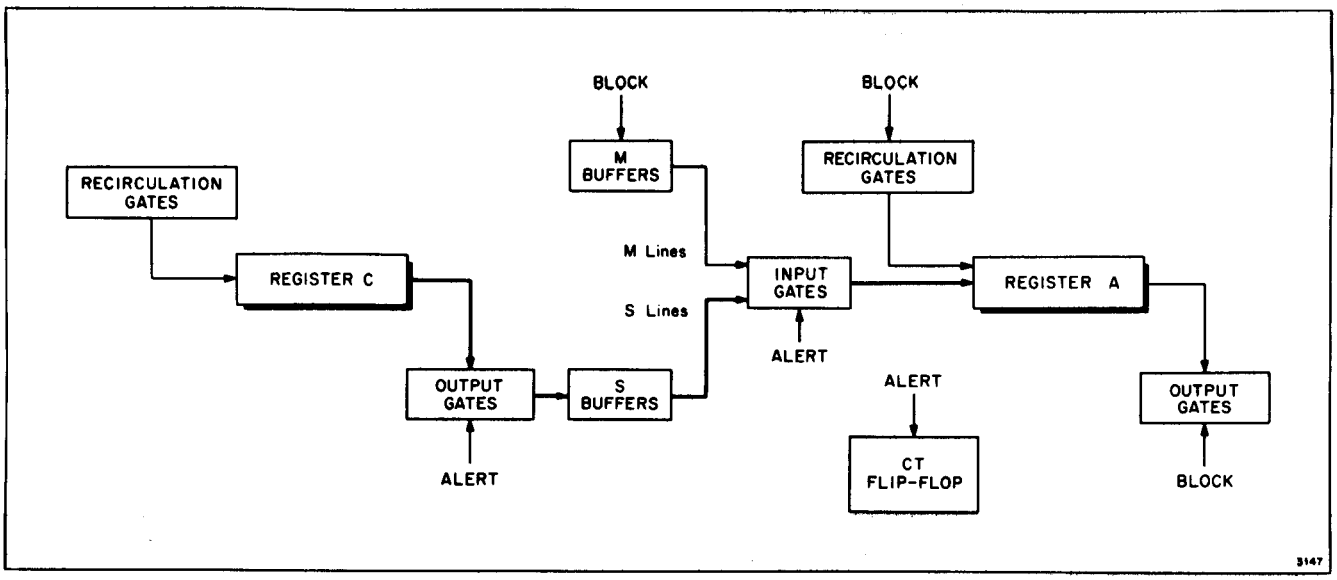


Figure 5-11. Second Stage of 22(I 11), 27(I 21), and 42(I 31) Test Instructions

SECTION VI

ELECTRONIC CIRCUITRY

6-1. INTRODUCTION

The general circuit design of the system stresses the use of the solid-state devices (semiconductor diodes, transistors, and magnetic amplifiers), and reduces the use of conventional vacuum-tube circuits to a minimum. The circuitry is composed of combinations of simple circuits, most of which are packaged. Each of these circuit types has a specific logical application.

This section describes in detail the theory of operation of several basic circuit components. The information presented can easily be projected into the analysis of circuits using these components. Semiconductor theory is presented first so that there is no difficulty in understanding the application of semiconductor components in the circuit descriptions which follow. The origin and control of the power pulses and blocking pulses in the clock is described next. Following the discussion of these pulses, which control the magnetic amplifiers, is a description of the theory and operation of magnetic amplifiers. The storage circuits, which utilize all of the components previously described, are then presented. Finally, the power supplies and power control circuits are described.

Current direction is taken as the direction of electron flow (from negative to positive) in the description of diodes and transistors. In the interest of consistency, the convention of electron flow is preserved throughout the circuitry section.

The schematic wiring diagrams in this manual are merely examples. In servicing a piece of equipment, refer to the diagrams which accompany it.

6-2. DIODES

6-3. BASIC THEORY

A semiconductor diode or transistor is generally composed of a crystal of a solid-state substance containing atoms of germanium (Ge) or silicon (Si) arranged in a geometric

pattern. Electrical conduction through the semiconductor substance depends upon the dislodging of electrons from the outer shells or energy levels of the atoms of germanium or silicon. To explain the conduction process it is necessary to discuss in a simplified manner the electron distribution in a crystal of germanium. (Since germanium and silicon have similar characteristics, only germanium structure need be described.)

6-4. GERMANIUM STRUCTURE

When in a solid state, pure germanium forms a crystalline structure or lattice network, a cubical structure illustrated in two dimensions in figure 6-1. For simplicity, only the valence band of each atom is shown and only the valence electrons are considered. The lines joining the nuclei of the germanium atoms represent the force of attraction holding the atoms together. Figure 6-1 shows how the four valence electrons of a germanium atom are shared by four neighboring atoms. Also each of the four neighboring atoms shares one of its valence electrons with the central atom. Each atom, therefore, has a total of eight electrons in its outermost ring. Four of these electrons are its own, and four belong to the surrounding atoms. The eight electrons in the outermost rings form a stable arrangement called a covalent bond among the individual atoms, and there are no free or excess electrons in the crystal.

6-5. CONDUCTION IN SEMICONDUCTORS. For conduction to take place it is necessary to raise electrons from the valence band to the next higher energy level, the conduction band, where they move under the influence of an electric field. The relative conductivity of the material is determined by the number of electrons available to take part in the conduction process and the ease with which they may be raised to the conduction-band level. As figure 6-1 shows, a pure germanium slab has no free electrons; the electrons in the covalent bond are tightly bound together and are not easily removed, or raised to the conduction-band level. Electrons in a covalent bond are in a stable state of low energy, are bound to the valence band, and are not free to take part in conduction. Pure germanium, then, is a very poor conductor of electricity.

If an electron is removed from a covalent bond, under the influence of an external energy source (heat, light, or an electric field), the atom with which that electron was associated has a net positive charge of 1 because of the absence of one negatively charged electron. The net positive charge which remains when an electron is removed from a covalent bond is called a hole.

Figure 6-2 shows the principles of hole creation and hole flow. In figure 6-2a the valence band is full of electrons, and no holes are present. In figure 6-2b an energy source moves electron 3 at room temperature to the conduction band, and a hole forms in its place in the valence band. In figure 6-2c an applied voltage causes the electrons in the conduction band to move to the right. When electron 2 moves one position to the right, the hole moves one position to the left. In figure 6-2d, as electron 1 moves one position to the right, the hole again moves one position to the left. Hole flow can be considered the inverse of electron flow at the valence-band level. The holes behave as though they had mass, a positive charge, velocity, and real energy. Electric and magnetic fields affect holes in the same way as they affect a particle with the mass of an electron and a positive charge of 1 under similar conditions.

6-6. DOPED GERMANIUM

The purpose of a germanium diode, as of a vacuum-tube diode, is to produce rectification. It should present a high impedance to current in one direction and a low impedance to current in the opposite direction. Since pure germanium (figure 6-1) offers a high impedance to current flowing in either direction, it does not serve to produce rectification. The conductivity of the germanium slab could be increased by applying external energy in the form of heat or light to develop electron-hole pairs like those in figure 6-2b. A much more efficient method of increasing the conductivity is to add minute quantities of selected impurities to the pure germanium. This process is called doping, and germanium processed in this manner is called doped germanium.

6-7. N-TYPE GERMANIUM. Figure 6-3 illustrates the results of adding an impurity such as arsenic (As), which has five valence electrons, to pure germanium. Four of the valence electrons of each arsenic atom enter into covalent bonds with four adjacent germanium atoms. Since there is no electron with which the fifth electron of the arsenic atom can form a covalent bond, only the attraction of the positive arsenic nucleus holds the fifth electron in place. Thermal agitation at room temperature is sufficient to break the bond between the excess electron and the arsenic nucleus. The electron is then free to move in the slab. Adding the impurity has provided a source of excess electrons in the germanium slab. Impurities which give up electrons to the slab are called donors, and germanium which has been doped with donors is

called N-type germanium. The N indicates that current through the slab is by negatively charged particles (electrons).

6-8. P-TYPE GERMANIUM. Figure 6-4 illustrates the results when a trivalent impurity such as gallium (Ga) is added to pure germanium. Again the impurity atoms enter the lattice network substitutionally. Each gallium atom contributes only three electrons to the covalent bond. For each gallium atom added there is a deficiency of one electron rather than an excess as in N-type germanium. Thermal agitation at room temperature forces an electron from a nearby germanium bond into the vacant position, creating a hole in the neighboring bond. Another nearby bond supplies an electron to fill this hole, creating a new hole, and so on. If a voltage is applied across a slab doped with a trivalent substance, there is a coordinated flow of holes toward the more negative potential. This type of conduction at the valence-band level is said to take place by holes. Impurities which accept electrons from the germanium slab to complete their covalent bond are called acceptors, and germanium which has been doped with acceptors is called P-type germanium. The P indicates that conduction through the slab is by holes or positive charges at the valence-band level.

In the P-type germanium each acceptor atom gains an electron and becomes a negatively charged ion. In the whole slab, however, the number of positive and negative charges remains equal, and the slab has a net charge of zero. Similarly, in the N-type germanium each donor atom gives up an electron to the slab and becomes a positively charged ion. Again, there is an equal number of positive and negative charges, and the slab has a net charge of zero.

6-9. JUNCTION DIODES

If a single crystal of germanium is doped in such a manner that there is an abrupt change from N-type to P-type, the unit formed is known as a junction diode. Figure 6-5 indicates the charges normally present in the components which form a junction diode, and figure 6-6 the normal condition at a PN junction.

At room temperature, by thermal diffusion, some of the electrons wander from the N-type to the P-type germanium, and some of the holes wander from the P-type to the N-type germanium. This charge motion results in a slight contact potential (tenths of a volt) between the N and P regions. The P region has an excess of electrons, and therefore a net negative charge. The N region has an excess of holes and a net positive charge. The potential across a junction is called

the barrier potential, shown in figure 6-6 as a battery connected between the N and P regions.

Barrier potential increases until it is balanced by the pressure of diffusion. At this point equilibrium is reached and further migration of electrons from the N to P region is repelled by the net negative charge on the P-type germanium. Similarly the migration of holes from the P to N region is repelled by the net positive charge on the N-type germanium. As a mechanical analogy, these restraining forces are described as potential hills (figure 6-7). In the no-bias curve in figure 6-7a, electrons in the N region are repelled from crossing the junction by the negative potential of the P region. The slope of the curve represents the magnitude of the repelling force. Because thermal energy at normal temperatures does not impart enough energy to the electrons to enable them to climb the hill representing the repelling force, most of the electrons remain in the N region. A similar situation exists for holes in the P region (figure 6-7b).

6-10. FORWARD BIAS. If an external d-c potential is applied across opposite ends of the crystal, the number of electrons and holes crossing the junction can be varied. As shown in figure 6-8a, the external source opposes the barrier potential and makes the potential hill less steep, enabling more electrons and holes to cross the junction. Electrons in the N region are repelled by the negative battery potential (external) and forced toward the junction. Holes in the P region are repelled by the positive battery potential (external) and forced toward the PN junction. Connecting the battery as shown creates what is known as forward bias. Its effect on the barrier potential is as shown on the forward bias characteristics in figure 6-7. If sufficient battery voltage is applied across the crystal, electrons and holes receive enough energy to climb the hill and cross the junction. After the crossing is made the electrons and holes combine. As an electron and hole combine at the junction area another electron is drawn up out of the P region to the positive terminal of the battery. This creates another hole to replace the one lost through combination with an electron at the junction. The external battery potential forces the newly formed hole to flow toward the junction where it can combine with an electron. As the first electron enters the positive battery terminal another electron leaves the negative terminal and enters the N region to replace the electron which combined with the hole. These actions occur simultaneously, and the result is a continuous circuit in which conduction is by electrons in the N region and by holes in the P region. The diode described here is biased in its low-impedance state (forward-biased).

6-11. REVERSE BIAS. If the external battery is connected as shown in figure 6-8b, the external source aids the barrier potential and increases the slope of the potential hill, as shown by the reverse bias characteristics in figure 6-7. Connecting the battery as shown creates what is known as reverse bias and decreases the number of electrons and holes crossing the PN junction. Holes in the P region are attracted away from the junction toward the negative battery terminal. Electrons in the N region are also drawn away from the junction toward the positive battery terminal. The area of transition around the PN junction is now devoid of carriers and effectively opens the circuit. The current in the external circuit is very small (microamperes), and the diode is said to be biased in the high-impedance direction (reverse-biased).

As a result of thermal agitation at room temperature, a few holes are formed in N-type germanium, and a few electrons are released in P-type germanium. These carriers exist in very small numbers and are called minority carriers as distinguished from the principal carriers (electrons in N-type and holes in P-type). The barrier potential aids minority carriers in crossing the junction. When the diode is reverse-biased it is these minority carriers which make up the small external current.

In the test circuit of figure 6-9a the diode is forward-biased when the switch is in position 1, and reverse-biased when the switch is in position 2. Figure 6-9b indicates the type of volt-ampere curve produced by such a test circuit. With the switch in position 1, the diode current (milliamperes) increases rapidly as the applied voltage is increased. The limiter prevents the diode current from reaching so high a value as to overheat and destroy the junction. When the switch is in position 2, only the small diode current (microamperes) due to minority carriers flows through the circuit. Increasing the inverse voltage causes only a slight increase in the reverse current until the Zener voltage is reached. At the Zener voltage the crystalline structure of the germanium slab breaks down, and due to the breaking down of the valence bonds, a large number of electrons and holes is released. Normal operation of a diode is restricted to voltages less than the Zener breakdown voltage of that diode.

6-12. JUNCTION DIODE AS RECTIFIER

Figure 6-10 shows the circuit and waveforms of a junction diode used as a rectifier. For the purpose of this explanation, an ideal diode is assumed which offers a zero

impedance to current in one direction and an infinitely high impedance to current in the opposite direction. Such ideal characteristics are not achieved commercially and are used here for illustration only.

When point A is positive with respect to point B the diode is forward-biased and offers a low impedance to current flow. The current in the circuit, indicated by the dotted arrow, is limited only by the value of load resistor R. Since the diode impedance is zero, the voltage drop across the diode is zero, and the full supply voltage is developed across resistor R as shown on the waveforms.

During the next alternation, when point A is negative with respect to point B, the diode is biased in the high-impedance direction and no current flows through the circuit. No voltage is developed across resistor R, and the full supply voltage is developed across the diode. By permitting a unidirectional or pulsating direct current to flow through the circuit the diode acts as a half-wave rectifier.

6-13. APPLICATIONS

The number of junction diodes utilized in the system approaches 20,000. Most of them are used in logical gates (AND circuits) and buffers (OR circuits).

In the system, all information is expressed in combinations of 0 bits and 1 bits, represented electrically as low or high signals. Figure 6-11 shows typical computer information, in which all pulses are at the zero reference level or at some positive potential. A pulse at a positive potential is called a high, and is represented logically as the positive alternation of a sine wave. Signals at the zero level are called lows; electrically, a low is merely the absence of a high. A correct graphical representation of a low would be a straight line, representing the zero or reference level, one pulse time in duration. For emphasis and to avoid confusion lows are sometimes indicated on logical diagrams as the negative-going alternation of a sine wave or a square wave. Electrically, however, the signal never goes below the reference level. To summarize, a low is merely the absence of a high; it is not a negative-going pulse.

In the diode configuration of figures 6-12c and 6-12d, a positive-going pulse (high) applied at A puts the diode in its low-impedance state. Electrons flow up from ground, through resistor R and the diode, to the source of the positive potential. Since the diode impedance is low, almost all of the supply voltage develops across resistor R. Point D

goes positive, and the output at D is a high. Similarly if a high is applied at B or C a high develops at D. If no voltage is applied at A, B, or C (all inputs low), then none of the diodes conducts, and no voltage develops across resistor R. Point D remains at ground potential and the output at D is a low.

Figure 6-12e shows the output at D for several combinations of inputs at A, B, and C. If lows are present at A and B and C, the output at D is a low. The diode configuration here is serving the logical function of a gate (AND circuit). If a high is present at A or B or C, a high is present at D. Now the same physical diode configuration is serving the logical function of a buffer (OR circuit).

In identifying gates or buffers it is necessary to specify whether high signals or low signals are being used. There is no physical difference between a gate and a buffer. The terms gate and buffer simply designate the purpose the unit is to serve in the circuit.

Figures 6-12c or 6-12d show that a signal, high or low, on any input circuit (A, B, or C) does not affect any other input circuit. The high back resistance of a diode minimizes crosstalk among several input circuits.

6-14. TRANSISTORS

6-15. BASIC THEORY

In this section the operation of both the NPN and PNP type junction transistors will be described. As far as possible, actual circuits will be used as examples. The system utilizes approximately 600 transistors in a variety of circuits too numerous to permit a separate discussion of each one in this manual. The principles outlined, however, are general enough to enable the reader to understand the operation of the many transistor circuits in the system.

The operation of a germanium slab which changes abruptly from N to P type has been described previously. A transistor is a slab of germanium which contains two such abrupt changes, from N to P to N (NPN type), or from P to N to P (PNP type). The essential feature of the junction transistor is that a thin layer (usually about 0.001 inch) of one conductivity type separates two larger regions of the opposite type.

6-16. COMMON-BASE CIRCUIT

Figure 6-13 shows isometrically both NPN and PNP type junction transistors. The barrier potentials across the emitter and collector junctions are shown as batteries. The emitter is so named because it injects carriers into the base region (somewhat analogous to the cathode of a vacuum tube). The collector is so named because it attracts carriers through the base region (analogous to the anode or plate of a vacuum tube). The base functions somewhat like the control grid in a standard triode tube.

In the normal operation of a transistor as a class A voltage or power amplifier the emitter-base region is forward-biased (biased in the low-impedance direction) and the collector-base region is reverse-biased (biased in the high-impedance direction). Figure 6-14 shows the d-c biasing potentials normally applied to NPN and PNP transistors.

6-17. NPN TRANSISTOR. In the NPN transistor shown in figure 6-14a, if switch S1 is closed and switch S2 is open, electrons flow from the battery $-E_E$ into the emitter and combine with holes at the junction. An electron in the valence band of the base region is raised to the conduction-band level (developing another hole), and flows through the external circuitry to $+E_E$. Due to the application of forward bias between the emitter and base, the potential hill at the emitter junction is low, and E_E must be kept at a low value or the emitter current (I_e) will become excessive. The operation of this circuit is exactly the same as that of the forward-biased diode previously discussed.

When switch S2 is closed and switch S1 is open, the operation of the collector-base circuit is exactly the same as the operation of the reverse-biased diode discussed previously. Due to the reverse bias applied between the collector and base, the potential hill at the collector junction is very steep. Only the minority carriers in the base and collector regions complete the high-impedance path from the battery $-E_C$ through the base, collector, resistor RO, and $+E_C$. Very little current flows through RO in the output circuit, so E_C is normally kept at a substantially higher voltage than E_E.

When switch S1 and switch S2 are both closed, electrons enter the emitter region and flow to the base. Electrons in the base region are not repelled by the barrier potential at the collector junction. These electrons in the base region may either combine with a hole and flow back to $+E_E$, or cross

the collector junction because of the attractive force of $+E_C$ and flow through the collector region and to $+E_C$. It is desirable that the electrons enter the slab at the emitter, flow through the base to the collector, and then flow through both batteries (connected series aiding). To discourage electron and hole combinations in the base region the base is made very thin. This reduces the transit time of electrons in the base region and therefore the time in which a combination can occur. The base region is also more lightly doped than the emitter and collector regions to reduce the number of holes available for combination. Through both of these means the electron-hole combinations are kept to a minimum, and more than 95 per cent of the electrons normally injected at the emitter arrive at the collector. The remaining electrons combine with holes in the base region and make up the small base current I_B.

So far only the d-c circuits associated with the NPN junction transistor have been investigated. To make the transistor act as a class A amplifier, it is only necessary to apply an a-c input signal between the emitter and base. (This assumes that E_E has been correctly chosen to bias the transistor at the correct operating point.)

Figure 6-15a shows a circuit in which an a-c signal may be applied across the input resistor RI, and this voltage, in series with E_E, is applied between emitter and base. In figure 6-15b, assume that at time 1 (t1) the a-c input voltage is such that the top of resistor RI goes positive with respect to the bottom of resistor RI. Now the voltages e_{RI} and E_E are connected series opposing, and the forward bias between the emitter and the base is reduced by the amount of e_{RI}. This means that the potential hill at the emitter junction becomes more steep and that the number of electrons flowing in the emitter-base circuit is decreased. Since fewer electrons are injected into the crystal at the emitter, fewer electrons arrive at the collector and flow down through the output resistor RO. With fewer electrons flowing down through RO the top of resistor RO becomes more positive, and a positive-going output signal is developed, as shown.

At time t2 the input signal is such that the top of resistor RI goes negative with respect to the bottom of resistor RI. Under these conditions e_{RI} and EE are connected series aiding, and effectively the forward bias between emitter and base is increased. Increasing the forward bias lowers the potential hill at the emitter junction and permits more electrons to be injected into the crystal at the emitter. When the number of electrons arriving at the base increases, the number of electrons arriving at the collector and flowing down through resistor RO increases. When the number of electrons flowing down through RO increases, the top of resistor RO becomes more negative, and a negative-going output signal is developed, as shown in figure 6-15b.

The output signal developed across resistor RO is an enlarged replica of the input signal developed across RI, with no phase inversion. The current flowing in the output circuit is a function of the current flowing in the input circuit. More specifically, the number of electrons injected into the emitter is a function of the emitter-base voltage; however, over 95 per cent of the total emitter current change is received at the collector. To develop a change in the output current (Ic), it is necessary to change the input current (Ie), and this is done by changing the emitter-base voltage.

6-18. TRANSISTOR AS VOLTAGE AMPLIFIER. The next point to be determined is why $e_{rO} > e_{rl}$ or, more specifically, why the transistor acts as a voltage amplifier. The ratio $\frac{\Delta I_c}{\Delta I_e}$ with E_c constant is referred to as the current gain factor, alpha (α). A typical value of alpha for junction transistors is $0.95<\alpha<1$ which means that actually there is a current loss between input and output circuits. The resistance between the emitter and base (with the collector circuit open) is commonly designated r11. Since the emitter-base section is forward-biased, r11 is low; a typical value is about 500 ohms. The resistance between the collector and base (with the emitter circuit open) is commonly designated r22. Since the collector-base section is reverse-biased, r22 is high; a typical value is about 100 kilohms.

In the ideal case of a transistor feeding into an infinitely high impedance, the following is true:

Where VA = voltage amplification,

$$VA = \frac{e_{out}}{e_{in}} = \frac{\Delta I_c \; r22}{\Delta I_e \; r11}$$

but $$\frac{\Delta I_c}{\Delta I_e} = \alpha$$

Substituting $$VA = \alpha\frac{r22}{r11} = 0.95\left(\frac{100 \text{ kilohms}}{500 \text{ ohms}}\right) = 190$$

Also, where PG = power gain,

$$PG = (\text{current gain})^2 \; (\text{resistance gain})$$

$$PG = \alpha^2\left(\frac{r22}{r11}\right) = (0.95)^2\left(\frac{100 \text{ kilohms}}{500 \text{ ohms}}\right) = 180$$

The gain figures indicated here are much higher than those attained in actual practice. The load resistance will always have some finite value, and the gain will decrease accordingly. Even though there is a current loss ($\alpha < 1$), there can be a voltage and/or power gain because of the high resistance gain involved.

6-19. PNP TRANSISTOR. In the PNP transistor (figure 6-14b), if switch S1 is closed and switch S2 is open, the emitter-base region acts as a conventional forward-biased diode. Electrons enter the base and combine with holes at the emitter junction. At the same time, electrons at the valence-band level are raised to the conduction-band level at the emitter. This develops new holes which are attracted toward the base. The important thing to note here is that the emitter acts as though it were injecting holes (principal carriers) into the germanium crystal. When S1 is open and S2 is closed, the collector-base region acts as a conventional reverse-biased diode, with only a minority-carrier current flowing. When S1 and S2 are both closed, holes are injected into the emitter region. When these holes cross the emitter junction and flow into the base region they can either combine with an electron and sustain the base current (I_b) or cross the collector junction, combine with an electron at the collector, and sustain the collector current (I_c). To keep the current gain factor as close to unity as possible, the base is made thin and is lightly doped, so that few electron-hole combinations take place in the base region.

Figure 6-16 shows a PNP transistor in a typical class-A amplifier circuit from the read-amplifier-package schematic (RAPS). The collector-base region is biased by the method described in section 6-16. The bias circuit for the emitter-base region introduces a bypass capacitor (CJ5) which theoretically offers an infinite impedance to the d-c bias current, but is practically a short circuit to alternating current of the applied signal frequency. The 5.6-kilohm resistor and battery circuit present a high impedance to the a-c signals developed across the transformer. The capacitor circuit presents a very low impedance, however. The a-c signals flow through the a-c source, bypass capacitor, and transistor, and back to the source. They bypass the 5.6-kilohm resistor and power supply, maintaining E_E at a steady value (hence the name bypass capacitor). The operating point of the transistor remains fixed.

The a-c input signal is applied across the secondary of transformer MT15, and the output voltage is developed across the primary of transformer MT 16. These windings are used in place of the input resistor RI and the output resistor RO in the previous examples. The transformers also provide an impedance match between stages.

If an a-c input signal causes the top of the input winding to go positive with respect to the bottom, the forward voltage between emitter and base increases. More holes are injected into the crystal at the emitter, and the number of holes arriving at the collector increases proportionally. More electrons leave $-E_C$, flow up through the output-transformer primary, and combine with holes at the collector. These extra electrons are raised to the conduction band at the emitter, and flow through the input winding and capacitor CJ5 to ground, which is $+E_C$. The a-c signal causes the top

of the output-transformer primary to go positive. Transformer action induces a signal into the secondary for application elsewhere.

If an input signal causes the top of the input winding to go negative, the forward voltage between emitter and base is reduced. Fewer holes are injected into the crystal at the emitter, and fewer holes arrive at the collector. The number of electrons flowing up through the primary of the output transformer decreases, and the top of the primary becomes less positive or effectively goes negative. A signal opposite in polarity to the output signal described in the preceding paragraph develops across the secondary of the output transformer.

6-20. COMMON-EMITTER CIRCUIT

All of the transistor amplifier circuits discussed have been common-base configurations. In the magnetic computers, as in most applications, the common-emitter configuration is more frequently used. The common-emitter circuit yields higher voltage and power gains, higher input impedance, and lower output impedance than the common-base circuit.

It is also possible to connect transistors in a common-collector circuit, which functions like a cathode-follower circuit, and has a high input impedance, a low output impedance, and a gain of less than 1. Common-collector stages are not used in the system and will not be discussed.

In the common-emitter circuit in figure 6-17, the polarity of battery E_B is such that the emitter-base region is forward-biased. The operation of the emitter-base circuit is the same as that of a forward-biased diode. Again, the principal carriers (electrons) are injected into the crystal at the emitter. As in the common-base circuit, most of the electrons which enter the base region are attracted to the collector by the positive attractive power of $+E_C$. Less than 5 per cent of the electrons which enter the base combine with holes and flow through resistor R1 and E_B. As in the common-base circuit, the base current I_B is very small compared with the current flowing between the emitter and collector.

If switch S1 is closed, an a-c signal develops across resistor R1. Assume that on the first alternation the top of resistor R1 goes positive with respect to the bottom. The a-c voltage now aids E_B, and the potential hill at the emitter junction becomes less steep. An increased number of electrons enters the emitter, arrives at the collector, and flows down through RO to E_C. The increased collector current causes the top of RO, and hence the output voltage, to become more negative. If the input signal goes positive, then, the output signal goes negative (a 180-degree phase shift).

On the second alternation, the top of resistor R1 goes negative with respect to the bottom. The voltage across

resistor R1 (e_{R1}) now opposes E_B, and the potential hill at the emitter junction becomes more steep. Fewer electrons enter the emitter, arrive at the collector, and flow down through R0 to E_C. Decreasing the current through R0 causes the output voltage to become more positive. Again the signal has undergone a 180-degree phase shift. Of the three possible transistor-amplifier configurations (common-base, common-emitter, common-collector), only the common-emitter circuit shifts the phase of a signal 180 degrees.

For junction transistors connected in the common-emitter configuration, the input impedance is about 800 ohms, and the output impedance is about 50 kilohms. The collector current (I_C) is the output current, and, since the input is applied to the base, I_B is the input current. Let the current gain for a common-emitter stage be designated β. Then

$$\beta = \frac{I_{output}}{I_{input}} = \frac{\Delta I_C}{\Delta I_B} \text{ , with } E_c \text{ constant}$$

Since ΔI_B is very small, β may be quite large, and is always greater than 1. It can be shown that $\beta = \frac{\alpha}{1-\alpha}$.
If $\alpha = 0.95$:

$$\beta = \frac{0.95}{1-0.95} = \frac{0.95}{0.05} = 19$$

Where VA is voltage amplification and PG is power gain, the maximum theoretical amplification for a typical common-emitter stage is:

VA = (current gain) (resistance gain)

= β (resistance gain)

= about 500 average

PG = (current gain)^2 (resistance gain)

= $(\beta)^2$ (resistance gain)

= in excess of 5000 average

These gain figures indicate that the common-emitter circuit is frequently preferable to the common-base configuration.

Despite its favorable gain characteristics the common-emitter circuit has a somewhat poorer frequency response than the common-base circuit. The large transit time of carriers in transistors causes α to decrease as the applied frequency increases. That frequency at which α decreases to 0.707 of its low-frequency value is termed the alpha cutoff frequency (α_{CO}). This frequency represents the 3-db down point on a frequency-response curve. Consider a common-base circuit in

which the frequency increases until α (normally 0.95) decreases 30 per cent below its maximum value. The voltage gain of this stage is about 70 per cent of its maximum value. In a common-emitter circuit at this frequency, current gain is as follows:

$$\beta = \frac{0.7(0.95)}{1-[0.7(0.95)]} = \frac{0.665}{0.335} \approx 2$$

The voltage amplification of this stage, then, is only 10.5 per cent of the maximum 19, and, for a given frequency, the gain of the common-emitter circuit is decreased much more than the gain of a common-base circuit. To summarize, the frequency response of a common-emitter stage falls off much more rapidly than the response of an equivalent common-base stage.

6-21. SYMBOLS

Thus far, the figures in this section have shown PN junctions in detail as an aid to understanding transistor operation. The standard transistor symbols in figure 6-18 are usually used on schematic wiring diagrams, however. The direction of the arrowhead on the emitter indicates whether a transistor is PNP or NPN type. In many circuits these symbols are shown rotated about their present positions; the symbol, however, remains the same.

6-22. SUMMARY

To summarize the principles presented in this section, an early version of the print-drum read-amplifier circuit is presented in figure 6-19. The permanently recorded code generator in the printer develops the indicated waveform on the primary of TR5. By transformer action this signal is induced into the secondary and applied to the input of Q1. The operation of this class A stage is identical to the operation of the circuit in figure 6-16. The signal developed across the primary of SSO-6 will have greater amplitude than the input to Q1, but the same phase. This signal is transformer coupled to Q2 by SSO-6 which also serves as an impedance-matching device between the stages. Q2 is RC coupled to Q3 in a manner similar to RC coupling as used between vacuum-tube stages. The 1.2-kilohm resistor serves as the coupling resistor between the stages. The voltage developed across this resistor is then applied to the series combination of C1-R1. That portion of the Q2 output voltage which appears across R1 is applied as the input to Q3.

The input circuit of Q3, an NPN transistor, is reverse-biased. That is because the stage is operated class C and is normally held cut off. Q3 conducts only if an input signal is applied such that the top of R1 goes sufficiently positive to overcome the inverse bias on the base and cause the potential hill at the emitter junction to be lowered. When Q3 is driven into a state of conduction, electrons flow down through R2 making the top of R2, and hence the output, less positive.

The input signals applied to Q3 are chosen so that Q3 bottoms; this causes the output signal to be squared off as shown on the diagram.

The diode in the Q3 output circuit is a clamping diode which maintains the steady-state output of Q3 at +16 volts. With no signal output from Q3 electrons flow from the +16-volt supply through CR9, R2, to the +45 volt supply. This clamps the output terminal at +16 volts (less a forward voltage drop across the diode small enough to be neglected). Output signals are then developed below the +16-volt level.

6-23. VOLTAGE BREAKDOWN IN JUNCTION TRANSISTORS

Application of a high inverse voltage across a junction causes two types of breakdown known as avalanche breakdown and punch-through breakdown.

Avalanche breakdown is the result of current multiplication by ionization. The diode volt-ampere curve in figure 6-9b shows that the inverse current remains substantially constant over a given range of applied reverse voltages. (Junction temperature is assumed constant.) As the applied inverse voltage increases, however, the minority carriers are accelerated until they contain sufficient energy to remove electrons from the valence band by collision. This process, called ionization, is similar to the ionization in gas tubes.

Each collision develops an electron-hole pair, making additional carriers available to take part in conduction. At a critical voltage each such pair produces one additional pair, on the average, sustaining the process. Current flowing across the junction is then limited only by the external series impedance. The voltage at which the junction breaks down and an ionization current exists is known as the avalanche breakdown voltage. Normal transistor action ceases at this voltage.

Punch-through breakdown takes place when the application of an inverse voltage across a junction causes the space-charge layer to widen. Inverse bias causes the region around the junction to become devoid of principal carriers (section 6-11). The width of this area of transition, or space-charge layer, is a function of the applied voltage; the layer widens as the inverse voltage increases. If one side of a junction has a higher resistivity than the other, the space-charge widening will take place predominantly on the high-resistance side. To discourage electron-hole combinations, the base region is doped more lightly than either the emitter or collector regions. Since it has few carriers, the base region has a higher resistivity than the collector region. When an inverse voltage is increased across the collector junction, the space-charge layer widens, and spreads toward the emitter junction. The inverse voltage applied across the collector junction which causes the space-charge layer to reach the other junction is called the punch-through voltage. At this voltage the transistor behaves as if the collector and emitter were connected

internally by a battery having a voltage equal to the punch-through voltage, and transistor action ceases.

If an inverse voltage (E_C) exceeding the punch-through voltage (E_P) is applied to the collector, the difference between these two voltage ($E_C - E_P$) appears at the emitter. The appearance of this voltage at the emitter may be used to detect punch-through. Transistors must be used in circuits so designed that the breakdown voltages are not reached.

6-24. TRANSISTOR IDENTIFICATION

Because of widespread variations among transistors, it is sometimes difficult to identify the polarity type and the terminal connections of an unknown transistor. Outlined here is a practical method by which maintenance personnel, equipped only with an ohmmeter, can identify a transistor and its terminals.

The ohmmeter serves as both a power supply and a current-indicating device. The current through the transistor increases as the resistance reading decreases.

CAUTION

When testing low-power transistors by this method use a high-sensitivity meter. Some low-sensitivity meter movements draw more current than can safely be passed through certain low-power transistors.

Proceed as follows:

(1) With the ohmmeter find the pair of transistor terminals which gives a high resistance reading when checked with both polarities of the meter. These are the collector and emitter terminals.

(2) Connect the meter with the correct polarity to give the lower of these two high resistance readings and select a meter range which gives approximately a center scale reading. This lower reading is obtained because the collector junction usually has a higher leakage current than the emitter junction. Assuming that the red meter lead is positive, the meter leads now indicate the normal class A biasing polarities for the transistor.

(3) Jumper the unconnected transistor lead (base terminal) to the terminal connected to the red (+) meter lead. If the resistance reading increases, the transistor is a PNP type and the red meter lead is connected to the emitter terminal. If the resistance reading decreases, the transistor is an NPN type and the red meter lead is connected to the collector terminal.

(4) To verify the results of step 3, jumper the base terminal to the terminal connected to the black (-) meter lead. If the resistance reading decreases, the transistor is a PNP type and the black meter lead is connected to the collector terminal. If the resistance reading increases, the transistor is an NPN type and the black lead is connected to the emitter terminal.

6-25. CLOCK

6-26. GENERAL DESCRIPTION

The clock, in the broadest sense, is nothing more than one of the system power supplies; it supplies power to operate all of the magnetic amplifiers in the system.

The clock is a linear, high-power, narrow-band amplifier which accepts the low-level sprocket signal from the storage drum and amplifies it to a level sufficient to drive the magnetic amplifiers. The clock output also drives external circuitry which develops probe and clear pulses. In addition to developing power pulses and blocking pulses for the computing circuitry, the clock acts as a central timing device for the system.

The clock circuitry, shown as a block diagram in figure 6-20 and a schematic in figure 6-27, includes a phase-control system which maintains a fixed phase relationship between the sprocket signals and the clock output. Through both a fast and a slow automatic gain control (AGC) system, the clock monitors its own output and maintains the amplitude of the output voltage within very close limits under all normal variations in loading and line voltage.

Since the clock must drive a load of very low impedance, it must include an impedance-matching device for maximum efficiency. This requirement is met by the use, in the output stage, of a 60:1 step-down transformer that contains a two-turn secondary and a 120-turn primary. The clock output is distributed by heavy, low-inductance bus bars.

Physically, the clock consists of two separate units, a driver chassis and an output chassis. The driver chassis contains all of the low-level circuitry, and the output chassis contains the six 4X250B power output tubes, with the associated tank circuitry. Each chassis is well shielded and grounded so that spurious pickup in any low-level stage is reduced to a minimum.

The general characteristics of the clock are as follows:

(1) Frequency. Both the input and the output sine-wave signals center around 707 kc.

(2) Voltage gain. The clock input is an 0.5-volt peak-to-peak sine wave. The clock output is a 36-volt peak-to-peak sine wave.

(3) Voltage regulation. The maximum contemplated change in load is between 60 and 70 watts. A 70-watt load change varies the output voltage no more than 10 per cent.

(4) Power gain. The clock is designed to step up the low-power sprocket signals to 1 kw.

(This system uses only one clock. In computer systems which utilize more than one clock, it is imperative that all clock output signals be identical in phase and in amplitude. Each clock-driver chassis contains a signal take-off point, the synchronizer-clock driver stage, which can be used to supply the driving signals to another clock. Through adjustment of this stage, the input to the second clock is made equal in amplitude and in phase to the input to the first clock. When the two clocks receive identical driving signals, they produce identical output signals.)

6-27. PRINCIPLES OF OPERATION

The operation of the two AGC systems and the phase control unit, all integral parts of the clock circuitry, will be discussed separately. The first objective will be to trace a sprocket signal through the clock circuitry to the output transformer.

In the block diagram (figure 6-20), the type of signal (sine wave, spike, etc.) and the phase relationships at a given time are shown at each stage. No attempt is made, however, to indicate the amplitude or power level of any signal in this illustration.

Two sprocket tracks are recorded on the drum and two heads are constantly reading each track. Two heads from adjacent tracks are connected in a series string and the two series strings are connected in parallel. Since the recorded information consists only of a 707 kc signal, the heads theoretically receive identical signals at all times, with no phase difference among the four induced signals. Irregularities in the recording medium and variations in the drum-to-head spacing modulate the signals received by the heads during a drum revolution. The effect of these modulations is lessened by the

series-parallel connection of the four heads and by the use of the total induced voltage across the series strings as input to the clock circuitry. Even a missing pulse in one pulse position on the track would reduce the clock input signal only a small amount below the normal level.

The 0.5-volt peak-to-peak sprocket output is applied to the primary of a 1:3 step-up transformer. The transformer secondary supplies the driving signal to the synchronizer clock-driver stage. The voltage amplifier half of this stage supplies a minimum signal of about 7 volts peak-to-peak to the RC network in its plate circuit. Capacitor C10 provides a variable phase shift of the signal applied to the cathode follower. Increasing the capacitance of C10 increases the phase angle between the amplifier output and the cathode-follower input. The cathode-follower output is developed at coaxial connector No. 1.

(If a synchronizer clock is used in conjunction with the processor clock, as in the two-clock systems previously mentioned, connector No. 1 is connected to the primary of the synchronizer-clock input transformer. Adjusting C10 makes the phase of the two clock inputs equal and adjusting R7 makes the amplitude of the two clock inputs equal. Since the clocks receive identical input signals, they produce identical output signals.)

The secondary of the input transformer also supplies the a-c signal to the first voltage amplifier, which develops an output signal having a minimum amplitude of 25 volts peak-to-peak. This signal is RC-coupled to the core driver, where the amplitude is increased further. The a-c plate circuit of the core driver contains a tank circuit with a low Q (7 to 10), which utilizes the input winding of the peaking core as part of its inductance. Because the peaking core is designed for fast saturation in either direction, the core flips very rapidly near the zero crossing of each sprocket alternation. If the signal shown in figure 6-22 is applied to the input of this core, the core flips or saturates in one direction when the signal crosses the axis at location A. When the signal again crosses the axis at location B the core flips in the opposite direction. Flipping is relatively independent of the amplitude of the core-driver output. The only requirement for flipping is that the applied signal cross both sides of the reference level.

To control the input of the 6AG7 tube, a 50-kilohm potentiometer (R3) is used for the grid resistor. If a greater than normal signal is applied to the 6AG7, the input to the 6AQ5 contains too many overshoots or damped oscillations. If a smaller than normal signal is applied to the 6AG7, unreliable

triggering results. Resistor R3 is adjusted so that the 6AG7 provides one clean spike at the input of the 6AQ5 for each sprocket alternation and to provide reliable triggering on every sprocket signal.

A voltage is induced in the peaking-core secondary only when there is a flux change about the primary, which occurs mainly during the switching operation. The signal induced in the secondary is an alternately positive and negative spike with a peak of 20 volts and a pulse width of 0.1 microsecond. This signal is applied to the input of the 6AQ5 (class B) smoothing-tank driver, producing a net input signal of 7 volts above ground. Because of the fast-flipping core the magnitude and phase of the input to this stage are not solely dependent upon the amplitude of the core-driver output. The function of the 1-kilohm resistor across the secondary of the peaking core is to damp out any oscillations or overshoots in the core and provide a clean input to the smoothing-tank amplifier.

In the smoothing-tank driver, the 7-volt peak input spikes are amplified and used to drive the smoothing-tank circuit. The smoothing tank, in the a-c plate circuit of the amplifier, has a Q of 10. The oscillating current in the tank circuit transforms the spiked output of the amplifier into a sine wave with a peak of 125 volts. The smoothing tank provides an additional safety factor in that, even if an occasional sprocket pulse is missing, the sustained oscillations in the tank still provide almost full input to the 6AG7. The reshaped sprocket signal is free of the original sprocket amplitude variations (runout).

The signal developed across the smoothing tank is coupled to the 6AG7 through an attenuator circuit. The drive control (R5) is adjusted so that only the desired percentage of the total smoothing-tank voltage is impressed across the input of the 6AG7. The 6AG7 and succeeding stages are then operated in the most nearly linear portion of their characteristic curves. If the smoothing-tank voltage varies from the 125-volt peak level, only a fraction of the variation appears at the input of the 6AG7. For all practical purposes the 6AG7 input can be considered to have a constant amplitude. The amplified sine wave from the 6AG7 is amplified further in one half of the 12AT7, the output of which is RC-coupled to the 6AQ5 phase-splitter driver. The output of the 6AQ5 is applied to a 1:1 transformer with a single-ended primary and a balanced secondary. The secondary provides two sine-wave outputs equal in amplitude but opposite in phase. Each of these signals is then applied to one of the 6146 push-pull drivers. Both of the push-pull drivers are biased class A, so each provides a sine-wave output. The outputs of the drivers are equal in amplitude but opposite in phase.

The push-pull stage consists of two banks of three 4X250B power tubes connected in parallel. Because class B operation results in increased plate efficiency, this stage is biased just beyond cutoff at -70 volts. The grids are driven to cathode potential, but the tubes draw little or no grid current. Because of the class B operation the input sine wave is rectified so that each bank of tubes produces only one alternation of a sine wave. In this application the push-pull tubes drive a smoothing-tank circuit in which the oscillating tank current develops a sine-wave voltage output. The voltage developed in the tank circuit is impressed across the primary of the output transformer. Two complete sine waves are developed across opposite ends of the centertapped secondary to provide both an A-phase and a B-phase output. The clock output consists of two 36-volt peak-to-peak sine waves of opposite phase.

To lessen the insulation requirements and the personnel hazard created by the plate caps of the six 4X250B power tubes, the centertap of the output-transformer primary is grounded, and the cathodes of the tubes are at a negative potential of 1600 volts. The unit is shielded to eliminate radiation and to prevent personnel from coming into contact with the high voltage.

Associated with the output stage, but physically separate, are four blocking-pulse transformers, a current and voltage monitoring panel, a set of high-voltage power supplies, and a plate overcurrent relay. The overcurrent relay is adjusted so that it turns off dc when the total plate current of the six 4X250B tubes reaches 1.48 amperes. This circuit is more fully described in section 6-100.

6-28. FAST AGC SYSTEM

6-29. GENERAL DESCRIPTION. The fast AGC system uses a difference amplifier designed to maintain each cycle of the clock output at the same amplitude. If a change in the load causes the amplitude of one cycle of the clock output voltage to vary, the fast AGC system changes the drive on the final stages of the clock until the clock output voltage returns to the required 36-volt peak-to-peak level.

6-30. PRINCIPLES OF OPERATION. As figure 6-27 indicates, one half of the 12AT7 tube is used as a conventional triode amplifier, and the other half as a cathode follower.

As described previously, a constant-amplitude sine-wave signal is applied to pin 2 of the amplifier. A signal is also taken from one side of the secondary of the output transformer (either side may be used), and applied to pin 7 of the cathode follower through a delay line. The delay line must be adjusted

so that the signal applied to pin 7 is exactly in phase with the signal on pin 2 of the 12AT7. Both halves of the 12AT7 use a common 15K unbypassed cathode resistor. The AGC system operates under any one of three conditions: clock output voltage normal, low, or high. The sizes of voltage chosen as examples are merely easy to manipulate mathematically; they are not typical of system operation.

6-31. CLOCK OUTPUT VOLTAGE NORMAL. If a positive-going 15-volt peak signal is applied to pin 2 of the triode amplifier, a positive-going signal from the output transformer is applied to pin 7 of the cathode follower. The positive signal on pin 7 increases the plate current through the cathode follower and develops a positive-going signal across the 15K cathode resistor. The 15-volt signal applied to pin 2 increases the plate current through the amplifier. The increased plate current develops a positive-going signal across the cathode resistor. The total a-c voltage developed across the cathode resistor is now a positive-going 14-volt peak signal. Since the actual driving voltage on the triode amplifier is the difference in potential between the grid and cathode, the driving voltage becomes a positive-going 1-volt signal (15 volts minus 14 volts). The 1-volt signal is amplified by the triode and provides a normal plate voltage signal to be applied to the 6AG5 phase-splitter driver. This drive is sufficient to maintain a 36-volt peak-to-peak output voltage.

6-32. CLOCK OUTPUT VOLTAGE LOW. If the clock output decreases on one cycle, the amplitude of the signal applied to pin 7 falls below the normal level. This smaller grid signal causes a smaller voltage to develop across the cathode resistor. If the total a-c voltage developed across the cathode resistor is 13.5 volts, the effective driving signal on the triode amplifier becomes 1.5 volts (15 volts minus 13.5 volts), and a greater-than-normal plate-voltage swing develops. The phase-splitter stage, driver stages, and push-pull stages all are driven harder, and the clock output voltage increases to the desired 36-volt peak-to-peak level.

6-33. CLOCK OUTPUT VOLTAGE HIGH. If the clock output is above normal, the amplitude of the signal at pin 7 rises above the normal level. This larger grid signal causes a larger voltage to develop across the cathode resistor. If the total a-c voltage developed across the cathode resistor increases to 14.5 volts, the effective driving signal on the triode amplifier decreases to 0.5 volt (15 volts minus 14.5 volts), and a lower-than-normal plate voltage swing develops. The output stages receive less drive, and the output voltage decreases to the desired 36-volt peak-to-peak level.

6-34. SLOW AGC SYSTEM

6-35. GENERAL DESCRIPTION. The slow AGC circuit is a slow acting amplitude-stabilization circuit. It affects the clock output only if several successive cycles of the clock output voltage drift from their normal amplitude. If an abnormal condition (for example, a change in supply voltage, a defective tube, or a component variation) causes the clock output to vary, the slow AGC system adjusts the amount of drive on the last stages of the clock circuitry and returns the clock output voltage to the required 36-volt peak-to-peak level.

6-36. PRINCIPLES OF OPERATION. The slow AGC system (figure 6-27) consists of three tubes: an 0A3 voltage-regulator tube which maintains 75 volts between its electrodes, a 6AG5 pentode, and a 6AL5 diode. Four resistors are connected in series across the 0A3 tube. Because of the voltage-regulating action of this tube the total voltage across the series combination of resistors is 75 volts, and the voltage across R2 is 75 volts, clamping the cathode of the 6AG5 at -75 volts. The combination R1-C1, R12, R6, and R7 are connected in series between grid and cathode of 6AG5. The series-opposing voltages across this network determine the bias on the tube. Capacitors C1 and C2 filter out any a-c component and provide an almost steady d-c potential between cathode and grid of the 6AG5. The sum of the voltages across resistors R8 and R9, connected between grid and cathode, determines the bias on the 6AG7 voltage amplifier. The voltage across R8 is directly proportional to the magnitude of the plate current in the 6AG5, since R8 is the plate load resistor of this tube. If the plate current in the 6AG5 increases, the negative voltage across R8 increases, and the bias on the 6AG7 increases. If the 6AG5 plate current decreases, the negative voltage across R8 decreases, and the 6AG7 bias decreases.

Either phase of the clock output voltage may be applied to C3. When a positive alternation of the clock output is applied to C3, the 6AL5 conducts and charges C3. Current flows from the -150-volt supply through R10, R12, the movable arm, R1, and the 6AL5 to charge C3 negative on the left. The voltage developed across R1 fixes the bias on the 6AG5. Since C1 charges to the potential across R1 during positive input alternations, it maintains this voltage during negative input alternations, maintaining the bias on the 6AG5. During the negative alternation of the input signal, diode CR1 turns on and charges C3 negative on the right through C2 to ground. On the next positive input alternation the 6AL5 again conducts to charge C3 in the opposite direction.

Like the fast AGC system the slow AGC system may operate when the clock output voltage is normal, low, or high.

6-37. CLOCK OUTPUT VOLTAGE NORMAL. When the clock output voltage is normal, no change in voltage is desired. A signal of normal amplitude is applied to C3. On the positive alternation of the clock output signal the 6AL5 conducts and maintains the normal voltage across the R1-C1 combination. Since the bias on the 6AG5 remains unchanged, the plate current remains steady. The clock output voltage remains unchanged.

6-38. CLOCK OUTPUT VOLTAGE LOW. When the clock output voltage is low, the amplitude of the signal applied to C3 is below normal. Since C3 charges to a potential less than normal, the 6AL5 conducts less, and less voltage develops across the R1-C1 combination over several cycles. Decreasing the voltage across R1-C1 increases the bias on the 6AG5, decreasing the plate current in this tube. This decreasing plate current decreases the voltage drop across R8, decreasing the bias on the 6AG7. The 6AG7 produces a greater output signal which drives the remaining stages harder and increases the clock output voltage to the required 36-volt peak-to-peak level.

If only one cycle of the clock output voltage is low, the voltage across R1-C1 changes very little because of the filtering action of C1. Several low cycles are required to produce any measurable voltage decrease across R1-C1; hence the name slow AGC.

6-39. CLOCK OUTPUT VOLTAGE HIGH. When the clock output is high, the amplitude of the signal applied to C3 is greater than normal. To charge C3 to a larger potential, the 6AL5 must conduct more heavily. After several cycles of such operation, a measurable increase in the voltage across R1-C1 results. The increased voltage across R1-C1 decreases the bias on the 6AG5, causing it to conduct more heavily. The increase in plate current through the 6AG5 increases the voltage drop across R8, causing the bias on the 6AG7 to increase. When the bias on the 6AG7 increases, the output signal decreases, and the remaining stages of the clock circuitry have a reduced driving signal. The clock output voltage is reduced to the required 36-volt peak-to-peak level.

6-40. PHASE-CONTROL SYSTEM

6-41. GENERAL DESCRIPTION. The phase-control unit monitors both the A-phase and B-phase clock outputs and compares the phase of these signals with that of the sprocket output signal in a phase-detector circuit. If the clock output voltages shift from their desired phase relationship with the sprocket voltage, a current-variable inductor (increductor) adjusts the phase shift through the clock so that the output signals and the sprocket signal are again placed in the correct phase relationship. This minimizes storage-unit errors.

The principal factors capable of producing a change in the phase of the clock signals are as follows:

(1) changes in drum speed due to variations in line frequency or voltage

(2) changes in the clock supply voltages

(3) drifting of the clock components with age

(4) mistuning of the clock

(5) changes in clock loading during any given program

The phase-control system is a simple control loop consisting of a phase detector, an amplifier, a clock system, and an increductor. Any change in phase between the sprocket reference signal and the clock output signals produces a d-c voltage change at the output of the phase detector. This voltage change is converted to a current change in a 6AG7 pentode. The current change is then sent through the control coil of the increductor. The variable inductor adjusts the phase shift through the clock so that the output of the phase detector is minimized. The phase detector produces a null when the clock outputs are in quadrature with the reference signal; thus the action of the loop is to maintain a phase shift of nearly 90 degrees through the clock. The actual phase shift maintained by the closed loop is $(90^{o}-\emptyset)$, where $\emptyset$ is the offset or error angle necessary to produce the required correction signal.

6-42. PRINCIPLES OF OPERATION. The following facts about parallel resonant circuits are necessary to an understanding of the phase-control system. If an above-resonant frequency is applied to a parallel tuned (tank) circuit, the circuit appears to be capacitive. If a below-resonant frequency is applied, the circuit appears to be inductive. (The clock, which contains three cascaded parallel resonant circuits, displays a phase change of 2.26 degrees per kilocycle change of sprocket frequency.) If the applied frequency is held constant and the inductive reactance of the tank circuit increases, the circuit appears capacitive and produces a lagging output voltage. If the frequency is held constant and the inductive reactance decreases, the circuit appears inductive and produces a leading output voltage.

The phase-detection unit of the system consists of three tubes (figure 6-27). Both halves of a 6AL5 duodiode (V1, V2) are used as the phase discriminator. An OA3 voltage regulator tube is used as the stable element, and a 6AG7 pentode is used as a d-c amplifier.

The voltage-regulating action of the 0A3 develops a constant 75 volts across the combination of R4 and R11. The 0A3 maintains a 75-volt drop across R17, clamping the cathode of the 6AG7 at -75 volts. The bias on the 6AG7 is determined by the summation of the voltages developed across the top of R4, R16, and R15, connected between the grid and the cathode. The two 1000-μμf capacitors filter out any a-c components and maintain a steady d-c bias on the 6AG7. If the voltage between points A and B of the phase-discriminator output circuit equals zero (no discriminator output), the bias on the 6AG7 is determined by the setting of the movable arm on R4.

To operate, a phase discriminator requires a common reference signal applied to the two diodes in the circuit. In this case, the reference signal is a sprocket signal taken from the plate of the 6AH6 sprocket voltage amplifier, and developed across coil L1. Any voltage developed across this coil is common to V1 and V2. The plate circuit of V1 includes R13, L1, and R15. The plate circuit of V2 includes R14, L1, and R16.

Resistors R13 and R14 form part of a voltage-divider network across the clock output transformer. These resistors are connected so that the voltage at the top of R13 is 180 degrees out of phase with the voltage at the bottom of R14. When the A phase of the clock output is positive and the B phase negative, electrons flow from the negative B-phase side of the transformer through C8, R18, R14, R13, R17, and C7 to the positive A-phase side of the transformer. With respect to the common connection (reference point) between R13 and R14, the bottom of R14 is negative and the top of R13 is positive. The voltages across R13 and R14 are always equal in amplitude and 180 degrees out of phase with each other. If the polarity of the A-phase and B-phase clock outputs are reversed, the polarity of the voltages across R13 and R14 will reverse, but their phase relationship remains the same.

Figure 6-21a is a vector diagram of the voltages developed across R13 and R14 with respect to their common connection when the A phase of the clock output is positive. In figure 6-21b the reference voltage E_{L1} developed across coil L1 has been added.

Since the total voltage across V1 (E_{V1}) is the vectorial sum of E_{L1} and E_{R13}, and the total voltage across V2 (E_{V2}) is the vectorial sum of E_{L1} and E_{R14}, the total voltage across each tube can be determined as in figure 6-21c.

If the phase relationship shown in figure 6-21c exists between the clock outputs and the sprocket signal, E_{V1} equals E_{V2}. This is the normal condition when the clock outputs and

the sprocket signal are in their proper phase relationship and no phase change is required. Since the voltages across V1 and V2 are equal, the plate current in V1 equals the plate current in V2. The current through V1, R13, L1, and R15 is equal to the current through V2, R14, L1, and R16. These currents develop equal voltages across R15 and R16. Since the resistors are connected back-to-back, there is no voltage difference between point A and point B. The discriminator, which is now considered to have no output, does not alter the bias on the 6AG7 nor the phase of the clock output signals. The clock outputs and the sprocket signal are now in their correct phase relationship.

It is possible for the discriminator to operate under two conditions other than the normal zero-output condition just described: with the phase of the clock output advanced, or with the phase retarded.

6-43. PHASE OF CLOCK OUTPUT ADVANCED. The phase of the clock output may shift ahead of the correct phase relationship with the sprocket (reference) signal because of changes in clock loading during a given program. To correct this condition, the inductive reactance of the second tank circuit is increased. The tank circuit then appears capacitive and the phase of the output signals shifts back until the clock output and the sprocket signal resume the correct phase relationship.

A vector diagram (figure 6-21d) shows what happens to the voltages across V1 and V2 when the phase of the clock output advances. Voltages E_{R13} and E_{R14} are still equal in amplitude and 180 degrees out of phase. Their phase advance is indicated on the vector diagram by the counterclockwise rotation of the vectors E_{R13} and E_{R14}. When the voltages across the resistors are added to the reference voltage E_{L1}, E_{V2} is greater than E_{V1}. Increasing the voltage across V2 increases the plate current. The current through R16 and V2 becomes greater than that through R15 and V1. The voltage developed across R16 becomes greater than the voltage arcoss R15 and point A of the discriminator output circuit becomes negative with respect to point B. As point A of the input circuit becomes more negative, the bias on the 6AG7 increases. As the bias increases, the plate current and the current through the bias and control windings of the increductor decreases. As the control current decreases, the inductance (and hence the inductive reactance) of the signal winding increases (figure 6-23), detuning the second tank circuit and shifting the phase of the clock outputs into the correct phase relationship with the sprocket signal. When the correct phase relationship is attained, no further corrective voltages are developed between points A and B of the detector output circuit.

6-44. PHASE OF CLOCK OUTPUT RETARDED. When the phase of the clock output lags the correct position in relation to the sprocket (reference) signal, the inductive reactance of the second tank circuit is decreased. The tank circuit then appears inductive, and the phase of the output signals shifts ahead until the clock output and the sprocket signal resume the correct phase relationship.

A vector diagram (figure 6-21e) shows what happens to the voltages across V1 and V2 when the phase of the clock output is retarded. Voltages E_{R13} and E_{R14} are still equal in amplitude and 180 degrees out of phase. Their phase shift is indicated by the clockwise rotation of the vectors E_{R13} and E_{R14}. When the vectorial sum of the voltages across the resistors and the coil is calculated, E_{V1} is greater than E_{V2}. Tube V1 draws more plate current than V2, and the current through R15 and V1 becomes greater than that through R16 and V2. The voltage across R15 becomes greater than the voltage across R16, and point A of the discriminator output circuit becomes positive with respect to point B. As point A becomes more positive the bias on the 6AG7 decreases, and both the plate current and the current through the bias and control windings of the increductor increase. As the control current increases, the inductance (and hence the inductive reactance) of the signal winding decreases (figure 6-23), detuning the second tank circuit and shifting the phase of the clock outputs into the correct phase relationship with the sprocket signal. When the correct phase relationship is attained, no further corrective voltages are developed between points A and B of the detector output circuit.

The sensitivity of the phase detector is approximately 45 millivolts per degree phase shift. The d-c output voltage as a function of the phase shift is plotted in figure 6-21f. The output voltage has a unique amplitude and polarity for each phase angle between zero and 180 degrees. Below zero and above 180 degrees the phase-detector output repeats itself. Correct sensing of the phase loop occurs only in the region between points A and B. If gross mistuning caused the operating point of the detector to move out of that region (for example, to point C), the phase loop would introduce a phase error instead of correcting one. Under clock alignment procedure, the maintenance manual describes sensing tests that guarantee correct operation of the phase detector.

6-45. CHANGE OF SPROCKET FREQUENCY. If the drum-motor power-line frequency varies there is a corresponding change in the drum speed, and hence a sprocket frequency change. Even with a variation in sprocket frequency the clock phase shift remains constant at about 90 degrees. The method by which this constant phase shift is maintained will now be described with

the aid of a set of curves in which phase is plotted as a function of frequency.

Assume that the total phase response of the clock circuit is as shown in figure 6-24, and that the phase-control unit is not operative (open loop). Assume a drum speed that produces a sprocket frequency of fo (707 kilocycles). Since all three tank circuits are tuned exactly to fo, they appear resistive, and the clock phase shift is 90 degrees.

Now assume a decrease in power-line frequency such that the sprocket frequency decreases to f1. As the sprocket frequency decreases below the resonant frequency of the tank circuits, each tank circuit appears inductive and produces a leading output voltage. In the example in figure 6-24, chosen for mathematical convenience only, the sprocket frequency decreases until each tank circuit introduces a phase shift of +15 degrees. The total phase shift introduced by the three tank circuits is then +45 degrees. When this is added to the normal 90-degree phase shift of the clock, the clock phase shift becomes 135 degrees. The phase of the clock output shifts to phase 1, and the operating point of the drum-clock system is point P.

The phase of the clock output signals is now advanced from its normal relationship to the sprocket signal. Closing the phase-control loop while the sprocket frequency is at f1 causes V2 to be driven harder than V1. As shown in figure 6-21, the phase-detector output is negative. Less current flows through the increductor control and bias windings; hence, the inductive reactance of the second tank circuit increases. The resonant point of the second tank circuit then shifts so that the clock phase shift returns to about 90 degrees.

Figure 6-25 shows the phase-control loop during correction. The starting phase trace (same as figure 6-24) is labeled tanks 1, 2, and 3 and represents the algebraic addition of the phase shifts in each of the three tanks in cascade. As the resonant frequency of the second tank circuit decreases, the circuit contributes less and less to the total clock phase shift. At f1 it contributes no phase shift. When the second tank circuit contributes no phase shift, the total clock phase shift is determined by the algebraic addition of the phase shifts produced by tanks 1 and 3 plus the normal 90-degree phase shift introduced by the remaining clock circuitry. The trace of the clock phase takes on a decreased slope, and the total clock phase is now +120 degrees instead of +135 degrees.

As shown in figure 6-26, the second tank circuit introduces a lagging phase shift as its resonant frequency decreases below f1. When the resonant point reaches f2, the second tank

circuit introduces a phase shift of -30 degrees. Since this is equal and opposite to the phase shift introduced by tanks 1 and 3, the total phase shift of the three tank circuits is zero. The total clock phase shift is restored to 90 degrees, and the signals applied to the phase detector are again in quadrature.

All changes in the resonant point of the second tank circuit are brought about automatically by the changing current in the increductor control and bias windings.

The phase-control system corrects for an increase in sprocket frequency in the same way, but the sign of the phase shift introduced into the tank circuits is opposite to that just described.

6-46. VOLTAGE AND CURRENT MONITORS

Measurements can be made at the meter panel of the B-supply, screen-grid, and control-grid bias voltages applied to the six 4X250B output tubes (figure 6-27) by rotating the voltage selector (SW57). By rotating the current selector (SW48) the increductor current, the cathode current of the individual output tubes, and the total plate current of all six output tubes can be measured.

The 0 - 500 volt d-c meter is used to measure the d-c voltage applied to the six output tubes. With switch SW57 on position 2, the meter reads the 300-volt screen-grid voltage. With the selector switch on position 3, the meter reads the 50-volt control-grid bias. With the selector switch on position 1, the range of the meter is extended to 2000 volts (E x 4) by the use of a 3-megohm multiplier resistor. Then, a meter reading of 400 volts indicates that the B-supply voltage is 1600 volts (400 x 4).

A 2-ohm wirewound resistor in the cathode lead of each of the output tubes provides a means for monitoring the cathode current of each tube. Each 2-ohm resistor is followed by an isolating network that prevents radio frequencies (RF) from being applied to the meter. The d-c plate return lead is connected to the centertap of the output tank coil. The total plate current drawn by all six output tubes passes through a 1-ohm resistor between the centertap and ground. The 1-ohm resistor provides a convenient monitoring point for the total plate current of the output stage. Since the increductor current passes through the 100-ohm resistor in the plate circuit of the 6AG7, this resistor is used as the monitoring point for the increductor current.

The range of the 0 - 50 microammeter is extended for all readings. To read the increductor current (selector switch

in position 8), the range is extended to 25 milliamperes ($I \times 5 \times 10^2$). To read the individual cathode currents (switch positions 2 through 7), the range is extended to 0.5 ampere ($I \times 10^4$). To read the total plate current (position 1), the range is extended to 2 amperes ($I \times 4 \times 10^4$).

The total plate current is less than the sum of the individual cathode currents because of the screen-grid and control-grid currents. It is possible to diagnose a condition of a shorted control grid or screen grid at the meter panel by noting that the cathode current increases above its normal level with no corresponding increase in total plate current. To do this, however, accurate records of the normal current readings must be kept.

One characteristic of the 4X250B tetrodes is the appearance of a reverse screen current at certain values of plate and control grid voltage. According to the tube manufacturer this is a normal condition for this type of tube. Should the screen current of the clock ever be monitored separately, a negative or reverse current would be considered normal.

6-47. MAGNETIC AMPLIFIERS

6-48. GENERAL DESCRIPTION

Basically the magnetic amplifier is a transformer in the form of a ring-type saturable core (toroid). Magnetic amplifiers offer the advantages of intrinsic reliability, low power consumption, small size, and long life expectancy.

The prime purpose of the magnetic amplifier, as of any other type of amplifier, is to produce an output signal that is a function of the input signal, but has increased power, or voltage, or both. In the magnetic amplifiers used in the system, the output current is greater than the input current. The power gain of a magnetic amplifier is inversely proportional to the applied signal frequency. At 707 kc, the signal frequency used, there is a power gain of approximately seven. Power gain is defined here as the number of amplifiers that can be driven by a single magnetic amplifier of the same type. This may also be referred to as output ability.

The magnetic amplifiers described here are of the series-pulse type. They are employed in two basic configurations, complementing and noncomplementing. The designation series indicates that the magnetic amplifier acts as a variable impedance in series with the load. The pulse type of magnetic amplifier, as distinguished from the carrier type, is an intrinsically digital device, one characteristic of which is that it standardizes the pulse width, amplitude, and time; all are important considerations in computer applications. A complementing magnetic amplifier produces an output opposite from the input. It gives full output when there is no input signal, and no output when an input is applied. It may be compared to a normally closed single-pole relay in which the relay is energized by the input signal. In the absence of an input, the contacts remain closed, and an output is developed. If an input is applied, the contacts open, and no output signal can be developed. The noncomplementing amplifier is designed to produce an output signal only in the presence of an input signal. It may be compared to a normally open single-pole relay. If no input is applied to the relay coil winding, the relay contacts remain open, and no output signal results. If an input signal is applied, the relay coil is energized, the relay contacts close, and an output signal is developed. Since less power is required to operate the relay than may be transferred by the relay contacts, the device may be considered a power amplifier.

The operation cycle of a magnetic amplifier is divided into two parts of equal duration. During the first half of the cycle, input information is applied to the primary (input winding). The comparable signal in the relay analogy is the signal

applied to the relay coil. Depending upon the relay type, this signal either opens or closes the relay contacts so that they offer either an infinitely high resistance or zero resistance to the passage of an output signal. In the magnetic amplifier, the input signal sets the core so that the secondary (output winding) offers either a high or a low impedance, depending upon the magnetic amplifier type, to any output signal attempting to pass through this winding. During the second half of the cycle a power pulse is applied to the secondary or output winding and, depending upon the core setting established during the first half cycle, a large or a very small current is permitted to flow through the winding. The magnitude of the current determines the output of the magnetic amplifier.

The input and output signals are of different phase, and the output is lagging the input by 180 degrees. Thus, at a frequency of 707 kc, there is a pulse time delay of 0.707 microseconds (1/707kc x 1/2) in going through each amplifier.

On both the complementer and the noncomplementer the numbered terminals on the coil windings refer to the pin numbers of the header in which the core is mounted.

6-49. BASIC PRINCIPLES OF OPERATION

Before attempting a detailed analysis of the complementing and noncomplementing magnetic amplifiers, a brief discussion of some of the theoretical concepts utilized in these devices is in order.

6-50. MAGNETIZATION CURVES. To represent the way flux density (B) in a magnetic material varies with the magnetizing force (H), B-H curves are used in which flux density is plotted as a function of the magnetizing force (figure 6-28). The quantity B is measured in gausses, one gauss being equal to one magnetic line of force per square centimeter or 6.45 lines per square inch. The quantity H is measured in oersteds, one oersted being equal to 0.4π ampere turns per centimeter or 2.015 ampere turns per inch.

If an a-c source is applied to a coil wound around a magnetic material (figure 6-29), the core first is magnetized to positive flux saturation, designated $+B_S$, when the current flows in the first direction (figure 6-28a). When the current decreases to zero, the magnetizing force (H) decreases to zero also, but the flux density, or measure of magnetization, is only partially reduced. The residual flux present when the magnetizing force is zero is called remanence and is designated B_r (figure 6-28b).

During the next alternation of the applied source the magnetizing force is applied in the opposite direction because the current flow is reversed. A point is reached at which the flux density is reduced to zero (figure 6-28c). The amount of magnetizing force of opposite polarity which must be applied to decrease the flux density to zero is called the coercive force and is designated H_C.

As the magnetizing force is increased further the core flux density increases to negative flux saturation, designated $-B_S$ (figure 6-28d). As the magnetizing current again decreases to zero (figure 6-28e), the flux density decreases to $-B_r$. The quantities $+B_r$ and $-B_r$ have the same magnitude but opposite direction.

During the next alternation the core is again driven to $+B_S$, and on all subsequent cycles the core traces the loop indicated in figure 6-28f. The complete loop, called the hysteresis loop, indicates the lag in changes of flux density (B) behind changes in the magnetizing force (H). The enclosed area is a measure of the energy lost in the core material during a given cycle. The H_C and B_r points are determined by the appropriate intercept of loop and axis.

6-51. COIL IMPEDANCE VARIATIONS. If a voltage source is applied across a coil (figure 6-29), a magnetic field expands out from each turn, linking all of the other turns of the coil as the current through the solenoid increases. The expanding magnetic field induces into every turn of the coil a voltage of a polarity that tends to oppose the original current that produced the field. The magnitude of this induced voltage in each turn of the coil is proportional to the rate of change of the magnetic field. The total voltage induced in the coil is the sum of the voltages induced in the individual turns and must be equal to the applied or source voltage, since there are no other voltage drops in the circuit. The impedance offered by the coil may be thought of in terms of the amount of current required to induce the given voltage in the coil.

If two cores with the hysteresis loops indicated by figure 6-30 are placed individually across the same source voltage as in figure 6-28, they both have the same induced voltage, since the source voltage is the same for both coils. However, the amount of current necessary to induce this voltage is not the same for both cores. In one core the amount of current indicated by point B in figure 6-30 flows during switching time; in the other core a smaller current, indicated by point A, flows. Since the voltage across both coils is the same but the currents through the coils are different, the coil drawing less current has the higher impedance ($Z = E/I$).

After a core reaches saturation, the current rises to a value limited only by circuit resistance. When the core is saturated there is no appreciable flux change for increases in current, and hence no induced voltage. The core can now be considered a short circuit.

The permeability of a coil, designated μ, is the ratio of flux change to change in magnetizing force ($\mu = \Delta B/\Delta H$). Since the hysteresis loop is nonlinear, the permeability is maximum when the core is switching and minimum when the core is at or near saturation. The induced voltage is maximum when the permeability is maximum, which occurs only during switching time.

The back emf or induced voltage depends upon the change in flux density and ceases to oppose current flow if the flux density does not continue to vary. This property of coils, called inductance, decreases current flow only during transient flux conditions, and is the reason a coil offers a high impedance to ac and practically no impedance to steadily applied dc.

Assume that a core is in the state of magnetization indicated by $-B_r$ in figure 6-28f. If a voltage across the winding causes current of such a direction as to switch the core to $+B_s$, the operating point moves up the loop from $-B_r$ toward $+B_s$. During this switching operation the permeability is maximum. As the flux changes direction and increases in the positive direction, it induces in the coil a back emf which opposes the original current flowing through the coil. Since the amplitude of current flowing through the coil is kept small for a given applied voltage, the coil may be thought of as offering a high impedance to this current. If the applied pulse is of just sufficient duration to switch the core, the coil offers a high impedance for the entire duration of the pulse. If the applied pulse is of longer duration, the coil offers a high impedance during the time the core switches from $-B_r$ to $+B_s$ and a low impedance for the remainder of the pulse duration.

If a core is at $-B_r$ and a voltage is applied which tends to drive the core to $-B_s$, there can be little flux change, since the core is nearly saturated already for magnetizing currents in this direction. Since there is effectively no flux change, no back emf is induced to limit current flow through the coil. The coil then is practically a short circuit, and a large current flows, limited only by circuit resistance.

To summarize, a coil exhibits a high impedance when the flux change is maximum; that is, when the core is switching from $-B_r$ toward $+B_s$ or from $+B_r$ toward $-B_s$. When the core is driven from remanence to the same polarity saturation, say from

$+B_r$ to $+B_s$, the impedance is very low at the time of application of the pulse. The high current which flows quickly drives the core to saturation, at which time the coil becomes essentially a short circuit. The coils on magnetic amplifiers are considered high-impedance devices during the increment of time in which the core is switching in either direction, and low-impedance devices at all other times.

6-52. CORE MATERIALS

The magnetic circuits described here use cores fabricated with a magnetic material exhibiting a more rectangular hysteresis loop than the one indicated in figure 6-29f. These cores, of toroidal construction, use a nonmagnetic stainless-steel bobbin to support the wraps of 4-79 Molybdenum-Permalloy magnetic tape that comprise the magnetic material in the core. The ratio of remanent flux density to saturation flux density (B_r/B_s) is the squareness ratio of the magnetic material. Ideally the ratio should be unity. To maintain a ratio near unity requires that there be no air gap in the magnetic path. Therefore, wrapped core construction is required. As many wraps are applied as are necessary to accommodate the required flux density.

If a positive voltage is applied when a core is at $-B_r$ (figure 6-31), the current rises instantly to a value corresponding to H_c. Since the bottom of the B-H loop is flat, there can be no flux change and hence no induced emf to oppose the buildup of current until the magnetizing force reaches H_c. When this value of magnetizing force is reached the flux begins to reverse, and the operating point moves up the B-H loop from $-B_r$ toward $+B_s$ at a linear rate.

The counter emf generated by the rate of flux change opposes the applied voltage and limits the current to a value corresponding to H_c. In the ideal B-H loop with vertical sides, where ampere turns do not vary, the current required for switching is constant until saturation is reached. The core then appears as a current sink while switching.

When the core reaches saturation there can no longer be any flux change and no counter emf can be developed. If the applied voltage is maintained the current rises to a large value limited only by circuit resistance.

If a negative voltage is applied when the core is at $-B_r$ there can be no flux change, since the core is already saturated for currents in this direction. Since there is no flux change, no voltage is developed across the winding except the IR drop of the winding. Thus the core immediately becomes a short circuit, and a large current flows, limited only by circuit resistance. Theoretically there is no time delay.

If the core is switching because of an applied voltage, and the voltage is removed when the operating point is at location 1 (figure 6-32), the core shifts back to location 2 on the H = 0 axis with no flux change. The coil is entirely nonreactive with no recovery of energy when the driving force is removed. The core then is a power-consuming element requiring an energy input to switch the core from one remanent point to the other.

While a perfectly rectangular loop (figure 6-31) is to be desired, practical limitations require that the loops for the cores of the magnetic amplifiers have a slight slope. This slope increases as the applied frequency increases.

6-53. COMPLEMENTING MAGNETIC AMPLIFIER

The complementer is designed to produce an output that is always the complement of the input. Full output voltage is developed in the absence of an input signal, and no output is developed if an input is applied. Figure 6-33b shows the waveforms.

The complementer has an input winding of 100 turns and an output winding of 300 turns.

Because the power pulses and blocking pulses used in the system are developed in a common source, the clock, the 180-degree phase difference between them remains fixed. Positive input signals are applied only when the power pulse is negative and the blocking pulse positive. The square polarity symbols shown on the core windings (figure 6-33a) indicate that the signals at the dotted ends of the two coils are of the same polarity at any given time. When a signal is applied to either winding, transformer action induces a voltage in the other winding that causes the dotted end of the second coil to assume the same polarity as the dotted end of the first coil.

The complementer can operate under any of the four conditions described here and shown in figure 6-33b.

6-54. CONDITION 1. Condition 1 is that there is no input, the power pulse is negative, and the blocking pulse is positive. Terminal 3 of the input winding (figure 6-33a) clamps at ground potential through input diode CR1 and diode CR5 of the previous stage. Terminal 1 of the input winding clamps at +3 volts through CR2. A circuit is now complete so that current may flow from the negative clock through R1, from terminal 3 to terminal 1 through the input winding, and through CR2 to +3 volts. Regardless of the core setting before the power pulse, this current flow drives the core to $+B_s$ (figure 6-28f).

6-55. CONDITION 2. Condition 2 is that the power pulse is positive and the blocking pulse negative, following a no-input cycle. The positive power pulse disconnects diodes CR1 and CR2 (figure 6-33a). The whole input winding is clamped at power-pulse potential, and no current can flow through the input coil. The input winding is prevented from interfering in the output circuit since it cannot now induce a voltage in the output winding. The positive power pulse also turns on CR3 and enables current to flow from the -29-volt supply, through RL, the output winding, and CR3 to the positive clock. This current tends to drive the core to $+B_S$, but since the core is already reset to $+B_r$ from condition 1, the output winding is effectively a short circuit to this current. Practically the entire power-pulse voltage develops across RL, providing an output. This satisfies the first requirement of the complementer; that is, an output is developed in the absence of an input signal. The negative blocking pulse received at this time turns off CR4, giving the output winding complete control over current flow in the output circuit.

6-56. CONDITION 3. Condition 3 is that the power pulse is negative, the blocking pulse is positive, and a positive input is applied. The negative power pulse clamps terminal 1 of the input winding to +3 volts through CR2. The positive input raises terminal 3 of the input winding above 3 volts, providing a circuit for a current from the negative clock through R2, from terminal 1 to terminal 3, through the input winding, and through CR1 to the positive input potential. The current is sufficient to set the core at $-B_S$ and it flows in such a direction as to drive the end of the input winding with the polarity symbol negative with respect to the other end. Transformer action induces a negative potential in the end of the output winding with the polarity symbol. The induced voltage tends to turn on CR3. Turning on CR3 would allow a current to flow through the output winding which would pull the core part way back up the loop. During the next cycle, when the power pulse became positive, the core would reach $+B_S$ before the end of the power-pulse duration, and a sneak output would develop. To prevent this undesirable output, the blocking pulse goes positive during the input cycle and turns on CR4, putting the output winding at a positive potential. Diode CR3 is held off by the positive potential and no current flows through the output winding. The blocking pulse counteracts the effect of the induced voltage in the output winding and prevents the development of a sneak output.

6-57. CONDITION 4. Condition 4 is that the power pulse is positive and the blocking pulse negative, following an input signal. The positive power pulse turns off CR1 and CR2, clamping the entire input winding at power-pulse potential. No current can flow through the input winding. The power pulse also turns on CR3, completing a circuit for a current from the

-29 volt supply, through RL, the output winding, and CR3 to positive clock potential. The current flows in such a direction as to set the core at $+B_S$. The core is already reset to $-B_r$. The positive power pulse causes the core to switch, and cores in a switching condition offer a high impedance. The small switching current through the output winding does not cause any output across RL. This satisfies the second requirement of the complementer; that is, no output is developed in the presence of an input signal.

To prevent the switching current through the output winding from causing a sneak output across RL when the power pulse is positive, a circuit from the -29-volt supply clamps the top of RL to ground through CR5. If a positive power pulse is applied when the output winding is at a high impedance, a small current flows through the output winding. The current through CR5, however, decreases by the same amount, and the net current change through RL equals zero. If the output winding is in a state of low impedance, the large increase in current upon application of a positive power pulse cannot be neutralized by the sink circuit, and an output develops.

Resistors R1 and R2 are both current-limiting. If the signals described in condition 3 are present, R1 limits the current flowing from the negative clock, through R1 and CR1 to the positive input potential. If the input winding shifts to a low-impedance state prior to the completion of the input and power pulses, R2 limits the current flowing from the negative clock, through R2, from terminal 1 to terminal 3 through the input winding and through CR1, to the positive input. This prevents shorting the output of the previous amplifier. If no input is provided, R1 limits the current flowing from the negative clock through R1, the input winding, and CR2 to +3 volts.

The power pulses must be of just sufficient duration to switch the core. Since the core offers a high impedance when switching and a low impedance when saturation is reached, an extraneous output signal develops if the power pulse is of longer duration than the switching time.

6-58. NONCOMPLEMENTING MAGNETIC AMPLIFIER

The noncomplementer is designed to produce no output in the absence of an input signal and full output voltage only in the presence of an input signal. See the waveforms in figure 6-34b.

In addition to an input winding of 100 turns and an output winding of 300 turns, as in the complementer, the noncomplementer has a bias winding of 25 turns. While the noncomplementer could be designed to operate with only two windings,

as in the arithmetic registers, other design considerations make it advisable to include the third (bias) winding on standard amplifiers. The bias winding as employed here does not develop sufficient magnetizing force by itself to switch the core in either direction. For a switching operation the bias winding is used in conjunction with either the input or the output winding.

As in the complementer, the sine-wave pulses used to drive the unit are taken from the low-impedance clock source. The following analysis assumes that the frequency, amplitude, and phase relationship of the applied signals remain constant.

The noncomplementer can operate under any of the four conditions described here and shown in figure 6-34b.

6-59. CONDITION 1. Condition 1 is that there is no input, the power pulse is negative, and the blocking pulse is positive. The negative power pulse turns on CR1 and clamps terminal 3 of the input winding to ground through input diode CR1 and diode CR5 of the previous stage. Diode CR2 turns on and clamps terminal 1 of the input winding to the positive blocking-pulse potential. A circuit is now complete for current to flow from the negative clock, through R1, from terminal 1 to terminal 3 through the input winding, and through CR2 to positive blocking-pulse potential. At the same time current flows from the clock through R3 and the bias winding to ground. The combined effect of the currents through the input and bias windings is sufficient to drive the core to $-B_s$. Transformer action induces in the output winding a voltage of such polarity that the end of the winding with the polarity symbol is negative. The induced voltage tends to turn on CR3. Turning on CR3 would allow a current to flow through the output winding, pulling the core partly back up the loop. During the next cycle, when the power pulse became positive, the core would be driven to $+B_s$ before the end of the power-pulse period, producing a sneak output. To prevent this undesirable output, the positive blocking pulse turns on CR4, places the output winding at a positive potential, keeps CR3 cut off, and insures that the negative power pulse drives the core all the way to $-B_s$.

6-60. CONDITION 2. Condition 2 is that the power pulse is positive and the blocking pulse negative, following a no-input cycle. At the beginning of this cycle the core is reset to $-B_r$ from condition 1. The positive power pulse turns off CR1 and CR2, causing both input winding terminals 1 and 3 to equal the power-pulse potential. No current can flow through the input winding since both ends of the coil are at the same potential. The negative blocking pulse also tends to reduce enhancement (back current) through CR2. The power pulse turns on CR3, and a circuit is complete for a current from the

-29-volt supply through RL, the output winding, and CR3 to positive clock. This current tends to drive the core toward $+B_s$. In switching from $-B_r$ toward $+B_s$, the core offers a high impedance. The current through the output winding is reduced further by the action of the bias winding. The positive power pulse causes a current from ground through the bias winding, and R3 to the positive clock, leaving terminal 6 positive with respect to terminal 4. By transformer action the bias winding induces a voltage in the output winding that makes terminal 9 positive with respect to terminal 7. The induced voltage is of such polarity that it reduces the current through the output winding so that no output signal is developed. This satisfies the first requirement of the noncomplementer; that is, no output is developed in the absence of an input.

The power pulse applied to the output winding must not switch the core from $-B_r$ all the way to $+B_s$. If the core is driven all the way to $+B_s$, it presents a low impedance and permits an extraneous output to develop.

6-61. CONDITION 3. Condition 3 is that the power pulse is negative, the blocking pulse is positive, and a positive input is applied. The negative power pulse and positive input pulse turn on CR1 and raise terminal 3 of the input winding to the positive input potential. The power pulse and the positive blocking pulse turn on CR2, placing terminal 1 of the input winding at blocking-pulse potential. Current can now flow from the negative clock through R2, where a parallel path forms. One circuit is through CR2 to the positive blocking-pulse potential; the other is through the input winding, CR1, to the positive input terminal. The second circuit is the one of prime interest here because at the same time a circuit is complete from the clock, through R3, bias winding, to ground. The currents through the input and bias windings oppose each other. The core remains at $+B_r$ from condition 2. The function of an input signal is to prevent resetting the core from the previous output cycle. The polarities of the power pulse and blocking pulse turn off CR3 and insure no current in the output circuit.

6-62. CONDITION 4. Condition 4 is that the power pulse is positive and the blocking pulse negative, following an input signal. The positive power pulse turns off CR1 and CR2, placing terminals 1 and 3 of the input winding at power pulse potential. Hence no current flows through this winding. The power pulse also turns on CR3 when the blocking pulse turns off CR4. A circuit is now complete from the -29-volt supply through RL, the output winding, and CR3 to the positive clock. This current tends to drive the core to $+B_s$, but since the core is already at $+B_r$, it presents a short circuit. The

circuit voltage develops across RL, providing an output. This satisfies the second requirement of the noncomplementer; that is, an output is developed in the presence of an input.

The noncomplementer includes a current sink circuit made up of RL and CR5 which serves the same purpose as in the complementer described previously. Resistors R1, R2, and R3 are used as current-limiting resistors.

In figures 6-33b and 6-34b, the input and output signals contain a 10-volt peak signal in addition to the 18- to 20-volt information pulses. These 10-volt signals are developed by the blocking pulses and have no logical significance. The blocking pulses applied to a stage appear in the output of that stage 180 degrees out of phase with the regular output signal and approximately one-half the amplitude of the output. These blocking pulses appear at the input of the driven stage, but they are not of the correct phase to cause any logical effect on the stage.

6-63. POWER REQUIREMENTS

In the complementer the only input current (22 ma) is that necessary to switch the core from $+B_S$ to $-B_r$. In the noncomplementer the input current must overcome the magnetomotive force set up by the current through the bias winding and prevent the core from resetting to $-B_S$. The input requirements for the noncomplementer are therefore slightly higher than those for the complementer, and the input current is about 30 ma. The output current for both of these units is 150 ma.

One complementer can drive seven others (inputs of 22 ma each). The output of one noncomplementer (150 ma) can drive five similar units (inputs of 30 ma each). Since any magnetic amplifier seldom drives all complementers or all noncomplementers, it is convenient to express power in terms of drive units.

Given a value of 4.3 ma to one drive unit, and using round numbers, the input to the complementer is five drive units (22/4.3) and the output is 35 drive units (150/4.3). The input to the noncomplementer is seven drive units (30/4.3) and the output is 35 drive units (150/4.3).

Frequently it is desired to drive more cores than is possible with a standard single-power core; that is, an output of more than 35 drive units is required. To gain output power, a special double-power core is used instead of two standard cores connected in parallel. The double-power core has about twice the volume of magnetic material of a single-power core,

and therefore requires twice the input power, 10 drive units being required for a complementer and 14 drive units for a noncomplementer. Because of the larger physical size, however, the space factor of the output winding is improved. Consequently, it is possible to furnish three times the standard output current before the output inductance and resistance limit the output current. The output of a double-power core is 105 drive units.

The circuit for a double-power core is practically identical with that for a single-power core. The only change is that resistors of different value are used and the output diode (CR3) is replaced by three diodes in parallel because of the increased current requirements of the circuit.

6-64. MUTUAL EXCLUSION

In the system, a magnetic amplifier may be connected to any number of driving sources. An amplifier, however, may receive only the allotted number of drive units at the input, regardless of the number of amplifiers driving it. If two amplifiers together are driving a total of seven complementers, the output current from each driver stage is about one-half the full output current. Only that current required by the driven units may be taken from an amplifier output. If the driven units are already supplied from other sources, the output current may be much less than maximum.

In many instances a magnetic amplifier with an output of 35 drive units is connected to more inputs than one unit could normally drive. More than one driving source is connected in such circuits, and the system is so designed that no one unit ever is required to supply more than 35 drive units. Also, if an amplifier is at no time the sole driving source for the cores to which it is connected, additional loads may be added until its effective load equals its maximum driving ability.

6-65. MAGNETIC AMPLIFIER CIRCUIT VARIATIONS

6-66. ARITHMETIC REGISTERS. An arithmetic register stores computer information for any desired period of time. Because of the inherent delay of magnetic amplifiers, one pulse time is required to pass a signal through two magnetic amplifiers in cascade. A series of 24 magnetic amplifiers provides sufficient delay to store the 12 digits of a computer word. If the output of the last amplifier is applied to the input of the first amplifier, a recirculating path is provided which can store the word for an indefinite period.

Since the only logical function the noncomplementer serves in the computer is to delay a signal, it is well adapted for the arithmetic register units. An arithmetic register is made up of a string of noncomplementers designed only to delay information for a given time. The noncomplementers used for this purpose have an S (special) or a T (transition) designation to indicate that they are slightly different from standard noncomplementers.

The noncomplementers used in the arithmetic registers have no bias windings to assist in core setting. The input to one of these cores must therefore be increased to ten drive units. Since one core drives only one other core in the register, the output of each core is reduced to about ten drive units, and the sneak-suppressor circuits may be omitted. Since there is only one input line to each core and no isolation of inputs is required, the input diodes also may be omitted. All low-power units containing no input diode and no sneak-suppressor circuit have an S designation.

Because the output of an arithmetic register may serve as input to several circuits simultaneously, a low-power S unit cannot be used in the output stage. The output stage of an arithmetic register is a standard noncomplementer with an output of 35 drive units. The input to the standard unit must have a ground reference level and contain no sneak signal. The stage immediately preceding the output stage then must contain a sneak-suppressor and a pulldown circuit. When a low-power core contains this output circuit (transition circuit), it has a T designation.

To summarize, the arithmetic register is made up of a series of S-type noncomplementers. The output stage is a standard noncomplementer, and the stage immediately preceding it is a T-type unit.

Figure 6-35 shows a simplified arithmetic register circuit capable of providing two pulse times of delay. The arithmetic registers used in the system are similar except for the addition of several more S-type noncomplementers to provide additional delay.

6-67. TRANSISTOR AMPLIFIER PACKAGE (TAP). Frequently it is necessary for a magnetic amplifier, either complementer or noncomplementer, to drive a relay or a transistor stage instead of another magnetic amplifier. In such applications the magnetic amplifier output must contain only information signals and no blocking pulses.

Since the blocking pulses must be removed from the output windings, diode CR4 of the standard magnetic amplifier circuit is removed. To replace the function of the blocking pulses on the core, the diode equivalent to CR5 is returned to +3 volts instead of ground potential. This insures that sneak outputs do not develop in the magnetic amplifier. The remainder of the circuitry on the special driver package is identical with the circuitry of the standard single-power magnetic amplifier.

The special package is limited only in that it may not be used to drive another magnetic amplifier.

6-68. STORAGE UNIT

6-69. GENERAL DESCRIPTION

The main storage unit stores both the data and the instructions which are processed by the system in the course of problem solution. The principal parts of the storage unit are a rotating drum with its associated read-write heads, recording and playback amplifiers, and head-selection circuitry (figure 6-36).

Information is stored on the surface of the drum in the form of small magnetized areas, which are generated (written) and sensed (read) by magnetic recording heads located within the drum housing. The five bits (four information bits and a check bit) which make up a digit are recorded (or read) simultaneously on five tracks around the circumference of the drum.

The matrix-selector package and the head-switch driver package comprise the necessary equipment to select a group of five magnetic heads for either reading or writing on a storage band in magnetic drum storage. These packages are used in conjunction with the diodes in the diode cluster which facilitate the head-switching operation.

All write signals developed across the heads are applied through the write transformer. The transformer secondary is centertapped to provide push-pull operation for the modified return-to-zero phase-modulation recording system. The input to the write transformer (WXPS) is supplied by four magnetic amplifiers, one for each phase for both zeros and ones. As shown in figure 3-4, two complementers and two noncomplementers are necessary to drive one WXPS package. The write-amplifier complementer-driver (WACD) package contains two noncomplementers but only one complementer. As a result a CC3 package (three complementers) is used in conjunction with every three WACD packages to complete the driver set. In figure 3-4 the WACD package consists of noncomplementers 3 and 4, and complementer 5; complementer 2 is taken from a CC3 package.

During the read operation, signal voltages induced in the head windings by the magnetized areas on the drum surface are applied to the read amplifier. In the read-amplifier (RAPS) package the sensed signals are amplified and phase-corrected before being applied to the read flip-flop. The read flip-flop (RFFS) package accepts the signal current from the read amplifier, gates it with a fixed-time probe pulse, and sets a transistor flip-flop or not, depending upon the phase of the input signal with respect to the gating pulse. The flip-flop drives a buffer stage which in turn drives an output stage of sufficient power to set a single-power magnetic amplifier.

By definition, the output of the detector is such that no signal is developed to represent a 1 bit, and a signal output represents a 0 bit. No special precautions are necessary to maintain stability other than requiring the output stage to produce no output signal for a 1 bit and to supply sufficient driving signal to a magnetic amplifier for a 0 bit.

The probe and clear circuits are both clock-driven units and each produces an output spike on every positive alternation of the clock driving signal. The probe pulses are gated with information signals from the RAPS package in the input gate of the RFFS package. If the information signals are of the correct phase with respect to the probe pulses, they set the flip-flop in the RFFS package. The clear pulses are applied directly to the flip-flop to insure that the flip-flop is cleared by the end of B-phase.

As shown in figure 6-40, the read and write circuits are connected to the WD lines by the coupling diodes CR5, CR6 and CR3, CR4, respectively. The write-pedestal package (WPPS) is a protective device to prevent the write signals from being impressed across the input transformer of the read amplifier (RAPS). The amplitude of the write signals is sufficient to overdrive and block the transistors in the read-amplifier circuit. The function of the write-pedestal circuit is to disconnect the read amplifier from the WD lines during write operations and, therefore, to prevent blocking the read circuits. If the read circuits became blocked, a recovery time would be necessary before they could be used again.

6-70. WRITE CIRCUITRY

6-71. GENERAL DESCRIPTION. Recording information on the drum requires pulsing the head (figure 6-37) so that it can magnetize small areas of the drum surface. The relative polarity of the small magnetized areas determines whether the recorded bit represents a zero or a one. Recording current

passes through the head first in one direction and then in the other; the order of these directions depends upon whether it is desired to record a 0 bit or a 1 bit.

To write a 0 bit with the circuit arrangement shown in figure 6-37, a voltage is induced in the secondary of the write transformer such that point A goes negative and point B goes positive with respect to the grounded centertap. Current flows from ground through the centertap of the write transformer, through CR1, half of the head winding, and back to ground through the head-winding centertap. During the next alternation, point B goes negative and point A goes positive with respect to ground. During this alternation current flows through the other half of the head winding.

To record a 1 bit on the drum, the order of the magnetizing currents is reversed. Point B is driven negative on the first alternation, and point A goes negative on the second alternation. Changing the order of the magnetizing currents changes the polarity of the bits recorded on the drum surface. In the example, the relative polarities of the 0 bits and 1 bits recorded on the drum are as shown in figure 6-37. The shaded area represents a north pole. These bits are recorded on the drum at a density of 160 bits per inch.

6-72. DIODE CLUSTER. The diode cluster shown above the drum housing (figure 6-36) contains the head diodes which were shown as CR1 and CR2 in figure 6-37. The purpose of these diodes is to facilitate the head-switching operation.

When none of the matrix-selector packages (MSP) (figure 6-40) are being driven, diodes CR1 and CR2, and the equivalent diodes in the other heads, are reverse-biased through the head-winding centertap and the -29-volt supply. Under this condition no current flows through any of the heads.

To write with head number 1, the MSP connected to that head returns the centertap of head winding number 1 to ground potential. With the reverse bias on CR1 and CR2 removed and a writing signal developed across the write transformer, current flows through head number 1 first in one direction and then in the other. The diodes of each of the remaining heads isolate them from this circuit.

6-73. WRITE TRANSFORMER PACKAGE (WXPS). The write transformer (figure 6-38) employs a centertapped secondary to provide push-pull operation for the modified return-to-zero phase-modulation recording system. The primary is not centertapped because it is connected across the outputs of the driving magnetic amplifiers. The clamping diodes in the output circuit of the magnetic amplifiers would present a short circuit across that half

of the primary which was negative with respect to the centertap. Since no centertap is used, the primary current is absorbed by resistive sinks at each end of the winding. These sink circuits must use a d-c supply because the drive phase at each end of the primary changes for zeros and ones.

The sink circuits also act as current-clamping circuits which limit the maximum writing current in the secondary. The secondary voltage is set to assure the establishment of the head current within one-half pulse time and yet clamp the zero-one transition currents at the same level as the non-transition currents. The idealized voltage and current waveforms in figure 6-39 clarify the operation of the limiter. Resistor R3 in the centertap of the secondary is used solely for monitoring purposes. The waveform for the current through or the voltage across this resistor is shown in figure 6-39.

Because of the reactive components in the write circuitry, the primary current lags the driving voltages. The primary current also accounts for the voltage pips at both inputs. If el is positive, current flows from the -29-volt supply through R2, the primary winding, and the input diode to the positive source potential. When the current through R2 exceeds the sink current, the bottom of R2 (input 2) goes more positive than +3 volts. This increase in voltage is shown as a voltage pip on the e2 waveform. When the primary current increases to maximum in the other direction, a similar pip develops at input 1. The difference between the input voltage and the pip voltage is the actual primary driving voltage during that interval of time.

The current through the centertap of the secondary is a unidirectional pulsating current which approaches the waveform shown. The writing current is approximately 110 ma for a 300-ma output from the driving magnetic amplifiers.

6-74. WRITE-AMPLIFIER COMPLEMENTER-DRIVER PACKAGE (WACD). Four double-powered magnetic amplifiers are required to drive one WXPS package, one for each phase for both zeros and ones. These magnetic amplifiers are slightly different from the standard magnetic amplifiers in that they do not use blocking pulses and their outputs are clamped at +3 volts instead of ground potential.

Since the outputs of the driving magnetic amplifiers are all clamped at +3 volts, the output pulses are all clipped below the 3-volt level. To compensate for this clipped output a transformer is included on the WACD package to boost the power-pulse voltage by about 15 per cent. The power pulses to be used on the CC3 package which completes the driver set are also taken from the transformer on the WACD package, since the CC3 package outputs are also clamped at +3 volts.

6-75. READ CIRCUITRY

6-76. GENERAL DESCRIPTION. At all times that a magnetic recording head in the storage system is not actively recording new information on the drum, whether or not it has been selected, small signal voltages are induced in its windings from previously recorded information on that track. These voltages are induced in the head windings whenever the magnetic field about a previously recorded bit links the coils of the head windings. This condition is met whenever there is a change in the relative position of the head winding and the recorded bit under the head.

While the sensing of recorded information by the heads is continuous, the heads must be coupled to external circuitry where the signals are shaped, timed, and amplified to a level sufficient to drive a magnetic amplifier before the sensed data can be utilized logically.

Figure 6-40 shows the read-write circuit interconnections in which the heads are the common elements between the read and write circuits. Twenty such heads are connected to a headbar but for simplicity only three have been shown here. The matrix-selector and write-pedestal packages are both shown as switches to aid in the understanding of their functions rather than their methods of actuation.

6-77. WRITE PEDESTAL PACKAGE (WPPS). The write-pedestal circuit disconnects the read amplifier from the WD lines during write operations to prevent the write signals from blocking the read circuits.

As shown in figure 6-41, the centertap on the primary of the read amplifier input transformer is normally held at -1.5 volts. This voltage is maintained through a circuit consisting of diodes CR7 and CR8, and resistor R5. During the write operation the write-pedestal circuit permits a +20-volt signal to be applied to the centertap of the read-amplifier input transformer. This is several volts higher than any write signals on the WD lines and insures that the coupling diodes CR5 and CR6 are reverse-biased during the write operation. Keeping CR5 and CR6 cut off prevents the write signals from entering the read-amplifier circuit.

Since five bits are being either written or read simultaneously, one write-pedestal package drives five read amplifiers simultaneously. A transistor amplifier package (TAP) provides the driving signals for the write-pedestal circuit and keeps the circuit free of blocking pulses.

The input signal to the write-pedestal circuit consists of a train of 16 pulses, one per pulse time. The pulses begin 4 pulse times before a write operation is to take place and continue until the writing is completed. Therefore, the write-pedestal voltage on the transformer centertap must rise within 4 pulse times. One word time is allowed for the write-pedestal voltage to fall, because it is not possible to read immediately after writing.

The write-pedestal circuit (figure 6-41) consists of a d-c restorer (CR4) followed by a choke-input T-type filter (L1, L2, C2). The output of the filter drives the base of a PNP transistor stage. The transistor is operated in the common-emitter configuration with the collector connected to the centertaps of the read-amplifier input transformers and the emitter returned to +20 volts. The stage is operated class C, and there is an inverse bias of slightly more than 1 volt between the base and the emitter of the transistor.

The d-c restorer diode CR4 sets the d-c level of the input signals and provides signal inversion. The output of the TAP is capacitively coupled to CR4, whose cathode is returned to +20 volts. With no output from the TAP, CR4 is held on and a small current flows from +20 volts through CR4, L1, L2, R2, and R3 to +35 volts. The TAP output is clamped to +3 volts by CR1 and CR3. The coupling capacitor C1, therefore, has 20 volts minus 3 volts, or 17 volts, across its terminals. When an output pulse appears, C1 discharges through CR4 to 20 minus E_{max}, where E_{max} is the peak output voltage of the TAP. When the output of the TAP returns to +3 volts, CR4 disconnects, and a negative pulse of amplitude E_{max} minus 3 volts is developed across the input of the filter. Applying a negative pulse to the filter causes the base of the transistor to go negative with respect to the emitter. This voltage provides a low-impedance path between the collector and emitter of the transistor and effectively returns the centertap of the read-amplifier input transformer to +20 volts through the transistor.

The filter section changes the block of 16 pulses into a single pulse 16 pulse times long. This insures that the read amplifier remains isolated during the entire writing operation.

A low-impedance source is required to drive the write-pedestal circuit. When the output pulse begins to fall, the output impedance of the TAP is high. To lower the output impedance of the TAP a 330-ohm pulldown resistor (R1) is connected to the clock through CR2.

6-78. READ-AMPLIFIER PACKAGE (RAPS). The read-amplifier circuit consists of two class-A, common-base, transformer-coupled transistor stages plus input and output transformers. Also

included in the RAPS circuitry are limiting, differentiating, and phase-correcting networks which enable the read amplifier to accept a signal from the head, amplify it, and transmit it to the read flip-flop in the proper phase.

The read-amplifier input transformer (T1) is used to change the input from balanced to single-ended. As shown in figure 6-40, the input transformer is coupled to the selected head by means of a d-c latching current which flows from the -29-volt supply through resistor R5 to the centertap of T1 primary, where it divides between the halves of the primary winding, through both halves of the head winding to the driven matrix selector (MSP).

While the currents through both halves of the input winding are approximately equal, it is only their sum which is a constant. Any unbalance in the head diodes or the coupling diodes CR5 and CR6 gives rise to an unbalanced current through the input winding of T1. When a head is selected for reading, an unbalanced current causes a d-c step voltage across the primary of T1.

In order not to carry this initial d-c unbalance into the amplifier and thus complicate the probing and gating arrangement, an RL differentiating network follows the input transformer (figure 6-42). Sufficient time is available between head selection and the arrival of the first significant bit of information to eliminate the effects of this step voltage by differentiation.

Coil L1 makes up the inductive component of the RL differentiating network which follows the input transformer T1. Due to the windings on the heads, the heads have an RL equivalent circuit. To make the heads appear as a pure resistance before differentiating, an RC compensator circuit (R1-C1) is placed in series with the secondary of T1. The differentiating circuit has a time constant of 0.4 microsecond, and in about 1.5 microseconds any step voltage developed across L1 decays. There is ample time in which to eliminate the step voltage between the time a head is selected and the arrival of the first information bits (sign digit).

The amplitude response produced by the differentiation circuit is accompanied by an unfavorable phase response which shifts the signal components enough to severely limit the allowable timing variations in the probe gate. To correct this phase distortion an all-pass lattice filter (L2, L3, C4 and C5) is inserted after the differentiator. The π-type filter (L4, L5, and C2) also provides a fixed delay at the signal

frequencies and reduces high-frequency noise. The transmission delay of the differentiator and corrector networks is calculated as one-half pulse time. To allow for this delay all writing on the drum is done one-half pulse time earlier than would otherwise be necessary.

The two common-base, transformer-coupled amplifier stages offer the advantage of great stability of current gain. The current gain is actually achieved in the step-down transformers, and any reasonable change of transistor current gain, alpha (normally $\alpha > 0.98$) has a negligible effect on the gain.

Diodes CR1 and CR2 and resistor R4 form a limiting network. Let R_e be the input impedance of transistor Q2. Let the bottom of the T2 primary winding be at a-c ground through C8. Diodes CR1 and CR2 are also returned to a-c ground through C7 and C8.

Let N:1 be the turns ratio of T2 and assume that a current (i) is flowing through the collector circuit of Q1. Neglecting losses, a larger current (Ni) flows in the emitter circuit of Q2, and a current (α Ni) flows in the collector circuit of Q2. The voltage across the secondary of T2 is

$$e_{sec.} = Ni\ (R4 + R_e) \qquad (1)$$

To develop this voltage the following voltage must exist across the primary of T2:

$$e_{pri} = N[Ni\ (R4 + R_e)] = N^2 i\ (R4 + R_e) \qquad (2)$$

Equation (2) implies that the voltage excursions across the T2 primary winding are directly proportional to the value of R4. Diodes CR1 and CR2 restrict the upper limits of the primary-winding voltage excursions. Should the voltage reach a predetermined value either CR1 or CR2 will turn on (depending upon signal polarity) and act as an a-c shunt across the primary winding through C7. Bypassing some of the primary current through the diodes will limit the primary voltage.

Diodes CR9 and CR10 across the primary of T1 are protector diodes. They insure that no writing signals are transmitted to the read amplifier circuit. These diodes operate only if for some reason the write pedestal voltage (+20 volts) is not applied to the centertap of the T1 primary winding during a writing operation. The amplitude of any normal read signal is insufficient to turn on CR9 or CR10.

A head normally develops a read signal of about 250 microamperes in the matched inputs of the read amplifier. Neglecting all losses, a current gain of 3 is realized in T1,

a gain of 5 in T2, and a gain of 2 in T3. The unit, therefore, has a total current gain of 30. This produces an output current of 7.5 milliamperes. When the alpha and compensator losses are included, a more realistic output current of about 4 milliamperes is realized from a read-amplifier package.

6-79. READ FLIP-FLOP PACKAGE (RFFS). By definition, the output of the flip-flop detector is such that no signal is developed to represent a 1-bit output, and a signal output represents a 0 bit. No special precautions are necessary to maintain stability other than requiring Q6 (figure 6-43) to produce no output signal for a 1 bit and to apply sufficient driving signal to a magnetic amplifier for a 0 bit.

When the flip-flop circuit is not being driven, both the emitter and base of Q1 are at +19 volts, so that there is no forward bias on this stage. The collector of Q1 and the emitter of Q2 are at +18 volts; however, the base of Q2 is held near +20 volts by the normal level of the probing signal. These voltages hold Q2 reverse-biased. Since the emitter of Q3 is at +19 volts and the base is returned to +16 volts through R6 and R7, current flows from the +16 volts supply through R7, R6, and Q3 to the +19 volts supply. With Q3 forward-biased, a current flows from the +16-volt supply through R4, and Q3 to the +19-volt supply. This current holds the collector of Q3 and the base of Q4 at approximately +19 volts. Since the emitter of Q4 is held at +19 volts, Q4 is normally held off. The base current of Q3 flowing through R7 holds the base of Q5 below +19 volts while the emitter of Q5 is connected directly to the +19-volt supply. Transistor Q5 conducts heavily and its collector voltage approaches +19 volts. This voltage minus the small drop across R9 is applied to the base of Q6 while the emitter of Q6 is held at +16 volts. This reverse bias is sufficient to hold Q6 cut off. In summary, during the normal, non-driven state (one output), Q3 and Q5 are held on and all other transistors in the read flip-flop circuit are biased off.

If a signal from the RAPS is now impressed across the secondary of T3 such that the base of Q1 is driven negative with respect to the emitter, a current flows from the +18-volt supply through R2 and Q1 to the +19-volt supply. This current raises the collector of Q1 and the emitter of Q2 to approximately +19 volts. If at this time a probing pulse arrives which lowers the base of Q2 below the emitter voltage, Q2 turns on and a current flows from the +16-volt supply through R7, R6, Q2, and Q1 to the +19-volt supply. This current raises the potential on the base of Q3 to +19 volts and turns off Q3. As Q3 turns off, the collector of Q3 and the base of Q4 approach +16 volts and Q4 turns on. Current flows from the +16-volt supply through R7 and Q4 to the +19-volt supply, and puts the collector of Q4 and the base of Q5 at about +19 volts. This

voltage turns off Q5, and the collector of Q5 and the base of Q6 fall below +16 volts. Transistor Q6 then conducts heavily, developing an output signal which approaches +16 volts.

If Q6 reached saturation current, the collector and emitter of Q6 would be at essentially the same potential (+16 volts). To prevent Q6 from drawing saturation current, CR4 turns on before saturation current is reached and holds the collector of Q6 below +16 volts. Diode CR5 prevents the collector of Q6 from going below ground potential during periods when Q6 is cut off.

Transistor Q2 remains on only for the duration of the probe pulse, 0.1 microsecond. Transistor Q3 is held off, however, by feedback from Q4. When Q4 turns on, its collector approaches +19 volts, and this voltage is applied to the base of Q3 through R6. Transistor Q3 is held off while Q4 is on, and Q4 stays on until the +20-volt clear pulse is applied to its base through R5 and CR3. The clear pulse (0.1 to 0.2 microsecond in duration) is sufficient to turn off Q4, at which time the collector of Q4 drops to nearly +16 volts. This voltage, applied to the bases of Q3 and Q5, causes Q3 and Q5 to turn on as Q4 turns off.

When an input signal is applied to Q1 such that the base is driven negative with respect to the emitter, Q1 turns on and places a load on T3. If the input signal polarity is reversed, Q1 remains off, leaving T3 unloaded. To balance the load on T3, CR1 and R1 are placed across the secondary of T3. During the periods when Q1 is off, CR1 conducts, and vice versa. This arrangement keeps the load on T3 relatively constant.

Capacitors C1 and C2 are both bypass capacitors. They prevent undesirable a-c coupling among the various stages.

6-80. PROBE AND CLEAR PACKAGE (PBC). The probe and clear circuits (figure 6-44) are both clock-driven units. Each produces an output spike on every positive alternation of the clock input signal.

The probe circuit (figure 6-44a) continuously develops negative-going pulses of 0.1-microsecond duration by the flipping action of a small core of square-loop magnetic tape with current from the sine-wave clock. The clock input is applied through an RC phase shifter (R1-C1) so that the probe timing can be adjusted. Normally a current that flows from the -29-volt supply through R3 and CR2 to ground clamps terminal 1 of the input winding to ground potential. A d-c reset current that flows from the -29-volt supply through R2, the input winding, and CR2 to ground insures that the core is normally reset toward $-B_S$. (See figure 6-28f.) Upon application of a

positive clock pulse, CR1 turns on, and a current (from the -29-volt supply through R3, the input winding, and CR1 to the positive clock) fast-flips the core toward $+B_s$. Upon removal of the positive input the core is slowly reset by the d-c reset circuit.

In the output circuit a current normally flows from the +20-volt supply through CR3 and R4 to the +45-volt supply. The output terminal, then, is normally clamped at +20 volts through CR3. When the core is fast-flipped toward $+B_s$, transformer action induces a voltage in the output winding which drives terminal 9 negative with respect to terminal 7. This negative-going pulse is applied to the output terminal through C2 and causes the output voltage to go well below +20 volts for the duration of the pulse (0.1 microsecond).

The clear circuit (figure 6-44b), which continuously develops positive-going pulses of 0.2-microsecond duration, operates like the probe circuit. The clock input is applied through an RL phase shifter (R5-L1). A current from the -29-volt supply through R7 and CR5 to ground clamps terminal 1 of the input winding to ground potential. A d-c reset current from the -29-volt supply through R6, the input winding, and CR5 to ground resets the core toward $-B_s$. Application of a positive clock input signal turns on CR4, and a current (from the -29-volt supply through R7, the input winding, and CR4 to the positive clock) fast-flips the core toward $+B_s$. The d-c reset current slowly resets the core after the removal of the positive input signal.

In the output circuit a current flows from ground through R8, where it divides between CR6 and CR7 to the +18-volt supply. The current through CR6 and the output winding aids in resetting the core toward $-B_s$. The output terminal is normally clamped to +18 volts through CR7. When the positive input signal causes the core to fast-flip toward $+B_s$, transformer action induces a voltage in the output winding which drives terminal 7 positive with respect to terminal 9. The positive-going signal on terminal 7 is applied to the output terminal through CR6 and causes the output voltage to go well above +18 volts for the duration of the pulse (0.2 microsecond).

The clear pulses are generated about 0.1 microsecond before the end of B-phase in order to bring the RFFS output down by the end of B-phase. Figure 6-45 shows the read-circuit waveforms.

6-81. HEAD SELECTION

6-82. MATRIX-SELECTOR PACKAGE (MSP). Essentially the matrix selector (figure 6-46) is a transistor with its collector connected to the centertaps of five heads in a storage band. The collector also returns to the -29-volt supply through resistor R5; with the transistor in the normal nonconducting state, all head windings are at -29 volts. This potential keeps the diodes from the information lines to the heads (CR1 and CR2 in figure 6-40) reverse-biased; therefore, the heads are disconnected from the information (read or write) lines.

When the transistor is driven to the conducting state, the collector voltage rises nearly to ground potential through the emitter. The inverse bias on CR1 and CR2 is now removed and the heads are now connected to the information lines for reading or writing.

In the absence of an input signal (figure 6-46), current flows from the +3-volt supply through CR1, R1, and R2 to the +35-volt supply. The transistor base is held at +3 volts through CR1, and the transistor remains cut off.

When a negative input signal is applied, the base goes negative with respect to the emitter, and the transistor turns on. The collector and head-winding centertap then approach the emitter potential (ground).

The negative input signal applied to the MSP comes from a pair of magnetic amplifiers on the MSI package and is, therefore, a train of half sine waves. Capacitor C1 acts as a filter to smooth out the input signal and reduce ripple in the collector circuit. Resistor R3 limits the input current to the transistor and also aids in reducing ripple.

Resistor R4 and capacitor C2 serve to attenuate ripple and also provide a low impedance to the initial pulse of write current through the heads. When the transistor is first turned on, all of the collector current flows through resistor R5. In about 2 microseconds this current reaches a value of approximately 120 milliamperes. Three microseconds later, if the heads are to be used for writing, the write current through the collector rises toward 500 milliamperes. During this rise time the collector drops below ground potential until the collector current increases enough to bottom the transistor. This drop may result in attenuating the first few writing pulses. The combination of R4 and C2 reduces this attenuation by limiting the voltage drop at the collector due to this cause to one volt.

6-83. HEAD-SWITCH DRIVER PACKAGE (MSIS). The head switch driver package (figure 6-47) contains the necessary magnetic amplifiers to drive the head switch (MSP) into conduction when an input (selection signal) is received. Three noncomplementers are used in order to give outputs of both phases to approximate a d-c input signal to the transistor switch. Each head-switch driver package drives one transistor head switch. Two input terminals are provided on the driver package so that selection signals may come from two separate sources without any external diode buffers. Since the cores are noncomplementing, output signals are developed only upon the application of an input signal.

When a group of heads is to be selected for reading or writing, a selection signal arrives at the input of the MSI several cycles before the appearance of the selected word. The first input signal (B phase) sets noncomplementers NC1 and NC3 to the low-impedance state. On the next half cycle, the A-phase output from NC1 sets NC2 to the low-impedance state, and the A-phase output from NC3 provides an input signal to the head switch transistor. On the next half cycle NC2 delivers a B-phase input to the transistor. Thus a B-phase input signal is converted to output signals occurring during both halves of the power pulse to approximate a d-c drive for the head-switch transistor.

The output circuit of NC2 and NC3 is modified to develop a negative rather than a standard positive output waveform. The polarity of the output windings and output diodes (CR12, CR13) is reversed, so that a negative power pulse of the proper phase is used rather than a positive power pulse.

Blocking pulses are eliminated from the output circuits of NC2 and NC3 because they tend to turn on the transistor. The purpose of blocking pulses in a standard noncomplementer is to insure that the output diode remains reverse-biased while the core is being reset to the high-impedance state. For the same purpose, a d-c bias voltage is used here to ensure that the blocking half cycle of the power pulse is of larger amplitude than the power half cycle.

The output circuits of NC2 and NC3 are connected to the base of the switch transistor, which is held at +3 volts by CR1 in conjunction with R1 and R2 (figure 6-46), and which also serves as output clamp and sneak suppressor for the magnetic amplifiers.

If a power pulse with an 18-volt peak centered around ground is used to drive NC2 and NC3, the negative power pulse has a peak of -21 volts and the blocking half cycle has a peak of +15 volts. The blocking half cycle is of smaller amplitude than the power half cycle.

6-84. POWER CONTROL AND POWER SUPPLIES

6-85. POWER TURN-ON PROCEDURE

Power is turned on by pushing the turn-on bar (marked DC READY) which actuates the DRUM ON, AC ON, and DC ON switches. The power-control circuits are shown as a block diagram in figure 6-48. The power turn-on operation takes place in three steps.

When the turn-on bar is first pressed the blowers in all units turn on. The turn-on bar should be held down a few seconds until the blowers reach normal operating speed. At this time the storage-drum airflow switches close, the DRUM ON light is illuminated, and the motor-generator set which drives the drum motor is energized (figure 6-48). To provide sufficient time for the drum to reach its normal operating speed a 12-minute delay is actuated also.

After the DRUM ON light is illuminated the turn-on bar is pressed a second time. Pressing the AC ON switch makes power available to the drive motors in all units. In addition the filament transformers are energized and the AC ON light is illuminated. A delay of 1 1/2 minutes is actuated to provide sufficient warm-up time for the filaments before dc is applied to the tubes. Twelve minutes after the first time the turn-on bar was pressed, signals are available from both the 12-minute and the 1-1/2-minute delay. Through a series of relay contacts which function as a gate, the DC READY light in the turn-on bar is illuminated.

After the DC READY light is illuminated the turn-on bar is pressed for the third time. Through the DC ON switch ac is then applied to the d-c power supplies and the DC ON light is illuminated to indicate that dc has been made available to all units.

Although ac is made available to all units the second time the turn-on bar is pressed, the drive motors in the reader, printer, or punch must be turned on manually if the individual unit is to be put into operation.

6-86. AC DISTRIBUTION

The distribution of ac to all units of the system, except the marginal-check fuse-alarm circuits which receive AC through the main-line switch, is initiated during the power turn-on operation. Figure 6-49 shows the a-c distribution circuits.

When the turn-on bar is first pressed the relay 4 contacts switch and energize all of the blowers. With the exception of the processor blowers, all of the blowers are connected across a 120-volt source and ACN. The 120-volt source is one side of the 240-volt, single-phase, 3-wire line. The processor blowers receive 240 volts, since they are connected across the two outside lines.

The relay 6 contacts also close the first time the turn-on bar is pressed and energize the motor of the motor-generator set. The motor is a 60-cycle unit but the generator produces a 300-cycle output to drive the drum motor. This higher frequency is required because the drum motor speed is approximately 18,000 rpm. Five seconds after the motor-generator set is energized the relay 34 contacts close, placing the drum-motor load on the generator. Five seconds is ample time for the generator output voltage to reach normal operating level. With the relay contacts in the position shown (figure 6-49), the drum-motor current flows through the starting fuses. In 12 minutes the drum motor attains normal operating speed, and the relay 8 contacts switch. The drum-motor current then flows through the smaller run fuses.

The second time the turn-on bar is pressed, the relay 11 contacts switch and energize the clock filament transformer, the RPU relay supply, and the marginal-check cabinet. Although 120 volts is available to the motors in the card reader and read punch, the motors must be started manually if the units are to be put into operation. The HSP filament transformers receive 240 volts, since they are connected across both sides of the line through relay 11.

The third time the turn-on bar is pressed, the relay 12 contacts switch and supply ac to the power supplies. A relay in the primary winding of the printer-actuator supply delays ac to the printer-actuator supply. The delay provides adequate time to establish the bias voltages before the development of the high d-c potential.

6-87. POWER-CONTROL CIRCUITS

In conjunction with the schematic diagram of the power-control circuits, figure 6-50, the following description explains in detail how the blowers, drum, ac, and dc are turned on. When the turn-on bar is pressed the DRUM ON, AC ON, and DC ON switches are all actuated simultaneously.

When the turn-on bar is first pressed, relay 4 is energized through the DRUM ON switch. The K4-1, 2, and 3 contacts energize the blower motors. A circuit is also completed through thermal-delay relay 3, which has a dropout time of 2 minutes. Relay 4 and the blower motors remain energized through the K3-1 contacts for 2 minutes after the system is turned off.

When the blowers reach normal operating speed, all the airflow switches operate. Relay 36 is then energized through the DRUM ON and storage-drum airflow switches. Relay 37 is also energized through the DRUM ON switch and the series of airflow and air-temperature switches. The K37-1 contacts require 8 seconds to switch. When the K36-1 contacts close, relays 6 and 34, the total time indicator, and the DRUM ON light are energized through the normally closed DRUM OFF switch, K36-1, K15-1 normally closed, and K33-3 normally closed.

The motor-generator set is energized through the K6-1 contacts, and in 5 seconds the drum motor is energized when the K34-1 contacts close. The K6-2 contacts hold relay 4 energized and the K6-3 contacts short the normally open DRUM ON switch.

Relay 7 is energized when the DRUM ON switch is first closed but the K7-1 contacts do not switch for 12 minutes, time for the drum to attain normal operating speed.

Relays 36 and 37 have 8- and 12-second dropouts respectively. These delayed dropouts prevent the system from going off the line due to a momentary interruption in the air flow. If the air flow is interrupted or if the temperature rises above a predetermined point, one or more of the airflow or air-temperature switches operates, illuminating the appropriate indicator lamp and turning off a-c power or drum power.

Eight seconds after the turn-on bar is first pressed, the K37-1 contacts close and the turn-on bar is pressed a second time. Relay 11 and the AC ON light are energized through the AC ON and AC OFF switches, K16-1 normally closed, and K37-1. The K11-1 and 2 contacts energize the filament transformers, and the K11-3 contacts short the AC ON switch. A circuit is also completed through the AC ON switch, K10-2 normally closed, and relay 9, but the relay 9 contacts do not switch for 1-1/2 minutes. This delay provides time for the filaments to warm up before the application of dc.

When the K9-1 contacts switch, a circuit is completed through K11-3, the AC OFF switch, K9-1, and relay 10. The K10-2 contacts drop out relay 9 and hold relay 10. Twelve minutes after the turn-on bar is first pressed, the K7-1 contacts switch and energize relay 8. The K8-2 and 3 contacts switch the drum motor from the start to the run fuses. A circuit is also completed through K7-1, the normally closed contacts of the three overcurrent relays, the normally closed contact of the processor interlock switch, K10-1, R22, and the three DC READY lights in series. Three lamps are used here to provide ample illumination for the turn-on bar.

When the DC READY light is illuminated the turn-on bar is pressed for the third time. Relay 12 and the total time indicator are energized through K7-1 normally open, the overcurrent relays, the processor interlock switch, K10-1 normally open, the DC ON normally open contact, the DC OFF switch, K17-1 normally closed, and K18-1 normally closed. The DC ON lamp is illuminated through R23. The K12-1, 2, 3, and 4 contacts energize the power supplies. The K12-5 and K32-1 contacts in series, short the DC ON switch normally open. Unless the clock output is sufficient to hold relay 32 energized through CR4 and CR5, the K32-1 contacts open and turn off dc. During clock alignment this circuit can be shorted out by the CLOCK ALARM BYPASS switch.

A positive potential must be developed to check the -dc fuse-fault circuits, and a negative potential to check the +dc fuse-fault circuits. When ac is applied to the half-wave rectifiers CR2 and CR3 through K32-1, K12-3, and K13-1, negative and positive potentials are developed across C5 and C6 respectively.

6-88. DRUM ALARM CIRCUITS

6-89. POWER SUPPLY. The drum alarm circuits use d-c microammeters, with holding coils, as indicating devices. A half-wave rectifier circuit is used to supply the dc the holding coils require. Refer to figure 6-50.

Diode CR1 makes up the rectifying unit and C4 is the filter capacitor across which dc is developed. Bleeder resistor R16 discharges C4 when the system is turned off. Power is normally supplied to the unit through K33-1 normally closed and K6-2. If power is turned off manually the K6-2 contacts open and deenergize the unit. If power is turned off automatically because of a drum alarm, power is supplied to the unit through the K33-1 normally open contacts and the trouble indication is retained until it is cleared manually.

6-90. HEAD-SPACING DETECTOR. The purpose of the continuously operating head-spacing detector circuit is to detect and indicate any change in the normal spacing between the heads and the drum. If the spacing deviates appreciably, the system turns off.

The four heads, connected in parallel, are positioned over a permanently recorded timing band. Assuming the drum speed is constant, the amplitude of the induced-voltage sine wave in the head windings is a function of the degree of coupling between the heads and the magnetized areas (bits) on the surface of the drum. As the head-to-drum spacing decreases the coupling becomes tighter and the amplitude of the induced voltage increases. If the spacing increases the voltage decreases.

The induced voltage is transformer-coupled to a half-wave rectifier circuit by T1. The PNP transistor, Q1, is connected collector-to-base shorted to act as a conventional diode. Then dc develops across C2, the output of the filter circuit. The meter is connected across C2 and gives an indication when the drum is rotating even though no other power is on.

Assume that the head-to-drum spacing increases above the desirable limit. The voltage induced in the heads and the voltage across C2 decreases, causing the indicator to move counterclockwise. The indicator closes the LO contacts and completes a circuit from the negative side of C4 through the normally closed TEST AND CLEAR switch, the hold coil, the LO contacts, K8-1 normally open, relay 33, and K14 to the positive side of C4. The hold coil keeps the LO contacts closed until the TEST AND CLEAR switch is opened manually.

The DRUM lamp is illuminated through K33-1 and 2. The K33-1 normally open contacts bypass all control switches and maintain dc across C4 even though computer power turns off. The K33-4 contacts bypass the K8-1 contacts and hold relay 33 energized even though computer power is off. When the computer is first turned on, the K8-1 contacts hold the circuit inoperative until the drum attains normal operating speed.

Instead of a conventional diode, transistor Q1 is used as a rectifier because it has a more favorable characteristic. The filter circuit consisting of C1, C2, L1, and L2 not only provides a steady d-c output but also absorbs any inductive surges in the meter movement when the hold coil is deenergized, thus preventing any unwanted erasures at the heads.

6-91. STATOR TEMPERATURE DETECTOR. The purpose of this circuit is to measure and indicate the temperature of the drum-motor stator windings and turn off the power if the temperature approaches an unsafe limit.

The detector unit is a thermocouple whose output varies as a function of the stator temperature. As the temperature increases the output increases and the indicator moves clockwise. When a predetermined temperature is reached the indicator closes the contacts and completes a circuit from the negative side of C4 through the normally closed TEST AND CLEAR switch, the hold coil, meter contacts, K8-1, relay 33, and R14 to the positive side of C4. Relay 33 initiates a power turn off and a DRUM indication, while the hold coil keeps the meter contacts closed and relay 33 energized until the TEST AND CLEAR switch is opened manually.

6-92. BEARING TEMPERATURE RISE DETECTORS. Two temperature-rise detector circuits, one for the drum bearings and the other for the drum motor bearings, function in the same manner. Since expansion is the physical consideration, the difference between the bearing and ambient temperatures is measured and indicated. When the temperature difference reaches a predetermined limit power is turned off.

Two thermocouples are connected series opposing in each circuit. When the drum is inoperative the bearing and ambient temperatures are equal, and the indicator reads zero. When the drum is in operation the bearing temperature exceeds the ambient temperature, and the indicator moves clockwise. The amount of indicator movement is a function of the temperature difference.

When the temperature difference approaches an unsafe limit the indicator closes the meter contacts and completes a circuit from the negative side of C4 through the normally closed TEST AND CLEAR switch, the hold coil, the meter contacts, relay 33, and R14 to the positive side of C4. Relay 33 initiates a power turn off and a DRUM indication, while the hold coil keeps the meter contacts closed and relay 33 energized until the TEST AND CLEAR switch is opened manually.

6-93. POWER TURN-OFF PROCEDURE

The recommended procedure for removing all power is as follows:

(1) Press the DC OFF switch. Relays 12 and 30 (figure 6-50) drop out, disabling the power supplies and the write circuits.

(2) Press the AC OFF switch. Relay 11 drops out, deenergizing the filament transformers and the motors of the reader and punch unit.

(3) Press the DRUM OFF switch. Relays 6 and 8 drop out, deenergizing the drum-motor generator set, the drum-alarm circuits, and all blower motors.

To disable only the dc, as during maintenance periods, it is only necessary to press the DC OFF switch. To disable both AC and DC, both the DC OFF switch and the AC OFF switch should be pressed. Although it is possible to disable both ac and dc by pressing only the AC OFF switch, or to disable the entire system by pressing only the DRUM OFF switch, these two procedures are not recommended because of the possibility of undesired drum erasures. When the DC OFF switch is pressed first, the write circuits are disabled by relay 30 and erasures are prohibited.

6-94. POWER SUPPLIES

6-95. GENERAL DESCRIPTION. The power supplies are designed to maintain an almost constant d-c output under widely varying input and load conditions. Figure 6-51 shows in block form the stages of a typical power supply. The a-c input is applied to a voltage-stabilizing transformer (VST) which supplies an almost constant ac to the rectifier. Although the rectifying and filtering stages differ in construction from one power supply to another, they are of conventional design and their operation requires little explanation.

6-96. VOLTAGE-STABILIZING TRANSFORMER. A widely varying supply voltage may be stabilized automatically and almost instantaneously by the use of a device containing an appropriate combination of inductance and capacitance. The principle of operation of the voltage-stabilizing device is similar to the principle of operation of a transmission line across which is connected a capacitance for the purpose of holding up the output voltage (figure 6-52). A capacitive current, supplied by the shunt capacitance, drawn through the series-distributed inductance of the line, provides a voltage rise. Adjusting the shunt capacitance when the applied voltage varies controls the amount of voltage rise, stabilizing the output voltage.

The equivalent circuit of a VST, shown in figure 6-53, contains the same elements as the transmission line shown in figure 6-52. Basically the VST circuit is a phase-shifting network made up of a linear inductance and the parallel combination of a fixed capacitance and a nonlinear inductance. The combination of capacitance and nonlinear inductance acts as a capacitor whose capacitance varies as a function of the applied voltage. As the applied voltage increases, the fixed capacitor current increases linearly while the nonlinear inductor current increases exponentially (figure 6-54). Since these currents are 180 degrees out of phase their difference, a net capacitive current, is drawn through the line.

When input voltage is applied, the current through L1 increases until E2 reaches point A. Beyond point A the line current decreases, and E1 decreases while E2 increases, until the vector sum of these voltages equals the input voltage. This point represents the minimum input voltage required for stabilization with E2 between A and B and the current between I_H and I_L.

The phase relationships are shown on figure 6-55a. Taking the input voltage (120 volts) as a reference vector, the line current leads the input voltage, since the load is capacitive. Voltage E1 leads the line current by 90 degrees and output voltage E2, lags the line current by 90 degrees.

Since the capacitance of the L2-C combination is inversely proportional to the voltage, a decrease in the input voltage results in an increase in the line current. This causes a change in the phase angle of voltages E1 and E2 but the amplitude of the output voltage E2 remains nearly constant.

If the load is changed from no load (NL) to full load (FL) a similar phase shift occurs in such a direction as to prevent any appreciable decrease in the output voltage (figure 6-55b).

The individual inductances and capacitance can actually be physically separated and connected as in figure 6-53 or they can be coupled magnetically as in figure 6-56. The latter method is the one used. Leakage inductance between the primary and secondary provides the linear inductance. The secondary winding and core section provide the nonlinear inductance. Electromagnetically the two types of association are equivalent. A compensating winding which further improves stabilization is added in the VST's in the system.

Figure 6-57 is a complete schematic of the +100-volt supply used. The VST output is applied to a full-wave bridge-rectifier circuit. Capacitor C2 filters the d-c output and R1 is a bleeder resistor. This power supply is designed to maintain an output voltage of +100 volts $\pm$ 5 per cent under widely varying input and load conditions.

6-97. POWER-SUPPLY INTERCONNECTIONS. Many of the voltages required by the system are developed in single power-supply units and applied directly to a load. However, many more voltages are obtained from interconnections among the various power supplies, as shown in figure 6-58.

The 15-volt and the -30-volt supplies are connected series aiding. Output voltages of -30 and -45 volts with respect to ground are developed by this combination. There is also a 2-volt supply, connected series aiding to the -30-volt supply, which provides -32 volts. If the Bull punch is to be used instead of the Tower punch, the -30-volt supply is replaced by a -40-volt supply and the preceding voltages are all increased by 10 volts to -40, -42, and -55 volts.

Although the +35-volt and +16-volt supplies are each connected directly across a load, they are connected together through R5, R8, and R4. Intermediate voltages between +16 and +35 volts may then be obtained between the R4 and R5 movable contacts and ground. Voltages between zero and +16 volts are available across R7. The movable contact which is set at the +10-volt level makes this voltage available for use throughout the system. The +3-volt level is developed in a separate supply because of the high current requirements at this voltage.

Other power supplies such as the -29-volt and -150-volt supplies are connected in a similar manner but fewer connections are provided for obtaining intermediate voltages. Capacitors C31 and C34 bypass noise impulses around R1 and prevent fluctuations in the -50-volt level.

In the high-voltage supplies -1600 volts is taken as the reference level. The -1650-volt level is obtained by connecting a 50-volt supply and the 1600-volt supply series aiding. The -1300-volt level is obtained by connecting a 300-volt supply and the 1600-volt supply series opposing.

6-98. VOLTAGE MONITOR

The system is equipped with the centralized voltage-monitoring system shown in figure 6-59, by which all the d-c voltage levels plus both phases of the clock output can be monitored using a single meter movement. Since all the voltages have a small allowable percentage of deviation, the meter is used to measure only the deviations. Only one meter scale is required since all readings are in per cent deviation rather than in volts.

To monitor a given voltage, selector switches 7 and 8 must be set as indicated on the chart in figure 6-59. To monitor the +3-volt supply, for example, the POLARITY SELECTOR, switch 8, is set to + and the VOLTAGE SELECTOR, switch 7, is

set to position A. This setting places a 4.39-k multiplier (R30) in series with the meter movement. Current then flows from ground through terminal 1 deck B, the meter movement and R18, terminal 1 deck A, and R30 to the +3-volt supply. If the output of the +3-volt supply is exactly +3 volts, just enough current flows through the meter movement to give a center scale reading.

If output of the 3-volt supply rises to +3.15 volts, additional current flows through the meter movement and the meter reads +5 per cent. If the output falls to +2.85 volts, less current flows through the meter and the meter reads -5 per cent. The maximum allowable deviation for the +3-volt supply is ± 5 per cent. If the monitor indicates a deviation greater than ± 5 per cent, the power supply circuit must be examined to determine the cause of the abnormal reading.

Since the meter contains a d-c movement, the clock output must be rectified before it can be monitored. To monitor the A-phase clock output, for example, switch 8 is set to + and switch 7 is set to position V. The A-phase clock output is rectified by CR1 and applied to the choke input filter consisting of L1 and C1. Diode CR2 shunts any leakage current through CR1 to ground. The multiplier resistance is composed of R1 and part of R3. (With a normal clock output of 36 volts peak-to-peak, R3 is adjusted so that the meter indicates a deviation of zero.) Current flows from ground through terminal 18 deck B, the meter movement and R18, terminal 18 deck A, the movable contact on R3, and R1 to the positive side of C1. If the clock output is normal the reading is center scale. If the output is off normal the reading indicates the deviation in percentage off normal.

6-99. FUSES

6-100. FUSE FAULT CIRCUITRY. Most computer circuits employ indicator (grasshopper) fuses. If the circuit current requirements are low a single indicator fuse is used. If the current requirements are high, a heavy cartridge fuse is placed in parallel with a smaller indicator fuse. If an overload should occur in the latter circuit, both fuses blow simultaneously. The cartridge fuse is used to conduct the large current required by the circuit and the indicator fuse is used to notify the maintenance engineer of a fuse fault. When a fuse fault occurs the system power is turned off automatically, whether entirely or in part depending upon which circuit contains the blown fuse. A typical fuse fault circuit is shown in figure 6-60.

If a fuse fault occurs in the processor blower circuits the standby alarm, relay 15, is energized through the indicator. On positive alternations of the supply voltage, current flows from ACN through R29, K15, K13-2 normally closed, CR1,

and the indicator to the positive ACC1. Capacitor C7 maintains an almost steady current through relay 15. The K15-1 contacts drop out the drum contactor, relay 6, and initiate the turn off of all power (figure 6-50).

If a fuse fault occurs in the -1600-volt supply circuit the a-c alarm, relay 16, is energized through the indicator. On positive alternations of the supply voltage, current flows from ACN through R30, K16, K13-3 normally closed, CR4, and the indicator to the positive ACC1. The K16-1 contacts drop out the a-c contactor, relay 11, and initiate the turn off of ac and dc (figure 6-50). The drum and blowers are not turned off when relay 16 is energized.

If a fuse fault occurs in the 20-volt probe circuit the +d-c alarm, relay 17, is energized through the indicator. Current flows from the negative side of C5 through R31, K17, K14-1 normally closed, R3, and the indicator to the +20-volt supply. The K17-1 contacts drop out the d-c contactor, relay 12, and turn off dc (figure 6-50).

If the current in the primary windings of the clock output transformer exceeds 1.5 amperes, one or both grasshopper fuses connected in series with the primary windings blows. Current then flows from the negative side of C5 (figure 6-60) through R31, K17, K14-1 normally closed, the 4.3-millihenry choke (figure 6-27), the blown fuse indicator, L5, and R19 to ground. DC is turned off when the relay 17 contacts switch.

An additional safety feature, the plate overcurrent relay (figure 6-27), is incorporated in the clock output circuit. Since R19 is connected in the d-c return lead of the six 4X250B output tubes, the total d-c plate current of the output stage can be monitored across this resistor. When the current through R19 reaches slightly under 1.5 amperes the current through K1 is sufficient to switch the relay contacts. When the K1-1 contacts switch, relay 17 is energized by current which flows from the negative side of C5 (figure 6-60) through R31, K17, K14-1 normally closed, and the K1-1 normally open contacts (figure 6-27) to ground. When the K17 contacts switch, dc is turned off and the plate overcurrent relay is deenergized.

DC is also turned off if the -d-c alarm, relay 18, is energized. The K18-1 contacts drop out the d-c contactor, relay 12, and turn off dc (figure 6-50).

Since an automatic power turn off can be caused by conditions other than a blown fuse, a fuse-fault indication must be made available to the maintenance engineer. To determine whether or not a fuse is blown, press the FUSE FAULT TEST switch. This switch energizes relays 13 and 14 through the

main line switch. When the K13-1 contacts switch, current flows from the main line through K13-1 normally open, CR2, R25, and R26-C5 during negative alternations of the supply voltage. A negative potential is then developed at the top of C5.

If a fuse fault has occurred in the processor blower circuits, when the FUSE FAULT TEST switch is closed current flows from the negative side of C5 through R34, the FUSE FAULT indicator lamp, K13-2 normally open, CR1, the fuse indicator, and R1 to ACN. In the absence of a ground-return resistor corresponding to R1, the circuit would be completed from the indicator through the drum-blower fuses and the blowers to ACN. Both return methods are used in the a-c circuits of the system.

If a fuse fault has occurred in the 20-volt probe circuit, when the FUSE FAULT TEST switch is closed, current flows from the negative side of C5 through R34, the FUSE FAULT lamp, K14-1 normally open, R3, the fuse indicator, and the bleeder resistor in the +20-volt power supply to ACN.

If the FUSE FAULT lamp lights when the FUSE FAULT TEST switch is pressed, it indicates that one or more fuses have blown. The maintenance engineer then checks the fuseboards for the blown fuses.

6-101. FUSEBOARD SERVICING PRECAUTIONS. The following precautions should be observed in servicing fuseboards:

(1) Do not touch or attempt replacement of any fuses on fuseboard No. 1 unless input power is removed from entire system by operation of the external circuit breaker.

(2) Do not touch or attempt replacement of any fuses on fuseboard No. 2 unless the a-c contactor, relay 11, is deenergized.

(3) Do not touch or attempt replacement of any fuses on fuseboards No. 3 and No. 4 unless the d-c contactor, relay 12, is deenergized for 1 minute or longer.

(4) Do not touch or attempt replacement of any fuses on fuseboard No. 5 unless the d-c contactor, relay 12, has been deenergized at least 5 minutes. After failure or suspected failure of fuses, short all six fuse terminals to ground and use an insulated fuse puller.

6-102. STANDARD SYMBOLS

The symbols shown in figure 6-61 are used on all schematic wiring diagrams for the system.

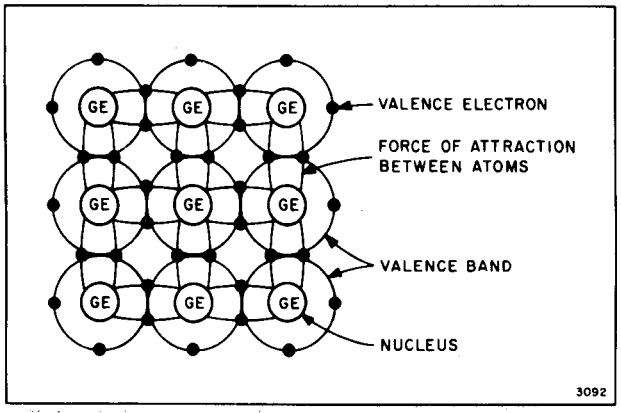


Figure 6-1. Covalent Bond in a Pure-Germanium Crystal

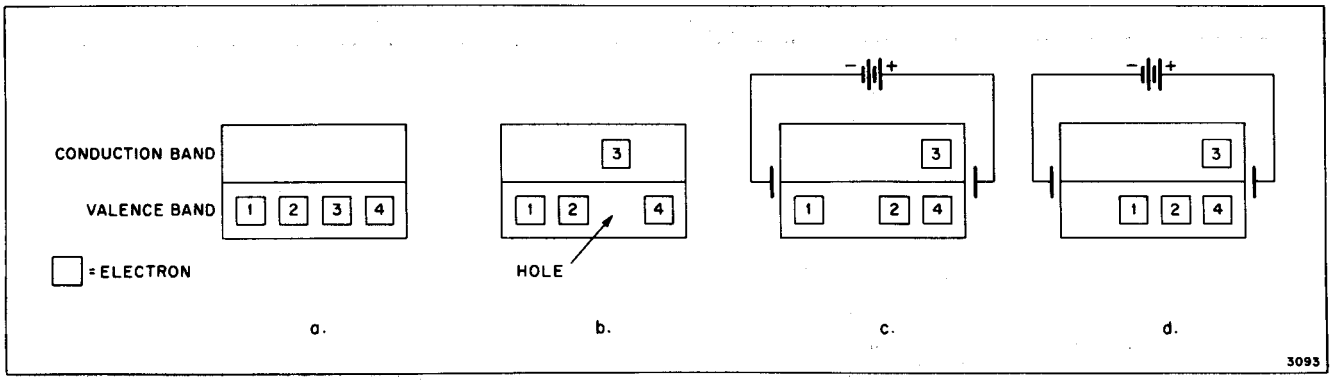


Figure 6-2. Hole Creation and Movement

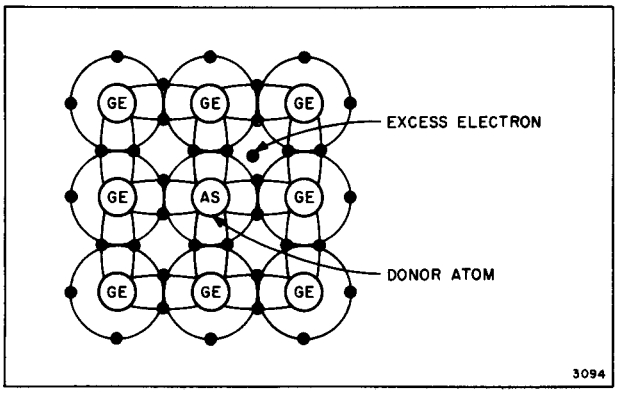


Figure 6-3. N-Type Germanium

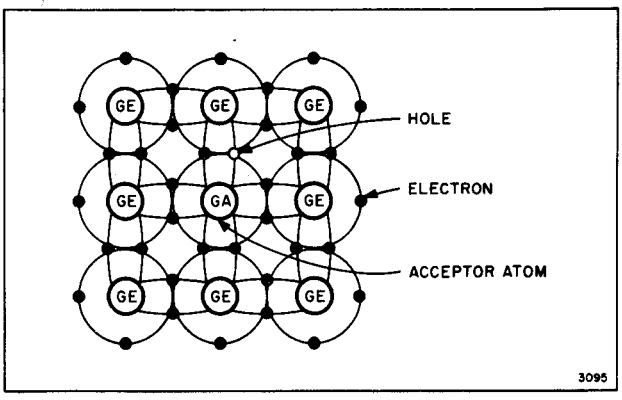


Figure 6-4. P-Type Germanium

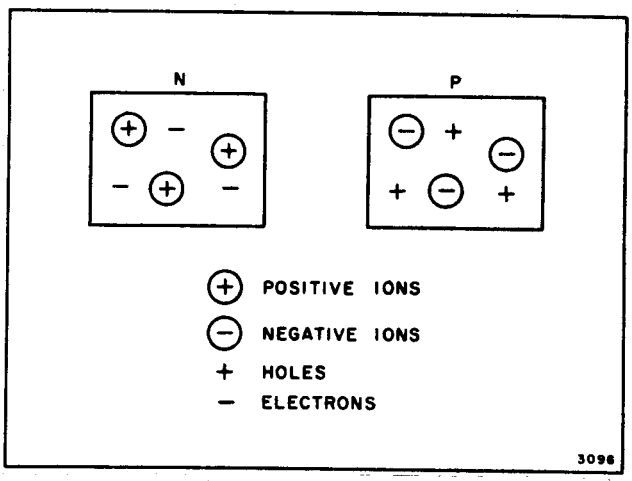


Figure 6-5. Charges in N-Type and P-Type Germanium

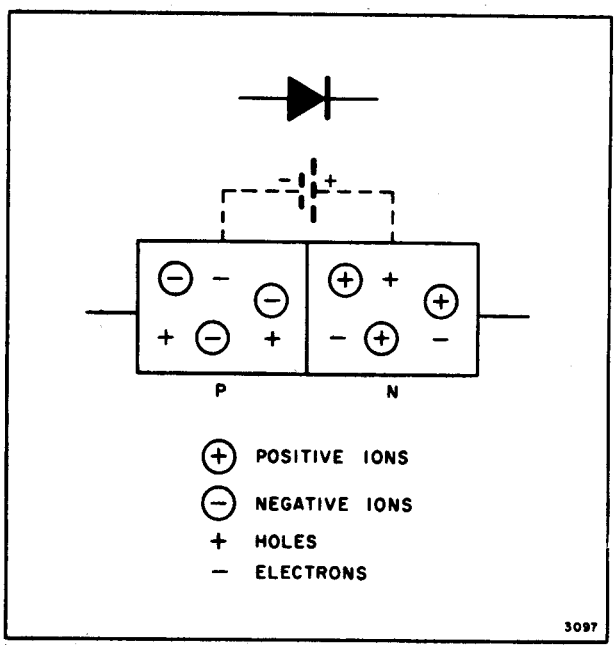


Figure 6-6. Junction Diode with Symbol

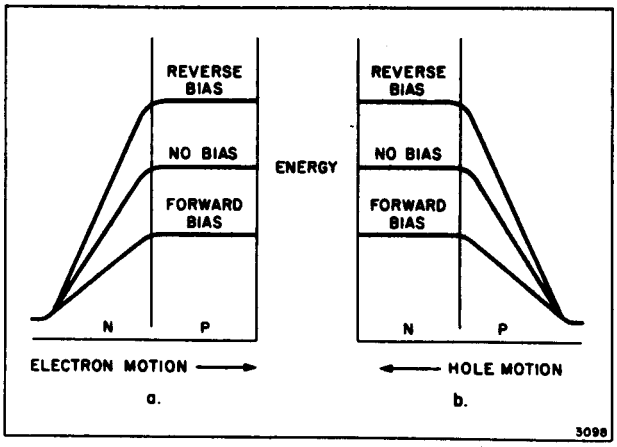


Figure 6-7. Voltage Gradients as Potential Hills

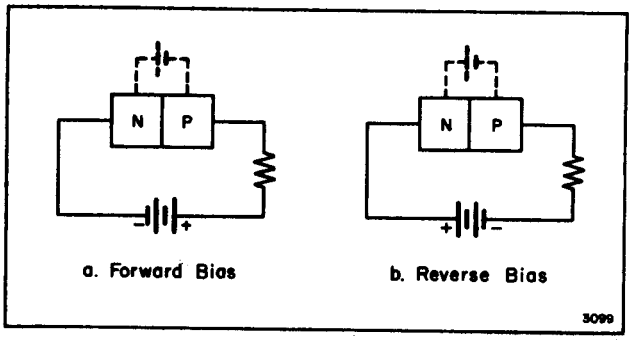


Figure 6-8. Biasing Connections

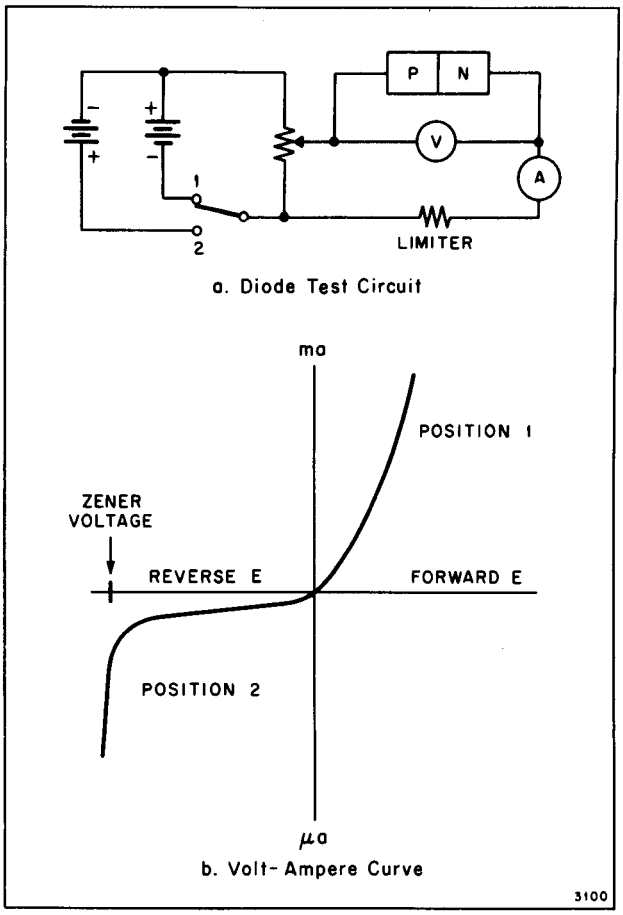


Figure 6-9. Diode Characteristic and Test Circuit

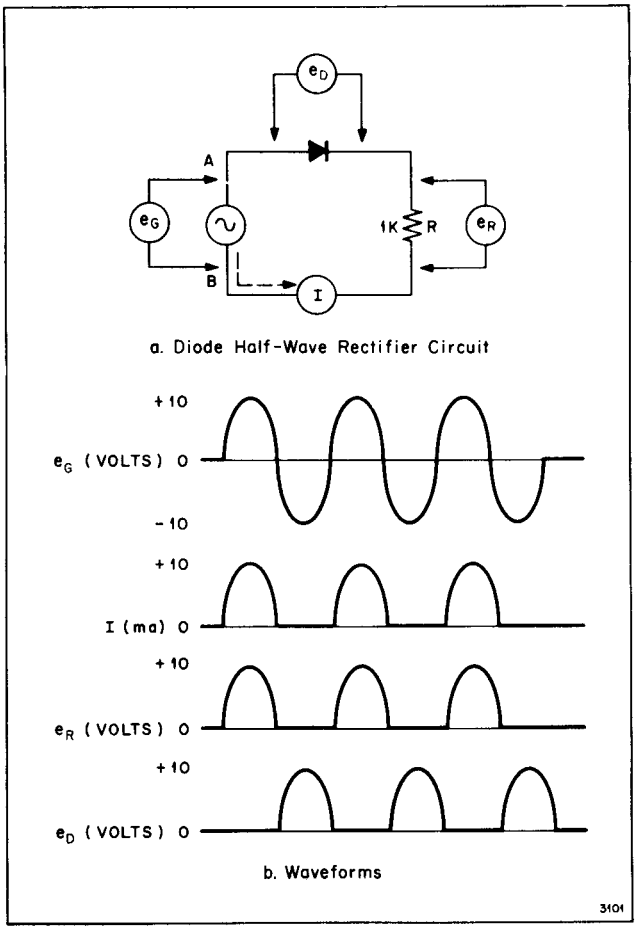


Figure 6-10. Junction Diode Used as Rectifier

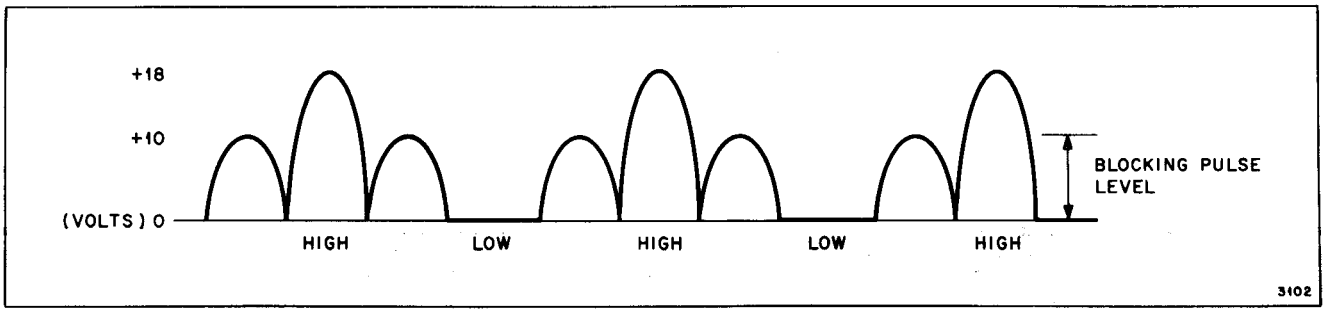


Figure 6-11. High and Low Information Pulses

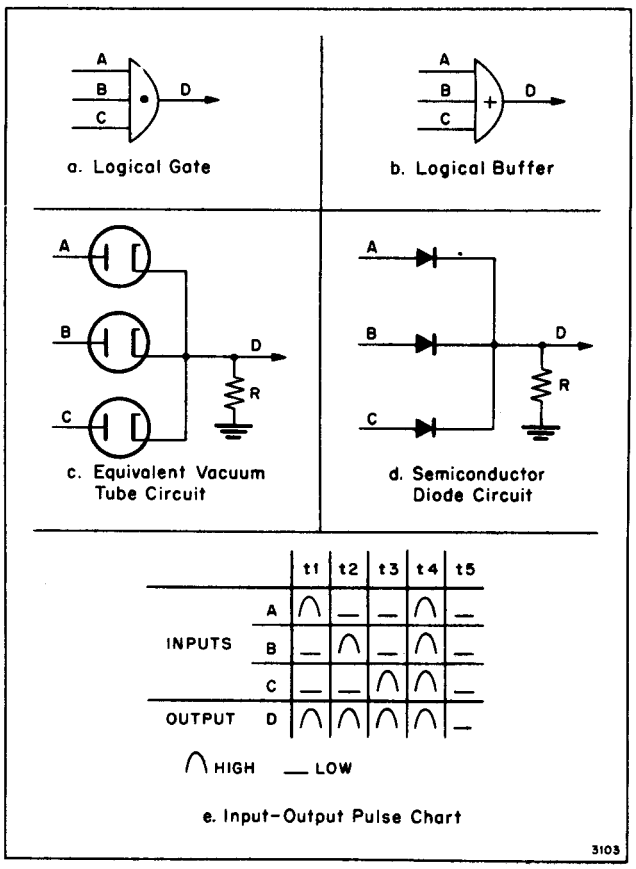


Figure 6-12. Gate and Buffer Circuits

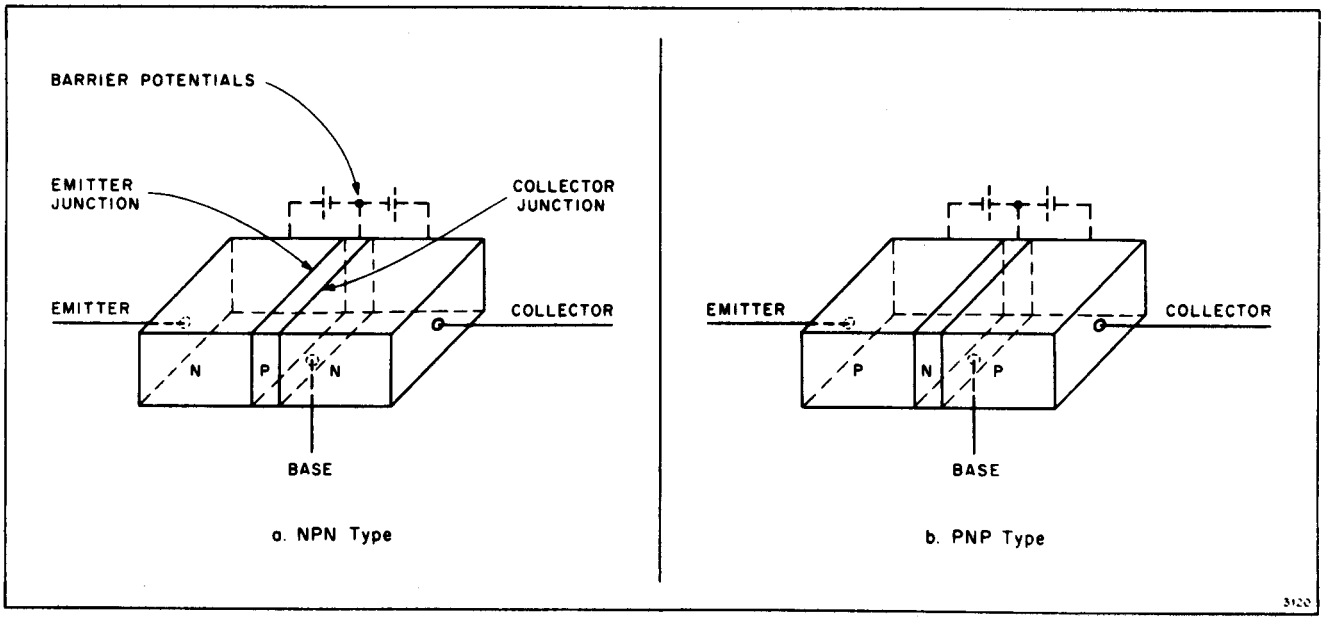


Figure 6-13. Junction Transistors

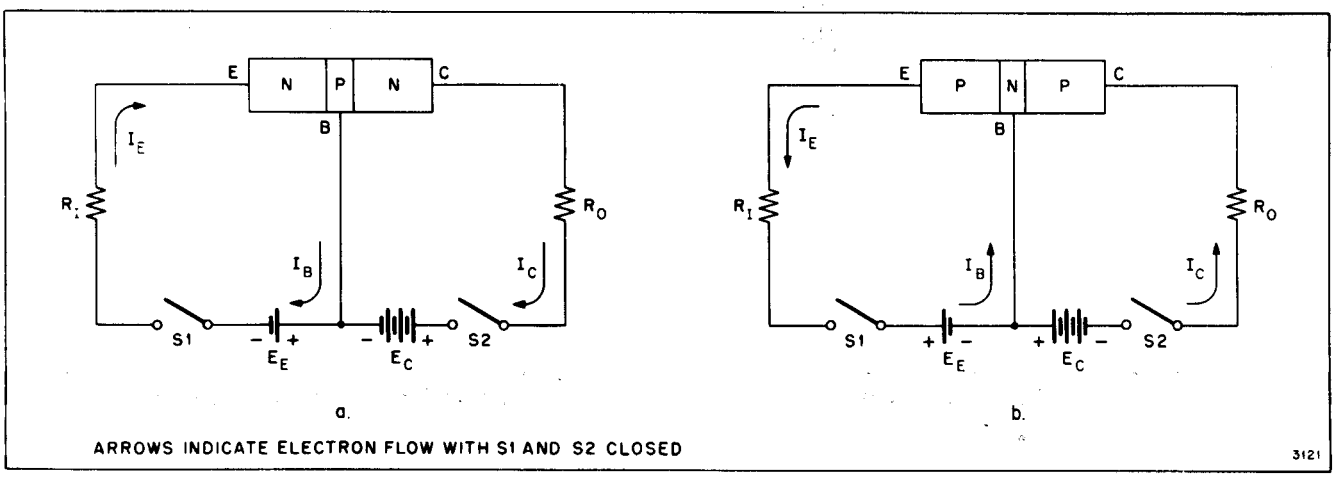


Figure 6-14. Application of Bias Potentials

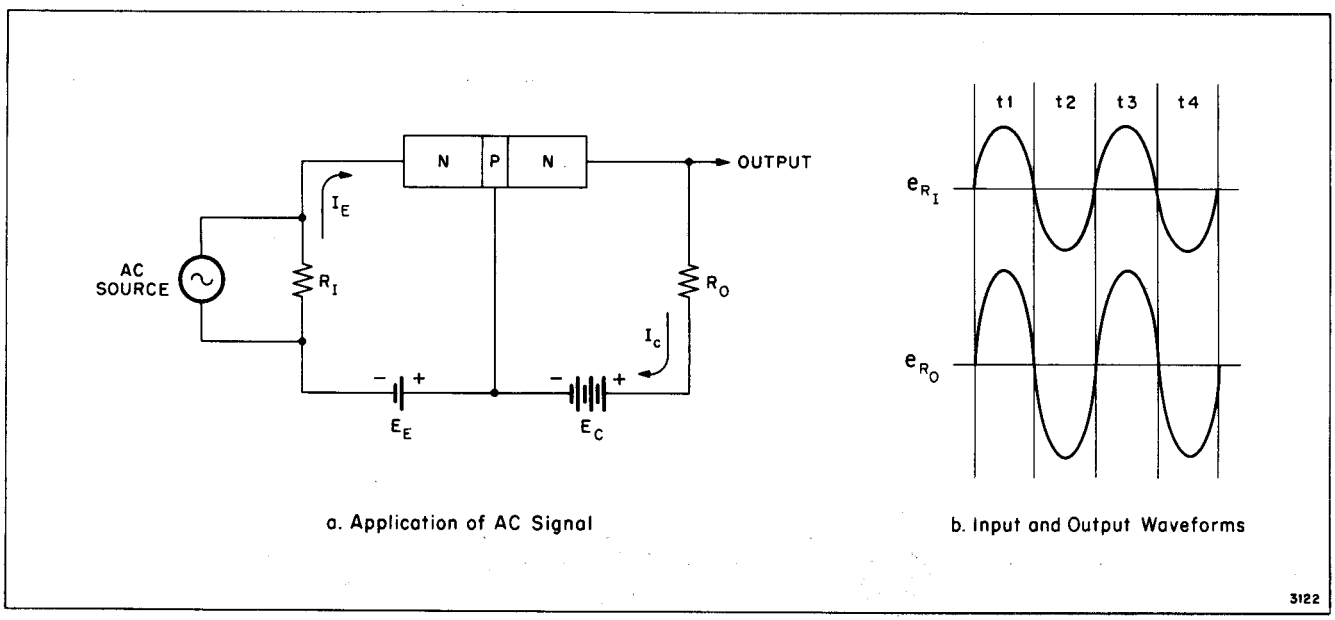


Figure 6-15. Common-Base Transistor Amplifier

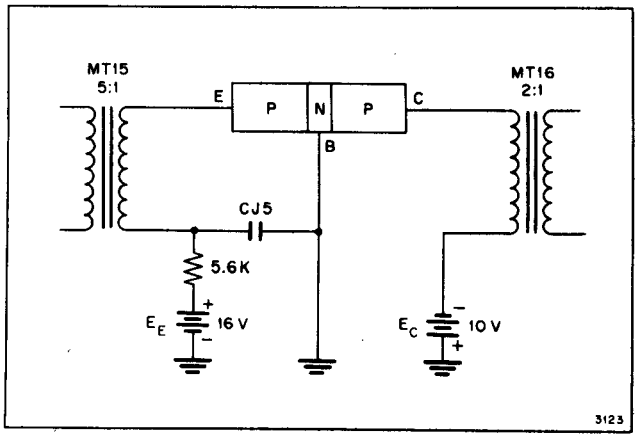


Figure 6-16. Common-Base Class A Amplifier Stage

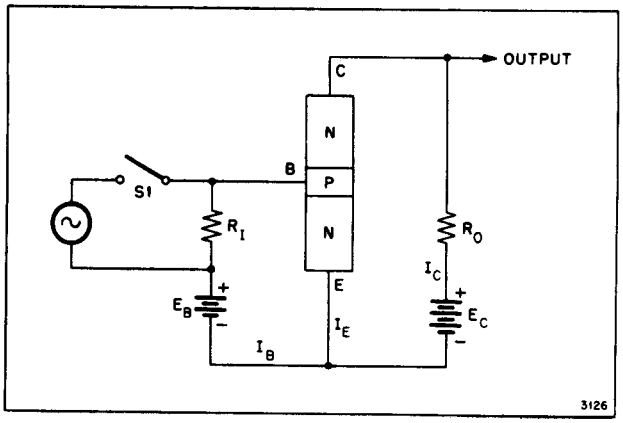


Figure 6-17. Common-Emitter Transistor Amplifier

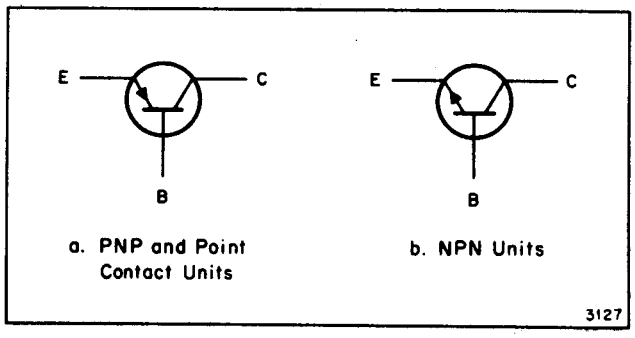


Figure 6-18. Transistor Symbols

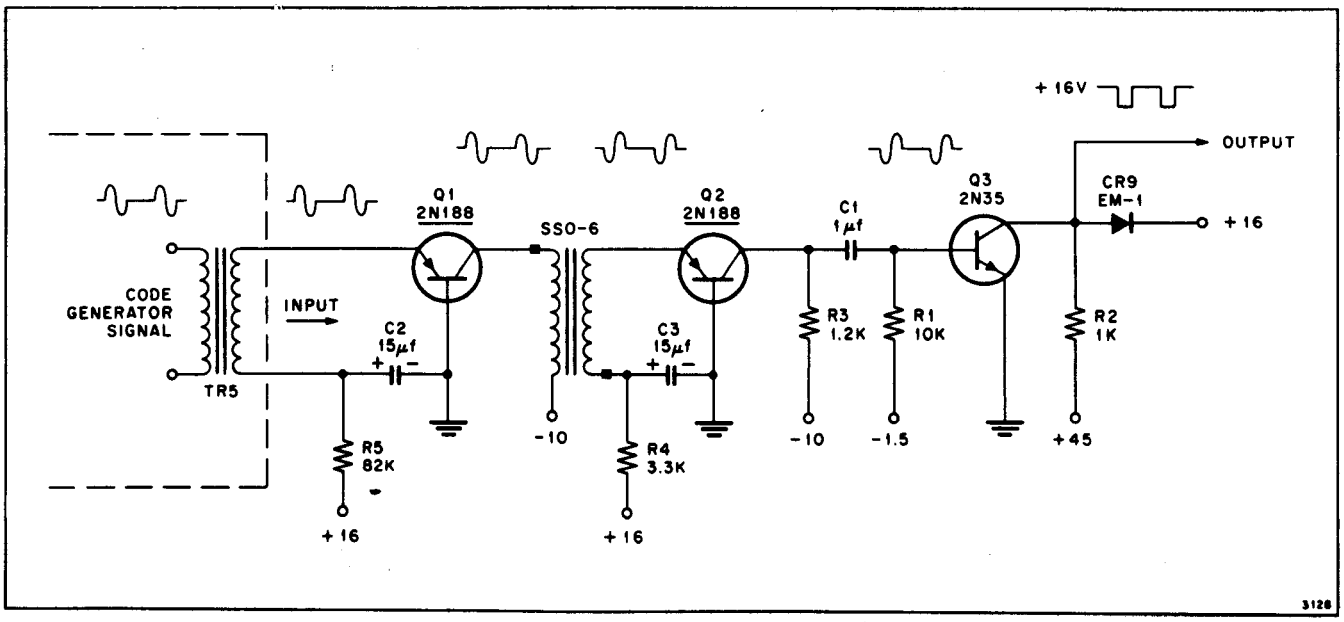
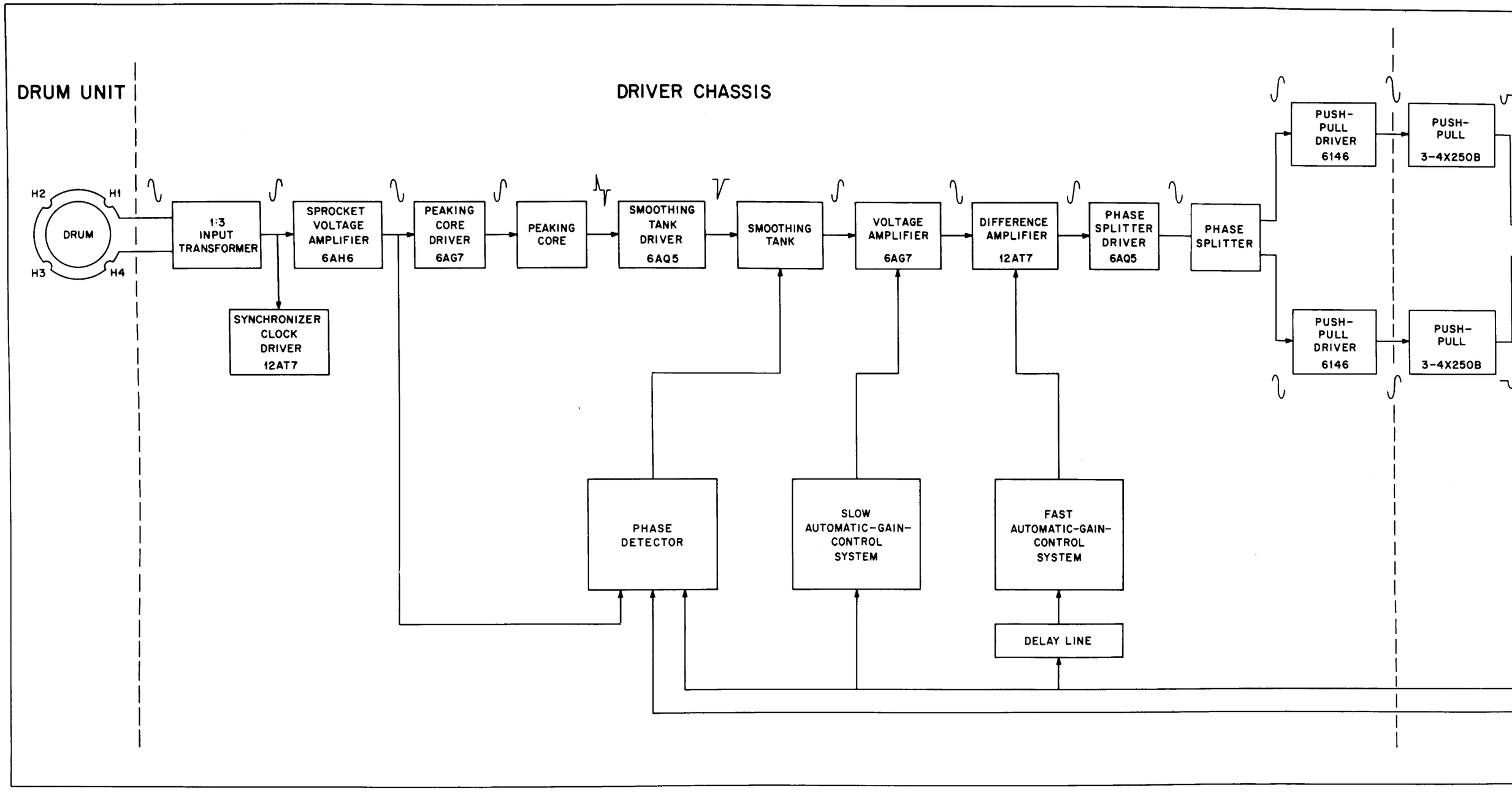


Figure 6-19. Typical Transistorized Circuit


DRUM UNIT
DRIVER CHASSIS
H2
H1
DRUM
H3
H4
1:3 INPUT TRANSFORMER
SYNCHRONIZER CLOCK DRIVER 12AT7
SPROCKET VOLTAGE AMPLIFIER 6AH6
PEAKING CORE DRIVER 6AG7
PEAKING CORE
SMOOTHING TANK DRIVER 6AQ5
SMOOTHING TANK
VOLTAGE AMPLIFIER 6AG7
DIFFERENCE AMPLIFIER 12AT7
PHASE SPLITTER DRIVER 6AQ5
PHASE SPLITTER
PUSH-PULL DRIVER 6146
PUSH-PULL 3-4X250B
PUSH-PULL DRIVER 6146
PUSH-PULL 3-4X250B
PHASE DETECTOR
SLOW AUTOMATIC-GAIN-CONTROL SYSTEM
FAST AUTOMATIC-GAIN-CONTROL SYSTEM
DELAY LINE

Figu

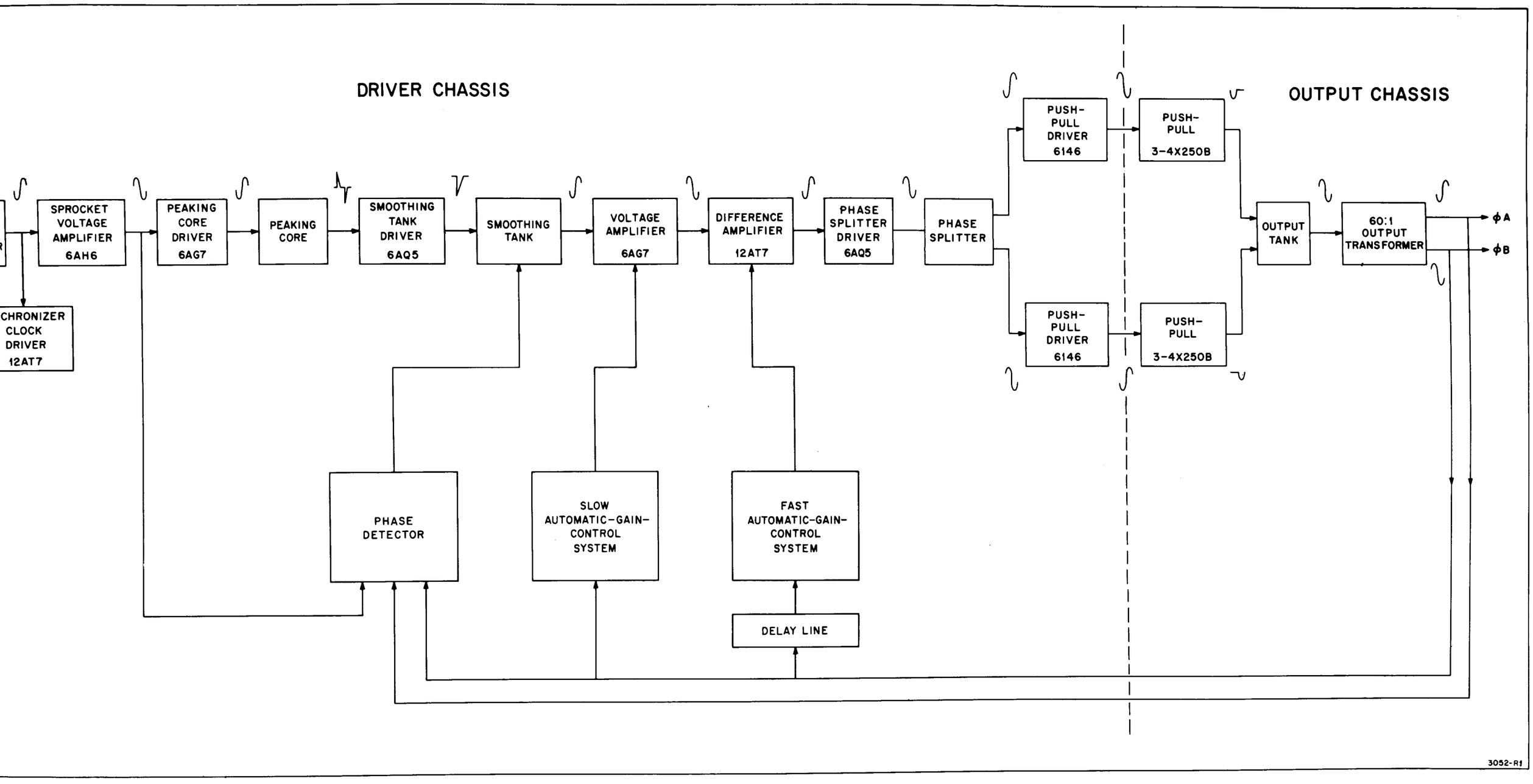


Figure 6-20. Clock, Block Diagram

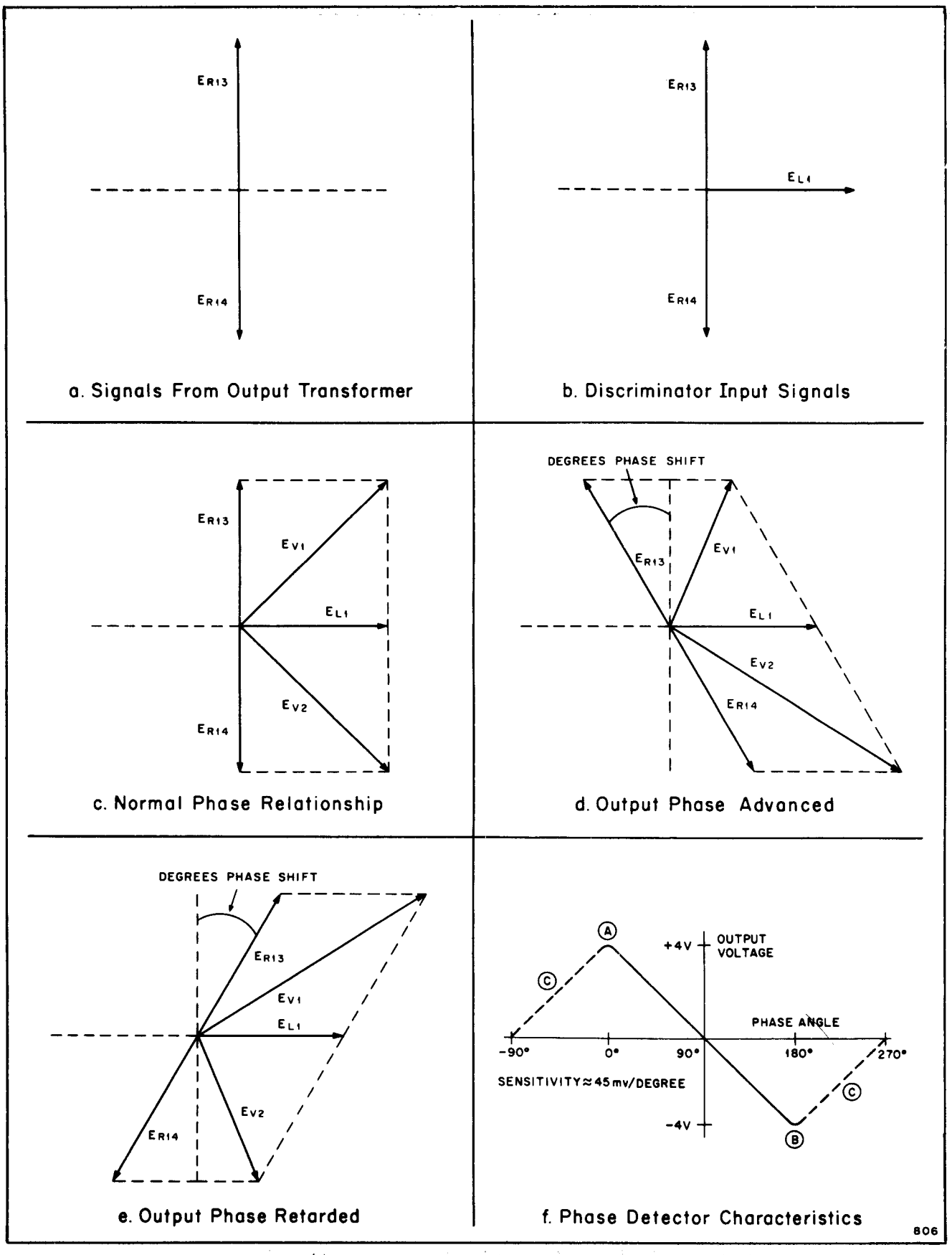


Figure 6-21. Phase Detector Signals

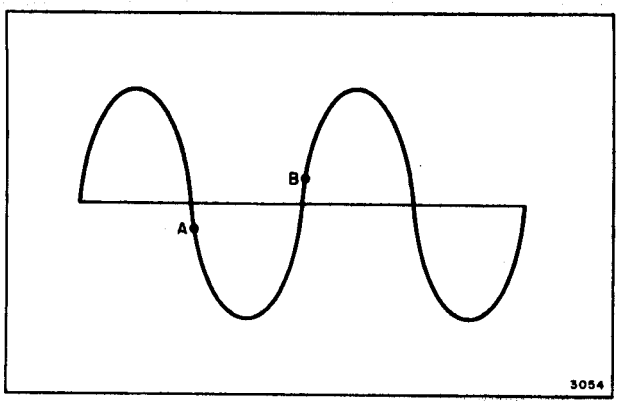


Figure 6-22. Core Flipping Points

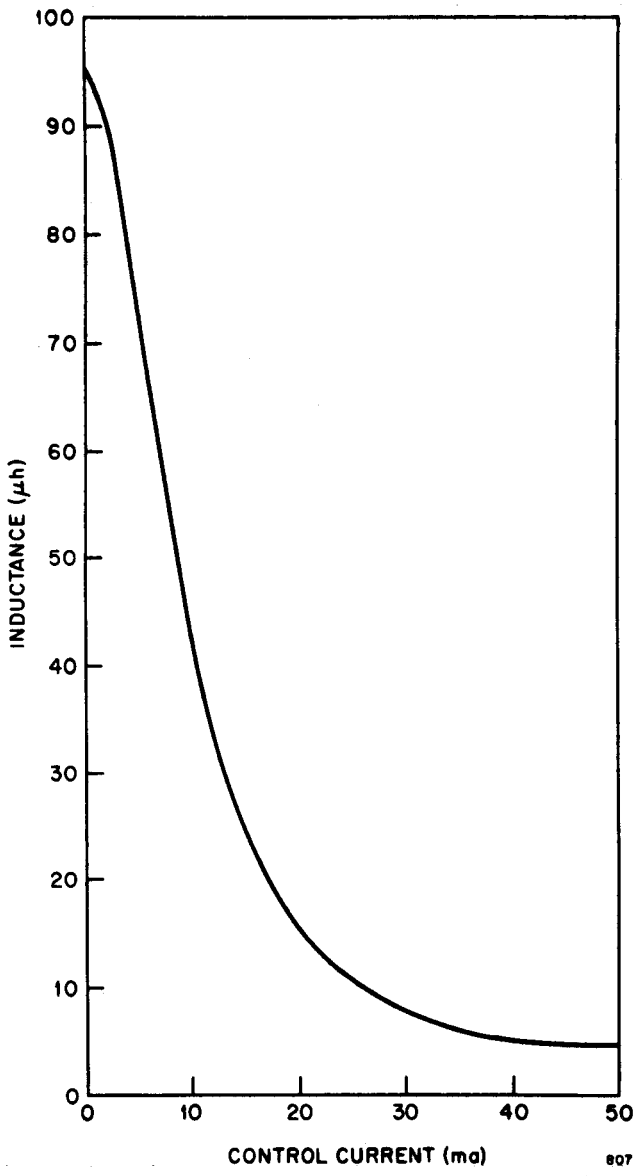


Figure 6-23. Increductor Characteristics

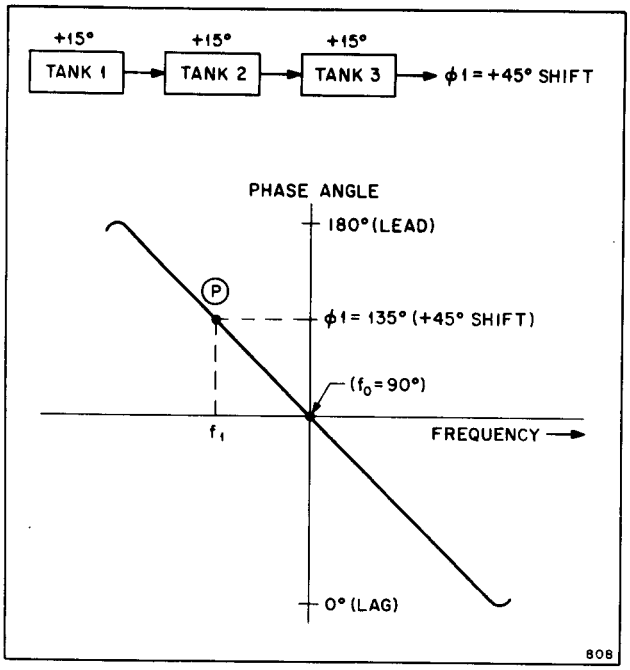


Figure 6-24. Phase Response of Three Cascaded Tank Circuits with No Phase Control

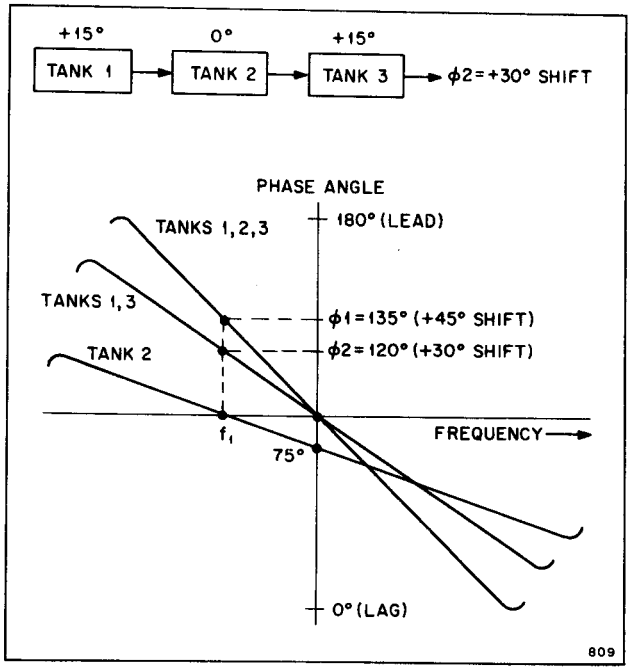


Figure 6-25. Partial Phase Correction

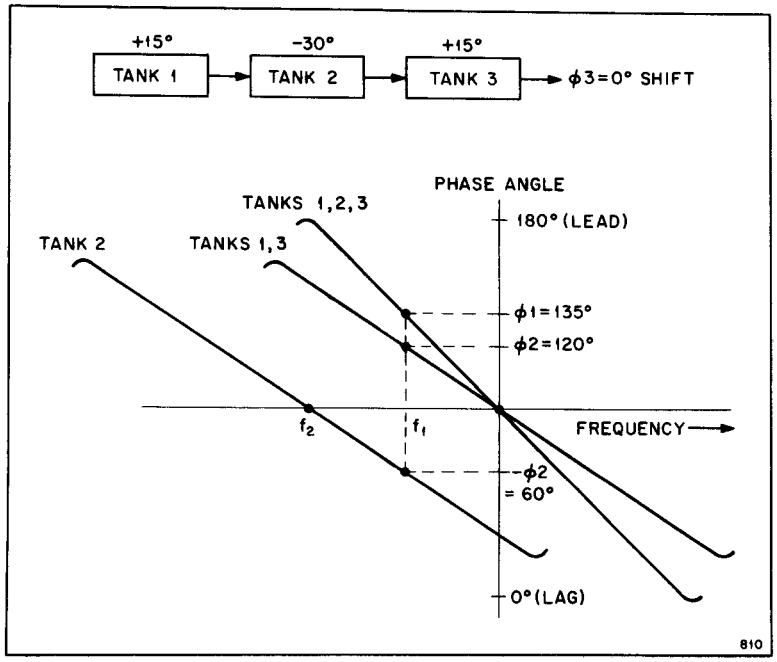


Figure 6-26. Full Phase Correction

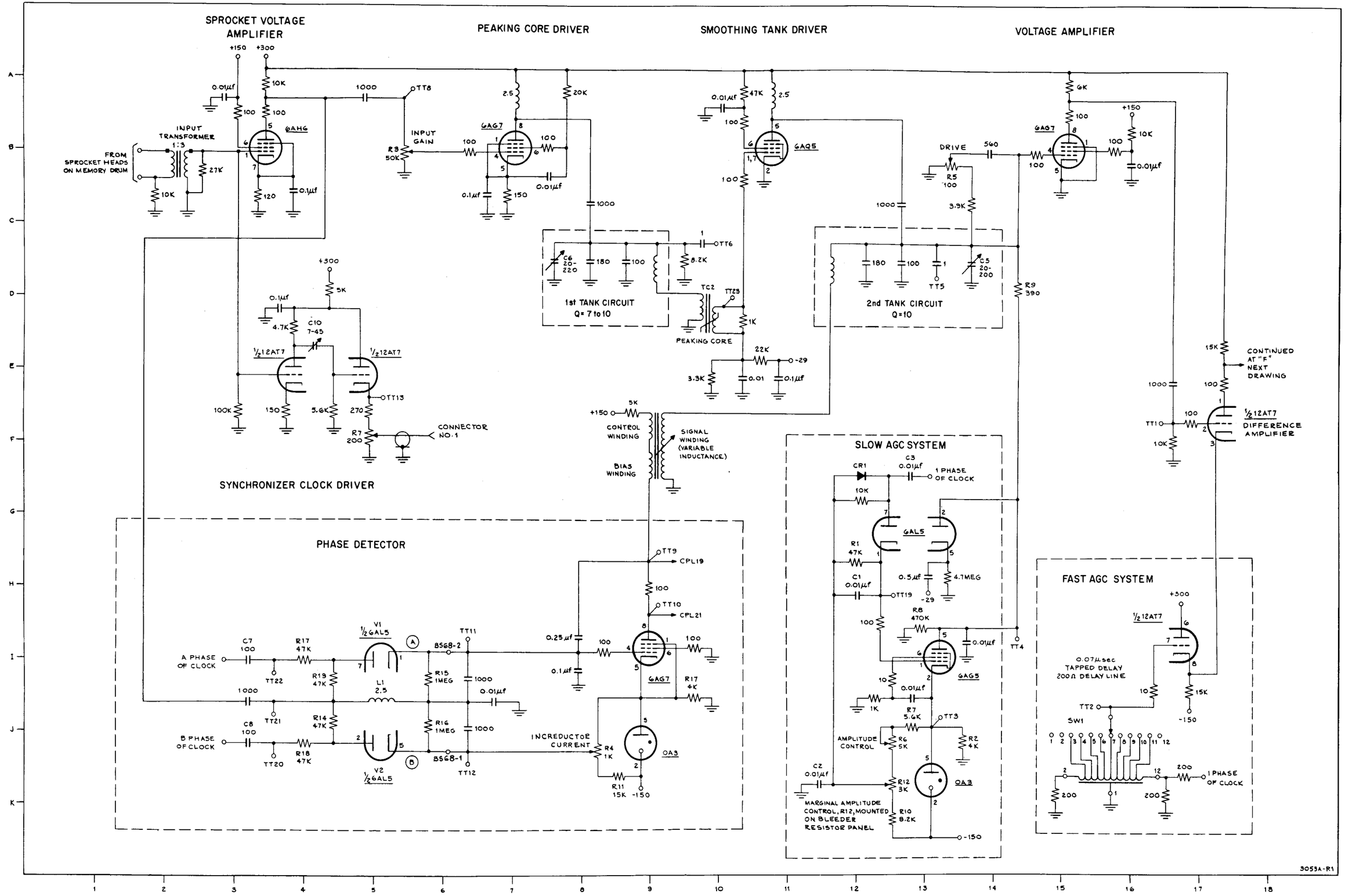


Figure 6-27. Clock, Schematic

DRIVER CHASSIS

OUTPUT CHASSIS

PUSH-PULL STAGE

PUSH-PULL DRIVERS

PHASE SPLITTER DRIVER

PHASE SPLITTER

TANK CIRCUIT

METER PANEL

NOTES:

UNLESS OTHERWISE NOTED,

CAPACITANCE IS IN MICRO-MICROFARADS
RESISTANCE IS IN OHMS AND
INDUCTANCE IS IN MICROHENRIES

MANUAL CONTROL AND TEST TERMINAL LOCATION:

DESIGNATION	NAME	LOCATION
C5	2nd TANK	D14
C6	1st TANK	D8
C9	OUTPUT TANK	D33
C10	SYNCHRONIZER CLOCK INPUT PHASE	E4
L6	OUTPUT TANK	D34
R3	INPUT GAIN	B5
R4	INCREDUCTOR CURRENT	J8
R5	DRIVE	D13
R6	AMPLITUDE CONTROL	J13
R7	SYNCHRONIZER CLOCK INPUT AMPLITUDE	F5
R12	MARGINAL AMPLITUDE CONTROL	K13
R20	OVERCURRENT RELAY CONTROL	H35
SW1	DELAY LINE	J16
SW48	CURRENT SELECTOR	J10
SW57	VOLTAGE SELECTOR	J26
TT1	TEST TERMINAL	F16
TT2		J16
TT3		J13
TT4		I14
TT5		D13
TT6		C10
TT7		D2
TT8		A5
TT9		H9
TT10		H9
TT11		I6
TT12		K6
TT13		E5
TT17		E21
TT18		F21
TT19		H13
TT20		J3
TT21		J3
TT22		I3
TT23		D10

30538-R1

Figure 6-27. Clock, Schematic (cont.)

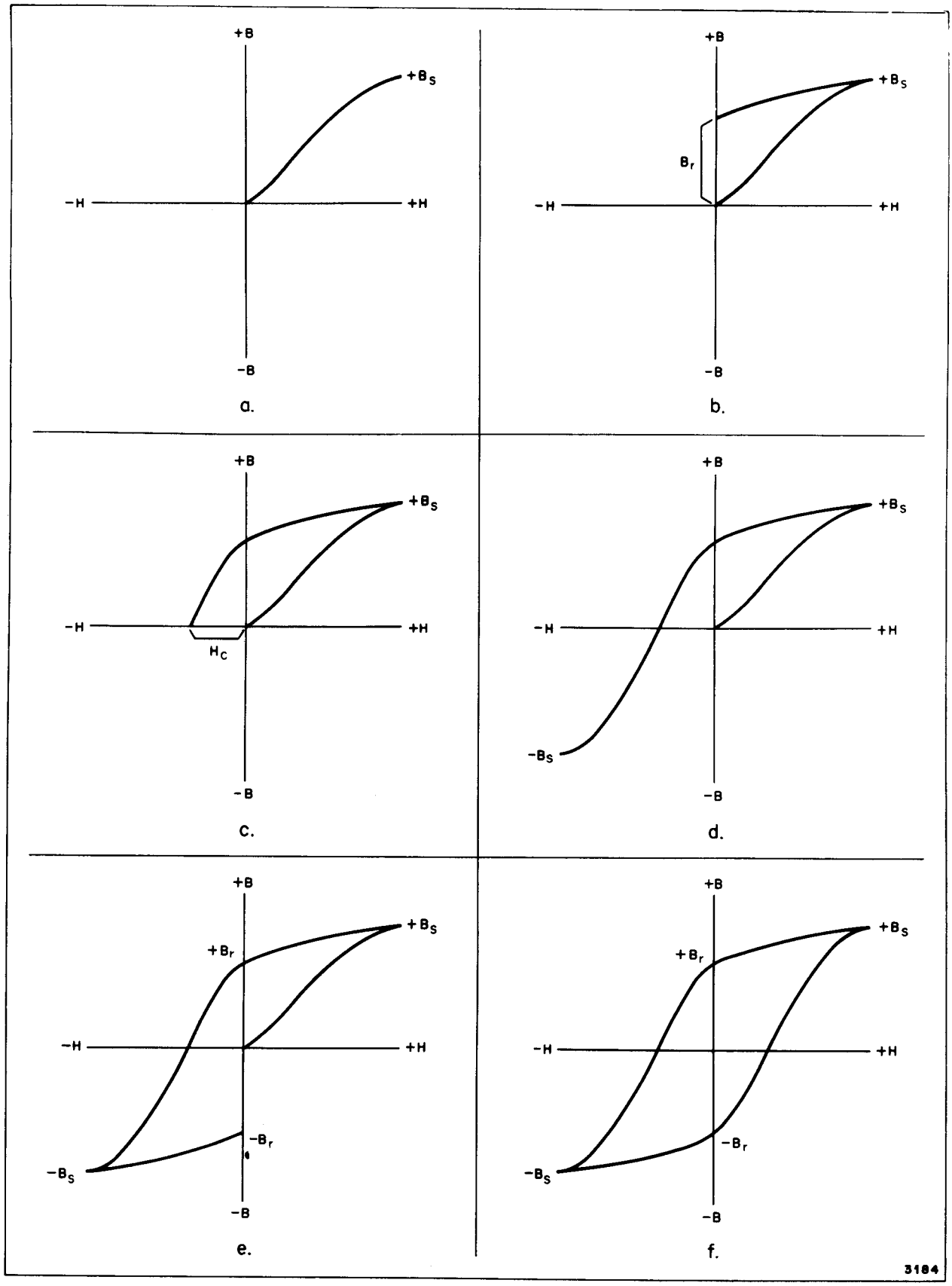


Figure 6-28. Hysteresis Loop Development

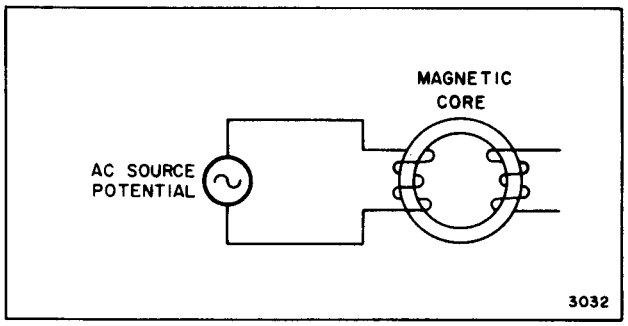


Figure 6-29. Magnetic Core with Windings

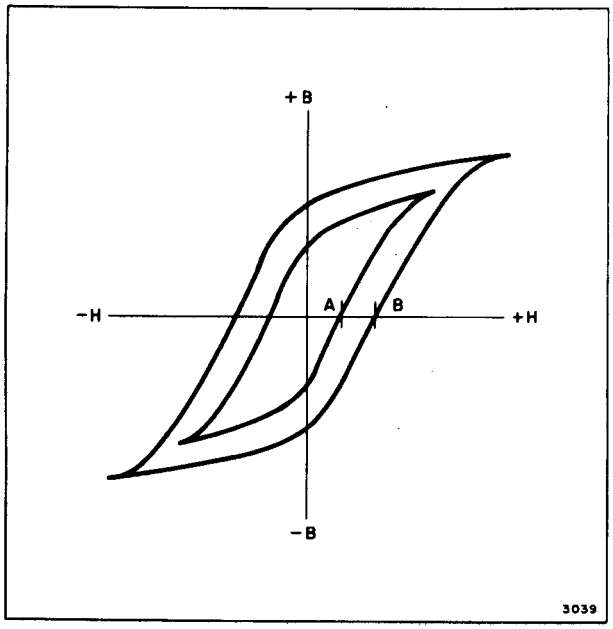


Figure 6-30. Typical Hysteresis Loops

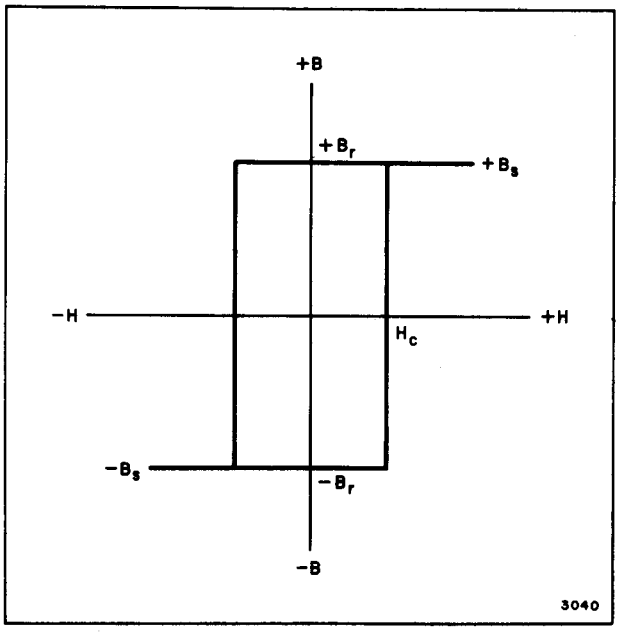


Figure 6-31. Idealized Hysteresis Loop

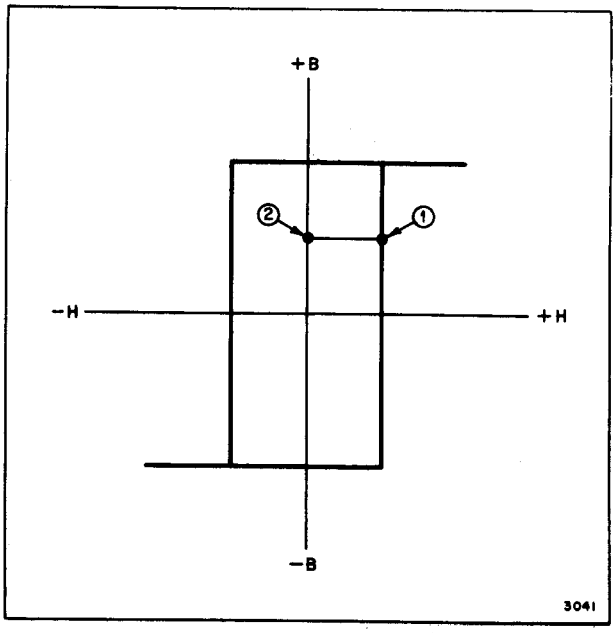


Figure 6-32. Hysteresis Loop for Nonreactive Coil

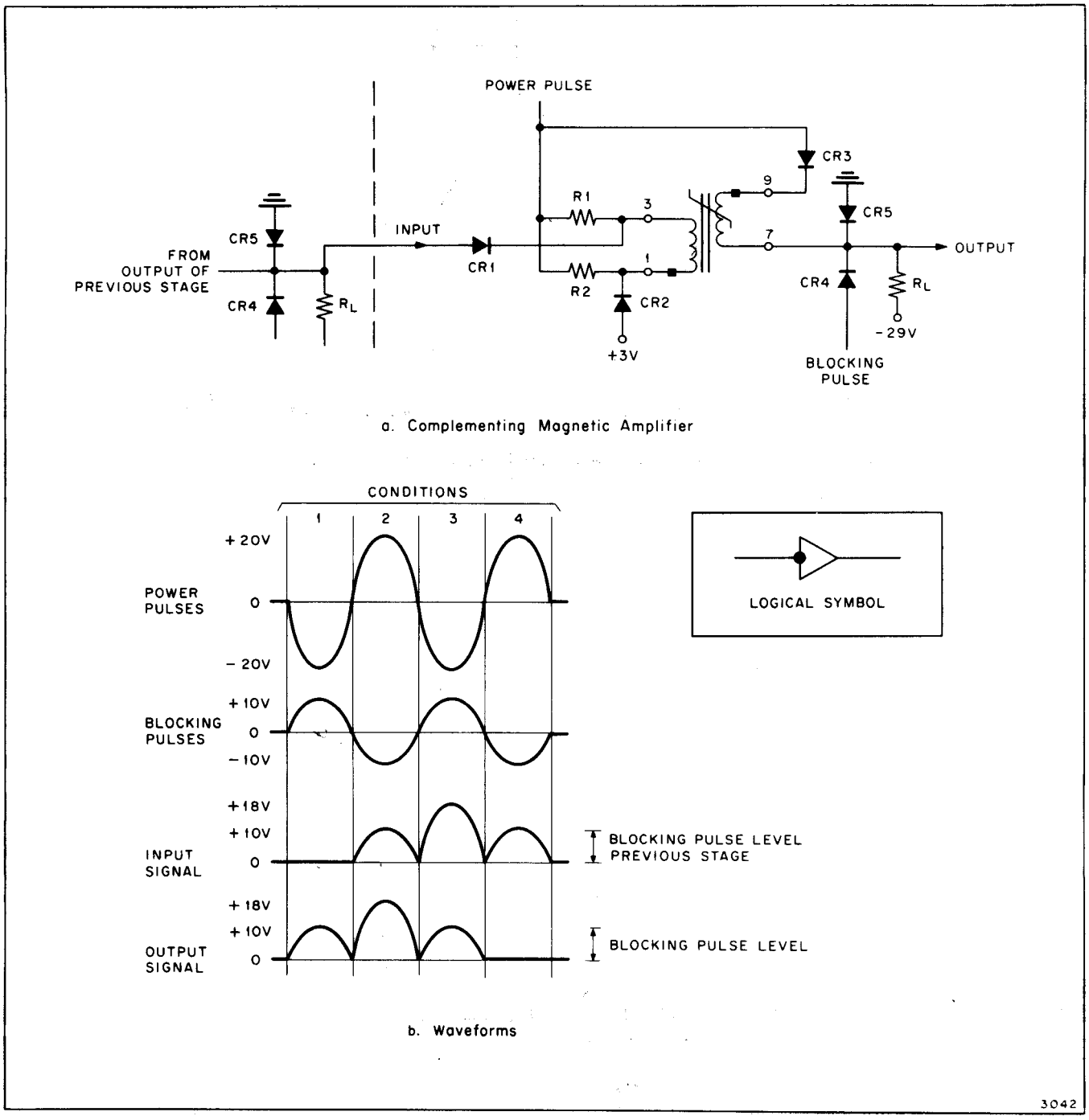


Figure 6-33. Complementing Magnetic Amplifier

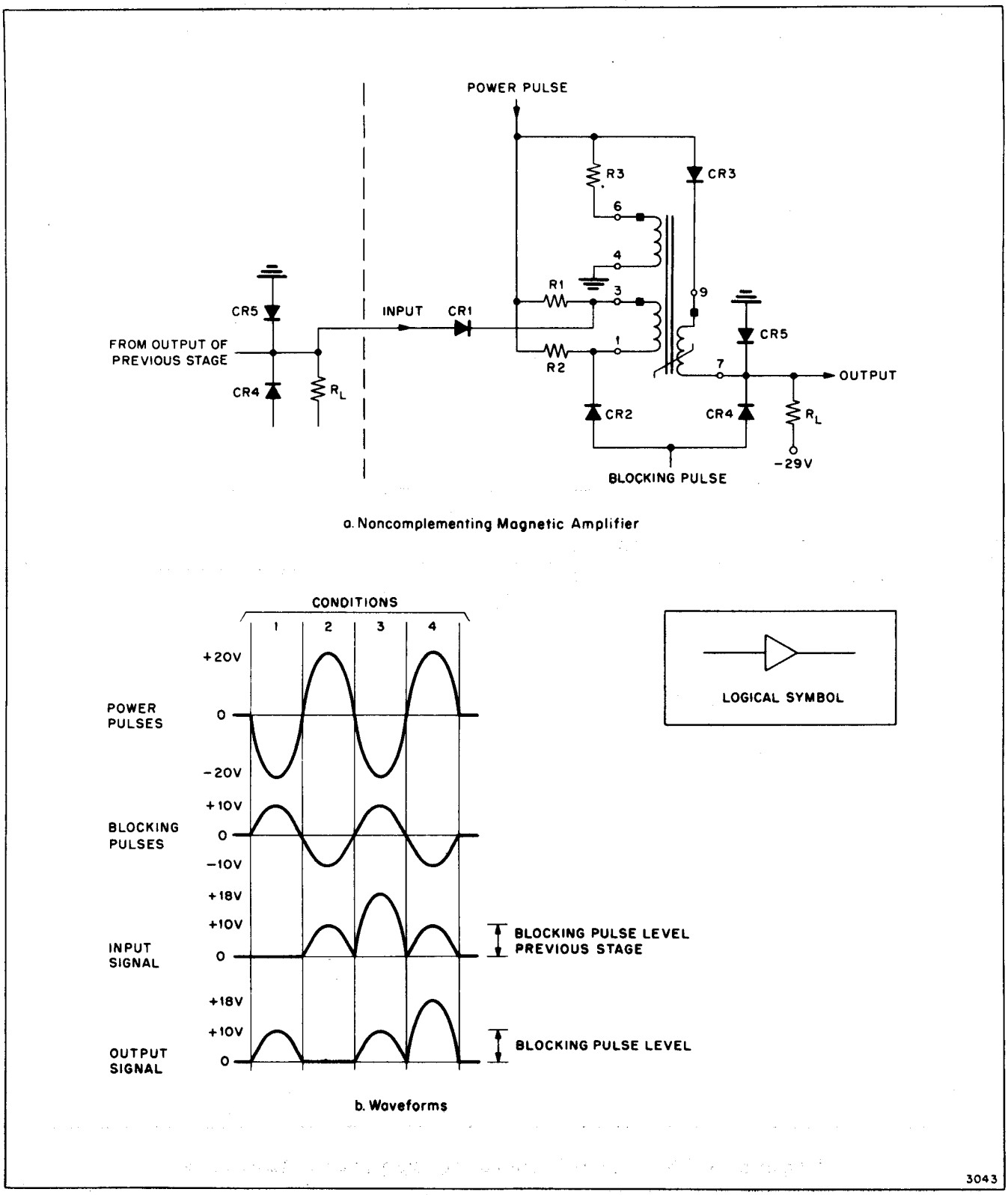


Figure 6-34. Noncomplementing Magnetic Amplifier

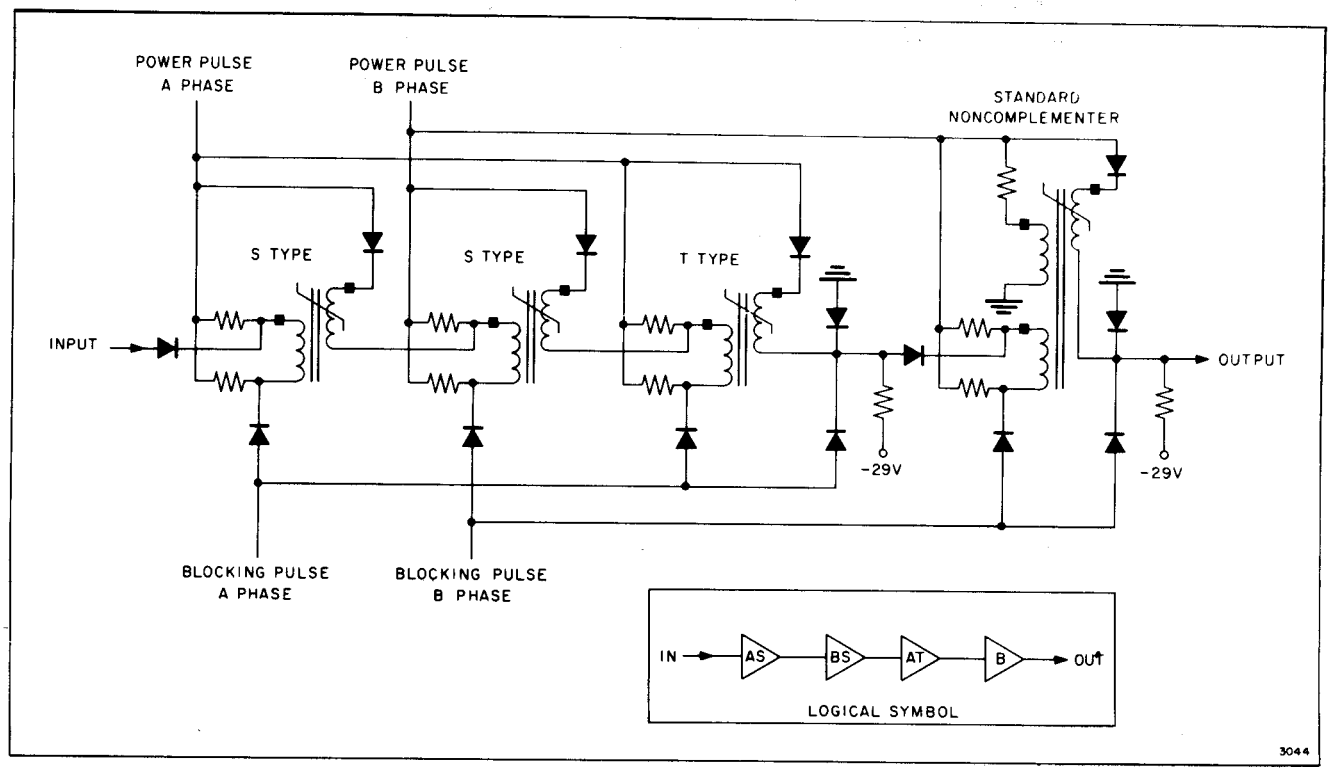


Figure 6-35. Arithmetic Register

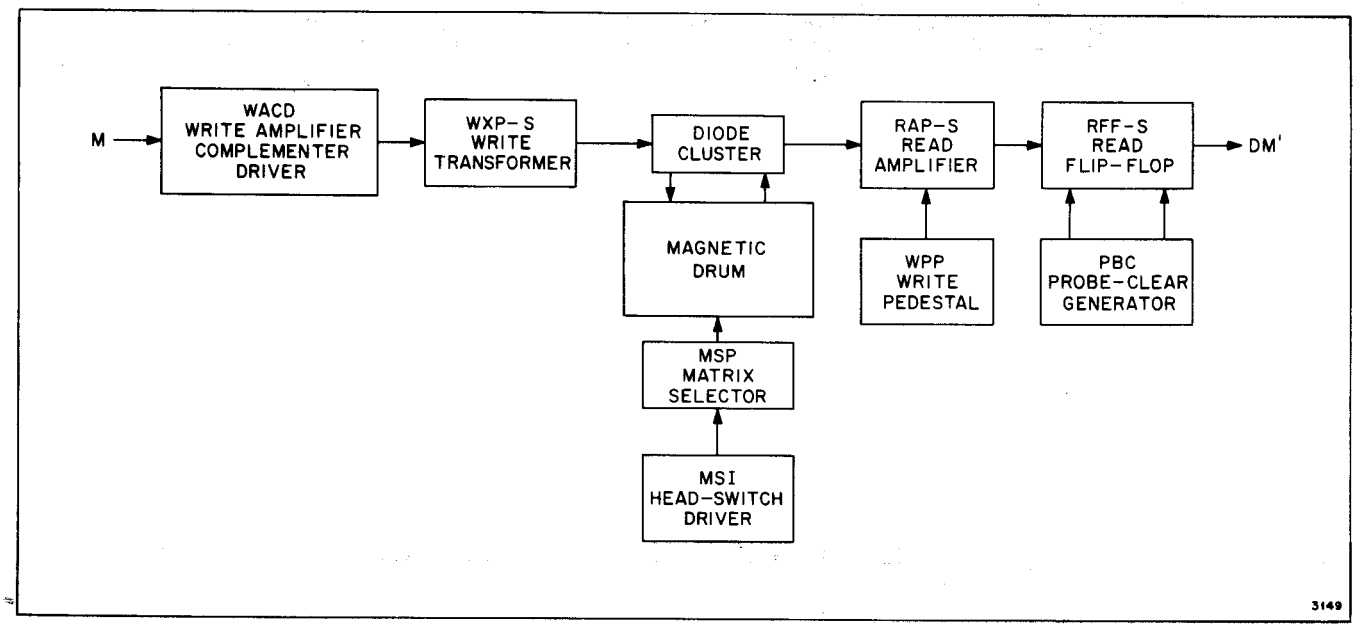


Figure 6-36. Storage Unit

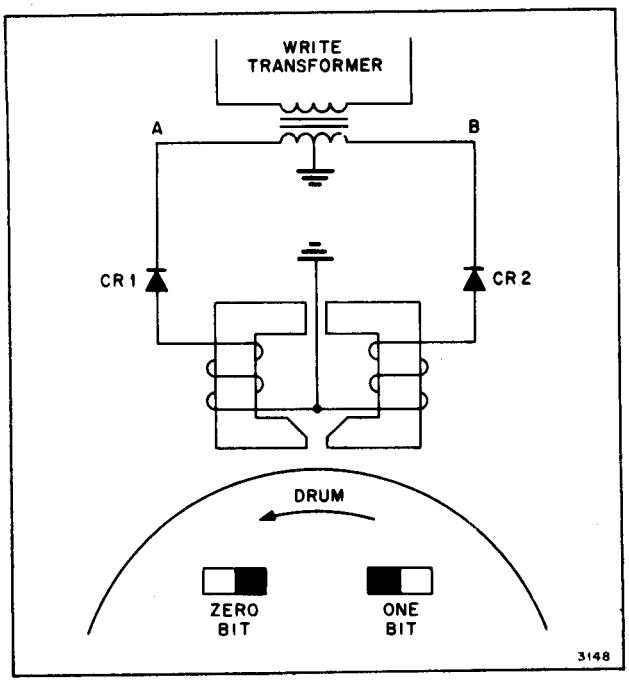


Figure 6-37. Recording Method

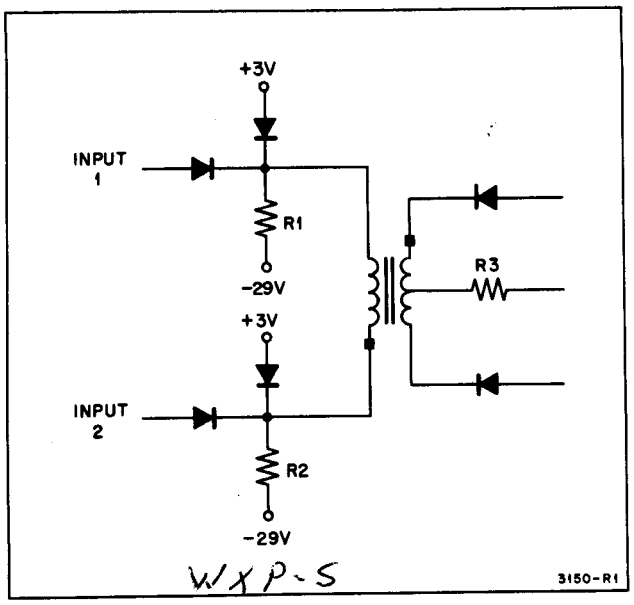


Figure 6-38. Write-Transformer Circuit

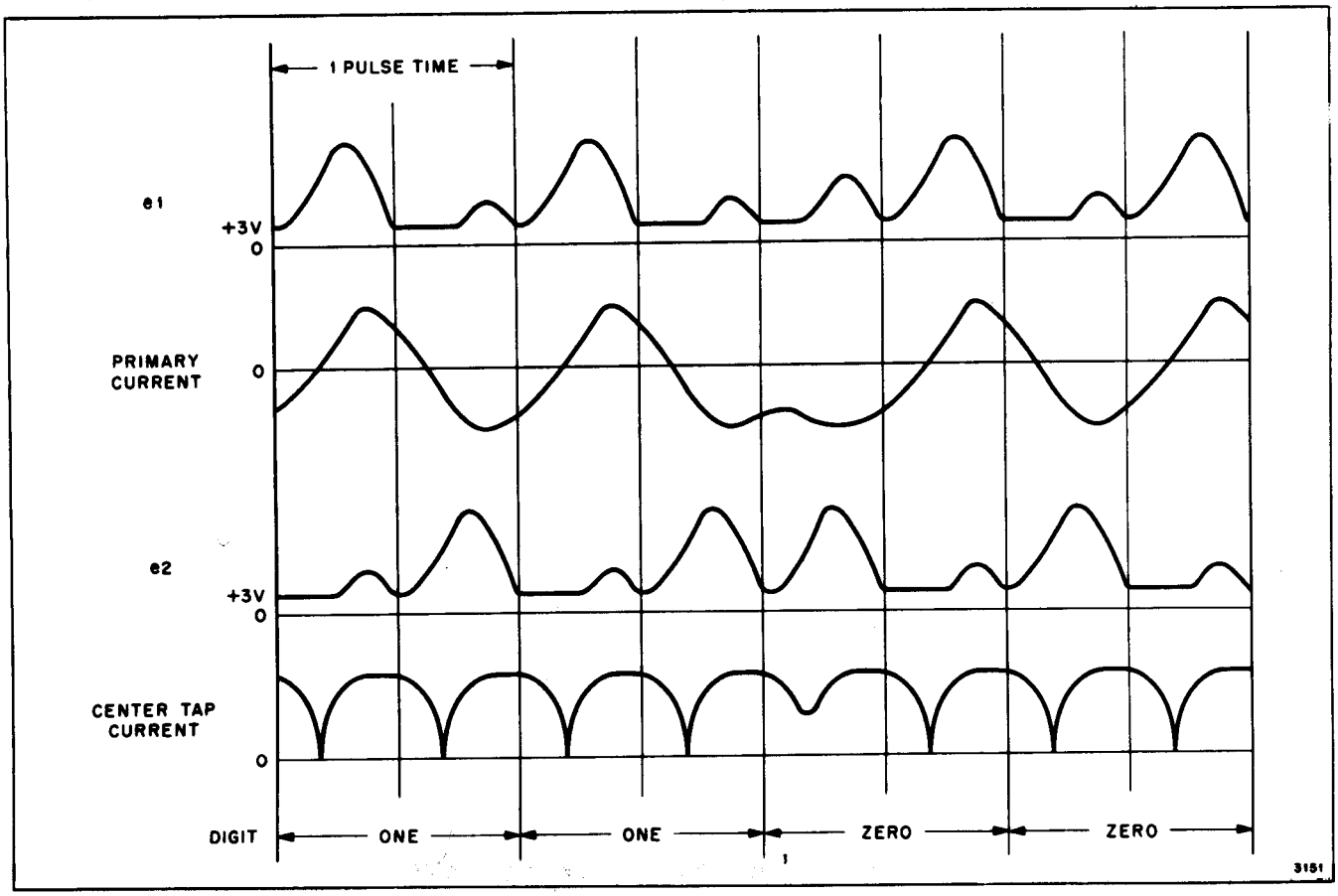


Figure 6-39. Write-Transformer Package Waveforms

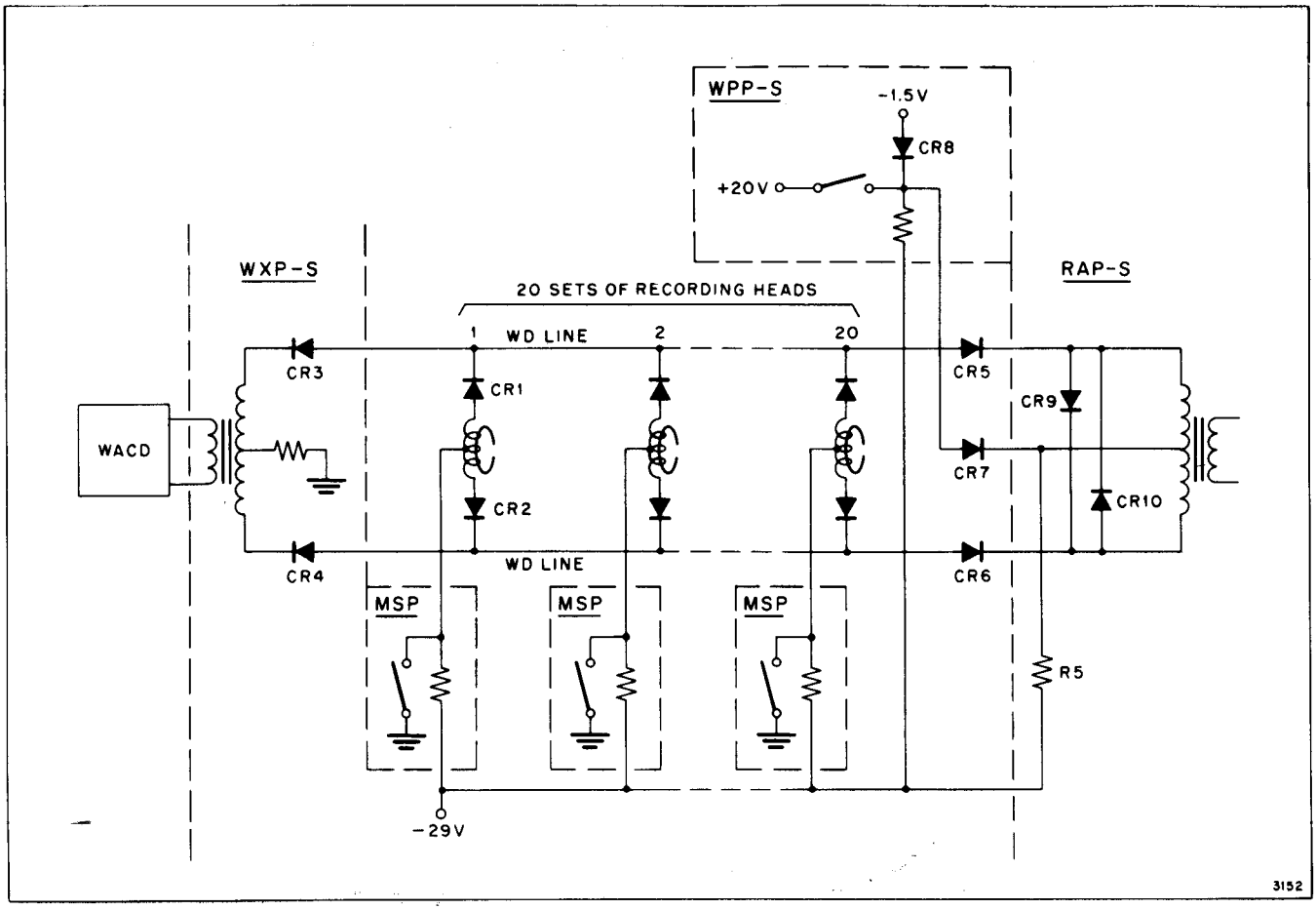


Figure 6-40. Read-Write Circuit Interconnections

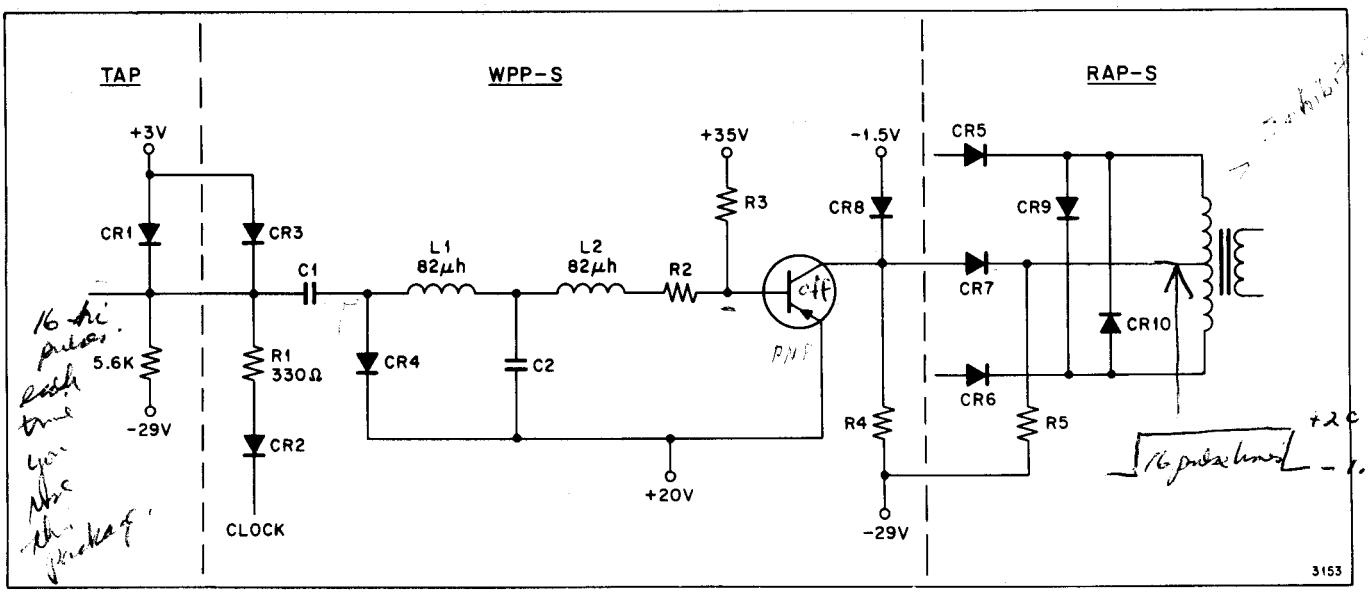


Figure 6-41. Write-Pedestal Circuit

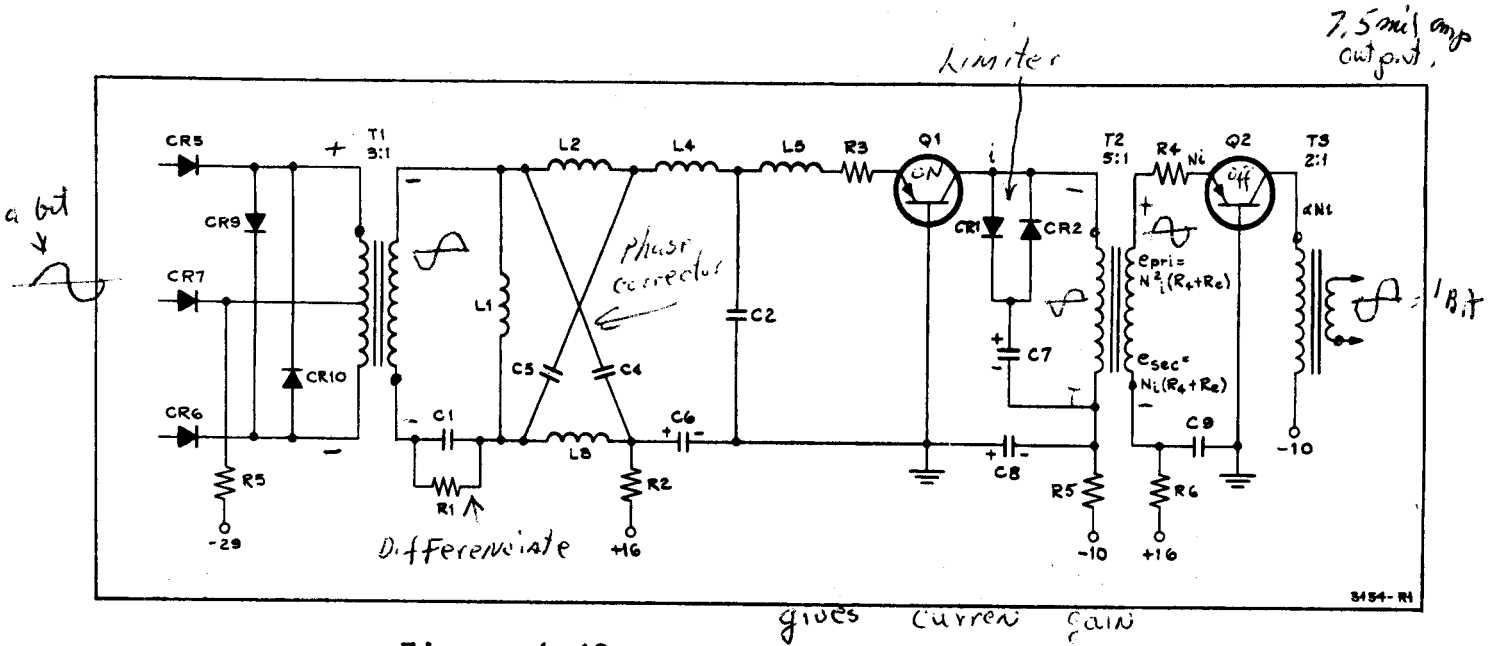


Figure 6-42. Read-Amplifier Circuit

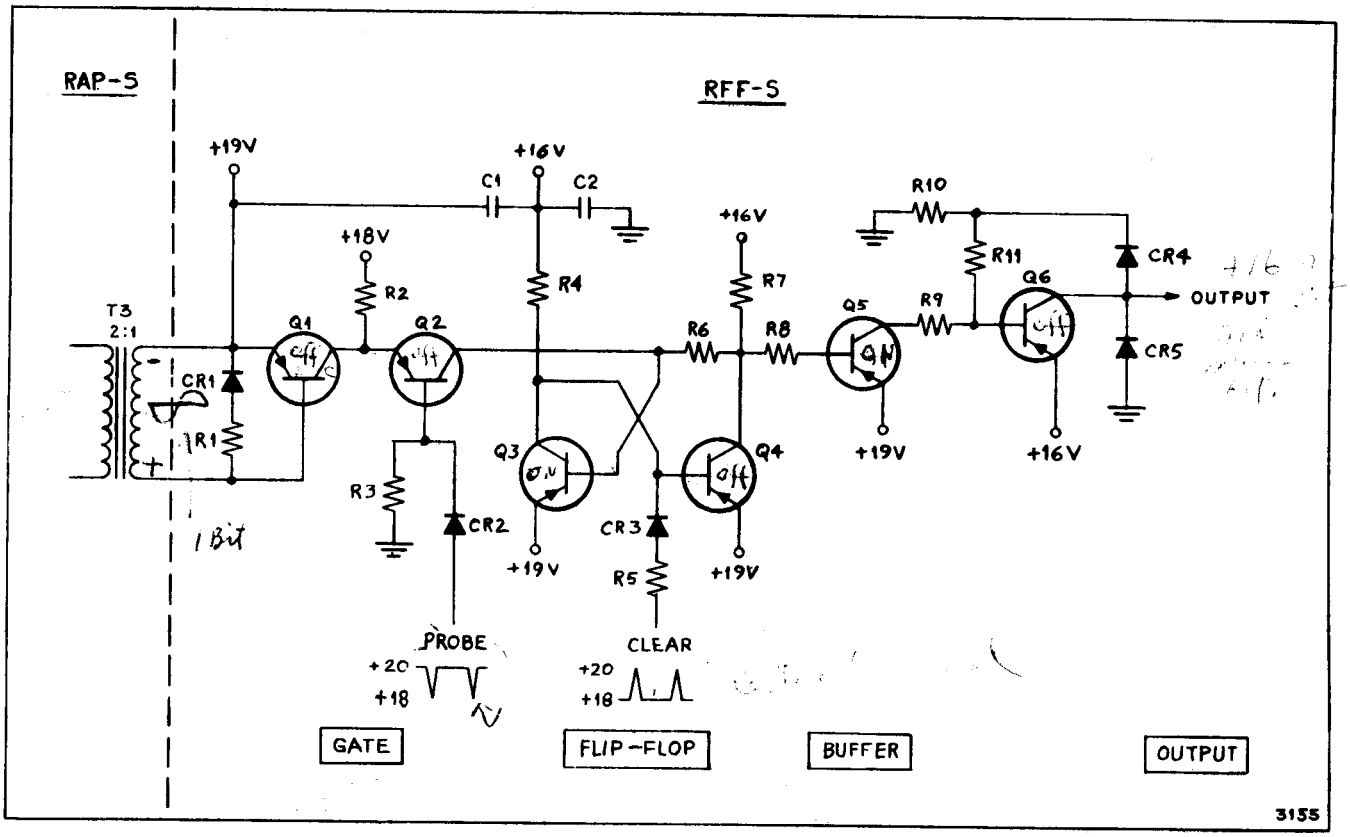


Figure 6-43. Read Flip-Flop Circuit

PBC Package

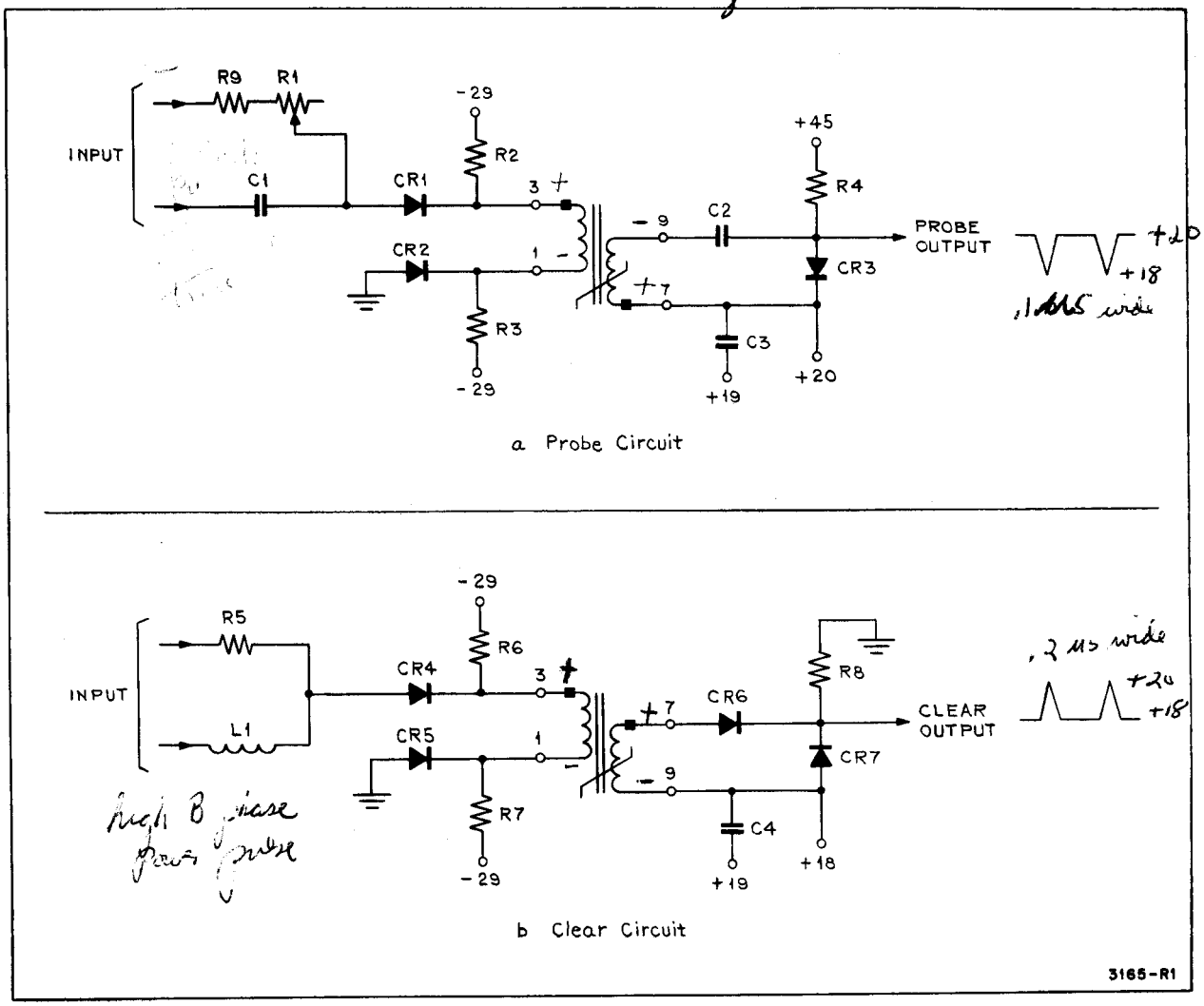


Figure 6-44. Probe and Clear Generator Circuits

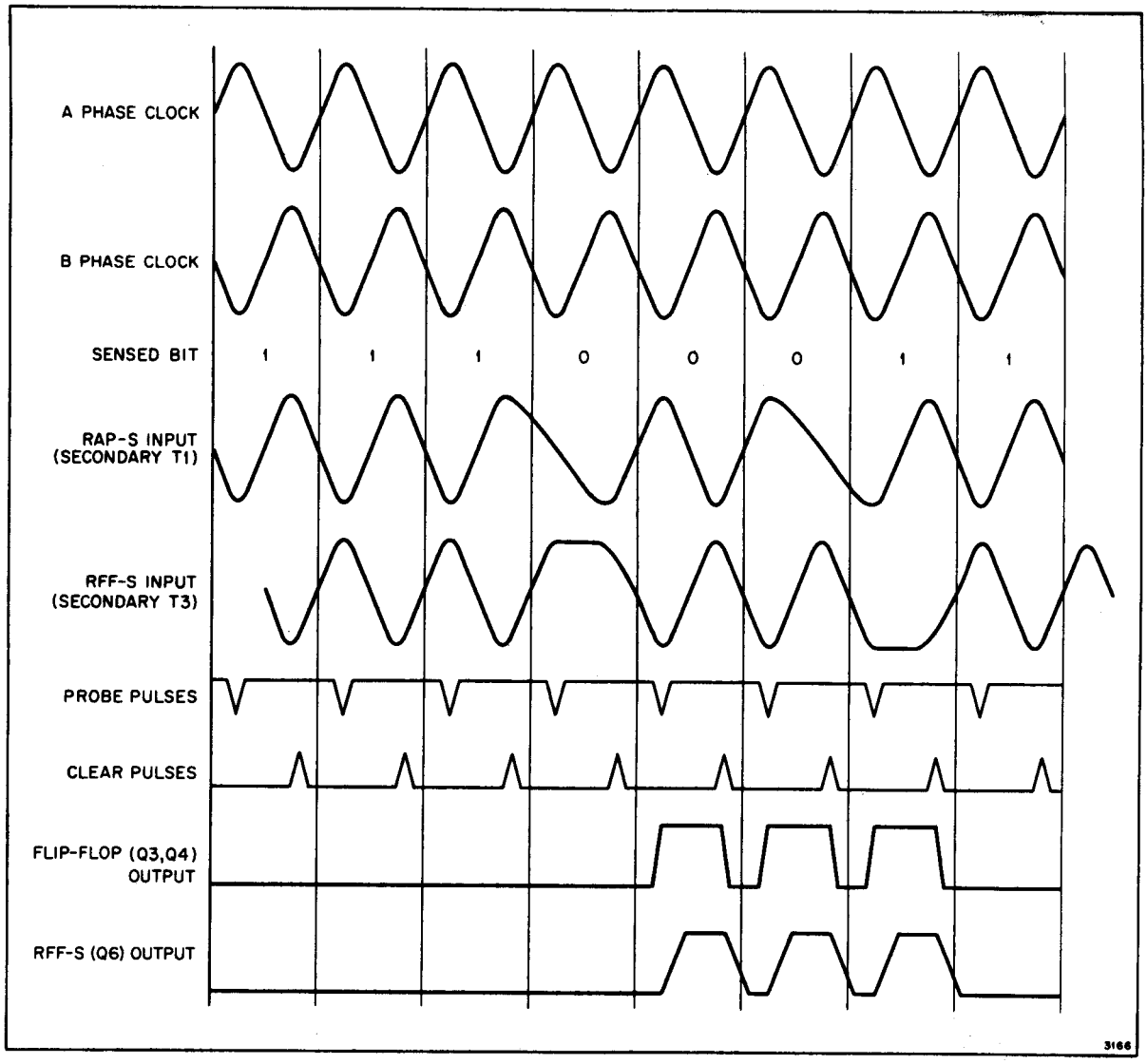


Figure 6-45. Read-Circuit Waveforms

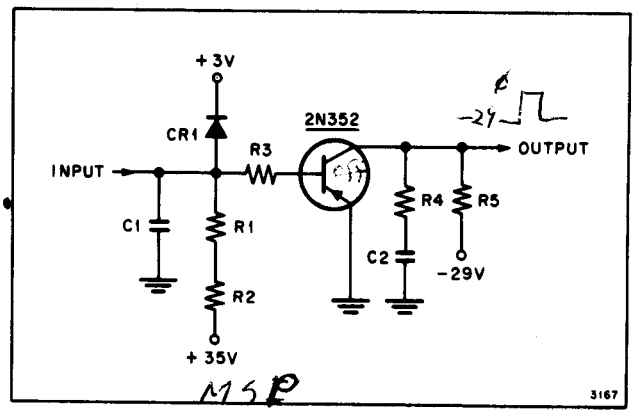


Figure 6-46. Matrix-Selector Circuit

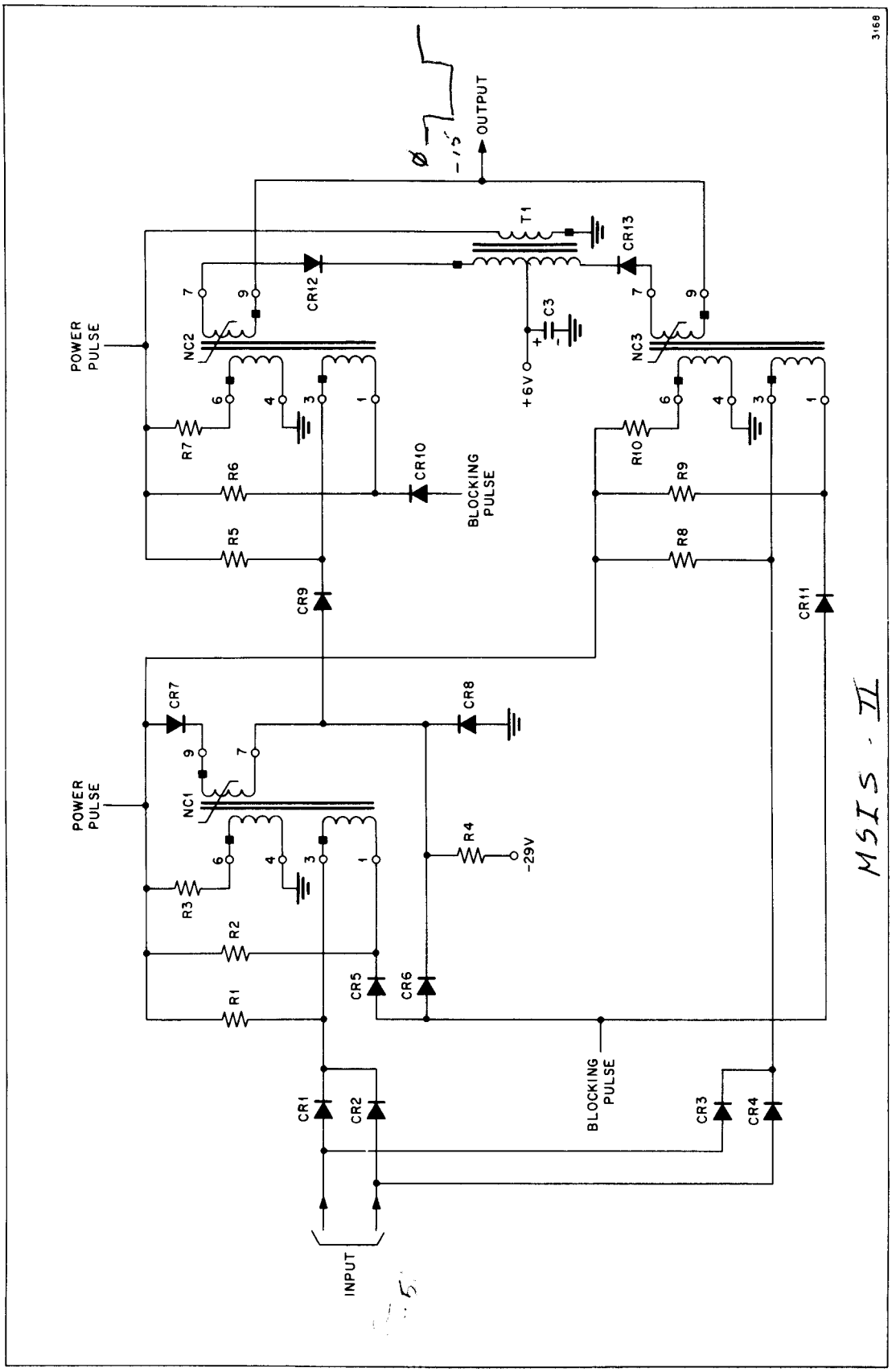


Figure 6-47. Switch-Driver Circuit

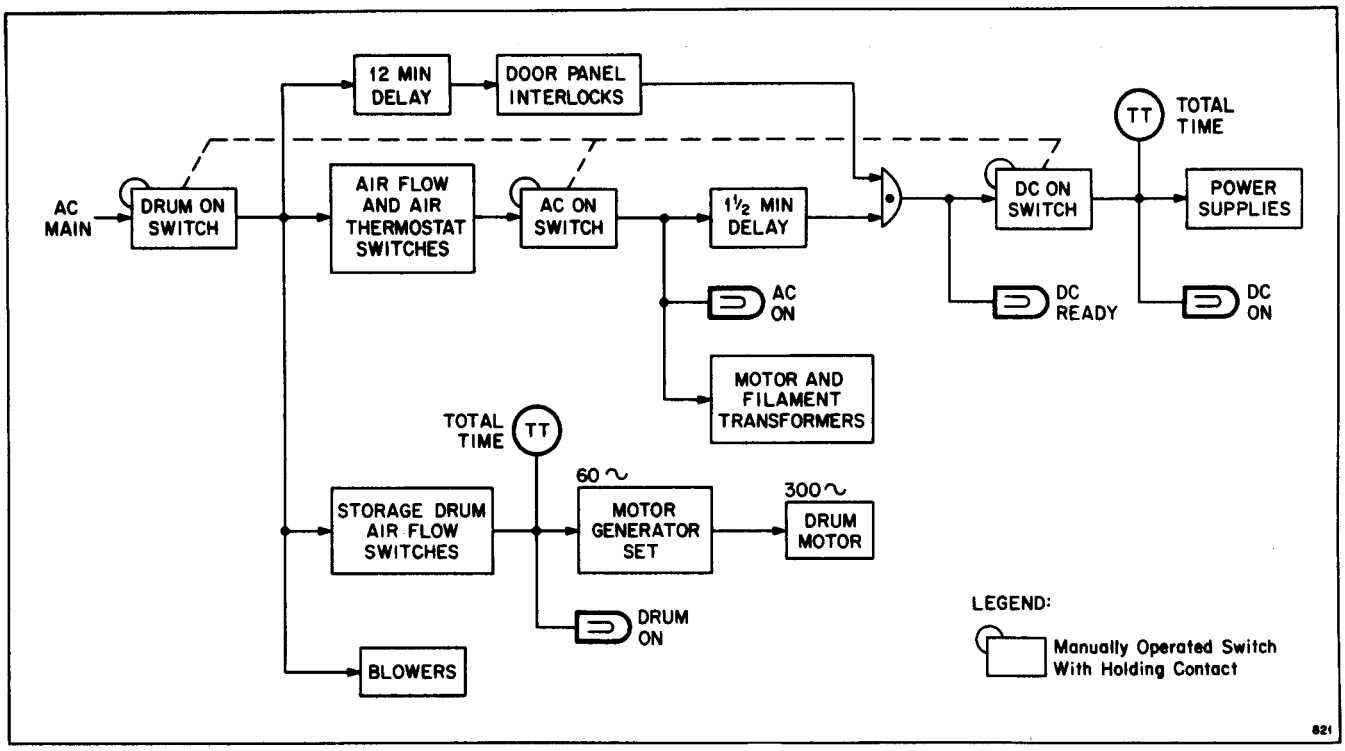


Figure 6-48. Power Control Circuits, Block Diagram

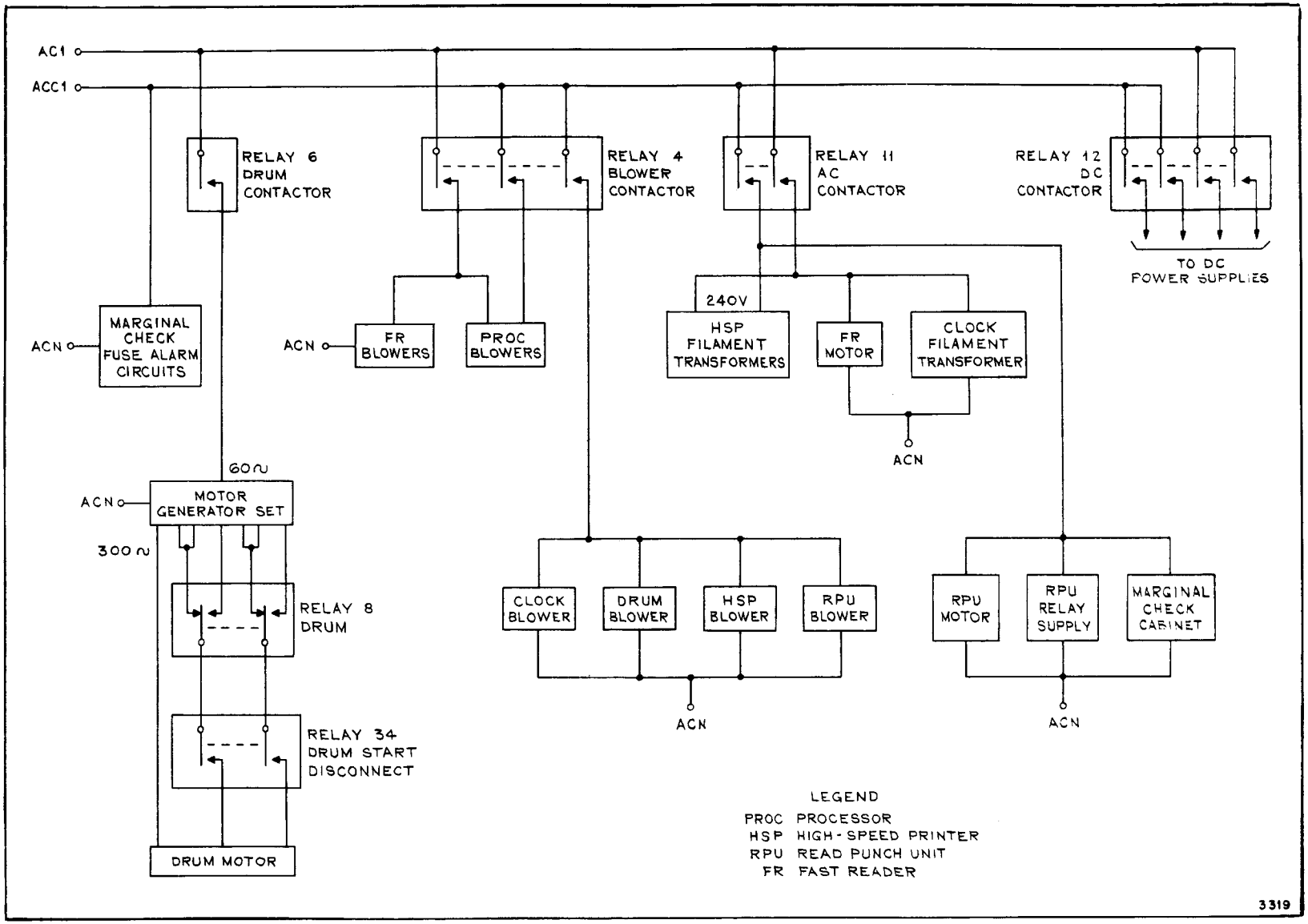
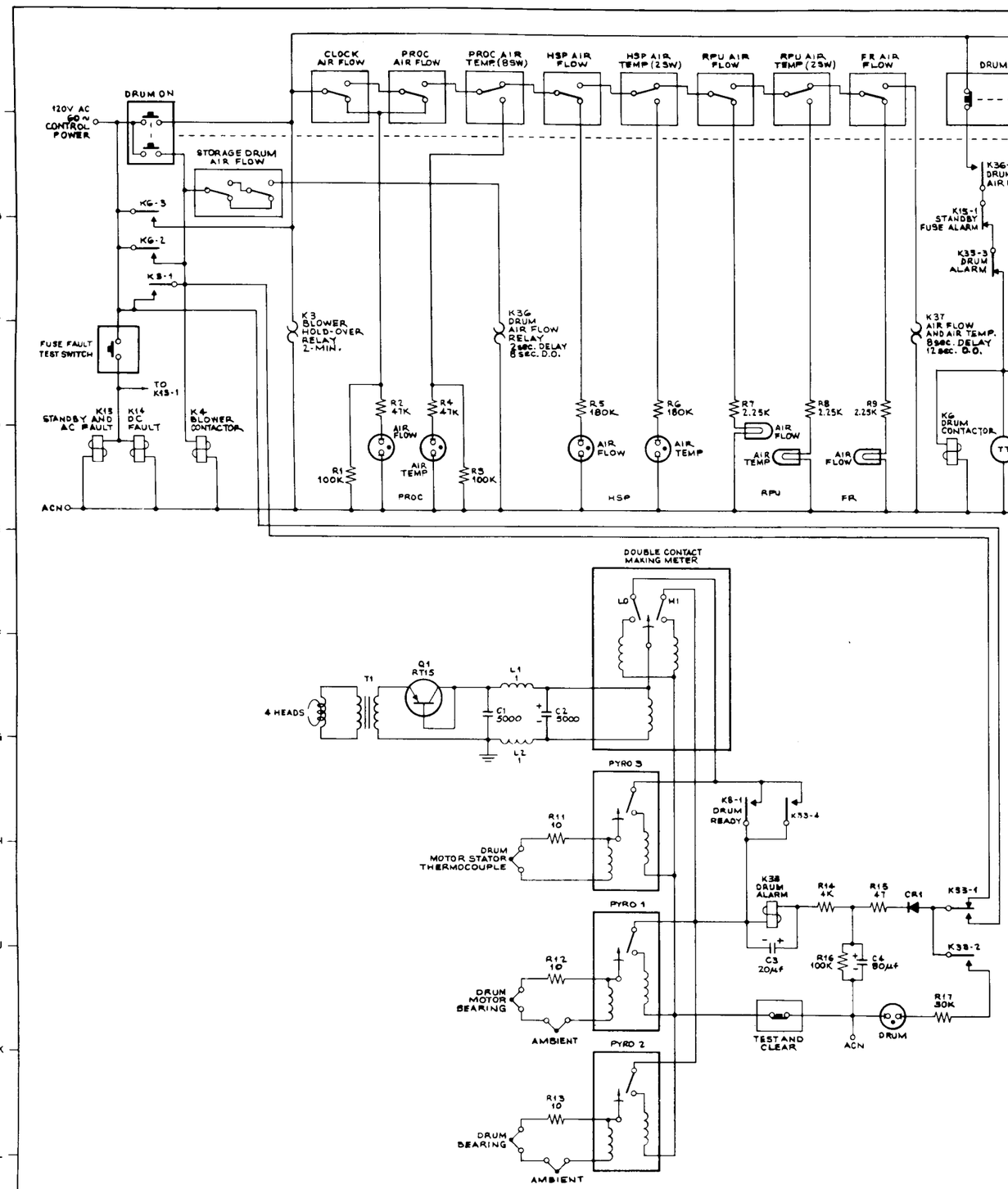


Figure 6-49. A-C Distribution Circuits, Block Diagram



RELAY COIL AND POLE LOCATI

RELAY NO.	COIL	P1	P2	P3
K3	C3	C1		
K4	D2	FIG.-6-49		
K6	D9	F13	B1	B1
K7	C11	B11		
K8	D11	H7	J15	J14
K9	B13	B12		
K10	B13	C14	B12	
K11	D12	FIG.-6-49	A12	
K12	D16	FIG.-6-49		
K13	D1	C17	B20	B20
K14	D1	C20	C20	D20
K15	A19	B10		
K16	B19	C12		
K17	C19	C16		
K18	D19	C16		
K30	D15	NS		NS
K32	A20	A16		
K33	J7	J9	J9	B9
K34	D10	J14	J15	
K36	C5	B10		
K37	C9	C12		

NS=NOT SHOWN

NOTES:
RESISTANCE IN OHMS,
CAPACITANCE IN MICROMICROFARADS,
INDUCTANCE IN MICROHENRIES,
UNLESS OTHERWISE NOTED.

Figure 6-50. Powe

PROC AIR FLOW
PROC AIR TEMP (BSW)
HSP AIR FLOW
HSP AIR TEMP (2SW)
RPU AIR FLOW
RPU AIR TEMP (2SW)
FR AIR FLOW
DRUM OFF
K36-1 DRUM AIR FLOW
K15-1 STANDBY FUSE ALARM
K33-3 DRUM ALARM
K3G DRUM AIR FLOW RELAY 2 sec DELAY 8 SEC. D.O.
K37 AIR FLOW AND AIR TEMP. 8 sec. DELAY 12 sec. D.O.
K7-1
K7 DRUM DELAY RELAY
K11-3
AC ON
AC OFF
K9 DC DELAY (1/2" MIN.
K10-2
ACN
K10 DC READY
K9-1
K10-1
K16-1 AC FUSE ALARM
K37-1 AIR FLOW AIR TEMP.
OVER-CURRENT RELAYS (3)
PROC INTERLOCK SWITCH
DC READY (8)
R22 1.25K
DC ON
DC OFF
K32-1
K12-5
6.3V AC
CLOCK ALARM BYPASS SWITCH
R24 22
CLOCK ALARM BYPASS
K32 CLOCK ALARM RELAY
CR4
A∅
B∅
CLOCK
CR5
K15 STANDBY ALARM
R29 47K
C7 8µf
K13-2
PROC STANDBY FUSE FAULT
K16 AC ALARM
R30 4.7K
C8 8µf
K13-3
PROC AC FUSE FAULT
K13-4
HSP AC FUSE FAULT
K17 +DC ALARM
R31 8.2K
K14-1
PROC +DC FUSE FAULT AND CLOCK OUTPUT TRANSFORMER
K14-2
HSP +DC FUSE FAULT
K18 -DC ALARM
R32 8.2K
K14-3
PROC -DC FUSE FAULT
K14-4
HSP -DC FUSE FAULT
K17-1 +DC FUSE ALARM
K18-1 -DC FUSE ALARM
TO FUSE FAULT TEST SWITCH
K13-1
CR2
CR3
R25 120
R28 120
K30 STORAGE WRITE INHIBIT
R23 2.25K
K12 DC CONTACTOR
C5 8µf
R26 100K
R27 100K
C6 8µf
HSP FUSE FAULT
PROC FUSE FAULT
R35 47K
R36 100K
R34 47K
R33 100K
R4 47K
R5 180K
R6 180K
R7 2.25K
R8 2.25K
R9 2.25K
AIR TEMP
AIR FLOW
PROC
HSP
RPU
FR
KG DRUM CONTACTOR
TT
K34 DRUM START DISCONNECT 5sec.
R10 2.25K
DRUM ON
K8 DRUM READY RELAY
K11 AC CONTACTOR
R18 100K
R19 47K
R21 47K
INTERLOCK
OVER-CURRENT
R20 100K

DOUBLE CONTACT MAKING METER
LO
HI
Q1 RT15
L1 1
C1 5000
C2 5000
L2 1
PYRO 3
PYRO 1
PYRO 2
R11 10
DRUM MOTOR STATOR THERMOCOUPLE
R12 10
DRUM MOTOR BEARING
AMBIENT
R13 10
DRUM BEARING
AMBIENT
K8-1 DRUM READY
K33-4
K38 DRUM ALARM
C3 20µf
R14 4K
R15 47
CR1
K33-1
K38-2
R16 100K
C4 60µf
TEST AND CLEAR
ACN
DRUM
R17 30K

AC1
KG-1
R38 47K
R37 100
ACN
ALTERNATOR DRIVE MOTOR
ACN
MOT
G
DRUM ALTERNATOR 300~
K8-3
K8-2
T2
T3
K34-1
K34-2
T3 SEC
T3 SEC
MOT
DRUM MOTOR

RELAY COIL AND POLE LOCATIONS

RELAY NO.	COIL	P1	P2	P3	P4	P5
K3	C3	C1				
K4	D2	FIG.-G-49				
K6	D9	F13	B1	B1		
K7	C11	B11				
K8	D11	H7	J15	J14		
K9	B13	B12				
K10	B13	C14	B12			
K11	D12	FIG.-G-49		A12		
K12	D16	FIG.-G-49				A17
K13	D1	C17	B20	B20	C20	
K14	D1	C20	C20	D20	E20	
K15	A19	B10				
K16	B19	C12				
K17	C19	C16				
K18	D19	C16				
K30	D15	NS		NS	NS	
K32	A20	A16				
K33	J7	J9	J9	B9	H7	
K34	D10	J14	J15			
K36	C5	B10				
K37	C9	C12				

NS=NOT SHOWN

NOTES:
RESISTANCE IN OHMS,
CAPACITANCE IN MICROMICROFARADS,
INDUCTANCE IN MICROHENRIES,
UNLESS OTHERWISE NOTED.

4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23

3318

Figure 6-50. Power Control Circuits, Schematic

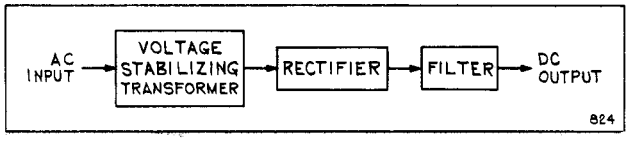


Figure 6-51. Typical Power Supply, Block Diagram

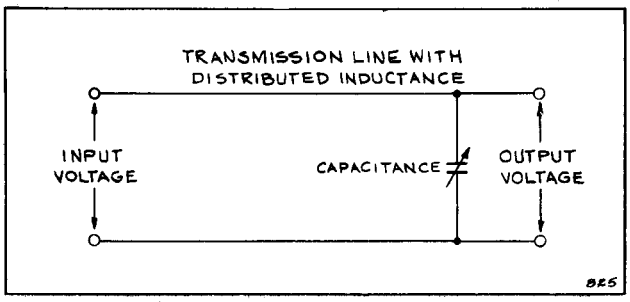


Figure 6-52. Holding Up Circuit

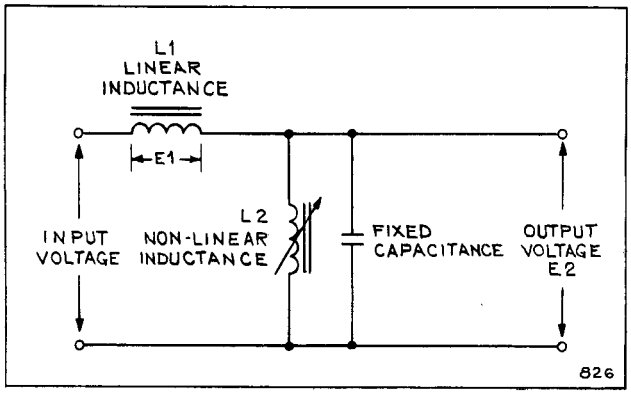


Figure 5-53. VST Equivalent Circuit

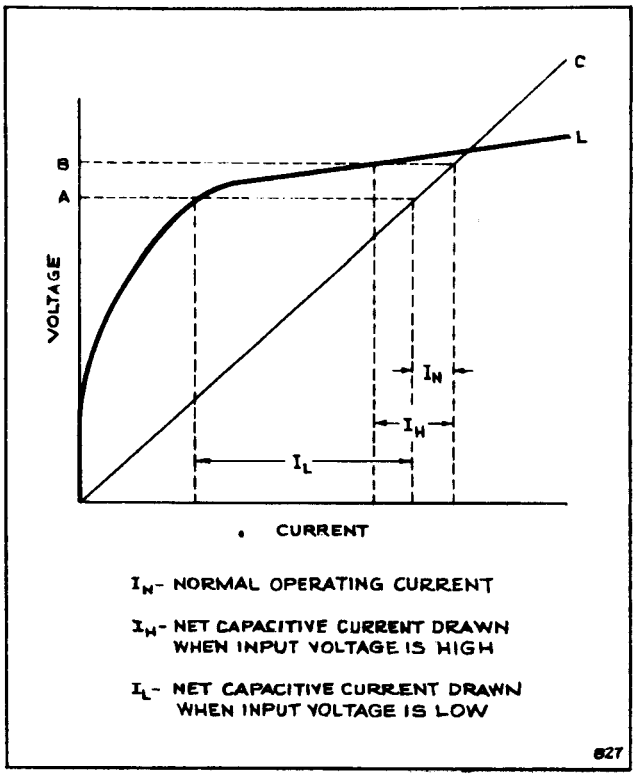


Figure 6-54. Circuit Characteristic Curve

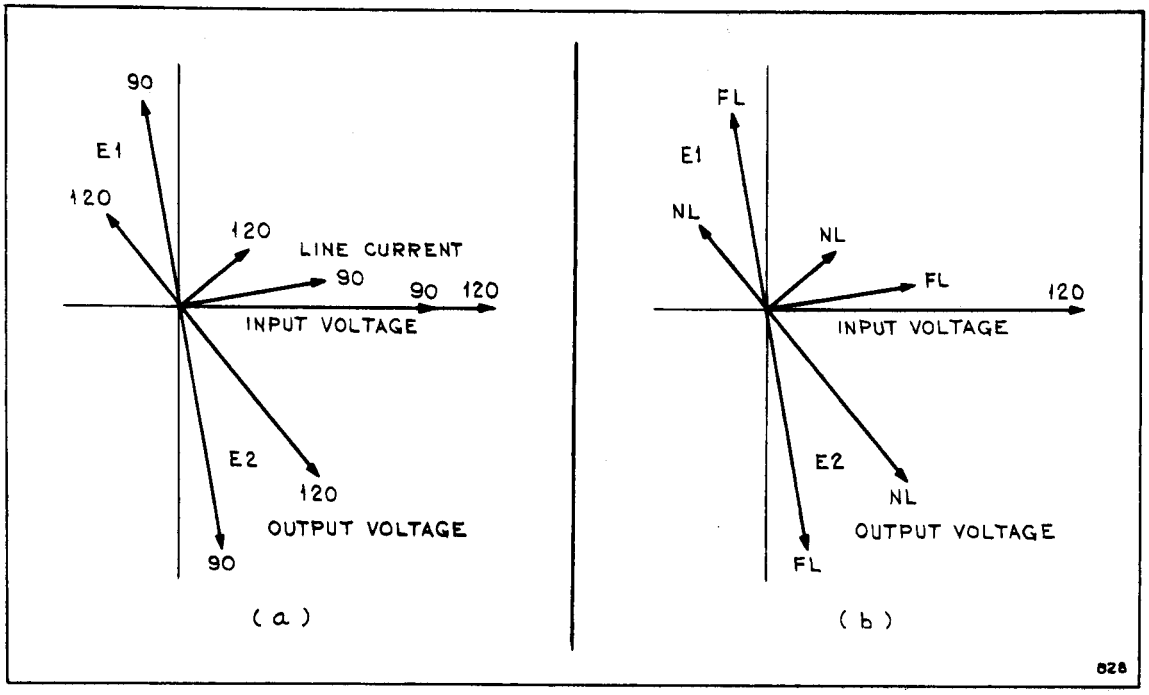


Figure 6-55. Phase Relationships

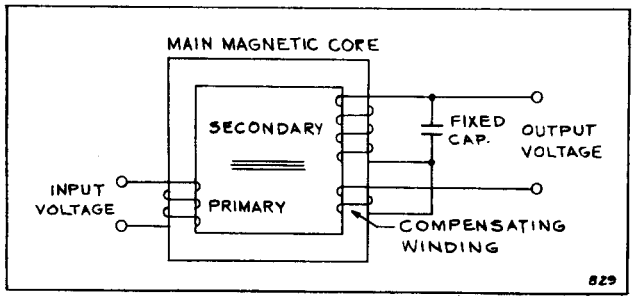


Figure 6-56. Basic Voltage-Stabilizing Transformer

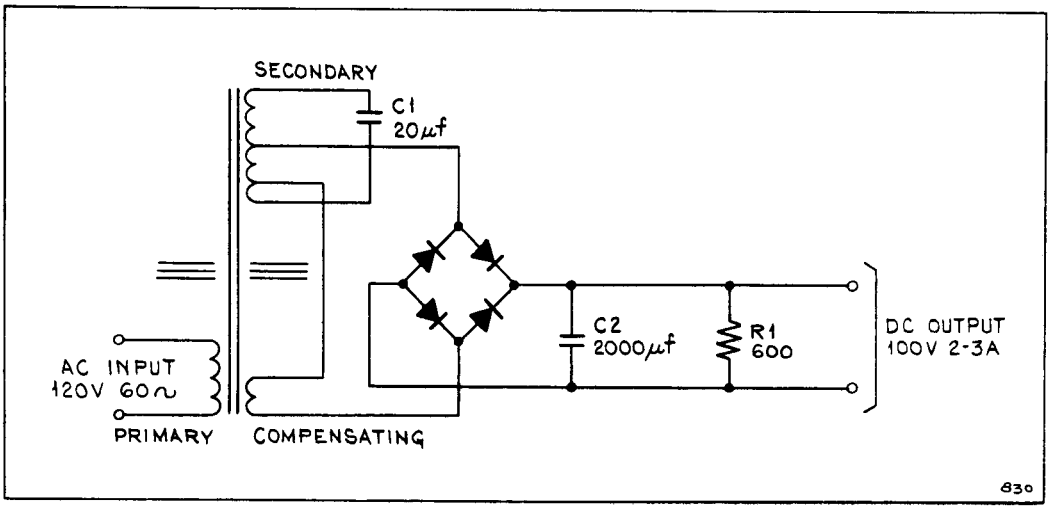


Figure 6-57. D-C Supply, 100 Volts

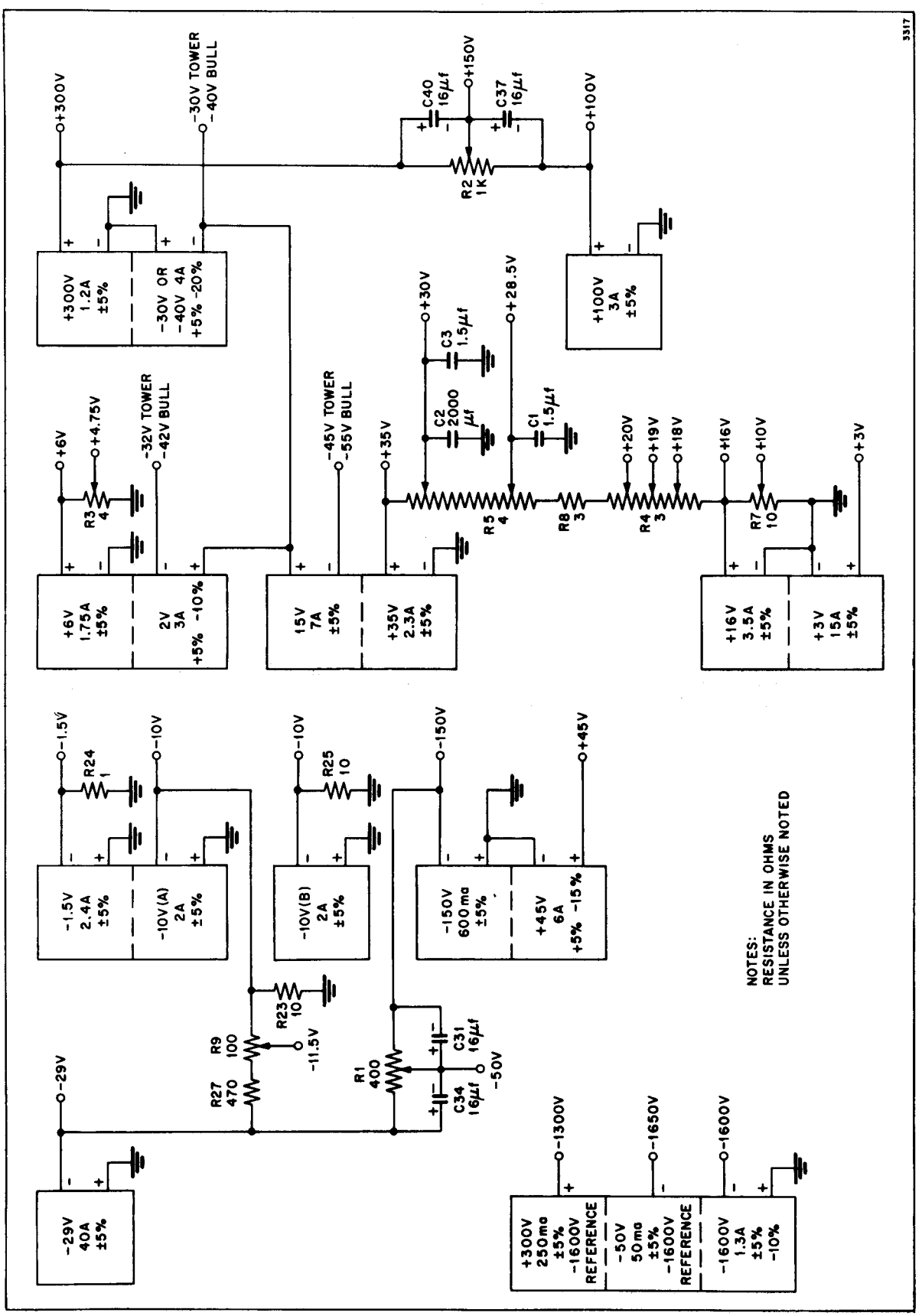
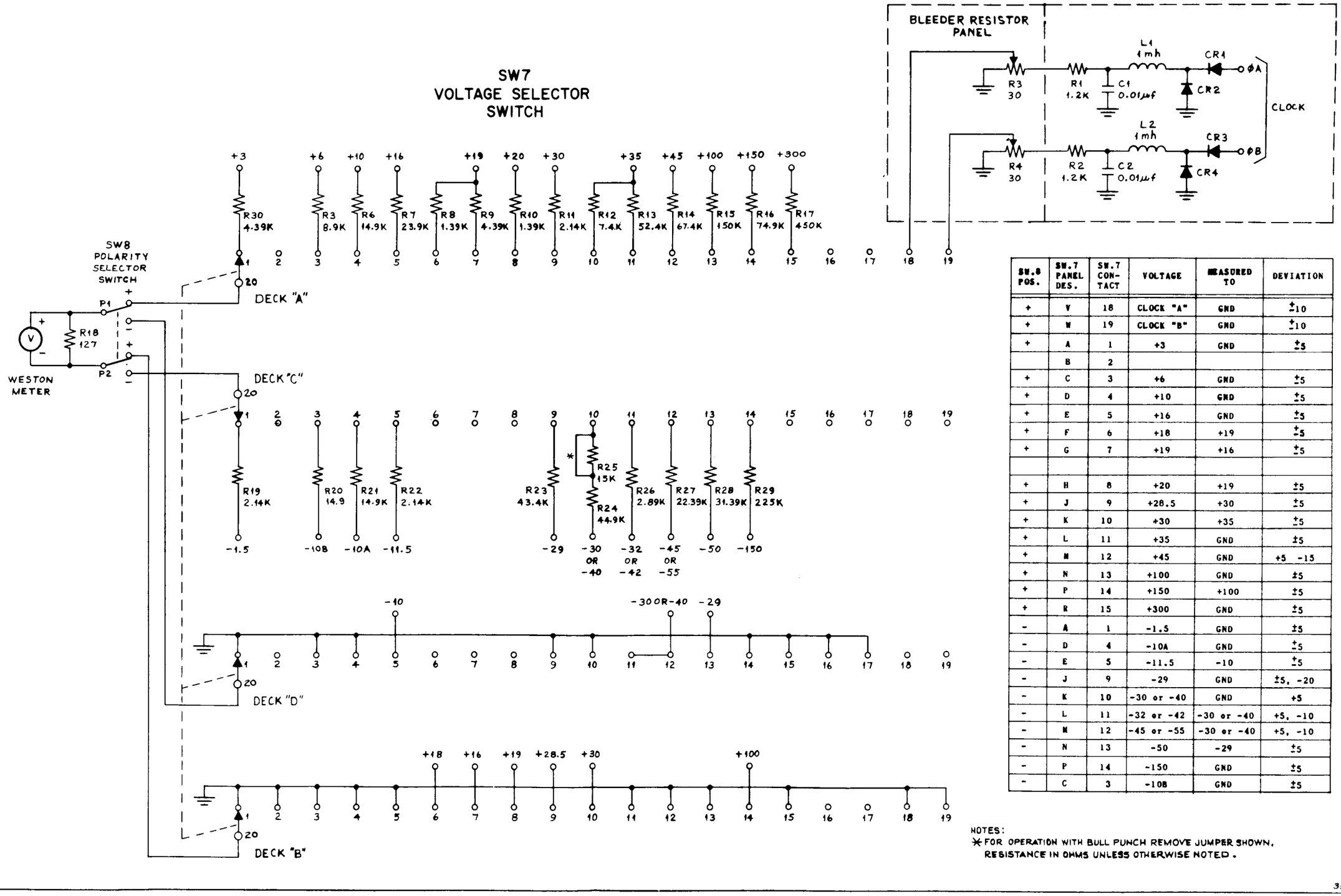


Figure 6-58. D-C Supplies, Block Diagram



SW.6 POS.	SW.7 PANEL DES.	SW.7 CONTACT	VOLTAGE	MEASURED TO	DEVIATION
+	V	18	CLOCK "A"	GND	±10
+	W	19	CLOCK "B"	GND	±10
+	A	1	+3	GND	±5
	B	2			
+	C	3	+6	GND	±5
+	D	4	+10	GND	±5
+	E	5	+16	GND	±5
+	F	6	+18	+19	±5
+	G	7	+19	+16	±5
+	H	8	+20	+19	±5
+	J	9	+28.5	+30	±5
+	K	10	+30	+35	±5
+	L	11	+35	GND	±5
+	M	12	+45	GND	+5 -15
+	N	13	+100	GND	±5
+	P	14	+150	+100	±5
+	R	15	+300	GND	±5
-	A	1	-1.5	GND	±5
-	D	4	-10A	GND	±5
-	E	5	-11.5	-10	±5
-	J	9	-29	GND	±5, -20
-	K	10	-30 or -40	GND	+5
-	L	11	-32 or -42	-30 or -40	+5, -10
-	M	12	-45 or -55	-30 or -40	+5, -10
-	N	13	-50	-29	±5
-	P	14	-150	GND	±5
-	C	3	-10B	GND	±5

NOTES:
* FOR OPERATION WITH BULL PUNCH REMOVE JUMPER SHOWN.
RESISTANCE IN OHMS UNLESS OTHERWISE NOTED.

Figure 6-59. Voltage Monitor Circuit

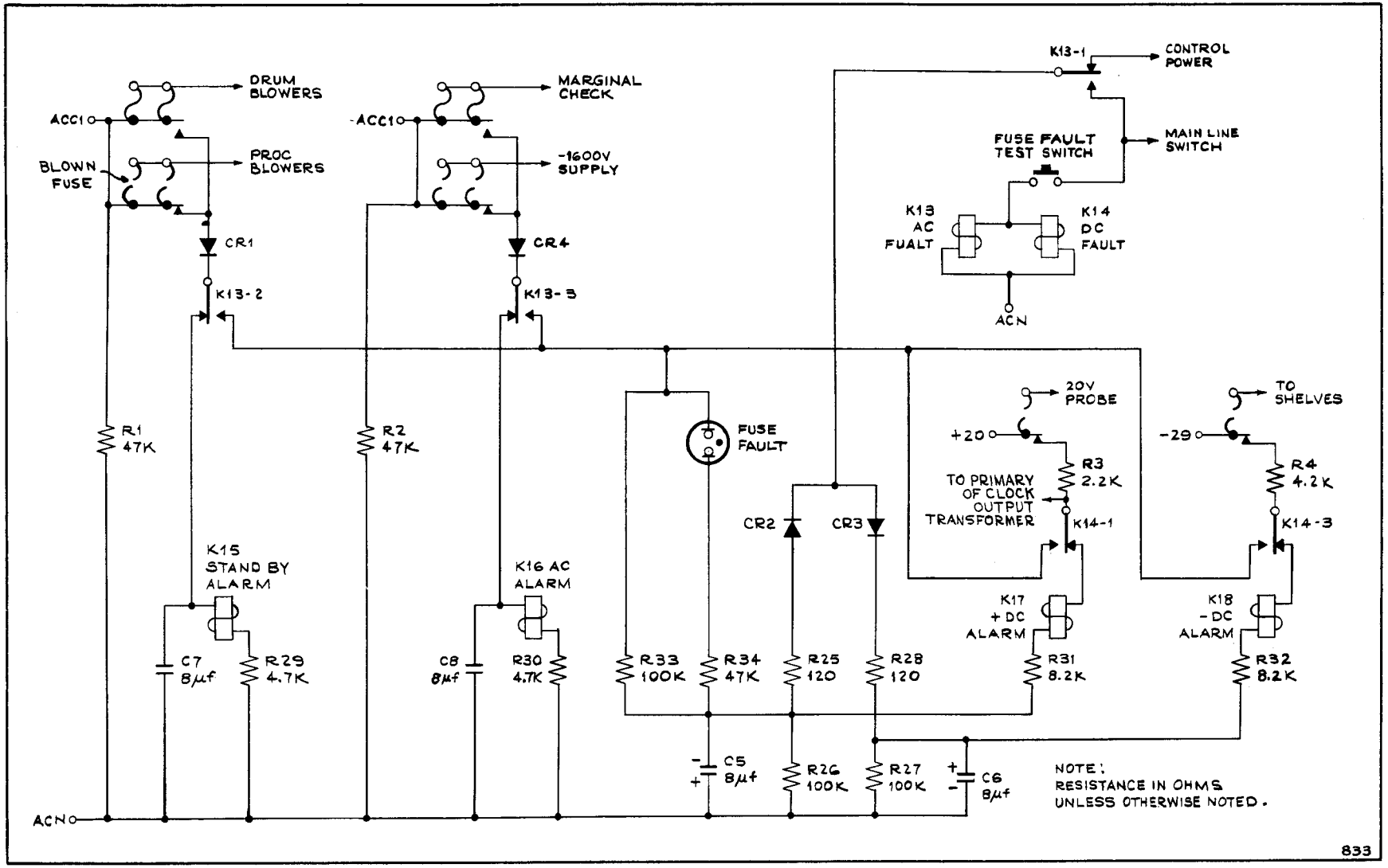


Figure 6-60. Typical Fuse Fault Circuit

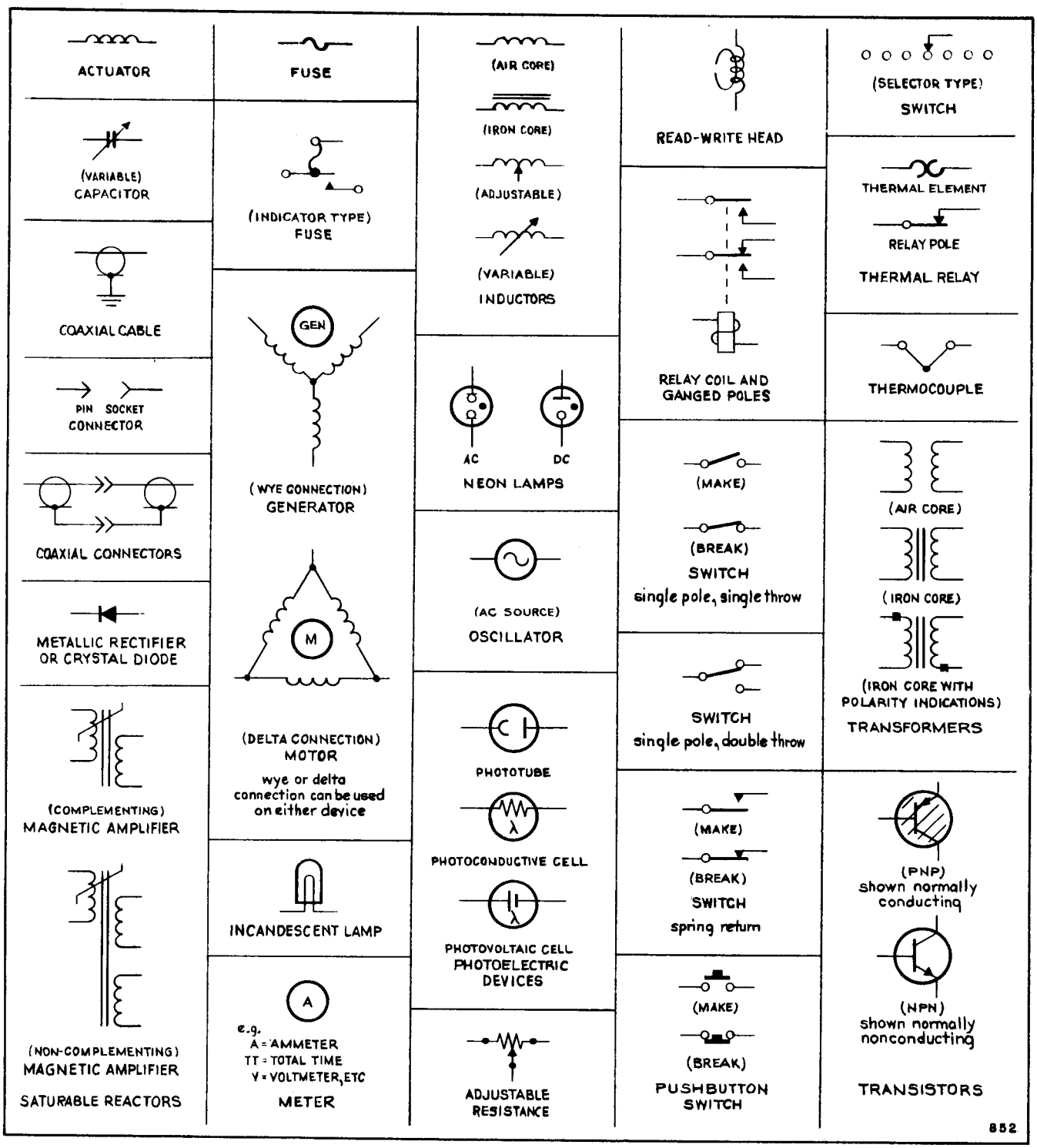


Figure 6-61. Standard Symbols

Appendix A, Logical Block Diagrams, is bound separately.

Table B-1. Control and Information Signals

The number of the appropriate logical block diagram in Appendix A is given in parenthesis after the source of each signal.

Signal	Source	Function
A $\overline{A}$	Outputs of binary-carry circuit (A12)	Indicates binary carry.
A' $\overline{A'}$	Outputs of binary-carry circuit (A12)	A' indicates true binary carry. $\overline{A'}$ used in storage selection.
A+ (plus) A- (minus)	Outputs of rA sign FF (A13)	Indicates sign of word in rA.
A1 A2 A3 A4	Normal recirculation outputs of rA (A8)	
A1' A2' A3' A4'	Outputs of rA during right shift (A8)	Carry information to rA through right-shift gates and to rX through circular-shift gates. Carry unprimed word stored in rA to be written into print-buffer band I before printing. Carry information in rA to M buffers when rA is addressed instead of main storage.
A"4 $\overline{A"4}$	Lengthened outputs of A4 subregister of rA during left shift (A8)	
A11 A21 A31 A41	Normal outputs of rA to S buffers (A8)	
A1OD A2OD A3OD A4OD	Display outputs of rA (A8) OD = output display	

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
A1M A2M A3M A4M	Early outputs of rA to M buffers (p0 = t7B) for writing contents of rA into main storage (A8)	
AOP	Output of abnormal-operation-printer FF (A35)	Sent to I/O abnormal-condition FF in static register.
AOR $\overline{\text{AOR}}$	Output of abnormal-operation-reader FF (A25)	Sent to I/O abnormal-condition FF in static register. Barred signal goes to ending pulse circuit.
AOT	Output of abnormal-operation-read-punch FF (A26)	Sent to I/O abnormal-condition FF in static register.
B1 $\overline{\text{B1}}$ B2 $\overline{\text{B2}}$ B3 $\overline{\text{B3}}$ B4 $\overline{\text{B4}}$	Outputs of print-buffer band I (A29)	To print comparator and to print-buffer error FF. Barred signals feed back into print-buffer band I.
B5 $\overline{\text{B5}}$ B6 $\overline{\text{B6}}$ B7 $\overline{\text{B7}}$ $\overline{\text{B8}}$	Outputs of print-buffer band II (A30)	B5, $\overline{\text{B5}}$, B6, and $\overline{\text{B6}}$ sent to print comparator. B5, $\overline{\text{B5}}$, B6, $\overline{\text{B6}}$, B7, and $\overline{\text{B7}}$ sent to print-buffer error FF. Barred signals feed back into print-buffer band II.
Bias check	Output from printer to print control (A35)	Signal indicates state of bias on print thyratrons. If no bias, charge-check FF generates a charge-check-extinguish signal and a signal to pick up charge relay.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
BL1 $\overline{\text{BL1}}$	Outputs of BL1 FF which indicate card buffer is loaded from card reader and 96 instruction (transfer to main storage) may be given (A24) BL = buffer loaded	BL1 alerts STR stepping gate 10 during 96 instruction and stepping gate 108 during 42 instruction. $\overline{\text{BL1}}$ alerts STR ending-pulse gate 113 during 42 instruction. BL1 alerts set gate of card-cycle error FF.
BL2 $\overline{\text{BL2}}$	Outputs of BL2 FF which indicate card buffer is loaded from read punch and 46 instruction (transfer to main storage) may be given (A26)	BL2 alerts STR stepping gate 107 during 46 instructions. $\overline{\text{BL2}}$ alerts STR ending-pulse gate 16 during 22 instruction.
Block RD1 Block RD2	Outputs of block-read 1 and block-read 2 FF's during search for register address (A2)	Block setting of read FF for main storage so that information is read from registers and not storage. Low Block RD1 alerts input gate 40 of M buffers to minus sign of register L and alerts gate to generate FS 66. Low Block RD2 alerts input gates 114, 115, 116, 117, and 42 of M buffers to contents and sign of register A.
BLPR	Generated by FS 42A during writing into print buffer (A29)	Blocks read amplifiers of print buffer.
BLRE1	Low output generated when read FF of card-buffer band I is set. When high, blocks reading (A22)	Blocks read amplifiers of card-buffer band I during writing.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
BLRE2	Low output generated when read FF of card-buffer band II is set. When high, blocks reading (A23)	Blocks read amplifiers of card-buffer band II during writing.
$\overline{\text{BRD1}}$ $\overline{\text{BRD2}}$	Outputs of block-read 1 and block-read 2 FF's during search for register address (A2)	$\overline{\text{BRD1}}$ gates contents and sign of rA onto M lines. $\overline{\text{BRD2}}$ gates sign of rL onto M lines and alerts gate to generate FS 66. $\overline{\text{BRD1}}$ and $\overline{\text{BRD2}}$ gate sign of rX onto M lines, set TS FF, and generate FS 17'.
Brush storage loaded	Signal from card-reader brush-loaded circuits (A24)	Indicates that 90 bits (one row of punched information) is stored in the capacitors. Alerts set gate of card-cycle error FF.
C $\overline{\text{C}}$	Output of force-decimal-carry circuit, initial force-decimal carry circuit, and quinary comparator (A12)	C signal used with A signal whenever decimal carry is needed. A = binary carry C = quinary carry A and C = decimal carry. Also used in storage selection.
C'	Output of quinary comparator (A12)	Sent to quinary adder to indicate true quinary carry.
C1 C2 C3 C4	Outputs from card-buffer band I (A22)	Sent to M buffers for writing into main storage. Also sent to read-punch shift register during punch setup.
C1A	Output of paper-feed FF (A35)	Puts high on input buffer of charge-control FF.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
C11 C21 C31 C41	Outputs of rC when CT FF is set (A1)	Reads m address from rC to S buffers for storage search.
C12 C22 C32 C42	Outputs of rC when CT FF is restored (A1)	Reads c address from rC to S buffers for storage search.
C13 C23 C33 C14 C24 C34	Continuous outputs of rC (A1)	
(To) card feed controls	Generated if either or both registration-check FF's for read stations are set to indicate an error (A25)	Stops motor.
Card jam	Input from read-punch circuits (A26)	Sets RPU abnormal-operation FF.
Card jam	Input from card-reader circuits (A25)	Sets card-reader abnormal-operation FF.
Carriage out	Input from printer to indicate that carriage is not in correct position for printing (A35)	Sets printer abnormal-operation FF.
CB1 $\overline{CB1}$ CB2 $\overline{CB2}$ CB3 $\overline{CB3}$ CB4 $\overline{CB4}$ CB5 $\overline{CB5}$ CB6 $\overline{CB6}$ CB7 $\overline{CB7}$	Outputs of print-comparator final-storage FF's (A33)	
CCC2 CCC3 CCC4 CCC5	Outputs of card-cycle counter for card reader (A24)	Sent to two registration-check FF's for both read stations.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
CCEA CCEB	Output from charge-check-extinguish FF (A35) CCE = charge-check extinguish	CCEA sets abnormal-operation-printer FF. CCEB blocks generation of PC or PC' signals to disconnect print thyratrons and deenergizes charge relay.
CCF	Output from one charge-check FF (A35) CCF = charge check fire	Sets printer abnormal-operation FF.
CCT	Generated by INT1 and FS 28 during 72 instruction if the previous 72 instruction has not been accepted (A4)	Generates JAM I2B and FS 64.
CG1 CG2 CG3 CG4 CG5 CG6 CG7	Low signals from code generator wheel inverted to highs for checking (A33) CG = code generator	Sets print-code error FF when printing if odd signal present.
Charge	Input from printer (A35)	Indicates whether capacitors are charging. If they are charging when they should not, generates CCE. If they are not charging when they should, generates CCF.
(To) charge control circuits	Generated when FS 42A is present or when paper-feed FF is set (A35)	Charges capacitors used during printing.
(To) charge relay	Output from one charge-check FF (A35)	Deenergizes relay.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
CK $\overline{CK}$ CK1 CK2 CK3 CK4 CK5 CK6 CK7 CK8	Outputs of check-bit computer (A19)	
CLC	Output of RPU drum-revolution counter when counter reads 3 (A26) CLC = clear counter	Clears read-punch (TG) column counter.
Clear cap.	Output of read-punch clear-cap. FF (A26)	Clears 90-capacitor storage.
Clear cntr	Signal from photocell disc timer on card reader (A24) cntr = counter	Indicates gap on photo-cell disc timer.
CL1A	Output from keyboard-alert switch (A5)	Clears four shift registers used during keyboard input.
CLP	Generated on first drum revolution of main storage to print-buffer transfer (A35) CLP = clear print counter	Clears print counter.
CLQ	Generated during multiplication, division, and staticize step (A14)	Clears multiplier-quotient counter (MQC)
CLSR	Generated at end of punch setup (A28)	Clears read-punch shift register and drum-revolution counter and sets go flip-flop.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
Code gen 1 Code gen 2 Code gen 3 Code gen 4 Code gen 5 Code gen 6 Code gen 7	Inputs from code-generator wheel on printer (A33)	Indicates card code for character moving into print position.
Column drive reset	Output of column-drive-reset FF to read-punch circuits (A27)	Generated on third drum revolution of punch setup for each row when Q5 and Q6 sentinels and CTR-3 signal are present.
CP $\overline{CP}$	Outputs of complement FF (A13)	Controls comparator and quinary adder.
CP1 CP2 CP3 CP4 CP5	Single-pulse outputs of five set gates of complement FF (A13)	Generates initial decimal carry in comparator.
CPF	Generated by depressing the GENERAL CLEAR switch on the operator's control panel (A5)	Resets the paper-feed error relay.
CRC	Single-pulse output of punch setup FF (A26)	Restores RPU field FF, sets read-punch row counter to one, sets RPU drum-revolution counter to two, and initially sets the column-drive-reset FF.
CRD	Single-pulse output of punch-setup FF (A26)	Restores RPU drum-revolution counter and clears read-punch row counter.
CRE	Single-pulse output of punch-setup FF (A26)	Restores RPU drum-revolution counter and clears read-punch row counter.
CT $\overline{CT}$	Outputs of conditional-transfer FF (A12)	Controls readout of correct address from rC and band-selection flip-flops.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
CTR-2	Output of RPU drum-revolution counter when the counter reads 2 (A26)	Alerts set gate of the column-drive-reset FF if column drivers are to be set early.
CTR-3	Output of RPU drum-revolution counter when counter reads 3 (A26)	Steps row counter when X sentinel is also present. One signal necessary to end punch setup and to set column-drive-reset FF.
CUE	Output from cycling-unit error FF (A16)	Sets stop FF.
DEA	Output from divide-end circuit when switch on engineering panel is closed (A15) DEA = divide end, A phase	Sets D3 FF and jams STR FF5 to one to create an undecodable combination.
DEB	Output from divide-end circuit when switch on engineering panel is closed (A15) DEB = divide end, B phase	Restores OR FF.
DI	Single-pulse output from overflow FF if improper division is attempted (dividend larger than divisor) (A13)	Generates ending pulse and sets overflow FF so that next address will be c+1.
DM1' DM2' DM3' DM4'	Outputs from normal storage during reading (A19)	Information signals sent to M buffers for distribution.
DM5	Check-bit read from normal storage (A19)	Read into rX to compute new check bit for word to be printed.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
DM11 DM21 DM31 DM41	Outputs of four DM gates when word-release switch is closed (A5)	Word stored temporarily in four shift registers during keyboard input is sent to M buffers and then to rA, rX, rL, or rC.
DM15 DM25 DM35 DM45	Outputs from fast storage during reading (A20)	Information signals sent to M buffers for distribution.
DM55	Check-bit read from fast storage (A20)	Used at set gates of memory-check FF.
EC	Output of energize-capacitors FF for read punch (A26)	Alerts gates which produce TR'1 through TR'12 signals by combining TR1 through TR6 signals from row counter with UF' and LF' signals. These signals transfer information from switches into capacitor storage.
EF1 EF2 EF3 EF4	Single-pulse output generated by setting of write FF of card buffer I (A22)	Sets shift FF of card-reader shift register so that stored bits can be written into card buffer on SR1 line.
EF'1 EF'2 EF'3 EF'4	Single-pulse output generated by setting of write FF of card buffer II (A23)	Sets shift FF of card-reader shift register so that stored bits can be written into card buffer on SR1 line.
EF1" EF2" EF3" EF4"	Single-pulse output generated by setting of write FF of card buffer II (A23)	Sets read-shift FF of card-reader shift register so that stored bits can be written into card buffer on SR2 line.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
Empty magazine	Signal from read punch (A26)	Sets read-punch abnormal-operation FF unless empty-station-inhibit switch is closed.
End punch set up	Signal generated when all punches are set up (A28)	Restores X-sentinel-storage FF, INT3 FF and punch-setup FF.
EP	Output of ending-pulse circuit (A2)	Clears static register and restores revolution-counter FF used during transfer from storage to print buffer.
EPR	Generated by the ONE LINE PRINT button on the operator's control panel (A5) EPR = every print	Sets abnormal-operation printer FF.
EQ $\overline{EQ}$	Signals produced from quinary-equality gates (A12)	EQ sent to force zero-plus gate of rA sign FF. $\overline{EQ}$ restores TS FF or CT FF.
Error delete switch	Output of control-panel switch (A5)	If switch is closed, prevents stop FF from being set in case of MRE, CUE, or TE.
ETG	Signal produced whenever column-group counter of read punch is on even count (A28)	Controls four set gates of card-buffer-band I write FF. Produces initial shift in register on all information read from card in second read station.
Even	Output of odd-even FF (A33)	Generates PC signal which is applied to grids of odd print thyratrons. Also alerts one gate of print distributor.
EW $\overline{EW}$ $\overline{EWA}$	Outputs of even-word FF (A16)	Synchronizes signals from control panel or input-output devices with internal computer signals.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
F134°	Input from read punch which indicates time at which punch setup order can be accepted (A26)	Synchronized into computer and used at set gate of punch-setup FF.
F140°	Input from read punch (lasts from 140° - 196°) which indicates time during which select-stacker instruction can be accepted (A26)	Sent to select-read-punch-stacker FF.
F334°	Input from read punch which indicates that all switches are closed in both read stations (A26)	Sets read-initial-storage FF.
Feed ribbon to printer	Output generated by presence of FS 42A (A35)	Sent to printer to feed ribbon before printing.
FFP	Output of RPU drum-revolution counter when count is one (A26)	Alerts input gates to shift register, set gates of readout FF, and set gate of read FF during punch setup.
FFR1	Output of FFR1 FF which is set during reading of cards by card reader (A24)	Alerts set gate of BL1 FF, set and restore gates of write FF's for both card-buffer bands. Generates write pedestal for both card buffers.
FFR2	Output of FFR2 FF which is set during reading of cards by read punch (A26)	Alerts set and restore gates of write FF and generates write pedestal for card-buffer band I. Alerts restore gates of FFR2 FF and read-synchronizing FF. Generates SC and alerts gate to generate STRC.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
FM FMA	Output of fast/normal FF (A18)	Controls switch-driver gates, read-write circuits B, and generation of RGF signal.
From drum on paper feed shaft	Output from printer each time one line of paper is advanced (A35)	Sets paper-index FF which generates index signal to reduce reading in print counter.
FS0 FS2 FS4 FS6 FS8 FS10 FS12 FS14 FS16 FS18 FS20 FS22 FS24 FS26 FS28 FS30 FS32 FS34 FS36 FS38	Outputs of switch drivers (A18)	Select correct storage switch.
Full chip box	Output from read punch (A26)	Sets RPU abnormal-operation FF.
Full stacker	Output from card reader indicating that one stacker or more is full (A25)	Sets abnormal-operation card-reader FF.
Full receiver 0	Output from read punch indicating that the normal or unselected stacker (or receiver) is full (A26)	Sets RPU abnormal-operation FF.
Full receiver 1	Output from read punch indicating that the selected stacker is full (A26)	Sets RPU abnormal-operation FF.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
G1 G2 G3 G4 G5 G6 G7 G8 G9 G10	Outputs of group counter for card reader (A24)	Gate 10 bits from capacitor to shift-register storage. G1 alerts set gate of FFR1 FF and G10 alerts DM gate during keyboard input.
G2A G4A G6A G8A G10A	Outputs of even FF's of group counter for card reader (A24)	Shifts bits in shift register, read from second card, one place to the right before reading out on SR1 line for writing into buffer.
GCB+ GCA1+ GCA2+	Generated by closing of GENERAL CLEAR switch on operator's panel (A5)	Clears counters and restores basic flip-flops at beginning of computation. GCB+ used before A-phase amplifiers. GCA1+ used before input-output B-phase amplifiers and GCA2+ used before processor B-phase amplifiers.
Gen B	Generated by WORD RELEASE button during keyboard input if word is to be placed in rA (A5)	To function encoder to generate same function signals as does the B instruction to send word on M lines into rA. FS 67 not generated to clear static register.
Gen Beta	Generated by WORD RELEASE button during keyboard input if word is to be placed in rC (A5)	To function encoder to generate same function signals as does the staticize instruction to send word on M lines into rC. FS 67 not generated to clear static register. Restores CT FF.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
Gen clear and probe	Generated if card-cycle counter is on count 3 or 4 and row counter is stepped (A24)	To card-reader circuit to brush-sense one row from cards.
Gen L	Generated by WORD RELEASE button during keyboard input if word is to be placed in rL (A5)	To function encoder to generate same function signals as does the L instruction to send word on M lines into rL. FS 67 not generated to clear static register.
Gen PC	Output of gen-PC FF which is set by even signal (A33)	Generates PC signal which is applied to grids of all odd print thyratrons.
Gen PC'	Output of gen-PC' FF which is set by odd signal (A33)	Generates PC' signal which is applied to grids of all even print thryatrons.
Gen Y	Generated by WORD RELEASE button during keyboard input if word is to be placed in rX (A5)	To function encoder to generate same function signals as does the Y instruction to send word on M lines into rX. FS 67 not generated to clear static register.
GO signal to card feed amp.	Output of go FF set after punches are setup (A26)	Drives relay 16 in read-punch unit.
H1 H2	Output of head-indicator FF (A22)	Designates which half of card buffer is under head-group one.
IER	Output of IER FF during multiplication (A15) IER = multiplIER	Alerts static-register ending-pulse gate to multiplication sentinel. Alerts gate of rX sign FF to sign of rA to insure that both parts of product carry same sign.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
IER+	Output of IER FF during multiplication (A15)	Blocks instruction decoder gate so that no odd function signals are generated during shift.
IERA1+	Output of IER FF during multiplication (A15)	To function encoder to generate one pulse time of FS 59.
IERA2+	Output of IER FF during multiplication (A15)	To function encoder to generate FS 59 and 56+.
IER-OR	Output of IER or OR flip-flops or generated by 32A during D3 step (A15)	Alerts gates of MQC to contents of rX.
Index	Output of paper-index FF set each time one line of paper is advanced (A35)	Generates step signal to count down reading of number of lines to feed paper which is set up in print counter.
Index A	Output of set paper-index FF (A35)	Restores space-paper FF which is set when paper is spaced manually from control panel.
INT1 $\overline{\text{INT1}}$	Outputs from interlock-1 FF which holds indication that card-cycle order for card reader has been given (A24)	INT1 sets picker-knife FF when proper point of card cycle is reached and $\overline{\text{INT1}}$ signal alerts ending-pulse gate during card-reader test instruction.
$\overline{\text{INT3}}$	Output from interlock-3 FF which holds indication that card-cycle order for read-punch has been given (A26)	Alerts static-register gate to step to second part of 81 instruction if punch setup completed from previous 81 instruction.
INTP	Signal generated if either print FF or paper-feed interlock FF is set (A35) INTP = interlock printer	Alerts static-register ending-pulse gate on print test instruction.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
IOS $\overline{\text{IOS}}$ IOSA	Output of IOS FF set if any noncontinuous-operation button on the control panel has been pushed (A5) IOS = interrupted operation signal	IOS alerts gates to generate interrupted-operation signals. $\overline{\text{IOS}}$ restores synchronizing FF. IOSA energizes processor-off-normal relay and lights the lamp on the control panel.
IP	Generated by the NO PRINT button on the operator's control panel (A35) IP = inhibit print	Prevents the generation of PC or PC' signals so that the print thyratrons cannot fire. Prevents the setting of paper-feed FF, charge-control FF, and charge-check-fire FF.
IR	Generated with write pedestal for normal storage (A19) IR = inhibit read	Generates write pedestal of fast storage.
IR2D	Output of write FF of normal storage (A19)	Generates write pedestal of normal storage.
IR7	Output of write FF for print-buffer band (A29)	Generates write pedestal of print buffer.
IRC	Output of the motor-control FF (A25)	Alerts set gate of registration-check 1 and 2 FF's and the restore gate of the interlock 1 FF.
IS1 IS2	Outputs of two IS FF's set by print sprocket (A33) IS = inhibit set	Inhibit setting of cores during sampling. IS2 also restores initial code storage FF's.
Jam 4	Generated by circuit which operates if zero reading for paper feeding has been set up in print counter (A35)	Jams one into FF3 of print counter to allow delay of countdown from four reading, while print capacitors charge.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
Jam 7	Generated by restoring of paper-feed FF (A35)	Goes to FF1, FF2, and FF4 of print counter to allow delay of countdown from seven reading, while paper is settling.
Jam 51	Generated by restoring of paper-feed-interlock FF (A35)	Jams ones into FF1, FF5, and FF7 of print counter to allow counting of characters to be printed.
Jam I2A	Output of I/O abnormal-condition FF (A2) Jam I2A = jam second stage of instruction (test) into static register	Partially jams static register to second stage of test instruction. Sets OF FF and restores CT FF.
Jam I2B	Output of I/O abnormal-condition FF (A2) Jam I2B = jam second stage of instruction (test) into static register.	Completes jamming of static register to second stage of test instruction and prevents CT FF from being set during this instruction.
JC1	Output of FFR2 FF during reading of cards by read punch (A26) JC = jam counter	Jams group counter (TG) to reading of one each time a row is transferred from switch to capacitor storage.
JC2	Output of RPU drum-revolution counter with count of one during punch setup (A26)	Jams group counter (TG) to reading of one during punch setup of one row.
JPC	Generated by restoring of print FF (A35) JPC = jam print counter	To FF1, FF2, FF5 and FF7 of print counter to allow delay of countdown from two reading, while print thyratrons de-ionize. Generates high $\overline{PF1}$ signal to interlock static register.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
JTR	Output of the read-synchronizing FF (A26)	Jams the read-punch row counter to a reading of one.
K1 K2 K3 K4 K5 K6 K7 K8	Outputs of quinary equality gates (A12)	Generate EQ or $\overline{EQ}$ signals.
L+ L-	Outputs of rL sign FF (A13)	Indicate sign of word in rL.
L1 L2 L3 L4	Outputs of rL (A10)	Carry information from rL to M lines.
L1OD L2OD L3OD L4OD	Register display output of rL (A10) OD = output display	Sent via rC to display lights on control panel.
L1M L2M L3M L4M	Early outputs of rL (A10)	Carry information from rL to M lines for writing into main storage.
LF	Output of reader field FF (A24) LF = lower field	Indicates that rows 7 through 12 of card are being sensed, in combination with signals R1 through R6 from row counter.
LF'	Output of RPU field FF (A28)	Indicates that rows 7 through 12 of card are being punched or sensed, in combination with signals TR1 through TR6 from row counter. Combined with TR1 through TR6 signals to generate TR'7 through TR'12 signals.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
M1 $\overline{M1}$ M2 $\overline{M2}$ M3 $\overline{M3}$ M4 $\overline{M4}$	Outputs of M buffers (A6)	
M1U $\overline{M1U}$ M2U $\overline{M2U}$ M3U $\overline{M3U}$	Outputs of unit adder (A11)	
ME	Generated if multiplication instruction is set up in static register and MULT.-DIV. ENDING switch on engineering panel is closed (A15) ME = multiply end	Simulates multiplication sentinel (0101) in MQC and generates FS 59 for final shift of simulated sentinel.
MRE	Output of memory-check FF (A19)	Sets stop FF if check bit has been dropped or added in reading from drum unless ERROR DELETE switch is closed. Energizes processor-off-normal relay, and lights lamp on control panel.
MS0 MS2 MS4 MS6 MS8 MS10 $\overline{MS10}$ MS20 $\overline{MS20}$	Outputs of band-selection FF's during search (A18)	Controls switch drivers.
N1 N3 N4 N1B N2B N3B N4B	Outputs of MQC count-down gates (A14)	Reduce reading setup in MQC by count of one.
NC	Signal generated if any noncontinuous-operation button on control panel has been pushed (A5)	Synchronized to generate IOS signal which alerts set gates of stop FF.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
NM NMA	Outputs of fast/normal FF (A18)	Controls switch drivers and permits reading from normal storage.
No card in read 1	Output from read punch indicating no card in read station 1, or error condition (A26)	Sets abnormal-operation read-punch FF unless EMPTY STATION INHIBIT switch on control panel is closed.
No card in read 2	Output from read punch indicating no card in read station 2, or error condition (A26)	Sets abnormal-operation read-punch FF unless EMPTY STATION INHIBIT switch on control panel is closed.
011 032 012 033 013 034 014 035 015 041 016 042 021 022 023 024 025 026 027 031	Outputs of quinary adder (A11)	Carry results of quinary addition to rA for storage.
0C1 0C2 0C3 0C4	Outputs of read circuits of card-buffer band II (A23)	Carry information read from buffer to M lines for writing into main storage.
Odd	Output of odd-even FF (A33)	Generates PC' signal which is applied to grids of even print thyratrons. Also alerts one gate of print distributor.
OF $\overline{OF}$	Outputs of overflow FF (A13)	Indicates overflow condition and sets overflow-delay FF so that next instruction will be taken from c+1 address instead of c address.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
OF2+	Output of overflow-delay FF (A13)	Restores OF FF and keeps TS FF set for one word time so that c+1 address is read. Prevents generation of St3B-.
OPO	Generated each drum revolution by coincidence of TS1 and t11B-	Synchronizes oscilloscope.
OR	Output of OR FF (A15) OR = divisOR	Alerts input gates of rX to contents of MQC, input gate of rA to SBW of rX, set gates of MQC, and set gate of OF FF.
OR+	Output of OR FF (A15)	Blocks generation of add function signals while shifting and blocks readout of contents of rL to M lines.
ORA+	Output of OR FF (A15)	Generates FS 56+ and 71, sets CP FF, and generates CLQ to clear MQC.
OTG	Generated whenever group counter for read punch is on odd count (A28)	Alerts four set gates of write FF of card-buffer band I.
Out of ribbon	Output from printer (A35)	Sets abnormal-operation-printer FF.
Out of paper	Output from printer (A35)	Sets abnormal-operation-printer FF.
P1 $\overline{P1}$ P2 $\overline{P2}$ P3 $\overline{P3}$ P4 $\overline{P4}$ P5 $\overline{P5}$ P6 $\overline{P6}$ P7 $\overline{P7}$	Outputs of print counter (A35)	Step print counter, restore paper-feed FF and paper-feed-interlock FF.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
$\overline{P1A}$ $\overline{P2A}$ $\overline{P3A}$ $\overline{P4A}$ $\overline{P5A}$ $\overline{P6A}$ $\overline{P7A}$	A-phase outputs of print counter (A35)	Inhibits set gate of paper-feed FF.
(To) paper feed control	Output of paper-feed FF (A35)	Controls paper-feed clutch on printer.
(To) paper feed brake	Output of paper-feed FF (A35)	Controls paper-feed brake on printer.
PBE	Output of print-buffer error FF (A30)	Sets printer-abnormal-operation FF.
PC1 PC2	Output from card-reader photocell circuits which detect leading edge of card (A25)	Restore read-station registration-check flip-flops.
PC1A PC1B PC2A PC2B PC3A PC3B PC4A PC4B PC5A PC5B PC6A PC6B PC7A PC7B PC8A PC8B PC9A PC9B PC10A PC10B PC11A PC11B PC12A PC12B PC13A PC13B PC14A PC14B	Outputs from print-word counter (A31)	Monitors words being read from buffer so that proper cores are set to fire print thyratrons.
PCE	Output of print-code error FF if error occurs in code generator (A32)	Sets abnormal-operation-printer FF.
PCS	Photocell signal from disc timer on card reader (A24)	Monitors each of 12 rows being sensed from cards.
PF $\overline{PF}$	Outputs of paper-feed FF (A35)	Indicates paper is actually being advanced.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
PFI $\overline{\text{PFI}}$ $\overline{\text{PFIA}}$	Outputs of paper-feed interlock FF (A35)	Blocks static-register step gates to prevent two simultaneous print instructions, and blocks printing and error detection until paper is completely advanced and all necessary delays completed.
PFE	Output from printer indicating paper not feeding properly (A35)	Restores paper-feed FF to stop paper from feeding and sets abnormal-operation-printer FF.
(To) picker knife	Output of picker-knife FF for card reader (A24)	Feeds card to card reader.
PR $\overline{\text{PR}}$	Outputs of print FF (A35)	Indicate printing is taking place. Block static-register step gates. Alert quadrant-counter gates, print-distributor gates, print-error circuits and set gate of charge-check-extinguish FF
PRB	Output of register-control FF (A31) PRB = print-B instruction	Generates function signals needed to read unprimed word into rA before writing into print buffer. Same function signals as needed during B instruction.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
PRG1 PRG2 PRG3 PRG4 PRG5 PRG6 PRG7 PRG8 PRG9 PRG10 PRG11 PRG12 PRG13	Outputs of print gate packages (A34)	Gate set signals to cores indicated by count in print word counter. Also gate sample signals to cores.
Print	Output of print comparator (A33)	Alerts print distributor gates.
Print C1	Generated when PRINTER CLEAR switch on operator panel is closed (A35)	Restores paper-feed and abnormal-operation printer FF's.
PRP1 PRP2 PRP3 PRP4 PRP5	Generated by every print sprocket (A33)	Sample 65 cores to fire print thyratrons if cores are set.
PRS1 PRS2 PRS3 PRS4 PRS5	Outputs of print set packages (A34)	These set signals gated to proper cores by PRG signals
PRY	Output of register-control FF (A31) PRY = print Y instruction	Generates function signals to read primed word into rX before writing into print buffer. Same function signals needed for Y instruction.
PSP $\overline{\text{PSP}}$	Generated by every other print sprocket (A33)	PSP alerts set gates of final code-storage FF's and generates step signal to count down reading of 51 in print counter. $\overline{\text{PSP}}$ restores final code-storage FF's.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
PSU	Output of punch-setup FF (A26)	Alerts input gates of information distribution matrix to bits from shift register.
PWRB PWRBA	Outputs of print-buffer-band-I write FF (A29)	Permits writing on print-buffer band II.
Q1 $\overline{Q1}$ Q2 $\overline{Q2}$ Q3 $\overline{Q3}$ Q4 $\overline{Q4}$	Outputs of MQC (A14)	Carry information from MQC.
QC1 $\overline{QC1}$ QC2 $\overline{QC2}$	Outputs of quadrant counter (A29)	Controls switching matrix during writing into and reading from print buffer.
QS1 $\overline{QS1}$ QS2 $\overline{QS2}$	Outputs of quadrant-selection FF's (A18)	Controls switch drivers.
QT stop	Signal generated by COMPARISON STOP button on operator panel (A5)	Sets stop FF if Q or T instruction is set up in static register.
QUAD+	Generated each time RPU drum-revolution counter is stepped by PS sentinel (every drum revolution during punch setup) (A26)	Controls even-word FF and steps revolution counter.
1R 13R 2R 14R 3R 15R 4R 16R 5R 17R 6R 18R 7R 19R 8R 20R 9R 21R 10R 22R 11R 23R 12R 24R	Outputs of quinary carry gates (A12)	Generates C and C' signals to indicate quinary carry, or $\overline{C}$ signal to indicate no quinary carry.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
R1 $\overline{R4}$ R2 R3 R4 R5 R6	Outputs of card-reader row counter (A28)	Monitors rows being sensed from upper or lower field of card.
R1' R2' R3' R4' R5' R6'	Outputs of card-reader row counter (A24)	Buffed together to generate R1-4 signal, R5, 6 signal, R1, 5 signal, or R2, 6 signal.
R1" R2" R3" R4" R5" R6"	Outputs of read-punch row counter (A28)	Monitors rows being sensed or punched from upper or lower field of card.
R1-4	Generated by combining signals R1' through R4' (A24)	Controls set gates of card-buffer write FF's to write unprimed words read by card reader.
R5, 6	Generated by combining signals R5' and R6' (A24)	Controls set gates of card-buffer write FF's to write primed words read by card reader.
R1, 5	Generated by combining signals R1' and R5' (A24)	Controls write input gates to track 1 of both card buffers to write first row of both primed and unprimed words read by card reader.
R2, 6	Generated by combining signals R2' and R6' (A24)	Controls write input gates to track 2 of both card buffers to write second row of both primed and unprimed words read by card reader.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
R1-4'	Generated by combining signals R1" through R4" (A28)	Controls set gates of card-buffer-I write FF to write unprimed words read by read-punch.
RC1 $\overline{RC1}$ RC2 $\overline{RC2}$	Outputs of revolution—counter FF's which monitor drum revolutions during storage-to-print-buffer transfer of words to be printed (A31)	Controls setting of various FF's used during printing.
RCC3	High signal generated as a result of empty magazine or registration error in either read station of card reader (A25)	In case of registration error prevents next card (which might be registering correctly) from restoring either registration-check FF. In case of empty magazine, restores FF3 and FF4 of card-cycle counter to prevent setting of either registration-check FF so that only empty magazine light is lit.
RCT1 RCT2	RCT1 generated by stepping of static register during regular search to staticize step; RCT2 generated during H, X and J search (A2)	Restore CT FF so that next search will be for c address. RCT2 also generates write pedestal.
R5, 6'	Generated by combining signals R5" and R6" (A28)	Controls set gates of card-buffer-I write flip-flop to write primed words read by read punch.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
R1, 5'	Generated by combining signals R1" and R5" (A28)	Controls write input gates to track 1 of card buffer I to write first row of both primed and unprimed words read by read punch.
R2, 6'	Generated by combining signals R2" and R6" (A28)	Controls write input gates to track 2 of card buffer I to write second row of both primed and unprimed words read by read punch.
RCT3 RCT4 RCT5	Outputs of ending-pulse gates on static register (A2)	Restore CT FF so that next search will be for c address. RCT3 and RCT4 restores band-selection FF's and RCT5 sets print FF.
RD	Output of read FF of main storage (A19)	Alerts set gate of check-timing FF. Alerts set gate of write FF, and generates write pedestal for card-buffer band I.
RD1 RD2 RD3 RD4	Register C outputs (A1) RD = register display	Display contents of rL, rX, rA, or rC on control panel.
RDSP $\overline{\text{RDSP}}$	Outputs of read-stop FF set during transfer of output words from main storage to card buffer (A22)	Prevents writing on card buffer from two sources at once (output words from main storage and input words from capacitor storage)
RECC	Generated by the ONE CARD READER button on the operator's control panel (A5) RECC = reader every card cycle	Sets abnormal-operation card-reader FF.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
Reset TS	Output of ending-pulse gate for H-X-J search (A2)	Restores TS FF.
RGF	Generated as a result of setting read FF of main storage, and selecting fast storage (A19)	Permits reading from fast storage.
RI	Generated by write pedestal of print-buffer band I (A29) RI = read inhibit	Permits simultaneous writing on print-buffer band II.
RO $\overline{RO}$	Outputs of read-out FF during setting up of punches (A26)	RO sets read FF of card buffer and sets punch-shift FF. $\overline{RO}$ inhibits gates of information-distribution matrix.
RS1	Output of shift FF for card reader (A25)	Alerts write input gates of card buffer.
RSA	Generated by REGISTER SELECTOR A button on operator panel (A5)	Alerts gate which produces gen. B signal for type-in to rA. Gates contents of rA to display panel neons, including sign stored in FF.
RSC	Generated by REGISTER SELECTOR C button on operator panel (A5)	Alerts gate which produces gen. beta signal for type-in to rC. Gates contents of rC to display panel neons.
RSC2	Output of read FF for card-buffer II (A23)	Sets write FF of main storage.
RSC5	Output of read FF for card-buffer band I (A22)	Sets write FF of main storage.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
RSX	Generated by REGISTER SELECTOR X button on operator panel (A5)	Alerts gate which produces gen. Y signal for type-in to rX. Gates contents of rX to display panel neons, including sign stored in FF.
RSL	Generated by REGISTER SELECTOR L button on operator panel (A5)	Alerts gate which produces gen. L signal for type-in to rL. Gates contents of rL to display panel neons, including sign stored in FF.
RSP	Output of keyboard-input FF when each key is released and when word is released (A27) RSP = restore sprocket	Restores sprocket-synchronizing FF and word-release-synchronzing FF's.
RTS	Generated if either or both quadrant-selection FF's are set during search (A18)	Restores TS FF.
S1 $\overline{S1}$ S2 $\overline{S2}$ S3 $\overline{S3}$ S4 $\overline{S4}$	Outputs of S buffers (A7)	Carry information into and out of registers.
S1C $\overline{S1C}$ S2C $\overline{S2C}$ S3C $\overline{S3C}$	Output of complement circuit for quinary bits (A11)	Carry information into quinary adder.
Sample pulse 1	Output of card-reader sample-pulse FF (A24)	Alerts gates which transfer 10 bits at a time from capacitor storage into shift register.
Sample pulse 2	Output of read-punch sample-pulse FF (A26)	Alerts gates which transfer 10 bits at a time from capacitor storage into shift register.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
SA0	Generated during search operation or when processing is stopped (A5) SA0=set abnormal operation	Alerts set gates of abnormal-operation FF's for the card reader, read punch, and printer.
SC	Generated if FFR2 FF is set and column-group counter is stepped (A28)	Clears read-punch shift register.
SCCC	Generated by stepping of card-cycle counter for card reader (A24)	Alerts set gate of card-cycle-counter FF5 and is sent to registration-check circuits.
SCI+	Generated by keyboard-alert switch (A5)	Permits card-reader and read-punch shift registers and counters to be used for keyboard input without generating signals normally used.
SCI1 SCI2 SCI3 SCI4	Output of keyboard encoder (A5)	Carry 4 bits of each digit typed in to four shift registers.
SCISA	Output of keyboard-input FF (A27)	Shifts information through four shift registers so that information typed in most significant digit first reads out of registers the same way.
SCISB	Output of keyboard-input FF (A27)	Supplies recirculation path to two group counters during keyboard input.
Scope Sync	Generated by timing signal t11A+ (A16)	Synchronizes oscilloscope.
Scope Sync	Generated by several different combinations of signals selected by switches (A26)	Synchronizes oscilloscope.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
SCS	Output of punch-shift FF during punch setup (A27)	Shifts bits read into shift register from card buffer.
Select A Select B	Generated by print sprocket pulses (A33)	Buffed together to gate sample pulse to 65 cores during printing.
Select Stacker 1	Output of select-stacker FF for card reader (A25)	Sorts card into stacker 1.
Select Stacker 2	Output of select-stacker FF for card reader (A25)	Sorts card into stacker 2.
Set 1 Set 2 Set 5 Set 6	Outputs of print-counter FF2, FF3, FF6, and FF7 (A35)	Change reading in print counter during count-down.
SET STOP	Generated by the card-cycle error FF (A24)	Sets the stop FF.
SGC	Output of punch-shift FF (A27) SGC = step group counter	Steps read-punch group counter and initially clears shift register.
(To) sort amplifier	Output of select-stacker FF for read punch (A26)	Drives relay 19 in read punch.
SP $\overline{SP}$	Outputs of stop FF (A5)	Indicates that computer is stopped. Gates on instruction decoder are blocked to prevent further instructions from being set up.
SPA	Output of the stop FF (A5)	Generates low signal SA0.
SPR	Output of sprocket-synchronizing FF during keyboard input (A5)	Alerts set gate of key-board-input FF.
Sprocket	Direct input from sprocket wheel on printer (A33)	Generates signals used to synchronize print-ing of one line.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
SRC	Generated when photocell signal is received from card reader (A24) SRC = step row counter	Steps row counter.
SR1	Output of card-reader shift register (A25)	Recirculates through register and goes to write input gates of card-buffer bands.
SR2	Output of read-punch shift register (A27)	Recirculates through register and goes to write input gates of card-buffer band I.
SS1	Generated when write FF of card-buffer band I is restored after writing words sensed by card reader (A22)	Steps card-reader group counter.
SS'1	Generated when write FF of card-buffer band I is restored after writing words sensed by read punch (A22)	Steps read-punch group counter.
SS2	Generated when write FF of card-buffer band II is restored after writing words sensed by card reader (A23)	Steps card-reader group counter.
SSP1 SSP2	SSP1 generated when FFR1 FF is set; SSP2 generated each time group counter is stepped (A24)	Both go to clear card-reader shift register after each group of 10 bits is shifted out.
ST $\overline{ST}$	Output of start FF (A5)	Restores stop FF.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
St3B-	Generated during search if no overflow (A16)	Times setting of band-selection FF's.
Staticize every minus	Generated by ONE INSTRUCTION button on control panel (A5)	Alerts one set gate of stop FF. Required signal to permit keyboard input.
STC	Generated by setting of register-control FF on first drum revolution (A31)	Sets charge-control FF.
Step	Generated by index signal each time paper is fed one line, or by PSP signal from print sprocket wheel (A35)	Reduces original reading in print counter.
Stop switch	Generated by STOP button on any of the three auxiliary control panels (A35, A25, and A26)	Sets abnormal-operation FF's.
STR1 $\overline{\text{STR1}}$ STR2 $\overline{\text{STR2}}$ STR4 $\overline{\text{STR4}}$ STR5 $\overline{\text{STR5}}$ STR6 $\overline{\text{STR6}}$ STR7 $\overline{\text{STR7}}$ STR8 $\overline{\text{STR8}}$	Outputs of static-register FF's (A2)	Decode instructions.
STRC	Generated by stepping of row counter by X sentinel on third drum revolution during punch setup (A28)	Restores column-drive reset FF and clears the read-punch row counter.
TE	Output of timing-error FF (A17)	Stops computer.
TECC	Generated by the ONE CARD RPU button on the operator's control panel (A5)	Sets abnormal-operation read-punch FF.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
TEF1 TEF2 TEF3 TEF4	Single pulse generated by setting of write FF of card buffer I (A22)	Sets read-shift FF of read-punch shift register so that stored bits can be written into card buffer on SR2 line.
TG1 TG2 TG3 TG4 TG5 TG6 TG7 TG8 TG9 TG10	Outputs from read-punch group counter (A28)	Gate 10 bits at a time from capacitor storage, during sensing. Gate 10 bits stored in shift register to information-distribution matrix during punch setup.
TG1A TG2A TG3A TG4A TG5A TG6A TG7A TG8A TG9A TG10A	A-phase outputs of read-punch group counter (A28)	Odd signals (1, 3, 5, 7, 9) buffed together to form OTG and even signals (2, 4, 6, 8, 10) to form ETG.
TOS2	Output of read-punch read-shift FF (A27)	Alert write input gates of card buffer I.
Tower power off	Signal from read-punch unit indicating power off in that unit.	Sets read-punch abnormal-operation FF.
TOX	Generated during translation from UCT into card code (A8) TOX = to register X	Places one bit in A2 position of rA.
TR1 TR2 TR3 TR4 TR5 TR6	Outputs of read-punch row counter (A28)	Combine with UF' and LF' to form signals TR'1 through TR'12 which identify 12 rows of card.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
TR'1 TR'7 TR'2 TR'8 TR'3 TR'9 TR'4 TR'10 TR'5 TR'11 TR'6 TR'12	Generated by combining TR1-TR6 with UF' and LF' signals (A28)	Identify 12 rows of actuator matrix during punch setup, and of sensing-switch matrix during sensing by read-punch. Note: signals are TR" instead of TR' when identifying rows of sensing-switch matrix.
TS $\overline{TS}$	Outputs of TS FF (A12)	TS indicates that address under head and address being searched for are located on same channel.
TS1 $\overline{TS1}$ TS2 $\overline{TS2}$ TS3 $\overline{TS3}$ TS4 $\overline{TS4}$ TS5 $\overline{TS5}$	Outputs of timing band (A17)	Identify storage locations around the drum. Also identify input-output sentinels.
UF	Output of reader field FF (A24) UF = upper field	Identifies upper-field rows on card sensed by card reader.
UF'	Output of RPU field FF (A28)	Identifies upper-field rows on card sensed by read-punch.
UFA	Output of the RPU field FF (A28)	Alerts set gate of column-drive-reset FF if column drivers are to be reset early.
$\overline{W1}$ $\overline{W2}$ $\overline{W3}$ $\overline{W4}$	Outputs from normal write input circuits to fast write input circuits (A19)	Carry information from M lines for writing into fast storage.
W6	Output from main-storage write FF (A19)	Alert write input-circuit gates of fast storage.
WD10 WD31 WD11 WD40 WD20 WD41 WD21 WD50 WD30 WD51	Outputs from normal-access storage (A19)	Set memory switches.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
WF10 WF11 WF20 WF21 WF30 WF31 WF40 WF41 WF50 WF51	Outputs from fast-access storage (A20)	Set memory switches.
WO	Output of card-buffer-band-I write FF (A22) WO = write output	Generates card-buffer write pedestal.
WR+ WR-	Generated by plus or minus buttons on keyboard (A5) WR = word release	Generates signals which release typed-in word into selected register, and sends sign of word into register FF.
WRA	A-phase output of word-release FF during keyboard input (A5)	Generates an RSP signal to restore word-release-synchronizing FF's, and supplies shift pulses to shift information out of four temporary-storage registers.
WRA+ WRA-	Signals generated when word is being typed into rA and one of the two word-release buttons has been depressed (A5)	Sets rA sign FF to selected state.
WRB	B-phase output of word-release FF during keyboard input (A5)	Generates function signals which open up path into selected register on M lines, and gates information stored in four registers to M lines. Generates ending pulse during staticize step.

Table B-1. Control and Information Signals (cont)

Signal	Source	Function
WRL+ WRL-	Signals generated when word is being typed into rL and one of the two word-release buttons has been depressed (A5)	Sets rL sign FF to selected state.
WRX+ WRX-	Signals generated when word is being typed into rX and one of the two word-release buttons has been depressed (A5)	Sets rX sign FF to selected state.
X+ X-	Outputs of rX sign FF (A13)	Indicates sign of word in rX.
X1 X2 X3 X4	Normal recirculation outputs of rX (A9)	
$\overline{X4}$	Output of subregister of rX (A9)	Used during printing to compute new check bit for word to be printed.

APPENDIX C

INSTRUCTION LIST

This appendix lists all of the instructions provided for the system. These instructions are divided into seven groups, as follows:

(1) Arithmetic instructions
(2) Transfer instructions
(3) Translate instructions
(4) Miscellaneous instructions
(5) Comparison instructions
(6) Input-output test instructions
(7) Input-output instructions

The four arithmetic instructions in group 1 and the 60 instruction of group 2 are explained in detail in Section IV of this manual. The input-output instructions (group 7) are explained in detail in the separate manuals for the three input-output devices. All the remaining instructions are explained on the block diagram level in Section V of this manual.

The letter m refers to the m address of the instruction word, the letter c to the c address. A dotted line in place of the m address means that any digits in this part of the instruction word are ignored by the computer. The parenthesis enclosing letters means "contents of." For example, (rA) means contents of register A.

The term "memory" is interchangeable with the term "main storage."

Table C-1. Instruction List

INSTRUCTION	DESCRIPTION	TIMING (number of word times for minimum latency)
	Arithmetic Instructions	
70 m c	Add algebraically (m) to (rA) and put result into rA.	5
75 m c	Subtract algebraically (m) from (rA) and put result into rA.	5
85 m c	Multiply (rL) by (m) and put 20-digit product into rA (most significant half) and rX (least significant half), each half having sign of product.	5 plus the number of digits in the multiplier plus the sum of the multiplier digits.
55 m c	Divide (m) by (rL) and put unrounded result and sign of the quotient in rA and remainder in rX. Remainder has sign of dividend. If divisor = dividend or divisor = 0, an overflow to c+1 will result.	20 plus the sum of the odd digits of the quotient plus the sum of the tens complements of the even digits. MSD is 1 (odd).
	Transfer Instructions	
25 m c	Transfer (m) to rA.	4
60 m c	Transfer (rA) to m.	4
05 m c	Transfer (m) to rX.	4
65 m c	Transfer (rX) to m.	4
30 m c	Transfer (m) to rL.	4
50 m c	Transfer (rL) to m.	4
77...c	Transfer (rA) to rL.	3

Table C-1. Instruction List (cont)

Translate Instructions		
12...c	Send (rA) and (rX) through the card-code-to-UCT translator, put the result into rA, and clear rX. (rA contains the unprimed word of the card image.) Sign of the result is the sign of the unprimed word in rA.	3
17...c	Send (rA) through the UCT-to-card-code translator and put the two words into rA and rX. (rA contains the unprimed word and rX the primed.) Signs of results are positive. All UCT-code zeros are translated to card-code punching zeros.	3
Miscellaneous Instructions		
20 m c	Superimpose the 1 bits of (m) on to (rA) and leave the result in rA. Sign of rA is undisturbed.	4
35 m c	Change the bits in each decimal digit of (rA) to binary zero wherever (m) has a binary zero in the corresponding bit position. Sign of rA is undisturbed.	4
32 n c	Shift (rA) to the right n places into rX, which also is shifting to the right into rA. The sign positions are not involved in this shift. n can vary between 0 and 10 and is a single digit inserted in the next to most significant digit position of m.	3 + n

Table C-1. Instruction List (cont)

Miscellaneous Instructions (cont)		
37 n c	Shift (rA) to the left n places, losing the most significant digits and bringing in zeros in the least significant places on the right. n can vary from 0 to 10 and is a single digit inserted in the next to most significant digit position of m. The sign digit is undisturbed.	3 + n
62...c	Zero-suppress the word in rA. Every card-code punching zero and comma (and any other character containing a one in the least significant bit position) to the left of the most significant digit is replaced by non-punching zeros.	4
67...c	Stop the computer.	Indefinite
Comparison Instructions		
82 m c	If (rA) equals (rL), the next instruction is in m; if not, the next instruction is in c.	3
87 m c	If (rA) is algebraically greater than (rL), the next instruction is in m; if not, the next instruction is in c.	3
Input-Output Test Instructions		
22 m c	If the read-punch unit buffer is loaded, transfer (rC) to rA and go to m for the next instruction. If not, go to c for the next instruction.	3

Table C-1. Instruction List (cont)

	Input-Output Test Instructions (cont)	
42 m c	If the high-speed reader unit buffer is loaded, transfer (rC) to rA and go to m for the next instruction. If not, go to c for the next instruction.	3
27 m c	If printer is available (print FF and paper feed interlock FF restored), transfer (rC) to rA and go to m for next instruction. If printer is not available (print FF and/or paper feed interlock FF set) go to c for the next instruction.	3
	Input-Output Instructions	
	Read-Punch Unit	
81 m c	Transfer the output card images from the band designated by m to the buffer band. When the memory-to-buffer transfer is completed, the computer is free to operate on other instructions.	203
46 m c	Wait until the buffer is loaded, then transfer the input card images from the read-punch buffer to the input band designated by m (0000, 0200, 0400, etc.).	203
57 m c	Select output stacker. If m = 0000, select stacker 0; if m = 0100, select stacker 1.	3

Table C-1. Instruction List (cont)

Input-Output Instructions (cont)		
	Card Reader	
72 m c	Feed one card into the continuously moving rollers of the feed. The card will be read at each station in turn, and the data stored in the buffer band. If previous 72 instruction has not yet been accepted, go to m for next instruction.	3
96 m c	Wait until the card-reader buffer is loaded, then transfer this data from the buffer to the memory band designated by m (0000, 0200, 0400, etc.).	203
47 m c	Select output stacker. If m = 0000, select stacker 0; if m = 0100, select stacker 1; if m = 0200, select stacker 2.	3
	Printer	
16 m c	Advance. Wait until the previous advance or print operation is completed, then move the paper the number of lines indicated by the two least significant digits of m. Once the paper movement is started, the computer is free to operate on other instructions.	3
11 m c	Advance and print. Wait until the previous advance (16) or print (11) operation is completed, then start to move paper the number of lines indicated by the two least significant digits of m. The two most significant digits of m indicate the print-interlace band.	591

A GLOSSARY OF TERMS

This glossary contains the definitions of terms used in the manual. Underscored terms in the definitions are those that are defined elsewhere in the glossary.

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RCA Service Company, The Language and Symbology of Digital Computer Systems, May 1958.

Abnormal condition. A condition that exists whenever a failure in the operation of the system has occurred or whenever the system is operated in a noncontinuous mode.

Acceptor. An impurity in a semiconductor which may induce hole conduction. It is used in the production of a P-type semiconductor.

Access time. The time required under specified conditions to transfer information to or from the magnetic storage drum, including the time necessary to locate the desired storage address.

Address. A numerical expression which designates a particular register or a particular location on the magnetic storage drum.

Alert. To place a low signal on a gate to prepare it for a possible gating function.

Alpha (α). Emitter-to-collector current amplification in transistors. For a junction transistor, alpha is less than one.

Alpha cutoff (α_{co}). The frequency at which the current amplification (alpha) of a transistor falls to 0.7 of its low frequency value, or 3 decibels down.

Arithmetic amplifier. See S-type and T-type noncomplementers.

Automatic gain control (AGC). A circuit arrangement which automatically adjusts the gain in a specified manner in response to changes in input.

Avalanche breakdown. The condition which exists when the inverse voltage applied across a PN junction is sufficient to cause electrons to ionize atoms upon collision, releasing new electrons and developing a cumulative increase or avalanche of current. The voltage at which avalanche breakdown occurs is called the Zener voltage.

Band. A group of tracks on the magnetic storage drum. Each band contains five tracks, except that the card buffer band contains only four tracks and the print buffer band only two.

Band selection. The part of the search operation which locates the desired band in main storage.

Barred signal. An overscored signal, for example $\overline{S1}$, always opposite in polarity to the corresponding unbarred signal, for example S1.

Barrier potential. The potential difference across the space-charge layer about a PN junction including a maximum of potential which prevents a low energy particle on one side of the region from passing to othe other side.

Base. A very narrow electrode located between the emitter and collector of a transistor. Current flow between the emitter and collector is dependent upon the current flow between the emitter and base, which in turn is dependent upon the emitter-to-base potential. The base is somewhat analogous to the control grid of a vacuum tube.

Beat note. A frequency resulting from the combination of two different frequencies. It is numerically equal to the difference between or the sum of these two frequencies.

Beta (β). The short-circuit current gain is a common-emitter transistor amplifier ($\beta = \frac{\alpha}{1 - \alpha}$), where α is the current amplification (the base-to-collector current gain of a transistor). For a junction transistor, beta is greater than one.

B-H curve. See hysteresis loop.

Binary. Referring to the binary number system.

Binary bit. The most significant bit of the four-bit UCT code. This bit is referred to as the binary bit because it determines which of two ranges of numerics (0 through 4 or 5 through 9) the quinary bits represent.

Binary number system. A system for representing decimal digits using the base 2, and containing only two numeric symbols, 0 and 1.

Biquinary code. A code for representing decimal digits. The code uses five binary numbers and a 0 bit to represent the digits 0 through 4 and the same binary numbers and a 1 bit to represent the digits 5 through 9.

Bit. A binary character (either 0 or 1) which, when combined with other bits in a certain order, can represent a numeric or alphabetic character.

Bleeder. A resistance connected in parallel with a power-supply output to protect equipment from excessive voltages if the load is removed or substantially reduced, to improve the voltage regulation, and to discharge the filter capacitors when the unit is turned off.

Block. To place a high signal on a gate to prevent the passage of any low signals, thus inhibiting the gating operation.

Block punch. A method of card punching in which all punching on a card is accomplished in one operation of the card-punching mechanism.

Blocking pulse. A continuous sine wave approximately 20 volts peak-to-peak in amplitude which is required for the correct operation of certain series-pulse magnetic amplifiers.

Blocking signal. A high input signal to a gate which inhibits the gating operation.

Bobbin. A small reel or spool used to support the wraps of thin magnetic tape which comprise the magnetic material in the core of a magnetic amplifier. The bobbin is frequently constructed of non-magnetic stainless steel.

Brush sensing. A method of detecting the presence of holes in a punched card. Conducting wire brushes are pressed against the cards to make electrical contact with a conducting surface below the card wherever a hole is present.

Buffer. A circuit or device whose output is generated when one or more of the input signals is a high. A buffer performs the function of the logical "OR".

Buffer storage. A storage medium used to compensate for a difference in rate of flow or time of occurrence when transferring information between the input-output devices and main storage.

c address. The last four digits of the instruction word which usually comprise the storage address of the next instruction.

Card buffer. Four tracks on the magnetic storage drum that store information that is to be punched in cards or that is read from cards. See buffer storage.

Card code. The code in which information is recorded on tabulating cards by means of punched holes. In the New Univac® system, the card code is a six-bit code.

Carrier. An entity capable of carrying electric charge through a solid; for example, a hole or a conduction electron in a semiconductor.

Carry

1. (verb) In the process of addition, to add the amount by which a sum overflows a column to the column of digits of next higher significance.
2. (noun) The amount by which a sum overflows a column of digits.

Cathode follower. An electron-tube circuit in which the output load is connected in the cathode circuit, and the input is applied between the control grid and the remote end of the cathode load. The circuit is characterized by low output impedance, high input impedance, and gain less than unity under most operating conditions.

Channel. An area which extends horizontally across the length of the magnetic storage drum and corresponds to one timing band address. There are two hundred channels (one for each timing band address) around the circumference of the storage drum.

Character. In the New Univac® system, a printed or typed letter, number, or symbol, which is combined with other characters to express information.

Check bit. A bit added to the bits representing a digit or character to facilitate the detection of error.

Check-bit error. An error that occurs when a 0 check bit is detected where a 1 check bit is required or vice versa.

Circular shift. See right shift.

Circulating register. A register in which the information is stored dynamically; that is, it constantly circulates in a closed loop.

Class A operation. The operation of an amplifier biased so that output current flows throughout the entire operating cycle.

Class AB operation. The operation of an amplifier biased so that output current flows for more than half but less than the entire operating cycle.

Class B operation. The operation of an amplifier biased so that output current flows for approximately half of the operating cycle.

Class C operation. The operation of an amplifier biased so that output current flows for appreciably less than half of the operating cycle.

Clear. To place a storage device (for example, a flip-flop or register) in a prescribed state; unless otherwise stated, this state is assumed to be the logically quiescent state.

Clear circuit. A circuit that generates signals to clear a storage circuit (for example, a flip-flop or register).

Clear pulse. A positive-going spike of 0.2-microsecond duration which has a peak amplitude 2 volts above the +18-volt reference level. The signal resets the flip-flops in the RFF-S packages after a read operation.

Clock. A linear, high-power, narrow-band amplifier which supplies power to operate the magnetic amplifiers of a computer (power pulses and blocking pulses). The clock acts as a central timing device for the computer.

Coercive force (H_c). The value of applied magnetizing force at which a hysteresis loop crosses the abscissa (has zero value of magnetization).

Collector. An electrode of a transistor through which the flow of principal carriers leaves the interelectrode region. The collector is analogous to the anode of a vacuum tube.

Comparator. A circuit for comparing information from two sources.

Comparison. The comparing of information from two sources to determine equality.

Complement. To invert a signal from a high to a low or from a low to a high.

Complementer (complementing amplifier). A magnetic amplifier which inverts the input signal. A low signal input to the complementer becomes a high output signal; a high input becomes a low output signal. Compare noncomplementer.

Computer code. See UCT code.

Computer word. See word.

Conditional transfer. A transfer of control from the m address to the c address, or vice versa, as a result of a comparison instruction.

Conduction band. A range of states in the energy spectrum of a solid in which electrons can move freely, allowing the material to carry an electric current.

Connecting diode. An isolating device used to avoid reaction of a driven circuit on the corresponding driving circuit.

Continuous mode. The normal method of operation of the computer in which the program is automatically processed to its completion.

Control signal. A signal generated by any of several circuits to control the operations performed during the execution of an instruction.

Core, toroidal. See toroidal core.

Counter. A device capable of changing from one to the next of a sequence of distinguishable states upon each receipt of an input signal.

Covalent bond. A chemical linkage in which the sharing of electrons occurs in pairs, each pair being equivalent to one conventional chemical bond. In the union there is a tendency for each atom to acquire an outermost layer of eight electrons.

Current sink. A circuit which conducts varying amounts of current necessary to clamp either the positive or negative peak value of a current waveform to some desired reference level.

Cycling unit. A circuit which is energized by the timing combination from the timing band and which generates the timing signals.

Data word. See word.

Decimal carry. See carry.

Delay line. A circuit used to delay, for a certain period of time, the starting of a waveform.

Depletion layer. See space-charge layer.

Digit. A single number, letter, or symbol represented by four bits in UCT code, and six bits in card code.

Discriminator. See phase detector.

Donor. An impurity in a semiconductor which may induce electronic conduction. It is used in the production of an N-type semiconductor.

Doping. The addition of selected impurities to a semiconductor to obtain a desired electrical property; that is, in the production of N-type and P-type semiconductors.

Emitter. An electrode of a transistor from which the flow of principal carriers enters the interelectrode region. The emitter is analogous to the cathode of a vacuum tube.

Ending pulse. A pulse generated to clear the static register of instruction digits at the completion of the instruction.

Energy level. A stationary state of energy of any physical system. The existence of many stable or quasi-stable states, in which the energy of the system stays constant over a considerable period of time.

Even combination. A group of bits containing an even number of ones.

Execute. To perform the various functions of an instruction.

Extract. To remove certain digits from a word according to a predetermined pattern. Similar but not identical to superimpose.

Extrinsic semiconductor. A semiconductor whose electrical properties are dependent upon its impurity content.

Fast-access storage. Five bands of the magnetic storage drum which provide minimum access time to locate a storage address and read or write information.

Feedback. The transfer of energy from a high-level point to a low-level point, usually from the output circuit of a device back to the input.

Ferractor® magnetic core. A transformer wound on a saturable core which exhibits a nearly rectangular hysteresis loop and which can be caused to assume either of two stable states.

Filter. A combination of circuit elements designed to pass a definite range of frequencies with low attenuation and to cause very high attenuation to all other frequencies. In power supplies, filters are used to smooth out the pulsating dc from the rectifier and produce a steady output.

Flip-flop. A circuit which assumes either of two stable internal states depending upon input conditions. In the magnetic computers, a flip-flop has two inputs, called set and restore, and one or more outputs. A set pulse places the circuit in one stable state. It remains in this state until it receives a restore pulse.

Force decimal carry. To generate signals that indicate a decimal carry when two digits are added that will produce a decimal carry.

Forward bias. A d-c potential applied across a PN junction of such polarity that current flows easily.

Full-wave rectifier. A circuit which utilizes both the positive and the negative alternations of an alternating current to produce a direct current.

Function signal. A signal generated by the instruction decoder or the function encoder to control the execution of an instruction.

Gate. A circuit or device whose output is generated only when every input signal is low. It performs the logical AND function.

General clear. The clearing of most controls, indicators, and flip-flops by the GENERAL CLEAR pushbutton on the control panel.

Half-wave rectifier. A circuit which passes one half of the input cycle and blocks the other half to produce pulsating dc.

Harmonic. An integral multiple of a fundamental frequency. (The second harmonic is twice the frequency of the fundamental, etc.)

Head. A magnetic core used for reading information from and writing onto a magnetic storage drum.

Head selection. That part of the search operation which determines the head that is to be used during reading or writing.

High signal. A definite positive voltage of approximately 16 volts peak.

Hole. A mobile vacancy in the electronic valence level of a semiconductor which behaves as if it had a positive charge and a mass equal to that of an electron.

Hysteresis loop (B-H curve). The curve exhibited by a magnetic material when magnetic flux density (B) is plotted as a function of the magnetizing force (H).

Impedance matching device. A device which, when connected between two transducers, matches the output impedance of one to the input impedance of the other in such a way that maximum power is transferred.

Improper division. A condition that occurs when the dividend is larger than the divisor.

Impurity. Atoms of a selected foreign substance which have been added substitutionally to a semiconductor crystal lattice.

Increductor. A saturable reactor in which dc flows through the control windings and ac flows through the signal windings. The dc produces a certain amount of saturation in the core. Hence the flux changes produced by the ac are not so great as they would be in the absence of dc, and the inductive effect of the signal windings is reduced. Incremental

changes in the inductance of the signal windings can be made by varying the operating point of the core, which is accomplished by changing the d-c level in the control windings.

Information. Any facts or data which can be processed, transferred, or communicated.

Information signal. A signal that represents a bit of a digit.

Information word. See word.

Initial force decimal carry. The generation of signals that indicate a decimal carry when no decimal carry has occurred. The signals are used during the arithmetic and comparison instructions and the search operation to alert the comparator and quinary-adder gates.

Input-output unit. A device through which information is fed into the system or through which information is delivered from the system.

Instruction. Information which tells the computer where to obtain the operands, what operations to perform, what to do with the result, and where to obtain the next instruction.

Instruction code. An artificial language for expressing the instructions to be carried out by the computer. The instruction code consists of two numeric characters.

Instruction digit. One of the two digits of the instruction code.

Instruction word. See word.

Ionization. A process which results in the formation of ions. Ionization by collision occurs in semiconductors when an electron is removed from an atom as the result of the energy gained in a collision with another electron possessing sufficiently large energy.

Jamming pulse. A signal, usually high, which forces a circuit, usually a flip-flop or counter, to a prescribed state.

Junction. A region of transition between semiconductor regions of different electrical properties; that is, between N-type and P-type semiconductor materials. The region is referred to as a PN junction.

Junction diode. A semiconductor diode whose nonsymmetrical volt-ampere characteristics result from the junction found between the N-type and P-type semiconductor materials.

Least significant digit. The lowest-order digit of a computer word or any other group of information containing more than one digit. It is always the digit farthest to the right in a computer word excluding the sign digit.

Left shift. To displace the digits of a word one or more places to the left, losing the most significant digits and replacing the least significant digits with zeros.

Logical circuitry. Circuitry designed to carry out the logical functions of gating, buffing, storage, delay, and inversion.

Logical drawing. A diagram showing, symbolically, the logical circuitry of the system without regard to electronic and wiring details.

Low signal. A zero voltage condition.

LSD. Abbreviation for least significant digit.

m address. The four digits of the instruction word which usually comprise the storage address of the operand to be used in the execution of the instruction.

Magnetic amplifier. A circuit built around a Ferractor ® magnetic core which amplifies and retimes a pulse. A magnetic amplifier delays the passage of a signal one-half pulse time. See complementer, noncomplementer, S-type and T-type noncomplementers.

Magnetic flux density (magnetic induction) (B). Magnetic induction is the basic observable property of the presence of a magnetic field. Although it is not a flow of charge, magnetic flux in a magnetic circuit is comparable with current in an electrical circuit. The quantity of flux is conventionally represented by imagining the lines of induction to be so spaced that the number of them through a given area is equal to the number of gauss or lines of flux (maxwells) per square centimeter.

Magnetic induction. See magnetic flux density.

Magnetic saturation. The condition of a magnetic material at high values of induction (magnetic flux density) in which the change in induction (B) is very small compared with the change in the magnetizing force (H). It is frequently thought of as the maximum magnetization of which a body or substance is capable.

Magnetic storage drum. A rotating cylinder upon which information in stored as magnetically polarized areas, usually along several parallel tracks around the circumference.

Magnetizing force (H). The applied magnetomotive force per unit length (ampere-turns/meter) required to provide the flux and the rate of change of flux specified by the conditions for which a dynamic hysteresis loop is determined.

Main storage. The area on the magnetic storage drum exclusive of the buffer storage bands, the timing band, and the sprocket track.

Matrix. Any logical network whose configuration is a rectangular array of intersections of its input-output leads, with elements connected at some of these intersections. The network usually functions as an encoder, decoder, or translator.

M buffers. See buffer. The M buffers are so named because their outputs are the M lines. The M buffers are used to transfer the contents of the registers and the magnetic storage drum to other processor circuits and vice versa.

Minority carrier. The type of carrier constituting less than half of the total number of carriers in a semiconductor; that is, electrons in P-type and holes in N-type.

M lines. The M buffer output lines. They distribute the M1 through M4 and the $\overline{M1}$ through $\overline{M4}$ signals.

Most significant digit. The highest-order digit of a computer word, or any other group of information containing more than one digit, excluding the SBW. It is always the leftmost digit of a word.

MQC. Abbreviation for multiplier-quotient-counter circuit.

MSD. Abbreviation for most significant digit.

Noncomplementer (noncomplementing amplifier). A non-inverting magnetic amplifier. The noncomplementer produces a high output signal from a high input signal and a low output signal from a low input signal. Compare complementer.

Noncomplementer, S-type. A special noncomplementer designed for use in arithmetic registers.

Noncomplementer, T-type. A special noncomplementer used as the next to the last stage in arithmetic registers.

Noncontinuous mode. A method of operating the system on an interrupted basis by pressing one of the NON-CONTINUOUS buttons on the operator's control panel. In this mode the system stops at predetermined points in the program.

Normal-access storage. Twenty bands of the magnetic storage drum with one head per track.

N-type semiconductor. See semiconductor.

Odd combination. A group of bits containing an odd number of ones.

Operand. Any one of the quantities entering into or resulting from an operation.

Operation

1. A process, usually mathematical.
2. The action of applying a mathematical or logical process.
3. The procedure of executing an instruction.

Overflow. The condition which arises when the result of an arithmetic operation exceeds ten digits (one word).

Override (the address). To force a search for the m address when the c address has been selected by the processor, or vice versa, by pressing the m or c pushbutton on the operator's control panel.

Package. The principal physical electronic module of the system. A package consists of a board upon which wiring is printed and components are mounted.

Parallel resonant circuit (tank circuit). A circuit composed of an inductance connected in parallel with a capacitance. In such a circuit the currents in the individual branches may be many times that in the line since they are out of phase and combine vectorially to give the line current. The impedance of a parallel resonant circuit is very high.

Parity check. A method of detecting erroneous recordings on the magnetic storage drum or printer code wheel by counting the number of 1 bits in each digit as it is read from the drum or code wheel.

Partial product. The product of any of the steps of the multiplication process except the last.

Peaking core (zero cross detector). A saturable reactor in which the core shifts from one state of saturation to the other very rapidly under the influence of even a small magnetizing force. As the operating point of the core undergoes these rapid shifts a sharply spiked voltage is induced in the output windings.

Permeability (μ). The capacity of a material to allow magnetic flux to penetrate or pass through it. Its magnitude equals the magnetic induction divided by the magnetizing force ($\mu = B/H$).

Permissive. Specifying the condition of a gate when all of its input signals are low.

Phase control unit. An integral part of the clock circuitry which maintains a 90-degree phase difference between the sprocket input signals and the clock output signals.

Phase detector (discriminator). A phase-sensitive circuit in which variations in the phase of the input signals determine the magnitude and polarity of the output voltage.

Phase splitter. A circuit which produces from the same input waveform two output waveforms which differ in phase from each other.

PN junction. See junction.

Position number. The alphanumeric notation assigned to the digit positions of a computer word; for example, p2.

Power pulse. A continuous sine wave approximately 40 volts peak-to-peak in amplitude which is required for the correct operation of certain series-pulse magnetic amplifiers.

Primed part. The two most significant bits of a card-code digit.

Principal carrier. The type of carrier constituting more than half of the total number of carriers in a semiconductor; that is, electrons in N-type and holes in P-type.

Print buffer. Two tracks on the magnetic storage drum that store information that is to be printed. See buffer storage.

Probe pulse. A negative-going spike of 0.1-microsecond duration which has a peak amplitude 2 volts below the +18-volt reference level. The signal is applied to the input gate of the RFF-S packages to permit the passage of sensed information only at the correct time.

Processor

1. Functionally, the section of the system that contains the control unit, magnetic storage drum, and arithmetic unit.
2. Physically, the unit that houses the computing and processing circuit packages, the magnetic storage drum, the operator's control panel, and the power supplies.

Program

1. A plan for the solution of a problem.
2. A set of instructions, routines, and subroutines arranged to cause the system to execute a sequence of operations.

Programmed stop. A stop resulting from a program instruction or subroutine that halts all computer operations at a predetermined place.

P-type semiconductor. See semiconductor.

Pulse time. The time necessary for one pulse to pass a given point in the circuitry.

Punch-through breakdown. An emitter-to-collector breakdown exhibited by junction transistors having a very narrow base region when sufficiently high collector voltages are applied to cause the space-charge layer to extend completely across the base region.

Quadrant. One fourth of a magnetic storage drum track or band.

Quadrant selection. The part of the search operation which selects the quadrant containing the desired address.

Quarter addition. Addition of binary digits with no carry.

Quinary bits. The three least significant bits of the four-bit UCT code. The bits are referred to as quinary bits because five different combinations of the three bits are used to represent the numerics 0 through 5. See binary bit.

Quinary carry. A carry resulting from the addition of quinary bits.

Quinary equality. Equality of the quinary bits of two quantities being compared.

Quinary value. The value of the quinary bits of a digit according to their decimal weights.

Read. To acquire information from the magnetic storage drum by means of heads or from punched cards by means of brushes. See also brush sensing.

Recirculation. The property of a register which enables it to return its contents to the input gates, providing a closed loop in which information is stored dynamically.

Record. To place information in storage by magnetizing areas of the magnetic storage drum. See write.

Rectifier. See full-wave rectifier, half-wave rectifier.

Register. A temporary storage device in which one computer word can be stored.

Register display. Forty lights on the operator's control panel which display the entire contents of a selected register in UCT code. Two extra lights are used to indicate the sign of the register contents on display.

Remanence. The residual flux present in a magnetic material when the magnetizing force is reduced to zero from a value sufficient to saturate the material.

Remington Rand code. See card code.

Restore. To place a flip-flop in a prescribed state, usually the logically quiescent state.

Reverse bias. A d-c potential applied across a PN junction of such polarity that only a small current flows.

Right shift. To displace the digits of a word in register A one or more places to the right into register X, and displace the digits of the word in register X an equal number of places to the right into register A. A circular shift.

Routine. A set of instructions arranged in the correct sequence to cause the system to perform a desired operation.

S buffers. See buffer. The S buffers are so named because their outputs are the S lines. The S buffers are used to transfer the contents of register A and register C to various other processor circuits.

SBW. The abbreviation for space between words, which is the pll position of a computer word.

Search. The step of the basic operation cycle during which a particular storage address is located.

Semiconductor, N-type. An extrinsic semiconductor in which the conduction electron density exceeds the hole density. The net ionized impurity content is donor type.

Semiconductor, P-type. An extrinsic semiconductor in which the hole density exceeds the conduction electron density. The net ionized impurity content is acceptor type.

Sense. To detect punched holes (information) on cards by means of brushes. See brush sensing.

Sentinel. A pulse, or combination of pulses, recorded in the timing band to control all the operations of the input-output units and the transfer of information between the input-output units and the processor.

Set. To place a flip-flop in a prescribed state, usually the state that is logically significant for action.

Shielding. A metallic covering used to prevent magnetic or electrostatic coupling between adjacent circuits.

Sine-wave clock. See clock.

S lines. The S buffer output lines. They distribute the S1 through S4 and the $\overline{S1}$ through $\overline{S4}$ signals.

Smoothing tank. A parallel resonant circuit which produces a sinusoidal output voltage even though the input voltage has an irregular waveshape.

Space-charge layer (depletion layer). A region near a junction which is void of current carriers. The mobile carrier charge density in this region is insufficient to neutralize the fixed charge density of the impurities.

Special search. A search for an information word or instruction word stored in a register (A, L, or $\overline{X}$) instead of on the storage drum.

Sprocket pulse. See sprocket signals.

Sprocket signals. Permanently recorded pulses on the sprocket track which produce a sinusoidal output of 2400 cycles per drum revolution. These signals drive the clock and, therefore, synchronize all computing circuits with the rotating drum.

Sprocket track. A track on the magnetic storage drum containing 2400 permanently recorded pulses that are read continuously. One sprocket pulse is provided for each bit position around the circumference of the magnetic storage drum. See sprocket signal.

Stacker. A mechanism that segregates processed cards into specified output bins.

Stage. See step, definition 1.

Static register. The register which stores the two instruction digits and generates signals which cause the instruction to be executed.

Staticize. To insert instruction code digits into the static register.

Staticize step. The step of the basic operation cycle during which the two instruction digits are placed in the static register and the entire instruction word is placed in register C.

Step

1. (noun) One phase of an instruction.
2. (verb) To advance a counter or flip-flop to its next state.

Stepping gate. A gate, the output of which sets the static register flip-flops 1 and 2 to advance the staticized instruction to the execution step.

Storage. Any device or circuit capable of retaining information, such as flip-flops, registers, magnetic storage drum.

Storage address. See address.

Storage drum. See magnetic storage drum.

Storage location. See address.

Storage switch. A switch which activates the heads to read or write information onto or from the magnetic storage drum.

S-type noncomplementer. See noncomplementer.

Subregister. One loop of a register capable of storing one bit of each digit of a computer word. Registers A, C, L, and X are each made up of four subregisters.

Subroutine. A sequence of instructions which causes the system to perform a well-defined operation. Several subroutines may be included in a routine.

Superimpose. To replace certain digits of a word with new digits according to a predetermined pattern.

Switch driver. A circuit whose output signal energizes a storage switch to enable reading or writing to take place.

Switch selection. The part of the search operation which determines which storage switch is to be energized.

Synchronizer. A logical circuit that controls the operations of an input-output unit and the flow of information between that input-output unit and the processor.

System error. An abnormal condition in any unit which causes the system to stop.

Tank circuit. See parallel resonant circuit.

Test (input-output). To determine whether a particular input-output unit is in use.

Thyratron. A hot-cathode, gas-discharge tube in which one or more electrodes are used to control electrostatically the starting of a unidirectional flow of current.

Timing band. A band of five tracks which controls the addressing of storage locations and the generation of timing signals in the cycling unit. Each of the 200 word-storage locations around the circumference of the magnetic storage drum is identified by a combination of digits permanently recorded in the timing band. See timing combination.

Timing combination. The bit combination (1101) that is permanently recorded in every timing band word location. The combination is read every word time to generate the timing signals in the cycling unit.

Timing signals. Signals generated by the cycling unit to time the internal operations of the system. Designated on logical drawings as t signals (for example, t11B).

Toroidal core. A magnetic core formed by winding thin wraps of magnetic tape on a bobbin in a tight continuous spiral.

Track. That part of a band of the magnetic storage drum which is available to a single head position.

Transducer. A device capable of being actuated by waves from one or more transmission systems or media, and of supplying related waves to one or more other transmission systems or media.

Transfer. The transmission of information from one place to another (for example, from magnetic storage drum to register or register to register). Also used as a verb.

Transistor-driving amplifier. A special magnetic amplifier the output of which is used to drive a transistor.

Translate. To convert information from one code to another without affecting the value or meaning.

T-type noncomplementer. See noncomplementer.

UCT code. The code in which information is recorded and processed within the central processor. The UCT code is a four-bit, biquinary code.

Unbarred signal. Any signal that is not overscored; for example, S1. It is always opposite in polarity to the corresponding barred signal; for example, $\overline{S1}$.

Unprimed part. The four least significant bits of a card-code digit.

Valence band. The band below the conduction band in a semiconductor. The range of energy states in the spectrum of a crystal in which lie the energies of the valence electrons which bind the crystal together. Hole flow takes place at the valence-band level.

Voltage divider. An impedance connected across a voltage source. The load is connected across a fraction of this impedance, and the load voltage is substantially in proportion to this fraction.

Weight. The decimal value of each bit in any bit code.

Word, computer. A group of 12 digits. The smallest unit of information that can be processed or stored by the system.

Word, data (information). A computer word consisting of ten information digits, a sign digit, and a space between words (SBW).

Word, instruction. A computer word consisting of the instruction code (two digits), the m address (four digits), the c address (four digits), a space-between-words position (SBW) (one digit), and the unused sign-digit position.

Word time. The time required for one word (12 digits) to pass a point in the circuitry. A word time is 12 pulse times or 17 microseconds in duration.

Write. To record information on the magnetic storage drum.

Write pedestal generator. A circuit whose output disconnects the read circuits when information is to be written onto the storage drum.

Zener voltage. See avalanche breakdown.

Zero cross detector. See peaking core.

Zero suppress. To eliminate all zero digits to the left of the most significant nonzero digit of a word.