

UNIVAC[®]
SOLID-STATE
90

Input Output Units

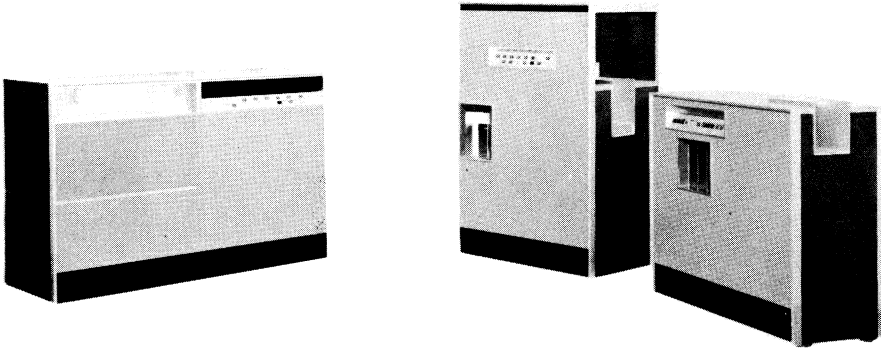


Remington Rand Univac
DIVISION OF SPERRY RAND CORPORATION

© 1959 - SPERRY RAND CORPORATION

CONTENTS

INTRODUCTION	1
90-COLUMN PUNCHED-CARD CODE	2
HIGH-SPEED READER	4
<i>General Description</i>	4
<i>Input Logic</i>	4
<i>Card Words</i>	7
<i>Timing Mechanism</i>	10
<i>Programming the Operation Cycle</i>	11
<i>Input Checking Routine</i>	15
<i>Error Conditions</i>	15
<i>Efficient Utilization of the High-Speed Reader</i>	16
READ-PUNCH UNIT	19
<i>General Description</i>	19
<i>Input-Output Logic</i>	20
<i>Card Words</i>	23
<i>Programming the Operation Cycle</i>	25
<i>Modes of Operation</i>	29
<i>Program Checking</i>	30
<i>Error Conditions</i>	31
HIGH-SPEED PRINTER	33
<i>General Description</i>	33
<i>Output Logic</i>	33
<i>Print Mechanism</i>	35
<i>Programming the Operation Cycle</i>	37
<i>Error Conditions</i>	40
STOP SUB-ROUTINES	43
<i>General Description</i>	43
<i>Contents of the Stop Routine</i>	43
<i>Operating Logic</i>	43



This manual is a reference in writing input and output program routines for the Remington Rand UNIVAC Solid-State 90. It contains basic and detailed functional descriptions of the **HIGH-SPEED READER**, **READ-PUNCH UNIT**, **HIGH-SPEED PRINTER** and the program instructions which control these units. An explanation of the Remington Rand 90-column punched-card code, an important programming prerequisite, and the buffer system and input/output logic of each unit is also included. The complete program instruction repertoire, programming techniques, and other detailed programming information is contained in separate publications.

90-COLUMN PUNCHED-CARD CODE

GENERAL DESCRIPTION

The Remington Rand punched-card, Figure 1, is composed of an Upper Field (UF) and a Lower Field (LF). Because there are 45 punch columns in each of the two fields, the Remington Rand card is referred to as a 90-column card. The columns comprising the Upper Field are numbered one through 45; the Lower Field columns are numbered 46 through 90.

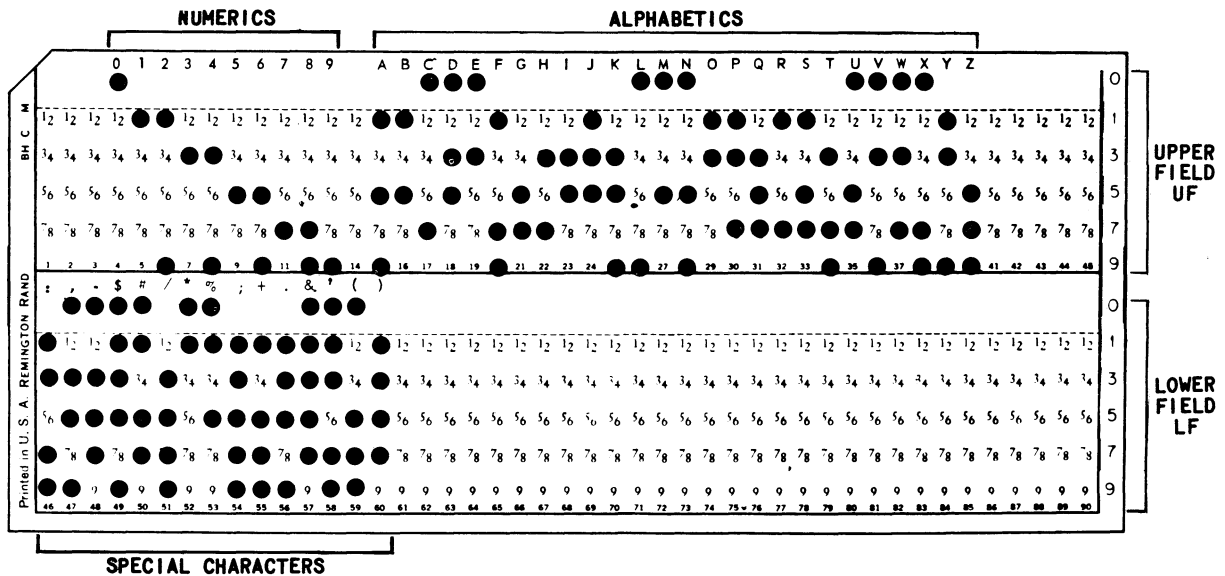


Figure 1 Remington Rand Punched Card and Card Code

Both the Upper and Lower Fields contain six rows numbered: 0, 1, 3, 5, 7, and 9. These numbers are called the card row punch positions. There are a total of 540 punch positions in each Remington Rand 90-column punched-card (45 columns per field X 6 card row positions per column X 2 fields = 540 punch positions).

NUMERIC REPRESENTATION

Zero and odd decimal values are represented in 90-column card code by a single punch in the appropriate card row punch position of a column. Zero, for example, is represented by a punch in the 0 punch position of a column (See column 4, Figure 1). Three is represented by a single punch in the 3 position of a column, five by a single punch in the 5 position of a column, and so on.

Even decimal numbers are represented by punches in two card row positions of a column. One of the punches is always in the 9 row position, the other is in either the 1, 3, 5, or 7 position depending upon the even decimal value to be represented. A decimal two is represented by punches in the 1 and 9 row positions of a column (See column 6, Figure 1). A decimal four is represented by punches in the 3 and 9 row positions; a decimal six by punches in the 5 and 9 row positions, and so on.

Because the 1, 3, 5, 7, and 9 row punch positions are used to indicate odd or even decimal values, depending upon whether a punch is present in the 9 row punch position, each individual punch position in a 90-column card is marked (1₂, 3₄, 5₆, etc) to indicate the complete potential of each punch position.

ALPHABETIC REPRESENTATION

Alphabets are represented by varying combinations of two and three punches in a particular card column. Figure 1 contains the 90-column card punch codes for each of the 26 characters of the alphabet.

SPECIAL CHARACTER REPRESENTATION

Special characters are represented in 90-column card code by varying combinations of from two to five punches in a card column. Figure 1 contains the punch codes for the 15 special characters representable in 90-column card code.

HIGH-SPEED READER

GENERAL DESCRIPTION

The High-Speed Reader is the major input source of the UNIVAC Solid-State 90. It reads information punched into 90-column cards at speeds of up to 450 cards per minute. The High-Speed Reader is composed basically of an input magazine, two card read stations (Read 1 and Read 2) and three output card stackers. The input magazine will contain up to 1000 cards; each of the three output stackers will contain as many as 1200 cards.

An input card is read at the Read 1 and is transported to Read 2 where it is read again. The information read at both read stations is transferred to a special area on the storage drum (Central Processor) called the card buffer. From the card buffer, the information is transferred into the main storage area of the drum where it is available for use according to the program. Figure 2 provides a simple diagram of the input operation of the High-Speed Reader.

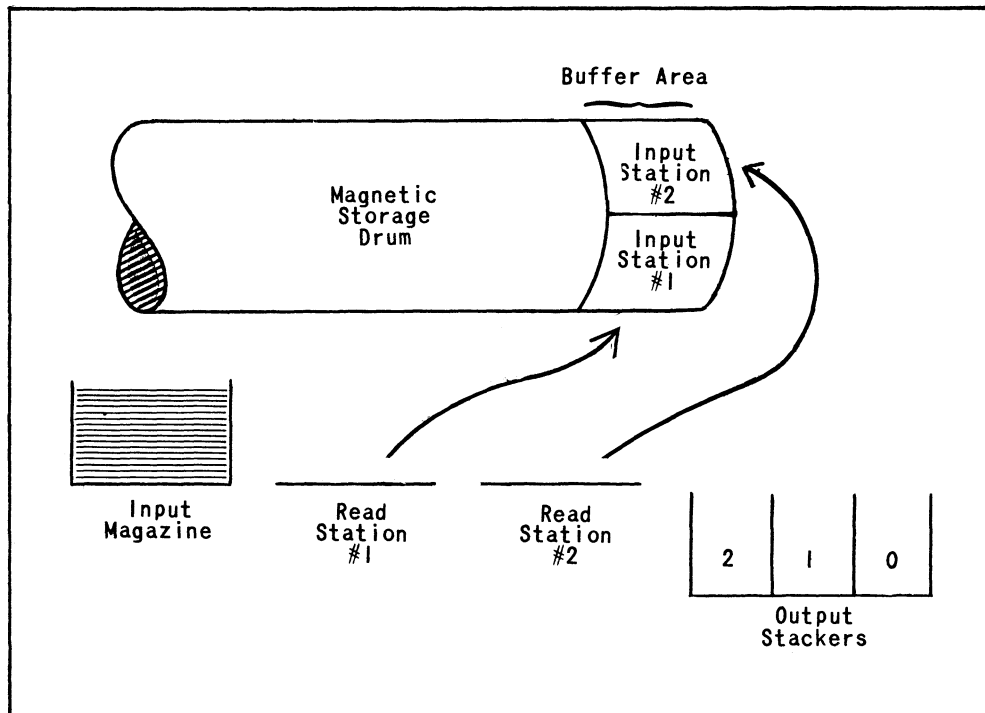


Figure 2 Functional Diagram Of The High-Speed Reader

INPUT LOGIC

Data cards entering the UNIVAC Solid-State 90 from either input unit normally contain information recorded in 6-bit Remington Rand card code. (Input cards may contain information recorded in 4-bit binary code of the computer). Figure 1 shows the 51 alphabetic, numeric, and special characters that may be punched in 90-column card code.

As cards enter the system, the presence of a punched hole indicates a binary one bit; the absence of a punched hole indicates a zero (no bit present). Figure 3 illustrates how the presence or absence of punched holes in a card are interpreted as binary ones and zeros.

<u>Card Row Positions</u>	<u>Binary Representation</u>
0	1 0 0 0 0 0 0 0 0 0
1	0 1 1 0 0 0 0 0 0 0
3	0 0 0 1 1 0 0 0 0 0
5	0 0 0 0 0 1 1 0 0 0
7	0 0 0 0 0 0 0 1 1 0
9	0 0 1 0 1 0 1 0 1 1
Decimal Value =	0 1 2 3 4 5 6 7 8 9

Figure 3 Numeric Card Code

Card Sensing

Under control of a program instruction (72), a card is transported from the input magazine into the roller mechanism of the Reader. Once the card movement is initiated, the card is automatically read at Read 1, then at Read 2, and finally is segregated into one of the output stackers. Read 2 enables the programmer to program comparisons with Read 1 to assure complete data identity and validity.

Normally, cards are fed continuously through the High-Speed Reader so that cards are being read simultaneously at Read 1 and Read 2. Each row of a card is read as the card moves under the 45 brushes at each read station. The first row read consists of the least significant bits of all digits in the Upper Field of the card; the next row read consists of the next higher-order bits, and so on. Therefore, six rows of a card must be sensed before complete characters are read.

After the six rows of the Upper Field have been read, the 45 brushes sense the six rows of the Lower Field.

Each time a card row passes under the read brushes, a pulse is placed on a roller beneath the card. Each brush which has a hole under it at the time the roller is pulsed receives a pulse from the roller. This pulse is equivalent to a binary 1 bit. Each brush which does not have a hole under it is insulated from the charged roller by the card. The insulation prevents a pulse from being placed on the brush. This lack of a pulse is equivalent to a binary 0 bit for that punch position.

Stacker Selection

After a card has passed Read 2, it moves to one of the three output stackers (See Figure 2). Stacker selection is made by the programmer through the use of a 47 instruction.

Capacitor Storage

Information read at Read 1 and Read 2 is first sent to a temporary storage called capacitor storage (Figure 4). Capacitor storage is capable of storing one row from the Read 1 and one row from the Read 2. Before the next card rows are read at both read stations, the information in capacitor storage is recorded in a special area of the magnetic storage drum called buffer storage.

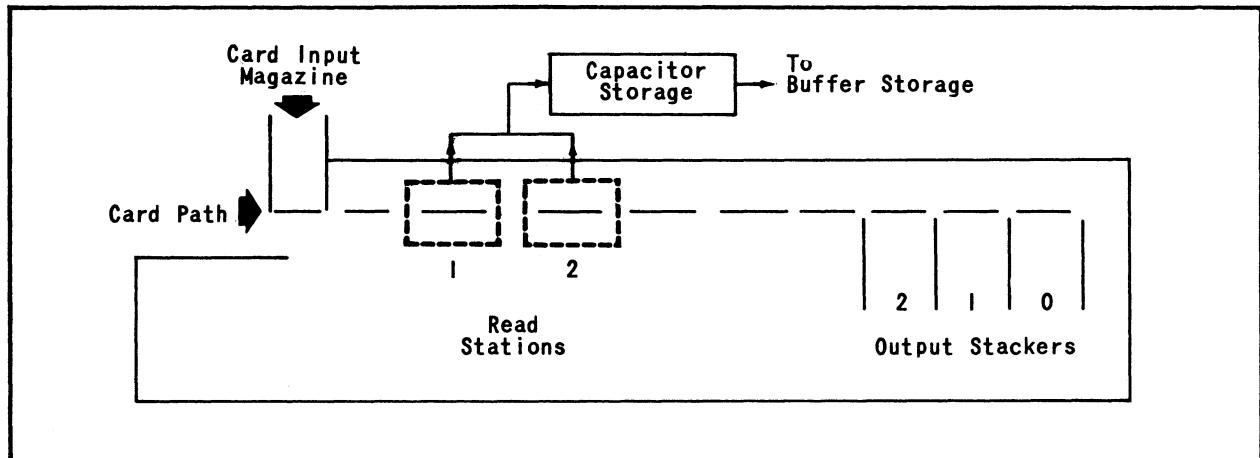


Figure 4 Functional Diagram of Card Movement in High-Speed Reader

Card Buffer Storage

The card buffer band on the magnetic storage drum is used to store information temporarily during input-output operations. As an intermediate storage between capacitor storage and main data storage, the card buffer band is necessary because of the difference in operating speeds of the relatively slow input-output units and the faster operating Central Processor. It also provides a storage area in which to assemble into complete words the information read row-by-row from the cards.

The card buffer storage band is used by both the High-Speed Reader and the Read-Punch Unit. Although it is not part of main storage, the card buffer contains 200 word locations, the same as any of the 25 main storage bands. Locations 000-099 serve the High-Speed Reader; locations 100-199 serve the Read-Punch Unit. (Only those operations concerning the High-Speed Reader portion of the buffer are presented in this section).

While information being read at Read 1 and Read 2 of the High-Speed Reader is being recorded in buffer storage, the Central Processor is free to execute other instructions. The read-write circuits which serve main storage are not involved in a transfer of information from the Reader to the buffer.

After the data in the cards being read at both read stations has been completely recorded in the buffer (instruction 72), another instruction (96) transfers the information to a predetermined band in main storage. This transfer can be accomplished in one drum revolution.

CARD WORDS

As stated previously, data cards entering the UNIVAC Solid-State 90 from either input unit normally contain information recorded in 6-bit Remington Rand card code. Ten 10-digit computer words can be punched into one 90-column card in card code, five words in the Upper Field and five in the Lower Field. Each card field contains four 10-digit words and one 5-digit word as shown in Figure 5.

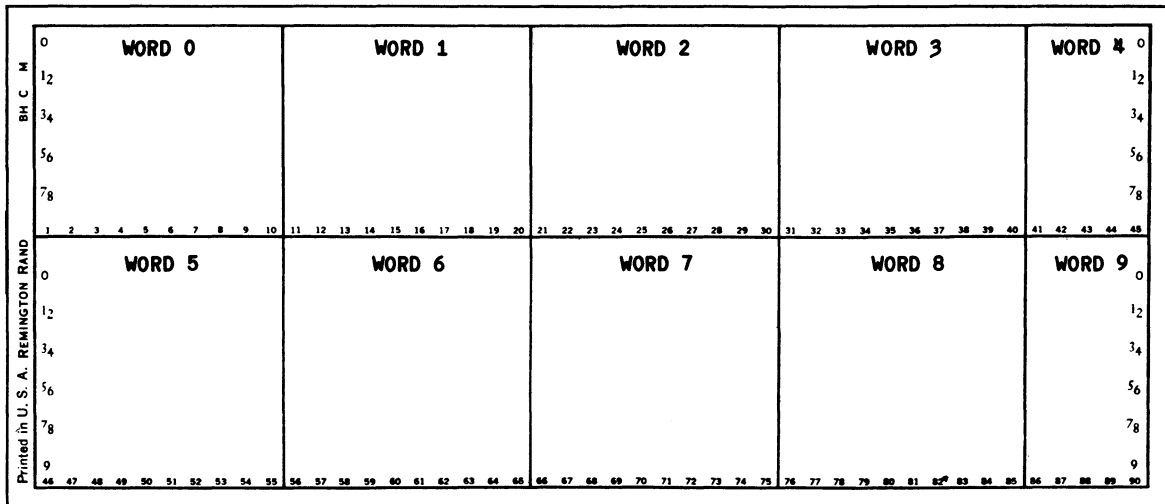


Figure 5 Basic Format of Card Words

Although words 4 and 9 contain only five digits of information, they are considered for computational purposes as 10-digit words.

Primed and Unprimed Card Word Parts

To store a word recorded in card code in either buffer storage or main storage, (words are stored in 4-bit computer code), the card word (six bits per digit) is divided into two parts, a primed word part and an unprimed word part.

Figure 6 shows a 10-digit word composed entirely of numeric characters. The unprimed part of each digit in the word is composed of the four bits in card row positions 0, 1, 3, and 5 (lower-order bits). The unprimed word part can be stored in one computer storage location because it is exactly the size of a 10-digit, 4-bit computer word.

Card Code				Decimal Value		
9	7	5	3	1	0	
0	0	0	0	0	1	= 0
0	0	0	0	1	0	= 1
1	0	0	0	1	0	= 2
0	0	0	1	0	0	= 3
1	0	0	1	0	0	= 4
0	0	1	0	0	0	= 5
1	0	1	0	0	0	= 6
0	1	0	0	0	0	= 7
1	1	0	0	0	0	= 8
1	0	0	0	0	0	= 9
Primed Part		Unprimed Part		Word		

Figure 6 Card Coded Word (10 Digits)

The primed word part, composed of the bits in card row positions 7 and 9, is stored in a second storage location. Two bits of the primed word part are unused.

Figure 7 on page 9 is the complete 90-column card code and computer code table for all alphabetic, numeric, and special characters. Primed and unprimed parts of each character are noted and separated. The two XX's under the prime word column indicate the unused bit positions.

Card Word Identification

The 72 instruction causes an input card to be moved from the input magazine through both read stations, and the primed and unprimed word parts to be placed in buffer storage. The 96 instruction causes the card data to be moved from the buffer to main storage. To enable the programmer to identify each word part (primed and unprimed) and the main storage location it will occupy, the card words, illustrated in Figure 5, are given more definitive notations as shown in Figure 8.

J = Unprimed portion of word
 J' = Primed portion of word
 1st digit of subscript = Read station where data is sensed
 2nd digit of subscript = Word number

Printed in U. S. A. REMINGTON RAND	B H C M	WORD 0	WORD 1	WORD 2	WORD 3	WORD 4																																							
	0					0																																							
	12					12																																							
	34	J ₁₀ J ₂₀	J ₁₁ J ₂₁	J ₁₂ J ₂₂	J ₁₃ J ₂₃	J ₁₄ J ₂₄	34																																						
56						56																																							
78	J' ₁₀ J' ₂₀	J' ₁₁ J' ₂₁	J' ₁₂ J' ₂₂	J' ₁₃ J' ₂₃	J' ₁₄ J' ₂₄	78																																							
1	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45
0	WORD 5	WORD 6	WORD 7	WORD 8	WORD 9	0																																							
12						12																																							
34	J ₁₅ J ₂₅	J ₁₆ J ₂₆	J ₁₇ J ₂₇	J ₁₈ J ₂₈	J ₁₉ J ₂₉	34																																							
56						56																																							
78	J' ₁₅ J' ₂₅	J' ₁₆ J' ₂₆	J' ₁₇ J' ₂₇	J' ₁₈ J' ₂₈	J' ₁₉ J' ₂₉	78																																							
9						9																																							

Figure 8 Primed and Unprimed Parts of Card Coded Word

Card Code to Machine Code

Machine Code to Card Code

Character	<u>Card Code</u>		<u>Machine Code</u>		<u>Machine Code</u>		<u>Card Code</u>	
	Unprime	Prime			Bit. Combo.	Unprime	Prime	
	<u>5310</u>	<u>XX97</u>				<u>5310</u>	<u>XX97</u>	
0	0001	0000	0000	0000	(0)	0001	0000	
1	0010	0000	0001	0001	(1)	0010	0000	
2	0010	0010	0010	0010	(2)	0010	0010	
3	0100	0000	0011	0011	(3)	0100	0000	
4	0100	0010	0100	0100	(4)	0100	0010	
5	1000	0000	1000	1000	(5)	1000	0000	
6	1000	0010	1001	1001	(6)	1000	0010	
7	0000	0001	1010	1010	(7)	0000	0001	
8	0000	0011	1011	1011	(8)	0000	0011	
9	0000	0010	1100	1100	(9)	0000	0010	
A	1010	0010	1011	1010		0110	0010	
B	1010	0000	1001	0110		0110	0010	
C	0001	0001	1010	0111		0100	0010	
D	1101	0000	1011	1101		0000	0010	
E	0101	0000	0011	1110		0000	0011	
F	0010	0011	1011	1111		0000	0011	
G	1000	0001	1010					
H	0100	0001	1011					
I	1100	0000	1011					
J	1110	0000	1011					
K	1100	0010	1101					
L	0001	0010	1100					
M	1001	0000	1000					
N	1001	0010	1001					
O	0110	0000	0011					
P	0110	0001	1011					
Q	1100	0001	1011					
R	0010	0001	1011					
S	1010	0001	1011					
T	0100	0011	1111					
U	1001	0001	1010					
V	0101	0010	0100					
W	0101	0001	1011					
X	0001	0011	1011					
Y	0110	0010	0110					
Z	1000	0011	1011					
Space	0000	0000	0000					
:	0110	0011	1111					
,	1101	0010	1101					
\$	1111	0010	1111					
-	1101	0001	1011					
#	1011	0001	1011					
*	0011	0000	0001					
%	1011	0000	1001					
;	1110	0011	1111					
/	1100	0011	1111					
+	1010	0011	1011					
.	1110	0010	1111					
&	1111	0001	1011					
'	0111	0011	1111					
(1001	0011	1011					
)	1110	0001	1011					

Figure 7 Card Code And Computer Code Table

The meanings of these additional notations are as follows:

J = unprimed word part
 J' = primed word part

1st digit of subscript = read station where card data was sensed
 2nd digit of subscript = word number.

Data transferred from buffer to main storage is placed in specific main storage locations within a card input/output interlace. (Figure 12, page 18.) The word positions within main storage are not sequential, but are spread at intervals of 20 storage locations on the drum. This allows minimum latency access.

The fixed interlace pattern allows the programmer to identify the storage location of each word part within a particular storage band. In programming the buffer to main storage transfer, the programmer may specify only the storage band into which the card data is to be placed. However, as stated previously, the storage locations within the band are fixed. For example, Word 0 of an input card is always placed in a particular storage band in the following interlace pattern:

<u>Unprimed Word</u>	<u>Primed Word</u>	<u>Word #</u>	<u>1st Read</u>	<u>2nd READ</u>	<u>Band</u>	<u>Storage</u>
J		0	1		Var.	001 (J10)
J		0		2	Var.	011 (J20)
	J'	0	1		Var.	006 (J'10)
	J'	0		2	Var.	016 (J'20)

TIMING MECHANISM

Each time a row of a card is read at a read station, the roller underneath the card is pulsed during the time that the row of the card is being probed by the sensing brushes. When a row is not being probed by the brushes, or when there is no card in the read stations, the roller remains de-energized. The pulse placed on the roller when a row is read is called the probe signal and is generated by High-Speed Reader synchronizing circuits.

To probe the roller (sense the card) at the correct time, generation of the probing pulse must be synchronized with the movement of the card. Synchronization is maintained by the timing disc and the synchronizer (Figure 9).

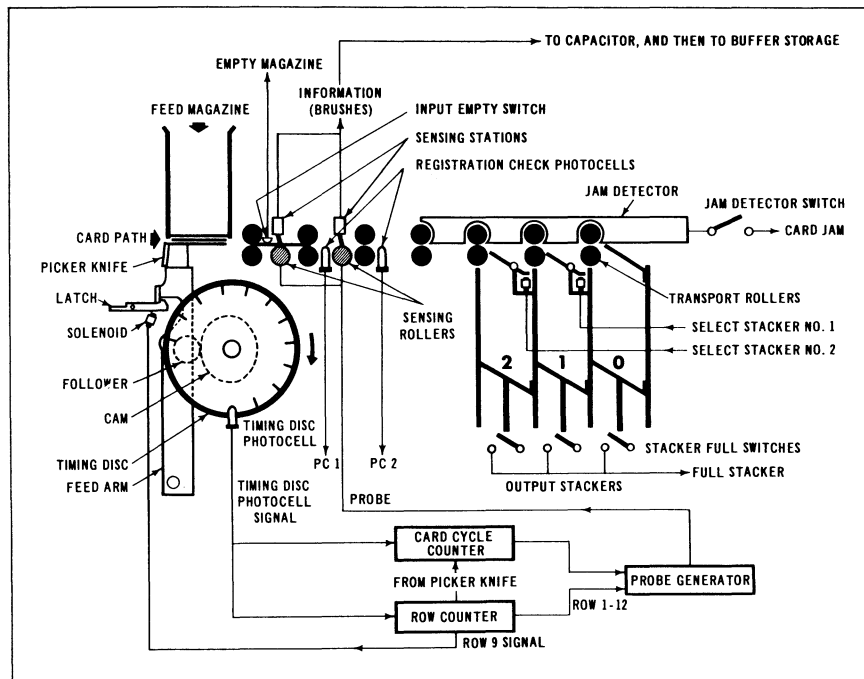


Figure 9 Electromechanical Schematic of Card Reader

The timing disc contains 12 slots located at intervals of 24 degrees around its circumference. A portion of the timing disc between the first and last slot (96 degrees) does not contain slots and is referred to as the gap. While the High-Speed Reader is operating, the timing disc rotates and generates timing-disc photocell signals each time a slot passes between the photocell and its lamp. The timing disc rotates once for each card pass (card cycle) and generates 12 photocell signals per card, one for each row on the card. The photocell signals generate pulses which probe both read stations simultaneously and thus read the cards. If no card is in the read station, the photocell signals do not generate any probe signals.

Information from the read stations is assembled row-by-row in the card buffer band. It remains there until an instruction (96) transfers it to main storage. If no instruction is given, the next input instruction (72) will cause processing to stop. Both of these operations (data transfers from stations to buffer and from buffer to main storage) are explained in detail in the following sections.

PROGRAMMING THE OPERATION CYCLE (See Figure 11 on page 17)

From the time input cards are placed in the input magazine of the High-Speed Reader until the time the information they contain is made ready for processing in main storage, the programmer makes use of four program instructions. These instructions, their basic functions, and the word time required for their execution are listed on the following page. In these descriptions, and throughout the remainder of this manual, the following conventions and abbreviations are used:

Next Card Cycle

The next 81 instruction must be given at least 3.5 milliseconds (assuming that the instruction is located in its minimum latency location which is $0198 + 201n$) preceding the point at which the next punch set-up operation would start. This instruction should be given at least 264 milliseconds after the point at which the previous punch set-up started (giving a range of 132.5 milliseconds during which an 81 instruction may be given), if it is to be preceded by a test instruction (22).

Actually, a card cycle instruction (81) may be given 140 milliseconds after the punch set-up operation is started (i.e. the point at which the punch set-up is completed), but there is no test instruction by which the programmer can determine this point. Hence, the programmer must wait until 264 milliseconds following the point at which the punch set-up started in order to use the test instruction. This insures that the card cycle instruction (81) can be given legitimately.

In unusual circumstances, it is possible that the programmer could time the 140 milliseconds by programmed operations and thus give the 81 instruction before the point at which the test instruction would pass. This however is not recommended. If the 81 instruction is not given early enough (at least 3.5 milliseconds before the proper point in the mechanical card cycle for the punch set-up to start) the time loss will be some function of how late the instruction is given, but not a linear function.

Stacker Selection

The stacker selection instruction (57) may be given during the 116 millisecond range starting 140 milliseconds after the start of the previous punch set-up operation. The 57 instruction must be given 20 milliseconds before the point at which the next punch set-up operation starts.

MODES OF OPERATION

The Read-Punch Unit has three basic modes of operation: 1) as a Read Unit only, 2) as a Punch Unit only, and 3) a combination of modes one and two.

Read Unit Only

In using the Read-Punch Unit as an input device only, every card cycle (81) instruction will activate all portions of the unit for the following operations:

- 1) The sensing of information at Read Stations 1 and 2.
- 2) The transfer of information located in the punch interlace positions to the punch positions of the card buffer. (The punch interlace positions are specified by a given band in the "m" portion of the 81 instruction.)

Card Cycle

When the High-Speed Reader is energized, the electromechanical system that transports the card through the card read cycle begins to function. A card is not sent through the Reader, however, until a 72 instruction (card cycle instruction) activates the picker knife which transports one card from the card feed magazine into the roller mechanism. Once the 72 instruction is given and the card enters the feed rollers, the programmer has no further control over the movement of the card until it reaches the selected output stacker. The programmer cannot control the data read from the card until it is completely accumulated in the buffer storage as a result of the 72 instruction.

The 96 instruction transfers both sets of input data from fixed locations on the buffer band to the interlace pattern in any desired band (specified in m in the instruction word) in the main drum storage.

Thus, input by the High-Speed Reader is accomplished by the use of the 72 (transfer from card to buffer) and 96 (transfer from buffer to main storage) program instructions.

Card-to-Buffer Transfer

The maximum feed rate in the High-Speed Reader is 450 cards per minute. The operations in the High-Speed Reader are overlapped so that the card in Read 1 and the card in Read 2 are both read simultaneously during each card cycle. These operations in the High-Speed Reader are all overlapped with computation, printing, and reading or punching by the Read-Punch Unit.

The mechanical card cycle operation (Figure 9) is initiated at specific intervals as determined by a continuously rotating cam (See Timing Mechanism section). Interlocks are provided for the card cycle (72 instruction) and the buffer-to-main storage transfer (96 instruction) to insure synchronization of the Central Processor with the High-Speed Reader. There are no stops in the High-Speed Reader card transport mechanism so that once the 72 instruction causes a card to be fed from the card feed magazine into the continuously moving rollers, the card cannot be stopped until it reaches the selected output stacker.

When a 72 instruction is given, the computer immediately stores an indication of this in a flip-flop which causes the picker knife to be actuated at the proper time (determined by the rotating cam) to feed the next card from the input magazine. When this flip-flop has been set, the Central Processor is free to operate on other instructions so that the normal execution time of the 72 instruction is only three word times. The signal to the picker knife resets the card cycle flip-flop. If the flip-flop is set when a 72 instruction is given (the flip-flop has not yet been signalled for the previous instruction) the Central Processor transfers control to the m address and the contents of rC is transferred to rA.

Buffer-to-Main Storage Transfer

The buffer-to-main storage transfer instruction (96) is interlocked by another flip-flop (buffer-loaded flip-flop) which indicates whether or not the buffer is loaded. When a 96 instruction is given, the computer is interlocked if the buffer is not loaded or if there is not a card under either set of read brushes.

A test instruction (42) is provided which samples the flip-flop to determine when the buffer loading is completed. Since cards are not stopped between the two read stations, it is imperative that the programmer give the 96 instruction in time for it to be completed before the point at which sensing of the next card begins.

To safeguard against the possibility of losing the card images, an "Alert 96" button is provided on the operating panel of the Central Processor. When this button is depressed, the Central Processor will stop if the buffer was not unloaded at the proper time. If a 96 instruction is given with only one card present in either read station, the buffer interlace locations of the station not occupied will read all binary one's.

Buffer Load Test

Figure 10 is a functional diagram of the operating cycle of the High-Speed Reader. "A" equals the range during which a 42 (buffer load test) instruction may be passed. A 96 instruction may be given during the range except during the last 3.5 milliseconds of the range. The completion of a 96 instruction given during the range resets the buffer loaded flip-flop which is otherwise reset by the sensing of the next row 1. This would interlock another 96 instruction during this range.

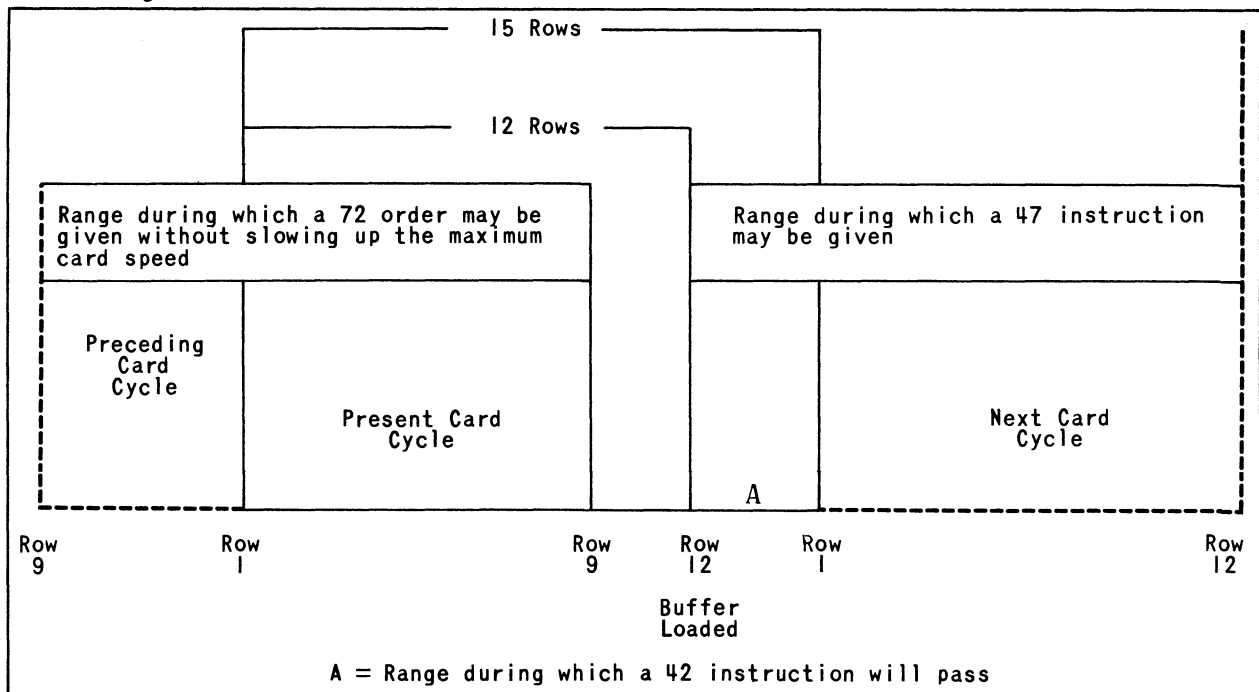


Figure 10 Functional Diagram of Operating Cycle

In Figure 10, the point at which the first row of the card is sensed is taken as the start of the card cycle and the reference point from which other points in the card cycle are timed. Twelve rows from this reference point, the buffer will be loaded with the sensed data of the card. Section A of the diagram indicates that a 42 instruction given anytime during the three row-times following the buffer being loaded will find the buffer loaded flip-flop set and will then transfer the contents of rC to rA and transfer control to the location specified by the m address part of the test instruction (42).

If, however, the test instruction is given during the last 3.5 milliseconds of the A range, the 96 instruction will bring in incorrect information.

Stacker Selection

The stacker selection instruction (47) for the card in Read 2 may be given after the buffer is loaded, but must be given before the start of sensing in row 12 of the following card in Read 2.

To maintain maximum card speed, the 72 instruction must be given during the range of 15 rows preceding the end of reading of row 9 of the present cards in the read stations. This includes 9 rows of the present card cycle and 6 rows of the previous card cycle. The actual operation of the picker knife, however, is not until row 3 of the next card cycle and the card does not arrive at the first set of sensing brushes until 12 row-times later. (See Figure 11 for timing.)

INPUT CHECKING ROUTINE

Programmed input checks are incorporated into the High-Speed Reader routine. If the programmer elects to code his own routine, rather than utilize the existing routines supplied by Remington Rand, this operation can be designed as follows:

Compare (for equality) the first and second read interlace positions of the card. Read 1 data will be on the band chosen by the programmer on the buffer-to-main storage transfer for the first card; Read 2 data will be on an alternate band. This comparison can be programmed in minimum latency, and will allow time for stacker selection in case of a discrepancy between Read 1 and Read 2 of any card.

If the computer is to be stopped in the event of a comparison discrepancy, a "halt" routine, similar to that provided in the input routine, must be provided. This protects any information which may have accumulated for punching or printing in the main program, or stored in back-up storages for output.

ERROR CONDITIONS

There are four basic error conditions which may occur during operation of the High-Speed Reader. They are:

1. Empty input magazine.

2. Bad card registration at the read stations.
3. Full output stacker.
4. Card jam.

In each case, the succeeding 96 instruction after the condition has occurred will cause the computer to select the instruction word located at storage location $c+1$. The program should be designed to transfer a stop instruction word to rX . This instruction word identifies the error and supplies the address where the next instruction will be located after the error has been corrected.

The program should then enter the stop subroutine of the High-Speed Reader routine which will permit saving of any data in the other input/output units. If the programmer wishes to ignore this condition, it is possible to do so by supplying a "skip" to the routine to be entered as the $c+1$ address.

EFFICIENT UTILIZATION OF THE HIGH-SPEED READER

The High-Speed Reader can be programmed to operate at rates of up to 450 cards per minute. The Read-Punch Unit can be programmed to operate at rates of up to 150 cards per minute. Since the operation of both units can be overlapped, an operating ratio of three-to-one, or better, for these units can be achieved. Therefore, wherever possible, the programmer should keep the High-Speed Reader operating at full speed in order to obtain efficient equipment utilization. This, in turn, requires consideration in the areas of system design and machine programming.

System Design

During the initial design of a computer run, consideration should be given to which input units will receive the bulk of the input data. Wherever possible, the programmer should use the High-Speed Reader as the basic input device.

When the Read-Punch Unit is utilized as combined input/output, it is possible to limit the speed of the Reader and thus impair the overall efficiency of the computer operation. For example, where results are punched into every second card in the Read-Punch Unit, output efficiency will drop 50% even though the cards are transported through the unit at 150 per minute. Therefore, overall computer efficiency will be adversely affected unless there is an average of six cards per punched result being processed through the High-Speed Reader.

Programming Techniques

In all runs which use the High-Speed Reader, the programmer should consider methods of keeping the Reader operating at the maximum speed consistent with the processing and output. This can be accomplished through programming techniques such as extending the buffer storage. In this case, reserve areas are allocated in storage to store raw data until ready for processing. It is necessary to remember that the law of supply and demand applies here; any gain in read speed will consume additional memory space for both stored programs and data.

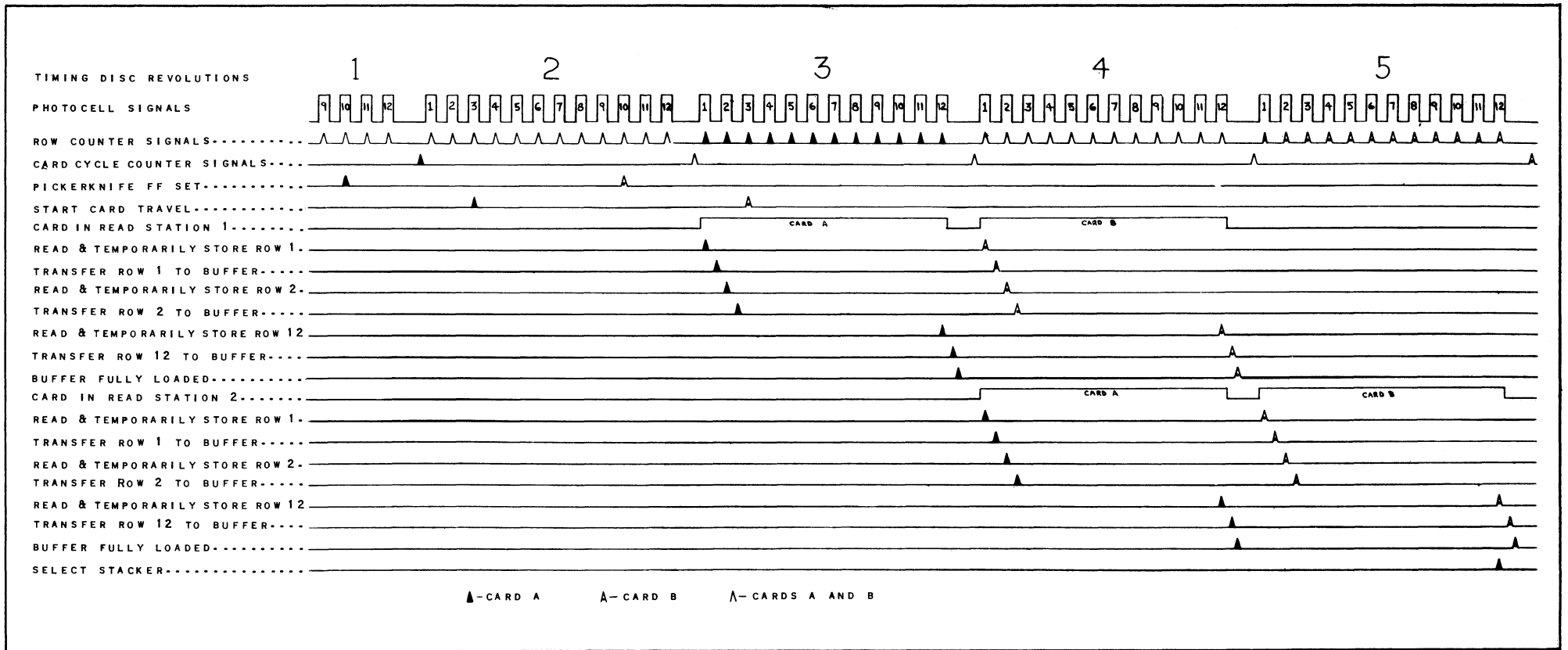


Figure II General Timing Diagram

STORAGE LOCATION OOXX		STORAGE LOCATION O1XX	
00	50	00	50
01 J10	51 J22	01	51
02	52	02 J15	52 J27
03	53	03	53
04	54	04	54
05	55	05	55
06 J'10	56 J'22	06	56
07	57	07 J'15	57 J'27
08	58	08	58
09	59	09	59
10	60	10	60
11 J20	61 J13	11	61
12	62	12 J25	62 J18
13	63	13	63
14	64	14	64
15	65	15	65
16 J'20	66 J'13	16	66
17	67	17 J'25	67 J'18
18	68	18	68
19	69	19	69
20	70	20	70
21 J11	71 J23	21	71
22	72	22 J16	72 J28
23	73	23	73
24	74	24	74
25	75	25	75
26 J'11	76 J'23	25	76
27	77	27 J'16	77 J'28
28	78	28	78
29	79	29	79
30	80	30	80
31 J21	81 J14	31	81
32	82	32 J26	82 J19
33	83	33	83
34	84	34	84
35	85	35	85
36 J'21	86 J'14	36	86
37	87	37 J'26	87 J'19
38	88	38	88
39	89	39	89
40	90	40	90
41 J12	91 J24	41	91
42	92	42 J17	92 J29
43	93	43	93
44	94	44	94
45	95	45	95
46 J'12	96 J'24	46	96
47	97	47 J'17	97 J'29
48	98	48	98
49	99	49	99

Figure 12 High Speed Reader Interlace Pattern

GENERAL DESCRIPTION

The Read-Punch Unit of the UNIVAC Solid-State 90 is a dual purpose unit capable of both sensing and punching Remington Rand 90-column punched-cards. It is composed basically of a card input magazine, a first read station (Read 1), a punch station, a second read station (Read 2) and two output card stackers.

Under normal operating conditions, the Read-Punch Unit processes cards at a speed of 150 cards per minute. Prepunched or blank cards are first sensed at Read 1. The sensed information is placed in capacitor storage and then sent to a special area on the magnetic drum (Central Processor) called the card buffer storage. From the card buffer, the information is transferred to main storage where it is available for processing according to the program. The processed information is then returned to the Read-Punch Unit and punched into cards at the punch station. The cards are then read at Read 2 to provide opportunity to check the identity and validity of both the Read 1 and card punch operations. Finally, the cards are sorted into the output stacker prescribed in the program. Figure 13 is a simple diagram of the input-output operation of the Read-Punch Unit.

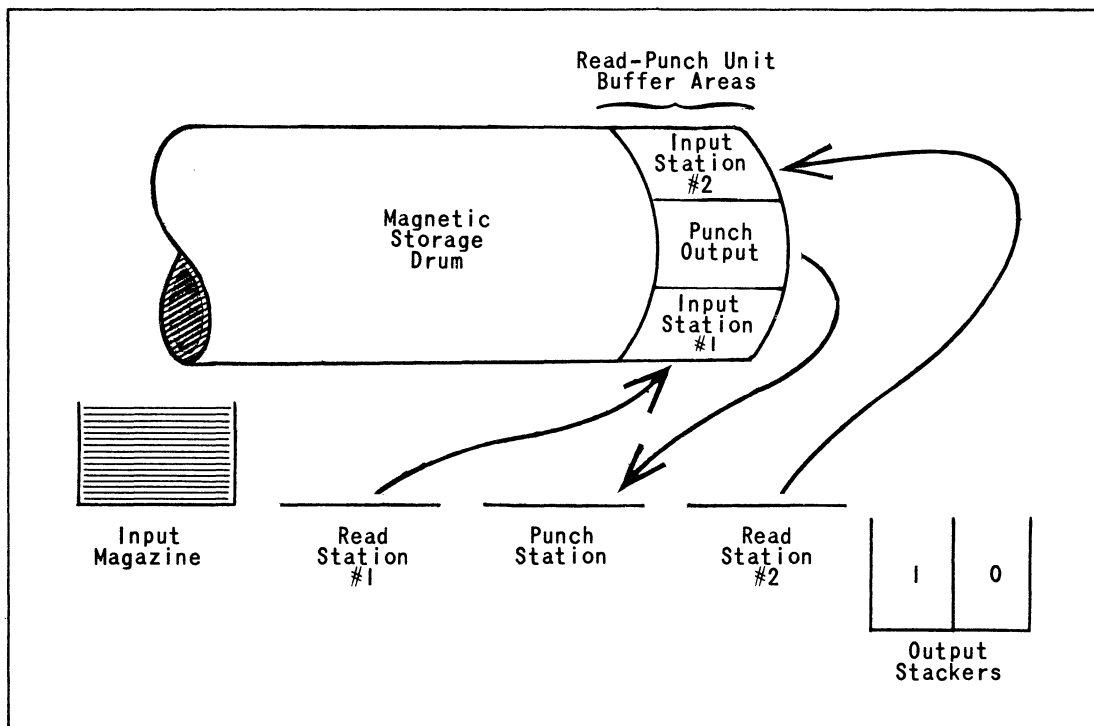


Figure 13 Functional Diagram Of The Read-Punch Unit

INPUT-OUTPUT LOGIC

Three program instructions control the operation cycle of the Read-Punch Unit. They are: 81, or card cycle instruction, (Read, Punch, and Move Cards); 46 (Transfer sensed information from the card buffer to main storage); 57 (Stacker selection). A fourth instruction (22) enables the programmer to test the buffer.

Instruction Codes

	Word Time
81 m c Transfer the output card images from the m band to the punch buffer. When the transfer is completed, the computer is free to operate on other instructions. The Read-Punch Unit will then punch the data from the punch buffer area into the card in the punch station. It then reads the cards now in both read stations, storing their images in the Read-Punch input buffer. Finally all cards are advanced one card station to the right in the Read-Punch Unit. m must be a multiple of 200 (i.e. 0000, 0200, 0400, etc.) For minimum latency this instruction should be in storage location 0198 + 20ln.	203
46 m c Wait until the Read-Punch input buffer is loaded, then transfer the input card images to band m. (m must be a multiple of 200.) For minimum latency, this instruction should be in storage location 0198 + 20ln.	203
22 m c This instruction permits the program to test the status of the Read-Punch input buffer. If the buffer is loaded, (rC) is transferred to rA and the next instruction is found at m. If the buffer is not loaded the next instruction is found at c. rA is not altered in this case.	3 if c address taken, otherwise 4
57 m c Select the output stacker designated by m. If m = 0000 the #0 stacker is selected, if m = 0100 the #1 stacker is selected. This instruction must be given within 116 ms after the Read-Punch input buffer is loaded if it is to operate on the card at the second read station. Otherwise stacker #0 is automatically selected.	3

Operation Cycle

Normally, the FEED ONE CARD button on the operating panel of the Read-Punch Unit is depressed three times to ready the unit for programmed operation. These fill operations are completely mechanical and no information is transferred to or from the Central Processor. Actual card reading and punching does not begin until the stations are loaded and an 81 instruction is received.

However, as shown in Figure 14 on page 22, the 81 instruction does not coincide with the beginning of the mechanical card cycle. It indirectly starts a card cycle, but, as shown in Figure 14, the instruction is given after approximately three quarters of the card cycle that was initiated by the previous 81 instruction.

At the beginning of the card cycle, cards in the two read stations (Cards B and D in Figure 14) are sensed. At 334 degrees of the card cycle, the sensed information is placed in capacitor storage. The information is then read, 10 bits at a time, into buffer storage. When the sensed information is completely written onto the buffer band, a 46 instruction transfers the information from the buffer to main storage.

During the time the sensed cards are moving to the next stations, the processor carries out computations on the information read from the card moving into the punch station (Card B). The information to be punched in that card is then stored in main storage. Card C is punched, under control of the mechanical card cycle, with previously processed information while the data for Card B is being computed.

The next 81 instruction, containing the number of output word storage band in its m address, is staticized in the static register, and the output words are transferred to the card buffer band. When the output words are all in the buffers, synchronizing circuits store the indication that an 81 instruction has been given, and the instruction is then cleared from the Static Register.

Starting at 134° of the mechanical card cycle caused by the previous 81 instruction, the synchronizing circuits set up the punch actuators with the output words stored in the buffer. Ten bits at a time are transferred serially from the card buffer to the shift register. Next, the ten bits are transferred in parallel to the information distribution matrix, and then to the actuator matrix to set up the punches for the card (Card B) moving into the punch station. During punch set-up time, the other cards are also moving. The card that was punched (Card C) is moving into the second read station, and the card that was sensed (Card D) in the second read station is on its way to the output stackers. At this point in the program a 57 instruction must be given if the card is to fall into stacker 1 instead of stacker 0.

The first mechanical card cycle ends as the cards come to rest in their respective stations. The synchronizing circuits complete the setting up of the punches and generate a signal that starts the next mechanical card cycle. A new card is fed, the cards in the read stations are sensed, and Card B in the punch station is punched.

Each successive 81 instruction, then, sets up punches for the card moving into the punch station and then initiates a new mechanical card cycle. The 46 instruction transfers the information sensed during a card cycle from the buffer to main storage. The 57 instruction need only be given to divert the card sensed in the second read station into stacker 1, otherwise it automatically falls into stacker 0.

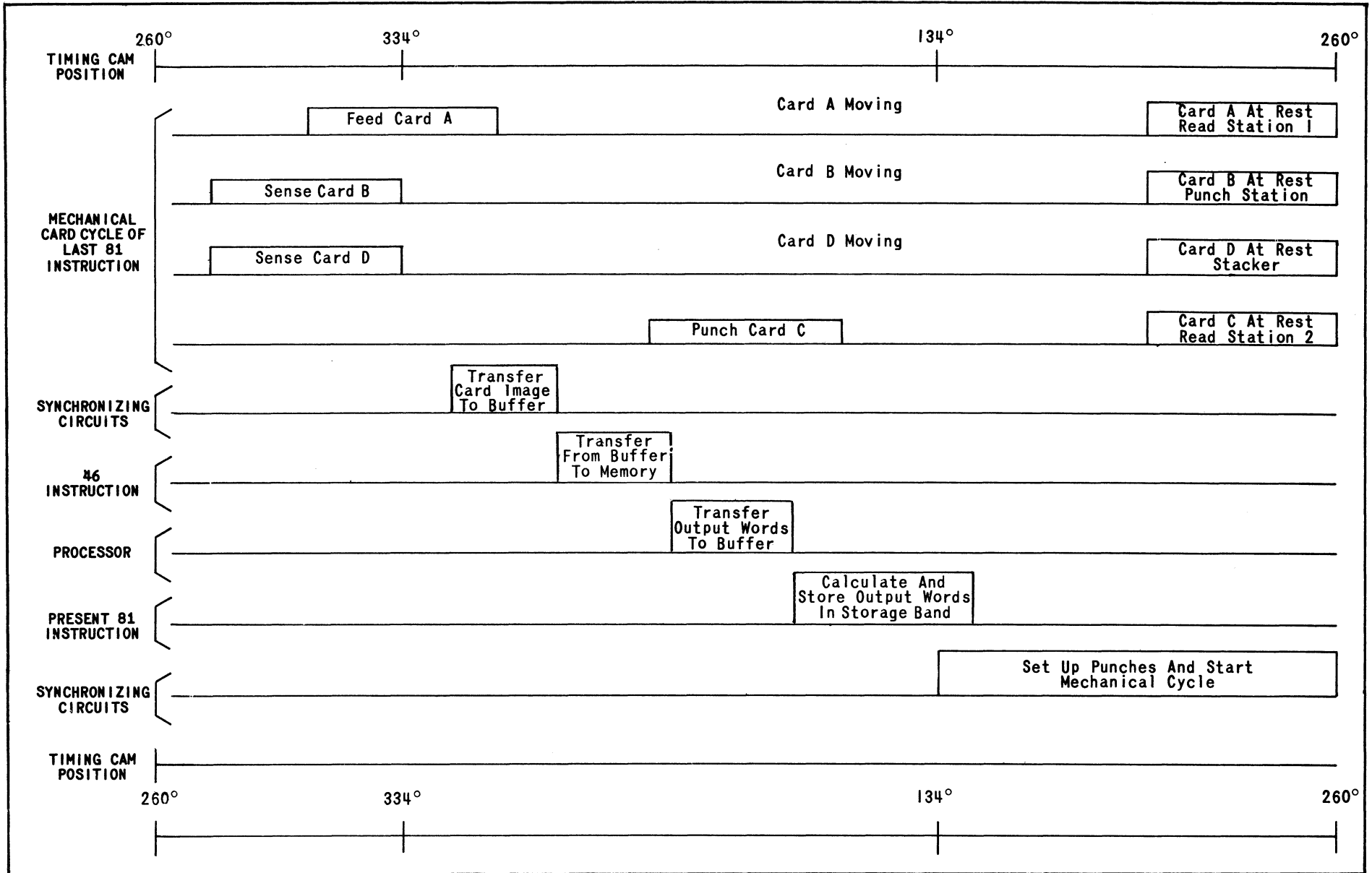


Figure 14 General Timing Diagram

Card Buffer Storage

The card buffer band on the magnetic storage drum is used to store information temporarily during input-output operations. As an intermediate storage between capacitory storage and main storage, the card buffer band is necessary because of the difference in speeds of operation of the relatively slow input-output units and the faster operating Central Processor.

The card buffer storage is used by both the High-Speed Reader and the Read-Punch Unit. Although it is not a part of main storage, the buffer contains 200 word locations, the same as any of the 25 main storage bands. Locations 000-099 serve the High-Speed Reader; locations 100-199 serve the Read-Punch Unit.

During input-output operations, information read from cards or information transferred from main storage to be punched is stored temporarily in the card buffer (Figure 15). After it is recorded in the card buffer, the information can then be transferred to main storage or to the punch actuators in one drum revolution.

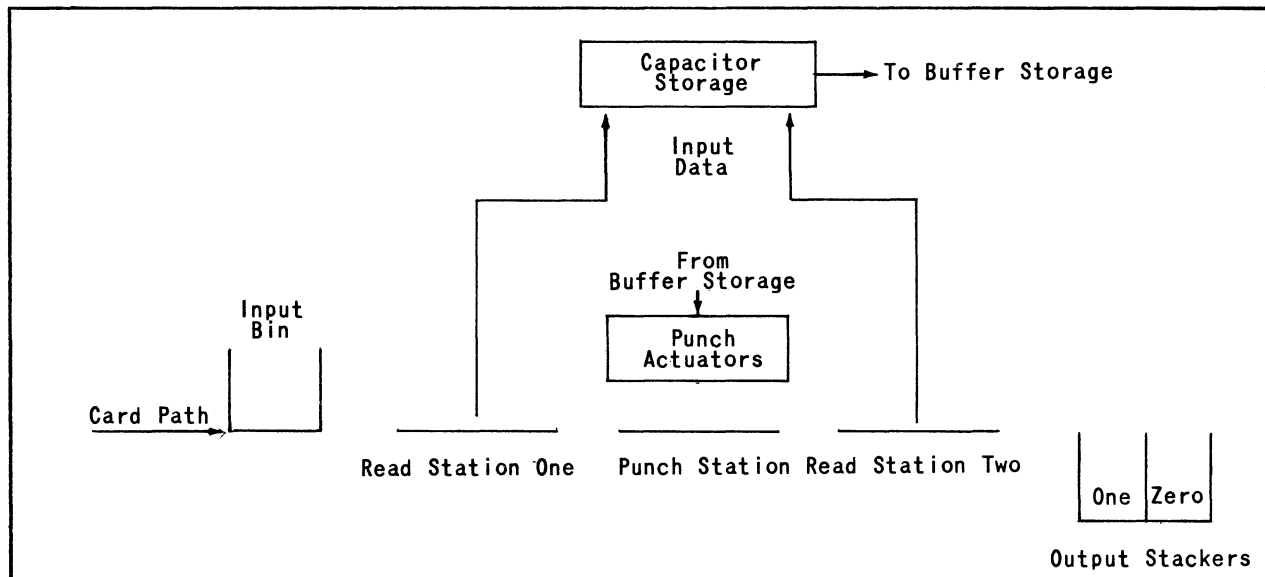


Figure 15 Read-Punch Unit

CARD WORDS

Information read from or punched into cards by the Read-Punch Unit is in the 6-bit Remington Rand punched-card code. Ten 10-digit computer words can be punched into one 90-column card in card code, five words in the Upper Field and five in the Lower Field. Each card field contains four 10-digit words and one 5-digit word as shown in Figure 16. Although words 4 and 9 contain only five digits of information, they are considered for computational purposes as 10-digit words.

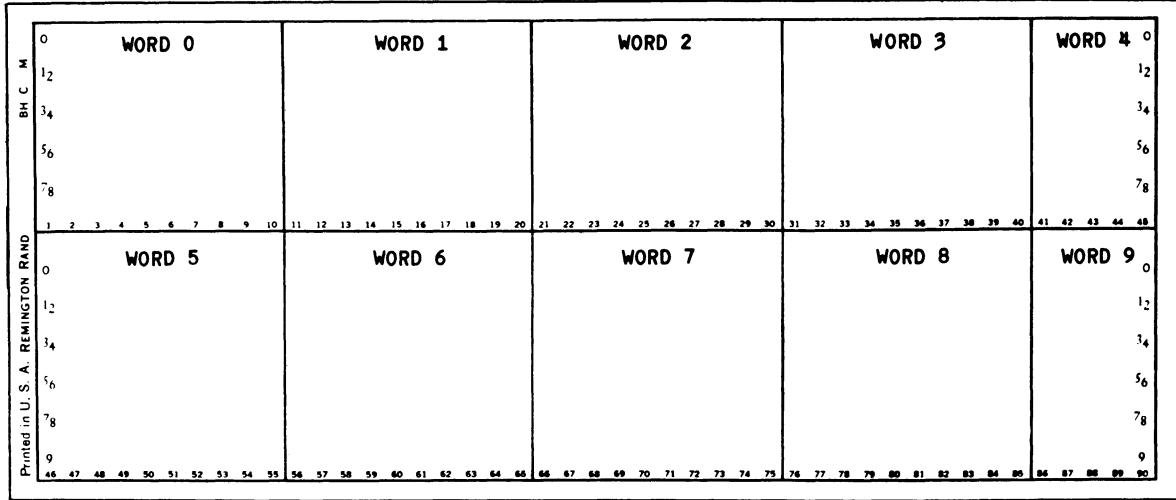


Figure 16 Basic Format of Card Words

Primed and Unprimed Word Parts

To store a word recorded in card code in either buffer storage or main storage, (words are stored in 4-bit computer code), the card word (six bits per digit) is divided into two parts, a primed word part and an unprimed word part.

Figure 17 shows a 10-digit word composed entirely of numeric characters. The unprimed part of each digit in the word is composed of the four bits in card row positions 0, 1, 3, and 5 (lower-order bits). The unprimed word part can be stored in one computer storage location because it is exactly the size of a 10-digit, 4-bit computer word.

Card Code			Decimal Value
9 7	5 3 1 0		
0 0	0 0 0 1	=	0
0 0	0 0 1 0	=	1
1 0	0 0 1 0	=	2
0 0	0 1 0 0	=	3
1 0	0 1 0 0	=	4
0 0	1 0 0 0	=	5
1 0	1 0 0 0	=	6
0 1	0 0 0 0	=	7
1 1	0 0 0 0	=	8
1 0	0 0 0 0	=	9
Primed Part	Unprimed Part		Word

Figure 17 Card Coded Word (10 Digits)

Figure 7 on page 9 is the complete 90-column card code and computer code table for all alphabetic, numeric, and special characters. Primed and unprimed parts of each character are noted and separated. The two XX's under the prime word column indicate the unused bit positions.

Card Word Identification

To enable the programmer to identify each word part (primed and unprimed) and the main storage location it will occupy, the card words, illustrated in Figure 16, are given more definitive notations. These notations, for input card words from Read 1 and Read 2 and for output card words, are shown in Figure 18 on page 26. The meanings of these additional notations are as follows:

I or O = Unprimed word part

I' or O' = Primed word part

1st digit of subscript = read station where card data was sensed

2nd digit of subscript = card word number

Data transferred from buffer to main storage is placed in specific main storage locations within a card input/output interlace (Figure 20 page 32). Thus, by correlating the word notations in Figure 18 with the interlace storage locations shown in Figure 20, the programmer may easily determine the main storage location of each card word part.

In programming the buffer-to-main storage transfer, the programmer may specify only the storage band into which the card data is to be placed. This is done by specifying the main storage band number in m of the 81 instruction. However, as previously stated, the interlace pattern for input/output words remains the same for all bands of the main storage.

PROGRAMMING THE OPERATION CYCLE

Input from punched-cards and output to punched-cards in the Read-Punch Unit are accomplished by the use of the Card Cycle (81) and Read (46) instructions. The 81 instruction first transfers data from the output interlace of the m band of main storage to the buffer band. When the main storage-to-buffer transfer is completed, the computer is free to operate on other instructions. The punch actuators are set-up independently of the computer. When the set-up is completed, the card cycle automatically punches, reads, and moves cards in all stations. The absence of a card from the input magazine, Read 1, or Read 2 causes an "empty station" indication which prevents the execution of the 81 instruction and causes a transfer to $c + 1$. A button is provided on the control panel of the Central Processor which allows the empty station signal to be ignored. If a card cycle (81) is forced (i.e. empty station ignored) when either read station is empty, the appropriate words in the buffer band will all be filled with 1's.

INPUT FROM
READ 1

WORD 0 I ₁₀	WORD 1 I ₁₁	WORD 2 I ₁₂	WORD 3 I ₁₃	WORD 4 I ₁₄
I' ₁₀	I' ₁₁	I' ₁₂	I' ₁₃	I' ₁₄
1 2 3 4 5 6 7 8 9 10	11 12 13 14 15 16 17 18 19 20	21 22 23 24 25 26 27 28 29 30	31 32 33 34 35 36 37 38 39 40	41 42 43 44 45
WORD 5 I ₁₅	WORD 6 I ₁₆	WORD 7 I ₁₇	WORD 8 I ₁₈	WORD 9 I ₁₉
I' ₁₅	I' ₁₆	I' ₁₇	I' ₁₈	I' ₁₉
46 47 48 49 50 51 52 53 54 55	56 57 58 59 60 61 62 63 64 65	66 67 68 69 70 71 72 73 74 75	76 77 78 79 80 81 82 83 84 85	86 87 88 89 90

OUTPUT FOR
PUNCHING

WORD 0 O ₁₀	WORD 1 O ₁₁	WORD 2 O ₁₂	WORD 3 O ₁₃	WORD 4 O ₁₄
O' ₁₀	O' ₁₁	O' ₁₂	O' ₁₃	O' ₁₄
1 2 3 4 5 6 7 8 9 10	11 12 13 14 15 16 17 18 19 20	21 22 23 24 25 26 27 28 29 30	31 32 33 34 35 36 37 38 39 40	41 42 43 44 45
WORD 5 O ₁₅	WORD 6 O ₁₆	WORD 7 O ₁₇	WORD 8 O ₁₈	WORD 9 O ₁₉
O' ₁₅	O' ₁₆	O' ₁₇	O' ₁₈	O' ₁₉
46 47 48 49 50 51 52 53 54 55	56 57 58 59 60 61 62 63 64 65	66 67 68 69 70 71 72 73 74 75	76 77 78 79 80 81 82 83 84 85	86 87 88 89 90

INPUT FROM
READ 2

WORD 0 I ₂₀	WORD 1 I ₂₁	WORD 2 I ₂₂	WORD 3 I ₂₃	WORD 4 I ₂₄
I' ₂₀	I' ₂₁	I' ₂₂	I' ₂₃	I' ₂₄
1 2 3 4 5 6 7 8 9 10	11 12 13 14 15 16 17 18 19 20	21 22 23 24 25 26 27 28 29 30	31 32 33 34 35 36 37 38 39 40	41 42 43 44 45
WORD 5 I ₂₅	WORD 6 I ₂₆	WORD 7 I ₂₇	WORD 8 I ₂₈	WORD 9 I ₂₉
I' ₂₅	I' ₂₆	I' ₂₇	I' ₂₈	I' ₂₉
46 47 48 49 50 51 52 53 54 55	56 57 58 59 60 61 62 63 64 65	66 67 68 69 70 71 72 73 74 75	76 77 78 79 80 81 82 83 84 85	86 87 88 89 90

Figure 18 Input and Output Card Words

The 46 instruction transfers the input data (read from cards in both read stations) from fixed locations in the buffer band to fixed interlace locations in any desired band in main storage. Before using the 46 instruction, it is necessary to determine, by means of a test instruction (22), whether the sensing of the cards has been completed.

The operations in the Read-Punch Unit are overlapped so that the following operations all occur once during each card cycle:

- 1) Reading the card at Read 1.
- 2) Punching the card in the Punch Station.
- 3) Reading the card at Read 2.

These operations in the Read-Punch Unit are all overlapped with computation, printing, and the operation of the High-Speed Reader as well.

Card Cycle

The card cycle instruction (81) may be given at any time, but if an 81 instruction is given in the 140 millisecond period during which the punch actuators are being set-up as a result of the previous 81 instruction, the machine will be interlocked until the punch set-up is completed. This situation should be avoided since it prevents exercising any control over the operation of the High-Speed Reader for a period of time that may be greater than one card cycle in the High-Speed Reader. Actually, there is no advantage in giving an 81 instruction that soon after the previous 81 instruction since a minimum time equal to the basic card cycle period must pass before the 81 instruction can be executed.

Punch Set-Up

When the card cycle instruction (81) is given, the computer immediately stores an indication of this in flip-flop and begins transferring the data from the output interlace in main storage to the punch buffer. The only exception to this occurs if the 81 instruction is given during the punch set-up time, in which case the machine is interlocked as described previously. This latency and transfer time (a minimum of 201 up to a maximum of 400 word times depending upon the latency resulting from the location of the 81 instruction) is the computer "execution time" required by the 81 instruction. When this buffer transfer is completed, the computer is free to proceed with the execution of other instructions in the mechanical card cycle. When the punch set-up has been completed, the card cycle flip-flop is reset.

Buffer-Loaded Test

The buffer-loaded flip-flop is set at a point 133 milliseconds before the point at which the punch set-up is started. Therefore, the 22 instruction which tests

for the buffer-loaded condition can be used to determine whether an 81 instruction can be given as well as whether a buffer-to-main storage transfer (46) instruction can be given. The use of the test instruction is the key to the proper timing and synchronization of the program and computer operation with the Read-Punch Unit.

Figure 19 indicates the timing of the 81, 46, 57 and 22 instructions with relation to the Read-Punch operating cycle.

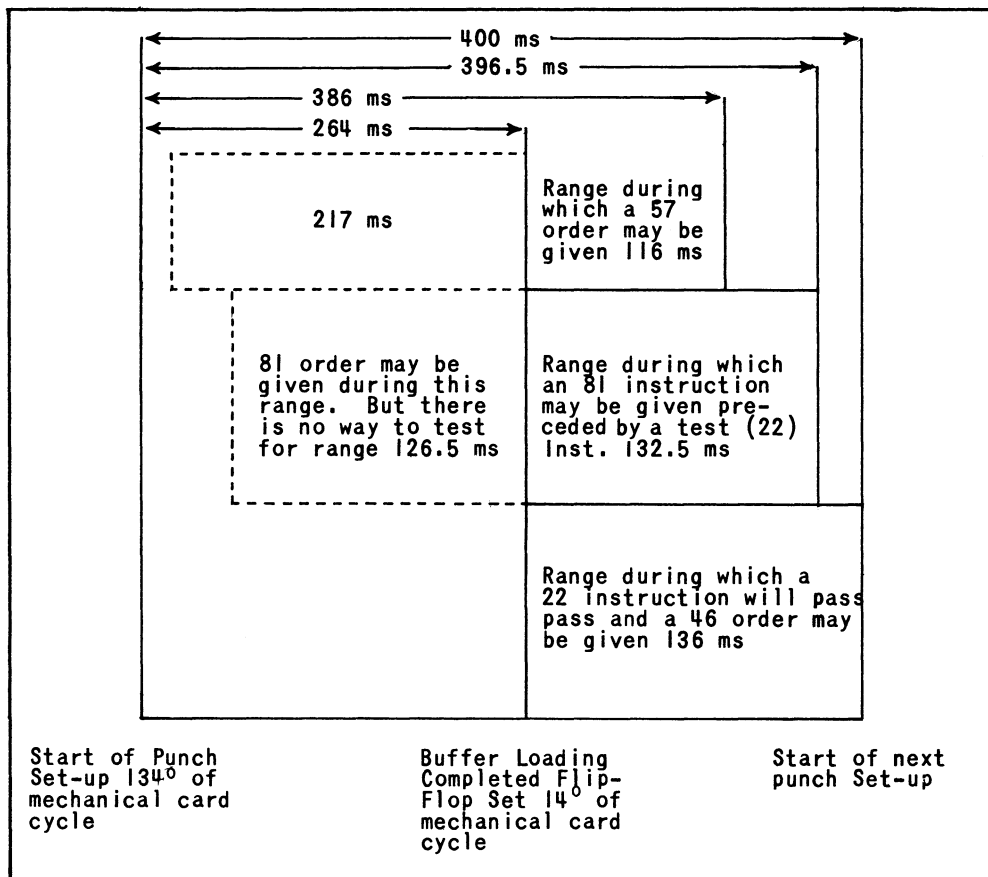


Figure 19 Diagram of Read-Punch Operating Cycle

In Figure 19, the point at which the punch set-up begins is taken as the start of the cycle and the reference point from which other points in the cycle are timed. This diagram shows that the buffer-loaded flip-flop will be set and the test instruction (22) will transfer (rC) to rA and transfer control to the location specified by the m address part of the test instruction. This occurs in a time range starting 264 milliseconds following the start of the punch set-up and ending when the buffer-to-memory transfer (46) instruction is given or when the next punch set-up is started if a card cycle (80) instruction is given (whichever occurs first). Therefore, there is a maximum range of 136 milliseconds during which the buffer loaded flip-flop is in the set condition.

- m represents a storage location or register
- c represents the address of the next program instruction
- (m) represents the contents of a storage location or register
- rA represents Register A
- rL represents Register L
- rC represents Register C
- rX represents Register X

Word Time

72 m c Pull a card into the continuously moving rollers of the feed. The card will be read at each station, in turn, and the data stored in the buffer band. The m address is ignored if executed. If a 72 order is given before the preceding 72 has begun to feed a card, the second 72 is not executed. Instead, (rC) go to rA and control goes to the m portion of the instruction in rC. The computer is free to operate on other instructions during the moving and reading of the cards.

3 if c address taken, otherwise 4

Word Time

96 m c Wait until the High-Speed Reader buffer is loaded, then transfer this data from the buffer to the memory band m (m must be a multiple of 200).

203

For minimum latency this instruction should be placed in cell $0198 + 201n$.

42 m c This instruction permits the programmer to test the status of the High-Speed Reader buffer. If the buffer is loaded (rC) is transferred to rA and the next instruction is found at m. If the buffer is not loaded, the next instruction is found at c. rA is not altered in this case.

3 if c address taken, otherwise 4

47 m c Select output stacker designated by m. If m = 0000 the #0 stacker is selected, if m = 0100 the #1 stacker is selected and if m = 0200 the #2 stacker is selected. To operate on the card at the second read station, this instruction must be given within 120.8 ms after the image is available in the buffer. If not, the card will enter the previously selected stacker.

3

Note: If a 96 instruction is given with only one card present in either read station, the buffer interlace locations of the station not occupied will read all binary 1's.

The "input buffer loaded" point can be directly detected by an instruction (the 42 m c).

3) The punching of this information into the card at the punch station.

Therefore the machine zeros must be transferred to the punch interlace positions as an initializing step in the program. The interlace positions can not be used as storages during the program. As an alternative, when the programmer does not wish to punch data into a card, the necessary coding may be provided to transfer machine zeros to the interlace positions whenever a punch cycle is to be initiated. The programmer should also keep in mind that he is processing unchecked data when using the Read-Punch Unit as an input device since the data cannot be checked until it has been read at Read 2.

Punch Unit Only

In using the Read-Punch Unit as an output device only, the programmer needs only to ignore the Read 1 positions in the interlace, and check the Read 2 positions against the data supplied for punching. If there is information pre-punched into the card, this should be considered when checking in order to have a valid second read. For further information on this subject, refer to the Back-up Punching Routine.

Combination Read-Punch

When using the Unit as both an input/output device, all of the considerations described primarily must be kept in mind by the programmer. For purposes of checking, he must save the information from Read 1 and from the punch station, and if necessary, compare certain portions of it to obtain equality between card words in the Read 2 check.

PROGRAM CHECKING

All checking of the Read-Punch Unit is accomplished by comparing for equality the contents of the second read interlace positions with the contents of the combined card words from the punch interlace positions and the first read interlace words. Sufficient time is provided to perform a stacker selection order after making these comparisons if an error is detected. If the error is considered by the programmer to be one which should stop further operations, the programmer should supply a stop order to rX containing information in the m portion of the word identifying the type of error. The program should then enter the Stop subroutine of the High-Speed Reader routine in order to protect other input/output information. (Note: Input data is not checked until this point if the Read-Punch Unit is used as a source of input data.)

ERROR CONDITIONS

There are four basic error conditions which may occur during operation of the Read-Punch Unit. They are:

1. Full output stacker.
2. Empty Read or Punch stations.
3. Empty input magazine
4. Card jam.

In each case, the succeeding 81 instruction after the condition has occurred will cause the computer to select the instruction word located at storage location $c+1$. If operations are to be stopped as a result of either of these error conditions, the program should be designed to transfer a "stop" instruction word to rX containing information in the m portion of the word identifying the type of error. The program should then enter the Stop subroutine of the High-Speed routine in order to protect other input/output information.

If the error conditions are to be ignored, a skip instruction should be transferred to the $c+1$ address.

STORAGE LOCATION OOXX		STORAGE LOCATION O1XX	
00	50	00	50
01	51	01 I10	51 I22
02 I15	52 I27	02	52
03	53	03 0'19	53 0'12
04	54	04	54
05	55	05	55
06	56	06 I'10	56 I'22
07 I'15	57 I'27	07	57
08	58	08 010	58 017
09	59	09	59
10	60	10	60
11	61	11 120	61 I13
12 I25	62 I18	12	62
13	63	13 0'10	63 0'17
14	64	14	64
15	65	15	65
16	66	16 I'20	66 I'13
17 I'25	67 I'18	17	67
18	68	18 015	68 013
19	69	19	69
20	70	20	70
21	71	21 I11	71 I23
22 I16	72 I28	22	72
23	73	23 0'15	73 0'13
24	74	24	74
25	75	25	75
26	76	26 I'11	76 I'23
27 I'16	77 I'28	27	77
28	78	28 011	78 018
29	79	29	79
30	80	30	80
31	81	31 I21	81 I14
32 I26	82 I19	32	82
33	83	33 0'11	83 0'18
34	84	34	84
35	85	35	85
36	86	36 I'21	86 I'14
37 I'26	87 I'19	37	87
38	88	38 016	88 014
39	89	39	89
40	90	40	90
41	91	41 I12	91 I24
42 I17	92 I29	42	92
43	93	43 0'16	93 0'14
44	94	44	94
45	95	45	95
46	96	46 I'12	96 I'24
47 I'17	97 I'29	47	97
48	98	48 012	98 019
49	99	49	99

Figure 20 Read-Punch Unit Interlace Pattern

GENERAL DESCRIPTION

The High-Speed Printer prints in a variety of formats, controlled by the program, at a speed of up to 600 lines per minute. Fifty-one print characters are available including 26 alphabets, 10 numerics, and 15 symbols and punctuation marks.

The High-Speed Printer produces printed lines of computed or tabulated results 130 characters wide, spaced six lines per inch vertically, and containing 10 characters per inch horizontally. Any sprocket-fed paper up to and including card stock, either blank or preprinted, can be printed by the High-Speed Printer. At least five carbon copies and one original copy can be produced by using paper between 11 and 13.5 pounds in weight. Impression control permits variation in the strength of the printing hammer stroke.

OUTPUT LOGIC

Under control of program instructions, information to be printed is first transferred from main storage to the print buffer on the magnetic storage drum. From the buffer the information is transferred to the print mechanism of the High-Speed Printer.

The printing cycle is controlled by two instructions, 11 and 16. The 11 instruction accomplishes the main storage-to-buffer data transfer, a paper advance, and the printing by the High-Speed Printer. The 16 instructions accomplishes paper advances (up to 79 lines) by the High-Speed Printer.

These instructions, and others which are related to the printing operation, are discussed in detail later in this manual.

Print Words

The 130 characters that can be printed one one line are divided into 13 10-digit print words. These words, and their corresponding print positions, are shown in Figure 21. Before a print instruction is executed, the 13 print words are accumulated by program instructions on a specific main storage band in fixed word locations of the print interlace pattern.

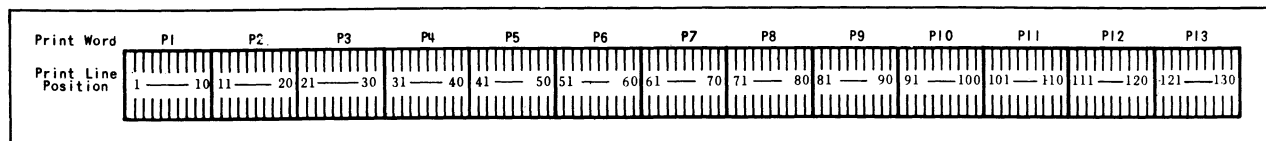


Figure 21 One Print Line

Print Interlace

Information stored in the print interlace is in 6-bit Remington Rand punched-card code, and thus requires two storage locations (words are stored in 4-bit computer code). Therefore, each print word is divided into two parts, a primed word part and an unprimed word part.

The primed word part is composed of the four lower-order bits of each character in the 10-digit print word. The unprimed word part is composed of the two higher-order bits of each character in the print word. Figure 22 contains the primed and unprimed parts of each character that can be printed by the High-Speed Printer.

UNPRIMED CHARACTER (5310)	(PRIMED CHARACTER (XX97))			
	XX00	XX01	XX10	XX11
0000	Space	7	9	8
0001	0	C	L	X
0010	1	R	2	F
0100	3	H	4	T
1000	5	G	6	Z
0011	*			
0101	E	W	V	
1001	M	U	N	(
0110	O	P	Y	:
1010	B	S	A	+
1100	I	Q	K	/
0111				.
1011	%	#		apostrophe
1101	D	-	,	
		dash	comma	
1110	J)	.	
			period	;
1111		&	\$	

Figure 22 Code Combinations for Print Characters

Print Word Identification

To enable the programmer to identify each word part (primed and unprimed) and the storage location it will occupy in the interlace pattern, each print word is given more definitive notation. These notations, and the interlace locations of each word part are shown in Figure 25 on page 42. Although the parts of each of the 13 print words are separated in the interlace, both parts of each word are printed in the corresponding print line positions shown in Figure 21. For example, P1 and P'1 refer to the unprimed and primed parts of print word 1. Both parts are combined and printed in print line position P1 (Figure 21) during the actual printing operation.

Because of the fixed interlace pattern (regardless of the storage band), the programmer may arrange words to be printed in a desired sequence within the interlace pattern. For example, the first word that is to appear on a particular print

line should be placed in interlace location 000 and 005 of a specified storage band. Consequently, during the print operation, the words appearing in these locations would constitute print word 1 (P1) and would be printed in print line positions 1 through 10 (Figure 21). Likewise, programming would be provided to place the last word to be printed (P13) in interlace locations 178 and 183 of the same band. During the print operation, both parts of P13 would be printed in print line positions 120 through 130.

Buffer Storage

The print buffer area on the main storage drum is used to store one line of information to be printed (13, 10-digit words). Under control of the print instruction (11) one line of information is transferred from the main storage interlace, to the buffer storage, and then to the print mechanism in the High-Speed Printer (Figure 23).

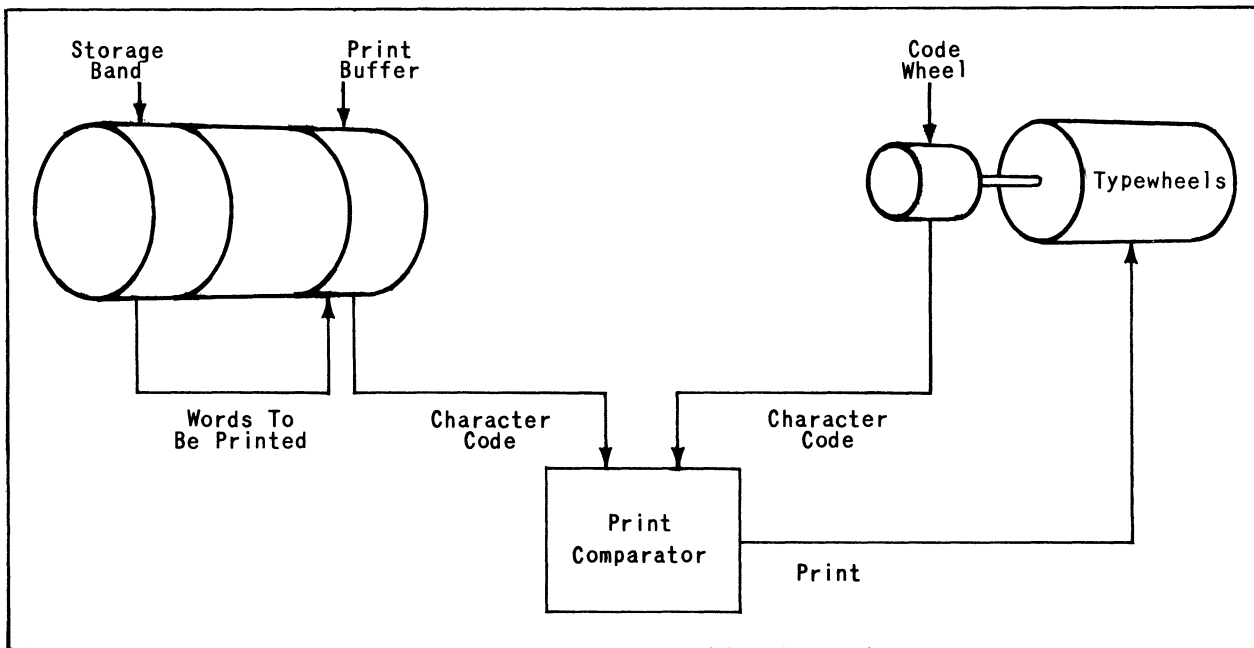


Figure 23 General Block Diagram of Print Operation

PRINT MECHANISM

The print mechanism of the High-Speed Printer is composed of 65 typewheels, and a code wheel containing the 6-bit code combinations for each of the 51 print characters. The code wheel and the typewheels are mounted on a common shaft as shown in Figure 24.

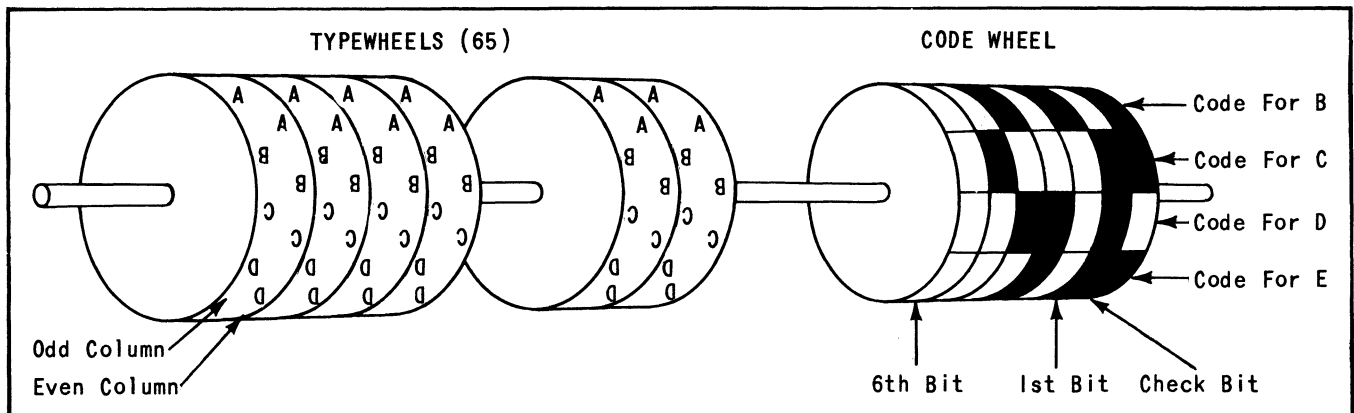


Figure 24 Typewheels and Code Wheel

Typewheels

Each of the 65 typewheels contains two columns of type. Each column contains the 51 printable characters. Sixty-five columns, representing corresponding columns on each of the 65 typewheels, are designated as odd; the alternate 65 columns are designated as even.

The columns of type are staggered in a checkerboard pattern on the typewheels (Figure 24) allowing each character to be surrounded by four spaces instead of four other type characters. This prevents smudging or partial printing of an adjacent character when only one character is being printed.

Code Wheel

The code wheel contains the 6-bit code combinations for each of the 51 type characters magnetically recorded around its surface. A parity bit (check) is stored on the code wheel as well as the six information bits.

As a character on the 65 typewheels moves into print position, the code combination for that character is read from the code wheel and compared with the 130 character combinations representing a line of output data. The identities are stored (see the Print Comparator, Figure 23) and then each actuates the appropriate print hammer.

Printing Cycle

The printing cycle always begins with the printing of characters in the odd columns. Assuming that the character in print position is a U, all the odd U's contained in the 13 words of output data are printed by comparing the digits of each of the 13 words with the code combination for a U read from the code wheel and actuating the appropriate print hammers. Next, all of the even U's move into print position and, after another sequence of 130 comparisons,

all of the even U's contained in the 13 words are printed. As the odd U's move into print position, the code combination for V is read from the code wheel into the comparator circuit to replace the combination for U. The 130 characters of output data are compared, in turn, for identity with character combinations from the code wheel corresponding to successive character positions on the typewheels.

The comparison and printing process continues for one complete revolution of the typewheels to print a complete line, after which the print buffer may be loaded with new data and the paper advanced in preparation for printing the next line. Printing can begin with any character once a comparison is obtained.

PROGRAMMING THE OPERATING CYCLE

The operation of the High-Speed Printer is controlled by the Advance instruction (16) and the Advance and Print instruction (11). The 16 instruction merely advances the paper a number of lines specified by the two least significant digits of the m address part of the instruction without affecting any data. The 11 instruction advances the paper in the same way, but then transfers 26 print words from the print interlace pattern in the m band (only the two most significant digits of the m address part of the instruction determine the band) to the print buffer band and initiates the print operation at the completion of the paper advance. Both of these instructions are provided with interlocks to hold up the computer if the previous 16 or 11 instruction is not completed before another one is given.

For programming the printing cycle, a 27 instruction is also provided. This instruction tests the status of the High-Speed Printer.

Program Instructions

The following is a list of the instructions used in programming the operation cycle of the High-Speed Printer. Included are descriptions of the function of the instructions and the word-times required for their execution.

An instruction for zero suppression in both printing and punching operations is available but not discussed in this text.

<u>Instruction Code</u>	<u>Function</u>	<u>Word Time</u>
11 m c	Wait until the previous printer operation is completed, then advance the paper "y" lines. While the paper advance is taking place, transfer the data from the m band print interlace to the print buffer band. The line is printed upon completion of the paper advance. The computer is released for other operations as soon as the	592

buffer band is loaded. The contents of rA and rX will be altered during the transfer of data to the buffer band.

The two most significant digits of m specify the print interlace band. The two least significant digits of m specify "y". Normally
00 y 49.

For minimum latency, the ll instruction should be in location $0198 + 789n$.

- | | | |
|--------|--|---------------------------------------|
| 16 m c | Wait until the previous printer operation is completed then advance the paper "y" lines. Once paper movement is started the computer is free for other operations. "y" is the same as defined in the ll instruction above. | 4 |
| 27 m c | This instruction tests the status of the printer. If a print or paper advance is in process the next instruction is selected from c, otherwise the next instruction is at m and (rC) are transferred to rA, | 3 if c address is taken, otherwise 4. |

Preliminary Processing

Before printing, it is necessary to program the transfer of 26 print words (13 primed words and 13 related unprimed words) into the print interlace pattern. The editing of the information to be printed must also be programmed. The band containing the interlace designated by the two most significant digits of the m address part of the print instruction (ll), may be any band not used for card image input/output interlaces.

Printing

The Advance instruction (16) merely advances the paper without affecting any data. It requires an "execution time" of only four word times after which the computer is free to continue with the execution of other instructions in the program while the paper advance proceeds independently of the computer. The Advance and Print instruction (ll) first initiates paper movement and causes the 26 print words in the print interlace to be transferred to the print buffer. The transfer from the print interlace pattern in the m band to the print buffer band requires almost three drum revolutions (592 word times). The 592 word times for this main storage-to-buffer transfer plus the latency time to the minimum latency location for the ll instruction ($0198 + 789n$) is the "execution time" of the print instruction. After that time, the computer is free to continue with the execution of other instructions in the program

and the print operation is completed independently of the computer. Therefore, paper movement and printing are overlapped with computing and card feed operations. The actual printing is initiated automatically when the paper movement is completed.

The advance instruction (16) does not affect the main storage, the buffer, nor any registers since no data is involved. This instruction delays the computer for only four word times unless the previous 16 or 11 instruction has not been completed, in which case there is an interlock condition which delays the computer until the previous 16 or 11 instruction is completed. Since no interlace pattern or buffer is involved, the 16 instructions may be placed in any drum address with the same latency considerations as for data comparisons.

Registers A and X are used in the main storage-to-buffer transfer part of the Print instruction. Therefore, any information stored in rA and rX will be destroyed if a Print instruction is given.

Printing Format

The 13 primed and 13 unprimed words from the interlace pattern cause printing to occur on the continuous paper forms in the print positions shown in Figure 2. As previously noted, all data to be printed must be completely edited for the proper columns and positioned in the proper interlace pattern by programming.

Minimum Latency Coding

For minimum latency, the Print instruction (11) should be placed in storage location $0198 + 789n$. If the 11 instruction is placed elsewhere, additional latency time to $0198 + 789n$ will result. After the main storage-to-buffer transfer is completed, the computer is free to proceed with the execution of other instructions while the code for each character on the print wheel is compared automatically with each character stored in the print buffer. Every time a coincidence is obtained, an indication is placed in a special storage associated with the print mechanism to control the print hammers. These operations and the proper timing of the print mechanism and print hammers are all automatic and do not require any consideration by the programmer.

Interlocks

If either an Advance (16) or a Print and Advance instruction (11) is given while a previous 11 or 16 instruction is in progress, the computer will be interlocked until the execution of that particular instruction is completed.

To prevent this situation, a 27 instruction is provided. This instruction tests the print flip-flop and the paper feed flip-flop to determine if both are set. If not, (rC) will be transferred to rA and control will be transferred to the address specified by the m part, but if either an 11 or 16 instruction is in process, the address of the next instruction will be specified by the c part of the 27 instruction.

ERROR CONDITIONS

When any error condition occurs in the High-Speed Printer, the computer will go to $c + 1$ (the entrance to a programmed error routine) and the appropriate neons will be lighted on the Printer control panel. The following list describes these error conditions:

1) Paper Feed Check:

The Paper Feed Check light will indicate that the paper for the Printer did not stop advancing after the time for the maximum paper advance (79 lines maximum). Depression of the Paper Feed Check light-button will advance the paper one line.

2) Change Ribbons:

Depression of this button will cause the Processor to transfer program control to a programmed routine which will bring the Processor to a stop. This transfer will take place when the first Advance and/or Print instruction is encountered after the ribbon has completely unwound in one direction.

3) Print Carriage Control:

In - This light/button indicates that the Printer carriage is in position for printing. Depression of this button moves the carriage from the "out" position to the "in" position.

Out - This light/button indicates that the Printer carriage is not in position for printing. While in this position the printer will not operate. Depression of this button moves the carriage into the "out" position.

4) No Ribbon:

This light indicates that the Printer has no ribbon or that the ribbon is broken.

5) No Paper:

This light indicates that the Printer has no paper or that the paper form has broken.

6) Charge Check Indicators:

These two lights, labeled Fire and Extinguish, indicate that the power for activating the print wheels is not being received properly.

7) Code Wheel:

This light indicates that a character to be printed has a bit structure which is erroneous. The line containing this character will be printed omitting the erroneous character.

MEMORY LOCATION OOXX		MEMORY LOCATION O1XX	
00	P1	50	P4
01		51	
02		52	
03		53	
04		54	
05	P'1	55	P'4
06		56	
07		57	
08		58	
09	P10	59	
10		60	
11		61	
12		62	P13
13		63	
14	P'10	64	
15		65	P3
16		66	
17		67	P'13
18	P6	68	
19		69	
20		70	P'3
21		71	
22		72	
23	P'6	73	
24		74	
25		75	P9
26		76	
27		77	
28		78	P12
29		79	
30		80	P'9
31		81	P2
32		82	
33		83	P'12
34		84	P5
35		85	
36		86	P'2
37		87	
38		88	
39		89	P'5
40		90	
41	P8	91	
42		92	
43		93	
44		94	P11
45		95	
46	P'8	96	
47		97	
48		98	
49		99	P'11

Figure 25 Print Interlace Pattern

GENERAL DESCRIPTION

Whenever a program determines that a computer stop is necessary, there may be cards already in motion or "on order" in the input/output units. These cards will be sent through the card stations and then to the stackers. Obviously, some provision must be made by the programmer to preserve the data contained in these cards. This is done by causing programming control to be transferred to Stop sub-routines.

In the High-Speed Reader, these cards should be sensed at the read stations, the data they contain transferred to buffer, then to reserve working storage (item advance), and then, checked for equality. The required stacker selection orders should also be executed. These operations are provided in the Stop sub-routine.

In the Read-Punch Unit, there may also be a card cycle in progress when the computer stop is required. If so, a similar sub-routine must be provided to perform the associated input/output operations on these cards before the computer is stopped.

CONTENTS OF THE STOP ROUTINE

Stop sub-routines are included in the buffer unload routines of the High-Speed Reader and the Read Punch Unit, and the Read Punch sentinel routine. When referred to as a whole, they are called the Stop Routine. The core of this routine is a programmed loop consisting of:

1. High-Speed Reader buffer test.
2. Read-Punch Unit buffer test.
3. A Timer which determines when the High-Speed Reader is empty.
4. A test of the Read-Punch Unit stacker sentinel, which indicates whether there is a card leaving the Read-Punch Unit for which no stacker is prescribed.

OPERATING LOGIC

The principal function of the Stop sub-routine is to transfer control to the proper routine when the High-Speed Reader buffer or Read-Punch Unit buffer becomes loaded. When it is determined that neither buffer is going to be loaded again, the Stop sub-routine stops the computer.

Errors Outside of Unload Buffer Sub-Routines

When an error is detected outside the High-Speed Reader unload buffer sub-routine, a stop instruction is stored by the Stop sub-routine. When the High-Speed Reader or the Read-Punch Unit buffer is loaded, control is sent to the corresponding buffer sub-routine. When the computer stops because of an error detected outside of the High-Speed Reader buffer sub-routine, no cards need to be re-enter-

ed in the High-Speed Reader. The programmer should supply directions for corrective action and will specify the point to which the program will go when the computer is again started.

An abnormal operating condition is an example of a condition, detected outside the High-Speed Reader unload buffer routine, which will require a computer stop. When this condition is detected in the High-Speed Reader, the program continues normally until there are no images in reserve storage and no cards in the High-Speed Reader. The abnormal condition is recognized by the Timer in the Read routine, and control is sent to the Stop routine. Except in instances to be described later, the program returns control to the Read routine when processing is continued. This fills the High-Speed Reader and transfers card image to working storage. In the event of a card jam or a registration error, the program should be continued from a rerun point.

For errors detected during the High-Speed Reader buffer routine which do not require a stop, the erroneous image can be overlaid.

Errors During the Gap

The gap of the High-Speed Reader routine is provided for stacker selection and other programming. Tests made during the gap may indicate that a stop is necessary. If so, control is transferred to a Stop routine. No more images will be reserved and the High-Speed Reader routine will count the cards passing through the High-Speed Reader so the operator can tell how many cards to put back into the magazine when restarting. After the computer stops and the error condition is corrected, control is transferred to input instruction, and then to the point in the main program where the High-Speed Reader buffer routine was entered.

Reread Errors

In case of a reread error, the High-Speed Reader routine is designed to cause a Stop. The stopping procedure is the same as above, with the cards being counted that pass through the High-Speed Reader after the reread error. Then, on restarting, input instruction is given, and control returns to the main program.

Multiple Errors

During the Stop sub-routine, control is transferred to the High-Speed Reader buffer routine, and to the Read-Punch Unit buffer routine. During these routines, an additional error may occur which requires a stop. If this happens, a multiple error condition is present.

Timer

A Timer is used in the High-Speed Reader routine to indicate that seven card

cycles have elapsed during which a buffer test has not passed. This Timer is used in two instances. The first is used to detect an abnormal operating condition in the High-Speed Reader. If the program is waiting for new input and none is received for seven card cycles, an abnormal condition is present. Seven cycles are allowed to make provision for instances where a misfeed or misfeeds are followed by a good feed. The second Timer is used to determine when the High-Speed Reader is empty.



UNIVAC[®]—The FIRST Name in Electronic Computing Systems