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PRELIMINARY

UNIVAC

1100 Systems

C/SP HARDWARE SYSTEM

OVERHEAD MANUAL

Marketing Education

UE- 7022

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C/SP HARDWARE SYSTEM

OVERHEAD MANUAL

This document contains diagrams which can be used for overhead transparencies in presenting the UNIVAC Communications/Symbiont Processor. Each diagram has a facing (odd pages) script describing it. For more detailed information, reference UNIVAC Documentation on the C/SP (indicated in Section VI of this manual). The intent of this manual is modular: presentations may be given using the overheads (even pages) as they are, along with the UNIVAC Documentation on the C/SP as reference, or the overheads may be used as a basis for the type of presentation needed.

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SECTION I

C/SP HARDWARE

SECTION I INDEX – C/SP HARDWARE

INTRODUCTION TO C/SP

The Communications/Symbiont Processor is a high performance internally programmed communications concentrator-multiplexer intended for use as an on-site communications subsystem. The C/SP can control low and high speed communication lines and provide interfacing to a central computer system.

The primary purpose of the C/SP is to unburden the central computer software of the need for complex communication handlers and sub-routines, thus relieving the load on the central computer. The throughput of the system is thus increased by the reduction of central system overhead. The C/SP is utilized to increase speed and efficiency of on-line message switching, data manipulations, formatting, editing, translation, and verification.

As a remote, the C/SP effects reduced line costs and unburdens the central complex by performing message/data manipulations and exchanging all data with it over high speed lines.

The C/SP consists of three main sections:

Memory
Central Processing Unit
I/O Section

C/SP Software consists of:

Terminal Management Supervisor (TMS)
Message Control Program (MCP)
Terminal Management Control Routine (TMCR)
Communication Control Routines (CCR)
Host Handler

Host Software consists of:

C/SP Symbiont
C/SP Handler
Initial Load Routine (non-resident)
Mass Storage Symbiont (non-resident)
Communication Routine (non-resident)
Assembler - Support Processor
Collector - Support Processor
Simulator - Support Processor

HARDWARE BLOCK DIAGRAM

All information transfers to and from the C/SP are handled by a maximum of seven channels designated as zero through six. Channels Ø and 6 are reserved for the General Purpose Communications and Special Device respectfully.

Channel Ø - GPCC: The link between the main storage and the communications line terminals (CLT's). The GPCC control's 8 CLT's (half-duplex) expandable to 64 CLT's (half-duplex) in increments of 8. GPCC expansion at this time may be to 2. In the future 4 GPCC's may be allowed per C/SP.

Channel 6 - Special Device Channel (SDC): To provide the means for local program loading and maintenance using an 80 card/minute reader. In the future, a printer and keyboard may be added.

Channels 1 - 5 - May be used for the Adapter, Multiplexer, and Selector. The Multiplexer/Selector are alike in that they can drive up to 8 control units and each control unit may control up to 16 devices (9000 peripherals, discs). The MUX/SEL are different in respect that the Selector Channel locks on to a control unit and drives the device, whereas the Multiplexer multiplexes through the control units to any device. The MUX operates in excess of 85K bytes/second. The Selector operates in excess of 625K bytes/second.

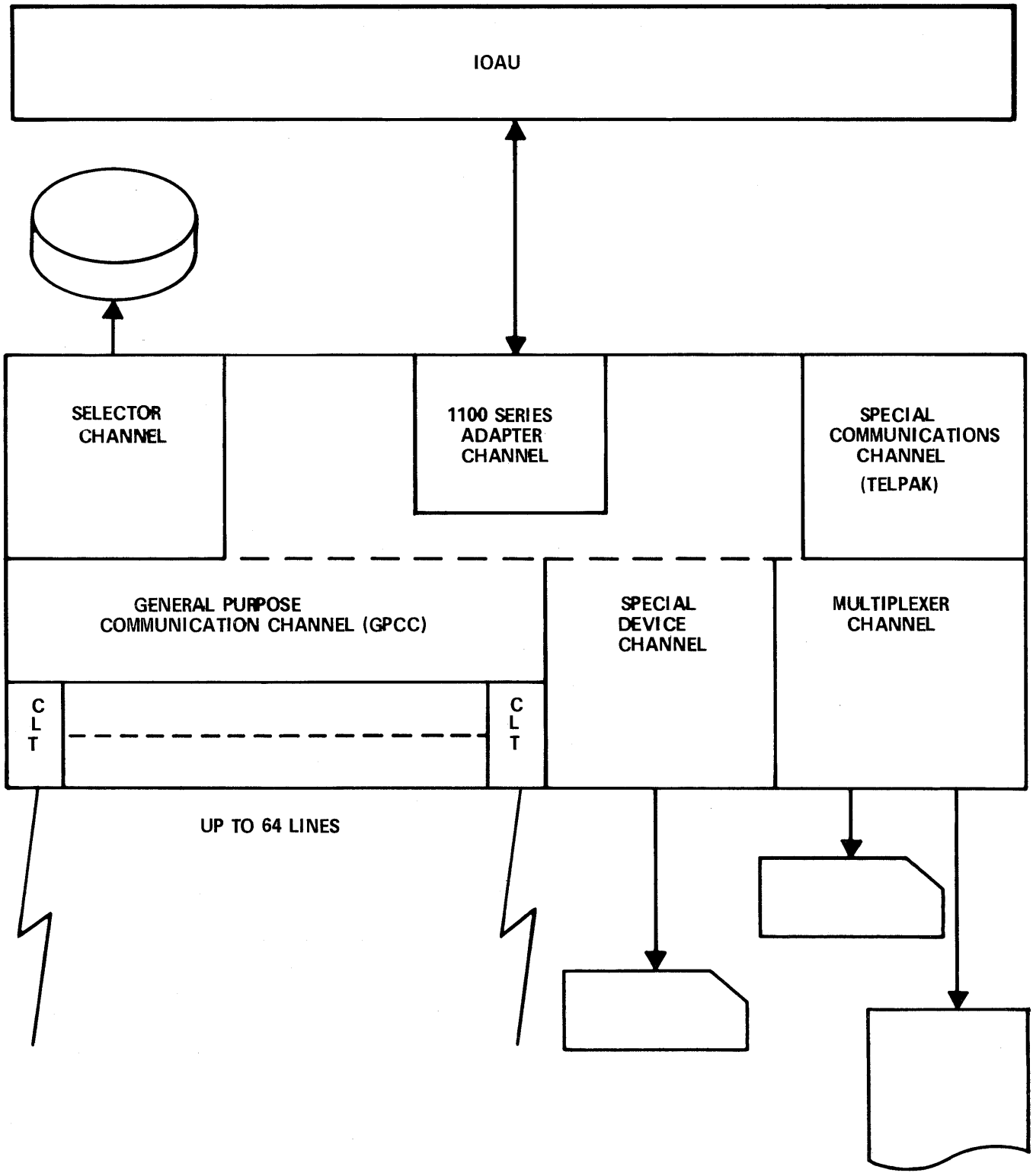
The Intercomputer Adapter (ICA) - Provides the means of communication between the C/SP and the Host Computer. The ICA operates at 300K 36-bit words per second on an Internally Specified Index (ISI) basis.

Special Purpose Communications Channel (SPCC) - Operates in 2 modes; either single duplex or full duplex.

Single duplex - Consists of 1 full duplex CLT which operates at 57K bytes per second.

Full duplex - Consists of 8 full duplex CLT's which operate at a combined maximum in excess of 300K bytes/second.

HARDWARE BLOCK DIAGRAM



MEMORY

Memory is divided into banks consisting of 2048 bytes per bank.

Each word consists of 4 bytes where a byte is 8 bits of data. Associated with each 8-bit byte is a 9th bit used as the parity bit for that byte. The parity bit is generated in storage when data is written and checked in storage when data is read out. The C/SP used odd parity unless specified as even under message discipline control for those terminals requiring even parity.

MEMORY

DECIMAL ADDRESS RANGE	HEXADECIMAL ADDRESS RANGE	LOGICAL MEMORY BANK
00000 – 02047	0000 – 07FF	0
02048 – 04095	0800 – 0FFF	1
04096 – 06143	1000 – 17FF	2
06144 – 08191	1800 – 1FFF	3
08192 – 10239	2000 – 27FF	4
10240 – 12287	2800 – 2FFF	5
12288 – 14335	3000 – 37FF	6
14336 – 16383	3800 – 3FFF	7
16384 – 18431	4000 – 47FF	8
18432 – 20479	4800 – 4FFF	9
20480 – 22527	5000 – 57FF	10
22528 – 24575	5800 – 5FFF	11
24576 – 26623	6000 – 67FF	12
26624 – 28671	6800 – 6FFF	13
28672 – 30719	7000 – 77FF	14
30720 – 32767	7800 – 7FFF	15
32769 – 34815	8000 – 87FF	16
34816 – 36863	8800 – 8FFF	17
36864 – 38911	9000 – 97FF	18
38912 – 40959	9800 – 9FFF	19
41960 – 43007	A000 – A7FF	20
43008 – 45055	A800 – AFFF	21
45056 – 47103	B000 – B7FF	22
47104 – 49151	B800 – BFFF	23
49152 – 51199	C000 – C7FF	24
51200 – 53247	C800 – CFFF	25
53248 – 55295	D000 – D7FF	26
55296 – 57343	D800 – DFFF	27
57344 – 59391	E000 – E7FF	28
59392 – 61439	E800 – EFFF	29
61440 – 63487	F000 – F7FF	30
63488 – 65535	F800 – FFFF	31

2K = 1 BANK
64 BANKS MAX.

FIXED MEMORY

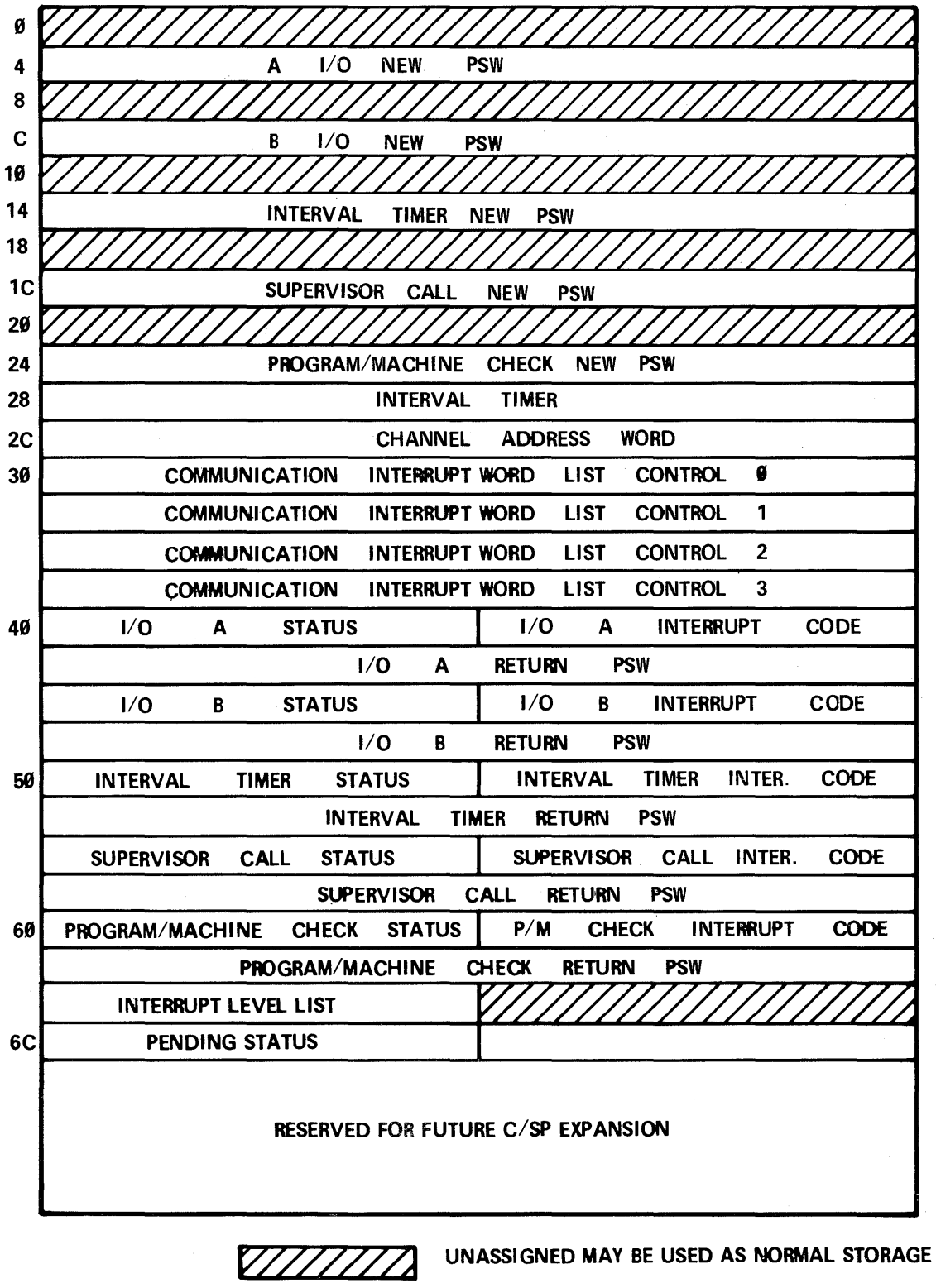
The low order memory locations are used by the C/SP in controlling the initiation of I/O commands, interrupt execution, and Internal Timer operation.

The area which is reserved for future C/SP expansion is used for four more CIW Lists when more than one GPCC is utilized in the C/SP System.

Address 68_{16} and 69_{16} are for the Interrupt Level List indicating a CIW was tabled by the GPCC. The foremost significant bits of address 69_{16} are set each time the GPCC tables an interrupt and each bit correspond to the list which was used. If more than one GPCC in the system, the same four bits are used.

Pending Status - Allows the software to pick up status information without requiring the acceptance of an interrupt.

FIXED MEMORY



WORD AND INSTRUCTION FORMATS

The C/SP memory bytes are assembled into 4-byte, 32-bit words. Some instructions and operations utilize the 16-bit half-word.

The C/SP instructions are made up of four formats: RR, RX, RS, SI.

RR (register to register) - The RR format contains an Operation Code and two register designators - R1 and R2. R1 and R2 contain values of 0-15 decimal and point at 16 registers of 32-bit length. (R1 contains Operand 1 and R2 contains Operand 2).

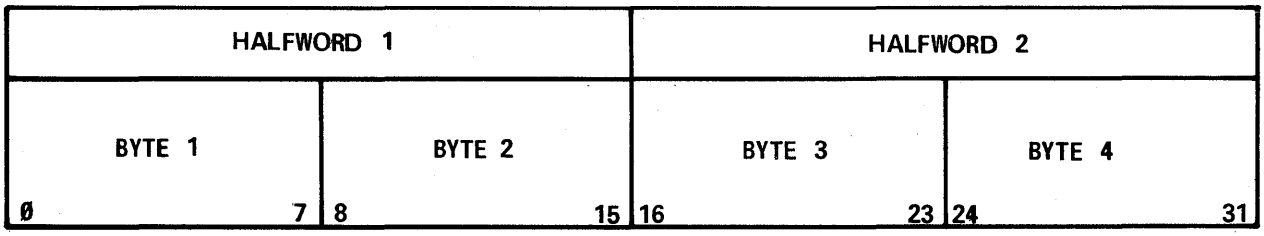
RX (register to indexed storage) - The RX format contains the OP Code, R1, X2, B2 and D2. The X2 designator points at an INDEX value in the registers. B2 points at a register containing a BASE value. D2 contains a twelve-bit DISPLACEMENT value. Operand 2 is referenced via ((X2)+(B2)) + D2 or the contents of the X2-register plus the contents of the B2-register plus the value in D2.

RS (register to storage) - The RS format uses R3 to point at the register containing a third operand (if used).

SI (storage and immediate operand) - The SI format provides an immediate operand (I2 contents) and an operand address - (B1) + D1.

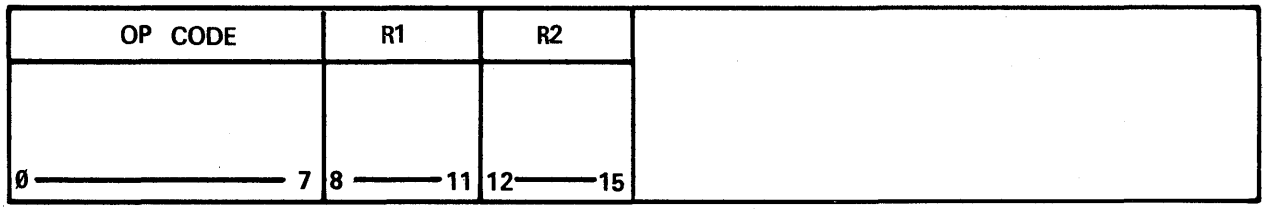
Note: The designator subscript identifies the associated operand. B1 is associated with Operand 1.

WORD AND INSTRUCTION FORMATS

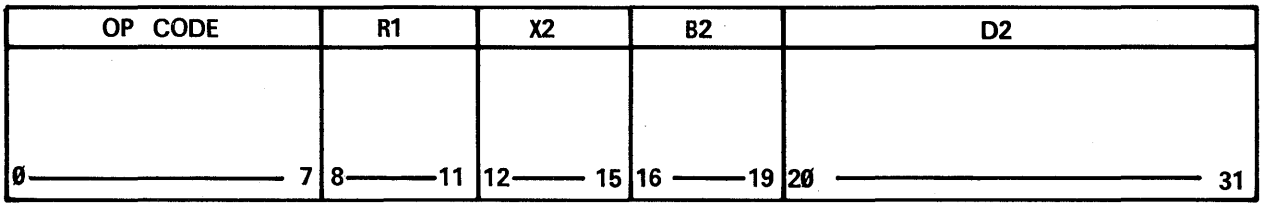


WORD FORMAT

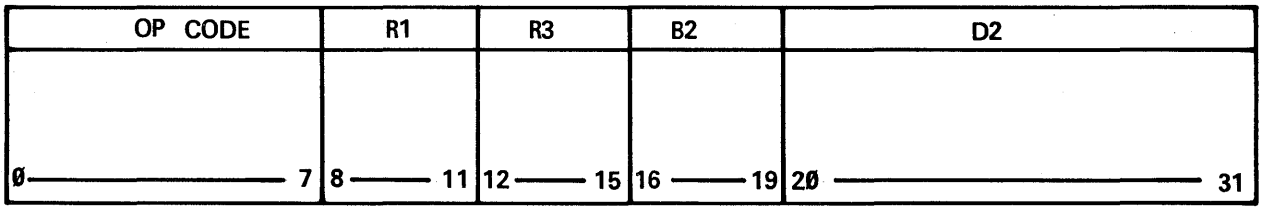
INSTRUCTION FORMAT



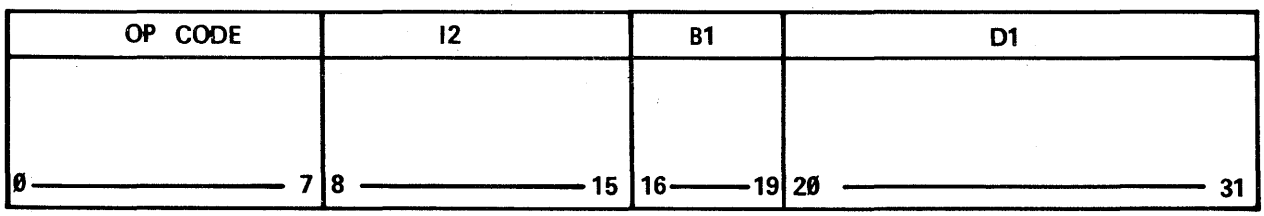
RR FORMAT



RX FORMAT



RS FORMAT



SI FORMAT

PROGRAM STATUS WORD

PSW - Contains the information required for execution. The PSW is always zero upon initialization.

3 classes - current (Prog. in control)
- becomes return upon interrupt
- new is fetched corresponding to interrupt type

Upon interrupt the PSW for the interrupted program is stored by type of interrupt in a certain location in fixed memory and a new PSW is placed in the PSR.

Mask bits (M) - when set to zero's - inhibits all interrupts. If set to 1 - allows the interrupt.
I/O A Channel Ø. Channel Ø (GPCC) interrupts are tabled.
I/O B Channels 1-6. Interrupts are stacked until allowed, then requested.
Last interrupt (7) for the interval timer.

P - Ø - supervisor mode (allows execution of the priviledged instructions).
1 - problem mode (or user mode)

CC - condition codes: (vary with the instruction, some use only 2 conditions)

ØØ - Equal
Ø1 - Less than
1Ø - Greater than
11 - Overflow

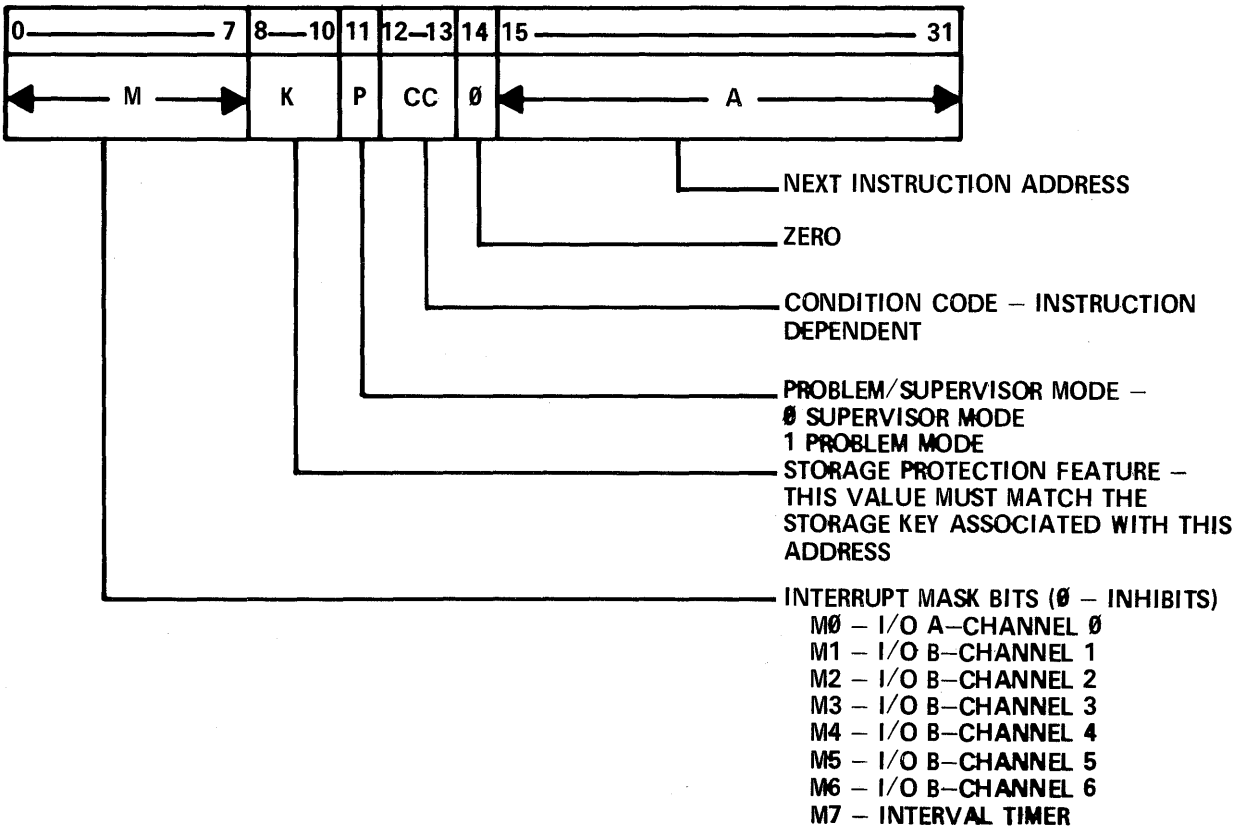
K - storage protect

Ø - Exec can reference anything no matter what the program key.
1 - Problem program
2-7 - Values for the user

Address = 18 bits

Upper 6 bits point to one of the hardware registers associated with each 2048 byte bank.
If the value in that register is equal to the value of the K-field in PSW, reference to the block of storage is allowed.
Otherwise an error occurs.

P S W


0 7
8 10
11
12–13
14
15 31
M
K
P
CC
Ø
A
NEXT INSTRUCTION ADDRESS
ZERO
CONDITION CODE – INSTRUCTION DEPENDENT
PROBLEM/SUPERVISOR MODE –
Ø SUPERVISOR MODE
1 PROBLEM MODE
STORAGE PROTECTION FEATURE –
THIS VALUE MUST MATCH THE STORAGE KEY ASSOCIATED WITH THIS ADDRESS
INTERRUPT MASK BITS (Ø – INHIBITS)
MØ – I/O A–CHANNEL Ø
M1 – I/O B–CHANNEL 1
M2 – I/O B–CHANNEL 2
M3 – I/O B–CHANNEL 3
M4 – I/O B–CHANNEL 4
M5 – I/O B–CHANNEL 5
M6 – I/O B–CHANNEL 6
M7 – INTERVAL TIMER

STORAGE PROTECT

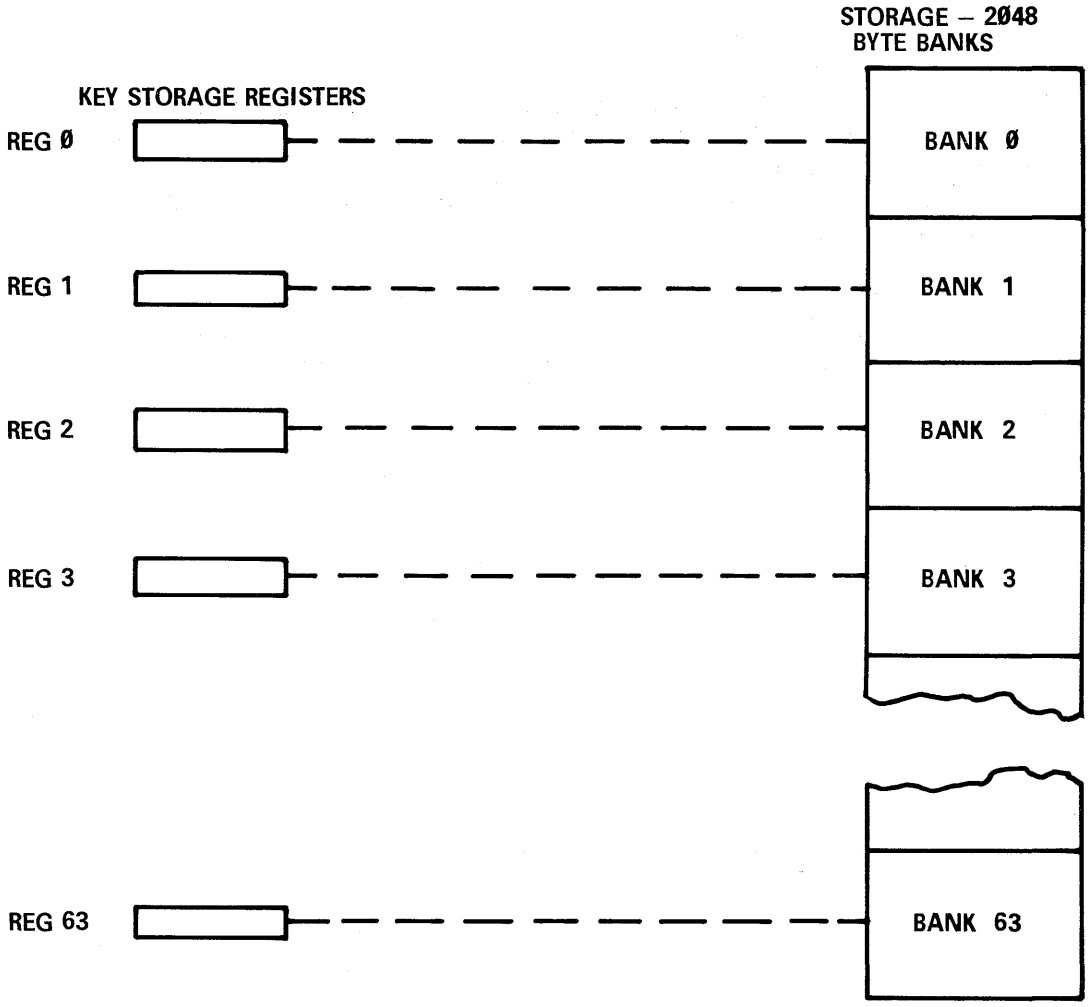
Storage is divided in 2048 byte blocks. Associated with each block is a set of hardware registers called key storage registers. These registers provide the basic protection for storage capacities up to 65K. Each register holds a 3-bit value for a maximum of 8 different storage keys.

When access to storage is initiated by the processor or I/O, the six most significant bits of the storage byte address select a location in the Key Memory which corresponds to the block of storage that is addressed. The Storage Key in the selected Key Memory location is compared for equality with the PSW key or in the case of I/O, with the I/O Protect Key. If the result is either that the two three-bit keys are equal or that the PSW Key (Protect Key if I/O) is binary zero (000), a match condition exists and access to storage is granted.

Otherwise, the processor signals the storage to abort and not execute the write or read cycle and a storage protection error is set which generates a Program/Machine Check class interrupt request. The Program Machine Check interrupt request is generated only if the storage protection error occurs on a storage access initiated by the processor. The action taken by the C/SP when a storage protection error occurs on an access initiated by an I/O Channel is described in the individual I/O channels that use storage protection.

Note that a PSW Key in the current PSW (or in the case of I/O, an I/O Protect Key) of binary zero (000) grants access to any storage block.

STORAGE PROTECT



INTERVAL TIMER

The Interval Timer is a feature in the processor which provides interval timing and time of day information. The Interval Timer can request service only at the end of a processor instruction execution prior to staticizing the next instruction. The processor is locked out during the entire interval timer service sequence. (I/O service sequences may be interlaced with timer in a normal manner as established by the storage priority). The interval timer requests service every 6 milliseconds. When a request for service is granted, the low order halfword of the Interval Timer is read out of storage (if C does not go to zero). If C goes to zero, the upper half is also read-out from storage and the T-field is incremented by 1. The R-field transferred into the C-field (for the new interval count), the interval timer class interrupt request is generated, the updated ITW is transferred back to storage and the service sequence ends.

The controlling program sets the C & R-field values, thus having full flexibility of controlling the interval of interrupt request and incrementation of the T-field. If the C-field is zero and the R-field is zero, the timer counting and generation of interrupt request, an IT request which is pending when next service request is generated has no effect on the service sequence with the exception, if the C-field is reduced to zero the pending interrupt is lost, (i.e., the request is still present but the timer holds only one interrupt request).

If the program desires access to the entire ITW, it must fetch the full word in one instruction, so as not to permit the timer to execute a service sequence and possible modify the ITW before the other halfword is fetched.

Bit 7 (M7) of the PSW when set to 1 permits interruption from the IT. If zero the timer cannot interrupt. Service sequences continue normally, but the interrupt request, when generated, remains pending. If the interval timer disable switch on the processor maintenance panel is in the on position, all timer service sequences are inhibited.

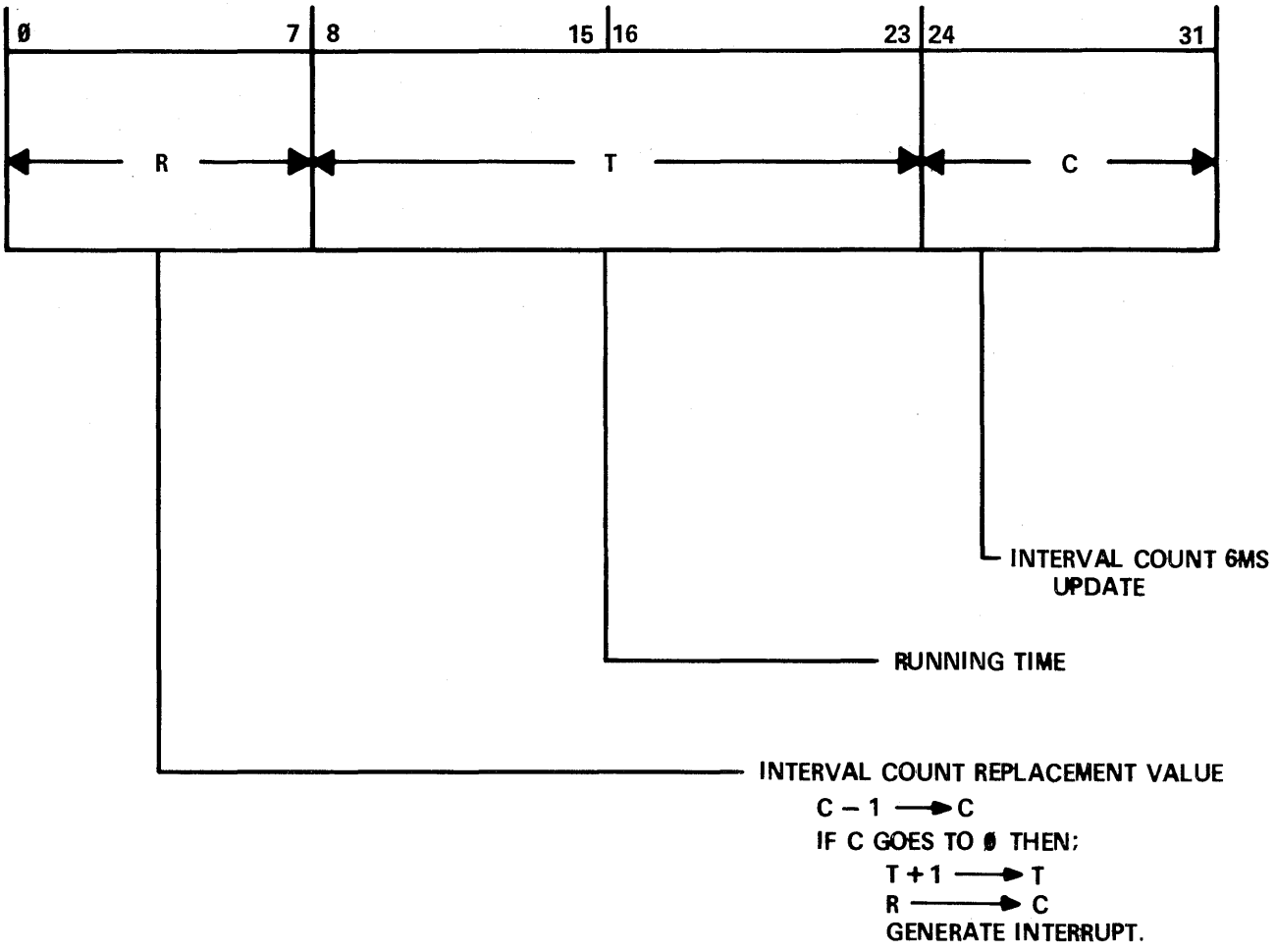
Timer service sequences are also inhibited:

1. When processor is in the one cycle mode.
2. When processor is in the one instruction mode.
*3. When processor is in the initial load mode.
*4. When processor is stopped because of HPR instruction.
*5. When processor is stopped because of detection of a tract stop.
6. When non-recoverable error has occurred.
*7. When processor is stopped due to a recoverable error detection and the stop on error switch on the maintenance panel is in 'on' position.
*8. When processor is stopped and is in the cleared state.

*-. These cases the Interval Timer service can resume at the end of the first instruction execution following the depression of the run switch.

The timer is assigned to the Interval Timer class of interrupt. When an interrupt request is accepted by the processor a status half word and an interrupt code half word are stored in fixed memory locations.

INTERVAL TIMER



C/SP INTERRUPT SEQUENCE

Interrupts

Automatic means to alert the C/SP processor to an exceptional or unexpected condition (end of I/O operation, program errors, machine errors, etc.) thus directing the processor to the appropriate program routine for handling. The system provides for interrupting any task in order to take on a task of higher priority.

Interrupt Sequence: 1. Begins by transferring the current PSW to fixed location in storage ('Return' PSW 2-3. Then the status half word and interrupt code half word is transferred to the assigned location. 4. 'New' PSW is fetched from the fixed location. 'New' becomes 'current' PSW and after processing, the processor can return to the interrupted program (load 'return' PSW) via the LPSW instruction. In certain cases of simultaneously presented interrupts, it is possible to execute more than one interrupt sequence before instruction processing is resumed.

Interrupt Class/Priority: There are 5 classes of interrupts; Supervisor Call, Program-Machine check (PMC), Interval Timer I/O B, I/O A. Within the classes may be several specific sources of interrupt requests.

I/O A, I/O B, and interval timer interrupt requests are controlled by the system mask bits in the 'current' PSW. If bits are set to zero the corresponding channel is not permitted to interrupt. No mask bit control exists over the supervisor call class and all interrupt requests are accepted (in this class). PMC interrupt requests are always accepted unless the processor is executing a PMC interrupt subroutine.

Interrupt Priority: It is possible to execute more than one interrupt sequence between instruction executions. The system mask bits (PSW) become effective immediately and therefore control subsequent interrupt sequences.

The order of executing the contiguous interrupt sequences varies and is a function of the pending instruction requests and mask bits.

The interrupt sequence selected is determined by the following priority:

1. PMC (invalid address strg. protection, or parity, 2. Interval Timing, 3. I/O B, 4. I/O A, 5. PMC (power failure, invalid operation, etc.)

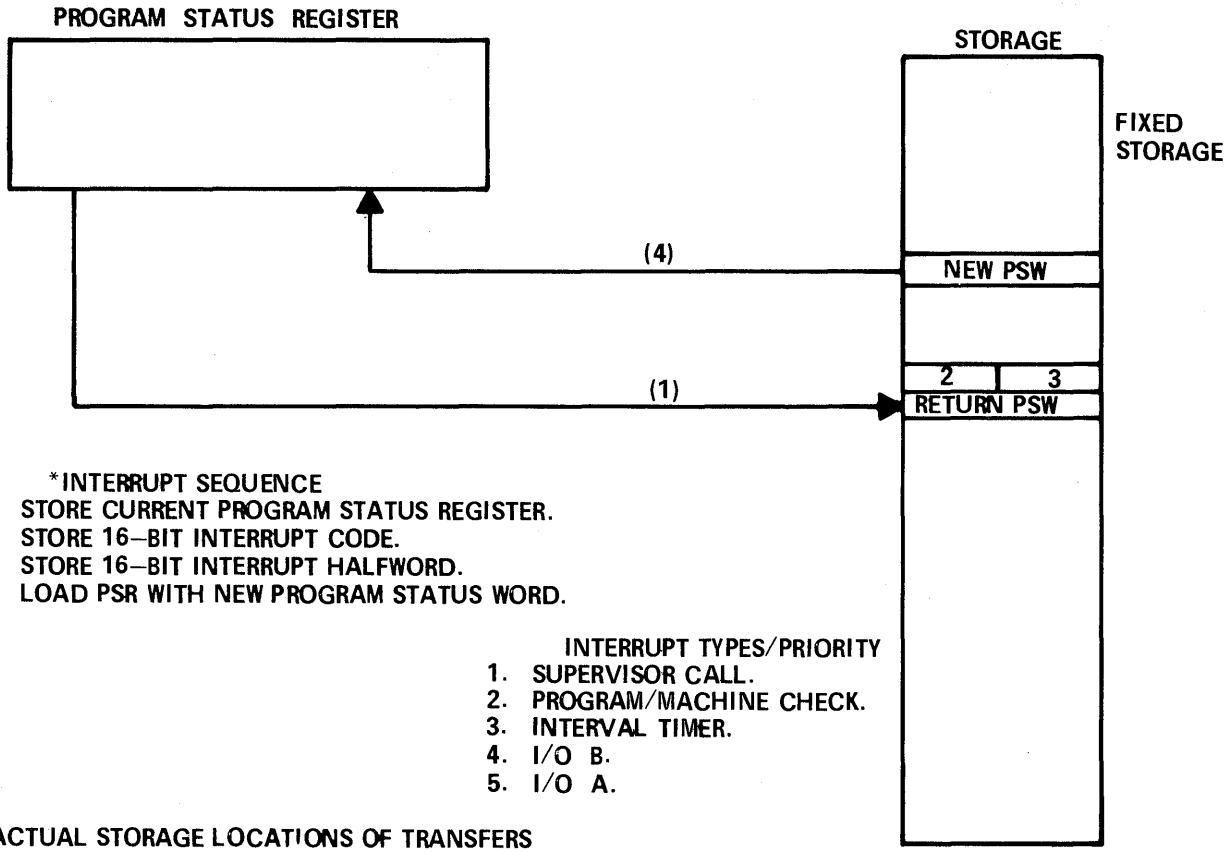
Supervisor Call is not included as the storing and fetching of PSW's is done in the execution phase of the instruction and should not be thought of as an interrupt sequence in the context described.

This does not determine the order, only indicates which interval sequence is selected when simultaneous interrupt requests are made. Example: if I/O A and I/O B interrupt request are presented simultaneously I/O B is processed first.

The final contents of PSW determine which interrrupt subroutine is entered, so the order of executing these subroutines is reversed from the order of executing the interrupt Sequence.

See Appendix A for more information.

INTERRUPT SEQUENCE



*INTERRUPT SEQUENCE

1. STORE CURRENT PROGRAM STATUS REGISTER.
2. STORE 16–BIT INTERRUPT CODE.
3. STORE 16–BIT INTERRUPT HALFWORD.
4. LOAD PSR WITH NEW PROGRAM STATUS WORD.

INTERRUPT TYPES/PRIORITY

1. SUPERVISOR CALL.
2. PROGRAM/MACHINE CHECK.
3. INTERVAL TIMER.
4. I/O B.
5. I/O A.

*ACTUAL STORAGE LOCATIONS OF TRANSFERS DEPENDENT ON INTERRUPT TYPES.

INTERRUPT CLASS AND CODE

During the interrupt sequence the status halfword and interrupt code halfword are transferred to the assigned locations in fixed memory.

I/O A class interrupt is assigned to channel zero. Channel 0 is reserved for the GPCC and the bits identifying the channel ID, channel #, device address are all set to 0 by the hardware as the channel ID and # equal zero and the device address is contained in the CIW.

I/O B class interrupts are assigned to channels 1-6. Bit 16 is set to 0, bits 17-19 are the channel identification code, bit 20 is set to 0, bits 21-23 are the channel number (1-6), and bits 24-31 are the device address.

The Interval Timer interrupt code halfword is always set to 0 by the hardware (timer).

PMC has a value for each type of interrupt within this class.

Supervisor Call- the 'R' bits are the bits from the SVC fields R1 & R2.

INTERRUPT CODE HALFWORD

INTERRUPT CLASS	INTERRUPT CODE
	BITS 16 ——— 31
I/O A	
CHANNEL Ø	Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø
	CHANNEL:
I/O B	I. D. NUMBER DEVICE ADDRESS
CHANNEL 0	Ø C C C Ø Ø Ø Ø D D D D D D D D
CHANNEL 1	Ø C C C Ø Ø Ø 1 D D D D D D D D
CHANNEL 2	Ø C C C Ø Ø 1 Ø D D D D D D D D
CHANNEL 3	Ø C C C Ø Ø 1 1 D D D D D D D D
CHANNEL 4	Ø C C C Ø 1 Ø Ø D D D D D D D D
CHANNEL 5	Ø C C C Ø 1 Ø 1 D D D D D D D D
CHANNEL 6	Ø C C C Ø 1 1 Ø D D D D D D D D
INTERVAL TIMER	Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø
PROGRAM/MACHINE CHECK (PMC)	
POWER FAILURE	Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø 1
PARITY	Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø 1 Ø
INVALID OPERATION	Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø 1 Ø Ø
PRIVILEGED OPERATION	Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø 1 Ø 1
STORAGE PROTECTION	Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø 1 1 Ø
INVALID ADDRESS	Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø 1 1 1
FORCE PMC SWITCH	Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø 1 Ø Ø Ø
MONITOR SWITCH	Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø 1 Ø Ø Ø Ø
SUPERVISOR CALL	Ø Ø Ø Ø Ø Ø Ø R R R R R R R R

C – CHANNEL IDENTIFICATION CODE
- Ø Ø Ø – GPCC
- Ø Ø 1 – SDC
- Ø 1 Ø – ICA
- 1 Ø Ø – SELECTOR
- 1 Ø 1 – MULTIPLEXER

INTERRUPT CLASS AND STATUS

The status halfword is stored during the interrupt sequence.

I/O A class interrupt- If bit 15 is set, indicates an error occurred on attempt to store a CIW and no CIW was stored.

I/O B class interrupt- The status is covered during the discussion of the individual channels.

Interval Timer status halfword- If bit 15 is set, indicates a parity error was detected when the Interval Timer read out one of the halfwords of the Interval Timer Word.

Program/Machine check and the Supervisor Call interrupts do not generate any status and these status halfwords are set to 0.

STATUS HALFWORD

INTERRUPT CLASS	STATUS HALFWORD
	BITS Ø ——— 15
I/O A	Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø E_1
I/O B	REFER TO INDIVIDUAL I/O CHANNEL
INTERVAL TIMER	Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø E_2
PROGRAM/MACHINE CHECK	Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø
SUPERVISOR CALL	Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø

* E_1 -- ERROR OCCURRED ON ATTEMPT TO READ OUT CIW CONTROL LIST

E_2 -- ERROR OCCURRED ON ATTEMPT TO READ OUT INTERVAL TIMER

START I/O INSTRUCTION

All input/output operations are initiated by this instruction. The effect of the SIO varies and is a function of the channel to which it is directed.

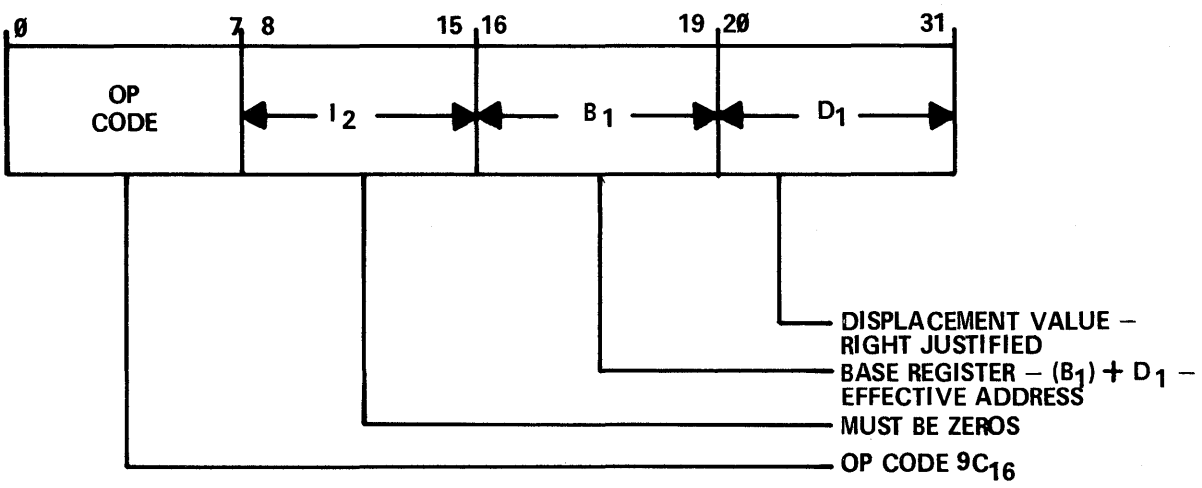
The operation code is 9C hexadecimal.
Bits 8-15 are not used and are set to zero.

B_1 - The number of the general register which holds the base address for operand 1.

D_1 - The displacement value for the base address of Operand 1.

The addition of the contents of B_1 and the value of D_1 fields form the effective address which is the channel number and device address to start the I/O sequence.

START I/O INSTRUCTION



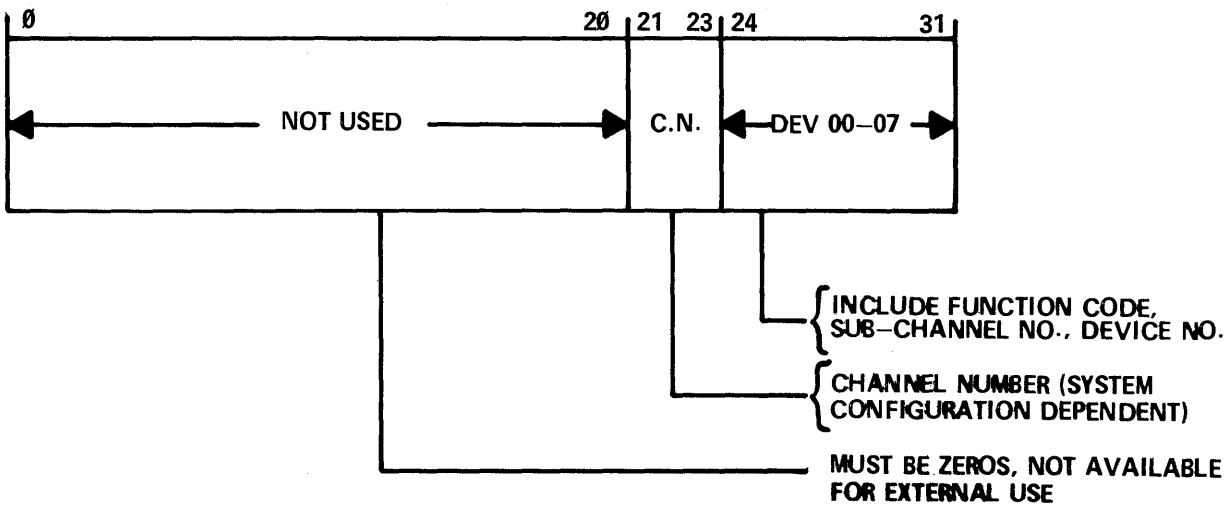
EFFECTIVE ADDRESS (SIO)

Bits 0-20 are set to zero and are not available for external use.

Bits 21-23 contain the channel number depending on the configuration.

Bits 24-31 contain the function to be performed, the sub-channel or control unit and the device number (8-bits referred to as DEV 00-07).

DEVICE ADDRESS FORMED BY $(B_1) + D_1$



DEV 00-07 FORMAT (SIO)

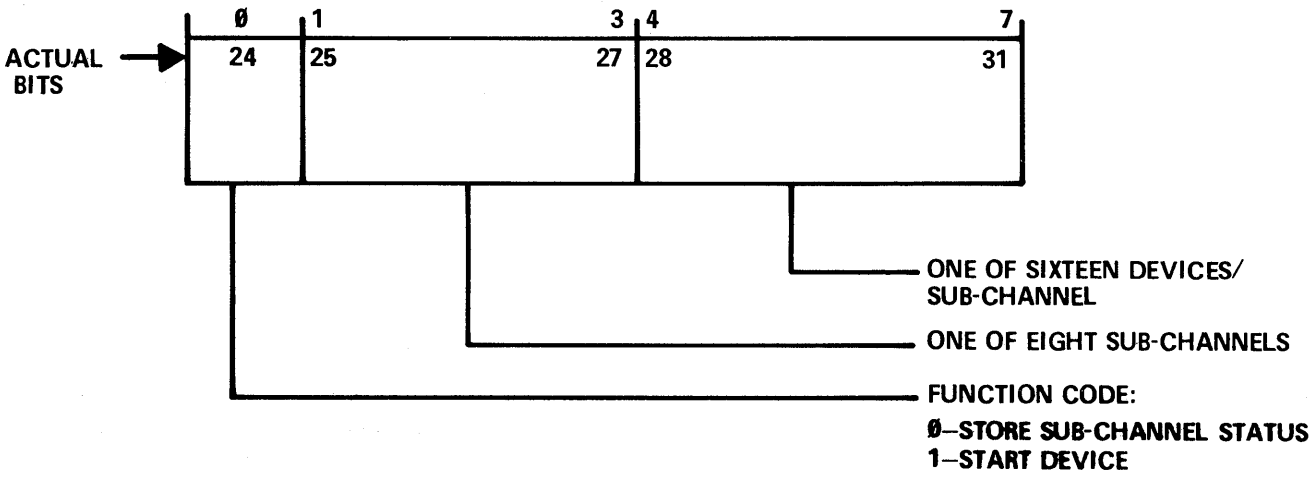
The 8-bits of DEV ØØ-Ø7 are indicated as:

bit Ø (24) - function code: If set, start the device; If not set, store the sub-channel status.

bit 1-3 (25-27) - Indicates which of the 8 sub-channels to perform the function on.

bit 4-7 (28-31) - Indicates which one of the 16 devices on the subchannel to perform the function on.

DEV 00–07 FORM



I/O FLOW

The overall I/O Flow involved in using the SIO instruction is as follows:

The program must first store a Channel Address Word (CAW) in fixed memory. The Channel Address Word, in general, contains a command to an input/output device or an address of such a command. In this case, the CAW indicates an address of a Channel Command Word (CCW-2 words). The CCW indicate the operation to be performed, the address of first byte of data to be transferred and the byte count.

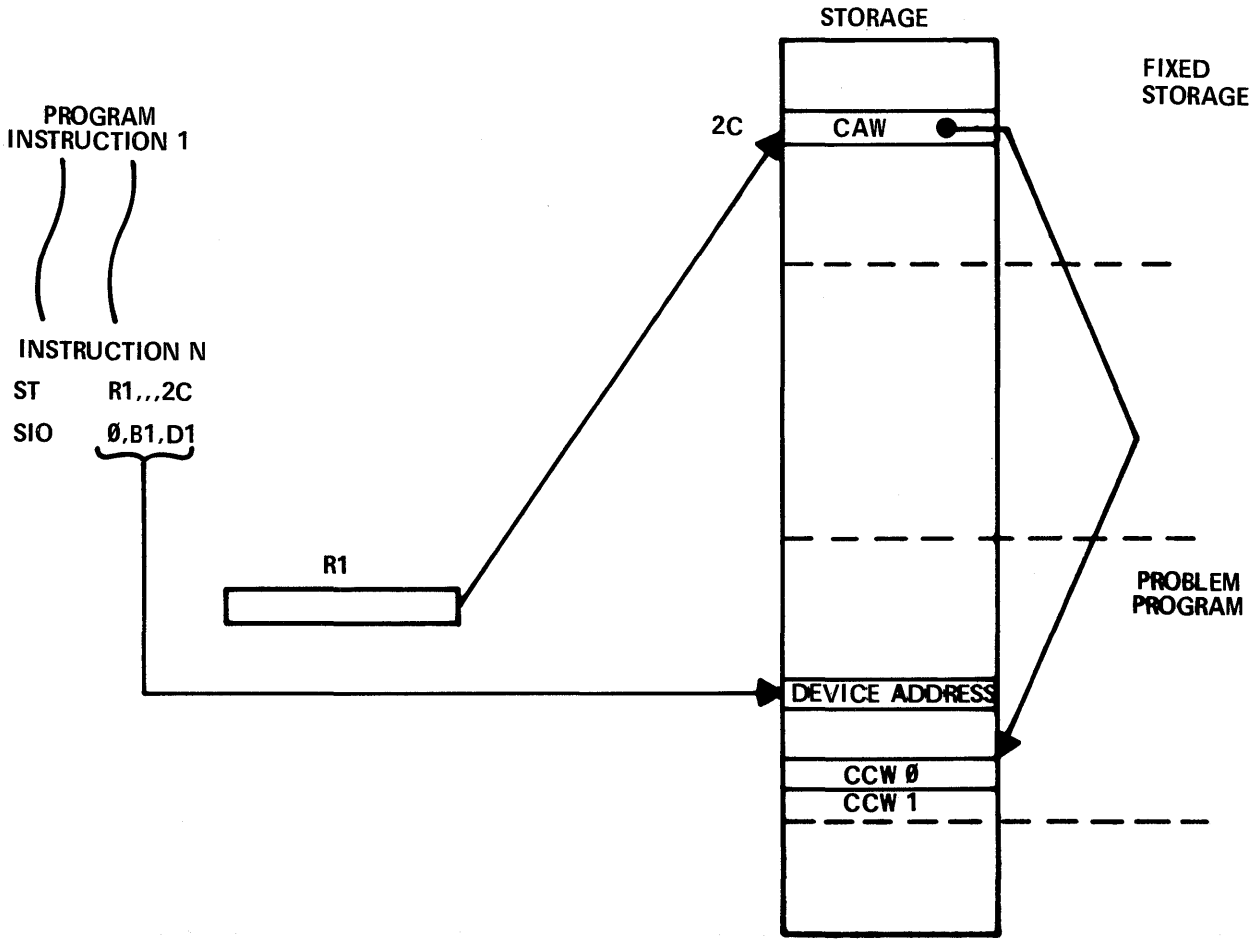
1. Store the CAW in fixed memory.

2. Issue SIO instruction.
   a. Before the channel responds with the condition code, it fetches the CAW and holds it in its hardware as required by the operation to be performed.

3. The channel gets the address of the Channel Command Word (CCW) from the CAW and the process is initiated.

NOTE: The operand field of the SIO instruction pointing to the device address does not mean the device address is in memory. This was done to show that the contents of B_1 register added to the value D_1 forms the device address.

I/O FLOW


STORAGE
FIXED STORAGE
PROGRAM INSTRUCTION 1
INSTRUCTION N
ST R1,,,2C
SIO Ø,B1,D1
2C
CAW
R1
PROBLEM PROGRAM
DEVICE ADDRESS
CCW Ø
CCW 1

Appendix A

A flip-flop is set in an interrupt sequence provided the 'current' PSW is loaded from PMC 'new' PSW. All subsequent PMC requests are not accepted. The flip-flop is reset by executing a LPSW instruction (or system clear switch on processor maintenance panel). A non-recoverable error situation then exists and the processor is stopped if any of the following occur: 1. PMC class interrupt request is generated, 2. Parity error when PSW is read from storage during an interrupt Sequence (including during the execution of a supervisor call instruction - SVC), 3. Parity error when PSW is read from storage during execution of LPSW instruction, 4. Recovery of program time out check Retriggerable Delay Flop (RDF) circuit. *

Processor Action: 1. Abnormal light on maintenance panel, 2. signal to generate PMC interrupt request, 3. turn off timing pulse clock, 4. generate channel clear signal to all attached channels.

Cause of the non-recoverable error may be determined by examining the indicators on maintenance panel and then reset by depressing system clear switch.

Interrupt Timing: The interrupt sequence takes place only at the end of an instruction execution and before a new instruction is started. The processor either waits until the end of the instruction before executing the interrupt sequence or it ends the instruction early; then it executes the interrupt sequence. If the processor waits until instruction has ended, it is then termed as 'completed'. The PSW then points to next instruction in program. If processor ends the instruction early, the instruction execution is termed 'suppressed' or 'terminated'. Suppressed - effect is as if no operation was specified (Results not stored and CC not changed).

Terminated: All, part, or none of the result will be stored and results are unpredictable. The next instruction address in 'Return' PSW points to the address of the instruction which was suppressed or terminated. An exception to this is the detection of a storage protection or invalid address error when fetching the first half word of an instruction to be executed following a branch instruction. Then the PSW holds the address of the branch instruction.

* Certain processor component malfunctions may cause the processor to enter a stalled condition or a program loop condition which would not result in a detected error and generation of a PMC interrupt. To assist in detecting an error of this type a SIO is issued to a pseudo I/O channel (7) only for this PMC function. The SIO issued to channel 7 triggers A 1.0-1.5 second retriggerable delay flop. A properly running program contains enough SIO instructions to insure the RDF never recovers.

NOTES

SECTION II

SPECIAL DEVICE CHANNEL

SECTION II INDEX – SPECIAL DEVICE CHANNEL

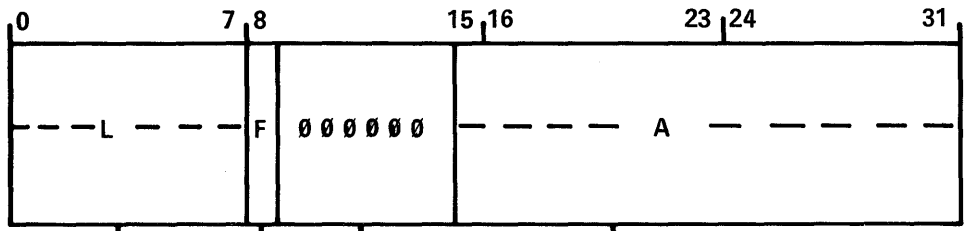
Special Device Channel (SDC)

The SDC provides the means for local program loading and maintenance using a card reader (Type 0708-27/28) which is 80 column 80 cards per minute reader.

Operation of the card reader is initiated by the C/SP program issuing a Start I/O (SIO) instruction. The SIO specifies a channel number and a device address. The SDC channel number is always 6 and the device address for the card reader is 02_{16}. Before the SIO is issued, a CAW must be scored in fixed memory location $2C_{16}$.

CAW - L - number of bytes to be transferred. Maximum if 256 bytes.
For the card reader the number is always 80 bytes.
A SIO is issued for each card to be read.
F if set, indicates termination upon detection of EOT.
Bits 9-14 set to zero by the controlling program.
A address to be used in the storage of data and is incremented as each byte is transferred.

CHANNEL ADDRESS WORD
SDC



ADDRESS OF STORAGE WHERE TRANSFER WILL BEGIN; WILL BE INCREMENTED BY 1 UPON TRANSFER OF ONE BYTE.

NOT USED MUST BE ZERO.

IF SET WILL TERMINATE CHANNEL UPON DETECTING EOT; MUST BE ZERO WHEN SIO ISSUED FOR CARD READER.

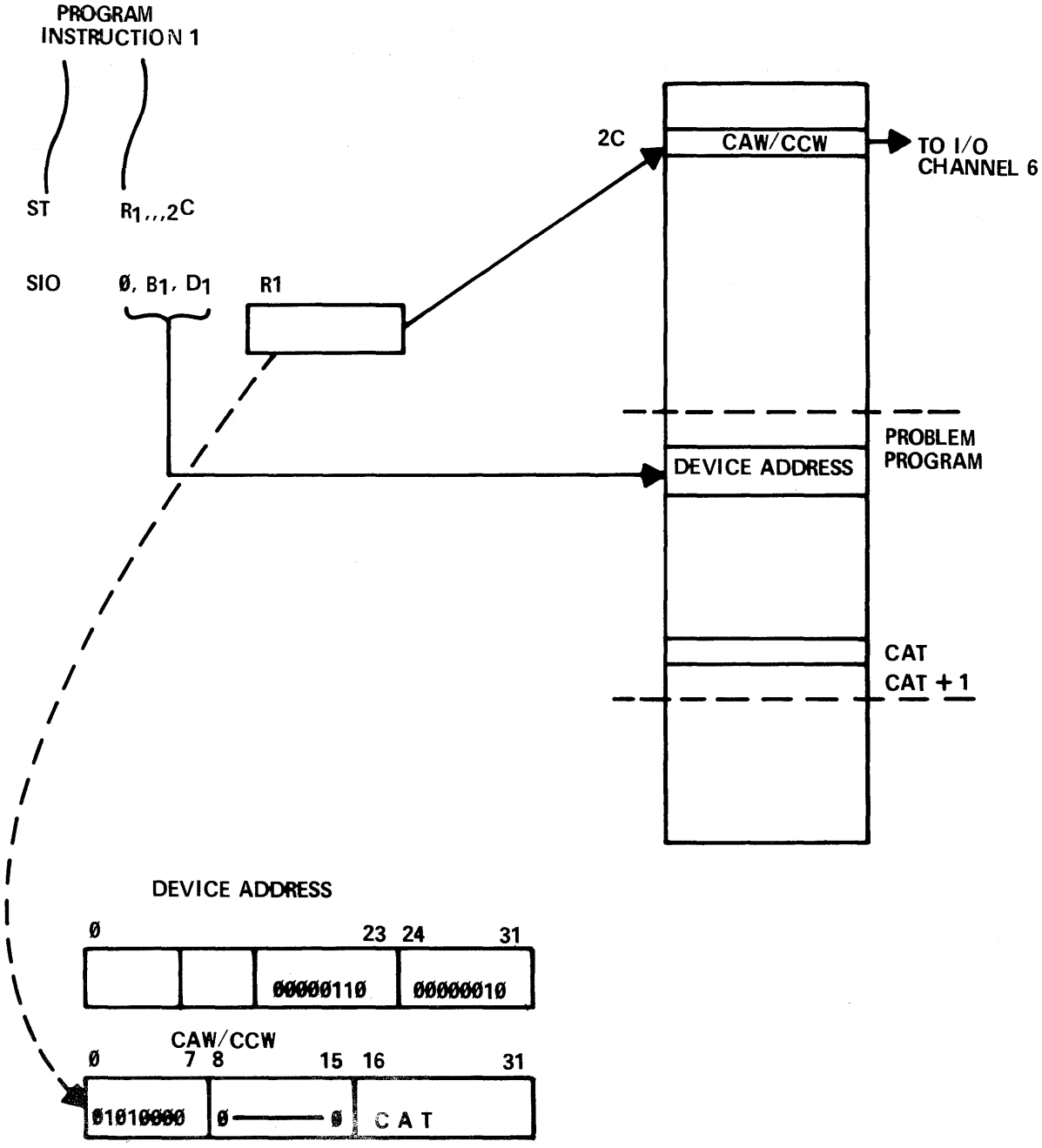
SPECIFIES NUMBER OF BYTES TO BE TRANSFERRED UNLESS EOT DETECTED. COUNT DECREMENTED BY ONE FOR EACH TRANSFER. MAXIMUM COUNT IS 256 BYTES WHICH HAS A VALUE OF 00_{16}. FOR CARD READER VALUE MUST BE 50_{16} (80 BYTES).

SDC General I/O Flow

The controlling program stores the CAW in fixed memory location $2C_{16}$. Since the card reader performs only one function (read one card) there are no external functions to be decided in the SDC, and there is no need to reference a Channel Command Word (CCW) as the CAW specifies the starting storage address, byte count and control bit for EOT.

1. Store the CAW in $2C_{16}$.
2. Issue SIO instruction.
3. The SDC fetches the CAW and holds the contents as required by the I/O operation to be performed (during the SIO time - before the SDC returns a condition code to C/SP).
4. The channel then initiates and controls the operation of the I/O device and the transfer of data between the device and storage.

SDC GENERAL I/O FLOW



Condition Code Settings

SIO with a Device Address of:

00 - Keyboard
01 - Incremental Printer
02 - Card Reader

Device address of 80_{16} indicates keyboard lockout and the SDC does not fetch the CAW.

Device address of 40_{16} indicates a test I/O function and the channel does not fetch the CAW.

I/O Pending Status - location 6C and 6D of fixed memory allow software to pick up status information without requiring the acceptance of an interrupt. Some channels store status in these location during SIO time when function of SIO is TIO. Some will store status when function is not TIO, such as end of operation or when pending status is the only thing preventing the channel or attached control unit from accepting a new command.

GPCC does <u>not</u> use pending status.

CONDITION CODE SETTINGS
SDC

SIO D.A. ØØ, Ø1, Ø2,

CC = ØØ	SIO EXECUTED
CC = Ø1	PARITY ERROR ON CAW FETCH
CC = 1Ø	BUSY EXECUTING PREVIOUS OPERATION
CC = 11	SDC OF LINE

SIO D.A. 8Ø

CC = ØØ/11	KEYBOARD NOT BUSY
CC = Ø1	NOT USED
CC = 1Ø	BUSY; WILL BE LOCKED OUT AFTER PREVIOUS OPERATION TERMINATES

SIO D.A. 4Ø

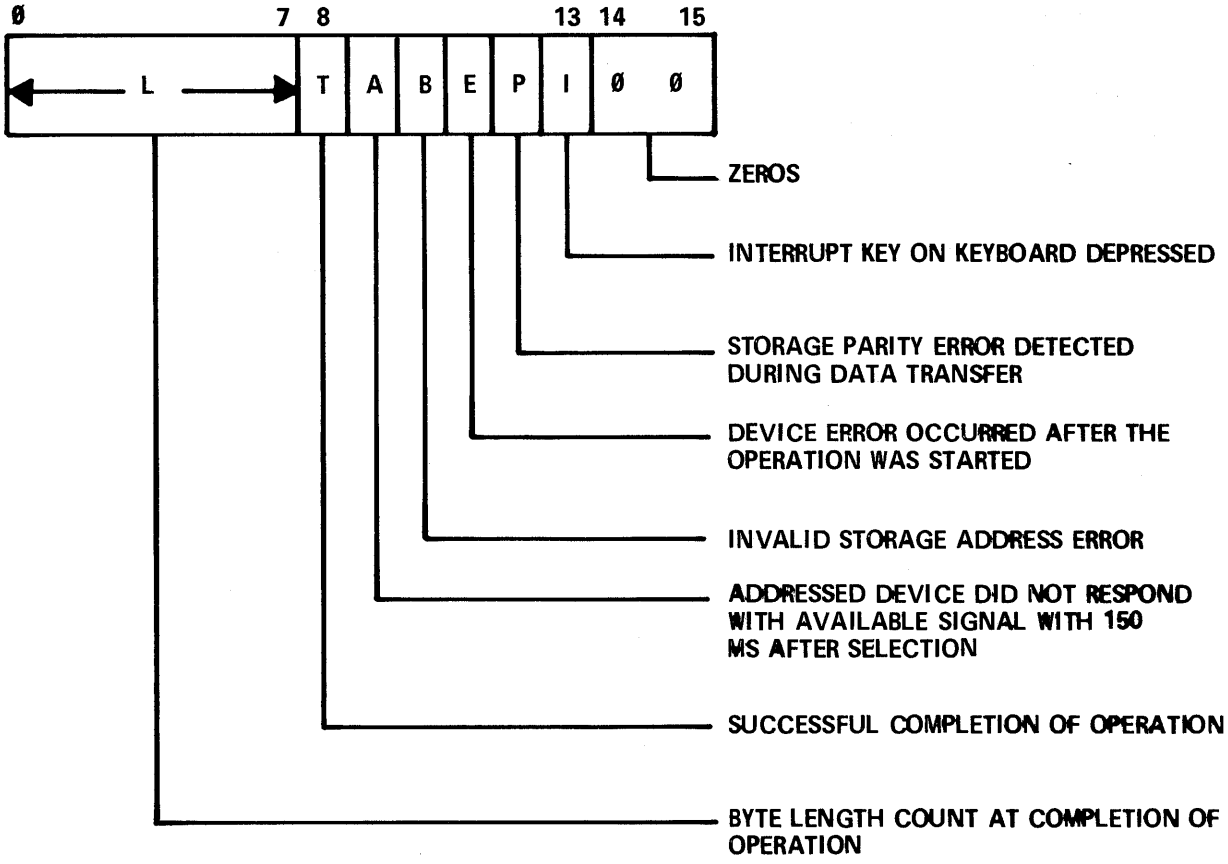
CC = ØØ/11	NOT BUSY
CC = Ø1	HOLDING PENDING STATUS
CC = 1Ø	BUSY

SDC Status Halfword

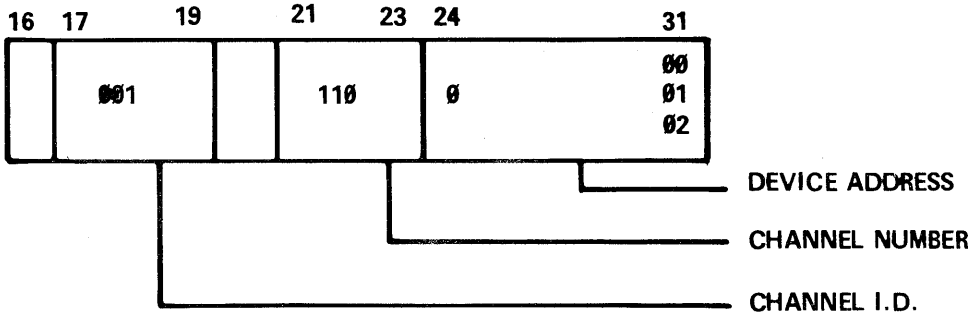
The SDC generates an interrupt request of the I/O B class upon completion of a data transfer error condition, or in response to the interrupt key on keyboard (if keyboard is attached). When the C/SP grants the interrupt request, the SDC stores interrupt code and status in the respective half word location in fixed memory.

The interrupt code halfword indicates the channel identification in bits 17-19 and is set to 001_2 by the SDC. Bits 21-23 are the channel number and set to 110_2 by the SDC. Bits 24-31 is the device address (Ø - keyboard, Ø1 - printer, Ø2 - card reader).

STATUS HALFWORD



INTERRUPT CODE HALFWORD



INITIALIZE CARD READER (SDC)

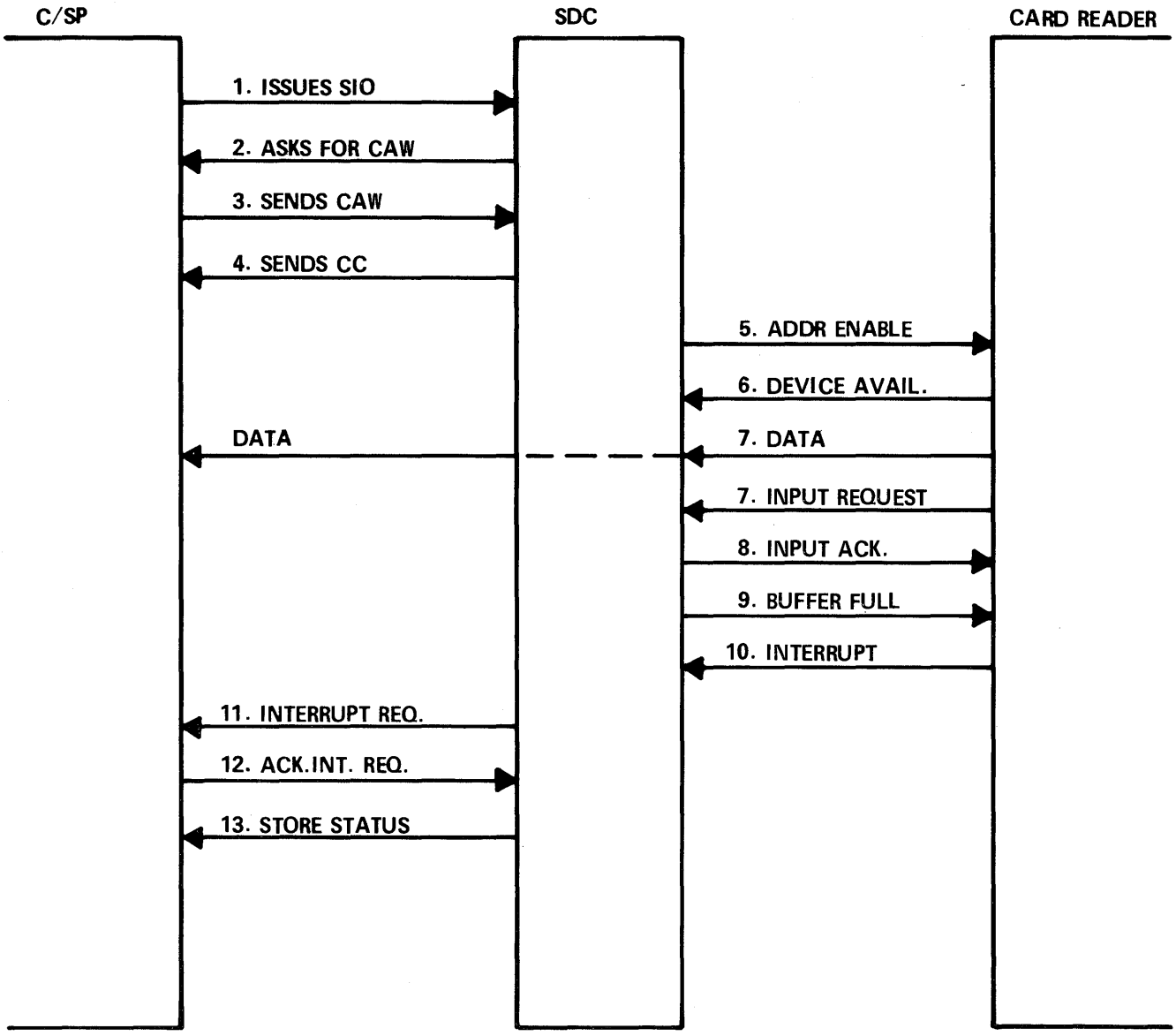
C/SP → SDC - The CAW has been stored in fixed memory.

1. C/SP issues the SIO instruction.
2-3. During the SIO time the SDC asks for and receives from the C/SP the Channel Address Word (CAW). Assume the channel is not busy.
4. The SDC responds with the condition code of ØØ.. SIO was executed.

SDC → Card Reader control unit

5. SDC generates an Address Enable Request.
6. CR control unit responds with Device Available.
7. CR control unit puts the data on the data lines and generates an Input Request at the same time.
8. SDC responds with an Input Acknowledge when the data has been stored.
9. When the byte count goes to zero (or error condition detected) SDC generates a Buffer Full signal.
10. CR control unit responds with an Interrupt signal which signals the SDC to generate an interrupt request to the C/SP.
11. SDC generates an Interrupt Request to C/SP.
12. C/SP generates an Acknowledge of the Interrupt Request indicating the C/SP is able to process the interrupt.
13. The SDC stores the status halfword and interrupt code halfword in the fixed memory locations for I/O B class of interrupt.

INITIALIZE SDC (CARD READER)



SECTION III

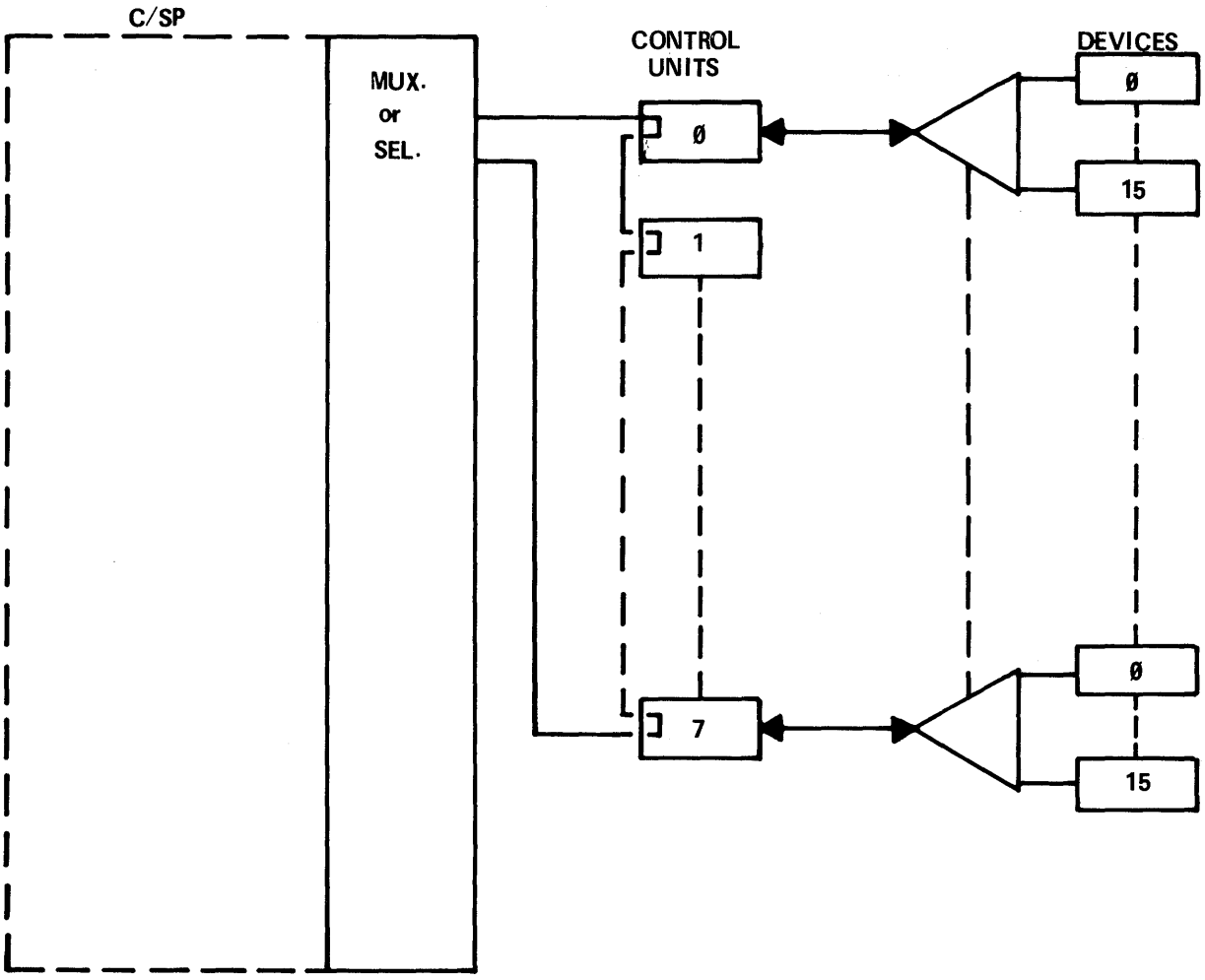
MULTIPLEXER/SELECTOR CHANNEL

SECTION III INDEX – MULTIPLEXER/SELECTOR CHANNEL

MULTIPLEXER/SELECTOR CHANNEL (MUX/SEL

The multiplexer and selector channels may be connected up to 8 control units which may be connected up to 16 devices, operating in half duplex mode (one transfer at a time). The channel provides general purpose channel programming, including command chaining, data chaining, transfer in channel and skip commands. The channel interfaces with main storage through the control section of the C/SP.

C/SP MULTIPLEXER/SELECTOR SELECTOR CHANNEL



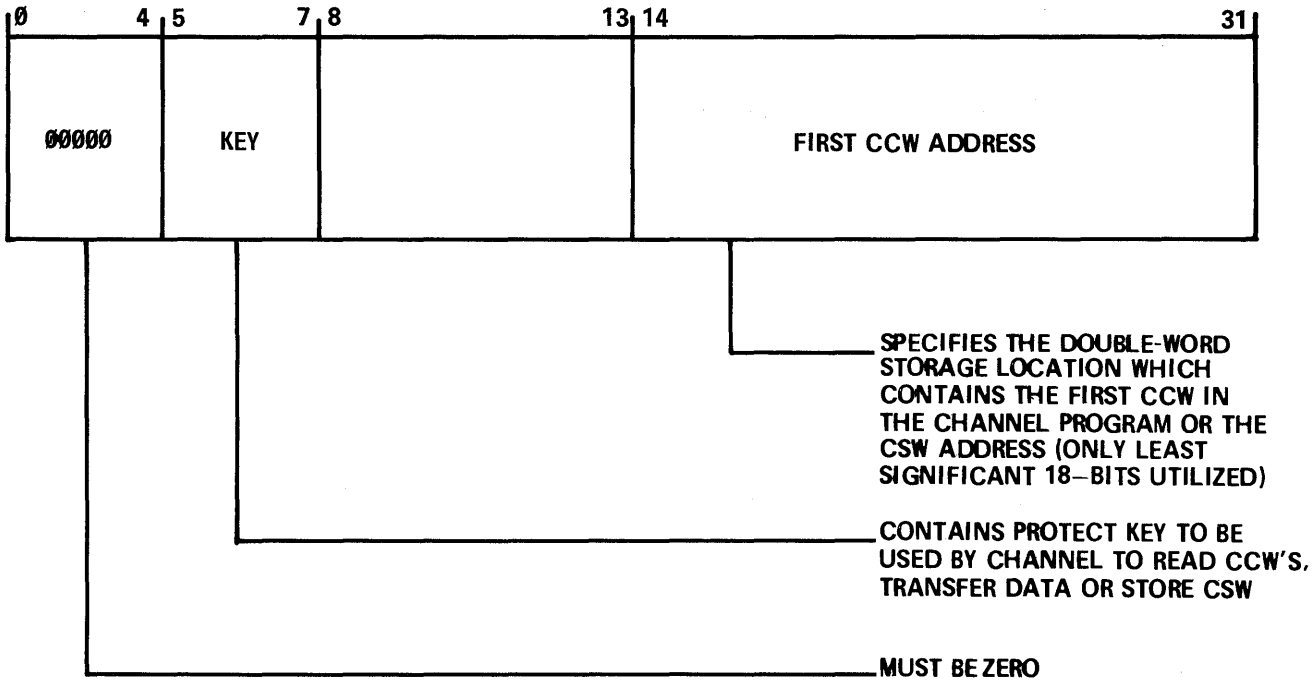
CHANNEL ADDRESS WORD (CAW)

The CAW must be set before issuing the SIO instruction (Address $2C_{16}$ in C/SP fixed memory).

bits 5-7: contain the storage - I/O protection key to be used by the channel to read the Channel Command Words (CCW), transfer data, or store the Channel Status Word (CSW).

bits 8-31: Specifies the storage location of the first Channel Command Word (CCW) if the function of the SIO instruction is to start the device. If the function is to store sub-channel status, the address of the Channel Status Word (CSW) is contained in these bit positions. Only the least significant 18 bits are utilized.

CHANNEL ADDRESS WORD
M/S



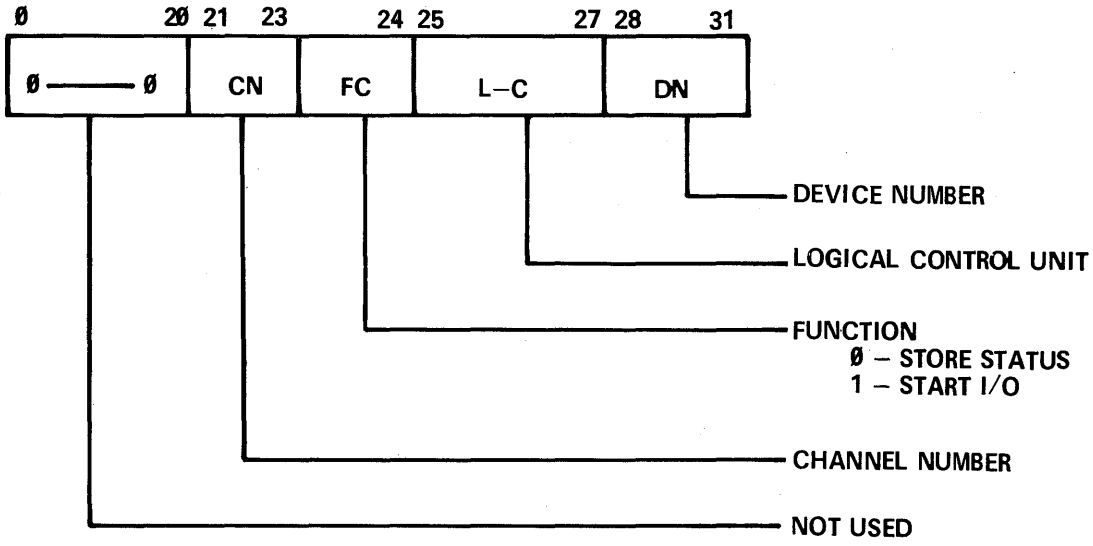
$(B_1) + D_1$ OF START I/O INSTRUCTION

Initiation of an I/O operation is by the SIO instruction specifying the channel number, and the address of the device associated with the execution of the operation. The SIO instruction generates signals on the 8 bussed address lines. The condition of the channel is indicated by the CC returned to the processor on 2 bussed C/SP I/O interface lines.

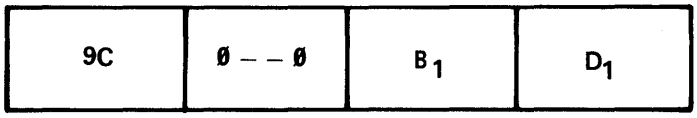
The address portion of the SIO instruction:

Channel number - depends on the configuration.
Function - either start the I/O operation or store status
Logical Control Unit (Ø-7)
Device Numbers - one of 16 devices per sub-channel (control unit) Ø/15.

$(B_1) + D_1$ OF START I/O INSTRUCTION MUX/SELECTOR



SIO INSTRUCTION



CHANNEL COMMAND WORD (CCW)

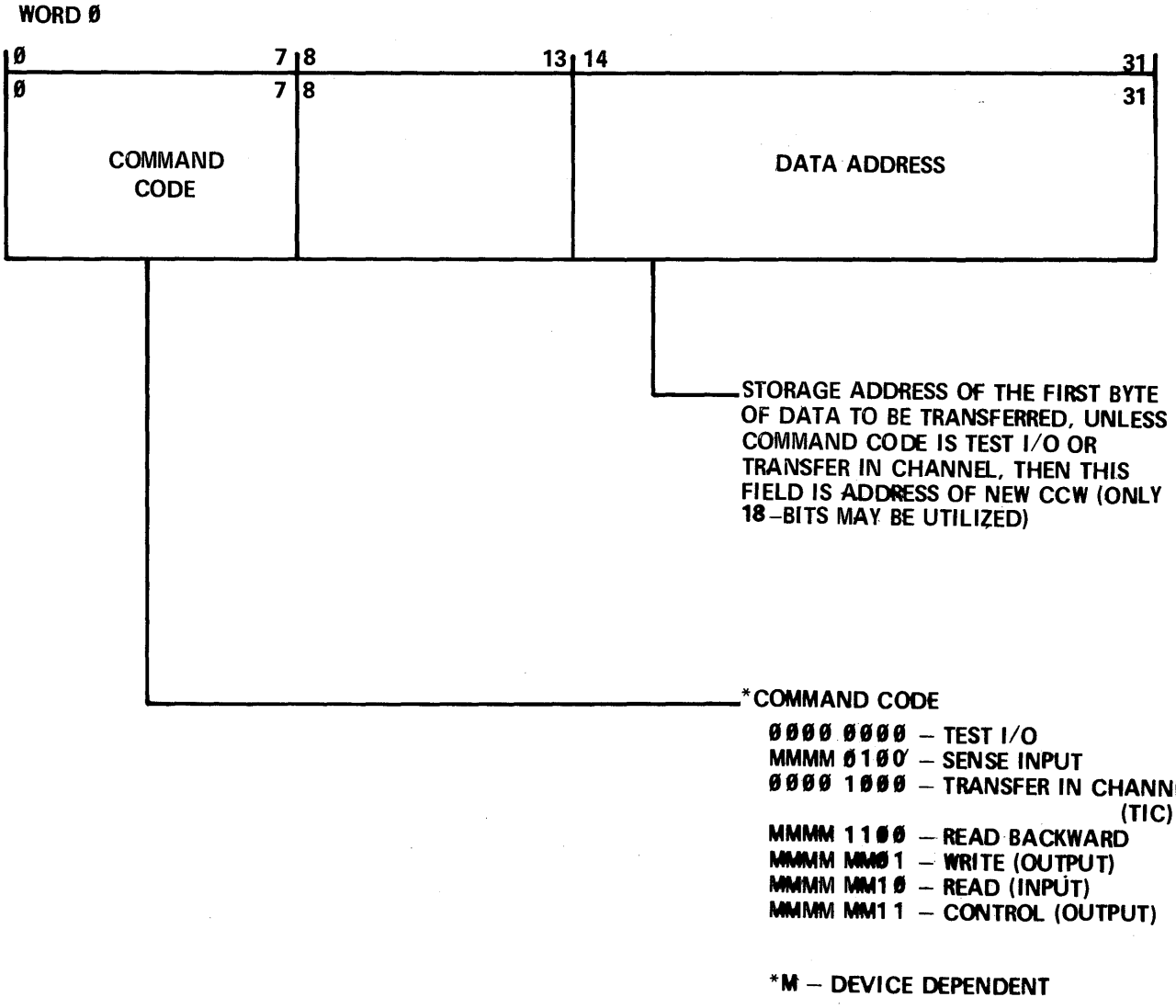
The CCW specifies the operation to be performed by the device or channel. When the specified operation is due to be executed, the CCW format is converted to that of a Hardware Channel Control Work (HCCW) and moved to internal storage location of the channel. The HCCW is modified and updated to control the operation as it progresses. There is a maximum of 8 double words (HCCW) for the multiplexer channel and 1 double word (HCCW) for the selector channel.

Bits Ø - 7: The command byte of the CCW (word Ø), specifies the operation to be performed by the device or channel. The 'M' bit positions depend on the I/O device.

Bits 14 - 31: Indicate the storage address of the first byte of data to be transferred. If the command byte indicates a Test I/O or Transfer in Channel command, then these bit positions contain a new CCW address.

> Transfer In Channel (TIC) - Provides a branching function for the channel; allowing execution of CCW's which are at non-sequential storage locations, for command and buffer loops. The CCW is ignored except for the address field which specifies the address of the next CCW. The object CCW of a TIC may not contain another TIC command.
>
> Sense - A special case of a read, in that sense bytes are read into storage instead of data. A detailed device status is presented as 'intervention required' for a printer. The number of sense bytes varies with the device.
>
> Control - A special case of a write; causing a signal to be sent to the device without any data being written, such as spacing the paper on a printer.

CHANNEL COMMAND WORD
M/S



CCW (WORD 1)

Bit 32 - CD: Indicates to chain data. Upon transfer completion, controlled by the current CCW, a new CCW is read from storage and the operation continues under control of the new CCW. The command byte is not interpreted except for a Transfer In Channel command.

Bit 33 - CC: Indicates to chain commands. Upon completion of the operation at the device (indicated by status code containing 'device end' set), a new CCW is read from storage and the operation specified by the new command code is initiated.

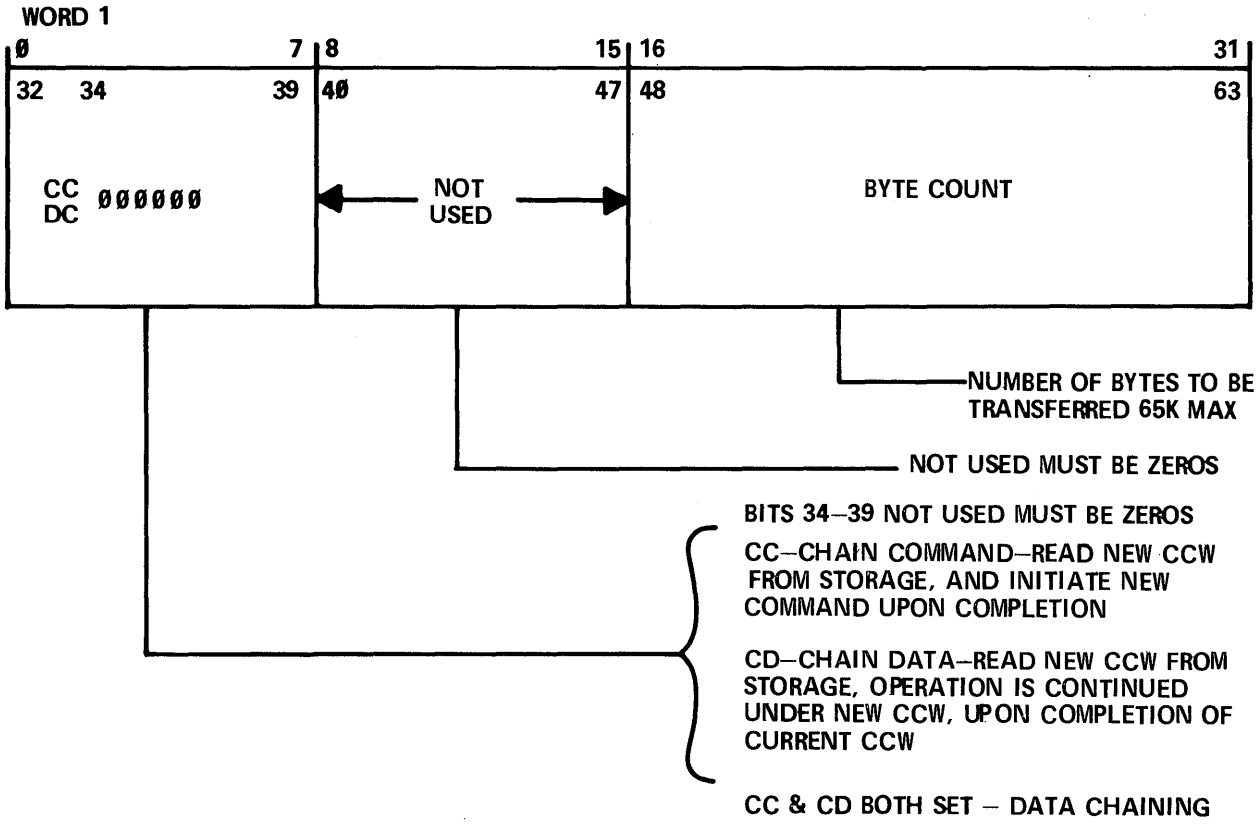
If both command and data chain bits are set, data chaining occurs.

Bits 34 - 39: Not used, must be zero.

Bits 40 - 47: Not used, must be zero.

Bits 48 - 63: Specifies the number of bytes to be transferred. Maximum count is 65K.

CHANNEL COMMAND WORD
M/S



CONDITION CODES MUX/SEL

To initiate the Test I/O command to the multiplexer or selector channels, the SIO instruction must be issued with the start device function (bit 24 of the device address set) and the command byte of the CCW containing the Test I/O command.

CONDITION CODES
MUX/SEL

SIO START FUNCTION

CC = ØØ OPERATION INITIATED

CC = Ø1 ERROR CONDITIONAL STATUS STORED IN HCCR STATUS FOR CHANNEL DEVICE AVAILABLE

CC = 1Ø BUSY CHANNEL OR SUB-CHANNEL

SIO STORE STATUS FUNCTION

CC = ØØ CHANNEL/DEVICE AVAILABLE

CC = Ø1 STATUS PENDING INFORMATION IN CSW

CC = 1Ø BUSY

CC = 11 CHANNEL NOT AVAILABLE OR STORAGE PARITY ERROR WHEN WRITING CSW

SIO TEST I/O FUNCTION

CC = ØØ AVAILABLE

CC = Ø1 STATUS INFORMATION IN HCCW

CC = 1Ø BUSY

CC = 11 CHANNEL OR DEVICE NOT AVAILABLE

CHANNEL STATUS WORD (M/S)

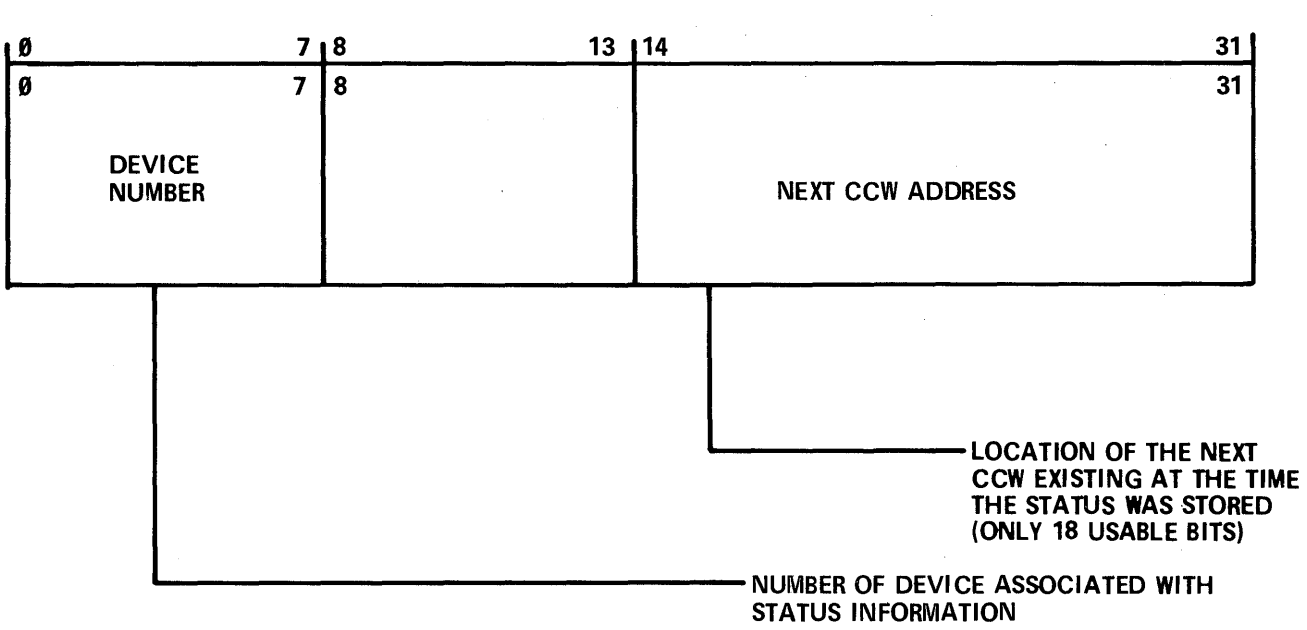
The CSW is a double word written by the channel when the sub-channel (control unit) in the status pending mode is addressed by a store sub-channel status function of the SIO. The status word is written at the double word location specified by the address provided in the CAW.

CSW (word Ø):

Bits Ø - 7: The device number associated with the status information.

Bits 14-31: The value of the next CCW address existing at the time the status information was stored.

CHANNEL STATUS WORD
M/S



CHANNEL STATUS WORD (M/S) - (continued)

Bits 32 - 39: Contain the device generated status byte.

Bit 32 - Attention: Present conditions asynchronous to I/O operations. Example: Inactive line becomes active.

Bit 33 - Status Modifier: Presented with device end. May be used to modify the channel sequence in chaining situations.

Bit 34 - Control Unit End: Set when control unit responds to interrogation with busy and status modifier set or abnormal condition detected during busy.

Bit 35 - Busy: Already executing.

Bit 36 - Channel End: End of data transfer.

Bit 37 - Device End: End of operation by an I/O device.

Bit 38 - Unit check: Program intervention is required.

Bit 39 - Unit Exception: Unusual condition, not necessarily an error has been detected.

Bits 40 - 47: Contain the sub-channel generated status byte.

Bit 40 - 41: Not used.

Bit 42 - Program Check: Programming errors detected.

Bit 43 - Protection Check: Attempt to read/write a protected area.

Bit 44 - Channel Check Data: Storage or I/O parity error occured during a data transfer.

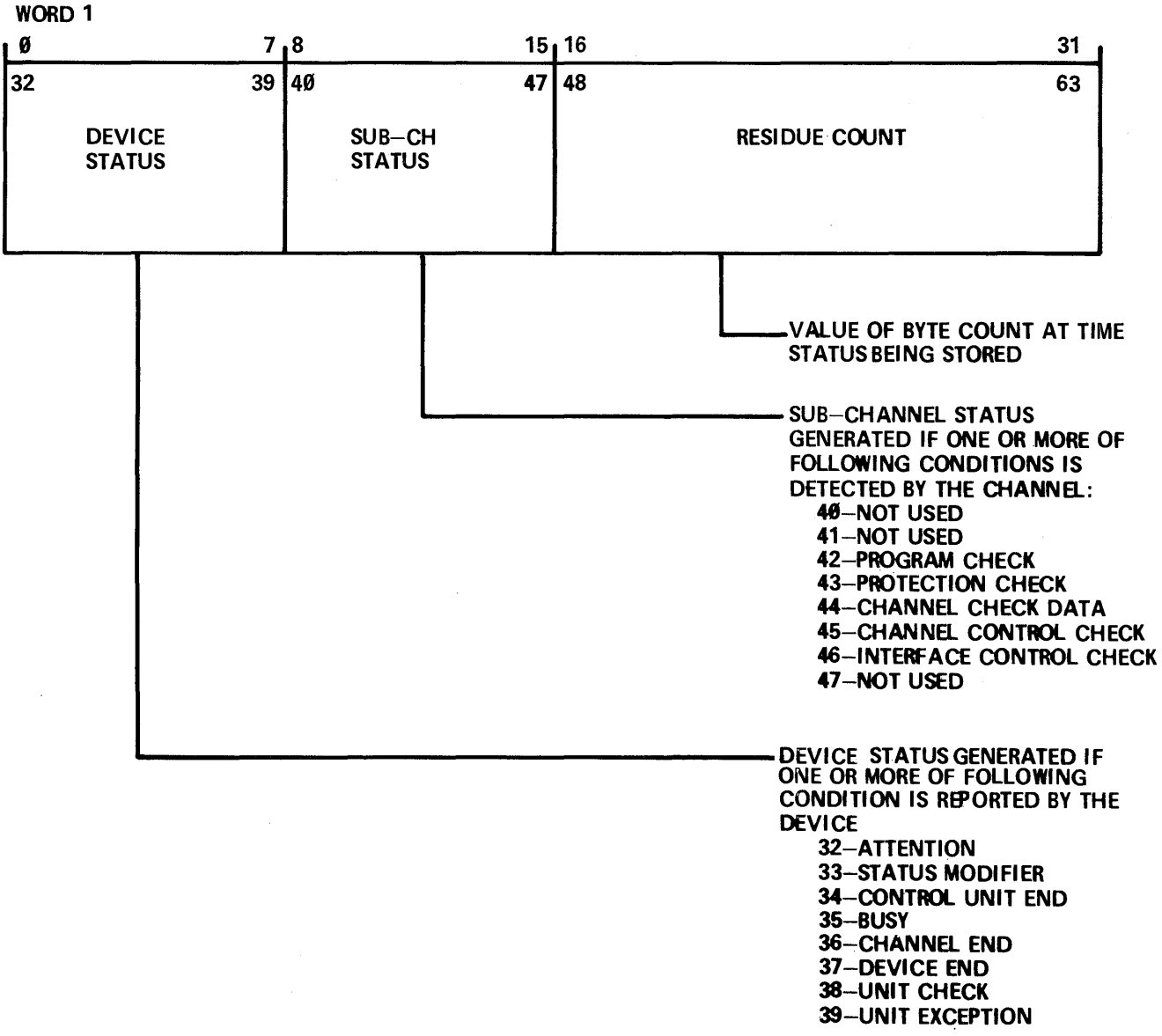
Bit 45 - Channel Control Check: Storage parity error during a control word read/write.

Bit 46 - Interface Control Check: Invalid signal sequence on the I/O bus.

Bit 47 - Not used.

Bits 48 - 63: The value of the byte count existing at the time the status information was stored.

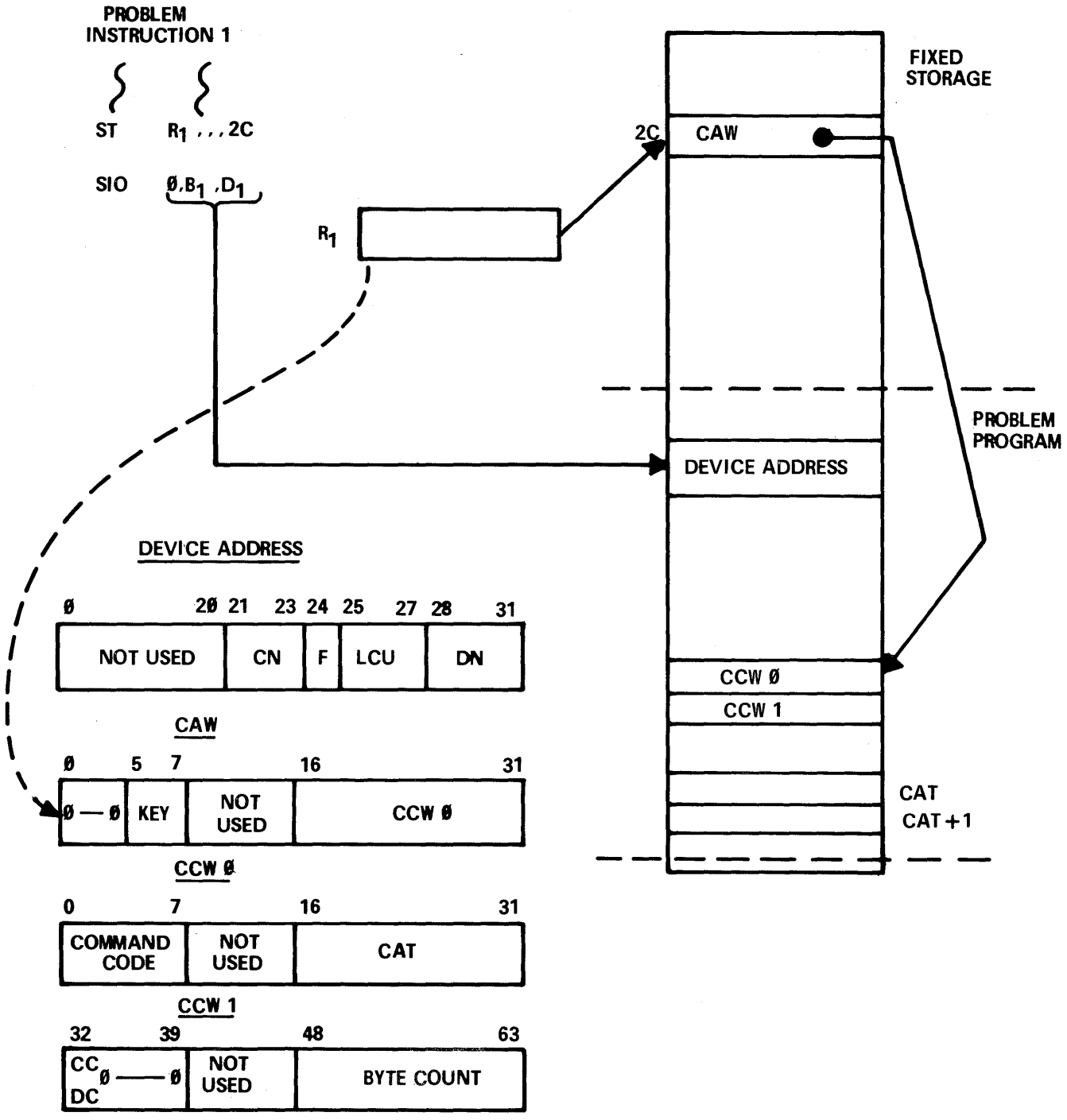
CHANNEL STATUS WORD
M/S



MUX/SEL GENERAL I/O FLOW

The program sets up the CAW and CCW's. The CAW is stored in fixed memory at address $2C_{16}$. The contents of B_1 and the value of D_1 form the device address. SIO is issued with the device address and assuming the channel and device is not busy, the CAW is read from fixed memory. The MUX/SEL channel stores the CAW in its' hardware and reads out the CCW's into its' hardware (now HCCW), the address of which is in the CAW. The channel interprets the command code and the execution begins, such as the transfer of data.

MUX/SEL GENERAL I/O FLOW

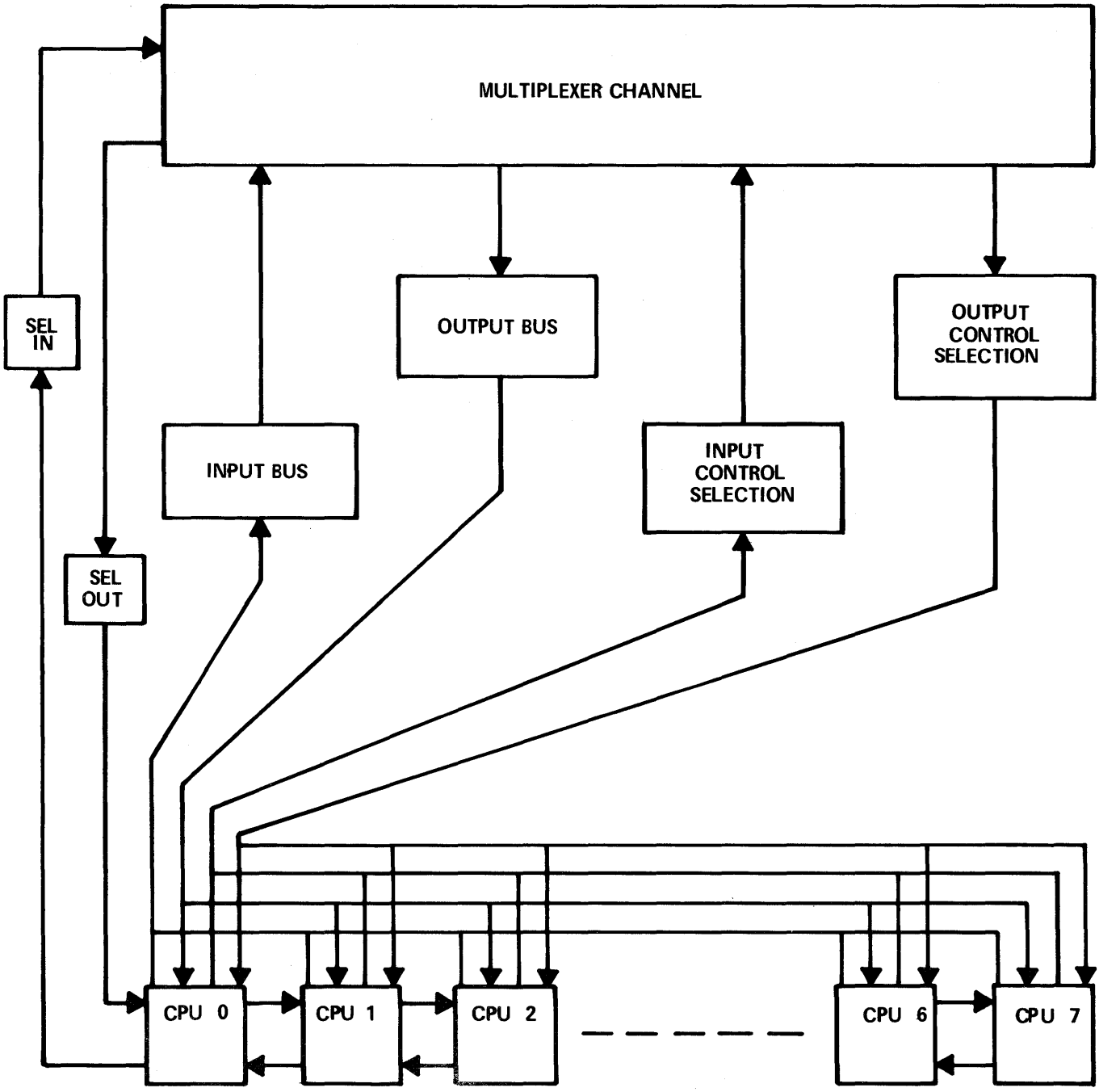


MULTIPLEXER/SELECTOR CHANNEL

The Input bus and Output bus contain the actual data to be transferred. They each consist of 8 data lines and 1 parity line. The data signals are sent in parallel. The input data, device numbers, and status information are transmitted to the channel via the input bus. The channel transmits output data, I/O commands, and device selection to the control units via the output bus.

The Input and Output control sections contain a combined total of seven selector lines (4 for the output section and 3 for the input section) and six tag lines (3 for the output section and 3 for the input section). The signals are sent in parallel, with the exception of the Select Out and the Select In, which are sent in serial.

MULTIPLEXER/SELECTOR CHANNEL



MULTIPLEXER/SELECTOR CONTROL LINES

Output Control Section Selection Lines:

1. Operational Out (OPL OUT) - indicates the channel is active and when the command is dropped a reset condition is indicated. No output control lines are enabled unless OPL OUT is active.
2. SELECT OUT (SEL OUT) - sent to the first logical control unit and continues on to the next until a control unit connects to the channel. At the last physical control unit the SEL OUT becomes a SELECT IN (SEL IN) and returns to the channel through the control units. SEL OUT and SEL IN perform the same function, therefore, the control unit may use either one for selection control, but not both.
3. HOLD OUT (HLD OUT) - sent in parallel to the control units at the same time as SEL OUT is sent serially. SEL OUT is valid only with HLD OUT.
4. SUPPRESS OUT (SUP OUT) - indicates special conditions including command chaining and status suppression.

Output Control Section Tag Lines: carry interlocked responses to the input tag line signals. In most cases, they specify information on the output bus.

1. ADDRESS OUT (ADR OUT) - used during a channel-initiated selection sequence to indicate a device number is available on the output bus.
2. SERVICE OUT (SRV OUT) - a positive response to service in (SRV IN) or STATUS IN (STA IN) indicating the channel has accepted the input data or status, or indicates on output that data is available on the output bus.
3. COMMAND OUT (CMD OUT) - has several applications.
   a. In response to ADR IN indicates a command is available on the output bus and proceed during a control-unit-initiated sequence.
   b. In response to SRV IN causes the control unit to terminate and eventually to initiate an interrupt sequence.
   c. Is a negative response to STA IN indicating the channel cannot accept the status byte at this time.

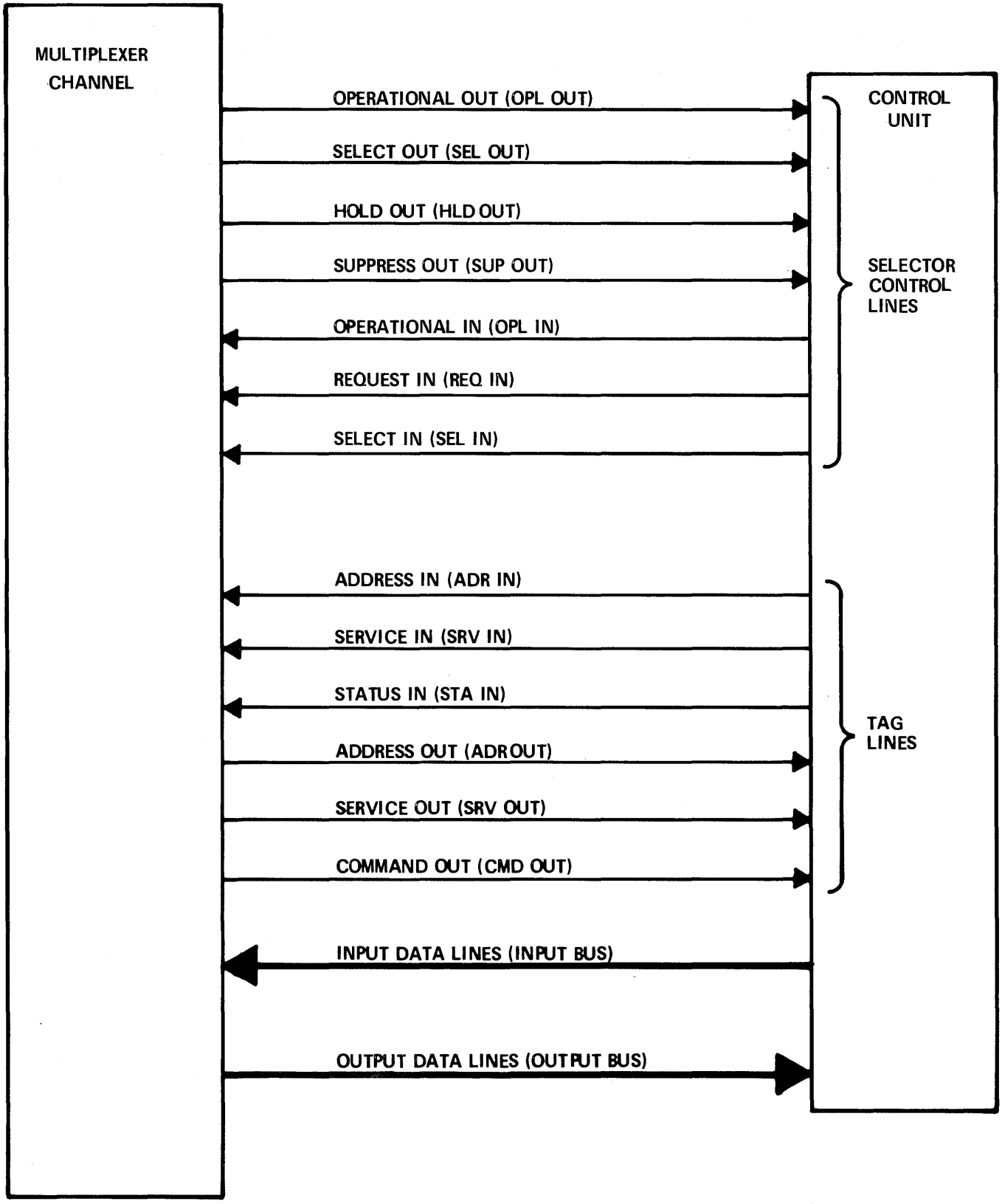
Input Control Section Selection Lines:

1. SELECT IN (SEL IN) - provides the return path for the SEL OUT and if seen at the channel indicates no control unit responded to the SEL OUT.
2. REQUEST IN (REQ IN) - indicates one or more of the control units require service.
3. OPERATIONAL IN (OPL IN) - indicates to the channel that a control unit is connected.

Input Control Section Tag Lines: Carry interlocked responses in conjunction with the output tag lines. In all cases, they specify information is available on the input bus.

1. ADDRESS IN (ADR IN) - The control unit activates an ADR IN indicating the device number has been placed on the input bus.
2. SERVICE IN (SRV IN) - indicates the control unit is ready to receive or transmit a byte of data.
3. STATUS IN (STA IN) - indicates that status information is available on the input bus.

MULTIPLEXER/SELECTOR CONTROL LINES



MULTIPLEXER/SELECTOR
INITIALIZE DEVICE

1. C/SP issues SIO
2-3. MUX/SEL asks for CAW, receives CAW, asks for and receives CCW.
4.* MUX/SEL sends condition code to C/SP.

Initialization of Device

5-6. MUX/SEL places the device address on the output bus and raises the Address out signal. All control units compare the address.
7. The Select Out and Hold Out signals are raised, by MUX/SEL.
8. Operational IN is raised, by control unit. Device now selected.
9-10. The device address is placed on the Input bus by the CU, Address In is raised, SEL/HLD OUT, Address Out are dropped.
11. The command is put on the Output bus and Command Out signal is raised by channel, Address In is dropped.
12. The command is interpreted, Command Out is dropped and status placed on Input bus, STATUS IN is raised by control unit. (STATUS is all zeros)
13. Service Out is raised by channel, then Operational In is dropped, Status In, and Service Out is dropped.
14. Control Unit raises Service In, indicating ready to receive byte of data.

Data Transfer begins

15-16 MUX/SEL requests and receives byte of data from C/SP.
17-18 MUX/SEL places data on the output bus and raises Service Out signal. Service In is dropped.
19. Control Unit raises SRV IN (ready for another data byte). SRV OUT is dropped.

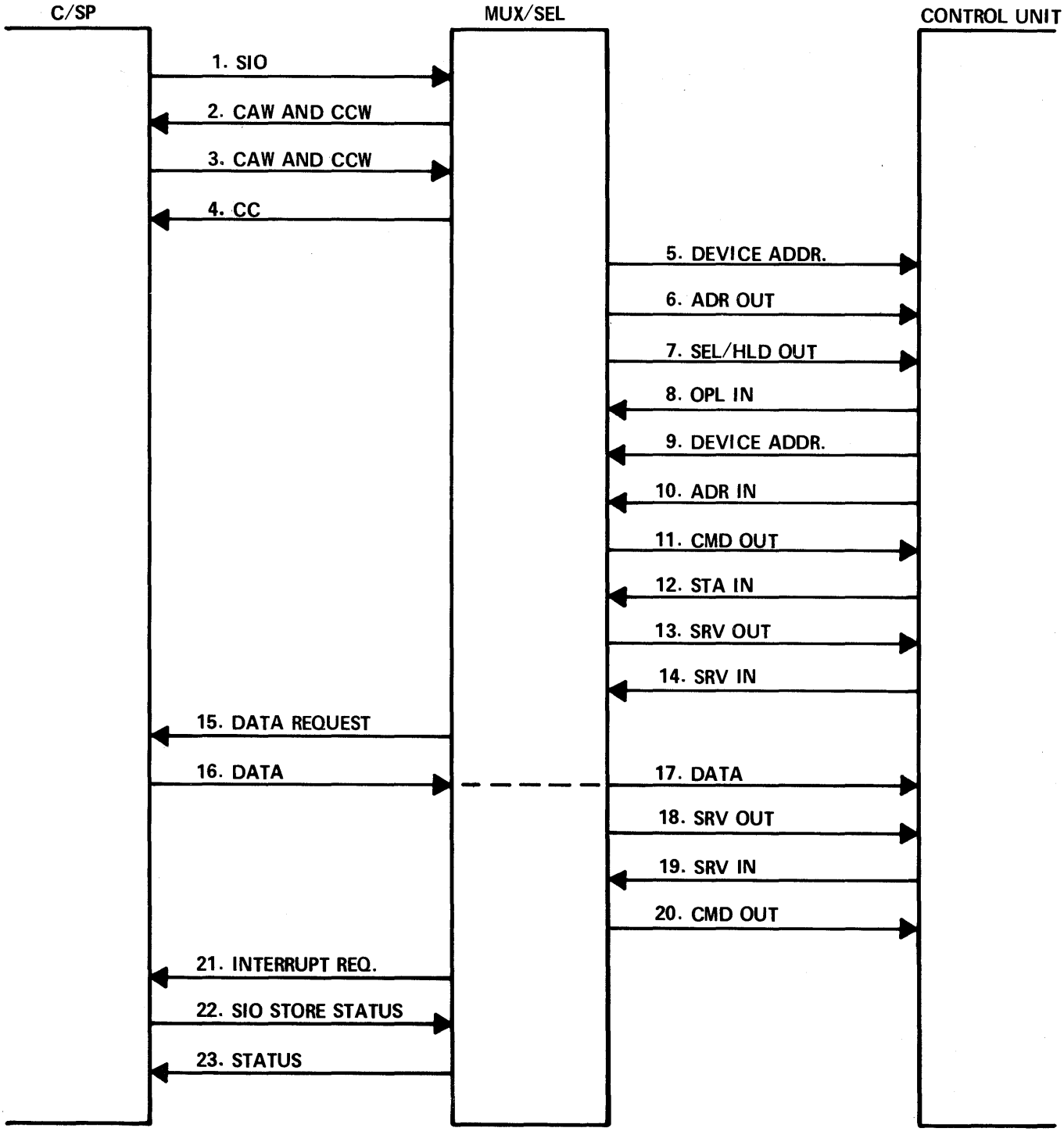
Termination

20. MUX/SEL raises a Command Out indicating the control unit to terminate. SRV IN is dropped.
21. Channel generates an Interrupt request to C/SP.
22. C/SP accepts, issues SIO to store the sub-channel status.
23. C/SP receives status, Terminates.

*The condition code returned to the C/SP does not necessarily return at this point. It varies as the channel may be busy, then the CC is returned immediately and no CAW is fetched.

This overhead is designed to show the amount of signals transmitted between the C/SP channel, and control units. It should not be interpreted as the absolute procedure.

MULTIPLEXER/SELECTOR INITIALIZE DEVICE



SECTION IV

ADAPTER CHANNEL

SECTION IV INDEX – INTERCOMPUTER ADAPTER CHANNEL

$(B_1) + D_1$ OF START I/O INSTRUCTION

The Intercomputer Adapter (ICA) provides the means of communication between the C/SP and 1100 computer.

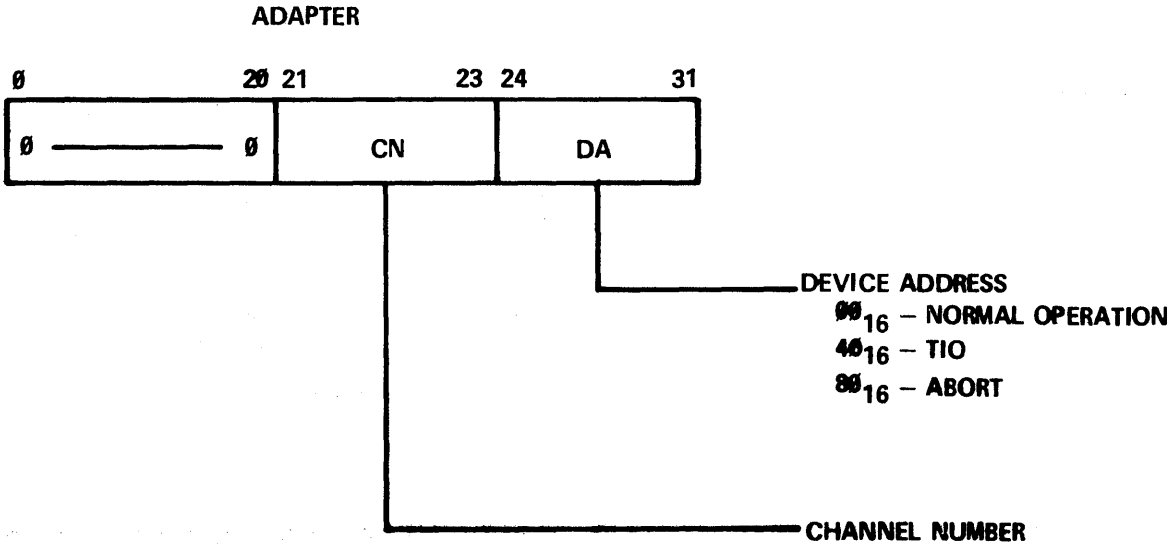
Data transfer operations take place only when the adapter channel has accepted matching commands from both C/SP and the Host computer, i.e., the command byte issued by the C/SP via the CCW and the external function (EF) issued by the host both indicate data transfers and in the same direction.

The C/SP indicates a data transfer by issuing a SIO instruction to the adapter channel. When recognized by the adapter channel, the adapter issues data request to the C/SP to get the CAW and then the CCW. The command byte is decoded and appropriate action is taken. If the command is input or output to/from the host, the adapter checks for the matching EF and command byte code. If no match, an External Interrupt (EI) is sent to host, thus any EF issued by the host is considered non-matching (before acknowledgement of the EI). If matching, the data transfer takes place.

The channel number varies according to system configuration.

The device address contains the function to be performed: $\emptyset\emptyset_{16}$ - normal data transfer; $4\emptyset_{16}$ - Test I/O to determine the condition of the ICA; $8\emptyset_{16}$ - Abort, immediately terminates no matter what operation is in progress. This command causes no interrupt to the Host processor.

$(B_1) + D_1$ OF START I/O INSTRUCTION
ADAPTER



CONDITION CODES ADAPTER

The adapter returns condition codes to the C/SP, depending on the function indicated by the device address of the SIO instruction.

SIO $\emptyset\emptyset_{16}$ (START)
CC = 1Ø Busy indicates transfer operation is in progress

SIO $4\emptyset_{16}$ (Test I/O)
The CAW is not fetched for this function.
CC = Ø1 Holding pending status - the status byte is stored in the status halfword in fixed memory. The condition code is returned to the C/SP, and the channel clears itself for the next operation.

SIO $8\emptyset_{16}$(ABORT) Aborts immediately no matter what operation is in progress. Abort is accepted or the channel may be off-line.

CONDITION CODES ADAPTER

SIO START

CC = ØØ	INSTRUCTION ACCEPTED
CC = Ø1	PARITY ERROR ON CAW OR CCW FETCH
CC = 1Ø	BUSY
CC = 11	CHANNEL OFF–LINE

SIO 4Ø TEST I/O

CC = ØØ	AVAILABLE FOR START I/O
CC = Ø1	HOLDING PENDING STATUS
CC = 1Ø	BUSY
CC = 11	CHANNEL OFF–LINE

SIO 8Ø ABORT

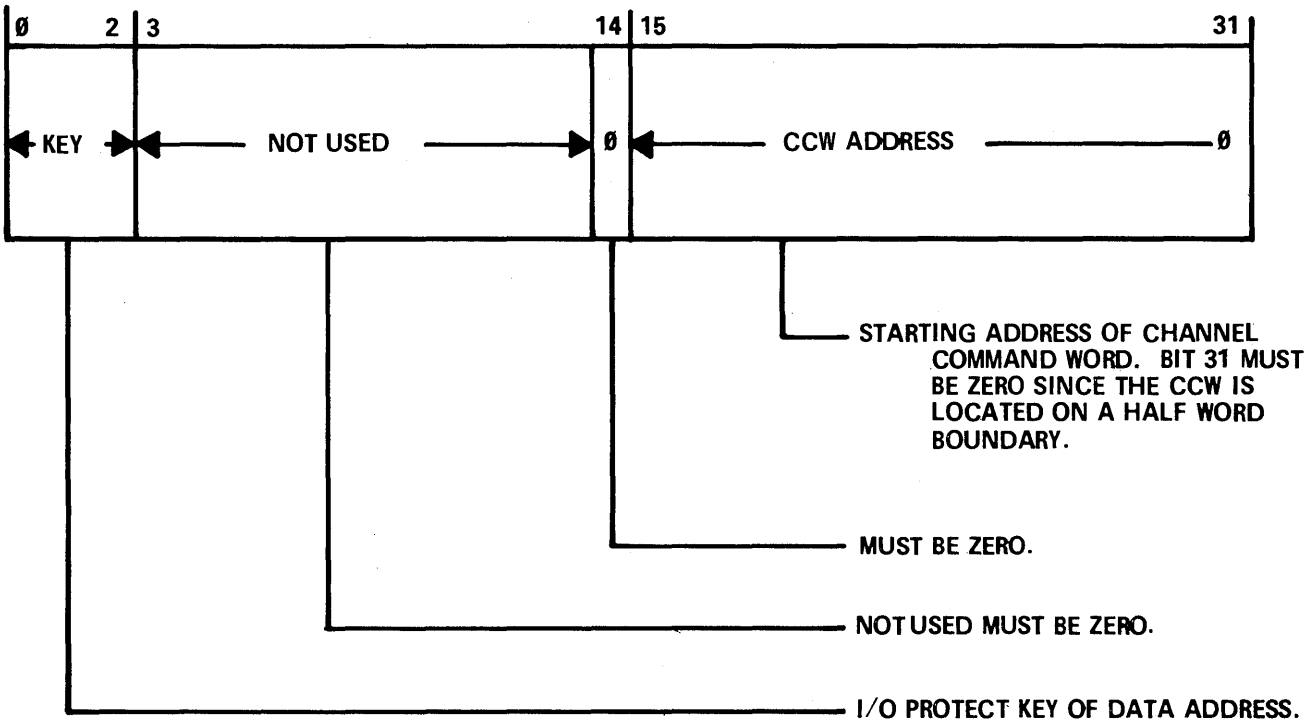
CC = ØØ	ACCEPTED
CC= Ø1	CHANNEL OFF–LINE

CHANNEL ADDRESS WORD (ICA)

During the SIO time (i.e., the time the channel interprets the function and returns the condition code to the C/SP) the ICA fetches the CAW, assuming the channel is not busy or off-line.

Bits Ø - 2: The I/O protect key of the data address of the CCW.
Bits 15 - 31: The address of Channel Command Word (CCW).

CHANNEL ADDRESS WORD
ICA



CHANNEL COMMAND WORD (CCW)

The CCW is a double word or 64 bits which contain the details of the I/O operation to be performed.

Bits Ø - 7 of CCW word zero is the command byte.

Command Byte:

'Set Host off-line' - indicates all data commands from the C/SP are executed in the test mode.

'Reset off-line condition' - indicates to the ICA to put the Host on-line again and also reset bit 6 of sense byte Ø.

'Transmit sense bytes' - All or none of the sense bytes are to be transmitted to C/SP as specified by the byte count in CCW 1. (Sense bytes are used to indicate command information, present data address, condition of ICA to C/SP and Host processor).

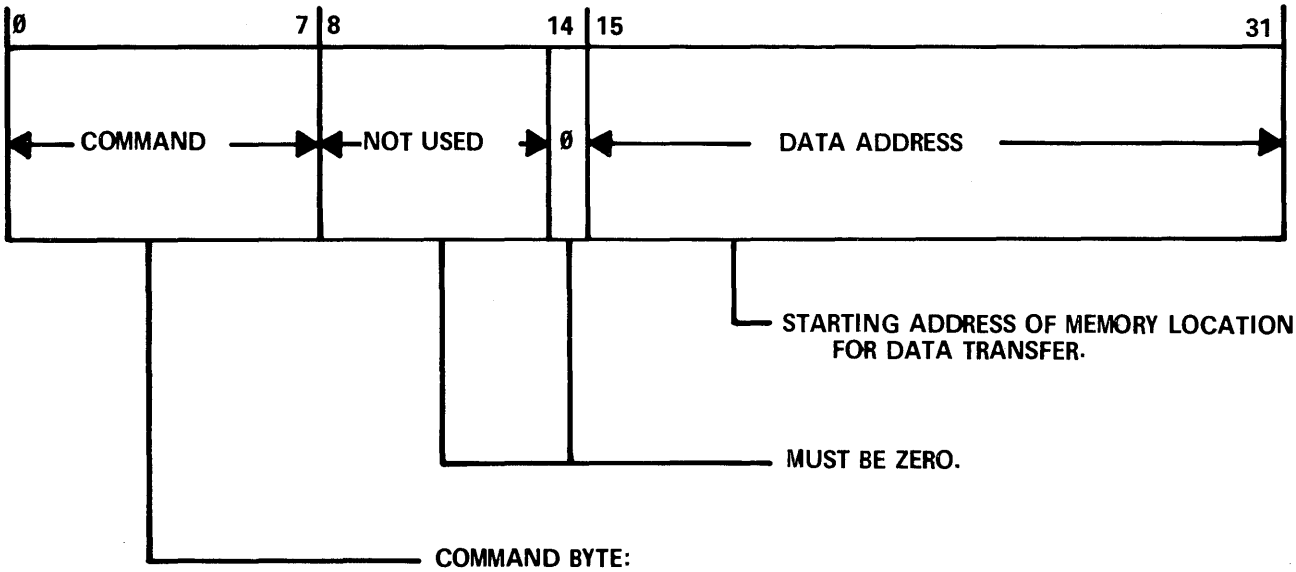
'Input - Output formats' - indicate the format of the data to be transferred and the direction of the transfer.

'Send External Interrupt to Host' - used to present status to Host processor. This is a control command, so no data transfer takes place.

Bits 15 - 31: The starting address for the data transfer.

CHANNEL COMMAND WORD
ICA

CCW WORD Ø



COMMAND BYTE:

XXX10000 SET MP OFF LINE, ADAPTER CHANNEL WILL IGNORE ANY COMMANDS FROM MP. TEST MODE – SENSE BYTE (BIT 6) SET.

XXX00000 RESET OFFLINE CONDITION.

XXXXX100 TRANSMIT SENSE BYTES, COUNT IN BYTE COUNT FIELD. (SEE SENSE BYTES IN NEXT FOIL)

DDYYYY01 INPUT FROM C/SP TO HOST PROCESSOR:

DD BITS	FORMAT
00	A
01	B
1X	C

DDYYYY10 OUTPUT FROM HOST PROCESSOR TO C/SP:

DD BITS	FORMAT
00	A
01	B
1X	C

YYYYYY11 SEND EXTERNAL INTERRUPT TO HOST.

X – NOT INTERPRETED BY ADAPTER CHANNEL.

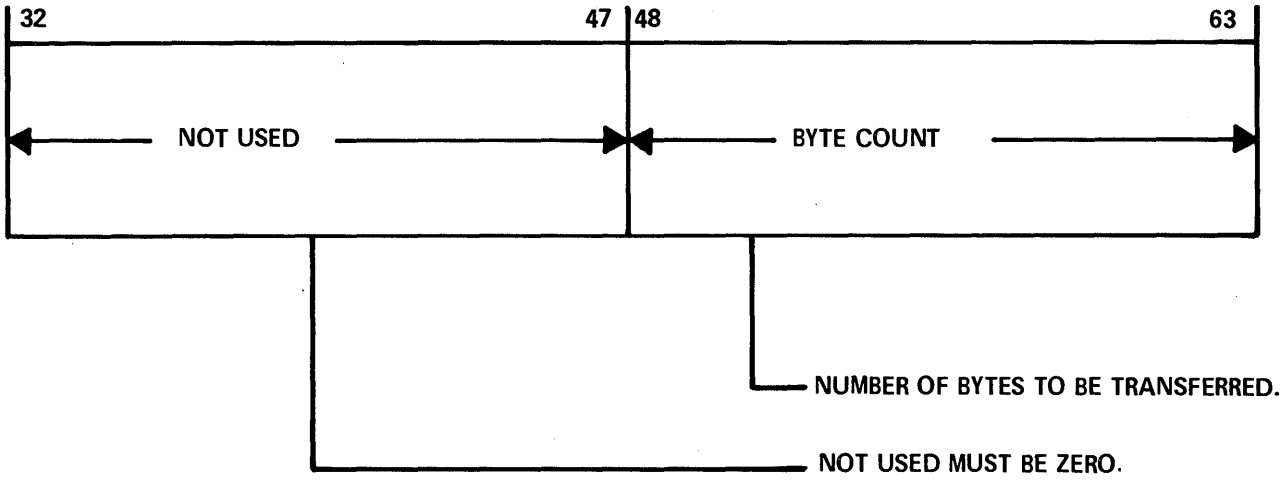
Y – INTERPRETED IN TEST MODE ONLY.

CCW WORD 1

Bits 48 - 63: The number of bytes to be transferred. May be the number of sense bytes to be transmitted in conjunction with the sense command issued in CCW Ø. Bits 32 - 47 are not used.

CHANNEL COMMAND WORD
ICA

CCW WORD 1



SENSE BYTES

BYTE Ø	INDICATES CONDITION OF ADAPTER CHANNEL TO THE C/SP.
BYTE 1 & 2	CONTAINS COMMAND INFORMATION FROM HOST PROCESSOR TO C/SP.
BYTE 3	CONTAINS INFORMATION ON ADAPTER CHANNEL FOR HOST PROCESSOR.
BYTE 4 & 5	USED IN TRANSFERRING THE HIGH ORDER 16 BITS OF PRESENT DATA ADDRESS.

ADAPTER SENSE BYTES 0, 1, 2

The C/SP may request none, 1, 2, 3, 4, 5, or 6 sense bytes as specified by the count in the CCW associated with the Sense Command.

Sense Byte Ø - is used to indicate the condition of the ICA channel to the C/SP.

Bit Ø - Invalid Command: Is set if the command byte from the C/SP cannot be decoded into a meaningful operation.

Bit 1 - not used.

Bit 2 - Parity Error: Set if parity error occurs on a transfer of data from C/SP to ICA.

Bit 3 - Invalid Address: Set if an invalid address is detected during data transfers.

Bit 4 - Storage Protection Error: Set if a storage protection error is determined during a data transfer.

Bit 5 - not used.

Bit 6 - Host Off-Line: Set when a 'Set Host Off-Line' command is received from the C/SP.

Bit 7 - not used.

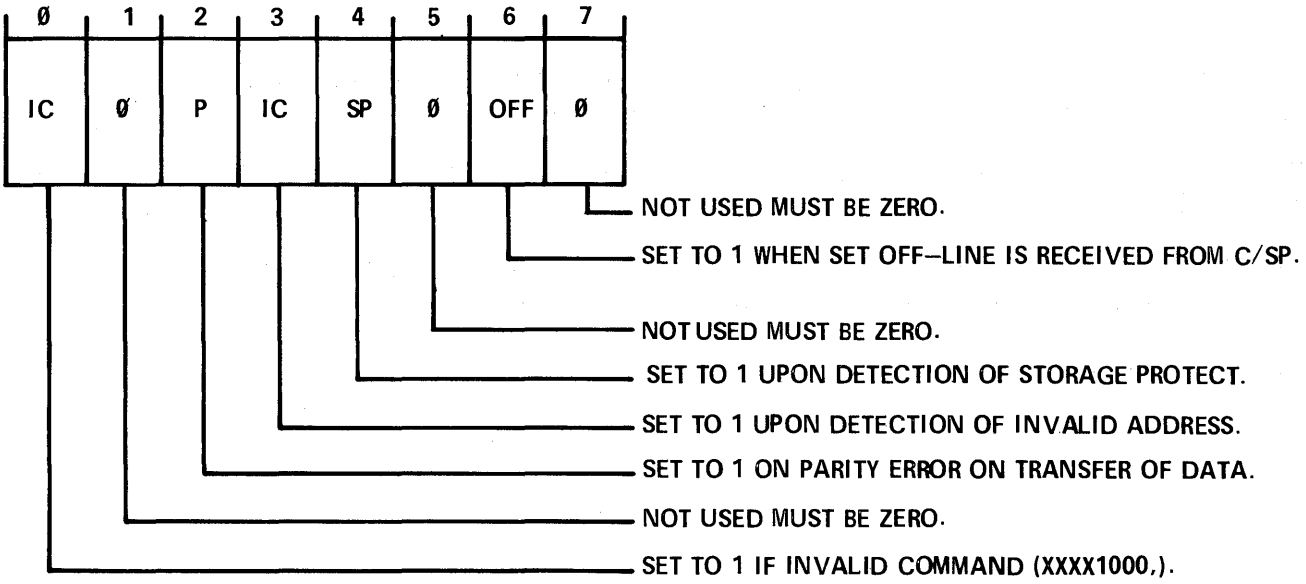
Sense Bytes 1 and 2 are used to transfer command information from the Host to C/SP.

Sense Byte 1 is bits 15 - 8 of the last External Function (EF) received by the ICA from the Host. This would be the word or character count on output from the Host.

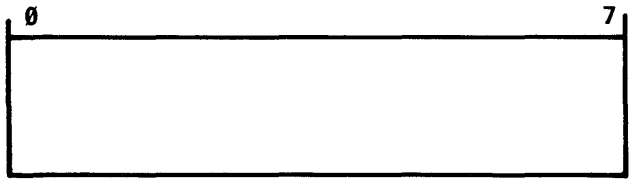
Sense Byte 2 is bits 7 - Ø of the last External Function (EF) received by the ICA from the Host. This is the C/SP protect Key, format of the data to be transferred and the direction of transfer.

SENSE BYTES 0,1,2
ICA

SENSE BYTE Ø

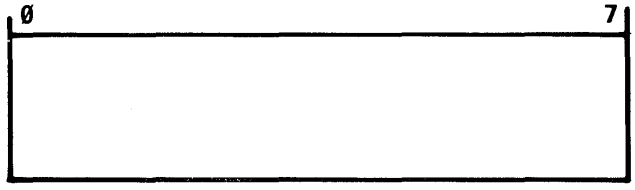


SENSE BYTE 1



FILLED BY BITS 15–8 OF LAST EF
RECEIVED BY ADAPTER CHANNEL.

SENSE BYTE 2



FILLED BY BITS 7–Ø OF LAST EF RECEIVED
BY ADAPTER CHANNEL.

ADAPTER SENSE BYTES 3,4, 5

Sense Byte 3 - used to transfer information concerning the operation of the ICA to the Host.

Bit Ø - not used

Bit 1 - Host Termination:

Set when any External Function (EF) is received by the ICA from the Host during a data transfer. The Unit Exception bit (Bit 7) of the Status Byte is simultaneously set. This bit (Bit 1) is reset to zero when Sense Byte 3 is sent to the C/SP.

Bit 2 - Inhibit Host Normal Termination Interrupt:

Set if Bit 16 (Termination Interrupt) of the last EF was set. This inhibits the ICA from sending the normal termination interrupt to Host.

Bit 3 - C/SP Data Transfer Error:

Set when the data transfer is terminated due to a storage protection, invalid address, or parity error in the transfer from the C/SP to ICA. Corresponding bits in Sense Byte Ø are also set.

Bit 4 - Indicates Format C.

Bit 5 - Indicates Format B.

Bit 6 - Indicates Output from Host.

Bit 7 - Indicates Input to Host.

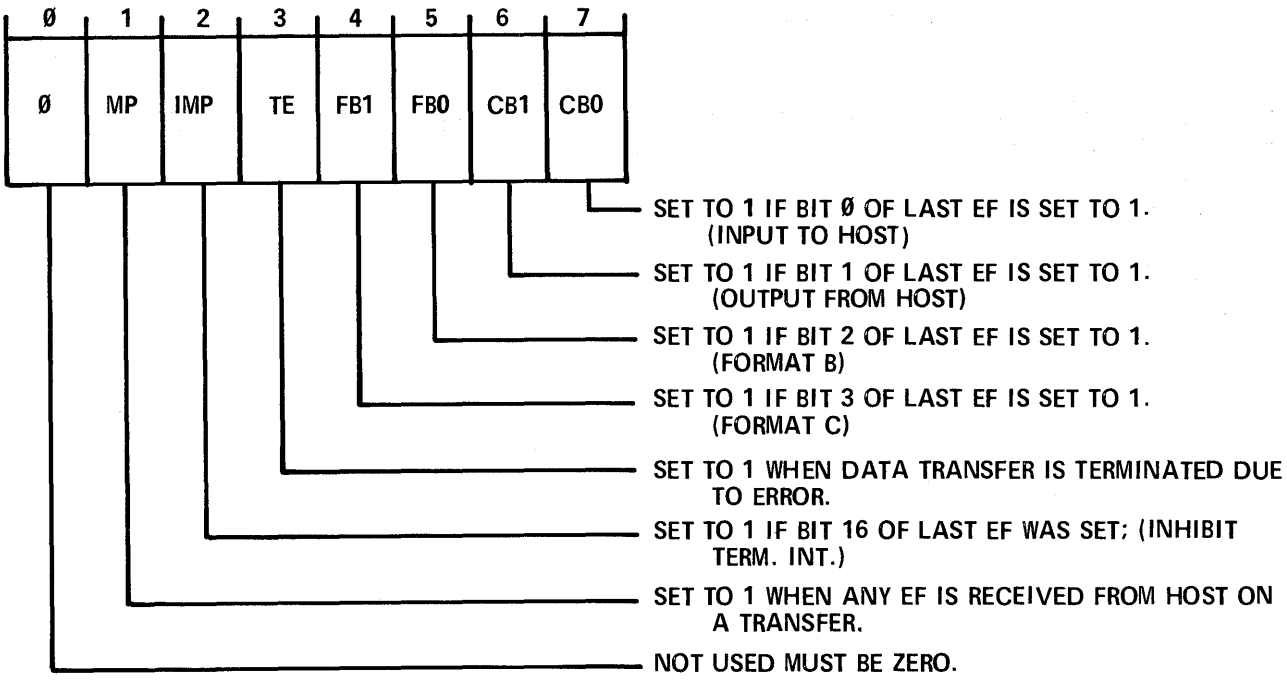
Sense Bytes 4 and 5 - used to transfer the high order 16 Bits of the present data address in the CCW.

Sense Byte 4 is bits 1 - 8 of the next data address that would have been accessed had the transfer not been terminated.

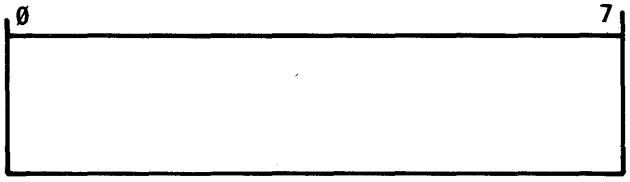
Sense Byte 5 is bits 9 - 16 of the next data address that would have been accessed had the transfer not been terminated.

SENSE BYTES 3,4,5
ICA

SENSE BYTE 3

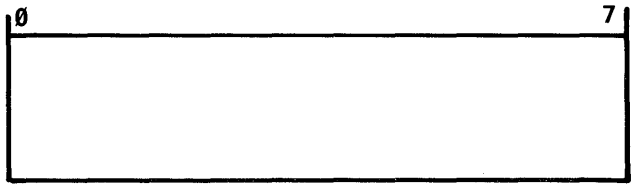


SENSE BYTE 4



FILLED BY BITS 1–8 OF NEXT DATA ADDRESS THAT WOULD HAVE BEEN ACCESSED HAD TRANSFER NOT BEEN TERMINATED.

SENSE BYTE 5



FILLED BY BITS 9–16 OF NEXT DATA ADDRESS THAT WOULD HAVE BEEN ACCESSED HAD TRANSFER NOT BEEN TERMINATED.

ADAPTER EXTERNAL FUNCTION WORD SENT BY THE HOST

The External Function (EF) is transferred from the Host to the ICA to provide data format and transfer direction information for the ICA and other information for the C/SP via sense bytes 1 and 2.

Bit 17 - not used.

Bit 16 - Termination Interrupt: When set, inhibits the normal termination interrupt to the Host and also sets Bit 2 of sense byte 3.

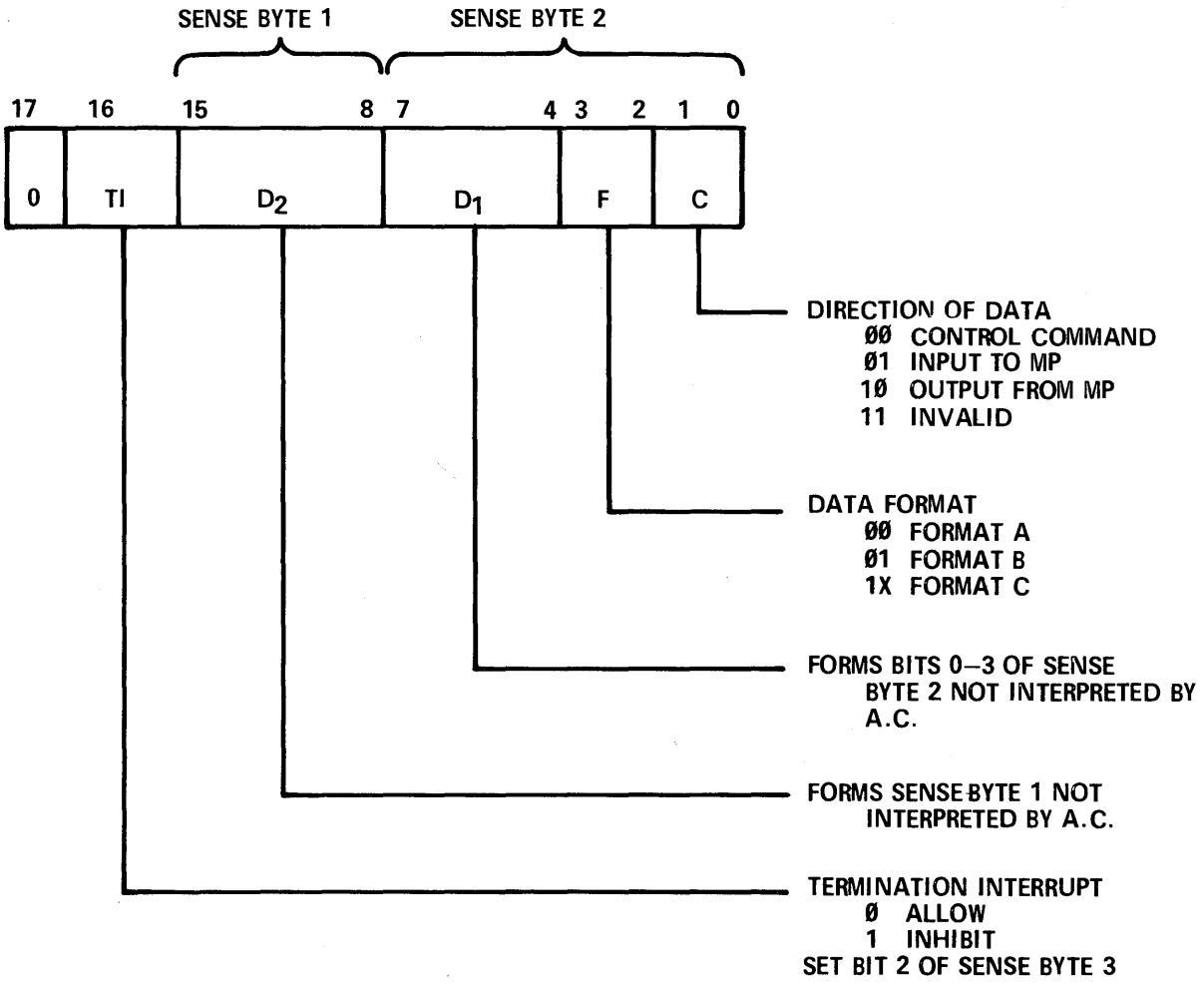
Bit 15 - 18: Forms Sense Byte 1 and are not interpreted by the ICA.

Bit 7 - 4: Forms bits Ø - 3 of Sense Byte 2 and are not interpreted by the ICA.

Bit 3 and 2: Informs the ICA and C/SP of the data format of the data to be transferred.

Bit 1 and Ø: Informs the ICA and C/SP of the direction of the data transfer.

EF SENT BY HOST
ICA

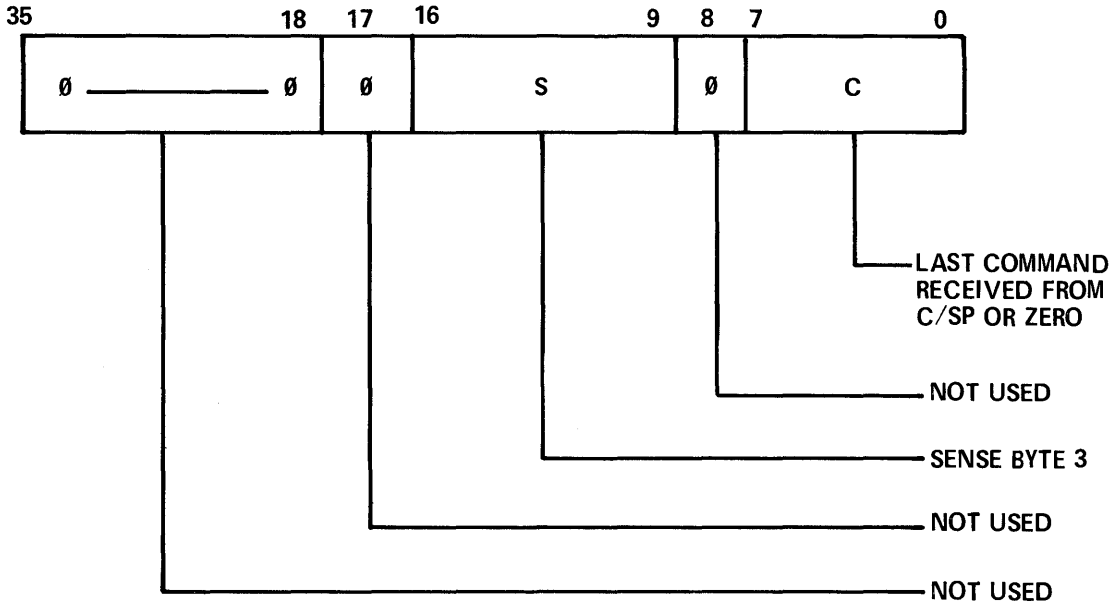


ADAPTER HOST EXTERNAL INTERRUPT WORD

The External Interrupt Word is used to inform the Host of the present condition of the adapter channel and is presented as part of the External Interrupt.

During the ending interrupt sequence to the Host, Field 'C' is set to zero.

HOST EXTERNAL INTERRUPT WORD

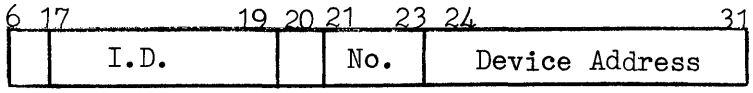


THE S AND C PORTIONS OF THIS WORD WILL BE ZEROED DURING THE ENDING OF THE INTERRUPT SEQUENCE.

Adapter Status Halfword and Interrupt Code Halfword

When an interrupt request is accepted by the C/SP, a status halfword and interrupt code halfword are stored in fixed memory of the C/SP. Only one byte of the status halfword is used and is referred to as the status byte. The interrupt code halfword indicates the ICA channel identification code, channel number, and device address (ICA - device address is zero).

Interrupt code halfword:



Status halfword (byte) - Used to inform the C/SP of significant conditions during the ICA operation.

Bit Ø - Attention bit: Set when a command has been received from the Host. This bit will remain set until the C/SP responds with a sense command. The ICA will not accept a data transfer command until it receives the sense command.

Bits 1 - 3: Are not used and are always zero.

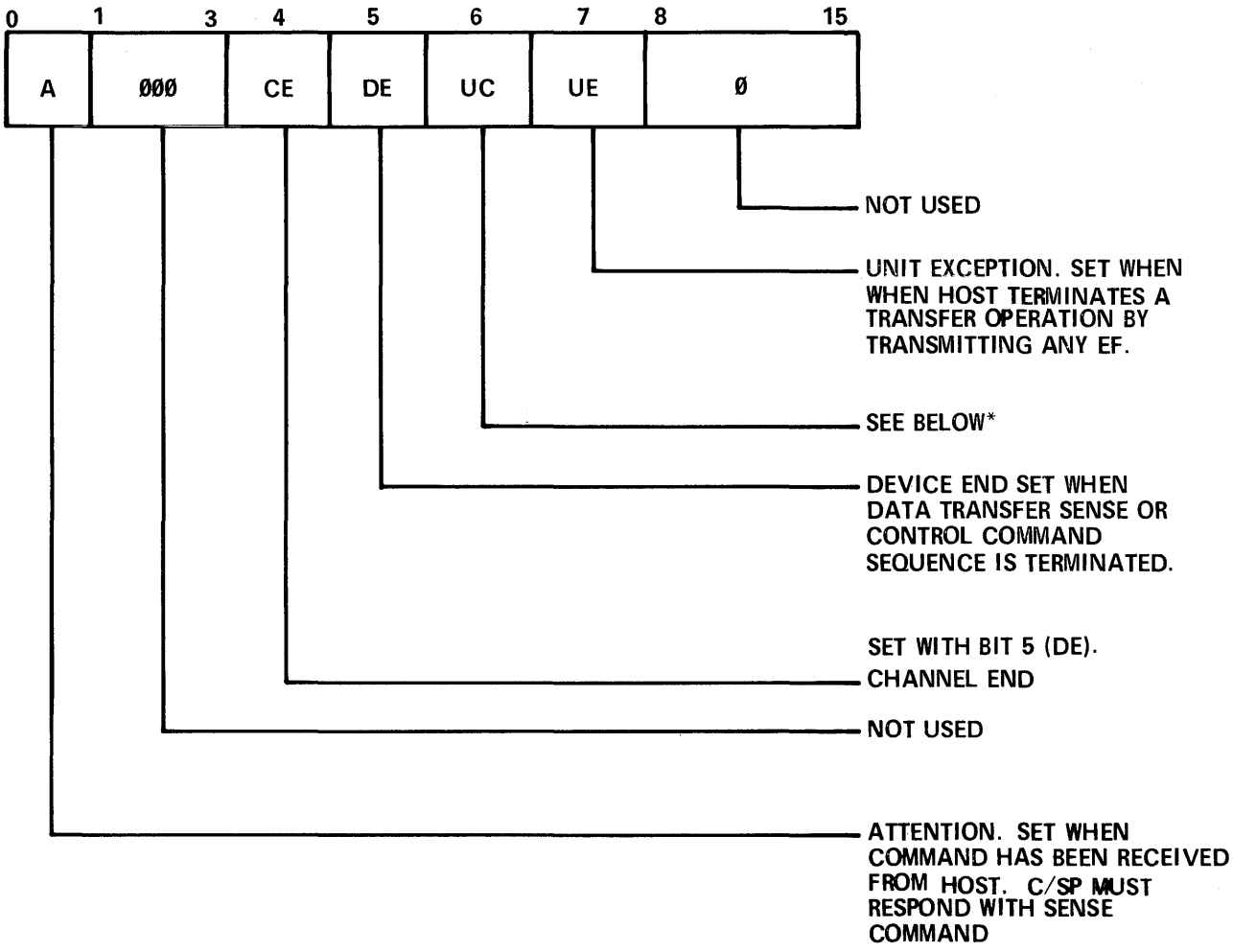
Bit 4 - Channel End: Set when the device and channel are terminated. Bit 5 device end is also set.

Bit 5 - Device End: Set when a data transfer, or control command sequence is terminated.

Bit 6 - Unit Check: Set when any of these errors are sensed during a data transfer; Invalid command, Parity error, Invalid address error, Storage protect error.

Bit 7 - Unit Exception: Set when the Host terminated a data transfer operation by transmitting any External Function.

STATUS HALF WORD
ADAPTER CHANNEL



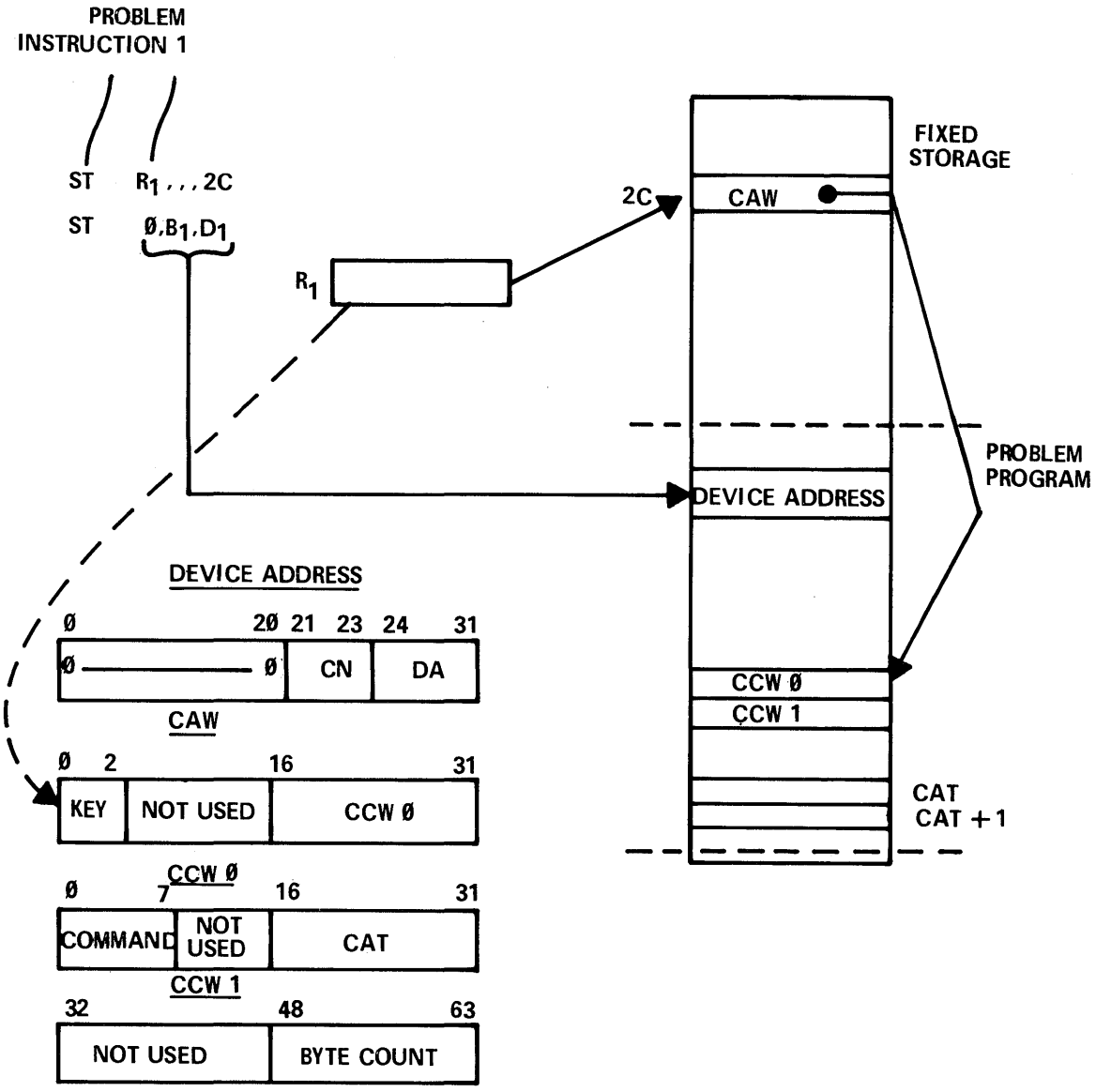
* UNIT CHECK SET WHEN: These errors are sensed during data transfers.

a. INVALID COMMAND (8_{16})
b. PARITY ERROR
c. INVALID ADDRESS ERROR
d. STORAGE PROTECT ERROR

ICA GENERAL FLOW

The program sets up the CAW and CCW's. The SIO instruction is issued to the ICA with the contents of B_1 added to the value of D_1 actually forming the device address consisting of the channel number, function (start I/O, Test I/O) and the device address of the device to be activated. (In the case of the ICA, the device is Ø.) The ICA reads the CAW from storage, gets the address for the CCW and reads the CCW out of storage. The command byte is interpreted and if a match exists with the EF (from the Host) the data transfer is initiated.

ICA GENERAL I/O FLOW



INTER-COMPUTER ADAPTER (ICA)

Whenever an interrupt request is sent to and accepted by the C/SP, a status halfword and interrupt code halfword are stored in C/SP fixed memory. If the status halfword has bit Ø set, the C/SP must respond with a sense command (to determine if input or output has been requested by the Host). If Bit Ø is not set, C/SP does not send sense command (checks other bits - as termination).

C/SP initiates data transfer.

1. C/SP initiates data transfer by issuing SIO instruction.

2. ICA accepts the SIO (indicated to C/SP via CC in PSW). The ICA, at the same time it recognizes the SIO, generates a data request to C/SP for the CAW.

3-4. ICA gets the CAW and generates a data request to C/SP for the CCW.

5. ICA gets the CCW and analyses the command byte of word Ø. The command in this case says input to Host.

6. ICA generates an External Interrupt to Host. During that sequence, the status of the adapter is also put on the line to Host. (sense byte 3)

7. IOAU sends back an acknowledge, which resets the External Interrupt, clears the input data lines and sense byte 3 (to all zeroes).

8. IOAU issues an External Function (EF) word to ICA to accept input. ICA determines if the command codes match (from C/SP and Host - C/SP wants to input to Host and Host will accept input).

Data Transfer begins.

9. ICA generates a Data Request of C/SP for data byte.

10. C/SP sends input byte.

11-12. ICA assembles a word, places the data on the input bus, and generates an input data request to IOAU. The data is sent during this time.

13. IOAU acknowledges the word has been received. Sequence #9 - 13 continues until the byte count in CCW goes to Ø.

Termination

14. ICA generates an External Interrupt to Host.

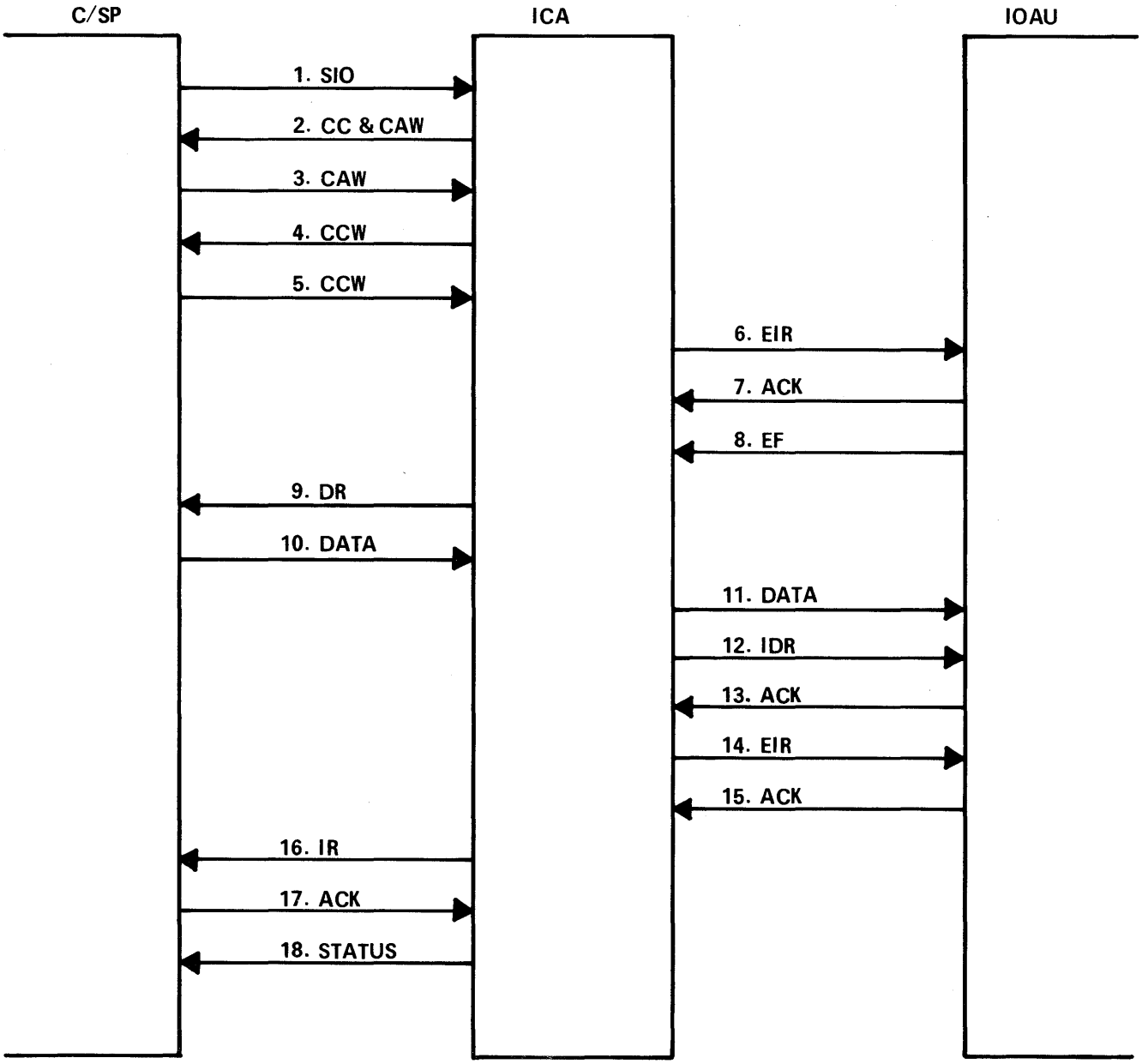
15. IOAU acknowledges.

16. ICA generates an Interrrupt request to C/SP indicating termination.

17. C/SP acknowledges it can accept the interrupt.

18. ICA sends the status halfword and interrupt code halfword to be stored in C/SP fixed memory location.

C/SP INITIATES DATA TRANSFER
ICA



HOST - (IOAU) INITIATES DATA TRANSFER

1. IOAU initiates data transfer by issuing an External function.

2. ICA generates an interrupt request to C/SP. When the C/SP acknowledges it can accept the interrupt, status is stored in fixed memory with the attention bit set.

3. C/SP must respond with a sense command.

4. ICA sends sense bytes. C/SP interprets the sense bytes and finds the Host has output for the C/SP and the amount of data to be transferred.

5. C/SP issues the output function.

Data Transfer Begins:

6. ICA generates an output data request to IOAU.

7. IOAU acknowledges and sends data word to ICA.

8. ICA unpacks the data word and sends the data bytes to C/SP.

9. C/SP acknowledges receipt of the bytes.

10. ICA, upon completion of the data bytes transferred to C/SP, requests another word from IOAU/Host and sequence #6 - 10 continues until byte count goes to Ø.

Termination:

11. ICA generates an External Interrupt to IOAU indicating termination.

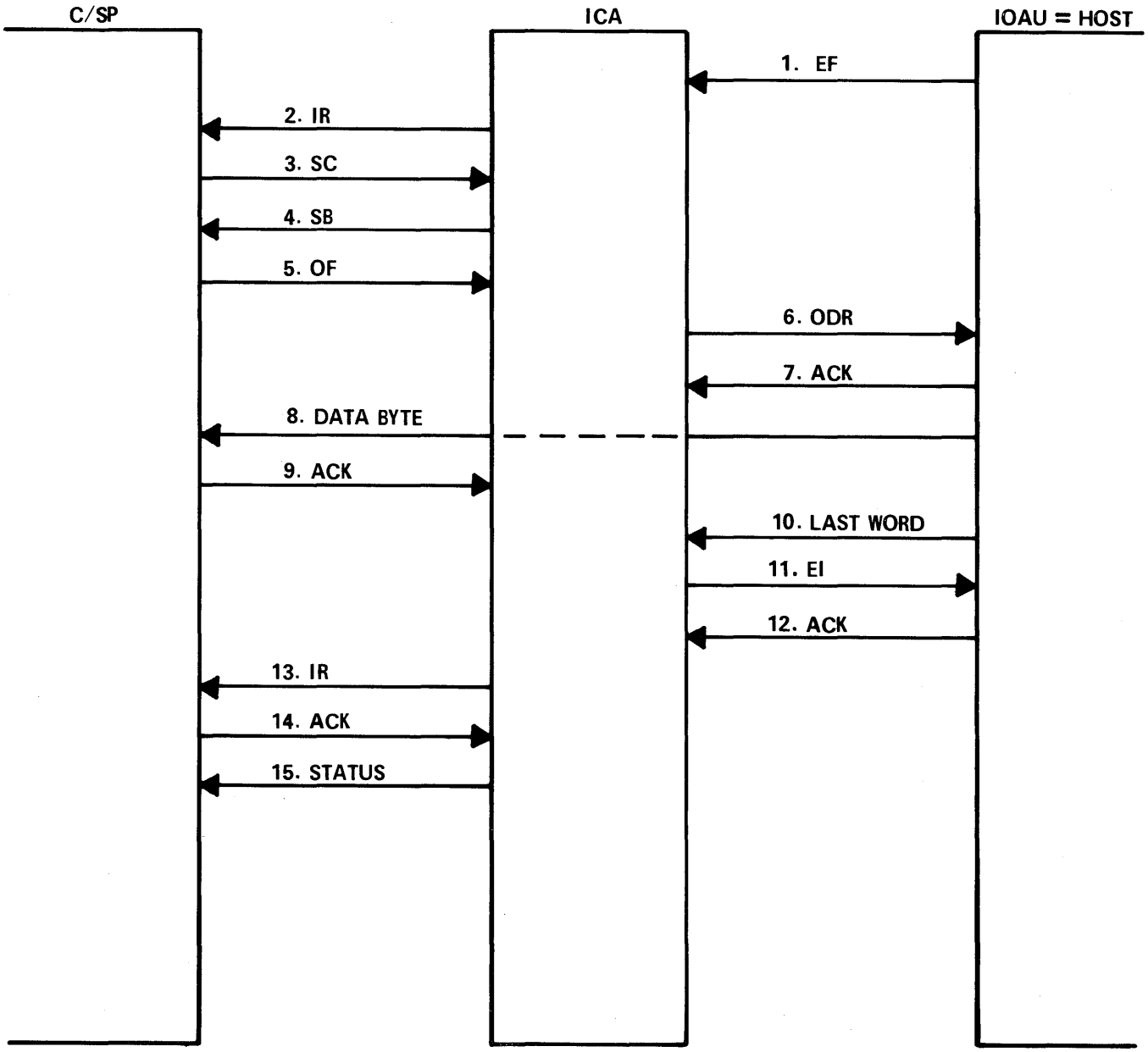
12. IOAU acknowledges.

13. ICA generates an interrupt request to C/SP to present status.

14. C/SP acknowledges indicating it is able to accept the interrupt.

15. ICA sends the status halfword and interrupt code halfword to be stored in C/SP fixed memory locations. C/SP checks status, etc. and takes appropriate action - in this case termination.

HOST—(IOAU) INITIATES DATA TRANSFER



FORMAT A

The bits indicated by X are ignored on output to C/SP and zero filled on input to Host. Four bytes per word, indicating quarter word mode.

FORMAT B

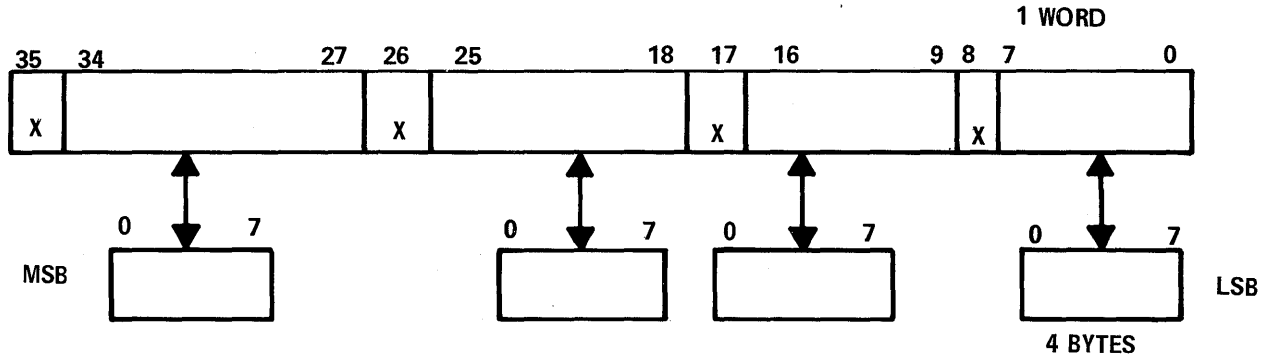
Bits indicated by XX are ignored on output to C/SP and zero filled on input to Host. Results in 6 Bit bytes, indicating field data.

FORMAT C

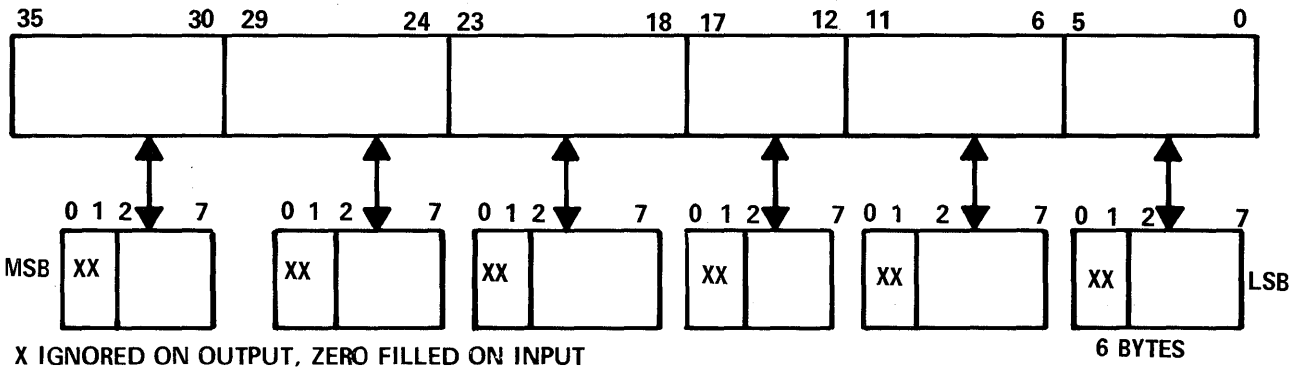
Double Word (72 bits) resulting in 9 bytes, indicating no loss of data.

ICA FORMATS

1108 FORMAT A

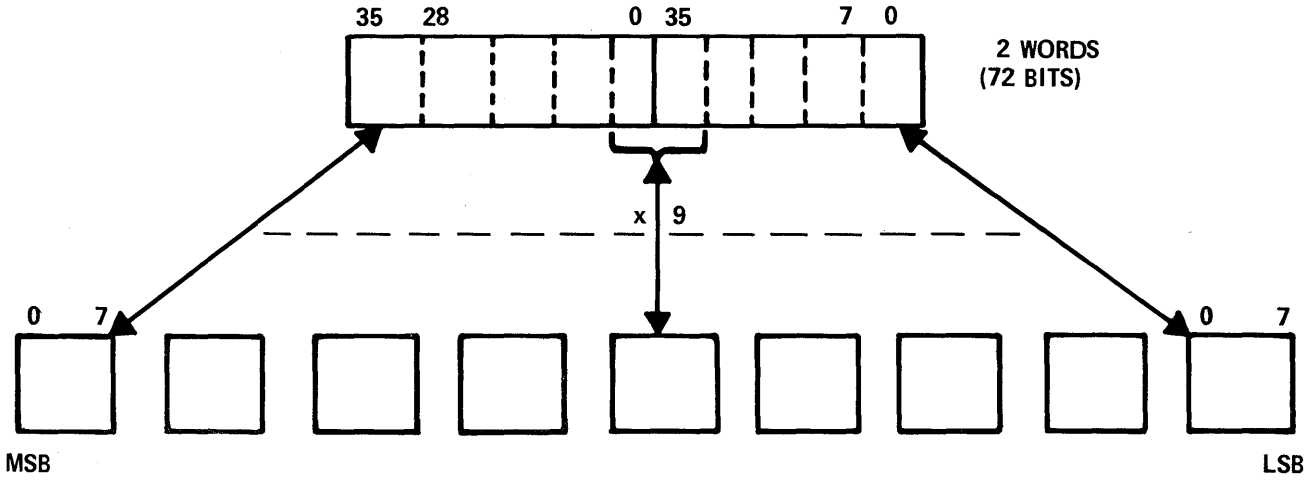


1108 FORMAT B



X IGNORED ON OUTPUT, ZERO FILLED ON INPUT

1108 FORMAT C



MSB – MOST SIGNIFICANT BIT
LSB – LEAST SIGNIFICANT BIT

SECTION V

GENERAL PURPOSE COMMUNICATION CHANNEL

SECTION V INDEX – GENERAL PURPOSE COMMUNICATION CHANNEL

General Purpose Communication Channel (GPCC)

The GPCC performs functions such as multiplexing the various CLT's, so that one CLT may be serviced at a time, recognizing special characters and/or sequences of characters, checking character parity, co-ordinating all data transfers to/from storage and executing other necessary operations.

The CLT's assemble and disassemble data characters for reception and transmission, from/to a communication line. The CLT's cover a wide range of communication with rates up to 50 kilobits/seconds, however, the CLT's must be selected so the combined rate of service requests (one per byte) is no more than 50,000 per second.

GPCC hardware consists of:

1. CLT's which provide the actual connection to the communication line or data set (as the case may be).

2. Timing assemblies to provide the line frequencies required by the CLT's.

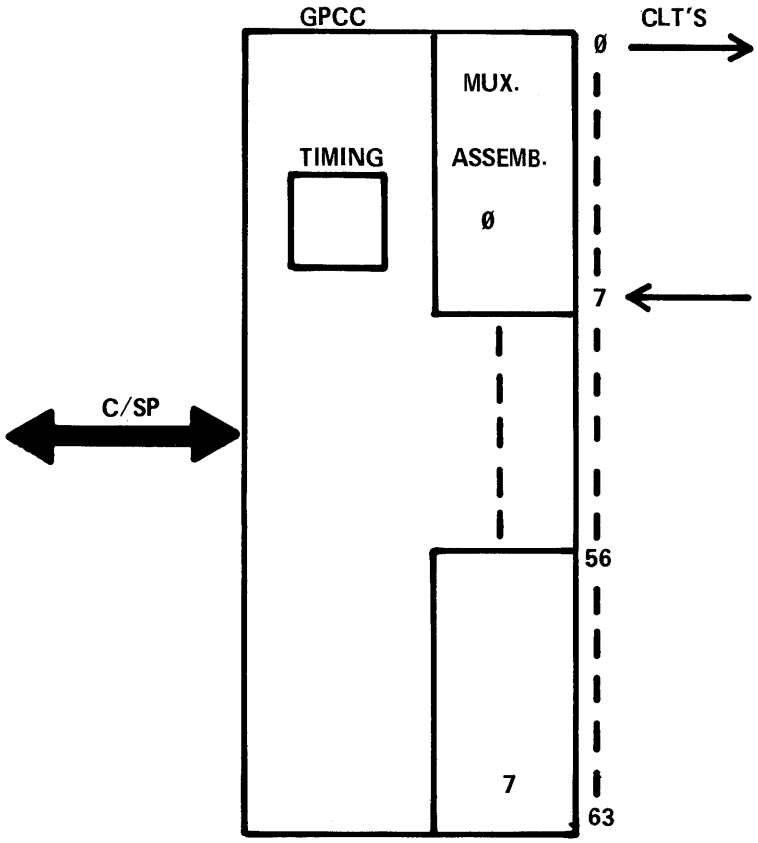
3. Multiplexer portion and assemblies provide the connection, on a priority basis, between the CLT's and the GPCC control logic.

4. CLT expansion up to 32 CLT's (full duplex)

5. GPCC control logic provides the basic logic which interfaces to, and controls the operation of the various CLT's, communicating with them as necessary through the multiplexer and its associated assemblies. In the GPCC control logic are a number of hardware registers, loaded under software control, which assist in these control functions.

6. CPU-I/O channel interface provides the interface between the processor/storage and the GPCC control logic. The interface logic recognizes and passes along SIO instructions intended for the GPCC. The logic requests storage access via the central storage priority network whenever required for data access or control information purposes. It also provides the logic path for interrupt requests from the GPCC to the C/SP (processor).

GENERAL PURPOSE COMMUNICATIONS CHANNEL (GPCC)



CHANNEL ADDRESS WORD (GPCC)

The CAW is accessed from storage by the GPCC when a SIO instruction with the GPCC channel # is detected. The CAW is used to initiate, modify, or terminate GPCC action. The GPCC stores the 16 most significant bits of the CAW in 'its' hardware and terms it an external function (XF) so as to distinguish it from any possible new CAW value associated with some succeeding SIO instruction. The actual execution of the stored XF may occur at some time later than the execution of the processor SIO instruction. If an SIO is issued while the GPCC is storing an unexecuted XF, it is rejected. There are 5 CAW formats and are distinguished by their most significant bits of byte 2.

Format 1 bit = Ø: Directed to an individual CLT, the address of which is specified in the SIO instruction used to turn CLT on, off, etc.

Format 2 bit = 1ØØ: Directed to the GPCC and loads a specified register within GPCC with a specified constant. Seven registers are available and vary in length between 4 and 7 bits. Three are used to establish the high order address bits of various control words in storage. The others used to search for other control codes, in data where Buadot or similar codes are used.

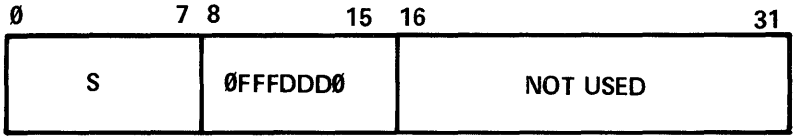
Format 3 bit = 11Ø: Used to modify specified bits within the first word of BCW.

Format 4 bit = 111: Used to replace the x-bits of BCW. These bits designate the currently active MDW. With the Y-bits of the BCW and GPCC register 2 they form the address of the current MDW.

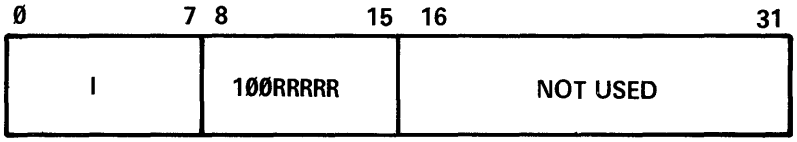
Format 5 bit = 1Ø1: Used to initiate an interrupt with special bits set in the CIW that is stored in the CIW List. Intent is to signal the controlling program through the interrupt handler routine that various time-outs have occurred.

GPCC CHANNEL ADDRESS WORD

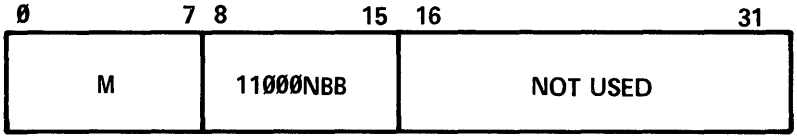
FORMAT 1 – COMMAND TO A CLT



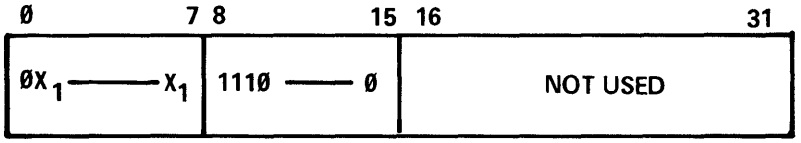
FORMAT 1 – LOAD PROGRAM LOADABLE REGISTER



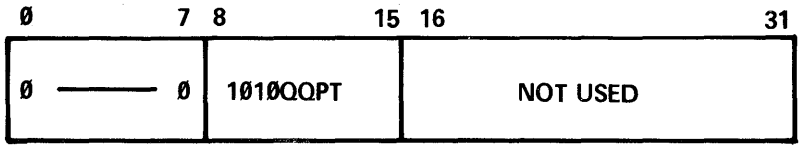
FORMAT 3 – MODIFY FIRST WORD OF BCW



FORMAT 4 – REPLACE X–BITS IN BCW



FORMAT 5 – INITIATE INTERRUPT



CONDITION CODE (GPCC)

THE GPCC RETURNS CONDITION CODES TO THE C/SP:

CC = ØØ	THE SIO INSTRUCTION WAS ACCEPTED
CC = Ø1	A PARITY ERROR OCCURRED ON A FETCH OF THE CAW
CC = 1Ø	THE GPCC IS BUSY
CC = 11	INDICATES THE GPCC IS OFF-LINE OR IN A FAULT CONDITION. NO ACTION TAKEN

CONDITION CODE
GPCC

SIO | CHANNEL NO. | DEVICE ADDRESS |

CC = ØØ ACCEPTED

CC = Ø1 PARITY ERROR ON FETCH OF CAW

CC = 1Ø BUSY

CC = 11 NO ACTION OFF LINE/FAULT CONDITION

CAW FORMAT 1

This format is directed to an individual CLT, the address of which is specified in the SIO instruction.

S = SYNC character to be loaded into the CLT when required. Left justified with the unused bits equal to zero. A SYNC character of all zeros is not allowed as it is translated as an asynchronous CLT operation.

Bit 8: Format select - must be zero.

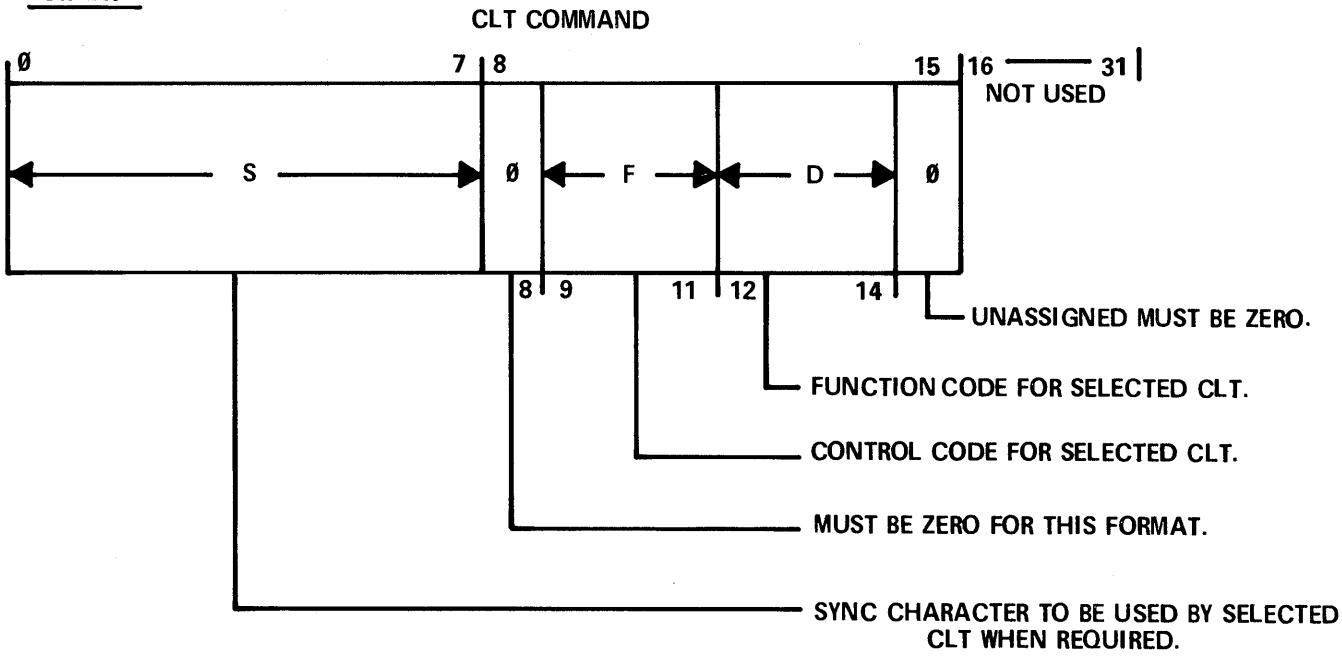
F: Control CLT action - Turn on/off input/output, enter test mode, disconnect from the communication line and turn off output, disconnect CLT from system, Mode Set.

D: Detail bits of XF code for the CLT. Combine with the 3-bit F-field indicating level of code used, number of stop bits to transmit, mode of CLT (half duplex or full).

Further explanation of the F and D fields in covered on the external functions of the CLT's.

CHANNEL ADDRESS WORD FORMAT
GPCC

FORMAT 1



CAW FORMAT 2

This format is directed to the GPCC and loads a specified register within the GPCC with a specified constant. There are 7 program loadable registers, which vary in length between 4 and 7 bits. Three of these registers are used to establish the high order address bits of various control words in storage. The others search for FIG/LTRS or other control codes, in data where Baudot or similar codes are used.

I = byte or partial byte to be stored in the GPCC register specified by the R-field and must be right justified.

bits 8 - 10 - Format select: Store data (I) field in a GPCC register.

R = specify the address of the register in the GPCC to be loaded.

Register 1: 7 bits - MSB of address for BCW's.

Register 2: 4 bits - MSB of address for MDW's.

Register 3: 7 bits - MSB of address for CIW's.

Register 24: 5 bits - special symbol for 5 level code.

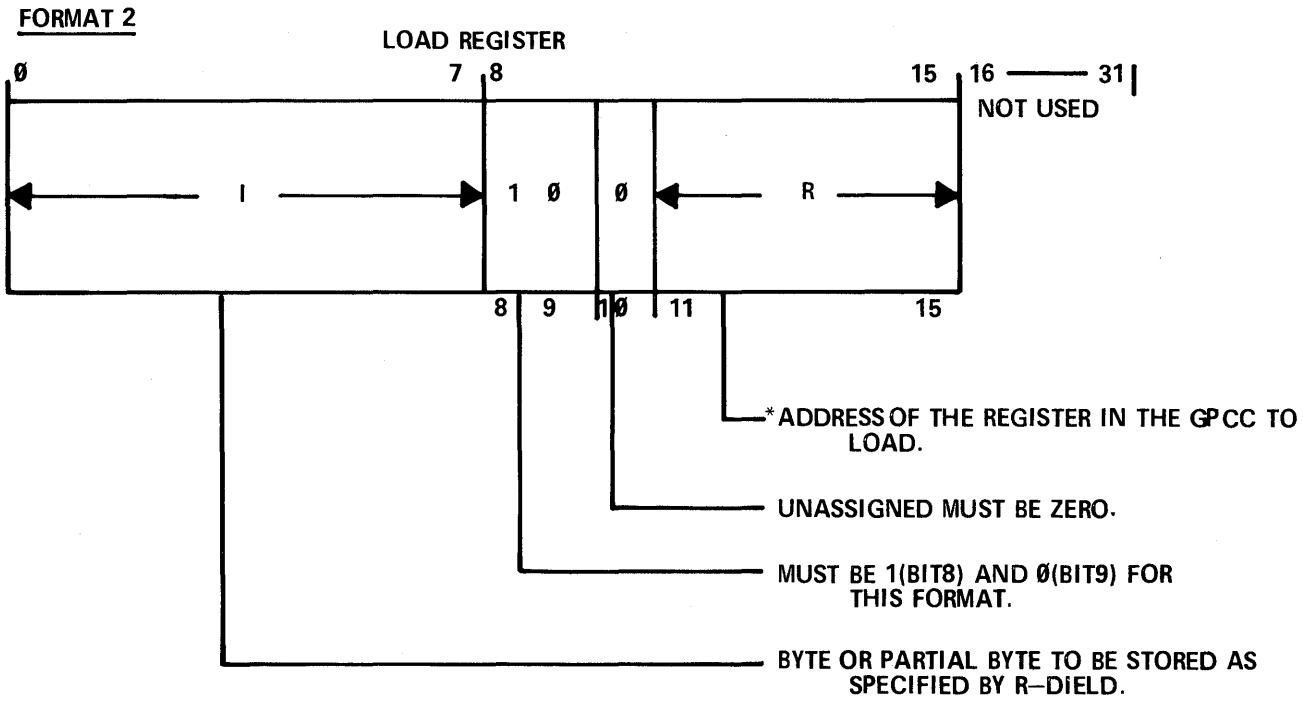
Register 26: 5 bits - special symbol for 5 level code.

Register 27: 6 or 7 bits - special symbol for 6 and 7 level code (7 level if parity generation/checking specified).

Register 28: 6 or 7 bits - same as Register 27.

Registers 25 - 28: specify the code level to be used by the addressed CLT.

CHANNEL ADDRESS WORD FORMAT
GPCC



*REGISTER 1	M.S.B. ADDRESS BCW – 7 BITS
REGISTER 2	M.S.B. ADDRESS MDW – 4 BITS
REGISTER 3	M.S.B. ADDRESS CIW – 7 BITS
REGISTER 25	SPECIAL SYMBOL LEVEL 5 CODE – 5 BITS
REGISTER 26	SPECIAL SYMBOL LEVEL 5 CODE – 5 BITS
REGISTER 27	SPECIAL SYMBOL LEVEL 6 CODE – 6 BITS
REGISTER 28	SPECIAL SYMBOL LEVEL 6 CODE – 6 BITS

CAW FORMAT 3

This format is used to modify specified bits within the first word (control word) of the Buffer Control Word (BCW) in a manner to avoid race conditions. The BCW may be modified by instructions in the processor repertoire. If a BCW is being used by the GPCC at the time an instruction is used to modify the BCW, it is possible that the GPCC will write into the BCW in storage and overlay the area written into by the instruction. Use of this format quarantees the BCW will be set to the condition specified.

M = mask bits: May be used to select any or all of bits of byte BB of BCW word zero.

bits 8 - 10: format select indicating CAW format 3.

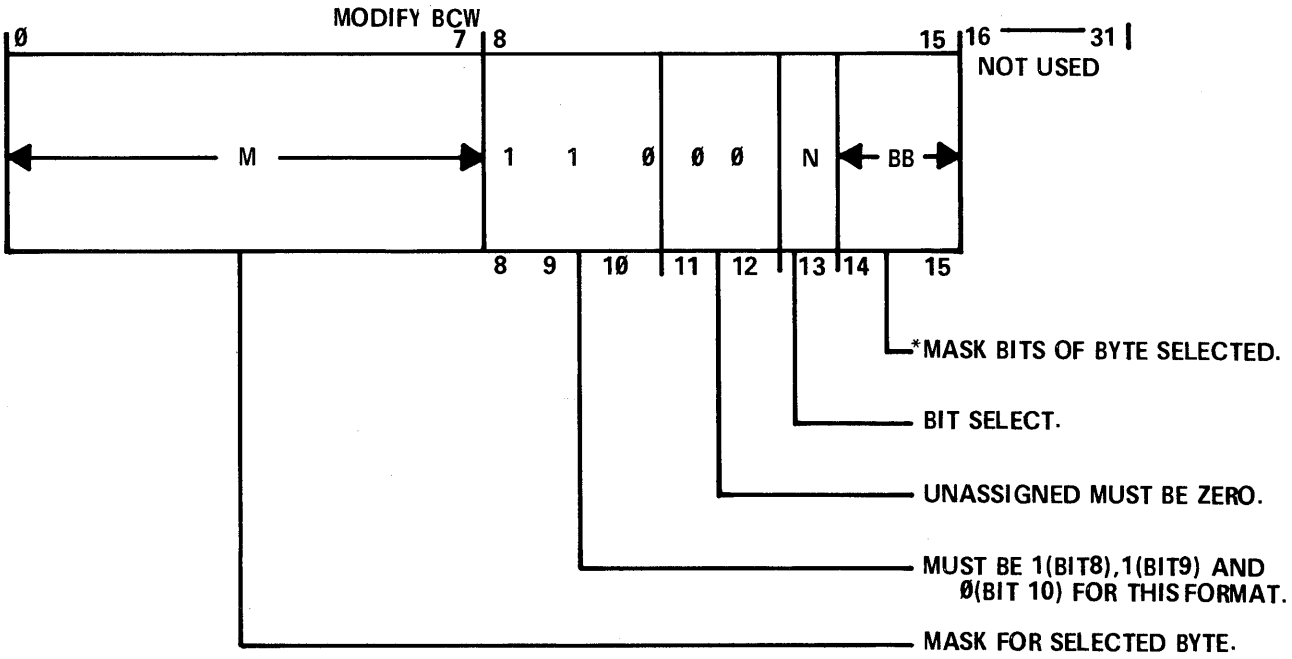
bits 11, 12: must be zero.

N = all selected bits in designated byte (BB) of BCW are set to match this value. Works in conjunction with the mask field (M).

bits 14, 15: designate byte of BCW Ø to be operated on by bit (N) in conjunction with mask (M).

CHANNEL ADDRESS WORD FORMAT
GPCC

FORMAT 3



ØØ = BB BYTE Ø, BITS Ø–7
Ø1 = BB BYTE 1, BITS 8–15
1Ø = BB BYTE 2, BITS 16–23
11 = BB BYTE 3, BITS 24–31

CAW FORMAT 4

This format is used to replace the x-bits within the BCW. The x-bits designate the currently active Message Discipline Word (MDW).

This format can be used to initiate a chain of MDW's.

Execution of the XF depends on the setting of the 'U' and 'M' bit in the designated BCW; If U = 1 and M = Ø, instruction is executed as described. If U = Ø or M = 1, the X-field is not replaced and an interrupt request is generated. A CIW using format 3 is stored.

bit Ø - must be zero.

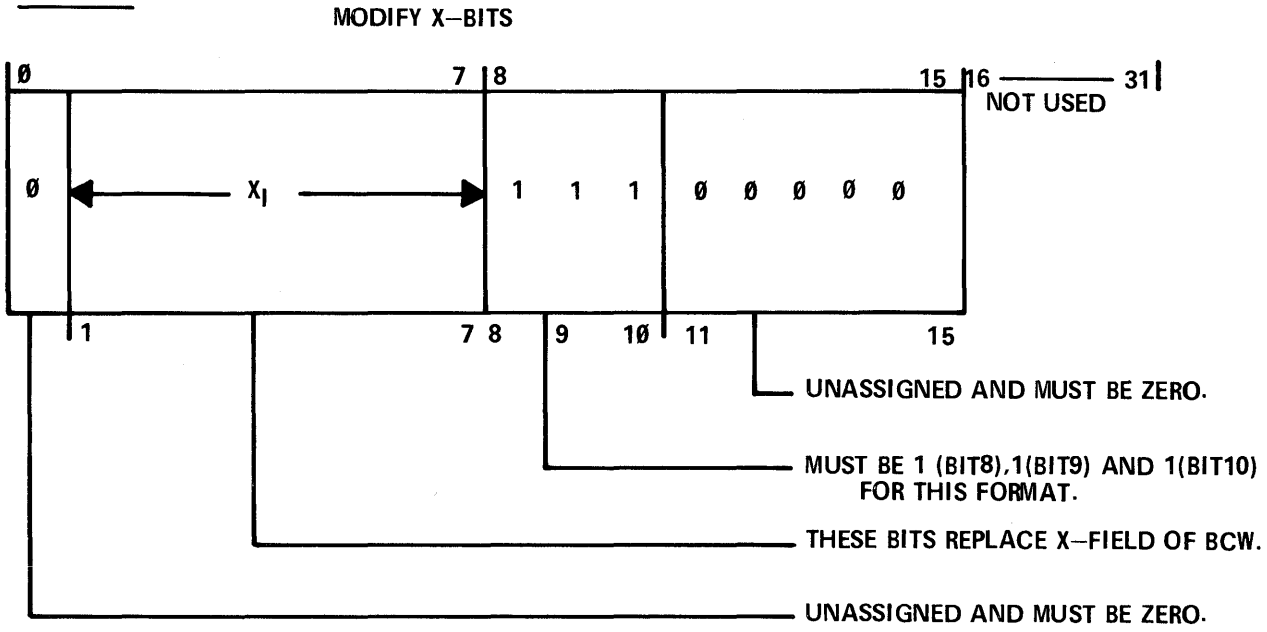
X_I - the address of the next MDW and replace X-field of the BCW.

bits 8 - 1Ø: format select indicating CAW format 4.

bits 11 - 15: must be zero.

CHANNEL ADDRESS WORD FORMAT
GPCC

FORMAT 4



CAW FORMAT 5

This format is used to generate an interrupt request and store a CIW of Format 3 type. Intent of this interrupt is to signal the controlling program, through interrupt handler, various time-outs have occurred. Format 5 is directed to the GPCC.

bits Ø - 7: must be zero.

bits 8 - 10: format select indicating CAW format 5. Generate an interrupt request and store a CIW for Format 3 with P and T Bits placed in the CIW. The device address in CIW is CLT address from SIO.

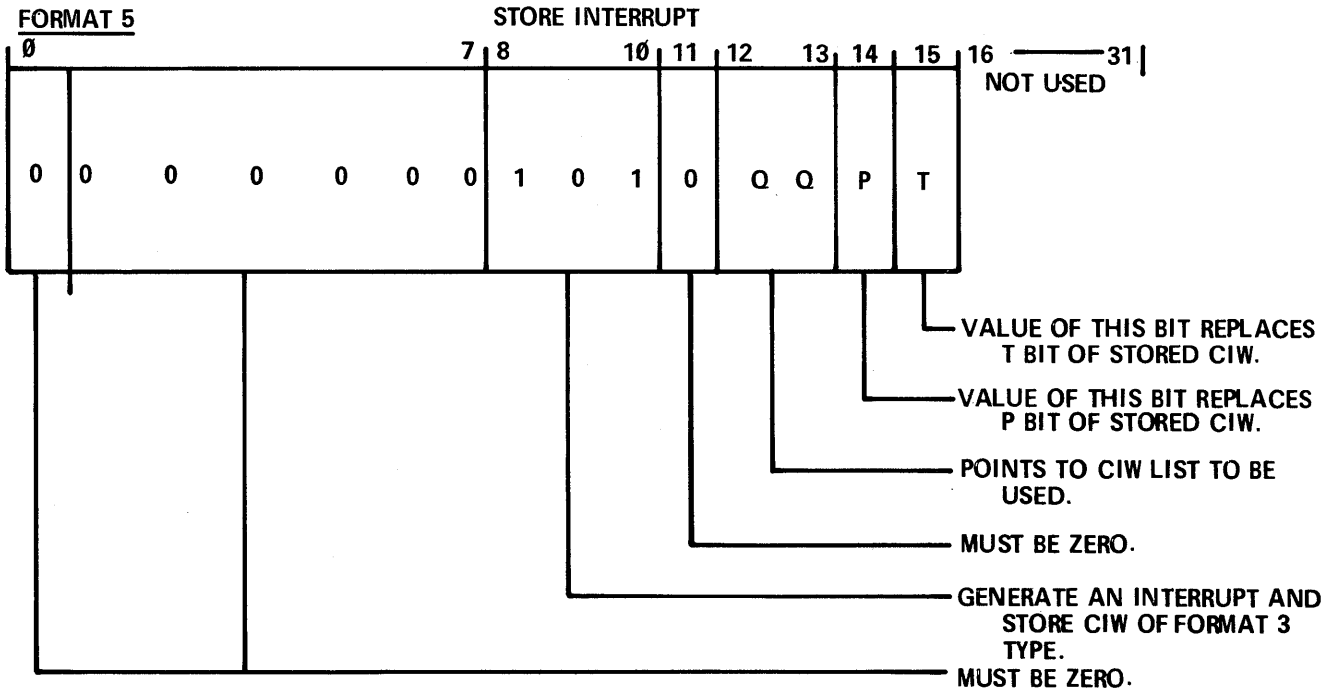
bit 11: must be zero.

QQ: which CIW List to store interrupt information.

P: this value will be placed in P-bit of CIW.

T: this value will be placed in T-bit of CIW.

CHANNEL ADDRESS WORD FORMAT
GPCC



BUFFER CONTROL WORD ADDRESS

Associated with each position on the multiplexer is an area in storage called the Buffer Control Word. The BCW contains status and control information, an X-field for an MDW address, data buffer address and length control fields. The status and control areas handle communication control and interrupt information. The MDW address points to an MDW within a channel program, consisting of a series of MDW's, which control data flow to/from the CLT.

BCW address is formed;

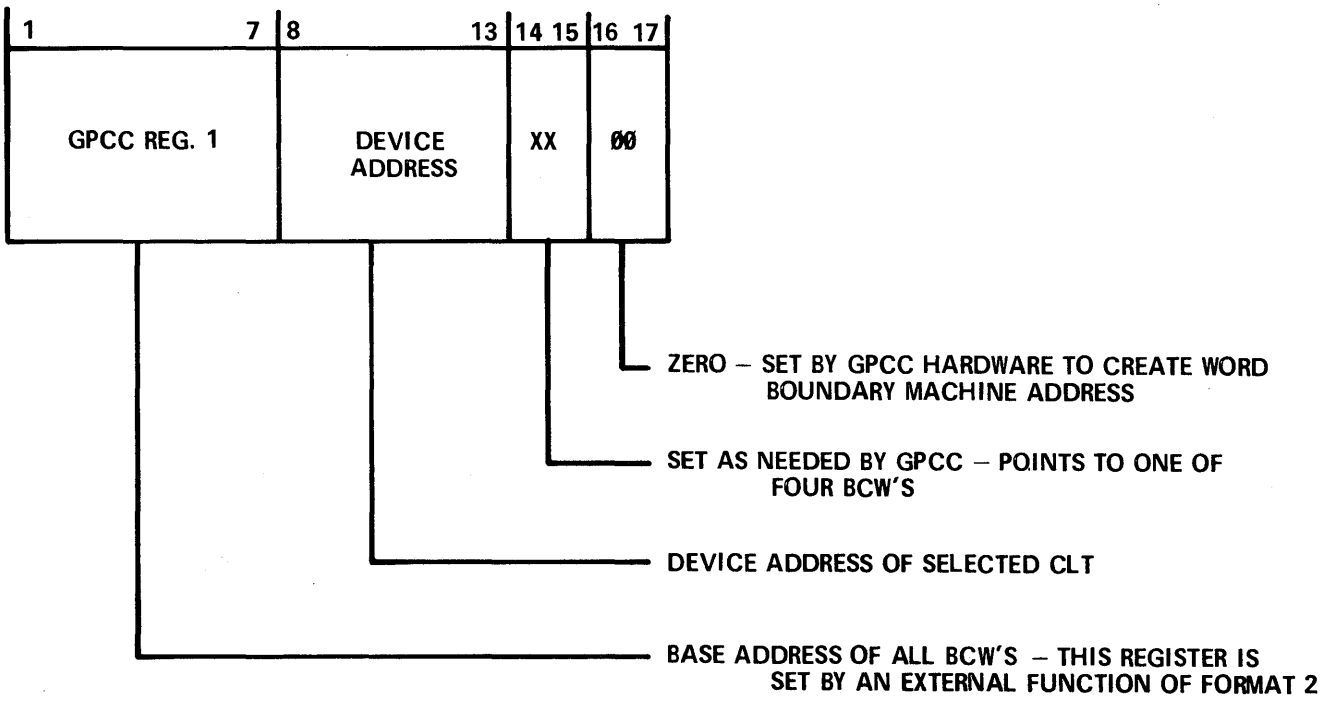
bits 7: contents of GPCC register 1. The register is set by XF of format 2.

bits 8-13: The device address of the selected CLT.

bits 14-15: specify 1 of 4 words to the BCW to be accessed (set as needed, by GPCC hardware).

bits 16=17: used by GPCC hardware to create an actual machine (byte) address.

BUFFER CONTROL WORD ADDRESS
GPCC



BCW FORMAT

The BCW's exercise primary control over the flow of data between an individual CLT and storage. Each multiplexer position has a corresponding BCW assigned to it. Full duplex CLT's (use two multiplexer positions) have 2 BCW's. Each BCW is 4 machine words in length. The base address of this table is defined by GPCC register 1.

The BCW has four kinds of control data within it:

1. Status information is stored in the CIW; however, certain parts are also stored in the BCW (word Ø) so the GPCC may also reference it.

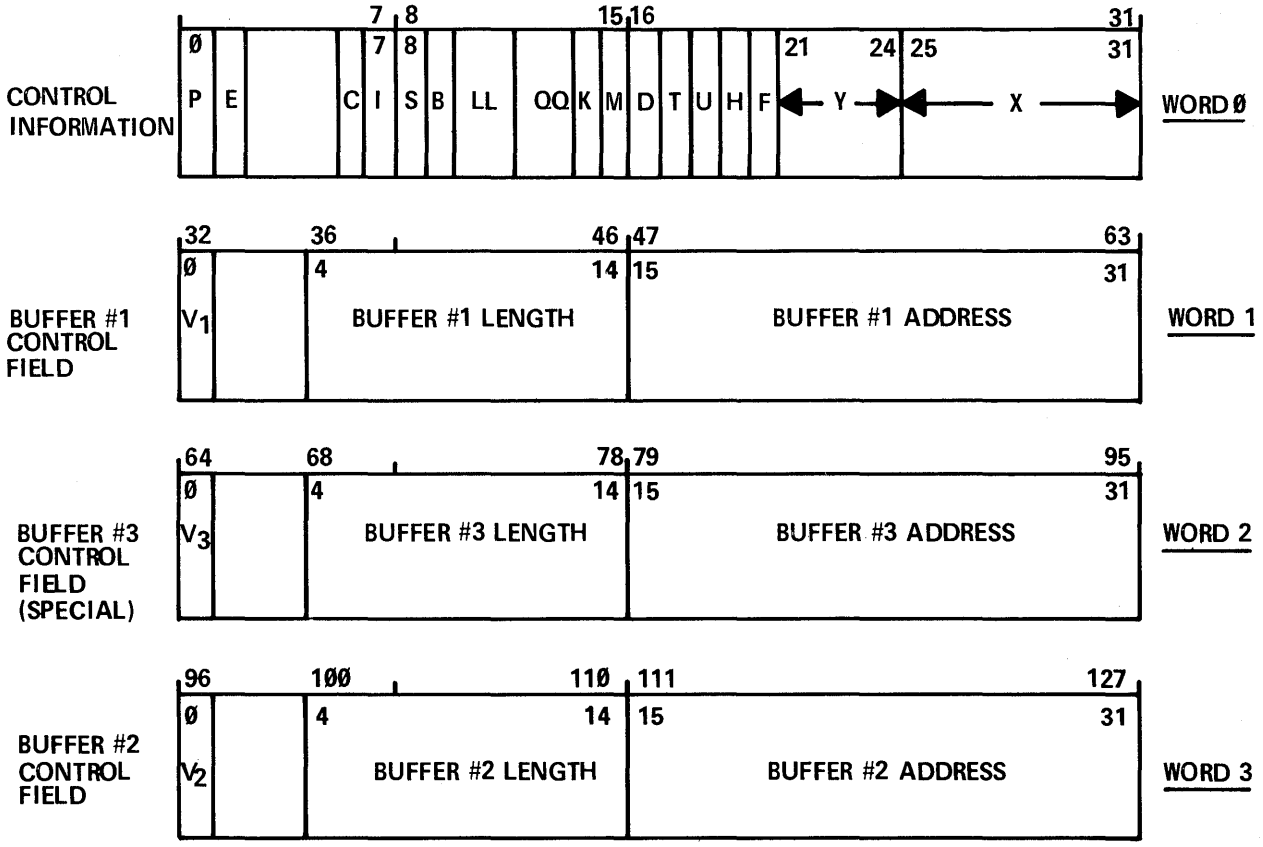
2. BCW (word Ø) has 13 bits for control purposes. These include control bits which the GPCC may change on an individual basis as the result of a service request sequence. Bits to control those message functions that are time invariant during a message (such as the code level) are also included.

3. BCW (word Ø) has an MDW address of 11 bits (current MDW).

4. Four of those bits (Y) designate the base of the MDW's which apply to a given message discipline. The remaining seven bits (X) indicate the specific MDW that is currently to be used. The X-bits may be replaced by XF or, under MDW control, during a service request sequence.

5. The last three machine words (1, 2, 3) of the BCW have identical formats and are used to control the buffer length and address of each buffer segment. Only one of these is active at any given instant as control toggles between word 1 and 3 as each buffer is completed. Word 2 provides a special buffer which may be selected under XF or MDW control (i.e., used for embedded messages). The buffer address and length fields specify the storage address and byte count (up to 2Ø48) to be transferred.

BUFFER CONTROL WORD FORMAT
GPCC



BCW (Word 1 and 3)

BCW control fields - control the storage address being used for the transfer. Normally, control alternates between word 1 and 3 whenever the length field is decremented to zero. The currently active word is designated by the H-bit of BCW word Ø. Word 2 may be activated to control the storage address transfer under control 'S' of the current MDW. In general, word 2, enables the partitioning of special messages into an area of storage which is separate from that which is used for the data text into which such messages are embedded for transmission purposes. While one buffer control field is active, the other 2 may be manipulated.

BCW - Word 1

V_1 (bit 32) - used to prevent violation of buffer boundaries. When the length is stepped to Ø, V_1 is set. If a new buffer address has not been established and V_1 is reset by the time another buffer has been exhausted, a service request would attempt to access a storage beyond the limits of the buffer and a CIW (format 3) is stored and 'W' (wrap around) bit set to 1.

On output this violation (buffer wrap around) causes termination. Therefore, service requests which occur before V_1 is reset, will not store additional CIW's nor will the data character be transferred to storage or the buffer address modified. Other operations in the service request occur normally; as a compare for match with character in MDW.

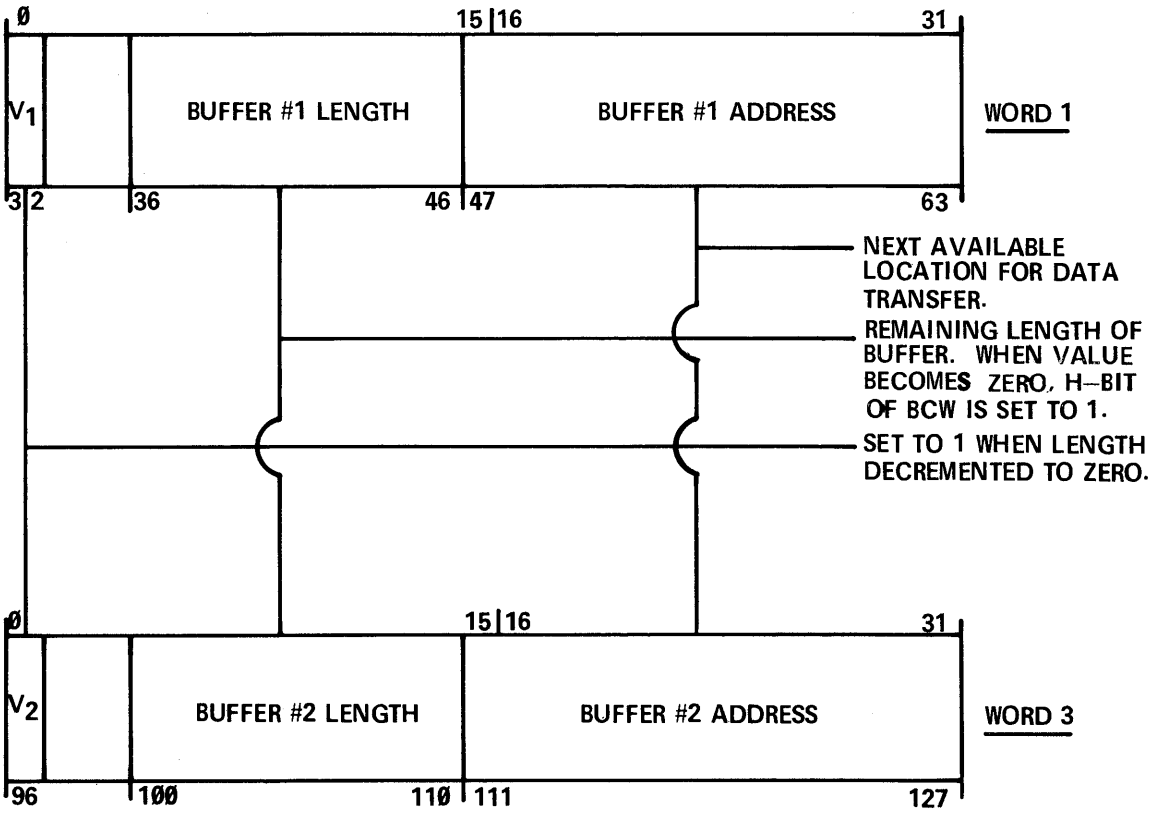
On input, if the GPCC finds $V_1 = 1$, the buffer length is examined. If all Ø's, indicates this is the service request which first discovered the violation. The CIW is stored etc., and the buffer length is decremented from all Ø's to all 1's. Subsequent service requests find V_1 set, detect the buffer field is all 1's and inhibit both generating a CIW and modifying the buffer length field.

Buffer length: Remaining length of the buffer (2Ø48 bytes maximum) decremented.

Buffer address: next available location (incremented).

BCW - Word 3 Same as word 1 except when buffer length goes to Ø, H in BCW Ø is set to Ø and control toggles to BCW word 1.

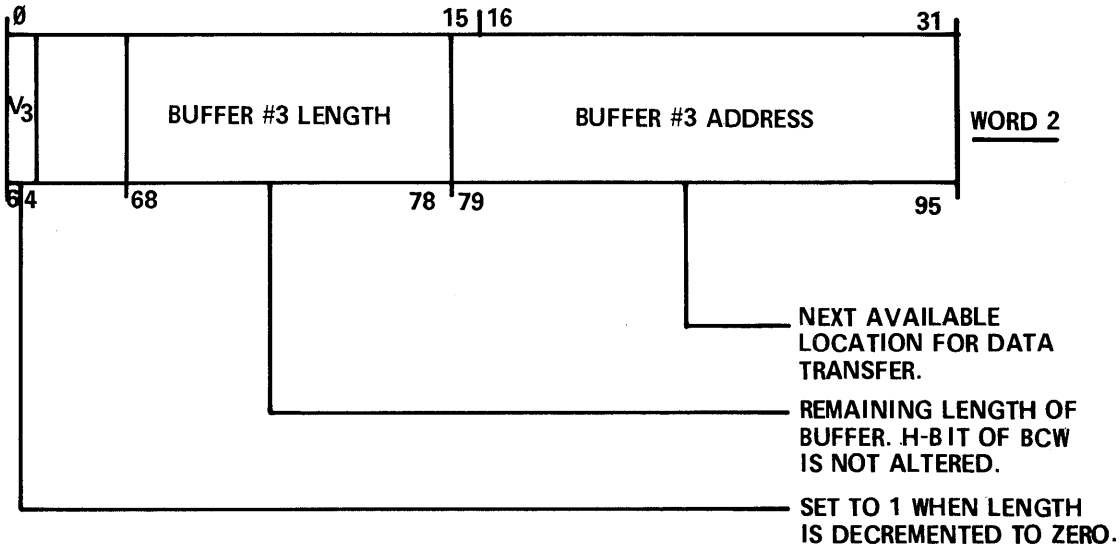
BUFFER CONTROL WORD
GPCC



BCW (Word 2)

Same as word 1 except H-bit is not effected when buffer length goes to zero. MDW program has to insure another buffer control field is activated. The MDW sequence has its 'S' bit set to 1 indicating use of BCW 2. This bit overrides the H-bit setting in BCW Ø.

BUFFER CONTROL WORD
GPCC



Buffer Control Word (Word Ø)

Control bits S, K, M, D, T, U, H, and F - normally initialized by the program to pass information to GPCC and may be modified during the course of a service request sequence.

S-bit: Set and reset by GPCC hardware. Reflects the state of the MDW last accessed. When set, indicates data was last transferred under control of BCW word 2.

K & M: When K = 1 and LL = ØØ, indicates a 5 level code received or sent and conversion to or from 6-level code in storage is desired.

See Appendix A for more information.

M-bit: Also used in conjunction with 'D' bit of the MDW to control the duplication of control character as required in transparent text.

D-bit: Established the direction of data flow. Ø = storage to CLT (output), 1 = CLT to storage (input).

T-bit: Turn off CLT after it transmits the character obtained in this service request. Conditions which set the T-bit:

1. Program intervention.
2. $T_Ø$ set in MDW and $X_Ø \longrightarrow$ X in BCW.
3. $T_Ø$ through T_6 bit set and a match occurs on C_1 - C_6 of MDW.
4. C-bit set (Bit 26 in CIW - control parity error of CIW format 3).
5. A-bit set (Bit 25 in CIW format 3 - address error MDW, BCW or data).
6. W-bit set (Bit 23 in CIW format 3 - buffer wrap around - output only).

U-bit: Determines whether or not the GPCC will execute the XF 111 (format 4 CAW); Ø = inhibit, 1 = allow.

H-bit: Determines which Buffer Control field is to be used. When a buffer is exhausted, the state of the H-bit is toggled to select another buffer control field and a CIW of Format 3 is stored. H = Ø, BCW word 1; H = 1, BCW word 3.

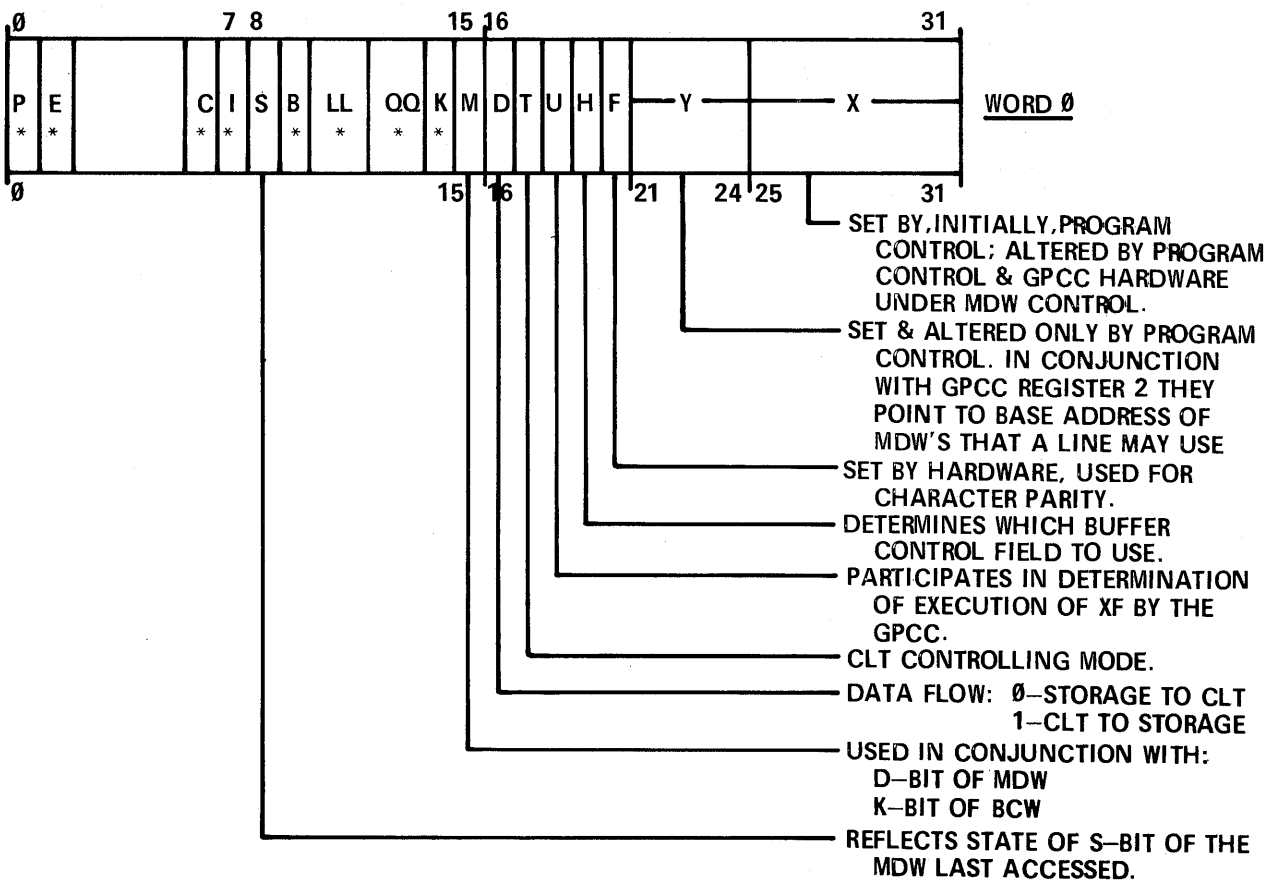
F-bit: Indicates a character parity error has occurred. On input, the F-bit is set only if the character is to be transferred to storage and bit Ø of the data byte is then set to 1.

X & Y bits: Indicates the address of first word of current MDW. 'Y' is base address of all MDW's for given line and 'X' designates the specific MDW of that set.

'X' - set by controlling program, altered by program and by GPCC hardware under MDW control.

'Y' - set and alterable by the controlling program only. In conjunction with GPCC register 2 they specify the base address of all MDW's a line may use.

BUFFER CONTROL WORD
GPCC



*NEXT FOIL

BCW (Word Ø) continued

These bits are set by the program and are not modified by GPCC hardware during course of a service request sequence. Similar bits also assigned in the MDW. P and E bits are not used when MDW is effective (B=Ø). QQ bits of BCW may be assigned differently from the QQ bits of an MDW and are used under different conditions.

P = parity bit; If set to 1, generate parity on output or test for parity on input. Has no effect unless 'B' is set to 1. If P is 1 on output and data from storage has incorrect parity, the GPCC makes the parity incorrect for the corresponding data character when it sends the character to the CLT (intent is to signal remote receiver to request re-transmission). If P = Ø on output, the GPCC sends the data unmodified to the CLT.

E - controls odd or even parity: Ø = odd, 1 = even. Setting has no effect unless 'B' and 'P' are = 1.

QQ = specify which list is to be used to store information in CIW. Used in all cases except:

1. When 'B' of BCW is Ø and CIW of format 1 is being stored, the QQ from the MDW is used.

2. An SIO instruction is issued to GPCC with CAW format 5, QQ from the CAW is used to select list into which the CIW of format 3 is written.

3. A CIW of format 3 is to be stored because an error condition exists which sets 'A' or 'C' to 1 in format 3 CIW, the value of QQ is forced to 11_2.

C & I = (status bits) set by GPCC whenever an error occurs during an attempt to store a CIW. When set indicates no CIW may be stored and the channel status word has its least significant bit set to 1, otherwise it is all zeros.

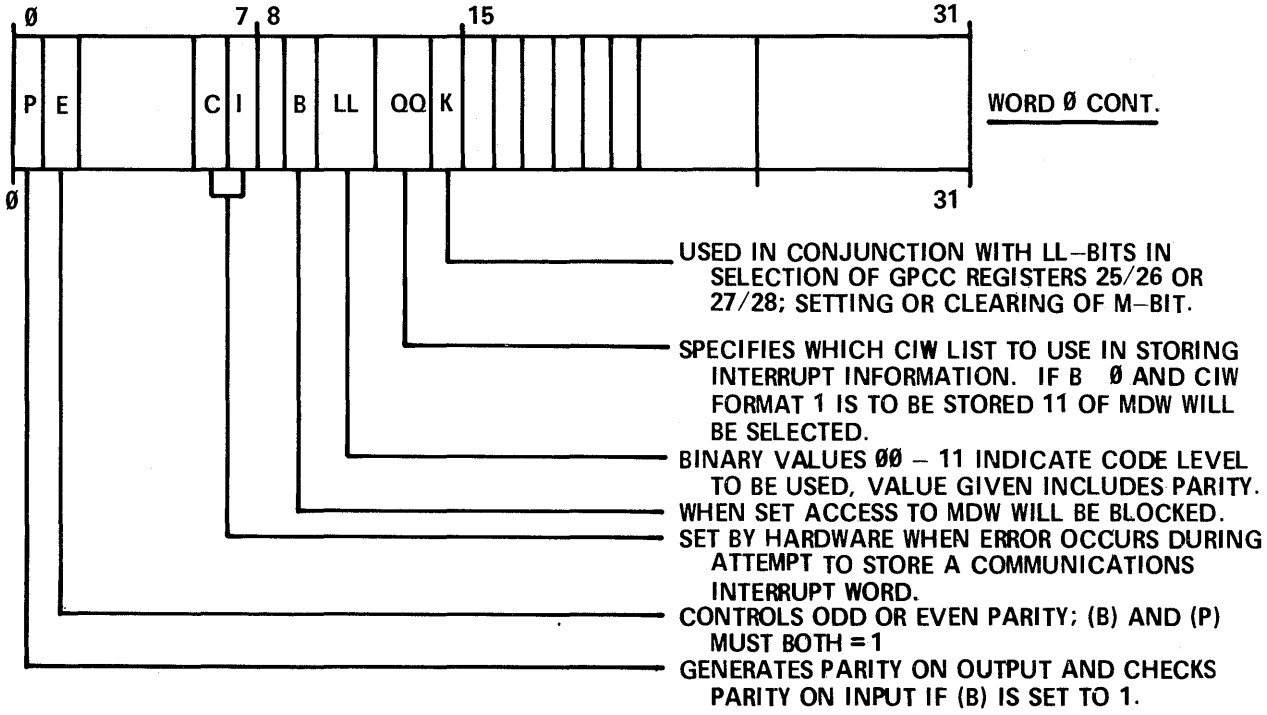
See Appendix A for more information.

B & LL bits = set by controlling program and are not modified by hardware in the course of a service request sequence.

B = if set, access to an MDW will be blocked, (makes CLT transparent, treating control characters as data).

LL = indicate the code level of a single character as 5, 6, 7, or 8 bits. The code level used by the CLT is specified in the CAW when an XF is issued to the CLT. 'LL' in BCW and CAW should be equal to bits per character including parity as seen by the actual communications line. Hardware reaction to the specific of 'LL' is otherwise indeterminate. On input (when parity specified) the parity bit is removed from the resulting byte before the byte is transferred to storage.

BUFFER CONTROL WORD
GPCC



MDW ADDRESS

bits 1-4 = contents of GPCC register 2. This register is set by an XF (CAW format 2).

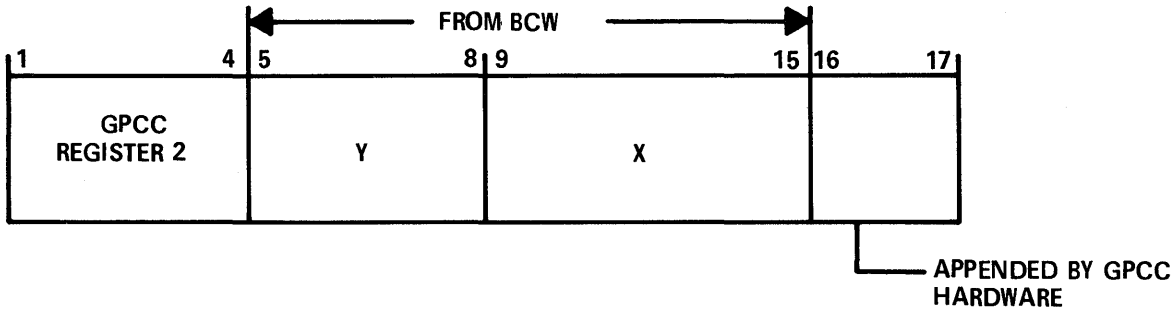
bits 5-8 = Y: from BCW, specify the base address of all MDW's that a line may use.

bits 9-15 = X: from BCW, reflect the address of the current MDW.

bits 16, 17 = appended by GPCC hardware to create actual address (byte).

This address is initiated by the program and is changed by the current MDW as a function of the data and message format.

MESSAGE DISCIPLINE WORD ADDRESS GPCC



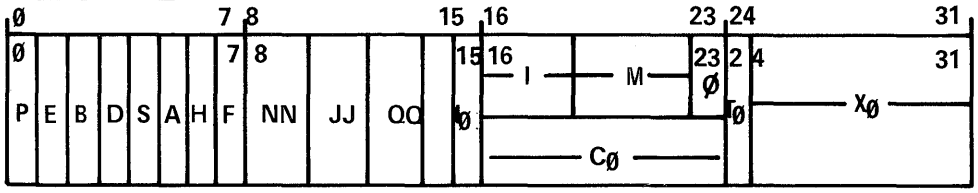
MDW FORMAT

Message Disipline Word (MDW) - used to supplement control provided by the BCW. BCW (word Ø) specifies whether an MDW will be accessed, and if so, which MDW. MDW's in storage define a given message discipline, are re-entrant since the hardware in no way modifies an MDW as a data transfer proceeds. Time variant control bits and the 'X' field which designates the currently active MDW are stored in the BCW. The MDW list may then be used by all lines that generate under the same message discipline. An MDW may be 1, 2, 3 or 4 machine words in length. The length is specified by 2 bits in the first word of the MDW. The main function of word Ø of an MDW is to provide control for the use of up to 6 characters of compare information that are contained in the last 3 words of an MDW. Also provides control for characteristics of a message which may be time-variant (parity checking/generation, and if so, odd or even). Each additional word contains two characters (up to 6 for the 3 words) and a T-bit, X-field associated with it. Each character is compared (by GPCC hardware) against the incoming or outgoing message. When a match is found, the associated T-bit, if 1, is moved to the T-bit position of the BCW and termination occurs. The X-field bits are also moved to the BCW where they replace the X-bits, which performs a transfer control, (due to the X-bits of BCW determining which MDW is to be used). All characters of a given MDW are compared until a match is found, then the X-bits are moved to the BCW to indicate a new 'current' MDW. Thus, contiguous character sequences may be generated, detected, etc., through a sequence of MDW's.

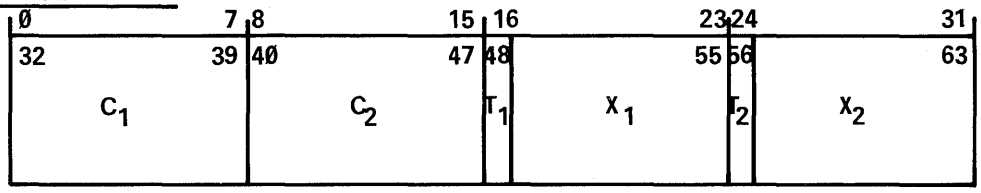
Control bits of word Ø allow for the generation of an interrupt word or the blocking of input-characters. Transfer to storage individually on each of the characters (in MDW's 1, 2, 3). Word Ø may also be used to directly insert a character into the output data stream. Another function provided by the MDW is activation and deactivation of special buffer address and length fields contained in word 2 of the BCW. This allows embedded messages to be transmitted on output, or recognized and partitioned on input. Such messages are used for acknowledges, polls, etc., in full duplex system.

MESSAGE DISCIPLINE WORD FORMAT
GPCC

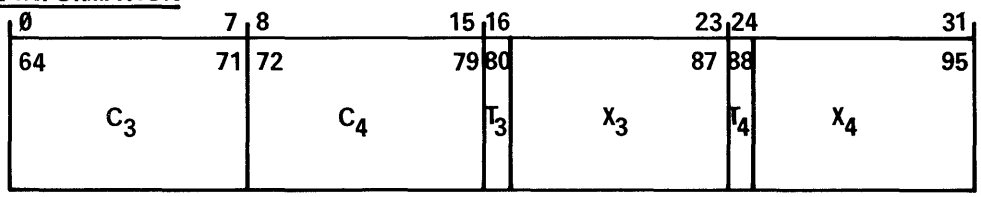
CONTROL INFORMATION



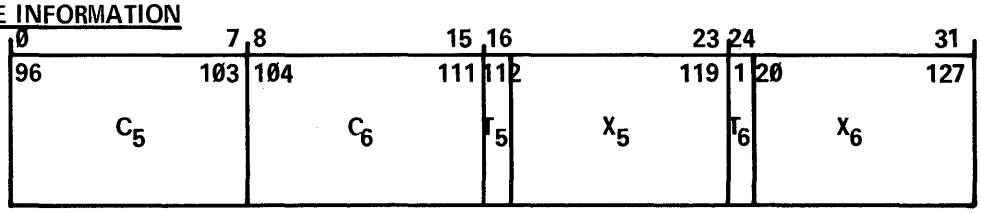
COMPARE INFORMATION



COMPARE INFORMATION



COMPARE INFORMATION



MDW (Word 1) COMPARE INFORMATION

C_1 - forms a character which the GPCC hardware compares against each character of the message as it is transferred. Comparison is performed on both Input and Output (if successful, termed a match). Must be right justified and leading zeros. Results of match: $X_1 \rightarrow$ S of BCW and new MDW selected, to be effective on next character of the message, T_1, if = 1, replaces 'T' of BCW causing termination at end of current message character.

C_2 - second compare character used as C_1, only T_2 and X_2 are used with it (same function as T_1 and X_1). C_1 and C_2 are compared in parallel with the data character. If C_1 and C_2 are =, and $X_1 = X_2$ then X_1 replaces X of BCW if match occurs.

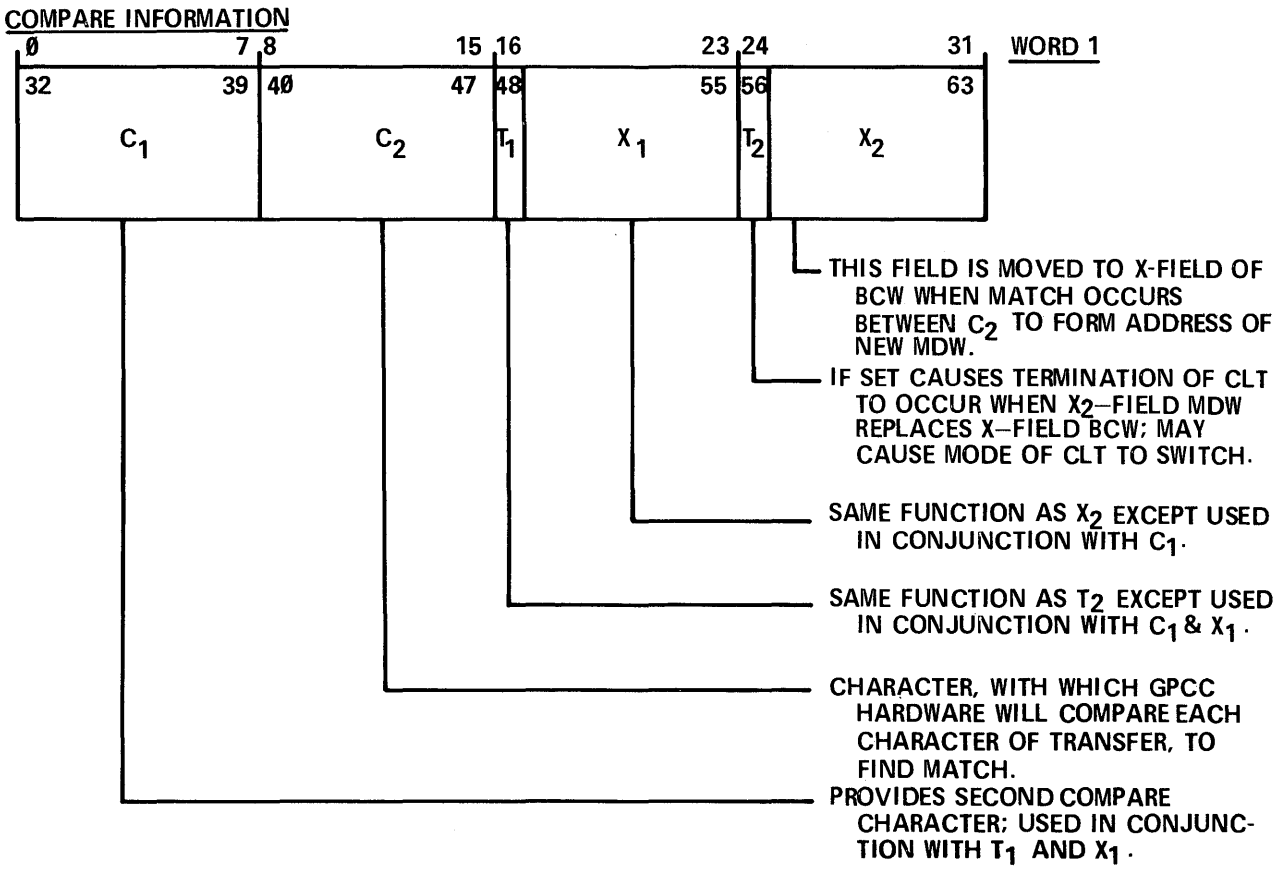
T_1 - If 1, causes a terminate whenever X_1 replaces X of BCW. T of BCW is set to 1 and terminate is signalled to the CLT causing switch from output to input (half-duplex).

X_1 - replaces X of BCW when match occurs. Exception-during duplication of character to the communication line.

T_2 - same as T_1 only in conjunction with C_2 and X_2.

X_2 - same as X_1 only in conjunction with C_2.

MESSAGE DISCIPLINE WORD
GPCC

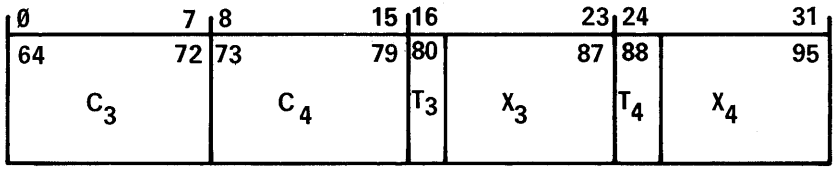


MDW (Word 2 and 3) COMPARE INFORMATION

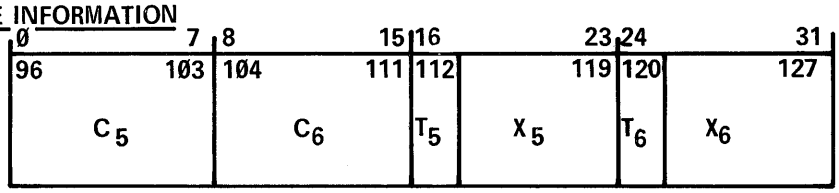
MDW - word 2 and 3 - same as word one. Makes possible the expansion of up to 6 possible compare characters.

MESSAGE DISCIPLINE WORD
GPCC

COMPARE INFORMATION



COMPARE INFORMATION



WORDS 2 & 3 ARE RELATED IN THE SAME MANNER AS WORD 1, THEY EXPAND THE COMPARABLE CHARACTERS TO A TOTAL OF SIX.

MDW (Word Ø) CONTROL INFORMATION

F - defined for output. If F = 1, NN of MDW must be Ø, the character $C_Ø$ is inserted into the data stream. BCW control field not modified.

NN - indicate the number of words of compare character as Ø1, 2, or 3. If NN = ØØ no comparison for a match can be made.

JJ = jump control used in conjunction with NN.

QQ - specify which list will be used to store a CIW (format 1).

bit 14 - must be Ø.

$I_Ø$ = 1, results in generation of an interrupt request and the storing of a CIW (format 1) whenever the $X_Ø$ field of MDW replaces X-field of BCW.

I-bits: if 'F' = Ø (MDW) control the generation of an interrupt request and storing of CIW (format 1) when one of the X_n fields of MDW replaces the X-field of BCW (on a match).

M-bits: if 'F' = Ø of MDW, enables the blocking from storage of an input character when one of the X_n fields of MDW replace X-field of BCW (on a match). Modification of BCW control field is also blocked.

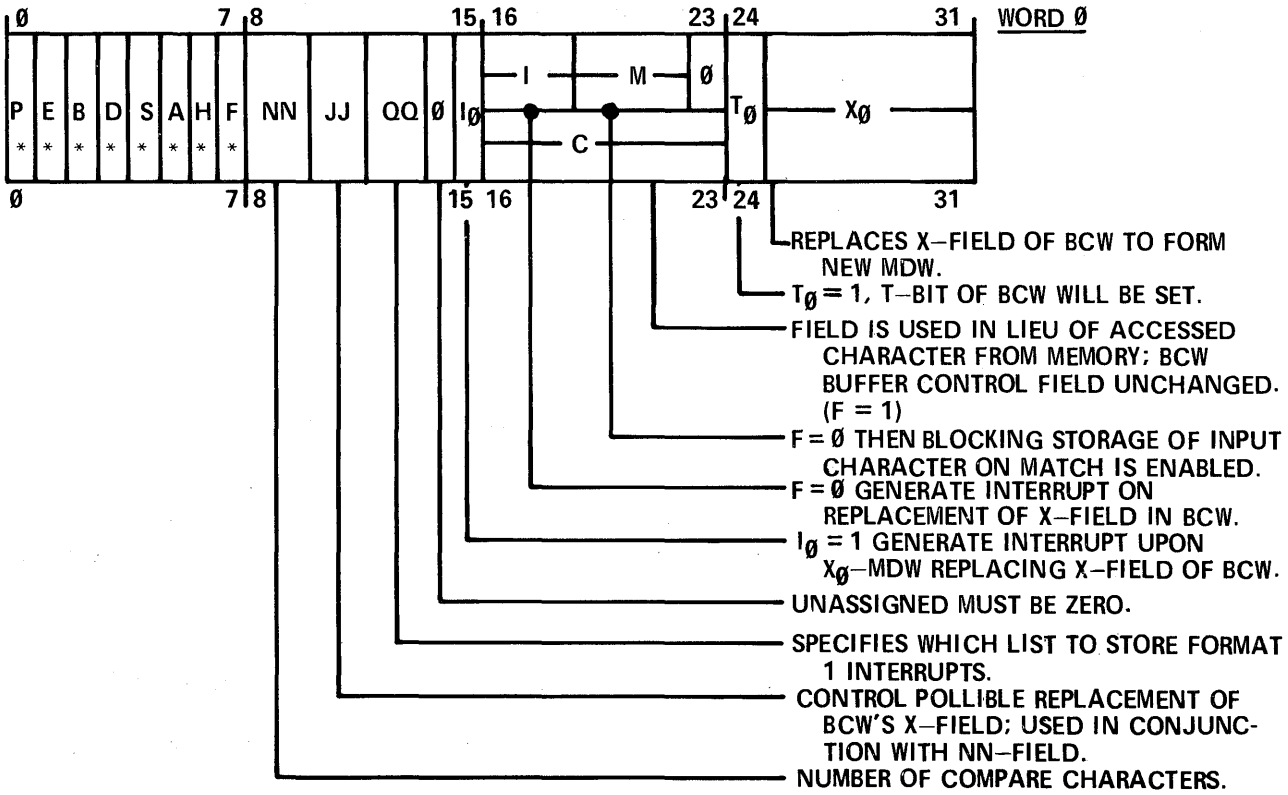
Bit 23 - must be zero.

$C_Ø$ - If 'F' = 1 of MDW, form a character which is transferred to a CLT and used in lieu of accessing a character from storage. The character in $C_Ø$ must be right justified. BCW control field is not modified. $C_Ø$ defined only for output.

$T_Ø$ = 1, sets T of BCW (resulting in termination of $X_Ø$ field of MDW replaces 'X' of BCW).

$X_Ø$ - used to replace the X-field of BCW (forms MDW address). May contain a jump address to the same or another MDW. When this transfer occurs, the GPCC hardware examines bits '$I_Ø$' and '$T_Ø$' to ascertain if a CIW should be stored or if a termination should occur, respectively.

MESSAGE DISCIPLINE WORD
GPCC



*NEXT FOIL

MDW (Word Ø)

P = 1, generate parity on output or test for parity on input.

E = Ø, odd parity, E = 1, even parity. Has no effect unless P = 1.

B = used for input only, B = 1 and NN = ØØ, or NN ≠ Ø and a match does not occur, the input character is not stored in storage and buffer control field of BCW is not modified. If NN ≠ Ø and a match occurs, the B bit has no effect.

D - function is dependent upon the direction of the data flow.
On output is mutually exclusive with code conversion. If D = 1, all characters on which a match occurs will be duplicated. In this case M (of BCW) is used as a binary counter. If M = Ø, the character is transferred, BCW control field is <u>not modified</u> and M is set to 1. If M = 1 the (same) character is again transferred, BCW control field modified and M reset to Ø. When D = 1, M = Ø, the replacement of X-field of the BCW is inhibited thus delaying the selection of a new MDW until the character duplication has been completed. The effect of the associated I-bits selection and T_n bit in the MDW also delayed, i.e., the interrupt request and/or termination, if specified, will be generated on the service request when the character is transmitted for a second time. This use is primarily intended for applications such as transparent text for instance when certain control characters are normally duplicated.
On input if D = 1, BCW-word 2 is to be used if a match <u>does not</u> occur. In addition an interrupt request is generated and a CIW (format 1) is stored. The data address stored in the CIW is that of the character that failed to match. Use is primarily intended to enable the recognition and partitioning of unplanned for, or unexpected characters within a control sequence (also if more than 6 possibilities, maximum allowable number of MDW control characters, exist within some control sequence.)

S = 1, causes BCW-word 2 to be used rather than word 1 and 3. Overrides H-bit of BCW-word Ø.

A = 1, causes 'U' of BCW to be set. If A = Ø, 'U' is reset to Ø. 'U' is used to determine if XF (format 4) may be executed. A and U = Ø designates, on output, that a sequence is now in progress which may not be interrupted for the purpose of embedding a message.

H = 1, sets 'D' of BCW designating input. Also resets 'F' of BCW clearing the indication of a previous parity error from the BCW. The GPCC signals terminate to the CLT via the T-bit line although the 'T' bit of BCW will not be set. This has the effect of switching a half-duplex CLT from output to input. Use of 'H' bit enables very rapid switching which is desirable in situation such as when a fast response to a poll may be expected. The action taken by the GPCC does not affect the handling of data on the current service request when H = 1.

MESSAGE DISCIPLINE WORD
GPCC

WORD Ø CONTINUED

P GENERATE/TEST PARITY.

E CONTROLS ODD OR EVEN PARITY; 0 – ODD, 1 – EVEN.

B BLOCKS STORAGE OF INPUT CHARACTER WHEN SET TO 1 AND NN EQUALS ZERO OR NN DOES NOT EQUAL ZERO BUT NO MATCH OCCURS.

D ON OUTPUT IF MATCH OCCURS CHARACTER IS DUPLICATED, NO MODIFICATION OF BCW IF M–BCW = 0. D MUST BE SET.

ON INPUT IF D = 1, NO MATCH OCCURS THEN BCW WORD 2 WILL BE USED.

S WHEN SET CAUSES BCW WORD 2 TO BE USED.

A CAUSES THE SETTING OR CLEARING OF U–FIELD BCW.

H IF SET TO 1 WILL SET D–FIELD BCW TO 1, ALSO CLEARS F–FIELD BCW MAY BE USED TO SWITCH MODES OF CLT.

I-FIELD

The I-bits (bits 16-18) of the MDW, control the generation of an interrupt request and the storing of the CIW (format 1), when one of the X-fields of the MDW replaces the X-field of the BCW as a result of a character match. Refer to the C/SP Processor and Storage Manual (UP-7866) Appendix B for explanation of this table.

I—FIELD

VALUE OF I → / CHARACTER COMPARE ↓	0	01	02	03	04	05	06	07
C1							X	X
C2						X	X	X
C3					X	X	X	X
C4				X	X	X	X	X
C5			X	X	X	X	X	X
C6		X	X	X	X	X	X	X

INTERRUPT, IF SET ON MATCH, AND $X_{\emptyset}$ REPLACES THE X—FIELD IN BCW

M-FIELD

The M-bits (bits 19-22) of the MDW, permits an input character to be blocked from storage when one of the X-fields of the MDW replace the X-field of the BCW on a character match. Modification of the BCW is also blocked. Refer to the C/SP Processor and Storage Manual (UP-7866), Appendix B, for explanation of this table.

M—FIELD

CHARACTER COMPARE → / VALUE OF M ↓	C1	C2	C3	C4	C5	C6
00						
1						X
2	X					
3	X					X
4	X	X				
5					X	X
6	X	X	X			
7		X	X	X		
8			X	X	X	
9				X	X	X
A	X	X	X	X		
B		X	X	X	X	
C			X	X	X	X
D	X	X	X	X	X	
E		X	X	X	X	X
F	X	X	X	X	X	X

*DELETE FROM STORE ON MATCH, BCW NOT INCREMENTED

NN/JJ FIELD

The 'NN'bits (bits 8-9) of the MDW indicate the number of words of compare characters.

The 'JJ' bits (bits 1Ø-11) of the MDW control the possible replacement of the X-field of the BCW with the X-fields of the MDW. In conjunction with the 'NN' bits and other variables, these bits determine whether or not a jump address is transferred from the MDW to the BCW during a service request sequence. Refer to the C/SP Processor and Storage Manual (UP-7866) for further explanation.

NN/JJ FIELD

N N	J J	NO CHANGE	REPLACE WITH $X_{\emptyset}$ FIELD OF MDW WORD $\emptyset$	REPLACE WITH X_N FIELD OF MDW WORD 1, 2 OR 3 (5)
$\emptyset$ $\emptyset$	$\emptyset$ $\emptyset$	INPUT (2)	(1)	
$\emptyset$ $\emptyset$	$\emptyset$ $\emptyset$	OUTPUT AND DATA BIT $\emptyset$ = $\emptyset$	OUTPUT AND DATA BIT $\emptyset$ = 1	
$\emptyset$ $\emptyset$	$\emptyset$ 1		UNCONDITIONAL	
$\emptyset$ $\emptyset$	1 $\emptyset$	L $\neq \emptyset$ (3)	L = $\emptyset$	
$\emptyset$ $\emptyset$	1 1		UNCONDITIONAL	
$\emptyset$ $\emptyset$	$\emptyset$ $\emptyset$	NO MATCH		MATCH (4)
$\emptyset$ $\emptyset$	$\emptyset$ 1		NO MATCH	MATCH
$\emptyset$ $\emptyset$	1 $\emptyset$	NO MATCH AND L $\neq \emptyset$	NO MATCH AND L = $\emptyset$	MATCH
$\emptyset$ $\emptyset$	1 1		NO MATCH	MATCH

NOTES:

1. BLANK TABLE POSITIONS INDICATE OPERATIONS CANNOT OCCUR FOR GIVEN VALUES OF NN AND JJ.
2. DATA BIT $\emptyset$ IS THE MOST SIGNIFICANT BIT OF OUTPUT BYTE FETCHED FROM STORAGE WHICH MAY BE USED AS A FLAG TO SELECT A NEW MDW IN TRANSMISSIONS WHEN THE CHARACTER LENGTH IS LESS THAN 8. $X \leftarrow X_{\emptyset}$ INHIBITED WHEN PARITY ERROR IS DETECTED ON FETCH OF DATA.
3. L IS CURRENT BUFFER LENGTH.
4. MATCH DENOTES SUCCESSFUL COMPARISON BETWEEN DATA AND COMPARE CHARACTERS IN CURRENT MDW.
5. REPLACEMENT $X_N \rightarrow X$ ON MATCH INHIBITED WHEN K (BCW) = $\emptyset$, M (BCW) = $\emptyset$ AND D (MDW) = 1. UNDER THIS CONDITION AN OUTPUT CHARACTER IS BEING DUPLICATED. THE REPLACEMENT OF $X_N \rightarrow X$ ALSO INHIBITED; THAT IS, A NO MATCH IS FORCED ON OUTPUT WHEN A PARITY ERROR IS INDICATED ON FETCH OF DATA FROM STORAGE.

CIW LIST CONTROL

Communication Interrupt Word (CIW)

While progressing through a given line discipline procedure occurance of various events may require program intervention. Example: buffer segment reassignment and transmission line malfunctions. To handle these events, the system automatically stores information about the situation, notifies the program by means of an I/O A class interrupt request, and continues operation. The program can process the interrupt information at its convenience without causing any impact to normal data flow. The interrupt information is stored as a CIW. One word of interrupt information is stored in a 256 word area of storage for each interrupt request generated. The 256 word area may be allocated in 1, 2, 3 or 4 lists (Ø-3). The lists do not actually assign priority to the interrupt. The order of processing is left to the program.

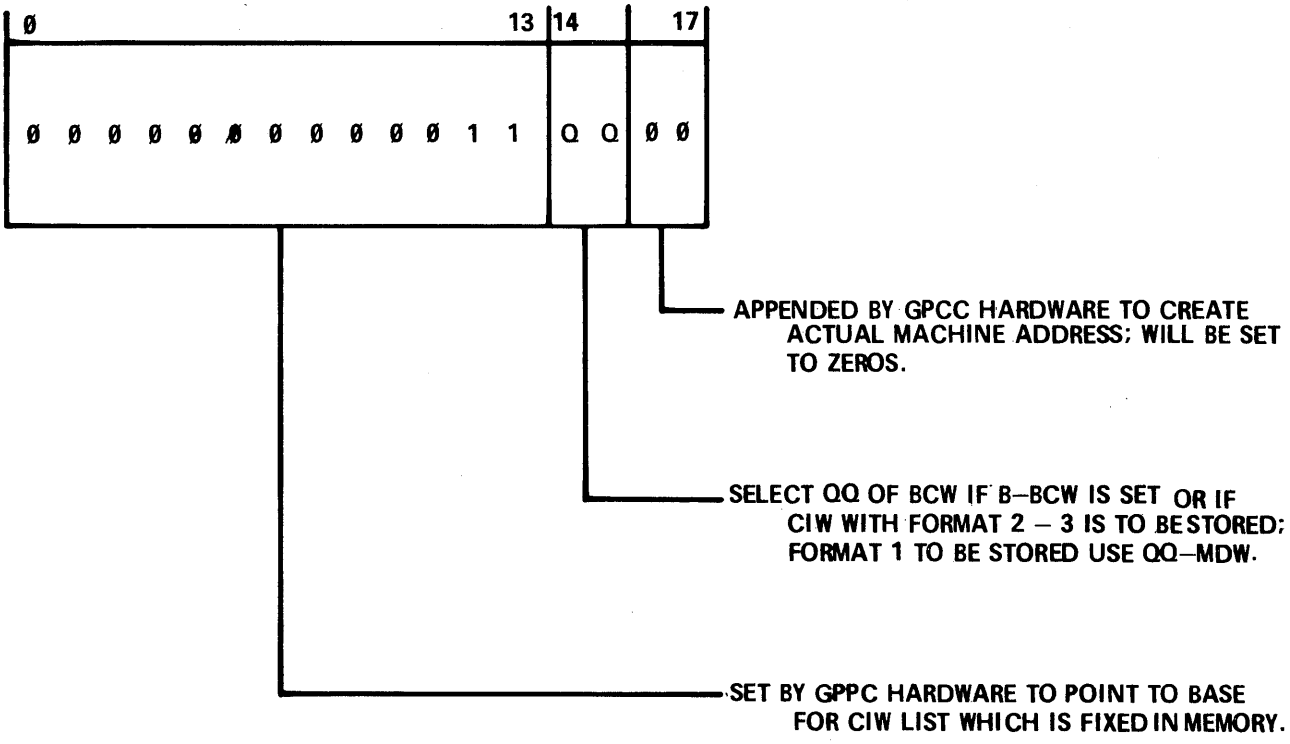
CIW List Control Words:

bits 1-13 = supplied by GPCC hardware and select base $3Ø_{16}$

bits 14, 15 - QQ = selected from

1. BCW if 'B' of BCW = 1 or if a CIW (format 2 or 3) is to be stored.
2. MDW if CIW of format 1 is to be stored.
3. An SIO instruction if issued to GPCC with CAW of format 5, then QQ bits of CQW used to select list that the CIW of format 3 is written into.
4. Condition when CIW of format 3 is to be an error which will set either A = 1 or C = 1 in the format 3 CIW. The value is forced (of QQ) to 11_2 regardless of the value of QQ in BCW.

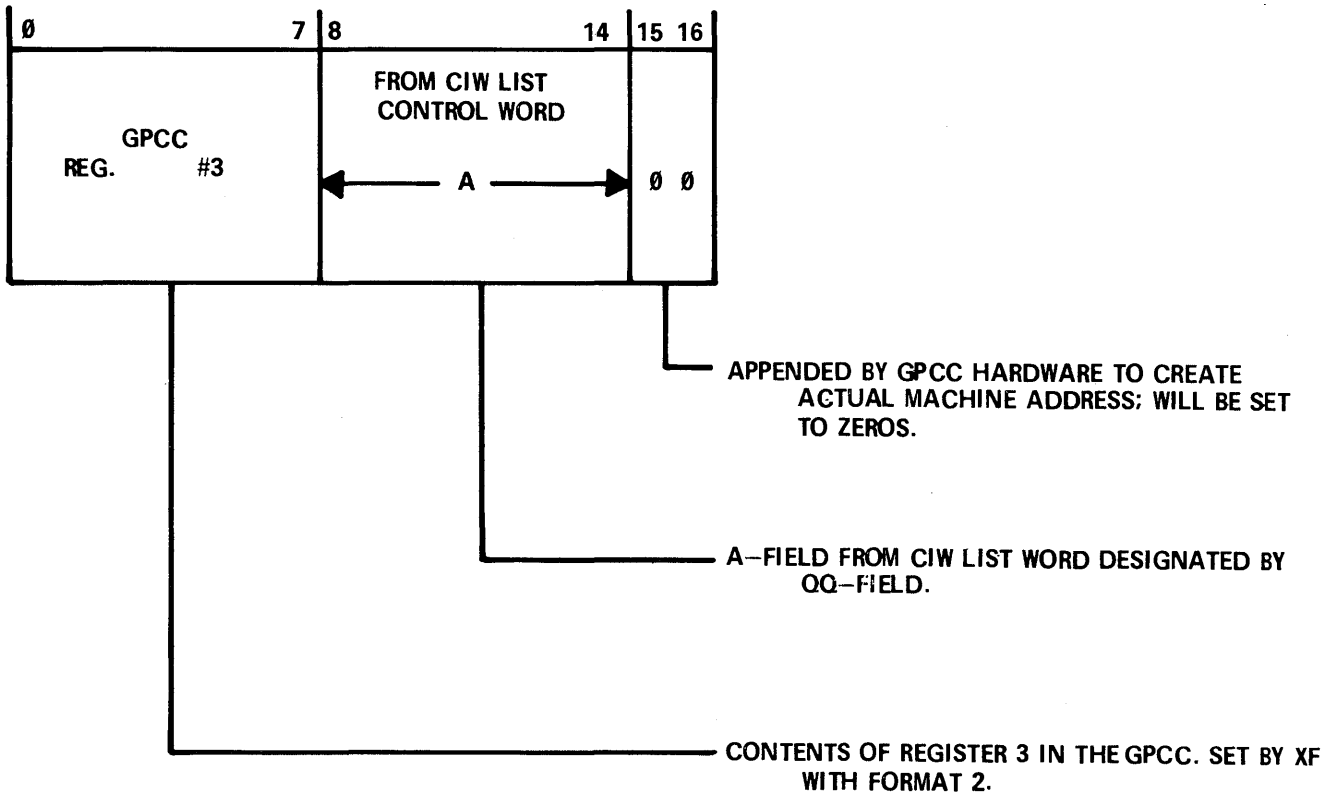
COMMUNICATION INTERRUPT WORD LIST CONTROL GPCC



CIW ADDRESS

The CIW Address is derived:
GPCC register 3 is set by an External Function (XF) of CAW format 2.
The 'A' field is from the CIW List Control Word designated by the QQ-bits.

COMMUNICATION INTERRUPT WORD ADDRESS GPCC



LIST CONTROL WORD

Each CIW List Control Word exercises control over one of the four possible CIW Lists.

A-field: the storage location in which the next CIW will be placed.

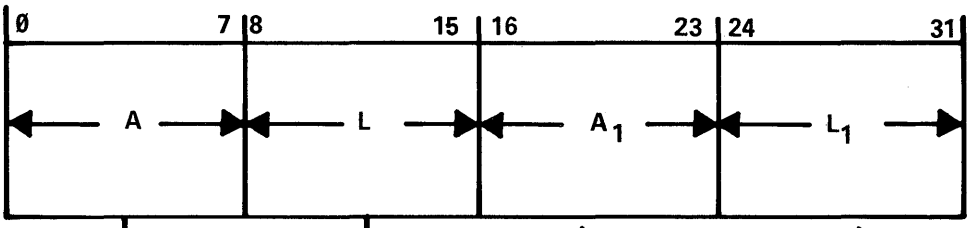
L-field: the number of locations remaining to end of that CIW list.

A_1-field: defines the first location of the CIW list.

L_1-field: initial length of CIW list.

Each time a CIW List Control Word is used 'A' is incremented and 'L' is decremented by GPCC hardware. When 'L' is stepped to Ø the 'A_1' & 'L_1' fields replace 'A' & 'L', (Done by hardware). A violation bit (CIW bit 1) prevents overwriting a CIW when wrap-around occurs. 'A_1' & 'L_1' are never modified by the hardware.

LIST CONTROL WORD
GPCC



WHEN THE L–FIELD OF THIS WORD IS DECREMENTED TO ZERO THE BITS 16 THRU 31 REPLACE BITS Ø THRU 15; NO HARDWARE MODIFICATION IS DONE ON A_1 OR L_1 .

DEFINES THE NUMBER OF LOCATIONS REMAINING TO THE END OF THIS CIW LIST; THIS FIELD IS DECREMENTED BY 1 AFTER A INTERRUPT WORD IS STORED.

DEFINES THE STORAGE LOCATION (IN PART) WHERE THE NEXT INTERRUPT WORD WILL BE STORED; THIS VALUE IS INCREMENTED BY 1 AFTER EACH STORAGE.

GPCC CHANNEL INTERRUPT WORD (CIW)

Three formats are used in the storing of CIW's.

Format 1: Is used for all CIW's which are generated under MDW control.

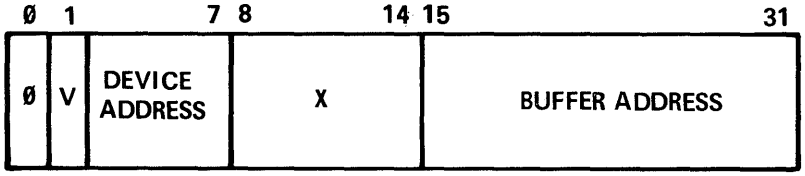
Format 2: Used whenever the only condition for generating an interrupt request, and storing a CIW, is CLT status of 1000_2.

Format 3: Used whenever detailed status from the GPCC or from a CLT is to be presented.

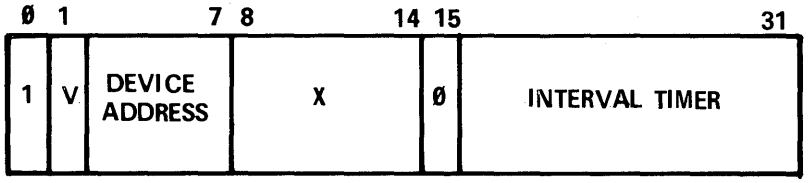
The formats are distinguished by bits Ø and 15. Format 1 has bit Ø set to Ø. Formats 2 and 3 have bit Ø set to 1 and bit 15 set to Ø and 1 respectively.

GPCC CHANNEL INTERRUPT WORD (CIW)

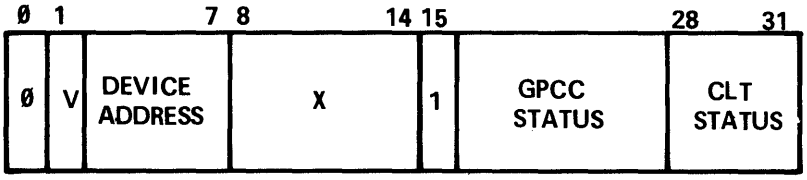
CIW FORMAT 1 – ALL CIW'S GENERATED UNDER MDW CONTROL



CIW FORMAT 2 WHEN CLT STATUS EQUALS 1000_2



CIW FORMAT 3 – DETAILED STATUS FROM GPCC OR CLT



CIW FORMAT 1

CIW - format 1: used for all CIW's generated under MDW control when:

1. I of MDW = 1 & X of MDW replaces X-field of BCW.
2. I-field of MDW decodes I = 1, & X_N of MDW replaces X-field of BCW.
3. 'D' of MDW = 1 on input and a match has not occurred.

Bit Ø - identifies format 1 (Ø)

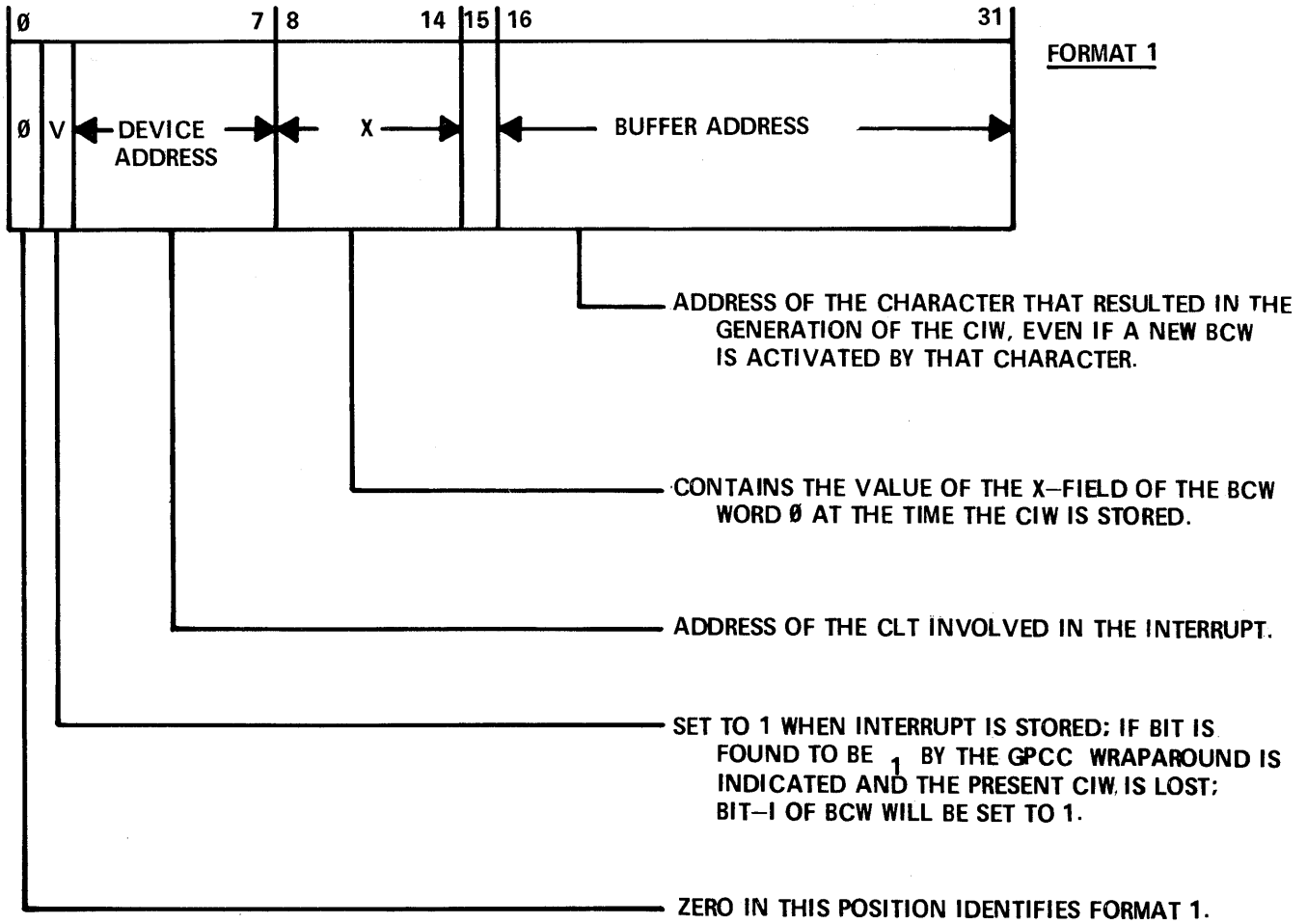
V - violation bit, to prevent the current interrupt word from being stored at the same location as an earlier one. Set to 1 by program after the interrupt is handled. If V = Ø on wrap around, the 'I' of BCW is set and the current CIW is lost.

Device Address - Address of CLT (Multiplexer position number) involved in the interrupt.

X-field - The same as X-field of BCW word Ø at the end of the sequence in which the CIW is stored. This address is used to obtain the next MDW to continue the data communication procedure.

Buffer Address - Same as buffer address in the current BCW now being used by the GPCC. The address is stored prior to incrementation so it points to the character that resulted in the generation of the CIW. This is true even if a new buffer control field is activated by that character (then a second CIW of format 3 is stored to indicate that condition).

COMMUNICATION INTERRUPT WORD
GPCC



CIW FORMAT 2

CIW - format 2: Used whenever the only condition for generating an interrupt request and storing a CIW is CLT status = $1\emptyset\emptyset\emptyset_2$. This status corresponds to the situation where an asynchronous CLT has detected a space to mark transition, it will again present $1\emptyset\emptyset\emptyset_2$ status generating an interrupt request and storing another CIW of format 2. These CIW's enable recognition of break, disconnect and error conditions on synchronous lines. $1\emptyset\emptyset\emptyset_2$ status is also generated by the Dialer CLT to indicate the automatic calling unit has switched the communication line back to the data set after having detected an answer from the called station.

Bit $\emptyset$ = 1 - identifier for format 2 if a $\emptyset$ is in bit 15 position.

V = violation bit (same as format 1)

Device address same as format 1

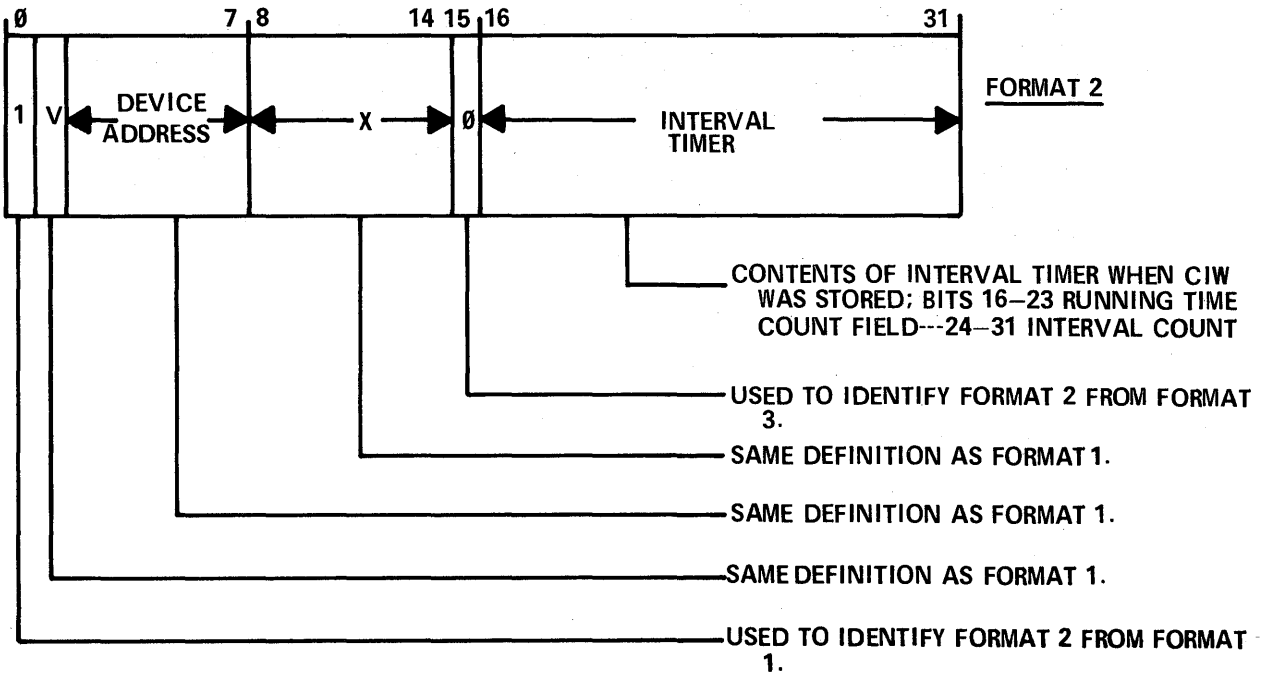
X field - same as format 1

Bit 15 = $\emptyset$, and a '1' in bit $\emptyset$ identify format 2

Interval timer = contains bits 16-31 of the interval timer word as it appeared when the CIW was stored. Bits 16-23 are the 'R' field and bits 24-31 are the count field of ITW.

Note: If parity error occurs on the fetch of the ITW during an attempt to store CIW format 2, a CIW format 3 is stored instead.

COMMUNICATION INTERRUPT WORD
GPCC



CIW FORMAT 3

CIW - Format 3: used whenever detailed status from the GPCC or CLT is to be presented.

1. GPCC defects error condition as parity, or buffer wrap around.
2. CLT presents status to the GPCC which in turn stores a CIW. including that status. ($1ØØØ_2$ status excluded since it uses format 2). One exception, where CLT status of $1ØØØ_2$ is stored in CIW of format 3.

3. 'H' of BCW has toggled from 1 to Ø or Ø to 1 indicating a completed buffer.
4. An XF of format 4 has <u>not</u> been executed by the GPCC.
5. An XF of format 5 has been executed by GPCC.

Bit Ø = A '1' in this position and a '1' in bit 15 identifies format 3.

X-field = same as format 1. Meaningless in some CIW's of format 3 as when error conditions bits 'A' or 'C' are set or when an XF of format 5 is executed which stores the 'P' and 'T' bits in the CIW.

H = 1 if BCW has toggled, indicating buffer has been exhausted.

R = 1, indicates XF (format 4) has not been executed due to 'U' of BCW being Ø or 'M' of BCW = 1.

Bits 18 - 20: not used, set to Ø by GPCC hardware.

P - An XF (format 5 is executed by GPCC which places 'P' of CAW into this position of CIW and stores the CIW (format 3).
T - XF (format 5) is executed by GPCC which places 'T' of CAW in this position and stores CIW format 3.
W - If = 1, indicates GPCC has accessed a buffer control field whose V bit = 1. If this condition occurs on output the 'T' of BCW is also set.

See Appendix B for more information.

Bit 24 - set to Ø by GPCC hardware (not used).

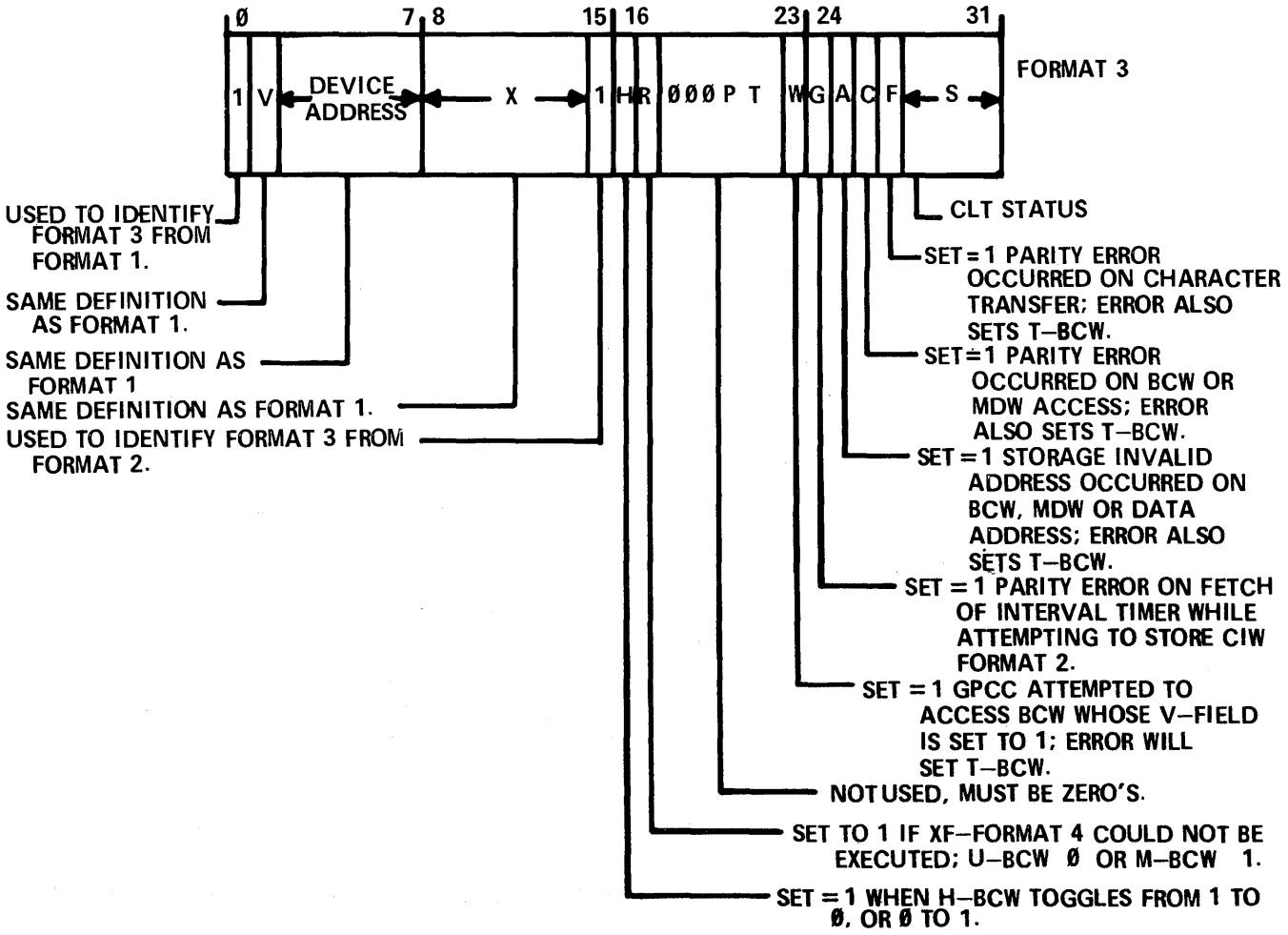
A - If = 1, indicates a storage invalid address has occurred on a BCW, MDW or data address. This error also sets 'T' of BCW and QQ bits are forced to 11_2.

C - If = 1, indicates parity error on BCW or an MDW access. Sets 'T' of BCW and forces QQ bits to 11_2.

F - If = 1, indicates parity error on access of output data character from storage or input character from the communication line. Error also sets 'F' of BCW.

S - contains CLT status. The GPCC accepts and stores CLT status in unmodified form, with exception of $1ØØØ_2$, (results in CIW format 2).

COMMUNICATION INTERRUPT WORD
GPCC



Communication Line Terminal (CLT): A CLT generally performs 3 functions;

1. Contains the interface circuitry and control circuitry to match the characteristics of a communication line facility.
2. Contains the input and output buffer registers to assemble and disassemble bit serial information from and to a communication line facility (least significant bit first).
3. Contains the necessary control and interface circuitry to request service and transmit data and control to, and receive data and control from, the multiplexer.

Two broad classes of CLT's: asynchronous and synchronous

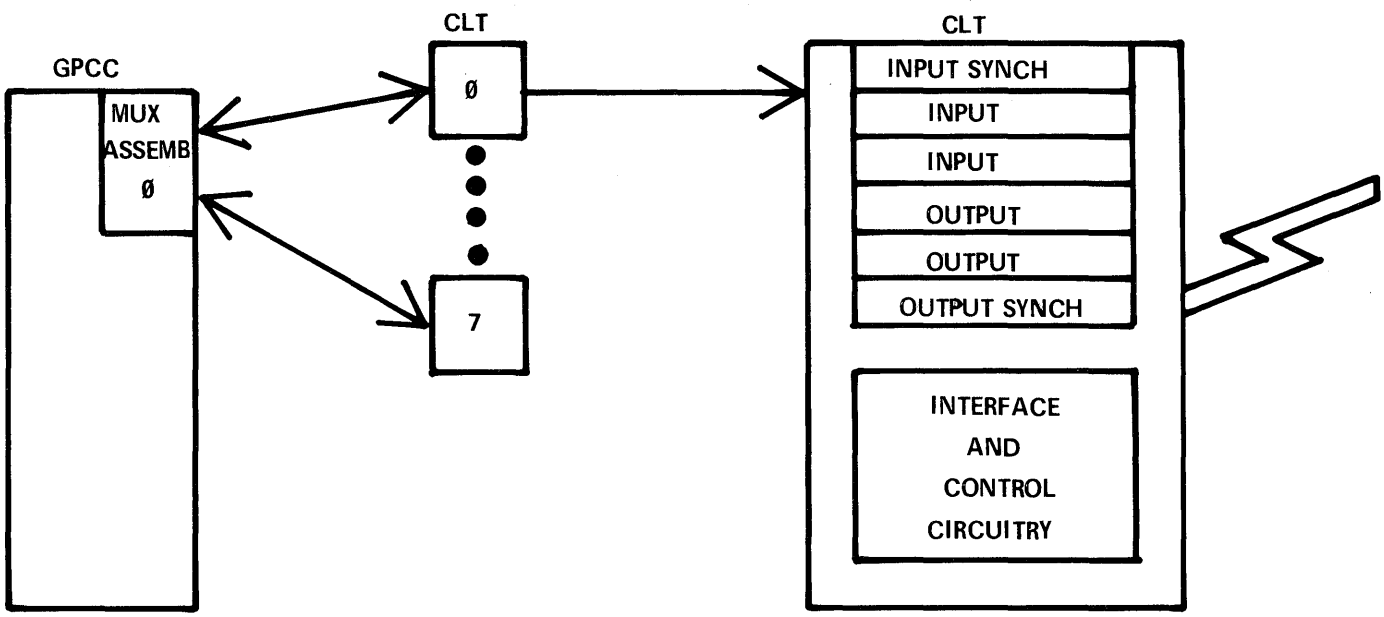
Asynchronous - operates in start/stop mode in which each character is preceeded by a start bit and followed by at least 1 stop bit. Output transmission rate is controlled by a clock located in a timing assembly of GPCC. Generation of a sampling signal for input is derived by the CLT from the same timing assembly as used for output.

Synchronous - derives its transmit and receive clocks from the communication line facility which assumes the responsibility of attaining bit synchronization. The CLT examines the input data stream and obtains character synchronization.

Three communication line facilities are provided by the various CLT's:

1. Data sets conforming to EIA standard RS-232-B, MIL standard 188B, and CCITT Interface Specifications.
2. Direct wire operation over limited distribution.
3. Asynchronous operation on a private line telegraph network.

COMMUNICATION LINE TERMINAL



ASYNCHRONOUS CLT EXTERNAL FUNCTION (XF)

Asynchronous CLT - performs functions of:

1. Request a data character from GPCC.
2. Storing up to 2 such characters.
3. Transmitting a data character to the data set, bit serially, attaching the proper start/stop bits.
4. Assembling bit-serial character after recognition of a start bit.
5. Storing up to 2 input characters.
6. Request GPCC to accept an input character.
7. Manipulating control leads to the data set.
8. Interpreting control signals on control leads from the data set.
9. Performing certain error checking.
10. Presenting CLT status to GPCC.
11. Accepting control commands termed XF from the GPCC.

To perform the above functions the CLT operates under control of parameters specified by the XF's. These parameters specify one or two stop bits on output transmissions, whether the CLT is to operate in half duplex or full duplex mode, whether or not the request to send lead to the data set is turned off when the CLT receives a 'turn off' indication from the GPCC and what code level is to be used by the CLT. The CLT utilizes the following interface leads: Protective ground, transmitted data, received data, request to send, clear to send, data set ready, signal ground, data carrier detected, restraint detected, data terminal ready ring indicator.

External Functions (XF) - The CLT is basically controlled by means of XF's. The controlling program loads the XF into fixed memory location $2C_{16}$ (CAW). Then the program issues a SIO. The GPCC fetches the CAW and forwards 6 bits to the CLT. The CLT is selected by the device address in the SIO instruction. In full duplex mode, the XF's are issued to the CLT using the output device address (even). If the input address is used, no CLT operation is initiated. In half duplex mode, the same device address is used for both input and output. The 6-bits passed to the CLT are selected from the CAW (3-bit F-field and a 3-bit D-field).

LL = code level.
S = number of stop bits to transmit
D & R = Ø, the character(s) stored in the CLT will be transmitted to the line, after which a marking condition is assumed.
D = Ø and R = 1, request to send is dropped immediately.
D = 1 and R = Ø (in front of Data-Terminal-Ready), Data-Terminal-Ready and Request-to-Send signals are dropped, disconnecting the line.
H = Ø, Place CLT in full duplex mode.
C = Ø, Do not drop Request-to-Send signal when turning off output on the CLT.
B = Ø, Stop the forced transmission of space.

ASYNCHRONOUS CLT XF'S

NAME	F–FIELD	D–FIELD	DESCRIPTION
XFØ	ØØØ	LLS	TURN ON OUTPUT
XF1	ØØ1	LLX	TURN ON INPUT
XF2	Ø1Ø	XXM	TURN OFF INPUT
XF3	Ø11	DRX	TURN OFF OUTPUT AND DISCONNECT
XF4	1ØØ	XXX	ENTER TEST MODE
XF5	1Ø1	XXX	DISCONNECT CLT FROM SYSTEM
XF6	11Ø	HCB	MODE SET
XF7	111	XXX	NOT USED

LL = LEVEL

ØØ = 5 LEVEL

Ø1 = 6 LEVEL

1Ø = 7 LEVEL

11 = 8 LEVEL

S = NUMBER OF STOP BITS

Ø = TRANSMIT TWO STOP BITS

1 = TRANSMIT ONE STOP BIT

H = Ø PLACE CLT IN FULL DUPLEX MODE.

H = 1 PLACE CLE IN HALF DUPLEX MODE.

C = Ø DO NOT DROP REQUEST TO SEND WHEN TURNING OFF OUTPUT ON CLT.

C = 1 DROP REQUEST TO SEND WHEN TURNING OFF CLT.

B = Ø STOP THE FORCED TRANSMISSION OF SPACE.

B = 1 START THE FORCED TRANSMISSION OF SPACE.

D = Ø, R = Ø CHARACTER(S) STORED IN THE CLT WILL BE TRANSMITTED TO LINE AFTER WHICH A MARKING CONDITION IS ASSUMED.

D = Ø,1 R = Ø,1 DATA TERMINAL READY AND REQUEST TO SEND DROPPED; DISCONNECTING LINE.

X – MUST BE ZEROS

SYNCHRONOUS CLT XF

Synchronous CLT - performs functions of:

1. Request data character from GPCC.
2. Storing up to 2 such characters.
3. Transmitting a data character to the data set (bit-serially).
4. Storing a synchronous character for input and output.
5. Assembling a bit-serially presented character after establishing character synchronization.
6. Storing up to 2 input characters.
7. Request GPCC to accept an input character.
8. Manipulating the control leads to the data set.
9. Interpreting control signals on control leads from the data set.
10. Performing certain error checking.
11. Presenting CLT status to the GPCC.
12. Accepting control commands termed XF from the GPCC.

Synchronous CLT controlled basically by means of XF's. The XF is loaded in CAW fixed location, controlling program issues SIO instruction, the GPCC fetches the CAW and forwards 14 bits to the selected CLT. The CLT is selected by the device address in the SIO instruction.

The 14 bits forwarded are selected from the CAW (format 1 type). A 3-bit F-field, 3-bit D-field, and 8-bit S-field.

LL = code level.

SSSSSSSS = The synchronous character to be used during an input-output transmission. Synchronous character is left justified. An S-field of all zeros is not allowed.

The CLT transmits 1 synchronous character and generates service requests to the GPCC as each character buffer (request) in the CLT is freed. The CLT alternates transmission from two output registers. If neither register contains a message character, the CLT transmits the synchronous character stored in its output section and sets the S_3 status bit, (output data overrun).

Input - LLN: N of the F-field specifies whether a new synchronous lead will be pulsed. This lead is used to reduce synchronization time when the input section of CLT is switched from one transmitter to another on a multi-party communication line.

SYNCHRONOUS CLT XF

NAME	F–FIELD	D–FIELD	S–FIELD	DESCRIPTION
XFØ	ØØØ	LLX	SSSSSSSS	TURN ON OUTPUT
XF1	ØØ1	LLN	SSSSSSSS	TURN ON INPUT
XF2	Ø1Ø	XXM		TURN OFF INPUT
XF3	Ø11	DRX		TURN OFF OUTPUT
XF4	1ØØ	XXX		ENTER TEST MADE
XF5	1Ø1	XXX		DISCONNECT CLT
XF6	11Ø	HCX		MODE SET
XF7	111	XXX		NOT USED

LL = 0 NOT ALLOWED

S–FIELD

6 LEVEL	$S_0\ S_1\ S_2\ S_3\ S_4\ S_5\ 0\ Ø$	SYNCHRONOUS
7 LEVEL	$S_0\ S_1\ S_2\ S_3\ S_4\ S_5\ S_6\ 0$	
8 LEVEL	$S_0\ S_1\ S_2\ S_3\ S_4\ S_5\ S_6\ S_7$	

OTHER SYMBOLS SAME AS ASYNCHRONOUS

ASYNCHRONOUS/SYNCHRONOUS CLT STATUS

Asynchronous CLT Status: 4 status bits ($S_\emptyset$, S_1, S_2, S_3) presented to GPCC by requesting service from the multiplexer. These bits are set to $\emptyset$ when GPCC acknowledges receipt of these bits.

$S_\emptyset$ = communication line is spacing at time of first strobe following the accumulation of a character. The CLT will not input this character. CLT then looks for 'mark' (service request inhibited). Upon detection CLT continues operation.

S_1 = ring indicator goes active and data terminal ready is not active. (presented once/ring - approximately every 6 seconds.)

S_2 = data carrier detector goes from active to inactive.

S_3 = input data overrun occur. Condition where both input registers in the CLT are full and the first bit of a new character is presented by the communication line. At least one character will be lost, but CLT will attempt to assemble the rest of the message.

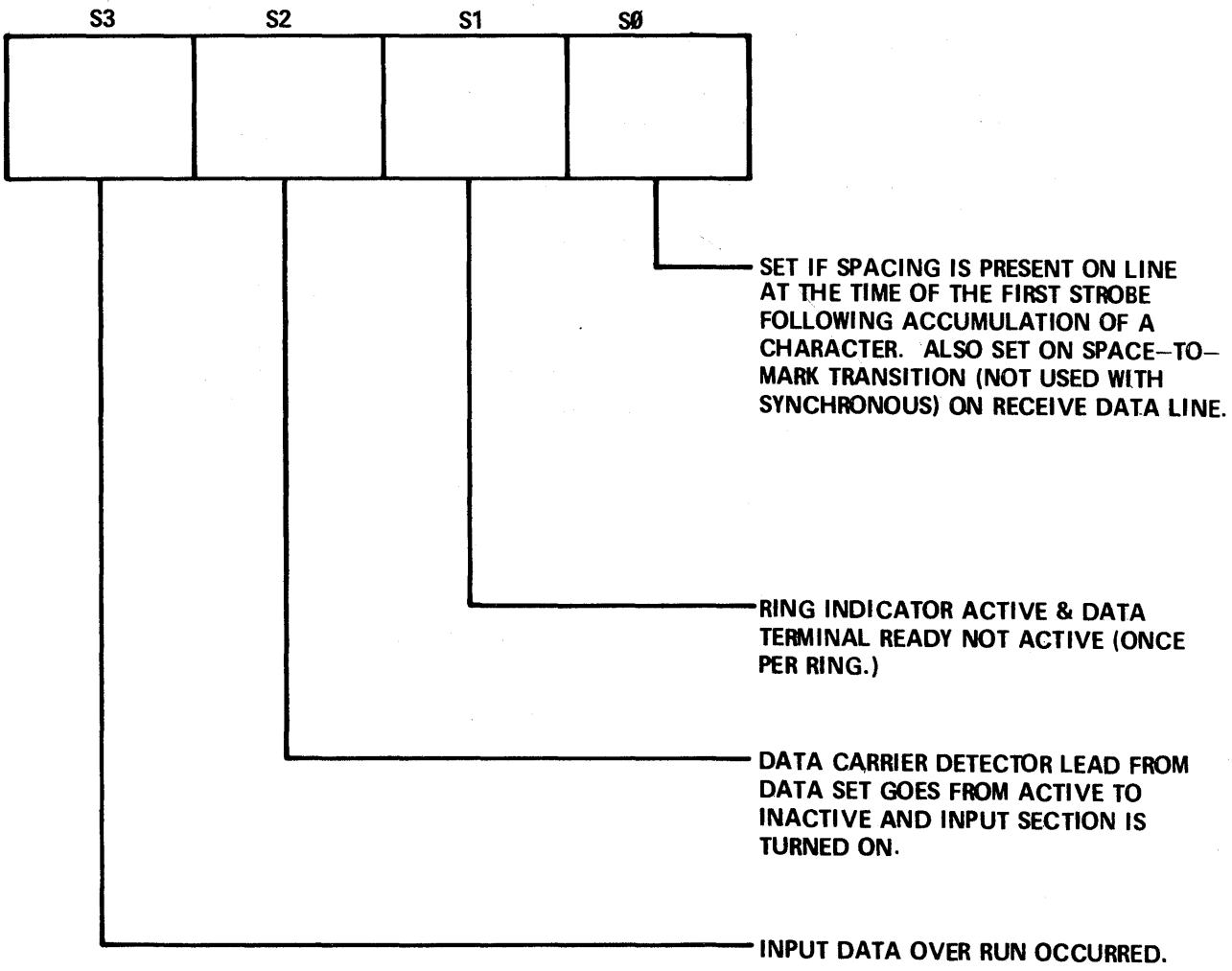
Synchronous CLT Status: 3 status bits - S_1, S_2, S_3 are generated.

S_1 = presented to the GPCC if the ring indicator goes active and data terminal ready is not active.

S_2 = presented to GPCC if the data carrier detector from the data set goes from active to inactive (provided input section is on).

S_3 = if output or input data overrun occurs. (Input-both registers are full, output-both registers are empty and data set wants to input or output the first bit of new character.)

ASYNCHRONOUS/SYNCHRONOUS CLT STATUS

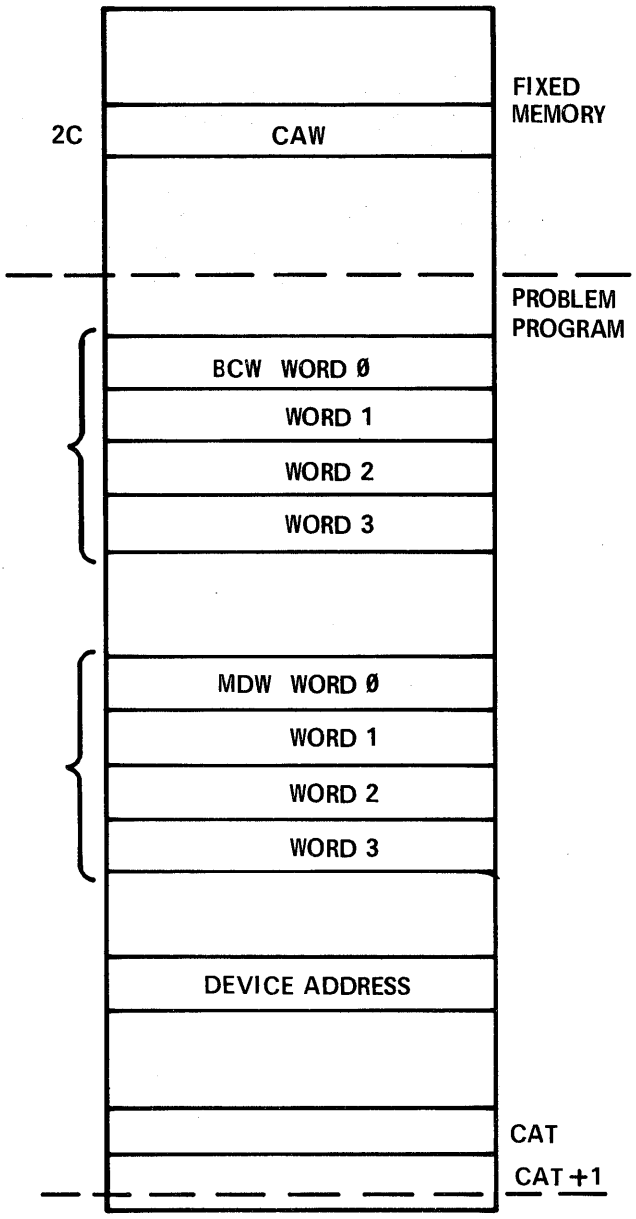


GPCC GENERAL FLOW

This diagram is designed to show the program initializing the base address of the BCW, MDW for the CLT selected by the device address field of the SIO instruction. The BCW is initialized to accept input of 80 bytes (50_{16}) and the address of where the data is to be transferred (CAT) in storage. The BCW contains the pointer to the current MDW, supplementing control of this line. The MDW contains 6 compare characters to be compared to each byte of input data.

GPCC GENERAL FLOW

```
L     R1,CAW2A
ST    R1,,,2C
SIO   START
L     R1,CAW2
ST    R1,,,2C
SIO   START
L     R1,,,2C
SIO   START
```



DEVICE ADDRESS

START: Ø — Ø21

CAW1: Ø | 7 8 | 15 — Ø — Ø26 | 00010000

CAW2: Ø | 7 8 | 15 — BCW | 10 — Ø1

CAW2A: Ø | 7 8 | 15 — MDW | 10 — Ø2

BCW: Ø | 31 — Ø — Ø110 — Ø10 — MDW

Ø	Ø — Ø50	CAT
Ø	Ø	
Ø	Ø	

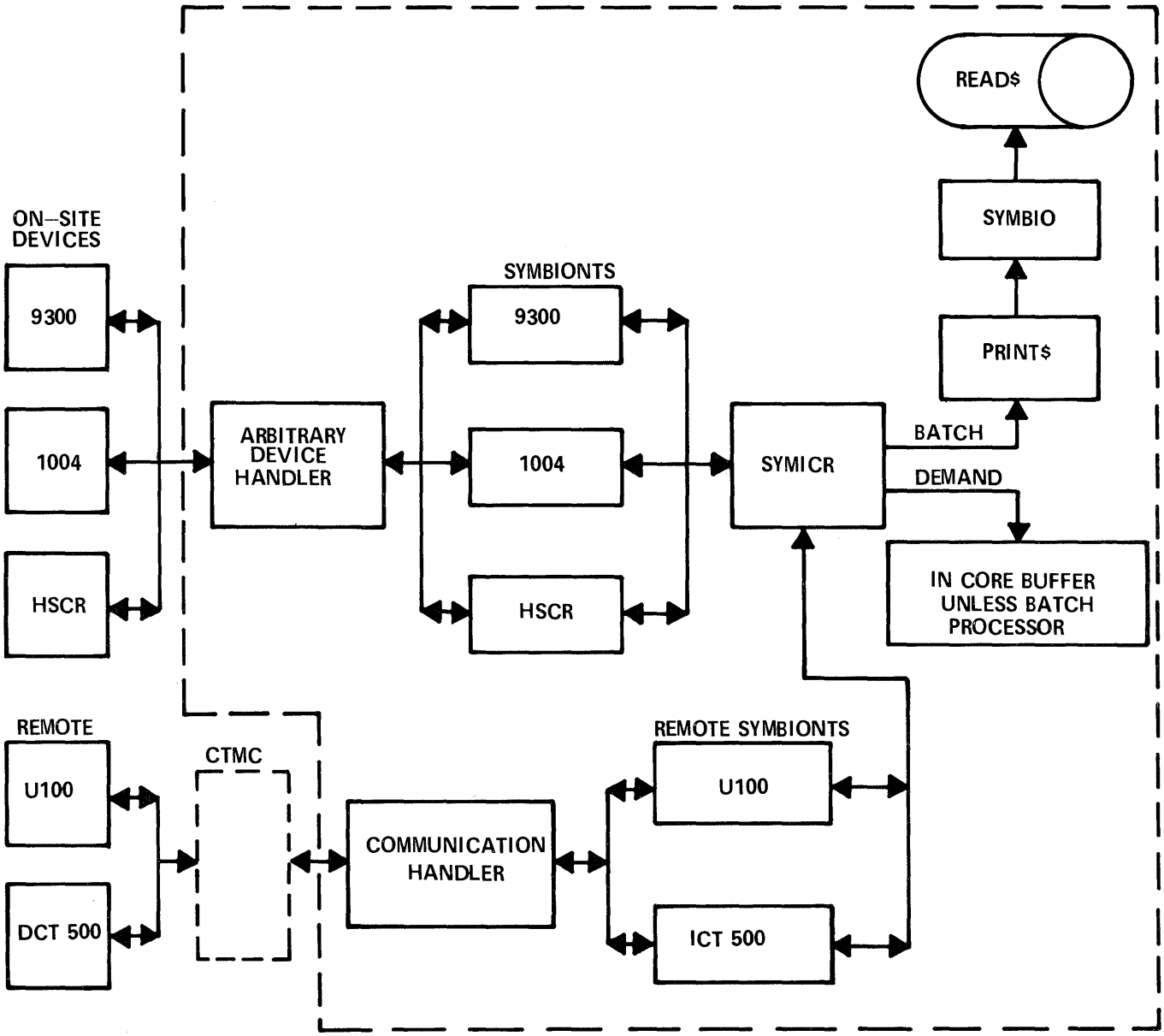
MDW: Ø | 31 — 1010 — Ø10110 — Ø10-01-Ø — Ø

SYN	SYN	T	X_1	T	X_2
SOH	STX	T	X_3	T	X_4
ETX	BP	T	X_5	T	X_6

HOST SYMBIONT/COMMUNICATION BLOCK INPUT

This diagram is designed to show a very basic concept of the on-site and remote handling of peripherals in the 1100 environment.

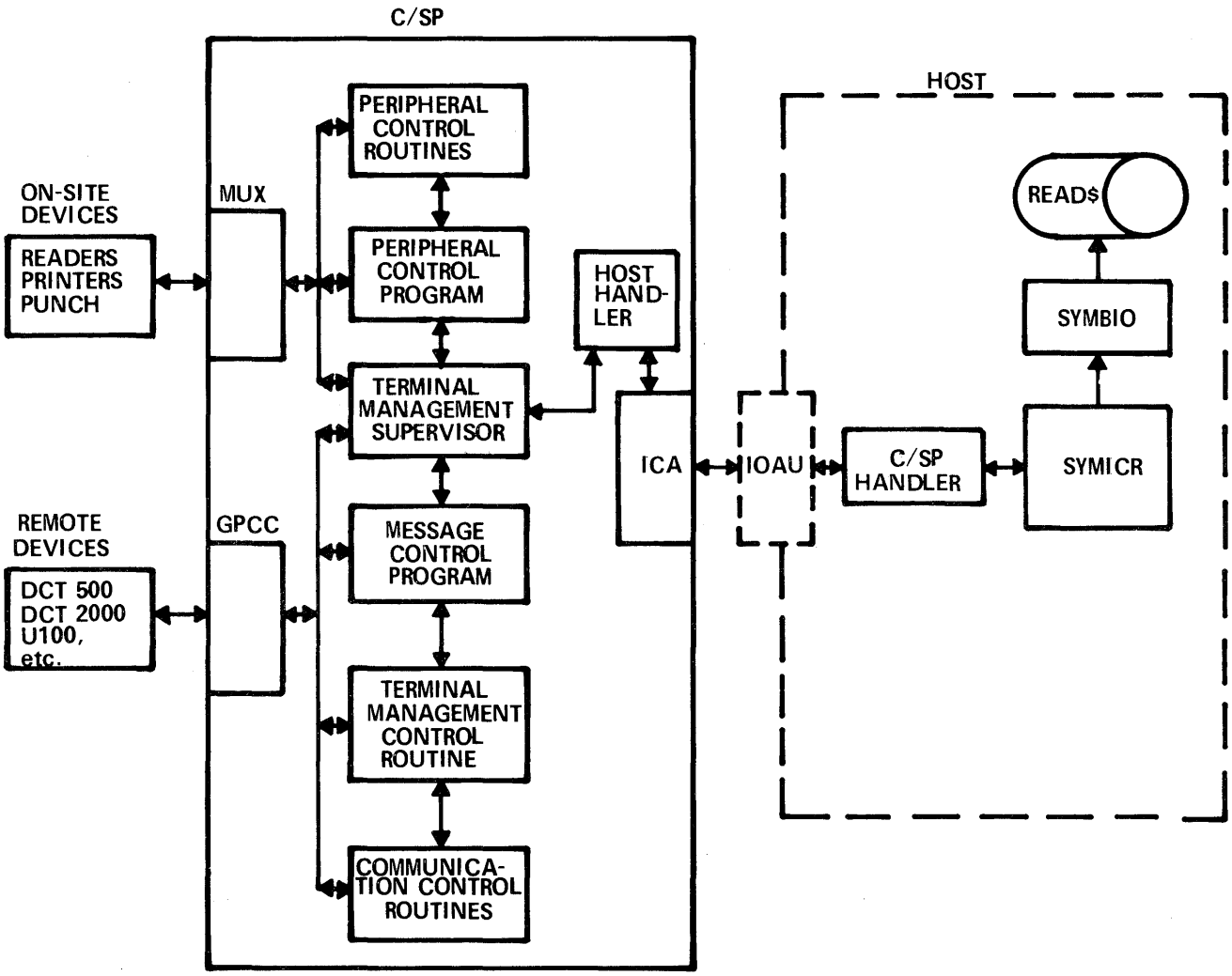
HOST SYMBIONT/COMMUNICATIONS INPUT



C/SP SYMBIONT/COMMUNICATIONS
BLOCK INPUT

Referring to the previous diagram, the C/SP concept relieves the host computer of much of the overhead involved in the handling of on-site and remote peripherals.

SYMBIONT/COMMUNICATIONS INPUT



APPENDIX A

C = 1, Invalid address or parity error during CIW control sequences. Error condition:

1. Invalid address on CIW List Control Word.

2. Parity error in CIW List Control Word.

3. Invalid Address error on CIW.

4. Parity error on CIW. If the error is on ICW, the GPCC executes the normal modification of the address and length fields of CIW List Control Word.

I = 1, CIW has been discarded because the current location in the interrupt list has the 'V' bit set to Ø indicating CIW list is full.

If either the 'C' or 'I' bits have been set in BCW, the GPCC will not generate any interrupt requests involving that BCW until 'C' or 'I' is reset (by controlling program). Service Request may occur, but the rest of the operation involving BCW's are ignored. The controlling program depends on timing out to resolve this situation. No data transfer takes place (i.e., zeros are transmitted to the communications lines).

K & M: When K = 1 and LL = ØØ indicates a 5 level code received or sent and conversion to or from 6-level code in storage is desired.

On input, each character is examined in the GPCC to determine if it is a special symbol. These symbols indicate how to interpret the 5-level code following them (LTRS/FIGS). Code held in GPCC register 25 sets M = 1, code held in register 26 sets M = Ø. Neither of these characters are transferred to storage with 'M' appended as a sixth bit. All other characters appear in a storage byte as ØØMBBBBB (B-bits of character). This permits the programmer to convert to any other code without having to search for embedded special symbols.

On output, bit 2 of each byte transferred from storage is compared with 'M'. If M = Ø and bit 2 = 1, contents of GPCC register 26 is sent to the CLT and M is set to 1. If 'M' = 1 and bit 2 = Ø, contents of GPCC register 25 is sent to the CLT and M is set to Ø. The Buffer Control field is not modified. If M = bit 2, the character from storage is transferred to the CLT and M is left unchanged. On character comparison, the comparison uses the 5-level coming from the CLT on Input. On output the data byte in storage is used (bit 2 appended). When K = 1 and LL = Ø1 a 6-level code is being received or sent and conversion to/from a 7-level code in storage is desired. The code stored in GPCC register 27 has the same effect as the code held in GPCC 25. Likewise GPCC register 28 has the same effect as GPCC register 26. The 'M' bit is appended as bit 1 on input. (MBBBBB), and bit 1 is compared to 'M' on output (otherwise this mode is similar to the 5-level conversion). When K = 1 and LL = 11, parity checking (input) or parity generation (output) is specified, a 6-level code and parity is being received/sent and conversion to/from 7-level is desired. This mode is identical to the 6-level except the special symbol in GPCC register 27 and 28 contains a 7-bit character.

Appendix B.

W = 1, indicates the GPCC has accessed a buffer control field whose V_N = 1. If this condition occurs on output the 'T' of the BCW is also set. On input the violation condition does not cause termination, however, subsequent service requests which occur before the V_N bit is reset, will not store additional CIW's with 'W' set to; nor will the data character be transferred to storage. Other operations in the service request occur normally, as comparison for a match with a character in the MDW. On input, if the GPCC finds V_N = 1, it examines the appropriate buffer length field of BCW. If this field is all zeros, it indicates this is the service request which first detected the violation. Then the CIW is stored and the buffer length field is decremented from all zeros to all ones. Subsequent service requests that find V_N = 1, detect the buffer length field is all ones and inhibits both the generating of a CIW and modifying the buffer length field.

SECTION VI

SOFTWARE OVERVIEW AND MATERIALS

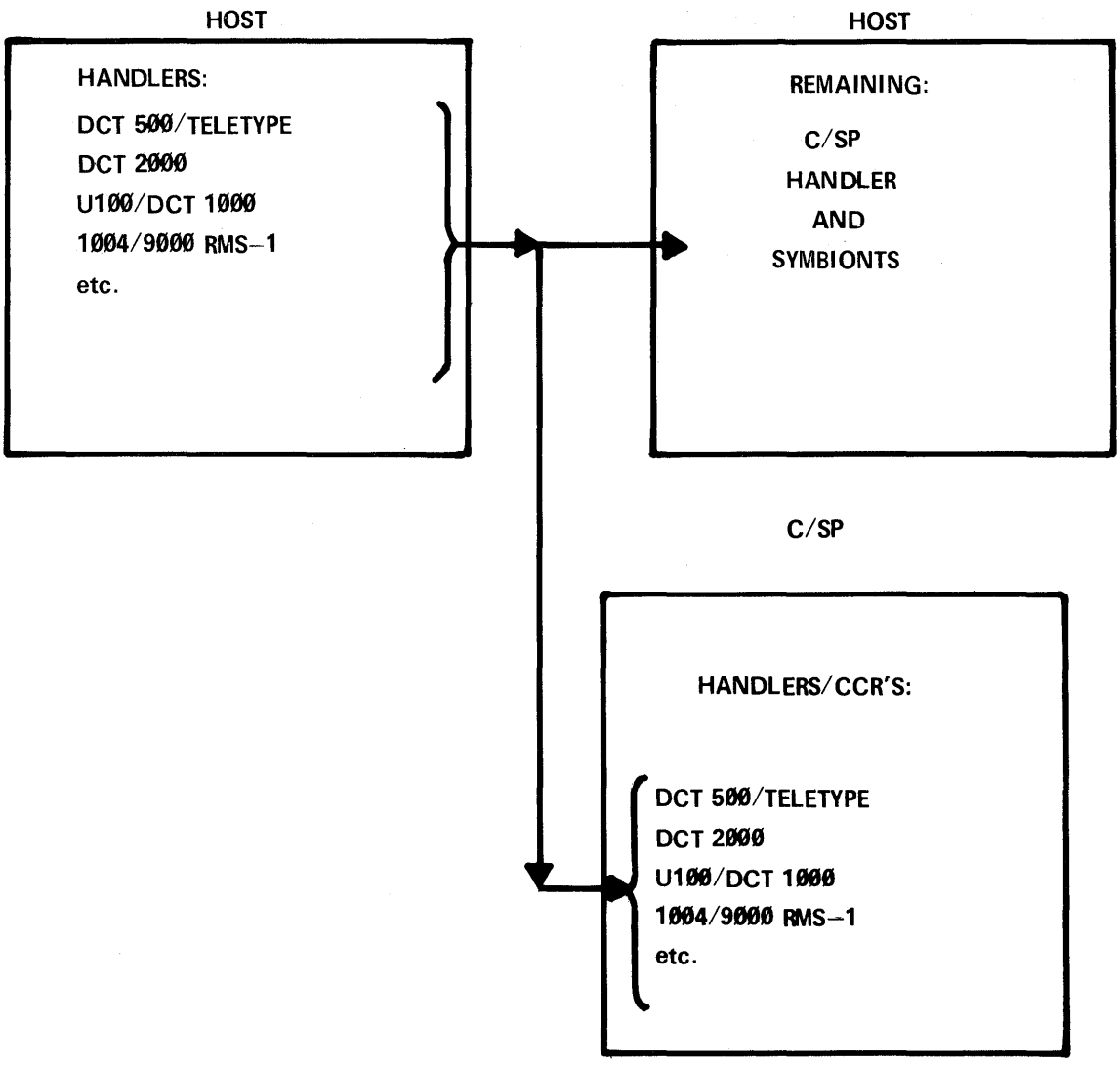
SECTION VI INDEX – SOFTWARE OVERVIEW & MATERIALS

INTRODUCTION TO C/SP SOFTWARE

The software provided on the C/SP is designed to reduce the communications overhead in the Host executive system and the user programs. The C/SP controls the remote communication devices, therefore, core requirements are reduced as the device symbionts/ handlers are not needed in the host computer, minimizing critical timing situations and the interrupts required to gather data or scan for intput. C/SP software also provides a simplified user interface for receiving or sending data to a remote device as the control characters for controlling a device and the standard code conversion is performed by a system message control program element.

Software Elements: written in modular elements to avoid fixed constraints and provide a system easily adjustable to new devices and specialized applications.

INTRODUCTION TO C/SP SOFTWARE



C/SP SOFTWARE IN HOST

Primary impact of the C/SP on the EXEC is the removal of device oriented symbionts and the substitution of a single C/SP symbiont. A C/SP handler is provided to interface the 11ØØ with the C/SP. Operator communication and the initial load function are provided for. Several elements in the EXEC require minor modifications.

C/SP symbiont

The batch/demand function links to the EXEC through SMICR as is currently being done with all input symbionts. The output function links directly to SMUPQ, by passing the stacking of output through SMNXTP. The C/SP stacks output requests under its own stacking shceme because of C/SP control over the output terminals.

1. Input functions - set to handle batch and demand, along with special I/O requests.

2. Output functions - handles output of information from the PRINT and punch files for batch and demand.

3. Remote functions - to allow the remote user access to the Host computer.

C/SP secondary symbionts

1. Program Load - allows the C/SP programs or the Host operator to request a program be found in Host and loaded into C/SP for execution.

2. Console Communications - marking a terminal up/down in the assign table, allowing input/output, to/from the console device.

3. Mass Storage - request access to mass storage file.

4. Logging - logging I/O errors along with other computer malfunctions on the EXEC error log.

C/SP Handler

Consists of those routines in the Host EXEC that are concerned with support of the user interface with C/SP and the control of the Host and C/SP environment. The handler is designed to provide the user with a simple interface with C/SP and its associated equipment, taking advantage of the capabilities of C/SP hardware. The user interface is similar to the interface provided by EXEC8 for a CTMC environment.

User Functions - control statements are provided to enable the user to assign and release remote devices. This enables the use of existing assignment and release linkage within the EXEC, with modifications to inform the C/SP of the operation performed.

1100 EXEC Modifications

CONFIG, SMTAGS, SMLIST, DRIVE, INTI2, FIFEE, and others.

1100-C/SP SOFTWARE

A. PRIMARY C/SP SYMBIONTS

   1. INPUT
   2. OUTPUT
   3. REMOTE

B. SECONDARY C/SP SYMBIONTS

   1. PROGRAM LOAD
   2. CONSOLE COMMUNICATIONS
   3. MASS STORAGE
   4. LOGGING

C. C/SP HANDLER

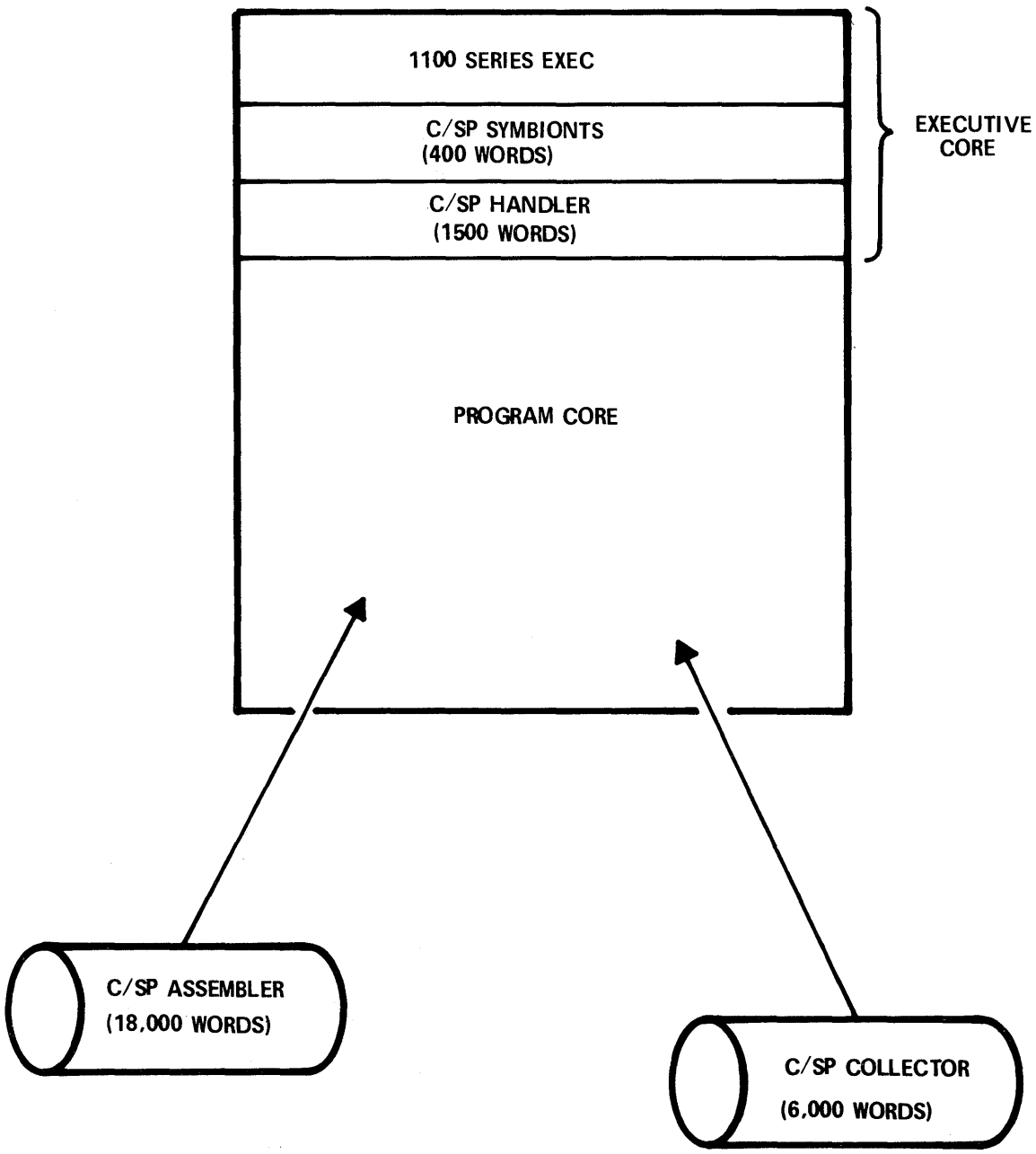
D. 1100 SERIES EXEC MODIFICATIONS

1100 STORAGE REQUIREMENTS

The C/SP Symbionts and C/SP Handler require approximately 400 words and 1500 words respectfully.

The C/SP Assembler requires approximately 18,000 words and the C/SP Collector approximately 6,000 words of 1100 mass storage.

1100 STORAGE REQUIREMENTS

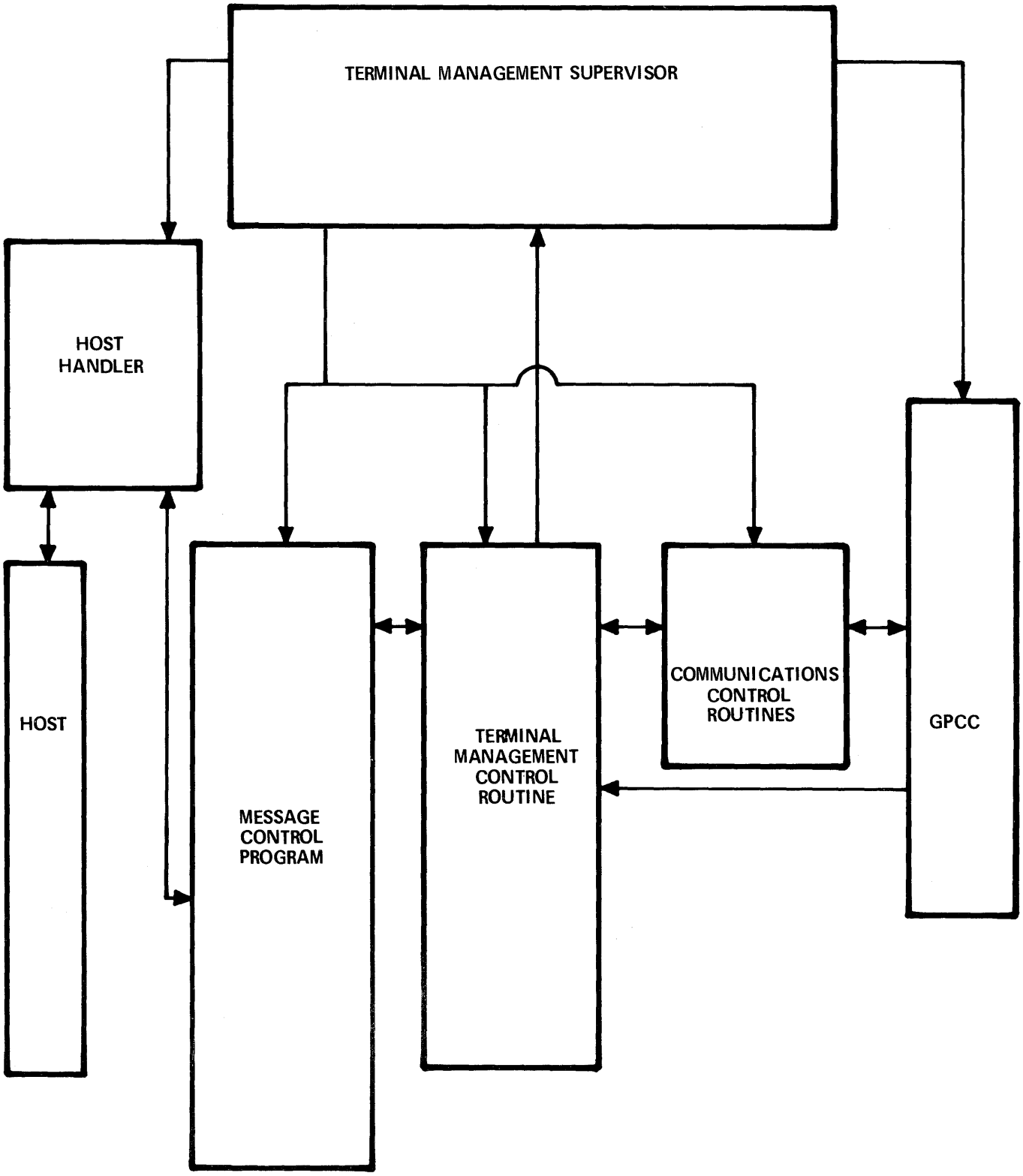


C/SP SOFTWARE BLOCK

The C/SP software which is executed in the C/SP, may be logically divided into five main programs controlling the I/O flow between the various hardware components.

1. Terminal Management Supervisor (TMS)
2. Message Control Program (MCP)
3. Terminal Management Control Routine (TMCR)
4. Communication Control Routines (CCR)
5. Host Handler

C/SP SOFTWARE BLOCK



C/SP SOFTWARE ELEMENTS

Terminal Management Supervisor (TMS)

Provides the basic supervisory functions for the C/SP system. It issues time slices to the various control routines and provides a priority based interaction between these routines. Issues I/O commands, processes interrupts, and coordinates the control of Terminal Management Control Routine, System Message Control Program, and the users MCPs.

Terminal Management Control Routine (TMCR)

Consists of routines for controlling the communication terminals on the C/SP system, performing functions which are common to all terminals.

Message Control Program (MCP)

MCP is a terminal dirver program which receives input from various terminals. It routes the input from the terminals to, a nd accepts messages from, a host processor.

Communications Control Routines (CCR)

Compensate for the differences of a given communication discipline for different devices.

Host Handler

Resident within C/SP and controls all commands between the C/SP and the Host system.

C/SP SOFTWARE ELEMENTS

A. TERMINAL MANAGEMENT SUPERVISOR

B. TERMINAL MANAGEMENT CONTROL ROUTINE

C. MESSAGE CONTROL PROGRAM

D. COMMUNICATIONS CONTROL ROUTINES

1. DCT 500/TELETYPE
2. BINARY SYNCHRONOUS
3. DCT 2000
4. UNIVAC 1004/9000 SERIES RMS–1
5. UNISCOPE 100/DCT 1000
6. REMOTE C/SP

E. HOST HANDLER

C/SP STORAGE REQUIREMENTS

C/SP storage is high performance plated wire, located in one or two units depending on the size of the storage capacity.

Capacity

Minimum memory - 32K bytes (8-bits of data). Expandable in increments of 16K to 131K bytes.

Cycle time - 630 nonoseconds read/write (2 bytes).

Operating mode - non-destructive read out.

Addressing - byte level (17 bit binary number).

Storage protection on program and I/O transfer.

The 32K systems communication capacility cannot be stated as tolerance for an abstract number of lines. Expressed in terms of a specific application and analyzation of several factors: number of terminals, mixture of terminals, anticipated thruput, and amount of storage required for users own code.

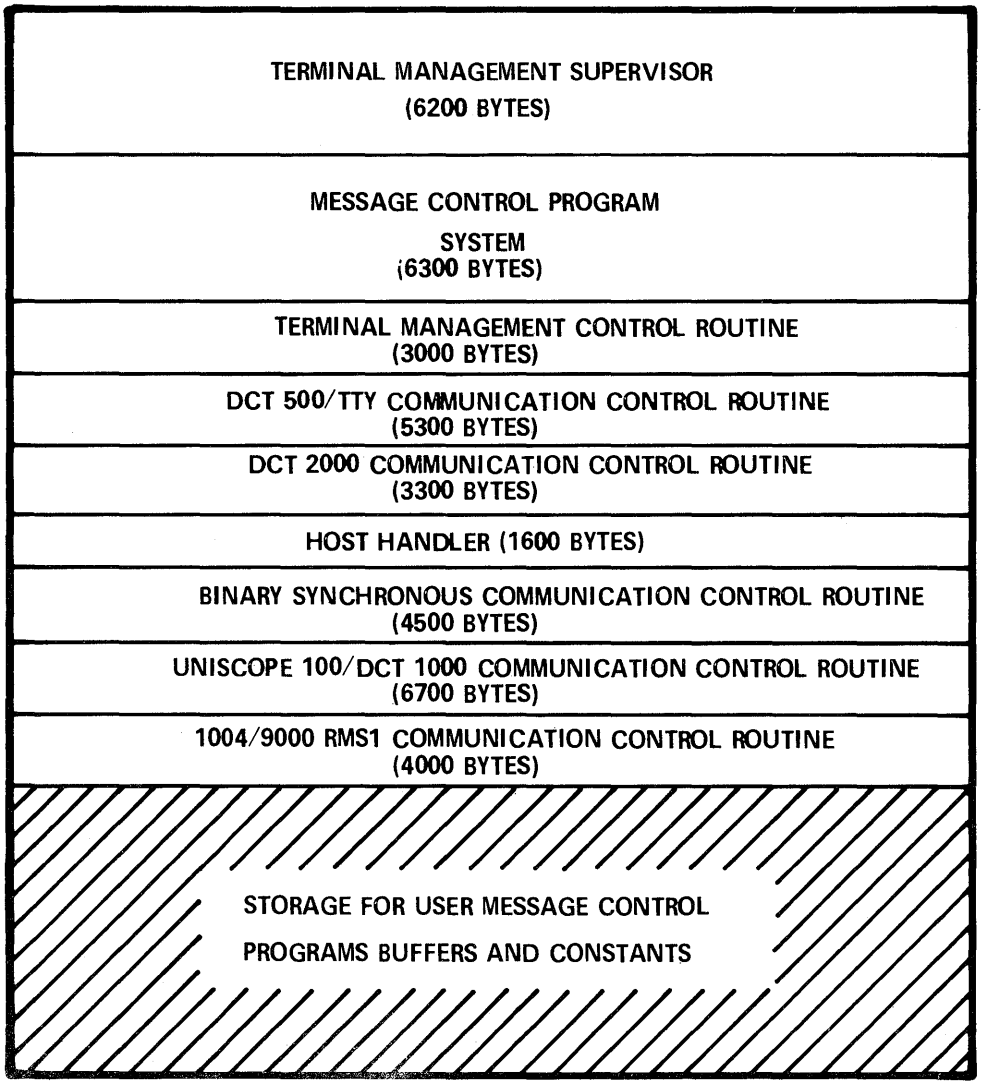
Preliminary estimates of storage occupancy for communications and symbiont support.

Supervisor	- 6200 bytes
MCP	- 6300 bytes
TMCR	- 3000 bytes
ICA	- 1600 bytes
SCP	- 4800 bytes

Additional storage, according to the application for each device type re-entrant CCR, is approximately 2500 bytes, (average). Variable buffers and tables:

1. Storage and buffers per line approximately 350 bytes.
2. Buffer Control Word per position is 16 bytes.
3. Constants per terminal approximately 10 bytes.

C/SP STORAGE REQUIREMENTS

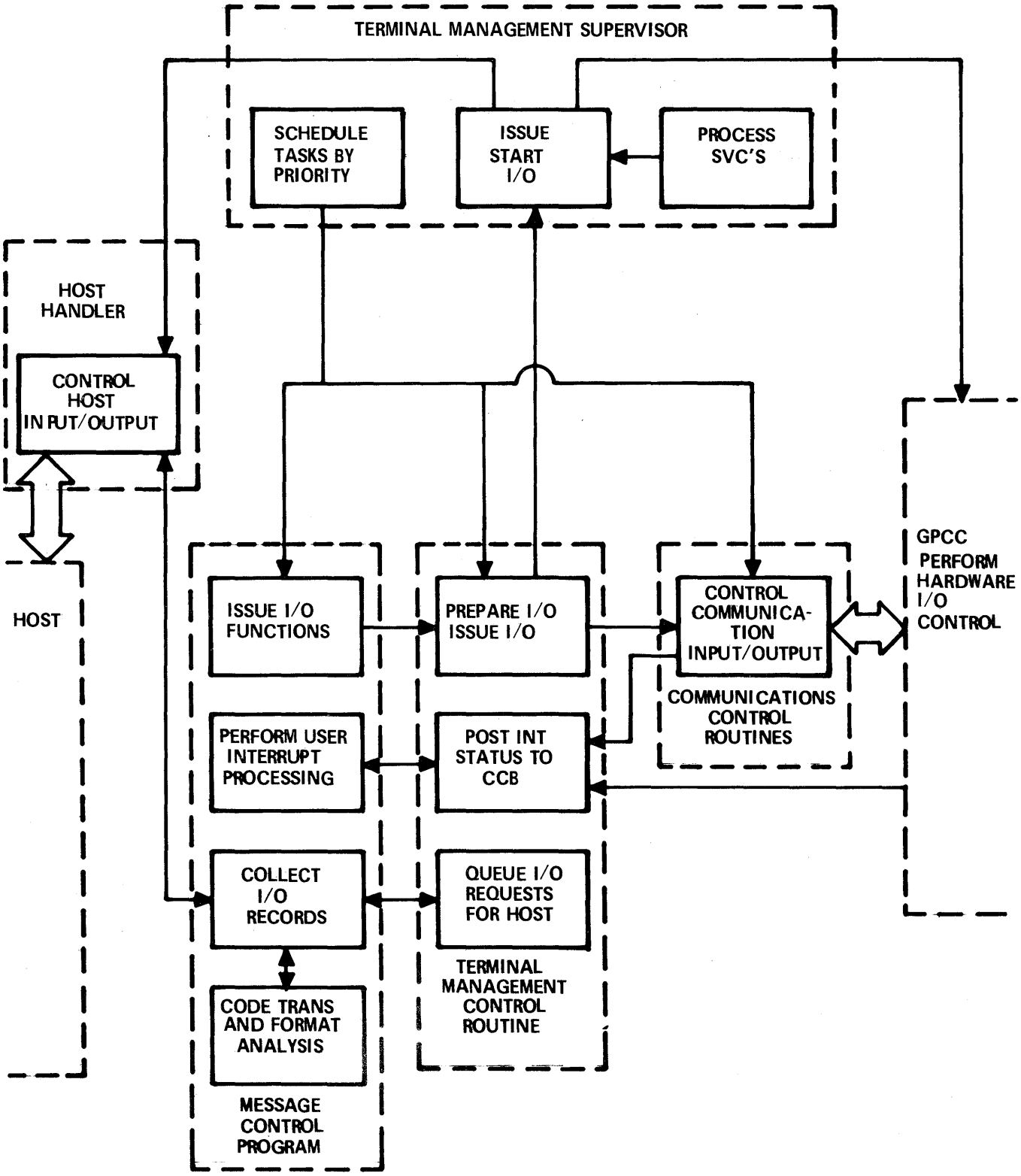


C/SP SOFTWARE BLOCK DIAGRAM

To illustrate the basic software flow, consider a message being routed from a terminal attached to the GPCC, to the Host system.

Upon interrupt from the GPCC, the TMS is activated. TMS activates the TMCR to pre-process the interrupt. TMCR activates the appropriate CCR to complete processing of the interrupt. Control is passed to the MCP which issues the I/O function to the Host handler. The Host handler issues the I/O function to the Host.

C/SP SOFTWARE BLOCK DIAGRAM



C/SP - 1100 SOFTWARE ELEMENTS
(Symbiont Support Software)

A. The Terminal Management Supervisor performs the same functions with the symbiont addition to the system as in the communication environment.

B. Symbiont or Peripheral Control Program - provides the host computer with an efficient interface to onsite paper peripheral devices. The interface is established to input system run streams and output system display information.

C. Peripheral Control Routines - designed to control the I/O associated with devices using the multiplexer channel and the special device channel. The types of devices controlled through the PCR include:

card reader/punch, paper tape, disc, printers, keyboard devices.

C/SP—1100 SOFTWARE ELEMENTS (SSS)

A. TERMINAL MANAGEMENT SUPERVISOR

B. SYMBIONT CONTROL PROGRAM

C. PERIPHERAL CONTROL ROUTINES

1. CARD READER
2. CARD PUNCH
3. PAPER TAPE
4. DISC
5. PRINTERS

1100 - C/SP SUPPORT SOFTWARE

C/SP support software - consists of a C/SP Assembler, MDW Compiler, Collector and Simulator. All are needed at program generation time only and not during communications processing.

C/SP Assembler (CSPASM) - 1 phase, 2 pass that operates under EXEC8. A modified version of the Procedure Definition Processor shall be provided to compile C/SP procedures in the EXEC library. An MDW compiler shall be provided that will process MDW source language.

C/SP Collector (MAPCC) - an 11ØØ processor to provide a means of collecting independent relative binary elements to produce an absolute program for execution in the C/SP.

C/SP Simulator (SIMUL) - A user program to run under the 1100 EXEC. It accepts C/SP object code, simulates execution on the C/SP and provides diagnostic printout to aid in the debugging of the C/SP program. Main purpose is to provide a means of developing the C/SP supervisor or operating system and testing it on an 1100.

1100—C/SP SUPPORT SOFTWARE

A. C/SP ASSEMBLER

   1. PROCEDURE DEFINITION PROCESSOR
   2. MESSAGE DISCIPLINE WORD COMPILER

B. C/SP SIMULATOR

C. C/SP COLLECTOR

C/SP ASSEMBLER

C/SP Assembler is a subset of the 1100 Assembler and resides in the Host Computer. The formats and conventions are a subset of the 9000 Assembler.

1. @ PROCESSOR, OPTIONS - F1.E1,F2.E2,F3.D3 - Same as the control card for 1100 series.

2. STATEMENT FORMAT - Is that of the 9000 Assembler. Columms 1-71; Assembler statement and comments. Column 72: used to indicate continuation. Column 73-80: program identification and sequencing.

3. TERMS, OPERATORS, and EXPRESSIONS:

   a. Self defining: B'101',X'FF',39,C'A'.
   b. Literals: = x'FF'
   c. Symbols: up to six alphanumeric characters of which the first must be alphabetic.
   d. Location counters: maintained by the assembler for the main control section and each dummy section created by the programmer.

4. OPERATORS and EVALUATION: Arithmetic, logical, relation, as *(multiply), ++(OR), = (equal).

5. EXPRESSIONS: Consists of one or more terms connected by operators.

6. INSTRUCTIONS: 52 half word and word instructions.

7. DIRECTIVES:

EQU	TITLE
START	SPACE
END	SET
ORG	DO
CNOP	ENDO
USING	GOTO
DROP	LABEL
ENTRY	AND OTHERS

C/SP ASSEMBLER

@ CSPASM, OPTION F1, E1, F2, E2, F3, E3

1. STATEMENT FORMAT
2. TERMS, OPERATORS, EXPRESSIONS
    a. SELF DEFINING
    b. LITERALS
    c. SYMBOLS
    d. LOCATION COUNTERS
3. OPERATORS AND EVALUATION
4. EXPRESSIONS
5. INSTRUCTIONS
6. DIRECTIVES

SUMMARY OF PROCESSOR INSTRUCTIONS - I

The Binary Arithmetic instructions provide the capability of modifying and valuating data. These instructions use full word memory, half-word memory and registers.

SUMMARY OF PROCESSOR INSTRUCTIONS-I

BINARY ARITHMETIC

INSTRUCTION	MNEMONIC	OP CODE	FORMAT
ADD	A	5A	RX
	AH	4A	RX
	AR	1A	RR
COMPARE	C	59	RX
	CH	49	RX
	CR	19	RR
DIVIDE HALF-WORD	DH	53	RX
LOAD	L	58	RX
	LH	48	RX
	LR	18	RR
MULTIPLY HALF-WORD	MH	52	RX
SHIFT LEFT SINGLE	SLA	8B	RS
SHIFT RIGHT SINGLE	SRA	8A	RS
SUBTRACT	S	5B	RX
	SH	4B	RX
	SR	1B	RR
STORE	ST	5Ø	RX
	STH	4Ø	RX

SUMMARY CONTINUED - II

The Branching instructions provides the capability of conditional transfer of control from one routine to another.

The Status Switching instructions are Supervisor instructions for controlling the multi-programming environment.

The Input/Output instructions (one) provides the data channel transfer capability. It is a supervisor or privileged instruction.

SUMMARY CONTINUED-II

BRANCHING

INSTRUCTION	MNEMONIC	OP CODE	FORMAT
BRANCH & LINK	BAL	45	RX
	BALR	Ø5	RR
BRANCH ON CONDITION	BC	47	RX
	BCR	Ø7	RR
BRANCH ON COUNT	BCT	46	RX
	BCTR	Ø6	RR
BRANCH ON INDEX HIGH	BXH	86	RS
BRANCH ON INDEX LOW OR EQUAL	BXLE	87	RS

STATUS SWITCHING

HALT & PROCEED	HPR	99	SI *
LOAD PSW	LPSW	82	SI *
SET STORAGE KEY	SSK	Ø8	RR *
SET SYSTEM MASK	SSM	8Ø	SI *
SUPERVISOR CALL	SVC	ØA	RR

INPUT/OUTPUT

START I/O	SIO	9C	SI *

* PRIVILEGED INSTRUCTIONS

SUMMARY CONTINUED - III

The Logical instructions provide the capability of testing and altering data by bit or groups of bits.

The Divide Polynomial is provided for cyclic redundancy check (sophisticated parity check).

SUMMARY CONTINUED—III

LOGICAL

INSTRUCTION	MNEMONIC	OP CODE	FORMAT
AND	N	54	RX
	NI	94	SI
	NR	14	RR
COMPARE LOGICAL	CL	55	RX
	CLI	95	SI
	CLR	15	RR
DIVIDE POLYNOMIAL	DP	81	RS
EXCLUSIVE OR	X	57	RX
	XI	97	SI
	XR	17	RR
INSERT CHARACTER	IC	43	RX
LOAD ADDRESS	LA	41	RX
MOVE	MVI	92	SI
OR	O	56	RX
	OI	96	SI
	OR	16	RR
SHIFT LEFT SINGLE LOGICAL	SLL	89	RS
SHIFT RIGHT SINGLE LOGICAL	SRL	88	RS
STORE	STC	42	RX
TEST UNDER MASK	TM	91	SI

C/SP COLLECTOR

The C/SP Collector is concerned with generating C/SP loadable (absolute) programs and resides in the Host Computer.

1. @MAPCC

2. Collector control statements or directives:
   a. LOADM: where the operand is FN.EN, Address FN is the file where the user wants the loadable program created. Address specifies the starting address.
   b. INCLUDE: specifies the relocatable program to be included in this collection.
   c. EQU: equates name to the value.
   d. RCORR: specify corrections to a relocatable program.
   e. LINKOP: collector options.
   f. SNAP: provides for dynamic memory dumps.
   g. ENDC: specifies the end of collector directives.
   h. ENTER: the location where the execution of the program starts.

C/SP COLLECTOR

@ MAPCC

1. LOADM OPERAND

   FN.EN, ADDRESS

2. INCLUDE FN.EN

3. EQU NAME/VALUE

4. RCORR FN.EN

   ADDRESS/X'mn...n'

5. LINKOP OPTIONS

   (a) MAP

   (b) NOABORT

6. SNAP FN.EN, ADDRESS, DUMP. SIZE,

   COUNT, FREQUENCY, R,A

7. ENDC

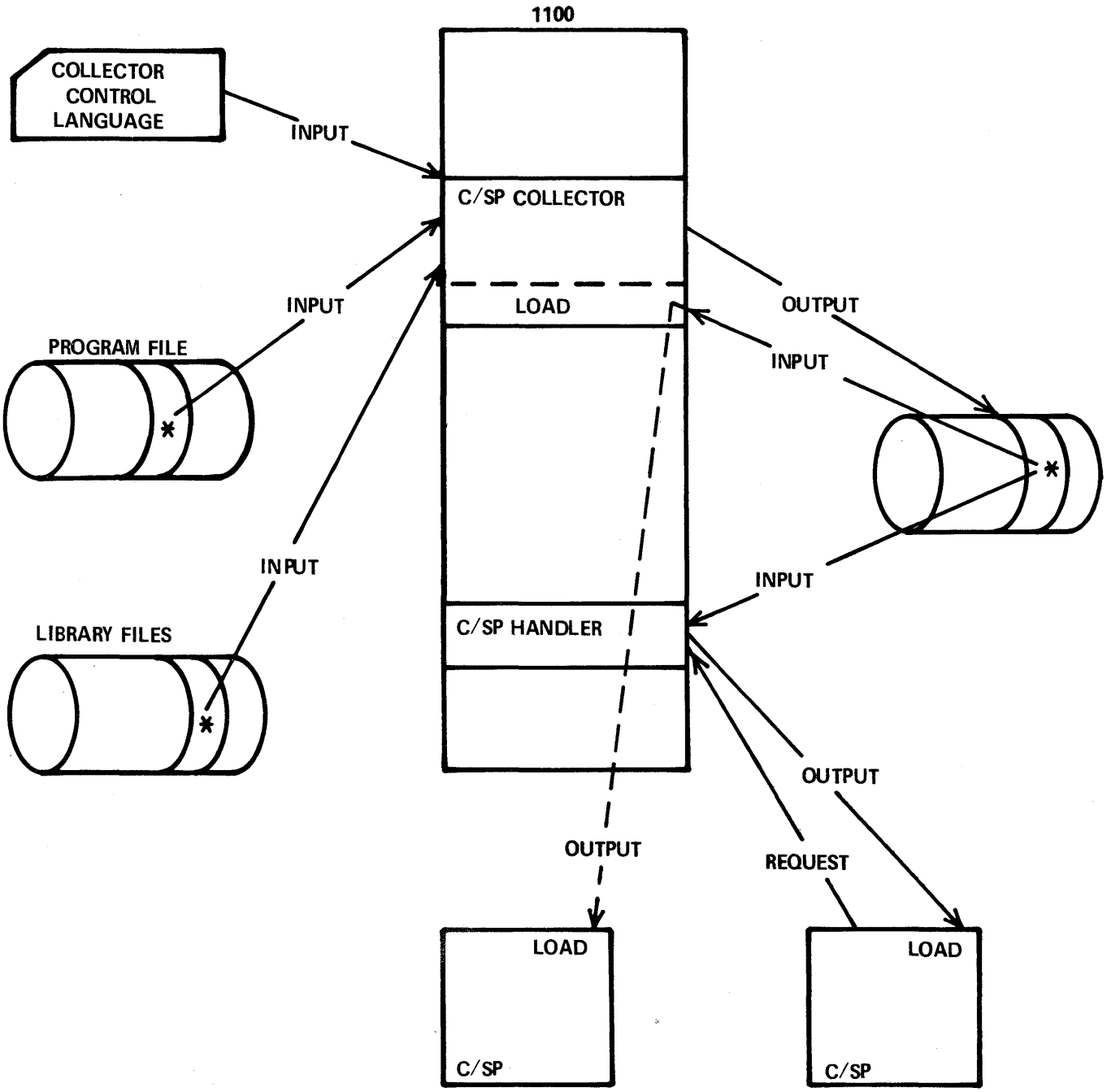
8. ENTER LABEL

C/SP COLLECTOR DIAGRAM

Input to the Collector, under direction of the Collector control language, is from object programs produced by the C/SP Assembler. The object programs may be found in a program file (established by the user via a @ ASG), in TPF$., and the system library.

The C/SP collector creates the loadable program in a program file which may be TPF$., or a user-established program file.

C/SP COLLECTOR



C/SP DOCUMENTATION AND VIDEO TAPES

Reference material available:

C/SP System Description	UP-7850
C/SP Processor Languages	UP-7870
C/SP Languages 1100 Series Supplement	UP-7874
C/SP Simulator	UP-7862
C/SP Processor and Storage	UP-7866
C/SP Operating System PRM	UP-7900

A C/SP Binder and Index Tabs are available under number UP-7880.

Other documentation for future release includes:

1. Operators Reference
2. Operating System 1100 Supplement
3. Installation Support Manual
4. OS Reference Booklet

The video tape presentations are available on the C/SP Hardware. The software presentations are in the process of being prepared.

C/SP DOCUMENTATION AND VIDEO

A. PRODUCT SOFTWARE DESCRIPTIONS

1. C/SP (CTMC REPLACEMENT)
2. C/SP (SYMBIONT SUPPORT SUBSYSTEM)

B. C/SP USER DOCUMENTATION

1. SYSTEM DESCRIPTION
2. SIMULATOR
3. PROCESSOR LANGUAGES
4. LANGUAGES 1100 SERIES SUPPLEMENT
5. PROGRAMMER REFERENCE
6. OPERATING SYSTEM (PRM)
7. OPERATING SYSTEM 1100 SUPPLEMENT
8. OPERATOR REFERENCE
9. INSTALLATION SUPPORT
10. OS REFERENCE BOOKLET

C. VIDEO PRESENTATIONS

1. INTRODUCTORY SEMINAR
2. PROCESSOR AND STORAGE
3. GENERAL PURPOSE COMMUNICATIONS CHANNEL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