SPERRY RAND

UNIVAC

MARKETING GUIDE

COMMUNICATIONS/ SYMBIONT PROCESSOR

WORLD WIDE MARKETING AND SERVICES

COMPANY CONFIDENTIAL

UNIVAC

COMMUNICATIONS/SYMBIONT PROCESSOR

MARKETING GUIDE

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Preface

This Marketing Guide was prepared by the Product Requirements Department for use by Field Marketing personnel throughout all Marketing divisions. The information contained in this Marketing Guide is based on latest available specifications prior to announcement and is subject to change. It will be supplemented with additional releases, manuals, and other documentation. The contents of this document are designed to assist the salesmen and analysts in a better understanding of the product and its potential markets. It contains sales ideas, product benefits, and possible uses and applications. It is strictly company confidential and its distribution should be limited to Univac personnel only.

November 10, 1970

INTRODUCTION

The C/SP is a high performance internally programmed symbiont processor which is intended for on-site peripheral and communications control. The C/SP can control a variety of low and high speed peripherals and communication lines and provide interfacing to a central computer system.

UNIVAC defines symbiont as a subroutine or piece of code which controls a peripheral in conjunction with another piece of code (symbiont) to effect a combined I/O function. Currently, symbionts are controlled by the central processor of a system. This results in the system remaining idle during the cycles required for the peripheral to dispatch the output or accept the input.

The primary purpose of the C/SP is to unburden the central computer hardware and software of the need to handle all types of terminal devices. The C/SP performs those functions which are concerned with source, destination, formatting, storage, retrieval, and translation of data coming from and going to the various remote devices.

Operating as a central site multiplexer or pre-processor, the PCC will serve as a terminus for those communication lines over which data will be transmitted to and from the computer. These lines may vary from the familiar teletype lines which transmit ten (10) characters per second to the ultra high speed broad band lines operating at over 28,800 characters per second. Each line may have one or more terminals transmitting and/or receiving data.

In any system a variety of individual line and terminal configurations may be operating under a number of different line procedures, code sets, control signals, and timing constraints. The C/SP has the capability of working with these differing conditions and presenting to the central computer data in a standard format ready for processing.

When used as a peripheral symbiont processor, the C/SP effectively simplifies the major system's interface to I/O devices by presenting one type of control sequence. All peripheral devices attached, and all communications lines are effectively controlled by the C/SP thus removing the entire symbiont complex from the main system. This results in both a time and a memory savings.

Among the salient features of the C/SP are:

- Modular design
- Communications oriented software
- 32K to 131K bytes of plated wire storage
- 630 manosecond read/write storage cycle
- Storage protection
- Sixteen 32-bit word General Purpose Register, external to storage
- 52 half-word and word instructions
- Half-word (16 bits and 2 parity) basic data path
- Multi-level interrupts

MARKETING STRATEGY

PRODUCT LINE OBJECTIVES

Data communications is considered to be the fastest growing segment of the EDP industry. UNIVAC has long held a prominent position in this field. This prominence can be attributed to UNIVAC's unique and enviable knowledge of data handling in a real-time environment.

UNIVAC is exerting a continued effort to maintain its lead in the market. The recent introductions of the UNIVAC DCT 500, DCT 1000, and the Uniscope 100 complete with modems and special interface facilities are a part of this effort.

The UNIVAC Communications/Symbiont Processor (C/SP) is our newest entry. It incorporates the most advanced technology and techniques. It is the next logical step in the development of the most comprehensive line of communication products offered by any EDP System supplier.

C/SP MARKET OBJECTIVES

The primary marketing objective of the C/SP is to enhance and expand the communications handling capabilities of UNIVAC's 1100 system. Accomplishing this objective will enable increased penetration into the real-time, time sharing, and remote demand batch market areas. To achieve this objective the C/SP offers:

- a significant reduction in host processor overhead associated with peripheral control,

communication character handling, and message interrupt processing.

- a significant reduction in storage allotment for peripheral and communications symbiont activity.

- optimized system performance by interfacing with the host operating system at the transaction or job level.

- optimized line handling capabilities by increasing the number of lines, improving efficiency, and simplifying user interface.

- flexibility and ease of implementing remote devices of all types and speeds.

- a system element which the user may implement, modify, or maintain without major consequence to the total system function.

- future expansion capabilities to further improve the cost/performance ratio.

The flexibility offered by the C/SP will promote the ability of a central site system to effectively interface with a wide assortment of available

remote communications terminals. In addition to supporting considerable selectivity of remote devices in new systems implementation, it will permit a smooth expansion of the system by offering simplicity in accommodating terminals of many manufacturers.

Characteristics which serve to implement interface flexibility include:

- Transparent CLT's
- Software modifiable interface functions
- Transient character comparisons
- Automatic program loop control
- Automatic code level conversions
- Controlled exclusion of message control characters
- Automatic termination of line activity

Greater throughput performance is achieved because communications handling is performed simultaneously with central site processing. The desirability of the C/SP stems from its extreme flexibility in matching device oriented transmission disciplines via software controlled buffer control elements. Virtually any type of code up to 8 bits, any form of integrity checks, any number of control code recognitions including sequences, and messages of any length can be accommodated with a unique method of hardware enhanced software. This unique design enables the programmer to make critical decisions within a character time insuring line service time adequate to sustain full duplex transmission at 4800 bps on all 32 lines simultaneously.

Additional performance improvement is achieved by the transfer of data to and from the host CPU in Internally Specified Indexing (ISI) mode. ISI channel operations offer a significant performance increase over Externally Specified Index (ESI) operations because main storage cycles are reduced by a factor of three (3) and storage is more effectively utilized. In addition, ISI operations require less interactivity with control tables and interrupt routines. This increased performance results in the host system being able to devote a greater portion of its activity to data processing rather than data servicing.

Particular System Benefits derived from front end processing include:

- Storage Savings - removal of device symbionts, reduced buffer requirements.

- Time Savings - interrupt handling associated with line control, line synchronization, control character recognition, imbedded ACK's, block acknowledgement, retransmission requests, etc.

- Channel Efficiency - block transfers of packed data, fewer accesses to storage, and higher transfer rates.

The capabilities of the C/SP for handling communications activities are enhanced by specialized hardware and software. A communications oriented Executive System controls the operation of the C/SP providing extensive interrupt handling capabilities, error logging, coordination and interfacing of

Communication Control Routines (CCR) within a multi-programming environment. The specialized hardware features enable a substantial reduction in software overhead both in terms of size and execution time. Hardware was particularly designed to facilitate those activities peculiar to a communications environment; these include the interrogation and checking of each character during the time-frame between the arrival of characters on a particular line.

EFFECTIVE IMPLEMENTATION

The implementation of the above objective involved several noteworthy decisions. These decisions included:

- choice of hardware components
- modularity of system components
- hardware efficiency versus software flexibility trade-offs
- incorporation of new techniques and technologies (e.g. firmware)
- size and extent of software operating system

The choice of available technologies decided on has resulted in a product which is decidedly advantageous to the large majority of large-scale system users. The benefits afforded are listed below. They are catagorized by improvements resulting from improved hardware design, software design and systems design.

HARDWARE

- increased speed - the speed of the C/SP is improved by the

selection of new MSI integrated circuitry and the utilization of 630 ns. plated wire main storage.

- increased interface transfer rate - high speed transfers at the host machine interface on a word basis (36 bits).

- increased efficiency - accomplished by effecting repetitive communications tasks which occur on all communication lines, in hardware, (e.g. character parity, control character recognition, interrupt tabling, etc.)

- increased throughput - by effectively transferring data to/from the host processor on a transaction basis thus improving I/O channel efficiency.

- increased flexibility - by controlling hardware line terminal functions with software modifiable control words.

- greater range of capacity - modularity permits up to 64 line terminals to be accommodated, all of which may be operated in a full duplex mode. Where half duplex operation is desired, the capacity is doubled (e.g. up to 128 lines)

SOFTWARE

- reduces host processor overhead - by absorbing the responsibility for all I/O activity on readers, punches, printers and communications lines.

- allows modification and additions - of device handlers with complete immunity to the host executive system.

- compactness - smaller device handlers due to effective firmware.

- simplifies user interface - by simple and effective links with C/SP operating system at the macro level. Message oriented tasks such as editing, compression, syntax and language checks may be generated by the user and linked to the operating system.

SYSTEM IMPROVEMENTS

- extended processing - the concurrent operation of foreground and background processing with virtually no contention for system facilities results in greater efficiency.

- system back-up - the separation of the communications function from host processor tasks enhances complete redundancy. The need for redundant communications processors is more easily and economically accomplished when the function is performed by a separate system.

- system tailoring - storage increments, line increments, and component duplication can be specified to fit the application, and expanded as need dictates.

- improved uptime - maintenance functions on the C/SP can be performed independently of main processor activities.

- transferability - communications network and control may be transferred in tact to a new or backup host system.

- system expansion - adding network terminals, or elements of software can be accomplished with minimum effect on host operation.

- system efficiency - by stressing efficient buffer management, program switching, and interrupt routines.

The C/SP is available as a Communications Processor on the 1106 and 1108.

All benefits and system improvements afforded the 1110 in the area of communications applies as well to the UNIVAC 1106 and 1108. Peripheral symbiont control, however, will not be available for the 1106 and 1108.

HARDWARE CHARACTERISTICS

Contents

1. STORAGE

High performance plated wire storage is an integral part of the C/SP. It is located within a separate cabinet.

In discussing C/SP Storage, it is convenient to make the following definitions:

Byte	8 Information Bits
Half-word	2 Consecutive Bytes
Full-word	4 Consecutive Bytes

Storage has the following characteristics:

Capacity - 32,768 bytes minimum; 131,072 bytes maximum

Cycle time - 630 nanoseconds read/write cycle

Operating mode - non-destructive readout

Storage data path - 18-bits wide (2 bytes and 2 parity bits)

Addressing - Direct and optional zero time indexing

Storage protection - Program and I/O transfer

Parity - Odd parity (1 parity bit per byte)

Storage Data Bounds

Fixed length fields (half-words and words) must be placed in storage on appropriate multiple byte boundaries. The binary address of these fields must be in the form:

Half-word	XX...XXO
Word	XX...XOO

All processor instructions are restricted to half-word boundaries.

Addressing

The addressing hardware accommodates a 17-bit address field which permits direct addressing of 131,072 bytes. While the address field permits the addressing of each byte, the least significant bit of the address is not used to access the data from storage.

On a read cycle the storage will present two bytes to the processor. If the particular reference requires byte address ability, the processor will select the appropriate byte based upon the least significant bit of the address field.

The capability for Partial Write is provided; that is, one byte may be written without altering the other byte in the storage half-word.

Parity

The parity bit associated with each byte provides odd parity for the byte. Parity generation and checking is performed in storage. The parity bits are, however, presented to the processor or an appropriate channel or a read cycle.

Storage Protection

Since there may be several programs resident in main storage at any one time, it becomes necessary to restrict storage accesses by a program to the storage limits assigned to it. On the C/SP this is accomplished in

the following way.

Associated with main storage there is a maximum of 64 3-bit registers called Key Storage Registers. The storage, beginning at address zero, is divided into a maximum of 64 blocks each of which contains 2048 bytes. Each of these blocks is assigned a Key Storage Register. The six most significant bits of a storage address are used to define the address of the Key Storage Register associated with the block containing the storage address.

Storage is segmented by grouping together all blocks whose associated Key Registers have the same setting. Since there are 3-bit positions in a Key Storage Register, a maximum of eight storage segments can be defined.

When a program is loaded, it is assigned a unique program number. This number is then loaded in the Key Storage Register associated with each 2048 byte block assigned to the program.

Storage protection against improper storage accessing is provided during instruction execution and I/O transfers.

Instruction Execution Protection

When a program is scheduled for execution, its program number is loaded into a register* uniquely identified with the program currently in operation. On each access to storage during processing the program number in

* Program Status Word

- 630 nanosecond cycle time
- Basic RX binary add instruction time of 2.52 us (4 cycles)
- Binary RR add instruction time of 1.26 us (2 cycles)

The processor contains sixteen general purpose registers, each 32-bits (one word) wide. These registers are used for arithmetic operations, instruction indexing, subroutine loop control, and the moving of data. The control section of the processor:

- Controls the sequence in which instructions are executed.
- Interprets and controls the execution of each instruction.
- Initiates the cycling of main storage.
- Sequences interrupt handling procedures.
- Controls transfers into and out of storage.
- Handles storage protection checking.
- Maintains program address location counter.
- Controls mode of operating.

Arithmetic Section

The Arithmetic Section of the processor performs all data manipulations including logical and numerical arithmetic, data comparisons, and shifting. It also performs single or double indexing of operand addresses. Arithmetic operations are performed in two's complement form. A fixed point arithmetic operand can be either 32-bit word or a 16-bit half-word. The sign of a fixed point operand is always the leftmost bit of the operand. When a half-word fixed point number is called from storage, it is always expanded to a right

justified fullword; the sign is extended to the left.

Logical operations on fixed length operands are performed in registers. Logical operations include comparing, translating, editing, bit setting, and bit testing.

INSTRUCTION SET

The C/SP instruction set consists of the following types:

- arithmetic
- branch
- compare
- data transfer
- logical
- privileged
- special

Each of these falls into one of four format arrangements. Each format has unique operation characteristics.

RR - (Register to Register) This instruction format is one half-word in length and is used for operations involving operands, all of which reside in general purpose registers.

RX - (Register to Indexed Storage) This format is one word in length and is used to perform operations involving one register to/from which data will be transferred from/to indexed storage. Various logical or arithmetical operations can be performed with this instruction.

RS - (Register to Storage) This format is one word in length and is used to perform shifting and branching operations.

SI - (Storage and Immediate Operand) This format is one word in length and involves instruction requiring an operand within the instruction.

Interval Timer

The Interval Timer which utilizes a fixed word location in storage is a feature in the processor which provides interval timing and time of day information. Interval timer requests for service are made every six (6) milliseconds.

3. INTERRUPT

The interrupt system provides an automatic means of alerting the PCC processor to exceptional or unexpected conditions such as the end of I/O operations, program errors, machine errors, etc., and directs the processor to the appropriate program routine following their detection. The system permits the interrupting of any task in order to process a task of higher priority. Among the features of the interrupt function are the following:

- Automatic tabling of communications channel interrupts
- A dynamically alterable priority structure
- A duplicate register set for supervisor operations
- Automatic program switch by interrupt type

The system design is such that processing occurs on a priority basis by class of interrupt. There are five classes of interrupt which are listed below in the order in which their interrupt requests are recognized by

the hardware.

- Program/Machine Check Interrupt. This type of interrupt is caused by any of the following conditions:
  - Invalid operation code
  - An attempt to execute a privileged instruction while in Problem Mode
  - Protection exception. (This occurs when the operating program attempts to access an area of storage which is not assigned to it.)
  - An attempt to address a location beyond the storage size installed.
  - Parity error upon a transfer of data to or from storage
  - Power failure
- Supervisor Call Interrupt. This interrupt results from the execution of a supervisor call instruction. Status information provides the operating system with a link to parameter information in the calling program.
- Time Interrupt. This interrupt occurs when a program setable interval counter reaches zero. The interval setting may vary from a count of one to 256; it is decremented by 1 every 6 MS.
- I/O B Interrupt. This type of interrupt will occur whenever one of

the channels or channel adapters accept or terminate an I/O function, or detects a device malfunction or a data parity error.

- I/O A Interrupt. This class of interrupt has the lowest priority after a Program/Maching Check Interrupt. It is generated by a variety of conditions monitored by the General Purpose Communications Channel (GPCC) in control of communications activity. Such conditions include data parity error, loss of transmission carrier, recognition of program specified control characters. Special interrupt tabling accommodations have been provided for with the GPCC.

Since not all the processing that is required for communications interrupts are equally time critical, the PCC provides for four interrupt lists in storage. Upon the occurrence of a communications interrupt, a Channel Interrupt Word is automatically stored on one of the lists; the list being selected on the basis of the priority of the cause of interrupt.

The contents of these words indicate the device causing the interrupt, the location in storage last used for the transfer of data, and the cause of the interrupt.

4. CHANNELS

All information transmission in and out of the C/SP is handled by channels. A channel controls the operation of input/output devices and the transfer

of data between devices and storage.

Among the outstanding features of the C/SP channels are:

- Direct interface to storage
- Independent operation
- Simultaneous operation
- Up to two GPCC's each capable of controlling up to 64 communication lines
- Priority interchangeability

There may be up to seven (7) channels, number 0 to 6, in the C/SP. Priority of these channels increases in descending channel number order, channel 0 having the highest order.

Channel Types

The C/SP is equipped with four types of channels:

1. Special Device Channel (SDC)
2. Inter-Computer Adapter Channel (CA)
3. Multiplexer Channel
4. General Purpose Communications Channel (GPCC)

Special Device Channel (SDC)

The primary function of the Special Device Channel is to provide the means for local program loading and maintenance using a card reader Type 0708-27/28.

This Card Reader is a serial 80 column, 80 card per minute device.

Inter-Computer Adapter Channel (ICA)

The 1100 Series Adapter Channel provides an interface for direction connection of the C/SP to an I/O channel of an 1100 Series System. The maximum transfer rate is in excess of 300,000 (36-bit) words per second.

The multiplexer channel provides the capability to connect up to eight peripheral subsystems of the type listed below:

- 0604 Card Punch - 250 cpm, 80 Column
- 0716 Card Reader - 1000 cpm, 80 Column
- 0768 Printer - 1100 - 1600 lpm, 132 Column

These peripheral subsystems may be connected in any combination of up to eight.

The multiplexer channel permits concurrent operation of the peripheral subsystem attached. A priority of subsystem service is established by the order of attachment to the daisy-chain arrangement. Subsystems not ready for service will propogate the invitational probe to the next subsystem on-line.

Transfer takes place in bit parallel, byte serial mode. Status conditions will be generated at the subsystem and sent to the CPU upon request. The multiplexer channel transfers data, once initiated, independent of program control.

General Purpose Communication Channel (GPCC)

The General Purpose Communication Channel is the link between the main storage and the Communication Line Terminals. The GPCC performs such functions as multiplexing the various Communication Line Terminals, recognizing special characters, checking character parity, coordinating all data transfers to and from storage, and executing other necessary operations.

The GPCC is required to analyze each data character and/or sequence(s) of characters which is transmitted through it and to act upon these characters in a manner which is a program changeable function on the line to which the GPCC is connected. The GPCC also interfaces with the C/SP Processor to service Start I/O instructions and interrupts. Associated with the GPCC is a display panel which contains an Active Line Indicator for each position.

The principal function of the GPCC is to multiplex a single channel of the C/SP so that the one data path may be shared by as many as 64 communication lines. The multiplexer selects one of 64 CLT data paths to time share the data path to the GPCC. Each of the 64 data paths available to the CLT's are referred to as multiplexer positions. The basic GPCC provides 8 multiplexer positions; these are expandable groups of 8 to a total 64.

A Communication Line Terminal (CLT) is placed in a GPCC terminal position

to interface a modem on the communication line. A CLT operating in full duplex mode requires two positions while one operating in a half-duplex mode requires but one. A variety of CLT models are provided to dial remote stations and to accommodate communication lines with rates up to 50 kilobits per second operating in either synchronous or asynchronous mode.

A CLT performs the function of inputting or outputting at a character in the following way:

1. Accepting control commands from the GPCC.
2. Requesting services from the C/SP to input or output a character.
3. Storing one character in each of the input and output sections of the CLT.
4. Transferring the character to or from the data set (modem) bit-serially.
5. Manipulating and interpreting the control leads to the data set.
6. Monitoring the lines for error conditions such as loss of carrier.
7. Presenting CLT status to the GPCC.

Differences in operation between a synchronous and an asynchronous CLT relate to the different methods of establishing character synchronization.

Synchronous:

1. Receives data bit-serially from the data set and tests for synchronizing code bit combination.

2. Upon recognition of a synchronous code, enters data mode by initiating service requests to the GPCC for each subsequent N-bits received.

   Note: N = code level.

Asynchronous:

1. Recognize and extract the start and stop bits associated with each character received from the data set.
2. Generate the start and stop bits associated with each character transferred to the data set.

The Dialer is a device which permits the GPCC to control an Automatic Calling Unit (ACU) for the purpose of originating calls automatically on a switched telephone network. It performs the following functions of:

1. Accepting control commands from the GPCC.
2. Requesting a dialing digit from the GPCC.
3. Transmitting a dialing digit to the ACU in 4-bit serial form.
4. Manipulating and interpreting the control leads of the ACU.
5. Presenting dialer status to the GPCC.

The CLT's have the ability to operate in test mode. This mode provides a means to checkout the operation of the CLT without involving the data set or the communication lines.

Timing assemblies provide the line frequencies required by the asynchronous CLT's. One line frequency is provided with the basic GPCC. Only one timing source is required for each different speed to be used in the system. Up to seven different frequency timing sources may be used on one GPCC.

The CPU-I/O Channel Interface section of the processor provides the interface between the C/SP Processor and the GPCC Control Logic. This interface recognizes I/O instructions intended for the GPCC; it provides for access to main storage and provides the logic paths for interrupts from the GPCC.

The Control Logic Section of the GPCC is the section that especially distinguishes the C/SP from competitive devices. The GPCC Control Logic interfaces to and controls the operation of the CLT's communicating with it through the multiplexer assembly. Contained within the logic are a number of hardware registers which are loaded under software control to assist in these control functions.

Control is exercised through various control word formats. These are:

Channel Address Word (CAW)
Buffer Control Word (BCW)
Message Discipline Word (MDW)
Channel Interrupt Word (CIW)

Channel Address Word (CAW)

The CAW is accessed from storage by the GPCC when a processor (START I/O) instruction with the GPCC's channel number is detected. The GPCC stores the 16 most significant bits of the CAW in its hardware. This stored command is called an external function. Five CAW formats are provided.

Buffer Control Word (BCW)

A BCW exercises primary control over the flow of data between an individual CLT and storage. Each GPCC terminal position has a corresponding BCW assigned to it.

Message Discipline Word (MDW)

An MDW may be used to supplement the control provided by the BCW. It exercises control over the data transfer relative to the control information contained in the data being transferred. Provisions are provided to compare each input character against up to six unique codes simultaneously. Among the functions under its control are:

1. store or not store character
2. interrupt or not interrupt on character recognition
3. terminate or not terminate line
4. link to new MDW control word

The BCW specifies whether an MDW will be accessed, and if so, which MDW will be accessed. All time variant constants and the field that designates the currently active MDW is in the BCW for each line. A MDW list may be used by all lines that operate under the same message discipline.

Channel Interrupt Word

A Channel Interrupt Word (CIW) is stored whenever a condition is recognized which requires the attention of the controlling program. The control supplied by the BCW/MDW has been designed to allow for the program to respond to interrupt conditions, thus, the advantages of a semi-soft interrupt scheme may be realized. Interrupts are tabled in the form of CIW's and an interrupt

request is generated. Additional interrupts will likewise be tabled even if the previous request has not been honored, thus, efficiency in examining CIW's by the program is provided.

SOFTWARE

INTRODUCTION

MINIMUM EQUIPMENT REQUIREMENTS

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INTRODUCTION

The C/SP Operating System is concerned with communication line control, data control, and data preprocessing. It provides a simplified, standard user interface for receiving from or sending data to a remote device.

Such things as message translation, editing, remote device acquire, sign-on procedures for demand and remote batch operation, job stream - job control statement sequence checking will be handled by the operating system, thereby, relieving the host processor, the host executive, and the host problem programs from the details normally associated with communications.

The Operating System has been written in MACRO form, to enable the user to assembly only those MACRO's needed to perform the required function.

An element of the operating system called the Message Control Program (MCP) will control a general class of terminals. The user may wish to develop an MCP to operate concurrently but independently of the system generated MCP. This would be desirable in the event there is a unique device monitoring process and unique software requirements to analyze and respond to the input data received from the process monitoring device.

The Operating System can be further tailored to the users requirements by use of input and output own code options as well as through user written contingency routines.

The operating system is but one element of the software support supplied with the C/SP. Elsewhere in this section is listed the other elements furnished to integrate the C/SP as a part of the total 1100 Series systems.

MINIMUM EQUIPMENT REQUIREMENTS

- Communications/Symbiont Processing
  - C/SP with 49K
  - One GPCC
  - 1110 Intercomputer Adapter
  - One MUX Channel, Reader, Printer
- Communications Processing
  - C/SP with 32K
  - One GPCC
  - 1100 Intercomputer Adapter
  - Spec. Dev. Channel & Reader

STORAGE ALLOCATION

The storage allotment for the system's communication capability cannot be stated as tolerance for an abstract number of lines. It can only be expressed in terms of a specific application and only after several factors have been analyzed such as type of terminals, mixture of terminals, anticipated throughput, and the amount of code for users' own code processing.

To assist in determination of storage requirements, the following preliminary estimates of storage occupancy are provided:

ELEMENT	BYTES
C/SP Operating System	25,000

Add to this approximately 3,000 bytes per device type for reentrant communications control routines. IBM - Binary Synchronous Control (BSC) routine requires 2,000 bytes extra and CRT display devices require 1,000 bytes extra.

SERVICES SUPPORTED

UNIVAC 1004/9000 Control Routine

UNIVAC DCT-2000 Control Routine (ASCII & XS3)

Teletypewriter Control Routine

Uniscope 100 Control Routine

UNIVAC DCT-1000 Control Routine

IBM BSC Control Routine

DCT-500 Control Routine

MODES OF PROCESSING SUPPORTED

Batch Terminal

Demand

Real-Time Service

Elements of Software Package

The software support provided for the C/SP falls into three categories:

1. Programs operating under the 1100 series operating system.
2. Modifications and additions to the 1100 series operating system.
3. C/SP resident programs

The number of elements comprising the Software Packages supporting the C/SP are too numerous to permit detailed descriptions in this document. They are present here in our line form so that their completeness may be appreciated and their inter-relatedness better comprehended.

1. Programs Operating under the 1100 Series Operating System
    a. UNIVAC C/SP Assembler
    b. C/SP Element Collector
    c. C/SP Program Test Simulator
    d. C/SP Service Routines
        (1) Initial Load of C/SP
        (2) Program Load of C/SP
        (3) Logging of Data for C/SP
        (4) Console Communications
    e. C/SP Symbionts
        (1) Input Symbiont
        (2) Output Symbiont
        (3) Exec Communications Symbiont
2. Modifications and additions to the 1100 Series Operating System
    a. C/SP Interface (C/SP Handler)
    b. The addition of New Executive Returns
    c. Addition of C/SP Parameter Tables
    d. C/SP Interrupt Answering routine
    e. C/SP Interrupt Processing routine
3. C/SP Resident Routines
    a. C/SP Operating System

        Terminal Management Supervisor

        Terminal Management Control Routine

        Communications Control Routines

Message Control Program

ICA Handler for C/SP Exec

Peripheral Control Program

Peripheral Control Routines

USER REQUIREMENTS

User requirements for those replacing current CTMC subsystems differ only slightly from those installing a new system. To implement the C/SP, the user would follow these procedures:

1. A new executive system would be generated. The remote device and communication line specifications would be designated in the manner presently used. The C/SP would be specified as the controlling device.
2. If the communication lines are controlled by a user supplied Real Time Program, this program would have to be reassembled. A parameter table, similar to the Line Terminal Table now used, would be included in this program. In addition, CTMC Executive Request Functions would be replaced by C/SP ER functions. These include:

INITIALIZE	CPS$
TERMINATE	CPT$
DIAL	CPD$
INPUT	CPI$
OUTPUT	CPO$
HANG UP	CPH$

3. The C/SP Operating System would be assembled on the host computer using the C/SP Assembler Program. The Macro's to be included in the system would be specifically called and the options permitted for each Macro would be specified as required for the users system. If input and output "own code" programs as a user supplied Master Control Program are to be used, they would be assembled at this time.
4. The assembler generated elements as well as C/SP elements stored in the executive systems library would be collected into a program. This program would then be stored on a random access device.
5. With the newly generated operating system in the 1100 system, a bootstrap operation would be requested of the host system from the C/SP. The resulting interrupt would be passed to the C/SP Handler in the Host Processor. The C/SP Handler would call the non-resident Initial Load of C/SP Service Routine which would, among other things, access the file in which the C/SP Operating System is stored and transfer it to the C/SP.

The software described in this outline will be available with initial deliveries of the system.

Questions & Answers

1. Q. Can C/SP communicate with an IBM BSC device?

   A. Yes.

2. Q. How many?

   A. Quantity is dependent on volume of work to be done in C/SP. Under normal loading conditions (C/SP handling one each reader, punch and printer, and MCP handling straight simple functions) the sustained throughput should approach 20,000 characters/second, which is equivalent to approximately 64 - 2400 bps lines.

3. Q. What reduction in host processor storage can be anticipated when using the C/SP?

   A. Typical savings can be exemplified by reference to 1110 symbiont/handlers which include:

DEVICE	# 1110 WORDS
DCT-500 TTY	2,000
DCT-1000	2,500
DCT-2000	2,500
U-100	2,500
U-300	2,500
1004/9000	2,500
Reader	240
Punch	250
Printer	350
Peripheral Control Routines	3,000
	18,340

The C/SP handler in the 1110 requires only 2,000 words of storage which effectively removes all of the above mentioned device handlers which may be required by the system configuration.

4. Q. What reduction in host processor execution time can be expected when a C/SP is used as a Communications Processor?

   A. Exact figures are not available, but an estimate of the number of instructions executed in support of a DCT-2000 input message of 80 characters is given below:

CTMC -- 1100 System	C/SP -- 1100 System
3340 Instructions	1706 Instructions

   Similar reductions can be expected for each type of device attached to the system. Increased performance can be achieved using the C/SP and blocking several input messages before transferring them to the host.

5. Q. How many I/O channels does the C/SP require on an 1100 System?

   A. One as opposed to two or more when the CTMC and 9300 are used.

6. Q. What facilities are provided for back-up in the C/SP?

   A. In those applications where the customer has a definite need for back-up facilities it is recommended that dual C/SP's be employed.

7. Q. What is the availability of the C/SP as a Communications Processor only?

   A. It will be available with initial 1110 deliveries. Second Quarter CY 72 for the 1106, 1108.

8. Q. What is the availability of the C/SP as a Symbiont Processor for the 1110?

   A. Second Quarter CY 72.

9. Q. When can the C/SP be demonstrated?

   A. Communications Processor for:

1106/1108	Second Quarter CY 71
1110	Second Quarter CY 71

   Symbiont Processor for:

1110	First Quarter CY 72

10. Q. What software will accompany initial deliveries of the C/SP?

    A. All software mentioned in the enclosed guide will be available for appropriate applications with first delivery of the C/SP.

11. Q. What is the minimum system configuration of a Communications Processor when used on an 1106 or 1108?

    A. Minimum system requirements for the Communications Processor when used on an 1106 or 1108 is as follows:

C/S Processor

32K Bytes Storage

1100 Channel Adapter

11. A. (Cont'd)

Special Device Channel with 80 cpm Reader

General Purpose Communications Channel

Appropriate Number of Communications Line Terminals

See minimum configurator "Communications Only"

Software support for the C/SP as a Communications Processor excludes those elements associated with peripheral control. Storage estimates are:

Operating system - 16,000 bytes

Each CCR added will require an allotment of storage indicated in the software section of this guide.