REFERENCE MANUAL

DATA LINE TERMINAL•5

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TABLE OF CONTENTS

1. GENERAL

The UNIVAC® Data Line Terminal-5 (DLT-5) is a high-speed data transmission terminal capable of full duplex, synchronous transmission of up to 4800 bits per second, used most frequently with the UNIVAC 1004 Card Processor. A UNIVAC 1004/DLT-5 complex may simultaneously send and receive up to 200 fully punched cards per minute. The received data may be printed, or punched, or printed and punched. Without the UNIVAC 1004 card punch, which operates at 200 cards per minute, the UNIVAC 1004/DLT-5 can simultaneously send and receive up to 400 fully punched cards per minute.

2. UNIVAC 1004

The UNIVAC 1004 is a powerful and highly efficient card processor. The 1004 utilizes a 400/600 card per minute reader, a 400/600 line per minute printer, and a cable-connected 200 card per minute punch. The system is controlled through a plugboard using the "wiring by exception" technique — utilizing a 961 character core memory, with an 8 microsecond cycle time. Included in the command structure is Add/Subtract, Compare, a complete set of edit commands, testing, branching, I/O etc. Multiply and Divide are via sub-routines. Most commands use the two address logic and all data is handled one character at a time. Introduction of the DLT-5 provides 1004 users with a powerful on-line, off-line communication system.

All input/output operations (read,

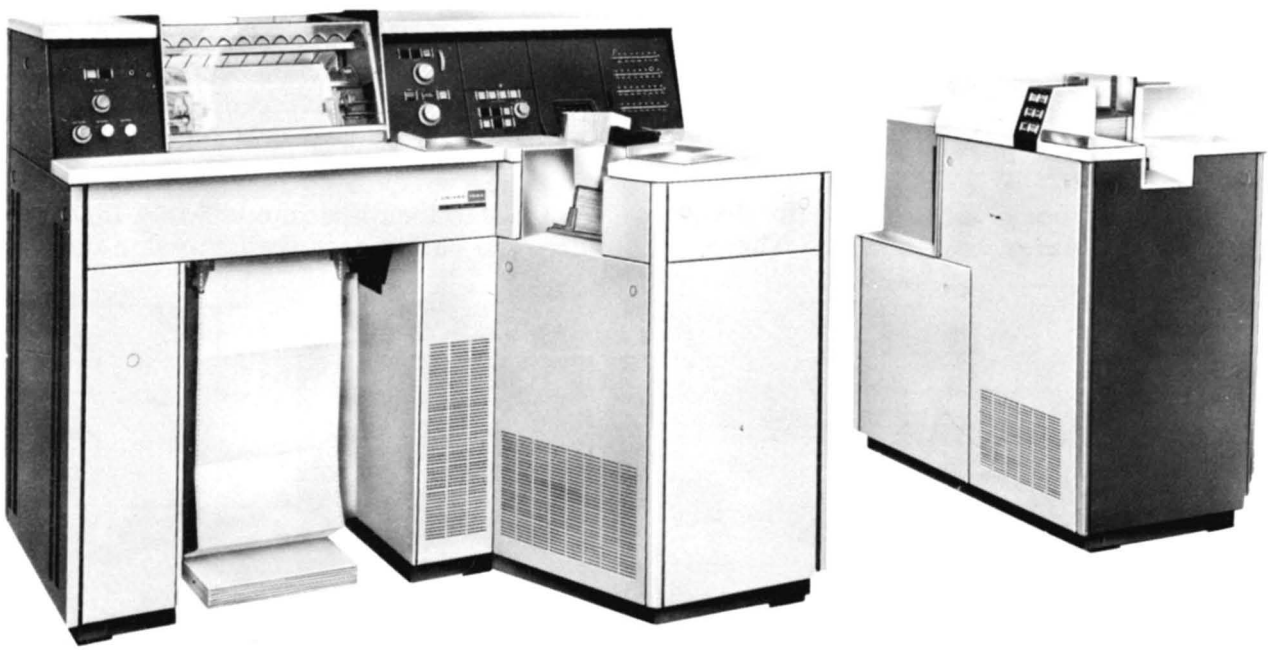


Figure 1
UNIVAC 1004 WITH PUNCH

print, punch) can occur concurrently. The reader, punch, and printer, however, may all be in operation simultaneously, but the data in and out of memory is handled on a time-share basis.

3. DATA LINE TERMINAL-5

The UNIVAC Data Line Terminal-5 transmits and receives data on a block-by-block basis, using synchronous transmission. A data block consists of 80 data characters preceded by a Start of Message (SOM) character and followed by End of Message (EOM) and Block Parity (B/P) characters. Transmission characters are 8 bits in length; 6 data bits, one control bit, and an odd parity bit. Each block transmission is completely protected by both character and block parity. The block parity character uses an even parity check for each longitudinal bit level in the data block.

The UNIVAC Data Line Terminal-5 is a free-standing unit with its own cabinetry, power supply and ventilation system. The logic module contains the communication character converters, magnetic core memory, and the associated control and timing circuitry.

Magnetic core memory is divided into four 80-character buffers. These buffers are assigned as an input pair and an output pair. During operation, buffer pairs alternate with each other to overlap block communication time with the time required to effect transfer with the Card Processor. As an example of this operation, assume that Buffer 1 Output, shown in Figure 4, contains the data block that has just been transmitted, and that Buffer 2 Output contains the next block to be transmitted. The first buffer cannot be erased until a response is received from the remote receiver. If that response is an ACKNOWLEDGE character, the contents of Buffer 2 Output are transmitted, while the next data block is transferred from the Card Processor into Buffer 1 Output. If the response is an ERROR character, the contents of Buffer 1 Output is retransmitted.

To illustrate input data, assume that Buffer 1 Input contains a complete data block that has just been received. When this block is checked and found to be error free, the ACKNOWLEDGE character is sent to the remote transmitter. While this data, contained in Buffer 1 Input, is being transferred to the UNIVAC 1004 Card Processor, Buffer 2 Input is already storing the first characters being received of the next data block.

The response characters for an input data block are immediately inserted into the output data transmission and are

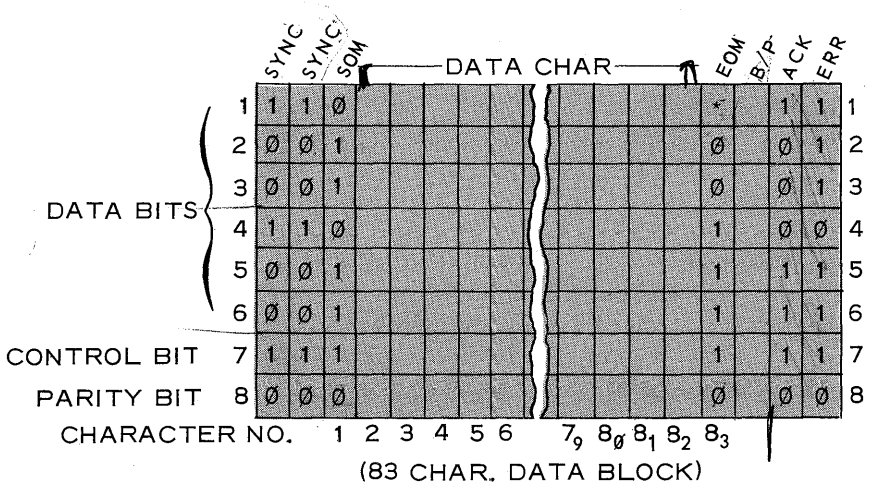


Figure 2

DATA BLOCK CONFIGURATION

Figure 3
DLT-5

not held until the output block is completed. The DLT-5 examines each input character for character parity check and determines if the received character is a data character or a response character which has been transmitted as the result of a completed output data block.

Receipt of an ACKNOWLEDGE character by a DLT-5 initiates transmission of the next output data block. If the response is an ERROR character, the data block will be retransmitted. Lack of a response within a predetermined time interval, after transmission of a data block, will cause the data block to be retransmitted. This time interval is normally 400 milliseconds but may be varied to be compatible with the particular propagation time of the associated communication circuit. The DLT-5 provides a check to prevent duplication of a data block due to the loss of the ACKNOWLEDGE character.

During periods when neither control characters or data characters are being transmitted, the DLT-5 will always transmit IDLE characters. The input portion of the DLT-5 expects to receive these IDLE characters from the remote transmitter when it is not receiving data or control characters. These IDLE char-

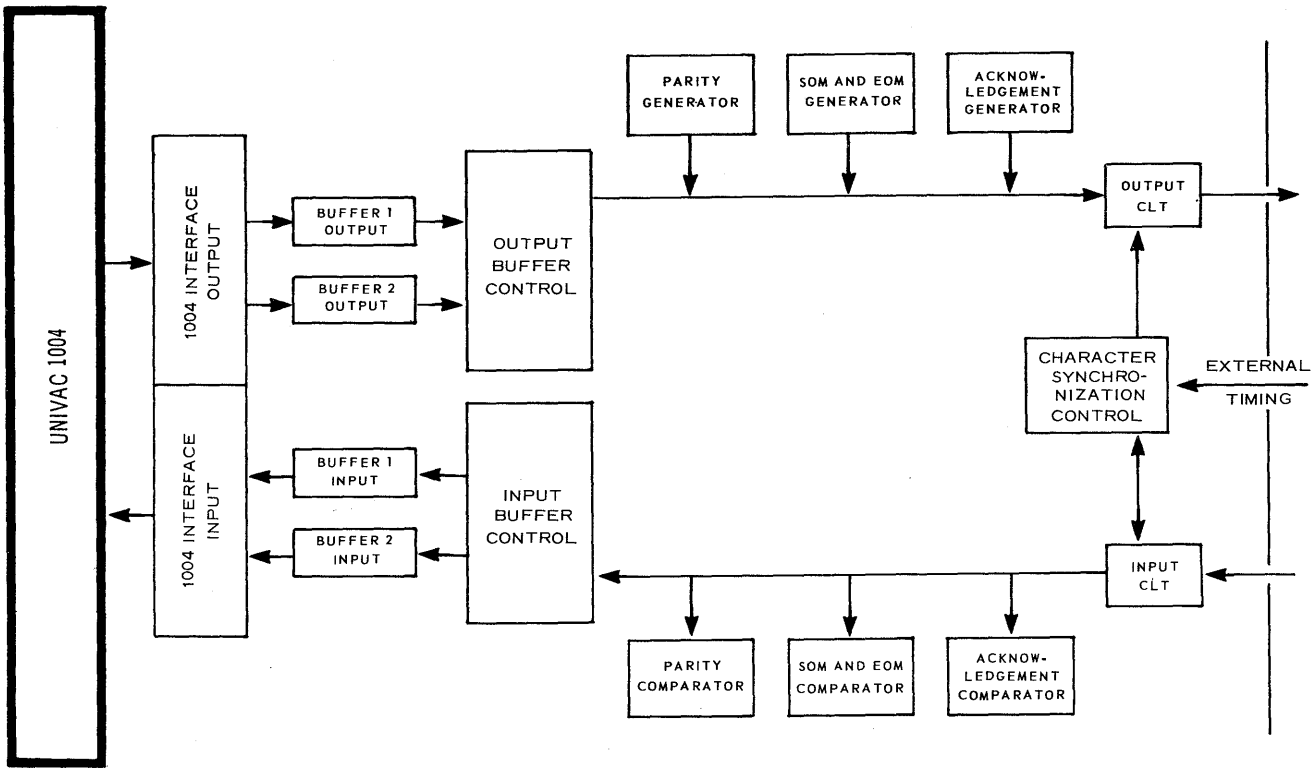


Figure 4

BLOCK DIAGRAM DLT-5

acters are utilized by the receiver to achieve and verify proper character synchronization.

The standard communication interface of the DLT-5 is in accordance with MIL STD 188B and is therefore compatible with the Government furnished communication equipment. This highly reliable interface comprises the following signal leads, as shown in Figure 6:

Figure 6:

a) Receive Data -
b) Send Data -
c) Receive Timing -
d) Send Timing -

The input impedance of the Receive Data circuit is 5000 ohms minimum and requires a maximum operating current of 100 micro-amperes. The input circuit

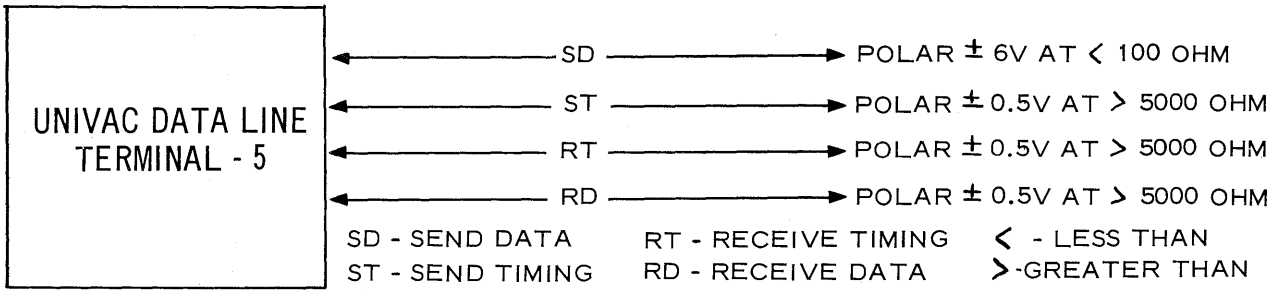


Figure 5

COMMUNICATION INTERFACE MIL STD 188B

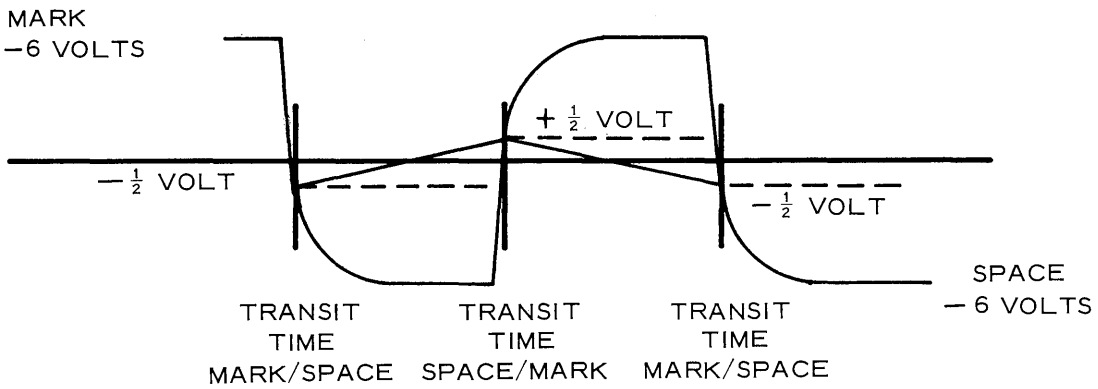


Figure 6
DISCRIMINATING LEVELS

sensitivity will provide correct operation on voltage excursions of plus/minus one-half volt. A positive voltage of at least one-half volt is interpreted as a marking (one) state. A negative voltage of at least one-half volt is interpreted as a spacing (zero) state. The Receive Data circuit operating differential is indicated in Figure 7.

The Send Data circuit has a source impedance of less than 100 ohms. Send signal levels are plus/minus six volts. Plus six volts is a marking (one) state and the minus six volts is a spacing (zero) state.

The assignment of the send and receive polarities may be interchanged, depending upon the requirements of the associated communication channel. It is assumed that the communication channel includes the security device and modulating-demodulating equipment, if either or both are provided.

The EIA standard interface, RS232A, is also available for compatibility to some commercial modulating-demodulating equipments.

All internal operations of the DLT-5 and an associated UNIVAC 1004 Card Processor are slaved to the external timing provided by the associated synchronous modulating–demodulating equipment. This design allows transmission rate modification to be performed by merely changing the external timing source, with absolutely no change to the UNIVAC 1004/DLT-5 complex.

4. TIMING

4.1 System Timing

The timing chart of Figure 7 shows the sequence of events when two UNIVAC 1004's are communicating with each other via the DLT-5 units. The lines drawn from one event to another, labeled A, B, C, and D, show the relationship of each with respect to the date being handled.

A – indicates when data is read from the card and sent to the DLT-5 at the time indicated.

B – indicates when the DLT-5 starts transmitting the data contained in its buffers.

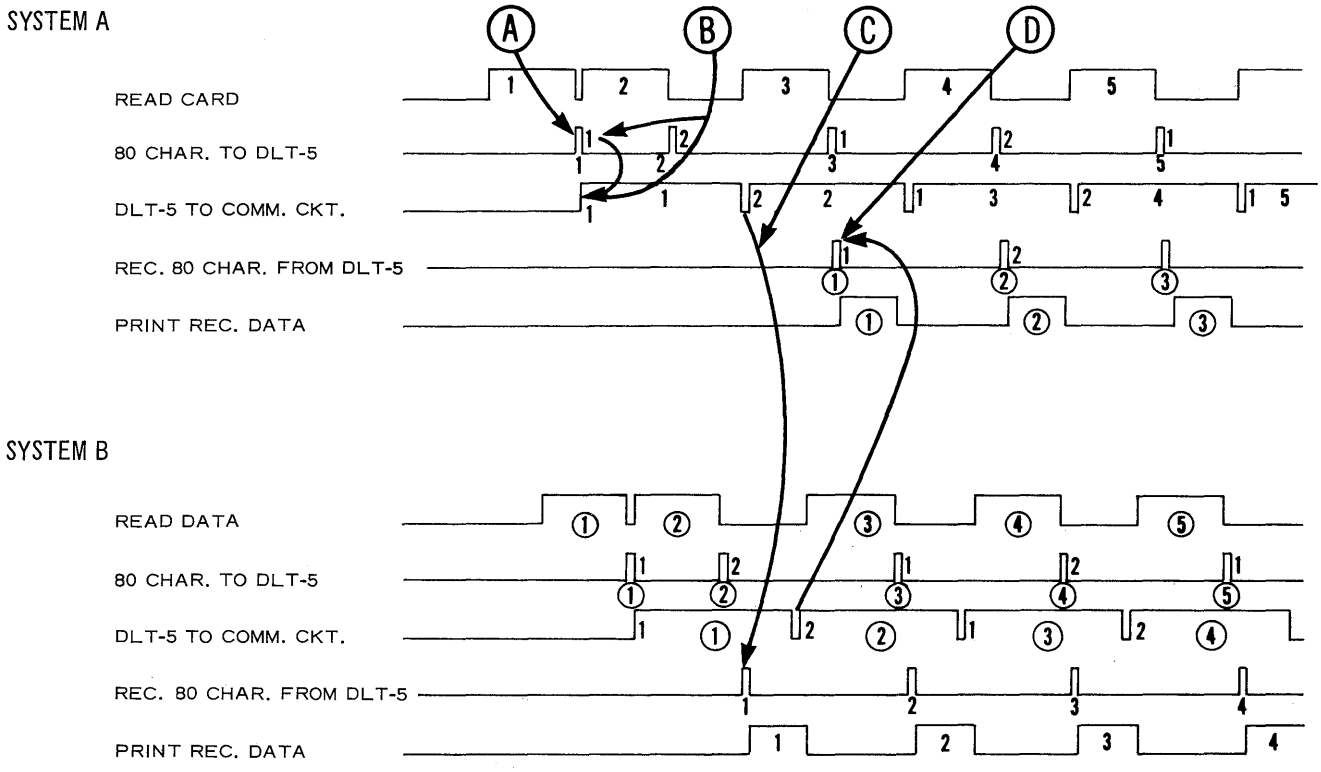
C – indicates when the other system (System B) transfers the data received by the DLT-5 to its UNIVAC 1004.

D – indicates when the print cycle can start, when data from the opposite system has been transferred to the system A 1004.

The transfer of data from the

Figure 7

TIMING CHART



UNIVAC 1004 to the DLT-5 or from the DLT-5 to the UNIVAC 1004 requires approximately 250 microseconds for an 80-character message.

For clarity, the sequence of operations has been prepared as it affects System A, with remarks regarding System B only when necessary.

Sequence of Operations

1) Since there is no message to receive from System B, System A 1004 reads one card. Data enters the read-in area of the 1004 memory.

2) The 1004 advances to the transmit step and sends all 80 characters just read from the card to the DLT-5 output buffer-one.

3) System A 1004 checks whether or not a message has been received from system B. The Buffer Read hub on the plugboard gives this indication.

4) Since there is no message to receive from system B, the 1004 of system A proceeds to read another card. Notice at this time, system B completes reading its first card, sends the data to its DLT-5 and proceeds to start transmitting that data to system

A; therefore, both systems are transmitting simultaneously.

5) After this second card has been read by system A, the card image is again sent to the DLT-5, but this time to output buffer-two. At this point, output buffer-one is being unloaded while output buffer-two is being loaded.

6) System A 1004 will again check to see if a message has been received from system B. Since the input buffer has not yet been loaded from system B there is no message in the input buffer.

7) System A 1004 will then check to see whether there is an output buffer available for loading from the 1004. Since the DLT-5 is still transmitting the first card image there will be no buffer available. The Buffer Write hub on the plugboard gives the Output Buffer Available indication.

8) System A 1004 will constantly repeat steps 6 and 7 until its DLT-5 completes transmission and an output buffer becomes available.

9) The system A 1004 will read the third card.

10) This third card image is transferred from the 1004 memory to the DLT-5 output buffer-one. Notice that the cards are alternately read into output buffer one and two.

11) At this point the 1004 program will again sample the Buffer Read hub. Since system B has now completely transferred its first message the hub will indicate that a message is available. The system A 1004 will now extract all 80 characters from input buffer-one of its DLT-5.

12) The data received in Step 11 is now printed.

13) At the completion of printing system A 1004 now checks to see whether another block of data has been received from system B. The next block has not yet been received.

14) System A 1004 now checks to see if an output buffer is available for another card read. There is no buffer available.

15) System A 1004 now loops through steps 13 and 14 until either an input buffer is filled or an output buffer becomes available. The first such occurrence is an output buffer becoming available.

16) The system A 1004 now reads the fourth card and transfers the card image to the DLT-5 output buffer-two.

17) During the reading of the fourth card the input buffer-two of system A DLT-5 completed its loading of data from system B DLT-5. After transferring the fourth card image to its DLT-5, system A 1004 now checks to see if an input buffer is available for transfer to the 1004.

18) Since data is available the system A 1004 will extract all 80 characters from the input buffer-two of its DLT-5.

19) The data received in Step 18 is now printed. At this point the cycle is repeated, going back to steps 13 through 19.

Figure 8
INTERNAL TIMING CHART

	PC0	PC1	PC2	PC3	PC4	PC5
INPUT SEQUENCE	TWO IL'S DECODED PC→1	SOM CORRECT PC→2 SOM ERROR PC→0	LINE→BUFFER EACH CHAR. RECV. MAR + 1→MAR AC + 1→AC PARITY ERROR DETECTED 1 → PE AC = 80 PC→3	EOM ERROR 1 → PE PC→4 EOM CORRECT PC→4	B/P ERROR 1 → PE PC→5 B/P CORRECT PC→5	PE = 1 ERR→LINE PC→1 PE = 0 NOREP = 1 ACK→LINE REQ→1004 SET ALT BUFFER PC→1 PE = 0 NOREP = 0 ACK→LINE PC→1
OUTPUT SEQUENCE	IL'S→LINE OR IS SET PC→1	SOM→LINE 0 → AC 0 → B/P PC→2	BUFFER→LINE EACH CHAR. TRANS. MAR + 1→MAR AC + 1→AC AC = 80 PC→3	EOM→LINE PC→4	B/P→LINE TIMER SET PC→5	IL→LINE ERR OR TIMER PC→1 ACK RECEIVED BUFFER CLEARED PC→0

LEGEND

PC	- PHASE COUNTER	PE	- PARITY ERROR REGISTER
IL	- IDLE CHARACTER	B/P	- BLOCK PARITY
SOM	- START OF BLOCK	REQ	- TRANSFER REQUEST
MAR	- MEMORY ADDRESS MESSAGE	ALT	- ALTERNATE
AC	- ADDRESS COUNTER	OR	- OUTPUT TRANSMISSION REQUEST
EOM	- END OF MESSAGE	NOREP	- NO REPEAT MESSAGE CHECK

4.2 Internal Timing

Internally, the UNIVAC Data Line Terminal-5 is controlled by six major phases. Since the device is full duplex, there are two independent phase counters which control the six phases for output and the six phases for input. The internal timing chart is presented in Figure 8.

Input Sequence

a) Phase Counter = 0

The input is attempting to establish character synchronization. Once character synchronization is established, the Phase Counter is incremented.

b) Phase Counter = 1

The input is looking for the Start of Message (SOM). If the SOM is decoded, the Phase Counter is incremented. If a character is received that is not an IDLE character or a control character, the Phase Counter is decremented (PC→0).

c) Phase Counter = 2

Each input character is placed in a buffer and the Memory Address Register (MAR) and the Address Counter (AC) are incremented by one. When the Address Counter (AC) equals 80, the Phase Counter is incremented. If any input character was found to have a parity error, then the Parity Error Flip-Flop (PE) is set to one. To prevent duplication of received blocks each character in the block is compared to the character in the same position in the previously received block and if they are

not the same the No Repeat Flip-Flop (NOREP) is set to one.

d) Phase Counter = 3

The input now looks for the EOM control character. If the EOM is in error, the PE is set to one and the Phase Counter incremented. If the EOM is correct, then the Phase Counter is incremented. Since the first bit of the EOM character alternates for every other message it is also compared with the EOM character of the previous block and if they are different the NOREP Flip-Flop is set to one if it had not already been set during Phase 2.

e) Phase Counter = 4

In this phase, the Block Parity character (B/P) is verified. If an error is found, PE is set to one. In either case, the Phase Counter is incremented.

f) Phase Counter = 5

In this phase, the response is sent to the remote transmitter. If the Parity Error Flip-Flop (PE) is set, an ERROR response is sent. The Phase Counter is set to one. If the Parity Error Flip-Flop (PE) is not set, an ACKNOWLEDGE response is sent and if the NOREP Flip-Flop is set to one an input transfer request is made to the associated UNIVAC 1004 Card Processor and the input buffer control toggles the other input buffer to the input line to receive the next data block. The Phase Counter is set to one.

Output Sequence

a) Phase Counter = 0

In this step, the output sends continuous IDLE (IL) characters to the line. When an output transmission request is set because an output buffer has been filled by the UNIVAC 1004, the Phase Counter is incremented.

b) Phase Counter = 1

A Start of Message (SOM) is sent to the line, the Address Counter (AC) is set to zero, and the Output Block Parity Register (B/P) is cleared to zero. The Phase Counter is incremented.

c) Phase Counter = 2

The buffer is transmitted to the line. As each character with parity is transferred from the buffer to the parallel-to-serial character converter, the Memory Address Register (MAR) and Address Counter (AC) are incremented. When the Address Counter (AC) is equal to 80, the Phase Counter is incremented.

d) Phase Counter = 3

The End of Message (EOM) is sent to the line and the Phase Counter is incremented.

e) Phase Counter = 4

In this phase, the Block Parity (B/P) character is sent to the line, the timer for a response is initiated, and the Phase Counter is incremented.

f) Phase Counter = 5

IDLE characters are sent constantly to the line. If an ERROR response is received or the timer interval elapses, the Phase Counter is set to one with respect to the same buffer. If an ACKNOWLEDGE response is received, the buffer is cleared and the Phase Counter is set to zero.

4.3 Buffer Sequencing

The sequence in which the two input and two output buffers are alternated back and forth might best be explained as follows with respect to Figure 9.

Assume that a pair of electronic switches has been assigned to each pair of I/O buffers. Since both input and output will function the same, only the input will be explained.

a) Switch 1 and 2 are for input Buffers 1 and 2. If Switch 1 and Switch 2 are both on, Buffer #1 will accept the next 80 characters from the UNIVAC 1004 and Buffer #2 is empty.

b) If Switch 1 and Switch 2 are both off, Buffer #1 is either in the process of being unloaded or was the last one to be loaded, and Buffer #2 is to be loaded with the next 80 character message from the UNIVAC 1004.

c) If Switch 1 is on and Switch 2 is off, Buffer # 1 will accept the next 80 character message from the 1004 and Buffer #2 is either in the process of being unloaded or was the last one to be loaded.

d) If Switch 1 is off and Switch 2 is on, Buffer #1 is either in the process of being unloaded or the last one to be loaded, and Buffer #2 will accept the next 80 character message from the UNIVAC 1004.

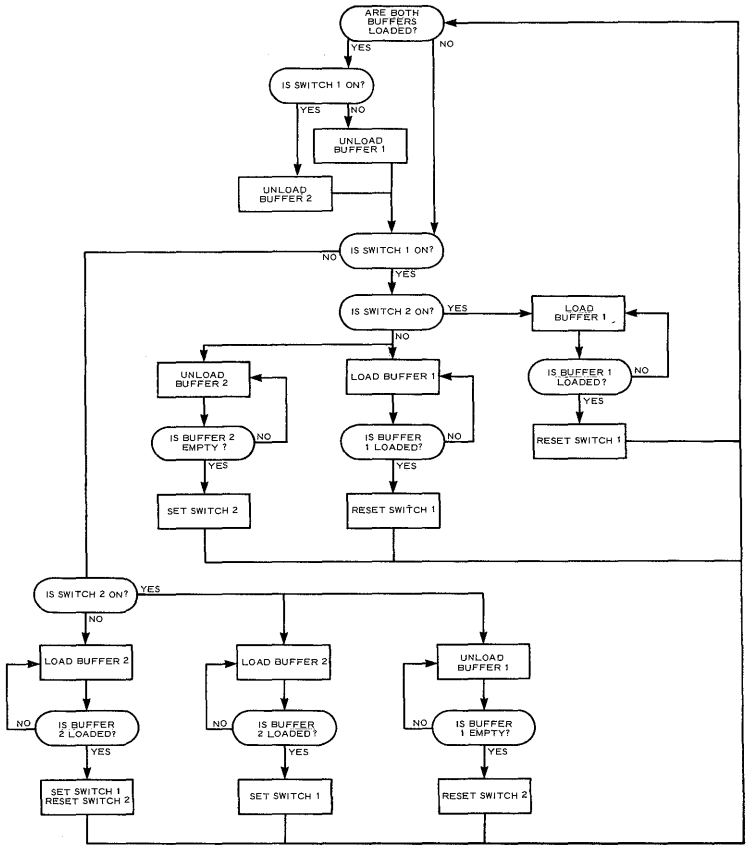
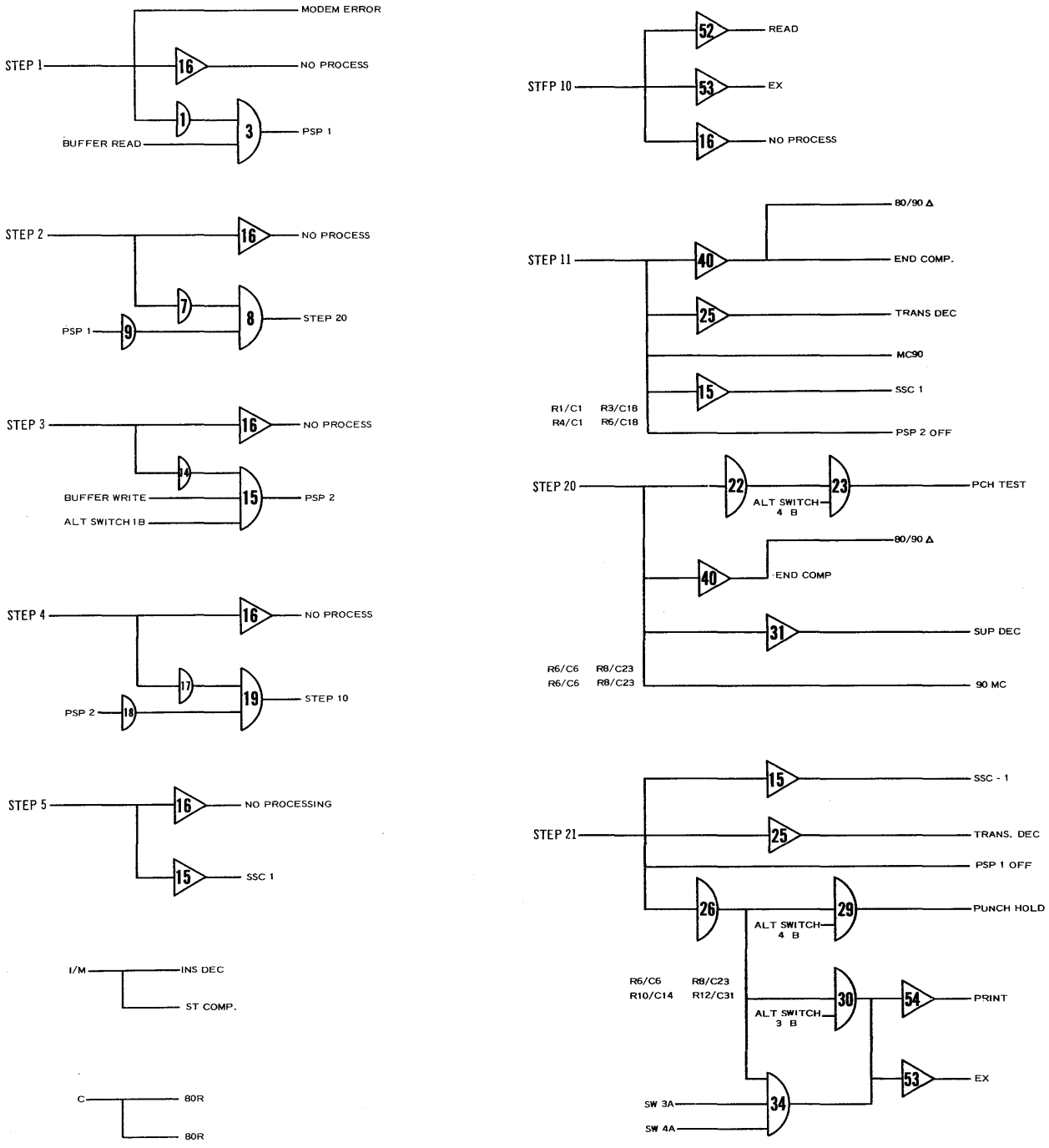


Figure 9

INPUT BUFFER SEQUENCING

Figure 10

Figure 10 also shows the plugboard wiring required for the UNIVAC 1004 to operate with the DLT-5.



5. PROGRAMMING

Since the DLT-5 is essentially a free-standing unit, programming via the UNIVAC 1004's plug board is negligible. The basic programmer's code chart explains the sequence of events used for the Timing Chart shown in Figure 7. Figure 10 will aid the reader in understanding the DLT-5 and, at the same time, it shows that the programmer need not be concerned with transmission errors, restart procedures, etc.

6. OPERATOR'S PANEL

The Operator's Panel for the DLT-5 is located on the upper front portion of the cabinet.

The following controls and indicators are provided.

1) Power On/Off

Switch light combination, when depressed one time, supplies power to the DLT-5 and light will glow. When depressed a second time, it will remove all power from the DLT-5.

2) Clear

When depressed, clears all pertinent registers and flip-flops. Buffer #1 Input indicator and Buffer #2 Output indicator will come on. Err, Sync, and Request indicators go off, and Control resets to first step for both input and output.

Buffer 1 and 2 Input Indicators

Buffer 1 will glow when either of the input buffers are available for loading from the line. Buffer 2 will glow when either of the input buffers are full, indicating the DLT-5 has data to send to the UNIVAC 1004.

Buffer 1 and 2 Output Indicators

Buffer 2 will glow when either of the output buffers are available for loading from the UNIVAC 1004. Buffer 1 will glow when either of the output buffers are full, indicating the DLT-5 is transmitting data.

Error

The error indicator will glow when a vertical parity error is detected, when the B/P characters do not match, or when the 82nd character is not the End of Message (EOM) character.

Sync

The Sync indicator will glow when the DLT-5 has achieved proper input character synchronization.

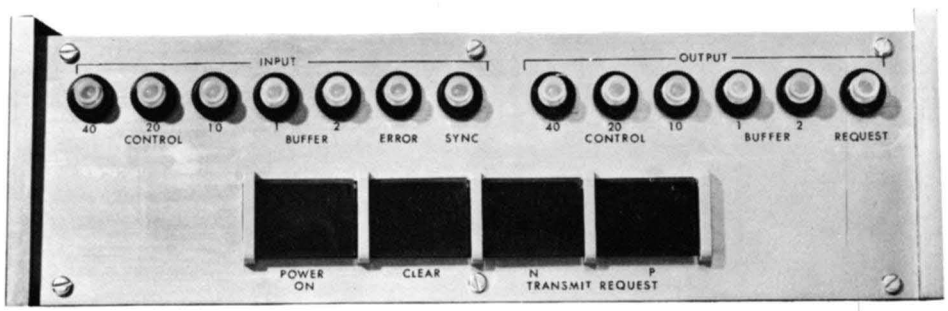


Figure 11
OPERATORS PANEL

Request

The Request indicator will glow when the UNIVAC 1004 is loading one of the DLT-5 output buffers.

Control Indicators

The DLT-5 operates in six basic phases, as described in detail in Section 4. These control indicators are labeled as 10, 20, and 40. The following table cross-references the control indicators with the Phase Counters:

PC	40	20	10
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1

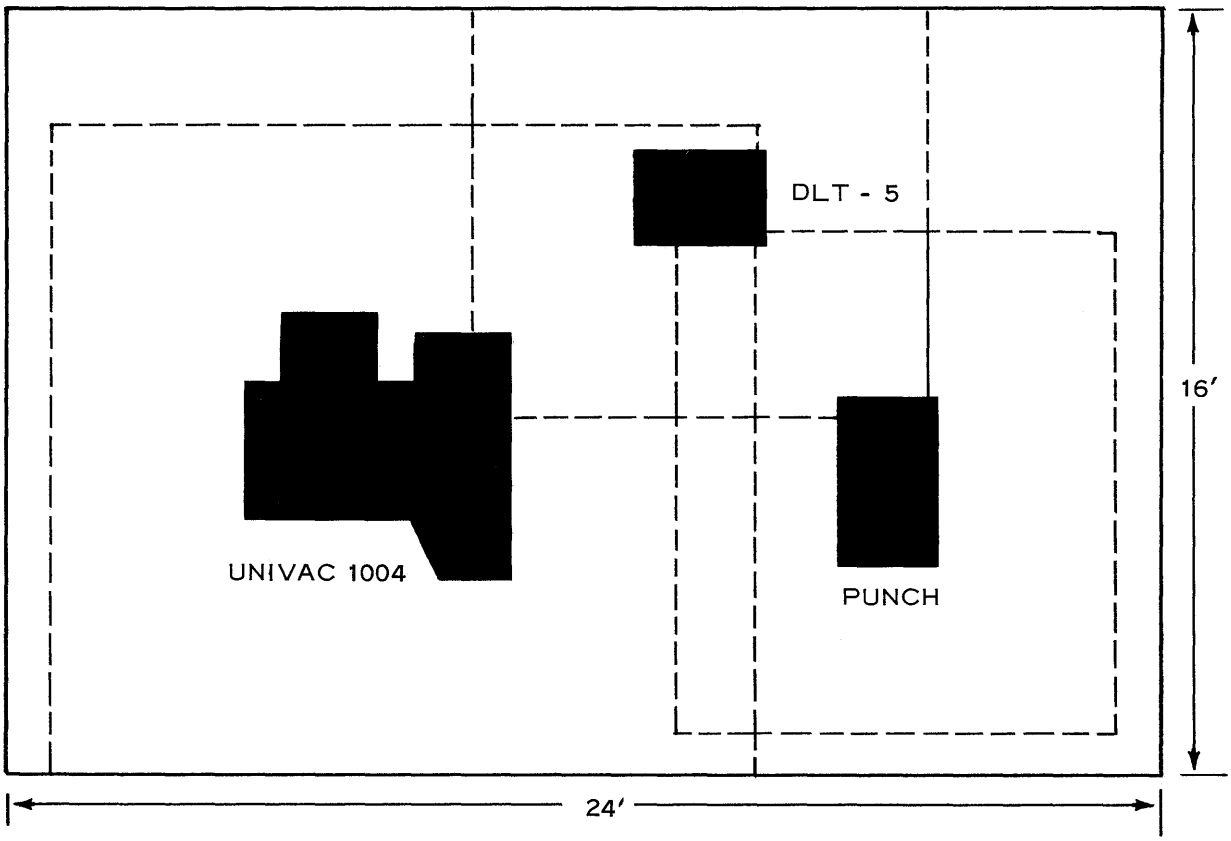


Figure 12
UNIVAC 1004/DLT-5 LAYOUT

7. INSTALLATION

As illustrated in Figure 12, the UNIVAC 1004/DLT-5 Complex may be installed in a minimum of 378 square feet for both operational and maintenance activities. The engineering design of the UNIVAC DLT-5 allows this unit to operate reliably without special air conditioning, special power, or site preparation. The following table presents the physical and environmental characteristics of the UNIVAC Data Line Terminal-5.

Dimensions	35" x 25" x 53"
Weight	600 pounds
Power Required	230 volt, 50/60 cycle, 10 amp circuit @ 1.5KVA
Maximum Operating-temperature	90° F.
Maximum Operating-humidity	85 % R.H.
BTU Dissipation	2350 BTU/hr.

UNIVAC

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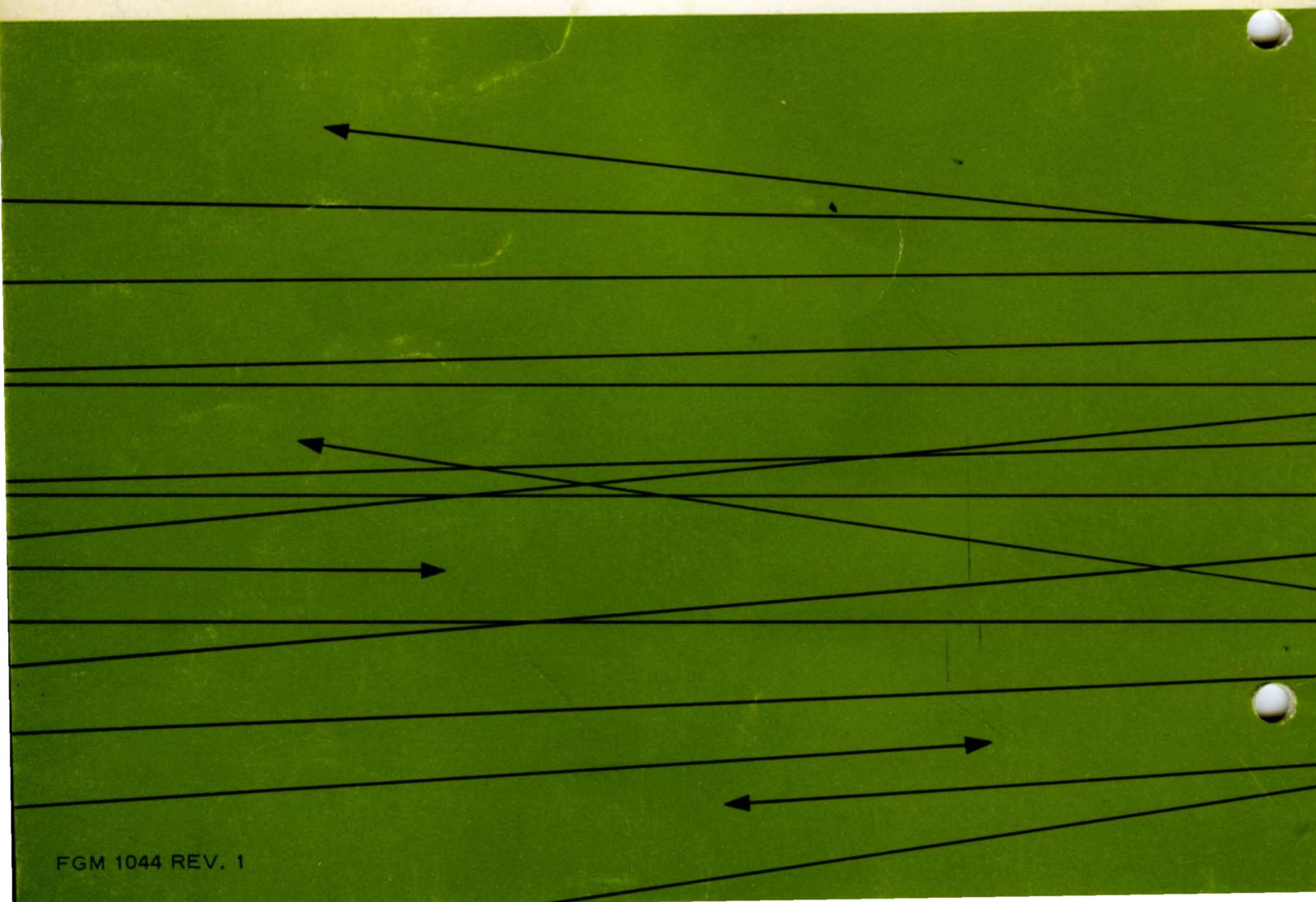

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