UMC

DATA BOOK

1986•1987

Microcomponent & Memory ICs

DATA BOOK

Microcomponent

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Memory ICs

MEDICAL APPLICATIONS

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The example of an applied circuit or combination with other equipment shown herein indicates characteristics and performance of semiconductor-applied products. The Company shall assume no responsibility for any problem involving a patent caused when applying the descriptions in the example.

UMC

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CROSS REFERENCE GUIDE

SRAM

UMC	UM2147	UM2148/UM2149	UM6167	UM6168
Synertek	SYP2147H	SYP2148H/SYP2149H	SYP2167	SYP2168
AMD	AM9247	AM2148/AM2149		AM99C68
Fujitsu	MBM2147H	MBM2148/MBM2149	MB8167A	MB8168
Intel	2147	2148/2149	2167	2168
Mostek	MK4104			
NS	NMC2147H	NMC2148H		
NEC	μPD2147		μPD4311	μPD4314
Toshiba	TMM315			
Hitachi		HM6148	HM6167	
T.I.	TMS2147H	TMS2149	TMS2167	TMS2168
Mitsubishi				

Mask ROM

UMC	UM2366/A	UM23128/A	UM23256/A
Synertek	SYP2365	SYP23128	SYP23256
AMD	AM9265	AM92128	
AMI	S2364	S23128	
G.I.	R0-3-9365	R0-9128	
Mostek	MK37000		MK38000
Motorola			MCM63256
NS			
NEC	μPD2364E	μPD23128A	μPD23256A
Signetics		26128A	
Toshiba	TMM2364P		TMM23256
Intel	2364A		

ORDERING INFORMATION

Microcomponent Products

Part Number	Clock (Speed)	Compatible Devices
UM8048-6	6MHz	Intel 8048-6
UM8035-6	6MHz	Intel 8035-6
UM8049-6	6MHz	Intel 8049-6
UM8039-6	6MHz	Intel 8039-6
UM8048-8	8MHz	Intel 8048-8
UM8035-8	8MHz	Intel 8035-8
UM8049-8	8MHz	Intel 8049-8
UM8039-8	8MHz	Intel 8039-8
UM8048-11	11MHz	Intel 8048-11
UM8035-11	11MHz	Intel 8035-11
UM8049-11	11MHz	Intel 8049-11
UM8039-11	11MHz	Intel 8039-11
UM8051/31	12MHz	Intel 8051/31
UM6502	1MHz	SYP6502
UM6502A	2MHz	SYP6502A
UM6502B	3MHz	SYP6502B
UM6502C	4MHz	
UM6507	1MHz	SYP6507
UM6507A	2MHz	SYP6507A
UM6512	1MHz	SYP6512
UM6512A	2MHz	SYP6512A
UM6512B	3MHz	SYP6512B
UM6845	1MHz	HD6845S
UM6845A	1.5MHz	HD68A45S
UM6845B	2MHz	HD68B45S
UM6845R	1MHz	SYP6845R
UM6845RA	2MHz	SYP6845RA
UM6845RB	3MHz	SYP6845RB
UM6845E	1MHz	SYP6845E
UM6845EA	2MHz	SYP6845EA
UM6845EB	3MHz	SYP6845EB
UM9007	–	CRT9007
UM8321A	30MHz	CRT9021A
UM8321B	28.5MHz	CRT(021B
UM8312	–	CRT9212
UM8272A	8MHz	FDC765A
UM8272A-4	4MHz	–
UM9228-1	–	–
UM8326	4MHz	FDC9216
UM8326B	8MHz	FDC9216B

*T: Clock

Part Number	Clock (Speed)	Compatible Devices
UM8329	8MHz	FDC9229
UM8329T	8MHz	FDC9229T
UM8329B	16MHz	FDC9229B
UM8329BT	16MHz	FDC9229BT
UM2661-1	Baud Rate 1	SYP2661-1
UM2661-2	Baud Rate 2	SYP2661-2
UM2661-3	Baud Rate 3	SYP2661-3
UM2681		MC2681 SCN2681 AC1N40
UM6520	1MHz	SYP6520
UM6520A	2MHz	SYP6520A
UM6521	1MHz	SYP6521
UM6521A	2MHz	SYP6521A
UM6522	1MHz	SYP6522
UM6522A	2MHz	SYP6522A
UM6532	1MHz	SYP6532
UM/532A	2MHz	SYP6532A
UM6551	1MHz	SYP6551
UM6551A	2MHz	SYP6551A
UM82C01	Interface with 1–11MHz 8048/49	–
UM82C55A	t_{RD} = 250 ns	HD82C55A
UM82C55A-5	t_{RD} = 200 ns	–
UM82C84A	8MHz	HD82C84A
UM82C84A-1	10MHz	–
UM82C88	–	HD82C88
UM8237A	3MHz	Intel 8237A
UM8237A-4	4MHz	Intel 8237A-4
UM8237A-5	4MHz	Intel 8237A-5
UM8253	2.6MHz	iP8253
UM8253-5	5MHz	iP8253-5
UM8254	8MHz	iP8254
UM8259A	t_{RHAX}=260ns	iP8259A
UM8259A-2	t_{RHAX}=235ns	iP8259A-2
UM8259A-8	t_{RHAX}=420ns	iP8259A-8

Memory Products

Part Number	Organization	Access Time (ns)	Max. Current (mA)		Synertek P/N
			Operating	Standby	
UM2332	4Kx8	450	100	–	–
UM2332-1	4Kx8	350	100	–	–
UM2332-2	4Kx8	250	100	–	–
UM2333	4Kx8	450	100	–	–
UM2333-1	4Kx8	350	100	–	–
UM2333-2	4Kx8	250	100	–	–
UM2364	8Kx8	450	100	–	SYP2364
UM2364-1	8Kx8	300	100	–	SYP2364-3
UM2364-2	8Kx8	200	100	–	SYP2364-2
UM2364A	8Kx8	450	100	12	SYP2364A
UM2364A-1	8Kx8	300	100	12	SYP2364A-3
UM2364A-2	8Kx8	200	100	12	SYP2364A-2
UM2366	8Kx8	450	100	–	SYP2365
UM2366-1	8Kx8	300	100	–	SYP2365-3
UM2366-2	8Kx8	200	100	–	SYP2365-2
UM2366A	8Kx8	450	100	12	SYP2365A
UM2366A-1	8Kx8	300	100	12	SYP2365A-3
UM2366A-2	8Kx8	200	100	12	SYP2365A-2
UM23128	16Kx8	450	100	–	SYP23128
UM23128-1	16Kx8	300	100	–	SYP23128-3
UM23128-2	16Kx8	200	100	–	SYP23128-2
UM23128A	16Kx8	450	100	10	SYP23128A
UM23128A-1	16Kx8	300	100	10	SYP23128A-3
UM23128A-2	16Kx8	200	100	10	SYP23128A-2
UM23256	32Kx8	450	100	–	SYP23256
UM23256-1	32Kx8	300	100	–	SYP23256-3
UM23256-2	32Kx8	200	100	–	SYP23256-2
UM23256A	32Kx8	450	100	10	SYP23256A
UM23256A-1	32Kx8	300	100	10	SYP23256A-3
UM23256A-2	32Kx8	200	100	10	SYP23256A-2
UM6104	1Kx4	250	7	0.01	–
UM6104-2	1Kx4	200	7	0.01	–
UM6104-3	1Kx4	150	7	0.01	–
UM6104-4	1Kx4	120	7	0.01	–
UM6104-1	1Kx4	2000	5	0.003	–
UM6104J	1Kx4	250	7	0.01	–
UM6104J-2	1Kx4	200	7	0.01	–
UM6104J-3	1Kx4	150	7	0.01	–
UM6104J-4	1Kx4	120	7	0.01	–
UM6114	1Kx4	90	40	0.20	–
UM6114-1	1Kx4	70	30	0.02	–
UM6114-2	1Kx4	55	30	0.02	–
UM6114-3	1Kx4	45	30	0.02	–

Part Number	Organization	Access Time (ns)	Max. Current (mA)		Synertek P/N
			Operating	Standby	
UM6114J†	1Kx4	90	40	0.02	–
UM6114J-1	1Kx4	70	30	0.02	–
UM6114J-2	1Kx4	55	30	0.02	–
UM6114J-3	1Kx4	45	30	0.02	–
UM6116-2	2Kx8	120	100	0.5	–
UM6116-3	2Kx8	90	100	0.5	–
UM6116-4	2Kx8	70	100	0.05	–
UM6116-5	2Kx8	55	100	0.05	–
UM6116J-2	2Kx8	120	100	0.5	–
UM6116J-3	2Kx8	90	100	0.5	–
UM6116J-4	2Kx8	70	100	0.05	–
UM6116J-5	2Kx8	55	100	0.05	–
UM6164-2	8Kx8	45	100	10	–
UM6164-1	8Kx8	55	100	10	–
UM6164	8Kx8	70	100	10	–
UM6167	16Kx1	70	60	2	–
UM6167-1	16Kx1	55	60	2	–
UM6167-2	16Kx1	45	60	2	–
UM6167L	16Kx1	70	50	0.05	–
UM6167L-1	16Kx1	55	50	0.05	–
UM6167L-2	16Kx1	45	50	0.05	–
UM6168	4Kx4	70	90	2	–
UM6168-1	4Kx4	55	90	2	–
UM6168-2	4Kx4	45	90	2	–
UM6168L	4Kx4	70	90	0.05	–
UM6168L-1	4Kx4	55	90	0.05	–
UM6168L-2	4Kx4	45	90	0.05	–
UM2147	4Kx1	70	160	20	SYP2147H
UM2147-1	4Kx1	55	180	30	SYP1147H-3
UM2147-2	4Kx1	45	180	30	SYP2147H-2
UM2147L	4Kx1	70	140	15	SYP2147HL
UM2147L-1	4Kx1	55	125	15	SYP2147HL-3
UM2148	1Kx4	70	150	30	SYP2148H
UM2148-1	1Kx4	55	150	30	SYP2148H-3
UM2148-2	1Kx4	45	150	30	SYP2148H-2
UM2148L	1Kx4	70	125	20	SYP2148HL
UM2148L-1	1Kx4	55	125	20	SYP2148HL-3
UM2149	1Kx4	70	150	–	SYP2149H
UM2149-1	1Kx4	55	150	–	SYP2149H-3
UM2149-2	1Kx4	45	150	–	SYP2149H-2
UM2149L	1Kx4	70	125	–	SYP2149HL
UM2149L-1	1Kx4	55	125	–	SYP2149HL-3

†: Ceramic Package

UMC

Mask ROM

Selection Guide

Part No.	Descriptions	Compatible Devices	Remarks	Page
UM2332	4Kx8 NMOS ROM (2532)	μPD 2332	Access Time 450, 350, 250 ns	1–3
UM2333	4Kx8 NMOS ROM (2732)	AM 9233	Access Time 450, 350, 250 ns	1–6
UM2364	8Kx8 NMOS ROM (2564)	SYP 2364	Access Time 450, 300, 200 ns	1–9
UM2366/A	8Kx8 NMOS ROM (2764)	SYP 2366	Access Time 450, 300, 200 ns	1–12
UM23128/A	16Kx8 NMOS ROM (27128)	SYP23128	Access Time 450, 300, 200 ns	1–15
* UM23256/A	32Kx8 NMOS ROM (27256)	SYP 23256	Access Time 450, 300, 200 ns	1–18

* Under Development

UM2332

4K × 8 NMOS ROM

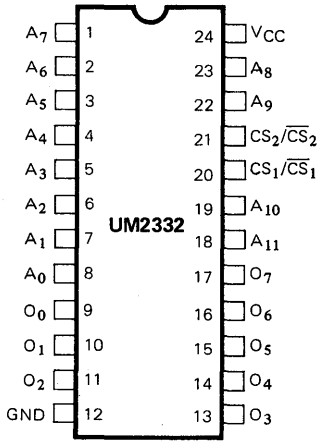
Features

- Access time 250/350/450ns (max.)
- Single +5V ±10% power supply
- TTL compatible inputs and outputs
- Three-state outputs
- Pin compatible with 2532 EPROM
- Two programmable chip selects for output control
- N-channel silicon gate technology

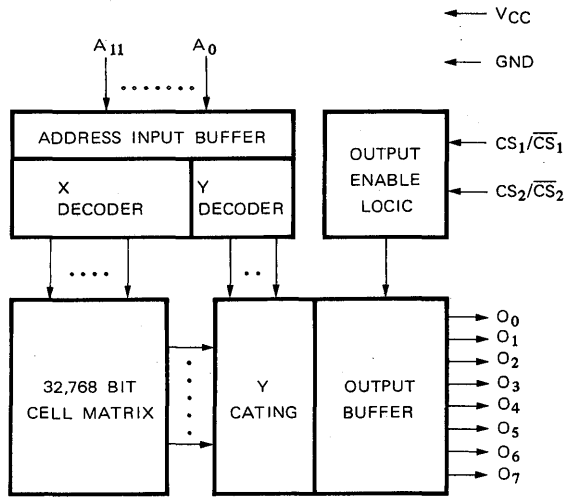
General Description

The UM2332 is a 32,768-bit static MOS read only memory organized as 4096 words by 8 bits. The device is completely static in operation, and operates from a single +5V power supply. All inputs and outputs are TTL compatible. The two chip select inputs are programmable. Programming of the device is accomplished by a custom masking process. The UM2332 is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Ambient temperature under bias, T_A . . . . . −10 to +80°C

Storage temperature, T_{STG} . . . . . −65 to +150°C

Applied voltage on any pin with respect to ground . . . . . −0.5 to +7V

Power dissipation, P_D 1.0W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Electrical Characteristics

(T_A = 0 to 70°C, V_{CC} = 5V ± 10% unless otherwise specified)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
V_{IL}	Input low voltage	−.05		0.8	V	
V_{IH}	Input high voltage	2.0		V_{CC}	V	
V_{OL}	Output low voltage			0.4	V	I_{OL} = 2.1mA
V_{OH}	Output high voltage	2.4		V_{CC}	V	I_{OH} = −400μA
I_{LI}	Input load current			10	μA	V_{IN} = V_{CC} = 5.25V
I_{LO}	Output leakage current			10	μA	V_{OUT} = V_{CC} = 5.25V
I_{CC}	V_{CC} current			100	mA	

Capacitance

(T_A = 25°C f = 1.0MHz)

Symbol	Parameter	Limits		Unit	Test Conditions
		Typ.	Max.		
C_{IN}	Input capacitance		7	pF	All pins except pin under tied to AC ground
C_{OUT}	Output capacitance		10	pF	

Note:

This parameter is periodically sampled and is not 100% tested.

A.C. Electrical Characteristics

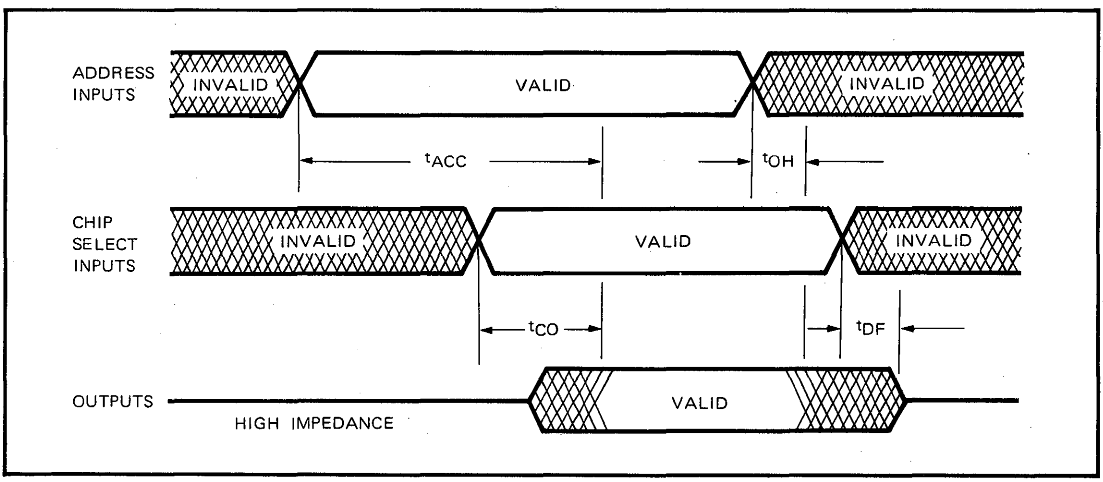
(T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	UM2332		UM2332-1		UM2332-2		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACC}	Address access time 1		450		350		250	ns
t_{CO}	Output enable delay from $CS_1/\overline{CS_1}$ or $CS_2/\overline{CS_2}$		150		120		120	ns
t_{DF}	Output disable delay from $CS_1/\overline{CS_1}$ or $CS_2/\overline{CS_2}$	0	100	0	100	0	100	ns
t_{OH}	Output hold from address change	10		10		10		ns

Test Conditions

Output load .... 1 TTL load and 100pF
Input transition time 20ns
Timing reference levels .... Input = 1.5V, Output = 0.8V and 2.0V

Timing Diagram



Ordering Information

Part Number	Access Time	Package
UM2332	450ns	Plastic
UM2332-1	350ns	Plastic
UM2332-2	250ns	Plastic

UMC

UM2333

4K × 8 NMOS ROM

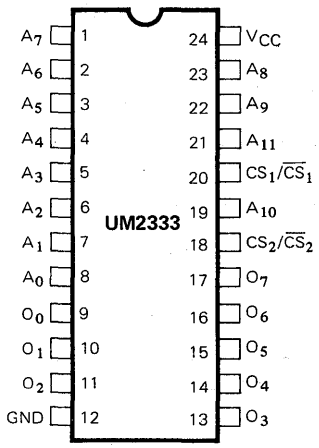
Features

- Access time 250/350/450ns (max.)
- Single +5V ±10% power supply
- TTL compatible inputs and outputs
- Three-state outputs
- Pin compatible with 2732 EPROM
- Two programmable chip selects for output control
- N-channel silicon gate technology

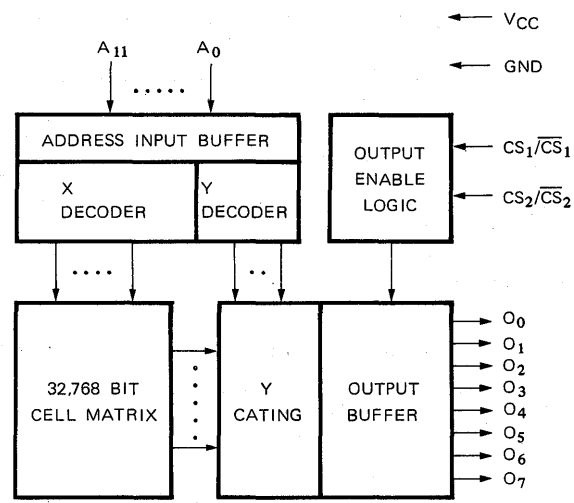
General Description

The UM2333 is a 32,768-bit static MOS read only memory organized as 4096 words by 8 bits. The device is completely static in operation, and operates from a single +5V power supply. All inputs and outputs are TTL compatible. The two chip select inputs are programmable. Programming of the device is accomplished by a custom masking process. The UM2333 is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Ambient temperature under bias, T_A . . . . . −10 to +80°C

Storage temperature, T_{STG} . . . . . −65 to +150°C

Applied voltage on any pin with respect to ground . . . . . −0.5 to +7V

Power dissipation, P_D 1.0W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Electrical Characteristics

(T_A = 0 to 70°C, V_{CC} = 5V ± 10% unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
V_{IL}	Input low voltage		−.05		0.8	
V_{IH}	Input high voltage		2.0		V_{CC}	V
V_{OL}	Output low voltage	I_{OL} = 2.1mA			0.4	V
V_{OH}	Output high voltage	I_{OH} = −400μA	2.4		V_{CC}	V
I_{LI}	Input load current	V_{IN} = V_{CC} = 5.25V			10	μA
I_{LO}	Output leakage current	V_{OUT} = V_{CC} = 5.25V			10	μA
I_{CC}	V_{CC} current				100	mA

Capacitance

(T_A = 25°C f = 1.0MHz)

Symbol	Parameter	Test Conditions	Limits		Unit
			Typ.	Max.	
C_{IN}	Input capacitance	All pins except pin under tied to AC ground		7	pF
C_{OUT}	Output capacitance			10	pF

Note:
This parameter is periodically sampled and is not 100% tested.

A.C. Electrical Characteristics

(T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	UM2333		UM2333-1		UM2333-2		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACC}	Address access time 1		450		350		250	ns
t_{CO}	Output enable delay from $CS_1/\overline{CS_1}$ or $CS_2/\overline{CS_2}$		150		120		120	ns
t_{DF}	Output disable delay from $CS_1/\overline{CS_1}$ or $CS_2/\overline{CS_2}$	0	100	0	100	0	100	ns
t_{OH}	Output hold from address change	10		10		10		ns

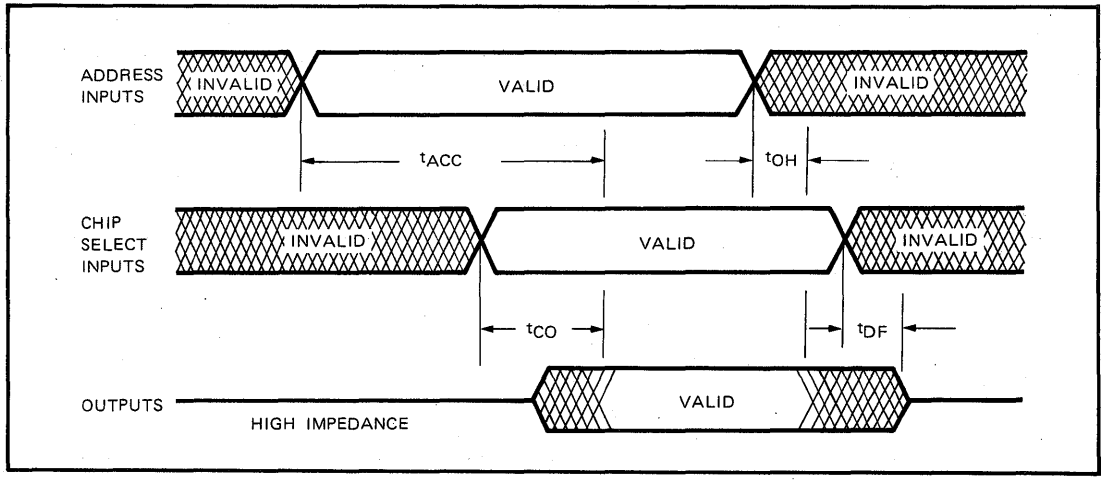
Test Conditions

Output load . . . . . 1 TTL load and 100pF

Input transition time 20ns

Timing reference levels . . . . . Input = 1.5V, Output = 0.8V and 2.0V

Timing Diagram



Ordering Information

Part Number	Access Time	Package
UM2333	450ns	Plastic
UM2333-1	350ns	Plastic
UM2333-2	250ns	Plastic

UM2364/UM2364A

8K × 8 NMOS ROM

Features

- 8192 x 8 Bit organization
- Single +5 Volt Supply
- Access Time – 200/300/450 ns (max.)
- Totally static operation
- Completely TTL compatible
- 24 Pin JEDEC approved pinout
- UM2364A – Automatic power down ($\overline{CE}$)
- UM2364 – non power down version
  – programmable chip select (CS)
- Three state outputs for wire-OR expansion
- EPROMs accepted as program data input
- 2564 EPROM compatible

General Description

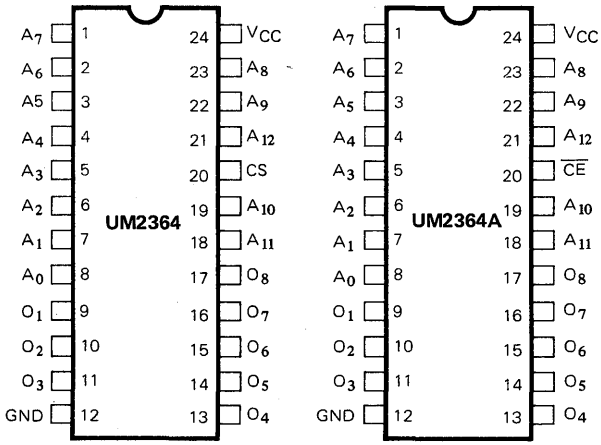
The UM2364 and UM2364A high performance Read Only Memories are organized 8192 words by 8 bits with access times from 200 ns to 450 ns. The ROMs are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. Both ROMs conform to the JEDEC approved pinout for 24 pin 64K ROMs.

The UM2364 offers the simplest operation (no power down.) Its programmable chip select allows two 64K ROMs to be OR-tied without external decoding.

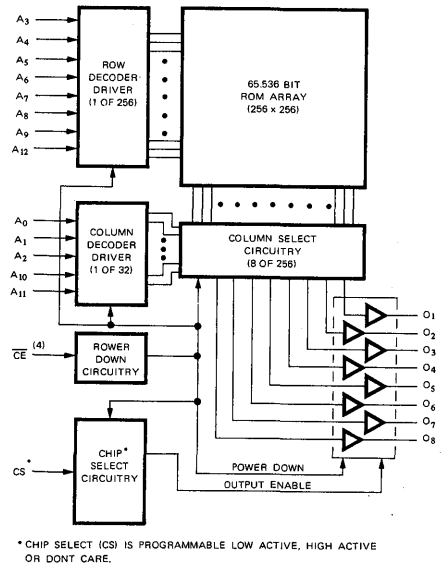
The UM2364A offers an automatic power down feature. Power down is controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes high, the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$ remains high. This unique feature provides system level power savings as much as 90%.

Both the UM2364 and UM2364A are pin compatible with the 2564 EPROM thus eliminating the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

Pin Configuration



Block Diagram



*CHIP SELECT (CS) IS PROGRAMMABLE LOW ACTIVE, HIGH ACTIVE OR DONT CARE.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . −10°C to 80°C
Storage Temperature . . . . . −65°C to 150°C
Voltage on Any Pin with Respect to Ground . . . . . −0.5V to +7V
Power Dissipation 1.0W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

(T_A = 0°C to +70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OH}	Output HIGH Level	2.4		V_{CC}	V	I_{OH} = −1.0 mA
V_{OL}	Output LOW Level			0.4	V	I_{OL} = 3.2 mA
V_{IH}	Input HIGH Level	2.0		V_{CC}	V	
V_{IL}	Input LOW Level	−0.5		0.8	V	
I_{LI}	Input Leakage Current			10	μA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 0V to V_{CC}
I_{CC}	Operating Supply Current			100	mA	Note 1
I_{SB}	Standby Supply Current			12	mA	Note 2
I_{OS}	Output Short Circuit Current			90	mA	Note 3

Capacitance

(T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_I	Input Capacitance		5	pf	V_{IN} = 0V
C_O	Output Capacitance		5	pf	V_{OUT} = 0V

Note: This parameter is periodically sampled and is not 100% tested.

A.C. Characteristics

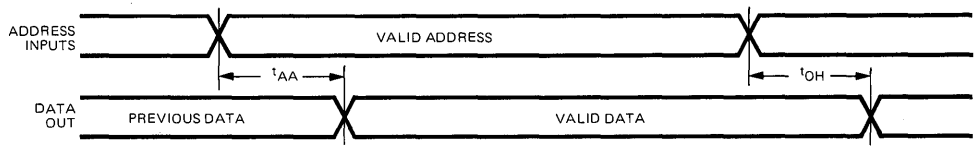
(T_A = 0°C to +70°C, V_{CC} = +5V ± 10%) (Note 7)

Symbol	Parameter	UM2364-2 UM2364A-2		UM2364-1 UM2364A-1		UM2364 UM2364A		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CYC}	Cycle Time	200		300		450		ns	
t_{AA}	Address Access Time		200		300		450	ns	
t_{OH}	Output Hold After Address Change	10		10		10		ns	
t_{ACE}	Chip Enable Access Time		200		300		450	ns	Note 4
t_{ACS}	Chip Select Access Time		85		100		150	ns	
t_{LZ}	Ouput LOW Z Delay	10		10		10		ns	Note 5
t_{HZ}	Output HIGH Z Delay		85		100		150	ns	Note 6
t_{PU}	Power Up Time	0		0		0		ns	Note 4
t_{PD}	Power Down Time		85		100		150	ns	Note 4

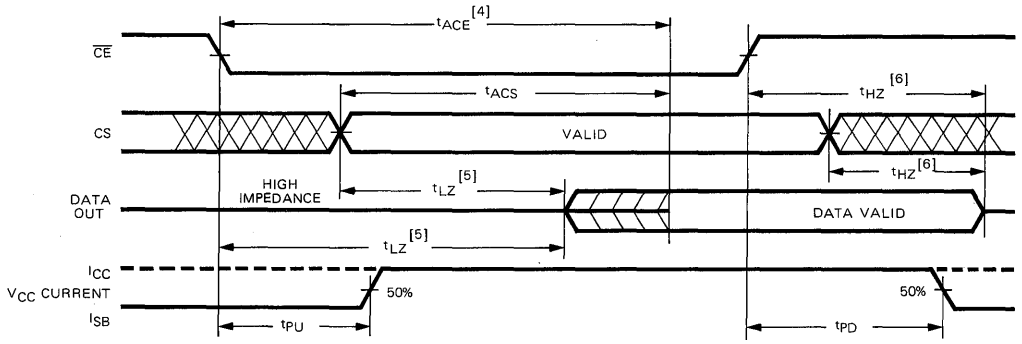
Notes:
1. Measured with device selected and outputs unloaded.
2. Applies to "A" versions only and measured with $\overline{CE}$ = 2.0V
3. For a duration not to exceed one second.
4. Applies to "A" versions (power down) only.
5. Output low impedance delay (t_{LZ}) is measured form $\overline{CE}$ going low or CS going active.
6. Output high impedance delay (t_{HZ}) is measured from $\overline{CE}$ going high or CS going inactive.
7. A minimum 0.5 ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved.

Timing Diagrams

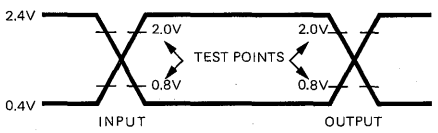
Propagation Delay from Address ($\overline{CE}$ LOW or CS = Active)



Propagation Delay from Chip Enable, Chip Select (Address Valid)



A.C. Testing Input, Output Waveform



AC TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.4V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0". INPUT PULSE RISE AND FALL TIMES ARE 5 ns.

A.C. Testing Load Circuit

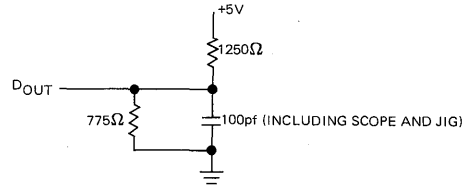


Figure 1.

Programming Instructions

All UMC Read Only Memories (ROM) utilize computer asided techniques to manufacture and test custom bit patterns. The customer's bit pattern and address information can be supplied to UMC in a number of different ways. UMC can process customer inputs in EPROM, ROM, PROM, paper tape, and computer punched cards. Contact your UMC sales representative for complete details on each of the various data input formats.

Programming instructions are listed at the end of the Memory Section.

Package Availability

Ordering Information

Order Number	Access Time	Operating Current	Standby Current	Package Type
UM2364	450 ns	100 mA	N.A.*	Plastic
UM2364-1	300 ns	100 mA	N.A.	Plastic
UM2364-2	200 ns	100 mA	N.A.	Plastic
UM2364A	450 ns	100 mA	12mA	Plastic
UM2364A-1	300 ns	100 mA	12 mA	Plastic
UM2364A-2	200 ns	100 mA	12 mA	Plastic

* Not Applicable.

UM2366 / UM2366A

8K × 8 NMOS ROM

Features

- 2765 EPROM pin compatible
- 8192 x 8 bit organization
- Single + 5 volt supply
- Access time – 200/300/450 ns (max)
- Totally static operation
- Completely TTL compatible
- 28 Pin JEDEC approved pinout
- UM2366A – automatic power down ($\overline{CE}$)
  - output enable function ($\overline{OE}$)
  - two programmable chip selects (CS)
- UM2366 – non power down version
  - four programmable chip selects (CS)
- Three state outputs for wire-or expansion
- EPROMs accepted as program data input

Description

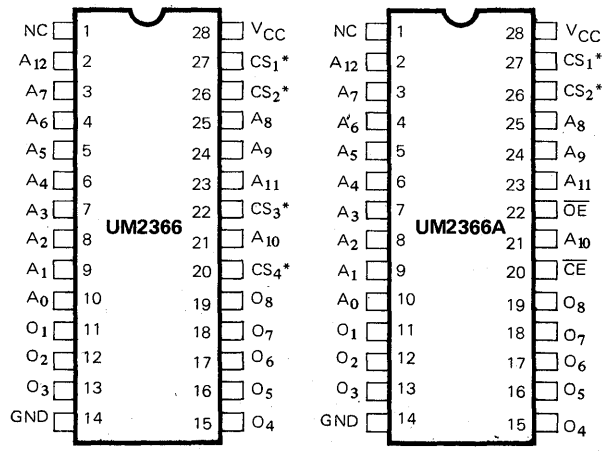
The UM2366 and UM2366A high performance Read Only Memories are organized 8192 words by 8 bits with access times from 200 ns to 450 ns. The ROMs are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. Both ROMs conform to the JEDEC approved pinout for 28 pin 64K ROMs.

The UM2366 offers the simplest operation (no power down.) Its four programmable chip selects allow up to sixteen 64K ROMs to be OR-tied without external decoding.

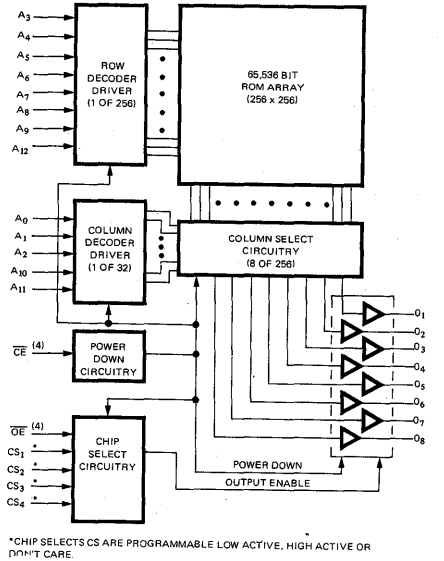
The UM2366A offers an automatic power down feature. Power down is controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes high, the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$ remains high. This unique feature provides system level power savings as much as 90%. An additional feature of the UM2366A is the Output Enable ($\overline{OE}$) function. This eliminates bus contention in multiple bus microprocessor systems. The two programmable Chip Selects (CS) allow up to four 64K ROMs to be OR-tied without external decoding.

Both the UM2366 and UM2366A are pin compatible with the 2764 EPROM thus eliminating the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

Pin Configuration



Block Diagram



*CHIP SELECTS CS ARE PROGRAMMABLE LOW ACTIVE, HIGH ACTIVE OR DON'T CARE.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . −10°C to 80°C

Storage Temperature . . . . . −65°C to 150°C

Voltage on Any Pin with Respect to Ground

. . . . . −0.5V + 7V

Power Dissipation 1.0W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent demage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

(T_A = 0°C to + 70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OH}	Output HIGH Level	2.4		V_{CC}	V	I_{OH} = −1.0 mA
V_{OL}	Output LOW Level			0.4	V	I_{OL} = 3.2 mA
V_{IH}	Input HIGH Level	2.0		V_{CC}	V	
V_{IL}	Input LOW Level	−0.5		0.8	V	
I_{LI}	Input Leakage Current			10	μA	V_{IN} = OV to V_{CC}
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = OV to V_{CC}
I_{CC}	Operating Supply Current			100	mA	Note 1
I_{SB}	Standby Supply Current			12	mA	Note 2
I_{OS}	Output Short Circuit Current			70	mA	Note 3

Capacitance

(T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_I	Input Capacitance		5	pf	V_{IN} = OV
C_O	Output Capacitance		5	pf	V_{OUT} = 0V

Note: This parameter is periodically sampled and is not 100% tested.

A.C. Characteristics

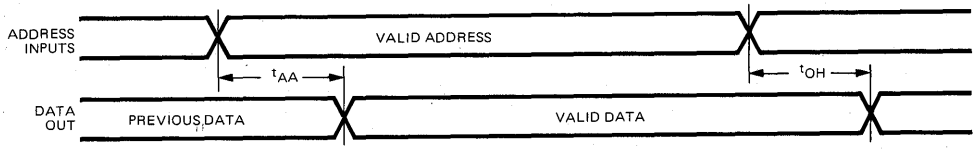
(T_A = 0°C to + 70°C, V_{CC} = +5V ± 10%) (Note 7)

Symbol	Parameter	UM2366-2 UM2366A-2		UM2366-1 UM2366A-1		UM2366 UM2366A		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CYC}	Cycle Time	200		300		450		ns	
t_{AA}	Address Access Time		200		300		450	ns	
t_{OH}	Output Hold After Address Change	10		10		10		ns	
t_{ACE}	Chip Enable Access Time		200		300		450	ns	Note 4
t_{ACS}	Chip Select Access Time		85		100		150	ns	
t_{AOE}	Output Enable Access Time		85		100		150	ns	Note 4
t_{LZ}	Output LOW Z Delay	10		10		10		ns	Note 5
t_{HZ}	Output HIGH Z Delay		85		100		150	ns	Note 6
t_{PU}	Power Up Time	0		0		0		ns	Note 4
t_{PD}	Power Down Time		85		100		150	ns	Note 4

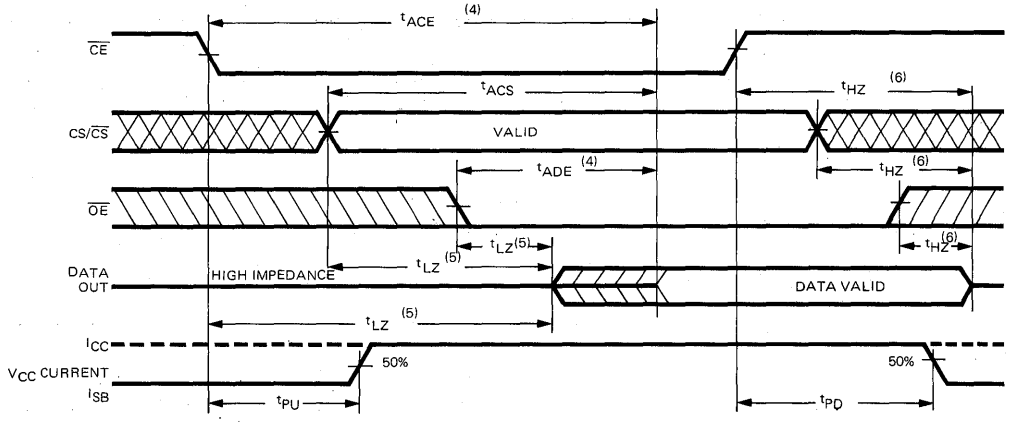
Notes:
1. Measured with device selected and outputs unloaded.
2. Applies to "A" versions only and measured with $\overline{CE}$ = 2.0V.
3. For a duration not to exceed one second.
4. Applies to "A" versions (power down) only.
5. Output low impedance delay (t_{LZ}) is measured from $\overline{CE}$ and $\overline{OE}$ going low and CS going active, whichever occurs last.
6. Output high impedance delay (t_{HZ}) is measured from either $\overline{CE}$ or $\overline{OE}$ going high or CS going inactive, whichever occurs first.
7. A minimum 0.5 ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved.

Timing Diagrams

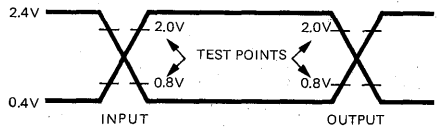
Propagation Delay from Address ($\overline{CE}$ = $\overline{OE}$ = LOW, CS/$\overline{CS}$ = Active)



Propagation Delay from Chip Enable, Chip Select (Address Valid)



A.C. Testing Input, Output Waveform



AC TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.4V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0". INPUT PULSE RISE AND FALL TIMES ARE 5 ns.

A.C. Testing Load Circuit

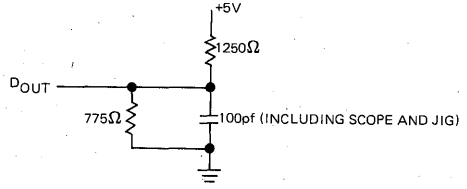


Figure 1.

Programming Instructions

All UMC Read Only Memories (ROM) utilize computer aided techniques to manufacture and test custom bit patterns. The customer's bit pattern and address information can be supplied to UMC in a number of different ways. UMC can process customer inputs in EPROM, ROM, PROM, paper tape, and computer punched cards. Contact your UMC sales representative for complete details on each of the various data input formats.

Programming instructions are listed at the end of the Memory Section.

Ordering Information

Part Number	Access Time	Operating Current	Standby Current	Package Type
UM2366	450 ns	100 mA	N.A.	Plastic
UM2366-1	300 ns	100 mA	N.A.	Plastic
UM2366-2	200 ns	100 mA	N.A.	Plastic
UM2366A	450 ns	100 mA	12 mA	Plastic
UM2366A-1	300 ns	100 mA	12 mA	Plastic
UM2366A-2	200 ns	100 mA	12 mA	Plastic

UM23128/UM23128A

16K × 8 NMOS ROM

Features

- EPROM pin compatible
- 16,384 x 8 bit organization
- single +5 volt supply
- Access time – 200/300/450 ns (max)
- Totally static operation
- Completely TTL compatible
- 28 pin JEDEC approved pinout
- UM23128A – automatic power down ($\overline{CE}$)
  - output enable function ($\overline{OE}$)
  - one programmable chip select (CS)
- UM23128 – non power down version
  - three programmable chip selects (CS)
- Three state outputs for wire-OR expansion
- EPROMS accepted as program data input

Description

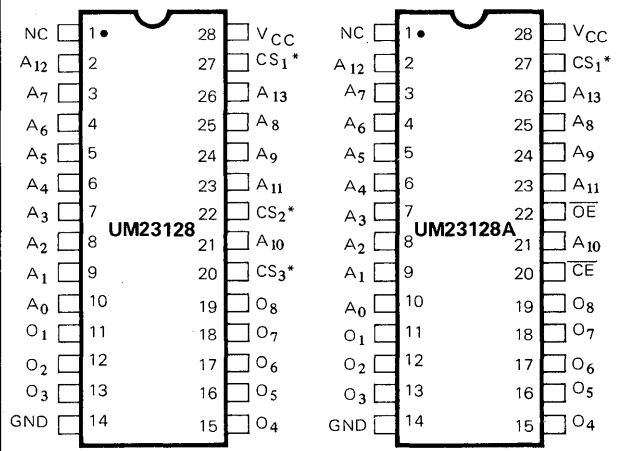
The UM23128 and UM23128A high performance Read Only Memories are organized 16,384 words by 8 bits with access times from 200 ns to 450 ns. The ROMs are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. Both ROMs conform to the JEDEC approved pinout for 28 pin 128K ROMs.

The UM23128 offers the simplest operation (no power down.) Its three programmable chip selects allow up to eight 128K ROMs to be OR-tied without external decoding.

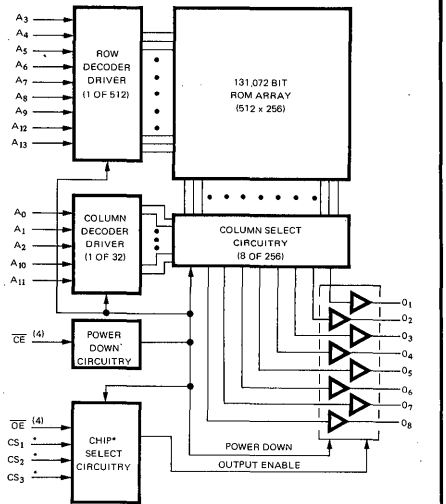
The UM23128A offers an automatic power down feature. Power down is controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes high, the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$ remains high. This unique feature provides system level power savings as much as 90%. An additional feature of the UM23128A is the Output Enable ($\overline{OE}$) function. This eliminates bus contention in multiple bus microprocessor systems. The programmable chip select allows two 128K ROMs to be OR-tied without external decoding.

Both the UM23128 and UM23128A are pin compatible with EPROMs thus eliminating the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias . . . . . −10°C to 85°C
Storage Temperature . . . . . −65°C to 150°C
Voltage on Any Pin with Respect to Ground
. . . . . −3.5V to +7V
Power Dissipation 1.0W
Electrostatic Discharge Rating (ESD)**
Inputs to Ground . . . . . ± 2000V

**Test Condition: MIL-STD-883B Method 3015.1

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

(T_A = 0°C to + 70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OH}	Output HIGH Level	2.4		V_{CC}	V	I_{OH} = -1.0 mA
V_{OL}	Output LOW Level			0.4	V	I_{OL} = 3.2 mA
V_{IH}	Input HIGH Level	2.0		V_{CC}	V	
V_{IL}	Input LOW Level	−3.0		0.8	V	
I_{LI}	Input Leakage Current			10	μA	V_{IN} = OV to V_{CC}
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = OV to V_{CC}
I_{CC}	Operating Supply Current			100	mA	Note 1
I_{SB}	Standby Supply Current			10	mA	Note 2
I_{OS}	Output Short Circuit Current			90	mA	Note 3

Capacitance

(T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_I	Input Capacitance		5	pf	V_{IN} = OV
C_O	Output Capacitance		5	pf	V_{OUT} = OV

Note: This parameter is periodically sampled and is not 100% tested.

A.C. Characteristics

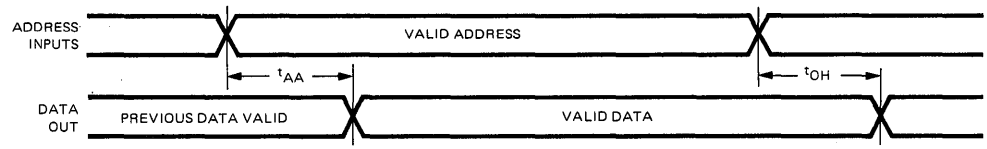
(T_A = 0°C to + 70°C, V_{CC} = +5V ± 10%) (Note 7)

Symbol	Parameter	UM23128-2 UM23128A-2		UM23128-1 UM23128A-1		UM23128 UM23128A		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CYC}	Cycle Time	200		300		450		ns	
t_{AA}	Address Access Time		200		300		450	ns	
t_{OH}	Output Hold After Address Change	10		10		10		ns	
t_{ACE}	Chip Enable Access Time		200		300		450	ns	Note 4
t_{ACS}	Chip Select Access Time		85		100		150	ns	
t_{AOE}	Output Enable Access Time		85		100		150	ns	Note 4
t_{LZ}	Output LOW Z Delay	10		10		10		ns	Note 5
t_{HZ}	Output HIGH Z Delay		85		100		150	ns	Note 6
t_{PU}	Power Up Time	0		0		0		ns	Note 4
t_{PD}	Power Down Time		100		120		150	ns	Note 4

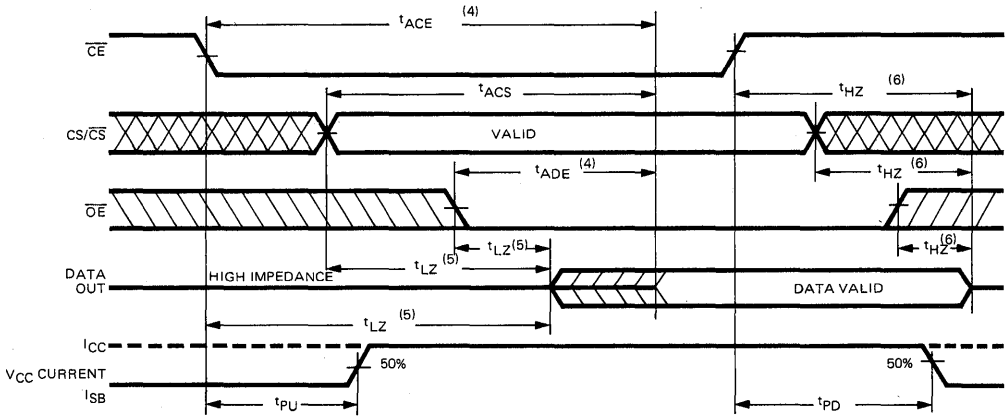
Notes:
1. Measured with device selected and outputs unloaded.
2. Applies to "A" versions only and measured with $\overline{CE}$ = 2.0V.
3. For a duration not to exceed one second with V_{OUT} = 0V
4. Applies to "A" versions (power down) only.
5. Output low impedance delay (t_{LZ}) is measured from $\overline{CE}$ and $\overline{OE}$ going low and CS going active, whichever occurs last.
6. Output high impedance delay (t_{HZ}) is measured from either $\overline{CE}$ or $\overline{OE}$ going high or CS going inactive, whichever occurs first.
7. A minimum 0.5 ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved.

Timing Diagrams

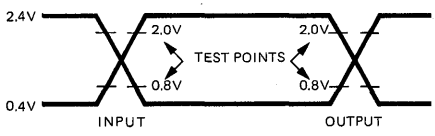
Propagation Delay from Address ($\overline{CE}$ = $\overline{OE}$ = LOW, CS/$\overline{CS}$ = Active)



Propagation Delay from Chip Enable, Chip Select (Address Valid)



A.C. Testing Input, Output Waveform



AC TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.4V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0". INPUT PULSE RISE AND FALL TIMES ARE 5 ns.

A.C. Testing Load Circuit

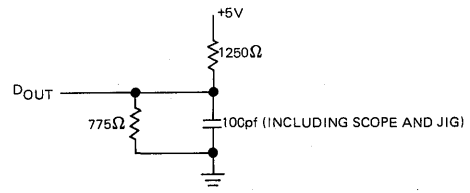


Figure 1.

Programming Instructions

All UMC Read Only Memories (ROM) utilize computer asided techniques to manufacture and test custom bit patterns. The customer's bit pattern and address information can be supplied to UMC in a number of different ways. UMC can process customer inputs in EPROM, ROM, PROM, paper tape, and computer punched cards. Contact your UMC sales representative for complete details on each of the various data input formats.

Programming instructions are listed at the end of the Memory Section.

Ordering Information

Part Number	Access Time	Operating Current	Standby Current	Package Type
UM23128	450 ns	100 mA	N.A.	Plastic
UM23128-1	300 ns	100 mA	N.A.	Plastic
UM23128-2	200 ns	100 mA	N.A.	Plastic
UM23128A	450 ns	100 mA	10 mA	Plastic
UM23128A-1	300 ns	100 mA	10 mA	Plastic
UM23128A-2	200 ns	100 mA	10 mA	Plastic

UM23256/UM23256A

32K × 8 NMOS ROM

Features

- EPROM pin compatible
- 32,768 x 8 bit organization
- Single +5 volt supply
- Access time–200/300/450ns (max)
- Totally static operation
- Completely TTL compatible
- 28 Pin JEDEC approved pinout
- UM23256A– automatic power down ($\overline{CE}$)
  – output enable function ($\overline{OE}$)
- UM23256 – non power down version
  – two programmable chip selects (CS)
- Three state outputs for wire-OR expansion
- EPROMs accepted as program data input

General Description

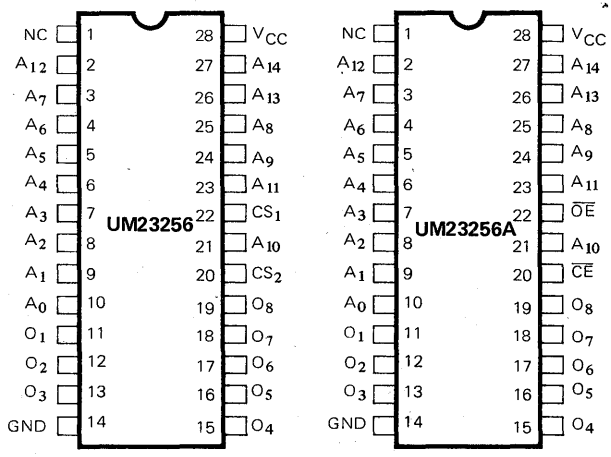
The UM23256 and UM23256A high performance Read Only Memories are organized 32,768 words by 8 bits with access times from 200 ns to 450 ns. The ROMs are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. Both ROMs conform to the JEDEC approved pinout for 28 pin 256K ROMs.

The UM23256 offers the simplest operation (no power down.) Its two programmable chip selects allow up to four 256K ROMs to be OR-tied without external decoding.

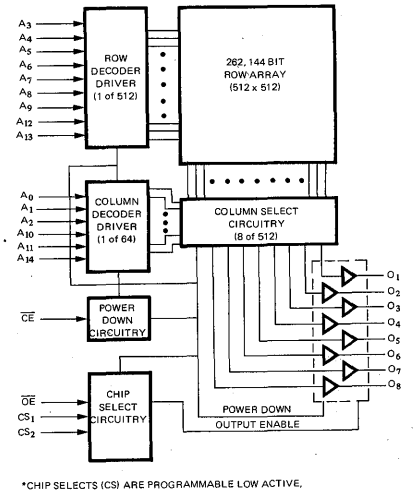
The UM23256A offers an automatic power down feature. Power down is controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes high, the device will automatically power down and remain in a low power stand-by mode as long as $\overline{CE}$ remains high. This unique feature provides system level power savings as much as 90%. An additional feature of the UM23256A is the Output Enable ($\overline{OE}$) function. This eliminates bus contention in multiple bus microprocessor systems.

Both the UM23256 and UM23256A are pin compatible with EPROMs thus eliminating the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

Pin Configuration



Block Diagram



*CHIP SELECTS (CS) ARE PROGRAMMABLE LOW ACTIVE, HIGH ACTIVE OR DON'T CARE

Absolute Maximum Ratings*

Temperature Under Bias . . . . . −10°C to 85°C

Storage Temperature . . . . . −65°C to 150°C

Voltage on Any Pin with Respect to Ground

. . . . . −3.5V to + 7V

Power Dissipation 1.0W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. Characteristics

(T_A = 0°C to + 70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OH}	Output HIGH Level	2.4		V_{CC}	V	I_{OH} = −1.0 mA
V_{OL}	Output LOW Level			0.4	V	I_{OL} = 3.2 mA
V_{IH}	Input HIGH Level	2.0		V_{CC}	V	
V_{IL}	Input LOW Level	−3.0		0.8	V	
V_{LI}	Input Leakage Current			10	μA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 0V to V_{CC}
I_{CC}	Operating Supply Current			100	mA	Note 1
I_{SB}	Standby Supply Current			10	mA	Note 2
I_{OS}	Output Short Circuit Current			90	mA	Note 3

Capacitance

(T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_I	Input Capacitance		5	pf	V_{IN} = 0V
C_O	Output Capacitance		5	pf	V_{OUT} = 0V

Note: This parameter is periodically sampled and is not 100% tested.

A. C. Characteristics

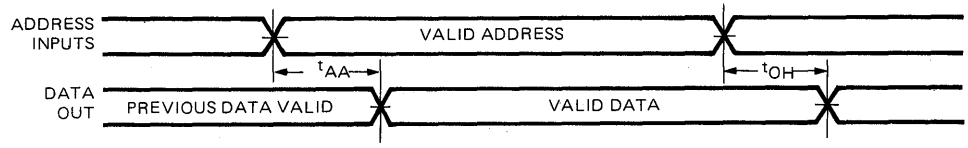
(T_A = 0°C to + 70°C, V_{CC} = +5V ± 10%) (Note 7)

Symbol	Parameter	23256-2 23256A-2		23256-1 23256A-1		23256 23256A		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CYC}	Cycle Time	200		300		450		ns	
t_{AA}	Address Access Time		200		300		450	ns	
t_{OH}	Output Hold After Address Change	10		10		10		ns	
t_{ACE}	Chip Enable Access Time		200		300		450	ns	Note 4
t_{ACS}	Chip Select Access Time		85		100		150	ns	
t_{AOE}	Output Enable Access Time		85		100		150	ns	Note 4
t_{LZ}	Ouput LOW Z Delay	10		10		10		ns	Note 5
t_{HZ}	Output HIGH Z Delay		85		100		150	ns	Note 6
t_{PU}	Power Up Time	0		0		0		ns	Note 4
t_{PD}	Power Down Time		100		120		150	ns	Note 4

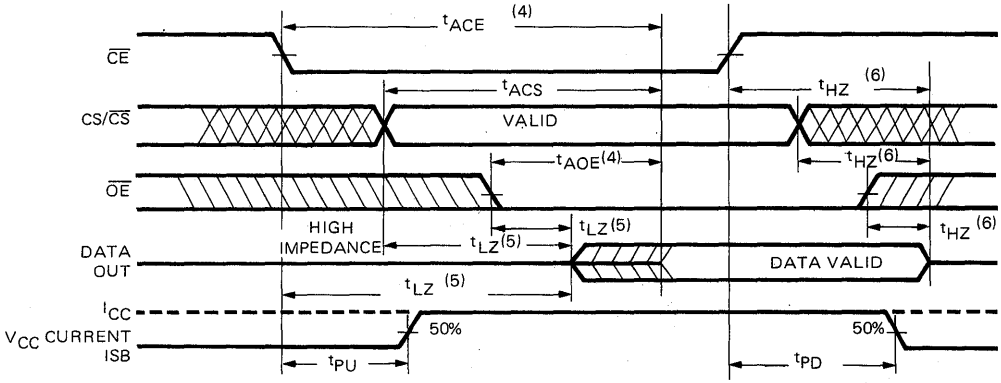
Notes:
1. Measured with device selected and outputs unloaded.
2. Applies to "A" versions only and measured with $\overline{CE}$ = 2.0V.
3. For a duration not to exceed one second with V_{OUT} = 0V.
4. Applies to "A" versions (power down) only.
5. Output low impedance delay (t_{LZ}) is measured from $\overline{CE}$ and $\overline{OE}$ going low and CS going active, whichever occurs last.
6. Output high impedance delay (t_{HZ}) is measured from either $\overline{CE}$ or $\overline{OE}$ going high or CS going inactive, whichever occurs first.
7. A minimum 0.5 ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved.

Timing Diagrams

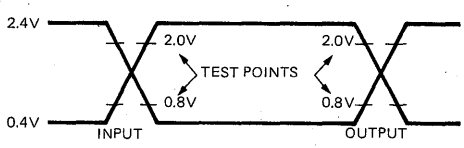
Propagation Delay from Address ($\overline{CE}$ = $\overline{OE}$ = LOW, CS/$\overline{CS}$ = Active)



Propagation Delay from Chip Enable, Chip Select (Address Valid)



A.C. Testing Input, Output Waveform



AC TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.4V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0". INPUT PULSE RISE AND FALL TIMES ARE 5 ns.

A.C. Testing Load Circuit

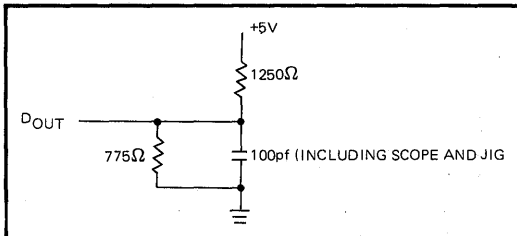


Figure 1.

Ordering Information

Part Number	Access Time	Operating Current	Standby Current	Package Type
UM23256	450 ns	100 mA	N.A.	Plastic
UM23256–1	300 ns	100 mA	N.A.	Plastic
UM23256–2	200 ns	100 mA	N.A.	Plastic
UM23256A	450 ns	100 mA	10 mA	Plastic
UM23256A–1	300 ns	100 mA	10 mA	Plastic
UM23256A–2	200 ns	100 mA	10 mA	Plastic

UMC

Static RAM

Selection Guide

Part No.	Descriptions	Compatible Devices	Remarks	Page
UM2147	4Kx1 High Speed NMOS SRAM	SYP 2147	Access Time 70, 55, 45 ns	2–3
UM2148	1Kx4 High Speed NMOS SRAM	SYP 2148	Access Time 70, 55, 45 ns	2–8
UM2149	1Kx4 High Speed NMOS SRAM	SYP 2149	Access Time 70, 55, 45 ns	2–13
UM6104	1Kx4 CMOS SRAM	HM 4334	Access Time 250, 200, 150, 120 ns for 5V, 2μs for 2.5V Operating	2–18
UM6104-1	1Kx4 CMOS SRAM	TC 5047AP		2–23
UM6114	1Kx4 CMOS SRAM		Access Time 100, 70, 55, 45 ns	2–28
UM6116-2/3/-4	2Kx8 High Speed CMOS SRAM	IDT 6116	Access Time 70, 90, 120 ns	2–33
UM6116-5	2Kx8 High Speed CMOS SRAM	IDT 6116	Access Time 55 ns	2–38
UM6164	8Kx8 High Speed CMOS SRAM	IDT 7164	Access Time 70, 55, 45 ns	2–43
UM6167	16Kx1 High Speed CMOS SRAM	HM 6167	Access Time 70, 55, 45 ns	2–50
UM6168	4Kx4 High Speed CMOS SRAM	HM 6168	Access Time 70, 55, 45 ns	2–55

UM2147

4K × 1 High Speed NMOS SRAM

Features

- 45 ns maximum access time
- No clocks or strobes required
- Automatic $\overline{CE}$ power down
- Identical cycle and access times
- Single +5V supply (± 10%)
- Pinout and function compatible to SY2147
- Total TTL compatible: All inputs and outputs
- Separate data input and output
- High density 18-pin package
- Three-state output

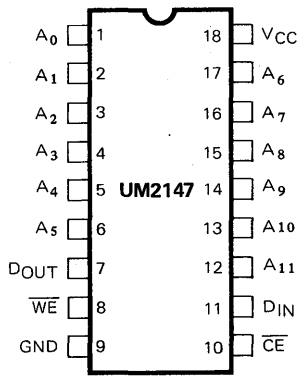
General Description

The UMC UM2147 is a 4096-Bit Static Random Access Memory organized 4096 words by 1-bit and is fabricated using UMC's new scaled N-channel silicon gate technology. It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate. Address set-up times are not required and the data is read out non-destructively with the same polarity as the input data. Separate data input and output pins provide maximum design flexibility. The three-state output facilitates memory expansion by allowing the outputs to be OR-tied to other devices.

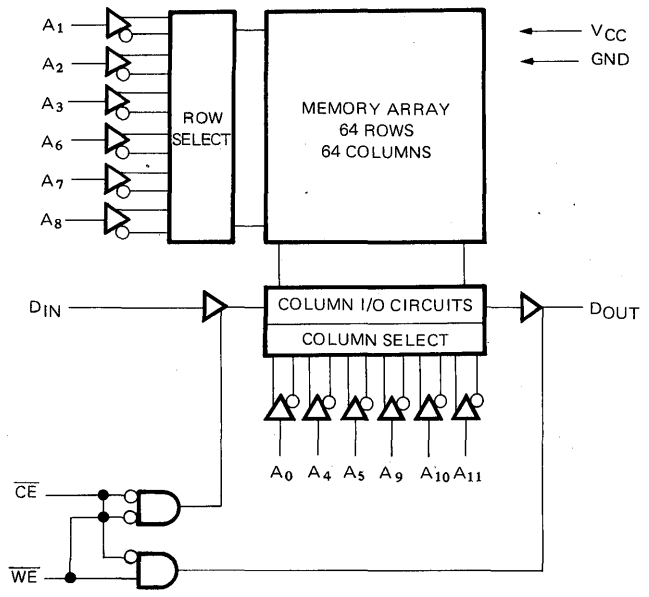
The UM2147 offers an automatic power down feature. Power down is controlled by the Chip Enable input. When Chip Enable ($\overline{CE}$) goes high, thus deselecting the UM2147 the device will automatically power down and remain in a standby power mode as long as $\overline{CE}$ remain high. This unique feature provides system level power savings as much as 80%.

The UM2147 is packaged in an 18-pin DIP for the highest possible density. The device is fully TTL compatible and has a single +5V power supply.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias . . . . . −10°C to 85°C
Storage Temperature . . . . . −65°C to 150°C
Voltage on Any Pin with Respect to Ground . . . . . −3.5V to +7V
Power Dissipation 1.2W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

(T_A = 0°C to +70°C, V_{CC} = 5V ± 10% Unless otherwise specified) (Note 8)

Symbol	Parameter	2147 /-1/-2		2147 L/L-1		Units	Conditions
		Min.	Max.	Min.	Max.		
I_{LI}	Input Load Current (All input pins)		10		10	µA	V_{CC} = Max, V_{IN} = Gnd to V_{CC}
$\|I_{LO}\|$	Output Leakage Current		50		50	µA	$\overline{CE}$ = V_{IH}, V_{CC} = Max. V_{OUT} = Gnd to 4.5V
I_{CC}	Power Supply Current		150		115	mA	T_A = 25°C; V_{CC} = Max. $\overline{CE}$ = V_{IL} Outputs Open
			160		125	mA	T_A = 0°C; V_{CC} = Max. $\overline{CE}$ = V_{IL} Outputs Open
I_{SB}	Standby Current		20		10	mA	V_{CC} = Min to Max, $\overline{CE}$ = V_{IH}
I_{PO}	Peak Power-on Current (Note 9)		50		30	mA	V_{CC} = Gnd to V_{CC} Min; $\overline{CE}$ = Lower of V_{CC} or V_{IH} Min
V_{IL}	Input Low Voltage	−3.0	0.8	−3.0	0.8	V	
V_{IH}	Input High Voltage	2.0	6.0	2.0	6.0	V	
V_{OL}	Output Low Voltage		0.4		0.4	V	I_{OL} = 8 mA
V_{OH}	Output High Voltage	2.4		2.4		V	I_{OH} = −4.0mA

Capacitance

(T_A=25°C, f = 1.0 MHz)

Symbol	Test	Typ.	Max.	Unit
C_{OUT}	Output Capacitance		6	pF
C_{IN}	Input Capacitance		5	pF

Note: This parameter is periodically sampled and not 100% tested.

A.C. Characteristics

(T_A = 0°C to +70°C, V_{CC} = 5V ±10% Unless otherwise specified) (Note 8, 10)

READ CYCLE

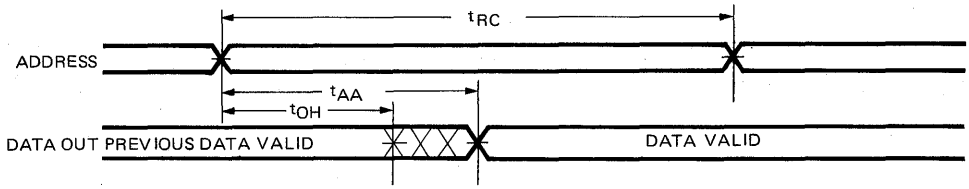
Symbol	Parameter	2147/L		2147-1/L-1		2147–2		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	70		55		45		ns	
t_{AA}	Address Access Time		70		55		45	ns	
t_{ACE1}	Chip Enable Access Time		70		55		45	ns	1
t_{ACE2}	Chip Enable Access Time		80		65		45	ns	2
t_{OH}	Output Hold from Address Change	5		5		5		ns	
t_{LZ}	Chip Selection to Output in Low Z	10		10		5		ns	7
t_{HZ}	Chip Deselection to Output in High Z	0	40	0	30	0	30	ns	7
t_{PU}	Chip Selection to Power Up Time	0		0		0		ns	
t_{PD}	Chip Deselection to Power Down Time		30		20		20	ns	

WRITE CYCLE

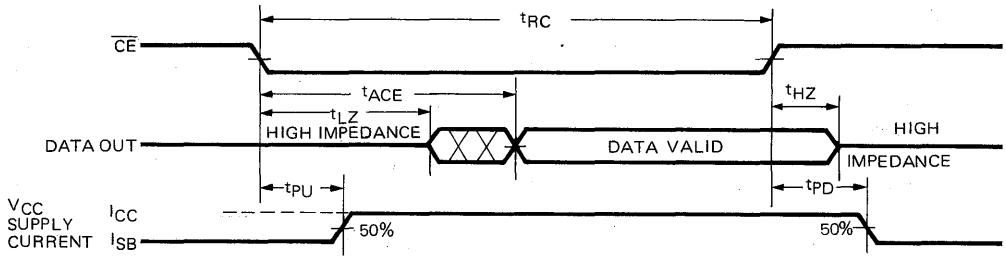
t_{WC}	Write Cycle Time	70		55		45		ns	
t_{CW}	Chip Enabled to End of Write	55		45		45		ns	
t_{AW}	Address Valid to End of Write	55		45		45		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{WP}	Write Pulse Width	40		25		25		ns	
t_{WR}	Write Recovery Time	15		10		0		ns	
t_{DW}	Data Valid to End of Write	30		25		25		ns	
t_{DH}	Data Hold Time	10		10		10		ns	
t_{WZ}	Write Enabled to Output in High Z	0	35	0	25	0	25	ns	7
t_{OW}	Output Active from End of Write	0		0		0		ns	7

Timing Diagrams

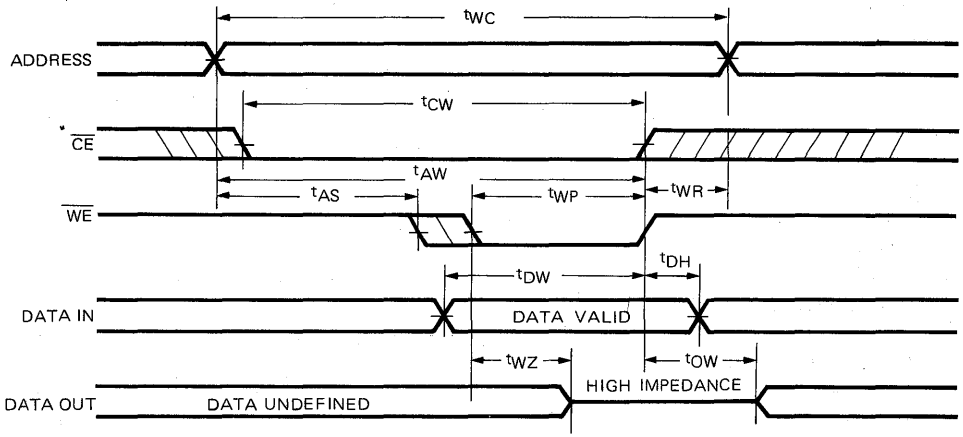
READ CYCLE NO. 1 (NOTES 3 AND 4)



READ CYCLE NO. 2 (NOTES 3 AND 5)



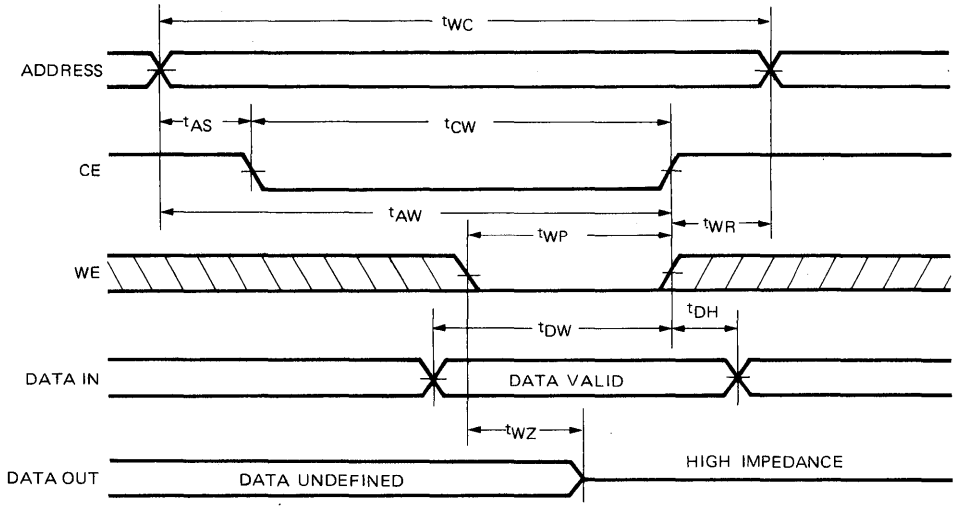
WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) (NOTE 6)



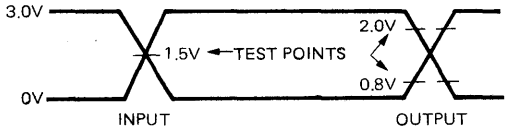
Notes:

1. Chip deselected for greater than 55 ns prior to selection.
2. Chip deselected for a finite time that is less than 55ns prior to selection. (If the deselect time is Ons, the chip is by definition selected and access occurs according to Read Cycle No. 1.).
3. $\overline{WE}$ is high for Read Cycles.
4. Device is continuously selected, $\overline{CE} = V_{IL}$.
5. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
6. If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in the high impedance state.
7. Transition is measured ± 500mV from low or high impedance voltage with load B. This parameter is sampled and not 100% tested.
8. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.
9. A pullup resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected: otherwise, power-on current approaches I_{CC} active.
10. A minimum 0.5 ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved.

WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED) (NOTE 6)

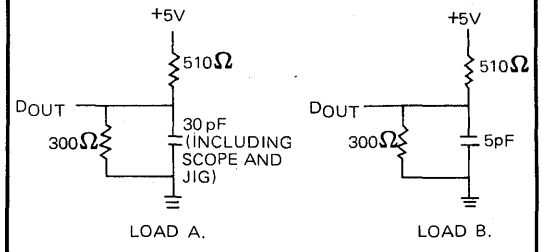


A.C. Testing Input, Output Waveform



A.C. TESTING: INPUTS ARE DRIVEN AT 3.0V FOR A LOGIC "1" AND 0.0V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0" AT THE OUTPUTS. THE INPUTS ARE MEASURED AT 1.5V. INPUT RISE AND FALL TIMES ARE 5 ns.

A.C. Testing Load Circuit



Ordering Information

Part Number	Access Time (Max.)	Operating Current (Max.)	Stand by Current (Max.)	Package Type
UM2147	70 ns	160 mA	20 mA	Plastic
UM2147–1	55 ns	180 mA	30 mA	Plastic
UM2147–2	45 ns	180 mA	30 mA	Plastic
UM2147L	70 ns	140 mA	10 mA	Plastic
UM2147L–1	55 ns	125 mA	15 mA	Plastic

UM2148

1K × 4 High Speed NMOS SRAM

Features

- 45 ns maximum access time
- No clocks or strobes required
- Automatic $\overline{CE}$ power down
- Identical cycle and access times
- Single +5V supply (± 10%)
- Pinout and function compatible to SY2148
- Industry standard 2114 pinout
- Totally TTL compatible all inputs and outputs
- Common data input and output
- High density 18-pin package
- Three-state output

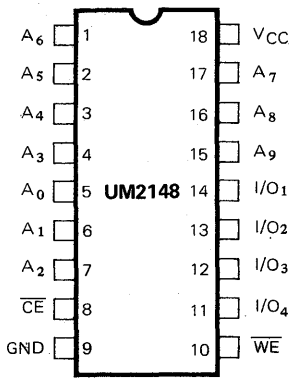
General Description

The UMC UM2148 is a 4096-Bit Static Random Access Memory organized 1024 words by 4 bits and is fabricated using UMC's new scaled N-channel silicon gate technology. It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate. Address set-up times are not required and the data is read out non-destructively with the same polarity as the input data. Common data input and output pins provide maximum design flexibility. The three-state output facilitates memory expansion by allowing the outputs to be OR-tied to other devices.

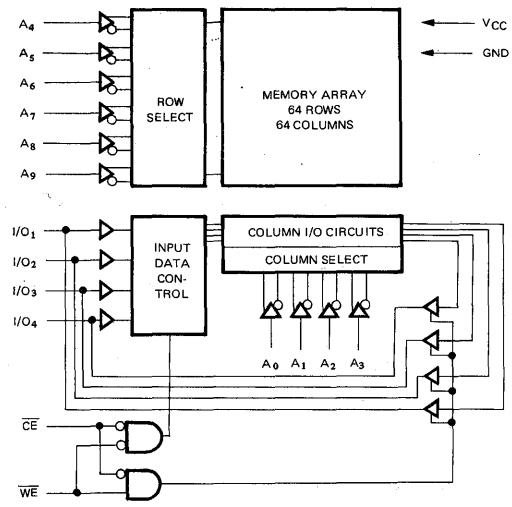
The UM2148 offers an automatic power down feature. Power down is controlled by the Chip Enable input. When Chip Enable ($\overline{CE}$) goes high, thus deselecting the UM2148 the device will automatically power down and remain in a standby power mode as long as $\overline{CE}$ remains high. This unique feature provides system level power savings as much as 85%.

The UM2148 is packaged in an 18-pin DIP for the highest possible density. The device is fully TTL compatible and has a single +5V power supply.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias . . . . . −10°C to 85°C
Storage Temperature . . . . . −65°C to 150°C
Voltage on Any Pin with Respect to Ground . . . . . −3.5V to +7V
Power Dissipation 1.0W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics

(T_A = 0°C to +70°C, V_{CC} = 5V ±10% Unless otherwise specified) (note 8)

Symbol	Parameter	2148/-1/-2		2148L/L-1		Units	Conditions	
		Min.	Max.	Min.	Max.			
I_{LI}	Input Load Current (All input pins)		10		10	μA	V_{CC} = Max, V_{IN} = Gnd to V_{CC}	
$\|I_{LO}\|$	Output Leakage Current		50		50	μA	$\overline{CE}$ = V_{IH}, V_{CC} = Max V_{OUT} = Gnd to 4.5V	
I_{CC}	Power Supply Current		140		115	mA	T_A = 25°C	V_{CC} = Max, $\overline{CE}$ = V_{IL}
			150		125	mA	T_A = 0°C	Outputs Open
I_{SB}	Standby Current		30		20	mA	V_{CC} = Min to Max, $\overline{CE}$ = V_{IH}	
I_{PO}	Peak Power-on Current (Note 9)		50		30	mA	V_{CC} = Gnd to V_{CC} Min $\overline{CE}$ = Lower of V_{CC} or V_{IH} Min	
V_{IL}	Input Low Voltage	−3.0	0.8	−3.0	0.8	V		
V_{IH}	Input High Voltage	2.0	6.0	2.0	6.0	V		
V_{OL}	Output Low Voltage		0.4		0.4	V	I_{OL} = 8mA	
V_{OH}	Output High Voltage	2.4		2.4		V	I_{OH} = −4mA	

Capacitance

(T_A = 25°C, f = 1.0 MHz)

Symbol	Test	Typ.	Max.	Unit
C_{OUT}	Output Capacitance		7	pF
C_{IN}	Input Capacitance		5	pF

Note: This parameter is periodically sampled and not 100% tested.

A.C. Characteristics

(T_A = 0°C to +70°C, V_{CC} = 5V ±10% Unless otherwise specified) (Note 8)

READ CYCLE

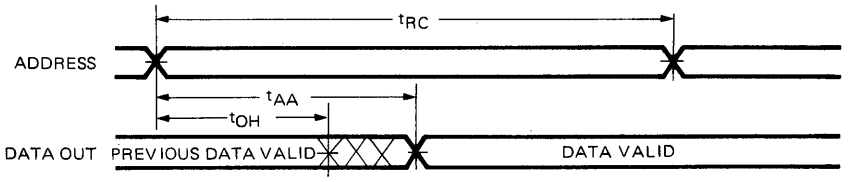
Symbol	Parameter	2148/L		2148-1/L-1		2148–2		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	70		55		45		ns	
t_{AA}	Address Access Time		70		55		45	ns	
t_{ACE1}	Chip Enable Access Time		70		55		45	ns	Note 1
t_{ACE2}	Chip Enable Access Time		80		65		55	ns	Note 2
t_{OH}	Output Hold from Address Change	5		5		5		ns	
t_{LZ}	Chip Selection to Output in Low Z	10		10		10		ns	Note 7
t_{HZ}	Chip Deselection to Output in High Z	0	20	0	20	0	20	ns	Note 7
t_{PU}	Chip Selection to Power Up Time	0		0		0		ns	
t_{PD}	Chip Deselection to Power Down Time		30		30		30	ns	

WRITE CYCLE

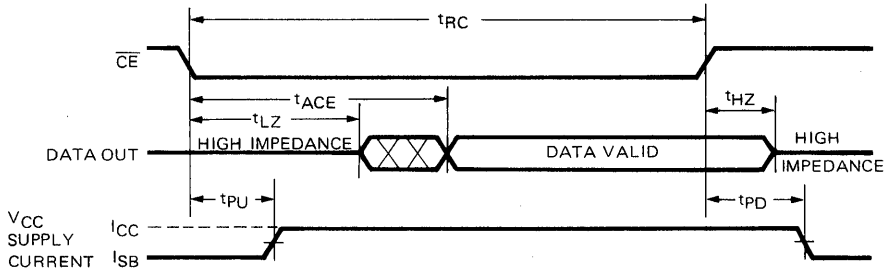
t_{WE}	Write Cycle Time	70		55		45		ns	
t_{CW}	Chip Enabled to End of Write	65		50		40		ns	
t_{AW}	Address Valid to End of Write	65		50		40		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{WP}	Write Pulse Width	50		40		35		ns	
t_{WR}	Write Recovery Time	5		5		5		ns	
t_{DW}	Data Valid to End of Write	25		20		20		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WZ}	Write Enabled to Output in High Z	0	25	0	20	0	15	ns	Note 7
t_{OW}	Output Active from End of Write	0		0		0		ns	Note 7

Timing Diagrams

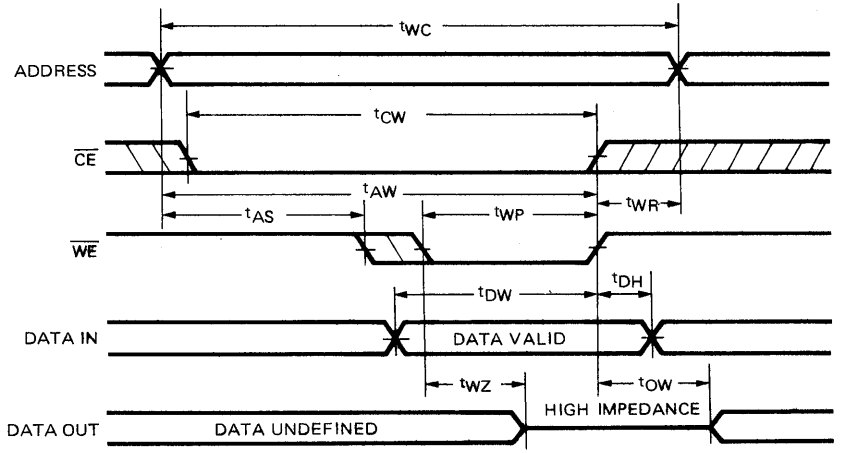
READ CYCLE NO. 1 (NOTES 3 AND 4)



READ CYCLE NO. 2 (NOTES 3 AND 5)



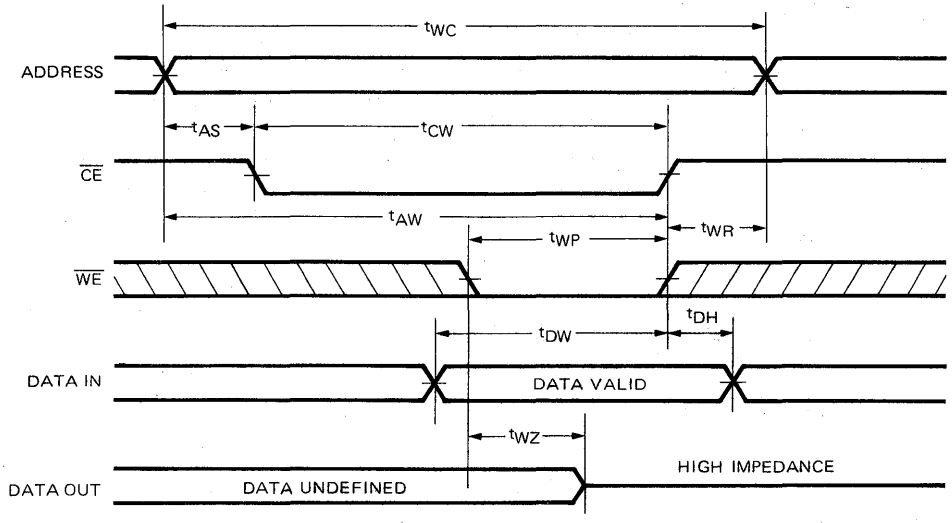
WRITE CYCLE NO. 1 (WE CONTROLLED) (NOTE 6)



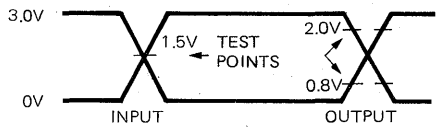
Notes:

1. Chip deselected for greater than 55ns prior to selection.
2. Chip deselected for a finite time that is less than 55ns prior to selection. (If the deselect time is Ons, the chip is by definition selected and access occurs according to Read Cycle No. 1).
3. $\overline{WE}$ is high for Read Cycles.
4. Device is continuously selected, $\overline{CE} = V_{IL}$.
5. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
6. If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in the high impedance state.
7. Transition is measured ±500mV from low or high impedance voltage with load B. This parameter is sampled and not 100% tested.
8. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.
9. A pullup resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected: otherwise, power-on current approaches I_{CC} active.
10. A minimum 0.5 ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved.

WRITE CYCLE NO. 2 (CE CONTROLLED) (NOTE 6)

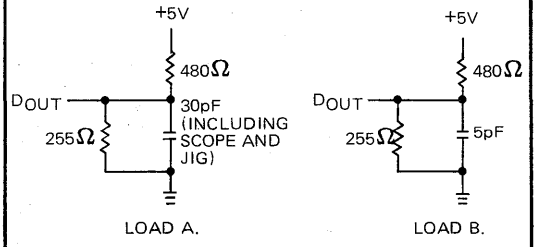


A.C. Testing Input, Output Waveform



A.C. TESTING: INPUTS ARE DRIVEN AT 3.0V FOR A LOGIC "1" AND 0.0V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0" AT THE OUTPUTS. THE INPUTS ARE MEASURED AT 1.5V. INPUT RISE AND FALL TIMES ARE 5 ns.

A.C. Testing Load Circuit



Ordering Information

Part Number	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)	Package Type
UM2148	70 ns	150 mA	30 mA	Plastic
UM2148–1	55 ns	150 mA	30 mA	Plastic
UM2148–2	45 ns	150 mA	30 mA	Plastic
UM2148L	70 ns	125 mA	20 mA	Plastic
UM2148L–1	55 ns	125 mA	20 mA	Plastic

1K × 4 High Speed NMOS SRAM

Features

- 45 ns maximum address access
- Fully static operation:
  No clocks or strobes required
- Fast chip select access time: 20ns max.
- Identical cycle and access times
- Single +5V supply
- Industry standard 2114 pinout
- Totally TTL compatible:
  All inputs and outputs
- Common data input and outputs
- High density 18-pin package
- Three-state output

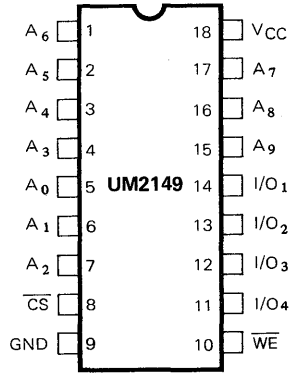
General Description

The UMC UM2149 is a 4096-Bit Static Random Access Memory organized 1024 words by 4 bits and is fabricated using UMC's new N-channel Silicon-Gate HMOS technology. It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate. Address set-up times are not required and the data is read out non-destructively with the same polarity as the input data. Common data input and output pins provide maximum design flexibility. The three-state output facilitates memory expansion by allowing the outputs to be OR-tied to other devices.

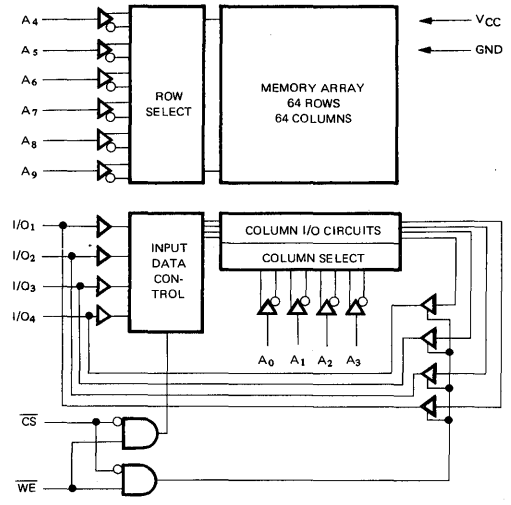
The UM2149 offers a chip select access that is faster than its address access. In a typical application, the address access begins as soon as the address is valid. At this time, the high order addresses are decoded and the desired memory is then selected. With the faster chip select access, this decode time will not add to the overall access time thus significantly improving system performance.

The UM2149 is packaged in an 18-pin DIP for the highest possible density. The device is fully TTL compatible and has a single +5V power supply.

Pin Configuration



Block Diagram



Absolute Maximum Ratings

Temperature Under Bias . . . . . –10°C to 85°C
Storage Temperature . . . . . –65°C to 150°C
Voltage on Any Pin with Respect to Ground . . . . . –3.5V to +7V
Power Dissipation 1.0W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics

(T_A = 0°C to +70°C, V_{CC} = 5V ± 10% Unless otherwise specified) (Note 8)

Symbol	Parameter	2149/-1/-2		2149L/L-1		Units	Conditions	
		Min.	Max.	Min.	Max.			
I_{LI}	Input Load Current (All input pins)		10		10	µA	V_{CC} = Max, V_{IN} = Gnd to V_{CC}	
$\lvert I_{LO} \rvert$	Output Leakage Current		50		50	µA	$\overline{CS}$ = V_{IH}, V_{CC} = Max. V_{OUT} = Gnd to 4.5V	
I_{CC}	Power Supply Current		140		115	mA	T_A = 25°C	V_{CC} = Max, $\overline{CS}$ = V_{IL} Outputs Open
			150		125	mA	T_A = 0°C	
V_{IL}	Input Low Voltage	–0.3	0.8	–0.3	0.8	V		
V_{IH}	Input High Voltage	2.0	6.0	2.0	6.0	V		
V_{OL}	Output Low Voltage		0.4		0.4	V	I_{OL} = 8 mA	
V_{OH}	Output High Voltage	2.4		2.4		V	I_{OH} = –4.0 mA	
I_{OS}	Output Short Circuit Current		±200		±200	mA	V_{OUT} = GND to V_{CC} (Note 7)	

Capacitance

(T_A = 25°C, f = 1.0 MHz)

Symbol	Test	Typ.	Max.	Unit
C_{OUT}	Output Capacitance		7	pF
C_{IN}	Input Capacitance		5	pF

Note: This parameter is periodically sampled and not 100% tested.

A.C. Characteristics

(T_A = 0°C to +70°C, V_{CC} = 5V ± 10% Unless otherwise specified) (Note 6, 8)

READ CYCLE

Symbol	Parameter	2149		2149–1		2149–2		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	70		55		45		ns	
t_{AA}	Address Access Time		70		55		45	ns	
t_{ACS}	Chip Select Access Time		30		25		20	ns	
t_{OH}	Output Hold from Address Change	5		5		5		ns	
t_{LZ}	Chip Selection to Output in Low Z	5		5		5		ns	Note 5
t_{HZ}	Chip Deselection to Output in High Z	0	15	0	15	0	15	ns	Note 5

WRITE CYCLE

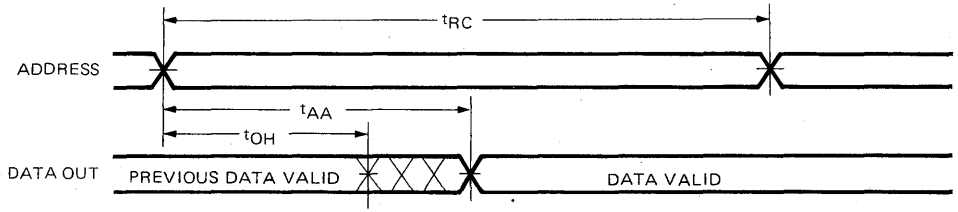
t_{WC}	Write Cycle Time	70		55		45		ns	
t_{CW}	Chip Selection to End of Write	65		50		40		ns	
t_{AW}	Address Valid to End of Write	65		50		40		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{WP}	Write Pulse Width	50		40		35		ns	
t_{WR}	Write Recovery Time	5		5		5		ns	
t_{DW}	Data Valid to End of Write	25		20		20		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WZ}	Write Enabled to Output in High Z	0	25	0	20	0	15	ns	Note 5
t_{OW}	Output Active from End of Write	0		0		0		ns	Note 5

(See following page for notes)

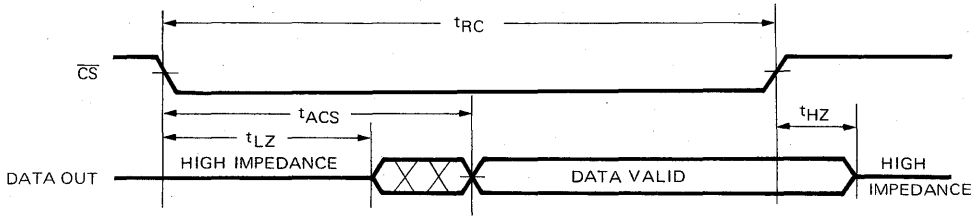
SRAM

Timing Diagrams

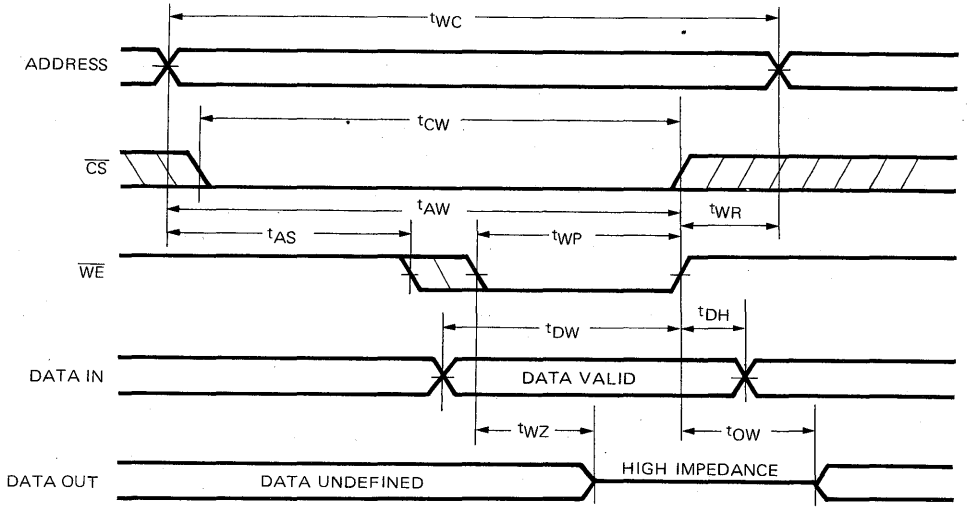
READ CYCLE NO. 1 (Notes 1 and 2)



READ CYCLE NO. 2 (Notes 1 and 3)



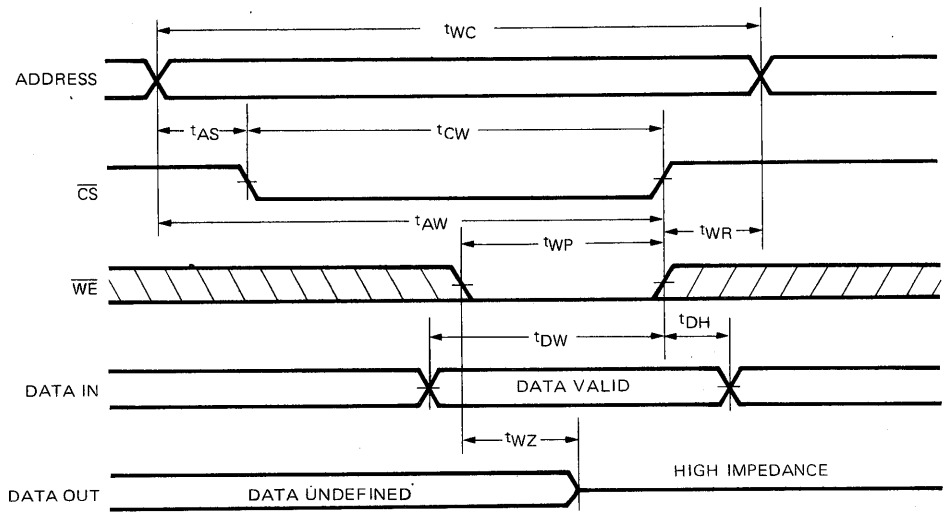
WRITE CYCLE NO. 1 ($\overline{WE}$ controlled) (Note 4)



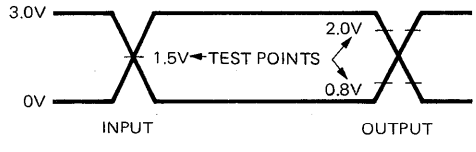
Notes:

1. $\overline{WE}$ is high for Read Cycles.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Addresses valid.
4. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in the high impedance state.
5. Transition is measured ± 500 mV from low or high impedance voltage with load B. This parameter is sampled and not 100% tested.
6. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.
7. Duration not to exceed one minute.
8. A minimum 0.5 ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved.

WRITE CYCLE NO. 2 ($\overline{CS}$ controlled) (note 4)

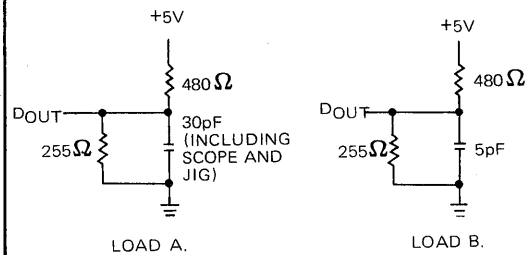


A.C. Testing Input, Output Waveform



A.C. TESTING: INPUTS ARE DRIVEN AT 3.0V FOR A LOGIC "1" AND 0.0V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0" AT THE OUTPUTS. THE INPUTS ARE MEASURED AT 1.5V. INPUT RISE AND FALL TIMES ARE 5 ns.

A.C. Testing Load Circuit



Ordering Information

Order Number	Access Time (Max.)	Supply Current (Max.)	Package Type
UM2149	70 ns	150 mA	Plastic
UM2149–1	55 ns	150 mA	Plastic
UM2149–2	45 ns	150 mA	Plastic
UM2149L	70 ns	125 mA	plastic
UM2149L–1	55 ns	125 mA	Plastic

UM6104

1K × 4 CMOS SRAM

Features

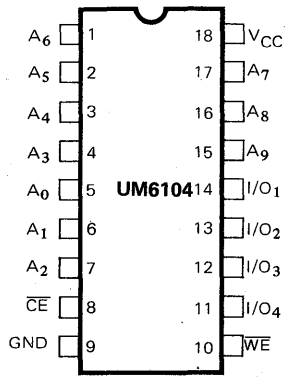
- Single + 5V power supply
- Low power standby
- Low power operation
- Fast Access time . . . . . 120/150/200/250 ns max.
- Data retention . . . . . 2.0V min.
- Three-state outputs
- On-chip address register
- Synchronous circuitry
- Standard 18 pin DIP package
- TTL compatible input/output

General Description

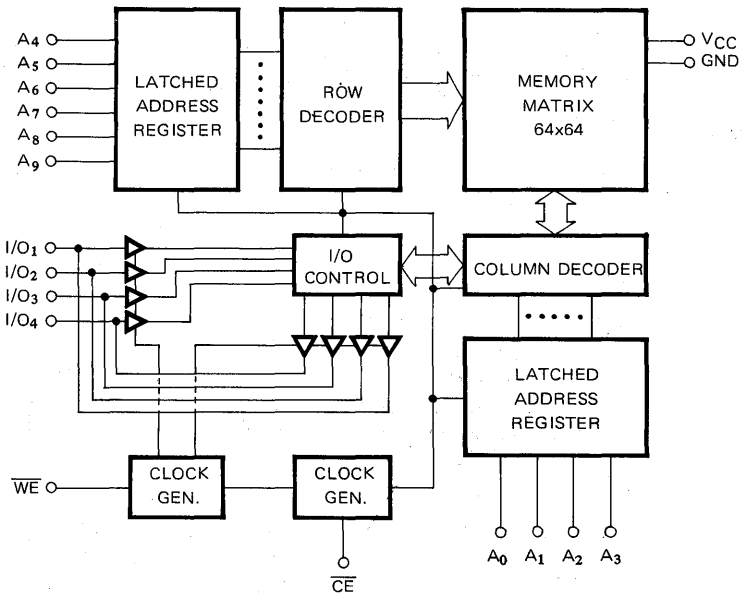
The UM6104 is a 1024x4 fully static CMOS RAM. The device utilizes synchronous circuitry to achieve performance and low power operation.

On chip latches are provided for the addresses allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory systems.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Ambient temperature under bias, T_A . . . . −10 to +80°C
Storage temperature, T_{ST} . . . . . −55 to +125°C
Input voltage, V_{IN} . . . . . −0.3 to V_{CC} +0.3V
Output voltage V_{OUT} . . . . . −0.3 to V_{CC} +0.3V
Maximum power supply voltage, V_{CC} max. . . . . +7.0V

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

D.C. Electrical Characteristics

(T_A = 0 to 70°C, GND = 0V, V_{CC} = 4.5 to 5.5V unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IL}	Input low voltage		−0.3	–	0.8	V
V_{IH}	Input high voltage		2.4	–	V_{CC} +0.3	V
I_{CCSB}	Standby supply current	$\overline{CE}$ = V_{CC}, I_{OUT} = 0mA V_{IN} = GND or V_{CC}			10	μA
I_{CCOP}	Operation supply current	f = 1 MHZ, I_{OUT} = 0 mA V_{IH} = V_{CC} V_{IL} = GND			7	mA
I_{CCDR}	Data retention supply current	V_{CC} = $\overline{CE}$ = 3V I_{OUT} = 0mA V_{IN} = GND or V_{CC}			5	μA
V_{CCDR}	Data retention supply voltage	$\overline{CE}$ = high	2.0			V
I_{LI}	Input leakage current	GND V_{IN} V_{CC}	−1.0	–	1.0	μA
I_{LO}	Output leakage current	GND V_{OUT} V_{CC}	−1.0	–	1.0	μA
V_{OL}	Output low voltage	I_{OL} = 3.2mA			0.4	V
V_{OH}	Output high voltage	I_{OH} = −1.0mA	2.4			V

Capacitance

(T_A = 25°C f = 1.0 MHz)

Symbol	Parameter	Test Conditions	Limits		Unit
			Typ.	Max.	
C_{IN}	Input capacitance	All pins except pin under		7	pF
C_{OUT}	Output capacitance	test tied to AC ground		10	pF

Note: This parameter is periodically sampled and is not 100% tested.

A.C. Electrical Characteristics

(T_A = 0 to 70°C, V_{CC} = 4.5 to 5.5V)

Symbol		Parameter	UM6104		UM6104-2		UM6104-3		UM6104-4		Unit
Conventional	Standard		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CA}	T_{ELQV}	Chip enable access time		250		200		150		120	ns
t_{COE}	T_{ELQX}	Chip enable output enable time		50	20		20		10		ns
t_{COZ}	T_{EHOZ}	Chip enable output disable time		80		80		60		50	ns
t_{WOZ}	T_{WLQZ}	Write enable output disable time		80		80		60		50	ns
t_{CE}	T_{ELEH}**	Chip enable pulse engative width	250		200		150		120		ns
t_{CE}	T_{EHEL}	Chip enable pulse positive width	100		80		70		50		ns
t_{AS}	T_{AVEL}	Address setup time	20		20		20		20		ns
t_{AH}	T_{ELAX}	Address hold time	100		80		60		40		ns
t_{RS}	T_{WHEL}	Read setup time	0		0		0		0		ns
t_{RH}	T_{EHWL}	Read hold time	0		0		0		0		ns
t_{RD}	T_{ELWL}	Read enable time	250		200		150		120		ns
t_{WS}	T_{WLEL}	Write setup time	–20		–20		–20		–20		ns
t_{WD}	T_{ELWH}	Write enable time	250		200		150		120		ns
t_{DS}	T_{DVEH}	Input data setup time	200		150		100		70		ns
t_{DH}	T_{EHDX}	Input data hold time	0		0		0		0		ns
t_{OH}	T_{EHQX} / T_{WLQX}	Output data hold time	0		0		0		0		ns
t_{C}*	T_{ELEL}	Read or Write cycle time	350		280		220		170		ns

Notes:

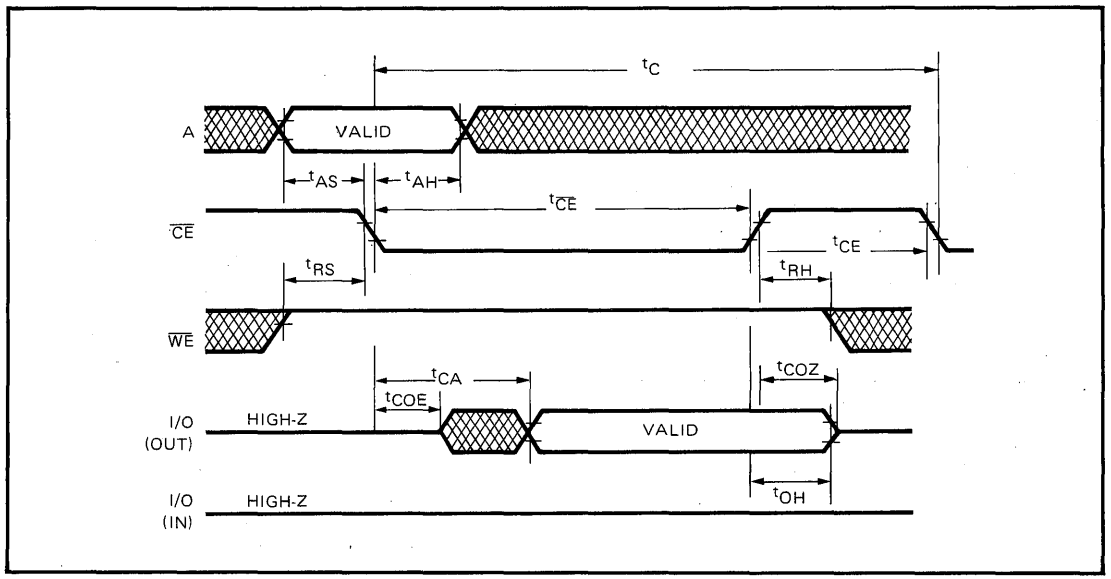
*: $T_{ELEL} = T_{ELEH} + T_{EHEL} + T_R + T_F$

**: For Read Modify Write cycle, $T_{ELEH} = T_{ELWL} + T_{WLEH} + T_F$

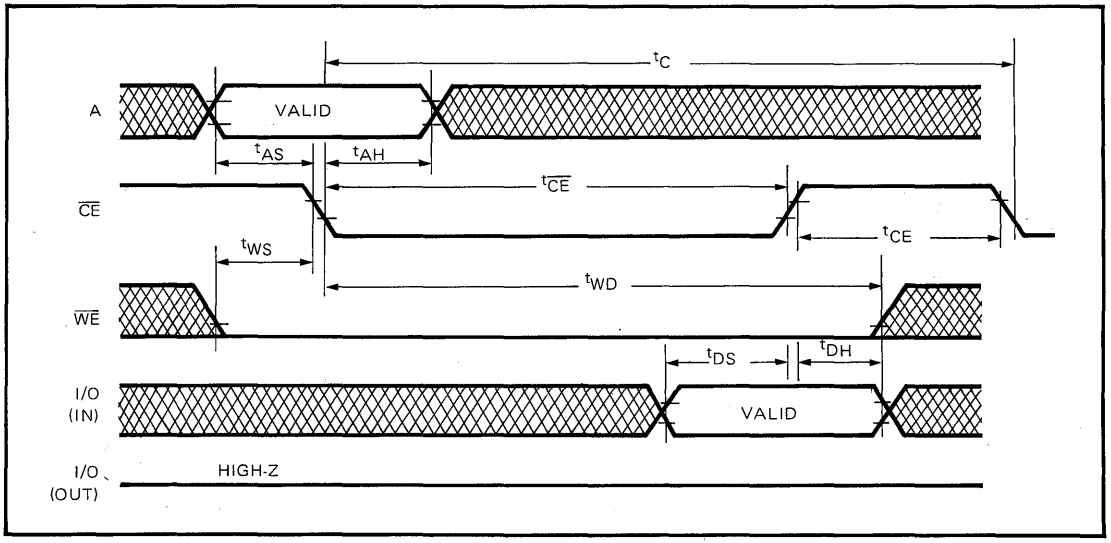
A. C. Test Conditions

Input pulse levels: 0.6V to 2.4V
Input pulse rise & fall times (T_R & T_F): 10 ns
Timing measurement levels: input: V_{IL} = 0.8V V_{IH} = 2.2V
output: V_{OL} = 0.6V V_{OH} = 2.4V
output load: 1 TTL GATE and C_L = 100pF

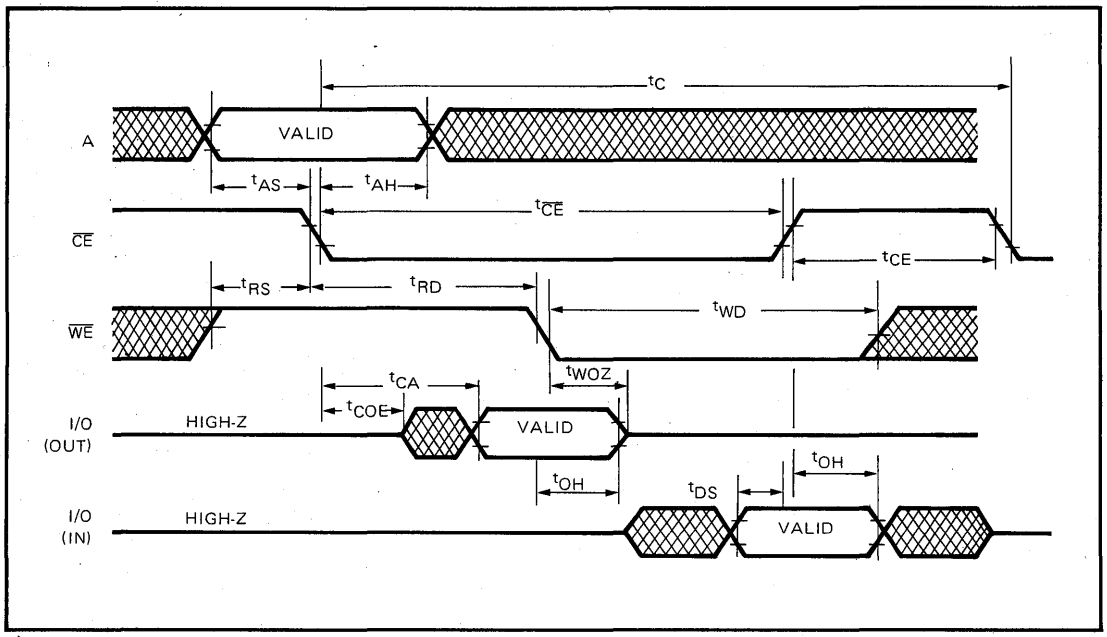
Read Cycle Timing Diagram



Write Cycle Timing Diagram



Read Modify Write Cycle Timing Diagram



Ordering Information

Part Number	Access Time (Max.)	Package
UM6104	250 ns	Plastic
UM6104–2	200 ns	Plastic
UM6104–3	150 ns	Plastic
UM6104–4	120 ns	Plastic
UM6104J	250 ns	CERDIP
UM6104J–2	200 ns	CERDIP
UM6104J–3	150 ns	CERDIP
UM6104J–4	120 ns	CERDIP

UM6104-1

1K × 4 CMOS SRAM

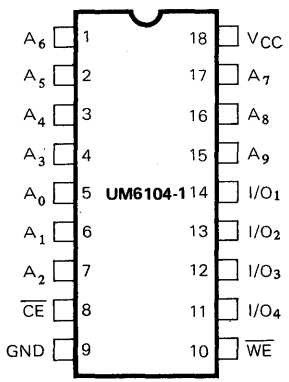
Features

- 2.5V minimum operating voltage
- Low power standby
- Low power operation
- Chip access time: 2.0 μs
- Data retention: 2.0V min.
- Three-state outputs
- On-chip address register
- Synchronous circuitry
- Standard 18 pin DIP package
- No clock required (complete static circuit)

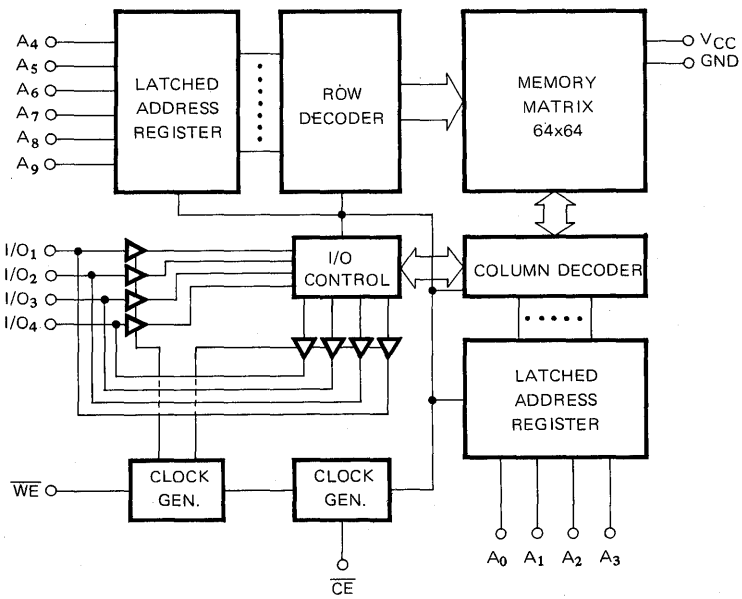
General Description

The UM6104-1 is a nonclocked CMOS static RAM organized as 1024 words by 4-bits. Since 1Kx4 CMOS static RAM is usually used in low voltage or low power consumption situation, such as telephonic equipments and portable equipments, UMC creates a new product version, UM6104-1 to serve these requirements. UM6104-1 dissipates very little current at the data retention mode and is suitable for use in non-volatile RAM applications with battery backup.

Pin Configuration



Block Diagram



Absolute Maximum Ratings

Ambient temperature under bias, T_A . . . . . −10 to +80°C
Storage temperature, T_{ST} . . . . . − 55 to +125°C
Input voltage, V_{IN} . . . . . −0.3 to V_{CC} +0.3V
Output voltage, V_{OUT} . . . . . −0.3 to V_{CC} +0.3V
Maximum power supply voltage, V_{CC} max. . . . . +7.0V

*Comments

Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

D.C. Electrical Characteristics

(T_A = 0 to 70°C, GND = 0V, V_{CC} = 2.5 to 5.5V unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
V_{CC}	Supply Voltage		2.5	3.0	5.5	V
V_{IL}	Input Low Voltage		−0.3	–	0.4	V
V_{IH}	Input High Voltage		2.2	–	V_{CC} +0.3	V
I_{CCSB}	Standby Supply Current	$\overline{CE}$ = V_{CC}, I_{OUT} = 0mA V_{IN} = GND or V_{CC}			3.0	μA
I_{CCOP}	Operation Supply Current	f = 400 KHz, I_{OUT} = 0mA V_{IH} = V_{CC} V_{IL} = GND			5.0	mA
I_{CCDR}	Data Retention Supply Current	V_{CC} = $\overline{CE}$ = 1.5V I_{OUT} = 0mA V_{IN} = GND or V_{CC}			1.0	μA
V_{CCDR}	Data Retention Supply Voltage	$\overline{CE}$ = high	1.5			V
I_{LI}	Input Leakage Current	GND V_{IN} V_{CC}	−1.0	–	1.0	μA
I_{LO}	Output Leakage Current	GND V_{OUT} V_{CC}	−1.0	–	1.0	μA
V_{OL}	Output Low Voltage	I_{OL} = 3.2mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −1.0mA	2.4			V

Capacitance

(T_A = 25°C f = 400 KHz)

Symbol	Parameter	Test Conditions	Limits		Unit
			Typ.	Max.	
C_{IN}	Input Capacitance	All pins except pin under		7	pF
C_{OUT}	Output Capacitance	test tied to AC ground		10	pF

Note:
This parameter is periodically sampled and is not 100% tested.

A.C. Electrical Characteristics

(T_A = 0 to 70°C, V_{CC} = 2.5 to 5.5V)

Symbol		Parameter	Limits		Units
Conventional	Standard		Min.	Max.	
t_{CA}	T_{ELQV}	Chip enable access time		2.0	μs
t_{COE}	T_{ELQX}	Chip enable output enable time		100	ns
t_{COZ}	T_{EHQZ}	Chip enable output disable time		500	ns
t_{WOZ}	T_{WLQZ}	Write enable output disable time		500	ns
$t_{\overline{CE}}$	T_{ELEH}**	Chip enable pulse negative width	2.0		μs
t_{CE}	T_{EHEL}	Chip enable pulse positive width	500		ns
t_{AS}	T_{AVEL}	Address setup time	100		ns
t_{AH}	T_{ELAX}	Address hold time	0		ns
t_{RS}	T_{WHEL}	Read setup time	0		ns
t_{RH}	T_{EHWL}	Read hold time	0		ns
t_{RD}	T_{ELWL}	Read enable time	2.0		μs
t_{WS}	T_{WLEL}	Write setup time	−100		ns
t_{WD}	T_{ELWH}	Write enable time	2.0		μs
t_{DS}	T_{DVEH}	Input data setup time	1.5		μs
t_{DH}	T_{EHDX}	Input data hold time	0		ns
t_{OH}	T_{EHQX} / T_{WLQX}	Output data hold time	0		ns
t_{C}*	T_{ELEL}	Read or write cycle time	2.5		μs

Notes:

*: $T_{ELEL} = T_{ELEH} + T_{EHEL} + T_R + T_F$

**: For Read Modify Write cycle, $T_{ELEH} = T_{ELWL} + T_{WLEH} + T_F$

AC Test Conditions

Input pulse levels: 0.6V to 2.4V

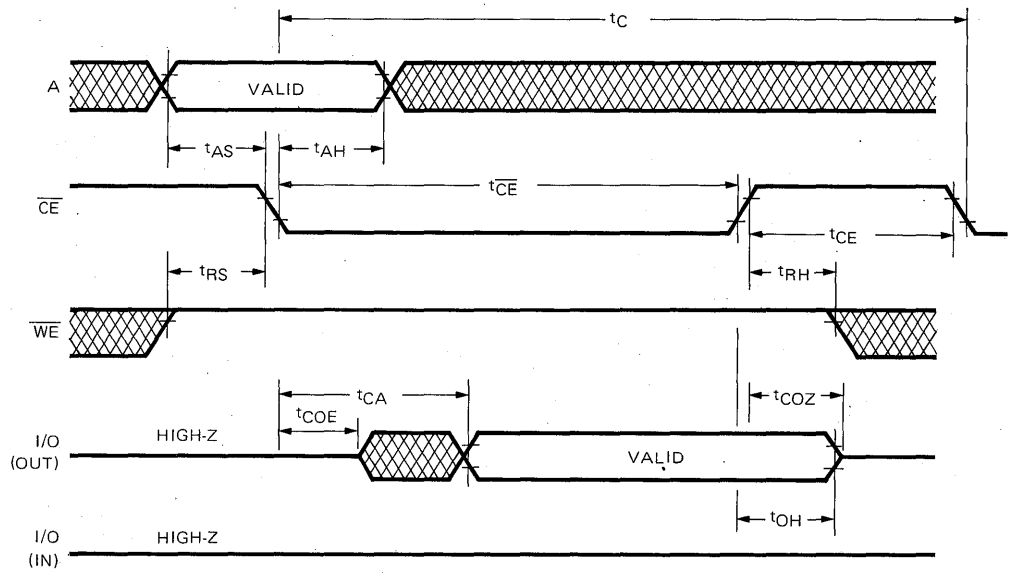
Input pulse rise & fall times (T_R & T_F): 10 ns

Timing measurement levels: input: V_{IL} = 0.8V V_{IH} = 2.2V

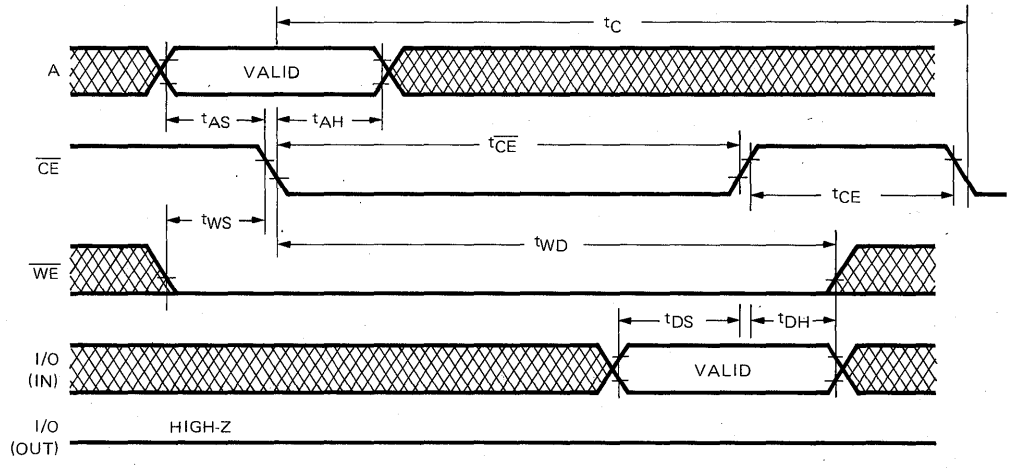
output: V_{OL} = 0.6V V_{OH} = 2.4V

Output load: 1 TTL GATE and C_L = 100 pF

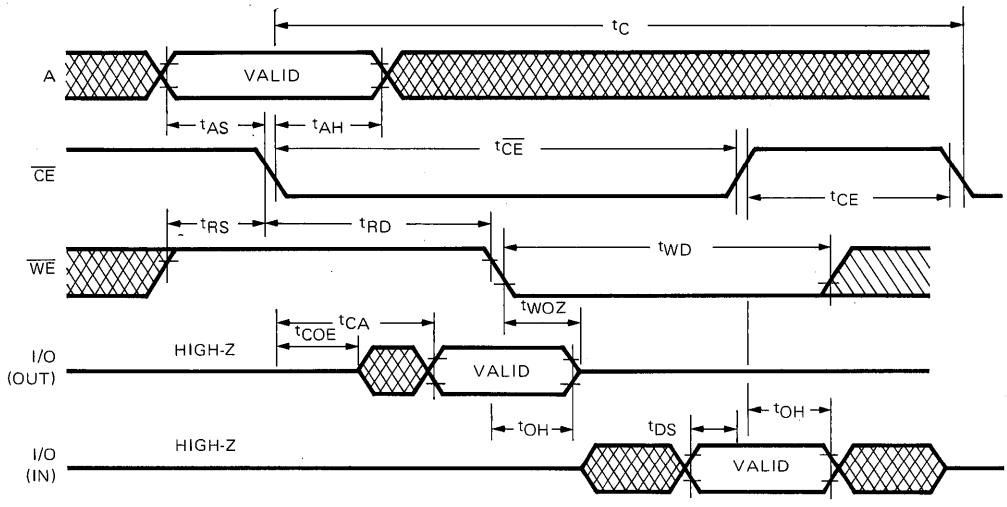
READ CYCLE TIMING DIAGRAM



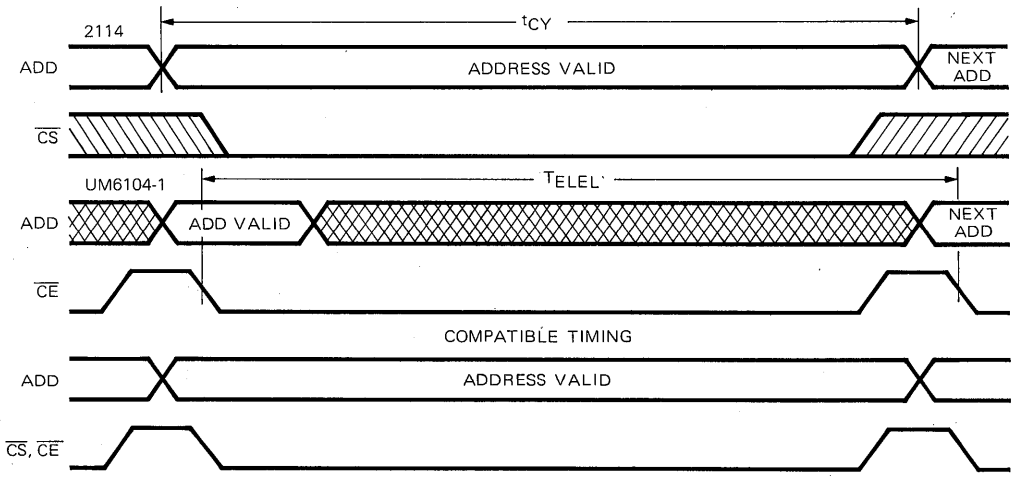
WRITE CYCLE TIMING DIAGRAM



READ MODIFY WRITE CYCLE TIMING DIAGRAM



2114 COMPATIBILITY



2114 – REQUIRES THE ADDRESS TO REMAIN VALID THROUGHOUT THE CYCLE.

UM6104-1 – REQUIRES VALID ADDRESS FOR ONLY A SMALL PORTION OF THE CYCLE, BUT REQUIRES $\overline{CE}$ t_C FALL TO INITIATE EACH CYCLE.

SRAM

UM6114

1K × 4 CMOS SRAM

Features

- High speed—45/55/70/90 ns (max.)
- Low power dissipation:
  50mW (Typ.) operating
  5μW (Typ.) standby
- Single 5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three state outputs
- Data retention supply voltage: 2.0—5.5V

General Description

The UM6114 is a 4,096 bit high speed and low power static random access memory organized as 1,024 words by 4 bits using CMOS technology, and operates from a single 5-volt supply.

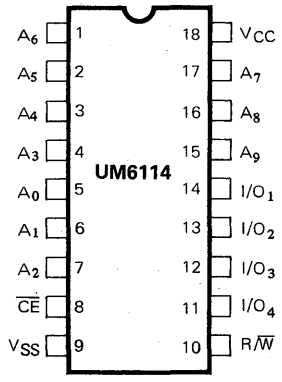
The UM6114 is compatible with the industry produced NMOS 2148 type 4K RAM, yet offers a more than 90% reduction in power of their NMOS equivalents.

The UM6114 is a fully CMOS RAM, therefore it is suited for use in low power applications where battery operation and battery back up for nonvolatility are required.

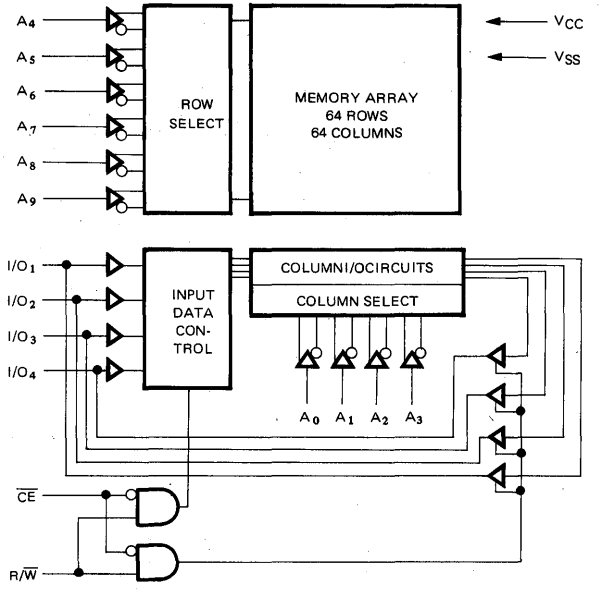
The UM6114 is guaranteed for data retention at a power supply as low as 2 volts. The UM6114 is directly TTL compatible in all inputs and outputs.

The UM6114 is offered in both standard 18 pin plastic and cerdip packages, 0.3 inches in width.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Supply Voltage V_{CC} -V_{SS} . . . . . −0.3V to 7V
Input Voltage V_{IN} . . . . . −0.3V to 7V
Input/Output Voltage Applied $V_{I/O}$ −0.3V to V_{CC} +0.3V
Temp Under Bias T_{BIAS} Ceramic. . . . . −55°C to 125°C
Temp Under Bias T_{BIAS} Plastic. . . . . −10°C to 85°C
Storage Temperature T_{STG} Ceramic . . −65°C to +150°C
Storage Temperature T_{STG} Plastic . . . . −40°C to +125°C
Power Dissipation P_T 1.0W
DC Output Current I_{OUT} 50mA

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Pin Names

A_0–A_9	ADDRESS
I/O_1–I/O_4	DATA INPUT/OUTPUT
CE	CHIP ENABLE INPUT
R/$\overline{W}$	READ WRITE CONTROL INPUT
V_{CC}/V_{SS}	POWER SUPPLY TERMINALS

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

SRAM

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	V_{CC} +0.3	V
V_{IL}	Input Low Voltage	−.3	–	+0.8	V
C_L	Output Load	–	–	30	pF
TTL	Output Load	–	–	1	–

D.C. Electrical Characteristics over the operating range

Symbol	Parameter	Test Conditions	6114-3			6114-2			6114-1			6114			Units
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}	–	–	±10	–	–	±10	–	–	±10	–	–	±10	μA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH} $V_{I/O}$ = GND to V_{CC}	–	–	±10	–	–	±10	–	–	±10	–	–	±10	μA
I_{CC}	Operating Power Supply Current	$\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA	–	15	30	–	15	30	–	15	30	–	20	40	mA
I_{CC1}		V_{IH} = 3.5V, V_{IL} = 0.6V $I_{I/O}$ = 0mA	–	10	–	–	10	–	–	10	–	–	10	–	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle =100%	–	–	50	–	–	50	–	–	50	–	–	50	mA
I_{SB}	Standby Power Current	$\overline{CE}$ = V_{IH}	–	5	10	–	5	10	–	5	10	–	5	10	mA
I_{SB1}		$\overline{CE}$ ≥ V_{CC}−0.2V, V_{IN} ≥ V_{CC}−0.2V or V_{IN} ≤ 0.2V	–	1	20	–	1	20	–	1	20	–	1	200	μA
V_{OL}	Output Low Voltage	I_{OL} = 2.4 mA	–	–	0.4	–	–	0.4	–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −1.0mA	2.4	–	–	2.4	–	–	2.4	–	–	2.4	–	–	V

*V_{CC} = 5V, T_A = 25°C

Truth Table

Mode	$\overline{CE}$	$\overline{R/W}$	I/O Operation
Standby	H	X	High Z
Read	L	H	D_{OUT}
Write	L	L	D_{IN}

Capacitance*

(T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} =0V	8	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ =0V	10	pF

* This parameter is periodically sampled and not 100% tested.

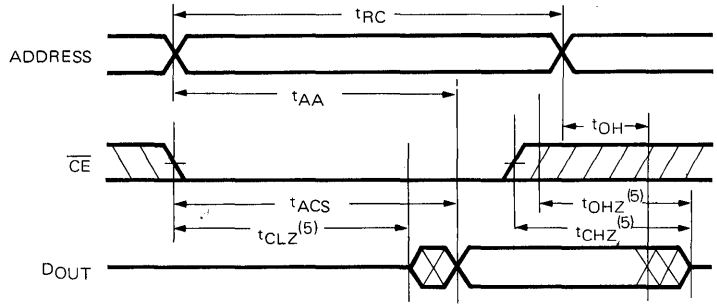
A.C. Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	1 TTL Gate and C_L = 30pF (Including scope and jig)

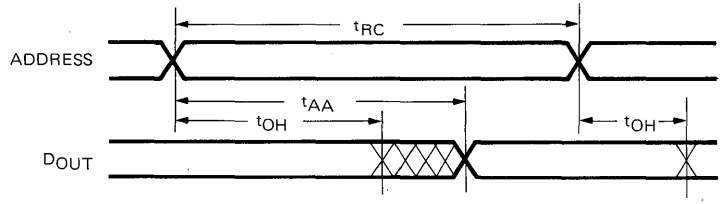
A.C. Electrical Characteristics over the operating range

Symbol	Parameter	6114-3 Min.	6114-3 Max.	6114-2 Min.	6114-2 Max.	6114-1 Min.	6114-1 Max.	6114 Min.	6114 Max.	Unit
READ CYCLE										
t_{RC}	Read Cycle Time	45	–	55	–	70	–	90	–	ns
t_{AA}	Address Access Time	–	45	–	55	–	70	–	90	ns
t_{ACS}	Chip Enable Access Time	–	45	–	55	–	70	–	90	ns
t_{CLZ}	Chip Enable to Output in Low Z	5	–	5	–	5	–	5	–	ns
t_{CHZ}	Chip Enable to Output in High Z	0	30	0	30	0	35	0	40	ns
t_{OHZ}	Output Disable to Output in High Z	0	25	0	30	0	35	0	40	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	45	–	55	–	70	–	90	–	ns
t_{CW}	Chip Enable to End of Write	40	–	40	–	45	–	55	–	ns
t_{AW}	Address Valid to End of Write	40	–	50	–	60	–	80	–	ns
t_{AS}	Address Set-up Time	5	–	5	–	10	–	10	–	ns
t_{WP}	Write Pulse Width	40	–	45	–	45	–	55	–	ns
t_{WR}	Write Recovery Time	5	–	5	–	5	–	5	–	ns
t_{WHZ}	Write to Output in High Z	0	25	0	25	0	40	0	50	ns
t_{DW}	Data to Write Time Overlap	25	–	25	–	30	–	30	–	ns
t_{DH}	Data Hold from Write Time	5	–	5	–	5	–	5	–	ns
t_{OW}	Output Active from End of Write	0	–	0	–	0	–	0	–	ns

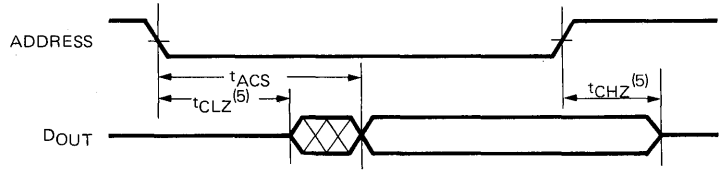
Timing Waveforms of Read Cycle No. 1[1]



READ CYCLE 2[1,2,]

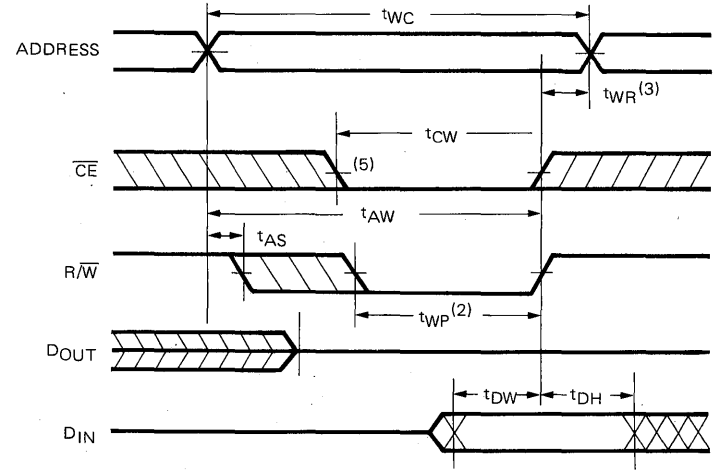


READ CYCLE 3[1,3]

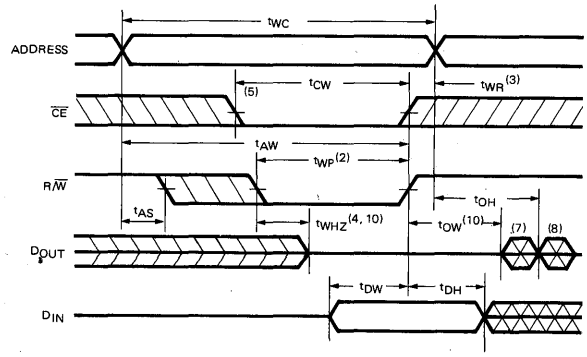


Notes:
1. R/W is High for Read Cycle.
2. Device is continuously selected, $\overline{CE} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CE}$ transition low.
4. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

Timing Waveforms of Write Cycle 1[1]



WRITE CYCLE 2[1]



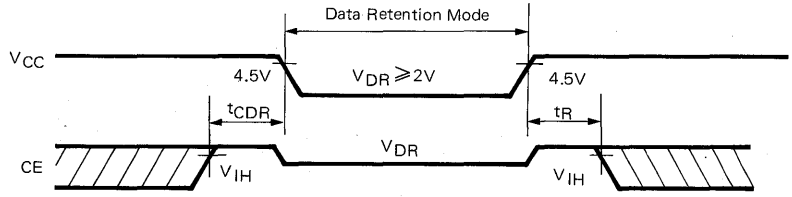
Notes:
1. R/W must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low CE and a low R/W.
3. tWR is measured form the earlier of CE or R/W going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
5. If the CE low transition occures simultaneously with the R/W low transitions or after the R/W transition, outputs remain in a high impedance state.
7. Dout is the same phase of write data of this write cycle.
8. Dout is the read data of next address.
9. If CE is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

Data Retention Characteristics over the operating temperature range

Symbol	Parameter	Test Conditions	Min.	Typ.[1]	Max.	Units
V_{DR}	V_{CC} for Retention Data	$\overline{CE} = V_{CC}$	2.0	–	–	V
I_{CCDR}	Data Retention Current	$V_{IN} = 0V$ or V_{CC}	–	2	20	μA
t_{CDR}	Chip Deselect to Data Retention Time	$V_{CC} = 2.0V$, $\overline{CE} = V_{CC}$	0	–	–	ns
t_R	Operation Recovery Time	$V_{IN} = 0V$ or V_{CC}	t_{RC}[2]	–	–	ns

1. $V_{CC} = 2V$, $T_A = +25°C$
2. I_{RC} = Read Cycle Time

Timing Waveform Low V_{CC} Data Retention Waveform



Ordering Information

Part Number	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)	Package Type
UM6114	90 ns	30 mA	10 mA	Plastic
UM6114-1	70 ns	30 mA	10 mA	Plastic
UM6114-2	55 ns	30 mA	10 mA	Plastic
UM6114-3	45 ns	40 mA	10 mA	Plastic
UM6114J	90 ns	30 mA	10 mA	CERDIP
UM6114J-1	70 ns	30 mA	10 mA	CERDIP
UM6114J-2	55 ns	30 mA	10 mA	CERDIP
UM6114J-3	45 ns	40 mA	10 mA	CERDIP

UM6116-2/UM6116-3/UM6116-4

2K × 8 High Speed CMOS SRAM

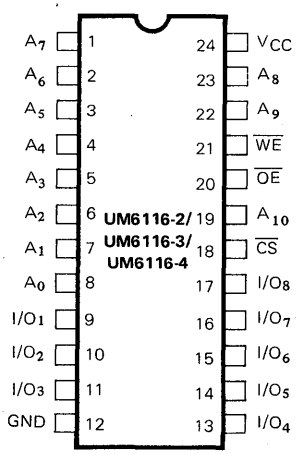
Features

- Single 5V supply and high density 24 pin package
- High speed: Fast access time
  70ns/90ns/120ns (max.)
- Low power standby and Low power operation
  Standby: 5μW (typ.)
  Operation: 250mW (typ.)
- Completely static RAM: No clock or timing strobe required
- Directly TTL compatible: All input and output
- Pin compatible with standard 16K EPROM/Mask ROM
- Equal access and cycle time

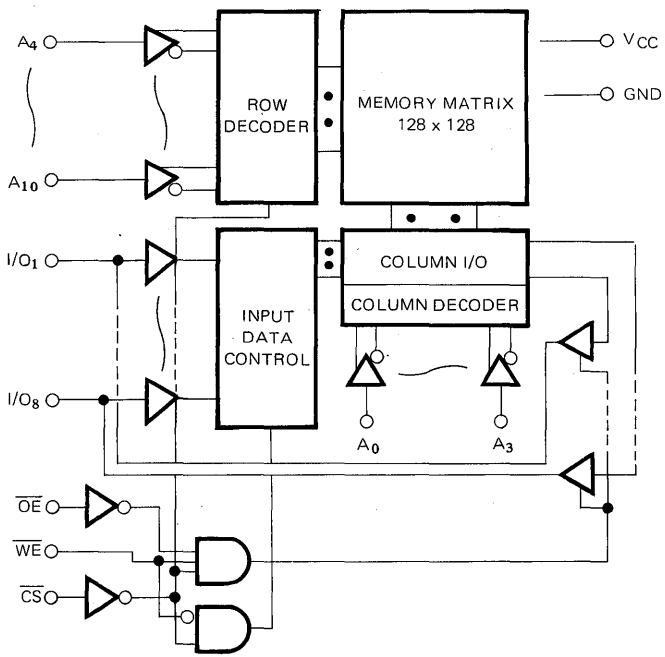
General Description

The UM6116 is a 16,384-bit static random access memory organized as 2048 words by 8 bits and operates from a signle 5 volt supply. It is built with UMC's high performance CMOS process. Six-transistor full CMOS memory cell provides low standby current and high-reliability. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures. The UM6116 is moulded in a standard 24-pin 600mil-DIP.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Voltage on Any Pin Relative to GND, V_T −0.3V to +7.0V
Operating Temperature, T_{opr} . . . . . 0°C to +70°C
Storage Temperature (Plastic), T_{stg}. . . . −55°C to +125°C
Temperature Under Bias, T_{bias} . . . . . −10°C to +85°C
Power Dissipation, P_T 1.0W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin
H	x	x	standby	I_{SB}, I_{SBT}	High Z
L	L	H	Read	I_{CC}	Dout
L	H	H	Read	I_{CC}	High Z
L	x	L	Write	I_{CC}	Din

DC and Operating Characteristics

(V_{CC} = 5V ± 5%, GND = 0V, T_A = 0 to +70°C)

Item	Symbol	Test Conditions	6116-4			6116-3			6116-2			Units
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input Leakage Current	I_{L1}	V_{CC}=5.5V, V_{IN}=GND to V_{CC}	–	–	10	–	–	10	–	–	10	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH}, $V_{I/O}$=GND to V_{CC}	–	–	10	–	–	10	–	–	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	–	50	100	–	50	100	–	50	100	mA
	I_{CC1}	V_{IH}=3.5V, V_{IL}=0.6V, $I_{I/O}$=0mA	–	45	–	–	45	–	–	45	–	mA
Dynamic Operating Current	I_{CC2}	Min. cycle, duty=100%	–	–	100	–	–	100	–	–	100	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}	–	5	10	–	5	15	–	5	10	mA
	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, V_{IN}≥V_{CC} -0.2V or V_{IN}≤0.2V	–	1	50	–	1	500	–	1	50	μA
Output Voltage	V_{OL}	I_{OL}=4mA	–	–	0.4	–	–	0.4	–	–	0.4	V
	V_{OH}	I_{OH}=-1.0mA	2.4	–	–	2.4	–	–	2.4	–	–	V
Input Voltage	V_{IH}		2.2	3.5	5.8	2.2	3.5	5.8	2.2	3.5	5.8	V
	V_{IL}		-0.3	–	+0.8	-0.3	–	+0.8	-0.3	–	+0.8	V

*V_{CC}=5V, T_A=25°C

A.C. Characteristics

(V_{CC} = 5V ± 5%, T_A = 0 to +70°C)

A.C. Test Conditions

Input Pulse Levels: 0V to 3.0V
Input Rise and Fall Times: 5ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

READ CYCLE

Item	Symbol	6116-4		6116-3		6116-2		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	70	–	90	–	120	–	ns
Address Access Time	t_{AA}	–	70	–	90	–	120	ns
Chip Select Access Time	t_{ACS}	–	70	–	90	–	120	ns
Chip Selection to Output in Low Z	t_{CLZ}	5	–	5	–	10	–	ns
Output Enable to Output Valid	t_{OE}	–	50	–	65	–	80	ns
Output Enable to Output in Low Z	t_{OLZ}	5	–	5	–	10	–	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	35	0	40	0	40	ns
Chip Disable to Output in High Z	t_{OHZ}	0	35	0	40	0	40	ns
Output Hold from Address Change	t_{OH}	5	–	5	–	10	–	ns

WRITE CYCLE

Item	Symbol	6116-4		6116-3		6116-2		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	70	–	90	–	120	–	ns
Chip Selection to End of Write	t_{CW}	45	–	55	–	70	–	ns
Address Valid to End of Write	t_{AW}	65	–	80	–	105	–	ns
Address Set Up Time	t_{AS}	10	–	10	–	20	–	ns
Write Pulse Width	t_{WP}	45	–	55	–	70	–	ns
Write Recovery Time	t_{WR}	5	–	5	–	5	–	ns
Output Disable to Output in High Z	t_{OHZ}	0	35	0	40	0	40	ns
Write to Output in High Z	t_{WHZ}	0	40	0	50	0	50	ns
Data to Write Time Overlap	t_{DW}	30	–	30	–	35	–	ns
Data Hold from Write Time	t_{DH}	5	–	5	–	5	–	ns
Output Active from End of Write	t_{OW}	0	–	0	–	5	–	ns

Capacitance* (f = 1MHz, T_A = 25°C)

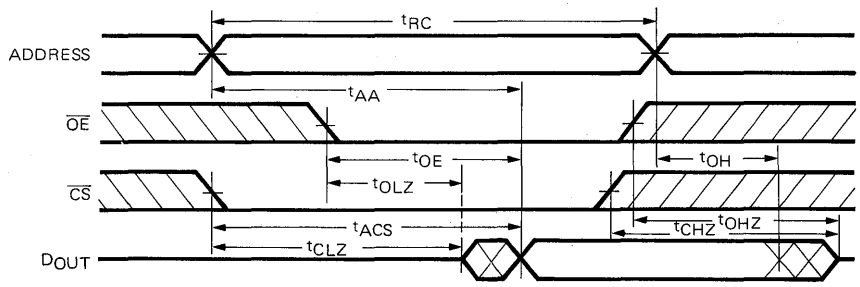
Item	Symbol	Test Conditions	Max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	8	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	10	pF

*This parameter is sampled and not 100% tested.

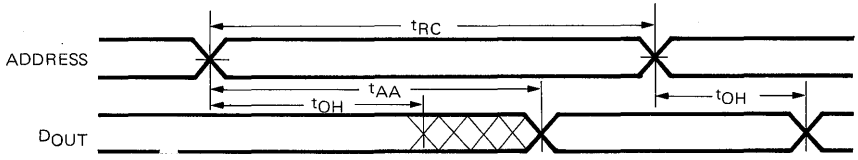
SRAM

Timing Waveform

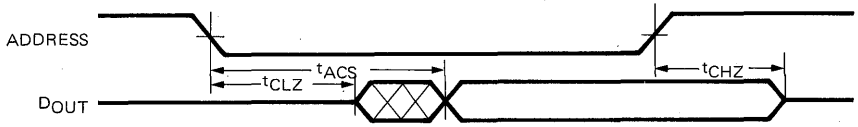
READ CYCLE (1)[1][5]



READ CYCLE (2)[1][2][4]

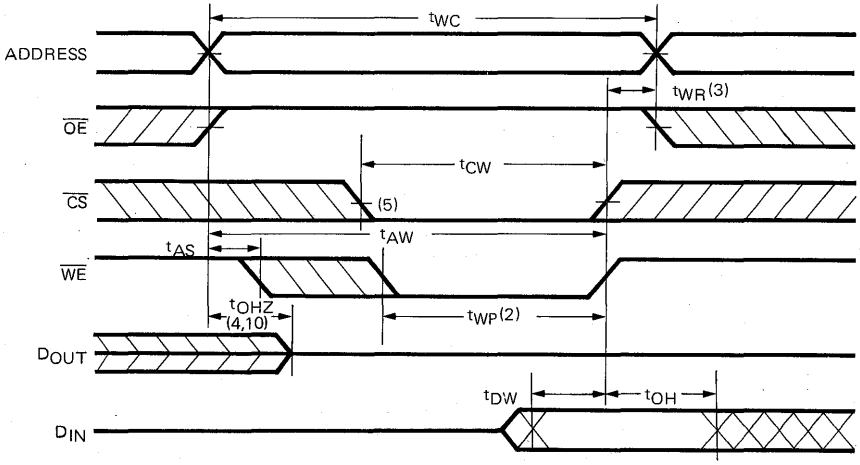


READ CYCLE (3)[1][3][4][5]

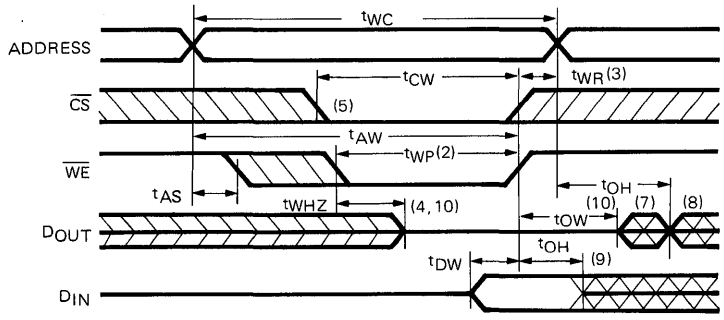


Notes:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

WRITE CYCLE (1)



WRITE CYCLE (2) (1)(6)



Notes:.

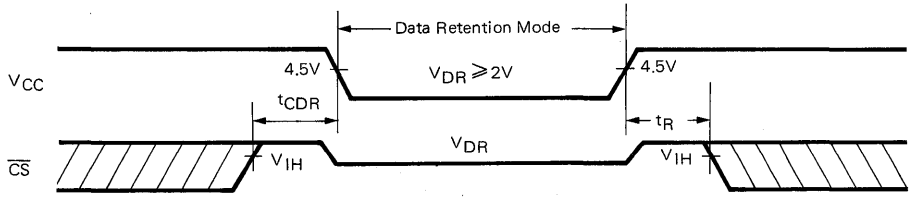
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

Data Retention Characteristics over the operating temperature range

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Units
V_{DR}	V_{CC} for Retention Data	$\overline{CS} = V_{CC}$	2.0	–	–	V
I_{CCDR}	Data Retention Current	V_{IN} = 0V or V_{CC}	–	2	20	μA
t_{CDR}	Chip Deselect to Data Retention Time	V_{CC} = 2.0V, CS = V_{CC}	0	–	–	ns
t_R	Operation Recovery Time	V_{IN} = 0V or V_{CC}	t_{RC}(2)	–	–	ns

1. V_{CC} = 2V, T_A = +25°C
2. I_{RC} = Read Cycle Time

Timing Waveform Low V_{CC} Data Retention Waveform



Ordering Information

Part Number	Access Time (Max.)	Package
UM6116-2	120 ns	Plastic
UM6116-3	90 ns	Plastic
UM6116-4	70 ns	Plastic
UM6116J-2	120 ns	CERDIP
UM6116J-3	90 ns	CERDIP
UM6116J-4	70 ns	CERDIP

UM6116-5

2K × 8 High Speed CMOS SRAM

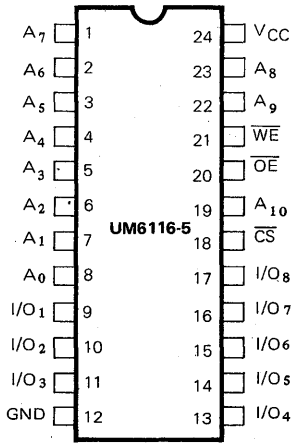
Features

- Single 5V supply and high density 24 pin package
- High speed: Fast access time 55ns (max.)
- Low power standby and Low power operation — Standby: 5μW (typ.); Operation: 250mW (typ.)
- Completely static RAM: No clock or timing strobe required
- Directly TTL compatible: All input and output
- Pin compatible with standard 16K EPROM/Mask ROM
- Equal access and cycle time

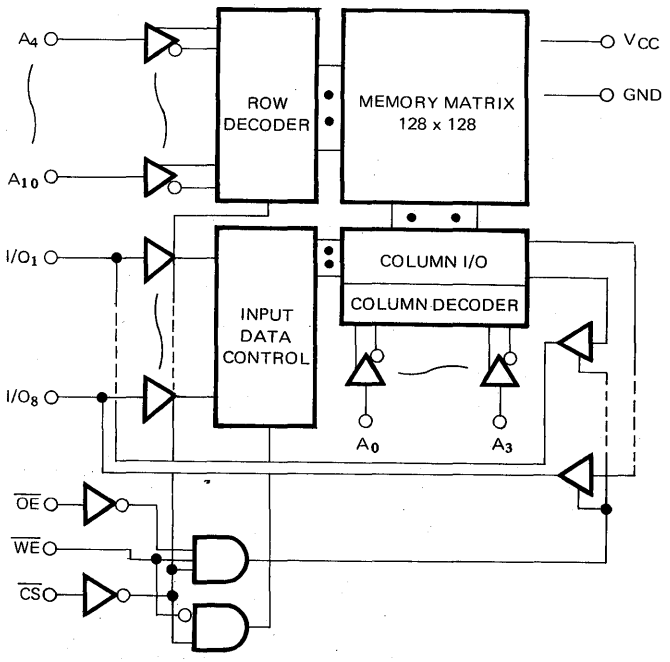
General Description

The UM6116 is a 16,384-bit static random access memory organized as 2048 words by 8 bits and operates from a signle 5 volt supply. It is built with UMC's high performance CMOS process. Six-transistor full CMOS memory cell provides low standby current and high-reliability. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures. The UM6116 is moulded in a standard 24-pin 600mil-DIP.

Pin Configuration



Block Diagram



Absolute Maximum Ratings

Voltage on Any Pin Relative to GND, V_T . −0.3V to +7.0V
Operating Temperature, T_{opr} . . . . . 0°C to +70°C
Storage Temperature (Plastic), T_{stg} . . . −55°C to +125°C
Temperature Under Bias, T_{bias} . . . . . −10°C to +85°C
Power Dissipation, P_T 1.0W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin
H	x	x	Standby	I_{SB}, I_{SBT}	High Z
L	L	H	Read	I_{CC}	Dout
L	H	H	Read	I_{CC}	High Z
L	x	L	Write	I_{CC}	Din

D.C. and Operating Characteristics

(V_{CC} = 5V ± 5%, GND = 0V, T_A = 0 to +70° C)

Item	Symbol	Test Conditions	6116-5			Units
			Min.	Typ.*	Max.	
Input Leakage Current	I_{LI}	V_{CC} =5.5V, V_{IN}=GND to V_{CC}	–	–	10	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH}, $V_{I/O}$ =GND to V_{CC}	–	–	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$ =0mA	–	50	100	mA
	I_{CC1}	V_{IH} =3.5V, V_{IL}=0.6V, $I_{I/O}$ =0mA	–	45	–	mA
Dynamic Operating Current	I_{CC2}	Min. cycle, duty=100%	–	–	100	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}	–	5	10	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC}-0.2V, V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤0.2V	–	1	50	μA
Output Voltage	V_{OL}	I_{OL} = 4mA	–	–	0.4	V
	V_{OH}	I_{OH} =-1.0mA	2.4	–	–	V
Input Voltage	V_{IH}		2.2	3.5	5.8	V
	V_{IL}		-0.3	–	+0.8	V

*V_{CC} = 5V, T_A = 25°C

A.C. Characteristics (V_{CC} = 5V ± 5%, T_A = 0 to +70°C)

A.C. Test Conditions

Input Pulse Levels: 0V to 3.0V
Input Rise and Fall Times: 5ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 30pF (including scope and jig)

READ CYCLE

Item	Symbol	6116-5		Unit
		Min.	Max.	
Read Cycle Time	t_{RC}	55	–	ns
Address Access Time	t_{AA}	–	55	ns
Chip Select Access Time	t_{ACS}	–	55	ns
Chip Selection to Output in Low Z	t_{CLZ}	5	–	ns
Output Enable to Output Valid	t_{OE}	–	35	ns
Output Enable to Output in Low Z	t_{OLZ}	5	–	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	30	ns
Chip Disable to Output in High Z	t_{OHZ}	0	25	ns
Output Hold from Address Change	t_{OH}	5	–	ns

WRITE CYCLE

Item	Symbol	6116-5		Unit
		Min.	Max.	
Write Cycle Time	t_{WC}	55	–	ns
Chip Selection to End of Write	t_{CW}	40	–	ns
Address Valid to End of Write	t_{AW}	50	–	ns
Address Set Up Time	t_{AS}	5	–	ns
Write Pulse Width	t_{WP}	40	–	ns
Write Recovery Time	t_{WR}	5	–	ns
Output Disable to Output in High Z	t_{OHZ}	0	25	ns
Write to Output in High Z	t_{WHZ}	0	25	ns
Data to Write Time Overlap	t_{DW}	25	–	ns
Data Hold from Write Time	t_{DH}	5	–	ns
Output Active from End of Write	t_{OW}	0	–	ns

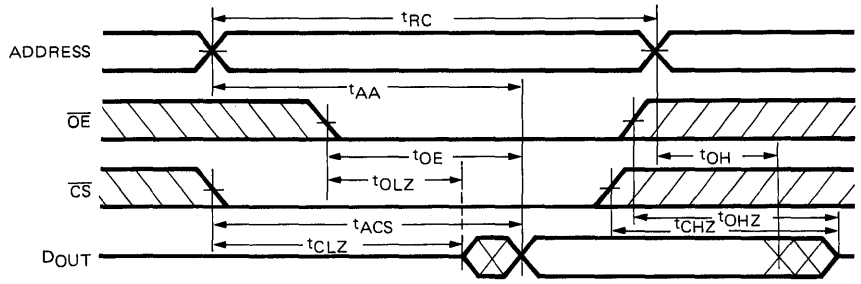
Capacitance* (f = 1MHz, T_A = 25°C)

Item	Symbol	Test Conditions	Max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	8	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	10	pF

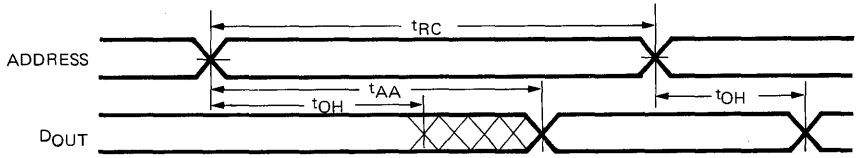
*This parameter is sampled and not 100% tested.

Timing Waveform

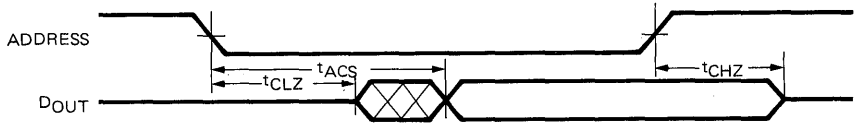
READ CYCLE (1)[1][5]



READ CYCLE (2)[1][2][4]

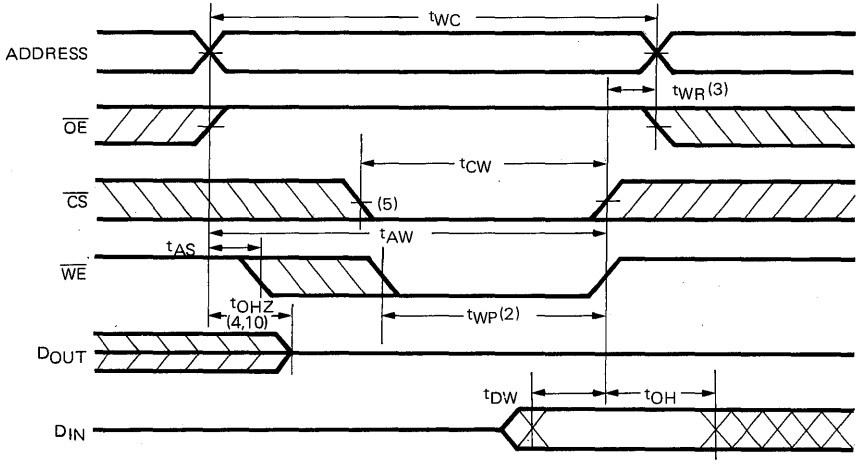


READ CYCLE (3)[1][3][4][5]



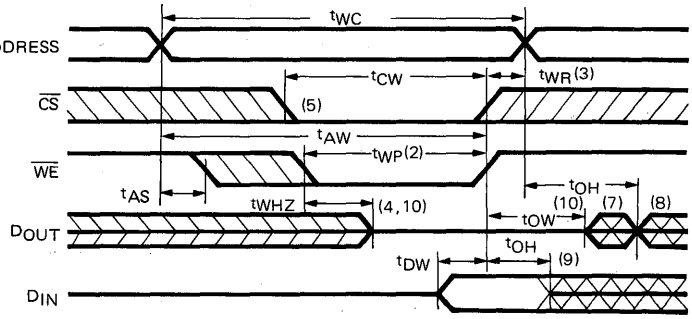
Notes:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

WRITE CYCLE (1)



SRAM

WRITE CYCLE (2) (1)(6)



Notes:

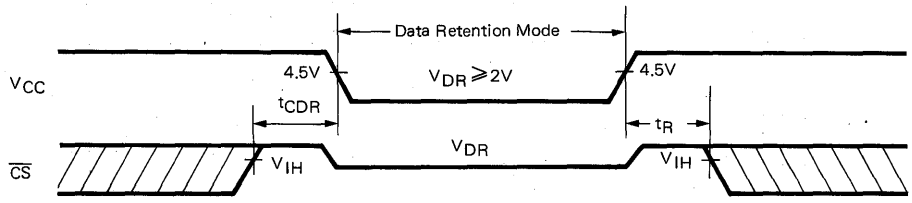
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

Data Retention Characteristics over the operating temperature range

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Units
V_{DR}	V_{CC} for Retention Data	$\overline{CS} = V_{CC}$	2.0	–	–	V
I_{CCDR}	Data Retention Current	V_{IN} = OV or V_{CC}	–	2	20	μA
t_{CDR}	Chip Deselect to Data Retention Time	V_{CC} = 2.0V, CS = V_{CC}	0	–	–	ns
t_R	Operation Recovery Time	V_{IN} = OV or V_{CC}	t_{RC} (2)	–	–	ns

1. V_{CC} = 2V, T_A = +25° C
2. I_{RC} = Read Cycle Time

Timing Waveform Low V_{CC} Data Retention Waveform



Ordering Information

Part Number	Access Time (Max.)	Package
UM6116-5	55 ns	Plastic
UM6116J-5	55 ns	CERDIP

UM6164

8K × 8 High Speed CMOS SRAM

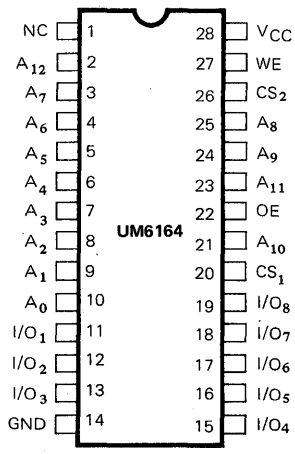
Features

- High-speed – 45/55/70ns (Max.)
- Low power dissipation
  300mW (Typ.) Operating
  100μW (Typ.) standby
- Single 5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three state outputs
- Data retention supply voltage: 2.0–5.5V

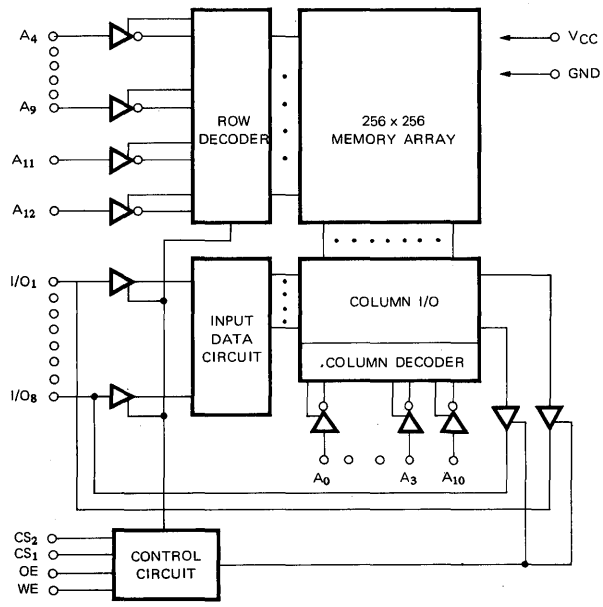
General Description

The UM6164 is a 65,536-bit static random access memory organized as 8192 words by 8 bits and operates from a single 5 volt supply. It is built with UMC's high performance twin tub CMOS process. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures. The UM6164 is moulded in a standard 28-pin, 600 mil-DIP.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Terminal Voltage with Respect to
GND (V_{TERM}) . . . . . −0.5V to +7.0V
Temperature Under Bias (T_{BIAS}) . . . . . −10°C to +125°C
Storage Temperature (T_{STG}) . . . . . −40° C to +150°C
Power Dissipation (P_T) 1.0W
DC Output Current (I_{OUT}) . . . . . 20 mA

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Pin Names

A_0–A_{12}	Address	WE	Write Enable
I/O_1–I/O_8	Data Input/Output	OE	Output Enable
CS_1	Chip Select One	CS_2	Chip Select Two
V_{CC}	Power	GND	Ground

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

D.C. Electrical Characteristics

(V_{CC} = 5V ±10%, GND = 0V, T_A = 0 to 70°C)

Symbol	Parameter	Test Conditions	Min.	Typ.[1]	Max.	Units
I_{LI}	Input leakage current	V_{IN} = GND to V_{CC}	–	–	5	μA
I_{LO}	Output Leakage Current	$CS_1 = V_{IH}$ or $CS_2 = V_{IL}$ or OE = V_{IH}, $V_{I/O}$ = GND to V_{CC}	–	–	5	μA
I_{CC}	Operating Power Supply Current	$CS_1 = V_{IL}$, $CS_2 = V_{IH}$, $I_{I/O}$ = 0mA	–	50	100	mA
I_{CC1}	Average Operating Current	Min, Duty Cycle = 100%, $CS_1 = V_{IL}$, $CS_2 = V_{IH}$	–	60	120	mA
I_{SB}	Standby Power Supply Current	$CS_1 = V_{IH}$ or $CS_2 = V_{IL}$, $I_{I/O}$ = 0mA	–	5	10	mA
I_{SB1}[2]		$CS_1 \geq V_{CC}-0.2V$, $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	–	.02	2	mA
I_{SB2}[2]		$CS_2 \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	–	.02	2	mA
V_{OL}	Output Voltage	I_{OL} = 2.1 mA	–	–	0.4	V
V_{OH}		I_{OH} = −1.0mA	2.4	–	–	V

1. Typical limits are at V_{CC} = 5.0V, T_A = 25° C and specified loading.
2. V_{IL} min = −0.3V

Recommended D.C. Operating Conditions

(T_A = 0 to +70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
G_{ND}	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	−0.5	0	0.8	V

Capacitance (1)

(T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	8	pF

Note: This parameter is sampled and not 100% tested.

A.C. Test Conditions

Parameter	Conditions
Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5 ns
Input and Output	1.5V
Timing Reference Level	
Output Load	1 TTL Gate and C_L = 30pF (including scope and jig)

SRAM

A.C. Electrical Characteristic

(over the operating range)

Symbol	Parameter		UM6164-2		UM6164-1		UM6164		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE									
t_{RC}	Read Cycle Time		45	–	55	–	70	–	
t_{AA}	Address Access Time		–	45	–	55	–	70	ns
t_{ACS1}	Chip Select Access Time	CS_1	–	45	–	55	–	70	ns
t_{ACS2}		CS_2	–	45	–	55	–	70	ns
t_{OE}	Output Enable to Output Valid		–	30	–	35	–	50	ns
t_{CLZ1}	Chip Selection to Output in Low Z	CS_1	5	–	5	–	5	–	ns
t_{CLZ2}		CS_2	5	–	5	–	5	–	ns
t_{OLZ}	Output Enable to Output in Low Z		5	–	5	–	5	–	ns
t_{CHZ1}	Chip Deselection to Output in High Z	CS_1	0	25	0	30	0	35	ns
t_{CHZ2}		CS_2	0	25	0	30	0	35	ns
t_{OHZ}	Output Disable to Output in High Z		0	25	0	30	0	35	ns
t_{OH}	Output Hold from Address Change		5	–	5	–	5	–	ns
WRITE CYCLE									
t_{WC}	Write Cycle Time		45	–	55	–	70	–	ns
t_{CW}	Chip Selection to End of Write		35	–	40	–	45	–	ns
t_{AS}	Address Setup Time		5	–	5	–	5	–	ns
t_{AW}	Address Valid to End of Write		40	–	50	–	65	–	ns
t_{WP}	Write Pulse Width		35	–	40	–	45	–	ns
t_{WR1}	Write Recovery Time	CS_1, WE	5	–	5	–	5	–	ns
t_{WR2}		CS_2	5	–	10	–	10	–	ns
t_{WHZ}	Write to Output in High Z		0	20	0	25	0	30	ns
t_{DW}	Data to Write Time Overlap		20	–	25	–	30	–	ns
t_{DH}	Data Hold from Write Time		5	–	5	–	5	–	ns
t_{OHZ}	OE to Output in High Z		0	25	0	25	0	25	ns
t_{OW}	Output Active from End of Write		5	–	5	–	5	–	ns

Note:

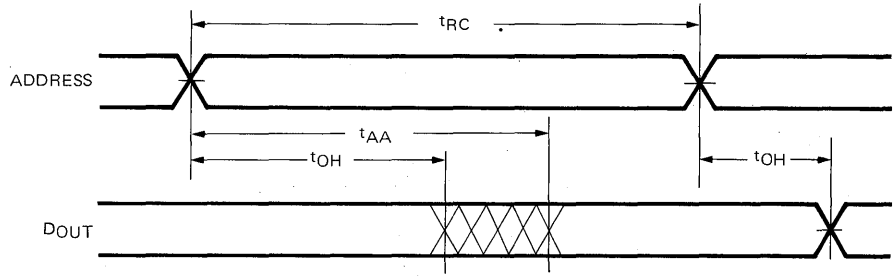
t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

Truth Table

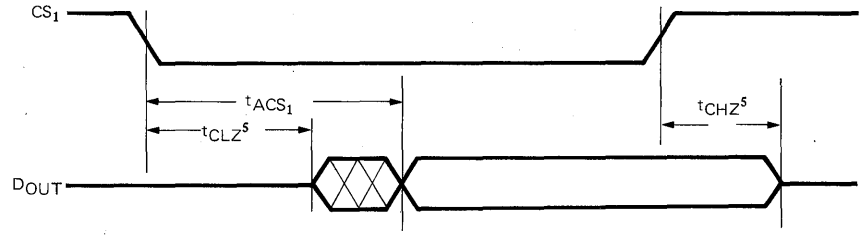
Mode	WE	CS_1	CS_2	OE	I/O Operation	V_{CC} Current	Notes
Not Selected (Power Down)	X	H	X	X	High Z	I_{SB}, I_{SB1}	
	X	X	L	X	High Z	I_{SB}, I_{SB2}	
Output Disabled	H	L	H	H	High Z	I_{CC}, I_{CC1}	
Read	H	L	H	L	D_{OUT}	I_{CC}, I_{CC1}	
Write	L	L	H	H	D_{IN}	I_{CC}, I_{CC1}	Write Cycle 1
	L	L	H	L	D_{IN}	I_{CC}, I_{CC1}	Write Cycle 2

Timing Waveforms

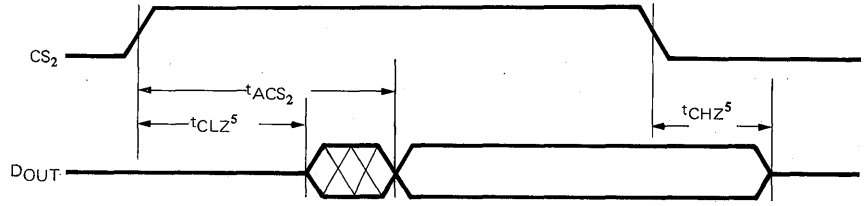
READ CYCLE[1, 2, 4]



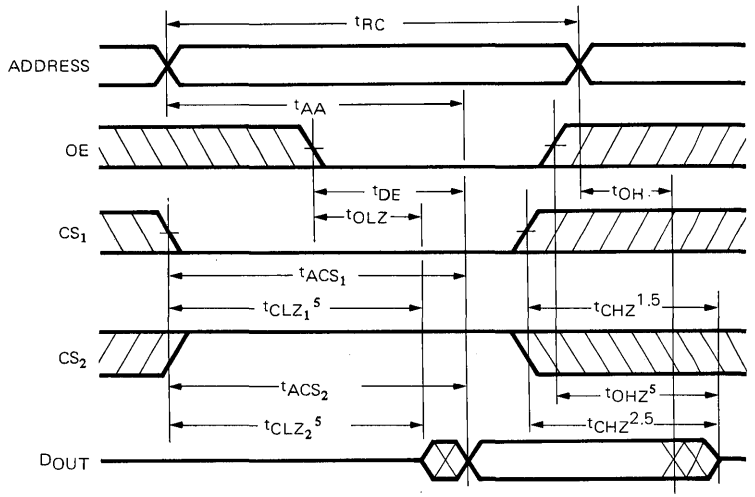
READ CYCLE 2[1, 3, 4, 6]



READ CYCLE 3[1, 4, 7]

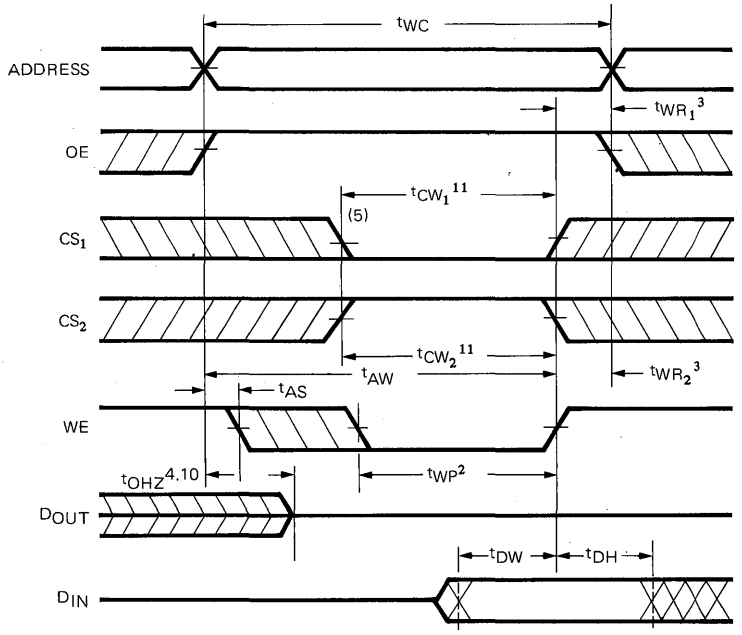


READ CYCLE 4[1]

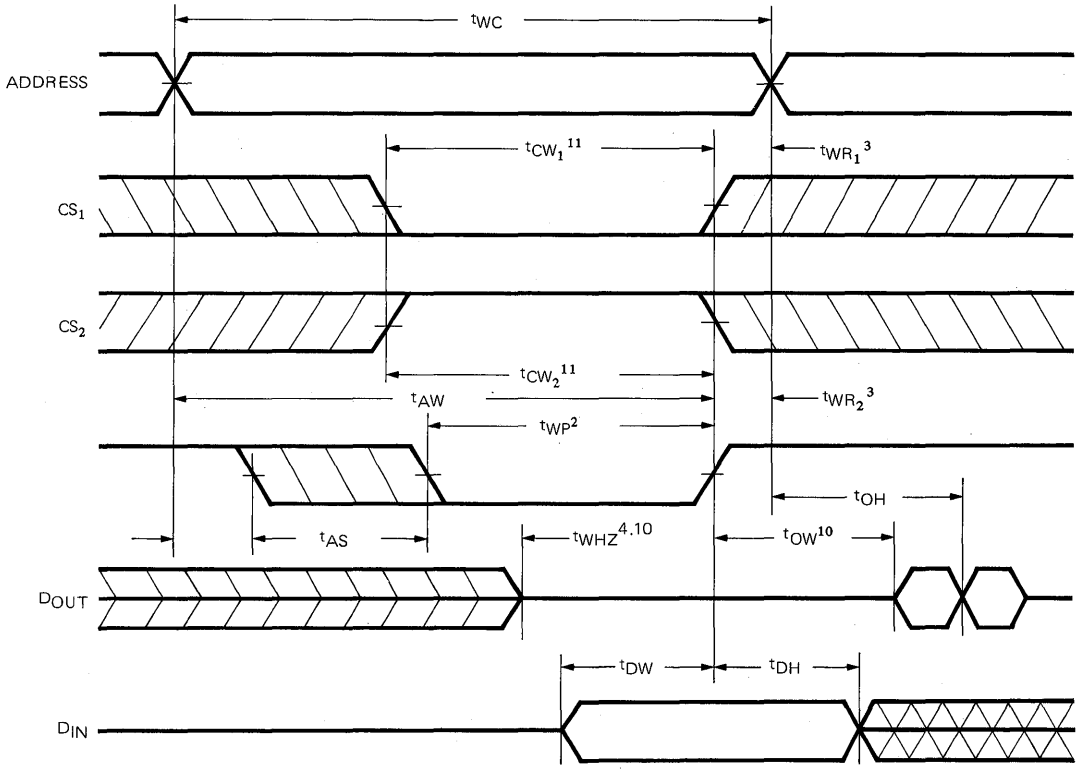


Notes: 1. WE is high for READ cycle.
2. Device is continuously selected $CS_1 = V_{IL}$ and $CS_2 = V_{IH}$.
3. Address valid prior to or coincident with CS_1 transition low.
4. $OE = V_{IL}$.
5. Transition is measured ± 500mV from steady state. This parameter is sampled and not 100% tested.
6. CS_2 is high.
7. CS_1 is low.

WRITE CYCLE 1[1]



WRITE CYCLE 2[1, 6]



Notes:

1. WE must be high during address transitions.
2. A write occurs during the overlap (t_{WP}) of a low CS_1 a high CS_2 and a low WE.
3. t_{WR} is measured from the earlier of CS, or WE going high or CS_2 going low to the end of write cycle.
4. During this period, I/O pins are in the output state SQ that the input signals of opposite phase to the outputs must not be applied.
5. If the CS_1 low transition or the CS_2 high transition occurs simultaneously with the WE low transitions or after the WE transition. Outputs remain in a high impedance state.
6. OE is continuously low (OE = V_{IL}).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If CS_1 is low and CS_2 is high during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ± 500mV from steady state. This parameter is sampled and not 100% tested.
11. t_{CW} is measured from the later of CS_1 going low or CS_2 going high to the end of write.

Data Retention Characteristics

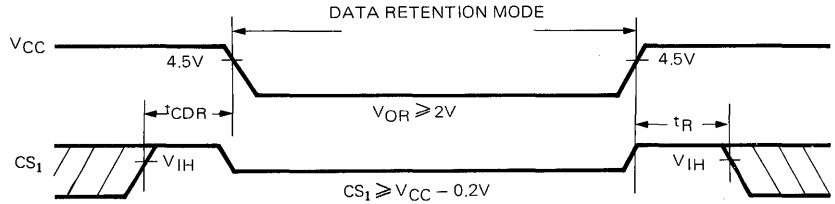
(T_A = 0 to +70°C)

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Units
V_{DR1}	V_{CC} for Data Retention	$CS_1 \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0	–	–	V
V_{DR2}		$CS_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0	–	–	V
I_{CCDR1}	Data Retention Current	$CS_1 \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	–	2	50	μA
I_{CCDR2}		$CS_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	–	2	50	μA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	–	–	ns
t_R	Operation Recovery Time		t_{RC}(2)	–	–	ns

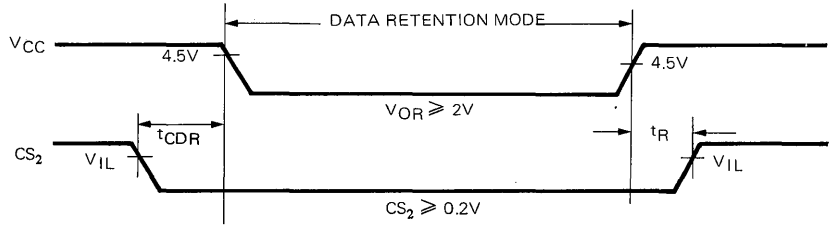
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time

Low V_{CC} Data Retention Waveform

CS_1 CONTROLLED



CS_2 CONTROLLED



Ordering Information

Part Number	Access Time (Max.)	Package
UM6164	70	Plastic DIP
UM6164-1	45	Plastic DIP
UM6164-2	55	Plastic DIP

SRAM

UM6167

16K × 1 High Speed CMOS SRAM

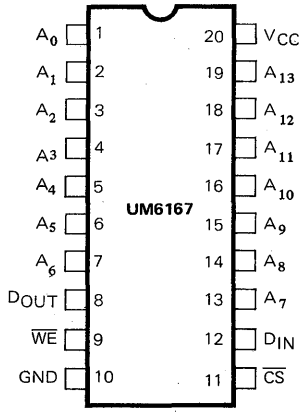
Features

- High-speed – 35/45/55/70 ns
- Low power dissipation
  150mW (Typ.) operating
  100μW (Typ.) stand by
- Single 5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three state outputs
- Data retention supply voltage: 2.0 – 5.5V

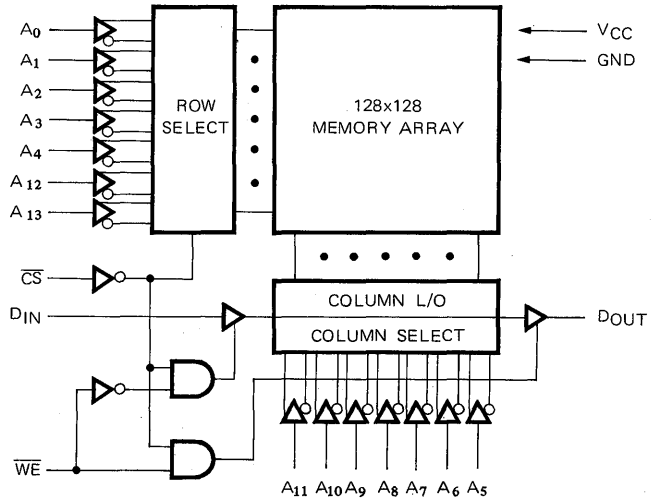
General Description

The UMC UM6167 is a 16,384 bit static random access memory organized as 16,384 words by 1 bit and operates from a single 5 volt supply. It is built with UMC's high performance twin tub CMOS process. Inputs and three-state outputs are TTL compatible. The UM6167 is moulded in a standard 20-pin, 300 mil DIP.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Terminal Voltage with Respect to GND, V_T . . . . . −0.5V to +7.0V
Operating Temperature, T_{OPR} . . . . . 0°C to +70°C
Temperature Under Bias, T_{BLAS} . . . . . −55°C to +125°C
Storage Temperature, T_{STC} . . . . . −65°C to +150°C
Power Dissipation, P_T 1.0W
DC Output Current, I_{OUT} 20mA

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

(T_A = 0°C to +70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Conditions	UM6167			UM6167L			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	–	–	2	–	–	2	μA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	–	–	2	–	–	2	μA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Output Open	–	30	60	–	25	50	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100%	–	30	60	–	25	50	mA
I_{SB}	Standby Power Supply Current	$\overline{CS} \geqslant V_{IH}$	–	5	20	–	5	20	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS} \geqslant V_{CC}$ −0.2V $V_{IN} \geqslant V_{CC}$ −0.2V or $\leqslant$0.2V	–	0.02	2	–	0.002	0.05	mA
V_{IL}	Input Low Voltage		−0.5	–	0.8	−0.5	–	0.8	V
V_{IH}	Input High Voltage		2.2	–	6.0	2.2	–	6.0	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA	–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4mA	2.4	–	–	2.4	–	–	V

Capacitance

(T_A = 25°C, f = 1.0MHz)

Symbol	Item	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	6	pF

Note: This parameter is sampled and not 100% tested.

Truth Table

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	High Z	Active

A.C. Characteristics

(T_A = 0°C to +70°C, V_{CC} = 5V ± 10%)

READ CYCLE

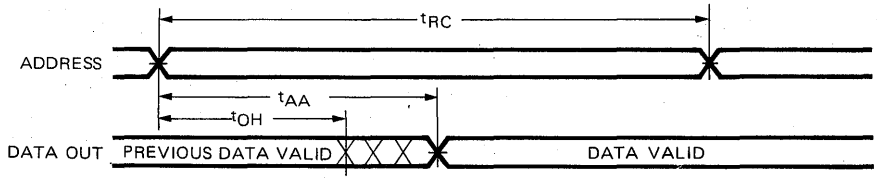
Symbol	Parameter	UM6167		UM6167-1		UM6167-2		UM6167-3		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	70	–	55	–	45	–	35	–	ns
t_{AA}	Address Access Time	–	70	–	55	–	45	–	35	ns
t_{ACE}	Chip Enable Access Time	–	70	–	55	–	45	–	35	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	ns
t_{LZ}	Chip Selection to Output in Low Z	5	–	5	–	5	–	5	–	ns
t_{HZ}	Chip Deselection to Output in High Z	0	35	0	30	0	30	0	25	ns
t_{PU}	Chip Selection to Power Up Time	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselection to Power Down Time	–	40	–	35	–	35	–	25	ns

WRITE CYCLE

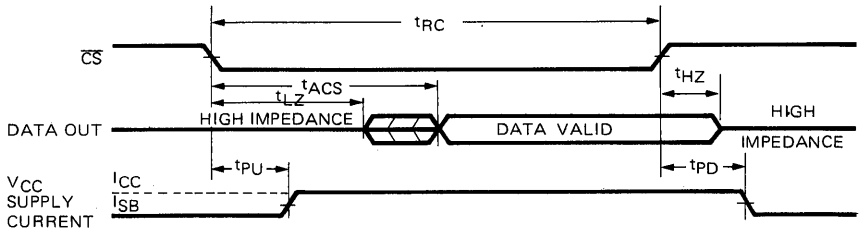
Symbol	Parameter	UM6167		UM6167-1		UM6167-2		UM6167-3		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	70	–	55	–	45	–	35	–	ns
t_{CW}	Chip Enabled to End of Write	55	–	45	–	40	–	35	–	ns
t_{AW}	Address Valid to End of Write	55	–	45	–	40	–	35	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	40	–	35	–	30	–	25	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	ns
t_{DW}	Date Valid to End of Write	25	–	25	–	20	–	17	–	ns
t_{DH}	Data Hold Time	3	–	3	–	3	–	3	–	ns
t_{WZ}	Write Enabled to Output in High Z	0	25	0	25	0	20	0	13	ns
t_{OW}	Output Active from End of Write	0	35	0	35	0	35	0	30	ns

Timing Diagrams

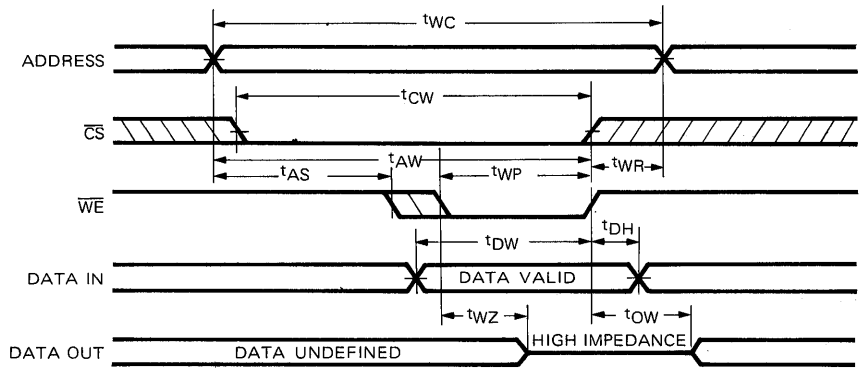
READ CYCLE NO. 1 (NOTES 1 AND 2)



READ CYCLE NO. 2 (NOTES 1 AND 3)

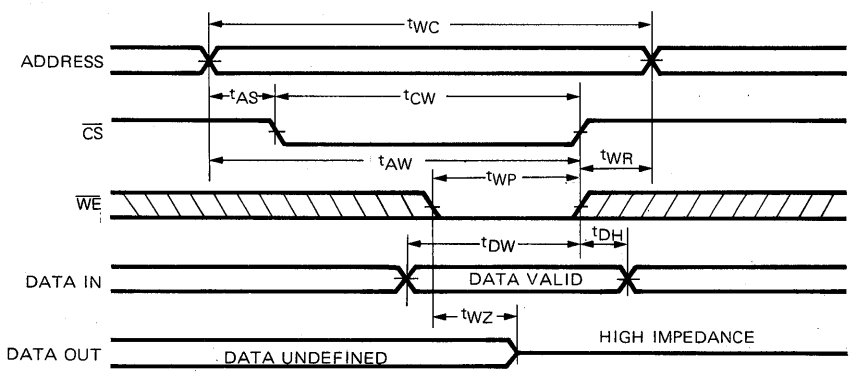


WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) (NOTE 4)



Notes:
1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transition address.
4. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.

WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED) (NOTE 4)



A.C. Test Conditions

Test	Typ.
Input Pulse Levels	GND to 30V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

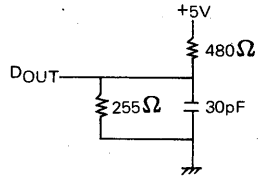


Figure 1. Output Load

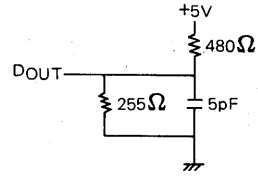


Figure 2. Output Load (for t_{MZ}, t_{LZ}, t_{WZ}, and t_{OW})

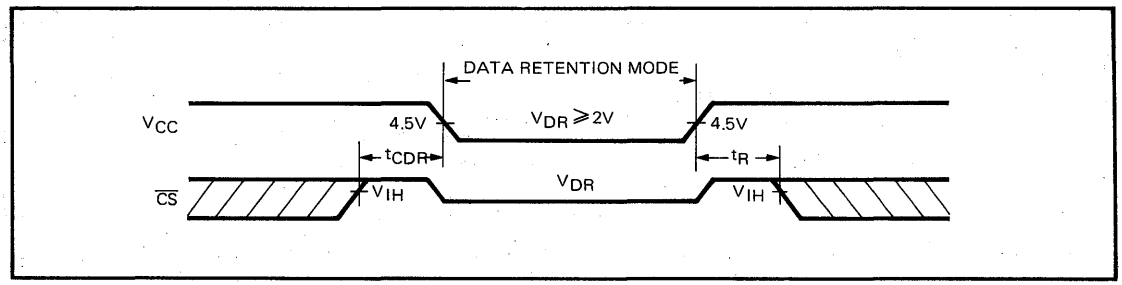
* Including scope and jig.

Low V_{CC} Data Retention Characteristics For L Version Only (T_A = 0 to 70°C)

Symbol	Parameter	Test Conditions	Min.	Typ.[1]	Max.	Units
V_{OR}	V_{CC} for Data Retention	$\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	2.0	–	–	V
I_{CCDA}	Data Retention Current		– –	0.5[2] 1.0[3]	20[2] 30[3]	µA
t_{CDA}	Chip Deselect to Data Retention Time		0	–	–	ns
t_R	Operation Recovery Time		t_{RC}[4]	–	–	ns

Notes: 1. T_A = 25°C, 2. at V_{CC} = 2V, 3. V_{CC} = 3V, 4. t_{RC} = Read Cycle Time

Timing Waveform Low V_{CC} Data Retention Waveform



Ordering Information

Part Number	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)	Package Type
UM6167	70 ns	60 mA	2 mA	Plastic
UM6167-1	55 ns	60 mA	2 mA	Plastic
UM6167-2	45 ns	60 mA	2 mA	Plastic
UM6167-3	35 ns	60 mA	2 mA	Plastic
UM6167L	70 ns	50 mA	50µA	Plastic
UM6167L-1	55 ns	50 mA	50µA	Plastic
UM6167L-2	45 ns	50 mA	50µA	Plastic
UM6167L-3	35 ns	50 mA	50µA	Plastic

UM6168

4K × 4 High Speed CMOS SRAM

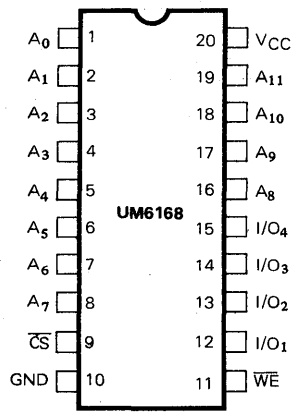
Features

- High-speed – 35/40/45/55/70 ns
- Low power dissipation
  225mW (typ.) operating
  100μW (typ.) standby
- Single 5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three state outputs
- Data retention supply voltage: 2.0 – 5.5V

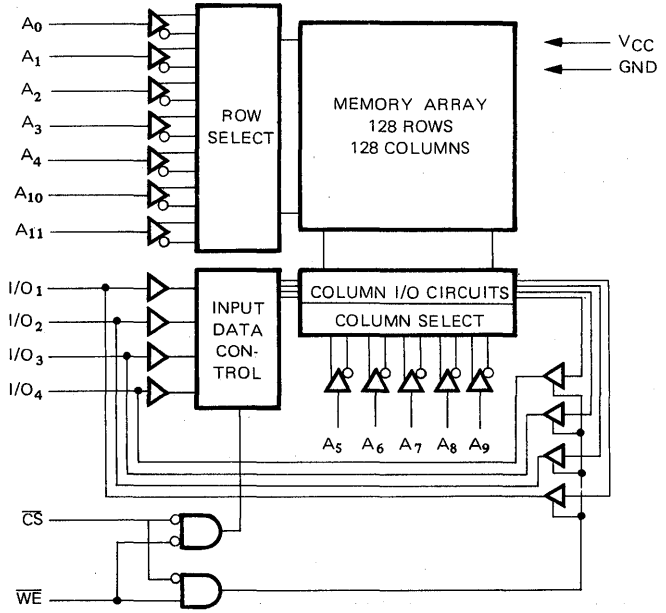
General Description

The UMC UM6168 is a 16,384 bit static random access memory organized as 4096 words by 4 bits and operates from a single 5 volt supply. It is built with UMC's high performance twin tub CMOS process. Inputs and three-state outputs are TTL compatible. The UM6168 is moulded in a standard 20-pin, 300 mil-DIP.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Terminal Voltage with Respect to GND, V_T ..... −0.5V to +7.0V
Operating Temperature, T_{OPR} ..... 0°C to +70°C
Temperature Under Bias, T_{BLAS} ..... −55°C to +125°C
Storage Temperature, T_{STC} ..... −65°C to +150°C
Power Dissipation, P_T 1.0W
DC Output Current, I_{OUT} 20mA

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics

(T_A = 0°C to +70°C, V_{CC} = 5V ±10%)

Symbol	Parameter	Test Conditions	UM6168			UM6168L			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	–	–	2	–	–	2	μA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	–	–	2	–	–	2	μA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Output Open	–	30	60	–	25	50	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100%	–	30	60	–	25	50	mA
I_{SB}	Standby Power Supply Current	$\overline{CS} \geqslant V_{IH}$	–	5	20	–	5	20	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS} \geqslant V_{CC}$ = −0.2V $V_{IN} \geqslant V_{CC}$ = −0.2V or $\leqslant$ 0.2V	–	0.02	2	–	0.002	0.05	mA
V_{IL}	Input Low Voltage		−0.5	–	0.8	−0.5	–	0.8	V
V_{IH}	Input High Voltage		2.2	–	6.0	2.2	–	6.0	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA	–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4mA	2.4	–	–	2.4	–	–	V

Capacitance

(T_A = 25°C, f = 1.0MHz)

Symbol	Item	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	6	pF

Note: This parameter is sampled and not 100% tested.

Truth Table

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	High Z	Active

A.C. Characteristics

(T_A = 0° C to +70° C, V_{CC} = 5V ± 10%)

READ CYCLE

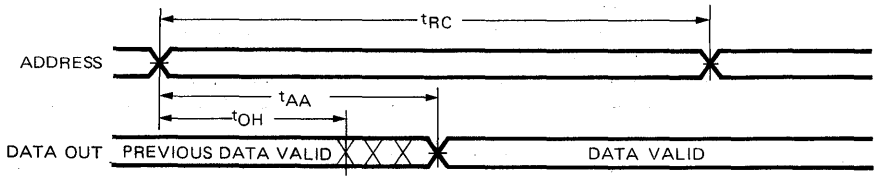
Symbol	Parameter	UM6168		UM6168-1		UM6168-2		UM6168-3		UM6168-4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	70	–	55	–	45	–	40	–	35	–	ns
t_{AA}	Address Access Time	–	70	–	55	–	45	–	40	–	35	ns
t_{ACE}	Chip Enable Access Time	–	70	–	55	–	45	–	40	–	35	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	ns
t_{LZ}	Chip Selection to Output in Low Z	5	–	5	–	5	–	5	–	5	–	ns
t_{HZ}	Chip Deselection to Output in High Z	0	30	–	25	–	20	–	20	–	15	ns
t_{PU}	Chip Selection to Power Up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselection to Power Down Time	–	40	–	35	–	35	–	35	–	25	ns
t_{RCS}	Read Command Set-up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{RCH}	Read Command Hold Time.	0	–	0	–	0	–	0	–	0	–	ns

WRITE CYCLE

Symbol	Parameter	UM6168		UM6168-1		UM6168-2		UM6168-3		UM6168-4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	60	–	50	–	40	–	40	–	35	–	ns
t_{CW}	Chip Enabled to End of Write	60	–	50	–	40	–	40	–	35	–	ns
t_{AW}	Address Valid to End of Write	60	–	50	–	40	–	40	–	35	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	40	–	35	–	30	–	30	–	25	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	ns
t_{DW}	Date Valid to End of Write	25	–	25	–	20	–	20	–	17	–	ns
t_{DH}	Data Hold Time	3	–	3	–	3	–	3	–	3	–	ns
t_{WZ}	Write Enabled to Output in High Z	–	25	–	25	–	20	–	20	–	13	ns
t_{OW}	Output Active from End of Write	–	40	–	35	–	35	–	35	–	30	ns

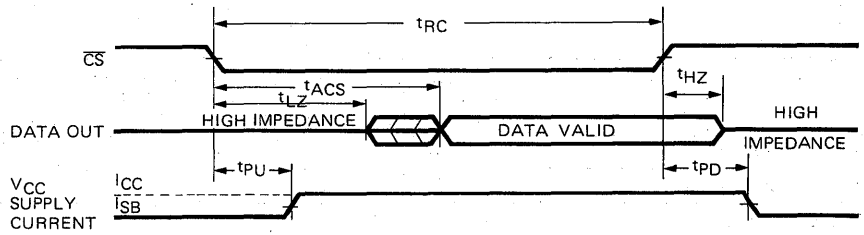
Timing Diagrams

READ CYCLE NO. 1 (NOTES 1 AND 2)

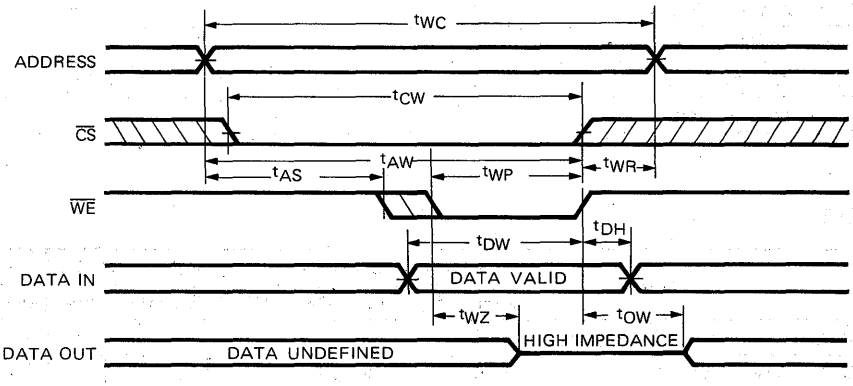


SRAM

READ CYCLE NO. 2 (NOTES 1 AND 3)

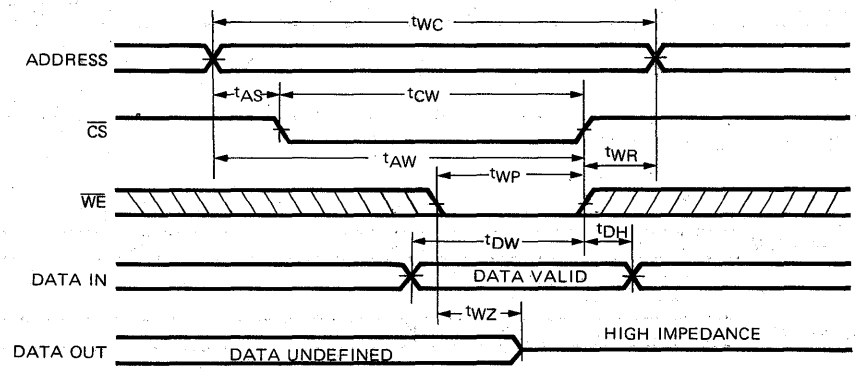


WRITE CYCLE NO. 1 (WE CONTROLLED) (NOTE 4)



Notes:
1. CS or WE must be high during address transitions.
2. If CS goes high simultaneously with WE high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transition address.
4. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.

WRITE CYCLE NO. 2 (CS CONTROLLED) (NOTE 4)



A.C. Test Conditions

Test	Typ.
Input Pulse Levels	GND to 30V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

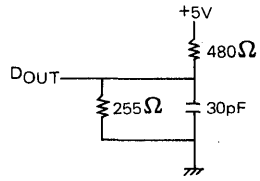


Figure 1. Output Load

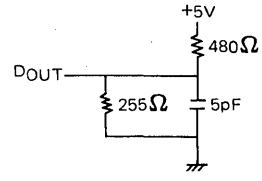


Figure 2. Output Load (for t_{MZ}, t_{LZ}, t_{WZ}, and t_{OW})

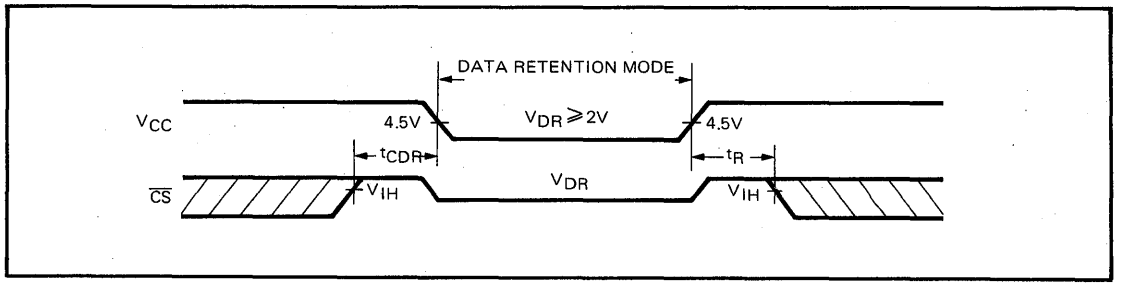
* Including scope and jig.

Low V_{CC} Data Retention Characteristics For L Version Only (T_A = 0 to 70°C)

Symbol	Parameter	Test Conditions	Min.	Typ.[1]	Max.	Units
V_{OR}	V_{CC} for Data Retention		2.0	–	–	V
I_{CCDA}	Data Retention Current	$\overline{CS} \geq V_{CC} - 0.2V$	– –	0.5[2] 1.0[3]	20[2] 30[3]	μA
t_{CDA}	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	0	–	–	ns
t_R	Operation Recovery Time		t_{RC}[4]	–	–	ns

Notes: 1. $T_A = 25°C$, 2. at $V_{CC} = 2V$, 3. $V_{CC} = 3V$, 4. t_{RC} = Read Cycle Time

Timing Waveform Low V_{CC} Data Retention Waveform



Ordering Information

Part Number	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)	Package Type
UM6168	70 ns	90 mA	2 mA	Plastic
UM6168-1	55 ns	90 mA	2 mA	Plastic
UM6168-2	45 ns	90 mA	2 mA	Plastic
UM6168-3	40 ns	90 mA	2 mA	Plastic
UM6168-4	35 ns	90 mA	2 mA	Plastic
UM6168L	70 ns	90 mA	50 μA	Plastic
UM6168L-1	55 ns	90 mA	50 μA	Plastic
UM6168L-2	45 ns	90 mA	50 μA	Plastic
UM6168L-3	40 ns	90 mA	50 μA	Plastic
UM6168L-4	35 ns	90 mA	50 μA	Plastic

Microcontroller

Selection Guide

Part No.	Descriptions	Compatible Devices	Remarks	Page
UM8048/35/ 49/39	8 Bit Single Chip NMOS μC	Intel 8048/35/ 49/39	6, 8, 11 MHz Version	3–3
* UM8051/31	8 Bit Single Chip NMOS μC	Intel 8051/31	–	3–14

* Under Development

UM8048/8035/8049/8039

Single Chip 8-Bit Microcomputer

Features

- 8-Bit CPU, ROM, RAM, I/O in single package
- Single 5V supply
- Up to 1.36 μsec instruction cycle for 11 MHz operation. All instructions 1 or 2 cycles
- Basic machine instructions: 96
  1-byte instructions: 68
  2-byte instructions: 28
- Single level interrupt
- UM8048/8049 is interchangeable with Intel's P8048/8049 in pin configuration and electrical characteristics
- UM8049-2K x 8 ROM 128 x 8 RAM 27 I/O Lines
  UM8048-1K x 8 ROM 64 x 8 RAM 27 I/O Lines
- Internal timer/event counter
- Easily expandable memory and I/O
- Compatible with MCS memory and I/O

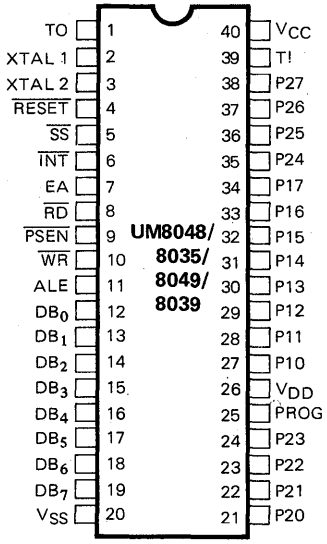
General Description

The UM8048/8035/8049/8039 is a totally self-sufficient 8-bit parallel computer fabricated on a single silicon chip using UMC N-channel silicon gate MOS process.

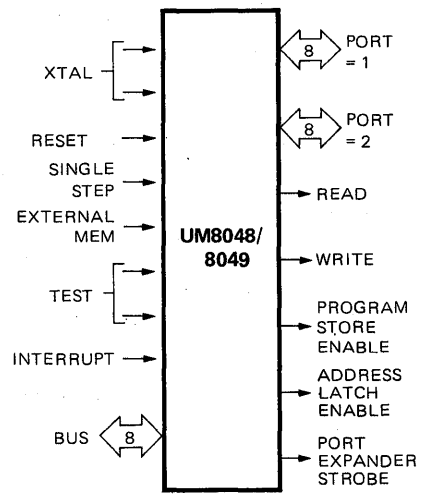
The UM8048 contains a 1K x 8 program memory, a 64 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on-board oscillator and clock circuits. The UM8049 contains a 2K x 8 program memory, a 128 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on board oscillator and clock circuits. For systems that require extra capability, the UM8048/8049 can be expanded using standard memories and MCS-48, MCS-80 and MCS-85 peripherals. The UM8035 is the equivalent of an UM8048 without program memory. The UM8039 is the equivalent to an UM8049 without program memory.

This microprocessor is designed to be an efficient controller as well as an arithmetic processor. The UM8048/8049 has extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and non instructions over two bytes in length.

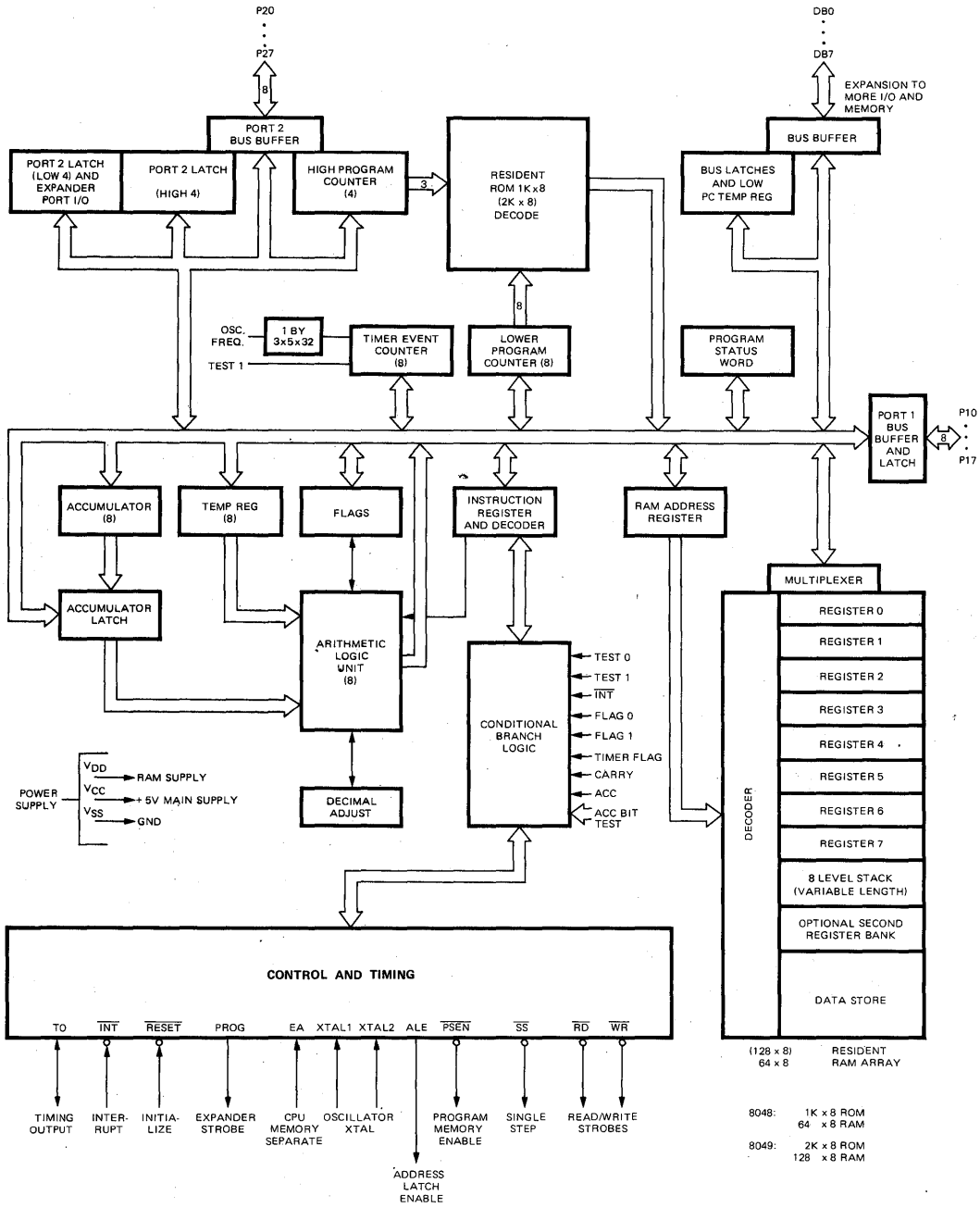
Pin Configuration



Logic Symbol



Block Diagram



Absolute Ratings*

Operating Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to 150°C
Voltage on Any Pin . . . . . −0.5V to +7V
Power Dissipation 1.5W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

(T = 0°C – 70°C V_{CC} = V_{DD} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
Input Low Voltage (All Except XTAL1, XTAL2, $\overline{RESET}$)	V_{IL}	−0.5		0.8	V	
Input High Voltage (All Except XTAL1, XTAL2, $\overline{RESET}$)	V_{IH}	2.0		V_{CC}	V	
Input High Voltage ($\overline{RESET}$, XTAL1, XTAL2)	V_{IH1}	3.8		V_{CC}	V	
Input Low Voltage ($\overline{RESET}$, XTAL1, XTAL2)	V_{IL1}	V_{SS}		0.5	V	
Output Low Voltage (BUS)	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output Low Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OL1}			0.45	V	I_{OL} = 1.8 mA
Output Low Voltage (PROG)	V_{OL2}			0.45	V	I_{OL} = 1.0 mA
Output Low Voltage (All Other Outputs)	V_{OL3}			0.45	V	I_{OL} = 1.6 mA
Output High Voltage (BUS)	V_{OH}	2.4			V	IOH = −400 μA
Output High Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OH1}	2.4			V	I_{OH} = −100 μA
Output High Voltage (All Other Outputs)	V_{OH2}	2.4			V	I_{OH} = −40 μA
Input Leakage Current (T1, $\overline{INT}$)	I_{IL}			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Input Leakage Current (P10-P17, P20-P27, EA, $\overline{SS}$)	I_{IL1}			−500	μA	$V_{CC} \geq V_{IN} \geq V_{SS}$ +0.45V
Input Leakage Current ($\overline{RESET}$)	I_{IL2}	20		−300	=A	$V_{CC} \geq V_{IN} \geq V_{IL1}$
Output Leakage Current (BUS, T0) (High Impedance State)	I_{OL}			±10	μA	$V_{CC} \geq V_{IN} \geq V_{SS}$ +0.45V
Power Down Supply Current	I_{DD}			8	mA	8MHz, 6MHz
				12		11MHz
Total Supply Current	I_{DD} + I_{CC}		35	70	mA	8MHz, 6MHz
			45	100		11MHz

A.C. Characteristics

(T_A = 0°C – 70°C, V_{CC} = V_{DD} = +5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Limits						Units	Test Conditions(1)
		6MHz		8MHz		11MHz			
		Min.	Max.	Min.	Max.	Min.	Max.		
Cycle Time	t_{CY}	2.5	15.0	1.875	15.0	1.36	15.0	μs	
ALE Pulse Width	t_{LL}	410		270		150		ns	
Address Setup Before ALE	t_{AL}	200		140		70		ns	
Address Hold From ALE	t_{LA}	120		85		50		ns	
Control Pulse Width ($\overline{RD}$, $\overline{WR}$)	t_{CC1}	1050		730		480		ns	
Control Pulse Width ($\overline{PSEN}$)	t_{CC2}	800		550		350		ns	
Data Setup Before $\overline{WR}$	t_{DW}	880		610		390		ns	
Data Hold After $\overline{WR}$	t_{WD}	115		75		40		ns	(2)
Data Hold ($\overline{RD}$, $\overline{PSEN}$)	t_{DR}	0	220	0	160	0	110	ns	
$\overline{RD}$ to Data in	t_{RD1}		800		520		330	ns	
$\overline{PSEN}$ to Data in	t_{RD2}		550		330		190	ns	
Address Setup Before $\overline{WR}$	t_{AW}	850		470		300		ns	
Address Setup Before Data in ($\overline{RD}$)	t_{AD1}		1680		1100		730	ns	
Address Setup Before Data in ($\overline{PSEN}$)	t_{AD2}	1250			720		460	ns	
Address Float to $\overline{RD}$, $\overline{WR}$	t_{AFC1}	290		210		140		ns	(2)
Address Float to $\overline{PSEN}$	t_{AFC2}	40		20		10		ns	(2)
Control Pulse ALE ($\overline{RD}$, $\overline{WR}$)	t_{CA1}	120		85		50		ns	
Control Pulse to ALE ($\overline{PSEN}$)	t_{CA2}	620		460		320		ns	
Interrupt Pulse Width	t_{INT}	3		3		3		MC	(3)
Power on Reset Time	t_{RES}	5		5		5		MC	(3)

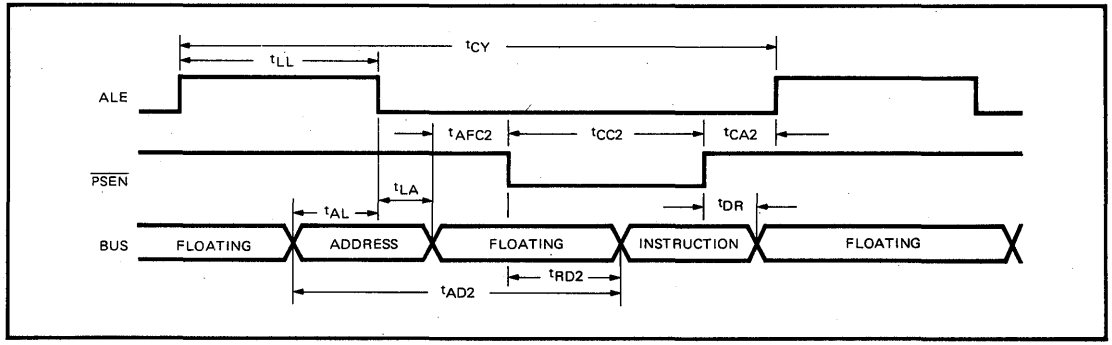
A.C. Characteristics (Continued)

Parameter	Symbol	Limits						Unit	Test Conditions(1)
		6MHz		8MHz		11MHz			
		Min.	Max.	Min.	Max.	Min.	Max.		
Port Control Setup Before Falling Edge of PROG	t_{CP}	200		110		100		ns	
Port Control Hold After Falling Edge of PROG	t_{PC}	460		300		160		ns	
PROG to P2 Input must be Valid	t_{PR}		1300		940		650	ns	
Output Data Setup Time	t_{DP}	850		600		400		ns	
Output Data Hold Time	t_{PD}	200		130		90		ns	
Input Data Hold Time	t_{PF}	0	250	0	190	0	140	ns	
PROG Pulse Width	t_{PP}	1500		1060		700		ns	
Port 2 I/O Data Setup to ALE	t_{PL}	460		300		160		ns	
Port 2 I/O Data Hold to ALE	t_{LP}	150		90		40		ns	
Port Output From ALE	t_{PV}		850		660		510	ns	

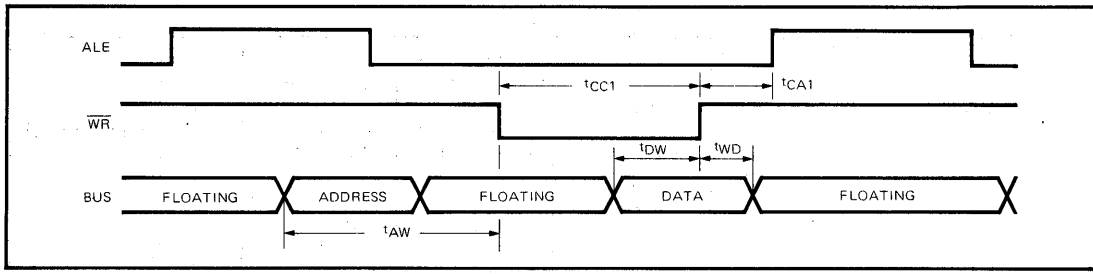
Notes: (1) Control Outputs C_L = 80 pf, Bus Outputs C_L = 150 pf
(2) Bus High Impedance Load 20 pf
(3) MC means machine cycle

Waveforms

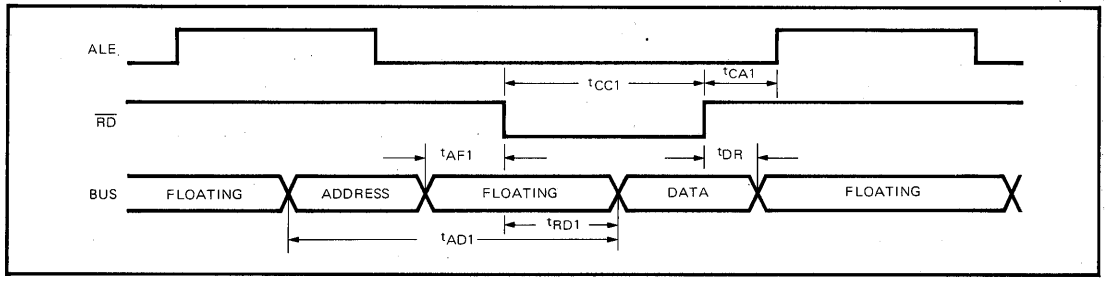
INSTRUCTION FETCH FROM EXTERNAL PROGRAM MEMORY



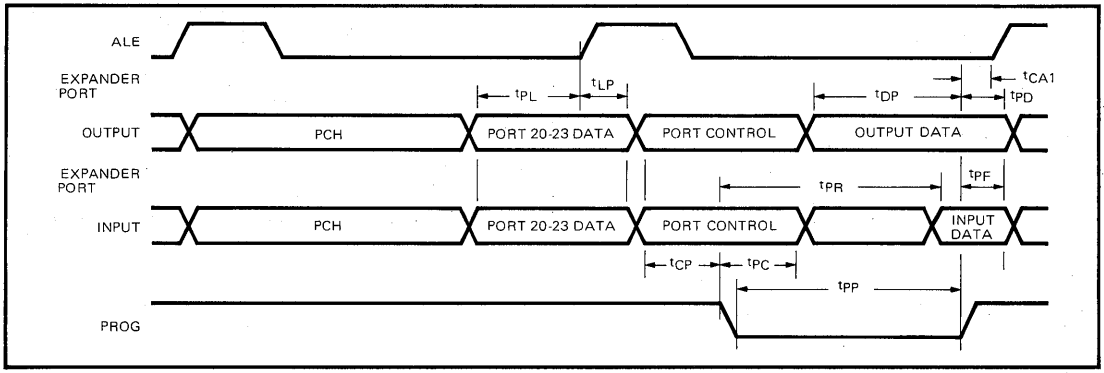
WRITE TO EXTERNAL DATA MEMORY



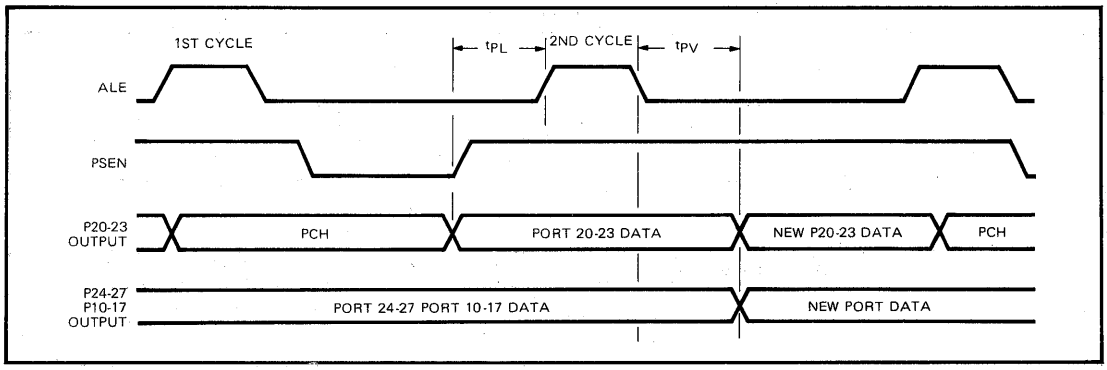
READ FROM EXTERNAL DATA MEMORY



PORT 2 TIMING



I/O PORT TIMING



Pin Description

Designation	Pin	Functions
V_{SS}	20	Circuit GND Potential
V_{DD}	26	+5V during operation. Low power standby pin
V_{CC}	40	Main power supply; +5V during operation
PROG	25	Output strobe for UM8243 I/O expander
Port 1: P10-P17	27-34	8-bit quasi-bidirectional port
Port 2:		
P24-P27	35-38	8-bit quasi-bidirectional port
P20-P23	21-24	P20-P23 contain the four high order program counter bits during an external program fetch and serve as a 4-bit I/O expander bus for UM8243.
BUS: D0-D7	12-19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under control of $\overline{PSEN}$. They also contains the address and data during an external RAM data access instruction under control of ALE, $\overline{RD}$, and $\overline{WR}$.
T0	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as clock output using ENTO CLK instruction.
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
$\overline{INT}$ (Active Low)	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active Low)
$\overline{RD}$ (Active Low)	8	Output strobe activated during a BUS read. Can be used to enable data onto the BUS from an external device. Used as a Read Strobe to External Data Memory.
$\overline{WR}$ (Active Low)	10	Output strobe during a BUS write. Used as write strobe to External Data Memory.
$\overline{RESET}$ (Active Low)	4	Input which is used to initialize the processor. Also used during verification, and power down.
ALE	11	Address Latch Enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.
$\overline{PSEN}$ (Active Low)	9	Program Store Enable. This output occurs only during a fetch to external program memory.
$\overline{SS}$ (Active Low)	5	Single step input can be used in conjuction with ALE to "single step" the processor through each instruction
EA	7	External Access input which forcess all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification
XTAL1	2	One side of crystal input for internal oscillator Also input for external source.
XTAL2	3	Other side of crystal input

Instruction Set

Mnemonic	Functions	Descriptions	Instruction Codes D7	D6	D5	D4	D3	D2	D1	D0	Cycles	Bytes
		Accumulntor										
ADD A, #data	(A)←(A) + data	Add immediate the specified Data to the Accumulator	0 d7	0 d6	0 d5	0 d4	0 d3	0 d2	1 d1	1 d0	2	2
ADD A, Rr	(A)←(A) + (Rr) for r = 0–7	Add contents of designated register to the Accumulator	0	1	1	0	1	r	r	r	1	1
ADD A,@ Rr	(A)←(A) + ((Rr)) for r = 0–1	Add indirect the contents of the data memory location to the Accumulator	0	1	1	0	0	0	0	r	1	1
ADDC A;# data	(A)←(A) + (C) + data	Add immediate with carry the specified data to the Accumulator	0 d7	0 d6	0 d5	1 d4	0 d3	0 d2	1 d1	1 d0	2	2
ADDC A, Rr	(A)←(A) + (C) + (Rr) for r = 0–7	Add with carry the contents of the designated register to the Accumulator	0	1	1	1	1	r	r	r	1	1
ADDC A,@ Rr	(A)←(A) + (C) + ((Rr)) for r = 0–1	Add indirect with carry the contents of data memory location to the Accumulator	0	1	1	1	0	0	0	r	1	1
ANL A, #data	(A)←(A) AND data	Logical AND specified immediate Data with Accumulator	0 d7	1 d6	0 d5	1 d4	0 d3	0 d2	1 d1	1 d0	2	2
ANL A, Rr	(A)←(A) AND (Rr) for r = 0–7	Logical NAD contents of designated register with Accumulator	0	1	0	1	1	r	r	r	1	1
ANL A,@ Rr	(A)←(A) AND ((Rr)) for r = 0–1	Logical AND indirect the contents of data memory with Accumulator	0	1	0	1	0	0	0	r	1	1
CPL A	(A)← NOT (A)	Complement the contents of the Accumulator	0	0	1	1	0	1	1	1	1	1
CLR A	(A)←0	Clear the contents of the Accumulator	0	0	1	0	0	1	1	1	1	1
DA A		Decimal Adjust the contents of the Accumulator	0	1	0	1	0	1	1	1	1	1
DEC A	(A)←(A) – 1	Decrement by 1 the Accumulator's contents	0	0	0	0	0	1	1	1	1	1
INC A	(A)←(A) + 1	Increment by 1 the Accumulator's contents	0	0	0	1	0	1	1	1	1	1
ORL A, #data	(A)←(A) OR data	Logical OR specified immediate data with Accumulator	0 d7	1 d6	0 d5	0 d4	0 d3	0 d2	1 d1	1 d0	2	2
ORL A, Rr	(A)←(A) OR (Rr) fro r = 0–7	Logical OR contents of designated register with Accumulator	0	1	0	0	1	r	r	r	1	1
ORL A,@ Rr	(A)←(A) OR ((Rr)) for r = 0–1	Logical OR indirect the contents of data memory location with Accumulator	0	1	0	0	0	0	0	r	1	1
RL A	(AN+1)←(AN) (A0)←(A7) for N = 0–6	Rotate Accumulator left by 1 bit without carry	1	1	1	0	0	1	1	1	1	1
RLC A	(AN+1)←(AN); N = 0–6, (A0)←(C) (C)←(A7)	Rotate Accumulator left by 1 bit through carry	1	1	1	1	0	1	1	1	1	1
RR A	(AN)←(AN+1); N = 0–6, (A7)←(A0)	Rotate Accumulator right by 1 bit without carry	0	1	1	1	0	1	1	1	1	1
RRC A	(AN)←(AN+1); N = 0–6, (A7)←(C) (C)←(A0)	Rotate Accumulator right by 1 bit through carry	0	1	1	0	0	1	1	1	1	1
SWAP A	(A4–7)⇌(A0–3)	Swap the two 4-bit nibbles in the Accumulator	0	1	0	0	0	1	1	1	1	1
XRL A1, # data	(A)←(A) XOR data	Logic XOR specified immediate data with Accumulator	1 d7	1 d6	0 d5	1 d4	0 d3	0 d2	1 d1	1 d0	2	2
XRL A, Rr	(A)←(A) XOR (Rr) for r = 0–7	Logical XOR contents of designated register with Accumulator	1	1	0	1	1	r	r	r	1	1
XRL A,@ Rr	(A)←(A) XOR ((Rr)) for r = 0–1	Logical XOR indirect the contents of data memory location with Accumulator	1	1	0	1	0	0	0	r	1	1

Instruction Set (Continued)

Mnemonic	Functions	Descriptions	Instruction Codes D7	D6	D5	D4	D3	D2	D1	D0	Cycles	Bytes
		Branch										
DJNZ Rr, addr	(Rr)←(Rr)−1; r=0–7 If (Rr) ≠ 0 (PC0–7)←addr	Decrement the specified register and test contents	1 a7	1 a6	1 a5	0 a4	1 a3	r a2	r a1	r a0	2	2
JBb addr	(PC0–7)←addr if Bb=1 (PC)←(PC)+2 if Bb=0	Jump to specified address if Accumulator bit is set	b2 a7	b1 a6	b0 a5	1 a4	0 a3	0 a2	1 a1	0 a0	2	2
JC addr	(PC0–7)←addr if C=1 (PC)←(PC)+2 if C=0	Jump to sepecified address if carry flag is set	1 a7	1 a6	1 a5	1 a4	0 a3	1 a2	1 a1	0 a0	2	2
JF0 addr	(PC0–7)←addr if P0=1 (PC)←(PC)+2 if F0=0	Jump to specified address if Flag F0 is set	1 a7	0 a6	1 a5	1 a4	0 a3	1 a2	1 a1	0 a0	2	2
JF1 addr	(PC0–7)←addr if F1=1 (PC)←(PC)+2 if F1=0	Jump to specified address if Flag F1 is set	0 a7	1 a6	1 a5	1 a4	0 a3	1 a2	1 a1	0 a0	2	2
JMP addr	(PC8–10)←addr 8–10 (PC0–7)←addr 0–7 (PC11)←DBF	Direct Jump to specified address within the 2K address block	a10 a7	a9 a6	a8 a5	0 a4	0 a3	1 a2	0 a1	0 a0	2	2
JMPP @A	(PC0–7)←((A))	Jump indirect to specified address with address page	1	0	1	1	0	0	1	1	2	1
JNC addr	(PC0–7)←addr if C=0 (PC)←(PC)+2 if C=1	Jump to specified address if carry flag is low	1 a7	1 a6	1 a5	0 a4	0 a3	1 a2	1 a1	0 a0	2	2
JN1 addr	(PC0–7)←addr if I=0 (PC)←(PC)+2 if I=1	Jump to specified address if interrupt is low	1 a7	0 a6	0 a5	0 a4	0 a3	1 a2	1 a1	0 a0	2	2
JNT0 addr	(PC0–7)←addr if T0=0 (PC)←(PC)+2 if T0=1	Jump to specified address if Test 0 is low	0 a7	0 a6	1 a5	0 a4	0 a3	1 a2	1 a1	0 a0	2	2
JNT1 addr	(PC0–7)←addr if T1=0 (PC)←(PC)+2 if T1=1	Jump to specified address if Test 1 is low	0 a7	1 a6	0 a5	0 a4	0 a3	1 a2	1 a1	0 a0	2	2
JNZ addr	(PC0–7)←addr if A≠0 (PC)←(PC)+2 if A=0	Jump to specified address if Accumulator is non-zero	1 a7	0 a6	0 a5	1 a4	0 a3	1 a2	1 a1	0 a0	2	2
JTF addr	(PC0–7)←addr if TF=1 (PC)←(PC)+2 if TF=0	Jump to specified address if Timer Flag is set to 1	0 a7	0 a6	0 a5	1 a4	0 a3	1 a2	1 a1	0 a0	2	2
JT0 addr	(PC0–7)←addr if T0=1 (PC)←(PC)+2 if T0=0	Jump to specified address if Test 0 is a 1	0 a7	0 a6	1 a5	1 a4	0 a3	1 a2	1 a1	0 a0	2	2
JT1 addr	(PC0–7)←addr if T1=1 (PC)←(PC)+2 if T1=0	Jump to specified address if Test 1 is a 1	0 a7	1 a6	0 a5	1 a4	0 a3	1 a2	1 a1	0 a0	2	2
JZ addr	(PC07)←addr if A=0 (PC)←(PC)+2 if A≠0	Jump to specified address if Accumulator is 0	1 a7	1 a6	0 a5	0 a4	0 a3	1 a2	1 a1	0 a0	2	2
		Control										
EN I		Enable the External Interrup input	0	0	0	0	0	1	0	1	1	1
DIS I		Disable the External Interrupt input	0	0	0	1	0	1	0	1	1	1
ENT0 CLK		Enable the Clock Output pin T0	0	1	1	1	0	1	0	1	1	1
SEL MB0	(DBF)←0	Select Bank 0-(locations 0-02047) of program Memory	1	1	1	0	0	1	0	1	1	1
SEL MB1	(DBF)←1	Select Bank 1 (locations 2048-4095) of Program Memory	1	1	1	1	0	1	0	1	1	1
SEL RB0	(BS)←0	Select Bank 0 (locations 0-7) of Data Memory	1	1	0	0	0	1	0	1	1	1
SEL RB1	(BS)←1	Select Bank 1 (locations 24-31) of Data Memory	1	1	0	1	0	1	0	1	1	1
		Data Moves										
MOV A, #data	(A)←data	Move immediate the specified data into the Accumulator	0 d7	0 d6	1 d5	0 d4	0 d3	0 d2	1 d1	1 d0	2	2
MOV A, Rr	(A)←(Rr); r=0–7	Move the contents of the designated registers into the Accumulator	1	1	1	1	1	r	r	r	1	1

Instruction Set (Continued)

Mnemonic	Functions	Descriptions	Instruction Codes D7	D6	D5	D4	D3	D2	D1	D0	Cycles	Bytes
		Data Moves (Cont.)										
MOV A, @ Rr	(A) ← ((Rr)); r=0–1	Move indirect the contents data memory location into the Accumulator	1	1	1	1	0	0	0	r	1	1
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator	1	1	0	0	0	1	1	1	1	1
MOV Rr, # data	(Rr) ← data; r=0–7	Move immediate the spocified data into the designated register	1 d7	0 d6	1 d5	1 d4	1 d3	r d2	r d1	r d0	2	2
MOV Rr, A	(Rr) ← (A); r=0–7	Move Accumulator Contents into the designated register	1	0	1	0	1	r	r	r	1	1
MOV @ Rr, A	((Rr)) ← (A), r=0–1	Move indirect Accumulator Contents into data memory location	1	0	1	0	0	0	0	r	1	1
MOV @ Rr, # data	((Rr)) ← data; r=0–1	Move immediate the specified data into data memory	1 d7	0 d6	1 d5	1 d4	0 d3	0 d2	0 d1	r d0	2	2
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the program status word	1	1	0	1	0	1	1	1	1	1
MOVP A, @ A	(PC0–7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator	1	0	1	0	0	0	1	1	2	1
MOVP3 A, @ A	(PC0–7) ← (A) (PC8–10) ← 011 (A) ← ((PC))	Move Program data in Page 3 into the Accumulator	1	1	1	0	0	0	1	1	2	1
MOVX A, @ R	(A) ← ((Rr)); r=0–1	Move indirect the contents of external data memory into the Accumulator	1	0	0	0	0	0	0	r	2	1
MOVX @ R, A	((Rr)) ← (A), r=0–1	Move indirect the contents of the Accumulator into external data memory	1	0	0	1	0	0	0	r	2	1
XCH A, Rr	(A) ⇌ (Rr); r=0–7	Exchange the Accumulator and designated register's contents	0	0	1	0	1	r	r	r	1	1
XCH A, @ Rr	(A) ← ((Rr)); r=0–1	Exchange indirect contents of Accumulator and location in data memory	0	0	1	0	0	0	0	r	1	1
XCHD A, @ Rr	(A0–3) ⇌ ((Rr0–3)); r=0–1	Exchange indirect 4 bit contents of Accumulator and data memory	0	0	1	1	0	0	0	r	1	1
		Flags										
CPL C	(C) ← NOT (C)	Complement carry bit	1	0	1	0	0	1	1	1	1	1
CPL F0	(F0) ← NOT (F0)	Complement Flag F0	1	0	0	1	0	1	0	1	1	1
CPL F1	(F1) ← NOT (F1)	Complement Flag F1	1	0	1	1	0	1	0	1	1	1
CLR C	(C) ← 0	Clear carry bit to 0	1	0	0	1	0	1	1	1	1	1
CLR F0	(F0) ← 0	Clear Flag 0 to 0	1	0	0	0	0	1	0	1	1	1
CLR F1	(F1) ← 0	Clear Flag 1 to 0	1	0	1	0	0	1	0	1	1	1
		Input/Output										
ANL BUS, #. data	(BUS) ← (BUS) AND data	Logical AND immediate specified data with contents of Bus	1 d7	0 d6	0 d5	1 d4	1 d3	0 d2	0 d1	0 d0	2	2
ANL Pp, # data	(Pp) ← (Pp) AND data p=1–2	Logical AND immediate specified data with designated port (1 or 2)	1 d7	0 d6	0 d5	1 d4	1 d3	0 d2	p d1	p d0	2	2
ANLD Pp, A	(Pp) ← (Pp) AND (A0–3) p=4–7	Logical AND contents of Accumulator with designated port (4–7)	1	0	0	1	1	1	p	p	2	1
IN A, Pp	(A) ← (Pp), p=1–2	Input data from designated port (1–2) into Accumulator	0	0	0	0	1	0	p	p	2	1
INS A, BUS	(A) ← (BUS)	Input strobed Bus data into Accumulator	0	0	0	0	1	0	0	0	2	1
MOVD A, Pp	(A0–3) ← (Pp); p=4–7 (A1–7) ← 0	Move contents of designated port (4–7) into Accumulator	0	0	0	0	1	1	p	p	2	1
MOVD Pp, A	(Pp) ← A0–3; p=4–7	Move contents of Accumulator into designated port (4–7)	0	1	1	1	1	p	p	1	2	1

Instruction Set (Continued)

Mnemonic	Functions	Descriptions	Instruction Codes D7	D6	D5	D4	D3	D2	D1	D0	Cycles	Bytes
		Input/Output (Cont.)										
ORL BUS, # data	(BUS) ← (BUS) OR data	Logical OR immediate specified data with contents of Bus	1 d7	0 d6	0 d5	0 d4	1 d3	0 d2	0 d1	0 d0	2	2
ORLD Pp, A	(Pp) ← (Pp) OR (A0–3) p=4–7	Logical OR contents of Accumulator with designated port (4–7)	1	0	0	0	1	1	p	p	2	1
ORL Pp, # data	(Pp) ← (Pp) OR data p=1–2	Logical OR immediate specified data with designated port (1–2)	1 d7	0 d6	0 d5	0 d4	1 d3	0 d2	p d1	p d0	2	2
OUTL BUS, A	(BUS) ← (A)	Output contents of Accumulator onto Bus	0	0	0	0	0	0	1	0	2	1
OUTL Pp, A	(Pp) ← (A); p=1–2	Output contents of Accumulator to designated port (1–2)	0	0	1	1	1	0	p	p	2	1
		Register										
DEC Rr	(Rr) ← (Rr) – 1; r=0–7	Decrement by 1 contents of designated register	1	1	0	0	1	r	r	r	1	1
INC Rr	(Rr) ← (Rr) + 1; r=0–7	Increment by 1 conents of designated register	0	0	0	1	1	r	r	r	1	1
INC @ R	((Rr)) ← ((Rr)) + 1; r=0–1	Increment indirect by 1 the contents of data memory location	0	0	0	1	0	0	0	r	1	1
		Subroutine										
Call addr	((SP)) ← (PC), (PSW4–7) (SP) ← (SP) + 1 (PC8–10) ← addr 8–10 (PC0–7) ← addr 0–7 (PC11) ← DBF	Call designated Subroutine	a10 a7	a9 a6	a8 a5	1 a4	0 a3	1 a2	0 a1	0 a0	2	2
RET	(SP) ← (SP) – 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word	1	0	0	0	0	0	1	1	2	1
RETR	(SP) ← (SP) – 1 (PC) ← ((SP)) (PSW4–7) ← ((SP))	Return from Subroutine restoring Program Status Word	1	0	0	1	0	0	1	1	2	1
		Timer/Counter										
EN TCNTI		Enable Internal interrupt Flag for Timer/Counter output	0	0	1	0	0	1	0	1	1	1
DIS TCNTI		Disable Internal interrupt Flag for Timer/Counter output	0	0	1	1	0	1	0	1	1	1
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator	0	1	0	0	0	0	1	0	1	1
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter	0	1	1	0	0	0	1	0	1	1
STOP TCNT		Stop Count for Event Counter	0	1	1	0	0	1	0	1	1	1
STRT CNT		Start Count for Event Counter	0	1	0	0	0	1	0	1	1	1
STRT T		Start Counter foe Timer	0	1	0	1	0	1	0	1	1	1
		Miscellaneous										
NOP		No Operation performed	0	0	0	0	0	0	0	0	1	1

Notes: 1. Instruction Code Designations r and p form the binary representation of the Registers and Ports involved.
2. References to the address and data are specified in bytes 2 and/or 1 of the instruction.
3. Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected.

Ordering Information

Part Number	Max. Freq.
UM8035-6	6 MHz
UM8039-6	
UM8035-8	8 MHz
UM8039-8	
UM8035-11	11 MHz
UM8039-11	

UM8051 / UM8031

Single Chip 8-Bit Microcomputer

Features

- 4K x 8 ROM
- 128 x 8 RAM
- Four 8-bit ports, 32 I/O lines
- Two 16-bit timer/event counters
- High-performance full-duplex serial channel
- External memory expandable to 128K
- Boolean processor
- UM8048 architecture enhanced with:
  - Non-paged jumps
  - Direct addressing
  - Four 8-register banks
  - Stack depth up to 128-bytes
  - Multiply, divide, subtract, compare
- Most instructions execute in 1μs
- 4μs multiply and divide

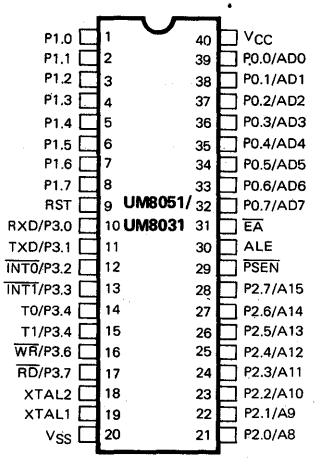
General Description

The UM8051/8031 is a stand-alone, high-performance single-chip computer fabricated with UMC's highly-reliable +5 Volt, NMOS technology and packaged in a 40-pin DIP. It provides the hardware features, architectural enhancements and new instructions that are necessary to make it a powerful and cost effective controller for applications requiring up to 64K bytes of program memory and/or up to 64K bytes of data storage.

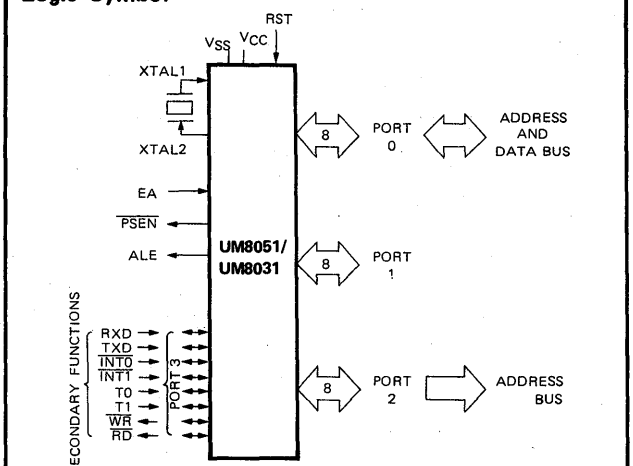
The UM8051/8031 contains a non-volatile 4K x 8 read-only program memory, a volatile 128 x 8 read/write data memory; 32 I/O lines; two 16-bit timer/counters; a five-source, two-priority-level, nested interrupt structure; a serial I/O port for either multi-processor communications, I/O expansion, or full duplex UART; and on-chip oscillator and clock circuits. The UM8031 is identical, except that it lacks the program memory. For systems that require extra capability, the UM8051 can be expanded using standard TTL compatible memories.

The UM8051 microcomputer, like its UM8048 predecessor, is efficient both as a controller and as an arithmetic processor. The UM8051 has extensive facilities for binary and BCD arithmetic and excels in bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 12 MHz crystal, 58% of the instructions execute in 1μs, 40% in 2μs and multiply and divide require only 4μs. Among the many instructions added to the standard UM8048 instruction set are multiply, divide, subtract and compare.

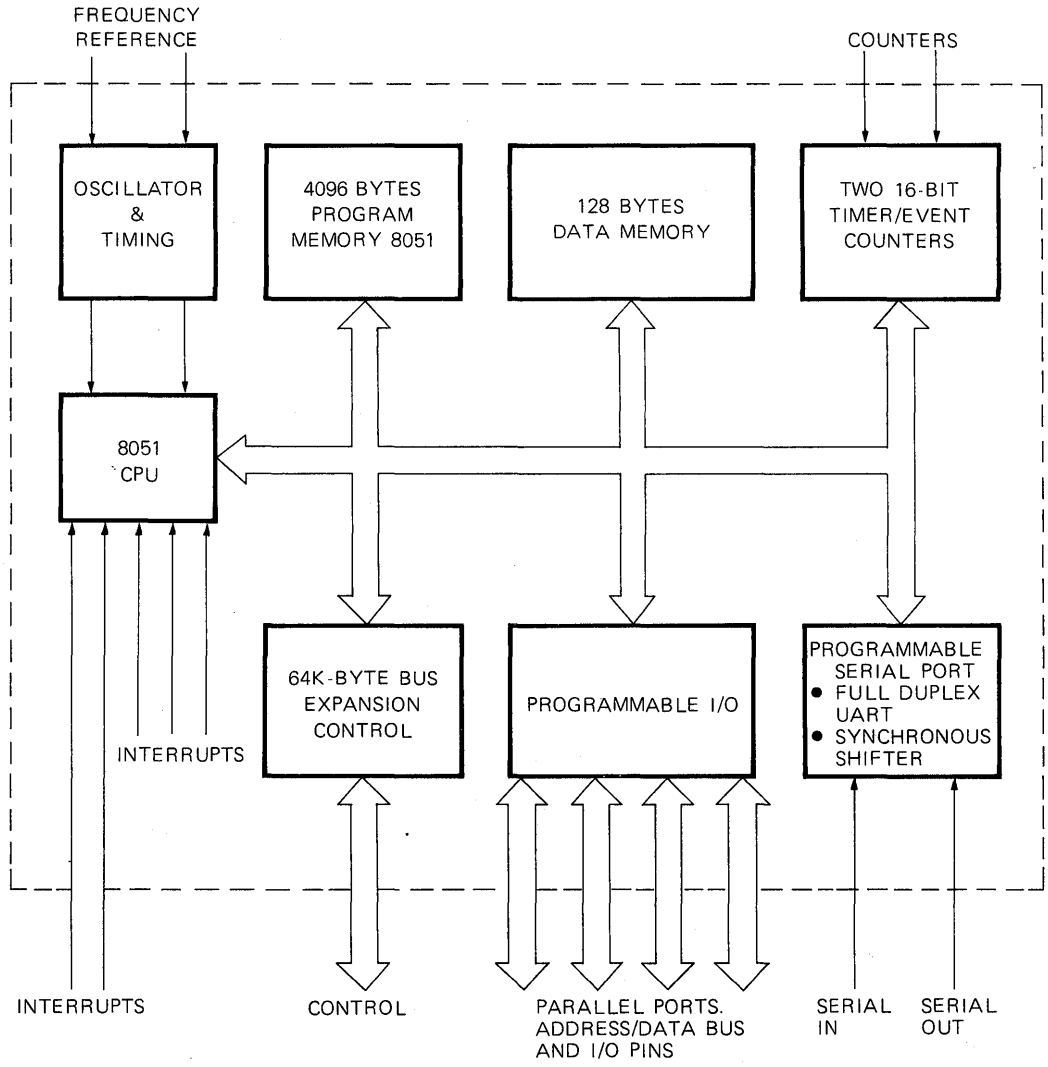
Pin Configuration



Logic Symbol



Block Diagram



Pin Description

Designation	Pin	Functions
V_{SS}	20	Circuit ground potential.
V_{CC}	40	+5V power supply during operation and program verification.
Port 0	32-39	Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data input and output during programming and verification. Port 0 can sink/source eight TTL loads.
Port 1	1-8	Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. Port 1 can sink/source four TTL load.
Port 2	21-28	Port 2 is an 8-bit bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source four TTL load.
Port 3	10-17	Port 3 is an 8-bit quasi-bidirectional I/O port with internal pullups. It also contains the interrupt, timer, serial port and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source four TTL load. The secondary function are assigned to the pins of Port 3, as follows: –RXD/data (P3.0). Serial port's receiver data input (asynchronous). –TXD/clock (P3.1). Serial port's transmitter data output (asynchronous). –$\overline{INT0}$ (P3.2). Interrupt 0 input. –$\overline{INT1}$ (P3.3). Interrupt 1 input. –T0 (P3.4). Input to counter 0. –T1 (P3.5). Input to counter 1. –$\overline{WR}$ (P3.6). The write control signal latches the data byte from Port 0 into the External Data Memory. –$\overline{RD}$ (P3.7). The read control signal enables External Data Memory to Port 0.
RST	9	A high on this pin for two machine cycles while the oscillator is running resets the device. A small external pulldown resistor ($\approx 8.2k\Omega$) from RST to V_{SS} permits power-on reset when a capacitor ($\approx 10\,\mu f$) is also connected from this pin to V_{CC}.
ALE	30	Address Latch Enable output for latching the low byte of the address during accesses to external memory. ALE is activated at a constant rate of 1/6 the oscillator frequency except during an external data memory access at which time one ALE pulse is skipped. ALE can sink/source 8 LS TTL inputs.
$\overline{PSEN}$	29	The Program Store Enable output is a control signal that enables the external Program Memory to the bus during external fetch operations. It is activated every six oscillator periods except during external data memory access. $\overline{PSEN}$ remains high during internal program execution.
$\overline{EA}$	31	When held at a TTL high level, the 8051 executes instructions from the internal ROM when the PC is less than 4096. When held at a TTL low level, the 8031/8051 fetches all instructions from external Program Memory. Do not float $\overline{EA}$ during normal operation.
XTAL1	19	Input to the inverting amplifier that forms part of the oscillator. This pin should be connected to ground when an external oscillator is used.
XTAL2	18	Output of the inverting amplifier that forms part of the oscillator, and input to the internal clock generator. XTAL2 receives the oscillator signal when an external oscillator is used.

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . 0°C to 70°C

Storage Temperature . . . . . −65°C to +150°C

Voltage on Any Pin With Respect to

Ground (V_{SS}) . . . . . −0.5V to +7V

Power Dissipation . . . . . 1 Watts

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. Characteristics

(T_A = 0°C to 70°C; V_{CC} = 5V ± 10%; V_{SS} = 0V)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
VIL	Input Low Voltage	−0.5	0.8	V	
VIH	Input High Voltage (Except RST and XTAL2)	2.0	V_{CC} + 0.5	V	
VIH1	Input High Voltage to RST For Reset. XTAL2	2.5	V_{CC} + 0.5	V	XTAL1 to V_{SS}
VOL	Output Low Voltage Ports 1, 2, 3 (Note 1)		0.45	V	IOL = 1.6mA
VOL1	Output Low Voltage Port 0, ALE, $\overline{PSEN}$ (Note 1)		0.45	V	IOL = 3.2mA
VOH	Output High Voltage Ports 1, 2, 3	2.4		V	IOH = −80μA
VOH1	Output High Voltage Port 0, ALE, $\overline{PSEN}$	2.4		V	IOH = −400μA
IIL	Logical 0 Input Current Ports 1, 2, 3		−800	μA	Vin = 0.45V
IIL2	Logical 0 Input Current for XTAL2		−2.5	mA	XTAL1 = V_{SS}, Vin = 0.45V
ILI	Input Leakage Current To Port 0, $\overline{EA}$		±10	μA	0.45V < Vin < V_{CC}
IIH1	Input High Current to RST/V_{PD} For Reset		500	μA	Vin < V_{CC} − 1.5V
ICC	Power Supply Current		125	mA	All outputs disconnected
CIO	Capacitance of I/O Buffer		10	pF	f_C = 1 MHz, T_A = 25°C

Note: VOL is degraded when the 8031/8051 rapidly discharges external capacitance. This AC noise is most pronounced during emission of address data. When using external memory, locate the latch or buffer as close to the 8031/8051 as possible.

A.C. Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, C_L for Port 0, ALE and PSEN Outputs = 100 pF; C_L for all other outputs = 80 pF)

EXTERNAL PROGRAM MEMORY CHARACTERISTICS

Symbol	Parameter	12 MHz 1Clock			Variable Clock 1/TCLCL = 3.5 MHz to 12 MHz		
		Min.	Max.	Units	Min.	Max.	Units
TLHLL	ALE Pulse Width	127		ns	2TCLCL-40		ns
TAVLL	Address Setup to ALE	43		ns	TCLCL-40		ns
TLLAX	Address Hold After ALE	48		ns	TCLCL-35		ns
TLLIV	ALE to Valid Instr In		233	ns		4TCLCL-100	ns
TLLPL	ALE To $\overline{PSEN}$	58		ns	TCLCL-25		ns
TPLPH	$\overline{PSEN}$ Pulse Width	215		ns	3TCLCL-35		ns
TPLIV	$\overline{PSEN}$ To Valid Instr In		125	ns		3TCLCL-125	ns
TPXIX	Input Instr Hold After $\overline{PSEN}$	0		ns	0		ns
TPXIZ	Input Instr Float After $\overline{PSEN}$		63	ns		TCLCL-20	ns
TPXAV	Address Valid After $\overline{PSEN}$	75		ns	TCLCL-8		ns
TAVIV	Address To Valid Instr In		302	ns		5TCLCL-115	ns
TAZPL	Address Float To $\overline{PSEN}$	0		ns	0		ns

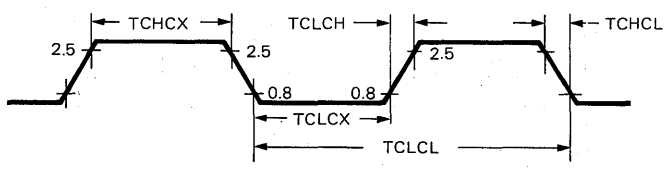
EXTERNAL DATA MEMORY CHARACTERISTICS

Symbol	Parameter	12 MHz Clock			Variable Clock 1/TCLCL = 3.5 MHz to 12 MHz		
		Min.	Max.	Unit	Min.	Max.	Unit
TRLRH	$\overline{RD}$ Pulse Width	400		ns	6TCLCL-100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		ns	6TCLCL-100		ns
TLLAX	Address Hold After ALE	48		ns	TCLCL-35		
TRLDV	$\overline{RD}$ To Valid Data In		250	ns		5TCLCL-165	ns
TRHDX	Data Hold After $\overline{RD}$	0		ns	0		ns
TRHDZ	Data Float After $\overline{RD}$		97	ns		2TCLCL-70	ns
TLLDV	ALE To Valid Data In		517	ns		8TCLCL-150	ns
TAVDV	Address To Valid Data In		585	ns		9TCLCL-165	ns
TLLWL	ALE To $\overline{WR}$ or $\overline{RD}$	200	300	ns	3TCLCL-50	3TCLCL + 50	ns
TAVWL	Address To $\overline{WR}$ or $\overline{RD}$	203		ns	4TCLCL-130		ns
TWHLH	$\overline{WR}$ or $\overline{RD}$ High To ALE High	43	123	ns	TCLCL-40	TCLCL + 40	ns
TDVWX	Data Valid To $\overline{WR}$ Transition	23		ns	TCLCL-60		ns
TQVWH	Data Setup Before $\overline{WR}$	433		ns	7TCLCL-150		ns
TWHQX	Data Hold After $\overline{WR}$	33		ns	TCLCL-50		ns
TRLAZ	Address Float After $\overline{RD}$		0	ns		0	ns

Datum	Emitting Ports	Degraded I/O Lines	VOL (peak) (Max.)
Address	P2, P0	P1, P3	0.8V
Write Data	P0	P1, P3, ALE	0.8V

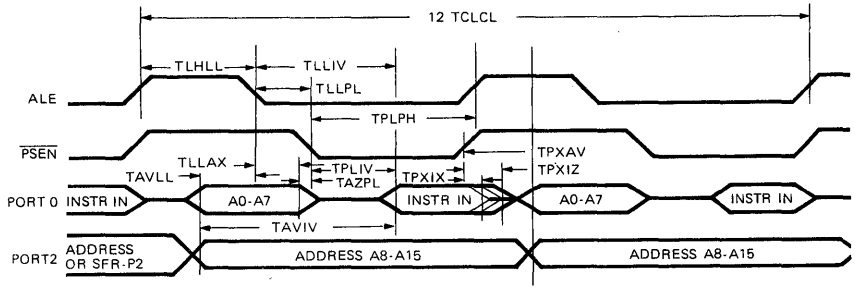
EXTERNAL CLOCK DRIVE CHARACTERISTICS (XTAL2)

Symbol	Parameter	Variable Clock freq = 3.5 MHz to 12 MHz		Unit
		Min.	Max.	
TCLCL	Oscillator Period	83.3	286	ns
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

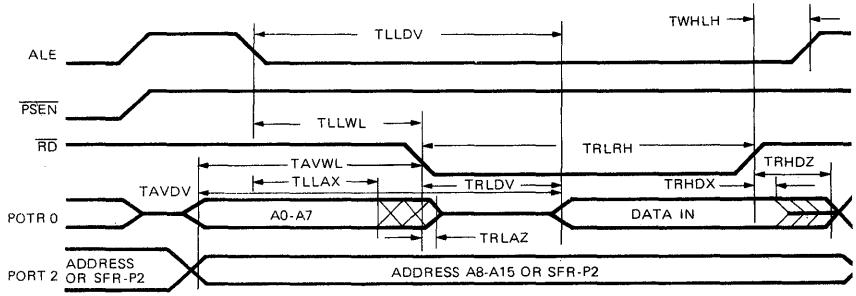


A.C. Timing Diagrams

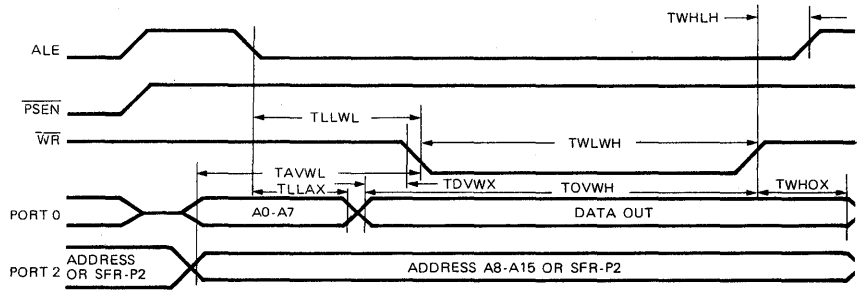
EXTERNAL PROGRAM MEMORY READ CYCLE



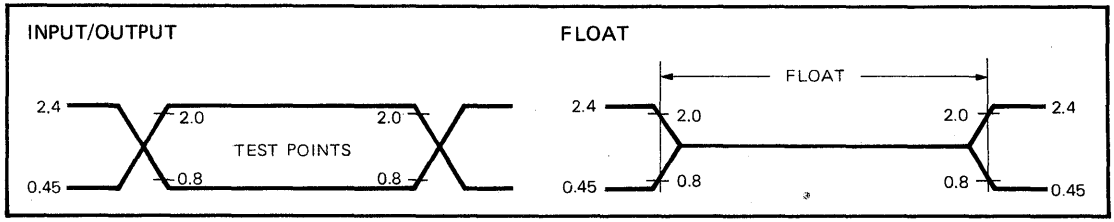
EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE

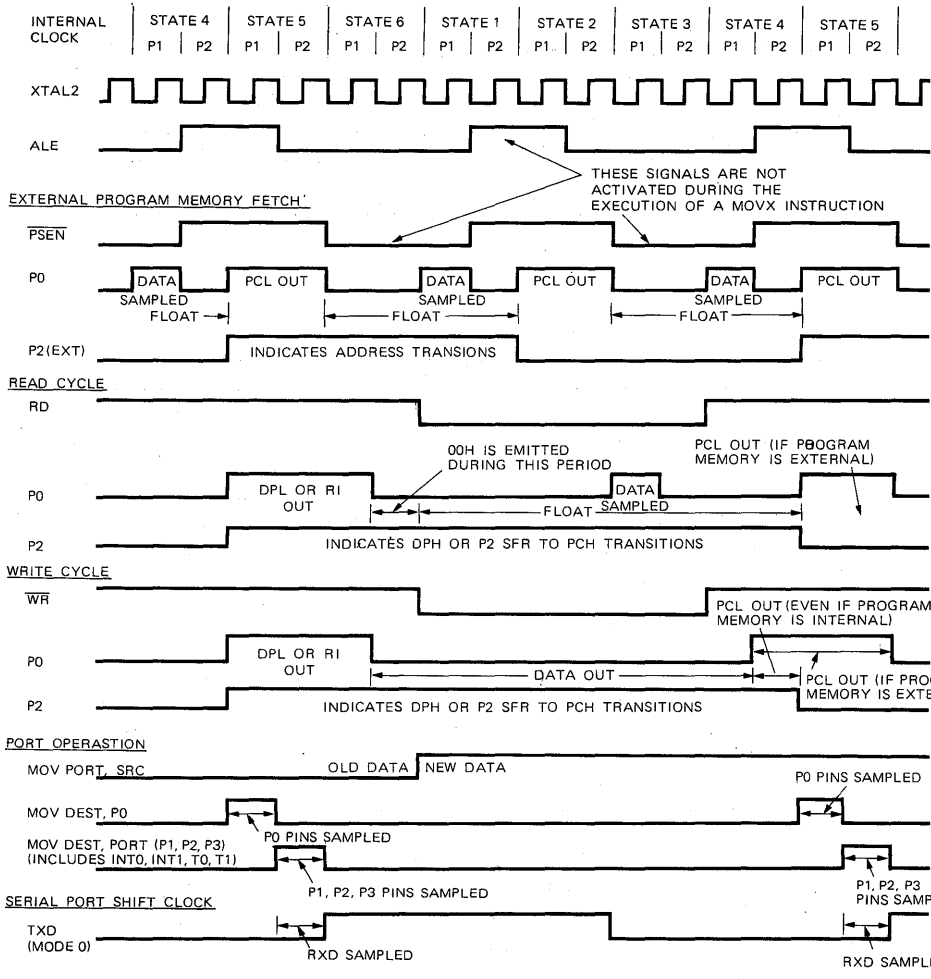


A.C. Testing Input/Output, Float Waveforms



AC inputs during testing are driven at 2.4V for a logic "1" and 0.45V for logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic."0". For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2mA or sources 400 μA at the voltage test levels.

Clock Waveforms



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 15 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component to component. Typically though, (T_A = 25°C, fully loaded) RD and WR propagation delays are approximately 50 ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

UM8051 Instruction Set Summary

INTERRUPT RESPONSE TIME

To finish execution of current instruction, respond to the interrupt request, push the PC and to vector to the first instruction of the interrupt service program requires 38 to 81 oscillator periods (3 to 7μs @ 12 MHz).

INSTRUCTIONS THAT AFFECT FLAG SETTINGS*

Instruction	Flag		
	C	OV	AC
Add	X	X	X
ADDC	X	X	X
SUBB	X	X	X
MUL	O	X	
DIV	O	X	
DA	X		
RRC	X		
RLC	X		
SETB C	1		
CLR C	O		
CPL C	X		
ANL C, bit	X		
ORL C, bit	X		
ORL C, bit	X		
MOV C, bit	X		
CJNE	X		

* Note that operations on SFR byte address 208 or bit addresses 209–215 (i.e., the PSW or bits in the PSW) will also affect flag settings.

Notes on instruction set and addressing modes:

Rn

Register R7 – R0 of the currently selected Register Bank.

Data

8-bit internal data location's address. This could be an Internal Data RAM location (0 – 127) or a SFR [i.e., I/O port, control register, status register, etc. (128 – 255)].

@ Ri

8-bit internal data RAM location (0 – 255) addressed indirectly through register R1 or R0.

#data

8-bit constant included in instruction.

#data 16

16-bit constant included in instruction.

Addr. 16

16-bit destination address. Used by LCALL & LJMP. A branch can be anywher within the 64K-byte Program Memory address space.

Addr. 11

11-bit destination address. Used by ACALL & AJMP. The branch will be within the same 2K-byte page of program memory as the first byte of the following instruction.

Rel

Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is – 128 to +127 bytes relative to first byte of the following instruction.

Bit

Direct Addressed bit in Internal Data RAM or Special Function Register.

* New operation not provided by UM8048/8049.

ARITHMETIC OPERATIONS

Mnemonic	Descriptions	Bytes	Cycles
ADD A, Rn	Add register to accumulator	1	1
ADD A, direct	Add direct byte to accumulator	2	1
ADD A, @ Ri	Add indirect RAM to accumulator	1	1
ADD A, # data	Add immediate data to accumulator	2	1
ADDC A, Rn	Add register to accumulator with carry	1	1
ADDC A, direct	Add direct byte to accumulator with carry	2	1
ADDC A, @ Ri	Add indirect RAM to accumulator with carry	1	1
ADDC A, # data	Add immediate data to Acc with carry	2	1
SUBB A, Rn	Subtract register from Acc with borrow	1	1
SUBB A, direct	Subtract direct byte from Acc with borrow	2	1
SUBB A, @ Ri	Subtract indirect RAM from Acc with borrow	1	1
SUBB A, # data	Subtract immediate data from Acc with borrow	2	1
INC A	Increment accumulator	1	1
INC Rn	Increment register	1	1
INC direct	Increment direct byte	2	1
INC @ Ri	Increment indirect RAM	1	1
DEC A	Decrement accumulator	1	1
DEC Rn	Decrement register	1	1
DEC direct	Decrement direct byte	2	1
DEC @ Ri	Decrement indirect RAM	1	1
INC DPTR	Increment data pointer	1	2
MUL AB	Multiply A & B	1	4
DIV AB	Divide A by B	1	4
DA A	Decimal adjust accumulator	1	1

LOGICAL OPERATIONS

Mnemonic	Descriptions	Bytes	Cycles
ANL R, Rn	AND register accumulator	1	1
ANL A, direct	AND direct byte to accumulator	2	1
ANL A, @ Ri	AND indirect RAM to accumulator	1	1
ANL A, # data	AND immediate data to accumulator	2	1
ANL direct, A	AND accumulator to direct byte	2	1
ANL direct, # data	AND immediate data to direct byte	3	2
ORL A, Rn	OR register to accumulator	1	1
ORL A, direct	OR direct byte to accumulator	3	1
ORL A, @ Ri	OR indirect RAM to accumulator	1	1
ORL A, # data	OR immediate data to accumulator	2	1
ORL direct, A	OR accumulator to direct byte	2	1
ORL direct, # data	OR immediate data to direct byte	3	2
XRL A, Rn	Exclusive-OR register to accumulator	1	1
XRL A, direct	Exclusive-OR direct byte to accumulator	2	1
XRL A, @ Ri	Exclusive-OR indirect RAM to accumulator	1	1
XRL A, # data	Exclusive-OR immediate data to accumulator	2	1
XRL direct, A	Exclusive-OR accumulator to direct byte	2	1
XRL direct, # data	Exclusive-OR immediate data to direct byte	3	2
CLR A	Clear accumulator	1	1
CPL A	Complement accumulator	1	1
RL A	Rotate accumulator left	1	1
RLC A	Rotate accumulator left through the carry	1	1
RR A	Rotate accumulator right	1	1
RRC A	Rotate accumulator right through the carry	1	1
SWAP A	Swap nibbles within the accumulator	1	1

DATA TRANSFER

Mnemonic	Descriptions	Bytes	Cycles
MOV A, Rn	Move register to accumulator	1	1
MOV A, direct	Move direct byte to accumulator	2	1
MOV A, @ Ri	Move indirect RAM to accumulator	1	1
MOV A # data	Move immediate data to accumulator	2	1
MOV Rn, A	Move accumulator to register	1	1
MOV Rn, direct	Move direct byte to register	2	2
MOV Rn, # direct	Move direct byte to register	2	1
MOV direct, A	Move accumulator to direct byte	2	1
MOV direct, Rn	Move register to direct byte	2	2
MOV direct, direct	Move direct byte to direct	3	2
MOV direct, @ Ri	Move indirect RAM to direct byte	2	2
MOV direct, # data	Move immediate data to direct byte	3	2
MOV @ Ri, A	Move accumulator to indirect RAM	1	1
MOV @ Ri, direct	Move direct byte to indirect RAM	2	2
MOV @ Ri, # data	Move immediate data to indirect RAM	2	1
MOV DPTR, # data 16	Load data pointer with a 16-bit constant	3	2
MOVC A, @ A + DPTR	Move code byte relative to DPTR to Acc	1	2
MOVC A, @ A + PC	Move code byte relative to PC and Acc	1	2
MOVX A, @ Ri	Move external RAM (8-bit addr) to Acc	1	2
MOVX A, @ DPTR	Move external RAM (16-bit addr) to Acc	1	2
MOVX @ Ri, A	Move Acc to external RAM (8-bit addr.)	1	2
MOVX @DPTR, A	Move Acc to external RAM (16-bit addr.)	1	2
PUSH direct	Push direct byte onto stack	2	2
POP direct	Pop direct byte from stack	2	2
XCH A, Rn	Exchange register with accumulator	1	1
XCH A, direct	Exchange direct byte with accumulator	2	1
XCH A, @ Ri	Exchange indirect RAM with accumulator	1	1
XCHD A, @ Ri	Exchange low-order digit indirect RAM with Acc	1	1

BOOLEAN VARIABLE MANIPULATION

Mnemonic	Descriptions	Bytes	Cycles
CLR C	Clear carry	1	1
CLR bit	Clear direct bit	2	1
SETB C	Set carry	1	1
SETB bit	Set direct bit	2	1
CPL C	Complement carry	1	1
CPL bit	Complement direct bit	2	1
ANL C, bit	AND direct bit to carry	2	2
ANL C,/bit	AND complement of direct bit to carry	2	2
ORL C, bit	OR direct bit to carry	2	2
ORL C,/bit	OR complement of direct bit to carry	2	2
MOV C, bit	Move direct bit to carry	2	2
MOV bit, C	Move carry to direct bit	2	2
JC rel	Jump if carry is set	2	2
JNC rel	Jump if carry not set	2	2
JB bit, rel	Jump if direct bit is set	3	2
JNB bit, rel	Jump if direct but is not set	3	2
JBC bit, rel	Jump if direct bit is set & clear bit	3	2

PROGRAMING BRANCHING

Mnemonic	Descriptions	Bytes	Cycles
ACALL addr. 11	Absolute subroutine call	2	2
LCALL addr. 16	Long subroutine call	3	2
RET	Return for subroutine	1	2
RETI	Return for interrupt	1	2
AJMP addr. 11	Absolute jump	2	2
LIMP addr. 16	Long jump	3	2
SJMP rel	Short jump (relative addr.)	2	2
JMP @ A + DPTR	Jump indirect relative to the DPTR	1	2
JZ rel	Jump if accumulator is zero	2	2
JNZ rel	Jump if accumulator is not zero	2	2
CJNE A, direct, rel	Compare direct byte to Acc and jump if not equal	3	2
CJNE A, # data, rel	Compare immediate to Acc and jump if not equal	3	2
CJNE Rn, # data, rel	Compare immediate to register and jump if not equal	3	2
CJNE @ Ri, # data, rel	Compare immediate to indirect and jump if not equal	3	2
DJNZ Rn, rel	Decrement register and jump if not zero	3	2
DJNZ direct, rel	Decrement direct byte and jump if not zero	3	2
NOP	No operation	1	1

Microprocessor

Selection Guide

Part No.	Descriptions	Compatible Devices	Remarks	Page
UM6502	8 Bit CPU	SYP 6502	1, 2, 3, 4 MHz Version	4–3
UM6507	8 Bit CPU	SYP 6507	1, 2 MHz Version	4–3
UM6512	8 Bit CPU	SYP 6512	1, 2, 3 MHz Version	4–3

UM6502 / UM6507 / UM6512

8-Bit Microprocessors

Features

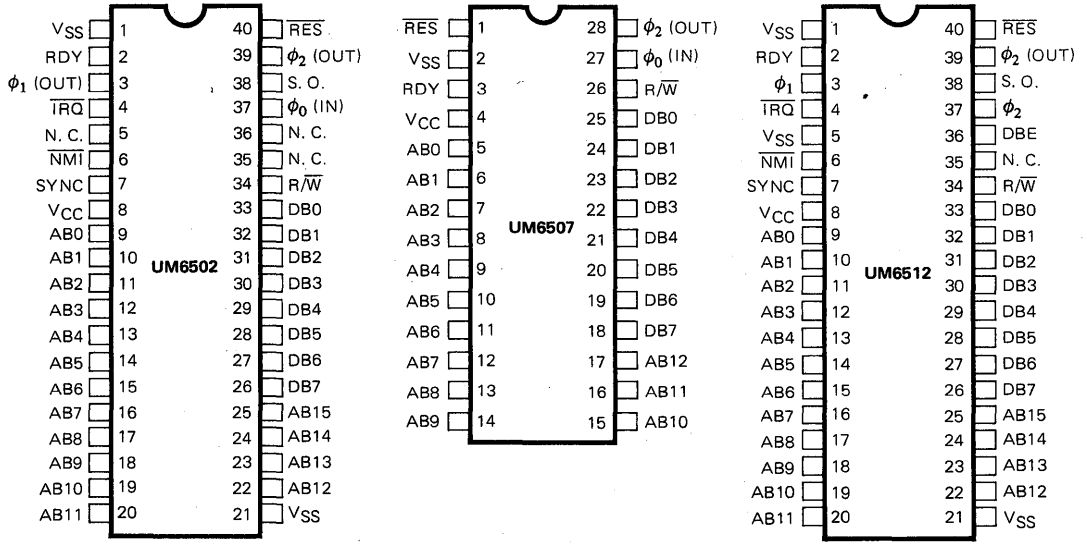
- Single 5V ± 5% power supply
- N channel, silicon gate, depletion load technology
- 56 instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- Non-maskable interrupt
- Bi-directional data bus
- Addressable memory range of up to 64K bytes
- "Ready" input
- Direct memory access capability
- Bus compatible with MC6800
- Choice of external or on-board clocks
- 1MHz, 2MHz, 3MHz and 4MHz versions
- On-chip clock options
  - —External single clock input
  - —Crystal time base input
- Pipeline architecture

General Description

The UM6502/UM6507/UM6512 microprocessors are totally software compatible with one another. These products provide a selection of addressable memory range, interrupt input options and on-chip clock oscillators and drivers. The UM6502/UM6507 on-chip clock versions are aimed at high performance, low cost applications where single phase inputs or crystals provide the time base. The UM6512 external clock version is geared for the multi-processor system applications where maximum timing control is mandatory. These products are bus compatible with the MC6800 product offering.

Microprocessor

Pin Configuration



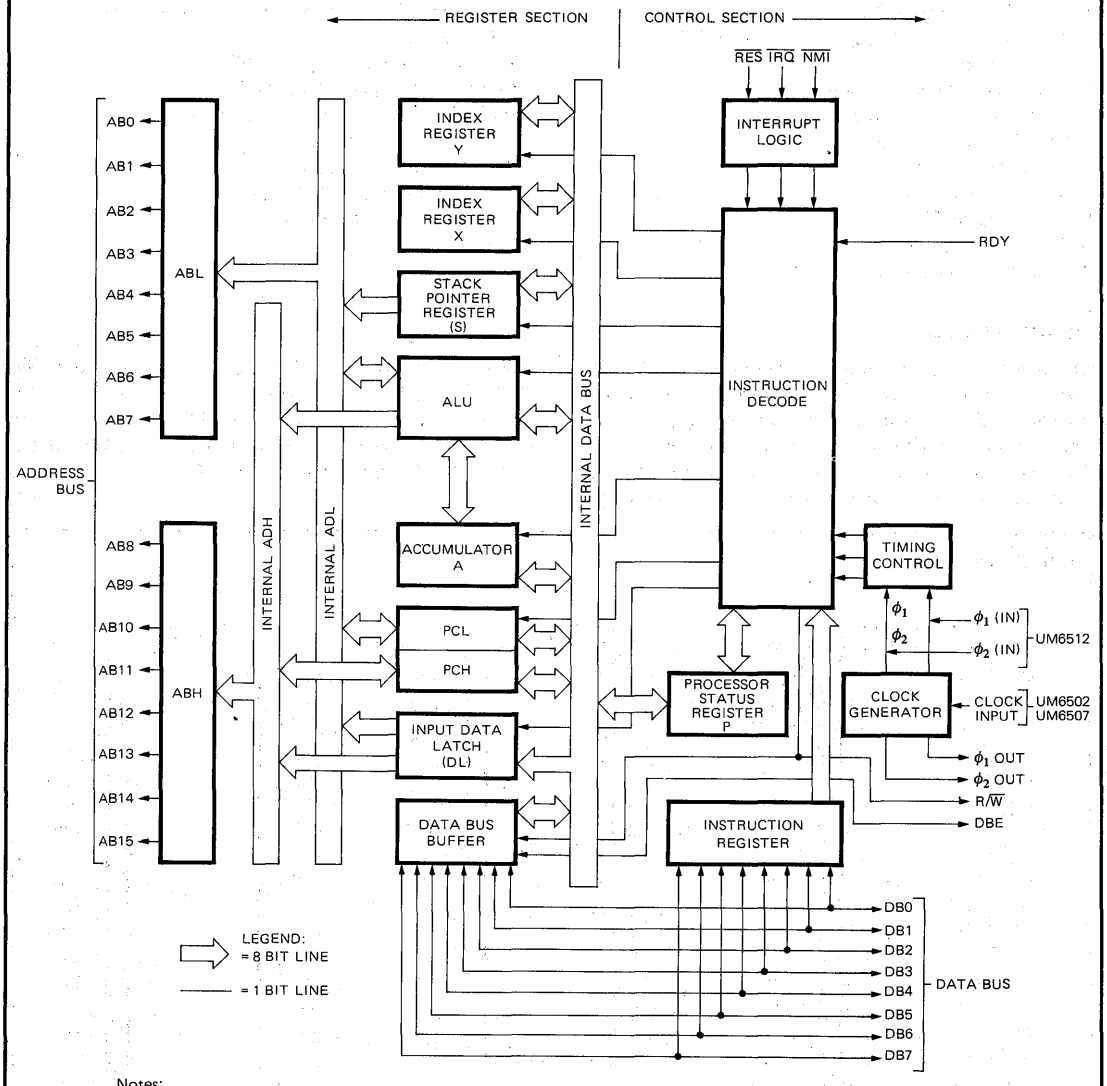
Absolute Maximum Ratings*

Supply Voltage V_{CC}	−0.3 to +7.0V
Input Voltage V_{IN}	−0.3 to +7.0V
Operating Temperature T_A	0 to 70°C
Storage Temperature T_{STG}	−55 to +150°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Notes:
1. CLOCK GENERATOR IS NOT INCLUDED ON UM6512
2. ADDRESSING CAPABILITY AND CONTROL OPTIONS VARY WITH EACH PRODUCTS.

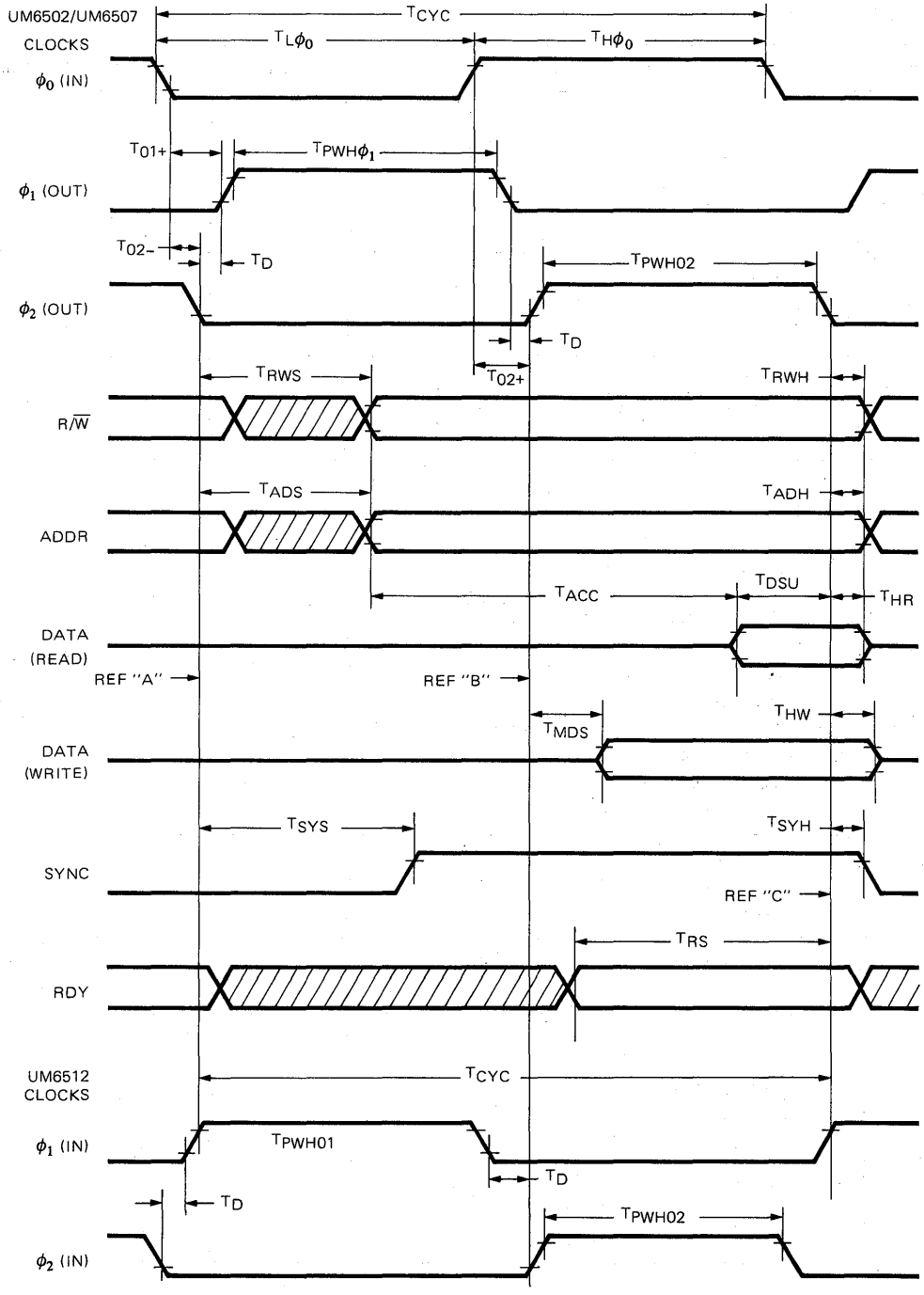
D.C. Characteristics

(V_{CC} = 5.0V ± 5%, T_A = 0 – 70°C)

(ϕ_1, ϕ_2 applies to UM6512, ϕ_0 (in) applies to UM6502/UM6507)

Symbol	Characteristics	Min.	Max.	Units
V_{IH}	Input High Voltage			
	Logic and ϕ_0 (in) for UM6502/UM6507 — 1, 2, 3 MHz	+ 2.0	V_{CC}	V
	Logic and ϕ_0 (in) for UM6502/UM6507 — 4 MHz	+ 3.3	V_{CC}	V
	ϕ_1 and ϕ_2 only for UM6512 — All Speeds	V_{CC} – 0.5	V_{CC} + 0.25	V
V_{IL}	Input Low Voltage			
	Logic, ϕ_0(in) (UM6502/UM6507)	–0.3	+0.8	
	ϕ_1, ϕ_2 (UM6512)	–0.3	+0.2	V
I_{IL}	Input Loading (V_{IN} = 0V, V_{CC} = 5.25V)			
	RDY, S.O.	–10	–300	μA
I_{IN}	Input Leakage Current (V_{IN} = 0 to 5.25V, V_{CC} = 0)			
	Logic (Excl. RDY, S.O.)	–	2.5	μA
	ϕ_1, ϕ_2 (UM6512)	–	100	μA
	ϕ_0(in) (UM6502/UM6507)	–	10.0	μA
I_{TSI}	Three-State (Off State) Input Current (V_{IN} = 0.4 to 2.4V, V_{CC} = 5.25V)			
	DB0-DB7	–	±10	μA
V_{OH}	Output High Voltage (I_{LOAD} = –100μAdc, V_{CC} = 4.75V) 1, 2 MHz	2.4	–	V
	SYNC, DB0-DB7, A0-A15, R/$\overline{W}$			
V_{OL}	Output Low Voltage (I_{LOAD} = 1.6mAdc, V_{CC} = 4.75V) 1, 2 MHz	–	0.4	V
	SYNC, DB0-DB7, A0-A15, R/$\overline{W}$			
P_D	Power Dissipation 1MHz and 2MHz (V_{CC} = 5.25V)	–	700	mW
C	Capacitance (V_{IN} = 0, T_A = 25°C, f = 1 MHz)			
C_{IN}	$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, S.O., DBE	–	10	
	DB0-DB7	–	15	
C_{OUT}	A0-A15, R/$\overline{W}$, SYNC	–	12	pF
C_{ϕ_0} (in)	ϕ_0 (in) (UM6502/UM6507)	–	15	
C_{ϕ_1}	ϕ_1 (UM6512)	–	50	
C_{ϕ_2}	ϕ_2 (UM6512)	–	80	

Microprocessor


UM6502/UM6507 CLOCKS
ϕ_0 (IN)
ϕ_1 (OUT)
ϕ_2 (OUT)
R/$\overline{W}$
ADDR
DATA (READ)
DATA (WRITE)
SYNC
RDY
UM6512 CLOCKS
ϕ_1 (IN)
ϕ_2 (IN)
TCYC
TLϕ0
THϕ0
T01+
TPWHϕ1
T02-
TD
TPWH02
T02+
TRWS
TRWH
TADS
TADH
TACC
TDSU
THR
REF "A"
REF "B"
TMDS
THW
TSYS
TSYH
REF "C"
TRS
TPWH01

Dynamic Operating Characteristics

(V_{CC} = 5.0 ± 5%, T_A = 0° to 70°C)

Parameter	Symbol	1 MHz		2 MHz		3 MHz		4 MHz		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
UM6512										
Cycle Time	T_{CYC}	1.00	40	0.50	40	0.33	40	0.25	40	μs
ϕ_1 Pulse Width	$T_{PWH\phi_1}$	430	–	215	–	150	–			ns
ϕ_2 Pulse With	$T_{PWH\phi_2}$	470	–	235	–	160	–			ns
Delay Between ϕ_1 and ϕ_2	T_D	0	–	0	–	0	–			ns
ϕ_1 and ϕ_2 Rise and Fall Times(1)	T_R, T_F	0	25	0	20	0	15			ns
UM6502/UM6507										
Cycle Time	T_{CYC}	1.00	40	0.50	40	0.33	40	0.25	40	μs
$\phi_{0(IN)}$ Low Time(2)	$T_{L\phi_0}$	480	–	240	–	160	–	110	–	ns
$\phi_{0(IN)}$ High Time(2)	$T_{H\phi_0}$	460	–	240	–	160	–	115	–	ns
ϕ_0 Neg to ϕ_1 Pos Delay(5)	T_{01+}	10	70	10	70	10	70	10	70	ns
ϕ_0 Neg to ϕ_2 Neg Delay(5)	T_{02-}	5	65	5	65	5	65	5	65	ns
ϕ_0 Pos to ϕ_1 Neg Delay(5)	T_{01-}	5	65	5	65	5	65	5	65	ns
ϕ_0 Pos to ϕ_2 Pos Delay(5)	T_{02+}	15	75	15	75	15	75	15	75	ns
$\phi_{0(IN)}$ Rise and Fall Time(1)	T_{RO}, T_{FO}	0	30	0	20	0	15	0	10	ns
ϕ_1 (OUT), Pulse Width	$T_{PWH\phi_1}$	$T_{L\phi_0}$-20	$T_{L\phi_0}$	$T_{L\phi_0}$-20	$T_{L\phi_0}$	$T_{L\phi_0}$-20	$T_{L\phi_0}$	$T_{L\phi_0}$-20	$T_{L\phi_0}$	ns
ϕ_2 (OUT), Pulse Width	$T_{PWH\phi_2}$	$T_{L\phi_0}$-40	$T_{L\phi_0}$-10	$T_{L\phi_0}$-40	$T_{L\phi_0}$-40	$T_{L\phi_0}$-40	$T_{L\phi_0}$-10	$T_{L\phi_0}$-40	$T_{L\phi_0}$-10	ns
Delay Between ϕ_1 and ϕ_2	T_D	5	–	5	–	5	–	5	–	ns
ϕ_1 and ϕ_2 Rise and Fall Times(1, 3)	T_R, T_F	–	25	–	25	–	15	–	15	ns
UM6502/UM6507/UM6512										
R/W Setup Time	T_{RWS}	–	225	–	140	–	110	–	90	ns
R/W Hold Time	T_{RWH}	30	–	30	–	15	–	10	–	ns
Address Setup Time	T_{ADS}	–	225	–	140	–	110	–	90	ns
Address Hold Time	T_{ADH}	30	–	30	–	15	–	10	–	ns
Read Access Time	T_{ACC}	–	650	–	310	–	170	–	110	ns
Read Data Setup Time	T_{DSU}	100	–	50	–	50	–	50	–	ns
Read Data Hold Time	T_{HR}	10	–	10	–	10	–	10	–	ns
Write Data Setup Time	T_{MDS}	20	175	20	100	20	75	–	70	ns
Write Data Hold Time	T_{HW}	60	150	60	150	30	130	20	–	ns
Sync Setup Time	T_{SYS}	–	350	–	175	–	100	–	90	ns
Sync Hold Time	T_{SYH}	30	–	30	–	15	–	15	–	ns
RDY Setup Time(4)	T_{RS}	200	–	200	–	150	–	120	–	ns

Notes:

1. Measured between 10% and 90% points.
2. Measured at 50% points.
3. Load = 1 TTL load + 30 pF.
4. RDY must never switch states within T_{RS} to end of ϕ_2.
5. Load = 100 pF.
6. The 2 MHz devices are identified by an "A" suffix.
7. The 3 MHz devices are identified by an "B" suffix.
8. The 4 MHz devices are identified by an "C" suffix.

Timing Diagram Note:

Because the clock generation for the UM6502/UM6507 and UM6512 is different, the two clock timing sections are referenced to the main timing diagram by three reference lines marked REF 'A', REF 'B' and REF 'C'. Reference between the two sets of clock timings is without meaning. Timing parameters are referred to these lines and scale variations in the diagrams are of no consequence.

Pin Description

Clocks (ϕ_1, ϕ_2)
The UM6512 requires a two phase non-overlapping clock that runs at the V_{CC} voltage level.

The UM6502/UM6507 clocks are supplied with an internal clock generator. The frequency of these clocks is externally controlled. Clock generator circuits are shown elsewhere in this data sheet.

Address Bus (A_0-A_{15})
(See sections on each micro for respective address lines on those devices.)

These outputs are TTL compatible, capable of driving one standard TTL load and 130 pF.

Data Bus (DB_0-DB_7)
Eight pins are used for the data bus. This is a bidirectional bus, transferring data to and from the device and peripherals. The outputs are three-state buffers, capable of driving one standard TTL load and 130 pF.

Data Bus Enable (DBE)
This TTL compatible input allows external control of the three-state data output buffers and will enable the microprocessor bus driver when in the high state. In normal operation DBE would be driven by the phase two (ϕ_2) clock, thus allowing data output from microprocessor only during ϕ_2. During the read cycle, the data bus drivers are internally disabled, becoming essentially an open circuit. To disable data bus drivers externally, DBE should be held low. This signal is available on the UM6512 only.

Ready (RDY)
This input signal allows the user to halt the microprocessor on all cycles except write cycles. A negative transition to the low state during or coincident with phase one, (ϕ_1) will halt the microprocessor with the output address lines reflecting the current address being fetched. This condition will remain through a subsequent phase two (ϕ_2) in which the Ready signal is low. This feature allows microprocessor interfacing with low speed PROMS as well as fast (max. 2 cycle) Direct Memory Access (DMA). If ready is low during a write cycle, it is ignored until the following read operation. Ready transitions must not be permitted during ϕ_2 time.

Interrupt Request ($\overline{IRQ}$)
This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At the time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no futher interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3KΩ external resistor should be used for proper wire-OR operation.

Non-Maskable Interrupt ($\overline{NMI}$)
A negative going transition on this input requests that a non-maskable interrupt sequence be generated within the microprocessor.

$\overline{NMI}$ is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for $\overline{IRQ}$ will be performed, regardless of the state interrupt mask flag. The vector address loaded into the program counter, low and high, are locations FFFA and FFFB respectively, thereby transferring program control to the memory vector located at these addresses. The instructions loaded at these locations cause the microprocessor to branch to a non-maskable interrupt routine in memory.

$\overline{NMI}$ also requires an external 3KΩ resistor to V_{CC} for proper wire-OR operations.

Inputs $\overline{IRQ}$ and $\overline{NMI}$ are hardware interrupts lines that are sampled during ϕ_2 (Phase 2) and will begin the appropriate interrupt routine on the ϕ_1 (phase 1) following the completion of the current instruction.

Set Overflow Flag (S. O.)
A NEGATIVE going edge on this input sets the overflow bit in the Status Code Register. This signal is sampled on the trailing edge of ϕ_1.

SYNC
This output line is provided to identify those cycles in which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during ϕ_1 of an OPCODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the ϕ_1 clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

Reset ($\overline{RES}$)
This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

After V_{CC} reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/$\overline{W}$ and SYNC signal will become valid. When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

Read/Write (R/$\overline{W}$)
This output signal is used to control the direction of data transfers between the processor and other circuits on the data bus. A high level on R/$\overline{W}$ signifies data into the processor; a low is for the data transfer out of the processor.

Programming Characteristics

INSTRUCTION SET – ALPHABETIC SEQUENCE

ADC	Add Memory to Accumulator with Carry
AND	"AND" Memory with Accumulator
ASL	Shift left One Bit (Memory or Accumulator)
BCC	Branch on Carry Clear
BCS	Branch on Carry Set
BEQ	Branch on Result Zero
BIT	Test Bits in Memory with Accumulator
BMI	Branch on Result Minus
BNE	Branch on Result not Zero
BPL	Branch on Result Plus
BNK	Force Break
BVÇ	Branch on Overflow Clear
BVS	Branch on Overflow Set
CLC	Clear Carry Flag
CLD	Clear Decimal Mode
CLI	Clear Interrupt Disable Bit
CLV	Clear Overflow Flag
CMP	Compare Memory and Accumulator
CPX	Compare Memory and Index X
CPY	Compare Memory and Index Y
DEC	Decrement Memory by One
DEX	Decrement Index X by One
DEY	Decrement Index Y by One
EOR	"Exclusive-or" Memory with Accumulator
INC	Increment Memory by One
INX	Increment Index X by One
INY	Increment Index Y by One
JMP	Jump to New Location
JSR	Jump to New Location Saving Return Address
LDA	Load Accumulator with Memory
LDX	Load Index X with Memory
LDY	Load Index Y with Memory
LSR	Shift One Bit Right (Memory or Accumulator)
NOP	No Operation
ORA	"OR" Memory with Accumulator
PHA	Push Accumulator on Stack
PHP	Push Processor Status on Stack
PLA	Pull Accumulator from Stack
PLP	Pull Processor Status from Stack
ROL	Rotate One Bit Left (Memory or Accumulator)
ROR	Rotate One Bit Right (Memory or Accumulator)
RTI	Return from Interrupt
RTS	Return from Subroutine
SBC	Subtract Memory from Accumulator with Borrow
SEC	Set Carry Flag
SED	Set Decimal Mode
SEI	Set Interrupt Disable Status
STA	Store Accumulator in Memory
STX	Store Index X in Memory
STY	Store Index Y in Memory
TAX	Transfer Accumulator to Index X
TAY	Transfer Accumulator to Index Y
TSX	Transfer Stack Pointer to Index X
TXA	Transfer Index X to Accumulator
TXS	Transfer Index X to Stack Pointer
TYA	Transfer Index Y to Accumulator

ADDRESSING MODES

Accumulator Addressing
This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

Immediate Addressing
In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

Absolute Addressing
In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

Zero Page Addressing
The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

Indexed Zero Page Addressing – (X, Y indexing)
This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, "X" or "Zero Page, Y." The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the secondbyte references a location in page zero. Additionally due to the "Zero Page" addressing

nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

Indexed Absolute Addressing – (X, Y indexing)
This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X," and "Absolute, Y." The effective address is formed by adding the contents of X or Y to the address contained in the second and thirdbytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

Implied Addressing
In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

Relative Addressing
Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

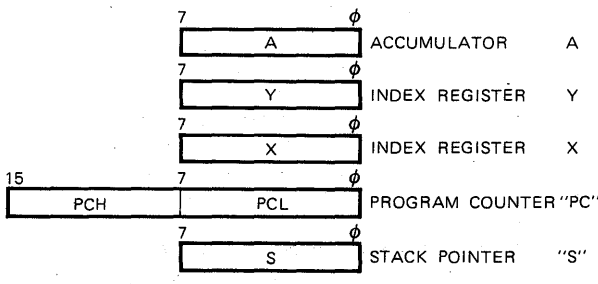
The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is-128 to + 127 bytes from the next instruction.

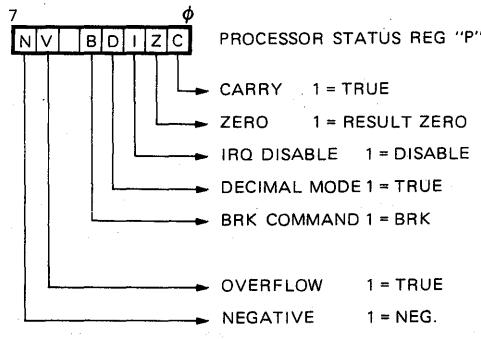
Indexed Indirect Addressing
In indexed indirect addressing (referred to as [Indirect, X]), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

Indirect Indexed Addressing
In indirect indexed addressing (referred to as [Indirect], Y), the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

Absolute Indirect
The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

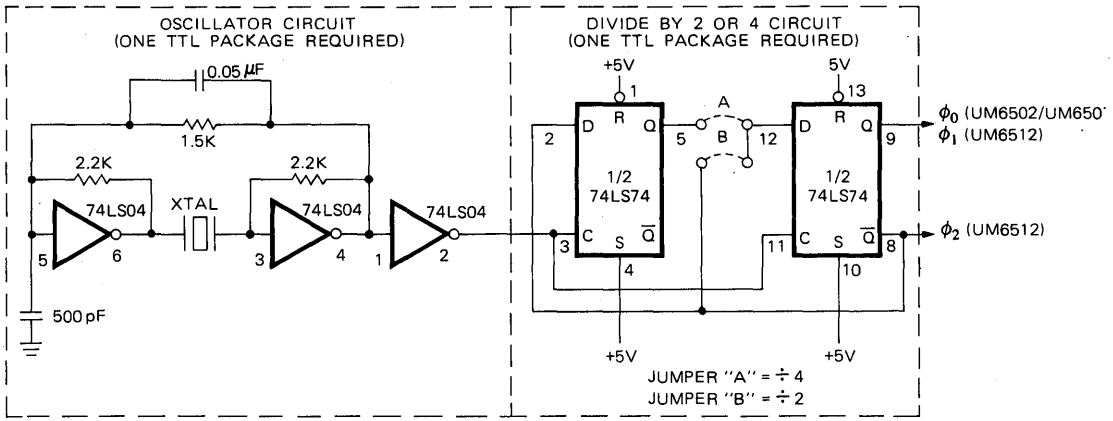
PROGRAMMING MODEL



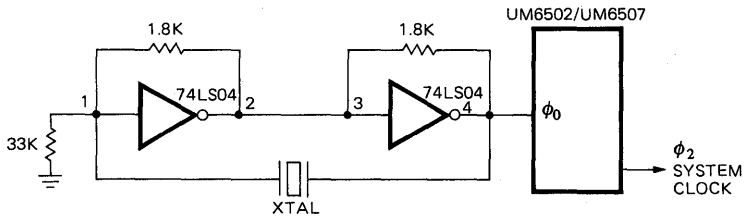


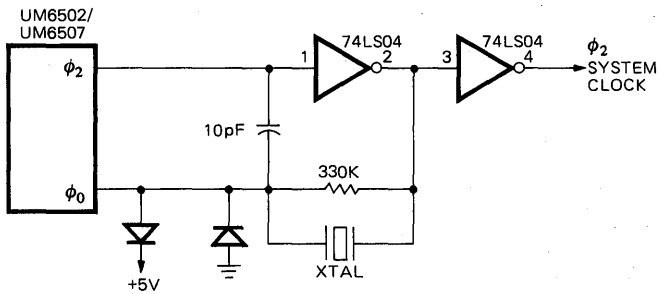
Clock Generation Circuits*

* Crystals used are CTS Knight MP Series or equivalents. (Series Mode)



Crystal Frequency	Output Frequency	
	÷2	÷4
3.579545 MHz	1.7897 MHz	0.894886 MHz
4.194304 MHz	2.097152 MHz	1.048576 MHz





Instruction Set

Instructions				Immediate			Absolute			Zeropage			Accum			Implied			(Ind. X)			((Ind. Y)		
Mnemonic			Operation	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
A	D	C	A + M + C → A (4) (1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2
A	N	D	A ∧ M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2
A	S	L	C ← [7 0] ← 0				0E	6	3	06	5	2	0A	2	1									
B	C	C	BRANCH ON C = 0 (2)																					
B	C	S	BRANCH ON C = 1 (2)																					
B	E	Q	BRANCH ON Z = 1 (2)																					
B	I	T	A ∧ M				2C	4	3	24	3	2												
B	M	I	BRANCH ON N = 1 (2)																					
B	N	E	BRANCH ON Z = 0 (2)																					
B	P	L	BRANCH ON N = 0 (2)																					
B	R	K	BREAK													00	7	1						
B	V	C	BRANCH ON V = 0 (2)																					
B	V	S	BRANCH ON V = 1 (2)																					
C	L	C	0 → C													18	2	1						
C	L	D	0 → D													D8	2	1						
C	L	I	0 → 1													58	2	1						
C	L	V	0 → V													B8	2	1						
C	M	P	A − M	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2
C	P	X	X − M	E0	2	2	EC	4	3	E4	3	2												
C	P	Y	Y − M	C0	2	2	CC	4	3	C4	3	2												
D	E	C	M − 1 → M				CE	6	3	C6	5	2												
D	E	X	X − 1 → X													CA	2	1						
D	E	Y	Y − 1 → Y													88	2	1						
E	O	R	A V M → A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2
I	N	C	M + 1 → M				EE	6	3	E6	5	2												
I	N	X	X + 1 → X													E8	2	1						
I	N	Y	Y + 1 → Y													C8	2	1						
J	M	P	JUMP TO NEW LOC				4C	3	3															
J	S	R	JUMP SUB				20	6	3															
L	D	A	M A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2
L	D	X	M → X (1)	A2	2	2	AE	4	3	A6	3	2												
L	D	Y	M → Y (1)	A0	2	2	AC	4	3	A4	3	2												
L	S	R	0 → [7 0] → C				4E	6	3	46	5	2	4A	2	1									
N	O	P	NO OPERATION													EA	2	1						
O	R	A	A V M → A	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2
P	H	A	A → MS S − 1 → S													48	3	1						
P	H	P	P → MS S − 1 → S													08	3	2						
P	L	A	S + 1 → S MS → A													68	4	1						
P	L	P	S + 1 → S MS → P													28	4	1						
R	O	L	← [7 0] ← [C] ←				2E	6	3	26	5	2	2A	2	1									
R	O	R	→ [C] → [0 7] →				6E	6	3	66	5	2	6A	2	1									
R	T	I	RTRN INT													40	6	1						
R	T	S	RTRN SUB													60	6	1						
S	B	C	A − M − $\overline{C}$ → A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2
S	E	C	1 → C													38	2	1						
S	E	D	1 → D													F8	2	1						
S	E	I	1 → 1													78	2	1						
S	T	A	A → M				8D	4	3	85	3	2							81	6	2	91	6	2
S	T	X	X → M				8E	4	3	86	3	2												
S	T	Y	Y → M				8C	4	3	84	3	2												
T	A	X	A → X													AA	2	1						
T	A	Y	A → Y													A8	2	1						
T	S	X	S → X													BA	2	1						
T	X	A	X → A													8A	2	1						
T	X	S	X → S													9A	2	1						
T	Y	A	Y → A													98	2	1						

(1) ADD 1 TO N IF PAGE BOUNDARY IS CROSSED
(2) ADD 1 TO N IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO N IF BRANCH OCCURS TO DIFFERENT PAGE
(3) CARRY NOT = BORROW
(4) IF IN DECIMAL MODE Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

Z Page. X			Abs. X			Abs. Y			Relative			Indirect			Z Page. Y			Processor Status Codes								Mnemonic
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	7	6	5	4	3	2	1	0	
																		N	V	.	B	D	I	Z	C	
75	4	2	7D	4	3	79	4	3										N	V	.	.	.	.	Z	C	ADC
35	4	2	3D	4	3	39	4	3										N	.	.	.	.	.	Z	.	AND
16	6	2	1E	7	3													N	.	.	.	.	.	Z	C	ASL
									90	7	2							.	.	.	.	.	.	.	.	BCC
									B0	2	2							.	.	.	.	.	.	.	.	BCS
									F0	2	2															BEQ
																		M_7	M_6	.	.	.	.	Z	.	BIT
									30	2	2							.	.	.	.	.	.	.	.	BMI
									D0	2	2							.	.	.	.	.	.	.	.	BNE
									10	2	2							.	.	.	.	.	.	.	.	BPL
																		.	.	.	1	.	1	.	.	BRK
									50	2	2							.	.	.	.	.	.	.	.	BVC
									70	2	2							.	.	.	.	.	.	.	.	BVS
																		.	.	.	.	.	.	.	0	CLC
																		.	.	.	.	0	.	.	.	CLD
																		.	.	.	.	.	0	.	.	CLI
																		.	0	.	.	.	.	.	.	CLV
D5	4	2	DD	4	3	D9	4	3										N	.	.	.	.	.	Z	C	CMP
																		N	.	.	.	.	.	Z	C	CPX
																		N	.	.	.	.	.	Z	C	CPY
D6	6	2	DE	7	3													N	.	.	.	.	.	Z	.	DEC
																		N	.	.	.	.	.	Z	.	DEX
																		N	.	.	.	.	.	Z	.	DEY
55	4	2	5D	4	3	59	4	3										N	.	.	.	.	.	Z	.	EOR
F6	6	2	FE	7	3													N	.	.	.	.	.	Z	.	INC
																		N	.	.	.	.	.	Z	.	INX
																		N	.	.	.	.	.	Z	.	INY
												6C	5	3				.	.	.	.	.	.	.	.	JMP
B5	4	2	BD	4	3	B9	4	3										N	.	.	.	.	.	Z	.	JSR
						BE	4	3							B6	4	2	N	.	.	.	.	.	Z	.	LDA
B4	4	2	BC	4	3													N	.	.	.	.	.	Z	.	LDX
56	6	2	5E	7	3													0	.	.	.	.	.	Z	C	LDY
																		.	.	.	.	.	.	.	.	LSR
15	4	2	1D	4	3	19	4	3										N	.	.	.	.	.	Z	.	NOP
																		.	.	.	.	.	.	.	.	ORA
																		.	.	.	.	.	.	.	.	PHA
																		.	.	.	.	.	.	.	.	PHP
																		N	.	.	.	.	.	Z	.	PLA
																					(RESTORED)					PLP
36	6	2	3E	7	3													N	.	.	.	.	.	Z	C	ROL
76	6	2	7E	7	3													N	.	.	.	.	.	Z	C	ROR
																					(RESTORED)					RTI
																		.	.	.	.	.	.	.	.	RTS
F5	4	2	FD	4	3	F9	4	3										N	V	.	.	.	.	Z	(3)	SBC
																		.	.	.	.	.	.	.	1	SEC
																		.	.	.	.	1	.	.	.	SED
																		.	.	.	.	.	1	.	.	SEI
95	4	2	9D	5	3	99	5	3										.	.	.	.	.	.	.	.	STA
															96	4	2	.	.	.	.	.	.	.	.	STX
94	4	2																.	.	.	.	.	.	.	.	STY
																		N	.	.	.	.	.	Z	.	TAX
																		N	.	.	.	.	.	Z	.	TAY
																		N	.	.	.	.	.	Z	.	TSX
																		N	.	.	.	.	.	Z	.	TXA
																		N	.	.	.	.	.	.	.	TXS
																		N	.	.	.	.	.	Z	.	TYA

X INDEX X
Y INDEX Y
A ACCUMULATOR
M MEMORY PER EFECTIVE ADDRESS
Ms MEMORY PER STACK POINTER

\+ ADD
– SUBTRACT
∧ AND
V OR
¥ EXCLUSIVE OR

M_7 MEMORY BIT 7
M_6 MEMORY BIT 6
n NO. CYCLES
NO. BYTES

Ordering Information

1 MHz	2 MHz	3 MHz	4 MHz
UM6502	UM6502A	UM6502B	UM6502C
UM6507	–	–	–
UM6512	UM6512A	UM6512B	UM6512C

Part Number	Clocks	Pins	IRQ	NMI	RYD	Addressing
UM6502	On-Chip	40	√	√	√	64K
UM6507	On-Chip	28			√	8K
UM6512	External	40	√	√	√	64K

Microprocessor

CRT Controller

Selection Guide *

Part No.	Descriptions	Compatible Devices	Remarks	Page
UM6845/A/B	CRT Controller	HD 6845S	1, 1.5, 2 MHz Version	5–3
UM6845R	CRT Controller	SYP 6845R	1, 2, 3 MHz Version	5–26
UM6845E	CRT Controller	SYP 6845E	1, 2, 3 MHz Version	5–39
*UM9007	CRT Controller	SMC 9007	–	5–56
UM8321	Video Attributes Controller	SMC 9021	30, 28.5 MHz Version	5–57
UM8312	Double Row Buffer	SMC 9212	–	5–71

* Under Development

UM6845/UM6845A/UM6845B

CRT Controller

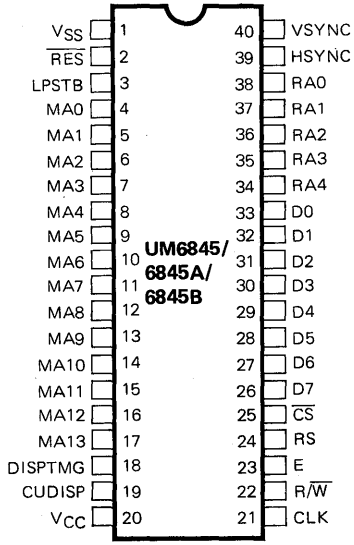
Features

- Applications include smart, programmable, intelligent CRT terminals; video games; information display
- Alphanumeric, semi-graphic, and full graphic capability
- Fully programmable via processor data bus and can generate timing for almost any alphanumeric screen density
- Single +5 volt supply, TTL compatible I/O, NMOS Technology
- Hardware scrolling by page, line or character
- Provides CPU's with synchronous signals to external device
- Programmable cursor format
- Light pen registers and input strobe signal to latch the light pen position on screen
- Line buffer-less operation. No external DMA required. Reading screen memory is mutliplexed between CRTC and CPU
- Programmable interlace or non-interlace scan
- 14-bit wide display memory reading address

General Description

The CRTC UM6845 family are LSI controllers designed to provide an interface for microcomputers to raster scan type CRT displays. The CRTC belongs to the MC6800 LSI Family and has full compatibility with CPU in both data lines and control lines. Its primary function is to generate timing signals which are necessary for raster-scan type CRT displays according to the specification programmed by the CPU.

Pin Configuration



Absolute Maximum Ratings

Supply Voltage, V_{CC}* . . . . . −0.3~+7.0V
Input Voltage, V_{IN}* . . . . . −0.3~+7.0V
Operating Temperature, T_{OPR} . . . . . 0°~70°C
Storage Temperature, T_{STG} . . . . . −55°~+150°C

*With respect to V_{SS} (SYSTEM GND)

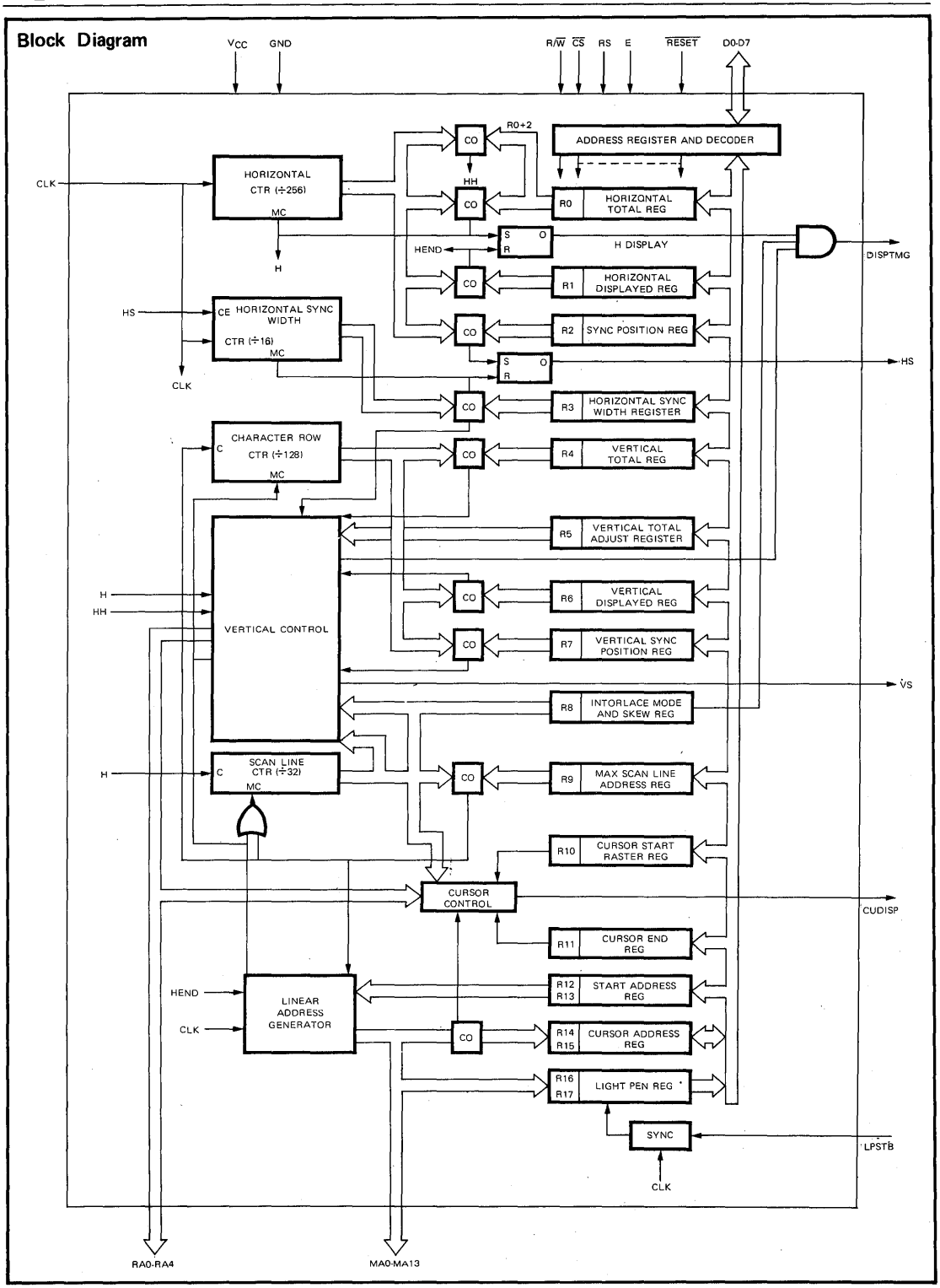
*Comments

Strees above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Electrical Characteristics

Item	Symbol	Test Conditions		Min.	Typ.	Max.	Units
Supply Voltage	V_{CC}	–		4.75	5.0	5.25	V
Input Voltage	V_{IL}	–		−0.3	–	0.8	V
	V_{IH}	–		2.0	–	V_{CC}	V
Input Leakage Current	I_{IN}	V_{IN} = 0 – 5.25V (Except D0 – D7)		−2.5	–	2.5	μA
Three-State Input Current (Off-State)	I_{TSI}	V_{IN} = 0.4 – 2.4V V_{CC} = 5.25V (D0 – D7)		−10	–	10	μA
Output "High" Voltage	V_{OH}	I_{LOAD} = 205A (D0 – D7)		2.4	–	–	V
		I_{LOAD} = −100μA (Other Outputs)					
Output "Low" Voltage	V_{OL}	I_{LOAD} = 1.6mA		–	–	0.4	V
Input Capacitance	C_{IN}	V_{IN} = 0 T_A = 25°C F = 1.0 MHz	D0 – D7	–	–	12.5	pF
			Other Input	–	–	10.0	pF
Output Capacitance	C_{OUT}	V_{IN} = 0V, T_A = 25°C, f = 1.0MHz		–	–	10.0	pF
Power Dissipation	P_D	T_A = 25°C, V_{CC} = 5.0V		–	–	1000	mW

Block Diagram



CRT Controller

A.C. Characteristics

(V_{CC} = 5V ± 5%, V_{SS} = 0V, T_A = −20 ~ +75°C)

BUS TIMING CHARACTERISTIC

MPU READ TIMING

Item	Symbol	UM6845			UM6845A			UM6845B			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Enable Cycle Time	$t_{cyc}E$	1.0	–	–	0.666	–	–	0.5	–	–	μS
Enable "High" Pulse Width	PW_{EH}	0.45	–	–	0.280	–	–	0.22	–	–	μS
Enable "Low" Pulse Width	PW_{EL}	0.40	–	–	0.280	–	–	0.21	–	–	μS
Enable Rise and Fall Time	t_{Er}, t_{Ef}	–	–	25	–	–	25	–	–	25	μS
Address Set Up Time	t_{AS}	140	–	–	140	–	–	70	–	–	nS
Data Delay Time	t_{DDR}	–	–	320	–	–	200	–	–	180	nS
Data Hold Time	t_H	10	–	–	10	–	–	10	–	–	nS
Address Hold Time	t_{AH}	10	–	–	10	–	–	10	–	–	nS
Data Access Time	t_{ACC}	–	–	460	–	–	360	–	–	250	nS

* See Fig-3

MPU WRITE TIMING

Item	Symbol	UM6845			UM6845A			UM6845B			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Enable Cycle Time	$t_{cyc}E$	1.0	–	–	0.666	–	–	0.5	–	–	μS
Enable "High" Pulse Width	PW_{EH}	0.45	–	–	0.280	–	–	0.22	–	–	μS
Enable "Low" Pulse Width	PW_{EL}	0.40	–	–	0.280	–	–	0.21	–	–	μS
Enable Rise and Fall Time	t_{Er}, t_{Ef}	–	–	25	–	–	25	–	–	25	nS
Address Set Up Time	t_{AS}	140	–	–	140	–	–	70	–	–	nS
Data Set Up Time	t_{DSW}	195	–	–	80	–	–	60	–	–	nS
Data Hold Time	t_H	10	–	–	10	–	–	10	–	–	nS
Address Hold Time	t_{AH}	10	–	–	10	–	–	10	–	–	nS

* See Fig-4

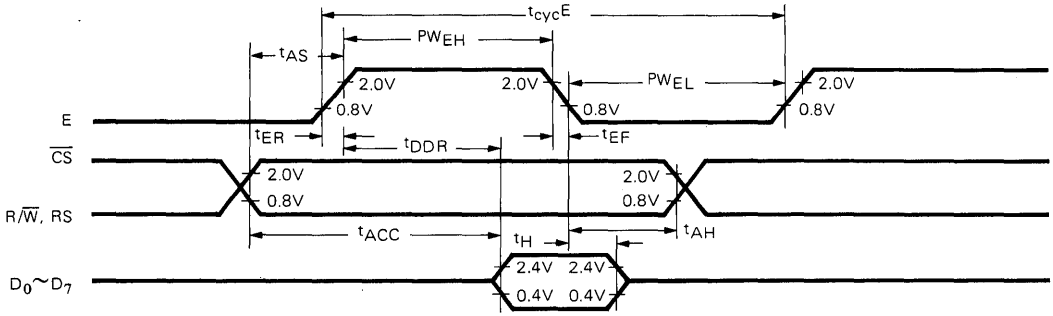


Figure 3. Read Sequence

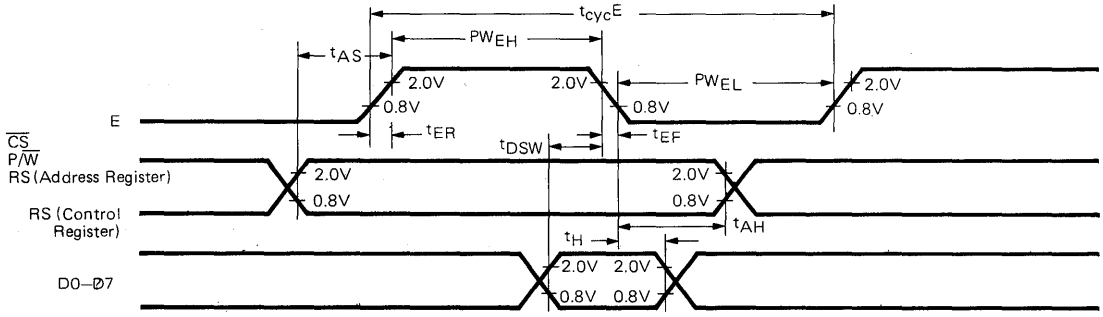
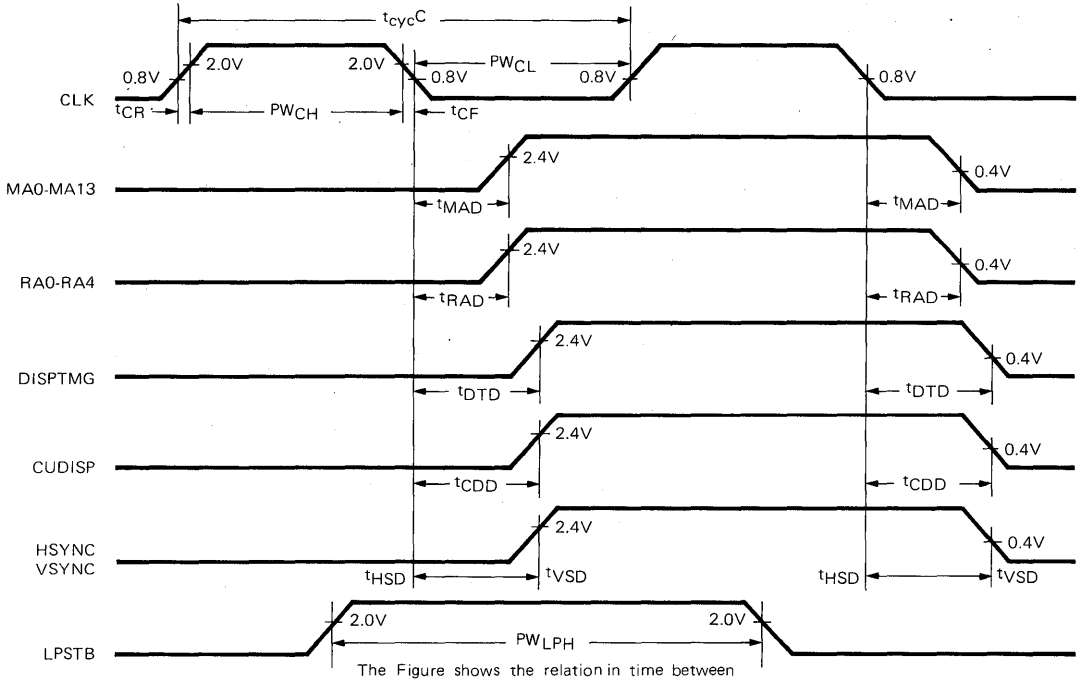


Figure 4. Write Sequence

CRTC SIGNAL TIMING

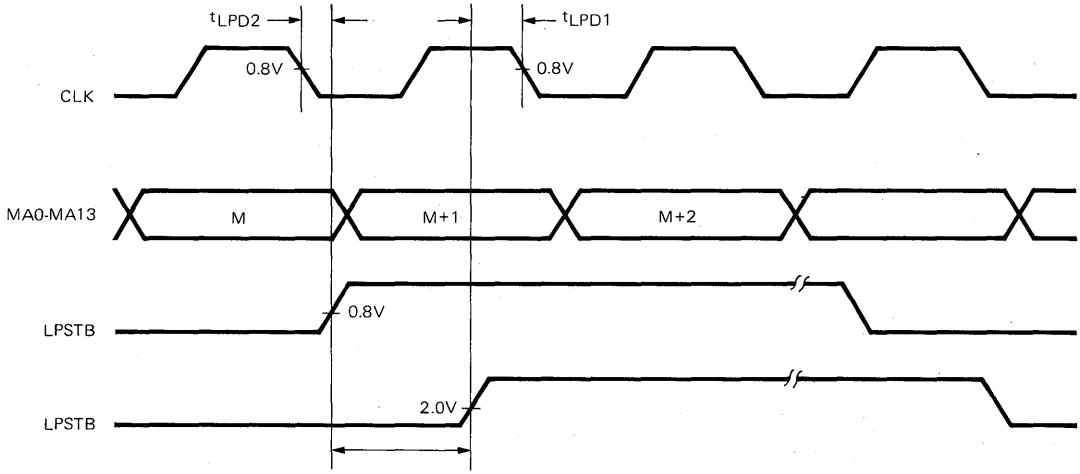
Item	Symbol	Min.	Typ.	Max.	Unit
Clock Cycle Time	$t_{cyc}C$	270	–	–	nS
Clock "High" Pulse Width	PW_{CH}	130	–	–	nS
Clock "Low" Pulse Width	PW_{CL}	130	–	–	nS
Rise and Fall Time for Clock Input	t_{Cr}, t_{Cf}	–	–	20	nS
Memory Address Delay Time	t_{MAD}	–	–	160	nS
Raster Address Delay Time	t_{RAD}	–	–	160	nS
DiSPTMG Delay Time	t_{DTD}	–	–	250	nS
CUDISP Delay Time	t_{CDD}	–	–	250	nS
Horizontal Sync Delay Time	t_{HSD}	–	–	200	nS
Vertical Sync Delay Time	t_{VSD}	–	–	250	nS
Light Pen Strobe Pulse Width	PW_{LPH}	60	–	–	nS
Light Pen Strobe	t_{LPD1}	–	–	70	nS
Uncertain Time of Acceptance	t_{LPD2}	–	–	0	nS

* See Fig. 5; Fig. 6



The Figure shows the relation in time between CLK signal and each output signal. Output sequence is shown in Application Notes.

Figure 5. CRTC Timing Chart



t_{LPD1}, t_{LPD2}: LPSTB's uncertain time of acceptance.

When LPSTB rises in this period. Display Memory Address "M+2" is set into the light pen register.

Figure 6. LPSTB Input Timing & Display Memory Address is Set Into the Light Pen Register.

Typical Crt Controller Application Block Diagram

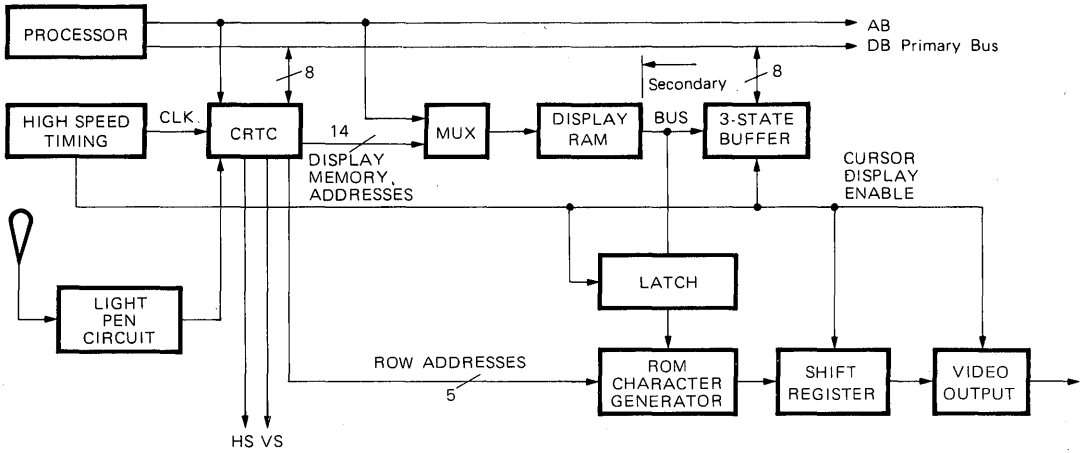


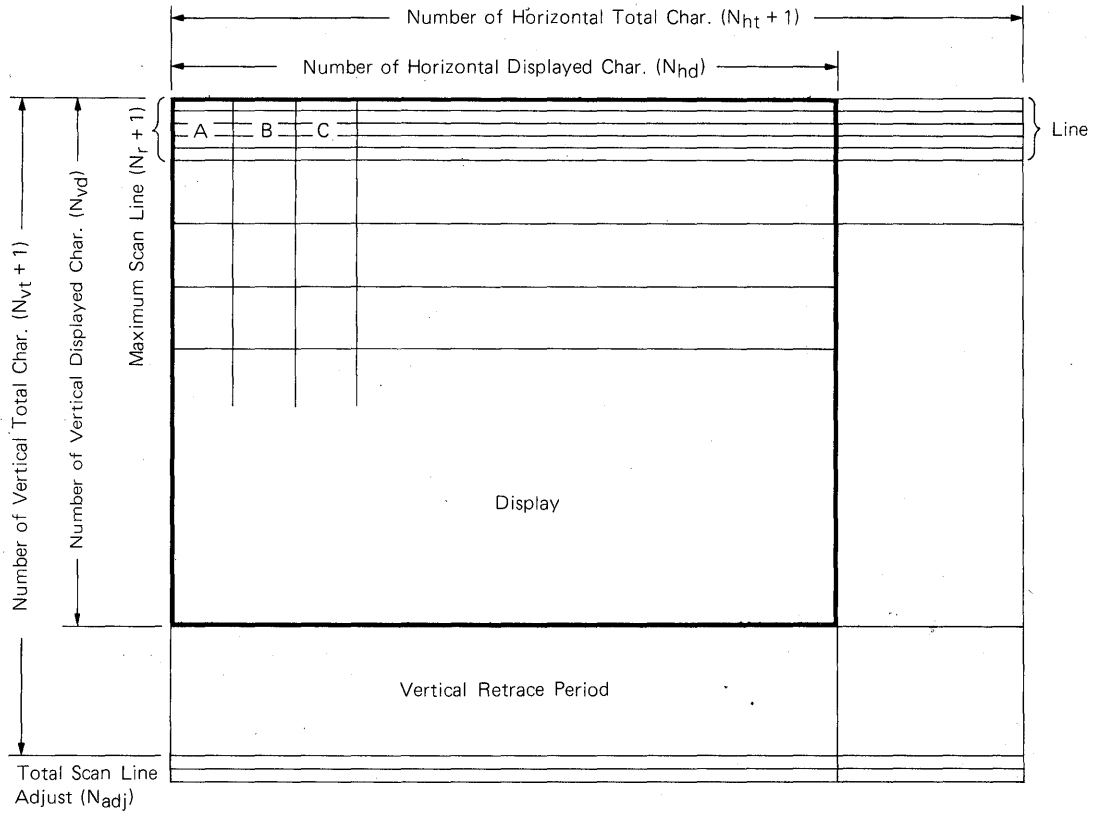
Figure 7. Typical CRT Controller Application

CRT Screen Format and Time Chart

REGISTERS PROGRAMMED VALUE

Register	Register Name	Specified Value	Programmed (Written) Value
R0	Horizontal Total	$N_{ht}+1$	N_{ht}
R1	Horizontal Displayed	N_{hd}	N_{hd}
R2	Horizontal Sync Position	$N_{hsp}+1$	N_{hsp}
R3	Sync Width	N_{vsw}, N_{hsw}	N_{vsw}, N_{hsw}
R4	Vertical Total	$N_{vt}+1$	N_{vt}
R5	Vertical Total Adjust	N_{adj}	N_{adj}
R6	Vertical Displayed	N_{vd}	N_{vd}
R7	Vertical Sync Position	$N_{vsp}+1$	N_{vsp}
R8	Interlace & Skew		
R9	Max. Raster Address	N_r+1/N_r+2	N_r
R10	Cursor Start Raster	N_{CSTART}	
R11	Cursor End Raster	N_{CEND}	
R12	Start Address (H)	0	
R13	Start Address (L)	0	
R14	Cursor (H)		
R15	Cursor (L)		
R16	Light Pen (H)		
R17	Light Pen L (L)		

SCREEN FORMAT



RESTRICTION ON PROGRAMMING INTERNAL REGISTER

(1) $0 < N_{hd} < N_{ht} + 1 \leqslant 256$

(2) $0 < N_{vd} < N_{vt} + 1 \leqslant 128$

(3) $0 \leqslant N_{hsp} \leqslant N_{ht}$

(4) $0 \leqslant N_{vsp} \leqslant N_{vt}$

(5) $0 \leqslant N_{CSTART} \leqslant N_{CEND} \leqslant N_r$ (Non-Interlace, Interlace Sync Mode)

$0 \leqslant N_{CSTART} \leqslant N_{CEND} \leqslant N_r + 1$ (Interlace Sync & Video Mode)

(6) $2 \leqslant N_r \leqslant 30$

(7) $3 \leqslant N_{ht}$ (Except Non-Interlace Mode)

$5 \leqslant N_{ht}$ (Non-Interlace Mode Only)

CRTC ADDRESSING FOR READING DISPLAY MEMORY

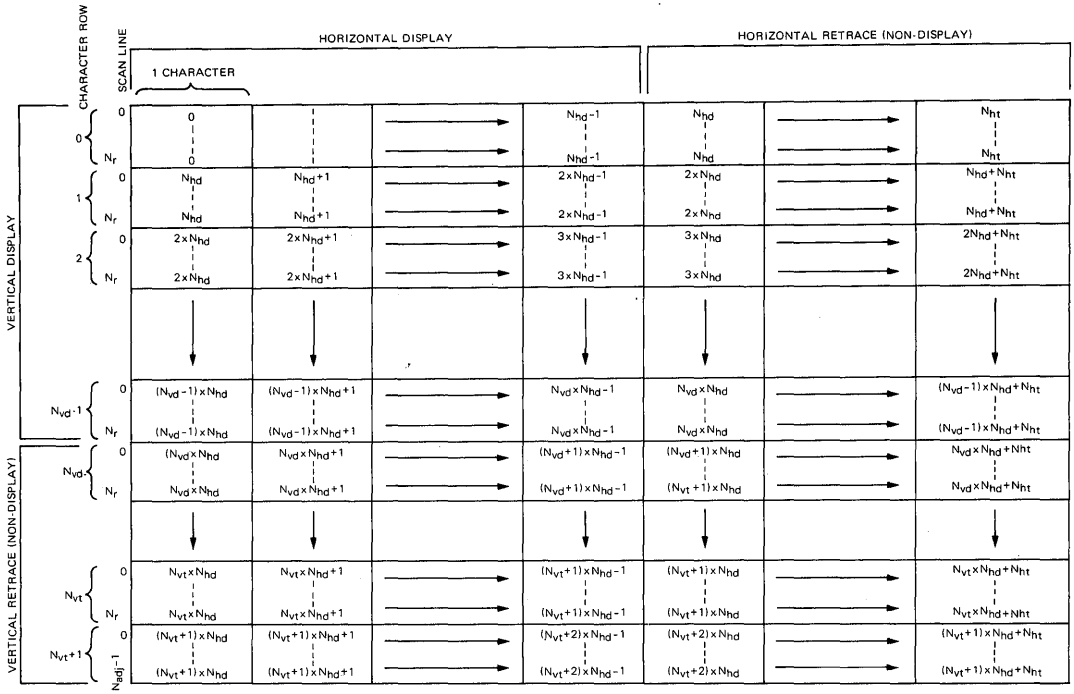


Figure 9. Display Memory Addressing (MA0-MA13) Stage Chart

Note: The initial MA is determined by the contents of state address register, R12/R13. Timing is shown for R12/R13 = 0. Only Non-Interlace-and Interlace Sync Modes are shown.

CRTC HORIZONTAL TIMING

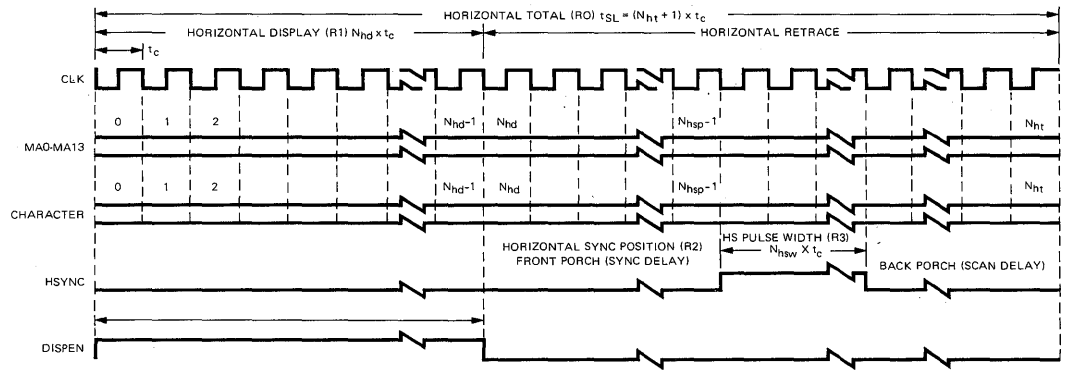


Figure 10. CRTC Horizontal Timing

CRTC VERTICAL TIMING

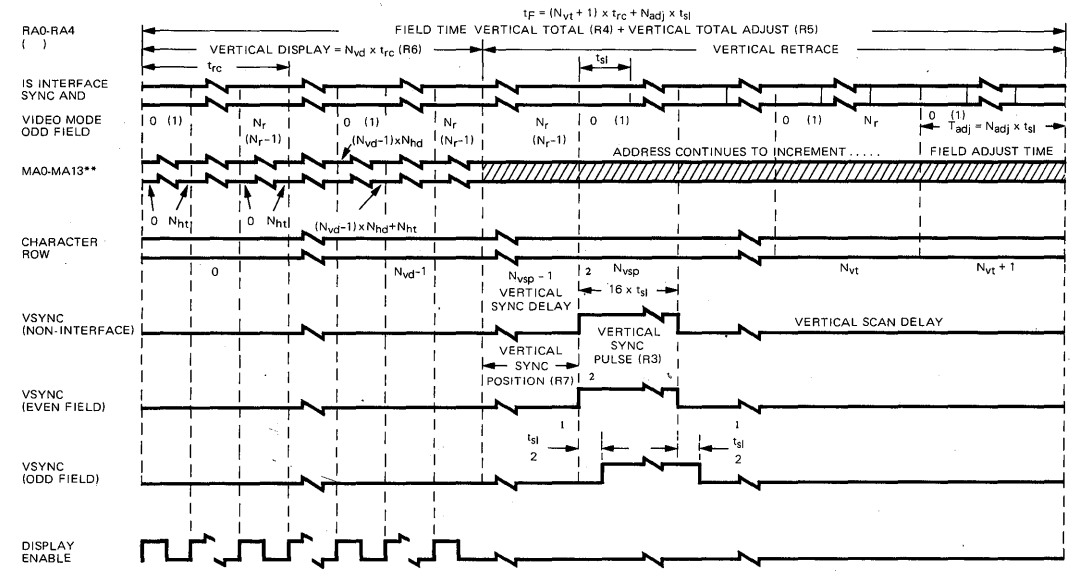


Figure 11. CRTC Vertical Timing

Notes: 1. The odd-field is offset ½ horizontal scan time.
2. Vertical sync pulse may be programmed from 1 to 16 scan line times.

CURSOR DISPLAY TIMING

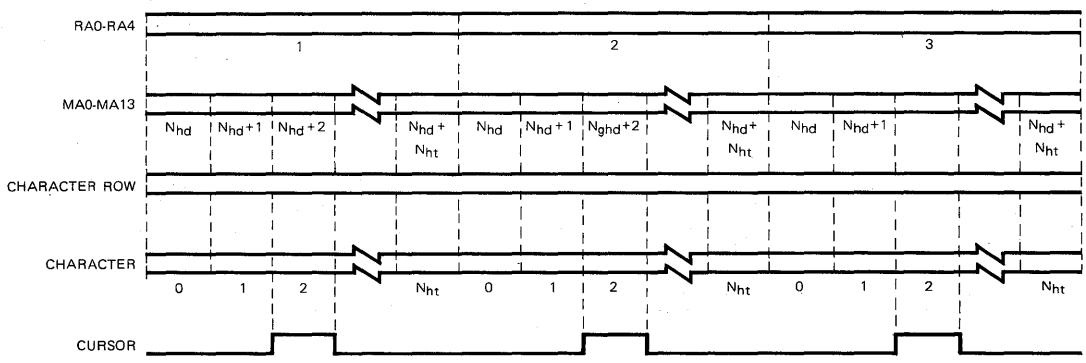


Figure 12. Cursor Timing

Notes: 1. Timing is shown for non-interlace and interlace modes.
2. Cursor Register = N_{hd} + 2.
3. Cursor start = 1.
4. Cursor End = 3.
5. R12/R13 = 0 for start address registers.

Example of Raster Scan Display

Fig. 13 shows an example where the same character is displayed in the non-interlace mode, interlace sync mode, and video mode.

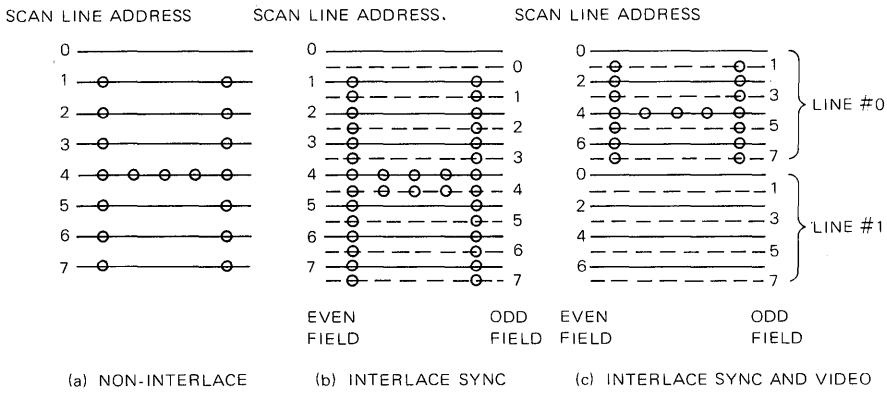


Figure 13. Interlace Control

Interface to Display Control Unit

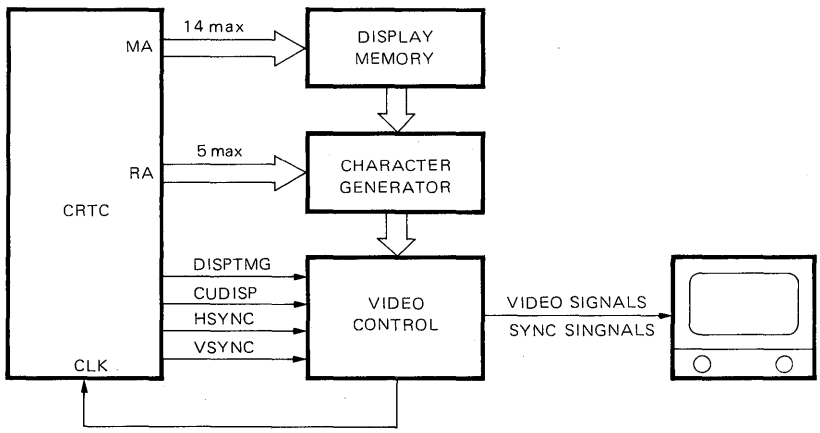


Figure 14. Interface to Display Control Unit

Fig. 14 shows the interface between the CRTC and display control unit. Display control unit is mainly composed of display Memory, Character Generator, and Video Control circuit. For display memory, 14 Memory Address lines (0-16383) max are provided and for character generator, 5 Raster Address lines (0-31) max are provided. For video control circuit, DISPTMG signal is used to control the blank period of video signal. CUDISP signal is used as video signal to display the cursor on the CRT screen. Moreover, HSYNC and VSYNC signals are used as drive signals respectively for CRT horizontal and vertical deflection circuits.

Outputs from video control circuit, (video signals and sync signals) are provided to CRT display unit to control the deflection and brightness of CRT, thus characters are displayed on the screen.

Circuitry Standard of Display Control Unit

Fig. 15. shows the detailed block diagram of the display control unit. This shows how to use CUDISP and DISPTMG signals. CUDISP and DISPTMG signals should be used being latched at least one time at external flip-flop F1 and F2. Flip-Flop F1 and F2 function to make one-character delay time so as to synchronize them with the video signal from parallel-serial converter. High-speed D-type flip-flop as TTL is used for this purpose. After being delayed at F1 and F2 DISPTMG signal is OR-ed with output from AND gate. By using this circuitry, blanking of horizontal and vertical retrace time is controlled and cursor video is mixed with character video signal.

Fig. 15 shows the example in the case that both display memory and CG can be accessed for horizontal one character time. Time chart for this case is shown in Fig. 18 This method is uded when a few characters need to be displayed in the horizontal direction on the screen.

When many characters are displayed in the horizontal direction on the screen and horizontal one-character time is so short that both display memory and CG cannot be accessed, the circuitry shown in Fig. 16 should be used. In this case, display memory output shall be latched and CG shall be accessed at the next cycle. The time chart in this case is shown in Fig. 19 CUDISP and DISPTMG signals should be provided after being delayed by one-character time by using skew bit of interlace & skew register (RS). Moreover, when there are some troubles about delay time of MA during horizontal one character time on high speed display operation, system shown in Fig. 17 should be adopted. The time chart in this case is shown in Fig. 20 Character video signal is delayed for two-character time because each MA output and display memory outputs are latched and are made to be in phase with CUDISP and DISPTMG signals by delaying for two-character time. Table 5 shows the circuitry selection standard of display units.

Table 5. Circuitry Standard of Display Control Unit

Case	Relation among t_{CH}, RM and CG	Block Diagram	Interlace & Skew Register Bit Programming			
			C1	C0	D1	D0
1	$t_{CH} >$ RM Access + CG Access + t_{MAD}	Fig. 15, 18	0	0	0	0
2	RM Access + CG Accwss + $t_{MAD} \geq t_{CH} >$ RM Access + t_{MAD}	Fig. 16, 19	0	1	0	1
3	RM Access + $t_{MAD} \geq t_{CH} >$ RM Access	Fig. 17, 20	1	0	1	0

t_{CH}: CHCP Period: t_{MAD}: MA Delay

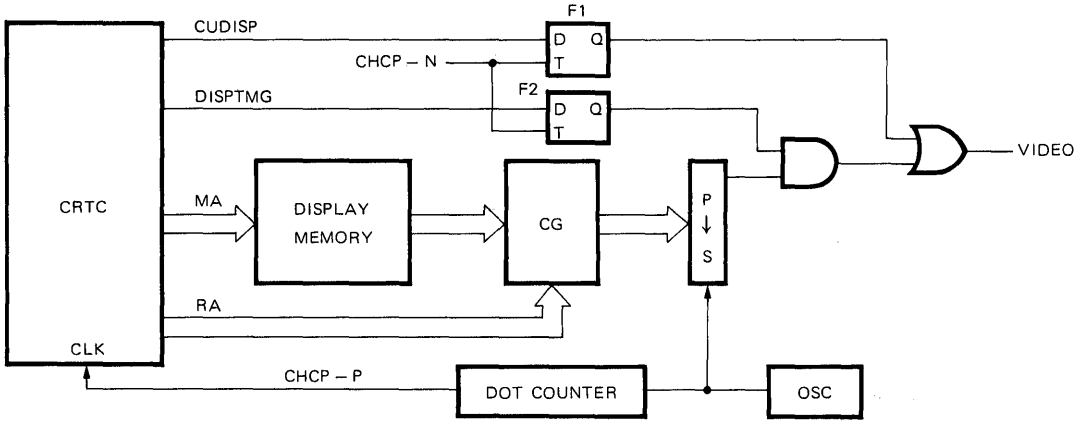


Figure 15. Display Control Unit (1)

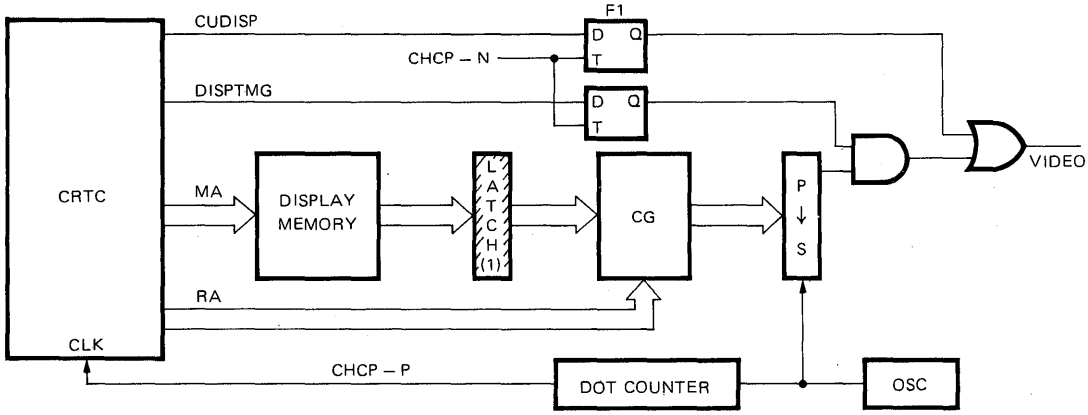


Figure 16. Display Control Unit (2)

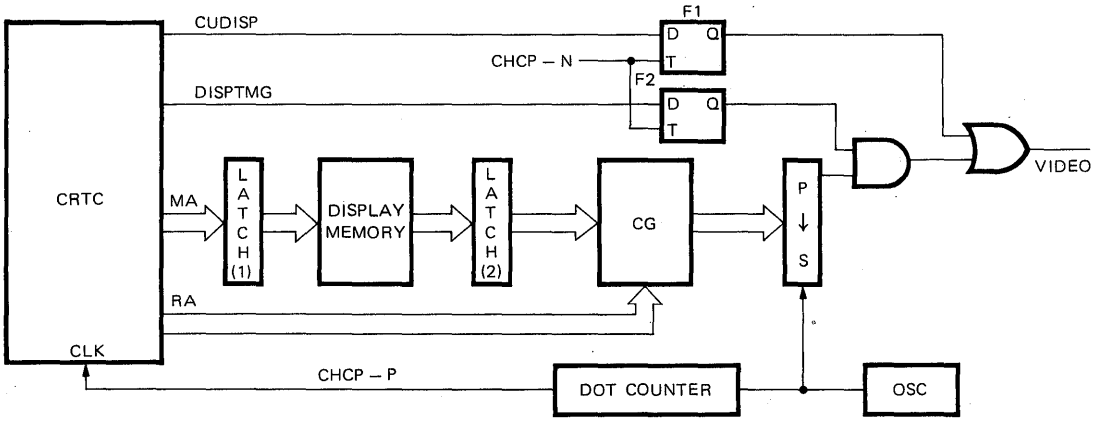


Figure 17. Display Control Unit (For high-speed display operation) (3)

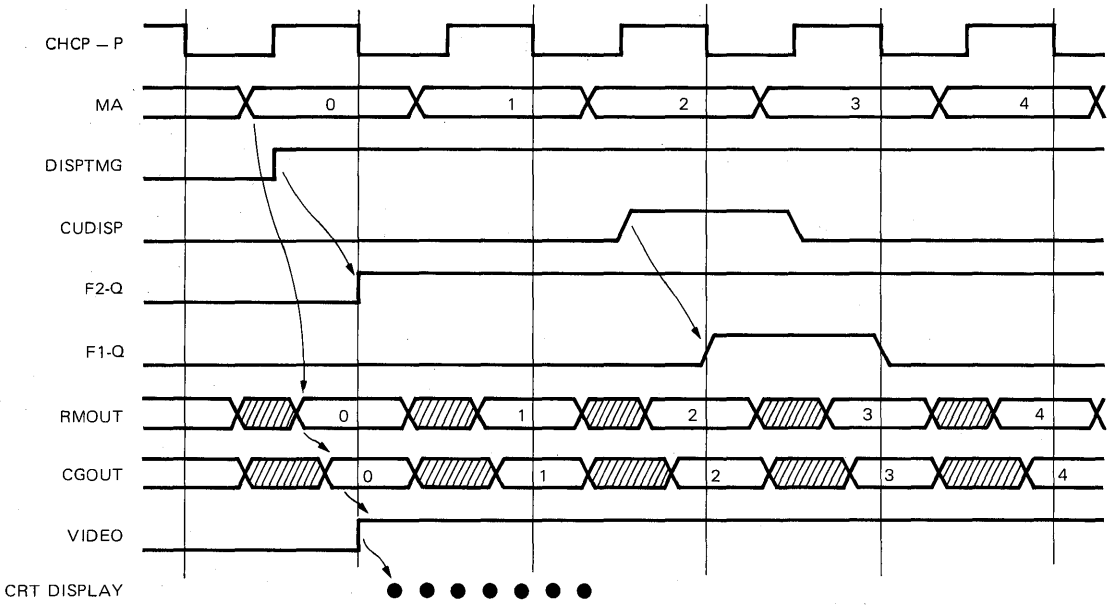


Figure 18. Time Chart of display Control Unit (1)

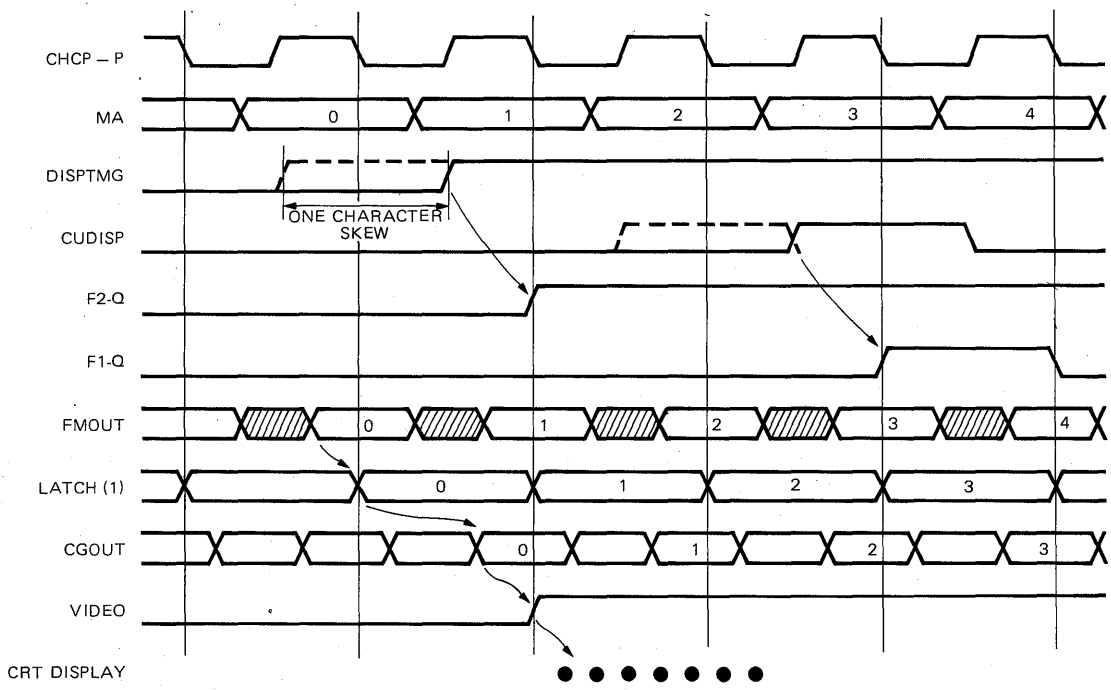


Figure 19. Time Chart of Display Control Unit (2)

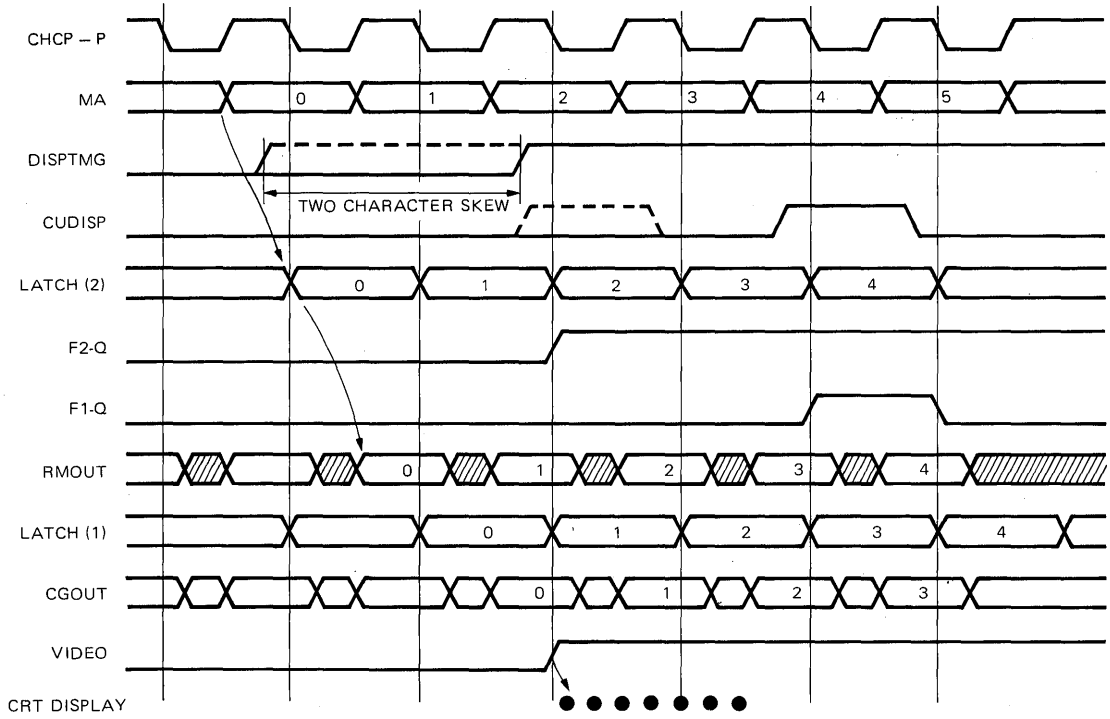


Figure 20. Time Chart of Display Unit (3)

How to Decide Parameters on the CRTC

Before the determination of parameters on the CRTC and the dot frequency of crystal, we must check the Specification of CRT Display Unit (Monitor) and the Screen Format. The output signal timing of CRTC, must be in the specification of Monitor to reach the formal display. (Such as DISPTMG, HSYNC, VSYNC.). Screen fromat includes:

(1) Horizontal display characters column number. (N_{hd})
(2) Vertical display row number. (N_{vd})
(3) Horizontal dot numbers per character. (Dot counter ($\div N\alpha$)).
(4) Vertical raster lines per row. ($N_r + 1$)

Example: for non-interlace mode one frame = 60 Hz
then one raster line frequency
= 60Hz x $[(N_{vt} + 1)\ (N_r + 1) + N_{adj}]$
CLK frequency of CRTC = raster line frequency x $(N_{ht} + 1)$

dot frequency of crystal = $N\alpha$ x CLK frequency of CRTC
= 60Hz x $[(N_{vt} + 1)\ (N_r + 1) + N_{adj}] \times [N_{ht} + 1] \times N\alpha$

* Relation between R0-R7 is in Figure 21.

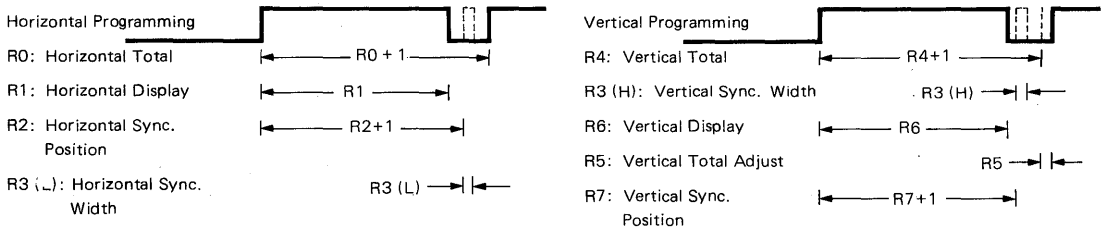


Figure 21.

Pin Description

Function	Name	Symbol	Pin No.
Processor Interface	Data Bus	D0 – D7	33, 32, 31, 30 29, 28, 27, 26
	Enable	E	23
	Chip Select	$\overline{CS}$	25
	Register Select	RS	24
	Read/Write	R/$\overline{W}$	22
CRT Control	Vertical Sync	VSYNC	40
	Horizontal Sync	HSYNC	39
	Display Enable	DISPTMG	18
Reading Display Memory/ Character Generator Addressing	Reading Memory Addresses	MA0-MA13	4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17
	Raster Addresses	RA0-RA4	38, 37, 36, 35, 34
Other Pins	Cursor	CUDISP	19
	Clock	CLK	21
	Light Pen Strobe	LPSTB	3
	Power	$V_{CC}^{(+)}$ $V_{SS}^{(-)}$	20, 1
	Reset	$\overline{RES}$	2

PROCESSOR INTERFACE

The CRTC interfaces to a processor bus on the bidirectional data bus (D0-D7) using $\overline{CS}$. RS. E. and R/$\overline{W}$ as control signals.

Data Bus (D0-D7)
The bidirectional data lines (D0-D7) allow data transfers between the CRTC internal register file and the processor. Data bus output drivers are 3-state buffers which remain in the high impedance state except when the processor performs a CRTC read operation.

Enable (E)
The Enable pin is a high impedance TTL/MOS compatible input which enables the data bus input/output buffers and clocks data to and from the CRTC. This signal is usually derived from the processor clock and the high to low transition is the active edge.

Chip Select ($\overline{CS}$)
The $\overline{CS}$ line is a high impedance TTL/MOS compatible input which selects the CRTC, when low, to read or write the internal Register File. This signal should only be active when there is a valid stable address being decoded from the processor.

Register Select (RS)
The RS line is a high impedance TTL/MOS compatible input which selects either the Address Register (RS = "o") or one of the Data Registers (RS = "1") of the internal Register File.

Read/Write (R/$\overline{W}$)
The R/$\overline{W}$ line is a high impedance TTL/MOS compatible input which determines whether the internal Register File gets written or read. A write is active at low ("0").

CRT CONTROL

The CRTC provides horizontal sync (HS), vertical sync (VS), and Display Enable (DISPTMG) signals.

Vertical Sync (V SYNC)
The TTL compatible output is an active high signal which drives the monitor directly or is fed to Video Processing Logic for composite signal generation. This signal determines the vertical position of the displayed text.

Horizontal Sync (H SYNC)
This TTL compatible output is an active high signal which drives the monitor directly or is fed to Video Processing Logic for composite generation. This signal determines the horizontal position of the displayed text.

Display Enable (DISPTMG)
This TTL compatible output is an active high signal which indicates the CRTC is providing addressing in the active display area.

READING DISPLAY/CHARACTER GENERATOR ADDRESSING

The CRTC provides Memory Addresses (MA0-MA13) to scan the display RAM. Also provided are Raster Addresses (RA0-RA4) for the character ROM.

Reading Memory Addresses (MA0-MA13)
These 14 outputs are used to read the display memory.

Raster Addresses (RA0-RA4)
These 5 outputs from the internal Raster Counter address the character ROM for the row of a character.

OTHER PINS

Cursor (CUDISP)
This output signal indicates the cursor display signal sent to the video processing logic to display in the proper area.

Clock (CLK)
CLK, TTL/MOS compatible input is used to synchronize all CRT control signals. An external dot counter is used to derive this signal which is usually the character rate in an alphanumeric CRT. The active transition is high to low.

Light Pen Strobe (LPSTB)
This high impedance TTL/MOS compatible input latches the current display memory address in the register file. Latching is on the low to high edge and is synchronized internally to character clock.

V_{CC}, Gnd (V_{CC}, V_{SS}) Power Supply Pins.
Reset ($\overline{RES}$)
The $\overline{RES}$ input is used to reset the CRTC. An input low level on $\overline{RES}$ forces CRTC into the following status:

(a) All the counters in CRTC are cleared and the device stops the display operation.
(b) All the outputs go to low level.
(c) Control registers in CRTC remain unchanged.

This signal is different from other MC 6800 family in the following functions:

(a) $\overline{RES}$ signal has capability of reset function only when LPSTB is at low level.
(b) The CRTC starts the display operation immediately after the release of $\overline{RES}$ signal.

CRTC INTERNAL REGISTER ASSIGNMENT

Table 1. CRTC Internal Register

$\overline{CS}$	RS	Address Register 4	3	2	1	0	Register #	Register File	Program Unit	Read	Write	Number of Bits 7	6	5	4	3	2	1	0
1	X	X	X	X	X	X	X	–	–	–	–								
0	0	X	X	X	X	X	AR	Address Register	–	No	Yes								
0	1	0	0	0	0	0	R0	Horizontal Total *	Char.	No	Yes								
0	1	0	0	0	0	1	R1	Horizontal Displayed	Char.	No	Yes								
0	1	0	0	0	1	0	R2	H. Sync Position*	Char.	No	Yes								
0	1	0	0	0	1	1	R3	Sync Width	V-Raster H-Char.	No	Yes	V1	V1	V1	V1	H	H	H	H
0	1	0	0	1	0	0	R4	Vertical Total *	Char. Row	No	Yes								
0	1	0	0	1	0	1	R5	V. Total Adjust	Scan Line	No	Yes								
0	1	0	0	1	1	0	R6	Vertical Displayed	Char. Row	No	Yes								
0	1	0	0	1	1	1	R7	V. Sync Position*	Char. Row	No	Yes								
0	1	0	1	0	0	0	R8	Interface Mode and Skew	–	No	Yes	C_1	C_0	D_1	D_0			I_1	I_0
0	1	0	1	0	0	1	R9	Max Scan Line Address	Scan Line	No	Yes								
0	1	0	1	0	1	0	R10	Cursor Start Raster	Scan Line	No	Yes		B	P					
0	1	0	1	0	1	1	R11	Cursor End Raster	Scan Line	No	Yes								
0	1	0	1	1	0	0	R12	Start Address (H)	–	Yes	Yes	0	0						
0	1	0	1	1	0	1	R13	Start Address (L)	–	Yes	Yes								
0	1	0	1	1	1	0	R14	Cursor (H)	–	Yes	Yes	0	0						
0	1	0	1	1	1	1	R15	Cursor (L)	–	Yes	Yes								
0	1	1	0	0	0	0	R16	Light Pen (H)	–	Yes	No	0	0						
0	1	1	0	0	0	1	R17	Light Pen (L)	–	Yes	No								

Table 1. Shows The Register File In CRTC, The Registers Marked* (Written Value) = (Specified Value) – 1

REGISTER DESCRIPTION

Address Register (AR)

The Address Register is a 5-bit write-only register used as an "indirect" or "pointer" register. Its contents are the address of one of the other 18 registers in the file. When RS and $\overline{CS}$ are low, the Address Register itself is addressed. When RS is high, the register file is accessed. (see Table 1).

Horizontal Total Register (R0)

This 8 bit Register determines the horizontal frequency of H Sync output. It is the total of displayed plus non-displayed character timeunits minus one.

Horizontal Displayed Register (R1)

This 8 bit register determines the number of displayed characters per horizontal line.

Horizontal Sync Position Register (R2)

This 8 bit register determines the horizontal sync position on the horizontal line.

Sync Width Register (R3)

V	V	V	V	H	H	H	H

This 8 bit write-only register determines the width of the vertical sync (VS) pulse and the horizontal sync (HS) pulse.

The HS pulse width may be programmed from 1-to-15 character clock periods. The VS pulse width may be programmed from 1-to-16 Raster scan lines. (see Table 2)

Vertical Total Register (R4) and Vertical Total Adjust Register (R5)

The vertical frequency of VSYNC is determined by both R4 and R5. The calculated number of character line times is usually an integer plus a fraction to get exactly a 50 or 60 Hz vertical refresh rate. The integer number of Character line times minus one is programmed in the 7 bit write-only Vertical Total Register, the fraction is programmed in the 5 bit write-only Vertical Scan Adjust Register as a number of scan line times.

Vertical Displayed Register (R6)

This 7-bit write-only register specifies the number of displayed character rows on the CRT screen, and is programmed in character row times. Any number smaller than the contents of R4 may be programmed into R6.

Vertical Sync Position (R7)

This 7-bit write-only register controls the position of vertical sync with respect to the reference. It is programmed in character row times. Any number equal to or less than the vertical total (R4) may be used.

Interlace Mode and Skew Register (R8)

C_1	C_0	D_1	D_0			I_1	I_0

This is a register used to program raster scan mode and skew of CUDISP signal and DISPTMG signal. In the non-interlace mode, the rasters of even number field and odd number field are scan duplicated. In the interlace sync mode, the rasters of odd number field are scanned in the middle of even number field. Thus, the same character pattern is displayed in both fields. In the interlace sync and video mode, the raster scan method is the same as the interlace sync mode, but it is controlled to display different character patterns in two fields. Skew function is used to delay the output timing of CUDISP and DISPTMG signals such that they are synchronized with serial video output signal. This is due to the time delay from display memory data to serial output character pattern. (see Table 3).

Table 2. Sync Width Register

VSW				Pulse Width Unit: H
2^7	2^6	2^5	2^4	
0	0	0	0	16H
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

H: Raster Period

HSW				Pulse Width Unit: CH
2^3	2^2	2^1	2^0	
0	0	0	0	No Used
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

CH: Character Clock Period

Table 3. Interlace Mode and Skew Register

Interlace Mode (2^1, 2^0)	I_1	I_0	Raster Scan Mode
	0	0	Non-Interlace Mode
	1	0	Non-Interlace Mode
	0	1	Interlace Sync Mode
	1	1	Interlace Sync & Video Mode
Cursor Skew Bit (2^7, 2^6)	C_1	C_0	CUDISP Signal
	0	0	Non-Skew
	0	1	One-Character Skew
	1	0	Two-Character Skew
	1	1	Non-Output
DISPTMG Skew Bit (2^5, 2^4)	D_1	D_0	DISPTMG Signal
	0	0	Non-Skew
	0	1	One-Character Skew
	1	0	Two-Character Skew
	1	1	Non-Ouptut

Maximum Raster Address Register (R9)

This is a register used to program maximum raster address within 5-bit. This register defines total number of rasters per character including space. This register is programmed as follows.

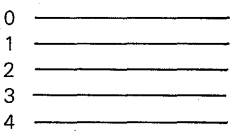
For Non-interlace Mode, Interlace Sync Mode

When total number of rasters is RN, (RN-1) shall be programmed.

For Interlace Sync & Video Mode

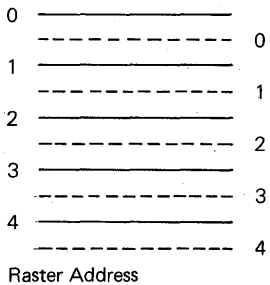
When total number of rasters in RN, (RN-2) shall be programmed.

Non-Interlace Mode



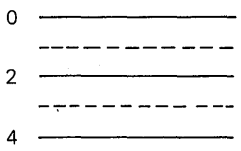
Total Number of Rasters 5
Programmed Value $N_r = 4$
(The same as displayed total number of rasters)

Interlace Sync Mode



Total Number of Raster 5
Programmed Value $N_r = 4$
(In the interlace sync mode, total number of rasters in both the even and odd fields is ten. On programming, half of it is defined as total number of rasters).

Interlace Sync & Video Mode



Total Number of Rasters 5
Programmed Value $N_r = 3$
(Total number of rasters is displayed in the even field and the odd field)

Cursor Start Raster Register (R10)

	B	P					

This is a register used to program the cursor start raster address by lower 5-bit (2^0-2^4) and the cursor display mode higher 2-bit (2^5, 2^6). (see Table-4).

Table 4. Cursor Display Mode

Cursor Display Mode	B	P	Cursor Display Mode
(2^6, 2^5)	0	0	Non-blink
	0	1	Cursor Non-display
	1	0	Blink, 16 Field Period
	1	1	Blink, 32 Field Period

Cursor End Raster Register (R11)
This is a register used to program to cursor end raster address.

Start Address Register (R12, R13)
These are used to program the first address of refresh memory to read out. Paging and Scrolling is easily performed using this register. This register can be read but the higher 2-bit (2^6, 2^7) of R12 are always "0".

Cursor Register (R14, R15)
These two read/write registers store the cursor location. The higher 2-bit (2^6, 2^7) of R14 are always "0".

Light Pen Register (R16, R17)
These read-only registers are used to catch the detection address of the light pen. The higher 2-bit (2^6, 2^7) of R16 are always "0". Its value needs to be corrected by software because there is time delay from address output of the CRTC to signal input LPSTB pin of the CRTC in the process raster is lit after address output and light pen detects it.

CRTC Register Comparison Table

NON-INTERLACE

Register	UM6845R MC6845 MC6845*1	MC6845R HD6845R	UM6845 HD6845S	UM6845E	SYS6545-1
R0 Htotal	Total-1	Total-1	Total-1	Total-1	Total-1
R1 Hdisp	Actual	Actual	Actual	Actual	Actual
R2 Hsync	Actual	Actual	Actual	Actual	Actual
R3 Sync Width	Horizontal (& Vertical *1)	Horizontal	Horizontal & Vertical	Horizontal & Vertical	Horizontal & Vertical
R4 Vtotal	Total-1	Total-1	Total-1	Total-1	Total-1
R5 Vtotal Adjustment	Any Value	Any Value	Any Value	Any Value	Any Value Except R5
R6 Vdisp	Any Value <R4	Any Value <R4	Any Value <R4	Any Value <R4	Any Value <R4
R7 Vsync	Actual-1	Actual-1	Actual-1	Actual-1	Actual-1
R8 B0-1	Interlace	Interlace	Interlace	Interlace	Interlace
Mode Select B2	–	–	–	Row/Column or Binary Addr.	Row/Column or Binary Addr.
B3	–	–	–	Shared or Transparent Addr.	Shared or Transparent Addr.
B4	(Display Enable Skew *1)	–	Display Enable Skew	Display Enable Skew	Display Enable Skew
B5	(Display Enable Skew *1)	–	Display Enable Skew	Cursor Skew	Cursor Skew
B6	(Cursor Skew *1)	–	Cursor Skew	RA4/	RA4/
B7	(Cursor Skew *1)	–	Cursor Skew	Transparent	Transparent
R9 Scan Lines	Total-1	Total-1	Total-1	Total-1	Total-1
R10 Cursor Start	Actual	Actual	Actual	Actual	Actual
R11 Cursor End	Actual	Actual	Actual	Actual	Actual
R12/R13 Display Addr.	Write Only Read/Write (MC6845 & *1)	Read/Write	Read/Write	Write Only	Write Only
R14/R15 Cursor Position	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
R16/R17 Position	Read Only	Read Only	Read Only	Read Only	Read Only
R18/R19 Update Addr. Register	N/A	N/A	N/A	Transparent Mode Only	Transparent Mode Only
R31 Dummy Register	N/A	N/A	N/A	Transparent Mode Only	Transparent Mode Only
Status Register	Yes (UM6845R)	No	No	Yes	Yes

CRTC Register Comparison Table (Continued)

INTERLACE SYNC

Register	UM6845R MC6845 MC6845*1	MC6845R HD6845R	UM6845 HD6845S	UM6845E	SYS6545-1
R0 Htotal	Total-1 = Odd or Even	Total-1 = Odd	Total-1 = Odd	Total-1 = Odd or Even	Total-1 = Odd

INTERALACE SYNC AND VIDEO

R4 Vtotal	Total-1	Total-1	Total-1	Total-1	Total/2-1
R6 Vdisp	Total	Total/2	Total	Total	Total/2
R7 Vsync	Actual-1	Actual-1	Actual-1	Actual-1	Actual/2
R9 Scan Lines	Total-1 Odd/Even	Total-1 Only Even	Total-1 Odd/Even	Total-1 Odd/Even	Total-1 Odd/Even
R10 Cursor Start	Odd/Even	Both Odd or	Odd/Even	Odd/Even	Odd/Even
R11 Cursor End	Odd/Even	Both Even	Odd/Even	Odd/Even	Odd/Even
Cclk	2.5 MHz	2.5 MHz	3.7 MHz	3.7 MHz	2.5 MHz

Ordering Information

Part Number	CPU Clock Rate	Package
UM6845	1MHz	Plastic
UM6845A	1.5MHz	Plastic
UM6845B	2MHz	Plastic

UM6845R/UM6845RA/UM6845RB

CRT Controller

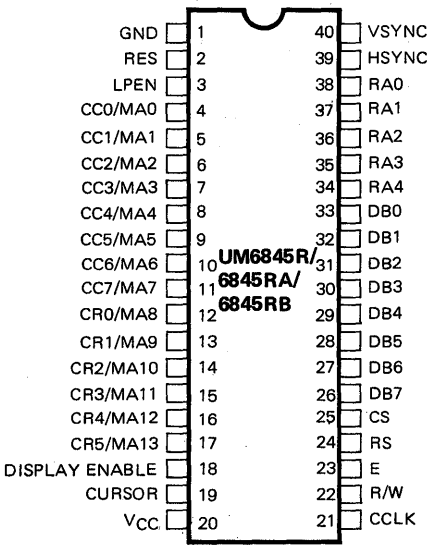
Features

- Single + 5 volt (±5%) power supply
- Alphanumeric and limited graphics capabilities
- Fully programmable display (rows, columns, blanking, etc.)
- Interlaced or non-interlaced scan
- 50/60 Hz operation
- Fully programmable cursor
- External light pen capability
- Capable of addressing up to 16K character Video Display RAM.
- No DMA required
- Compatible with SY6845R
- Straight-binary addressing for Video Display RAM

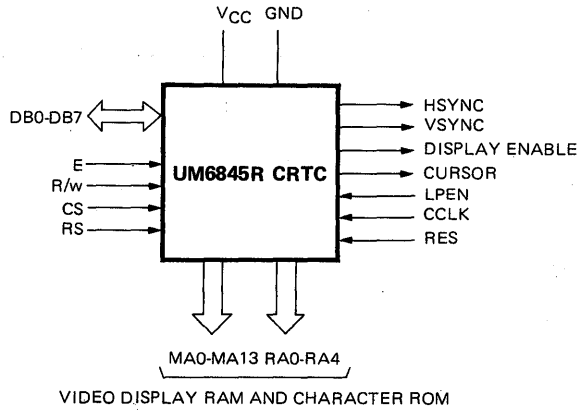
General Description

The UM6845R is a CRT Controller intended to provide capability for interfacing any microprocessor family to CRT or TV-type raster scan displays. A unique feature is the inclusion of several modes of operation, so that the system designer can configure the system with a wide assortment of techniques.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Supply Voltage, V_{CC} . . . . . −0.3V to + 7.0V
Input/Output Voltage, V_{IN} . . . . . −0.3V to + 7.0V
Operating Temperature, T_{OP} . . . . . 0°C to 70°C
Storage Temperature, T_{STG} . . . . . −55°C to 150°C
Notice:
All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

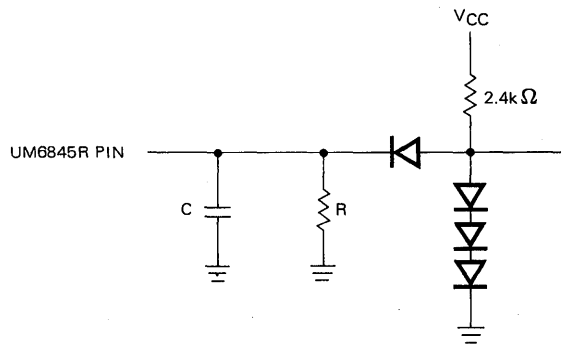
D.C. Electrical Characteristics

(V_{CC} = 5.0V ± 5%, T_A = 0 − 70°C, unless otherwise noted)

Symbol	Characteristics	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	2.0		V_{CC}	V
V_{IL}	Input Low Voltage	−0.3		0.8	V
I_{IN}	Input Leakage (ϕ2, R/$\overline{w}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK)	−		2.5	μA
I_{TSI}	Three-State Input Leakage (DB0-DB7) V_{IN} = 0.4 to 2.4V	−10.0		+10.0	μA
V_{OH}	Output High Voltage I_{LOAD} = −205 μA (DB0-DB7) I_{LOAD} = −100 μA (all others)	2.4		−	V
V_{OL}	Output Low Voltage I_{LOAD} = 1.6mA	−		0.4	V
P_D	Power Dissipation	−	325	650	mW
C_{IN}	Input Capacitance ϕ2, R/$\overline{w}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK DB0-DB7	− −		10.0 12.5	pF pF
C_{OUT}	Output Capacitance	−		10.0	pF

CRT Controller

TEST LOAD

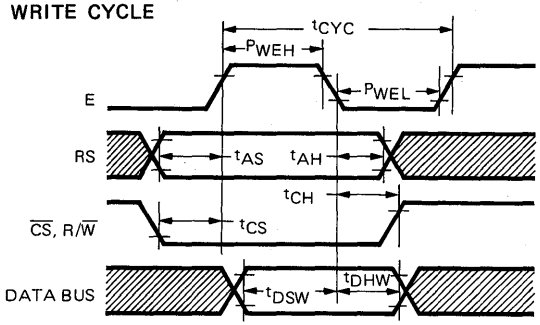


R = 11KΩ FOR DB_0-DB_7
R = 24KΩ FOR ALL OTHER OUTPUTS
C = 130pF TOTAL FOR D_0-D_7
C = 30 pF ALL OTHER OUTPUTS

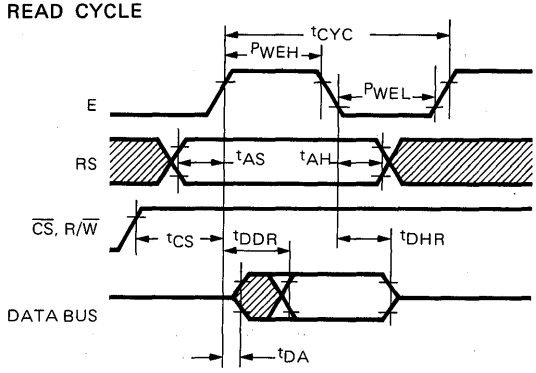
A.C. Electrical Characteristics

MPU BUS INFERFACE CHARACTERISTICS

WRITE CYCLE



READ CYCLE



WRITE TIMING CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0 – 70°C, unless otherwise noted)

Symbol	Characteristics	UM6845R		UM6845RA		UM6845RB		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	–	0.5	–	0.33	–	μs
P_{WEH}	E Pulse Width, High	440	–	200	–	150	–	ns
P_{WEL}	E Pulse Width, Low	420	–	190	–	140	–	ns
t_{AS}	Address Set-Up Time	80	–	40	–	30	–	ns
t_{AH}	Address Hold Time	0	–	0	–	0	–	ns
t_{CS}	R/$\overline{W}$, $\overline{CS}$ Set-Up Time	80	–	40	–	30	–	ns
t_{CH}	R/$\overline{W}$, $\overline{CS}$ Hold Time	0	–	0	–	0	–	ns
t_{DSW}	Data Bus Set-Up Time	165	–	60	–	60	–	ns
t_{DHW}	Data Bus Hold Time	10	–	10	–	10	–	ns

(t_r and t_f = 10 to 30 ns)

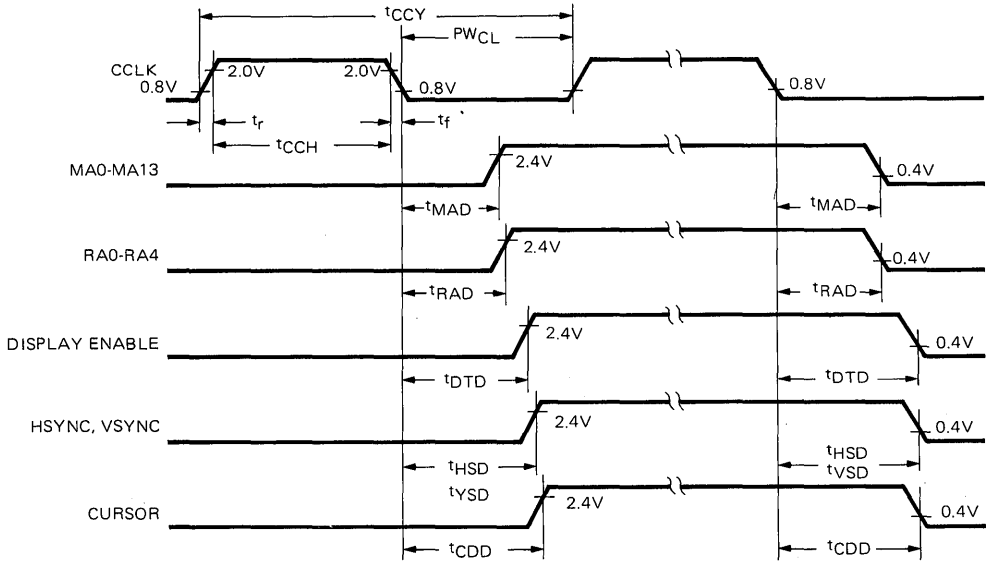
READ TIMING CHARACTERISTICS . (V_{CC} = 5.0V ± 5%, T_A = 0 – 70°C, unless otherwise noted)

Symbol	Characteristics	UM6845R		UM6845RA		UM6845RB		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	–	0.5	–	0.33	–	μs
P_{WEH}	E Pulse Width, High	440	–	200	–	150	–	ns
P_{WEL}	E Pulse Width, Low	420	–	190	–	140	–	ns
t_{AS}	Address Set-Up Time	80	–	40	–	30	–	ns
t_{AH}	Address Hold Time	0	–	0	–	0	–	ns
t_{CS}	R/$\overline{W}$, $\overline{CS}$ Set-Up Time	80	–	40	–	30	–	ns
t_{DDR}	Read Access Time (Valid Data)	–	290	–	150	–	100	ns
t_{DHR}	Read Hold Time	20	60	20	60	20	60	ns
t_{DA}	Data Bus Active Time (Invalid Data)	40	–	40	–	40	–	ns

(t_r and t_f = 10 to 30 ns)

MEMORY AND VIDEO INTERFACE CHARACTERISTICS

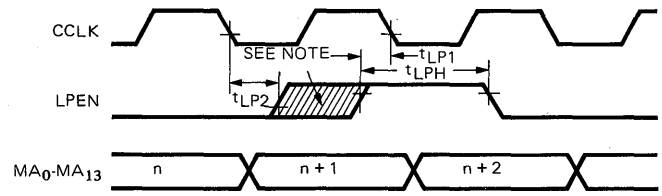
(V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)



Symbol	Parameter	Min.	Typ.	Max.	Units
T_{CCH}	Minimum Clock Pulse Width, High	200			ns
T_{CCY}	Clock Frequency			2.5	MHz
T_r, t_f	Rise and Fall Time for Clock Input			20	ns
t_{MAD}	Memory Address Delay Time		100	160	ns
t_{RAD}	Raster Address Delay Time		100	160	ns
t_{DTD}	Display Timing Delay Time		160	300	ns
t_{HSD}	Horizontal Sync Delay Time		160	300	ns
t_{VSD}	Vertical Sync Delay Time		160	300	ns
t_{CDD}	Cursor Display Timing Delay Time		160	300	ns

LIGHT PEN STROBE TIMING

NOTE:
"Safe" time position for LPEN positive edge to cause address n+2 to load into Light Pen Register. t_{LP2} and t_{LP1} are time positions causing uncertain results.



Symbol	Characteristics	UM6845R		UM6845RA		UM6845RB		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{LPH}	LPEN Strobe Width	100	–	100	–	100	–	ns
t_{LP1}	LPEN to CCLK Delay	–	120	–	120	–	120	ns
t_{LP2}	CCLK to LPEN Delay	–	0	–	0	–	0	ns

t_r and t_f = 20 ns (max.)

Pin Description

MPU INTERFACE SIGNAL DESCRIPTION

E (Enable)
The enable signal is the system input and is used to trigger all data transfers between the system microprocessor and the UM6845R. Since there is no maximum limit to the allowable E cycle time, it is not necessary for it to be a continuous clock. This capability permits the UM6845R to be easily interfaced to non-6500-compatible microprocessors.

R/$\overline{W}$ (Read/Write)
The R/$\overline{W}$ signal is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the UM6845R; a low on the R/$\overline{W}$ pin allows a write to the UM6845R

$\overline{CS}$ (Chip Select)
The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The UM6845R is selected when $\overline{CS}$ is low.

RS (Register Select)
The Register Select input is used to access internal registers, A low on this pin permits writes into the Address Register and reads from the Status Register. The contents of the Address Register is the identity of the register accessed when RS is high.

DB_0–DB_7 (Data Bus)
The DB_0–DB_7 pins are the eight data lines used for transfer of data between the processor and the UM6845R. These lines are bi-directional and are normally high-impedance except during read/write cycles when the chip is selected.

VIDEO INTERFACE SIGNAL DESCRIPTION

HSYNC (Horizontal Sync)
The HSYNC signal is an active-high output used to determine the horizontal position of displayed text. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC (Vertical Sync)
The VSYNC signal is an active-high output used to determine the vertical position of displayed text. Like HSYNC, VSYNC may be used to drive a CRT monitor or composite video generation circuits. VSYNC position and width are both fully programmable.

DISPLAY ENABLE
The DISPLAY ENABLE signal is an active-high output and is used to indicate when the UM6845R is generating active display information. The number of horizontal displayed characters and the number of vertical displayed characters are both fully programmable and together are used to generate the DISPLAY ENABLE signal.

CURSOR
The CURSOR signal is an active-high output and is used to indicate when the scan coincides with the programmed cursor position. The cursor position may be programmed to be any character in the address field. Furthemore, within the character, the cursor may be programmed to be any block of scan lines, since the start scan line and the end scan line are both programmable.

LPEN
The LPEN signal is an edge-sensitive input and is used to load the internal Light Pen Register with the contents of the Refresh Scan Counter at the time the active edge occurs. The active edge of LPEN is the low-to-high transition.

CCLK
The CCLK signal is the character timing clock input and is used as the time base for all internal count/control functions.

$\overline{RES}$
The $\overline{RES}$ signal-is an active-low input used to initialize all internal scan counter circuits. When $\overline{RES}$ is low, all internal counters are stopped and cleared, all scan and video outputs are low, and control registers are unaffected. $\overline{RES}$ must stay low for at least one CCLK period. All scan timing is initiated when $\overline{RES}$ goes high. In this way, $\overline{RES}$ can be used to synchronize display frame timing with line frequency.

MEMORY ADDRESS SIGNAL DESCRIPTION

MA0–MA13 (Video Display RAM Address Lines)
These signals are active-high outputs and are used to address the Video Display RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters/line and lines/frame.

- **Binary Addressing**
  Characters are stored in successive memory locations. Thus, the software must be developed so that row and column co-ordinates are translated to sequentially-numbered addresses for video display memory operations.

RA0-RA4 (Raster Address Lines)
These signals are active-high outputs and are used to select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

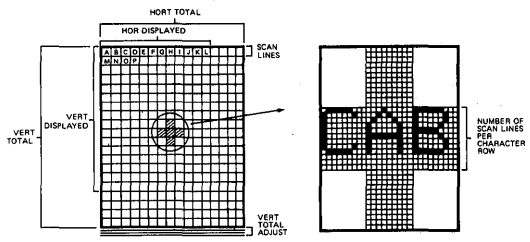


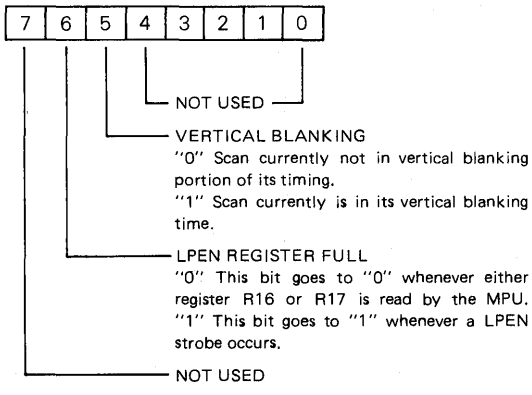
Figure 1. Video Display Format

Description of Internal Registers

Figure 1 illustrates the format of a typical video display and is necessary to understand the functions of the various UM6845R internal registers. Figure 2 illustrates vertical and horizontal timing. Figure 3 summarizes the internal registers and indicates their address selection and read/write capabilities.

Address Register
This is a 5-bit register which is used as a "pointer" to direct UM6845R data transfers to and from the system MPU. Its contents is the number of the desired register (0-31). When RS is low, then this register may be loaded; when RS is high, then the register selected is the one whose identity is stored in this register.

Status Register
This 2-bit register is used to monitor the status of the CRTC, as follows:

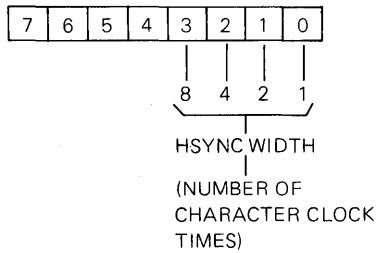


Horizontal Total (R0)
This 8-bit register contains the total of displayed and non-displayed characters, minus one, per horizontal line. The frequency of HSYNC is thus determined by this register.

Horizontal Displayed (R1)
This 8-bit register contains the number of displayed characters per horizontal line.

Horizontal Sync Position (R2)
This 8-bit register contains the position of the HSYNC on the horizontal line, in terms of the character location number on the line. The position of the HSYNC determines the left-to-right location of the displayed text on the video screen. In this way, the side margins are adjusted.

Horizontal and Vertical SYNC Widths (R3)
This 4-bit register programs the width of HSYNC.



VSYNC width is set to 16 scan line times.

Vertical Total (R4)
The Vertical Total Register is a 7-bit register containing the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to be longer than the period of the line frequency, then $\overline{RES}$ may be used to provide absolute synchronism.

Vertical Total Adjust (R5)
The Vertical Total Adjust Register is a 5-bit write only register containing the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

Vertical Displayed (R6)
This 7-bit register contains the number of displayed character rows in each frame. In this way, the vertical size of the displayed text is determined.

Vertical Sync Position (R7)
This 7-bit register is used to select the character row time at which the VSYNC pulse is desired to occur and, thus, is used to position the displayed text in the vertical direction.

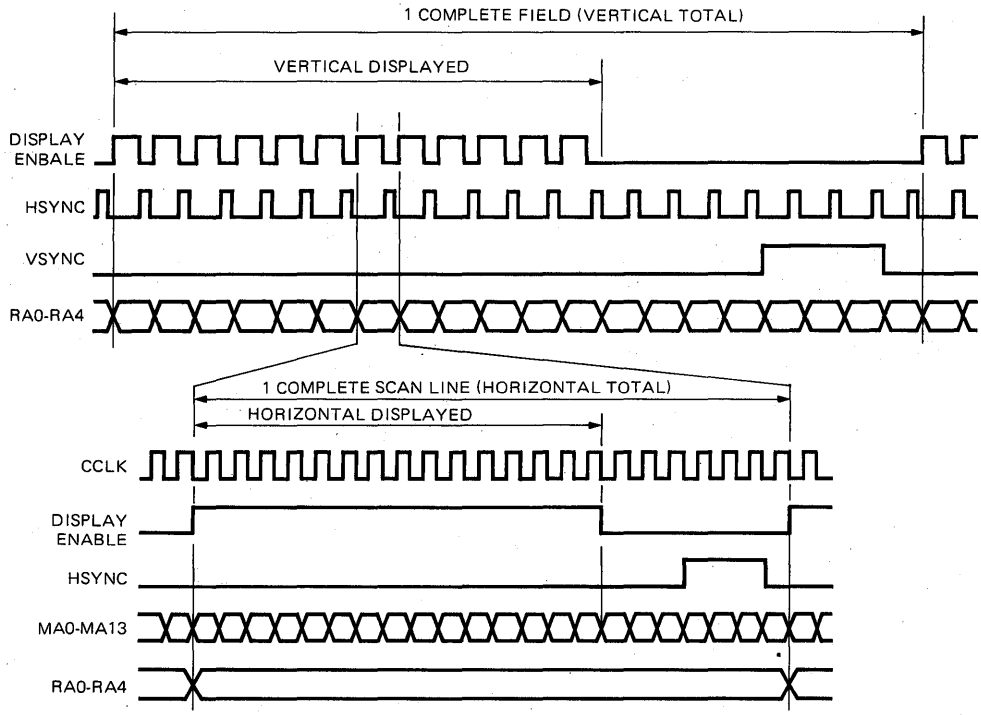
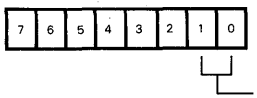


Figure 2. Vertical and Horizontal Timing

Mode Control (R8)

This register is used to select the operating modes of the UM6845R and is outlined as-follows:



BIT		OPERATION
1	0	
X	0	Non-Interlace
0	1	Interlace SYNC Raster Scan
1	1	Interlace SYNC and Video Raster Scan

Scan Line (R9)

This 5-bit register contains the number of scan lines per character row, including spacing minus one.

Cursor Start (R10) and Cursor End (R11)

These 5-bit registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R10 are used to select the cursor mode, as follows:

BIT		CURSOR MODE
6	5	
0	0	No Blinking
0	1	No Cursor
1	0	Blink at 16 x field period
1	1	Blink at 32 x field period

Note that the ability to program both the start and end scan line for the cursor enables either block cursor or underline to be accommodated. Registers R14 and R15 are used to control the character position of the cursor over the entire 16K address field.

Display Start Address High (R12) and Low (R13)

These registers together comprise a 14-bit register whose contents is the memory address of the first character of the displayed scan (the character on the top left of the video display, as in Figure 4. Subsequent memory addresses are generated by the UM6845R as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address associated with the first character of the desired line of text to be displayed first. Entire pages of text may be scrolled or changed as well via R12 and R13.

Cursor Position High (R14) and Low (R15)

These registers together comprise a 14-bit register whose contents is the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, then the CURSOR output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the CURSOR output by a full CCLK time to accommodate slow access memories.

LPEN High (R16) and Low (R17)

These registers together comprise a 14-bit register whose contents is the light pen strobe position, in terms of the video display address at which the strobe occurred. When the LPEN input changes from low to high, then, on the next negative-going edge of CCLK, the contents of the internal scan counter is stored in registers R16 and R17.

CS	RS	Address Reg.					Reg. No.	Register Name	Stored Info.	RD	WR	Register Bit.							
		4	3	2	1	0						7	6	5	4	3	2	1	0
1		–	–	–	–	–	–												
0	0	–	–	–	–	–	–	Address Reg.	Red. No.		√				A_4	A_3	A_2	A_1	A_0
0	0	–	–	–	–	–	–	Status Reg.		√			L	V					
0	1	0	0	0	0	0	R0	Horiz. Total	#Charac, -1		√	●	●	●	●	●	●	●	●
0	1	0	0	0	0	1	R1	Horiz. Displayed	#Charac.		√	●	●	●	●	●	●	●	●
0	1	0	0	0	1	0	R2	Horiz, Sync Position	#Charac.		√	●	●	●	●	●	●	●	●
0	1	0	0	0	1	1	R3	VSYNC, HSYNC Widths	#Scan Lines and #Char, Times		√					H_3	H_2	H_1	H_0
0	1	0	0	1	0	0	R4	Vert. Total	#Charac, Rows -1		√		●	●	●	●	●	●	●
0	1	0	0	1	0	1	R5	Vert, Total Adjust	#Scan Lines		√				●	●	●	●	●
0	1	0	0	1	1	0	R6	Vert, Displayed	#Charac Rows		√		●	●	●	●	●	●	●
0	1	0	0	1	1	1	R7	Vert. Sync Position	#Charac, Rows		√		●	●	●	●	●	●	●
0	1	0	1	0	0	0	R8	Mode Control			√							I_1	I_0
0	1	0	1	0	0	1	R9	Scan Line	#Scan Lines-1		√				●	●	●	●	●
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line No.		√		B_1	B_0	●	●	●	●	●
0	1	0	1	0	1	1	R11	Cursor End	Scan Line No.		√				●	●	●	●	●
0	1	0	1	1	0	0	R12	Display Start Addr (H)			√				●	●	●	●	●
0	1	0	1	1	0	1	R13	Display Start Addr (L)			√	●	●	●	●	●	●	●	●
0	1	0	1	1	1	0	R14	Cursor Position (H)		√	√				●	●	●	●	●
0	1	0	1	1	1	1	R15	Cursor Position (L)		√	√	●	●	●	●	●	●	●	●
0	1	1	0	0	0	0	R16	Light Pen Reg (H)		√					●	●	●	●	●
0	1	1	0	0	0	1	R17	Light Pen Reg (L)		√		●	●	●	●	●	●	●	●

Notes: ● Designates binary bit

▨ Designates unused bit. Reading this bit is always "0", except for $\overline{CS}$ = 1, which does not drive the data bus at all.

Figure 3. Internal Register Summary

TOTAL = 90

DISPLAY = 80

TOTAL = 34

DISPLAY = 24

0	1	2	---	---	77	78	79	80	81	---	89
80	81	82	---	---	157	158	159	160	161	---	169
160	161	162	---	---	237	238	239	240	241	---	249
⋮							⋮				⋮
⋮							⋮				⋮
⋮							⋮				⋮
1760	1761	1762	---	---	1837	1838	1839	1840	1841	---	1849
1840	1841	1842	---	---	1917	1918	1919	1920	1921	---	1929
1920	1921	1922	---	---	1997	1998	1999	2000	2001	---	2009
2000	2001	2002	---	---	2077	2078	2079	2080	2081	---	2089
⋮							⋮				⋮
2640	2641	2642	---	---	2717	2718	2719	2720	2721	---	2729

STRAIGHT BINARY ADDRESSING SEQUENCE

Figure 4. Display Address Sequences (with Start Address = 0) for 80 x 24 Example

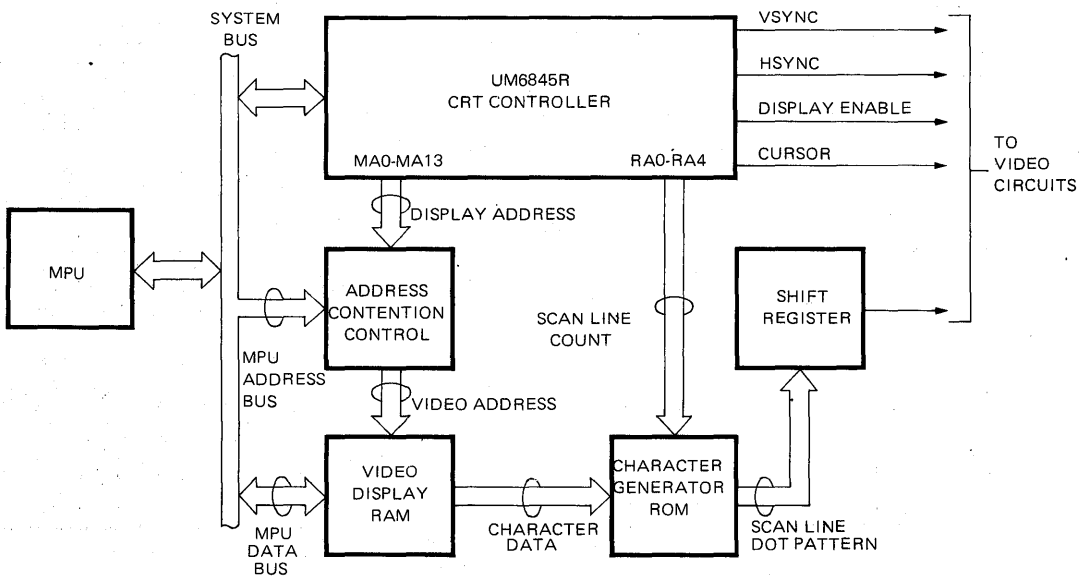


Figure 5. Shared Memory System Configuration

Memory Contention Schemes for Shared Memory Addressing

From the diagram of Figure 5, it is clear that both the UM6845R and the system MPU must be capable of addressing the video display memory. The UM6845R repetitively fetches character information to generate the video signals in order to keep the screen display active. The MPU occasionally accesses the memory to change the displayed information or to read out current data characters. Three ways of resolving this dual-contention requirement are apparent:

MPU PRIORITY

In this technique, the address lines to the video display memory are normally driven by the UM6845R unless the MPU needs access, in which case the MPU addresses immediately override those from the UM6845R and the MPU has immediate access.

$\phi1/\phi2$ MEMORY INTERLEAVING

This method permits both the UM6845R and the MPU access to the video display memory by time-sharing via the system $\phi1$ and $\phi2$ clocks. During the $\phi1$ portion of each cycle (the time when E is low), the UM6845R address outputs are gated to the video display memory. In the $\phi2$ time, the MPU address lines are switched in. In this way, both the UM6845R and the MPU have unimpeded access to the memory. Figure 6 illustrates the timings.

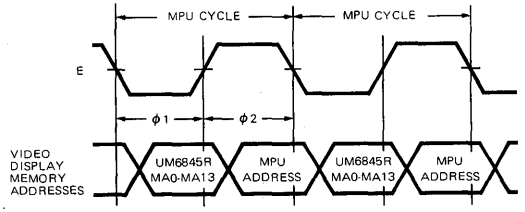


Figure 6. $\phi1/\phi2$ Interleaving

INTERLACE MODES

There are three raster-scan display modes (see Figure 7).

a) Non-Interlaced Mode. In this mode each scan line is refreshed at the vertical field rate (50 or 60Hz).

In the interlaced scan modes, even and odd fields alternate to generate frames. The horizontal and vertical timing relationship causes the scan lines in the odd fields to be displaced from those in the even fields. The two additional raster-scan display modes pertain to interlaced scans.

b) Interlace Sync Mode. This mode is used when the same information is to be displayed in both odd and even fields. Enhanced readability results because the spaces between adjacent rows are filled and a higher quality character is displayed. This is achieved with only a slight alteration in the device operation: in alternate fields, the position of the VSYNC signal is delayed by ½ of a scan line time. This is illustrated in Figure 8 and is the only difference in the UM6845R operation in this mode.

c) Interlaced Sync and Video Mode. This mode is used to double the character density on the screen by displaying the even lines in even fields and the odd lines in odd fields. As in the Interlace-Sync mode, the VSYNC position is delayed in alternate display fields. In addition, the address generation is altered.

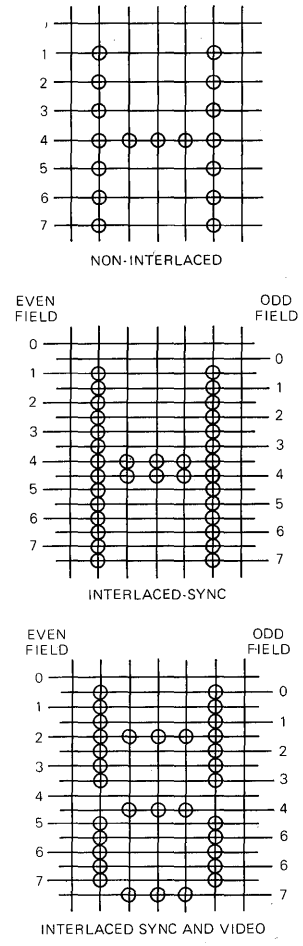


Figure 7. Comparison of Display Modes

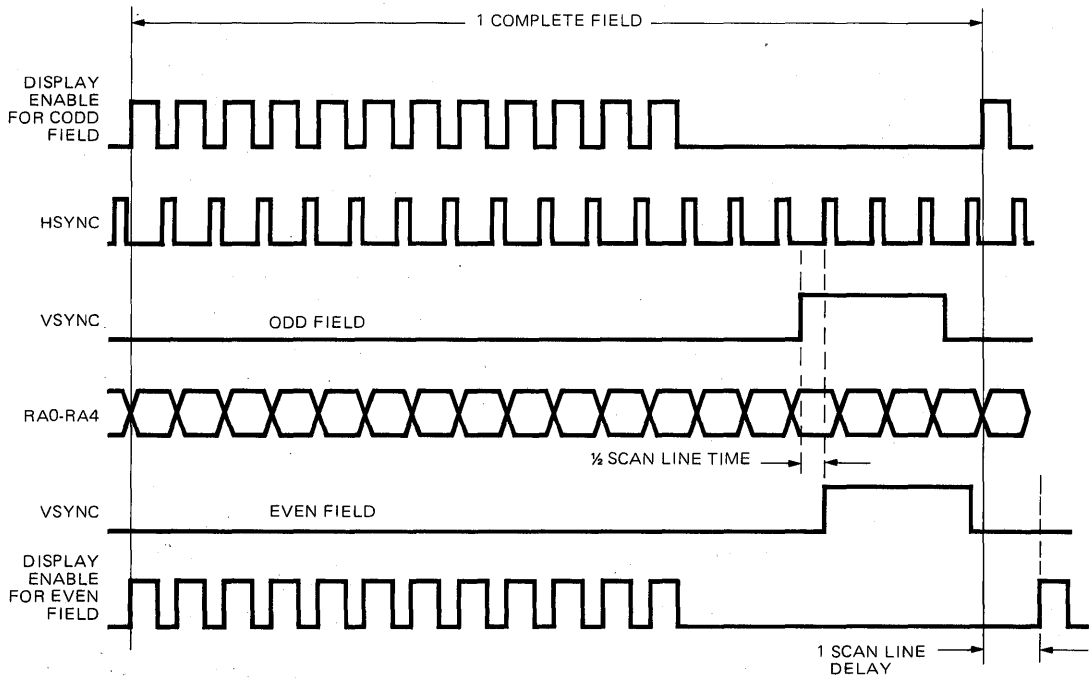


Figure 8. Interface Sync Mode and Interface Sync & Video Mode Timing

CRTC Register Comparison Table

NON-INTERLACE

Register	UM6845R MC6845 MC6845*1	MC6845R HD6845R	UM6845 HD6845S	UM6845E	SYS6545-1
R0 Htotal	Total-1	Total-1	Total-1	Total-1	Total-1
R1 Hdisp	Actual	Actual	Actual	Actual	Actual
R2 Hsync	Actual	Actual	Actual	Actual	Actual
R3 Sync Width	Horizontal (& Vertical *1)	Horizontal	Horizontal & Vertical	Horizontal & Vertical	Horizontal & Vertical
R4 Vtotal	Total-1	Total-1	Total-1	Total-1	Total-1
R5 Vtotal Adjustment	Any Value	Any Value	Any Value	Any Value	Any Value Except R5
R6 Vdisp	Any Value <R4	Any Value <R4	Any Value <R4	Any Value <R4	Any Value <R4
R7 Vsync	Actual-1	Actual-1	Actual-1	Actual-1	Actual-1
R8 B0-1	Interlace	Interlace	Interlace	Interlace	Interlace
Mode Select B2	–	–	–	Row/Column or Binary Addr.	Row/Column or Binary Addr.
B3	–	–	–	Shared or Transparent Addr.	Shared or Transparent Addr.
B4	(Display Enable Skew *1)	–	Display Enable Skew	Display Enable Skew	Display Enable Skew
B5	(Display Enable Skew *1)	–	Display Enable Skew	Cursor Skew	Cursor Skew
B6	(Cursor Skew *1)	–	Cursor Skew	RA4/	RA4/
B7	(Cursor Skew *1)	–	Cursor Skew	Transparent	Transparent
R9 Scan Lines	Total-1	Total-1	Total-1	Total-1	Total-1
R10 Cursor Start	Actual	Actual	Actual	Actual	Actual
R11 Cursor End	Actual	Actual	Actual	Actual	Actual
R12/R13 Display Addr.	Write Only Read/Write (MC6845 & *1)	Read/Write	Read/Write	Write Only	Write Only
R14/R15 Cursor Position	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
R16/R17 Position	Read Only	Read Only	Read Only	Read Only	Read Only
R18/R19 Update Addr. Register	N/A	N/A	N/A	Transparent Mode Only	Transparent Mode Only
R31 Dummy Register	N/A	N/A	N/A	Transparent Mode Only	Transparent Mode Only
Status Register	Yes (UM6845R)	No	No	Yes	Yes

CRTC Register Comparison Table (Continued)

INTERLACE SYNC

Register	UM6845R MC6845 MC6845*1	MC6845R HD6845R	UM6845 HD6845S	UM6845E	SYS6545-1
R0 Htotal	Total-1 = Odd or Even	Total-1 = Odd	Total-1 = Odd	Total-1 = Odd or Even	Total-1 = Odd

INTERALACE SYNC AND VIDEO

R4 Vtotal	Total-1	Total-1	Total-1	Total-1	Total/2-1
R6 Vdisp	Total	Total/2	Total	Total	Total/2
R7 Vsync	Actual-1	Actual-1	Actual-1	Actual-1	Actual/2
R9 Scan Lines	Total-1 Odd/Even	Total-1 Only Even	Total-1 Odd/Even	Total-1 Odd/Even	Total-1 Odd/Even
R10 Cursor Start	Odd/Even	Both Odd or	Odd/Even	Odd/Even	Odd/Even
R11 Cursor End	Odd/Even	Both Even	Odd/Even	Odd/Even	Odd/Even
I_{CCLK}	2.5 MHz	2.5 MHz	3.7 MHz	3.7 MHz	2.5 MHz

Ordering Information

Part Number	CPU Clock Rate	Package
UM6845R	1 MHz	Plastic
UM6845RA	2 MHz	Plastic
UM6845RB	3 MHz	Plastic

UM6845E/UM6845EA/UM6845EB

CRT Controller

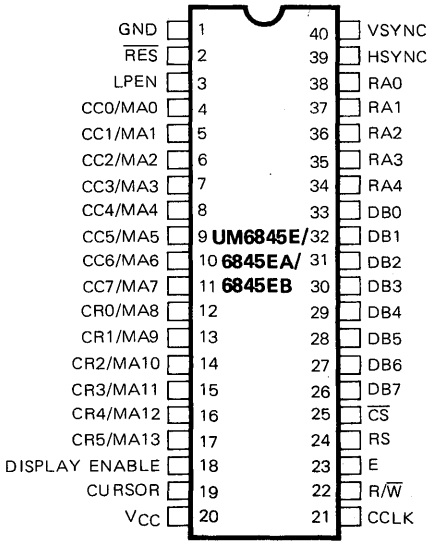
Features

- Single + 5 volt (±5%) power supply
- Alphanumeric and limited graphics capabilities
- Fully programmable display (rows, columns, blanking, etc.).
- Interlaced or non-interlaced scan
- 50/60 Hz operation
- Fully programmable cursor
- External light pen capability
- Capable of addressing up to 16K character Video Display RAM
- No DMA required
- Pin-compatible with MC6845R
- Row/Column or straight-binary addressing for Video Display RAM
- Video Display RAM may be configured as part of microprocessor memory field or independently slaved to 6845
- Internal status register
  3.7 MHz character clock
- Transparent address mode

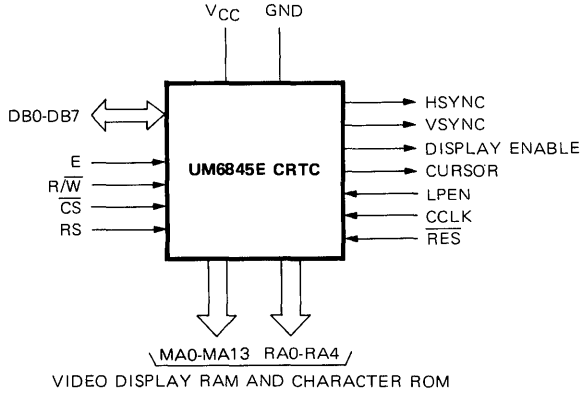
General Description

The UM6845E is a CRT Controller intended to provide capability for interfacing and 8 or 16 bit microprocessor family to CRT or TV-type raster scan displays. A unique feature is the inclusion of several modes of operation, so that the system designer can configure the system with a wide assortment of techniques.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Supply Voltage, V_{CC} . . . . . −0.3V to +7.0V
Input/Output Voltage, V_{IN} . . . . . −0.3V to +7.0V
Operating Temperature, T_{OP} . . . . . 0°C to 70°C
Storage Temperature, T_{STG} . . . . . −55°C to 150°C

All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

*Comments

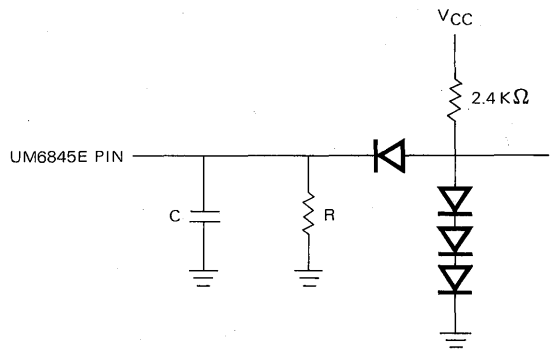
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = 5.0V ±5%, T_A = 0 − 70°C, unless otherwise noted)

Symbol	Characteristics	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	2.0		V_{CC}	V
V_{IL}	Input Low Voltage	−0.3		0.8	V
I_{IN}	Input Leakage (ϕ2, R/W, RES, CS, RS, LPEN, CCLK)	−		2.5	μA
I_{TSI}	Three-State Input Leakage (DB0-DB7) V_{IN} = 0.4 to 2.4V	−10.0		+10.0	μA
V_{OH}	Output High Voltage I_{LOAD} = −205μA (DB0-DB7) I_{LOAD} = −100μA (all others)	2.4		−	V
V_{OL}	Output Low Voltage I_{LOAD} = 1.6mA	−		0.4	V
P_D	Power Dissipation	−	325	650	mW
C_{IN}	Input Capacitance ϕ2, R/W, RES, CS, RS, LPEN, CCLK DB0-DB7	 − −		 10.0 12.5	 pF pF
C_{OUT}	Output Capacitance	−		10.0	pF

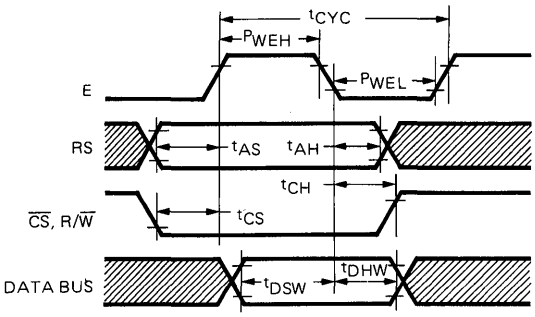
Test Load



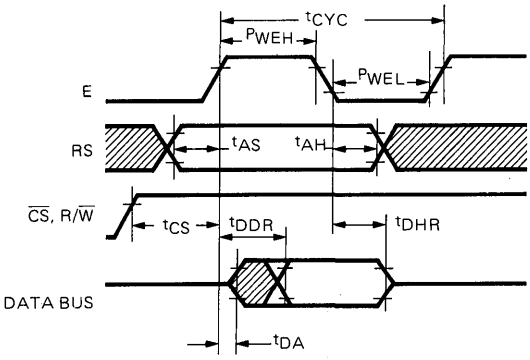
R = 11KΩ FOR DB_0-DB_7
R = 24KΩ FOR ALL OTHER OUTPUTS
C = 130pF TOTAL FOR D_0-D_7
C = 30pF ALL OTHER OUTPUTS

MPU Bus Interface Characteristics

WRITE CYCLE



READ CYCLE



Write Timing Characteristics (V_{CC} = 5.0V ± 5%, T_A = 0 – 70°C, unless otherwise noted)

Symbol	Characteristics	UM6845E		UM6845EA		UM6845EB		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	–	0.5	–	0.33	–	μs
P_{WEH}	E Pulse Width, High	440	–	200	–	150	–	ns
P_{WEL}	E Pulse Width, Low	420	–	190	–	140	–	ns
t_{AS}	Address Set-Up Time	80	–	40	–	30	–	ns
t_{AH}	Address Hold Time	0	–	0	–	0	–	ns
t_{CS}	R/W, CS Set-Up Time	80	–	40	–	30	–	ns
t_{CH}	R/W, CS Hold Time	0	–	0	–	0	–	ns
t_{DSW}	Data Bus Set-Up Time	165	–	60	–	60	–	ns
t_{DHW}	Data Bus Hold Time	10	–	10	–	10	–	ns

(t_r and t_f = 10 to 30 ns)

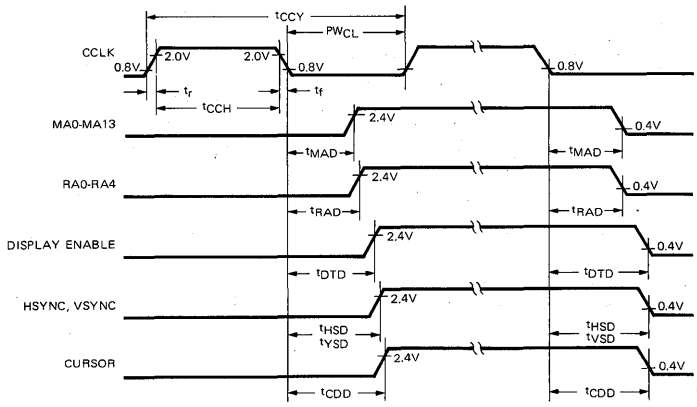
Read Timing Characteristics (V_{CC} = 5.0V ± 5%, T_A = 0 – 70°C, unless otherwise noted)

Symbol	Characteristics	UM6845E		UM6845EA		UM6845EB		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	–	0.5	–	0.33	–	μs
P_{WEH}	ϕ_2 Pulse Width, High	440	–	200	–	150	–	ns
P_{WEL}	ϕ_2 Pulse Width, Low	420	–	190	–	140	–	ns
t_{AS}	Address Set-Up Time	80	–	40	–	30	–	ns
t_{AH}	Address Hold Time	0	–	0	–	0	–	ns
t_{CS}	R/W, CS Set-Up Time	80	–	40	–	30	–	ns
t_{DDR}	Read Access Time (Valid Data)	–	290	–	150	–	100	ns
t_{DHR}	Read Hold Time	10	–	10	–	10	60	ns
t_{DA}	Data Bus Active Time (Invalid Data)	20	60	20	60	20	60	ns
t_{TAD}	MA0-MA13 Switching Delay (Refer to Figure Trans. Addressing)	100 typ.	160	100 typ.	160	90 typ.	130	ns

(t_r and t_f = 10 to 30 ns)

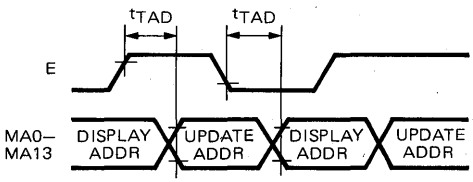
Memory and Video Interface Characteristics

(V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

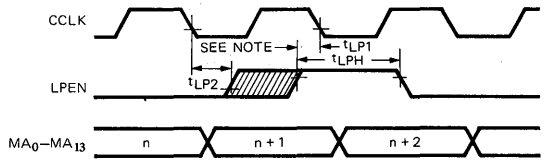


Symbol	Parameter	Min.	Typ.	Max.	Units
t_{CCH}	Minimum Clock Pulse Width, High	130			ns
t_{CCV}	Clock Frequency			3.7	MHz
t_r, t_f	Rise and Fall Time for Clock Input			20	ns
t_{MAD}	Memory Address Delay Time		100	160	ns
t_{RAD}	Raster Address Delay Time		100	160	ns
t_{DTD}	Display Timing Delay Time		160	250	ns
t_{HSD}	Horizontal Sync Delay Time		160	250	ns
t_{VSD}	Vertical Sync Delay Time		160	250	ns
t_{CDD}	Cursor Display Timing Delay Time		160	250	ns

Transparent Addressing (ϕ1/ϕ2 Interleaving)



Light Pen Strobe Timing



Note: "Safe" time position for LPEN positive edge to cause address n + 2 to load into Light Pen Register. t_{LP2} and t_{LP1} are time positions causing uncertain results.

Symbol	Characteristics	UM6845E		UM6845EA		UM6845EB		Unit
		Min.	max.	Min.	Max.	Min.	Max.	
t_{LPH}	LPEN Strobe Width	100	–	100	–	100	–	ns
t_{LP1}	LPEN to CCLK Delay	–	120	–	120	–	120	ns
t_{LP2}	CCLK to LPEN Delay	–	0	–	0	–	0	ns

t_r and t_f = 20 ns (max.)

MPU Interface Signal Description

E (Enable)
The enable signal is the system input and is used to trigger all data transfers between the system microprocessor and the UM6845E. Since there is no maximum limit to the allowable E cycle time, it is not necessary for it to be a continuous clock. This capability permits the UM6845E to be easily interfaced to non-6500-compatible microprocessors.

R/$\overline{W}$ (Read/Write)
The R/$\overline{W}$ signal is generated by the microporocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the UM6845E, a low on the R/$\overline{W}$ pin allows a write to the UM6845E.

$\overline{CS}$ (Chip Select)
The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The UM6845E is selected when $\overline{CS}$ is low.

RS (Register Select)
The Register Select input is used to access internal registers. A low on this pin permits write into the Address Register and reads from the Status Register. The contents of the Address Register is the identity of the register accessed when RS is high.

DB_9-DB_7 (Data Bus)
The DB_0-DB_7 pins are the eight data lines used for transfer of data between the processor and the UM6845E. These lines are bi-directional and are normally high-impedance except during read/write cycles when the chip is selected.

Video Interface Signal Description

HSYNC (Horizontal Sync)
The HSYNC signal is an active-high output used to determine the horizontal position of displayed text. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC (Vertical Sync)
The VSYNC signal is an active-high output used to determine the vertical position of displayed text. Like HSYNC, VSYNC may be used to drive a CRT monitor or composite video generation circuits. VSYNC position and width are both fully programmable.

DISPLAY ENABLE
The DISPLAY ENABLE signal is an active-high output and is used to indicate when the UM6845E is generating active display information. The number of horizontal displayed characters and the number of vertical displayed characters are both fully programmable and together are used to generate the DISPLAY ENABLE signal. DISPLAY ENABLE may be delayed by one character time by setting bit 4 of R8 to a "1"

CURSOR
The CURSOR signal is an active-high output and is used to indicate when the scan coincides with the programmed cursor position. The cursor position may be programmed to be any character in the address field. Furthermore, within the character, the cursor may be programmed to be any block of scan lines, since the start scan line and the end scan line are both programmable. The CURSOR position may be delayed by one character time by setting bit 5 of R8 to a "1"

LPEN
The LPEN signal is an edge-sensitive input and is used to load the internal Light Pen Register with the contents of the Refresh Scan Counter at the time the active edge occurs. The active edge of LPEN is the low-to-high transition.

CCLK
The CCLK signal is the character timing clock input and is used as the time base for all internal count/control functions.

$\overline{RES}$
The $\overline{RES}$ signal is an active-low input used to initialize all internal scan counter circuits. When $\overline{RES}$ is low, all internal counters are stopped and cleared, all scan and video outputs are low, and control registers are unaffected. $\overline{RES}$ must stay low for at least one CCLK period. All scan timing is initiated when $\overline{RES}$ goes high. In this way, $\overline{RES}$ can be used to synchronize display frame timing with line frequency.

Memory Address Signal Description

MA0-MA13 (Video Display RAM Address Lines)
These signals are active-high outputs and are used to address the Video Display RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters/line and lines/frame.

There are two selectable address modes for MA0-MA13:

- Binary
  Characters are stored in successive memory locations. Thus, the software must be developed so that row and column co-ordinates are translated to sequentially numbered addresses for video display memory operations.
- Row/Column
  In this mode, MA0-MA7 function as column addresses CC0-CC7, and MA8-MA13, as row addresses CR0-CR5. In this case, the software may handle addresses in terms of row and column locations, but additional address compression circuits are needed to convert CC0-CC7 and CR0-CR5 into a memory-efficient binary scheme.

RA0-RA4 (Raster Address Lines)

These signals are active-high outputs and are used to select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

The high-order line, RA4, is unique in that it can also function as a strobe output pin when the UM6845E is programmed to operate in the "Transparent Address Mode". In this case the strobe is an active-high output and is true at the time the Video Display RAM update address is gated on to the address lines, MA0-MA13. In this way, updates and readouts of the Video Display RAM can be made under control of the UM6845E with only a small amount of external circuitry.

Description of Internal Registers

Figure 1 illustrates the format of a typical video display and is necessary to understand the functions of the various UM6845E internal registers. Figure 2 illustrates vertical and horizontal timing. Figure 3 summarizes the internal registers and indicates their address selection and read/write capabilities.

Address Register

This is a 5-bit register which is used as a "pointer" to direct UM6845E data transfers to and from the system MPU. Its contents is the number of the desired register (0-31). When RS is low, then this register may be loaded; when RS is high, then the register selected is the one whose identity is stored in this register.

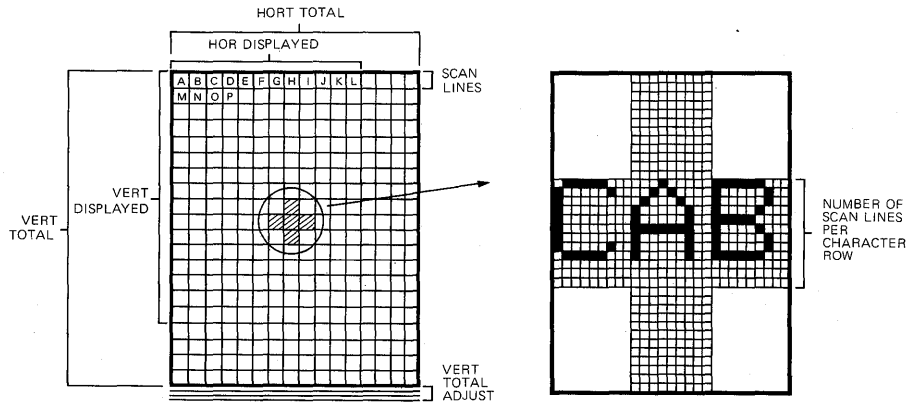
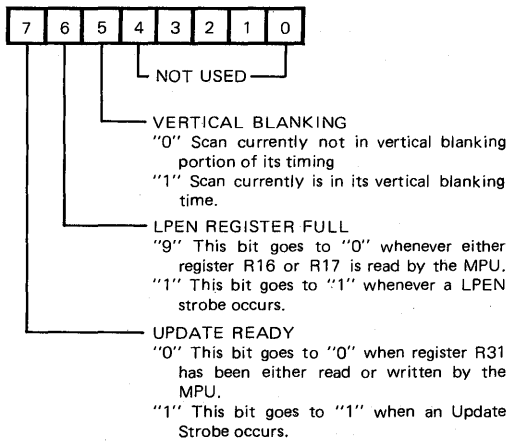


Figure 1. Video Display Format

Status Register

This 3-bit register is used to monitor the status of the CRTC, as follows:



Horizontal Total (R0)

This 8-bit register contains the total of displayed and non-displayed characters, minus one, per horizontal line. The frequency of HSYNC is thus determined by this register.

Horizontal Displayed (R1)

This 8-bit register contains the number of displayed characters per horizontal line.

Horizontal Sync Position (R2)

This 8-bit register contains the position of the HSYNC on the horizontal line, in terms of the character location number on the line. The position of the HSYNC determines the left-to-right location of the displayed text on the video screen. In this way, the side margins are adjusted.

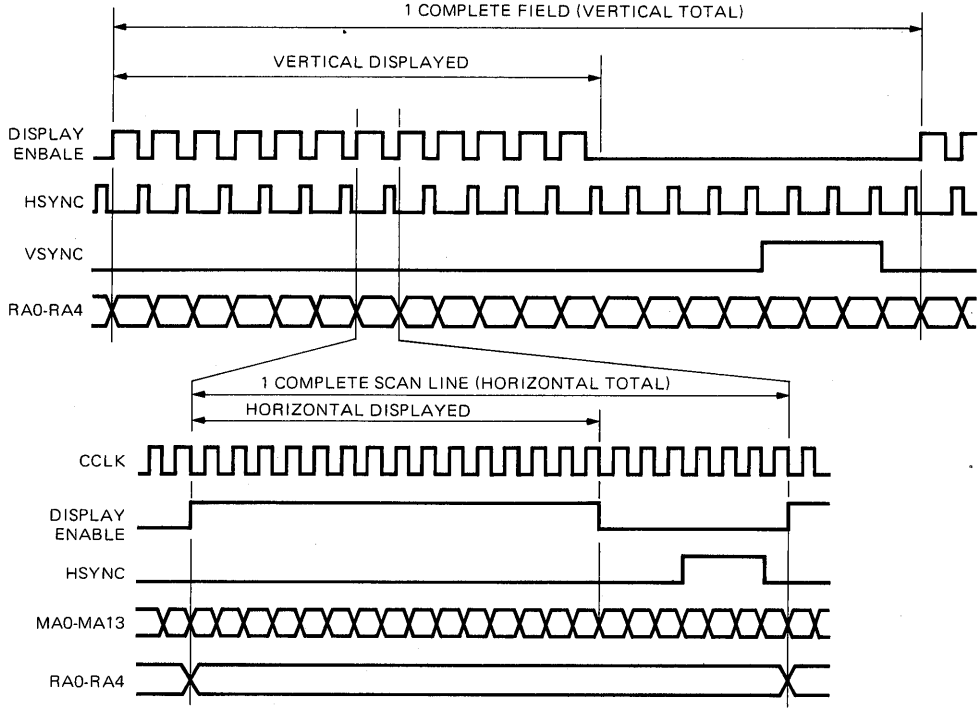
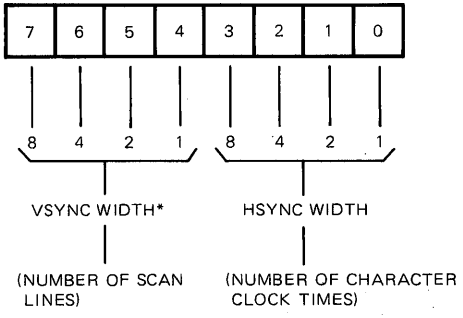


Figure 2. Vertical and Horizontal Timing

Horizontal and Vertical SYNC Widths (R3)

This 8-bit register contains the widths of both HSYNC and VSYNC, as follows:



*IF BITS 4-7 ARE ALL "0", THEN VSYNC WILL BE 16 SCAN LINES WIDE.

Control of these parameters allows the UM6845E to be interfaced to a variety of CRT monitors, since the HSYNC and VSYNC timing signals may be accommodated without the use of external one-shot timing.

Vertical Total (R4)

The Vertical Total Register is a 7-bit register containing the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to be longer than the period of the line frequency, then $\overline{RES}$ may be used to provide absolute snchronism.

Vertical Total Adjust (R5)

The Vertical Total Adjust Register is a 5-bit write only register containing the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

Vertical Displayed (R6)

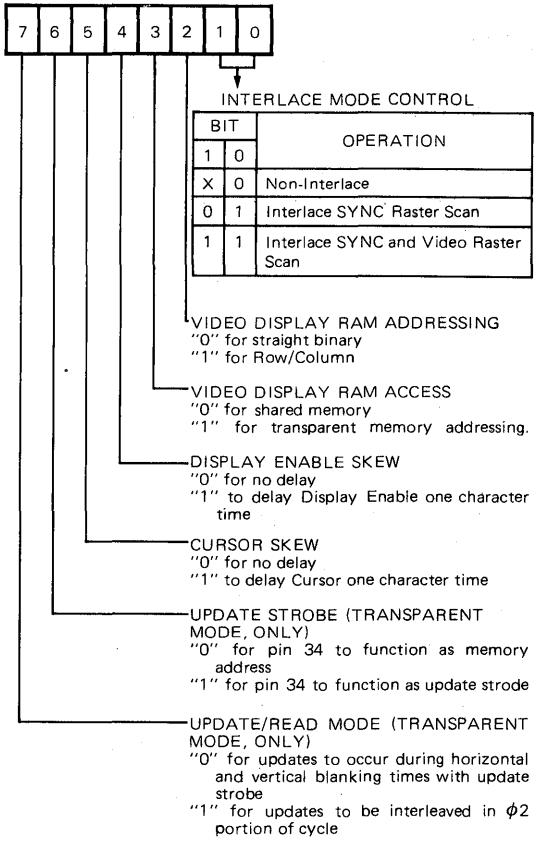
This 7-bit register contains the number of displayed character rows in each frame. In this way, the vertical size of the displayed text is determined.

Vertical Sync Position (R7)

This 7-bit register is used to select the character row time at which the VSYNC pulse is desired to occur and, thus, is used to position the displayed text in the vertical direction.

Mode Control (R8)

This register is used to select the operating modes of the UM6845E and is outlined as follows:



Scan Line (R9)

This 5-bit register contains the number of scan lines per character row, including spacing minus one.

Cursor Start (R10) and Cursor End (R11)

These 5-bit registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R 10 are used to select the cursor mode, as follows:

BIT 6	BIT 5	Cursor Mode
0	0	No Blinking
0	1	No Cursor
1	0	Blink at 16 x field period
1	1	Blink at 32 x field period

Note that the ability to program both the start and end scan line for the cursor enables either block cursor or underline to be accommodate. Registers R14 and R15 are used to control the character position of the cursor over the entire 16K address field.

Display Start Address High (R12) and Low (R13)

These registers together comprise a 14-bit register whose contents is the memory address of the first character of the displayed scan (the character on the top left of the video display, as in Figure 1). Subsequent memory addresses are generated by the UM6845E as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address associated with the first character of the desired line of text to be displayed first. Entire pages of text may be scrolled or changed as well via R12 and R13.

Cursor Position High (R14) and Low (R15)

These registers together comprise a 14-bit register whose contents is the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, then the CURSOR output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the CURSOR output by a full CCLK time to accommodate slow access memories.

LPEN High (R16) and Low (R17)

These registers together comprise a 14-bit register whose contents is the light pen strobe position, in terms of the video display address at which the strobe occurred. When the LPEN input changes from low to high, then, on the next negative-going edge of CCLK, the contents of the internal scan counter is stored in registers R16 and R17.

Update Address High (R18) and Low (R19)

These registers together comprise a 14-bit register whose contents is the memory address at which the next read or update will occur (for transparent address mode, only). Whenever a read/update occurs, the update location automatically increments to allow for fast updates or readouts of consecutive character locations. This is described elsewhere in this document.

Dummy Location (R31)

This register does not store any data, but is required to detect when transparent addressing updates occur. This is necessary to increment the Update Address Register and to set the Update Ready bit in the status register.

Description of Operation

Register Formats

Register pairs R12/R13, R14/R15, R16/R17, and R18/R19 are formatted in one of two ways:

1. Straight binary if register R8, bit 2 is a "0".
2. Row/Column if register R8, bit 2 is a "1". In this

case the low byte is the Character Column and the high byte is the Character Row.

Figure 4 illustrates the address sequence for the video display control for each mode.

Note from Figure 4 that the straight-binary mode has the advantage that all display memory addresses are stored in a continuous memory block, starting with address 0 and ending at 1919. The disadvantage with this method is that, if it is desired to change a displayed character location, the row and column identity of the location must be converted to its binary address before the memory may be written. The row/column mode, on the other hand, does not need to undergo this conversion. However, memory is not used as efficiently, since the memory addresses are not continuous, but gaps exist. This reguires that the system be equipped with more memory than is actually used and this extra memory is wasted. Alternatively, address compression logic may be employed to translate the row/column format into a continuous address block.

In this way, the user may select whichever mode is best for the given application. The trade-offs between the modes are software versus hardware. Straight-binary mode minimizes hardware requirements and row/column requires minimum software.

Video Display RAM Addressing

There are two modes of addressing for the video display memory:

1. Shared Memory

   In this mode the memory is shared between the MPU address bus and the UM6845E address bus. For this case, memory contention must be resolved by means of external timing and control circuits. Both the MPU and the UM6845E must have access to the video display RAM and the contention circuits must resolve this multiple access requirement. Figure 5 illustrates the system configuration.

$\overline{CS}$	RS	Address Reg. 4	3	2	1		Reg. No.	Register Name	Stored Info.	RD	WR	Register Bit 7	6	5	4	3	2	1	0
1		–	–	–	–	–	–												
0	0	–	–	–	–	–	–	Address Reg.	Reg. No.		√				A_4	A_3	A_2	A_1	A_0
0	0	–	–	–	–	–	–	Status Reg.		√		U	L	V					
0	1	0	0	0	0	0	R0	Horiz, Total	#Charac, – 1		√	●	●	●	●	●	●	●	●
0	1	0	0	0	0	1	R1	Horiz, Displayed	#Charac.		√	●	●	●	●	●	●	●	●
0	1	0	0	0	1	0	R2	Horiz, Sync Position	#Charac.		√	●	●	●	●	●	●	●	●
0	1	0	0	0	1	1	R3	VSYNC, HSYNC Widths	#Scan Lines and #Char, Times		√	V_3	V_2	V_1	V_0	H_3	H_2	H_1	H_0
0	1	0	0	1	0	0	R4	Vert, Total	#Charac, Row – 1		√		●	●	●	●	●	●	●
0	1	0	0	1	0	1	R5	Vert, Total Adjust	#Scan Lines		√				●	●	●	●	●
0	1	0	0	1	1	0	R6	Vert, Displayed	#Charac, Rows		√		●	●	●	●	●	●	●
0	1	0	0	1	1	1	R7	Vert, Sync Poisition	#Charac, Rows		√		●	●	●	●	●	●	●
0	1	0	1	0	0	0	R8	Mode Control			√	U_1	U_0	C	D	T	RC	I_1	I_0
0	1	0	1	0	0	1	R9	Scan Line	#Scan Lines–1		√				●	●	●	●	●
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line No.		√		B_1	B_0	●	●	●	●	●
0	1	0	1	0	1	1	R11	Cursor End	Scan Line No.		√				●	●	●	●	●
0	1	0	1	1	0	0	R12	Display Start Addr (H)	Row		√			●	●	●	●	●	●
0	1	0	1	1	0	1	R13	Display Start Addr (L)	Col		√	●	●	●	●	●	●	●	●
0	1	0	1	1	1	0	R14	Cursor Position (H)	Row	√	√			●	●	●	●	●	●
0	1	0	1	1	1	1	E15	Cursor Position (L)	Col	√		●	●	●	●	●	●	●	●
0	1	1	0	0	0	0	R16	Light Pen Reg (H)		√				●	●	●	●	●	●
0	1	1	0	0	0	1	R17	Light Pen Reg (L)		√		●	●	●	●	●	●	●	●
0	1	1	0	0	1	0	R18	Update Location (H)			√			●	●	●	●	●	●
0	1	1	0	0	1	1	R19	Update Location (L)			√	●	●	●	●	●	●	●	●
0	1	1	1	1	1	1	R31	Dummy Location											

Notes: ● Designates binary bit

▨ Designates unused bit, Reading this bit is always "0", except for R31, which does not drive the data bus at all, and for CS = "1" which operates likewise.

Figure 3. Internal Register Summary

CRT Controller

Straight Binary Addressing Sequence

TOTAL = 90

DISPLAY = 80

TOTAL = 34 / DISPLAY = 24

0	1	2	---	---	77	78	79	80	81	---	89
80	81	82	---	---	157	158	159	160	161	---	169
160	161	162	---	---	237	238	239	240	241	---	249
⋮							⋮				⋮
⋮							⋮				⋮
⋮							⋮				⋮
1760	1761	1762	---	---	1837	1838	1839	1840	1841	---	1849
1840	1841	1842	---	---	1917	1918	1919	1920	1921	---	1929
1920	1921	1922	---	---	1997	1998	1999	2000	2001	---	2009
2000	2001	2002	---	---	2077	2078	2079	2080	2081	---	2089
⋮							⋮				⋮
2640	2641	2642	---	---	2217	2718	2719	2720	2721	---	2729

Row/Column Addressing Sequence

TOTAL = 90

DISPLAY = 80

COLUMN ADDRESS (MA0-MA7)

TOTAL = 34 / DISPLAY = 24 / ROW ADDRESS (MA8-MA13)

	0	1	2			77	78	79	80	81		89
0	0	1	2	---	---	77	78	79	80	81	---	89
1	256	257	258	---	---	333	334	335	336	337	---	345
2	512	513	514	---	---	589	590	591	592	593	---	601
	⋮							⋮				⋮
	⋮							⋮				⋮
21	⋮							⋮				⋮
22	5632	5633	5634	---	---	5709	5710	5711	5712	5713	---	5721
23	5888	5889	5890	---	---	5965	5966	5697	5968	5969	---	5977
24	6144	6145	6146	---	---	6221	6222	6223	6224	6225	---	6233
25	6400	6401	6402	---	---	6477	6478	6479	6480	6481	---	6489
	⋮							⋮				⋮
33	8448	8449	8450	---	---	8525	8526	8527	8528	8529	---	8537

Figure 4. Display Address Sequences (with Start Address = 0) for 80 x 24 Example

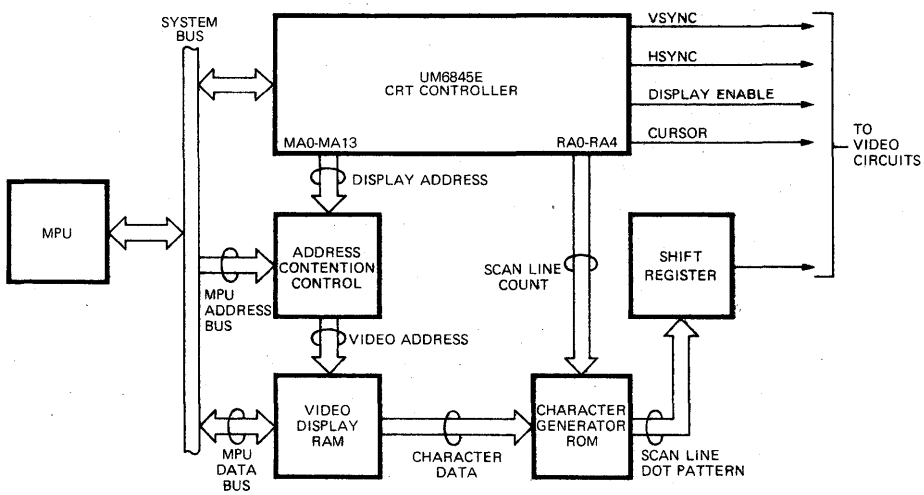


Figure 5. Shared Memory System Configuration

2. Transparent Memory Addreessing.

For this mode, the display RAM is not directly accessible by the MPU, but is controlled entirely by the UM6845E. All MPU accesses are made via the UM6845E and a small amount of external circuits. Figure 6 shows the system configuration for this approach.

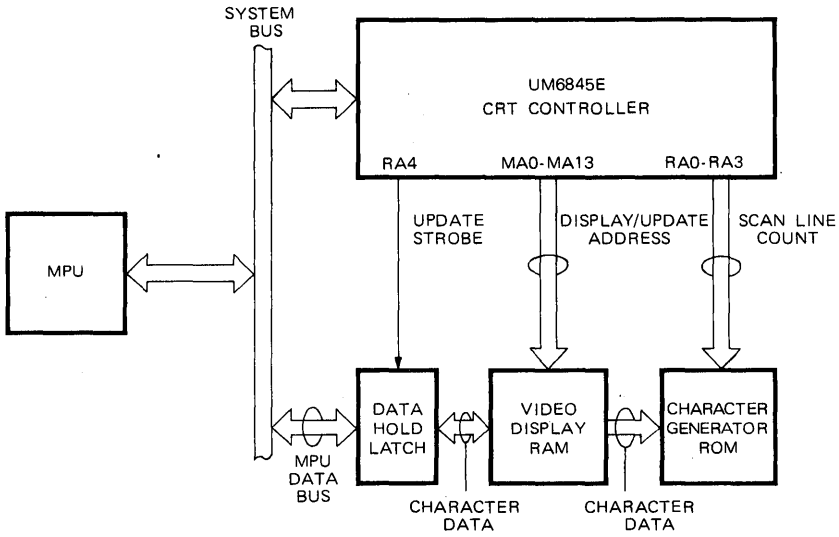


Figure 6. Transparent Memory Addressing System Configuration (Data Hold Latch needed for Horizontal/Vertical Blanking updates, only).

Memory Contention Schemes for Shared Memory Addressing

From the diagram of Figure 4, it is clear that both the UM6845E and the system MPU must be capable of addressing the video display memory. The UM6845E repetitively fetches character information to generate the video signals in order to keep the screen display active. The MPU occasionally accesses the memory to change the displayed information or to read out current data characters. Three ways of resolving this dualcontention requirement are apparent:

- **MPU Priority**

  In this technique, the address lines to the video display memory are normally driven by the UM6845E unless the MPU needs access, in which case the MPU addresses immediately overried those from the UM6845E and the MPU has immediate access.

- **$\phi 1/\phi 2$ Memory Interleaving**

  This method permits both the UM6845E and the MPU access to the video display memory by timesharing via the system $\phi 1$ and $\phi 2$ clocks. During the $\phi 1$ portion of each cycle (the time when E is low), the UM6845E address outputs are gated to the video display memory. In the $\phi 2$ time, the MPU address lines are switched in. In this way, both the UM6845E and the MPU have unimpeded access to the memory. Figure 7 illustrates the timings.

- **Vertical Blanking**

  With this approach, the address circuitry is identical to the case for MPU Priority updates. The only difference is that the Vertical Retrace status bit (bit 5 of the Status Register) is used by the MPU so that access to the video display memory is only made during vertical blanking time (when bit 5 is a "1"). In this way, no visible screen perturbations result.

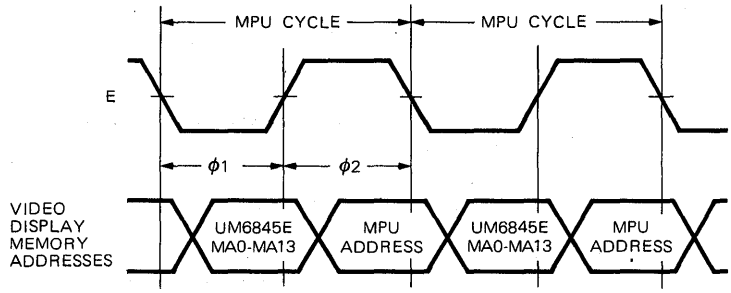


Figure 7. φ1/φ2 Interleaving

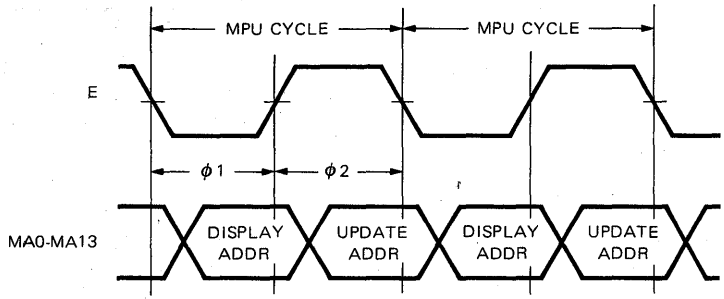


Figure 8. φ1/φ2 Transparent Interleaving

Transparent Memory Addressing

In this mode of operation, the video display memory address lines are not switched by contention circuits, but are generated by the UM6845E. In effect, the contention is handled by the UM6845E. As a result, the schemes for accomplishing MPU memory access are different:

■ **φ1/φ2 Interleaving**

This mode is similar to the Interlave mode used sed with shared memory. In this case, however, the φ2 address is generated from the Update Address Register (Registers R18 and R19) in the UM6845E. Thus, the MPU must first load the address to be accessed into R18/R19 and then this address is always gated onto the MA lines during φ2. Figure 8 shows the timing.

■ **Horizontal/Vertical Blanking**

In this mode, the Update Address is loaded by the MPU, but is only gated onto the MA lines during horizontal or vertical blank times, so memory accesses do not interfere with the display appearance. To signal when the update address is on the MA lines, an update strobe (STR) is provided as an alternate function of pin 34. Data hold latches are necessary to temporarily retain the character to be stored until the retrace time occurs. In this way, the system MPU is not halted waiting for the blanking time to arrive. Figure 9 illustrates the address and strobe timing for this mode.

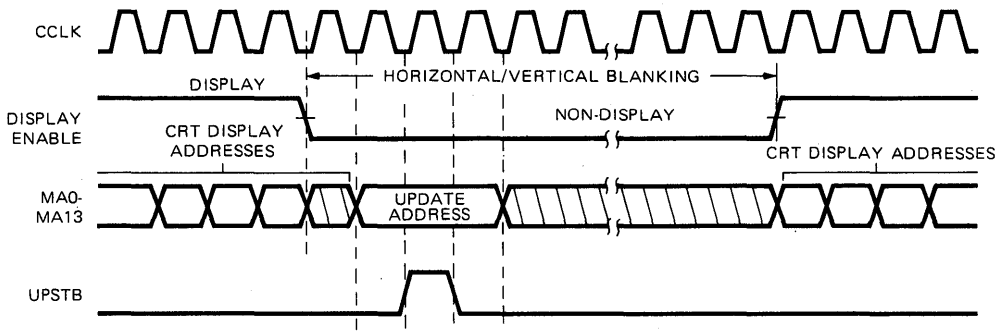


Figure 9. Retrace Update Timings

Interlace Modes

There are three raster-scan display modes (see Figure 10).

a) Non-Interlaced Mode

In this mode each scan line is refreshed at the vertical field rate (50 or 60 Hz).

In the interlaced scan modes, even and odd fields alternate to generate frames. The horizontal and vertical timing relationship causes the scan lines in the odd fields to be displaced from those in the even fields. The two additional raster-scan display modes pertain to interlaced scans.

b) Interlace-Sync Mode

This mode is used when the same information is to be displayed in both odd and even fields. Enhanced readability results because the spaces between adjacent rows are filled and a higher quality character is displayed. This is achieved with only a slight alteration in the device operation: in alternate fields, the position of the VSYNC signal is delayed by ½ of a scan line time. This is illustrated in Figure 11 and is the only difference in the UM6845E operation in this mode.

c) Interlaced Sync and Video Mode

This mode is used to double the character density on the screen by displaying the even lines in even fields and the odd lines in odd fields. As in the Interlace-Sync mode, the VSYNC position is delayed in alternate display fields. In addition, the address generation is altered.

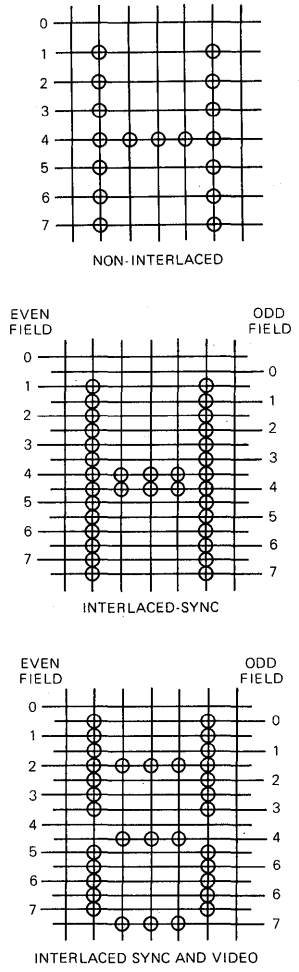


Figure 10. Comparison of Display Modes

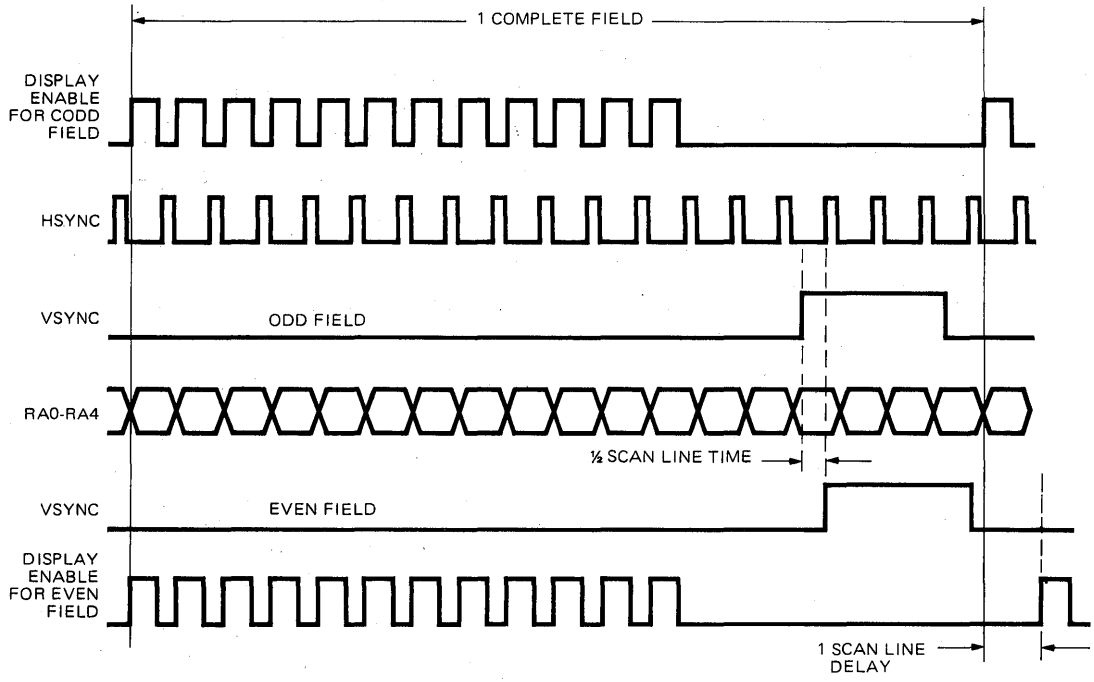


Figure 11. Interlace Sync Mode and Interlace Sync & Video Mode Timing

Cursor and Display Enable Skew Control

Bits 4 and 5 of the Mode Control register (R8) are used to delay the Display Enable and Cursor outputs, respectively. Figure 12 illustrates the effect of the delays.

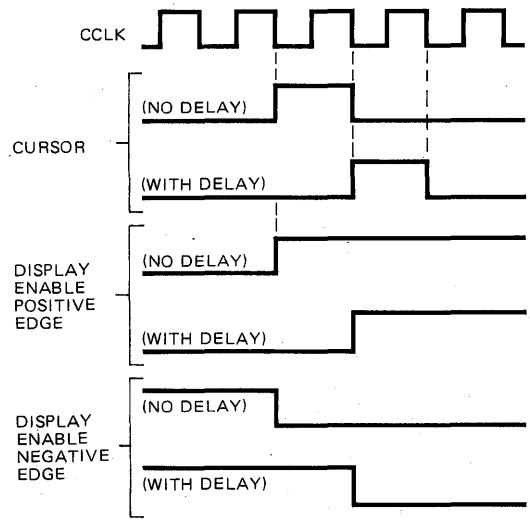


Figure 12. Cursor and Display Enalbe Skew

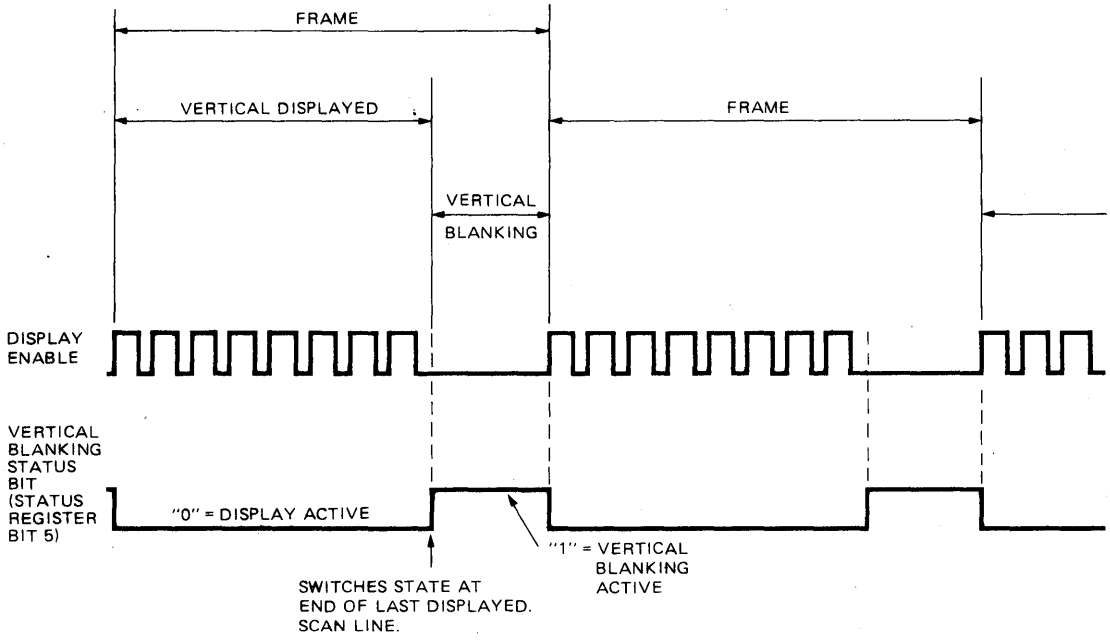


Figure 13. Operation of Vertical Blanking Status Bit

CRTC Register Comparison Table

NON-INTERLACE

Register	UM6845R MC6845 MC6845*1	MC6845R HD6845R	UM6845 HD6845S	UM6845E	SYS6545-1
R0 Htotal	Total-1	Total-1	Total-1	Total-1	Total-1
R1 Hdisp	Actual	Actual	Actual	Actual	Actual
R2 Hsync	Actual	Actual	Actual	Actual	Actual
R3 Sync Width	Horizontal (& Vertical *1)	Horizontal	Horizontal & Vertical	Horizontal & Vertical	Horizontal & Vertical
R4 Vtotal	Total-1	Total-1	Total-1	Total-1	Total-1
R5 Vtotal Adjustment	Any Value	Any Value	Any Value	Any Value	Any Value Except R5
R6 Vdisp	Any Value <R4	Any Value <R4	Any Value <R4	Any Value <R4	Any Value <R4
R7 Vsync	Actual-1	Actual-1	Actual-1	Actual-1	Actual-1
R8 B0-1	Interlace	Interlace	Interlace	Interlace	Interlace
Mode Select B2	–	–	–	Row/Column or Binary Addr.	Row/Column or Binary Addr.
B3	–	–	–	Shared or Transparent Addr.	Shared or Transparent Addr.
B4	(Display Enable Skew *1)	–	Display Enable Skew	Display Enable Skew	Display Enable Skew
B5	(Display Enable Skew *1)	–	Display Enable Skew	Cursor Skew	Cursor Skew
B6	(Cursor Skew *1)	–	Cursor Skew	RA4/	RA4/
B7	(Cursor Skew *1)	–	Cursor Skew	Transparent	Transparent
R9 Scan Lines	Total-1	Total-1	Total-1	Total-1	Total-1
R10 Cursor Start	Actual	Actual	Actual	Actual	Actual
R11 Cursor End	Actual	Actual	Actual	Actual	Actual
R12/R13 Display Addr.	Write Only Read/Write (MC6845 & *1)	Read/Write	Read/Write	Write Only	Write Only
R14/R15 Cursor Position	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
R16/R17 Position	Read Only	Read Only	Read Only	Read Only	Read Only
R18/R19 Update Addr. Register	N/A	N/A	N/A	Transparent Mode Only	Transparent Mode Only
R31 Dummy Register	N/A	N/A	N/A	Transparent Mode Only	Transparent Mode Only
Status Register	Yes (UM6845R)	No	No	Yes	Yes

CRTC Register Comparison Table (Continued)

INTERLACE SYNC

Register	UM6845R MC6845 MC6845*1	MC6845R HD6845R	UM6845 HD6845S	UM6845E	SYS6545-1
R0 Htotal	Total-1 = Odd or Even	Total-1 = Odd	Total-1 = Odd	Total-1 = Odd or Even	Total-1 = Odd

INTERALACE SYNC AND VIDEO

R4 Vtotal	Total-1	Total-1	Total-1	Total-1	Total/2-1
R6 Vdisp	Total	Total/2	Total	Total	Total/2
R7 Vsync	Actual-1	Actual-1	Actual-1	Actual-1	Actual/2
R9 Scan Lines	Total-1 Odd/Even	Total-1 Only Even	Total-1 Odd/Even	Total-1 Odd/Even	Total-1 Odd/Even
R10 Cursor Start	Odd/Even	Both Odd or	Odd/Even	Odd/Even	Odd/Even
R11 Cursor End	Odd/Even	Both Even	Odd/Even	Odd/Even	Odd/Even
I_{CCLK}	2.5 MHz	2.5 MHz	3.7 MHz	3.7 MHz	2.5 MHz

Ordering Information

Part Number	CPU Clock Rate	Package
UM6845E	1 MHz	Plastic
UM6845EA	2 MHz	Plastic
UM6845EB	3 MHz	Plastic

UM9007

ADVANCED PRODUCT DESCRIPTION

CRT Controller

Features

- Fully programmable display format
- Programmable monitor sync. format
- Direct outputs to CRT monitor
- Binary, row-table driven or sequential video addressing modes
- Programmable status row position and address registers
- Bidirectional partial or full page smooth scroll
- Attribute assemble mode
- Double height, double width data row mode
- Programmable DMA burst mode
- Configurable with a variety of memory contention arrangements
- Light pen register
- Maskable processor interrupt line
- Three-state video memory address bus
- Partial or full page blank capability
- Two interlace modes: enhanced video and alternate scan line
- Programmable for horizontal split screen applications
- Graphics compatible
- VT-100 compatible
- RS-170 Interlaced composite sync. available

General Description

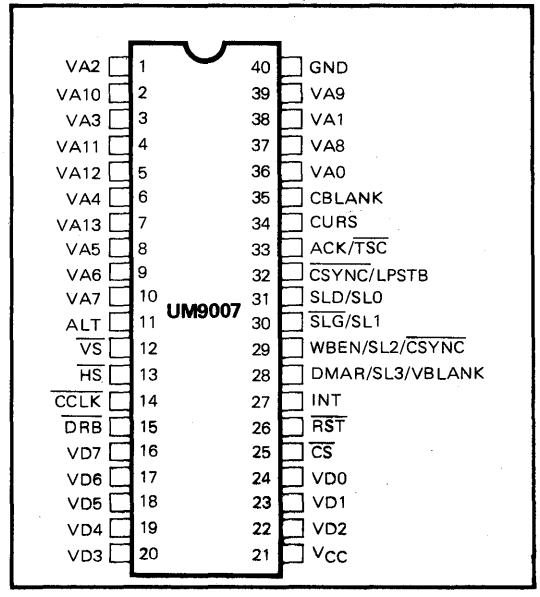
The CRTC UM9007 is a next generation video processor/controller—an MOS LSI integrated circuit which supports either sequential or row-table driven memory addressing modes. As indicated by the features above, the UM9007 provides the user with a wide range of programmable features permitting low cost implementation of high performance CRT systems. Its 14 address lines can directly address up to 16K of video memory. This is equivalent to eight pages of an 80 character by 24 line CRT display. Smooth or jump scroll operations may be performed anywhere within the addressable memory. In addition, status rows can be defined anywhere on the screen.

In the sequential video addressing mode, a Table Start Register points to the address of the first character of the first data row on the screen. It can be easily changed to produce a scrolling effect on the screen. By using this register in conjunction with two auxiliary address registers and two sequential break registers, a screen roll can be produced with a stable status row held at either the first or last data row position.

In the row-table driven video addressing mode, each row in the video display is designated by its own address. This provides the user with greater flexibility than sequential addressing since the rows of characters are linked by pointers instead of residing in sequential memory locations. Operations such as data row insertion, deletion, and replication are easily accomplished by manipulating pointers instead of entire lines. The row table itself can be stored in memory in a linked list or in a contiguous format.

The UM9007 works with a variety of memory contention schemes including operation with a Single Row Buffer, a Double Row Buffer such as the UM8312, or no buffer at all, in which case character addresses are output during each displayable scan line.

User accessable internal registers provide such features as light pen, interrupt enabling, cursor addressing, and CRTC status. Ten of these registers are used for screen formatting with the ability to define over 200 characters per data row and up to 256 data rows per frame. These 10 registers contain the "vital screen parameters".



UM8321

CRT Video Attributes Controller(VAC)

Features

- On chip attributes logic
  - Reverse video
  - Character blank
  - Character blink
  - Underline
  - Full/half intensity
- Four modes of operation
  - Wide graphics
  - Thin graphics
  - Character mode without underline
  - Character mode with underline
- On Chip logic for double height double width characters
- Accepts scan line information in parallel or serial format
- Four cursor modes dynarnically selectable via 2 input pins
  - Underline
  - Blinking underline
  - Reverse video
  - Blinking reverse video
- Programmable character blink rate
- Programmable cursor blink rate
- On chip data and attribute latches
- +5 volt operation
- TTL compatible
- MOS n-Channel silicon gate
- Compatible with UM9007

General Description

The UM8321 Video Attributes Controller (VAC) is an n-channel MOS/LSI device containing graphics logic, attributes logic, data and attributes latches, cursor control and a high speed video shift register. A character generator ROM and a CRT Video attributes controller UM8321 provide all of the major circuitry for the display portion of a CRT video terminal.

The UM8321 serial video output may be connected directly to 3 CRT monitor's video input.

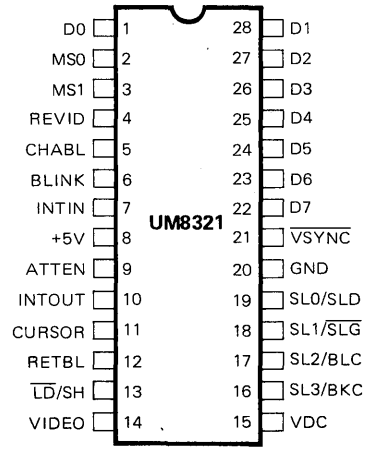
The UM8321 attributes include: reverse video, underline, character blank, character blink, and full/half intensity selection. In addition. When used in conjunction with the UM9007, the UM8321 will provide double height or double width characters.

Four programmable cursor modes are provided on the UM8321. They are underline, blinking underline, reserve video character block, and blinking reverse video character block. When used in the serial scan line input mode, the cursor mode may be selected via two input pins. When used in the parallel scan line input mode, the cursor mode is a mask program option and is fixed at the time of manufacture.

Two graphics modes are provided. In the wide graphics mode, the UM8321 produces a graphic entity the size of the character block. The graphic entity contains eight parts, each of which is associated with one bit of the input byte, thereby providing 256 unique graphic symbols. The thin graphics mode enables the user to create thin line drawings and forms.

In both graphics rnodes, continuous horizontal and vertical lines may be drawn. Additional flexibility is provided by allowing the mask programming of the placement and dimensions of the blocks or lines within a character block. In the thin graphics mode, mask programming allows serrated horizontal or vertical lines.

Pin Configuration



Absolute Maximum Ratings*

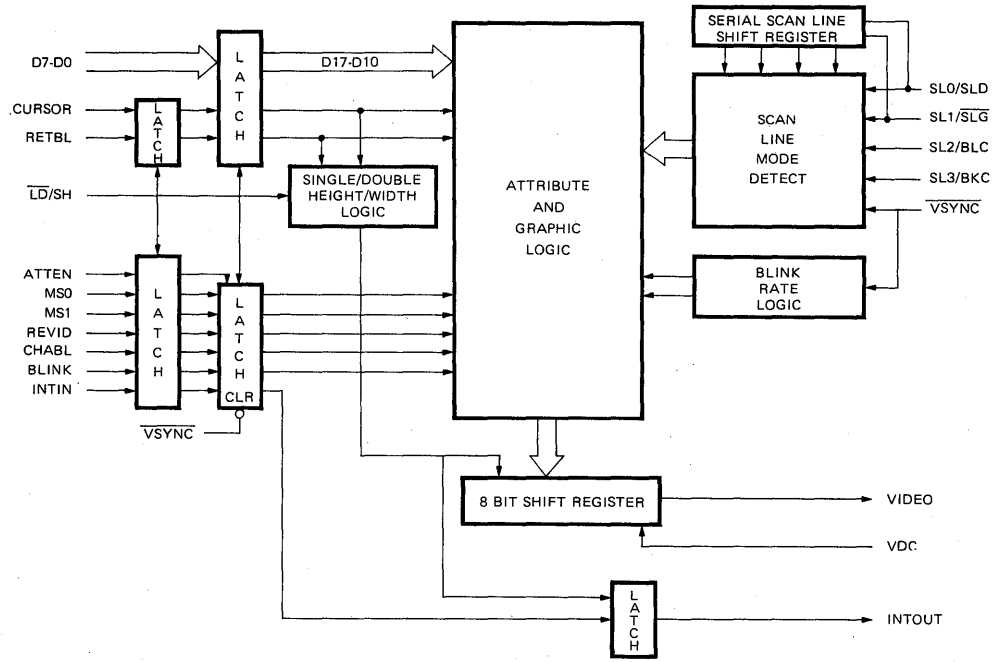
Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . . −55°C to +150°C
Lead Temperature (soldering, 10 sec.) . . . . . +325°C
Positive Voltage on any Pin, with respect to ground . . . . . +8.0V
Negative Voltage on any Pin, with respect to ground . . . . . −0.3V

*Comments

Streeses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

Note: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

Block Diagram



Electrical Characteristics (T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, unless otherwise noted)

D.C. CHARACTERISTICS

Parameter	Min.	Typ.	Max.	Units	Conditions
Input Voltage Levels					
Low Level V_{IL}			0.8	V	
High Level V_{IH1}	2.0			V	All inputs except VDC, $\overline{LD}$/SH
High Level V_{IH2}	4.3			V	For VDC, LD/SH Input
Output Voltage Levels					
Low Level V_{OL}			0.4	V	I_{OL} = 0.4 mA
High Level V_{OH}	2.4			V	I_{OH} = 100μA
Input Leakage Current					
Leakage I_{L1}			10	μA	$0 \leqslant V_{IN} < V_{CC}$; excluding VDC, $\overline{LD}$/SH
Leakage I_{L2}			50	μA	$0 \leqslant V_{IN} < V_{CC}$; for VDC $\overline{LD}$/SH
Input Capacitance					
C_{IN1}		10		pf	Excluding VDC, $\overline{LD}$/SH
C_{IN2}		20		pf	For $\overline{LD}$/SH
C_{IN3}		25		pf	For VDC
Power Supply Current					
I_{CC}		60	80	mA	

A.C. CHARACTERISTICS

Parameter	Min.	Typ.	Max.	Units	Conditions
VDC					
$1/t_{CY1}$ VDC Frequency	1.0		28.5	MHz	
t_{CKL} VDC Low	10			ns	
t_{CKH} VDC High	10			ns	
t_{CKR} VDC Rise Time	10		10	ns	Measured from 10% to 90% points
t_{CKF} VDC Fall Time			10	ns	Measured from 90% to 10% points
$\overline{LD}$/SH					
t_{CY2}	315			ns	
t_{S1}	7			ns	
t_{H1}	0			ns	
Input Setup and Hold					
t_{S2}	35			ns	
t_{H2}	0			ns	
Miscellaneous Timing					
t_{PD}			35	ns	C_L = 15 pf
t_{DW}	t_{CY2}				

Pin Description

Pin No.	Name	Symbol	Functions
1, 28, 27, 26, 25, 24, 23, 22	Data	D7-D0	In the character mode, the data on these inputs is passed through the Attributes logic into the 8 bit high speed video shift register. The binary information on D7 will be the first bit output after the $\overline{LD}$/SH input goes low. In the thin or wide graphics mode these 8 inputs will individually control the on/off condition of the particular portion of the character block of line drawing. Figure 4 and Figure 5 illustrate the wide and thin graphics modes respectively and their relationships to D7-D0.
2 3	Mode Select 0 Mode Select 1	MS0 MS1	These 2 inputs define the four modes of operation of the UM8321 as follows: MS1, MS0 = 00; Wide graphics mode = 10; Thin graphics mode = 01; Character mode without underline = 11; Character mode with underline See section entitled Display Modes for details.
4	Reverse Video	REVID	When this input and Retrace Blank (RETBL) are both low, data from the Attributes and Graphics logic is presented directly to the video shift register. When this input is high and RETBL is low, the Attribute and Graphics logic will invert the data before presenting it to the video shift register.
5	Character blank	CHABL	When this input is high, the parallel inputs to the video shift register are all set low (or high depending on the state of REVID) thus providing a constant video level for the entire length of the character block.
6	Blink	BLINK	When this input is high and both the RETBL and CHABL inputs are low, the character will blink at the programmed character blink rate. Blinking is accomplished by causing the video to go to the background level during the "off" portion of the Character Blink cycle. This video level may be either the white or black level depending on state of REVID. The duty cycle for the character blink is 75/25 (on/off). This input is ignored if it coincides with the CURSOR input and the cursor is formatted to blink.
7	Intensity In	INTIN	The INTIN input along with the INTOUT output provides a user controlled general purpose attribute. Data input to INTIN will appear at INTOUT with the same delay as that from any other attribute input to the serial video output (VIDEO). By using an external mixing circuit, it is possible to raise or lower the voltage level of the video output to produce such attributes as "half intensity" or "intensity".
8	Supply Voltage	+5V	+5 volt power supply.
9	Attribute Enable	ATTEN	When this input is high, the internal attributelatch is updated at the positive going edge of the $\overline{LD}$/SH input with data appearing on the REVID, CHABL, MS1, MS0, BLINK and INTIN inputs. By selectively bringing this input high, the user will update the attribute only at specific character times; all subsequent characters will carry with them the attributes last updated thus allowing "field" or "embedded" attributes. When using a wide video memory where attribute bits are attached to every character, the internal attribute latch may be updated at each character by tieing this input high (thus allowing for "invisible" attributes).
10	Intensity Out	INTOUT	This output is used in conjunction with the INTIN Input to provide a three character pipeline delay to allow for general purpose attributes (such as intensity) to be implemented. See INTIN (pin 7).
11	Cursor	CURSOR	When this input is high and RETBL is low, the programmed cursor format will be displayed. When this input is high, and RETBL is high, the UM8321 enters the double width mode. See section entitled cursor formats for details.

Pin Description (Continued)

Pin No.	Name	Symbol	Functions
12	Retrace Blank	RETBL	When this input is high, the parallel inputs to the video shift register are unconditionally cleared to all zeros and loaded on the next $\overline{LD}$/SH pulse. This forces the VIDEO output to a low voltage level, independent of all attributes, for blanking the CRT during horizontal and vertical retrace time.
13	$\overline{Load}$/Shift	$\overline{LD}$/SH	The 8 bit video shift register parallel-in load or serial-out shift operation is established by the state of this input. When high, this input enables the shift register for serial shifting with each video dot clock pulse (VDC input). When low, the video shift register is parallel loaded on the next video dot clock pulse and all data and attributes are moved to the next position in the internal pipeline. In addition, input data and attributes are latched on the positive transition of $\overline{LD}$/SH.
14	Video	VIDEO	The Video output provides the serial dot stream to the CRT. Video is shifted out on the rising edge of the video dot clock VDC. The timing of $\overline{LD}$/SH input will determine the number of backfill dots. See Figure 1.

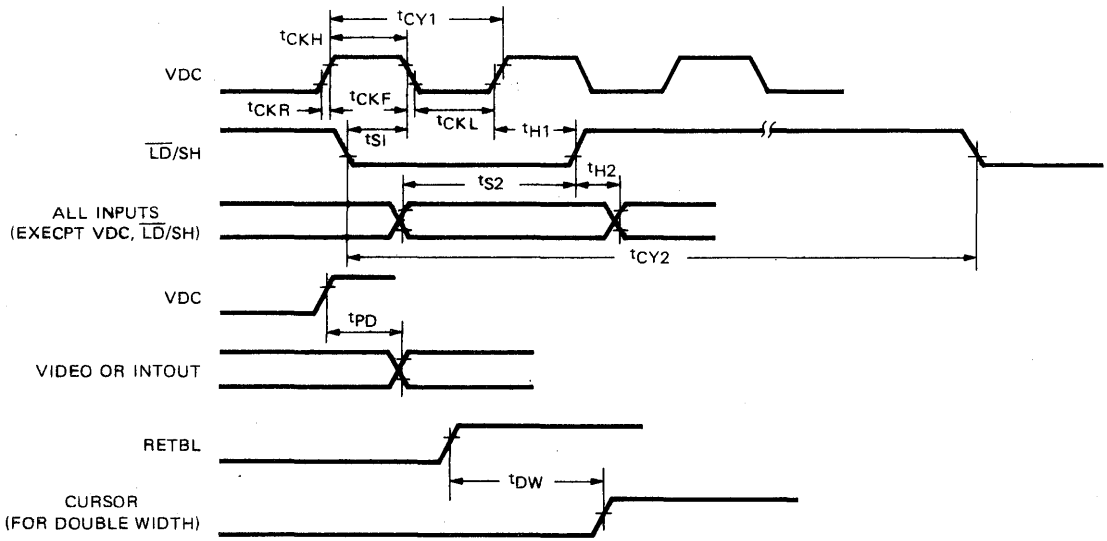


Figure 1. UM8321 Input/Output Timing

PIN No.	Name	Symbol	Functions
15	Video Dot Clock	VDC	This input clock controls the rate at which video is shifted out on the VIDEO output.
16	Scan line 3/Block Cursor	SL3/BKC	This input has two separate functions depending on the way scan line information is presented to the UM8321. Parallel scan line mode – This input is the most significant bit of the binary scan line row address. Serial scan line mode – This input controls the cursor's physical dimensions. If high the cursor will appear as a reverse video block (the entire character cell will be displayed in reverse video). If low, the cursor will appear as an underline on the scan line(s) programmed.

Pin Description (Continued)

Pin No.	Name	Symbol	Functions
17	Scan line 2/Blink Cursor	SL3/BLC	This input has two separate functions depending on the way scan line information is presented to the UM8321. Parallel scan line mode – This input is the second most significant bit of the binary scan line row address. Serial scan line mode – This input if low, will cause the cursor to alternate between normal and reverse video at the programmed cursor blink rate. The duty cycle for the cursor blink is 50/50 (on/off). If this input is high, the cursor will be non-blinking.
18	Scan Line 1/Scan Line Gate	SL1/$\overline{SLG}$	This input has two separate functions depending on the way scan line information is presented to the UM8321. Parallel scan line mode – This input is the next to the least significant bit of the binary scan line row address. Serial scan line mode – This input will be low for 5 or 6 LD/SH pulses to allow the scan line information to be serially shifted into the serial scan line shift register. If this signal is low for 7 or more $\overline{LD}$/SH pulses, the UM8321 will assume the parallel input scan line row address mode.
19	Scan line 0/Scan Line data	SL0/SLD	This input has two separate functions depending on the way scan line information is presented to the UM8321. Refer to Figure 2. Parallel scan line mode – This input is the least significant bit of the binary scan line row address. Serial scan line mode – This input will present the scan line information in serial form (least significant bit first) to the UM8321 and permits the proper scan line information to enter the serial scan line shift register during the $\overline{LD}$/SH pulses framed by $\overline{SLG}$ (pin 18).

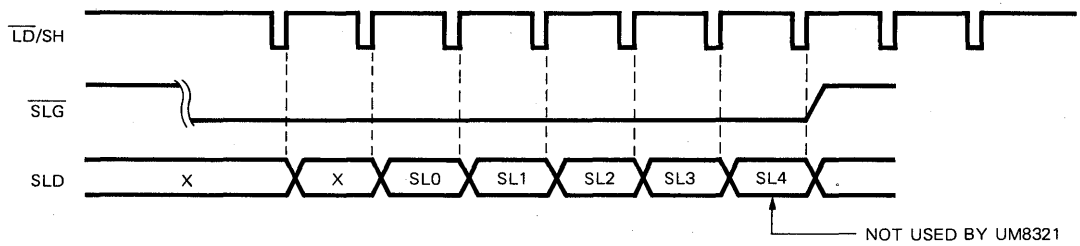


Figure 2. Serial Scan Line Mode Timing

PIN No.	Name	Symbol	Functions
20	Ground	GND	Ground
21	Vertical Sync	$\overline{VSYNC}$	This input is typically connected to the vertical sync output of the CRT controller and is used as the clock input for the two on-chip mask programmable blink rate dividers. The cursor blink rate (50/50 duty cycle) will always be twice the character blank rate (75/25 duty cycle). In addition, the internal attributes are reset when this input is low. The $\overline{VSYNC}$ input is also used to determine the scan line mode (parallel or serial) used. See the section "Scan Line Input Modes".

Attributes Function

Retrace Blank – The RETBL input causes the VIDEO to go to the zero (black) level regardless of the state of all other inputs.

Reverse Video – The REVID input causes inverted data to be loaded into the video shift register.

Character Blank – The CHABL input forces the video to go to the current background level as defined by Reverse Video.

Underline – MS1, MS0 = 1, 1 forces the video to go to the inverse of the background level for thescan lines(s) programmed for underline.

Blink – The BLINK input will cause characters to blink by forcing the video to the background level 25% of the time and allowing the normal video for 75% of the time. When the cursor is programmed to blink (not controlled by the BLINK input), the video alternates from normal to reverse video at 50% duty cycle. The cursor blink rate always overrides the character blink rate when they both appear at the same character position.

Intensity (Half Intensity) – The INTIN input and the INTOUT output allow an intensity (or half intensity) attribute to be carried through the pipeline of the UM8321. An external mixer can be used to combine VICEO and INTOUT to create the desired video level. See Figure 3a and Figure 3b.

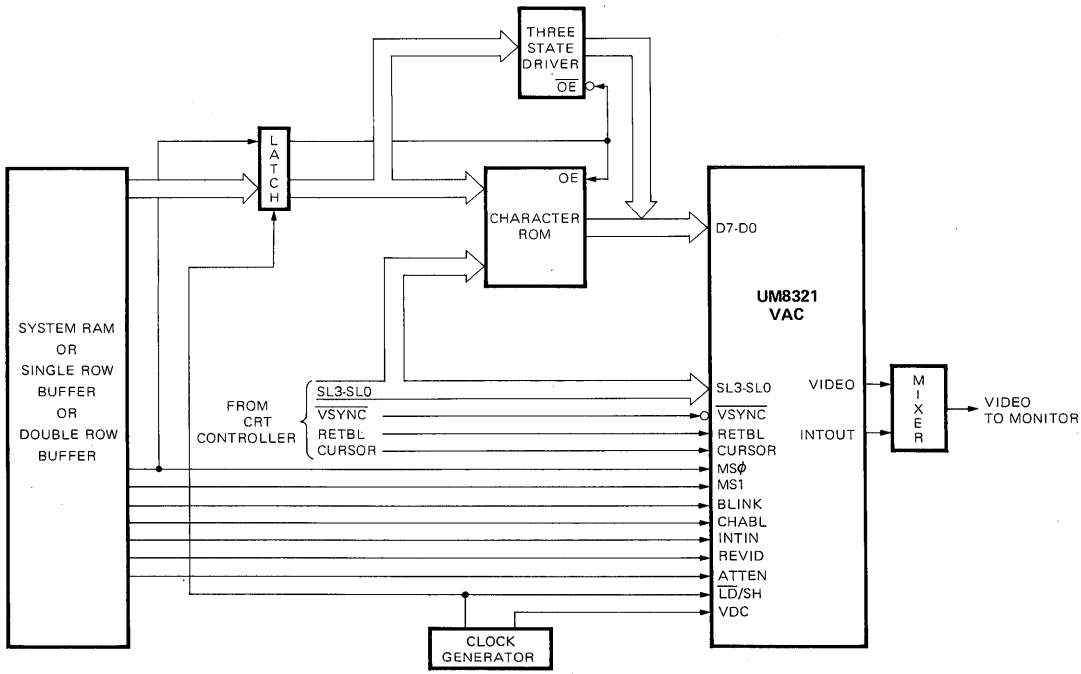


Figure 3a: UM8321 System Configuration in Parallel Scan Line Mode

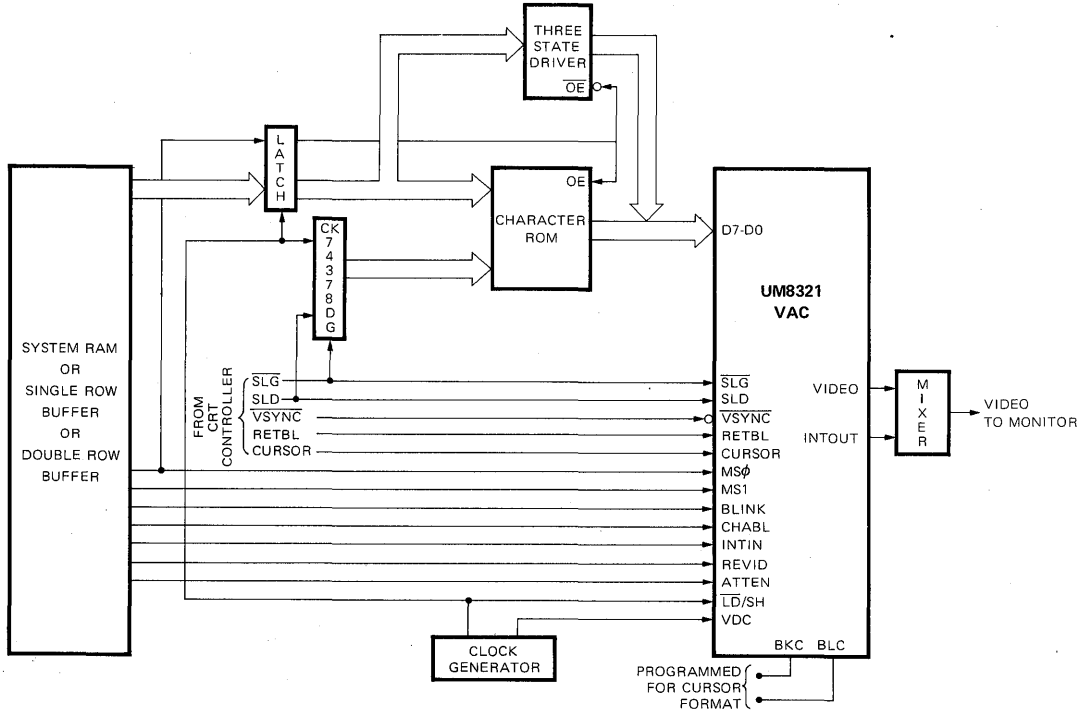


Figure 3b: UM8321 System Configuration in Serial Scan Line mode

Table 1 illustrates the effect of the REVID, CHABL, UNDLN attributes as a function of the cursor format and the CURSOR and RETBL inputs.

Table 1. UM8321 Attribute Combinations

Cursor Format	UM8321 Inputs					Video Shift Register Loaded With
	Retbl	Cursor	Revid	Chabl	Undln	
x	1	x	x	x	x	All zero's
	0	0	0	0	0	Data
	0	0	0	0	1	$\overline{DATA}$ for selected scan line(s); Data for all other scan lines
	0	0	0	1	x	All zero's
	0	0	1	0	0	$\overline{DATA}$
	0	0	1	0	1	$\overline{DATA}$ for selected scan line(s); data for all other scan lines
	0	0	1	1	x	One's for all scan lines
Underline[2]	0	1	0	0	x[1]	$\overline{DATA}$ for selected scan line(s) for cursor; data for all other scan lines
	0	1	0	1	x[1]	One's for selected scan line(s) for cursor; zero's for all other scan lines
	0	1	1	0	x[1]	$\overline{DATA}$ for selected scan line(s) for cursor; Data for all other scan lines
	0	1	1	1	x[1]	Zero's for selected scan line(s) for cursor; one's for all other scan lines

Table 1. UM8321 Attribute Combinations (Continued)

Cursor Format	UM8321 Inputs					Video Shift Register Loaded with	
	Retbl	Cursor	Revid	Chabl	UndIn		
Blinking[3] Underline[2]	0	1	0	0	x[1]	$\overline{\text{DATA}}$ for selected scan line(s) blinking; Data for all other scan lines.	
	0	1	0	1	x[1]	One's for selected scan line(s) blinking; zero's for all other scan lines.	
	0	1	1	0	x[1]	DATA for selected scan line(s) blinking; $\overline{\text{Data}}$ for all other scan lines.	
	0	1	1	1	x1	Zero's for selected scan line(s) blinking; one's for all other scan lines.	
Revid Block	0	1	0	0	0	$\overline{\text{Data}}$ for all scan lines.	
	0	1	0	0	1	Data for selected scan line(s) for underline; $\overline{\text{data}}$ for all other scan lines.	
	0	1	0	1	x	One's for all scan lines.	
	0	1	1	0	0	Data for all scan lines	
	0	1	1	0	1	$\overline{\text{DATA}}$ for selected scan line(s) for underline; data for all other scan lines	
	0	1	1	1	x	Zero's for all scan lines	
Blinking[3] Revid Block	0	1	0	0	0	On $\overline{\text{Data}}$ for all scan lines	Off Data for all scan lines
	0	1	0	0	1	Data for selected scan line(s) for underline; $\overline{\text{Data}}$ for all other scan lines	$\overline{\text{Data}}$ for selected scan line(s) for underline; Data for all other scan lines
	0	1	0	1	x	One's for all scan lines	Zero's for all scan lines
	0	1	1	0	0	Data for all scan lines	$\overline{\text{Data}}$ for all scan lines
	0	1	1	0	1	$\overline{\text{DATA}}$ for selected scan line(s); Data for all other scan lines	DATA for selected scan line(s); $\overline{\text{Data}}$ for all other scan lines
	0	1	1	1	x	Zero's for all scan lines	One's for all scan lines

1 – if the programmed scan line(s) for cursor and underline coincide, the cursor takes precedence; otherwise both are displayed.

2 – at programmed scan line(s) for underline

3 – at cursor blink rate

Note: cursor blink rate overrides character blink rate.

Display Modes

Inputs MS1 and MS0 select one of four display modes. All attributes except underline operate independent of the display mode used. Figures 3a and 3b illustrate a typical UM8321 configuration which operates in all display modes for both the parallel and serial scan line modes respectively.

MS1, MS0 = 00 — Wide Graphics Mode.
— In this display mode, inputs D7-D0 define a graphics entity as illustrated in figure 4. Note that individual bits in D7-D0 will illuminate particular portion of the character block. Table 2 shows all programming ranges possible when defining the wide graphic boundaries. No underline is possible in this display mode.

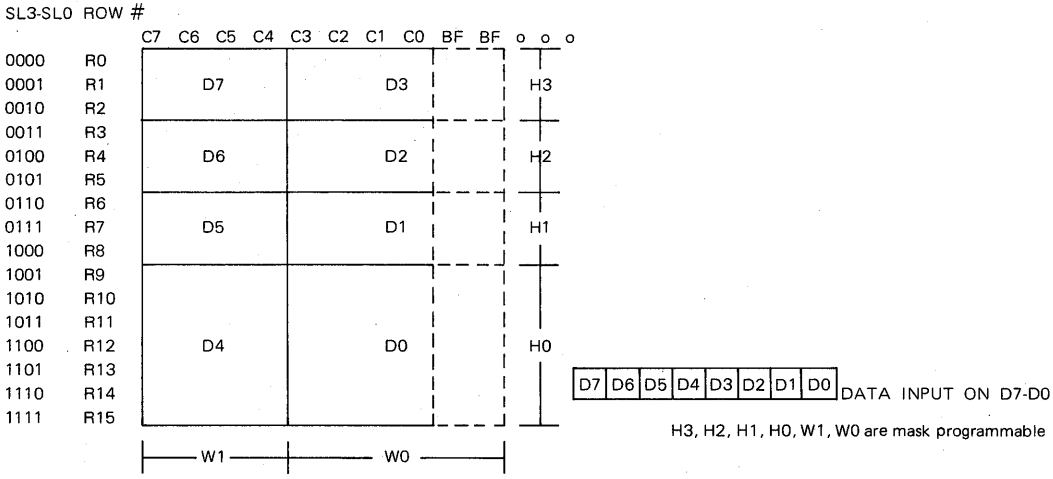


Figure 4. Wide Graphics Mode for Standard UM8321

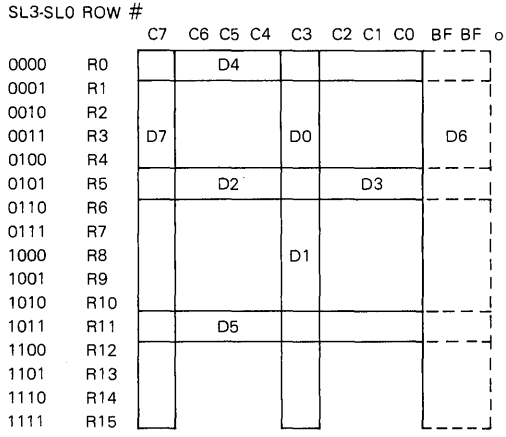
Table 2. Wide Graphics Mask Programming Options

Options	Choices	Standard UM8321
Height of graphic block*		
D7 and D3	any scan line(s)	R0, R1, R2
D6 and D2	any scan line(s)	R3, R4, R5
D5 and D1	any scan line(s)	R6, R7, R8
D4 and D0	any scan line(s)	R9, R10, R11, R12, R13, R14, R15
Width of D7, D6, D5, D4**	any number of dots 0 to 8	C7, C6, C5, C4
Width of D3, D2, D1, D0**	any number of dots 0 to 8	C3, C2, C1, C0, BF

* Any graphic block pair can be removed by programming for zero scan lines.

** Total number of dots for both must be equal to the total dots per character with no overlap.

MS1, MS0 = 10 — Thin Graphics Mode.
In this display mode, inputs D7-D0 define a graphic entity as illustrated in figure 5. Note that individual bits in D7-D0 will illuminate particular horizontal or vertical line segments within the character block. Table 3 shows all programming ranges possible when defining the thin graphics boundaries. No underline is possible in this display mode.



HORIZONTAL LENGTH VERTICAL POSITION

D2	C7-C3	PROGRAMMABLE
D3	C3-BF	PROGRAMMABLE
D4	C7-BF*	PROGRAMMABLE
D5	C7-BF*	PROGRAMMABLE

VERTICAL HEIGHT HORIZONTAL POSITION

D0	R0-R5	PROGRAMMABLE
D1	R6-R15	PROGRAMMABLE
D6	R0-R15*	PROGRAMMABLE
D7	R0-R15*	PROGRAMMABLE

D7	D6	D5	D4	D3	D2	D1	D0

DATA INPUT ON D7-D0

* These values are fixed

Figure 5. Thin Graphics Mode for Standard UM8321

Table 3. Thin Graphics Mask Programming Options

Options	Choices	Standard UM8321
Backfill	C1 or C0	C0
Horizontal position for		
D2 and D3	any scan line(s) R0-R15	R5
D4	any scan line(s) R0-R15	R0
D5	any scan line(s) R0-R15	R11
Horizontal length for		
D2[2]	any continuous dots C7-C0, BF	C7-C3
D3[2]	all dots not covered by D2	C3-BF
Blanked dots for serrated horizontal lines		
D2	any dot(s) C7-C0, BF	none
D3	any dot(s) C7-C0, BF	none
D4 and D5	any dot(s) C7-C0, BF	none
Vertical position for		
D0 and D1	any dot(s) C7-C0, BF	C3
D6[1]	any dot(s) C6-C0, BF	BF
D7[1]	any dot(s) C7-C0	C7
Vertical length for		
D0	any scan line(s)	R0 to R5
D1	all scan lines not used by D0	R6 to R15
D6	no choice; always R0-R15	R0 to R15
D7	no choice; always R0-R15	R0 to R15

1 — D7 must always come before D6 With no overlap; otherwise D6 is lost.

2 — D2 and D3 must always over only one dot.

MS1, MS0 = 01 — Character Mode Without Underline. In this display mode, inputs D7-D0 go directly from the input latch to the video shift register via the Attributes and Graphics logic. This mode requires either a bit mapped system RAM (1 bit in RAM equals 1 pixal on the CRT) or an external character generator as shown in figures 3a and 3B.

MS1, MS0 = 11 — Character Mode With Underline. Same operation as MS1, MS0 = 01 with the underline attribute appearing on the scan line(s) mask programmed.

BACKFILL

Backfill is a mechanism that allows a character width of greater than 8 dots and provides dot information (usually blanks) for all dot positions beyonds 8. The character width is defined by the period of the $\overline{LD}$/SH input. For the character modes, backfill is added to the tail end of the character by two methods which are mask programmable.

Method A — The backfill (BF) dots will be the same as the dot displayed in position C7.

Method B — The backfill (BF) dots will be the same as the dot displayed in position C0.

For the wide graphics mode, the backfill dots will always be the same as the dot displayed in position C0 (method B) with no programmable option.

CURSOR FORMATS

Four cursor formats are possible with the UM8321. If the parallel scan line input mode is used, one of four cursor formats may be selected as a mask programmed option. If the serial scan line input mode is used, the cursor format is selected via input pins 16 and 17 (SL3/BKC, SL2/BLC). See Table 4. The four cursor modes are as follows:

Table 4. Cursor Formats

Scan Line Input Mode	Pin 17	Pin 16	Cursor Function
Serial	1	0	Underline
	1	1	Reverse Video Block
	0	0	Blinking Underline
	0	1	Blinking Reverse Video Block
Parallel	x	x	Mask programmable Only

Underline — The cursor will appear as an underline. The position and width of the cursor underline is mask programmed.

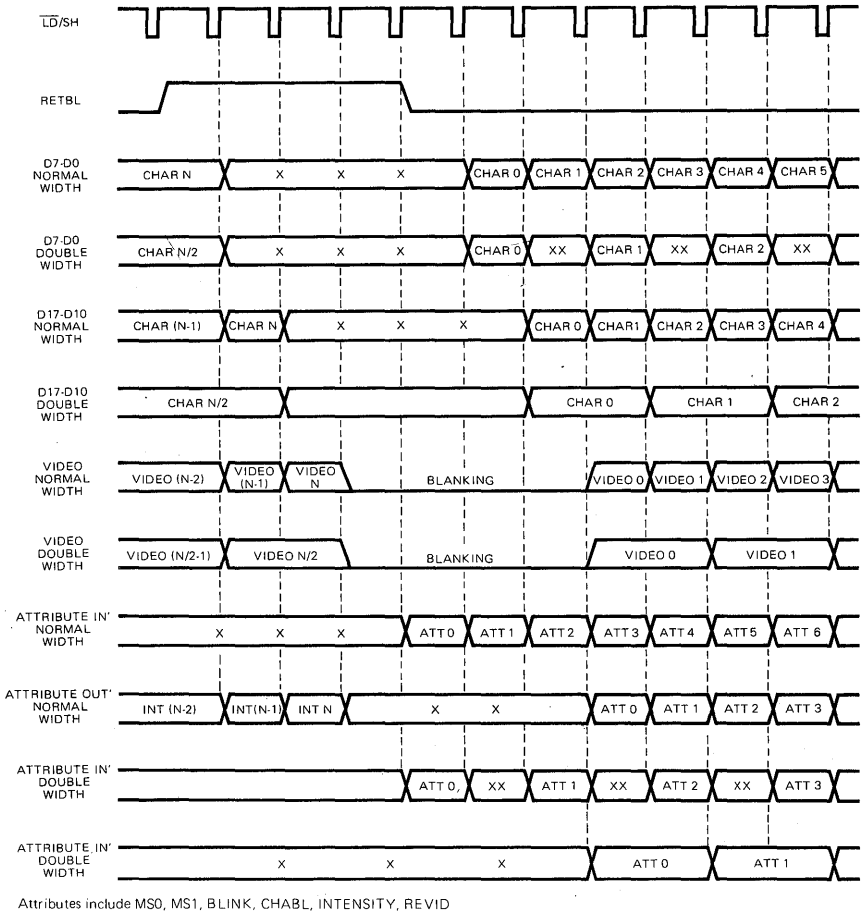
Blinking Underline — The cursor will appear as an underline. The underline will alternate between normal and reverse video at the mask programmed cursor blink rate.

Reverse Video Block — The cursor will appear as a reverse Video Block (The entire character cell will be displayed in reverse video).

Blinking Reverse Video Block — The cursor will appear as a reverse video block and the entire block (character plus background) will alternate between normal and reverse video at the masked programmed cursor blink rate.

Double Width Mode

In order to display dobuble width characters, video must be shifted out at half frequency and the video shift register must receive new information (parallel load) every other $\overline{LD}$/SH input pulse. In order to divide the video dot clock (VDC) and the $\overline{LD}$/SH pulse internally at the proper time, the cursor input should be pulsed during RETBL prior to the scan line to be displayed as double width. The CURSOR input must remain low for a minimum of 1 $\overline{LD}$/SH period from the leading edge of RETBL. The CURSOR input can stay high for the entire RETBL time but should not extend into active video. If it does, a cursor will be displayed. It is assumed that the CRT controller knows when a particular scan line should be double width and it should activate the CURSOR in the manner just described. Double height/double width characters can also be displayed if the scan line count is incremented by the CRT controller every other scan line. With respect to the UM8321, no distinction between double width and double height display is necessary. Figure 6 illustrates timing for both single and double width modes. The UM9007, which supports double height double width characters, will produce the CURSOR signal as required by the UM8321 with no additional hardware.



Attributes include MS0, MS1, BLINK, CHABL, INTENSITY, REVID

Figure 6. UM8321 Functional I/O Timing

Scan Line Input Modes

Scan line information can be introduced into the UM8321 in parallel format or serial format. Table 5 illustrates the pin definition as a function of the scan line input mode. The UM8321 will automatically recognize the proper scan line mode by observing the activity on pin 18. In parallel mode, this input will be stable for at least 1 scan line and in serial mode this input will remain low for about 5 or 6 $\overline{LD}$/SH periods. If pin 18 goes active low for less than seven but more than two continuous $\overline{LD}$/SH periods during the last scan line that has an active low on the $\overline{VSYNC}$ input, the serial mode will be locked in for the next field. The parallel scan line input mode will be selected for the next field if the following two condition occur during $\overline{VSYNC}$ low time. First, at least one positive transition must occur on pin 18 and second, pin 18 must be low for seven or more $\overline{LD}$/SH periods. Refer to Figure 7 for timing details.

Table 5. Pin Definition for Parallel and Serial Scan Line Modes

Scan Line Input Mode	UM8321 Pin Number			
	19	18	17	16
Serial	SLD	$\overline{SLG}$	BLC	BKC
Parallel	SL0	SL1	SL2	SL3

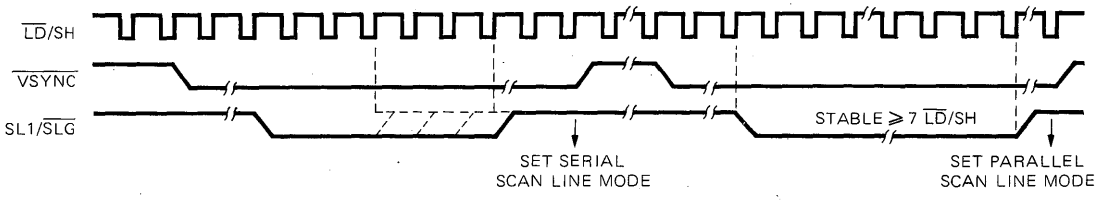


Figure 7. Serial/Parallel Scan Line Mode Selection Timing

Program Otpions

The UM8321 has a variety of mask programmed options. Tables 2 and 3 illustrate the range of these options for the wide and thin graphics modes respectively. Table 6 illustrates the range of the miscellaneous mask programmed options. In addition, Table 2, 3 and 6 show the mask programmed options for the standard UM8321.

Table 6. Miscellaneous Mask Programming Options

Options	Choices	Standard UM8321
Backfill in character mode	C7 or C0	C7
Character blink rate (division of VSYNC frequency)	8 to 60; divisible by 4 (7.5 Hz to 1 Hz)[1]	32 (1.875 Hz)[1]
Cursor blink rate[2]	Twice the character blink rate	16 (3.75 Hz)[1]
Character underline position	any scan line(s) R0-R15	R11
Cursor underline[3]	any scan line(s) R0-R15	not applicable
Cursor format[4]	Underline Blinking underline Reverse video block Blinking reverse video block	Blinking reverse video block

1 – Assumes VSYNC input frequency of 60 Hz.
2 – Valid only if the cursor is formatted to blink.
3 – Valid only if the cursor is formatted for underline.
4 – Valid for the parallel scan line mode only.

Ordering Information

Part No.	Operation Option	Package Type
8321A	30 MHz	Plastic
8321B	28.5 MHz	Plastic

UM8312

Double Row Buffer(DRB)

Features

- Low cost solution to CRT memory contention problem
- Provides enhanced processor throughput for CRT display systems
- Replaces shift registers or several RAM and counter IC's in CRT display system
- Permits display of one data row while next data row is being loaded
- Data may be written into buffer at less than the video painting rate
- Double data row buffer permits second data row to be loaded anytime during the display of the preceding data row
- Permits active video on all scan lines of data row
- Dynamically variable number of characters per data Row—. . . 64, 80, 132, ... up to a maximum of 135
- Cascadable for data rows greater than 135 characters
- Stackable for "Invisible Attributes" or character widths of greater than 8 Bits
- Three-state outputs
- Up to 4 MHz read/write data rate
- Compatible with UM9007 and other CRT controllers
- 28 pin dual-in-line package
- +5 volt only power supply
- TTL compatible

General Description

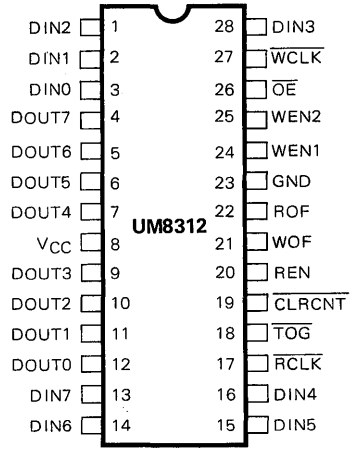
The UM8312 Double Row Buffer (RDB) provides a low cost solution to memory contention between the system processor and the CRT controller in video display systems.

The UM8312 DRB is a RAM-based buffer which provides two rows of buffering. It appears to the system as two octal shift registers of dynamically variable length (2-135 bytes) plus steering logic.

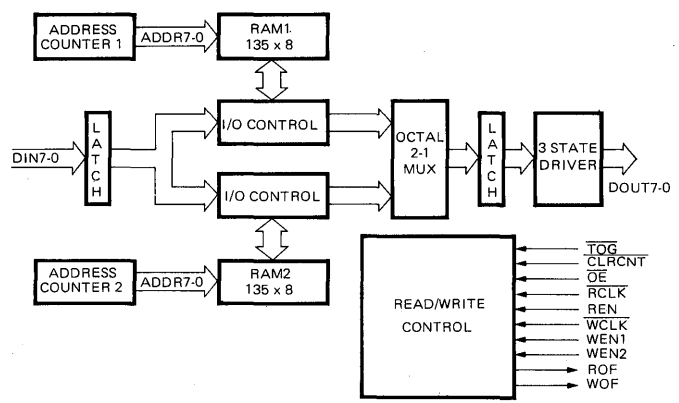
The UM8312 permits the loading of one data row while the previous data row is being displayed. The loading of data may take place during any of the scan line times of the data row. This relaxed time-constraint allows the processor to perform additional processing on the data or service other high priority interrupt conditions (such as a Floopy Disk DMA request) which may occur during a single video scan line. The result is enhanced processor throughput and flicker-free display of data.

CRT Controller

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Operating Temperature Range . . . . . 0°C to + 70°C
Storage Temperature Range . . . . . −55°C to + 150°C
Lead Temperature (soldering, 10 sec.) . . . . . +325°C
Positive Voltage on any Pin, with respect to ground . . . . . +8.0V
Negative Voltage on any Pin, with respect to ground . . . . . −0.3V

*Comments

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics (T_A = 0°C to 70°C, V_{CC} = +5V ± 5%)

D.C. CHARACTERISTICS

Parameter	Min.	Typ.	Max.	Units	Conditions
INPUT VOLTAGE LEVELS					
Low Level V_{IL}			0.8	V	
High Level V_{IH1}	2.0			V	excluding $\overline{RCLK}$; $\overline{WCLK}$
High Level V_{IH2}	4.2			V	$\overline{RCLK}$, $\overline{WCLK}$
OUTPUT VOLTAGE LEVELS					
Low Level V_{OL}			0.4	V	
High Level V_{OH}	2.4			V	
INPUT LEAKAGE CURRENT					
High Leakage I_{LH1}			10	μA	excluding $\overline{OE}$
Low Leakage I_{LL1}			10	μA	excluding WEN1
High Leakage I_{LH2}			400	μA	WEN1
Low Leakage I_{LL2}			400	μA	$\overline{OE}$
INPUT CAPACITANCE					
C_{IN1}		10		pF	excluding $\overline{RCLK}$, $\overline{WCLK}$
C_{IN2}		15		pF	$\overline{RCLK}$, $\overline{WCLK}$
POWER SUPPLY CURRENT					
I_{CC}		100	140	mA	

A.C. CHARACTERISTICS

Parameter	Min.	Typ.	Max.	Units	Conditions
t_{CYW}	300			ns	Write clock period
t_{CYR}	300			ns	Read clock period
t_{CKH}	247		DC	ns	
t_{CKL}	33			ns	
t_{CKR}			10	ns	measured from 10% to 90% points
t_{CKF}			10	ns	measured from 90% to 10% points
t_{DS}	50			ns	referenced to $\overline{WCLK}$
t_{DH}	0			ns	referenced to $\overline{WCLK}$
t_{EN1}[2]	0			ns	
t_{EN2}[2]	100			ns	
t_{ENH}[2]	0			ns	
t_{DV}			175	ns	C_L = 50pF; referenced from $\overline{RCLK}$
t_{DOFF}			175	ns	
t_{DON}			175	ns	
t_{OF}[3]			175	ns	C_L = 30pF
t_{CS}	100			ns	
t_{CH}	0			ns	
t_{WT}[4]		$1t_{CYW}$			

1 – Reference points for all AC parameters are 2.4V high and 0.4V low.
2 – For REN, referenced from $\overline{RCLK}$; for WEN1 or $\overline{WEN2}$ referenced to $\overline{WCLK}$.
3 – For ROF, referenced from $\overline{RCLK}$; for WOF referenced from $\overline{WCLK}$.
4 – At least 1 WCLK rising edge must occur between $\overline{CLRCNT}$ or $\overline{TNG}$ (whichever occurs last) and WEN (= WEN1-WEN2).

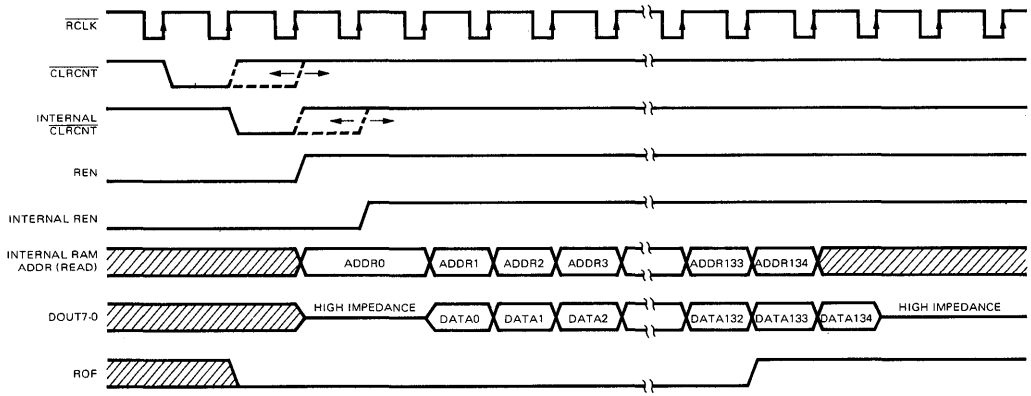


Figure 1. UM8312 Double Row Buffer Read Timing

Pin Description

Pin No.	Name	Symbol	Functions
3-0, 28, 16-13	Data inputs	DIN0-DIN7	DIN DIN7 are the data inputs from the system memory.
12-9, 7-4	Data outputs	DOUT0-DOUT7	DOUT0-DOUT7 are the data outputs from the UM8312 internal data output latch. Valid information will appear on DOUT0-DOUT7 two RCLK periods after the rising edge of REN. This introduces two pipeline delays when supplying data to the character generator.
17	Read Clock	RCLK	RCLK increments the current "read" address register, clocks data through the "read" buffer and moves data through the internal pipeline at the trailling edge. See Figure 1.
18	Toggle Signal	TOG	TOG alternates the function of each buffer between read and write. TOG normally occurs at every data row bundary. Switching of the buffers occurs when both TOG and CLRCNT are low. See Figure 2.
19	Clear Counter	CLRCNT	Clear Counter clears the current "read" address counter at the next RCLK positive edge. CLRCNT is normally asserted low at the beginning of each horizontal retrace interval. CLRCNT clears the current "write" address counter when the TOG is active.
20	Read Enable	REN	REN enables the loading of data from the selected "read" buffer into the output latch. Data is loaded when Read Clock is active.
21	Write Overflow	WOF	WOF high indicates that data is being written into the last memory position (position 135). When WOF is high, further writing into the selected "write" buffer is disabled. WOF may be connected to the WEN1 or WEN2 inputs of a second UM8312 for cascaded operation where data row lengths of greater than 135 characters are desired. See Figure 3.
22	Read Overflow	ROF	The Read Overflow output is high when data is being read from the last memory position (position 135). ROF high disables further reading from the selected "read" buffer. ROF may be connected to the REN input of a second UM8312 for cascaded operation where data row lengths of greater than 135 characters are desired. DOUT0-7 will switch into a high impedance state at the second positive transition of RCLK after ROF goes high. See Figure 3.
24, 25	Write Enable	WEN1, WEN2	WEN allows input data to be written into the selected "write" buffer during WCLK active. Both WEN1 and WEN2 must be high to enable writing. WEN1 has an internal pullup resistor allowing it to assume a high if pin 24 is left open.
26	Output Enable	OE	When the OE input is low the data outputs DOUT0-DOUT7 are enabled. When OE is high, DOUT0-DOUT7 present a high impedance state. OE has an internal pulldown resistor allowing it to assume a low if pin 26 is left open.
27	Write Clock	WCLK	WCLK clocks input data into the selected "write" buffer and increments the current "write" address register when WEN1 and WEN2 are high.
8	Power Supply	V_{CC}	+5 Volt supply
23	Ground	GND	Ground

Operational Description

Block diagram illustrates the internal architecture of the UM8312. It contains 135 bytes of RAM in each of its two buffers. In normal operation, data is written into the input latch on the positive-going edge of Write Clock ($\overline{WCLK}$). When both Write Enable (WEN1, WEN2) signals go high, the next $\overline{WCLK}$ causes data from the input latch to be written into the selected buffer (1 or 2) and the associated address counter to be incremented by one. Loading of the selected RAM buffer continues until WEN goes inactive or until the buffer has been fully loaded. At the next data row boundary, the Toggle Signal ($\overline{TOG}$) will go low. When Clear Counter ($\overline{CLRCNT}$) goes low, the next Read Clock ($\overline{RCLK}$) will begin to reset both buffer address counters to zero, switching the buffer just loaded from a "write buffer" to a "read buffer", permitting the next row of data to be written into the other buffer. Data from the current "read" buffer is read out of the buffer and to the output latch whenever Read Enable (REN) is high during a Read Clock ($\overline{RELK}$). Each read-out from the buffer RAM causes the "read" address counter to be incremented. REN is normally high during the entire visible line time of each scan line of the data row. $\overline{CLRCNT}$ resets the present "read" address counter. The negative edge of $\overline{CLRCNT}$ is detected by the UM8312 and the internal "read" address counter is cleared independent of the $\overline{CLRCNT}$ pulse width. The $\overline{CLRCNT}$ input may be tied to the REN input for proper operation.

Figures 1 and 2 illustrate the functional timing for reading and writing the UM8312. It is possible to cascade two or more UM8312's to allow for data storage greater than 135 bytes by employing the read overflow (ROF) and write overflow (WOF) outputs. Figure 3 illustrates two UM8312's cascaded together.

The UM8312 is compatible with the UM9007 video processor and controller (VPAC^{TM}) and the UM9021 video attributes controller (VAC). A typical video configuration employing the three parts is illustrate in figure 4.

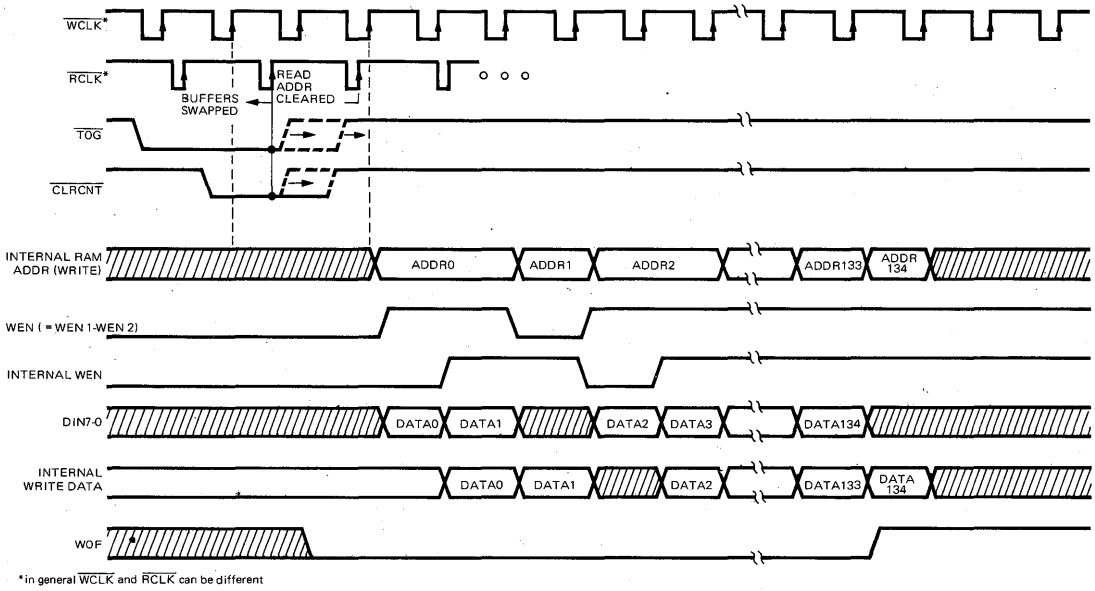


Figure 2. UM8312 Double Row Buffer Write Timing

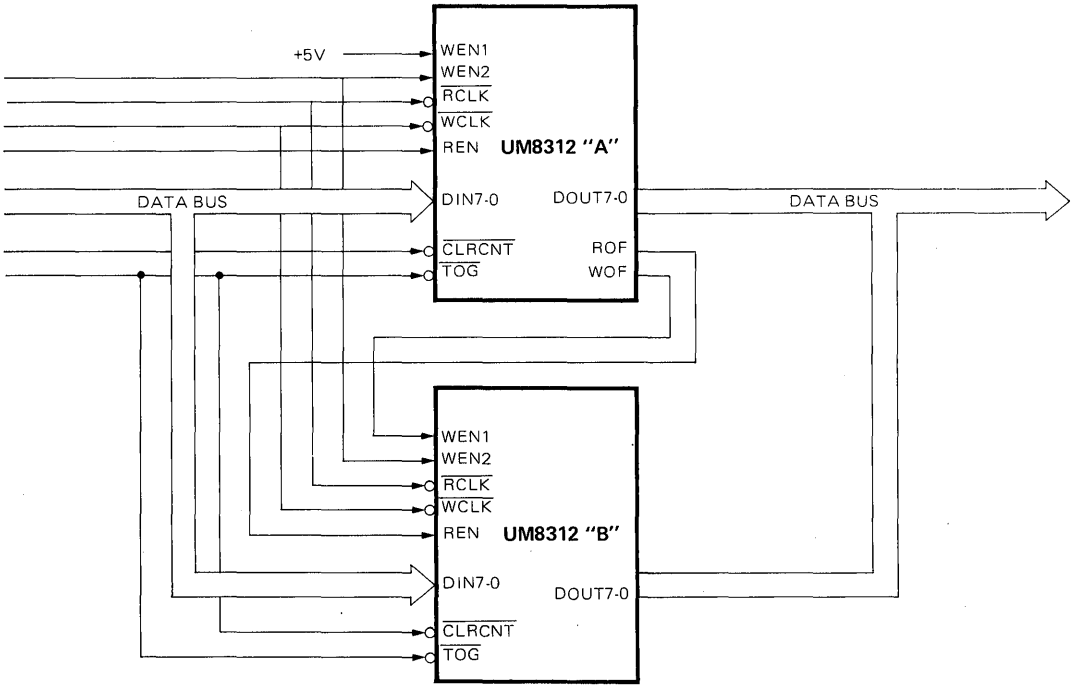


Figure 3. UM8312 Cascaded Configuration For Data Row Lengths Up To 270 Characters

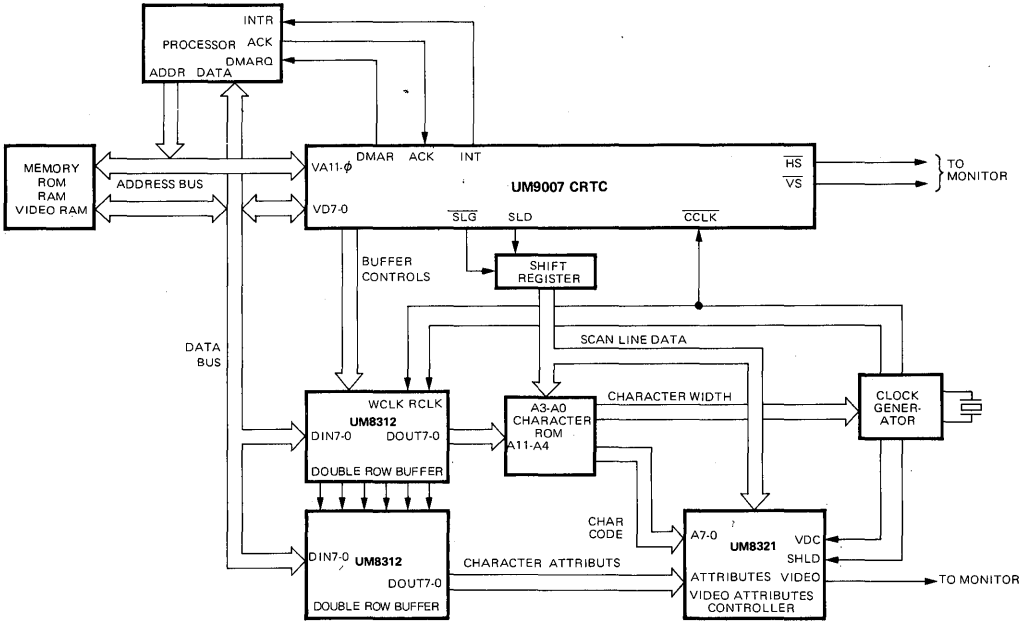


Figure 4. UM8312 Configured With The UM9007 CRTC And The UM8321 CRT VAC

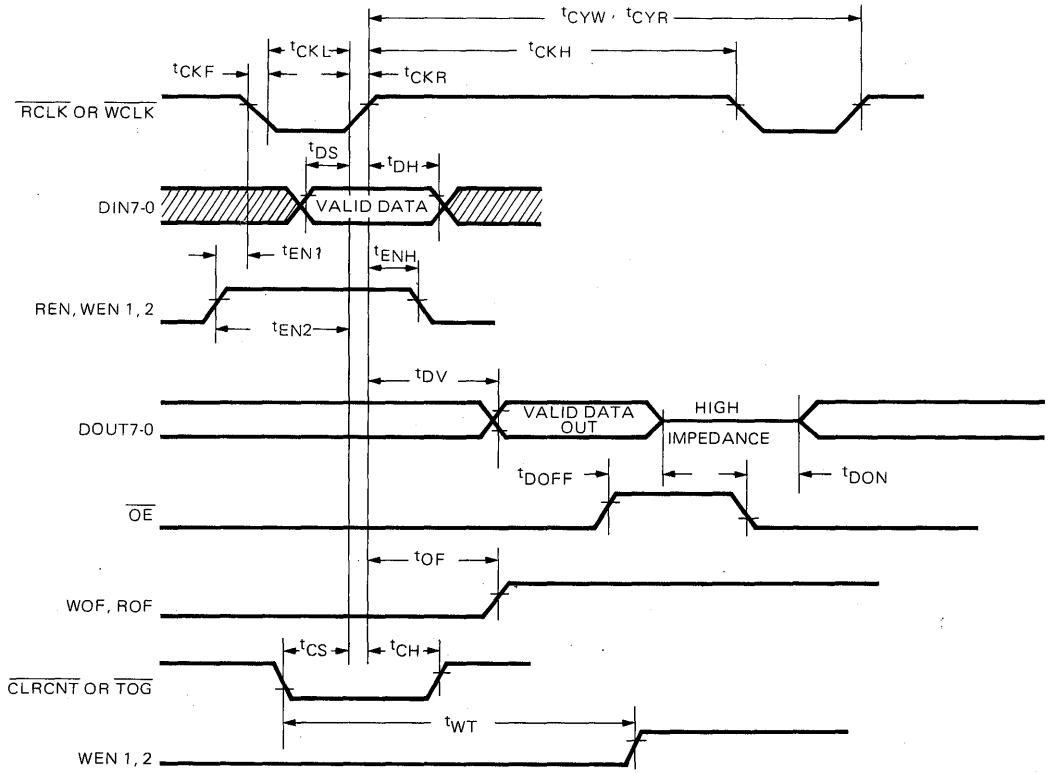


Figure 5. UM8312 I/O Timing

Floppy Disk Controller

Selection Guide

Part No.	Descriptions	Compatible Devices	Remarks	Page
UM8272A	Floppy Disk Controller	μPD 765A	4, 8 MHz Version	6–3
UM9228-1	Floppy Data Separator	–	Special Design for IBM PC	6–24
UM8326/B	Floppy Data Separator	WD 9216	4, 8 MHz Version	6–29
UM8329/T/B/BT	Floppy Data Separator	SMC 9229	Clock/X' TL Input 8, 16 MHz Version	6–34

UM8272A/UM8272A-4

Floppy Disk Controller

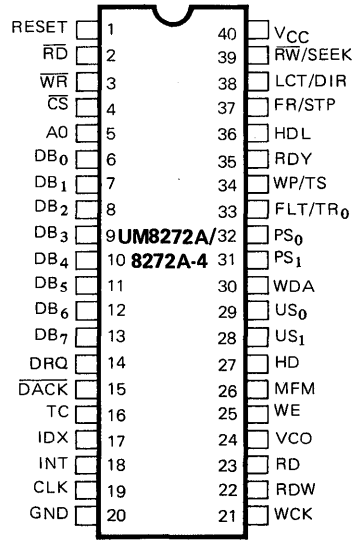
Features

- IBM Compatible in Both Single and Double Density Recording Formats
- Programmable Data Record Lengths: 128, 256, 512, or 1024 Bytes/Sector
- Multi-Sector and Multi-Track Transfer Capability
- Drives Up to 4 Floppy or Mini-Floppy Disks
- Data Transfers in DMA or Non-DMA Mode
- Parallel Seek Operations on Up to Four Drives
- Compatible with all intel and Most Other Microprocessors
- Single-Phase 8MHz/4MHz Clock for UM8272A/UM8272A-4 respectively
- Single + 5 Volt Power Supply (± 10%)

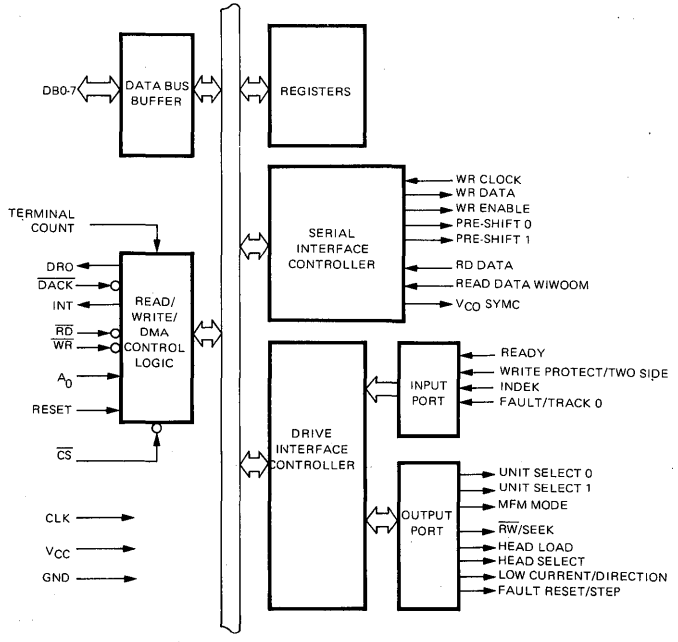
General Description

The UM8272A is an LSI Floppy Disk Controller (FDC) Chip, which contains the circuitry and control functions for interfacing a processor to 4 Floppy Disk Drives. It is capable of supporting either IBM 3740 single density format (FM), or IBM System 34 Double Density format (MFM) including double sided recording. The UM8272A

Pin Configuration



Block Diagram



Floppy Disk Controller

provides control signals which simplify the design of an external phase locked loop and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a Floppy Disk Drive interface. The UM8272A is a pin-compatible upgrade to the 8272.

Hand-Shaking signals are provided in the UM8272A which make DMA operation easy to incorporate with the aid of an external DMA Controller chip. The FDC will operate in either DMA or Non-DMA mode. In the Non-DMA mode, the FDC generates interrupts to the processor every time a data byte is available. In the DMA mode, the processor need only load the command into the FDC and all data transfers occur under control of the UM8272A and DMA controller.

There are 15 separate commands which the UM8272A will execute. Each of these commands requires multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available:

Read Data	Write Data
Read ID	Format a Track
Read Deleted Data	Write Deleted Data
Read a Track	Seek
Scan Equal	Recalibrate (Restore to Track 0)
Scan High or Equal	Sense interrupt Status
Scan Low or Equal	Sense Drive Status
Specify	

Address mark detection circuitry is internal to the FDC which simplifies the phase locked loop and read electronics. The track stepping rate, head load time, and head unload time may be programmed by the user. The UM8272A offers many additional features such as multiple sector transfers in both read and write with a single command, and full IBM compatibility in both single and double density models.

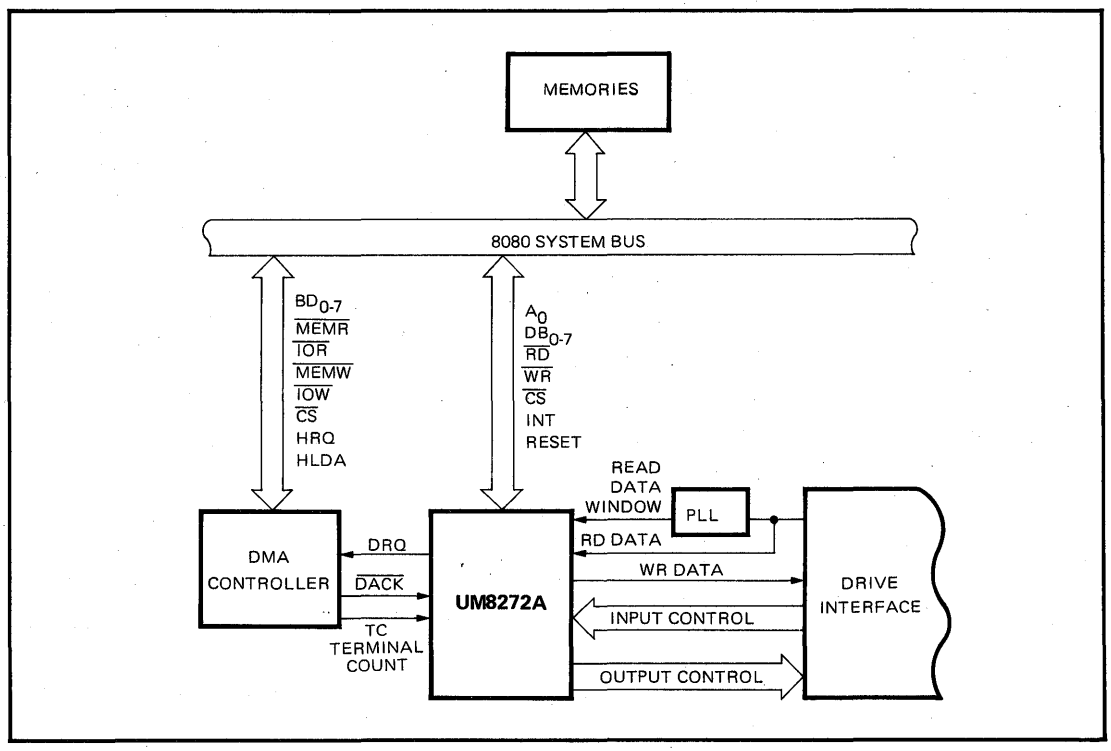


Figure 1. System Configuration

Absolute Maximum Ratings*

Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C
All Output Voltages	−0.5 to +7 Volts
All Input Voltages	−0.5 to +7 Volts
Supply Voltage V_{CC}	−0.5 to +7 Volts
Power Dissipation	1 Watt

*Comments

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

(T_A = 0°C to +70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	Limits		Units	Conditions
		Min.	Max.		
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4	V_{CC}	V	I_{OH} = −400 μA
I_{CC}	V_{CC} Supply Current		120	mA	
I_{IL}	Input Load Current (All Input Pins)		10 −10	μA μA	V_{IN} = V_{CC} V_{IN} = 0 V
I_{LOH}	High Level Output Leakage Current		10	μA	V_{OUT} = V_{CC}
I_{OFL}	Output Float Leakage Current	−10	+10	μA	0.45 V ≤ V_{OUT} ≤ V_{CC}

Capacitance

(T_A = 25°C, f_c = 1 MHz, V_{CC} = 0V)

Symbol	Parameter	Limits		Unit	Conditions
		Min.	Max.		
$C_{IN}(\phi)$	Clock Input Capacitance		20	pF	All Pins Except Pin Under Test Tied to AC Ground
C_{IN}	Input Capacitance		10	pF	
$C_{I/O}$	Input/Output Capacitance		20	pF	

A.C. Characteristics

(T_A = 0°C to +70°C, V_{CC} = +5.0V ± 10%)

CLOCK TIMING

Symbol	Parameter	Min.	Max.	Units	Notes
T_{CY}	Clock Period	120	500	ns	Note 5
t_{CH}	Clock High Period	40		ns	Note 4, 5
t_{RST}	Reset Width	14		t_{CY}	

READ CYCLE

t_{AR}	Select Setup to $\overline{RD}\downarrow$	0		ns	
t_{RA}	Select Hold from $\overline{RD}\uparrow$	0		ns	
t_{RR}	$\overline{RD}$ Pulse width	250		ns	
t_{RD}	Data Delay from $\overline{RD}\downarrow$		200	ns	
t_{DF}	Output Float Delay	20	100	ns	

A.C. Characteristics (Continued)

(T_A = 0°C to + 70°C, V_{CC} = +5.0V ± 10%)

WRITE CYCLE

Symbol	Parameter	Typ.	Min.	Max.	Units	Notes
t_{AW}	Select Setup to $\overline{WR}\downarrow$		0		ns	
t_{WA}	Select Hold from $\overline{WR}\uparrow$		0		ns	
t_{WW}	$\overline{WR}$ Pulse Width		250		ns	
t_{DW}	Data Setup to $\overline{WR}\uparrow$		150		ns	
t_{WD}	Data Hold from $\overline{WR}\uparrow$		10		ns	

INTERRUPTS

t_{RI}	INT Delay from $\overline{RD}\uparrow$			500	ns	Note 6
t_{WI}	INT Delay from $\overline{WR}\uparrow$			500	ns	Note 6

DMA

t_{ROCY}	DRQ Cycle Period		13		μs	Note 6
t_{AKRO}	$\overline{DACK}\downarrow$ to DRQ↓			200	ns	
t_{ROR}	DRQ ↑ to $\overline{RD}\downarrow$		800		ns	Note 6
t_{ROW}	DRQ ↑ to $\overline{WR}\downarrow$		250		ns	Note 6
t_{RORW}	DRQ ↑ to $\overline{RD}\uparrow$ or $\overline{WR}\uparrow$			12	μs	Note 6

FDD INTERFACE

t_{WCY}	WCK Cycle Time	2 or 4 1 or 2			μs	MFM = 0 MFM = 1 Note 2
t_{WCH}	WCK High Time	250	80	350	ns	
t_{CP}	Pre-Shift Delay from WCK↑		20	100	ns	
t_{CD}	WDA Delay from WCK ↑		20	100	ns	
t_{WDD}	Write Data Width		t_{WCH} −50		ns	
t_{WE}	WE ↑ to WCK ↑ or WE ↓ to WCK ↓ Delay		20	100	ns	
t_{WWCY}	Window Cycle Time	2 1			μs	MFM = 0 MFM = 1
t_{WRD}	Window Setup to RDD ↑		15		ns	
t_{RDW}	Window Hold from RDD ↓		15		ns	
t_{RDD}	RDD Active Time (HIGH)		40		ns	

FDD SEEK/DIRECTION/STEP

t_{US}	$US_{0,1}$ Setup to $\overline{RW}$/SEEK ↑		12		μs	Note 6
t_{SU}	$US_{0,1}$ Hold after $\overline{RW}$/SEEK ↓		15		μs	Note 6
t_{SD}	$\overline{RW}$/SEEK Setup to LCT/DIR		7		μs	Note 6
t_{DS}	$\overline{RW}$/SEEK Hold from LCT/DIR		30		μs	Note 6
t_{DST}	LCT/DIR Setup to FR/STEP↑		1		μs	Note 6
t_{STD}	LCT/DIR Hold from FR/STER ↓		24		μs	Note 6
t_{STU}	$DS_{2,1}$ Hold from FR/Step ↓		5		μs	Note 6
t_{STP}	STEP Active Time (High)	5			μs	Note 6
t_{SC}	STEP Cycle Time		33		μs	Note 3, 6
t_{FR}	FAULT RESET Active Time (High)		8	10	μs	Note 6
t_{IDX}	INDEX Pulse Width	10			t_{CY}	
t_{TC}	Terminal Count Width		1		t_{CY}	

Notes:
1. Typical values for T_A = 25°C and nominal supply voltage.
2. The former values are used for standard floppy and the latter values are used for mini-floppies.
3. t_{SC} = 33 μs min, is for different drive units. In the case of same unit, t_{SC} can be ranged from 1 ms to 16 ms with 8 MHzclock period, and 2 ms to 32 ms with 4 MHz clock, under software control.
4. From 2.0V to + 2.0V.
5. At 4 MHz, the clock duty cycle may range from 16% to 76%. Using an 8 MHz clock the duty cycle can range from 32% to 52%. Duty cycle is defined as: D.C. = 100 ($t_{CH} \rightarrow t_{CY}$) with typical rise and fall times of 5 ns.
6. The specified values listed are for an 8 MHz clock period, Multiply timings by 2 when using a 4 MHz clock period.

Pin Description

Pin			Input/ Output	Connection to	Functions
No.	Symbol	Name			
1	RST	Reset	Input	Processor	Places FDC in idle state Resets output lines to FDD to "0" (low). Does not effect SRT, HUT or HLT in Specify command. If RDY pin is held high during Reset, FDC will generate interrupt 1.024 ms later. To clear this interrupt use Sense Interrupt Status command.
2	$\overline{RD}$	Read	Input (1)	Processor	Control signal for transfer of data from FDC to Data Bus, when "0" (low).
3	$\overline{WR}$	Write	Input (1)	Processor	Control signal for transfer of data to FDC via Data Bus, when "0" (low).
4	$\overline{CS}$	Chip Select	Input	Processor	IC selected when "0" (low), allowing $\overline{RD}$ and $\overline{WR}$ to be enabled.
5	A_0	Data/Status Reg Select	Input (1)	Processor	Selects Data Reg (A_0 = 1) or Status Reg (A_0 = 0) contents of the FDC to be sent to Data Bus.
6-13	DB_0-DB_7	Data Bus	Input (1) Output	Processor	Bi-Directional 8-Bit Data Bus.
14	DRQ	Data DMA Request	Output	DMA	DMA Request is being made by FDC when DRW = "1".
15	$\overline{DACK}$	DMA Acknowledge	Input	DMA	DMA cycle is active when "0" (low) and Controller is performing DMA transfer.
16	TC	Terminal Count	Input	DMA	Indicates the termination of a DMA transfer when "1" (high). It terminates data transfer during Read/ Write/Scan command in DMA or interrupt mode.
17	IDX	Index	Input	FDD	Indicates the beginning of a disk track.
18	INT	Interrupt	Output	Processor	Interrupt Request Generated by FDC.
19	CLK	Clock	Input		Single Phase 8 MHz Squarewave Clock.
20	GND	Ground			D.C. Power Return.
21	WCK	Write Clock	Input		Write Data rate to FDD. FM = 500 kHz, MFM = 1 MHz, with a pulse width of 250 ns for both FM and MFM.
22	RDW	Read Data Window	Input	Phase Lock Loop	Generated by PLL, and used to sample data from FDD.

Pin Description (Continued)

Pin			Input Output	Connection to	Functions
No.	Symbol	Name			
23	RDD	Read Data	Input	FDD	Read data from FDD, containing clock and data bits.
24	VCO	VCO Sync	Output	Phase Lock Loop	Inhibits VCO in PLL when "0" (low), enables VCO when "1".
25	WE	Write Enable	Output	FDD	Enables write data into FDD.
26	MFM	MFM Mode	Output	Phase Lock Loop	MFM mode when "1", FM mode when "0".
27	HD	Head Select	Output	FDD	Head 1 selected when "1" (high). Head 2 selectwd when "0" (low).
28, 29	US_1, US_0	Unit Select	Output	FDD	FDD Unit Selected.
30	WDA	Write Data	Output	FDD	Serial clock and data bits to FDD.
31, 32	PS_1, PS_0	Precompensation (pre-shift)	Output	FDD	Write Precompensation status during MFM mode. Determines early, late, and normal times.
33	FLT/TR_0	Fault/Track 0	Input	FDD	Senses FDD fault condition, in Read/Write mode; and Track 0 condition in Seek mode.
34	WP/TS	Write Protect/ Two-Side	Input	FDD	Senses Write Protect Status in Read/ Write mode; and Two Side Media in Seek mode.
35	RDY	Ready	Input	FDD	Indicates FDD is ready to send or receive data.
36	HDL	Head Load	Output	FDD	Command which causes read/write head in FDD to contact diskette.
37	FR/STP	Fit Reset/Stop	Output	FDD	Resets fault F.F. in FDD in Read/ Write mode, contains stop pulses to move head to another cylinder in Seek mode.
38	LCT/DIR	Low Current/ Direction	Output	FDD	Lowers Write current on inner tracks in Read/Write mode, determines direction head will stop in Seek mode. A fault reset pulse is issued at the beginning of each Read or Write command prior to the occurrence of the Head Load signal.
39	$\overline{RW}$/SEEK	Read Write/SEEK	Output	FDD	When "1" (high) Seek mode selected and when "0" (low) Read/Write mode selected.
40	V_{CC}	+5V			DC Power.

Note: (1) Disabled when $\overline{CS}$ = 1.

UM8272A Enhancements

On the UM8272A, after detecting the Index Pulse, the VCO Sync output stays low for a shorter period of time. See Figure 2A.

On the 8272 there can be a problem reading data when Gap 2A is 00 and there is no 1AM. This occurs on some older floppy formats. The UM8272A cures this problem by adjusting the VCO Sync timing so that it is not low during the data field. See Figure 2B.

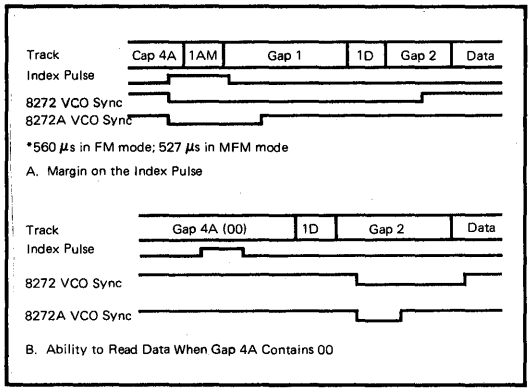


Figure 2. UM8272A Enhancements over the 8272

UM8272A Registers – CPU Interface

The UM8272A contains two registers which may be accessed by the main system processor, a Status Register and a Data Register. The 8-bit Main Status Register contains the status information of the FDC, and may be accessed at any time. The 8-bit Data Register (actually consists of several registers in a stack with only one register presented to the data bus at a time), stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after execution of a command. The Status Register may only be read and is used to facilitate the transfer of data between the processor and UM8272A.

The relationship between the Status/Data registers and the signals $\overline{RD}$, $\overline{WR}$, and A_0 is shown in Table 1.

Table 1. A_0, $\overline{RD}$, $\overline{WR}$ decoding for the selection of Status/ Data register functions.

A_0	$\overline{RD}$	$\overline{WR}$	Function
0	0	1	Read Main Status Register
0	1	0	Illegal (see note)
0	0	0	Illegal (see note)
1	0	0	Illegal (see note)
1	0	1	Read from Data Register
1	1	0	Write into Data Register

Note: Design must guarantee that the UM8272A is not subjected to illegal inputs.

The Main Status Register bits are defined in Table 2.

Table 2. Main Status Register bit description.

Bit Number	Name	Symbol	Descriptions
DB_0	FDD 0 Busy	D_0B	FDD number 0 is in the Seek mode. If any of the bits isset FDC will not accept read or write command.
DB_1	FDD 1 Busy	D_1B	FDD number 1 is in th Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_2	FDD 2 Busy	D_2B	FDD number 2 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_3	FDD 3 Busy	D_3B	FDD number 3 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_4	FDC Busy	CB	A read or write command is in process. FDC will not accept any other command.
DB_5	Execution Mode	EXM	This bit is set only during execution phase in non-DMA mode. When DB_5 goes low, execution phase has ended, and result phase was started. It operates only during NON-DMA modes of operation.
DB_6	Data Input/Output	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO = "1" then transfer is from Data Register to the Processor. If DIO = "0", then transfer is from the Processor to Data Register.
DB_7	Request for Master	RQM	Indicates Data Register is ready to send or receive data to or from the Processor. Both bits DIO and RQM should be used to perform the hand-shaking functions of "ready" and "direction" to the processor.

The DIO and RQM bits in the Status Register indicate when Data is ready and in which direction data will be transferred on the Data Bus. The max time between the last $\overline{RD}$ or $\overline{WR}$ during command or result phase and DIO and RQM getting set or reset is 12 µs. For this reason every time Main Status REgister is read the CPU should wait 12 µs. The max time from the trailing edge of the last RD in the result phase to when DB, (FDC Busy) goes low is 12 µs.

Note: There is a 12µS or 24µS ROM flag delay when using an 8 or 4 MHz clock respectively.

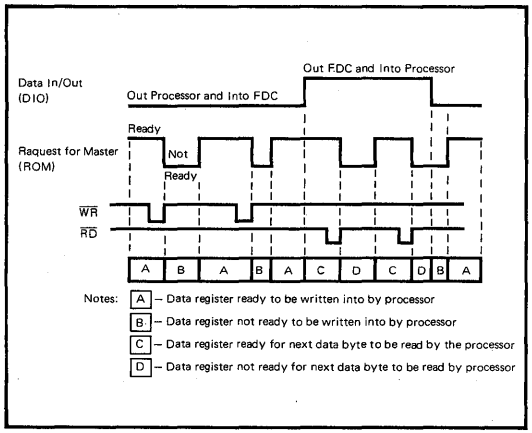


Figure 3. Status Register Timing

The UM8272A is capable of executing 15 different commands. Each command is initiated by a multi-byte transfer from the processor, and the result after execution of the command may also be a multi-byte transfer back to the processor. Because of this multi-byte interchange of information between the UM8272A and the processor, it is convenient to consider each command as consisting of three phases:

Command Phase:	The FDC receives all information required to perform a particular operation from the processor.
Execution Phase:	The FDC performs the operation it was instructed to do.
Resuit Phase:	After completion of the operation, status and other housekeeping information are made available to the processor.

During Command or Result Phases the Main Status Register (described in Table 2) must be read by the processor before each byte of information is written into or read from the Data Register. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the UM8272A. Many of the commands require multiple bytes, and as a result the Main Status Register must be read prior to each byte transfer to the UM8272A. On the other hand, during the Result Phase, D6 and D7 in the Main Status Register must both be 1's (D6 = 1 and D7 = 1) before reading each byte from the Data Register. Note, this reading of the Main Status Register before each byte transfer to the UM8272A is required in only the Command and Result Phases, and NOT during the Execution Phase.

During the Execution Phase, the Main Status Register need not be read. If the UM8272A is in the non-DMA Mode, then the receipt of each data byte (if UM8272A is reading data from FDD) is indicated by an interrupt signal on pin 18 (INT = 1). The generation of a Read signal (RD = 0) will reset the interrupt as well as output the Data onto the Data Bus. For example, if the processor cannot handle Interrupts fast enough (every 13 μs for MFM mode) then it may poll the Main Status Register and then bit D7 (RQM) functions just like the Interrupt signal. If a Write Command is in process, then the WR signal performs the reset to the Interrupt signal.

The UM8272A always operates in a multi-sector transfer mode. It continues to transfer data until the TC input is active. In Non-DMA Mode, the system must supply the TC input.

If the UM8272A is in the DMA Mode, no Interrupts are generated during the Execution Phase. The UM8272A generates DRQ's (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both a $\overline{DACK}$ = 0 (DMA Acknowledge) and a RD = 0 (Read signal). When the DMA Acknowledge signal goes low ($\overline{DACK}$ = 0) then the DMA Request is reset (DRQ = 0). If a Write Command has been programmed then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the Execution Phase has been completed (Terminal Count has occurred) then an Interrupt will occur (INT = 1). This signifies the beginning of the Result Phase. When the first byte of data is read during the Result Phase, the Interrupt is automaticaily raset (INT = 0).

It is important to note that during the Resuit Phase all bytes shown in the Command Table must be read. The Read Data Command, for example, has seven bytes of data in the Result Phase. All seven bytes must be read in order to successfully complete the Read Data Command. The UM8272A will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result Phase.

The UM8272A contains five Status Registers. The Main Status Register mentioned above may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are only available during the Result Phase, and may be read only after successfully completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

The bytes of data which are sent to the UM8272A to from the Command Phase, and are read out of the UM8272A in the Result Phase, must occur in the order shown in the Table 3 That is, the Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result Phases are allowed. After the last byte of data in the Command Phase is sent to the UM8272A, the Execution Phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result Phase, the command is automatically ended and the UM8272A is ready for a new command. A command may be aborted by simply sending a Terminal Count signal to pin 16 (TC=1). This is a convenient means of ensuring that the processor may always get the UM8272A's attention even if the disk system hangs up in an abnormal manner.

Command Symbol Description

Symbol	Name	Descriptions
A_0	Address Line 0	A_0 controls selection of Main Status Register (A_0 = 0) or Data Register (A_0 = 1).
C	Cylinder Number	C stands for the current/selected Cylinder (track) number 0 through 76 of the medium.
D	Data	D stands for the data pattern which is going to be written into a sector.
D_7-D_0	Data Bus	8-bit Data Bus, where D_7 stands for a most significant bit, and D_0 stands for a least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the Sector.
EOT	End of Track	EOT stands for the final Sector number on a Cylinder. During Read or Write operation FDC will stop date transfer after a sector # equal to EOT.
GPL	Gap Length	GPL stands for the length of Gap 3. During Read/Write commands this value determines the number of bytes that VCOs will stay low after two CRC bytes. During Format command it determines the size of Gap 3.
H	Head Address	H stands for head number 0 or 1, as specified in ID field.
HD	Head	HD stands for a selected head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words.)
HLT	Head Load Time	HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	HUT stands for the head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
MT	Multi-Track	If MT is high, a multi-track operation is to be performed. If MT = 1 after finishing Read/Write operation on side 0 FDC will automatically start searching for sector 1 on side 1.
N	Number	N stands for the number of data bytes written in Sector.
NCN	New Cylinder Number	NCN stands for a new Cylinder number, which is going to be reached as a result of the Seek operation. Desired position of Head.
ND	Non-DMA Mode	ND stands for operation in the Non-DMA Mode.
PCN	Present Cylinder Number	PCN stands for the Cylinder number at the completion of SENSE INTERRUPT STATUS Command. Position of Head at present time.
R	Record	R stands for the Sector number, which will be read or written.
R/W	Read/Write	R/W stands for either Read (R) or Write (W) signal.
SC	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip	SK stands for Skip Deleted Data Address Mark.
SRT	Step Rate Time	SRT stands for the Stepping Rate for the FDD. (1 to 16 ms in 1 ms increments.) Stepping Rate applies to all drives, (F = 1 ms, E = 2 ms, etc.)
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	ST 0-3 stand for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by A_0 = 0); ST 0-3 may be read only after a command has been executed and contain information relevant to that particular command.
STP		During a Scan operation, if STP = 1, the data in continguous sectors is compared byte by byte with data sent from the processor (or DMA); and is STP = 2, then alternate sectors are read and compared.
US0, US1	Unit Select	US stands for a selected drive number 0 or 1.

Table 3. UM8272A Command Set

PHASE	R/W	DATABUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
READ DATA										
Command	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	———			C				———	Sector ID information prior to Command execution. The 4 by tes are commanded against header on Floppy Disk.
	W	———			H				———	
	W	———			R				———	
	W	———			N				———	
	W	———			EOT				———	
	W	———			GPL				———	
	W	———			DTL				———	
Execution										Data-transter between the FDD and main-system
Result	R	———			ST 0				———	Status information after Command execution
	R	———			ST 1				———	
	R	———			ST 2				———	
	R	———			C				———	Sector ID information after Command execution
	R	———			H				———	
	R	———			R				———	
	R	———			N				———	
READ DELETED DATA										
Command	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	———			C				———	Sector ID information Prior to Command execution. The 4 by tes are commanded against header on Floppy Disk.
	W	———			H				———	
	W	———			R				———	
	W	———			N				———	
	W	———			EOT				———	
	W	———			GPL				———	
	W	———			OTL				———	
Execution										Data-transter between the FDD and main-system
Result	R	———			ST 0				———	Status information after Command execution
	R	———			ST 1				———	
	R	———			ST 2				———	
	R	———			C				———	Sector ID information after Command execution
	R	———			H				———	
	R	———			R				———	
	R	———			N				———	
WRITE DATA										
Command	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	———			C				———	Sector ID information Prior to Command execution. The 4 by tes are commanded against header on Floppy Disk.
	W	———			H				———	
	W	———			R				———	
	W	———			N				———	
	W	———			EOT				———	
	W	———			GPL				———	
	W	———			DTL				———	
Execution										Data-transter between the main-system and FDD
Result	R	———			ST 0				———	Status information after Command execution
	R	———			ST 1				———	
	R	———			ST 2				———	
	R	———			C				———	Sector ID information after Command execution
	R	———			H				———	
	R	———			R				———	
	R	———			N				———	
WRITE DELETED DATA										
Command	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	———			C				———	Sector ID information Prior to Command execution. The 4 by tes are commanded against header on Floppy Disk.
	W	———			H				———	
	W	———			R				———	
	W	———			N				———	
	W	———			EOT				———	
	W	———			GPL				———	
	W	———			DTL				———	
Execution										Data-transter between the FDD and main-system
Result	R	———			ST 0				———	Status information after Command execution
	R	———			ST 1				———	
	R	———			ST 2				———	
	R	———			C				———	Sector ID information after Command execution
	R	———			H				———	
	R	———			R				———	
	R	———			N				———	

PHASE	R/W	DATABUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
READ A TRACK										
Command	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	———			C				———	Sector ID information prior to Command execution
	W	———			H				———	
	W	———			R				———	
	W	———			N				———	
	W	———			EOT				———	
	W	———			GPL				———	
	W	———			DTL				———	
Execution										Data-transter between the FDD and main-system. FDC reads all data fields from index hole to EOT
Result	R	———			ST 0				———	Status information after Command execution
	R	———			ST 1				———	
	R	———			ST 2				———	
	R	———			C				———	Sector ID information after Command execution
	R	———			H				———	
	R	———			R				———	
	R	———			N				———	
READ ID										
Command	W	0	MF	0	0	1	0	1	0	Commands
	W	X	X	X	X	X	HD	US1	US0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R	———			ST 0				———	Status information after Command execution
	R	———			ST 1				———	
	R	———			ST 2				———	
	R	———			C				———	Sector ID information read during Execution Phase from Floppy Disk
	R	———			H				———	
	R	———			R				———	
	R	———			N				———	
FORMAT A TRACK										
Command	W	0	MF	0	0	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	———			N				———	Bytes/Sector
	W	———			SC				———	Sectors/Track
	W	———			GPL				———	Gap 3
	W	———			D				———	Filler Byte
Execution										FDC formats an entire trach
Result	R	———			ST 0				———	Status information after Command execution
	R	———			ST 1				———	
	R	———			ST 2				———	
	R	———			C				———	In this case, the ID information has no meaning
	R	———			H				———	
	R	———			R				———	
	R	———			N				———	
SCAN EQUAL										
Command	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	———			C				———	Sector ID information Prior to Command execution.
	W	———			H				———	
	W	———			R				———	
	W	———			N				———	
	W	———			EOT				———	
	W	———			GPL				———	
	W	———			STP				———	
Execution										Data-compared be-tween the FDD and main-system
Result	R	———			ST 0				———	Status information after Command execution
	R	———			ST 1				———	
	R	———			ST 2				———	
	R	———			C				———	Sector ID information after Command execution
	R	———			H				———	
	R	———			R				———	
	R	———			N				———	

Note: 1 Symbols used in this table are described at the and of this section.

2 A_0 should equal binary 1 for all operations.

3 X = Don't care, usually made to equal binary 0.

Table 3. UM8272A Command Set (Continued)

PHASE	R/W	DATABUS D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	REMARKS
SCAN LOW OR EQUAL			
Command	W	MT MF SK 1 1 0 0 1	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior Command execution,
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	STP	
Execution			Data-compared between the FDD and main-system
Result	R	ST 0	Status information after Command execution
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution
	R	H	
	R	R	
	R	N	
SCAN HIGH OR EQUAL			
Command	W	MT MF SK 1 1 1 0 1	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior Command execution
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	STP	
Execution			Data-compared between the FDD and main-system
Result	R	ST 0	Status information after Command execution
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution
	R	H	
	R	R	
	R	N	

PHASE	R/W	DATABUS D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	REMARKS
RECALIBRATE			
Command	W	0 0 0 0 0 1 1 1	Command Codes
	W	X X X X X 0 US1 US0	
Execution			Head retracted to Track 0
SENSE INTERRUPT STATUS			
Command	W	0 0 0 0 1 0 0 0	Command Codes
Result	R	ST 0	Status information at the end of seek-operation about the FDC
	R	PCN	
SPECIFY			
Command	W	0 0 0 0 0 1 1	Command Codes
	W	SRT HUT	
	W	HLT ND	
SENSE DRIVE STATUS			
Command	W	0 0 0 0 0 1 0 0	Command Codes
	W	X X X X X HD US1 US0	
Result	R	ST 3	Status information about FDD
SEEK			
Command	W	0 0 0 0 1 1 1 1	Command Codes
	W	X X X X X HD US1 US0	
	W	NCN	
Execution			Head is positioned over proper Cylinder on Diskette
INVALID			
Command	W	Invalid Codes	Invalid Command Codes (NoOp – FDC goes into Standby State)
Result	R	ST 0	ST 0 = 80 (16)

Polling Feature of the UM8272A

After power-up RESET, the Drive Select Lines DS0 and DS1 will automatically go into a polling mode. In between commands (and between step pulses in the SEEK command) the UM8272A polls all four FDDs looking for a change in the Ready line from any of the drives. If the Ready line changes state (usually due to a door opening or closing) then the UM8272A will generate an interrupt. When Status Register 0 (ST0) is read (after Sense Interrupt Status is issued), Not Ready (NR) will be indicated. The polling of the Ready line by the UM8272A occurs continuously between instructions, thus notifying the processor which drives are on or off line. Approximate scan timing is shown in Table 4.

Table 4. Scan Timing

DS1	DS0	APPROXIMATE SCAN TIMING
0	0	220μS
0	1	220μS
1	0	220μS
1	1	440μS

Command Descriptions

During the Command Phase, the Main Status Register must be polled by the CPU before each byte is written into the Data Register. The DIO (DB6) and RQM (DB7) bits in the Main Status Register must be in the "0" and "1" states respectively, before each byte of the command may be written into the UM8272A. The beginning of the execution phase for any of these commands will cause DIO and RQM to switch to "1" and "0" states respectively.

READ DATA

A set of nine (9) byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head setting time (defined in the Specify Command), and begins reading ID address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the Data field) byte-by-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Data Command must

be terminated by the receipt of a Terminal Count signal. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminate the Read Data Command.

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track), MFM (MFM/FM), and N (Number of Bytes/Sector). Table 5 on the next page shows the Transfer Capacity. The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder,

Table 5. Transfer Capacity

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskette
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

data will be transferred starting at Sector 1. Side 0 and completing at Sector L. Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to OFFH.

At the completion of the Read Data Command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another. If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK=0), then the FDC sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serived by the processor every 27 μs in the FM Mode, and every

13 μs in the MFM Mode, or the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID Information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 3 shows the values for C, H, R, and N, when the processor terminates the Command.

Table 6. ID Information When Processor Terminates Command

MT	EOT	Final Sector Transferred to Processor	ID Information at Result Phase			
			C	H	R	N
0	1A 0F 08	Sector 1 to 25 at Side 0 Sector 1 to 14 at Side 0 Sector 1 to 7 at Side 0	NC	NC	R + 1	NC
	1A 0F 08	Sector 26 at Side 0 Sector 15 at Side 0 Sector 8 at Side 0	C + 1	NC	R = 01	NC
	1A 0F 08	Sector 1 to 25 at Side 1 Sector 1 to 14 at Side 1 Sector 1 to 7 at Side 1	NC	NC	R + 1	NC
	1A 0F 08	Sector 26 at Side 1 Sector 15 at Side 1 Sector 8 at Side 1	C + 1	NC	R = 01	NC
1	1A 0F 08	Sector 1 to 25 at Side 0 Sector 1 to 14 at Side 0 Sector 1 to 7 at Side 0	NC	NC	R + 1	NC
	1A 0F 08	Sector 26 at Side 0 Sector 15 at Side 0 Sector 8 at Side 0	NC	LSB	R = 01	NC
	1A 0F 08	Sector 1 to 25 at Side 1 Sector 1 to 14 at Side 1 Sector 1 to 7 at Side 1	NC	NC	R + 1	NC
	1A 0F 08	Sector 26 at Side 1 Sector 15 at Side 1 Sector 8 at Side 1	C + 1	LSB	R = 01	NC

Note: 1. NC (no Change): The same value as the one at the beginning of command execution.
2. LSB (Least Significant Bit): The least significant bit of H is complemented.

WRITE DATA

A set of nine (9) bytes are required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specifled, head settling time (defined in the Specify Command), and begins reading ID Fields. When the current sector number ("R"), stored in the ID Register. (IDR) compares with the sector number read off the diskette, then the FDC takes data from the processor byte-by-byte via the data bus, and outputs it to the FDD. After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written into. The FDC continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count-signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written then the remainder of the data field is filled with 00 (zeros).

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (Incorrect CRC) in one of the ID Fields, if sets the DE (Data Error) flag of Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write Command operates in much the same manner as the Read Command. The Following items are the same; refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head Huload Time Interval
- ID Information when the processor terminates command (see Table 1)
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC must occur every 31 μs in the FM mode, and every 15 μs in the MFM mode. If the time interval between data transfers is longer than this then the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Write Data Command.

For Mini-floppies, multiple track writes are usually not permitted. This is because of the turn-off time of the erase head coils—the head switches tracks before the erase head turns off. Therefore the system should typically wait 1.3 mS before attempting to step or change sides.

WRITE DELETED DATA

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

READ DELETED DATA

This command is the same as the Read Data Command except that when the FDC detects a Data Address Mark at the beginning of a Data Field (and SK = 0 (low), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address Mark and reads the next sector.

READ A TRACK

This command is similar to READ DATA Command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering the INDEX HOLE the FDC starts reading all data fields on the track as continuous blocks of data. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Status Register 1 to a 1 (high) if there is no comparison. Multitrack or skip operations are not allowed with this command.

This command terminates when EOT number of sectors have been read. If the FDC does not find an ID Address Mark on the diskette after it encounters the INDEX HOLE for the second time, then it sets the MA (missing address mark) flag in Status Register 1 to a 1 (high), an and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

READ ID

The READ ID Command is used to give the present position of the recording head. The FDC stores the values from the first ID Field it is able to read. If no proper ID Address Mark is found on the diskette, before the INDEX HOLE is encountered for the second time then the MA (Missing Address Mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high) and the command is terminated.

FORMAT A TRACK

The Format Command allows an entire track to be formatted. After the INDEX HOLE is detected, Data is written on the Diskette: Gaps, Address Marks, ID Fields and Data Fields, all per the IBM System 34 (Double Density) or System 3740 (Single Density). Format are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (Gap Length), and D (Data Pattern) which are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor, that is, four data requests per sector are made by the FDC for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

After formatting each sector, the processor must send new values for C, H, R, and N to the UM8272A for each sector on the track. The contents of the R Register is incremented by one after each sector is formatted, thus, the R register contains a value of R + 1 when it is read during the Result Phase. This incrementing and formatting continues for the whole track until the FDC encounters the INDEX HOLE for the second time, whereupon it terminates the command.

If a FAULT signal is received from the FDD at the end of a write operation, then the FDC sets the EC flag of status Register 0 to a 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also the loss of a READY signal at the beginning of a command execution phase causes command termination.

Table 7 shows the relationship between N, SC, and GPL for various sector sizes:

Table 9. Sector Size Reiationships

	8" STANDARD FLOPPY					5¼" MINI FLOPPY				
Format	**Sector Size**	**N**	**SC**	**GPL[1]**	**GPL[2]**	**Remarks**	**Sector Size**	**N**	**SC**	**GPL[1]**	**GPL[2]**
FM Mode	128 bytes/Sector	00	1A	07	1B	IBM Diskette 1	128 bytes/Sector	00	12	07	09
	256	01	0F	0E	2A	IBM Diskette 2	128	00	10	10	19
	512	02	06	1B	3A		256	01	06	18	30
	1024	03	04	47	8A		512	02	04	46	87
	2048	04	02	C8	FF		1024	03	02	D8	FF
	4096	05	01	C8	FF		2048	04	01	C8	FF
MFM Mode	256	01	1A	0E	36	IBM Diskette 2D	256	01	12	0A	0C
	512	02	0F	1B	54		256	01	10	20	32
	1024	03	08	35	74	IBM Diskette 2D	512	02	08	2A	50
	2048	04	04	99	FF		1024	03	04	80	F0
	4096	05	02	C8	FF		2048	04	02	CB	FF
	8192	06	01	C8	FF		4096	05	01	C8	FF

Notes: 1. Suggested values of GPL in Read or write Commands to avoid splice point between data field and ID field of contiguous sections.
2. Suggested values of GPL in formal command.

During the Command Phase of the Seek operation the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON BUSY state. While the FDC is in the NON BUSY state, another Seek Command may be issued, and in this manner parallel seek operations may be done on up to 4 Drives at once.

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the seek operation, then the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated.

Note that the UM8272A Read and Write Commands do not have implied Seeks. Any R/W command should be preceded by: 1) Seek Command; 2) sense Interrupt Status; and 3) Read ID.

RECALIBRATE

This command causes the read/write head within the FDD to retract to the Track 0 position. The FDC clears the contents of the PCN counter, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 1 (high) and Step Pulses are issued. When the Track 0 signal goes high, the SE (SEEK END) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 Step Pulses, have been issued, the FDC sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 to both 1s (highs), and terminates the command.

The ability to overlap RECALIBRATE Commands to multiple FDDs, and the loss of the READY signal, as described in the SEEK Command, also applies to the RECALIBRATE Command.

SENSE INTERRUPT STATUS

An Interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data Command
   b. Read a Track Command
   c. Read ID Command
   d. Read Deleted Data Command
   e. Write Data Command
   f. Format a Cylinder Command
   g. Write Deleted Data Command
   h. Scan Commands
2. Ready Line of FDD changes state
3. End of Seek or Recallbrate Command
4. During Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernbile by the processor. However, interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status Command. This command when issued resets the interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

Neither the Seek or Recalibrate Command have a Result Phase. Therefore, it is mandatory to use the Sense interrupt Status Command after these commands to effectively terminate them and to provide verification of the head position (PCN).

Table 8. Seek, Interrupt Codes

Seek End Bit 5	Interrupt Code		CAUSE
	Bit 6	Bit 7	
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate Command
1	1	0	Abnormal Termination of Seek or Recalibrate Command

SPECIFY

The Specify Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms . . . OF = 240 ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and when the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms . . . . FE = 254 ms).

The step rate should be programmed 1 ms longer than the minimum time required by the drive.

The time intervals mentioned above are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock, if the clock was reduced to 4 MHz (minifloppy application) then all time intervals are increased by a factor of 2.

The choice of DMA or NON-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1) the NON-DMA mode is selected, and when ND = 0 the DMA mode is selected.

SENSE DRIVE STATUS

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information.

INVALID

If an invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command. No interrupt is generated by the UM8272A during this condition. Bit 6 and bit 7 (DIO and RQM) in the Main Status Register are both high ("1") indicating to the processor that the UM8272A is in the Result Phase and the contents of Status Register 0 (ST0) must be read. When the processor reads Status Register 0 it will find an 80H Indicating and invalid command was received.

A Sense interrupt Status Command must be sent after a Seek or Recalibrate interrupt, otherwise the FDC will consider the next command to be an invalid Command.

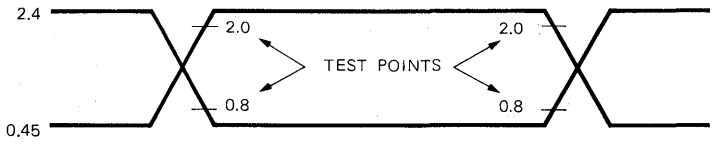
In some applications the user may wish to use this command as a No-Op command, to place the FDC in a stand by or no operation state.

Table 9. Status Registers

Bit No.	Bit Name	Bit Symbol	Descriptions
			STATUS REGISTER 0
D_7	Interrupt Code	IC	$D_7 = 0$ and $D_6 = 0$ Normal Termination of Command, (NT). Command was completed and properly executed.
D_6			$D_7 = 0$ and $D_6 = 1$ Abnomal Termination of Command, (AT). Execution of Command was started, but was not successfully completed.
			$D_7 = 1$ and $D_6 = 0$ Invalid Command issue, (IC). Command which was issued was never started.
			$D_7 = 1$ and $D_6 = 1$ Abnormal Termination because during command execution the ready signal from FDD changed state.
D_5	Seek End	SE	When the FDC completes the SEEK Command, this flag is set to (high).
D_4	Equipment Check	EC	If a fault Signal is received from the FDD, or if the Track 0 Signal fails to occur after 77 Step Pulses (Recalibrate Command) then this flag is set.
D_3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single sided drive, then this flag is set.
D_2	Head Address	HD	This flag is used to indicate the state of the head at Interrupt.
D_1	Unit Select 1	US 1	These flags are used to indicate a
D_0	Unit Select 0	US 0	Drive Unit Number at Interrupt
			STATUS REGISTER 1
D_7	End of Cylinder	EN	When the FDC tries to access a Sector beyond the final Sector of a Cylinder, this flag is set.
D_6			Not used. This bit is always 0 (low).
D_5	Data Error	DE	When the FDC detects a CRC error in either the ID field or the data field, this flag is set.
D_4	Over Run	OR	If the FDC is not serviced by the main-systems during data transfers, within a certain time interval, this flag is set.
D_3			Not used. This bit always 0 (low).
D_2	No Data	ND	During execution of READ DATA, WRITE DELETED DATA or SCAN Command, if the FDC cannot find the Sector specified in the IDR Register, this flag is set.
			During executing the READ ID Command, if the FDC cannot read the ID field without an error, then this flag is set.
			During the execution of the READ A Cylinder Command, if the starting sector cannot be found, then this flag is set.
D_1	Not Writable	NW	During execution of WRITE DATA WRITE DELETED DATA or Format A Cylinder Command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D_0	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the Index hole twice, then this flag is set.
			If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in Data Field) of Status Register 2 is set.
			STATUS REGISTER 2
D_7			Not used. This bit is always 0 (low.)
D_6	Control Mark	CM	During executing the READ DATA or SCAN Command, if the FDC encounters a Sector which contains a Deleted Data Address Mark, this flag is set.
D_5	Data Error in Data Field	DD	If the FDC detect a CRC error in the data field then this flag is set.
D_4	Wrong Cylinder	WC	This bit is related with the ND bit. and when the contents of C on the medium is different from that stored in the IDR, this flag is set.
D_3	Scan Equal Hit	SH	During execution, the SCAN Command, if the condition of "equal" is satisfied, this flag is set.
D_2	Scan Not Satisfied	SN	During executing the SCAN Command, if the FDC cannot find a Sector on the cylinder which meets the condition, then this flag is set.
D_1	Bad Cylinder	BC	This bit is related with the ND bit, and when the content of C on the medium is different from that stored in the IDR and the content of C is FF, then this flag is set.
D_0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.
			STATUS REGISTER 3
D_7	Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
D_6	Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
D_5	Ready	RDY	This bit is used to indicate the status of the Ready signal from the FDD.
D_4	Track 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
D_3	Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD.
D_2	Head Address	HD	This bit is used to indicate the status of Side Select signal to the FDD.
D_1	Unit Select 1	US 1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D_0	Unit Select 0	US 0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

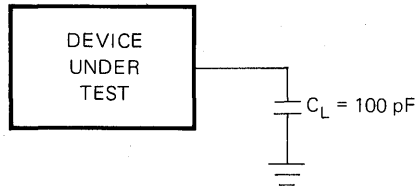
A.C. Testing Input, Output Waveform

INPUT/OUTPUT



A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0"

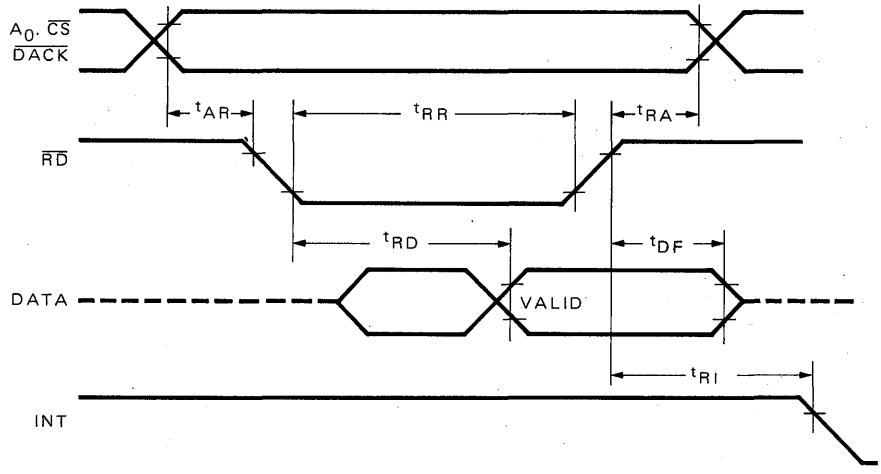
A.C. Testing Load Circuit



C_L = 100 pF
C_L INCLUDES JIG CAPACITANCE

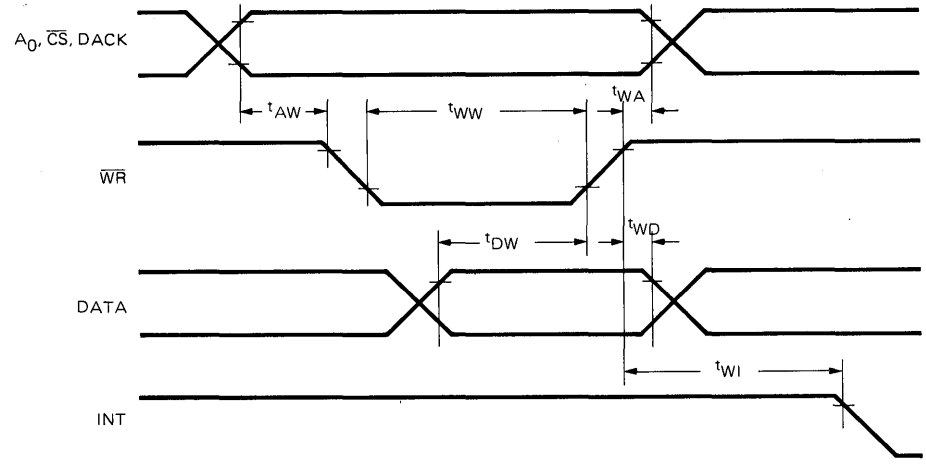
Waveforms

PROCESSOR READ OPERATION

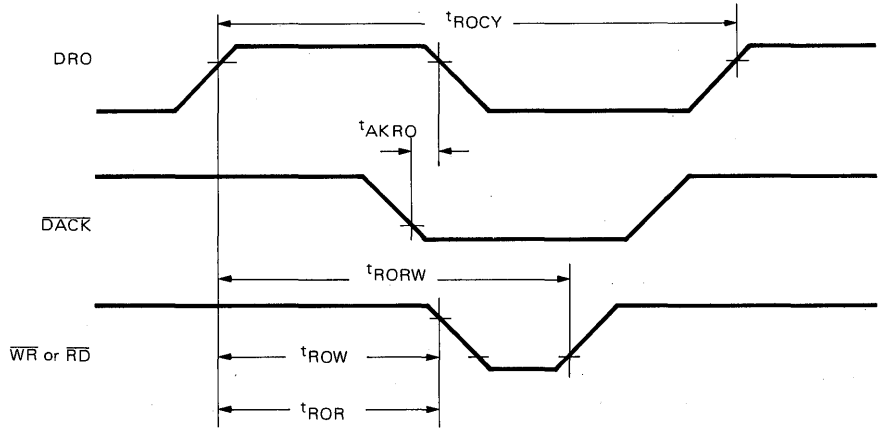


Waveforms (Continued)

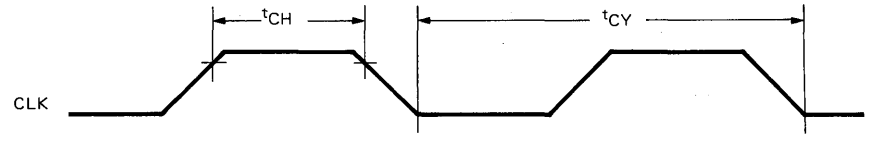
PROCESSOR WRITE OPERATION



DMA OPERATION

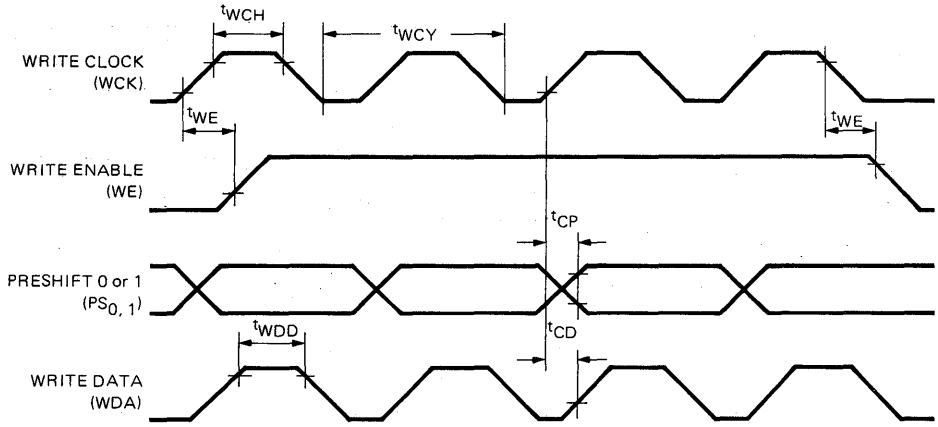


CLOCK TIMING



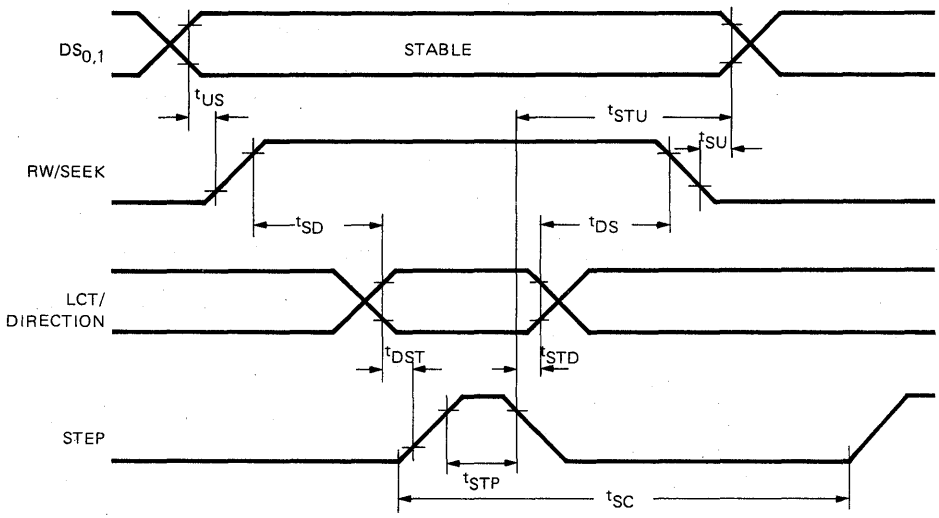
Waveforms (Continued)

FDD WRITE OPERATION

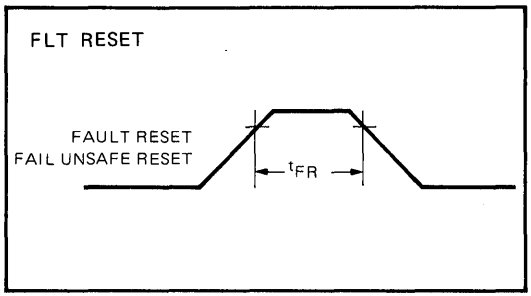


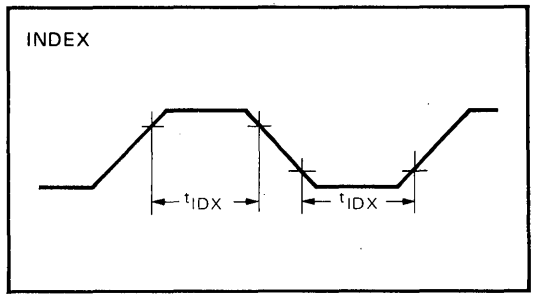
	PRESHIFT 0	PRESHIFT 1
NORMAL	0	0
LATE	0	1
EARLY	1	0
INVALID	1	1

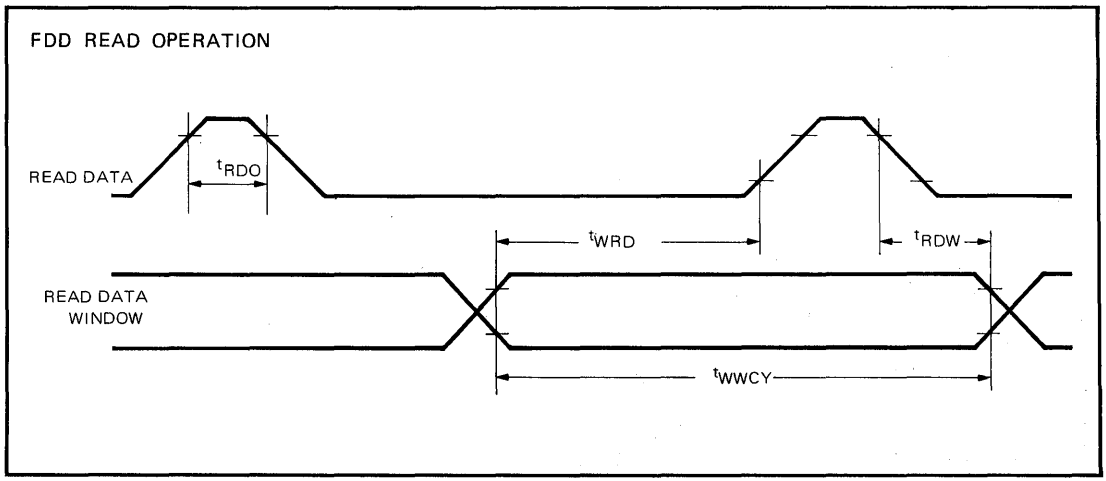
SEEK OPERATION

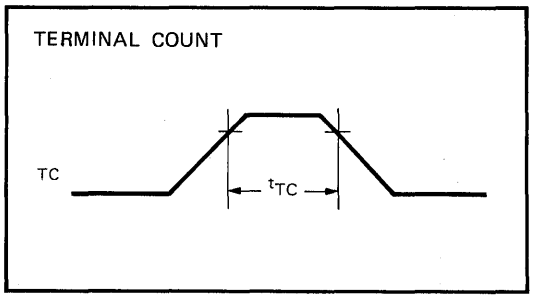


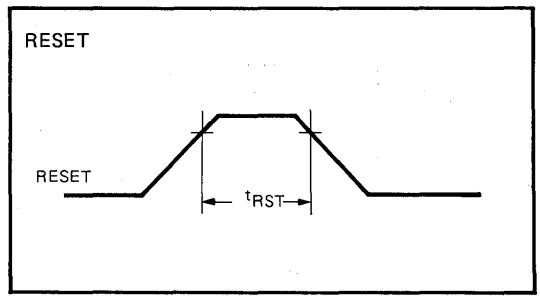
Waveforms (Continued)











Ordering Information

Part Number	Operation Clock	Package
UM8272A – 4	4 MHz	Plastic
UM8272A	8 MHz	Plastic

UM9228-1

Floppy Data Separator

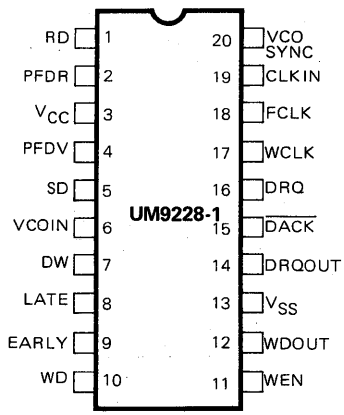
Features

- Floppy Data Separator
  - Performs complete data separation function with a little external circuit for floppy disk drives
  - Separates MFM encoded data
  - 5¼" double density compatible
- Early and late 250 ns write precompensation
- External 16 MHz clock required
- Compatible with the FDC 765A (8272A) floppy disk controllers
- DMA interface logic
- CMOS technology
- Single + 5 Volt supply
- TTL compatible
- For IBM PC disk drives especially

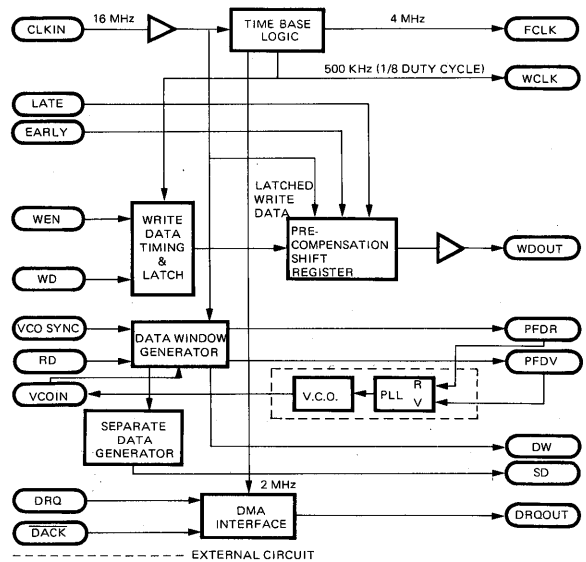
General Description

The UM9228-1 is an CMOS integrated circuit designed to complement the 765A (8272A) type of floppy disk controller chip; especially for IBM PC. It incorporates a data separator, write precompensation logic, and DMA interface logic. A FDC 765A together with UM9228-1 and some buffers drive and decoder can be formed a IBM PC diskette adapter. The UM9228-1 operates from a +5 Volt supply and simply requires a 16 MHz external clock input. All input and output are TTL compatible. The UM9228-1 is available for 5¼" double density disk controller.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Ambient temperature under bias, T_A . . . . . 0 to + 70°C
Storage temperature, T_{STG} . . . . . −55 to + 125°C
Applied voltage on any pin with respect to ground
. . . . . −0.3 to + 8V
Power dissipation, P_D 0.5W

*Comments

Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

D.C. Electrical Characteristics

(T_A = 0 to 70°C, V_{CC} = 5V ± 5% unless otherwise specified.)

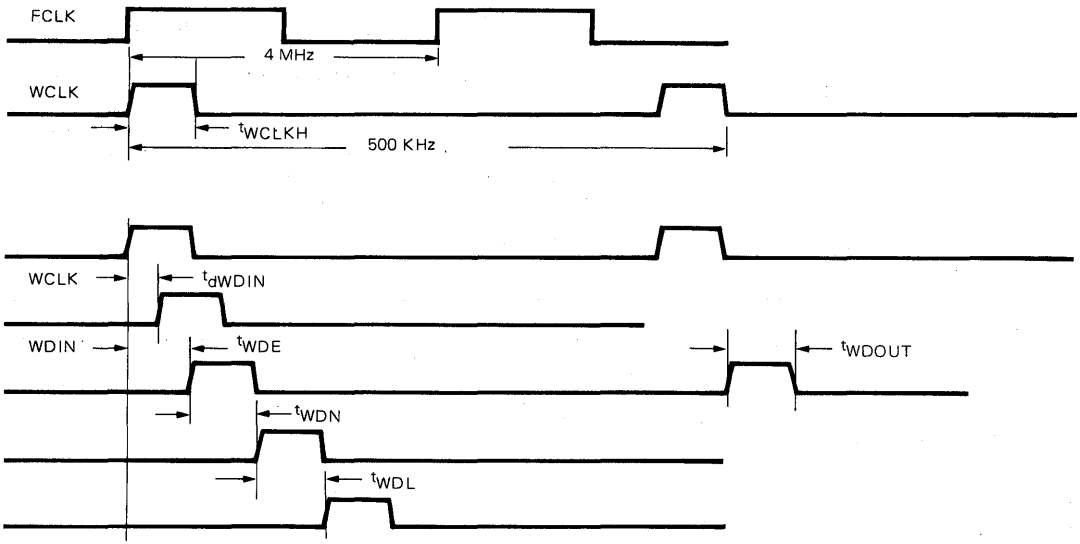
Parameter	Test Conditions	Limits			Units
		Min.	Typ.	Max.	
Input Voltage Low Level V_{IL} High Level V_{IH}		 −0.3 2.0		 0.8 V_{CC}	 V V
Standby Current I_{ST}				10	μA
Input Current (for all input) Low Level I_{IL} High Level I_{IH}	 V_{IH} = 2.7V V_{IL} = 0.4V			 −200 20	 μA μA
Output Current (for all input) Low Level I_{OL} High Level I_{OH}	 V_{OL} = 0.4V V_{OH} = 4.5V	 4 −500			 mA μA
Power Supply Current I_{CC}	CLKIN = 16 MHz VCOIN = 4 MHz			10	mA
Input Leakage Current I_{IL}				10	μA
Input Capacitance C_{IN}				10	pF

A.C. Electrical Characteristics

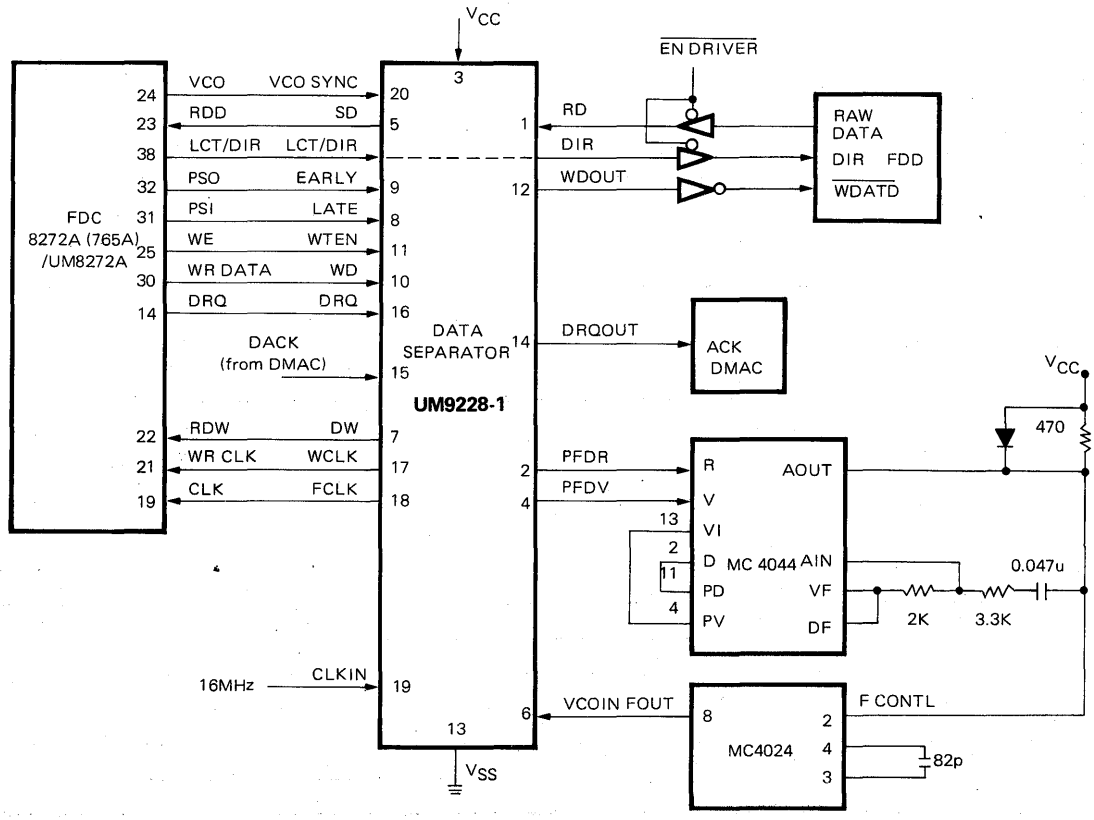
(T_A = 0 to 70°C, V_{CC} = 5V ± 5%, CLKIN = 16 MHz, VCOIN = 4 MHz)

Parameter	Limits			Units
	Min.	Typ.	Max.	
CLKIN frequency	1		16	MHz
VCOIN frequency	0		4	MHz
VCOIN DUTY CYCLE	30	50	70	%
DRQ to DRQOUT Delay t_{dDRQ}			2.0	μs
t_{WCLKH}		250		ns
t_{WDOUT}		250		ns
t_{dWDIN}	0		200	ns
t_{WDE}		250		ns
t_{WDN}		250		ns
t_{WDL}		250		ns

Precompensation



Application Circuits



Pin Description

Pin No.	Symbol	I/O	Descriptions
1	RD	I	Read Data: Data read from FDD.
2	PFDR	O	Reference Data Sample Pulse. This signal is applied to the reference input of a PLL circuit. See block diagram.
3	V_{CC}	I	+5 Volt power supply
4	PFDV	O	This output is connected to an input of a PLL circuit. See block diagram.
5	SD	O	Separate Data: This output is the generated data pulse derived from the RD input.
6	VCOIN	I	This signal is the V.C.O. output of a PLL circuit used to generate data window.
7	DW	O	Data Window: This is derived from RD input to be applied to FDC.
8	LATE	I	See Fig. 3.
9	EARLY	I	See Fig. 3.
10	WD	I	Write Data: The write data stream from the floppy disk controller.
11	WEN	I	Write Enable: This input is from FDC starting the write operation.
12	WDOUT	O	Write Data Output: The precompensated write data stream to the drive.
13	V_{SS}	I	Ground
14	DRQOUT	O	Data Request Output: This is delayed DRQ signal from FDC.
15	$\overline{DACK}$	I	DMA Acknowledge: This is direct memory access acknowledge from DMA controller.
16	DRQ	I	DMA Request: This is high when FDC make a DMA request.
17	WCLK	O	Write Clock: This signal is the write clock to the floppy disk controller.
18	FCLK	O	FDC Clock: This output is the master clock to the floppy disk controller.
19	CLKIN	O	Clock Input: This input is connected to a external 16 MHz clock input.
20	VCC SYNC	I	This is connected to VCO output pin of FDC 765.

Operational Description

DATA SEPARATOR

UM9228-1 is used with a external PLL circuit (see fig. 1) to detect the leading edges of the disk data pulse and adjust the phase of the internal clock to provide the data window (DW) clock.

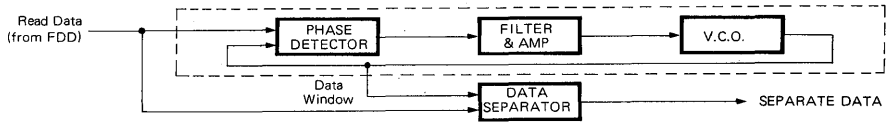


Fig. 1: Data Window Generator

The data window clock frequency is normally 250 KHz. See fig. 2.

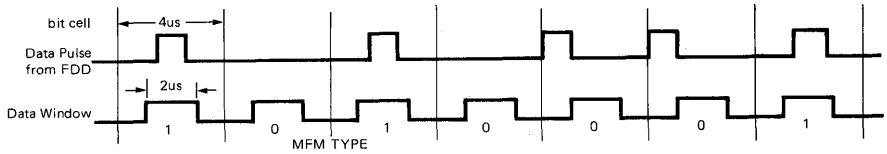
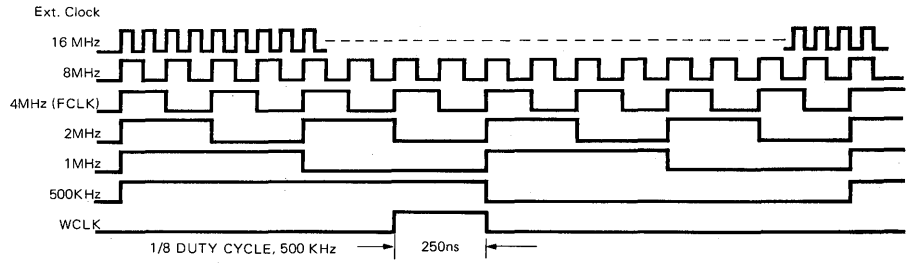


Fig. 2: Data Window

TIME BASE LOGIC

It compromises 5 stages of ripple counter and a duty cycle clamping circuit. The write clock (WCLK) duty cycle is 1/8.



WRITE PRECOMPENSATION

The desired precompensation delay (250 ns) is determined by the state of EARLY and LATE inputs of UM9228-1.

	Early	Late
Nominal	0	0
Late	0	1
Early	1	0
Invalid	1	1

Fig. 3: Write Precompensation State

DMA INTERFACE

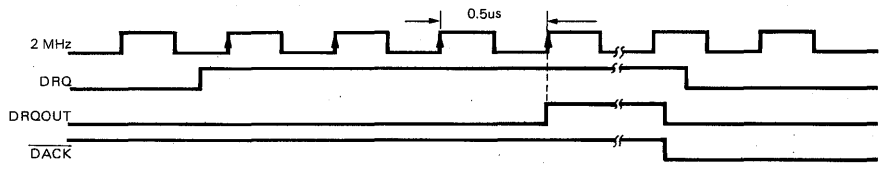


Fig. 4: DMA Interface Timing

When requiring data read/write, FDC will check $\overline{\text{DACK}}$ from DMAC and will set DRQ (low to high) if $\overline{\text{DACK}}$ is high.
The DMA Interface delay DRQ from FDC by 4 stage shift register as the timing shown above. This delay will prevent cpu from being busy doing DMA without adequate system operation.

UM8326/8326B

Floppy Disk Data Separator (FDDS)

Features

- Performs complete data separation function for floppy disk drives
- Separates FM or MFM encoded data from any magnetic media
- Eliminates several SSI and MSI devices normally used for data separation
- No critical adjustments required
- Compatible with standard microsystems' FDC 1791, FDC 1793 and other floppy disk controllers
- Small 8-pin dual-in-line package
- +5 Volt only power supply
- TTL compatible inputs and outputs

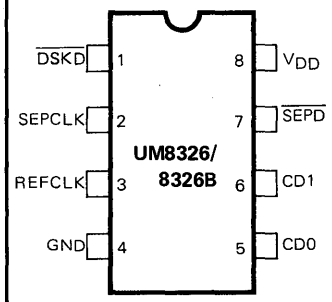
General Description

The Floppy Disk Data Separator provides a low cost solution to the problem of converting a single stream of pulses from a floppy disk drive into separate clock and data inputs for a Floppy Disk Controller.

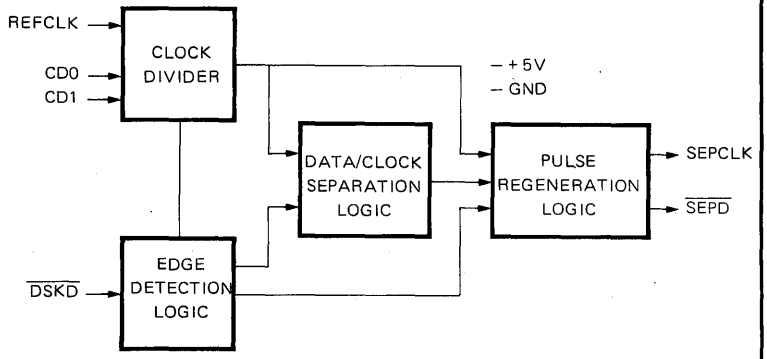
The FDDS consists primarily of a clock divider, a long-term timing corrector, a short-term timing corrector, and re-clocking circuitry. Sypplied in an 8-pin Dual-in-Line package to save board real estate, the FDDS operates on +5 volts only and is TTL compatible on all inputs and outputs.

The UM8326 is available in two versions; the UM8326, which is intended for 5¼" disks and the UM8326B for 5¼" and 8" disks.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Operating Temperature Range . . . . . 0°C to + 70°C
Storage Temperature Range . . . . . −55°C to + 150°C
Positive Voltage on any Pin, with respect to ground
. . . . . + 8.0V
Negative Voltage on any Pin, with respect to ground
. . . . . − 0.3V

Note:
When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

*Comments

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics

D.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{DD} = +5V ± 5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Units	Conditions
INPUT VOLTAGE LEVELS					
Low Level V_{IL}			0.8	V	
High Level V_{IH}	2.0			V	
OUTPUT VOLTAGE LEVELS					
Low Level V_{OL}			0.4	V	I_{OL} = 1.6 mA
High Level V_{OH}	2.4			V	I_{OH} = −100μA
INPUT CURRENT					
Leakage I_{IL}			10	μA	$0 \leqslant V_{IN} \leqslant V_{DD}$
INPUT CAPACITANCE					
All Inputs			10	pF	
POWER SUPPLY CURRENT					
I_{DD}			60	mA	

A.C. CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
f_{CY}	REFCLK Frequency	0.2		4.3	MHz	UM8326
f_{CY}	REFCLK Frequency	0.2		8.3	MHz	UM8326B
t_{CKH}	REFCLK High Time	50		2500	ns	
t_{CKL}	REFCLK Low Time	50		2500	ns	
t_{SDON}	REFCLK to SEPD "ON" Delay		100		ns	
t_{SDOFF}	REFCLK to SEPD "OFF" Delay		100		ns	
t_{SPCK}	REFCLK to SEPCLK Delay			100	ns	
t_{OLL}	DSKD Active Low Time	0.1		100	μs	
t_{OLH}	DSKD Active High Time	0.2		100	μs	

Pin Description

Pin No.	Name	Symbol	Function
1	$\overline{\text{Disk Data}}$	$\overline{\text{DSKD}}$	Data input signal direct from disk drive. Contains combined clock and data waveform.
2	Separated Clock	SEPCLK	Clock signal output from the FDDS derived from floppy disk drive serial bit stream.
3	Reference Clock	REFCLK	Reference clock input
4	Ground	GND	Ground
5, 6	Clock Divisor	CD0 CD1	CD0 and CD1 control the internal clock divider circuit. The internal clock is a submultiple of the REFCLK according to the following table: CD1 CD0 Divisor 0 0 1 0 1 2 1 0 4 1 1 8
7	$\overline{\text{Separated Data}}$	$\overline{\text{SEPD}}$	$\overline{\text{SEPD}}$ is the data output of the FDDS
8	Power Supply	V_{DD}	+5 volt power supply

Operational Description

A reference clock (REFCLK) of between 2 and 8 MHz is divided by the FDDS to provide an internal clock. The division ratio is selected by inputs CD0 and CD1. The reference clock and division ratio should be chosen per table 1.

The FDDS detects the leading edges of the disk data pulses and adjusts the phase of the internal clock to provide the SEPARATED CLOCK output.

Separate short and long term timing correctors assure accurate clock separation.

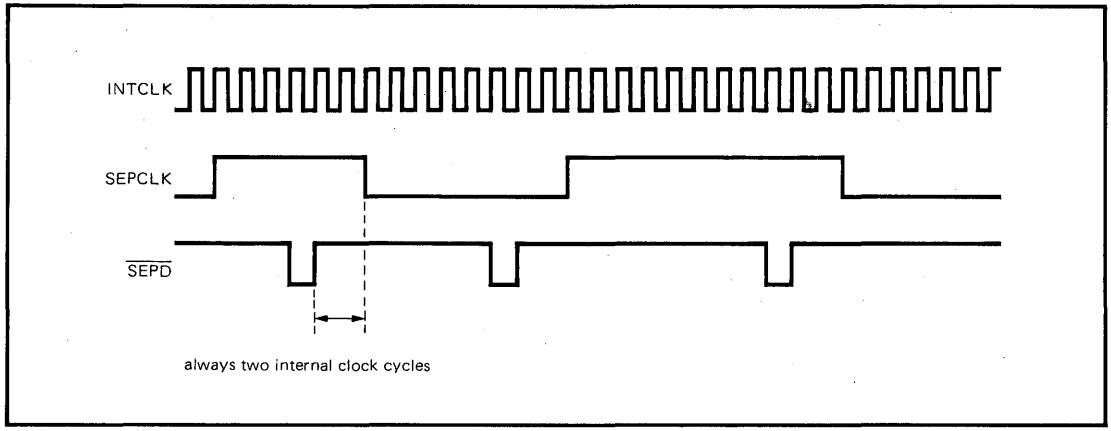
The internal clock frequency is nominally 16 times the SEPCLK frequency. Depending on theinternal timing correction, the internal clock may be a minimum of 12 times to a maximum of 22 times the SEPCLK frequency.

The reference clock (REFCLK) is divided to provide the internal clock according to pins CD0 and CD1.

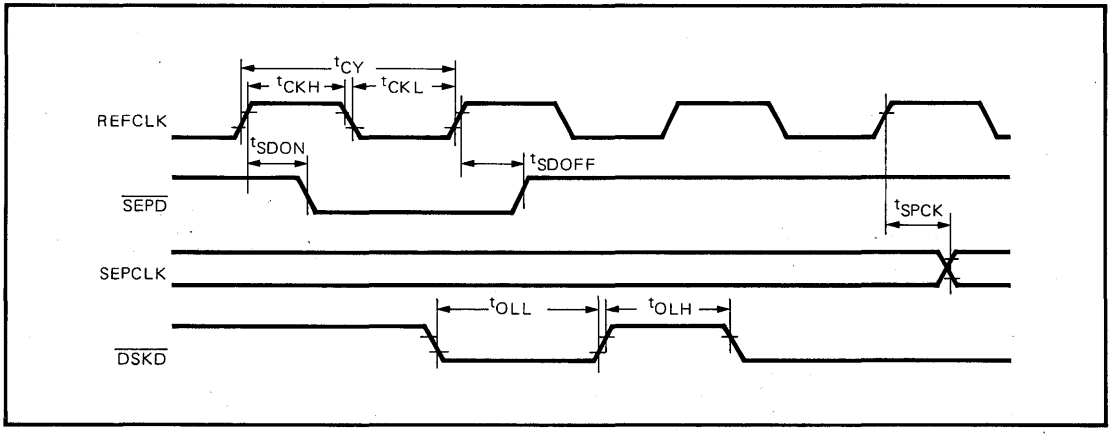
Table 1. Clock Divider Selection Table

Drive (8" or 5¼")	Density (DD or SD)	REFCLK MHz	CD1	CD0	Remarks
8	DD	8	0	0	
8	SD	8	0	1	Select either one
8	SD	4	0	0	
5¼	DD	8	0	1	Select either one
5¼	DD	4	0	0	
5¼	SD	8	1	0	
5¼	SD	4	0	1	Select any one
5¼	SD	2	0	0	

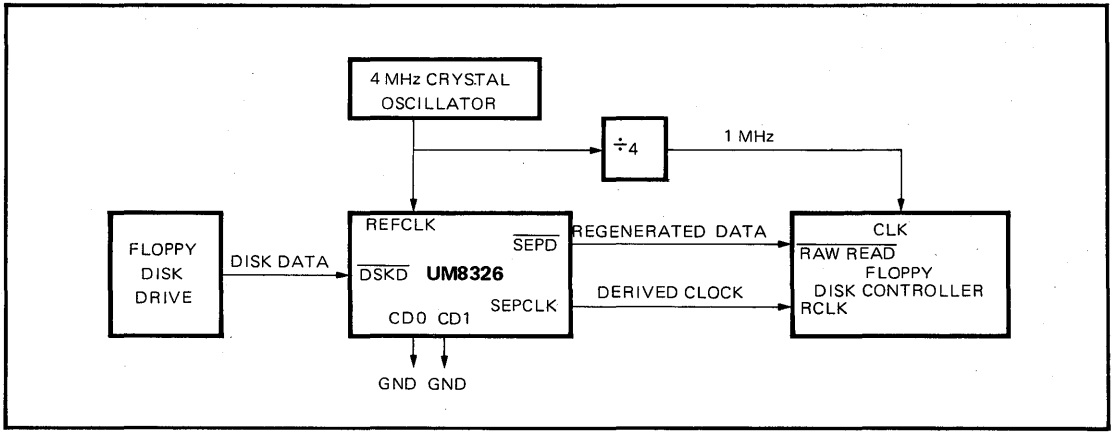
Timing Diagram (1)



Timing Diagram (2)



Typical System Configuration (5¼" Drive, Double Density)



Comparison of Data Separator (UM9228-1, UM8329, UM8326)

PINOUT COMPARISON

Function	UM9228-1	UM8329	UM8326	Remarks
Power Supply:				
V_{CC}	Pin 3 V_{CC}	Pin 20 V_{CC}	Pin 8 V_{DD}	
V_{SS}	13 V_{SS}	10 Ground	4 GND	
Precompensation:				
EARLY	9 EARLY	13 EARLY	-------	See B
LATE	8 LATE	14 LATE	-------	
Amount Control	-------	17 P0	-------	
	-------	18 P1	-------	
	-------	19 P2	-------	
Read Data:				
From FDD	1 RD	1 DSKD	1 DSKD	
To FDC	5 SD	6 SPED	7 SPED	
Data Row	7 DW	5 SEPCLK	2 SEPCLK	
Write Data:				
From FDC	10 WD	12 WDIN	-------	Sec C
To FDD	12 WDOUT	7 WDOUT	-------	
Write Enable	11 WEN	-------	-------	
Write Clock	17 WCLK	9 CLKOUT	-------	
179X/765MODE	-------	2 FDCSEL	5 CD0	See D
Density	-------	3 MINI	6 CD1	
	-------	4 DENS	-------	
MASTER CLK to FDC	18 FCLK	8 HLT/CLK	-------	
Extermal Clock I/P	19 CLKIN	11 XTAL/CLKIN	3 REFCLK	
TEST	-------	16 TEST	-------	
179X/MODE ESP	-------	15 HLD	-------	
DMA	16 DRO	-------	-------	See E
	15 BACK	-------	-------	
	14 DROO/P	-------	-------	
VFO	2 PROR	-------	-------	See F
	4 PFDV	-------	-------	
	6 VCOIN	-------	-------	
VCO SYN	20 VCOSNC	-------	-------	

TIME PRECOMPENSATION

It is a more advanced function to solve "peak Shift" problem. UM9228-1 defines compensation time to be 250ns according to IBM PC design. UM8329's compensation time is programmable, yet UM8326 does not have this function.

WRITE DATA

UM9228-1 and UM8329 have write data function in IC, but UM8326 does not; and UM9228-1 has the "write enable" pin to guarantee write function unfail.

MODE SELECT

UM8329 and UM8326 allow user to select different FDCs and to interface different FDCs; but UM9228-1 is especially used in 5½ FDD (MFM coding) interface.

DMA MODE

UM9228-1 can accept DMA request and define the delay time between two different DMA requests to be 5 μs to guarantee system can work normally.

VFO CIRCUIT

Because UM9228-1 does not have VFO and PLL circuit, user must combine MC4024 and MC4044 to build a complete data separator. Please see UM9228-1 application circuit intensively.

Ordering Information

Part Number	Frequency Option	Package Type
UM8326	4MHz	Plastic
UM8326B	8MHz	Plastic

UM8329/8329T/8329B/8329BT

Floppy Disk Interface Circuit

Features

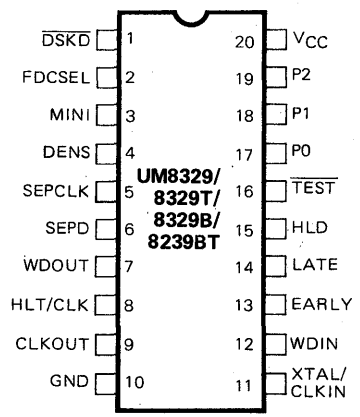
- Digital date separator
  - Performs complete data separation function for floppy disk drives
  - Separates FM and MFM encoded data
  - No critical adjustments necessary
  - 5¼" and 8" compatible
- Variable write precompensation
- Internal crystal oscillator circuit
- Track-selectable write precompensation
- Retriggerable head-load timer
- Compatible with the FDC 179X, 8272A, and other standard floppy disk controllers
- SAN-III MOS N-CHANNEL TECHNOLOGY
- Single + 5 volt supply
- TTL compatible

General Description

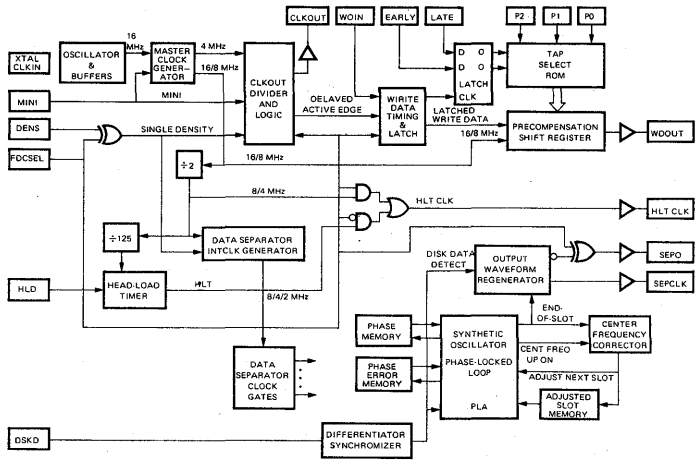
The UM8329/B is an MOS integrated circuit designed to complement either the 179X or 8272A (765A) type of floppy disk controller chip. It incorporates a digital data separator, write precompensation logic, and a head-load timer in one 0.3-inch wide 20-pin package. A single pin will configure the chip to work with either the 179X or 8272A type of controller. The UM8329/B provides a number of different dynamically selected precompensation values so that different values may be used when writing to the inner and outer tracks of the floppy disk drive. The UM8329/B operates from a +5V supply and simply requires that a 16 or 8 MHz crystal or TTL-level clock be connected to the XTAL/CLKIN pin. All inputs and outputs are TTL compatible.

The UM8329 is available in four versions: The UM8329/T are intended for 5¼" disks and the UM8329B/T for 5¼" and 8" disks. The UM8329/B have an internal crystal oscillator circuit; the UM8329T/BT require an external clock.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . . −55°C to +150°C
Positive Voltage on any I/O Pin, with respect to ground . . . . . +7.0V
Negative Voltage on any I/O Pin, with respect to ground . . . . . −0.3V
Power Dissipation 0.75W

Note: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is siwtched on and off. In addition, voltage transients on the AC power line may appear on the DC output.

Comments*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

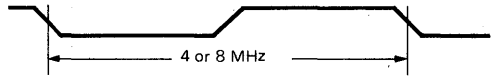
Parameter	Min.	Typ.	Max.	Units	Conditions
D.C. Characteristics					
INPUT VOLTAGE					
Low Level V_{IL}	−0.3		0.8	V	Except XTAL/CLKIN
High Level V_{IH}	2.0		(V_{CC})	V	
XTAL/CLKIN INPUT VOLTAGE					
Low Level	−0.3		0.8	V	
High Level	2.4		(V_{CC})	V	
OUTPUT VOLTAGE					
Low Level V_{OL}			0.4	V	I_{OL} = 1.6 mA except HLT/CLK
					I_{OL} = 0.4 mA, HLT/CLK only
High Level V_{OH}	2.4			V	I_{OH} = −100 μA except HLT/CLK
					I_{OH} = −400 μA, HLT/CLK only
POWER SUPPLY CURRENT					
I_{CC}			100	mA	
INPUT LEAKAGE CURREN					
I_{IL}			10	μA	V_{IN} = 0 to V_{CC}
INPUT CAPACITANCE			10	pF	Except CLKIN
C_{IN}			25	pF	CLKIN only

Electrical Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

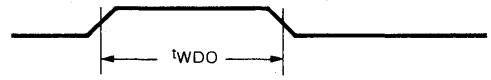
Parameter	Min.	Typ.	Max.	Units	Conditions
A.C. Characteristics	All times assume CLKIN = 16 MHz unless otherwise specified)				
XTAL/CLKIN Frequency	3.95	16	16.2	MHz	UM8329B
	3.95	8	8.1	MHz	UM8329T
XTAL/CLKIN Duty Cycle	25		75	%	
t_{CIKOH}	465	500	515	ns	FDCSEL = low; MINI = high.
	215	250	265	ns	FDCSEL = low; MINI = low.
	90	125	140	ns	FDCSEL = high.
t_{WdO}	280	312.5	350	ns	Time Doubles with MINI = 1
t_d	50		400	ns	
t_{dNEC}	0		400	ns	
t_{WdE}	500	562.5	625	ns	9 clock times ± 1 clock time
t_{WdN}					See fig. 2
t_{WdL}					See fig. 2
t_S	1.0			μs	

A.C. Timing Characteristics

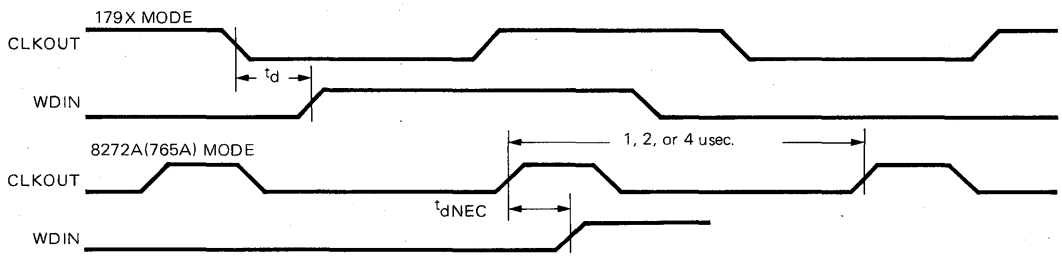
HLT/CLK (8272A MODE)



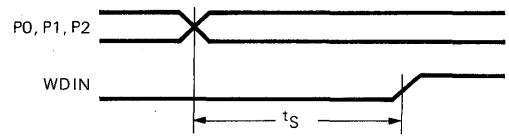
WDOUT PULSE WIDTH



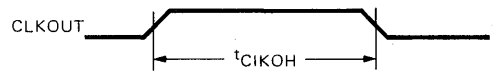
CLKOUT VS. WDIN TIMING



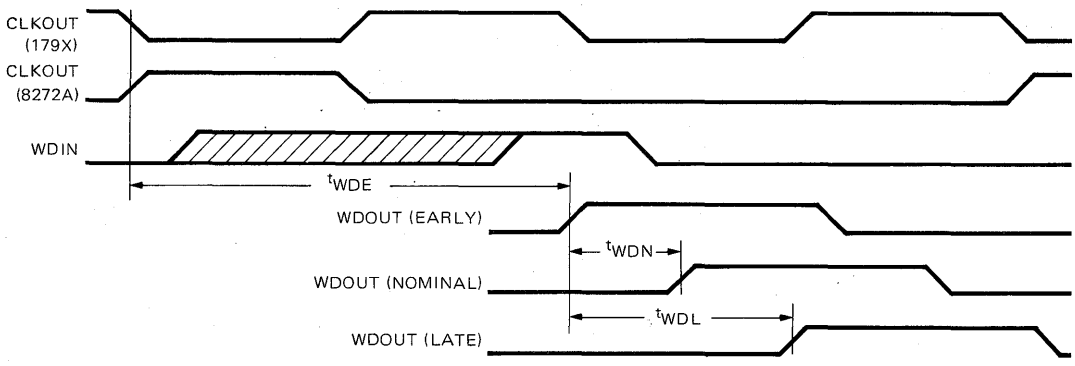
SET-UP TIME P0, P1 AND P2 TO WDIN



CLKOUT



PRECOMPENSATION

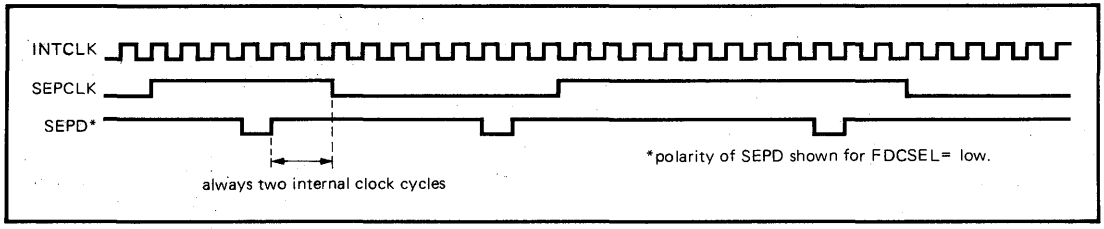


Ref. to Fig. 2 for t_p (precompensation) value

Pin Description

Pin No.	Symbol	I/O	Descriptions
1	$\overline{DSKD}$	I	This input is the raw read data received from the drive. (This input is active low.)
2	FDCSEL	I	This input signal, when low programs the UM8329/B for a 179X type of LSI controller. When FDCSEL is high, the UM8329/B is programmed for a 8272A (765A) type of controller. (See fig. 4.)
3	MINI	I	The state of this input determines whether the UM8329/B is configured to support 8" or 5¼" floppy disk drive interfaces. It is used in conjunction with the DENS input to prescale the clock for the data separator. The state of this input also alters the CLKOUT frequency, the precompensation value, the head load delay time (when in 179X mode) and the HLT/CLK frequency (when in 8272A mode). (See figs. 2, 3, and 4.)
4	DENS	I	The state of this input determines whether the UM8329/B is configured to support single density (FM) or double density (MFM) floppy disk drive interfaces. It is used in conjunction with the MINI input to prescale the clock for the data separator. The state of this input also alters the CLKOUT frequency when in the 8272A mode. (See figs. 2, 3, and 4.)
5	SEPCLK	O	A square-wave window clock signal output derived from the $\overline{DSKD}$ input.
6	SEPD	O	This output is the regenerated data pulse derived from the raw data input ($\overline{DSKD}$). This signal may be either active low or active high as determined by FDCSEL (pin 2).
7	WDOUT	O	The precompensated WRITE DATA stream to the drive.
8	HLT/CLK	O	When in the 8272A mode (FDCSEL high), this output is the master clock to the floppy disk controller. When in the 179X mode, this signal goes high after the head load delay has occured following the HLD input going high. This output is retriggerable. (See fig. 3.)
9	CLKOUT	O	This signal is the write clock to the floppy disk controller. Its frequency is determined by the state of the MINI, DENS, and FDCSEL input pins. (See fig. 3.)
10	GND		Ground
11	XTAL/CLKIN	I	This input is for direct connection to a 16 MHz or 8 MHz crystal UM8329/B only). The other pin of the crystal is grounded. XTAL/CLKIN may alternatively be connected to a single-phase TTL-level clock. The UM8329T and BT require an external TTL-level clock.
12	WDIN	I	The write data stream from the floppy disk controller.
13	EARLY	I	When this input is high, the current WRITE DATA pulse will be written early to the disk.
14	LATE	I	When this input is high, the current WRITE DATA pulse will be written late to the disk. When both EARLY and LATE are low, the current WRITE DATA pulse will be written at the nominal position.
15	HLD	I	This input is only used in 179X mode. A high level at this input causes a high level on the HLT/CLK output after the specified head-load time delay has elapsed. The delay is selected by the state of the MINI output. (See fig. 3.)
16	$\overline{TEST}$	I	This input (when low) decreases the head-load time delay and initializess the data separator. This pin is for test purposes only. This input has an internal pull-up resistor and should be tied high or disconnected for normal operation.
17	P0	I	P2-P0 select the amount of precompensation applied to the write data. (See fig. 2.)
18	P1	I	
19	P2	I	
20	V_{CC}		+5 VOLT SUPPLY

Operational Description



DATA SEPARATOR

The XTAL/CLKIN input clock is internally divided by the UM8329/B to provide an internal clock. The division ratio is selected by the FDCSEL, MINI and DENS inputs depending on the type of drive used. (See fig. 1.)

The UM8329/B detects the leading (negative) edges of the disk data pulses and adjusts the phase of the internal clock to provide the SEPCLK output.

Separate short- and long-term timing correctors assure accurate clock separation.

The SEPCLK frequency is nominally 1/16 the internal clock frequency. Depending on the internal timing correction, the duration of any SEPCLK half-cycle may vary from a nominal of 8 to a minimum of 6 and a maximum of 11 internal clock cycles.

Inputs			f(XTAL/CLKIN) /f(INTCLK)
FDCSEL	DENS	MINI	
0	0	0	2
0	0	1	4
0	1	0	4
0	1	1	8
1	0	0	4
1	0	1	8
1	1	0	2
1	1	1	4

Fig. 1.

PRECOMPENSATION

The desired precompensation delay is determined by the state of the P0, P1 and P2 inputs of the UM8329/B as per fig. 2. Logic levels present on these pins may be changed dynamically as long as the inputs are stable during the time the floppy disk controller is writing to the driver and the inputs meet the minimum setup time with respect to the write data from the floppy disk controller.

MINI	P2	P1	P0	Precomp Value
0	0	0	0	0 ns
0	0	0	1	62.5 ns
0	0	1	0	125 ns
0	0	1	1	187.5 ns
0	1	0	0	250 ns
0	1	0	1	250 ns
0	1	1	0	312.5 ns
0	1	1	1	312.5 ns
1	0	0	0	0 ns
1	0	0	1	125 ns
1	0	1	0	250 ns
1	0	1	1	375 ns
1	1	0	0	500 ns
1	1	0	1	500 ns
1	1	1	0	625 ns
1	1	1	1	625 ns

Note: All values shown are obtained with a 16 MHz reference clock. Multiply pre-comp values by two for 8 MHz operation.

Fig. 2 Write precompensation value selection

HEAD LOAD TIMER

The head load time delay is either 40 ms or 80 ms, depending on the state of MINI. (See fig. 3.) The purpose of this delay is to ensure that the head has enough time to engage properly. The head load timer is only used in the 179X mode; it is non-functional in the 8272A mode.

The FDC 179X initiates the loading of the floppy disk drive head by setting HLD high. The controller then waits the programmed amount of time until the HLT signal from the goes high before starting a read or write operation UM8329/B.

Inputs			Outputs	
FDCSEL	DENS	MINI	CLKOUT	HLT/CLK
0	0	0	2 MHz	40 ms*
0	0	1	1 MHz	80 ms*
0	1	0	2 MHz	40 ms*
0	1	1	1 MHz	80 ms*
1	0	0	500 KHz	8 MHz
1	0	1	250 KHz	4 MHz
1	1	0	1 MHz	8 MHz
1	1	1	500 KHz	4 MHz

Note: All values shown are obtained with a 16 MHz reference clock. Divide all frequencies and multiply all periods by two for 8 MHz operation.

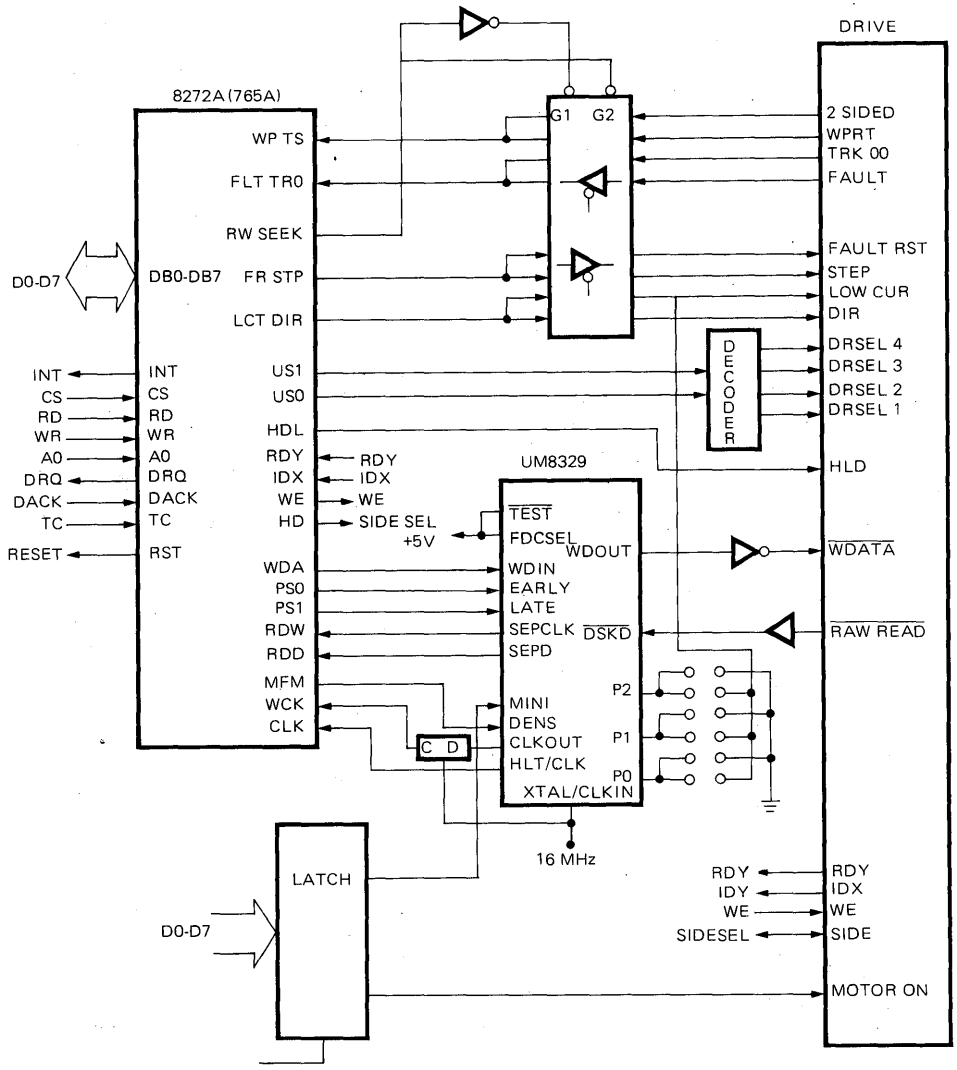
*May be mask programmed at factory to any value from 1 to 512 min is 15.625 μs increments (MINI low) or 1 to 1024 ms in 31.25 μs increments (MINI high).

Fig. 3. Clock and head load time delay selection

Inputs			Floppy Disk Drive Type	Floppy Disk Drive Density	Floppy Disk Controller Type
FDCSEL	DENS	MINI			
0	0	0	8" Drive	Double	179X
0	0	1	5¼" Drive	Double	179X
0	1	0	8" Drive	Single	179X
0	1	1	5¼" Drive	Single	179X
1	0	0	8" Drive	Single	8272A (765A)
1	0	1	5¼" Drive	Single	8272A (765A)
1	1	0	8" Drive	Double	8272A (765A)
1	1	1	5¼" Drive	Double	8272A (765A)

Fig. 4 Floppy disk drive and controller selection

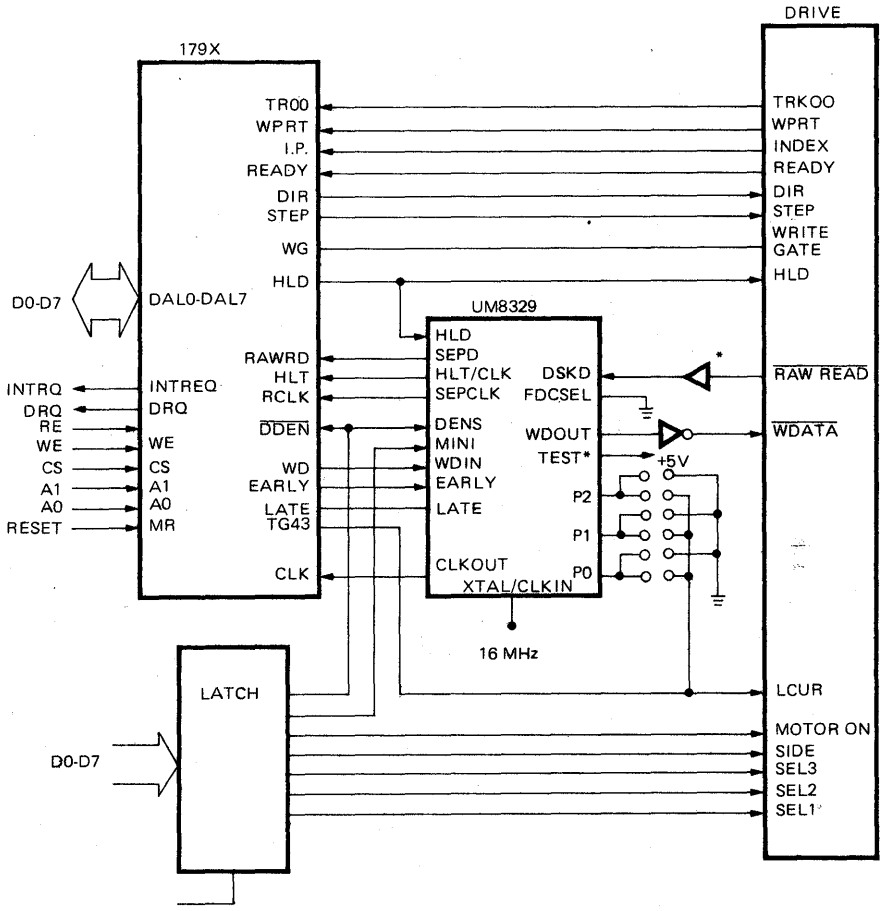
Typical System Implementation – 8272A(765A) FDC



* The UM8329T/BT, as all other NMOS integrated circuits, presents a high impedance on all inputs.

To avoid soft errors caused by transmission line effects and noise where there is long cabling between the floppy disk drive and the controller board, the use of a (noninverting) TTL schmidt-trigger input gate or bus transceiver is recommended at the DSKD input to the UM9229/B.

Typical System Implementation – 179X FDC



* The UM9229/B, as all other NMOS integrated circuits, presents a high impedance on all inputs.

To avoid soft errors caused by transmission line effects and noise where there is long cabling between the floppy disk drive and the controller board, the use of a (noninverting) TTL schmidt-trigger input gate or bus transceiver is recommended at the DSKD input to the UM9229/B.

Ordering Information

Part Number	Operation Type	Frequency Option	Package Type
UM8329	CLK/XTAL	8 MHZ	Plastic
UM8329B	CLK/XTAL	16 MHZ	Plastic
UM8329T	CLK	8 MHZ	Plastic
UM8329BT	CLK	16 MHZ	Plastic

Peripheral IC

Selection Guide

Part No.	Descriptions	Compatible Devices	Remarks	Page
UM2661	EPCI	SCN 2661	Three Kinds of Baud Rate	7–3
UM2681	DUART	SCN 2681		7–18
UM6520/A	PIA	SYP 6520	1, 2 MHz Version	7–41
UM6521/A	PIA Enhance 6520	SYP 6521	1, 2 MHz Version	7–52
UM6522/A	VIA	SYP 6522	1, 2 MHz Version	7–63
UM6532/A	RAM I/O Timer Array	SYP 6532	1, 2 MHz Version	7–80
UM6551/A	ACIA	SYP 6551	1, 2 MHz Version	7–87
UM82C01	Capacitance Keyboard Encoder			7–96
* UM82C284	Clock Generator and Ready Interface for iAPX 286 Processor	Intel 82284		7–107
* UM82C288	Bus Controller for iAPX 286 Processors	Intel 82288		7–108
UM82C55A	CMOS Programmable Peripheral Interface	HARRIS 82C55A		7–109
UM82C84A	Clock Generator & Driver	HARRIS 82C84A		7–128
UM82C88	Bus Controller	HARRIS 82C88		7–135
* UM8237A/ A-4/A-5	DMA Controller	Intel 8237A	3, 4, 5 MHz Version	7–142
UM8253/ 8253-5	Programmable Interval Timer	Intel 8253/ 8253-5		7–143
UM8254	Programmable Interval Timer	Intel 8254		7–154
UM8259A	Programmable Interrupt Controller	Intel 8259A		7–169
* UM82C6818	Real Timer Clock Plus RAM (RTC)	MC 146818		7–186
* UM82C8167	Microprocessor Real Time Clock	MM 58167A		7–187
* UM82450	ACE	NS 16450		7–188
* UM8250	ACE	NS 8250		7–188

* Under Development

UM2661

Enhanced Programmable Communications Interface

Features

Synchronous Operation

- 5 to 8-bit characters plus parity
- Single or double SYN operation
- Internal or external character synchronization
- Transparent or non-transparent mode
- Transparent mode DLE stuffing (Tx) and detection (Rx)
- Automatic SYN or DLE-SYN insertion
- SYN, DLE and DLE-SYN stripping
- Odd, even, or no parity
- Local or remote maintenance loop back mode
- Baud rate: dc to 1M bps (1X clock)

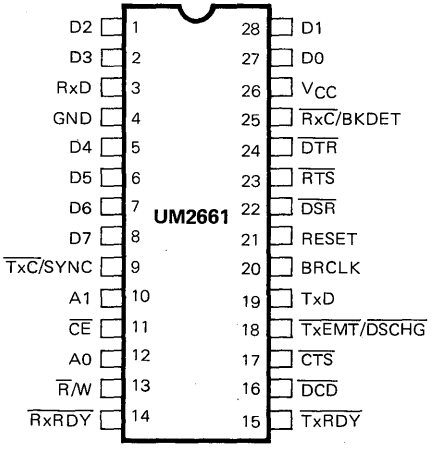
Asynchronous Operation

- 5 to 8-bit characters plus parity
- 1, 1½ or 2 stop bit transmitted
- Odd, even, or no parity
- Parity, overrun and framing error detection
- Line break detection and generation
- False start bit detection
- Automatic serial echo mode (echoplex)
- Local or remote maintenance loop back mode
- Baud rate: dc to 1M bps (1X clock)
  - dc to 62.5K bps (16X clock)
  - dc to 15.625K bps (64X clock)

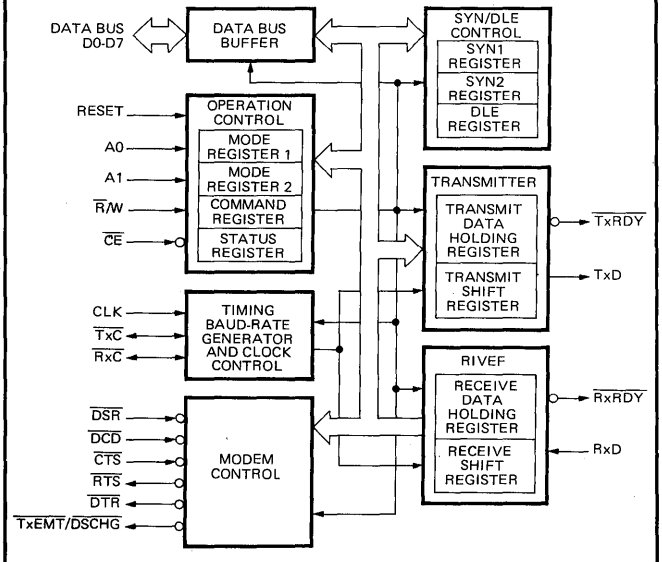
Other Features

- Internal or external baud rate clock
- 3 baud rate sets (2661-1, -2, -3)
- 16 internal rates for each set
- Double buffered transmitter and receiver
- Dynamic character length switching
- Full or half duplex operation
- TTL compatible inputs and outputs
- RxC and TxC pins are short circuit protected
- 3 open drain MOS outputs can be wire-ORed
- Single 5V power supply
- No system clock required
- 28-pin dual-in-line package

Pin Configuration



Block Diagram



Peripheral IC

Absolute Maximum Ratings*

Supply Voltage V_{CC} . . . . . −0.3V to +7.0V
Input/Output Voltage V_{IN} . . . . . −0.3V to +7.0V
Operating Temperature T_{OP} . . . . . 0°C to 70°C
Storage Temperature T_{STG} . . . . . −55°C to 150°C
Notice:
All inputs contain protection circuity to prevent damage to high static charges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

*Comments

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

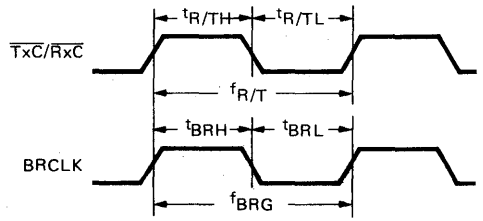
D.C. Characteristics

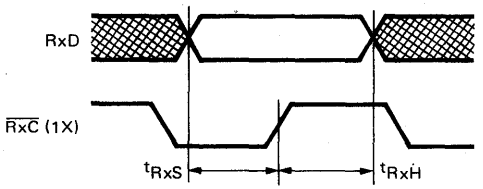
(V_{CC} = 5.0V ± 5%, T_A = 0-70°C, unless otherwise noted)

Characteristics	Symbol	Min.	Typ.	Max.	Units
Input High Voltage	V_{IH}	2.0		V_{CC}	V
Input Low Voltage	V_{IL}			0.8	V
Input Leakage Current V_{IN} = 0 to 5.5V	I_{IN}			10	μA
Input Leakage Current for High Impedance State	I_{TSI}			10	μA
Output High Voltage: I_{LOAD} = −400μA	V_{OH}	2.4			V
Output Low Voltage: I_{LOAD} = 2.2 mA	V_{OL}			0.4	V
Input Capacitance: f_c = 1 MHz	C_{IN}			20	pF
Output Capacitance	C_{OUT}			20	pF
Power Dissipation (V_{CC} = 5.25V)	P_D			650	mW

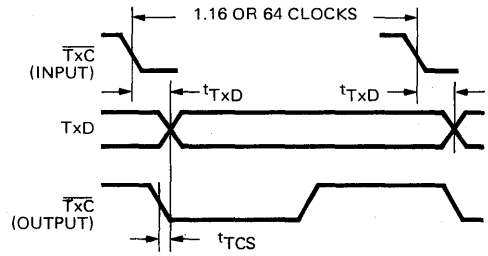
Receiver/Transmitter Signal Timing

CLOCKS





TRANSMIT TIMING

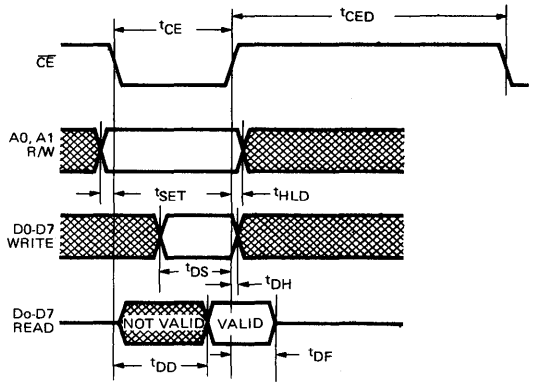


Symbol	Characteristics	Min.	Typ.	Max.	Units
$t_{R/TH}$	TxC or RxC HIGH	500			ns
$t_{R/TL}$	TxC or RxC LOW	500		1.0	ns
$f_{R/T}$	TxC or RxC freq.	DC		1.0	MHz
t_{BRH}	BRCLK HIGH	70			ns
t_{BRL}	BRCLK LOW	70			ns
f_{BRG}	BRCLK freq. (1)		4,9152		MHz
t_{RxS}	RxD SETUP	300			ns
t_{RxH}	RxD HOLD	350			ns
t_{TxD}	TxD DELAY FROM TxC C_L = 150 pF			650	ns
t_{TCS}	SKEW TxD vs TxC C_L = 150 pF		0		ns

Note: f_{BRG} = 4,9152 applicable for -1 and -2, f_{BRG} = 5,0688 for -3.

Read/Write Timing Characteristics

(V_{CC} = 5.0V ± 5%, T_A = 0-70°C, unless otherwise noted)



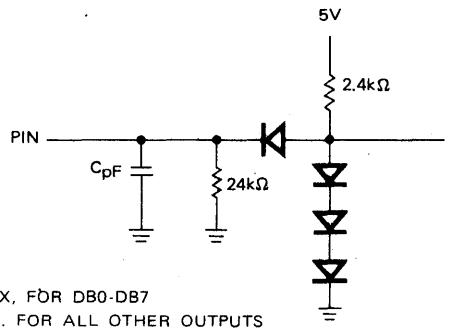
Symbol	Characteristics	Min.	Max.	Unit
t_{CE}	$\overline{CE}$ Pulse Width	250		ns
t_{CED}	$\overline{CE}$ to $\overline{CE}$ Delay	600		ns
t_{SET}	Address and R/W Set Up	10		ns
t_{HLD}	Address and $\overline{R}/W$ Hold	10		ns
t_{DS}	Write Data Set Up	150		ns
t_{DH}	Write Data Hold	0		ns
t_{DD}	Read Data Delay C_L = 150 pF		200	ns
t_{DF}	READ DATA HOLD C_L = 150 pF	10	100	ns

Table 1. Effect of MR17 and MR16 on Character Fill and Character Stripping (Synchronous Mode)

MR17	MR16	Mode	Synchronizing Sequence	Character Fill	Character(s) Stripped CR7=0, CR6=1
0	0	Double SYN Normal	SYN1-SYN2	SYN1-SYN2	SYN1 SYN1-SYN2(1)
1	0	Single SYN Normal	SYN1	SYN1	SYN1(1)
0	1	Double SYN Transparent	SYN1-SYN2	DLE-SYN1	DLE-SYN1(1) SYN1-SYN2(1) (Only Initial Synchronizing Sequence) DLE (also Sets SR3 if Parity Disabled and it is not Following a DLE or SYN1) In a DLE-DLE Sequence Only the First DLE is Stripped
1	1	Single SYN Transparent	SYN1	DLE-SYN1	DLE-SYN1(1) SYN1 (only Initial Synchronizing Sequence) DLE and DLE-DLE same as Double SYN Transparent

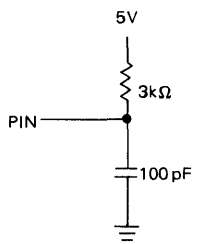
Note: Symbol indicates SYN DET status set upon detection of initial synchronizing characters and after SYNC has been achieved by detection of DLE-SYN1 pair.

Test Load



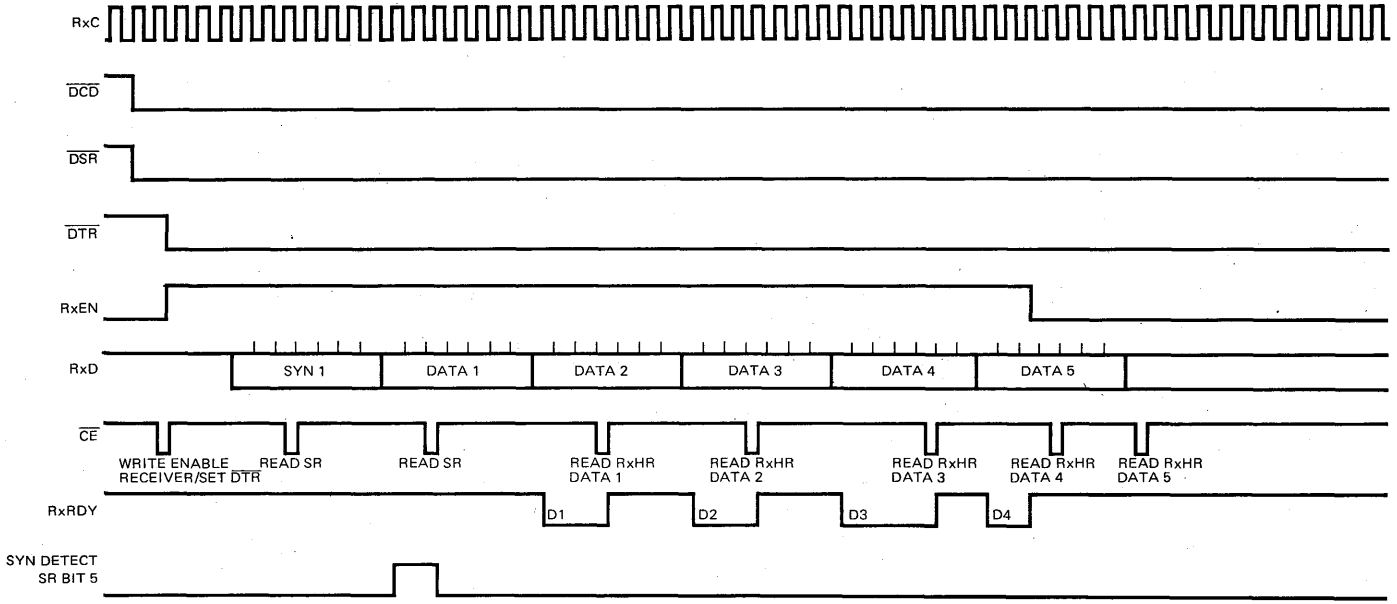
C = 130 pF MAX, FOR DB0-DB7
C = 30 pF MAX. FOR ALL OTHER OUTPUTS

OPEN COLLECTOR OUTPUT TEST LOAD



Peripheral IC

SYNCHRONOUS MODE 7-BIT CHARACTER, NO PARITY



ASYNCHRONOUS MODE 7-BIT CHARACTER, NO PARITY, 1 STOP BIT

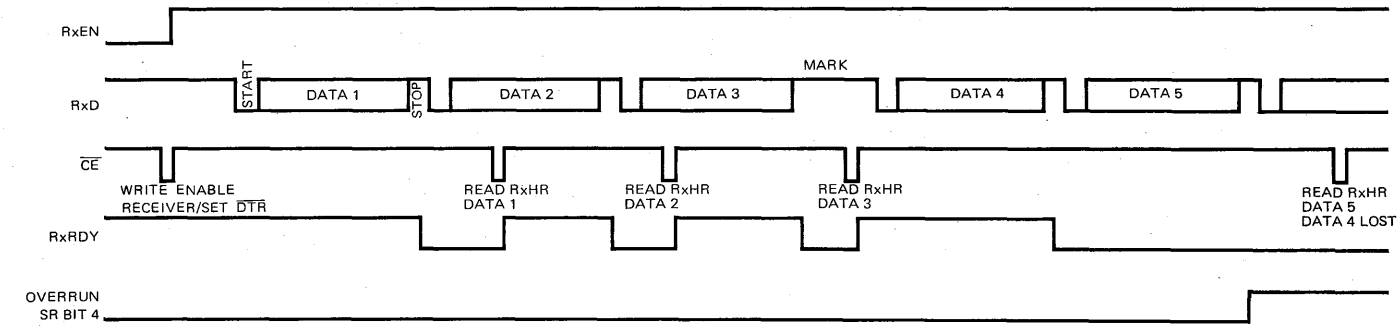
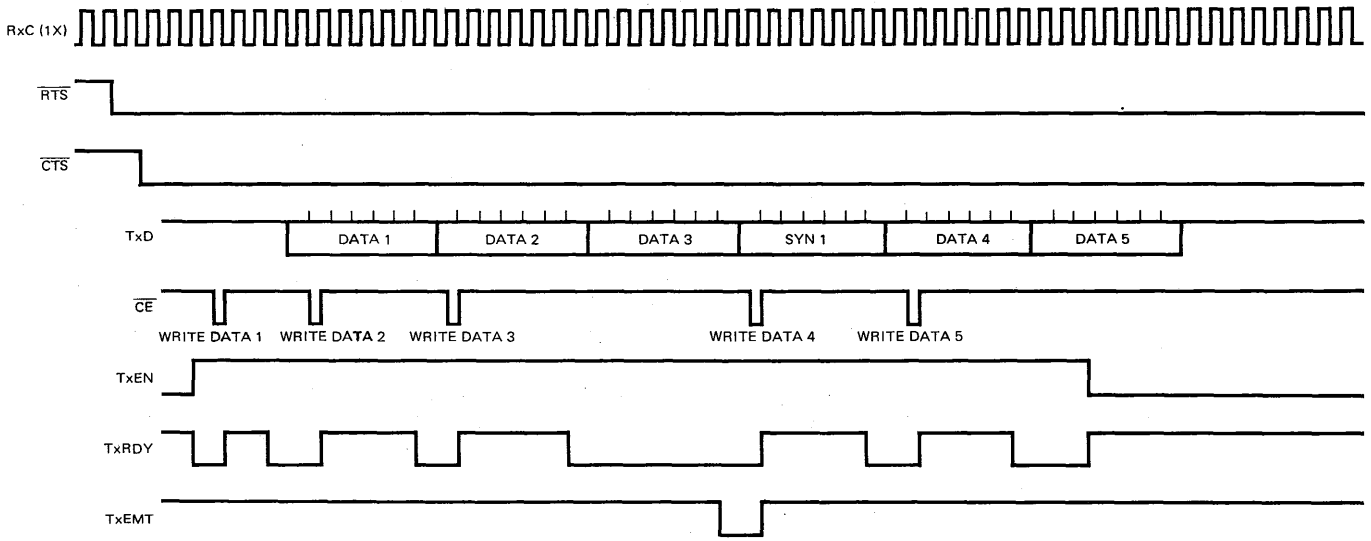


Figure 1. Receiver Operation Timing Diagram



ASYNCHRONOUS MODE 7-BIT CHARACTER, NO PARITY, 1 STOP BIT

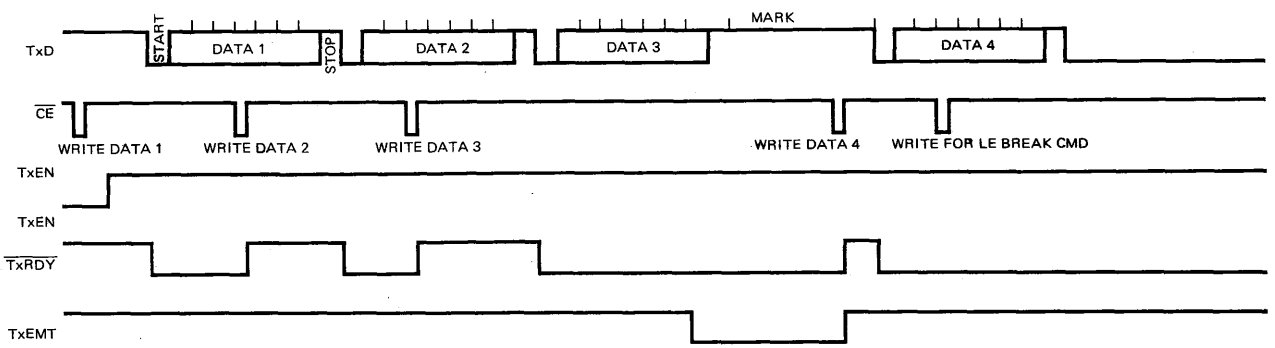


Figure 2. Transmitter Operation Timing Diagram

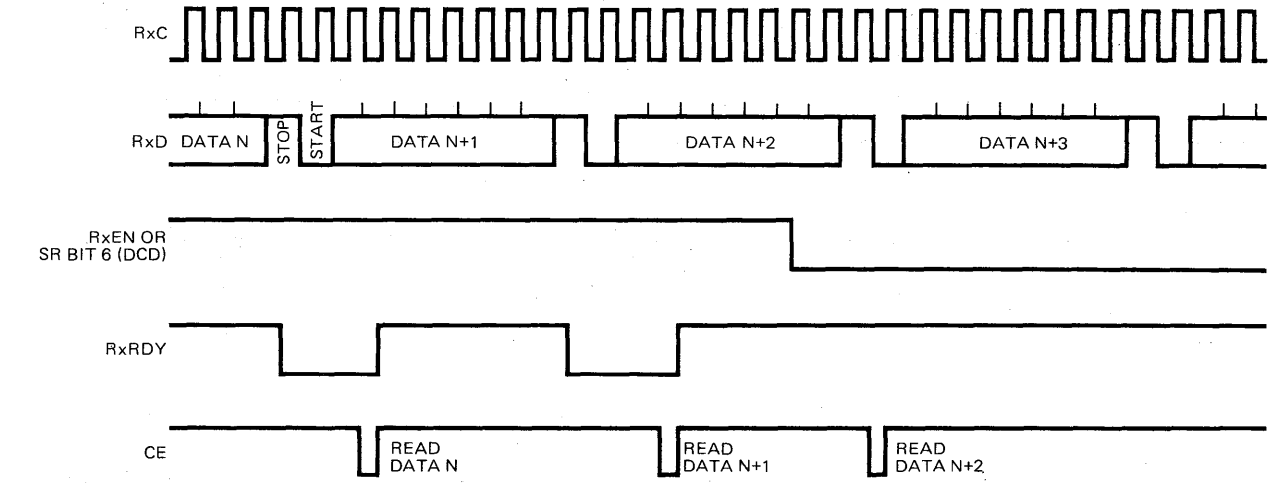


Figure 3. Asynchronous Receiver Operation with Loss of $\overline{DCD}$ or Disabling RxEN

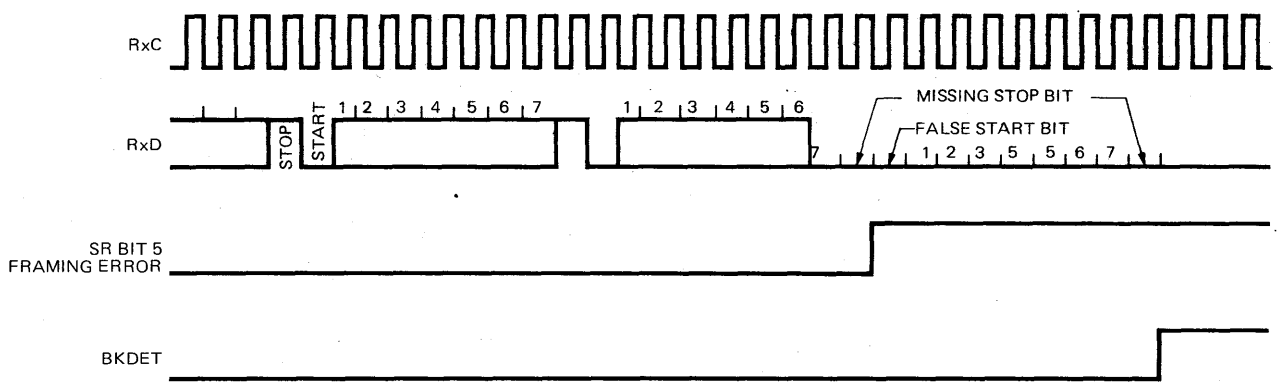


Figure 3. Framing Error and Break Detection Timing

Table 2. Baud Rate Generator Characteristics

2661-1 (BRCLK = 4.9152 MHz)

MR 2				Baud Rate	Actual Frequency 16X Clock (KHz)	Percent Error	Divisor
3	2	1	0				
0	0	0	0	50	0.8	–	6144
0	0	0	1	75	1.2	–	4096
0	0	1	0	110	1.7598	–0.01	2793
0	0	1	1	134.5	2.152	–	2284
0	1	0	0	150	2.4	–	2048
0	1	0	1	200	3.2	–	1536
0	1	1	0	300	4.8	–	1024
0	1	1	1	600	9.6	–	512
1	0	0	0	1050	16.8329	0.196	292
1	0	0	1	1200	19.2	–	256
1	0	1	0	1800	28.7438	–0.19	171
1	0	1	1	2000	31.9168	–0.26	154
1	1	0	0	2400	38.4	–	128
1	1	0	1	4800	76.8	–	64
1	1	1	0	9600	153.6	–	32
1	1	1	1	19200	307.2	–	16

2661-2 (BRCLK = 4.9152 MHz)

MR 2				Baud Rate	Actual Frequency 16X Clock (KHz)	Percent Error	Divisor
3	2	1	0				
0	0	0	0	45.5	0.7279	0.005	6752
0	0	0	1	50	0.8	–	6144
0	0	1	0	75	1.2	–	4096
0	0	1	1	110	1.7598	–0.01	2793
0	1	0	0	134.5	2.152	–	2284
0	1	0	1	150	2.4	–	2048
0	1	1	0	300	4.8	–	1024
0	1	1	1	600	9.6	–	512
1	0	0	0	1200	19.2	–	256
1	0	0	1	1800	28.7438	–0.19	171
1	0	1	0	2000	31.9168	–0.26	154
1	0	1	1	2400	38.4	–	128
1	1	0	0	4800	76.8	–	64
1	1	0	1	9600	153.6	–	32
1	1	1	0	19200	307.2	–	16
1	1	1	1	38400	614.4	–	8

2661-3 (BRCLK = 5.0688 MHz)

MR 2				Baud Rate	Actual Frequency 16X Clock (KHz)	Percent Error	Divisor
3	2	1	0				
0	0	0	0	50	0.8	–	6336
0	0	0	1	75	1.2	–	4224
0	0	1	0	110	1.76	–	2880
0	0	1	1	134.5	2.1523	0.016	2355
0	1	0	0	150	2.4	–	2112
0	1	0	1	300	4.8	–	1056
0	1	1	0	600	9.6	–	528
0	1	1	1	1200	19.2	–	264
1	0	0	0	1800	28.8	–	176
1	0	0	1	2000	32.081	0.253	158
1	0	1	0	2400	38.4	–	132
1	0	1	1	3600	57.6	–	88
1	1	0	0	4800	76.8	–	66
1	1	0	1	7200	115.2	–	44
1	1	1	0	9600	153.6	–	33
1	1	1	1	19200	316.8	3.126	16

Note: 16X CLK is used in asynchronous mode. In synchronous mode, clock multiplier is 1X and BRG can be used only for T x C

Signal Descriptions

CPU Interface

Reset (Reset)
A high on this input performs a master reset on the UM2661. This signal asynchronously terminates any device activity and clears the mode, command and status registers. The device assumes the idle state and remains there until initialized with the appropriate control words.

A_0, A_1 (Address 0, 1)
Address lines used to select the internal registers.

$\overline{R}$/W (Read/Write)
The direction of data transfers between the EPCI and the CPU is controlled by the R/W input. When CE and $\overline{R}$/W are both low the contents of the selected registers will be transferred to the data bus. With CE low and $\overline{R}$/W high a write to the selected register is performed.

$\overline{CE}$ (Chip Enable)
When low, the selected register will be accessed. When high the D_0-D_7 lines will be placed in the high impedance state.

DB_0-DB_7 (Data Bus)
An 8-bit three-state positive true data bus used to transfer commands, data and status between the EPCI and the CPU.

$\overline{TxRDY}$ (Transmitter Ready)
This output is the complement of status register bit SR0. When low, it indicates that the transmit data holding register (TxHR) is ready to accept a data character from the CPU. It goes high when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open drain output which can be "wire-ORed" to the CPU interrupt.

$\overline{RxRDY}$ (Receiver Ready)
This output is the complement of status register bit SR1. When low, it indicates that the receive data holding register (RxHR) has a character ready for input to the CPU. It goes high when the RxHR is read by the CPU and also when the receiver is disabled. It is an open drain output which can be "wire-ORed" to the CPU interrupt line.

$\overline{TxEMT/DSCHG}$
This output is the complement of status register bit SR2. When low, it indicates that the transmitter has completed serialization of the last character loaded by the CPU, or that a change of state of the DSR or DCD inputs has occurred. This output goes high when the status register is read by the CPU if the TxEMT condition does not exist. Otherwise, the TxHR must be loaded by the CPU for this line to go high. It is an open drain output which can be "wire OR-ed" to the CPU interrupt line.

Transmitter/Receiver Signals

BRCLK (Baud Rate Clock)
Clock input to the internal baud rate generator. This is not required when external receiver and transmitter clocks are used.

$\overline{RxC}$/BKDET (Receiver Clock, Break Detect)
When the EPCI is programmed for External Receiver Clock, this pin will act as an input and control the rate at which a character is received. The frequency is programmed in Mode Register 1 and may be 1X, 16X or 64X the baud rate. Data are sampled on the rising edge. If internal Receiver Clock is programmed this pin will provide an output, either a 1X/16X clock or Break Detect signal determined by programming Mode Register 2.

$\overline{TxC}$/XSYNC (Transmitter Clock/External SYNC)
When the EPCI is programmed for External Transmitter clock, this pin will act as an input and control the rate at which the character is transmitted. The frequency is programmed in Mode Register 1 and may be 1X, 16X or 64X the baud rate. Date changes on the falling edge of this clock. If the UPCI is programmed for Internal Transmitter clock, this pin can be either an output providing a 1X/16X clock or an input for External Synchronization determined by Mode Register 2 programming.

RxD (Receive Data)
RxD is the serial data input to the receiver.

TxD (Transmit Data)
TxD is the serial data output from the transmitter. When the transmitter is disabled the output will be in the high, "Mark", state.

$\overline{DSR}$ (Data Set Ready)
$\overline{DSR}$ is an input that can be used to indicate to the UPCI Data Set Ready or Ring Indicator. Its complement appears in the Status Register as bit SR7. A change of state on $\overline{DSR}$ will cause $\overline{TxEMT/DSCHG}$ to go low if either CR0 or CR2=1.

$\overline{DCD}$ (Data Carrier Detect)
The $\overline{DCD}$ input must be low for the receiver to operate. If DCD goes high while receiving, the RxC is internally inhibited. The complement of $\overline{DCD}$ appears in the Status Register as bit SR6. A change of state in $\overline{DCD}$ will cause $\overline{TxEMT/DSCHG}$ to go low if either CR0 or CR2=1.

$\overline{CTS}$ (Clear To Sned)
The $\overline{CTS}$ input must be low for the transmitter to operate. If $\overline{CTS}$ goes high while transmitting, the character currently in the Transmit Shift Register will be transmitted before termination TxD will then go to the high level (Mark).

$\overline{DTR}$ (Data Terminal Ready)
The $\overline{DTR}$ output is the complement of CR1. It is normally used to indicate Data Terminal Ready.

$\overline{RTS}$ (Reguest To Send)
The $\overline{RTS}$ output is the complement of CR5. If the Transmit Shift Register is not empty when CR5 is reset, $\overline{RTS}$ will not go high until one TxC after the last serial bit is transmitted.

Functional Description

The internal organization of the EPCI consists of six major blocks, (see Fig. 1). These are the Transmitter, Receiver, Clock Control, Operation Control, Modem Control and SYN/DLE Control. These blocks internally communicate over common data and control buses. The data bus is also linked to the CPU via a bi-directional three-state interface. Briefly, these blocks perform the following functions:

Transmitter
The Transmitter receives parallel data from the CPU and converts it to a serial bit stream, inserting Start, Stop, and Parity bits, as selected by the user, and outputs a composite serial data stream.

Receiver
The Receiver accepts serial data from the sending device, converts it to a parallel format checking for appropriate Start, Stop and Parity bits and Control Characters, as selected by the user, and sends the assembled character to the CPU.

Timing Control
The Timing Control block contains a programmable Baud Rate Generator (BRG) which is able to accept external Transmit ($\overline{TxC}$) or Receiver ($\overline{RxC}$) clocks or to divide external clock (BRCLK) for controlling data transfers. The BRCLK input allows the user to program one of 16 commonly used baud rates.

Operating Control
The Operation Control block contains four registers; Mode Registers 1 and 2, (MR1, MR2) the Command Register (CR) and Status Register (SR). These registers are used to store configuration and operation commands from the CPU. They generate the necessary internal control signals for proper device operation, and maintain status information for the CPU.

Modem Control
The modem control section provides interfacing for three input signals and three output signals used for "handshaking" and status indication between the CPU and a modem.

SYN/DLE Control
This section contains control circuitry and three 8-bit registers storing the SYN1, SYN2, and DLE character provided by the CPU. These registers are used in the synchronous mode of operation to provide the characters required for synchronization, idle fill and data transparency.

Operational Description

The EPCI's operation is determined by programming the Mode and Command Registers. Baud rate, asynchronous or synchronous communication, and SYN characters are determined before enabling the transmitter or receiver.

Asynchronous Receiver Operation
After the Mode Registers are configured the receiver is enabled when the RxEN bit in the Command Register (CR2) is set to a 1 and $\overline{DCD}$ is low. The EPCI then monitors the RxD input waiting for a high to low transition. If a transition is detected, the RxD input is again sampled one-half bit time later. If RxD is now high, a search for a valid start bit is begun again. If RxD is still low a valid start bit is assumed and the receiver continues to sample the RxD input at one bit time intervals until the correct number of data bits, parity bit and one stop bit have been assembled. The character is then transferred to the Receive Data Holding Register (RxHR); RxRDY in the status Register is set (SR1); the $\overline{RxRDY}$ output goes low. If the character length is less than 8 bits, the high order unused bits in the holding register are set to zero. The parity error, framing error, and overrun error status bits are strobed into the status register on the positive going edge of $\overline{RxC}$ corresponding to the received character boundry. See Figure 6 and 8.

If the stop bit is present, the receiver will immediately begin its search for the next start bit. If the stop bit is absent (framing error), the receiver will interpret a space bit if it persists into the next bit time interval. If a break condition is detected (RxD is low for the entire character as well as the stop bit) only one character consisting of all zeros (with the FE status bit set) will be transferred to the holding register. The RxD input must return to a high condition before a search for the next start bit begins. See Figure 9.

Pin 25 can be programmed as a Break Detect (BKDET) output by setting both bits 4 and 7 of Mode Register 2 (MR2). When these bits are set and a break is detected, the BKDET output will go high. If RxD returns high for at least one RxD time. BKDET will return low.

Synchronous Receiver Operation
When the EPCI is programmed for synchronous operation, the receiver will remain idle until the receiver enable bit

(CR2) is set. At this time the EPCI enters the hunt mode. Data are shifted into the receive data shift register (RxSR) one bit at a time. The contents of RxSR are then compared to the contents of the SYN1 register. If the two are not equal, the next bit is shifted in and the comparison is repeated. When the two registers match, the hunt mode is terminated and character assembly mode begins. If single SYN operation is programmed, the SYN DETECT status bit is set. If double SYN operation is programmed, the first character assembled after SYN1 must be SYN2 in order for the SYN DETECT bit to be set. Otherwise the EPCI returns to the hunt mode. (Note that the sequence SYN1-SYN1-SYN2 will not achieve synchronization). See Figure 6.

When synchronization has been achieved, the EPCI continues to assemble characters and transfer them to the holding register, setting the $\overline{\text{RxRDY}}$ status bit and asserting the $\overline{\text{RxRDY}}$ output each time a character is transferred. The PE and OE status bits are set as appropriate. Further receipt of the appropriate SYN sequence sets the SYN DETECT status bit. If the SYN stripping mode is commanded, SYN characters are not transferred to the holding register. Note: the SYN characters used to establish initial synchronization are not transferred to the holding register in any case.

By setting MR24 (MR2 bit 4) and MR27=1 pin 9 ($\overline{\text{RxC}}$/SYNC) will be programmed as an external jam synchronization input. When XSYNC is selected internal SYN1, SYN1-SYN2 and DLE-SYN1 detection is disabled. Each positive going signal on XSYNC will cause the receiver to establish synchronization on the rising edge of the next RxC pulse. Character assembly will start with the RxD input at this edge. XSYNC must be lowered prior to the next rising edge of RxC. This external synchronization will cause the SYN DETECT status bit to be set until the status register is read. Refer to XSYNC timing diagram.

Asynchronous Transmitter Operation

When the EPCI is programmed to transmit the transmitter will remain idle until $\overline{\text{CTS}}$ is low and the TxEN bit (CR0) is set. The EPCI will respond by setting status register (SR) bit 0 and asserting the $\overline{\text{TxRDY}}$ output. When the CPU writes a character into the transmit data holding register (TxHR), SR0 is reset and $\overline{\text{TxRDY}}$ returns high. The character is then transferred to the transmit shift register (TxSR) when it is idle or has completed transmission of the previous character. SR0 is again set, and $\overline{\text{TxRDY}}$ goes low. See Figure 7.

In the asynchronous mode, the transmitter automatically sends a start bit followed by the programmed number of data bits, the least significant bit being sent first. It then appends an optional odd or even parity bit and the programmed number of stop bits. If, following transmission of the data bits, a new character is not available in the transmit holding register, the TxD output remains in the marking (high) condition and the TxEMT/DSCHG output and its corresponding status bit are asserted. Transmission resumes when the CPU loads a new character into the holding register. The transmitter can be forced to output a continuous low (BREAK) condition by setting CR3.

Synchronous Transmitter Operation

When the ECPI is initially programmed for synchronous transmission it will remain in the idle state (RxD high) until TxEN is set. At this point TxD remains high, $\overline{\text{TxRDY}}$ will go low and both will stay in this state until the first character (usually a SYN character) is written into the TxHR. This starts transmission, with $\overline{\text{TxRDY}}$ going low each time a character is shifted from the TxHR to the TxSR. If $\overline{\text{TxRDY}}$ is not serviced before the previous character is shifted out of the TxSR, the $\overline{\text{TxEMT}}$ output will go low and the EPCI will automatically fill the pending gap with SYN1, SYN1, SYN2 doublets, or DLE-SYN1 doublets, depending on the state of MR6 and MR17. Transmission will be continuous until TxFN is reset to 0. See Figure 7.

If the send DLE bit (CR3) is set, the DLE character is automatically transmitted prior to the transmission of any character stored in the TxHR. Since this is a one time command, CR3 does not have to be reset.

EPCI Programming

Before data communications can be started the EPCI must be programmed by writing to its mode and command registers. Additionally, if synchronous communication has been selected the appropriate SYN1, SYN2 and DLE registers must be loaded Reference the Register Addressing Table and Initialization Flow Chart for address requirements and programming procedure.

The Register Addressing table shows MR1 and MR2 at the same address. The EPCI has an internal pointer that initially direat that first read or write to MR1, then on the next access at the same address the pointer directs the operation to MR2. A similar sequence occurs for the SYN and DLE registers; first SYN1 then SYN2 then DLE. If more than the required number of accesses are made the internal pointer resets to the first register. The pointer is also reset to MR1 and SYN1 by a RESET input or a read of the Command Register, but unaffected by any other read or write operation.

Register Formats

The register formats are summarized in Figures 2 through 5 MR1 and MR2 define the general operating characteristics. The Command Register controls the basic operation defined by MR1 and MR2. The Status Register indicates the EPCI operating status and the condition of external

inputs. These registers are cleared by a RESET input (SR6 and SR7 excepted).

Mode Register 1 (MR1)

MR11 and MR10 select the communication mode and baud rate multiplier. Note: the multiplier in asynchronous mode applies only if the external input option is selected by MR24 and RM25.

MR13 and MR12 select Character length. Character length does not include the parity bit, when selected, and does not include the start and stop bits in asynchronous operation.

MR14, when set, selects parity. A parity bit will be transmitted with each character, and a parity check will be performed on each character received.

MR15 selects either odd or even parity.

In the asynchronous mode MR16 and MR17 select the number of stop bits; 1, 15 or 2. If 1X baud rate is programmed 1.5 stop bits defaults to 1 on transmit.

In the synchronous mode MR17 controls the number of SYN characters used to establish synchronization, and the number of fill characters to be transmitted when $\overline{TxRDY}$ and $\overline{TxEMT}$ are 0.

MR16 controls selection of the transparent mode. When MR16 is set (transparent selected) DLE-SYN1 is used for character fill and SYN detect (SR 5), but the normal synchronization sequence is used to establish character sync. When transmitting in the synchronous transparent mode, a DLE character in the TxHR will cause a second DLE character to be transmitted. Note: if the send DLE command (CR3) is active when a DLE character is in the TxHR only one additional DLE will be transmitted.

The bits in the mode register affecting character assembly and disassembly (MR12–MR16) can be changed dynamically (during active receive/transmit operation). The character mode register affects both the transmitter and receiver; therefore in synchronous mode, changes should be made only in half duplex mode (RxEN=1 or TxEN=1, but not both simultaneously=1). In asynchronous mode, character changes should be made when RxEN and TxEN=0 or when TxEN=1 and the transmitter is marking in half duplex mode (RxEN=0).

To effect assembly/disassembly of the next received/transmitted character, MR12--15 must be changed within n bit times of the active going state of $\overline{RxDRY/TxRDY}$. Transparent and non-transparent mode changes (MR16) must occur within n-1 bit times of the character to be affected when the receiver or transmitter is active. (n = smaller of the new and old character lengths.)

Mode Register 2 (MR2)

MR20 through MR23 select the internal Baud Rate Generator (BRG). There are sixteen selectable rates for each version as outlined in Table 1.

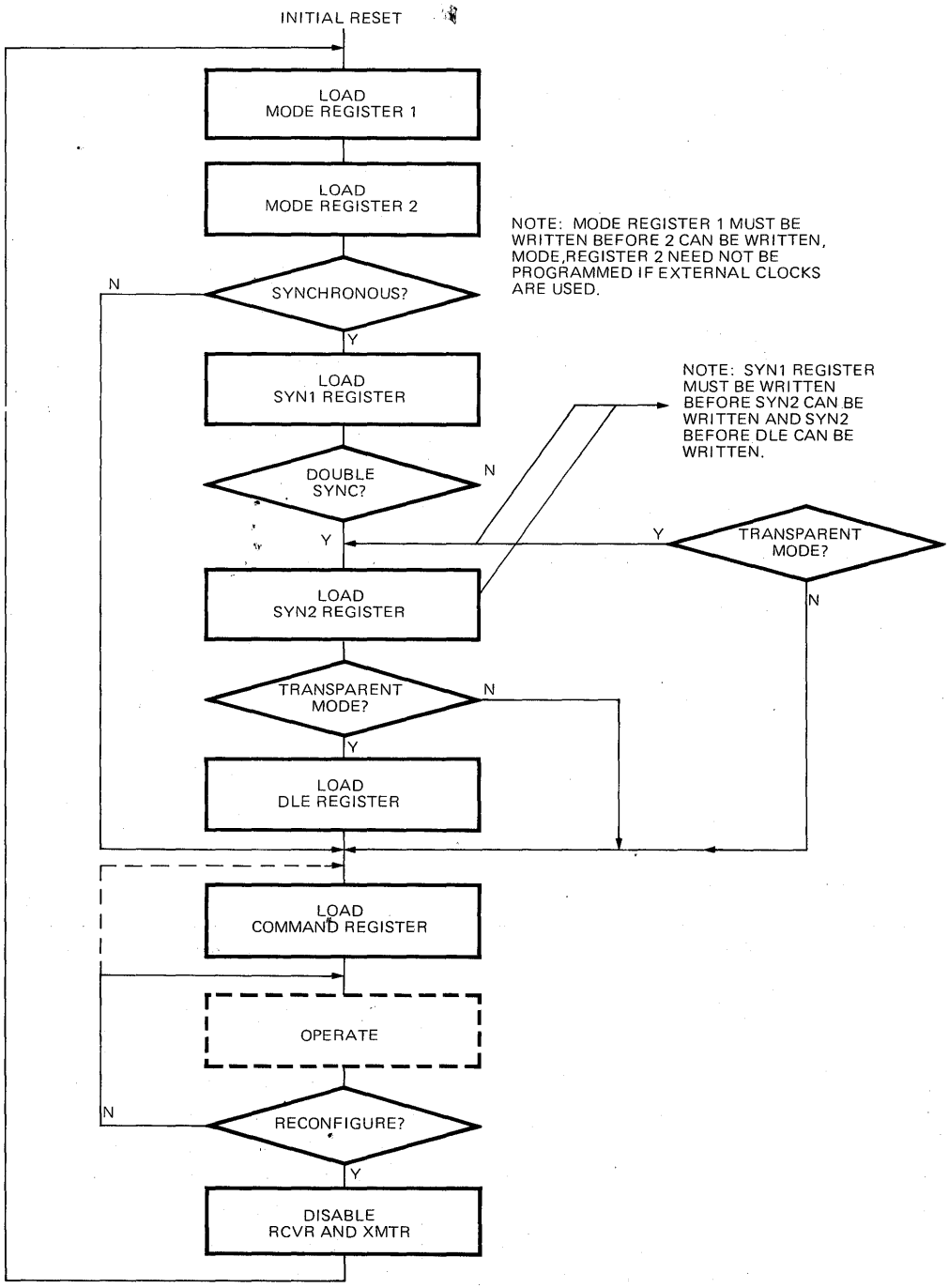
MR24 through MR27 define the receive and transmit clock source and the function of pins 9 and 25. Reference Figure 3.

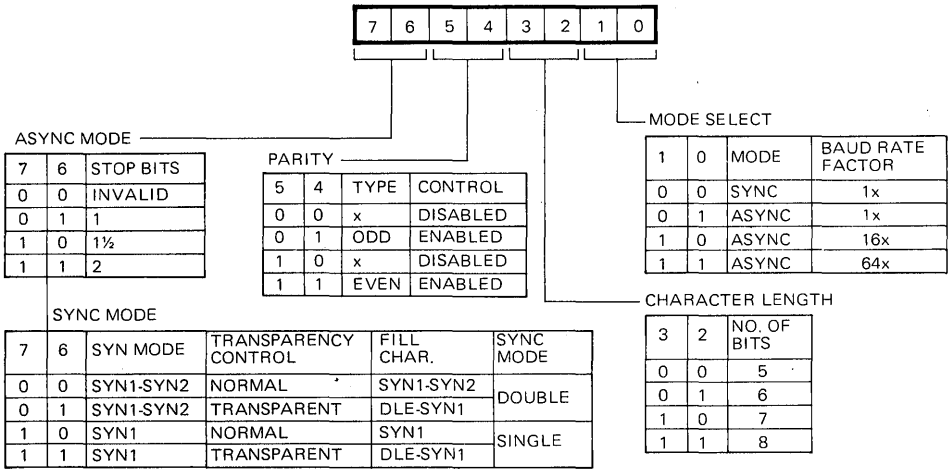
Table 3. UM2661 Register Addressing

CE	A_1	A_0	$\overline{R}/W$	Functions
1	X	X	X	Three-state Data Bus
0	0	0	0	Read Receive Holding Register (RxHR)
0	0	0	1	Write Transmit Holding Register (TxHR)
0	0	1	0	Read Status Register (SR)
0	0	1	1	Write SYN1/SYN2/DLE Registers
0	1	0	0	Read Mode Registers (MR1, MR1/MR2)
0	1	0	1	Write Mode Registers (MR1, MR1/MR2)
0	1	1	0	Read Command Register
0	1	1	1	Write Command Register

Peripheral IC

EPCI Initialization Flow Chart





7	6	STOP BITS
0	0	INVALID
0	1	1
1	0	1½
1	1	2

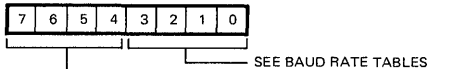
5	4	TYPE	CONTROL
0	0	x	DISABLED
0	1	ODD	ENABLED
1	0	x	DISABLED
1	1	EVEN	ENABLED

1	0	MODE	BAUD RATE FACTOR
0	0	SYNC	1x
0	1	ASYNC	1x
1	0	ASYNC	16x
1	1	ASYNC	64x

3	2	NO. OF BITS
0	0	5
0	1	6
1	0	7
1	1	8

7	6	SYN MODE	TRANSPARENCY CONTROL	FILL CHAR.	SYNC MODE
0	0	SYN1-SYN2	NORMAL	SYN1-SYN2	DOUBLE
0	1	SYN1-SYN2	TRANSPARENT	DLE-SYN1	
1	0	SYN1	NORMAL	SYN1	SINGLE
1	1	SYN1	TRANSPARENT	DLE-SYN1	

Figure 4. Mode Register 1



7	6	5	4	TxC	RxC	PIN9	PIN25	MODE
0	0	0	0	E	E	TxC	RxC	SYNC/ASYNC
0	0	0	1	E	I	TxC	1x	SYNC/ASYNC
0	0	1	0	I	E	1x	RxC	SYNC/ASYNC
0	0	1	1	I	I	1x	1x	SYNC/ASYNC
0	1	0	0	E	E	TxC	RxC	SYNC/ASYNC
0	1	0	1	E	I	TxC	16x	SYNC/ASYNC
0	1	1	0	I	E	16x	RxC	SYNC/ASYNC
0	1	1	1	I	I	16x	16x	SYNC/ASYNC
1	0	0	0	I	E	XSYNC	RxC	SYNC
1	0	0	1	I	I	TxC	BKDET	ASYNC
1	0	1	0	I	E	XSYNC	RxC	SYNC
1	0	1	1	I	I	1x	BKDET	ASYNC
1	1	0	0	I	E	XSYN	RxC	SYNC
1	1	0	1	I	I	TxC	BKDET	ASYNC
1	1	1	0	I	E	XSYNC	RxC	SYNC
1	1	1	1	I	I	16x	BKDET	ASYNC

Command Register (CR)

CR0 (TxEN) will enable or disable the transmitter. When TxEN=0, TxD, $\overline{\text{TxRDY}}$ and $\overline{\text{TxEMT}}$ are all high, the transmitter is disabled. When TxEN goes active, $\overline{\text{TxRDY}}$ will go low requesting the first character to be written to the TxHR, and the TxD output will be enabled to transmit. When TxEN goes inactive, the UPCI will complete transmission of any character still in the TxSR. TxD will then go to the marking state and $\overline{\text{TxRDY}}$ and $\overline{\text{TxEMT}}$ will go high. Refer to Transmit timing diagram.

CR1 controls the $\overline{\text{DTR}}$ output. The $\overline{\text{DTR}}$ output is a logical complement of CR1.

CR2 (RxEN) will enable or diable the receiver. When RxEN 0, the receiver is in an idle mode with $\overline{\text{RxRDY}}$ high. A 0 to 1 transition of RxEN will initiate a start bit search in asynchronous mode or initiate the hunt mode in synchronous transmission. A 1 to 0 transition of RxEN immediately terminates receiver operation.

In the asynchronous mode setting CR3 will force the TxD output low (break condition) at the end of the current transmitted character. TxD will then remain low until CR3 is cleared; at that time TxD will go high for a minimum 1 bit time before resuming normal transmission.

In the synchronous mode setting CR3 will force the transmission of the DLE character prior to sending the character in the TxHR. Because this is a one-time command, bit 3 will automatically reset.

CR5 controls the state of the $\overline{\text{RTS}}$ output. When CR5=1, $\overline{\text{RTS}}$ will go low and the transmit logic will be enabled. A 1 to 0 transition of CR5 will cause $\overline{\text{RTS}}$ to go high one TxC time after the last serial bit is transmitted, (if the TxSR was not already empty).

CR7 and CR6 provide four alternate modes of operation in both synchronous and asynchronous operation. When both bits are 0 normal operation is selected.

In the asynchronous mode, when only CR6 is set automatic echo mode is selected Clocked, regenerated received data are automatically directed to the TxD line while normal receiver operation continues. The receiver must be enabled (CR2=1), but the transmitter need not be enabled. CPU to receiver communications continues normally, but the CPU to transmitter link is disabled. Only the first tharacter of a break condition is echoed. The TxD output will go high until the next valid start is detected. The following conditions are true while in automatic echo mode:

Peripheral IC

1. Data assembled by the receiver are automatically placed in the transmit holding register and re-transmitted by the transmitter on the TxD output.
2. Transmit clock = receive clock.
3. $\overline{\text{TxRDY}}$ output = 1.
4. The $\overline{\text{TxEMT/DSCHG}}$ pin will reflect only the data set change condition.
5. The TxEN command (CR0) is ignored.

In the synchronous mode, when only CR6 is set automatic SYN/DLE stripping is performed. The state of MR17 and MR16 controls which characters are stripped. Reference Figure 6 for a detailed example of the characters stripped.

Note: automatic stripping does not affect setting of the SYN and DLE detect status bits.

Two diagnostic modes are achievable in both synchronous and asynchronous operation; local loop back with CR7=1 and CR6=0, and remote loopback with both bits=1.

Local Loop Back

1. The transmitter output is connected to the receiver input.
2. $\overline{\text{DTR}}$ is connected to $\overline{\text{DCD}}$ and $\overline{\text{RTS}}$ is connected to $\overline{\text{CTS}}$.
3. Transmit clock is connected to the receive clock.
4. The $\overline{\text{DTR}}$, $\overline{\text{RTS}}$ and $\overline{\text{TxD}}$ outputs are held high.
5. The $\overline{\text{CTS}}$, $\overline{\text{DCD}}$, $\overline{\text{DSR}}$ and $\overline{\text{RxD}}$ inputs are ignored.

Note: CR bits 0, 1 and 5 must be set, CR2 is a don't care.

Remote Loop Back

1. Data assembled by the receiver are automatically placed in the transmit holding register and re-transmitted by the transmitter on the TxD output.
2. Receive clock is connected to the transmit clock.
3. No data are sent to the local CPU, but the error status conditions (PE, OE, FE) are set.
4. The $\overline{\text{RxRDY}}$, $\overline{\text{TxRDY}}$, and $\overline{\text{TxEMT/DSCHG}}$ outputs are held high.
5. CR1 (TxEN) is ignored.
6. All other signals operate normally.

Status Register

SRD is the transmitter ready ($\overline{\text{TxRDY}}$) status, it is the logical complement of the $\overline{\text{TxRDY}}$ output. This bit indicates the state of the TxHR when the transmitter is enabled (TxEN=1). A 0 indicates TxHR is full, a 1 indicates TxHR is empty and requires servicing by the CPU. This bit is cleared by writing to TxHR or by disabling the transmitter (TxEN=0). Note: SRO is not set in either the auto echo or remote loop back modes.

SR1 is the receiver ready (RxRDY) status. It is the logical complement of the $\overline{\text{RxRDY}}$ output. This bit indicates the state of the RxHR when the receiver is enabled (RxEN=1). A 0 indicates the RxHR is empty, a 1 indicates the RxHR is full and requires servicing by the CPU. This bit is cleared by writing to the TxHR or by disabling the receiver. (RxEN=0).

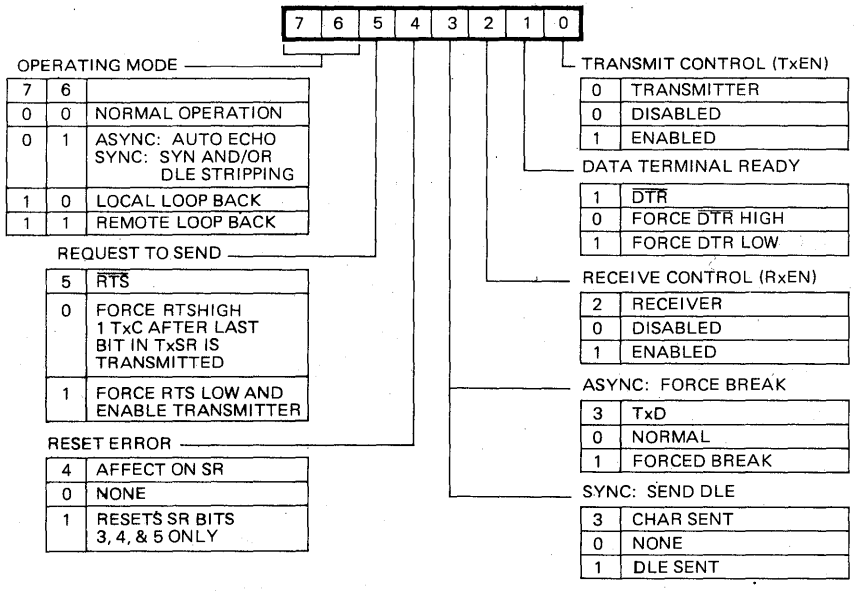


Figure 5. Command Register

SR2 indicates a change of state of either $\overline{DSR}$ or $\overline{DCD}$ or that the TxSR is empty. This bit is the logical complement of the $\overline{TxEMT/DSCHG}$ output. A read of the status register will clear bit 2 if a state change on DSR or $\overline{DCD}$ has occurred. If a second successive read of the status register indicates bit 2=0, then $\overline{DCD}$ or $\overline{DSR}$ changed. If bith 2 is still set, then the TxSR is empty. Because the transmitter does not start until the first character has been written to the TxHR, $\overline{TxEMT}$ status will not be reflected until transmission of the first character is complete, $\overline{TxEMT}$ status is cleared by writing to the TxHR or disabling the transmitter. Note: $\overline{TxEMT}$ status will be set in synchronous mode even though "fill" characters are being transmitted.

SR3 when set reflects a parity error when parity checking is enabled in both the synchronous and asynchronous modes. In the synchronous transparent mode, (MR16=1) and the parity enable bit (MR14) is 0, SR3 will then indicate DLE detect when set. This indicates that a character matching DLE register was received and the present character is neither SYN1 nor DLE. This bit is cleared when the next character following the above sequence is loaded into the RxHR, when the receiver is disabled or by a reset error command.

SR4 indicates an overrun error when set. An overrun condition exists when the CPU does not read the RxHR before the next received character is transferred to it. (The previous character is lost.) SR4 is cleared by the reset error command and when the receiver is disabled.

In the asynchronous mode SR5 indicates that the received character was not framed by a stop bit. If the RxHR is all 0's when bit 5 is set, a break condition was present. In synchronous non-transparent mode, it indicates receipt of the SYN1 character in single SYN mode or the SYN1-SYN2 pair in double SYN mode. In synchronous transparent mode this bit is set upon detection of the initial synchronizing characters (SYN1 or SYN1-SYN2) and after synchronization has been achieved, when a DLE-SYN1 pair is received. The bit is reset when the receiver is disabled, when the reset error command is given in asynchronous mode, and when the status register is read by the CPU in the synchronous mode.

SR6 and SR7 reflect the condition of the $\overline{DCD}$ and $\overline{DSR}$ inputs respectively. Their state is the logical complement of their respective inputs.

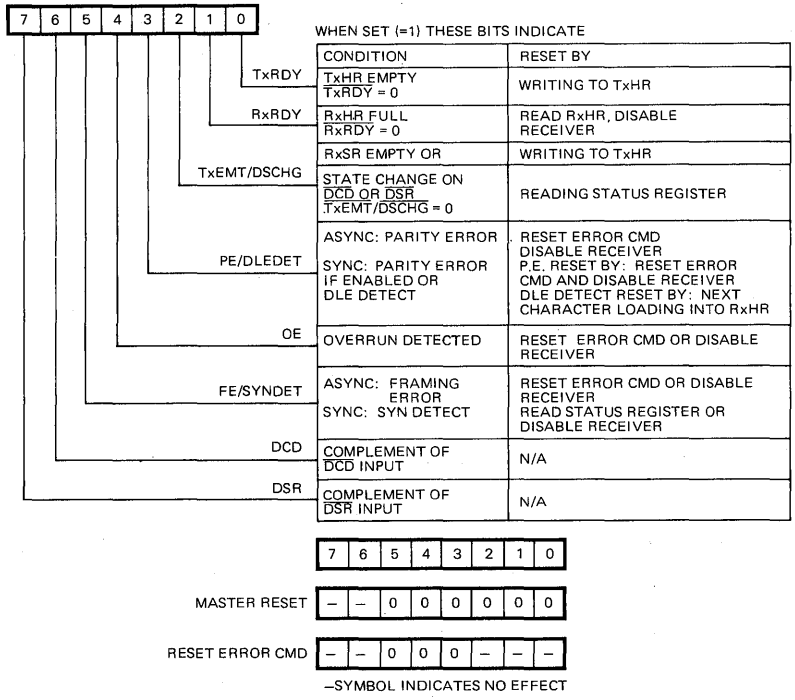


Figure 6. Status Register

Ordering Information

Part Number	BRCLK	Baud Rate
UM2661-1	4.9152 MHz	50 ~19200
UM2661-2	4.9152 MHz	45.5~38400
UM2661-3	5.0688 MHz	50 ~19200

Peripheral IC

UM2681 SERIES

Dual Asynchronous Receiver/ Transmitter (DUART)

Features

- Dual full-duplex asynchronous receiver/transmitter
- Ouadruple buffered receiver data registers
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16 bit increments
- Programmable baud rate for each receiver and transmiter selectable from:
  - 18 fixed rates: 50 to 38.4K baud
  - One user defined rate derived from programmable timer/counter
  - External 1x or 16x clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
- Multi-function programmable 16-bit counter/timer
- Multi-function 7-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate wire-OR'able interrupt outputs
- Maximum data transfer: 1X—1MB/sec, 16X—125KB/sec
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- TTL compatible
- Single +5V power supply

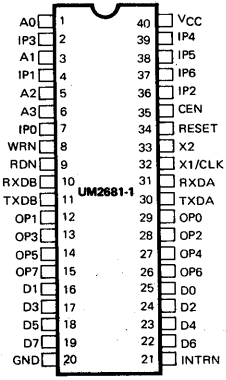
General Description

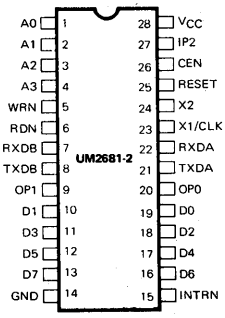
The UM2681 Dual Universal Asynchronous Receiver/ Transmitter (DUART) is a single chip NMOS-LSI communications device that provides two independent full-duplex asynchronous receiver/transmitter channels in a single package. It interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

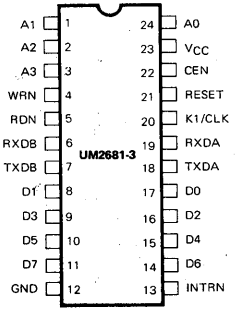
The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is quadruply buffered to minimize the potential of receiver overrun or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the buffer of the receiving device is full.

Pin Configuration







Also provided on the UM2681 are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

The UM2681 is available in three package versions to satisfy various system requirements.

Absolute Maximum Ratings*

Operating ambient temperature . . . . . 0° to +70°C

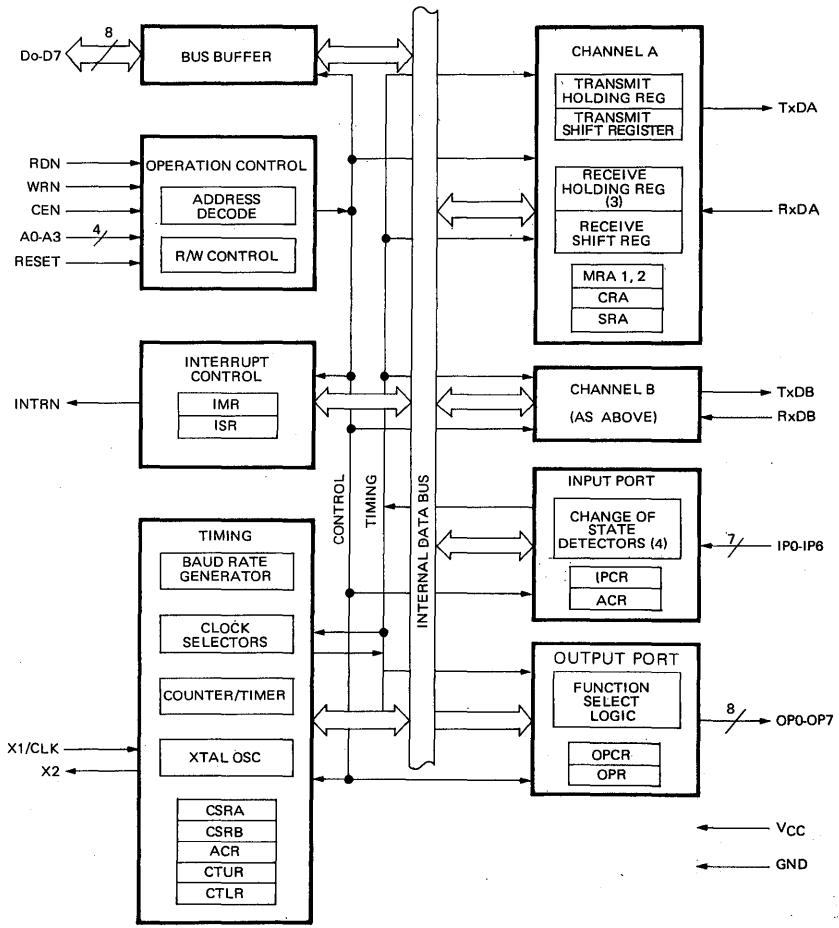
Storage temperature . . . . . –65° to +150°C

All voltages with respect to ground . . . . –0.5V to +6.0V

*Comments

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



D.C. Electrical Characteristics

(T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%)

Parameter		Test Conditions	Limits			Units
			Min.	Typ.	Max.	
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage (except X1/CLK)		2.0			V
V_{IH}	Input high voltage (X1/CLK)		4.0			V
V_{OL}	Output low voltage	I_{OL} = 2.4 mA			0.4	V
V_{OH}	Output high voltage (except o.c., outputs)	I_{OH} = −400 μA	2.4			V
I_{IL}	Input leakage current	V_{IN}= 0 to V_{CC}	−10		10	μA
I_{LL}	Data bus 3-state leakage current	V_O = 0 to V_{CC}	−10		10	μA
I_{OC}	Open collector output leakage current	V_O = 0 to V_{CC}	−10		10	μA
I_{CC}	Power supply current				150	mA

A.C. Electrical Characteristics

(T_A = 0°C to + 70°C, V_{CC} = 5.0V ± 5%)

Parameter		Tentative Limits			Units
		Min.	Typ.	Max.	
Reset Timing (Figure 1)					
t_{RES}	RESET pulse width	1.0			μs
Bus Timing (Figure 2)					
t_{AS}	A0-A3 setup time to RDN, WRN low	10			ns
t_{AH}	A0-A3 hold time from RDN, WRN high	0			ns
t_{CS}	CEN setup time to RDN, WRN low	0			ns
t_{CH}	CEN hold time from RDN, WRN high	0			ns
t_{RW}	WRN, RDN pulse width	225			ns
t_{DD}	Data valid after RDN low			175	ns
t_{DF}	Data bus floating after RDN high			100	ns
t_{DS}	Data setup time before WRN high	100			ns
t_{DH}	Data hold time after WRN high	20			ns
t_{RWD}	High time between READs and/or WRITEs	200			ns

Parameter		Tentative Limits			Units
		Min.	Typ.	Max.	
Port Timing (Figure 3)					
t_{PS}	Port input setup time before RDN low	0			ns
t_{PH}	Port input hold time after RDN high	0			ns
t_{PD}	Port output valid after WRN high			400	ns
Interrupt Timing (Figure 4)					
t_{IR}	INTRN (or OP3-OP7 when used as interrupts) high from:				
	Read RHR (RXRDY/FFULL interrupt)			300	ns
	Write THR (TXRDY interrupt)			300	ns
	Reset command (delta break interrupt)			300	ns
	Stop C/T command (counter interrupt)			300	ns
	Read IPCR (input port change interrupt)			300	ns
	Write IMR (clear of interrupt mask bit)			300	ns
Clock Timing (Figure 5)					
t_{CLK}	X1/CLK high or low time	100			ns
t_{CLK}	X1/CLK frequency	2.0	3.6864	4.0	MHz
t_{CTC}	CTCLK (IP2) high or low time	100			ns
f_{CTC}	CTCLK (IP2) frequency	0		4.0	MHz
t_{RX}	high or low time	220			ns
f_{RX}	RxC frequency (16X)	0		2.0	MHz
	(1X)	0		1.0	MHz
t_{TX}	TxC high or low time	220			ns
f_{TX}	TxC frequency (16X)	0		2.0	MHz
	(1X)	0		1.0	MHz
Transmitter Timing (Figure 6)					
t_{TXD}	TxD output delay from TxC low			350	ns
t_{TCS}	TxC output skew from TxD output data	0		150	ns
Receiver Timing (Figure 7)					
t_{RXS}	RxD data setup time to RxC high	240			ns
t_{RXH}	RxD data hold time from RxC high	200			ns

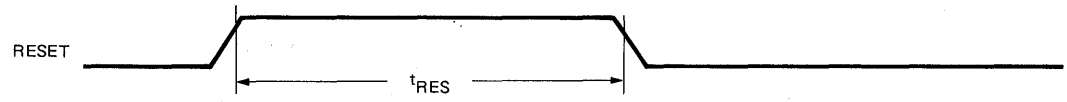


Figure 1. Reset Timing

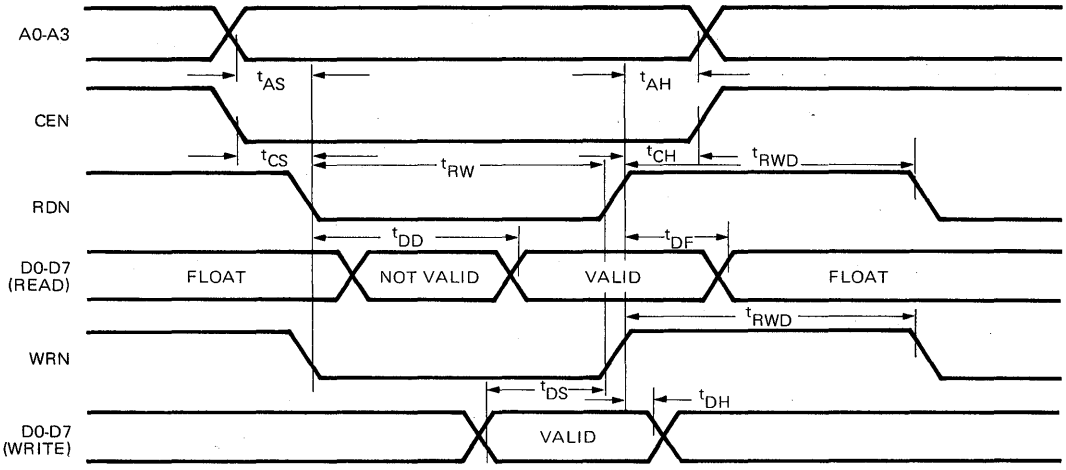


Figure 2. Bus Timing

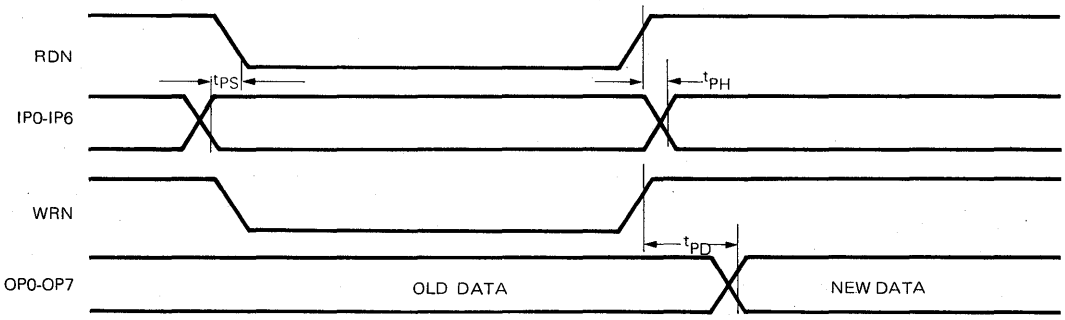


Figure 3. Port Timing

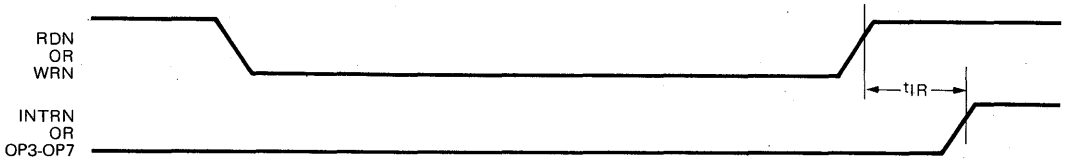


Figure 4. Interrupt Timing

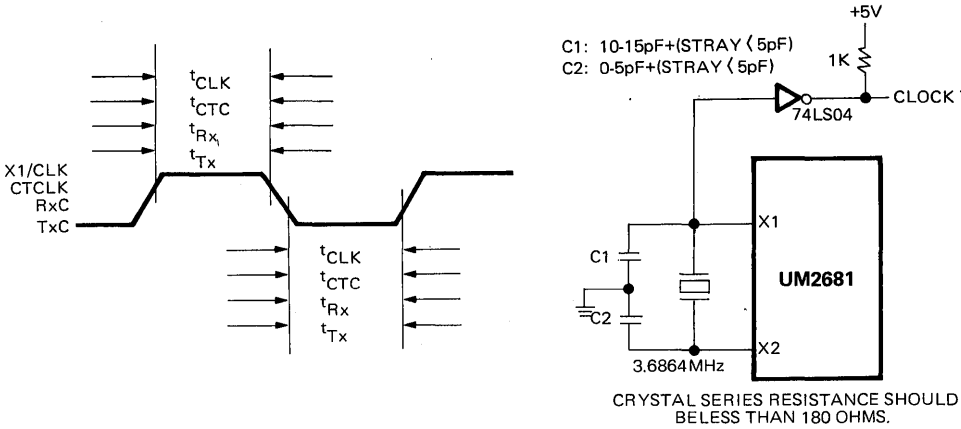


Figure 5. Clock Timing

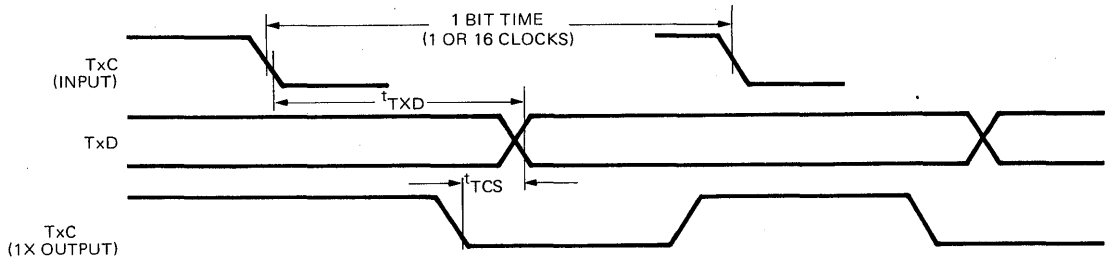


Figure 6. Transmit

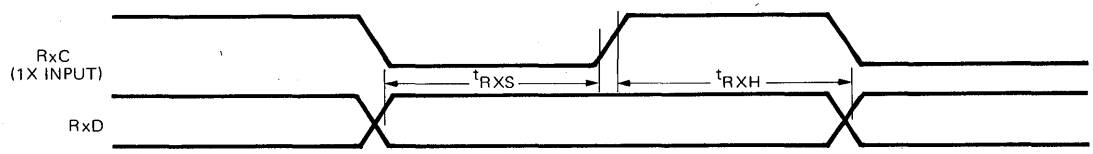
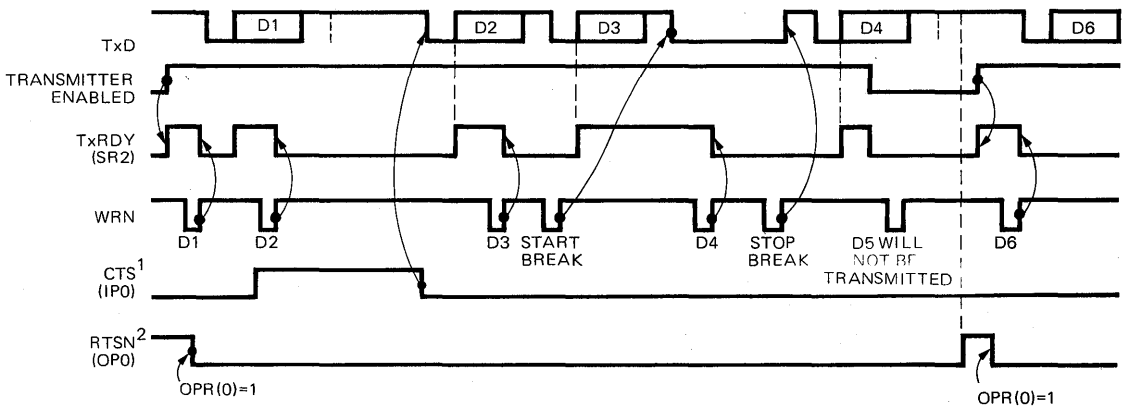


Figure 7. Receive



Notes: TIMING SHOWN FOR MR2(4) = 1
TIMING SHOWN FOR MR2(5) = 1

Figure 8. Transmitter Timing

Peripheral IC

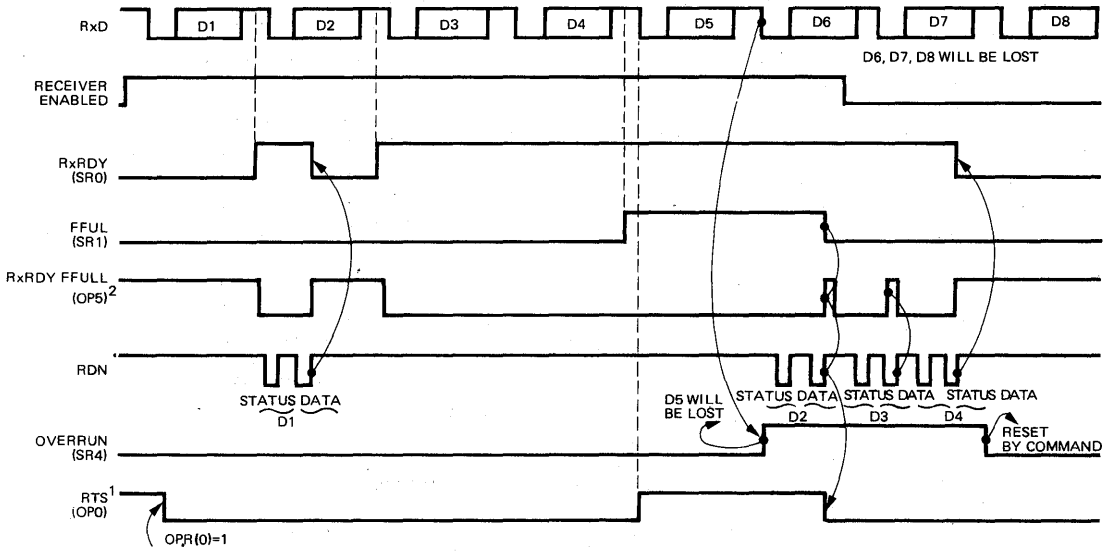


Figure 9. Receiver Timing

Notes: 1. Timing shown for MR1(7)=1.
2. Shown for OPCR(4)=1 and MR(6)=0.

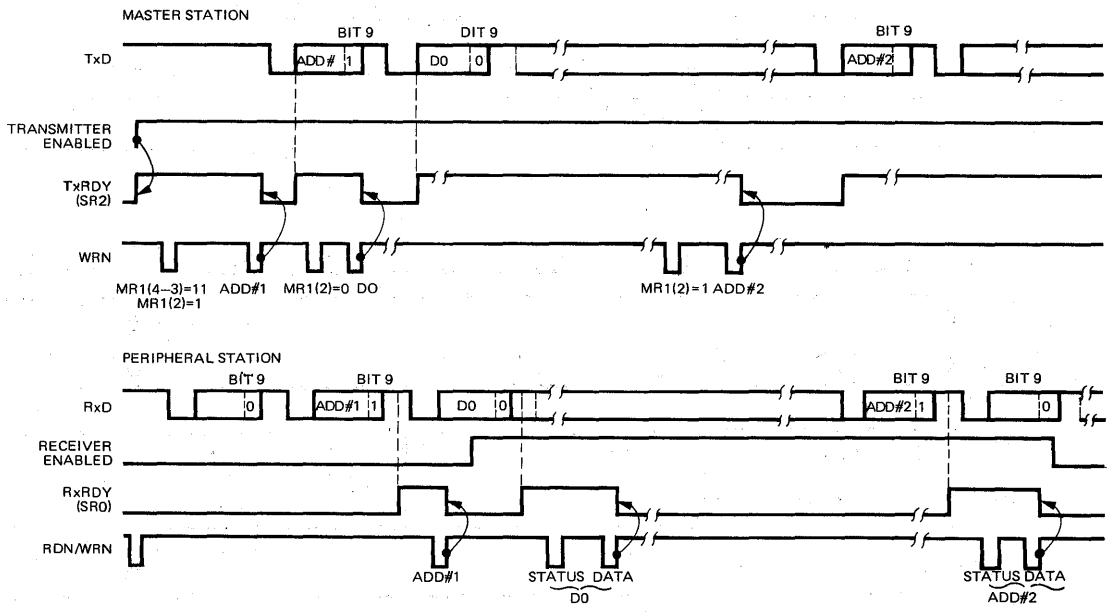


Figure 10. Wake Up Mode

Pin Description

Mnemonic	Applicable			Type	Names and Functions
	40	28	24		
D0-D7	X	X	X	I/O	**Data Bus:** Bidirectional 3-state data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	X	X	X	I	**Chip Enable:** Active low input signal. When low, data transfers between the CPU and the DUART are enabled on D0-D7 as controlled by the WRN, RND and A0-A3 inputs. When high, places the D0-D7 lines in the 3-state condition.
WRN	X	X	X	I	**Write Strobe:** When low and CEN is also low, the contents of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	X	X	X	I	**Read Strobe:** When low and CEN is also low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0-A3	X	X	X	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESET	X	X	X	I	**Reset:** A high level clears internal registers (SRA, SRB, IMB, ISR, OPR, OPCR), puts OP0-OP7 in the high state, stops the counter/timer, and puts channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (high) state.
INTRN	X	X	X	O	**Interrupt Request:** Active low, open drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	X	X	X	I	**Crystal 1:** Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 5).
X2	X	X		O	**Crystal 2: Conection** for other side of the crystal. Should be connected to ground if a crystal is not used. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 5).
RxDA	X	X	X	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. 'Mark' is high, 'space' is low.
RxDB	X	X	X	I	**Channel B Receiver Serial Data Input:** The least significant bit is received first. 'Mark' is high, 'space' is low.
TxDA	X	X	X	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is high, 'space' is low.
TxDB	X	X	X	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is high, 'space' is low.
OP0	X	X		O	**Output 0:** General purpose output, or channel A request to send (RTSAN, active low). Can be deactivated on receive or transmit.
OP1	X	X		O	**Output 1:** General purpose output, or channel B request to send (RTSBN, active low). Can be deactivated on receive or transmit.
OP2	X			O	**Output 2:** General purpose output, or channel A transmitter 1X or 16X clock output, or channel A receiver 1X clock output.

Pin Description (Continued)

Mnemonic	Applicable			Type	Names and Functions
	40	28	24		
OP3	X			O	**Output 3:** General purpose output, or open drain, active low counter/timer output, or channel B transmitter 1X clock output, or channel B receiver 1X clock output.
OP4	X			O	**Output 4:** General purpose output, or channel A open drain, active low, RxRDYA/ FFULLA output.
OP5	X			O	**Output 5:** General purpose output, or channel B open drain, active low, RxRDYB/ FFULLB output.
OP6	X			O	**Output 6:** General purpose output, or channel A open drain, active low, TxRDYA output.
OP7	X			O	**Output 7:** General purpose output, or channel B open drain, active low, TxRDYB output.
IP0	X			I	**Input 0:** General purpose input, or channel A clear to send active low input (CTSAN).
IP1	X			I	**Input 1:** General purpose input, or channel B clear to send active low input (CTSBN).
IP2	X	X		I	**Input 2:** General purpose input, or counter/time external clock input.
IP3	X			I	**Input 3:** General purpose input, or channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	X			I	**Input 4:** General purpose input, or channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	X			I	**Input 5:** General purpose input, or channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP6	X			I	**Input 6:** General purpose input or channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
V_{CC}	X	X	X	I	**Power Supply:** +5V supply input.
GND	X	X	X	I	**Ground**

Block Diagram

The 2681 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications channels A and B, input port and output port. Refer to the block diagram.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data busses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer.

Interrupt Control

A single active low interrupt output (INTRN) is provided which is activated upon the occurrence of any of eight internal events. Associated with the interrupt system are the interrupt mask register (IMR) and the interrupt status register (ISR). The IMR may be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions.

Outputs OP3-OP7 can be programmed to provide discrete interrupt outputs for the transmitters, receivers, and counter/timer.

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a 3.6864 MHz crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the baud rate generator (BRG), the counter/timer, and other internal circuits. A clock signal within the limits specified in the specifications section of this data sheet must always be supplied to the DUART.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. The clock outputs from the BRG are at 16X the actual baud rate. The counter/time can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or an external timing signal.

The counter/timer (C/T) can be programmed to use one of several timing sources as its input. The output of the C/T is available to the clock selectors and can also be programmed to be output at OP3. In the counter mode, the contents of the C/T can be read by the CPU and it can be stopped and started under program control. In the timer mode, the C/T acts as a programmable divider.

Communications Channels A and B

Each communications channel of the 2681 comprises a full duplex asynchronous receiver/transmitter (UART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter timer, or from an external input.

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU.

Input Port

The inputs to this unlatched 7-bit port can be read by the CPU by performing a read operation at address D_{16}. A high input results in a logic 1 while a low input results in a logic 0. D_7 will always be read as a logic 1. The pins of this port can also serve as auxiliary inputs to certain portions of the DUART logic.

Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1, and IP0. A high-to-low or low-to-high transition of these inputs lasting longer than 25-50μs will set the corresponding bit in the input port will change register. The bits are cleared when the register is ready by the CPU. Any change of state can also be programmed to generate an interrupt to the CPU.

Output Port

The 8-bit multi-purpose output port can be used as a general purpose output port, in which case the outputs are the complements of the output port register (OPR). OPR [n] = 1 results in OP [n] = low and viceversa. Bits of the OPR can be individually set and reset. A bit is set by performing a write operating at address E_{16} with the accompanying data specifying the bits to be set (1 = set, 0 = not change). Likewise, a bit is reset by a write at address F_{16} with the accompanying data specifying the bits to be reset (1 = reset, 0 = no change).

Outputs can be also individually assigned specific functions by appropriate programming of the channel. A mode registers (MR1A, MR2A), the channel B mode registers (MR1B, MR2B), and the output port configuration register (OPCR).

Operational Description

Transmitter

The 2681 is conditioned to transmit data when the transmitter is enabled through the command register. The 2681 indicates to the CPU that it is ready to accept a character by setting the TxRDY bit in the status register. This condition can be programmed to generate an interrupt request at OP6 or OP7 and INTRN. When a character is loaded into the transmit holding register (THR), the above conditions are negated. Data is transferred from the holding register to the transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again

which means one full character time of buffering is provided. Characters cannot be loaded into the THR while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains high and the TxEMT bit in the status register (SR) will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the THR. If the transmitter is disabled, it continues operating until the character currently begin transmitted is completely sent out. The transmitter can be forced to send a continuous low condition by issuing a send break command.

The transmitter can be reset through a software command. If it is reset, operation ceases immediately and the transmitter must be enabled through the command register before resuming operation. If CTS operation is enabled, the CTSN input must be low in order for the character to be transmitted. If it goes high in the middle of a transmission, the character in the shift register is transmitted and TxDA then remains in the marking state until CTSN goes low. The transmitter can also control the deactivation of the RTSN output. If programmed, the RTSN output will be reset one bit time after the character in the transmit shift register and transmit holding register (if any) are completely transmitted, if the transmitter has been disabled.

Receiver

The 2681 is conditioned to receive data when enabled through the command register. The receiver looks for a high to low (mark to space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16X clock for 7-1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled high, the start bit is invalid and the search for a valid start bit begins again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and the parity bit (if any) have assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the receive holding register (RHR) and the RxRDY bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at OP4 or OP5 and INTRN. If the character legnth is less than eight bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and RxD remains low for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

The parity error, framing error, overrun error and received break state (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set. If a break condition is detected (RxD is low for the entire character including the stop bit), a character consisting of all zeros will be loaded into the RHR and the received break bit in the SR is set to 1. The RxD input must return to a high condition for at least one-half bit time before a search for the next start bit begins.

The RHR consists of a first-in-first-out (FIFO) stack with a capacity of three characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FFULL status bit is set if all three stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits (see below) are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are also appended to each data character in the FIFO (overrun is not). Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis: the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore the status register should be read prior to reading the FIFO.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exits, the contents of the FIFO are not affected: the character previously in the shift register is lost and the overrun error status bit (SR[4]) will be set upon receipt of the start bit of the new (overruning) character.

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be reasserted automatically. This feature can be used to prevent an overrun, in the receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

If the receiver is disabled, the FIFO characters can be read. However, no additional characters can be received until the receiver is enabled again. If the receiver is reset, the FIFO and all of the receiver status, and the corresponding output ports and interrupt are reset. No additional characters can be received until the receiver is enabled again.

Multidrop Mode

The DUART is equipped with a wake up mode used for multidrop applications. This mode is selected by programming bits MR1A [4:3] or MR1B[4:3] to '11' for channels A and B respectively. In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, with receivers that are normally disabled, examine the received data stream and 'wakeup' the CPU (by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, an address/data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1A[2]/MR1B[2]. MR1A[2]/MR1B[2] = 0 transmits a zero in the A/D bit position, which identifies the corresponding data bits as data, while MR1A[2]/MR1B[2] = 1 transmits a one in the A/D bit position, which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits into the THR.

In this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character into the RHR FIFO if the received A/D bit is a one (address tag), but discards the received character if the received A/D bit is a zero (data tag). If enabled, all received characters are transferred to the CPU via the RHR. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SRA[5] or SRB[5]). Framing error, overrun error, and break detect operate normally whether or not the receiver is enabled.

Programming

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in Table 1.

The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems. For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped.

Mode registers 1 and 2 of each channel are accessed via independent auxiliary pointers. The pointer is set to MR1x by RESET or by issuing a 'reset pointer' command via the corresponding command register. Any read or write of the mode register while the pointer is at MR1x switches the pointer to MR2x. The pointer then remains at MR2x, so that subsequent accesses are always to MR2x unless the pointer is reset to MR1x as described above.

Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Table 2 for register bit descriptions.

MR1A—Channel A Mode Register 1

MR1A is accessed when the channel A MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRA. After reading or writing MR1A, the pointer will point to MR2A.

MR1A(7)—Channel A Receiver Request-to-Send Control — This bit controls the deactivation of the RNSAN output (OP0) by the receiver. This output is normally asserted by setting OPR[0]. MR1A[7]=1 causes RTSAN to be negated upon receipt of a valid start bit if the channel A FIFO is full. However, OPR[0] is not reset and RTSAN will be asserted again when an empty FIFO position is available. This feature can be used for flow control to prevent overrun in the receiver by using the RTSAN output signal to control the CTSN input of the transmitting device.

MR1A[6] — Channel A Receiver Interrupt Select — This bit selects either the channel A receiver ready status

(RXRDY) or the channel A FIFO full status (FFULL) to be used for CPU interrupts. It also causes the selected bit to be output on OP4 if it is programmed as an interrupt output via the OPCR.

MR1A[5] – Channel A Error Mode Select – This bit selects the operating mode of the three FIFOed status bits (FE, PE, received break) for channel A. In the 'character' mode, status is provided on a character-by-character basis: the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these bits is the accumulation (logical OR) of the status for all characters coming to the top of the FIFO since the last 'reset error' command for channel A was issued.

MR1A[4:3] – Channel A Parity Mode Select – If 'with parity' or 'force parity' is selected, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR1A[4:3] = 11 selects channel A to operate in the special multidrop mode described in the Operation section.

MR1A[2] – Channel A Parity Type Select – This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1A[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special multidrop mode it selects the polarity of the A/D bit.

MR1A[1:0] – Channel A Bits per Character Select – This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

MR2A – Channel A Mode Register 2

MR2A is accessed when the channel A MR pointer points to MR2, which occurs after any access to MR1A. Accesses to MR2A do not change the pointer.

MR2A[7:6] – Channel A Mode Select – Each channel of the DUART can operate in one of four modes. MR2A[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2A[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need

Table 1. UM2681 Register Addressing

A3	A2	A1	A0	Read (RDN=0)	Write (WRN=0)
0	0	0	0	Mode Register A (MR1A, MR2A)	Mode Register A (MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock Select Reg. A (CSRA)
0	0	1	0	* Reserved *	Command Register A (CRA)
0	0	1	1	RX Holding Register A (RHRA)	TX Holding Register A (THRA)
0	1	0	0	Input Port Change Reg. (IPCR)	Aux. Control Register (ACR)
0	1	0	1	Interrupt Status Reg. (ISR)	Interrupt Mask Reg. (IMR)
0	1	1	0	Counter/Timer Upper (CTU)	C/T Upper Register (CTUR)
0	1	1	1	Counter/Timer Lower (CTL)	C/T Lower Register (CTLR)
1	0	0	0	Mode Register B (MR1B, MR2B)	Mode Register B (MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock Select Reg. B (CSRB)
1	0	1	0	* Reserved *	Command Register B (CRB)
1	0	1	1	RX Holding Register B (RHRB)	TX Holding Register B (THRB)
1	1	0	0	* Reserved *	* Reserved *
1	1	0	1	Input Port	Output Port Conf. Reg. (OPCR)
1	1	1	0	Start Counter Command	Set Output Port Bits Command
1	1	1	1	Stop Counter Command	Reset Output Port Bits Command

Table 2. Register Bit Formats

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	RX RTS Control	**RX INT Select**	**Error Mode**	**Parity Mode**		**Parity Type**	**Bits Per Char.**	
MR1A **MR1B**	0=no 1=yes	0=RXRDY 1=FFULL	0=char 1=block	00=with parity 01=force parity 10=no parity 11=multi-drop mode		0=even 1=odd	00=5 01=6 10=7 11=8	

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	Channel Mode		**TxRTS Control**	**CTS Enable Tx**	**Stop Bit Length***			
MR2A **MR2B**	00=Normal 01=Auto echo 10=Local loop 11=Remote loop		0=no 1=yes	0=no 1=yes	0=0.563 1=0.625 2=0.688 3=0.750	4=0.813 5=0.875 6=0.938 7=1.000	8=1.563 9=1.625 A=1.688 B=1.750	C=1.813 D=1.875 E=1.938 F=2.000

*Add 0.5 to values shown for 0-7 if channel is programmed for 5 bits/char.

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CSRA **CSRB**	**Receiver Clock Select**				**Transmitter Clock Select**			
	See text				See text			

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		Miscellaneous Commands			**Disable Tx**	**Enable Tx**	**Disable Rx**	**Enable Rx**
CRA **CRB**	not used- must be 0	See test			0=no 1=yes	0=no 1=yes	0=no 1=yes	0=no 1=yes

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	Received Break	**Framing Error**	**Parity Error**	**Overrun Error**	**TxEMT**	**TxRDY**	**FFULL**	**RxRDY**
SRA **SRB**	0=no 1=yes *	0=no 1=yes *	0=no 1=yes *	0=no 1=yes	0=no 1=yes	0=no 1=yes	0=no 1=yes	0=no 1=yes

*These status bits are appended to the corresponding data character in the receive FIFO. A read of the status register provides these bits (7:5) from the top of the FIFO together with bits 4:0. These bits are cleared by a reset error status command. In character mode they are discarded when the corresponding data character is read from the FIFO.

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	OP7	**OP6**	**OP5**	**OP4**	**OP3**		**OP2**	
OPCR	0=OPR[7] 1=TxRDYB	0=OPR[6] 1=TxRDYA	0=OPR[5] 1=RxRDY/ FFULLB	0=OPR[4] 1=RxRDY/ FFULLA	00=OPR[3] 01=C/T OUTPUT 10=TxCB (1X) 11=RxCB(1X)		00=OPR[2]* 01=TxCA (16X) 10=TxCA (1X) 11=RxCA (1X)	

Peripheral IC

Table 2. Register Bit Formats (Continued)

ACR

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BRG Set Select	Counter/Timer Mode and Source			Delta IP3 Int	Delta IP2 Int	Delta IP1 Int	Delta IP0 Int
0=set1 1=set2	See table 4			0=off 1=on	0=off 1=on	0=off 1=on	0=off 1=on

IPCR

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Delta IP3	Delta IP2	Delta IP1	Delta IP0	IP3	IP2	IP1	IP0
0=no 1=yes	0=no 1=yes	0=no 1=yes	0=no 1=yes	0=low 1=high	0=low 1=high	0=low 1=high	0=low 1=high

ISR

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Input Port Change	Delta Break B	RxRDY/ FFULLB	TxRDYB	Counter Ready	Delta BREAK	RxRDY/ FFULLA	TxRDYA
0=no 1=yes	0=no 1=yes	0=no 1=yes	0=no 1=yes	0=no 1=yes	0=no 1=yes	0=no 1=yes	0=no 1=yes

IMR

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
In Port Change Int	Delta Break B Int	RxRDY/ FFULLB Int	TxRDYB Int	Counter Ready Int	Delta Break A Int	RxRDY/ FFULLA Int	TxRDYA Int
0=off 1=on	0=off 1=on	0=off 1=on	0=off 1=on	0=off 1=on	0=off 1=on	0=off 1=on	0=off 1=on

CTUR

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]

CTLR

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]

not be enabled.
4. The channel A TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e., transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured. MR2A [7:6] =10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxDA output is held high.
4. The RxDA input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2A[7:6] =11. In this mode:

1. Received data is relocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., transmitted parity bit is as received.
5. The receiver must be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected, the device will switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes: if the de-selection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop bit has been retransmitted.

MR2A[5] — Channel A Transmitter Request-to-Send Control — This bit controls the deactivation of the RTSAN output (OP0) by the transmitter. This output is normally asserted by setting OPR[0]) and negated by resetting OPR[0]. MR2A[50=1 causes OPR[0] to be reset automatically one bit time after the characters in the channel A transmit shift register and in the THR, if any, are completely transmitted, including the programmed number of stop bits, if the transmitter is not enabled. This feature can be used to automatically terminate the transmission of a message as follows:

1. Program auto-reset mode: MR2A[5] =1.
2. Enable transmitter.
3. Assert RTSAN: OPR[0] =1.
4. Send message.
5. Disable transmitter after the last character is loaded into the channel A THR.
6. The last character will be transmitted and OPR[0] will be reset one bit time after the last stop bit, causing RTSAN to be negated.

MR2A[4] — Channel A Clear-to-Send Control — If this bit is 0, CTSAN has no effect on the transmitter. If this bit is a 1, the transmitter checks the state of CTSAN (IP0) each time it is ready to send a character. If IP0 is asserted (low), the character is transmitted. If it is negated (high), the TxDA output remains in the marking state and the transmission is delayed until CTSAN goes low. Changes in CTSAN while a character is being transmitted do not affect the transmission of that character.

MR2A[3:0] — Channel A Stop Bit Length Select — This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1-9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a characterlength of 5 bits, 1-1/16 to 2 stop bits can be programmed in increments of 1/16 bit. The receiver only checks for a 'mark' condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit if parity is enabled) in all cases.

If an external 1X clock is used for the transmitter, MR2A [3] =0 selects one stop bit and MR2A[3] =1 selects two stop bits to be transmitted.

MR1B — Channel B Mode Register 1

MR1B is accessed when the channel B MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR1B, the pointer will point to MR2B.

The bit definitions for this register are identical to the bit definitions for MR1A, except that all control actions apply

to the channel B receiver and transmitter and the corresponding inputs and outputs.

MR2B – Channel B Mode Register 2

MR2B is accessed when the channel B MR pointer points to MR2, which occurs after any access to MR1B. Accesses to MR2B do not change the pointer.

The bit definitions for this register are identical to the bit definitions for MR2A, except that all control actions apply to the channel B receiver and transmitter and the corresponding inputs and outputs.

CSRA – Channel A Clock Select Register

CSRA[7:4] – Channel A Receiver Clock Select – This field selects the baud rate clock for the channel A receiver as follows:

CSRA[7:4]				Baud Rate CLOCK = 3.6864MHz ACR[7]=0	ACR[7]=1
0	0	0	0	50	75
0	0	0	1	110	110
0	0	1	0	134.5	134.5
0	0	1	1	220	150
0	1	0	0	300	300
0	1	0	1	600	600
0	1	1	0	1,200	1,200
0	1	1	1	1,050	2,000
1	0	0	0	2,400	2,400
1	0	0	1	4,800	4,800
1	0	1	0	7,200	1,800
1	0	1	1	9,600	9,600
1	1	0	0	38.4K	19.2K
1	1	0	1	Timer	Timer
1	1	1	0	IP4–16X	IP4–16X
1	1	1	1	IP4–1X	IP4-1X

The receiver clock is always a 16X clock except for CSRA [7:4] =1111.

CSRA[3:0] – Channel A Transmitter Clock Select – This field selects the baud rate clock for the channel A transmitter. The field definition is as per CSRA[7:4] except as follows:

CSRA[3:0]				Baud Rate ACR[7]=0	ACR[7]=1
1	1	1	0	IP3 – 16X	IP3 – 16X
1	1	1	1	IP3 – 1X	IP3 – 1X

The transmitter clock is always a 16X clock except for CSRA[3:0] =1111.

CSRB - Channel B Clock Select Register

CSBR[7:4] – Channel B Receiver Clock Select – This field selects the baud rate clock for the channel B receiver. The field definition is as per CSRA[7:4] except as follows:

CSRB[7:4]				Baud Rate ACR[7]=0	ACR[7]=1
1	1	1	0	IP6 – 16X	IP6 – 16X
1	1	1	1	IP6 – 1X	IP6 – 1X

The receiver clock is always a 16X clock except for CSRB [7:4] =1111.

CSRB[3:0] – Channel B Transmitter Clock Select – This field selects the baud rate clock for the channel B transmitter. The field definition is as per CSRA[7:4] except as follows:

CSRB[3:0]				Baud Rate ACR[7]=0	ACR[7]=1
1	1	1	0	IP5 – 16X	IP5 – 16X
1	1	1	1	IP5 – 1X	IP5 – 1X

The transmitter clock is always a 16X clock except for CSRB[3:0] =1111.

CRA – Channel A Command Register

CRA is a register used to supply commands to channel A. Multiple commands can be specified in a single write to CRA as long as the commands are non-conflicting, e.g., the enable transmitter' and 'reset transmitter' commands cannot bespecified in a single command word.

CRA[6:4] – Channel A Miscellaneous Commands – The encoded value of this field may be used to specify a single command as follows:

CRA[6:4]	Command
0 0 0	No command.
0 0 1	Reset MR pointer. Causes the channel A MR pointer to point to MR1.
0 1 0	Reset receiver. Resets the channel A receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.
0 1 1	Reset transmitter. Resets the channel A transmitter as if a hardware reset had been applied.

1 0 0 Reset error status. Clears the channel A. Received Break, Parity Error, Framing Error, and Overrun Error bits in the status register (SRA[7:4]). Used in character mode to clear OE status (although RB, PE, and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.

1 0 1 Reset channel A break change interrupt. Causes the channel A break detect change bit in the interrup status register (ISR[2]) to be cleared to zero.

1 1 0 Start break. Forces the TXDA output low (spacing). If the transmitter is empty the start of the break condition will be delayed up to two bit times. If the transmitter is active the break begins when transmission of the character is completed. If a character is in the THR, the start of the break will be delayed until that character, or any others loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted.

1 1 1 Stop Break. The TXDA line will go high (marking) within two bit times. TXDA will remain high for one bit time before the next character, if any, is transmitted.

CRA[3] – Disable Channel A Transmitter – This command terminates transmitter operation and resets the TxRDY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

CRA[2] – Enable Channel A Transmitter – Enables operation of the channel A transmitter. The TxRDY status bit will be aserted.

CRA[1] – Disable Channel A Receiver – This command terminates operation of the receiver immediately – a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special multidrop mode is programmed, the receiver operates even if it is disabled. See Operation section.

CRA[0] – Enable Channel A Receiver – Enables operation of the channel A receiver. If not in the special wakeup mode, this also forces the receiver into the search for start-bit state.

CRB – Channel B Command Register

CRB is a register used to supply commands to channel B. Multiple commands can be specified in a single write to CRB as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

The bit definitions for this register are identical to the bit definitions for CRA, except that all control actions apply to the channel B receiver and transmitter and the corresponding inputs and outputs.

SRA – Channel A Status Register

SRA[7] – Channel A Received Break – This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received: further entries to the FIFO are inhibited until the RxDA line returns to the marking state for at least one-half a bit time (two successive edges of the internal or external 1 x clock).

When this bit is set, the channel A 'change in break' bit in the ISR (ISR[2]) is set. ISR[2] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until at least the end of the next character time in order for it to be detected.

SRA[6] – Channel A Framing Error – This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SRA[5] – Channel A Parity Error – This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity.

In the special multidrop mode the parity error bit stores the received A/D bit.

SRA[4] – Channel A Overrun Error – This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost.

This bit is cleared by a 'reset error status' command.

SRA[3] – Channel A Transmitter Empty (TxEMTA) – This bit will be set when the channel A transmitter underruns, i.e., both the transmit holding register (THR) and the transmit shift register are empty. It is set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission. It is reset when the THR is loaded by the CPU or when the transmitter is disabled.

SRA[2] – Channel A Transmitter Ready (TxRDYA) – This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, viz., characters loaded into the THR while the transmitter is disabled will not be transmitted.

SRA[1] – Channel A FIFO Full (FFULLA) – This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, FFULL will not be reset when the CPU reads the RHR.

SRA[0] – Channel A Receiver Ready (RxRDYA) – This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR, if after this read there are no more characters still in the FIFO.

SRB – Channel B Status Register

The bit definitions for this register are identical to the bit definitions for SRA, except that all status applies to the channel B receiver and transmitter and the corresponding inputs and outputs.

OPCR – Output Port Configuration Register

OPCR[7] – OP7 Output Select – This bit programs the OP7 output to provide one of the following:

- The complement of OPR[7]
- The channel B transmitter interrupt output which is the complement of TxRDYB. When in this mode OP7 acts as an open collector output. Note that this output is not masked by the contents of the IMR.

OPCR[6] – OP6 Output Select – This bit programs the OP6 output to provide one of the following:

- The complement of OPR[6]
- The channel A transmitter interrupt output, which is the complement of TxRDYA. When in this mode OP6 acts as an open collector output. Note that this output is not masked by the contents of the IMR.

OPCR[5] – OP5 Output Select – This bit programs the OP5 output to provide one of the following:

- The complement of OPR[5]
- The channel B receiver interrupt output, which is the complement of ISR[5]. When in this mode OP5 acts as an open collector output. Note that this output is not masked by the contents of the IMR.

OPCR[4] – OP4 Output Select – This bit programs the OP4 output to provide one of the following:

- The complement of OPR[4]
- The channel A receiver interrupt output, which is the complement of ISR[1]. When in this mode OP4 acts as an open collector output. Note that this output is not masked by the contents of the IMR.

OPCR[3:2] – OP3 Output Select – This field programs the OP3 output to privde one of the following:

- The complement of OPR[3]
- The counter/timer output, in which case OP3 acts as an open collector output. In the timer mode, this output is a square wave at the programmed frequency. In the counter mode, the output remains high until terminal count is reached, at which time it goes low. The output returns to the high state when the counter is stopped by a stop counter command. Note that this output is not masked by the contents of the IMR.
- The 1X clock for the channel B transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the channel B receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

OPCR[1:0] – OP2 Output Select – This field programs the OP2 output to provide one of the following:

- The complement of OPR[2]
- The 16X clock for the channel A transmitter. This is the clock selected by CSRA[3:0], and will be a 1X clock if CSRA [3:0] = 1111.
- The 1X clock for the channel A transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.

– The 1X clock for the channel A receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

ACR – Auxiliary Control Register

ACR[7] – Baud Rate Generator Set Select – This bit selects one of two sets of baud rates to be generated by the BRG:

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05K, 1.2K, 2.4K, 4.8K, 7.2K, 9.6K, and 38.4K baud.

Set 2: 75, 110, 134.5, 150, 300, 600, 1.2K, 1.8K, 2.0K, 2.4K, 4.8K, 9.6K, and 19.2K baud.

The selected set of rates is available for use by the channel A and B receivers and transmitters as described in CSRA and CSRB. Baud rate generator characteristics are given in Table 3.

ACR[6:4] – Counter/Timer Mode and Clock Source Select – This field selects the operating mode of the counter/timer and its clock source as shown in Table 4.

ACR[3:0] – IP3, IP2, IP1, IP0 Change of State Interrupt Enable – This field selects which bits of the Input Port Change register (IPCR) cause the input change bit in the interrupt status register (ISR[7]) to be set. If a bit is in the 'on' state, the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which results in the generation of an interrupt output if IMR[7]=1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

IPCR – Input Port Change Register

IPCR[7:4] – IP3, IP2, IP1, IP0 Change of State – These bits are set when a change of state, as defined in the Input Port section of this data sheet, occurs at the respective input pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register.

The setting of these bits can be programmed to generate an interrupt to the CPU.

IPCR[3:0] – IP3, IP2, IP1, IP0 Current State – These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the interrupt mask register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR – the true status will be provided regardless of the contents of the IMR. The contents of this register are initialized to 00_{16} when the DUART is reset.

ISR[7] – Input Port Change Status – This bit is a '1' when a change of state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been selected to cause an interrupt by the programming of ACR[3:0]. The bit is cleared when the CPU reads the IPCR.

ISR[6] – Channel B Change in Break – This bit, when set, indicates that the channel B receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a channel B 'reset break change interrupt' command.

ISR[5] – Channel B Receiver Ready or FIFO Full – The function of this bit is programmed by MR1B[6]. If programmed as receiver ready, it indicates that a character has been received in channel B and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer causes the channel B FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive

Table 3. Baud Rate Generator Characteristics Crystal or Clock = 3.6864 MHz

Nominal Rate (Baud)	Actual 16X Clock (KHz)	Error (Percent)
50	0.8	0
75	1.2	0
110	1.759	−0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	−0.260
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
19.2K	307.2	0
38.4K	614.4	0

Table 4. ACR [6:4] Field Definition

ACR [6:4]			Mode	Clock Source
0	0	0	Counter	External (IP2)
0	0	1	Counter	TXCA – 1X clock of channel A transmitter
0	1	0	Counter	TXCB – 1X clock of channel B transmitter
0	1	1	Counter	Crystal or external clock (X1/CLK) divided by 16
1	0	0	Timer	External (IP2)
1	0	1	Timer	External (IP2) divided by 16
1	1	0	Timer	Crystal or external clock (X1/CLK)
1	1	1	Timer	Crystal or external clock (X1/CLK) divided by 16

shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

ISR[4] – Channel B Transmitter Ready – This bit is a duplicate of TxRDYB (SRB[2]).

ISR[3] – Counter Ready – In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/timer reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the counter/timer.

ISR[2] – Channel A Change in Break – This bit, when set, indicates that the channel A receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a channel A 'reset break change interrupt' command.

ISR[1] – Channel A Receiver Ready or FIFO Full – The function of this bit is programmed by MR1A[6]. If programmed as receiver ready, it indicates that a character has been received in channel A and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer causes the channel' A FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

ISR[0] – Channel A Transmitter Ready – This bit is a duplicate of TxRDYA (SRA[2]).

IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR cause an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the programmable interrupt output OP3-OP7 or the reading of the ISR.

CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs respectively of the value to be used by the counter/timer in either the counter or timer modes of operation The minimum value which may be loaded into the CTUR/CTLR registers is 0002_{16}. Note that these registers are write-only and cannot be read by the CPU.

In the timer (programmable divider) mode, the C/T generates a square wave with a period of twice the value (in clock periods) to the CTUR and CTLR. If the value in CTUR or CTLR is changed, the current half-period will not be affected, but subsequent half periods will be. In this mode the C/T runs continuously. Receipt of a start counter command (read with A3-A0=1110) causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command (read with A3-A0=111). The command, however, does not stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR by the CPU. Counting begins upon receipt of a start counter command. Upon reaching terminal count (0000_{16}), the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If OP3 is programmed to be the output of the C/T, the output remains high until terminal count is reached, at which time it goes low. The output returns to the high state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter command. If new values have not been loaded, the previous count values are preserved and used for the next count cycle.

In the counter mode, the current value of the upper and lower 8 bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8-bits to the upper 8-bits occurs between the times that both halves of the counter are read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

Ordering Information

Part Number	Package
UM2681-1	40 DIP
UM2681-2	28 DIP
UM2681-3	24 DIP

UM6520/UM6520A

Peripheral Interface Adapter(PIA)

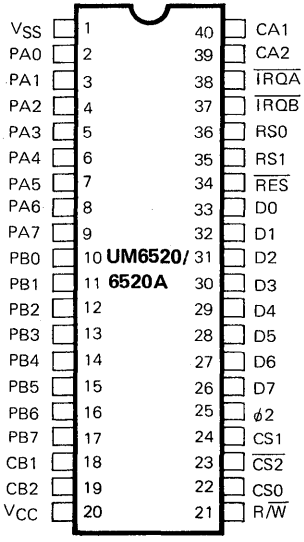
Features

- Direct replacement for Motorola MC6820
- Single +5V power supply
- Two 8-bit bi-directional I/O ports with individual data direction control
- CMOS-compatible peripheral port A lines
- Automatic "handshake.' control of data transfers
- Programmable interrupt capability
- Automatic initialization on power up
- 1 and 2 MHz versions

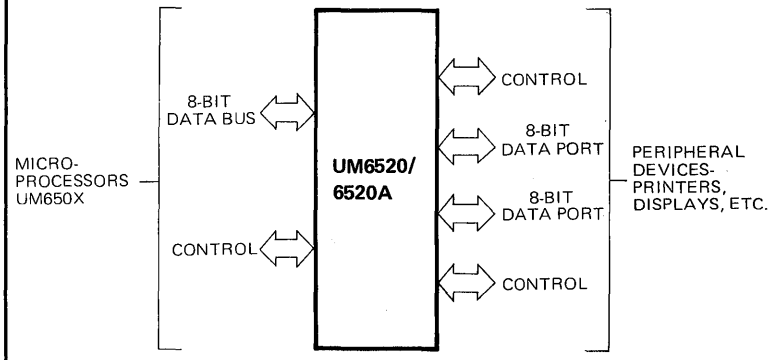
General Description

The UM6520/A peripheral Interface Adapter (PIA) is designed to provide a broad range of peripheral control to microcomputer systems. Control of peripheral devices is accomplished through two 8-bit bi-directional I/O ports. Each I/O line may be programmed to be either an input or an output. In addition, four peripheral control lines are provided to perform "handshaking" during data transfers.

Pin Configuration



Block Diagram



Peripheral IC

Absolute Maximum Ratings*

Supply Voltage V_{CC} . . . . . −0.3V to +7.0V
Input Voltage V_{IN} . . . . . −0.3V to +7.0V
Operating Temperature Range T_A . . . . . 0°C to +70°C
Storage Temperature Range T_{STG} . . . . −55°C to +150°C
Note:
This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

*Comments

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

(V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0-70°C unless otherwise noted)

Characteristics	Symbol	Min.	Max.	Units
Input High Voltage	V_{IH}	+2.0	V_{CC}	V
Input Low Voltage	V_{IL}	−0.3	+0.8	V
Input Leakage Current V_{IN} = 0 to 5.0V R/$\overline{W}$, $\overline{Reset}$, RS_0, RS_1, CS_0, CS_1, $\overline{CS_2}$, CA_1, CB_1, ϕ_2	I_{IN}	–	±2.5	μA
Three-State (Off State Input Current) (V_{IN} = 0.4 to 2.4 V, V_{CC} = max), D_0-D_7, PB_0-PB_7, CB_2	I_{TSI}	–	±10	μA
Input High Current (V_{IH} = 2.4 V), PA_0-PA_7, CA_2	I_{IH}	−100	–	μA
Input Low Current (V_{IL} = 0.4 V), PA_0-PA_7, CA_2	I_{IL}	–	1.6	mA
Output High Voltage (V_{CC} = min, I_{OH} = −100 μA)	V_{OH}	2.4	–	V
Output Low Voltage (V_{CC} = min, I_{OL} = 1.6 mA)	V_{OL}	–	+0.4	V
Output High Current (Sourcing) (V_{OH} = 2.4 V) (V_O = 1.5 V, the current for driving other than TTL, e.g., Darlington Base), PB_0-PB_7, CB_2	I_{OH}	−100 −1.0	– −10	μA mA
Output Low Current (Sinking) (V_{OL} = 0.4 V)	I_{OL}	1.6	–	mA
Output Leakage Current (Off-State), $\overline{IRQA}$, $\overline{IRQB}$	I_{OFF}	–	10	μA
Power Dissipation (V_{CC} = 5.25 V)	P_D	–	500	mW
Input Capacitance (V_{IN} = 0, T_A = 25°C, f = 1.0 MHz) D_0-D_7, PA_0-PA_7, PB_0-PB_7, VA_2, CB_2 R/$\overline{W}$, $\overline{Reset}$, RS_0, RS_1, CS_0, CS_1, $\overline{CS_2}$, CA_1, CB_1, ϕ_2	C_{IN}	 – – –	 10 7.0 20	pF
Output Capacitance (V_{IN} = 0, T_A = 25°C, f = 1.0 MHz)	C_{OUT}	–	10	pF

Note: Negative sign indicates outward current flow, positive indicates inward flow.

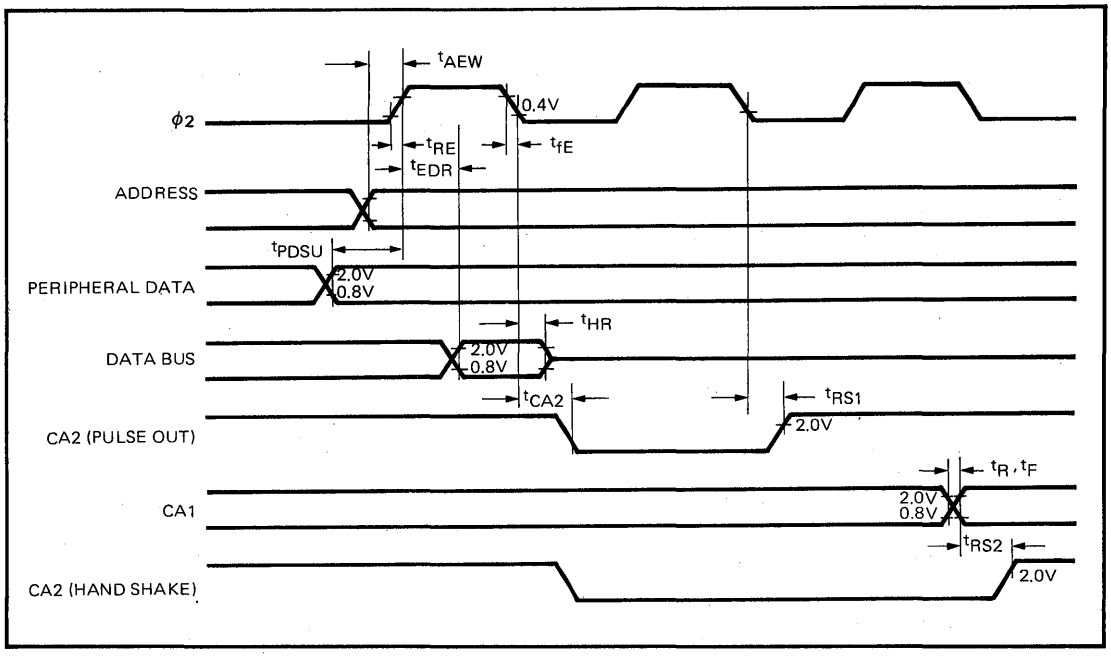


Figure 1. Read Timing Characteristics

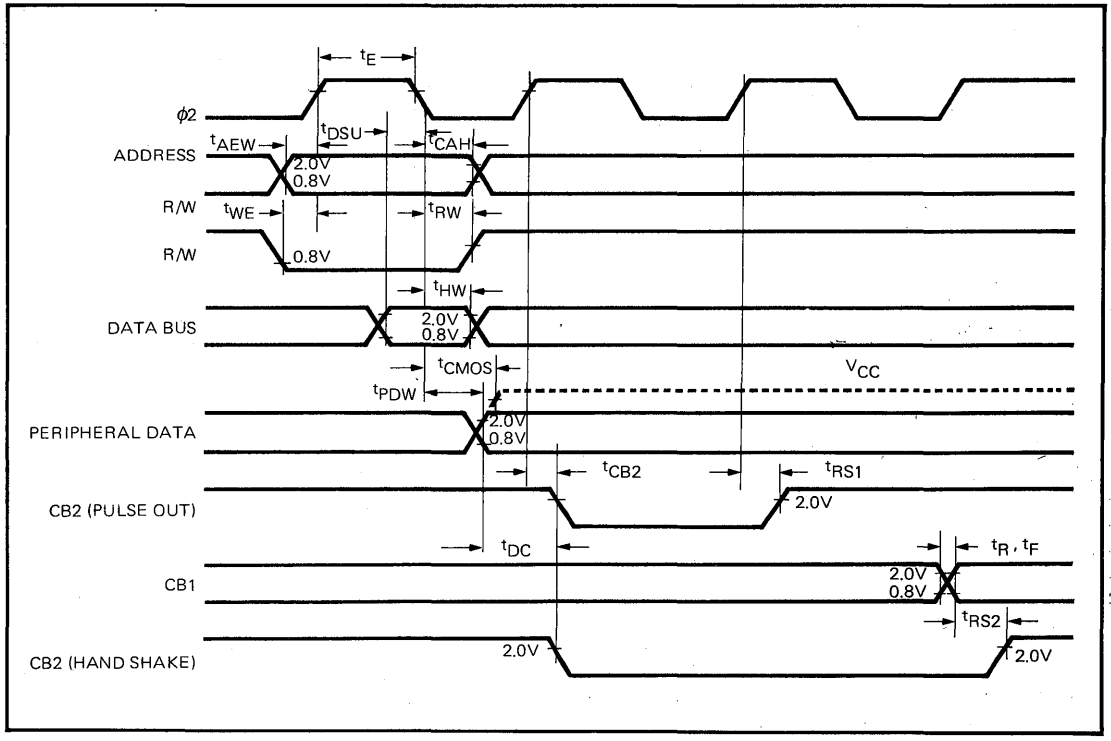


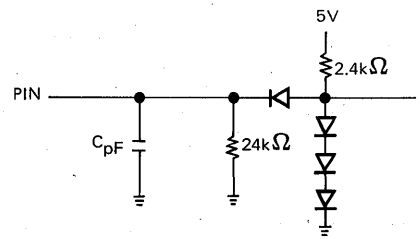
Figure 2. Write Timing Characteristics

Switching Characteristics

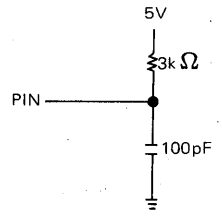
(V_{CC} = +5V ± 5%, T_A = 0-70°C, unless otherwise noted)

Characteristics	Symbol	UM6520 (1 MHz)		UM6520A (2 MHz)		Units
		Min.	Max.	Min.	Max.	
READ TIMING CHARACTERISTICS						
Delay Time, Address Valid to ϕ_2 Positive Transition	T_{AEW}	180	–	90	–	ns
Delay Time, ϕ_2 Positive Transition to Date Valid on Bus	T_{EDR}	–	395	–	190	ns
Peripheral Data Setup Time	T_{PDSU}	300	–	150	–	ns
Data Bus Hold Time	T_{HR}	10	–	10	–	ns
Delay Time, ϕ_2 Negative Transition to CA2 Negative Transition	T_{CA2}	–	1.0	–	0.5	μs
Delay Time, ϕ_2 Negative Transition to CA2 Positive Transition	T_{RS1}	–	1.0	–	0.5	μs
Rise and Fall Time for CA1 and CA2 Input Signals	t_r , t_f	–	1.0	–	0.5	μs
Delay Time from CA1 Active Transition to CA2 Positive Transition	T_{RS2}	–	2.0	–	1.0	μs
Rise and Fall Time for ϕ_2 Input	t_{rE} , t_{fE}	–	25	–	25	ns
WRITE TIMING CHARACTERISTICS						
ϕ_2 Pulse Width	T_E	0.440	–	0.200	–	μs
Delay Time, Address Valid to ϕ_2 Positive Transition	T_{AEW}	180	–	90	–	ns
Delay Time, Data Valid to ϕ_2 Negative Transition	T_{DSU}	300	–	150	–	ns
Delay Time, Read/Write Negative Transition to ϕ_2 Positive Transition	T_{WE}	130	–	65	–	ns
Data Bus Hold Time	T_{HW}	10	–	10	–	ns
Delay Time, ϕ_2 Negative Transition to Peripheral Data Valid	T_{PDW}	–	1.0	–	0.5	μs
Delay Time, ϕ_2 Negative Transition to Peripheral Data Valid CMOS (V_{CC} – 30%) PA0-PA7, CA2	T_{CMOS}	–	2.0	–	1.0	μs
Delay Time, ϕ_2 Positive Transition to CB2 Negative Transition	T_{CB2}	–	1.0	–	0.5	μs
Delay Time, Peripheral Data Valid to CB2 Negative Transition	T_{DC}	0	1.5	0	0.75	μs
Delay Time, ϕ_2 Positive Transition CB2 Positive Transition	T_{RS1}	–	1.0	–	0.5	μs
Rise and Fall Time for CB1 and CB2 Input Signals	t_r , t_f	–	1.0	–	0.5	μs
Delay Time, CB1 Active Transition to CB2 Positive Transition	T_{RS2}	–	2.0	–	1.0	μs
Delay Time, ϕ_2 Negative Transition to Read/Write Positive Transition	T_{RW}	50	–	25	–	ns

Test Load



C = 130 pF MAX. FOR DB0-DB7
C = 30 pF MAX. FOR ALL OTHER OUTPUT



OPEN COLLECTOR
OUTPUT TEST LOAD

Interface Signal Description

$\overline{RES}$ (Reset)

This signal is used to initialize the PIA. A low signal on the $\overline{RES}$ input causes all internal registers to be cleared.

ϕ_2 (Input Clock)

This input is the system ϕ_2 clock and is used to trigger all data transfers between the microprocessor and the PIA.

R/$\overline{W}$ (Read/Write)

This signal is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ signal permits the processor to read data supplied by the PIA; a low on the R/$\overline{W}$ signal permits the processor to Write into the PIA.

$\overline{IRQA}$, $\overline{IRQB}$ (Interrupt Requests)

$\overline{IRQA}$ and $\overline{IRQB}$ are interrupt lines generated by the PIA for ports A and B respectively. These signals are active low signals and have open-drain outputs, thus allowing multiple IRQ signals from multiple PIA's to be wire-ORed together before connecting to the processor IRQ signal input.

D_0-D_7 (Data Bus)

These eight data bus lines are used to transfer data information between the processor and the PIA. These signals are bi-directional and are normally highimpedance except when selected for a read operation.

CS0, CS1, $\overline{CS2}$ (Chip Selects)

The PIA is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. These three chip select lines are normally connected to the processor address lines either directly or through external decoder circuits.

RS0, RS1 (Register Selects)

These two signals are used to select the various registers inside the PIA.

Internal Architecture

The UM6520/A is organized into two independent sections referred to as the "A Side" and the "B Side." Each section consists of a Control Register (CRA, CRB), Data Direction Register (DDRA, DDRB), Output Register (ORA, ORB), Interrupt Status Control and the buffers necessary to drive the Peripheral Interface buses. Figure 3 is a block diagram of the UM6520/A.

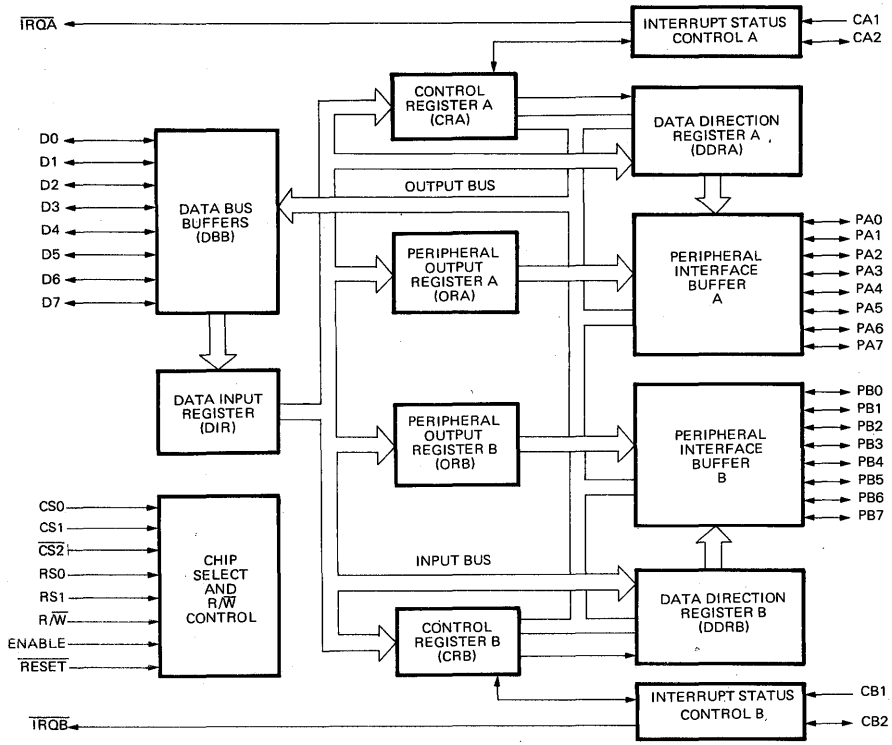


Figure 3. UM6520/UM6520A Block Diagram

	7	6	5 4 3	2	1 0
CRA	IRQA1	IRQA2	CA2 Control	DDRA Access	CA1 Control
	7	6	5 4 3	2	1 0
CRB	IRQB1	IRQB2	CB2 Control	DDRB Access	CB1 Control

Figure 4. Control Registers

Data Input Register

When the Microprocessor writes data into the UM6520/A, the data which appears on the data bus during the Phase Two clock pulse is latched into the Data Input Register. It is then transferred into one of six internal registers of the UM6520/A after the trailing edge of Phase Two. This assures that the data on the peripheral output lines will make smooth transitions from high to low or from low to high and the voltage will remain stable except when it is going to the opposite polarity.

Control Registers (CRA and CRB)

Figure 4 illustrates the bit designation and functions in the Control Registers. The Control Registers allow the microprocessor to control the operation of the Interrupt Control inputs (CA1, CA2, CB1, CB2), and Peripheral Control outputs (CA2, CB2). Bit 2 in each register controls the addressing of the Data Direction Registers (DDRA, DDRB) and the Output Registers (ORA, ORB). In addition, two bits (bit 6 and 7) are provided in each control register to indicate the status of the interrupt input lines (CA1, CA2, CB1, CB2). These interrupt status bits (IRQA1, (IRQB1) are normally interrogated by the microprocessor during the interrupt service routine to determine the source of an active interrupt. These are the interrupt lines which drive the interrupt input ($\overline{IRQ}$, $\overline{NMI}$) of the microprocessor.

Data Direction Registers (DDRA, DDRB)

The Data Direction Registers allow the processor to program each line in the 8-bit Peripheral I/O port to be either an input or an output. Each bit in DDRA controls the corresponding line in the Peripheral A port and each bit in DDRB controls the corresponding line in the Peripheral B port. Placing a "0" in a bit position in the Data Direction Register cause the corresponding Peripheral I/O line to act as an input; a "1" causes it to act as an output.

Peripheral Output Registers (ORA, ORB)

The Peripheral Output Registers store the output data which appears on the Peripheral I/O port. Writing a "0" into a bit in ORA causes the corresponding line on the Peripheral A port to go low ($< 0.4V$) if that line is programmed to act as an output. A "1" causes the corresponding output to go high. The lines of the Peripheral B port are controlled by ORB in the same manner.

Interrupt Status Control

The four interrupt/peripheral control lines (CA1, CA2, CB1, CB2) are controlled by the Interrupt Status Control logic (A, B). This logic interprets the contents of the corresponding Control Register, detects active transitions on the interrupt inputs and performs those operations necessary to assure proper operation of these four peripheral interface lines.

Peripheral Interface Buffers (A, B) and Data Bus Buffers (DBB)

These Buffers provide the necessary current and voltage drive on the peripheral I/O ports and data bus to assure proper system operation and to meet the device specifications.

Functional Description

Bit 2 (DDR) in each Control Register (CRA and CRB) controls the accessing to the Data Direction Register or the Peripheral interface. If bit 2 is a "1", a Peripheral Output register (ORA, ORB) is selected, and if bit 2 is a "0", a Data Direction Register (DDRA, DDRB) is selected. The Data Direction Register Access Control bit, together with the Register Select lines (RS0, SR1) selects the various internal registers as shown in Figure 5.

In order to write data into DDRA, ORA, DDRB, or ORB registers, bit 2 in the proper Control Register must first be set. The desired register may then be accessed with the address determined by the address interconnect technique used.

Register Select Lines (RS0), (RS1)

These two register select lines are used to select the various registers inside the UM6520/A. These input lines are used in conjunction with internal control registers to select a particular register that is to be accessed by the microprocessor. These lines are normally connected to microprocessor address output lines. These lines operate in conjunction with the chip-select inputs to allow the microprocessor to address a single 8-bit register within the microprocessor address space. This register may be an internal register (CRA, ORA, etc.) or it may be a Peripheral I/O port.

The processor may write directly into the Control Registers (CRA, CRB), the Data Direction Registers (DDRA, DDRB) and the Peripheral Output Registers (ORA, ORB). In addition, the processor may directly read the contents of the Control Registers and the Data Direction Registers. Accessing the Peripheral Output Register for the purpose of reading data back into the processor operates differently on the ORA and the ORB registers and therefore are discussed separately below.

Reading the Peripheral A I/O Port

The Peripheral A I/O port consists of 8 lines which can be programmed to act as inputs or outputs. When programmed to act as outputs, each line reflects the contents of the corresponding bit in the Peripheral Output Register. When programmed to act as inputs, these lines will go high or low depending on the input data. The Peripheral Output Register (ORA) has no effect on those lines programmed to act as inputs. The eight lines of the Peripheral A I/O port therefore contain either input or output data depending on whether the line is programmed to act as an input or an output. Performing a Read operation with RS1 = 0, RS0 = 0 and the Data Direction Register Access Control bit (CRA-2) = 1, directly transfers the data on the Peripheral A I/O lines into the processor (via the data bus). This will contain both the input and output data. The processor must be programmed to recognize and interpret only those bits which are important to the particular peripheral operation being performed.

Since the processor always reads the Peripheral A I/O port pins instead of the actual Peripheral Output Register (ORA), it is possible for the data read into the processor to differ from the contents of the Peripheral Output Register for an output line. This is true when the I/O pin is not allowed to go to a full +2.4V DC when the Peripheral Output register contains a logic 1. In this case, the processor will read a 0 from the Peripheral A pin, even though the corresponding bit in the Peripheral Output Register is a 1.

Reading the Peripheral B I/O Port

Reading the Peripheral B I/O port yields a combination of input and output data in a manner similar to the Peripheral A port. However, data is read directly from the Peripheral B Output Register (ORB) for those lines programmed to act as outputs. It is therefore possible to load down the Peripheral B Output lines without causing incorrect data to be transferred back into the processor on a Read operation.

Interrupt Request Lines ($\overline{IRQA}$, $\overline{IRQB}$)

The active low Interrupt Request lines ($\overline{IRQA}$ and $\overline{IRQB}$) act to interrupt the microprocessor either directly or through external interrupt priority circuitry. These lines are "open drain" and are capable of sinking 1.6 milliamps from an external source. This permits all interrupt request lines to be tied together in a "wired-OR" configuration. The "A" and "B" in the titles of these lines correspond to the "A" peripheral port and the "B" peripheral port. Hence each interrupt request line services one peripheral data port.

Each Interrupt Request line has two interrupt flag bits

Register Select Pin		Data Direction Register Access Control Bit		Register Selected
RS1	RS0	CRA-2	CRB-2	
0	0	1	–	Peripheral Interface A
0	0	0	–	Data Direction Register A
0	1	–	–	Control Register A
1	0	–	1	Peripheral Interface B
1	0	–	0	Data Direction Register B
1	1	–	–	Control Register B

Figure 5. Register Addressing

which can cause the Interrupt Request line to go low. These flags are bits 6 and 7 in the two Control Registers. These flags act as the link between the peripheral interrupt signals and the microprocessor interrupt inputs. Each flag has a corresponding interrupt disable bit which allows the processor to enable or disable the interrupt from each of the four interrupt inputs (CA1, CA2, CB1, CB2).

The four interrupt flags are set by active transitions of the signal on the interrupt input (CA1, CA2, CB1, CB2).

Control of $\overline{IRQA}$

Control Register A bit 7 is always set by an active transition of the CA1 interrupt input signal. Interrupting from this flag can be disabled by setting bit 0 in the Control Register A (CRA) to a logic 0. Likewise, Control Register A bit 6 can be set by an active transition of the CA2 interrupt input signal. Interrupting from this flag can be disabled by setting bit 3 in the Control Register to a logic 0.

Both bit 6 and bit 7 in CRA are reset by a "Read Peripheral Output Register A" operation. This is defined as an operation in which the proper chip-select and register-select signals are provided to allow the processor to read the Peripheral A I/O port.

Control of $\overline{IRQB}$

Control of $\overline{IRQB}$ is performed in exactly the same manner as that described above for $\overline{IRQA}$. Bit 7 in CRB is set by an active transition on CB1; interrupting from this flag is controlled by CRB bit 0. Likewise, bit 6 in CRB is set by an active transition on CB2; interrupting from this flag is controlled by CRB bit 3.

Also, both bit 6 and bit 7 are reset by a "Read Peripheral B Output Register" operation.

SUMMARY:
$\overline{IRQA}$ goes low when CRA-7 = 1 and CRA-0 = 1 or when CRA-6 = 1 and CRA-3 = 1
$\overline{IRQB}$ goes low when CRB-7 = 1 and CRB-0 = 1 or when CRB-6 = 1 and CRB-3 = 1

It should be stressed at this point that the flags act as the link between the peripheral interrupt signals and the processor interrupt inputs. The interrupt disable bits allow the processor to control the interrupt function.

Interface Between UM6520/A and Peripheral Devices

The UM6520/A provides two 8-bit bi-directional ports and 4 interrupt/control lines for interfacing to peripheral devices. These ports and the associated interrupt/control lines are referred to as the "A" side and the "B" side. Each side has its own unique characteristics and will therefore be discussed separately below.

Peripheral I/O Ports

The Peripheral A and Peripheral B I/O Ports allow the microprocessor to interface to the input lines on the peripheral device by loading data into the Peripheral Output Register. They also allow the processor to interface with the peripheral device output lines by reading the data on the Peripheral Port input lines directly onto the data bus and into the internal registers of the processor.

Peripheral A I/O Port (PA0-PA7)

Each of the Peripheral I/O lines can be programmed to act as an input or an output. This is accomplished by setting a "1" in the corresponding bit in the Data Direction Register for those lines which are to act as outputs. A "0" in a bit of the Data Direction Register causes the corresponding Peripheral I/O lines to act as an input.

The buffers which drive the Peripheral A I/O lines contain "passive" pull-ups as shown in Figure 6. These pull-up devices are resistive in nature and therefore allow the output voltage to go to V_{CC} for a logic 1. The switches can sink a full 1.6mA, making these buffers capable of driving one standard TTL load.

In the input mode, the pull-up devices shown in Figure 6 are still connected to the I/O pin and still supply current to this pin. For this reason, these lines represent one standard TTL load in the input mode.

Peripheral B I/O Port (PB0-PB7)

The Peripheral B I/O port duplicates many of the functions of the Peripheral A port. The process of programming these lines to act as an input or an output has been discussed previously. Likewise, the effect of reading or writing this port has been discussed. However, there are several characteristics of the buffers driving these lines which affect their use in peripheral interfacing.

The Peripheral B I/O port buffers are push-pull devices

as shown in Figure 7. The pull-up devices are switched "OFF" in the "0" state and "ON" for a logic 1. Since these pull-ups are active devices, the logic "1" voltage is not guaranteed to go higher than +2.4V. They are TTL compatible but are not CMOS compatible.

However, the active pull-up devices can source up to 1mA at 1.5V. This current drive capability is provided to allow direct connection to Darlington transistor switches. This allows very simple control of relays, lamps, etc.

Because these outputs are designed to drive transistors directly, the output data is read directly from the Peripheral Output Register for those lines programmed to act as inputs.

The final characteristic which is a function of the Peripheral B push-pull buffers is the high-impedance input state. When the Peripheral B I/O lines are programmed to act as inputs, the output buffer enters the high impedance state.

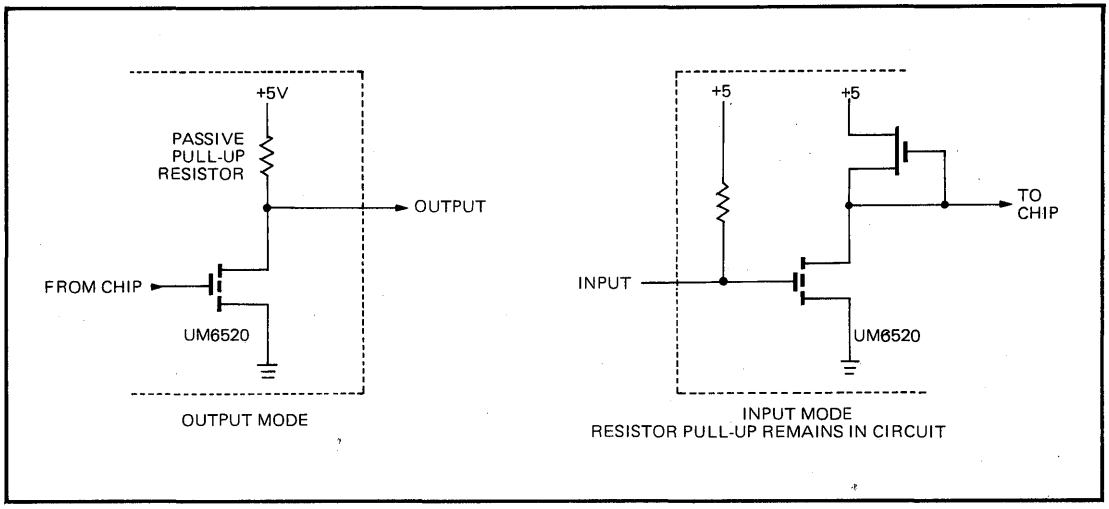


Figure 6. Port A Buffer Circuit (PA_0-PA_7)

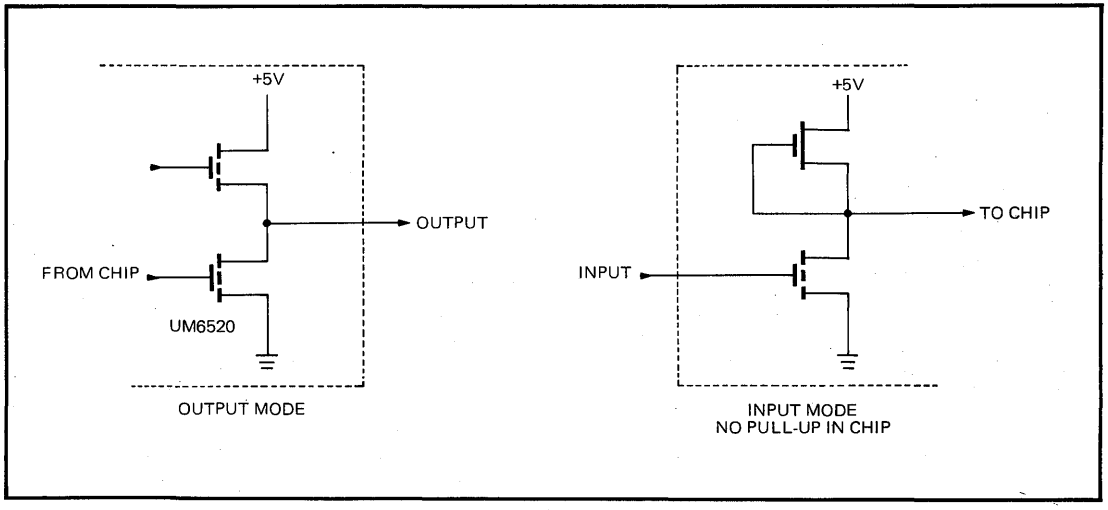


Figure 7. Port B Buffer Circuit (PB_0-PB_7)

Interrupt Input/Peripheral Control Lines (CA1, CA2, CB1, CB2)

The four interrupt input/peripheral control lines provide a number of special peripheral control functions. These lines greatly enhance the power of the two general purpose interface ports (PA0-PA7, PB0-PB7). Figure 8 summarizes the operation of these control lines.

Peripheral A Interrupt Input/Peripheral Control Lines (CA1, CA2)

CA1 is an interrupt input only. An active transition of the signal on this input will set bit 7 of the Control Register A to a logic 1. The active transition can be programmed by setting a "0" in bit 1 of the CRA if the interrupt flag (bit 7 of CRA) is to be set on a negative transition of the CA1 signal or a "1" if it is to be set on a positive transition.

Note: A negative transition is defined as a transition from a high to a low, and a positive transition is defined as a transition from a low to a high voltage.

Setting the interrupt flag will interrupt the processor through $\overline{IRQA}$ if bit 0 of CRA is a 1 as described previously.

CA2 can act as a totally independent interrupt input or as a peripheral control output. As an input (CRA, bit 5 = 0) it acts to set the interrupt flag, bit 6 of CRA, to a logic 1 on the active transition selected by bit 4 of CRA.

These control register bits and interrupt inputs serve the same basic function as that described above for CA1. The input signal sets the interrupt flag which serves as the link between the peripheral device and the processor interrupt structure. The interrupt disable bit allows the processor to exercise control over the system interrupts.

In the Output mode (CRA, bit 5 = 1), CA2 can operate independently to generate a simple pulse each time the microprocessor reads the data on the Peripheral A I/O port. This mode is selected by setting CRA, bit 4 to a "0" and CRA, bit 3 to a "1". This pulse output can be used to control the counters, shift registers, etc. which make sequential data available on the Peripheral input lines.

A second output mode allows CA2 to be used in conjunction with CA1 to "handshake" between the processor and the peripheral device. On the A side, this technique allows positive control of data transfers from the peripheral device into the microprocessor. The CA1 input signals the processor that data is available by interrupting the processor. The processor reads the data and sets CA2 low. This signals the peripheral device that it can make new data available.

The final output mode can be selected by setting bit 4 of CRA to a 1. In this mode, CA2 is a simple peripheral control output which can be set high or low by setting bit 3 of CRA to a 1 or a 0 respectively.

Peripheral B Interrupt Input/Peripheral Control Lines (CB1, CB2)

CB1 operates as an interrupt input only in the same manner as CA1. Bit 7 of CRB is set by the active transition selected by bit 0 of CRB. Likewise, the CB2 input mode operates exactly the same as the CA2 input modes. The CB2 output modes, CRB bit 5 = 1, differ somewhat from those of CA2. The pulse output occurs when the processor writes data into the Peripheral B Output Register. Also, the "handshaking" operates on data transfers from the processor into the peripheral device.

CA1/CB1 CONTROL

CRA (CRB)		Active Transition of Input Signal*	IRQA (IRQB) Interrupt Outputs
Bit 1	Bit 0		
0	0	Negative	Disable – remain high
0	1	Negative	Enable – goes low when bit 7 in CRA (CRB) is set by active transition of signal on CA1 (CB1)
1	0	Positive	Disable – remain high
1	1	Positive	Enable – as explained above

*Note: Bit 7 of CRA (CRB) will be set to a logic 1 by an active transition of the CA1 (CB1) signal. This is independent of the state of Bit 0 in CRA (CRB).

CA2/CB2 INPUT MODES

CRA (CRB)			Active Transition of Input Signal*	IRQA (IRQB) Interrupt Outputs
Bit 5	Bit 4	Bit 3		
0	0	0	Negative	Disable – remains high
0	0	1	Negative	Enable – goes low when bit 6 in CRA (CRB) is set by active transition of signal on CA2 (CB2)
0	1	0	Positive	Disable – remains high
0	1	1	Positive	Enable – as explained above

*Note: Bit 6 of CRA (CRB) will be set to a logic 1 by an active transition of the CA2 (CB2) signal. This is independent of the state of Bit 3 in CRA (CRB).

CA2 OUTPUT MODES

CRA			Mode	Descriptions
Bit 5	Bit 4	Bit 3		
1	0	0	"Handshake" on Read	CA2 is set high on an active transition of the CA1 interrupt input signal and set low by a microprocessor "Read A Data" operation. This allows positive control of data transfers from the peripheral device to the microprocessor.
1	0	1	Pulse Output	CA2 goes low for one cycle after a "Read A Data" operation. This pulse can be used to signal the peripheral device that data was taken.
1	1	0	Manual Output	CA2 set low
1	1	1	Manual Output	CA2 set high

CB2 OUTPUT MODES

CRB			Mode	Descriptions
Bit 5	Bit 4	Bit 3		
1	0	0	"Handshake" on Write	CB2 is set low on microprocessor "Write B Data" operation and is set high by an active transition of the CB1 interrupt input signal. This allows positive control of data transfers from the microprocessor to the peripheral device.
1	0	1	Pulse Output	CB2 goes low for one cycle after a microprocessor "Write B Data" operation. This can be used to signal the peripheral device that data is available.
1	1	0	Manual Output	CB2 set low
1	1	1	Manual Output	CB2 set high

Figure 8. Summary of Operation of Control Lines

UM6521 / UM6521A

Peripheral Interface Adapter(PIA)

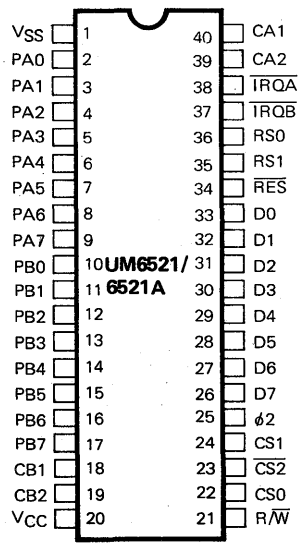
Features

- Extended performance version of UM6520
- Single +5V power supply
- Two 8-bit bi-directional I/O ports with individual data direction control
- CMOS-compatible peripheral port A lines
- Automatic "handshake" control of data transfers
- Programmable interrupt capability
- Automatic initialization on power up
- 1 and 2 MHz versions
- Direct replacement for Motorola MC6821

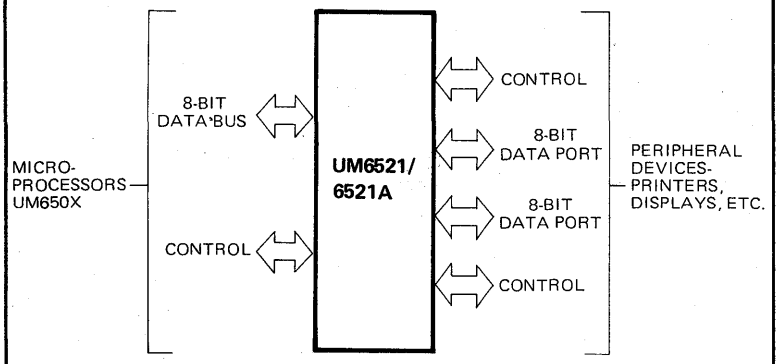
General Description

The UM6521/A Peripheral Interface Adapter (PIA) is designed to provide a broad range of peripheral control to microcomputer systems. It is functionally compatible with the UM6520, but with more drive capability and improved performance. Control of peripheral devices is accomplished through two 8-bit bi-directional I/O ports. Each I/O line may be programmed to be either an input or an output. In addition, four peripheral control lines are provided to perform "handshaking" during data transfers.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Supply Voltage V_{CC} . . . . . −0.3V to +7.0V
Input Voltage V_{IN} . . . . . −0.3V to +7.0V
Operating Temperature Range T_A . . . . . 0°C to +70°C
Storage Temperature Range T_{STG} . . . . −55°C to +150°C
Notice:
This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

*Comments

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

(V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to 70°C unless otherwise noted)

Symbol	Characteristic	Min.	Max.	Units
V_{IH}	Input High Voltage	+2.0	V_{CC}	V
V_{IL}	Input Low Voltage	−0.3	+0.8	V
I_{IN}	Input Leakage Current V_{IN} = 0 to 5.0V R/W, $\overline{Reset}$, RS_0, RS_1, CS_0, CS_1, $\overline{CS_2}$, CA_1, CB_1, ϕ_2	–	±2.5	μA
I_{TSI}	Three-State (Off State Input Current) (V_{IN} = 0.4 to 2.4 V, V_{CC} = max), D_0-D_7, PB_0-PB_7, CB_2	–	±10	μA
I_{IH}	Input High Current (V_{IH} = 2.4 V), PA_0-PA_7, CA_2	−200	–	μA
I_{IL}	Input Low Current (V_{IL} = 0.4 V), PA_0-PA_7, CA_2	–	2.4	mA
V_{OL}	Output Low Voltage (I_L = 3.2 mA), $\overline{IRQA}$, $\overline{IRQB}$	–	0.4	V
V_{OH}	Output High Voltage (I_L = 205 μA), D_0-D_7	2.4	–	V
V_{OL}	Output Low Voltage (I_L = 3.2mA), PA_0-PA_7, PB_0-PB_7, CA_2, CB_2	–	0.4	V
V_{OH}	Output High Voltage (I_H = −200 μA), PA_0-PA_7, PB_0-PB_7, CA_2, CB_2	2.4	–	V
I_{OH}	Output High Current (Direct Transistor Drive Outputs) (V_{OUT} = 1.5 V), PB_0-PB_7, CB_2	−1.0	−10.0	mA
I_{OFF}	Output Leakage Current (Off-State), $\overline{IRQA}$, $\overline{IRQB}$	–	10	μA
P_D	Power Dissipation (V_{CC} = 5.25 V)	–	500	mW
C_{IN}	Input Capacitance (V_{IN} = 0, T_A = 25°C, f = 1.0 MHz) D_0-D_7, PA_0-PA_7, PB_0-PB_7, CA_2, CB_2 R/$\overline{W}$, $\overline{Reset}$, RS_0, RS_1, CS_0, CS_1, $\overline{CS_2}$ CA_1, CB_1, ϕ_2	 – – –	 10 7.0 20	 pF pF pF
C_{OUT}	Output Capacitance (V_{IN} = 0, T_A = 25°C, f = 1.0 MHz)	–	10	pF

Note: Negative sign indicates outward current flow, positive indicates inward flow.

Peripheral IC

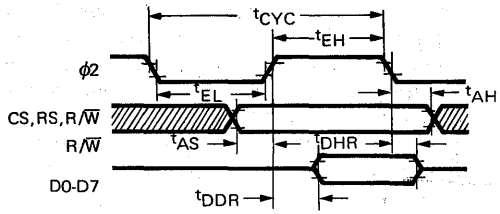


Figure 1. Read Timing Characteristic

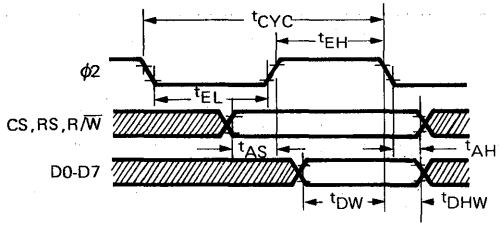


Figure 2. Write Timing Characteristics

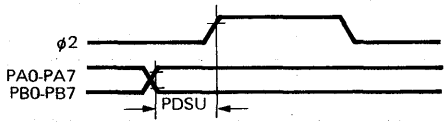


Figure 3. Peripheral Data Setup Time

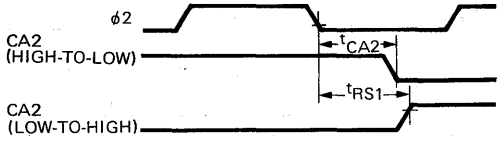


Figure 4. CA_2 Timing

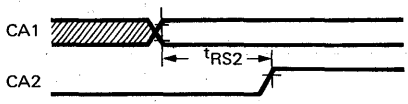


Figure 5. CA_1 /CA_2 Timing

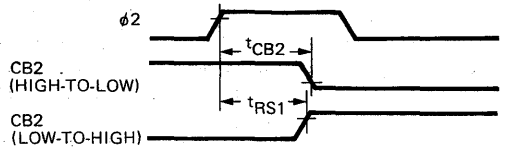


Figure 6. CB_2 Timing

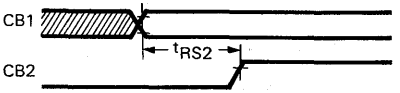


Figure 7. CB_1 /CB_2 Handshake Timing

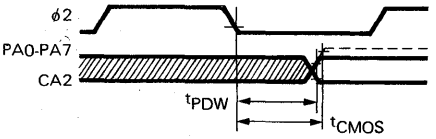


Figure 8. PA Port Delay Time

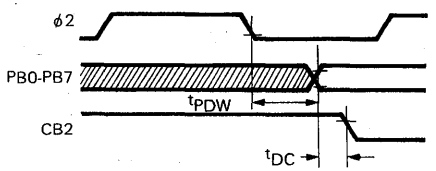


Figure 9. PB Port Delay Time

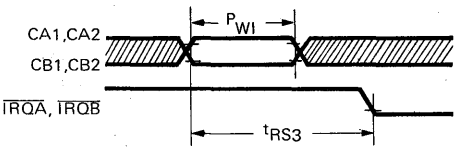


Figure 10. Interrupt Timing

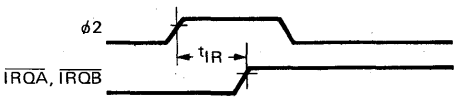


Figure 11. Interrupt Clear Timing

Processor Interface Timing

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C unless otherwise noted)

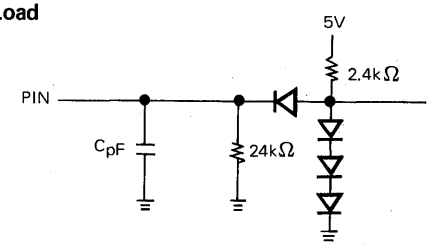
Symbol	Parameter	UM6521		UM6521A		Units
		Min.	Max.	Min.	Max.	
t_{CY}	Cycle Time	1000	–	500	–	ns
t_{EH}	ϕ_2 Pulse Width	440		200	–	ns
t_{EL}	ϕ_2 Pulse Delay	430	–	210	–	ns
t_{AS}	CS, RS, R/$\overline{W}$ Setup Time	160	–	70	–	ns
t_{AH}	CS, RS, R/$\overline{W}$ Hold Time	10	–	10	–	ns
t_{DDR}	Data Delay Time, Read Cycle	–	320	–	180	ns
t_{DHR}	Data Hold Time, Read Cycle	10	–	10	–	ns
t_{DSW}	Data Setup Time, Write Cycle	195	–	60	–	ns
t_{DHW}	Data Hold Time, Write Cycle	10	–	10	–	ns

Processor Interface Timing

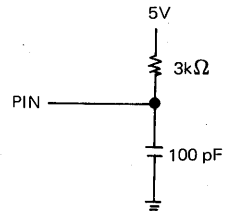
(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C unless otherwise noted)

Symbol	Parameter	UM6521		UM6521A		Units
		Min.	Max.	Min.	Max.	
t_{PDSU}	Peripheral Data Setup Time	200	–	100	–	ns
t_{CA2}	CA_2 Delay Time, High-to-Low	–	1.0	–	0.5	μs
t_{RS1}	CA_2 Delay Time, Low-to-High	–	1.0	–	0.5	μs
t_{RS2}	CA_2 Delay Time, Handshake Mode	–	2.0	–	1.0	μs
t_{CB2}	CB_2 Delay Time, High-to-Low	–	1.0	–	0.5	μs
t_{RS1}	CB_2 Delay Time, Low-to-High	–	1.0	–	0.5	μs
t_{RS2}	CB_2 Delay Time, Handshake Mode	–	2.0	–	1.0	μs
t_{PDW}	Peripheral Port Delay Time	–	1.0	–	0.5	μs
t_{CMOS}	Peripheral Port Delay Time (CMOS)	–	2.0	–	1.0	μs
t_{DC}	CB_2 Delay Time from Data Valid	20	–	20	–	ns
P_{WI}	Interrupt Input Pulse Width	500	–	500	–	ns
t_{RS3}	Interrupt Response Time	–	1.0	–	1.0	μs
t_{IR}	Interrupt Clear Delay	–	1.6	–	0.85	μs
t_R, t_F	Rise and Fall Times – CA_1, CA_2, CB_1, CB_2	–	1.0	–	1.0	μs

Test Load



C = 130 pF MAX. FOR DB0-DB7
C = 30 pF MAX. FOR ALL OTHER OUTPUTS



OPEN COLLECTOR
OUTPUT TEST LOAD

Peripheral IC

Interface Signal Description

$\overline{RES}$ (Reset)

This signal is used to initialize the PIA. A low signal on the $\overline{RES}$ input causes all internal registers to be cleared.

ϕ_2 (Input Clock)

This input is the system ϕ_2 clock and is used to trigger all data transfers between the microprocessor and the PIA.

R/$\overline{W}$ (Read/Write)

This signal is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ signal permits the processor to read data supplied by the PIA; a low on the R/$\overline{W}$ signal permits the processor to Write into the PIA.

$\overline{IRQA}$, $\overline{IRQB}$ (Interrupt Requests)

$\overline{IRQA}$ and $\overline{IRQB}$ are interrupt lines generated by the PIA for ports A and B respectively. These signals are active low signals and have open-drain outputs, thus allowing multiple IRQ signals from multiple PIA's to be wire-ORed together before connecting to the processor IRO signal input.

D_0-D_7 (Data Bus)

These eight data bus lines are used to transfer data information between the processor and the PIA. These signals are bi-directional and are normally highimapedance except when selected for a read operation.

CS0, CS1, $\overline{CS2}$ (Chip Selects)

The PIA is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. These three chip select lines are normally connected to the processor address lines either directly or through external decoder circuits.

RS0, RS1 (Register Selects)

These two signals are used to select the various registers inside the PIA.

Internal Architecture

The UM6520 is organized into two independent sections referred to as the "A Side" and the "B Side." Each section consists of a Control Register (CRA, CRB), Data Direction Register (DDRA, DDRB), Output Register (ORA, ORB), Interrupt Status Control and the buffers necessary to drive the Peripheral Interface buses. Figure 12 is a block diagram of the UM6521.

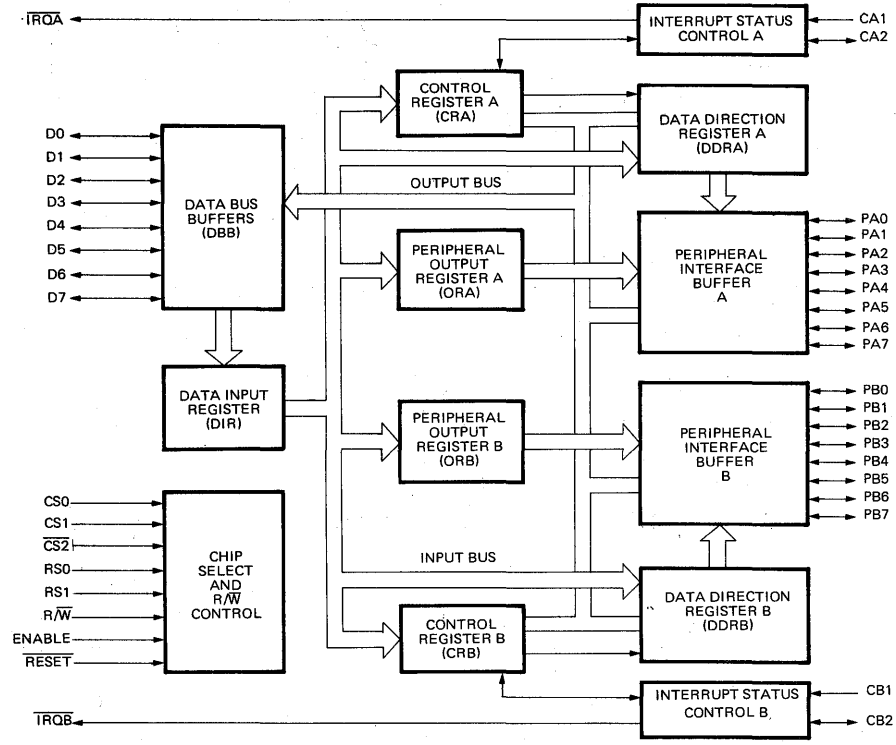


Figure 12. UM6521 Block Diagram

	7	6	5 4 3	2	1 0
CRA	IRQA1	IRQA2	CA2 Control	DDRA Access	CA1 Control
	7	6	5 4 3	2	1 0
CRB	IRQB1	IRQB2	CB2 Control	DDRB Access	CB1 Control

Figure 13. Control Registers

Data Input Register

When the microprocessor writes data into the Um6521, the data which appears on the data bus during the Phase Two clock pulse is latched into the Data Input Register. It is then transferred into one of six internal registers of the UM6521 after the trailing edge of Phase Two. This assures that the data on the peripheral output lines will make smooth transitions from high to low or from low to high and the voltage will remain stable except when it is going to the opposite polarity.

Control Registers (CRA and CRB)

Figure 4 illustrates the bit designation and functions in the Control Registers. The Control Registers allow the microprocessor to control the operation of the Interrupt Control inputs (CA1, CA2, CB1, CB2), and Peripheral Control outputs (CA2, CB2). Bit 2 in each register controls the addressing of the Data Direction Registers (DDRA, DDRB) and the Output Registers (ORA, ORB). In addition, two bits (bit 6 and 7) are provided in each control register to indicate the status of the interrupt input lines (CA1, CA2, CB1, CB2). These interrupt status bits (IRQA1, (IRQB1) are normally interrogated by the microprocessor during the interrupt service routine to determine the source of an active interrupt. These are the interrupt lines which drive the interrupt input ($\overline{IRQ}$, $\overline{NMI}$) of the microprocessor.

Data Direction Registers (DDRA, DDRB)

The Data Direction Registers allow the processor to program each line in the 8-bit Peripheral I/O port to be either an input or an output. Each bit in DDRA controls the corresponding line in the Peripheral A port and each bit in DDRB controls the corresponding line in the Peripheral B port. Placing a "0" in a bit position in the Data Direction Register causes the corresponding Peripheral I/O line to act as an input; a "1" causes it to act as an output.

Peripheral Output Registers (ORA, ORB)

The Peripheral Output Registers store the output data which appears on the Peripheral I/O port. Writing a "0" into a bit in ORA causes the corresponding line on the Peripheral A port to go low ($\leq$ 0.4V) if that line is programmed to act as an output. A "1" causes the corresponding output to go high. The lines of the Peripheral B port are controlled by ORB in the same manner.

Interrupt Status Control

The four interrupt/peripheral control lines (CA1, CA2, CB1, CB2) are controlled by the Interrupt Status Control logic (A, B). This logic interprets the contents of the corresponding Control Register, detects active transitions on the interrupt inputs and performs those operations necessary to assure proper operation of these four peripheral interface lines.

Peripheral Interface Buffers (A, B) and Data Bus Buffers (DBB)

These Buffers provide the necessary current and voltage drive on the peripheral I/O ports and data bus to assure proper system operation and to meet the device specifications.

Functional Description

Bit 2 (DDR) in each Control Register (CRA and CRB) controls the accessing to the Data Direction Register or the Peripheral interface. If bit 2 is a "1", a Peripheral Output register (ORA, ORB) is selepted, and if bit 2 is a "0", a Data Direction Register (DDRA, DDRB) is selected. The Data Direction Register Access Control bit, together with the Register Select lines (RS0, SR1) selects the various internal registers as shown in Figure 14.

In order to write data into DDRA, ORA, DDRB, or ORB registers, bit 2 in the proper Control Register must first be set. The desired register may then be accessed with the address determined by the address interconnect technique used.

Register Select Lines (RS0), (RS1)

These two register select lines are used to select the various registers inside the UM6521. These input lines are used in conjunction with internal control registers to select a particular register that is to be accessed by the microprocessor. These lines are normally connected to microprocessor address output lines. These lines operate in conjunction with the chip-select inputs to allow the microprocessor to address a single 8-bit register within the microprocessor address space. This register may be an internal register (CRA, ORA, etc.) or it may be a Peripheral I/O port.

The processor may write directly into the Control Registers (CRA, CRB), the Data Direction Registers (DDRA, DDRB) and the Peripheral Output Registers (ORA, ORB). In addition, the processor may directly read the contents of the Control Registers and the Data Direction Registers. Accessing the Peripheral Output Register for the purpose of reading data back into the processor operates differently on the ORA and the ORB registers and therefore are discussed separately below.

Reading the Peripheral A I/O Port

The Peripheral A I/O port consists of 8 lines which can be programmed to act as inputs or outputs. When programmed to act as outputs, each line reflects the contents of the corresponding bit in the Peripheral Output Register. When programmed to act as inputs, these lines will go high or low depending on the input data. The Peripheral Output Register (ORA) has no effect on those lines programmed to act as inputs. The eight lines of the Peripheral A I/O port therefore contain either input or output data depending on whether the line is programmed to act as an input or an output. Performing a Read operation with RS1 = 0, RS0 = 0 and the Data Direction Register Access Control bit (CRA-2) = 1, directly transfers the data on the Peripheral A I/O lines into the processor (via the data bus). This will contain both the input and output data. The processor must be programmed to recognize and interpret only those bits which are important to the particular peripheral operation being performed.

Since the processor always reads the Peripheral A I/O port pins instead of the actual Peripheral Output Register (ORA), it is possible for the data read into the processor to differ from the contents of the Peripheral Output Register for an output line. This is true when the I/O pin is not allowed to go to a full +2.4V DC when the Peripheral Output register contains a logic 1. In this case, the processor will read a 0 from the Peripheral A pin, even though the corresponding bit in the Peripheral Output register is a 1.

Reading the Peripheral B I/O Port

Reading the Peripheral B I/O port yields a combination of input and output data in a manner similar to the Peripheral A port. However, data is read directly from the Peripheral B Output Register (ORB) for those lines programmed to act as outputs. It is therefore possible to load down the Peripheral B Output lines without causing incorrect data to be transferred back into the processor on a Read operation.

Interrupt Request Lines ($\overline{IRQA}$, $\overline{IRQB}$)

The active low Interrupt Request lines ($\overline{IRQA}$ and $\overline{IRQB}$) act to interrupt the microprocessor either directly or through external interrupt priority circuitry. These lines are "open drain" and are capable of sinking 1.6 milliamps from an external source. This permits all interrupt request lines to be tied together in a "wired-OR" configuration. The "A" and "B" in the titles of these lines correspond to the "A" peripheral port and the "B" peripheral port. Hence each interrupt request line services one peripheral data port.

Each Interrupt Request line has two interrupt flag bits

Register Select Pin		Data Direction Register Access Control Bit		Register Selected
RS1	RS0	CRA-2	CRB-2	
0	0	1	–	Peripheral Interface A
0	0	0	–	Data Direction Register A
0	1	–	–	Control Register A
1	0	–	1	Peripheral Interface B
1	0	–	0	Data Direction Register B
1	1	–	–	Control Register B

Figure 14. Register Addressing

which can cause the Interrupt Request line to go low. These flags are bits 6 and 7 in the two Control Registers. These flags act as the link between the peripheral interrupt signals and the microprocessor interrupt inputs. Each flag has a corresponding interrupt disable bit which allows the processor to enable or disable the interrupt from each of the four interrupt inputs (CA1, CA2, CB1, CB2).

The four interrupt flags are set by active transitions of the signal on the interrupt input (CA1, CA2, CB1, CB2).

Control of $\overline{IRQA}$

Control Register A bit 7 is always set by an active transition of the CA1 interrupt input signal. Interrupting from this flag can be disabled by setting bit 0 in the Control Register A (CRA) to a logic 0. Likewise, Control Register A bit 6 can be set by an active transition of the CA2 interrupt input signal. Interrupting from this flag can be disabled by setting bit 3 in the Control Register to a logic 0.

Both bit 6 and bit 7 in CRA are reset by a "Read Peripheral Output Register A" operation. This is defined as an operation in which the proper chip-select and register-select signals are provided to allow the processor to read the Peripheral A I/O port.

Control of $\overline{IRQB}$

Control of $\overline{IRQB}$ is performed in exactly the same manner as that described above for $\overline{IRQA}$. Bit 7 in CRB is set by an active transition on CB1; interrupting from this flag is controlled by CRB bit 0. Likewise, bit 6 in CRB is set by an active transition on CB2; interrupting from this flag is controlled by CRB bit 3.

Also, both bit 6 and bit 7 are reset by a "Read Peripheral B Output Register" operation.

SUMMARY:	
$\overline{IRQA}$ goes low	when CRA-7 = 1 and CRA-0 = 1 or when CRA-6 = 1 and CRA-3 = 1
$\overline{IRQB}$ goes low	when CRB-7 = 1 and CRB-0 = 1 or when CRB-6 = 1 and CRB-3 = 1

It should be stressed at this point that the flags act as the link between the peripheral interrupt signals and the processor interrupt inputs. The interrupt disable bits allow the processor to control the interrupt function.

Interface Between UM6521 and Peripheral Devices

The UM6521 provides two 8-bit bi-directional ports and 4 interrupt/control lines for interfacing to peripheral devices. These ports and the associated interrupt/control lines are referred to as the "A" side and the "B" side. Each side has its own unique characteristics and will therefore be discussed separately below.

Peripheral I/O Ports

The Peripheral A and Peripheral B I/O Ports allow the microprocessor to interface to the input lines on the peripheral device by loading data into the Peripheral Output Register. They also allow the processor to interface with the peripheral device output lines by reading the data on the Peripheral Port input lines directly onto the data bus and into the internal registers of the processor.

Peripheral A I/O Port (PA0-PA7)

Each of the Peripheral I/O lines can be programmed to act as an input or an output. This is accomplished by setting a "1" in the corresponding bit in the Data Direction Register for those lines which are to act as outputs. A "0" in a bit of the Data Direction Register causes the corresponding Peripheral I/O lines to act as an input.

The buffers which drive the Peripheral A I/O lines contain "passive" pull-ups as shown in Figure 15. These pull-up devices are resistive in nature and therefore allow the output voltage to go to V_{CC} for a logic 1. The switches can sink a full 1.6mA, making these buffers capable of driving one standard TTL load.

In the input mode, the pull-up devices shown in Figure 15 are still connected to the I/O pin and still supply current to this pin. For this reason, these lines represent one standard TTL load in the input mode.

Peripheral B I/O Port (PB0-PB7)

The Peripheral B I/O port duplicates many of the functions of the Peripheral A port. The process of programming these lines to act as an input or an output has been discussed previously. Likewise, the effect of reading or writing this port has been discussed. However, there are several characteristics of the buffers driving these lines which affect their use in peripheral interfacing.

The Peripheral B I/O port buffers are push-pull devices as shown in Figure 16. The pull-up devices are switched "OFF" in the "0" state and "ON" for a logic 1. Since

these pull-ups are active devices, the logic "1" voltage is not guaranteed to go higher than +2.4V. They are TTL compatible but are not CMOS compatible.

However, the active pull-up devices can source up to 1mA at 1.5V. This current drive capability is provided to allow direct connection to Darlington transistor switches. This allows very simple control of relays, lamps, etc.

Because these outputs are designed to drive transistors directly, the output data is read directly from the Peripheral Output Register for those lines programmed to act as inputs.

The final characteristic which is a function of the Peripheral B push-pull buffers is the high-impedance input state. When the Peripheral B I/O lines are programmed to act as inputs, the output buffer enters the high impedance state.

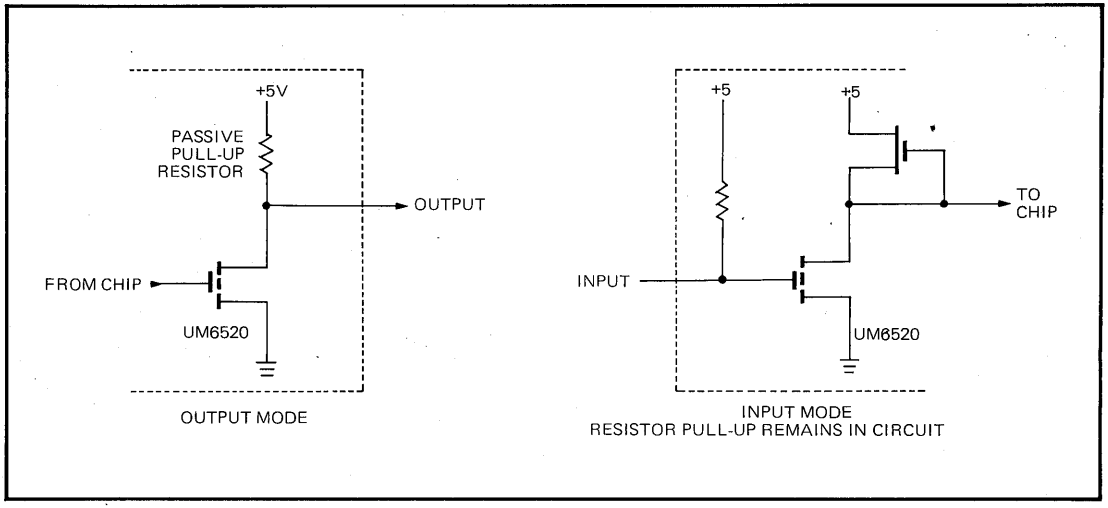


Figure 15. Port A Buffer Circuit (PA_0-PA_7)

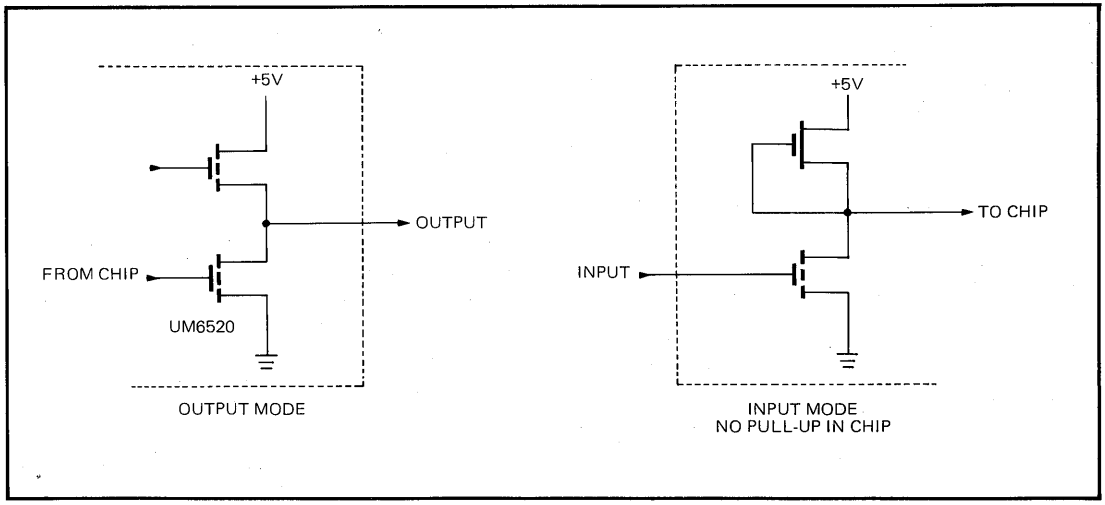


Figure 16. Port B Buffer Circuit (PB_0-PB_7)

Interrupt Input/Peripheral Control Lines (CA1, CA2, CB1, CB2)

The four interrupt input/peripheral control lines provide a number of special peripheral control functions. These lines greatly enhance the power of the two general purpose interface ports (PA0-PA7, PB0-PB7). Figure 17 summarizes the operation of these control lines.

Peripheral A Interrupt Input/Peripheral Control Lines (CA1, CA2)

CA1 is an interrupt input only. An active transition of the signal on this input will set bit 7 of the Control Register A to a logic 1. The active transition can be programmed by setting a "0" in bit 1 of the CRA if the interrupt flag (bit 7 of CRA) is to be set on a negative transition of the CA1 signal or a "1" if it is to be set on a positive transition.

NOTE: A negative transition is defined as a transition from a high to a low, and a positive transition is defined as a transition from a low to a high voltage.

Setting the interrupt flag will interrupt the processor through $\overline{IRQA}$ if bit 0 of CRA is a 1 as described previously.

CA2 can act as a totally independent interrupt input or as a peripheral control output. As an input (CRA, bit 5 = 0) it acts to set the interrupt flag, bit 6 of CRA, to a logic 1 on the active transition selected by bit 4 of CRA.

These control register bits and interrupt inputs serve the same basic function as that described above for CA1. The input signal sets the interrupt flag which serves as the link between the peripheral device and the processor interrupt structure. The interrupt disable bit allows the processor to exercise control over the system interrupts.

In the Output mode (CRA, bit 5 = 1), CA2 can operate independently to generate a simple pulse each time the microprocessor reads the data on the Peripheral A I/O port. This mode is selected by setting CRA, bit 4 to a "0" and CRA, bit 3 to a "1". This pulse output can be used to control the counters, shift registers, etc. which make sequential data available on the Peripheral input lines.

A second output model allows CA2 to be used in conjunction with CA1 to "handshake" between the processor and the peripheral device. On the A side, this technique allows positive control of data transfers from the peripheral device into the microprocessor. The CA1 input signals the processor that data is available by interrupting the processor. The processor reads the data and set CA2 low. This signals the peripheral device that it can make new data available.

The final output mode can be selected by setting bit 4 of CRA to a 1. In this mode, CA2 is a simple peripheral control output which can be set high or low by setting bit 3 of CRA to a 1 or a 0 respectively.

Peripheral B Interrupt Input/Peripheral Control Lines (CB1, CB2)

CB1 operates as an interrupt input only in the same manner as CA1. Bit 7 of CRB is set by the active transition selected by bit 0 of CRB. Likewise, the CB2 input mode operates exactly the same as the CA2 input modes. The CB2 output modes, CRB bit 5 = 1, differ somewhat from those of CA2. The pulse output occurs when the processor writes data into the Peripheral B Output Register. Also, the "handshaking" operates on data transfers from the processor into the peripheral device.

CA1/CB1 CONTROL

CRA (CRB)		Active Transition	IRQA (IRQB) Interrupt Outputs
Bit 1	Bit 0	of Input Signal*	
0	0	Negative	Disable – remain high
0	1	Negative	Enable – goes low when bit 7 in CRA (CRB) is set by active transition of signal on CA1 (CB1)
1	0	Positive	Disable – remain high
1	1	Positive	Enable – as explained above

*Note: Bit 7 of CRA (CRB) will be set to a logic 1 by an active transition of the CA1 (CB1) signal. This is independent of the state of Bit 0 in CRA (CRB).

CA2/CB2 INPUT MODES

CRA (CRB)			Active Transition of Input Signal*	IRQA (IRQB) Interrupt Outputs
Bit 5	Bit 4	Bit 3		
0	0	0	Negative	Disable – remains high
0	0	1	Negative	Enable – goes low when bit 6 in CRA (CRB) is set by active transition of signal on CA2 (CB2)
0	1	0	Positive	Disable – remains high
0	1	1	Positive	Enable – as explained above

*Note: Bit 6 of CRA (CRB) will be set to a logic 1 by an active transition of the CA2 (CB2) signal. This is independent of the state of Bit 3 in CRA (CRB).

CA2 OUTPUT MODES

CRA			Mode	Descriptions
Bit 5	Bit 4	Bit 3		
1	0	0	"Handshake" on Read	CA2 is set high on an active transition of the CA1 interrupt input signal and set low by a microprocessor "Read A Data" operation. This allows positive control of data transfers from the peripheral device to the microprocessor.
1	0	1	Pulse Output	CA2 goes low for one cycle after a "Read A Data" operation. This pulse can be used to signal the peripheral device that data was taken.
1	1	0	Manual Output	CA2 set low
1	1	1	Manual Output	CA2 set high

CB2 OUTPUT MODES

CRB			Mode	Descriptions
Bit 5	Bit 4	Bit 3		
1	0	0	"Handshake" on Write	CB2 is set low on microprocessor "Write B Data" operation and is set high by an active transition of the CB1 interrupt input signal. This allows positive control of data transfers from the microprocessor to the peripheral device.
1	0	1	Pulse Output	CB2 goes low for one cycle after a microprocessor "Write B Data" operation. This can be used to signal the peripheral device that data is available.
1	1	0	Manual Output	CB2 set low
1	1	1	Manual Output	CB2 set high

Figure 17. Summary of Operation of Control Lines

Ordering Information

Part Number	Speed	Package
UM6521	1 MHz	Plastic
UM6521A	2 MHz	Plastic

UM6522/UM6522A

Versatile Interface Adapter(VIA)

Features

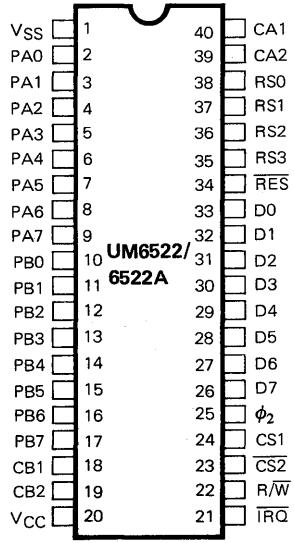
- Two 8-bit bidirectional I/O ports
- Two 16-bit programmable timer/counters
- Serial data port
- Single +5V power supply
- TTL compatible expect Port A
- CMOS compatible peripheral Port A lines
- Expanded "handshake" capability allows positive control of data transfers between processor and peripheral devices
- Latched output and input registers
- 1 MHz and 2 MHz operation

General Description

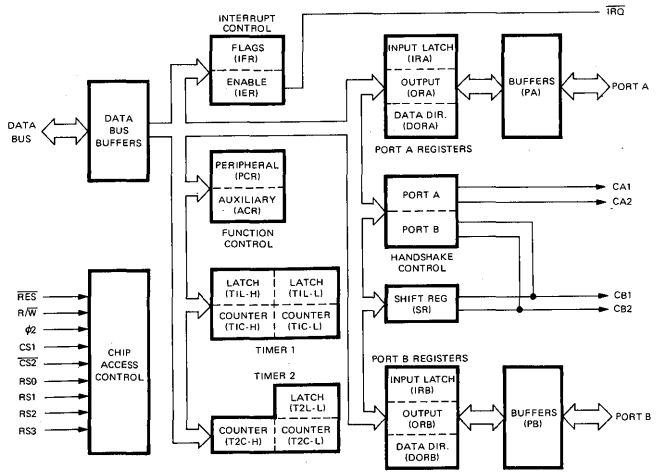
The UM6522 Versatile Interface Adapter (VIA) is a very flexible I/O control device. In addition, this device contains a pair of very powerful 16-bit interval timers, a serial-to-parallel/parallel-to-serial shift register and input data latching on the peripheral ports. Expanded handshaking capability allows control of bi-directional data transfers between VIA's in multiple processor systems.

Control of peripheral devices is handled primarily through two 8-bit bi-directional ports. Each line can be programmed as either an input or an output. Serveral peripheral I/O lines can be controlled directly from the interval timers for generating programmable frequency square waves or for counting externally generated pulses. To facilitate control of the many powerful features of this chip, an interrupt flag register, an interrupt enable register and a pair of function control registers are provided.

Pin Configuration



Block Diagram



Peripheral IC

Absolute Maximum Ratings*

Supply Voltage . . . . . +8.0 VOLTS
Operating Voltage Range . . . . . +4V to +7V
Input Voltage Applied . . . . . GND–2.0V to 6.5V
I/O Pin Voltage Applied . . . . . GND–0.5V to V_{CC} +0.5V
Storage Temperature Range . . . . . –65°C to +150°C
Operating Temperature Range . . . . . 0°C to +70°C
Maximum Power Dissipation . . . . . 1 Watt

*Comments

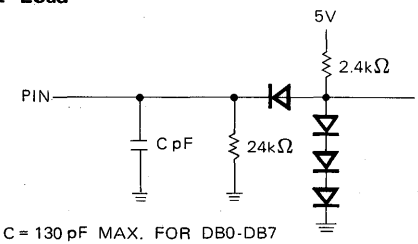
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

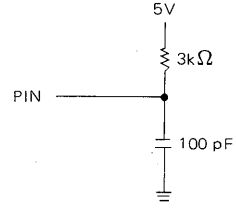
(V_{CC} = 5.0V ± 5%, T_A = 0 – 70°C unless otherwise noted)

Symbol	Characteristic	Min.	Max.	Units
V_{IH}	Input High Voltage (all except ϕ2)	2.4	V_{CC}	V
V_{CH}	Clock High Voltage	2.4	V_{CC}	V
V_{IL}	Input Low Voltage	–0.3	0.4	V
I_{IN}	Input Leakage Current – V_{IN} = 0 to 5 Vdc R/$\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, RS3, CS1, $\overline{CS2}$, CA1, ϕ2	–	±2.5	μA
I_{TSI}	Off-state Input Current – V_{IN} = 0.4 to 2.4V V_{CC} = Max, D0 to D7	–	±10	μA
I_{IH}	Input High Current – V_{IH} = 2.4V PA0–PA7, CA2, PB0–PB7, CB1, CB2	–100	–	μA
I_{IL}	Input Low Current – V_{IL} = 0.4 Vdc PA0–PA7, CA2, PB0–PB7, CB1, CB2	–	–1.6	mA
V_{OH}	Output High Voltage V_{CC} = min, I_{load} = –100 μAdc PA0–PA7, CA2, PB0–PB7, CB1, CB2	2.4	–	V
V_{OL}	Output Low Voltage V_{CC} = min, I_{load} = 1.6 mAdc	–	0.4	V
I_{OH}	Output High Current (Sourcing) V_{OH} = 2.4V V_{OH} = 1.5V (PB0–PB7)	 –100 –1.0	 – –	 μA mA
I_{OL}	Output Low Current (Sinking) V_{OL} = 0.4 Vdc	1.6	–	mA
I_{OFF}	Output Leakage Current (Off state) $\overline{IRQ}$	–	10	μA
C_{IN}	Input Capacitance – T_A = 25°C, f = 1 MHz (R/$\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, RS3, CS1, $\overline{CS2}$, D0–D7, PA0–PA7, CA1, CA2, PB0–PB7) (CB1, CB2) (ϕ2 Input)	 – – –	 7.0 10 20	 pF pF pF
C_{OUT}	Output Capacitance – T_A = 25°C, f = 1 MHz	–	10	pF
P_D	Power Dissipation (V_{CC} = 5.25V)	–	700	mW

Test Load



C = 130 pF MAX. FOR DB0-DB7
C = 30 pF MAX. FOR ALL OTHER OUTPUTS



OPEN COLLECTOR
OUTPUT TEST LOAD

Figure 2. Test Load (for all Dynamic Parameters)

Read Timing Characteristics (Figure 3.)

Symbol	Parameter	UM6522		UM6522A		Units
		Min.	Max.	Min.	Max.	
T_{CY}	Cycle Time	1	50	0.5	50	μs
T_{ACR}	Address Set-Up Time	180	–	90	–	ns
T_{CAR}	Address Hold Time	0	–	0	–	ns
T_{PCR}	Peripheral Data Set-Up Time	300	–	300	–	ns
T_{CDR}	Data Bus Delay Time	–	340	–	200	ns
T_{HR}	Data Bus Hold Time	10	–	10	–	ns

Note: tr, tf = 10 to 30ns.

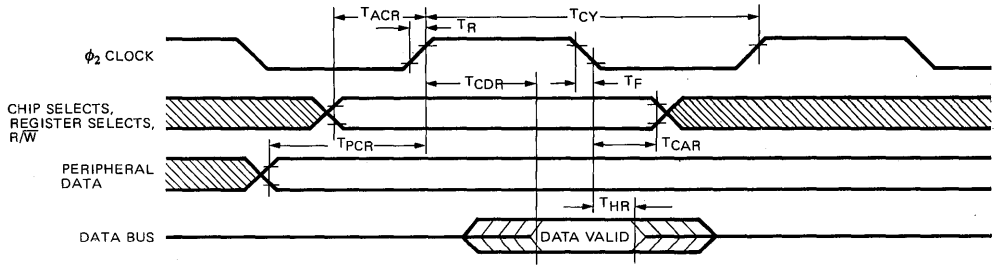


Figure 3. Read Timing Characteristics

Write Timing Characteristics (Figure 4.)

Symbol	Parameter	UM6522		UM6522A		Units
		Min.	Max.	Min.	Max.	
T_{CY}	Cycle Time	1	50	0.50	50	μs
T_C	φ2 Pulse Width	0.44	25	0.22	25	μs
T_{ACW}	Address Set-Up Time	180	–	90	–	ns
T_{CAW}	Address Hold Time	0	–	0	–	ns
T_{WGW}	R/$\overline{W}$ Set-Up Time	180	–	90	–	ns
T_{CWW}	R/$\overline{W}$ Hold Time	0	–	0	–	ns
T_{DCW}	Data Bus Set-Up Time	300	–	150	–	ns
T_{HW}	Data Bus Hold Time	10	–	10	–	ns
T_{CPW}	Peripheral Data Delay Time	–	1.0	–	1.0	μs
T_{CMOS}	Peripheral Data Delay Time to CMOS Levels	–	2.0	–	2.0	μs

Note: tr, tf = 10 to 30ns.

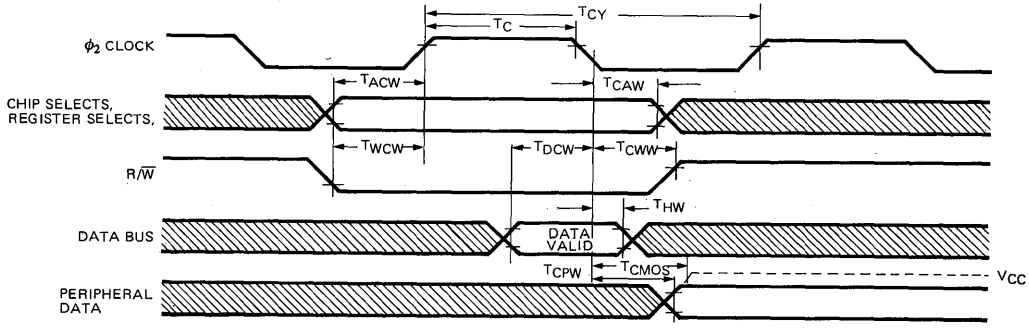


Figure 4. Write Timing Characteristics

Peripheral Interface Characteristics

Symbol	Characteristic	Min.	Max.	Typ.	Units	Figure
t_r, t_f	Rise and Fall Time for CA1, CB1, CA2, and CB2 Input Signals	–	1.0		μs	–
T_{CA2}	Delay Time, Clock Negative Transition to CA2 Negative Transition (read handshake or pulse mode)	–	1.0		μs	5a, 5b
T_{RS}	Delay Time, Clock Negative Transition to CA2 Positive Transition (pulse mode)	–	1.0		μs	5a
T_{RS2}	Delay Time, CA1 Active Transition to CA2 Positive Transition (handshake mode)	–	2.0		μs	5b
T_{WHS}	Delay Time, Clock Positive Transition to CA2 or CB2 Negative Transition (write handshake)	0.05	1.0		μs	5c, 5d
T_{DS}	Delay Time, Peripheral Data Valid to CB2 Negative Transition	0.20	1.5		μs	5c, 5d
T_{RS3}	Delay Time, Clock Transition to CA2 or CB2 Positive Transition (pulse mode)	–	1.0		μs	5c
T_{RS4}	Delay Time, CA1 or CB1 Active Transition to CA2 or CB2 Positive Transition (handshake mode)	–	2.0		μs	5d
T_{21}	Delay Time Required from CA2 Output to CA1 Active Transition (handshake mode)	400	–		ns	5d
T_{IL}	Set-up Time, Peripheral Data Valid to CA1 or CB1 Active Transition (input latching)	300	–		ns	5e
T_{SR1}	Shift-Out Delay Time – Time from ϕ_2 Falling Edge to CB2 Data Out	–	300		ns	5f
T_{SR2}	Shift-In Setup Time – Time from CB2 Data in to ϕ_2 Rising Edge	300	–		ns	5g
T_{SR3}	External Shift Clock (CB1) Setup Time Relative to ϕ_2 Trailing Edge	100	T_{CY}		ns	5g
T_{IPW}	Pulse Width – PB6 Input Pulse	2 x T_{CY}	–			5i
T_{ICW}	Pulse Width – CB1 Input Clock	2 x T_{CY}	–			5h
T_{IPS}	Pulse Spacing – PB6 Input Pulse	2 x T_{CY}	–			5i
T_{ICS}	Pulse Spacing – CB1 Input Pulse	2 x T_{CY}	–			5h
T_{AI}	CA1, CB1 Set Up Prior to Transition to Arm Latch	T_C + 50	–		ns	5h
T_{PDH}	Peripheral Data Hold After CA1, CB1 Transition	150	–		ns	5e
T_{PWI}	Set Up Required on CA1, CB1, CA2 or CB2 Prior to Triggering Edge	T_C + 50	–		ns	5j
T_{DPR} T_{DPL}	Shift Register Clock – Delay from ϕ_2 to CB1 Rising Edge to CB1 Falling Edge			200 125	ns ns	5k 5k

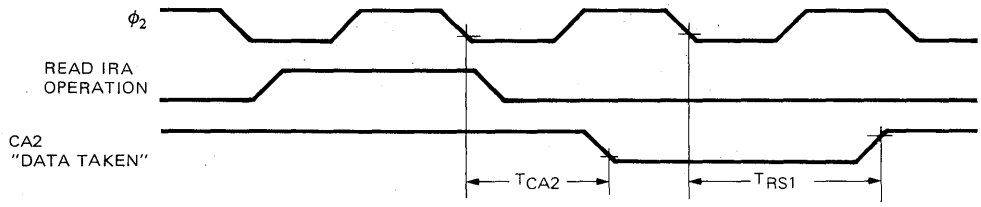


Figure 5a. CA2 Timing for Read Handshake, Pulse Mode

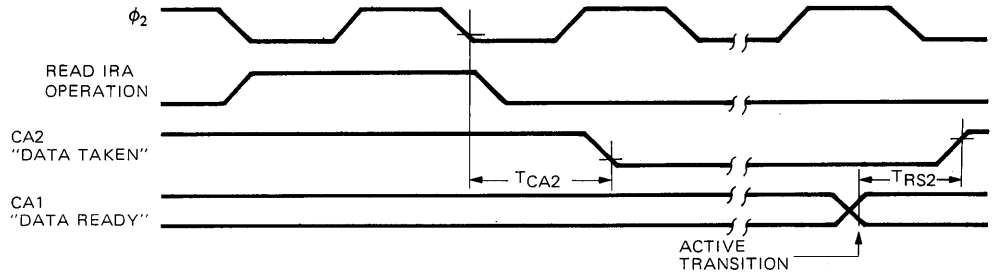


Figure 5b. CA2 Timing for Read Handshake, Handshake Mode

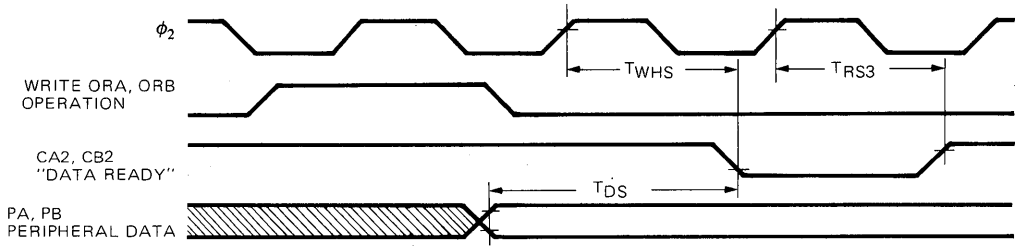


Figure 5c. CA2, CB2 Timing for Write Handshake, Pulse Mode

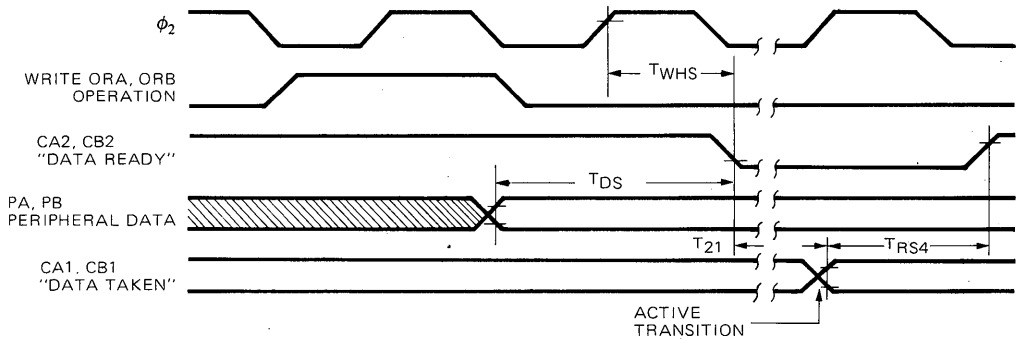


Figure 5d. CA2, CB2 Timing for Write Handshake, Handshake Mode

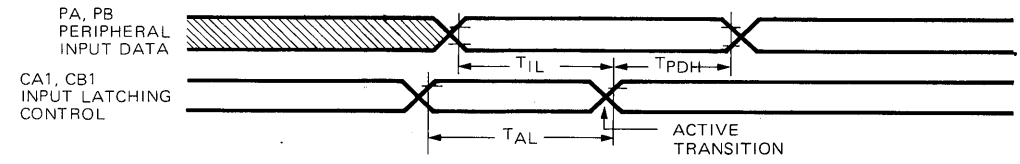


Figure 5e. Peripheral Data Input Latching Timing

Peripheral IC

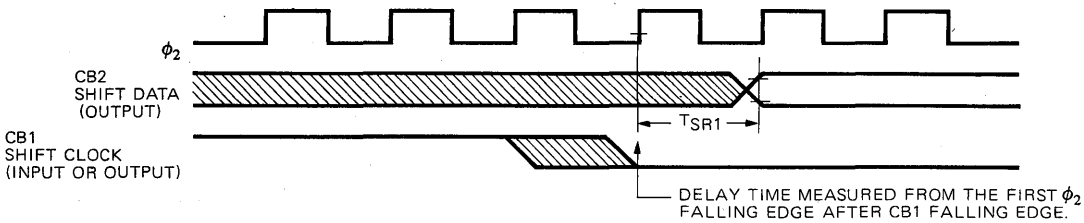


Figure 5f. Timing for Shift Out with Internal or External Shift Clocking

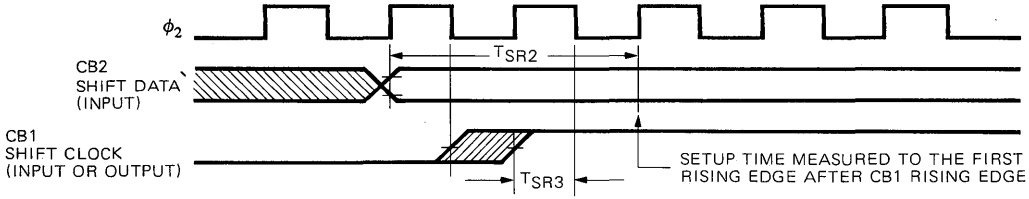


Figure 5g. Timing for Shift in with Internal or External Shift Clocking

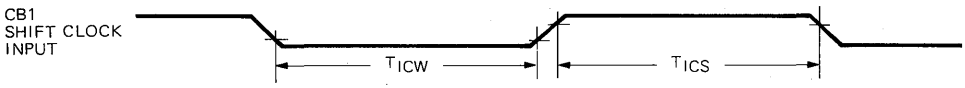


Figure 5h. External Shift Clocking

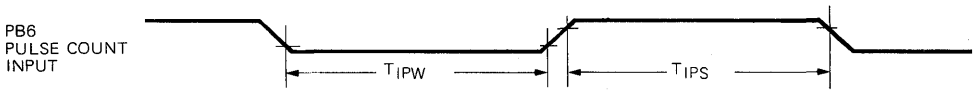


Figure 5i. Pulse Count Input Timing

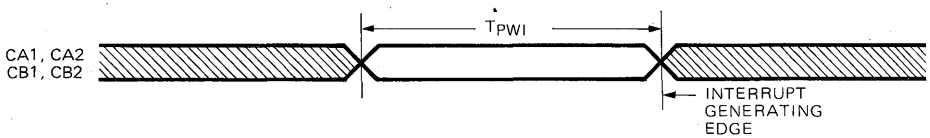


Figure 5j. Setup Time to Triggering Edge

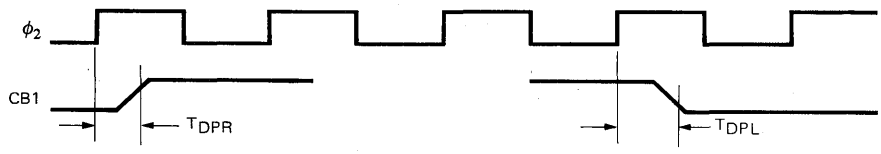


Figure 5k. Shift-in/out with Internal Clock Delay CD2 to CB1 Edge

Pin Description

$\overline{RES}$ (Reset)

The reset input clears all internal registers to logic 0 (except T1 and T2 latches and counters and the Shift Register). This places all peripheral interface lines in the input state, disables the timers, shift register, etc. and discables interrupting from the chip.

$\phi 2$ (Input Clock)

The input clock is the system $\phi 2$ clock and is used to trigger all data transfers between the system processor and the UM6522.

R/$\overline{W}$ (Read/Write)

The direction of the data transfers between the UM6522 and the system processor is controlled by the R/$\overline{W}$ line. If R/$\overline{W}$ is low, data will be transferred out of the processor into the selected UM6522 register (write operation). If R/$\overline{W}$ is high and the chip is selected, data will be transferred out of the UM6522 (read operation).

DB0-DB7 (Data Bus)

The eight bi-directional data bus lines are used to transfer data between the UM6522 and the system processor. During read cycles, the contents of the selected UM6522 register are placed on the data bus lines and transferred into the processor. During write cycles, these lines are high-impedance inputs and data is transferred from the processor into the selected register. When the UM6522 is unselected, the data bus lines are high-impedance.

CS1, $\overline{CS2}$ (Chip Selects)

The two chip select inputs are normally connected to processor address lines either directly or through decoding. The selected UM6522 register will be accessed when CS1 is high and $\overline{CS2}$ is low.

RS0-RS3 (Register Selects)

The four Register Select inputs permit the system processor to select one of the 16 internal registers of the UM6522, as shown in Figure 6.

$\overline{IRQ}$ (Interrupt Request)

The Interrupt Request output goes low whenever an internal interrupt flag is set and the corresponding interrupt enable bit is a logic 1. This output is "open-drain" to allow the interrupt request signal to be "wire-or'ed" with other equivalent signals in the system.

Register Number	RS Coding				Register Desig.	Descriptions	
	RS3	RS2	RS1	RS0		Write	Read
0	0	0	0	0	ORB/IRB	Output Register "B"	Input Register "B"
1	0	0	0	1	ORA/IRA	Output Register "A"	Input Register "A"
2	0	0	1	0	DDRB	Data Direction Register "B"	
3	0	0	1	1	DDRA	Data Direction Register "A"	
4	0	1	0	0	T1C-L	T1 Low-Order Latches	T1 Low-Order Counter
5	0	1	0	1	T1C-H	T1 High-Order Counter	
6	0	1	1	0	T1L-L	T1 Low-Order Latches	
7	0	1	1	1	T1L-H	T1 High-Order Latches	
8	1	0	0	0	T2C-L	T2 Low-Order Latches	T2 Low-Order Counter
9	1	0	0	1	T2C-H	T2 High-Order Counter	
10	1	0	1	0	SR	Shift Register	
11	1	0	1	1	ACR	Auxiliary Control Register	
12	1	1	0	0	PCR	Peripheral Control Register	
13	1	1	0	1	IFR	Interrupt Flag Register	
14	1	1	1	0	IER	Interrupt Enable Register	
15	1	1	1	1	ORA/IRA	Same as Reg 1 Except No. "Handshake"	

Figure 6. UM6522 Internal Register Summary

PA0-PA7 (Peripheral A Port)

The Peripheral A port consists of 8 lines which can be individually programmed to act as inputs or outputs under control of a Data Direction Register. The polarity of output pins is controlled by an Output Register and input data may be latched into an internal register under control of the CA1 line. All of these modes of operation are controlled by the system processor through the internal control registers. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. Figure 7 illustrates the output circuit.

CA1, CA2 (Peripheral A Control Lines)

The two Peripheral A control lines act as interrupt inputs or as handshake outputs. Each line controls an internal interrupt flag with a corresponding interrupt enable bit. In addition, CA1 controls the latching of data on Peripheral A port input lines. CA1 is a highimpedance input only; while CA2 represents one standard TTL load in the input mode. CA2 will drive one standard TTL load in the output mode.

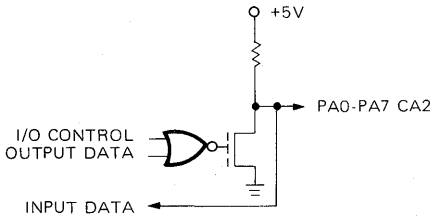


Figure 7. Peripheral A Port Output Circuit

PB0-PB7 (Peripheral B Port)

The Peripheral B port consists of eight bi-directional lines which are controlled by an output register and a data direction register in much the same manner as the PA port. In addition, the PB7 output signal can be controlled by one of the interval timers while the second timer can be programmed to count pulses on the PB6 pin. Peripheral B lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. In addition, they are capable of sourcing 1.0mA at 1.5VDC in the output mode to allow the outputs to directly drive Darlington transistor circuits. Figure 8 is the circuit schematic.

CB1, CB2 (Peripheral B Control Lines)

The Peripheral B control lines act as interrupt inputs or as handshake outputs. As with CA1 andCA2, each line controls an interrupt flag with a corresponding interrupt enable bit. In addition, these lines act as a serial port under control of the Shift Register. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. Unlike PB0-PB7. CB1 and CB2 cannot drive Darlington transistor circuits.

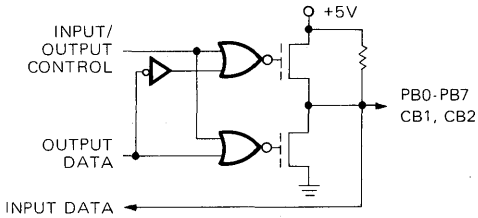


Figure 8. Peripheral B Port Output Circuit

Functional Description

Port A and Port B Operation

Each 8-bit peripheral port has a Data Direction Register (DDRA, DDRB) for specifying whether the peripheral pins are to act as inputs or outputs. A 0 in a bit of the Data Direction Register causes the corresponding peripheral pin to act as an input. A 1 causes the pin to act as an output.

When programmed as an output each peripheral pin is also controlled by a corresponding bit in the Output Register (ORA' ORB). A 1 in the Output Register causes the output to go high, and a "0" causes the output to go low. Data may be written into Output Register bits corresponding to pins which are programmed as inputs. In this case, however, the output signal is unaffected.

Reading a peripheral port causes the contrents of the Input Register (IRA, IRB) to be transferred onto the Data Bus. With input latching disabled, IRA will always reflect the levels on the PA pins. With input latching enabled and the selected active transition on CA1 having occurred, IRA will contain the data present on the PA lines at the time of the transition. Once IRA is read, however, it will appear transparent, reflecting the current state of the PA lines until the next "latching" transition.

The IRB register operates similar to the IRA register. However, for pins programmed as outputs there is a difference. When reading IRA, the level on the pin determines whether a 0 or a 1 is sensed. When reading IRB, however, the bit stored in the output register, ORB, is the bit sensed. Thus, for outputs which have large loading effects and which pull an output "1" down or which pull an output "0" up, reading IRA may result in reading a "0" when a "1" was actually programmed, and reading a "1" when a "0" was programmed. Reading IRB, on the other hand, will read the "1" or "0" level actually programmed, no matter what the loading on the pin.

Figures 9, 10 and 11 illustrate the formats of the port registers. In addition, the input latching modes are selected by the Auxiliary Control Register (Figure 16.)

Handshake Control of Data Transfers

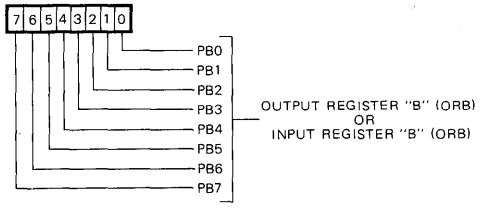
The UM6522 allows positive control of data transfers between the system processor and peripheral devices through the operation of "handshake" lines. Port A lines (CA1, CA2) handshake data on both a read and a write operation while the Port B lines (CB1, CB2) handshake on a write operation only.

Read Handshake

Positive control of data transfers from peripheral devices into the system processor can be accomplished very effectively using Read Handshaking. In this case, the peripheral device must generate the equivalent of a "Data Ready" signal to the processor signifying that valid data is present on the peripheral port. This signal normally interrupts the processor, which then reads the data, causing generation of a "Data Taken" signal. The peripheral device responds by making new data available. This process continues until the data transfer is complete.

In the UM6522, automatic "Read" Handshaking is possible on the Peripheral A port only. The CA1 interrupt input pin accepts the "Data Ready" signal and CA2 generates the "Data Taken" signal. The "Data Ready" signal will set an internal flag which may interrupt the processor or which may be polled under program control. The "Data Taken" Signal can either be a pulse or a level which is set low by the system processor and is cleared by the "Data Ready" signal. These options are shown in Figure 12 which illustrates the normal Read Handshaking sequence.

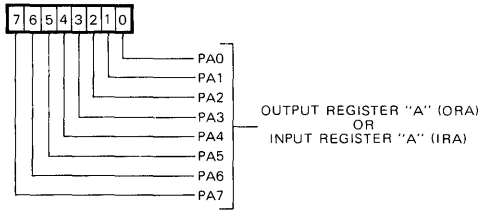
REG 0 – ORB/IRB



Pin Data Direction Selection	Write	Read
DDRB="1" (OUTPUT)	MPU writes Output Level (ORB)	MPU reads output register but in ORB. Pin Level has no affect.
DDRB="0" (INPUT) (Input latching disabled)	MPU writes inot ORB but no effect	MPU reads input level on PB Pin.
DDRB="0" (INPUT) (Input Latching enabled)	On Pin Level until DDRB changed	MPU reads IRB bit, which is the level of the PB pin at the time of the last CB1 active transition.

Figure 9. Output Register B (ORB), Input Register B (IRB)

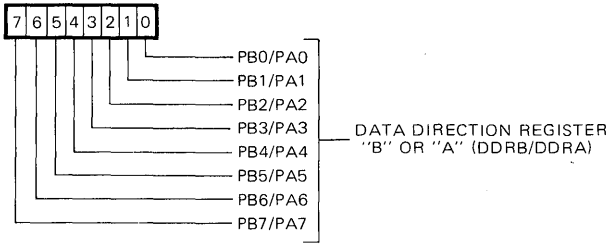
REG 1 – ORA/IRA



Pin Data Direction Selection	Write	Read
DDRA="1" (OUTPUT) (Input latching disabled)	MPU writes Output Level (ORA)	MPU reads level on PA pin.
DDRA="1" (OUTPUT) (Input 'atching enabled)		MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition.
DDRA="0" (INPUT) (Input latching disabled)	MPU writes into ORA, but no effect on pin level, until DDRA changed.	MPU reads level on PA pin.
DDRA="0" (INPUT) (Input latching enabled)		MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition.

Figure 10. Output Register A (ORA), Input Register A (IRA)

REG 2 (DDRB) AND REG 3 (DDRA)



"0" ASSOCIATED PB/PA PIN IS AN INPUT (HIGH–IMPEDANCE)

"1" ASSOCIATED PB/PA PIN IS AN OUTPUT, WHOSE LEVEL IS DETERMINED BY ORB/ORA REGISTER BIT

Figure 11. Data Direction Registers (DDRB, DDRA)

Write Handshake

The sequence of operations which allows handshaking data from the system processor to a peripheral device is very similar to that described for Read Handshaking. However, for Write Handshaking, the UM6522 generates the "Data

Ready" signal and the peripheral device must respond with the "Data Taken" signal. This can be accomplished on both the PA port and the PB port on the UM6522. CA2 or CB2 act as a "Data Ready" output in either the handshake mode or pulse mode and CA1 or CB1 accept the "Data Taken" signal from the peripheral device, setting the interrupt flag and cleaning the "Data Ready" output. This sequence is shown in Figure 13.

Selection of operating modes for CA1, CA2, CB1, and CB2 is accomplished by the Peripheral Control Register (Figure 14).

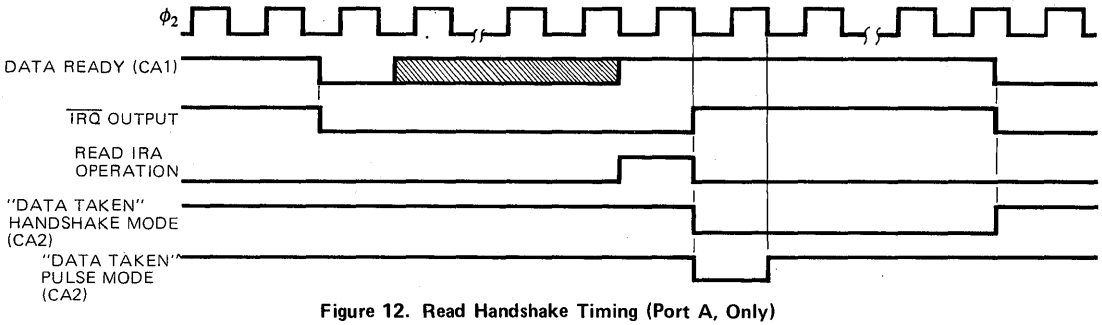


Figure 12. Read Handshake Timing (Port A, Only)

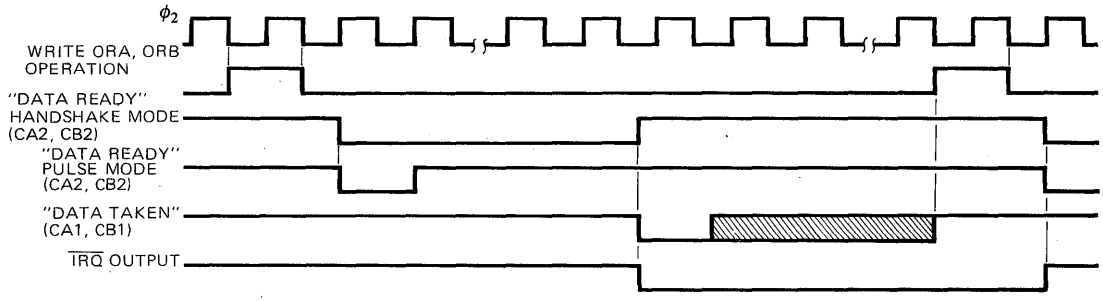


Figure 13. Write Handshake Timing

REG 12 – PERIPHERAL CONTROL REGISTER

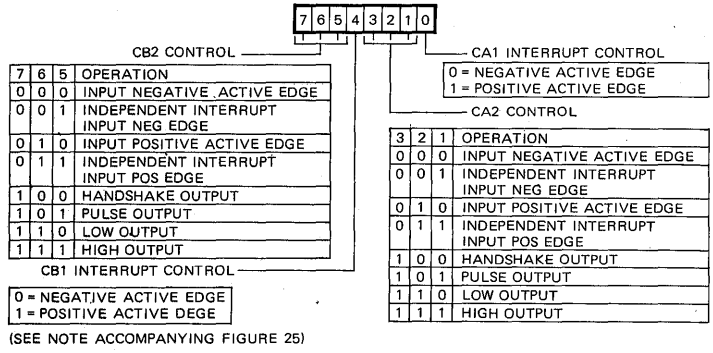


Figure 14. CA1, CA2, CB1, CB2 Control

Timer Operation

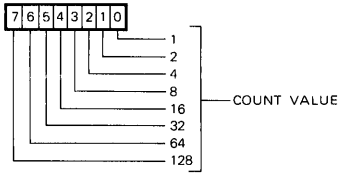
Interval Timer T1 consists of two 8-Bit latches and a 16-bit counter. The latches are used to store data which is to be loaded into the counter. After loading, the counter decrements at $\phi 2$ clock rate. Upon reaching zero, an interrupt flag will be set, and IRQ will go low if the interrupt is enabled. The timer will then disable any further interrupts, or (when programmed to) will automatically transfer the contents of the latches into the counter and begin to decrement again. In addition, the timer may be programmed to invert the output signal on a peripheral pin

each time it "times-out". Each of these modes in discussed separately below.

The T1 counter is depicted in Figure 15 and the latches in Figure 16.

Two bits are provide in the Auxiliary Control Register (bits 6 and 7) to allow selection f the T1 operating modes. The four possible modes are depicted in Figure 17.

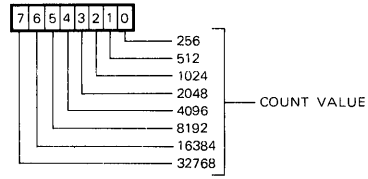
Reg 4 — Timer 1 Low-Order Counter



WRITE — 8 BITS LOADED INTO T1 LOW-ORDER LATCHES. LATCH CONTENTS ARE TRANSFERRED INTO LOW ORDER COUNTER AT THE TIME THE HIGH ORDER COUNTER IS LOADED (RFG 5).

READ — 8 BITS FROM T1 LOW-ORDER COUNTER TRANSFERRED TO MPU. IN ADDITION, T1 INTERRUPT FLAG IS RESET (BIT 6 IN INTERRUPT FLAG REGISTER).

Reg 5 — Timer 1 High-Order Counter

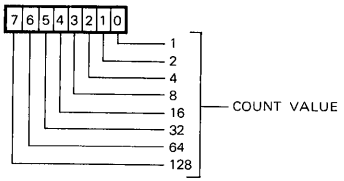


WRITE — 8 BITS LOADED INTO T1 HIGH-ORDER LATCHES. ALSO, AT THIS TIME BOTH HIGH AND LOW-ORDER LATCHES TRANSFERRED INTO T1 COUNTER, AND INITIATES COUNTDOWN. T1 INTERRUPT FLAG ALSO IS RESET.

READ — 8 BITS FROM T1 HIGH-ORDER COUNTER TRANSFERRED TO MPU.

Figure 15. T1 Counter Registers

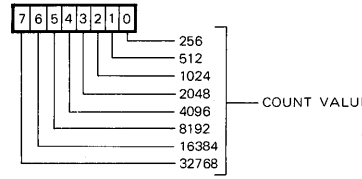
Reg 6 — Timer 1 Low-Order Latches



WRITE — 8 BIT LOADED INTO T1 LOW-ORDER LATCHES. THIS OPERATION IS NO DIFFERENT THAT A WRITE INTO REG 4.

READ — 8 BITS FROM T1 LOW-ORDER LATCHES TRANSFERRED TO MPU. UNLIKE REG 4 OPERATION, THIS DOES NOT CAUSE RESET OF T1 INTERRUPT FLAG.

Reg 7 — Timer 1 High-Order Latches

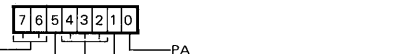


WRITE — 8 BITS LOADED INTO T1 HIGH-ORDER LATCHES. UNLIKE REG 4 OPERATION NO LATCH-TO-COUNTER TRANSFERS TAKE PLACE.

READ — 8 BITS FROM T1 HIGH-ORDERLATCHES TRANSFERRED TO MPU.

Figure 16. T1 Latch Registers

Reg 11 — Auxiliary Control Register



7	6	OPERATION	PB7
0	0	TIMED INTERRUPT EACH TIME T1 IS LOADED	DISABLED
0	1	CONTINUOUS INTERRUPTS	
1	0	TIMED INTERRUPT EACH TIME T1 IS LOADED	ONE-SHOT OUTPUT
1	1	CONTINUOUS INTERRUPTS	SQUARE WAVE OUTPUT

5	OPERATION
0	TIMED INTERRUPT
1	COUNT DOWN WITH PULSES ON PB6

4	3	2	OPERATION
0	0	0	DISABLED
0	0	1	SHIFT IN UNDER CONTROL OF T2
0	1	0	SHIFT IN UNDER CONTROL OF $\phi 2$
0	1	1	SHIFT IN UNDER CONTROL OF EXT CLK
1	0	0	SHIFT OUT FREE RUNNING AT T2 RATE
1	0	1	SHIFT OUT UNDER CONTROL OF T2
1	1	0	SHIFT OUT UNDER CONTROL OF $\phi 2$
1	1	1	SHIFT OUT UNDER CONTROL OF EXT CLK

Figure 17. Auxiliary Control Register

Note: The processor does not write directly into the low order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low order latch when the processor writes into the high order counter. In fact, it may not be necessary to write to the low order counter in some applications since the timing operation is triggered by writing to th high order counter.

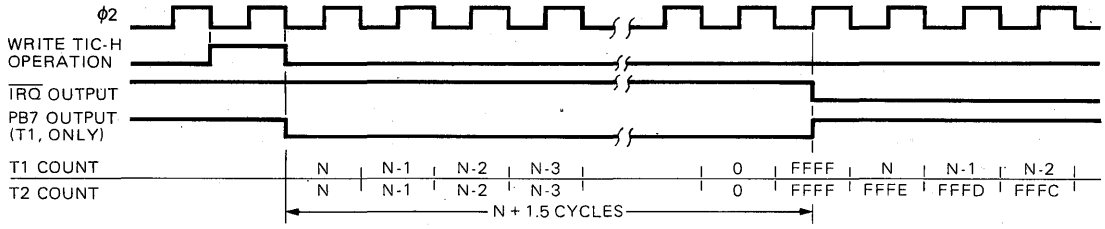


Figure 18. Timer 1 and Timer 2 One-Shot Mode Timing

Timer 1 One-Shot Mode

The interval timer one-shot mode allows generation of a single interrupt for each Timer load operation. In addition, Timer 1 can be programmed to produce a single negative pulse on PB7.

To generate a single interrupt ACR bits 6 and 7 must be 0 then either TIL-L or TIC-L must be written with the low-order count value. (A write to TIC-L is effectively a Write to TIL-L). Next the high-order count value is written to TIC-H, (the value is simultaneously written into TIL-H), and TIL-L is transferred to TIC-L. Countdown begins on the $\phi 2$ following the write TIC-H and decrements at the $\phi 2$ rate. T1 interrupt occurs when the counters reach 0. Generation of a negative pulse on PB7 is done in the same manner except ACR bit 7 must be a one. PB7 will go low after a Write TIC-H and go high again when the counters reach 0.

The T1 interrupt flag is reset by either writing TIC-H (starting a new count) or by reading TIC-L.

Timing for the one-shot mode is illustrated in Figure 18.

Timer 1 Free-Run Mode

The most important advantage associated with the latches in T1 is the ability to produce a continuous series of evenly spaced interrupts and the ability to produce a square wave on PB7 whose frequency is not affected by variations in the processor interrupt response time. This is accomplished in the "free-running" mode.

In the free-running mode, the interrupt flag is set and the signal on PB7 is inverted each time the counter reaches zero. However, instead of continuing to decrement from zero after a time-out, the timer automatically transfers the contents of the latch into the counter (16 bits) and continues to decrement from there. It is not necessary to rewrite the timer to enable setting the interrupt flag on the next time-out. The interrupt flag can be cleared by reading TIC-L, by writing directly into the flag as described later, or if a new count value is desired by a write to TIC-H.

All interval timers in the UM6522 are "re-triggerable". Rewriting the counter will always re-initialize the time-out period. In fact, the time-out can be prevented completely if the processor continues to rewrite the timer before it reaches zero. Timer 1 will operate in this manner if the processor writes into the high order counter (T1C-H). However, by loading the latches only, the processor can access the timer during each down-counting operation without affecting the time-out in process. Instead, the data loaded into the latches will determine the length of the next time-out period. This capability is particularly valuable in the free-running mode with the output enabled. In this mode, the signal on PB7 is inverted and the interrupt flag is set with each time-out. By responding to the interrupts with new data for the latches, the processor can determine the period of the next half cycle during each half cycle of the output signal on PB7. In this manner, very complex waveforms can be generated. Timing for the free-running mode is shown in Figure 19.

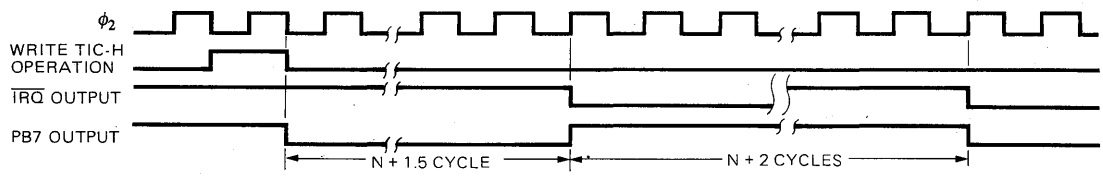


Figure 19. Timer 1 Free-Run Mode Timing

Note: A precaution to take in the use of PB7 as the timer output concerns the data direction Register contents for PB7. Both DDRB bit 7 and ACR bit 7 must be 1 for PB7 to function as the timer output. If either is a 0, then PB7 functions as a normal output pin, controlled by ORB bit 7.

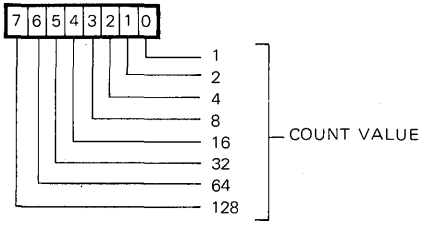
Timer 2 Operation

Timer 2 operates as an interval timer (in the "one-slot" mode only), or as a counter for counting negative pulses on the PB6 peripheral pin. A single control bit is provided in the Auxiliary Control Register to select between these two modes. This timer is comprised of a "write-only" low-order latch (T2L-L), a "read-only" low-order counter and a read/write high order counter. The counter registers act as a 16-bit counter which decrements at $\phi 2$ rate. Figure 20 illustrates the T2 Counter Registers.

Timer 2 One-Shot Mode

As an interval timer, T2 operates in the "one-shot" mode similar to Timer 1. In this mode, T2 provides a signle interrupt for each "write T2C-H" operation. After timing out, (reading 0) the counters "roll-over" to all 1's ($FFFF_{16}$) and continue decrementing, allowing the user to read them and determine how long T2 interrupt has been set. However, setting of the interrupt flag will be disabled after initial time-out so that it will not be set by the counter continuing to decrement through zero. The processor must rewrite T2C-H to enable setting of the interrupt flag. The interrupt flag is cleared by reading T2C-L or by writing T2C-H. Timing for this operation is shown in Figure 18.

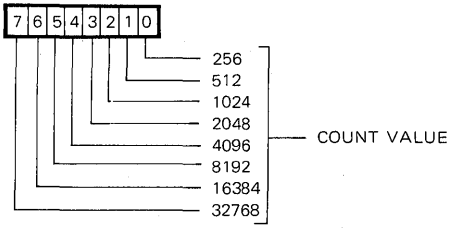
Reg 8 – Timer 2 Low-Order Counter



WRITE – 8 BITS LOADED INTO T2 LOW-ORDERLATCHES.

READ – 8 BITS FROM T2 LOW-ORDER COUNTER TRANSFERRED TO MPU. T2 INTERRUPT FLAG IS RESET.

Reg 9 – Timer 2 High-Order Counter



WRITE – 8 BITS LOADED INTO T2 HIGH-ORDER COUNTER. ALSO, LOW-ORDER LATCHES TRANSFERRED TO LOW-ORDER COUNTER, IN ADDITION, T2 INTERRUPT FLAG IS RESET.

READ – 8 BIT FROM T2 HIGH-ORDER COUNTER TRANSFERRED TO MPU.

Figure 20. T2 Counter Registers

Timer 2 Pulse Counting Mode

In the pulse counting mode, T2 serves primarily to count a predetermined number of negative-going pulses on PB6. This is accomplished by first loading a number into T2. Writing into T2C-H clears the interrupt flag and allows the counter to decrement each time a pulse is applied to PB6. The interrupt flag will be set when T2 reaches zero. At this time the counter will continue to decrement with each pulse on PB6. However, it is necessary to rewrite T2C-H to allow the interrupt flag to set on subsequent down-counting operations. Timing for this mode is shown in Figure 21. The pulse must be low on the leading edge of $\phi 2$.

Shift Register Operation

The Shift Register (SR) performs serial data transfers into and out of the CB2 pin under control of an internal modulo-8 counter. Shift pulses can be applied to the CB1 pin from an external source or, with the proper mode selection, shift pulses generated internally will appear on the CB1 pin for controlling external devices.

The control bits which select the various shift register operating modes are located in the Auxiliary Control Register. Figure 22 illustrates the configuration of the SR data bits and the SR control bits of the ACR.

Figures 23 and 24 illustrate the operation of the various shift register modes.

Interrupt Operation

Controlling interrupts within the UM6522 involves three principal operations. These are flagging the interrupts, enabling interrupts and signaling to the processor that an active interrupt exists within the chip. Interrupt flags are set by interrupting conditions which exist within the chip or on inputs to the chip. These flags normally remain set until the interrupt has been serviced. To determine the source of an interrupt, the microprocessor must examine these flags in order from highest to lowest priority. This is accomplished by reading the flag register into the processor accumulator, shifting this register either right or left and then using conditional branch instructions to detect an active interrupt.

Associated with each interrupt flag is an interrupt enable bit. This can be set or cleared by the processor to enable interrupting the processor from the corresponding interrupt flag. If an interrupt flag is set to a logic 1 by an interrupting condition, and the corresponding interrupt enable bit is set to a 1, the Interrupt Request Output ($\overline{IRQ}$) will go low. $\overline{IRQ}$ is an "open-collector" output which can be "wire-or'ed" with other devices in the system to interrupt the processor.

In the UM6522, all the interrupt flags are contained in one register. In addition, bit 7 of this register will be read as a logic 1 when an interrupt exists within the chip. This allows very convenient polling of serveral devices within a system to locate the source of an interrupt.

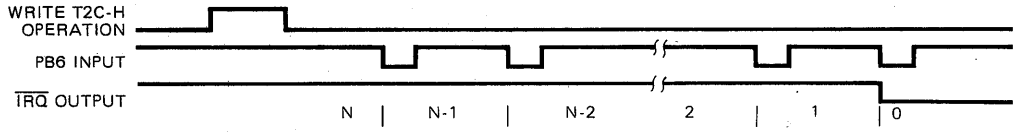
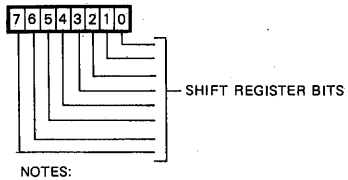


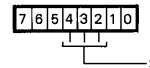
Figure 21. Timer 2 Pulse Counting Mode

Reg 10 — H Reg 10 — Shift Register



NOTES:
1. WHEN SHIFTING OUT. BIT 7 IS THE FIRST BIT OUT AND SIMUL TANEOUSLY IS ROTATED BACK INTO BIT 0.
2. WHEN SHIFTING IN, BITS INITIALLY ENTER BIT 0 AND ARE SHIFTED TOWARDS BIT 7.

Reg 11 — Auxiliary Control Register



4	3	2	OPERATION
0	0	0	DIABLED
0	0	1	SHIFT IN UNDER CONTROL OF T2
0	1	0	SHIFT IN UNDER CONTROL OF $\phi 2$
0	1	1	SHIFT IN UNDER CONTROL OF EXT CLK
1	0	0	SHIFT OUT RREE-RUNNING AT T2 RATE
1	0	1	SHIFT OUT UNDER CONTROL OF T2
1	1	0	SHIFT OUT UNDER CONTROL OF $\phi 2$
1	1	1	SHIFT OUT UNDER CONTROL OF EXT CLK

Figure 22. SR and ACR Control Bits

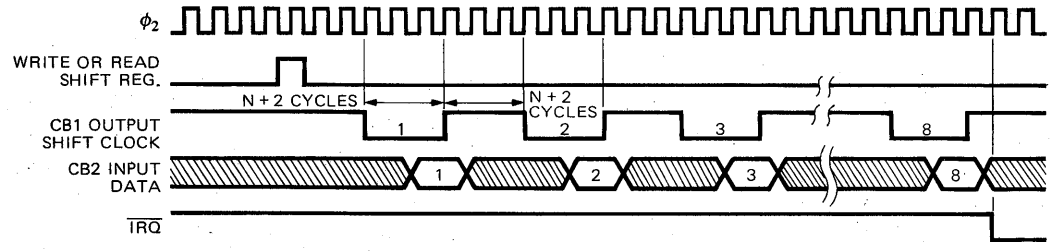
SR Disabled (000)

The 000 mode is used to disable the Shift Register. In this mode the microprocessor can write or read the SR, but the shifting operating is disabled and operation of CB1 and CB2 is controlled by the appropriate bits in the Peripheral Control Register (PCR). In this mode the SR Interrupt Flag is disabled (held to a logic 0).

Shift in Under Control of T2 (001)

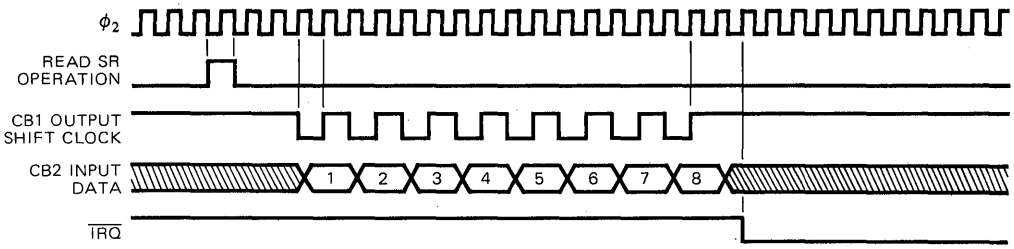
In the 001 mode the shifting rate is controlled by the low order 8 bits of T2. Shift pulses are generated on the CB1 Pin to control shifting in external devices. The time between transitions of this output clock is a function of the system clock period and the contents of the low order T2 latch (N).

The shifting operation is triggered by writing or reading the shift register. Data is shifted first into the low order bit of SR and is then shifted into the next higher order bit of the shift register on the negative-going edge of each clock pulse. The input data should change before the positive-going edge of the CB1 clock pulse. This data is shifted into the shift register during the $\phi 2$ clock cycle following the positive-going edge of the CB1 clock pulse. After 8 CB1 clock pulses, the shift register interrupt flag will be set and $\overline{IRQ}$ will go low.



Shift in Under Control of $\phi 2$ (010)

In mode 010 the shift rate is a direct function of the system clock frequency. CB1 becomes an output which generates shift pulses for controlling external devices. Timer 2 operates as an independent interval timer and has no effect on SR. The shifting operation is triggered by reading or writing the Shift Register. Data is shifted first into bit 0 and is then shifted into the next higher order bit of the shift register on the trailing edge of each $\phi 2$ clock pulse. After 8 clock pulses, the shift register interrupt flag will be set, and the output clock pulses on CB1 will stop.



Shift in Under Control of External CB1 Clock (011)

In mode 011 CB1 becomes an input. This allows an external device to load the shift register at its own pace. The shift register counter will interrupt the processor each time 8 bits have been shifted in. However, the shift register counter does not stop the shifting operation; it acts simply as a pulse counter. Reading or writing the Shift Register resets the Interrupt flag and initializes the SR counter to count another 8 puises.

Note that the data is shifted during the first system clock cycle following the positive-going edge of the CB1 shift pulse. For this reason, data must be held stable during the first full cycle following CB1 going high.

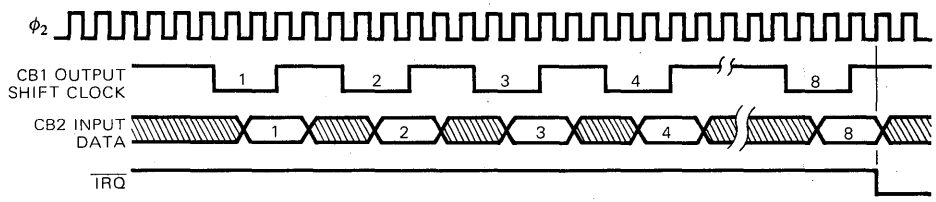
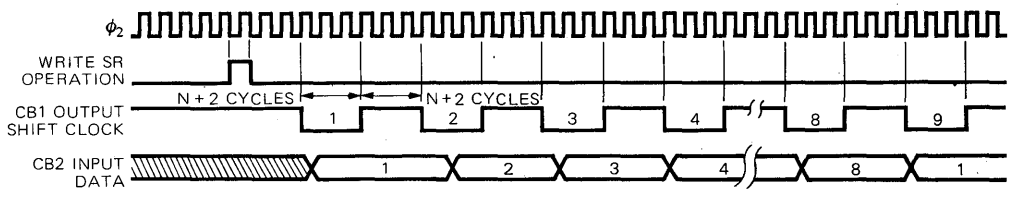


Figure 23. Shift Register Input Modes

Shift Out Free-Running at T2 Rate (100)

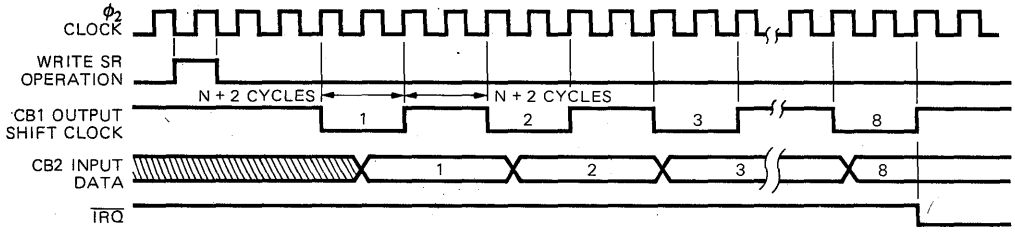
Mode 100 is very similar to mode 101 in which the shifting rate is set by T2. However, in mode 100 the SR Counter does not stop the shifting operation. Since the Shift Register bit 7 (SR7) is recirculated back into bit 0, the 8 bits loaded into the shift register will be clocked onto CR2 repetitively. In this mode the shift register counter is disabled, and $\overline{IRQ}$ is never set.



Peripheral IC

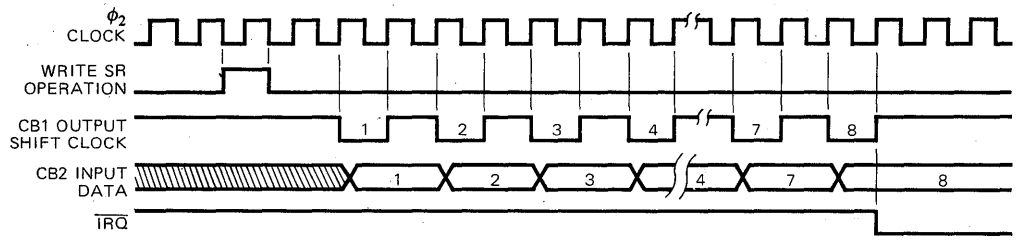
Shift Out Under Control of T2 (101)

In mode 101 the shift rate is controlled by T2 (as in the previous mode). However, with each read or write of the shift register the SR Counter is reset and 8 bits are shifted onto CB2. At the same time, 8 shift pulses are generated on CB1 to control shifting in external devices. After the 8 shift pulses, the shifting is disabled, the SR Interrupt Flag is set and CB2 remains at the last data level.



Shift Out Under Control of $\phi 2$ (110)

In mode 110, the shift rate is controlled by the $\phi 2$ system clock.



Shift Out Under Control of External CB1 Clock (111)

In mode 111 shifting is controlled by pulses applied to the CB1 pin by an external device. The SR counter sets the SR Interrupt flag each time it counts 8 pulses but it does not disable the shifting function. Each time the microprocessor writes or reads the shift register, the SR Interrupt flag is reset and the SR counter is initialized to begin counting the next 8 shift pulses on pin CB1. After 8 shift pulses, the interrupt flag is set. The microprocessor can then load the shift register with the next byte of data.

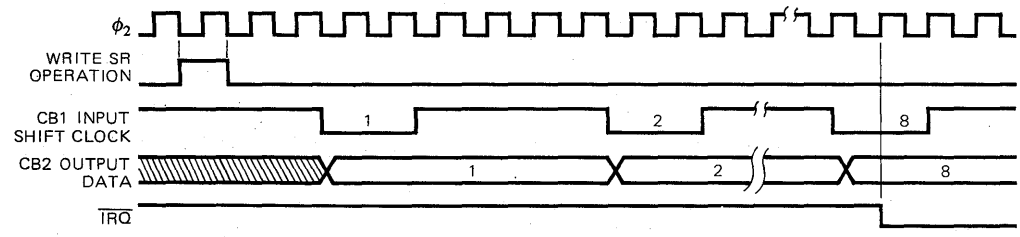


Figure 24. Shift Register Output Modes

The Interrupt Flag Register (IFR) and Interrupt Enable Register (IER) are depicted in Figure 25 and 26, respectively.

The IFR may be read directly by the processor. In addition, individual flag bits may be cleared by writing a "1" into the appropriate bit of the IFR. When the proper chip select and register signals are applied to the chip, the contents of this register are placed on the data bus. Bit 7 indicates the status of the IRQ output. This bit corresponds to the logic function: IRQ = IFR6 x IER6 + IFR5 x IER5 + IFR4 x IER4 + IFR3 x IER3 + IFR2 x IER2 + IFR1 x IER1 + IFR0 x IER0. Note: X = logic AND, + = Logic OR.

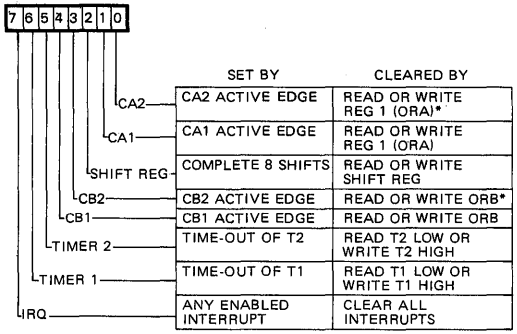
The IFR bit 7 is not a flag. Therefore, this bit is not directly cleared by writing a logic 1 into it. It can only be cleared by clearing all the flags in the register or by disabling all the active interrupts as discussed in the next section.

For each interrupt flag in IFR, there is a corresponding bit in the Interrupt Enable Register. The system processor can set or clear selected bits in this register to facilitate controlling individual interrupts without affecting others. This is accomplished by writing to address 1110 (IER address). If bit 7 of the data placed on the system data bus during this write operation is a 0, each 1 in bits 6 through 0 clears the corresponding bit in the Interrupt Enable Register. For each zero in bits 6 through 0, the corresponding bit is unaffected.

Setting selected bits in the Interrupt Enable Register is accomplished by writing to the same address with bit 7 in the data word set to a logic 1. In this case, each 1 in bits 6 through 0 will set the corresponding bit. For each zero, the corresponding bit. For each zero, the corresponding bit will be unaffected. The individual control of the setting and clearing operations allows very convenient control of the interrupts during system operation.

In addition to setting and clearing IER bits, the processor can read the contents of this register by placing the proper address on the register select and chip select inputs with the R/$\overline{W}$ line high. Bit 7 will be read as a logic 1.

Reg 13 — Interrupt Flag Register

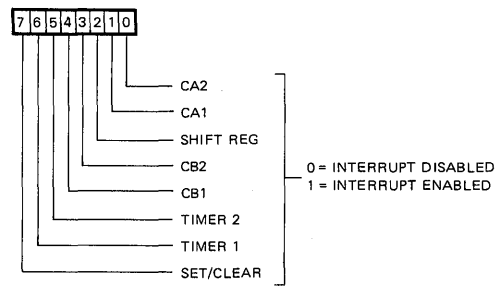


	SET BY	CLEARED BY
CA2	CA2 ACTIVE EDGE	READ OR WRITE REG 1 (ORA)*
CA1	CA1 ACTIVE EDGE	READ OR WRITE REG 1 (ORA)
SHIFT REG	COMPLETE 8 SHIFTS	READ OR WRITE SHIFT REG
CB2	CB2 ACTIVE EDGE	READ OR WRITE ORB*
CB1	CB1 ACTIVE EDGE	READ OR WRITE ORB
TIMER 2	TIME-OUT OF T2	READ T2 LOW OR WRITE T2 HIGH
TIMER 1	TIME-OUT OF T1	READ T1 LOW OR WRITE T1 HIGH
IRQ	ANY ENABLED INTERRUPT	CLEAR ALL INTERRUPTS

* IF THE CA2/CB2 CONTROL IN THE PCR IS SELECTED AS "INDEPENDENT" INTERRUPT INPUT, THEN READING OR WRITING THE OUTPUT REGISTER ORA/ORB WILL NOT CLEAR THE FLAG BIT. INSTEAD, THE BIT MUST BE CLEARED BY WRITING INTO THE IFR, AS DESCRIBED PREVIOUSLY.

Figure 25. Interrupt Flag Register (IFR)

Reg 14 — Interrupt Enable Register



Notes:
1. IF BIT 7 IS A "0", THEN EACH "1" IN BITS 0-6 DISABLES THE CORRESPONDING INTERRUPT.
2. IF BIT 7 IS A "1", THEN EACH "1" IN BITS 0-6 ENABLES THE CORRESPONDING INTERRUPT.
3. IF A READ OF THIS REGISTER IS DONE, BIT 7 WILL BE "1" AND ALL OTHER BITS WILL REFLECT THEIR ENABLE/DISABLE STATE.

Figure 26. Interrupt Enable Register (IER)

Ordering Information

Part Number	Frequency	Package
UM6522	1 MHz	Plastic
UM6522A	2 MHz	Plastic

UM6532/UM6532A

RAM, I/O, Timer Array

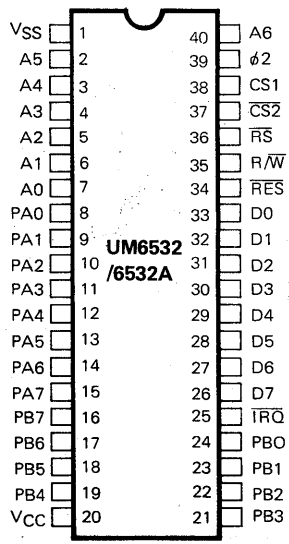
Features

- 8 bit bi-directional Data Bus for direct communication with the microprocessor
- Programmable edge-sensitive interrupt
- 128 x 8 static RAM
- Two 8 bit bi-directional data ports for interface to peripherals
- Two programmable I/O peripheral data direction registers
- Programmable interval timer
- Programmable interval timer interrupt
- Peripheral pins with direct transistor drive capability
- High impedance three-state data pins

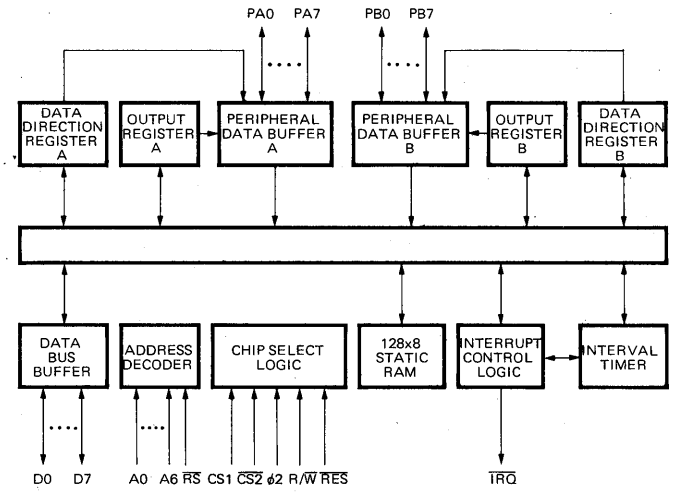
General Description

The UM6532 is designed to operate in conjunction with the UM6500 Microprocessor Family. It is comprised of a 128x8 static RAM, two software controlled 8 bit bi-directional data ports allowing direct interfacing between the microprocessor unit and peripheral devices, a software programmable interval timer with interrupt capable of timing in various intervals from 1 to 262,144 clock periods, and a programmable edge-detect interrupt circuit.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Supply Voltage . . . . . +8.0 Volts
Operating Voltage Range . . . . . +4V to +7V
Input Voltage Applied . . . . . GND–2.0V to 6.5V
I/O Pin Voltage Applied . . . . . GND–0.5V to V_{CC}+0.5V
Storage Temperature Range . . . . . –65°C to +150°C
Operating Temperature Range . . . . . 0°C to +70°C
Maximum Power Dissipation . . . . . 1 Watt

*Comments

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may effect device relability.

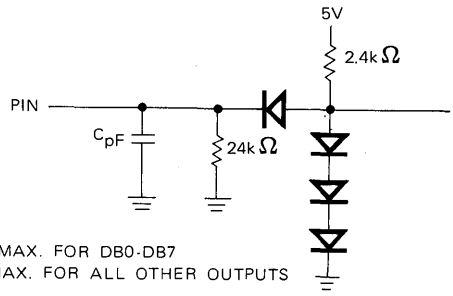
D.C. Characteristics

(V_{CC} = 5.0V ± 5%, V_{SS} = 0V, T_A = 0 – 70°C)

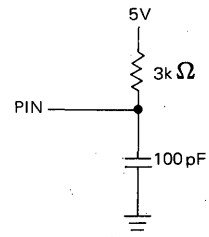
Characteristic	Symbol	Min.	Typ.	Max.	Units
Input High Voltage	V_{IH}	2.4		V_{CC}	V
Input Low Voltage	V_{IL}	0.3		0.4	V
Input Leakage Current; V_{IN} = V_{SS}+ 5V A0-A6, $\overline{RS}$, R/W, $\overline{RES}$, ϕ2, CS1, $\overline{CS2}$	I_{IN}		1.0	2.5	μA
Input Leakage Current for High Impedance State (Three State); V_{IN} = 0.4V to 2.4V; D0-D7	I_{TSI}		±1.0	±10.0	μA
Input High Current; V_{IN} = 2.4V PA0-PA7, PB0-PB7	I_{IH}	–100	–300		μA
Output High Voltage V_{CC} = MIN, I_{LOAD} –100μA (PA0-PA7, PB0-PB7, D0-D7) I_{LOAD} 3MA (PB0-PB7)	V_{OH}	 2.4 1.5			V
Output Low Voltage V_{CC} = MIN, I_{LOAD} 1.6MA	V_{OL}			0.4	V
Output High Current (Sourcing); V_{OH} ⩾ 2.4V (PA0-PA7, PB0-PB7, D0-D7) ⩾ 1.5V Available for direct transistor drive (PB0-PB7)	I_{OH}	 –100 3.0	 –1000 5.0		 μA mA
Output Low Current (Sinking); V_{OL} ⩽ 0.4V	I_{OL}	1.6			mA
Clock Input Capacitance	C_{CIK}			30	pf
Input Capacitance	C_{IN}			10	pf
Output Capacitance	C_{OUT}			10	pf
Power Dissipation (V_{CC} = 5.25V)	P_D			680	mW

*All inputs contain protection circuitry to prevent damage due to high static charges. Care should be exercised to prevent unnecessary application of voltage outside the specification range.

Test Load



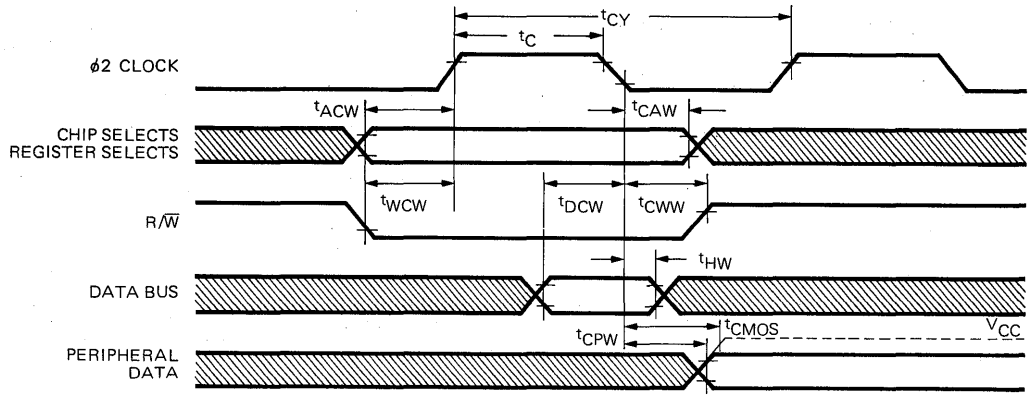
C = 130 pF MAX. FOR DB0-DB7
C = 30 pF MAX. FOR ALL OTHER OUTPUTS



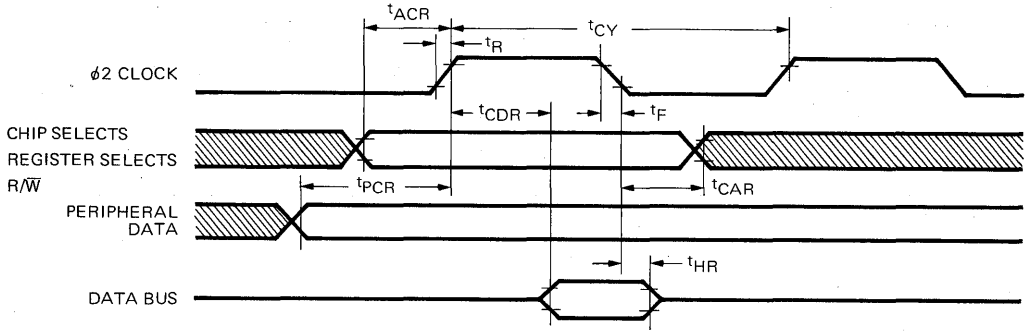
OPEN COLLECTOR
OUTPUT TEST LOAD

Peripheral IC

Write Timing Characteristics



Read Timing Characteristics



Write Timing Characteristics

Symbol	Parameter	UM6532		UM6532A		Units
		Min.	Max.	Min.	Max.	
T_{CY}	Cycle Time	1	50	0.50	50	μs
T_C	ϕ2 Pulse Width	0.44	25	0.22	25	μs
T_{ACW}	Address Set-Up Time	180	–	90	–	ns
T_{CAW}	Address Hold Time	0	–	0	–	ns
T_{WCW}	R/$\overline{W}$ Set-Up Time	180	–	90	–	ns
T_{CWW}	R/$\overline{W}$ Hold Time	0	–	0	–	ns
T_{DCW}	Data Bus Set-Up Time	265	–	100	–	ns
T_{HW}	Data Bus Hold Time	10	–	10	–	ns
T_{CPW}	Peripheral Data Delay Time	–	1.0	–	1.0	μs
T_{CMOS}	Peripheral Data Delay Time to CMOS Levels	–	2.0	–	2.0	μs

Note: t_r , t_f = 10 to 30 ns.

Read Timing Characteristics

Symbol	Parameter	UM6532		UM6532A		Units
		Min.	Max.	Min.	Max.	
T_{CY}	Cycle Time	1	50	0.5	50	μs
T_{ACR}	Address Set-Up Time	180	–	90	–	ns
T_{CAR}	Address Hold Time	0	–	0	–	ns
T_{PCR}	Peripheral Data Set-Up Time	300	–	300	–	ns
T_{CDR}	Data Bus Delay Time	–	340	–	200	ns
T_{HR}	Data Bus Hold Time	10	–	10	–	ns

Note: tr, tf = 10 to 30ns.

Interface Signal Description

Reset ($\overline{RES}$)

During system initialization a Logic "0" on the $\overline{RES}$ input will cause a zeroing of all four I/O registers. This in turn will cause all I/O buses to act as inputs thus protecting external components from possible damage and erroneous data while the system is being configured under software control. The Data Bus Buffers are put into an OFF-STATE during Reset. Interrupt capability is disabled with the $\overline{RES}$ signal. The $\overline{RES}$ signal must be held low for at least one clock period when reset is required.

Input Clock

The input clock is a system Phase Two clock which can be either a low level clock ($V_{IL}<0.4$, $V_{IH}>2.4$) or high level clock ($V_{IL}<0.2$, $V_{IH} = V_{CC}{}^{+0.3}_{-0.2}$).

Read/Write (R/$\overline{W}$)

The R/W signal is supplied by the microprocessor and is used to control the transfer of data to and from the UM6532. A high on the R/$\overline{W}$ pin allows the processor to read (with proper addressing) the UM6532. A low on the R/$\overline{W}$ pin allows a write (with proper addressing) to the UM6532.

Interrupt Request ($\overline{IRQ}$)

The $\overline{IRQ}$ output is derived from the interrupt control logic. It will normally be high with a low indicating an interrupt from the UM6532. $\overline{IRQ}$ is an open-drain output, permitting several units to be wire-or'ed to the common $\overline{IRQ}$ microprocessor input pin. The $\overline{IRQ}$ output may be activated by a transition on PA7 or timeout of the Interval Timer.

Data Bus (D0-D7)

The UM6532 has eight bi-directional data lines (D0-D7). These lines connect to the system's data bus and allow transfer of data to and from the microprocessor. The output buffers remain in the off state except when a Read operation occurs.

Peripheral Data Ports (PA0-PA7, PB0-PB7)

The UM6532 has two 8-bit peripheral I/O Ports, Port A (lines PA0-PA7) and Port B (lines PB0-PB7). Each line is individually programmable as either an input or an output. By writing a "0" to any bit position of the Data Direction Register (DDRA or DDRB) the corresponding line will be programmed an an input. Likewise, by writing a "1" to any bit position in DDRA or DDRB will cause the corresponding line to act as an output.

When a Port line is programmed as an input and its output register (ORA or ORB) is read by the MPU, the TTL level on the Port line will be transferred to the data bus. When the Port lines are programmed as outputs, the lines will reflect the data written by the MPU into the output registers. See Edge Sense Interrupt Section for an additional use of PA7.

Address and Select Lines (A0-A6, $\overline{RS}$, CS1 and $\overline{CS2}$)

A0-A6 and $\overline{RS}$ are used to address the RAM, I/O registers, Timer and Flag register. CS1 and $\overline{CS2}$ are used to select (enable access to) the UM6532.

Internal Organization

A block diagram of the internal architecture is shown in Figure 1. The UM6532 is divided into four basic sections: RAM, I/O, Timer, and Interrupt Control. The RAM interfaces directly with the microprocessor through the system data bus and address lines. The I/O section consists of two 8-bit halves. Each half contains a Data Direction Register (DDR) and an I/O register.

RAM 128 Bytes (1024 Bits)

A 128 x 8 static RAM is contained on the UM6532. It is addressed by A0-A6 (Byte Select), $\overline{RS}$, CS1, and $\overline{CS2}$.

Internal Peripheral Registers

There are four 8-bit internal registers: two data direction registers and two output registers. The two data direction registers (A side and B side) control the direction of the data into and out of the peripheral I/O. A logic zero in a bit of the data direction register (DDRA and DDRB) causes the corresponding line of the I/O port to act as an input. A logic one causes the corresponding line to act as an output. The voltage on any line programmed as an output is determined by the corresponding bit in the output register (ORA and ORB).

Data is read directly from the PA lines during a peripheral read operation. For a PA pin programmed as an output, the data transferred into the processor will be the same as the data in the ORA only if the voltage on the line is allowed to be $\geqslant$2.4 volts for a logic one and $\leqslant$0.4 volts for a zero. If the loading on the line does not allow this, then the data resulting from the read operation may not match the contents of ORA.

The output buffers for the PB lines are somewhat different from the PA buffers. The PB buffers are push-pull devices which are capable of sourcing 3 mA at 1.5 volts. This allows these lines to directly drive transistor circuits. To assure that the processor will read the proper data when performing a peripheral read operation, logic is provided in the peripheral B port to permit the processor to read the contents of ORB, instead of the PB lines.

Interval Timer

The Timer section of the UM6532 contains three basic parts: preliminary divide down register, programmable 8-bit register and interrupt logic. These are illustrated in Figure 1.

The Interval Timer can be programmed to count up to 256 time intervals. Each time interval can be either 1T, 8T, 64T, or 1024T increments, where T is the system clock period. When a full count is reached, the interrupt flag is set to a logic "1". After the interrupt flag is set the internal clock continues counting down, but at a 1T rate to a maximum of-255T. This allows the user to read the counter and then determine how long the interrupt has been set.

The 8-bit system Data Bus is used to transfer data to and from the Interval Timer. If a count of 52 time intervals were to be counted, the pattern 0 0 1 1 0 1 0 0 would be put on the Data Bus and written into the Interval Time register.

At the same time that data is being written to the Interval Timer, the counting intervals of 1, 8, 64, 1024T are decoded from address lines A0 and A1. During a Read or Write operation address line A3 controls the interrupt capability of $\overline{IRQ}$, i.e., A3=1 enables $\overline{IRQ}$, A3=0 disables $\overline{IRQ}$. In either case, when timeout occurs, bit 7 of the Interrupt Flag Register is set. This flag is cleared when the Timer register is either read from or written to by the processor. If $\overline{IRQ}$ is enabled by A3 and an interrupt occurs $\overline{IRQ}$ will go low. When the Timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read, i.e., 51, 50, 49, etc.

When the Timer has counted down to 0 0 0 0 0 0 0 0 an interrupt will occur on the next count time and the counter will read 1 1 1 1 1 1 1 1. After interrupt, the Timer register decrements at a divide by "1" rate of the system clock. If after interrupt, the Timer is read and a value of 1 1 1 0 0 1 0 0 is read, the time since interrupt is 28T. The value read is in two's complement.

Value read = 1 1 1 0 0 1 0 0
Complement = 0 0 0 1 1 0 1 1
Add 1 = 0 0 0 1 1 1 0 0 = 28.

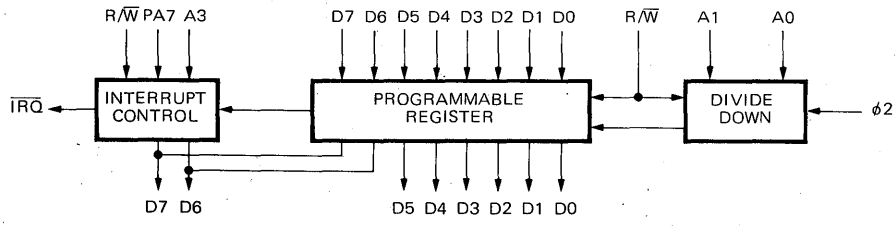


Figure 1. Basic Elements of Interval Timer

Thus, to arrive at the total elapsed time, merely do a two's complement and add to the original time written into the Timer. Again, assume time written as 0 0 1 1 0 1 0 0 (=52). With a divide by 8, total time to interrupt is (52x8) + 1 = 417T. Total elapsed time would be 416T + 28T = 444T, assuming the value read after interrupt was 1 1 1 0 0 1 0 0.

After an interrupt, whenever the Timer is written or read the interrupt is reset. However, the reading of the Timer at the same time the interrupt occurs will not reset the interrupt flag.

Figure 2 illustrates an example of interrupt.

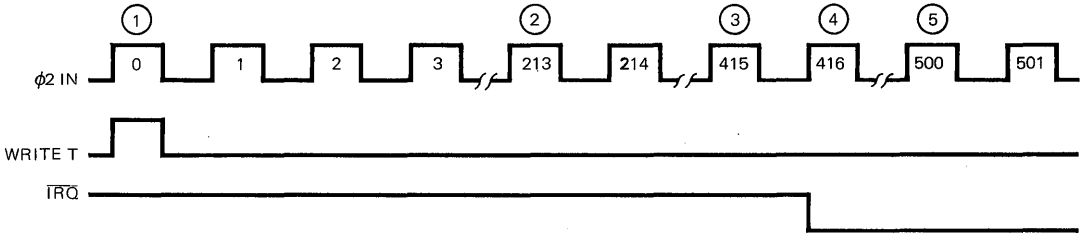


Figure 2. Timer Interrupt Timing

1. Data written into Interval Timers is 0 0 1 1 0 1 0 0 = 52_{10}
2. Data in Interval timer is 0 0 0 1 1 0 0 1 = 25_{10}

$$52 - \frac{231}{8} - 1 = 52 - 26 - 1 = 25$$

3. Data in Interval Timer is 0 0 0 0 0 0 0 0 = 0_{10}

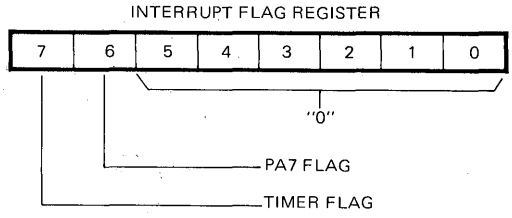
$$52 - \frac{415}{8} - 1 = 52 - 51 - 1 = 0$$

4. Interrupt has occurred at $\phi 2$ pulse #416
   Data in Interval Timer = 1 1 1 1 1 1 1 1
5. Data in Interval Timer is 1 0 1 0 1 1 0 0
   two's complement is 0 1 0 1 0 1 0 0 = 84_{10}
   $84 + (52 \times 8) = 500_{10}$

When reading the Timer after an interrupt, A3 should be low so as to disable the $\overline{IRQ}$ pin. This is done so as to avoid future interrupts until after another Write operation.

Interrupt Flag Register

The Interrupt Flag Register consists of two bits: the timer interrupt flag and the PA7 interrupt flag. When a read operation is performed on the Interrupt Flag Register, the bits are transferred to the processor on the data bus, as the diagram below, indicates.



The PA7 flag is cleared when the Interrupt Flag Register is read. The timer flag is cleared when the timer register is either written or read.

Addressing

Addressing of the UM6532 is accomplished by the 7 address inputs, the $\overline{RS}$ input and the two chip select inputs $\overline{CS1}$ and $\overline{CS2}$. To address the RAM, CS1 must be high with $\overline{CS2}$ and $\overline{RS}$ low. To address the I/O and Interval Timer CS1 and $\overline{RS}$ must be high with $\overline{CS2}$ low. As can be seen to access the chip CS1 is high and $\overline{CS2}$ is low. To distinguish between RAM or I/O-Timer Section the $\overline{RS}$ input is used. When this input is low the RAM is addressed, when high the I/O Interval Timer section is addressed. To distinguish between Timer and I/O, address line A2 is utilized. When A2 is high the Interval Timer is accessed. When A2 is low the I/O section is addressed. Table 1 illustrates the chip addressing.

Edge Sense Interrupt

In addition to its use as a peripheral I/O line, PA7 can function as an edge sensitive input. In this mode, an active transition on PA7 will set the internal interrupt flag (bit 6 of the Interrupt Flag Register). When this occurs, and providing the PA7 interrupt is enabled, the IRQ output will go low.

Control of the PA7 edge detecting logic is accomplished by performing a write operation to one of four addresses. The data lines for this operation are "don't care" and the addresses to be used are found in Table 1.

The setting of the internal interrupt flag by an active transition on PA7 is always enabled, whether PA7 is set up as an input or an output.

The $\overline{RES}$ signal disables the PA7 interrupt and sets the active transition to the negative edge-detect state. During the reset operation, the interrupt flag may be set by a negative transition. It may, therefore, be necessary to clear the flag before its normal use as an edge detecting input is enabled. This can be achieved by reading the Interrupt Flag Register.

I/O Register-Timer Addressing

Table 1 illustrates the address deconding for the internal elements and timer programming. Address line A2 distinguishes I/O registers from the Timer. When A2 is low and $\overline{RS}$ is high, the I/O registers are addressed. Once the I/O registers are addressed, address lines A1 and A0 decode the desired register.

When the timer is selected A1 and A0 decode the "divide-by" matrix. This decoding is defined in Table 1. In addition. Address A3 is used to enable the interrupt flag to $\overline{IRQ}$.

Table 1 Addressing Decode

Functions	$\overline{RS}$	A6	A5	A4	A3	A2	A1	A0	WR	RD
RAM	L	X	X	X	X	X	X	X	✓	✓
ORA	H	–	–	–	–	L	L	L	✓	✓
DDRA	H	–	–	–	–	L	L	H	✓	✓
ORB	H	–	–	–	–	L	H	L	✓	✓
DDRB	H	–	–	–	–	L	H	H	✓	✓
Time, ÷1, IRQ ON	H	–	–	H	H	H	L	L	✓	
Timer, ÷8, IRQ ON	H	–	–	H	H	H	L	H	✓	
Timer, ÷64, IRQ ON	H	–	–	H	H	H	H	L	✓	
Timer, ÷1024, IRQ ON	H	–	–	H	H	H	H	H	✓	
Timer, ÷1, IRQ OFF	H	–	–	H	L	H	L	L	✓	
Timer, ÷8, IRQ OFF	H	–	–	H	L	H	L	H	✓	
Timer, ÷64, IRQ OFF	H	–	–	H	L	H	H	L	✓	
Timer, ÷1024, IRQ OFF	H	–	–	H	L	H	H	H	✓	
Read Timer, IRQ ON	H	–	–	–	H	H	–	L		✓
Read Timer, IRQ OFF	H	–	–	–	L	H	–	L		✓
Read Interrupt Flags	H	–	–	–	–	H	–	H		✓
RA7 IRQ OFF, NEG EDGE	H	–	–	L	–	H	L	L	*	
PA7 IRQ OFF, POS EDGE	H	–	–	L	–	H	L	H	*	
PA7 IRQ ON, NEG EDGE	H	–	–	L	–	H	H	L	*	
PA7 IRQ ON, POS EDGE	H	–	–	L	–	H	H	H	*	

Notes: X = Address – = Address bits don't care * = Data bits are "don't care"

Ordering Information

Part Number	Speed	Package
UM6532	1 MHz	Plastic
UM6532A	2 MHz	Plastic

UM6551 / UM6551A

Asynchronous Communication Interface Adapter

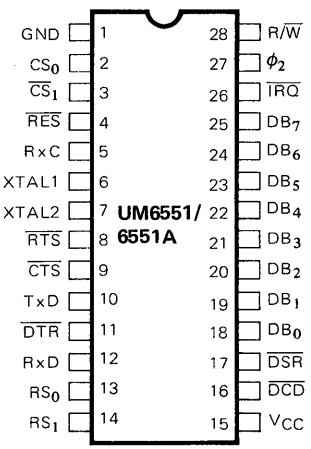
Features

- On-chip baud rate generator: 15 programmable baud rates derived from a standard 1.8432 MHz external crystal (50 to 19,200 baud)
- Programmable interrupt and status register to simplify software design
- Single +5 volt power supply
- Serial echo mode
- False start bit detection
- 8-bit bi-directional data bus for direct communication with the microprocessor
- External 16x clock input for non-standard baud rates (up to 125 k baud)
- Programmable: word lengths; number of stop bits; and parity bit generation and detection
- Data set and modem control signals provided
- Parity: (odd, even, none, mark, space)
- Full-duplex or half-duplex operation
- 5, 6, 7, 8, and 9 bit transmission

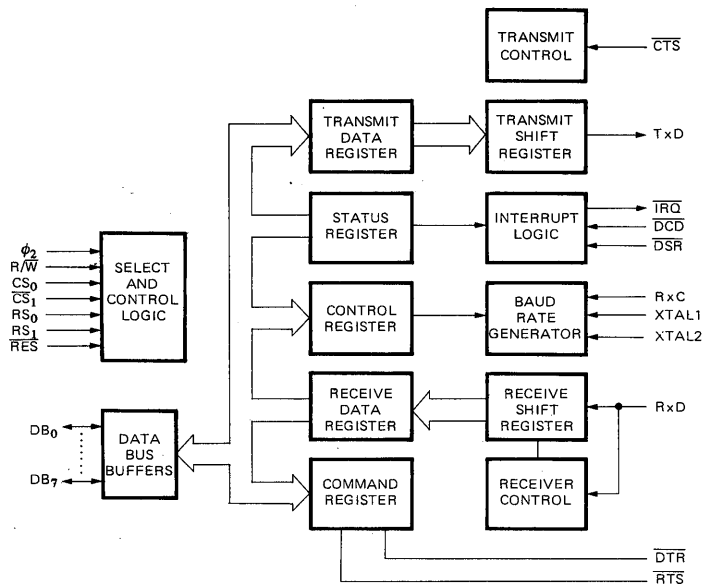
General Description

The UM6551 is an Asynchronous Communication Adapter (ACIA) intended to provide for interfacing the 6500/6800 microprocessor families to serial communication data sets and modems. A unique feature is the inclusion of an on-chip programmable baud rate generator, with a crystal being the only external component required.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Supply Voltage V_{CC} . . . . . −0.3V to +7.0V
Input/Output Voltage V_{IN} . . . . . −0.3V to +7.0V
Operating Temperature T_{OP} . . . . . 0°C to 70°C
Storage Temperature T_{STG} . . . . . −55°C to 150°C

Note:
All inputs contain protection circuitry to prevent damage to high static charges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

(V_{CC} = 5.0V ± 5%, T_A = 0−70°C, unless otherwise noted)

Characteristics	Symbol	Min.	Typ.	Max.	Units
Input High Voltage	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	−0.3	–	0.8	V
Input Leakage Current: V_{IN} = 0 to 5V ($\phi 2$, R/$\overline{W}$, $\overline{RES}$, CS_0, $\overline{CS_1}$, RS_0, RS_1, $\overline{CTS}$, RxD, $\overline{DCD}$, $\overline{DSR}$)	I_{IN}	–	±1.0	±2.5	μA
Input Leakage Current for High Impedance State (Three State)	I_{TSI}	–	±2.0	±10.0	μA
Output High Voltage: I_{LOAD} = −100μA (DB_0-DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$)	V_{OH}	2.4	–	–	V
Output Low Voltage: I_{LOAD} = 1.6mA (DB_0-DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	V_{OL}	–	–	0.4	V
Output High Current (Sourcing): V_{OH} = 2.4V (DB_0-DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$)	I_{OH}	−100	–	–	μA
Output Low Current (Sinking): V_{OL} = 0.4V (DB_0-DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	I_{OL}	1.6	–	–	mA
Output Leakage Current (Off State): V_{OUT} = 5V ($\overline{IRQ}$)	I_{OFF}	–	1.0	10.0	μA
Clock Capacitance ($\phi 2$)	C_{CLK}	–	–	20	pF
Input Capacitance (Except XTAL 1 and XTAL2)	C_{IN}	–	–	10	pF
Output Capacitance	C_{OUT}	–	–	10	pF
Power Dissipation (See Graph) (T_A = 0°C) V_{CC} = 5.25V	P_D	–	170	300	mW

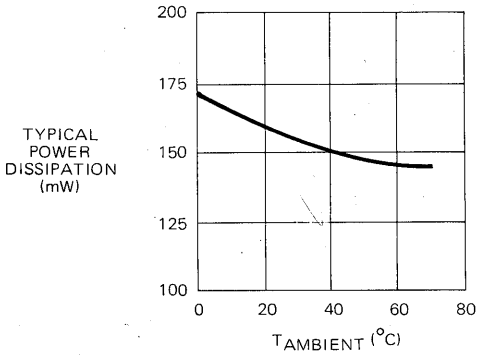


Figure 1. Power Dissipation vs. Temperature

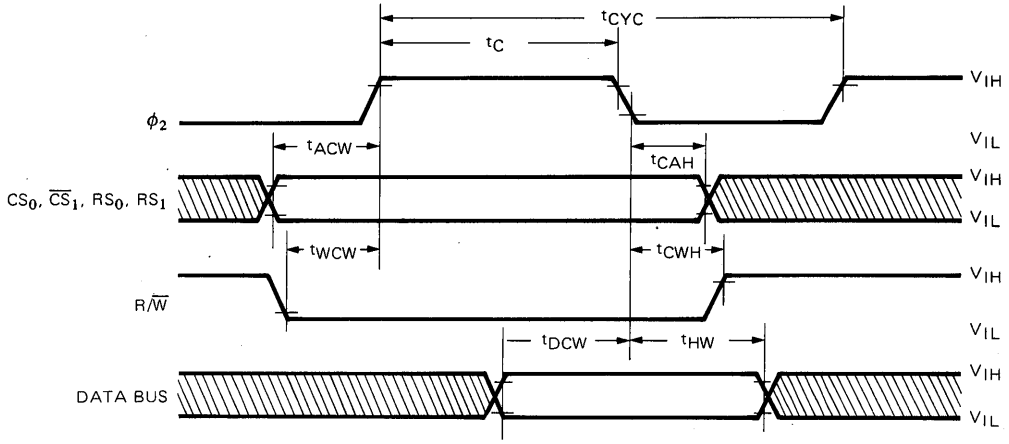


Figure 2. Write Timing Characteristics

Write Cycle

(V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristics	Symbol	UM6551		UM6551A		Units
		Min.	Max.	Min.	Max.	
Cycle Time	t_{CYC}	1.0	–	0.5	–	μs
φ2 Pulse Width	t_C	400	–	200	–	ns
Address Set-Up Time	t_{ACW}	120	–	70	–	ns
Address Hold Time	t_{CAH}	0	–	0	–	ns
R/$\overline{W}$ Set-Up Time	t_{WCW}	120	–	70	–	ns
R/$\overline{W}$ Hold Time	t_{CWH}	0	–	0	–	ns
Data Bus Set-Up Time	t_{DCW}	150	–	60	–	ns
Data Bus Hold Time	t_{HW}	20	–	20	–	ns

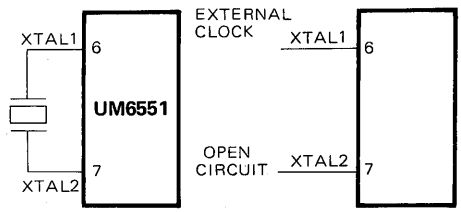
(t_r and t_f = 10 to 30 ns)

Crystal Specification

1. Temperature stability ± 0.01% (0° to 70°C)
2. Characteristics at 25°C ± 2°C
   a. Frequency (MHz) 1.8432
   b. Frequency tolerance (±%) 0.02
   c. Resonance mode Series
   d. Equivalent resistance (ohm) 400 max.
   e. Drive level mW 2
   f. Shunt capacitance pF 7 max.
   g. Oscillation mode Fundamental

No other external components should be in the crystal circuit

Clock Generation



INTERNAL CLOCK EXTERAL CLOCK

Peripheral IC

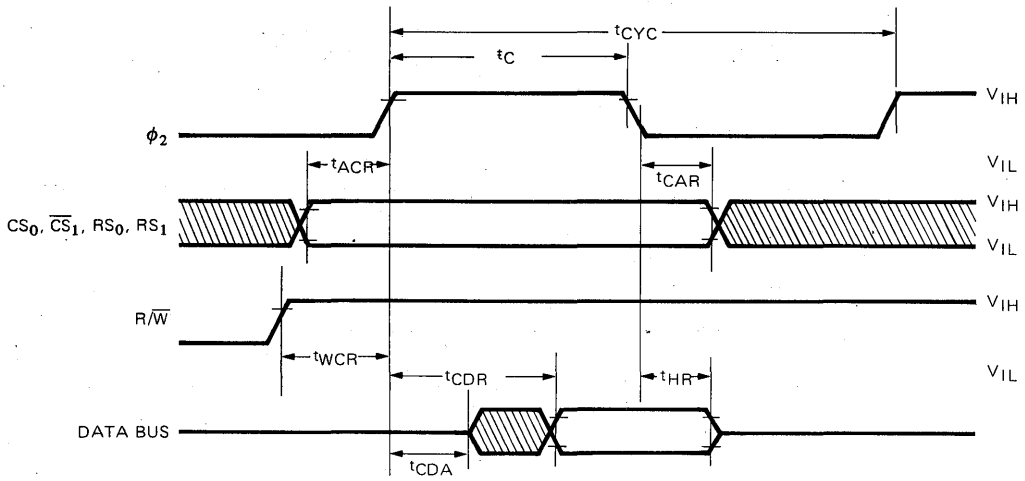


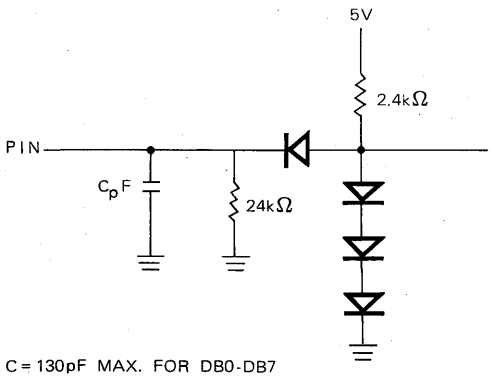
Figure 3. Read Timing Characteristics

Read Cycle

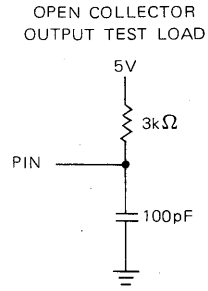
(V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristics	Symbol	UM6551		UM6551A		Units
		Min.	Max.	Min.	Max.	
Cycle Time	t_{CYC}	1.0	–	0.5	–	μs
Pulse Width (φ2)	t_C	400	–	200	–	ns
Address Set-Up Time	t_{ACR}	120	–	70	–	ns
Address Hold Time	t_{CAR}	0	–	0	–	ns
R/W Set-Up Time	t_{WCR}	120	–	70	–	ns
Read Access Time (Valid Data)	t_{CDR}	–	200	–	150	ns
Read Data Hold Time	t_{HR}	20	–	20	–	ns
Bus Active Time (Invalid Data)	t_{CDA}	40	–	40	–	ns

Test Load



C = 130pF MAX. FOR DB0-DB7
C = 30pF MAX. FOR ALL OTHER OUTPUTS



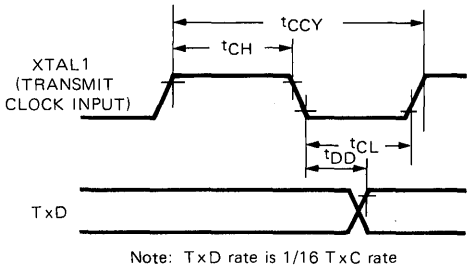


Figure 4a. Transmit Timing with External Clock

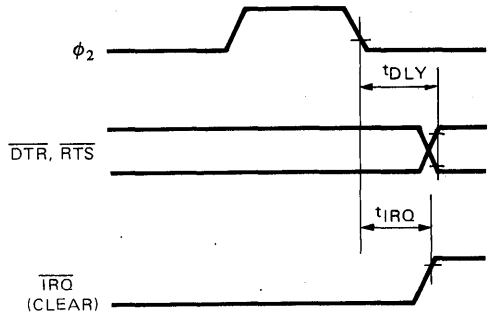


Figure 4b. Interrupt and Output Timing

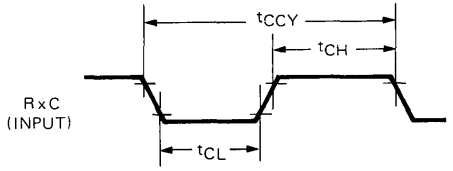


Figure 4c. Receive External Clock Timing

Transmit/Receive Characteristics

Characteristics	Symbol	UM6551		UM6551A		Unit
		Min.	Max.	Min.	Max.	
Transmit/Receive Clock Rate	t_{CCY}	400*	–	400*	–	ns
Transmit/Receive Clock High Time	t_{CH}	175	–	175	–	ns
Transmit/Receive Clock Low Time	t_{CL}	175	–	175	–	ns
XTAL 1 to TxD Propagation Delay	t_{DD}	–	500	–	500	ns
Propagation Delay ($\overline{RTS}$, $\overline{DTR}$)	t_{DLY}	–	500	–	500	ns
$\overline{IRQ}$ Propagation Delay (Clear)	t_{IRQ}	–	500	–	500	ns

(t_r, t_f = 10 to 30 ns input clocks only)

* The baud rate with external clocking is: Baud Rate = $\frac{1}{16 \times T_{CCY}}$

Interface Signal Description

$\overline{RES}$ (Reset)

During system initialization a low on the $\overline{RES}$ input will cause internal registers to be cleared.

ϕ2 (Input Clock)

The input clock is the system ϕ2 clock and is used to trigger all data transfers between the system microprocessor and the UM6551.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the UM6551. A low on the R/$\overline{W}$ pin allows a write to the UM6551.

$\overline{IRQ}$ (Interrupt Request)

The $\overline{IRQ}$ pin is an interrupt signal from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common $\overline{IRQ}$ microprocessor input. Normally a high level, $\overline{IRQ}$ goes low when an interrupt occurs.

DB_0-DB_7 (Date Bus)

The DB_0-DB_7 pins are the eight data lines used for transfer of data between the processor and the UM6551. These lines, are bi-directional and are normally high-impedance except during Read cycles when selected.

CS_0, CS_1 (Chip Selects)

The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The UM6551 is selected when CS_0 is high and $\overline{CS_1}$ is low.

RS_ϕ, RS_1 (Register Selects)

The two register select lines are normally connected to the processor address lines to allow the processor to select the various UM6551 internal registers. The following table indicates the internal register select coding:

RS_1	RS_0	Write	Read
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

The table shows that only the Command and Control registers are read/write. The Programmed Reset operation does not cause an data transfer, but is used to clear the UM6551 registers. The Programmed Reset is slightly different from the Hardware Reset ($\overline{RES}$) and these differences are described in the individual register definitions.

Acia/Modem Interface Signal Description

XTAL1, XTAL2 (Crystal Pins)

These pins are normally directly connected to the external crystal (1.8432 MHz) used to derive the various baud rates. Alternatively, an externally generated clock may be used to drive the XTAL1 pin, in which case the XTAL2 pin must float.

TxD (Transmit Data)

The TxD output line is used to transfer serial NRZ (nonreturn-to-zero) data to the modem. The LSB (least significant bit) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected.

RxD (Receive Data)

The RxD input line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or the rate of an externally generated receiver clock. This selection is made by programming the Control Register.

RxC (Receive Clock)

The RxC is a bi-directional pin which serves as either the receiver 16x clock input or the receiver 16x clock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

$\overline{RTS}$ (Request to Send)

The $\overline{RTS}$ output pin is used to control the modem from the processor. The state of the $\overline{RTS}$ pin is determined by the contents of the Command Register.

$\overline{CTS}$ (Clear to Send)

The $\overline{CTS}$ input pin is used to control the transmitter operation. The enable state is with $\overline{CTS}$ low. The transmitter is automatically disabled if $\overline{CTS}$ is high.

DTR (Data Terminal Ready)

This output pin is used to indicate the status of the UM6551 to the modem. A low on $\overline{DTR}$ indicates the UM6551 is enabled and a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

$\overline{DSR}$ (Data Set Ready)

The $\overline{DSR}$ input pin is used to indicate to the UM6551 the status of the modem. A low indicates the "ready" state and a high, "not-ready." $\overline{DSR}$ is a high-impedance input and must not be a no-connect. If unused, it should be driven high or low, but not switched.

Note: if Command Register Bit 0 = 1 and a change of state on $\overline{DSR}$ occurs, $\overline{IRQ}$ will be set, and Status Register Bit 6 will reflect the new level. The state of $\overline{DSR}$ does not affect either Transmitter or Receiver operation.

$\overline{DCD}$ (Data Carrier Detect)

The $\overline{DCD}$ input pin is used to indicate to the UM6551 the status of the carrierdetect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not. $\overline{DCD}$, like $\overline{DSR}$, is a high-impedance input and must not be a no-connect.

Note: If Command Register Bit 0 = 1 and a change of state on $\overline{DCD}$ occurs, $\overline{IRQ}$ will be set, and Status Register Bit 5 will reflect the new level. The state of $\overline{DCD}$ does not affect Transmitter operation, but must be low for the Receiver to operate.

Internal Organization

The Transmitter/Receiver sections of the UM6551 are depicted by the block diagram in Figure 5.

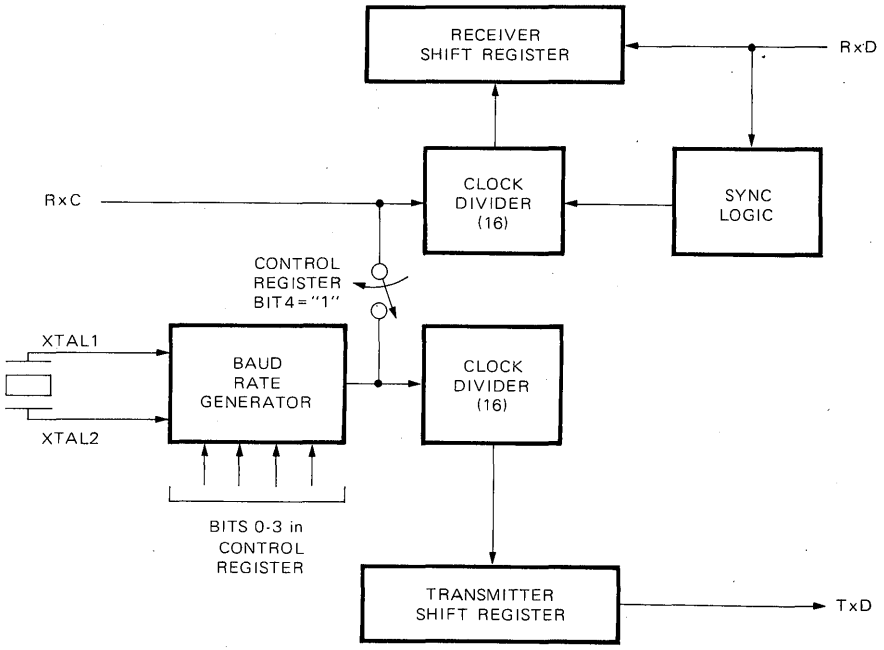


Figure 5. Transmitter/Receiver Clock Circuits

Bits 0-3 of the Control Register select the divisor used to generate the baud rate for the Transmitter. If the Receiver clock is to use the same baud rate as the Transmitter, then R x C becomes an output pin and can be used to slave other circuits to the UM6551.

Control Register

The Control Register is used to select the desired mode for the UM6551. The word length, number of stop bits, and clock controls are all determined by the Control Register, which is depicted in Figure 6.

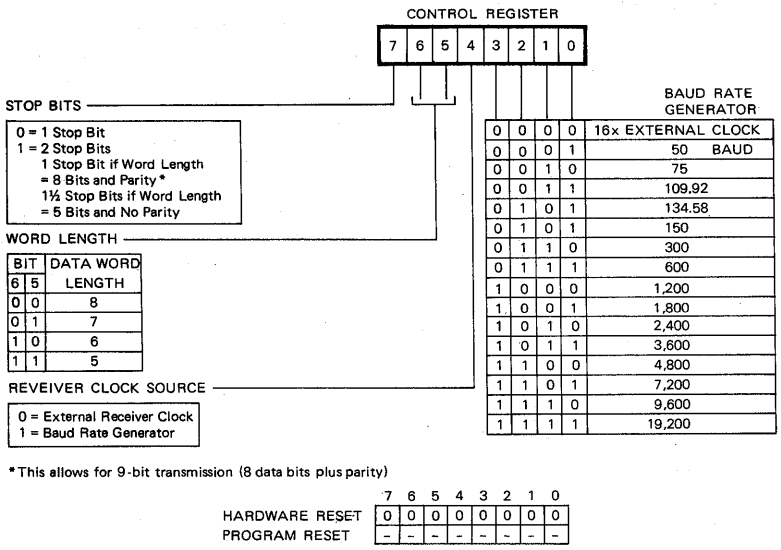


Figure 6. Control Register Format

Command Register

The Command Register is used to control Specific Transmit/Receive functions and is show in Figure 7.

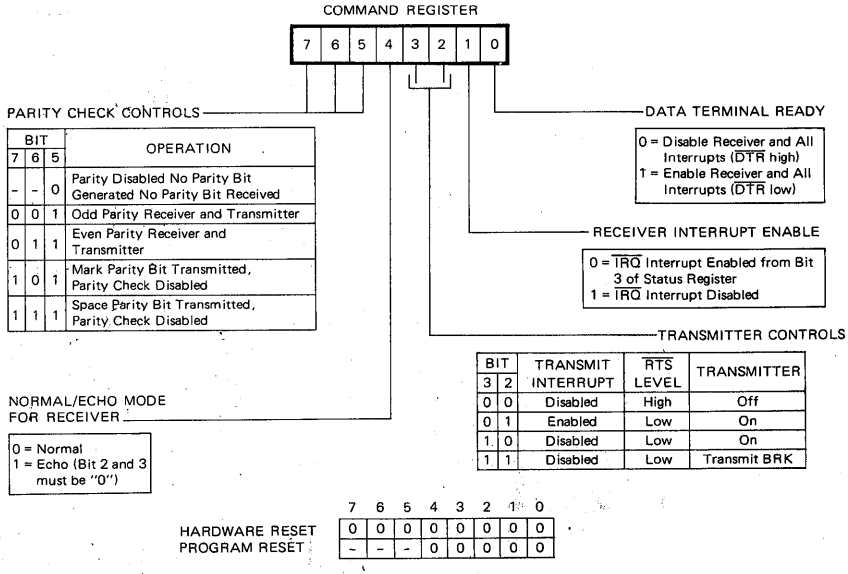
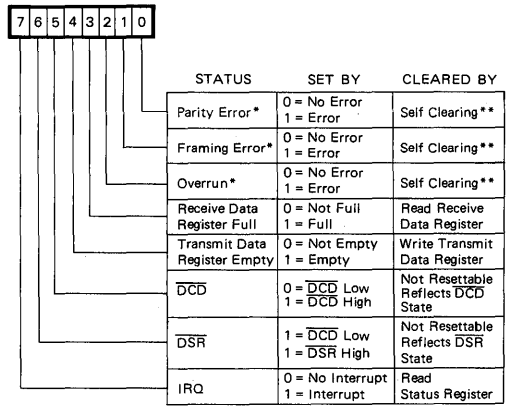


Figure 7. Command Register Format

Status Register

The Status Register is used to indicate to the processor the status of various UM6551 functions and is outlined in Figure 8.



STATUS	SET BY	CLEARED BY
Parity Error*	0 = No Error 1 = Error	Self Clearing**
Framing Error*	0 = No Error 1 = Error	Self Clearing**
Overrun*	0 = No Error 1 = Error	Self Clearing**
Receive Data Register Full	0 = Not Full 1 = Full	Read Receive Data Register
Transmit Data Register Empty	0 = Not Empty 1 = Empty	Write Transmit Data Register
$\overline{DCD}$	0 = $\overline{DCD}$ Low 1 = $\overline{DCD}$ High	Not Resettable Reflects $\overline{DCD}$ State
$\overline{DSR}$	1 = $\overline{DCD}$ Low 1 = $\overline{DSR}$ High	Not Resettable Reflects $\overline{DSR}$ State
IRQ	0 = No Interrupt 1 = Interrupt	Read Status Register

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	-	-	1	0	0	0	0
PROGRAM RESET	-	-	-	-	-	0	-	-

*NO INTERRUPT GENERATED FOR THESE CONDITIONS.
**CLEARED AUTOMATICALLY AFTER A READ OF RDR AND THE NEXT ERROR FREE RECEIPT OF DATA.

Figure 8. Status Register Format

Transmit and Receive Data Registers

These registers are used as temporary data storage for the UM6551 Transmit and Receive circuits. The Transmit Data Register is characterized as follows:

- Bit 0 is the leading bit to be transmitted.
- Unused data bits are the high-order bits and are "don't care" for transmission.

The Receiver Data Register is characterized in a similar fashion:

- Bit 0 is the leading bit received.
- Unused data bits are the high-order bits and are "0" for the receiver.
- Parity bits are not contained in the Receive Data Register, but are stripped-off after being used for external parity checking. Parity and all unused high-order bits are "0".

Figure 9 illustrates a signle transmitted or received data word, for the example of 8 data bits, parity, and 1 stop bit.

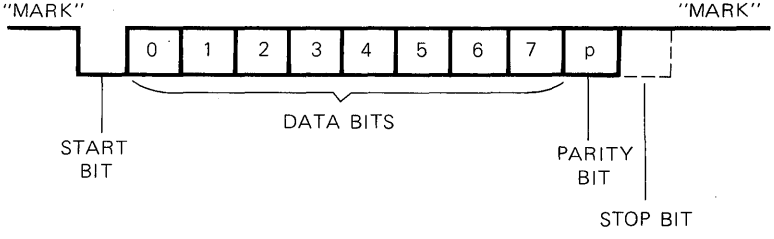


Figure 9. Serial Data Stream Example

Ordering Information

Part Number	Clock Rate	Package
UM6551	1 MHz	Plastic
UM6551A	2 MHz	Plastic

UM82C01

Capacitance Keyboard Encoder (CKE)

Features

- 16x8 matrix, can build up to 128 key capacitance keyboard
- Single chip with 16 scan drive outputs and 8 sense inputs
- Two types of package. 28 pin for 88 key KB and 40 pin for 128 key KB
- Keyboard scanning and encoding under complete control of the user's computer, especially UM8048 microcomputer
- Single 5V supply
- High-speed CMOS technology
- Serve as easy interface to UM8048
- New CMOS sense technology, CMOS analog sense circuit is built in
- Byte wide sense, higher performance than serial sense technology
- Wide UM8048 frequency range, 1M to 11 MHz UM8048 can be used

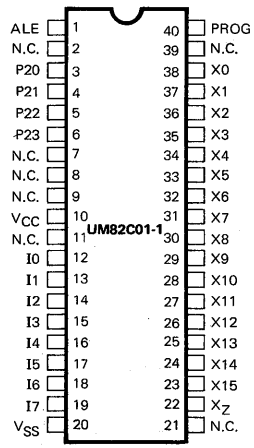
General Description

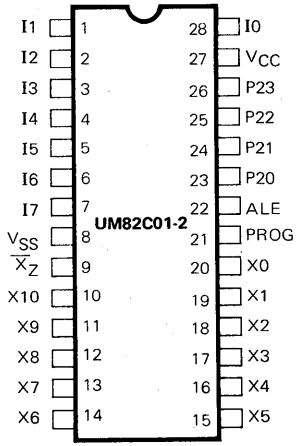
UM82C01 is a CMOS LSI, which offers interface between microcomputer and capacitive keyboard matrix. 40 pin UM82C01-1 is capable of scanning up to 128 lowcost capacitive keys. 28 pin UM82C01-2 serve keyboard applications with less than 88 keys.

The keyboard scan is under complete control of the UM8048 series microcomputer writing to expand I/O port, port 2 data is multiplexed to initiate one of the scan lines. Sense circuit will receive the scan signal through capacitive keys if one key is pressed. Sense circuit includes CMOS analog and digital circuit, which sense action by following amplifing and latching of analog signal from capacitive switch. These 8 bits data are then divided and latched marcing two nibbles. Two instructions can read these two nibbles from port 2. Then the microcomputer can analyze them and generate the scan code.

Antiscan is used to enhance the simple capacitive switches that are usually used in capacitive keyboard, offering switching threshold in sense input. This provides the keyboard with mechanical hysteresis which builts in the more expensive hall-effect and reed switches.

Pin Configuration





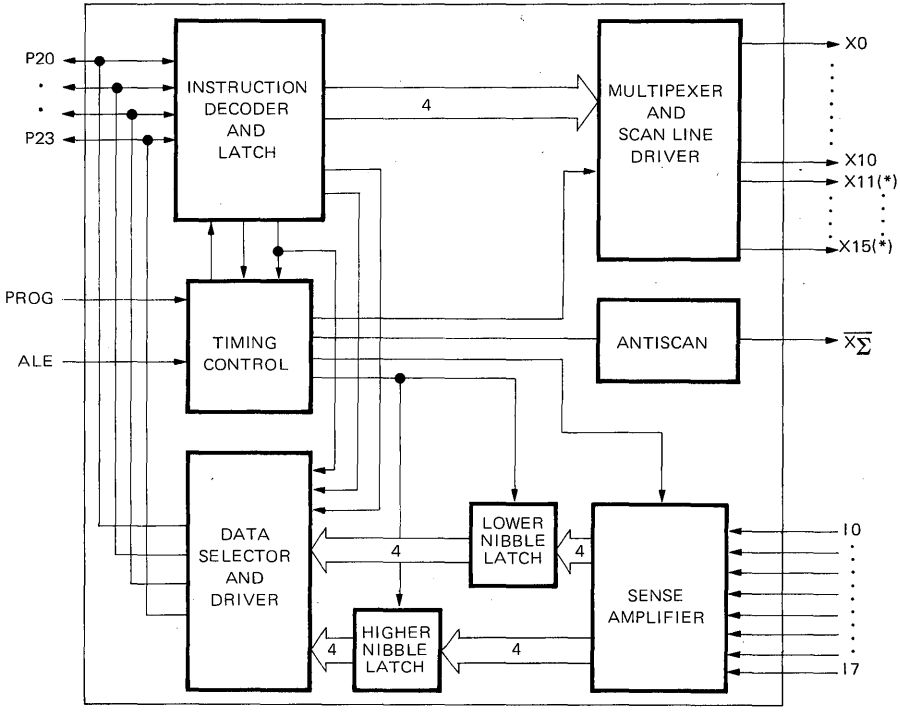
Absolute Maximum Ratings

Operating Temperature . . . . . 0° to 70°C
Storage Temperature . . . . . −55° to 150°C
Power Supply . . . . . Max. 7V
Voltage on Any Pin . . . . . V_{SS} −0.7V to V_{CC} +0.7V

*Comments

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions .for extended periods may effect device reliability.

Block Diagram



(*) Only in UM82C01-1

Peripheral IC

D.C. Characteristics

(Operating Voltage 5V ± 10%)

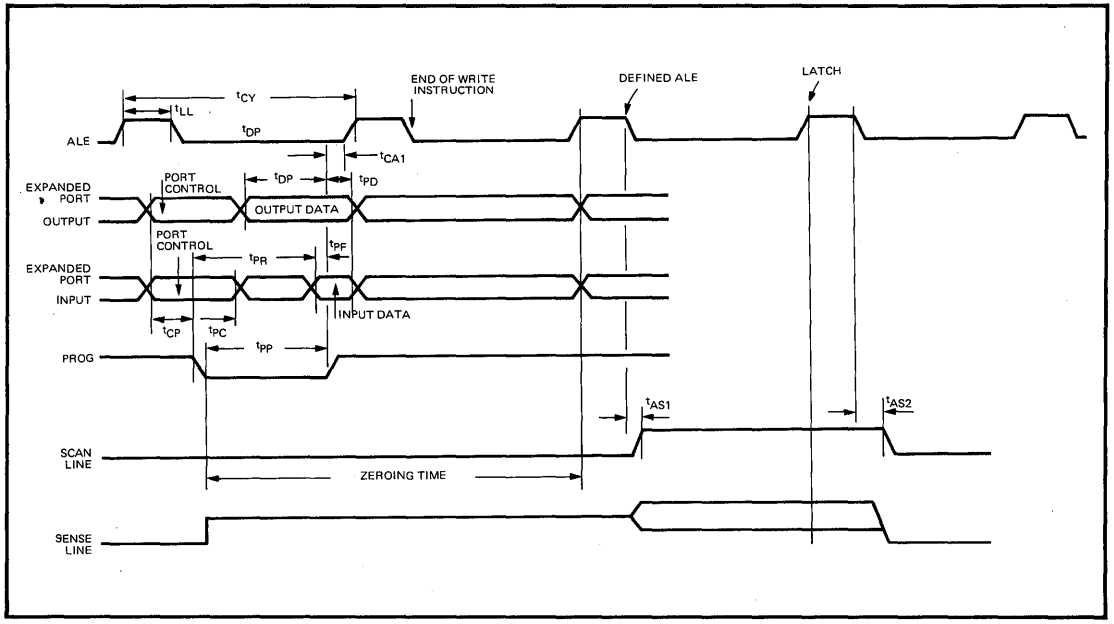
Item	Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Digital	Input Low Voltage	V_{IL}	−0.5		0.8	V	
	Input High Voltage	V_{IH}	2.0		V_{CC}	V	
	Output Low Voltage, I/O Port	V_{OLP}			0.45	V	I_{OL} = 5 mA
	Output High Voltage, I/O Port	V_{CHP}	V_{CC}-0.45		V_{CC}	V	I_{OH} = −400μA
	Output Low Voltage, Scan Line	V_{OLS}			0.45	V	I_{OL} = 5 mA
	Output High Voltage, Scan Line	V_{OHS}	V_{CC}-0.45		V_{CC}	V	I_{OH} = −5 mA
Analog	Input High to Reference	ΔV_H	0.1		1.8	V	Lying on Voltage Reference V_{REF}
	Input Low to Reference	ΔV_L	−0.1		−1.8	V	
Operating Current		I_{CC}			15	mA	
Stand by Power Supply Current		I_{SB}			200	μA	No sensing and Scanning

A.C. Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Characteristics	Symbol	UM8048/UM82C01						Units	Conditions
		4 MHz			11 MHz				
		Min.	Typ.	Max.	Min.	Typ.	Max.		
Address Latch Width	t_{LL}	700			150			ns	
Cycle Time	t_{CY}	3.75			1.36			μs	
Port Control Setup to PROG	t_{CP}	420			100			ns	
Port Control Hold to PROG	t_{PC}	800			160			ns	
Port Output Data Setup	t_{DP}	1350			400			ns	
Port Data Hold from PROG	t_{PD}	320			90			ns	
PROG Strobe to ALE	t_{CAI}	210			50			ns	
PROG Pulse Width	t_{PP}	2370			700			ns	
PROG to Port 2 Input Valid	t_{PR}			2130			700	ns	
Input Data Hold from PROG	t_{PF}			380			140	ns	
ALE to SCAN Setup	t_{AS_1}			200			100	ns	
ALE to SCAN Ended	t_{AS_2}			200			100	ns	

Timing Diagram



Pin Description

Pin	Names	I/O	Functions
P20-P23	I/O Port	I/O	This four-bit bidirectional port contains the address and control bits from UM8048 μC on a high to low transition of PROG. During a low to high transition of the PROG signal, the port contains the selected scan data for UM82C01 if the last command is a write operation. The sense nibble data from UM82C01 is latched during the low to high transition if the last command is a read operation. There exists a state flow in two continuous read operations which is called "read cycle". Upper nibble coming from sense inputs I4 to I7 are transferred in P20 to P23 from UM82C01 during low to high transition of PROG of MOVD A, P5 instruction, and lower nibble coming from I0 to I3 are transferred in P20 to P23 during low to high transition of PROG of MOVD A, P4 instruction.
ALE	Address Latch Enable Strobe	I	This pin comes direct from UM8048 ALE. It is used as the time base as well as address latch strobe. Our target is to let UM8048 work between 1MHz to 11MHz, so ALE varies from 66.6KHz to 733.3KHz. General PC key boards use 4 to 5MHz UM8048, hence, ALE is typically a 266.6KHz strobe signal for a 4MHz UM8048. When ALE first goes from low to high in a write cycle, the PROG is activated and goes to low and at this time, Port 2 containing port address and write instruction code is valid and should be latched by UM82C01 to initiate the scan mode.

Pin Description (Continued)

Pin	Names	I/O	Functions
ALE	Address Latch Enable Strobe	I	UM82C01 begins Zeroing stage of its sense amplifier at this instant. PROG will go to high before second ALE of this write instruction. The Zeroing stage ends at the next ALE low to high transient. If you see Timing Diagram on P. 11, you will find that this edge triggers the selected scan line to be active. The second ALE, which is next to end write instruction, is used to control scan line to inactive and its active transient is the high to low edge. In read cycle, when first ALE goes from high to low, PROG is activated to go to low, port 2 containing port address and read instruction code is valid and should be latched by UM82C01 to initiate the read mode.
PROG	Control Strobe	I	An active low strobe comes direct from UM8048 PROG. In the view point of UM8048, PROG is a control strobe to expanded I/O. UM82C01 is designed to locate expanded port 4 and port 5 in UM8048. Every time PROG is activated, UM82C01 is initiated to enter write or read mode. When PROG goes inactive in a write cycle, selected scan data is valid in port 2 and is latched by UM82C01 to encode the scan line. In a read cycle, latched upper nibble and lower nibble are valid circularly in port 2 at every PROG low to high transition.
X0-X15	Scan Line Out	O	These are the 16 full range drive outputs. One of the lines is activated in a write cycle. Selected scan data is latched and used to decode these sixteen scan lines so the scanning is fully programmable by UM8048. The selected scan line is activated in the defined ALE rising edge and ended in the next ALE falling edge. (Reference to Timing Diagram on P. 11) The defined ALE is the first ALE after the write instruction is finished. There are eleven scan lines for 28 pin UM82C01-2 X11 to X15 and are included in scan line driver for 40 pin UM82C01-1.
$\overline{X}_Z$	Antiscan Out	O	This is the antiscan output. This output is activated whenever no scanning occurs, and is deactivated when any one of X0 to X15 is activated. Antiscan is used to reduce the voltage in sense input when there is no scanning that prevents logic error.
10-17	Sense Line Input	I	These eight lines are inputs from capacitance keyboard matrix. The small current pulses caused by the scan lines and pressed keyswitches are detected here.
V_{CC}	Power Supply	I	Connected to +5V power supply.
V_{SS}	Ground	I	Normally connected to +0V ground.

Application Description

The Microprocessor

The capacitance keyboard encoder (CKE) UM82C01 is designed to serve as an interface to UM8048 series 8-bit microprocessor. The user can control the keyboard function easily through programming of microprocessor, which includes scanning reading and serve as an interface to host computer.

The Keyboard

A keyboard is an array of switches. The array consists of two dimensional matrix. One side of the matrix (X-lines) is used to drive the array with a microprocessor chosen signal, while the other side (1-lines) is connected to sense circuits. In traditional configuration, users make use of mechanical contact switches. With a new sensing mechanism, capacitive switches present a good solution.

The Capacitive Switch

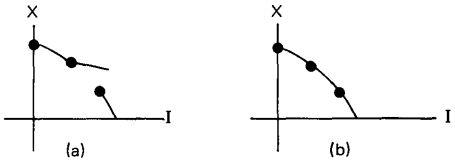


Figure 1. Mechanical Switch (a) Key off (b) Key on

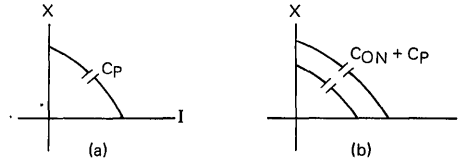
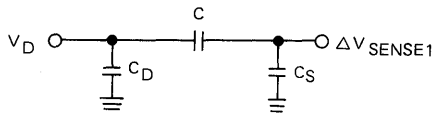


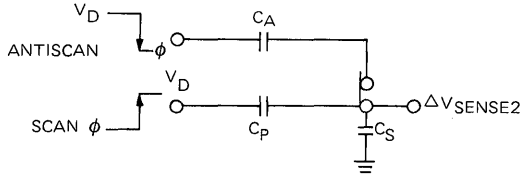
Figure 2. Capacitive Switch (a) Key off (b) key on

Fig. 1 shows the traditional mechanical switch, (a) The key switch is off, X-line and I-line are open to each other, (b) The key switch is on, X-line and i-line short together. Fig. 2, shows the capacitive switch, (a) The key switch is off; only a small parasitic capacitance exists between X-line and I-line, (b) The key switch is on, a Con + Cp appears between X-line and I-line.



$$\Delta V_{SENSE1} = V_D \cdot \frac{\frac{1}{C_S}}{\frac{1}{C_S} + \frac{1}{C}} = V_D \cdot \frac{C}{C_S + C}$$

Figure 3a. Equivalent circuit for Capacitive Key



$$\Delta V_{SENSE2} = V_D \frac{C_P}{C_S + C_P + C_A} - V_D \frac{C_A}{C_S + C_P + C_A}$$

Figure 3b. Equivalent circuit for Capacitive Key with Antiscan Consideration

In Fig. 3a, an equivalent circuit for capacitive key is shown. The voltage ΔV_{SENSE1} is decided by the scanning voltage V_D, capacitance C and C_S.

In Fig. 3b, an antiscanning consideration is presented. The scanning trigger edge is taking place with the inverse voltage "antiscan". After this edge, the voltage ΔV_{SENSE2} is decided by the voltage devided by C_P minus the voltage divided by C_A.

Writing

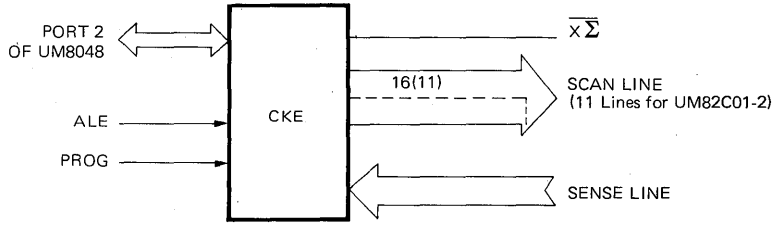


Figure 4. Logic Symbol of the CKE

Peripheral IC

In system configuration, the CKE is designed to stand in the expanded I/O port of 8048 microcomputer. The CKE uses the PORT 2, ALE and PROG to serve as an interface to the microprocessor. When 8048 writes a scan code to CKE, the CKE must be accessed through the expanded PORT 4. When UM8048 reads the sensing code from the CKE, the CKE must be accessed through the expanded PORT 4 and 5. The PORT 6 and 7 are reserved for the user.

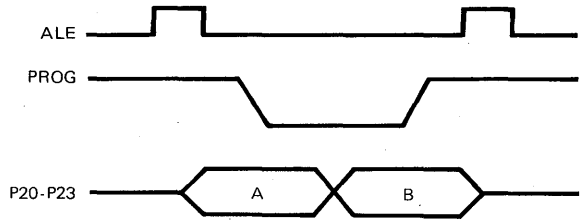


Figure 5. PROG Timing of UM8048 I/O PORT Expansion

Address	P21	P20	PORT	Definitions
	0	0	PORT 4	Writing Port
	0	1	PORT 5	(Same as PORT 4)
	1	0	PORT 6	
	1	1	PORT 7	
Instruction	**P23**	**P22**	**Instruction**	**Definitions**
	0	0	READ	
	0	1	WRITE	Writing Instruction
	1	0	OR	
	1	1	AND	

Figure 6. Expanded Port Definition in Writing Cycle

By using PORT 4 (PORT 5 the same) of UM8048 series microcomputer, the user can write his scanning data to the CKE chip. After the writing, two NOP instructions should be used to permit correct decoding and scanning. The timing diagram is shown in Fig. 7.

For example, if the user wants to scan X_1-line, the recommended Assembly is as listed:

Label	Command	Arguments	Comments
	⋮		
SCAN1:	MOV	A, #ϕ1H	; #ϕ1H Can Vary From ; #$\phi\phi$H To #ϕFH
	MOVD	P4, A	
	NOP		; Wait Until CKE Starts
	NOP		; Scanning.
	⋮		

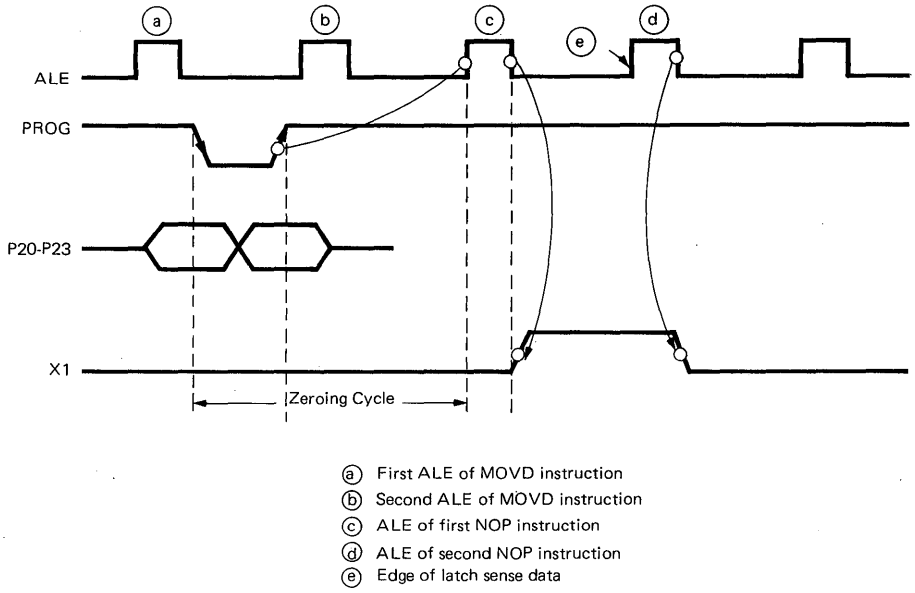


Figure 7. Timing Diagram of Writing and Scanning

Scanning

The CKE latches port address and instruction at the PROG high to low edge in Fig. 7, then enters the writing mode. At the PROG low to high edge, the CKE latches the data in P20–P23 which is now defined as the expanded PORT 4, and decodes the data to select the programmed scan line. Although the decoding and selection does not take much time, the scan line does not activate immediately.

From the PROG falling edge to the rising edge of the ALE, to the MOVD instruction in Fig. 7, the Sense Amplifier of CKE is "Zeroing". After the zeroing cycle, all the sense input are balanced at the reference voltage, and the selected scan line is activated at the falling edge of this ALE.

The scanning line X_0 to X_{15} can each be decoded from the hexadecimal data programmed in the PORT 4 at the writing cycle.

The scanning cycle equals to an ALE cycle, so the scanning closes at the ALE falling edge of second NOP instruction as shown in Fig. 7. Before the end of scanning, Sense Amplifier will latch the sense data; these will be discussed in the Sensing section.

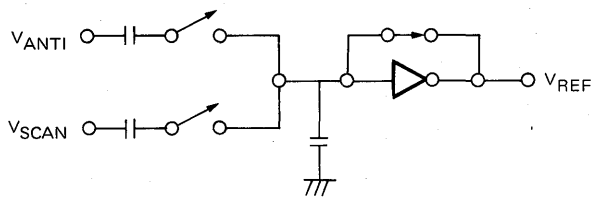
Antiscan

Antiscan line X_Σ is low whenever any scanning is activated, and is high when all scan line X_0 to X_{15} are low.

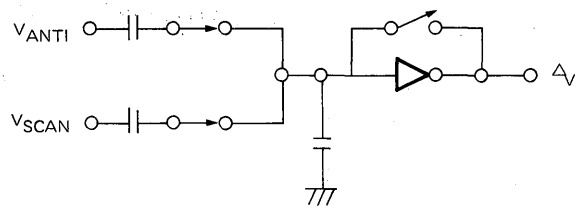
If no key is pressed, the antiscan will generate a $-\Delta V$ to the reference voltage, so that the Sense Amplifier will sense a voltage lower than reference voltage and latch a denoted low after amplification. If any key is pressed and the key is scanned, the voltage divided by the on capacitance will be a $+\Delta V$, so that the Sense Amplifier will sense a voltage higher than reference and latch a logic high after amplification.

The effect on whether antiscanning is larger than scanning depends on whether the key is pressed or not A new CMOS sense technology called "Sense Amplifier" is built in the CKE. In Fig. 8, we show the zeroing and sensing of this technology. In zeroing cycle, the switch between the input and output of the inverter is closed, so the sense input pad equals the reference voltage. After zeroing cycle, the shorting switch at the inverting stage is opened and sensing circuit is activated. In Fig. 7, we can see scanning also starts after zeroing. In fact, sensing is there writing for scanning. During the scanning cycle,

Sensing



(a) Zeroing



(b) Sensing

Fig. 8. Zeroing and Sensing

the CKE will latch the sensing input at the edge in Fig. 7.

The CKE uses byte-wide sensing, and has 8-bit latches. After latching, the data is separated into two nibbles, called Higher Nibble and Lower Nibble, and stored.

Reading

Because the CKE serves as an interface to UM8048 microcomputer by expanded PORT, the data must be 4-bit wide. Whenever there is data in the latches, the user can read the sensing data in nibble form. The CKE is designed to stand at the PORT 4 and PORT 5 in reading cycle.

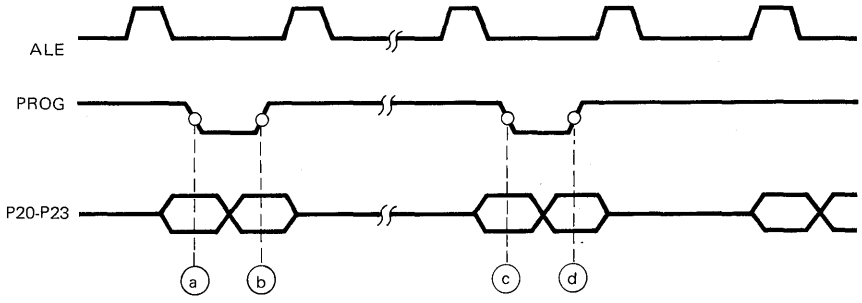
Address	P21	P20	PORT	Definitions
	0	0	PORT 4	Reading Lower Nibble
	0	1	PORT 5	Reading Higher Nibble
	1	0	PORT 6	Not used
	1	1	PORT 7	Not Used

Instruction	P23	P22	Instruction	Definitions
	0	0	Read	Reading Instruction
	0	1	Write	
	1	0	Or	
	1	1	And	

The latched data can be read by UM8048 in two read instructions, these two instructions need not but can be continuous, and higher nibble is defined to be read from PORT 5, lower nibble from PORT 4. Users must pay attention for if no reading is instructed before the next writing, 82C01 will reject the writing instruction until the reading instruction have been excuited.

The recommended reading Assembly is as listed and the timing diagram is shown in Fig. 10.

```
Label       Command     Arguments     Comments
                :
Read 1:     MOVD        A, P5         ; Read Higher Nibble
            SWAP        A
            MOV         Rn, A
Read 2:     MOVD        A, P4         ; Read Lower Nibble and
            ORL         A, Rn         ; Combine Nibbles to be Byte
                :
```



(a) Port address and instruction of READ 1
(b) High nibble output from CKE
(c) Port address and instruction of READ 2
(d) Lower nibble output from CKE

Figure 10. Port Timing of Reading

After the reading cycle, the microcomputer can use the read data to generate scan code or key code easily.

Application Note

UM82C01 is a new solution for capacitance keyboard. The application there for differs from the present capacitance Con and P.C. Board parasitic capacitance Cp of general capacitance keyboard and consideration should be given to design take them into. Con and Cp are listed in Table 1. C_S, C_A and C_{BS} are listed in Table 2. Table 3 (a) and (b) are recommendations of the capacitance selection.

Table 1. Definition of Con and C_p

Name	Symbol	Min.	Typ.	Max.	Unit
Key on Capacitance	C_{ON}	8	20		pf
P.C.B. Parasitic Capacitance	C_P		1	3	pf

Table 2. Definition of C_S, C_A and C_{BS}

Name	Symbol	Min.	Typ.	Max.	Unit
Shunt Capacitance	C_S		80	150	pf
Antiscan Capacitance	C_A	4		8	pf
Capacitance between two sense	C_{BS}			5	pf

Table 3. Recommended Application of C_A for various C_{ON}

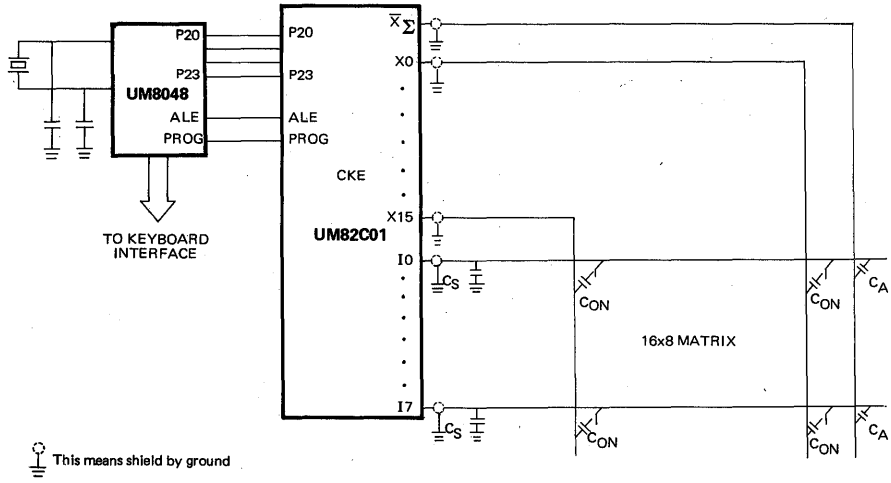
Symbol	Range		Unit
	Lower	Upper	
C_{ON}	10	25	pf
C_A	4	8	pf
C_P	0	3	pf

(a)

Symbol	Range		Unit
	Lower	Upper	
C_{ON}	25	35	pf
C_A	8	15	pf
C_P	0	3	pf

(b)

Typical Application



Ordering Information

Part Number	Package
UM82C01–1	40 DIP
UM82C01–2	28 DIP

UM82C284

Clock Generator And Ready Interface

ADVANCED PRODUCT DESCRIPTION

Features

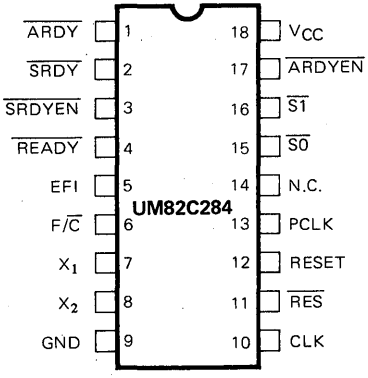
- Generates system clock for 80286 processors
- Uses crystal or TTL signal for frequency source
- Provides local READY and Multibus* READY synchronization
- 18-pin package
- Single +5V power supply
- Genrates system reset output from schmitt trigger input

General Description

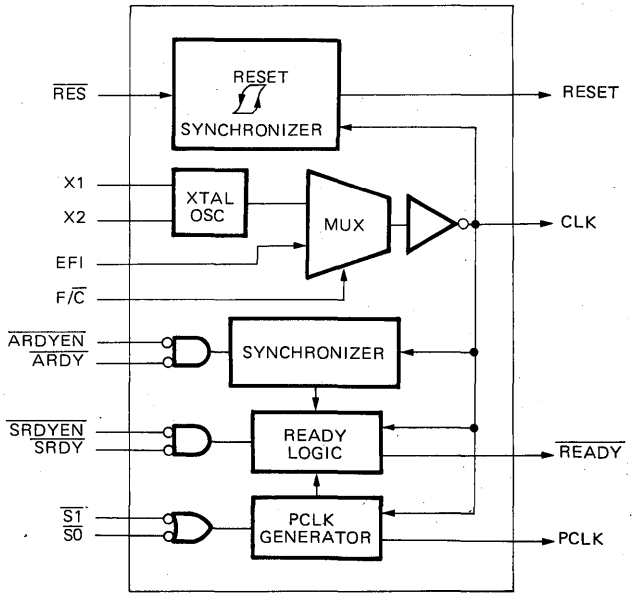
UM82C284 is a clock generator/driver which provides clock signals for 80286 processors and support components. It also contains logic to supply $\overline{\text{READY}}$ to the CPU from either asynchronous or synchronous sources and synchronous RESET from an asynchronous input with hysteresis. It is fabricated in Si-Gate CMOS process.

*Multibus is a patented bus of INTEL

Pin Configuration



Block Diagram



Peripheral IC

UM82C288

Bus Controller

ADVANCED PRODUCT DESCRIPTION

Features

- Provides commands and control for local and system bus
- Offers wide flexibility in system configurations
- Flexible command timing
- Optional Multibus* compatible timing
- Single +5V supply

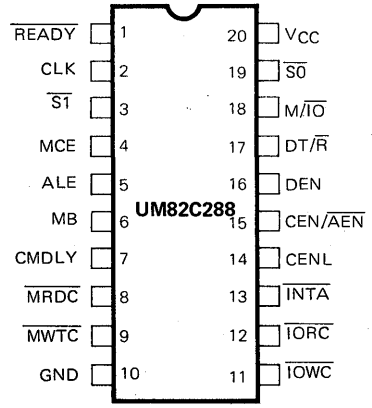
General Description

The UM82C288 Bus Controller is a 20-pin Si-Gate CMOS component for use in 80286 microsystems. The bus controller provides command and control outputs with flexible timing options. Separate command outputs are used for memory and I/O devices. The data bus is controlled with separate data enable and direction control signals.

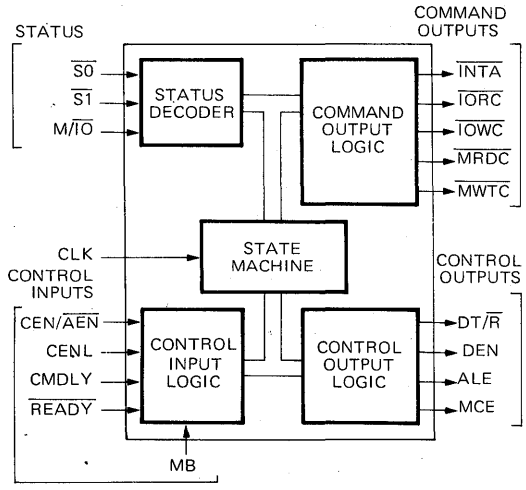
Two modes of operation are possible via a strapping option: Multibus compatible bus cycles, and high speed bus cycles.

*Multibus is a patented bus of Intel

Pin Configuration



Block Diagram



UM82C55A

CMOS Programmable Peripheral Interface

Features

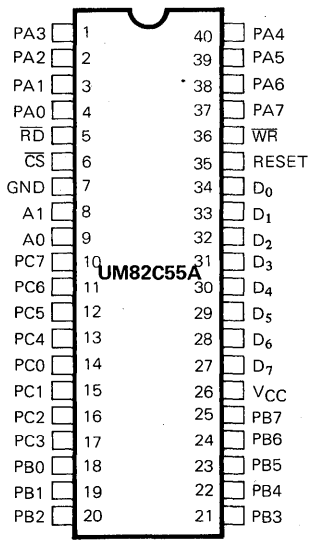
- Pin compatible with NMOS 8255A
- 24 programmable I/O pins
- Fully TTL compatible
- Bus-hold circuitry on all I/O ports eliminates pull-up resistors
- High speed, no "wait state" operation with 8MHz 80C86
- Direct bit set/reset capability
- Enhanced control word read capability
- Single 5V power supply
- 2.5mA drive capability on all I/O port outputs
- Low standby power $-I_{CCSB} = 10\mu A$

General Description

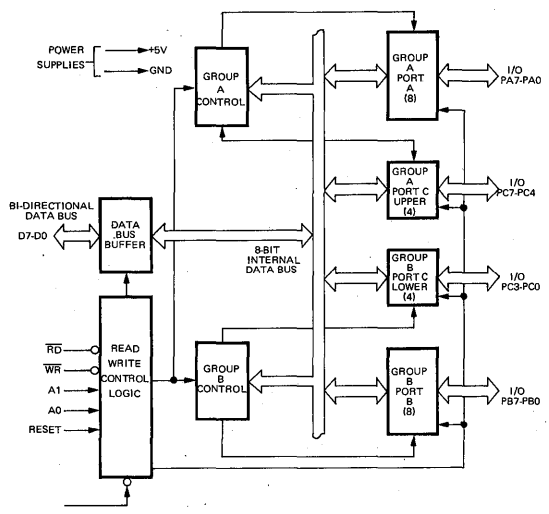
The UM82C55A is a high performance CMOS version of the industry standard 8255A and is manufactured using a selfaligned silicon gate CMOS process. It is a general purpose programmable I/O device which may be used with many different microprocessors. There are 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. The high performance of the UM82C55A make it compatible with microprocessors such as the 8086, 8048, 8051.

Static CMOS circuit design insures low operating power. TTL compatibility of V_{IH}=2.0 volts over the industrial temperature range and bus hold circuitry eliminate the need for pull-up resistors.

Pin Configuration



Block Diagram



PIN NAMES

D_7-D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
VCC	+5 VOLTS
GND	0 VOLTS

Peripheral IC

Absolute Maximum Ratings *

Supply Voltage . . . . . +8.0 VOLTS
Operating Voltage Range . . . . . +4V to +7V
Input Voltage Applied . . . . . GND–2.0V to 6.5V
I/O Pin Voltage Applied . . . . . GND–0.5V to VCC+0.5V
Storage Temperature Range . . . . . –65°C to +150°C
Operating Temperature Range . . . . . 0°C to +70°C
Maximum Power Dissipation . . . . . 1 Watt

*Comments

Stresses above those listed in the "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. Electrical Characteristics

($VCC = 5.0V+/-5\%$; $T_A = 0°C$ to $+70°C$)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IH}	Logical One Input Voltage	2.0		V	
V_{IL}	Logical Zero Input Voltage		0.8	V	
V_{OH}	Logical One Output Voltage	3.0 VCC–0.4		V V	$I_{OH} = -2.5mA$ $I_{OH} = -100\ \mu A$
V_{OL}	Logical Zero Output Voltage		0.4	V	$I_{OL} = +2.5$ mA
I_{IL}	Input Leakage Current	–1.0	1.0	μA	$0V \leqslant V_{IN} \leqslant V_{CC}$
I_O	I/O Pin Leakage Current	–10.0	10.0	μA	$0V \leqslant V_O \leqslant V_{CC}$
I_{BHH}	Bus Hold High Leakage Current	–50	–300	μA	$V_O = 3.0V$ Ports A, B, C
I_{BHL}	Bus Hold Low Leakage Current	+50	+300	μA	$V_O = 1.0V$ Port A only
I_{DAR}	Darlington Drive Current	–2.0		mA	Ports A, B, C Test Condition 3
I_{CC}	Power Supply Current		10	μA	$V_{CC} = 5.5V$ $V_{IN} = V_{CC}$ or G_{ND} Outputs Open

Capacitance

($T_A = 25°C$; $V_{CC} = GND = 0V$; $V_{IN} = +5V$ or GND)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_{IN}*	Input Capacitance		5	pF	FREQ = 1 MHZ Unmeasured Pins Returned to GND
$C_{I/O}$*	I/O Pin Capacitance		20	pF	

*Guaranteed and sampled, but not 100% tested

Characteristics

(V_{CC} = +5V ±5%, GND = 0V; T_A = 0°C to +70°C)

READ

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{AR}	Address Stable Before READ	0		ns	
t_{RA}	Address Stable After READ	0		ns	
t_{RR}	READ Pulse Width	150		ns	
t_{RD}	Data Valid From READ		100	ns	1
t_{DF}	Data Float After READ	10	75	ns	2
t_{RV}	Time Between READs and/or WRITEs	300		ns	

WRITE

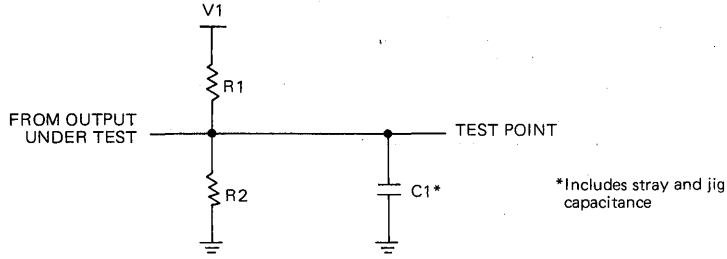
Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{AW}	Address Stable Before WRITE	0		ns	
t_{WA}	Address Stable After WRITE	20		ns	Ports A & B
		60		ns	Port C
t_{WW}	WRITE Pulse Width	100		ns	
t_{DW}	Data Valid to WRITE High	100		ns	
t_{WD}	Data Valid After WRITE High	30		ns	Ports A & B
		60		ns	Port C

OTHER TIMINGS

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{WB}	WR = 1 to Output		350	ns	1
t_{IR}	Peripheral Data Before RD	0		ns	
t_{HR}	Peripheral Data After RD	0		ns	
t_{AK}	ACK Pulse Width	100		ns	
t_{ST}	STB Pulse Width	100		ns	
t_{PS}	Per. Data Before STB High	20		ns	
t_{PH}	Per. Data After STB High	50		ns	
t_{AD}	ACK = 0 to Output		175	ns	1
t_{KD}	ACK = 1 to Output Float	20	250	ns	2
t_{WOB}	WR = 1 to OBF = 0		150	ns	1
t_{AOB}	ACK = 0 to OBF = 1		150	ns	1
t_{SIB}	STB = 0 to IBF = 1		150	ns	1
t_{RIB}	RD = 1 to IBF = 0		150	ns	1
t_{RIT}	RD = 0 to INTR = 0		200	ns	1
t_{SIT}	STB = 1 to INTR = 1		150	ns	1
t_{AIT}	ACK = 1 to INTR = 1		150	ns	1
t_{WIT}	WR = 0 to INTR = 0		200	ns	1
t_{RES}	Reset Pulse Width	500		ns	see note 1

Note: Period of initial Reset pulse after power-on must be at least 50usec. Subsequent Reset pulses may be 500 ns minimum.

A.C. Test Circuits

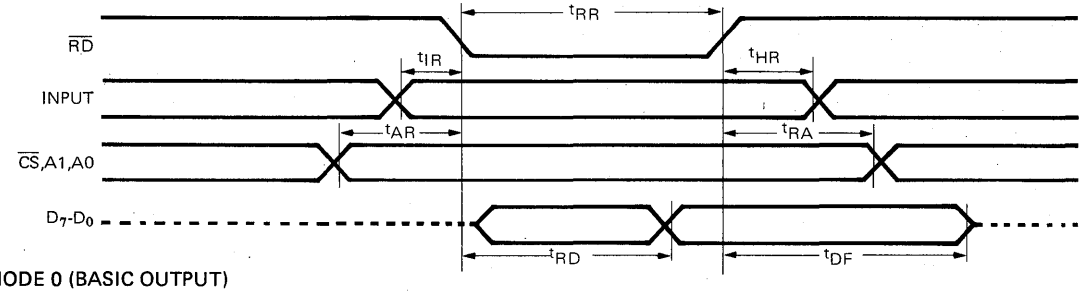


Test Condition	V1	R1	R2	C1
1	1.7V	523Ω	Open	150 pf
2	5.0V	2kΩ	1.7kΩ	50 pf
3	1.5V	750Ω	Open	Open

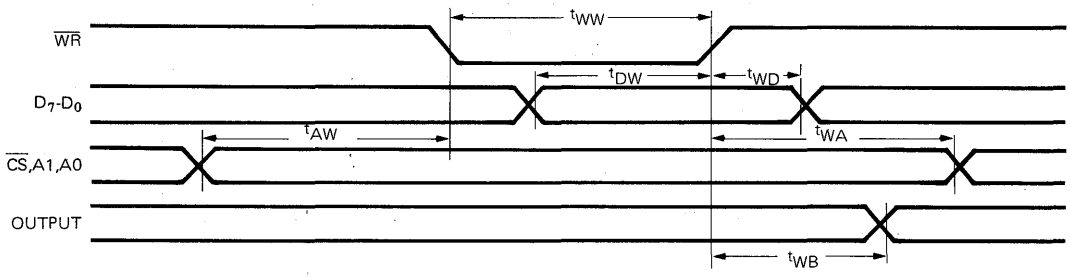
TEST CONDITION DEFINITION TABLE

Waveforms

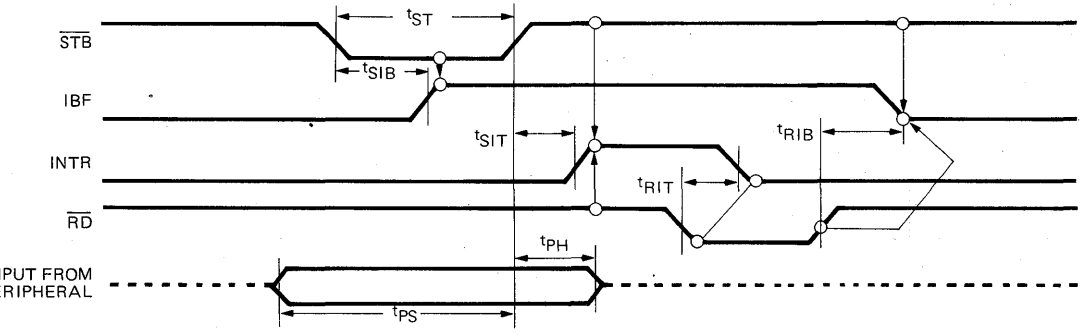
MODE 0 (BASIC INPUT)



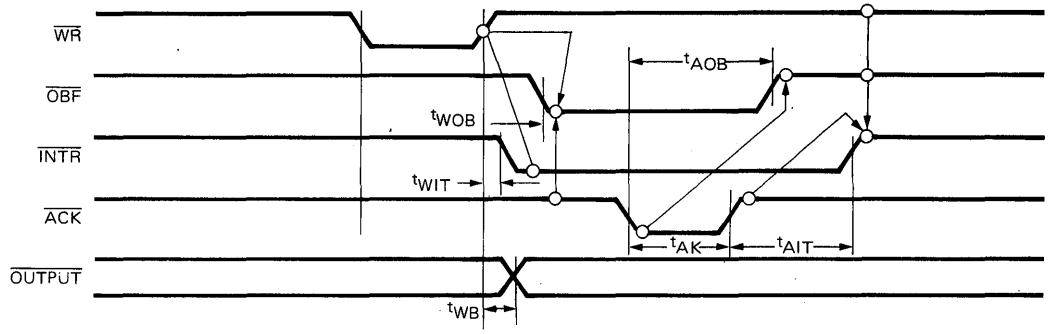
MODE 0 (BASIC OUTPUT)



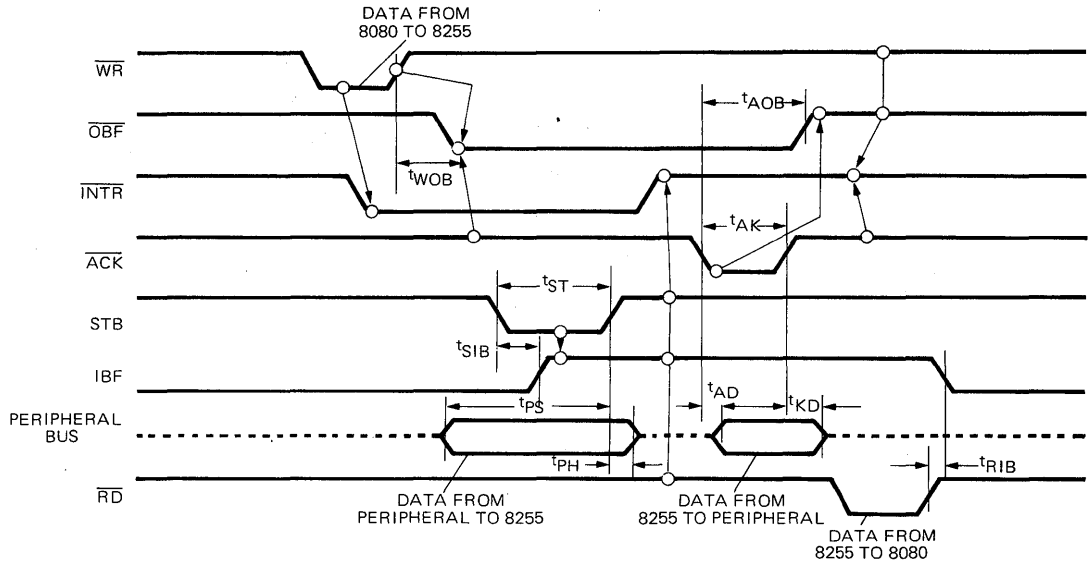
MODE 1 (STROBED INPUT)



MODE 1 (Strobe Output)

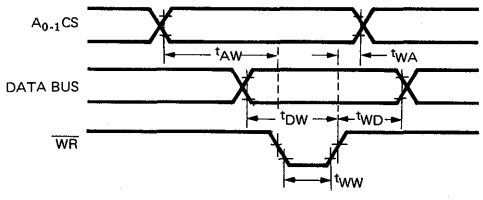


MODE 2 (BIDIRECTIONAL)

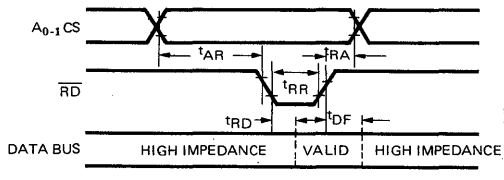


Note: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible. (INTR = IBF · $\overline{MASK}$ · $\overline{STB}$ · $\overline{RD}$ + $\overline{OBF}$ · $\overline{MASK}$ · $\overline{ACK}$ · $\overline{WR}$)

WRITE TIMING



READ TIMING



Peripheral IC

Pin Description

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the UM82C55A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

$\overline{(CS)}$

Chip Select. A "low" on this input pin enables the communication between the UM82C55A and the CPU.

$\overline{(RD)}$

Read. A "low" on this input pin enables the UM82C55A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the UM82C55A.

$\overline{(WR)}$

Write. A "low" on this input pin enables the CPU to write data or control words into the UM82C55A.

(A_0 and A_1)

Port Select 0 and Port Select 1. These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus (A_0 and A_1).

UM82C55A BASIC OPERATION

A	A_2	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Input Operation (Read)
0	0	0	1	0	Port A → Data Bus
0	1	0	1	0	Port B → Data Bus
1	0	0	1	0	Port C → Data Bus
1	1	0	1	0	Control Word → Data Bus
					Output Operation (Write)
0	0	1	0	0	Data Bus → Port A
0	1	1	0	0	Data Bus → Port B
1	0	1	0	0	Data Bus → Port C
1	1	1	0	0	Data Bus → Control
					Disable Function
x	x	x	x	1	Data Bus → 3-State
x	x	1	1	0	Data Bus → 3-State

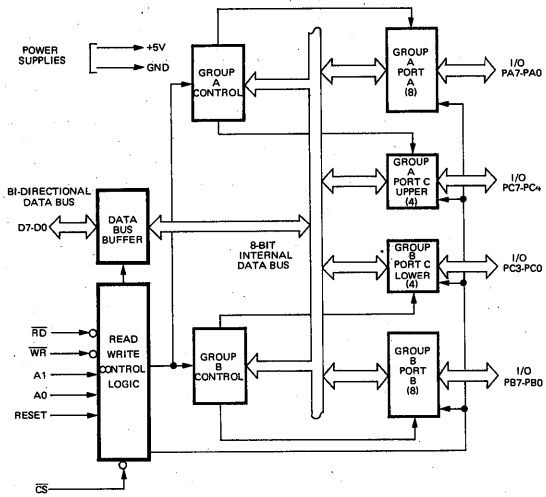


Figure 1. UM82C55A Block Diagram Data Bus Buffer and Read/Write Control Logic Functions

(Reset)

Reset. A "high" on this input clears the control register and all ports (A, B, C) are set to the input mode. "Bus hold" devices internal to the UM82C55A will hold the I/O port inputs to a logic "1" state with a maximum hold current of 300 μA.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the UM82C55A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the UM82C55A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A– Port A and Port C upper (C7-C4)
Control Group B–Port B and Port C lower (C3-C0)

The control word register can be both written and read as shown in the "Basic Operation" table. Figure 4 shows the control word format for both Read and Write operations. When the control word is read, bit D7 will always be a logic "1", as this implies control word mode information.

Ports A, B and C

The UM82C55A contains three 8-bit ports (A, B, and C). All can be configured to a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the UM82C55A.

Port A One 8-bit data output latch/buffer and one 8-bit data input latch. Both "pull-up" and "pull-down" bus-hold devices are present on Port A.

Port B One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input)x This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

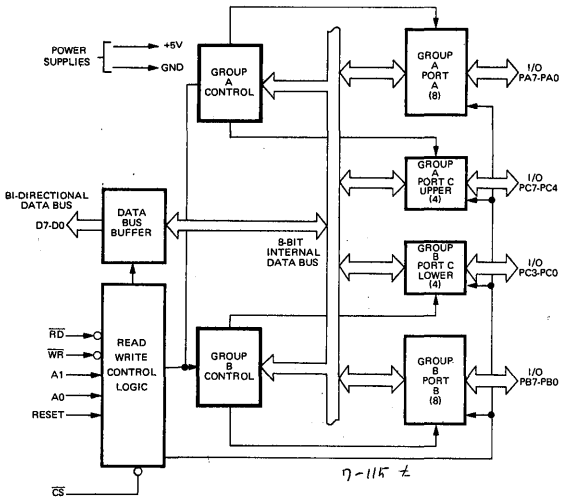


Figure 2. UM82C55A Block Diagram Showing Group A and Group B Control Functions

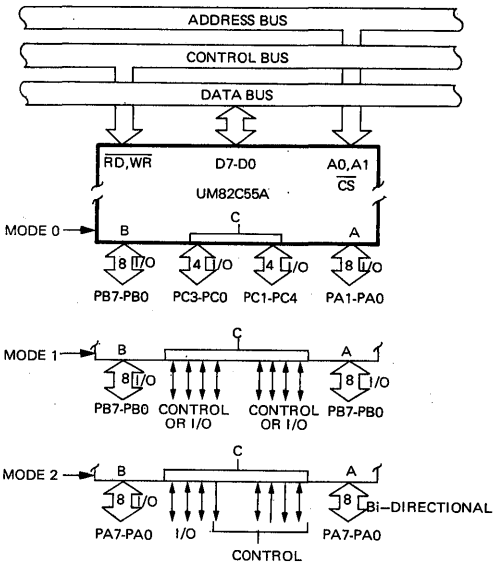


Figure 3. Basic Mode Definitions and Bus Interface

Operational Description

Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0 – Basic Input/Output
Mode 1 – Strobed Input/Output
Mode 2 – Bi-Directional Bus

When the reset input goes "high", all ports will be set to the input mode with all 24 port lines held at a logic "one" level by internal bus hold devices. After the reset is removed, the UM82C55A can remain in the input mode with no additional initialization required. This eliminates the need for pullup or pulldown resistors in all-CMOS designs. During the execution of the system program, any of the other modes may be selected using a single output instruction. This allows a single UM82C55A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance: Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

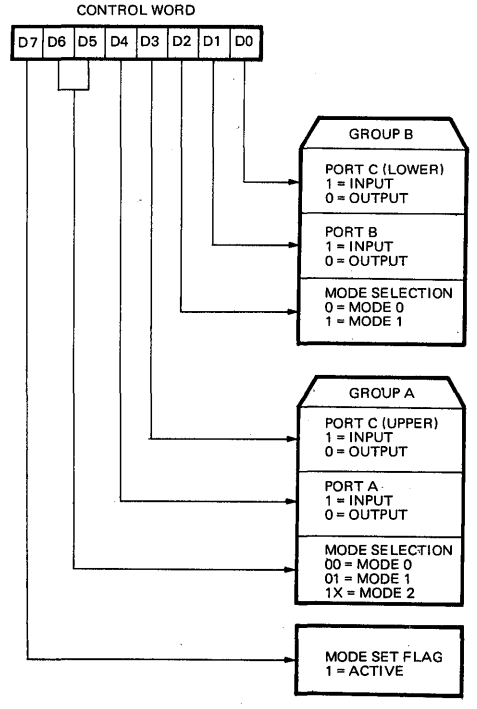


Figure 4. Mode Definition Format

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the UM82C55A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

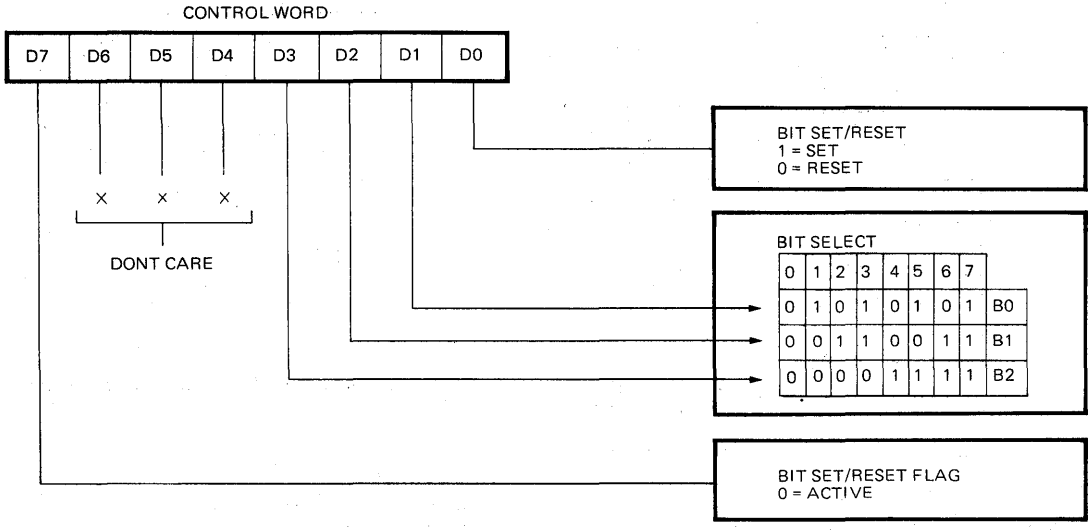


Figure 5. Bit Set/Reset Format

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUT put instruction. This feature reduces software requirements in control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the UM82C55A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the programmer to enable or disable a CPU interrupt by a specific I/O device without affecting any other device in the interrupt structure.

INTE Flip-flop Definition

(BIT-SET) – INTE is SET – Interrupt enable.
(BIT–RESET) – INTE is RESET – Interrupt disable.

Note: All Mask flip-flops are automatically reset during mode selection and device Reset.

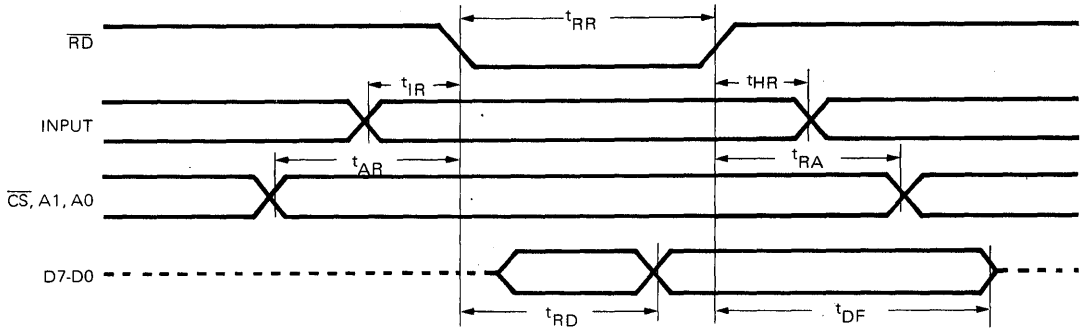
Operating Modes

Mode 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No handshaking is required, data is simply written to or read from a specific port.

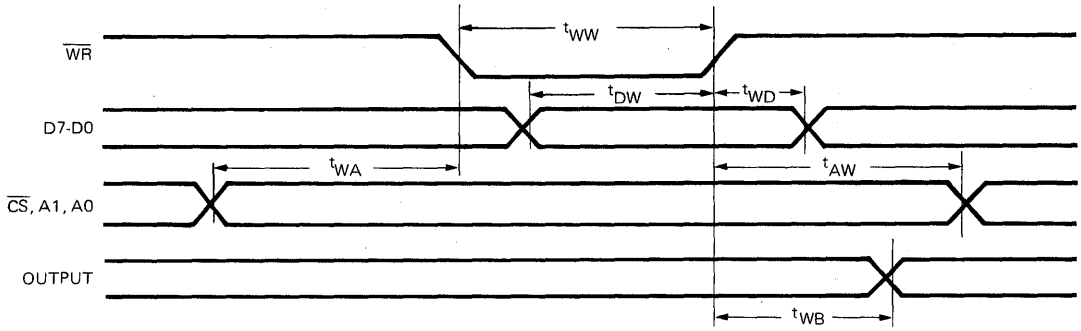
Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports
- Any port can be input or output
- Outputs are latched
- Inputs are not latched
- 16 different Input/Output configurations possible.

MODE 0 (BASIC INPUT)



MODE 0 (BASIC OUTPUT)



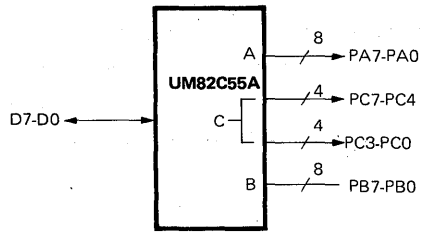
Mode 0 Port Definition

A		B		Group A			Group B	
D_4	D_3	D_1	D_0	Port A	Port C (Upper)	#	Port B	Port C (Lower)
0	0	0	0	Output	Output	0	Output	Output
0	0	0	1	Output	Output	1	Output	Input
0	0	1	0	Output	Output	2	Input	Output
0	0	1	1	Output	Output	3	Input	Input
0	1	0	0	Output	Input	4	Output	Output
0	1	0	1	Output	Input	5	Output	Input
0	1	1	0	Output	Input	6	Input	Output
0	1	1	1	Output	Input	7	Input	Input
1	0	0	0	Input	Output	8	Output	Output
1	0	0	1	Input	Output	9	Output	Input
1	0	1	0	Input	Output	10	Input	Output
1	0	1	1	Input	Output	11	Input	Input
1	1	0	0	Input	Input	12	Output	Output
1	1	0	1	Input	Input	13	Output	Input
1	1	1	0	Input	Input	14	Input	Output
1	1	1	1	Input	Input	15	Input	Input

Mode 0 Configurations

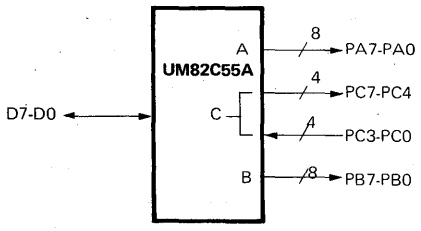
CONTROL WORD #0

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0



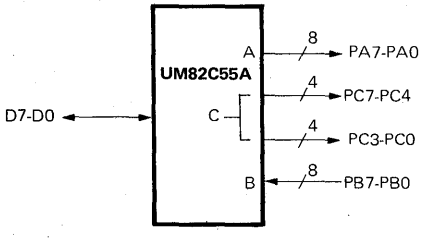
CONTROL WORD #1

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	1



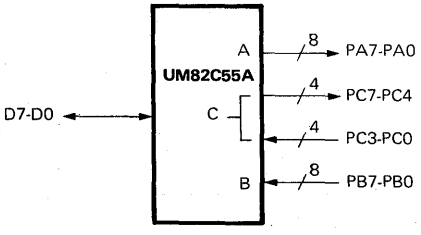
CONTROL WORD #2

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	1	0



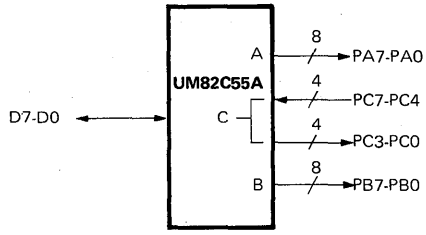
CONTROL WORD #3

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	1	1



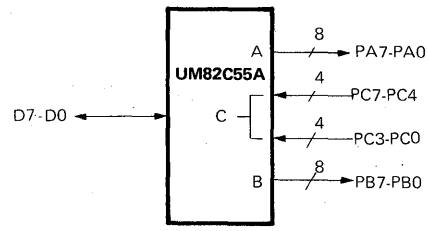
CONTROL WORD #4

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	0



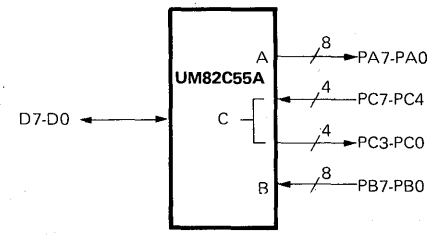
CONTROL WORD #5

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	1



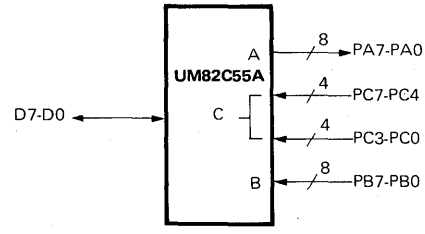
CONTROL WORD #6

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	1	0



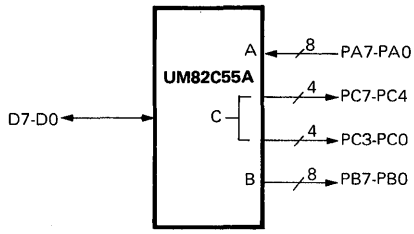
CONTROL WORD #7

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	1	1



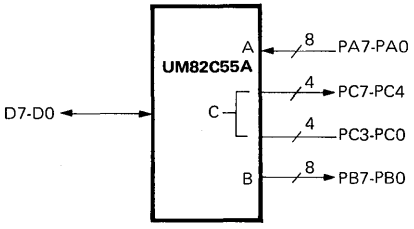
CONTROL WORD #8

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	0



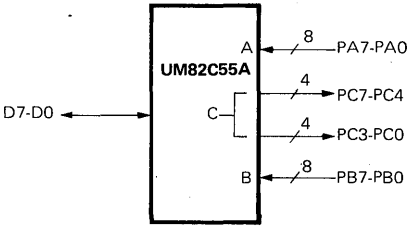
CONTROL WORD #9

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	1



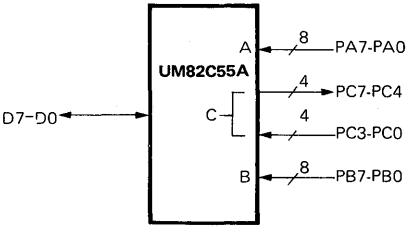
CONTROL WORD #10

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	1	0



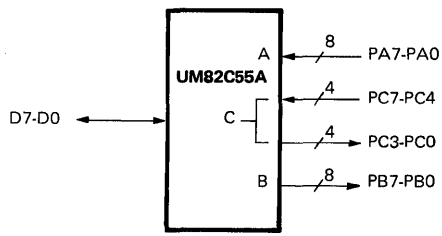
CONTROL WORD #11

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	1	1



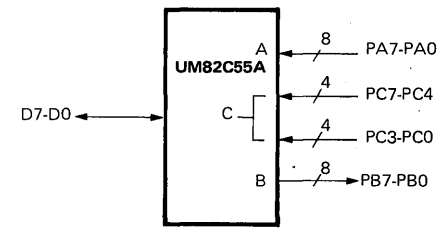
CONTROL WORD #12

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	0	0	0



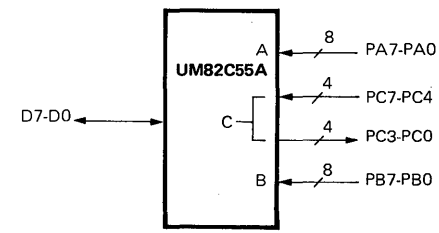
CONTROL WORD #13

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	0	0	1



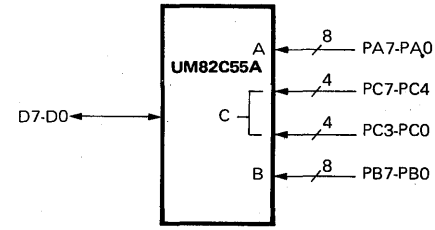
CONTROL WORD #14

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	0	1	0



CONTROL WORD #15

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	0	1	1



Operating Modes

Mode 1 (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, port A and port B use the lines on port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions

- Two Groups (Group A and Group B)
- Each group contains one 8-bit port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit port.

Input Control Signal Definition

$\overline{STB}$ (Strobe Input)
A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by $\overline{STB}$ input being low and is reset by the rising edge of the $\overline{RD}$ input.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the condition; STB is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

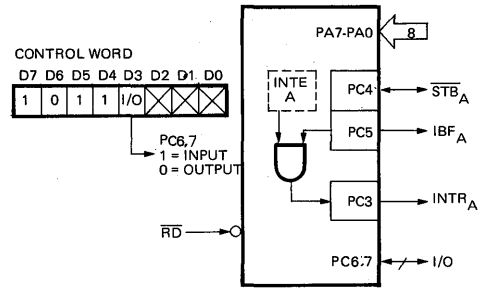
INTE A

Controlled by bit set/reset of PC_4.

INTE B

Controlled by bit set/reset of PC_2.

MODE 1 (PORT A)



MODE 1 (PORT B)

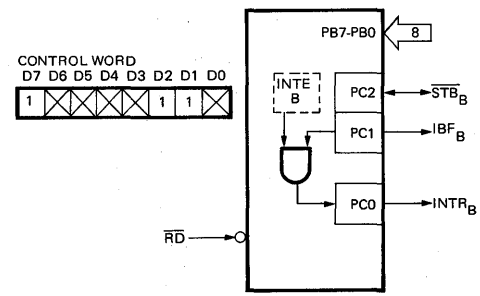


Figure 6. MODE 1 Input

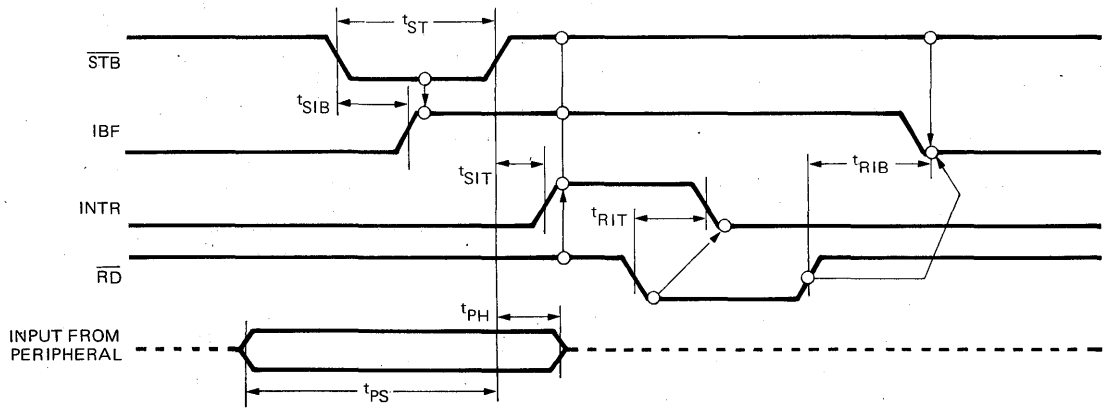


Figure 7. MODE 1 (Strobed Input)

Output Control Signal Definition

$\overline{OBF}$ (Output Buffer Full F/F). The OBF output will go "low" to indicate that the CPU has written data out to the specified port. The $\overline{OBF}$ F/F will be set by the rising edge of the $\overline{WR}$ input and reset by $\overline{ACK}$ Input being low.

$\overline{ACK}$ (Acknowledge Input). A "low" on this input informs the UM82C55A that the data from port A or port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the $\overline{CPU}$.

INTR (Interrupt Request). A "high" on this output can be used to interrupt the $\overline{CPU}$ when an output device has accepted data transmitted by the CPU. INTR is set when $\overline{ACK}$ is a "one", OBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{WR}$.

INTE A

Controlled by Bit Set/Reset of PC_6.

INTE B

Controlled by Bit Set/Reset of PC_2.

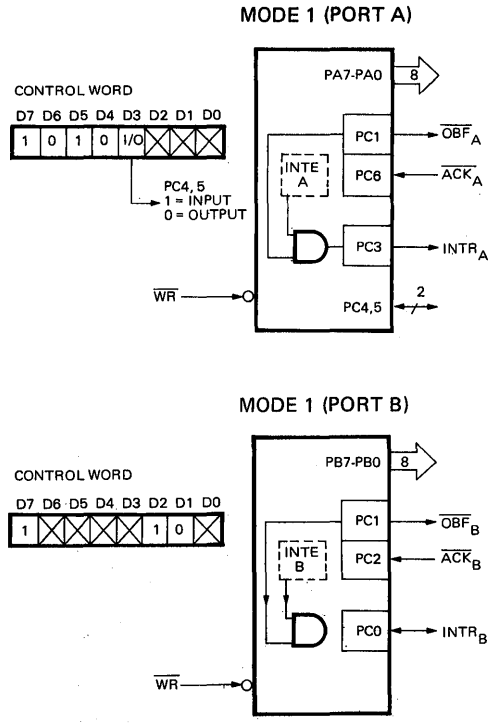


Figure 8. MODE 1 Output

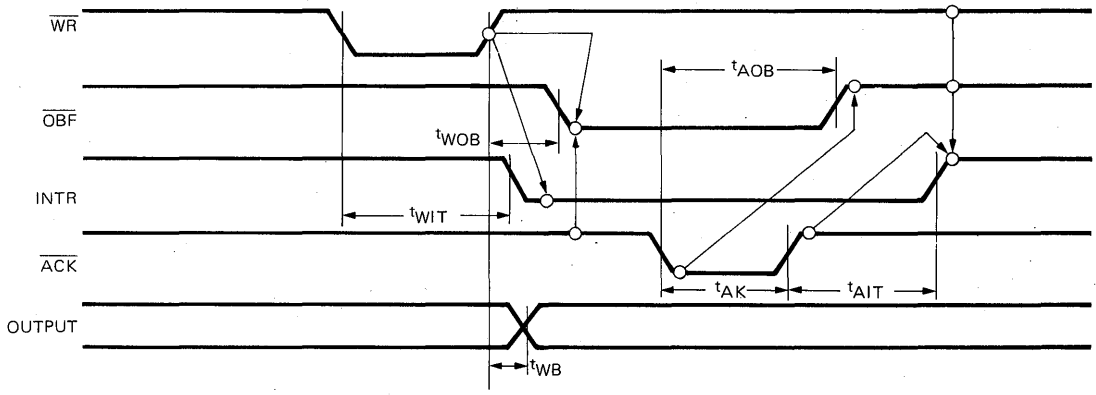


Figure 9. MODE 1 (Strobed Output)

Combinations of MODE 1; Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications:

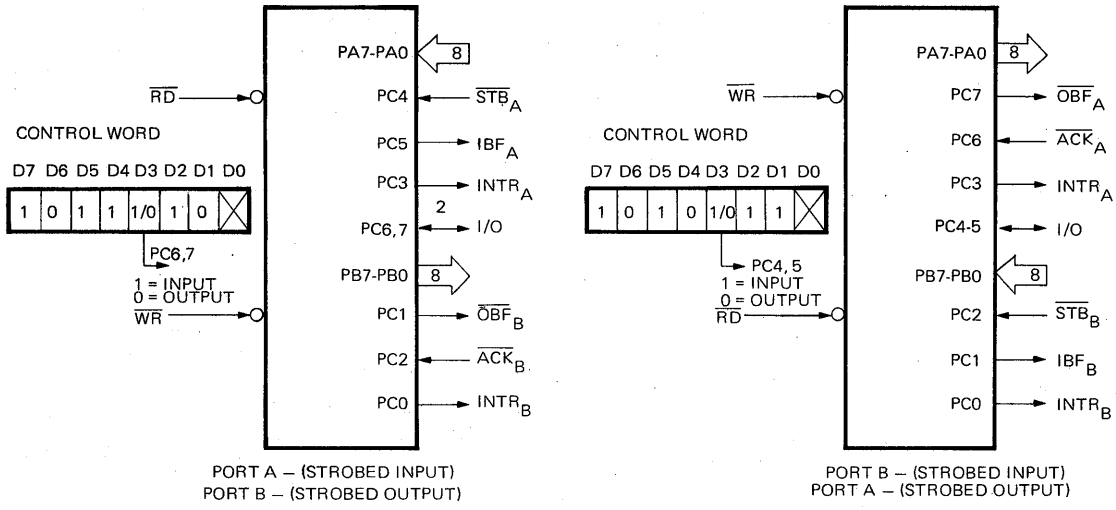


Figure 10. Combinations of MODE 1

Operating Modes

MODE 2 (Strobed Bidirectional Bus I/O)

The functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline similar to MODE 1. Interrupt generation and enable/disable functions are also available.

MODE 2 Basic Function Definitions:

- Used in Group A only.
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

Bidirectional Bus I/O Control Signal Definition

INTR (Interrupt Request). A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

$\overline{OBF}$ (Output Buffer Full). The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to port A.

$\overline{ACK}$ (Acknowledge). A "Low" on this input enables the tri-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 (The INTE Flip-Flop Associated with $\overline{OBF}$). Controlled by bit set/reset of PC_6.

Input Operations

$\overline{STB}$ (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F). A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE Flip-Flop Associated with IBF). Controlled by bit set/reset of PC_4.

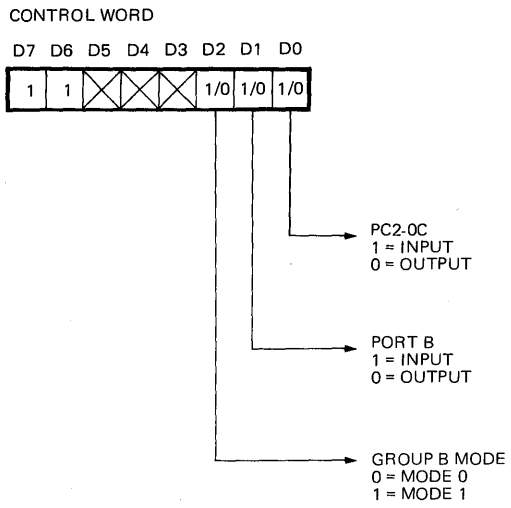


Figure 11. MODE Control Word

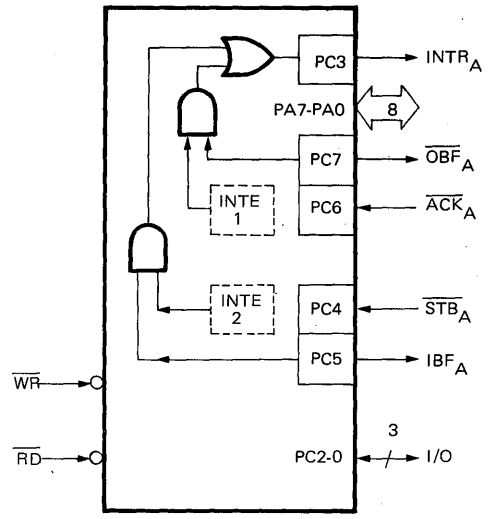


Figure 12. MODE 2

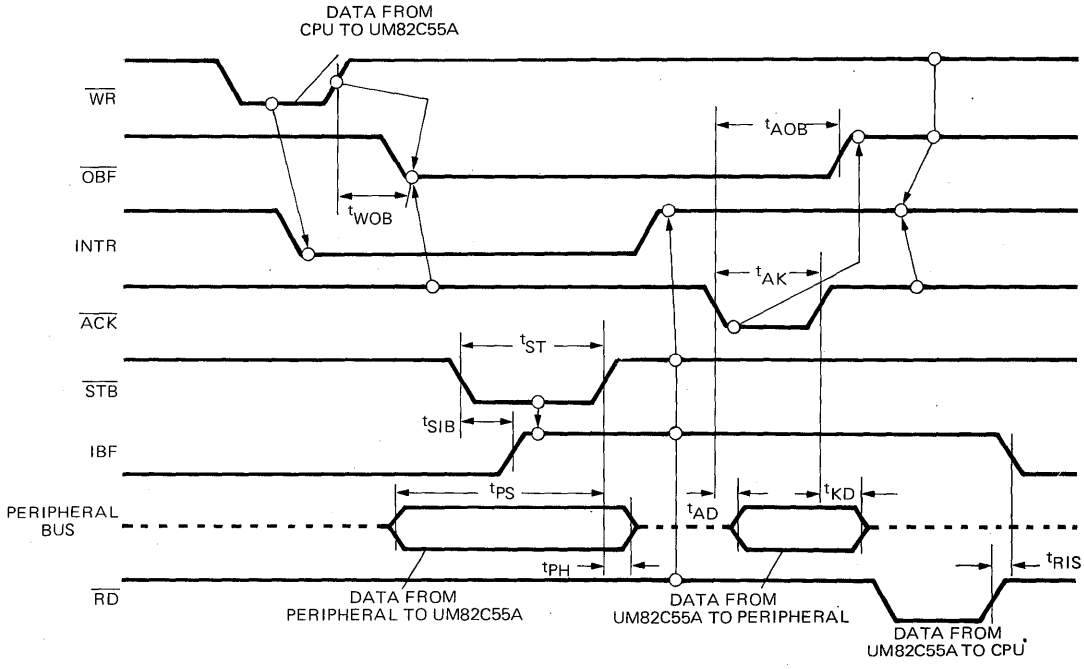
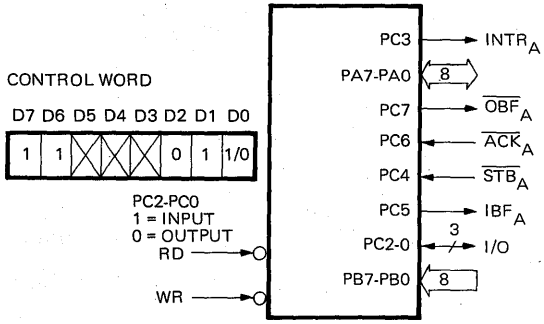


Figure 13. MODE 2 (Bidirectional)

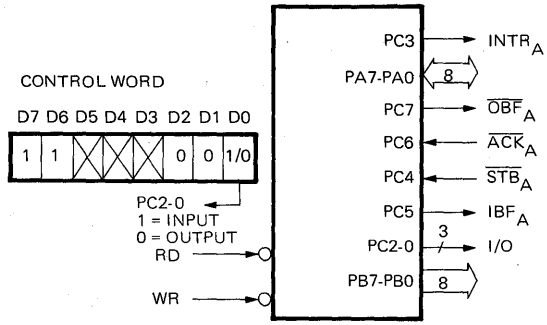
Note: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before RD is permissible. (INTR = IBF · MASK · $\overline{STB}$ · $\overline{RD}$ + $\overline{OBF}$ · MASK · $\overline{ACK}$ · $\overline{WR}$)

Peripheral IC

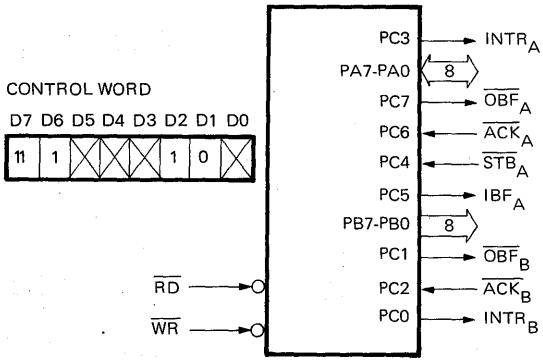
MODE 2 AND MODE 0 (INPUT)



MODE 2 AND MODE 0 (OUTPUT)



MODE 2 AND MODE 1 (OUTPUT)



MODE 2 AND MODE 1 (INPUT)

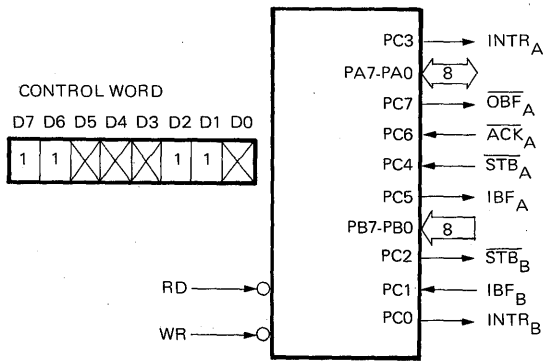


Figure 14. MODE 2 Combinations

Mode Definition Summary

	MODE 0		MODE 1		MODE 2
	IN	OUT	IN	OUT	Group A Only
PA_0	IN	OUT	IN	OUT	←
PA_1	IN	OUT	IN	OUT	←
PA_2	IN	OUT	IN	OUT	←
PA_3	IN	OUT	IN	OUT	←
PA_4	IN	OUT	IN	OUT	←
PA_5	IN	OUT	IN	OUT	←
PA_6	IN	OUT	IN	OUT	←
PA_7	IN	OUT	IN	OUT	←
PB_0	IN	OUT	IN	OUT	—
PB_1	IN	OUT	IN	OUT	—
PB_2	IN	OUT	IN	OUT	—
PB_3	IN	OUT	IN	OUT	—
PB_4	IN	OUT	IN	OUT	—
PB_5	IN	OUT	IN	OUT	—
PB_6	IN	OUT	IN	OUT	—
PB_7	IN	OUT	IN	OUT	—
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O
PC_1	IN	OUT	IBF_B	$\overline{OBF}_B$	I/O
PC_2	IN	OUT	$\overline{STB}_B$	$\overline{ACK}_B$	I/O
PC_3	IN	OUT	$INTR_A$	$INTR_A$	INTRA
PC_4	IN	OUT	$\overline{STB}_A$	I/O	$\overline{STB}_A$
PC_5	IN	OUT	IBF_A	I/O	IBF_A
PC_6	IN	OUT	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$
PC_7	IN	OUT	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$

MODE 0 OR MODE 1 ONLY

Special Mode Combination Considerations:
There are several combinations of modes possible. For any combination, some or all of Port Clines are used for control or status. The remaining bits are either inputs or outputs as defined by a "Set Mode" command.

During a read of Port C, the state of all the Port Clines, except the $\overline{ACK}$ and $\overline{STB}$ lines, will be placed on the data bus. In place of the $\overline{ACK}$ and $\overline{STB}$ line states, flag status will appear on the data bus in the PC2, PC4, and PC6 bit positions as illustrated by Figure 17.

Through a "Write Port C" command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a "Write Port C" command, nor can the interrupt enable flags be accessed. To write to any Port C output programmed as an output in a Mode 1 group or to change an interrupt enable flag, the "Set/Reset Port C Bit" command must be used.

With a "Set/Reset Port C Bit" command, any Port C line programmed as an output (including INTR, IBF and OBF) can be written, or an interrupt enable flag can be either set or reset. Port C lines programmed as inputs, including $\overline{ACK}$ and $\overline{STB}$ lines, associated with Port C are not affected by a "Set/Reset Port C Bit" command. Writing to the corresponding Port C bit positions of the $\overline{ACK}$ and $\overline{STB}$ lines with the "Set/Reset Port C Bit" command will affect the Group A and Group B interrupt enable flags, as illustrated in Figure 17.

INPUT CONFIGURATION

D7	D6	D5	D4	D3	D2	D1	D0
I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$
GROUP A					GROUP B		

OUTPUT CONFIGURATION

D7	D6	D5	D4	D3	D2	D1	D0
$\overline{OBF}_A$	$INTE_A$	I/O	I/O	$INTR_A$	$INTE_B$	$\overline{OBF}_B$	$INTR_B$
GROUP A					GROUP B		

Figure 15. MODE 1 Status Word Format

D7	D6	D5	D4	D3	D2	D1	D0
$\overline{OBF}_A$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$			
GROUP A					GROUP B		

(DEFINED BY MODE 0 OR MODE 1 SELECTION)

Figure 16. MODE 2 Status Word Format

Interrupt Enable Flag*	Position	Alternate Port C Pin Signal (Mode)
INTE B	PC2	$\overline{ACK}_B$ (Output Mode 1) or $\overline{STB}_B$ (Input Mode 1)
INTE A2	PC4	$\overline{STB}_A$ (Input Mode 1 or Mode 2)
INTE A1	PC6	$\overline{ACK}_A$ (Output Mode 1 or Mode 2)

Figure 17. Interrupt Enable Flags in Modes 1 and 2

Current Drive Capability:
Any output on Port A, B or C can sink or source 2.5mA. This feature allows the UM82C55A to directly drive Darlington type drivers and high-voltage displays that require such sink or source current.

Reading Port C Status
In Mode 0, Port C transfers data to or from the peripheral device. When the UM82C55A is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C allows that programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

Applications of the UM82C55A

The UM82C55A is a very powerful tool for interfacing peripheral equipment to the microcomputer system. It represents the optimum use of available pins and is flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a "service routine" associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the UM82C55A is programmed by the I/O service routine and becomes an extension of the system software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the detailed operational description, a control word can easily be developed to initialize the UM82C55A to exactly "fit" the application. Figures 10 through 24 present a few examples of typical applications of the UM82C55A.

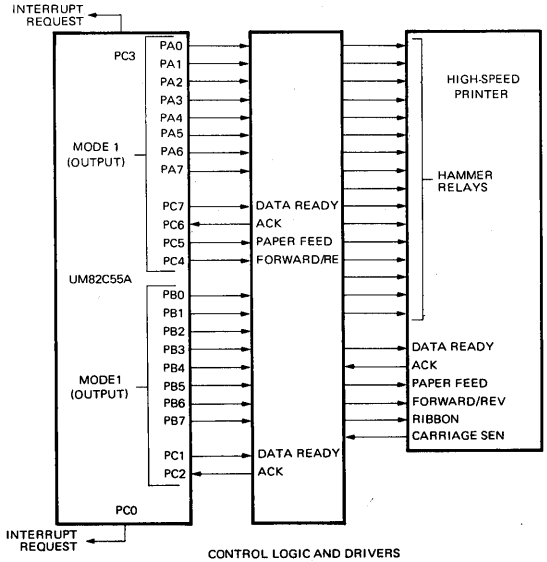


Figure 18. Printer Interface

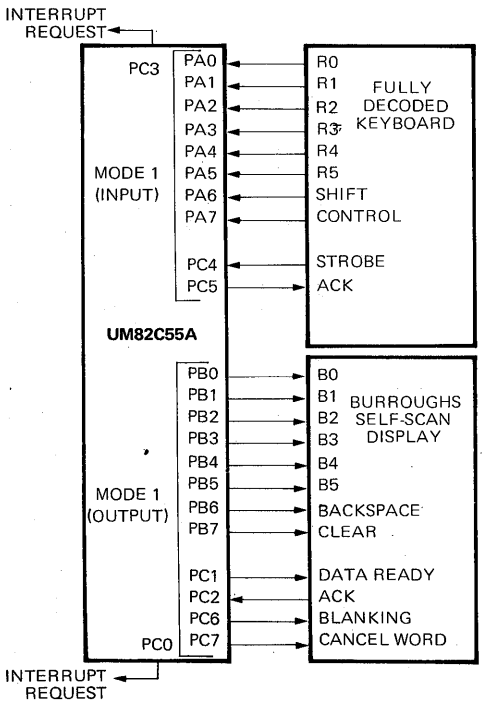


Figure 19. Keyboard and Display Interface

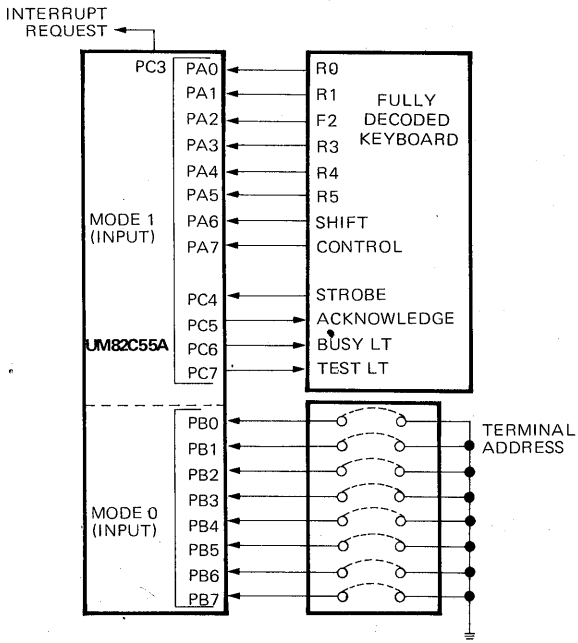


Figure 20. Keyboard and Terminal Address Interface

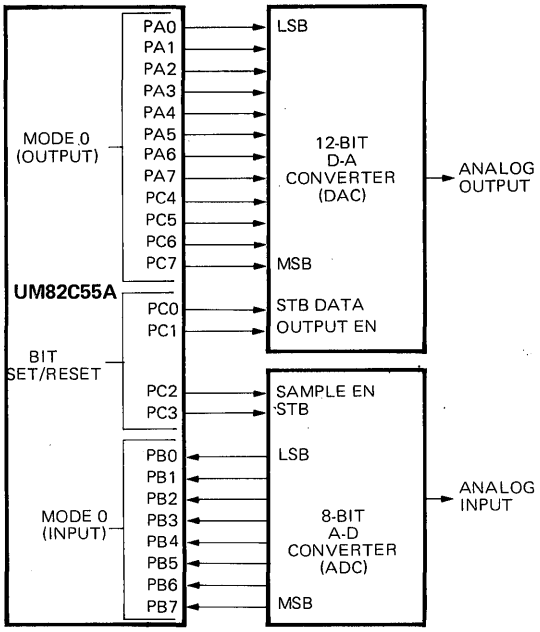


Figure 21. Digital to Analog, Analog to Digital

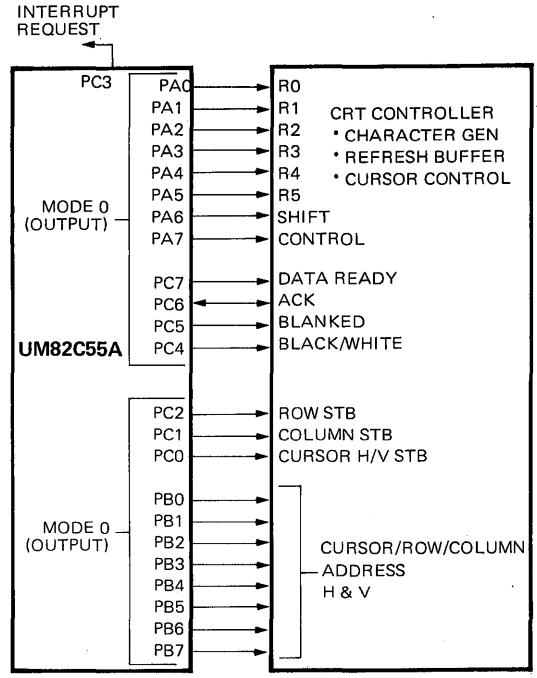


Figure 22. Basic CRT Controller Interface

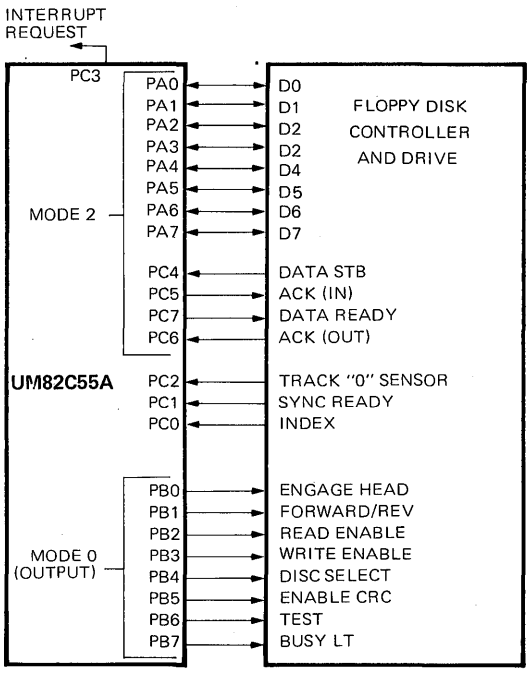


Figure 23. Basic Floppy Disk Interface

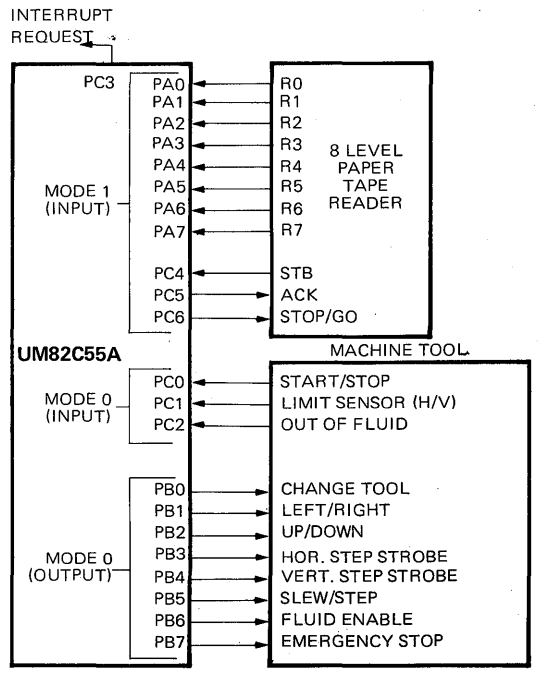


Figure 24. Machine Tool Controller Interface

UM82C84A

PRELIMINARY

CMOS Clock Generator Driver

Features

- Generates the system clock for CMOS or NMOS Microprocessors
- Up to 25 MHz operation
- Uses a parallel mode crystal circuit or external frequency source
- Provides ready synchronization
- Generates system reset output from schmitt trigger input
- Capable of clock synchronization with other $8284A_s$
- TTL compatible inputs/outputs
- Very low power consumption
- 18 Pin package
- Single +5V power supply

General Description

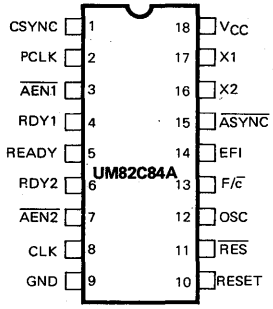
The UM82C84A is a high performance CMOS clock generator-driver which is designed to service the requirements of both CMOS and NMOS microprocessors such as the 80C86, 80C88, 8086 and the 8088. The chip contains a crystal controlled oscillator, a divide-by-three counter and complete "Ready" synchronization and reset logic.

Static CMOS circuit design permits operation with an external frequency source from DC to 25MHz. Crystal controlled operation to 25MHz is guaranteed with the use of a parallel, fundamental mode crystal and two small load capacitors.

All inputs (except X1, X2 and $\overline{RES}$) are TTL compatible with a V_{IH} of 2.0 volts over the industrial temperature and voltage ranges.

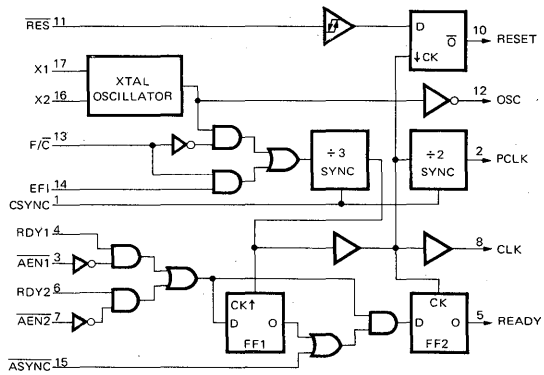
Power consumption is a fraction of that of the equivalent bipolar circuits. This speed-power characteristic of CMOS permits the designer to custom tailor his system design with respect to power and/or speed requirements.

Pin Configuration



Control Pin	Logical 1	Logical 0
F/$\overline{C}$	External Clock	Crystal Drive
$\overline{RES}$	Normal	Reset
RDY1 RDY2	Bus Ready	Bus not Ready
$\overline{AENT}$ $\overline{AEN2}$	Address Disabled	Address Enabled
ASYNC	2 Stage Ready Synchronization	1 Stage Ready Synchronization

Block Diagram



Absolute Maximum Ratings*

Supply Voltage . . . . . +8.0 Volts
Operating Voltage Range . . . . . +4V to +7V
Applied Voltage on Any Pin
V_{IN} . . . . . GND −0.3V to V_{CC} 0.3V
Ambient Temperature Under Bias T_A . . . . . 0°C to +70°C
Storage Temperature Range
T_{STG} . . . . . −65°C to +150°C
Maximum Power Dissipation . . . . . 1 Watt

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Electrical Characteristics

V_{CC} = 5.0V ± 10% T_A = 0°C to +70°C

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IH}	Logical One Input Voltage	2.0		V	
V_{IL}	Logical Zero Input Voltage		0.8	V	
V_{T+}	Reset Input High Voltage	0.7 V_{CC}		V	
V_{T+}-V_{T-}	Reset Input Hysteresis	0.2 V_{CC}			
V_{OH}	Logical One Output Voltage	V_{CC}-0.4		V	I_{OH} = -4.0mA for CLK output I_{OH} = -2.5mA for all others
V_{OL}	Logical Zero Output Voltage		0.4	V	I_{OL} = +4.0mA for CLK output I_{OL} = +2.5mA for for others
I_{CL}	Input Leakage Current	−1.0	1.0	μA	$0V < V_{IN} < V_{CC}$ except $\overline{ASYNC}$, X1-see note 1
I_{CC}	Power S Supply Current		40	mA	Crystal Frequency = 25MHz Outputs Open

Notes:
ASYNC pin includes an internal 17.5KΩ nominal pull-up resistor. For $\overline{ASYNC}$ input at GND, $\overline{ASYNC}$ input leakage current= 130μA nominal.
X1-crystal feedback input.

Capacitance

(T_A = 25°C. V_{CC} = GND=0V; V_{IN} =+5V or GND)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_{IN}*	Input Capacitance		5	pf	Freq. = 1 MHz

*Guaranteed and sampled, but not 100% tested

A.C. Characteristics

(T_A = 0°C to +70°C, V_{CC} = 5V ± 10%)

TIMING REQUIREMENTS

Symbol	Parameter	Min.	Max.	Units	Test Conditions
tEHEL	External Frequency HIGH Time	13		ns	90%–90% V_{IN}
tELEH	External Frequency LOW Time	13		ns	10%–10% V_{IN}
tELEL	EFI Period	36		ns	
	XTAL Frequency	2.4	25	HNz	
tR1VCL	RDY1, RDY2 Active Setup to CLK	35		ns	ASYNC = HIGH
tR1VCH	RDY1, RDY2 Inactive Setup to CLK	35		ns	ASYNC= LOW
tR1VCL	RDY1, RDY2 Inactive Setup to CLK	35		ns	
tCLR1X	RDY1, RDY2 Hold to CLK	0		ns	
tAYVCL	ASYNC Setup to CLK	50		ns	
tCLAYX	ASYNC Hold to CLK	0		ns	
tA1VR1V	AEN1, AEN2 Setup to RDY1, RDY2	15		ns	
tCLA1X	AEN1, AEN2 Hold to CLK	0		ns	
tYHEN	CSYNC Setup to EFI	20		ns	
tEHYL	CSYNC Hold to EFI	20		ns	
tYHYL	CSYNC Width	2.tELEL		ns	
t_{I1HCL}	RES Setup to CLK	65		ns	(Note 2)
tCLI1H	RES Hold to CLK	20		ns	(Note 2)

TIMING RESPONSES

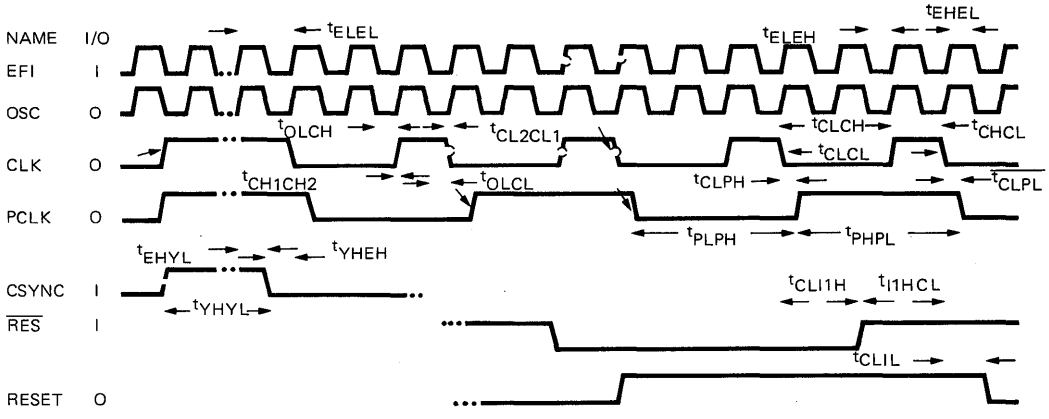
Symbol	Parameter	Min.	Max.	Units	Test Conditions
tCLCL	CLK Cycle Period	125		ns	
tCHCL	CLK HIGH Time	(1/3 tCLCL)+2.0		ns	Fig. 7 & Fig. 8
tCLCH	CLK LOW Time	(2/3 tCLCL)215.0		ns	Fig. 7 & Fig. 8
tCH1CH2	CLK Rise or Fall Time		10	ns	1.0V to 3.5V
tCL2CL1					
tPHPL	PCLK HIGH Time	tCLCL–20		ns	
tPLPH	PCLK LOW Time	tCLCL–20		ns	
tRYLCL	Ready Inactive to CLK (See note 4)	–8		ns	Fig. 8 & Fig. 10
tRYHCH	Ready Active to CLK (See note 3)	(2/3 tCLCL)–15.0		ns	Fig. 9 & Fig. 10
tCLIL	CLK to Reset Delay		40	ns	
tCLPH	CLK to PCLK HIGH Delay		22	ns	
tCLPL	CLK to PCLK LOW Delay		22	ns	
tOLCH	OSC to CLK HIGH Delay	–5	22	ns	
tOLCL	OSC to CLK LOW Delay	2	35	ns	

Notes:

1. Output signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. Setup and hold necessary only to guarantee recognition at next clock.
3. Applies only to T3 TW states.
4. Applies only to T2 states.
5. All timing delays are measured at 1.5 volts unless otherwise noted.
6. Input signals must switch between V_{IL} max–.4 V_{OH} and V_{IH} min +.4 volts in 15ns unless otherwise specified.

Figure 1. Illustrates test load measurement condition.

Waveforms



Note: All timing measurements are made at 1.5 volts. Unless otherwise noted.

Figure 2. Waveforms for Clocks and Reset Signals

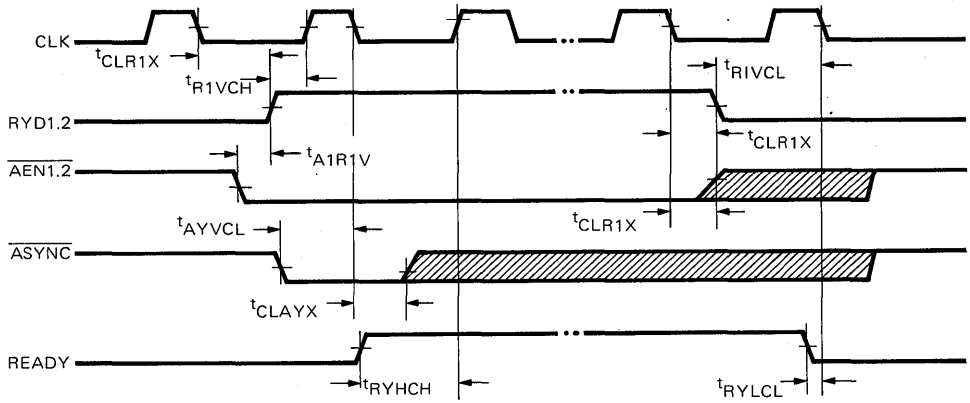


Figure 3. Waveforms for Ready Signals (For Asynchronous Devices)

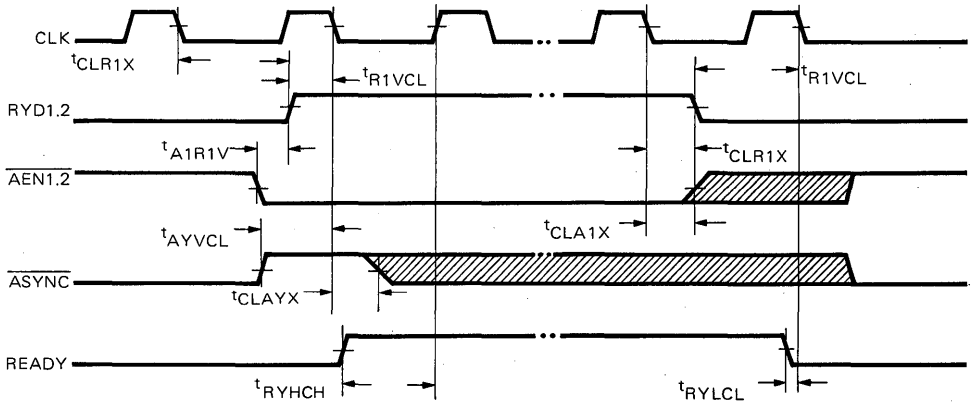


Figure 4. Waveforms for Ready Signals (For Synchronous Devices)

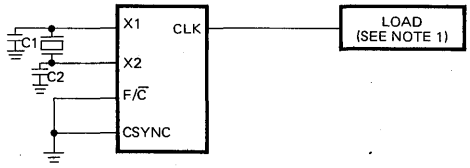


Figure 5. Clock High and Low Time (Using X1, X2)

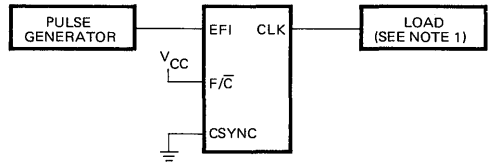


Figure 6. Clock High and Low Time (Using EFI)

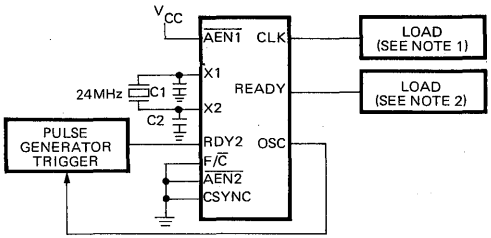


Figure 7. Ready to Clock (Using X1, X2)

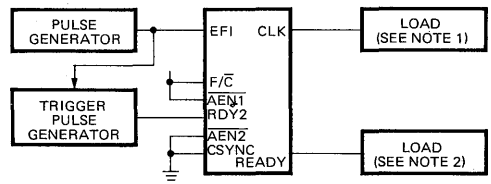
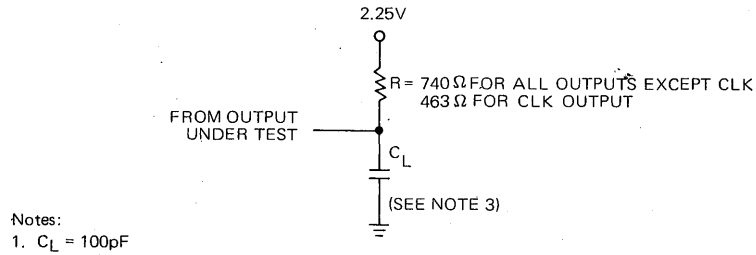


Figure 8. Ready to Clock (Using EFI)



Notes:
1. C_L = 100pF
2. C_L = 30pF
3. C_L INCLUDES PROBE AND JIG CAPACITANCE

Figure 9. Test Load Measurement Conditions

Table 1. Crystal Specifications

Parameter	Typical Crystal
Frequency	2.4–25MHz, Fundamental, "AT" cut
Type of Operation	Parallel
Unwanted Modes	–6db (Min)
Load Capacitance	18–32pf

Pin Description

Pin	I/O	Definitions
$\overline{AEN1}$, $\overline{AEN2}$	I	ADDRESS ENABLE: $\overline{AEN}$ is an active LOW signal. $\overline{AEN}$ serves to qualify its respective Bus Ready Signal (RYD1 or RDY2). $\overline{AEN1}$ validates RDY1 while $\overline{AEN2}$ validates RDY2. Two AEN signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Busses. In non Multi-Master configurations, the $\overline{AEN}$ signal inputs are tied true (LOW).
RDY1, RDY2	I	BUS READY (Transfer Complete). RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available. RDY1 is qualified by AEN1 while RDY2 is qualified by AEN2.
$\overline{ASYNC}$	I	READY SYNCHRONIZATION SELECT: $\overline{ASYNC}$ is an input which defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is low, two stages of READY synchronization are provided. When $\overline{ASYNC}$ is left open or HIGH a single stage of READY synchronization is provided.
READY	O	READY: READY is an active HIGH signal which is the synchronized RDY signal input. READY is cleared after the guaranteed hold time to the processor has been met.
X1, X2	I	CRYSTAL IN: X1 and X2 are the pins to which a crystal is attached. The crystal frequency is 3 times the desired processor clock frequency.
F/$\overline{C}$	I	FREQUENCY/CRYSTAL SELECT: F/$\overline{C}$ is a strapping option. When strapped LOW, F/$\overline{C}$ permits the processor's clock to be generated by the crystal. When F/$\overline{C}$ is strapped HIGH, CLK is generated from the EFI input.
EFI	I	EXTERNAL FREQUENCY IN: When F/$\overline{C}$ is strapped HIGH, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired CLK output.
CLK	O	PROCESSOR CLOCK: CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus. CLK has an output frequency which is 1/3 of the crystal of EFI input frequency and a 1/3 duty cycle.
PCLK	O	PERIPHERAL CLOCK: PCLK is a peripheral clock signal whose output frequency is 1/2 that of CLK and has a 50% duty cycle.
OSC	O	OSCILLATOR OUTPUT: OSC is the output of the internal oscillator circuity. Its frequency is equal to that of the crystal.
$\overline{RES}$	I	RESET IN: $\overline{RES}$ is an active LOW signal which is used generate RESET. The UM82C84A provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration.
RESET	O	RESET: RESET is an active HIGH signal which is used to reset the 80C86 family processors. Its timing characteristics are determinded by $\overline{RES}$.
CSYNC	I	CLOCK SYNCHRONIZATION: CSYNC is an active HIGH signal which allows multiple UM82C84As to be synchronized to provide clocks that are in phase. When CSYNC is HIGH the internal counters are reset. When CSYNC goes LOW the internal counters are allowed to resume counting. CSYNC needs to be externally synchronized to EFI. When using the internal oscillator CSYNC should be hardwired to ground.
GND		Ground
V_{CC}		+5V supply

Functional Description

Oscillator

The oscillator circuit of the UM82C84A is designed primarily for use with an external parallel resonant, fundamental mode crystal from which the basic operating frequency is derived.

The crystal frequency should be selected at three times the required CPU clock. X1 and X2 are the two crystal input crystal connections. For the most stable operation of the oscillator (OSC) output circuit, two capacitors (C1 = C2) as shown in the waveform figures are recommended. The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source. Capacitors C1, C2 are chosen such that their combined capacitance:

$$CT = \frac{C1 \cdot C2}{C1+C2} \quad \text{(Including stray capacitance)}$$

matches the load capacitance as specified by the crystal manufacturer. This insures operation within the frequency tolerance specified by the crystal manufacturer.

Clock Generator

The clock generator consists of a synchronous divide-by-three counter with a special clear input that inhibits the counting. This clear input (CSYNC) allows the output clock to be synchronized with an external event (such as another UM82C84 clock). It is necessary to synchronize the CSYNC input to the EFI clock external to the UM82C84A. This is accomplished with two flip-flops. The counter output is a 33% duty cycle clock at one-third the input frequency.

The F/C input is a strapping pin that selects either the crystal oscillator or the EFI input as the clock for the –3 counter. If the EFI input is selected as the clock source, the oscillator section can be used independently for another clock source*. Output is taken from OSC.

Clock Outputs

The CLK output is a 33% duty cycle clock driver designed to drive the 80C86, 80C88 processors directly. PCLK is a peripheral clock signal whose output frequency is 1/2 that of CLK. PCLK has a 50% duty cycle.

Reset Logic

The reset logic provides a Schmitt trigger input ($\overline{RES}$) and a synchronizing flip-flop to generate the reset timing. The reset signal si synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the UM82C84A. Wave-forms for clocks and reset signals are illustrated in Figure 1.

Ready Synchronization

Two READY inputs (RDY1, RDY2) are provided to accommodate two system busses. Each input has a qualifier ($\overline{AEN1}$ and $\overline{AEN2}$, respectively). The $\overline{AEN}$ signals validate their respective RDY signals. If a Multi-Master system is not being used the $\overline{AEN}$ pin should be tied LOW.

Synchronization is required for all asynchronous active-going edges of either RDY input to guarantee that the RDY setup and hold times are met. Inactive-going edges of RDY in normally ready systems do not require synchronization but must satisfy RDY setup and hold as a matter of proper system design.

The $\overline{ASYNC}$ input defines two modes of READY synchronization operation.

When $\overline{ASYNC}$ is LOW, two stages of synchronization are provided for active READY input signals. Positive-going asynchronous READY inputs will first be synchronized to flip-flop one at the rising edge of CLK (requiring a setup time tR1VCH) and then synchronized to flip-flop two at the next falling edge of CLK, after which time the READY output will go active (HIGH). Negative-going asynchronous READY inputs will be synchronized directly to flip-flop two at the falling edge of CLK, after which time the READY output will go inactive. This mode of operation is intended for use by asynchronous (normally not ready) devices in the system which cannot be guaranteed by design to meet the required RDY setup timing, tR1VCL, on each bus cycle.

When $\overline{ASYNC}$ is high or left open, the first READY flip-flop is bypassed in the READY synchronization logic. READY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices that can be guaranteed to meet the required RDY setup time.

$\overline{ASYNC}$ can be changed on every bus cycle to select the appropriate mode of synchronization for each device in the system.

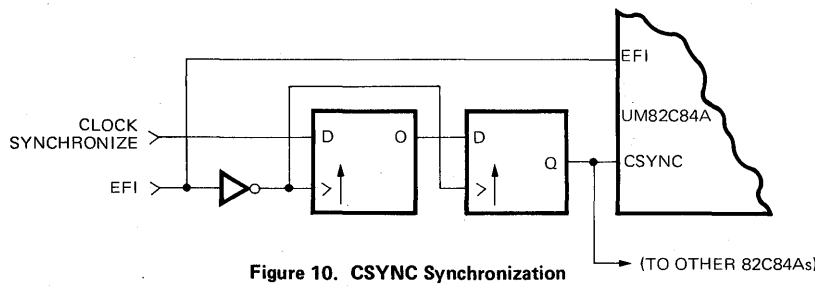


Figure 10. CSYNC Synchronization

*Note: If EFI input is used, then crystal input X1 must be tied to V_{CC} or GND and X2 should be left open. If the crystal inputs are used, then EFI should be tied to V_{CC} or GND.

UM82C88

PRELIMINARY

Bus Controller

Features

- Pin compatible with bipolar 8288
- Provides advanced commands for multimaster busses
- 3-state command outputs
- Bipolar drive capability
- Fully TTL compatible
- High performance HCMOS process
- Single 5V power supply
- Low power operation

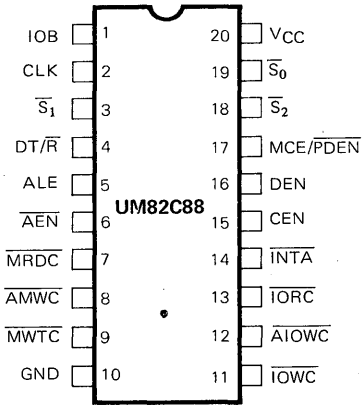
  I_{CCSB} – 10μA

  I_{CCOP} – 1mA/MHz

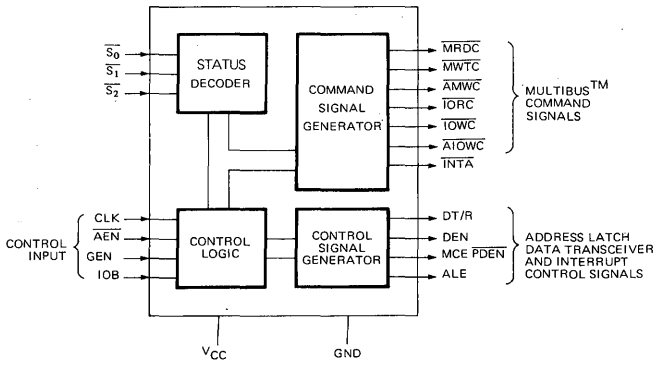
General Description

The UM82C88 is a high performance CMOS Bus Controller manufactured using a self-aligned silicon gate CMOS process. The UM82C88 provides the control and command timing signals for 80C86 and 8086/88 systems. The high output drive capability of the UM82C88 eliminates the need for additional bus drivers. High speed and industry standard configuration make the UM82C88 compatible with microprocessors such as the 80C86, 8086, 8088, 8089, 80186, and 80188.

Pin Configuration



Block Diagram



*TM Multibus is an INTEL Corp trademark

Peripheral IC

Absolute Maximum Ratings*

Supply Voltage . . . . . +8.0 Volts
Operating Voltage Range . . . . . +4V to +7V
Input Voltage Applied . . . . . GND −2.0V to +6.5V
Output Voltage Applied . . . . . GND −0.5V to V_{CC} +0.5V
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range . . . . . 0°C to +70°C
Maximum Power Disipation . . . . . 1 Watt

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Electrical Characteristics

(V_{CC} = 5.0V ±10%; T_A = 0°C to +70°C)

Symbol	Parameter	Min.	Max.	Units	Conditions
V_{IH}	Logic One Input Voltage	2.0		V V	
V_{IL}	Logic Zero Input Voltage		0.8	V	
V_{IHC}	LCK Logical One Input Voltage	0.7 V_{CC}		V	
V_{ILC}	CLK Logical Zero Input Voltage		0.2 VCC	V	
V_{OH}	Output High Voltage Command Outputs	3.0 VCC−0.4		V V	I_{OH} = −8.0mA I_{OH} = −2.5mA
	Output High Voltage Control Outputs	3.0 VCC−0.4		V V	I_{OH} = −4.0mA I_{OH} = −2.5mA
V_{OL}	Output Low Voltage Command Outputs		0.5	V	I_{OL} = +20.0mA
	Output Low Voltage Control Outputs		0.4	V	I_{OL} = +8.0mA
I_{IL}	Input Leakage Current	−1.0	1.0	μA	$0V \leqslant V_{IN} \leqslant V_{CC}$ except $\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$
I_{BHH}	Input Leakage Current-Status Bus	−50	−300	μA	V_{IN} = 2.0V $\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$ (see Note 1)
I_O	Output Leakage Current	−10.0	10.0	μA	$0V \leqslant V_O \leqslant V_{CC}$
I_{CCSB}	Standby Power Supply		10	μA	V_{CC} = 5.5V V_{IN} = V_{CC} or GND Outputs Open
I_{CCOP}	Operating Power Supply Current		1	mA/MHz	V_{CC} = 5.5V Outputs Open

Capacitance

(T_A = 25°C; V_{CC} = GND = OV; V_{IN} = +5V or GND)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_{IN}*	Input Capacitance		5	pf	FREQ = 1MHz Unmeasured pins returned to GND
C_{OUT}*	Output Capacitance		16	pf	

*Guaranteed and sampled, but not 100% tested

A.C. Characteristics

(V_{CC} = +5V ±10%, GND = 0V; T_A = 0°C to 70°C)

TIMING REQUIREMENTS

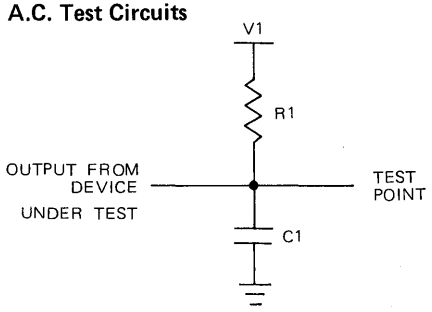
Symbol	Parameter	Min.	Max.	Unit	Conditions
T_{CLCL}	CLK Cycle Period	125		ns	
T_{CLCH}	CLK Low Time	66		ns	
T_{CHCL}	CLK High Time	40		ns	
T_{SVCH}	Status Active Setup Time	35		ns	
T_{CHSV}	Status Active Hold Time	10		ns	
T_{SHCL}	Status Inactive Setup Time	35		ns	
T_{CLSH}	Status Inactive Hold Time	10		ns	

TIMING RESPONSES

Symbol	Parameter	Min.	Max.	Unit	Conditions
T_{CVNV}	Control Active Delay	5	45	ns	1
T_{CVNX}	Control Inactive Delay	10	45	ns	1
T_{CLLH}	ALE Active Delay (from CLK)		20	ns	1
T_{CLMCH}	MCE Active Delay (from CLK)		25	ns	1
T_{SVLH}	ALE Active Delay (from Status)		20	ns	1
T_{SVMCH}	MCE Active Delay (from Status)		30	ns	1
T_{CHLL}	ALE Inactive Delay	4	22	ns	1
T_{CLML}	Command Active Delay	5	35	ns	2
T_{CLMH}	Command Inactive Delay	5	35	ns	2
T_{CHDTL}	Direction Control Active Delay		50	ns	1
T_{CHDTH}	Direction Control Inactive Delay		30	ns	1
T_{AELCH}	Command Enable Time[1]		40	ns	3
T_{AEHCZ}	Command Disable Time[2]		40	ns	4
T_{AELCV}	Enable Delay Time	110	250	ns	2
T_{AEVNV}	$\overline{AEN}$ to DEN		25	ns	1
T_{CEVNV}	CEN to DEN, $\overline{PDEN}$		25	ns	1
T_{CELRH}	CEN to Command		TCLML +10	ns	2
T_{LHLL}	ALE High Time	TCLCH −10		ns	1

Note: 1. T_{AELCH} measurement is between 1.5V and 2.5V.
2. T_{AEHCZ} measured at 0.5V change in VO.

A.C. Test Circuits



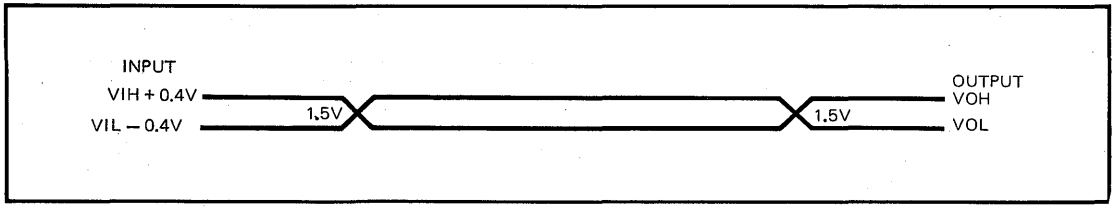
*Includes stray and jig capacitance

Test Conditions	IOH	IOL	V_1	R_1	C_1
1	−4.0mA	+ 8.0mA	2.13V	220Ω	80pf
2	−8.0mA	+20.0mA	2.29V	91Ω	300pf
3	−8.0mA	–	1.50V	187Ω	300pf
4	−8.0mA	–	1.50V	187Ω	50pf

Test Condition Definition Table

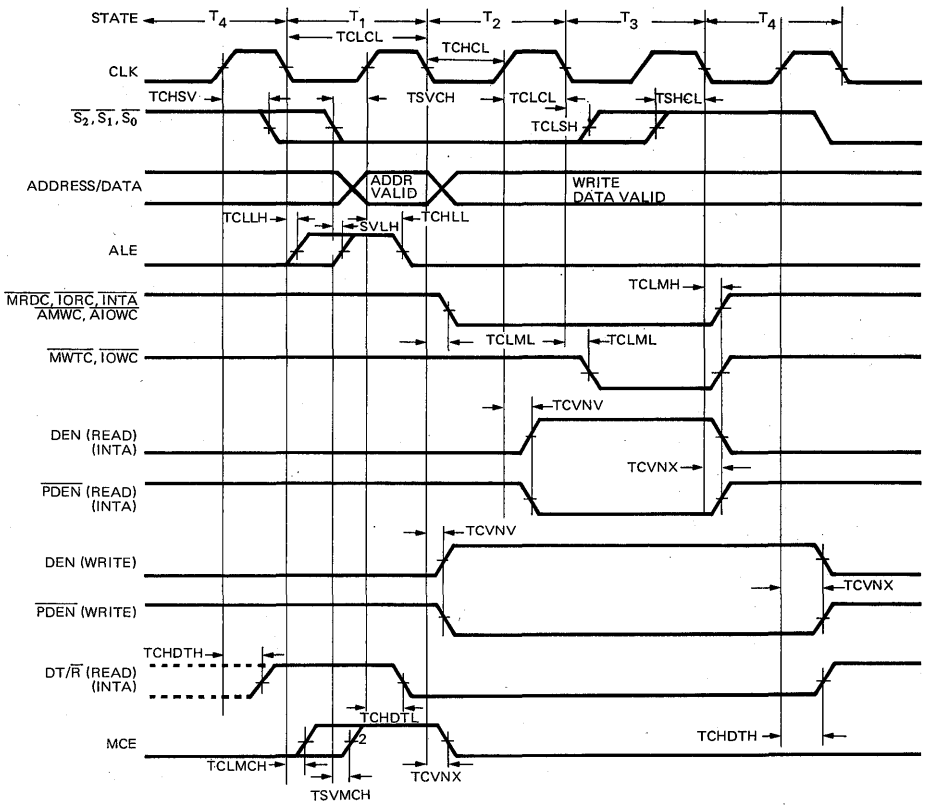
Peripheral IC

A.C. Testing Input, Output Waveform



A.C. Testing: All input signals (other than CLK) must switch between VIL –0.4V and VIH +0.4V. CLK must switch between 0.4V and 3.9V. T_R and T_F must be less than or equal to 15ns.

Waveforms

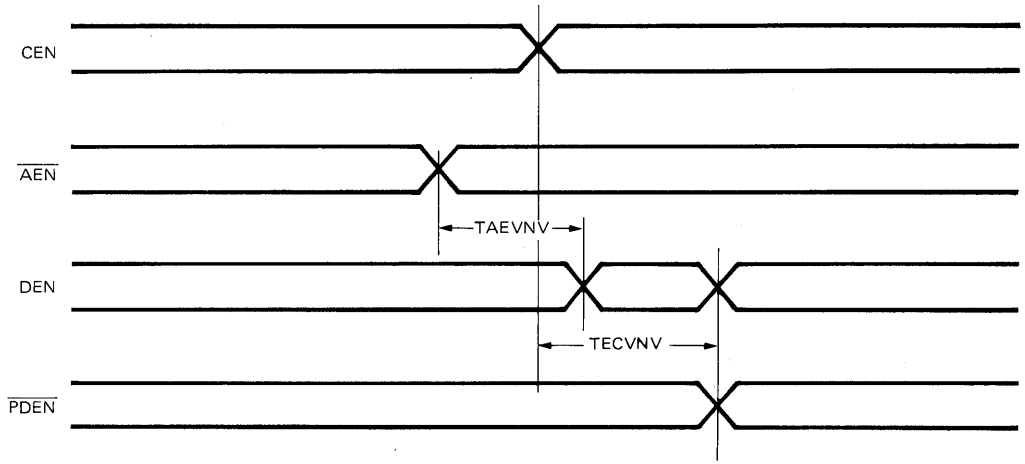


Notes:

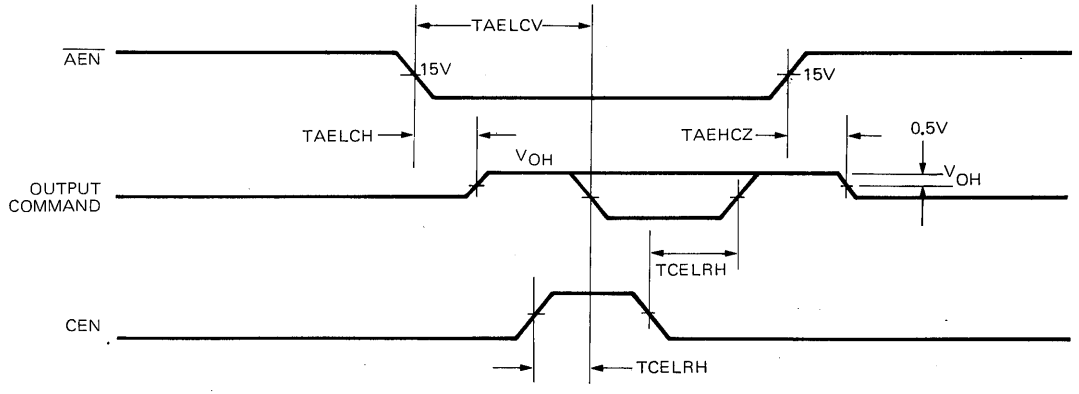
1 Address/data bus is shown only for reference purposes
2 Leading edge of ale and mce is determined by the falling edge of CLK or status going active whichever occurs last
3 All timing me asurements are made at 15V unless specified otherwise

Waveforms (Continued)

DEN, $\overline{PDEN}$ QUALIFICATION TIMING



ADDRESS ENABLE ($\overline{AEN}$) TIMING (3-STATE ENABLE/DISABLE)



Note:
CEN must be low or valid prior to T_2 to prevent the command from being generated.

Pin Description

Symbol	Pin Number	Type	Functions
V_{CC}	20	O	+5V power supply
GND	10		Ground
$\overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2$	19, 3, 18	I	Status input pins: These pins are the input pins from the 80C86, 8086/88/8089 processors. The UM82C88 decodes these inputs to generate command and control signals at the appropriate time. When Status pins are not in use (passive), command outputs are held HIGH (See Table 1.)
CLK	2	I	Clock: This is a CMOS compatible input which receives a clock signal from the UM82C84A clock generator and serves to establish when command/control signals are generated.
ALE	5	O	Address Latch Enable: This signal serves to strobe an address into the address latches. This signal is active HIGH and latching occurs on the falling (HIGH to LOW) transition. ALE is intended for use with transparent D type latches, such as the 82C82.
DEN	16	O	Data Enable: This signal serves to enable data transceivers onto either the local or system data bus. This signal is active HIGH.
DT/$\overline{R}$	4	O	Data Transmit/Receive: This signal establishes the direction of data flow through the transceivers. A HIGH on this line indicates Transmit (write to I/O or memory) and a LOW indicates Transmit (write to I/O or memory) and a LOW indicates Receive (Read).
$\overline{AEN}$	6	I	Address Enable: $\overline{AEN}$ enables command outputs of the UM82C88 Bus Controller a minimum of 110ns (250ns maximum) after it becomes active (LOW). $\overline{AEN}$ going inactive immediately 3-states the command output drivers. $\overline{AEN}$ does not affect the I/O command lines if the UM82C88 is in the I/O Bus mode (IOB tied HIGH).
CEN	15	I	Command Enable: When this signal LOW all UM82C88 command outputs and the DEN and PDEN control outputs are forced to their inactive state. When this signal is HIGH, these same outputs are enabled.
IOB	1	I	Input/Output Bus Mode: When the IOB is strapped HIGH the UM82C88 functions in the I/O Bus mode. When it is strapped LOW, the UM82C88 functions in the System Bus mode (See I/O Bus and System Bus sections).
$\overline{AIOWC}$	12	O	Advanced I/O Write Command: The $\overline{AIOWC}$ issues an I/O Write Command earlier in the machine cycle to give I/O devices an early indication of a write instruction. Its timing is the same as a read command signal. $\overline{AIOWC}$ is active LOW.
$\overline{IOWC}$	11	O	I/O Write Command: This command line instructs an I/O device to read the data on the data bus. The signal is active LOW.
$\overline{IORC}$	13	O	I/O Read Command: This command line instructs an I/O device to drive its data onto the data bus. This signal is active LOW.
$\overline{AMWC}$	8	O	Advanced Memory Write Command: The $\overline{AMWC}$ issues a memory write command earlier in the machine cycle to give memory devices an early indication of a write instruction. Its timing is the same as a read command signal. $\overline{AMWC}$ is active LOW.
$\overline{MWTC}$	9	O	Memory Write Command: This command line instructs the memory to record the data present on the data bus. This signal is active LOW.
$\overline{MRDC}$	7	O	Memory Read Command: This command line instructs the memory to drive its data onto the data bus. $\overline{MRDC}$ is active LOW.
$\overline{INTA}$	14	O	Interrupt Acknowledge: This command line tells an interrupting device that its interrupt has been acknowledged and that it should drive vectoring information onto the data bus. This signal is active LOW.
MCE/$\overline{PDEN}$	17	O	This is a dual function pin. MCE (IOB is tied LOW): Master Cascade Enable occurs during an interrupt sequence and serves to read a Cascade Address from a master UM82C59A Priority Interrupt Controller onto the data bus. The MCE signal is active HIGH. $\overline{PDEN}$ (IOB is tied HIGH): Peripheral Data Enable enables the data bus transceiver for the I/O bus that DEN performs for the system bus. $\overline{PDEN}$ is active LOW.

Functional Description

Command and Control Logic

The command logic decodes the three 80C86, 8086, 8088 or 8089 status lines ($\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$) to determine what command is to be issued (see Table 1).

Table 1. Command Decode Definition

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Processor State	UM82C88 Command
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Code Access	$\overline{MRDC}$
1	0	1	Read Memory	$\overline{MRDC}$
1	1	0	Write Memory	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	None

I/O BUS Mode

The UM82C88 is in the I/O Bus mode if the IOB pin is strapped HIGH. In the I/O Bus mode, all I/O command lines ($\overline{IORC}$, $\overline{IWC}$, $\overline{AIOWC}$, $\overline{INTA}$) are always enabled (i.e., not dependent on $\overline{AEN}$). When an I/O command is initiated by the processor, the UM82C88 immediately activates the command lines using $\overline{PDEN}$ and DT/$\overline{R}$ to control the I/O bus transceiver. The I/O command lines should not be used to control the system bus in this configuration because no arbitration is present. This mode allows one UM82C88 Bus Controller to handle two external busses. No waiting is involved when the CPU wants to gain access to the I/O bus. Normal memory access requires a "Bus Ready" signal ($\overline{AEN}$ LOW) before it will proceed. It is advantageous to use the IOB mode if I/O or peripherals dedicated to one processor exist in a multi-processor system.

System BUS Mode

The UM82C88 is in the System Bus Mode if the IOB pin is strapped LOW. In this mode, no command is issued until a specified time period after the AEN line is activated (LOW). This mode assumes bus arbitration logic will inform the bus controller (on the AEN line) when the bus is free for use. Both memory and I/O commands wait for bus arbitration. This mode is used when only one bus exists. Here, both I/O and memory are shared by more than one processor.

Command Outputs

The advanced writer commands are made available to initiate write procedures early in the machine cycle. This signal can be used to prevent the processor from entering an unnecessary wait state.

The command outputs are:

- $\overline{MRDC}$ – Memory Read Command
- $\overline{MWTC}$ – Memory Write Command
- $\overline{IORC}$ – I/O Read Command
- $\overline{IOWC}$ – I/O Write Command
- $\overline{AMWC}$ – Advanced Memory Write Command
- $\overline{AIOWC}$ – Advanced I/O Write Command
- $\overline{INTA}$ – Interrupt Acknowledge

$\overline{INTA}$ (Interrupt Acknowledge) acts as an I/O read during an interrupt cycle. Its purpose is to inform an interrupting device that its interrupt is being acknowledged and that it should place vectoring information onto the data bus.

Control Outputs

The control outputs of the UM82C88 are Data Enable (DEN), Data Transmit/Receive (DT/$\overline{R}$) and Master Cascade Enable/Peripheral Data Enable (MCE/$\overline{PDEN}$). The Den signal determines when the external bus should be enabled onto the local bus and the DT/R determines the direction of data transfer. These two signals usually go to the chip select and direction pins of a transceiver.

The MCE/$\overline{PDEN}$ pin changes function with the two modes of the UM82C88. When the UM82C88 is in the IOB mode (IOB HIGH), the $\overline{PDEN}$ signal serves as a dedicated data enable signal for the I/O or Peripheral System bus.

Interrupt Acknowledge and MCE

The MCE signal is used during an interrupt acknowledge cycle if the UM82C88 is in the System Bus mode (IOB LOW). During any interrupt sequence, there are two interrupt acknowledge cycles that occur back to back. During the first interrupt cycle no data or address transfers take place. Logic should be provided to mask off MCE during this cycle. Just before the second cycle begins the MCE signal gates a master Priority Interrupt Controller's (PIC) cascade address onto the processor's local bus where ALE (Address Latch Enable) strobes it into the address latches. On the leading edge of the second interrupt cycle, the addressed slave PIC gates an interrupt vector onto the system data bus where it is ready by the processor.

If the system contains only one PIC, the MCE signal is not used. In this case, the second Interrupt Acknowledge signal gates the interrupt vector onto the processor bus.

Address Latch Enable and Halt

Address Latch Enable (ALE) occurs during each machine cycle and serves to strobe the current address into the 82C82 address latches. ALE also serves to strobe the status ($\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$) into a latch for halt state decoding.

Command Enable

The Command Enable (CEN) input acts as a command qualifier for the UM82C88. If the CEN pin is high, the UM82C88 functions normally. If the CEN pin is pulled LOW, all command lines are held in their inactive state (not 3-state). This feature can be used to implement memory partitioning and to eliminate address conflicts between system bus devices and resident bus devices.

UM8237A/8237A-4/8237A-5

Programmable DMA Controller (DMAC)

ADVANCED PRODUCT DESCRIPTION

Features

- Enable/Disable control of individual DMA requests
- Four independent DMA channels
- Independent autoinitialization of all channels
- Memory-to-memory transfers
- Memory block initialization
- Single 5V power supply
- High performance: transfers up to 1.6M bytes/second with 5MHz 8237A-5
- Directly expandable to any number of channels
- End of process input for terminating transfers
- Software DMA requests
- Independent Polarity control for DREQ and DACK signals
- Available in EXPRESS
  – Standard Temperature Range

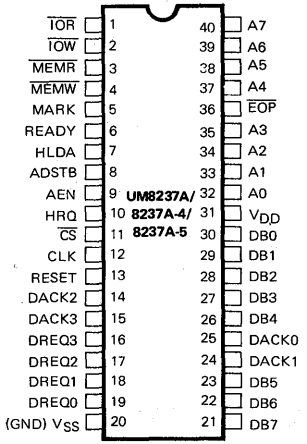
General Description

The UM8237A Direct Memory Access Controller (DMAC) is a peripheral interface circuit for microprocessor systems. It is designed to improve system performance by allowing external devices to directly transfer information from the system memory. Memory-to-memory transfer capability is also provided. The UM8237A offers a wide variety of programmable control features to enhance data throughput and system optimization and to allow dynamic reconfiguration under program control.

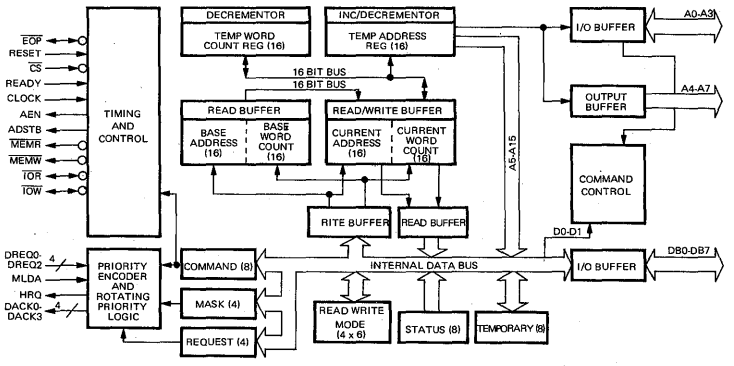
UM8237A is fabricated in Si-Gate NMCS process with each channel has a full 64K address and word count capability.

The 8237A-4 and 8237A-5 are 4 MHz and 5 MHz selected versions of the standard 3 MHz 8237A respectively.

Pin Configuration



Block Diagram



UM8253 / UM8253-5

Programmable Interval Timer

Features

- MCS-85™ compatible UM8253-5
- 3 independent 16-bit counters
- DC to 2.6 MHz
- Programmable counter modes
- Count binary or BCD
- Single +5V supply

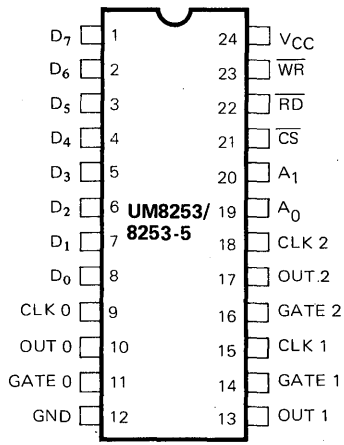
General Description

The UM8253 is a programmable counter timer device designed for use as an microcomputer peripheral. It uses NMOS technology with a single +5V supply and is packaged in a 24-pin plastic DIP.

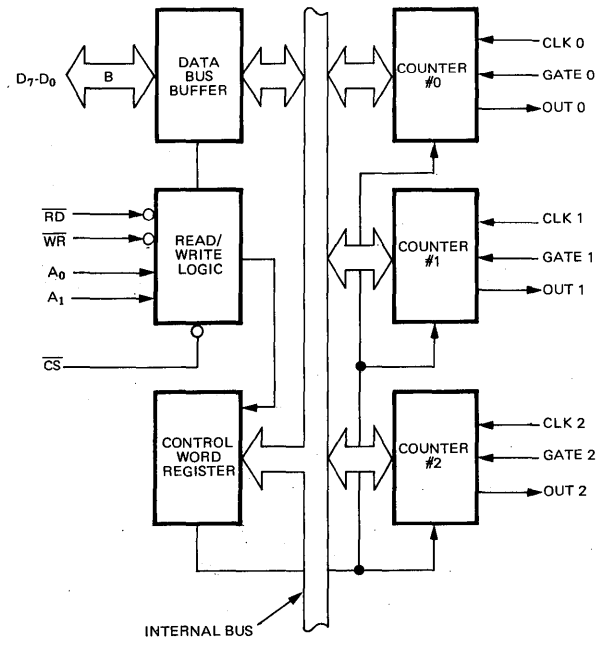
It is organized as 3 independent 16-bit counters, each with a count rate of up to 2.6 MHz. All modes of operation are software programmable.

*MCS-85™ is the trademark of Intel microsystem.

Pin Configuration



Block Diagram



Peripheral IC

Absolute Maximum Ratings*

Ambient Temperature Under Bias T_A . . . . . 0°C to 70°C

Storage Temperature T_{STG} . . . . . –65°C to +150°C

Voltage on Any Pin with Respect to Ground . . . . . –0.5V to +7V

Power Dissipation . . . . . 1 Watt

*Comments

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Min	Max.	Units	Conditions
V_{IL}	Input Low Voltage	–0.5	0.8	V	
V_{IH}	Input High Voltage	2.2	V_{CC}+0.5V	V	
V_{OL}	Output Low Voltage		0.45	V	Note 1
V_{OH}	Output High Voltage	2.4		V	Note 2
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to 0.45V
I_{CC}	V_{CC} Supply Current		140	mA	

Capacitance

(T_A = 25°C, V_{CC} = GND = 0V)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1 MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to V_{SS}

A.C. Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5.0V ± 10%, GND = 0V)

Bus Parameters (Note 3)

READ CYCLE

Symbol	Parameter	UM8253		UM8253-5		Units
		Min.	Max.	Min.	Max.	
t_{AR}	Address Stable Before $\overline{READ}$	50		30		ns
t_{RA}	Address Hold Time for $\overline{READ}$	5		5		ns
t_{RR}	$\overline{READ}$ Pulse Width	400		300		ns
t_{RD}	Data Delay From $\overline{READ}$ (4)		300		200	ns
t_{DF}	$\overline{READ}$ to Data Floating	25	125	25	100	ns
t_{RV}	Recovery Time Between READ and Any Other Control Singnal	1		1		μs

A.C. Characteristics (Continued)

WRITE CYCLE

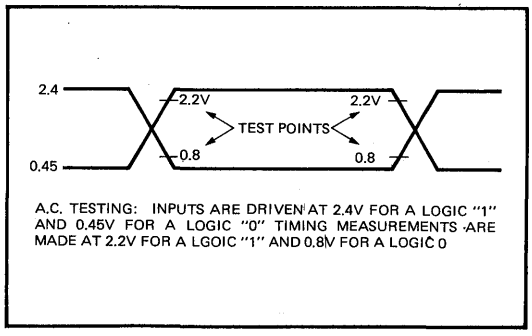
Symbol	Parameter	UM8253		UM8253-5		Units
		Min.	Max.	Min.	Max.	
t_{AW}	Address Stable Before $\overline{WRITE}$	50		30		ns
t_{WA}	Address Hold Time for $\overline{WRITE}$	30		30		ns
t_{WW}	$\overline{WRITE}$ Pulse Width	400		300		ns
t_{DW}	Data Set Up Time for $\overline{WRITE}$	300		250		ns
t_{WD}	Data Hold Time for $\overline{WRITE}$	40		30		ns
t_{RV}	Recovery time Between $\overline{WRITE}$ and Any Other Control Signal	1		1		μs

Clock and Gate Timing

Symbol	Parameter	UM8253		UM8253-5		Unit
		Min.	Max.	Min.	Max.	
t_{CLK}	Clock Period	380	dc	380	dc	ns
t_{PWH}	High Pulse Width	230		230		ns
t_{PWL}	Low Pulse Width	150		150		ns
t_{GW}	Gate Width High	150		150		ns
t_{GL}	Gate Width Low	100		100		ns
t_{GS}	Gate Set Up Time to CLK↑	100		100		ns
t_{GH}	Gate Hold Time After CLK↑	50		50		ns
t_{OD}	Output Delay From CLK↓[4]		400		400	ns
t_{ODG}	Output Delay From Gate↓[4]		300		300	ns

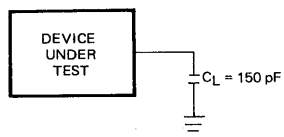
Notes:
1. I_{OL} = 2.2 mA.
2. I_{OH} = −400 μA.
3. AC timings measured at V_{OH} 2.2, V_{OL} = 0.8.
4. C_L = 150pF.

A.C. Testing Input, Output Waveform



A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0" TIMING MEASUREMENTS ARE MADE AT 2.2V FOR A LGOIC "1" AND 0.8V FOR A LOGIC 0

A.C. Testing Load Circuit

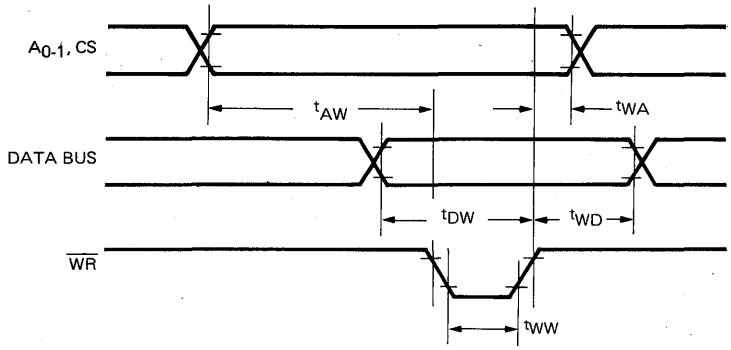


C_L INCLUDES JIG CAPACITANCE

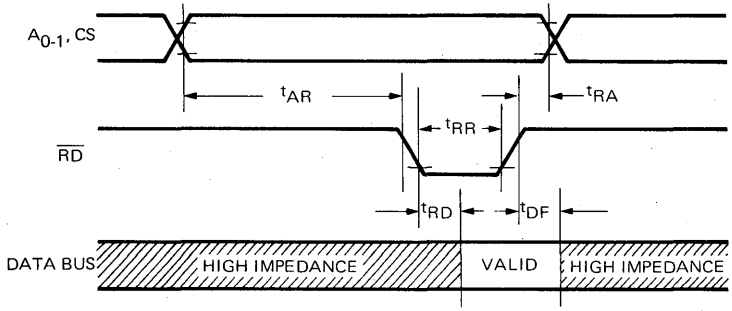
Peripheral IC

Waveforms

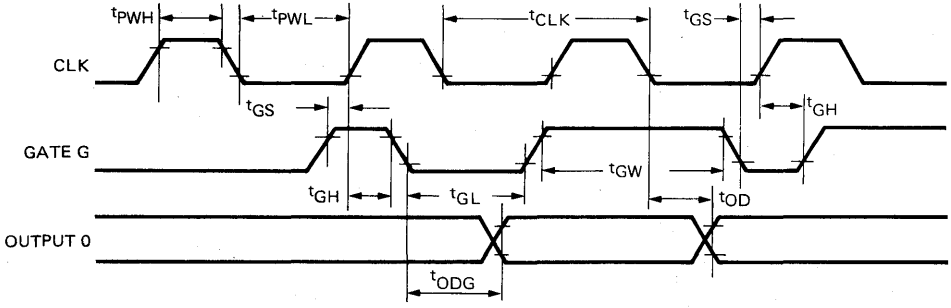
WRITE TIMING



READ TIMING



CLOCK AND GATE TIMING



Functional Description

General

The UM8253 is a programmable interval timer/counter specifically designed for use with microcomputer systems. Its function is that of a general purpose, multiming element that can be treated as an array of I/O ports in the system software.

The UM8253 solves one of the most common problems in any microcomputer system the generation of accurate time delays under software control. Instead of setting up timing loops in systems software, the programmer configures the UM8253 to match his requirements, initializes one of the counters of the UM8253 with the desired quantity, then upon command the UM8253 will count out the delay and interrupt the UPU when it has completed its tasks. It is easy to see that the software overhead is minimal and that multiple delays can easily be maintained by assignment of priority levels.

Other counter/timer functions that are non-delay in nature but also common to most microcomputers can be implemented with the UM8253.

- Programmable Rate Generator
- Event Counter
- Binary Rate Multiplier
- Real Time Clock
- Digital One-Shot
- Complex Motor Controller

Data Bus Buffer

This 3-state, bi-directional, 8-bit buffer is used to interface the UM8253 to the system data bus. Data is transmitted or received by the buffer upon execution of input or OUT put CPU instructions. The Data Bus Buffer has three basic functions.

1. Programming the MODES of the UM8253.
2. Loading the count registers.
3. Reading the count values.

Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and in turn generates control signals for overall device operation. It is enable or disabled by CS so that no operation can occur to change the function unless the device has been selected by the system logic.

$\overline{RD}$ (Read)

A "low" on this input informs the UM8253 that the CPU is inputting data in the form of a counters value.

$\overline{WR}$ (Write)

A "low" on this input informs the UM8253 that the CPU is outputting data in the form of mode information or loading counters.

A_0 , A_1

These inputs are normally connected to the address bus. Their function is to select one of the three counters to be operated on and to address the control word register for mode selection.

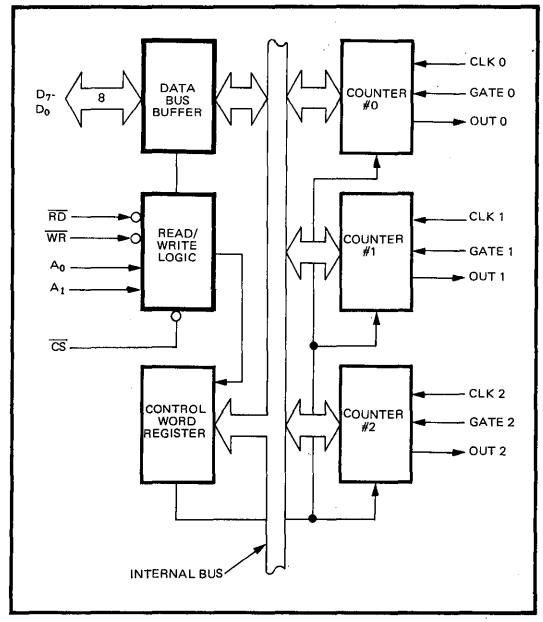


Figure 1. Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions

CS	RD	WR	A_1	A_0	
0	1	0	0	0	Load Counter No. 0
0	1	0	0	1	Load Counter No. 1
0	1	0	1	0	Load Counter No. 2
0	1	0	1	1	Write Mode Word
0	0	1	0	0	Read Counter No. 0
0	0	1	0	1	Read Counter No. 1
0	0	1	1	0	Read Counter No. 2
0	0	1	1	1	No-Operation 3-State
1	X	X	X	X	Disable 3-State
0	1	1	X	X	No-Operation 3-State

$\overline{CS}$ (Chip Select)

A "low" on this input enables the UM8253. No reading or writing will occur unless the device is selected. The $\overline{CS}$ input has no effect upon the actual operation of the counters.

Control Word Register

The Control Word Register is selected when A_0, A_1 are 11. It then accepts information from the data bus buffer and stores it in a register. The information stored in this register controls the operational MODE of each counter, selection of binary or BCD counting and the loading of each count register.

The Control Word Register can only be written into; no read operation of its contents is available.

Counter #0, Counter #1, Counter #2

These three functional blocks are identical in operation so only a single Counter will be described. Each Counter consists of a single, 16-bit, pre-settable, DOWN counter. The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of MODES stored in the Control Word Register.

The counters are fully independent and each can have separate Mode configuration and counting operation, binary or BCD. Also, there are special features in the control word that handle the loading of the count value so that software overhead can be minimized for these functions.

The reading of the contents of each counter is available to the programmer with simple READ operations for event counting applications and special commands and logic are included in the UM8253 so that the contents of each counter can be read "on the fly" without having to inhibit the clock input.

UM8253 System Interface

The UM8253 is a component of the UMC Microcomputer Systems and interfaces in the same manner as all other peripherals of the family. It is treated by the systems software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A_0, A_1 connect to the A_0, A_1 address bus signals of the CPU. The CS can be derived directly from the address bus using a linear select method. Or it can be connected to the output of a decoder, such as an 8205 for larger systems.

Operational Description

General

The complete functional definit on of the UM8253 is programmed by the systems software. A set of control words must be sent out by the CPU to initialize each counter of the UM8253 with the desired MODE and

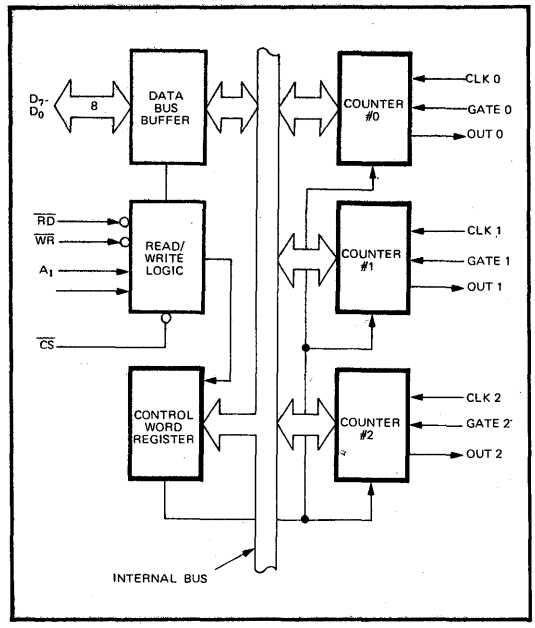


Figure 2. Block Diagram Showing Control Word Register and Counter Functions

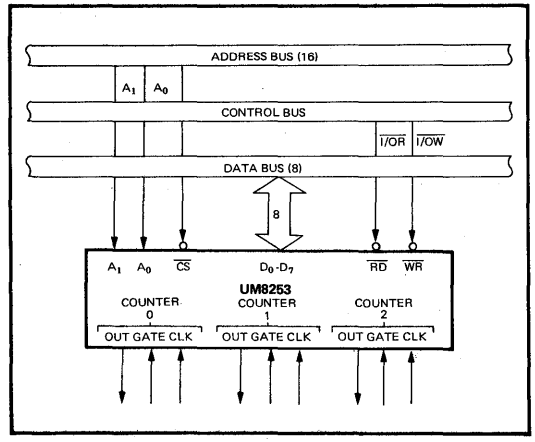


Figure 3. UM8253 System Interface

quantity information, prior to initialization, the MODE, count, and output of all counters is undefined. These control words program the MODE, Loading sequence and selection of binary or BCD counting.

Once programmed, the UM8253 is ready to perform whatever timing tasks it is assigned to accomplish.

The actual counting operation of each counter is completely independent and additional logic is provided on-chip so that the usual problems associated with efficient monitoring and management of external, asynchronous events or rates to the microcomputer system have been eliminated.

Programming the UM8253

All of the MODES for each counter are programmed by the systems software by simple I/O operations.

Each counter of the UM8253 is individually programmed by writing a control word into the Control Word Register. (A_1, A_1 = 11)

Control Word Format

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Definition of Control

SC – Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

RL – Read/Load:

RL1	RL0	
0	0	Counter Latching operation (see READ/WRITE procedure Section)
1	0	Read/Load most significant byte only.
0	1	Read/Load least significant byte only.
1	1	Read/Load least significant byte first, then most significant byte.

M – MODE:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD:

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

Counter Loading

The count register is not loaded until the count value is written (one or two bytes, depending on the mode selected by the RL bits), followed by a rising edge and a falling edge of the clock. Any read of the counter prior to that falling clock edge may yield invalid data.

MODE Definition

MODE 0: Interrupt on Terminal Count. The output will be initially low after the mode set operation. After the count is loaded into the selected count register, the output will remain low and the counter will count. When terminal count is reached the output will go high and remain high until the selected count register is reloaded with the mode or a new count is loaded. The counter continues to decrement after terminal count has been reached.

Rewriting a counter register during counting results in the following:

(1) Write 1st byte stops the current counting.
(2) Write 2nd byte starts the new count.

MODE 1: Programmable One-Shot. The output will go low on the count following the rising edge of the gate input.

The output will go high on the terminal count. If a new count value is loaded while the output is low it will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse.

The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the gate input.

MODE 2: Rate Generator. Divide by N counter. The output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value.

The gate input, when low, will force the output high. When the gate input goes high, the counter will start from the initial count. Thus, the gate input can be used to synchronize the counter.

When this mode is set, the output will remain high until after the count register is loaded. The output then can also be synchronized by software.

MODE 3: Square Wave Rate Generator. Similar to MODE 2 except that the output will remain high until one half the count has been completed (for even numbers) and go low for the other half of the count. This is accomplished by decrementing the counter by two on the falling edge of each clock pulse. When the counter reaches terminal count, the state of the output is changed and the counter is reloaded with the full count and the whole process is repeated.

If the count is odd and the output is high, the first clock pulse (after the count is loaded) decrements the count by 1. Subsequent clock pulses decrement the clock by 2. After timeout, the output goes low and the full count is reloaded. The first clock pulse (following the reload) decrements the counter by 3. Subsequent clock pulses decrement the count by 2 until timeout. Then the whole process is repeated. In this way, if the count is odd, the output will be high for (N+1)/2 counts and low for (N–1)/2 counts.

In Modes 2 and 3, if a CLK source other than the system clock is used, GATE should be pulsed immediately following WR of a new count value.

MODE 4: Software Triggered Strobe. After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period, then will go high again.

If the count register is reloaded during counting, the new count will be loaded on the nest CLK pulse. The count will be inhibited while the GATE input is low.

MODE 5: Hardware Triggered Strobe. The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of any trigger.

Signal Status / Modes	Low or Going Low	Rising	High
0	Disables counting	––	Enables counting
1	––	1) Initiates counting 2) Resets output after next clock	––
2	1) Disables counting 2) Sets output immediately high	1) Reloads counter 2) Initiates counting	Enables counting
3	1) Disables counting 2) Sets output immediately high	1) Reloads counter 2) Initiates counting	Enables counting
4	Disables counting	––	Enables counting
5	––	Initiates counting	––

Figure 4. Gate Pin Operations Summary

UM8253 Read/Write Procedure

Write Operations

The systems software must program each counter of the UM8253 with the mode and quantity desired. The programmer must write out to the UM8253 a MODE control word and the programmed number of count register bytes (1 or 2) prior to actually using the selected counter.

The actual order of the programming is quite flexible. Writing out of the MODE control word can be in any sequence of counter selection, e.g., counter #0 does not have to be first or counter #2 last. Each counter's MODE control word register has a separate address so that its loading is completely sequence independent. (SC0, SC1)

The loading of the Count Register with the actual count value, however, must be done in exactly the sequence programmed in the MODE control word (RL0, RL1). This loading of the counter's count register is still sequence independent like the MODE control word loading, but when a selected count register is to be loaded it ***must*** be loaded with the number of bytes programmed in the MODE control word (RL0, RL1). The one or two bytes to be loaded in the count register do not have to follow the associated MODE control word. They can be programmed at any time following the MODE control word loading as long as the correct number of bytes is loaded in order.

All counters are down counters. Thus, the value loaded into the count register will actually be decremented. Loading all zeroes into a count register will result in the maximum count (2^{16} for Binary or 10^4 for BCD). In

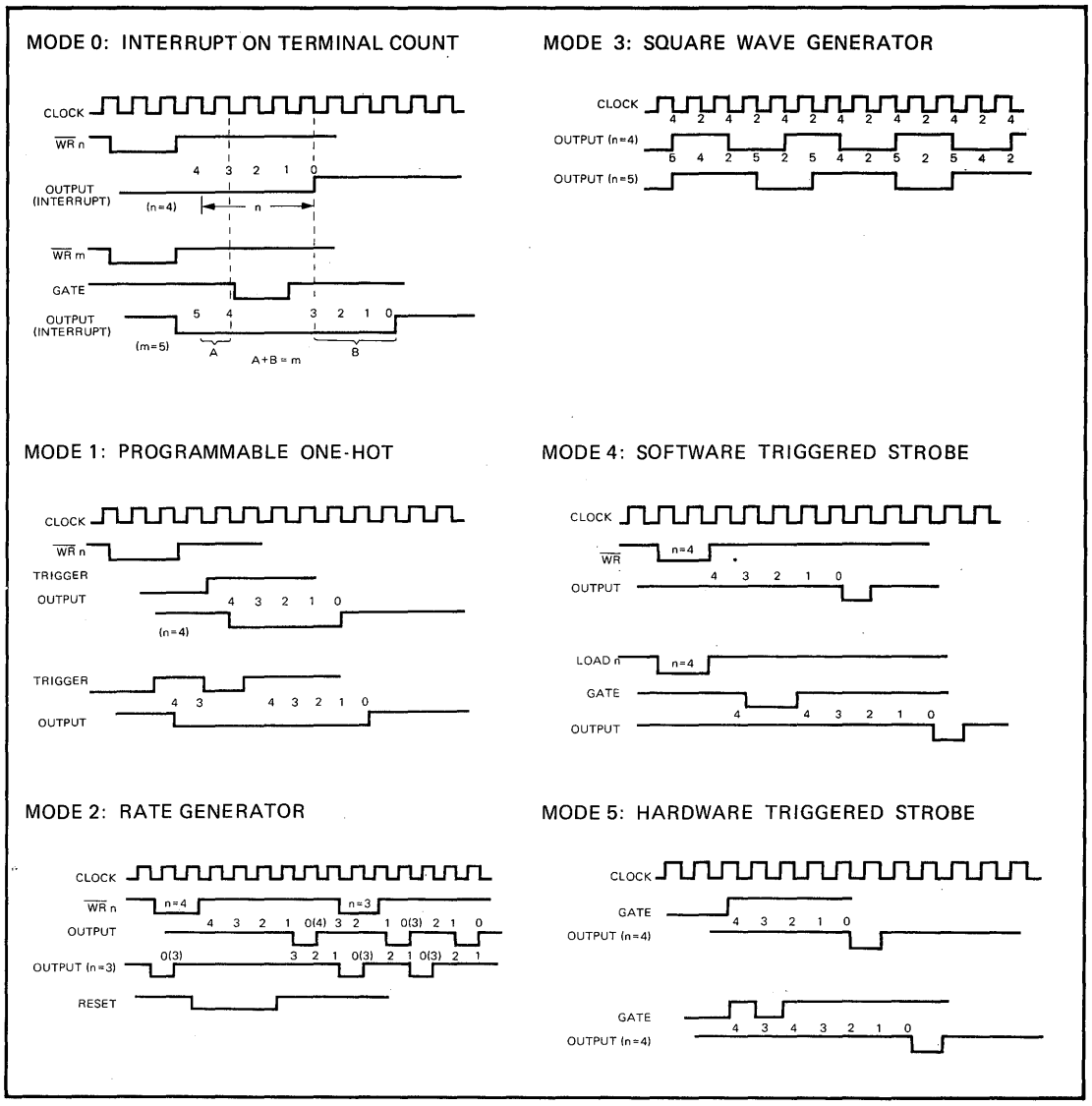


Figure 5. UM8253 Timing Diagrams

MODE 0 the new count will not restart until the load has been completed. It will accept one of two bytes depending on how the MODE control words (RL0, RL1) are programmed. Then proceed with the restart operation.

Read Operations

In most counter applications it becomes necessary to read the value of the count in progress and make a computational decision based on this quantity. Event counters are probably the most common application that uses this function. The UM8253 contains logic that will allow the programmer to easily read the contents of any of the three counters without disturbing the actual count in progress.

There are two methods that the programmer can use to read the value of the counters. The first method involves the use of simple I/O read operations of the selected counter. By controlling the A0, A1 inputs to the UM8253 the programmer can select the counter to be read

(remember that no read operation of the mode register is allowed A0, A1-11). The only requirement with this method is that in order to assure a stable count reading the actual operation of the selected counter ***must be inhibited*** either by controlling the Gate input or by external logic that inhibits the clock input. The contents of the counter selected will be available as follows:

first I/O Read contains the least significant byte (LSB).

second I/O Read contains the most significant byte (MSB).

Due to the internal logic of the UM8253 it is absolutely necessary to complete the entire reading procedure. If two bytes are programmed to be read then two bytes must be read before any loading WR command can be sent to the same counter.

Read Operation Chart

A1	A0	RD	
0	0	0	Read Counter No. 0
0	1	0	Read Counter No. 1
1	0	0	Read Counter No. 2
1	1	0	Illegal

Reading While Counting

In order for the programmer to read the contents of any counter without effecting or disturbing the counting operation the UM8253 has special internal logic that can be accessed using simple WR commands to the MODE register. Basically, when the programmer wishes to read the contents of a selected counter "on the fly" he loads the MODE register with a special code which latches the present count value into a storage register so that its contents contain an accurate, stable quantity. The programmer then issues a normal read command to the selected counter and the contents of the latched register is available.

	MODE Control Word Counter n
LSB	Count Register byte Counter n
MSB	Count Register byte Counter n

Note: Format shown is a simple example of loading the UM8253 and does not imply that it is the only for

Figure 6. Programming Format

MODE Register for Latching Count

A0, A1 = 11

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	0	0	X	X	X	X

SC1, SC0 – specify counter to be latched.

D5, D4 – 00 designates counter latching operation.

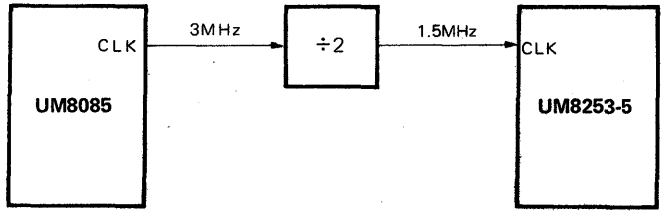
X – don't care.

The same limitation applies to this mode of reading the counter as the previous method. That is, it is mandatory to complete the entire read operation as programmed. This command has no effect on the counter's mode.

			A_1	A_0
No. 1		MODE Control Word Counter 0	1	1
No. 2		MODE Control Word Counter 1	1	1
No. 3		MODE Control Word Counter 2	1	1
No. 4	LSB	Count Register Byte Counter 1	0	1
No. 5	MSB	Count Register Byte Counter 1	0	1
No. 6	LSB	Count Register Byte Counter 2	1	0
No. 7	MSB	Count Register Byte Counter 2	1	0
No. 8	LSB	Count Register Byte Counter 0	0	0
No. 9	MSB	Count Register Byte Counter 0	0	0

Note: The exclusive addresses of each counter's count register make the task of programming the UM8253 a very simple matter, and maximum effective use of the device will result if this feature is fully utilized.

Figure 7. Alternate Programming Formats



If an UM8085 clock output is to drive an UM8253-5 clock input, it must be reduced to 2MHz or less.

Figure 8. MCS-85™ Clock Interface*

Ordering Information

Part Number	CLK
UM8253	2.6MHz
UM8253–5	5MHz

UM8254

Programmable Interval Timer

Features

- Compatible with most microprocessor including 8080A, 8085A, iAPX88 and iAPX86*
- Handles inputs from DC to 8 MHz
- Six programmable counter modes
- Status read-back command
- Three independent 16-bit counters
- Binary or BCD counting
- Single +5V supply

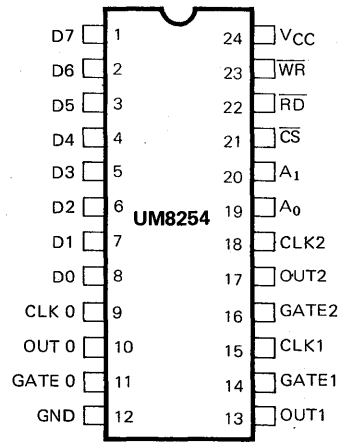
General Description

The UM8254 is a counter/timer device designed to solve the common timing control problems in microcomputer system design. It provides three independent 16-bit counters, each capable of handling clock inputs up to 8 MHz. All modes are software programmable. The UM8254 is a superset of the UM8253.

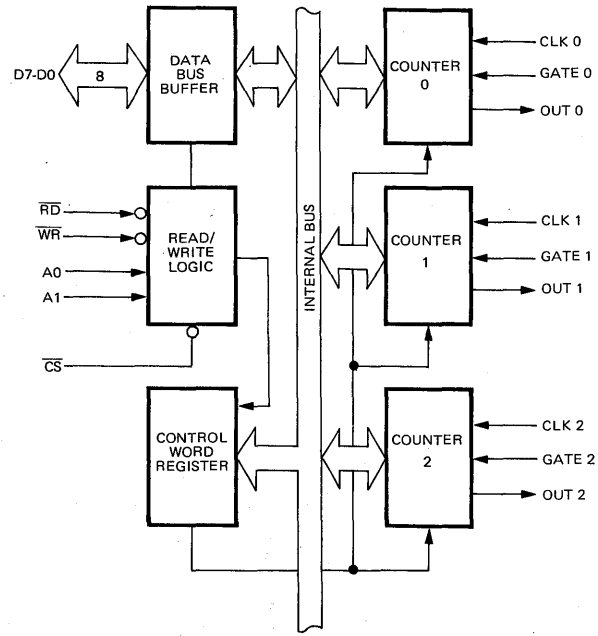
The UM8254 uses HMOS technology and comes in a 24-pin plastic package.

*iAPX88 and iAPX86 are all trademarks of Intel microsystem.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Ambient Temperature Under Bias T_A . . . . . 0°C to 70°C

Storage Temperature T_{STG} . . . . . –65°C to +150°C

Voltage on Any Pin with Respect to Ground . . . . . –0.5V to +7V

Power Dissipation . . . . . 1 Watt

*Comments

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V + 10%)

Symbol	Parameter	Min.	Max.	Units	Conditions
V_{IL}	Input Low Voltage	–0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5V	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = –400 μA
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to 0.45V
I_{CC}	V_{CC} Supply Current		140	mA	

Capacitance

(T_A = 25°C, V_{CC} = GND = 0V)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_{IN}	Input Capacitance		10	pF	f_C = 1 MHz
$C_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins returned to V_{SS}

A.C. Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, GND = 0V)

Bus Parameters (Note 1)

READ CYCLE

Symbol	Parameter	UM8254		Unit
		Min.	Max.	
t_{AR}	Address Stable Before $\overline{RD}\downarrow$	45		ns
t_{SR}	$\overline{CS}$ Stable Before $\overline{RD}\downarrow$	0		ns
t_{RA}	Address Hold Time After $\overline{RD}\uparrow$	0		ns
t_{RR}	RD Pulse Width	150		ns
t_{RD}	Data Delay from $\overline{RD}\downarrow$		120	ns
t_{AD}	Data Delay from Address		220	ns
t_{DF}	$\overline{RD}\uparrow$ to Data Floating	5	90	ns
t_{RV}	Command Recovery Time	200		ns

Note: AC timings measured at V_{OH} = 2.0V, V_{OL} = 0.8V

A.C. Characteristics (Continued)

WRITE CYCLE

Symbol	Parameter	UM8254		Units
		Min.	Max.	
t_{AW}	Address Stable Before $\overline{WR}\downarrow$	0		ns
t_{SW}	$\overline{CS}$ Stable Before $\overline{WR}\downarrow$	0		ns
t_{WA}	Address Hold Time $\overline{WR}\uparrow$	0		ns
t_{WW}	$\overline{WR}$ Pulse Width	150		ns
t_{DW}	Data Setup Time Before $\overline{WR}\uparrow$	120		ns
t_{WD}	Data Hold Time After $\overline{WR}\uparrow$	0		ns
t_{RV}	Command Recovery Time	200		ns

Clock and Gate

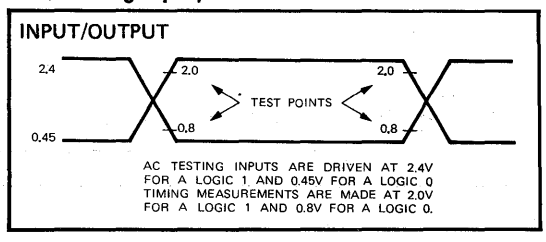
(T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, GND = 0V)

Symbol	Parameter	UM8254		Units
		Min.	Max.	
t_{CLK}	Clock Period	125	DC	ns
t_{PWH}	High Pulse Width	60(3)		ns
t_{PWL}	Low Pulse Width	60(3)		ns
t_R	Clock Rise Time		25	ns
t_F	Clock Fall Time		25	ns
t_{GW}	Gate Width High	50		ns
t_{GL}	Gate Width Low	50		ns
t_{GS}	Gate Setup Time to CLK↑	50		ns
t_{GH}	Gate Hold Time After CLK↑	50(2)		ns
t_{OD}	Output Delay from CLK↓		150	ns
t_{ODG}	Output Delay from Gate↓		120	ns
t_{WC}	CLK Delay for Loading	0	55	ns
t_{WG}	Gate Delay for Sampling	−5	50	ns
t_{WO}	OUT Delay from Mode Write		260	ns
t_{CL}	CLK Set Up for Count Latch	−40	45	ns

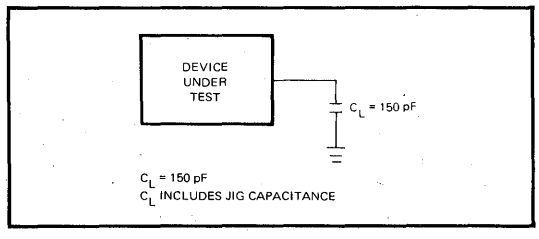
Note 2: In modes 1 and 5 triggers are sampled on each rising clock edge. A second trigger within 120 ns of the rising clock edge may not be detected.

Note 3: Low-going glitches that violate tPWH, tPWL may cause errors requirring counter reprogramming.

A.C. Testing Input, WTPUT Waveform

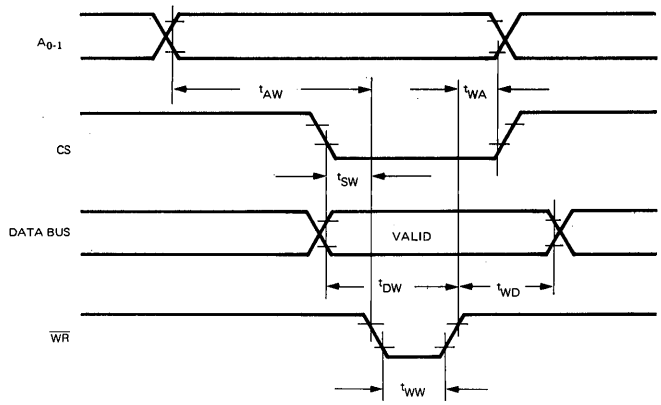


A.C. Testing Load Circuit

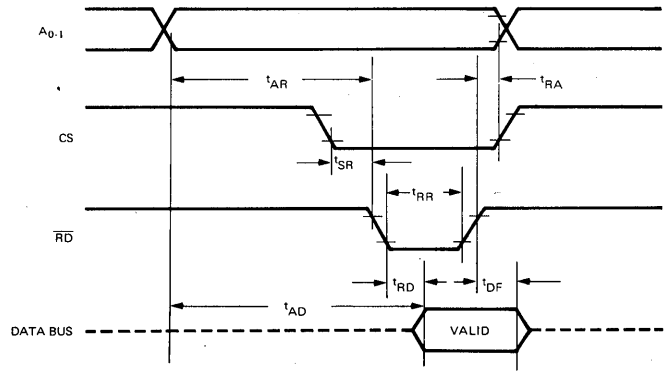


Waveforms

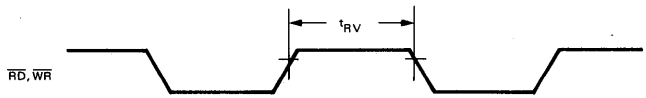
WRITE



READ



RECOVERY



CLOCK AND GATE

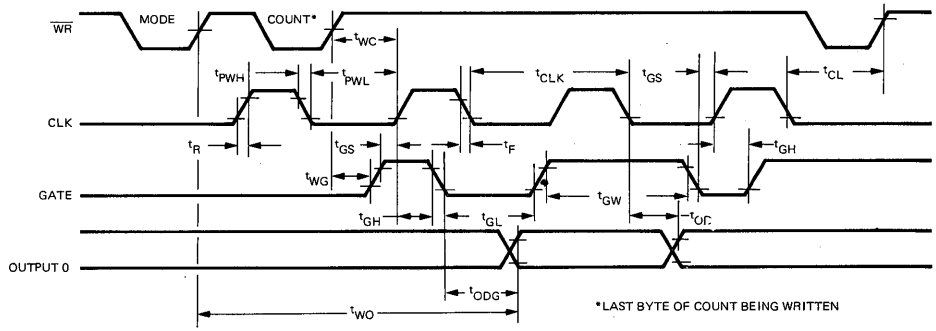


Table 1. Pin Description

Symbol	Pin No.	Type	Name and Function
D_7-D_0	1-8	I/O	Data: Bi-directional three state data bus lines, connected to system data bus.
CLK 0	9	I	Clock 0: Clock Input of Counter 0.
OUT 0	10	O	Output 0: Output of Counter 0.
GATE 0	11	I	Gate 0: Gate Input of Counter 0.
GND	12		Ground: Power supply connection.
V_{CC}	24		Power +5V power supply connection.
$\overline{WR}$	23	I	Write Control: This Input is low during CPU write operations.
$\overline{RD}$	22	I	Read Control: This input is low during CPU read operations.
$\overline{CS}$	21	I	Chip Select: A low on this input enables the 8254 to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.
A_1, A_0	20-19	I	Address: Used to select one of the three Counters or the Control Word Register for read or write operations. Normally connected to the system address bus.
			A_1 A_0 Selects 0 0 Counter 0 0 1 Counter 1 1 0 Counter 2 1 1 Control Word Register
CLK2	18	I	Clock 2: Clock Input of Counter 2.
OUT 2	17	O	Out 2: Output of Counter 2.
GATE2	16	I	Gate 2: Gate Input of Counter 2.
CLK 1	15	I	Clock 1: Clock Input of Counter 1.
GATE1	14	I	Gate 1: Gate Input of Counter 1.
OUT 1	13	O	Out 1: Output of Counter 1.

Functional Description

General

The UM8254 is a programmable interval timer/counter designed for use with microcomputer systems. It is a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The UM8254 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in software, the programmer configures the UM8254 to match his requirements and programs one of the counters for the desired delay. After the desired delay, the UM8254 will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated.

Some of the other counter/timer functions common to microcomputers which can be implemented with the UM8254 are:

- Real time clock
- Event counter
- Digital one-shot
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

Block Diagram

Data Bus Buffer

This 3-state, bi-directional, 8-bit buffer is used to interface the UM8254 to the system bus (see Figure 1).

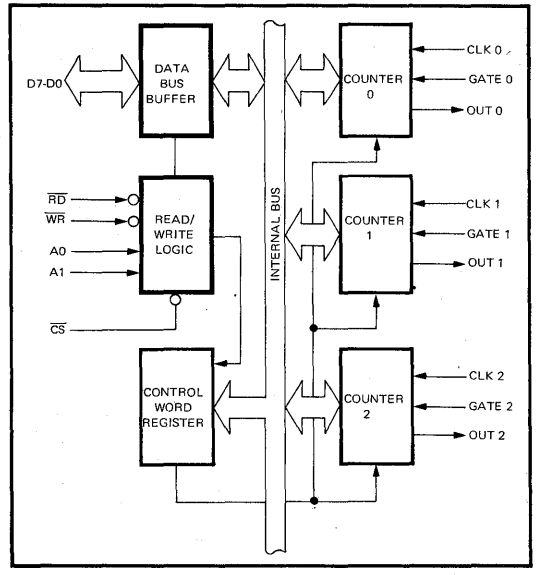


Figure 1. Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions

Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and generates control signals for the other functional blocks of the UM8254. A_1 and A_0 select one of the three counters or the Control Word Register to be read from/written into. A "low" on the $\overline{RD}$ input tells the Um8254 that the CPU is reading one of the counters. A "low" on the $\overline{WR}$ input tells the UM8254 that the CPU is writing either a Control Word or an initial count. Both $\overline{RD}$ and $\overline{WR}$ are qualified by $\overline{CS}$; $\overline{RD}$ and $\overline{WR}$ are ignored unless the UM8254 has been selected by holding $\overline{CS}$ low.

Control Word Register

The Control Word Register (see Figure 2) is selected by the Read/Write Logic when A_1, A_0 = 11. If the CPU then does a write operation to the UM8254, the data is stored in the Control Word Register and is interpreted as a Control Word used to define the operation of the Counters.

The Control Word Register can only be written to; status information is available with the Read-Back Command.

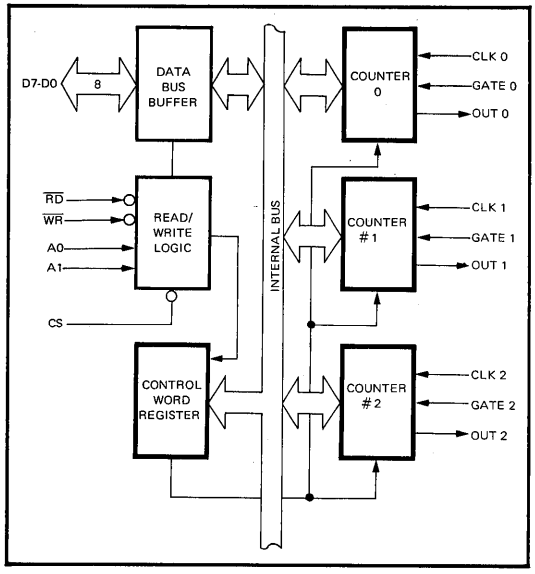


Figure 2. Block Diagram Showing Control Word Register and Counter Functions

Counter 0, Counter 1, Counter 2

These three functional blocks are identical in operation, so only a single Counter will be described. The internal block diagram of a single counter is shown in Figure 3.

The Counters are fully independent. Each Counter may operate in a different Mode.

The Control Word Register is shown in the figure; it is not part of the Counter itself, but its contents determine how the Counter operates.

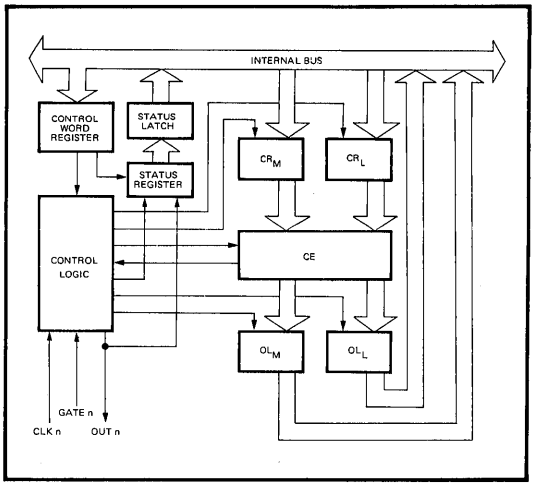


Figure 3. Internal Block Diagram of a Counter

The status register, shown in the Figure, when latched, contains the current contents of the Control Word Register and status of the output and null count flag. (See detailed explanation of the Read-Back command.)

The actual counter is labelled CE (for "Counting Element"). It is a 16-bit presettable synchronous down counter.

OL_M and OL_L are two 8-bit latches. OL stands for "Output Latch"; the subscripts M and L stand for "Most significant byte" and "Least significant byte" respectively. Both are normally referred to as one unit and called just OL. These latches normally "follow" the CE, but if a suitable Counter Latch Command is sent to the UM8254, the latches "latch" the present count until read by the CPU and then return to "following" the CE. One latch at a time is enabled by the counter's Control Logic to drive the internal bus. This is how the 16-bit Counter communicates over the 8-bit internal bus. Note that the CE itself cannot be read; whenever you read the count, it is the OL that is being read.

Similarly, there are two 8-bit registers called CR_M and CR_L (for "Count Register"). Both are normally referred to as one until and called just CR. When a new count is written to the Counter, the count is stored in the CR and later transferred to the CE. The Control Logic allows one register at a time to be loaded from the internal bus. Both bytes are transferred to the CE simultaneously. CR_M and CR_L are cleared when the Counter is programmed. In this way, if the Counter has been programmed for one byte counts (either most significant byte only or least significant byte only) the other byte will be zero. Note that the CE cannot be written into; whenever a count is written, it is written into the CR.

The Control Logic is also shown in the diagram. CLK n, GATE n, and OUT n are all connected to the outside world through the Control Logic.

Write Operations

The programming procedure for the UM8254 is very flexible. Only two conventions need to be remembered:

1) For each Counter, the Control Word must be written before the initial count is written.
2) The initial count must follow the count format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

Since the Control Word Register and the three Counters have separate addresses (selected by the A_1, A_0 inputs), and each Control Word specifies the Counter it applies to (SC0, SC1 bits), no special instruction sequence is required. Any programming sequence that follows the conventions above is acceptable.

A new initial count may be written to a Counter at any time without affecting the Counter's programmed Mode in any way. Counting will be affected as described in the Mode definitions. The new count must follow the programmed count format.

If a Counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same Counter. Otherwise, the Counter will be loaded with an incorrect count.

	A_1	A_0		A_1	A_0
Control Word – Counter 0	1	1	Control Word – Counter 2	1	1
LSB of count – Counter 0	0	0	Control Word – Counter 1	1	1
MSB of count – Counter 0	0	0	Control Word – Counter 0	1	1
Control Word – Counter 1	1	1	LSB of count – Counter 2	1	0
LSB of count – Counter 1	0	1	MSB of count – Counter 2	1	0
MSB of count – Counter 1	0	1	LSB of count – Counter 1	0	1
Control Word – Counter 2	1	1	MSB of count – Counter 1	0	1
LSB of count – Counter 2	1	0	LSB of count – Counter 0	0	0
MSB of count – Counter 2	1	0	MSB of count – Counter 0	0	0

	A_1	A_0		A_1	A_0
Control Word – Counter 0	1	1	Control Word – Counter 1	1	1
Control Word – Counter 1	1	1	Control Word – Counter 0	1	1
Control Word – Counter 2	1	1	LSB of count – Counter 1	0	1
LSB of count – Counter 2	1	0	Control Word – Counter 2	1	1
LSB of count – Counter 1	0	1	LSB of count – Counter 0	0	0
LSB of count – Counter 0	0	0	MSB of count – Counter 1	0	1
MSB of count – Counter 0	0	0	LSB of count – Counter 2	1	1
MSB of count – Counter 1	0	1	MSB of count – Counter 0	0	0
MSB of count – Counter 2	1	0	MSB of count – Counter 2	1	0

Note: In all four examples, all counters are programmed to Read/Write two-byte counts. These are only four of many possible programming sequences.

Figure 4. A Few Possible Programming Sequences

Read Operations

It is often desirable to read the value of a Counter without disturbing the count in progress. This is easily done in the UM8254.

There are three possible methods for reading the Counters. The first is through the Read-Back command. The second is a simple read operation of the Counter, which is selected with the A_1, A_0 inputs. The only requirement is that 1) the CLK input of the selected Counter must be inhibited by using either the GATE input or external logic; or 2) the count must first be latched. Otherwise, the count may be in process of changing when it is read, giving an undefined result.

UM8254 System Interface

The UM8254 is a component of Microcomputer Systems and interfaces in the same manner as all other peripherals of the family. It is treated by the systems software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A_0, A_1 connect to the A_0, A_1 address bus signals of the CPU. The CS can be derived directly from the address bus using a linear select method. Or it can be connected to the output of a decoder, such as an UM8205 for larger systems.

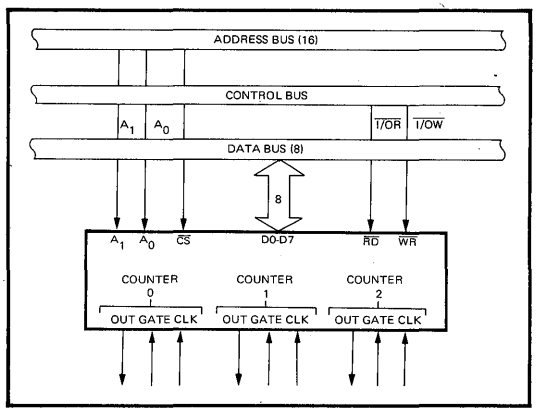


Figure 5. UM8254 System Interface

Operational Description

General

After power-up, the state of the UM8254 is undefined. The Mode, count value, and output of all Counters are undefined.

How each Counter operates is determined when it is programmed. Each Counter must be programmed before it can be used. Unused counters need not be programmed.

Programming the UM8254

Counters are programmed by writing a Control Word and then an initial count.

All Control Words are written into the Control Word Register, which is selected when A_1, A_0 = 11. The Control Word itself specifies which Counter is being programmed.

By contrast, initial counts are written into the Counters, not the Control Word Register. The A_1, A_0 inputs are used to select the Counter to be written into. The format of the initial count is determined by the Control Word used.

Control Word Format

A_1, A_0 = 11, $\overline{CS}$ = 0, $\overline{RD}$ = 1, WR = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC–Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (See Read Operations)

RW–Read/Write:

RW1	RW0	
0	0	Counter Latch Command (see Read Operations)
0	1	Read/Write least significant byte only.
1	0	Read/Write most significant byte only.
1	1	Read/Write least significant byte first, then most significant byte.

M–MODE:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD:

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

Note: Don't care bits (X) should be 0 to insure compatibility with future UMC products.

Figure 6. Control Word Format

Counter Latch Command

The other method involves a special software command called the "Counter Latch Command" Like a Control Word, this command is written to the Control Word Register, which is selected when A_1, A_0 = 11. Also like a Control Word, the SC0, SC1 bits select one of the three Counters, but two other bits, D5 and D4, distinguish this command from a Control Word.

A_1, A_0 = 11; CS = 0; RD = 1; WR = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	0	0	X	X	X	X

SC1, SC0 – specify counter to be latched

SC1	SC0	Counter
0	0	0
0	1	1
1	0	2
1	1	Read-Back Command

D5, D4–00 designates Counter Latch Command
X – don't care

Note: Don't care bits (X) should be 0 to insure compatibility with future UMC products.

Figure 7. Counter Latching Command Format

The selected Counter's output latch (OL) latches the count at the time the Counter Latch Command is received. This count is held in the latch until it is read by the CPU (or until the Counter is reprogrammed). The count is then unlatched automatically and the OL returns to "following" the counting element (CE). This allows reading the contents of the Counters "on the fly" without affecting counting in progress. Multiple Counter Latch Commands may be used to latch more than one Counter. Each latched Counter's OL holds its count until it is read. Counter Latch Commands do not affect the programmed Mode of the Counter in any way.

If a Counter is latched and then, some time later, latched again before the count is read, the second Counter Latch Command is ignored. The count read will be the count at the time the first Counter Latch Command was issued.

With either method, the count must be read according to the programmed format; specifically, if the Counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other; read or write or programming operations of other Counters may be inserted between them.

Another feature of the UM8254 is that reads and writes of the same Counter may be interleaved; for example, if the Counter is programmed for two byte counts, the following sequence is valid.

1. Read least significant byte.
2. Write new least significant byte.
3. Read most significant byte.
4. Write new most significant byte.

If a Counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between reading the first and second byte to another routine which also reads from that same Counter. Otherwise, an incorrect count will be read.

Read-Back Command

The read-back command allows the user to check the count value, programmed Mode, and current state of the OUT pin and Null Count flag of the selected counter(s).

The command is written into the Control Word Register and has the format shown in Figure 8. The command applies to the counters selected by setting their corresponding bits D3, S2, D1 = 1.

A_0, A_1 = 11, $\overline{CS}$ = 0, $\overline{RD}$ = 1, $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	$\overline{COUNT}$	$\overline{STATUS}$	CNT2	CNT1	CNT0	0

D_5: 0 = Latch count of selected counter(s)
D_4: 0 = Latch status of selected counter(s)
D_3: 1 = Select counter 2
D_2: 1 = Select counter 1
D_1: 1 = Select counter 0
D_0: Reserved for future expansion; must be 0

Figure 8. Read-Back Command Format

The read-back command may be used to latch multiple counter output latches (OL) by setting the $\overline{COUNT}$ bit D5 = 0 and selecting the desired counter(s). This single command is functionally equivalent to several counter latch commands, one for each counter latched. Each counter's latched count is held until it is read (or the counter is reprogrammed). That counter is automatically unlatched when read, but other counters remain latched until they are read. If multiple count read-back commands are issued to the same counter without reading the count, all but the first are ignored; i.e., the count which will be read is the count at the time the first read-back command was issued.

The read-back command may also be used to latch status information of selected counter(s) by setting $\overline{STATUS}$ bit D4=0. Status must be latched to be read; status of a counter is accessed by a read from that counter.

The counter status format is shown in Figure 9. Bits D5 through D0 contain the counter's programmed Mode exactly as written in the last Mode Control Word. OUTPUT bit D7 contains the current state of the OUT pin. This allows the user to monitor the counter's output via software, possibly eliminating some hardware from a system.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
OUTPUT	NULL COUNT	RW1	RW0	M2	M1	M0	BCD

D_7 1 = Out pin is 1
0 = Out pin is 0
D_6 1 = Null count
0 = Count available for reading
D_5-D_0 = Counter programmed mode (See Figure 7)

Figure 9. Status Byte

NULL COUNT bit D6 indicates when the last count written to the counter register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the Mode of the counter and is described in the Mode Definitions, but until the count is loaded into the counting element (CE), it can't be read from the counter. If the count is latched or read before this time, the count value will not reflect the new count just written. The operation of Null Count is shown in Figure 10.

This Action:	Causes:
A. Write to the control word register.(1)	Null count = 1
B. Write to the count register (CR):(2)	Null count = 1
C. New count is loaded into CE (CR→CE):	Null count = 0

(1) Only the counter specified by the control word will have its null count set to 1. Null count bits of other counters are unaffected.

(2) If the counter is programmed for two byte counts (least significant byte then most significant byte) null count goes to 1 when the second byte is written.

Figure 10. Null Count Operation

If multiple status latch operations of the counter(s) are performed without reading the status, all but the first are ignored; i.e., the status that will be read is the status of the counter at the time the first status read-back command was issued.

Both count and status of the selected counter(s) may be latched simultaneously by setting both COUNT and STATUS bits D5, D4 = 0. This is functionally the same as issuing two separate read-back commands at once, and the above discussions apply here also. Specifically, if multiple count and/or status read-back commands are issued to the same counter(s) without any intervening reads, all but the first are ignored. This is illustrated in Figure 11.

Command								Descriptions	Results
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	1	0	0	0	0	1	0	Read back count and status of Counter 0	Count and status latched for Counter 0
1	1	1	0	0	1	0	0	Read back status of Counter 1	Status latched for Counter 1
1	1	1	0	1	1	0	0	Read back status of Counters 2, 1	Status latched for Counter 2, but not Counter 1
1	1	0	1	1	0	0	0	Read back count of Counter 2	Count latched for Counter 2
1	1	0	0	0	1	0	0	Read back count and status of Counter 1	Count latched for Counter 1, but not status
1	1	1	0	0	0	1	0	Read back status of Counter 1	Command ignored, status already latched for Counter 1

Figure 11. Read-Back Command Example

If both count and status of a counter are latched, the first read operation of that counter will return latched status, regardless of which was latched first. The next one or two reads (depending on whether the counter is programmed for one or two type counts) return latched count. Subsequent reads return unlatched count.

CS	RD	WR	A_1	A_0	
0	1	0	0	0	**Write into Counter 0**
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	No-Operation (3-State)
1	X	X	X	X	No-Operation (3-State)
0	1	1	X	X	No-Operation (3-State)

Figure 12. Read/Write Operations Summary

Mode Definitions

The following are defined for use in describing the operation of the UM8254.

CLK pulse: a rising edge, then a falling edge, in that order, of a Counter's CLK input.

trigger: a rising edge of a Counter's GATE input.

Counter loading: the transfer of a count from the CR to the CE (refer to the "Functional Description")

MODE 0: Interrupt on Terminal Count

Mode 0 is typically used for event counting. After the Control Word is written, OUT is initially low, and will remain low until the Counter reaches zero. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written into the Counter.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

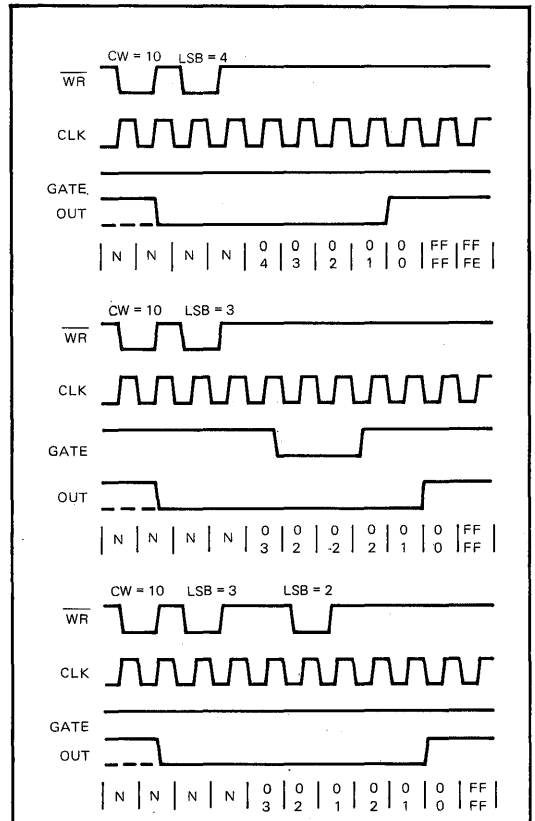
After the Control Word and initial count are written to a Counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not go high untill N + 1 CLK pulses after the initial count is written.

If a new count is written to the Counter, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1) Writing the first byte disables counting. OUT is set low immediately (no clock pulse required).
2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the counting sequence to by synchronized by software. Again, OUT does not go high until N + 1 CLK pulses after the new count of N is written.

If an initial count is written while GATE = 0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later; no CLK pulse is needed to load the Counter as this has already been done.



Note: THE FOLLOWING CONVENTIONS APPLY TO ALL MODE TIMING DIAGRAMS:
1. COUNTERS ARE PROGRAMMED FOR BINARY (NOT BCD) COUNTING AND FOR READING/WRITING LEAST SIGNIFICANT BYTE(LSB) ONLY.
2. THE COUNTER IS ALWAYS SELECTED (CS ALWAYS LOW).
3. CW STANDS FOR "CONTROL WORD". CW=10 MEANS A CONTROL WORD OF 10, HEX IS WRITTEN TO THE COUNTER.
4. LSB STANDS FOR "LEAST SIGNIFICANT BYTE" OF COUNT.
5. NUMBERS BELOW DIAGRAMS ARE COUNT VALUES.
   THE LOWER NUMBER IS THE LEAST SIGNIFICANT BYTE.
   THE UPPER NUMBER IS THE MOST SIGNIFICANT BYTE. SINCE THE COUNTER IS PROGRAMMED TO READ/WRITE LSB ONLY, THE MOST SIGNIFICANT BYTE CANNOT BE READ.
   N STANDS FOR AN UNDEFINED COUNT.
   VERTICAL LINES SHOW TRANSITIONS BETWEEN COUNT VALUES.

Figure 13. Mode 0

MODE 1: Hardware Retriggerable One-Shot

Out will be initially high. OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and will remain low until the Counter reaches zero. OUT will then go high and remain high until the CLK pulse after the next trigger.

After writing the Control Word and initial count, the Counter is armed. A trigger results in loading the Counter and setting OUT low on the next CLK pulse, thus starting the one-shot pulse. An initial count of N will result in a one-shot pulse N CLK cycles in duration. The one-shot is retriggerable, hence OUT will remain low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.

If a new count is written to the Counter during a one-shot pulse, the current one-shot is not affected unless the Counter is retriggered. In that case, the Counter is loaded with the new count and the one-shot pulse continues until the new count expires.

MODE 2: Rate Generator

This Mode functions like a divide-by-N counter. It is typically used to generate a Real Time Clock interrupt. Out will initially be high. When the initial count has decremented to 1, OUT goes low for one CLK pulse. OUT then goes high again, the Counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the Counter with the initial count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. OUT goes low N CLK Pulses after the initial count is written. This allows the Counter to be synchronized by software also.

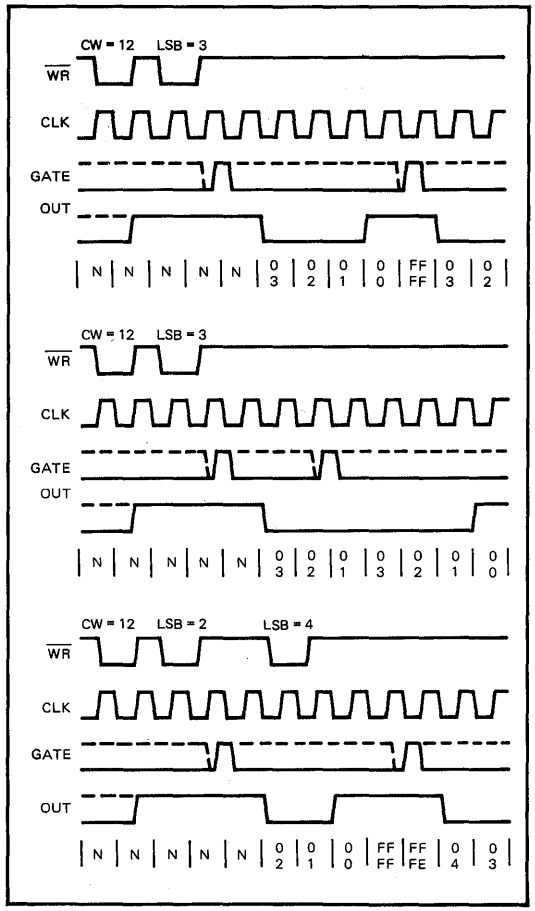
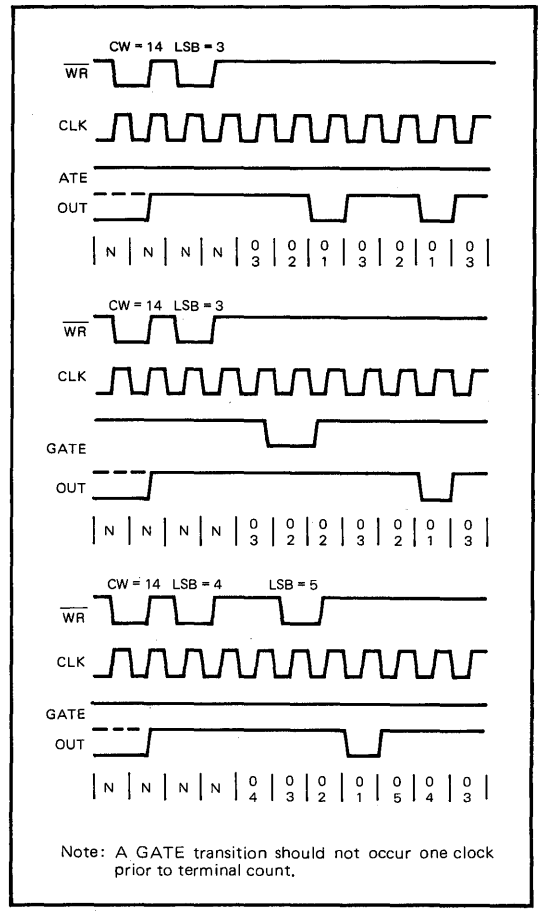


Figure 14. Mode 1



Note: A GATE transition should not occur one clock prior to terminal count.

Figure 15. Mode 2

Peripheral IC

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current period, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current counting cycle. In mode 2, a COUNT of 1 is illegal.

MODE 3: Square Wave Mode

Mode 3 is typically used for Baud rate generation. Mode 3 is similar to Mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the initial count has expired, OUT goes low for the remainder of the count. Mode 3 is periodic; the sequence above is repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately; no CLK pulse is required. A trigger reloads the Counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current half-cycle.

Mode 3 is implemented as follows:

Even counts: OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires OUT changes value and the Counter is reloaded with the initial count. The above process is repeated indefinitely.

Odd counts: OUT is initially high. The initial count minus one (an even number) is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. One CLK pulse after the count expires, OUT goes low and the Counter is reloaded with the initial count minus one. Succeeding CLK pulses decrement the count by two. When the count expires, OUT goes high again and the Counter is reloaded with the initial count minus one. The above process is repeated indefinitely. So for odd counts, OUT will be high for (N+1)/2 counts and low for (N−1)/2 counts.

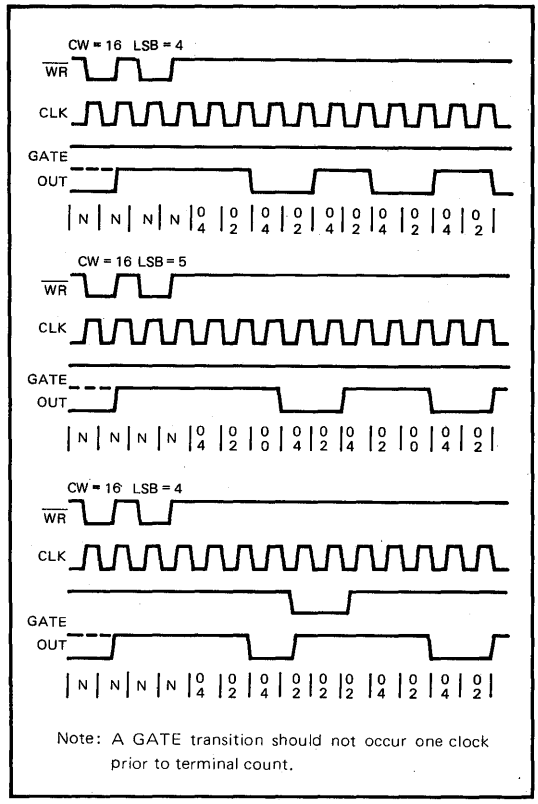


Figure 16. Mode 3

MODE 4: Software Triggered Strobe

OUT will be initially high. When the initial count expires, OUT will go low for one CLK pulse and then go high again. The counting sequence is "triggered" by writing the initial count.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N+1 CLK pulses after the initial count is written.

If a new count is written during counting, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1) Writing the first byte has no effect on counting.
2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the sequence to be "retriggered" by software. OUT strobes low N+1 CLK pulses after the new count of N is written.

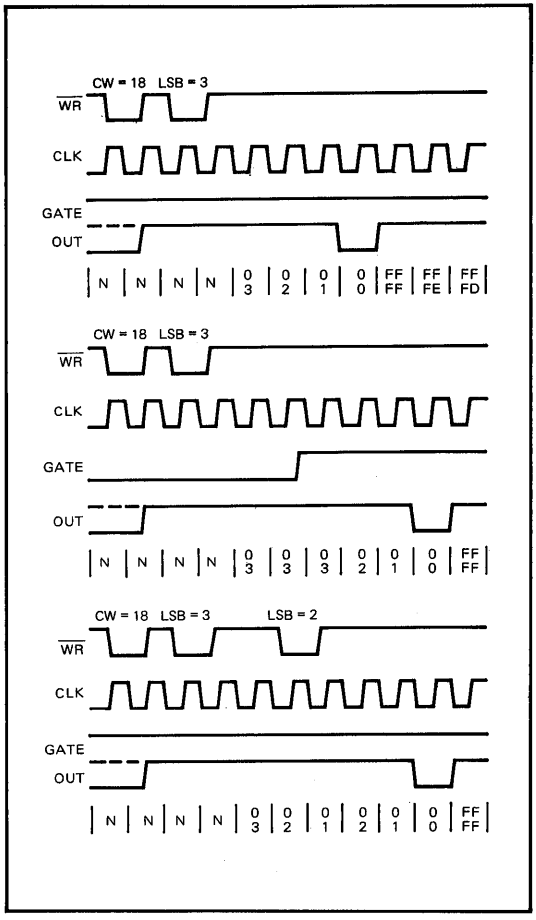


Figure 17. Mode 4

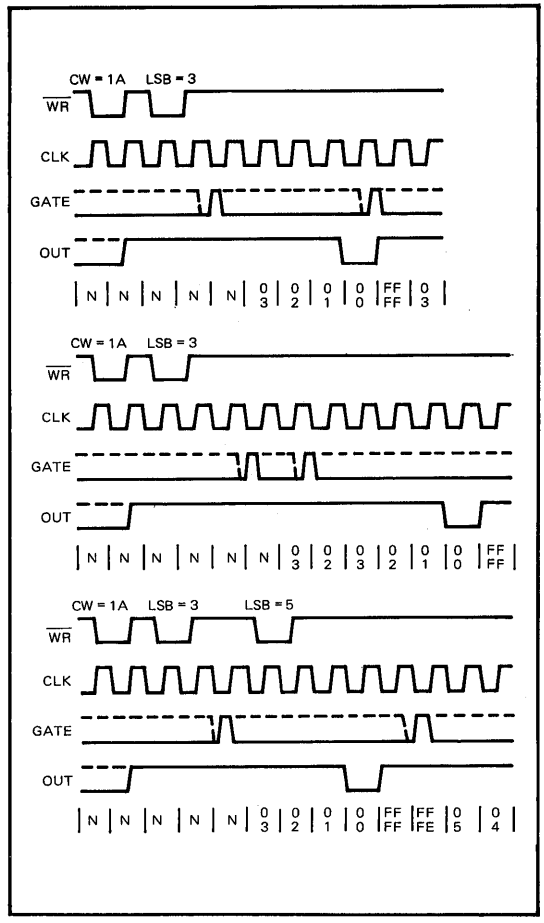


Figure 18. Mode 5

MODE 5: Hardware Triggered Strobe (Retriggerable)

OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one CLK pulse and then go high again.

After writing the Control Word and initial count, the counter will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N+1 CLK pulses after a trigger.

A trigger results in the Counter being loaded with the initial count on the next CLK pulse. The counting sequence is retriggerable. OUT will not strobe low for N+1 CLK pulses after any trigger. GATE has no effect on OUT.

If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written but before the current count expires, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from there.

Signal Status Modes	Low or Going Low	Rising	High
0	Disables counting		Enables counting
1	—	1) Initiates counting 2) Resets output after next clock	—
2	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
3	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
4	Disables counting	—	Enables counting
5	—	Initiates counting	—

Figure 19. Gate Pin Operations Summary

Mode	Min Count	Max Count
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0
5	1	0

Note: 0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

Figure 20. Minimum and Maximum Initial Counts

Operation Common to All Modes

Programming

When a Control Word is written to a Counter, all Control Logic is immediately reset and OUT goes to a known initial state; no CLK pulses are required for this.

Gate

The GATE input is always sampled on the rising edge of CLK. In Modes 0, 2, 3, and 4 the GATE input is level sensitive, and the logic level is sampled on the rising edge of CLK. In Modes 1, 2, 3, and 5 the GATE input is rising-edge sensitive. In these Modes, a rising edge of GATE (trigger) sets an edge-sensitive flip-flop in the Counter. This flip-flop is then sampled on the next rising edge of CLK; the flip-flop is reset immediately after it is sampled. In this way, a trigger will be detected no matter when it occurs – a high logic level does not have to be maintained until the next rising edge of CLK. Note that in Modes 2 and 3, the GATE input is both edge- and level- sensitive. In Modes 2 and 3, if a CLK source other than the system clock is used, GATE should be pulsed immediately following WR of a new count value.

Counter

New counts are loaded and Counters are decremented on the falling edge of CLK.

The largest possible initial count is 0; this is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

The Counter does not stop when it reaches zero. In Modes 0, 1, 4, and 5 the Counter "wraps around" to the highest count, either FFFF hex for binary counting or 9999 for BCD counting, and continues counting. Modes 2 and 3 are periodic; the Counter reloads itself with the initial count and continues counting from there.

UM8259A

Programmable Interrupt Controller

Features

- iAPX86, iAPX88 compatible
- MCS-80®, MCS-85® compatible
- Eight-level priority controller
- Expandable to 64 levels
- Programmable interrupt modes
- Individual request mask capability
- Single +5V supply (no clocks)
- 28-pin dual-in-line package
- Available in EXPRESS
- – Standard temperature range
  – Extended temperature range

General Description

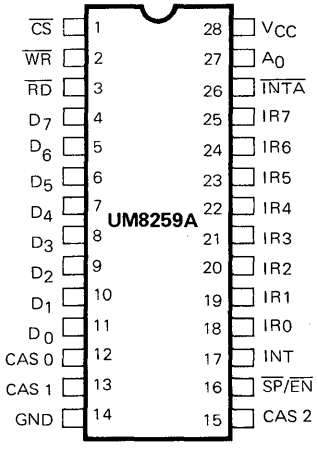
The UM8259A Programmable Interrupt Controller handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without additional circuitry. Packaged in a 28-pin DIP, it uses NMOS technology and requires a single +5V supply. Circuitry is static, requiring no clock input.

The UM8259A is designed to minimize the software and real time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

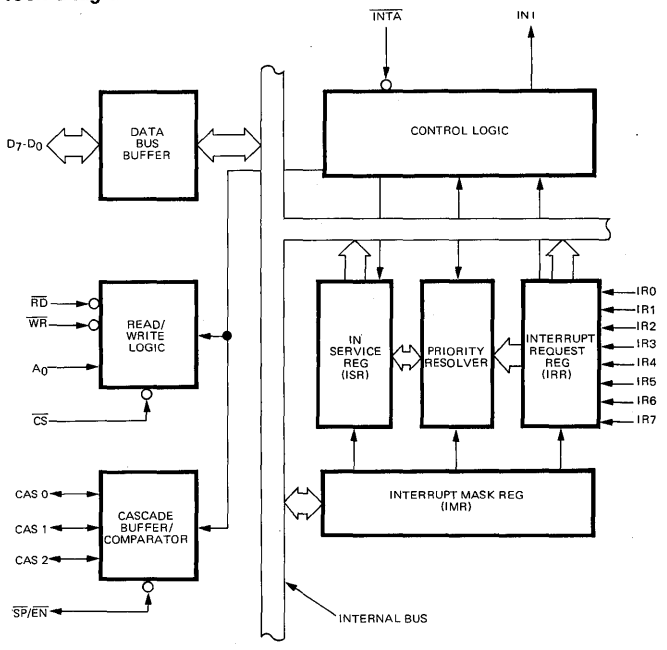
The UM8259A is fully compatible with the Intel 8259A. Software originally written for the 8259A will operate the UM8259A in all 8259A equivalent modes.

*iAPX86, iAPX88, MCS-80 and MCS-85 are all trademarks of Intel microsystem.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . –65°C to +150°C
Voltage on Any Pin with
Respect to Ground . . . . . –0.5V to +7V
Power Dissipation . . . . . 1 Watt

*Comments

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Min.	Max.	Units	Conditions
V_{IL}	Input Low Voltage	–0.5	0.8	V	
V_{IH}	Input High Voltage	2.0*	V_{CC}+ 0.5V	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = –400μA
$V_{OH(INT)}$	Interrupt Output High Voltage	3.5		V	I_{OH} = –100μA
		2.4		V	I_{OH} = –400μA
I_{LI}	Input Load Current	–10	+10	μA	0V V_{IN} V_{CC}
I_{LOL}	Output Leakage Current	–10	+10	μA	0.45V V_{OUT} V_{CC}
I_{CC}	V_{CC} Supply Current		85	mA	
I_{LIR}	IR Input Load Current		–300	μA	V_{IN} = 0
			10	μA	V_{IN} = V_{CC}

*Note: For Extended Temperature EXPRESS V_{IH} = 2.3V.

Capacitance

(T_A = 25°C; V_{CC} = GND = 0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1 MHZ
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to V_{SS}

A.C. Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 10%)

TIMING REQUIREMENTS

Symbol	Parameter	Min.	Max.	Units	Conditions
TAHRL	A0/$\overline{CS}$ Setup to $\overline{RD}$/$\overline{INTA}$↓	0		ns	
THRAX	A0/$\overline{CS}$ Hold after $\overline{RD}$/$\overline{INTA}$↑	0		ns	
TRLRH	$\overline{RD}$ Pulse Width	235		ns	
TAHWL	A0/$\overline{CS}$ Setup to $\overline{WR}$↓	0		ns	
TWHAX	A0/$\overline{CS}$ Hold after $\overline{WR}$↑	0		ns	
TWLWH	$\overline{WR}$ Pulse Width	290		ns	
TDVWH	Data Setup to $\overline{WR}$↑	240		ns	
TWHDX	Data Hold after $\overline{WR}$↑	0		ns	
TJLJH	Interrupt Request Width (Low)	100		ns	See Note 1
TCVIAL	Cascade Setup to Second or Third $\overline{INTA}$↓ (Slave only)	55		ns	
TRHRL	End of $\overline{RD}$ to next $\overline{RD}$ End of $\overline{INTA}$ to next $\overline{INTA}$ within an $\overline{INTA}$ sequence only	160		ns	
TWHWL	End of $\overline{WR}$ to next $\overline{WR}$	190		ns	

A.C. Characteristics (Continued)

Symbol	Parameter	Min.	Max.	Unit	Conditions
*TCHCL	End of Command to next Command (Not same command type)	500		ns	
	End of $\overline{INTA}$ sequence to next $\overline{INTA}$ sequence.				

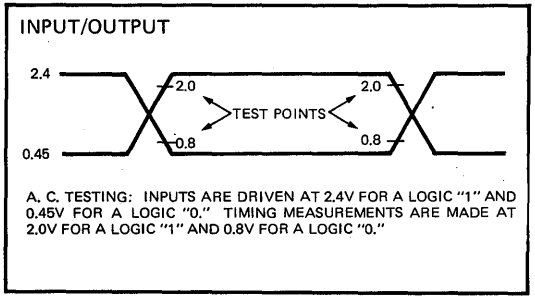
*Worst case timing for TCHCL in an actual microprocessor system is typically much greater than 500 ns (i.e. 8085A = 1.6μs, 8085A-2 = 1 μs, 8086 = 1 μs, 8086-2 = 625 ns)

Note: This is the low time required to clear the input latch in the edge triggered mode.

Timing Responses

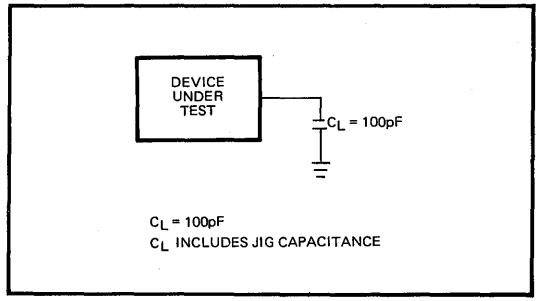
Symbol	Parameter	Min.	Max.	Units	Conditions
TRLDV	Data Valid from $\overline{RD}/\overline{INTA}\downarrow$		200	ns	C of Data Bus = 100 pF
TRHDZ	Data Float after $\overline{RD}/\overline{INTA}\uparrow$	10	100	ns	C of Data Bus Max text C = 100 pF Min. test C = 15 pF
TJHIH	Interrupt Output Delay		350	ns	
TIALCV	Cascade Valid from First $\overline{INTA}$ (Master Only)		565	ns	C_{INT} = 100 pF
TRLEL	Enable Active from $\overline{RD}\downarrow$ or $\overline{INTA}\downarrow$		125	ns	$C_{CASCADE}$ = 100 pF
TRHEH	Enable Inactive from $\overline{RD}\uparrow$ or $\overline{INTA}\uparrow$		150	ns	
TAHDV	Data Valid from Stable Address		200	ns	
TCVDV	Cascade Valid to Valid Data		300	ns	

A.C. Testing Input, Output Waveform



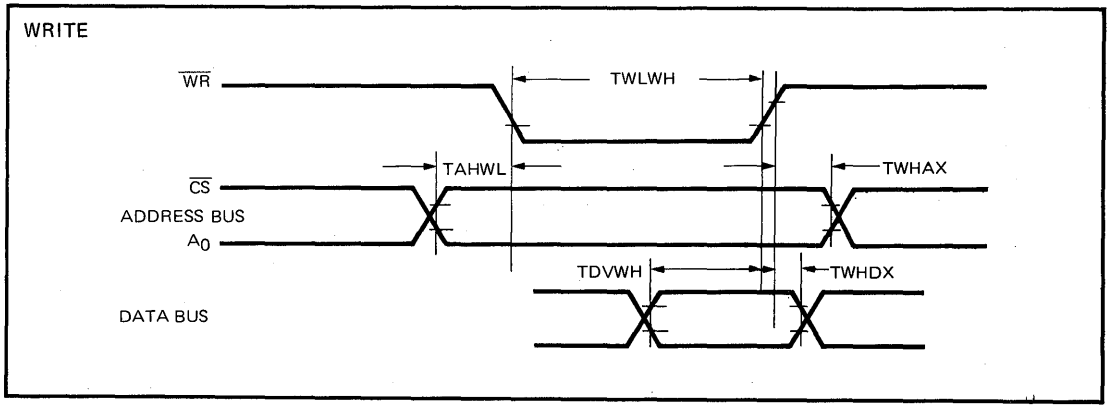
A. C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0." TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0."

A.C. Testing Load Circuit



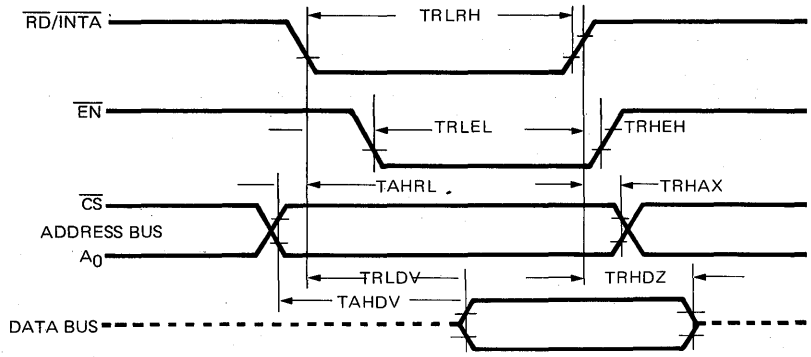
C_L = 100pF
C_L INCLUDES JIG CAPACITANCE

Waveforms

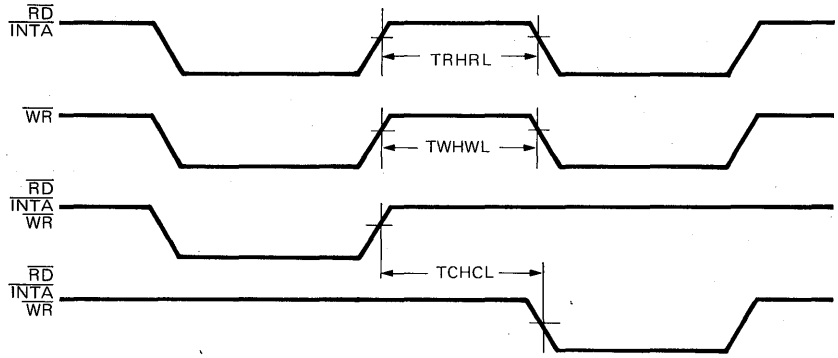


Waveforms (Continued)

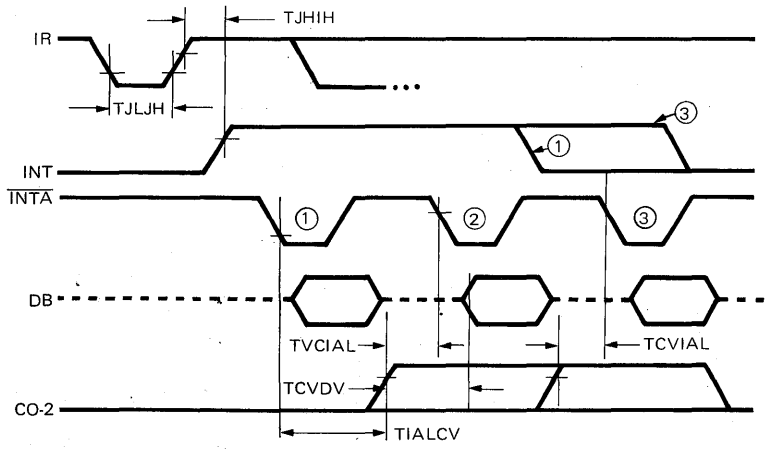
READ/INTA



OTHER TIMING



INTA SEQUENCE



Notes: Interrupt output must remain HIGH at least until leading edge of first INTA.

1. Cycle 1 in iAPX86, iAPX88 systems, the Data Bus is not active.

Pin Description

Symbol	Pin No.	Type	Name and Functions
V_{CC}	28	I	Supply: +5V Supply.
GND	14	I	Ground.
$\overline{CS}$	1	I	Chip Select: A low on this pin enables RD and WR communication between the CPU and the UM8259A. INTA functions are independent of CS.
$\overline{WR}$	2	I	Write: A low on this pin when CS is low enables the UM8259A to accept command words from the CPU.
$\overline{RD}$	3	I	Read: A low on this pin when CS is low enables the Um8259A to release status onto the data bus for the CPU.
D7–D0	4–11	I/O	Bidirectional Data Bus: Control, status and interrupt-vector information is transferred via this bus.
CAS_0–CAS_2	12, 13, 15	I/O	Cascade Lines: The CAS lines form a private UM8259A bus to control a multiple UM8259A structure. These pins are outputs for a master UM8259A and inputs for a slave UM8259A.
$\overline{SP}/\overline{EN}$	16	I/O	Slave Program/Enable Buffer: This is a dual function pin. When in the Buffered Mode it can be used as an output to control buffer transceivers (EN). When not in the buffered mode it is used as an input to designate a master (SP = 1) of slave (SP = 0).
INT	17	O	Interrupt: This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
IR_0–IR_7	18–25	I	Interrupt Requests: Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on an IR input (Level Triggered Mode).
$\overline{INTA}$	26	I	Interrupt Acknowledge: This pin is used to enable UM8259A interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
A_0	27	I	A0 Address Line: This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ pins. It is used by the UM8259A to decipher various Command Words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A0 address line (A1 for iAPX 86, 88).

Functional Description

Interrupts in Microcomputer Systems

Microcomputer system design requires that I/O devices such as keyboards, displays, sensors and other components receive servicing in an efficient manner so that large amounts of the total system tasks can be assumed by the microcomputer with little or no effect on throughput.

The most common method of servicing such devices is the Polled approach. This is where the processor must test each device in sequence and in effect "ask" each one if it needs servicing. It is easy to see that a large portion of the main program is looping through this continuous polling cycle and that such a method would have a serious, detrimental effect on system throughput, thus limiting the tasks that could be assumed by the microcomputer and reducing the cost effectiveness of using such devices.

A more desirable method would be one that would allow the microprocessor to be executing its main program and only stop to service peripheral devices when it is told to do so by the device itself. In effect, the method would provide an external asynchronous input that would inform the processor that it should complete whatever instruction that is currently being executed and fetch a new routine that will service the requesting device. Once this servicing is complete, however, the processor would resume exactly where it left off.

This method is called Interrupt. It is easy to see that system throughput would drastically increase, and thus more task could be assumed by the microcomputer to further enhance its cost effectiveness.

The Programmable Interrupt Controller (PIC) functions as an overall manager in an Interrupt-Driven system environment. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced, and issues an interrupt to the CPU based on this determination.

Each peripheral device or structure usually has a special program or "routine" that is associated with its specific functional or operational requirements; this is referred to as a "service routine". The PIC, after issuing an interrupt to the CPU, must somehow input information into the CPU that can "point" the Program Counter to the Service routine associated with the requesting device. This "pointer" is an address in a vectoring table and will often be referred to, in this document, as vectoring data.

The UM8259A

The UM8259A is a devicespecifically designed for use in real time, interrupt driven microcomputer systems. It manages eight levels or requests and has built-in features for expandability to other UM8259A's (up to 64 levels). It is programmed by the system's software as an I/O peripheral. A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the UM8259A can be configured to match his system requirements. The priority modes can be changed or reconfigured dynamically at any time during the main program. This means that the complete interrupt structure can be defined as required, based on the total system environment.

Interrupt Request Register (IRR) and In-Service Register (ISR)

The Interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR is used to store all the interrupt levels which are requesting service; and the ISR is used to store all the interrupt levels which are being serviced.

Priority Resolver

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during $\overline{INTA}$ pulse.

Interrupt Mask Register (IMR)

The IMR stores the bits which mask the interrupt lines to be masked. The IMR operates on the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

INT (Interrupt)

This output goes directly to the CPU interrupt input. The V_{OH} level on this line is designed to be fully compatible with the 8080A, 8085A and 8086 input levels.

$\overline{INTA}$ (Interrupt Acknowledge)

$\overline{INTA}$ pulses will cause the UM8259A to release vectoring information onto the data bus. The format of this data depends on the system mode (μPM) of the UM8259A.

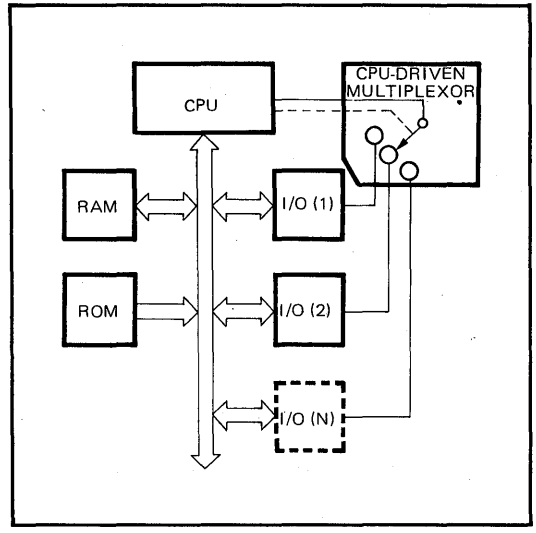


Figure 1a. Polled Method

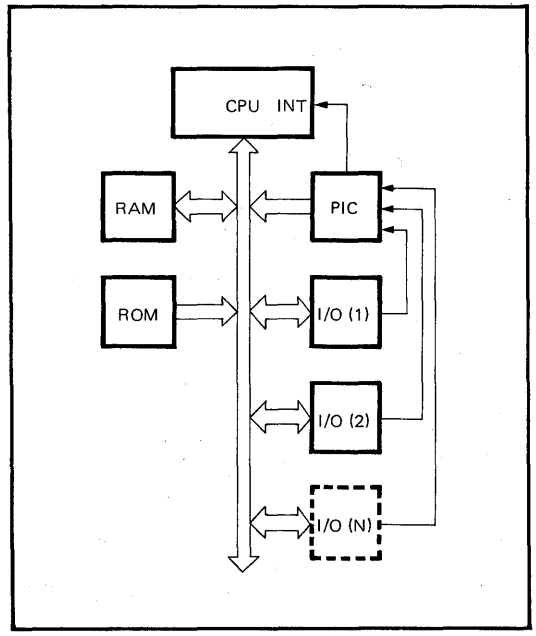


Figure 1b. Interrupt Method

Data Bus Buffer

This 3-state, bidirectional 8-bit buffer is used to interface the UM8259A to the system Data Bus. Control words and status information are transferred through the Data Bus Buffer.

Read/Write Control Logic

The function of this block is to accept OUT put commands from the CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the UM8259A to be transferred onto the Data Bus.

$\overline{CS}$ (Chip Select)

A LOW on this input enables the UM8259A. No reading or writing of the chip will occur unless the device is selected.

$\overline{WR}$ (Write)

A LOW on this input enables the CPU to write control words (ICWs and OCWs) to the UM8259A.

$\overline{RD}$ (Read)

A LOW on this input enables the UM8259A to send the status of the interrupt Request Register (IRR). In Service Register (ISR), the Interrupt Mask Register (IMR), or the Interrupt level onto the Data Bus.

A_0

This input signal is used in conjunction with $\overline{WR}$ and $\overline{RD}$ signals to write commands into the various command registers, as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines.

The Cascade Buffer/Comparator

This function block stores and compares the IDs of all UM8259A's used in the system. The associated three I/O pins (CAS0–2) are outputs when the UM8259A is used as a master and are inputs when the UM8259A is used as a slave. As a master, the UM8259A sends the ID of the interrupting slave device onto the CAS0–2 lines. The slave thus selected will send its preprogrammed subroutine address onto the Data Bus during the next one or two consecutive $\overline{INTA}$ pulses. (See section "Cascading the UM8259A".)

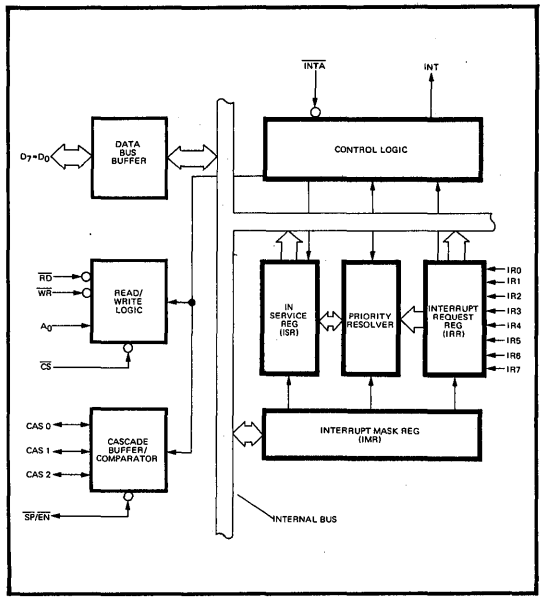


Figure 2a. UM8259A Block Diagram

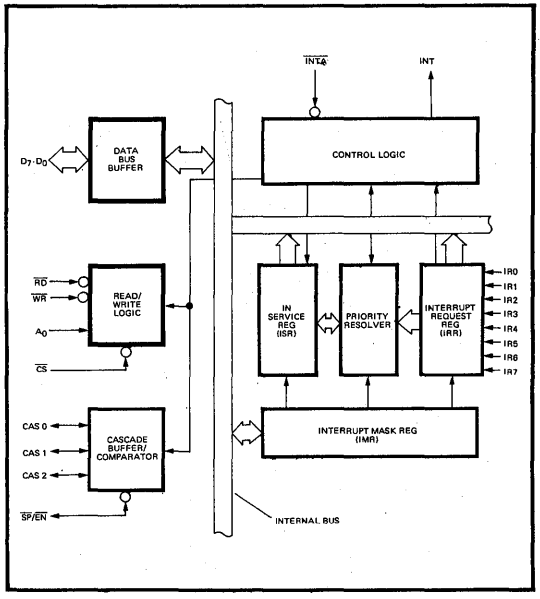


Figure 2b. UM8259A Block Diagram

Peripheral IC

Interrupt Sequence

The powerful features of the UM8259A in a microcomputer system are its programmability and the interrupt routine addressing capability. The latter allows direct or indirect jumping to the specific interrupt routine requested without any polling of the interrupting devices. The normal sequence of events during an interrupt depends on the type of CPU being used.

The events occur as follows in an MCS-80/85 system:

1. One of more of the INTERRUPT REQUEST lines (IR7–0) are raised high, setting the corresponding IRR bit(s).
2. The UM8259A evaluates these requests, and sends an INT to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an $\overline{INTA}$ pulse.
4. Upon receiving an $\overline{INTA}$ from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The UM8259A will also release a CALL instruction code (11001101) onto the 8-bit Data Bus through its D7–0 pins.
5. This CALL Instruction will initiate two more $\overline{INTA}$ pulses to be sent to the UM8259A from the CPU group.
6. These two $\overline{INTA}$ pulses allow the UM8259A to release its preprogrammed subroutine address onto the Data Bus. The lower 8-bit address is released at the first $\overline{INTA}$ pulse and the higher 8-bit address is released at the second $\overline{INTA}$ pulse.
7. This completes the 3-byte CALL instruction released by the UM8259A. In the AEOI mode the ISR bit is reset at the end of the third $\overline{INTA}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

The events occurring in an iAPX 86 system are the same until step 4.

4. Upon receiving an $\overline{INTA}$ from the CPU group, the highest priority ISR bit is set and the corresponding IRR bit is reset. The UM8259A does not drive the Data Bus during this cycle.
5. The iAPX 86/10 will initiate a second $\overline{INTA}$ pulse. During this pulse, the UM8259A releases an 8-bit pointer onto the Data Bus where it is read by the CPU.
6. This completes the interrupt cycle. In the AEOI mode the ISR bit is reset at the end of the second $\overline{INTA}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

If no interrupt request is present at step 4 of either sequence (i.e., the request was too short in duration) the UM8259A will issue an interrupt level 7. Both the vectoring bytes and the CAS lines will look like an interrupt level 7 was requested.

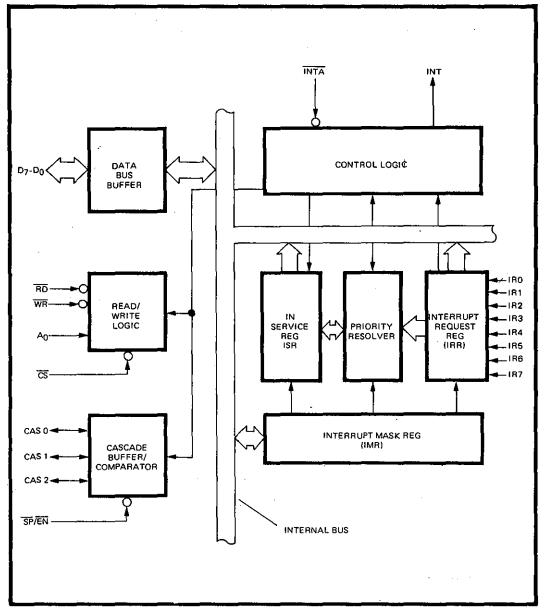


Figure 2c. UM8259A Block Diagram

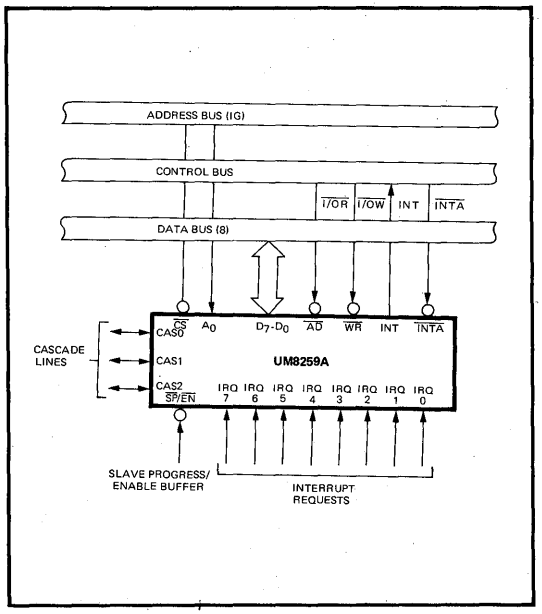


Figure 3. UM8259A Interface to Standard System Bus

Interrupt Sequence Outputs

MCS-80®, MCS-85®

This sequence is timed by three $\overline{INTA}$ pulses. During the first $\overline{INTA}$ pulse the CALL opcode is enabled onto the data bus.

Content of First Interrupt Vector Byte

	D7	D6	D5	D4	D3	D2	D1	D0
CALL CODE	1	1	0	0	1	1	0	1

During the second $\overline{INTA}$ pulse the lower address of the appropriate service routine is enabled onto the data bus. When Interval=4 bits A_5-A_7 are programmed, while A_0-A_4 are automatically inserted by the UM8259A. When Interval=8 only A_6 and A_7 are programmed, while A_0-A_5 are automatically inserted.

Content of Second Interrupt Vector Byte

IR	Interval = 4							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	A5	1	1	1	0	0
6	A7	A6	A5	1	1	0	0	0
5	A7	A6	A5	1	0	1	0	0
4	A7	A6	A5	1	0	0	0	0
3	A7	A6	A5	0	1	1	0	0
2	A7	A6	A5	0	1	0	0	0
1	A7	A6	A5	0	0	1	0	0
0	A7	A6	A5	0	0	0	0	0

IR	Interval = 8							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	1	1	1	0	0	0
6	A7	A6	1	1	0	0	0	0
5	A7	A6	1	0	1	0	0	0
4	A7	A6	1	0	0	0	0	0
3	A7	A6	0	1	1	0	0	0
2	A7	A6	0	1	0	0	0	0
1	A7	A6	0	0	1	0	0	0
0	A7	A6	0	0	0	0	0	0

During the third INTA pulse the higher address of the appropriate service routine, which was programmed as byte 2 of the initialization sequence (A_8-A_{15}), is enabled onto the bus.

Content of Third Interrupt Vector Byte

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

iAPX 86, iAPX 88

IAPX 86 mode is similar to MCS-80 mode except that only two interrupt Acknowledge cycles are issued by the processor and no CALL opcode is sent to the processor. The first interrupt acknowledge cycle is similar to that of MCS-80, 85 systems in that the UM8259A uses it to internally freeze the state of the interrupts for priority resolution and as a master it issues the interrupt code on the cascade lines at the end of the INTA pulse. On this first cycle it does not issue any data to the processor and leaves its data bus buffers disabled. On the second interrupt acknowledge cycle in iAPX 86 mode the master (or slave if so programmed) will send a byte of data to the processor with the acknowledged interrupt code composed as follows (note the state of the ADI mode control is ignored and A_5-A_{11} are unused in iAPX 86 mode):

Content of Interrupt Vector Byte for iAPX 86 System Mode

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

Programming the UM8259A

The Um8259A accepts two types of command words generated by the CPU:

1. Initialization Command Words (ICWs): Before normal operation can begin, each UM8259A in the system must be brought to a starting point – by a sequence of 2 to 4 bytes timed by $\overline{WR}$ pulses.
2. Operation Command Words (OCWs): These are the command words which command the UM8259A to operate in various interrupt modes. These modes are:
   a. Fully nested mode
   b. Rotating priority mode
   c. Special mask mode
   d. Polled mode

The OCWs can be written into the UM8259A anytime after initialization.

Initialization Command Words (ICWs)

General

Whenever a command is issued with A0=0 and D4=1, this is interpreted as Initialization Command Word 1 (ICW1). ICW1 starts the initialization sequence during which the

Peripheral IC

following automatically occur.

a. The edge sense circuit is reset, which means that following initialization, an interrupt request (IR) input must make a low-to-high transition to generate an interrupt.
b. The Interrupt Mask Register is cleared.
c. IR7 input is assigned priority 7.
d. Theslave mode address is set to 7.
e. Special Mask Mode is cleared and Status Read is set to IRR.
f. If IC4=0, then all functions selected in ICW4 are set to zero. (Non-Buffered mode*, no Auto-EOI, MCS-80, 85 system).

*Note: Master/Slave in ICW4 is only used in the buffered mode.

Initialization Command Words 1 and 2 (ICW1, ICW2)

A_5-A_{15}: Page starting address of service routines. In an MCS 80/85 system, the 8 request levels will generate CALLs to 8 locations equally spaced in memory. These can be programmed to be spaced at intervals of 4 or 8 memory locations, thus the 8 routines will occupy a page of 32 or 64 bytes, respectively.

The address format is 2 bytes long (A_0-A_{15}). When the routine interval is 4, A_0-A_4 are automatically inserted by the UM8259A. While A_5-A_{15} are programmed externally. When the routine interval is 8, A_0-A_5 are automatically inserted by the UM8259A, while A_6-A_{15} are programmed externally.

The 8-byte interval will maintain compatibility with current software, while the 4-byte interval is best for a compact jump table.

In an iAPX 86 system A_{15}-A_{11} are inserted in the five most significant bits of the vectoring byte and the UM8259A sets the three least significant bits according to the interrupt level. A_{10}-A_5 are ignored and ADI (Address interval) has no effect.

LTIM: If LTIM=1, then the UM8259A will operate in the level interrupt mode. Edge detect logic on the interrupt inputs will be disabled.

ADI: CALL address interval. ADI=1 then interval=4; ADI=0 then interval=8.

SNGL: Single. Means that this is the only UM8259A in the system. If SNGL=1 no ICW3 will be issued.

IC4: If this bit is set – ICW4 has to be read. If ICW4 is not needed, set IC4=0.

Initialization Command Word 3 (ICW3)

This word is read only when there is more than one UM8259A in the system and cascading is used, in which case SNGL=0. It will load the 8-bit slave register. The functions of this register are:

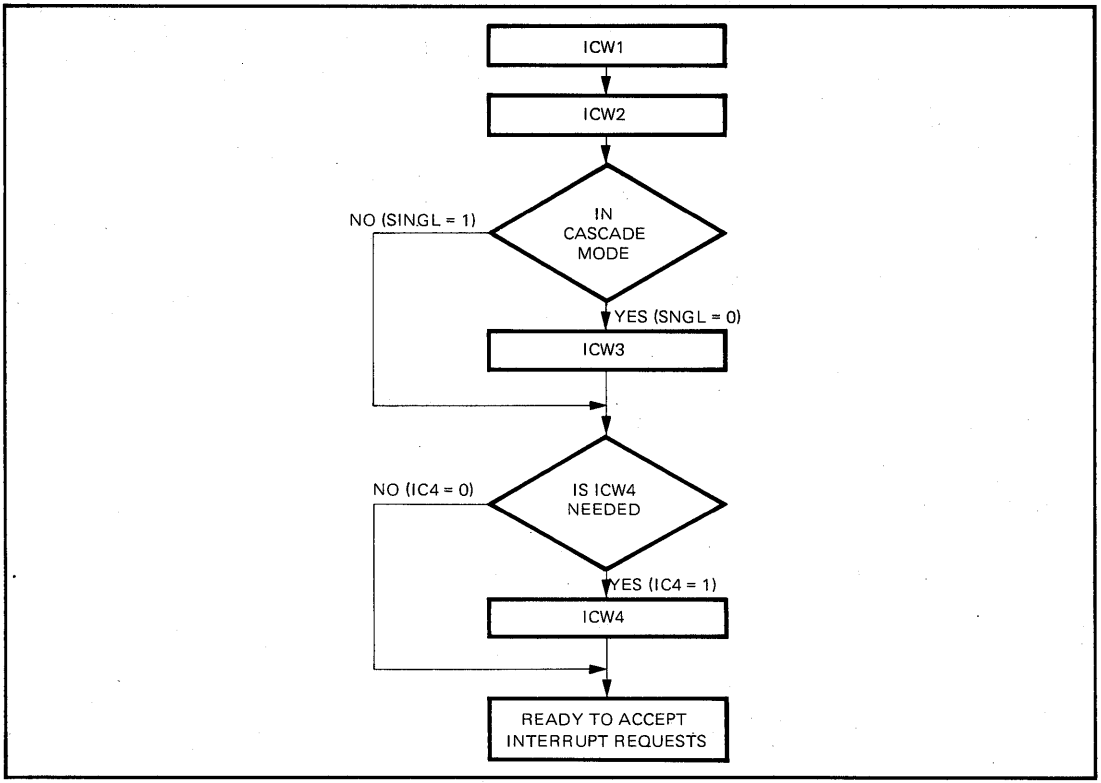
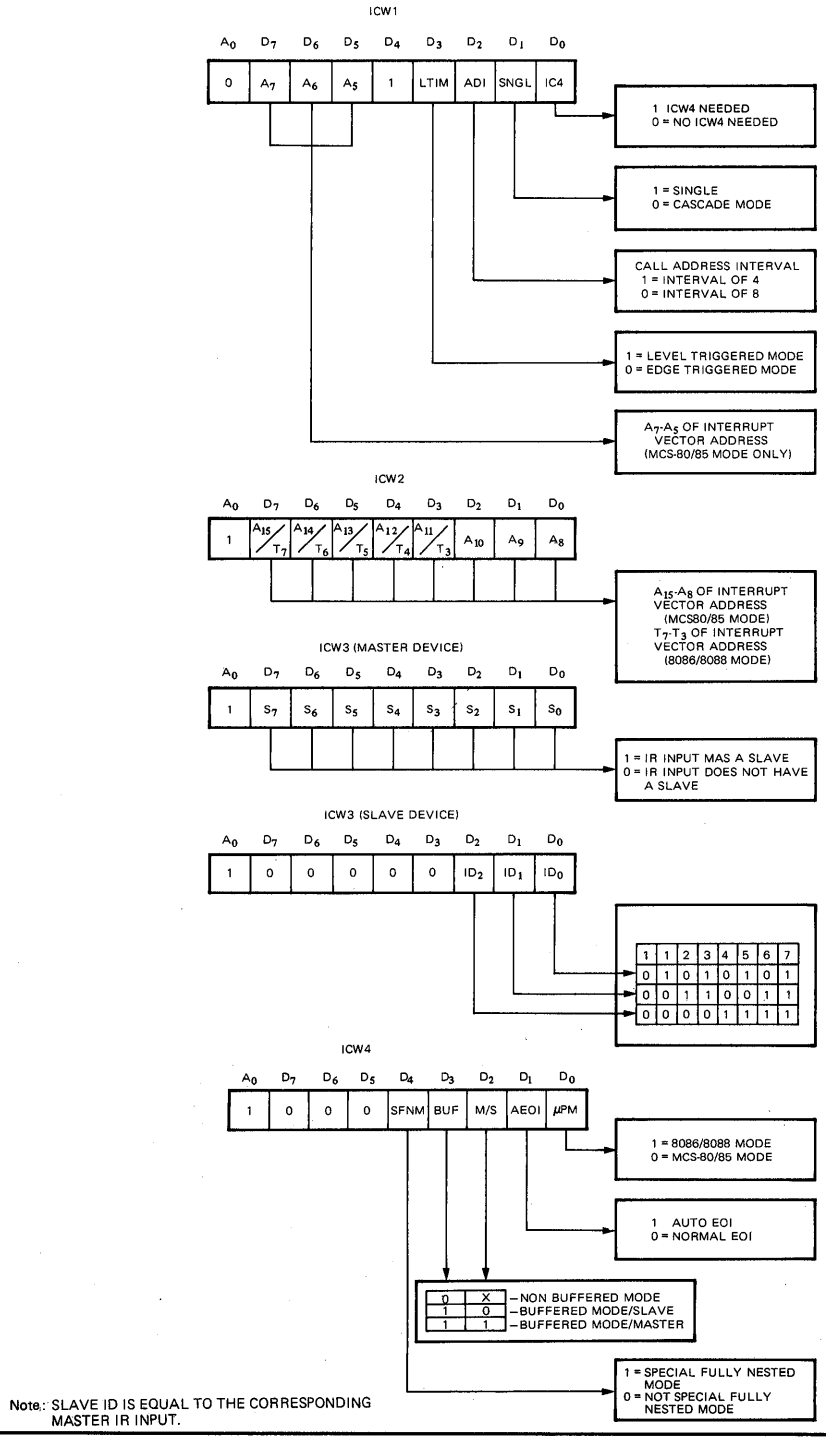


Figure 4. Initialization Sequence



Note: SLAVE ID IS EQUAL TO THE CORRESPONDING MASTER IR INPUT.

Figure 5. Initialization Command Word Format

a. In the master mode (either when SP=1, or in buffered mode when M/S=1 in ICW4) a "1" is set for each slave in the system. The master then will release byte 1 of the call sequence (for MCS-80/85 system) and will enable the-corresponding slave to release bytes 2 and 3 (for iAPX 86 only byte 2) through the cascade lines.

b. In the slave mode (either when $\overline{SP}$=0, or if BUF=1 and M/S=0 in ICW4) bits 2-0 identify the slave. The slave compares its cascade input with these bits and, if they are equal, bytes 2 and 3 of the call sequence (or just byte 2 for iAPX 86 are released by it on the Data Bus.

Initialization Command Word 4 (ICW4)

SFNM: If SFNM=1 the special fully nested mode is programmed.

BUF: If BUF=1 the buffered mode is programmed. In buffered mode $\overline{SP}/\overline{EN}$ becomes an enable output and the master/slave determination is by M/S.

M/S: If buffered mode is selected: M/S=1 means the UM8259A is programmed to be a master, M/S=0 means the UM8259A is programmed to be a slave. If BUF=0, M/S has no function.

AEOI: If AEOI=1 the automatic end of interrupt mode is programmed .

μPM: Microprocessor mode: μPM=0 sets the UM8259A for MCS-80, 85 system operation, μPM=1 sets the UM8259A for iAPX 86 system operation.

Operation Command Words (OCWs)

After the Initialization Command Words (ICWs) are programmed into the UM8259A, the chip is ready to accept interrupt requests at its input lines. However, during the UM8259A operation, a selection of algorithms can command the UM8259A to operate in various modes through the Operation Command Words (OCWs).

				OCW1				
A0	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	M7	M5	M5	M4	M3	M2	M1	M0
				OCW2				
0	R	SL	EOI	0	0	L2	L1	L0
				OCW3				
0	0	ESMM	SMM	0	1	p	RR	RIS

Operation Control Word 1 (OCW1)

OCW1 sets and clears the mask bits in the interrupt Mask Register (IMR). M_7-M_0 represent the eight mask bits. M=1 indicates the channel is masked (inhibited), M=0 indicates the channel is enabled.

Operation Control Word 2 (OCW2)

R, SL, EOI – These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations can be found on the Operation Command Word Format.

L_2, L_1, L_0 – These bits determine the interrupt level acted upon when the SL bit is active.

Operation Control Word 3 (OCW3)

ESMM – Enable Special Mask Mode. When this bit is set to 1 it enables the SMM bit to set or reset the Special Mask Mode. When ESMM=0 the SMM bit becomes a "don't care".

SMM – Special Mask Mode. If ESMM=1 and SMM=1 the UM8259A will enter Special Mask Mode. If ESMM=1 and SMM=0 the UM8259A will revert to normal mask mode. When ESMM=0, SMM has no effect.

Fully Nested Mode

This mode is entered after initialization unless another mode is programmed. The interrupt requests are ordered in priority form 0 through 7 (0 highest). When an interrupt is acknowledged the highest priority request is determined and its vector placed on the bus. Additionally, a bit of the Interrupt Service register (ISO-7) is set. This bit remains set until the microprocessor issues an End of Interrupt (EOI) command immediately before returning from the service routine, or if AEOI (Automatic End of Interrupt) bit is set, until the trailing edge of the last INTA. While the IS bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels will generate an interrupt (which will be acknowledged only if the microprocessor internal interrupt enable flip-flop has been re-enabled through software).

After the initialization sequence, IR0 has the highest priority and IR7 the lowest. Priorities can be changed, as will be explained, in the rotating priority mode.

End of Interrupt (EOI)

The In Service (IS) bit can be reset either automatically following the trailing edge of the last in sequence $\overline{INTA}$ pulse (when AEOI bit in ICW1 is set) or by a command word that must be issued to the UM8259A before returning from a service routine (EOI command). An EOI command must be issued twice if in the Cascade mode, once for the master and once for the corresponding slave.

There are two forms of EOI command: Specific and Non-Specific. When the UM8259A is operated in modes which preserve the fully nested structure, it can determine which IS bit to reset on EOI. When a Non-Specific EOI command is issued the UM8259A will automatically reset the highest IS bit of those that are set, since in the fully nested mode the highest IS level was necessarily the last level acknowledged and service. A non-specific EOI can

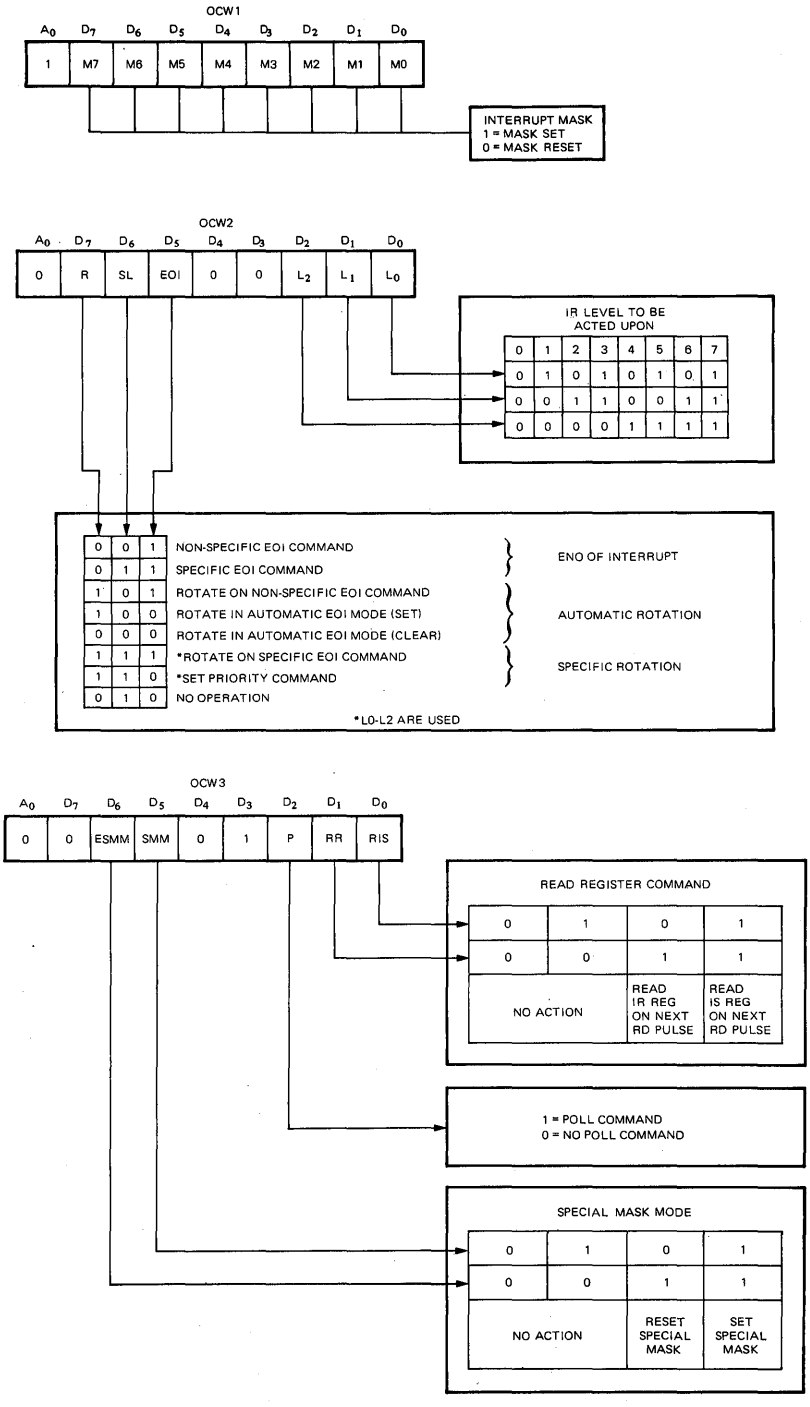


Figure 6. Operation Command Word Format

be issued with OCW2 (EOI=1, SL=0, R=0).

When a mode is used which may disturb the fully nested structure, the UM8259A may no longer be able to determine the last level acknowledged. In this case a Specific End of Interrupt must be issued which includes as part of the command the IS level to be reset. A specific EOI can be issued with OCW2 (EOI=1, SL=1, R=0, and L0-L2 is the binary level of the IS bit to be reset).

It should be noted that an IS bit that is masked by an IMR bit will not be cleared by a non-specific EOI if the UM8259A is in the Special Mask Mode.

Automatic End of Interrupt (AEOI) Mode

If AEOI=1 in ICW4, then the UM8259A will operate in AEOI mode continuously until reprogrammed by ICW4. In this mode the UM8259A will automatically perform a non-specific EOI operation at the trailing edge of the last interrupt acknowledge pulse (third pulse in MCS-80/85, second in iAPX 86). Note that from a system standpoint, this mode should be used only when a nested multilevel interrupt structure is not required within a single UM8259A.

The AEOI mode can only be used in a master UM8259A and not a slave.

Automatic Rotation (Equal Priority Devices)

In some applications there are a number of interrupting devices of equal priority. In this mode a device, after being service, receives the lowest priority, so a device requesting an interrupt will have to wait, in the worst case until each of 7 other devices are serviced at most once. For example, if the priority and "in service" status is:

Before Rotate (IR4 the highest priority requiring service)

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
"IS" Status	0	1	0	1	0	0	0	0

	Lowest Priority							Highest Priority
Priority Status	7	6	5	4	3	2	1	0

After Rotate (IR4 was servided, all other priorities rotated correspondingly)

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0s
"IS" Status	0	1	0	0	0	0	0	0

	Highest Priority							Lowest Priority
Priority Status	2	1	0	7	6	5	4	3

There are two ways to accomplish Automatic Rotation using OCW2, the Rotation on Non-Specific EOI Command (R=1, SL=0, EOI=1) and the Rotate in Automatic EOI Mode which is set by (R=1, SL=0, EOI=0) and cleared by (R=0, SL=0, EOI=0).

Specific Rotation (Specific Priority)

The programmer can change priorities by programming the bottom priority and thus fixing all other priorities; i.e., if IR5 is programmed as the bottom priority device, then IR6 will have the highest one.

The Set Priority command is issued in OCW2 where: R=1, SL=1; L0-L2 is the binary priority level code of the bottom priority device.

Observe that in this mode internal status is updated by software control during OCW2. However, it is independent of the End of Interrupt (EOI) command (also executed by OCW2). Priority changes can be executed during an EOI command by using the Rotate on Specific EOI command in OCW2 (R=1, SL=1, EOI=1 and L0-L2=IR level to receive bottom priority).

Interrupt Masks

Each Interrupt Request input can be masked individually by the Interrupt Mask Register (IMR) programmed through OCW1. Each bit in the IMR masks one interrupt channel if it is set (1). Bit 0 masks IR0, Bit 1 masks IR1 and so forth. Masking an IR channel does not affect the other channels operation.

Special Mask Mode

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

The difficulty here is that if an Interrupt Request is acknowledged and an End of Interrupt command did not reset its IS bit (i.e., while executing a service routine), the UM8259A would have inhibited all lower priority requests with no easy way for the routine to enable them.

That is where the Special Mask Mode comes in. In the special Mask Mode, when a mask bit is set in OCW1, it inhibits further interrupts at that level and enables interrupts from all other levels (lower as well as higher) that are not masked.

Thus, any interrupts may be selectively enabled by loading the mask register.

The special Mask Mode is set by OCW3 where: SSMM=1, SMM=1, and cleared where SSMM=1, SMM=0.

Poll Command

In this mode the INT output is not used or the microprocessor internal Interrupt Enable flip-flop is reset, disabling its interrupt input. Service to devices is achieved by software using a Poll command.

The Poll command is issued by setting P="1" in OCW3. The UM8259A treats the next $\overline{RD}$ pulse to the UM8259A (i.e., $\overline{RD}$=0, $\overline{CS}$=0 as an interrupt acknowledge, sets the appropriate IS bit if there is a request, and reads the priority level. Interrupt is frozen from $\overline{WR}$ to $\overline{RD}$.

The word enabled onto the data bus during $\overline{RD}$ is:

D7	D6	D5	D4	D3	D2	D1	D0
1	–	–	–	–	W2	W1	W0

W0-W2: Binary code of the highest priority level requesting service.

I: Equal to a "1" if there is an interrupt.

This mode is useful if there is a routine command common to several levels so that the $\overline{INTA}$ sequence is not needed (saves ROM space). Another application is to use the poll mode to expand the number of priority levels to more than 64.

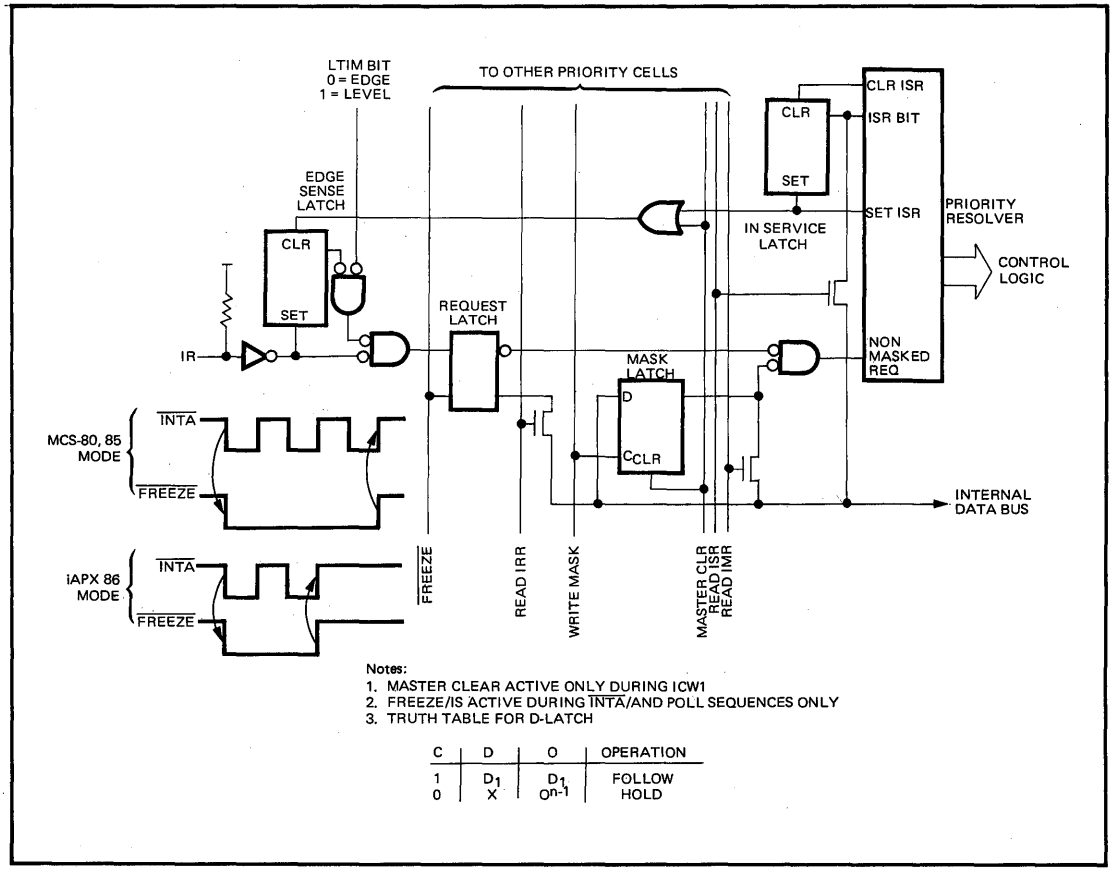
Reading the 8259A Status

The input status of several internal registers can be read to update the user information on the system. The following registers can be read via OCW3 (IRR and ISR or OCW1 [IMR]).

Interrupt Request Register (IRR): 8-bit register which contains the levels requesting an interrupt to be acknowledged. The highest request level is reset from the IRR when an interrupt is acknowledged. (Not affected by IMR.).

In-Service Register (ISR): 8-bit register which contains the priority levels that are being serviced. The ISR is updated when an End of Interrupt Command is issued.

Interrupt Mask Register: 8-bit register which contains the interrupt request lines which are masked.



Notes:
1. MASTER CLEAR ACTIVE ONLY DURING ICW1
2. FREEZE/IS ACTIVE DURING $\overline{INTA}$/AND POLL SEQUENCES ONLY
3. TRUTH TABLE FOR D-LATCH

C	D	O	OPERATION
1	D_1	D_1	FOLLOW
0	X	O^{n-1}	HOLD

Figure 7. Priority Cell–Simplified Logic Diagram

The IRR can be read when, prior to the RD pulse, a Read Register Command is issued with OCW3 (RR=1, RIS=0.).

The ISR can be read when, prior to the RD pulse, a Read Register Command is issued with OCW3 (RR=1, RIS=1).

There is no need to write an OCW3 before every status read operation, as long as the status read corresponds with the previous one; i.e., the UM8259A "remembers" whether the IRR or ISR has been previously selected by the OCW3. This is not true when poll is used.

After initialization the UM8259A is set to IRR.

For reading the IMR, no OCW3 is needed. The output data bus will contain the IMR whenever $\overline{RD}$ is active and AO=1 (OCW1).

Polling overrides status read when P=1, RR=1 in OCW3.

Edge and Level Triggered Modes

This mode is programmed using bit 3 in ICW1.

If LTIM='0', an interrupt request will be recognized by a low to high transition on an IR input. The IR input can remain high without generating another interrupt.

If LTIM='1', an interrupt request will be recognized by a 'high' level on IR Input, and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued or the CPU interrupt is enabled to prevent a second interrupt from occurring.

The priority cell diagram shows a conceptual circuit of the level sensitive and edge sensitive input circuitry of the UM8259A. Be sure to note that the request latch is a transparent D type latch.

In both the edge and level triggered modes the IR inputs must remain high until after the falling edge of the first INTA. If the IR input goes low before this time a DEFAULT IR7 will occur when the CPU acknowledges the interrupt. This can be a useful safeguard for detecting interrupts caused by spurious noise glitches on the IR inputs. To implement this feature the IR7 routine is used for "clean up" simply executing a return instruction, thus ignoring the interrupt. If IR7 is needed for other purposes a default IR7 can still be detected by reading the ISR. A normal IR7 interrupt will set the corresponding ISR bit, a default IR7 won't. If a default IR7 routine occurs during a normal IR7 routine, however, the ISR will remain set. In this case it is necessary to keep track of whether or not the IR7 routine was previously entered. If another IR7 occurs it is a default.

The Special Fully Nested Mode

This mode will be used in the case of a big system where cascading is used, and the priority has to be conserved within each slave. In this case the fully nested mode will be programmed to the master (using ICW4). This mode is similar to the normal nested mode with the following exceptions:

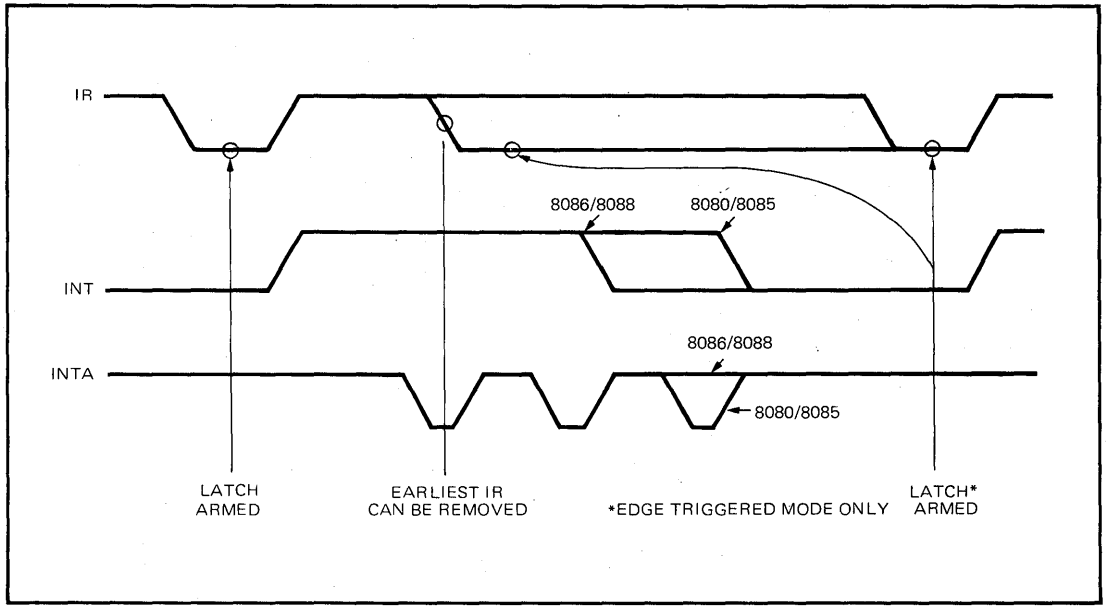


Figure 8. IR Triggering Timing Requirements

a. When an interrupt request from a certain slave is in service this slave is not locked out from the master's priority logic and further interrupt requests from higher priority IR's within the slave will be recognized by the master and will initiate interrupts to the processor. (In the normal nested mode a slave is masked out when its request is in service and no higher requests from the sameslave can be serviced.)

b. When exiting the Interrupt Service routine the software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a non-specific End of Interrupt (EOI) command to the slave and then reading its In-Service register and checking for zero. If it is empty, a non-specific EOI can be sent to the master too. If not, no EOI should be sent.

Buffered Mode

When the UM8259A is used in a large system where bus driving buffers are required on the data bus and the cascading mode is used, there exists the problem of enabling buffers.

The buffered mode will structure the UM8259A to send an enable signal on $\overline{SP}/\overline{EN}$ to enable the buffers. In this mode, whenever the UM8259A's data bus outputs are enabled, the $\overline{SP}/\overline{EN}$ output becomes active.

This modification forces the use of software programming to determine whether the UM8259A is a master or a slave. Bit 3 in ICW4 programs the buffered mode, and bit 2 in ICW4 determines whether it is a master or a slave.

Cascade Mode

The UM8259A can be easily interconnected in a system of one master with up to eight slaves to handle up to 64 priority levels.

The master controls the slaves through the 3 line cascade bus. The cascade bus acts like chip selects to the slaves during the $\overline{INTA}$ sequence.

In a cascade configuration, the slave interrupt outputs are connected to the master interrupt request inputs. When a slave request line is activated and afterwards acknowledged, the master will enable the corresponding slave to release the device routine address during bytes 2 and 3 of INTA. (Byte 2 only for 8086/8088).

The cascade bus lines are normally low and will contain the slave address code from the trailing edge of the first INTA pulse to the trailing edge of the third pulse. Each UM8259A in the system must follow a separate initialization sequence and can be programmed to work in a different mode. An EOI command must be issued twice: once for the master and once for the corresponding slave. An address decoder is required to activate the Chip Select (CS) input of each UM8259A.

The cascade lines of the Master UM8259A are activated only for slave inputs, non slave inputs leave the cascade line inactive (low).

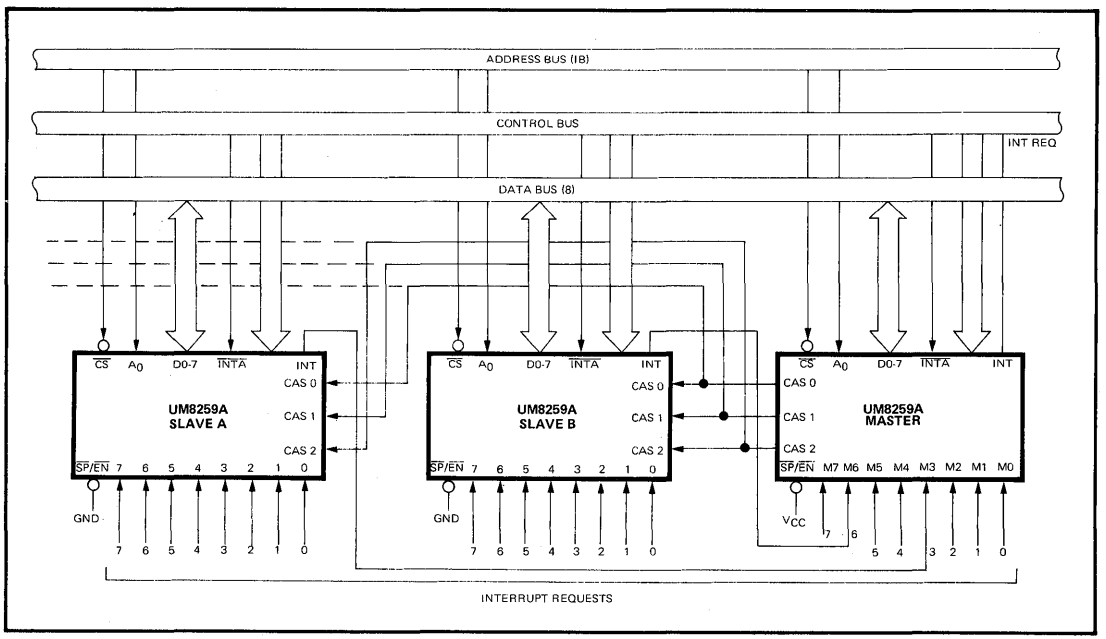


Figure 9. Cascading the UM8259A

UM82C6818

Real Time Clock Plus RAM (RTC)

ADVANCED PRODUCT DESCRIPTION

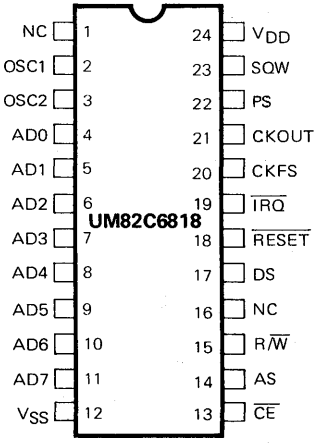
Features

- Internal time base and oscillator
- Counts seconds, minutes, and hours of the day
- Counts days of the week, date, month, and year
- 3V to 6V operation
- Time base input options: 4.194304 MHz, 1.048576 MHz, or 32.768 kHz
- Time base oscillator for parallel resonant crystals
- Binary or BCD representation of time, calendar, and alarm
- 12 or 24-hour clock with AM and PM in 12-hour mode
- automatic end of month recognition
- automatic leap year compensation
- Multiplexed bus for pin efficiency
- Interfaced with software as 64 RAM locations
  - 14 bytes of clock and control registers
  - 50 bytes of general purpose RAM
- Status bit indicates data integrity
- Bus compatible interrupt signals ($\overline{IRQ}$)
- Three interrupts are separately software maskable and testable
  - Time-of-day alarm, once-per-second to once-per-day
  - Periodic rates from 30.5 μs to 500 ms
  - End-of-clock update cycle
- Programmable square-wave output signal
- Clock output may be used as microprocessor clock input
  - At time base frequency ÷1 or ÷4

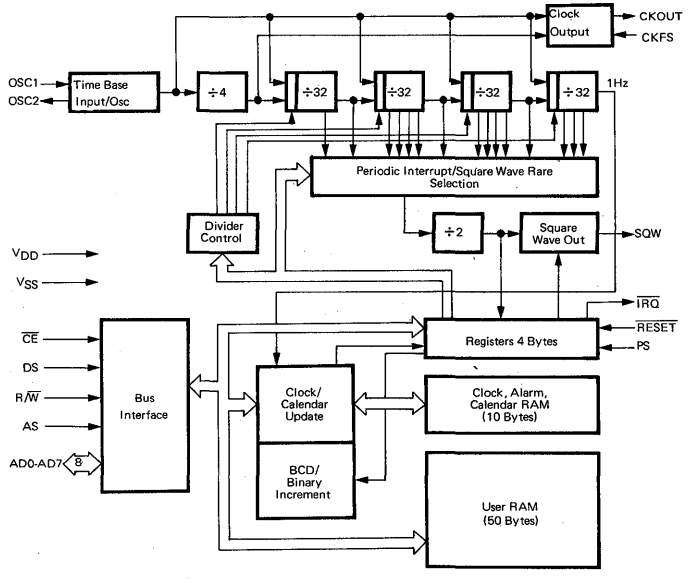
General Description

The UM82C6818 Real-Time Clock plus RAM is fabricated in high performance CMOS process to interface with 1MHz processor buses. It combines three unique features: a complete time-of-day clock with alarm and one hundred year calendar, a programmable periodic interrupt and square-wave generator, and 50 bytes of static RAM.

Pin Configuration



Block Diagram



UM82C8167A

ADVANCED PRODUCT DESCRIPTION

Real Time Clock (RTC)

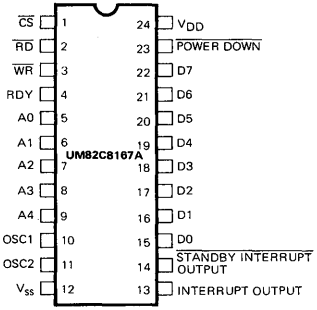
Feature

- Microprocessor compatible (8-bit data bus)
- Milliseconds through month counters
- 56 bits of RAM with comparator to compare the real time counter to the RAM data
- 2 INTERRUPT OUTPUTS with 8 possible interrupt signals
- Single +5V power supply
- POWER DOWN input that disables all inputs and outputs except for one of the interrupts
- Status bit to indicate rollover during a read
- 32,768 Hz crystal oscillator
- Four-year calendar (no leap year)
- 24-hour clock
- 24 pin dual-in-line package

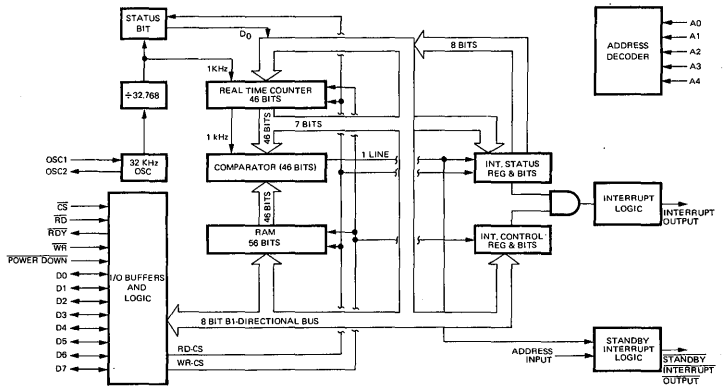
General Description

The UM82C8167A is a Si-gate CMOS LSI used as a real time clock in micro system. This product includes an addressable real time counter, 56 bits of static RAM and two interrupt outputs. User can disable the chip from the rest of the system for standby low power operation by using of a POWER DOWN input. With an on chip oscillation circuit, it can generate the 32,768 Hz time base.

Pin Configuration



Block Diagram



Peripheral IC

UM82450 / UM8250

ADVANCED PRODUCT DESCRIPTION

Asynchronous Communication Element (ACE)

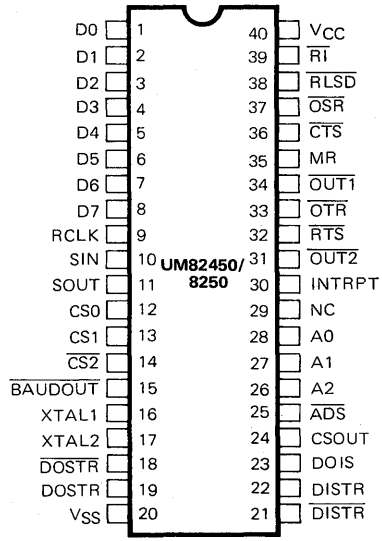
Feature

- Adds or deletes standard asynchronous communication bits (Start, Stop, and Parity) to or from serial data stream
- Full double buffering eliminates need for precise synchronization
- Independently controlled transmit, receive, line status, and data set interrupts
- Programmable baud rate generator allows division of any input clock by 1 to ($2^{16} - 1$) and generates the internal 16x clock
- Independent receiver clock input
- Modem control functions (CTS, RTS, DSR, DTR, RI, and carrier detect)
- Single +5 volt power supply
- Fully programmable serial-interface characteristics
  - 5-, 6-, 7-, or 8-Bit characters
  - Even, Odd, or No-Parity bit generation and detection
  - 1-, 1½-, or 2-Stop bit generation
  - Baud rate generation (DC to 56K baud)
- False start bit detection
- Complete status reporting capabilities
- Easily interfaces to most popular microprocessors
- Line break generation and detection
- Internal diagnostic capabilities
  - Loopback controls for communications link fault isolation
  - Break, parity, overrun, framing error simulation
- Full prioritized interrupt system controls

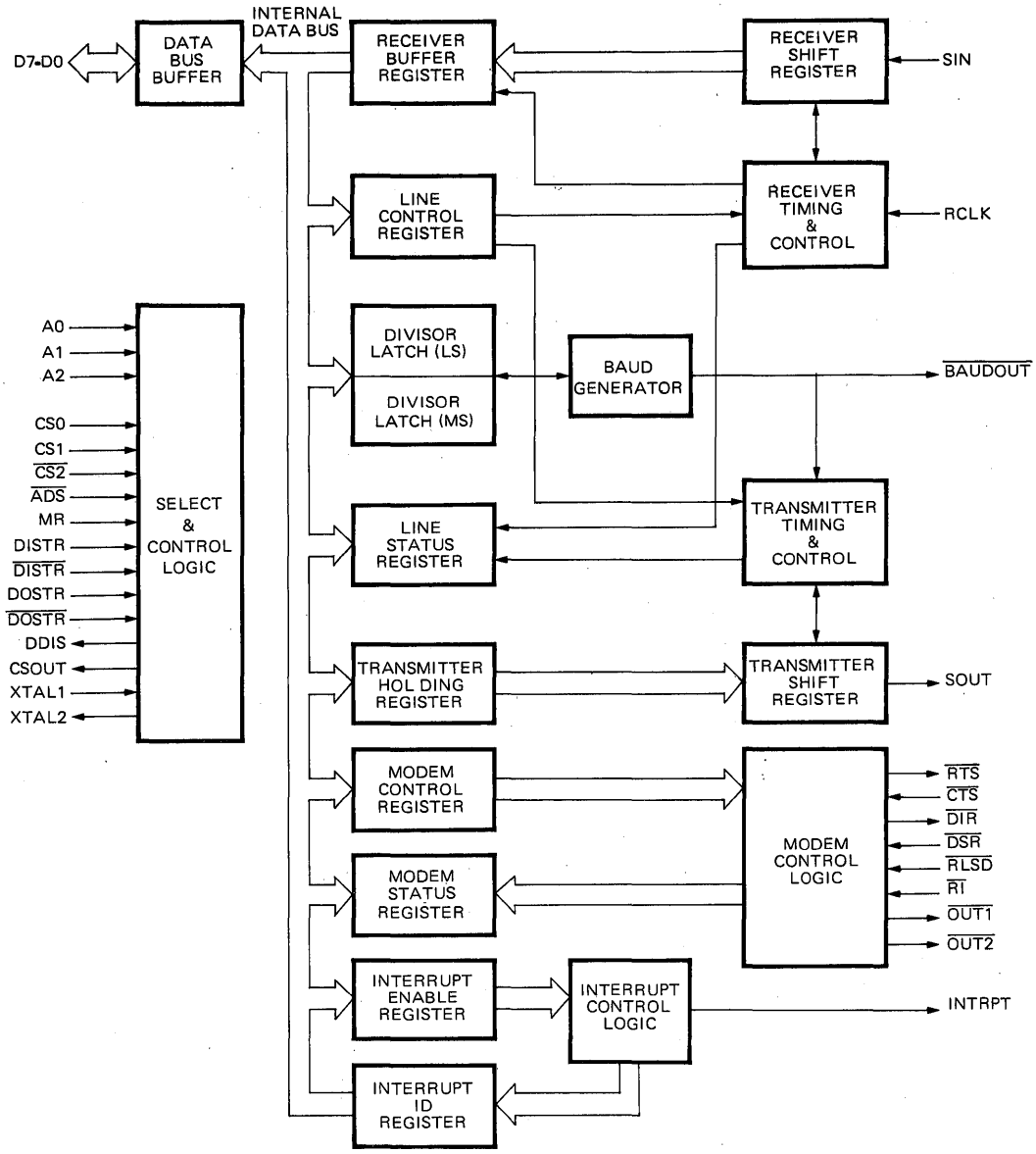
General Description

UM82450 and UM8250 are programmable Asynchronous Communication Element (ACE) chips fabricated with Si-Gate NMOS process. The UM82450 is an improved specification version of the UM8250. These two products perform serial-to-parallel conversion on data characters received from the CPU. The CPU can read the complete status of the ACE at any time during the functional operation. They also includes a programmable baud rate generator that is capable of dividing the timing reference clock input by divisors of 1 to ($2^{16} - 1$), and producing a 16x clock for driving the internal transmitter logic.

Pin Configuration



Block Diagram



Peripheral IC

General Information

GUIDE TO MOS HANDLING

We at UMC are continually looking for more effective ways to provide protection for MOS devices. Present configurations of protective devices are the result of years of research and review of field problems.

Even though the oxide breakdown may be far beyond the voltage levels encountered in normal operation, excessive voltages may cause permanent damage. We recognize that it is not 100 percent effective despite our evolving the best designed protective device possible.

A large number of failed returns have been due to misapplication of biases. In particular, forward bias conditions cause excessive current through the protective devices, which in turn will vaporize metal lines to the inputs. Careful inspection of the device data sheets and proper pin designation should help reduce this failure mode.

Gate ruptures caused by static discharge have also accounted for a large percentage of device failures in customers' manufacturing areas. Precautions should be taken to minimize the possibility of static charges which occur during handling and assembly of MOS circuits.

The following guidelines for handling MOS are offered to assist our customers in reducing the hazards which may be detrimental to MOS circuits. Precautions listed herein are used at UMC.

A. Cover all benches used for assembly or test of MOS circuits with conductive sheets. Warning: Never expose an operator directly to a hard electrical ground. For safety reasons, the operator must have a resistace of at least 100K Ohms between himself and hard electrical ground.

B. Have grounding plates on door and/or floor of all entrances to work areas. This must be contacted by people entering the area.

C. Wear conductive straps inside and outside of employees' shoes so that body charges are grounded when entering work area.

D. Wear Anti-static neutralized smocks to eliminate the possibility of static charges being generated by friction of normal wear. The two types available are Dupont anti-static nylon and Dupont neutralized 65 percent polyester/35 percent cotton.

E. Wear cotton gloves while handling parts. Nylon gloves and rubber finger cots are not allowed.

F. To help reduce generation of static voltages, humidity is controlled at a minimum of 35 percent.

G. Transport all parts in conductive trays. Do not use plastic containers. Store axial leaded parts in conductive foam, e.g. Velofoam #7611.

H. All equipment used in the assembly area must be thoroughly grounded. Attention should be given to equipment that may be inductively coupled and generate stray voltages. Soldering irons must have grounded tips. Grounding must also be provided for solder posts, reflow soldering equipment, etc.

I. It is advisable to place a grounding clip across the finger of the board to ground all leads and line on the board during assembly of ICs to printed circuit boards.

J. Use of carpets is discouraged in work areas, but in other areas, carpets may be treated with anti-static solution to reduce static generation.

K. Handle MOS parts on conductive surfaces and the handler must touch the conductive surface first before touching the parts.

L. Furthermore, no power should be applied to the socket or board when the MOS device is being inserted. This permits any static charge accumulated on the MOS device to be safely removed before power is applied.

M. Do not handle MOS leads by their leads unless absolutely necessary. Handle MOS devices by their packages as much as possible.

N. In general, materials prone to static charge accumulation should not come in contact with MOS devices.

Observe these precautions even when an MOS device is suspected of being defective. The real cause of failure cannot be accurately determined if the device is damaged because of static charge build-up.

IMPORTANT REMINDER: EVEN THE MOST ELABORATE PHYSICAL PREVENTION TECHNIQUES WILL NOT ELIMINATE DEVICE FAILURE IF PERSONNEL ARE NOT FULLY TRAINED IN PROPER HANDLING OF MOS DEVICES.

For further information, please contact Quality Assurance/ Reliability Department.

United Microelectronics Corp.
No. 3 Industrial East Third Road
Science-Based Industrial Park
Hsinchu City, Taiwan Republic of China

UMC

QUALITY/ RELIABILITY

Quality Assurance Operations:

It is the policy of UMC to design, manufacture, and deliver products that not only meet our specified standards, but also satisfy our customer standards. To this end, Quality Assurance at UMC has the authority to exercise control of quality over every phase of the design and manufacturing process.

Each step in the production process has clear lines of responsibility allowing each employee to identify his task in relation to the overall quality program. Customer feedback is an important phase in the Quality Assurance System: it serves as a barometer of our progress and makes us strive to provide products with meet our customers' requirements and needs.

Reliability Program:

The key to establishing a new product, process or package, or to changing an existing one, is meeting the regid qualification requirements. Qualification must be run and approved by the appropriate reliability department before any revenue shipment may be made. The reliability goals which have been set during the concept stage must be demonstrated by the qualification. Controlling product quality and reliability is a complex task requiring a high degree of integration, organizational involvement and use of specialized disciplines.

Design control through part selection and application, design rules, circuit analysis, derating requirements and environmental and reliability qualification testing.

Procured material quality through a rigorous supplier selection, qualification and monitoring process. Our computerized control system automatically assures procurement only from selected and approved sources. The right for any supplier to be on the approved list must be earned!

Product quality level monitoring and control through our automated reporting and analysis systems, and improvement through a corrective action system including impositions of extensive product failure free burn-in requirements. But the final measure of outgoing quality is our continuous product sampling program, where a significant percentage of finished products is subjected to a "customer audit". Only products which meet the stipulated qulity levels may ship.

Reliability qualification testing procedure shall be in accordance with Table 1, 2 and 3.

Table 1. Die Related Qualification Procedure

Test	Mil-Std-883C		UMC Spec.	Conditions	Industrial Grade	
	Method	Cond.			Ceramic PKG	Plastic PKG
Subgroup 1 A. Operating Life	1005 1015	—	24-205-01	T_A = 125°C	LTPD 5% 1000 HRS 3 LOTS	LTPD 7% 1000 HRS 3 LOTS
B. Bias Life	1005 1015	—	24-205-01	T_A = 125°C	LTPD 5% 1000 HRS 3 LOTS	LTPD 7% 1000 HRS 3 LOTS
Subgroup 2 A. Temperature Cycling	1010	C	24-210-01	-65°C-25°C-150°C 10Min. 5Max. 10Min. 200 Cycles	LTPD 15% 1 LOT	LTPD 15% 1 LOT
B. Storage Life	1008	—	24-208-01	T_A = 150°C	LTPD 5% 1000 HRS 1 LOT	LTPD 7% 1000 HRS 1 LOT
Subgroup 3 ESD	3015	—	24-415-01	T_A = 25°C	LTPD 15% 1 LOT	LTPD 15% 1 LOT

Table 2. Package Related Qualification Procedure

Test	Mil-Std-883C		UMC Spec.	Conditions	Industrial Grade	
	Method	Cond.			Ceramic PKG	Plastic PKG
Subgroup 1 Physical Dimension	2016	–	24-316-01	–	3 Derices Accept 0	3 Derices Accept 0
Subgroup 2 Lead Fatigue	2004	B2	24-304-01	6 Leads Each Beut Through 3 Cycles with 8 oz Force	LTPD 15% Accept 0	LTPD 15% Accept 0
Subgroup 3 A. Thermal Shock	1011	C	24-211-01	-65° to 150°C 5Min. 5Min.	LTPD 15% 100 Cycles 3 Lots	LTPD 15% 100 Cycles 3 Lots
B. Moisture Resistance	1004	–	24-204-01	85°C/85% R.H. with Bias	LTPD 5% 1000HRS 1 Lot	LTPD 7% 1000HRS 1 Lot
C. Pressure Cooker	–	–	24-204-02	121°C 15 PSIG 100% R.H.	N/A	LTPD 15% 216HRS 3 Lots
Subgroup 4 Salt Atmosphere	1009	A	24-209-01	35°C 5% NACL 24HRS	LTPD 15% 1 Lot	LTPD 15% 1 Lot
Subgroup 5 A. Seal Fine, Gross	1014	–	24-214-01	As Applicable	LTPD 15% Accept 0	N/A
B. Constant Acceleration	2001	E	24-301-01	Plane Y1 Only 20,000 G (196,000 M/Sec2)	LTPD 15%	N/A
Subgroup 6 Bond Strength	2011	C (or) D	24-311-01	–	LTPD 10%	LTPD 10%

Table 3. Lot Related Qualification Procedure

Test	Mil-Std-883C		UMC Spec.	Conditions	Industrial Grade	
	Method	Cond.			Ceramic PKG	Plastic PKG
Subgroup 1 Physical Dimensions	2016	–	24-316-01	–	3 Devices Accept 0	3 Devices Accept 0
Subgroup 2 A. Resistance to Solvents (Marking Durability)	2015	–	24-315-01	Per Specification	5 Devices Accept 0 1 Lot	5 Devices Accept 0 1 Lot
B. Internal Visual and Mechanical	2014	–	24-314-01	Failure Criteria From Design and Construction Requirements	2 Devices Accept 0	N/A
C. Bond Strength Thermocompression Ultrasonic Wedge	2011	C (or) D	24-311-01	–	LTPD 10% Accept 0	LTPD 10% Accept 0
Subgroup 3 Solderability	2003	–	24-303-01	Soldering Temperature 245°C+(-)5°C	LTPD 15% Accept 0 3 Lots	LTPD 15% Accept 0 3 Lots

Quality Conformance Inspection:

After initial product process evaluations are successfully completed, regular testing of volume production is performed on a 100% basis so that test specifications are met in all respects. Additionally, production lots are sampled and life and stress tested periodically.

Date from reliability tests is made avaliable to customers on request. This includes access to long term life and reliability histories.

Quality conformace inspection shall be in accordance with Table 4. Inspection lots failing to meet quality conformance inspection for a given product assurance level shall be rejected.

Table 4. Quality Conformance Inspection

Test	Mil-Std-883C		UMC Spec.	Conditions	Industrial Grade	
	Method	Cond.			Ceramic PKG	Plastic PKG
1. Die Inspection	2010	B	24-310-01	Production Sort	100%	100%
				Q. C. Audit	AQL 0.65%	AQL 0.65%
2. Wire Pull	2011	C(or)D	24-311-01	Q. C. Audit	LTPD 10%	LTPD 10%
3. Stab Bake Screen	1008	C	24-208-01	48 HRS 150°C	100%	100%
4. Temp. Cycle Screen	1010	C	24-210-01	10 Cycles	As Required	As Requered
5. Pressure Cooker	—	—	24-204-03	121°C 15 PSIG 100% R.H.	N/A	LTPD 15% 216HRS
6. Fine Leak	1014	A	24-214-01	—	LTPD 7%	N/A
7. Gross Leak	1014	C	24-214-02	—	LTPD 7%	N/A
8. Const Acceler	2001	E	24-301-01	Y1 Only	LTPD 7%	N/A
9. Electrical Test	—	—	Per Test Procedure Functional and D. C. Parametric	Production Sort	100%	100%
				Q. C. Audit	AQL 0.25%	AQL 0.25%
10. Sampling Burn-in	1015	—	24-215-01	125°C 48 Hrs	LTPD 5% by Lot	LTPD 7% by Lot
11. Delectrical Test (Post Burn-in)	—	—	Per Test Procedure Functional and D. C. Parametric	Production Sort	100%	100%
				Q. C. Audit	AQL 0.25%	AQL 0.25%
12. Electrical Test (Temp. Extremes)	—	—	Per Test Procedure Functional and D. C. Parametric	Production Sort	100%	100%
				Q. C. Audit	AQL 0.25%	AQL 0.25%
13. Ext. Visual/ Marking	2009	—	24-309-01	Q. C. Audit	AQL 0.65%	AQL 0.65%
14. Solderability	2003	—	24-303-01	Q. C. Audit	LTPD 15%	LTPD 15%
15. Operating Life (or) HTRB	1005 1015	— —	24-205-01 24-205-02	125°C 1000 Hrs	LTPD 5%	LTPD 7%
16. Burn-in	1015	—	24-215-01	125°C 48 Hrs	As Required	As Required

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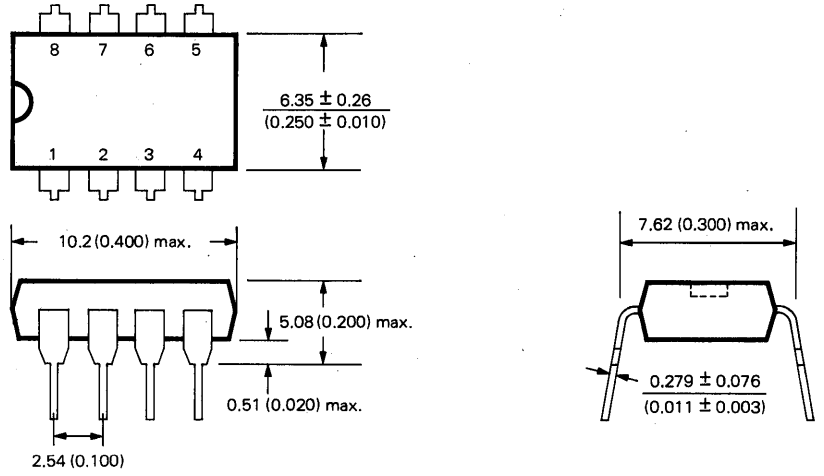
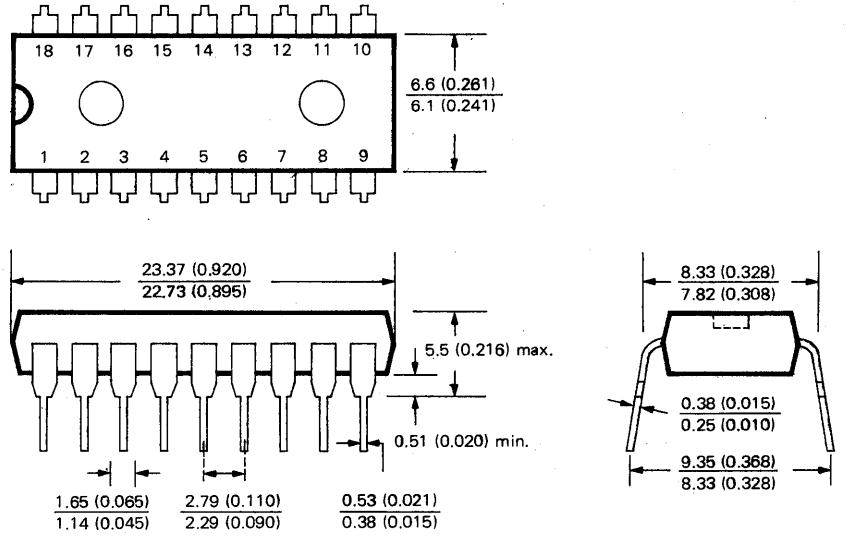
Plastic DIP
8 Lead



Plastic DIP
18 Lead



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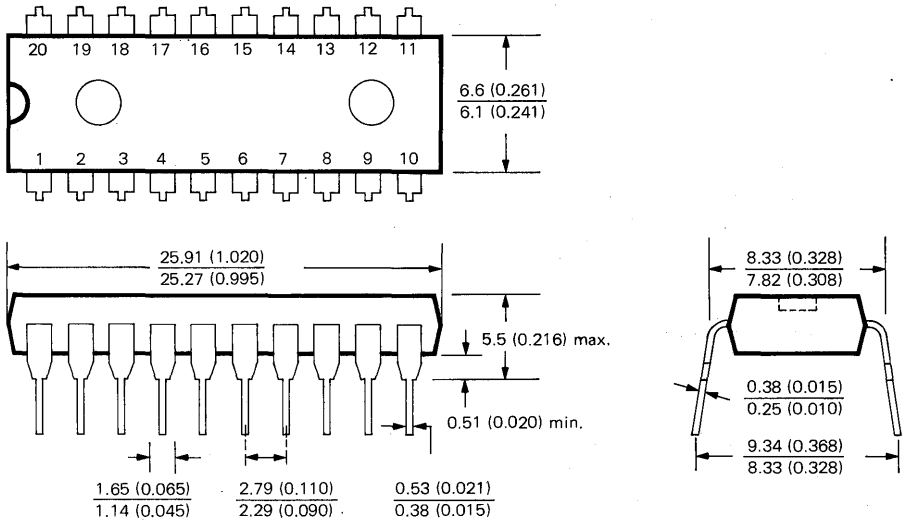
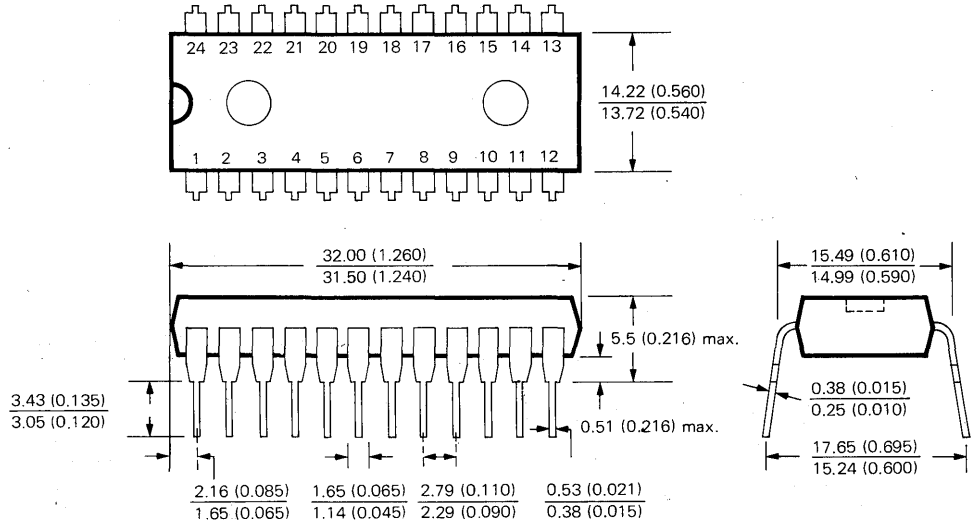
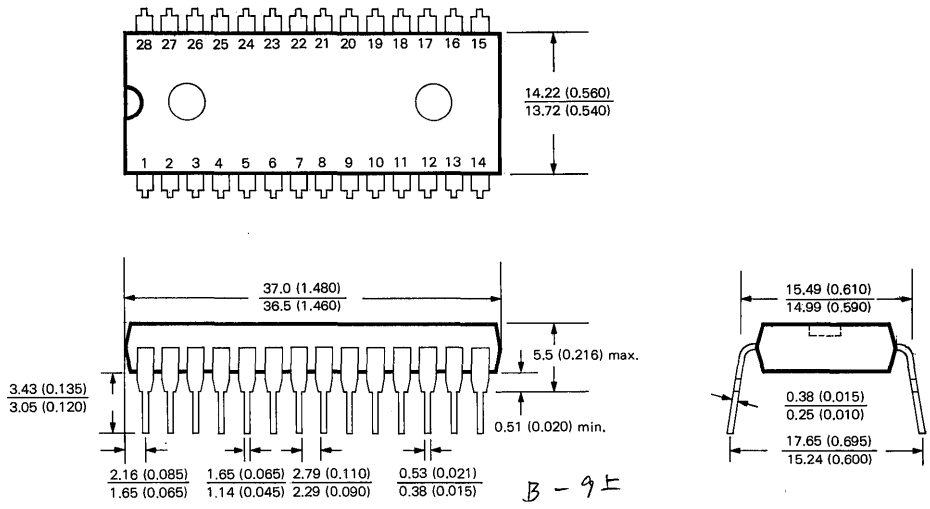
20 Lead



Plastic DIP
24 Lead



Plastic DIP
28 Lead



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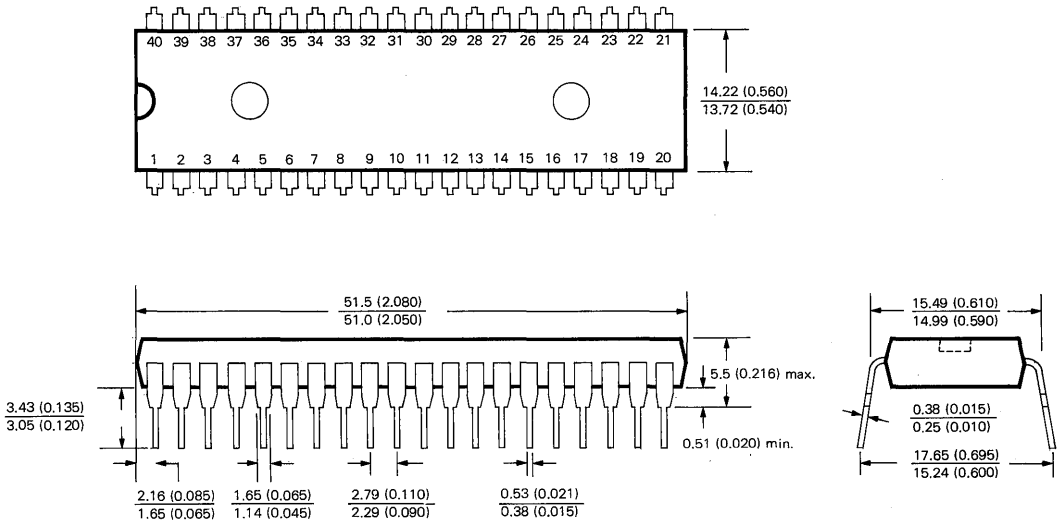
Plastic DIP
40 Lead



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