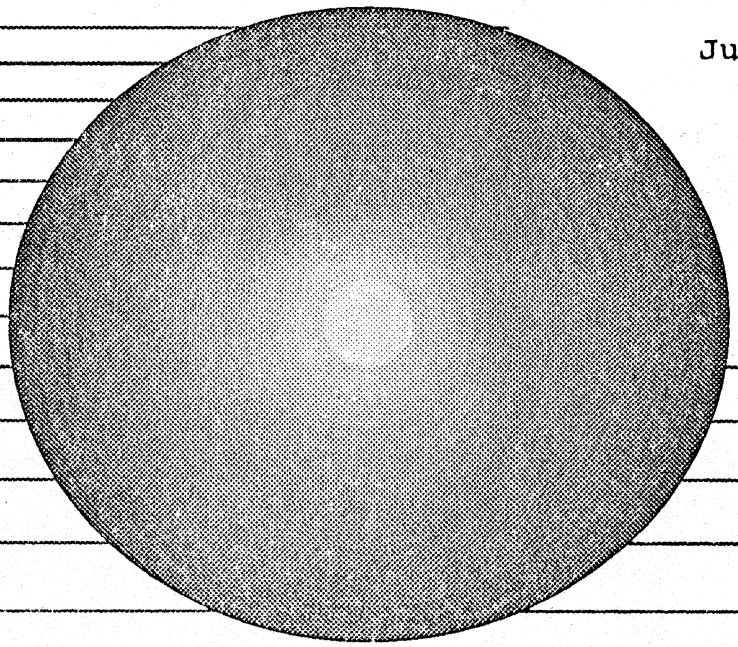
ULTRAVIEW

VBAT

VME Bus Anomaly Trigger

User's Manual

June 1988



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1. INTRODUCTION

The VME Bus Anomaly Trigger (VBAT) is a massively parallel trigger board which automatically recognizes violations of the VMEbus specification in real-time.

The VME Bus Anomaly Trigger (VBAT) board is simply plugged into a slot in any VME computer system, where it automatically monitors all bus traffic and continuously and concurrently screens for a broad range of common timing violations of the VMEbus protocols. Each violation illuminates an LED and generates a fast trigger output within 20 to 80 nanoseconds, giving the engineer a direct lead to the problem. This broad-coverage trigger can then trigger a conventional logic analyzer for immediate viewing of the problem.

The VBAT aids designers and integrators of VME boards and systems by finding serious latent non-compliances in new products, as well as violations that cause all-too-common "incompatibilities" between VME boards from diverse vendors.

FINDS DESIGN ERRORS BY WATCHING EVERY BUS CYCLE IN A MACHINE DURING ACTUAL OPERATION

The VBAT's 104 asynchronous rule-based trigger elements continuously and simultaneously screen 98 VMEbus lines, to detect 28 classes of VMEbus timing violations. It detects any data, address and strobe lines that are not stable during the required intervals as well as strobes that are shorter than allowed or have improper timing relationships with other signals. Finally, by recognizing timing edges that are out-of-sequence, the VBAT finds violations of the important VMEbus arbitration, data transfer and interrupt protocols.

The VBAT can be used as a partial "non-compliance detector," as it uncovers design, manufacturing and field-failure-induced flaws in portions of the bus interface circuitry of both VME masters and slaves, as well as a wide variety of hardware problems, originating in other parts of a VME board, that indirectly cause illegal bus activity. It does this by watching the boards in question during real-world use in the actual system configuration of concern.

A VBAT installed in a malfunctioning system can, for example, help determine why a customer is having trouble integrating a particular manufacturer's board into a foreign system, or why a another vendor's board doesn't function properly in this manufacturer's system.

DIFFERENT FROM A LOGIC ANALYZER OR "BUS MONITOR" BOARD

The most difficult part of debugging solely with a logic analyzer or conventional "bus monitor" board is determining what to trigger on. Often the symptom of failure gives no clue as to its cause. The VBAT's 104 parallel triggers continuously comb the bus for illegal activity, and can often establish an immediate trigger on extremely obscure bugs which might otherwise require days to devise a suitable triggering strategy for a conventional logic analyzer. The VBAT is even fast enough to trigger some oscilloscopes (containing delay lines) on repetitive violations.

The VBAT's capabilities are almost completely different than those of existing logic analyzer and bus monitor boards. Its 104 concurrently active trigger elements give nearly two orders of magnitude more coverage than the one or two simple OR'ed trigger conditions of a conventional logic analyzer. It is through such sheer "brute force" fault coverage that the VBAT's automatic triggering becomes practical for debugging. Also, it's asynchronous triggers finds faults of much shorter duration than are detectable with a logic analyzer's trigger circuitry. Finally, the VBAT's edge-sequence-rule-based triggering recognizes events that cannot be directly detected using logic analyzers. For example, the VBAT automatically recognizes "instability", (i.e.. changes on a line) on all address and data lines at once, without the need to be told the correct state of these lines beforehand. This is essential for concurrently screening for all address and data stability violations in all VMEbus cycles. This capability further enables the VBAT to detect extraneous transitions on strobe lines due to metastability and bus ringing and noise.

The VBAT is passive, and therefore does not alter, in any way, the operation of the VME bus based system. The VBAT merely watches bus activity, and does not drive any lines.

2. FEATURES

* Concurrently screens 98 lines for 28 classes of violations

* Finds serious latent non-compliances in new VME boards.

* Ends finger-pointing by isolating the true cause(s) of "incompatibilities" between boards from different vendors.

* Triggers on many deep bugs in VME boards that are indirectly visible at the bus, WITHOUT the need to devise a trigger strategy.

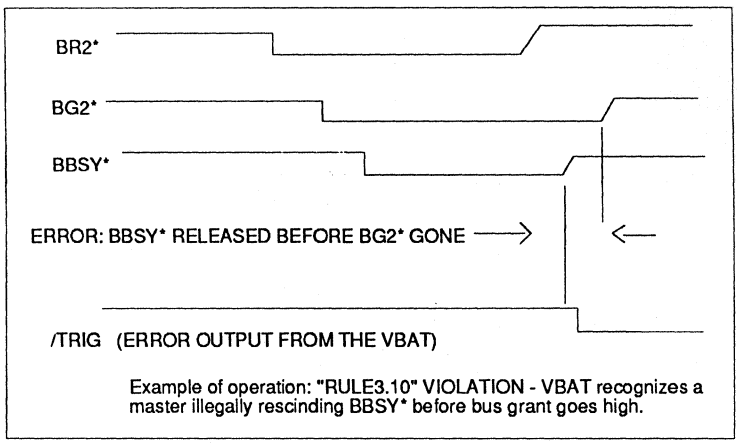
* Fully automatic. 104 preset triggers eliminate the need to specify trigger words or attach probes. Just plug it in.

* Asynchronous edge-sequence triggers isolate events too short or complex to reasonably trigger conventional analyzers.

* Detects complex arbitration, interrupt and data transfer problems.

* 37 individual LED's and trigger outputs.

* Excellent field tool. May be sent rapidly to troubled customers.



Example of operation: "RULE3.10" VIOLATION - VBAT recognizes a master illegally rescinding BBSY* before bus grant goes high.

* Detects extra transitions on strobe lines caused by metastability or bus ringing, cross-talk and ground bounce.

* Screens ALL types and sizes of VMEbus data transfer cycles.

* Real-world use reveals that a large number of VME systems have violations, most of which are simple to rectify.

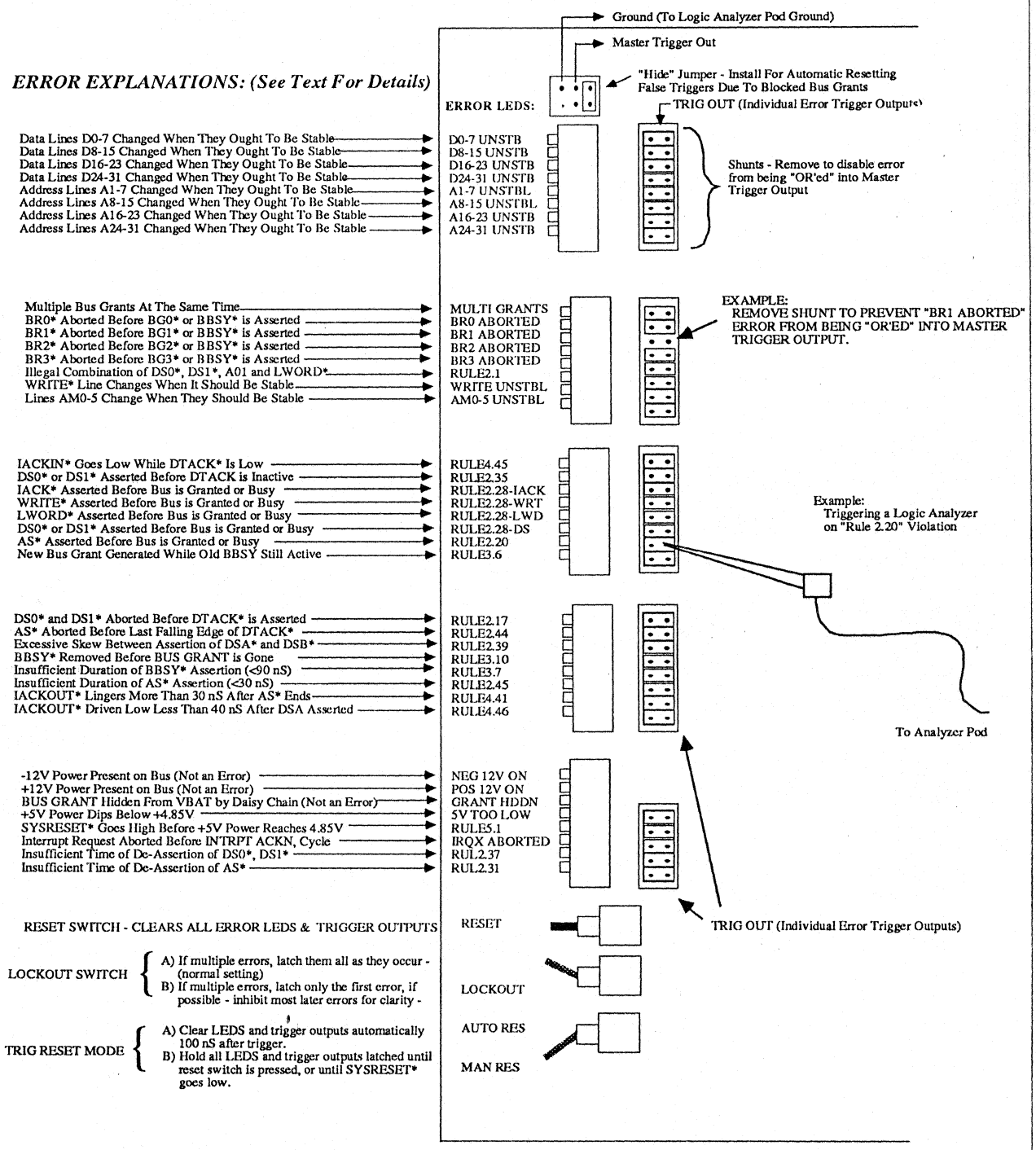


Figure 1. Switch, Jumper, LED and Trigger Functions

3. SPECIFICATIONS

VME BUS SPECIFICATION COMPLIANCE: *Revision C.1 October 1985, also IEEE P1014*

BOARD SIZE: *220 x 233 mm - Standard double-height VME board, but with extra length so that LED's and jumpers are conveniently accessible when board is installed in system.*

VIOLATIONS SCREENED FOR:

1) Data lines D31-D00 changing when they should be stable. (VMEbus specification rules 2.16, 2.48, 2.54, 2.56, 4.36, 4.38).

2) Address lines A31-A01 changing when they should be stable. (Rules 2.30, 2.40, 4.18).

3) Multiple bus grants (more than one at a time).

4) Bus request line(s) aborted prior to BBSY or bus grant active. (Part of Rule 3.11, also caused by Rule 3.13 violation).*

5) Illegal combination of DS0, DS1*, A01, LWORD* (Rule 2.1).*

6) WRITE line unstable when it should be stable. (Rules 2.38, 2.49, 4.23 and 4.31).*

7) Address Modifiers AM5-AM0 changing when they should be stable. (Rules 2.30 and 2.40).

8) IACKIN asserted while DTACK is low (Rule 4.45).*

9) DSO,1 asserted before DTACK* high (Rule 2.35, 4.20).*

10) IACK asserted before bus granted (Part of Rules 2.28, 4.16).*

11) WRITE asserted before bus granted (Part of Rule 2.28).*

12) LWORD asserted before bus granted (Part of Rules 2.28, 4.16).*

13) DSO,1 asserted before bus granted (Part of Rules 2.28, 4.16).*

14) AS asserted before bus granted (Rule 2.20, 4.16).*

15) New bus grant generated before BBSY rescinded (Rule 3.6).*

16) DS0,1 rescinded before DTACK asserted (Rules 2.17, 4.30).*

VIOLATIONS SCREENED FOR: (cont'd)

17)AS removed before last falling edge on DTACK* (Rules 2.44, 4.27).*

18) Excessive skew between DSA, DSB* assertion (Rules 2.39, 4.24).*

19) BBSY rescinded before bus grant goes high (Rule 3.10).*

20) Insufficient duration of BBSY - <90 ns (Rule 3.7).*

21) Insufficient duration of AS (Rules 2.45, 4.28).*

22) IACKOUT lingers more than 30 ns after AS* ends (Rules 4.41, 4.47).*

23) IACKOUT driven low less than 40 ns after DSA* (Rule 4.46).*

24) +5 Volt power dips below 4.85 Volts.

25) SYSRESET high before +5V power reaches 4.85V (part of rule 5.1).*

26) Interrupt request line(s) aborted prior to interrupt acknowledge cycle . (Rules 4.5 and 4.6).

27) Insufficient DS de-assertion time (Rules 2.37, 4.22).*

28) Insufficient AS de-assertion time (Rules 2.31 and 4.17).*

NOTE: All above rules are defined in detail in the user manual, and also in the Rev. C.1 VMEbus Spec. (and IEEE P1014 document).

NON-VIOLATIONS INDICATED:

1) +12 Volt and -12 Volt Power Present.

2) Daisy-chained bus grant(s) hidden from VBAT during error - VBAT therefore is unable to fully examine bus arbitration functionality.

TRIGGER CHARACTERISTICS:

1) Master active-low trigger, as well as individual active-low TTL output for each type of violation.

2) Trigger speed: *Individual Triggers: Asserted 20 to 80 nS after fault*
Master Trigger: Asserted within 100 nS of fault

3) Any or all violation triggers may be used independently & concurrently.

4) Trigger lockout modes: *A) If more than one fault, all faults indicated.*
B) If more than one fault, only first fault generally indicated, if possible. Later faults locked out where possible.

5) Trigger reset modes: *A) Manual - error LED and trigger are latched until reset via pushbutton.*
B) Automatic - LED and trigger reset approximately 90 ns after occurrence.

4. WHAT THE VBAT CAN AND CANNOT DO

The following are examples of problems the VBAT **can** help uncover.

1) Improper design of a board's bus interface circuitry.
2) Metastable conditions in the arbitration circuitry.
3) Errors in the interrupter circuitry.
4) Excessive bus noise, including cross-talk, ringing and ground-bounce.
5) Two masters simultaneously attempting to access the bus.
6) Two slaves responding to the same address.
7) Slave boards which do not respond with stable data at the time they assert DTACK*.

WHAT THE VBAT CANNOT DO

The VBAT cannot be used as a completely "definitive bus compliance validator"' since it does not check for all possible bus specification violations. Also, while the VBAT triggers on most significant violations of bus timing, a signal only out of spec by several nanoseconds may not trigger it.

The VBAT cannot detect bugs which do not, at least indirectly cause illegal bus timing on the signals lines tested by the VBAT. Fortunately, a wide variety of hardware design bus in VME boards DO affect the bus timing in such a manner as to be detectable by the VBAT.

While the VBAT, when properly used, is believed to be free of any deficiencies which could indicate false errors, an error indication by the VBAT should never, by itself, be used to implicate a vendor. All errors reported by the VBAT should be verified by actually viewing the bus activity causing the error using a 100 MHz, or faster, logic analyzer. This is extremely easy to do, since the VBAT's trigger will point to the precise time the error occurs. Only on the basis of such subsequent confirmation of the existence of errors should any vendor be presumed to be at fault. Please refer to the section "Operating Instructions" for the proper methods for preventing false error indications.

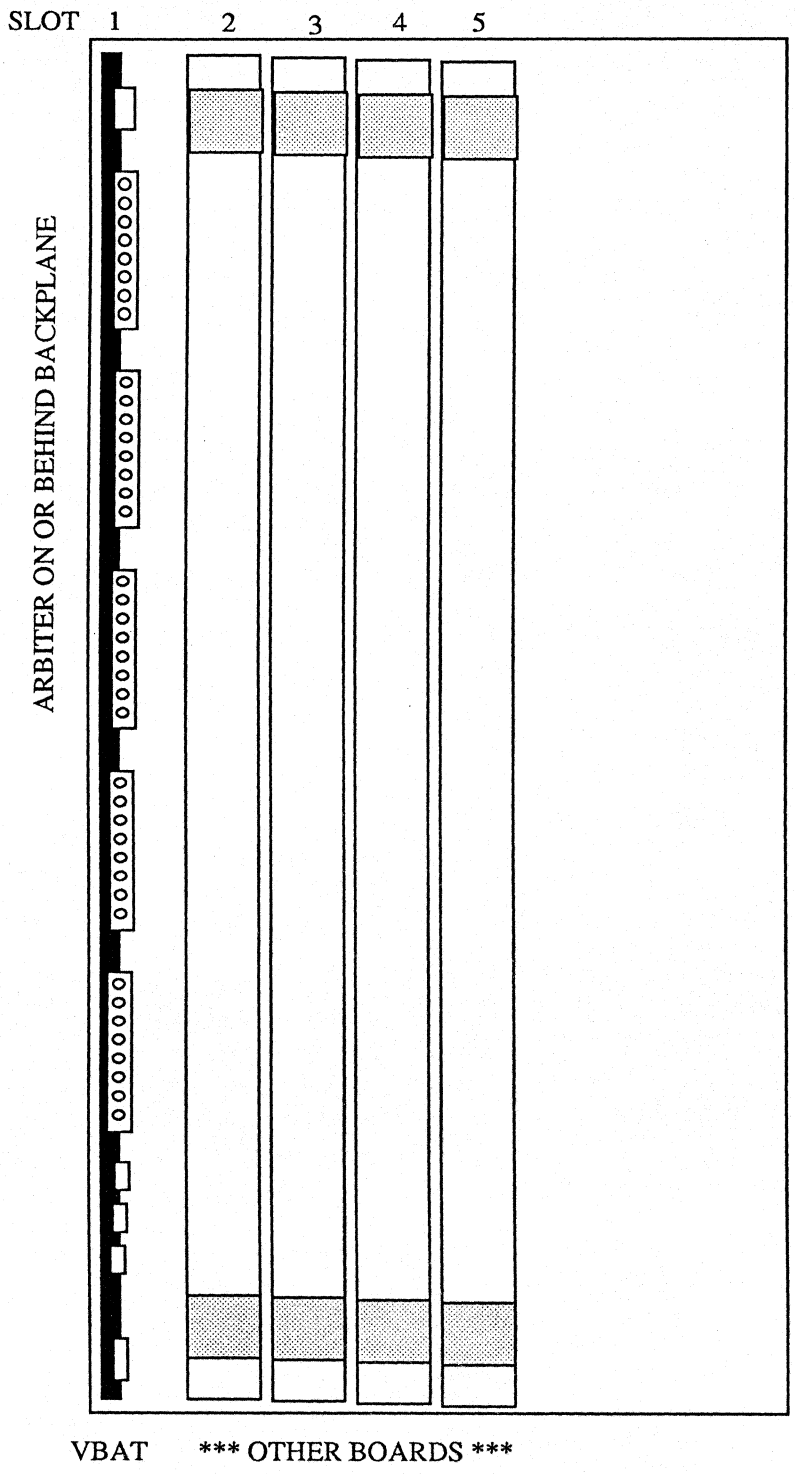


Figure 2a - Ideal Location

(Usable only if Arbiter is on or behind backplane.)

5. OPERATING INSTRUCTIONS

The VME BUS ANOMALY TRIGGER is very easy to use. The following are the steps in using the board.

1) Turn power on VME system OFF.

2) Plug VME BUS ANOMALY TRIGGER into empty slot on bus. It is not necessary to remove or install daisy-chain jumpers for that slot - they may be left in whatever condition they were originally in. Generally, the VBAT should be plugged as close to the leftmost slot as possible, so that the operation of the beginning of the bus grant daisy chains will be visible to the VBAT, and not blocked by bus masters using the bus. DO NOT USE AN EXTENDER BOARD, FOR BEST RESULTS. If an extender must be used, its length must not exceed 12 inches, and it must contain full ground and power planes.

> ***IMPORTANT***
>
> *If the system arbiter is located on the motherboard itself, the VBAT should initially be located in the very FIRST slot on the bus. See figure 2A.*
>
> *If the system arbiter is located on the master in the first bus slot, then the VBAT should initially be located in bus slot 2. See figure 2B. In this case certain errors may momentarily be falsely indicated by the VBAT, as discussed later.*

3) Set board switches as described below in "SWITCH FUNCTIONS". For initial debugging, set the board to "MAN RES" and do not use lockout.

4) Boot up system, and run it as usual. Be sure to use the system in such a way that all masters and slaves access the bus, or are accessed.

5) If one or more red LED's illuminate, a violation has occurred. A trigger signal (low-going transition) will simultaneously occur on the corresponding jumper post(s), for effortlessly triggering a logic analyzer. Figure 1 illustrates the correct points for connecting a line from the VBAT to

trigger a logic analyzer. For best results use a logic analyzer set for 100 MHz, or faster, acquisition speed. In some cases, a logic analyzer sampling rate of up to 400 MHz may be needed to verify very short errors.

Each type of violation is discussed in detail in the later section of this manual. As mentioned in (2) above, some false errors will momentarily occur if the board is located downstream (in a slot to the right of) any bus master, due to one or more bus grant daisy chain signals being blocked by the master. The VBAT will automatically reset these errors if the HIDE jumper is installed, as shown in figure 1. The momentary trigger signals for such an error may be blocked (prevented from being OR'ed into the master trigger) by removing the jumper located directly behind the LED indicating the error, as illustrated in figure 1. To avoid confusion, use only the INDIVIDUAL TRIGGER OUTPUTS (not the master trigger) when debugging.

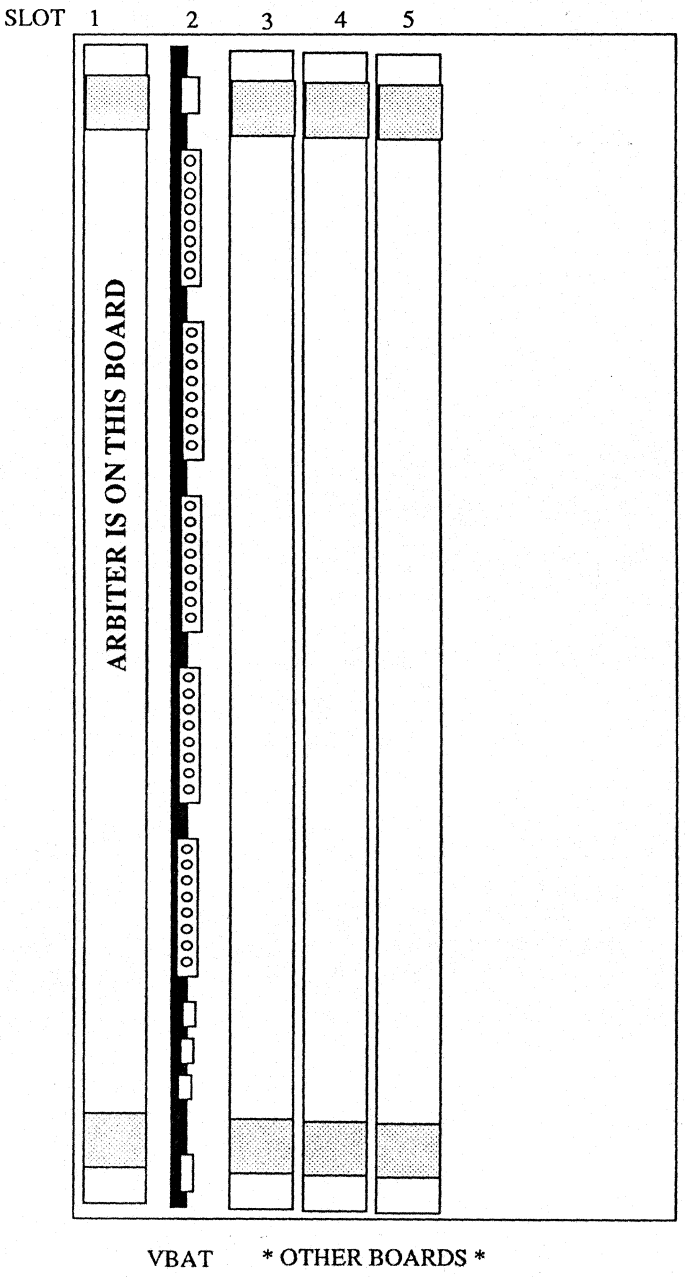


Figure 2b - Acceptable Location

(Required in most installations because Arbiter is located on the board in Slot 1.)

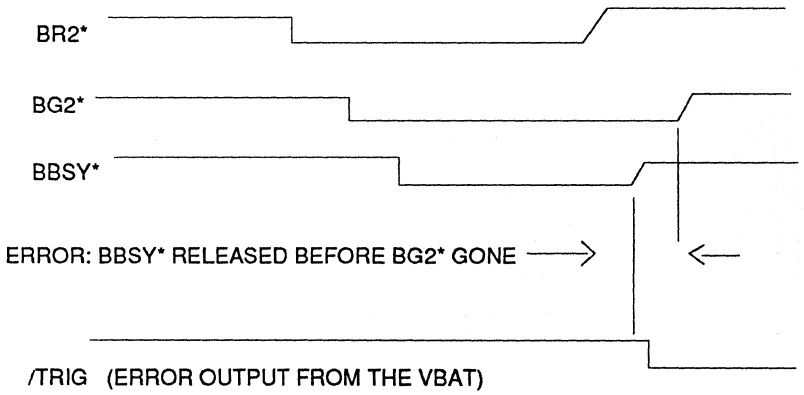
5.1 SWITCH FUNCTIONS

There are three switches on the VME BUS ANOMALY TRIGGER board. Their functions are discussed below:

1) AUTO RESET/MAN RESET SWITCH.

In the MAN RES position, the trigger signal(s) will remain active and the corresponding LED(s) will remain illuminated until manually reset using the RESET pushbutton. This is normally the best mode for troubleshooting. Always use the MAN RES position if there is more than one violation in your VME system.

In the AUTO RES position, the trigger signal will automatically reset itself after approximately 100 nanoseconds. This position allows fast re-arming in the case that multiple occurrences of the trigger signal are to be acquired using a logic analyzer. Due to the short duration of the trigger signal, the LED's will usually not be visible in this modes.



Example of operation: "RULE3.10" VIOLATION - VBAT recognizes a master illegally rescinding BBSY* before bus grant goes high.

In some cases, in which the error repeats itself at a high rate (e.g. every cycle by a particular master), the LED may glow dimly, and VBAT's trigger signal may be used to trigger an ordinary oscilloscope to view the bus activity at the time of the trigger. If the scope has pre-trigger viewing (i.e. >30 ns delay lines in the vertical channels), it is often possible to view the few nanoseconds leading up to the trigger, and thus see the cause.

NEVER use the AUTO RES mode if more than one error is present, as the occurrence of the first error may cause the second error to be ignored.

2) LOCKOUT SWITCH

In the LOCKOUT position, if more than one violation is found, and if the first violation occurs more than 100 nanoseconds before the next, only the violation event which first occurs will usually be detected, and will illuminate the appropriated LED. This enables the "real initiator" of the trouble to be distinguished from subsequent events. Note that the following error conditions CANNOT be blocked, even if they occur subsequent to the first.

BRO ABORTED, BR1 ABORTED, BR2 ABORTED, BR3 ABORTED,
WRITE UNSTBL, RULE2.35, RULE2.17, RULE2.44,
RULE2.39, RULE2.45, RULE4.41, RULE4.45, RULE4.46,
RULE2.37, RULE2.31

If the switch is NOT in the LOCKOUT position, all violations which occur will illuminate the appropriate LED's as they occur. These LED's will remain lit until the trigger is RESET. For simplest debugging, it is generally best NOT to use the LOCKOUT mode.

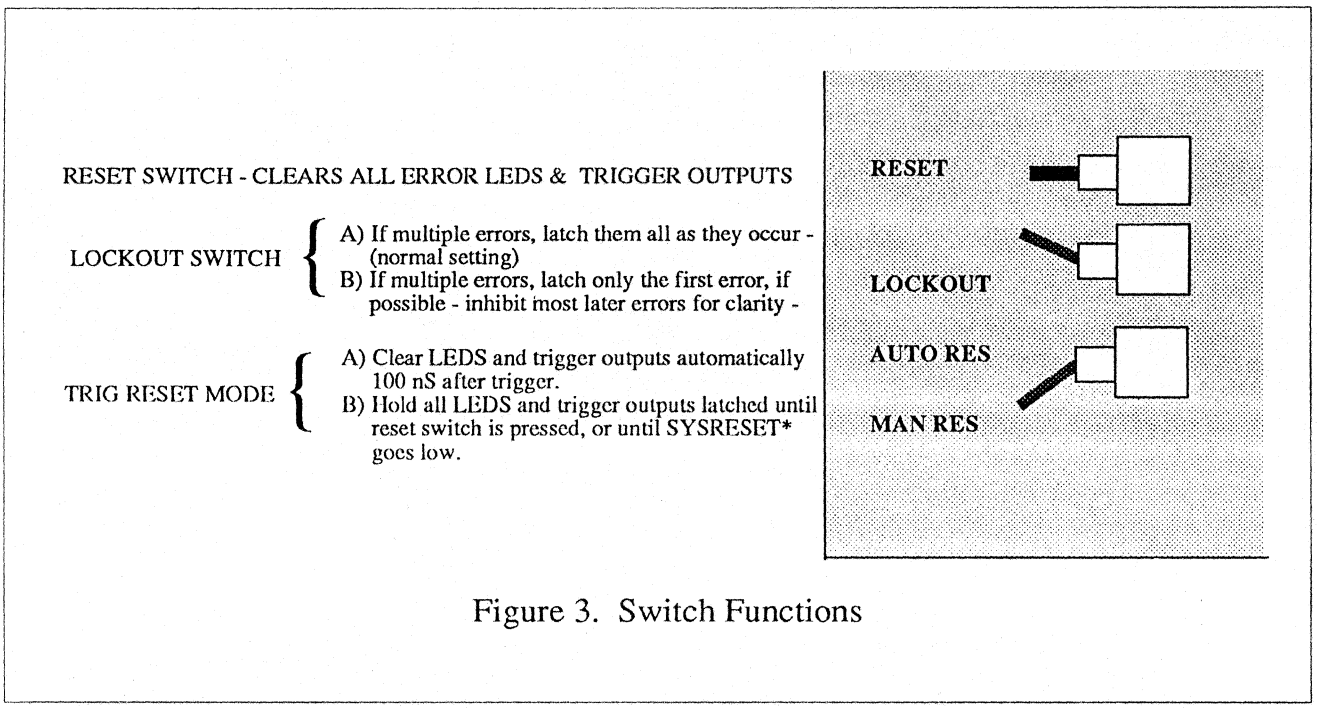


Figure 3. Switch Functions

5.2 JUMPER SETTINGS

"ERROR-ENABLE" JUMPERS (SHUNTS)

Behind each RED error LED there is a jumper (shunt), as shown in figure 1. Each installed shunt enables the trigger for the corresponding error to be OR'ed into the master trigger signal. If the shunt is removed, the error will not cause the master trigger signal to be asserted. Regardless of whether or not a given shunt is installed, if an error occurs, the corresponding LED will light and the post at the jumper position furthest from the LED will contain the trigger signal for that error only. In this way, the individual error trigger signals are each available separately. Figure 1 illustrates the connection of a logic analyzer to one of these individual trigger lines. Set up the logic analyzer to trigger when this line is a logic 0.

Normally, all of the shunts should be installed, as there is really no reason for even using the master trigger. If a violation occurs repeatedly, but this error has been determined NOT to be causing the actual system problem, you may temporarily ignore the error LED and its corresponding individual trigger. However, the system problem which leads to this error should eventually be fixed. Most of the errors revealed by the VBAT board are potentially serious, and should not be permanently ignored.

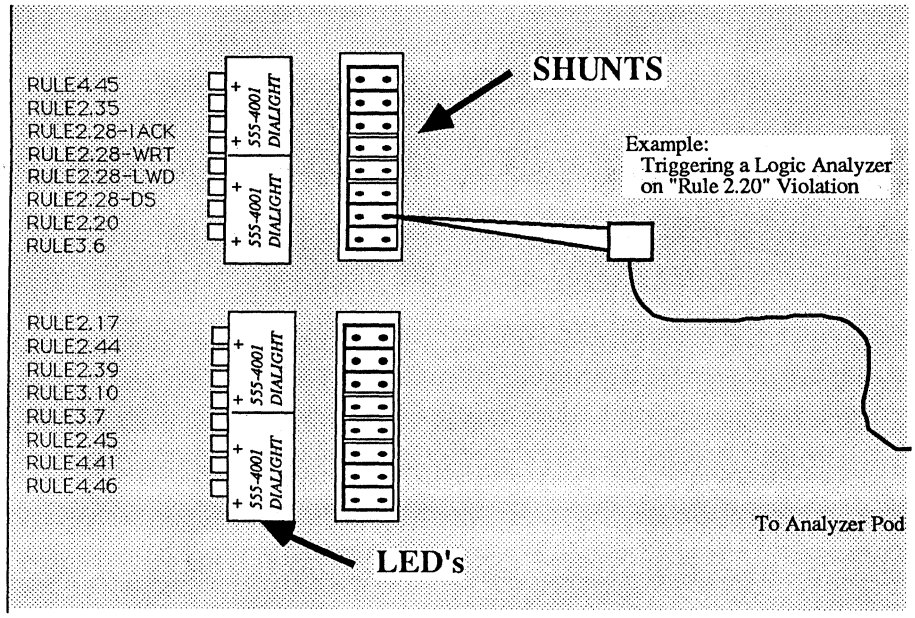


Figure 4. "Error-Enable" Jumpers

"HIDE" JUMPER

As mentioned above, some false errors will be recognized if the board is located downstream (in a slot to the right of) an active bus master, due to one or more bus grant daisy chain signals being BLOCKED by the master. These conditions appear as errors, since the VBAT will see BBSY*, AS*, DS0*, DS1*, WRITE*, or LWORD* but it will not first see the necessary grant signal (BG0*, BG1*, BG2*, or BG3*). The false errors which may be indicated are as follows:

BR0 ABORTED, BR1 ABORTED, BR2 ABORTED, BR3 ABORTED
RULE2.28-IACK, RULE2.28-WRT, RULE2.28-LWD, RULE2.28-DS,
RULE2.20

The best way to prevent any of the above possible false errors is to locate the VBAT as close to the arbiter as possible, ideally in the leftmost slot in the backplane if the arbiter is located on the back of the backplane, as shown in figure 2(a). If this is not possible, and it usually is NOT, then the VBAT should be located in the SECOND slot in the backplane, as shown in figure 2(b). One or more momentary false errors would then only occur when the board in the first slot is an active master (drives the bus).

Fortunately, the VBAT will automatically reset these errors if the HIDE jumper is installed, as shown in figures 1 and 5. In this case the error trigger will momentarily go active (low) when the error is (falsely) thought to be present. Then, as soon as BBSY* goes active, the absence of any of BG0* through BG3 (due to daisy chain blockage) will cause the VBAT to automatically reset the error, which it only then knows is a false alarm. This resetting occurs within a few tens of nanoseconds in most cases. The presence of one of these momentary errors will be indicated by the yellow "GRANT HDDN" LED being illuminated.

For simplest debugging, the HIDE jumper should always remain installed.

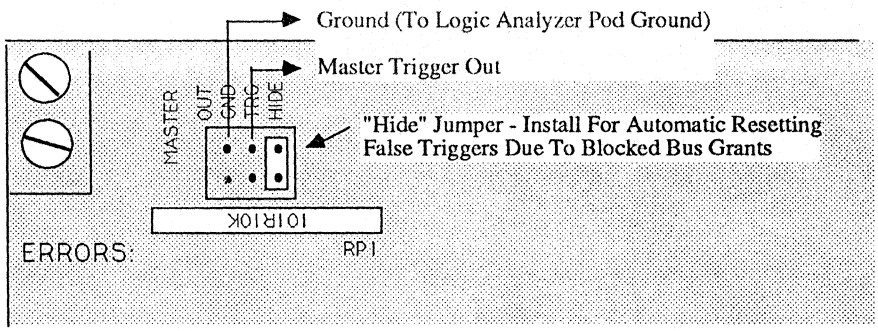


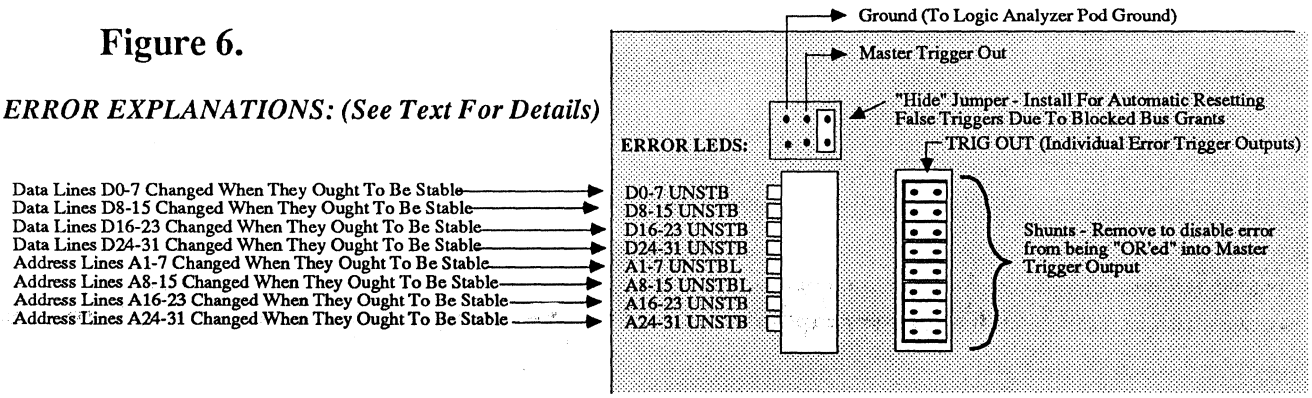
Figure 5. "Hide" Jumper

6. BRIEF SUMMARY OF ERROR INDICATORS

ERROR TITLE	H/F*	BRIEF DESCRIPTION
D0-7 UNSTB		Data lines D0-D7 change during an interval when they should be stable.
D8-15 UNSTB		Data lines D8-D15 change during an interval when they should be stable.
D16-23 UNSTB		Data lines D16-D23 change during an interval when they should be stable.

Figure 6.

ERROR EXPLANATIONS: (See Text For Details)



D24-31 UNSTB	Data lines D24-D31 change during an interval when they should be stable.
A1-7 UNSTB	Address lines A1-A7 change during an interval when they should be stable.
A8-15 UNSTBL	Address lines A8-A15 change during an interval when they should be stable.
A16-23 UNSTBL	Address lines A16-A23 change during an interval when they should be stable.
A24-31 UNSTBL	Address lines A24-31 change during an interval when they should be stable.

MULTI GRANTS *H* More than one grant (BG0* - BG3*) occurs at a time.

BR0 ABORTED *F* Bus request BR0* is rescinded before BG0* occurs.

BR1 ABORTED *F* Bus request BR1* is rescinded before BG1* occurs.

BR2 ABORTED *F* Bus request BR2* is rescinded before BG2* occurs.

BR3 ABORTED *F* Bus request BR3* is rescinded before BG3* occurs.

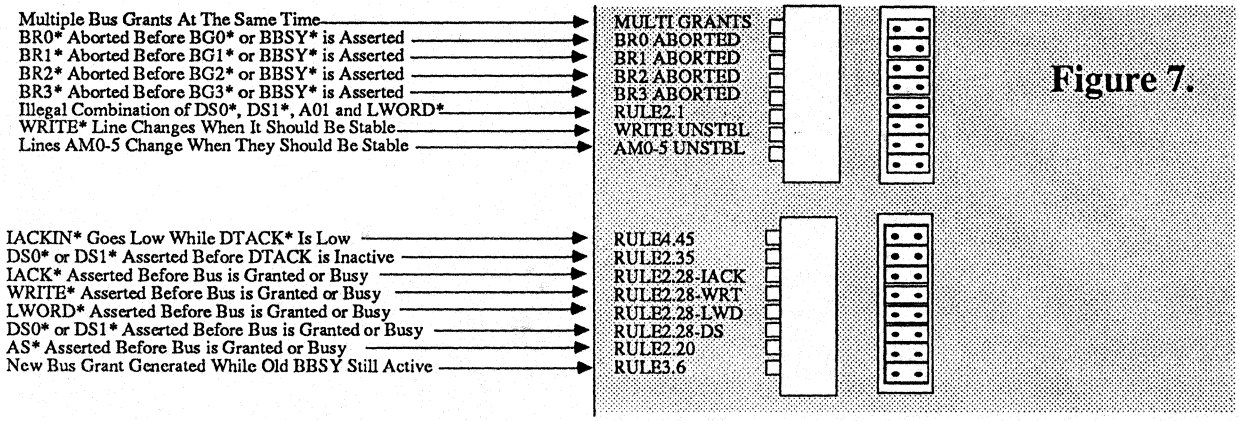


Figure 7.

RULE2.1 Either of the following illegal combination occur:
DS1* = high, DS0* = low, A01 = high, LWORD* = low
or DS1* = low, DS0* = high, A01 = high, LWORD* = low

WRITE UNSTBL WRITE* line is not stable (i.e. changes state) during time when data strobes DS0*, DS1* are active.

AM0-5 UNSTB Address Modifier lines AM0-AM5, or IACK line change during an interval where they should be stable.

RULE4.45 IACKIN* is asserted while DTACK* is active (low).

RULE2.35 DS0* or DS1* are driven low before DTACK* and BERR* have gone high (inactive).

RULE2.28-IACK *F* IACK* is driven low before the bus has been properly granted to the master.

RULE2.28-WRT *F* WRITE* is driven low before the bus has been properly granted to the master.

RULE2.28-LWD	*F*	LWORD* is driven low before the bus has been properly granted to the master.
RULE2.28-DS	*F*	DS0* or DS1* are driven low before the bus has been properly granted to the master.
RULE2.20	*F*	AS* is driven low before the bus has been properly granted to the master.
RULE3.6	*H*	A new bus grant is generated before BBSY* goes away.
RULE2.17		DS0* or DS1* are rescinded before DTACK* or BERR* are received.
RULE2.44		AS* is rescinded before the last falling edge on DTACK* or BERR* occurs.
RULE2.39		Excessive skew (>20 ns) between the starting edges of the first and second data strobes.
RULE3.10	*H*	Requester rescinds BBSY* before bus grant goes high.
RULE3.7		BBSY* is active for too short a time (< 90 ns).

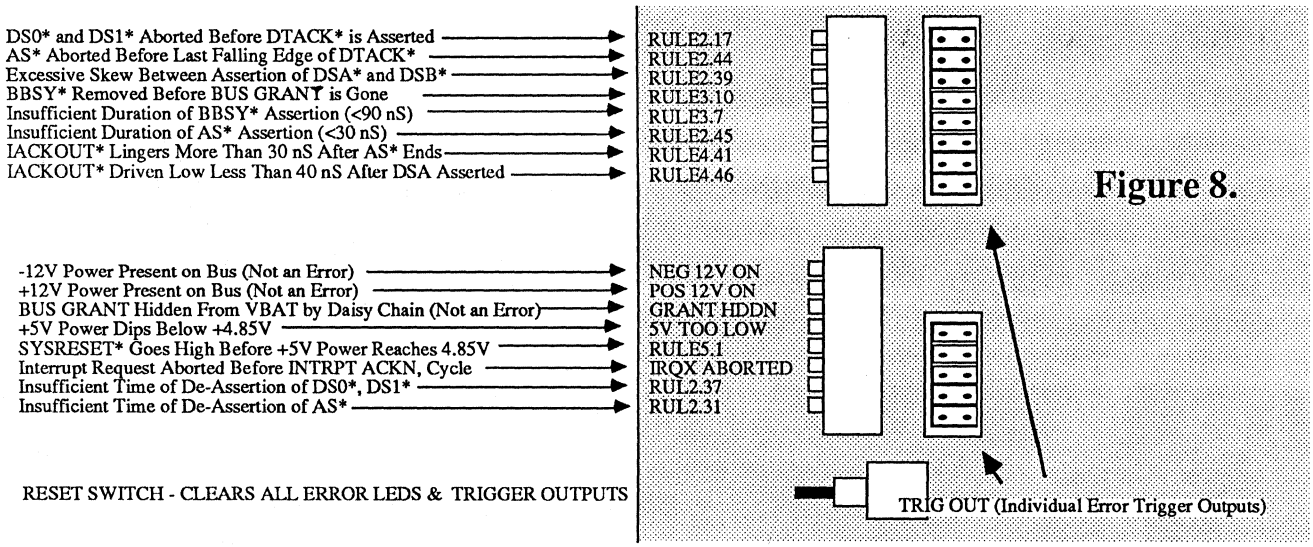


Figure 8.

RULE2.45		AS* is active for too short a time (less than 30 ns)
RULE4.41	*H*	IACKOUT* line of a master is not driven high within 40 ns after AS* is driven high. Error condition is only visible for boards which are located to the left of the VBAT.

RULE4.46	*H*	IACKOUT* line is driven low less than 30 ns after the falling edge on AS*, when the IACKIN* is low when the IACK DAISY-CHAIN DRIVER detects a falling edge on DSA.
NEG 12V ON		-12 Volt power exists on the bus. NOT AN ERROR.
POS 12V ON		+12 Volt power exists on the bus. NOT AN ERROR.
GRANT HDDN		The VBAT was not able to fully detect errors on the bus grant daisy chain signals BG0-BG3, because the VBAT was located to the right of the active master, and the daisy chain signal was BLOCKED. NOT ITSELF AN ERROR CONDITION.
5V TOO LOW		+5 Volt power on the bus dipped below 4.85 volts.
RULE5.1		During power up, the SYSRESET* signal goes away before the +5V lines go above 4.85 volts.
IRQX ABORTED		An interrupt line IRQ1-IRQ7 is aborted before the appropriate interrupt acknowledge cycle is started.
RULE2.37		DS0* or DS1* are inactive for an insufficient time between successive bus cycles (<30 ns).
RULE2.31		AS* is inactive for an insufficient time between successive bus cycles (<30 ns).

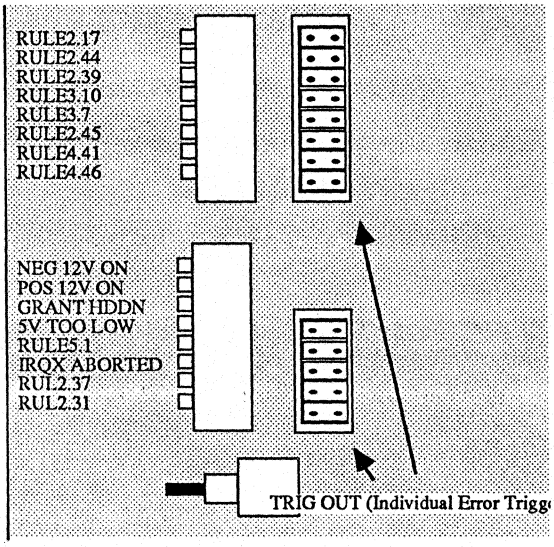


Figure 9.

NOTES:

*1) "*H*" denotes an error which may NOT be detected if a bus grant or IACKIN/IACKOUT daisy chain, is interrupted before the appropriate BGx* or IACKOUT* signal could reach the VBAT. To remedy this, the VBAT should, where possible, be located to the left of an active master which could block the daisy chain.*

*2) "*F*" denotes an error which may momentarily be FALSELY detected, even though no error condition actually exists, if a bus grant daisy chain is interrupted before the appropriate BGx* signal could reach the VBAT. This error will automatically be cleared by the VBAT as soon as the BBSY* signal occurs if the HIDE jumper is installed in the VBAT. However, to prevent even this momentary error indication, the VBAT should, where possible, be located to the left of a master which could block the daisy chain. If not possible, and if the momentary low-going trigger cannot be tolerated, it may be necessary to ignore these momentary error indications. Fortunately none of these errors will remain latched (if the HIDE jumper is installed).*

7. HOW TO USE THE VBAT TRIGGER OUTPUT TO VIEW THE ACTUAL VIOLATIONS, AND WHAT TO DO IF YOU CANNOT SEE THEM!

The most common problem VBAT users encounter is seeing one of its LED's light up, but then being unable to actually see anything wrong with the bus signals when using the corresponding trigger output to trigger a logic analyzer. This can be quite frustrating, since the VBAT obviously believes something is wrong, but when displaying the actual relevant bus signals on the logic analyzer screen, everything looks normal. However, usually there is a subtle, but real problem which warrants further investigation.

The following are the main reasons for getting a trigger from the VBAT, but being unable to see the violation:

I. VIEWING THE WRONG BUS CYCLE WITH THE LOGIC ANALYZER

You may not be viewing the actual cycle which is generating the trigger. To prevent this possibility, it is simply necessary to do the following:

1) Always use the individual triggers, and not the master trigger. In this way, there can be no question as to which type of error to look for at the time of the trigger.

2) Always display the actual VBAT TRIGGER OUTPUT on the logic analyzer along with the relevant bus signals. In this way, when you see the high-to-low transition of the trigger signal, the erroneous bus signals will be easy to spot, as they will be very closely time-aligned with the trigger signal's transition. Generally the violation will be seen 20 to 80 nanoseconds before the low-going transition of the trigger signal.

3) It is generally best to use the MAN RES mode, and only trigger on lines whose LEDs stay latched on. As mentioned earlier, some errors will momentarily appear, due to bus grant daisy chain signals being hidden from the VBAT, but will automatically reset within a few tens of nanoseconds. Therefore, by ignoring all LEDs which do not stay latched, NONE of these false errors will ever be a problem.

II. INSUFFICIENT LOGIC ANALYZER BANDWIDTH

The logic analyzer or digital strorage scope may not have sufficient bandwidth to see certain very brief violations which the VBAT is capable of reliably detecting. The VBAT can trigger on certain violations (primarily glitches on strobe, data and address lines) which are as brief as 3 nanoseconds in duration. A 50 MHz, 100 Mhz or even 200 MHz logic analyzer may simply not be fast enough to reliably catch such short glitches. Even if the glitch coincides with the actual instant in which the analyzer is sampling the signal, it still may never be detected by the analyzer! This could occur if the analog bandwidth of the input buffers in the logic analyzer pods is insufficient. The actual analog probe bandwidth is often not a good match for its sampling rate. In this case, the brief glitch may come and go before the pod's slow rise time gives the buffered signal a chance to cross the logic analyzer's threshold. For this reason, if the VBAT gives an error but you are unable to actually see any problem, we recommend the following:

1) Use a faster logic analyzer. While a 100 MHz sampling speed is fast enough for viewing most violations, in some case a sampling rate of 400 MHz or more may be required.

2) If the violation is still not visible, change the threshold of the analyzer. Certain glitches in VMEbus systems have amplitudes of only two volts or so. Generally, if the logic analyzer threshold is tried at both 1.2 volts and at 2.0 volts, the problem will be seen.

3) If the problem is still not visible, please call Ultraview Customer Support at (415) 657-9501, who will be eager to assist you in tracking down the problem.

III. MARGINAL BUS SIGNALS

Very high frequency bus noise may be confusing the VBAT into thinking that there is an error. Such noise and ringing may not be visible on any but the fastest logic analyzers and scopes.

1) Look for excessive ringing on the falling edge (high to low transition) of strobes. Such ringing will effectively make the strobe appear to momentarily go high 10-30 nanoseconds after it goes low, triggering the VBAT (and potentially causing problems in VME systems). Such ringing can only be studied properly with an oscilloscope having a bandwidth of 250 to 400 MHz or faster. A slower oscilloscope may have insufficient rise time to accurately track the fast slewing waveform, resulting in the ringing appearing to have much less amplitude than it really has! What you see with any instrument is a band-limited version of what is really happening. Also, when using a fast oscilloscope, it is crucial to use the shortest ground lead

available for the particular scope probe. Some probes have a 2-5 inch ground lead for general use, and a 1-inch ground lead which is recommended for viewing very high frequency signals.

2) Look for excessively slow rising edges on strobes. Bus noise, in combination with these slow-rising edges may make the VBAT think that the signals have multiple transitions, when in fact there is only one. The following open collector signals, which will often have rise times of 20 to 100 nanoseconds may be capable of falsely triggering the VBAT:

DTACK*, BERR*, BBSY*

The following tri-state or totem-pole signals may also rise slowly, and may falsely trigger the VBAT:

AS*, BG0*-BG3*, DS0*, DS1*, LWORD*, WRITE*, IACK*

The rising edge of such strobes should be monitored with a 250MHz (or faster) oscilloscope. If these slow-rising signals rise to 2.4 volts within 100 nanoseconds, and if any superimposed noise is has a peak-to peak amplitude of less than 0.5 volts, then the VBAT's error may generally be ignored, as there will probably be no resulting problems in the systems. However, if the rise time is greater than 150 nanoseconds, it may be the result of excessive capacitance on these lines, often caused by VME boards having PC traces much longer than the 2-inch maximum called out in the VMEbus specification. Noise greater than 0.5 to 1 volt peak-to peak may actually not be noise, but a glitch, in which an offending buffer is turned off or driven high, and then momentarily driven low again.

It should be noted that signals which either rise so slowly, or have so much ringing that they appear to have multiple transitions may not only "fool" the VBAT, but would also potentially fool other VME boards whose receivers do not have hysteresis. Receivers which have hysteresis (e.g. 74LS244, 74LS240) are recommended by the spec, but appear NOT to be required, potentially causing system problems. Therefore, such problems should be closely investigated. **Ultraview Customer Support**, at (415) 657-9501, will be eager to discuss such issues with you in more detail. Such support is supplied at no charge and is considered to be part of our product. We encourage you to take advantage of it.

8. DETAILED EXPLANATION OF ERRORS

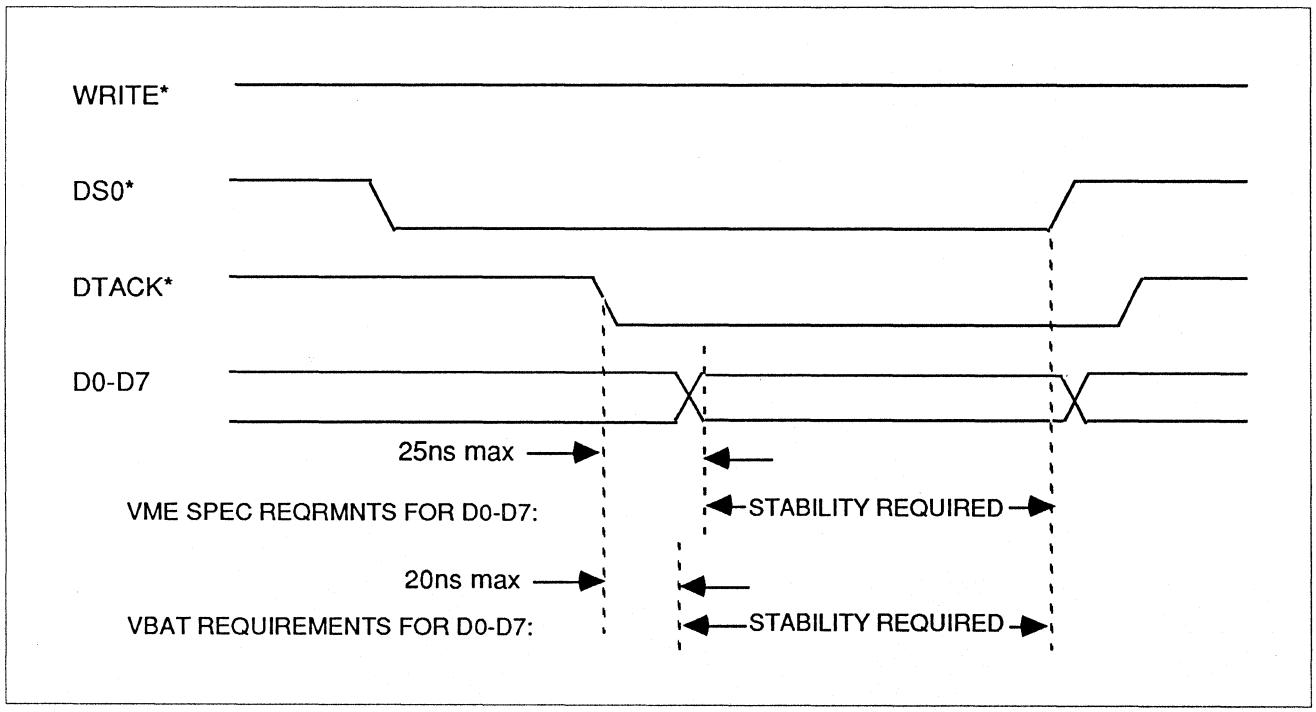
A description of each type of error indication is given below, along with occasional suggestions as to the type of design problem which could lead to the specific error. For more details, the VMEbus specification should be consulted.

8.1 D0-7 UNSTB

The "D0-7 UNSTB" LED illuminates when a change is detected on data lines D0-7 during an interval where these lines should be stable. The conditions under which they are checked for stability depend upon the type of bus cycle in progress. Each type of cycle is discussed below. As the VBAT is capable of seeing instabilities lasting as short as 5 nanoseconds, a logic analyzer with an acquisition speed of 400 MHz may be required to verify the shortest instabilities. The following signals must be viewed on the logic analyzer to verify this error: D0-7, DS0, DTACK*, WRITE*, and the trigger post behind the D0-7 UNSTB LED.

8.1.1 D0-7 unstable during VME bus read cycle

The following diagram illustrates the key signals present during a normal VME bus read cycle, and shows the time period during which data lines D0-7 are required to be stable.

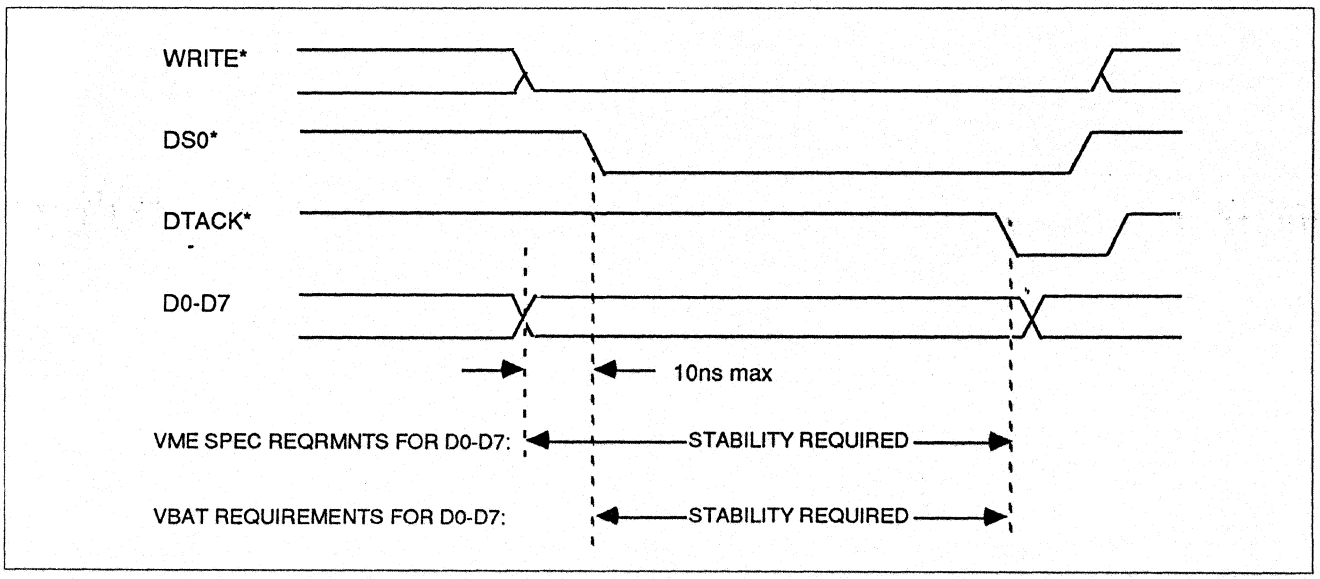


CONDITIONS WHICH COULD CAUSE THE ABOVE ERROR:

1) Memory board, or other slave, asserts DTACK* before it is supplying valid data.
2) Design error in slave, in which data is not latched and therefore does not remain stable and valid even after addresses go away and until data strobe DSO* is rescinded.
3) Design error in slave, in which board selects itself using address strobe (AS*) only. In this way, the slave may be falsely responding to a bus cycle when it is really not being addressed. This will result in two slaves responding to the same bus cycle.
4) Design error in master, in which master's data transceivers are illegally changed in directions after DTACK, and consequently "fight" with slave's buffers.

8.1.2 D0-7 unstable during VME bus write cycle

The following diagram illustrates the key signals present during a normal VME bus write cycle, and shows the time period during which data lines DO-7 are required to be stable.



CONDITIONS WHICH COULD CAUSE THE ABOVE ERROR:

1) Design error in a bus master, in which data is not set up sufficiently in advance of the assertion of DSO* or so that data does not remain until DTACK* is detected.
2) Design error in bus arbitration in one or more masters, resulting in two or more masters taking control of the bus simultaneously. This condition is most common in systems in which overlapped arbitration (early release of BBSY*) is employed, due to increased opportunity for design errors.

8.2 D8-15 UNSTB

The "D8-15 UNSTB" LED illuminates when a change is detected on data lines D8-D15 during an interval where these lines should be stable. The conditions for stability are essentially the same as for "D0-7 UNSTB" above, but with DS1* substituted for DS0* in the above diagram.

8.3 D16-23 UNSTB

The "D16-23 UNSTB" LED illuminates when a change is detected on data lines D16-D23 during an interval where these lines should be stable. The conditions for stability are essentially the same as for "D0-7 UNSTB." Of course, stability is checked for D16-23 during longword cycles only.

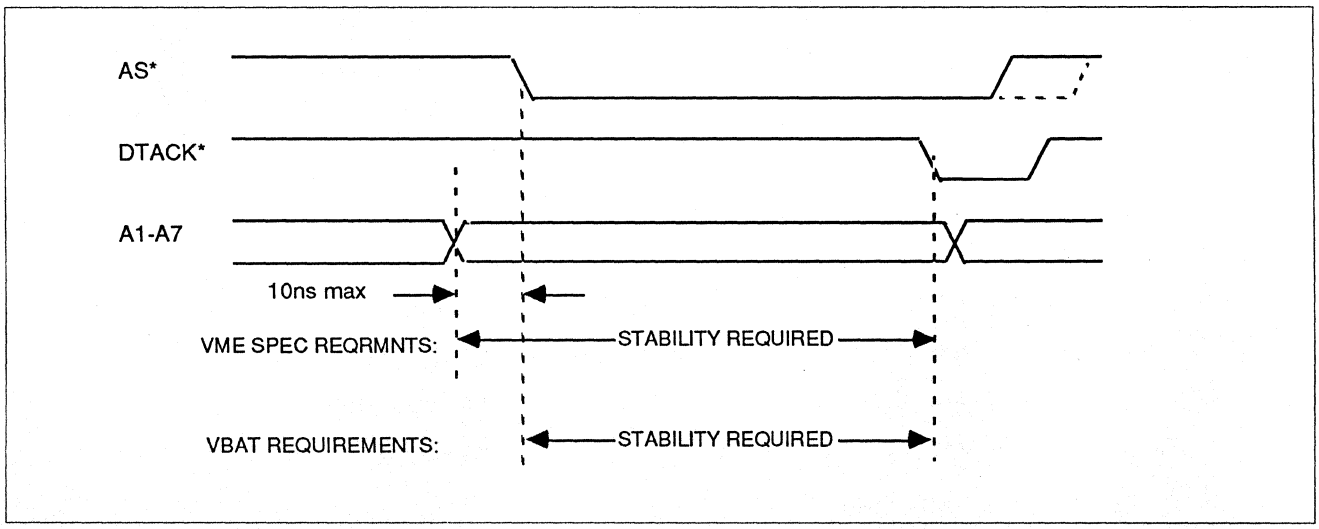
8.4 D24-31 UNSTB

The "D24-31 UNSTB" LED illuminates when a change is detected on data lines D24-D31 during an interval where these lines should be stable. The conditions for stability are essentially the same as for "D18-15 UNSTB." Of course, stability is checked for D24-31 during longword cycles only.

8.5 A1-7 UNSTB

The "A1-7 UNSTB" LED illuminates when a change is detected on address lines A1-A7 during an interval where these lines should be stable. Since the VBAT can detect instabilities lasting as short as 5 nanoseconds, a 400 MHz logic analyzer may be required to verify these instabilities, in some extreme cases. The following signals must be viewed on the logic analyzer to verify this error: A1-A7, AS*, DTACK* and the trigger post behind the A1-7 UNSTB LED.

The following diagram illustrates the key signals present during a normal VME bus cycle, and shows the time period during which address lines A1-7 are required to be stable.



CONDITIONS WHICH COULD CAUSE THE ABOVE ERROR:

1) Design error in a bus master, in which address is not set up sufficiently in advance of the assertion of AS* or so that address does not remain until DTACK* is detected.
2) Design error in bus arbitration in one or more masters, such that two or more masters take control of the bus simultaneously. This condition is most common in systems in which overlapped arbitration (early release of BBSY*) is employed, due to slightly increased opportunity for design errors.

8.6 A8-15 UNSTBL

The "A8-15 UNSTB" LED illuminates when a change is detected on address lines A8-A15 during an interval where these lines should be stable. Stability is checked during all cycles except interrupt acknowledge VMEbus cycles, as these cycles do not use lines A8-A15.

8.7 A16-23 UNSTBL

The "A16-23 UNSTB" LED illuminates when a change is seen on lines A16-A23 during an interval where these lines should be stable. Stability is only checked during cycles in which "standard" or "extended" addressing are specified by the address modifiers, as short address and interrupt acknowledge cycles do not use lines A16-A23.

8.8 A24-31 UNSTBL

The "A24-31 UNSTB" LED illuminates when a change is detected on lines A24-A31 during an interval where these lines should be stable. Stability is only checked during all cycles in which "extended addressing" is indicated by the address modifiers, since no other cycles use these lines.

8.9 MULTI GRANTS

The "MULTI GRANTS" LED illuminates when more than one bus grant (BG0* - BG3*) occurs at a time. The VME specification requires that only one grant should ever occur at any time. The following signals must be viewed on the logic analyzer to verify this error: BG0*, BG1*, BG2*, BG3* and the VBAT's trigger post behind the MULTI GRANTS LED.

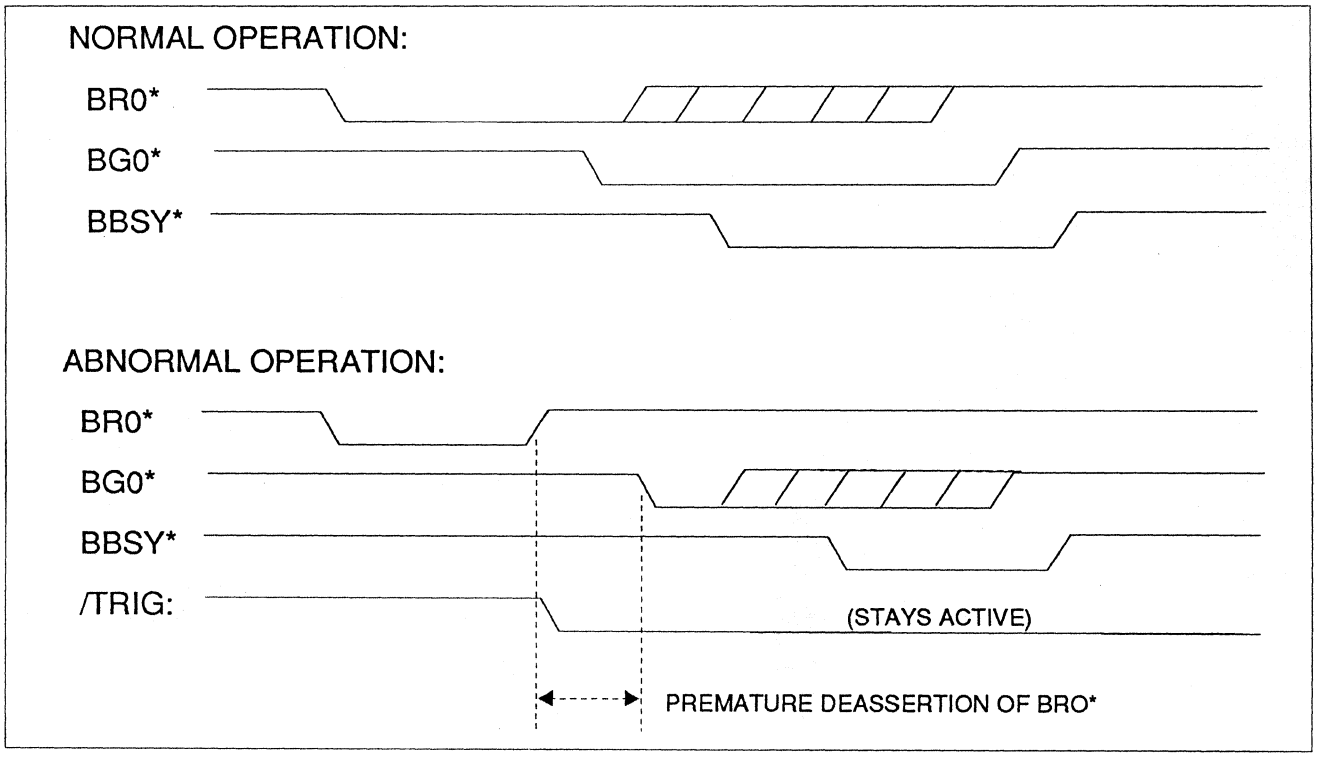
This error will not be visible to the VBAT if the VBAT is located to the right of a master which is taking over the bus and therefore does not pass a grant down the daisy chain.

CONDITIONS WHICH COULD CAUSE THE ABOVE ERROR:

1) Design error in a bus arbiter, in which grants at two or more levels are simultaneously generated.
2) Design error in bus grant daisy chain circuitry in a master which resides to the left of the VBAT, causing the master to generate a BGxOUT* signal even when no BGxIN* is issued to it.

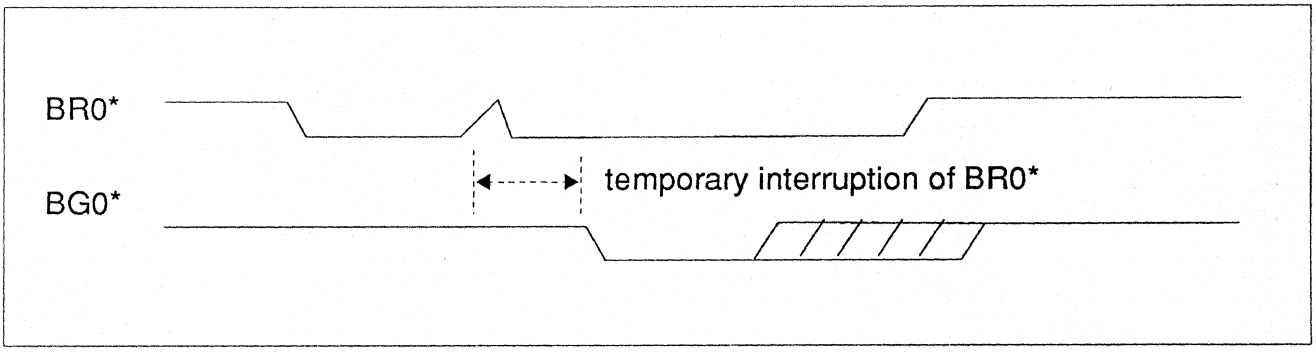
8.10 BR0 ABORTED

The "BR0 ABORTED" LED illuminates when bus request BR0* is prematurely aborted (rescinded) before BG0* or BBSY* occurs. To verify this error, the following signals must be viewed on the screen of a fast logic analyzer: BR0*, BG0* (at the slot where the VBAT is installed), BBSY* and the trigger output behind the BR0 ABORTED LED. The following figure illustrates normal operation, as well as the type of incorrect operation which would trigger the "BR0 ABORTED" error.



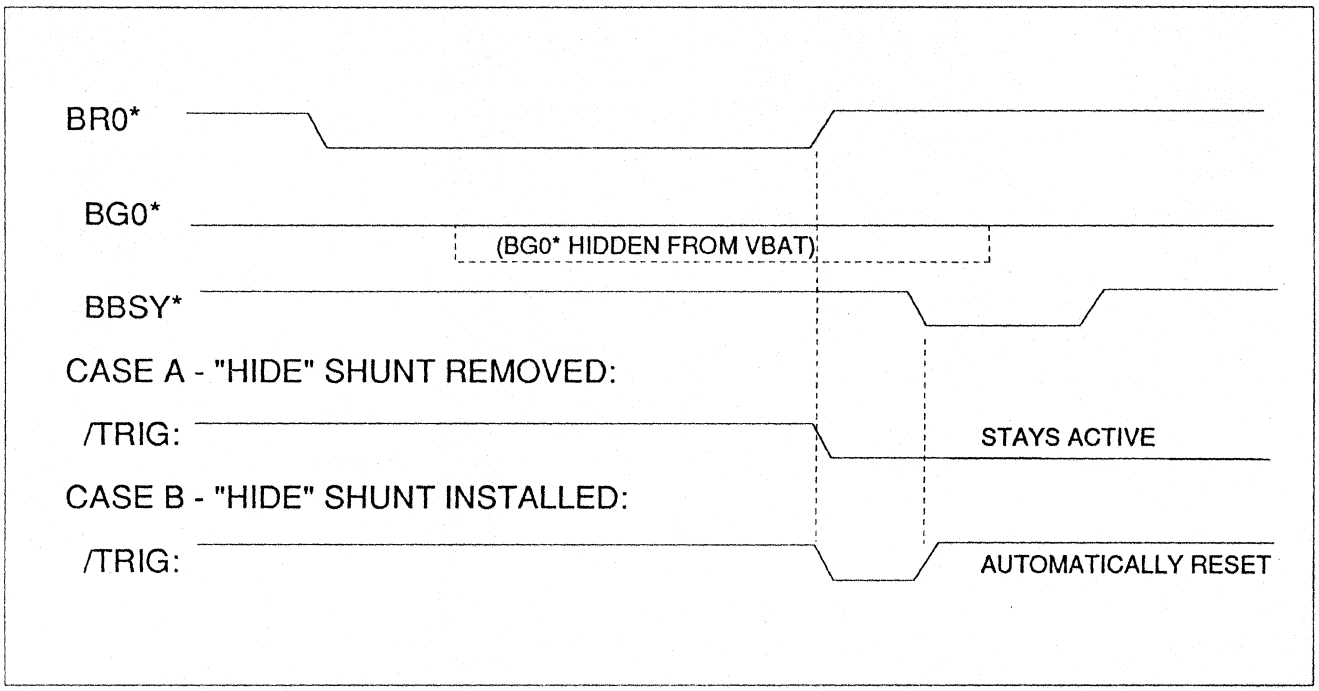
CONDITIONS WHICH COULD CAUSE THE ABOVE ERROR:

1) Design error in a bus requester, in which a request is made and then aborted.
2) Bus noise (usually due to ringing or ground bounce, here), in which a bus request is issued, and then noise causes it to momentarily go inactive (high) as show below:



CONDITION WHICH WOULD CAUSE A FALSE MOMENTARY ERROR INDICATON WHEN NONE IN FACT EXISTS:

1) The BG0* signal will not be visible to the VBAT if the VBAT is located to the right of a master which is taking over the bus and therefore does not pass a bus grant down the daisy chain. This will cause a momentary "false positive" indication of an error, as shown below:



To prevent the above temporary false indication, locate the VBAT in as leftwards a slot as possible in the backplane (without locating it before the arbiter, of course). In this way the bus grant signal will not be blocked by a master using the bus.

8.11 BR1 ABORTED

The "BR1 ABORTED" LED illuminates when Bus request BR1* is prematurely aborted (rescinded) before BG1* or BBSY* occurs. The operation of this trigger is the same as for "BR0 ABORTED" above, except that it pertains to BR1* instead of BR0*.

8.12 BR2 ABORTED

The "BR2 ABORTED" LED illuminates when Bus request BR2* is prematurely aborted (rescinded) before BG2* or BBSY* occurs. The operation of this trigger is the same as for "BR0 ABORTED", except that it pertains to BR2* instead of BR0*.

8.13 BR3 ABORTED

The "BR3 ABORTED" LED illuminates when Bus request BR3* is prematurely aborted (rescinded) before BG3* or BBSY* occurs. The operation of this trigger is the same as for "BR0 ABORTED", except that it pertains to BR3* instead of BR0*.

8.14 RULE2.1

The "RULE2.1" LED illuminates when either of the following illegal combinations occur:

DS1* = high, DS0* = low, A01 = high, LWORD* = low

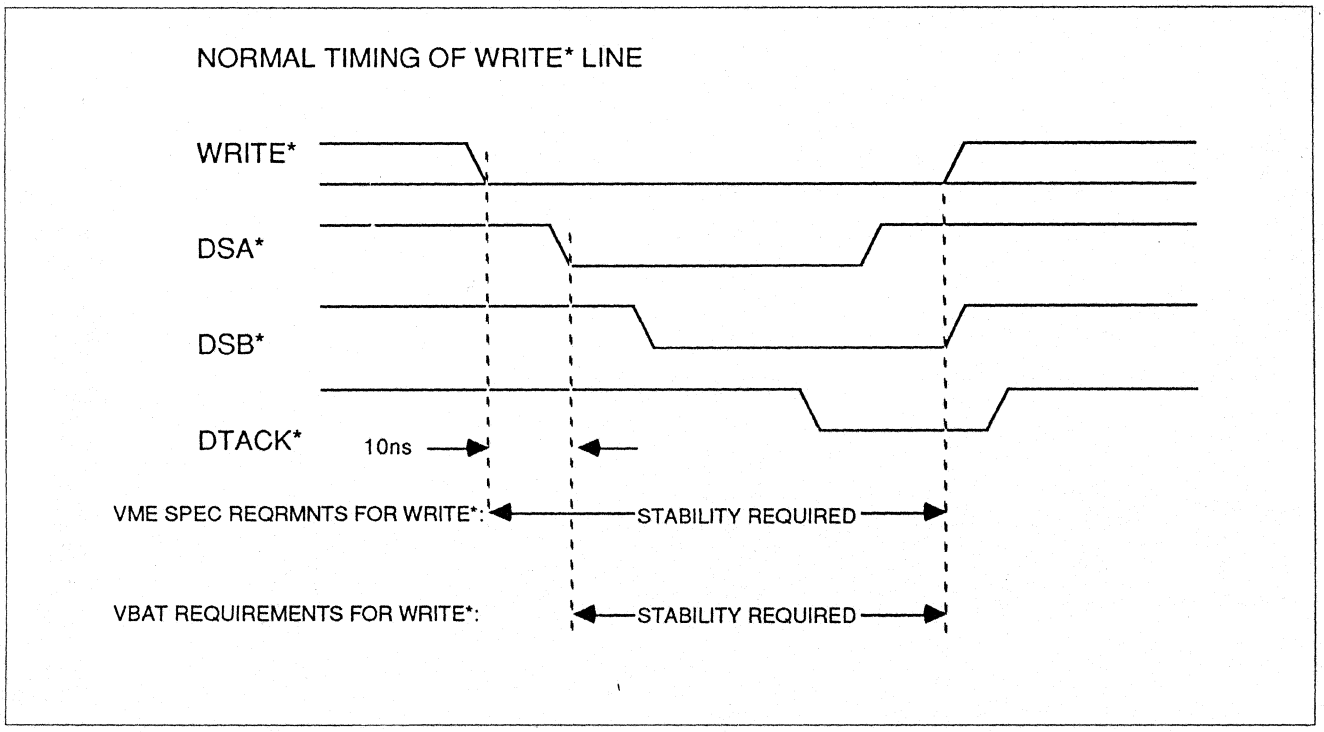
or ***DS1* = low, DS0* = high, A01 = high, LWORD* = low***

To verify this error, DS0*, DS1*, A01, LWORD*, DTACK* and the VBAT trigger output behind the RULE2.1 LED must be displayed on a fast logic analyzer.

8.15 WRITE UNSTBL

The "WRITE UNSTBL" LED illuminates when the WRITE* line is not stable (e.g. line changes state) during the entire time when data strobes DS0* and DS1* are active.

To verify this error, the following lines must be displayed, on a fast (>100 MHz) logic analyzer: WRITE*, DS0*, DS1*, DTACK* AND VBAT trigger output behind the "WRITE UNSTBL" LED.

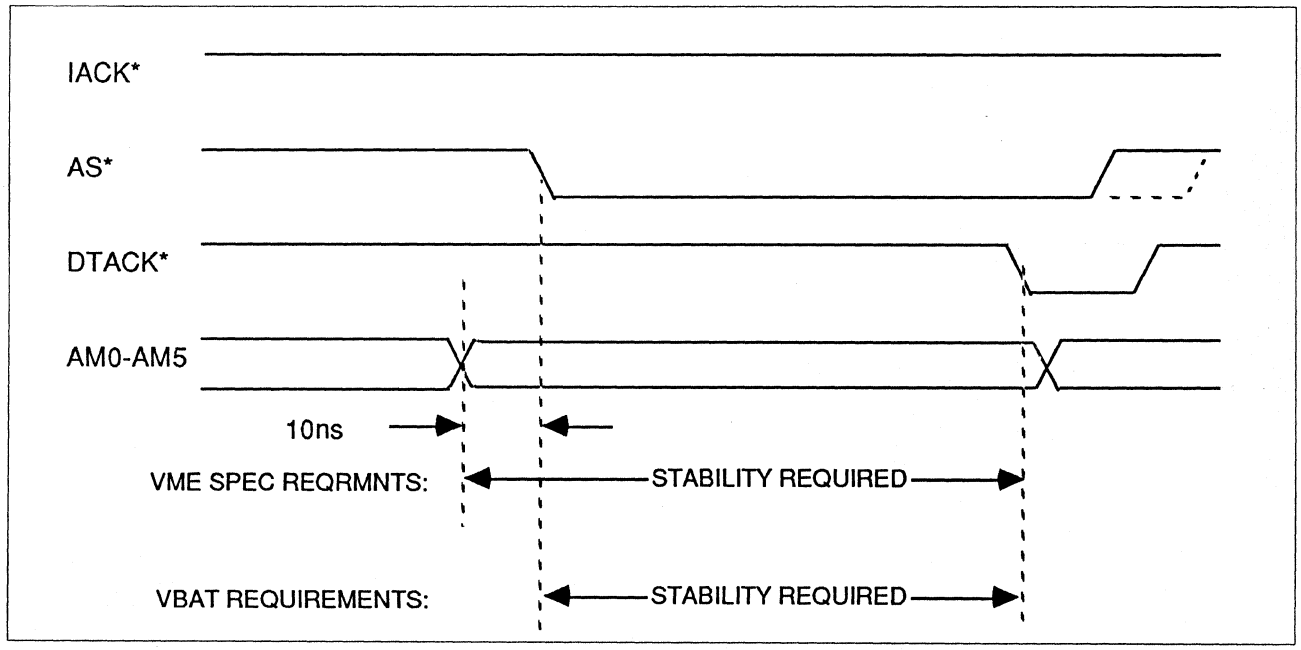


Note that DSA* and DSB* refer, respectively, to the first occurring and second occurring of data strobes DS0* and DS1*.

8.16 AM0-5 UNSTB

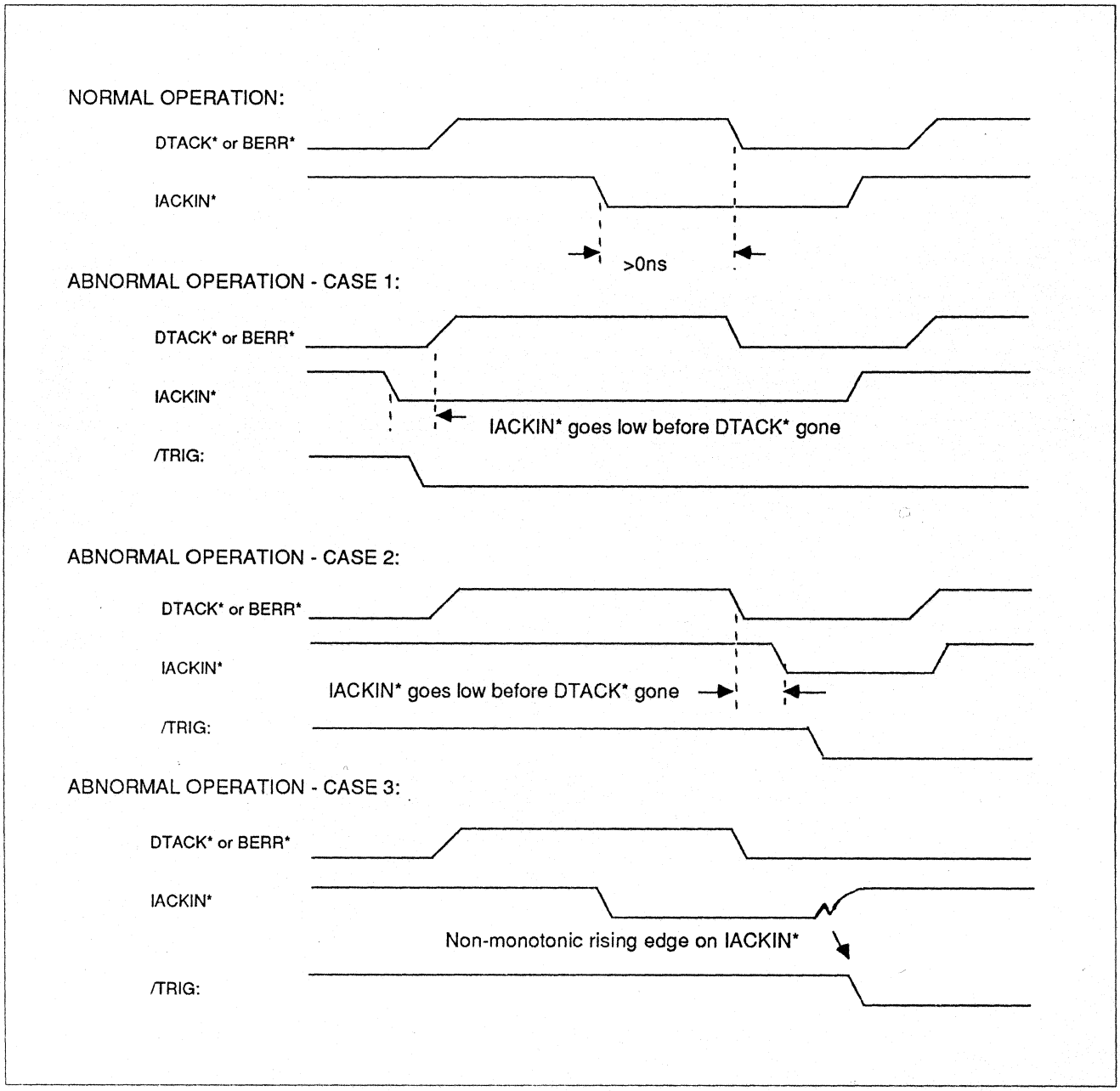
The "AM0-5 UNSTB" LED illuminates when a change is detected on address modifier lines AM0-AM5, or on line IACK during an interval where these lines should be stable. The conditions for stability are roughly the same as for "A1-7 UNSTB" except that the AM's are not checked when IACK* is active, since the address modifiers are not relevant during interrupt acknowledge cycle. To verify this error, the following signals must be displayed on the screen of a fast (>100 MHz) logic analyzer: AM0-AM5, AS*, DTACK*, IACK* and the trigger signal behind the AM0-5 UNSTB LED on the VBAT.

The following diagram illustrates the key signals present during a normal VME bus cycle, and points out the time period during which address modifier lines AM0-AM5 are required to be stable.



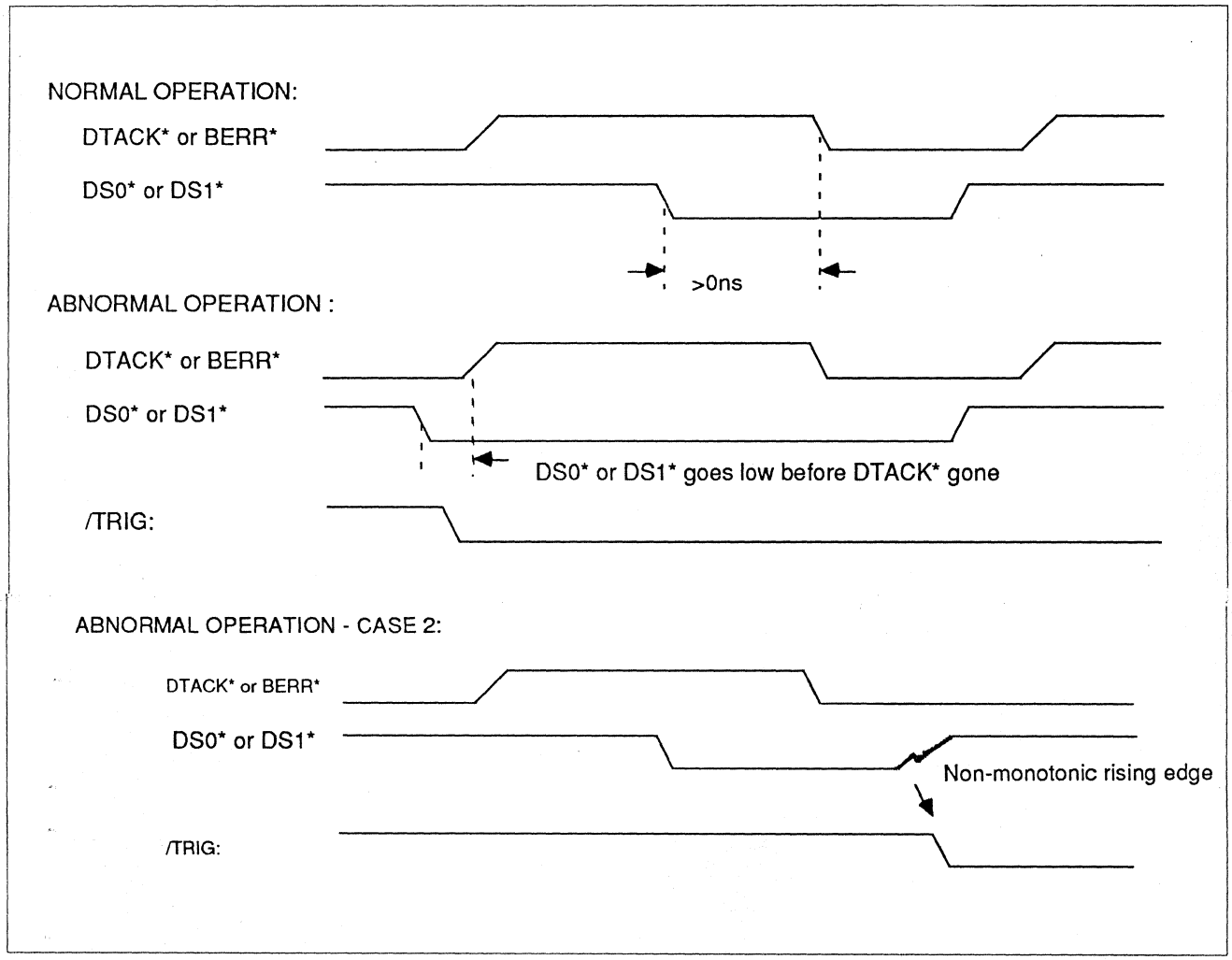
8.17 RULE 4.45

The "RULE4.45" LED illuminates when IACKIN* goes low before DTACK* and BERR* have gone high (been rescinded after the previous cycle), or if IACKIN* goes low after DTACK is driven low during the present cycle. To verify this error, it is necessary for the logic analyzer to display DTACK*, BERR*, AS*, IACKIN* (at the slot the VBAT is installed in) and the "RULE4.45" trigger output on the VBAT. The following diagram illustrates normal operation, as well as conditions which would trigger an error.



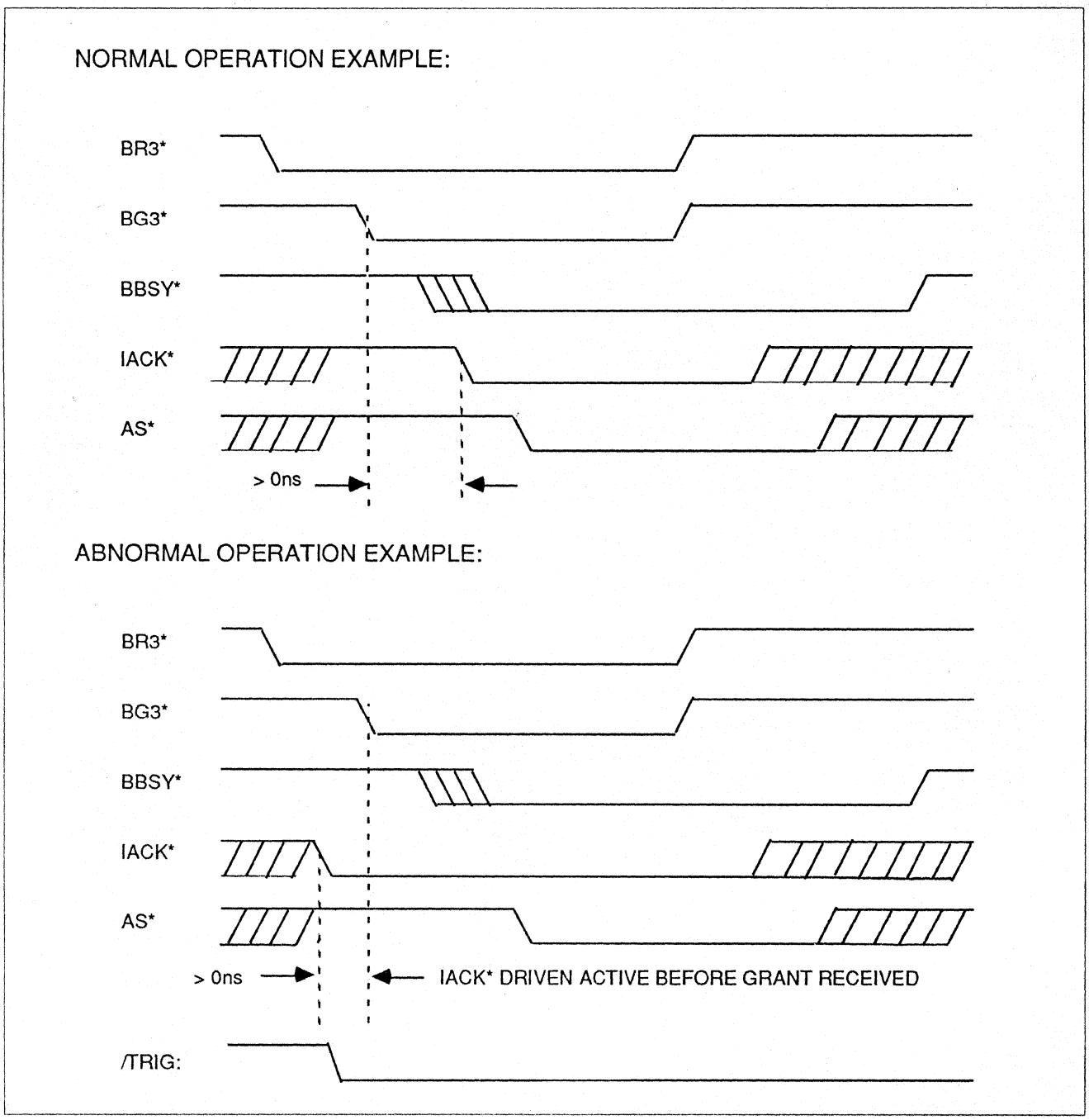
8.18 RULE 2.35

The "RULE2.35" LED illuminates when DS0* or DS1* are driven low before DTACK* and BERR* have gone high (been rescinded after the previous cycle). To verify this violation, the following signals must be displayed on a fast (> 100 MHz) logic analyzer: DS0*, DS1*, DTACK*, BERR*, and the VBAT trigger output behind the "RULE2.35" LED. The following diagram illustrates normal operation, as well as a condition which would trigger an error.



8.19 RULE 2.28-IACK

The "RULE2.28-IACK" LED illuminates when IACK* is driven low before the bus has been properly granted to the master. No master is permitted to drive the IACK* line (as well as others dealt with below) until it receives the appropriate bus grant, or unless BBSY* is already active. To verify this violation, the following signals must be displayed on a very fast (preferably 200 MHz) logic analyzer: BG0*-BG3*, BBSY*, IACK*, AS*, and the "RULE2.28-IACK" trigger from the VBAT. Conditions for normal and abnormal operation are shown below:



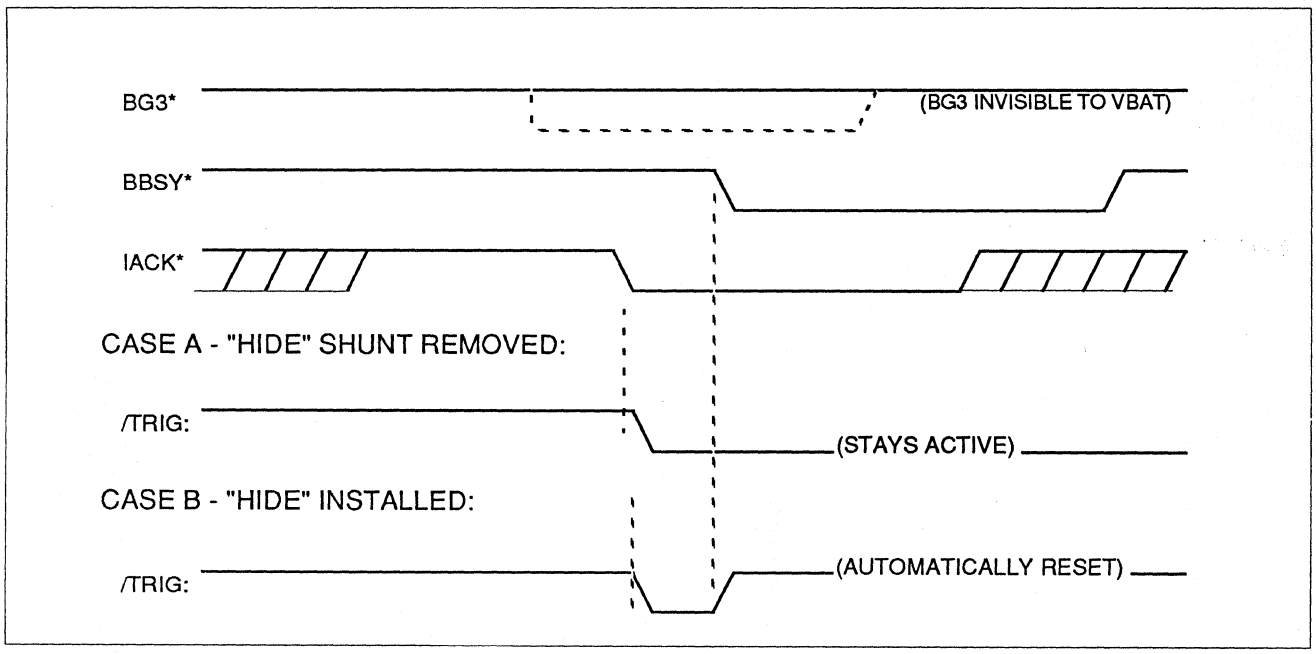
CONDITIONS WHICH COULD CAUSE THE ABOVE ERROR:

1) Design error in which a bus master takes over the bus before it receives a valid bus grant, or takes over the bus momentarily after it has just relinquished it.
2) Design error in arbitor or upstream master, in which a bus grant is given to the "violating" board, and then is rescinded.

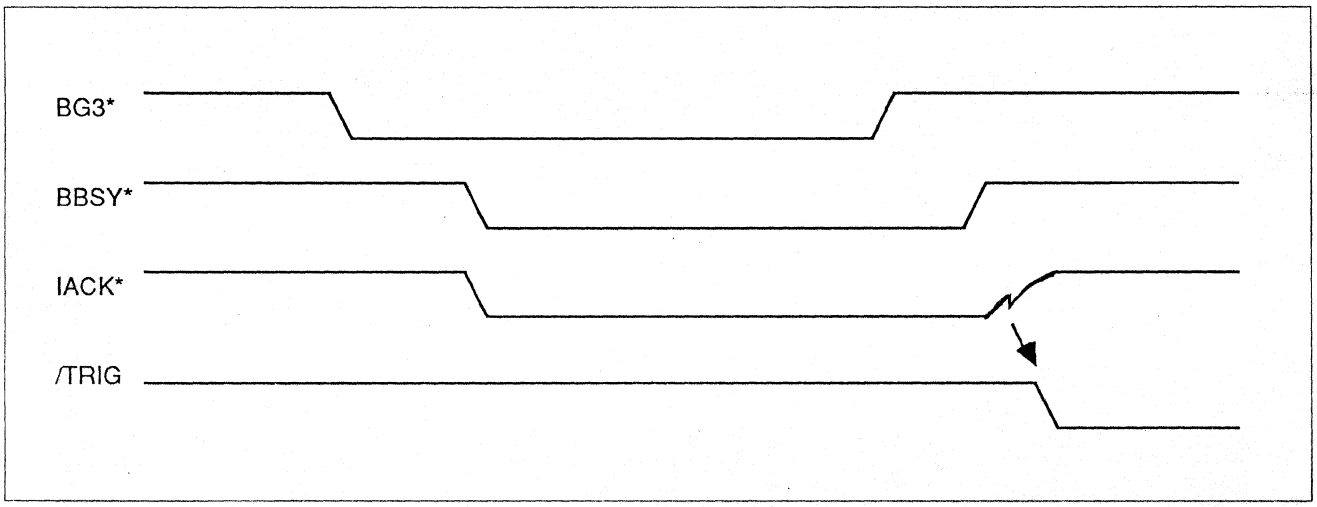
CONDITION WHICH WOULD CAUSE A FALSE ERROR WHEN NONE EXISTS:

1) The BG3* signal will not be visible to the VBAT if the VBAT is located to the right of a a master which is taking over the bus and therefore does not pass a bus grant down the daisy chain. This will cause a momentary "false positive" error indication, as shown below. In this case, the YELLOW "GRANT HDDN" LED will also light.

   To prevent the above false indication, locate the VBAT in as leftwards a slot as possible in the backplane. In this way the bus grant signal will not be blocked by a master using the bus.

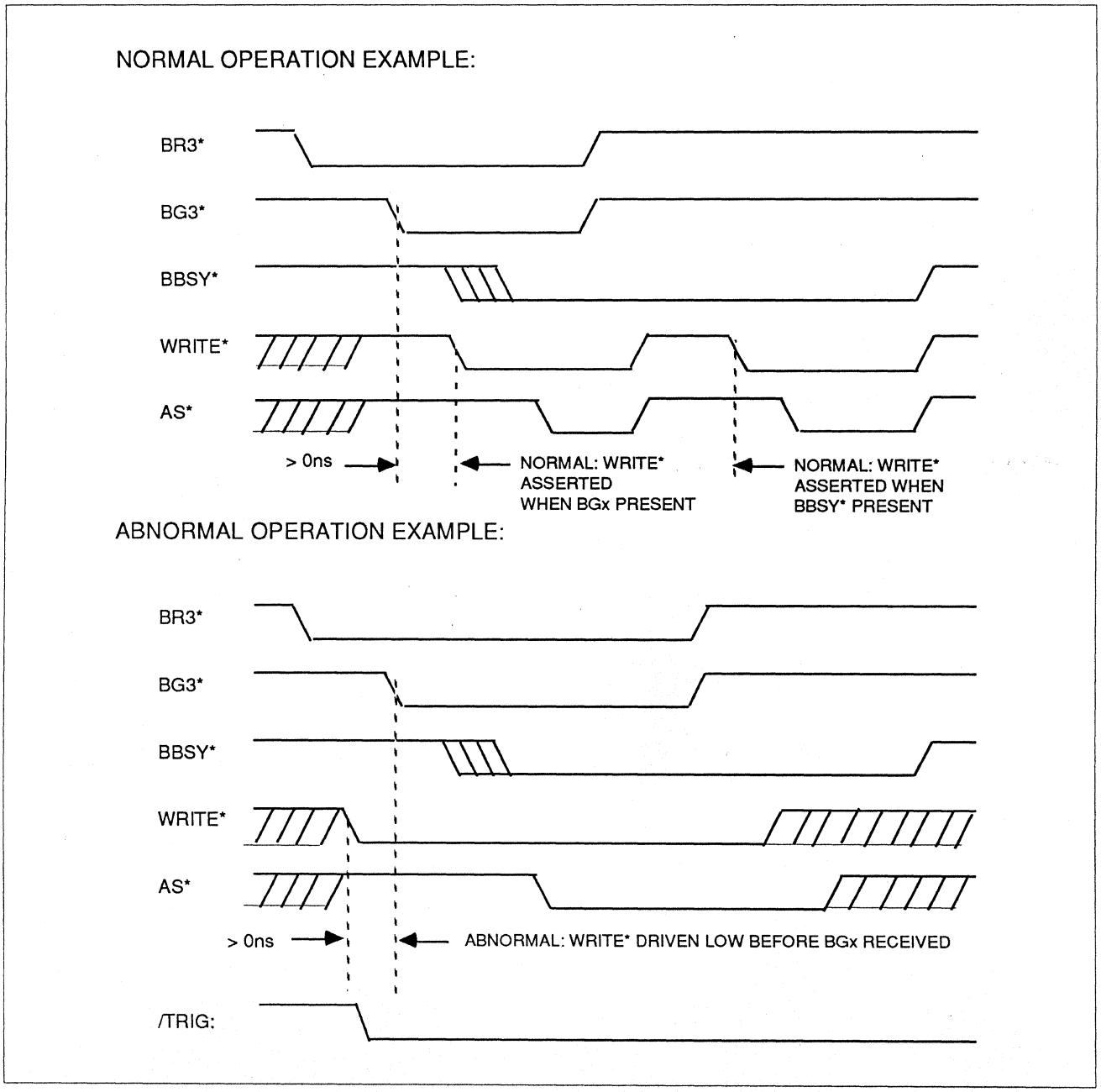


2) Severe noise during slow deassertion of IACK*, as illustrated below:



8.20 RULE 2.28-WRT

This LED illuminates when WRITE* has been driven low before the bus has been properly granted to the master. No master is permitted to drive the WRITE* line (as well as others dealt with below) until it receives the appropriate bus grant, or unless BBSY* is already active. Conditions for normal and abnormal operation are shown below. To verify this violation, the following signals must be displayed on a very fast (preferably 200 MHz) logic analyzer: BG0*-BG3* (at the VME slot where the VBAT is installed), BBSY*, WRITE*, AS*, DTACK* and the VBAT trigger behind the "RULE2.28-WRT" LED.



CONDITIONS WHICH COULD CAUSE THE ABOVE ERROR:

Same as for RULE 2.28-IACK above.

CONDITION WHICH WOULD CAUSE A FALSE ERROR, WHEN NO ERROR EXISTS:

Same as for RULE2.28-IACK above.

8.21 RULE 2.28-LWD

This LED illuminates when LWORD* has been driven low before the bus has been properly granted to the master. Operation is essentially the same as for "RULE2.28-WRT", above, except that LWORD* should be substituted for WRITE* in all of the diagrams above.

8.22 RULE 2.28-DS

This LED illuminates when DS0* or DS1* have been driven low before the bus has been properly granted to the master. Operation essentially the same as for "RULE2.28-WRT"" above, except that DS0* or DS1* should be substituted for WRITE* in all of the diagrams above.

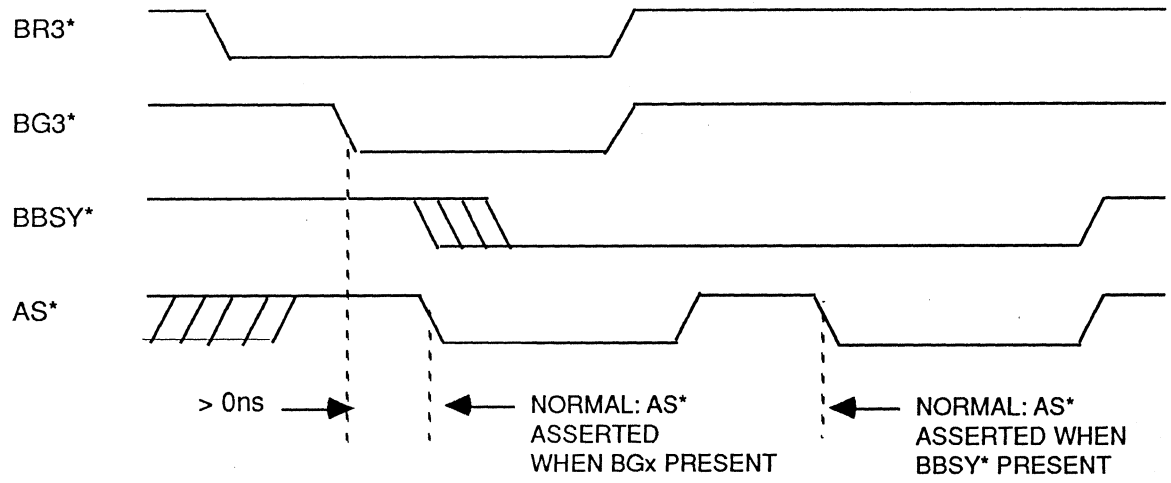
8.23 RULE 2.20

This LED illuminates when AS* has been driven low before the bus has been properly granted to the master. Operation is very similar to that for "RULE2.28-WRT", except that AS* should be substituted for WRITE*, as illustrated below.

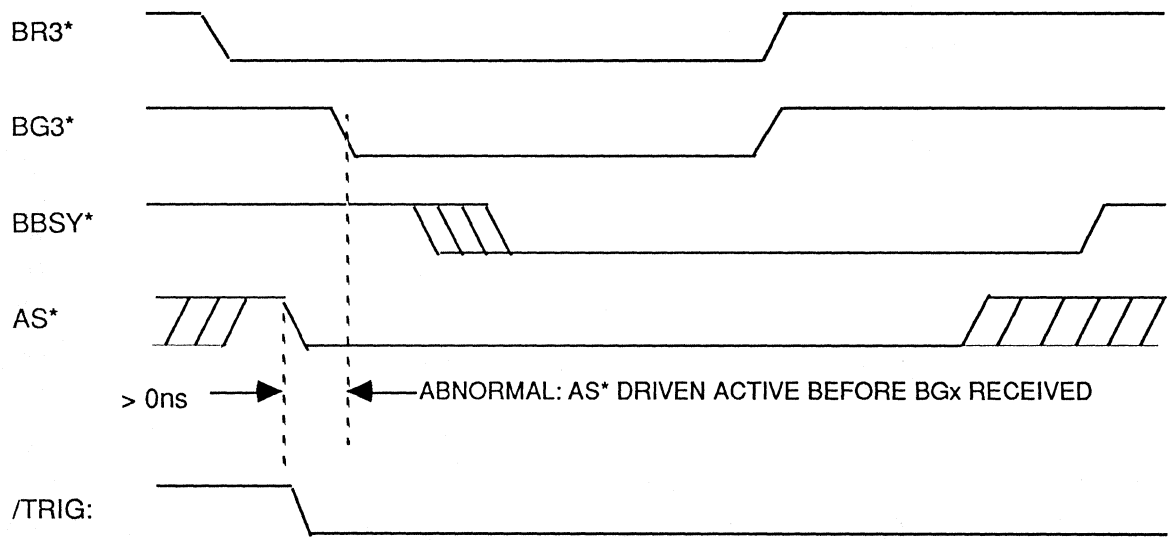
```
NOTE: In addition to its normal function (see next page), the
   RULE2.20 trigger can often detect NON-MONOTONIC rising (ending)
   edges of AS*.  Such behavior is usually the result of a slow-
   rising AS* waveform which dwells near the threshold region for a
   long time, making it susceptible to multiple transitions through
   the receiver's threshold due to any coupled noise.  Slow rise time
   is often caused by excessive bus capacitance due to boards having
   p.c. traces that are much longer than the specified 2 inches.

   Such noise on AS* is potentially serious since during overlapped
   arbitration, a new master often counts on seeing a well-defined
   ending edge on AS* from the previous master as its signal that
   the new master may begin driving the bus.  Also, many slaves
   capture the addressing information on the falling edge of AS*.  A
   non-monotonic rising edge could appear as a momentary re-asser-
   tion (falling edge) of AS*.  Therefore, this alternate activator
   of the RULE2.20 trigger should be investigated carefully.
```


NORMAL OPERATION EXAMPLE:



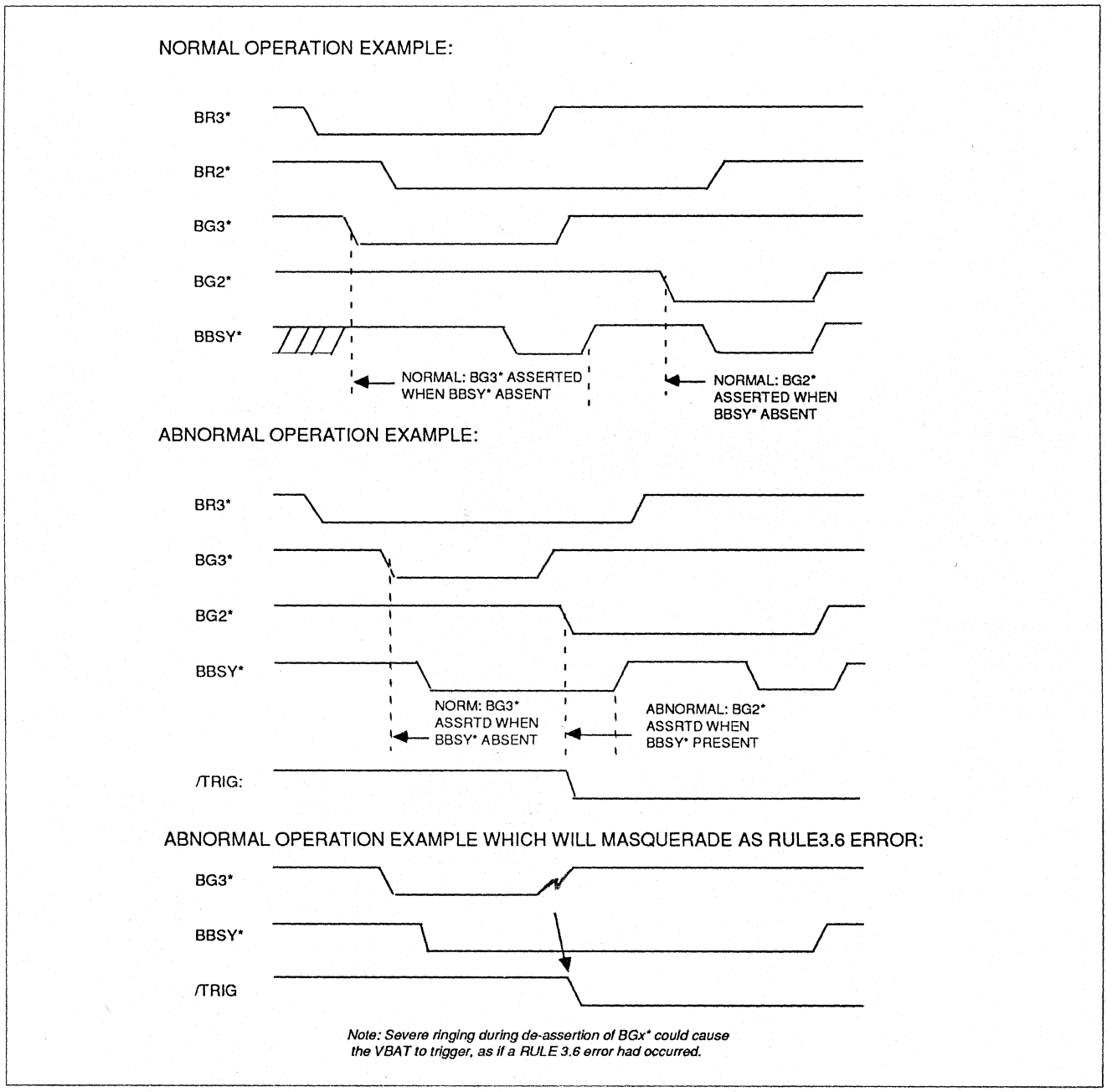
ABNORMAL OPERATION EXAMPLE:



8.24 RULE 3.6

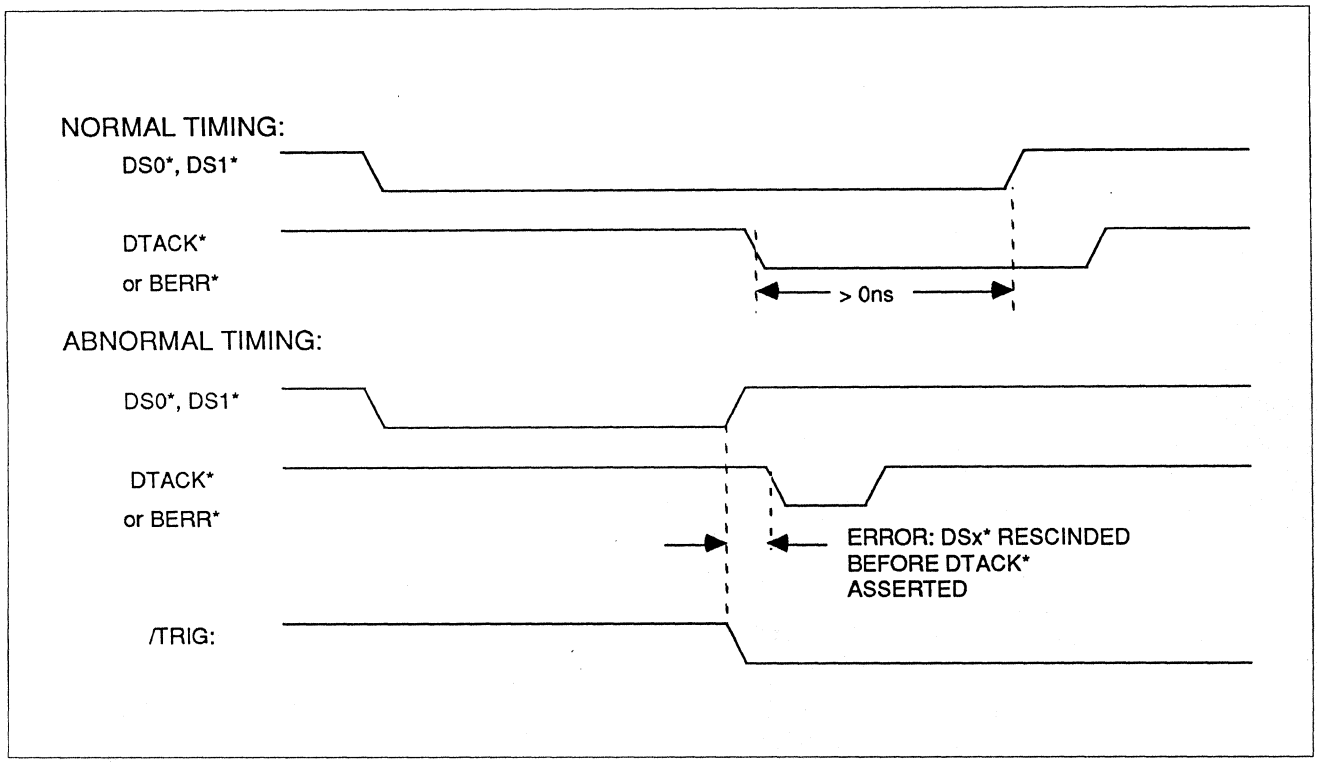
This LED illuminates when the bus is granted to a new master (BGx goes active) before BBSY* goes away. A new bus grant BGx is prohibited from being issued until BBSY* from the previous master goes away, as illustrated below. To verify this error, a logic analyzer must be set up to display BG0*-BG3*, BBSY* and the VBAT's "RULE3.6" trigger.

The RULE3.6 error will not be visible to the VBAT if the VBAT is located downstream of (to the right of) a master which is taking over the bus and therefore does not pass a bus grant down the daisy chain.



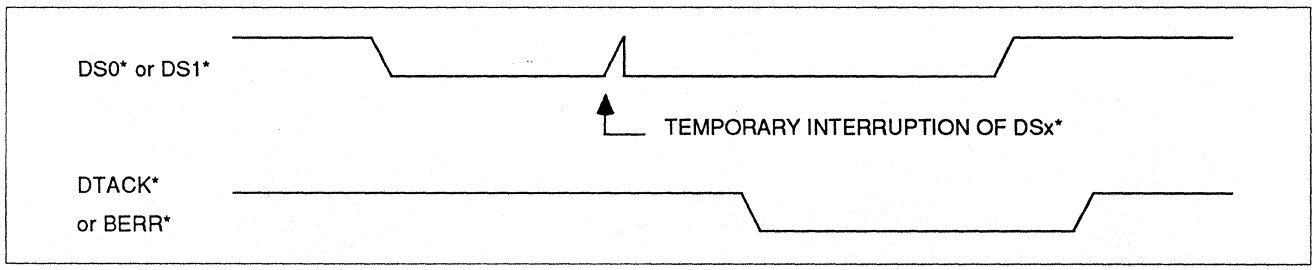
8.25 RULE 2.17

This LED illuminates when DS0* or DS1* is rescinded before DTACK* or BERR* is received. The correct interlocked timing relationship between the data strobes and DTACK*/BERR* is illustrated below, along with an example of a condition which would cause an error. To verify this error, a fast (200 MHz preferably) logic analyzer must be set up to display DS0*, DS1*, DTACK*, BERR* and the VBAT's "RULE2.17" trigger output.



CONDITIONS WHICH COULD CAUSE THE ABOVE ERROR

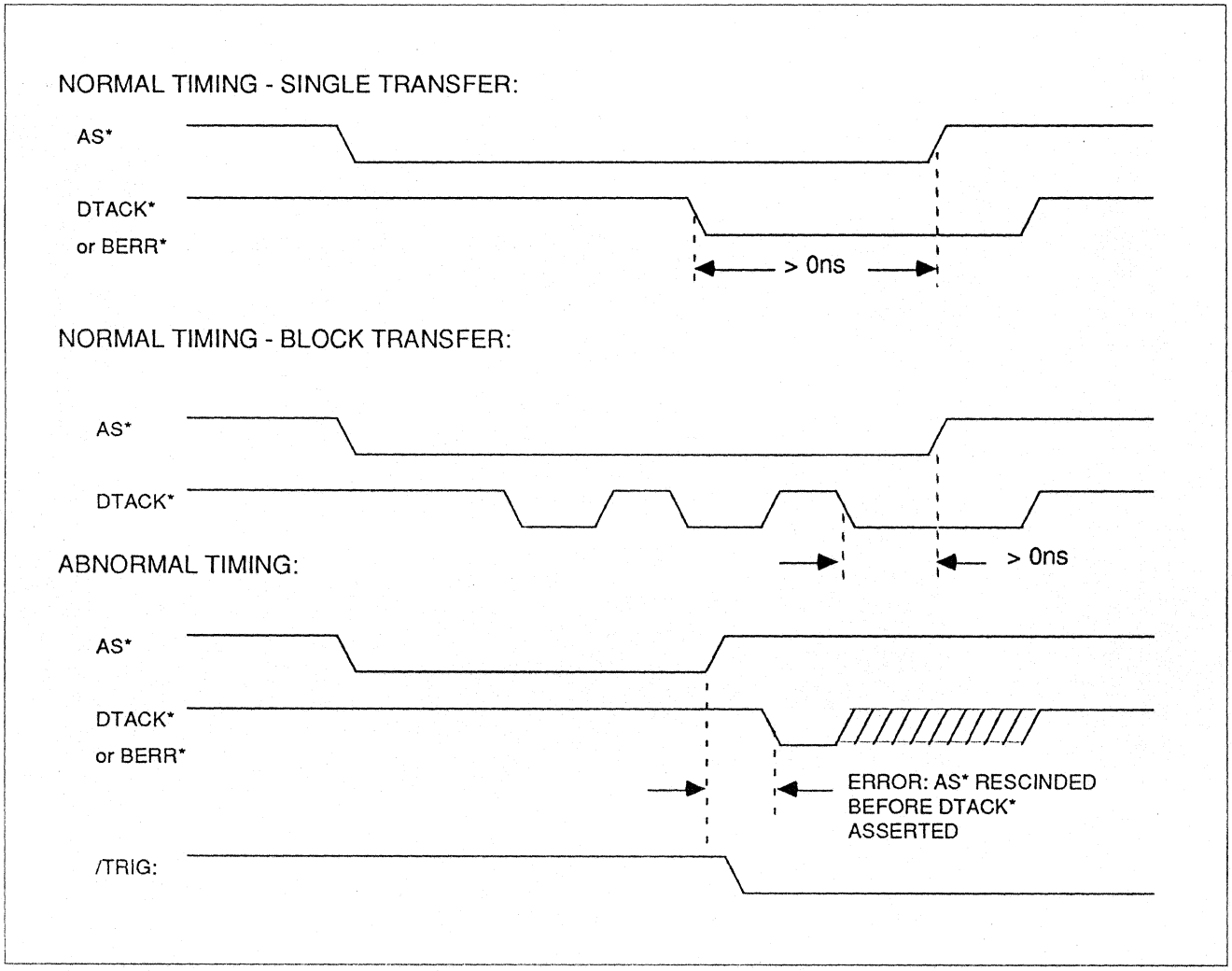
1) Design error in a bus master, in which one or both data strobes are rescinded before DTACK* is received.
2) Bus noise (usually due to ringing or ground bounce, here), in which a data strobe is asserted, and then noise causes it to momentarily go inactive (high) as shown below:



8.26 RULE 2.44

This LED illuminates when AS* is rescinded before the last falling edge on DTACK* or BERR* occurs. A bus master must hold AS* low until it detects the last falling edge on DTACK* or BERR*. To verify this error, a very fast (preferably 200+ MHz) logic analyzer should be set up to display AS*, DTACK*, BERR*, DS0*, DS1*, and the VBAT's "RULE2.44" trigger output.

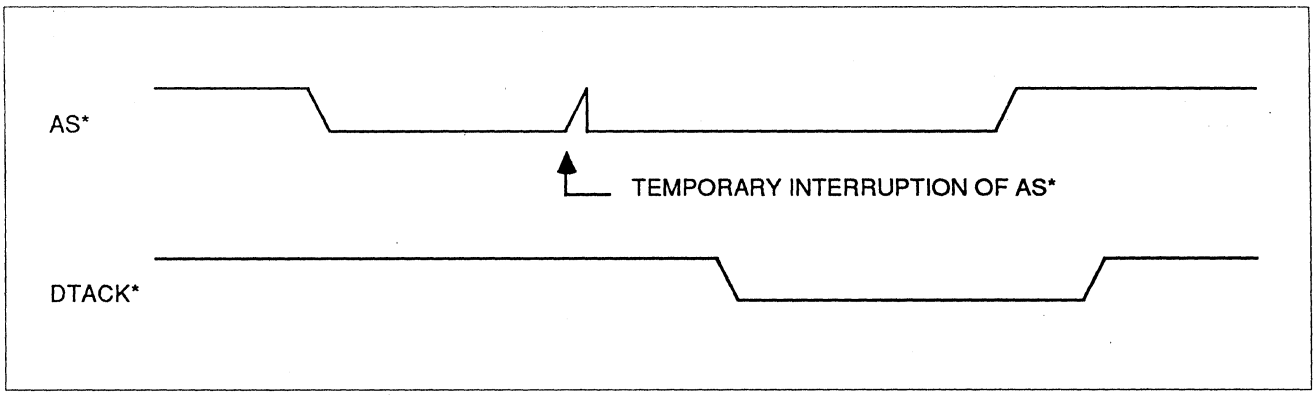
The correct interlocked timing relationship between address strobe AS* and DTACK*/BERR* is illustrated below, along with an example of condition which would cause an error.



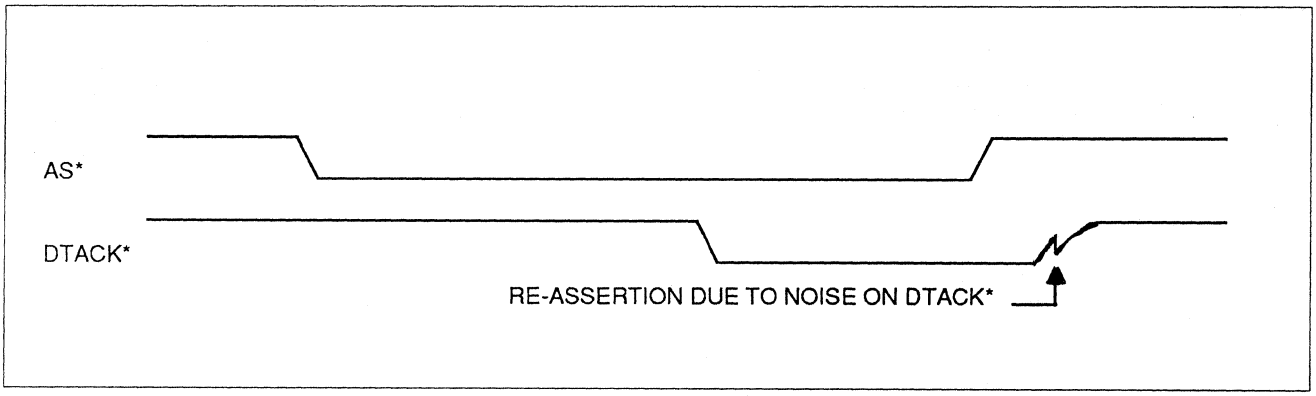
CONDITIONS WHICH COULD CAUSE THE ABOVE ERROR:

1) Design error in a bus master, in which AS* is rescinded before DTACK* is received.

2) Bus noise (usually due to ringing or ground bounce, here), in which AS* is asserted, and then noise causes it to momentarily go inactive (high) as shown below:

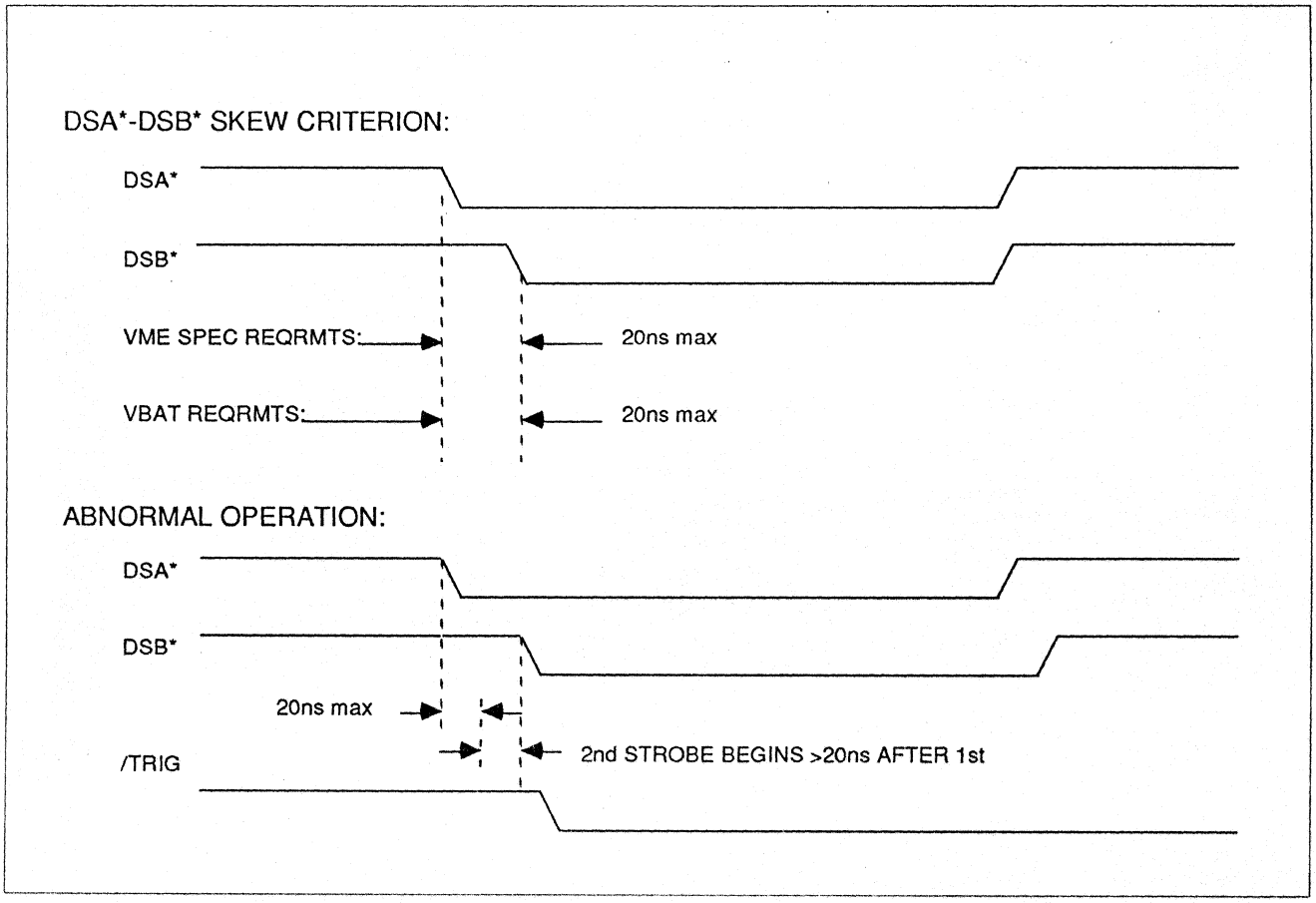


3) Bus noise (usually due to ringing or ground bounce, here), in which DTACK* is asserted, then rescinded, and noise causes it to momentarily go active (low) again as shown below. This situation is common, due to the slow and gradual de-assertion of DTACK*, which is normally an open collector output.



8.27 RULE 2.39

This LED illuminates when, during cycles where both data strobes are driven low, there is excessive skew (>20 ns) between the starting edges of the first and second strobes. This situation is illustrated below. To verify this error, a very fast (preferably 200+ MHz) logic analyzer should be set up to display DS0*, DS1*, DTACK* and the VBAT's "RULE2.39" trigger output.



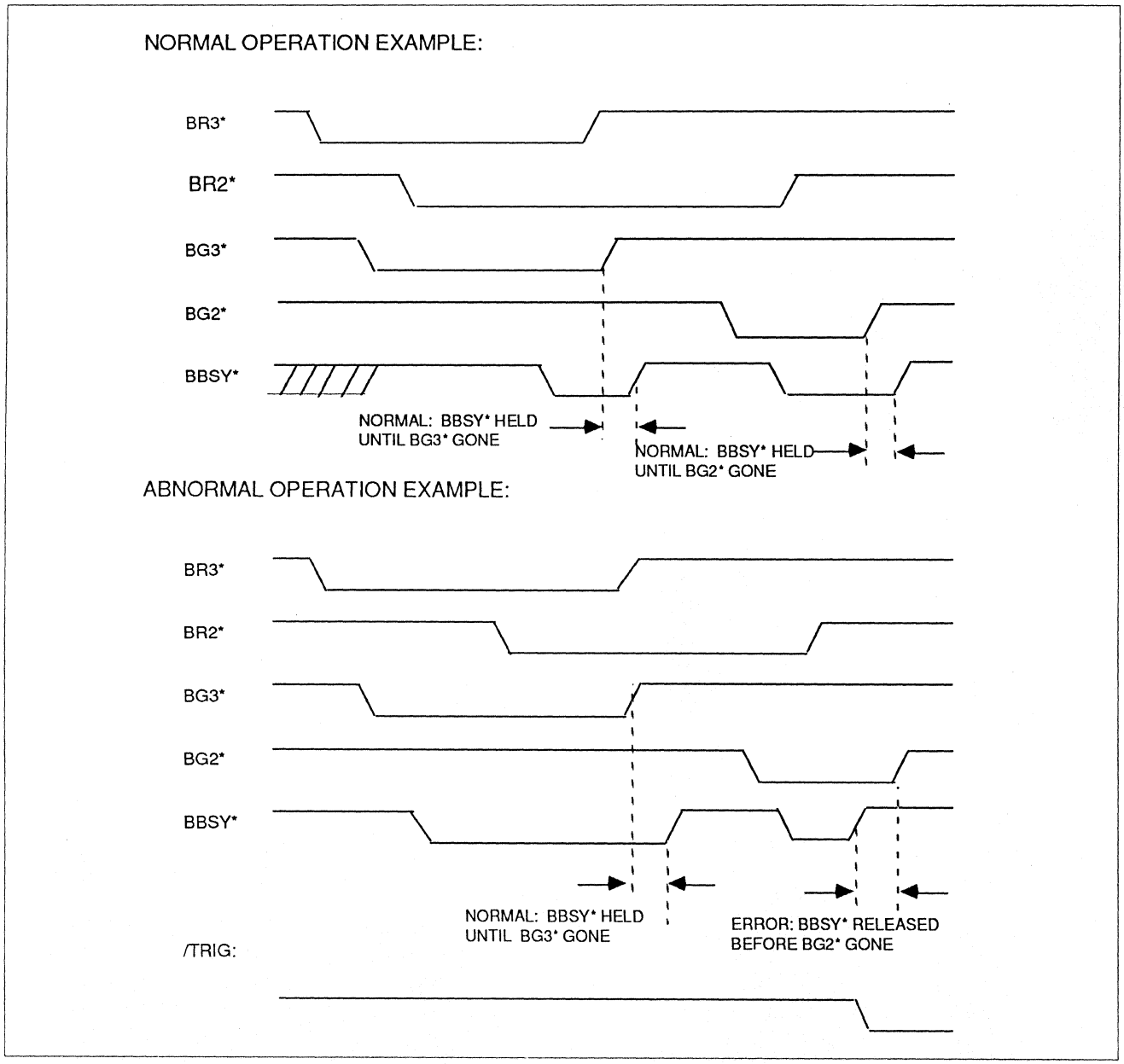
NOTE: In addition to its normal function, the "RULE2.39" trigger can often detect NON-MONOTONIC rising (ending) edges of DS0* or DS1*. Such behavior is usually the result of a slow-rising DS0* or DS1* waveform which dwells near the threshold region for a long time, making it susceptible to multiple transitions through the receiver's threshold due to any coupled noise. Slow rise time is often caused by excessive bus capacitance due to boards having p.c. traces for DS0* and DS1* that are much longer than the specified 2 inches.

Such noise is potentially serious since some slaves use the ending edges of DS0* or DS1* for incrementing counters, etc. Multiple edges could cause trouble in that, and other, cases. Therefore, this alternate activator of the RULE2.39 trigger should be investigated carefully.

8.28 RULE 3.10

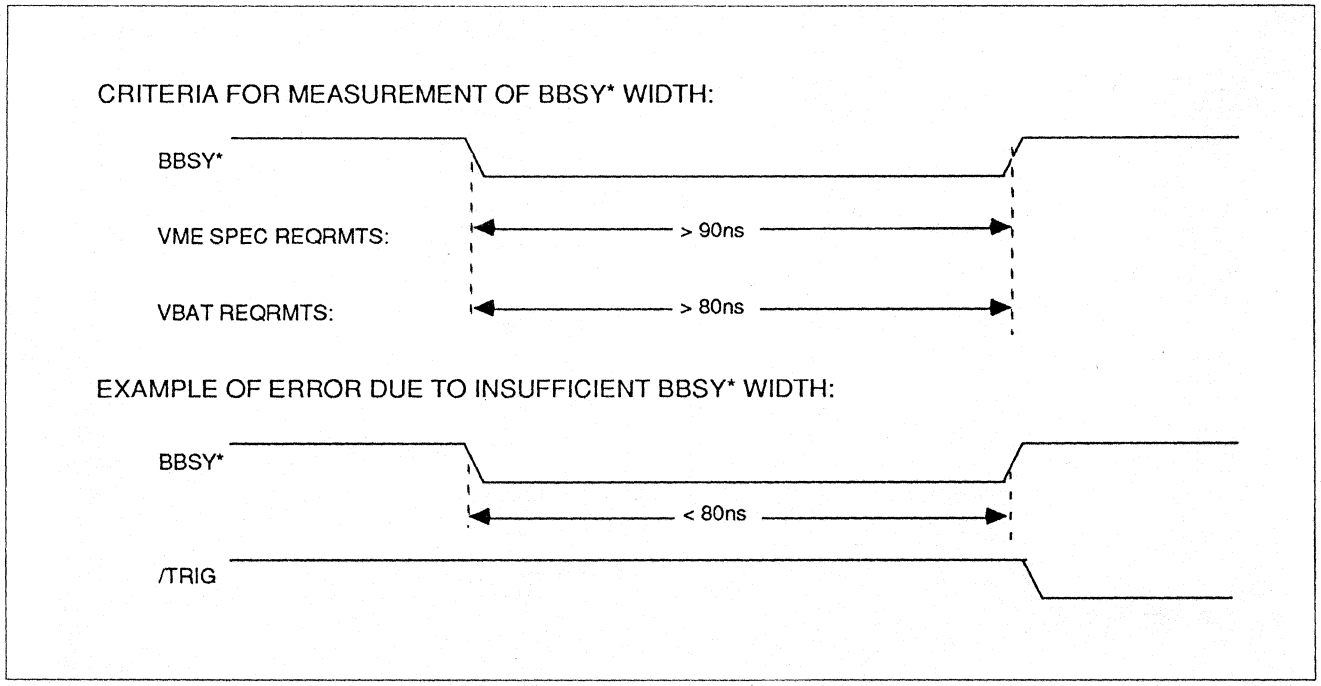
This LED illuminates when a requester rescinds BBSY* before the bus grant goes high. The VME specification requires that BBSY* be held active until the bus grant which originally led to BBSY* is rescinded, as illustrated below. To verify this error, a fast logic analyzer should be set up to display BG0* through BG3* (at the VBAT's slot), BBSY* and the VBAT's "RULE3.10" trigger output.

This error will not be detectable if the VBAT is located to the right of a master which is taking over the bus and therefore does not pass a bus grant down the daisy chain.



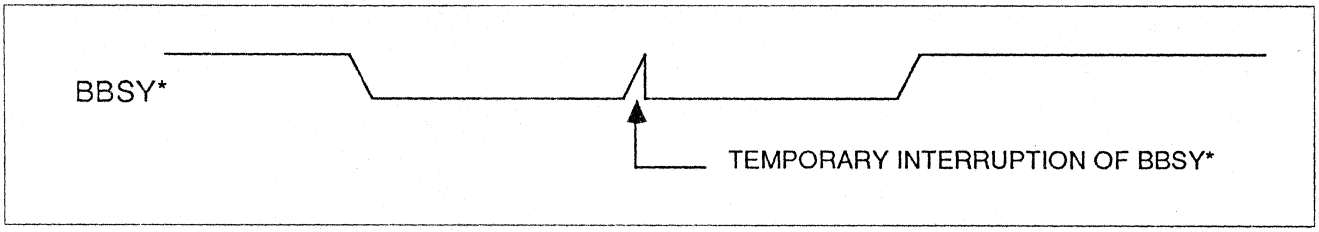
8.29 RULE 3.7

This LED illuminates when BBSY* is active for too short a time (less than 90 ns). To verify this error, a very fast (preferably 200+ MHz) logic analyzer should be set up to display BBSY* and the VBAT's trigger output behind the "RULE3.7" LED.

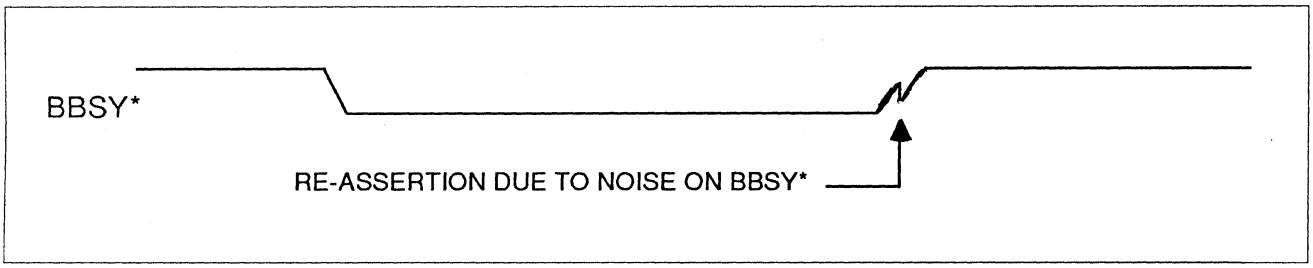


CONDITIONS WHICH COULD CAUSE THE ABOVE ERROR:

1) Design error in an "overlapped arbitration" bus master, in which BBSY* is rescinded immediately after AS* is asserted, without giving due consideration to ensuring that BBSY has been held active for long enough.
2) Bus noise (usually due to cross-talk from the nearby data lines D0-D15, or the ringing or ground bounce, here), in which BBSY* is asserted, and then noise causes it to momentarily go inactive (high) as shown below:

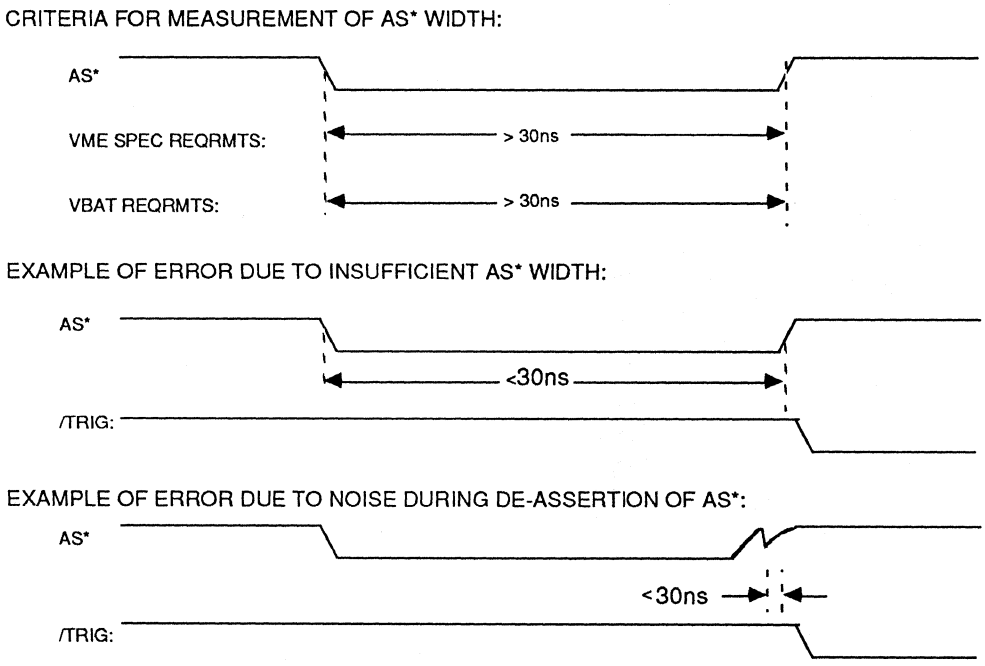


3) Bus noise (usually due to ground bounce, aggravated by the slow rise time of this open-collector line), in which BBSY* is asserted, then rescinded, and noise causes it to momentarily go active (low) again as show below. This situation is common, due to the slow and gradual de-assertion of BBSY*, due to the fact that BBSY* is normally an open collector output.



8.30 RULE 2.45

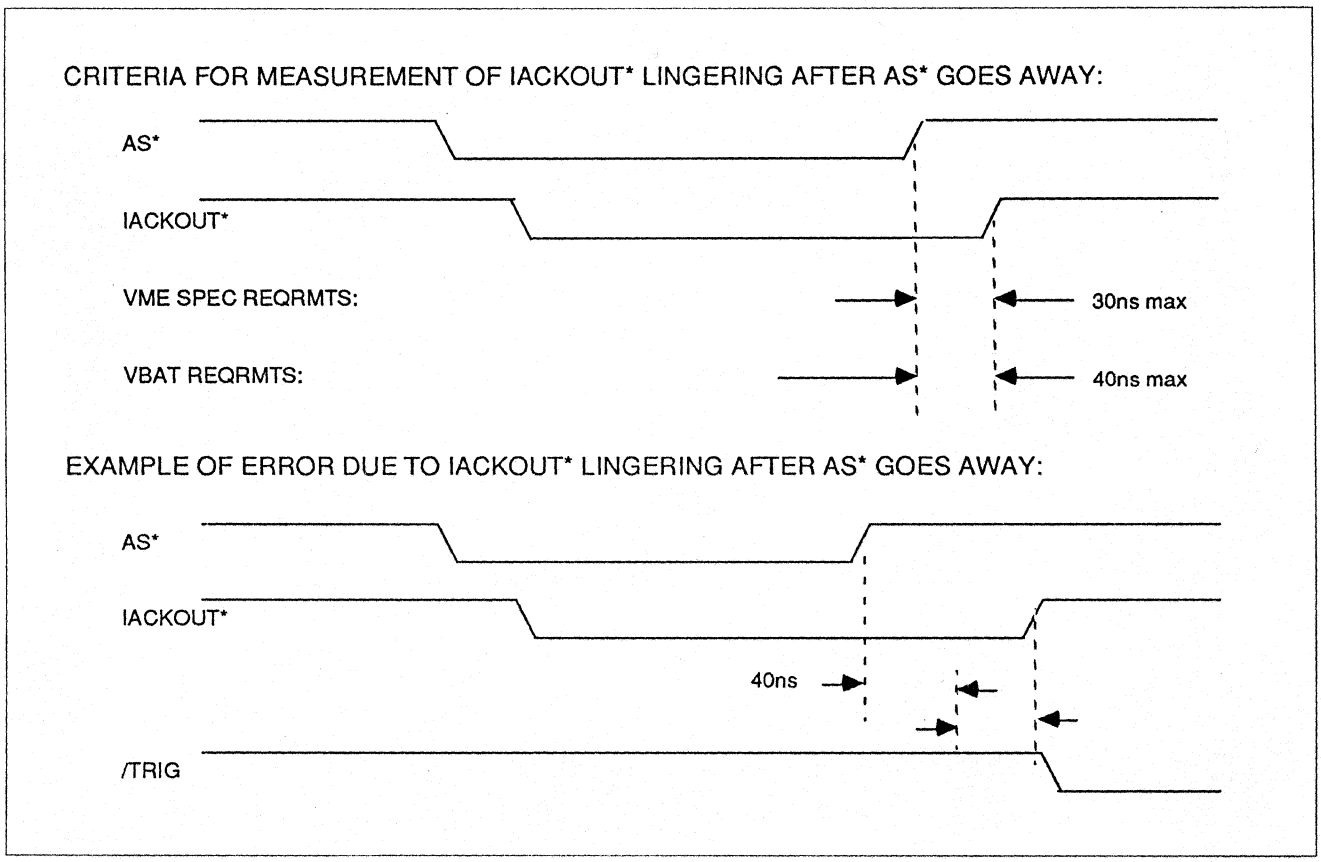
This LED illuminates when AS* is active for too short a time (less than 30 ns). To verify this error, a very fast (preferably 200-500 MHz) logic analyzer should be set up to display AS*, DTACK* and the VBAT's trigger output (behind the RULE2.45 LED).



Note: This error is generally caused by very slow de-assertion of AS. It will generally not cause system problems if all boards in the VME system use receivers with hysteresis (such as 74LS244's). If such receivers are not used, then serious problems can result. This problem is difficult to see using a logic analyzer, and therefore should be studied with a fast (250-400 Mhz oscilloscope).*

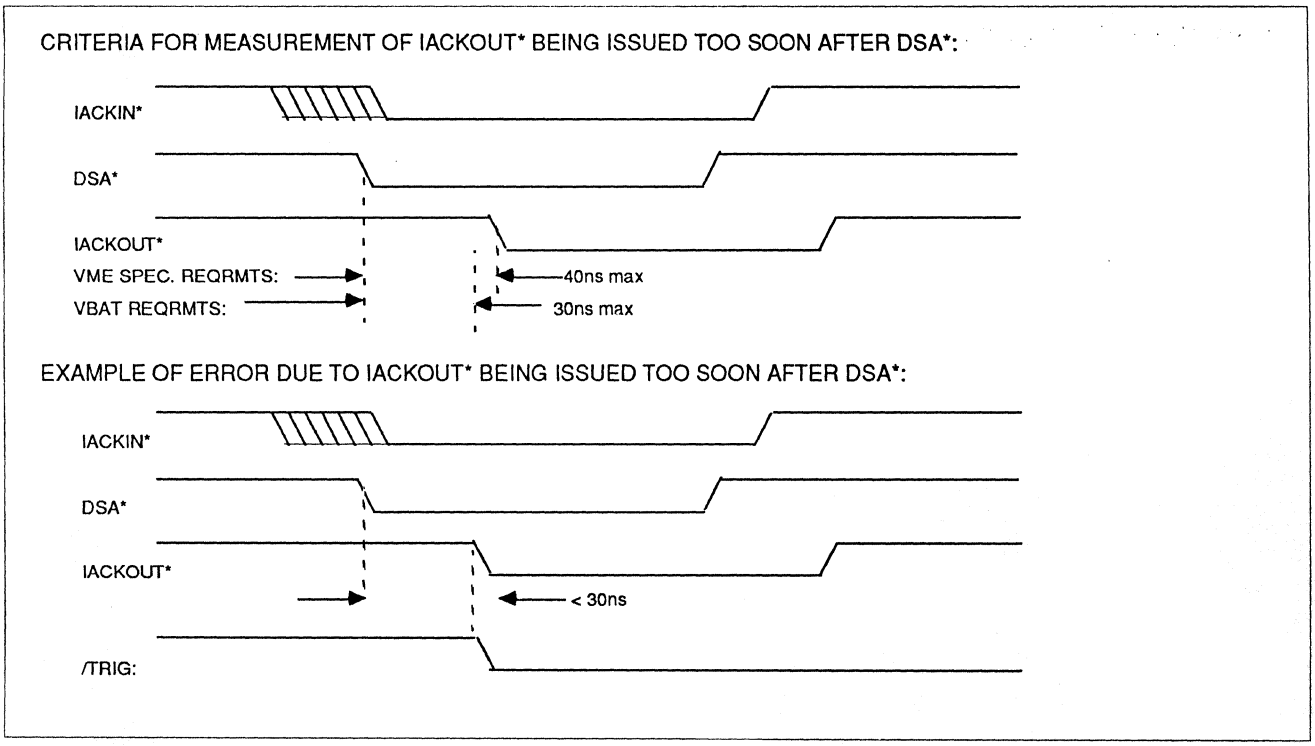
8.31 RULE 4.41

This LED illuminates when, at the end of an interrupt acknowledge cycle, the IACKOUT* line of a master was not driven high within 40 ns after AS* was driven high. The VBAT is only capable of detecting errors in boards which are located to the left of (upstream of) the VBAT. This is because IACKOUT* is a daisy-chain line. To verify this error, a fast (>100 MHz) logic analyzer should be set up to display AS*, IACK*, IACKOUT* (at the VBAT's VMEbus slot), and the VBAT's "RULE4.41" trigger output.



8.32 RULE 4.46

This LED illuminates when the IACKOUT* line of the board to the left of the VBAT is driven low less than 30 ns after the falling edge on AS*, when the IACKIN* is low when the IACK DAISY-CHAIN DRIVER detects a falling edge on DSA*. To verify this error, a fast (>100 MHz) logic analyzer should be set up to display AS*, DS0*, DS1*, IACKIN* and IACKOUT* at the board to the left of the VBAT, and the VBAT's "RULE 4.46" trigger output.



CONDITIONS WHICH COULD CAUSE ABOVE ERROR:

1) Design error in which IACKOUT* is issued by an interrupter in direct response to IACKIN* without qualifying the output with AS* and DS*, and without providing enough delay for metastable settling. THIS ERROR IS MADE VERY FREQUENTLY, since this rule was not spelled out in early VME specification revisions.

CONDITION WHICH WOULD CAUSE A FALSE ERROR, WHEN NO ERROR ACTUALLY EXISTS:

2) The VBAT is used in slot 1, or any slot to the left of where the first interrupter in the system is located. Since IACKIN* is derived from IACK* at slot 1, it will NECESSARILY violate this rule. For this reason, this error should be checked out, and then IGNORED if the above case is true.

8.33 NEG 12V ON

This NON-ERROR (green) LED is illuminated when -12 Volt power exists on the bus. The -12 volt power is merely checked for existence, not for accuracy. This is not an error condition. If the LED fails to illuminate, the -12 Volt power has failed completely, which is an ERROR. THIS ERROR DOES NOT GENERATE A TRIGGER SIGNAL.

8.34 POS 12V ON

This NON-ERROR (green) LED is illuminates when +12 Volt power exists on the bus. The -12 volt power is merely checked for existence, not for accuracy. This is not an error condition. If the LED fails to illuminate, the +12 Volt power has failed completely, which is an ERROR. THIS ERROR DOES NOT GENERATE A TRIGGER SIGNAL.

8.35 GRANT HDDN

This NON-ERROR (yellow) LED illuminated at the time the first error condition is detected, if the VBAT was not able to fully detect errors on the bus grant daisy chain signals BG0-BG3, because the VBAT was located to the right of the the active master, and the daisy chain signal was therefore BLOCKED. The "GRANT HIDDN" indication is not in itself an error condition, but is a warning that the following errors may be hidden from being detected by the VBAT:

MULTI GRANTS, RULE3.6 AND RULE3.10,

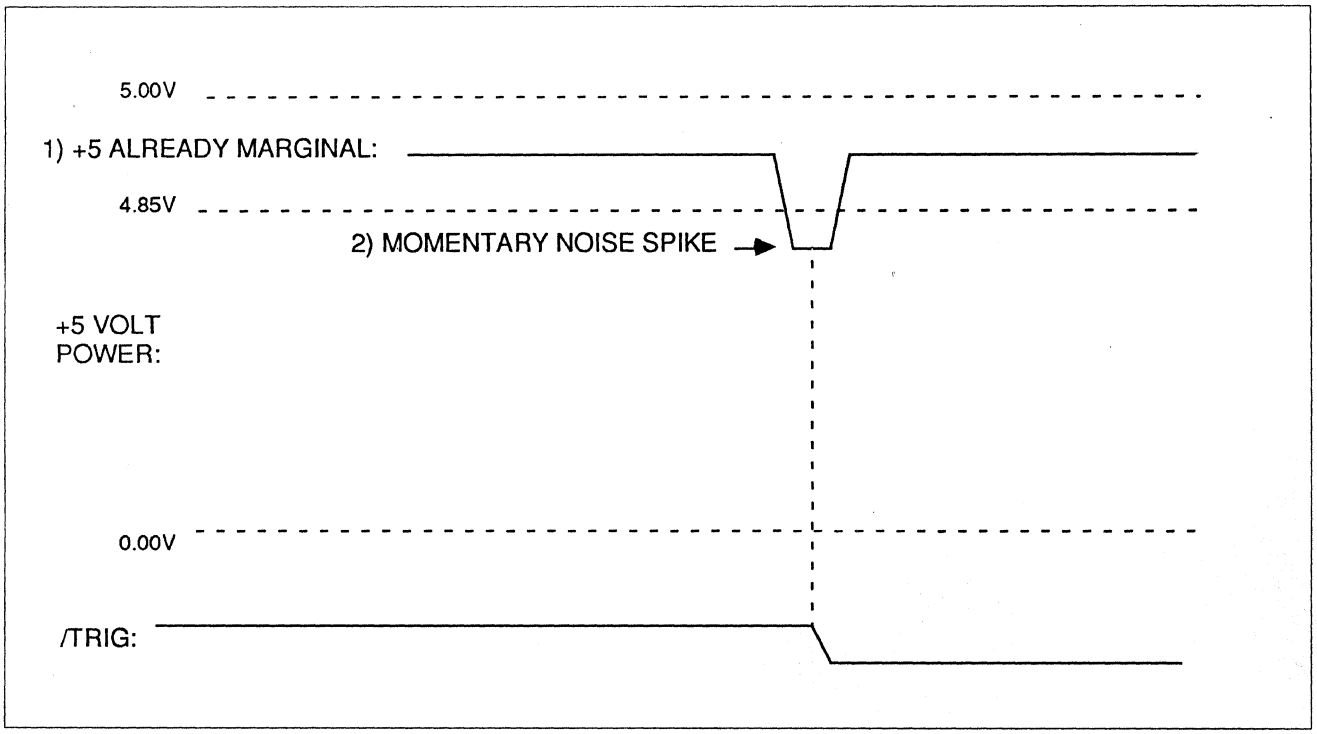
and that the following errors may momentarily be falsely indicated as positive by the VBAT

BR0 ABORTED, BR1 ABORTED, BR2 ABORTED, BR3 ABORTED, RULE2.28-IACK, RULE2.28-WRT, RULE2.28-LWD, RULE2.28-DS, RULE2.20

Repositioning the VBAT leftward of the active masters in the system will prevent the "GRANT HDDN" warning. Where this is not possible, the HIDE jumper being installed will reset the false triggers as soon as BBSY* is detected during the offending bus cycle.

8.36 +5V TOO LOW

The "5V TOO LOW" LED illuminates when the +5 Volt power on the bus dips below 4.85 volts. This trigger is capable of detecting even very brief power dropouts. This type of problem is far more common than is generally realized. The operation of the trigger is illustrated below:

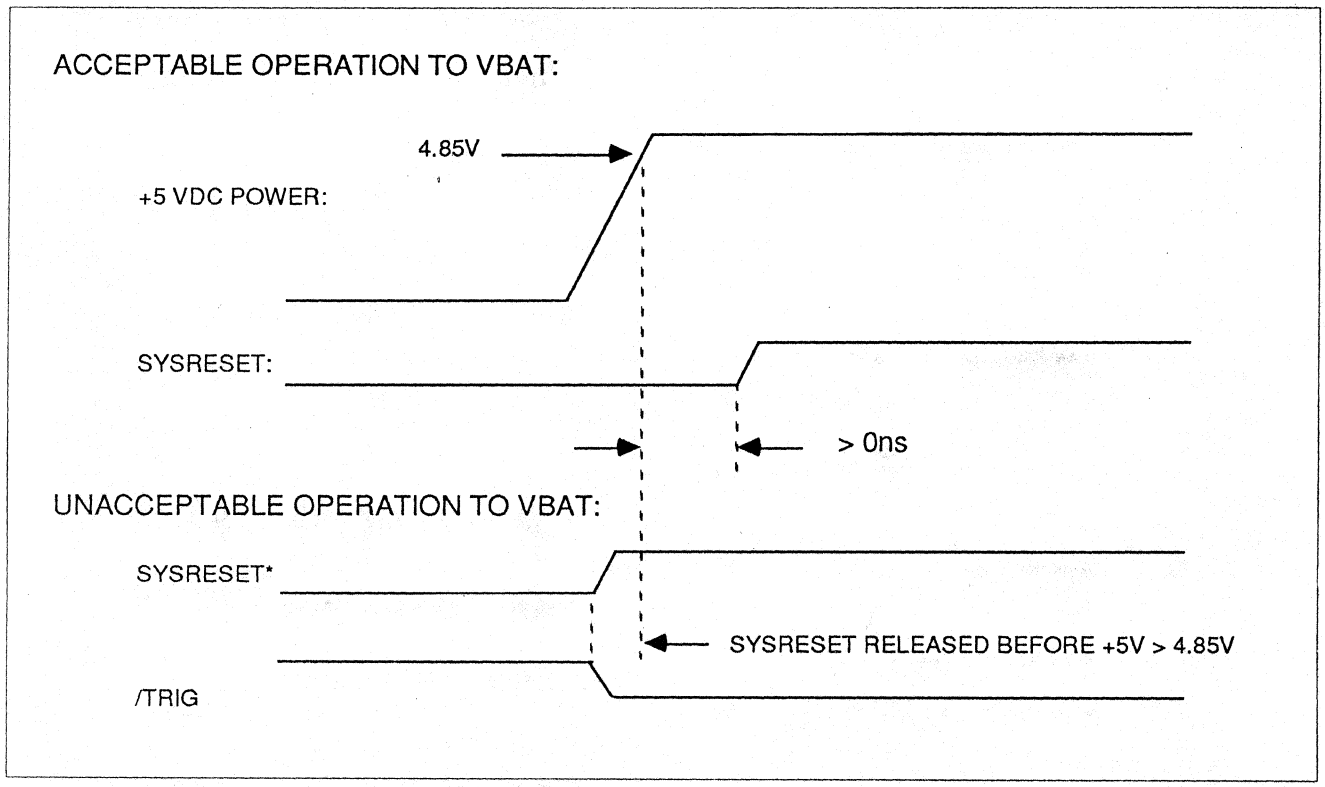


CONDITIONS WHICH CAN CAUSE THE ABOVE ERROR:

1) The +5 volt power at the power supply may be misadjusted, to too low a value.
2) The wiring which transmits the +5 volt power between the power supply and the backplane may be too thin, resulting in excessive voltage drop. This problem may generally be solved by properly connecting the remote-sense power supply inputs at the backplane.

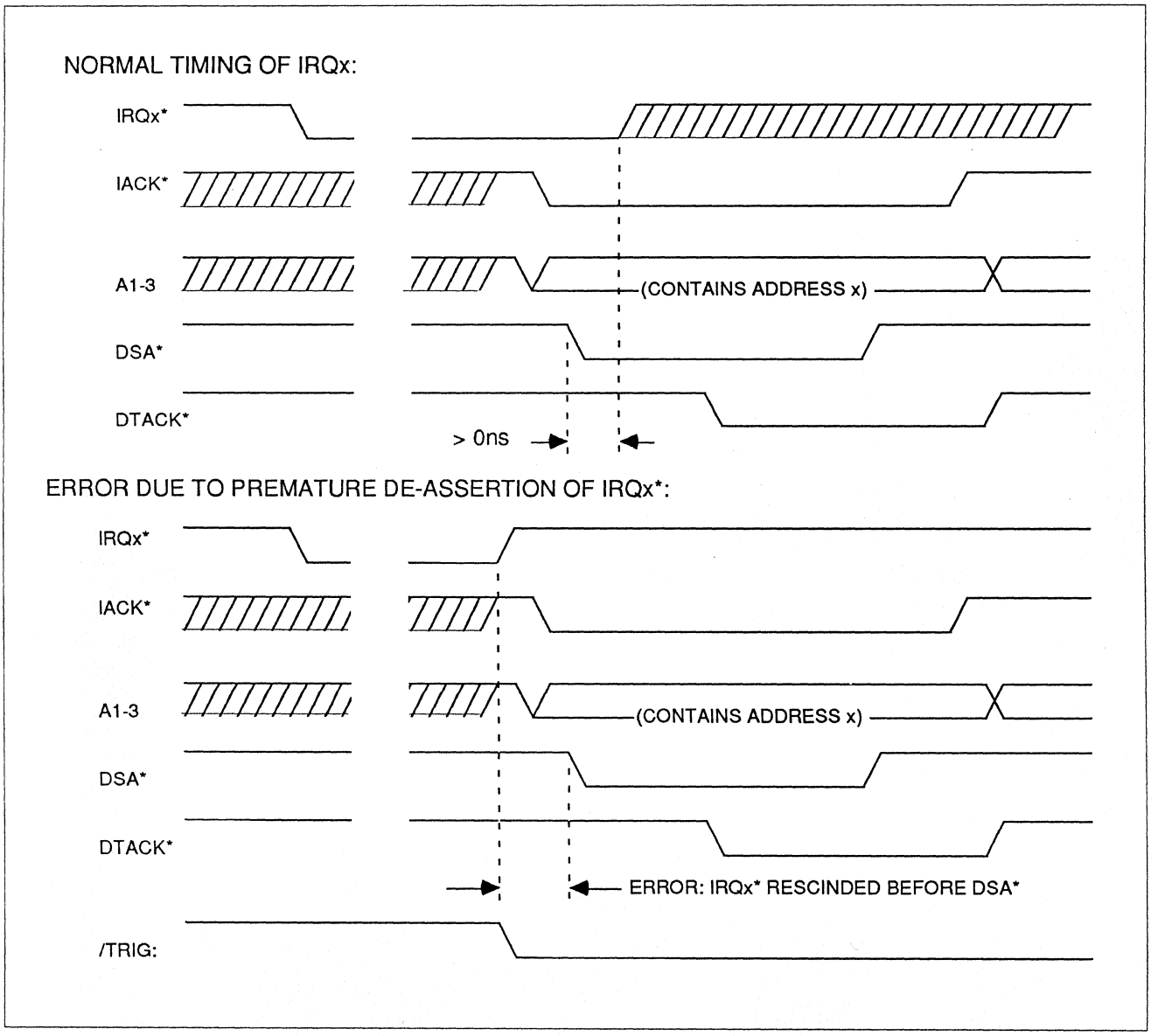
8.37 RULE 5.1

The "RULE5.1" LED illuminates if, during power up, the SYSRESET* signal goes away before the +5V lines go above 4.85 volts. The VME specification requires that SYSRESET* be held low until 200 mS after the +5 VOLT power goes to 4.875 volts. The VBAT is more lenient, requiring the +5VOLT lines to reach at least 4.85V before SYSRESET* is released, as illustrated below:



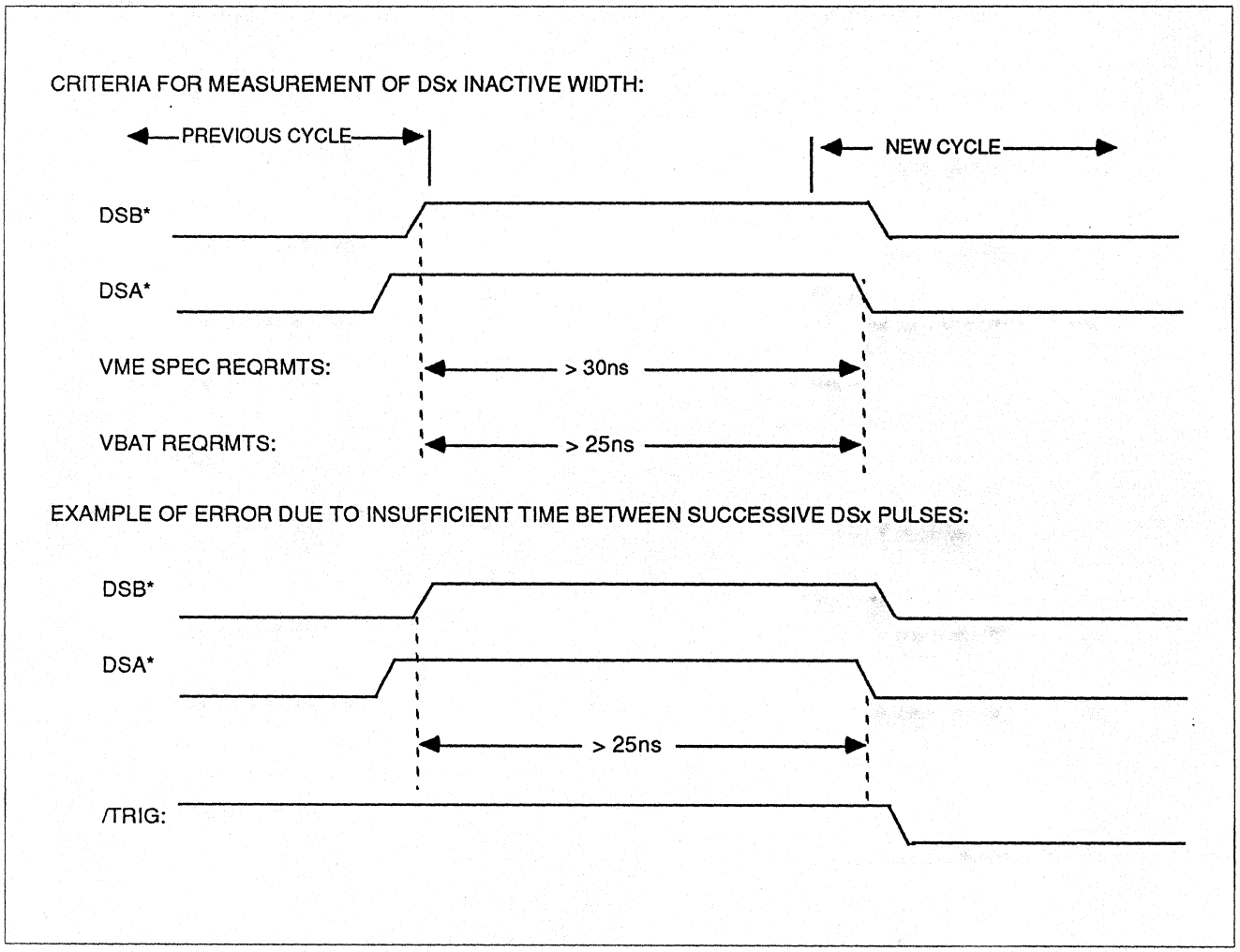
8.38 IRQX ABORTED (RULES 4.5, 4.6)

An interrupt line IRQ1*-IRQ7* is aborted before the appropriate interrupt acknowledge cycle is started. Rules 4.5 and 4.6 of the VME bus specification prohibit an interrupter from releasing and interrupt request line IRQx before it detects a falling edge on DSA* during the interrupt acknowledge cycle which acknowledges its interrupt. To verify this violation, a fast (preferably at least 100 MHz) logic analyzer should be set up to display DS0*, DS1*, IRQ1* through IRQ7*, IACK*, A01-A03, DTACK* and the VBAT's "IRQX* ABORTED" trigger output. The following illustrates the normal timing between interrupt and interrupt acknowledge cycles.



8.39 RULE 2.37

The "RULE2.37" LED illuminates if DS0* or DS1* are inactive for an insufficient time between successive bus cycles (<30 ns). To verify this violation, a very fast (preferably at least 200 MHz) logic analyzer should be set up to display DS0*, DS1*, DTACK* and the VBAT trigger output behind the RULE2.37 LED.



Note that DSA and DSB* refer to the first occurring and second occurring, respectively, of data strobes DS0* and DS1*.*

NOTE: In addition to its normal function, the "RULE2.37" trigger can often detect NON-MONOTONIC rising (ending) edges of DS0* or DS1*. Such behavior is usually the result of a slow-rising DS0* or DS1* For further details, refer back to section 8.27, which discussed a similar situation for the rule 2.39 trigger.

8.40 RULE 2.31

This LED illuminates if AS* is inactive for an insufficient time (<30 ns) between successive bus cycles. To verify this violation, a very fast (preferably at least 200 MHz) logic analyzer should be set up to display AS*, DTACK*, and the VBAT trigger output behind the "RULE2.31" LED.