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TEXAS INSTRUMENTS

MANUAL REVISION HISTORY

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Preface

This document provides technical information about the standard and optional hardware devices of the Texas Instruments (TI) BUSINESS-PRO(TM) Computer, TI Part No. 2240803-0001. The information in this document is intended to be used by system designers, value added retailers (VARs), maintenance personnel, and system users. This manual is divided into the following six sections and seven appendixes:

Section

Section	
1	Introduction -- Provides general information about the BUSINESS-PRO computer, a general system overview, and system specifications.
2	Main Logic Board -- Provides detailed information about the operation and the capabilities of the BUSINESS-PRO main logic board. This section includes information about the system central processing unit, the system memory and memory control logic, the direct-memory access logic, the input/output (I/O) control logic, and various system interfaces.
3	Power Supply -- Provides tabulated information about the BUSINESS-PRO system power supply.
4	Keyboard -- Provides descriptive information about BUSINESS-PRO keyboard, its interface to the system, and the commands used for communication and data transfer between the system and the keyboard.
5	Floppy Disk Drive Controller -- Provides information about the controller and the floppy disk drive interface.
6	Hardware Options -- Provides information about the various optional hardware devices and subsystems that are available for the BUSINESS-PRO computer.

Appendixes

A	Memory and I/O Maps -- Provides a list of the system memory addresses and their allocations, and a general list of the system I/O address allocations.
B	TI Mode I/O Maps -- Provides categorized lists of the TI mode I/O address allocations.
C	PC-AT Mode I/O Maps -- Provides categorized lists of the PC-AT mode I/O address allocations.
D	PAL(R) Programming Information -- Provides tables of the main logic board programmable array logic (PAL) functions, based on the PAL programming equations.
E	Logic Diagrams -- Provides system logic diagrams.
F	Option Board Outline -- Gives outline dimensions for full- and half-size boards.
G	Switch and Jumper Settings -- Gives a summary of the switch and jumper option settings.

Section 1

Introduction

1.1 GENERAL

The Texas Instruments (TI) BUSINESS-PRO(TM) Computer, a member of the TI Professional Computer line, can be configured for a variety of computer applications. The BUSINESS-PRO offers most of the features of the Texas Instruments Professional Computer (TIPC) plus greater memory and mass storage capacity, greater expandability, and greater speed.

The BUSINESS-PRO can be configured to be compatible with most of the software designed for the TIPC as well as that designed for the IBM(R) Personal Computer AT(TM) (PC-AT). The computer supports a wide variety of operating systems, including MS(R)-DOS and XENIX(R). While using MS-DOS, the user can switch back and forth between the TI mode and the PC-AT mode with the appropriate hardware.

The BUSINESS-PRO computer's unique turbo operating mode increases the speed of the computer by deleting memory wait states. This enhancement allows both 16-bit and 8-bit memory transfer operations with minimum delay.

The BUSINESS-PRO system consists of a high-resolution, bit-mapped display (either color or monochrome), a combined TIPC and PC-AT keyboard, and a system unit that includes a floor stand. The computer and its floor stand fit easily under a desk top. A variety of mass storage devices can be installed in the system unit. The system can be used as a high-performance, single-user workstation; a local area network (LAN) server; an artificial intelligence (AI) workstation; or as a clustered, multiuser system running in the XENIX software environment.

1.1.1 Workstation Applications

The single-user capability is ideal for users who require a faster computer for processing large quantities of data. Also, it is appropriate for running memory intensive, AI-based software that includes integrated window environments and large expert systems. The BUSINESS-PRO is also well-suited for users who require access to large databases with natural language interfaces or for engineering applications.

1.1.2 Local Area Networks

The LAN server capability of the BUSINESS-PRO provides high-performance and security capabilities to work groups who require resource sharing and teamwork among different workstations. A LAN allows users to share databases and peripheral devices, and to distribute their processing needs.

1.1.3 Multiuser Environments

The multiuser cabability of the BUSINESS-PRO allows multiple users to share a single processor. A typical multiuser configuration consists of the BUSINESS-PRO system unit with TI Model 931 or TI Model 924 Video Terminals connected to it. The system unit can provide the mass storage and a printer.

1.2 BUSINESS-PRO Hardware

The BUSINESS-PRO computer hardware is characterized by its high-performance capabilities and configuration flexibility. The following paragraphs provide an overview of the BUSINESS-PRO hardware.

1.2.1 System Unit

The system unit houses the main logic board, the system power supply, the mass storage devices, and various controllers and interface boards. The main logic board contains the central processing unit (CPU), direct memory access (DMA) logic, input/output (I/O) logic, and various supporting circuits.

1.2.1.1 Central Processing Unit. The CPU is based on the Intel(R) 80286, 16-bit microprocessor. An optional 80287 numeric coprocessor can be added to the CPU to provide enhanced operations for those applications involving a large number of floating point mathematic operations.

Intel is a registered trademark of Intel Corporation.

1.2.1.2 System Memory. The main logic board contains 512K bytes of 150-nanosecond RAM that can be expanded to 3.64 megabytes without using any of the systems 14 expansion slots. The expansion slots can be used to expand the main memory up to a total of 14.64 megabytes.

1.2.1.3 Serial and Parallel Ports. The main logic board provides a parallel port and a serial port. The parallel port can support a printer or other options requiring parallel data. The serial port is a programmable, PC-AT compatible port that provides asynchronous communication between the system and various options that require serial data transfers.

1.2.1.4 Mass Storage System. The system unit provides mounting rails that can accommodate up to six half-height mass storage devices. For maximum flexibility, the user can choose a combination of half-height and full-height peripherals (with appropriate controller required). The following mass storage devices are available from Texas Instruments:

* Half-height, 21-megabyte Winchester disk drive
* Full-height, 40-megabyte Winchester disk drive
* Full-height, 72-megabyte Winchester disk drive
* Full-height, 120-megabyte Winchester disk drive
* Half-height, 1.2-megabyte floppy disk drive
* Half-height, 360-kilobyte floppy disk drive
* Half-height, tape backup drive

1.2.1.5 Expansion Slots. The BUSINESS-PRO system unit contains 8 full-size, and 6 half-size expansion slots. Three of these slots are 8-bit slots that allow the installation of PC-XT compatible options. As an example of the degree of flexibility the slots can provide, a system with a 3.64-megabyte main memory, a floppy controller, a Winchester disk controller with one or more Winchester disk drives, a video controller, and a tape backup system still has 10 slots available for other options.

1.2.2 Keyboard

The BUSINESS-PRO keyboard provides both TI and PC-AT operations with a standard typewriter layout, plus some special keys and keypads. These include dedicated function keys, cursor control keys, and a numeric keypad. The keyboard also features tactile typing response and a variable tilt adjustment. The standard configuration provides 100 keys, many of which can be relocated using special software. Also, spaces are provided for additional keys, which can increase the total key count to 144.

1.2.3 Display Units

The BUSINESS-PRO provides optional dual-resolution display units in either a color version or a monochrome version. Both versions support software designed for the TIPC as well as software designed for the IBM color/graphics monitor adapter. The display units feature tilt/swivel bases that provide two identical connectors to accommodate a keyboard and/or an optical mouse. The use of identical connectors permits the keyboard and the mouse to connect to either side of the monitor base. The units also provide an internal speaker with volume control.

1.2.4 Optical Mouse

The optical mouse and its associated pad provide fast and easy cursor control on the display screen. The mouse features three buttons whose functions depend upon the software. The mouse is especially useful for graphics applications.

1.2.5 Communications

The communications hardware options include the TI mode RS-232 serial interface and the EtherLink(TM) hardware kit.

The RS-232 provides a serial port for communicating with external devices such as modems, serial printers, and other computers. Although the RS-232 is provided for TI mode applications, specially designed hardware allows its use in the PC-AT mode to provide a third or fourth communications port.

The EtherLink hardware kit provides a means of connecting the BUSINESS-PRO to a local area network.

1.2.6 Graphics

The TI mode CRT controller provides high-resolution, bit-mapped, three-plane graphics in eight colors with the color display unit or in eight levels of intensity with the monochrome display. The PC-AT mode CRT controller provides IBM CGA-compatible graphics and IBM monochrome/printer adapter compatible text (excluding the printer functions). Both controllers are specially-designed for use with an 80286-based computer system. They can be installed simultaneously to allow dual-mode operation.

EtherLink is a trademark of 3Com Corporation.

1.3 BUSINESS-PRO COMPUTER STANDARD CONFIGURATIONS

The BUSINESS-PRO computer system is available in two standard hardware configurations: the single-drive floppy system and the Winchester system. To allow the user maximum flexibility when configuring the system, neither of these basic configurations contains the video controllers or the display units.

1.3.1 Single-Drive Floppy System

The single-drive floppy system includes the following components:

* System unit with a main logic board
* Bus interface board that provides 14 expansion slots
* Keyboard
* 1.2-megabyte floppy disk drive and controller
* Keylock

1.3.2 Winchester System

The Winchester system includes the following components:

* System unit with a main logic board
* Bus interface board that provides 14 expansion slots
* Keyboard
* 1.2-megabyte floppy disk drive and controller
* 21-megabyte, half-height Winchester disk drive and controller
* Keylock

1.3.3 System Unit Enclosure

The system unit enclosure is 19.8 centimeters (7.75 inches) wide 47.7 centimeters (18.8 inches) high, and 47.0 centimeters (18.5 inches) deep. The system enclosure houses the bus interface board, the main logic board, and a system power supply with an integral ventilation fan. An optional RAM expansion board can be attached to an edge connector on the main logic board to provide up to 3 megabytes of additional RAM without using an expansion slot. Appendix E contains the system interconnect diagram.

1.3.3.1 Main Logic Board. The main logic board contains the CPU, the memory-control logic, and I/O control devices. The board provides connectors for the 25-pin parallel printer port, the 25-pin asynchronous serial port, and an 8-conductor keyboard cable. It also provides a 100-pin interface connector to the bus interface board.

1.3.3.2 Bus Interface Board. The bus interface board provides the system bus connections between the main logic board and the option boards. The board provides eight full-size and six half-size option slots. Each option board contains a bulkhead mounting plate to secure the board in the chassis and to provide a mount for any required external-access connectors. The bus interface board mounts above the main logic board. A small interface board connects the two boards together.

1.3.3.3 System Power Supply. The system power supply is self-contained within a box, which mounts inside the system enclosure. The power supply contains a dc fan that obtains its operating voltage from the 12-volt secondary of the power transformer. The power supply provides 225 watts ouput power to operate a fully configured system.

The power switch is located on the front panel of the computer. A cable connects the switch to the rear of the power supply. The switch also controls power to a switched power-access connector to which a display unit can be connected. This arrangement allows the user to control power to both the system unit and the display unit with a single switch.

1.3.3.4 Mass Storage Device Mounting. The system enclosure accepts mounting slides for the mass storage devices. The slides allow the devices to be installed or removed from the front of the system unit. A typical configuration includes one or two 1.2-megabyte floppy disk drives and one or two full-size Winchester disk drives. A wiring harness from the system power supply provides power for the devices.

A 34-pin ribbon cable connects between the floppy disk controller and the floppy drive compartment; it handles data and control signal transfers between the controller and the first two floppy drives. The Winchester disk drives also use a 34-pin ribbon cable for control of multiple drives, however, each drive requires a separate data interface to the controller.

NOTE

The addresses in this manual are in hexadecimal notation, as stated in column headings and by a trailing H after the hexadecimal number.

1.4 BUSINESS-PRO SPECIFICATIONS

Table 1-1 lists the environmental, electrical, and physical specifications for the BUSINESS-PRO computer system.

Table 1-1 BUSINESS-PRO System Specifications

Characteristic	Specification
Environmental requirements:	
Temperature:	
Operating	+10 to +35 degrees C (+50 to +95 degrees F) with a temperature gradient of less than 10 degrees C (50 degrees F) per hour
Nonoperating	-40 to +65 degrees C (-40 to +149 degrees F)
Relative humidity (noncondensing):	
Operating	15 to 80 percent
Nonoperating	5 to 95 percent
Altitude	-300 to 12 000 meters (-984.24 to 39 369.50 feet)
Power Requirements:	
Voltage:	
Domestic	90 to 140 volts ac
International	180 to 264 volts ac
Frequency:	
Domestic	57 to 63 Hertz
International	47 to 53 Hertz

Table 1-1 BUSINESS-PRO System Specifications (Continued)

Characteristic	Specification
Physical dimensions:	
System Unit:	
Width	19.8 cm (7.8 in)
Depth	47.0 cm (18.5 in)
Height	47.2 cm (18.6 in)
Weight	26.1 kg (58.0 lbs)
Color monitor:	
Width	38.1 cm (15.0 in)
Depth	38.9 cm (15.3 in)
Height	41.9 cm (16.5 in)
Weight	11.7 kg (26.0 lbs)
Monochrome monitor:	
Width	33.8 cm (13.3 in)
Depth	32.3 cm (12.7 in)
Height	36.6 cm (14.4 in)
Weight	6.8 kg (15.0 lbs)
Keyboard:	
Width	54.1 cm (21.3 in)
Depth	19.3 cm (7.6 in)
Height	4.5 cm (1.8 in)
Weight	2.1 kg (4.8 lbs)

Section 2

Main Logic Board

2.1 GENERAL

Figure 2-1 shows a block diagram of the BUSINESS-PRO computer's main logic board. This board contains the system's central processing unit (CPU) and its supporting logic, the system memory and memory control logic, direct-memory access (DMA) logic, and various other devices and circuits that generate and control system operations.

Appendix E contains the main logic board's logic diagrams and an index to its various circuits.

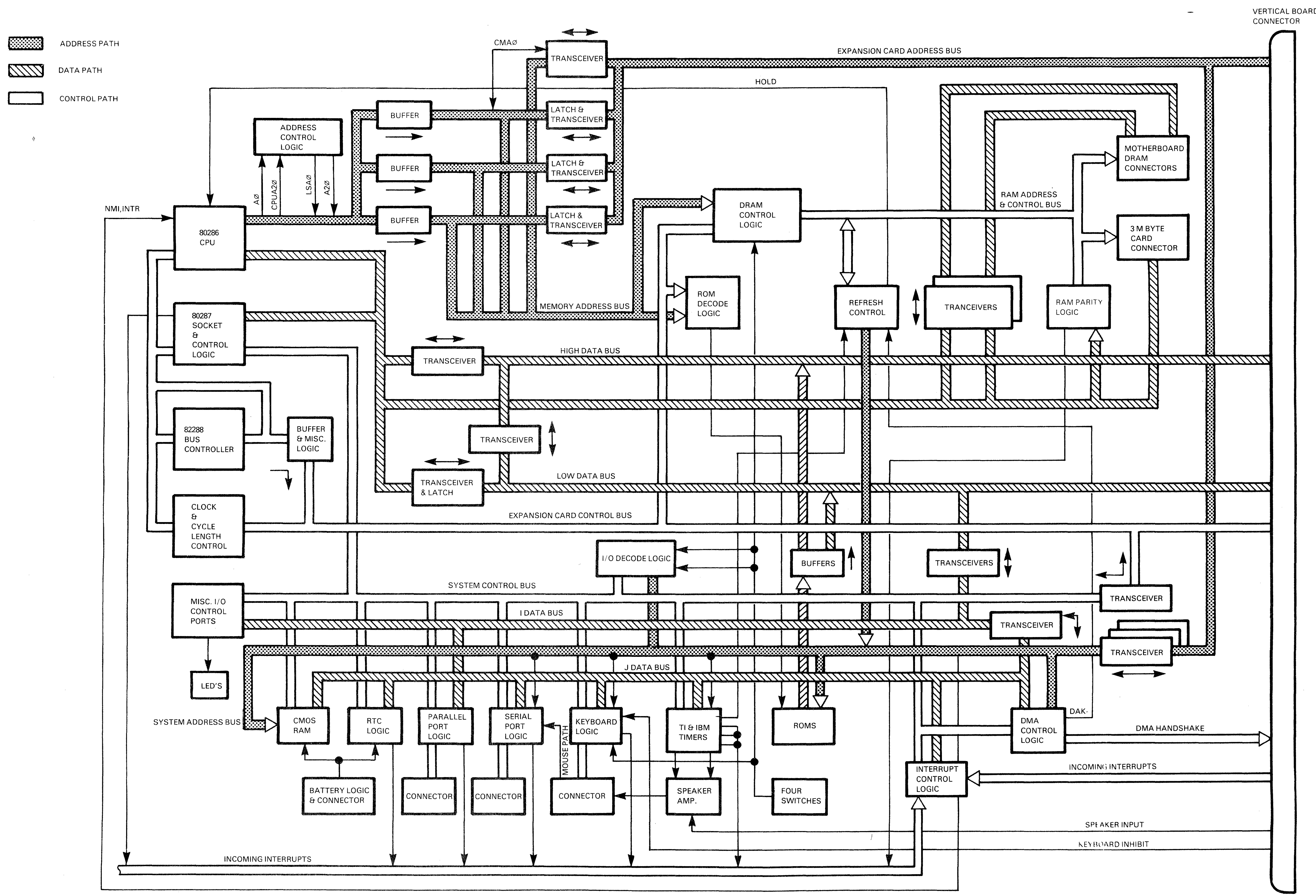

Figure 2-1 Main Logic Board Block Diagram

Figures 2-2 and 2-3 show the locations of the connectors, jumpers, switches, and the coprocessor on the two versions of the main logic board. The two boards, TI Part No. 2240843-0001 and 2535670-0001, can be distinguished by the presence or absence of the coprocessor option jumpers. The original board, TI Part No. 2240843-0001 does not have these jumpers; the later version does. The following is a list of the reference designators and their functions:

* J2 -- Expansion bus connector.
* J3 -- Expansion RAM interface connector.
* J4 and J5 -- Coprocessor option jumpers.
* J8 -- Serial port interface connector.
* J9 -- Parallel port connector.
* J10 -- Connector for the 6-volt battery.
* J11 -- Keyboard/mouse interface connector.
* J12 and J13 -- Interface connectors for on-board expansion RAM board 1.
* J14 and J15 -- Interface connectors for on-board expansion RAM board 2.
* J16 and J17 -- Interface connectors for on-board expansion RAM board 3.
* J18 and J19 -- Interface connectors for on-board expansion RAM board 4.
* J20 -- Power connector for the main logic board.
* E1, E2, and E3 -- Speaker terminals for systems that do not have a speaker in the monitor.
* SW1 -- Five-section, dual-inline-package (DIP) switch that provides all required manual switching for the main logic board. The following table shows the use and setting for each section of the switch.

Section	Use	Setting	
Switch 1	CRT switch	Off=mono	On=color
Switch 2	Parallel port	Off=port 1	On=port 2
Switch 3	Serial port	Off=port 1	On=port 2
Switch 4	128K-byte DRAM	Off=disable	On=enable
Switch 5	Base DRAM	Off=512K bytes	On=256K bytes

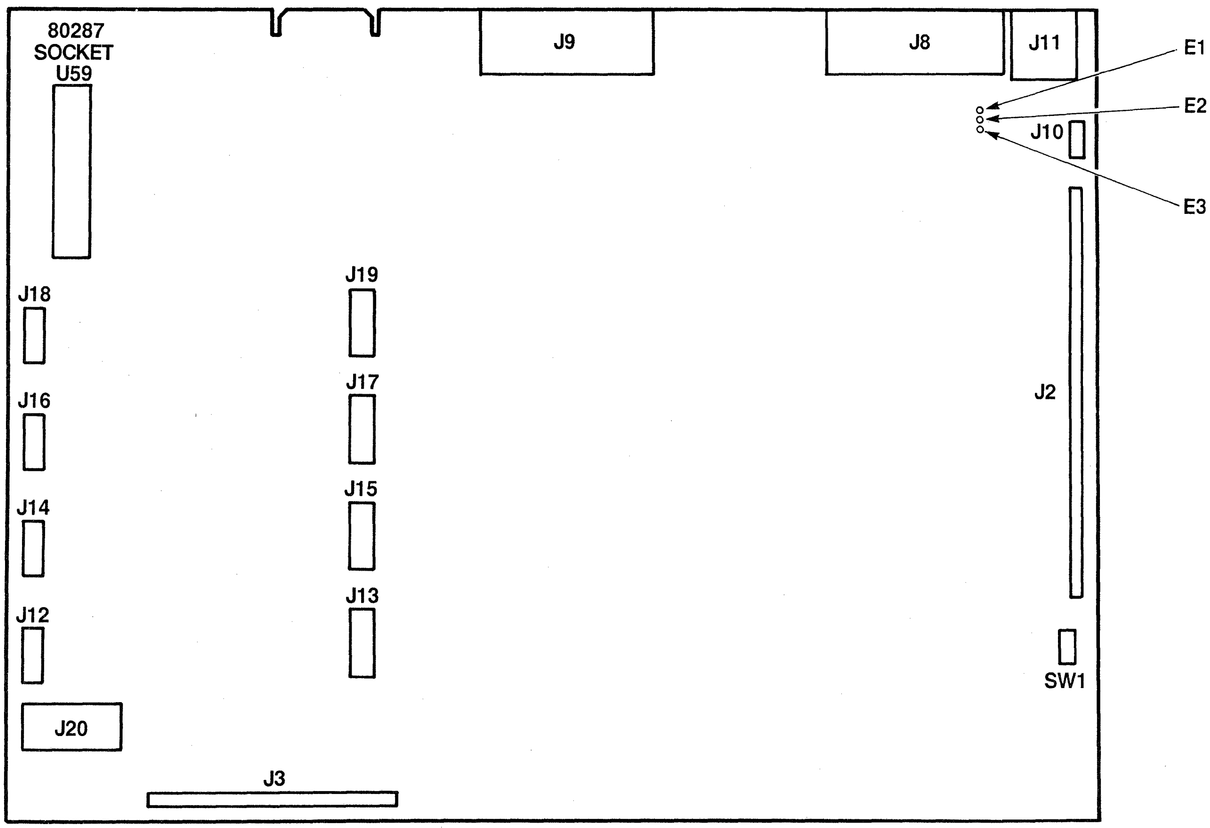

Figure 2-2 Main Logic Board, TI Part No. 2240843-0001, Key Components

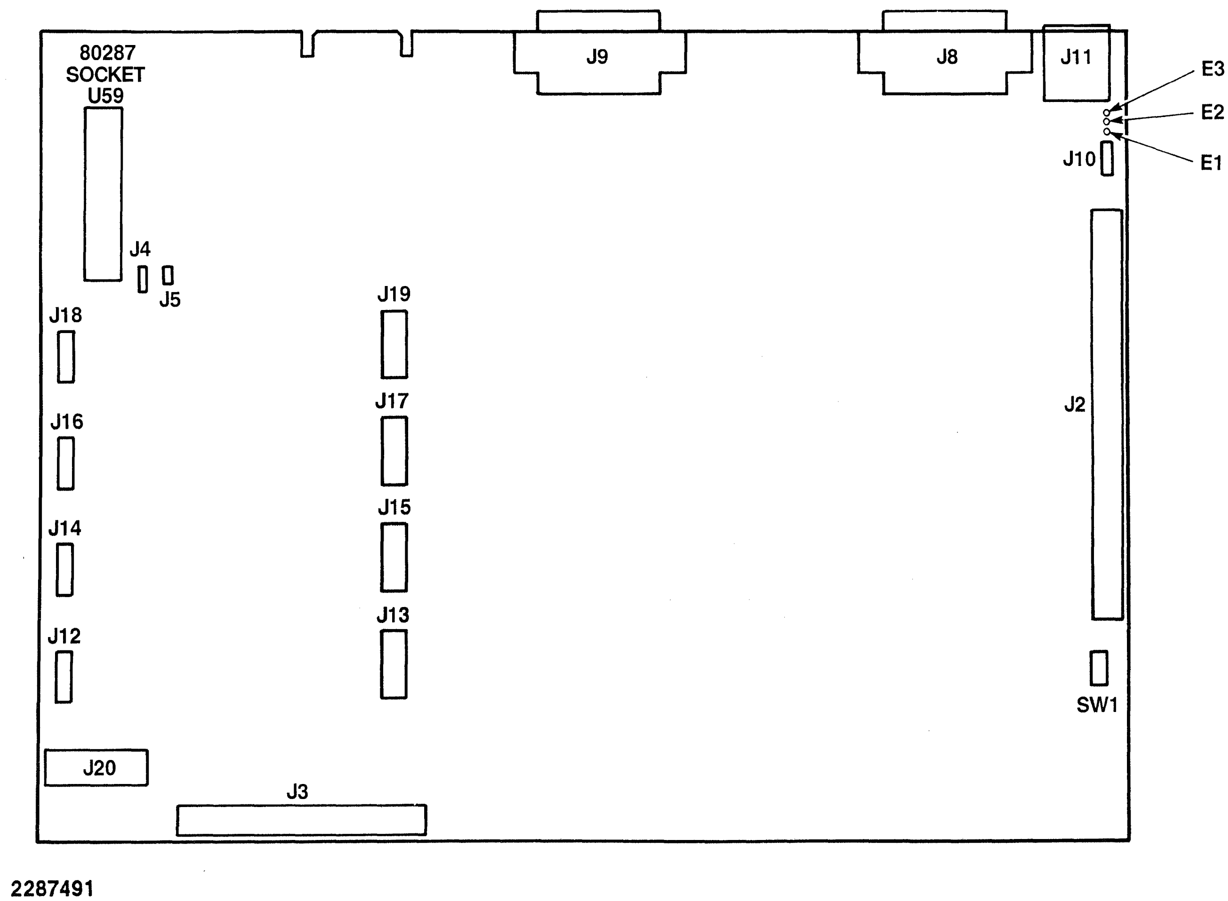

Figure 2-3 Main Logic Board, TI Part No. 2535670-0001, Key Components

The following paragraphs describe the circuits of the main logic board.

2.2 SYSTEM CENTRAL PROCESSING UNIT

The system central processing unit (CPU) consists of an 80286 microprocessor unit and an optional 80287 numeric coprocessor. The microprocessor unit (MPU) and the coprocessor operate in parallel so that they appear to associated components as a single chip. If both devices are installed, the term CPU refers to both the 80286 and the 80287. The system CPU also includes the system clocks, the CPU bus buffers and latches, and the CPU status decoding and control line generation logic. The following paragraphs describe the circuits.

2.2.1 Microprocessor Unit

The MPU can operate in either the real address mode or the protected virtual address mode. A reset operation places the MPU in the real address mode, which provides up to 1 megabyte of real address space. The MPU can then be placed in the protected virtual address mode, in which 1 gigabyte of virtual addresses can be mapped into a 16-megabyte real address space. This mode also provides memory protection to isolate the operating system and to ensure privacy for the programs and data of each task. The only way to return to the real address mode from the protected virtual address mode is to reset the MPU.

2.2.2 Optional Numeric Coprocessor

An additional socket is available for the installation of an 80287 IC optional numeric coprocessor. For additional information, refer to the paragraphs entitled Numeric Coprocessor in Section 6.

2.2.3 CPU Bus Buffering

A set of address and control latches and various bus buffers (data, address, and control) are provided as part of the CPU. The following paragraphs describe these circuits.

2.2.3.1 Address and Control Bus Buffering. The CPU controls the address and control bus buffers, transceivers, and latches via the address latch enable (ALE) and hold acknowledge (HOLDA) signal, and a set of control lines labeled P/MD, D/PM, and PM/D, where P, D, and M represent processor-driven cycles, DMA-driven cycles, and master-driven cycles, respectively.

These control lines assume the following levels for the indicated type of cycle:

* P/DM -- High for a processor-driven cycle and low for a master- or DMA-driven cycle.

* D/PM -- High for a DMA-driven cycle and low for a processor- or master-driven cycle.

* PM/D -- High for a processor- or master-driven cycle and low for a DMA-driven cycle.

Table 2-1 lists the various devices and their states for the various types of cycles.

Table 2-1 Address and Control Bus Buffering

Devices	MPU Driven Cycles On-Board Memory	MPU Driven Cycles Other	Master Cycle	DMA or Refresh Cycle
U3 and U5	On	On	Off	Off
U4	Latched	Fall Thru	Off	Off
U34, U35 and U36	Latched A --> B	Latched A --> B	Fall Thru B --> A	Fall Thru B --> A
U37	A --> B	A --> B	B --> A	B --> A
U38, U39 and U40	A --> B	A --> B	A --> B	B --> A
U41	Off	Off	Off	On
U42	On	On	Off	Off

2.2.3.2 Data Bus Buffering. The data bus buffers, transceivers, and latches are, for the most part, under PAL(R) control. To provide for correct data transfer during 8-bit operations, the active byte of data is written or read on the low byte of the system data bus during byte wide cycles. Data bus transceiver U21 creates this byte switch. Table 2-2 shows the different buffer states for various operations. Refer to the device programming tables in Appendix D for more information.

Table 2-2 Buffer States of the Data Bus

CPU Driven Cycles	U19	U20	U21	U22	U93
R/W 80287	Off	Off	Off *1	a->b	Off
R/W on-board memory	a->b	a->b	Off	a->b	Off
8-bit device low-byte transfer	b->a R a->b W	Off	Off	b->a R a->b W *2	b->a R a->b W *2
8-bit device high-byte transfer	Off	b->a R a->b W	a->b R b->a W	b->a R a->b W *2	b->a R a->b W *2
8 bit device word transfer	lo-byte 1st latch b R a->b W ---------- hi-byte 2nd stored->a R Off W	b->a R a->b W	Off ---------- a->b R b->a W	b->a R a->b W *2	b->a R a->b W *2
16-bit device transfer	b->a R a->b W *1	b->a R a->b W *3	Off	b->a R a->b W *2	b->a R a->b W *2
MASTER CYCLE	a->b R b->a W *1,*4	a->b R b->a W *3,*4	Off *1	b->a R a->b W *2	b->a R a->b W *2
DMA CYCLE	a->b R b->a W *1	a->b R b->a W *3	Off *1	Off	Off
REFRESH	Off	Off	Off	Off	Off

*1 - Condition true for word or low-byte transfers.
*2 - Condition true if the device accessed is on the specified bus. If not, U93 is off, and U22 is driven a->b.
*3 - Condition true for word or high-byte transfers.
*4 - Condition true for transfers involving on-board memory.

2.2.4 CPU Clock Generation and Bus Control

The CPU clock generator consists of a 24-megahertz can oscillator, a divide-by-two flip-flop, and a divide-by-four flip-flop. These flip-flops provide the 12-megahertz and 6-megahertz system clocks, each of which has a duty cycle of 50 percent. These clocks are buffered by an inverting buffer.

A programmable array logic (PAL) device contains synchronizing logic for the ARDY-, JRDY-, and 0WS- lines from the wait-state control logic and the RES- line from the power-good circuit. Refer to the device programming tables in Appendix D for more information.

2.2.5 Reset Circuit

The main logic board provides the following reset conditions:

* System reset -- Power-up and dropout conditions initiate this reset.

* MPU software reset -- A software instruction initiates this reset to return the MPU to the real address mode from the protected virtual address mode.

* Coprocessor software reset -- A software instruction initiates this reset to return the coprocessor to the real address mode from the protected virtual address mode.

* Shutdown reset -- A shutdown cycle initiates this reset.

The following paragraphs describe the reset conditions.

2.2.5.1 Software Reset and Shutdown Cycles. A programmer can reset the MPU by writing the appropriate command to the keyboard microprocessor. Writing to I/O address 64H with the pulse output port bit 0 command (FEH) on the data bus causes the keyboard microprocessor to pulse the software reset (SFTRST-) signal low for approximately 6 microseconds, thus initiating a software reset to the MPU. The paragraph in Section 6 entitled Numeric Coprocessor describes the method of initiating a coprocessor software reset.

Multiple protection exceptions, while attempting to execute a single instruction, initiate a shutdown cycle. When this occurs, the CPU performs a unique bus operation to indicate to the hardware that a shutdown cycle is in progress and that an MPU reset should be initiated.

When either a software reset or a shutdown cycle is executing, a flip-flop and counter hold the MPU software reset (SOFRES) signal true for at least 16 processor clock cycles to ensure that reset occurs. SOFRES affects only the MPU and not the coprocessor or the rest of the system.

2.2.5.2 System Reset. The power-good or reset detection circuit detects insufficient power conditions if the power on the main logic board is not sufficient to provide reliable operation. A TL7705A supply voltage supervisor monitors the +5-volt supply. This configuration provides automatic restart in the event of a voltage decrease large enough to affect the power supply but not enough to completely shut it down. A timing capacitor ensures that any power-up or dropout activates the reset (RES-) line for at least 5 milliseconds. This reset condition affects the entire system.

2.2.6 Control Signals

The 80288 bus controller receives status information from the MPU and converts it to the following control signals:

* Memory-read control -- BCMRDC-
* Memory-write control -- BCMWTC-
* I/O-read control -- BCIORC-
* I/O-write control -- BCIOWC-
* Interrupt acknowledge -- INTA-

These signals, except INTA-, are further qualified before being passed to the expansion bus. This qualifying eliminates the possibility of contention on the data bus. BCMRDC- and BCMWTC- are transferred to the expansion bus only when the expansion memory is enabled (I/O port 68, bit 3). BCIOWC- and BCIORC- are transferred to the bus when the ongoing I/O transfer operation is not an access to the 2-kilobyte nonvolatile RAM.

2.3 WAIT-STATE CONTROL LOGIC

Figure 2-4 shows a processor-driven cycle with two wait states (Tw1 and Tw2). A PAL device controls the bus controller outputs and the number of wait states that are inserted into an MPU cycle. This logic supplies five basic MPU cycles whose lengths can be varied by the expansion bus option boards via the WAIT- signal and the zero-wait-state (0WS-) signal. The following paragraphs describe these wait-state cycles.

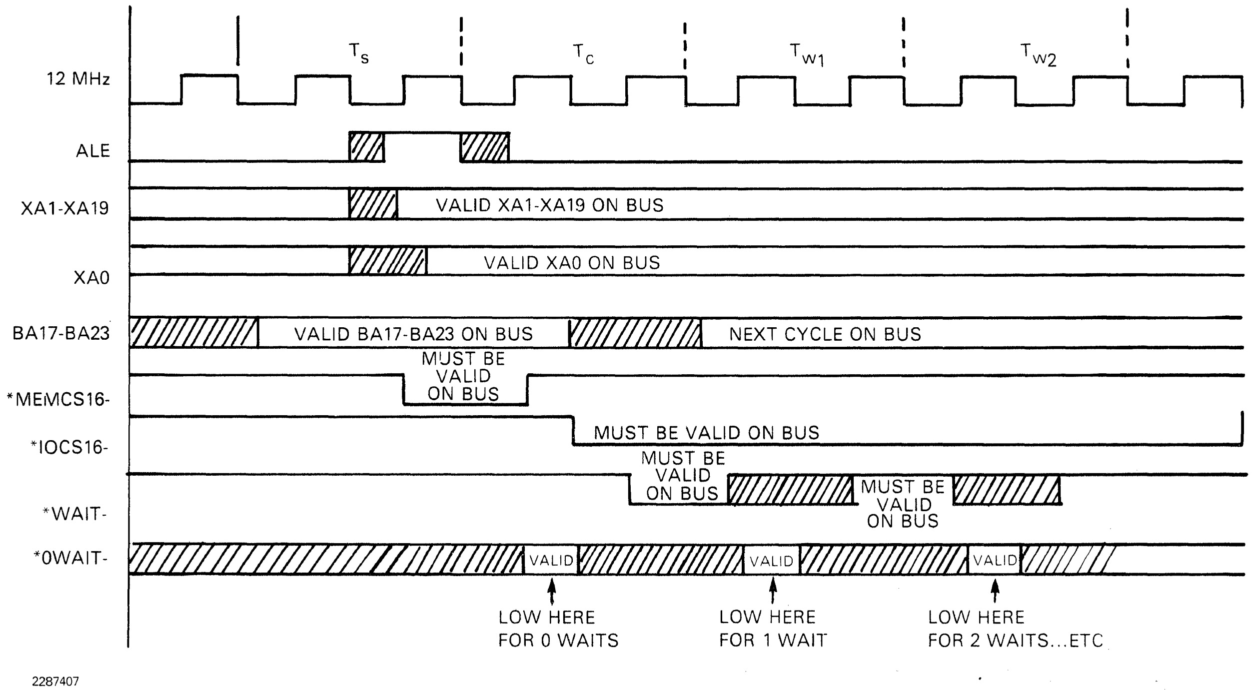

Figure 2-4 Required Input Timing for a Processor-Driven Cycle

2.3.1 Zero-Wait-State Memory Cycles

These cycles are performed whenever the CPU attempts to access the on-board system memory or the memory expansion board with an active TURBO (high) signal (I/O port address 68H, bit 0). An active TURBO signal turns on a light-emitting diode (LED) on the front panel of the system unit. No wait states are inserted for these memory cycles. Therefore, the cycle time is 335 nanoseconds. The bus controller outputs are not delayed. These cycles allow both 16-bit and 8-bit memory transfer operations.

2.3.2 One-Wait-State Memory Cycles

MPU-driven memory cycles for standard, 16-bit memory peripherals have one wait state as shown in Figure 2-5. These cycles last 500 nanoseconds from start to completion, and the bus controller outputs are not delayed. The following types of transfer operations use this type of memory cycle:

* An access to the on-board memory or the 3 megabyte memory expansion board with the TURBO signal inactive.
* An access to the system ROMs.
* An access to the TI compatible video board.
* A memory cycle with an active (low) expansion bus signal (MEM16-).

One-wait-state memory cycles allow both 16-bit and 8-bit memory transfer operations.

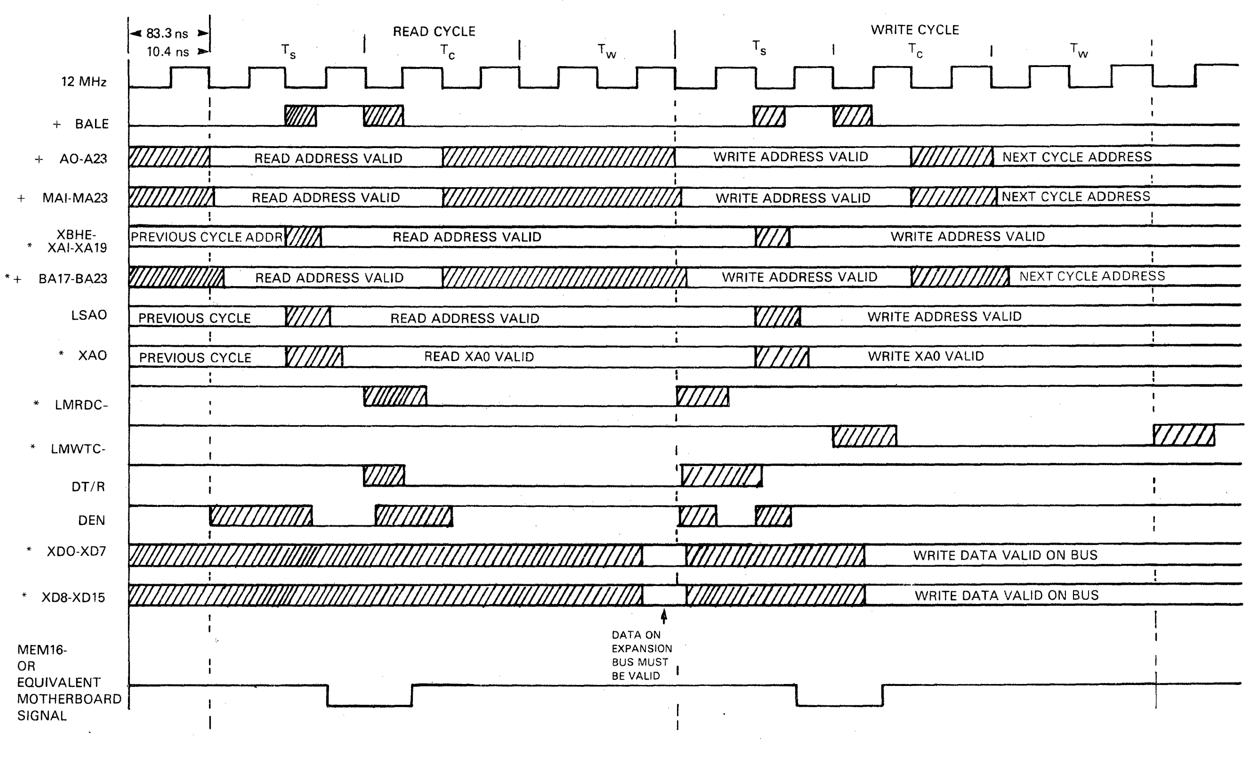

Figure 2-5 One-Wait-State MPU-Driven Memory Cycles

2.3.3 One-Wait-State I/O Cycles

Figure 2-6 shows an MPU-driven I/O read cycle and an MPU-driven I/O write cycle; each of which has one wait state. These cycles are performed for MPU-controlled I/O operations with an active (low) I/O expansion bus signal (IO16-). The bus controller outputs are delayed by 83 nanoseconds so that they do not become active until the middle of the Tc state. However, they still become inactive at the normal (end-of-cycle) time. These cycles require 500 nanoseconds for completion, and they support both 16-bit and 8-bit I/O transfer operations.

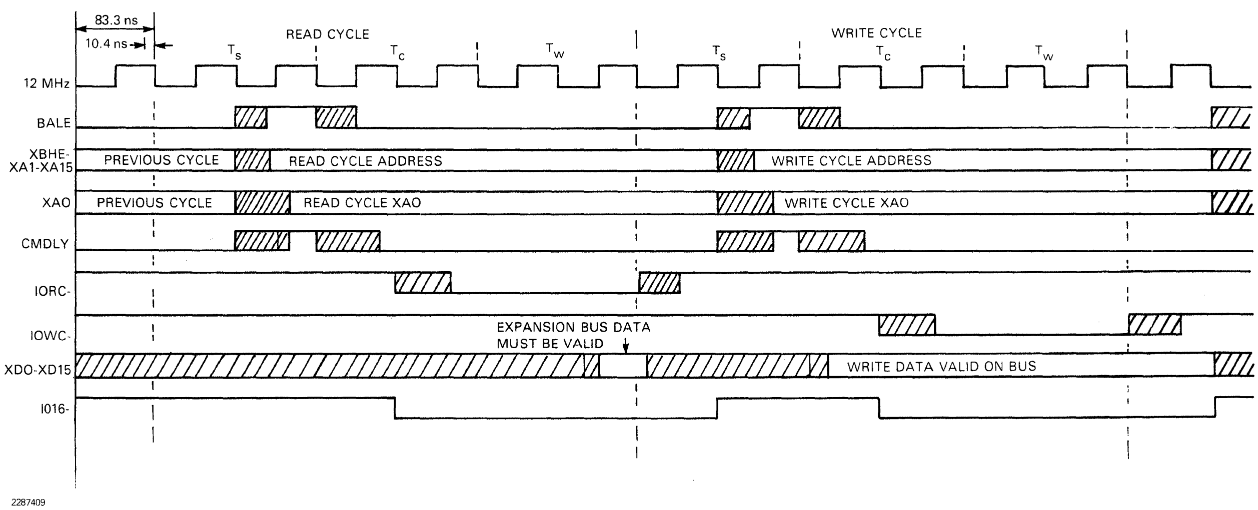

Figure 2-6 One-Wait-State MPU-Driven I/O Cycles

2.3.4 Four-Wait-State Cycles

Figure 2-7 shows an MPU-driven cycle with four wait states. MPU-controlled transfer operations are given four wait states if all of the following conditions are true:

* Both MEM16- and IO16- are inactive (high) for an 8-bit data transfer operation.
* The cycle is not an access to on-board memory or the 3 megabyte memory expansion board.
* The cycle is not an access to the system ROMs.
* The cycle is not a memory access to the TI compatible video board.

For four-wait-state cycles, the bus controller outputs are delayed by 83 nanoseconds so that they do not become active until the middle of the Tc state. However, they still become inactive at the normal (end-of-cycle) time. These cycles support only 8-bit transfer operations to either memory or the I/O space, and they require 1 microsecond for completion.

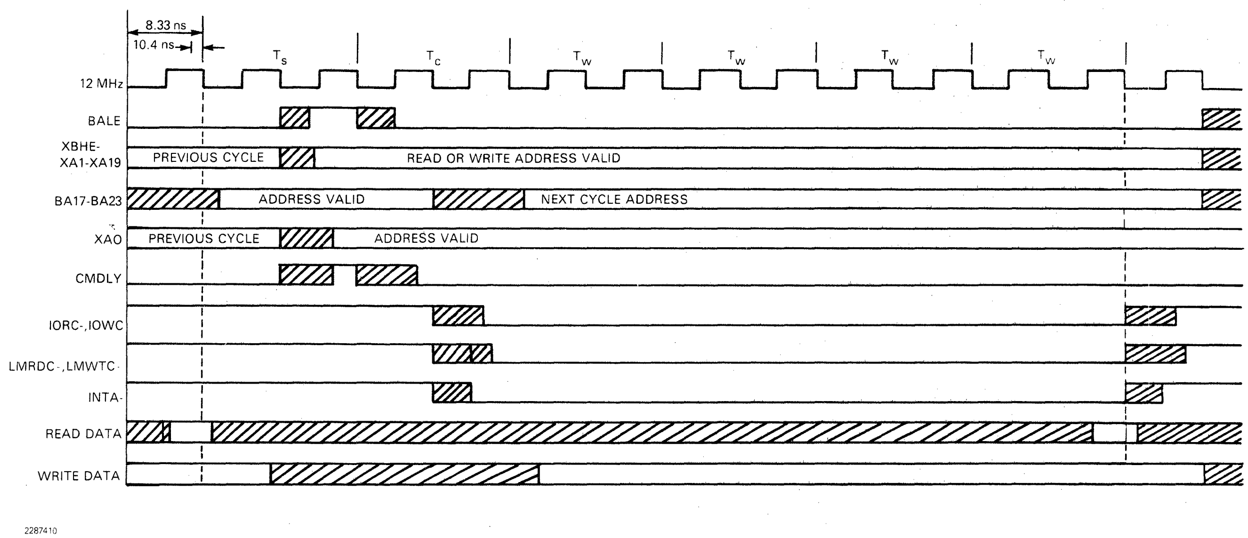

Figure 2-7 Four-Wait-State MPU-Driven Memory or I/O Cycle

2.3.5 Ten-Wait-State Cycles

Figure 2-8 shows an MPU-driven cycle with ten wait states. MPU-controlled access operations are issued ten wait states if all of the following conditions are true:

* Both MEM16- and IO16- are inactive for a 16-bit data transfer operation.

* The cycle is not an access to on-board memory or the 3 megabyte memory expansion board.

* The cycle is not an access to the system ROMs.

* The cycle is not a memory access to the TI compatible video board.

The ten-wait-state transfer mode allows the 16-bit MPU to handle word communications with 8-bit peripheral devices. The operation begins as a normal four-wait-state transfer operation, in which the 80288 outputs are delayed by 83 nanoseconds and the low data byte is transferred as normal.

At the end of the fourth wait state, the bus controller outputs are forced to their inactive states. This signals any device that is being written to that the current transfer operation is complete. If the MPU is attempting to read data, the data latch is clocked at this time. This causes the low-order data byte to be saved so that it can be read by the MPU at cycle completion. During the fifth wait state, the MPU forces address line ALTA0 high and latches it, thus causing the high-order data byte to be transferred.

During the sixth wait state, the bus controller reactivates its output signals, and the cycle ends after the tenth wait state. The total cycle time for this type of cycle is two microseconds.

To an option board on the expansion bus, the ten-wait-state cycle appears to be two consecutive four-wait-state transfer operations except that the expansion bus signal (BALE) is not activated during the second (high-byte) transfer.

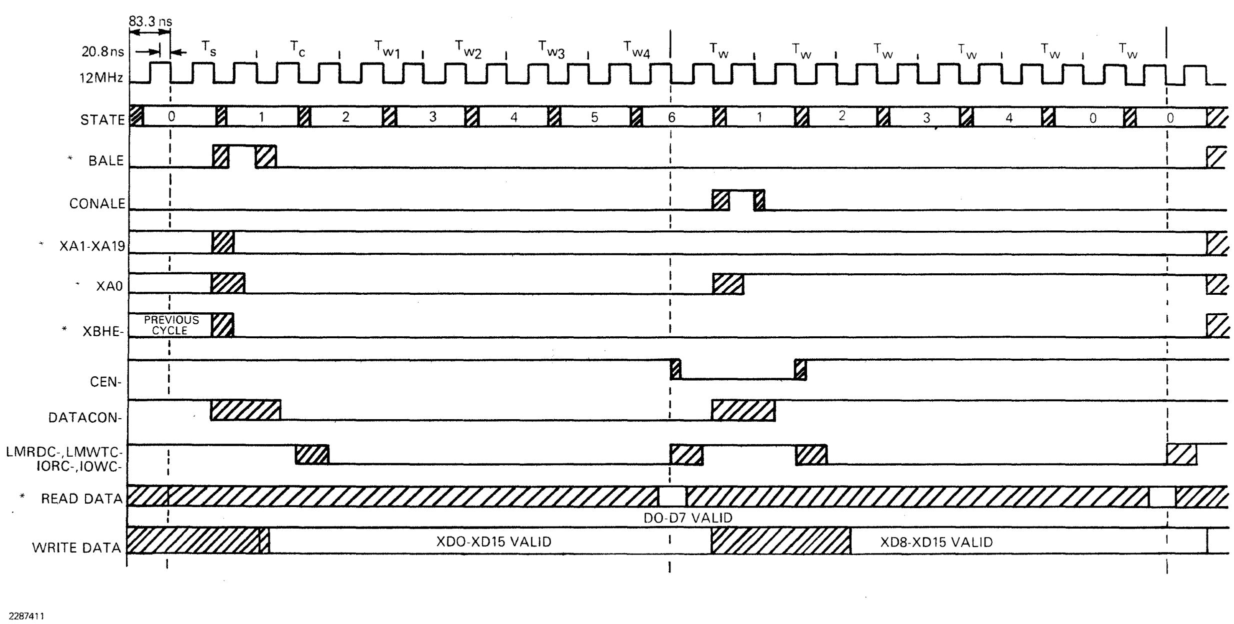

Figure 2-8 Ten-Wait-State MPU-Driven Memory or I/O Cycle

2.4 SYSTEM MEMORY

The BUSINESS-PRO system memory consists of the system ROMs, the on-board dynamic random-access memory (DRAM), and optional expansion DRAM. The following paragraphs describe the system memory.

2.4.1 Main Memory

The main logic board memory consists of 256 kilobytes of DRAM (bank 0) when SW1 position 5 (between pins 5 and 6) is in the ON position. When SW1 position 5 is in the OFF position, 512 kilobytes of main logic board memory are available. The address range for this memory space is 000000H through 07FFFFH. If the switch has four sections, the main logic board memory is automatically 512 kilobytes. When SW1 position 4 (between pins 4-7) is in the ON position and the 128-kilobyte RAM option boards are installed (bank 1), the main logic board memory consists of 640 kilobytes. The address range is 080000H through 09FFFFH. for bank 1.

The 3 megabyte memory expansion board can accomodate up to 12 memory expansion modules, each pair with a capacity of 512 kilobytes. Thus, the on-board memory can be expanded by a total of 3 megabytes for a total memory size of 3.64 megabytes. The address range for this 3-megabyte expansion memory space is 100000H through 3FFFFFH.

The expansion RAM interface connector (header J3) on the main logic board provides power, address, data, and control lines for the 3 megabyte memory expansion board. Table 2-3 lists the header pin assignments.

NOTE

> Switch 1 is a five-section, dual-inline-package (DIP) switch that provides all required manual switching for the main logic board. All references to the closed switch position in this section relate to the schematic representation of the switch. The closed position is equivalent to the position marked ON.

Table 2-3 RAM Expansion Signal Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name
01	+5V	02	+5V
03	+5V	04	+5V
05	+5V	06	GND
07	GND	08	GND
09	GND	10	WE-
11	LBHE-	12	LA0
13	GND	14	LA19
15	LA20	16	LA21
17	MDH-	18	MDL-
19	RAS	20	GND
21	XRA0	22	XRA1
23	XRA2	24	XRA3
25	XRA4	26	XRA5
27	XRA6	28	XRA7
29	XRA8	30	CAS-
31	MDIR	32	POH
33	POL	34	SPE1-
35	SPE2-	36	D0
37	D1	38	D2
39	D3	40	D4
41	D5	42	D6
43	D7	44	D8
45	D9	46	D10
47	D11	48	D12
49	D13	50	D14
51	D15	52	+5V
53	+5V	54	+5V
55	+5V	56	GND
57	GND	58	GND
59	GND	60	GND

2.4.2 System ROMs

The system ROMs are two TMS47128 16-kilobit by 8-bit memory chips with a 250-nanosecond access time. The system memory can also accommodate 32-kilobit ROMs.

The system ROMs contain the system device service routines (DSRs), which are discussed in the BUSINESS-PRO Software Technical Reference Manual. The ROMs are accessed simultaneously at addresses 0F0000H through 0FFFFFH and FF0000H through FFFFFFH, where the eight most-significant bits are used to create the ROM chip select (ROMCS-) signal. Each of the ROMs holds one byte of a 16-bit word.

The ROM data buffers are controlled by the MPU via the memory read (BCMRDC-) command. Therefore, only the CPU can read the system ROMs, and they cannot be read by any bus masters or DMA devices.

2.5 MEMORY CONTROL LOGIC

The memory control logic provides the memory strobes and control signals, as well as address multiplexing for the on-board and expansion memory. The following paragraphs describe the subsystems of the memory control logic.

2.5.1 DMA Controller and Memory Page Register

The system uses two 8237A DMA controller chips and an LS612 memory mapper chip (memory page register) to provide a DMA interface that is compatible with the IBM Personal Computer AT (PC-AT). These three chips implement four 8-bit channels and three 16-bit channels, all of which can access up to 16 megabytes of the system memory. These channels can operate as full bus masters, or they can use a fly-by transfer cycle to operate in the slave mode. In either case, a peripheral device generates the DMA request.

In the slave mode, the DMA controller generates the device acknowledge, the I/O strobe, and a system memory address in response to the DMA request. The 8237A chips generate the lower 16 address bits and the LS612 chip generates the upper 8 bits. The only function of the LS612 chip is to hold the current upper address bits; it cannot increment these bits across the 16-bit address boundaries. Therefore, all slave-mode transfer operations are limited to 64 kilobytes or 64 kilowords, depending on which transfer mode (byte or word) is selected.

During slave-mode operations, system memory access is limited to word boundaries (even addresses) for the 16-bit channels, whereas the 8-bit channels can access memory on either byte or word boundaries. The channel arbitration can be changed by reprogramming the 8237A chips, but the system is configured with the 16-bit channels on top of the 8-bit channels. Once an access is granted to a particular channel, that channel has control of the bus until it is ready to relinquish it to another channel.

In the master mode, the DMA controller provides only the device acknowledge signal in response to a DMA request, and the peripheral device then gains control of the bus by activating the MASTER- bus line to the DMA controller and generating the system address and the I/O or memory strobe. In this mode, the master device can use the refresh signal to perform its own memory refresh operations.

Memory refresh cycles can occur at 15-microsecond intervals (see paragraph 2.5.1.1 entitled DMA/Refresh Arbiter and Refresh Controller). Therefore, to prevent possible loss of memory refresh, data transfer operations (either slave or master) are limited to durations of 15 microseconds.

2.5.1.1 DMA/Refresh Arbiter and Refresh Controller. During normal system operations, the MPU has control of the system bus. However, on receiving a request from either the DMA controller or the refresh controller, the DMA/refresh arbiter removes bus control from the MPU and grants it to the requesting controller.

When either the DMA controller or the refresh sequence controller generates a request (DMARQ or LRFQ-, respectively), the refresh arbiter responds by generating the HOLD signal to the MPU and an acknowledge (DAK or RAK-) signal to the requesting controller after the MPU has activated HOLDA. This places the MPU in a hold condition and grants control of the system bus to the requesting controller. After completing its system bus cycles, the requesting controller relinquishes bus control by releasing the request. This signals the arbiter to release the MPU from its hold state.

To eliminate conflicts between simultaneous DMA and refresh requests, the refresh arbiter samples DMARQ and LRFQ- on alternate rising edges of the 24-megahertz system clock. Thus, the next rising clock edge following activation of the requests determines which of the requests is granted. Following power-up or after each bus-grant cycle, the first rising edge of the 24-megahertz system clock samples the LRFQ-.

During execution of certain instructions, which must not be interrupted by pending hold requests, the MPU chip can prevent the DMA controller or the refresh controller from gaining control of the bus by activating LOCK- to the refresh sequence controller. When active, this signal prevents the refresh arbiter from generating HOLD or either of the acknowledge signals.

The dual mode refresh generator generates special bus cycles to refresh the system dynamic random-access memory (DRAM). In response to an active RAK- from the refresh arbiter, the generator activates the REFRESH- control line and generates a memory read cycle. The active REFRESH- line enables an 8-bit refresh address onto the lower part of the system bus and enables the refresh portion of the LS612 page register. On completion of the memory cycle, the refresh address is incremented and saved for the next refresh cycle while the page register value remains constant.

Refresh cycles can occur at 15-microsecond intervals or as 8-cycle bursts at 120-microsecond intervals. The system software selects this optional burst-refresh operation by writing a 1 to ID1 at I/O port address 68H.

2.5.1.2 Memory Decode Logic. The memory decode logic generates control signals for the memory banks and some other miscellaneous control signals.

The memory bank decode logic generates eight sets of memory control signals from a decode of address bits MA19 through MA21. These signals include the column address strobe (CAS-), the high and low write enable (WEH- and WEL-) signals, and the high and low data buffer enable (MDH- and MDL-) signals. The decodes for memory banks zero and one reside on the main logic board, while those for memory banks two through seven are located on the 3-megabyte memory expansion board.

The miscellaneous decodes are as follows:

* G1A- -- This line indicates that the current cycle is an access to the TI memory space and that the memory controller should generate a row/column address cycle.

* TIVID- -- TI compatible video. This line enables 16-bit cycles for the alphagraphics video (AGV) board.

* PCVDET- -- PC-AT video detect. This line detects accesses to the AGV memory space.

* YL -- This line indicates that address lines MA17 and MA18 should be inverted to interchange the PC-AT and TI video memory spaces.

* 64KSEL- -- 64K select. This line switches the DRAM address multiplexer to the 8-bit addressing mode for the 64K DRAMs in bank 1.

* 1MB- and 1MB+ -- These lines become active for memory accesses below the 1-megabyte address range.

2.5.1.3 Memory Cycle Generation Logic. The memory cycle generation logic provides the undecoded DRAM control strobes, the DRAM bank address, and the DRAM row/column address. The logic contains the following circuits:

* Input signal chopper

* Shift register pulse combiner

* Row address strobe (RAS) forming gate

* Bank address latch

* DRAM address multiplexer

The first three circuits function as a synchronous delay line and pulse forming network that generates the following signals:

* Row address strobe (RAS)
* Column address strobe (CAS-)
* Multiplexer select (MUX)
* Data buffer enable (MDH- and MDL-)
* Write enable (WE-)
* Address latch enable (373EN)

The input signal chopper uses the 12-megahertz system clock (12MHZ) to convert the MPU bus cycle status signals (S0 and S1) to short pulses during the beginning of a memory cycle. The resulting signals (RDOUT1-, RDOUT2-, WROUT1-, and WROUT2-) are then directed to the RAS forming gate, which uses them to generate RAS. RDOUT1- and WROUT1- are also directed to a PAL shift register, which uses them to generate other strobes.

The other circuits latch the DRAM bank address and bus buffer direction signals and handle the DRAM row and column address multiplexing. During refresh cycles, the DRAM address multiplexer shifts the 8-bit refresh address to allow refreshing of the 3-megabyte expansion memory board.

2.5.1.4 Parity Error Logic. This logic processes parity errors during CPU and DMA accesses to the 3-megabyte expansion memory board. During memory write operations, the logic generates a parity syndrome bit, and for memory read operations, it detects odd parity errors. This parity-error detection is disabled during DRAM refresh operations and can be triggered artificially by the diagnostic software.

High-byte and low-byte parity generation and error-detection functions are independent of each other. Parity-error detection causes the bank address and the high/low bank enable bits to be clocked into a register for subsequent reading by error-recovery software. The parity-error generator then produces a nonmaskable interrupt (NMI) to the MPU. The system software can subsequently clear the NMI.

2.6 I/O SUBSYSTEM

The I/O subsystem decodes ten I/O address lines for the I/O devices on the main logic board. To ensure correct transfer of data to 8-bit I/O devices during byte-wide I/O transfer operations, the CPU data buffers place the active data byte on the low byte of the system data bus. The I/O subsystem also includes various output latches and the input buffer bit assignments and their uses.

2.6.1 I/O Decode Logic

The I/O decode logic consists of an ALS138 decode/multiplexer, three I/O decode PALs, and the serial/parallel port decode PAL. Refer to Appendix D for the PAL device programming tables.

2.6.2 Real-Time Clock (RTC) and Nonvolatile RAM

The nonvolatile RAM and the RTC store the system configuration information described in the BUSINESS-PRO Software Technical Reference Manual. In addition, the RTC provides normal RTC services for the system. A 6-volt battery pack supplies backup voltage to these chips to ensure that they remain operational in the absence of system power. The following paragraphs describe these circuits.

2.6.2.1 Battery Circuit. The 6-volt battery pack (between terminals 1 and 4 of the battery connector) is connected in parallel with the +5 volt supply. The series diodes (CR3 and CR5) drop the battery voltage to +4.8 volts for application to the nonvolatile RAM and the RTC.

Under normal operating conditions, the nonvolatile RAM, the RTC, and the CD4069 inverter receive their Vcc from the +5 volt power supply line via transistor Q3. Under these conditions, the inverter holds the nonvolatile RAM and RTC enable (NVENAB-) signal active (low).

In the event of a power loss or power shutdown, the 6-volt battery pack assumes the role of Vcc supply for the nonvolatile RAM and the RTC. During this transition period, RES- becomes active, and the inverter drives NVENAB- high to disable the nonvolatile RAM and the RTC outputs. Once the shutdown is complete, RES- deactivates, and the battery pack holds NVENAB- inactive via pullup resistor R45.

A second function of inverter U51 is to act as a buffer during the power-loss transition period to prevent glitches on the RES- line from momentarily activating NVENAB-.

2.6.2.2 Nonvolatile RAM. The HM6116-LP supplies 2 kilobytes of nonvolatile memory for storing system configuration information. The MPU uses 2048 I/O port addresses to access this nonvolatile RAM, which cannot be accessed by any other device, including a bus master. The 2048 I/O port addresses do not appear on the expansion bus. That is, the I/O strobes are inhibited when this memory space is recognized. Therefore, devices that ignore the upper I/O port addresses are not activated. The 2 kilobytes of CMOS RAM may also be disabled by software (I/O port 68H, bit 2). The BUSINESS-PRO Software Technical Reference Manual defines the nonvolatile RAM I/O port addresses.

2.6.2.3 Real-Time Clock. The MC146818 chip contains the RTC and 64 bytes of CMOS RAM. The RTC uses 14 bytes of this RAM for its internal operations, while the remaining 50 bytes are reserved for system configuration information. The RTC uses the same port for both addresses and data. Therefore, an access to the internal RAM requires that two steps be performed in the following order:

1. The RAM address to be accessed is placed on the data bus (JD bus) and an OUT instruction is sent to port 70H.

2. For a write access, the data is placed on the JD bus, and a second OUT instruction is sent to port 71H. For a read access, an IN instruction is sent to port 71H. This returns the data from the selected RAM address to the arithmetic-logic (AL) register of the MPU.

Table 2-4 lists the RTC's internal RAM addresses and the data stored at each address. Addresses 00H through 09H contain ten bytes of date and time information. The remaining bytes contain diagnostic status and system configuration information.

Table 2-4 Real-Time Clock's Internal RAM Addresses

Address	Description
00H	Byte 0 -- Seconds.
01H	Byte 1 -- Seconds alarm.
02H	Byte 2 -- Minutes.
03H	Byte 3 -- Minutes alarm.
04H	Byte 4 -- Hours.
05H	Byte 5 -- Hours alarm.
06H	Byte 6 -- Day of week.
07H	Byte 7 -- Date of month.
08H	Byte 8 -- Month.
09H	Byte 9 -- Year.
0AH	Byte 10 -- Status register A: Bits 0 through 3: Rate selection bits (RS0 through RS3). These bits select a divider output frequency. The system initializes these bits to 0110, which selects a 1.024-kilohertz square-wave output frequency and a 976.562-microsecond periodic interrupt rate.

Table 2-4. Real-Time Clock's Internal RAM Addresses (Continued)

Address	Description
0AH	Bits 4 through 6: The 22-stage divider bits (DV0 through DV2). These bits identify which time-base frequency is being used. The system initializes the divider to a 32.768-kilohertz time base. Bit 7: Update in progress bit (UIP).When high, this bit indicates that the time update cycle is in progress. When low, it indicates that the current date and time are available to be read.
0BH	Byte 11 -- Status register B: Bit 0: Daylight savings enabled bit (DSE). When high, this bit enables daylight savings time. When low, it enables standard time. The system initializes this bit to 0. Bit 1: The 24-hour/12-hour bit. When high, this bit indicates that the hours byte (byte 4) is in the 24-hour mode. When low, it indicates that the hours byte is in the 12-hour mode. The system initializes this bit to 1. Bit 2: Date mode bit (DM). When high, this bit indicates the binary format for the time and date calendar. When low, it indicates the binary coded decimal (BCD) format. The system initializes this bit to 0. Bit 3: Square-wave enabled bit (SQWE). When high, this bit sets the square-wave frequency as set by the rate-selection bits in register A. When low, it disables the square wave. The system initializes this bit to 0.

Table 2-4. Real-Time Clock's Internal RAM Addresses (Continued)

Address	Description
0BH	Bit 4: Update-ended interrupt enabled bit (UIE). When high, this bit enables the update-ended interrupt. When low, it disables the interrupt. The system initializes this bit to 0.
	Bit 5: Alarm interrupt enable bit (AIE). When high, this bit enables the alarm interrupt. When low, it disables the interrupt. The system initializes this bit to 0.
	Bit 6: Periodic interrupt enable bit (PIE). When high, this bit enables the periodic interrupt. When low, it disables the interrupt. The rate bits and divider bits of register A specify the rate at which these interrupts occur. The system initializes this bit to 0.
	Bit 7: Set bit. When high, this bit sets the time update cycle to advance the counts at a rate of one per second. When low, it aborts any update cycle in progress, and the program can initialize the 14 time bytes without any further updates occurring until a 0 is written to this bit.
0CH	Byte 12 -- Status register C:
	Bits 0 through 3: Reserved bits.
	Bits 4 through 7: Flag bits (IRQF, PF, AF, and UF). These are read-only bits that are affected when the AIE, PIE, and UIE interrupts are enabled in register B.

Table 2-4. Real-Time Clock's Internal RAM Addresses (Continued)

Address	Description
0DH	Byte 13 -- Status register D: Bits 0 through 6: Reserved bits. Bit 7: Valid RAM bit (VRB). This is a read-only bit that indicates the condition of the RTC's contents through the power sense pin. A low state of the power-sense pin indicates that the RTC has lost its power (dead battery). When high, the VRB indicates power on the RTC. When low, it indicates loss of RTC power.
0EH	Byte 14 -- Diagnostic status byte: Bits 0 and 1: Reserved bits. Bit 2: Time status indicator. When low, this bit indicates that the time is valid. When high, it indicates that the time is invalid. Bit 3: Fixed disk formatter/drive C initialization status bit. When low, this bit indicates that the formatter and disk drive are functioning properly and that the system can attempt an initial program load (IPL) operation. When high, it indicates that the formatter and/or drive C has failed initialization, thus preventing the system from attempting an IPL. Bit 4: Memory size miscompare bit. When low, this bit indicates that a power-up check has determined that the memory size is the same as that listed in the configuration register. When high, it indicates that the memory size is different.

Table 2-4. Real-Time Clock's Internal RAM Addresses (Continued)

Address	Description
0EH	Bit 5: Incorrect configuration information bit. When low, this bit indicates that the equipment byte (byte 20) contains valid configuration information. When high, it indicates that the information is invalid. Bit 6: Configuration record checksum status indicator bit. When low, this bit indicates that the configuration record checksum is valid. When high, it indicates that the checksum is invalid. Bit 7: RTC power bit. When low, this bit indicates that the RTC has sufficient power. When high, it indicates that the RTC has lost its power.
0FH	Byte 15 -- Shutdown status byte: The power-up diagnostics define the individual bits of this byte.
10H	Byte 16 -- Floppy disk drive type byte: Bits 0 through 3: Second disk drive type. These bits form a 4-bit binary code that defines the type of floppy disk drive that is installed as a second disk. The code definitions are as follows: 0000 -- No disk drive present. 0001 -- Double-sided floppy disk. 0010 -- High-capacity floppy disk. 0011 through 1111 -- Reserved.

Table 2-4. Real-Time Clock's Internal RAM Addresses (Continued)

Address	Description
10H	Bits 4 through 7: First disk drive type. These bits form a 4-bit binary code that defines the type of floppy disk drive installed as the first disk. The code definitions are as follows: 0000 -- No disk drive present. 0001 -- Double-sided floppy disk. 0010 -- High-capacity floppy disk. 0011 through 1111 -- Reserved.
11H	Byte 17 -- Reserved byte.
12H	Byte 18 -- Fixed disk drive type byte: Bits 0 through 3: Second disk drive type. These bits form a 4-bit binary code that defines the type of fixed disk drive installed as a second disk. The code definitions are as follows: 0000 -- No disk drive present. 0001 -- 306 cylinders, 4 heads, landing zone cylinder 305, write precompensation start cylinder 128. 0010 -- 615 cylinders, 4 heads, landing zone cylinder 615, write precompensation start cylinder 300. 0011 -- 615 cylinders, 6 heads, landing zone cylinder 615, write precompensation start cylinder 300. 0100 -- 940 cylinders, 8 heads, landing zone cylinder 940, write precompensation start cylinder 512. 0101 -- 940 cylinders, 6 heads, landing zone cylinder 940, write precompensation start cylinder 512.

Table 2-4. Real-Time Clock's Internal RAM Addresses (Continued)

Address	Description
12H	0110 -- 615 cylinders, 4 heads, landing zone cylinder 615, no write precompensation.
	0111 -- 462 cylinders, 8 heads, landing zone cylinder 511, write precompensation start cylinder 256.
	1000 -- 733 cylinders, 5 heads, landing zone cylinder 733, no write precompensation.
	1001 -- 900 cylinders, 15 heads, landing zone cylinder 901, no write precompensation.
	1010 -- 820 cylinders, 3 heads, landing zone cylinder 820, no write precompensation.
	1011 -- 855 cylinders, 5 heads, landing zone cylinder 855, no write precompensation.
	1100 -- 855 cylinders, 7 heads, landing zone cylinder 855, no write precompensation.
	1101 -- 306 cylinders, 8 heads, landing zone cylinder 319, write precompensation start cylinder 128.
	1110 -- 733 cylinders, 7 heads, landing zone cylinder 733, no write precompensation.
	1111 -- Reserved.
	Bits 4 through 7:
	First disk drive type. These bits form a 4-bit binary code that defines the type of fixed disk drive installed as a first disk. The code definitions are the same as those for the second disk drive (bits 0 through 3 above).
13H	Byte 19 -- Reserved byte.

Table 2-4. Real-Time Clock's Internal RAM Addresses (Continued)

Address	Description
14H	Byte 20 -- Equipment byte: Bit 0: Floppy disk status bit. When high, this bit indicates that a floppy disk drive is installed. When low, it indicates that no floppy disk drives are present. Bit 1: Math coprocessor presence bit. When high, this bit indicates that a coprocessor is installed in the CPU. When low, it indicates that no coprocessor is present. Bits 2 and 3: Unused bits. Bits 4 and 5: Primary display bits. This 2-bit binary code indicates the type of display unit installed as a primary display. The code definitions are as follows: 00 -- Reserved. 01 -- The primary display is connected to the color graphics monitor interface in the 40-column mode. 10 -- The primary display is connected to the color graphics monitor interface in the 80-column mode. 11 -- The primary display is connected to the monochrome display and the printer interface. Bits 6 and 7: Floppy disk drive quantity bit. This 2-bit binary code indicates the number of floppy disk drives installed in the system. The code definitions are as follows: 00 -- One floppy disk drive installed.

Table 2-4. Real-Time Clock's Internal RAM Addresses (Continued)

Address	Description
	01 -- Two floppy disk drives installed. 10 and 11 -- Reserved.
15H-16H	Bytes 21 and 22 -- Low and high base memory bytes. These two bytes indicate the total memory installed and available to the system. Valid sizes are as follows: 0100H -- 256 kilobytes of on-board RAM. 0200H-- 512 kilobytes of on-board RAM. 0280H -- 640 kilobytes total system memory consisting of 512 kilobytes of on-board RAM and 128 kilobytes of expansion board RAM.
17H-18H	Bytes 23 and 24 -- Low and high memory expansion bytes. These bytes indicate the total expansion memory installed and available to the system. Valid sizes are as follows: 0200H -- 512 kilobytes. 0400H -- 1024 kilobytes. 0600H -- 1536 kilobytes.
19H-2DH	Bytes 25 through 45 -- Reserved bytes.
2EH-2FH	Bytes 46 and 47 -- High and low checksum address bytes.
30H-31H	Bytes 48 and 49 -- Low and high memory expansion bytes. These bytes indicate the total expansion memory installed and available to the system. Valid sizes are as follows: 0200H -- 512 kilobytes. 0400H -- 1024 kilobytes. 0600H -- 1536 kilobytes.

Table 2-4. Real-Time Clock's Internal RAM Addresses (Continued)

Address	Description
32H	Byte 50 -- Date century byte. This byte contains the BCD value for the current century.
33H	Byte 51 -- Information flag byte: Bits 0 through 5: Reserved bits. Bit 6: First user message. The setup utility uses this bit to generate a first user message following initial system setup. Bit 7: Memory expansion option bit. When high, this bit indicates that a memory expansion board is installed.
34H-3FH	Bytes 52 through 63 -- Reserved for RTC operations.

2.6.3 Keyboard Interface

The keyboard interface receives serial data from the keyboard and converts it to parallel data for the system. It then generates an interrupt to signal the system that it has a data byte ready for transfer. The keyboard interface also allows a limited number of commands to be sent to the keyboard for diagnostic purposes.

The keyboard controller is an Intel 8042 microprocessor that performs all necessary scan code conversions and data serialization. A switch (SW1, pins 1 to 10) in the keyboard interface logic indicates to the keyboard controller whether the system monitor is monochrome or color. Placing this switch in its closed (ON) position activates the COLOR- signal to the keyboard controller. This signals the controller that a color monitor is installed.

The keyboard connector (J11) provides the following interface signals:

* Pin 1 -- Keyboard clock (KBD CLK) to the keyboard

* Pin 2 -- Serial data (KBD DATA) to and from the keyboard

* Pin 3 -- Not used

* Pin 4 -- Signal ground

* Pin 5 -- Fused +5 volts

* Pin 6 -- MOUSEDATA input from the mouse

* Pin 7 -- Audio output (MONAUD) to the monitor

* Pin 8 -- Signal ground

TI monitors provide convenience connectors that allow the keyboard to be connected to the system via the monitor base. Other monitor manufacturers may not provide this convenience connector, in which case the keyboard must be connected directly to J11 on the main logic board.

2.6.3.1 Receiving Data From the Keyboard. The keyboard sends 11-bit serial frames and a synchronizing clock to the keyboard interface. These frames contain the following bits:

* A start bit

* Eight data bits (one byte)

* An odd parity bit

* A stop bit

On receiving the stop bit, the keyboard controller disables the interface until the system accepts the data byte. If the parity bit is set, the controller automatically sends a RESEND command to the keyboard. If the controller is unable to receive the data correctly, it sets its output buffer contents to FFH and sets its status register parity bit to indicate a receive parity error.

If a keyboard frame transfer takes more than 2 milliseconds, the controller sets its output buffer contents to FFH and sets its status register receive time-out bit to indicate a time-out error. No retries are attempted for this type of error.

2.6.3.2 Sending Data to the Keyboard. The keyboard uses the same 11-bit serial frame format to send data to the keyboard as that used to receive keyboard data.

When a send data byte is available in the keyboard controller, the keyboard must begin clocking the frame within 15 milliseconds, and it must complete its clocking within 2 milliseconds. If the keyboard fails to meet the requirements, the controller sets its output buffer contents to FEH and sets its status register transmit time-out bit to indicate a time-out error.

If a keyboard response to a data transmission contains a parity error, the controller sets its output buffer contents to FEH and activates both the transmit time-out bit and the parity error bit in its status register. No retries are attempted for any transmission error.

2.6.3.3 Keyboard Commands. The keyboard controller responds as indicated to the following valid commands at I/O port 64H:

* Command code 20H -- Read Keyboard Controller Command Byte. The controller places the current command byte in its output buffer.

* Command code 60H -- Write Keyboard Controller Command Byte. The controller places the next data byte to be written to I/O port address 60H in its command byte. The command byte contains the following bits:

  - Bit 0: Enable output-buffer-full interrupt. Setting this bit high causes the controller to generate an interrupt when placing data into its output buffer.

  - Bit 1: Reserved bit (set to 0).

  - Bit 2: System flag. The controller places the value written to this bit in its status register system flag bit.

  - Bit 3: Inhibit override. Setting this bit high disables the inhibit function of the keyboard.

  - Bit 4: Disable keyboard. Setting this bit high drives the keyboard clock low. This disables the keyboard interface and prevents data from being sent or received.

  - Bit 5: PC-AT mode. Setting this bit high programs the keyboard to support the PC-AT interface.

  - Bit 6: PC-AT mode.

  - Bit 7: Reserved bit (set to 0).

* Command code AAH -- Self-Test. This command causes the controller to perform its internal diagnostic tests. If no errors are detected, the controller sets its output buffer contents to 55H.

* Command code ABH -- Interface Test. This command causes the controller to test its keyboard clock and keyboard data lines. The controller then places one of the following test-result codes in its output buffer:

  - 00H: No error detected.

  - 01H: Keyboard clock line stuck low.

  - 02H: Keyboard clock line stuck high.

  - 03H: Keyboard data line stuck low.

  - 04H: Keyboard data line stuck high.

* Command code ACH -- Diagnostic Dump. This command causes the controller to send the following to the system:

  - 16 bytes of controller RAM

  - Current state of input port

  - Current state of output port

  - Controller status word

* Command code ADH -- Disable Keyboard Interface. This command activates bit 4 of the controller's command byte. Activating this bit drives the clock line low so that data cannot be sent or received.

* Command code AEH -- Enable Keyboard Interface. This command clears bit 4 of the controller's command byte to re-enable sending and receiving.

* Command code C0H -- Read Input Port. This command causes the controller to place the data at its input port in its output buffer. This command should be used only when the controller output buffer is empty.

* Command code D0H -- Read Output Port. This command causes the controller to place the data at its output port in its output buffer. This command should be used only when the controller output buffer is empty.

CAUTION

Bit 0 of the controller output port is connected to the system reset line. Writing a 0 to this bit can cause an accidental system reset when executing either the Write Output Port command or the Pulse Output Port command. Therefore, do not write a 0 to this bit.

* Command code D1H -- Write Output Port. This command causes the controller to place in its output port the next byte of data written to I/O port 60.

* Command code E0H -- Read Test Inputs. This command causes the controller to read the keyboard clock and the keyboard data inputs and to place the data in bits 0 and 1, respectively, of the controller output buffer.

* Command codes F0H through FFH -- Pulse Output Port. This command causes the controller to pulse 1 or more of bits 0 through 3 of its output ports low for approximately 6 microseconds. Setting any one of command bits 0 through 3 low, indicates that its corresponding output port bit should be pulsed.

2.6.3.4 Keyboard Interface I/O Ports. The keyboard controller contains an 8-bit input port (P10 through P17), an 8-bit output port (P20 through P27), and a 2-bit test input port (TEST0 and TEST1). The port bit definitions are as follows:

* Inputs P10 through P15 -- Not used.

* Input P16 -- COLOR-. When high, this bit indicates that the primary display is connected to a monochrome interface. When low, it indicates that the primary display is attached to a color graphics interface.

* Input P17 -- Keyboard inhibit. When low, this bit indicates that keyboard operations are inhibited. When high, it indicates that keyboard operations are not inhibited.

* Output P20 -- System reset. When low, this bit initiates a system software reset.

* Output P21 -- Gate A20.

* Outputs P22 and P23 -- Not used.

* Output P24 -- Keyboard interrupt. When high, this bit indicates that the controller output buffer has a data byte ready for transfer.

* Output P25 -- Not used.

* Output P26 -- Keyboard clock output.

* Output P27 -- OUTDATA. Data output to the keyboard.

* Test input TEST0 -- Keyboard clock input.

* Test input TEST1 -- Keyboard data input.

2.6.4 Parallel Printer Port

The printer port (J9) connects 8-bit, parallel data to the printer and control signals between the printer and the printer interface logic.

The STROBE- signal strobes the parallel data bytes (DATA0 through DATA7) into the printer. The printer then activates the BUSY signal to indicate to the CPU that it is busy and cannot accept another character. Upon completion of the current printing operation (printing the received character), the printer deactivates BUSY and momentarily activates the acknowledge (ACK-) signal. The rising edge of ACK- generates an interrupt to the CPU if the interrupt enable (INTREN) line is active.

When operating in the PC-AT mode (TI/IBM set low), switch 2 (SW1, pins 2 to 9) sets the parallel port as either port 1 (SW1 open) or port 2 (SW1 closed). In TI mode this parallel port is at I/O address 01H, 02H, and 03H.

To allow normal data flow to the printer after reset, the printer data latch at address 02H for the TI mode or address 378H (or 278H if configured as port 2) for the PC-AT mode is enabled. PAL device U85 decodes these addresses to generate PARDAT-. I/O write signal YIOW- and I/O read signal BIOR- enable PARDAT- through two sections of OR gate U91 to generate PDATW- and PDATR-, respectively. PDATW- strobes data from the ID bus onto the DATA bus during a write operation, and PDATR- enables data from the DATA bus onto the ID bus during a read operation. This loopback arrangement allows the software to read the last byte of data sent to the printer.

Unique data can be read from the printer by disabling the output of data latch U86 while it is reading from the DATA bus. This is done by setting bit 7 of I/O port 68 high, thus deactivating printer data enable signal PTRDATEN-. The source of any data read during this time is the option device connected to the parallel port.

Some control and status signals for the TI mode and the PC-AT mode are of different polarities and/or bit assignments. Appendixes B and C contain the I/O maps for the TI and PC-AT modes, respectively.

Table 2-5 lists and describes the printer port input and output signals and shows the pin assignments for the 25-pin main logic connector (J9) and the 36-pin connector at the other end of the printer cable. The table also describes the functions of each signal.

Table 2-5 Parallel Printer Port Pin Assignments

Signal Name	Function	Source	Port Connector Pin Number	Printer Connector Pin Number
STROBE-	Strobes data into the printer on its falling edge.	System	1	1
DATA0 through DATA7	Data bit	System	2 through 9	2 through 9
ACK-	Indicates that another character can be accepted	Printer	10	10
BUSY	Indicates that another data byte cannot be accepted	Printer	11	11
PAPOUT	Indicates that the printer is out of paper	Printer	12	12
SLOT	Indicates that the printer is on line	Printer	13	13
AUTOFD-	Indicates that the printer is to line feed on carriage return	System	14	14
ERROR-	Indicates a printer error	Printer	15	32
INIT-	Resets printer	System	16	31
SLCTIN-	Always low	System	17	36
	Return		18	33
	Return		19	21
	Return		20	20
	Return		21	23
	Return		22	25
	Return		23	27
	Return		24	29
	Return		25	30

2.6.5 Serial Port

The serial interface is a fully programmable, PC-AT compatible port that provides asynchronous communications between the system and various serial devices such as serial printers, dumb terminals, and mouses. The port can be programmed to add or remove either a start bit, a stop bit, or a parity bit. A programmable baud-rate generator provides operations in the range of 50 through 56 000 bauds (Table 2-6).

The principal elements of the port are an NS16450 communications controller and some line buffers and receivers. Switch 3 (SW1, pins 3 to 8) configures the port as either port 1 (switch 3 open) or port 2 (switch 3 closed). The CPU handles all communications with the serial port options by addressing the appropriate port and setting bits in the modem control register of the controller or reading bits of the modem status register.

CAUTION

> Since the mouse (which is plugged into the system monitor) also uses this port, do not plug any other device into the serial port connector when the mouse is present.

The serial port interface uses a 25-pin, male, D-type connector (J8) located on the BUSINESS-PRO main circuit board. Table 2-6 lists and defines the individual pins of the serial port connector. Pins 9 through 19, 21, and 23 through 25 are not connected.

Table 2-6 RS-232 Serial Interface Divisors Using 1.8432 MHZ Crystal

Desired Baud Rate	Divisor Used to Generate 16X Clock	Error Percentage Between Desired & Actual
56 000 (NOTE 1)	2	2.86
38 400 (NOTE 1)	3	--
19 200 (NOTE 1)	6	--
9 600	12	--
7 200	16	--
4 800	24	--
3 600	32	--
2 400	48	--
2 000	58	0.69
1 800	64	--
1 200	96	--
600	192	--
300	384	--
150	768	--
134.5	857	0.058
110	1047	0.026
75	1536	--
50	2304	--

NOTE:

1. Not supported by ROM.

Table 2-7 Serial Port Pin Assignments

Pin	Source	Definition
1	System	Chassis ground
2	System	Transmit data (TXDAT)
3	Option	Receive data (RXDAT)
4	System	Request-to-send (RTS)
5	Option	Clear-to-send (CLTSD)
6	Option	Data-set ready (DSRD)
7	System	Logic ground
8	Option	Data carrier detect (CARDT)
20	System	Data terminal ready (DTR)
22	Option	Ring indicator (RI)

The following paragraphs describe the various serial port controller input and output signals.

2.6.5.1 Clear-to-Send Signal. The clear-to-send (CLTSD) signal is an input signal that indicates that the option connected to the serial port is ready to accept data from the system. The CPU can test the condition of this signal by reading bit 4 of the modem status register. Bit 0 of this register indicates whether the condition of CLTSD has changed since the last reading.

2.6.5.2 Data-Set Ready Signal. The data-set ready (DSRD) signal is an input signal indicates that the option is ready to establish a communication link for the purpose of exchanging data with the system. The CPU can test the condition of this signal by reading bit 5 of the modem status register. Bit 1 of this register indicates whether the condition of DSRD has changed since the last reading.

2.6.5.3 Data Carrier Detect Signal. The data carrier detect (CARDT) signal is an input signal that indicates that the option has detected a data carrier. The CPU can test the condition of this signal by reading bit 7 of the modem status register. Bit 3 of this register indicates whether the condition of CARDT has changed since the last reading.

2.6.5.4 Ring Indicator Signal. The ring indicator (RI) signal is an input signal that indicates that the option has detected a telephone ringing signal. The CPU can test the condition of this signal by reading bit 6 of the modem status register. Bit 2 of this register indicates whether RI has changed from its active state to its inactive state since the last reading.

2.6.5.5 Data Terminal Ready Signal. The data terminal ready (DTR) signal is an output signal that indicates to the option that the system is ready to communicate. The CPU activate DTR by programming bit 0 of the modem control register to its active condition. A system reset operation sets this bit to its inactive state.

2.6.5.6 Request-to-Send Signal. The request-to-send (RTS) signal is an output signal that informs the option that the system is ready to send data. The CPU can activate RTS by programming bit 1 of the modem control register to its active condition. A system reset operation sets this bit to its inactive state.

2.6.6 Timing Services

The BUSINESS-PRO main logic board provides separate timers for TI and PC-AT operations. These timers are identical except that the PC-AT compatible timer has a readable status register and is accessible in both modes, whereas the TI compatible timer can only be accessed in the TI mode. The following paragraphs describe these timers.

2.6.6.1 TI Compatible Timer. This timer uses an Intel 8253-5 counter/timer to provide a programmable speaker oscillator and two programmable interval timers (A and B). The speaker oscillator output and the interrupts generated by timers A and B are masked out for PC-AT operations. Therefore, these signals are valid only for TI operations.

The speaker oscillator clock input is a 1.19-megahertz square wave signal (1.19MHZ). Internal division of this high-frequency input clock provides a range of audio outputs (SPKOUT) to the speaker that can be as low as 18 Hertz. This arrangement (division of the high-frequency input) enhances the quality of the musical tones provided by the oscillator. Another feature of the oscillator is its ability to allow interruption of output tones without the need for reprogramming. This is done by internally gating the input clock with the speaker enable (SPKEN) signal (I/O port address 00H bit 0).

The second timer (timer A) is designed for system applications. Timer A uses a 600-kilohertz clock input to generate the output signal called 53OUT1. The rising edge of 53OUT1 generates an interrupt (INTT1) if in TI mode and the timer A enable (TIMAEN) signal (I/O port address 00H bit 1) is high. Toggling TIMAEN low resets the interrupt and holding it low completely disables the interrupt. INTT1 generates a level-3 (IR03) interrupt to interrupt controller U31. The expansion bus can also generate this level-3 interrupt via expansion bus interrupt signal XIR3.

The third timer (timer B) is for special purpose timing applications. Timer B uses the 600-kilohertz clock input to generate the output signal called 53OUT2. The rising edge of 53OUT2 generates an interrupt (INTT2) if in TI mode and the timer B enable (TIMBEN) signal (I/O port address 00H bit 2) is high. Toggling TIMBEN low resets the interrupt, and holding it low completely disables the interrupt. INTT2 generates a level-2 (IR02) interrupt to interrupt controller U31. The expansion bus can also generate this level-3 interrupt via expansion bus interrupt signal XIR9.

2.6.6.2 PC-AT Compatible Timer. The PC-AT compatible timer uses an Intel 8254-2 counter/timer, which is functionally identical to the 8253-5 device except for its extra read-only status register. All three timing units are clocked by the 1.19-megahertz square wave and their outputs are as follows:

* First timer -- Interrupt IR00. This interrupt is valid for PC-AT operation but is masked out for the TI mode.

* Second timer -- 54OUT1. This output provides timing service for the refresh circuitry.

* Third timer -- 54OUT2. This output provides an audio input to the speaker amplifier for the PC-AT mode. Interruption of output tones may be accomplished without reprogramming the timer. This is done by writing to I/O port address 61H bit 0 (low disabled) GATESPIC signal. This signal (54OUT2) is also masked out for TI operations.

2.6.6.3 Speaker Amplifier. The speaker amplifer is an LM386 operational amplifier that provides an audio output (MONAUD) to the 8-ohm monitor speaker. The amplifier also allows mixing of audio signals from external devices (option expansion boards). These external audio signals are available at expansion bus connector J6 and are applied to the amplifier's summing input. An attenuator network (resistors R40 and R41) ensure that the audio inputs (SKDTB and SPEAKER) do not overdrive the amplifier whose normal gain is 20.

TI monitors provide an internal speaker and some volume-control circuits. If a TI monitor is used, a jumper between terminals E1 and E2 provides a path from the amplifier output to the monitor speaker via keyboard connector J11 and a connector on the monitor base. If a TI monitor is not used, an external speaker cable can be connected between terminals E1 and E3 to provide a path for the amplifier output. In this case, the speaker may be located within the system unit, and some additional circuitry may be required to obtain the desired volume.

2.6.7 Interrupt System

The BUSINESS-PRO interrupt logic can encode 15 separate interrupts to activate any one of the CPU's 15 interrupt routines. A nonmaskable interrupt (NMI) is also available to provide very high-priority interrupts. Table 2-8 lists the interrupt levels and defines their uses in the TI and/or the PC-AT mode. The paragraphs that follow Table 2-8 describe the interrupt system.

Table 2-8 BUSINESS-PRO Interrupt Levels

	PC-AT Mode		TI Mode	
Interrupt Level	Bus Pin	Use	Bus Pin	Use
NMI	A01	Parity error	A01	Parity error or vertical retrace
IR00	N/A	Timer 0	D03	Comm port 1
IR01	N/A	Keyboard	D04	Comm port 2
IR02	N/A	Cascade for IR08 through IR15	B04	XIRQ9 or timer 2
IR08	N/A	RTC	N/A	Not used
IR09	B04	Reserved	See IR02	Not used
IR10	D03	Communication port 1	See IR00	Not used
IR11	D04	Communication port 2	See IR01	Not used
IR12	D05	Reserved	N/A	Not used
IR13	N/A	Math coprocessor	See IR07	Not used
IR14	D07	Winchester drive	See IR06	Not used
IR15	D06	Reserved	N/A	Not used

Table 2-8 BUSINESS-PRO Interrupt Levels (Continued)

Interrupt Level	PC-AT Mode Bus Pin	PC-AT Mode Use	TI Mode Bus Pin	TI Mode Use
IR03	B25	Serial port 2 or tape drive	B25	Serial port 2, tape drive, or timer 1
IR04	B24	Serial port 1	B23	Parallel port 2 or Ethernet
IR05	B23	Ethernet or parallel port 2	B24	Serial port 1 or parallel printer
IR06	B22	Floppy disk	B22 D07	Floppy disk Winchester drive
IR07	B21	Parallel port 1	B21	Parallel port 1, keyboard, or math coprocessor

NOTE:

The interrupt levels in this table are listed in their order of priority. That is, the NMI has the highest priority and IR07 has the lowest priority.

2.6.7.1 Interrupt Levels 0 Through 15. The principal elements of the interrupt logic are two 8259A programmable interrupt controllers, which are cascaded in IBM PC-AT compatible mode and are programmed for edge-sensitive interrupt detection. These devices prioritize the incoming interrupts, provide interrupt masking, and generate an interrupt vector to the CPU during an interrupt acknowledge cycle (INTA- active). A set of OR gates allow some of the interrupt levels to be shared. A set of multiplexers allow switching between TI and PC-AT compatible interrupts.

During the interrupt acknowledge cycle, the interrupt controller's internal decoding logic array enables the contents of the I/O data bus onto the system data bus. This data (which is expected to be the vector from the programmable interrupt controller) cannot be disabled. Therefore, the system can have no other interrupt controllers.

All expansion interrupt signals are terminated by either a pulldown resistor pack to ground or a pullup resistor pack to +5 volts. Generally, the expansion interrupts shared by other interrupts in the TI mode are pulled down, while all others are pulled up.

2.6.7.2 Nonmaskable Interrupt. The main function of the NMI is to detect parity errors in the memory system, but the TI compatible video option board can also use it to indicate the vertical synchronization function if it has been enabled by software. During a nonmaskable interrupt condition, the NMI input to the MPU must remain active (high) for a minimum of 350 nanoseconds to be recognized by the MPU. Also, to ensure proper recognition, the NMI line must remain inactive for a minimum of 350 nanoseconds between consecutive NMIs. In the case of simultaneously occurring NMIs, it is possible that only one will be recognized.

NMIs can be masked out to allow testing of the memory system without possible interruption by parity errors. This can be done by performing an I/O write operation to port address 61H with either bit 2 high (on-board NMIs) or bit 3 high (expansion board NMIs). An I/O write operation to port address 70H with bit 7 high masks out all NMIs.

2.7 EXPANSION BUS INTERFACE

The expansion bus interface board contains the I/O expansion bus interface logic, including all necessary bus connectors and passive termination. The board mounts above the main logic board in the system enclosure and connects to the main logic via a small board called the vertical board. A common wiring harness connects voltages from the power supply to both the bus interface board and the main logic board.

The expansion bus interface provides the capability of adding memory-mapped and I/O-mapped devices to the system. The interface provides seven DMA channels and an interrupt system for devices that require interrupts for efficient operation. It provides 14 slots with fourteen 62-pin connectors and eleven 38-pin connectors. These slots can accommodate any or all of the following option boards:

* Six full-length, PC-AT compatible boards with 16-bit DMA channels.

* Two full-length, PC-AT compatible boards with 8-bit DMA channels.

* Five half-size boards with 16-bit DMA channels.

* One half-size board with an 8-bit DMA channel.

Logic sheet 26 (see Appendix E) shows the expansion bus connectors. Table 2-9 lists the connector pin numbers and their corresponding signals. These signals are defined as follows:

* 6BUS -- Expansion bus clock. This 6-megahertz, 50 percent duty cycle clock provides synchronization for the expansion bus option boards.

* XD0 through XD15 -- Expansion data bus. These bidirectional data lines carry data between the expansion interface and the CPU, the system memory, and the I/O interface.

* WAIT- -- Devices on the expansion bus generate this signal to indicate to the MPU or the DMA controller that the current memory cycle or I/O cycle needs to be extended.

* AEN -- Address enable. The DMA controller activates this line to indicate that it has acquired control of the address bus, the data bus, and the read/write control signals from the MPU.

* XA0 through XA19 -- Expansion address bus. These lines are driven by either the CPU, the DMA controller, or a bus master to address memory and I/O devices within the system. These lines are latched by the falling edge of BALE during CPU driven cycles.

* DRST -- Device reset. A system power-up operation generates this signal to initialize the logic on the expansion bus option boards.

* SPEAKER -- This line carries audio from the expansion bus option boards to the system speaker amplifier. This signal does not appear on the edge connectors but may be jumpered to via connector J6 on the expansion bus interface board.

* 0WS- -- Zero wait states. An option board generates this signal to indicate to the system that it needs no additional wait states to complete the cycle. The minimum default for any device on the I/O bus is one wait state.

* MWTC- and LMWTC- -- Memory write control and lower memory write control. When active (low), these lines indicate that a memory write operation is in progress. MWTC- is active for all memory write cycles, while LMWTC- is active only for write cycles to the lower 1-megabyte memory space. These signals can be masked by software.

* MRDC- and LMRDC- -- Memory read control and lower memory read control. When active (low), these lines indicate that a memory read operation is in progress. MRDC- is active for all memory read cycles, while LMRDC- is active only for read cycles to the lower 1-megabyte memory space. These signals can be masked by software.

* IOWC- -- I/O write control. When active, this line indicates that an I/O write operation is in progress.

* IORC- -- I/O read control. When active, this line indicates that an I/O read operation is in progress.

* 14.3MHZ -- This 14.318-megahertz (70-nanosecond period, 50 percent duty cycle) clock is provided to accommodate any PC-AT compatible option boards that may require it.

* BA17 through BA23 -- Upper address lines. These lines extend the addressing capability of the expansion address bus to 16 megabytes. These lines are not latched during MPU cycles, and the active (high) state of BALE can be used to guarantee their validity. I/O options latch these lines on the falling edge of either BALE or address enable (AEN) during DMA cycles.

* BALE -- The CPU uses this line to indicate that it is placing a valid address on the address bus. When used in conjunction with AEN, this signal indicates that the address is valid. BALE is forced high during DMA and refresh cycles.

* NMI- -- Nonmaskable interrupt. The nonmaskable interrupt signal logic uses this signal to generate an NMI input to the MPU. This signal normally indicates a system parity error condition.

* IRQ3 through IRQ7 and IRQ9 through IRQ15 -- An I/O device uses these lines to indicate to the CPU that the device requires attention. In the event that more than one device requires service at the same time, IRQ9 through IRQ15 are cascaded from a slave interrupt controller at level 2. Thus, these devices have a higher priority than the direct input devices at interrupt levels IRQ3 through IRQ7.

* DRQ0 through DRQ3 and DRQ5 through DRQ7 -- DMA request. When active (high), these lines indicate to the DMA controller that a peripheral device requires attention. Each of these lines is associated with 1 of 7 DMA channels. Channels 0 through 3 provide 8-bit data transfers; channels 5 through 7 provide 16-bit data transfers.

* DACK0- through DACK3- and DACK5- through DACK7- -- DMA acknowledge. The DMA controller uses these lines to acknowledge requests from peripheral devices. Each of these lines is associated with one of the 7 DMA channels.

* T/C -- Terminal count. The DMA controller activates this line during a DMA data transfer operation to indicate that the last data byte has been sent.

* REFRESH- -- The DMA controller or bus master activates this line to indicate that a memory refresh cycle has been requested or is in progress.

* XBHE- -- Expansion bus high enable. The falling edge of BALE latches this signal to indicate that an upper data bus (XD8 through XD15) transfer operation is in progress.

* MASTER- -- An external bus master that desires to gain control of the system, activates this line after activating its associated DRQ line and receiving the appropriate DACK-. If the bus master requires more than 15 microseconds to complete its operation, it must also gain control of the system memory refresh to prevent possible corruption of system memory. The presence of a coprocessor in the CPU limits DMA (master) cycles to 500 microseconds.

* MEM16- -- An option board generates this signal to indicate to the system that it is capable of performing 16-bit memory data transfer operations.

* IO16- -- An option board generates this signal to indicate to the system that it is capable of performing 16-bit I/O data transfer operations.

Table 2-9 Expansion Bus Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
A01	NMI-	B01	GND	C01	XBHE-	D01	MEM16-
A02	XD7	B02	DRST	C02	BA23	D02	IO16-
A03	XD6	B03	+5V	C03	BA22	D03	IRQ10
A04	XD5	B04	IRQ9	C04	BA21	D04	IRQ11
A05	XD4	B05	-5V	C05	BA20	D05	IRQ12
A06	XD3	B06	DRQ2	C06	BA19	D06	IRQ15
A07	XD2	B07	-12V	C07	BA18	D07	IRQ14
A08	XD1	B08	0WS-	C08	BA17	D08	DACK0-
A09	XD0	B09	+12V	C09	MRDC-	D09	DRQ0
A10	WAIT-	B10	GND	C10	MWTC-	D10	DACK5-
A11	AEN	B11	LMWTC-	C11	XD8	D11	DRQ5
A12	XA19	B12	LMRDC-	C12	XD9	D12	DACK6-
A13	XA18	B13	IOWC-	C13	XD10	D13	DRQ6
A14	XA17	B14	IORC-	C14	XD11	D14	DACK7-
A15	XA16	B15	DACK3-	C15	XD12	D15	DRQ7
A16	XA15	B16	DRQ3	C16	XD13	D16	+5V
A17	XA14	B17	DACK1-	C17	XD14	D17	MASTER-
A18	XA13	B18	DRQ1	C18	XD15	D18	GND
A19	XA12	B19	REFRESH-				
A20	XA11	B20	6BUS				
A21	XA10	B21	IRQ7				
A22	XA9	B22	IRQ6				
A23	XA8	B23	IRQ5				
A24	XA7	B24	IRQ4				
A25	XA6	B25	IRQ3				
A26	XA5	B26	DACK2-				
A27	XA4	B27	T/C				
A28	XA3	B28	BALE				
A29	XA2	B29	+5V				
A30	XA1	B30	14.3MHZ				
A31	XA0	B31	GND				

Section 3

Power Supply

3.1 POWER SUPPLY OUTPUT VOLTAGES

This section contains tabulated information about the BUSINESS-PRO computer's power supply output voltages. The nominal output voltages of the power supply are listed in Table 3-1.

3.2 BUSINESS-PRO POWER CONSUMPTION

Table 3-2 is a list of the basic electrical components that make up the BUSINESS-PRO, along with the amount of power consumed by each item.

Nominal Output Voltage	Average Maximum Current	Maximum Surge Current	Tolerance (Percent)	Peak-to-Peak Ripple
+5.1 Vdc (Reg)	25.0 Amperes		+3, -2	50 millivolts
+12.0 Vdc (Reg)	7.5 Amperes	10.8 Amperes	+/- 5	100 millivolts
-12.0 Vdc	0.8 Amperes		+/- 8	100 millivolts

Table 3-1 Power Supply Nominal Output Voltages

Table 3-2 Power Configuration Table

Device	Power Consumed -- Amperes (Typical) 5-volt	12-volt	-12-volt	Power	Slot
Main Logic Board	5.50	0.05	0.05	18.7	
Fan		0.30		3.6	
3 Megabyte RAM	1.50			7.5	
Mouse	0.25			2.0	
Keyboard	0.40			2.0	
PC-AT CRT Controller	1.50			7.5	F1
TI CRT Controller	1.50			7.5	F2
Speech	1.50	0.20	0.10	11.1	F3
LAN	1.70			8.5	F4
Tape Controller	1.50			7.5	F6
Winchester Controller	1.00			5.0	H1
Floppy Controller	0.75			3.8	H2
TI Communication	0.31	0.05	0.05	2.8	H4
TI Communication	0.31	0.05	0.05	2.8	H5
Winchester Drive	1.00	1.50		23.0	P1/P2
Winchester Drive	1.00	1.50		23.0	P3/P4
Cartridge Tape	1.00	2.00		29.0	P5
Floppy Disk	0.50	1.00		14.5	P6
Totals	21.37	6.65	0.25	179.8	

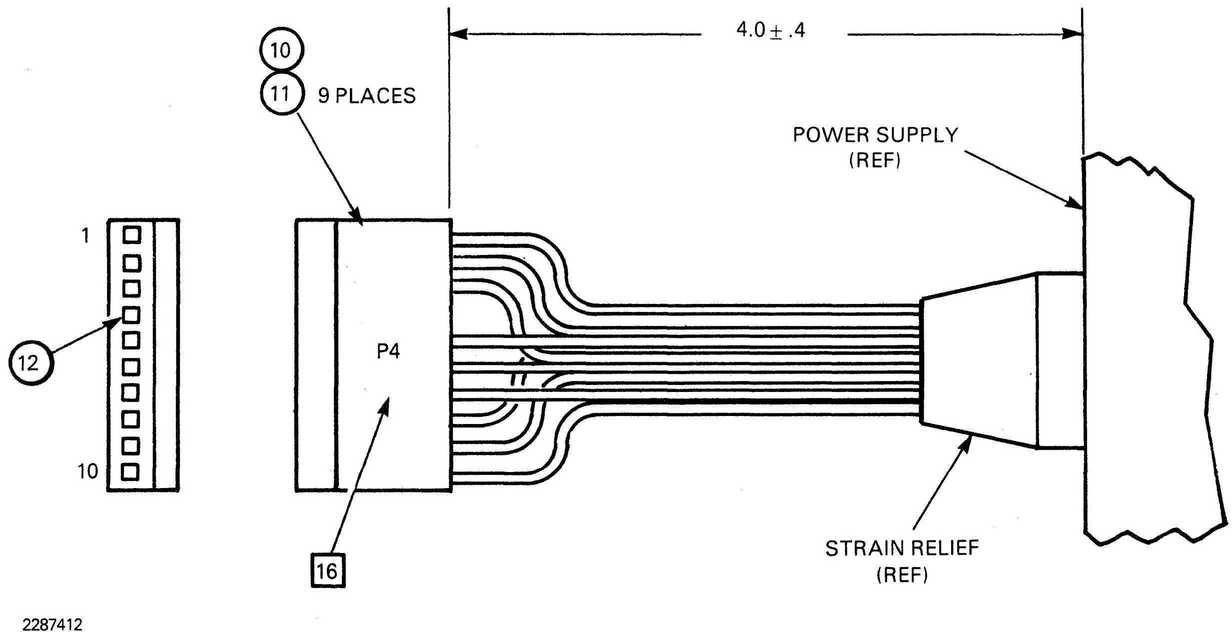

Figure 3-1 Main Logic Board Power Connector

Table 3-3 Main Logic Board Power Connector Pinouts

Pin Number	Output	Wire Color
1	+5 Vdc	Red
2	+5 Vdc	Red
3	+5 Vdc	Red
5	+12 Vdc	Yellow
6	Ground	Black
7	+5 Vdc	Red
8	Ground	Black
9	Ground	Black
10	Ground	Black

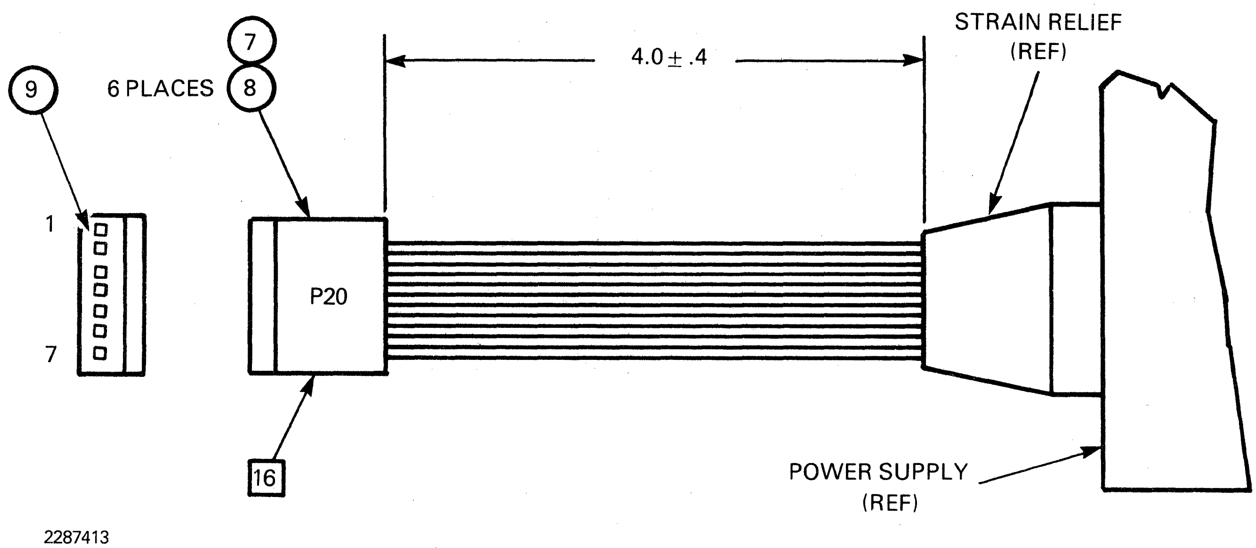

Figure 3-2 Expansion Bus Board Power Connector

Table 3-4 Expansion Bus Board Power Connector Pinouts

Pin Number	Output	Wire Color
1	+12 Vdc	Yellow
3	+5 Vdc	Red
4	Ground	Black
5	-12 Vdc	Green
6	+5 Vdc	Red
7	Ground	Black

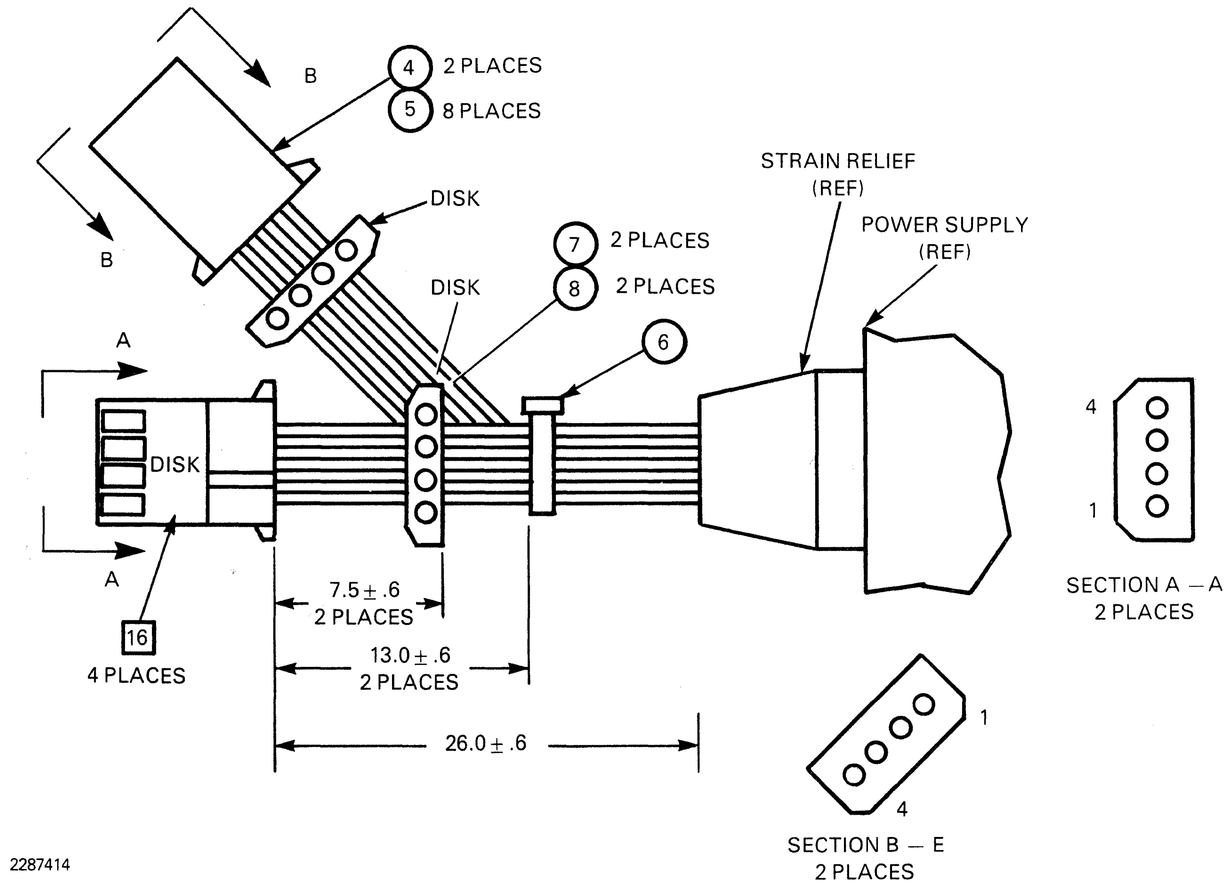

Figure 3-3 Disk Drives 1 Through 4 Power Connector

Table 3-5 Disk Drives 1 Through 4 Power Connector Pinouts

Pin Number	Output	Wire Color
1	+12 Vdc	Yellow
2	Ground	Black
3	Ground	Black
4	+5 Vdc	Red

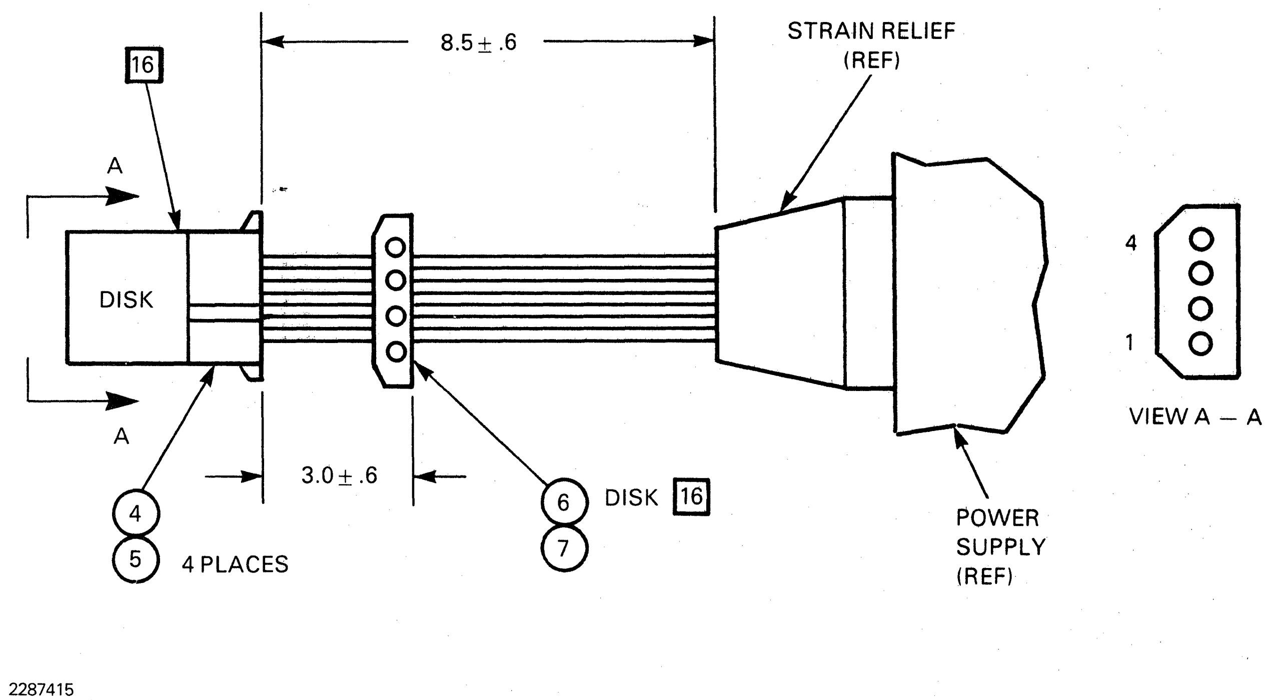

Figure 3-4 Disk Drives 5 and 6 Power Connector

Table 3-6 Disk Drives 5 and 6 Power Connector Pinouts

Pin Number	Output	Wire Color
1	+12 Vdc	Yellow
2	Ground	Black
3	Ground	Black
4	+5 Vdc	Red

Section 4

Keyboard

4.1 GENERAL

The BUSINESS-PRO keyboard provides both TI Professional Computer (TIPC) and IBM Personal Computer AT (PC-AT) capabilities. This easy-to-use keyboard includes the following advanced design features:

* Typamatic transmission
* N-key rollover
* Programmable key click
* Improved tactile response
* Standard typewriter layout
* Dedicated function keys
* Separate cursor-control keypad
* Numeric keypad
* Variable tilt adjustment

The keyboard also features a total of 100 keys. These can be expanded to a total of 144 by removing dummy keycaps from the unit and replacing them with normal keycaps. Special software can be used to program these additional keys.

The following paragraphs describe some of the keyboard features.

4.1.1 Typamatic Transmission

Typamatic transmission is the ability of the keyboard to repeat keycode transmissions continuously when a key is depressed and held down. The frequency at which this occurs depends on the typamatic rate, which can be set by a command from the system (paragraph 4.5.5). The typamatic delay is also programmable, and its purpose is to provide sufficient delay between the time that a key is depressed and the time that typamatic transmission actually begins. This prevents the accidental repetition of characters.

If you hold down more than one key at a time, only the last key depressed repeats at the typamatic rate. When this key is released, the typamatic action stops even if the other keys are still held down.

4.1.2 N-Key Rollover

N-key rollover is the ability of the keyboard to recognize and correctly decode the key depressed most recently regardless of the number of keys currently depressed.

4.1.3 Key Click

The keyboard features an electronic clicker to provide a simulated key click sound. This key click feature is controlled by system commands (paragraph 4.5.1), which can turn the clicker on or off or adjust its volume.

4.1.4 Mode Indicators

The mode indicators are three light-emitting diodes (LEDs) located at the upper right corner of the keyboard. These LEDs indicate the state of the capitals lock (Caps Lock), the numbers lock (Num Lock), and the Scroll Lock keys. Commands from the system turn the LEDs on or off.

4.1.5 Keyboard Buffer

The keyboard buffer is a 16-character, first-in, first-out (FIFO) memory that stores data generated by the keyboard until the keyboard interface is ready to receive it. In anticipation of a Resend command from the system, the keyboard buffer retains a previously transmitted character until the next one is transmitted. If the buffer becomes full, it substitutes an Overrun command (command code 00H) for the seventeenth character. All keystrokes following the overrun condition are lost.

The following commands are transmitted directly (without buffering) as soon as they are generated:

* Command code AAH -- Self-Test OK command
* Command code EEH -- Echo Response command
* Command code FAH -- Acknowledge command
* Command code FDH -- Diagnostic Failure command
* Command code FEH -- Resend command

4.2 KEYBOARD OPERATIONS

After performing a self-test at power-up the keyboard scans the key-switches and sends the scan codes of pressed keys to the keyboard interface in the proper sequence. To ensure proper, fault-free operation, the keyboard also tests its sense amplifier periodically during normal operation. The following paragraphs describe the keyboard operations.

4.2.1 Keyboard Self-Tests

The keyboard performs a self-test at power-up and another one periodically to determine the operational status of the keyboard. Upon self-test completion, the keyboard sends a status command to the system.

4.2.1.1 Basic Assurance Self-Test. The keyboard performs the basic assurance self-test within one second after power-up or upon receiving a Reset command from the system. The basic assurance self-test performs a checksum test on the keyboard read-only memory (ROM) and an addressing test on its random-access memory (RAM). The test also performs an operational check on the keyboard sense amplifier and turns on all three mode-indicator LEDs for 300 milliseconds. Upon self-test completion, the keyboard sends either a Self-Test OK command or a Diagnostic Failure command to the system.

4.2.1.2 Periodic Self-Test. The periodic self-test checks the sense amplifier's response to a known input. If the test fails, the keyboard sends a Diagnostic Failure command to the system. If the test passes, the keyboard sends no command.

4.2.2 Power-Up Sequence

At power-up, the keyboard logic generates a power-on reset, during which the mode-indicator LEDs are turned on for a period of two to three seconds. Immediately after this power-on reset operation, the keyboard begins its basic assurance self-test. During this time, keyboard transmission is inhibited for a period of 300 milliseconds to 9 seconds, after which the keyboard sends a status command to the system. Upon passing the self-test, the keyboard assumes the initial default state and begins its normal key-switch scanning operation. Table 4-1 lists the initial default conditions.

Table 4-1 Initial Keyboard Default Conditions

Function	Default State
Typamatic rate	15 ±3 keycodes per second
Typamatic delay	500 ±10 milliseconds
Operation	Scanning key switches
Key click volume	Off
Mode-indicator LEDs	Off

4.3 KEYBOARD CONNECTOR SPECIFICATIONS

Figure 4-1 shows the keyboard connector pin arrangement. The keyboard connector is a 5-pin DIN connector that provides the required interface signals between the keyboard and the system. A connector at the base of the BUSINESS-PRO monitor provides a convenient connection for the keyboard. Table 4-2 lists the keyboard connector pin assignments.

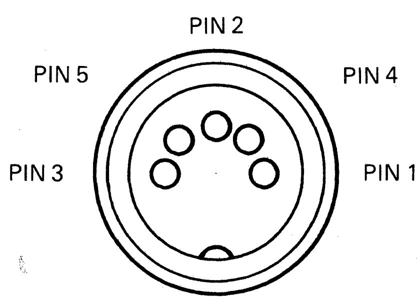

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Figure 4-1 Keyboard Connector Pin Arrangement

Table 4-2 Keyboard Connector Pin Assignments

Pin Number	Function
1	Clock
2	Data
3	Reserved
4	Signal ground
5	5.1 +0.51 volts dc

NOTES:

1. The TTL levels for the data and clock lines are: high -- 2.4 to 5.25 volts; low -- 0.0 to 0.4 volt.

2. The cable shield is connected to chassis.

The following paragraphs describe the keyboard interface lines.

4.3.1 Clock Line

The clock line is a bidirectional line that transfers timing and control information from the system to the keyboard and status information from the keyboard to the system. Open-collector drivers at each end of the clock line enable either the system or the keyboard to control the state of the line.

In its idle condition, the clock line is normally high. When clocking data or commands, the clock has a period of 60 (±5) microseconds with a 50 percent duty cycle. A clock cycle consists of a 30 microsecond period in which the signal is low followed by a 30 microsecond period in which it is high.

4.3.2 Data Line

The data line is a bidirectional line that transfers data from the keyboard to the system and transfers commands from the system to the keyboard. All information transfers (data or commands) are performed in bit-serial fashion. Open-collector drivers at each end of the data line control the direction and state of the line.

4.4 HARDWARE HANDSHAKING PROTOCOLS

The following paragraphs describe the hardware handshaking protocols for keyboard-to-system and system-to-keyboard transmissions.

4.4.1 Keyboard Transmission

Each keyboard transmission consists of an 11-bit frame of serial data that begins with a single-bit, logical-low start element (bit 0) and ends with a single-bit, logical-high stop element (bit 10). The other nine bits (1 through 9) are the 8-bit data byte (DATA0 through DATA7) followed by a single, odd parity bit. Figure 4-2 shows the data frame format.

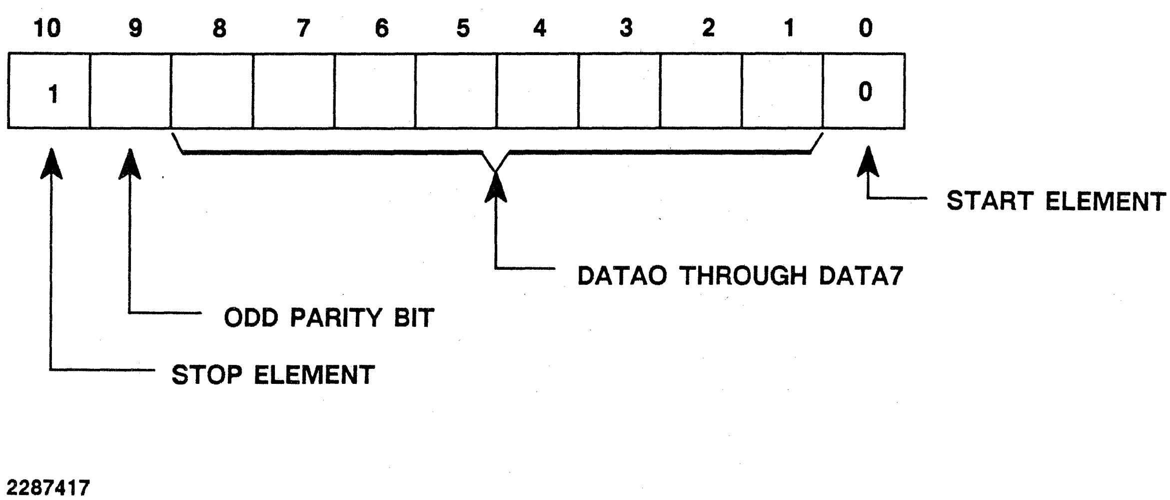

Figure 4-2 Keyboard Data Frame Format

Each key station has a unique make code, which is a two-digit (single-byte) hexadecimal number. The break code for a given key station is identical to its make code, except that it is always preceded by F0H which identifies the code as a a break code. Thus, a break code transmission requires two data frames, whereas a make code transmission requires only one. Figure 4-3 shows the key station numbers and their respective make codes.

Figure 4-3 Key Station/Code Map

1 C3H	2 C2H	3 B9H	4 B8H	5 B7H	6 B6H	7 B5H	8 B4H	9 B3H	10 B2H	11 B1H	12 DFH	13 DEH	14 DDH	15 DCH	16 DBH	17 D9H	18 D8H	19 D4H	20 9CH	21 96H	22 89H	23 88H	24 87H	25 86H	26 85H
27 05H *	28 06H *	29 BAH	30 OEH *	31 16H *	32 IEH *	33 26H *	34 25H *	35 2EH *	36 36H *	37 3DH *	38 3EH *	39 46H *	40 45H *	41 4EH *	42 55H *	43 5DH *	44 66H *	45 D3H	46 9BH	47 95H	48 BAH	49 76H *	50 77H *	51 7EH *	52 84H *
53 04H *	54 0CH *	55 BBH	56 0DH *	57 15H *	58 IDH *	59 24H *	60 2DH *	61 2CH *	62 35H *	63 3CH *	64 43H *	65 44H *	66 4DH *	67 54H *	68 5BH *	5AH *	69 D2H	70 9AH	71 94H	72 8BH	73 6CH *	74 75H *	75 7DH *	76 7CH *	
77 03H *	78 0BH *	79 BCH	80 14H *	81 ICH *	82 1BH *	83 23H *	84 2BH *	85 34H *	86 33H *	87 3BH *	88 42H *	89 4BH *	90 4CH *	91 52H *	92 D7H	93	94 D1H	95 99H	96 93H	97 8CH	98 6BH *	99 73H *	100 74H *	101 7BH *	
102 02H *	103 0AH *	104 BDH	105 12H *	106 BFH	107 1AH *	108 22H *	109 21H *	110 2AH *	111 32H *	112 31H *	113 3AH *	114 41H *	115 49H *	116 4AH *	117 51H *	118 59H *	119 9EH	120 98H	121 92H	122 8DH	123 69H *	124 72H *	125 7AH *	126 79H *	
127 01H *	128 09H *	129 BEH	130 11H *	131 C1H	132 19H *	133 29H *	134 D5H	135 D6H	136 58H *	137 9DH	138 97H	139 91H	140 BEH	141 B0H	142 70H *	143 71H *	144 81H								

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* PC-AT COMPATIBLE KEY SCAN CODS

The keyboard transmits under either of the following conditions:

* Detection of a valid key depression (make code) or a valid key release (break code)

* Recognition of a valid system command

The keyboard supplies the clock that synchronizes the data sent by the keyboard. Each keyboard transmission requires a maximum of 2 milliseconds, and the keyboard samples the clock line at least once every 60 microseconds during the keyboard transmission.

The keyboard responds to each system command or data transmission within 20 milliseconds unless the system prevents a keyboard output. If the keyboard response is invalid or contains a parity error, the system sends the command or data again. In this case, the system does not issue a Resend command.

4.4.1.1 Transmission Process. Figure 4-4 shows a timing diagram for a complete data frame transmission. Simultaneous detection of a high clock line and a high data line signals the keyboard that it can begin a data transmission. Each data transmission requires the following steps:

1. The keyboard places the start element on the data line (sets the data line low).

2. The keyboard pulses the clock low for one half clock period, then changes the clock to its high state to clock in the start element. The clock remains high for one half clock period, thus completing the clock cycle.

3. While the clock is high, the keyboard places the first data bit (DATA0) on the data line.

4. The keyboard performs another clock cycle (as in step 2) to clock in DATA0.

5. The keyboard repeats steps 3 and 4 for each of the remaining data bits (DATA1 through DATA7) and for the parity bit.

6. The keyboard places the stop element on the data line (sets the data line high).

7. The eleventh falling edge of the clock clocks in the stop element, and the system holds the clock line low to indicate that it has received and is processing data.

8. Upon completion of the data processing, the system relinquishes control of the clock line, allowing it to return to its high state. This indicates that the

operation is complete and that another keyboard transmission can begin.

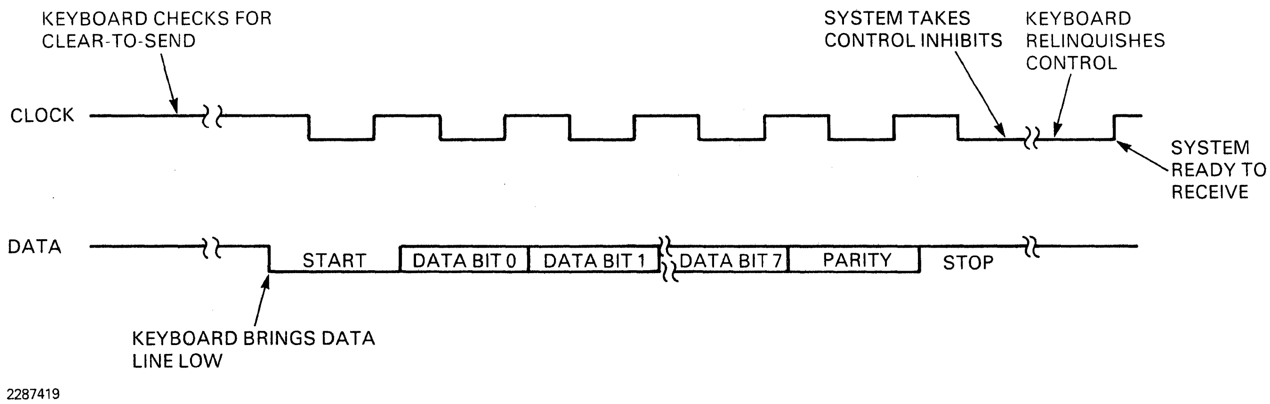

Figure 4-4 Keyboard Transmission Timing -- Completed Transmission

4.4.1.2 Aborted Keyboard Transmission. Figure 4-5 shows a timing diagram for a typical aborted keyboard transmission.

The system can interrupt a keyboard transmission at any time by driving the clock line low and holding it in this state. Between each data bit, the keyboard samples the clock line for a high condition. Detection of a low clock at this time indicates a clock line contention.

If the keyboard detects a clock line contention prior to the rising edge of the tenth clock cycle, the keyboard aborts the transmission by turning off the output device of both its clock line and data line drivers. The aborted data byte then remains in the keyboard buffer from which it can be resent if the system requires.

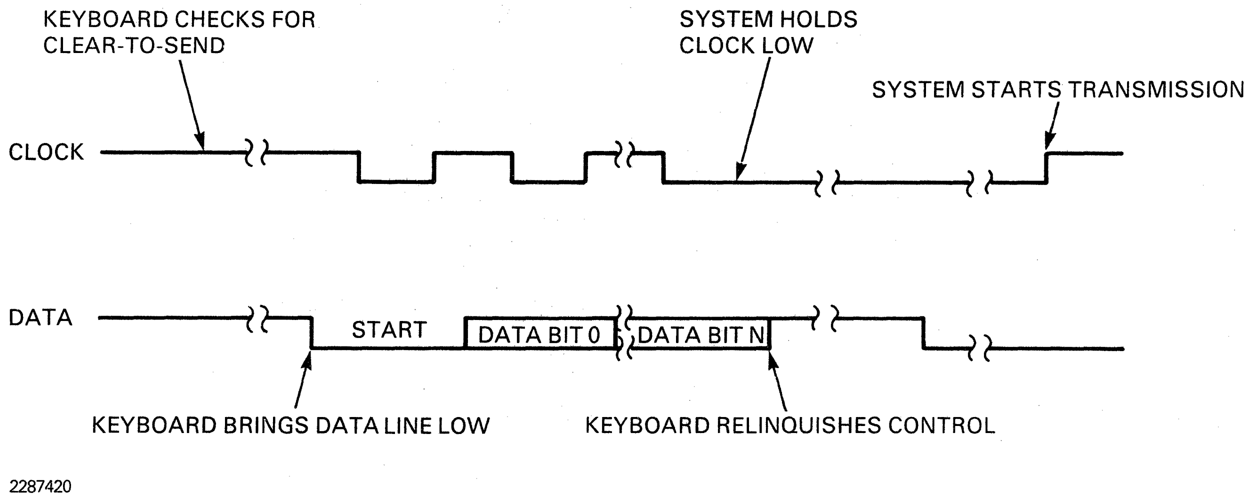

Figure 4-5 Keyboard Transmission Timing -- Aborted Transmission

4.4.1.3 Inhibited Keyboard Transmission. Detection of a low clock line during normal sampling inhibits keyboard transmission. In this case, the keyboard retains any data that is ready to be transmitted in its buffer and relinquishes control of the data and clock lines.

Detection of a high clock line and a low data line also causes any data that is ready to be transmitted to remain stored in the keyboard buffer. In this case, after storing the data, the keyboard prepares to receive a transmission from the system.

4.4.2 System Unit Transmission

Figure 4-6 shows a timing diagram for a typical system unit transmission. A system unit transmission uses the same data frame format as does a keyboard transmission. The keyboard begins clocking the data out of the system unit within 15 milliseconds after initiation of a transmission. Each data frame transmission requires a maximum of 2 milliseconds.

A system unit transmission can occur under either of the following conditions:

* There is no keyboard transmission in progress. This is indicated by the data and clock lines remaining in a high state for longer than one clock period.

* The keyboard is transmitting but has not reached the tenth clock cycle. In this case, the system unit can force an abortion of the keyboard transmission, after which the system transmission can begin.

A system transmission requires the following sequence of events:

1. The system unit sets the clock line low for more than the clock period. The keyboard aborts any transmission that has not reached the rising edge of its tenth clock cycle and inhibits any transmission not already started.

2. The system unit places the start element on the data line (sets the data line low) and holds it in this state while allowing the clock line to go high.

3. After recognizing the start element, the keyboard waits a minimum of one half clock cycle, then sets the clock line low.

4. During the low state of the clock, the system unit places the first data bit on the data line and holds it there until after the next falling edge of the clock. The keyboard samples the data while the clock line is high.

5. Step 4 is repeated until all eight data bits and the parity bit have been transmitted.

6. The system unit places the stop element on the data line (sets the data line high).

7. The keyboard sets the clock line high. Then, while the clock line is high, the keyboard sets and holds the data line low until after the next rising edge of the clock.

8. After generating one more clock period, the keyboard turns off the output device of the clock line driver. This relinquishes control of the clock line.

9. The system unit sets the clock line low and holds it low for more than one clock cycle to inhibit further transmission.

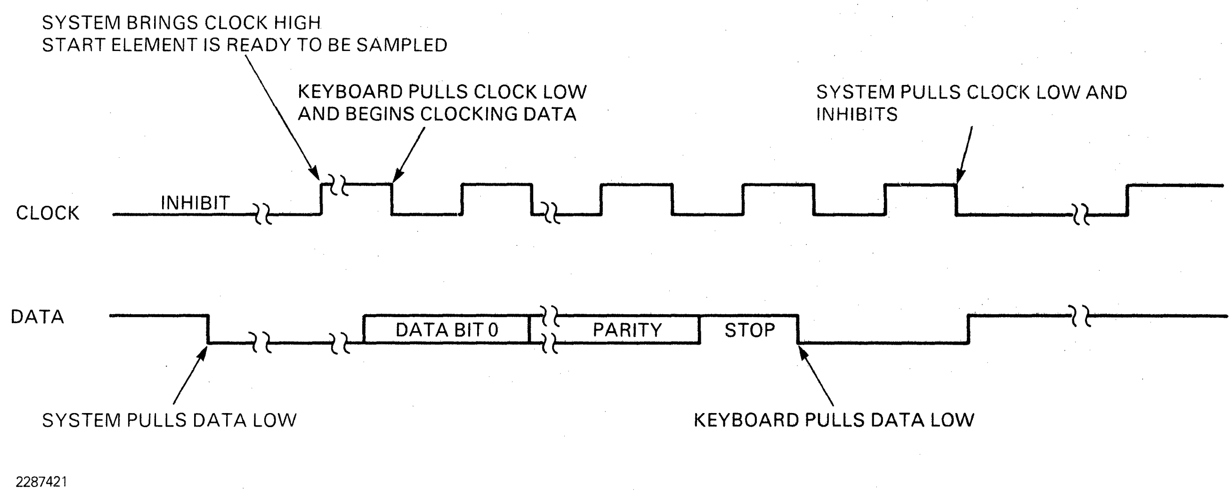

Figure 4-6 System Unit Transmission Timing

4.5 SYSTEM-TO-KEYBOARD COMMANDS

The system-to-keyboard commands are of two general types: single-byte commands and dual-byte commands. The single-byte commands consist of a command code that causes the keyboard to perform a required function. The dual-byte commands are commands, such as the Set Typamatic Rate and Delay command, for which the system must provide an additional byte. This additional byte contains the required data.

The system-to-keyboard command set contains the following commands:

* Command code ECH -- Set Key click Volume
* Command code EDH -- Turn Mode Indicator LEDs On/Off
* Command code EEH -- Echo
* Command code EFH -- No Operation
* Command code F0H -- No Operation
* Command code F1H -- No Operation
* Command code F2H -- No Operation
* Command code F3H -- Set Typamatic Rate and Delay
* Command code F4H -- Enable
* Command code F5H -- Default Disable
* Command code F6H -- Set Default
* Command code F7H -- No Operation
* Command code F8H -- No Operation
* Command code F9H -- No Operation
* Command code FAH -- No Operation
* Command code FBH -- No Operation
* Command code FCH -- No Operation
* Command code FDH -- No Operation
* Command code FEH -- Resend
* Command code FFH -- Reset

The following paragraphs describe the system-to-keyboard commands.

4.5.1 Set Key Click Volume Command

When the keyboard receives the command byte (ECH) of this dual-byte command, it responds by sending an Acknowledge command, then waits for the data byte (Figure 4-7).

The data byte contains one of the following key click volume codes:

* 00 -- Key click off
* 01 -- Low key click volume
* 10 -- Medium key click volume
* 11 -- High key click volume

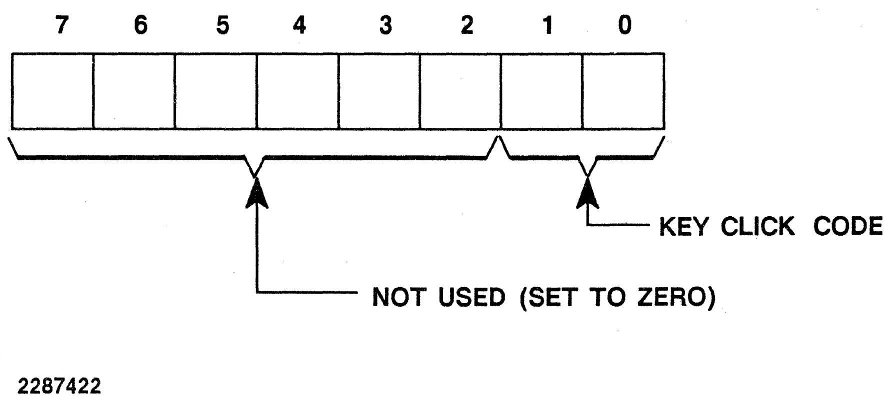

Figure 4-7 Set Key Click Volume Command Data Byte

4.5.2 Turn Mode Indicator LEDs On/Off Command

When the keyboard receives the command byte (EDH) of this dual-byte command, it responds by sending an Acknowledge command, then waits for the data byte (Figure 4-8). The data byte contains three data bits, each of which turns one of the three indicator LEDs either on or off, depending on the state of the bit. A high-level bit turns the associated LED on; a low-level bit turns it off. After receiving the data byte, the keyboard responds by sending an Acknowledge command and setting the indicator LEDs as required by the data bits.

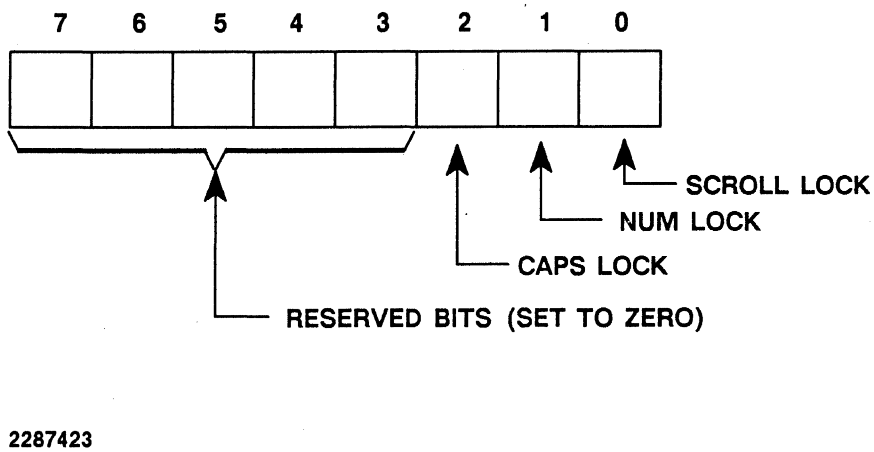

Figure 4-8 Second Byte of the Indicator LED Command

4.5.3 Echo Command

When the keyboard receives the Echo command (EEH), it responds by transmitting the Echo Response command (EEH) back to the system.

4.5.4 No Operation Command

When the keyboard receives one of the eleven No Operation commands, it returns an Acknowledge command to the system and performs no operation other than normal key detection.

4.5.5 Set Typamatic Rate and Delay Command

When the keyboard receives the command byte (F3H) of this dual-byte command, it responds by sending an Acknowledge command, then stops decoding switch closures while waiting for the data byte. The data byte (Figure 4-9) provides the typamatic rate and delay information. Upon receiving the data byte, the keyboard returns a second Acknowledge command then sets the typamatic delay and rate as indicated by the data byte. The delay is 250 milliseconds ±20 percent, times the binary value of bits 5 and 6. The rate can be in the range of 2.0 to 30.0 characters per second, as shown in Table 4-3.

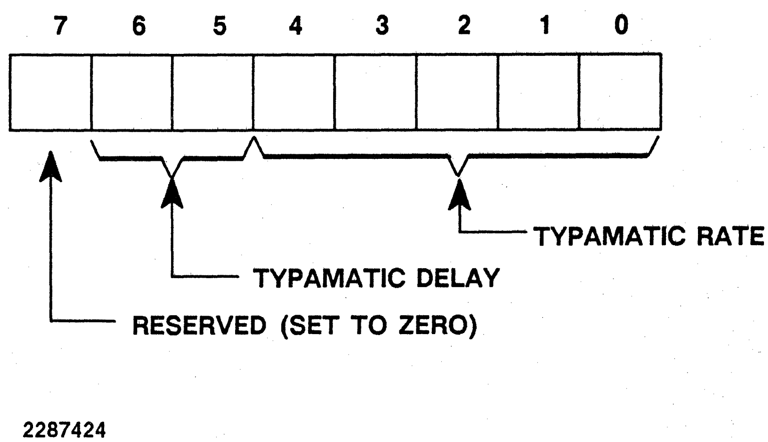

Figure 4-9 Second Byte of the Set Typamatic Rate Command

Table 4-3 Typamatic Rates

Rate Bits	Rate (Changes/Second)	Rate Bits	Rate (Changes/Second)
00000	30.0	10000	7.5
00001	26.6	10001	6.7
00010	24.0	10010	6.0
00011	21.8	10011	5.5
00100	20.0	10100	5.0
00101	18.4	10101	4.6
00110	17.1	10110	4.3
00111	16.0	10111	4.0
01000	15.0	11000	3.7
01001	13.3	11001	3.3
01010	12.0	11010	3.0
01011	10.9	11011	2.7
01100	10.0	11100	2.5
01101	9.2	11101	2.3
01110	8.6	11110	2.1
01111	8.0	11111	2.0

4.5.6 Enable Command

When the keyboard receives an Enable command (F4H), it responds by sending an Acknowledge command, then it begins normal operation (scanning the keycodes).

4.5.7 Default Disable Command

When the keyboard receives the Default Disable command (F5H), it responds by sending an Acknowledge command. The keyboard then clears the keyboard buffer, sets all conditions to their initial default states, stops scanning keycodes, and awaits further instructions.

4.5.8 Set Default Command

When the keyboard receives a Set Default command (F6H), it responds by sending an Acknowledge command. The keyboard then sets all conditions to their initial default states and continues to scan keycodes.

4.5.9 Resend Command

The system issues the Resend command (FEH) in response to a defective data frame from the keyboard. The Resend command must be sent after a keyboard transmission is completed and before the next transmission begins. When the keyboard receives a Resend command, it resends the last byte transmitted unless the last byte was a keyboard-to-system Resend command. In this case, the keyboard sends the byte that was sent immediately prior to the keyboard-to-system Resend command.

4.5.10 Reset Command

When the keyboard receives a Reset command (FFH), it responds by sending an Acknowledge command and waits for the clock and data lines to indicate that the system has accepted the Acknowledge command. The keyboard then performs the basic assurance self-test, sets all conditions to their initial default states, and clears the keyboard buffer.

4.6 KEYBOARD-TO-SYSTEM COMMANDS

The keyboard can send a limited number of commands to the system to indicate certain status information. The keyboard-to-system command set contains the following commands:

* Command code 00H -- Overrun
* Command code AAH -- Self-Test OK
* Command code EEH -- Echo Response
* Command code F0H -- Break Code Prefix
* Command code FAH -- Acknowledge
* Command code FDH -- Diagnostic Failure
* Command code FEH -- Resend

The following paragraphs describe the keyboard-to-system commands.

4.6.1 Overrun Command
The keyboard sends an Overrun command (00H) to indicate to the system that the keyboard buffer is full.

4.6.2 Self-Test OK Command
The keyboard sends the Self-Test OK command (AAH) to indicate successful completion of the basic assurance self-test. The system interprets any other command received while expecting a Self-Test OK command as a keyboard failure.

4.6.3 Echo Response Command
The keyboard sends the Echo Response commmand (EEH) in response to an Echo command (EEH) from the system.

4.6.4 Break Code Prefix Command
The Break Code Prefix command (F0H) is the first byte of a dual-byte sequence. This command-code byte precedes a make-code byte to indicate that the associated key has been released.

4.6.5 Acknowledge Command
The keyboard sends an Acknowledge command (FAH) in response to any valid command except for Echo or Resend. The Acknowledge command indicates that the keyboard has received a command and performed the required function. If the keyboard is interrupted while sending an Acknowledge command, it discontinues the command transmission and accepts the new command.

4.6.6 Diagnostic Failure Command
The keyboard sends the Diagnostic Failure command (FDH) to indicate that either the basic assurance self-test or the periodic self-test has failed.

4.6.7 Resend Command
The keyboard sends the Resend command (FEH) in response to an invalid input or an input containing incorrect parity.

4.7 KEYBOARD CONFIGURATIONS

Figures 4-10 through 4-18 show the keycap configurations that are available for the BUSINESS-PRO keyboard.

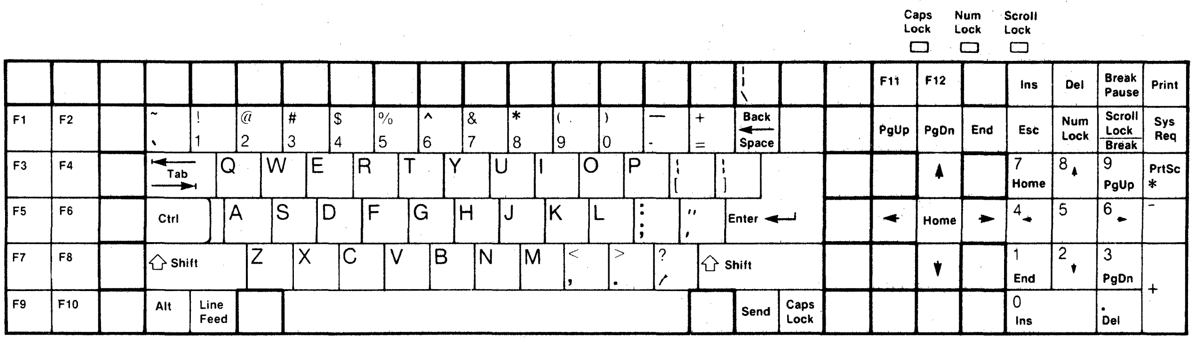

Figure 4-10 Keycap Configuration -- Domestic

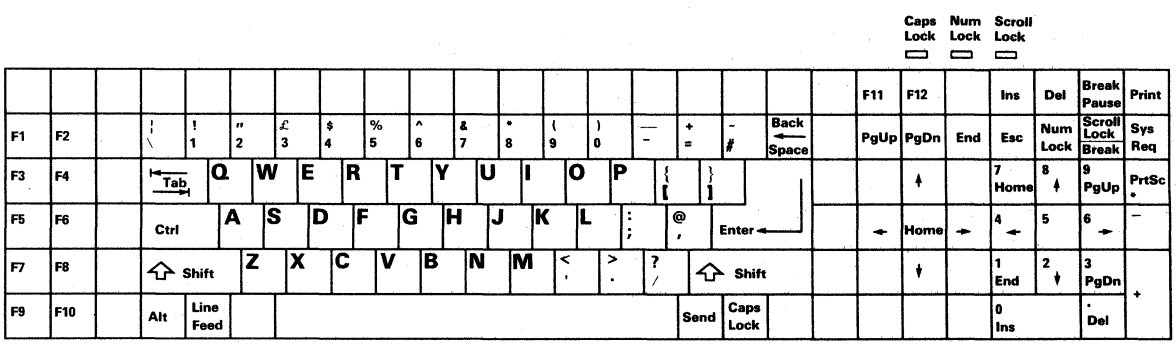

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Figure 4-11 Keycap Configuration -- Germany

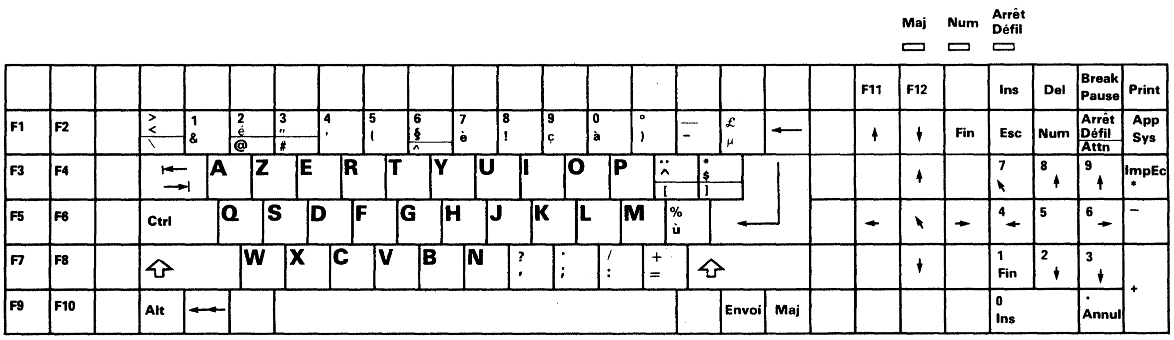

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Figure 4-12 Keycap Configuration -- France

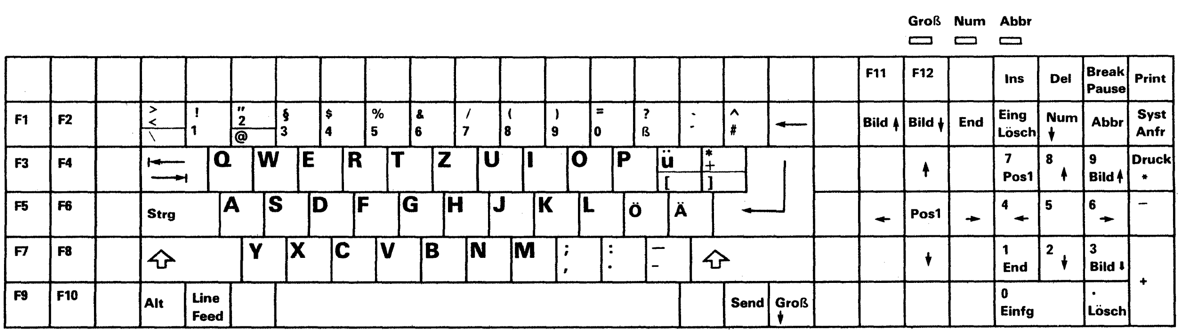

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Figure 4-13 Keycap Configuration -- Italy

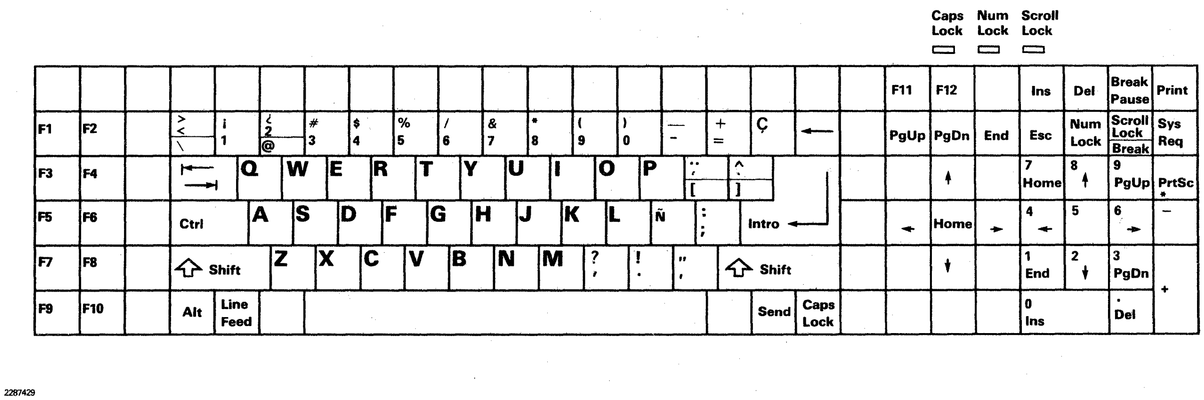


Figure 4-14 Keycap Configuration -- Norway

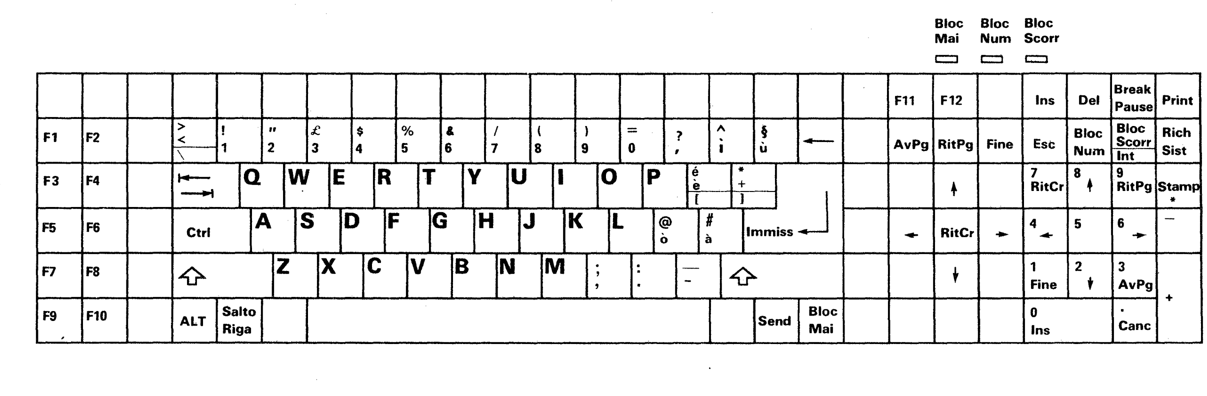
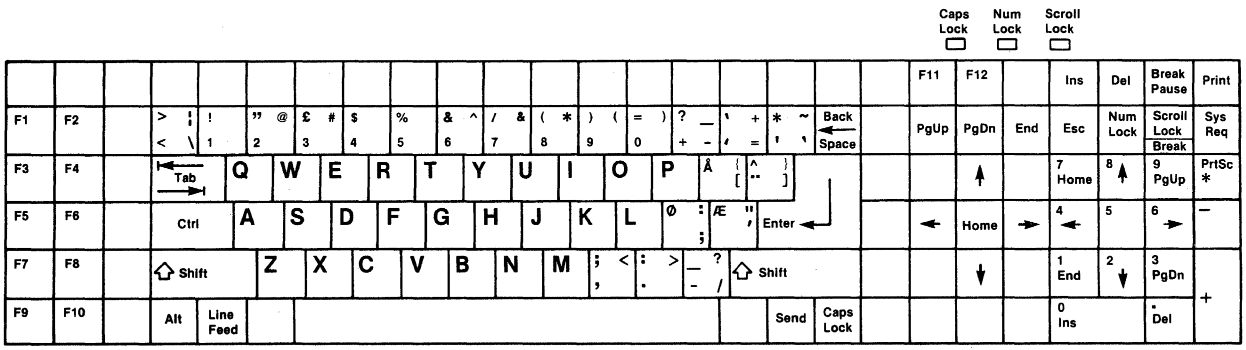
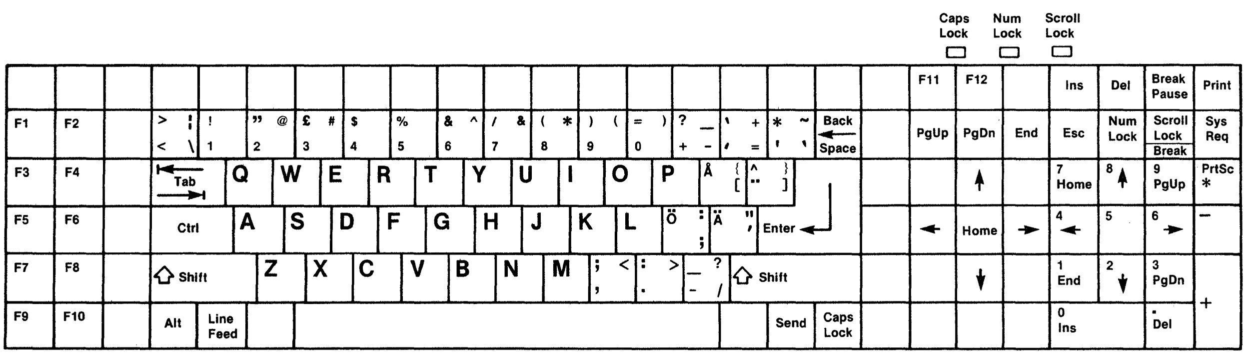


Figure 4-15 Keycap Configuration -- Spain



2287312

Figure 4-16 Keycap Configuration -- Sweden



2287314

Figure 4-17 Keycap Configuration -- Switzerland

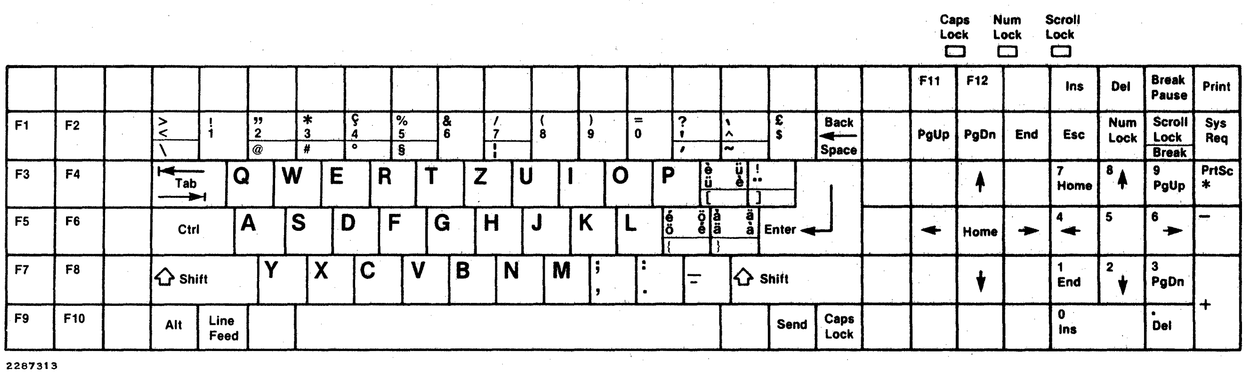


Figure 4-18 Keycap Configuration -- United Kingdom

Section 5

Floppy Disk Drive Controller

5.1 GENERAL

The standard BUSINESS-PRO floppy disk drive subsystem consists of a four-drive floppy disk controller and a 1.2-megabyte floppy disk drive. This section describes the floppy disk drive subsystem.

NOTE

> The 1.2-megabyte and 360-kilobyte disk drives are options that can be used with the floppy disk controller. These drives are described in Section 6 of this manual.

5.1.1 Floppy Disk Controller

The floppy disk controller is an 8-bit peripheral controller board that can control both high-capacity (1.2 megabyte) and low-capacity (360-kilobyte) floppy disk drives. The controller contains the logic devices required for generating control signals and handling data, control, and status transfer operations between the floppy disk drive subsystem and the host. These logic devices comprise the following controller circuits:

* Floppy disk drive interface
* Host I/O interface and control logic
* Host DMA interface and control logic
* Floppy disk controller logic
* Write precompensation logic
* High-density and low-density data separators

Appendix E contains a logic diagram (Drawing No. 2240921) for the floppy disk controller. The following paragraphs describe the floppy disk controller functions.

5.1.1.1 Floppy Disk Drive Interface. The floppy disk controller can interface from one to four 1.2-megabyte or 360-kilobyte disk drives via I/O connectors on the controller board. The controller connectors and their interfaces are as follows:

* J3 (standard usage) -- internal disk drives A and B
* J4 (optional usage) -- internal disk drives C and D (SW1-3 ON)
* J5 (optional usage) -- external disk drives C and D (SW1-3 OFF)

Figure 5-1 is a functional block diagram of the floppy disk controller. Figure 5-2 is a simplified block diagram of the interface of the controller connectors to the disk drives.

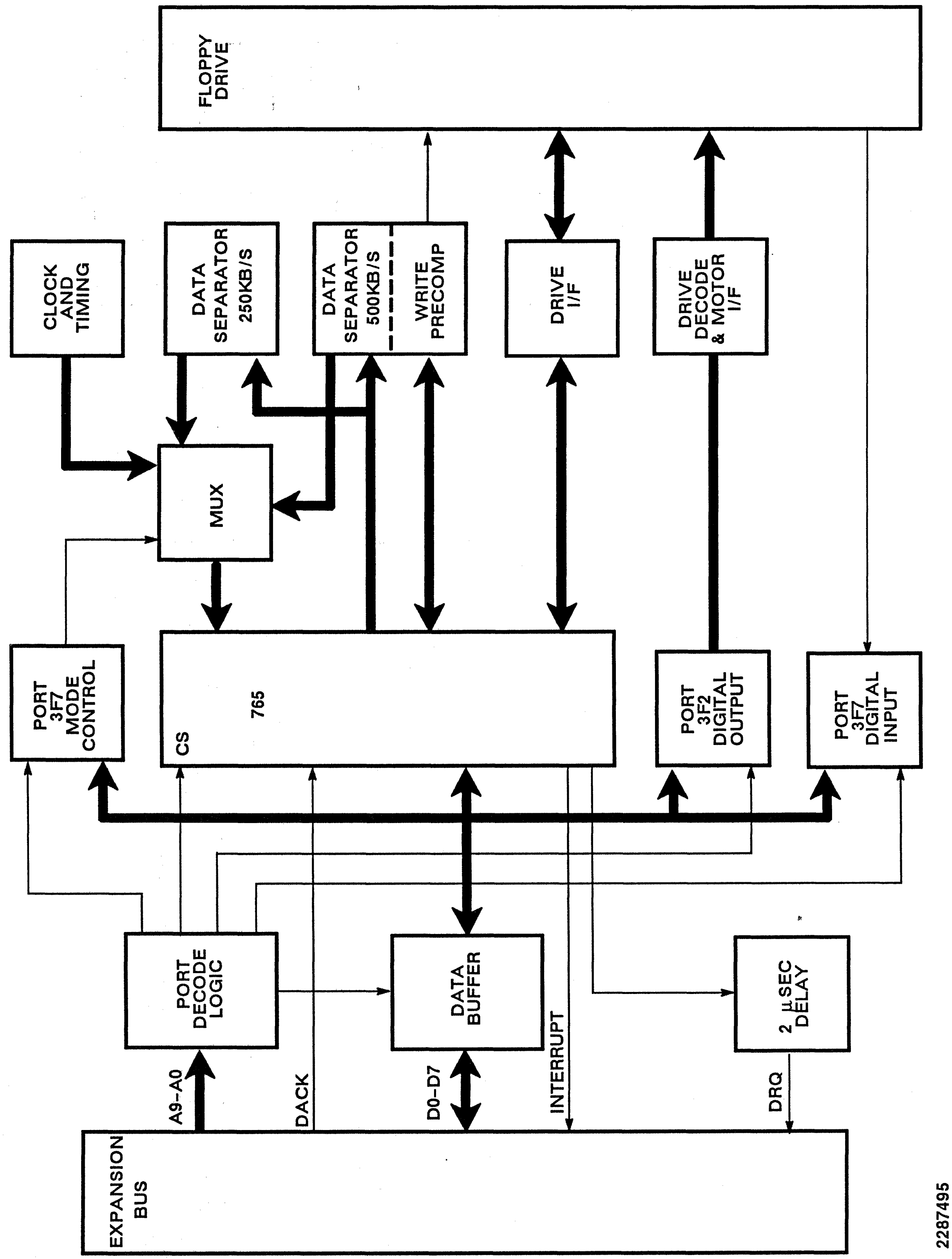


Figure 5-1 Functional Block Diagram of Floppy Disk Controller

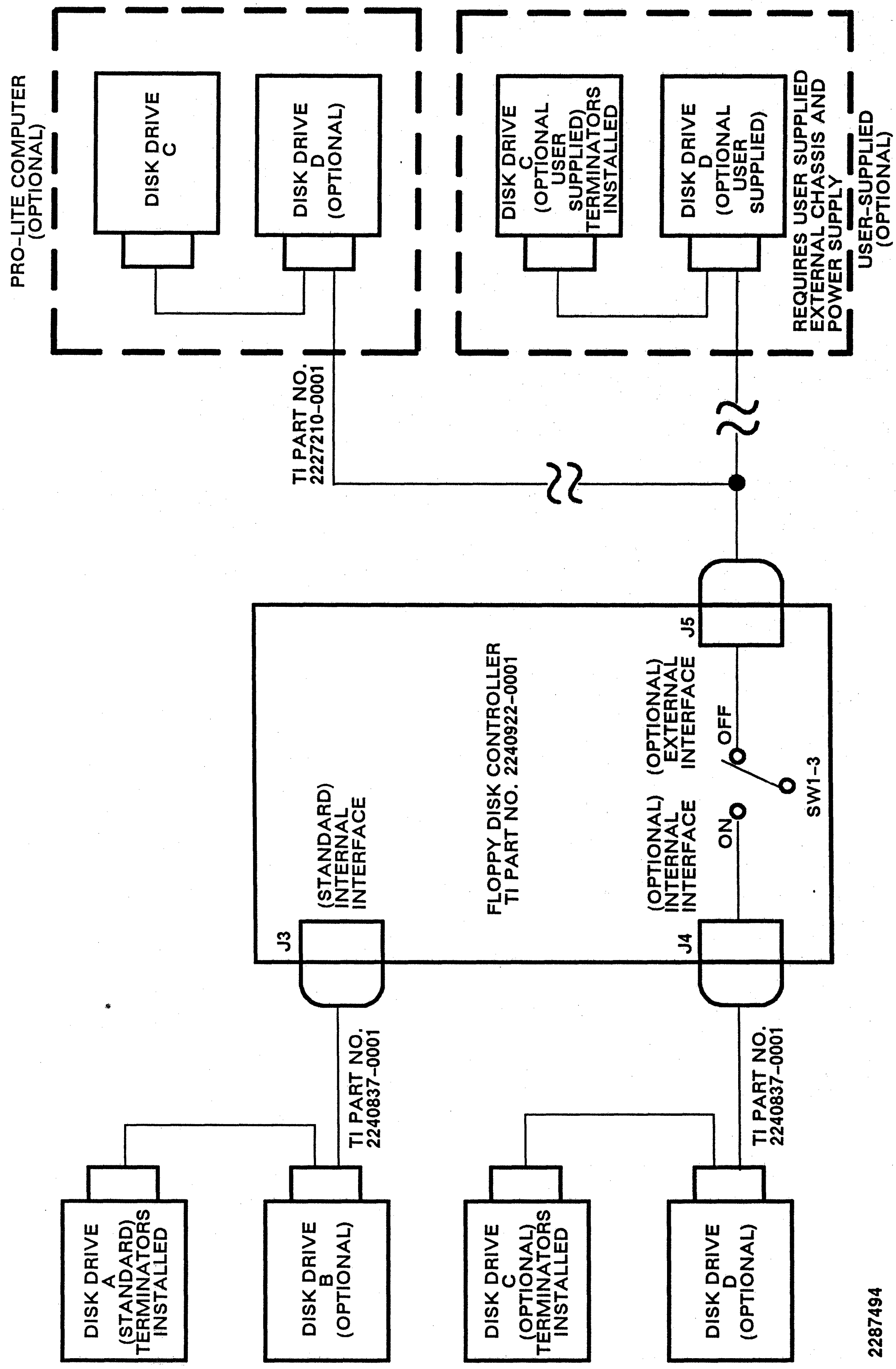


Figure 5-2 Simplified Block Diagram of Disk Drive Interfaces

Low-impedance ribbon cables connect interface signals between the three I/O connectors on the controller board and the disk drives via a series of buffers and receivers on the controller. All signals for connectors J4 and J5 are controlled through a common set of drivers, but connector J3 uses a separate set of drivers. All three connectors have separate receivers and terminating resistors.

Connectors J3 (standard internal interface) and J4 (optional internal interface) use 34-pin ribbon cables to connect from one to four disk drives, mounted internally in the system unit. The ribbon cable from connector J3 connects to the first two drives, which are designated A and B. Drive A is mounted in the top of the chassis with its drive select 0 jumper installed and its terminating resistors installed. If drive B is installed, it is mounted below drive A with its drive select 1 jumper installed and its terminating resistors disabled.

Connector J4 is identical to connector J3 except for the drive select signals which are configured for drive select 2 and drive select 3 jumpers on the disk drives. These drives are designated C and D. Drive C is mounted just below drive B with the drive select 2 jumper installed and the terminating resistors enabled. The second drive connected to connector J4 is designated drive D with its drive select 3 jumper installed and terminating resistors disabled.

Connector J5 (if used) mates with a 37-pin, D-type connector which is compatible with the PC-XT expansion floppy disk drive connector. Two optional external disk drives, designated C and D, or a PRO-LITE computer expansion cable can be connected to J5.

NOTE

Any time connector J5 is used for external configurations, SW1-3 must be set to OFF.

The pinouts for connectors J3 and J4 of the floppy disk controller are shown in Tables 5-1 and 5-2, respectively. The pinouts for connector J5 are shown in Table 5-3. The J5 connector is a 37-pin, D-type connector accessible from the back panel of the system unit.

Table 5-1 Internal Floppy Disk Controller Connectors J3

Signal Pins	Return Pins	Signal Name	Source	Function
2	1	LOW1-	System	High density=1, low density=0.
4	3			Not used.
8	7	INDX1-	Floppy	Indicates index hole.
10	9	DS1-	System	Drive select 1.
12	11	DS2-	System	Drive select 2.
16	15	MOEN1	System	Drive motors on.
18	17	DIR1-	System	Step in/out direction.
20	19	STEP1-	System	Step in/out command.
22	21	WDATA1-	System	Serial data to drive.
24	23	WE1-	System	Low enables writing to floppy disk.
26	25	TK001-	Floppy	Low indicates head is over track 00.
28	27	WP1-	Floppy	Indicates disk is write-protected.
30	29	RDATA1-	Floppy	Serial data from drive.
32	31	HSL1-	System	Side select; high=0, low=1.
34	33	DCHG1-	Floppy	Indicates media change for high-density drive.

Table 5-2 Internal Floppy Disk Controller Connectors J4

Signal Pins	Return Pins	Signal Name	Source	Function
2	1	LOW2-	System	High density=1, low density=0.
4	3			Not used.
6	5	DS4-	System	Drive select 4.
8	7	INDX2-	Floppy	Indicates index hole.
14	13	DS3-	System	Drive select 3.
16	15	MOEN2	System	Drive motors on.
18	17	DIR2-	System	Step in/out direction.
20	19	STEP2-	System	Step in/out command.
22	21	WDATA1-	System	Serial data to drive.
24	23	WE2-	System	Low enables writing to floppy disk.
26	25	TK002-	Floppy	Low indicates head is over track 00.
28	27	WP2-	Floppy	Indicates disk is write-protected.
30	29	RDATA2-	Floppy	Serial data from drive.
32	31	HSL2-	System	Side select; high=0, low=1.

Table 5-3 External Interface for Floppy Disk Controller, J5

Signal Pins	Return Pins	Signal Name	Source	Function
1	20			Not used.
2	21			Not used.
3	22	LOW3-	System	Low speed mode=0, high speed mode=1.
4	23			Not used.
5	24			Not used.
6	25	INDX3-	Floppy	Indicates index hole.
7	26	MOEN3-	System	Enables drive motor 3.
8	27	DS4-	System	Enables drive select 4.
9	28	DS3-	System	Enables drive select 3.
10	20	MOEN4-	System	Enables drive motor 4.
11	30	DIR3-	System	Step in/out direction.
12	31	STEP3-	System	Step in/out command.
13	32	WDATA3-	System	Serial data to drive.
14	33	WE3-	System	Low enables writing to floppy disk drive.
15	34	TK003-	Floppy	Low indicates head is over track 00.
16	35	WP3-	Floppy	Indicates drive is write-protected.
17	36	RDATA3-	Floppy	Serial data from drive.
18	37	HSL3-	System	Side select; high=0, low=1.
19	37	DCHG3-	Floppy	Indicates media change for high-density drive.

Floppy Disk Controller Interface to PRO-LITE Computer. Connector J5 on the floppy disk controller can also be connected to an external cable for use with the PRO-LITE computer. In this configuration the PRO-LITE disk drive is used as the third drive of the BUSINESS-PRO computer. The diskette used with the PRO-LITE must be formatted for 40 tracks on the PRO-LITE computer. (The BUSINESS-PRO computer does not support the 720-kilobyte microfloppy disk drive.)

To use the PRO-LITE with the BUSINESS-PRO computer, perform the following steps:

1. Connect a modified cable (TI Part Number 2227210-0001) between J5 on the floppy disk controller and the PRO-LITE computer. (Be sure to use the grey-colored cable because the ground lines are twisted to eliminate noise.)

2. On the floppy disk controller, set switch SW1-3 to OFF to enable the external drive connector (J5).

3. Reboot the PRO-LITE computer. The message SYSTEM ERROR - 0030 is displayed on the PRO-LITE screen to indicate the external drive cable is detected and the PRO-LITE is configured as the third drive of the BUSINESS-PRO computer.

4. Reboot the BUSINESS-PRO with MS-DOS 3.05 or greater. The PRO-LITE drive indicator should flash on and then off during boot.

5. If you have not already done so, run the BUSINESS-PRO setup program to select the PRO-LITE as drive C and/or D. Make sure you do not receive any CMOS or configuration errors during power-up tests.

6. Format a diskette for 40 tracks, as follows:

   To format the diskette on the PRO-LITE, use MS-DOS 2.12 (or greater) commands.

   CONFIG A: 2,40 (Configures drive A as a 40-track, double-sided drive.)

   FORMAT A: (Formats the diskette in drive A as a 40-track diskette.)

5.1.1.2 Host I/O Interface and Control Logic. Connector P1 on the floppy disk controller board carries the interface signals between the host and the controller. The host I/O interface contains the following circuits and devices:

* Address decode logic
* DMA interface and control logic
* Floppy disk controller IC
* Floppy disk write precompensation
* Data separators

Address Decode Logic. The address decode logic decodes expansion bus address lines XA0 through XA9 to provide one of two unique I/O base addresses for the controller board. These I/O base addresses are in the range of 03F2H through 03F7H (primary), or 0372H through 0377H (alternate). SW2 selects between the primary address range (SW2 OFF) and the alternate address range (SW2 ON). The PAL device decodes the individual read/write ports within the selected base address and either enables or disables the expansion data bus transceiver. A buffer provides buffering for the following expansion bus lines:

* Address line XA0
* I/O write line IOWC-
* I/O read line IORD-

The digital output register is selected via primary I/O base address 03F2H or alternate I/O base address 0372H as shown in Table 5-5. A power-up operation clears the register output lines. All of these lines are active high except bit 2 (FRST). A power-up operation sets this line low to reset the floppy controller IC. This line must be set high before the floppy controller IC can be accessed. Bits 0 and 1 (DRL and DRH) select 1 of up to 4 floppy disk drives, depending upon the system configuration. Bit 3 (DMAEN) enables buffer U12 to gate the floppy interrupt (FINT) and the device request (LDRQ) onto the expansion bus level 6 interrupt (IR06) and device request (DRQ) lines, respectively. Bits 4 through 7 (MOEN1 through MOEN4) are the motor enable lines for floppy disk drives 1 through 4, respectively. Each of these lines turns on the motor of its associated drive.

Primary ports 03F4H and 03F5H and alternate ports 0374H and 0375H reside in the floppy disk controller IC. Port 03F4H or 0374H is a read-only register that provides controller/drive status information to the host. The host can access this status register at any time. Port 03F5H or 0375H is the controller data register. This register stores data and command information, as well as parameter and status information, for the floppy disk drives. Access to this register provides programming for the subsystem and allows determination of the result of any issued command.

Writing a binary value of 00 to bits 0 and 1 of port 03F7H or 0377H selects the high-capacity operating mode. This operating mode results in the following conditions:

* Floppy disk drive motor speed -- 360 revolutions per minute (rpm)
* Data separation rate -- 500 kilobits per second
* Floppy disk controller IC clock frequency -- 8 megahertz
* Write clock frequency -- 1 megahertz

Writing a binary value of either 01, 10, or 11 to bits 0 and 1 of port 03F7 or 0377 selects the low-density operating mode. This operating mode results in the following conditions:

* Floppy disk drive motor speed -- 300 rpm
* Data separation rate -- 250 kilobits per second
* Floppy disk controller IC clock frequency -- 4 megahertz
* Write clock frequency -- 500 kilohertz

The host can read bit 7 of primary port 03F7 or alternate port 0377 to determine if a disk change has occurred in the selected floppy disk drive. The remaining bits (0 through 6) are used by the Winchester controller.

This sharing of the port between the floppy disk controller and the Winchester controller requires that this port be handled differently from the other controller ports. When the host reads this port, the floppy disk controller IC disables the expansion bus data transceiver, latches the media-change signal (DCHG) at latch U8 at the beginning of the read cycle, then gates the signal onto bit 7 of the expansion data bus via U7. When the host reads other ports on the controller board, U7 is placed in its tristate condition, and the expansion data bus transceiver is enabled.

<u>Host DMA Interface and Control Logic</u>. The host DMA interface and control logic PAL provide the DMA interface signals, signals for selecting internal or external floppy disk drives 3 and 4, and other signals for selecting either the high-density or the low-density operating modes.

During DMA operations to the floppy disk drive, the PAL device generates the floppy disk acknowledge (FDACK-) signal in response to the DMAEN signal from the floppy disk controller and the DACK2- signal from the host DMA controller. FDACK- enables the expansion bus data transceiver and provides the device-request enable signal to the floppy disk controller IC. The terminal count signal is gated with DACK2- to generate the FTC signal. This signifies the end of the DMA data transfer operation.

An active EN3/4- signal enables either the external drive connector (J5) or the internal drive connector (J4), depending upon the position of SW1-3. Its OFF position enables J5; its ON position enables J4.

CAUTION

> Changing the position of SW1-3 switches the input signals from the drive. It does not switch the output signals, making it possible to inadvertently write data to the wrong disk. To avoid this possibility, drives should never be connected to connectors J4 and J5 at the same time.

The mode-select signals (MDSEL and MDSEL-) select either the high-density or low-density operating mode. The conditions of these signals are determined by writing to bits 0 and 1 at I/O port address 03F7H. A binary value of 00 written to this address sets MDSEL low and MDSEL- high, thus selecting the high-density mode. Writing any other value to this address sets MDSEL high and MDSEL- low (low-density mode).

Floppy Disk Controller IC. The floppy disk controller handles data transfer and control operations between the host and the floppy disk drive. It provides such high-level functions as serial/parallel data conversion, sector location, seek operations, and disk formatting.

The floppy disk controller's internal clock frequency is controlled by software and can be changed by writing to I/O port address 03F7H. During high-density operations, the controller operates at a clock frequency of 8 megahertz to provide a data transfer rate of 500-kilobits per second. For standard minifloppy drives with a data transfer rate of 250-kilobits per second, the clock frequency is set to 4 megahertz.

Floppy Disk Write Precompensation. An inherent characteristic of double-density recording is a condition called bit shift, which results when certain data patterns are written to a disk. This bit shift condition tends to move the read data transitions outside the normal range of the read circuitry, and the condition grows progressively worse as the heads move inward toward the shorter track lengths near the center of the disk.

Optimized write precompensation is provided by shifting the write data to the disk by a value of 125 nanoseconds. The direction of the shift is determined by PS0 and PS1 signal lines of the NEC controller. The write precompensation logic uses these lines from the floppy disk controller IC to shift the data as follows:

Direction of Shift	PS0	PS1	Comments
Normal	0	0	No shift
Late	0	1	125 nanosecond delay
Early	1	0	-125 nanosecond delay
Invalid	1	1	Invalid

Data Separators. The floppy disk controller has two data separators: one used for high-density transfer rates (500K bits per second) and one used for low-density transfer rates (250K bits per second). These data separators, which work identically, synchronize the read clock with the read data pulses during data recovery operations by providing a continuous clock locked in a phase relationship with the read data.

The circuitry for the data separators is shown on sheets 9 and 10 of the logic diagram located in Appendix E. The data separators consist of components U23, U26, U27, U28, and U30. U23 is a one-shot multivibrator, with one-half used for high and one-half used for low data densities. This one-shot multivibrator is used to shorten and stabilize the pulse width of the incoming read pulses so that the phase-locked loop (PLL) and data recovery operations perform properly during the lockup interval. For the high-density mode, the one-shot multivibrator fixes the the incoming read data pulses at 189 nanoseconds, plus or minus 10 percent. For the low-density mode the incoming read data pulses are fixed at 392 nanoseconds, plus or minus 10 percent.

The WD1691 at locations U27 (high density) and U28 (low density) is used to implement a phase-locked loop with U30 (shown on sheet 10 of the logic diagram located in Appendix E), which is the voltage controlled oscillator (VCO). Other external components provide the loop filter. The phase-locked loop provides a continuous clock that is locked in a specific phase relationship with transitions in the incoming data. For this system, the falling edge of the RDDATA- signal should be nearly centered on the high or low pulse of the RDCLK signal. Data is valid in either half of the RCLK signal, but data pulses in adjacent half cycles of the RCLK signal are not allowed.

U30 is a dual voltage controlled oscillator with separate enable signals for each half, ensuring that the two VCOs do not interfere with one another. While the VCO is operating in the high-density mode, the half of the VCO for the low-density mode is disabled, and vice versa. To provide the best capture range and lock stability, the free-running frequency of the VCO (with the FC input at pins 1 and 2 of U30 at 1.3 volts, RDDATA- high) is 4.0 megahertz for high density and 2.0 megahertz for low density at the FO output pins. These frequencies are preset at the factory by adjusting trim pots at R20 (high density) and R19 (low density). If it is necessary to change the adjustments, perform the following steps:

1. Ensure RDDATA- is high. This forces the PU and PD signal lines from U27 and U28 to a tristate condition.

2. Measure the voltage on the FC signal lines with a device having greater than a 5-megohm input impedance. This should be 1.3 volts, plus or minus 5 percent.

3. Measure and/or adjust the VCO frequency on the FO signal lines of U30 (if necessary) as follows:

   a. For high density. Measure the frequency at pin 10 of U30 and adjust R20 (if necessary) to obtain 4.0 megahertz, plus or minus 5 percent. When the adjustments are made correctly, the PLL should be able to lock up to an incoming pulse train with the frequency between 425 kilohertz and 575 kilohertz (plus or minus 15 percent) within 150 microseconds. The pulses should be low-going, 2 microseconds maximum, applied to the RDDATA- input (pin 30 of J3 or J4, or pin 17 of J5).

   b. For low density. Measure the frequency at pin 7 of U30 and adjust R19 (if necessary) to obtain 2.0 megahertz, plus or minus 5 percent. When the adjustments are made correctly, the PLL should be able to lock up to an incoming pulse train with the frequency between 212 kilohertz and 287 kilohertz (plus or minus 15 percent) within 150 microseconds. The pulses should be low-going, 2 microseconds maximum, applied to the RDDATA- input (pin 30 of J3 or J4, or pin 17 of J5).

The output generated by the PLL is the read data clock on pins 12 of U28 and U30. These clock lines, one for high density and one for low density, are fed to a multiplexer where either one can be selected by MDSEL as the read data clock (RCLK) and supplied to the NEC765A floppy disk controller IC (pin 22 of U11 on sheet 5 of the logic diagram). Signal line RD765 from the U26 multiplexer is read data, containing clock and data bits supplied to pin 23 of U11 as RDATA.

Both the high-density and low-density separators are capable of working with either single-density (FM) or double-density (MFM) data. The choice is controlled by the MFM line (logic 0 for single density and logic 1 for double density) from the NEC765A floppy disk controller IC, which is the data density (DDEN) input, to pin 15 of U27 and U28.

5.1.2 Floppy Disk Controller Programming Information

The main system processor has access to several internal data and status registers in the floppy disk controller IC.

5.1.2.1 Floppy Disk Controller IC Internal Registers. The uPD765A floppy disk controller IC, located on the floppy disk controller board, has several internal registers consisting of data registers, status registers, control registers, and input/output registers. The functions and I/O port address of these registers are described in the following paragraphs.

<u>Data Registers and I/O Port Addresses</u>. The 8-bit data register (which actually consists of several registers in a stack with only one register presented to the data bus at one time) stores data, commands, and parameters and provides floppy disk drive status information. Data bytes are written into and read out of the data register in order to obtain the results after a particular command.

An I/O address map of the floppy disk controller, along with the register functions at each address, is shown in Table 5-4. Functions of the bit positions in the registers at each I/O port address are listed in Tables 5-5 through 5-8.

Table 5-4 Floppy Disk Controller I/O Port Address Map

I/O Port Addresses Primary (Hexadecimal)	Secondary	Read Registers	Write Registers
3F2	372		Digital output
3F4	374	Main status	Main status
3F5	375	Floppy disk data	Floppy disk data
3F7	377	Digital input	Floppy disk control

Interrupt request level = 6; DMA request level = 2

Table 5-5 3F2 Digital Output Register Bits

Bit	Signal	Function
0	DRL	Drive select (low bit)
1	DRH	Drive select (high bit)
2	FRST	Function reset
3	DMAEN	Enables interrupts and DMA
4	MOEN1	Enables drive A motor
5	MOEN2	Enables drive B motor
6	MOEN3	Enables drive C motor
7	MOEN4	Enables drive D motor

DRH	DRL	Drive Selected
0	0	0
0	1	1
1	0	2
1	1	3

Table 5-6 3F4H Main Status Register

Bit	Function
0	Drive A busy/seeking
1	Drive B busy/seeking
2	Drive C busy/seeking
3	Drive D busy/seeking
4	Floppy busy command in progress
5	Non-DMA mode
6	Data transfer direction (high=floppy to host)
7	Master-data-register ready request

Table 5-7 3F7H Floppy Disk Diagnostic Register

Bits	Function
0 | 6	Apply to currently selected Winchester drive
7	Diskette change

Table 5-8 3F7H Floppy Disk Register

Bit	Function
0	LD0 -- Mode select low bit
1	LD1 -- Mode select high bit
2	Not used
3	Not used
4	Not used
5	Not used
6	Not used
7	Not used

NOTE:

The mode select bits are used to select between high-capacity disk drive mode and low-capacity mode, as follows:

LD1	LD0	Mode
0	0	High-capacity (500K bps)
0	1	Low-capacity (250K bps)
1	0	Low-capacity (250K bps)
1	1	Low-capacity (250K bps)

5.1.2.2 Controller Commands. The uPD765A floppy disk controller IC performs 15 different commands, as follows:

* Read Data
* Read Deleted Data
* Write Data
* Write Deleted Data
* Read a Track
* Read ID
* Format a Track
* Scan Equal
* Scan Low or Equal
* Scan High or Equal
* Recalibrate
* Sense Interrupt Status
* Specify
* Sense Drive Status
* Seek
* Invalid Command

Each command is initiated by a multibyte transfer from the processor. The results after execution of the command can also be a multibyte transfer back to the processor. Because of this interchange between the processor and the floppy controller, each command consists of three phases, as follows:

* Command phase -- The processor writes a sequence of commands to the floppy controller directing the controller to perform a specific operation.
* Execution phase -- The floppy controller performs the specified operation.
* Result phase -- When the operation completes, status and other information are available to the processor through a sequence of read commands.

Listed below are the codes required to execute each command. The symbols used in the command phase and result phase are defined in Table 5-9, which follows the command descriptions. An X indicates a don't-care condition.

Read Data.

Command Phase:	MT	MF	SK	0	0	1	1	0
	X	X	X	X	X	HD	US1	US0

(C,H,R,N,EOT,GPL,DTL)

Result Phase: (ST0,ST1,ST2,C,H,R,N)

Comment: The host outputs the nine command phase bytes. The floppy disk controller selects the drive, loads the drive heads (if previously unloaded), and begins reading ID address marks and ID data fields to locate the selected sector. When the sector is found, data is transferred (via DMA) to host memory. Multisector and multitrack operation is allowed. Completion of the command updates the result phase registers, interrupts the system processor (if interrupt is enabled), and unloads the heads following the head unload interval.

Read Deleted Data.

Command Phase:	MT	MF	SK	0	1	1	0	0
	X	X	X	X	X	HD	US1	US0

(C,H,R,N,EOT,GPL,DTL)

Result Phase: (ST0,ST1,ST2,C,H,R,N)

Comment: The Read Deleted Data command and the Read a Track command are the same except for the command opcode. The Read Deleted Data transfers sectors that contain the deleted data address mark.

Write Data.

Command Phase:	MT	MF	0	0	0	1	0	1
	X	X	X	X	X	HD	US1	US0

(C,H,R,N,EOT,GPL,DTL)

Result Phase: (ST0,ST1,ST2,C,H,R,N)

Comment: The host outputs the nine command phase bytes and the floppy disk controller selects the drive, loads the heads, and searches the sector ID fields. When the C,H,R, and N sector fields match the command register data, the controller transfers byte data via DMA to the drive. Command completion updates the result registers and interrupts the host processor.

Write Deleted Data.

Command Phase:	MT	MF	0	0	1	0	0	1
	X	X	X	X	X	HD	US1	US0

(C,H,R,N,EOT,GPL,DTL)

Result Phase: (ST0,ST1,ST2,C,H,R,N)

Comment: The Write Deleted Data command is the same as a normal write operation, except that a deleted data address mark is written as the beginning of the data field in place of a normal data address mark.

Read a Track.

Command Phase:	0	MF	SK	0	0	0	1	0
	X	X	X	X	X	HD	US1	US0

(C,H,R,N,EOT,GPL,DTL)

Result Phase: (ST0,ST1,ST2,C,H,R,N)

Comment: The Read a Track command and the Read Deleted Data command are the same except the Read a Track command transfers all sectors from the index mark through the end of track sector.

Read ID.

Command Phase:

```
0   MF  0   0   1   0   1    0
X   X   X   X   X   HD  US1  US0
```

Result Phase: (ST0,ST1,ST2,C,H,R,N)

Comment: The first correct ID information on the cylinder is stored in the data register. Sector ID information is read from the floppy disk during the execution phase.

Format a Track.

Command Phase:

```
0   MF  0   0   1   1   0    1
X   X   X   X   X   HD  US1  US0
```

(N,SC,GPL,D)

Result Phase: (ST0,ST1,ST2,C,H,R,N)

Comment: The selected track is formatted from the index mark through the last track sector with address marks, ID fields, data fields, and field gaps for either the standard single-density or double-density format. The ID field (4 bytes) is furnished by the host for each sector. The data field is filled with the data defined in the command register (DTF).

Scan Equal.

Command Phase:

```
MT  MF  SK  1   0   0   0    1
X   X   X   X   X   HD  US1  US0
```

(C,H,R,N,EOT,GPL,STP)

Result Phase: (ST0,ST1,ST2,C,H,R,N)

Comment: The selected sector is compared on a byte basis between the drive information and the host data. If the scan condition is satisfied, the SH (Scan Equal Hit) bit is set in status register 2.

Scan Low or Equal.

Command Phase:

MT	MF	SK	1	1	0	0	1
X	X	X	X	X	HD	US1	US0

(C,H,R,N,EOT,GPL,STP)

Result Phase: (ST0,ST1,ST2,C,H,R,N)

Comment: The Scan Low or Equal command is similar to the Scan High or Equal command, except for the logical compare condition. If the condition is not satisfied, the SN (Scan Not Hit) bit is set in result register ST2.

Scan High or Equal.

Command Phase:

MT	MF	SK	1	1	1	0	1
X	X	X	X	X	HD	US1	US0

(C,H,R,N,EOT,GPL,STP)

Result Phase: (ST0,ST1,ST2,C,H,R,N)

Comment: The Scan High or Equal command is simliar to the Scan Low or Equal command, except for the logical compare condition. If the scan condition is not satisfied, the SN (Scan Not Hit) bit is set in result register ST2.

Recalibrate.

Command Phase:

0	0	0	0	0	1	1	1
X	X	X	X	X	0	US1	US0

Comment: The heads of the selected drive are retracted to track position 0. The track 0 position flag is available as a separate signal from the selected drive and in the ST3 status byte.

Sense Interrupt Status.

Command Phase: 0 0 0 0 1 0 0 0

Result Phase: (ST0,PCN)

Comment: Controller status register 0 and the current cylinder are available in the result registers following this command. The command clears the floppy section interrupt level.

Specify.

Command Phase: 0 0 0 0 0 0 1 1

(SRT,HUT,HLT,ND)

Comment: The Specify command sets the head load and unload rates, the drive step rate, and the DMA data transfer mode.

Sense Drive Status.

Command Phase:	0	0	0	0	0	1	0	0
	X	X	X	X	X	HD	US1	US0

Result Phase: (ST3)

Comment: This command returns selected drives status ST3 during the result phase.

Seek.

Command Phase:	0	0	0	0	1	1	1	1
	X	X	X	X	X	HD	US1	US0

(NCN)

Comment: This command positions the read/write head over the proper cylinder on the diskette. The controller compares the current head position with NCN and if there is a difference, issues step pulses in the proper direction to reach NCN. When the present cylinder number (PCN) is equal to NCN, the controller sets the Seek End flag to ST0 and terminates the command.

Invalid Command.

Command Phase: <------Invalid Codes---->

Result Phase: (ST0)

Comment: An invalid command causes bits 7 and 6 of ST0 to be set and the controller enters the standby state.

Symbol Descriptions. Table 5-9 defines the symbols used in the above commands.

Table 5-9 Definition of Symbols

Symbol	Name	Definition
A0	Address line 0	Controls selection of main status register (A = 0) or data register (A = 1).
C	Cylinder number	Stands for the currently selected cylinder numbers 0 through 76 of the disk drive.
D	Data	Stands for the data pattern to be written into a sector.
D(0-7)	Data bus	8-bit data bus: D7=MSB, D0=LSB.
DTL	Data length	Stands for the data length to be read out of or written into a sector.
EOT	End-of-track	Final sector number on a cylinder. After EOT, the controller stops data transfer.
GPL	Gap length	During format commands, GPL specifies length of Gap 3. During read/write commands, GPL is the number of bytes that VCOs stay low after CRC.
H	Head address	Head number 0 or 1 specified in ID field.
HD	Head	Selected head number 0 or 1.
HLT	Head load time	Head load time in the disk drive is 2 to 254 milliseconds in 2 millisecond increments.
HUT	Head unload time	Head unload time after a read or write is 16 to 254 milliseconds in 16 millisecond increments.
MF	FM or MFM mode	FM is selected when MF=0; MFM is selected when MF=1.

Table 5-9 Definition of Symbols (Continued)

Symbol	Name	Definition
MT	Multitrack	If MT is high after a read/write operation on side 0, the controller automatically starts searching for sector 1, side 1.
N	Number	Number of data bytes written in a sector.
NCN	New cylinder number	New cylinder that will be reached after seek operation. NCN is the desired position of the head.
ND	Non-DMA mode	Non-DMA operation.
PCN	Present cylinder number	Cylinder number at end of Sense Interrupt Status command.
R	Record	Sector number that will be read or written.
R/W	Read/write	Read or write signal.
SC	Sector	Number of sectors per cylinder.
SK	Skip	Skip deleted data address mark.
SRT	Step rate time	Stepping rate for all disk drives. F=1 millisecond, E=2 milliseconds, and so forth.
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	ST(0-3) represents one to four status registers. Status information is available after command execution. Not to be confused with the main status register, which is selected by A0=0.
STP		Scan Test. If STP=1, the data in contiguous sectors is compared with data sent during a scan operation. If STP=2, alternate sectors are read and compared.
US0 US1	Unit select	Selected drive number 0 or 1.

5.1.2.3 Status Registers. Four internal status registers, ST0 through ST3, contain information about the floppy disk controller. These registers are used to facilitate the transfer of data between the controller and the processor. Values of the bit positions of these registers are noted above in the execution of the various controller commands. The following paragraphs describe the status registers.

Status Register 0 (ST0).

Bits	Description
7 & 6	Interrupt code (IC) 00 = Normal termination (NT) of the command. The command was completed and properly executed. 01 = Abnormal termination (AT) of the command. The execution of the command was started but was not successfully completed. 10 = Invalid command (IC). The issued command was never started. 11 = Abnormal completion because the ready signal from the disk drive changed states.
5	Seek end (SE). Set to 1 when the controller completes the Seek command.
4	Equipment check (EC). Set to 1 if a fault signal is received from the disk drive or if the track 0 signal fails to occur after 77 step pulses.
3	Not ready (NR). Set to 1 when the disk drive is in the not ready state and a Read or Write command is issued to side 1 of a single-sided diskette.
2	Head address(HD). Indicates the state of the head at interrupt.
1 & 0	Unit select 1 and 2 (US1 and US2). Indicates the unit number of the disk drive at interrupt.

Status Register 1 (ST1).

Bit	Description
7	End of cylinder (EN). Set when the controller tries to gain access to a sector beyond the final sector of a cylinder.
6	Not used, always 0.
5	Data error (DE). Set when the controller detects a CRC (Cyclic Redundancy Check) error in either the ID field or the data field.
4	Overrun (OR). Set if the controller is not serviced by the main system within a certain time limit during data transfers.
3	Not used, always 0.
2	No data (ND). Set if the controller cannot find the sector specified in the ID register during the execution of a Read Data, Write Deleted Data, or scan command. This flag is also set if the controller cannot read the ID field without an error during the execution of a Read ID command or if the starting sector cannot be found during the execution of a Read Cylinder command
1	Not writable (NW). Set if the controller detects a write-protect signal from the disk drive during execution of a Write Data, Write Deleted Data, or Format Cylinder command.
0	Missing address mark (MA). Set if the controller cannot detect the ID register mark. At the same time, the MD of status register 2 is set.

<u>Status Register 2 (ST2)</u>.

Bit	Description
7	Not used, always 0.
6	Command mark (CM). This flag is set if the controller encounters a sector that has a deleted data address mark during execution of a Read Data or scan command.
5	Data error in data field (DD). Set if the controller detects an error in the data.
4	Wrong cylinder (WC). Related to no data (ND). Set when the contents of cylinder C on the media are different from those stored in the ID register.
3	Scan equal hit (SH). Set if the contiguous sector data equals the processor data during the execution of a scan command.
2	Scan not satisfied (SN). Set if the controller cannot find a sector on the cylinder that meets the condition during a scan command.
1	Bad cylinder (BC). Related to ND. When the contents of cylinder C on the medium are different from the contents stored in the IDR (internal drive register) and the contents of cylinder C are FF, then this flag is set.
0	Missing address mark in data field (MD). Set if the controller cannot find a data address mark or a deleted data address mark when data is read from the medium.

Status Register 3 (ST3).

Bit	Description
7	Fault (FT). Status of the fault signal from the disk drive.
6	Write protect (WP). Status of the write-protect signal from the disk drive.
5	Ready (RY). Status of the ready signal from the disk drive.
4	Track 0 (T0). Status of the track 0 signal from the disk drive.
3	Two side (TS). Status of the two-side signal from the disk drive.
2	Head address (HD). Status of the side select signal from the disk drive.
1	Unit select 1 (US1). Status of the unit select 1 signal from the disk drive.
0	Unit select 0 (US0). Status of the unit select 0 signal from the disk drive.

Section 6

Hardware Options

6.1 GENERAL

This section provides information about the optional devices that are available for the BUSINESS-PRO computer system. These options are as follows:

* Random-access memory (RAM) expansion kits (128 kilobytes or 512 kilobytes)
* Floppy disk drives (360 kilobytes or 1.2 megabytes)
* Winchester disk controller
* Winchester disk drives (21 megabytes, 40 megabytes, 72 megabytes, or 120 megabytes)
* Tape drive and tape controller
* TI mode CRT controller
* PC-AT mode CRT controller
* Color display unit
* Monochrome display unit
* RS-232 communications interface
* Optical mouse
* Numerical coprocessor

6.2 RAM EXPANSION

The main logic board contains 512 kilobytes of on-board RAM consisting of two 256-kilobyte dynamic RAM boards. Two special 64-kilobyte RAM expansion boards (128-kilobyte RAM expansion kit) allow expansion of this on-board RAM to a total capacity of 640 kilobytes. In addition, a special memory area allows installation of as many as six 512-kilobyte RAM expansion boards to increase the on-board memory size to 3.64 megabytes. The following paragraphs describe the 128-kilobyte and the 512-kilobyte RAM expansion kits.

6.2.1 128-Kilobyte RAM Expansion Kit

The 128-kilobyte RAM expansion kit increases the available system memory capacity from 512 kilobytes to 640 kilobytes. The kit consists of two 64-kilobyte memory boards each of which contains nine 64-kilobyte by 1-bit DRAM devices. These boards occupy memory addresses 080000H through 09FFFFH.

The 64-kilobyte RAM expansion boards mount directly on the main logic board via two interface connectors (P1 and P2). P1 and P2 of the first RAM expansion board connect to J16 and J17 on the main circuit board. P1 and P2 of the second RAM expansion board connect to J18 and J19. When these boards are installed on the main circuit board, switch 4 (SW1, pins 4 and 7) must be set to the ON position. The 128-kilobyte RAM expansion kit contains the following items:

* Two 64-kilobyte RAM expansion boards, TI Part No. 2227053-0001

* <u>128 Kb RAM Expansion</u> manual, TI Part No. 2536082-0001

6.2.1.1 128-Kilobyte RAM Expansion Kit Interface Signals. Two connectors (P1 and P2) provide the data and control paths between the 64-kilobyte RAM expansion boards and the main logic board. Table 6-1 lists and describes the interface signals and shows their connector and pin assignments.

6.2.1.2 128-Kilobyte RAM Expansion Kit Specifications. The 128-kilobyte RAM expansion kit specifications are as follows:

* RAM cycle time (nonturbo mode) -- 500 nanoseconds

* RAM cycle time (turbo mode) -- 333 nanoseconds

* Average supply current -- 300 milliamperes

* Type of error checking -- odd parity

Table 6-1 128-Kilobyte RAM Interface Signals

Signal	Connector and Pin Number	Description
MD0	P2-3	Memory data lines 0 through 7. These lines carry data directly to or from the expansion board DRAMs with no on-board buffering.
MD1	P2-2	
MD2	P2-1	
MD3	P1-1	
MD4	P1-2	
MD5	P1-3	
MD6	P1-10	
MD7	P1-7	
+5 Vdc	P1-4	Volts dc for the DRAMs.
PE	P1-5	Even and odd parity. These lines provide I/O data to the parity DRAM to reflect the odd parity that is generated and detected by the main logic board.
PO	P1-6	
CAS-	P2-6	Column address strobe. The falling edge of CAS- latches column addresses into the DRAMs at the beginning of a memory cycle; a later falling edge latches data in during a memory write cycle.
RAS-	P1-8	Row address strobe. The falling edge of RAS- latches row addresses into the DRAMs at the beginning of a memory cycle; the signal goes high at the completion of the cycle.
W2-	P2-4	Memory write strobe. Memory write cycles activate W2- to allow the falling edge of CAS- to latch data into the DRAMs; the signal remains high during a memory read cycle.
GND	P1-9	Ground.
GND	P2-14	Ground.
A8	P1-11	Address line 0 through 8. These multiplexed address lines provide the DRAM addresses. These addresses change from row to column addresses at the beginning of a memory cycle; they return to row addresses at cycle completion.
A7	P2-12	
A6	P2-9	
A5	P2-11	
A4	P2-13	
A3	P2-5	
A2	P2-10	
A1	P2-7	
A0	P2-8	
	P1-12	Not used.

6.2.2 512-Kilobyte RAM Expansion Kit

An optional 3-megabyte RAM expansion board allows use of as many as six 512-kilobyte RAM expansion kits to increase the total main logic board capacity to 3.64 megabytes. The 3-megabyte RAM expansion board plugs into a connector (J3) on the edge of the main logic board.

Each 512-kilobyte RAM expansion kit consists of two 256-kilobyte RAM expansion boards. Each expansion board qcontains nine 256-kilobyte by 1-bit DRAM devices. These boards mount directly on the 3-megabyte RAM expansion board via an interface connector (P1). The boards occupy memory locations in the range of 010000H through 03FFFFH. The 512-kilobyte RAM expansion kit contains the following items:

* Two 256-kilobyte RAM expansion boards, TI Part No. 2240931-0001

* <u>512 Kb RAM Expansion</u> manual, TI Part No. 2536071-0001

6.2.2.1 512-Kilobyte RAM Expansion Kit Interface Signals. Connector P1 provides the data and control paths between the 256-kilobyte RAM expansion boards and the 3-megabyte RAM expansion board. Table 6-2 lists and describes the interface signals and shows their pin assignments on connector P1.

Table 6-2 512-Kilobyte RAM Expansion Kit Interface Signals

Signal	Pin Number	Description
+5 Vdc	1	These lines provide the operating voltages for the 256-kilobyte RAM expansion board's active devices.
+5 Vdc	2	
+5 Vdc	3	
RA0	4	RAM address lines 0 through 8. These multiplexed address lines provide the addresses for the DRAM devices. These addresses change from row to column addresses at the beginning of a memory cycle. They return to row addresses at cycle completion. Each line is triple buffered on the 3-megabyte RAM expansion board; each buffer drives up to four 256-kilobyte RAM expansion boards.
RA1	5	
RA2	6	
RA3	7	
RA4	8	
RA5	9	
RA6	10	
RA7	11	
RA8	12	
RAS-	13	Row address strobe. The falling edge of this signal latches row addresses into the DRAMs at the beginning of a memory cycle; the signal goes high at the completion of the cycle.

Table 6-2 512-Kilobyte RAM Expansion Kit Interface Signals (Continued)

Signal	Pin Number	Description
CAS-	14	Column address strobe. The falling edge of this signal latches column addresses into the DRAMs at the beginning of a memory cycle; it latches write data for write cycles if W- is already low. CAS- remains inactive (high) during refresh cycles.
W-	15	Memory write strobe. This signal's high state selects the read mode, and its low (active) state selects the write mode. W- must be active prior to the activation of CAS- to place the DRAM data outputs (Qs) in their high-impedance states for the entire cycle. This is necessary for common I/O operation.
PE- PO	16 17	Parity data write to the RAM board and parity data read from the RAM board. Odd parity is generated and detected by the main logic board.
MDIR	18	Memory direction. The state of this signal determines the data transfer direction. Setting the signal high enables data through the octal bus transceiver from the 3-megabyte RAM expansion board to the 256-kilobyte DRAMs. Setting the signal low enables data transfers in the opposite direction.
MD0 MD1 MD2 MD3 MD4 MD5 MD6 MD7	19 20 21 22 23 24 25 26	Memory data lines 0 through 7. These lines carry data to and from the RAM expansion board DRAMs via an on-board octal bus transceiver.
MDEN-	27	Memory data enable. Activation of this signal enables data through the octal bus transceiver in the direction selected by the state of MDIR.
GND	28	Ground.
GND	29	Ground.
GND	30	Ground.

6.2.2.2 512-Kilobyte RAM Expansion Kit Specifications. The important specifications of the 512-kilobyte RAM expansion kit are as follows:

* DRAM cycle time (nonturbo operation) -- 500 nanoseconds
* DRAM cycle time (turbo operation) -- 333 nanoseconds
* DRAM access time -- 150 nanoseconds
* RAS refresh rate -- 64 rows per millisecond
* Average power consumption -- 5 amperes
* Type of error checking -- Odd parity

6.3 BUSINESS-PRO MASS STORAGE OPTIONS

The mass storage configuration for the BUSINESS-PRO is user-selected and can include as many as six half-height mass storage devices connected to the system in daisy-chain fashion. The configuration can include any combination of as many as four floppy disk drives or four Winchester disk drives. The following optional mass storage devices are available for use with the BUSINESS-PRO computer:

* 1.2-megabyte floppy disk drive
* 360-kilobyte floppy disk drive
* 21-megabyte, half-height Winchester disk drive
* 40-megabyte, full-height Winchester disk drive
* 72-megabyte, full-height Winchester disk drive
* 120-megabyte, full-height Winchester disk drive
* 60-megabyte cartridge tape drive

The following paragraphs describe the optional mass storage devices.

6.3.1 1.2-Megabyte Floppy Disk Drive

The 1.2-megabyte floppy disk drive is a dual-mode disk drive that records on a 5 1/4-inch, floppy diskette. The dual-mode feature provides the capability of either high-density (96 tracks per inch) or low-density (48 tracks per inch) recording.

The 1.2-megabyte floppy disk drive circuits use open-collector NAND gate buffers as line drivers and Schmitt trigger inverters as line receivers. (Use of these Schmitt trigger devices provides noise immunity for the signal lines.) All input signals are terminated by 150-ohm resistors and are pulled up to Vcc in the last disk drive in the daisy-chain configuration.

6.3.1.1 1.2-Megabyte Floppy Disk Drive Features. The following features characterize the 1.2-megabyte floppy disk drive:

* Stores and retrieves information on 5 1/4-inch floppy diskettes (either high-density or low-density)

* Operates at two speeds:

  - 360 revolutions per minute (rpm) for high-density media

  - 300 rpm for low-density media

* Reads from or writes to high-density diskettes that provide 1.2 megabytes of storage per diskette.

* Reads from or writes to double-density diskettes. However, diskettes written by the 1.2-megabyte drive are reliable only in 1.2-megabyte drives thereafter.

6.3.1.2 1.2-Megabyte Floppy Disk Drive Kit. The 1.2-megabyte floppy disk drive kit, TI Part No. 2240952-0001 consists of the following components:

* 1.2-megabyte, half-height floppy disk drive, TI Part No. 2240884-0001

* <u>1.2 Mb Half-Height Floppy Drives</u> manual, TI Part No. 2240891-0001

* Daisy-chain cable, TI Part No. 2240837-0001

6.3.1.3 1.2-Megabyte Floppy Disk Drive Tabulated Information. Tables 6-3 through 6-7 provide tabulated information about the 1.2-megabyte floppy disk drive.

NOTE

> The 1.2-megabyte floppy disk drive contains a set of eight dual-inline-package (DIP) switches that can be used to insert (switch ON) or remove (switch OFF) the terminator resistors from the circuit. These switches are all set to their ON positions at the factory. When installing the drives in a daisy-chain configuration, you should ensure that all terminator switches are turned OFF on all drives except the last one in the daisy chain.

Table 6-3 1.2-Megabyte Floppy Drive Interface Connector P1

Signal	Pin Number	Description
LOW SPEED	2	When active, this input signal enables low-speed (360-rpm) operation. Correct read/write operations are not guaranteed until at least 400 milliseconds after a speed change has occurred. The disk drive uses the DRIVE SELECT signal to latch this input line.
HEAD LOAD	4	Not used.
DRIVE SELECT 0 DRIVE SELECT 1 DRIVE SELECT 2 DRIVE SELECT 3	10 12 14 6	These input signals activate the in-use light for a selected disk drive. They also enable all other disk drive signals except MOTOR ON.
INDEX	8	This output signal notifies the disk controller that an index hole has been detected (once per disk revolution). With the drive motor at full speed, the leading edge of this signal occurs approximately every 200 milliseconds for low-speed or approximately every 166.7 milliseconds for high-speed operation.
MOTOR ON	16	This input signal activates the drive motor.
DIRECTION SELECT	18	This input signal determines the travel direction of the read/write heads. Its high state causes the heads to move outward toward track 0. Its low state causes the heads to move inward toward track 39.
STEP	20	This input signal causes a single-track movement of the read/write heads in the direction specified by the DIRECTION SELECT signal.
WRITE DATA	22	This input signal provides data when enabled by an active WRITE GATE signal.

Table 6-3 1.2-Megabyte Floppy Drive Interface Connector P1 (Continued)

Signal	Pin Number	Description
WRITE GATE	24	This input signal enables the WRITE DATA signal and disables the STEP and the READ DATA signals.
TRACK 00	26	This output signal notifies the controller that the read/write heads are positioned at track 0.
WRITE PROTECT	28	This output signal notifies the controller that the diskette is protected against any write operations and cannot, therefore, be written to.
READ DATA	30	This output signal notifies the controller that the drive has detected a clock or a data bit under its read/write heads.
SIDE SELECT	32	This input signal determines which side of the diskette is to be read from or written to. Its high state selects side 0 (bottom side). Its low state selects side 1 (top side).
DISKETTE CHANGE	34	This output signal notifies the controller that the diskette has been changed since the last access operation. Opening the diskette access door activates DISKETTE CHANGE. Either of the following conditions deactivates the signal: Power is applied to the drive. A diskette is installed, the door is closed, and a step pulse is issued to the drive.

NOTE:

All odd-numbered pins are connected to ground.

Table 6-4 1.2-Megabyte Floppy Disk Drive Power Connector P2

Pin Number	Voltage
1	+12 ± 0.6 volts dc
2	+12 volts dc return
3	+5 ± 0.25 volts dc
4	+5 volts dc return

Table 6-5 1.2-Megabyte Floppy Disk Drive Jumper Settings

Jumper	Factory Setting	Function
DS0 DS1 DS2 DS3	In Out Out Out	This jumper configuration designates the disk drive to be drive 1.
HS	Out	This position of jumper HS prevents head loading upon activation of the DRIVE SELECT signal.
HM	In	This position of jumper HM causes the heads to load upon activation of the MOTOR ON signal.
MR	In	This position of jumper MR disables the READY signal.
TD	In	This position of jumper TD prevents the drive from being connected in a daisy-chain configuration with 8-inch floppy disk drives.
HL LB	In In	This configuration defines pin 4 of data connector P1 as the HEAD LOAD signal.
INU LA	Out Out	This configuration defines pin 4 of data connector P1 as in use.

Table 6-6 1.2-Megabyte Floppy Disk Drive Performance Specifications

Characteristic	Specification High Speed	Low Speed
Capacity:		
Formatted	1228.8 kilobytes	368.6 kilobytes
Unformatted	1604 kilobytes	500.0 kilobytes
Recording density	9646 bits per inch	5876 bits per inch
Track density	96 tracks per inch	48 tracks per inch
Rotational speed	360 ± 5.4 rpm	300 ± 4.5 rpm
Tracks per side	80	40
Sector size	512 bytes	512 bytes
Sectors per track	15	8 or 9
Access time:		
Average	91 milliseconds	95 milliseconds
Track-to-track	3 milliseconds	3 milliseconds
Settling time	15 milliseconds	15 milliseconds
Motor start time	1.2 seconds (maximun)	
Head load time	50 milliseconds (maximum)	50 milliseconds (maximum)
Encoding method	Modified frequency modulation (MFM)	Modified frequency modulation (MFM)
Data transfer rate rate	500 kilobits per second	250 kilobits per second
Error rate:		
Soft read errors	1/10(9) bits read	1/10(9) bits read
Hard read errors	1/10(12) bits read	1/10(12) bits read
Seek errors	1/10(6) seek operations	1/10(6) seek operations

Table 6-7 1.2-Megabyte Floppy Disk Drive Power Requirements

Item	Value
Operating current:	
+5 volts dc line	0.4 ampere (typical) 0.5 ampere (maximum)
+12 volts dc line	0.3 ampere (typical) 1.2 amperes (maximum)
Maximum ripple content (peak-to-peak):	
+5 volts dc line	100 millivolts
+12 volts dc line	200 millivolts
Voltage tolerance	± 5%
Power dissipation	5.6 watts (typical)

6.3.2 360-Kilobyte Floppy Disk Drive

The 360-kilobyte floppy disk drive can store and retrieve up to 360 kilobytes of information on a 5 1/4-inch, floppy diskette. The drive uses a direct-drive method of rotation, thus avoiding the problems inherent to a belt-driven system. The drive can be mounted in any of the top four drive positions in the BUSINESS-PRO system enclosure.

The 360-kilobyte floppy disk drive circuits use open-collector NAND gate buffers as line drivers and Schmitt trigger inverters as line receivers. (Use of these Schmitt trigger devices provides noise immunity for the signal lines.) All input signals are terminated by 150-ohm resistors and are pulled up to Vcc in the last disk drive in the daisy-chain configuration.

6.3.2.1 360-Kilobyte Floppy Disk Drive Kit. The 360-kilobyte floppy disk drive kit, TI Part No. 2240972-0001 includes the following items:

* 360-kilobyte, half-height floppy disk drive, TI Part No. 2234298-0002

* 360 Kb Half-Height Floppy Drives manual, TI Part No. 2240978-0001

* Daisy-chain cable, TI Part No. 2240837-0001

6.3.2.2 360-Kilobyte Floppy Disk Drive Tabulated Information. Tables 6-8 through 6-11 provide tabulated information about the 360-kilobyte floppy disk drive.

NOTE

The 360-kilobyte floppy disk drive contains a set of seven DIP switches that can be used to insert (switch ON) or remove (switch OFF) the terminator resistors from the circuit. These switches are all set to their ON positions at the factory. When installing the drives in a daisy-chain configuration, you should ensure that all terminator switches are turned OFF on all drives except the last one in the daisy chain.

Pins 2 and 34 of the 360-kilobyte floppy disk drive interface connector P1 are reserved. All other pin descriptions are the same as those listed in Table 6-3.

Table 6-8 360-Kilobyte Floppy Disk Drive Power Connector P2

Pin Number	Voltage
1	+12 ± 0.6 volts dc
2	+12 volts dc return
3	+5 ± 0.25 volts dc
4	+5 volts dc return

Table 6-9 360-Kilobyte Floppy Disk Drive Jumper Settings

Jumper	Factory Setting	Function
DS0	In	This jumper configuration designates the disk drive to be drive 1.
DS1	Out	
DS2	Out	
DS3	Out	
HS	Out	This position of jumper HS prevents head loading upon activation of the DRIVE SELECT signal.
HM	In	This position of jumper HM causes head loading upon activation of the MOTOR ON signal.
MX	Out	Not defined.

Table 6-10 360-Kilobyte Floppy Disk Drive Specifications

Characteristic	Specification
Capacity:	
Formatted	368.6 kilobytes
Unformatted	500.0 kilobytes
Recording density	5876 bits per inch
Track density	48 tracks per inch
Rotational speed	300 $\pm$ 6 rpm
Tracks per side	40
Sector size	512 bytes
Sectors per track	8 or 9
Read/write heads	2
Access time:	
Average	148 milliseconds
Track-to-track	5 milliseconds
Settling time	15 milliseconds
Motor start time	1 second (maximum)

Table 6-10 360-Kilobyte Floppy Disk Drive Specifications (Continued)

Characteristic	Specification
Head settle time	15 milliseconds (maximum)
Encoding method	Modified frequency modulation (MFM)
Data transfer rate	250 kilobits per second
Error rate:	
Soft read errors	1/10(9) bits read
Hard read errors	1/10(12) bits read
Seek errors	1/10(6) seek operations

Table 6-11 360-Kilobyte Floppy Disk Drive Power Requirements

Item	Value
Operating current:	
+5 volts dc line	0.9 ampere (typical) 1.2 amperes (maximum)
+12 volts dc line	0.5 ampere (typical) 1.3 amperes (maximum)
Maximum ripple content (peak-to-peak):	
+5 volts dc line	50 millivolts
+12 volts dc line	100 millivolts
Voltage tolerance	$\pm$ 5%
Power dissipation	11 watts (typical)

6.3.3 Winchester Disk Controller

The optional Winchester disk controller is a full-sized, 16-bit board that controls the operations of as many as four Winchester disk drives via the industry-standard ST-506 interface. The disk drives connect to the controller in a daisy-chain configuration.

6.3.3.1 Winchester Disk Controller Kit. The Winchester disk controller kit, TI Part No. 2241059-0001 includes the following items:

* Winchester disk controller, TI Part No. 2240925-0001
* Winchester Controller manual, TI Part No. 2241056-0001

6.3.3.2 Winchester Disk Controller Diagrams. Figure 6-1 is a functional block diagram of the Winchester controller. Figures 6-2 through 6-4 are cabling diagrams of the Winchester controller connected in two-drive and three-drive configurations. Figure 6-3 shows the controller connected in a two-drive XENIX system.

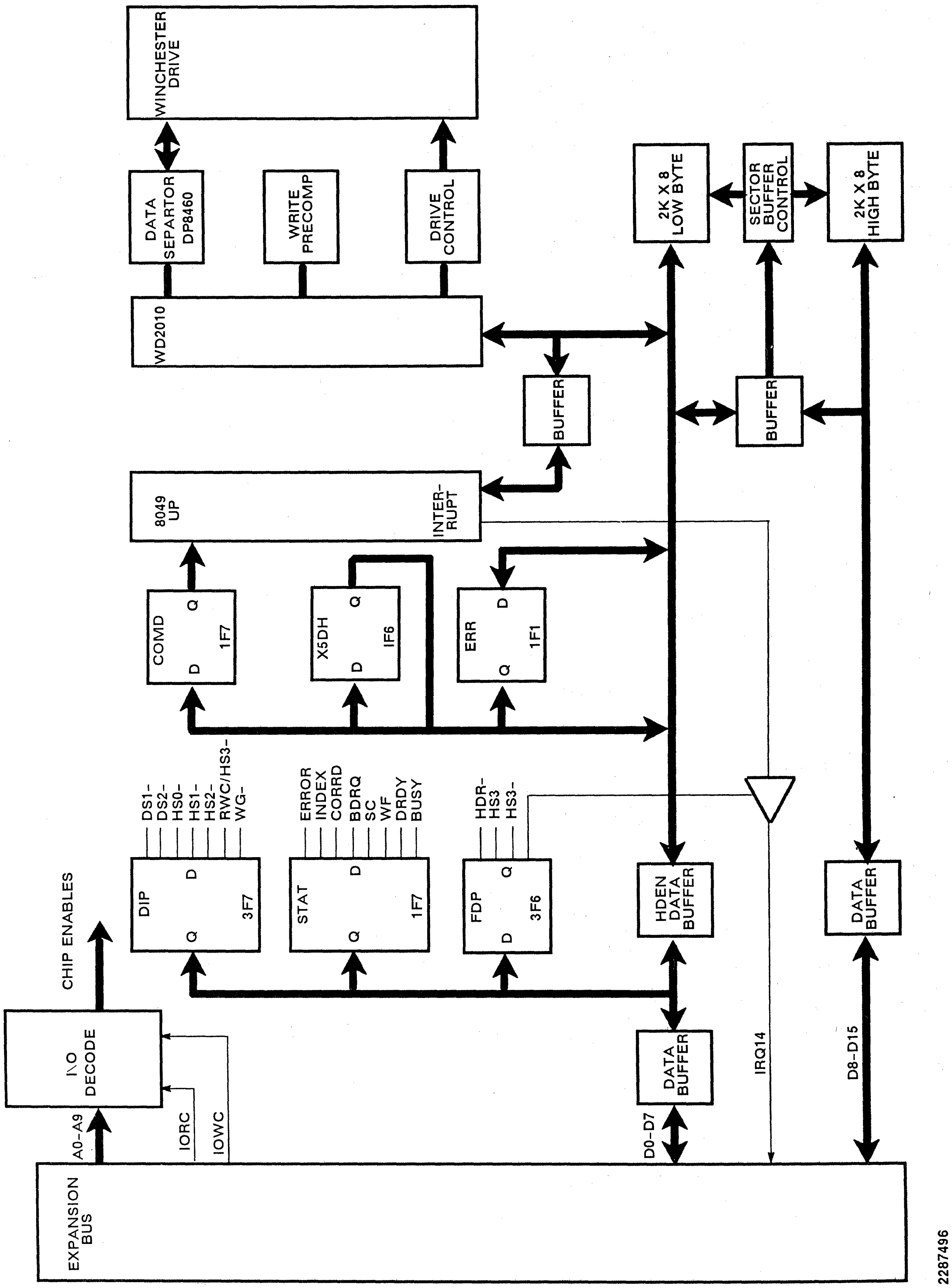


Figure 6-1 Winchester Controller Functional Block Diagram

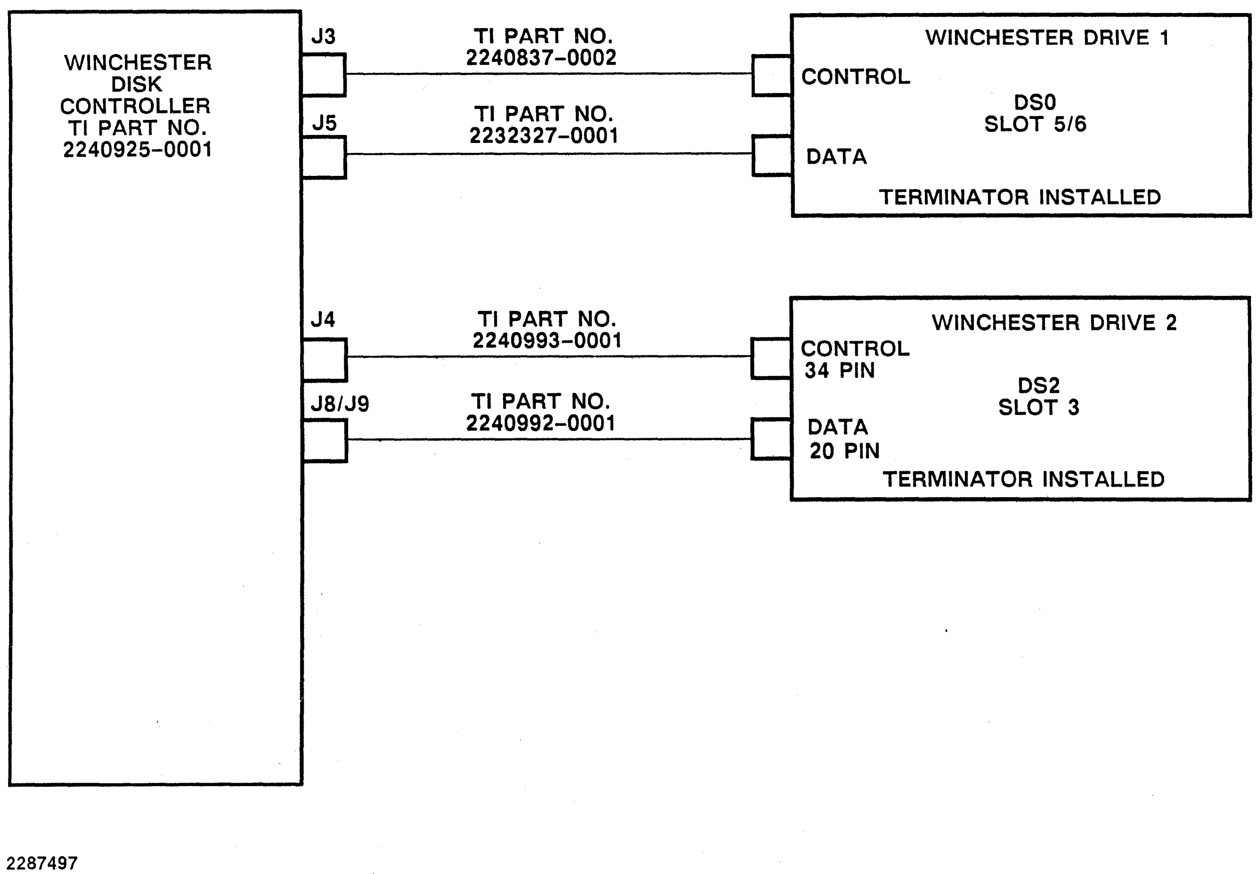


Figure 6-2 Controller Connected in a Two-Drive Configuration

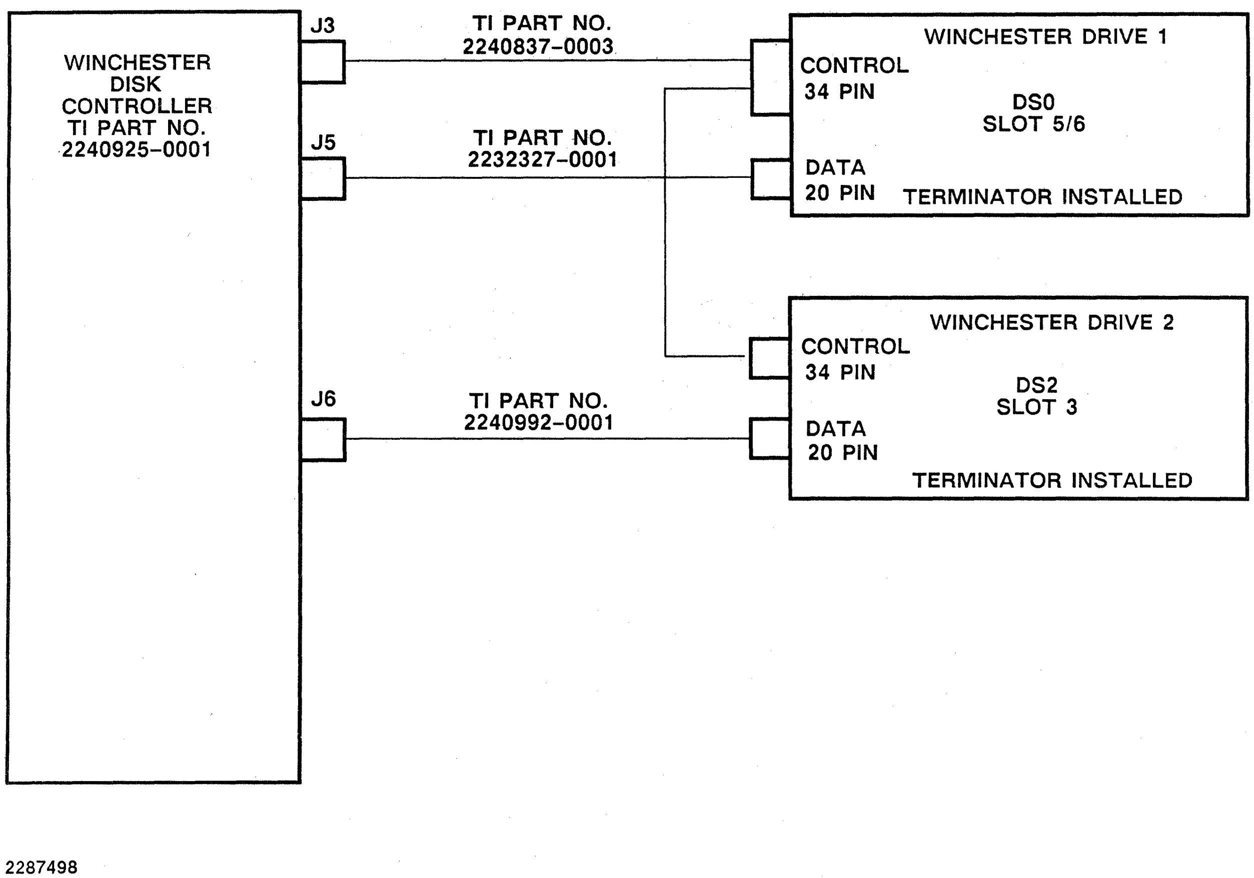
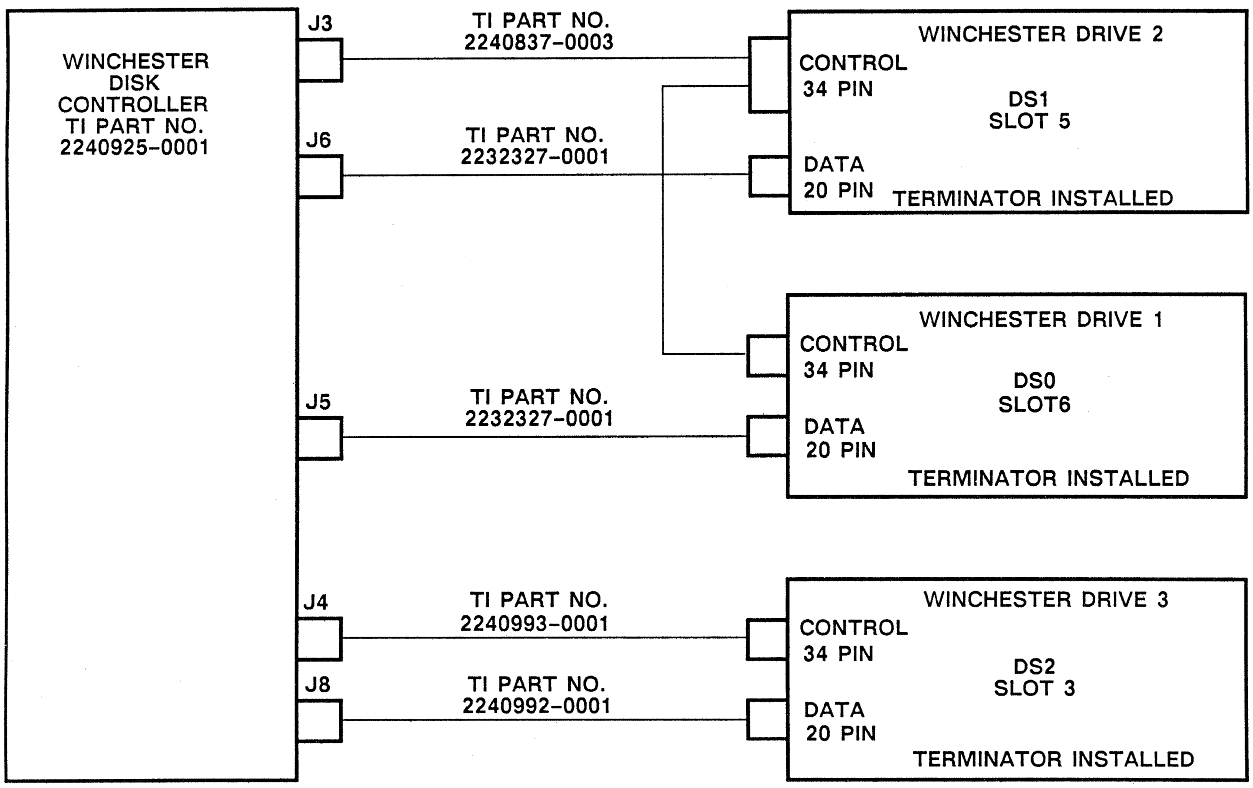


Figure 6-3 Controller Connected in a Two-Drive XENIX System



2287499

Figure 6-4 Controller Connected in a Three-Drive Configuration

6.3.3.3 Winchester Disk Controller Tabulated Information. Tables 6-12 through 6-20 provide tabulated information about the Winchester disk controller. The controller connectors and their functions are as follows:

* Control connector J3 -- control interface for disk drives 1 and 2

* Control connector J4 -- control interface for disk drives 3 and 4

* Data connector J5 -- handles data transfers between the controller and disk drive 1

* Data connector J6 -- handles data transfers between the controller and disk drive 2

* Drive-in-use connector J7 -- allows the user to attach the controller to the drive-in-use indicator on the front of the system enclosure

* Data connector J8 -- handles data transfers between the controller and disk drive 3

* Data connector J9 -- handles data transfers between the controller and disk drive 4

Table 6-12 Winchester Disk Controller Control Connector J3

Signal	Pin Number	Description
DS0- DS1-	26 28	Select signals for drives 1 and 2. The controller generates these signals to select the active drive as determined by the positions of the drive-select jumpers on the disk drives. DS0- enables the drive on J5 (drive 1). DS1- selects the drive on J6 (drive 2).
HS0- HS1- HS2- HS3-	14 18 4 2	Head-select signals 0 through 3. The controller sets these signals to select 1 of 15 read/write heads. HS0- through HS3- form a 4-bit binary code in the range of 1111 through 0000, where 1111 selects head 0.
PWG-	6	Write gate. This controller output signal enables the write driver to allow the selected read/write head to record data on the disk. This signal must remain inactive during read operations or during the transmission of step pulses to the disk drive.
PSC-	8	Seek complete. The disk drive activates this signal to indicate that the drive is selected and that the read/write heads are in the correct position. PSC- must be active before attempting any read or write operations.
PTK000-	10	Track 0. The disk drive activates this signal to indicate that the drive is selected and that the read/write heads are positioned at track 0.
PWF-	12	Write fault. The disk drive activates this signal to indicate that PWG- is active and that one or more of the following conditions is true: Write current is absent.

Table 6-12 Winchester Disk Controller Control Connector J3 (Cont)

Signal	Pin Number	Description
PWF- (Continued)		Write data is absent. The drive is not ready. An invalid read/write head has been selected. Incorrect dc voltage levels. PSC- is inactive. PWF- can also indicate that PWG- is inactive while write current is present. An active PWF- disables all write operations.
PINDEX-	20	Index. The disk drive activates this signal to indicate that it has detected the physical beginning of a track.
PDRDY-	22	Ready. The disk drive activates this signal to indicate that the drive is receiving power, that the disk rotation is within the prescribed tolerance, and that the read/write heads are over the recording zone. Neither the selection of a new head nor a normal seek operation deactivates this signal.
STEP-	24	Step pulse. The controller generates the step pulse to cause the read/write head to move a distance of one cylinder in the direction specified by the state of DIR-.
DIR-	34	Direction. The controller generates this signal to define the direction of read/write head movement for stepping operations. Its low state causes head movement toward the center of the disk; its high condition causes head movement toward track 0.

NOTE:

All odd-numbered pins, except pin 3, are connected to ground. Pin 3 has been removed for connector keying. Pin 16 is reserved.

Table 6-13 Winchester Disk Controller Control Connector J4

Signal	Pin Number	Description
DS2- DS3-	30 32	Select signals for drives 3 and 4. The controller generates these signals to select the active drive as determined by the positions of the drive-select jumpers on the disk drives. DS2- selects the drive on J8. DS3- selects the drive on J9.
SHD0- SHD1- SHD2- SHD3-	14 18 4 2	Head select signals 0 through 3. The controller sets these signals to select 1 of 15 read/write heads. HS0- through HS3- form a 4-bit binary code in the range of 1111 through 0000, where 1111 selects head 0.
SWG-	6	Write gate. This controller output signal enables the write driver to allow the selected read/write head to record data on the disk. This signal must remain inactive during read operations or during the transmission of step pulses to the disk drive.
SSC-	8	Seek complete. The disk drive activates this signal to indicate that the drive is selected and that the read/write heads are in the correct position. SSC- must be active before attempting any read or write operations.
STK000-	10	Track 0. The disk drive activates this signal to indicate that the drive is selected and that the read/write heads are positioned at track 0.
SWF-	12	Write fault. The disk drive activates this signal to indicate that SWG- is active and that one or more of the following conditions is true: Write current is absent. Write data is absent. The drive is not ready.

Table 6-13 Winchester Disk Controller Control Connector J4 (Cont)

Signal	Pin Number	Description
SWF- (Continued)		An invalid read/write head has been selected. Incorrect dc voltage levels. SSC- is inactive. SWF- can also indicate that SWG- is inactive while write current is present. An active SWF- disables all write operations.
SINDEX-	20	Index. The disk drive activates this signal to indicate that it has detected the physical beginning of a track.
SDRDY-	22	Ready. The disk drive activates this signal to indicate that the drive is receiving power, that the disk rotation is within the prescribed tolerance, and that the read/write heads are over the recording zone. Neither the selection of a new head nor a normal seek operation deactivates this signal.
SSTEP-	24	Step pulse. The controller generates the step pulse to cause the read/write head to move a distance of one cylinder in the direction specified by the state of SDIR-.
SDIR-	34	Direction. The controller generates this signal to define the direction of read/write head movement for stepping operations. Its low state causes head movement toward the center of the disk; its high condition causes head movement toward track 0.

NOTE:

All odd-numbered pins, except pin 3, are connected to ground. Pin 3 has been removed for connector keying. Pin 16 is reserved.

Table 6-14 Winchester Disk Controller Data Connector J5

Signal	Pin Number	Description
1MFMWR+	13	Write-data plus and write-data minus
1MFMWR-	14	(differential signal pair)
1MFMRD+	17	Read-data plus and read-data minus
1MFMRD-	18	(differential signal pair)

NOTE:

Pins 1, 3, 5, 7, 9, and 10 are reserved. All other pins, except pin 6, are connected to ground. Pin 6 has been removed for connector keying.

Table 6-15 Winchester Disk Controller Data Connector J6

Signal	Pin Number	Description
2MFMWR+	13	Write-data plus and write-data minus
2MFMWR-	14	(differential signal pair)
2MFMRD+	17	Read-data plus and read-data minus
2MFMRD-	18	(differential signal pair)

NOTE:

Pins 1, 3, 5, 7, 9, and 10 are reserved. All other pins, except pin 6, are connected to ground. Pin 6 has been removed for connector keying.

Table 6-16 Winchester Disk Controller Data Connector J8

Signal	Pin Number	Description
3MFMWR+ 3MFMWR-	13 14	Write-data plus and write-data minus (differential signal pair)
3MFMRD+ 3MFMRD-	17 18	Read-data plus and read-data minus (differential signal pair)

NOTE:

Pins 1, 3, 5, 7, 9, and 10 are reserved. All other pins, except pin 6, are connected to ground. Pin 6 has been removed for connector keying.

Table 6-17 Winchester Disk Controller Data Connector J9

Signal	Pin Number	Description
4MFMWR+ 4MFMWR-	13 14	Write-data plus and write-data minus (differential signal pair)
4MFMRD+ 4MFMRD-	17 18	Read-data plus and read-data minus (differential signal pair)

NOTE:

Pins 1, 3, 5, 7, 9, and 10 are reserved. All other pins, except pin 6 are connected to ground. Pin 6 has been removed for connector keying.

Table 6-18 Winchester Disk Controller Switches SW1 Through SW4

Switch	Factory Setting	Function
SW1	OFF	Sets the controller I/O port address range to 1F0H through 1F7H
SW2	OFF	Sets the controller I/O port address range to 3F6H through 3F7H
SW3	OFF	Not used
SW4	OFF	Not used

NOTE:

Both ranges may be activated at the same time.

Table 6-19 Winchester Disk Controller Performance Specifications

Characteristic	Specification
Possible number of drives	1 through 4
Number of cylinders	2048 (maximum)
Number of sectors	1 to 256
Bytes per sector	256, 512, and 1024
Data encoding	MFM
Number of heads	16 (maximum)
Drive selects	4 (maximum)
Data transfer rate	5 megabytes per second
Error correction capability	5-bit correction span

6.3.3.4 External Activity Indicator.
The Winchester disk controller external activity indicator follows the state of the status register. The activity LED connector is a 4-pin, single-row, straight header. Pins 1 and 4 of this connector are tied together as the LED+ signal. Pins 2 and 3 are tied together as the LED- signal. The LED- signal is driven by an open collector device capable of sinking 40 milliamperes when at a transistor-to-transitor (TTL) level. The LED+ signal is pulled up to Vcc through a current-limiting resistor that limits the LED current to approximately 20 milliamperes.

6.3.4 Winchester Disk Controller System Addresses
The Winchester controller is accessed as an I/O device on the system unit bus and has two base addresses available to the programmer. The primary base address of the Winchester controller is 1FXH/3FXH and the secondary base address is 17XH/37XH. The base address is selected by DIP switches on the controller board, as described later in this section. The I/O ports used by the Winchester controller and the function of each port is shown in Table 6-20.

Table 6-20 Winchester Controller I/O Port Addresses

I/O Address Primary (Hexadecimal)	I/O Address Secondary (Hexadecimal)	Name/Function Read	Name/Function Write
1F0	170	Sector buffer	Sector buffer
1F1	171	Error register	Write precompensation
1F2	172	Sector count	Sector count
1F3	173	Sector number	Sector number
1F4	174	Cylinder low	Cylinder low
1F5	175	Cylinder high	Cylinder high
1F6	176	Size/drive/head	Size/drive/head
1F7	177	Status register	Command register
3F6	376	Reserved	Fixed disk register
3F7	377	Diagnostic register	Fixed disk register

6.3.4.1 I/O Port Descriptions. The following sections describe the operation of each of the I/O ports listed in the table above.

<u>Sector Buffer</u>. This is a RAM area used to hold data to be transferred to or from the hard disk. The system has access to this sector buffer when Busy is cleared and BDRQ is active; the Winchester controller has access to the sector buffer in other cases. Data is accessed in the buffer serially; the buffer address automatically increments with each read or write operation. The data register provides a 16-bit path to the system for sector buffer transfers to and from the system. When a Read or Write Long command is performed, the four error detection and correction (ECC) bytes are transferred, one byte at a time, on XD(0-7) using the system processor byte I/O mode. (See Table 6-22 for a definition of the long mode flag.) This sector buffer contains enough storage capacity to buffer one sector of data for the hard disk, plus the four ECC bytes for read/write long commands. Sector sizes of 256, 512, and 1024 bytes are supported.

<u>Error Register</u>. The Winchester controller writes to this register to specify errors or diagnostic codes to the system. The error register is an 8-bit, read-only register containing error information that pertains to the previous command executed. The system has access to the error register whenever the Busy bit is not set. Data in the error register is valid only if the error bit is set in the status register or if internal diagnostics have been executed. Diagnostics are executed at power-up and by execution of the diagnostics command. In operational mode, each bit of the register indicates a different error as shown in Figure 6-5.

```
[7] [6] [5] [4] [3] [2] [1] [0]
 |   |   |   |   |   |   |   |
 |   |   |   |   |   |   |   ----- Data address mark not found
 |   |   |   |   |   |   --------- Track 00 error
 |   |   |   |   |   ------------- Aborted command
 |   |   |   |   ----------------- Not used
 |   |   |   --------------------- ID not found
 |   |   ------------------------- Not used
 |   ----------------------------- Data ECC error
 --------------------------------- Bad block detect
```

Figure 6-5 Error Register Bit Definitions

At the completion of an internal diagnostic test, the error register contains one of the following codes, indicating the status of the hardware. The diagnostic codes are shown in Table 6-21.

Table 6-21 Diagnostic Code Definitions

Code	Status
01H	Pass
02H	Controller fault
03H	Sector buffer fault
04H	Not used
05H	Microcontroller fault
0AH	Size/drive/head register fault

Write Precompensation Register. The write precompensation register is an 8-bit, write-only register specifying the cylinder number divided by four at which write precompensation is to start. Loading this register with a value of FF disables write precompensation.

Sector Count Register. This register specifies the number of sectors to transfer (0=256) for Read, Verify, or Write commands. For the Format Track or Set Parameters command, this register specifies the number of sectors per track. For multiple sector commands, this register is decremented, and the sector number register is incremented. This register is a read/write register, which can be accessed by the system when the Busy bit is cleared.

Sector Number Register. This read/write register specifies the sector number of the starting sector for Read, Verify, and Write commands. This register is incremented for multiple sector commands. The system has access to this register whenever the Busy bit in the status register is cleared.

Cylinder High and Low Registers. The cylinder high and low registers are read/write registers that specify the cylinder number of the starting sector in Read, Verify, Write, or Format Track commands. The controller supports multiple sector operations across track and cylinder boundaries. The cylinder low register is an 8-bit register containing the low-order byte of the cylinder to be accessed. The cylinder high register is an 8-bit register with bits 0, 1, and 2 specifying the high order bits of the cylinder to be accessed. The controller supports a maximum of 2047 cylinders.

Size/Drive/Head Register. The size/drive/head register is an 8-bit, read/write register that directly controls the drive and head selects for the Winchester disk drive, as well as the sector size bits used in the Read, Verify, Write, and Format commands. This register is loaded with the maximum number of heads for each drive before a Set Parameters command is issued. The system has access to this register when Busy is cleared; otherwise, the controller has access to the register. Figure 6-6 shows the bit definitions for this register.

```
[7] [6] [5] [4] [3] [2] [1] [0]
 |   |   |   |   |   |   |   |
 |   |   |   |   |   |   |   ----- Head select 0
 |   |   |   |   |   |   --------- Head select 1
 |   |   |   |   |   ------------- Head select 2
 |   |   |   |   ----------------- Head select 3
 |   |   |   --------------------- Drive select, drive 1=0
 |   |   ------------------------- Sector size 0
 |   ----------------------------- Sector size 1
 --------------------------------- ECC enabled=1
```

Sector size bit mapping:

00 - 256 byte sector
01 - 512
10 - 1024
11 - undefined

Figure 6-6 Size/Drive/Head Register Bit Definitions

Status Register. The status register is an 8-bit, read-only register that contains status information from the controller. The system has access to this register at any time, but data in this register is valid only when the Busy bit is cleared. This register must be read to determine the result of any operation. Reading this register clears the interrupt request on the system bus. A description of the bits in the status register is given in Figure 6-7.

```
[7] [6] [5] [4] [3] [2] [1] [0]
 |   |   |   |   |   |   |   |
 |   |   |   |   |   |   |   ----- Error
 |   |   |   |   |   |   --------- Index from selected drive
 |   |   |   |   |   ------------- Corrected data
 |   |   |   |   ----------------- Data request
 |   |   |   --------------------- Seek complete from drive
 |   |   ------------------------- Write fault from drive
 |   ----------------------------- Drive ready from drive
 --------------------------------- Controller busy
```

Figure 6-7 Status Register Bit Definitions

Command Register. This 8-bit, write-only register is used to load commands for the Winchester controller board when the Busy bit in the status register is cleared. Before writing to the command register the sector count, sector number, cylinder low, cylinder high, and size/drive/head registers must be loaded. Writing to the command register clears the interrupt request to the system. Writing any bit pattern to this register that is not defined below results in a aborted command error. Valid command bit patterns are shown in Table 6-22. Stepping rates are given in Table 6-23.

Table 6-22 Winchester Controller Commands

Bit Positions 7 6 5 4 3 2 1 0	Command
0 0 0 0 0 0 0 0	Scan ID
0 0 0 0 0 0 0 1	Get Software Version
0 0 0 1 <--R-->	Restore
0 0 1 0 0 0 L T	Read
0 0 1 1 0 0 L T	Write
0 1 0 0 0 0 0 T	Verify
0 1 0 1 0 0 0 0	Format Track
0 1 1 1 <--R-->	Seek
1 0 0 0 0 0 0 B	Select Drive Bank
1 0 0 1 0 0 0 0	Perform Internal Diagnostic
1 0 0 1 0 0 0 1	Set Parameters

NOTES:

R - Stepping rate. The stepping rate field of a command maps to real values as indicated in the next table.

L - Long mode flag (0=normal mode, normal ECC functions, 1=long mode, no ECC bytes developed or error checking takes place). When set to 1, the controller does not perform ECC checking on the data field. Instead, the data field is extended by four bytes to include what would normally be the ECC bytes for a read or write operation.

T - Retry flag (0=enable retry, 1=disable retry). When the retry flag is set to 1, the controller does not perform retries on data transfers that generate errors.

B - Bank select (0=set to bank 0, 1=set to bank 1). When the bank select is set to 1, the controller enables selection of drives 3 and 4. When the bank select is set to 0, the controller enables selection of drives 1 and 2.

Table 6-23 Controller-Supported Stepping Rates

R	Rate
0 0 0 0	35us
0 0 0 1	0.5ms
0 0 1 0	1.0ms
0 0 1 1	1.5ms
0 1 0 0	2.0ms
0 1 0 1	2.5ms
0 1 1 0	3.0ms
0 1 1 1	3.5ms
1 0 0 0	4.0ms
1 0 0 1	4.5ms
1 0 1 0	5.0ms
1 0 1 1	5.5ms
1 1 0 0	6.0ms
1 1 0 1	6.5ms*
1 1 1 0	3.2us
1 1 1 1	16.0us

NOTE:

* This rate is used for all subsequent operations that do not specify a stepping rate.

<u>Fixed Disk Control Register</u>.

This register is an 8-bit, write-only register used to control the operation of the Winchester controller card. This register is decoded in the floppy controller I/O address block, and the address of this register follows the address of the floppy controller card. Only bits 1, 2, and 3 of this register are used; bits 0, 4, 5, 6, and 7 are reserved. A description of the bits in this register is given in Figure 6-8.

The /Inten bit is used to enable/disable the Winchester interrupt onto the system interrupt bus. The interrupt is enabled by the power-up reset.

The /Hdr bit is used to generate a software-controlled reset. When set, the software-controlled reset maintains the fixed disk section logic reset as long as the bit is on. This bit is set to a logic 1 for a minimum of 10 microseconds and then reset to a logic 0 to complete the reset function. The HS3 bit is used to enable the head select 3 output for accessing heads 8 through 15.

```
[7] [6] [5] [4] [3] [2] [1] [0]

 |   |   |   |   |   |   |   |
 |   |   |   |   |   |   |   ----- Reserved
 |   |   |   |   |   |   --------- /Inten - Enable interrupt
 |   |   |   |   |   ------------- /Hdr - Reset controller
 |   |   |   |   ----------------- HS3 - Enable head 3 select
 |   |   |   --------------------- Reserved
 |   |   ------------------------- Reserved
 |   ----------------------------- Reserved
 --------------------------------- Reserved
```

Figure 6-8 Fixed Disk Control Register

Diagnostic Register. This register is an 8-bit, read-only register used for diagnostics. Bits 0 through 6 refer to the currently selected hard disk drive. Bit 7 is used for the diskette change line for the floppy disk controller logic. The bit definitions for this register are given in Figure 6-9.

```
[7] [6] [5] [4] [3] [2] [1] [0]

 |   |   |   |   |   |   |   |
 |   |   |   |   |   |   |   ----- /Drive select 0 (0=selected)
 |   |   |   |   |   |   --------- /Drive select 1
 |   |   |   |   |   ------------- /Head select 0
 |   |   |   |   ----------------- /Head select 1
 |   |   |   --------------------- /Head select 2
 |   |   ------------------------- /Head select 3/reduced write
 |   ----------------------------- /Write gate current
 ---------------------------------  Not used
```

Figure 6-9 Diagnostic Register Bit Definitions

6.3.4.2 Controller Command Functions.

Scan ID - 00H. Immediately upon receiving the Scan ID command, peripheral controller hardware raises the Busy flag in the host status register. At the same time, the Command Ready bit goes active, activating the 8049 microprocessor IC. The processor then executes code to update the head, sector size, and cylinder registers. Busy is cleared and an interrupt is sent to the host at the completion of this command.

Get Software Version - 01H. Upon receiving this command, the Busy bit is set in the status register. The controller loads the software major version number into the cylinder high register and the revision number into the cylinder low register. Busy is cleared, and an interrupt is sent to the system at the completion of this command.

Restore - 10H. The Restore command sets the Busy bit, and the controller then executes code to position the heads of the drive specified by the size/drive/head register and the current bank to cylinder 0. If track 0 is not detected after 2047 step pulses have been issued, a track 0 not found error is placed into the error register, and the error bit is set in the status register. The stepping rate field of the command is not used for the restore operation itself but is stored in the controller to be used as the stepping rate value for operations requiring implied seek operations, such as read and write commands. The restore operation waits until a seek complete is detected before issuing another step pulse. Busy is cleared, and an interrupt is sent to the system at the completion of this command.

Read - 20H. The Busy bit is set upon receipt of this command. If the disk drive heads are not already at the specified starting address, an implied Seek is performed using the stepping rate previously specified by a Restore or Seek command. If no stepping rate has been specified, the default rate of 6.5 milliseconds is used. The sector is then read into the sector buffer, ECC (error detection/correction) is applied if so specified, and the corrected data bit is activated if required. If the long bit is set in the command, ECC is not performed on the input data. Instead, four extra bytes of data are read from the disk into the sector buffer. If an uncorrectable error occurs during the read operation, the appropriate error code is loaded into the error register, and the error bit is set in the status register. The controller then sets the data request bit in the status register, clears Busy, and sends an interrupt to the system. The Read command terminates after the system empties the data register.

For multiple sector read operations, the above sequence repeats until all sectors are transferred. If an uncorrectable error occurs, the command terminates. Note that even if an uncorrectable error does occur, the command does not terminate until the system empties the data register.

Write - 30H. Upon receiving the Write command, the controller sets the Data Request bit in the status register and waits until the system fills the sector buffer. When the data register is full, the Busy bit is set. If the heads are not at the specified starting address, an implied Seek is performed using the stepping rate previously specified by a Restore or Seek command. If no stepping rate has been specified, the default rate of 6.5 milliseconds is used. The sector data is then written to the disk. If an error occurs during the write operation, the appropriate error code is loaded into the error register, and the error flag is set. The Write command is terminated by the controller clearing Busy and sending an interrupt to the system.

For multiple sector write operations, the data request bit is set each time the controller is ready to receive the next sector until all sectors are transferred or an uncorrectable error occurs. If an uncorrectable error occurs, the command is terminated as described above.

Verify - 40H. The Verify command operates in the same manner as the Read command, with the exception that the long bit is not valid for this command.

Format Track - 50H. The Format Track command causes the controller to raise the data request bit and wait until the system has filled the sector buffer. Sector buffer full activates the Busy bit in the status register. If the heads are not at the specified starting address, an implied Seek is performed, using the stepping rate previously specified by a Restore or Seek command. If no stepping rate was specified, the default rate of 6.5 milliseconds is used.

The track is then formatted according to the data that was loaded into the sector buffer. The command is terminated by the controller clearing the Busy bit and sending an interrupt to the system. No error checking is done by this command.

Seek - 70H. The Seek command sets the Busy flag in the status register and then steps the heads to the sector address specified by the system. The stepping rate field of the command is used for the seek operation and is also stored in the controller to be used as the stepping rate for operations requiring implied seek operations, such as read and write commands. The Seek command is terminated by the controller clearing Busy and sending an interrupt to the system. The controller does not wait for the drive to complete the seek operation before terminating the command.

Select Drive Bank - 80H. Immediately upon receiving the Select Drive Bank command, peripheral controller hardware raises the Busy flag in the system status register. At the same time, the Command Ready bit goes active, activating the 8049 microprocessor IC. The Bank bit of the command is then stored away for use on all subsequent commands. Busy is cleared, and an interrupt is sent to the system at the completion of this command.

Perform Internal Diagnostic - 90H. The Busy bit is set in the status register. The internal processor, the Winchester controller IC, the sector buffer, and the size/drive/head register are tested for correct operation. The error register is loaded to reflect the status of the hardware. Busy is cleared and an interrupt is sent to the system at the completion of this command. Upon completion of the command, the error register is read to determine the results of the diagnostics command.

Set Parameters - 91H. The Busy bit is set in the status register, and the drive parameters are stored by the controller for use in track and cylinder boundary crossing for multiple sector operations. Before loading this command into the command register, the sector count register must be loaded with the number of sectors per track and the size/drive/head register must be loaded with the drive and the number of heads. Busy is cleared, and an interrupt is generated and sent to the system upon completion of this command.

6.3.5 Winchester Disk Drives

The optional Winchester disk drives that can be used with the Winchester controller on the BUSINESS-PRO are as follows:

* 21-megabyte disk drive
* 40-megabyte disk drive
* 72-megabyte disk drive
* 120-megabyte disk drive

The features of these are described in the following paragraphs.

6.3.5.1 Types of Winchester Disk Drives. The label on each Winchester disk drive specifies the drive type. Table 6-24 lists the types of Winchester disk drives currently available from Texas Instruments that can be used with the BUSINESS-PRO. TI part numbers and parameters for each type are also provided.

Table 6-24 BUSINESS-PRO Drive Types

Characteristics	Drive Types 16	18	20	25	26	28
TI part number	2243928-2	2245231-1	2245231-3	2243928-1	2235275-1	2238028-1
Formatted capacity	21MB	40MB	72MB	10MB	18MB	120MB
Cylinders	615	925	925	612	697	918
Heads	4	9	9	2	3	15
Drive tracks	2460	4625	8325	1224	2091	13770
Reduced write cur.	N/R	N/R	N/R	N/R	N/R	N/R
Write precomp cyl.	128	0	0	128	128	None
Control byte	00	00	00	00	00	08
Landing zone	656	Auto	Auto	656	Head Lock	Auto
Sectors/track	17	17	17	17	17	17
Bytes/sector	512	512	512	512	512	512
Avg. access time	85ms	30ms	30 ms	85 ms	40 ms	30 ms
Unformatted cap.	25498368	48174000	86713200	12749184	21779856	143.43MB
Capacity/track	1046	9634800	9634800	10416	10416	10416
Comments	Rack&Pin	Rotary VC	Rotary VC	Rotary VC	Rotary VC	Rotary VC

Upon system start-up, the program automatically installs the disk drives in the system. The program also installs the pertinent parameters for each drive. Table 6-25 provides a list of all the drive types that can be used on the BUSINESS-PRO with a comparison of the Texas Instruments and IBM types of Winchester disk drives.

Table 6-25 Comparison of Winchester Disk Drive Types

TI Type	IBM Type	Cylinder	Heads	Write Precompensation	Landing Zone	Formatted Capacity (Megabytes)
1	1	306	4	128	305	10
2	2	615	4	300	615	21
3	3	615	6	300	615	32
4	4	940	8	512	940	65
5	5	940	6	512	940	49
6	6	615	4	No	615	21
7	7	462	8	256	511	32
8	8	733	5	No	733	31
9	9	900	15	No	901	117
10	10	820	3	No	820	21
11	11	855	5	No	855	37
12	12	855	7	No	855	52
13	13	306	8	128	319	21
14	14	733	7	No	733	44
15	15		Reserved - set to zeros			
16	2	615	4	0	Auto	21
17	10	925	3	0	Auto	24
18	11	925	5	0	Auto	40
19	12	925	7	0	Auto	56
20	NA	925	9	0	Auto	72
21	NA	925	3	512	Auto	26
22	NA	1024	5	512	Auto	44
23	NA	1024	7	512	Auto	62
24	4	1024	8	512	Auto	71
25	NA	612	2	128	656	10
26	NA	697	3	128	Hd lock	18
27	NA	612	2	400	None	10
28	NA	918	15	None	Auto	119
29	NA	640	4	256	Auto	22

6.3.6 21-Megabyte Winchester Disk Drive

The optional 21-megabyte Winchester disk drive is a microprocessor-controlled disk drive that can handle data at a rate of 5 megabits per second. The disk drive features open-loop stepper head positioning and rack-pinion head actuators. The interface between the disk drive and the Winchester disk controller is the industry-standard ST-506.

6.3.6.1 21-Megabyte Winchester Drive Kit. The 21-megabyte Winchester disk drive kit, TI Part No. 2240994-0001 includes the following items:

* 21-megabyte, half-height Winchester disk drive, TI Part No. 2243928-0002

* Daisy-chain cable, TI Part No. 2240837-0001

* Data cable, TI Part No. 2240835-0001

* <u>Half-Height Winchester Drives</u> manual, TI Part No. 2241055-0001

NOTE

> Installation of the half-height Winchester disk drive in drive positions 1 through 4 requires an optional Winchester cable kit, TI Part No. 2536057-0001. Installation as a second drive in XENIX systems requires optional Winchester cable kit, TI Part No. 2536057-0002.

6.3.6.2 21-Megabyte Disk Drive Tabulated Information. Tables 6-26 through 6-28 provide tabulated information about the 21-megabyte Winchester disk drive.

Table 6-26 21-Megabyte Disk Drive Control Connector J1

Signal	Pin Number	Description
	2	Reserved.
HEAD SELECT 0- HEAD SELECT 1- HEAD SELECT 2-	14 18 4	The host controller sets these signals to select one of the four read/write heads. These signals form a 3-bit binary code in the range of 000 (head 0) through 100 (head 4).
WRITE GATE-	6	The host controller generates this signal to enable the write driver. This allows data to be recorded on the disk via a selected read/write head. During read operations, or when step pulses are transmitted to the drive, this signal must be inactive.
SEEK COMPLETE-	8	The disk drive generates this signal to indicate to the host controller that the drive is selected and that the read/write heads are in position. SEEK COMPLETE- must be active before a read or write operation is attempted. Any one of the following conditions deactivates the signal: The last leading edge of a step pulse or series of step pulses plus a 500-nanosecond delay has occurred. A seek operation is in progress. A recalibration sequence is in progress.
TRACK 0-	10	The disk drive generates this signal to indicate to the host controller that the read/write heads are positioned at track 0.

Table 6-26 21-Megabyte Disk Drive Control Connector J1 (Continued)

Signal	Pin Number	Description
WRITE FAULT-	12	The disk drive generates this signal to indicate to the host controller that WRITE GATE- is active and that one of the following conditions is true: Write current is absent. Write data is absent. The drive is not ready. An invalid read/write head has been selected. Incorrect dc voltage levels. SEEK COMPLETE- is inactive. WRITE FAULT- can also indicate that WRITE GATE- is inactive while write current is present. An active WRITE FAULT- signal disables all write operations. The controller latches this signal on its leading edge, thus ensuring the detection of any transient condition.
	16	Reserved.
INDEX-	20	The disk drive generates this signal to indicate to the host controller that it has detected the beginning of a track.
READY-	22	The disk drive generates this signal to indicate to the host controller that the drive is receiving power, has reached its proper operating speed, and that the read/write heads are over the recording zone.

Table 6-26 21-Megabyte Disk Drive Control Connector J1 (Continued)

Signal	Pin Number	Description
STEP-	24	The host controller generates this signal to cause the read/write heads to move one cylinder in the direction specified by the state of DIRECTION IN-. Pulse duration can vary between 2 and 200 microseconds with a minimum interval of 5 microseconds between pulses. If the direction of head movement is toward track 0 and the number of step pulses exceeds the number of cylinders, the drive recalibrates the head to track 0.
DRIVE SELECT 1- DRIVE SELECT 2- DRIVE SELECT 3- DRIVE SELECT 4-	26 28 30 32	The host controller generates these signals to select the active drive as defined by the position of the drive-select switches on the disk drives. Since all control signals are gated with DRIVE SELECT-, one of these signals must be active to enable communication with the controller.
DIRECTION IN-	34	The host controller generates this signal to specify the direction of read/write head movement. A high condition of DIRECTION IN- causes head movement toward track 0; a low condition causes inward movement of the heads.

NOTE:

All odd-numbered pins are connected to ground.

Table 6-27 21-Megabyte Disk Drive Data Connector J2

Signal	Pin Number	Description
DRIVE SELECTED-	1	The disk drive activates this signal 1 microsecond after detecting the leading edge of DRIVE SELECT- and deactivates it 1 microsecond after the trailing edge. This signal acknowledges to the host that the drive is selected.
	3	Reserved.
	5	Reserved.
	7	Reserved.
	9	Reserved.
SIGNAL GROUND	11	Signal ground.
+MFM WRITE DATA -MFM WRITE DATA	13 14	This differential signal pair carries the MFM-encoded data to the disk drive during a write-to-disk operation. All disk tracks greater than 128 are write precompensated.
SIGNAL GROUND	15	Signal ground.
+MFM READ DATA -MFM READ DATA	17 18	This differential signal pair carries data to the host during read-from-disk operations.
SIGNAL GROUND	20	Signal ground.

NOTE:

All other pins are connected to ground.

Table 6-28 21-Megabyte Disk Drive Power Connector J3

Pin Number	Voltage
1	+12 volts dc
2	+12 volts dc return
3	+5 volts dc return
4	+5 volts dc

6.3.6.3 Configuring a 21-Megabyte Disk Drive. A DIP switch determines the drive number for any given drive (Figure 6-10). Switches 5 through 8 specify drive numbers 4 through 1, respectively. All drives are shipped from the factory with the switches configured as drive 1 (SW8 is ON). A plug-in, terminating resistor pack must be installed in the last drive of a daisy-chain configuration and must be removed for all others. All drives are shipped from the factory with the terminating resistor pack installed.

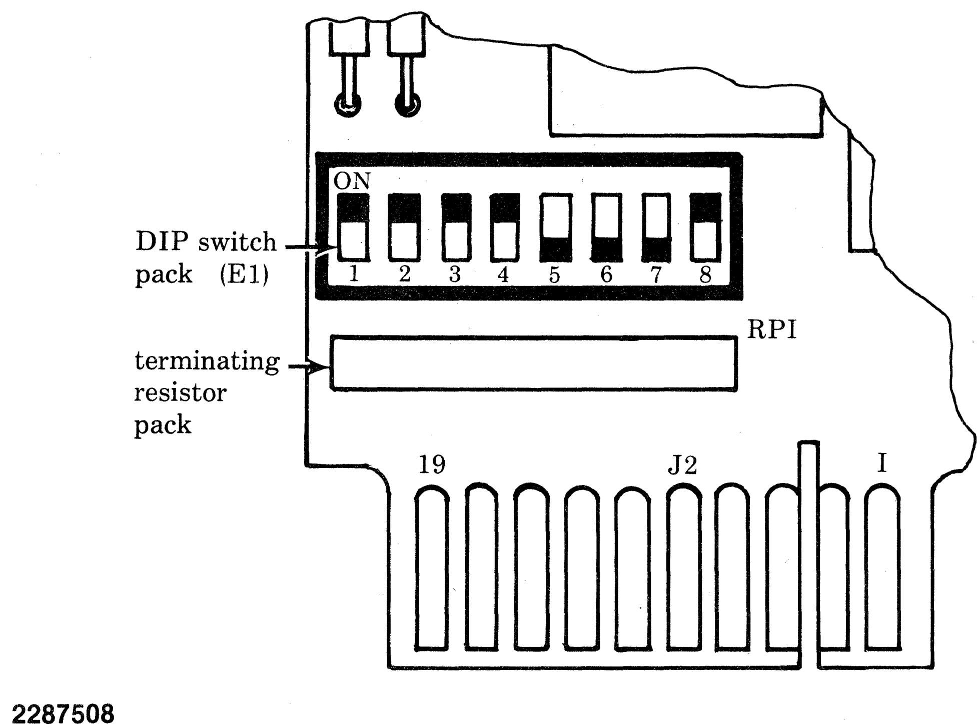


Figure 6-10 21-Megabyte Disk Drive Select Switches and Terminator

Table 6-29 21-Megabyte Disk Drive Performance Specifications

Characteristic	Specification
Unformatted data capacity:	
Bytes per track	10 416
Bytes per surface	6 374 592
Bytes per drive	25 498 368
Media configuration:	
Platters per drive	2
Cylinders per drive	612
Tracks per cylinder	4
Sectoring method	Soft
Recording method	MFM-encoded data
Data transfer rate	5 megabits per second (nominal)
Rotational speed	3 600 ±36 rpm
Average rotational latency	8.33 milliseconds
Drive start time	25 seconds
Drive stop time	20 seconds
Minimum step pulse rate	2 microseconds
Maximum step pulse period	200 microseconds
Typical seek time: (NOTE 1)	
Track-to-track	15 milliseconds
Buffered settling	85 milliseconds (avg)
Maximum buffered including settling	190 milliseconds
Window margin	±18 nanoseconds (minimum)

Table 6-29 21-Megabyte Disk Drive Performance Specifications (Cont)

Characteristic	Specification
Defective tracks per drive (NOTE 2)	30 (maximum)
Defect-free media location	Cylinder 0
Index pulses per revolution	1

NOTE:

1. Seek time for any given seek operation is measured from the last step pulse issued. Average seek time is defined as the quotient of the sum of the time required for all possible movements divided by the total number of movements.

2. A defective track is defined as a track that contains one or more media defects.

Table 6-30 21-Megabyte Disk Drive Power Requirements

Item	Value
Voltage tolerance	+5 percent
Typical operating current:	
+5 volts dc line	0.75 ampere
+12 volts dc line	0.75 ampere
Maximum starting current:	
+5 volts dc line	1.3 amperes
+12 volts dc line	4.5 amperes
Ripple (equivalent resistive load):	
+5 volts dc line	2 percent
+12 volts dc line	1 percent (peak-to-peak)
Power consumption:	
Typical	13.0 watts
Maximum	15.3 watts

6.3.7 40-Megabyte Winchester Disk Drive

The optional 40-megabyte Winchester disk drive is a full-height disk drive that features a rotary voice-coil positioner that is controlled by a closed-loop servo system. To protect its disk surfaces, the drive positions and locks its read/write heads over a dedicated landing zone whenever power is removed. The disk drive interface to the host controller is the industry-standard ST506.

6.3.7.1 40-Megabyte Winchester Disk Drive Kit. The 40-megabyte Winchester disk drive kit, TI Part No. 2241087-0001 includes the following items:

* 40-megabyte, full-height Winchester disk drive, TI Part No. 2245231-0001
* Internal peripheral cable assembly, TI Part No. 2240835-0001
* <u>Full-Height Winchester Drives</u> manual, TI Part No. 2536072-0001

NOTE

> Installation of the 40-megabyte Winchester disk drive in drive positions 1 through 4 requires the use of an optional Winchester cable kit, TI Part No. 2536057-0001. Installation as a second drive in XENIX systems requires optional Winchester cable kit, TI Part No. 2536057-0002.

6.3.7.2 40-Megabyte Disk Drive Tabulated Information. Tables 6-31 through 6-35 provide tabulated information about the 40-megabyte Winchester disk drive.

NOTE

> The 40-megabyte disk drive control connector and data connector are both designated as J3. Both connectors are edge connectors located on two different printed wiring boards inside the unit. The control connector has 34-pins; the data connector has 20 pins.

Table 6-31 40-Megabyte Disk Drive Control Connector J3

Signal	Pin Number	Signal Description
HEAD SELECT 0- HEAD SELECT 1- HEAD SELECT 2- HEAD SELECT 3-	14 18 4 2	The host controller sets these signals to select one of the nine read/write heads. These signals form a 4-bit binary code in the range of 0000 (head 0) through 1000 (head 8).
WRITE GATE-	6	The host controller generates this signal to enable the write driver. This allows data to be recorded on the disk via the selected read/write head. For read operations, or when step pulses are transmitted to the drive, this signal must be active.
SEEK COMPLETE-	8	The disk drive generates this signal to indicate to the host controller that the drive is selected and that the read/write heads are in position. SEEK COMPLETE- must be active before a read or write operation is completed. Any one of the following conditions deactivates SEEK COMPLETE-: The last leading edge of a step pulse or series of step pulses plus a 500 nanosecond delay. A seek operation is in progress. A recalibration sequence is in progress.
TRACK 0-	10	The disk drive generates this signal to indicate to the host controller that the read/write heads are positioned at track 0.

Table 6-31 40-Megabyte Disk Drive Control Connector J3 (Continued)

Signal	Pin Number	Description
WRITE FAULT-	12	The disk drive generates this signal to indicate to the host controller that WRITE GATE- is active and that one of the following conditions is true: Write current is absent. Write data is absent. The drive is not ready. An invalid read/write head has been selected. Incorrect dc voltage levels. SEEK COMPLETE- is inactive. WRITE FAULT- can also indicate that WRITE GATE- is inactive while write current is present. An active WRITE FAULT- signal disables all write operations. The controller latches this signal on its leading edge, thus ensuring the detection of any transient condition.
	16	Reserved.
INDEX-	20	The disk drive generates this signal to indicate to the host controller that the drive has detected the beginning of a track.
READY-	22	The disk drive generates this signal to indicate to the host controller that the drive is receiving power, has reached its proper operating speed, and the read/write heads are over the recording zone.

Table 6-31 40-Megabyte Disk Drive Control Connector J3 (Continued)

Signal	Pin Number	Description
STEP-	24	This controller-generated signal causes the read/write heads to move one cylinder in the direction specified by the state of DIRECTION IN-. Pulse length can vary between 2 and 200 microseconds with a minimum interval of 8 microseconds between pulses. If the direction of head movement is toward track 0 and the number of step pulses exceeds the number of cylinders, the drive recalibrates the head to track 0.
DRIVE SELECT 1- DRIVE SELECT 2- DRIVE SELECT 3- DRIVE SELECT 4-	26 28 30 32	These controller-generated signals select the active drive as defined by the position of the drive-select switches on the disk drives. Since all control signals are gated with DRIVE SELECT-, one of these signals must be active to enable communication with the controller.
DIRECTION IN-	34	This controller-generated signal specifies the direction of head movement. High causes head movement toward track 0; low causes inward head movement.

NOTE:

All odd-numbered pins are connected to ground.

Table 6-32 40-Megabyte Disk Drive Data Connector J3

Signal	Pin Number	Description
DRIVE SELECTED-	1	The disk drive activates this signal 1 microsecond after detecting the leading edge of DRIVE SELECT- and deactivates it 1 microsecond after the trailing edge. This signal acknowledges to the host that the drive is selected.
+MFM WRITE DATA -MFM WRITE DATA	13 14	This differential signal pair carries the MFM-encoded data to the disk drive during a write-to-disk operation. All disk tracks greater than 128 are write precompensated.
+MFM READ DATA -MFM READ DATA	17 18	This differential signal pair carries data to the host during read-from-disk operations.

NOTE:

Pins 3, 5, 7, and 9 are reserved. Pins 11, 15, and 20 are connected to signal ground. All other pins are connected to chassis ground.

Table 6-33 40-Megabyte Disk Drive Power Connector J2

Pin Number	Voltage
1	+12 volts dc
2	+12 volts dc return
3	+5 volts dc return
4	+5 volts dc

6.3.7.3 Configuring 40-Megabyte Disk Drive. An 8-pin, double-row (4-position) header and a jumper plug determine the drive number for any given drive (Figure 6-11). Jumper positions 1 through 4 specify drive numbers 1 through 4, respectively. All drives are shipped from the factory with the jumper configured as drive 1 (jumper plugged into position 1).

A plug-in, terminating resistor pack must be installed in the last drive of a daisy-chain configuration and must be removed for all others. All drives are shipped from the factory with the terminating resistor pack installed.

The radial-select option jumper allows the user to select a radial-cabling configuration in which each drive in the system requires a separate control and data cable. Drives are shipped from the factory with this jumper removed to allow the drive to be connected in a daisy-chain configuration.

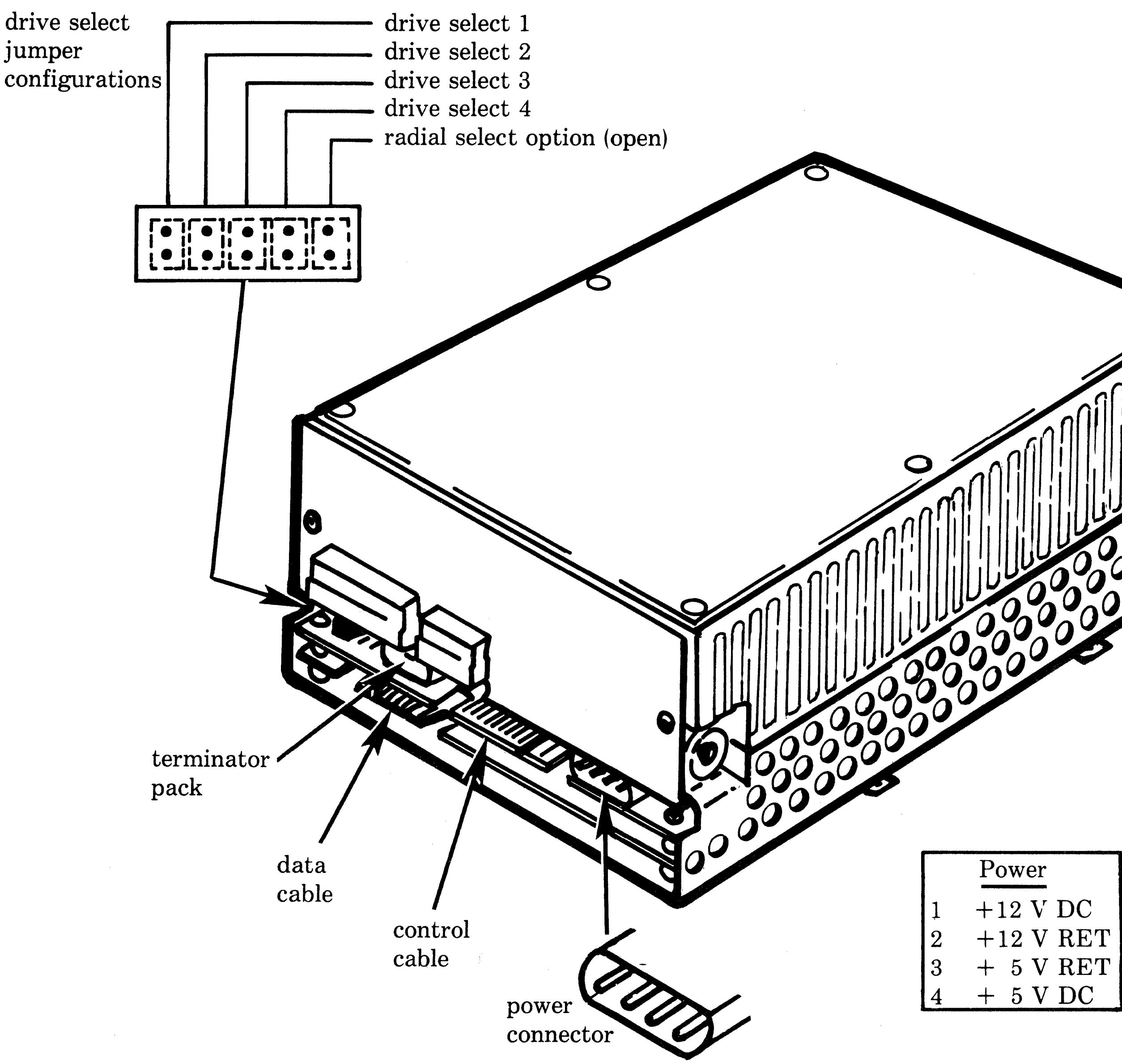


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Figure 6-11 40- and 72-Megabyte Disk Drive Select Switches and Terminator

Table 6-34 40-Megabyte Disk Drive Performance Specifications

Characteristic	Specification
Unformatted data capacity:	
Bytes per track	10 416
Bytes per surface	9 634 800
Bytes per drive	48 174 000
Media configuration:	
Platters per drive	3
Servo surfaces	1
Data surfaces	5
Cylinders per drive	925
Tracks per cylinder	5
Sectoring method	Soft
Recording method	MFM-encoded data
Data transfer rate	5 megabits per second (nominal)
Rotational speed	3 600 ±18 rpm
Rotational latency	8.33 milliseconds (average)
Drive start time	35 seconds
Drive stop time	30 seconds
Step pulse period:	
Minimum	8 microseconds
Maximum	200 microseconds

Table 6-34 40-Megabyte Disk Drive Performance Specifications (Cont)

Characteristic	Specification
Seek times (typical):	
Track-to-track	7 milliseconds
Average	35 milliseconds
925 tracks	85 milliseconds
Maximum bit shift	±31 nanoseconds
Media defects per drive	44
Defect-free cylinders	0, 1, and 2
Index pulses per revolution	1
Write-to-read recovery time	10 microseconds (maximum)

Table 6-35 40-Megabyte Disk Drive DC Power Requirements

Item	Value
Voltage tolerance	±5 percent
Typical operating current:	
+5 volts dc line	0.75 ampere
+12 volts dc line	2.00 amperes
Maximum operating current:	
+5 volts dc line	0.9 ampere
+12 volts dc line	2.4 amperes
Maximum starting current:	
+5 volts dc line	1.3 amperes
+12 volts dc line	4.5 amperes
Ripple (peak-to-peak):	
+5 volts dc line	50 millivolts
+12 volts dc line	100 millivolts

6.3.8 72-Megabyte Winchester Disk Drive

The optional 72-megabyte Winchester disk drive is a full-height disk drive that features a rotary voice-coil positioner that is controlled by a closed-loop servo system. To protect its disk surfaces, the drive positions and locks its read/write heads over a dedicated landing zone whenever power is removed. The disk drive interface to the host controller is the industry-standard ST506.

6.3.8.1 72-Megabyte Winchester Disk Drive Kit. The 72-megabyte Winchester disk drive kit, TI Part No. 2241087-0002 includes the following items:

* 72-megabyte, full-height Winchester disk drive, TI Part No. 2245231-0003
* Internal peripheral cable assembly, TI Part No. 2240835-0001
* Full-Height Winchester Drives manual, TI Part No. 2536072-0001

NOTE

Installation of the 72-megabyte Winchester disk drive in drive positions 1 through 4 requires an optional Winchester cable kit, TI Part No. 2536057-0001. Installation as a second drive in XENIX systems requires optional Winchester cable kit, TI Part No. 2536057-0002.

6.3.8.2 72-Megabyte Disk Drive Tabulated Information. Tables 6-36 through 6-40 provide tabulated information about the 72-megabyte Winchester disk drive.

NOTE

The 72-megabyte disk drive control connector and data connector are both designated as J3. Both connectors are edge connectors located on two different printed wiring boards inside the unit. The control connector has 34-pins; the data connector has 20 pins.

Table 6-36 72-Megabyte Disk Drive Control Connector J3

Signal	Pin Number	Signal Description
HEAD SELECT 0- HEAD SELECT 1- HEAD SELECT 2- HEAD SELECT 3-	14 18 4 2	The host controller sets these signals to select one of the nine read/write heads. These signals form a 4-bit binary code in the range of 0000 (head 0) through 1000 (head 8).
WRITE GATE-	6	The host controller generates this signal to enable the write driver. This allows data to be recorded on the disk via the selected read/write head. During read operations, or when step pulses are transmitted to the drive, this signal must be inactive.
SEEK COMPLETE-	8	The disk drive generates this signal to indicate to the host controller that the drive is selected and that the read/write heads are in position. SEEK COMPLETE- must be active before a read or write operation is attempted. Any one of the following conditions deactivates the signal: The last leading edge of a step pulse or series of step pulses plus a 500-nanosecond delay. A seek operation is in progress. A recalibration sequence is in progress.
TRACK 0-	10	The disk drive generates this signal to indicate to the host controller that the read/write heads are positioned at track 0.

Table 6-36 72-Megabyte Disk Drive Control Connector J3 (Continued)

Signal	Pin Number	Description
WRITE FAULT-	12	The disk drive generates this signal to indicate to the host controller that WRITE GATE- is active and that one of the following conditions is true: Write current is absent. Write data is absent. The drive is not ready. An invalid read/write head has been selected. Incorrect dc voltage levels. SEEK COMPLETE- is inactive. WRITE FAULT- can also indicate that WRITE GATE- is inactive while write current is present. An active WRITE FAULT- signal disables all write operations. The controller latches this signal on its leading edge, thus ensuring the detection of any transient condition.
	16	Reserved.
INDEX-	20	The disk drive generates this signal to indicate to the host controller that it has detected the beginning of a track.
READY-	22	The disk drive generates this signal to indicate to the host controller that the drive is receiving power, has reached its proper operating speed, and the read/write heads are over the recording zone.

Table 6-36 72-Megabyte Disk Drive Control Connector J3 (Continued)

Signal	Pin Number	Description
STEP-	24	The host controller generates this signal to cause the read/write heads to move one cylinder in the direction specified by the state of DIRECTION IN-. Pulse duration can vary between 2 and 200 microseconds with a minimum interval of 8 microseconds between pulses. If the direction of head movement is toward track 0 and the number of step pulses exceeds the number of cylinders, the drive recalibrates the head to track 0.
DRIVE SELECT 1- DRIVE SELECT 2- DRIVE SELECT 3- DRIVE SELECT 4-	26 28 30 32	The host controller generates these signals to select the active drive as defined by the position of the drive-select switches on the disk drives. Since all control signals are gated with DRIVE SELECT-, one of these signals must be active to enable communication with the controller.
DIRECTION IN-	34	The host controller generates this signal to specify the direction of read/write head movement. A high condition of DIRECTION IN- causes head movement toward track 0; a low condition causes inward movement of the heads.

NOTE:

All odd-numbered pins are connected to ground.

Table 6-37 72-Megabyte Disk Drive Data Connector J3

Signal	Pin Number	Description
DRIVE SELECTED-	1	The disk drive activates this signal 1 microsecond after detecting the leading edge of DRIVE SELECT- and deactivates it 1 microsecond after the trailing edge. This signal acknowledges to the host that the drive is selected.
+MFM WRITE DATA -MFM WRITE DATA	13 14	This differential signal pair carries the MFM-encoded data to the disk drive during a write-to-disk operation. All disk tracks greater than 128 are write precompensated.
+MFM READ DATA -MFM READ DATA	17 18	This differential signal pair carries data to the host during read-from-disk operations.

NOTE:

Pins 3, 5, 7, and 9 are reserved. Pins 11, 15, and 20 are connected to signal ground. All other pins are connected to chassis ground.

Table 6-38 72-Megabyte Disk Drive Power Connector J2

Pin Number	Voltage
1	+12 volts dc
2	+12 volts dc return
3	+5 volts dc return
4	+5 volts dc

6.3.8.3 Configuring 72-Megabyte Disk Drive. An 8-pin, double-row (4-position) header and a jumper plug determine the drive number for any given drive. Jumper positions 1 through 4 specify drive numbers 1 through 4, respectively. All drives are shipped from the factory with the jumper configured as drive 1 (jumper plugged into position 1). Refer to Figure 6-11.

A plug-in, terminating resistor pack must be installed in the last drive of a daisy-chain configuration and removed for all others. All drives are shipped from the factory with the terminating resistor pack installed.

The radial-select option jumper allows the user to select a radial-cabling configuration in which each drive in the system requires a separate control and data cable. Drives are shipped from the factory with this jumper removed to allow the drive to be connected in a daisy-chain configuration.

Table 6-39 72-Megabyte Disk Drive Performance Specifications

Characteristic	Specification
Unformatted data capacity:	
Bytes per track	10 416
Bytes per surface	9 634 800
Bytes per drive	86 713 200
Media configuration:	
Platters per drive	5
Servo surfaces	1
Data surfaces	9
Cylinders per drive	925
Tracks per cylinder	9
Sectoring method	Soft
Recording method	MFM-encoded data
Data transfer rate	5 megabits per second (nominal)

Table 6-39 72-Megabyte Disk Drive Performance Specifications (Cont)

Characteristic	Specification
Rotational speed	3 600 ±18 rpm
Rotational latency	8.33 milliseconds (average)
Drive start time	35 seconds
Drive stop time	30 seconds
Step pulse period:	
Minimum	8 microseconds
Maximum	200 microseconds
Seek times (typical):	
Track-to-track	7 milliseconds
Average	35 milliseconds
925 tracks	85 milliseconds
Maximum bit shift	±31 nanoseconds
Media defects per drive	44
Defect-free cylinders	0 and 1
Index pulses per revolution	1
Write-to-read recovery time	10 microseconds (maximum)

Table 6-40 72-Megabyte Disk Drive DC Power Requirements

Item	Value
Voltage tolerance	±5 percent
Typical operating current:	
+5 volts dc line	0.75 ampere
+12 volts dc line	2.00 amperes
Maximum operating current:	
+5 volts dc line	0.9 ampere
+12 volts dc line	2.4 amperes
Maximum starting current:	
+5 volts dc line	1.3 amperes
+12 volts dc line	4.5 amperes
Ripple (peak-to-peak):	
+5 volts dc line	50 millivolts
+12 volts dc line	100 millivolts

6.3.9 120-Megabyte Winchester Disk Drive

The optional 120-megabyte Winchester disk drive is a full-height disk drive that features a rotary voice-coil positioner that is controlled by a closed-loop servo system. To protect its disk surfaces, the drive positions and locks its read/write heads over a dedicated landing zone whenever power is removed. The disk drive interface to the host controller is the industry-standard ST506.

6.3.9.1 120-Megabyte Winchester Disk Drive Kit. The 120-megabyte Winchester disk drive kit, TI Part No. 2541087-0001 includes the following items:

* 120-megabyte, full-height Winchester disk drive, TI Part No. 2238028-0001

* Internal peripheral cable assembly, TI Part No. 2240991-0001

* Full-Height Winchester Drives manual, TI Part No. 2536072-0001

NOTE

Installation of the 120-megabyte Winchester disk drive in drive positions 3 or 4 requires an optional Winchester cable kit, TI Part No. 2240835-0001. Installation as a second drive in XENIX systems requires an optional Winchester cable kit, TI Part No. 2536057-0002.

6.3.9.2 120-Megabyte Disk Drive Tabulated Information. Tables 6-41 through 6-44 provide tabulated information about the 120-megabyte Winchester disk drive.

NOTE

The 120-megabyte disk drive control connector (J1) and data connector (J2) are edge connectors located on two different printed wiring boards inside the unit. The control connector has 34-pins; the data connector has 20 pins.

Table 6-41 120-Megabyte Disk Drive Control Connector J1

Signal	Pin Number	Signal Description
HEAD SELECT 0- HEAD SELECT 1- HEAD SELECT 2- HEAD SELECT 3-	14 18 4 2	The host controller sets these signals to select one of the nine read/write heads. These signals form a 4-bit binary code in the range of 0000 (head 0) through 1000 (head 8).
WRITE GATE-	6	The host controller generates this signal to enable the write driver. This allows data to be recorded on the disk via the selected read/write head. During read operations, or when step pulses are transmitted to the drive, this signal must be inactive.
SEEK COMPLETE-	8	The disk drive generates this signal to indicate to the host controller that the drive is selected and that the read/write heads are in position. SEEK COMPLETE- must be active before a read or write operation is attempted. Any one of the following conditions deactivates the signal: The last leading edge of a step pulse or series of step pulses plus a 500-nanosecond delay. A seek operation is in progress. A recalibration sequence is in progress.
TRACK 0-	10	The disk drive generates this signal to indicate to the host controller that the read/write heads are positioned at track 0.

Table 6-41 120-Megabyte Disk Drive Control Connector J1 (Continued)

Signal	Pin Number	Description
WRITE FAULT-	12	The disk drive generates this signal to indicate to the host controller that WRITE GATE- is active and that one of the following conditions is true: Write current is absent. Write data is absent. The drive is not ready. An invalid read/write head has been selected. Incorrect dc voltage levels. SEEK COMPLETE- is inactive. WRITE FAULT- can also indicate that WRITE GATE- is inactive while write current is present. An active WRITE FAULT- signal disables all write operations. The controller latches this signal on its leading edge, thus ensuring the detection of any transient condition.
	16	Reserved.
INDEX-	20	The disk drive generates this signal to indicate to the host controller that it has detected the beginning of a track.
READY-	22	The disk drive generates this signal to indicate to the host controller that the drive is receiving power, has reached its proper operating speed, and the read/write heads are over the recording zone.

Table 6-41 120-Megabyte Disk Drive Control Connector J1 (Continued)

Signal	Pin Number	Description
STEP-	24	The host controller generates this signal to cause the read/write heads to move one cylinder in the direction specified by the state of DIRECTION IN-. Pulse duration can vary between 2 and 200 microseconds with a minimum interval of 8 microseconds between pulses. If the direction of head movement is toward track 0 and the number of step pulses exceeds the number of cylinders, the drive recalibrates the head to track 0.
DRIVE SELECT 1- DRIVE SELECT 2- DRIVE SELECT 3- DRIVE SELECT 4-	26 28 30 32	The host controller generates these signals to select the active drive as defined by the position of the drive-select switches on the disk drives. Since all control signals are gated with DRIVE SELECT-, one of these signals must be active to enable communication with the controller.
DIRECTION IN-	34	The host controller generates this signal to specify the direction of read/write head movement. A high condition of DIRECTION IN- causes head movement toward track 0; a low condition causes inward movement of the heads.

NOTE:

All odd-numbered pins are connected to ground.

Table 6-42 120-Megabyte Disk Drive Data Connector J2

Signal	Pin Number	Description
DRIVE SELECTED-	1	The disk drive activates this signal 1 microsecond after detecting the leading edge of DRIVE SELECT- and deactivates it 1 microsecond after the trailing edge. This signal acknowledges to the host that the drive is selected.
+MFM WRITE DATA -MFM WRITE DATA	13 14	This differential signal pair carries the MFM-encoded data to the disk drive during a write-to-disk operation. All disk tracks greater than 128 are write precompensated.
+MFM READ DATA -MFM READ DATA	17 18	This differential signal pair carries data to the host during read-from-disk operations.

NOTE:

Pins 3, 5, 7, and 9 are reserved. Pins 2, 4, 6, 8, 11, 12, 15, 16, and 20 are connected to signal ground.

Table 6-43 120-Megabyte Disk Drive Power Connector J3

Pin Number	Voltage
1	+12 volts dc
2	+12 volts dc return
3	+5 volts dc return
4	+5 volts dc

6.3.9.3 Configuring 120-Megabyte Disk Drive. A 6-pin, single-row (4-position) header and a jumper plug (refer to Figure 6-12) determine the drive number for any given drive, as follows:

Jumper Pins	Drive Select
5 and 6	1
4 and 5	2
2 and 3	3
1 and 2	4

All drives are shipped from the factory with the jumper configured as drive 1 (jumper on pins 5 and 6). A plug-in, terminating resistor pack must be installed in the last drive of a daisy-chain configuration and removed for all others. All drives are shipped from the factory with the terminating resistor pack installed.

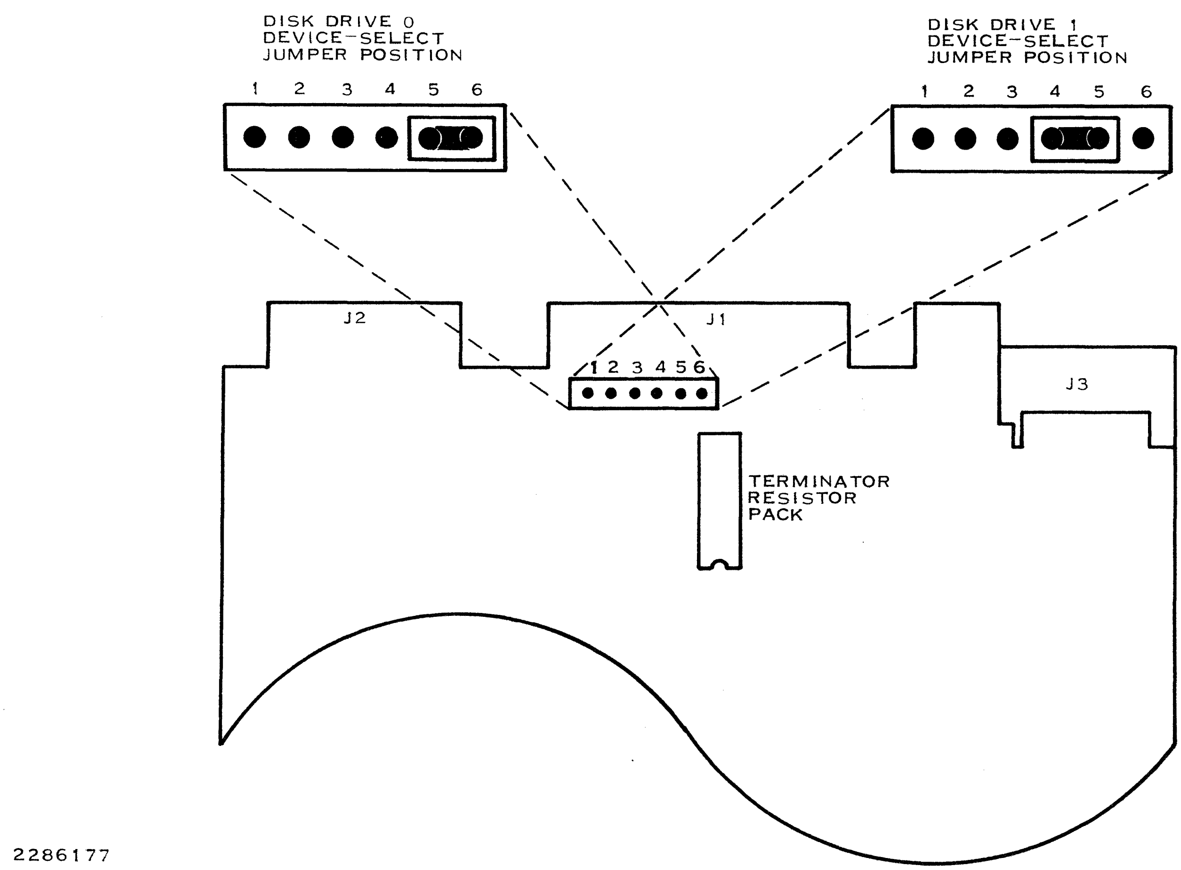


Figure 6-12 120-Megabyte Disk Drive Select Pins and Terminator

Table 6-44 120-Megabyte Disk Drive Performance Specifications

Characteristic	Specification
Unformatted data capacity:	
Bytes per track	10 416
Bytes per surface	9 560 000
Bytes per drive	143 430 200
Formatted data capacity:	
Bytes per track	8 704
Bytes per surface	7 990 000
Bytes per drive	120 000 000
Media configuration:	
Platters per drive	8
Servo surfaces	1
Data surfaces	9
Cylinders per drive	918
Tracks per cylinder	15
Sectoring method	Soft
Recording method	MFM-encoded data
Data transfer rate	5 megabits per second (nominal)
Rotational speed	3 600 +0 rpm, -7.2 rpm
Rotational latency	8.33 milliseconds (average)
Drive start time	20 seconds, maximum
Drive stop time	10 seconds, maximum

Table 6-44 120-Megabyte Disk Drive Performance Specifications (Cont)

Characteristic	Specification
Step pulse period:	
Minimum	2 microseconds
Maximum	200 microseconds
Seek times (maximum):	
Track-to-track	5 milliseconds
Average	30 milliseconds
925 tracks	48 milliseconds
Maximum bit shift	±31 nanoseconds
Media defects per drive	44
Defect-free cylinders	0 and 1
Index pulses per revolution	1
Write-to-read recovery time	8 microseconds, maximum

Table 6-45 120-Megabyte Disk Drive DC Power Requirements

Item	Value
Voltage tolerance	± 5 percent
Typical operating current:	
+5 volts dc line	1.70 ampere
+12 volts dc line	1.60 amperes
Maximum operating current:	
+5 volts dc line	1.9 ampere
+12 volts dc line	2.5 amperes
Maximum starting current:	
+5 volts dc line	1.9 amperes
+12 volts dc line	4.5 amperes
Ripple (peak-to-peak):	
+5 volts dc line	50 millivolts
+12 volts dc line	120 millivolts

6.3.10 Tape System

The optional BUSINESS-PRO tape system consists of a streaming tape drive and a tape controller. The tape system provides low-cost backup for the Winchester disk drive and data transportation from one system to another. The following paragraphs describe the optional tape drive and the tape controller.

6.3.10.1 Tape Drive Kit. The tape drive kit, TI Part No. 2240836-0001, contains the following items:

* 60-megabyte tape drive, TI Part No. 2536125-0001
* Tape controller, TI Part No. 2536126-0001
* Tape controller cable assembly, TI Part No. 2240996-0001
* Tape Backup Hardware manual, TI Part No. 2241043-0001
* CT600 tape cartridge, TI Part No. 2249438-0001 (or equivalent)
* **Streaming tape utility, TI Part No. 2534765-0001**

6.3.10.2 Tape Drive. The tape drive is a 1/4-inch streaming, cartridge tape drive that mounts in the same space as a 5 1/4-inch floppy disk drive.

Tape Drive Features. The following features characterize the cartridge tape drive:

* Uses a nine-track, moving-head drive to read and/or write data in either direction in a serpentine pattern
* Uses the industry-standard QIC-24 data format
* Has a built-in tape controller that uses a subset of the QIC-02 command set
* Uses either a 60-megabyte (DC600A) or a 45-megabyte (DC300XL) tape cartridge.

Tape Drive Tabulated Information. Tables 6-46 through 6-50 provide tabulated information about the tape drive.

Table 6-46 Tape Drive Interface Signals Connector J1

Signal	Pin Number	Description
GO-	2	Go control for the capstan servo system. This input signal causes the tape drive to begin tape motion in the direction specified by the reverse (REV-) signal.
REV-	4	Direction control for the capstan servo system. When active, this input signal causes the tape drive to move the tape in reverse upon activation of GO-.
TR3- TR2- TR1- TR0-	6 8 10 12	Track select bits. These input signals form a binary code that causes the tape drive to select one of nine tracks. The codes are as follows: Track 0 -- TR3- through TR0- equal 0000 Track 1 -- TR3- through TR0- equal 0001 Track 2 -- TR3- through TR0- equal 0010 Track 3 -- TR3- through TR0- equal 0011 Track 4 -- TR3- through TR0- equal 0100 Track 5 -- TR3- through TR0- equal 0101 Track 6 -- TR3- through TR0- equal 0110 Track 7 -- TR3- through TR0- equal 0111 Track 8 -- TR3- through TR0- equal 1000
RST-	14	Reset. Activation of this signal for a period of 70 microseconds or longer causes the drive to reset its head assembly to track 0.
	16	Reserved.
	18	Reserved.
	20	Reserved.

Table 6-46 Tape Drive Interface Signals -- Connector J1 (Cont)

Signal	Pin Number	Description
DS0-	22	Drive 0 select. This input signal enables output interface signals, write current, and erase current. The tape drive responds to DS0- by generating a drive-selected signal to the controller.
HC-	24	High-current select. The tape controller activates this input to the tape drive when it detects that a 60-megabyte tape has been installed in the tape drive. This signal causes the tape drive to increase its write current.
RDP-	26	Read-data pulses. This output signal sends serial data to the controller when recorded data passes under the read head.
UTH- LTH-	28 30	Upper and lower tape hole position codes. These output signals indicate to the controller the specific position of the tape based on the position of the tape holes with respect to the drive's tape hole sensors.
SLD-	32	Selected response from tape drive. This output signal indicates to the controller that the tape drive has recognized and responded to a DS0- signal.
CIN-	34	Cartridge in place. This output signal indicates to the controller that a tape cartridge has been inserted in the tape drive.
USF-	36	Unsafe. The tape drive activates this output signal to notify the tape controller that it has detected a write-protected tape cartridge. When active, this signal prevents any write or erase operations to the tape.

Table 6-46 Tape Drive Interface Signals -- Connector J1 (Cont)

Signal	Pin Number	Description
TCH-	38	Capstan tachometer pulse. The controller generates eight of these pulses for each capstan revolution to control the capstan speed. Each occurrence of TCH- represents a tape movement of 0.145 ±0.003 inch since the last occurrence.
WDA- WDA+	40 42	Write-data. This differential signal pair is sent to the standard interface during the time of an active write-enable signal. The tape drive records data at a nominal rate of 10 000 flux transitions per inch or a data density of 8 000 bits per inch.
THD-	44	Read threshold. This input signal causes the tape drive read threshold to invoke a 35-percent qualifying amplitude threshold.
	46	Not used.
WEN-	48	Write-enable control. This input signal allows write data to be gated to the tape drive write head.
EEN-	50	Erase-enable control. Activation of this input signal and selecting track 0 causes the tape drive to erase the entire tape.

NOTE:

All odd-numbered pins are connected to ground.

Table 6-47 Tape Position Codes

UTH-	LTH-	Tape Location
1	1	Beginning-of-tape (BOT). The BOT holes are located nearest the recording area just to the right of the tape hole sensor.
0	1	End-of-tape (EOT). The EOT holes are located nearest the recording area just to the left of the tape hole sensor.
1	0	Warning zone. The tape hole sensor is located between the BOT hole and the load-point hole.
0	0	Recording zone. If a BOT or an EOT position has occurred since the last tape cartridge insertion, this code indicates that the tape sensor is located between the load-point hole and the early-warning hole. Otherwise, this code indicates that the tape position is unknown.

Table 6-48 Tape Drive Power Connector J2

Pin	Voltage
1	+12 volts dc
2	+12 volts dc return
3	+5 volts dc
4	+5 volts dc return

Table 6-49 Tape Drive Performance Specifications

Characteristic	Specification
Number of tracks	9
Number of write head gaps	2
Number of read head gaps	2
Capacity:	
DC600A cartridge	60 megabytes
DC300XL cartridge	45 megabytes
Tape Speed	90 ±0.27 inches per second (ips) long term (greater than 180 inches)
	90 ±0.63 ips short term (less than 180 inches)
Backup time at 90 ips nonstop:	
DC600A cartridge	12 minutes
DC300XL cartridge	9 minutes
Track capacity:	
DC600A cartridge	6.67 megabytes
DC300XL cartridge	5.0 megabytes
Recording mode	Nonreturn-to-zero -- change on ones (NRZI)
Recording data density	8 000 bits per inch
Encoding method	4 to 5 run-length limited (RLL)
Flux density	10 000 flux transitions per inch
Data transfer rate	90 bytes per second
Start/stop time	300 milliseconds (maximum)

Table 6-50 Tape Drive Power Requirements

Item	Value
Operating current:	
+5 volts dc line	0.6 ampere (maximum)
+12 volts dc line	1.6 ±0.8 amperes (cartridge dependent)
Tape start/stop surge current:	
+5 volts dc line	0.6 ampere (maximum)
+12 volts dc line	4.4 amperes for 300 milliseconds (maximum)
Power consumption:	
Continuous streaming	32 watts (total)
Start/stop power surges	59 watts (total)

6.3.10.3 Tape Controller. The tape controller plugs into one of the BUSINESS-PRO computer's option slots and serves as an interface between the host expansion bus and the tape drive. Tables 6-51 through 6-56 provide tabulated information about the tape controller.

Table 6-51 Tape Controller/Expansion Bus Interface Signals

Signal Name	Pin Number	Description
	A01	Not used by the tape system.
XD7 XD6 XD5 XD4 XD3 XD2 XD1 XD0	A02 A03 A04 A05 A06 A07 A08 A09	Data 0 through 7. These bidirectional data lines handle all data transfers between the host and the tape system. XDO is the least-significant bit; XD7 is the most-significant. These lines are placed in their tristate condition when not in use.
	A10	Not used by the tape system.
AEN	A11	Address enable. This active high signal prevents both writing to and reading from the I/O base address through I/O base address plus seven. This allows data transfers under DMA control.
XA19 XA18 XA17 XA16 XA15 XA14 XA13 XA12 XA11 XA10 XA9 XA8 XA7 XA6 XA5 XA4 XA3 XA2 XA1 XA0	A12 A13 A14 A15 A16 A17 A18 A19 A20 A21 A22 A23 A24 A25 A26 A27 A28 A29 A30 A31	Address 0 through 19. These lines carry the low 20 bits of the system address. Address 0 is the least-significant bit; Address 19 is the most-significant bit. The I/O address is established by comparing XA3 through XA9 with jumper settings on the controller. (The default setting is 220H.) The addresses of the status, control, and I/O data registers are offset from the base address as follows: Base address+0=data register. Base address+1=control and status register. Base address+2=DMA start address. Base address+3=DMA stop address. Base address+4=reserved. Base address+5=reserved. Base address+6=reserved. Base address+7=reserved. Base address+8=reserved.

Table 6-51 Controller/Expansion Bus Interface Signals (Continued)

Signal Name	Pin Number	Description
GND	B01	Ground.
DRST	B02	Drive reset. This active high signal resets the tape drive by causing the controller to write to the DMA stop register.
	B03	Not used by the tape system.
	B04	Not used by the tape system.
	B05	Not used by the tape system.
DRQ3 DRQ2 DRQ1	B16 B06 B18	DMA request lines. These controller output signals generate DMA requests to the host. Jumper settings on the controller determine which DMA request line is used. DRQ1 has the highest priority. These lines are placed in their tristate conditions when not being used by the controller to allow other expansion bus devices to use them.
	B07	Not used by the tape system.
	B08	Not used by the tape system.
+12V	B09	+12 volts dc from the host power supply.
GND	B10	Ground.
	B11	Not used by the tape system.
	B12	Not used by the tape system.
IOWC-	B13	I/O write. The rising edge of this active low signal latches commands and data into the controller's I/O registers during an I/O cycle.
IORC-	B14	I/O read. This active low signal causes the controller to place data or status information on the data lines during an I/O cycle.

Table 6-51 Controller/Expansion Bus Interface Signals (Continued)

Signal Name	Pin Number	Description
DACK3- DACK2- DACK1-	B15 B26 B17	DMA acknowledge. These active low signals indicate to the controller that the host is ready to proceed with a pending DMA cycle. A set of jumpers on the controller establishes which DMA acknowledge line is used. The acknowledge and request lines must be set to the same priority.
	B19	Not used by the tape system.
	B20	Not used by the tape system.
CXIR7 CXIR6 XIR5 CXIR4 CXIR3	B21 B22 B23 B24 B25	Interrupt requests. These signals generate interrupt requests to the host. Jumper settings on the controller determine which one of the interrupts is being used. These lines are placed in their tristate conditions to allow other expansion bus devices to use them when they are not being used by the controller.
T/C	B27	Terminal count. This active high input to the controller indicates the end of a DMA cycle.
BALE	B28	Buffered address latch enable.
+5V	B29	+5 volts dc supply line.
14.3MHZ	B30	Oscillator. The controller generates its own oscillator signal from an on-board 3.579545-megahertz, crystal-controlled oscillator. Therefore, the controller does not use this host-generated oscillator signal.
GND	B31	Ground.

Table 6-52 Tape Controller Jumper Settings

Jumper	Position	Function
CC	In	Tape format. When installed, this jumper configures the controller for the QIC-24 tape format.
DD	Out	Tape speed. When not installed, this jumper configures the controller for a tape speed of 90 ips.
Y	In	Number of tracks. When installed, this jumper configures the controller for 9-track operation.
KK	In	Power-on confidence test. When installed, this jumper enables the power-on confidence test.
A9 A8 A7 A6 A5 A4 A3	In Out Out Out In Out Out	I/O register base address. This configuration of jumpers A3 through A9 sets the base register address to 220H.
DRQ1 DRQ2 DRQ3	Out Out In	DMA channel. This configuration of jumpers DRQ1 through DRQ3 selects channel 3.
DAK1 DAK2 DAK3	Out Out In	DMA acknowledge. This must match the DRQ selection.
IRQ2 IRQ3 IRQ4 IRQ5 IRQ6 IRQ7	Out In Out Out Out Out	Interrupt priority. This configuration of jumpers IRQ2 through selects IRQ3 as the interrupt level.
FF	Out	Loop on error. This jumper is for factory use only.
HH	Out	Test configuration. This jumper is for factory use only.
NN	Out	Not used.

Table 6-53 Tape Controller Diagnostic Indicators

LED Number	Definition
DS1	Controller chip error
DS2	RAM buffer chip error
DS3	Data separator logic error
DS4	Not used
DS5	Not used

Table 6-54 Tape Controller Registers

Register	Description
Data	The data register is an 8-bit register that can be either written to or read from. The data register is located at the I/O register base address with offset zero.
Control	The control register is an 8-bit register with individual bits that provide control information for the tape system. The control register is located at the I/O register base address plus one. Its individual bits provide the following control functions: Bit 0 -- Not used. Bit 1 -- Not used. Bit 2 -- Not used. Bit 3 -- Not used. Bit 4 -- Done interrupt enable (DNIEN). Activation of this bit while the IEN bit is high gates the operation-completed condition onto the selected interrupt line (IRQ5-).

Table 6-54 Tape Controller Registers (Continued)

Register	Description
Control (Continued)	
	Bit 5 -- Interrupt enable (IEN). Activation of this bit gates an interrupt condition onto the selected interrupt request line (DRQ3-).
	Bit 6 -- Request (REQ). Activation of this bit indicates that the host has written command information to or has read status information from the data register.
	Bit 7 -- Reset controller microprocessor. Activation of this bit for a period of at least 25 microseconds resets the controller microprocessor and initiates a power-on confidence test.
Status	The status register is an 8-bit register that provides certain status information to the host. The status register is located at the I/O register base address plus one. The individual bits provide the following status information:
	Bit 0 -- Not used.
	Bit 1 -- Not used.
	Bit 2 -- Not used.
	Bit 3 -- Direction (DIRC). This bit controls the data-transfer direction between the controller and the host. Its high state indicates that the transfer direction is from the host to the controller.
	Bit 4 -- Done (DONE). When active, this bit indicates that a data transfer between the controller and the data bus is complete.
	Bit 5 -- Exception (EXC). When low, this bit indicates to the host that an exception condition exists. The host must issue a status command to determine the cause of the condition.

Table 6-54 Tape Controller Registers (Continued)

Register	Description
Status (Continued)	
	Bit 6 -- Ready (RDY). When low, this bit indicates one of the following conditions: Command data has been taken from the data bus. Status data has been gated to the data bus. Either a BOT command, an Erase command, or a Cartridge Initialization command has been completed. A Write File Mark command has been completed. The tape system is ready to receive a block of data, a Write command, or a Write File Mark command. The tape system is ready to transmit the next block of data or is ready to receive a Read command or a Read File Mark command. The controller is ready to receive a command.
	Bit 7 -- Interrupt request flag (IRQF). When low, this bit indicates an active interrupt request.
Start DMA	Writing to this 8-bit register initiates a DMA request. The start DMA register is located at the I/O register base address plus two.
Stop DMA	Writing to this 8-bit register turns the DMA bit off. The start DMA register is located at the I/O register base address plus three.

Table 6-55 Tape Controller Performance Specifications

Characteristic	Specification
Host bus size	8 bits
Tape drive interface	Compatible with QIC-36
Tape format	QIC-24
Command set	Subset of QIC-02
Tape speed	90 inches per second
Number of tracks	9
Block size	512 bytes
Shipping configuration:	
I/O register base address	220H
DMA request channel	DRQ3
DMA acknowledge	DAK3
Interrupt request	IRQ3

Table 6-56 Tape Controller Power Requirements

Item	Value
Regulation:	
+5 volts dc line	±5 percent
+12 volts dc line	±5 percent
Ripple content (peak-to-peak):	
+5 volts dc line	100 millivolts
+12 volts dc line	50 millivolts
Operating current:	
+5 volts dc line	0.85 ampere (typical) 1.25 amperes (maximum)
+12 volts dc line	85 milliamperes (typical) 100 milliamperes (maximum)
Power consumption:	
Total	5.27 watts
Maximum	7.82 watts

6.4 VIDEO OPTIONS

The video options provide a variety of monitor configurations with convenient connectors for the mouse and keyboard. The following video options are available:

* TI mode video controller
* PC-AT mode video controller
* Color display unit
* Monochrome display unit

The following paragraphs describe the video options.

6.4.1 Video Controllers

Two optional video controllers allow the user to choose between TI mode or PC-AT mode video operations. The following paragraphs provide information about the two controllers: the TI mode CRT controller and the PC-AT mode CRT controller.

6.4.1.1 TI Mode CRT Controller. The optional TI mode CRT (cathode ray tube) controller is a full-sized, 16-bit board that supports TIPC alphanumeric and 3-plane graphics. The controller can display 256 different characters with the following attributes:

* Eight colors/levels of intensity
* Reverse video
* Underline
* Nondisplay (blank)
* Blink

NOTE

The TI mode CRT controller does not support either an external character font or the second set of character codes available on the TIPC.

TI Mode CRT Controller Kit. The TI mode CRT controller kit, TI Part No. 2240967-0001 includes the following items:

* TI mode CRT controller, TI Part No. 2240937-0001
* TI Mode CRT Controller manual, TI Part No. 2241034-0001

Tables 6-57 through 6-60 provide tabulated information about the TI mode CRT controller.

NOTE

This controller provides interfaces to the attached monitor and to the PC-AT controller (if present). The monitor interface is via connector J3; the PC-AT interface is via connector J4. Tables 6-57 and 6-58 describe the signals at connectors J3 and J4, respectively.

Table 6-57 TI Mode CRT Controller/Monitor Interface Connector J3

Signal	Pin Number	Description
MODE SELECT	1	Mode select. The controller generates this signal to select either the TI mode or the PC-AT mode of operation. The low state of the signal places the video monitor in the TI mode; the high state places it in the PC-AT mode.
H SYNC	2	Horizontal synchronization for the attached video monitor.
V SYNC	3	Vertical synchronization for the attached video monitor (active low).
RED GREEN BLUE INTENSITY	4 6 8 10	Red video, green video, blue video, and video intensity. These signals form a 4-bit code that determines the color to be displayed on the video monitor. See the Color Display Unit section.

NOTES:

The cable shield connects to chassis ground.

Pins 5, 7, 9, 11, 12, and 13 are ground connections.

Pins 14 and 15 are not connected.

Table 6-58 TI Mode/PC-AT Mode Controller Interface Connector J4

Signal	Pin Number	Description
V RED V GRN V BLU INTEN	1 3 5 7	Red video, green video, blue video, and video intensity. These signals are buffered versions of the red, green, blue, and intensity signals described in Table 6-57.
H DRIVE	9	Horizontal synchronization. This signal is a buffered version of H SYNC described in Table 6-57.
V DRIVE	11	Vertical synchronization. This signal is a buffered version of V SYNC described in Table 6-57.
J5	13	U38 enable. When low, this signal enables buffer U38. This device buffers the color, intensity, and horizontal/vertical drive signals for the CRT controller.
TIPC-	15	Mode select. The controller generates this signal to select either the TI mode or the PC-AT mode of operation. The low state of the signal places the video monitor in the TI mode.

NOTE:

Pins 17 and 19 and all even-numbered pins are grounded.

Table 6-59 TI Mode CRT Controller Expansion Interface Signals

Signal	Connector and Pin Number	Description
NMI-	P1-1	Nonmaskable interrupt. This signal is activated by vertical-retrace when enabled by software.
GND	P1-2	Ground.
RESET	P1-4	Reset. Initializes the CRT controller board at power-up.
XD15	P2-35	Expansion data bus. These bidirectional data lines carry data between the CRT controller and the CPU.
XD14	P2-33	
XD13	P2-31	
XD12	P2-29	
XD11	P2-27	
XD10	P2-25	
XD9	P2-23	
XD8	P2-21	
XD7	P1-3	
XD6	P1-5	
XD5	P1-7	
XD4	P1-9	
XD3	P1-11	
XD2	P1-13	
XD1	P1-15	
XD0	P1-17	
+5V	P1-6	+5 volts dc for the CRT controller board.
WAIT-	P1-19	Wait. The CRT controller generates this signal to indicate to the MPU that the current memory cycle needs to be extended.
GND	P1-20	Ground.
AEN	P1-21	Address enable. The DMA controller on the main logic board generates this signal to indicate that it has acquired control of the system buses in order to perform a DMA cycle.

Table 6-59 TI Mode CRT Controller Expansion Interface Signals (Cont)

Signal	Connector and Pin Number	Description
IOWC-	P1-26	I/O write control. This signal indicates that an I/O write cycle to the CRT is in progress.
XA16	P1-29	Expansion address bus.
XA15	P1-31	
XA14	P1-33	
XA13	P1-35	
XA12	P1-37	
XA11	P1-39	
XA10	P1-41	
XA9	P1-43	
XA8	P1-45	
XA7	P1-47	
XA6	P1-49	
XA5	P1-51	
XA4	P1-53	
XA3	P1-55	
XA2	P1-57	
XA1	P1-59	
XA0	P1-61	
BALE	P1-56	Buffered address latch. The CPU uses this signal to indicate to the CRT controller that it is placing a valid address on the expansion address bus.
+5V	P1-58	+5 volts dc for the CRT controller board.
XBHE-	P2-1	Expansion bus high byte enable. The falling edge of BALE latches this signal to indicate that data is being transferred via the upper eight data lines (XD8 through XD15).
BA23	P2-3	Extended address lines. These lines extend the addressing capability of the expansion address bus to 16 megabytes.
BA22	P2-5	
BA21	P2-7	
BA20	P2-9	
BA19	P2-11	
BA18	P2-13	
BA17	P2-15	

Table 6-59 TI Mode CRT Controller Expansion Interface Signals (Cont)

Signal	Connector and Pin Number	Description
MRDC-	P2-17	Memory-read control. This signal indicates that a memory-read operation is in progress.
MWTC-	P2-19	Memory-write control. This signal indicates that a memory-write operation is in progress.
+5V	P2-32	+5 volts dc for the CRT controller.
MASTER-	P2-34	Master. The CRT controller monitors this line to detect DMA access.
GND	P2-36	Ground.

Table 6-60 TI Mode CRT Controller Performance Specifications

Characteristic	Specification
Graphics resolution	720 pixels (horizontal) by 300 pixels (vertical)
Character resolution	80 characters (horizontal) by 25 characters (vertical)
Total available characters	256
Size of character block	9 pixels (horizontal) by 12 pixels (vertical)
Character attributes	Nondisplay (blank), underline, reverse video, blink, and colors/levels of intensity
Colors/levels of intensity	8
Horizontal scan rate	19 200 Hertz
Video bandwidth	18 megahertz

6.4.1.2 TI Mode CRT Controller Board. The CRT controller board supports either a monochrome or a color TTL (transistor-to-transistor logic) display and makes the BUSINESS-PRO computer a complete alphanumeric and raster graphics system.

The controller board provides one page of high-resolution (80 columns x 25 lines) alphanumeric display and 8 color graphics with a resolution of 720 x 300. The system makes no physical distinction between color and monochrome; the board supports output in 8-level gray scale or 8-color RGB (red, green, blue). Color is determined by the monitor used. For logic diagrams of this controller, refer to Appendix E, drawing number 2223011.

Table 6-61 lists the video ac parameters.

Table 6-61 Video AC Parameters

Ref	Parameter	Value
A	Video dot frequency	18.000 megahertz
B	Video dot pulsewidth	55.55 nanoseconds
C	Character block horizontal	9 dots
D	Character block vertical	12 dots
E	Number of character lines	25 rows
F	Characters/character line	80 columns
G	Number of active scan lines	300
H	Total scan lines	320
J	Vertical synchronization width	0.156 milliseconds
K	Vsync front porch	0.0 milliseconds
L	Vsync back porch	0.884 milliseconds
M	Vertical blanking interval	1.040 milliseconds
N	Active vertical display time	15.60 milliseconds
	Total vertical time	16.63 milliseconds
Q	Vertical rate	60.10 Hertz
R	Hsync width	4.50 microseconds
S	Hsync front porch	2.00 microseconds
T	Hsync back porch	5.50 microseconds
U	Horizontal blanking interval	12.00 microseconds
V	Active horizontal display time	39.99 microseconds
W	Total horizontal time	51.99 microseconds
X	Horizontal rate	19 231 Hertz

<u>Display Characteristics</u>. The display characteristics are as follows:

* A 7 x 9 character in a 9 x 12 image cell

* Twenty-five lines of 80 characters

* A resolution of 720 pixels horizontally x 300 pixels vertically

* A horizontal scan rate of 19 200 lines per second

* A vertical scan rate of 60 Hertz

* A dot rate of 18 megahertz

NOTE

The horizontal scan rate is an important consideration, because many monitors have a horizontal scan rate of 15 750. Only monitors having a horizontal scan rate of 19 200 lines per second can operate with the TI mode CRT controller.

<u>Address Map</u>. The TI mode CRT controller (referred to as the CRT controller in this section) is located at address ranges C0000H through DFFFFH for the CPU, and A0000H through BFFFFH for the bus masters and DMA controllers. However, the alpha board (TI Part No. 2223100-0001) and graphics board (TI Part No. 2223061-0002) used in the Texas Instruments Professional Computer (TIPC) are located at address range C0000H through DFFFFH. Since the TIPC does not allow DMA or bus masters, all current software is compatible.

The CRT controller actually decodes A0000H through B0000H. The main logic board inverts lines A17 and A18 on CPU accesses to A0000H through DFFFFH when the CRT controller is enabled (port 12H, bit 1=1). The CRT controller has been remapped to prevent potential conflicts with the option ROM space in the PC-AT mode, address range C0000H through DFFFFH. Table 6-62 shows the memory map. The bus masters and DMA controllers should use the expansion bus address to access the CRT controller, and the CPU should use the CPU address. When port 12H, bit 1=0, the CRT controller (with the exception of port 12H) is disabled. To read or write, any device on the CRT controller port 12H, bit 1 must equal 1.

NOTE

When the CRT controller is enabled, the option ROM space is at A0000H through BFFFFH for the CPU and C0000H through DFFFFH for bus masters and DMA.

Table 6-62 CRT System Memory Map

CPU Address (Hexadecimal)	Expansion Bus Address (Hexadecimal)	Purpose
C0000 to C7FFF	A0000 to A7FFF	Graphics plane A
C8000 to CFFFF	A8000 to AFFFF	Graphics RAM plane B
D0000 to D7FFF	B0000 to B7FFF	Graphics RAM plane C
DE000 to DE7FF	BE000 to BE7FF	Active character memory
DE800 to DEFFF	BE000 to BE7FF	Phantom character memory
DF000 Bit 0	BF000 Bit 0	Miscellaneous input buffer blue feedback, read-only
Bit 1	Bit 1	Miscellaneous input buffer red feedback, read-only
Bit 2	Bit 2	Miscellaneous input buffer green feedback, read-only
Bit 3	Bit 3	Miscellaneous input buffer interrupt pending, read-only
DF010	BF010	Graphics blue palette latch write-only
DF020	BF020	Graphics green palette latch write-only
DF030	BF030	Graphics red palette latch write-only
DF810	BF810	CRTC address register, write-only
DF811	BF811	CRTC status register, write-only
DF812	BF812	CRTC registers write access, write-only
DF813	BF813	CRTC registers read access, read-only
DF820 Bit 7	BF820 Bit 7	Miscellaneous output latch, interrupt enable
DF820 Bit 6	BF820 Bit 6	Miscellaneous output latch, alphanumeric screen enable
0012 Bit 1	(I/O Map)	High=CRT controller enabled for alpha graphics board. Low=CRT controller disabled.

Character Attributes. The video memory of the controller is organized as 2 kilobytes x 16 bits. The first 8 bits convey character information. The second 8 bits select the following attributes on a character basis:

Bit	Description
0	Intensity level 1 (Blue)
1	Intensity level 2 (Red)
2	Intensity level 4 (Green)
3	Character enable
4	Reverse
5	Underline
6	Blink
7	Not used

NOTE

The three intensity bits (bit 0 through bit 2) determine the gray scale intensity level and the red-green-blue (RGB) outputs for color. Thus, normal monochrome video is handled by a one-of-eight intensity select, instead of a high-intensity bit.

To access the character attributes, the software writes the attribute values into an attribute latch. The attribute value is then assigned to the character each time that a character is written to the screen (until a screen read operation is done).

When any character on the screen is read, its attributes are copied to the attribute latch. These values are then read by a subsequent latch read operation.

Handling the attributes by this method ensures that in block moves (moving data from one screen area to another) the characters retain their attributes.

Character Sets. The video controller contains a 4-kilobyte character generator ROM, which contributes 256 characters. This ROM is internal to the video generator (VG).

Scrolling. The hardware maintains a screen start register that supports character line scrolling in four directions. The software determines the need for a scroll, then changes the value of this register by one line. The screen appears to jump by one line. The scrolling operation always affects all of the screen. You cannot scroll one region without affecting another.

Since screen memory is limited to 2 kilobytes, a scrolling operation results in a page wrap; that is, the original top line of the screen moves to the bottom of the screen. Therefore, the software must clear the top line of the screen (or bottom) before the scroll-up (or scroll-down) operation takes place. To simplify programming of the line clear operation, the 2 kilobytes of memory overlays a 4-kilobyte address space.

Status lines must be implemented in software. That is, during scroll operations, the status line must be moved to its new memory position before writing. The screen start register changes the screen-to-memory correspondence.

<u>CRT Controller IC</u>. The CRT controller (CRTC) IC (6845EA) contains the logic for:

* Generating the horizontal and vertical synchronizing signals
* Blanking display during retrace
* Addressing screen memory during screen refresh
* Cursor coincidence
* Starting screen display registers for use in scrolling

The CRTC contains 18 registers that must be appropriately set before board operation begins. To access these registers, the CPU first writes the address of the register to be accessed into the CRTC address register. Then, information can be written to that register. When writing to or reading from (where applicable) the data register, the information is accessed by the address latched in the address register.

Table 6-63 shows how to program these registers, using the signals chip select (CS), register select (RS), and read/write (R/W-). Assume the following conditions:

* A character rate (SWM-) of 2.0 megahertz
* 12 lines per character block
* 25 rows on the display
* 24 character times of horizontal blanking (12.0 microseconds)
* 20 line times of vertical blanking (1.04 milliseconds)

For more detailed programming information, refer to <u>The Rockwell Data Book</u>.

Table 6-63 CRTC Programming Values

Signal Name CS-	A1	VA0	Register Address	Register Name	Refresh Rate 60 Hertz
H	X	X	--	No register selected	--
L	L	L	--	Set address register	--
L	L	H	--	Read status register	--
L	H	L	0	Horizontal total characters minus one	103
L	H	L	1	Horizontal displayed characters	80
L	H	L	2	Horizontal sync position	84
L	H	L	3	VSYNC width, HSYNC width	39
L	H	L	4	Vertical total rows minus 1	24
L	H	L	5	Vertical adjust lines	20
L	H	L	6	Vertical displayed rows	25
L	H	L	7	Vertical sync position	25
L	H	L	8	Mode control	00
L	H	L	9	Scan lines per row minus 1	11
L	H	L	10	Cursor start line and BLINK	40
L	H	L	11	Cursor end line	11
L	H	L	12	Display start address high	00
L	H	L	13	Display start address low	00
L	H	X	14	Cursor position address high	00
L	H	X	15	Cursor position address low	00
L	H	H	16	Light pen position address high	--
L	H	H	17	Light pen position address low	--

NOTE:

H=High signal; L=Low signal; X=Don't care.

<u>CRT Screen/CPU Arbitration Logic Subsystem</u>. The CRT controller arbitration logic gives the programmer free access to the CRT display. The refresh memory and its control logic allow two complete memory cycles between each character displayed on the screen, so there is very little overhead time caused by arbitration conflicts. One cycle accesses the character for display; the CPU uses the other cycle for read or write operations. Therefore, the CPU waits less than two display-character times for memory access.

All alphanumerics address decode and timing are controlled by the data address bus selector (DABS). The attribute logic, character ROM, and mixing of alphanumerics and graphics are internal to the video generator (VG).

Attribute Interaction. The attributes available for use with the character display can be used in any of 128 possible combinations. The following paragraphs explain what happens when several attributes are active at the same time.

The attributes have a priority in their effects, and the highest priority attributes affect all attributes that have a lower priority. The order of priority is as follows:

Highest	Color attributes (red, blue, green)
	Reverse video and cursor
	Character enable
	Blink
Lowest	Underline

For example, when the underline and blink attributes are set, both character and underline blink. When the character enable is set to disable, no character, underline, or blinking activity is present. When reverse video and blink are set, the character goes on and off, the background is lighted, and the foreground is dark and blinking. When the character enable is set to disable and reverse video is set, the entire cell is lighted (according to the color attributes).

The color attributes define the characteristics of the light portion of the character, that is, either the color (when a color monitor is used) or the intensity (when a monochrome monitor is used).

When graphics are used with alphanumerics, the graphics screen shows through the dark portion of the alphanumeric character display. Table 6-64 gives the mapping of colors to intensity in the video output.

Table 6-64 Color Map

Code	Color	Monochrome Intensity Level
000	Black	0
001	Blue	1
010	Red	4
011	Magenta	5
100	Green	2
101	Cyan	3
110	Yellow	6
111	White	7

To blank the alphanumerics display to black, set the CRT Enable bit in the miscellaneous output latch to low. The board enters this state on power-up.

CRT Interrupt Logic Subsystem. The CRTC board contains a logic subsystem that allows the CRTC to generate an interrupt during the vertical interval. The processor uses this interrupt when doing scrolls with a status line or other operations that must be done during the vertical blanking interval. To enable this interrupt, set the Interrupt Enable bit in the miscellaneous latch to high. Vertical blanking generates the CPU nonmaskable interrupt and sets the Interrupt Pending bit. This bit is read from the miscellaneous buffer. To reset the interrupt, set the Interrupt Enable bit to low.

6.4.1.3 Diagnostic Loopback. One diagnostic test requires that the three color outputs be looped back to the miscellaneous input buffer so that the CPU can read them. Using a program with proper timing from the vertical interval, the CPU can check the action of the attribute bits and the graphics board palette circuits.

6.4.1.4 Graphics Controller Board. The graphics and the alphanumerics both use the same number of pixels on the screen: 720 horizontal by 300 vertical. Each pixel can contain a maximum of three attribute bits (labeled A, B, and C). These attribute bits are converted by a palette look-up table to three colors: red, blue, and green.

Aspects of the graphics controller board described in this section include:

* Pixel addressing
* Color selection
* Timing and synchronization
* Graphics logic array program

Pixel Addressing. Each dot on the graphics screen is a pixel. Each pixel has a 3-bit value associated with it that selects 1 of 8 palettes (0 through 7). Each palette is assigned 1 of 8 colors, as determined by the contents of the latch. The latch is simply an array of eight 3-bit values. The palette number of each pixel is an index into that array. So, the color of a pixel is the color value of the latch entry that corresponds to the palette number of the pixel. Changing either the palette or the color assigned to the palette changes the color of that pixel. Changing the color assigned to a palette changes the color of every pixel with the same palette number.

A plane is a block of memory containing 1 bit for each pixel in the display. Each of the 3 bits assigned to a pixel is in a different plane. All three planes are formatted identically; only the segment address differs from plane to plane. The segment addresses of the three planes are C000H, C800H, and D000H. For example, if a bit assigned to pixel (x, y) is the fifth bit of memory location C000:mmmm, then the other 2 bits assigned to that pixel are the fifth bits of locations C800:mmmm and D000:mmmm.

In Table 6-65, memory addresses refer to offsets into the segment of any of the three graphics planes. This illustration shows the organization of graphics screen memory into pixels. Pixels are numbered (x coordinate, y coordinate) and are zero relative.

Table 6-65 Organization of Graphics Screen Memory Into Pixels

Byte Address (Hex)	Pixels Represented			
0000-005B	(8,0-15,0)	(0,0-7,0)	(24,0-31,0)	(16,0-23,0)
005C-00B7	(8,1-15,1)	(0,1-7,1)	. . . .	
	.	.	.	
	.	.	.	

NOTES:

Pixel (0,0) is the MSB of location 0001.

Pixel (7,0) is the LSB of location 0001.

Pixel (8,0) is the MSB of location 0000.

Pixel (15,0) is the LSB of location 0000.

Pixel (16,0) is the MSB of location 0003.

The bytes are flip-flopped in this way so that if a move instruction is executed from a word in the graphics plane to a word register, the register then contains 16 consecutive pixel bits arranged from MSB to LSB. For example, if a MOV AX, ES:0000H is executed (where ES contains the segment address of the desired graphics plane), the MSB of AX is pixel (0,0) and the LSB is pixel (15,0). With this scheme, 45 words are necessary to represent the 720 pixels in each row of the display. One unused word appears at the end of each line, so a new row begins every 46 words, or 92 bytes. Line one (zero-relative) begins at byte address 92 decimal, 005CH. Therefore, pixel (0,1) is the MSB of location 005DH and pixel (8,1) is the MSB of location 005CH (because the bytes are flip-flopped).

Example:

To find the values of the rightmost 16 pixels on the bottom line of the display, use the following formula.

```
   299 (zero-relative number of last line on display)
  x 92 (bytes per line)
  - 88 (first word=0, second word=2, so 45th word=88)
 -----
27 596  (6BCCH)
```

So, MOV AX, ES:6BCC puts the values of the last 16 pixels on the display in AX, with the LSB of AX being the pixel in the lower right corner.

The three graphics planes are named A, B, and C. The segment addresses of the planes A, B, and C are C000H, C800H, and D000H, respectively. In determining the palette number of a pixel, the bit from the C plane is the most significant, the bit from the A plane is the least significant, and the B plane bit is in the middle.

Example:

To find the color of the pixel in the lower right corner of the display, first find the palette number assigned to it.

The MSB of the palette number is the LSB of D000H:6BCCH.

The middle bit of the palette number is the LSB of C800H:6BCCH.

The LSB of the palette number is the LSB of C000H:6BCCH.

For example, if these three bits are 1, 0, and 1, respectively, then the color of the lower right pixel is the color assigned to palette 5. If the default color assignments are in effect, the color of the pixel is cyan.

<u>Color Selection</u>. Each of the 8 entries in the latch has 1 bit for each of the 3 primary colors: green, red, and blue. The eight available colors are formed by combinations of those three colors, as listed in Table 6-66.

Table 6-66 Color Combinations

Green	Red	Blue	Color	Color Number
0	0	0	Black	0
0	0	1	Blue	1
0	1	0	Red	2
0	1	1	Magenta	3
1	0	0	Green	4
1	0	1	Cyan	5
1	1	0	Yellow	6
1	1	1	White	7

To access the latch, you must write all 8 bits of a particular primary color to the appropriate memory location for that color. You cannot change all 3 bits corresponding to one palette number in a single write operation. The latch consists of 3 memory locations, 1 for each of the primary colors. These locations are:

Blue latch	DF00:0010H
Green latch	DF00:0020H
Red latch	DF00:0030H

You can write to these locations, but you cannot read from them. For this reason, it is necessary to maintain a memory image of the 3 color latches if individual palettes are to be changed. You are then able to change a single palette by setting the appropriate bits in the memory image to the desired value and updating all 3 color latches.

Each of the 3 color bits of a palette is in the same bit position in all 3 color latches. However, the scheme for determining which bit in the latch is addressed by a pixel is not the same as determining the palette number. In determining the latch bit addressed by the 3-bit value assigned to a pixel, the B plane value is the most significant, and the C plane value is in the middle. The A plane value is still the least significant. Bit 7 is the MSB, and bit 0 is the LSB of the color latch byte. Table 6-67 displays the correspondence between the bits assigned to a pixel and the bit positions in any of the 3 color latches. It also shows the comparison of these bit positions to the palette numbers.

Table 6-67 Bit Correlations

B Plane Bit	C Plane Bit	A Plane Bit	Latch Bit Addressed	Palette Number
0	0	0	0	0
0	0	1	1	1
0	1	0	2	4
0	1	1	3	5
1	0	0	4	2
1	0	1	5	3
1	1	0	6	6
1	1	1	7	7

Table 6-68 shows this correspondence horizontally, so that the color latch byte appears as a byte register.

Table 6-68 Color Latch Byte

B plane bit	1	1	1	1	0	0	0	0
C plane bit	1	1	0	0	1	1	0	0
A plane bit	1	0	1	0	1	0	1	0
Latch bit addressed	7	6	5	4	3	2	1	0
Palette number	7	6	3	2	5	4	1	0

Example:

This example shows how to create a memory image of the default values of the three color latches.

Combining information from Table 6-66 with information from Table 6-67 yields the information necessary to construct Table 6-69.

Table 6-69 Default Values of Color Latches

Latch Bit	Palette Number (Color Number)	Green Bit	Red Bit	Blue Bit
7	7 (White)	1	1	1
6	6 (Yellow)	1	1	0
5	3 (Magenta)	0	1	1
4	2 (Red)	0	1	0
3	5 (Cyan)	1	0	1
2	4 (Green)	1	0	0
1	1 (Blue)	0	0	1
0	0 (Black)	0	0	0

The default condition is palette number=color number; therefore, the color latches are set as follows:

Green latch=11001100 binary=CCH at DF00:0020H

Red latch=1111000 binary=FOH at DF00:0030H

Blue latch=10101010 binary=AAH at DF00:0010H

Example:

The following example lists the steps necessary to change palette 3 to yellow from the default condition (magenta).

1. Find the desired palette number (three) in Table 6-69; then, find the associated latch bit (five).

2. Find the desired color (yellow) in Table 6-69; then, find the bit settings (red=1, green=1, blue=0).

3. Set bit five in each of the color latches to the values determined in the previous step. This change creates the new values:

   a. Green latch=11101100 binary=ECH

   b. Red latch=11110000 binary=FOH

   c. Blue latch=10001010 binary=8AH

4. Write the new values (from the previous step) to the three color latch addresses. (In this example, it is not necessary to change the red latch, because the value did not change.)

Timing and Synchronization.

The same dot clock that generates internal timing for the alphanumerics also clocks the graphics video. Monitoring the display enable (DE) signal from the CRTC chip (6845) helps to synchronize the pixel outputs from the alphanumerics. If the DE signal has been low for a long period, the graphics controller (CG) assumes that the scan is in the vertical interval. When DE goes high again, the GC resets the graphics memory and scan counters to zero. When DE is low for a short period (during horizontal retrace, for example), the scan counters are stopped. This places the last pixel on a line adjacent to the first pixel on the following line.

The graphics video controller gives the CPU free access to the screen memory. During a single screen display cycle, the hardware can access the refresh memory twice--once to read the data for screen display and once for the CPU to read or write data if needed. To provide enough time for this access, a display cycle accesses 16 adjacent pixels of 3 attribute bits each. These are read in parallel and loaded into three 16-bit shift registers for display. After the memory has been read for screen display, the CPU access cycle begins if a read or write cycle is requested.

Dynamic memory is used on the graphics video board because of the large amount of memory required. The memory chips are organized into 16 kilowords by 4 bits and are packaged in an 18-pin, dual-inline-package (DIP). The 8 address lines are multiplexed into 256 row addresses and 64 column addresses to get to the 16 000 locations in the memory. The addresses to the RAM also need to be multiplexed between the CPU and the refresh counter.

The graphics timing and address decode are controlled by graphics controller (GC). Palette latches, the DRAM data interface, and video shift registers are controlled by the graphics RAM interface (GRI).

6.4.1.5 TIPC Compatibility. On the TI mode CRTC, the memory maps are identical to current TIPC software. Otherwise, the alphanumerics/graphics board is compatible with TIPC software, except as follows:

* TI mode CRTC does not support an external character ROM.

* There is no composite video output. Conversion to black and white takes place in the monitor itself.

* The attribute latch operates differently from the TIPC attribute latch on a 16-bit read operation from alphanumeric memory. The TIPC places the attribute corresponding to the high byte in the attribute latch, while the BUSINESS-PRO places the low byte in the attribute latch.

* The TI mode CRTC has port 12H, which enables and/or disables the board.

* The monochrome grey scale does not match the current BUSINESS-PRO grey scale as shown in Table 6-70.

Table 6-70 TIPC vs BUSINESS-PRO Monochrome Compatibility

Code	Color	Current TIPC	BUSINESS-PRO
0 0 0	Black	0	0
0 0 1	Blue	1	1
0 1 0	Red	2	4
0 1 1	Magenta	3	5
1 0 0	Green	4	2
1 0 1	Cyan	5	3
1 1 0	Yellow	6	6
1 1 1	White	7	7

6.4.1.6 PC-AT Mode CRT Controller. The optional PC-AT mode CRT controller is a full-sized, 16-bit board that supports both PC-AT monochrome and PC-AT color applications. The controller provides an interface to the optional PC-AT monitors or any standard NTSC (National Television System Committee) format peripheral.

<u>Monochrome Mode Character Attributes</u>. The controller supports the following character attributes in monochrome (mono) mode:

* Highlight
* Reverse video
* White character/black background
* Underline
* Nondisplay (blank)
* Blink
* Connection for alternate video controller

<u>Color Mode Character Attributes</u>. The controller supports one of the following character attributes in color mode:

* Any of 16 foreground, any of 8 background, and blink
* Any o
* Any of ~~16 f~~oreground and any of 16 background

<u>PC-AT Mode CRT Controller Kit</u>. The PC-AT mode CRT controller kit, TI Part No. 2240968-0001, includes the following items:

* PC-AT mode CRT controller (dual mode video board), TI Part No. 2240940-0001
* PC-AT II alternate mode CRT controller, TI Part No. 2540315-0001
* CRT controller cable, TI Part No. 2240960-0001
* <u>PC-AT Mode CRT Controller</u> manual, TI Part No. 2241039-0001

<u>PC-AT Mode CRT Controller Tabulated Information</u>. Tables 6-71 through 6-75 provide tabulated information about the PC-AT mode CRT controller.

NOTE

The BUSINESS-PRO can contain either a basic PC-AT CRT controller or an alternate PC-AT II CRT controller, but it cannot contain both controllers at the same time. The J4 edge connector on the PC-AT CRT controller is tied to J4 on the TI mode CRT controller via a daisy-chain cable, TI Part No. 2240960-0001. The TI mode CRT controller then becomes a throughput channel and connects to the monitor via edge connector J3. Tables 6-71 and 6-72 describe the signals at connectors J3 and J4, respectively, for the PC-AT CRT controller.

Table 6-71 PC-AT Mode CRT Controller/Monitor Interface Connector J3

Signal	Pin Number	Description
CVM	1	Mode select. High=PCAT video rates; low=mono/TIPC video rate.
CVH	2	Horizontal synchronization for the attached video monitor.
CVV	3	Vertical synchronization for the attached video monitor.
CVR CVG CVB CVI	4 6 8 10	Red video, green video, blue video, and video intensity. These signals form a four-bit code that determines the color to be displayed on the video monitor.
EXTSYNC- *	14	External synchronization.

NOTES:

The cable shield connects to chassis ground.

Pins 5, 7, 9, 11, 12, and 13 are ground connections.

Pins 14 and 15 are not connected.

For TI monitors, HSYNC is a high pulse; VSYNC is a low pulse.

* Used on alternate PC-AT II controller only.

Table 6-72 lists and describes the pinouts of edge connector J4, which connects the PC-AT CRT controller to J4 of the TI mode CRT controller via a 20-pin daisy-chain cable.

Table 6-72 Interface Connector J4

Signal	Pin Number	Description
EXRED EXGRN EXBLU EXINT	1 3 5 7	Red video, green video, blue video, and video intensity. These signals are buffered versions of the red, green, blue, and intensity signals described in Table 6-71.
EXHORIZ	9	Horizontal synchronization. This signal is a buffered version of HSYNC described in Table 6-71.
EXVERT	11	Vertical synchronization. This signal is a buffered version of VSYNC described in Table 6-71.
+5V (VCC)	13	+5 volts dc supply line.
EXVIDON-	15	Board-enable signal from the TI mode CRT controller.
EXKCYC-	17	Used on PC-AT II CRT controller only. Selects monitor speed (see J3, pin 1).

NOTE:

Pin 19 and all even-numbered pins (2 through 20) are connected to ground.

Table 6-73 PC-AT Mode CRT Controller Expansion Interface Signals

Signal	Connector and Pin	Description
	P1-1	Not used.
GND	P1-2	Ground.
RESET	P1-4	Reset.
XD15	P2-35	Expansion data bus. These bidirectional data lines carry data between the CRT controller and the CPU.
XD14	P2-33	
XD13	P2-31	
XD12	P2-29	
XD11	P2-27	
XD10	P2-25	
XD9	P2-23	
XD8	P2-21	
XD7	P1-3	
XD6	P1-5	
XD5	P1-7	
XD4	P1-9	
XD3	P1-11	
XD2	P1-13	
XD1	P1-15	
XD0	P1-17	
+5V	P1-6	+5 volts dc for the CRT controller board.
WAIT-	P1-19	Wait. The CRT controller generates this signal to indicate to the MPU that the current memory cycle needs to be extended.
GND	P1-20	Ground.
AEN	P1-21	Address enable. The DMA controller on the main logic board generates this signal to indicate that it has acquired control of the system buses in order to perform a DMA cycle.
IOW-	P1-26	I/O write control. This signal indicates that an I/O write cycle is in progress.
IOR-	P1-28	I/O read command.

Table 6-73 PC-AT Mode Controller Expansion Interface Signals (Cont.)

Signal	Connector and Pin	Description
+12V	P1-22	+12 volts dc, for the light pen connector.
XA16	P1-29	Expansion address bus.
XA15	P1-31	
XA14	P1-33	
XA13	P1-35	
XA12	P1-37	
XA11	P1-39	
XA10	P1-41	
XA9	P1-43	
XA8	P1-45	
XA7	P1-47	
XA6	P1-49	
XA5	P1-51	
XA4	P1-53	
XA3	P1-55	
XA2	P1-57	
XA1	P1-59	
XA0	P1-61	
BALE	P1-56	Address latch enable. Falling edge indicates BA23 through BA17 are valid.
+5V	P1-58	+5 volts dc for the CRT controller board.
14.32MHZ	P1-60	Video clock for color mode.
XBHE-	P2-1	Expansion bus high byte enable. The falling edge of BALE latches this signal to indicate that data is being transferred via the upper eight data lines (XD8 through XD15).
BA23	P2-3	Extended address lines. These lines extend the addressing capability of the expansion address bus to 16 megabytes.
BA22	P2-5	
BA21	P2-7	
BA20	P2-9	
BA19	P2-11	
BA18	P2-13	
BA17	P2-15	
MRDC-	P1-24	Memory-read control. Indicates a memory-read operation is in progress in the lowest 1 megabyte of address space.

Table 6-73 PC-AT Mode Controller Expansion Interface Signals (Cont.)

Signal	Connector and Pin Number	Description
MWTC-	P1-22	Memory-write control. Indicates a memory-write operation is in progress in the lowest 1 megabyte of address space.
MEM16-	P2-2	Device indicates that it is capable of 16-bit memory transfers.
+5V	P2-32	+5 volts dc for the CRT controller.
MASTER-	P2-34	Master. The CRT controller monitors this signal line to detect DMA access.
GND	P2-36	Ground.

Table 6-74 Light Pen Enable Connector J5

Signal	Pin Number	Description
LPENIN	1	Low=light pen active. High to low transition indicates light pen detects something.
	2	No connection. Key for connector orientation.
LPENSW	3	Intended for switch from light pen.
GND	4	Ground.
+5V	5	+5 volts dc supply line.
+12V	6	+12 volts dc supply line.

Table 6-75 PC-AT CRT Controller Specifications

Characteristic	Specification
Monochrome mode:	
Character resolution	80 characters (horizontal) by 25 characters (vertical)
Characters available	256
Character block size	9 pixels (horizontal) by 12 pixels (vertical)
Character attributes	Nondisplay (blank), underline, reverse video, blink, highlight, and white character/black background
Horizontal scan rate	19.2 kilohertz
Video bandwidth	18 megahertz
Composite video output:	
Horizontal scan rate	15.75 kilohertz
Color burst	3.58 megahertz
Color/graphics, 80-character alphanumeric mode:	
Character resolution	80 characters (horizontal) by 25 characters (vertical)
Characters available	256
Character block size	8 pixels (horizontal) by 8 pixels (vertical)
Character attributes	16 foreground and 16 background colors or 16 foreground colors, 8 background, and blink
Horizontal scan rate	15.75 kilohertz
Video bandwidth	14.32 megahertz

Table 6-75 PC-AT CRT Controller Specifications (Continued)

Characteristic	Specification
Color/graphics, 40 character alphanumeric mode:	
Character resolution	40 characters (horizontal) by 25 characters (vertical)
Characters available	256
Character block size	8 pixels (horizontal) by 8 pixels (vertical)
Character attributes	16 foreground and 16 background colors or 16 foreground colors, 8 background, and blink
Horizontal scan rate	15.75 kilohertz
Video bandwidth	7.16 megahertz
Character resolution for the 640-dot, graphics mode	640 pixels (horizontal) by 200 pixels (vertical)
Character resolution for the 320-dot, graphics mode	320 pixels (horizontal) by 200 pixels (vertical)

6.4.1.7 PC-AT CRT Controller Operational Modes. The PC-AT mode CRT controller emulates the functions of the IBM monochrome and color/graphics display adapters. The operational mode of the controller is independent of the type of display unit actually being used with the controller.

PC-AT CRT Controller Configurations. The IBM compatible CRT controller has two versions. The earlier version is referred to as the PC-AT CRT controller, and the present production version is referred to as the PC-AT II CRT controller. Both controllers perform the same basic functions of an IBM monochrome and color/graphics adapter, and both have a connector (J4) for passing TIPC compatible video to the CRT monitor, but most of the differences are transparent to the system software. The primary difference between the two controllers is a 9-function DIP switch installed on the PC-AT II controller that allows the user to select options to customize the system. The BUSINESS-PRO is shipped from the factory with all switches set to ON. These switches are listed and described in Table 6-76 and are also discussed in detail in the paragraphs following the table.

Table 6-76 SW1 Selectable Options

Switch	Function	
1	Interface size select	
2	Vertical synchronization polarity	
3	Horizontal synchronization polarity	
4	Monochrome mode enable	
5	Monochrome RAM size select	
6 (LSB)	Port 12, bit 4	4-bit select code
7	Port 12, bit 5	
8	Port 12, bit 6	
9 (MSB)	Port 12, bit 7	

Switches 6 through 9 (SW1-1 through SW1-9) are described as follows:

* SW1-1 -- Two data sizes can be transferred on the PC-AT bus: 8-bit data (SW1-1 ON) and 16-bit data (SW1-1 OFF). Any controller board in the 0A000H through 0BFFFH address space that responds to DMA transfers must be an 8-bit controller, which is true for any system with an IBM compatible color/graphics adapter. In the standard TI configuration, SW1-1 is set to ON for 8-bit configuration.

* SW1-2 -- The polarity of the vertical synchonization signals going out of the digital port allows the incorporation of non-TI standard monitors into the system. In the standard TI configuration, SW1-1 is set to ON for low-pulse vertical synchronization.

* SW1-3 -- The polarity of the horizontal synchronization signals going out of the digital port are switch-selectable. This allows the use of non-TI CRT monitors. SW1-3 is set to ON for high pulse horizontal synchronization.

* SW1-4 -- This switch enables emulation of a monochrome adapter. When the switch is OFF, video equipment from another vendor can be installed.

* SW1-5 -- This switch selects monochrome RAM size: ON=4K-byte RAM; OFF=16K-byte RAM. IBM compatible monochrome boards have only 4K-bytes of controller RAM, while the BUSINESS-PRO has 16K-bytes of RAM required for color/graphics adapter emulation. SW1-5 enables extended RAM capability because when this switch is ON, the controller wraps around the 4K-byte RAM boundary.

* SW1-6 through SW1-9 -- These switches are matched against control bits 4 (LSB) through 7 (MSB) in I/O port 12. They are factory set to ON, which identifies the PC-AT II controller as unit 0. This allows placing up to 16 PC-AT II controllers, each with its own CRT on a system. Unit 0 is the only one initialized by the system ROM.

Other enhancements in the PC-AT II CRTC are as follows:

* EXTKCYC- signal is added to pin 17 of J4 interboard connector to allow use of a third-party video board that is compatible with either TI or IBM color/graphics CRT timing.

* EXTSYNC- is added to an external synchronization pin of the CRT controller IC which allows external equipment to put the PC-AT II controller into synchronization. The 6845 IC Data Manual contains the timing information for these functions.

NOTE

> On the PC-AT CRT controller, all registers and RAM are available at all times. On the PC-AT II alternate CRT controller, only those registers and RAM addresses belonging to the current mode are available.

Three major operational modes are possible with the PC-AT CRT controller. They are:

* Monochrome

* Color/graphics

* Pass-through (In conjunction with the TI-mode CRT controller)

Monochrome Mode. The monochrome mode is entered by writing data to the monochrome mode control port (3B8H). The controller must be in the monochrome mode to write to the monochrome data register (3B5H). I/O port 12H must also have bit 1 cleared (set to 0).

The I/O addresses available in the monochrome mode are shown in Table 6-77.

Table 6-77 PC-AT Controller Monochrome I/O Addresses

I/O Address (Hexadecimal)	Function
3B4	Monochrome index register
3B5	Monochrome data register
3B8	Monochrome mode control port
3BA	Monochrome mode status port

Any even address in the range 3B0H through 3B7H is the same as 3B4H, and any odd address in this range is the same as 3B5H. Port 3B4H is the index register that selects 1 of the 18 internal registers of the controller. Port 3B5H accesses the data selected by port 3B4H. Refer to Table 6-83 (CRT Timing Parameters) for the standard values to be set.

When the program writes to I/O port 3B8H, the PC-AT controller goes into the monochrome mode. The bits of port 3B8H are as follows:

Bit	Description
3	When high, display is enabled; when low, the screen is blank.
5	When high, blinking is enabled for alpha modes; when low, the blink attribute bit becomes background intensity control.

NOTE:

All other bits in port 3B8H are ignored.

When I/O port 3BAH is read, status is reported by its bits, as follows:

Bit	Description
0	When high, horizontal sync is active.
1	Blue bit loopback (Not IBM compatible).
2	Green bit loopback (Not IBM compatible).
3	Red bit loopback (IBM inputs white here).

Color/Graphics Mode. When the system writes data to the color/graphics control port (3D8H), the CRT controller goes into the color/graphics mode. Table 6-78 shows the I/O addresses available in the color/graphics mode.

Table 6-78 PC-AT CRTC Color/Graphics I/O Addresses

I/O Address (Hexadecimal)	Function
3D4	Color/graphics index register
3D5	Color/graphics data register
3D8	Color/graphics mode control port
3D9	Color/graphics color select register
3DA	Color/graphics mode status port
3DB	Clear light pen status
3DC	Set light pen status

Any even address in the range of 3D0H through 3D7H is the same as 3D4H, and any odd address in this range is the same as 3D5H. Port 3D5H is used to access the data selected by port 3D4H. Port 3D4H is the CRT controller index register that selects 1 of the 18 internal registers of the CRT controller. Refer to Table 6-83, CRT Timing Parameters, for the standard values to set.

In the color/graphics operational mode, the PC-AT CRT controller operates in one of the following modes:

* 40-character alphanumeric
* 80-character alphanumeric
* 320-dot graphics
* 640-dot graphics

Color/Graphics Mode Control, Port 3D8H. Writing to the color/graphics mode control port (3D8H) puts the controller in the color/graphics mode and selects the color/graphics mode (from those listed above) that is operational. Table 6-79 describes the bit functions of the control port.

Table 6-79 Bit Functions of Control Port 3D8H

Bits	Functions
0	80-character alphanumeric mode
1	320-dot or 640-dot graphics mode
2	Color burst disable (NOTE 1)
3	High=video enable; low=screen blank
4	640-dot graphics
5	Blink enable (NOTE 2)
6	Not used
7	Not used

NOTES:

1. Ignored on PC-AT; operates on PC-AT II; color burst is automatically disabled for higher resolution modes.

2. If high, blink is enabled for character modes; if low, this bit becomes background intensity control.

NOTE

The blink attribute alternates between a character and reverse video, rather than between a character and a blank cell.

Table 6-80 shows the bit values of the various graphics modes for the color/graphics mode control port 3D8H.

Table 6-80 Valid Color/Graphics Modes for 3D8H

Bits 5	4	3	2	1	0	Hex	Mode
1	0	1	0	0	0	28	40-character alphanumeric
1	0	1	0	0	1	29	80-character alphanumeric
0	0	1	0	1	0	0A	320-pixel graphics
0	1	1	0	1	0	1A	640-pixel graphics
0	0	0	0	0	0	00	Blank screen

Color Select Register Port 3D9H. I/O port 3D9H primarily controls the border color and is active in the write mode only. Table 6-81 describes the contents of the color select register.

Table 6-81 PC-AT CRT Controller Color Select Register

Bit	Alphanumeric Mode	320-Dot Graphics Mode	640-Dot Graphics Mode
0	Blue border	Blue border	Blue foreground
1	Green border	Green border	Green foreground
2	Red border	Red border	Red foreground
3	Border intensity	Border intensity	Foreground intensity
4	Not used	Blue for nonzero pixels	Not used
5	Not used	Intensity for nonzero pixels	Not used
6	Not used	Not used	Not used
7	Not used	Not used	Not used

NOTE:

Zero is the standard setting for all modes.

NOTE

In the 320-dot graphics mode, the border color defined by bits 0 through 3 is also the color selected for pixel code 0.

When the controller is in either the alphanumeric mode or the 320-dot graphics mode, the first nibble is the border color. In the 640-dot graphics mode, there is no border, and the first nibble becomes the foreground color (usually white). Bits 4 and 5 are relevant only in the 320-dot graphics mode where they provide the blue and intensity values for all nonzero pixels. IBM terminology describes this as palette select.

<u>Light Pen Ports 3DCH and 3DBH</u>. From a programming point of view, the light pen interface consists of the Set Light Pen Status command (3DCH), the Clear Light Pen Status command (3DBH), and the color/graphics mode status port 3DAH. The light pen sets a flip-flop that is read via the 3DA status port. Writing data to light pen control port 3DBH resets the flip-flop and clears the light pen status. Data written to the light pen control I/O port 3DCH sets the light pen status.

<u>Status Port 3DAH</u>. The color/graphics mode status port (3DAH) is a read-only port. Table 6-82 lists and describes the bit functions of this status port.

Table 6-82 Bit Functions of Status Port 3DAH

Bits	Functions
0	When high, horizontal blanking is active.
1	When high, light pen is triggered.
2	When low, light pen switch is active.
3	When high, vertical synchronization is active.
4–7	Not used.

NOTE:

I/O ports 3DDH, 3DEH, 3DFH, 3B9H, and 3BBH read-only ports at these addresses cannot be created for other equipment.

Passthrough -- Alternate Video Port. Writing a logic 1 to bit 1 of port 12 (02) accesses the alternate video controller cable when the TI mode and PC-AT mode CRT controllers are connected together. The LSB of port 12H (01) determines the memory map of the expansion bus. When bit 1 is a logic 1, address ranges A/B and C/D are swapped. That is, CPU address 0CXXXXH appears as 0AXXXXH on the expansion bus. Standard settings are 00 or 11.

6.4.1.8 CRT Timing Parameters. The CRT controller contains 18 registers that must be programmed before operation of the controller begins. To access these registers, the CPU first writes the address of the register to be accessed into the CRTC register. Then, information can be written to that register. As a result of this operation, vertical and horizontal scan rates and other timing parameters are generated throughout the CRTC. Table 6-83 is a list of the registers that are written to and the data that is entered into each register to generate the CRT timing parameters.

Table 6-83 CRT Timing Parameters

CRTC Register	40-Char. Mode	320- or 640- Dot Graphics	80-Char. Mode	Monochrome Mode (NOTE 1)	
0	38	38	71	67	
1	28	28	50	50	
2	2D	2D	5A	54	
3	0A	0A	0A	39	
4	1F	7F	1F	18	
5	06	06	06	14	
6	19	64	19	19	
7	1C	70	1C	19	
8	02	02	02	00	
0	07	01	07	0B	
A (10)	06	X	06	0A	(NOTE 2)
B (11)	07	X	07	0B	(NOTE 3)
C (12)	0	00	0	0	(NOTE 4)
D (13)	0	00	0	0	
E (14)	0	X	0		(NOTE 5)
F (15)	0	X	0	0	
10 (16)	L	L	L	X	(NOTE 6)
11 (17)	L	L	L	X	

NOTES:

Values in this table are hexadecimal except those in parentheses.

X indicates "don't care."

0 instead of 00 implies that other values are possible.

Read the 6845 CRT controller manual (Rockwell Data Book) before using parameters different from those in this table.

1. Monochrome mode is not IBM compatible.

2. Start scan line of cursor.

3. End scan line of cursor.

4. The display start address is one-half the RAM address.

5. The cursor position is one-half the RAM address.

6. Registers 16 and 17 are light pen position addresses. These locations are 3 or 4 greater than the actual pen position.

Character Sets.

The character sets for the PC-AT mode CRT controller are contained in a 24-pin 8K-byte by 8 (8 kilobyte by 8 bit) ROM. The ROM contains two fonts: one for monochrome and one for color/graphics mode. The lower 4K is reserved for the color/graphics font, and the upper 4K is reserved for the monochrome font. The input address lines can be divided into three groups. The least significant 4 bits represent the scanline addresses; the next 8 bits represent the character code; and the remaining bit indicates the monochrome mode. Each character is stored in 16 successive bytes, with the MSB representing the leftmost column in the character cell.

In the color/graphics mode, the same font is used for both 40-character and 80-character displays; the 40-character mode doubles the dot width of the character. The LSB in color/graphics characters represents the rightmost bit in an 8-character cell. The ninth bit is active in only the monochrome mode and only for the characters in the range C0H through DFH. When active, it is the same as the eighth bit of the font ROM data.

6.4.2 Color Display Unit

The optional color display unit is a 13-inch, high-resolution video display unit whose dual-resolution capabilities allow it to be used with both the TI mode and the PC-AT mode video controllers. The unit mounts on a tilt/swivel base which contains the following connectors:

* Two interchangeable keyboard/mouse connectors

* A data interface connector

* A power connector

The unit enclosure also contains an audio speaker. Both domestic and international versions of the display unit are available.

6.4.2.1 Color Display Unit Kit. The domestic color display unit kit, TI Part No. 2240805-8003, includes the following items:

* Color display unit, TI Part No. 2240805-0003

* Monitor cable set, TI Part No. 2534995-0001

* Color Display Unit manual, TI Part No. 2240838-0001

The international color display unit kit, TI Part No. 2240805-8004 includes the following items:

* Color display unit, TI Part No. 2240805-0004

* Monitor cable set, TI Part No. 2534995-0001

* Power cable, 240 volt, 50 Hertz, TI Part No. 2534994-0002

* Color Display Unit manual, TI Part No. 2240838-0001

6.4.2.2 Color Display Unit Tabulated Information. Tables 6-84 through 6-89 provide tabulated information about the color display unit.

Table 6-84 Color Display Unit/Controller Interface Connector J2

Signal	Pin Number	Description
MODE SELECT	1	The CRT controller generates this signal to place the attached monitor in either the TI mode or the PC-AT mode. The low state of MODE places the monitor in the TI mode; the high state places it in the PC-AT mode.
HSYNC	2	Horizontal synchronization signal output from the CRT controller.
VSYNC	3	Vertical synchronization signal output from the CRT controller.
RED VIDEO GREEN VIDEO BLUE VIDEO INTENSITY	4 6 8 10	The state of these controller-generated signals determine the color displayed by the monitor.
SPEAKER	12	A timer on the main logic board generates this audio input to the monitor speaker.
	14	No connection.
	15	No connection.
KBDATA	17	Keyboard data. This is the bidirectional serial data line that carries data between the keyboard and the keyboard controller on the main logic board.
KBCLOCK	21	Keyboard clock. The keyboard generates this clock to synchronize data transfers between it and the keyboard controller on the main logic board.

Table 6-84 Color Display Unit/Controller Interface Connector J2 (Cont)

Signal	Pin Number	Description
MOUSEDATA	23	Mouse data. This line carries the serial data from the mouse to the main logic board.
+5V	22	+5 volts dc supply voltage for the monitor.

NOTE:

Pin 19 is reserved. Pins 14, 15, 24, and 25 are not connected.

Pins 5, 7, 9, 11, 13, 16, 18, and 20 are connected to ground.

The connector shield is connected to chassis ground.

6.4.2.3 Displayed Colors. The RED VIDEO, GREEN VIDEO, BLUE VIDEO and INTENSITY input signals determine the colors displayed by the color display unit. Table 6-85 lists the displayed colors and the signal-state combinations that cause them.

Table 6-85 Color Display Unit Color Map

Color	Signal State INTENSITY	RED	GREEN	BLUE
Black	0	0	0	0
Blue	0	0	0	1
Green	0	0	1	0
Cyan	0	0	1	1
Red	0	1	0	0
Magenta	0	1	0	1
Brown	0	1	1	0
White	0	1	1	1
Gray	1	0	0	0
Light blue	1	0	0	1
Light green	1	0	1	0
Light cyan	1	0	1	1
Light red	1	1	0	0
Light magenta	1	1	0	1
Yellow	1	1	1	0
White	1	1	1	1

Table 6-86 Color Display Unit Video AC Parameters

Parameter	TI Mode/Mono Mode	PC-AT Mode
Video dot rate	18.000 megahertz	14.318 megahertz
Video dot time	55.550 nanoseconds	69.840 nanoseconds
Active scan lines	300	200
VSYNC pulse width	0.156 milliseconds	1.020 milliseconds
VSYNCH front porch	0.000 milliseconds	1.530 milliseconds
VSYNCH back porch	0.884 milliseconds	1.400 milliseconds
Vertical retrace	1.040 milliseconds	3.950 milliseconds
Vertical display time:		
Active	15.600 milliseconds	12.740 milliseconds
Total	16.640 milliseconds	16.690 milliseconds
Vertical rate	60.100 Hertz	59.920 Hertz
HSYNC pulse width	4.500 microseconds	4.470 microseconds
HSYNC front porch	2.000 microseconds	5.590 microseconds
HSYNC back porch	5.500 microseconds	8.940 microseconds
Horizontal retrace	12.000 microseconds	19.000 microseconds
Horizontal display time:		
Active	40.000 microseconds	44.700 microseconds
Total	52.000 microseconds	63.700 microseconds
Horizontal rate	19.231 kilohertz	15.700 kilohertz
Total scan lines	320	262
Horizontal pixels	720	640

6.4.2.4 Keyboard/Mouse Cable Connector J4. Two identical connectors (both labeled J4) located at the front of the display unit base allow the user to connect both a keyboard and/or a mouse. Both connectors are identical; therefore, you can use either one for the keyboard or the mouse. Table 6-87 lists the connector signals and their assigned pin numbers.

Table 6-87 Keyboard/Mouse Connector J4

Signal	Pin Number	Description
KBCLOCK	1	Keyboard clock. The keyboard generates this clock to synchronize data over the keyboard data line.
KBDATA	2	Keyboard data. Bidirectional data line that handles the bit-serial data transfers between the keyboard and the main logic board.
	3	Reserved.
GND	4	Ground.
+5V	5	+5 volts dc.
MOUSEDATA	6	Mouse data line. Bit-serial data line that transfers data from the mouse to the main logic board.
SPEAKER	7	Speaker. Audio output from the speaker amplifier on the main logic board.
GND	8	Ground.

NOTE:

The connector shield is connected to chassis ground.

Table 6-88 Color Display Unit Performance Specifications

Characteristic	Specification TI Mode/Mono Mode	 PC-AT Mode
Resolution	720 by 300 pixels	640 by 200 or 320 by 200 pixels
Colors displayed	8 (maximum)	16 (maximum)
Character resolution	25 rows by 80 columns	25 rows by 80 columns
Horizontal scan rate	19.231 kilohertz	15.700 kilohertz
Vertical scan rate	60.10 Hertz	59.92 Hertz
Video dot rate	18.000 megahertz	14.318 megahertz
Display size	9.45 by 7.09 inches	9.45 by 6.69 inches

Table 6-89 Color Display Unit AC Power Requirements

Item	Value Domestic Version	 International Version
Voltage	90 to 140 volts ac	180 to 264 volts ac
Frequency	57 to 63 Hertz	47 to 53 Hertz
Power	110 watts (maximum)	110 watts (maximum)

6.4.3 Monochrome Display Unit

The optional monochrome display unit is a 12-inch, medium-resolution monochrome monitor that features an anti-glare CRT display and medium-persistence (P42), green phosphor. The unit also features dual-mode resolution that allows it to be operated with either the TI mode or the PC-AT mode CRT controllers. The unit mounts on a tilt/swivel base that contains the following connectors:

* Two interchangeable keyboard/mouse connectors

* A data interface connector

* A power connector

The unit enclosure also contains an audio speaker. Both domestic and international versions of the display unit are available.

6.4.3.1 Monochrome Display Unit Kit. The domestic version of the monochrome display unit kit, TI Part No. 2240804-8001, includes the following items:

* Monochrome display unit, TI Part No. 2240804-0001

* Monitor cable set, TI Part No. 2534995-0001

* Power cable, 120 volt, 60 Hertz, TI Part No. 2534994-0001

* Monochrome Display Unit manual, TI Part No. 2240828-0001

The international version of the monochrome display unit kit, TI Part No. 2240804-8002, includes the following items:

* Monochrome display unit, TI Part No. 2240804-0002

* Monitor cable set, TI Part No. 2534995-0001

* Power cable, 240 volt, 50 Hertz, TI Part No. 2534994-0002

* Monochrome Display Unit manual, TI Part No. 2240828-0001

6.4.3.2 Monochrome Display Unit Tabulated Information. Tables 6-90 through 6-95 provide tabulated information about the monochrome display unit.

Table 6-90 Monochrome Display Unit/Controller Interface Connector J2

Signal	Pin Number	Description
MODE SELECT	1	The CRT controller generates this signal to place the attached monitor in either the TI mode or the PC-AT mode. The low state of MODE SELECT places the monitor in the TI mode; the high state places it in the PC-AT mode.
HSYNC	2	Horizontal synchronization signal output from the CRT controller.
VSYNC	3	Vertical synchronization signal output from the CRT controller.
RED VIDEO GREEN VIDEO BLUE VIDEO INTENSITY	4 6 8 10	The state of these controller-generated signals determine the intensity of the monitor screen display.
SPEAKER	12	A timer on the main logic board generates this audio input to the monitor speaker.
KBDATA	17	Keyboard data. This is the bidirectional serial data line that carries data between the keyboard and the keyboard controller on the main logic board.
KBCLOCK	21	Keyboard clock. The keyboard generates this clock to synchronize data transfers between the keyboard and the keyboard controller on the main logic board.

Table 6-90 Monochrome Display Unit/Controller Interface Connector J2

Signal	Pin Number	Description
+5V	22	+5 volts dc supply voltage for the monitor.
MOUSEDATA	23	Mouse data. This line carries the serial data from the mouse to the main logic board.

NOTE:

Pin 19 is reserved. Pins 14, 15, 24, and 25 are not connected.

Pins 5, 7, 9, 11, 13, 16, 18, and 20 are connected to ground.

The connector shield is connected to chassis ground.

6.4.3.3 Displayed Intensities. The RED VIDEO, GREEN VIDEO, BLUE VIDEO, and INTENSITY input signals determine the intensity level of the display screen. Table 6-91 lists the displayed intensities and the signal-state combinations that cause them.

Table 6-91 Monochrome Display Unit Intensity Levels

	Signal State			
Level	INTENSITY	RED	GREEN	BLUE
0 (Minimum)	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15 (Maximum)	1	1	1	1

Table 6-92 Monochrome Display Unit Video AC Parameters

Parameter	TI Mode/Mono Mode	PC-AT Mode
Video dot rate	18.000 megahertz	14.318 megahertz
Video dot time	55.55 nanoseconds	69.84 nanoseconds
Active scan lines	300	200
VSYNC pulse width	0.156 milliseconds	1.020 milliseconds
VSYNCH front porch	0.000 milliseconds	1.530 milliseconds
VSYNCH back porch	0.884 milliseconds	1.400 milliseconds
Vertical retrace	1.040 milliseconds	3.950 milliseconds
Vertical display time:		
Active	15.600 milliseconds	12.740 milliseconds
Total	16.640 milliseconds	16.690 milliseconds
Vertcal rate	60.100 Hertz	59.920 Hertz
HSYNC pulse width	4.500 microseconds	4.470 microseconds
HSYNC front porch	2.000 microseconds	5.590 microseconds
HSYNC back porch	5.500 microseconds	8.940 microseconds
Horizontal retrace	12.000 microseconds	19.000 microseconds
Horizontal display time:		
Active	40.000 microseconds	44.700 microseconds
Total	52.000 microseconds	63.700 microseconds
Horizontal rate	19.231 kilohertz	15.700 kilohertz
Total scan lines	320	262
Horizontal pixels	720	640

6.4.3.4 Keyboard/Mouse Cable Connector J4. Two identical connectors (both labeled J4) located at the front of the display unit base allow the user to connect both a keyboard and/or a mouse. Both connectors are identical. Therefore, you can use either one for the keyboard or the mouse. Table 6-93 lists the connector signals and their assigned pin numbers.

Table 6-93 Keyboard/Mouse Connector J4

Signal	Pin Number	Description
KBCLOCK	1	Keyboard clock. The keyboard generates this clock to synchronize data over the keyboard data line.
KBDATA	2	Keyboard data. Bidirectional data line that handles the bit-serial data transfers between the keyboard and the main logic board.
	3	Reserved.
GND	4	Ground.
+5V	5	+5 volts dc.
MOUSEDATA	6	Mouse data line. Bit-serial data that transfers data from the mouse to the main logic board.
SPEAKER	7	Speaker. Audio output from the speaker amplifier on the main logic board.
GND	8	Ground.

NOTE:

The connector shield is connected to chassis ground.

Table 6-94 Monochrome Display Unit Performance Specifications

Characteristic	Specification TI Mode/Mono Mode	PC-AT Mode
Resolution	720 by 300 pixels	640 by 200 or 320 by 200 pixels
Intensities displayed	8 (maximum)	16 (maximum)
Character resolution	25 rows by 80 columns	25 rows by 80 columns
Horizontal scan rate	19.231 kilohertz	15.700 kilohertz
Vertical scan rate	60.10 Hertz	59.92 Hertz
Video dot rate	18.000 megahertz	14.318 megahertz
Display size	8.11 by 6.06 inches	8.11 by 6.06 inches

Table 6-95 Monochrome Display Unit AC Power Requirements

Item	Value Domestic Version	International Version
Voltage	90 to 130 volts ac	200 to 250 volts ac
Frequency	57 to 63 Hertz	47 to 53 Hertz
Power	37 watts (maximum)	37 watts (maximum)

6.5 TI MODE RS-232 SERIAL INTERFACE

The optional TI mode video controller is a half-sized, 8-bit board that provides one of two switch-selectable TI communications ports. The controller handles asynchronous protocols as well as most synchronous protocols, including synchronous data link control (SDLC) and high-level data link control (HDLC). The board does not require the programming of any software delays when performing back-to-back I/O cycles.

6.5.1 TI Mode RS-232 Serial Interface Kit

The TI mode RS-232 serial interface kit, TI Part No. 2240969-0001, includes the following items:

* TI mode RS-232 serial interface board, TI Part No. 2240934-0001

* TI Mode RS-232 Serial Interface manual, TI Part No. 2241042-0001

NOTE

> The TI mode RS-232 serial interface can be programmed in the PC-AT mode, provided existing software is modified to address its I/O ports.

6.5.2 TI Mode RS-232 Serial Interface Tabulated Information

Tables 6-96 through 6-99 provide tabulated information about the TI mode RS-232 serial interface.

Table 6-96 TI Mode RS-232 Serial Interface Connector J1

Signal	Pin Number	Signal Name
AA	1	Chassis ground
BA	2	Transmitted data
BB	3	Received data
RTS/CA	4	Request-to-send
CTS/CB	5	Clear-to-send
DSR/CC	6	Data-set ready
AB	7	Signal ground
DCD/CF	8	Data carrier detect
SCA/CH	11	Secondary request-to-send
SCF/CI	12	Secondary clear-to-send
TXC/DB	15	Transmitter clock in
RSC/DD	17	Receiver clock in
DTR/CD	20	Data terminal ready
RI/CE	22	Ring indicator
SCA/CH	23	Secondary request-to-send
DA	24	External transmitter clock

NOTE:

Pins 9, 10, 13, 14, 16, 18, 19, 21, and 25 are not connected.

NOTE

When operated in the TI mode, IRQ10 and IRQ11 are rerouted by the hardware to IRQ0 and IRQ1, respectively for TI compatibility.

Table 6-97 Port-Selection Switches SW1-1 Through SW1-4

Port	Switch Settings SW1-1	SW1-2	SW1-3	SW1-4
1	ON	ON	OFF	OFF
2	OFF	OFF	ON	ON

Table 6-98 TI Mode RS-232 Serial Interface Port Addresses

Port 1 Address (Hex)	Port 2 Address (Hex)	Function
00E0	00E8	Interrupt acknowledge. An I/O write operation at this address followed by an I/O write operation performs an interrupt-acknowledge operation.
00E4	00EC	Channel B command. These addresses allow access to any 1 of 15 read or write registers that control the Z8530 operations.
00E5	00ED	Channel B data. These addresses are used to read received data and to write transmitted data.
00E6	00EE	Channel A command. These addresses allow access to any 1 of 15 read or write registers that control the Z8530 operations.
00E7	00EF	Channel A data. These addresses are used to read received data and to write transmitted data.

NOTES:

For additional information on programming the Z8530, refer to Zilog(R) literature.

Zilog is a registered trademark of Zilog Incorporated.

6.5.3 Baud Rate Generation

An on-board 4.9152-megahertz crystal oscillator and a divide-by-2 counter provide a clock for the internal baud rate generators of the Z8530. Table 6-99 lists the possible baud rates and their synchronous (sync) and asynchronous (async) program values.

Table 6-99 TI Mode RS-232 Interface Programmable Baud Rate Values

	Values		Error Percentage	
Baud Rate	Sync	Async	Sync	Async
19 200	62	2	0.000	0.000
9 600	126	6	0.000	0.000
7 200	169	9	-1.960	-3.030
4 800	254	14	0.000	0.000
3 600	339	19	0.098	1.587
2 400	510	30	0.000	0.000
2 000	612	36	0.065	1.053
1 800	681	41	-0.049	-0.775
1 200	1 022	62	0.000	0.000
600	2 046	26	0.000	0.000
300	4 094	54	0.000	0.000
200	6 142	82	0.000	0.000
150	8 190	10	0.000	0.000
134.5	9 134	69	0.001	0.001
110	11 169	96	-0.001	0.026
75	16 382	1 022	0.000	0.000
50	24 574	1 534	0.000	0.000

6.6 OPTICAL MOUSE

The optical mouse is an input-only device that detects the amount and direction of motion of the mouse on a 9-inch by 11-inch reflective pad. The mouse features three command buttons. The mouse communicates to the system through the serial port whose I/O address is determined by the position of the serial switch on the main logic board. The mouse connects to either of the 8-pin connectors on the front of either of the optional display units. The mouse is compatible with Mouse Systems M2.

6.6.1 Optical Mouse Kit

The optical mouse kit, TI Part No. 2536970-0001, includes the following items:

* Optical mouse and pad, TI Part No. 2240954-0001

* Optical Mouse manual, TI Part No. 2241060-0001

6.6.2 Optical Mouse Tabulated Information

Tables 6-100 through 6-102 provide tabulated information about the optical mouse.

Table 6-100 Optical Mouse Interface Signals

Signal	Pin Number	Description
GND	4	Ground.
+5V	5	+5 volts dc.
MOUSEDATA	6	Mouse data line. Bit-serial data line that transfers data from the mouse to the main logic board.
GND	8	Ground.

NOTE:

Pins 1, 2, 3, and 7 are not used by the mouse.

Table 6-101 Mouse Data Format

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	0	0	0	0	L	M	R
2	X7	X6	X5	X4	X3	X2	X1	X0
3	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
4	X7	X6	X5	X4	X3	X2	X1	X0
5	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

NOTES:

1. L, M, and R represent the reporting bits of the left, middle, and right command buttons, respectively. An activated button produces a zero bit.

2. Bytes 2 and 3 are the twos complement of report number n.

3. Bytes 4 and 5 are the twos complement of report number n+1.

4. X0 and Y0 are the least significant data bits.

Table 6-102 Optical Mouse Performance Specifications

Characteristic	Specification
Movement/data generation	Electro-optical
Resolution	100 lines per inch
Data sampling rate	20 reports per second (minimum)
Data rate	1 200 baud
Tracking velocity	30 inches per second (maximum)

6.7 80287 NUMERIC COPROCESSOR

The microprocessor and the coprocessor together compose the central processing unit of the BUSINESS-PRO computer. Either a 4-megahertz or an 8-megahertz 80287 coprocessor can be added to the CPU by inserting the coprocessor in the socket provided and setting the jumper plugs at J4 and J5 for the appropriate clock speeds.

NOTE

> When installing a coprocessor in the main logic board (TI Part No. 2240843-0001), no jumpers are required. The following information about jumpers J4 and J5 apply only to the main logic board (TI Part No. 2535670-0001).

When installing a coprocessor operating at 4 megahertz, insert a jumper plug between pins 1 and 2 of J4 and insert another at J5. For this operating mode, the coprocessor uses the same system clock as does the CPU. An internal divider in the coprocessor reduces this 12-megahertz clock to a frequency of 4 megahertz.

When installing an 8-megahertz coprocessor, insert the jumper between pins 2 and 3 of J4 and omit the jumper at J5. This configuration supplies an 8-megahertz, 1/3-duty cycle clock to the coprocessor. This clock is not internally divided, so with this configuration, the coprocessor runs at a frequency of 8 megahertz.

Since the coprocessor and the MPU operate in parallel, the MPU can continue to perform other functions while the coprocessor handles mathematical calculations. Both the coprocessor and the MPU decode the special escape instructions in the instruction stream, and the MPU supervises all data transfer operations and instruction execution for the coprocessor.

If the coprocessor is not present, the special escape instructions either have no effect or cause an exception. Therefore, the software should check for the presence of a coprocessor and use the appropriate routines as required. A math coprocessor presence bit is located in the RAM internal to the real-time clock (RTC) chip at bit 1 of address 0014H.

On receiving an instruction, the coprocessor activates its BUSY- signal to notify the MPU that instruction execution is in progress. The processor WAIT instruction then forces the MPU to wait for the results of the coprocessor calculation before processing other instructions.

If the appropriate coprocessor internal exception mask is not set, the device activates its ERROR- signal on detecting an exception condition. This ERROR- signal generates hardware interrupt 13 and causes the BUSY- signal to the MPU to latch in the busy state. An input/output (I/O) write operation to address 00F0H with D0 through D7 set to zero clears the BUSY- signal. If the coprocessor needs data to complete its calculation, it signals the MPU by activating the processor enable request (PEREQ) line, and the MPU acknowledges the request by activating the processor enable acknowledge (PEACK-) line.

As with the MPU, a system reset operation places the coprocessor in the real address mode from which it can be placed in the protected virtual address mode by an Enter Protected Mode (FSETPM) instruction. Just as with the MPU, the only way to return the coprocessor to the real address mode is to reset the device. The operating system can do this without affecting the MPU or any other circuitry by writing all zeros to data bits D0 through D7 at I/O port address 00F1H.

I/O ports 00F8H to 00FFH are reserved for the 80286/80287 interface. To guarantee correct operation of the coprocessor, programs must not perform any I/O operations to these addresses.

Appendix A

System Memory and I/O Maps

This appendix provides general maps of the BUSINESS-PRO memory and I/O addresses. Each table defines the address assignments for both the IBM Personal Computer AT (PC-AT) mode and the TI Professional Computer (TI) mode. Appendixes B and C provide detailed I/O maps for the TI mode and the PC-AT mode, respectively.

Table A-1 Memory Map (Real Mode)

Address Range (Hexadecimal)	PC-AT Mode	TI Mode
000000-07FFFF	512-kilobyte RAM	512-kilobyte RAM
080000-09FFFF	128-kilobyte RAM	128-kilobyte RAM
0A0000-0BFFFF	Video display RAM	Option memory
0C0000-0D7FFF	Option memory	Graphics ROM
0D8000-0DDFFF	Option memory	Reserved
0DE000-0DFFFF	Option memory	Char memory
0E0000-0EFFFF	Reserved	Reserved
0F0000-0FFFFF	64-kilobyte system ROM	64-kilobyte system ROM

Table A-2 Memory Map (Virtual/Protected Mode)

Address Range (Hexadecimal)	PC-AT Mode	TI Mode
100000-3FFFFF	3-megabyte memory PWB	3-megabyte memory PWB
400000-EFFFFF	11-megabyte memory expansion RAM	11-megabyte memory expansion RAM
F00000-FDFFFF	Reserved	Reserved
FE0000-FEFFFF	64-kilobyte reserved	64-kilobyte reserved
FF0000-FFFFFF	64-kilobyte system ROM	64-kilobyte system ROM

Table A-3 System I/O Maps

Address (Hex)	PC-AT Mode	TI Mode
0000	DMA channel 0* address	Timer port
0001	DMA channel 0* word count	Printer input port
0002	DMA channel 1* address	Printer data
0003	DMA channel 1* word count	LEDs and printer output
0004	DMA channel 2 address	DMA channel 2 address
0005	DMA channel 2 word count	DMA channel 2 word count
0006	DMA channel 3 address	DMA channel 3 address
0007	DMA channel 3 word count	DMA channel 3 word count
0008	Read status; write command	Read status; write command
0009	Write request register	Write request register
000A	Write single mask register bit	Write single mask register bit

* DMA channels 0 and 1 are not accessible in the TI mode.

Table A-3 System I/O Maps (Continued)

Address (Hex)	PC-AT Mode	TI Mode
000B	Write mode register	Write mode register
000C	Clear byte pointer flip-flop	Clear byte pointer flip-flop
000D	Read temporary register; write master clear	Read temporary register; write master clear
000E	Clear mask register	Clear mask register
000F	Write all mask register bits	Write all mask register bits
0010	Not usable	Not usable
0011	Not usable	Not usable
0012	PC-AT or TI mode port	PC-AT or TI mode port
0013	LED port	Not usable
0014	Not usable	8253 counter 0
0015	Not usable	8253 counter 1
0016	Not usable	8253 counter 2
0017	Not usable	8253 control
0018	Not usable	8259 interrupt 1 (duplicate)
0019	Not usable	8259 interrupt 1 (duplicate)
001A | 001F	Not usable	Not usable
0020	8259 interrupt 1	8259 interrupt 1 (duplicate)
0021	8259 interrupt 1	8259 interrupt 1 (duplicate)
0022 | 003F	Not usable	Not usable

Table A-3 System I/O Maps (Continued)

Address (Hex)	PC-AT Mode	TI Mode
0040	8254 timer counter 0	8254 timer counter 0
0041	8254 timer counter 1	8254 timer counter 1
0042	8254 timer counter 2	8254 timer counter 2
0043	8254 timer control register	8254 timer control register
0044 | 005F	Not usable	Not usable
0060	Keyboard data	Keyboard data
0061	Port B	Port B
0062	Not usable	Not usable
0063	Not usable	Not usable
0064	Keyboard status/command port	Keyboard status/command port
0065 | 0067	Not usable	Not usable
0068	Memory control port	Memory control port
0069 | 006F	Not usable	Not usable
0070	RTC address port/enable NMI	RTC address port/enable NMI
0071	RTC data port	RTC data port
0072 | 007F	Not usable	Not usable
0080	Diagnostic-checkpoint port	Diagnostic-checkpoint port

Table A-3 System I/O Maps (Continued)

Address (Hex)	PC-AT Mode	TI Mode
0081	DMA channel 2--diskette (page address)	DMA channel 2--diskette (page address)
0082	DMA channel 3	DMA channel 3
0083	DMA channel 1	DMA channel 1
0084 | 0086	Not used	Not used
0087	DMA channel 0	DMA channel 0
0088	Not used	Not used
0089	DMA channel 6	DMA channel 6
008A	DMA channel 7	DMA channel 7
008B	DMA channel 5	DMA channel 5
008C | 008E	Not used	Not used
008F	Refresh	Refresh
0090 | 009F	Not usable	Not usable
00A0	8259 interrupt 2	8259 interrupt 2
00A1	8259 interrupt 2 mask register	8259 interrupt 2 mask register
00A2 | 00BF	Not usable	Not usable
00C0	Channel 0 base and current address	Channel 0 base and current address
00C2	Channel 0 base and current word count	Channel 0 base and current word count

Table A-3 System I/O Maps (Continued)

Address (Hex)	PC-AT Mode	TI Mode
00C4	Channel 1 base and current address	Channel 1 base and current address
00C6	Channel 1 base and current word count	Channel 1 base and current word count
00C8	Channel 2 base and current address	Channel 2 base and current address
00CA	Channel 2 base and current word count	Channel 2 base and current word count
00CC	Channel 3 base and current address	Channel 3 base and current address
00CE	Channel 3 base and current word count	Channel 3 base and current word count
00D0	Read status; write command register	Read status; write command register
00D2	Write request register	Write request register
00D4	Write single mask register bit	Write single mask register bit
00D6	Write mode register	Write mode register
00D8	Clear byte pointer flip-flop	Clear byte pointer flip-flop
00DA	Read temporary register; write master clear	Read temporary register; write master clear
00DC	Clear mask register	Clear mask register
00DE	Write all mask register bits	Write all mask register bits
00E0 | 00E7	Comm port 1 (TI)	Comm port 1 (TI)

Table A-3 System I/O Maps (Continued)

Address (Hex)	PC-AT Mode	TI Mode
00E8 | 00EF	Comm port 2 (TI)	Comm port 2 (TI)
00F0	Coprocessor busy latch clear	Coprocessor busy latch clear
00F1	Reset coprocessor	Reset coprocessor
00F2 | 00F7	Not usable	Not usable
00F8 | 00FF	Coprocessor	Coprocessor
0100 | 011F	Not used	Not used
0120 | 016F	Reserved	Reserved
0170	Fixed disk data register (alternative)	Fixed disk data register (alternative)
0171	Fixed disk error/write precompensation register	Fixed disk error/write precompensation register
0172	Fixed disk sector count	Fixed disk sector count
0173	Fixed disk sector number	Fixed disk sector number
0174	Fixed disk cylinder low	Fixed disk cylinder low
0175	Fixed disk cylinder high	Fixed disk cylinder high
0176	Fixed disk drive/head	Fixed disk drive/head
0177	Fixed disk status/command register	Fixed disk status/command register

Table A-3 System I/O Maps (Continued)

Address (Hex)	PC-AT Mode	TI Mode
0178 - 01EF	Not used	Not used
01F0	Fixed disk data register	Fixed disk data register
01F1	Fixed disk error/write precompensation register	Fixed disk error/write precompensation register
01F2	Fixed disk sector count	Fixed disk sector count
01F3	Fixed disk sector number	Fixed disk sector number
01F4	Fixed disk cylinder low	Fixed disk cylinder low
01F5	Fixed disk cylinder high	Fixed disk cylinder high
01F6	Fixed disk drive/head	Fixed disk drive/head
01F7	Fixed disk status/command register	Fixed disk status/command register
01F8 - 01FF	Not used	Not used
0200 - 0207	Game I/O	Game I/O
0208 - 021F	Not used	Not used
0220 - 0227	Tape drive	Tape drive
0228 - 0277	Not used	Not used
0278 - 027F	Printer port 2 (PC-AT)	Printer port 2 (PC-AT)

Table A-3 System I/O Maps (Continued)

Address (Hex)	PC-AT Mode	TI Mode
0280–02F7	Not used	Not used
02F8–02FF	Serial port 2 (PC-AT)	Serial port 2 (PC-AT)
0300–031F	Prototype board	Prototype board
0320–036F	Not used	Not used
0370–0377	Alt floppy controller	Alt floppy controller
0378–037F	Printer port 1 (PC-AT)	Printer port 1 (PC-AT)
0380–038F	SDLC, bisynchronous 2	SDLC, bisynchronous 2
0390–039F	Not used	Not used
03A0–03AF	Bisynchronous 1	Bisynchronous 1
03B0–03BF	Monochrome display and printer	Monochrome display and printer
03C0–03CF	Reserved	Reserved

Table A-3 System I/O Maps (Continued)

Address (Hex)	PC-AT Mode	TI Mode
03D0 - 03DF	Color/graphics monitor adapter	Color/graphics monitor adapter
03E0 - 03EF	Not used	Not used
03F0 - 03F7	Floppy controller	Floppy controller
03F8 - 03FF	Serial port 1	Serial port 1
0400 - 7FFF	Duplicate	Duplicate
8000 - 87FF	Nonvolatile RAM	Nonvolatile RAM
8800 - FFFF	Duplicate	Duplicate

Table A-4 DMA Channel Uses

Channel	Use
0	Spare
1	SDLC
2	Floppy disk
3	Tape drive
4	Cascade for controller 1
5	Spare
6	Spare
7	Spare

Table A-5 Tape Drive Interrupt and DMA Levels

Device	Default Interrupt Level	Default DMA Channel	Alternate Interrupt Levels	Alternate DMA Levels
Tape Drive	3	3	2,4,5,6,7	1,2

NOTES:

Refer to Table A-4 for DMA channel use.

Refer to Table 2-8 for interrupt map.

Table A-6 Configurable Interrupt Levels

Device	Default Interrupt Levels PC-AT Mode	TI Mode
TI Mode, RS-232, Serial Port:		
Configured for Comm 1	10	00
Configured for Comm 2	11	01
Main Logic Board, Parallel Port:		
Configured for Port 1	07	07 and 05
Configured for Port 2	05	04 and 05
Main Logic Board, Serial Port:		
Configured for Port 1	04	05
Configured for Port 2	03	03

NOTE:

Refer to Table 2-8 for interrupt map.

Appendix B

TI Mode I/O Maps

The tables in this appendix provide detailed I/O maps for the BUSINESS-PRO computer's TI mode.

Table B-1 Timer, DMA, and LED Control

Address (Hex)	Bit	Power-Up State	Description
0000	0	Low	Speaker timer enable
	1	Low	Timer 1 interrupt enable
	2	Low	Timer 2 interrupt enable
	3–7		Not used
0001	0–3		Not used
	4		Printer port busy (active high)
	5		Printer paper out (active high)
	6		Printer selected (active high)
	7		Printer fault (active low)
0002	0–7		Printer data
0003	0	Low	LED 1 (low=on, high=off)
	1	Low	LED 2 (low=on, high=off)
	2	Low	LED 2 (low=on, high=off)
	3		Not used

Table B-1 Timer, DMA, and LED Control (Continued)

Address (Hex)	Bit	Power-Up State	Description
0003 (Continued)			
	4	Low	Printer auto-feed (active low)
	5	Low	Printer strobe (active low)
	6	Low	Printer initialize (active low)
	7	Low	Printer interrupt enable (active high)
0004			Channel 2 base and current address
0005			Channel 2 base and current word count
0006			Channel 3 base and current address
0007			Channel 3 base and current word count
0008			Read status, write command register
0009			Write request register
000A			Write single mask register bit
000B			Write mode register
000C			Clear byte pointer flip-flop
000D			Read temporary register; write master clear
000E			Clear mask register
000F			Write all mask register bits

Table B-2 Mode Select and Timer

Address (Hex)	Bit	Power-Up State	Description
0010			Not usable.
0011			Not usable.
0012	0	Low	PC-AT/TI mode enable (low=PC-AT mode, high=TI mode).
	1	Low	PC-AT/TI video enable (low=PC-AT mode, high=TI mode).
	2	Low	When high, this bit allows software to force a parity error by reading a memory location in the 640-kilobyte address range that has previously been loaded with 00H, 55H, AAH, or FFH.
	3		Read-only parity error (high byte).
	4		Read-only parity error (low byte). Write-only PC-AT video select bit (LSB).
	5		Read-only RAM bank parity error code bit 0. Write-only PC-AT video select bit 1.
	6		Read-only RAM bank parity error code bit 1. Write-only PC-AT video select bit 2.
	7		Read-only RAM bank parity error code bit 2. Write-only PC-AT video select bit (MSB).
0013			Not usable.
0014			8253 counter 0.
0015			8253 counter 1.
0016			8253 counter 2.
0017			8253 control.

Table B-2 Mode Select and Timer (Continued)

Address (Hex)	Bit	Power-Up State	Description
0018			8259 interrupt (duplicate).
0019			8259 interrupt mask register (duplicate).
001A | 001F			Not usable.

Table B-3 Interrupt Controller 1

Address (Hex)	Description
0020	8259 interrupt (duplicate).
0021	8259 interrupt mask register (duplicate).
0022 | 003F	Not usable.

Table B-4 8254-2 Timer

Address (Hex)	Description
0040	8254 timer counter 0.
0041	8254 timer counter 1.
0042	8254 timer counter 2.
0043	8254 timer control register.
0044 | 005F	Not usable.

Table B-5 8042 Keyboard

Address (Hex)	Bit	Power-Up State	Description
0060			Keyboard data register:
0061	0	Low	Gate 2 input to 8254-2 timer.
	1	Low	Timer 2 output enable (active high).
	2	High	Parity error enable (active low).
	3	High	Expansion bus NMI enable (active low).
	4		Refresh bit.
	5		Timer 2 output.
	6		Expansion bus NMI.
	7		Parity error.
0062			Not usable.
0063			Not usable.
0064			Keyboard control register read-only status port:
	0		Output buffer full. High indicates data is available for reading.
	1		Input buffer full. High indicates data has been written into the buffer but has not yet been read by the controller.
	2	Low	System flag. This bit is defined by the value written into the command byte.
	3		Command/data. High indicates data has been written to address 64H (command). Low indicates data has been written to address 60H (data).

Table B-5 8042 Keyboard (Continued)

Address (Hex)	Bit	Power-Up State	Description
0064 (Continued)			
	4		Inhibit switch. Low indicates all keyboard functions are inhibited.
	5		Transmit time-out. High indicates a transmission started by the keyboard controller was not properly completed.
	6		Receive time-out. High indicates that a transmission started by the keyboard controller was not properly completed.
	7		Parity error. High indicates a parity error.
0064			Write-only command port. System software can use this port to reset the MPU. Refer to Section 2 of this manual for command definitions.
0065 | 0067			Not usable.
0068	0	Low	Low enables a one-wait-state memory cycle. High enables a zero-wait-state memory cycle.
	1	Low	Low enables single refreshes. High enables burst refreshes.
	2	Low	Nonvolatile RAM enable (high disables 2 kilobytes of the nonvolatile RAM).
	3	Low	Low enables expansion memory.
	4	Low	Bank select 0.

Table B-5 8042 Keyboard (Continued)

Address (Hex)	Bit	Power-Up State	Description
	5	Low	Bank select 1.
	6	Low	Bank select 2.
	7	Low	High allows incoming data from the parallel printer port of the main logic board.

Table B-6 Real-Time Clock and NMI Mask

Address (Hex)	Bit	Power-Up State	Description
0070	0–5		Nonvolatile RAM address port
	6		Not usable
	7	High	NMI enabled (active low)
0071			Nonvolatile RAM data port
0072–007F			Not usable

Table B-7 DMA Page Register

Address	Description
0080	Diagnostic-checkpoint port. This port is a read/write port in the LS612 page register.
0081	DMA channel 2 (floppy drive).
0082	DMA channel 3 (tape drive).
0083	DMA channel 1 (SDLC).
0084 | 0086	Not used.
0087	DMA channel 0.
0088	Not used.
0089	DMA channel 6.
008A	DMA channel 7.
008B	DMA channel 5.
008C | 008E	Not used.
008F	Refresh.
0090 | 009F	Not usable.

Table B-8 Slave Interrupt Controller

Address (Hex)	Description
00A0	8259 interrupt
00A1	8259 interrupt mask register
00A2 | 00BF	Not usable

Table B-9 DMA Controller 2

Address (Hex)	Description
00C0	Channel 0 base and current address
00C2	Channel 0 base and current word count
00C4	Channel 1 base and current address
00C6	Channel 1 base and current word count
00C8	Channel 2 base and current address
00CA	Channel 2 base and current word count
00CC	Channel 3 base and current address
00CE	Channel 3 base and current word count
00D0	Read status; write command register
00D2	Write request register
00D4	Write single mask register bit
00D6	Write mode register
00D8	Clear byte pointer flip-flop
00DA	Read temporary register; write master clear
00DC	Clear mask register
00DE	Write all mask register bits

Table B-10 Communication Ports

Address (Hex)	Description
00E0 | 00E3	Communication port 1 interrupt acknowledge
00E4	Communication port 1 channel B command
00E5	Communication port 1 channel B data
00E6	Communication port 1 channel A command
00E7	Communication port 1 channel A data
00E8 | 00EB	Communication port 2 interrupt acknowledge
00EC	Communication port 2 channel B command
00ED	Communication port 2 channel B data
00EE	Communication port 2 channel A command
00EF	Communication port 2 channel A data

Table B-11 Coprocessor

Address (Hex)	Bit	Description
00F0	0-7	Clear-coprocessor busy. Writing 0s to this port clears the latched busy signal.(Activation of the coprocessor error signal during a coprocessor busy condition latches the busy signal.)
00F1	0-7	Coprocessor reset. Writing 0s to this port resets the coprocessor.
00F2-00F7		Not usable.
00F8-00FF		Reserved.

NOTE

Addresses 0100H through 011FH are not used.
Addresses 0120H through 016FH are reserved.

Table B-12 Alternate Fixed Disk

Address (Hex)	Bit	Description
0170		Data register
0171		Error register for read accesses; write precompensation for write accesses
	0	Data address mark not found
	1	Track 000 error
	2	Aborted command
	3	Not used
	4	ID not found
	5	Not used
	6	Data ECC error
	7	Bad block detected
0172		Sector count
0173		Sector number
0174		Cylinder low
0175		Cylinder high
0176		Size/drive/head
	0	Head select 0
	1	Head select 1
	2	Head select 2
	3	Head select 3
	4	Drive 1=0; Drive 2=1
	5	Sector size (low bit)

Table B-12 Alternate Fixed Disk (Continued)

Address (Hex)	Bit	Description
0176 (Continued)		
	6	Sector size (high bit)
	7	High=ECC to be enabled
0177		Status register for read accesses; command register for write accesses
	0	Error
	1	Index pulse from selected drive
	2	Corrected data
	3	Data request
	4	Seek complete from the drive
	5	Write fault from the drive
	6	Drive ready from the drive
	7	Controller busy

NOTE

Addresses 0178H through 01EFH are not used.

Table B-13 Fixed Disk

Address (Hex)	Bit	Description
01F0		Data register
01F1		Error register for read accesses; write precompensation for write accesses
	0	Data address mark not found
	1	Track 000 error
	2	Aborted command
	3	Not used
	4	ID not found
	5	Not used
	6	Data ECC error
	7	Bad block detected
01F2		Sector count
01F3		Sector number
01F4		Cylinder low
01F5		Cylinder high
01F6		Size/drive/head
	0	Head select 0
	1	Head select 1
	2	Head select 2
	3	Head select 3
	4	Drive 1=0; Drive 2=1
	5	Sector size (low bit)

Table B-13 Fixed Disk (Continued)

Address (Hex)	Bit	Description
01F6 (Continued)		
	6	Sector size (high bit)
	7	High=ECC to be enabled
01F7		Status register for read accesses; command register for write accesses
	0	Error
	1	Index pulse from selected drive
	2	Corrected data
	3	Data request
	4	Seek complete from the drive
	5	Write fault from the drive
	6	Drive ready from the drive
	7	Controller busy

NOTE

Addresses 01F8H through 01FFH are not used. Addresses 0200H through 0207H are reserved for game I/O. Addresses 0208H through 0277H are not used.

Table B-14 Parallel Printer Port 2--Option Board

Address (Hex)	Bit	Description
0278		Data latch.
0279		Printer status:
	0 through 2	Not used.
	3	Low indicates an error condition.
	4	Printer selected (active high).
	5	End of paper (active high).
	6	Printer acknowledge (active high).
	7	Printer busy (active low).
027A		Printer controls:
	0	Strobe (active high).
	1	Line feed.
	2	Initialize printer (active low).
	3	Printer select (active high).
	4	Interrupt enable (active high).
	5 through 7	Not used.
027B		Not usable.
027C		Data latch (duplicate).
027D		Printer status (duplicate):
	0 through 2	Not used.

Table B-14 Parallel Printer Port 2--Option Board (Continued)

Address (Hex)	Bit	Description
027D (Continued)		
	3	Low indicates an error condition.
	4	Printer selected (active high).
	5	End of paper (active high).
	6	Printer acknowledge (active low).
	7	Printer busy (active low).
027E		Printer controls (duplicate):
	0	Strobe (active high).
	1	Line feed.
	2	Initialize printer (active low).
	3	Printer select (active high).
	4	Interrupt enable (active high).
	5 | 7	Not used.
027F		Not usable.

NOTE

Addresses 0280H through 02F7H are not used.

Table B-15 Serial Port 2

Address (Hex)	Bit	Description
02F8		Transmit or receive buffer, or least-significant byte of the divisor latch.
02F9		Most-significant byte of the divisor latch or interrupt enable register. The following bit definitions apply to the interrupt enable register:
	0	Enable data-available interrupt.
	1	Enable transmit holding-register empty interrupt.
	2	Enable receive line status interrupt.
	3	Enable modem status interrupt.
	4–7	Always set to logical 0.
02FA		Interrupt identification register:
	0	Interrupt is pending indicator.
	1 2	These bits identify the highest-priority pending interrupt.
	3–7	Always set to logical 0.
02FB		Line control register:
	0	Word-length-select bit 0.
	1	Word-length-select bit 1.
	2	Number of stop bits.
	3	Parity enable.

Table B-15 Serial Port 2 (Continued)

Address (Hex)	Bit	Description
02FB (Continued)		
	4	Even parity select.
	5	Stuck parity.
	6	Set break.
	7	Divisor-latch-access bit.
02FC		Modem control register:
	0	Data terminal ready.
	1	Request-to-send.
	2	Output 1.
	3	Output 2.
	4	Loop.
	5-7	Always set to logical 0.
02FD		Line status register:
	0	Receive data-ready indicator.
	1	Overrun error indicator.
	2	Parity error indicator.
	3	Framing error indicator.
	4	Break interrupt indicator.
	5	Transmitter holding register empty.
	6	Transmitter shift register empty.
	7	Always set to logical 0.

Table B-15 Serial Port 2 (Continued)

Address (Hex)	Bit	Description
02FE		Modem status register:
	0	Delta clear-to-send.
	1	Delta data-set ready.
	2	Trailing-edge ring indicator.
	3	Delta receive line signal detect.
	4	Clear-to-send.
	5	Data-set ready.
	6	Ring indicator.
	7	Receive line signal detect.
02FF		Reserved.

NOTE

Addresses 0300H through 031FH are reserved for the prototype board. Addresses 0320H through 035FH are not used. Addresses 0360H through 036FH are reserved.

Table B-16 Alternate Floppy Disk Controller

Address (Hex)	Bit	Description
0370		Not usable
0371		Not usable
0372		Digital output register:
	0	Drive select (low bit)
	1	Drive select (high bit)
	2	Function reset
	3	Enable interrupts and DMA
	4	Enable drive A motor
	5	Enable drive B motor
	6	Enable drive C motor
	7	Enable drive D motor
0373		Not usable
0374		Status register:
	0	Drive A busy/seeking
	1	Drive B busy/seeking
	2	Drive C busy/seeking
	3	Drive D busy/seeking
	4	Diskette-busy command in progress
	5	NonDMA mode
	6	Data transfer direction (high=floppy disk to host)
	7	Master-data-register ready request

Table B-16 Alternate Floppy Disk Controller (Continued)

Address (Hex)	Bit	Description
0375		Floppy disk data register
0376		Fixed disk register:
	0	Reserved
	1	Enables interrupt
	2	Hard disk reset
	3	Head select 3
0377		Diagnostic register:
	0	Drive select 0 status
	1	Drive select 1 status
	2	Head select 0 status
	3	Head select 1 status
	4	Head select 2 status
	5	Head select 3 or reduced write current status
	6	Write gate status
	7	Disk change
0377		Floppy disk register:
	0	Mode select (low bit)
	1	Mode select (high bit)
	2–7	Not used

Table B-17 Parallel Printer Port 1 -- Option Board

Address (Hex)	Bit	Description
0378		Data latch.
0379		Printer status:
	0–2	Not used.
	3	Low indicates an error condition.
	4	Printer selected (active high).
	5	End of paper (active high).
	6	Printer acknowledge (active low).
	7	Printer busy (active low).
037A		Printer controls:
	0	Strobe (active high).
	1	Line feed.
	2	Initialize printer (active low).
	3	Printer select (active high).
	4	Interrupt enable (active high).
	5–7	Not used.
037B		Not usable.
037C		Data latch (duplicate).
037D		Printer status (duplicate):
	0–2	Not used.

Table B-17 Parallel Printer Port 1 -- Option Board (Continued)

Address (Hex)	Bit	Description
037D (Continued)		
	3	Low indicates an error condition.
	4	Printer selected (active high).
	5	End of paper (active high).
	6	Printer acknowledge (active low).
	7	Printer busy (active low).
037E		Printer controls (duplicate):
	0	Strobe (active high).
	1	Line feed.
	2	Initialize printer (active low).
	3	Printer select (active high).
	4	Interrupt enable (active high).
	5 | 7	Not used. | |
037F		Not usable.

Table B-18 Bisynchronous 2

Address (Hex)	Bit	Description
0380		8255A-5 port A:
	0	Low indicates an interface ring indicator <u>on</u> condition.
	1	Low indicates an interface data carrier detect <u>on</u> condition.
	2	An oscillating condition indicates that the transmit clock is active.
	3	Low indicates an interface clear-to-send <u>on</u> condition.
	4	An oscillating condition indicates that the receive clock is active.
	5	High indicates a modem status change.
	6	High indicates an active timer 2 output.
	7	High indicates an active timer 1 output.
0381		8255A-5 port B:
	0	Low enables the modem interface data signal rate select.
	1	Low enables the modem interface select standby.
	2	Low enables the test function.
	3	High resets the modem status changed logic.
	4	High resets the 8273.
	5	High enables gate timer 2.
	6	High enables gate timer 1.
	7	Low enables level 4 interrupt.

Table B-18 Bisynchronous 2 (Continued)

Address (Hex)	Bit	Description
0382		8255A-5 port C:
	0	High enables gating of the internal clock (output).
	1	High enables gating of the external clock (output).
	2	High enables the electronic wrap (output).
	3	Low enables gating of interrupts 3 and 4 (output).
	4	An oscillating condition indicates receive data (input).
	5	An oscillating condition indicates timer 0 output (input).
	6	Low indicates test active (input).
	7	Not used.
0383		8255 mode set register.
0384		8253 counter 0.
0385		8253 counter 1.
0386		8253 counter 2.
0387		8253 control word (mode register).
0388		8273 read-only status register:
	0	High indicates that the transmit interrupt result is available.
	1	High indicates that the receive interrupt result is available.
	2	High enables the transmit interrupt.

Table B-18 Bisynchronous 2 (Continued)

Address (Hex)	Bit	Description
0388 (Continued)		
	3	High enables the receive interrupt.
	4	High indicates that the command result buffer is full.
	5	High indicates that the command parameter buffer is full.
	6	High indicates that the command buffer is full.
	7	High indicates a command busy condition.
0388		8273 write-only command register.
0389		8273 parameter/result.
038A		8273 transmit interrupt status.
038B		8273 receive interrupt status.
038C		8273 data.
038D through 038F		Not used.

NOTE

Addresses 0390H through 039FH are not used.

Table B-19 Bisynchronous 1

Address (Hex)	Bit	Description
03A0		8255A-5 port A for bisynchronous control:
	0	Low indicates an interface ring indicator on condition.
	1	Low indicates an interface data carrier detect on condition.
	2	An oscillating condition indicates the transmit clock is active.
	3	Low indicates an interface clear-to-send on condition.
	4	An oscillating condition indicates that the receive clock is active.
	5	High indicates an active transmit ready.
	6	High indicates an active timer 2 output.
	7	High indicates an active timer 1 output.
03A1		8255A-5 port B for bisynchronous control:
	0	Low enables the modem interface data signal rate selector.
	1	Low enables the modem interface select standby.
	2	Low enables the test function.
	3	Not used.
	4	High resets the 8251A.
	5	High enables gate timer 2.

Table B-19 Bisynchronous 1 (Continued)

Address (Hex)	Bit	Description
03A1 (Continued)		
	6	High enables gate timer 1.
	7	High gates timers 1 and 2 to level 4 interrupt.
03A2		8255A-5 port C for bisynchronous control:
	0	High enables gating of the internal clock (output).
	1	High enables gating of the external clock (output).
	2	High enables the electronic wrap (output).
	3	Low enables timers 1 and 2, interrupt 6, and receive interrupt 3.
	4	An oscillating condition indicates receive data (input).
	5	An oscillating condition indicates timer 0 output (input).
	6	Low indicates test active (input).
	7	Low enables bisynchronous control.
03A3		8255 mode set register.
03A4		Counter 0.
03A5		Counter 1.
03A6		Counter 2.

Table B-19 Bisynchronous 1 (Continued)

Address (Hex)	Bit	Description
03A7		8253-5 control word (mode register):
	0	Binary or BCD (binary coded decimal) counting
	1 | 3	Mode.
	4	Read/load.
	5	Read/load.
	6	Select counter.
	7	Select counter.
03A8		Data select.
03A9		Mode instruction format for BSC:
	0	Not used (always 0).
	1	Not used (always 0).
	2	Character length bit.
	3	Character length bit.
	4	High enables parity.
	5	High=even parity.
	6	High indicates that SYNDET is an input.
	7	Low=double synchronization character.
03A9		Command/instruction format for bisynchronous control:
	0	Transmit enable.
	1	Data terminal ready.

Table B-19 Bisynchronous 1 (Continued)

Address (Hex)	Bit	Description
03A9 (Continued)		
	2	Receive enable.
	3	Send break character.
	4	Error reset.
	5	Request-to-send.
	6	Internal reset.
	7	Enter hunt mode.
03AA | 03AF		Not usable.

Table B-20 Monochrome Display and Printer

Address (Hex)	Bit	Description
03B0 | 03B3		Not used
03B4		6845 index register
03B5		6845 data register
03B6		Not used
03B7		Not used
03B8		CRT control port 1:
	0	High resolution mode (active high)
	1	Not used
	2	Not used

Table B-20 Monochrome Display and Printer (Continued)

Address (Hex)	Bit	Description
03B8 (Continued)		
	3	Video enable (active high)
	4	Not used
	5	Enable blink (active high)
	6	Not used
	7	Not used
03B9		Reserved
03BA		CRT status port:
	0	Horizontal (active high)
	1	Green dot data
	2	Blue dot data
	3	Black/white video (red dot data)
	4 | 7	Not used |
03BB		Reserved
03BC		Parallel data port
03BD		Printer status port
03BE		Printer control port
03BF		Not used

NOTE

Addresses 03C0H through 03CFH are reserved.

Table B-21 Color/Graphics Monitor Adapter

Address (Hex)	Bit	Description
03D0		6845 registers.
03D1		6845 registers.
03D2		Not usable.
03D3		Not usable.
03D4		6845 index register.
03D5		6845 data register.
03D6		Not usable.
03D7		Not usable.
03D8		Mode select register:
	0	80x25 alphanumeric mode.
	1	Graphics select.
	2	Black/white select.
	3	Enable video signal.
	4	High-resolution (640x200) black/white mode.
	5	Changed background intensity to blink bit.
	6	Not used.
	7	Not used.
03D9		Color select register:
	0 | 3	These bits select the screen border color in the 40x25 alphanumeric mode and the screen background color (C0 and C1) in the medium-resolution (320x200) color/ graphics mode.

Table B-21 Color/Graphics Monitor Adapter (Continued)

Address (Hex)	Bit	Description
03D9 (Continued)		
	4	When high, this bit selects an alternate,intensified color set. For the alphanumeric mode, this bit selects the background colors.
	5	This bit is used only in the medium-resolution color/ graphics mode to select the active screen color set.
	6	Not usable.
	7	Not usable.
03DA		Status register:
	0	Display enable.
	1	Light-pen trigger set.
	2	Light-pen switch made.
	3	Vertical synchronization.
	4 | 7	Not used.
03DB		Clear light pen latch.
03DC		Preset light pen latch.
03DD | 03DF		Not usable.

NOTE

Addresses 03E0H through 03EFH are not used.

Table B-22 Floppy Disk Controller

Address (Hex)	Bit	Description
03F0		Not usable
03F1		Not usable
03F2		Digital ouput register:
	0	Drive select (low bit)
	1	Drive select (high bit)
	2	Function reset
	3	Enable interrupts and DMA
	4	Enable drive A motor
	5	Enable drive B motor
	6	Enable drive C motor
	7	Enable drive D motor
03F3		Not usable
03F4		Status register:
	0	Drive A busy/seeking
	1	Drive B busy/seeking
	2	Drive C busy/seeking
	3	Drive D busy/seeking
	4	Disk busy command in progress
	5	NonDMA mode
	6	Data transfer direction (high=floppy disk to host)
	7	Master-data-register ready request

Table B-22 Floppy Disk Controller (Continued)

Address (Hex)	Bit	Description
03F5		Floppy disk data
03F6		Fixed disk register:
	0	Reserved
	1	Enables interrupt
	2	Hard disk reset
	3	Head select 3
03F7		Diagnostic register:
	0	Drive select 0 status
	1	Drive select 1 status
	2	Head select 0 status
	3	Head select 1 status
	4	Head select 2 status
	5	Head select 3 or reduced write current status
	6	Write gate
	7	Disk change
03F7		Floppy disk register:
	0	Mode select (low bit)
	1	Mode select (high bit)
	2–7	Not used

Table B-23 Serial Port 1

Address (Hex)	Bit	Description
03F8		Transmit or receive buffer, or least-significant byte of the divisor latch.
03F9		Most-significant byte of the divisor latch or interrupt enable register. The following bit definitions apply to the interrupt enable register:
	0	Enable data-available interrupt.
	1	Enable transmit holding-register empty interrupt.
	2	Enable receive line status interrupt.
	3	Enable modem status interrupt.
	4–7	Always set to logical 0.
03FA		Interrupt identification register:
	0	Interrupt is pending indicator.
	1, 2	These bits identify the highest-priority pending interrupt.
	3–7	Always set to logical 0.
03FB		Line control register:
	0	Word-length-select bit 0.
	1	Word-length-select bit 1.
	2	Number of stop bits.
	3	Parity enable.

Table B-23 Serial Port 1 (Continued)

Address (Hex)	Bit	Description
03FB (Continued)		
	4	Even parity select.
	5	Stuck parity.
	6	Set break.
	7	Divisor-latch-access bit.
03FC		Modem control register:
	0	Data terminal ready.
	1	Request-to-send.
	2	Output 1.
	3	Output 2.
	4	Loop.
	5–7	Always set to logical 0.
03FD		Line status register.
	0	Receive data-ready indicator.
	1	Overrun error indicator.
	2	Parity error indicator.
	3	Framing error indicator.
	4	Break interrupt indicator.
	5	Transmitter holding register empty.
	6	Transmitter shift register empty.
	7	Always set to logical 0.

Table B-23 Serial Port 1 (Continued)

Address (Hex)	Bit	Description
03FE		Modem status register:
	0	Delta clear-to-send.
	1	Delta data-set ready.
	2	Trailing-edge ring indicator.
	3	Delta receive line signal detect.
	4	Clear-to-send.
	5	Data-set ready.
	6	Ring indicator.
	7	Receive line signal detect.
03FF		Reserved.
0400 | 7FFF		Duplicate.
8000 | 87FF		Nonvolatile RAM.
88FF | FFFF		Duplicate.

Appendix C

PC-AT Mode I/O Maps

The tables in this appendix provide detailed I/O maps for the BUSINESS-PRO computer's IBM Personal Computer AT (PC-AT) compatible mode.

Table C-1 DMA Controller 1

Address (Hex)	Description
0000	Channel 0 base and current address
0001	Channel 0 base and current word count
0002	Channel 1 base and current address
0003	Channel 1 base and current word count
0004	Channel 2 base and current address
0005	Channel 2 base and current word count
0006	Channel 3 base and current address
0007	Channel 3 base and current word count
0008	Read status, write command register
0009	Write request register
000A	Write single mask register bit
000B	Write mode register
000C	Clear byte pointer flip-flop
000D	Read temporary register; write master clear
000E	Clear mask register
000F	Write all mask register bits

Table C-2 Mode Select and Timer

Address (Hex)	Bit	Power-Up State	Description
0010 | 0011			Not usable.
0012	0	Low	Low=PC-AT mode, high=TI mode.
	1	Low	High=TI compatible video. Low=PC-AT compatible video.
	2	Low	When high, this bit allows software to force a parity error by reading a memory location in the 640-kilobyte address range that has previously been loaded with 00H, 55H, AAH, or FFH.
	3		Read-only high byte parity error.
	4		Read-only low byte parity error. Write-only PC-AT video select bit (LSB).
	5		Read-only RAM bank parity error code bit 0. Write-only PC-AT video select bit 1.
	6		Read-only RAM bank parity error code bit 1. Write-only PC-AT video select bit 2.
	7		Read-only RAM bank parity error code bit 2. Write-only PC-AT video select bit (MSB).
0013	0	Low	LED 1 (low=on, high=off).
	1	Low	LED 2 (low=on, high=off).
	2	Low	LED 3 (low=on, high=off).
	3 | 7		Not used.
0014 | 001F			Not usable.

Table C-3 Master Interrupt Controller

Address (Hex)	Description
0020	8259 interrupt
0021	8259 interrupt mask register
0022 | 003F	Not usable

Table C-4 8254-2 Timer

Address (Hex)	Description
0040	8254 timer counter 0
0041	8254 timer counter 1
0042	8254 timer counter 2
0043	8254 timer control register
0044 | 005F	Not usable

Table C-5 8042 Keyboard

Address (Hex)	Bit	Power-Up State	Description
0060	0–7		Keyboard data register.
0061	0	Low	Gate 2 input to 8254-2 timer.
	1	Low	Timer 2 output enable (active high).
	2	High	Parity error enable (active low).
	3	High	Expansion bus NMI enable (active low).
	4		Refresh bit.
	5		Timer 2 output.
	6		Expansion bus NMI.
	7		Parity error.
0062			Not usable.
0063			Not usable.
0064			Keyboard control register read-only status port:
	0		Output buffer full. High indicates data is available for reading.
	1		Input buffer full. High indicates data has been written into the buffer but has not yet been read by the controller.
	2	Low	System flag. This bit is defined by the value written into the command byte.
	3		Command/data. High indicates data has been written to address 64H (command). Low indicates data has been written to address 60H (data).
	4		Inhibit switch. Low indicates all keyboard functions are inhibited.

Table C-5 8042 Keyboard (Continued)

Address (Hex)	Bit	Power-Up State	Description
0064 (Continued)			
	5		Transmit time-out. High indicates that a transmission started by the keyboard controller was not properly completed.
	6		Receive time-out. High indicates that a transmission started by the keyboard controller was not properly completed.
	7		Parity error. High indicates a parity error.
0064			Write-only command port. System software can use this port to reset the MPU. Refer to Section 2 of this manual for command definitions.
0065 | 0067			Not usable.
0068	0	Low	Low enables a one-wait-state memory cycle. High enables a zero-wait-state memory cycle.
	1	Low	Low enables single refreshes. High enables burst refreshes.
	2	Low	Nonvolatile RAM enable (high disables 2 kilobytes of the nonvolatile RAM).
	3	Low	Low enables expansion bus memory.
	4	Low	Bank select 0.
	5	Low	Bank select 1.
	6	Low	Bank select 2.
	7	Low	High allows incoming data from the main logic board parallel port.
0069 | 006F			Not usable.

Table C-6 Real-Time Clock and NMI Mask

Address (Hex)	Bit	Power-Up State	Description
0070	0–5		Nonvolatile RAM address port
	6		Not usable
	7	High	NMI enabled (active low)
0071			Nonvolatile RAM data port
0072–007F			Not usable

Table C-7 DMA Page Register

Address (Hex)	Description
0080	Diagnostic-checkpoint port. This port is a read/write port in the LS612 page register.
0081	DMA channel 2 (floppy drive).
0082	DMA channel 3 (tape drive).
0083	DMA channel 1 (SDLC).
0084 | 0086	Not used.
0087	DMA channel 0.
0088	Not used.
0089	DMA channel 6.
008A	DMA channel 7.
008B	DMA channel 5.
008C | 008E	Not used.
008F	Refresh.
0090 | 009F	Not usable.

Table C-8 Slave Interrupt Controller

Address (Hex)	Description
00A0	8259 interrupt
00A1	8259 interrupt mask register
00A2 | 00BF	Not usable

Table C-9 DMA Controller 2

Address (Hex)	Description
00C0	Channel 0 base and current address
00C2	Channel 0 base and current word count
00C4	Channel 1 base and current address
00C6	Channel 1 base and current word count
00C8	Channel 2 base and current address
00CA	Channel 2 base and current word count
00CC	Channel 3 base and current address
00CE	Channel 3 base and current word count
00D0	Read status; write command register
00D2	Write request register
00D4	Write single mask register bit
00D6	Write mode register
00D8	Clear byte pointer flip-flop
00DA	Read temporary register; write master clear
00DC	Clear mask register
00DE	Write all mask register bits

Table C-10 Communication Ports

Address (Hex)	Description
00E0 | 00E3	Communication port 1 interrupt acknowledge
00E4	Communication port 1 channel B command
00E5	Communication port 1 channel B data
00E6	Communication port 1 channel A command
00E7	Communication port 1 channel A data
00E8 | 00EB	Communication port 2 interrupt acknowledge
00EC	Communication port 2 channel B command
00ED	Communication port 2 channel B data
00EE	Communication port 2 channel A command
00EF	Communication port 2 channel A data

Table C-11 Coprocessor

Address (Hex)	Bit	Description
00F0	0–7	Clear-coprocessor busy. Writing 0s to this port clears the latched busy signal. (Activation of the coprocessor error signal during a coprocessor busy condition latches the busy signal.)
00F1	0–7	Coprocessor reset. Writing 0s to this port resets the coprocessor.
00F2–00F7		Not usable.
00F8–00FF		Reserved.

NOTE

Addresses 0100H through 011FH are not used.
Addresses 0120H through 016FH are reserved.

Table C-12 Alternate Fixed Disk

Address (Hex)	Bit	Description
0170		Data register
0171		Error register for read accesses; write precompensation for write accesses
	0	Data address mark not found
	1	Track 000 error
	2	Aborted command
	3	Not used
	4	ID not found
	5	Not used
	6	Data ECC error
	7	Bad block detected
0172		Sector count
0173		Sector number
0174		Cylinder low
0175		Cylinder high
0176		Size/drive/head
	0	Head select 0
	1	Head select 1
	2	Head select 2
	3	Head select 3
	4	Drive 1=0; Drive 2=1
	5	Sector size (low bit)

Table C-12 Alternate Fixed Disk (Continued)

Address (Hex)	Bit	Description
0176 (Continued)		
	6	Sector size (high bit)
	7	High=ECC to be enabled
0177		Status register for read accesses; command register for write accesses
	0	Error
	1	Index pulse from selected drive
	2	Corrected data
	3	Data request
	4	Seek complete from the drive
	5	Write fault from the drive
	6	Drive ready from the drive
	7	Controller busy

NOTE

Addresses 0178H through 01EFH are not used.

Table C-13 Fixed Disk

Address (Hex)	Bit	Description
01F0		Data register
01F1		Error register for read accesses; write precompensation for write accesses.
	0	Data address mark not found
	1	Track 000 error
	2	Aborted command
	3	Not used
	4	ID not found
	5	Not used
	6	Data ECC error
	7	Bad block detected
01F2		Sector count
01F3		Sector number
01F4		Cylinder low
01F5		Cylinder high
01F6		Size/drive/head
	0	Head select 0
	1	Head select 1
	2	Head select 2
	3	Head select 3
	4	Drive 1=0; Drive 2=1
	5	Sector size (low bit)

Table C-13 Fixed Disk (Continued)

Address (Hex)	Bit	Description
01F6 (Continued)		
	6	Sector size (high bit)
	7	High=ECC to be enabled
01F7		Status register for read accesses; command register for write accesses
	0	Error
	1	Index pulse from selected drive
	2	Corrected data
	3	Data request
	4	Seek complete from the drive
	5	Write fault from the drive
	6	Drive ready from the drive
	7	Controller busy

NOTE

Addresses 01F8H through 01FFH are not used. Addresses 0200H through 0207H are reserved for game I/O. Addresses 0208H through 02F7H are not used.

Table C-14 Parallel Printer Port 2

Address (Hex)	Bit	Description
0278		Data latch.
0279		Printer status:
	0–2	Not used.
	3	Low indicates an error condition.
	4	Printer selected (active high).
	5	End of paper (active high).
	6	Printer acknowledge (active low).
	7	Printer busy (active low).
027A		Printer controls:
	0	Strobe (active high).
	1	Line feed.
	2	Initialize printer (active low).
	3	Printer select (active high).
	4	Interrupt enable (active high).
	5*	Low indicates 128 kilobytes of memory on the main logic board are enabled. (Read-only bit on the main logic board parallel port.)
	6*	High indicates all NMIs are being masked out. (Read-only bit on the main logic board parallel port.)

NOTE:

*Bits 5 through 7 are not used on PC-AT compatible parallel port option boards.

Table C-14 Parallel Printer Port 2 (Continued)

Address (Hex)	Bit	Description
027A (Continued)		
	7*	High indicates the serial port on the main logic board is located at addresses 03F8H through 03FFH. (Read-only bit on the main logic board parallel port.)
027B		Not usable.
027C		Data latch (duplicate).
027D		Printer status (duplicate):
	0–2	Not used.
	3	Low indicates an error condition.
	4	Printer selected (active high).
	5	End of paper (active high).
	6	Printer acknowledge (active low).
	7	Printer busy (active low).
027E		Printer controls (duplicate):
	0	Strobe (active high).
	1	Line feed.
	2	Initialize printer (active low).
	3	Printer select (active high).
	4	Interrupt enable (active high).

NOTE:

*Bits 5 through 7 are not used on PC-AT compatible parallel port option boards.

Table C-14 Parallel Printer Port 2 (Continued)

Address (Hex)	Bit	Description
027E (Continued)		
	5*	Low indicates 128 kilobytes of memory on the main logic board are enabled. (Read-only bit on the main logic board parallel port.)
	6*	High indicates all NMIs are being masked out. (Read-only bit on the main logic board parallel port.)
	7*	High indicates the serial port on the main logic board is located at addresses 03F8H through 03FFH. (Read-only bit on the main logic board parallel port.)
027F		Not usable.

NOTE:

*Bits 5 through 7 are not used on PC-AT compatible parallel port option boards.

NOTE

Addresses 0280H through 02F7H are not used.

Table C-15 Serial Port 2

Address (Hex)	Bit	Description
02F8		Transmit or receive buffer, or least-significant byte of the divisor latch.
02F9		Most-significant byte of the divisor latch or interrupt enable register. The following bit definitions apply to the interrupt enable register:
	0	Enable data-available interrupt.
	1	Enable transmit holding-register empty interrupt.
	2	Enable receive line status interrupt.
	3	Enable modem status interrupt.
	4–7	Always set to logical 0.
02FA		Interrupt identification register:
	0	Interrupt is pending indicator.
	1, 2	These bits identify the highest-priority pending interrupt.
	3–7	Always set to logical 0.
02FB		Line control register:
	0	Word-length-select bit 0.
	1	Word-length-select bit 1.
	2	Number of stop bits.
	3	Parity enable.
	4	Even parity select.

Table C-15 Serial Port 2 (Continued)

Address (Hex)	Bit	Description
02FB (Continued)		
	5	Stuck parity.
	6	Set break.
	7	Divisor-latch-access bit.
02FC		Modem control register:
	0	Data terminal ready.
	1	Request-to-send.
	2	Output 1.
	3	Output 2.
	4	Loop.
	5-7	Always set to logical 0.
02FD		Line status register:
	0	Receive data-ready indicator.
	1	Overrun error indicator.
	2	Parity error indicator.
	3	Framing error indicator.
	4	Break interrupt indicator.
	5	Transmitter holding register empty.
	6	Transmitter shift register empty.
	7	Always set to logical 0.

Table C-15 Serial Port 2 (Continued)

Address (Hex)	Bit	Description
02FE		Modem status register:
	0	Delta clear-to-send.
	1	Delta data-set ready.
	2	Trailing-edge ring indicator.
	3	Delta receive line signal detect.
	4	Clear-to-send.
	5	Data-set ready.
	6	Ring indicator.
	7	Receive line signal detect.
02FF		Reserved.

NOTE

Addresses 0300H through 031FH are reserved for the prototype board. Addresses 0320H through 035FH are not used. Addresses 0360H through 036FH are reserved.

Table C-16 Alternate Floppy Disk Controller

Address (Hex)	Bit	Description
0370		Not usable
0371		Not usable
0372		Digital output register:
	0	Drive select (low bit)
	1	Drive select (high bit)
	2	Function reset
	3	Enable interrupts and DMA
	4	Enable drive A motor
	5	Enable drive B motor
	6	Enable drive C motor
	7	Enable drive D motor
0373		Not usable
0374		Status register:
	0	Drive A busy/seeking
	1	Drive B busy/seeking
	2	Drive C busy/seeking
	3	Drive D busy/seeking
	4	Diskette-busy command in progress
	5	NonDMA mode
	6	Data transfer direction (high=floppy disk to host)
	7	Master-data-register ready request

Table C-16 Alternate Floppy Disk Controller (Continued)

Address (Hex)	Bit	Description
0375		Floppy disk data register
0376		Fixed disk register:
	0	Reserved
	1	Enables interrupt
	2	Hard disk reset
	3	Head select 3
0377		Diagnostic register:
	0	Drive select 0 status
	1	Drive select 1 status
	2	Head select 0 status
	3	Head select 1 status
	4	Head select 2 status
	5	Head select 3 or reduced write current status
	6	Write gate status
	7	Disk change
0377		Floppy disk register:
	0	Mode select (low bit)
	1	Mode select (high bit)
	2–7	Not used

Table C-17 Parallel Printer Port 1

Address (Hex)	Bit	Description
0378		Data latch.
0379		Printer status:
	0–2	Not used.
	3	Low indicates an error condition.
	4	Printer selected (active high).
	5	End of paper (active high).
	6	Printer acknowledge (active low).
	7	Printer busy (active low).
037A		Printer controls:
	0	Strobe (active high).
	1	Line feed.
	2	Initialize printer (active low).
	3	Printer select (active high).
	4	Interrupt enable (active high).
	5*	Low indicates 128 kilobytes of memory on the main logic board are enabled. (Read-only bit on the main logic board parallel port.)
	6*	High indicates all NMIs are being masked out. (Read-only bit on the main logic board parallel port.)

NOTE:

*Bits 5 through 7 are not used on PC-AT compatible parallel port option boards.

Table C-17 Parallel Printer Port 1 (Continued)

Address (Hex)	Bit	Description
037A (Continued)		
	7*	High indicates the serial port on the main logic board is located at addresses 03F8H through 03FFH. (Read-only bit on the main logic board parallel port.)
037B		Not usable.
037C		Data latch (duplicate).
037D		Printer status (duplicate):
	0–2	Not used.
	3	Low indicates an error condition.
	4	Printer selected (active high).
	5	End of paper (active high).
	6	Printer acknowledge (active low).
	7	Printer busy (active low).
037E		Printer controls (duplicate):
	0	Strobe (active high).
	1	Line feed.
	2	Initialize printer (active low).
	3	Printer select (active high).
	4	Enable interrupt (active high).

NOTE:

*Bits 5 through 7 are not used on PC-AT compatible parallel port option boards.

Table C-17 Parallel Printer Port 1 (Continued)

Address (Hex)	Bit	Description
037E (Continued)		
	5*	Low indicates 128 kilobytes of memory on the main logic board are enabled. (Read-only bit on the main logic board parallel port.)
	6*	High indicates all NMIs are being masked out. (Read-only bit on the main logic board parallel port.)
	7*	High indicates the serial port on the main logic board is located at addresses 03F8H through 03FFH. (Read-only bit on the main logic board parallel port.)
037F		Not usable.

NOTE:

*Bits 5 through 7 are not used on PC-AT compatible parallel port option boards.

Table C-18 Bisynchronous 2

Address	Bit	Description
0380		8255A-5 port A:
	0	Low indicates an interface ring indicator on condition.
	1	Low indicates an interface data carrier detect on condition.
	2	An oscillating condition indicates transmit clock is active.
	3	Low indicates an interface clear-to-send on condition.
	4	An oscillating condition indicates the receive clock is active.
	5	High indicates a modem status change.
	6	High indicates an active timer 2 output.
	7	High indicates an active timer 1 output.
0381		8255A-5 port B:
	0	Low enables the modem interface data signal rate select.
	1	Low enables the modem interface select standby.
	2	Low enables the test function.
	3	High resets the modem status changed logic.
	4	High resets the 8273.
	5	High enables gate timer 2.
	6	High enables gate timer 1.
	7	Low enables level 4 interrupt.

Table C-18 Bisynchronous 2 (Continued)

Address (Hex)	Bit	Description
0382		8255A-5 port C:
	0	High enables gating of the internal clock (output).
	1	High enables gating of the external clock (output).
	2	High enables the electronic wrap (output).
	3	Low enables gating of interrupts 3 and 4 (output).
	4	An oscillating condition indicates receive data (input).
	5	An oscillating condition indicates timer 0 output (input).
	6	Low indicates test active (input).
	7	Not used.
0383		8255 mode set register.
0384		8253 counter 0.
0385		8253 counter 1.
0386		8253 counter 2.
0387		8253 mode register.
0388		8273 read-only status register:
	0	High indicates that the transmit interrupt result is available.
	1	High indicates that the receive interrupt result is available.
	2	High enables the transmit interrupt.

Table C-18 Bisynchronous 2 (Continued)

Address (Hex)	Bit	Description
0388 (Continued)		
	3	High enables the receive interrupt.
	4	High indicates that the command result buffer is full.
	5	High indicates that the command parameter buffer is full.
	6	High indicates that the command buffer is full.
	7	High indicates a command busy condition.
0388		8273 write-only command register.
0389		8273 parameter/result.
038A		8273 transmit interrupt status.
038B		8273 receive interrupt status.
038C		8273 data.
038D | 038F		Not used.

NOTE

Addresses 0390H through 039FH are not used.

Table C-19 Bisynchronous 1

Address (Hex)	Bit	Description
03A0		8255A-5 port A for bisynchronous control:
	0	Low indicates an interface ring indicator on condition.
	1	Low indicates an interface data carrier detect on condition.
	2	An oscillating condition indicates the transmit clock is active.
	3	Low indicates an interface clear-to-send on condition.
	4	An oscillating condition indicates the receive clock is active.
	5	High indicates an active transmit ready.
	6	High indicates an active timer 2 output.
	7	High indicates an active timer 1 output.
03A1		8255A-5 port B for bisynchronous control:
	0	Low enables the modem interface data signal rate selector.
	1	Low enables the modem interface select standby.
	2	Low enables the test function.
	3	Not used.
	4	High resets the 8251A.
	5	High enables gate timer 2.
	6	High enables gate timer 1.

Table C-19 Bisynchronous 1 (Continued)

Address	Bit	Description
03A1 (Continued)		
	7	High gates timers 1 and 2 to level 4 interrupt.
03A2		8255A-5 port C for bisynchronous control:
	0	High enables gating of internal clock (output).
	1	High enables gating of external clock (output).
	2	High enables the electronic wrap (output).
	3	Low enables timers 1 and 2, interrupt 6, and receive interrupt 3.
	4	An oscillating condition indicates receive data (input).
	5	An oscillating condition indicates timer 0 output (input).
	6	Low indicates test active (input).
	7	Low enables bisynchronous control.
03A3		8255 mode initialization.
03A4		Counter 0.
03A5		Counter 1.
03A6		Counter 2.
03A7		8253-5 control word (mode register):
	0	Binary or BCD (binary coded decimal) counting.
	1–3	Mode.

Table C-19 Bisynchronous 1 (Continued)

Address	Bit	Description
03A7 (Continued)		
	4	Read/load.
	5	Read/load.
	6	Select counter.
	7	Select counter.
03A8		Data select.
03A9		Mode instruction format for BSC:
	0	Not used (always 0).
	1	Not used (always 0).
	2	Character length bit.
	3	Character length bit.
	4	High enables parity.
	5	High=even parity.
	6	High indicates that SYNDET is an input.
	7	Low=double synchronization character.
03A9		Command/instruction format for bisynchronous control:
	0	Transmit enable.
	1	Data terminal ready.
	2	Receive enable.
	3	Send break character.
	4	Error reset.
	5	Request-to-send.
	6	Internal reset.

Table C-19 Bisynchronous 1 (Continued)

Address (Hex)	Bit	Description
03A9 (Continued)		
	7	Enter hunt mode.
03AA | 03AF		Not usable.

Table C-20 Monochrome Display and Printer

Address (Hex)	Bit	Description
03B0 | 03B3		Not used
03B4		6845 index register
03B5		6845 data register
03B6		Not used
03B7		Not used
03B8		CRT control port 1:
	0	High resolution mode (active high)
	1	Not used
	2	Not used
	3	Video enable (active high)
	4	Not used
	5	Enable blink (active high)
	6	Not used

Table C-20 Monochrome Display and Printer (Continued)

Address (Hex)	Bit	Description
03B8 (Continued)		
	7	Not used
03B9		Reserved
03BA		CRT status port:
	0	Horizontal (active high)
	1	Green dot data
	2	Blue dot data
	3	Black/white video (red dot data)
	4–7	Not used
03BB		Reserved
03BC		Parallel data port
03BD		Printer status port
03BE		Printer control port
03BF		Not used

NOTE

Addresses 03C0H through 03CFH are reserved.

Table C-21 Color/Graphics Monitor Adapter

Address (Hex)	Bit	Description
03D0		6845 registers.
03D1		6845 registers.
03D2		Not usable.
03D3		Not usable.
03D4		6845 index register.
03D5		6845 data register.
03D6		Not usable.
03D7		Not usable.
03D8		Mode select register:
	0	80x25 alphanumeric mode.
	1	Graphics select.
	2	Black/white select.
	3	Enable video signal.
	4	High-resolution (640x200) black/white mode.
	5	Changed background intensity to blink bit.
	6	Not used.
	7	Not used.
03D9		Color select register:
	0-3	These bits select the screen border color in the 40x25 alphanumeric mode and the screen background color (C0 and C1) in the medium-resolution (320x200) color/graphics mode.

Table C-21 Color/Graphics Monitor Adapter (Continued)

Address (Hex)	Bit	Description
03D9 (Continued)		
	4	When high, this bit selects an alternate, intensified color set. For the alphanumeric mode, this bit selects the background colors.
	5	This bit is used only in the medium-resolution color/ graphics mode to select the active screen color set.
	6	Not usable.
	7	Not usable.
03DA		Status register:
	0	Display enable.
	1	Light pen trigger set.
	2	Light pen switch made.
	3	Vertical synchronization.
	4 | 7	Not used.
03DB		Clear light pen latch.
03DC		Preset light pen latch.
03DD | 03DF		Not usable.

NOTE

Addresses 03E0H through 03EFH are not used.

Table C-22 Floppy Disk Controller

Address (Hex)	Bit	Description
03F0		Not usable
03F1		Not usable
03F2		Digital ouput register:
	0	Drive select (low bit)
	1	Drive select (high bit)
	2	Function reset
	3	Enable interrupts and DMA
	4	Enable drive A motor
	5	Enable drive B motor
	6	Enable drive C motor
	7	Enable drive D motor
03F3		Not usable
03F4		Status register:
	0	Drive A busy/seeking
	1	Drive B busy/seeking
	2	Drive C busy/seeking
	3	Drive D busy/seeking
	4	Diskette-busy command in progress
	5	NonDMA mode
	6	Data transfer direction (high=floppy disk to host)
	7	Master-data-register ready request

Table C-22 Floppy Disk Controller (Continued)

Address (Hex)	Bit	Description
03F5		Floppy disk data
03F6		Fixed disk register:
	0	Reserved
	1	Enables interrupt
	2	Hard disk reset
	3	Head select 3
03F7		Diagnostic register:
	0	Drive select 0 status
	1	Drive select 1 status
	2	Head select 0 status
	3	Head select 1 status
	4	Head select 2 status
	5	Head select 3 or reduced write current status
	6	Write gate status
	7	Disk change
03F7		Floppy disk register:
	0	Mode select (low bit)
	1	Mode select (high bit)
	2–7	Not used

Table C-23 Serial Port 1

Address (Hex)	Bit	Description
03F8		Transmit or receive buffer or least-significant byte of the divisor latch.
03F9		Most-significant byte of the divisor latch or interrupt enable register. The following bit definitions apply to the interrupt enable register:
	0	Enable data-available interrupt.
	1	Enable transmit holding-register empty interrupt.
	2	Enable receive line status interrupt.
	3	Enable modem status interrupt.
	4 | 7	Always set to logical 0. |
03FA		Interrupt identification register:
	0	Interrupt is pending indicator.
	1 2	These bits identify the highest-priority pending interrupt.
	3 | 7	Always set to logical 0. |
03FB		Line control register:
	0	Word-length-select bit 0.
	1	Word-length-select bit 1.
	2	Number of stop bits.
	3	Parity enable.
	4	Even parity select.

Table C-23 Serial Port 1 (Continued)

Address (Hex)	Bit	Description
03FB (Continued)		
	5	Stuck parity.
	6	Set break.
	7	Divisor-latch-access bit.
03FC		Modem control register:
	0	Data terminal ready.
	1	Request-to-send.
	2	Output 1.
	3	Output 2.
	4	Loop.
	5 | 7	Always set to logical 0.
03FD		Line status register.
	0	Receive data-ready indicator.
	1	Overrun error indicator.
	2	Parity error indicator.
	3	Framing error indicator.
	4	Break interrupt indicator.
	5	Transmitter holding register empty.
	6	Transmitter shift register empty.
	7	Always set to logical 0.

Table C-23 Serial Port 1 (Continued)

Address (Hex)	Bit	Description
03FE		Modem status register:.
	0	Delta clear-to-send.
	1	Delta data-set ready.
	2	Trailing-edge ring indicator.
	3	Delta receive line signal detect.
	4	Clear-to-send.
	5	Data-set ready.
	6	Ring indicator.
	7	Receive line signal detect.
03FF		Reserved.
0400 – 7FFF		Duplicate.
8000 – 87FF		Nonvolatile RAM.
88FF – FFFF		Duplicate.

Appendix D

PAL Programming Information

This appendix tabulates programming information for the various programmable array logic (PAL) devices on the BUSINESS-PRO main logic board. These devices respond to various clocks, control signals, and address information to generate control signals for memory, DMA, and I/O operations.

The following conventions apply to all tables in this appendix:

* When the logical AND of terms from one row is ORed with the logical AND of terms from another row, the output goes low if the result is true.

* Output signals are listed in the left hand column. Some of these signals are generated by a PAL device only for its own internal use. These signals are indicated by an asterisk (*).

* The input variables and the device pins where they appear are listed at the top of the columns.

Table D-1 through Table D-12 list the functions of the main logic board PAL devices.

Table D-1 Reset/Ready Control PAL U14

Logic Sheet 5

	1 24MHZB	2 RES-	3 MS1	4 MS0	5 COWS-	6 IDLE	7 YR	8 ARDY-	9 JRDY	12 6MHZ-	13 XR	14 RESET	15 RX-*	16 Q0*	17 Q1*	18 READY-	19 12MHZ-
Q1*	C	-	0	-	-	0	-	-	-	1	-	0	-	1	1	-	1
	C	-	-	0	-	0	-	-	-	1	-	0	-	1	1	-	1
	C	-	-	-	-	0	-	-	-	-	-	0	-	0	0	-	-
Q0*	C	-	0	-	-	0	-	-	-	1	-	0	-	1	1	-	1
	C	-	-	0	-	0	-	-	-	1	-	0	-	1	1	-	1
	C	-	-	-	-	0	-	-	-	-	-	0	-	1	0	-	-
	C	-	-	-	-	0	-	-	-	-	-	0	-	0	1	1	-
XR	C	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0
	C	-	-	-	-	-	-	-	-	-	0	-	-	-	-	-	1
RESET	C	-	-	-	-	-	-	-	-	-	0	-	-	-	-	-	0
	C	-	-	-	-	-	-	-	-	-	-	0	-	-	-	-	1
RX-*	C	-	-	-	-	-	0	0	-	1	-	-	-	-	-	-	0
	C	-	-	-	-	-	0	-	0	1	-	-	-	-	-	-	0
	C	-	-	-	-	-	0	-	-	0	-	-	0	-	-	-	0
	C	-	-	-	-	-	0	-	-	-	-	-	0	-	-	-	1
READY-	C	-	-	-	0	-	-	-	-	0	-	-	-	0	1	-	0
	C	-	-	-	-	-	-	0	-	0	-	-	0	0	1	-	0
	C	-	-	-	-	-	-	-	-	1	-	-	-	-	-	0	0
	C	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	1
	C	-	-	-	-	-	1	-	-	-	-	-	-	-	-	-	-

Table D-2 Memory and I/O Control PAL U60

Logic Sheet 6

	1 12MHZ-	2 STAT	3 TURBO	4 G1A	5 STOP	6 0WS-	7 6MHZ	8 DATACON-	9 BRDY-	13 Q3	14 Q2*	15 Q1	16 Q0*	17 CEN-	19 MM/IO
Q1	C	-	-	-	-	-	1	-	-	-	0	0	0	-	-
	C	-	-	-	-	1	1	-	-	-	0	1	1	-	-
	C	-	-	-	-	1	1	-	-	-	1	0	0	-	-
	C	-	-	-	-	0	1	1	-	-	-	-	-	1	-
	C	-	-	-	-	-	0	-	-	-	-	0	-	-	-
	C	-	-	-	-	-	1	-	-	-	1	1	0	0	-
	C	-	-	-	0	-	-	-	-	-	-	-	-	-	-
Q2*	C	-	-	-	-	-	1	-	-	-	0	0	-	-	-
	C	-	-	-	-	1	1	-	-	-	0	1	0	-	-
	C	-	-	-	-	1	1	1	-	-	1	0	0	-	-
	C	-	-	-	-	-	1	-	-	-	1	1	0	0	-
	C	-	-	-	-	0	1	1	-	-	-	-	-	1	-
	C	-	-	-	-	-	0	-	-	-	0	-	-	-	-
	C	-	-	-	0	-	-	-	-	-	-	-	-	-	-
Q3	C	0	-	-	-	-	1	-	-	-	0	0	0	-	-
	C	-	1	0	-	-	1	-	-	-	0	0	0	-	1
	C	0	-	-	-	0	1	1	-	-	-	-	-	1	-
	C	-	-	-	-	-	1	1	-	-	1	0	0	-	-
	C	-	-	-	-	-	0	-	-	0	-	-	-	-	-
	C	-	-	-	0	-	-	-	-	-	-	-	-	-	-
Q0*	C	0	-	-	-	-	1	-	-	-	0	0	0	-	-
	C	-	1	0	-	-	1	-	-	-	0	0	0	-	1
	C	-	-	-	-	-	1	1	-	-	1	0	0	-	-
	C	-	-	-	-	-	1	-	-	-	-	-	1	-	-
	C	0	-	-	-	0	1	-	-	-	-	-	-	1	-
	C	-	-	-	-	-	1	-	-	-	1	1	0	1	-
	C	-	-	-	-	-	0	-	-	-	-	-	0	-	-
	C	-	-	-	0	-	-	-	-	-	-	-	-	-	-
CEN-	C	-	-	-	-	-	0	-	-	-	0	0	1	0	-
	C	-	-	-	-	-	0	0	0	-	1	1	0	-	-
	C	-	-	-	-	-	1	-	-	-	1	1	0	0	-

Table D-2. Memory and I/O Control PAL U60 (Continued)

Logic Sheet 6

	1 12MHZ-	2 STAT	3 TURBO	4 G1A	5 STOP	6 0WS-	7 6MHZ	8 DATACON-	9 BRDY-	13 Q3	14 Q2*	15 Q1	16 Q0*	17 CEN-	19 MM/IO
CONALE	C	-	-	-	-	-	-	-	-	-	0	-	-	-	-
	C	-	-	-	-	-	-	-	-	-	1	0	-	-	-
	C	-	-	-	-	-	0	-	-	-	1	1	-	-	-
	C	-	-	-	-	-	1	-	-	-	1	1	-	1	-
MASK0WS	C	-	-	-	-	-	-	1	-	-	-	-	-	1	-

Table D-3 I/O Decode Logic PAL U54

Logic Sheet 9

	1 DMA1CS-	2 INTR1CS-	3 PPICS-	4 TI/IBM	5 PDMA4	6 PDMA3	7 PDMA2	8 PDMA1	9 PDMA0	11 IO-
XDMA1CS-	0	-	-	0	0	-	-	-	-	-
	0	-	-	1	0	0	1	-	-	-
	0	-	-	1	0	1	-	-	-	-
PRT0-	0	-	-	1	0	0	0	0	0	0
PRT3-	0	-	-	1	0	0	0	1	1	0
	0	-	-	0	1	0	0	1	1	0
PRT12-	0	-	-	-	1	0	0	1	0	0
53CS-	0	-	-	1	1	0	1	-	-	-
INT1-	-	0	-	-	-	-	-	-	-	-
	0	-	-	1	1	1	0	0	-	-
42CS-	-	-	0	-	0	0	-	-	0	-
42C/D-	-	-	0	-	0	0	0	-	0	-

Table D-4 I/O Decode Logic PAL U55

Logic Sheet 9

	1 PPICS-	2 CS287-	3 PDMA4	4 PDMA3	5 PDMA0	6 IOR-	7 IOW-	8 ADD	9 INTA-	11 CSNVRAM
PRT61-	0	-	0	0	1	0	-	-	-	0
	0	-	0	0	1	-	0	-	-	-
PRT70-	0	-	1	-	0	-	0	-	-	-
PRT71-	0	-	1	-	1	-	-	-	-	0
	0	-	1	-	1	-	0	-	-	-
PRT68-	0	-	0	1	0	0	-	-	-	0
	0	-	0	1	0	-	0	-	-	-
DATA8DIR-	-	-	-	-	-	-	-	-	0	-
	-	1	-	-	-	0	-	1	-	-
	-	-	-	-	-	0	-	-	-	1
RST287-	-	0	1	0	1	-	0	-	-	-
NPCS-	-	0	1	1	-	-	-	-	1	0
BUSYCLR-	-	0	1	0	0	-	0	-	-	-

Table D-5 I/O Decode Logic PAL U56

Logic Sheet 9

	1 INTA-	2 XM/IO	3 FSYS16+	4 IO16-	5 AEN1-	6 AEN2-	7 CSNVRAM	8 SIOWC-	9 MEMR-	11 MEMW-	13 PDMBHE-	14 PDMA0	15 DMAEN-	16 Q1	
DIR245	-	-	-	-	1	1	-	-	-	0	0	-	-	-	
	-	-	-	-	0	-	-	-	0	-	-	-	-	-	
	-	0	-	-	1	1	-	0	-	-	0	-	-	-	
GATE245-	-	-	0	-	1	1	-	-	0	-	0	1	-	-	
	-	-	0	-	1	1	-	-	-	0	0	1	-	-	
	1	0	-	1	1	1	0	-	-	-	0	1	-	-	
	1	0	-	-	1	1	1	0	-	-	0	1	-	-	
	1	0	1	-	0	-	-	1	-	-	0	-	-	-	
	-	-	1	-	0	-	-	-	-	0	0	-	-	-	
	-	-	1	-	0	-	-	-	0	-	0	-	-	-	
ENDCYC-	-	0	-	0	-	-	0	-	-	-	-	-	-	1	
	-	1	1	-	-	-	-	-	-	-	-	-	-	1	
DATA01	-	1	0	-	1	1	-	-	-	-	0	0	-	-	
	1	0	-	1	1	1	-	-	-	-	0	0	-	-	
	1	0	-	-	1	1	1	-	-	-	0	0	-	-	
DMAEN-	-	-	-	-	0	-	-	-	-	-	-	-	-	-	
	-	-	-	-	-	0	-	-	-	-	-	-	-	-	
PDMBHE-	-	-	-	-	0	-	-	-	-	-	-	1	-	-	NOTE 1
	-	-	-	-	-	0	-	-	-	-	-	-	-	-	NOTE 1
PDMA0	-	-	-	-	-	0	-	-	-	-	-	-	-	-	NOTE 2

NOTES:

1. PDMBHE- is an output only when DMAEN- is low.

2. PDMA0 is an output only when AEN2- is low.

Table D-6 Serial/Parallel Port Decode PAL U85

Logic Sheet 15

	1 TI/IBM	2 PJMP1	3 SJMP1	4 PDMA9	5 PDMA8	6 PDMA7	7 PDMA6	8 PDMA5	9 PDMA4	11 PDMA3	13 PDMA2	14 PDMA1	15 PDMA0	16 PARDAT-	17 PARCNTL	18 PARSTAT
PARDAT-	0	1	-	1	1	0	1	1	1	1	-	0	0	-	-	-
	0	0	-	1	0	0	1	1	1	1	-	0	0	-	-	-
	1	-	-	0	0	0	0	0	0	0	0	1	0	-	-	-
PARSTAT	0	1	-	1	1	0	1	1	1	1	-	0	1	-	-	-
	0	0	-	1	0	0	1	1	1	1	-	0	1	-	-	-
	1	-	-	0	0	0	0	0	0	0	0	0	1	-	-	-
PARCNTL	0	1	-	1	1	0	1	1	1	1	-	1	0	-	-	-
	0	0	-	1	0	0	1	1	1	1	-	1	0	-	-	-
	1	-	-	0	0	0	0	0	0	0	0	1	1	-	-	-
SEREN-	-	-	1	1	1	1	1	1	1	1	-	-	-	-	-	-
	-	-	0	1	0	1	1	1	1	1	-	-	-	-	-	-
PTREN-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	-	-
	-	-	1	1	1	1	1	1	1	1	-	-	-	-	-	-
	-	-	0	1	0	1	1	1	1	1	-	-	-	-	-	-
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	-
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0

Table D-7 CPU Data Bus Control PAL U92

Logic Sheet 12

	1 24MHZ	2 12MHZ	3 6MHZ	4 G1A-	5 MA0	6 MBHE-	7 XLSA0	8 XPDMBHE-	9 CDEN	12 YMS0	13 DAK	15 CDH-	16 CDIR	17 J/M*	18 CMA0	19 YMDIR
CDH-	C	0	0	1	-	-	-	1	1	-	0	-	-	-	-	0
	C	0	0	1	-	-	-	1	1	0	0	-	-	-	-	-
	C	0	0	-	-	-	-	1	1	1	0	-	-	0	-	1
	C	0	1	-	-	-	-	1	1	-	0	-	-	0	-	-
	C	1	-	-	-	-	-	1	1	-	0	-	-	0	-	-
	C	1	1	-	-	-	-	-	1	-	0	-	-	1	-	-
	C	-	-	-	-	-	-	-	1	-	0	0	-	1	-	-
	C	-	-	0	-	0	-	-	1	-	1	-	-	-	-	-
CDL-	C	0	0	1	-	-	1	-	1	-	0	-	-	-	-	0
	C	0	0	1	-	-	1	-	1	0	0	-	-	-	-	-
	C	0	0	-	-	-	1	-	1	1	0	-	-	0	-	1
	C	0	1	-	-	-	1	-	1	-	0	-	-	0	-	-
	C	1	-	-	-	-	1	-	1	-	0	-	-	0	-	-
	C	1	1	-	-	-	-	-	1	-	0	-	-	1	-	-
	C	-	-	-	-	-	-	-	1	-	0	0	-	1	-	-
	C	-	-	0	-	-	-	-	1	-	1	-	-	-	0	-
CDIR	C	0	0	1	-	-	-	-	1	-	0	-	-	-	-	0
	C	0	0	-	-	-	-	-	1	1	0	-	0	-	-	1
	C	0	1	-	-	-	-	-	1	-	0	-	0	-	-	-
	C	1	-	-	-	-	-	-	1	-	0	-	0	-	-	-
	C	-	-	-	-	-	-	-	1	-	1	-	-	0	-	-
J/M*	C	0	0	1	-	-	-	-	1	-	0	-	-	-	-	0
	C	0	0	1	-	-	-	-	1	0	0	-	-	-	-	-
	C	0	0	-	-	-	-	-	1	1	0	-	-	0	-	1
	C	0	1	-	-	-	-	-	1	-	0	-	-	0	-	-
	C	1	-	-	-	-	-	-	1	-	0	-	-	0	-	-
	C	-	-	-	-	-	-	-	1	-	1	-	-	-	-	1

Table D-8 Refresh Arbiter PAL U101

Logic Sheet 19

	1 CK2	2 RST-	3 LK-	4 RFB	5 AEN-	6 HOLDA	7 DRQ	8 RFQ-	9 FH-	15 XDRQ*	16 XRFQ*	17 Q0*	18 Q1*	19 LHLDA*
LHLDA*	C	-	-	-	-	0	-	-	-	-	-	-	-	-
Q1*	C	1	-	-	-	-	-	-	-	-	-	1	1	0
	C	1	-	-	-	-	-	-	-	1	-	0	0	-
	C	1	-	-	-	-	-	-	-	-	1	1	0	0
	C	1	-	-	-	-	-	-	-	1	-	1	0	0
Q0*	C	1	-	-	-	-	-	-	-	-	0	1	1	0
	C	1	-	-	-	-	-	-	-	-	1	1	0	1
	C	1	-	-	-	-	-	-	-	1	-	1	0	1
	C	1	-	-	-	-	-	-	-	-	1	0	1	-
	C	1	-	-	-	-	-	-	-	1	-	0	1	-
XRFQ*	C	-	-	-	-	-	-	1	-	-	-	1	1	-
	C	-	0	-	-	-	-	-	-	-	-	1	1	-
	C	-	-	-	-	-	-	-	-	1	-	0	0	-
	C	-	0	-	-	-	-	-	-	-	-	1	0	0
	C	-	-	0	-	-	-	-	-	-	-	0	1	-
	C	-	-	-	-	-	-	-	-	-	0	-	0	-
	C	-	-	-	-	-	-	-	-	-	0	0	1	-
	C	0	-	-	-	-	-	-	-	-	-	-	-	-
XDRQ*	C	-	-	-	-	-	0	-	-	-	-	0	0	-
	C	1	-	-	-	-	-	-	-	-	1	1	1	0
	C	-	0	-	-	-	-	-	-	-	-	0	0	-
	C	-	0	-	-	-	-	-	-	-	-	1	0	0
	C	-	-	-	1	-	0	-	-	-	-	0	1	-
	C	-	-	-	-	-	-	-	-	0	-	-	1	-
	C	-	-	-	-	-	-	-	-	0	-	1	0	-
	C	0	-	-	-	-	-	-	-	-	-	-	-	-
DAK	C	-	-	-	-	-	-	-	-	0	0	0	1	-
	C	-	-	-	-	-	-	-	-	-	1	1	0	1
	C	-	-	-	-	-	-	-	-	-	1	0	1	-
	C	-	-	-	-	-	-	-	-	-	-	1	0	0
	C	-	-	-	-	-	-	-	-	-	-	1	1	-
	C	-	-	-	-	-	-	-	-	-	-	0	0	-
	C	0	-	-	-	-	-	-	-	-	-	-	-	-

Table D-8. Refresh Arbiter PAL U101 (Continued)

Logic Sheet 19

	1 CK2	2 RST-	3 LK-	4 RFB	5 AEN-	6 HOLDA	7 DRQ	8 RFQ-	9 FH-	15 XDRQ*	16 XRFQ*	17 Q0*	18 Q1*	19 LHLDA*
RAK-	C	1	-	-	-	-	-	-	-	0	1	1	0	1
	C	1	-	-	-	-	-	-	-	0	1	0	1	-
HOLD	C	-	-	-	-	-	-	-	1	0	-	0	0	-
	C	-	-	-	-	-	-	-	1	0	0	1	0	0
	C	-	-	-	-	-	-	-	1	0	0	0	1	-
	C	-	-	-	-	-	-	-	1	-	-	1	1	1
	C	-	-	-	-	-	-	-	1	-	0	1	1	0
	C	0	-	-	-	-	-	-	1	-	-	-	-	-

Table D-9 Refresh Sequence Control PAL U102

Logic Sheet 19

	1 24MHZB	2 RST-	3 LOCK-	4 SOFTRES	5 MS1	6 RAK-	7 OUT1/8	8 54OUT1	9 DB	13 REFDET	14 LRFQ-	15 LK-*	16 DRAK-*	17 DO14*	18 DO1*	19 X2
DO14*	C	-	-	-	-	-	0	-	-	-	-	-	-	-	-	-
DO1*	C	-	-	-	-	-	-	0	-	-	-	-	-	-	-	-
LRFQ-	C	-	-	-	-	-	-	0	0	-	-	-	-	-	1	1
	C	-	-	-	-	-	0	-	1	-	-	-	-	1	-	1
	C	1	-	-	-	-	-	-	-	-	0	-	-	-	-	1
DRAK-*	C	-	-	-	-	0	-	-	-	-	-	-	-	-	-	-
REFDET	C	-	-	-	-	0	-	-	-	1	-	-	1	-	-	-
	C	-	-	-	-	1	-	-	-	0	-	-	-	-	-	-
	C	-	-	-	-	-	-	-	-	0	-	-	0	-	-	-
	C	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-
LK-*	C	1	-	-	1	-	-	-	-	-	-	0	-	-	-	-
	C	1	-	1	-	-	-	-	-	-	-	-	-	-	-	-
GLOCK-	C	-	-	-	-	-	-	-	-	-	-	0	-	-	-	-
	C	-	0	-	-	-	-	-	-	-	-	-	-	-	-	-
	C	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Table D-10 Dual-Mode Refresh Generator PAL U104

Logic Sheet 19

	1 24MHZB	2 12MHZ	3 6MHZ	4 SRES	5 WAIT-	6 RAK-	7 RCO	8 DB	9 IDLE	12 CK590	13 RFBUSY	14 X2	15 X1	16 Q0*	17 Q1*	18 Q2*	19 PRESET
Q2*	C	0	-	-	-	-	-	-	0	-	-	-	-	-	-	0	-
	C	1	1	-	-	-	-	-	0	-	-	-	-	-	-	0	-
	C	1	0	-	-	0	-	-	0	-	-	-	-	1	1	1	-
	C	1	0	-	-	-	-	-	0	-	-	-	-	1	0	0	-
	C	1	0	-	-	-	-	-	0	-	-	-	-	0	1	0	-
	C	1	0	-	-	-	-	-	0	-	-	-	-	0	1	1	-
Q1*	C	0	-	-	-	-	-	-	0	-	-	-	-	-	0	-	-
	C	1	1	-	-	-	-	-	0	-	-	-	-	-	0	-	-
	C	1	0	-	-	0	-	-	0	-	-	-	-	1	1	1	-
	C	1	0	-	-	-	-	-	0	-	-	-	-	1	1	0	-
	C	1	0	-	-	-	-	0	0	-	-	-	-	0	0	1	-
	C	1	0	-	-	-	1	1	0	-	-	-	-	0	0	1	-
	C	1	0	-	-	0	-	-	0	-	-	-	-	1	0	1	-
Q0*	C	0	-	-	-	-	-	-	0	-	-	-	-	0	-	-	-
	C	1	1	-	-	-	-	-	0	-	-	-	-	0	-	-	-
	C	1	0	-	-	-	-	-	0	-	-	-	-	1	0	0	-
	C	1	0	-	0	-	-	-	0	-	-	-	-	0	1	0	-
	C	1	0	-	-	-	-	-	0	-	-	-	-	1	1	0	-
	C	1	0	-	-	-	0	1	0	-	-	-	-	0	0	1	-
	C	1	0	-	-	-	-	-	0	-	-	-	-	0	1	1	-
X1	C	0	-	-	-	-	-	-	0	-	-	-	0	-	-	-	-
	C	1	1	-	-	-	-	-	0	-	-	-	0	-	-	-	-
	C	1	0	-	-	0	-	-	0	-	-	-	0	1	1	1	-
	C	1	0	-	-	-	-	-	0	-	-	-	-	0	1	1	-
	C	1	0	-	-	-	-	-	0	-	-	-	-	1	0	0	-
	C	1	0	-	-	-	-	-	0	-	-	-	0	0	1	0	-
	C	1	0	-	-	-	-	-	0	-	-	-	0	-	0	1	-
	C	1	0	-	-	-	-	-	0	-	-	-	0	1	1	1	-
X2	C	0	-	-	-	-	-	-	0	-	-	0	-	-	-	-	-
	C	1	1	-	-	-	-	-	0	-	-	0	-	-	-	-	-
	C	1	0	-	-	0	-	-	0	-	-	-	-	1	1	1	-
	C	1	0	-	-	-	0	1	0	-	-	0	-	0	0	1	-
	C	1	0	-	-	-	-	-	0	-	-	0	-	1	0	0	-
	C	1	0	-	-	-	-	-	0	-	-	0	-	-	1	0	-
	C	1	0	-	-	-	-	-	0	-	-	0	-	1	0	1	-
	C	1	0	-	-	-	-	-	0	-	-	0	-	-	1	1	-

Table D-10. Dual-Mode Refresh Generator PAL U104 (Continued)

Logic Sheet 19

		1 24MHZB	2 12MHZ	3 6MHZ	4 SRES	5 WAIT-	6 RAK-	7 RCO	8 DB	9 IDLE	12 CK590	13 RFBUSY	14 X2	15 X1	16 Q0	17 Q1	18 Q2	19 PRESET
RFBUSY	C	0	-	-	-	-	-	-	0	-	0	-	-	-	-	-	-	
	C	1	1	-	-	-	-	-	0	-	0	-	-	-	-	-	-	
	C	1	0	-	-	-	-	0	0	-	-	-	-	0	0	1	-	
	C	1	0	-	-	-	1	1	0	-	-	-	-	0	0	1	-	
	C	1	0	-	-	0	-	-	0	-	0	-	-	1	0	1	-	
CK590	C	0	-	-	-	-	-	-	0	0	-	-	-	-	-	-	-	
	C	1	1	-	-	-	-	-	0	0	-	-	-	-	-	-	-	
	C	1	0	-	-	-	-	-	0	-	-	-	-	1	1	0	-	
PRESET	C	0	-	0	-	-	-	-	1	-	-	-	-	-	-	-	-	
	C	0	1	0	-	-	-	-	0	-	-	-	-	-	-	-	-	
	C	0	0	-	-	-	-	-	0	-	-	-	-	-	-	-	0	
	C	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	

Table D-11 Main Memory Control PAL U119

Logic Sheet 22

	1 CK2	2 RO-	3 WO-	4 MDIR	5 BHE-	6 A0	7 RST	8 DXC-	9 FR	13 D1M-*	15 LEN	16 XCAS-	17 WE-	18 D1C-*
D1M-*	C	0	-	-	-	-	-	-	-	-	-	-	-	-
	C	-	0	-	-	-	-	-	-	-	-	-	-	-
D1C-*	C	0	1	-	-	-	0	-	-	-	-	-	-	-
	C	1	0	-	-	-	0	-	-	-	-	-	-	-
MUX	C	0	-	-	-	-	-	-	-	-	-	-	-	-
	C	-	0	-	-	-	-	-	-	-	-	-	-	-
	C	-	-	-	-	-	-	-	-	0	-	-	-	-
XCAS-	C	0	1	-	-	-	0	-	0	-	-	-	-	-
	C	1	0	-	-	-	0	-	0	-	-	-	-	-
	C	-	-	-	-	-	0	-	0	-	-	-	-	0
	C	-	-	-	-	-	0	-	1	-	-	0	-	-
373EN	C	0	1	-	-	-	0	-	-	-	-	-	-	-
	C	1	0	-	-	-	0	-	-	-	-	-	-	-
	C	-	-	-	-	-	0	-	-	-	-	-	-	0
	C	-	-	-	-	-	0	0	-	-	-	-	-	-
WE-	C	1	0	-	-	-	0	-	-	-	-	-	-	-
	C	-	-	1	-	-	0	-	-	-	-	-	-	0
	C	-	-	1	-	-	0	0	-	-	-	-	-	-
MDH-	C	-	-	-	-	-	0	-	-	-	-	-	0	-
	C	-	-	0	0	-	0	-	-	-	0	-	-	-
MDL-	C	-	-	-	-	-	0	-	-	-	-	-	0	-
	C	-	-	0	-	0	0	-	-	-	0	-	-	-

Table D-12 Parity Control PAL U124

Logic Sheet 20

	2 G1A-	3 MRDC-	4 64KSEL-	5 DAK	6 PKEN-	7 WE-	8 XCAS-	9 RST-	11 NPARER	14 L64KSEL-	15 IJ112	16 POL	17 POH	
L64KSEL-	-	-	0	0	-	-	1	1	-	-	-	-	-	NOTE 1
	-	-	-	0	-	-	0	1	-	0	-	-	-	NOTE 1
	-	-	0	1	-	-	-	1	-	-	-	-	-	NOTE 1
	-	-	0	-	-	-	-	1	-	0	-	-	-	NOTE 1
	-	-	0	-	-	-	1	1	-	1	-	-	-	NOTE 1
DUMY*	-	-	-	-	-	-	-	1	-	-	-	1	1	NOTE 2
POH	-	-	-	-	-	-	-	-	0	-	-	-	-	NOTE 3
POL	-	-	-	-	-	-	-	-	0	-	-	-	-	NOTE 3
PK	-	-	-	0	0	1	-	1	-	-	0	-	-	
	0	0	-	1	0	-	-	1	-	-	-	-	-	

NOTES:

1. L64KSEL- is an output only when RST- is high.

2. DUMY is an output only when RST- is low.

3. POH and POL are outputs only when WE- is low and RST- is high.

Appendix E

System Logic Diagrams

E.1 MAIN LOGIC BOARD LOGIC DIAGRAMS

The first part of this appendix contains the logic diagrams for the main logic board, drawing number 2240842 (26 sheets). The following list of the various logic circuits indicates the logic diagram sheet on which the circuits are located:

* Processor logic -- sheet 3
* System ROM and reset logic -- sheet 4
* System clocks -- sheet 5
* Coprocessor logic -- sheet 6
* Reset and nonmaskable interrupt logic -- sheet 7
* Interrupt controllers -- sheet 8
* Decode logic -- sheet 9
* Ports decode logic -- sheet 10
* Real-time clock -- sheet 11
* Data bus control and internal data ports -- sheet 12
* Bus latches -- sheet 13
* Keyboard and mouse interface -- sheet 14
* Printer logic -- sheet 15
* DMA controller -- sheet 17
* DMA/refresh arbiter and refresh controller -- sheet 19
* Parity error logic -- sheet 20
* 640K memory decode and buffers -- sheet 21
* DRAM control sequencer -- sheet 22

* DRAM bank decode and address multiplexer -- sheet 23
* DRAM bank 0 -- sheet 24
* DRAM bank 1 -- sheet 25
* Expansion bus interface -- sheet 26

E.2 OTHER BUSINESS-PRO LOGIC DIAGRAMS

Other logic diagrams contained in this appendix are as follows:

Diagram Number	Subject	Sheets
2240841	CPU Printed Wiring Board	2
2240845	Bus Interface Connector Board	6
2240849	Vertical Board	2
2240921	Floppy Disk Controller Board	10
2240924	Winchester Disk Controller Board	13
2240927	3 Megabyte Expansion Board	7
2240930	256 X 9 DRAM Expansion Card	3
2240933	Communication Board	3
2240936	Alpha Graphics Video Board	9
2223011	Alpha CRT Controller	3
2240939	Dual Mode Video Board	6
2540317	PC-AT Mode II CRT Controller (To Be Supplied)	
________	System Interconnect Diagram (To Be Supplied)	

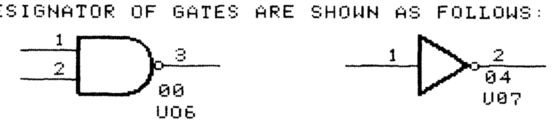
8	7	6	5	4	3	2	1

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	CN 500336 (E) D.JONES	12-2-85	[illegible]

NOTES, UNLESS OTHERWISE SPECIFIED:

1. ALL DEVICES ARE PREFIXED WITH SN74, A LETTER "T" IN A PREFIX IS EQUAL TO "LS", AND A LETTER "F" AS A SUFFIX IS EQUAL TO CHIP CARRIER.
2. VCC IS APPLIED TO PIN 8 OF ALL 8-PIN IC's, PIN 14 OF ALL 14-PIN IC's, PIN 16 OF ALL 16-PIN IC's, PIN 20 OF ALL 20-PIN IC's, ETC.
3. GROUND IS APPLIED TO PIN 4 OF ALL 8-PIN IC's, PIN 7 OF ALL 14-PIN IC's, PIN 8 OF ALL 16-PIN IC's, PIN 10 OF ALL 20-PIN IC's, ETC.
4. DEVICE TYPE, PIN NUMBERS, AND REFERENCE DESIGNATOR OF GATES ARE SHOWN AS FOLLOWS:



00 AND 04 = DEVICE TYPES
1, 2, AND 3 = PIN NUMBERS
U06 AND U07 = REFERENCE DESIGNATORS

5. RESISTANCE VALUES ARE IN OHMS.
6. RESISTORS ARE 1/4 WATT, 5%.
7. CAPACITANCE VALUES ARE IN MICROFARADS.

COMPUTER GENERATED DRAWING ; DO NOT REVISE MANUALLY

-1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES

PARTS LIST

REVISION STATUS OF SHEETS

REV	A	A	A	A	A	A		A	A	A
SH	1	2	3	4	5	6	7	8	9	10
REV	A	A	A	A	A	A				A
SH	11	12	13	14	15	16	17	18	19	20
REV	A		A							
SH	21	22	23	24	25	26				
REV										
SH										

NEXT ASSY	USED ON
2240843	8721

APPLICATION

		DATE
DWN	R.WHEELER	07-03-85
CHK	P.PETERSON	08-13-85
ENGR	S.WALLACE	08-13-85
APVD ENGR	S.WALLACE	08-13-85
QA	W.DILLER	08-13-85
APVD MFG	S.RILEY	08-15-85
RLSE	P.PETERSON	08-19-85

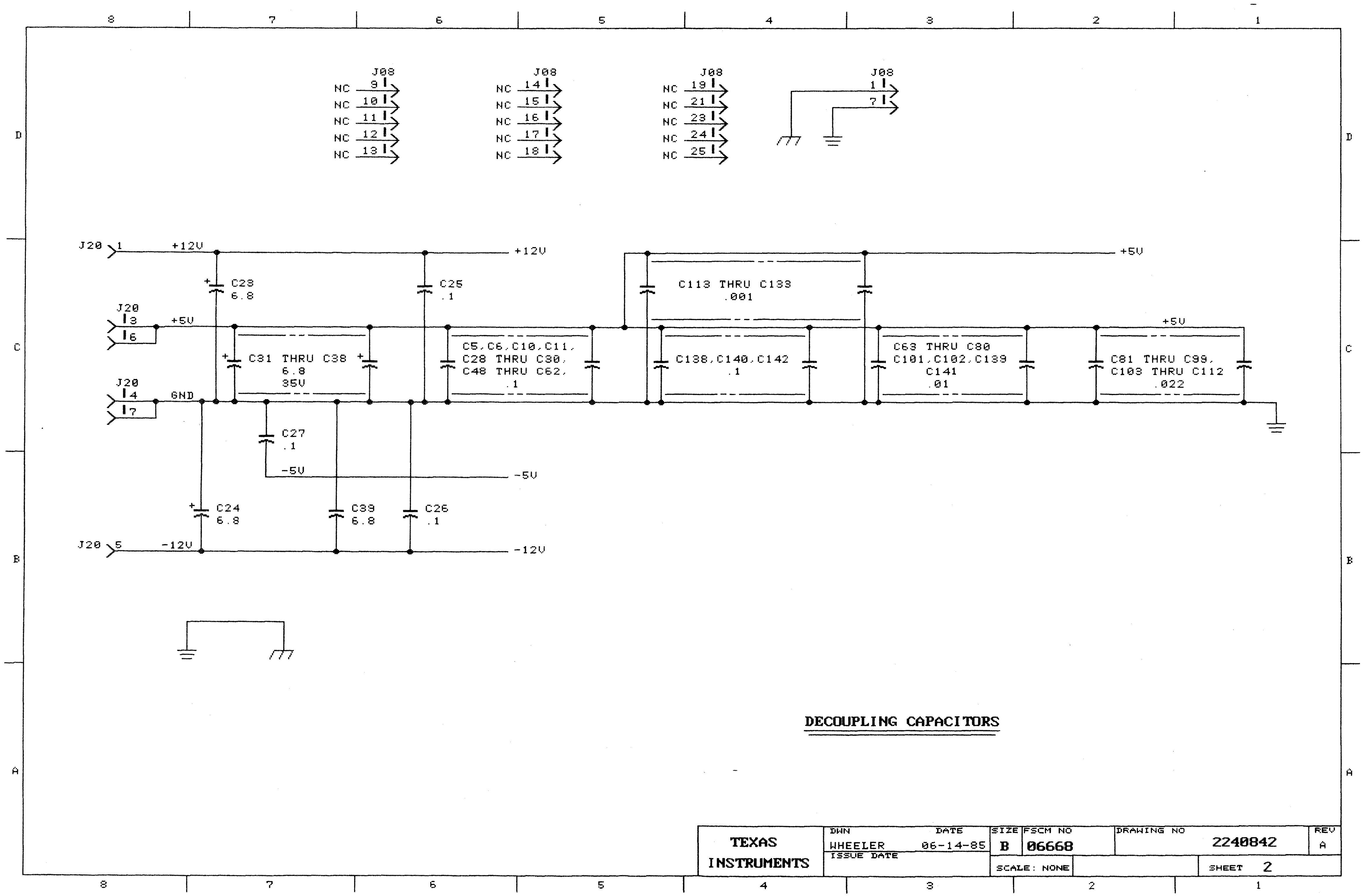
TEXAS INSTRUMENTS
Data Systems Group

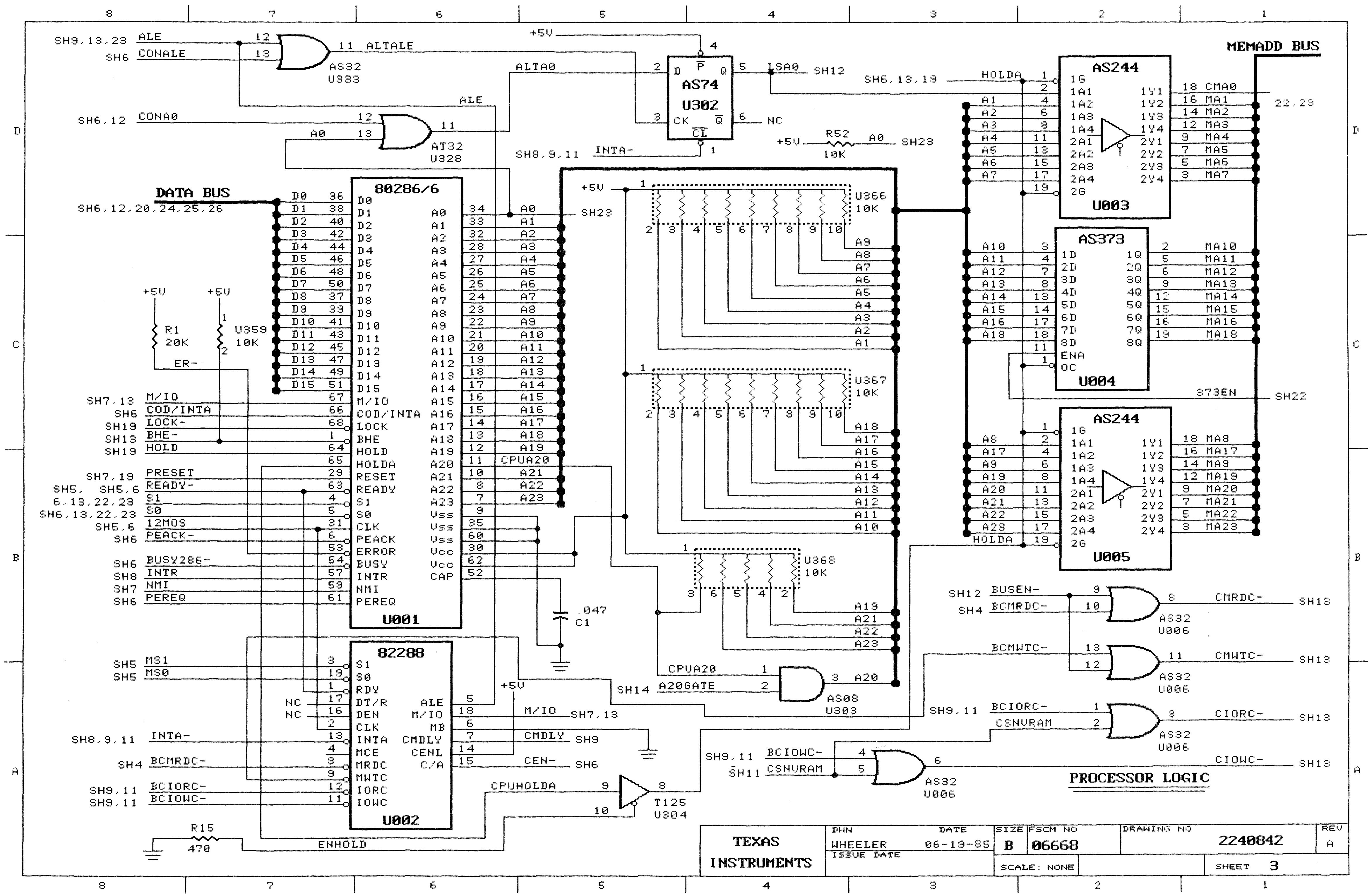
DIAGRAM, LOGIC, DETAILED-
MAIN LOGIC, EXCALIBUR

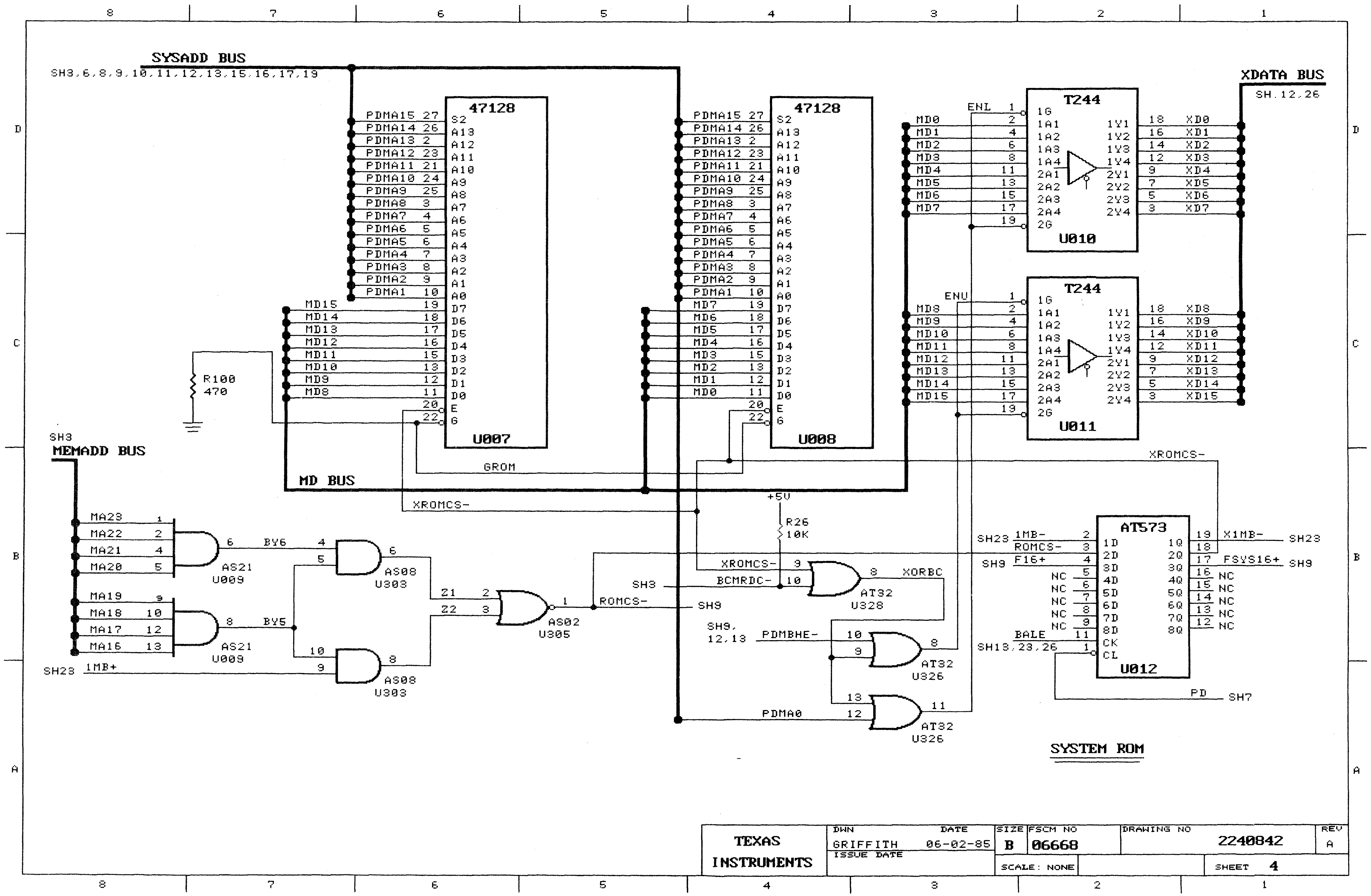
SIZE	FSCM NO	DRAWING NO	REV
B	06668	2240842	A

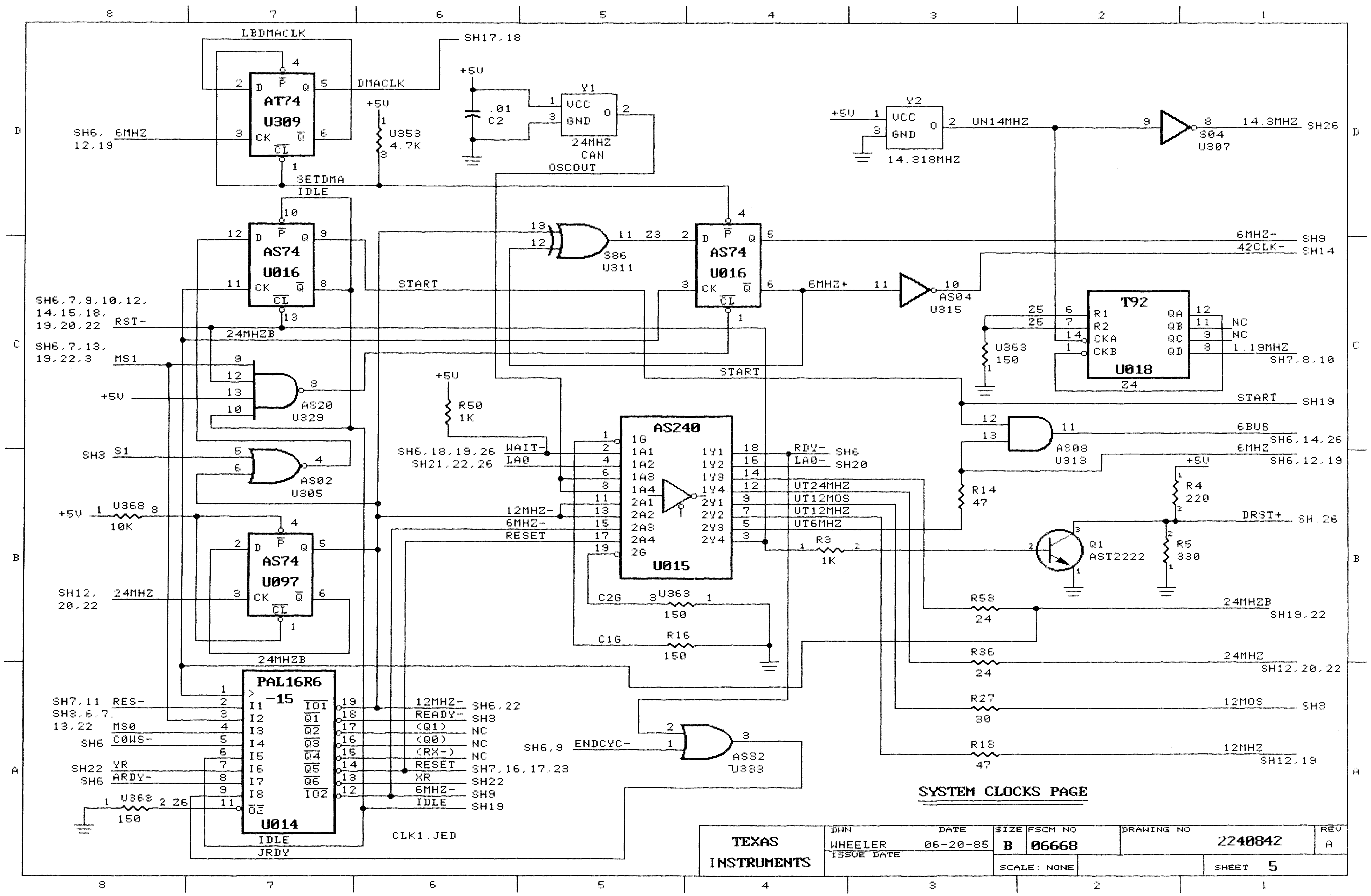
SCALE NONE SHEET 1 OF 26

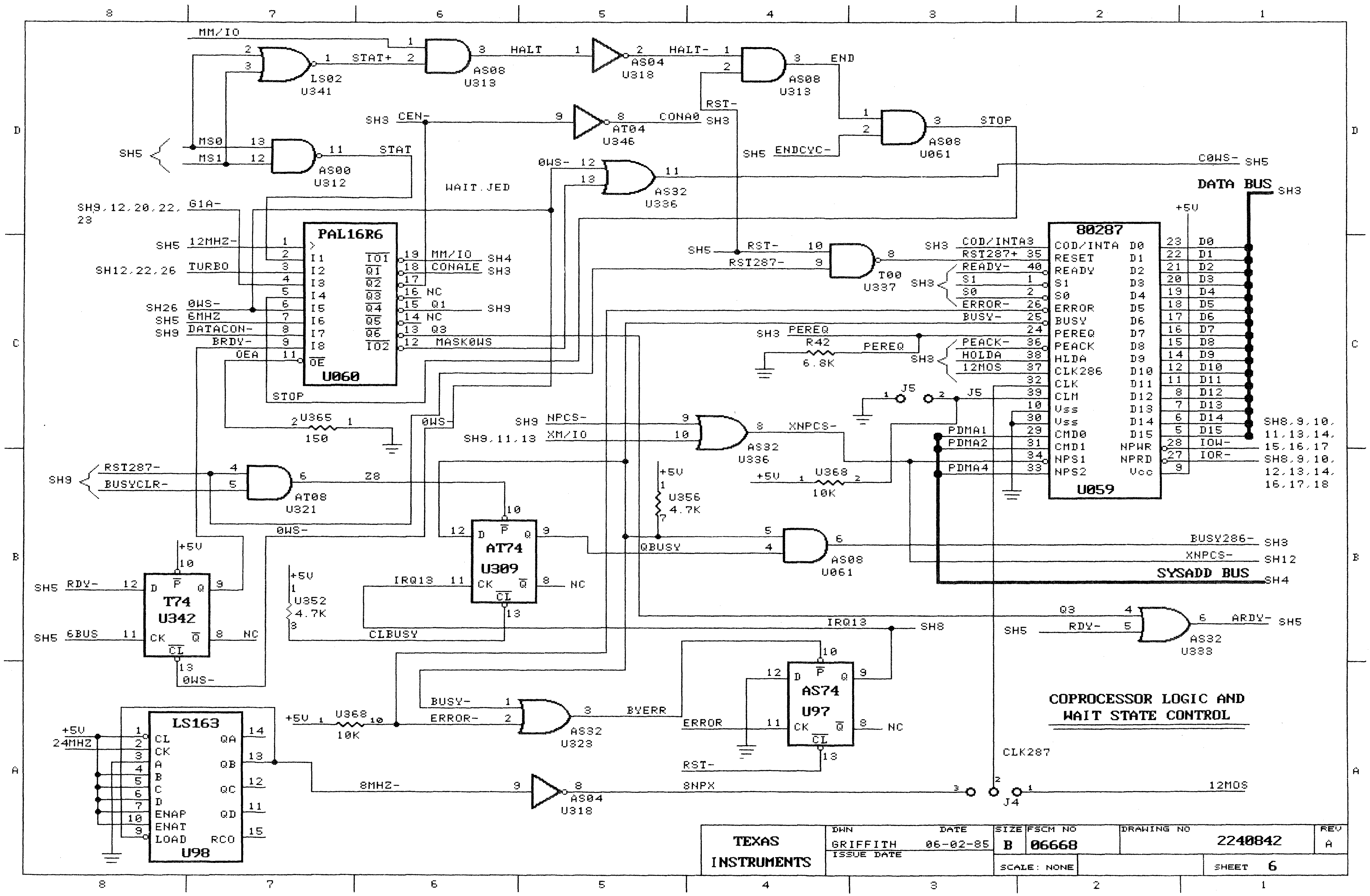
43 DB

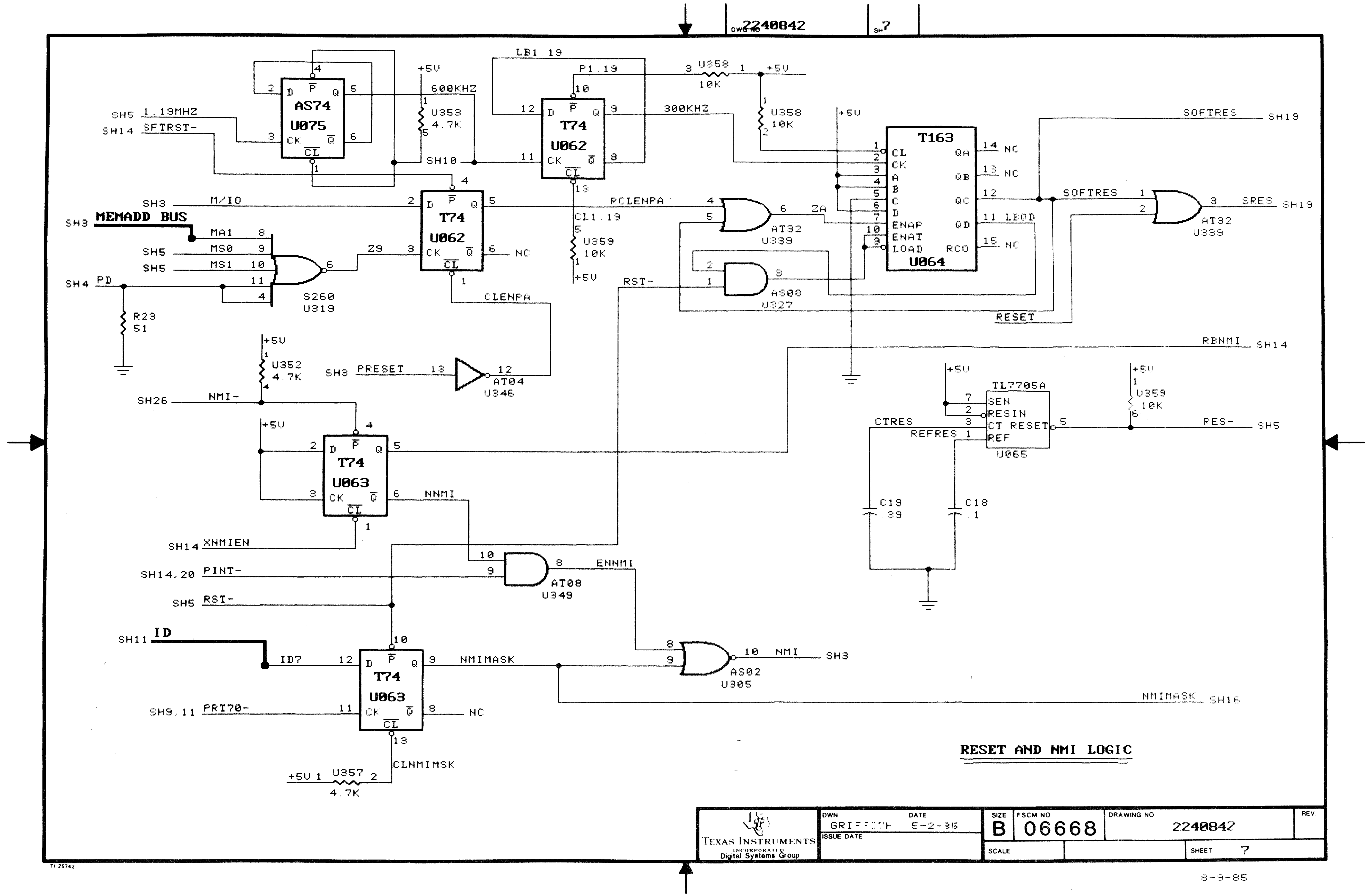

J08
NC 9
NC 10
NC 11
NC 12
NC 13
NC 14
NC 15
NC 16
NC 17
NC 18
NC 19
NC 21
NC 23
NC 24
NC 25
1
7
J20 1 +12V
+12V
C23 6.8
C25 .1
C113 THRU C133 .001
+5V
J20 3 6 +5V
C31 THRU C38 6.8 35V
C5, C6, C10, C11, C28 THRU C30, C48 THRU C62, .1
C138, C140, C142 .1
C63 THRU C80 C101, C102, C139 C141 .01
C81 THRU C99, C103 THRU C112 .022
J20 4 7 GND
C27 .1
-5V
-5V
C24 6.8
C39 6.8
C26 .1
J20 5 -12V
-12V
DECOUPLING CAPACITORS
TEXAS INSTRUMENTS
DWN WHEELER
DATE 06-14-85
ISSUE DATE
SIZE B
FSCM NO 06668
DRAWING NO 2240842
REV A
SCALE: NONE
SHEET 2

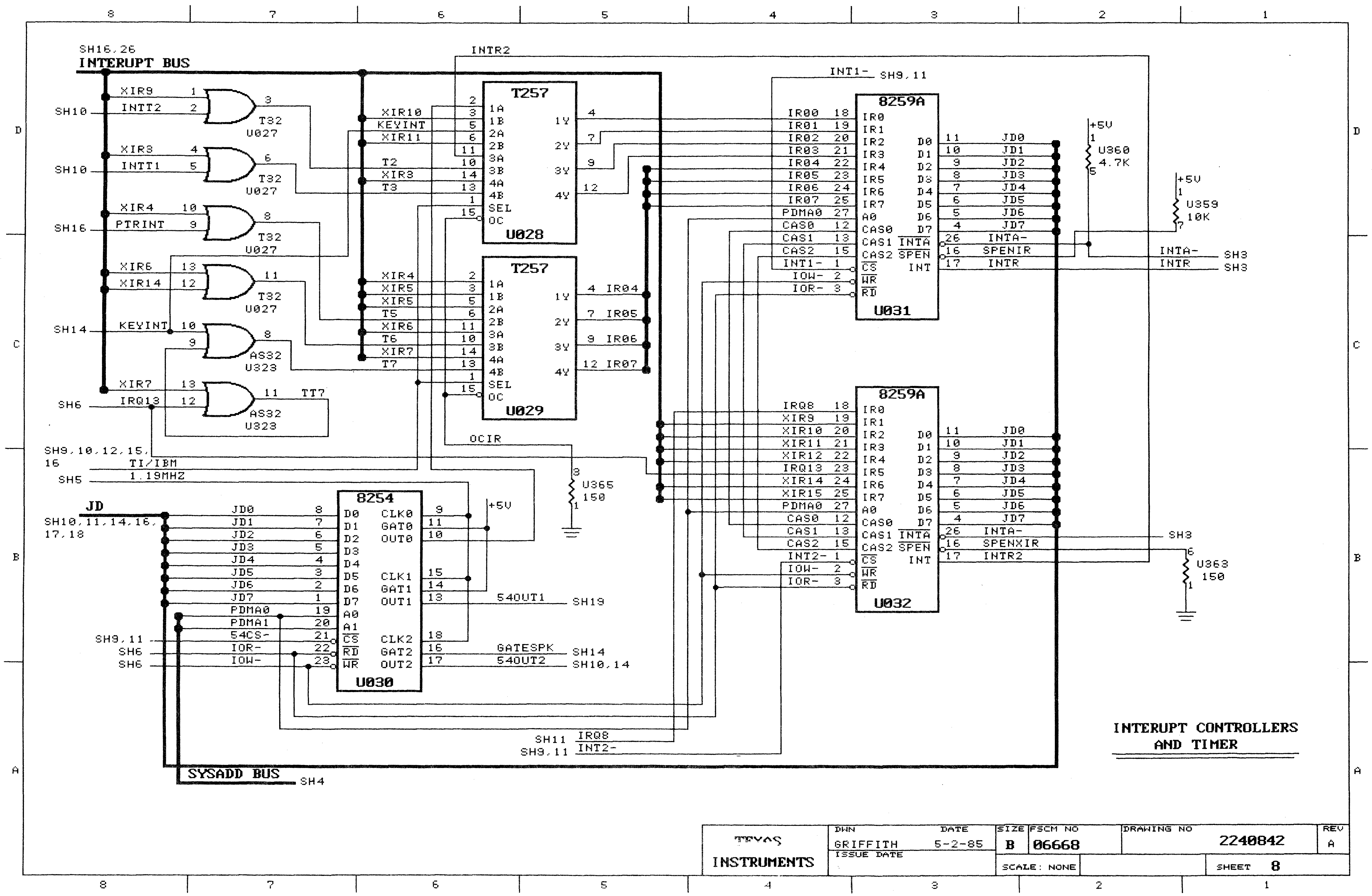

DATA BUS
MEMADD BUS
80286/6
U001
82288
U002
AS244
U003
AS373
U004
AS244
U005
AS74
U302
PROCESSOR LOGIC
TEXAS INSTRUMENTS
WHEELER
06-19-85
06668
2240842
SHEET 3

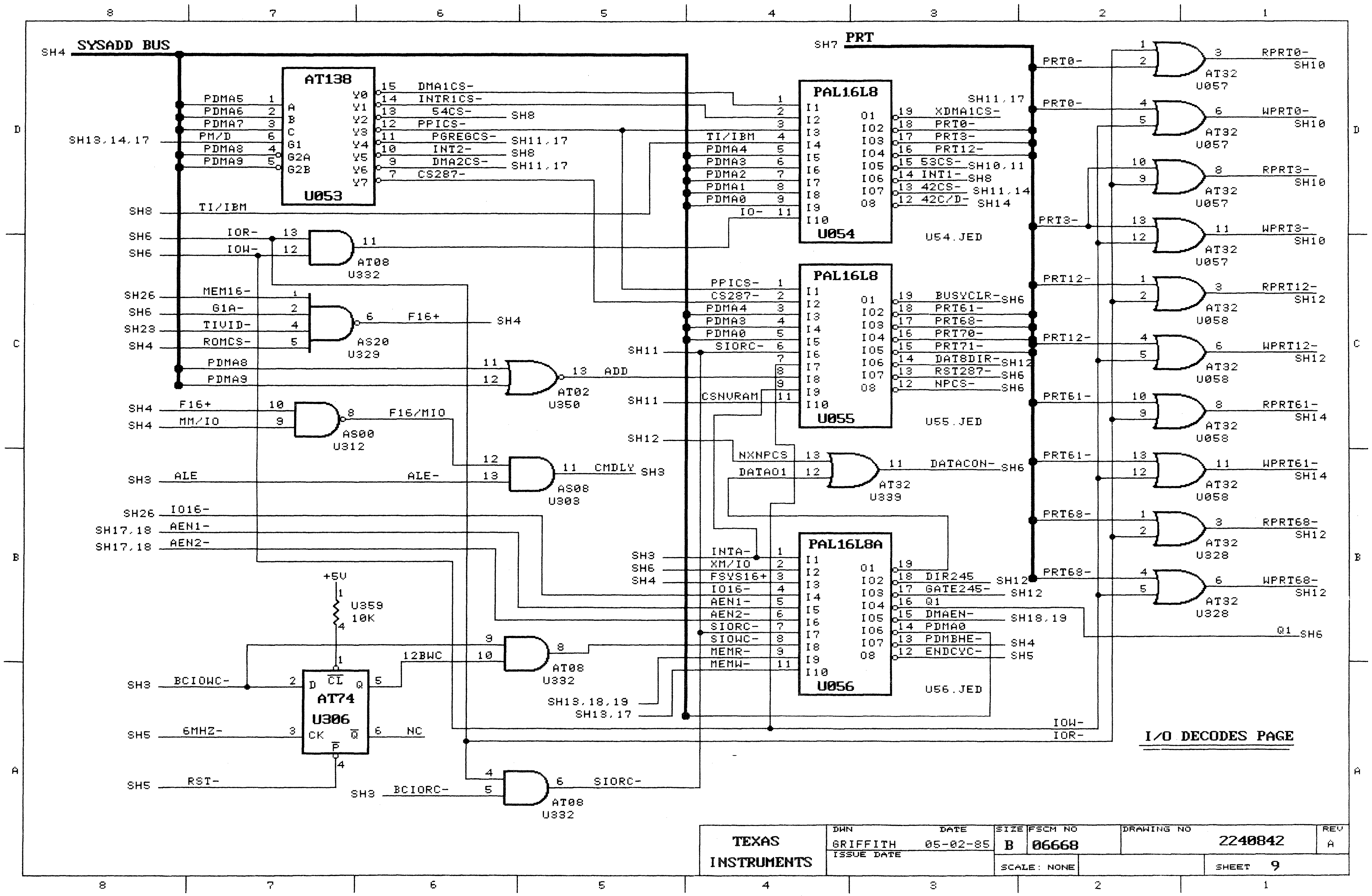

SYSADD BUS
SH3,6,8,9,10,11,12,13,15,16,17,19
47128
U007
47128
U008
MD BUS
MEMADD BUS
R100
470
GROM
XROMCS-
T244
U010
T244
U011
XDATA BUS
SH.12,26
AT573
U012
+5V
R26
10K
AS21
U009
AS08
U303
AS02
U305
AT32
U328
AT32
U326
ROMCS-
XORBC
BCMRDC-
PDMBHE-
PDMA0
SYSTEM ROM
TEXAS INSTRUMENTS
GRIFFITH 06-02-85
B 06668
2240842
SHEET 4

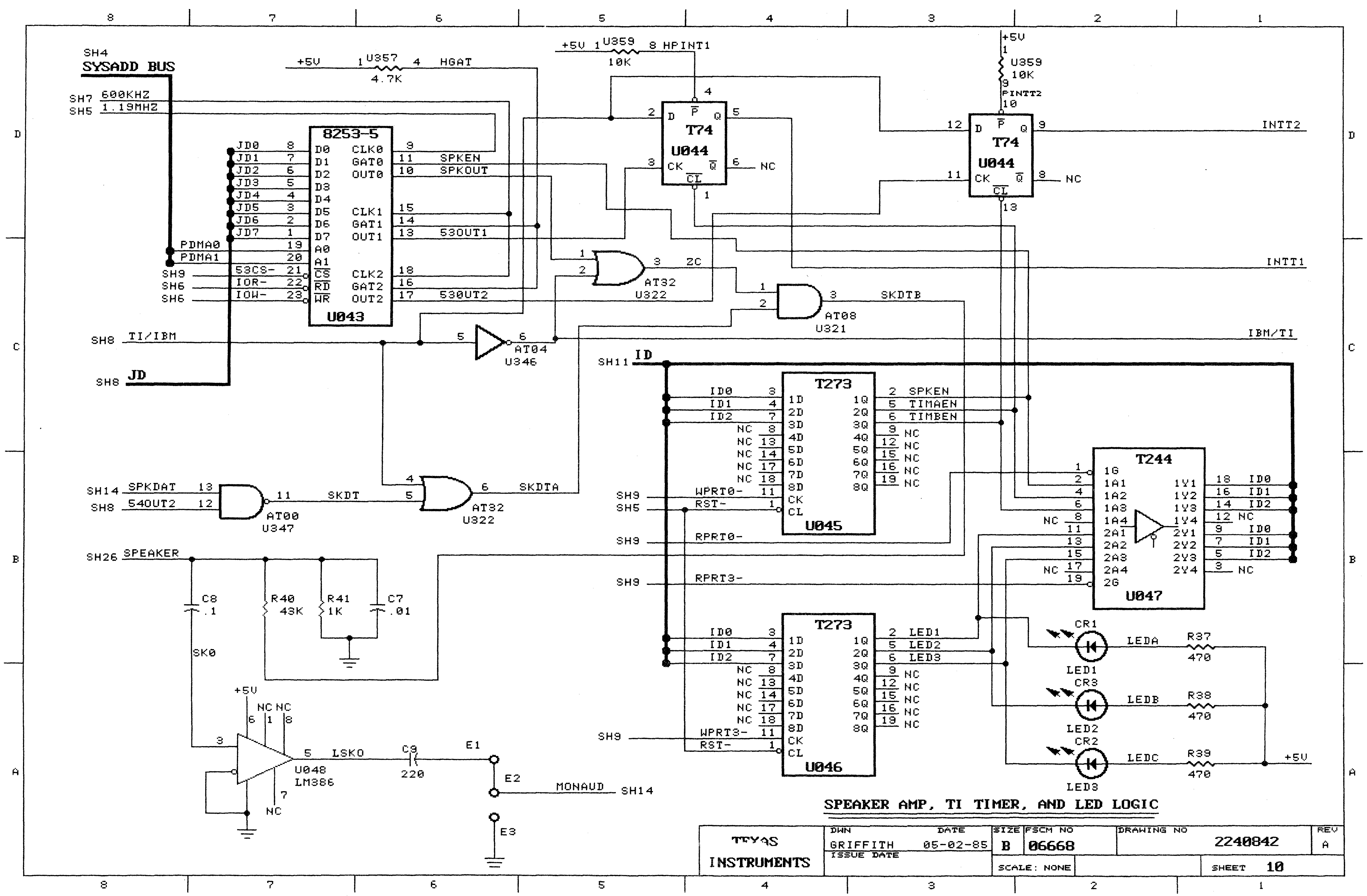

SYSTEM CLOCKS PAGE
TEXAS INSTRUMENTS
DWN WHEELER
DATE 06-20-85
SIZE B
FSCM NO 06668
DRAWING NO 2240842
REV A
SCALE: NONE
SHEET 5
CLK1.JED

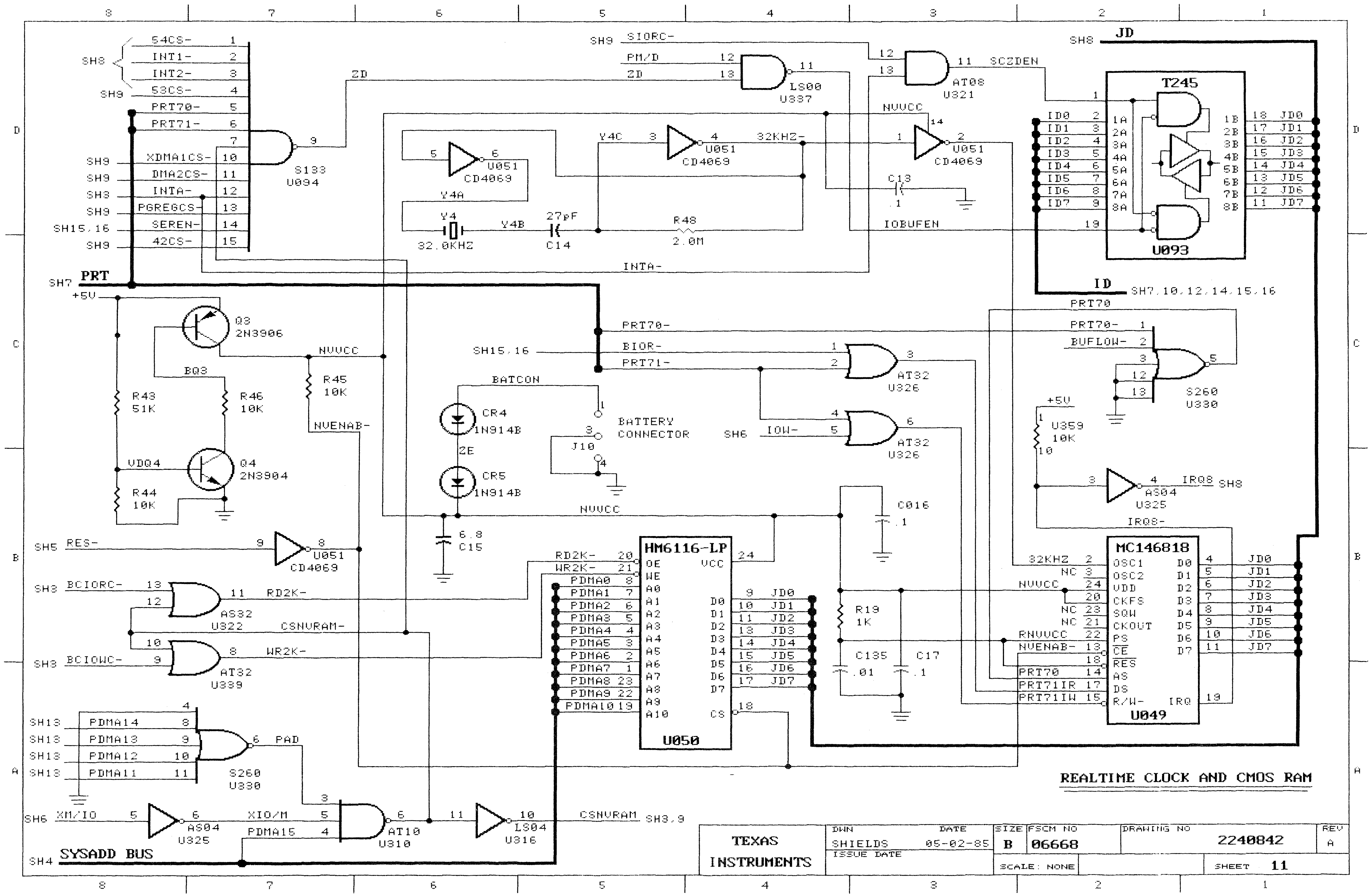

COPROCESSOR LOGIC AND
WAIT STATE CONTROL
PAL16R6
U060
80287
U059
DATA BUS
SYSADD BUS
LS163
U98
T74
U342
AT74
U309
AS74
U97
TEXAS
INSTRUMENTS
DWN
GRIFFITH
DATE
06-02-85
ISSUE DATE
SIZE
B
FSCM NO
06668
DRAWING NO
2240842
REV
A
SCALE: NONE
SHEET 6


RESET AND NMI LOGIC
AS74
U075
T74
U062
T74
U062
T163
U064
T74
U063
T74
U063
TL7705A
U065
MEMADD BUS
ID
SOFTRES
SRES
RBNMI
RES-
NMIMASK
NMI
ENNMI
NNMI
CLENPA
RCLENPA
PRESET
NMI-
XNMIEN
PINT-
RST-
PRT70-
CLNMIMSK
600KHZ
300KHZ
1.19MHZ
SFTRST-
M/IO
MA1
MS0
MS1
PD
CTRES
REFRES
LBOD
RESET
TEXAS INSTRUMENTS
Digital Systems Group
B 06668
2240842
SHEET 7

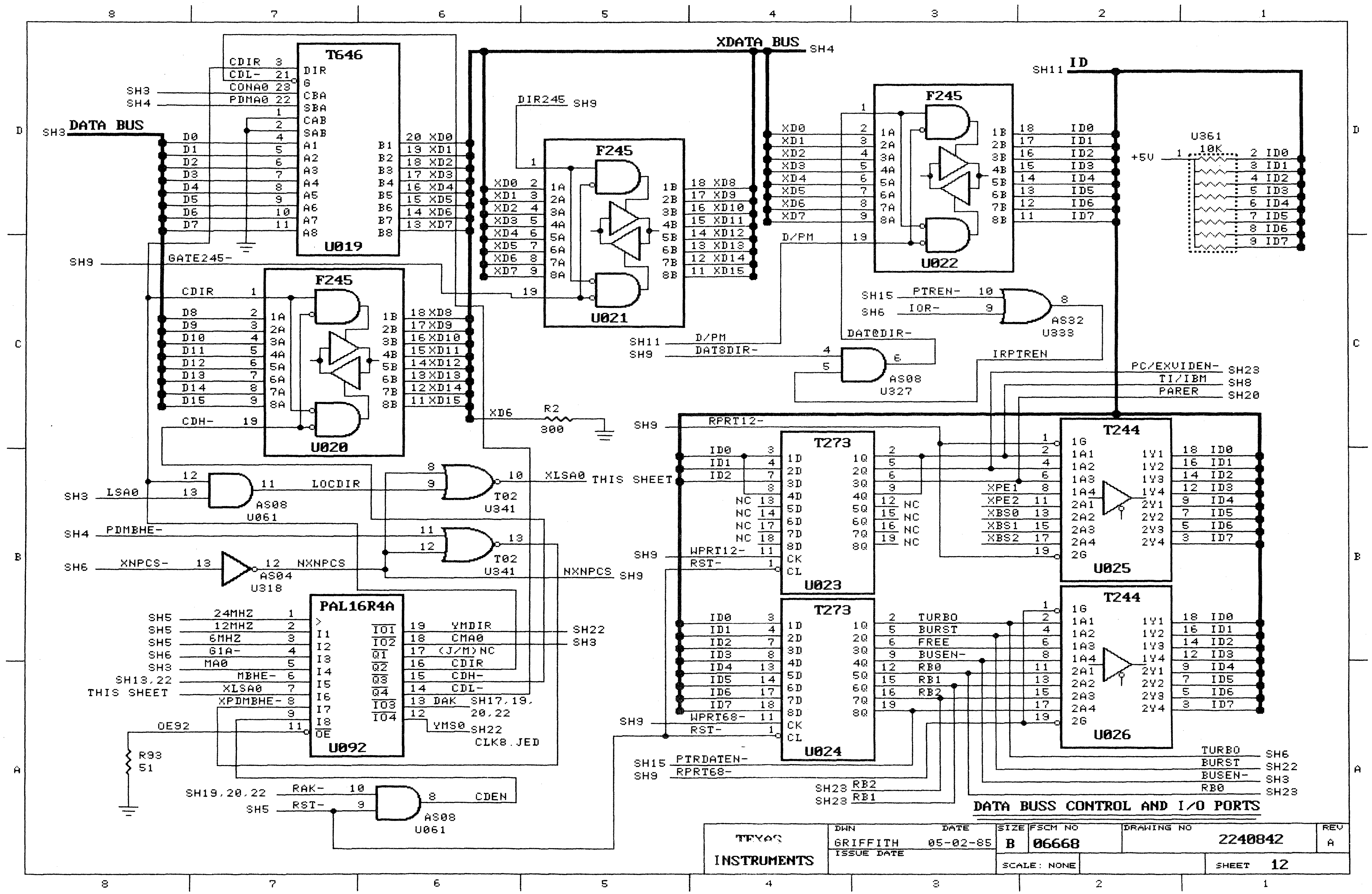

INTERUPT BUS
SYSADD BUS
T257
U028
U029
8259A
U031
U032
8254
U030
INTERUPT CONTROLLERS AND TIMER
TEXAS INSTRUMENTS
GRIFFITH
5-2-85
06668
2240842
SCALE: NONE
SHEET 8

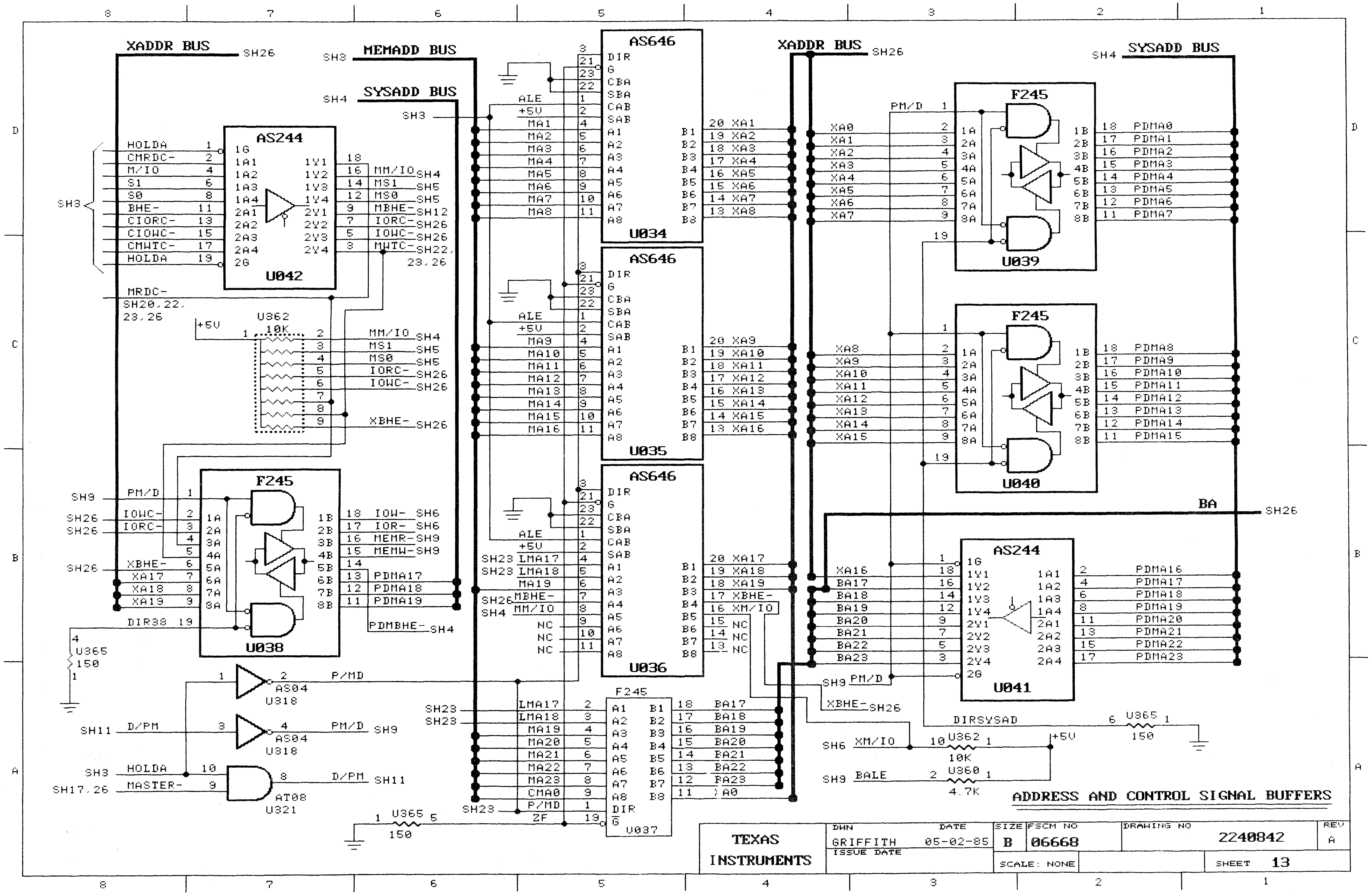

SYSADD BUS
PRT
AT138
U053
PAL16L8
U054
PAL16L8
U055
PAL16L8A
U056
AT74
U306
U359
10K
+5V
PDMA5
PDMA6
PDMA7
PM/D
PDMA8
PDMA9
DMA1CS-
INTR1CS-
54CS-
PPICS-
PGREGCS-
INT2-
DMA2CS-
CS287-
TI/IBM
IOR-
IOW-
MEM16-
G1A-
TIVID-
ROMCS-
F16+
MM/IO
F16/MIO
ALE
ALE-
CMDLY
ADD
IO16-
AEN1-
AEN2-
BCIOWC-
6MHZ-
RST-
BCIORC-
12BWC
SIORC-
NC
XDMA1CS-
PRT0-
PRT3-
PRT12-
53CS-
INT1-
42CS-
42C/D-
U54.JED
BUSVCLR-
PRT61-
PRT68-
PRT70-
PRT71-
DAT8DIR-
RST287-
NPCS-
U55.JED
CSNVRAM
NXNPCS
DATA01
DATACON-
INTA-
XM/IO
FSYS16+
SIOWC-
MEMR-
MEMW-
DIR245
GATE245-
Q1
DMAEN-
PDMA0
PDMBHE-
ENDCYC-
U56.JED
RPRT0-
WPRT0-
RPRT3-
WPRT3-
RPRT12-
WPRT12-
RPRT61-
WPRT61-
RPRT68-
WPRT68-
AT32
U057
U058
U328
U339
AT08
U332
AS20
U329
AT02
U350
AS00
U312
AS08
U303
I/O DECODES PAGE
TEXAS INSTRUMENTS
DWN GRIFFITH
DATE 05-02-85
ISSUE DATE
SIZE B
FSCM NO 06668
DRAWING NO 2240842
REV A
SCALE: NONE
SHEET 9

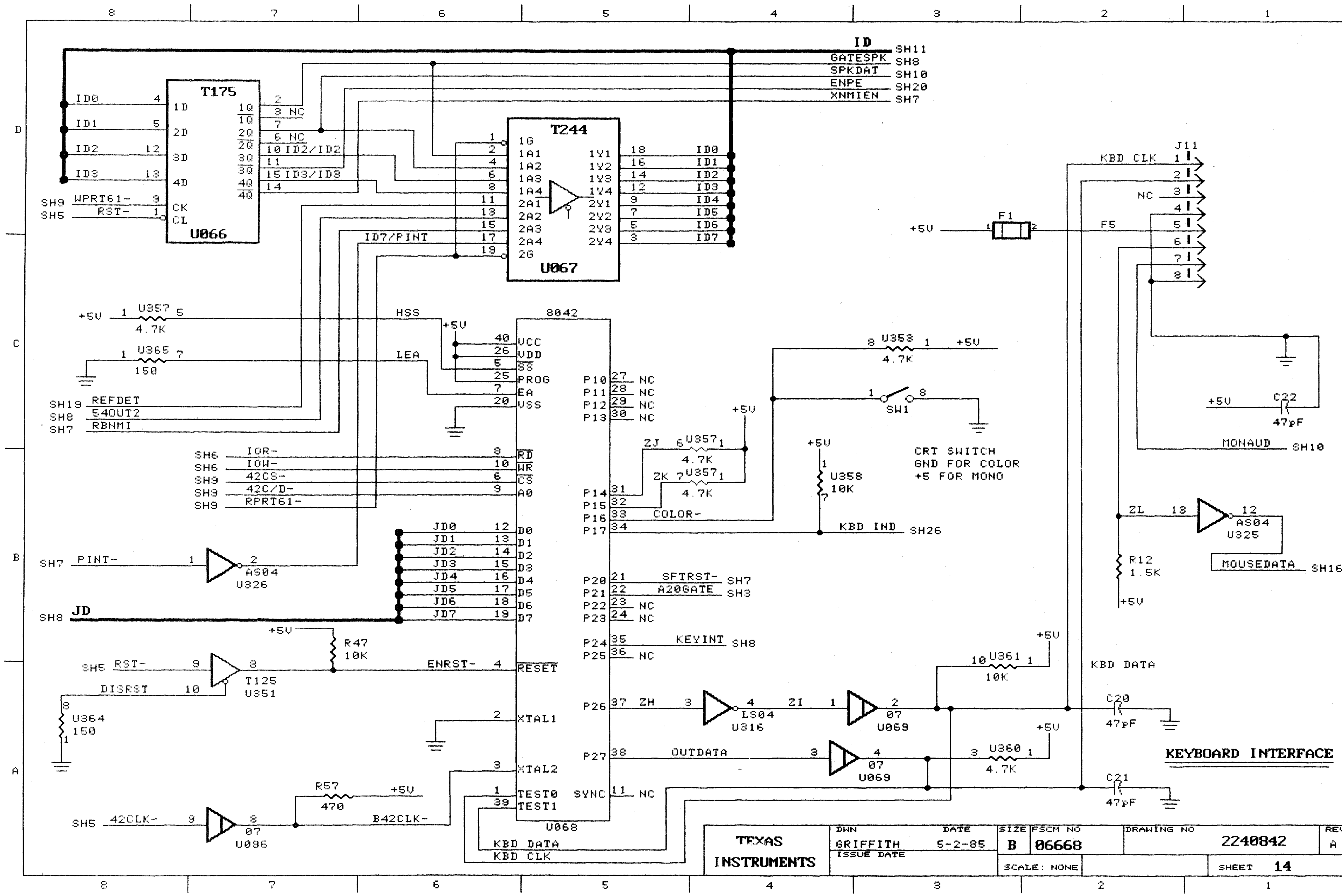

SH4
SYSADD BUS
SH7 600KHZ
SH5 1.19MHZ
+5V U357 4.7K HGAT
+5V U359 10K HPINT1
+5V U359 10K PINTT2
8253-5
U043
D0 D1 D2 D3 D4 D5 D6 D7 A0 A1 CS RD WR
CLK0 GAT0 OUT0 CLK1 GAT1 OUT1 CLK2 GAT2 OUT2
JD0 JD1 JD2 JD3 JD4 JD5 JD6 JD7
PDMA0 PDMA1
SH9 53CS-
SH6 IOR-
SH6 IOW-
SPKEN
SPKOUT
53OUT1
53OUT2
T74
U044
INTT2
INTT1
AT32 U322
2C
AT08 U321
SKDTB
SH8 TI/IBM
AT04 U346
IBM/TI
SH8 JD
SH11 ID
T273
U045
ID0 ID1 ID2
SPKEN TIMAEN TIMBEN
SH9 WPRT0-
SH5 RST-
SH9 RPRT0-
SH9 RPRT3-
T244
U047
SH14 SPKDAT
SH8 54OUT2
AT00 U347
SKDT
AT32 U322
SKDTA
SH26 SPEAKER
C8 .1
R40 43K
R41 1K
C7 .01
SK0
+5V
NC NC
U048 LM386
LSK0
C9 220
E1
E2
E3
MONAUD SH14
U046
SH9 WPRT3-
LED1 LED2 LED3
CR1 LED1
CR3 LED2
CR2 LED3
LEDA R37 470
LEDB R38 470
LEDC R39 470
+5V
SPEAKER AMP, TI TIMER, AND LED LOGIC
TEXAS INSTRUMENTS
DWN GRIFFITH DATE 05-02-85
ISSUE DATE
SIZE B
FSCM NO 06668
DRAWING NO 2240842
REV A
SCALE: NONE
SHEET 10

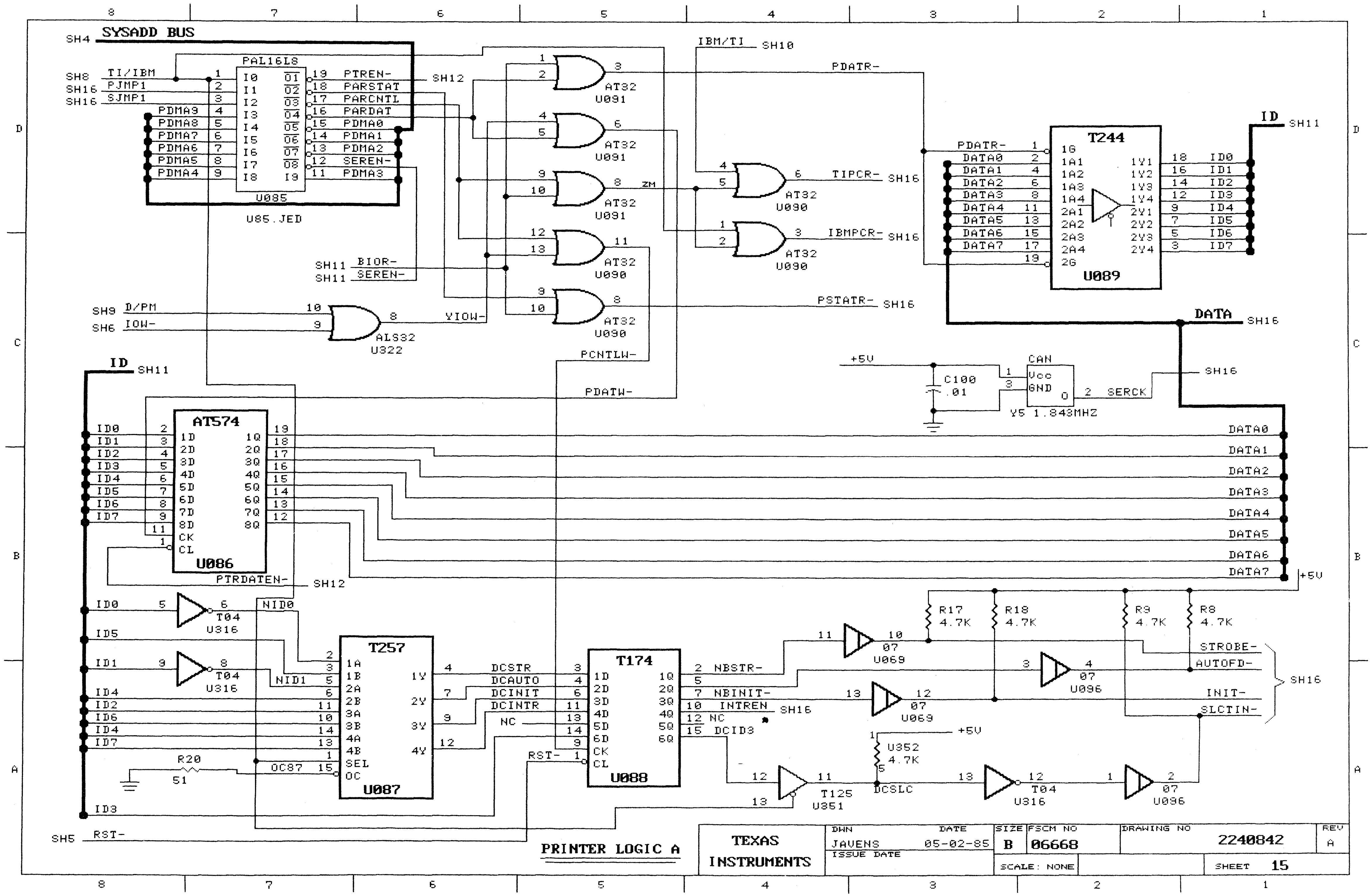


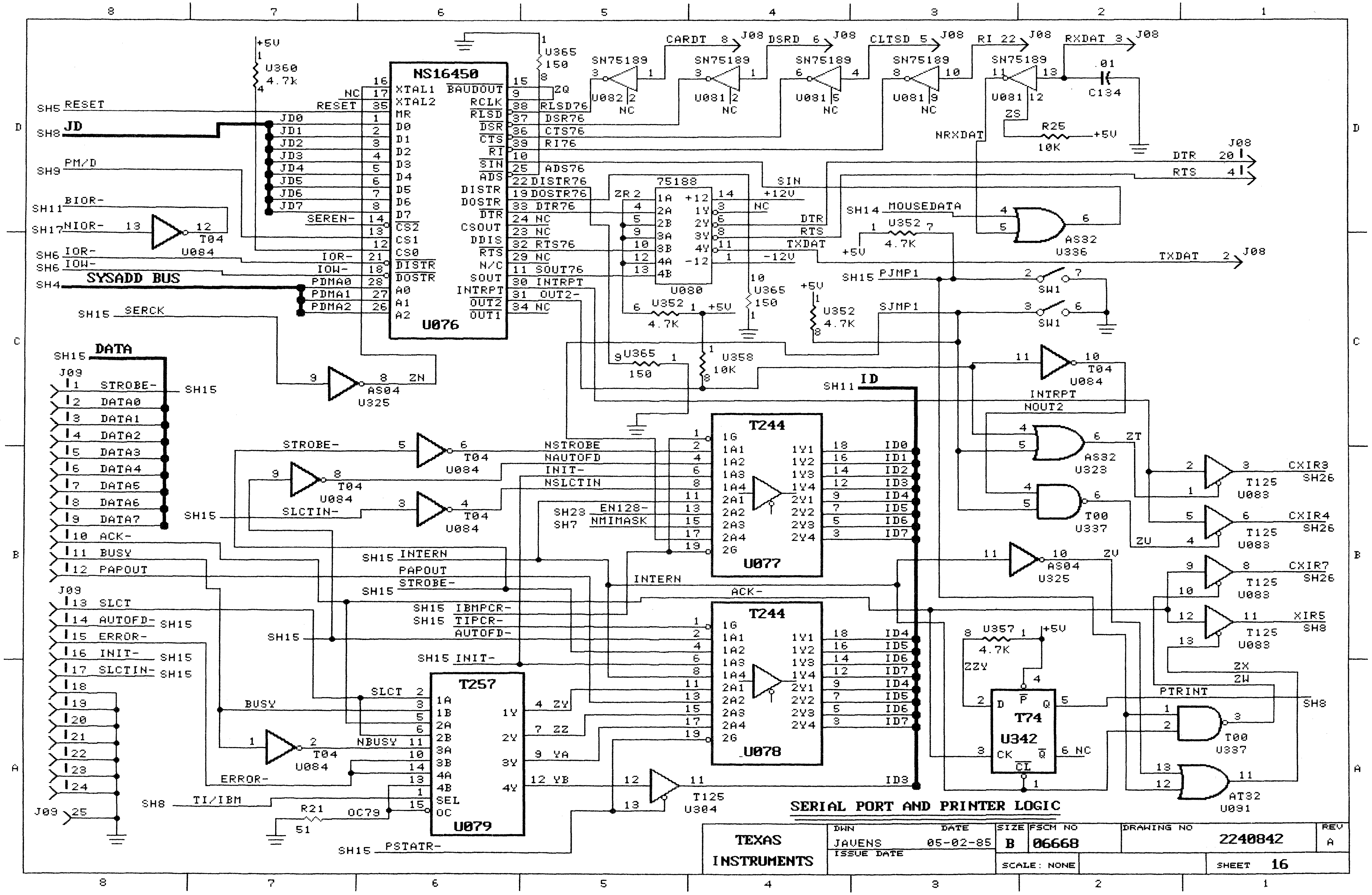
REALTIME CLOCK AND CMOS RAM
HM6116-LP
U050
MC146818
U049
T245
U093
PRT
SYSADD BUS
JD
ID
SH7,10,12,14,15,16
BATTERY CONNECTOR
J10
Q3 2N3906
Q4 2N3904
R43 51K
R44 10K
R45 10K
R46 10K
R48 2.0M
R19 1K
CR4 1N914B
CR5 1N914B
Y4 32.0KHZ
C14 27pF
C15 6.8
C016 .1
C135 .01
C17 .1
C13 .1
U051 CD4069
U094 S133
U337 LS00
U321 AT08
U326 AT32
U330 S260
U322 AS32
U339 AT32
U325 AS04
U310 AT10
U316 LS04
U359 10K
NVVCC
NVENAB-
CSNVRAM-
IOBUFEN
SCZDEN
INTA-
BATCON
IRQ8
TEXAS INSTRUMENTS
DWN SHIELDS
DATE 05-02-85
SIZE B
FSCM NO 06668
DRAWING NO 2240842
REV A
SCALE: NONE
SHEET 11

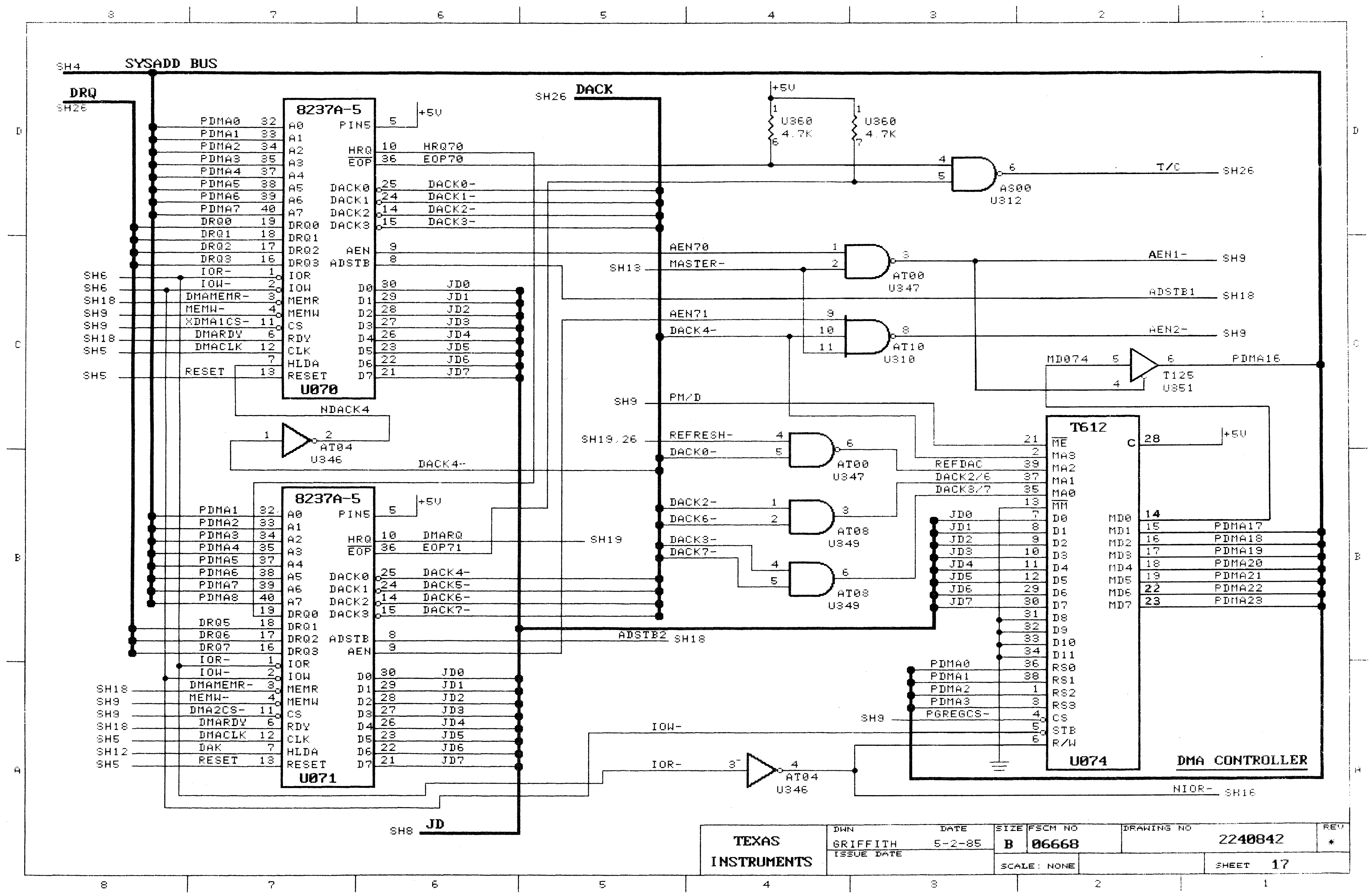

XDATA BUS
DATA BUS
ID
T646
U019
F245
U020
F245
U021
F245
U022
U361
10K
+5V
AS32
U333
AS08
U327
T273
U023
T273
U024
T244
U025
T244
U026
AS08
U061
T02
U341
AS04
U318
PAL16R4A
U092
AS08
U061
R2
300
R93
51
XLSA0 THIS SHEET
NXNPCS
DIR245
GATE245-
CDIR
CDH-
CDL-
LOCDIR
LSA0
PDMBHE-
XNPCS-
RPRT12-
WPRT12-
RPRT68-
WPRT68-
RST-
PTREN-
IOR-
DAT8DIR-
D/PM
IRPTREN
PC/EXUIDEN-
TI/IBM
PARER
TURBO
BURST
FREE
BUSEN-
RB0
RB1
RB2
PTRDATEN-
RAK-
CDEN
24MHZ
12MHZ
6MHZ
G1A-
MA0
MBHE-
XPDMBHE-
OE92
YMDIR
CMA0
(J/M) NC
DAK
YMS0
CLK8.JED
DATA BUSS CONTROL AND I/O PORTS
TEXAS INSTRUMENTS
DWN GRIFFITH
DATE 05-02-85
ISSUE DATE
SIZE B
FSCM NO 06668
DRAWING NO 2240842
REV A
SCALE: NONE
SHEET 12

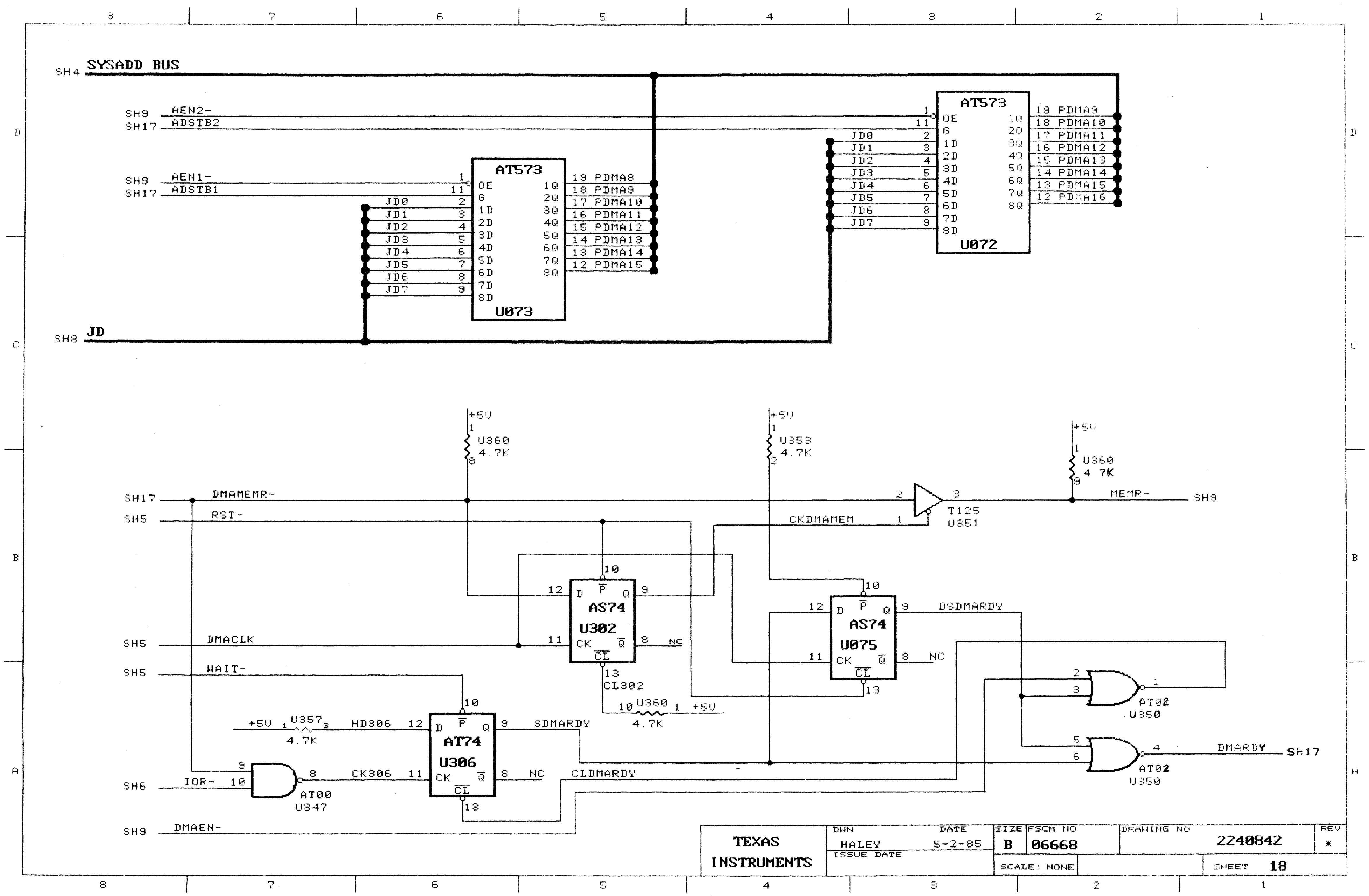

XADDR BUS
MEMADD BUS
SYSADD BUS
AS244
U042
AS646
U034
U035
U036
F245
U037
U038
U039
U040
U041
U318
U321
U362
U365
BA
ADDRESS AND CONTROL SIGNAL BUFFERS
TEXAS INSTRUMENTS
GRIFFITH
05-02-85
B
06668
2240842
SCALE: NONE
SHEET 13

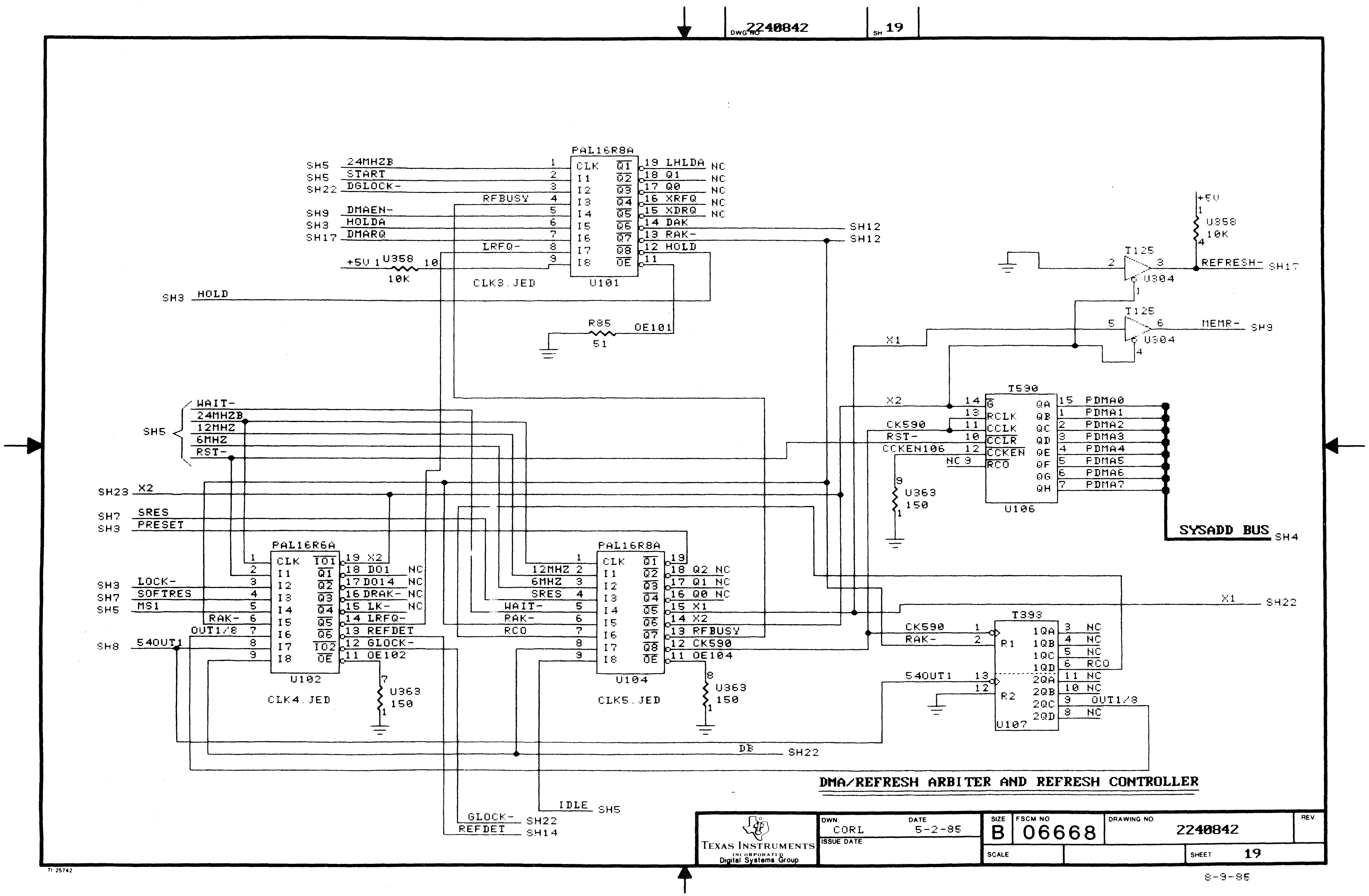

T175
U066
T244
U067
8042
U068
ID
SH11
GATESPK
SH8
SPKDAT
SH10
ENPE
SH20
XNMIEN
SH7
J11
KBD CLK
F1
+5V
F5
MONAUD
SH10
CRT SWITCH
GND FOR COLOR
+5 FOR MONO
SW1
KBD IND
SH26
MOUSEDATA
SH16
KBD DATA
KEYINT
SFTRST-
A20GATE
OUTDATA
COLOR-
PINT-
JD
RST-
DISRST
ENRST-
42CLK-
B42CLK-
REFDET
540UT2
RBNMI
IOR-
IOW-
42CS-
42C/D-
RPRT61-
WPRT61-
KEYBOARD INTERFACE
TEXAS INSTRUMENTS
DWN
GRIFFITH
DATE
5-2-85
ISSUE DATE
SIZE
B
FSCM NO
06668
DRAWING NO
2240842
REV
A
SCALE: NONE
SHEET
14

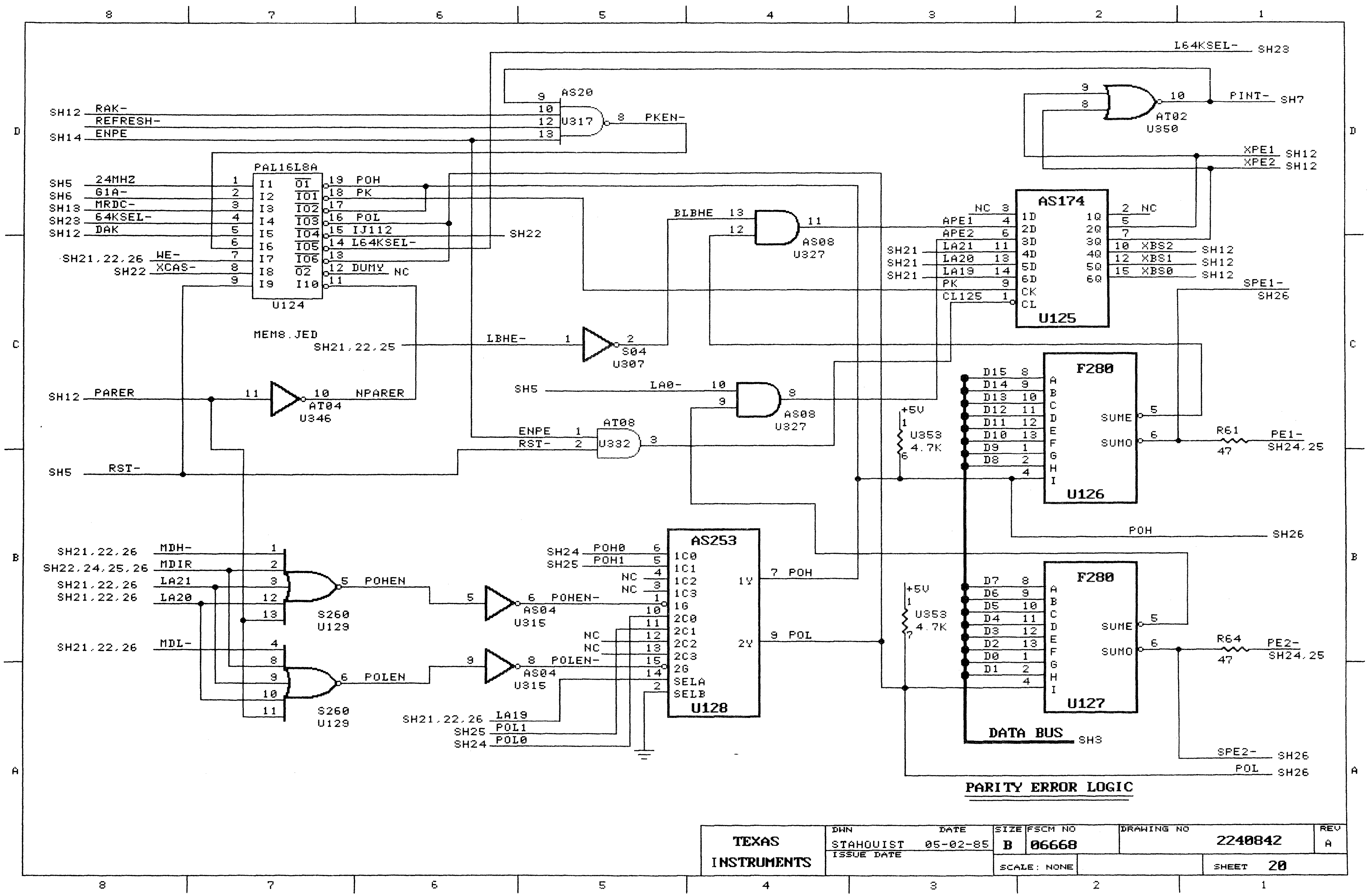

SYSADD BUS
PAL16L8
U085
U85.JED
AT32
U091
U090
ALS32
U322
T244
U089
AT574
U086
T257
U087
T174
U088
T04
U316
07
U069
U096
T125
U351
U352
4.7K
R17
R18
R9
R8
R20
51
C100
.01
CAN
Y5 1.843MHZ
IBM/TI
PDATR-
TIPCR-
IBMPCR-
PSTATR-
PCNTLW-
PDATW-
PTRDATEN-
DATA
ID
SERCK
DCSTR
DCAUTO
DCINIT
DCINTR
NBSTR-
NBINIT-
INTREN
DCID3
DCSLC
STROBE-
AUTOFD-
INIT-
SLCTIN-
RST-
PRINTER LOGIC A
TEXAS INSTRUMENTS
DWN JAVENS
DATE 05-02-85
SIZE B
FSCM NO 06668
DRAWING NO 2240842
REV A
SCALE: NONE
SHEET 15

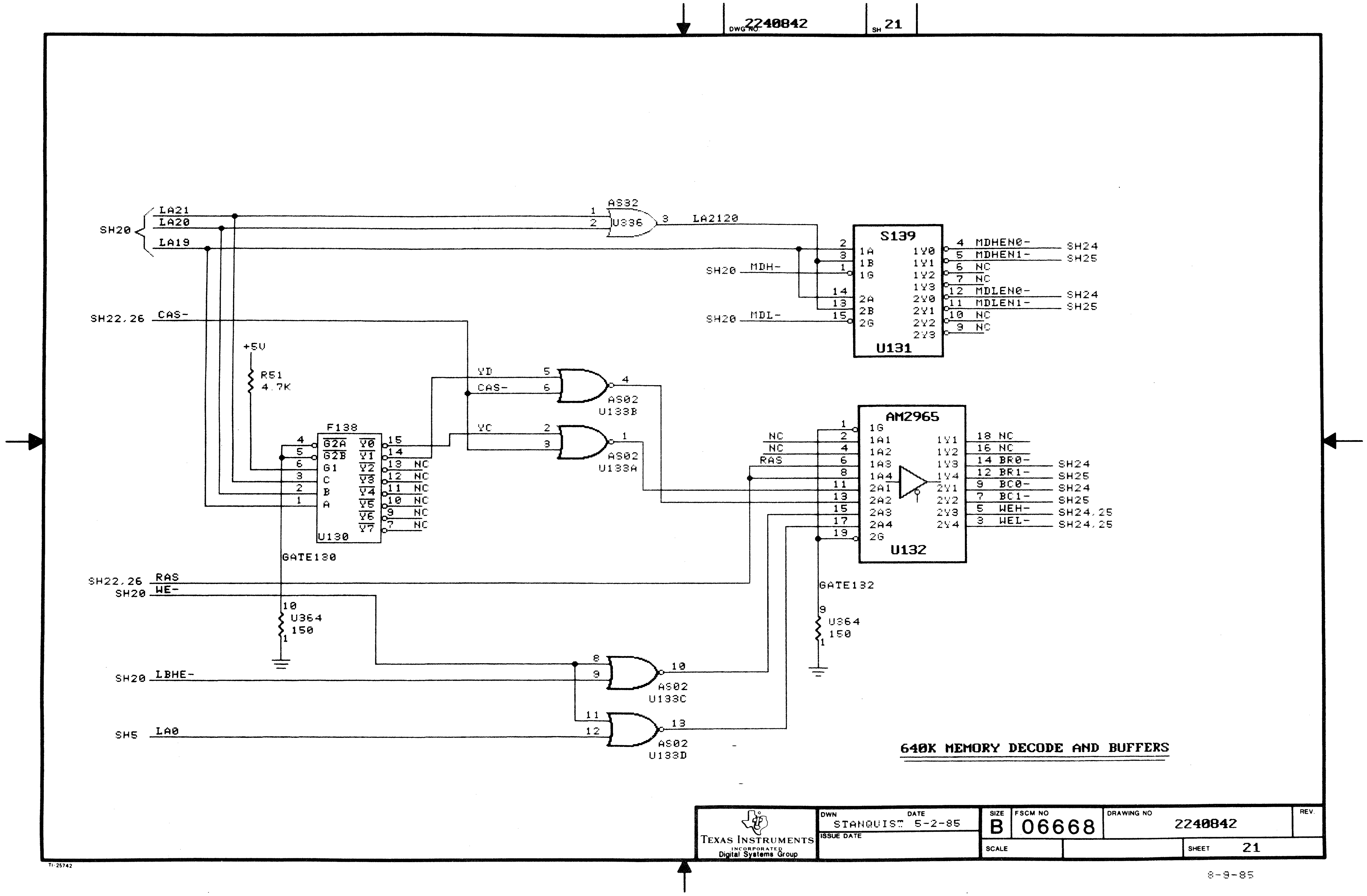

NS16450
U076
75188
U080
SN75189
U082
U081
T244
U077
U078
T257
U079
T74
U342
AS32
U336
U323
T00
U337
T04
U084
AS04
U325
T125
U083
U384
AT32
U091
SYSADD BUS
DATA
ID
JD
C134
R25
R21
SW1
SERIAL PORT AND PRINTER LOGIC
TEXAS INSTRUMENTS
JAVENS
05-02-85
B
06668
2240842
A
SCALE: NONE
SHEET 16

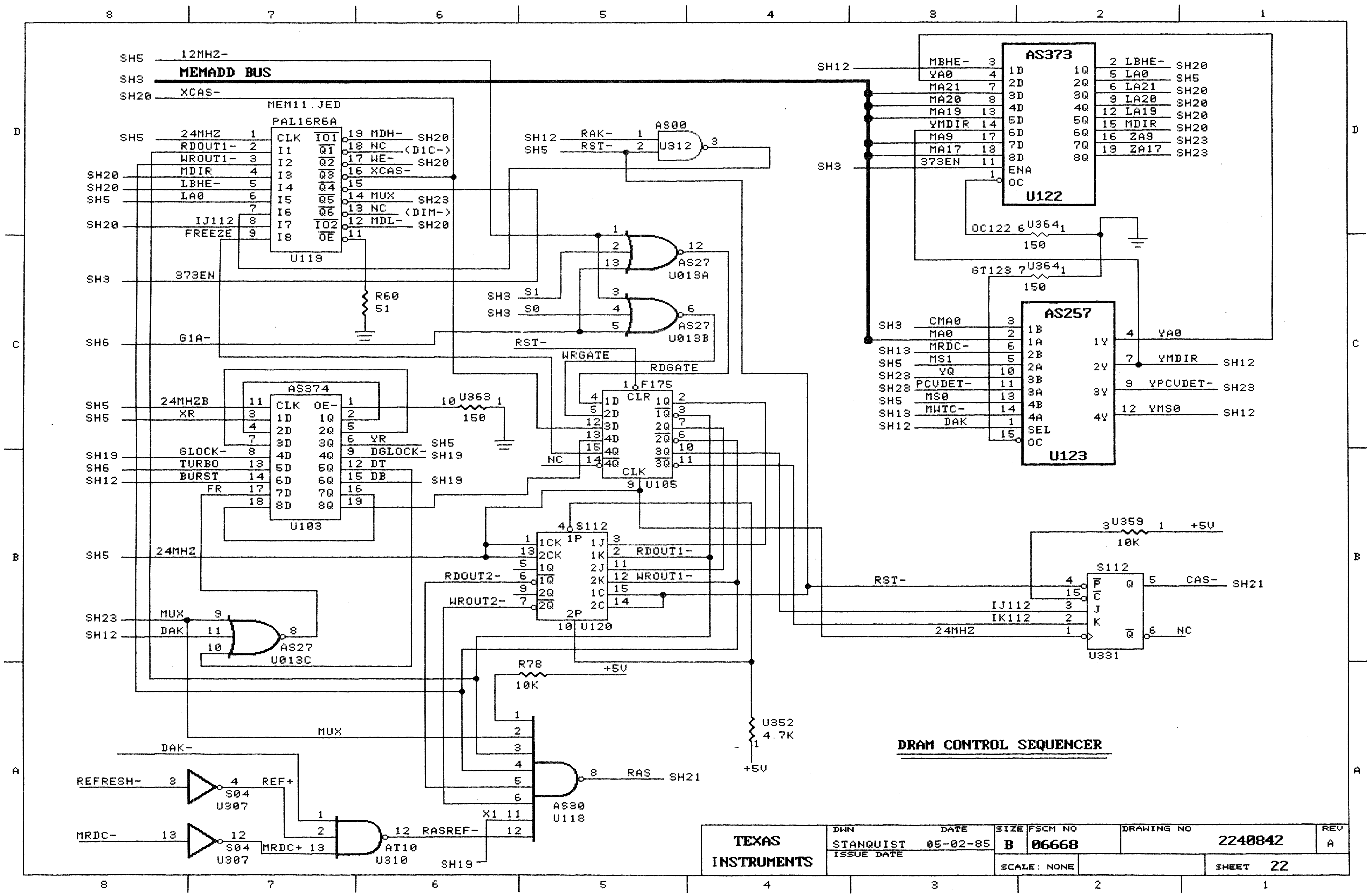

SYSADD BUS
DRQ
DACK
8237A-5
U070
U071
T612
U074
DMA CONTROLLER
JD
TEXAS INSTRUMENTS
GRIFFITH
5-2-85
B
06668
2240842
SHEET 17

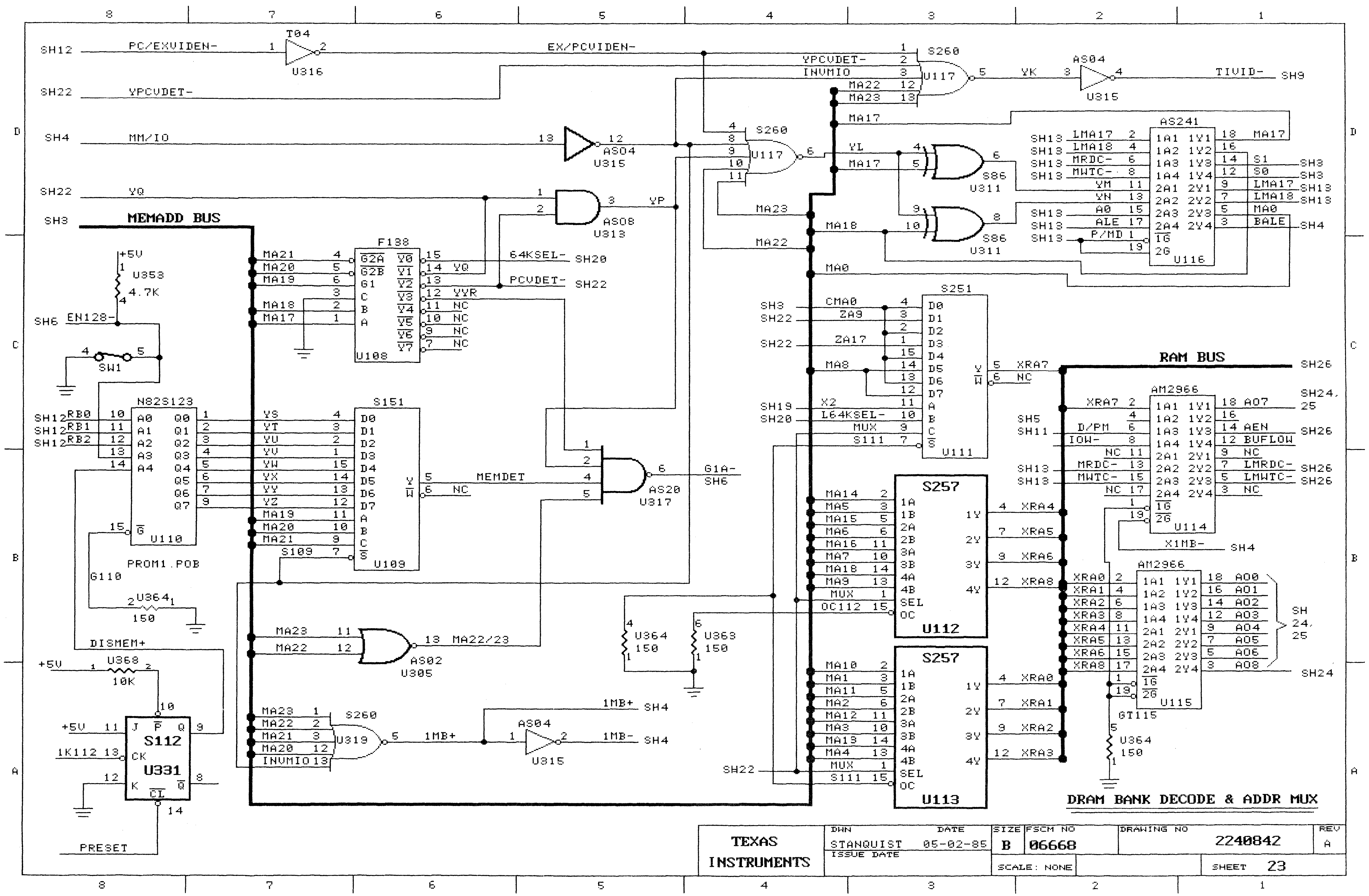

SYSADD BUS
JD
AT573
U073
U072
AS74
U302
U075
AT74
U306
AT00
U347
AT02
U350
T125
U351
DMAMEMR-
RST-
DMACLK
WAIT-
IOR-
DMAEN-
MEMR-
CKDMAMEM
DSDMARDY
SDMARDY
CLDMARDY
DMARDY
TEXAS INSTRUMENTS
HALEY
5-2-85
06668
2240842
SHEET 18

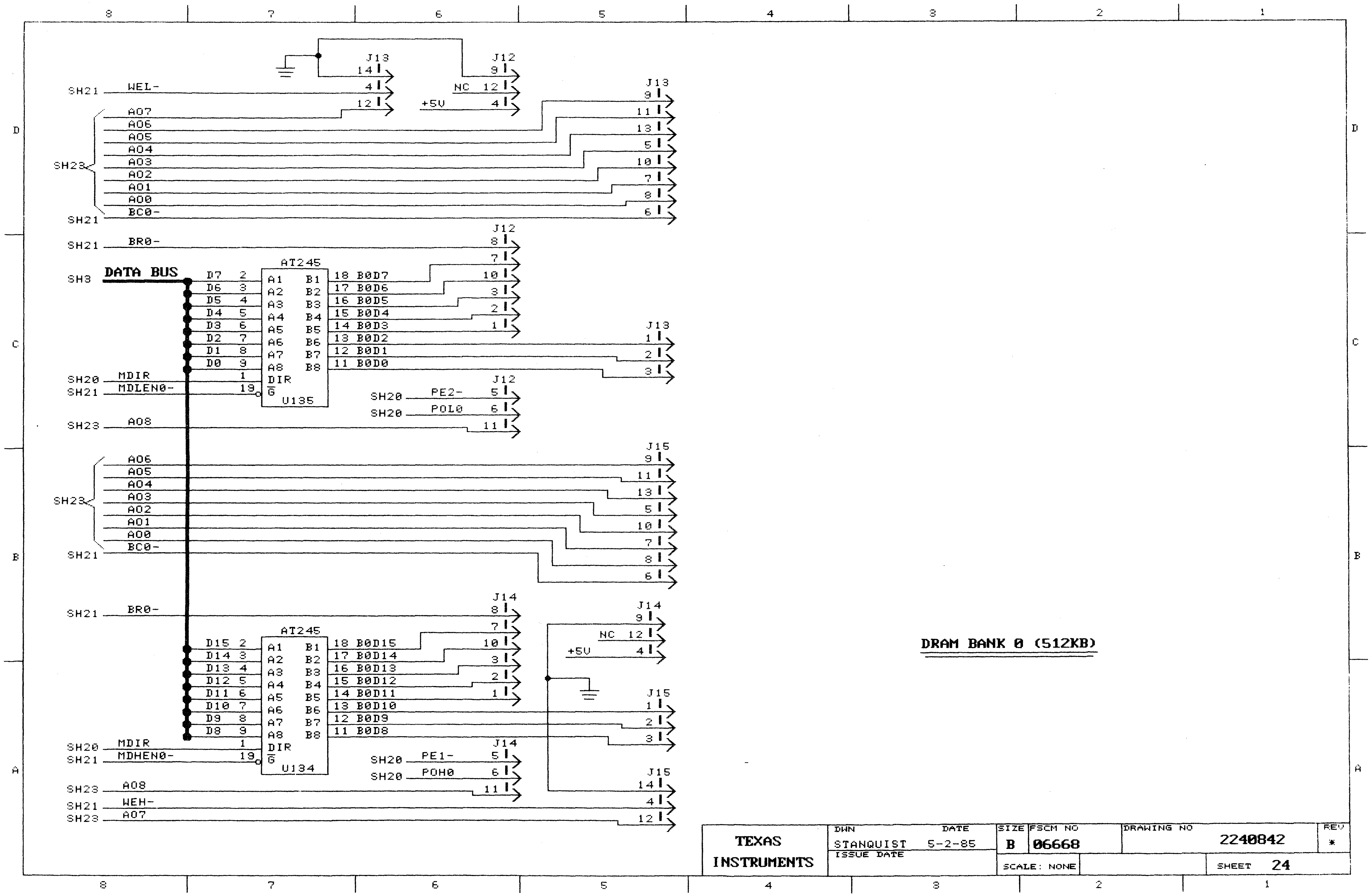

DMA/REFRESH ARBITER AND REFRESH CONTROLLER
SYSADD BUS
Texas Instruments
Digital Systems Group
DWN CORL
DATE 5-2-85
SIZE B
FSCM NO 06668
DRAWING NO 2240842
SHEET 19
8-9-85

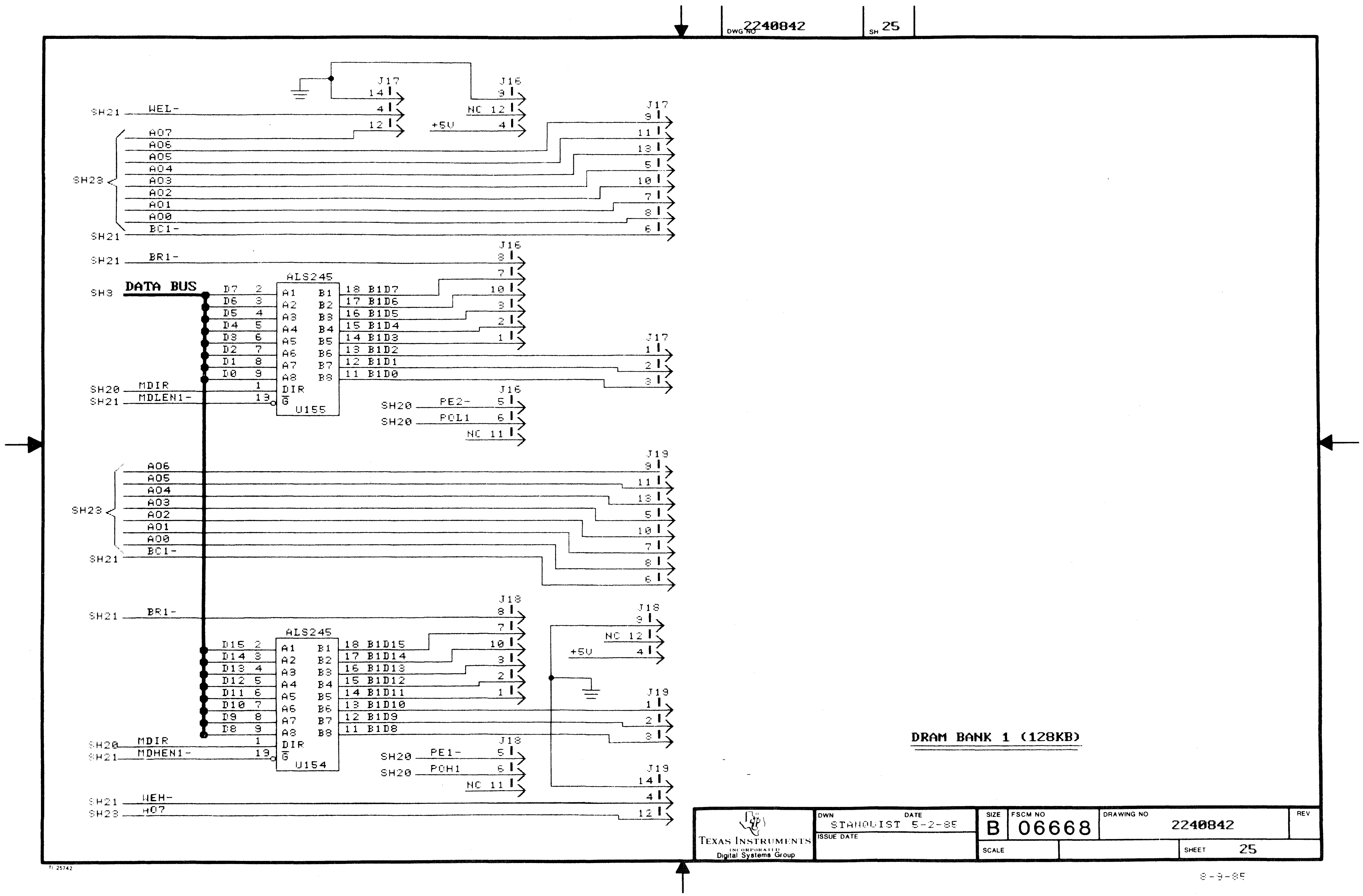

PARITY ERROR LOGIC
TEXAS INSTRUMENTS
DWN STAHOUIST DATE 05-02-85
SIZE B FSCM NO 06668
DRAWING NO 2240842
REV A
SCALE: NONE
SHEET 20
PAL16L8A
U124
MEM8.JED
AS174
U125
F280
U126
U127
AS253
U128
DATA BUS

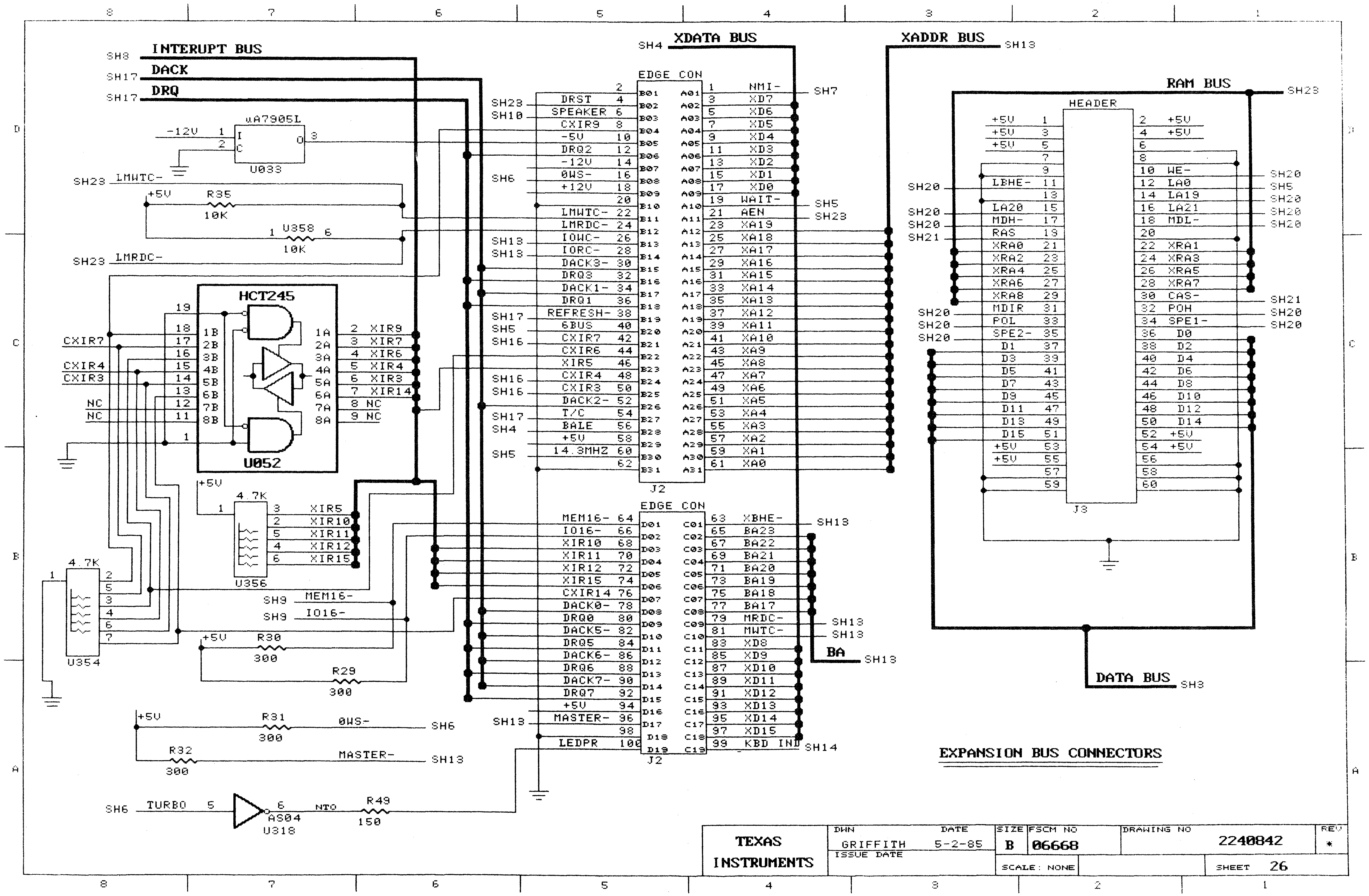

2240842
21
SH20
LA21
LA20
LA19
AS32
U336
LA2120
S139
U131
MDH-
MDL-
MDHEN0-
MDHEN1-
MDLEN0-
MDLEN1-
SH24
SH25
SH22,26
CAS-
+5V
R51
4.7K
F138
U130
GATE130
AS02
U133B
U133A
U133C
U133D
AM2965
U132
RAS
WE-
LBHE-
SH5
LA0
BR0-
BR1-
BC0-
BC1-
WEH-
WEL-
SH24,25
GATE132
U364
150
NC
640K MEMORY DECODE AND BUFFERS
TEXAS INSTRUMENTS
Digital Systems Group
STANQUIST 5-2-85
B
06668
2240842
SHEET 21
8-9-85


DRAM CONTROL SEQUENCER
TEXAS INSTRUMENTS
STANQUIST 05-02-85
B 06668
2240842
SHEET 22


MEMADD BUS
RAM BUS
PC/EXVIDEN-
EX/PCVIDEN-
VPCVDET-
INVMIO
MM/IO
VQ
VP
VK
TIVID-
MEMDET
G1A-
EN128-
+5V
U353
4.7K
SW1
N82S123
PROM1.POB
U110
F138
U108
S151
U109
S260
U117
U319
AS04
U315
U316
AS08
U313
AS20
U317
AS02
U305
MA22/23
S86
U311
AS241
U116
S251
U111
S257
U112
U113
AM2966
U114
U115
S112
U331
U368
10K
U364
U363
150
DISMEM+
PRESET
1MB+
1MB-
64KSEL-
PCVDET-
XRA7
X1MB-
DRAM BANK DECODE & ADDR MUX
TEXAS INSTRUMENTS
DWN STANQUIST
DATE 05-02-85
ISSUE DATE
SIZE B
FSCM NO 06668
DRAWING NO 2240842
REV A
SCALE: NONE
SHEET 23


J13
J12
SH21 WEL-
NC
+5V
SH23
A07
A06
A05
A04
A03
A02
A01
A00
SH21 BC0-
SH21 BR0-
SH3 DATA BUS
AT245
U135
SH20 MDIR
SH21 MDLEN0-
SH20 PE2-
SH20 POL0
SH23 A08
J15
AT245
U134
SH20 MDIR
SH21 MDHEN0-
SH20 PE1-
SH20 POH0
SH21 WEH-
J14
DRAM BANK 0 (512KB)
TEXAS INSTRUMENTS
DWN STANQUIST DATE 5-2-85
ISSUE DATE
SIZE B
FSCM NO 06668
DRAWING NO 2240842
REV *
SCALE: NONE
SHEET 24


DRAM BANK 1 (128KB)
DATA BUS
ALS245
U155
U154
TEXAS INSTRUMENTS
Digital Systems Group
STANDQUIST 5-2-85
B
06668
2240842
SHEET 25


INTERUPT BUS
DACK
DRQ
XDATA BUS
XADDR BUS
RAM BUS
HEADER
HCT245
U052
EDGE CON
J2
J3
BA
DATA BUS
EXPANSION BUS CONNECTORS
TEXAS INSTRUMENTS
DWN GRIFFITH DATE 5-2-85
SIZE B FSCM NO 06668
DRAWING NO 2240842
SHEET 26
SCALE: NONE

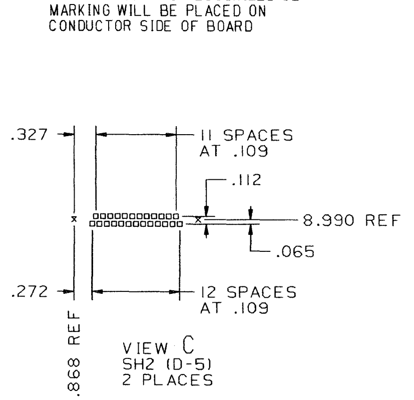
DWG NO 2240841 SH 1

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	ECN 526815 (E) K.MOORE 2-11-85	2-12-85	A.VENEGAS
	FORMAL RELEASE		
B	ECN530674 (D) F.ESPINOZA 2-11-85 THIS REV NOT GERBERED	3-14-85	VENEGAS
C	ECN534912 (C) F.PETERSON 4-08-85 THIS REV NOT GERBERED	4-8-85	MILLER
D	ECN538659 (E) D.SELVIDGE 5-05-85	5-6-85	MILLER
E	ECN549544 (E) SELVIDGE 6-6-85	6-7-85	VENEGAS
F	ECN532523 (E) SELVIDGE 10-7-85	10/14/85	[signature] for F.V.

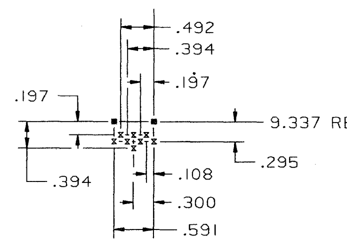
NOTES: UNLESS OTHERWISE SPECIFIED:

1. REGISTRATION MARKS ON ITEM 2 TO BE USED FOR POSITIONING MARKING AT HOLES SHOWN.
2. MINIMUM COPPER WALL THICKNESS .001.
3. TOOLING DIMENSIONS.
4. MARK PER PROCESS 6, HEIGHT TO BE CONTROLLED BY ITEM 2.
5. ALL HOLES LOCATIONS NOT DIMENSIONED ARE ON .025 GRID INCREMENTS IN RELATION TO DATUM 0.
6. ALL HOLES ARE WITHIN .014 TRUE POSITION OF DATUM 0, WHEN PINNED TO PLANE A
7. HOLE TOLERANCE +.006 -.002
8. ~~SOLDER MASK SHALL BE APPLIED TO CONDUCTOR SIDE OF BOARD PER PROCESS 4. INTERNAL INDEXING HOLES MAY BE USED FOR POSITIONING.~~
9. PLATE ENTIRE CONDUCTOR AREA ON BOTH SIDES OF BOARD PER PROCESS 1
10. THE MAXIMUM PERMISSIBLE WARP AND TWIST SHALL BE .015 PER INCH
11. INTERNAL AND EXTERNAL CORNERS TO BE .06 RADIUS MAX AT SHOP OPTION
12. MANUFACTURER'S RECOGNIZED UL MARKING WILL BE PLACED ON CONDUCTOR SIDE OF BOARD
13. MARK APPROPRIATE REVISION LETTER PER PROCESS 5 OR 7 IN SPACE PROVIDED BY ITEM 2. (FARSIDE)
14. FINISHED BOARD SHALL MEET UL 94V-1 FLAMMABILITY RATING AND BE MARKED WITH THE REQUIRED UL CODE NUMBER
15. ~~PLUG IN CONNECTOR TABS TO BE ELECTROPLATED PER PROCESS 2 AND 3 ON BOTH SIDES OF THE BOARD FROM BOARD EDGE TO DIMENSION SHOWN~~
16. DESIGN MEETS ITEM 3, EXCEPT:
    A. TERMINAL AREAS NOT RELIEVED FROM PLANE AREAS.
    ~~B. FINE LINE SPACING BETWEEN .100 CENTERS AND WIDTHS~~
    ~~C. SPACING BETWEEN CONDUCTORS AND LINE WIDTH 8 MILS (.008) ALL LAYERS~~
    D. CONDUCTOR TO BOARD EDGE SPACING IS .070 ON INTERNAL LAYERS
17. ~~FINISHED BOARD SHALL MEET THE REQUIREMENTS OF ITEM 3, EXCEPT: A. NON-PLATED THRU HOLES TO BOARD EDGE SPACING CHECKS .034.~~
18. THICKNESS SELECTED AT FABRICATION TO MEET THE TOTAL BOARD THICKNESS SPECIFIED ON THIS DRAWING.
19. BOARDS TO BE ELECTRICALLY TESTED
20. PLATING SHOP OPTION
21. BAR CODE MAY BE PLACED IN SPACE PROVIDED BY ITEM 2 AT NEXT ASSEMBLY.
22. MASK OFF REGISTRATION MARKS BEFORE SCREENING.
23. FINE-LINE DESIGN
24. SUPPLIER SHALL MARK INDIVIDUAL BOARDS FOR TRACEABILITY. RUN/LOT OR DATE/CODE MARKING IS ACCEPTABLE.
25. HOLE TOLERANCE +.004,-.002 APPLIES TO COPPER PLATED HOLE

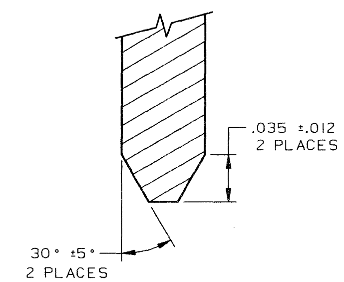
REVISION LEVEL CONTROL						
THIS DRAWING	A	B	C	D	E	F
MARKING	A	B	C	D	D	F
CONTINUITY TEST (19)	A	B	C	D	D	F
PROFILE	A	A	C	D	D	D
HOLE CONFIGURATION DRILL DECK	A	B	C	D	E	F
LAYER 1 (COMP SIDE)	A	B	C	D	E	F
LAYER 2	A	B	C	D	D	F
LAYER 3	A	B	C	D	D	F
LAYER 4	A	B	C	D	D	F
LAYER 5	A	B	C	D	D	F
LAYER 6	A	B	C	D	E	F
LAYER 7	A	B	C	D	D	F
LAYER 8 (COND SIDE)	A	B	C	D	D	F



VIEW C
SH2 (D-5)
2 PLACES



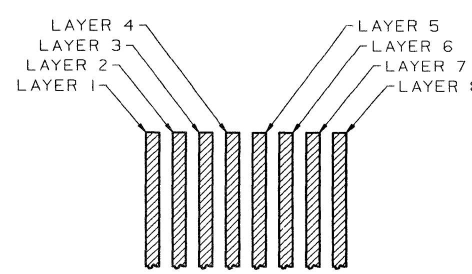
VIEW B
SH2 (C-3)



SECTION A-A
SH2 (D-6)
SCALE 20/1
ROTATED 90°

Notes	SYM	FINISHED HOLE DIAMETER: UNSUPPORTED	FINISHED HOLE DIAMETER: PLATED THRU +.007 -.003 (2)	REMARKS
	⌑	----	SHOP OPTION	DRILL ALIGNMENT
	○	----	.039	"F" COUPON
	✳	----	.025	TEST COUPON
16A	△	----	.025	
	◇	----	.029	
25	⧄	----	.033	
7 6	Y	----	.035	
7 6	+	----	.039	
7 6	X	----	.039	
16A	□	----	.046	
	⧖	----	.055	
16A	Z	----	.080	
	⧗	----	.125	
	⊠	SHOP OPTION	.126	EXTERNAL INDEXING
16A	⇧	----	.177	
20 7 6	✡	----	.187	INTERNAL INDEXING
	⊞	.058±.003	----	
	⊛	.094±.003	----	
	※	.152±.004	----	
	⩕	.234±.005	----	

TABLE OF LAYERS			
NO	DESCRIPTION	REMARKS	COPPER WT
L1	TOP LAYER	PADS/ROUTING	1 OZ
L2	SIGNAL	ROUTING	1 OZ
L3	GND	PLANE	1 OZ
L4	SIGNAL	ROUTING	1 OZ
L5	SIGNAL	ROUTING	1 OZ
L6	+5V	PLANE	1 OZ
L7	SIGNAL	ROUTING	1 OZ
L8	BOTTOM LAYER	PADS/ROUTING	1 OZ



SECTION D-D
SH2 (B-2)
SCALE NONE

-1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION	NOTES
REF	5	981001	END PRODUCT SPECIFICATION		
AR	4	802780	GLASS CLOTH, IMPREGNATED RESIN (B STAGE)		
REF	3	981003	PWB SPECIFICATION, TYPE III, CLASS B		16
REF	2	2240841	MASTER PATTERN AW		1,4,13,21
AR	1	802779	1 OZ CU CL FR 4 UL APPROVED		14

PARTS LIST

SEQ NO	PROCESS IDENT	PROCESS F-SPEC	CLASSIFICATION NO	CLASSIFICATION ADDITIONAL	NOTES
7	MARK	914-01	00	HGT .09, CLR BLK	13
6	MARK	901-01	00	CLR WHT,USING ITEM 2 (CAT 5)	4
5	MARK	903-01	01	HGT .09, CLR BLK (CAT 5)	13
~~4~~	~~SLDRM~~	~~IPC-SM-840~~	~~02~~	~~TYPE A, CLR GRN, USING ITEM 2~~	~~8~~
~~3~~	~~GLDPL~~	~~39-02~~	~~19~~	~~THICKNESS .00003 MIN~~	~~15~~
~~2~~	~~NKLPL~~	~~42-02~~	~~00~~	~~THICKNESS .0002 MIN~~	~~15~~
1	TINLD	10-00	00	THICKNESS .0003 MIN REFLOWED	9

PROCESSES—FOR CORRELATION TO GOVT/IND SPECIFICATIONS, SEE TI DRAWING 729467

REV STATUS OF SHEETS			
REV	F	F
SH	1	2

NEXT ASSY	USED ON
2240843	8721

APPLICATION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES
- TOLERANCES: ANGLES ±1° 3 PLACE DECIMALS ±.010 2 PLACE DECIMALS ±.02
- INTERPRET DRAWING PER MIL-D-1000
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY MACHINED DIAMETERS .010 FIM
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

~~HOLE TOLERANCE: .013 THRU .125 +.004 -.001; .126 THRU .250 +.005 -.001; .251 THRU .500 +.006 -.001; .501 THRU .750 +.008 -.001; .751 THRU 1.000 +.010 -.001; 1.001 THRU 2.000 +.012 -.001~~

		DATE
DWN	D.SELVIDGE	12-4-84
CHK	A.VENEGAS	2-12-85
ENGR	J. G.	2-12-85
APVD	STEVE WALLACE	2-12-85
QA	WES DILLER	2-12-85
CONTR	SUSAN RILEY	2-12-85
RLSE	PETE PETERSON	2-12-85

TEXAS INSTRUMENTS INCORPORATED Digital Systems Group

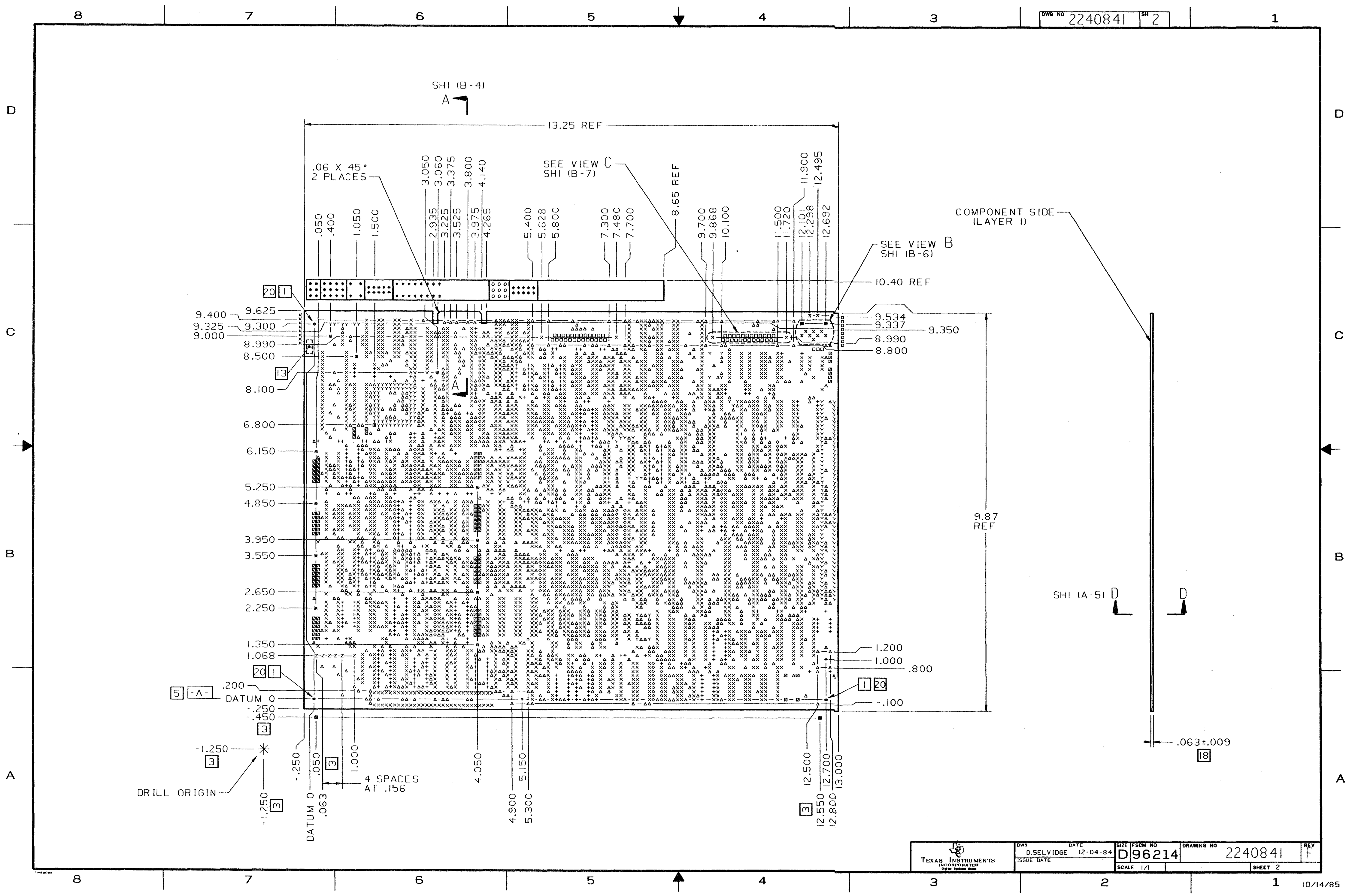
PRINTED WIRING BOARD, CPU

SIZE D FSCM NO 96214 DRAWING NO 2240841

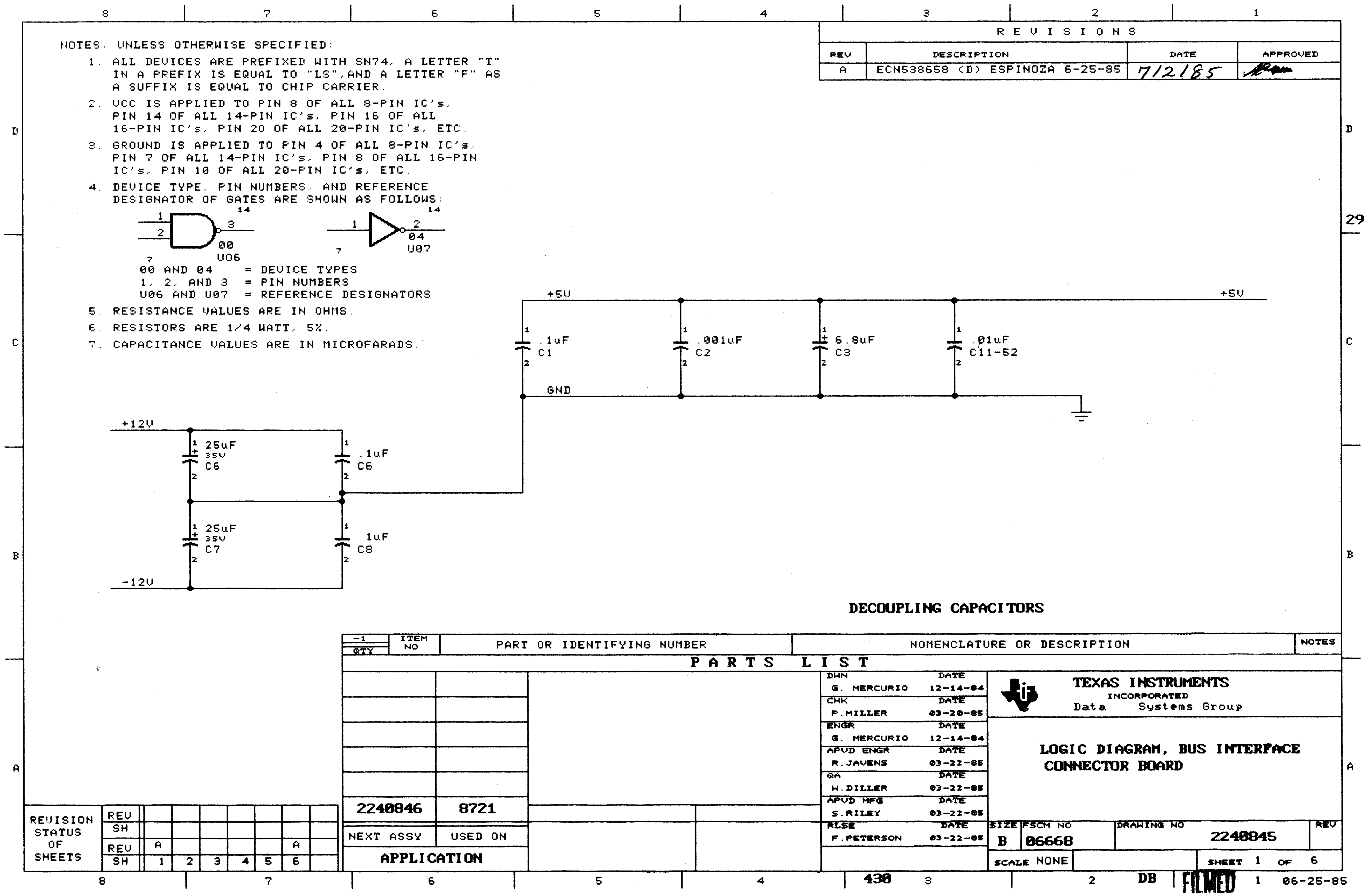
SCALE 1/1 SHEET 1 OF 2

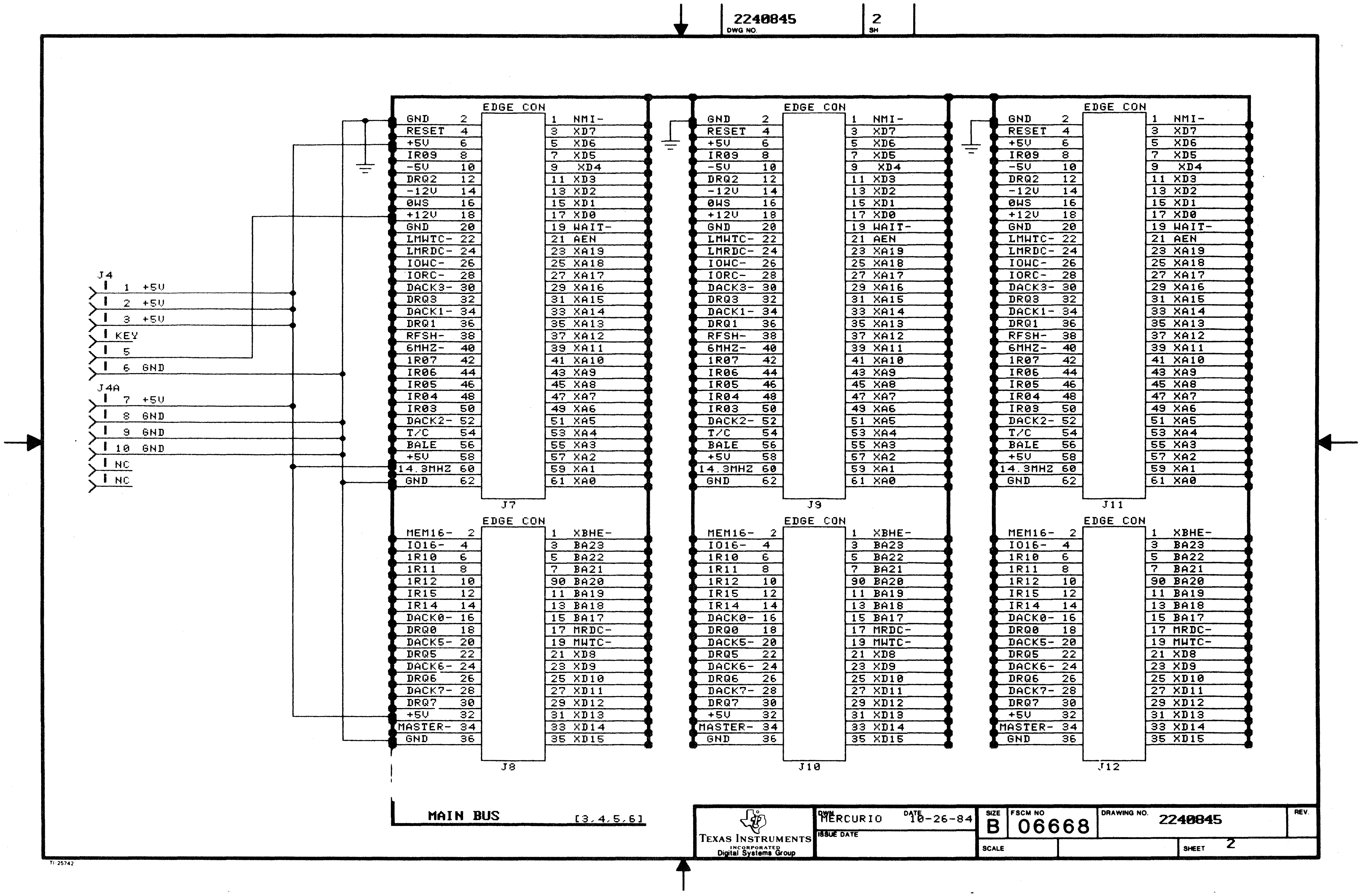
220 (A-GLPW,MA:H-MT) TYPE III TB 10/14/85

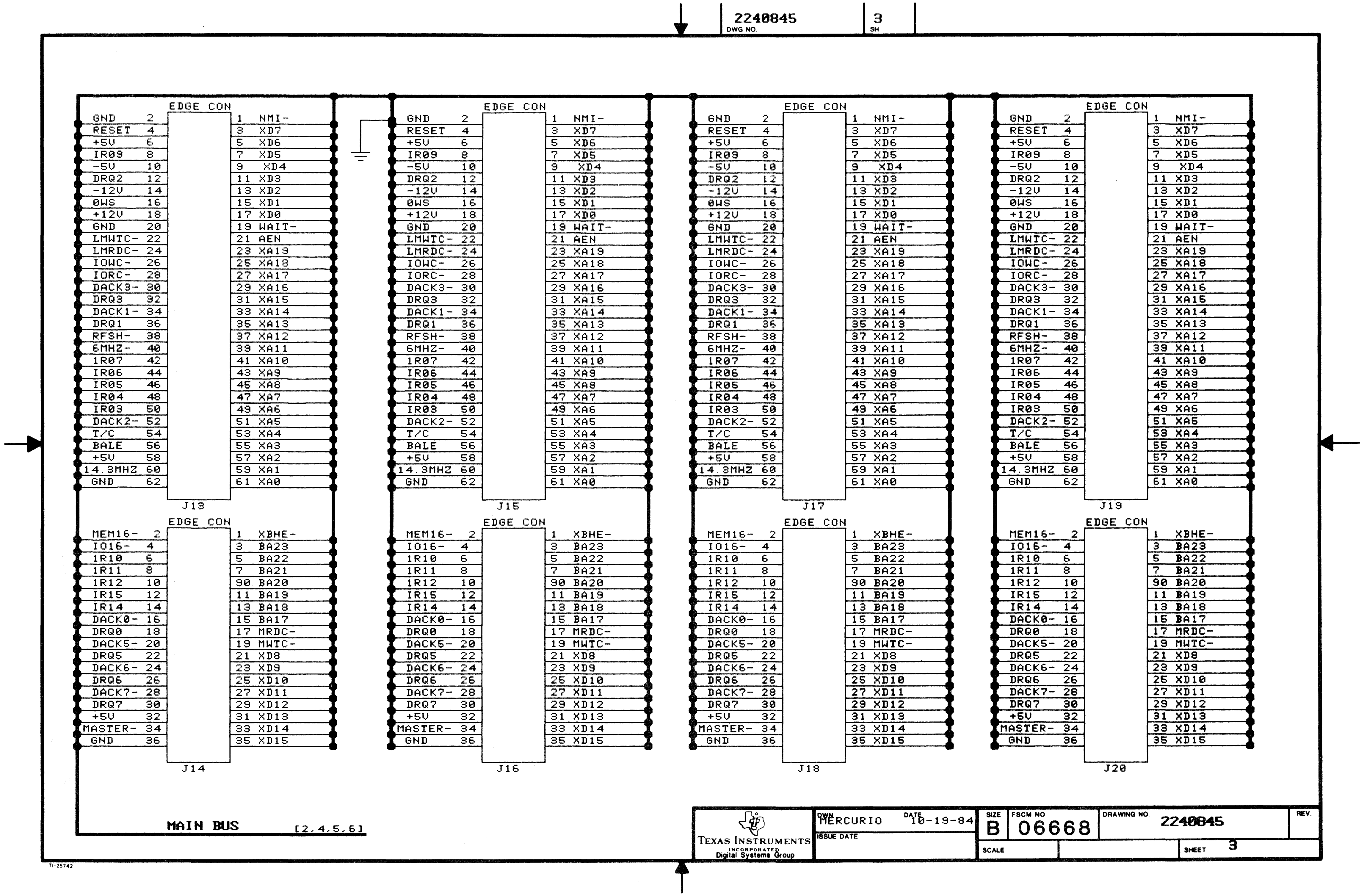
29

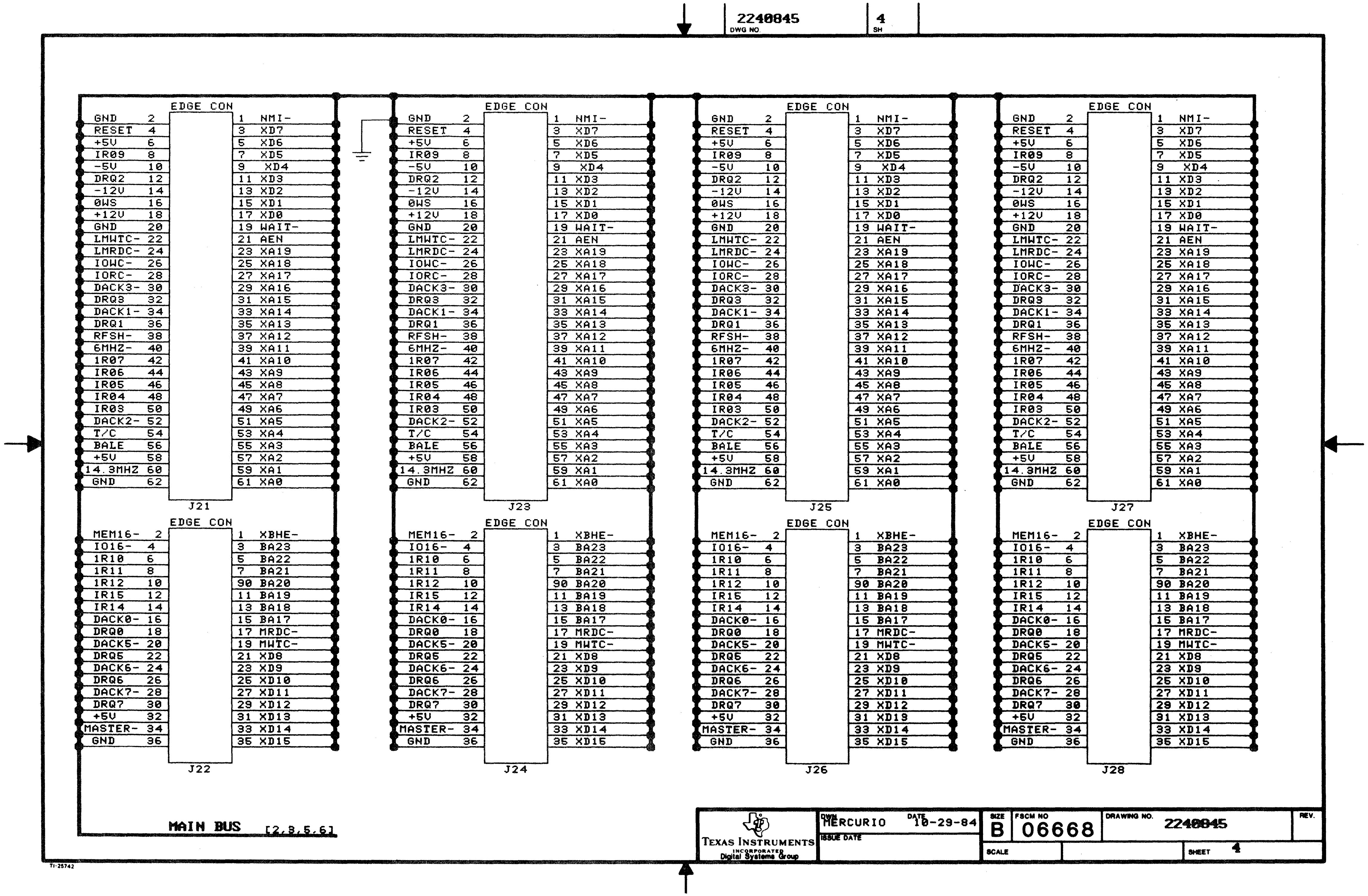


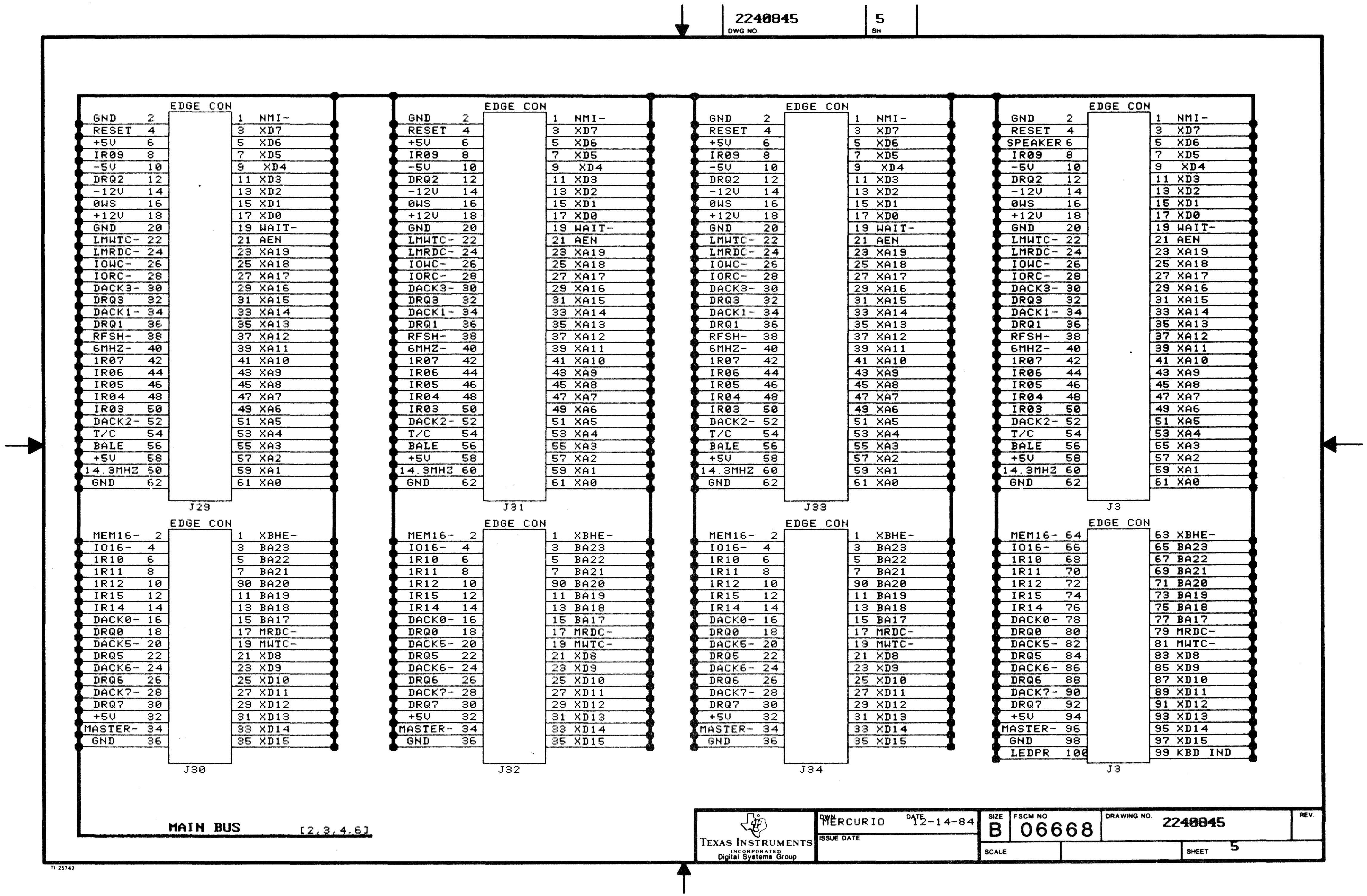
DWG NO 2240841 SH 2
SHI (B-4)
13.25 REF
.06 X 45°
2 PLACES
SEE VIEW C
SHI (B-7)
8.65 REF
SEE VIEW B
SHI (B-6)
10.40 REF
COMPONENT SIDE
(LAYER 1)
9.87
REF
SHI (A-5)
DATUM 0
DRILL ORIGIN
4 SPACES
AT .156
.063±.009
TEXAS INSTRUMENTS
D.SELVIDGE 12-04-84
D 96214
2240841
F
SCALE 1/1
SHEET 2
10/14/85

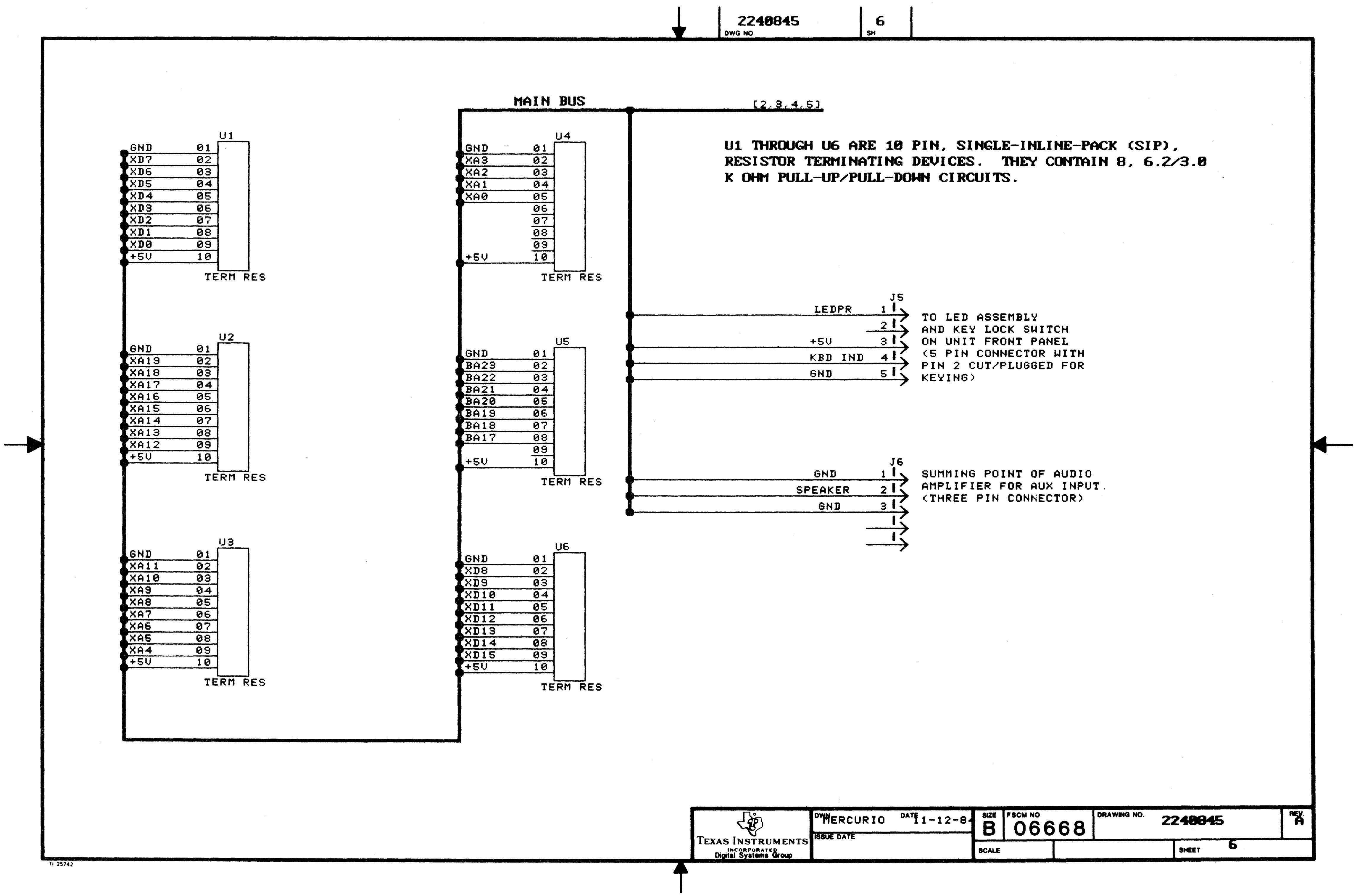

REVISIONS
REV
DESCRIPTION
DATE
APPROVED
A
ECN538658 (D) ESPINOZA 6-25-85
7/2/85
NOTES: UNLESS OTHERWISE SPECIFIED:
1. ALL DEVICES ARE PREFIXED WITH SN74. A LETTER "T" IN A PREFIX IS EQUAL TO "LS", AND A LETTER "F" AS A SUFFIX IS EQUAL TO CHIP CARRIER.
2. VCC IS APPLIED TO PIN 8 OF ALL 8-PIN IC's, PIN 14 OF ALL 14-PIN IC's, PIN 16 OF ALL 16-PIN IC's, PIN 20 OF ALL 20-PIN IC's, ETC.
3. GROUND IS APPLIED TO PIN 4 OF ALL 8-PIN IC's, PIN 7 OF ALL 14-PIN IC's, PIN 8 OF ALL 16-PIN IC's, PIN 10 OF ALL 20-PIN IC's, ETC.
4. DEVICE TYPE, PIN NUMBERS, AND REFERENCE DESIGNATOR OF GATES ARE SHOWN AS FOLLOWS:
00
U06
04
U07
00 AND 04 = DEVICE TYPES
1, 2, AND 3 = PIN NUMBERS
U06 AND U07 = REFERENCE DESIGNATORS
5. RESISTANCE VALUES ARE IN OHMS.
6. RESISTORS ARE 1/4 WATT, 5%.
7. CAPACITANCE VALUES ARE IN MICROFARADS.
+5V
.1uF
C1
.001uF
C2
6.8uF
C3
.01uF
C11-52
GND
+12V
25uF
35V
C6
.1uF
C6
25uF
35V
C7
.1uF
C8
-12V
DECOUPLING CAPACITORS
QTY
ITEM NO
PART OR IDENTIFYING NUMBER
NOMENCLATURE OR DESCRIPTION
NOTES
PARTS LIST
DWN G. MERCURIO 12-14-84
CHK P. MILLER 03-20-85
ENGR G. MERCURIO 12-14-84
APVD ENGR R. JAVENS 03-22-85
QA W. DILLER 03-22-85
APVD MFG S. RILEY 03-22-85
RLSE F. PETERSON 03-22-85
TEXAS INSTRUMENTS
INCORPORATED
Data Systems Group
LOGIC DIAGRAM, BUS INTERFACE CONNECTOR BOARD
2240846
8721
NEXT ASSY
USED ON
APPLICATION
REVISION STATUS OF SHEETS
SIZE B
FSCM NO 06668
DRAWING NO 2240845
SCALE NONE
SHEET 1 OF 6
430
DB
FILMED
06-25-85


2240845
DWG NO.
2
SH
EDGE CON
GND 2
RESET 4
+5V 6
IR09 8
-5V 10
DRQ2 12
-12V 14
0WS 16
+12V 18
GND 20
LMWTC- 22
LMRDC- 24
IOWC- 26
IORC- 28
DACK3- 30
DRQ3 32
DACK1- 34
DRQ1 36
RFSH- 38
6MHZ- 40
1R07 42
IR06 44
IR05 46
IR04 48
IR03 50
DACK2- 52
T/C 54
BALE 56
+5V 58
14.3MHZ 60
GND 62
1 NMI-
3 XD7
5 XD6
7 XD5
9 XD4
11 XD3
13 XD2
15 XD1
17 XD0
19 WAIT-
21 AEN
23 XA19
25 XA18
27 XA17
29 XA16
31 XA15
33 XA14
35 XA13
37 XA12
39 XA11
41 XA10
43 XA9
45 XA8
47 XA7
49 XA6
51 XA5
53 XA4
55 XA3
57 XA2
59 XA1
61 XA0
J7
J9
J11
EDGE CON
MEM16- 2
IO16- 4
1R10 6
1R11 8
1R12 10
IR15 12
IR14 14
DACK0- 16
DRQ0 18
DACK5- 20
DRQ5 22
DACK6- 24
DRQ6 26
DACK7- 28
DRQ7 30
+5V 32
MASTER- 34
GND 36
1 XBHE-
3 BA23
5 BA22
7 BA21
90 BA20
11 BA19
13 BA18
15 BA17
17 MRDC-
19 MWTC-
21 XD8
23 XD9
25 XD10
27 XD11
29 XD12
31 XD13
33 XD14
35 XD15
J8
J10
J12
J4
1 +5V
2 +5V
3 +5V
KEY
5
6 GND
J4A
7 +5V
8 GND
9 GND
10 GND
NC
NC
MAIN BUS
[3,4,5,6]
TEXAS INSTRUMENTS
INCORPORATED
Digital Systems Group
DWN MERCURIO
DATE 10-26-84
ISSUE DATE
SIZE B
FSCM NO 06668
DRAWING NO. 2240845
REV.
SCALE
SHEET 2


2240845
DWG NO.
3
SH
EDGE CON
GND 2
RESET 4
+5V 6
IR09 8
-5V 10
DRQ2 12
-12V 14
0WS 16
+12V 18
GND 20
LMWTC- 22
LMRDC- 24
IOWC- 26
IORC- 28
DACK3- 30
DRQ3 32
DACK1- 34
DRQ1 36
RFSH- 38
6MHZ- 40
IR07 42
IR06 44
IR05 46
IR04 48
IR03 50
DACK2- 52
T/C 54
BALE 56
+5V 58
14.3MHZ 60
GND 62
1 NMI-
3 XD7
5 XD6
7 XD5
9 XD4
11 XD3
13 XD2
15 XD1
17 XD0
19 WAIT-
21 AEN
23 XA19
25 XA18
27 XA17
29 XA16
31 XA15
33 XA14
35 XA13
37 XA12
39 XA11
41 XA10
43 XA9
45 XA8
47 XA7
49 XA6
51 XA5
53 XA4
55 XA3
57 XA2
59 XA1
61 XA0
J13
J15
J17
J19
EDGE CON
MEM16- 2
IO16- 4
IR10 6
IR11 8
IR12 10
IR15 12
IR14 14
DACK0- 16
DRQ0 18
DACK5- 20
DRQ5 22
DACK6- 24
DRQ6 26
DACK7- 28
DRQ7 30
+5V 32
MASTER- 34
GND 36
1 XBHE-
3 BA23
5 BA22
7 BA21
90 BA20
11 BA19
13 BA18
15 BA17
17 MRDC-
19 MWTC-
21 XD8
23 XD9
25 XD10
27 XD11
29 XD12
31 XD13
33 XD14
35 XD15
J14
J16
J18
J20
MAIN BUS
[2,4,5,6]
TEXAS INSTRUMENTS
INCORPORATED
Digital Systems Group
DWN MERCURIO
DATE 10-19-84
ISSUE DATE
SIZE B
FSCM NO 06668
DRAWING NO. 2240845
REV.
SCALE
SHEET 3


2240845
DWG NO
4
SH
EDGE CON
GND 2
RESET 4
+5V 6
IR09 8
-5V 10
DRQ2 12
-12V 14
0WS 16
+12V 18
GND 20
LMWTC- 22
LMRDC- 24
IOWC- 26
IORC- 28
DACK3- 30
DRQ3 32
DACK1- 34
DRQ1 36
RFSH- 38
6MHZ- 40
IR07 42
IR06 44
IR05 46
IR04 48
IR03 50
DACK2- 52
T/C 54
BALE 56
+5V 58
14.3MHZ 60
GND 62
1 NMI-
3 XD7
5 XD6
7 XD5
9 XD4
11 XD3
13 XD2
15 XD1
17 XD0
19 WAIT-
21 AEN
23 XA19
25 XA18
27 XA17
29 XA16
31 XA15
33 XA14
35 XA13
37 XA12
39 XA11
41 XA10
43 XA9
45 XA8
47 XA7
49 XA6
51 XA5
53 XA4
55 XA3
57 XA2
59 XA1
61 XA0
J21
J23
J25
J27
EDGE CON
MEM16- 2
IO16- 4
IR10 6
IR11 8
IR12 10
IR15 12
IR14 14
DACK0- 16
DRQ0 18
DACK5- 20
DRQ5 22
DACK6- 24
DRQ6 26
DACK7- 28
DRQ7 30
+5V 32
MASTER- 34
GND 36
1 XBHE-
3 BA23
5 BA22
7 BA21
90 BA20
11 BA19
13 BA18
15 BA17
17 MRDC-
19 MWTC-
21 XD8
23 XD9
25 XD10
27 XD11
29 XD12
31 XD13
33 XD14
35 XD15
J22
J24
J26
J28
MAIN BUS [2,3,5,6]
TEXAS INSTRUMENTS
INCORPORATED
Digital Systems Group
DWN MERCURIO
DATE 10-29-84
ISSUE DATE
SIZE B
FSCM NO 06668
DRAWING NO. 2240845
REV.
SCALE
SHEET 4
TI-25742


2240845
DWG NO.
5
SH
EDGE CON
GND 2 / 1 NMI-
RESET 4 / 3 XD7
+5V 6 / 5 XD6
IR09 8 / 7 XD5
-5V 10 / 9 XD4
DRQ2 12 / 11 XD3
-12V 14 / 13 XD2
0WS 16 / 15 XD1
+12V 18 / 17 XD0
GND 20 / 19 WAIT-
LMWTC- 22 / 21 AEN
LMRDC- 24 / 23 XA19
IOWC- 26 / 25 XA18
IORC- 28 / 27 XA17
DACK3- 30 / 29 XA16
DRQ3 32 / 31 XA15
DACK1- 34 / 33 XA14
DRQ1 36 / 35 XA13
RFSH- 38 / 37 XA12
6MHZ- 40 / 39 XA11
IR07 42 / 41 XA10
IR06 44 / 43 XA9
IR05 46 / 45 XA8
IR04 48 / 47 XA7
IR03 50 / 49 XA6
DACK2- 52 / 51 XA5
T/C 54 / 53 XA4
BALE 56 / 55 XA3
+5V 58 / 57 XA2
14.3MHZ 50 / 59 XA1
GND 62 / 61 XA0
J29
EDGE CON
MEM16- 2 / 1 XBHE-
IO16- 4 / 3 BA23
IR10 6 / 5 BA22
IR11 8 / 7 BA21
IR12 10 / 90 BA20
IR15 12 / 11 BA19
IR14 14 / 13 BA18
DACK0- 16 / 15 BA17
DRQ0 18 / 17 MRDC-
DACK5- 20 / 19 MWTC-
DRQ5 22 / 21 XD8
DACK6- 24 / 23 XD9
DRQ6 26 / 25 XD10
DACK7- 28 / 27 XD11
DRQ7 30 / 29 XD12
+5V 32 / 31 XD13
MASTER- 34 / 33 XD14
GND 36 / 35 XD15
J30
EDGE CON
GND 2 / 1 NMI-
RESET 4 / 3 XD7
+5V 6 / 5 XD6
IR09 8 / 7 XD5
-5V 10 / 9 XD4
DRQ2 12 / 11 XD3
-12V 14 / 13 XD2
0WS 16 / 15 XD1
+12V 18 / 17 XD0
GND 20 / 19 WAIT-
LMWTC- 22 / 21 AEN
LMRDC- 24 / 23 XA19
IOWC- 26 / 25 XA18
IORC- 28 / 27 XA17
DACK3- 30 / 29 XA16
DRQ3 32 / 31 XA15
DACK1- 34 / 33 XA14
DRQ1 36 / 35 XA13
RFSH- 38 / 37 XA12
6MHZ- 40 / 39 XA11
IR07 42 / 41 XA10
IR06 44 / 43 XA9
IR05 46 / 45 XA8
IR04 48 / 47 XA7
IR03 50 / 49 XA6
DACK2- 52 / 51 XA5
T/C 54 / 53 XA4
BALE 56 / 55 XA3
+5V 58 / 57 XA2
14.3MHZ 60 / 59 XA1
GND 62 / 61 XA0
J31
EDGE CON
MEM16- 2 / 1 XBHE-
IO16- 4 / 3 BA23
IR10 6 / 5 BA22
IR11 8 / 7 BA21
IR12 10 / 90 BA20
IR15 12 / 11 BA19
IR14 14 / 13 BA18
DACK0- 16 / 15 BA17
DRQ0 18 / 17 MRDC-
DACK5- 20 / 19 MWTC-
DRQ5 22 / 21 XD8
DACK6- 24 / 23 XD9
DRQ6 26 / 25 XD10
DACK7- 28 / 27 XD11
DRQ7 30 / 29 XD12
+5V 32 / 31 XD13
MASTER- 34 / 33 XD14
GND 36 / 35 XD15
J32
EDGE CON
GND 2 / 1 NMI-
RESET 4 / 3 XD7
+5V 6 / 5 XD6
IR09 8 / 7 XD5
-5V 10 / 9 XD4
DRQ2 12 / 11 XD3
-12V 14 / 13 XD2
0WS 16 / 15 XD1
+12V 18 / 17 XD0
GND 20 / 19 WAIT-
LMWTC- 22 / 21 AEN
LMRDC- 24 / 23 XA19
IOWC- 26 / 25 XA18
IORC- 28 / 27 XA17
DACK3- 30 / 29 XA16
DRQ3 32 / 31 XA15
DACK1- 34 / 33 XA14
DRQ1 36 / 35 XA13
RFSH- 38 / 37 XA12
6MHZ- 40 / 39 XA11
IR07 42 / 41 XA10
IR06 44 / 43 XA9
IR05 46 / 45 XA8
IR04 48 / 47 XA7
IR03 50 / 49 XA6
DACK2- 52 / 51 XA5
T/C 54 / 53 XA4
BALE 56 / 55 XA3
+5V 58 / 57 XA2
14.3MHZ 60 / 59 XA1
GND 62 / 61 XA0
J33
EDGE CON
MEM16- 2 / 1 XBHE-
IO16- 4 / 3 BA23
IR10 6 / 5 BA22
IR11 8 / 7 BA21
IR12 10 / 90 BA20
IR15 12 / 11 BA19
IR14 14 / 13 BA18
DACK0- 16 / 15 BA17
DRQ0 18 / 17 MRDC-
DACK5- 20 / 19 MWTC-
DRQ5 22 / 21 XD8
DACK6- 24 / 23 XD9
DRQ6 26 / 25 XD10
DACK7- 28 / 27 XD11
DRQ7 30 / 29 XD12
+5V 32 / 31 XD13
MASTER- 34 / 33 XD14
GND 36 / 35 XD15
J34
EDGE CON
GND 2 / 1 NMI-
RESET 4 / 3 XD7
SPEAKER 6 / 5 XD6
IR09 8 / 7 XD5
-5V 10 / 9 XD4
DRQ2 12 / 11 XD3
-12V 14 / 13 XD2
0WS 16 / 15 XD1
+12V 18 / 17 XD0
GND 20 / 19 WAIT-
LMWTC- 22 / 21 AEN
LMRDC- 24 / 23 XA19
IOWC- 26 / 25 XA18
IORC- 28 / 27 XA17
DACK3- 30 / 29 XA16
DRQ3 32 / 31 XA15
DACK1- 34 / 33 XA14
DRQ1 36 / 35 XA13
RFSH- 38 / 37 XA12
6MHZ- 40 / 39 XA11
IR07 42 / 41 XA10
IR06 44 / 43 XA9
IR05 46 / 45 XA8
IR04 48 / 47 XA7
IR03 50 / 49 XA6
DACK2- 52 / 51 XA5
T/C 54 / 53 XA4
BALE 56 / 55 XA3
+5V 58 / 57 XA2
14.3MHZ 60 / 59 XA1
GND 62 / 61 XA0
J3
EDGE CON
MEM16- 64 / 63 XBHE-
IO16- 66 / 65 BA23
IR10 68 / 67 BA22
IR11 70 / 69 BA21
IR12 72 / 71 BA20
IR15 74 / 73 BA19
IR14 76 / 75 BA18
DACK0- 78 / 77 BA17
DRQ0 80 / 79 MRDC-
DACK5- 82 / 81 MWTC-
DRQ5 84 / 83 XD8
DACK6- 86 / 85 XD9
DRQ6 88 / 87 XD10
DACK7- 90 / 89 XD11
DRQ7 92 / 91 XD12
+5V 94 / 93 XD13
MASTER- 96 / 95 XD14
GND 98 / 97 XD15
LEDPR 100 / 99 KBD IND
J3
MAIN BUS
[2,3,4,6]
TEXAS INSTRUMENTS
INCORPORATED
Digital Systems Group
DWN MERCURIO
DATE 12-14-84
ISSUE DATE
SIZE B
FSCM NO 06668
DRAWING NO. 2240845
REV.
SCALE
SHEET 5
TI 25742



2240845 DWG NO 6 SH
MAIN BUS [2,3,4,5]
U1 THROUGH U6 ARE 10 PIN, SINGLE-INLINE-PACK (SIP), RESISTOR TERMINATING DEVICES. THEY CONTAIN 8, 6.2/3.0 K OHM PULL-UP/PULL-DOWN CIRCUITS.
U1 GND 01 XD7 02 XD6 03 XD5 04 XD4 05 XD3 06 XD2 07 XD1 08 XD0 09 +5V 10 TERM RES
U2 GND 01 XA19 02 XA18 03 XA17 04 XA16 05 XA15 06 XA14 07 XA13 08 XA12 09 +5V 10 TERM RES
U3 GND 01 XA11 02 XA10 03 XA9 04 XA8 05 XA7 06 XA6 07 XA5 08 XA4 09 +5V 10 TERM RES
U4 GND 01 XA3 02 XA2 03 XA1 04 XA0 05 06 07 08 09 +5V 10 TERM RES
U5 GND 01 BA23 02 BA22 03 BA21 04 BA20 05 BA19 06 BA18 07 BA17 08 09 +5V 10 TERM RES
U6 GND 01 XD8 02 XD9 03 XD10 04 XD11 05 XD12 06 XD13 07 XD14 08 XD15 09 +5V 10 TERM RES
J5 LEDPR 1 2 +5V 3 KBD IND 4 GND 5
TO LED ASSEMBLY AND KEY LOCK SWITCH ON UNIT FRONT PANEL (5 PIN CONNECTOR WITH PIN 2 CUT/PLUGGED FOR KEYING)
J6 GND 1 SPEAKER 2 GND 3
SUMMING POINT OF AUDIO AMPLIFIER FOR AUX INPUT. (THREE PIN CONNECTOR)
TEXAS INSTRUMENTS INCORPORATED Digital Systems Group
DWN MERCURIO DATE 11-12-84
ISSUE DATE
SIZE B FSCM NO 06668 DRAWING NO. 2240845 REV. A
SCALE SHEET 6
TI-25742

2240849 DRAWING NO | 1 SH

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	ECN538653 (D) ESPINOZA 6-21-85	7/2/85	[illegible]

NOTES, UNLESS OTHERWISE SPECIFIED:

1. ALL DEVICES ARE PREFIXED WITH SN74, A LETTER "T" IN A PREFIX IS EQUAL TO "LS", AND A LETTER "F" AS A SUFFIX IS EQUAL TO CHIP CARRIER
2. VCC IS APPLIED TO PIN 8 OF ALL 8-PIN IC's, PIN 14 OF ALL 14-PIN IC's, PIN 16 OF ALL 16-PIN IC's, PIN 20 OF ALL 20-PIN IC's, ETC
3. GROUND IS APPLIED TO PIN 4 OF ALL 8-PIN IC's, PIN 7 OF ALL 14-PIN IC's, PIN 8 OF ALL 16-PIN IC's, PIN 10 OF ALL 20-PIN IC's, ETC
4. DEVICE TYPE, PIN NUMBERS, AND REFERENCE DESIGNATOR OF GATES ARE SHOWN AS FOLLOWS:

00 AND 04 = DEVICE TYPES
1, 2, AND 3 = PIN NUMBERS
U06 AND U07 = REFERENCE DESIGNATORS

5. RESISTANCE VALUES ARE IN OHMS
6. RESISTORS ARE 1/4 WATT, 5%
7. CAPACITANCE VALUES ARE IN MICROFARADS

29

COMPUTER GENERATED DRAWING ; DO NOT REVISE MANUALLY

-1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES

PARTS LIST

UNLESS OTHERWISE SPECIFIED
* DIMENSIONS ARE IN INCHES
* TOLERANCES: ANGLES +/-1 DEG
3 PLACE DECIMALS +/-.010
2 PLACE DECIMALS +/-.02
* INTERPRET DRAWING PER MIL-D-1000
* REMOVE BURRS AND SHARP EDGES
* CONCENTRICITY MACHINED DIAMETERS .010 FIM
* DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
* PARENTHETICAL INFO FOR REF ONLY

HOLE TOLERANCE

.013 THRU .125 +.004 -.001	.126 THRU .250 +.005 -.001	.251 THRU .500 +.006 -.001
.501 THRU .750 +.008 -.001	.751 THRU 1.000 +.010 -.001	1.001 THRU 2.000 +.012 -.001

DWN	G.MERCURIO	DATE 10-12-84
CHK	F.PETERSON	DATE 3-22-85
ENGR	G.MERCURIO	DATE 10-12-84
APVD ENGR	R.JAVENS	DATE 3-22-85
QA	W.DILLER	DATE 3-22-85
APVD MFG	S.RILEY	DATE 3-22-85
RELEASE	F.PETERSON	DATE 3-22-85

NEXT ASSY	USED ON
2240850	8721

APPLICATION

REV	A	A
SH	1	2

REVISION STATUS OF SHEETS

TEXAS INSTRUMENTS
Data Systems Group

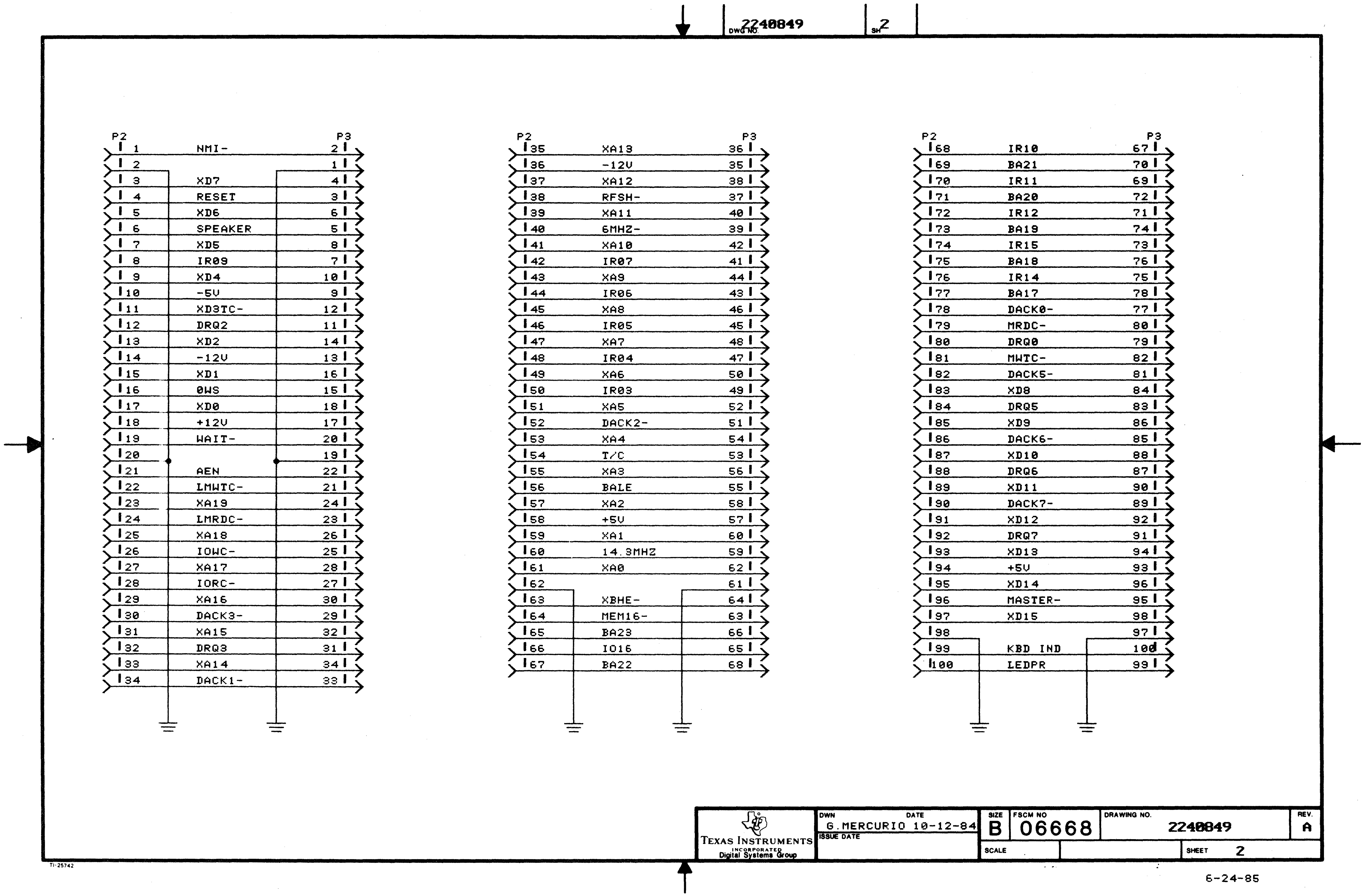
DIAGRAM, LOGIC, DETAILED-
VERTICAL BOARD - EXCALIBUR

SIZE B | FSCM NO 06668 | DRAWING NO 2240849

SCALE NONE | SHEET 1 OF 2

FILMED DB 6-21-85

430


DWG NO. 2240849 SH 2
P2 P3
1 NMI- 2
2 1
3 XD7 4
4 RESET 3
5 XD6 6
6 SPEAKER 5
7 XD5 8
8 IR09 7
9 XD4 10
10 -5V 9
11 XD3TC- 12
12 DRQ2 11
13 XD2 14
14 -12V 13
15 XD1 16
16 0WS 15
17 XD0 18
18 +12V 17
19 WAIT- 20
20 19
21 AEN 22
22 LMWTC- 21
23 XA19 24
24 LMRDC- 23
25 XA18 26
26 IOWC- 25
27 XA17 28
28 IORC- 27
29 XA16 30
30 DACK3- 29
31 XA15 32
32 DRQ3 31
33 XA14 34
34 DACK1- 33
P2 P3
35 XA13 36
36 -12V 35
37 XA12 38
38 RFSH- 37
39 XA11 40
40 6MHZ- 39
41 XA10 42
42 IR07 41
43 XA9 44
44 IR06 43
45 XA8 46
46 IR05 45
47 XA7 48
48 IR04 47
49 XA6 50
50 IR03 49
51 XA5 52
52 DACK2- 51
53 XA4 54
54 T/C 53
55 XA3 56
56 BALE 55
57 XA2 58
58 +5V 57
59 XA1 60
60 14.3MHZ 59
61 XA0 62
62 61
63 XBHE- 64
64 MEM16- 63
65 BA23 66
66 IO16 65
67 BA22 68
P2 P3
68 IR10 67
69 BA21 70
70 IR11 69
71 BA20 72
72 IR12 71
73 BA19 74
74 IR15 73
75 BA18 76
76 IR14 75
77 BA17 78
78 DACK0- 77
79 MRDC- 80
80 DRQ0 79
81 MWTC- 82
82 DACK5- 81
83 XD8 84
84 DRQ5 83
85 XD9 86
86 DACK6- 85
87 XD10 88
88 DRQ6 87
89 XD11 90
90 DACK7- 89
91 XD12 92
92 DRQ7 91
93 XD13 94
94 +5V 93
95 XD14 96
96 MASTER- 95
97 XD15 98
98 97
99 KBD IND 100
100 LEDPR 99
TEXAS INSTRUMENTS
INCORPORATED
Digital Systems Group
DWN G.MERCURIO DATE 10-12-84
ISSUE DATE
SIZE B
FSCM NO 06668
DRAWING NO. 2240849
REV. A
SCALE
SHEET 2
TI-25742
6-24-85

2240921 DRAWING NO — SH 1

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	ECN538277 (C) ESPINOZA 6-28-85	7-2-85	A. VENEJAS
B	CN 530758 (D) D.JONES	10-1-85	C. KEELER
C	CN 548997 (E) D.JONES	12-2-85	C. KEELER

NOTES: UNLESS OTHERWISE SPECIFIED:

1. ALL DEVICES ARE PREFIXED WITH SN74. A LETTER "T" IN A PREFIX IS EQUAL TO "LS". EXCEPT WHEN USED AS A SUFFIX. "AT" IS EQUAL TO "ALS". AND A LETTER "F" AS A SUFFIX IS EQUAL TO A CHIP CARRIER
2. VCC IS APPLIED TO PIN 8 OF ALL 8-PIN IC's. PIN 14 OF ALL 14-PIN IC's. PIN 16 OF ALL 16-PIN IC's. PIN 20 OF ALL 20-PIN IC's. ETC
3. GROUND IS APPLIED TO PIN 4 OF ALL 8-PIN IC's. PIN 7 OF ALL 14-PIN IC's. PIN 8 OF ALL 16-PIN IC's. PIN 10 OF ALL 20-PIN IC's. ETC
4. DEVICE TYPE, PIN NUMBERS, AND REFERENCE DESIGNATOR OF GATES ARE SHOWN AS FOLLOWS:

00 AND 04 = DEVICE TYPES
1, 2, AND 3 = PIN NUMBERS
U06 AND U07 = REFERENCE DESIGNATORS

5. RESISTANCE VALUES ARE IN OHMS
6. RESISTORS ARE 1/4 WATT, 5%
7. CAPACITANCE VALUES ARE IN MICROFARADS

29

COMPUTER GENERATED DRAWING ; DO NOT REVISE MANUALLY

-1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES

PARTS LIST

UNLESS OTHERWISE SPECIFIED
* DIMENSIONS ARE IN INCHES
* TOLERANCES: ANGLES +/-1 DEG
  3 PLACE DECIMALS +/-.010
  2 PLACE DECIMALS +/-.02
* INTERPRET DRAWING PER MIL-D-1000
* REMOVE BURRS AND SHARP EDGES
* CONCENTRICITY MACHINED DIAMETERS .010 FIM
* DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
* PARENTHETICAL INFO FOR REF ONLY

HOLE TOLERANCE

.013 THRU .125 +.004 -.001	.126 THRU .250 +.005 -.001	.251 THRU .500 +.006 -.001
.501 THRU .750 +.008 -.001	.751 THRU 1.000 +.010 -.001	1.001 THRU 2.000 +.012 -.001

DWN	C.HALEY	DATE 02-21-85
CHK	F.PETERSON	DATE 04-18-85
ENGR	C.HALEY	DATE 04-20-85
APVD ENGR	C.HALEY	DATE 04-20-85
QA	W.DILLER	DATE 04-29-85
APVD MFG	R.LEVERETT	DATE 04-22-85
RELEASE	F.PETERSON	DATE 04-29-85

TEXAS INSTRUMENTS
Data Systems Group

DIAGRAM, LOGIC, DETAILED-
FLOPPY CONTROLLER
EXCALIBUR

SIZE B — FSCM NO 06668 — DRAWING NO 2240921
SCALE NONE — SHEET 1 OF 10

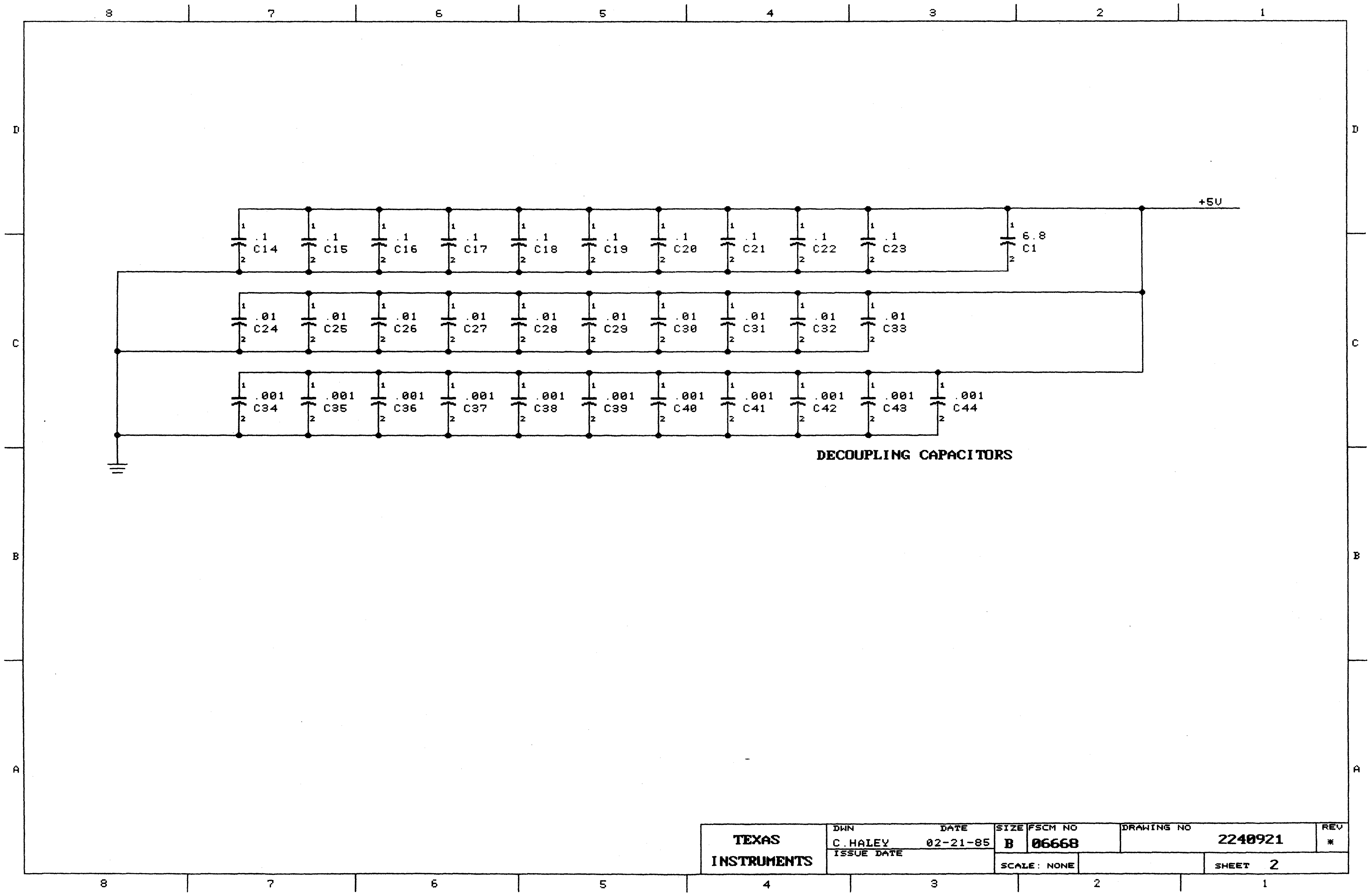
NEXT ASSY	USED ON
2240922	8721

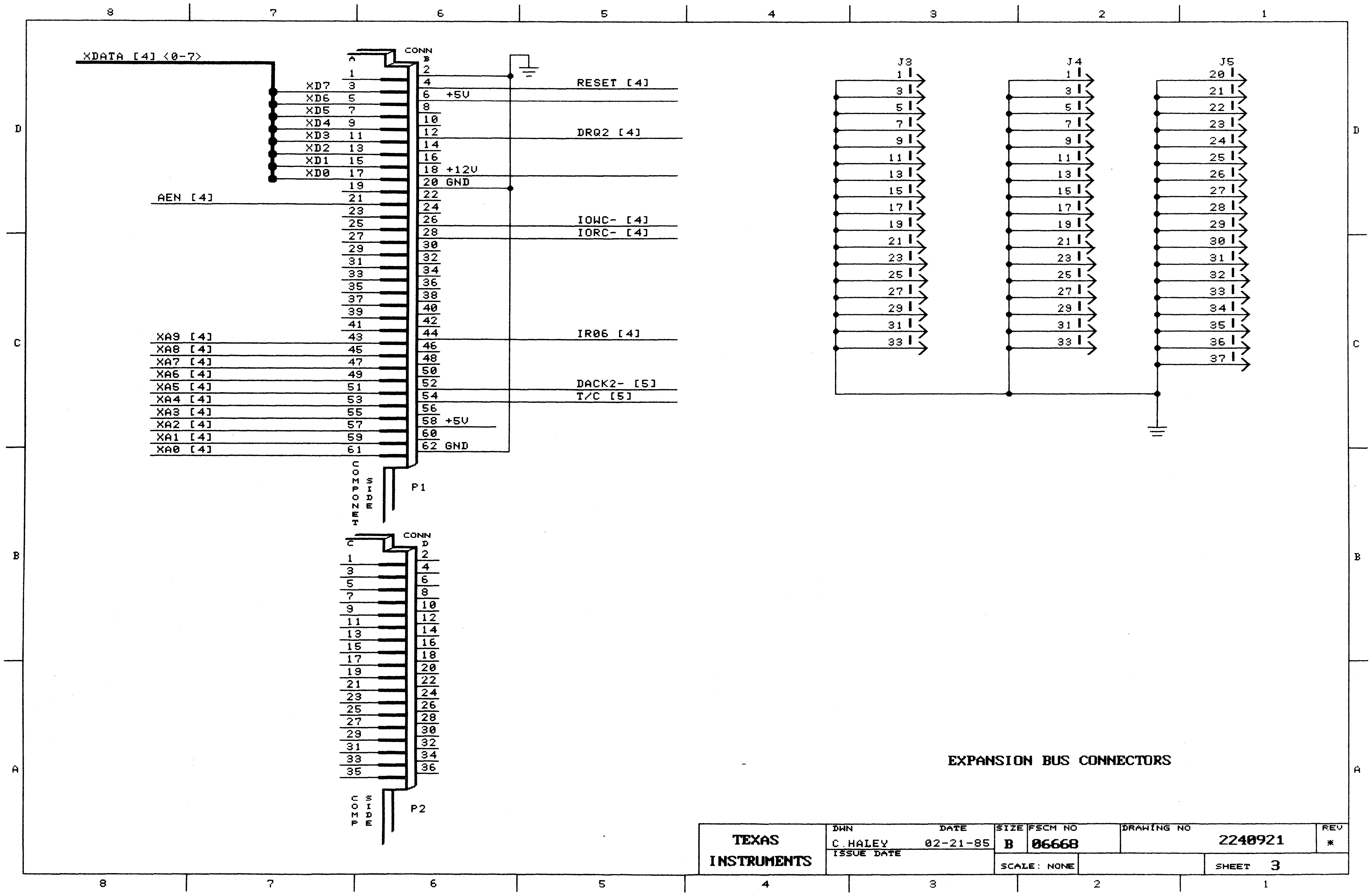
APPLICATION

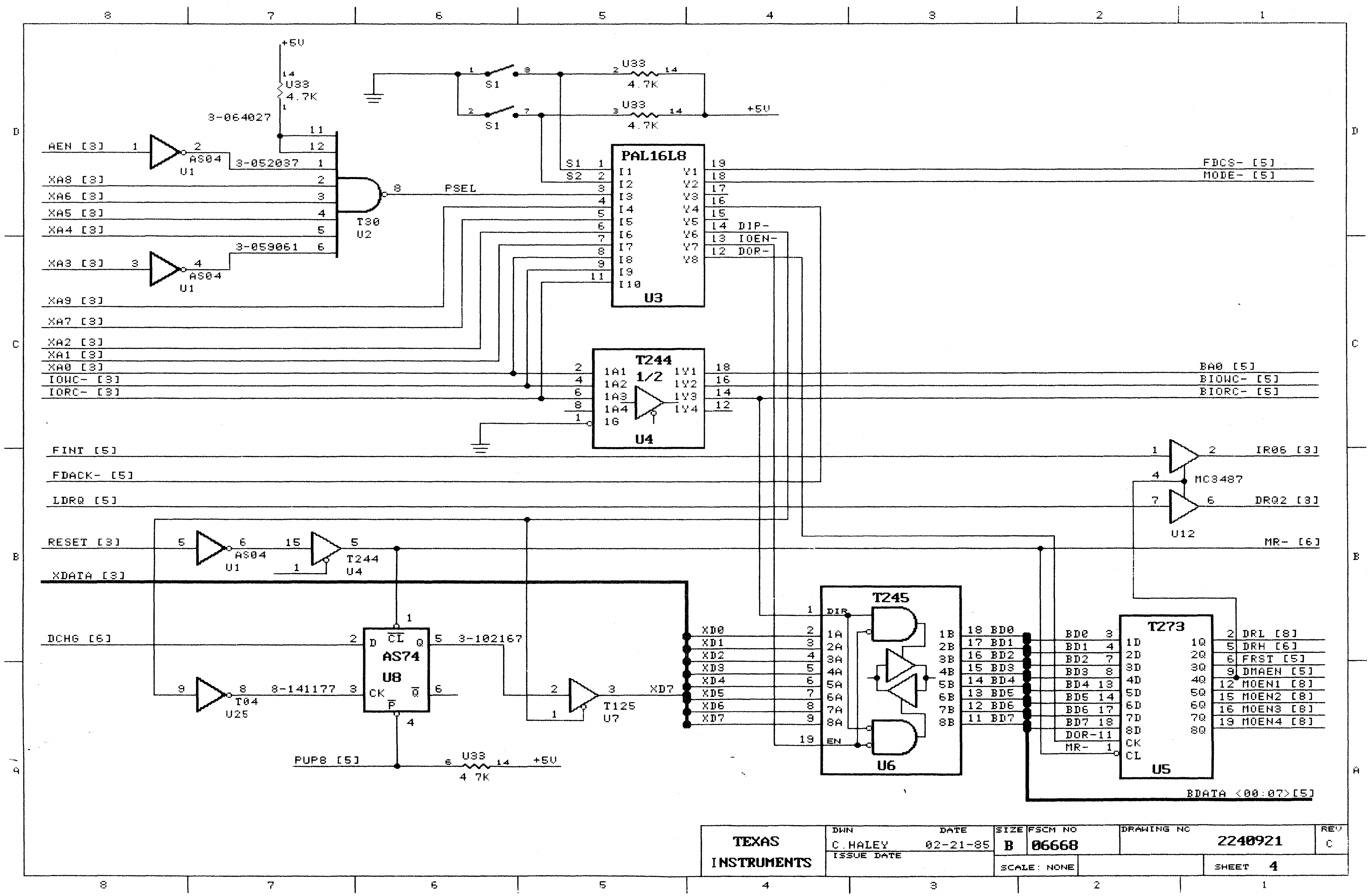
REV										
SH										
REV	C			C	C	C	A		C	C
SH	1	2	3	4	5	6	7	8	9	10

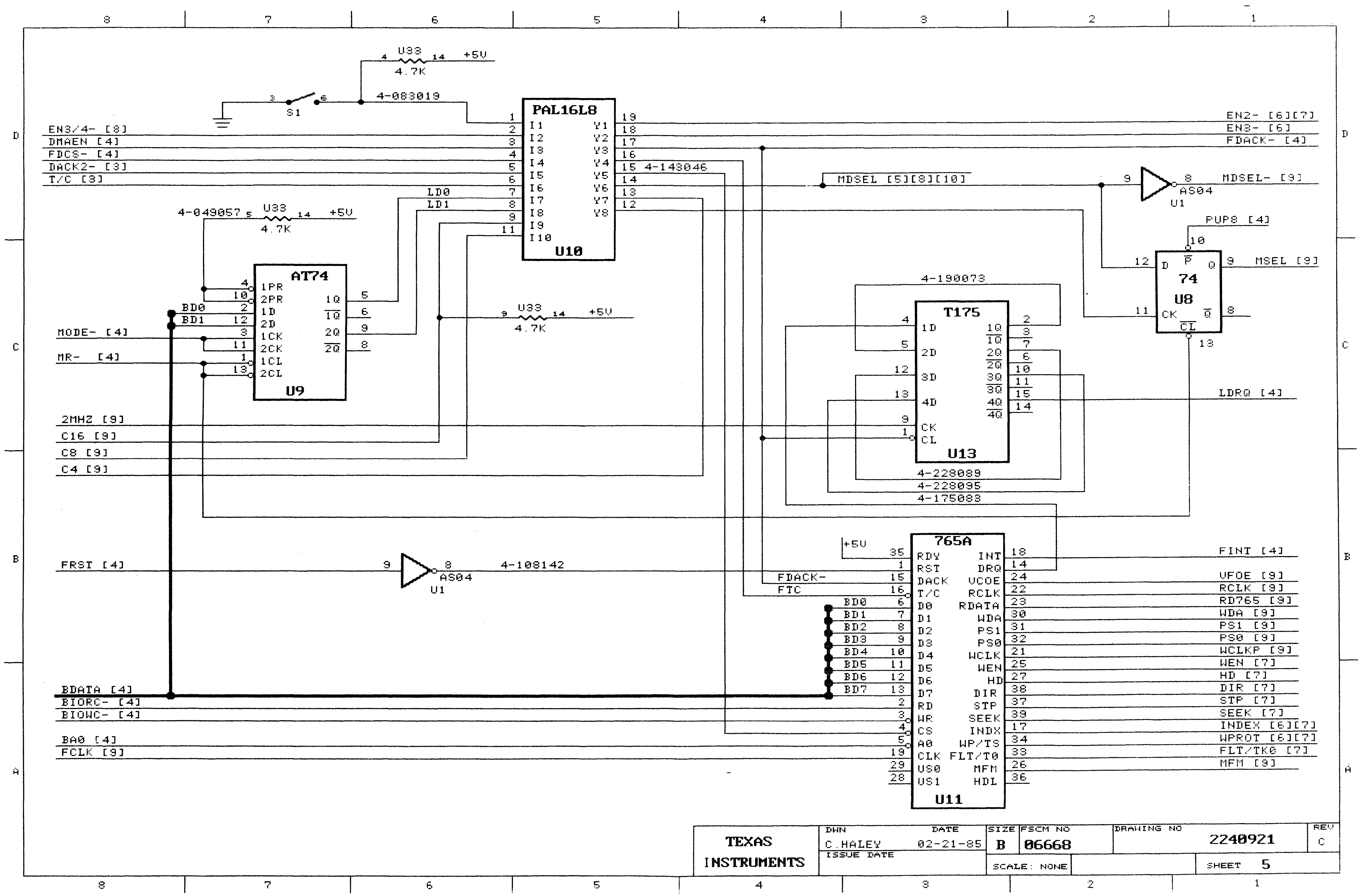
REVISION STATUS OF SHEETS

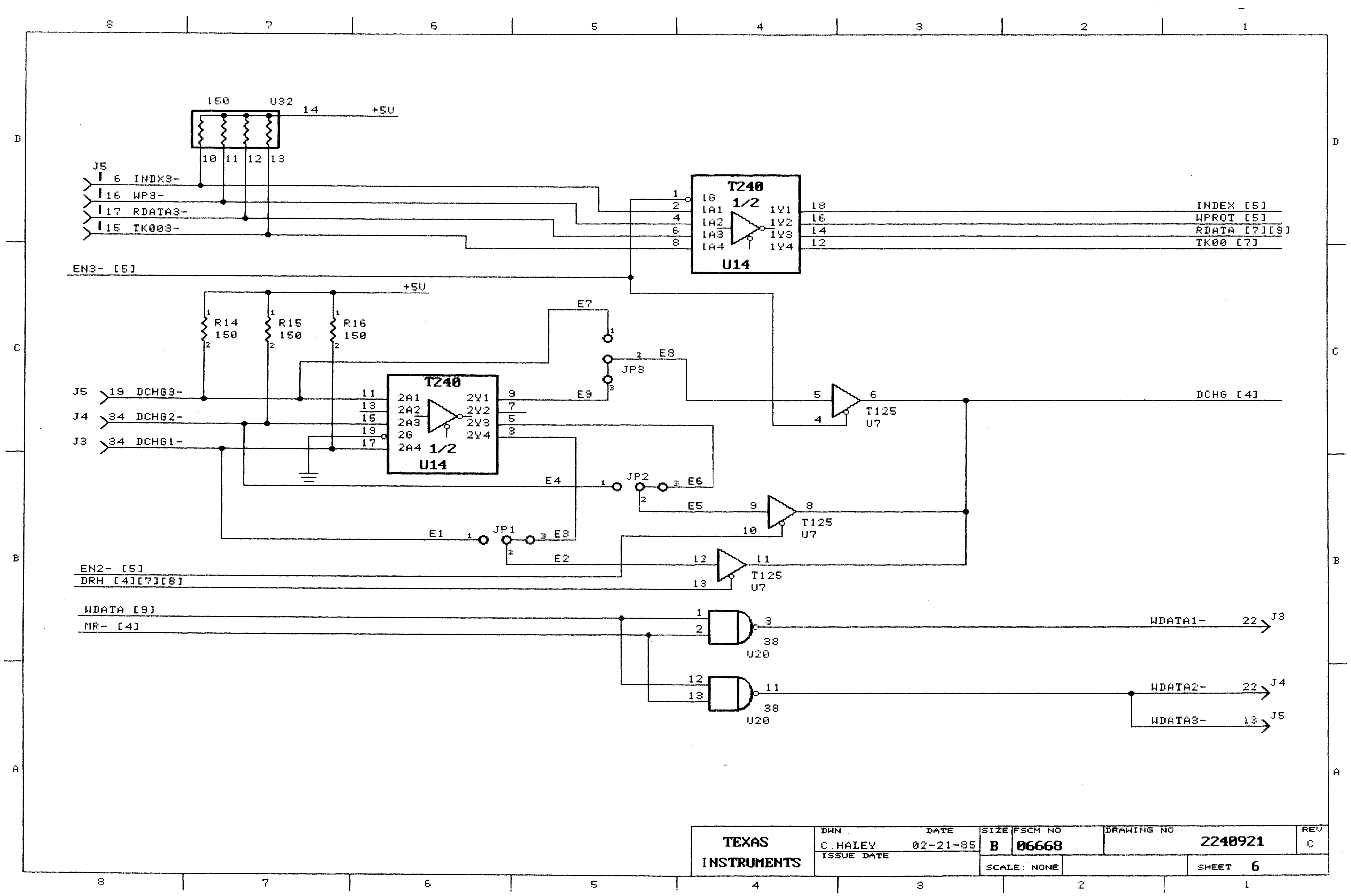
430 — DB — 6-28-85

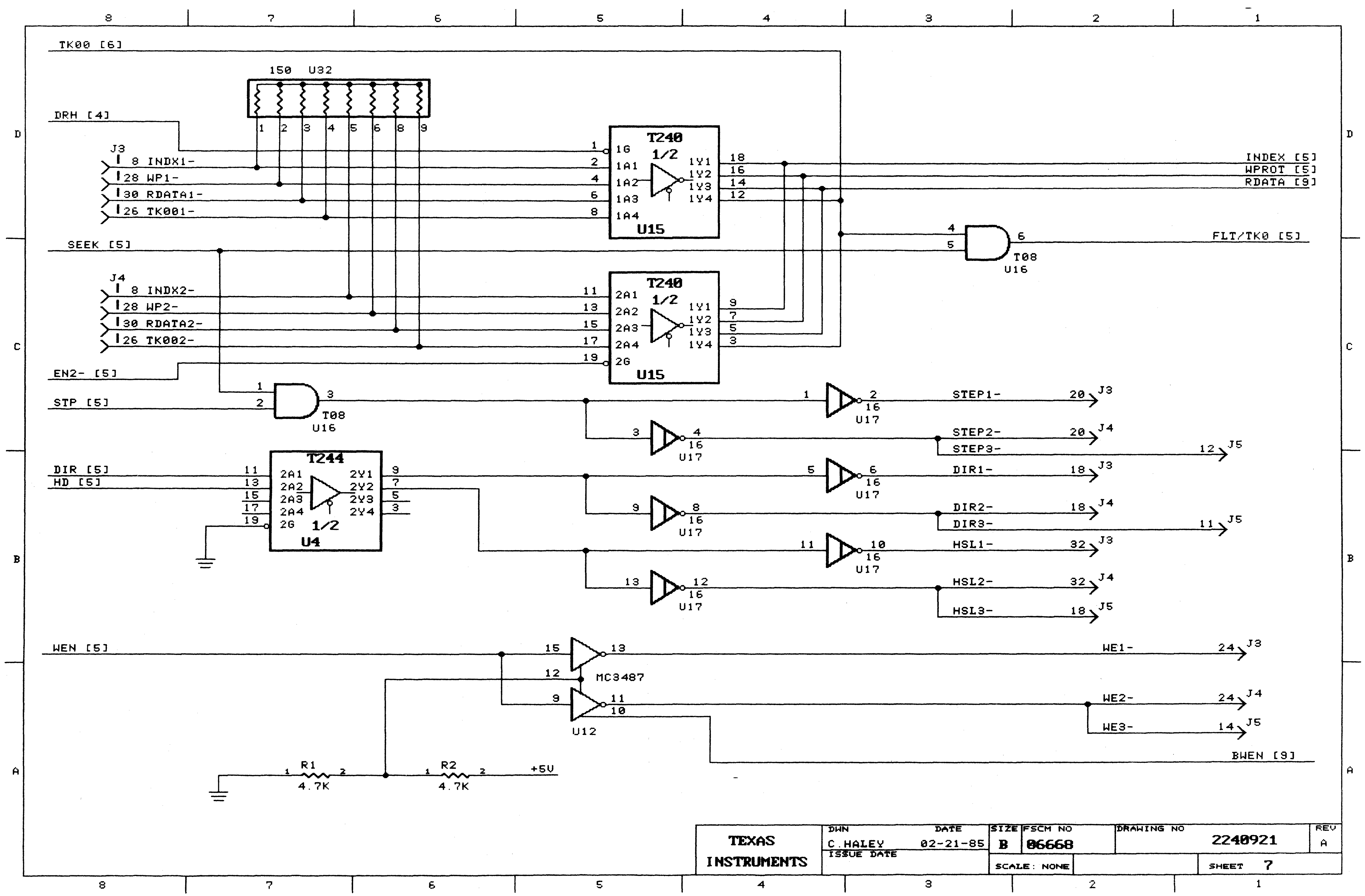

+5V
.1 C14
.1 C15
.1 C16
.1 C17
.1 C18
.1 C19
.1 C20
.1 C21
.1 C22
.1 C23
6.8 C1
.01 C24
.01 C25
.01 C26
.01 C27
.01 C28
.01 C29
.01 C30
.01 C31
.01 C32
.01 C33
.001 C34
.001 C35
.001 C36
.001 C37
.001 C38
.001 C39
.001 C40
.001 C41
.001 C42
.001 C43
.001 C44
DECOUPLING CAPACITORS
TEXAS INSTRUMENTS
DWN C.HALEY
DATE 02-21-85
ISSUE DATE
SIZE B
FSCM NO 06668
DRAWING NO 2240921
REV *
SCALE: NONE
SHEET 2

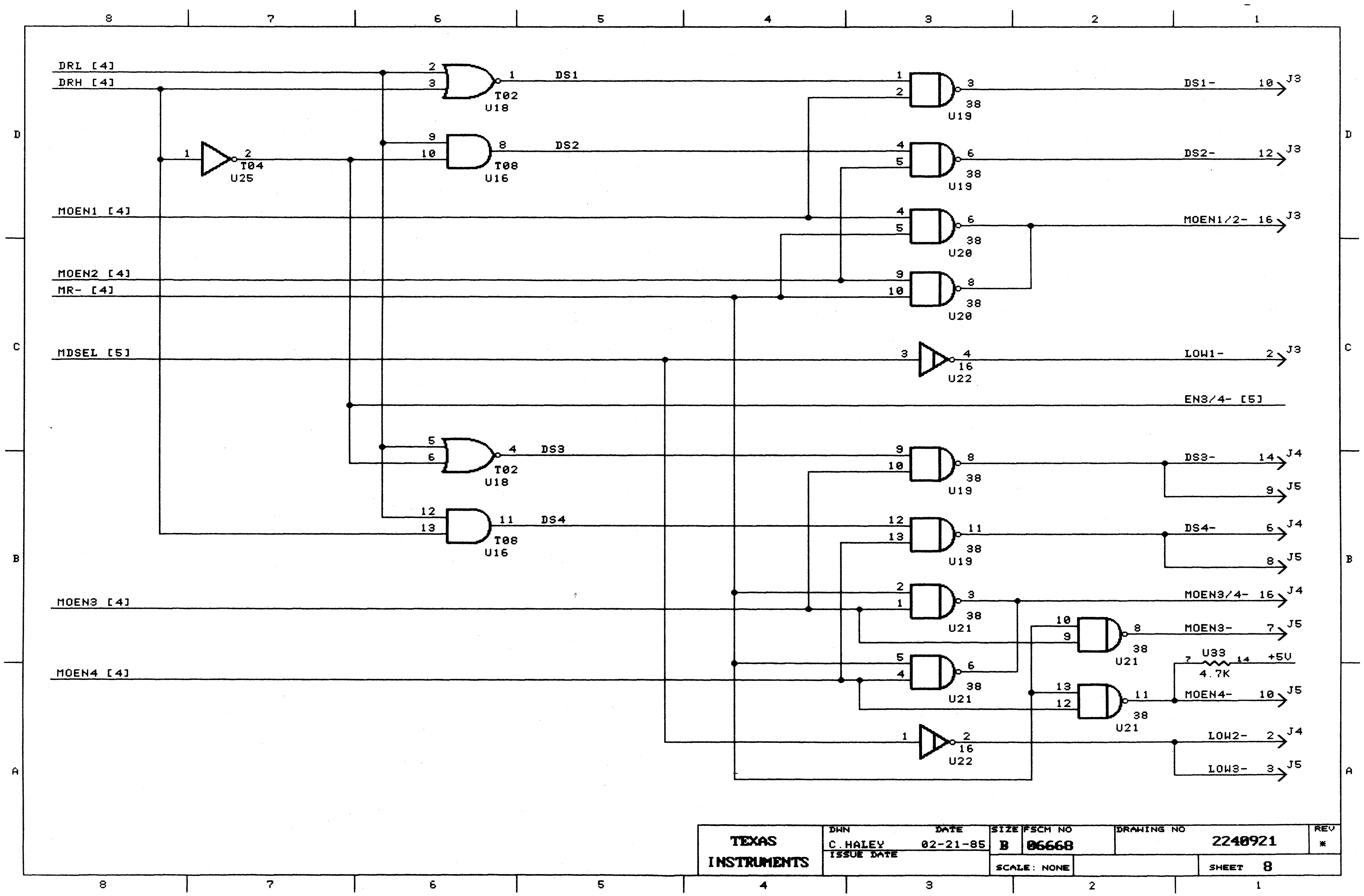

XDATA [4] (0-7)
CONN A B
XD7 3
XD6 5
XD5 7
XD4 9
XD3 11
XD2 13
XD1 15
XD0 17
AEN [4] 21
XA9 [4] 43
XA8 [4] 45
XA7 [4] 47
XA6 [4] 49
XA5 [4] 51
XA4 [4] 53
XA3 [4] 55
XA2 [4] 57
XA1 [4] 59
XA0 [4] 61
6 +5V
18 +12V
20 GND
58 +5V
62 GND
RESET [4]
DRQ2 [4]
IOWC- [4]
IORC- [4]
IR06 [4]
DACK2- [5]
T/C [5]
COMPONENT SIDE
P1
CONN C D
COMP SIDE
P2
J3
J4
J5
EXPANSION BUS CONNECTORS
TEXAS INSTRUMENTS
DWN C.HALEY
DATE 02-21-85
ISSUE DATE
SIZE B
FSCM NO 06668
DRAWING NO 2240921
REV *
SCALE: NONE
SHEET 3


PAL16L8
U3
T244
1/2
U4
T245
U6
T273
U5
AS74
U8
AEN [3]
XA8 [3]
XA6 [3]
XA5 [3]
XA4 [3]
XA3 [3]
XA9 [3]
XA7 [3]
XA2 [3]
XA1 [3]
XA0 [3]
IOWC- [3]
IORC- [3]
FINT [5]
FDACK- [5]
LDRQ [5]
RESET [3]
XDATA [3]
DCHG [6]
PUP8 [5]
PSEL
FDCS- [5]
MODE- [5]
BA0 [5]
BIOWC- [5]
BIORC- [5]
IR06 [3]
DRQ2 [3]
MR- [6]
MC3487
U12
DRL [8]
DRH [6]
FRST [5]
DMAEN [5]
MOEN1 [8]
MOEN2 [8]
MOEN3 [8]
MOEN4 [8]
BDATA <00:07>[5]
DIP-
IOEN-
DOR-
3-064027
3-052037
3-059061
3-102167
8-141177
T30
U2
AS04
U1
T244
U4
T04
U25
T125
U7
U33
4.7K
S1
+5V
TEXAS INSTRUMENTS
DWN C.HALEY
DATE 02-21-85
ISSUE DATE
SIZE B
FSCM NO 06668
DRAWING NO 2240921
REV C
SCALE: NONE
SHEET 4

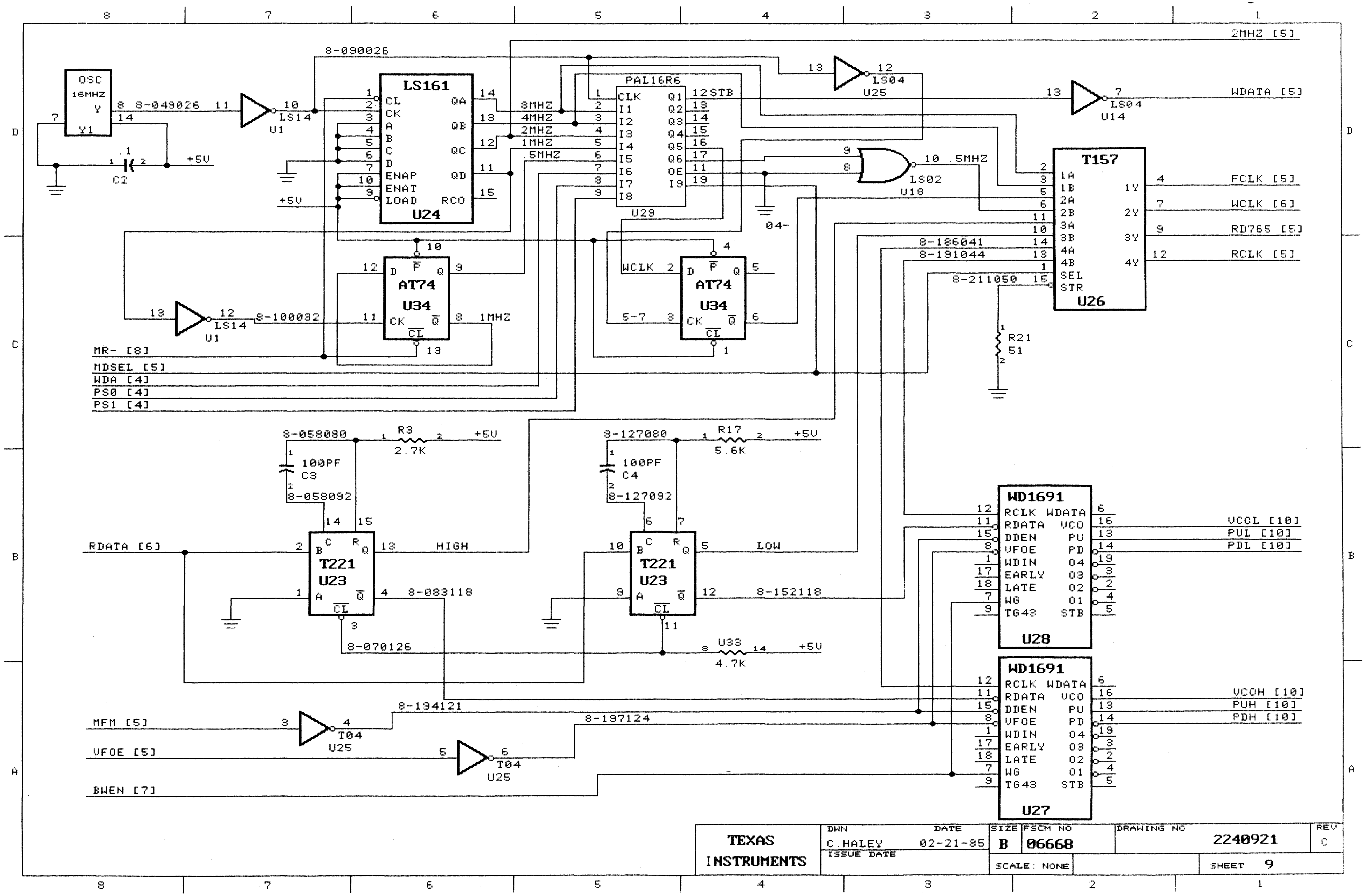

PAL16L8
U10
AT74
U9
T175
U13
74
U8
765A
U11
AS04
U1
S1
EN3/4- [8]
DMAEN [4]
FDCS- [4]
DACK2- [3]
T/C [3]
MODE- [4]
MR- [4]
2MHZ [9]
C16 [9]
C8 [9]
C4 [9]
FRST [4]
BDATA [4]
BIORC- [4]
BIOWC- [4]
BA0 [4]
FCLK [9]
EN2- [6][7]
EN3- [6]
FDACK- [4]
MDSEL [5][8][10]
MDSEL- [9]
PUP8 [4]
MSEL [9]
LDRQ [4]
FINT [4]
VFOE [9]
RCLK [9]
RD765 [9]
WDA [9]
PS1 [9]
PS0 [9]
WCLKP [9]
WEN [7]
HD [7]
DIR [7]
STP [7]
SEEK [7]
INDEX [6][7]
WPROT [6][7]
FLT/TK0 [7]
MFM [9]
TEXAS INSTRUMENTS
C.HALEY 02-21-85
B 06668
2240921
C
SCALE: NONE
SHEET 5

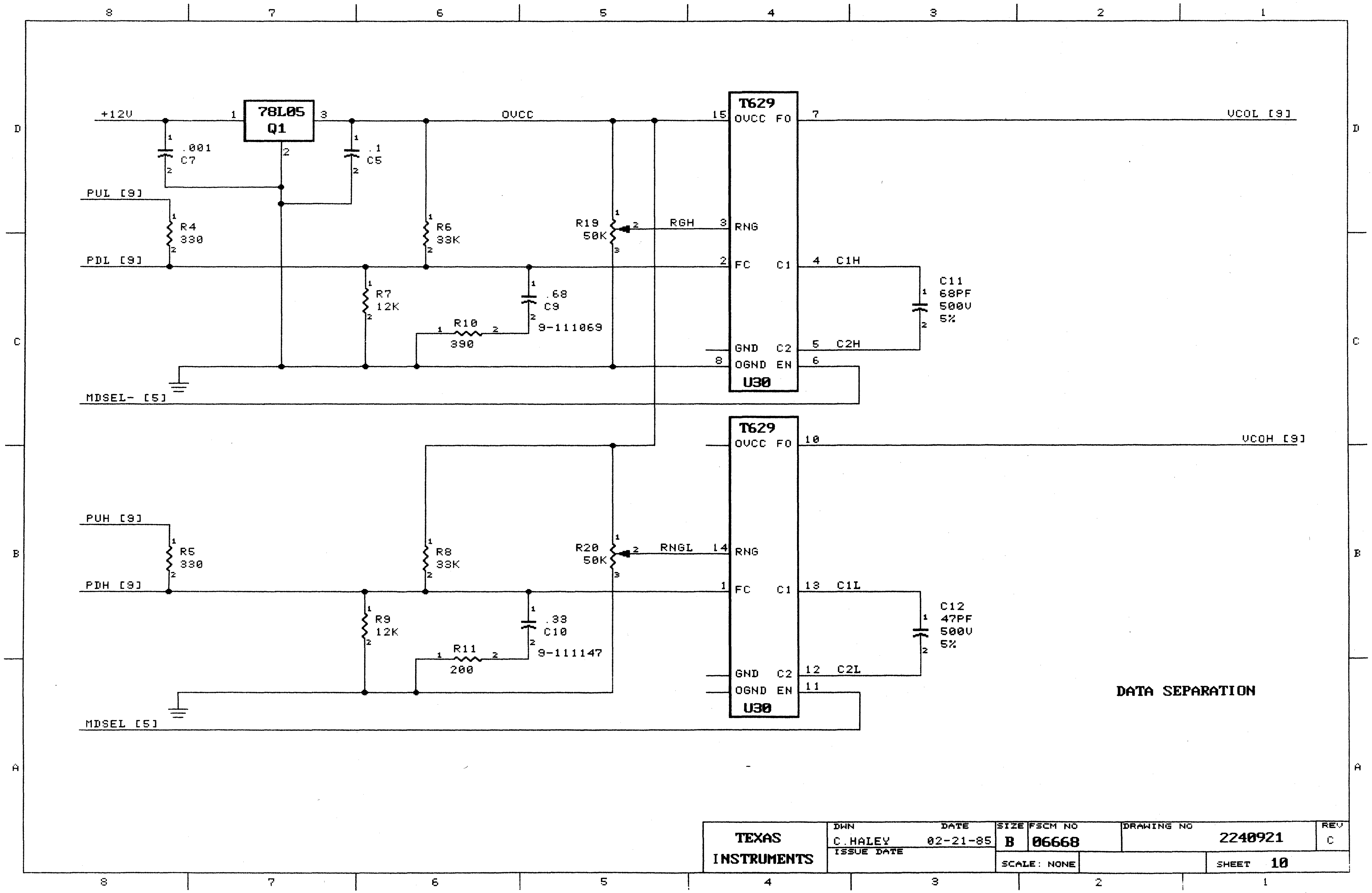

150 U32 14 +5V
10 11 12 13
J5
6 INDX3-
16 WP3-
17 RDATA3-
15 TK003-
T240
1/2
U14
INDEX [5]
WPROT [5]
RDATA [7][9]
TK00 [7]
EN3- [5]
+5V
R14 150
R15 150
R16 150
E7
E8
JP3
E9
J5 19 DCHG3-
J4 34 DCHG2-
J3 34 DCHG1-
T240
2A1 2A2 2A3 2G 2A4
2Y1 2Y2 2Y3 2Y4
1/2
U14
T125
U7
DCHG [4]
E4 JP2 E6
E5
E1 JP1 E3
E2
EN2- [5]
DRH [4][7][8]
WDATA [9]
MR- [4]
38
U20
WDATA1- 22 J3
WDATA2- 22 J4
WDATA3- 13 J5
TEXAS INSTRUMENTS
DWN C.HALEY DATE 02-21-85
ISSUE DATE
SIZE B FSCM NO 06668
DRAWING NO 2240921
REV C
SCALE: NONE
SHEET 6


TK00 [6]
DRH [4]
150 U32
J3
8 INDX1-
28 WP1-
30 RDATA1-
26 TK001-
T240
1/2
U15
INDEX [5]
WPROT [5]
RDATA [9]
SEEK [5]
FLT/TK0 [5]
T08
U16
J4
8 INDX2-
28 WP2-
30 RDATA2-
26 TK002-
EN2- [5]
STP [5]
DIR [5]
HD [5]
T244
1/2
U4
U17
STEP1-
STEP2-
STEP3-
DIR1-
DIR2-
DIR3-
HSL1-
HSL2-
HSL3-
WEN [5]
MC3487
U12
WE1-
WE2-
WE3-
BWEN [9]
R1
4.7K
R2
4.7K
+5V
TEXAS INSTRUMENTS
DWN C.HALEY
DATE 02-21-85
ISSUE DATE
SIZE B
FSCM NO 86668
DRAWING NO 2240921
REV A
SCALE: NONE
SHEET 7



DRL [4]
DRH [4]
DS1
DS2
MOEN1 [4]
MOEN2 [4]
MR- [4]
MDSEL [5]
DS3
DS4
MOEN3 [4]
MOEN4 [4]
DS1-
DS2-
MOEN1/2-
LOW1-
EN3/4- [5]
DS3-
DS4-
MOEN3/4-
MOEN3-
MOEN4-
LOW2-
LOW3-
+5V
4.7K
U33
TEXAS INSTRUMENTS
DWN C.HALEY
DATE 02-21-85
ISSUE DATE
SIZE B
FSCM NO 06668
DRAWING NO 2240921
REV *
SCALE: NONE
SHEET 8


OSC 16MHZ
LS161
U24
PAL16R6
U29
LS04
U25
U14
T157
U26
LS02
U18
AT74
U34
LS14
U1
T221
U23
WD1691
U28
U27
T04
2MHZ [5]
WDATA [5]
FCLK [5]
WCLK [6]
RD765 [5]
RCLK [5]
MR- [8]
MDSEL [5]
WDA [4]
PS0 [4]
PS1 [4]
RDATA [6]
MFM [5]
VFOE [5]
BWEN [7]
VCOL [10]
PUL [10]
PDL [10]
VCOH [10]
PUH [10]
PDH [10]
TEXAS INSTRUMENTS
C.HALEY 02-21-85
B 06668
2240921
SHEET 9


+12V
78L05
Q1
.001
C7
.1
C5
OVCC
T629
OVCC FO
VCOL [9]
PUL [9]
R4
330
R6
33K
R19
50K
RGH
RNG
PDL [9]
FC C1
C1H
C11
68PF
500V
5%
R7
12K
.68
C9
R10
390
9-111069
GND C2
OGND EN
C2H
U30
MDSEL- [5]
T629
OVCC FO
VCOH [9]
PUH [9]
R5
330
R8
33K
R20
50K
RNGL
RNG
PDH [9]
FC C1
C1L
C12
47PF
500V
5%
R9
12K
.33
C10
R11
200
9-111147
GND C2
OGND EN
C2L
U30
DATA SEPARATION
MDSEL [5]
TEXAS INSTRUMENTS
DWN C.HALEY
DATE 02-21-85
ISSUE DATE
SIZE B
FSCM NO 06668
DRAWING NO 2240921
REV C
SCALE: NONE
SHEET 10

2240924 DRAWING NO | 1 SH

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	ECN538271 (C) ESPINOZA 7-8-85	8-15-85	A. VENEGAS
B	CN 549645 (B) D.JONES	12-2-85	C. KEELER
C	CN 549697 (E) D.JONES	12-2-85	C. KEELER

NOTES, UNLESS OTHERWISE SPECIFIED:

1. ALL DEVICES ARE PREFIXED WITH SN74. A LETTER "T" IN A PREFIX IS EQUAL TO "LS", EXCEPT WHEN USED AS A SUFFIX. "AT" IS EQUAL TO "ALS", AND A LETTER "F" AS A SUFFIX IS EQUAL TO A CHIP CARRIER
2. VCC IS APPLIED TO PIN 8 OF ALL 8-PIN IC's, PIN 14 OF ALL 14-PIN IC's, PIN 16 OF ALL 16-PIN IC's, PIN 20 OF ALL 20-PIN IC's, ETC
3. GROUND IS APPLIED TO PIN 4 OF ALL 8-PIN IC's, PIN 7 OF ALL 14-PIN IC's, PIN 8 OF ALL 16-PIN IC's, PIN 10 OF ALL 20-PIN IC's, ETC
4. DEVICE TYPE, PIN NUMBERS, AND REFERENCE DESIGNATOR OF GATES ARE SHOWN AS FOLLOWS:

00 AND 04 = DEVICE TYPES
1, 2, AND 3 = PIN NUMBERS
U06 AND U07 = REFERENCE DESIGNATORS

5. RESISTANCE VALUES ARE IN OHMS
6. RESISTORS ARE 1/4 WATT, 5%
7. CAPACITANCE VALUES ARE IN MICROFARADS
8. CAPACITORS ARE 50V

29

COMPUTER GENERATED DRAWING ; DO NOT REVISE MANUALLY

-1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES

PARTS LIST

REV	A	C	A							
SH	11	12	13							
REV	C	A	A	A	A	C		C	C	A
SH	1	2	3	4	5	6	7	8	9	10

REVISION STATUS OF SHEETS

2240925	8721
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
* DIMENSIONS ARE IN INCHES
* TOLERANCES: ANGLES +/-1 DEG
3 PLACE DECIMALS +/-.010
2 PLACE DECIMALS +/-.02
* INTERPRET DRAWING PER MIL-D-1000
* REMOVE BURRS AND SHARP EDGES
* CONCENTRICITY MACHINED DIAMETERS .010 FIM
* DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
* PARENTHETICAL INFO FOR REF ONLY

HOLE TOLERANCE

.013 THRU .125 +.004 -.001	.126 THRU .250 +.005 -.001	.251 THRU .500 +.006 -.001
.501 THRU .750 +.008 -.001	.751 THRU 1.000 +.010 -.001	1.001 THRU 2.000 +.012 -.001

		DATE
DWN	C.HALEY	02-20-85
CHK	F.PETERSON	04-18-85
ENGR	C.HALEY	04-19-85
APVD ENGR	C.HALEY	04-19-85
QA	W.DILLER	04-29-85
APVD MFG	R.LEVERETT	04-22-85
RELEASE	F.PETERSON	04-29-85

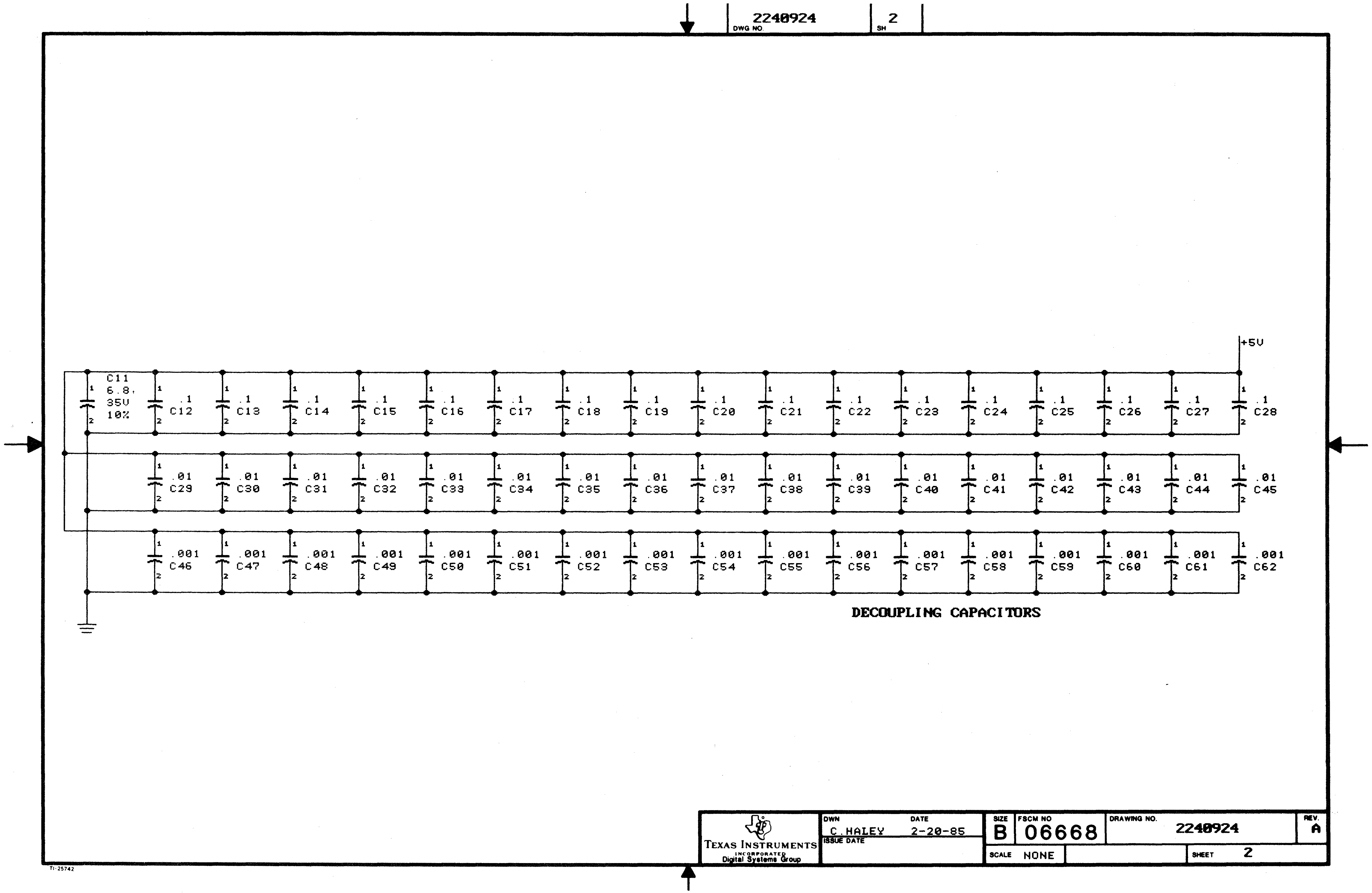
TEXAS INSTRUMENTS
Data Systems Group

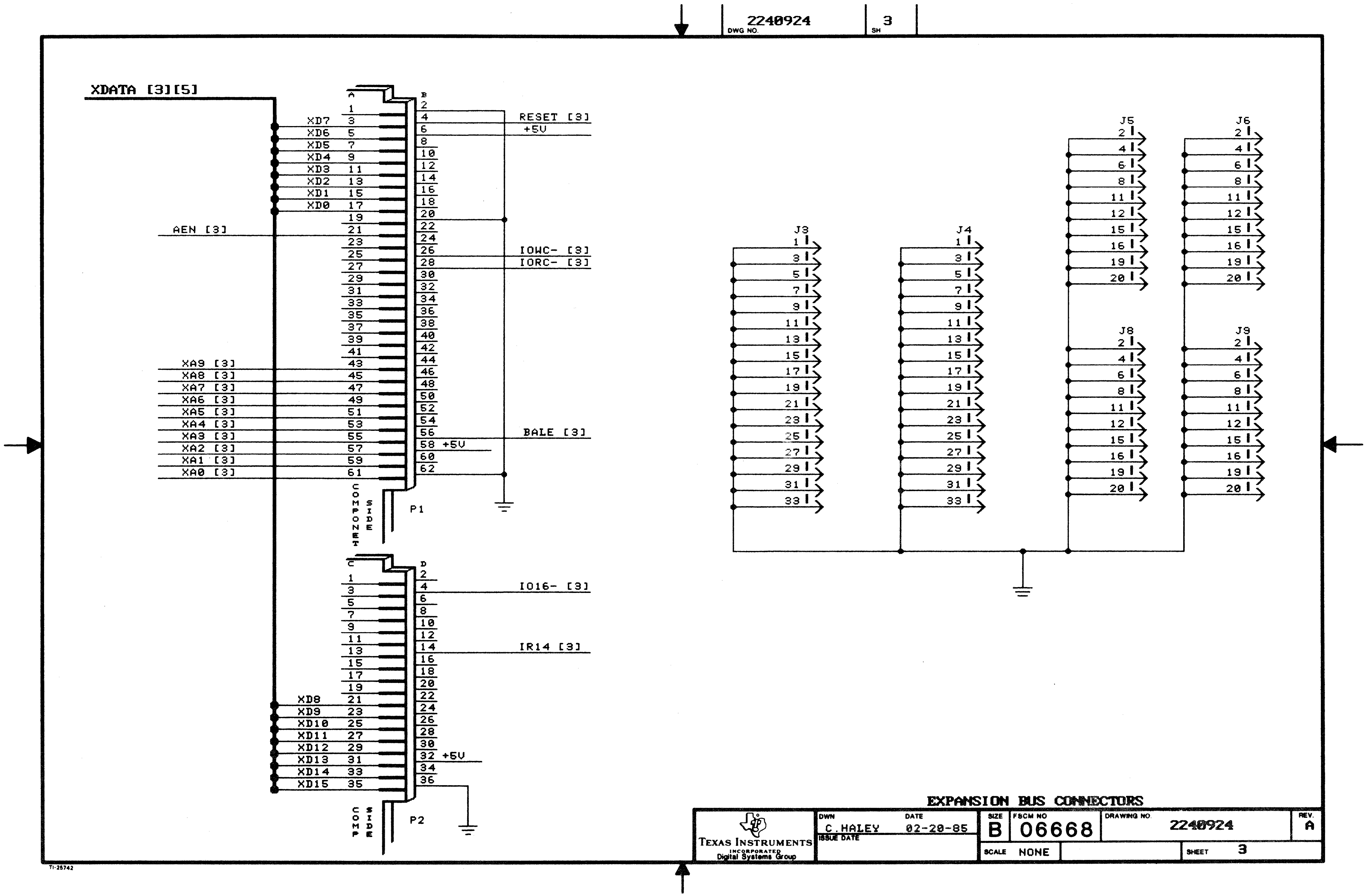
DIAGRAM, LOGIC, DETAILED-
WINCHESTER CONTROLLER-
EXECALIBUR

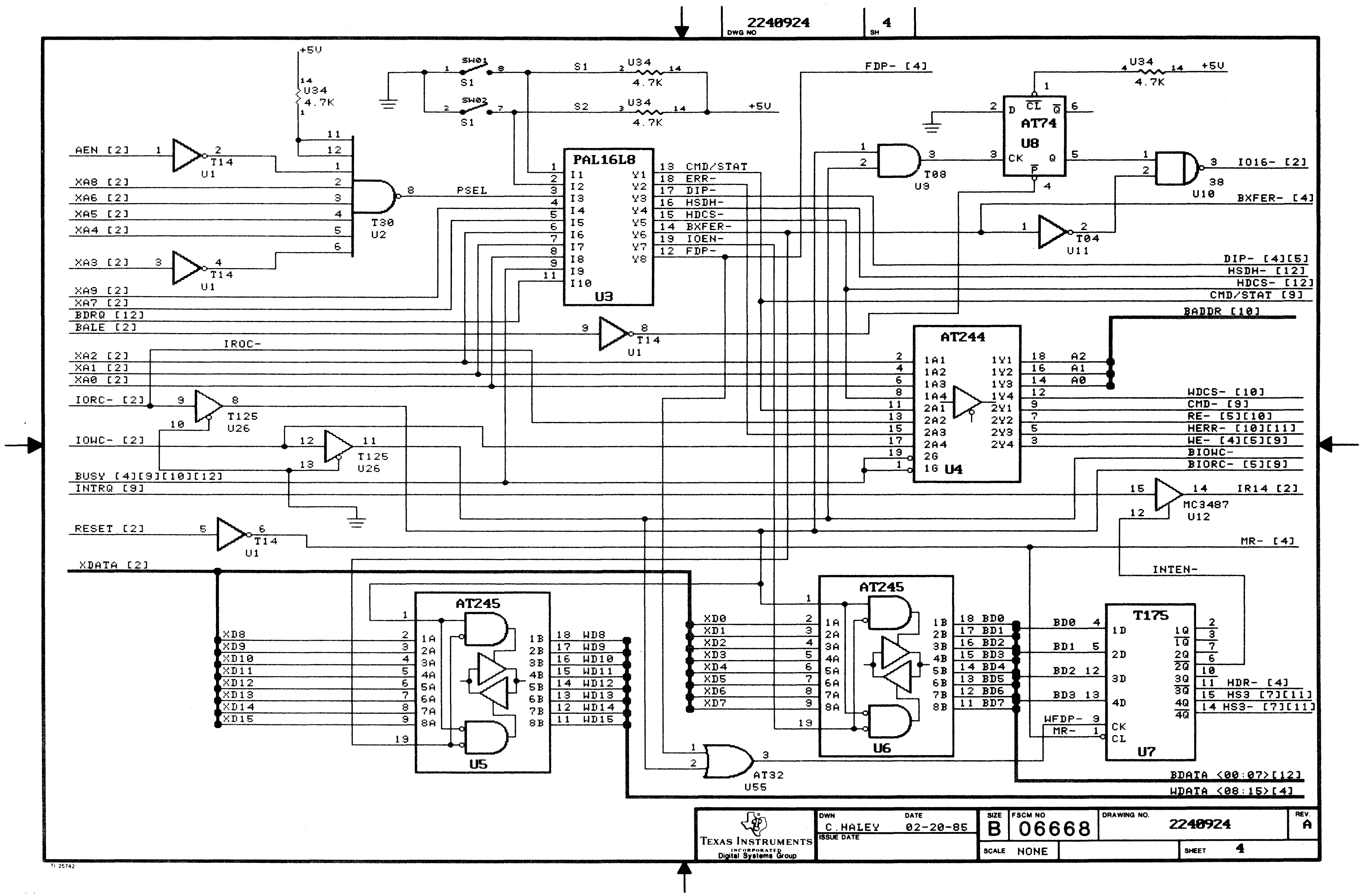
SIZE	FSCM NO	DRAWING NO
B	06668	2240924

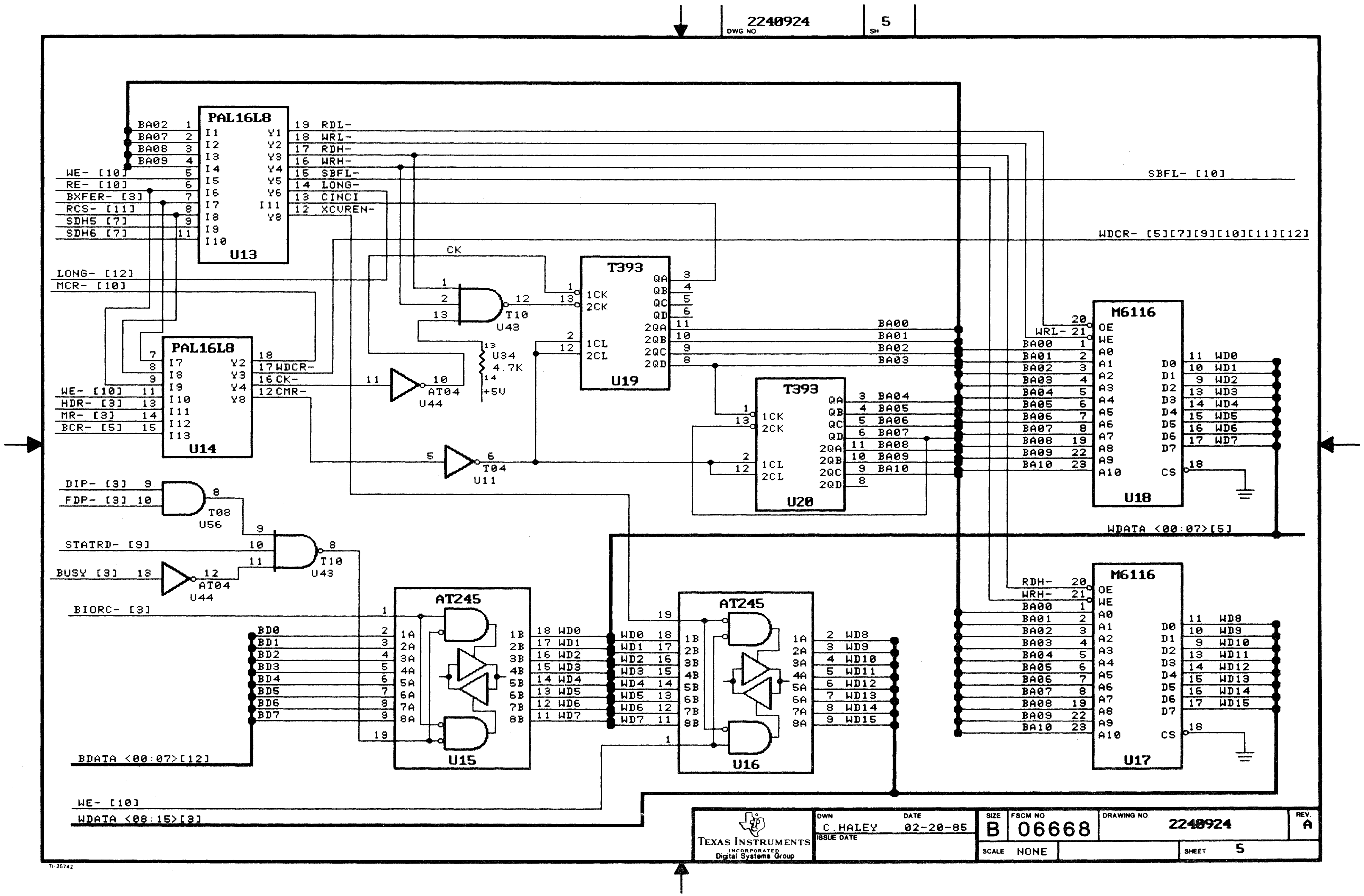
SCALE NONE | SHEET 1 OF 13

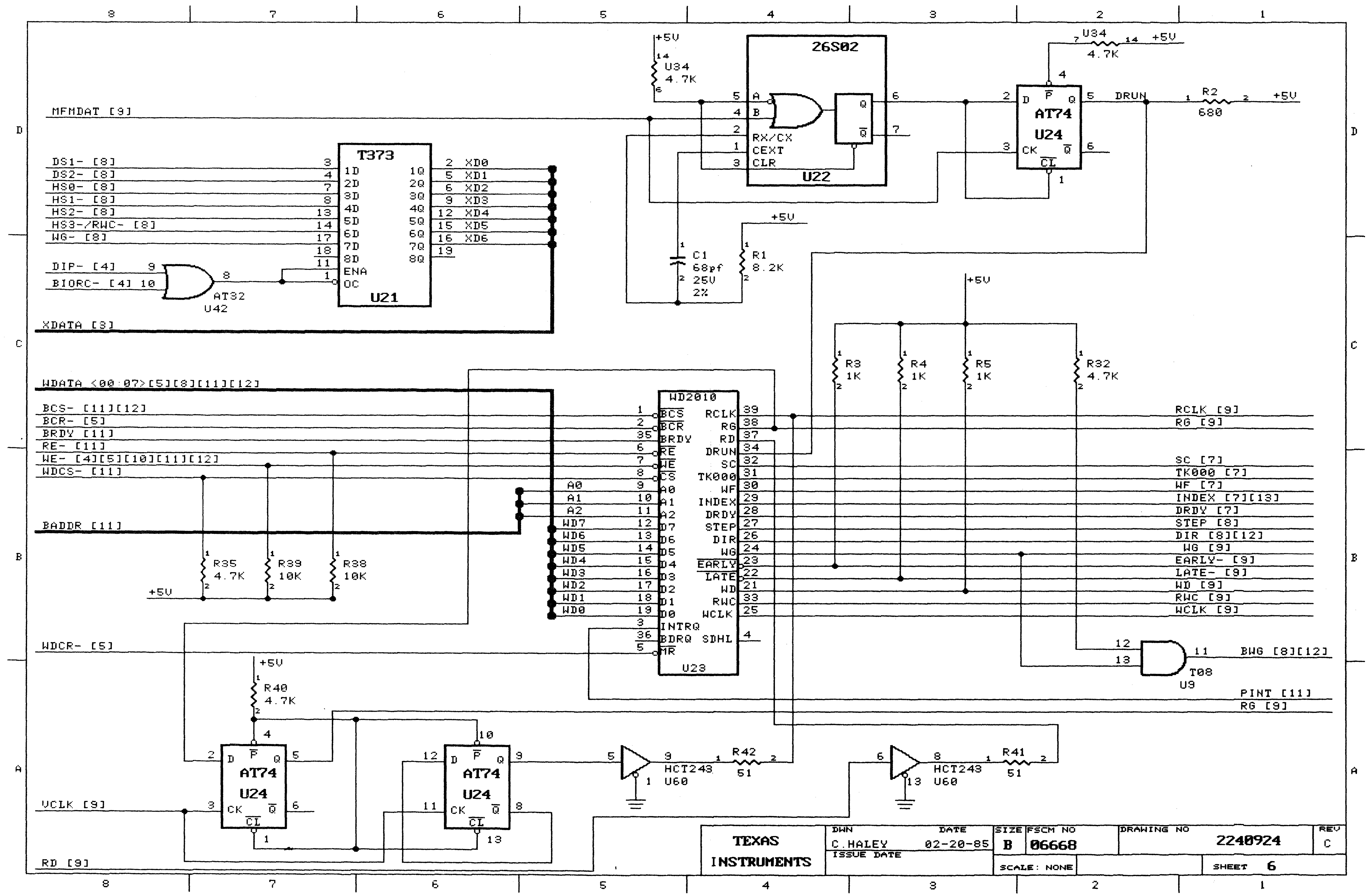
430 DB 7-08-85

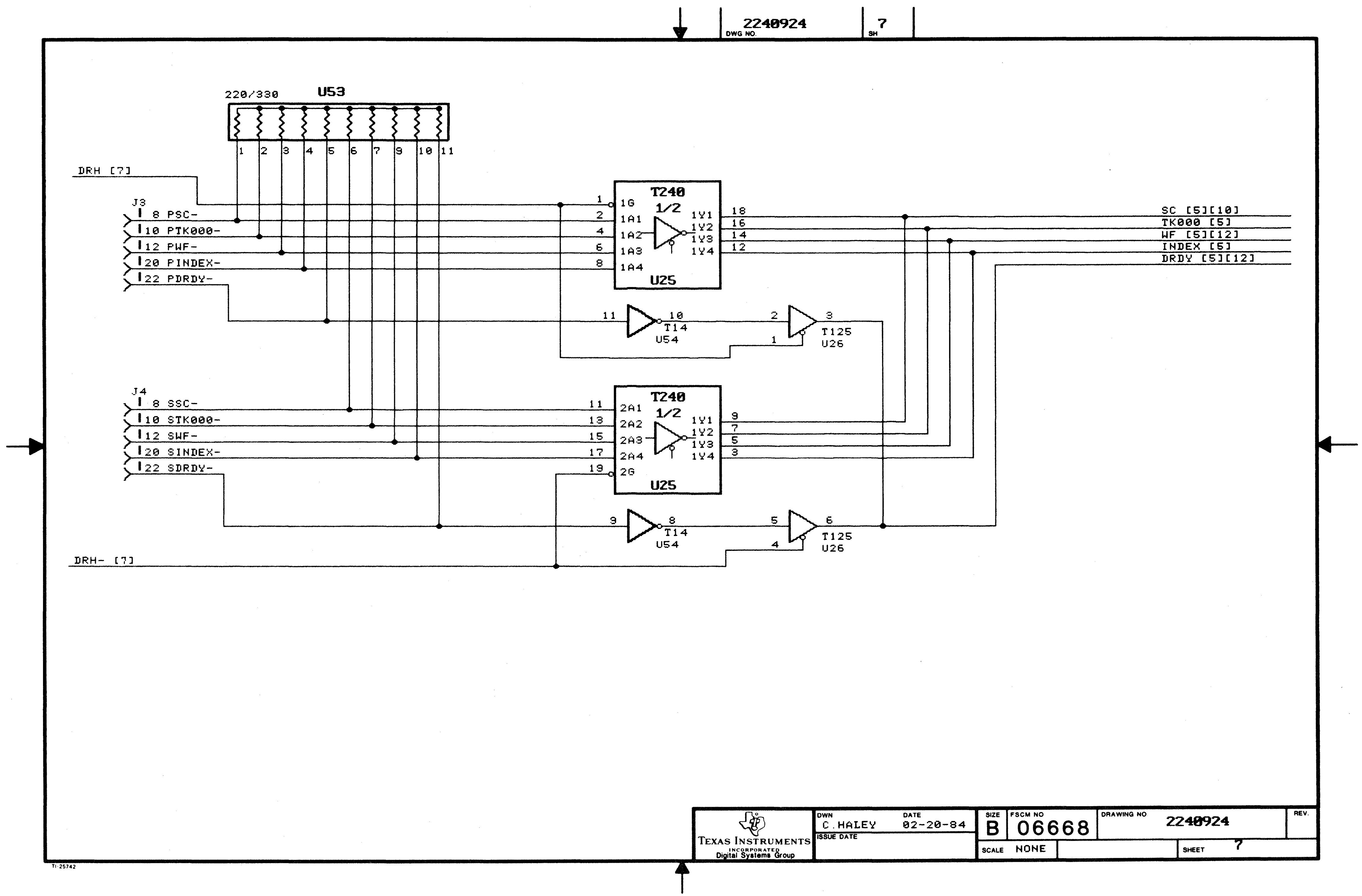

2240924
DWG NO
SH 2
+5V
C11
6.8,
35V
10%
.1 C12
.1 C13
.1 C14
.1 C15
.1 C16
.1 C17
.1 C18
.1 C19
.1 C20
.1 C21
.1 C22
.1 C23
.1 C24
.1 C25
.1 C26
.1 C27
.1 C28
.01 C29
.01 C30
.01 C31
.01 C32
.01 C33
.01 C34
.01 C35
.01 C36
.01 C37
.01 C38
.01 C39
.01 C40
.01 C41
.01 C42
.01 C43
.01 C44
.01 C45
.001 C46
.001 C47
.001 C48
.001 C49
.001 C50
.001 C51
.001 C52
.001 C53
.001 C54
.001 C55
.001 C56
.001 C57
.001 C58
.001 C59
.001 C60
.001 C61
.001 C62
DECOUPLING CAPACITORS
TEXAS INSTRUMENTS
INCORPORATED
Digital Systems Group
DWN C. HALEY
DATE 2-20-85
ISSUE DATE
SIZE B
FSCM NO 06668
DRAWING NO. 2240924
REV. A
SCALE NONE
SHEET 2

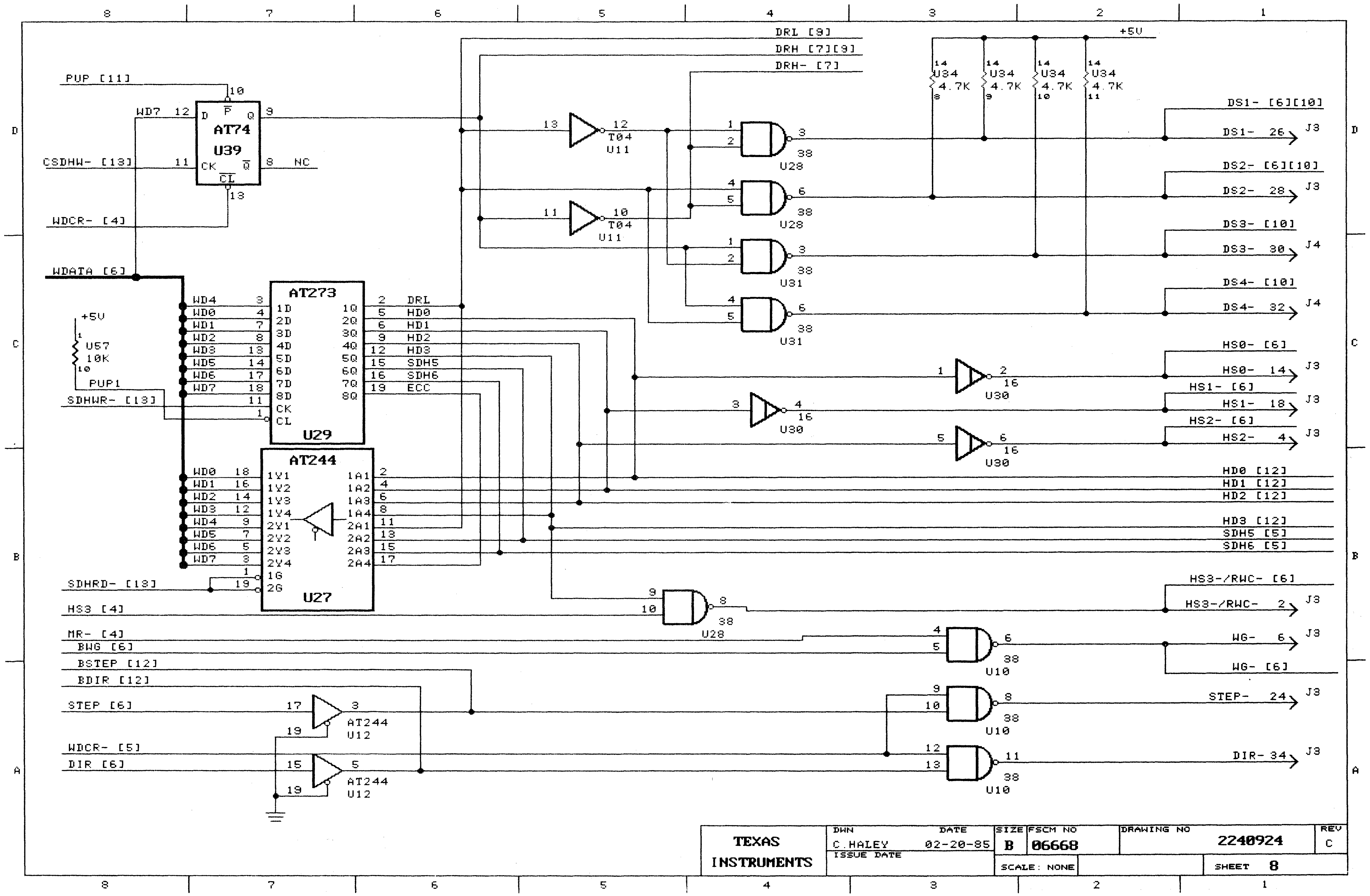

2240924
DWG NO.
3
SH
XDATA [3][5]
XD7
XD6
XD5
XD4
XD3
XD2
XD1
XD0
AEN [3]
XA9 [3]
XA8 [3]
XA7 [3]
XA6 [3]
XA5 [3]
XA4 [3]
XA3 [3]
XA2 [3]
XA1 [3]
XA0 [3]
RESET [3]
+5V
IOWC- [3]
IORC- [3]
BALE [3]
+5V
COMPONENT SIDE
P1
IO16- [3]
IR14 [3]
XD8
XD9
XD10
XD11
XD12
XD13
XD14
XD15
+5V
COMP SIDE
P2
J3
J4
J5
J6
J8
J9
EXPANSION BUS CONNECTORS
TEXAS INSTRUMENTS
INCORPORATED
Digital Systems Group
DWN
C.HALEY
DATE
02-20-85
ISSUE DATE
SIZE
B
FSCM NO
06668
DRAWING NO
2240924
REV.
A
SCALE
NONE
SHEET
3
TI-25742

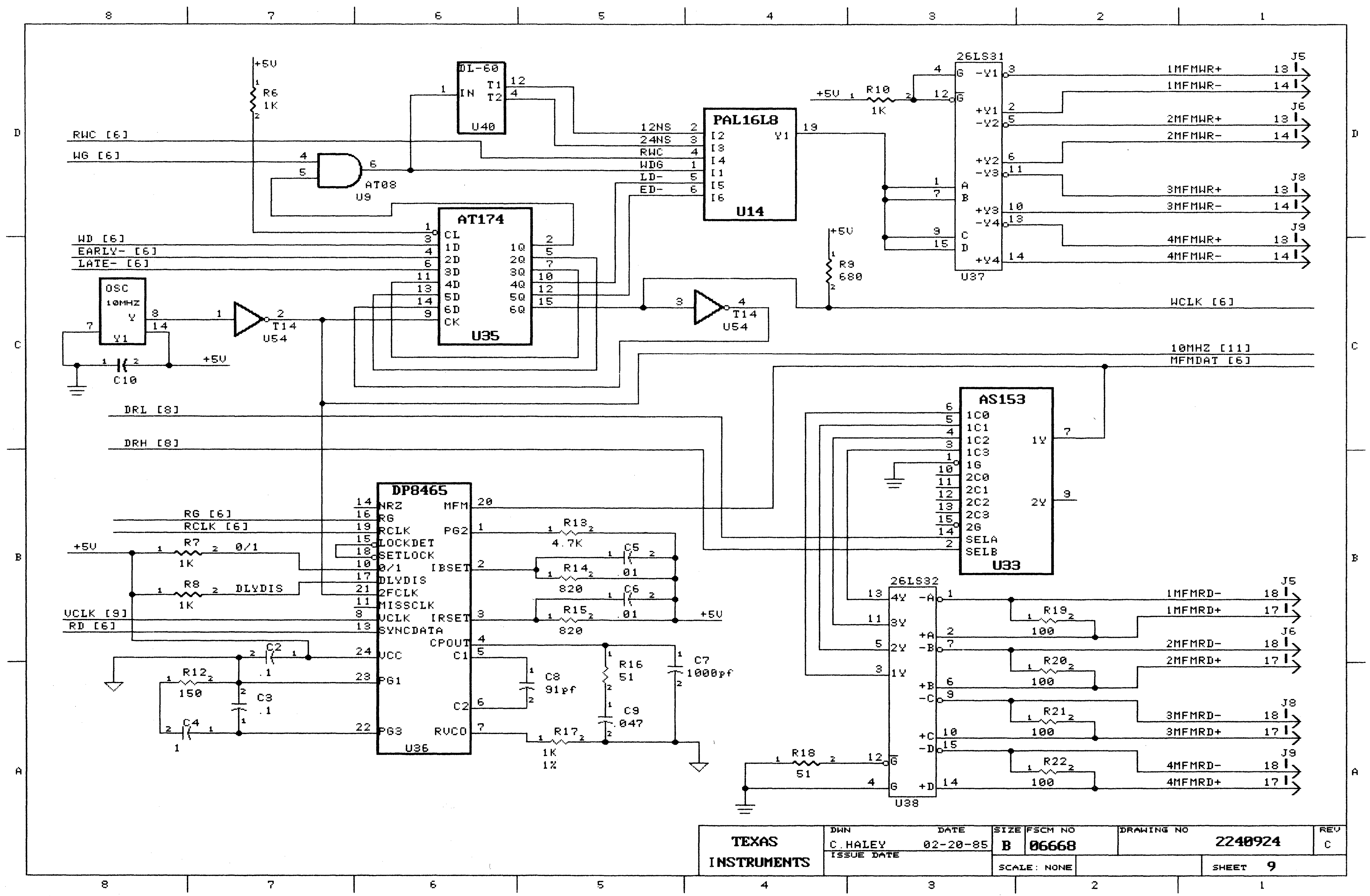

2240924
4
PAL16L8
U3
AT74
U8
AT244
U4
AT245
U5
AT245
U6
T175
U7
AT32
U55
MC3487
U12
TEXAS INSTRUMENTS
Digital Systems Group
C.HALEY
02-20-85
B
06668
2240924
A
NONE
4
BDATA <00:07>[12]
WDATA <08:15>[4]

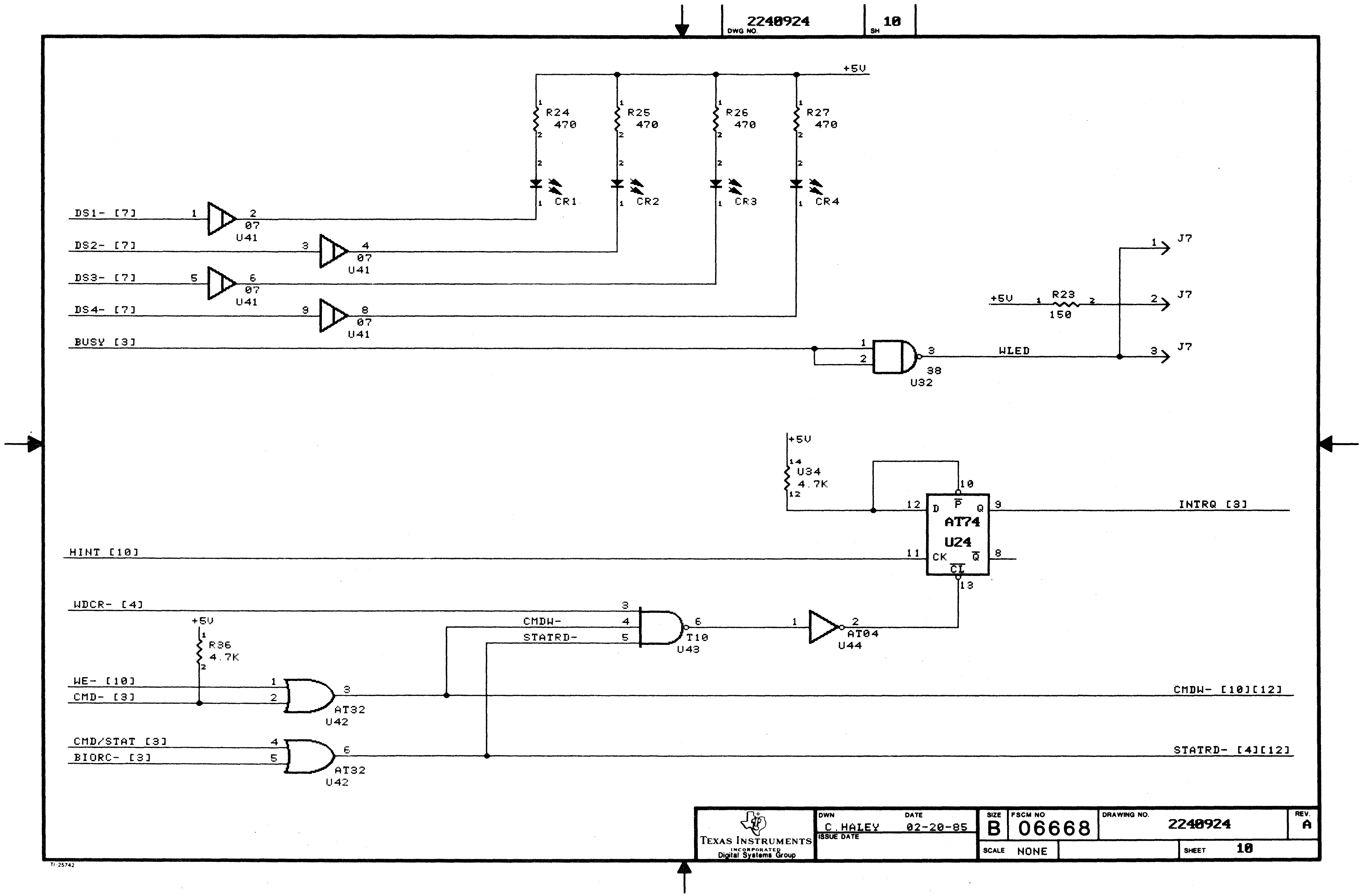

2240924
DWG NO.
5
SH
PAL16L8
U13
BA02
BA07
BA08
BA09
WE- [10]
RE- [10]
BXFER- [3]
RCS- [11]
SDH5 [7]
SDH6 [7]
RDL-
WRL-
RDH-
WRH-
SBFL-
LONG-
CINCI
XCVREN-
SBFL- [10]
WDCR- [5][7][9][10][11][12]
CK
LONG- [12]
MCR- [10]
T10
U43
U34
4.7K
+5V
T393
U19
BA00
BA01
BA02
BA03
PAL16L8
U14
WDCR-
CK-
CMR-
WE- [10]
HDR- [3]
MR- [3]
BCR- [5]
AT04
U44
T04
U11
T393
U20
BA04
BA05
BA06
BA07
BA08
BA09
BA10
M6116
U18
WD0
WD1
WD2
WD3
WD4
WD5
WD6
WD7
WDATA <00:07>[5]
DIP- [3]
FDP- [3]
T08
U56
STATRD- [9]
BUSY [3]
T10
U43
AT04
U44
BIORC- [3]
AT245
U15
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
BDATA <00:07>[12]
AT245
U16
WD8
WD9
WD10
WD11
WD12
WD13
WD14
WD15
M6116
U17
RDH-
WRH-
WE- [10]
WDATA <08:15>[3]
TEXAS INSTRUMENTS
INCORPORATED
Digital Systems Group
DWN
C. HALEY
DATE
02-20-85
ISSUE DATE
SIZE
B
FSCM NO
06668
DRAWING NO.
2240924
REV.
A
SCALE
NONE
SHEET
5
TI-25742

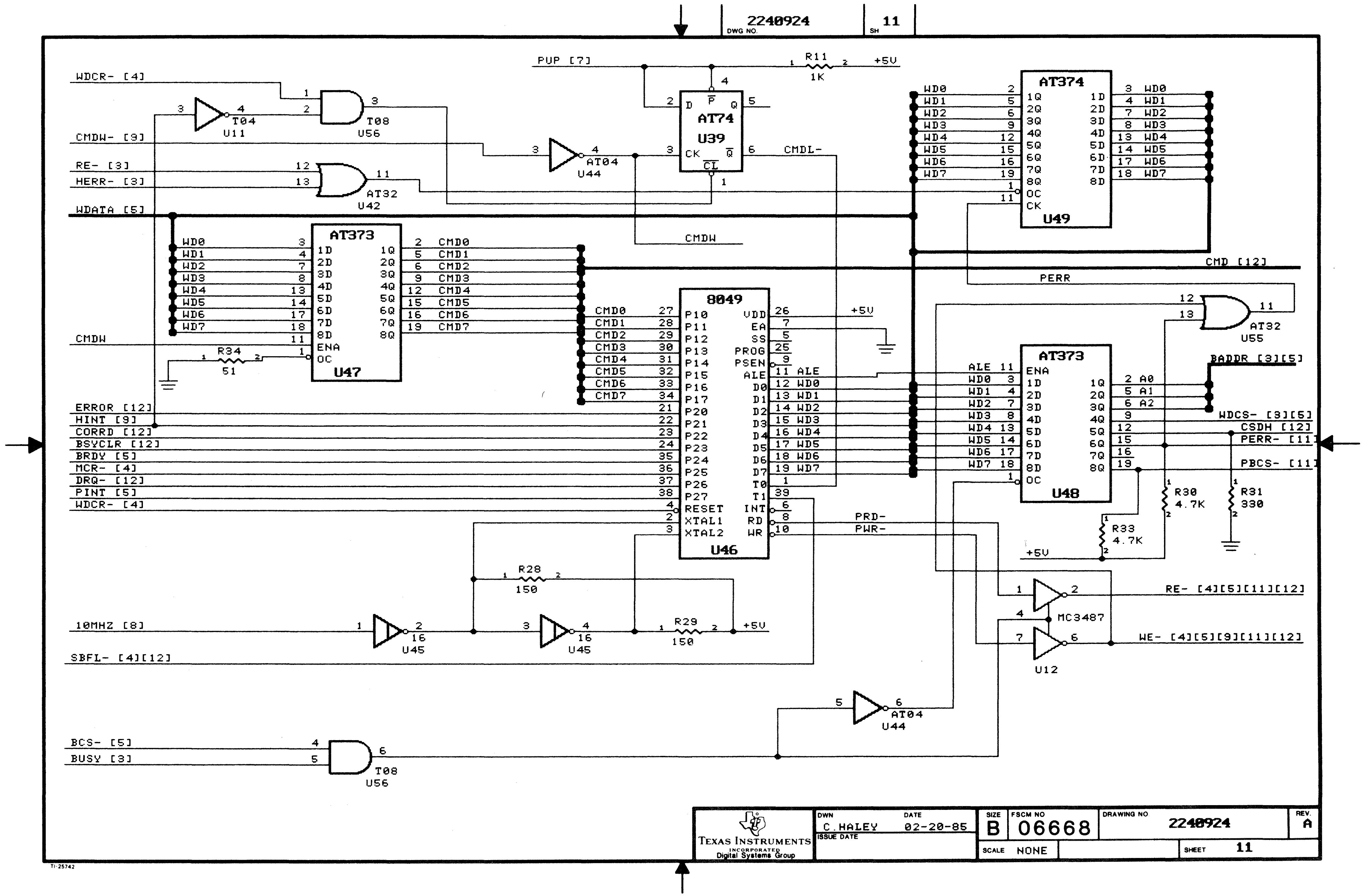

26S02
U22
T373
U21
WD2010
U23
AT74
U24
MFMDAT [9]
XDATA [3]
WDATA <00:07>[5][8][11][12]
BADDR [11]
WDCR- [5]
VCLK [9]
RD [9]
RCLK [9]
RG [9]
BWG [8][12]
PINT [11]
TEXAS INSTRUMENTS
C.HALEY 02-20-85
2240924
SHEET 6

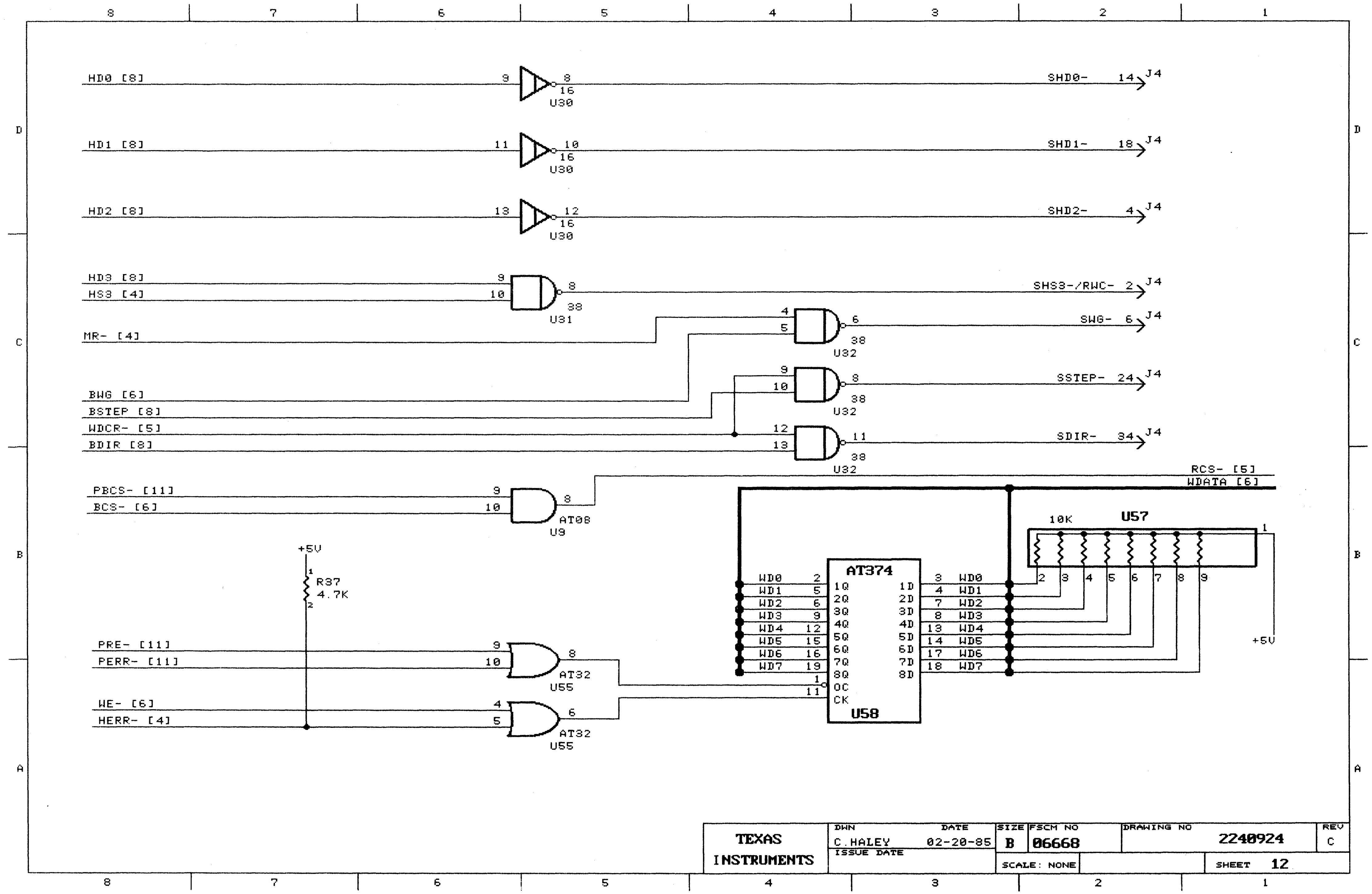

2240924
DWG NO.
7
SH
220/330
U53
DRH [7]
J3
8 PSC-
10 PTK000-
12 PWF-
20 PINDEX-
22 PDRDY-
T240
1/2
U25
SC [5][10]
TK000 [5]
WF [5][12]
INDEX [5]
DRDY [5][12]
T14
U54
T125
U26
J4
8 SSC-
10 STK000-
12 SWF-
20 SINDEX-
22 SDRDY-
DRH- [7]
TEXAS INSTRUMENTS
INCORPORATED
Digital Systems Group
DWN
C.HALEY
DATE
02-20-84
ISSUE DATE
SIZE
B
FSCM NO
06668
DRAWING NO
2240924
REV.
SCALE
NONE
SHEET
7


PUP [11]
WD7
CSDHW- [13]
WDCR- [4]
WDATA [6]
AT74
U39
NC
+5V
U57
10K
PUP1
SDHWR- [13]
AT273
U29
AT244
U27
DRL
HD0
HD1
HD2
HD3
SDH5
SDH6
ECC
DRL [9]
DRH [7][9]
DRH- [7]
T04
U11
U28
U31
U30
U34
4.7K
DS1- [6][10]
DS1- 26
DS2- [6][10]
DS2- 28
DS3- [10]
DS3- 30
DS4- [10]
DS4- 32
J3
J4
HS0- [6]
HS0- 14
HS1- [6]
HS1- 18
HS2- [6]
HS2- 4
HD0 [12]
HD1 [12]
HD2 [12]
HD3 [12]
SDH5 [5]
SDH6 [5]
SDHRD- [13]
HS3 [4]
HS3-/RWC- [6]
HS3-/RWC- 2
MR- [4]
BWG [6]
BSTEP [12]
BDIR [12]
STEP [6]
WDCR- [5]
DIR [6]
AT244
U12
U10
WG- 6
WG- [6]
STEP- 24
DIR- 34
TEXAS INSTRUMENTS
DWN C.HALEY
DATE 02-20-85
ISSUE DATE
SIZE B
FSCM NO 06668
SCALE: NONE
DRAWING NO 2240924
REV C
SHEET 8

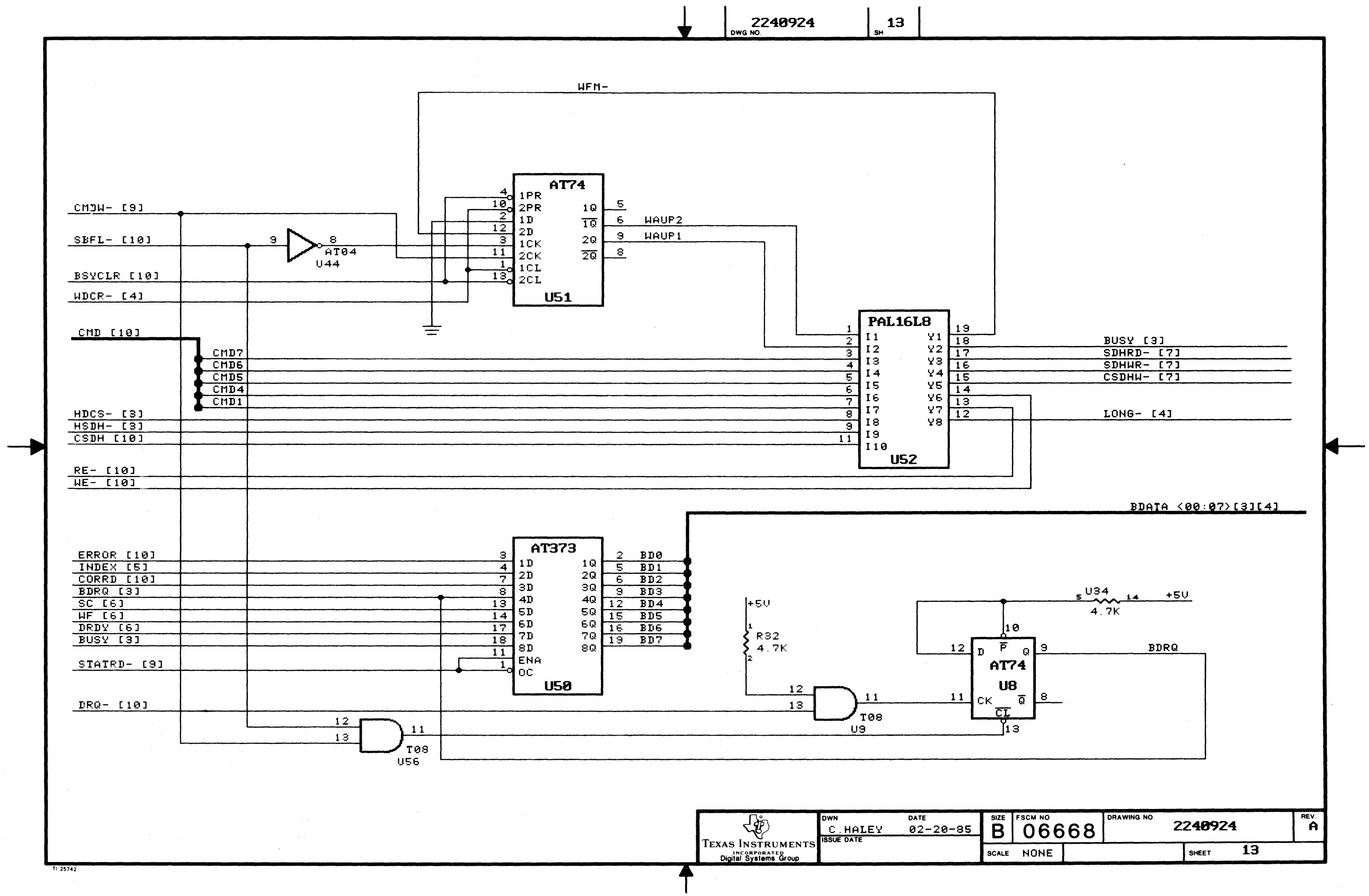

DL-60
U40
PAL16L8
U14
26LS31
U37
AT08
U9
AT174
U35
OSC 10MHZ
U54
AS153
U33
DP8465
U36
26LS32
U38
RWC [6]
WG [6]
WD [6]
EARLY- [6]
LATE- [6]
DRL [8]
DRH [8]
RG [6]
RCLK [6]
VCLK [9]
RD [6]
WCLK [6]
10MHZ [11]
MFMDAT [6]
1MFMWR+
1MFMWR-
2MFMWR+
2MFMWR-
3MFMWR+
3MFMWR-
4MFMWR+
4MFMWR-
1MFMRD-
1MFMRD+
2MFMRD-
2MFMRD+
3MFMRD-
3MFMRD+
4MFMRD-
4MFMRD+
J5
J6
J8
J9
TEXAS INSTRUMENTS
DWN C.HALEY
DATE 02-20-85
ISSUE DATE
SIZE B
FSCM NO 06668
DRAWING NO 2240924
REV C
SCALE: NONE
SHEET 9


2240924 DWG NO.
10 SH
+5V
R24 470
R25 470
R26 470
R27 470
CR1
CR2
CR3
CR4
DS1- [7]
DS2- [7]
DS3- [7]
DS4- [7]
07 U41
BUSY [3]
38 U32
WLED
+5V R23 150
J7
+5V U34 4.7K
AT74 U24
INTRQ [3]
HINT [10]
WDCR- [4]
CMDW-
STATRD-
T10 U43
AT04 U44
+5V R36 4.7K
WE- [10]
CMD- [3]
AT32 U42
CMDW- [10][12]
CMD/STAT [3]
BIORC- [3]
STATRD- [4][12]
TEXAS INSTRUMENTS INCORPORATED Digital Systems Group
DWN C. HALEY
DATE 02-20-85
ISSUE DATE
SIZE B
FSCM NO 06668
DRAWING NO. 2240924
REV. A
SCALE NONE
SHEET 10


2240924
11
PUP [7]
R11
1K
+5V
WDCR- [4]
T04
U11
T08
U56
CMDW- [9]
AT04
U44
AT74
U39
CMDL-
RE- [3]
HERR- [3]
AT32
U42
WDATA [5]
AT373
U47
WD0
WD1
WD2
WD3
WD4
WD5
WD6
WD7
CMD0
CMD1
CMD2
CMD3
CMD4
CMD5
CMD6
CMD7
CMDW
R34
51
AT374
U49
CMD [12]
PERR
AT32
U55
8049
U46
VDD
EA
SS
PROG
PSEN
ALE
RESET
XTAL1
XTAL2
INT
RD
WR
AT373
U48
BADDR [3][5]
A0
A1
A2
WDCS- [3][5]
CSDH [12]
PERR- [11]
PBCS- [11]
R30
4.7K
R31
330
R33
4.7K
ERROR [12]
HINT [9]
CORRD [12]
BSYCLR [12]
BRDY [5]
MCR- [4]
DRQ- [12]
PINT [5]
WDCR- [4]
PRD-
PWR-
R28
150
R29
150
10MHZ [8]
U45
SBFL- [4][12]
MC3487
U12
RE- [4][5][11][12]
WE- [4][5][9][11][12]
AT04
U44
BCS- [5]
BUSY [3]
T08
U56
Texas Instruments
Digital Systems Group
C.HALEY
02-20-85
B
06668
2240924
A
NONE
11



HD0 [8]
HD1 [8]
HD2 [8]
HD3 [8]
HS3 [4]
MR- [4]
BWG [6]
BSTEP [8]
WDCR- [5]
BDIR [8]
PBCS- [11]
BCS- [6]
PRE- [11]
PERR- [11]
WE- [6]
HERR- [4]
+5V
R37
4.7K
U30
U31
U32
U9
AT08
U55
AT32
AT374
U58
U57
10K
SHD0- 14 J4
SHD1- 18 J4
SHD2- 4 J4
SHS3-/RWC- 2 J4
SWG- 6 J4
SSTEP- 24 J4
SDIR- 34 J4
RCS- [5]
WDATA [6]
WD0
WD1
WD2
WD3
WD4
WD5
WD6
WD7
TEXAS INSTRUMENTS
DWN C.HALEY
DATE 02-20-85
ISSUE DATE
SIZE B
FSCM NO 06668
DRAWING NO 2240924
REV C
SCALE: NONE
SHEET 12

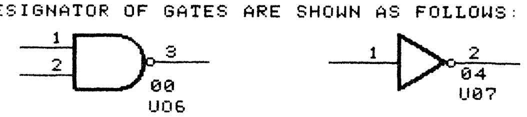

2240924
13
WFM-
AT74
U51
CMDW- [9]
SBFL- [10]
BSVCLR [10]
WDCR- [4]
AT04
U44
WAUP2
WAUP1
CMD [10]
CMD7
CMD6
CMD5
CMD4
CMD1
HDCS- [3]
HSDH- [3]
CSDH [10]
RE- [10]
WE- [10]
PAL16L8
U52
BUSY [3]
SDHRD- [7]
SDHWR- [7]
CSDHW- [7]
LONG- [4]
BDATA <00:07>[3][4]
ERROR [10]
INDEX [5]
CORRD [10]
BDRQ [3]
SC [6]
WF [6]
DRDY [6]
BUSY [3]
STATRD- [9]
DRQ- [10]
AT373
U50
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
+5V
R32
4.7K
U34
4.7K
+5V
AT74
U8
BDRQ
T08
U9
T08
U56
TEXAS INSTRUMENTS
INCORPORATED
Digital Systems Group
DWN
C. HALEY
DATE
02-20-85
ISSUE DATE
SIZE
B
FSCM NO
06668
DRAWING NO.
2240924
REV.
A
SCALE
NONE
SHEET
13

2240927 DRAWING NO | 1 SH

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	ECN538657 (D) WHEELER 5-30-85	6/21/85	[signature]

NOTES, UNLESS OTHERWISE SPECIFIED:

1. ALL DEVICES ARE PREFIXED WITH SN74, A LETTER "T" IN A PREFIX IS EQUAL TO "LS", AND A LETTER "F" AS A SUFFIX IS EQUAL TO CHIP CARRIER
2. VCC IS APPLIED TO PIN 8 OF ALL 8-PIN IC's, PIN 14 OF ALL 14-PIN IC's, PIN 16 OF ALL 16-PIN IC's, PIN 20 OF ALL 20-PIN IC's, ETC
3. GROUND IS APPLIED TO PIN 4 OF ALL 8-PIN IC's, PIN 7 OF ALL 14-PIN IC's, PIN 8 OF ALL 16-PIN IC's, PIN 10 OF ALL 20-PIN IC's, ETC
4. DEVICE TYPE, PIN NUMBERS, AND REFERENCE DESIGNATOR OF GATES ARE SHOWN AS FOLLOWS:



00 AND 04 = DEVICE TYPES
1, 2, AND 3 = PIN NUMBERS
U06 AND U07 = REFERENCE DESIGNATORS

5. RESISTANCE VALUES ARE IN OHMS
6. RESISTORS ARE 1/4 WATT, 5%
7. CAPACITANCE VALUES ARE IN MICROFARADS
8. DISTRIBUTE THE .001 UF CAPACITORS AMONG THE IC'S
9. NUMBERS IN BRACKETS ARE REF TO SHEETS, ie [2] SHEET 2
10. CAPACITORS ARE 50 VOLT

29

COMPUTER GENERATED DRAWING : DO NOT REVISE MANUALLY

-1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES

PARTS LIST

UNLESS OTHERWISE SPECIFIED
* DIMENSIONS ARE IN INCHES
* TOLERANCES: ANGLES +/-1 DEG
  3 PLACE DECIMALS +/-.010
  2 PLACE DECIMALS +/-.02
* INTERPRET DRAWING PER MIL-D-1000
* REMOVE BURRS AND SHARP EDGES
* CONCENTRICITY MACHINED DIAMETERS .010 FIM
* DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
* PARENTHETICAL INFO FOR REF ONLY

HOLE TOLERANCE

.013 THRU .125 +.004 -.001	.126 THRU .250 +.005 -.001	.251 THRU .500 +.006 -.001
.501 THRU .750 +.008 -.001	.751 THRU 1.000 +.010 -.001	1.001 THRU 2.000 +.012 -.001

NEXT ASSY	USED ON
2240928	8721

APPLICATION

	NAME	DATE
DWN	R.JAVENS	10-25-84
CHK	F.PETERSON	3-22-85
ENGR	S.WALLACE	3-22-85
APVD ENGR	R.JAVENS	3-22-85
QA	W.DILLER	3-22-85
APVD MFG	S.RILEY	3-22-85
RELEASE	F.PETERSON	3-22-85

TEXAS INSTRUMENTS
Data Systems Group

DIAGRAM, LOGIC, DETAILED-3M EXPANSION BOARD, EXCALIBUR

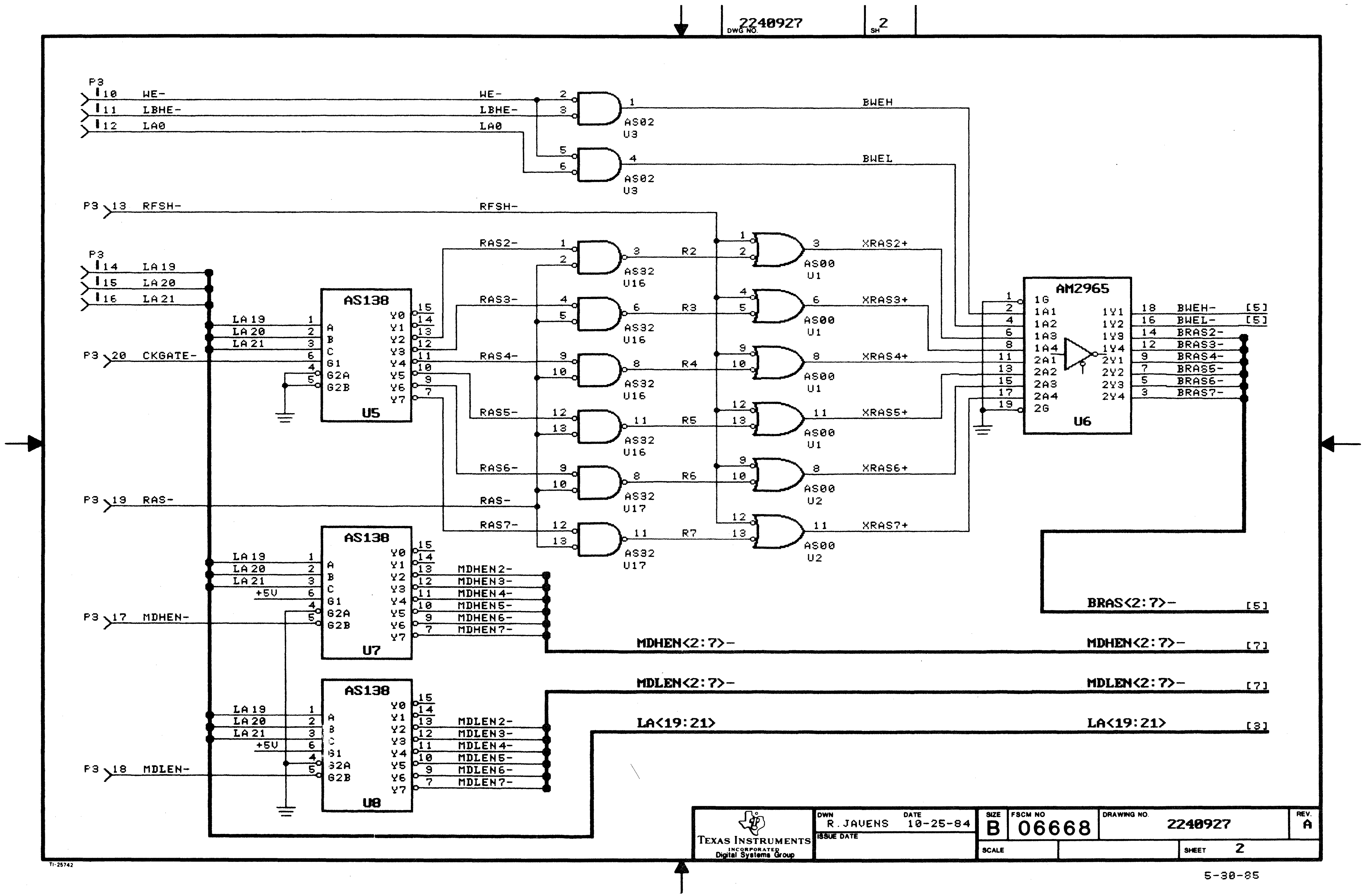
SIZE B | FSCM NO 06668 | DRAWING NO 2240927
SCALE NONE | SHEET 1 OF 7

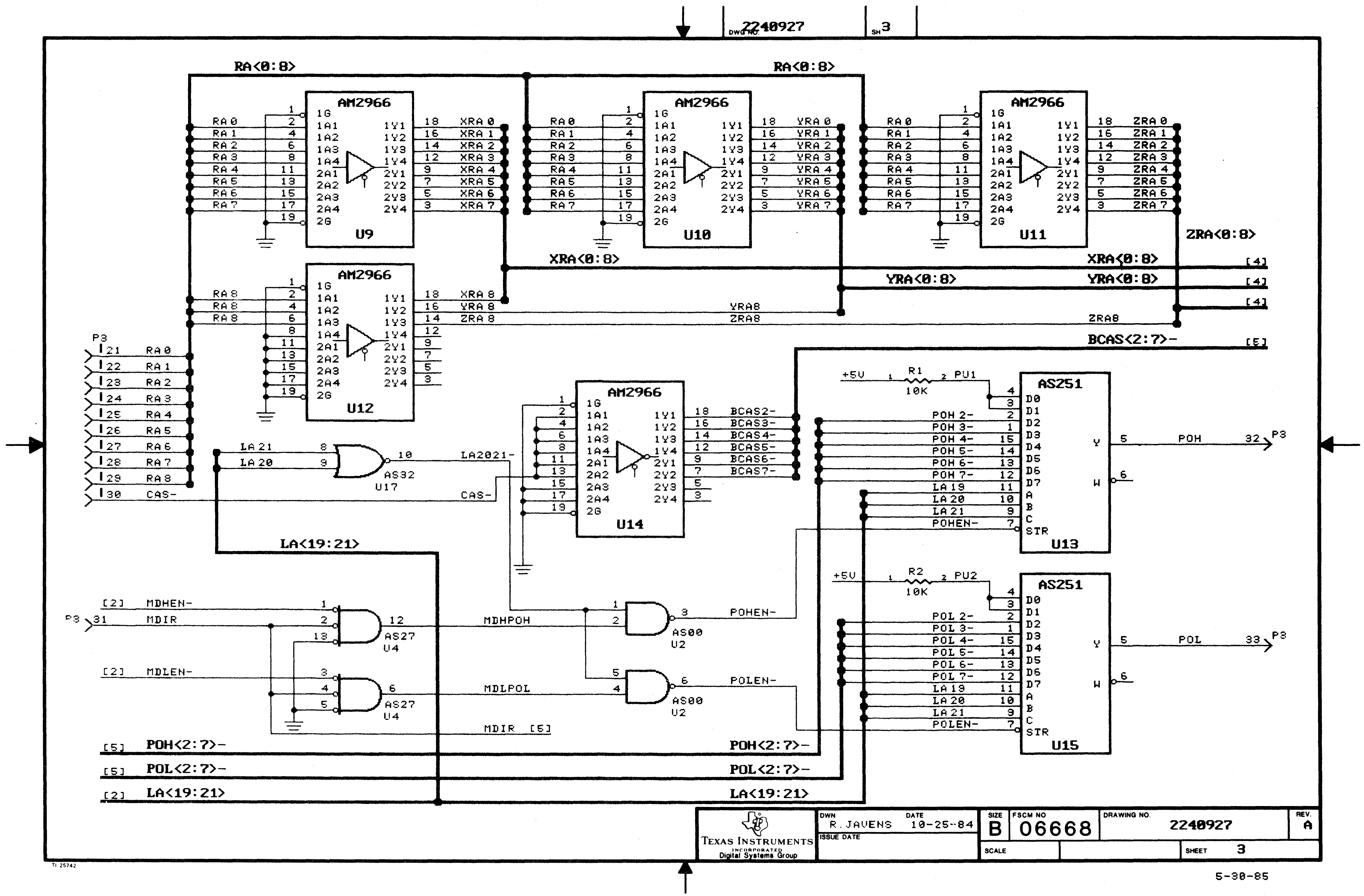
REV	A	A	A				
SH	1	2	3	4	5	6	7

REVISION STATUS OF SHEETS

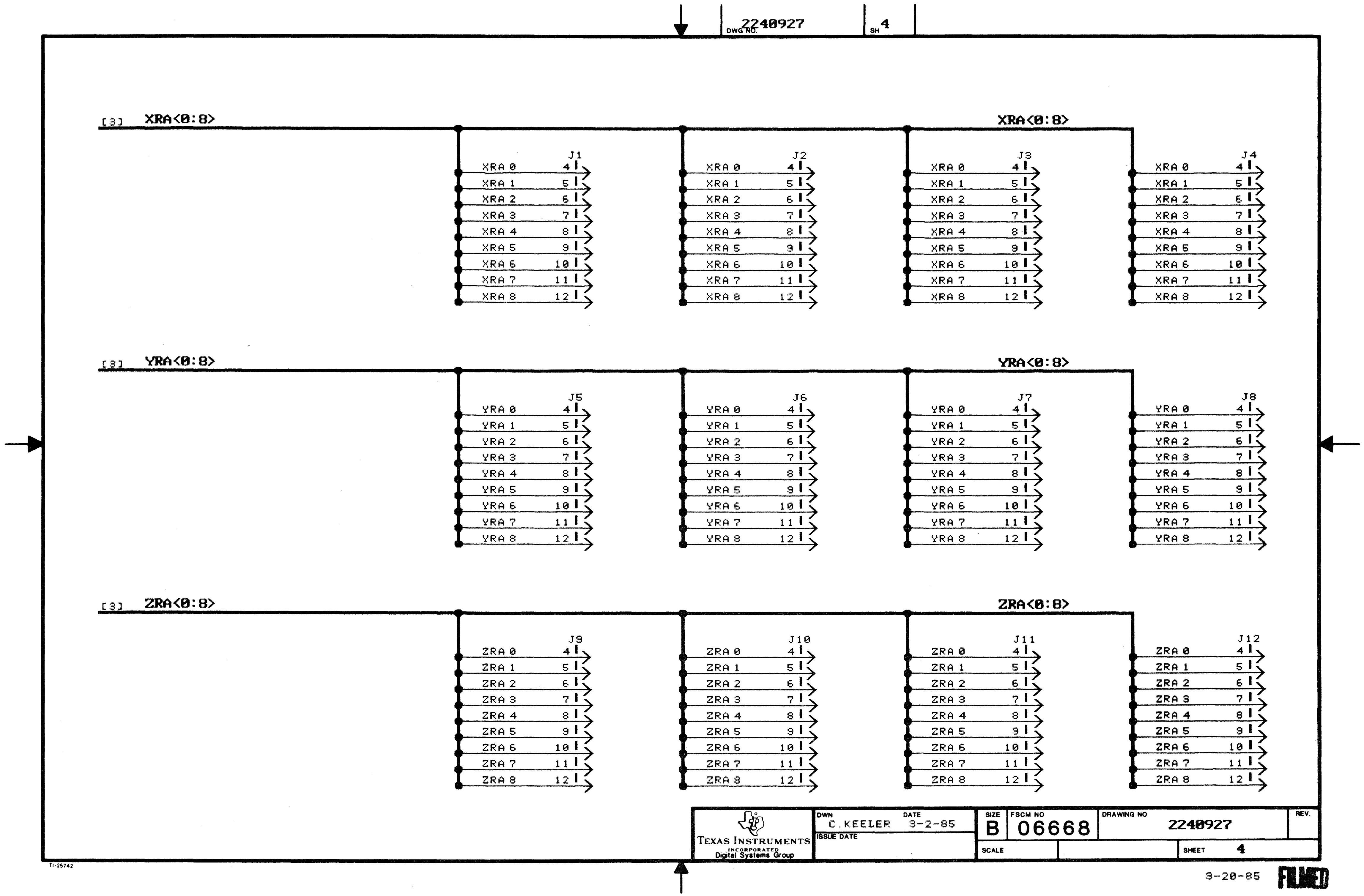
430

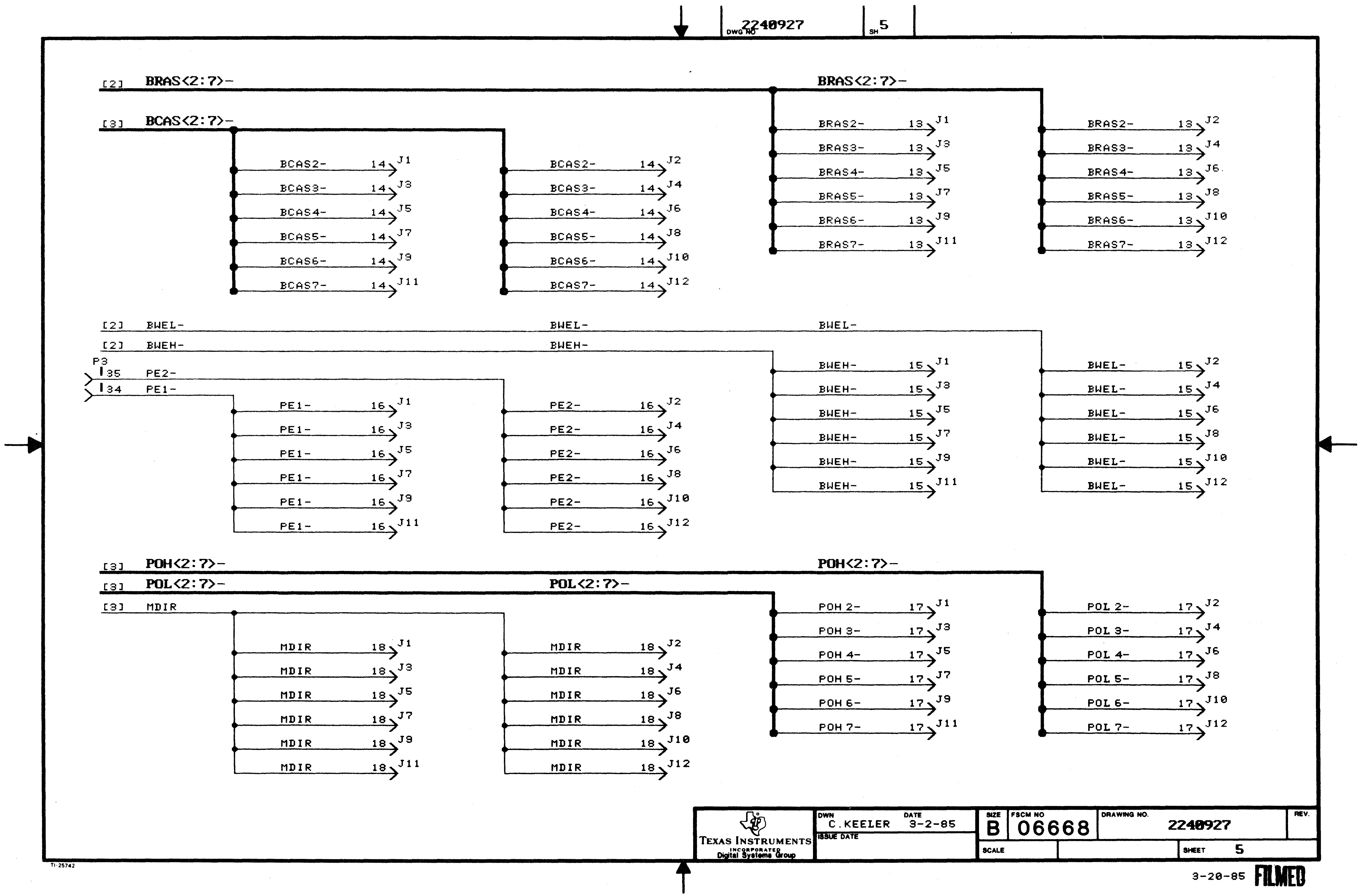
FILMED DB 5-30-85

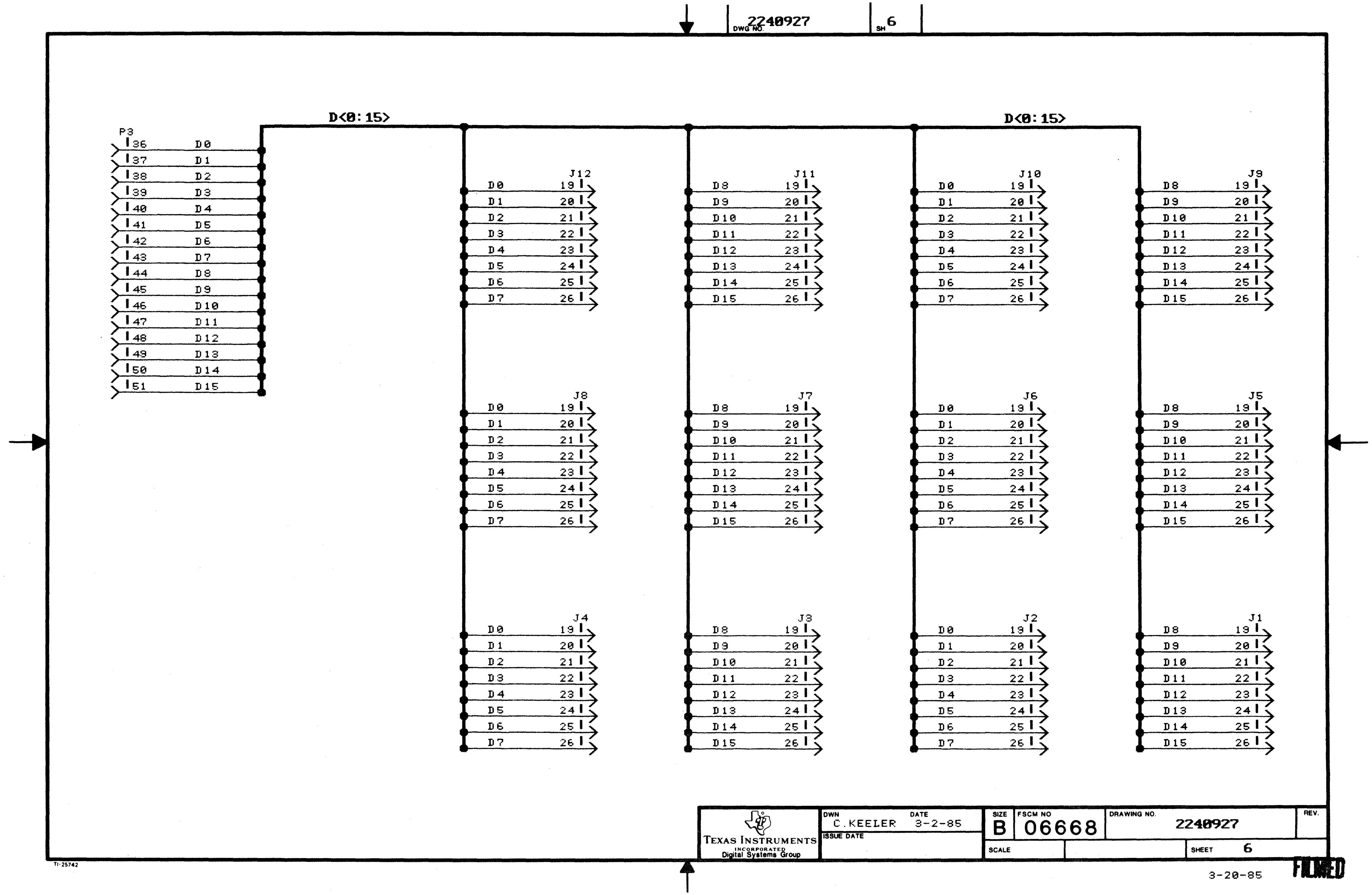

2240927
2
WE-
LBHE-
LA0
BWEH
BWEL
AS02
U3
RFSH-
RAS2-
RAS3-
RAS4-
RAS5-
RAS6-
RAS7-
RAS-
CKGATE-
MDHEN-
MDLEN-
LA19
LA20
LA21
AS138
U5
U7
U8
AS32
U16
U17
AS00
U1
U2
XRAS2+
XRAS3+
XRAS4+
XRAS5+
XRAS6+
XRAS7+
AM2965
U6
BWEH- [5]
BWEL- [5]
BRAS2-
BRAS3-
BRAS4-
BRAS5-
BRAS6-
BRAS7-
BRAS<2:7>- [5]
MDHEN<2:7>- [7]
MDLEN<2:7>- [7]
LA<19:21> [3]
MDHEN2-
MDHEN3-
MDHEN4-
MDHEN5-
MDHEN6-
MDHEN7-
MDLEN2-
MDLEN3-
MDLEN4-
MDLEN5-
MDLEN6-
MDLEN7-
+5V
TEXAS INSTRUMENTS
Digital Systems Group
R. JAVENS
10-25-84
B
06668
2240927
A
SHEET 2
5-30-85

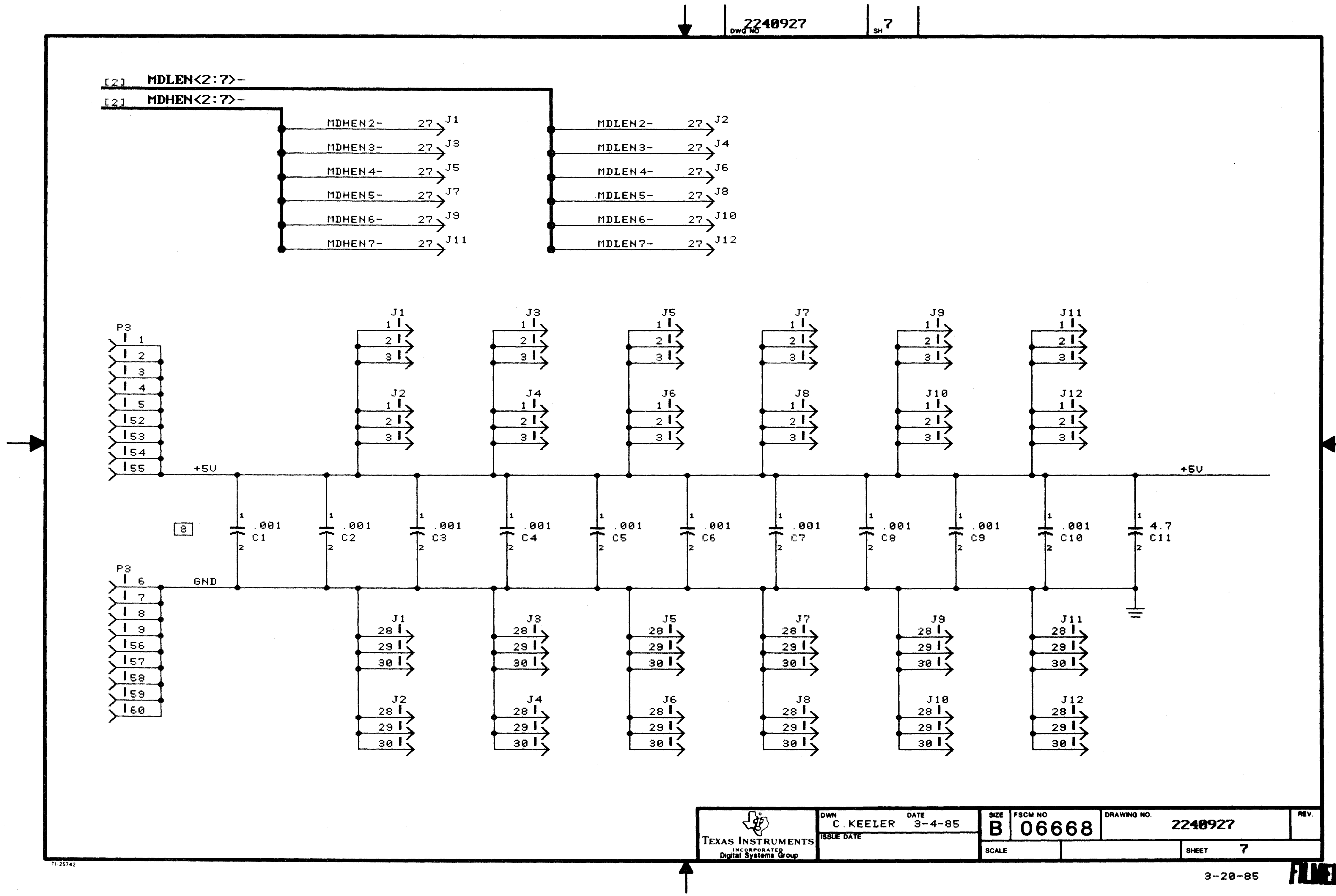


2240927
SH 3
RA<0:8>
AM2966
U9
U10
U11
U12
U14
XRA<0:8>
YRA<0:8>
ZRA<0:8>
BCAS<2:7>-
LA<19:21>
AS251
U13
U15
AS32
U17
AS27
U4
AS00
U2
MDHEN-
MDIR
MDLEN-
MDHPOH
MDLPOL
POHEN-
POLEN-
POH
POL
POH<2:7>-
POL<2:7>-
R1
R2
10K
+5V
PU1
PU2
CAS-
LA2021-
P3
TEXAS INSTRUMENTS
Digital Systems Group
DWN R. JAVENS
DATE 10-25-84
SIZE B
FSCM NO 06668
DRAWING NO. 2240927
REV. A
SHEET 3
5-30-85


2240927
4
[3] XRA<0:8>
XRA<0:8>
J1
J2
J3
J4
XRA 0
XRA 1
XRA 2
XRA 3
XRA 4
XRA 5
XRA 6
XRA 7
XRA 8
[3] YRA<0:8>
YRA<0:8>
J5
J6
J7
J8
YRA 0
YRA 1
YRA 2
YRA 3
YRA 4
YRA 5
YRA 6
YRA 7
YRA 8
[3] ZRA<0:8>
ZRA<0:8>
J9
J10
J11
J12
ZRA 0
ZRA 1
ZRA 2
ZRA 3
ZRA 4
ZRA 5
ZRA 6
ZRA 7
ZRA 8
TEXAS INSTRUMENTS
INCORPORATED
Digital Systems Group
DWN C. KEELER
DATE 3-2-85
ISSUE DATE
SIZE B
FSCM NO 06668
DRAWING NO. 2240927
REV.
SCALE
SHEET 4
3-20-85
FILMED


2240927
SH 5
BRAS<2:7>-
BCAS<2:7>-
BWEL-
BWEH-
PE2-
PE1-
POH<2:7>-
POL<2:7>-
MDIR
TEXAS INSTRUMENTS
Digital Systems Group
C.KEELER 3-2-85
B 06668
2240927
SHEET 5
3-20-85 FILMED


2240927
DWG NO.
SH 6
D<0:15>
D<0:15>
P3
J12
J11
J10
J9
J8
J7
J6
J5
J4
J3
J2
J1
TEXAS INSTRUMENTS
INCORPORATED
Digital Systems Group
DWN C.KEELER
DATE 3-2-85
ISSUE DATE
SIZE B
FSCM NO 06668
DRAWING NO. 2240927
REV.
SCALE
SHEET 6
3-20-85
FILMED



2240927
7
[2] MDLEN<2:7>-
[2] MDHEN<2:7>-
MDHEN2- 27 J1
MDHEN3- 27 J3
MDHEN4- 27 J5
MDHEN5- 27 J7
MDHEN6- 27 J9
MDHEN7- 27 J11
MDLEN2- 27 J2
MDLEN3- 27 J4
MDLEN4- 27 J6
MDLEN5- 27 J8
MDLEN6- 27 J10
MDLEN7- 27 J12
P3
+5V
GND
.001 C1
.001 C2
.001 C3
.001 C4
.001 C5
.001 C6
.001 C7
.001 C8
.001 C9
.001 C10
4.7 C11
8
TEXAS INSTRUMENTS INCORPORATED Digital Systems Group
DWN C. KEELER DATE 3-4-85
ISSUE DATE
SIZE B FSCM NO 06668
DRAWING NO. 2240927
REV.
SCALE
SHEET 7
3-20-85
FILMED

2240930 DRAWING NO 1 SH

R E V I S I O N S			
REV	DESCRIPTION	DATE	APPROVED
A	ECN538654 (D) WHEELER 5-30-85	6/15/85	

NOTES, UNLESS OTHERWISE SPECIFIED:

1. ALL DEVICES ARE PREFIXED WITH SN74, A LETTER "T" IN A PREFIX IS EQUAL TO "LS", AND A LETTER "F" AS A SUFFIX IS EQUAL TO CHIP CARRIER
2. VCC IS APPLIED TO PIN 8 OF ALL TMS4256 IC's AND TO PIN 20 OF ALL AS645 IC's
3. GROUND IS APPLIED TO PIN 16 OF ALL TMS4256 IC's AND TO PIN 10 OF ALL AS645 IC's
4. DEVICE TYPE, PIN NUMBERS, AND REFERENCE DESIGNATOR OF GATES ARE SHOWN AS FOLLOWS:

00 AND 04 = DEVICE TYPES
1, 2, AND 3 = PIN NUMBERS
U06 AND U07 = REFERENCE DESIGNATORS

5. RESISTANCE VALUES ARE IN OHMS
6. RESISTORS ARE 1/4 WATT, 5%
7. CAPACITANCE VALUES ARE IN MICROFARADS
8. DISTRIBUTE THE .001 UF CAPACITORS AMONG THE IC'S
9. NUMBERS IN BRACKETS ARE REF TO SHEETS, ie [2] SHEET 2

29

COMPUTER GENERATED DRAWING ; DO NOT REVISE MANUALLY

QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES

PARTS LIST

NEXT ASSY	USED ON
2240931	8721

APPLICATION

REV	A		A
SH	1	2	3

REVISION STATUS OF SHEETS

UNLESS OTHERWISE SPECIFIED
* DIMENSIONS ARE IN INCHES
* TOLERANCES: ANGLES +/-1 DEG
  3 PLACE DECIMALS +/-.010
  2 PLACE DECIMALS +/-.02
* INTERPRET DRAWING PER MIL-D-1000
* REMOVE BURRS AND SHARP EDGES
* CONCENTRICITY MACHINED DIAMETERS .010 FIM
* DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
* PARENTHETICAL INFO FOR REF ONLY

HOLE TOLERANCE

.013 THRU .125 +.004 -.001	.126 THRU .250 +.005 -.001	.251 THRU .500 +.006 -.001
.501 THRU .750 +.008 -.001	.751 THRU 1.000 +.010 -.001	1.001 THRU 2.000 +.012 -.001

		DATE
DWN	R.JAVENS	10-12-84
CHK	F.PETERSON	3-22-85
ENGR	R.JAVENS	3-22-85
APVD ENGR	S.WALLACE	3-22-85
QA	W.DILLER	3-22-85
APVD MFG	S.RILEY	3-22-85
RELEASE	F.PETERSON	3-22-85

TEXAS INSTRUMENTS
Data Systems Group

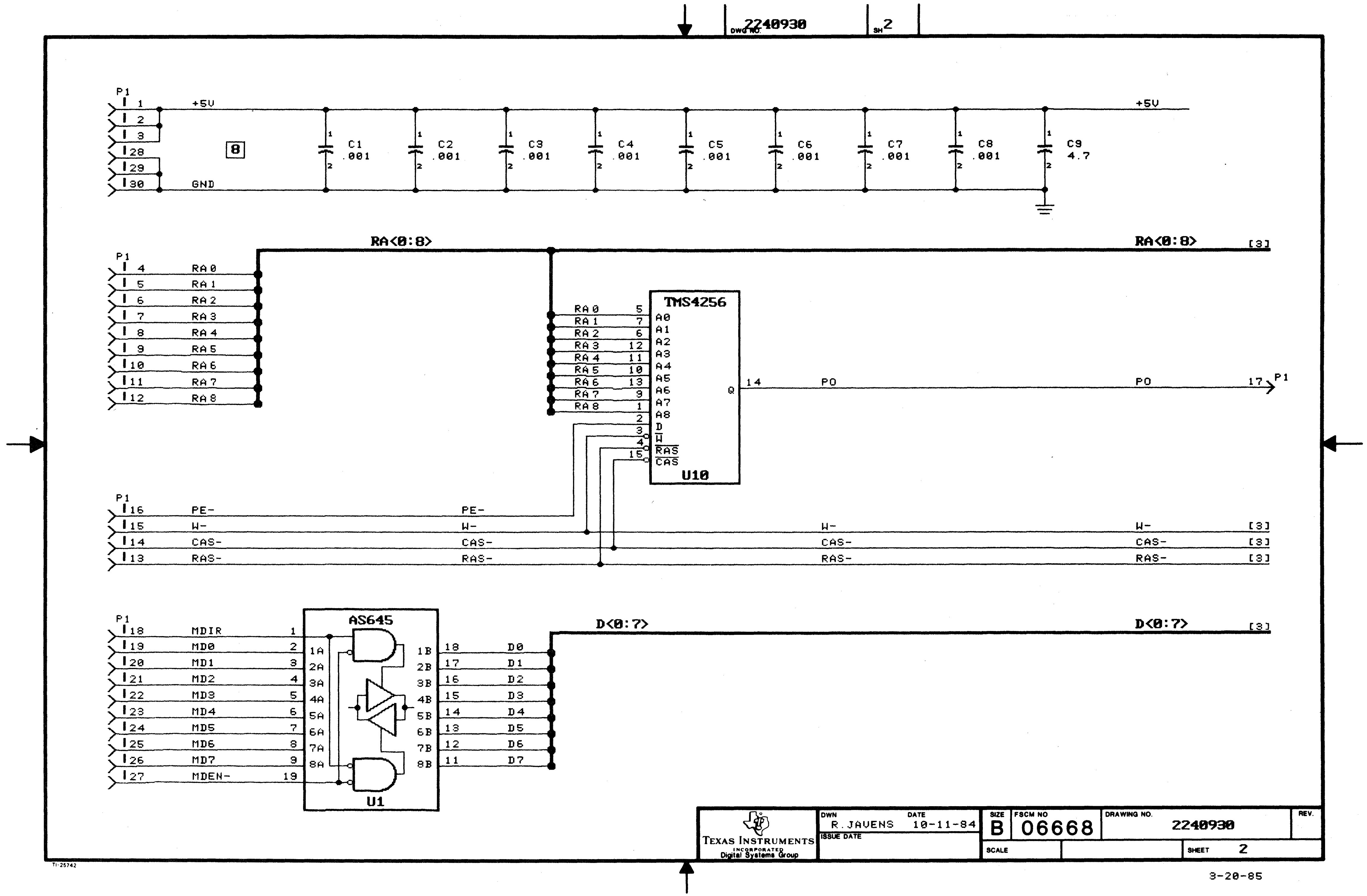
DIAGRAM, LOGIC, DETAILED-256KX9 DRAM EXPANSION CARD, EXCALIBUR

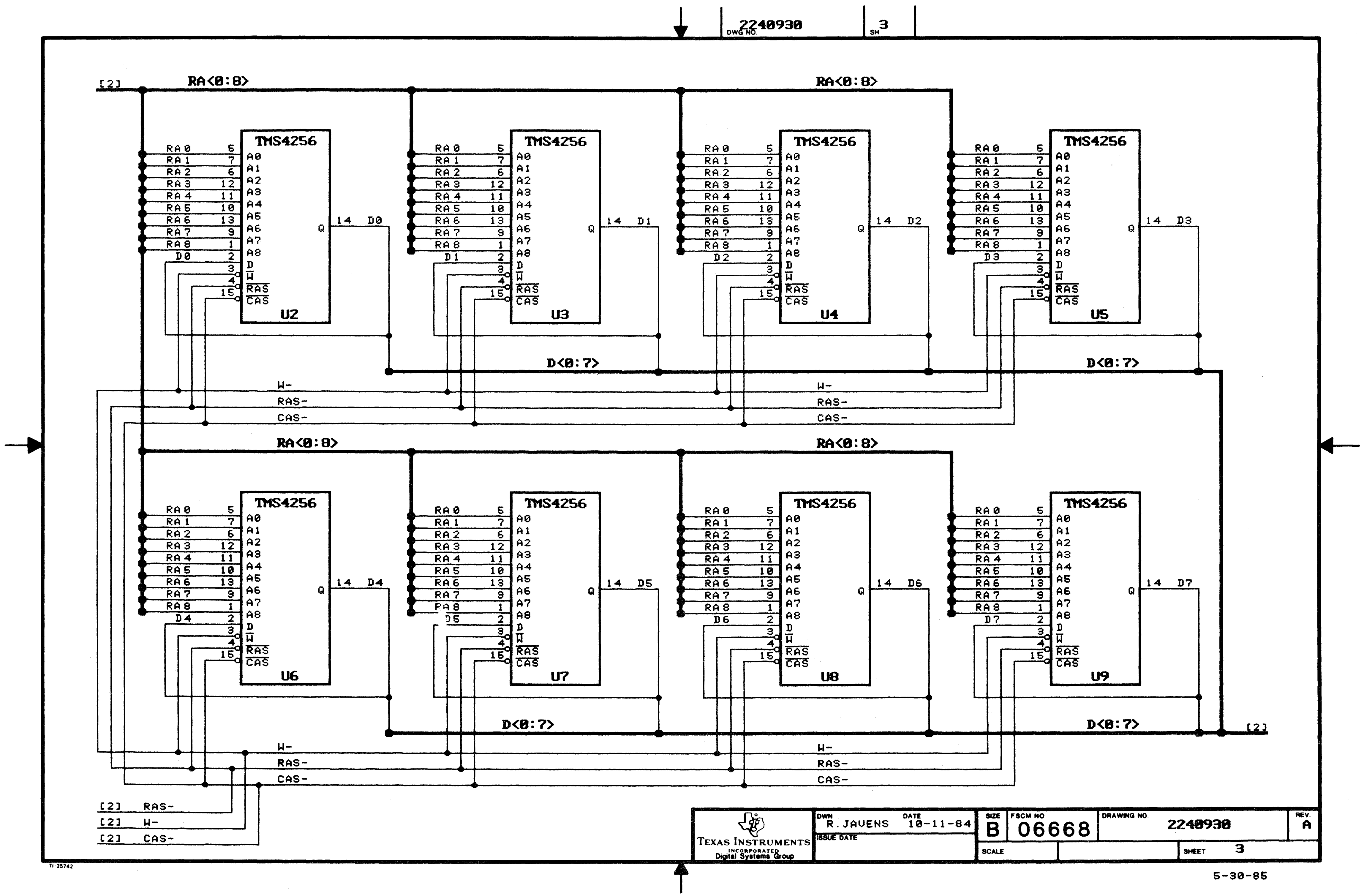
SIZE	FSCM NO	DRAWING NO
B	06668	2240930

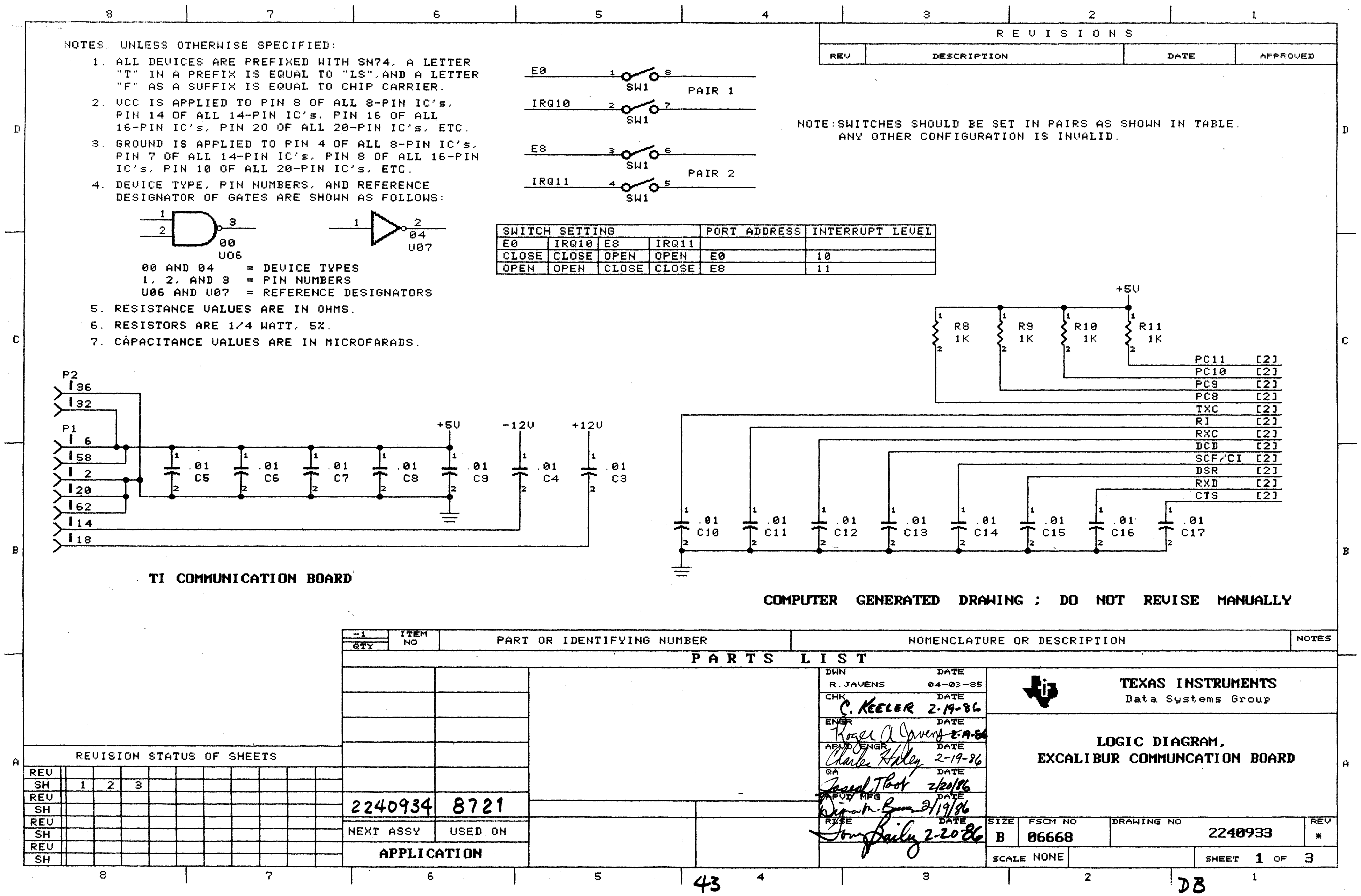
SCALE NONE   SHEET 1 OF 3

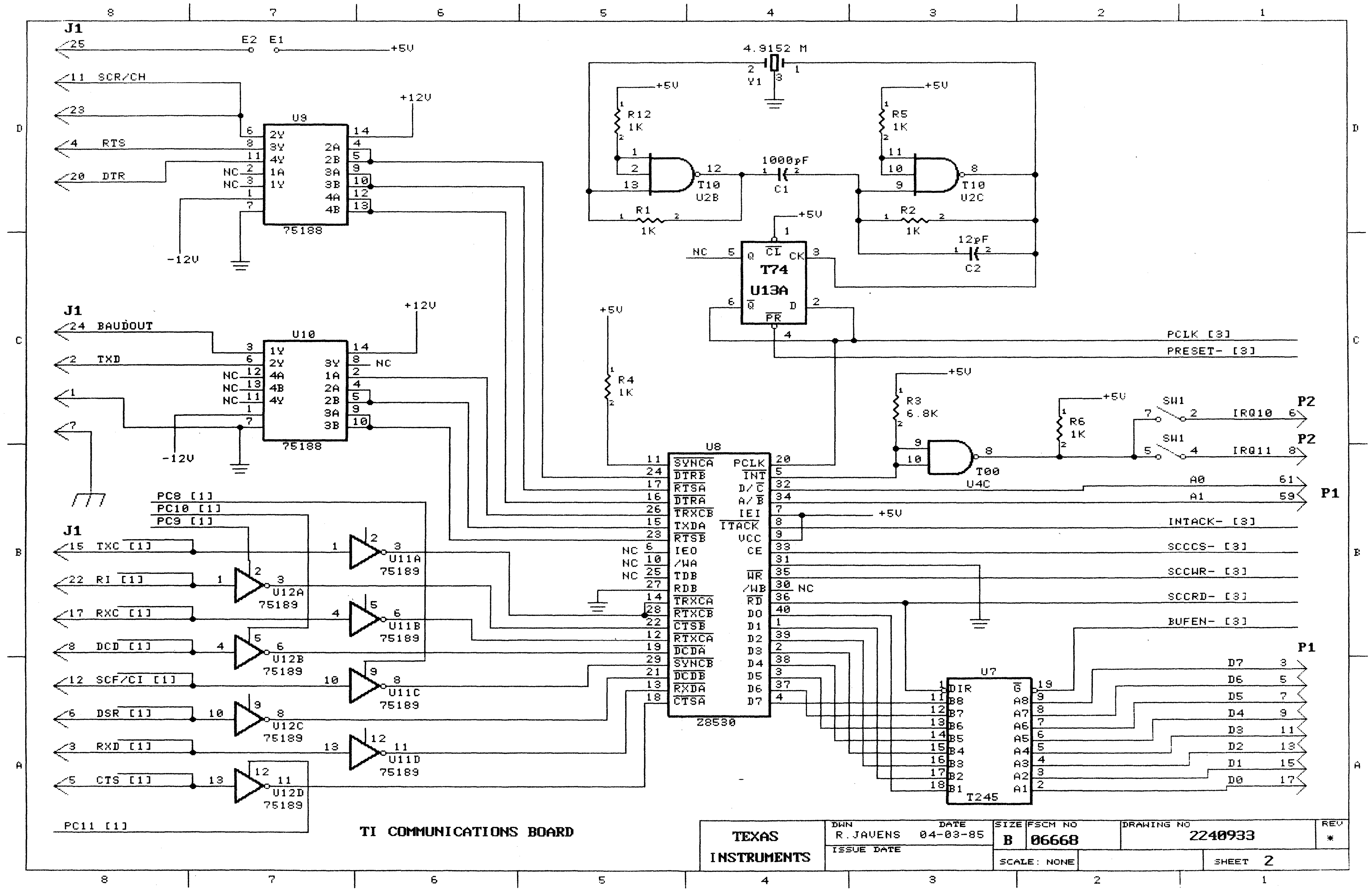
430

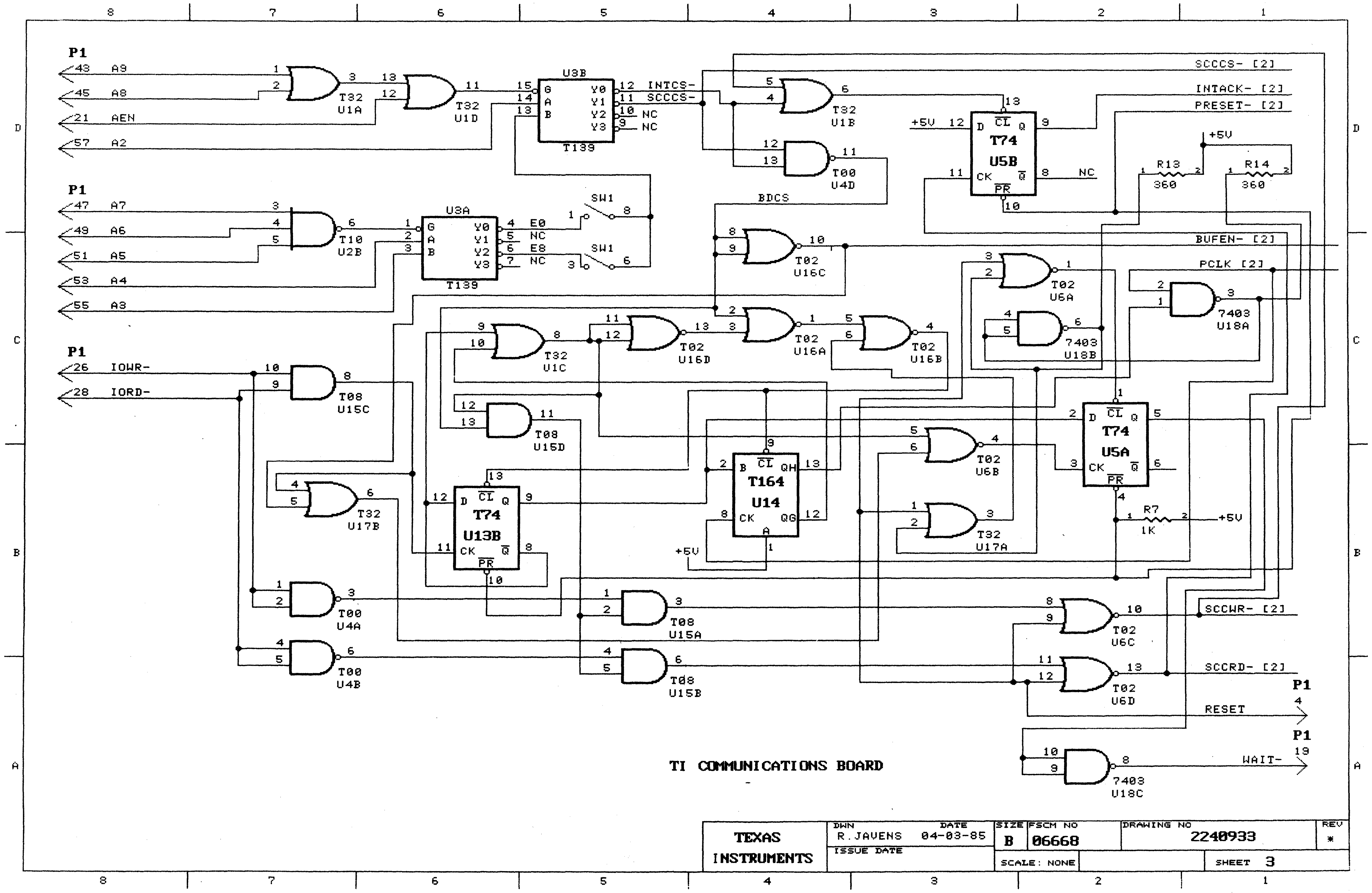
DB FILMED 5-30-85


2240930
SH 2
P1
+5V
GND
8
C1 .001
C2 .001
C3 .001
C4 .001
C5 .001
C6 .001
C7 .001
C8 .001
C9 4.7
RA<0:8>
[3]
RA0
RA1
RA2
RA3
RA4
RA5
RA6
RA7
RA8
TMS4256
U10
PO
PE-
W-
CAS-
RAS-
AS645
U1
MDIR
MD0
MD1
MD2
MD3
MD4
MD5
MD6
MD7
MDEN-
D<0:7>
D0
D1
D2
D3
D4
D5
D6
D7
TEXAS INSTRUMENTS
Digital Systems Group
R. JAVENS
10-11-84
B
06668
2240930
SHEET 2
3-20-85


2240930
3
RA<0:8>
D<0:7>
TMS4256
U2
U3
U4
U5
U6
U7
U8
U9
W-
RAS-
CAS-
[2] RAS-
[2] W-
[2] CAS-
TEXAS INSTRUMENTS
INCORPORATED
Digital Systems Group
R. JAVENS
10-11-84
B
06668
2240930
A
3
5-30-85


NOTES, UNLESS OTHERWISE SPECIFIED:
1. ALL DEVICES ARE PREFIXED WITH SN74, A LETTER "T" IN A PREFIX IS EQUAL TO "LS", AND A LETTER "F" AS A SUFFIX IS EQUAL TO CHIP CARRIER.
2. VCC IS APPLIED TO PIN 8 OF ALL 8-PIN IC's, PIN 14 OF ALL 14-PIN IC's, PIN 16 OF ALL 16-PIN IC's, PIN 20 OF ALL 20-PIN IC's, ETC.
3. GROUND IS APPLIED TO PIN 4 OF ALL 8-PIN IC's, PIN 7 OF ALL 14-PIN IC's, PIN 8 OF ALL 16-PIN IC's, PIN 10 OF ALL 20-PIN IC's, ETC.
4. DEVICE TYPE, PIN NUMBERS, AND REFERENCE DESIGNATOR OF GATES ARE SHOWN AS FOLLOWS:
00 AND 04 = DEVICE TYPES
1, 2, AND 3 = PIN NUMBERS
U06 AND U07 = REFERENCE DESIGNATORS
5. RESISTANCE VALUES ARE IN OHMS.
6. RESISTORS ARE 1/4 WATT, 5%.
7. CAPACITANCE VALUES ARE IN MICROFARADS.
E0 SW1 IRQ10 SW1 PAIR 1
E8 SW1 IRQ11 SW1 PAIR 2
NOTE: SWITCHES SHOULD BE SET IN PAIRS AS SHOWN IN TABLE. ANY OTHER CONFIGURATION IS INVALID.
SWITCH SETTING | PORT ADDRESS | INTERRUPT LEVEL
E0 | IRQ10 | E8 | IRQ11
CLOSE | CLOSE | OPEN | OPEN | E0 | 10
OPEN | OPEN | CLOSE | CLOSE | E8 | 11
REVISIONS
REV DESCRIPTION DATE APPROVED
+5V R8 1K R9 1K R10 1K R11 1K
PC11 [2] PC10 [2] PC9 [2] PC8 [2] TXC [2] RI [2] RXC [2] DCD [2] SCF/CI [2] DSR [2] RXD [2] CTS [2]
P2 36 32 P1 6 58 2 20 62 14 18
+5V -12V +12V
.01 C5 .01 C6 .01 C7 .01 C8 .01 C9 .01 C4 .01 C3
.01 C10 .01 C11 .01 C12 .01 C13 .01 C14 .01 C15 .01 C16 .01 C17
TI COMMUNICATION BOARD
COMPUTER GENERATED DRAWING ; DO NOT REVISE MANUALLY
QTY ITEM NO PART OR IDENTIFYING NUMBER NOMENCLATURE OR DESCRIPTION NOTES
PARTS LIST
REVISION STATUS OF SHEETS
REV SH 1 2 3
2240934 8721
NEXT ASSY USED ON
APPLICATION
DWN R. JAVENS DATE 04-03-85
CHK C. KEELER 2-19-86
TEXAS INSTRUMENTS
Data Systems Group
LOGIC DIAGRAM,
EXCALIBUR COMMUNCATION BOARD
SIZE B FSCM NO 06668 DRAWING NO 2240933 REV *
SCALE NONE SHEET 1 OF 3
43 DB


J1
E2 E1
+5V
SCR/CH
RTS
DTR
U9
75188
+12V
-12V
BAUDOUT
TXD
U10
75188
NC
4.9152 M
Y1
R12 1K
R5 1K
1000pF
C1
T10 U2B
T10 U2C
R1 1K
R2 1K
12pF
C2
T74
U13A
R4 1K
R3 6.8K
R6 1K
SW1
IRQ10
IRQ11
P2
T00 U4C
U8
Z8530
PCLK [3]
PRESET- [3]
A0
A1
P1
INTACK- [3]
SCCCS- [3]
SCCWR- [3]
SCCRD- [3]
BUFEN- [3]
PC8 [1]
PC10 [1]
PC9 [1]
TXC [1]
RI [1]
RXC [1]
DCD [1]
SCF/CI [1]
DSR [1]
RXD [1]
CTS [1]
PC11 [1]
U11A 75189
U12A 75189
U11B 75189
U12B 75189
U11C 75189
U12C 75189
U11D 75189
U12D 75189
U7
T245
D7
D6
D5
D4
D3
D2
D1
D0
TI COMMUNICATIONS BOARD
TEXAS INSTRUMENTS
DWN R. JAVENS
DATE 04-03-85
ISSUE DATE
SIZE B
FSCM NO 06668
DRAWING NO 2240933
REV *
SCALE: NONE
SHEET 2


P1
A9
A8
AEN
A2
A7
A6
A5
A4
A3
IOWR-
IORD-
T32 U1A
T32 U1D
U3B
T139
INTCS-
SCCCS-
NC
U3A
E0
E8
SW1
T10 U2B
T32 U1B
T00 U4D
BDCS
T74 U5B
+5V
R13 360
R14 360
SCCCS- [2]
INTACK- [2]
PRESET- [2]
BUFEN- [2]
PCLK [2]
T02 U16C
T02 U6A
7403 U18A
7403 U18B
T32 U1C
T02 U16D
T02 U16A
T02 U16B
T08 U15C
T08 U15D
T32 U17B
T74 U13B
T164 U14
T02 U6B
T32 U17A
T74 U5A
R7 1K
T00 U4A
T00 U4B
T08 U15A
T08 U15B
T02 U6C
T02 U6D
SCCWR- [2]
SCCRD- [2]
RESET
WAIT-
7403 U18C
TI COMMUNICATIONS BOARD
TEXAS INSTRUMENTS
DWN R.JAVENS
DATE 04-03-85
ISSUE DATE
SIZE B
FSCM NO 06668
DRAWING NO 2240933
REV *
SCALE: NONE
SHEET 3

NOTES, UNLESS OTHERWISE SPECIFIED:

1. ALL DEVICES ARE PREFIXED WITH SN74, A LETTER "T" IN A PREFIX IS EQUAL TO "LS", AND A LETTER "F" AS A SUFFIX IS EQUAL TO CHIP CARRIER.
2. VCC IS APPLIED TO PIN 8 OF ALL 8-PIN IC's, PIN 14 OF ALL 14-PIN IC's, PIN 16 OF ALL 16-PIN IC's, PIN 20 OF ALL 20-PIN IC's, ETC.
3. GROUND IS APPLIED TO PIN 4 OF ALL 8-PIN IC's, PIN 7 OF ALL 14-PIN IC's, PIN 8 OF ALL 16-PIN IC's, PIN 10 OF ALL 20-PIN IC's, ETC.
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00 AND 04 = DEVICE TYPES
1, 2, AND 3 = PIN NUMBERS
U06 AND U07 = REFERENCE DESIGNATORS

5. RESISTANCE VALUES ARE IN OHMS.
6. RESISTORS ARE 1/4 WATT, 5%.
7. CAPACITANCE VALUES ARE IN MICROFARADS.
8. U28 HAS PIN 14 TIED TO +5VU28 .
9. U39 HAS PIN 20 TIED TO +5VU39 .

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

COMPUTER GENERATED DRAWING ; DO NOT REVISE MANUALLY

-1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES

PARTS LIST

REVISION STATUS OF SHEETS

REV									
SH	1	2	3	4	5	6	7	8	9

NEXT ASSY	USED ON
2240934	8721

APPLICATION

DWN A. MCBRIDE DATE 01-20-85
CHK DATE
ENGR DATE
APVD ENGR DATE
QA DATE
APVD MFG DATE
RLSE DATE

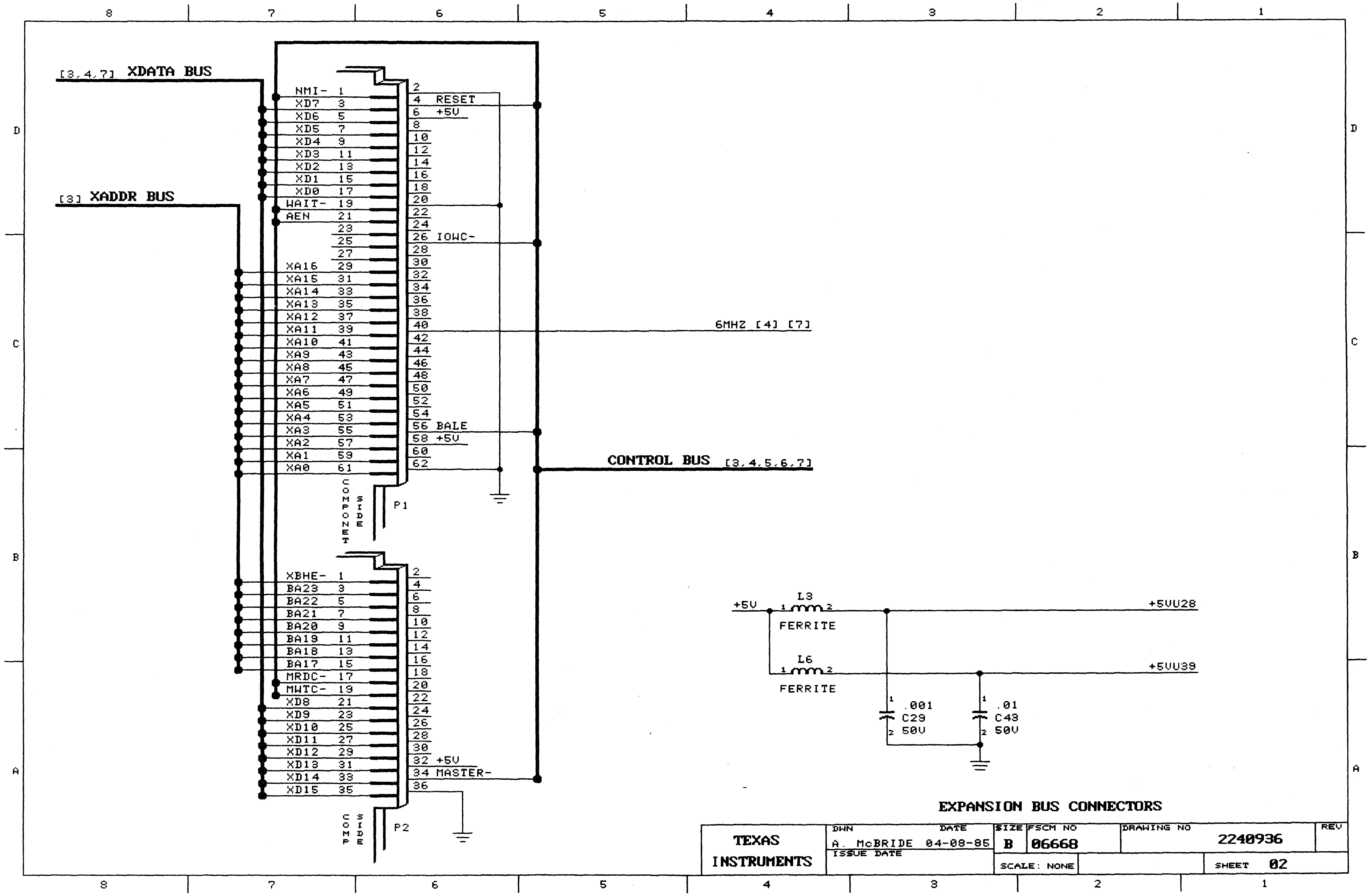
TEXAS INSTRUMENTS
Data Systems Group

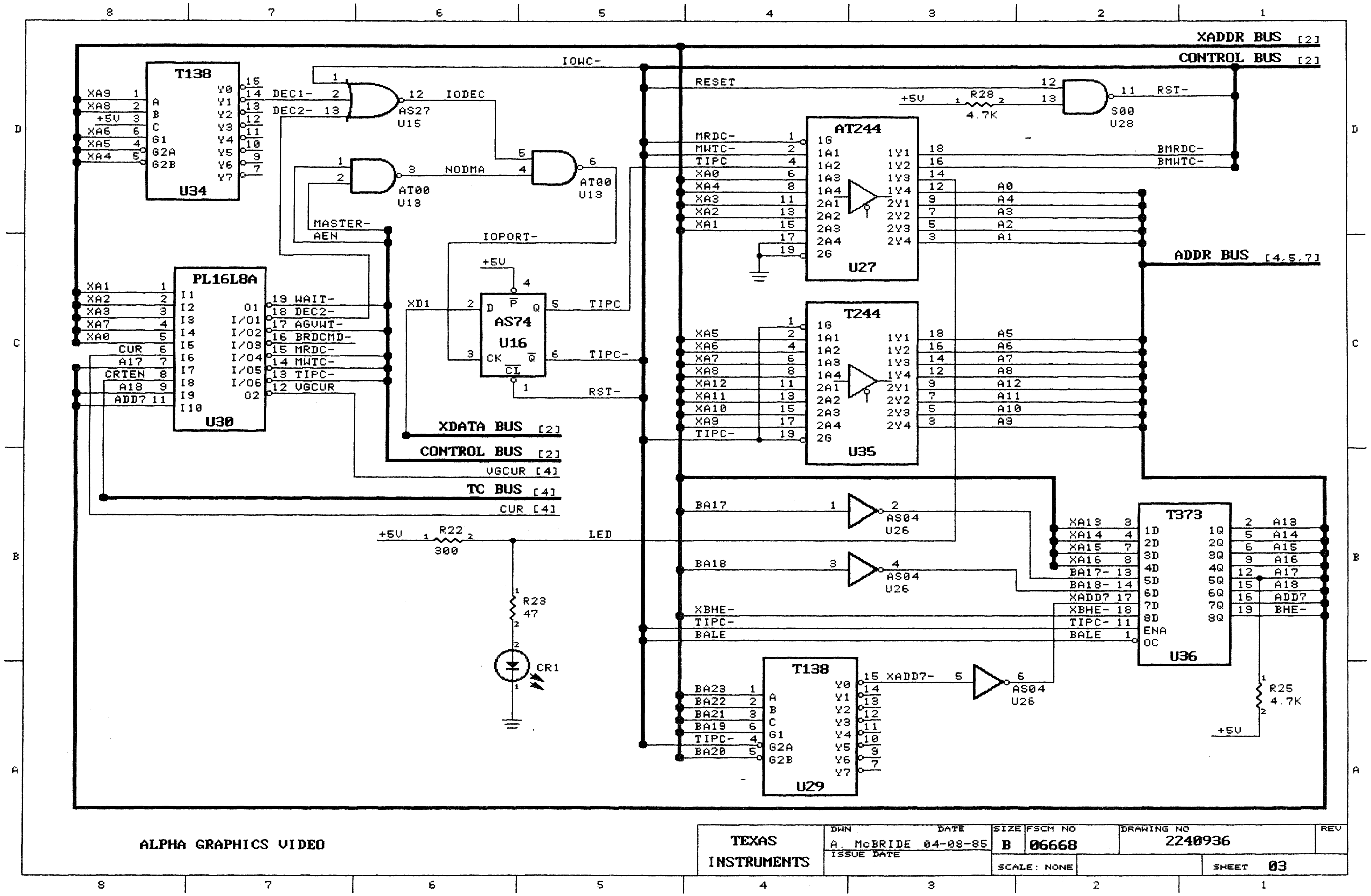
LOGIC DIAGRAM,
ALPHA GRAPHICS VIDEO

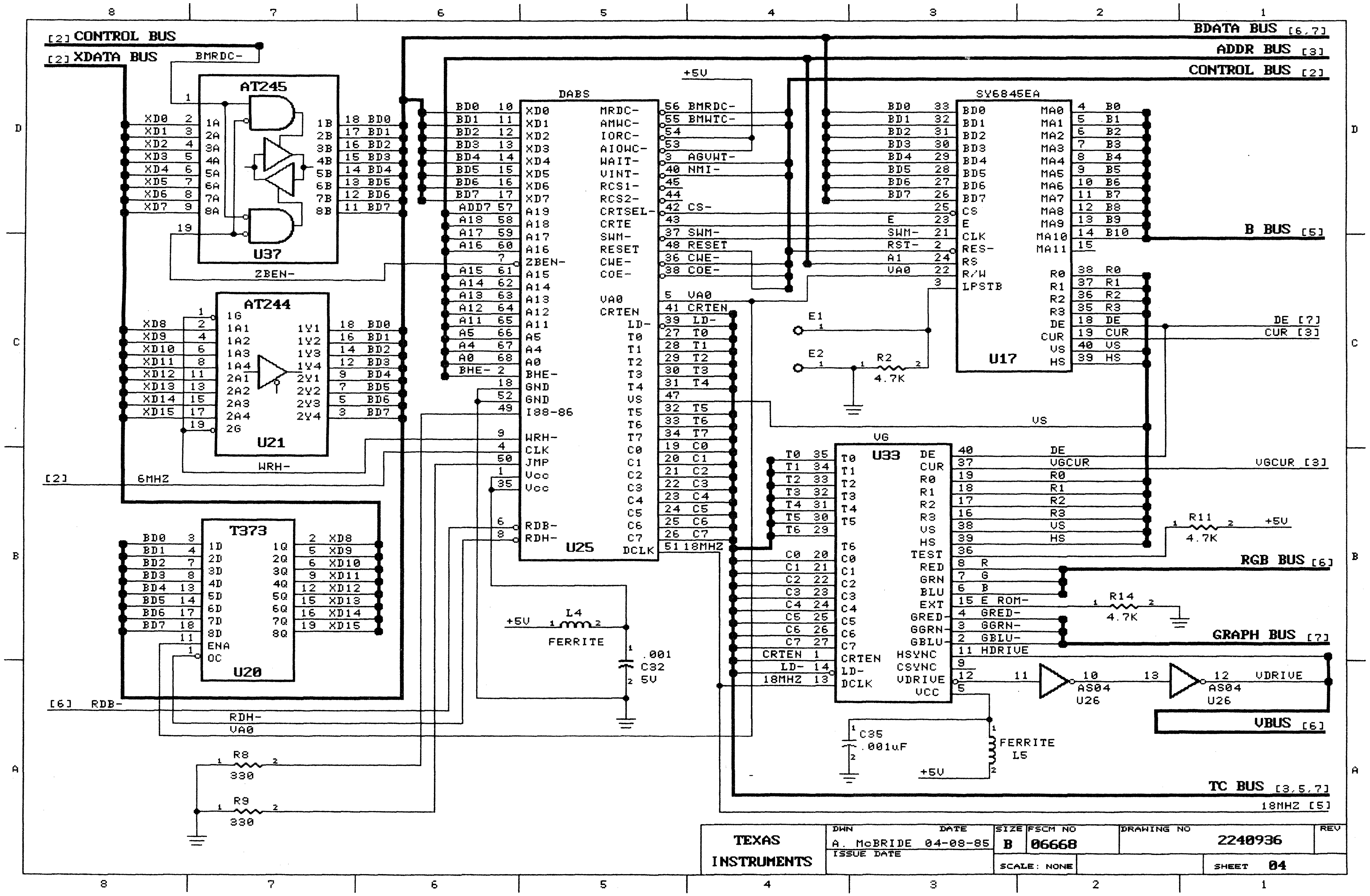
SIZE	FSCM NO	DRAWING NO	REV
B	06668	2240936	

SCALE NONE SHEET 1 OF 9

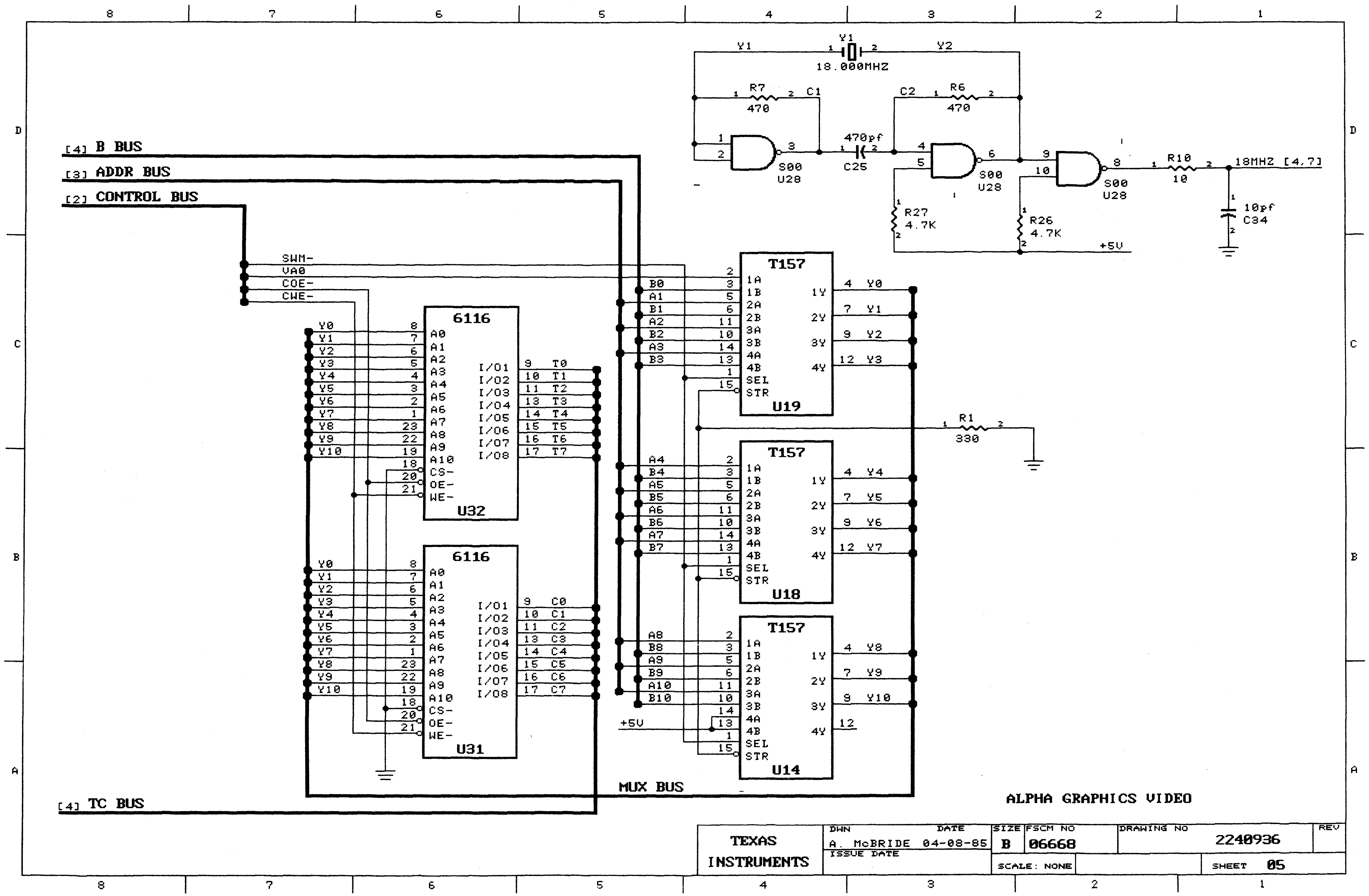
43 DB

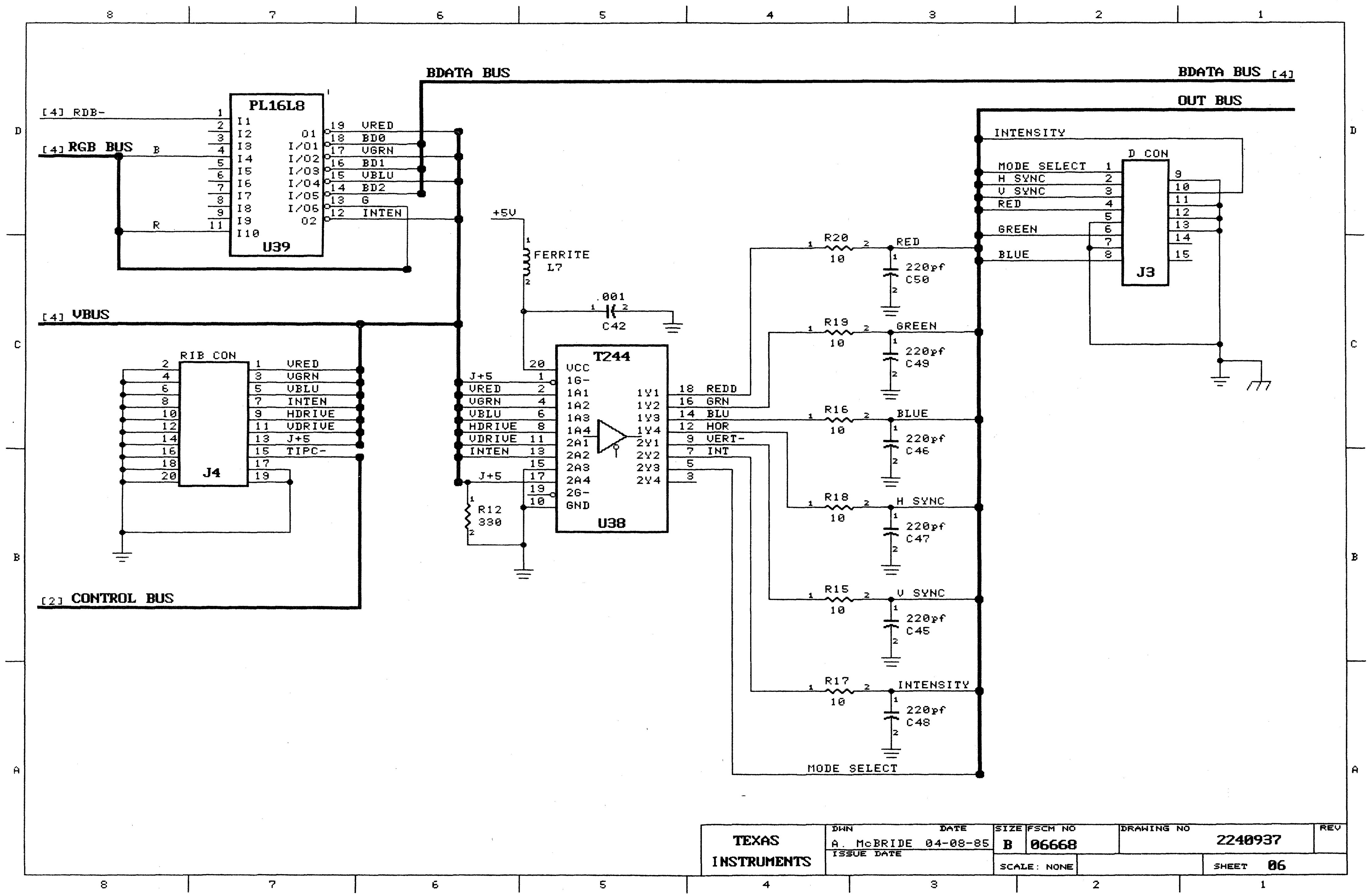

[3,4,7] XDATA BUS
[3] XADDR BUS
NMI- 1
XD7 3
XD6 5
XD5 7
XD4 9
XD3 11
XD2 13
XD1 15
XD0 17
WAIT- 19
AEN 21
XA16 29
XA15 31
XA14 33
XA13 35
XA12 37
XA11 39
XA10 41
XA9 43
XA8 45
XA7 47
XA6 49
XA5 51
XA4 53
XA3 55
XA2 57
XA1 59
XA0 61
4 RESET
6 +5V
26 IOWC-
56 BALE
58 +5V
6MHZ [4] [7]
CONTROL BUS [3,4,5,6,7]
COMPONET SIDE
P1
XBHE- 1
BA23 3
BA22 5
BA21 7
BA20 9
BA19 11
BA18 13
BA17 15
MRDC- 17
MWTC- 19
XD8 21
XD9 23
XD10 25
XD11 27
XD12 29
XD13 31
XD14 33
XD15 35
32 +5V
34 MASTER-
COMP SIDE
P2
+5V
L3 FERRITE
L6 FERRITE
+5VU28
+5VU39
.001 C29 50V
.01 C43 50V
EXPANSION BUS CONNECTORS
TEXAS INSTRUMENTS
DWN A. McBRIDE DATE 04-08-85
ISSUE DATE
SIZE B FSCM NO 06668
DRAWING NO 2240936
REV
SCALE: NONE
SHEET 02


XADDR BUS [2]
CONTROL BUS [2]
IOWC-
RESET
+5V
R28
4.7K
S00
U28
RST-
T138
U34
XA9
XA8
XA6
XA5
XA4
DEC1-
DEC2-
AS27
U15
IODEC
AT00
U13
NODMA
MASTER-
AEN
IOPORT-
AT244
U27
MRDC-
MWTC-
TIPC
XA0
XA3
XA2
XA1
BMRDC-
BMWTC-
A0
A4
A3
A2
A1
ADDR BUS [4,5,7]
PL16L8A
U30
XA1
XA2
XA3
XA7
XA0
CUR
A17
CRTEN
A18
ADD7
WAIT-
AGVWT-
BRDCMD-
TIPC-
VGCUR
XD1
AS74
U16
T244
U35
XA5
XA6
XA7
XA8
XA12
XA11
XA10
XA9
A5
A6
A7
A8
A12
A11
A10
A9
XDATA BUS [2]
CONTROL BUS [2]
VGCUR [4]
TC BUS [4]
CUR [4]
BA17
BA18
AS04
U26
T373
U36
XA13
XA14
XA15
XA16
BA17-
BA18-
XADD7
XBHE-
TIPC-
BALE
A13
A14
A15
A16
A17
A18
ADD7
BHE-
+5V
R22
300
LED
R23
47
CR1
T138
U29
BA23
BA22
BA21
BA19
BA20
XADD7-
R25
4.7K
ALPHA GRAPHICS VIDEO
TEXAS INSTRUMENTS
DWN A. McBRIDE
DATE 04-08-85
ISSUE DATE
SIZE B
FSCM NO 06668
DRAWING NO 2240936
REV
SCALE: NONE
SHEET 03

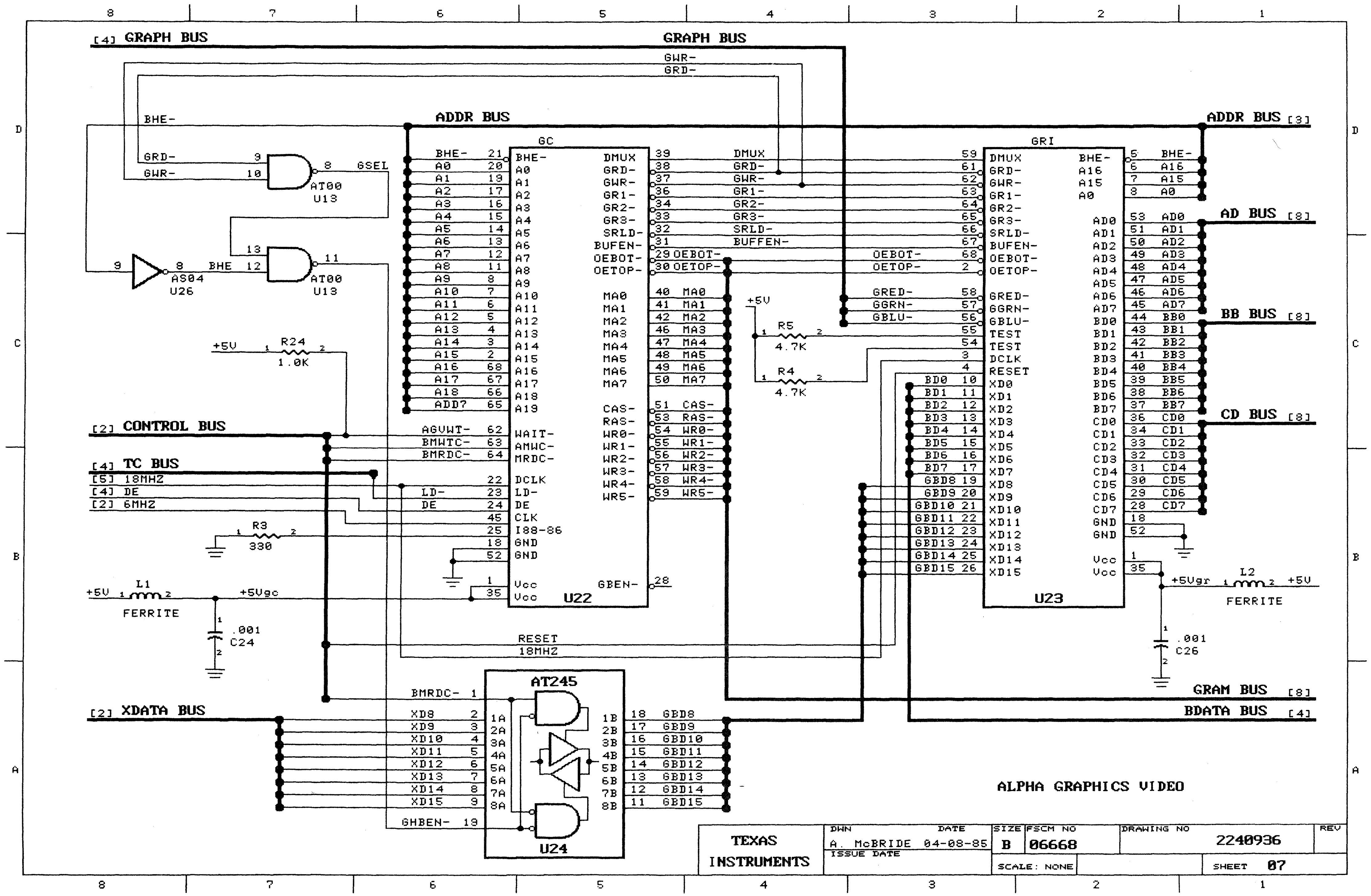


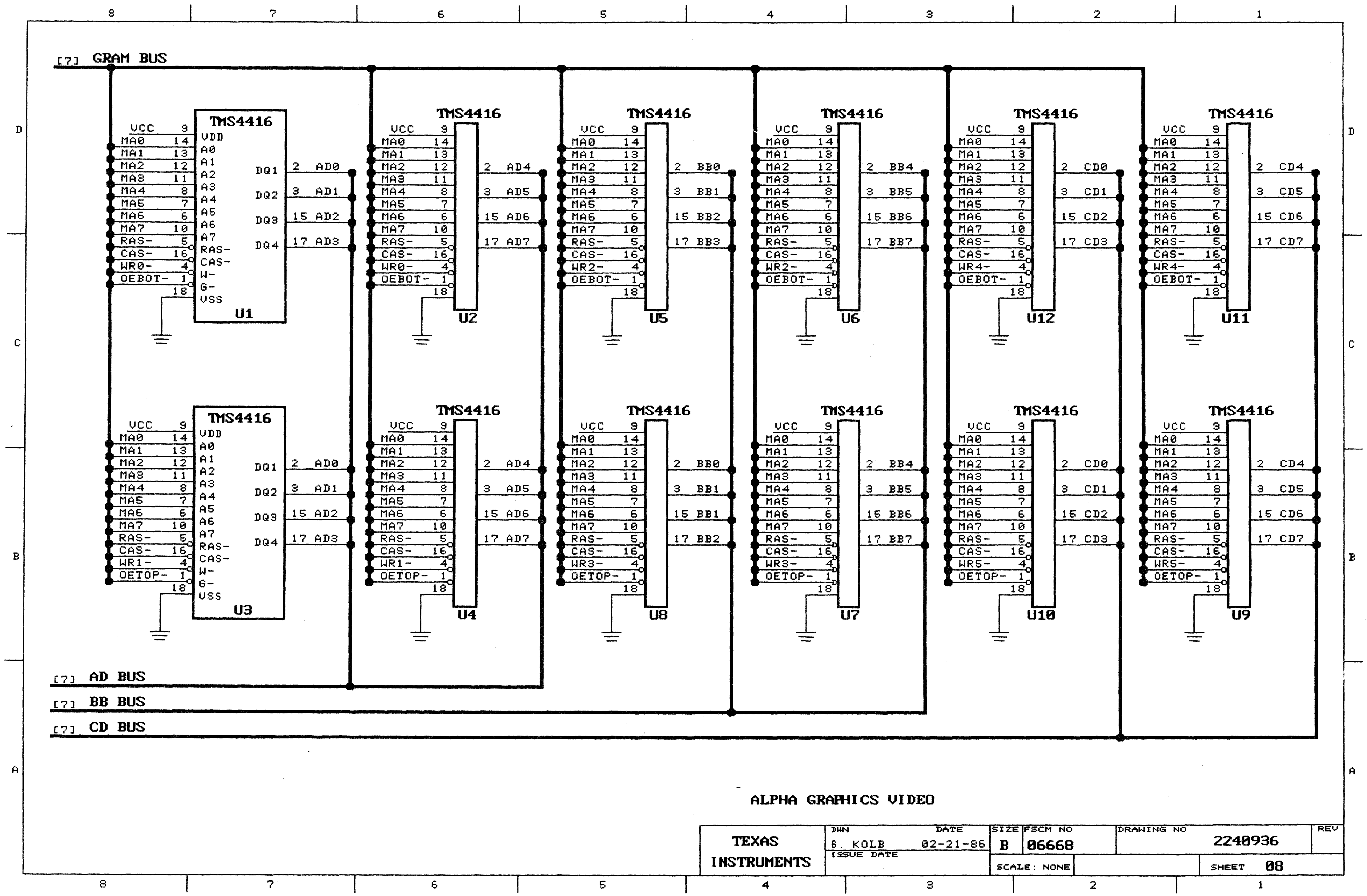
[2] CONTROL BUS
[2] XDATA BUS
BMRDC-
AT245
U37
ZBEN-
AT244
U21
WRH-
[2] 6MHZ
T373
U20
[6] RDB-
RDH-
VA0
R8 330
R9 330
DABS
U25
+5V
L4 FERRITE
.001 C32 5V
BDATA BUS [6,7]
ADDR BUS [3]
CONTROL BUS [2]
SY6845EA
U17
B BUS [5]
E1
E2
R2 4.7K
DE [7]
CUR [3]
VS
U33
VGCUR [3]
R11 4.7K +5V
RGB BUS [6]
R14 4.7K
GRAPH BUS [7]
AS04 U26
VDRIVE
VBUS [6]
C35 .001uF
FERRITE L5
TC BUS [3,5,7]
18MHZ [5]
TEXAS INSTRUMENTS
DWN A. McBRIDE
DATE 04-08-85
ISSUE DATE
SIZE B
FSCM NO 06668
DRAWING NO 2240936
REV
SCALE: NONE
SHEET 04

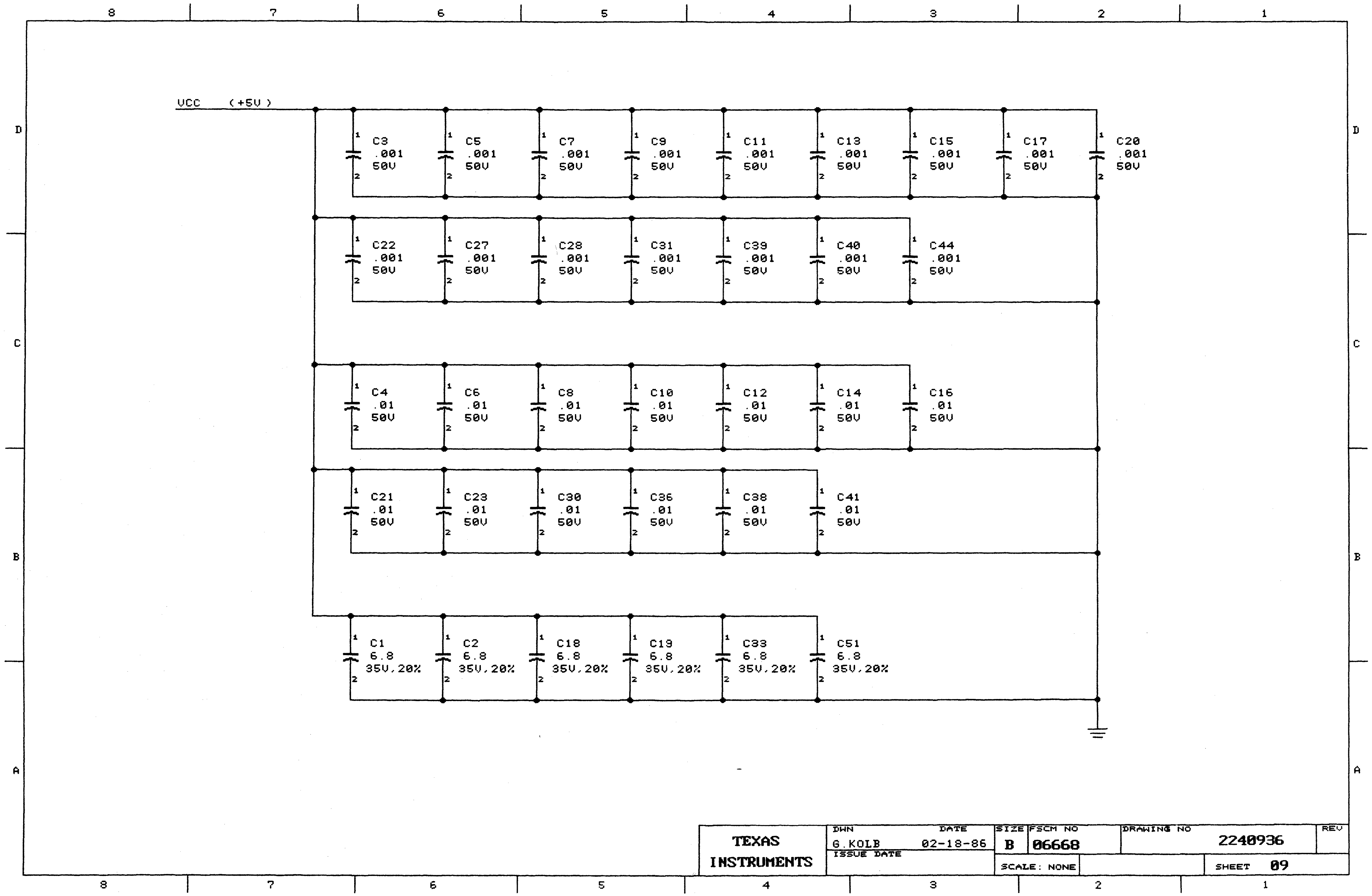

Y1
18.000MHZ
Y2
R7
470
C1
C2
R6
470
470pf
C25
S00
U28
R10
10
18MHZ [4,7]
10pf
C34
R27
4.7K
R26
4.7K
+5V
[4] B BUS
[3] ADDR BUS
[2] CONTROL BUS
SWM-
VA0
COE-
CWE-
6116
U32
6116
U31
T157
U19
T157
U18
T157
U14
R1
330
+5V
MUX BUS
[4] TC BUS
ALPHA GRAPHICS VIDEO
TEXAS INSTRUMENTS
DWN
DATE
A. McBRIDE 04-08-85
ISSUE DATE
SIZE
B
FSCM NO
06668
DRAWING NO
2240936
REV
SCALE: NONE
SHEET 05



BDATA BUS
BDATA BUS [4]
OUT BUS
[4] RDB-
[4] RGB BUS
PL16L8
U39
VRED
BD0
VGRN
BD1
VBLU
BD2
G
INTEN
[4] VBUS
RIB CON
J4
VRED
VGRN
VBLU
INTEN
HDRIVE
VDRIVE
J+5
TIPC-
[2] CONTROL BUS
+5V
FERRITE L7
.001 C42
T244
U38
R12 330
REDD
GRN
BLU
HOR
VERT-
INT
R20 10
RED
220pf C50
R19 10
GREEN
220pf C49
R16 10
BLUE
220pf C46
R18 10
H SYNC
220pf C47
R15 10
V SYNC
220pf C45
R17 10
INTENSITY
220pf C48
MODE SELECT
INTENSITY
D CON
MODE SELECT
H SYNC
V SYNC
RED
GREEN
BLUE
J3
TEXAS INSTRUMENTS
DWN A. McBRIDE
DATE 04-08-85
ISSUE DATE
SIZE B
FSCM NO 06668
SCALE: NONE
DRAWING NO 2240937
REV
SHEET 06


GRAPH BUS
ADDR BUS
AD BUS
BB BUS
CD BUS
CONTROL BUS
TC BUS
XDATA BUS
GRAM BUS
BDATA BUS
GC
GRI
U22
U23
U24
AT245
AT00
U13
AS04
U26
R24 1.0K
R3 330
R5 4.7K
R4 4.7K
L1 FERRITE
L2 FERRITE
C24 .001
C26 .001
ALPHA GRAPHICS VIDEO
TEXAS INSTRUMENTS
A. McBRIDE 04-08-85
B
06668
2240936
SCALE: NONE
SHEET 07


[7] GRAM BUS
TMS4416
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
[7] AD BUS
[7] BB BUS
[7] CD BUS
ALPHA GRAPHICS VIDEO
TEXAS INSTRUMENTS
DWN G. KOLB DATE 02-21-86
ISSUE DATE
SIZE B
FSCM NO 06668
DRAWING NO 2240936
REV
SCALE: NONE
SHEET 08


VCC (+5V)
C3 .001 50V
C5 .001 50V
C7 .001 50V
C9 .001 50V
C11 .001 50V
C13 .001 50V
C15 .001 50V
C17 .001 50V
C20 .001 50V
C22 .001 50V
C27 .001 50V
C28 .001 50V
C31 .001 50V
C39 .001 50V
C40 .001 50V
C44 .001 50V
C4 .01 50V
C6 .01 50V
C8 .01 50V
C10 .01 50V
C12 .01 50V
C14 .01 50V
C16 .01 50V
C21 .01 50V
C23 .01 50V
C30 .01 50V
C36 .01 50V
C38 .01 50V
C41 .01 50V
C1 6.8 35V, 20%
C2 6.8 35V, 20%
C18 6.8 35V, 20%
C19 6.8 35V, 20%
C33 6.8 35V, 20%
C51 6.8 35V, 20%
TEXAS INSTRUMENTS
DWN G.KOLB DATE 02-18-86
ISSUE DATE
SIZE B FSCM NO 06668
DRAWING NO 2240936
REV
SCALE: NONE
SHEET 09

2240939 DRAWING NO | 1 SH

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

NOTES, UNLESS OTHERWISE SPECIFIED:

1. ALL DEVICES ARE PREFIXED WITH SN74. A LETTER "T" IN A PREFIX IS EQUAL TO "LS", EXCEPT WHEN USED AS A SUFFIX. "AT" IS EQUAL TO "ALS", AND A LETTER "F" AS A SUFFIX IS EQUAL TO A CHIP CARRIER
2. VCC IS APPLIED TO PIN 8 OF ALL 8-PIN IC's, PIN 14 OF ALL 14-PIN IC's, PIN 16 OF ALL 16-PIN IC's, PIN 20 OF ALL 20-PIN IC's, ETC
3. GROUND IS APPLIED TO PIN 4 OF ALL 8-PIN IC's, PIN 7 OF ALL 14-PIN IC's, PIN 8 OF ALL 16-PIN IC's, PIN 10 OF ALL 20-PIN IC's, ETC
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1, 2, AND 3 = PIN NUMBERS
U06 AND U07 = REFERENCE DESIGNATORS

5. RESISTANCE VALUES ARE IN OHMS
6. RESISTORS ARE 1/4 WATT, 5%
7. CAPACITANCE VALUES ARE IN MICROFARADS

29

COMPUTER GENERATED DRAWING ; DO NOT REVISE MANUALLY

-1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES

PARTS LIST

REV										
SH	11	12								
REV										
SH	1	2	3	4	5	6	7	8	9	10

REVISION STATUS OF SHEETS

NEXT ASSY	USED ON
2240940	8721

APPLICATION

UNLESS OTHERWISE SPECIFIED
* DIMENSIONS ARE IN INCHES
* TOLERANCES: ANGLES +/-1 DEG
  3 PLACE DECIMALS +/-.010
  2 PLACE DECIMALS +/-.02
* INTERPRET DRAWING PER MIL-D-1000
* REMOVE BURRS AND SHARP EDGES
* CONCENTRICITY MACHINED DIAMETERS .010 FIM
* DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
* PARENTHETICAL INFO FOR REF ONLY

HOLE TOLERANCE

.013 THRU .125 +.004 -.001	.126 THRU .250 +.005 -.001	.251 THRU .500 +.006 -.001
.501 THRU .750 +.008 -.001	.751 THRU 1.000 +.010 -.001	1.001 THRU 2.000 +.012 -.001

		DATE
DWN	F. ROTH	10-30-84
CHK	[signature]	4/19/85
ENGR	[signature]	4/22/85
APVD ENGR	Bruce Sawtelle	4/22/85
QA	[signature]	4/29
APVD MFG	[signature]	4/29/85
RELEASE	[signature]	4/29/85

TEXAS INSTRUMENTS
Data Systems Group

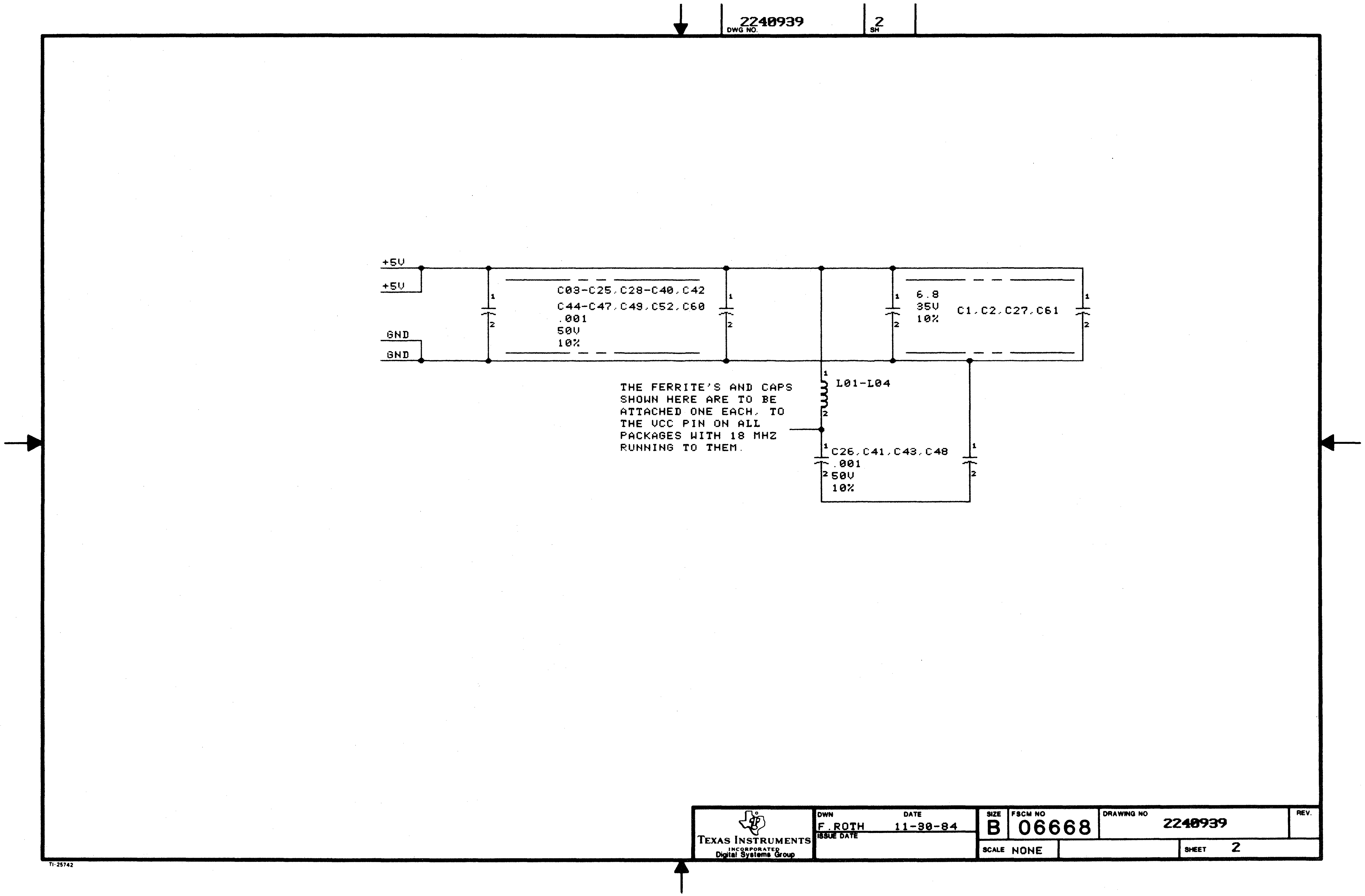
DIAGRAM, LOGIC, DETAILED-DUAL MODE VIDEO BOARD

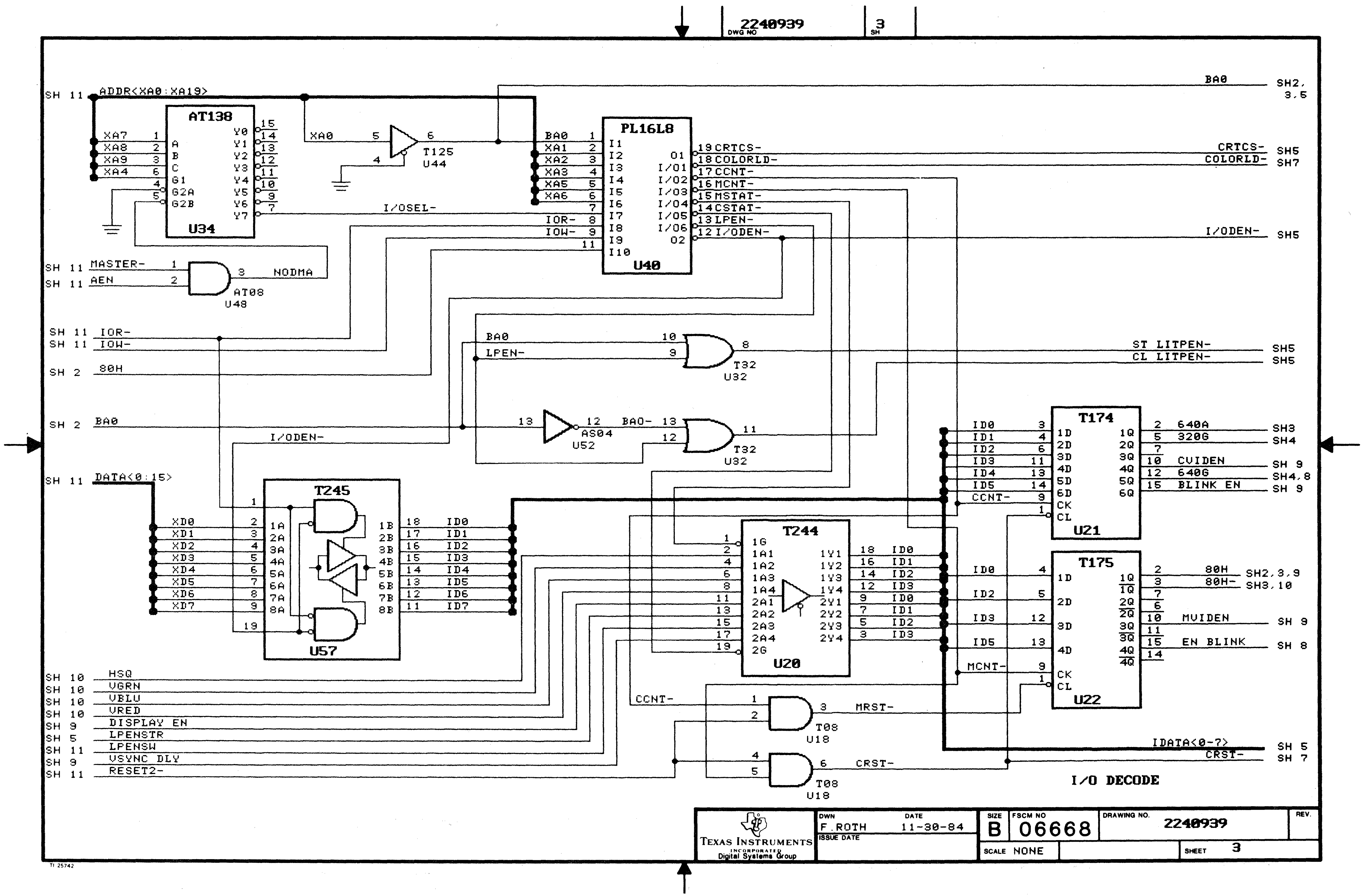
SIZE	FSCM NO	DRAWING NO
B	06668	2240939

SCALE NONE | SHEET 1 OF 12

430 DB

FILMED


2240939
DWG NO.
2
SH
+5V
+5V
GND
GND
C03-C25,C28-C40,C42
C44-C47,C49,C52,C60
.001
50V
10%
6.8
35V
10%
C1,C2,C27,C61
L01-L04
THE FERRITE'S AND CAPS SHOWN HERE ARE TO BE ATTACHED ONE EACH, TO THE VCC PIN ON ALL PACKAGES WITH 18 MHZ RUNNING TO THEM.
C26,C41,C43,C48
.001
50V
10%
TEXAS INSTRUMENTS
INCORPORATED
Digital Systems Group
DWN
F. ROTH
DATE
11-90-84
ISSUE DATE
SIZE
B
FSCM NO
06668
DRAWING NO
2240939
REV.
SCALE
NONE
SHEET
2


2240939
3
AT138
U34
PL16L8
U40
T125
U44
AT08
U48
T32
U32
AS04
U52
T245
U57
T244
U20
T174
U21
T175
U22
T08
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I/ODEN-
NODMA
MASTER-
AEN
IOR-
IOW-
80H
BA0
LPEN-
ST LITPEN-
CL LITPEN-
CRTCS-
COLORLD-
CCNT-
MCNT-
MSTAT-
CSTAT-
LPEN-
640A
320G
CUIDEN
640G
BLINK EN
80H-
MUIDEN
EN BLINK
MRST-
CRST-
HSQ
VGRN
VBLU
VRED
DISPLAY EN
LPENSTR
LPENSW
VSYNC DLY
RESET2-
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11-30-84
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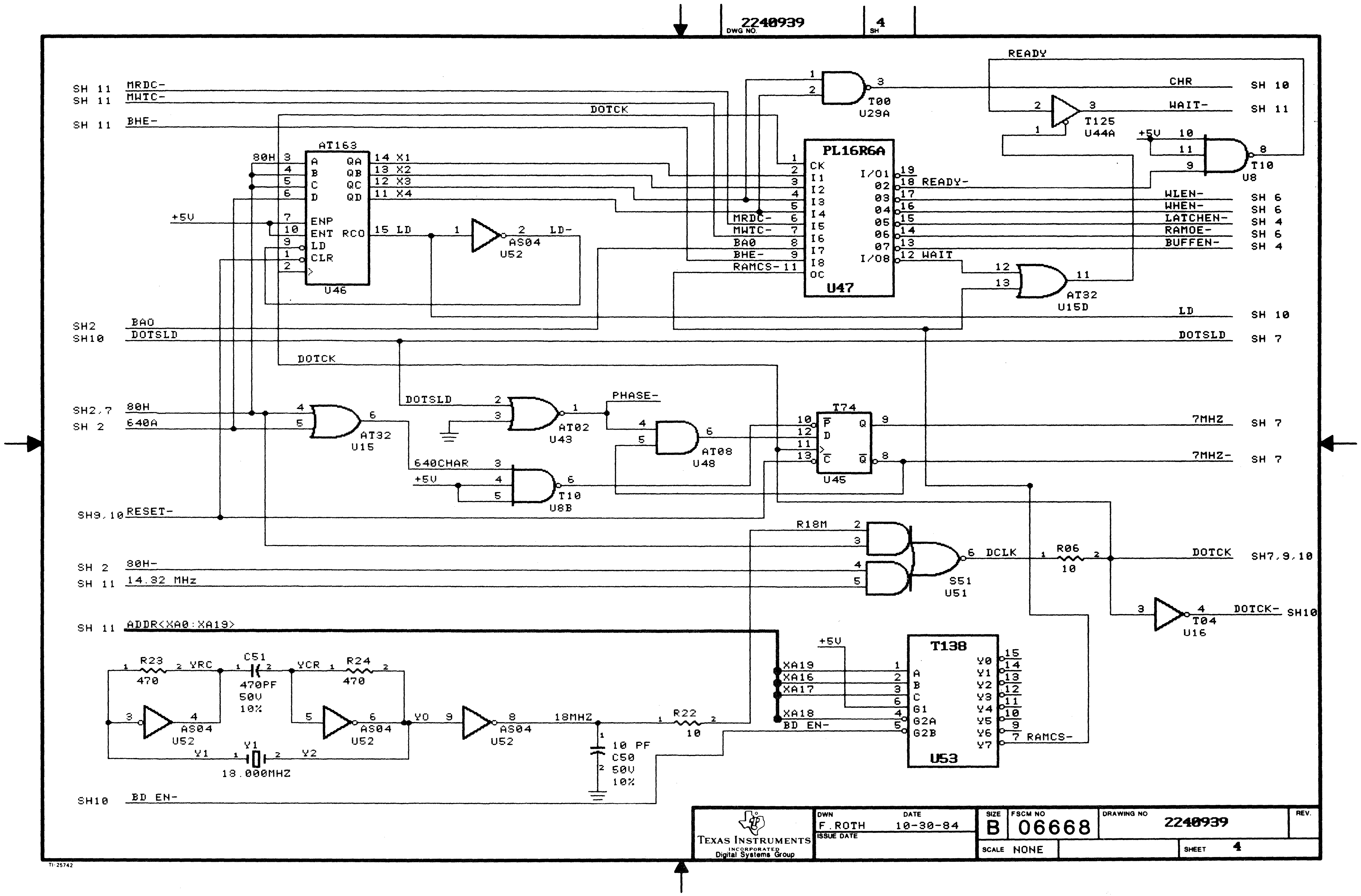
SHEET 3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U47
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CHR
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WHEN-
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RAMOE-
BUFFEN-
LD
DOTSLD
DOTCK
7MHZ
7MHZ-
DCLK
DOTCK-
MRDC-
MWTC-
BHE-
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RESET-
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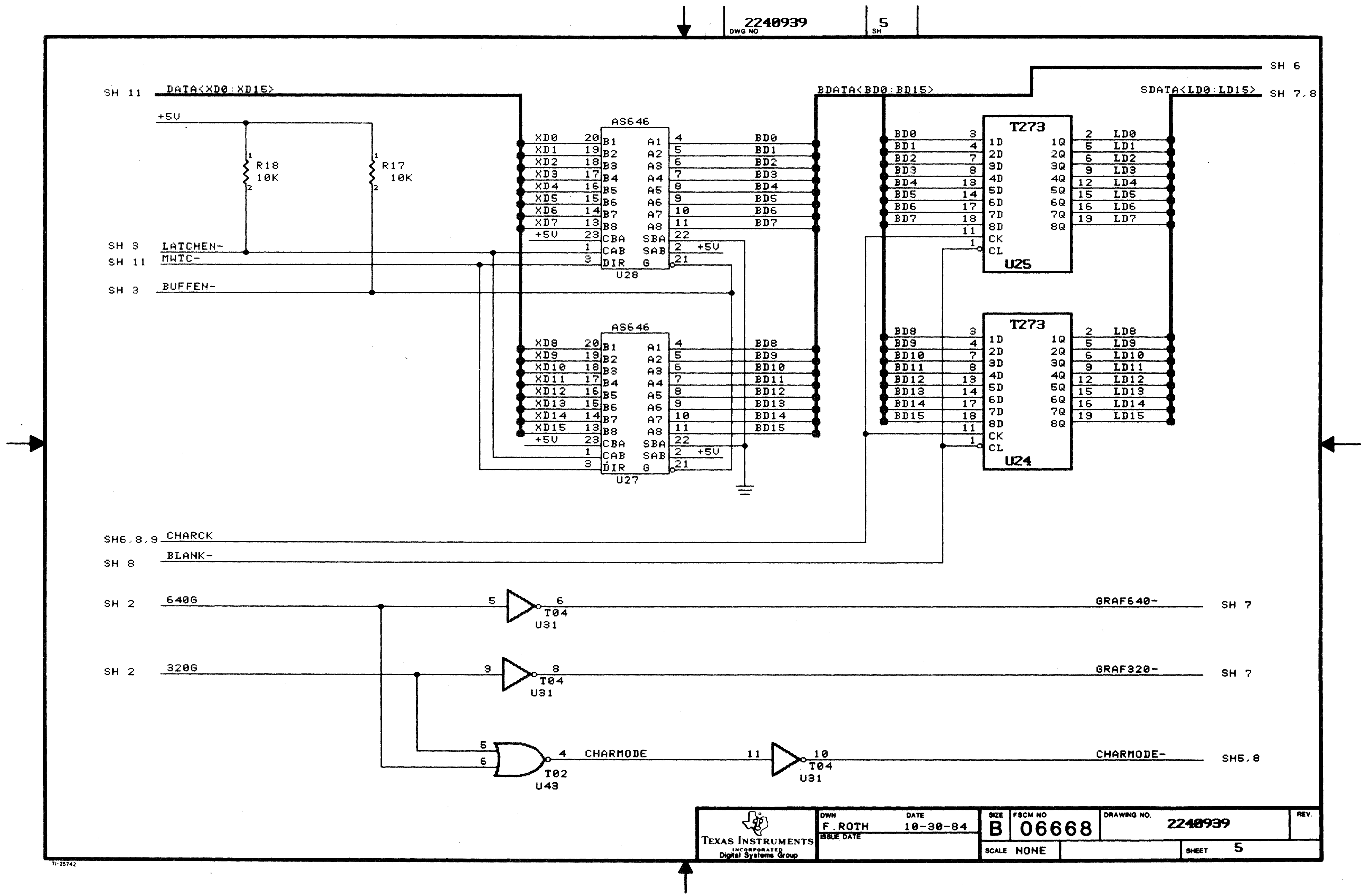
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R18 10K
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SH 3 LATCHEN-
SH 11 MWTC-
SH 3 BUFFEN-
AS646
U28
U27
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SH 6
SDATA<LD0:LD15> SH 7,8
T273
U25
U24
SH6,8,9 CHARCK
SH 8 BLANK-
SH 2 640G
T04 U31
GRAF640- SH 7
SH 2 320G
GRAF320- SH 7
T02 U43
CHARMODE
CHARMODE- SH5,8
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Digital Systems Group
F.ROTH 10-30-84
B 06668
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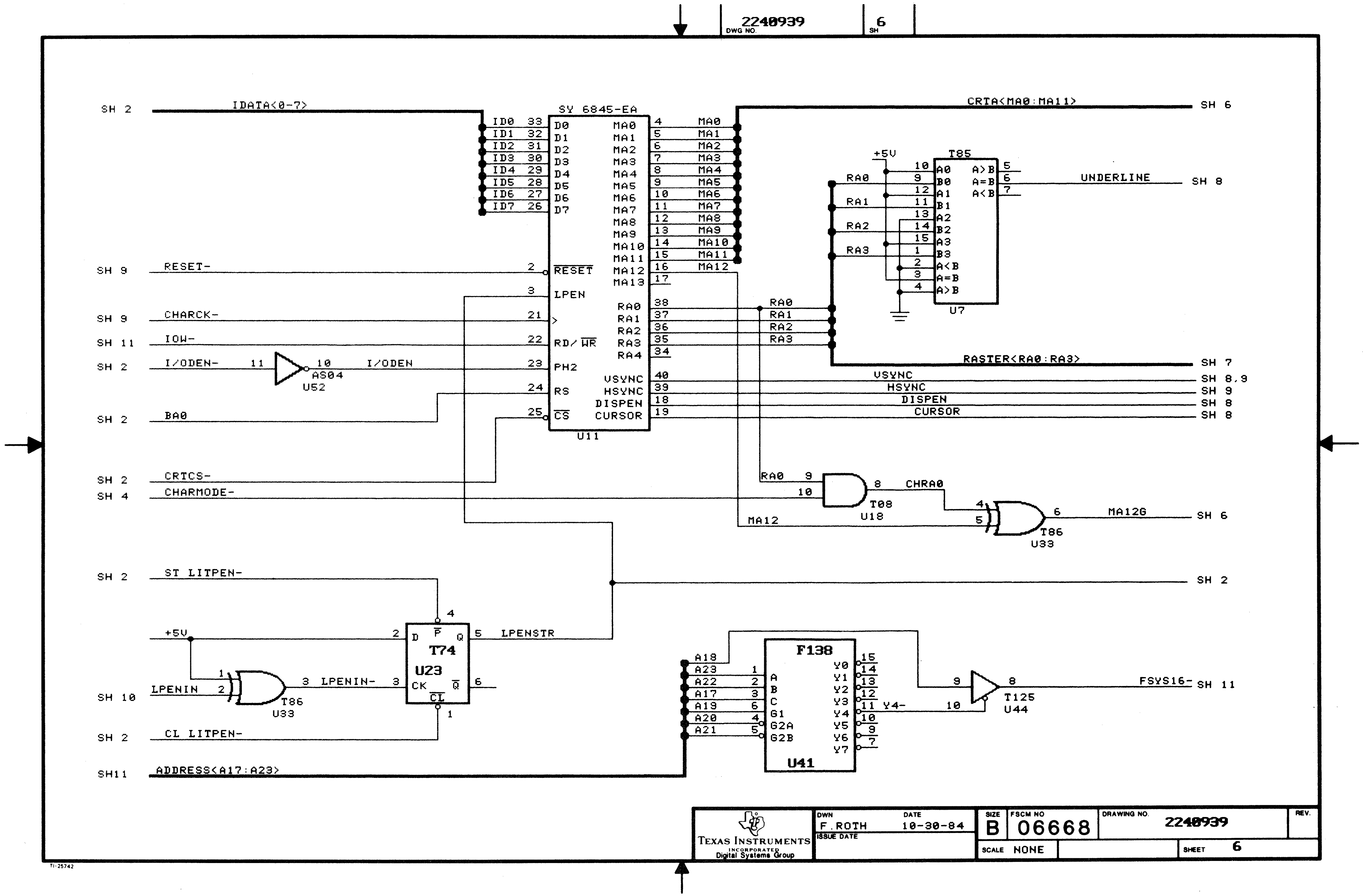
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SH 6
T85
U7
UNDERLINE
SH 8
RASTER<RA0:RA3>
SH 7
VSYNC
HSYNC
DISPEN
CURSOR
SH 9
RESET-
CHARCK-
SH 11
IOW-
I/ODEN-
AS04
U52
BA0
U11
CRTCS-
SH 4
CHARMODE-
CHRA0
T08
U18
MA12
MA12G
T86
U33
ST LITPEN-
+5V
LPENSTR
T74
U23
SH 10
LPENIN
LPENIN-
CL LITPEN-
ADDRESS<A17:A23>
F138
U41
T125
U44
FSYS16-
TEXAS INSTRUMENTS
Digital Systems Group
F.ROTH
10-30-84
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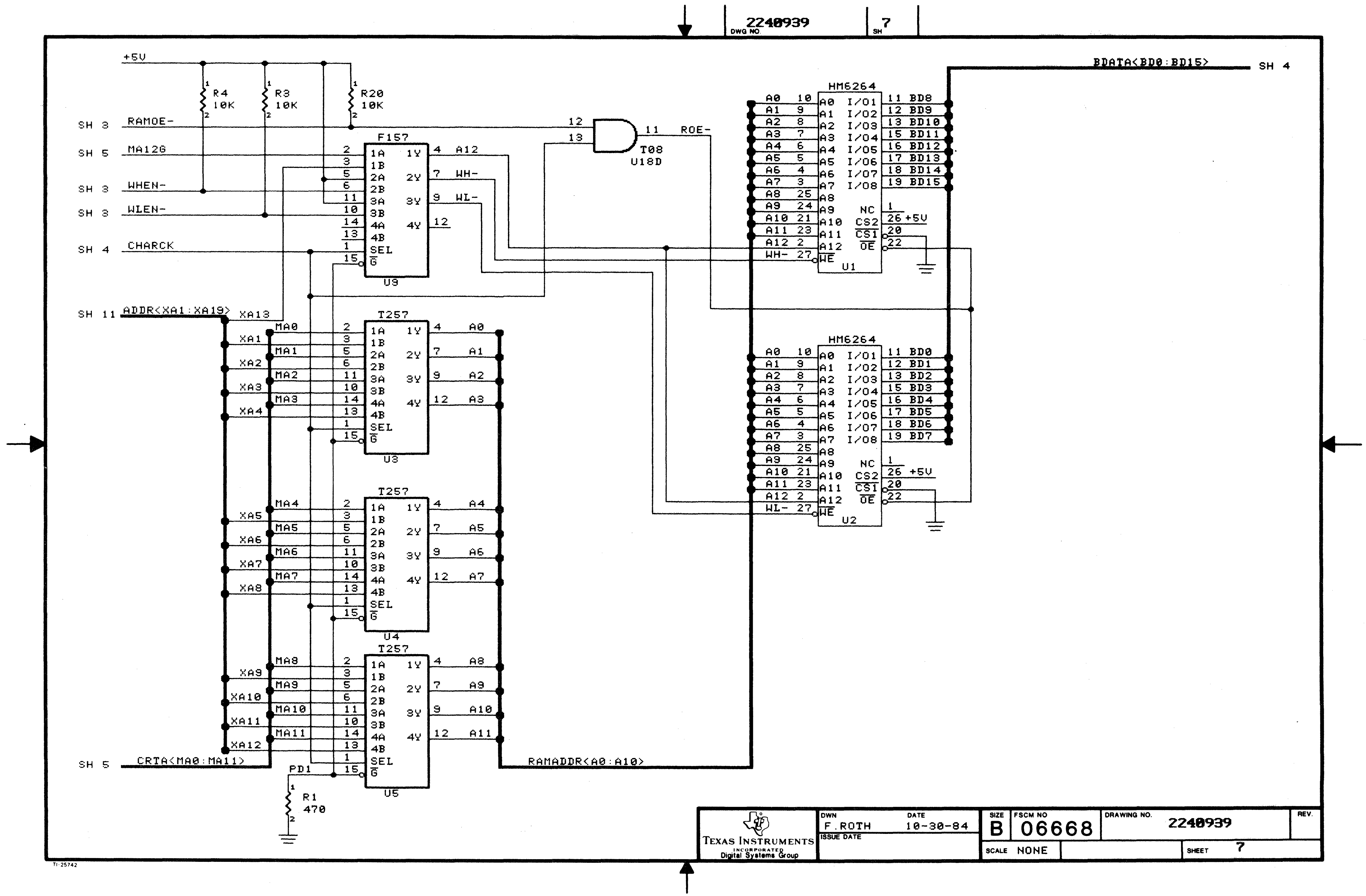
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+5V
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R3 10K
R20 10K
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SH 5 MA12G
SH 3 WHEN-
SH 3 WLEN-
SH 4 CHARCK
SH 11 ADDR<XA1:XA19>
SH 5 CRTA<MA0:MA11>
F157
U9
T257
U3
U4
U5
T08
U18D
ROE-
A12
WH-
WL-
PD1
R1 470
RAMADDR<A0:A10>
BDATA<BD0:BD15>
SH 4
HM6264
U1
U2
+5V
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Digital Systems Group
F.ROTH
10-30-84
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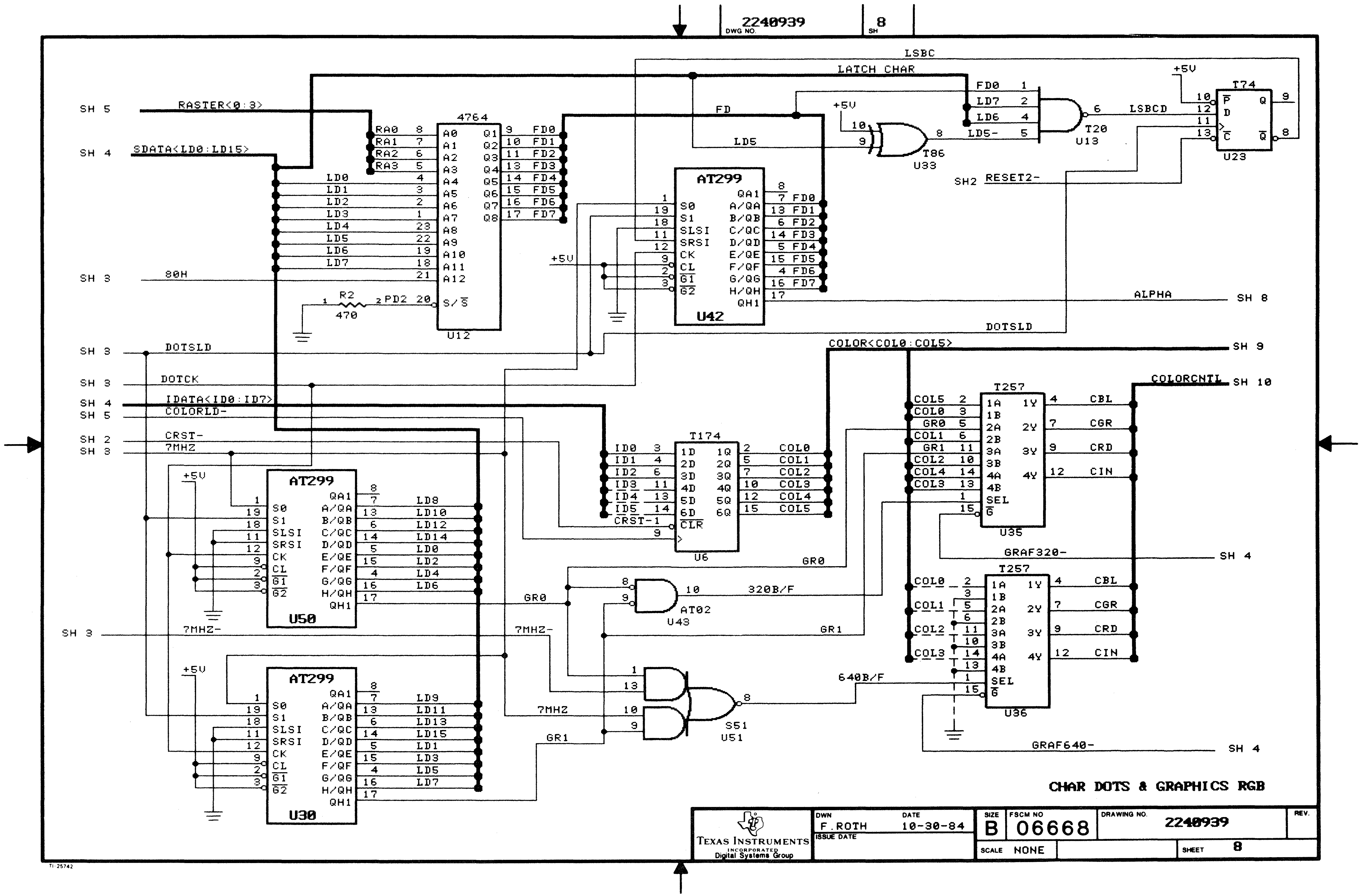
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8
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LATCH CHAR
+5V
T74
FD0 1
LD7 2
LD6 4
LD5- 5
6 LSBCD
T20
U13
U23
FD
LD5
+5V
T86
U33
SH2 RESET2-
SH 5 RASTER<0:3>
SH 4 SDATA<LD0:LD15>
4764
RA0
RA1
RA2
RA3
LD0
LD1
LD2
LD3
LD4
LD5
LD6
LD7
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
S/S̄
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
FD0
FD1
FD2
FD3
FD4
FD5
FD6
FD7
U12
SH 3 80H
R2
470
PD2
AT299
S0
S1
SLSI
SRSI
CK
CL
G1
G2
QA1
A/QA
B/QB
C/QC
D/QD
E/QE
F/QF
G/QG
H/QH
QH1
U42
+5V
ALPHA SH 8
DOTSLD
SH 3 DOTSLD
COLOR<COL0:COL5> SH 9
SH 3 DOTCK
SH 4 IDATA<ID0:ID7>
SH 5 COLORLD-
SH 2 CRST-
SH 3 7MHZ
COLORCNTL SH 10
T257
COL5
COL0
GR0
COL1
GR1
COL2
COL4
COL3
1A
1B
2A
2B
3A
3B
4A
4B
SEL
G
1Y
2Y
3Y
4Y
CBL
CGR
CRD
CIN
U35
GRAF320- SH 4
T174
ID0
ID1
ID2
ID3
ID4
ID5
CRST-
1D
2D
3D
4D
5D
6D
CLR
1Q
2Q
3Q
4Q
5Q
6Q
U6
AT299
U50
LD8
LD10
LD12
LD14
LD0
LD2
LD4
LD6
GR0
320B/F
AT02
U43
SH 3 7MHZ-
7MHZ-
GR1
T257
U36
640B/F
S51
U51
7MHZ
GR1
AT299
U30
LD9
LD11
LD13
LD15
LD1
LD3
LD5
LD7
GRAF640- SH 4
CHAR DOTS & GRAPHICS RGB
TEXAS INSTRUMENTS
INCORPORATED
Digital Systems Group
DWN
F.ROTH
DATE
10-30-84
ISSUE DATE
SIZE
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06668
DRAWING NO.
2240939
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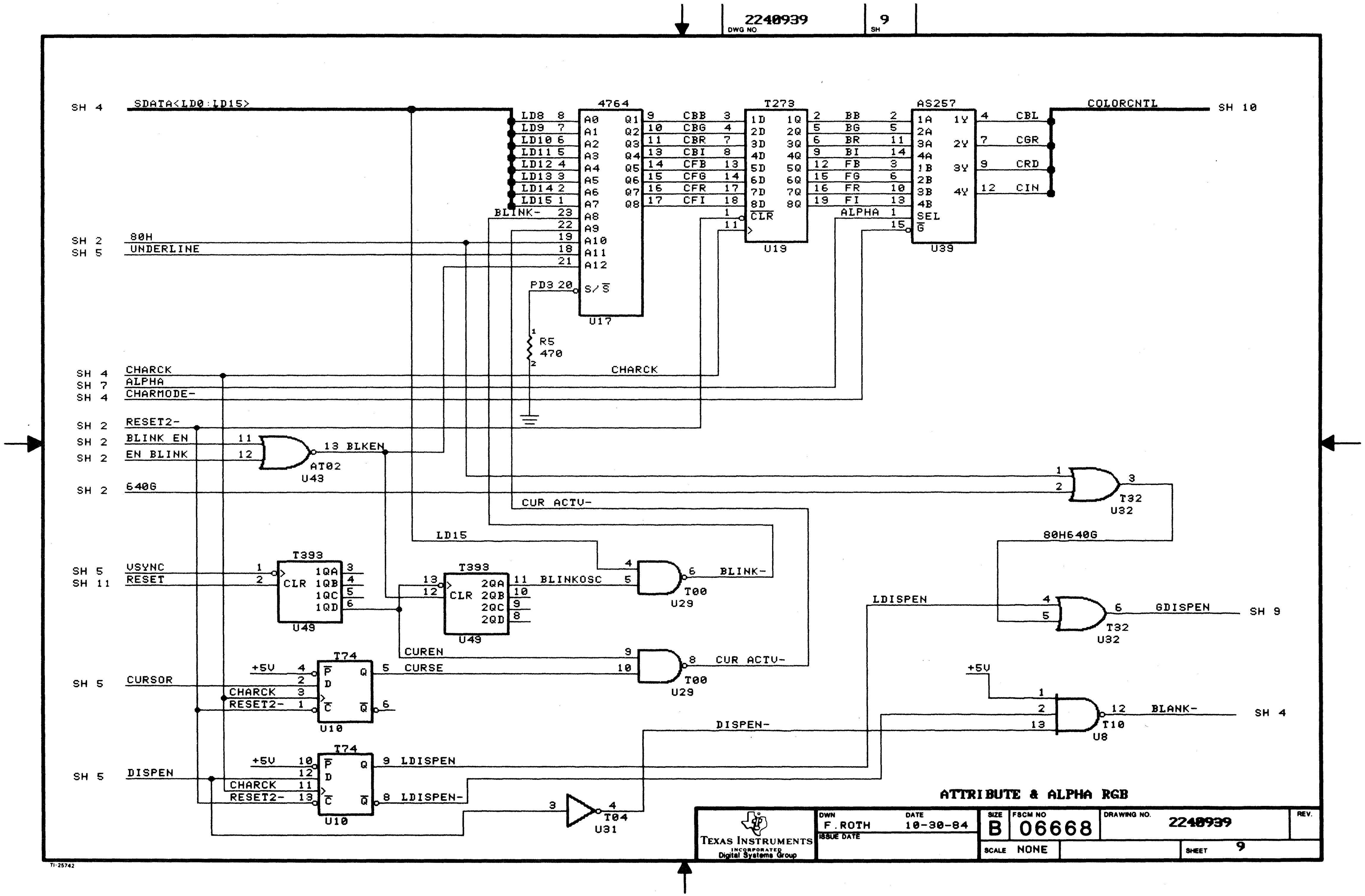
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9
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T273
AS257
COLORCNTL
CBL
CGR
CRD
CIN
U17
U19
U39
BLINK-
80H
UNDERLINE
PD3
R5
470
CHARCK
ALPHA
CHARMODE-
RESET2-
BLINK EN
EN BLINK
BLKEN
AT02
U43
640G
CUR ACTV-
T32
U32
LD15
80H640G
VSYNC
RESET
T393
U49
BLINKOSC
T00
U29
LDISPEN
GDISPEN
CUREN
CURSOR
T74
+5V
CURSE
U10
BLANK-
T10
U8
DISPEN-
DISPEN
LDISPEN-
T04
U31
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TEXAS INSTRUMENTS
Digital Systems Group
F.ROTH
10-30-84
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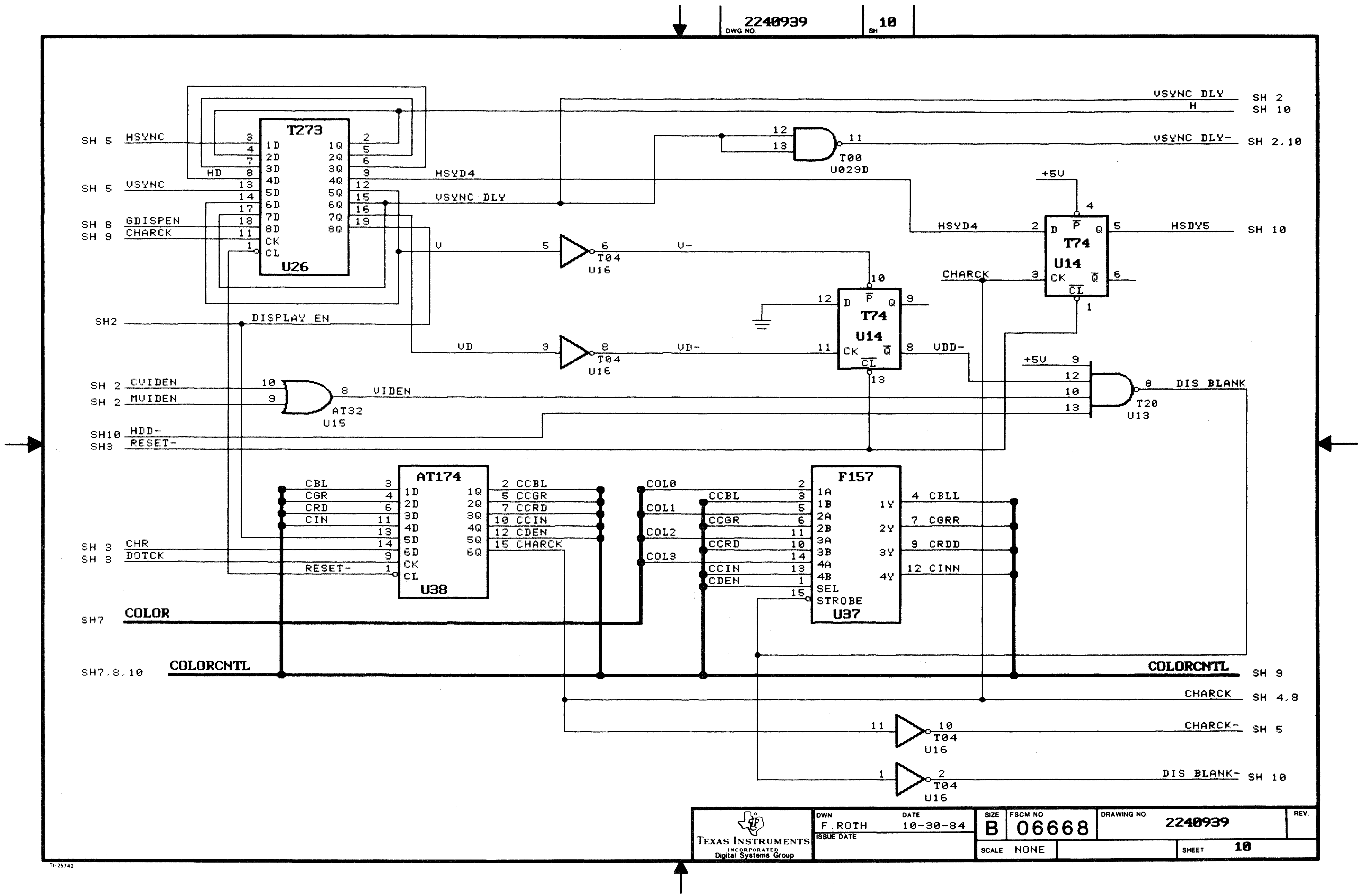
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U26
T74
U14
AT174
U38
F157
U37
AT32
U15
T00
U029D
T04
U16
T20
U13
HSYNC
VSYNC
GDISPEN
CHARCK
DISPLAY EN
CVIDEN
MVIDEN
VIDEN
HDD-
RESET-
CHR
DOTCK
COLOR
COLORCNTL
VSYNC DLY
VSYNC DLY-
HSYD4
HSDY5
DIS BLANK
DIS BLANK-
CHARCK-
TEXAS INSTRUMENTS
F.ROTH
10-30-84
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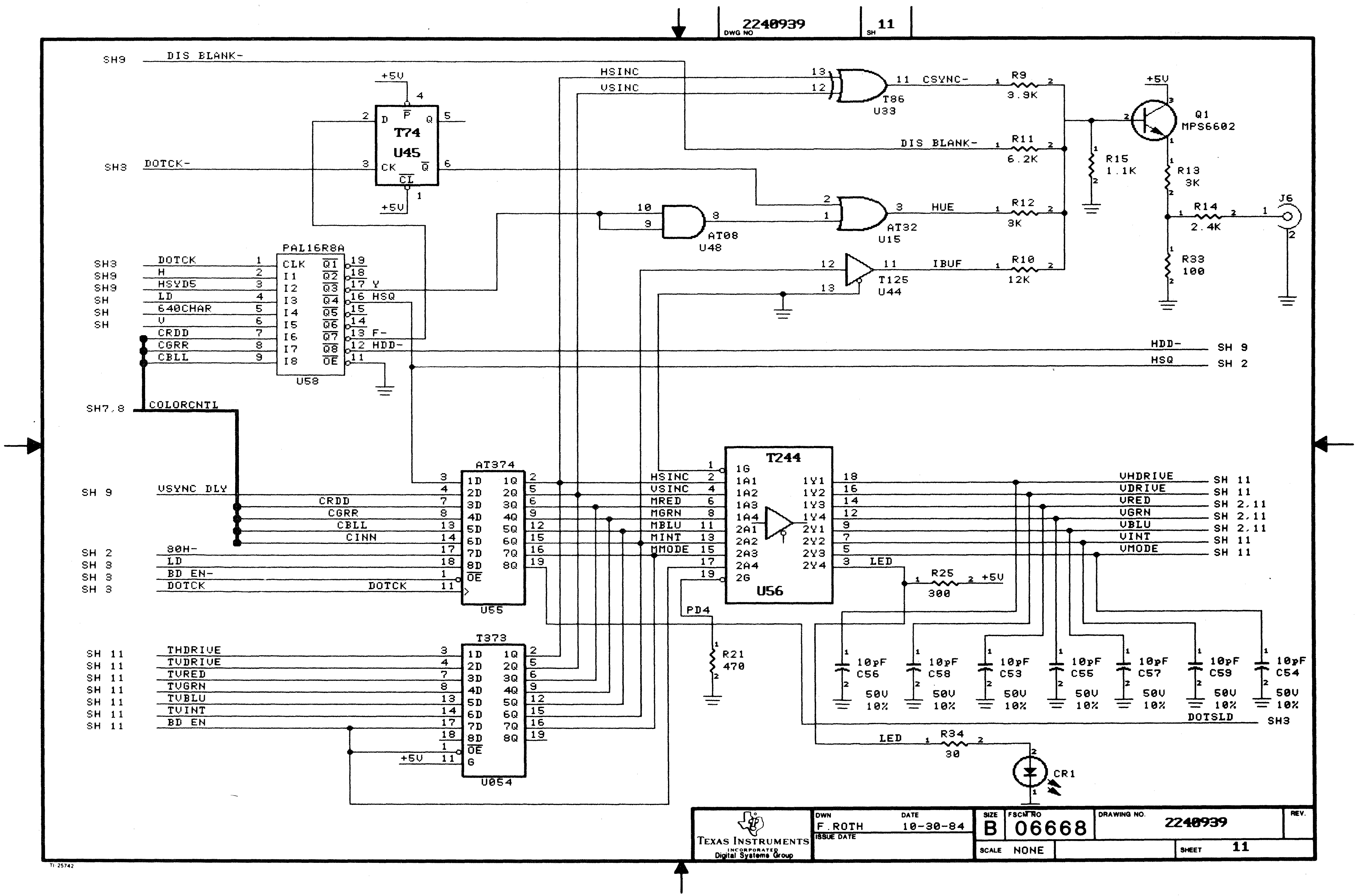

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DWG NO
SH 11
SH9 DIS BLANK-
HSINC
USINC
+5V
T74
U45
SH3 DOTCK-
T86
U33
CSVNC-
R9 3.9K
Q1 MPS6602
DIS BLANK-
R11 6.2K
R15 1.1K
R13 3K
AT08
U48
AT32
U15
HUE
R12 3K
R14 2.4K
J6
T125
U44
IBUF
R10 12K
R33 100
PAL16R8A
U58
DOTCK
H
HSYD5
LD
640CHAR
V
CRDD
CGRR
CBLL
HSQ
HDD-
SH 9
SH 2
SH7,8 COLORCNTL
AT374
U55
T244
U56
SH 9 USYNC DLY
CRDD
CGRR
CBLL
CINN
80H-
LD
BD EN-
DOTCK
HSINC
USINC
MRED
MGRN
MBLU
MINT
MMODE
VHDRIVE
VDRIVE
VRED
VGRN
VBLU
VINT
VMODE
SH 11
SH 2,11
LED
R25 300
+5V
PD4
R21 470
T373
U054
THDRIVE
TVDRIVE
TVRED
TVGRN
TVBLU
TVINT
BD EN
10pF
C56
C58
C53
C55
C57
C59
C54
50V 10%
DOTSLD
SH3
LED
R34 30
CR1
TEXAS INSTRUMENTS INCORPORATED Digital Systems Group
DWN F. ROTH
DATE 10-30-84
ISSUE DATE
SIZE B
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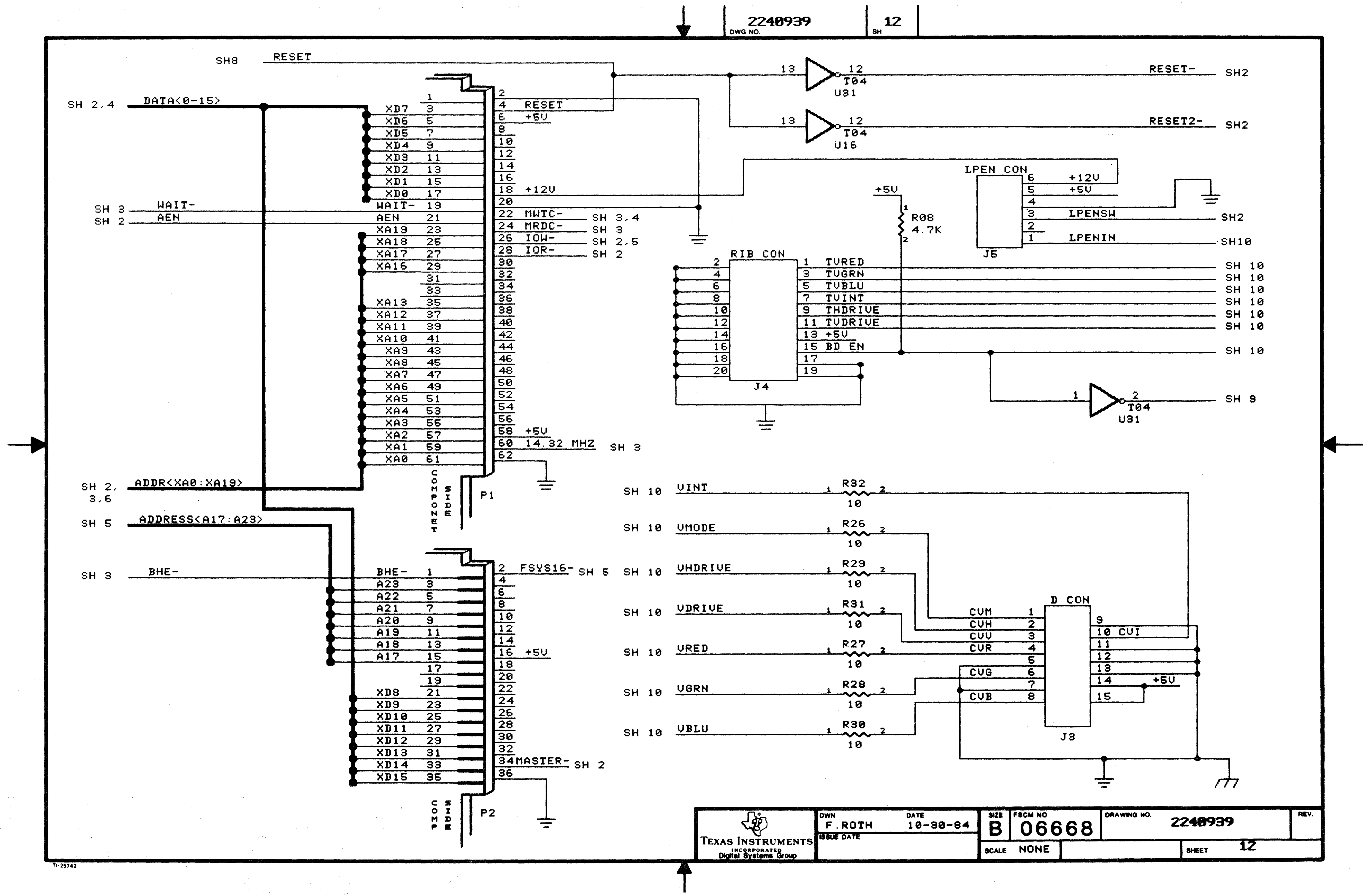
2240939
12
RESET
DATA<0-15>
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BHE-
WAIT-
AEN
RESET-
RESET2-
LPEN CON
RIB CON
D CON
P1
P2
J3
J4
J5
U31
U16
R08 4.7K
VINT
VMODE
VHDRIVE
VDRIVE
VRED
VGRN
VBLU
TVRED
TVGRN
TVBLU
TVINT
THDRIVE
TVDRIVE
BD EN
LPENSW
LPENIN
MWTC-
MRDC-
IOW-
IOR-
14.32 MHZ
FSYS16-
MASTER-
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F.ROTH
10-30-84
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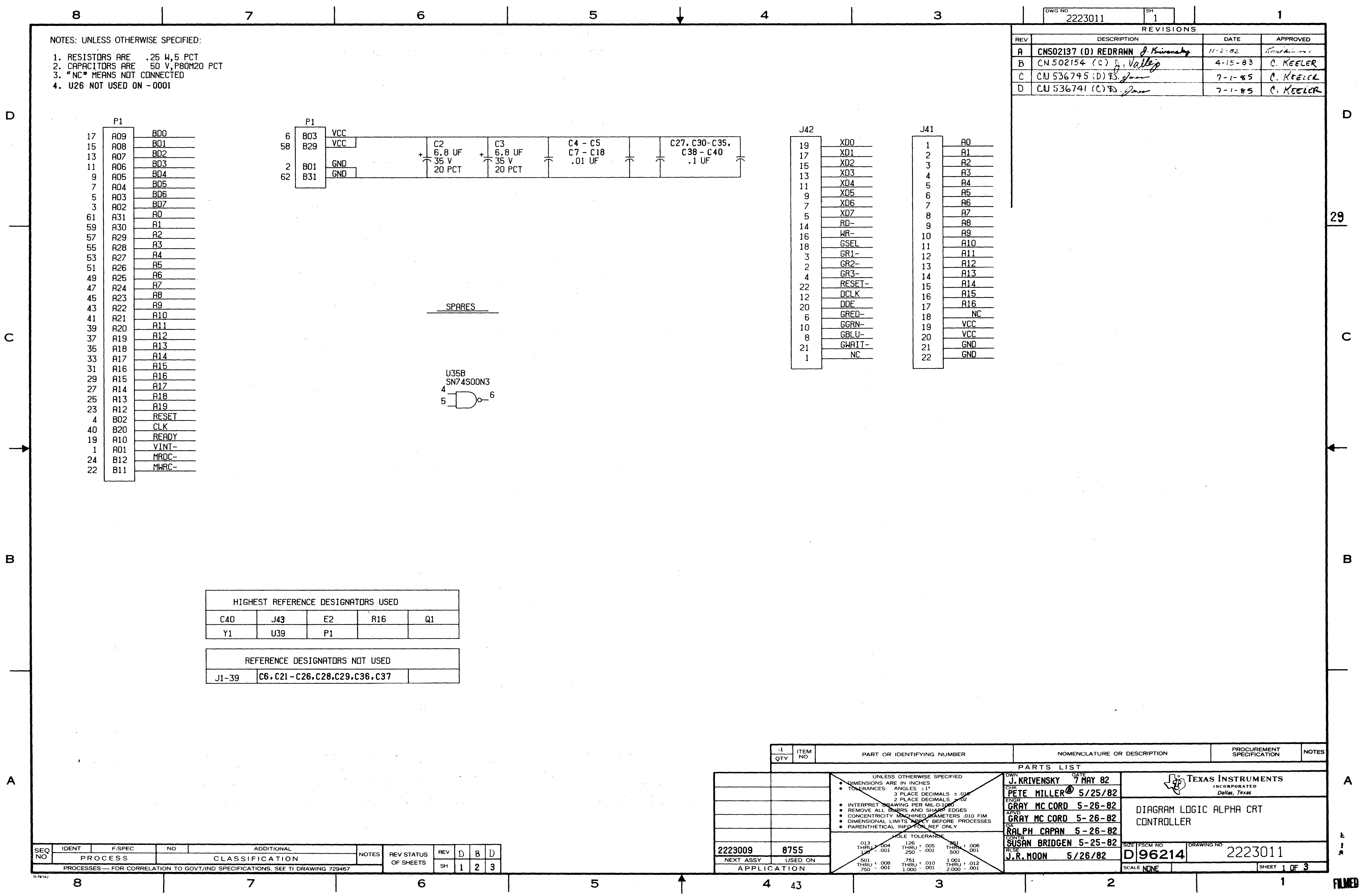

HIGHEST REFERENCE DESIGNATORS USED				
C40	J43	E2	R16	Q1
Y1	U39	P1		

REFERENCE DESIGNATORS NOT USED		
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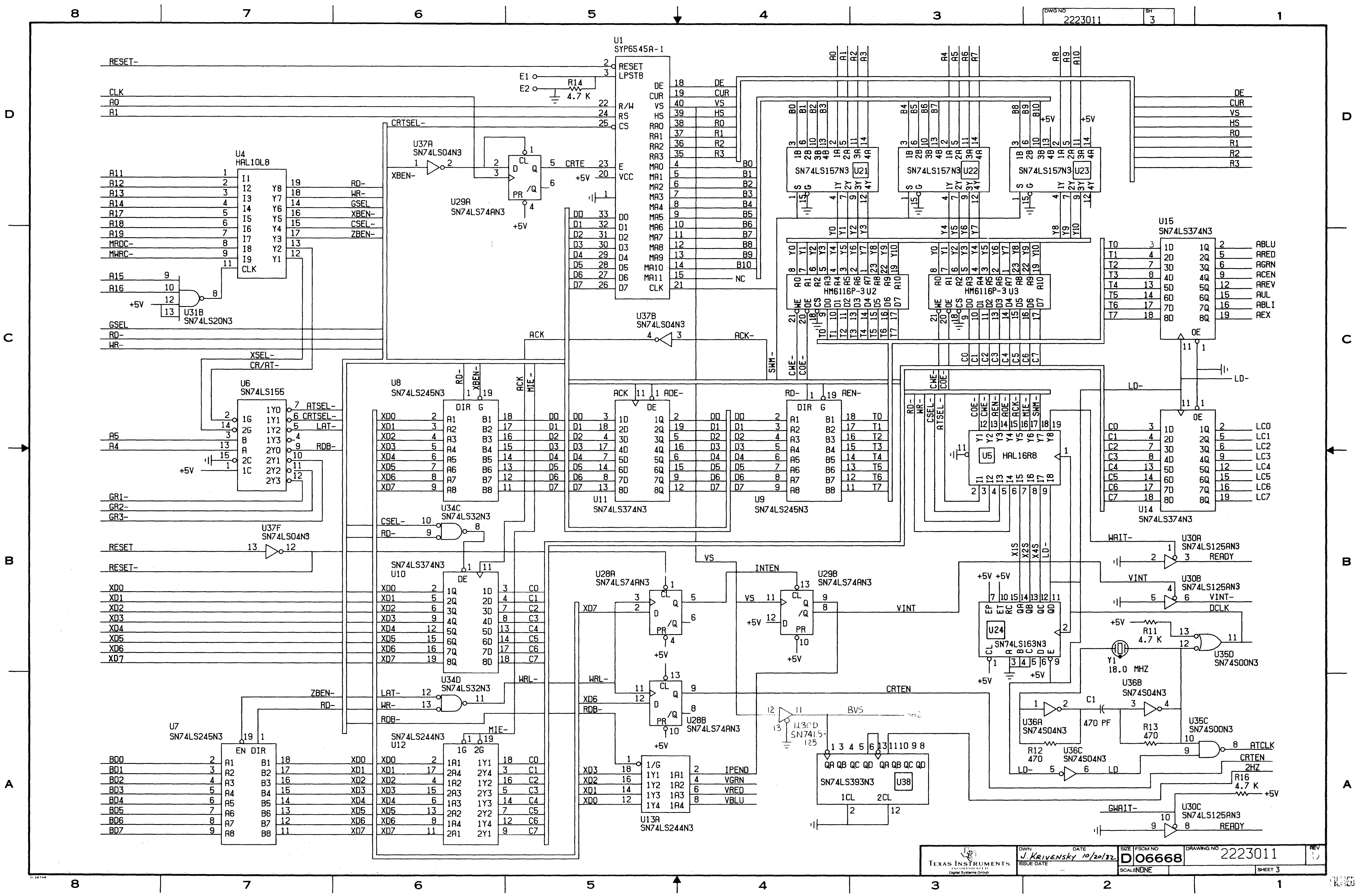
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U8
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SN74LS374N3
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SN74LS374N3
U12
SN74LS244N3
U13A
SN74LS244N3
U14
SN74LS374N3
U15
SN74LS374N3
HM6116P-3 U2
HM6116P-3 U3
SN74LS157N3 U21
SN74LS157N3 U22
SN74LS157N3 U23
U5 HAL16R8
U24 SN74LS163N3
SN74LS393N3 U38
U29A
SN74LS74AN3
U29B
SN74LS74AN3
U28A
SN74LS74AN3
U28B
SN74LS74AN3
U37A
SN74LS04N3
U37B
SN74LS04N3
U37F
SN74LS04N3
U31B
SN74LS20N3
U34C
SN74LS32N3
U34D
SN74LS32N3
U30A
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U30B
SN74LS125AN3
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SN74LS125AN3
U35C
SN74S00N3
U35D
SN74S00N3
U36A
SN74S04N3
U36B
SN74S04N3
U36C
SN74S04N3
Y1
18.0 MHZ
R14
4.7 K
R11
4.7 K
R16
4.7 K
R12
470
R13
470
C1
470 PF
RESET-
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A0
A1
CRTSEL-
XBEN-
GSEL
RD-
WR-
XSEL-
CR/AT-
RESET
ATSEL-
CRTSEL-
LAT-
RDB-
ZBEN-
ACK
ACK-
MIE-
ADE-
AEN-
VS
INTEN
VINT
CRTEN
IPEND
VGRN
VRED
VBLU
WAIT-
READY
VINT-
DCLK
ATCLK
2HZ
GWAIT-
LD-
DE
CUR
HS
R0
R1
R2
R3
ABLU
ARED
AGRN
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AREV
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ABLI
AEX
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LC3
LC4
LC5
LC6
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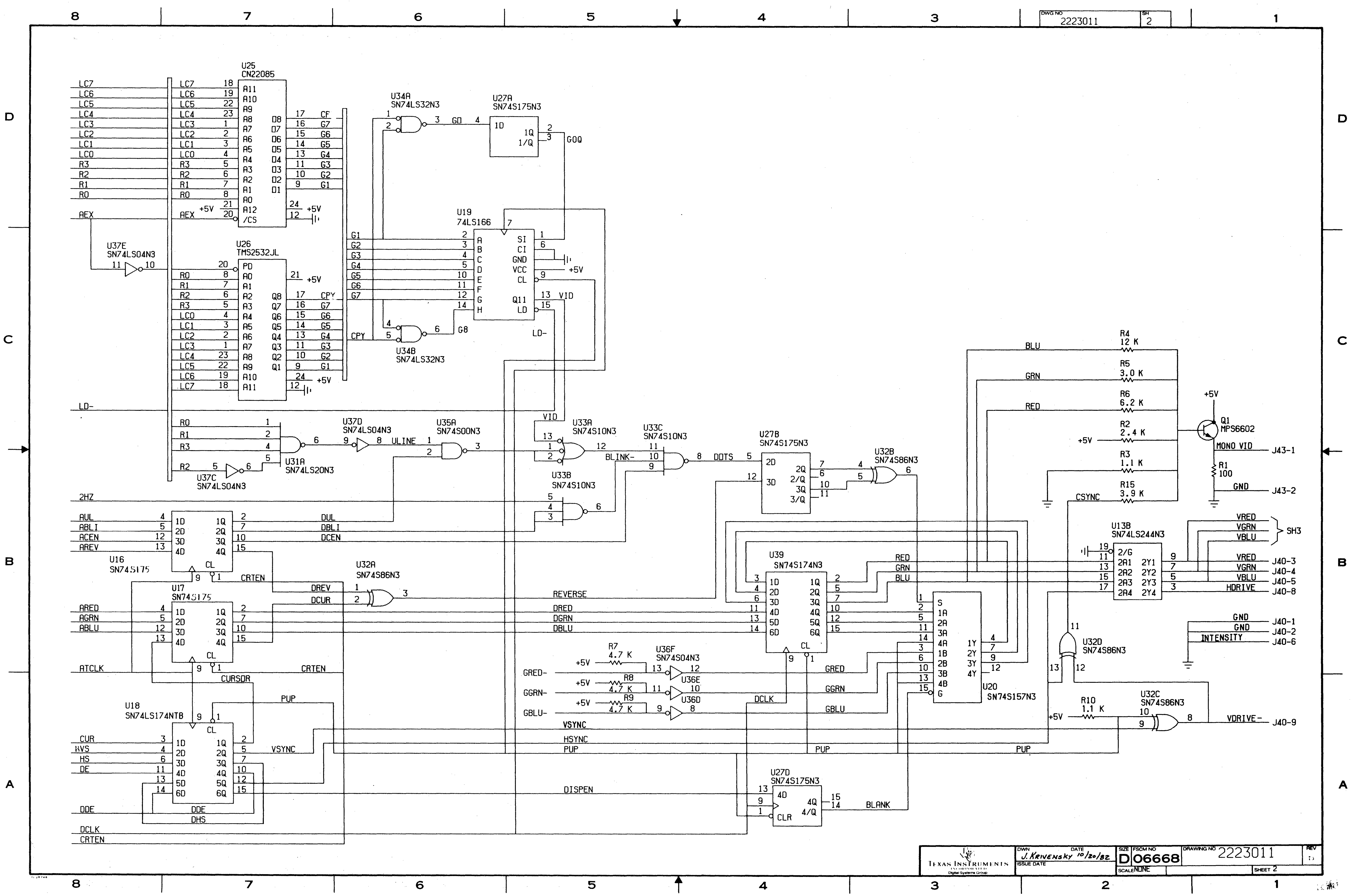
TEXAS INSTRUMENTS
J. KRIVENSKY 10/20/82
D 06668
2223011
SCALE NONE
SHEET 3



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SN74LS32N3
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U18
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U27D
SN74S175N3
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MPS6602
R4 12 K
R5 3.0 K
R6 6.2 K
R2 2.4 K
R3 1.1 K
R15 3.9 K
R1 100
R7 4.7 K
R8 4.7 K
R9 4.7 K
R10 1.1 K
LC7
LC6
LC5
LC4
LC3
LC2
LC1
LC0
R3
R2
R1
R0
AEX
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ACEN
AREV
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AGRN
ABLU
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HS
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DCLK
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DBLU
ULINE
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GOQ
VID
CPY
BLU
GRN
RED
CSYNC
GRED-
GGRN-
GBLU-
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GGRN
GBLU
BLANK
+5V
GND
MONO VID
J43-1
J43-2
VRED
VGRN
VBLU
SH3
HDRIVE
J40-3
J40-4
J40-5
J40-8
J40-1
J40-2
J40-6
INTENSITY
VDRIVE-
J40-9
TEXAS INSTRUMENTS
J. KRIVENSKY 10/20/82
D 06668
2223011
SCALE NONE
SHEET 2

Appendix F

Option Board Outline

The following illustrations give outline dimensions for a full-size board and a half-size board to allow the user to design and customize his own boards to fit the BUSINESS-PRO cabinet.

TO BE SUPPLIED

Appendix G

Switch and Jumper Settings

This appendix is a summary of the switch and jumper options available to the user in the BUSINESS-PRO.

TO BE SUPPLIED

Index

This index lists key topics of this manual and specifies where each topic appears, as follows:

* Sections -- Section references appear as Section n, where n represents the section number.

* Appendixes -- Appendix references appear as Appendix Y, where Y represents the appendix letter.

* Paragraphs -- Paragraph references appear as alphanumeric characters separated by decimal points. This first character refers to the section or appendix containing the paragraph, and any other numbers indicate the sequence of the paragraph within the section or appendix. For example:

  - 3.5.2 refers to Section 3, paragraph 5.2.

  - A.2 refers to Appendix A, paragraph 2.

* Figures -- Figure references appear as Fn-x or FY-x, where n represents the section and Y represents the appendix containing the figure; x represents the number of the figure within the section or appendix. For example, F2-7 refers to the seventh figure in Section 2.

* Tables -- Table references appear as Tn-x or TY-x, where n represents the section and Y represents the appendix containing the table; x represents the number of the table within the section or appendix. For example, TB-4 refers to the fourth table in Appendix B.

* See and See also references -- See and See also direct you to other entries in the index. For example:

Logical Unit Number . . . . See LUNO
Device . . . . . See also individual device names or numbers

Page numbers that correspond to these index references appear in the Table of Contents.

USER'S RESPONSE SHEET

Manual Title: ____

____

Manual Date: ______________________ Date of This Letter: ______________

User's Name: ______________________ Telephone: ______________

Company: ______________________ Office/Department: ______________

Street Address: ____

City/State/Zip Code: ____

Please list any discrepancy found in this manual by page, paragraph, figure, or table number in the following space. If there are any other suggestions that you wish to make, feel free to include them. Thank you.

Location in Manual **Comment/Suggestion**

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