TEXAS INSTRUMENTS

NuBus™

Interface Products

Data Book

1991

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NuBus™ Interface Products Data Book

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INTRODUCTION

This Data Book presents technical information on the TI NuBus™ support product line. Specifications and operational information is included for the following high-performance Advanced-CMOS devices:

1. SN74ACT2440 – NuBus™ Interface Controller
2. SN74ACT2441 – MCP† NuBus™ Interface Controller
3. SN74ALS2442 – NuBus™ Block Slave Address Generator
4. SN74BCT2420 – NuBus™ Address/Data Tranceiver and Registers
5. SN74BCT2423/24 – 16-Bit Latched Multiplexer/Demultiplexer Bus Transceivers
6. SN74BCT2425 – MCP† NuBus™ Address/Data Tranceivers and Registers.

In addition, this Data Book contains design specification data for all six devices previously listed. Three application reports are also included: *Support NuBus™ Block Slave Transfers Using Texas Instruments SN74ACT2440, SN74BCT2420, and SN74ALS2442*, *Designing Simple NuBus™ Slave-Only Applications Using Texas Instruments SN74ACT2440 and SN74BCT2420*, and *Memory Interleave/ Interface Applications* using Texas Instruments *SN74BCT2423 and SN74BCT2424*.

A section on the development of logic symbols to meet both ANSI/IEEE Std 91-1984 and IEC Publication 617-12 is included for the reader's better understanding.

The ESD Guidelines utilized by TI are discussed in another section for the reader's better understanding.

Package dimensions are given in the Mechanical Data section of the book in metric measurement (and parenthetically in inches).

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† Macintosh Coprocessor Platform
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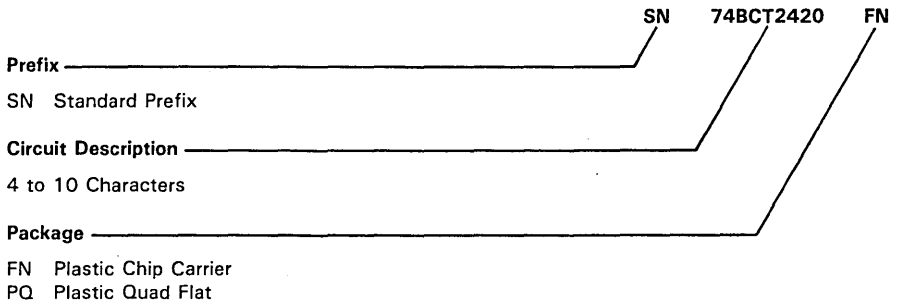
Factory orders for NuBus™ products described in this book should include a three-part type number as explained in the following example:



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INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

C_i **Input capacitance**
The internal capacitance at an input of the device.

C_o **Output capacitance**
The internal capacitance at an output of the device.

f_{max} **Maximum clock frequency**
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

I_{CC} **Supply current**
The current into† the V_{CC} supply terminal of an integrated circuit.

I_{CCH} **Supply current, outputs high**
The current into† the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the high level.

I_{CCL} **Supply current, outputs low**
The current into† the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the low level.

I_{IH} **High-level input current**
The current into† an input when a high-level voltage is applied to that input.

I_{IL} **Low-level input current**
The current into† an input when a low-level voltage is applied to that input.

I_{OH} **High-level output current**
The current into† an output with input conditions applied that, according to the product specification, will establish a high level at the output.

I_{OL} **Low-level output current**
The current into† an output with input conditions applied that, according to the product specification, will establish a low level at the output.

I_{OS} (I_O) **Short-circuit output current**
The current into† an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

†Current out of a terminal is given as a negative value.

I_{OZH} **Off-state (high-impedance-state) output current (of a three-state output) with high-level voltage applied**

The current flowing into† an output having three-state capability with input conditions established that, according to the production specification, will establish the high-impedance state at the output and with a high-level voltage applied to the output.

NOTE: This parameter is measured with other input conditions established that would cause the output to be at a low level if it were enabled.

I_{OZL} **Off-state (high-impedance-state) output current (of a three-state output) with low-level voltage applied**

The current flowing into† an output having three-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output and with a low-level voltage applied to the output.

NOTE: This parameter is measured with other input conditions established that would cause the output to be at a high level if it were enabled.

t_a **Access time**

The time interval between the application of a specified input pulse and the availability of valid signals at an output.

t_{dis} **Disable time (of a three-state output)**

The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state. (t_{dis} = t_{PHZ} or t_{PLZ}).

t_{en} **Enable time (of a three-state output)**

The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low). (t_{en} = t_{PZH} or t_{PZL}.)

t_f **Fall time**

The time interval between two reference points (90% and 10% unless otherwise specified) on a waveform that is changing from the defined high level to the defined low level.

t_h **Hold time**

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

t_{pd} **Propagation delay time**

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. (t_{pd} = t_{PHL} or t_{PLH}).

†Current out of a terminal is given as a negative value.

t_{PHL} **Propagation delay time, high-to-low level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{PHZ} **Disable time (of a three-state output) from high level**
The time interval between the specified reference points on the input and the output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

t_{PLH} **Propagation delay time, low-to-high-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PLZ} **Disable time (of a three-state output) from low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

t_{PZH} **Enable time (of a three-state output) to high level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

t_{PZL} **Enable time (of a three-state output) to low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

t_r **Rise time**
The time interval between two reference points (10% and 90% unless otherwise specified) on a waveform that is changing from the defined low level to the defined high level.

t_{su} **Setup time**
The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

t_t **Transition time (general)**
The time interval between two reference points (10% and 90% unless otherwise specified) on a waveform that is changing from the defined low level to the defined high level (rise time) or from the defined high level to the defined low level (fall time).

t_w **Pulse duration (width)**
The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

V_{IH} **High-level input voltage**
An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.
NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} **Low-level input voltage**
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.
NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{OH} **High-level output voltage**
The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output.

V_{OL} **Low-level output voltage**
The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output.

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New or revised data sheets in this book use letter symbols in accordance with standards recently adopted by JEDEC, the IEEE, and the IEC. Two basic forms are used. The first form is usually used in this book when intervals can easily be classified as access, cycle, disable, enable, hold, refresh, setup, transition, or valid times and for pulse durations. The second form can be used generally but in this book is used primarily for time intervals not easily classifiable. The second (unclassified) form will be described first. Since some manufacturers use this form for all time intervals, symbols in the unclassified form are given with the examples for most of the classified time intervals.

Unclassified time intervals

Generalized letter symbols can be used to identify almost any time interval without classifying it using traditional or contrived definitions. Symbols for unclassifed time intervals identify two signal events listed in from-to sequence using the format:

$$t_{AB\text{-}CD}$$

Subscripts A and C indicate the names of the signals for which changes of state or level or establishment of state or level constitute signal events assumed to occur first and last, respectively, that is, at the beginning and end of the time interval. Every effort is made to keep the A and C subscript length down to one letter, if possible (e.g., R for READ and W for WRITE).

Subscripts B and D indicate the direction of the transitions and/or the final states or levels of the signals represented by A and C, respectively. One or two of the following is used:

H = high or transition to high
L = low or transition to low
V = a valid steady-state level
X = unknown, changing, or "don't care" level
Z = high-impedance (off) state

The hyphen between the B and C subscripts is omitted when no confusion is likely to occur.

Classified time intervals (general comments, specific times follow)

Because of the information contained in the definitions, frequently the identification of one or both of the two signal events that begin and end the intervals can be significantly shortened compared to the unclassified forms. For example, it is not necessary to indicate in the symbol that an access time ends with valid data at the output. However, if both signals are named (e.g., in a hold time), the from-to sequence is maintained.

Access time

The time interval between the application of a specific input pulse and the availability of valid signals at an output.

Example symbology:

Classified	Unclassified	Description
$t_{a(A)}$	t_{AVQV}	Access time from address
$t_{a(S)}$, $t_{a(CS)}$	t_{SLQV}	Access time from chip select (low)

Cycle time

The time interval between the start and end of a cycle.

NOTE: The cycle time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval that must be allowed for the digital circuit to perform a specified function (e.g., read, write, etc.) correctly.

Example symbology:

Classifed	Unclassified	Description
$t_{c(R)}$, $t_{c(rd)}$	$t_{AVAV(R)}$	Read cycle time
$t_{c(W)}$	$t_{AVAV(W)}$	Write cycle time

Disable time (of a three-state output)

The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

Example symbology:

Classified	Unclassified	Description
$t_{dis(S)}$	t_{SHQZ}	Output disable time after chip select (high)
$t_{dis(W)}$	t_{WLQZ}	Output disable time after write enable (low)

These symbols supersede the older forms t_{PVZ} or t_{PXZ}.

Enable time (of a three-state output)

The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low).

Example symbology:

Classified	Unclassifed	Description
$t_{en(SL)}$	t_{SLQV}	Output enable time after chip select low

These symbols supersede the older form t_{PZV}.

Hold time

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

Example symbology:

Classified	Unclassified	Description
$t_{h(D)}$	t_{WHDX}	Data hold time (after write high)

NOTE: The from-to sequence in the order of subscripts in the unclassified form is maintained in the classified form. In the case of hold times, this causes the order to seem reversed from what would be suggested by the terms.

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Pulse duration (width)

The time interval between the specified reference points on the leading and trailing edges of the pulse waveform.

Example symbology:

Classified	Unclassified	Description
$t_{w(W)}$	tWLWH	Write pulse duration
$t_{w(R)}$	tRLRH	Read pulse duration

Setup time

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

Example symbology:

Classified	Unclassified	Description
$t_{su(D)}$	tDVWH	Data setup time (before write high)

Transition times (also called rise and fall times)

The time interval between two reference points (10% and 90% unless otherwise specified) on the same waveform that is changing from the defined low level to the defined high level (rise time) or from the defined high level to the defined low level (fall time).

Example symbology:

Classified	Unclassified	Description
t_t		Transition time (general)

Valid time

(a) General

The time interval during which a signal is (or should be) valid.

(b) Output data-valid time

The time interval in which output data continues to be valid following a change of input conditions that could cause the output data to change at the end of the interval.

Example symbology:

Classified	Unclassified	Description
$t_{v(A)}$	tAXQX	Output data valid time after change of address

This supersedes the older form t_{PVX}.

The following symbols are used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
↶	=	value/level is re-entered
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state-output
a . . h	=	the level of steady-state inputs at inputs A through H respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$	=	complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑
⎍	=	one high-level pulse
⎴	=	one low-level pulse
TOGGLE	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, ⎍ or ⎴, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

Shift registers provide a good example of the features of a function table. The function table of a shift register embodies all of the symbols used in most function tables. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

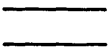
The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output Q_A, data entered at B will be at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D respectively, and the data previously at Q_D is no longer in the register. The entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both mode inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

The function table functional tests do not reflect all possible combinations or sequential modes.

TIMING DIAGRAM SYMBOL	MEANING: INPUT FORCING FUNCTIONS	MEANING: OUTPUT RESPONSE FUNCTIONS
	Must be steady high or low	Will be steady high or low
	High-to-low changes permitted	Will be changing from high to low some time during designated interval
	Low-to-high changes permitted	Will be changing from low to high sometime during designated interval
	Don't Care	State unknown or changing
	(Does not apply)	Centerline represents high-impedance (off) state.

The front page of the data sheet begins with a list of key features such as organization, interface, compatibility, operation, and technology. In addition, the top view of the device is shown with the pinout provided. Next, a general description of the device, system interface considerations, and elaboration on other device characteristics are presented. The next section is an explanation of the device's operation which includes the function of each pin (i.e., the relationship between each input/output and a given type of application).

Augmenting the descriptive text, there appears a logic symbol prepared in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12 and explained in Section 4 of this book. Following the symbol is usually a functional block diagram or a logic diagram. Usually, the next few pages contain the absolute maximum ratings (e.g., voltage supplies, input voltage, and temperature) applicable over the operating free-air temperature range. If the device is used outside of these values, it may be permanently destroyed or at least it would not function as intended. Next, are the recommended operating conditions, (e.g., supply voltages, input voltages, and operating temperature). These devices are specified to work reliably and to meet all data sheet parameters when operated in accordance with the recommended operating conditions and within the specified timing. If the device is operated outside of these limits (minimum/maximum), it is no longer specified to meet the data sheet parameters. Operation beyond the absolute maximum ratings can result in catastrophic failures.

The next section provides a table of electrical characteristics over full ranges of recommended operating conditions (e.g., input and output currents, output voltages, etc.). These are presented as minimum, typical, and maximum values. Typical values are representative of operation at an ambient temperature of $T_A = 25\,°C$ with all power supply voltages at nominal value.

The next few tables involve the device timing characteristics. The parameters are presented as minimum, typical (or nominal), and maximum. The switching characteristics over recommended supply voltage range are device performance characteristics inherent to device operation once the inputs are applied. These parameters are specified for the test conditions given. The timing requirements over recommended supply voltage range and operating free-air temperature indicate the device control requirements such as hold times, setup times, and transition times. These values are referenced to the relative positioning of signals on the timing diagrams that follow. The interrelationship of the timing requirements to the switching characteristics is illustrated in the parameter measurement information section.

At the end of a data sheet additional applications information may be provided such as how to use the device, graphs of electrical characteristics, or other data on electrical characteristics.

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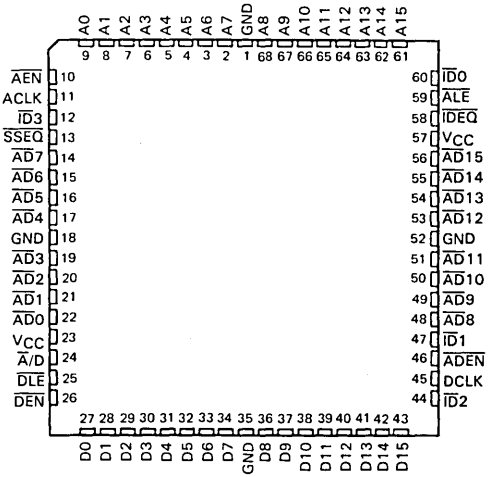
D3159, NOVEMBER 1988–REVISED JANUARY 1989

- **Designed for NuBus™ Interface Applications**
- **Conforms to ANSI/IEEE Std 1196-1987**
- **On-Chip Comparator Provides I/D Slot Identification**
- **Multiplexed Real-Time and Latched Address/Data**
- **Designed to Operate with SN74ACT2440 NuBus™ Controller**
- **BiCMOS Design Substantially Reduces Standby Current**
- **Dependable Texas Instruments Quality and Reliability**

FN PACKAGE
(TOP VIEW)



description

The 'BCT2420 consists of bus transceiver circuits, D-type flip-flops, latches, and control circuitry arranged for multiplexed transmission of address and data information in NuBus™ applications. An on-chip comparator has been included to detect when a NuBus™ transfer cycle is requesting the local board. The device conforms to ANSI/IEEE Std 1196-1987 and operates with Texas Instruments SN74ACT2440 NuBus™ Controller. In addition, the device is easily configured around ASIC or other PAL®-based controllers.

The 'BCT2420 was designed using Texas Instruments BiCMOS process, which features bipolar drive characteristics and greatly reduces the standby power of the device when disabled. This feature is especially valuable when the device is not performing a NuBus™ transaction.

The $\overline{AEN}$, $\overline{DEN}$ and $\overline{ADEN}$ inputs control the transceiver functions. Three 16-bit I/O ports, A15-A0, D15-D0, and $\overline{AD}15$-$\overline{AD}0$, provide for address and data transfer. When the NuBus™ performs a write cycle to the local board, address information is saved on the rising edge of ACLK. During the last portion of the NuBus™ write cycle, data information is saved on the rising edge of DCLK.

When the local board is performing a write to the NuBus™, address and data is multiplexed onto the NuBus™ via the $\overline{A}$/D line. Address and data can be latched by using the $\overline{ALE}$ and $\overline{DLE}$ input lines respectively.

The $\overline{IDEQ}$ output is used to signal that the local board is being requested by the NuBus™. This output is typically fed to the NuBus™ controller. $\overline{IDEQ}$ goes active (low) when $\overline{AD}15$-$\overline{AD}12$ are low and $\overline{AD}11$-$\overline{AD}8$ match $\overline{ID}3$-$\overline{ID}0$. $\overline{IDEQ}$ stays valid until the next address clock (ACLK) occurs. Internal 10-kΩ pull-up resistors are included on the $\overline{ID}3$-$\overline{ID}0$ inputs.

The $\overline{SSEQ}$ output is used to signal the local board that super-slot addresses are being requested. This output is active (low) whenever $\overline{AD}15$-$\overline{AD}12$ are equal to $\overline{ID}3$-$\overline{ID}0$, except when $\overline{ID}3$-$\overline{ID}0$ are all low.

In typical NuBus™ applications, two devices are required to provide the full 32-bit address/data path. Refer to the typical NuBus™ interface diagram on page 9 for additional information.

The SN74BCT2420 is characterized for operation from 0°C to 70°C.

NuBus is a trademark of Texas Instruments Incorporated.
PAL is a registered trademark of Monolithic Memories Inc.

FUNCTION TABLES

INPUTS						OUTPUTS
A15-A0	D15-D0	$\overline{ALE}$	$\overline{DLE}$	A/D	$\overline{ADEN}$	$\overline{AD15}$-$\overline{AD0}$
H	X	L	X	L	L	L
L	X	L	X	L	L	H
X	X	H	X	L	L	Q_O
X	H	X	L	H	L	L
X	L	X	L	H	L	H
X	X	X	H	H	L	Q_O
X	X	X	X	X	H	Z

INPUTS			OUTPUTS
$\overline{AD15}$-$\overline{AD0}$	ACLK, DCLK	$\overline{AEN}$, $\overline{DEN}$	A15-A0, D15-D0
H	↑	L	L
L	↑	L	H
X	L	L	Q_O
X	X	H	Z

$\overline{AD15}$-$\overline{AD12}$	$\overline{ID3}$-$\overline{ID0}$	$\overline{SSEQ}$
EQ $\overline{ID3}$-$\overline{ID0}$	NE 0	L
NE $\overline{ID3}$-$\overline{ID0}$	X	H
X	EQ 0	H

$\overline{AD15}$-$\overline{AD12}$	$\overline{AD11}$-$\overline{AD8}$	$\overline{IDEQ}$
EQ 0	EQ $\overline{ID3}$-$\overline{ID0}$	L
X	NE $\overline{ID3}$-$\overline{ID0}$	H
NE 0	X	H

NOTE: Symbol 'Q_O' denotes previous logic state preserved.
Symbol 'Z' denotes high-impedance state.

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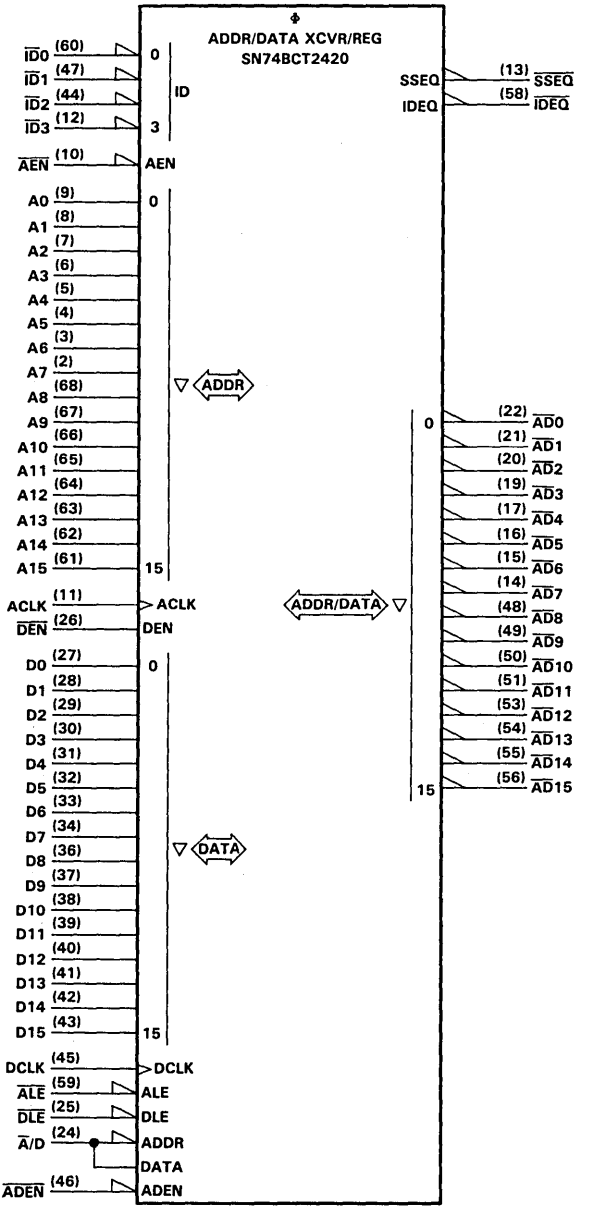
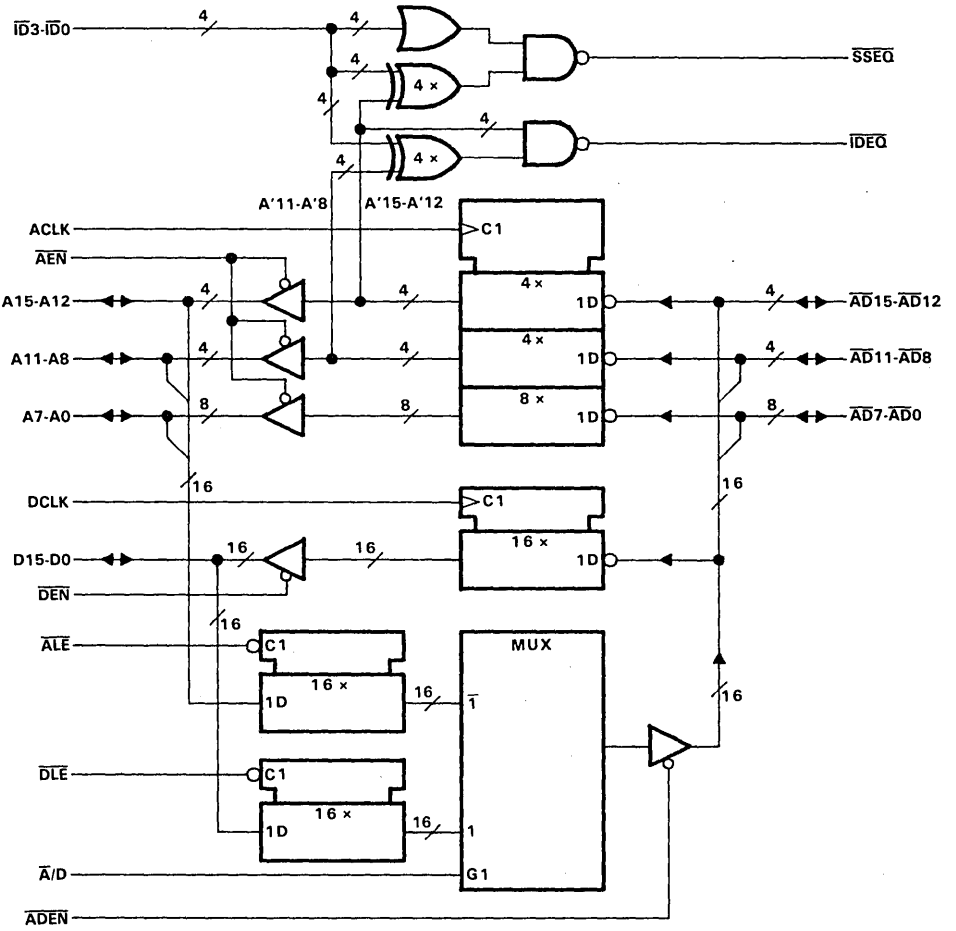
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984.

logic diagram



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TERMINAL FUNCTIONS

PIN NAME	DESCRIPTION
A15-A0	Address Bus. This 16-bit I/O port is connected to the local board's address bus. When information is transferred between this port and the NuBus™ port ($\overline{AD}$15-$\overline{AD}$0), the data is inverted to conform to NuBus™ specifications.
ACLK	Address Clock. This input saves the address portion of NuBus™ read or write cycles. Data present at the $\overline{AD}$15-$\overline{AD}$0 inputs is clocked into the address register on the low-to-high transition of ACLK.
$\overline{A}$/D	Address/Data Select. This input controls the address/data multiplexer. When $\overline{A}$/D is driven low, the local address port, A15-A0, is selected as input to the $\overline{AD}$15-$\overline{AD}$0 outputs. When $\overline{A}$/D is taken high, the local data port, D15-D0, is selected as input to the $\overline{AD}$15-$\overline{AD}$0 outputs.
$\overline{AD}$15-$\overline{AD}$0	Address/Data Port. This 16-bit active-low I/O port directly interfaces to the NuBus™ address/data lines. These lines are multiplexed to carry address information at the beginning of a NuBus™ cycle and data information later in the cycle.
$\overline{ADEN}$	Address/Data Output Enable. This active-low input enables the $\overline{AD}$15-$\overline{AD}$0 outputs. When $\overline{ADEN}$ is taken high, the $\overline{AD}$15-$\overline{AD}$0 outputs are in the high-impedance state, allowing input from the NuBus™.
$\overline{AEN}$	Address Enable. This active-low input enables the local address outputs, A15-A0, to place data onto the local board. When $\overline{AEN}$ is taken high, the A15-A0 outputs are in the high-impedance state, allowing input from the local address bus.
$\overline{ALE}$	Address Latch Enable. This active-low input controls the latch that holds the address received from the local address bus, A15-A0. When $\overline{ALE}$ is low, the latch is transparent. When $\overline{ALE}$ is taken high, the address present at the A15-A0 inputs is latched and remains latched while $\overline{ALE}$ is held high.
D15-D0	Data Bus. This 16-bit I/O port is connected to the local board's data bus. When information is transferred between this port and the NuBus™ port ($\overline{AD}$15-$\overline{AD}$0), the data is inverted to conform to NuBus™ specifications.
DCLK	Data Clock. This input saves the data portion of NuBus™ write cycles. Data present at the $\overline{AD}$15-$\overline{AD}$0 inputs is clocked into the data register on the low-to-high transition of DCLK.
$\overline{DEN}$	Data Enable. This active-low input enables the local data port outputs, D15-D0, to place data onto the local board. When $\overline{DEN}$ is taken high, the D15-D0 outputs are in the high-impedance state, allowing input from the local board.
$\overline{DLE}$	Data Latch Enable. This active-low input controls the latch that holds the data received from the local data bus, D15-D0. When $\overline{DLE}$ is low, the latch is transparent. When $\overline{DLE}$ is taken high, the data present at the D15-D0 inputs is latched and remains latched while $\overline{DLE}$ is held high.
$\overline{ID}$3-$\overline{ID}$0	Card-Slot Identification. These four inputs accept binary-coded location information for each NuBus™ slot position on the backplane. These four lines are typically hard-wired logic levels unique to each NuBus™ slot connector. For convenient implementation, the inputs have internal 10-kΩ pull-up resistors that ensure the logic high level when the inputs are left open-circuited. The internal comparator uses these inputs to identify when the local hardware card is being accessed.
$\overline{IDEQ}$	Identification Equal. This active-low output is used to signal that the local board is being accessed by the NuBus™. $\overline{IDEQ}$ goes low whenever $\overline{AD}$15-$\overline{AD}$12 are low and $\overline{AD}$11-$\overline{AD}$8 match $\overline{ID}$3-$\overline{ID}$0. Since the internal comparator uses data from the address register, the address register must be clocked before the local board samples $\overline{IDEQ}$. $\overline{IDEQ}$ is valid for the entire NuBus™ cycle after ACLK.
$\overline{SSEQ}$	Super-Slot Equal. This active-low output is used to signal the local board that super-slot addresses are being requested in the super-slot mode. $\overline{SSEQ}$ goes low when $\overline{AD}$15-$\overline{AD}$12 match $\overline{ID}$3-$\overline{ID}$0 and $\overline{ID}$3-$\overline{ID}$0 are not all low. Since the internal comparator uses data from the address register, the address register must be clocked before the local board samples $\overline{SSEQ}$. $\overline{SSEQ}$ is valid for the entire NuBus™ cycle after ACLK.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (all inputs and I/O ports) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Ax, Dx, $\overline{AD}$x outputs			−15	mA
		$\overline{SSEQ}$, $\overline{IDEQ}$ outputs			−2.6	
I_{OL}	Low-level output current	Ax, Dx, $\overline{AD}$x outputs			24	mA
		$\overline{SSEQ}$, $\overline{IDEQ}$ outputs			16	
f_{clock}	Clock frequency		0		40	MHz
t_w	Pulse duration	ACLK, DCLK high	12.5			ns
		ACLK, DCLK low	12.5			
		$\overline{ALE}$, $\overline{DLE}$ low	12.5			
t_{su}	Setup time	$\overline{AD}$x before ACLK↑, DCLK↑	5			ns
		Ax before $\overline{ALE}$↑	5			
		Dx before $\overline{DLE}$↑	5			
t_h	Hold time	$\overline{AD}$x after ACLK↑, DCLK↑	2			ns
		Ax after $\overline{ALE}$↑	2			
		Dx after $\overline{DLE}$↑	2			
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA			−1.2	V
V_{OH}	Ax, Dx, $\overline{ADx}$	V_{CC} = 4.5 V to 5.5 V, I_{OH} = −400 μA	V_{CC}−1.5			V
		V_{CC} = 4.5 V, I_{OH} = −3 mA	2.8	3.6		
		V_{CC} = 4.5 V, I_{OH} = −15 mA	2			
	$\overline{SSEQ}$, $\overline{IDEQ}$	V_{CC} = 4.5 V to 5.5 V, IOH = −400 μA	V_{CC}−2			
		V_{CC} = 4.5 V, I_{OH} = −2.6 mA	2.4	3.2		
V_{OL}	Ax, Dx, $\overline{ADx}$	V_{CC} = 4.5 V, I_{OL} = 12 mA		0.25	0.4	V
		V_{CC} = 4.5 V, I_{OL} = 24 mA		0.35	0.5	
	$\overline{SSEQ}$, $\overline{IDEQ}$	V_{CC} = 4.5 V, I_{OL} = 8 mA		0.25	0.4	
		V_{CC} = 4.5 V, I_{OL} = 16 mA		0.35	0.5	
I_I		V_{CC} = 5.5 V, V_I = 5.5 V			100	μA
I_{IH}‡	$\overline{AEN}$, $\overline{DEN}$, $\overline{ADEN}$	V_{CC} = 5.5 V, V_I = 2.7 V			20	μA
	$\overline{ID3}$-$\overline{ID0}$				−400	
	All other inputs				−100	
I_{IL}‡	$\overline{ID3}$-$\overline{ID0}$	V_{CC} = 5.5 V, V_I = 0.4 V			−750	μA
	All other inputs				−200	
I_{OS}§		V_{CC} = 5.5 V, V_O = 0 V	−60		−225	mA
I_{CC}	Enabled	V_{CC} = 5.5 V, V_{IL} = 0.5 V, V_{IH} = 3 V, Outputs open		110	160	mA
	Disabled			30	40	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		LOAD CONDITIONS			MIN	TYP†	MAX	UNIT
		R1, R2, and R_L	C_L	LOAD CIRCUIT				
f_{max}	Maximum clock frequency				40			MHz
t_{pd}	Propagation time, ACLK↑ to Ax ($\overline{AEN}$ = L)	R1 = 500 Ω, R2 = 500 Ω	50 pF	S1 Open‡		9	16	ns
t_{pd}	Propagation time, DCLK↑ to Dx ($\overline{DEN}$ = L)	R1 = 500 Ω, R2 = 500 Ω	50 pF	S1 Open‡		9	16	ns
t_{pd}	Propagation time, Ax to $\overline{AD}$x ($\overline{ALE}$ = L, $\overline{A}$/D = L)	R1 = 270 Ω, R2 = 470 Ω	300 pF	S1 Closed§		10	18	ns
t_{pd}	Propagation time, Dx to $\overline{AD}$x ($\overline{DLE}$ = L, $\overline{A}$/D = H)	R1 = 270 Ω, R2 = 470 Ω	300 pF	S1 Closed§		11	18	ns
t_{pd}	Propagation time, $\overline{ALE}$ low to $\overline{AD}$x (A/D = L)	R1 = 270 Ω, R2 = 470 Ω	300 pF	S1 Closed§		10	18	ns
t_{pd}	Propagation time, $\overline{DLE}$ low to $\overline{AD}$x ($\overline{A}$/D = H)	R1 = 270 Ω, R2 = 470 Ω	300 pF	S1 Closed§		11	18	ns
t_{pd}	Propagation time, $\overline{A}$/D to $\overline{AD}$x	R1 = 270 Ω, R2 = 470 Ω	300 pF	S1 Closed§		10	16	ns
t_{pd}	Propagation time, ACLK to $\overline{IDEQ}$	R_L = 500 Ω	50 pF	¶		12	20	ns
t_{pd}	Propagation time, ACLK to $\overline{SSEQ}$	R_L = 500 Ω	50 pF	¶		12	18	ns
t_{pd}	Propagation time, $\overline{ID}$x to $\overline{IDEQ}$	R_L = 500 Ω	50 pF	¶		12	22	ns
t_{pd}	Propagation time, $\overline{ID}$x to $\overline{SSEQ}$	R_L = 500 Ω	50 pF	¶		12	22	ns
t_{en}	Enable time, $\overline{AEN}$ to Ax	R1 = 500 Ω, R2 = 500 Ω	50 pF	‡		10	16	ns
t_{en}	Enable time, $\overline{DEN}$ to Dx	R1 = 500 Ω, R2 = 500 Ω	50 pF	‡		10	16	ns
t_{en}	Enable time, $\overline{ADEN}$ to $\overline{AD}$x	R1 = 270 Ω, R2 = 470 Ω	300 pF	§		10	18	ns
t_{dis}	Disable time, $\overline{AEN}$ to Ax	R1 = 500 Ω, R2 = 500 Ω	50 pF	‡		6	10	ns
t_{dis}	Disable time, $\overline{DEN}$ to Dx	R1 = 500 Ω, R2 = 500 Ω	50 pF	‡		6	10	ns
t_{dis}	Disable time, $\overline{ADEN}$ to $\overline{AD}$x	R1 = 270 Ω, R2 = 470 Ω	50 pF	§		6	10	ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡See Parameter Measurement Information for load circuit (three-state outputs, A15-A0, D15-D0) and voltage waveforms.
§See Parameter Measurement Information for load circuit (NuBus™ Interface, $\overline{AD}$15-$\overline{AD}$0) and voltage waveforms.
¶See Parameter Measurement Information for load circuit (bi-state totem-pole outputs, $\overline{SSEQ}$, $\overline{IDEQ}$) and voltage waveforms.

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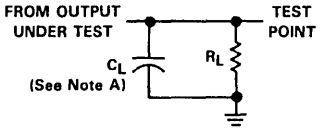
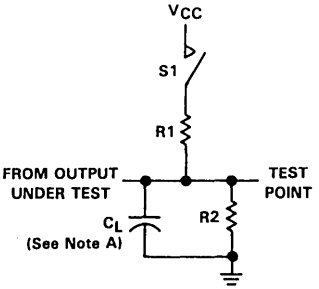
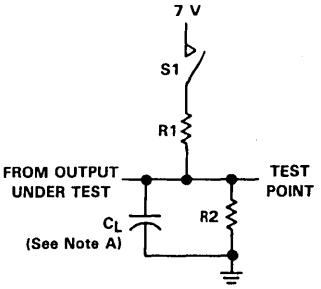
PARAMETER MEASUREMENT INFORMATION



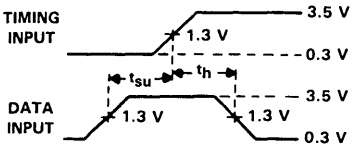
LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS
$\overline{SSEQ}$, $\overline{IDEQ}$



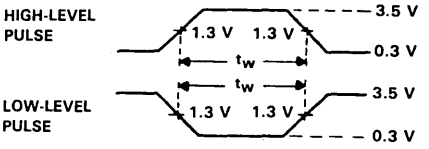
LOAD CIRCUIT FOR
NuBus™ INTERFACE
$\overline{AD}15 - \overline{AD}0$



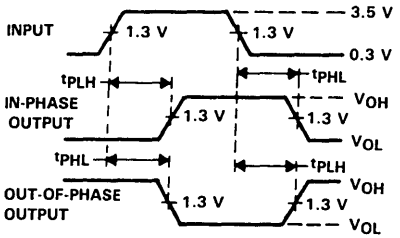
LOAD CIRCUIT FOR
THREE-STATE OUTPUTS
A15 – A0, D15 – D0



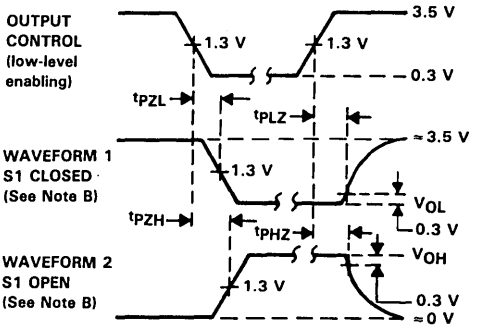
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal condition such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%
D. The outputs are measured one at a time with one transition per measurement.

FIGURE 1

APPLICATION INFORMATION

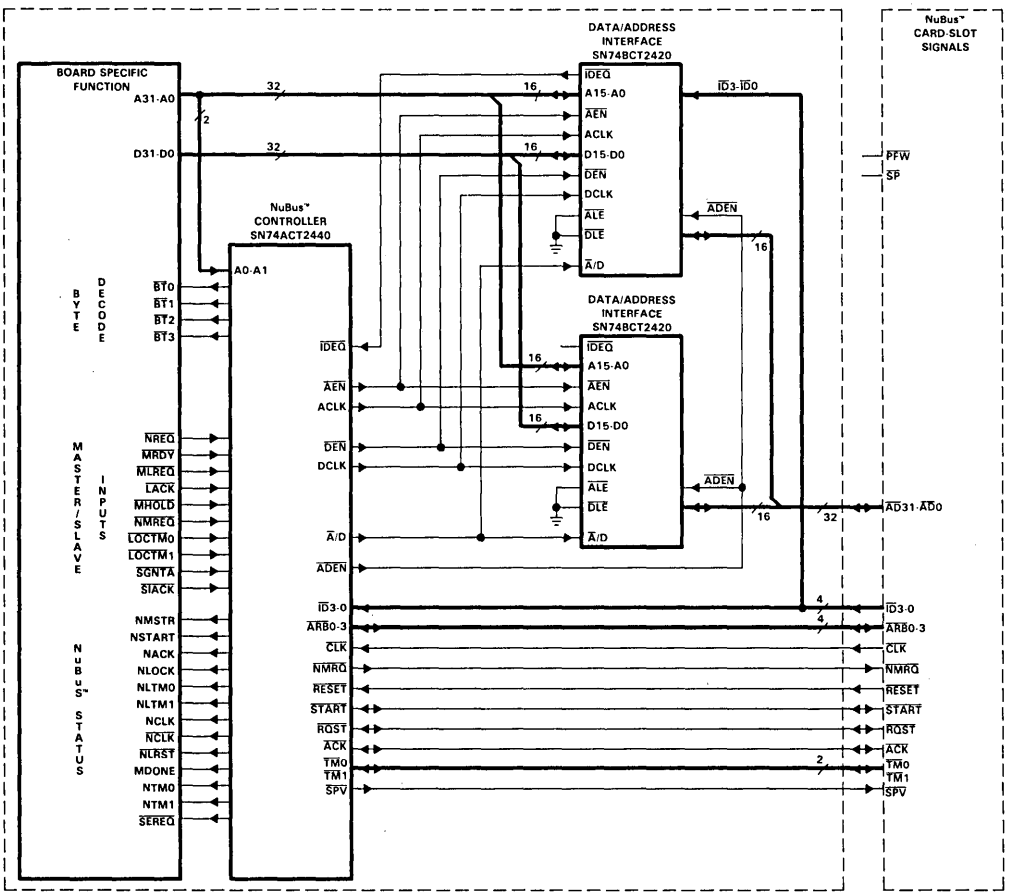


FIGURE 2. TYPICAL NuBus™ INTERFACE

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D3305, JULY 1989–REVISED OCTOBER 1989

- **Multiplexed Real-Time and Latched Data**
- **Byte Control for Byte-Write Applications**
- **Useful in NuBus™ Interface Applications**
- **Useful in Memory Interleave Applications**
- **BiCMOS Design Substantially Reduces Standby Current**
- **Dependable Texas Instruments Quality and Reliability**

description

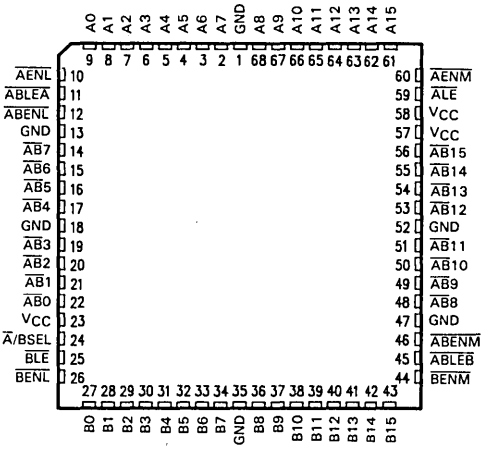
The 'BCT2423 and 'BCT2424 are general-purpose 16-bit bidirectional transceivers with data storage latches and byte control circuitry arranged for use in applications where two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing of address and data information in microprocessor- or bus-interface applications. These devices are also useful in memory-interleaving applications. The 'BCT2423 and 'BCT2424 offer inverted and noninverted data paths, respectively.

The 'BCT2423 and 'BCT2424 were designed using Texas Instruments BiCMOS process, which features bipolar drive characteristics, but also greatly reduces the standby power of the device when disabled. This is valuable when the device is not performing an address or data transfer.

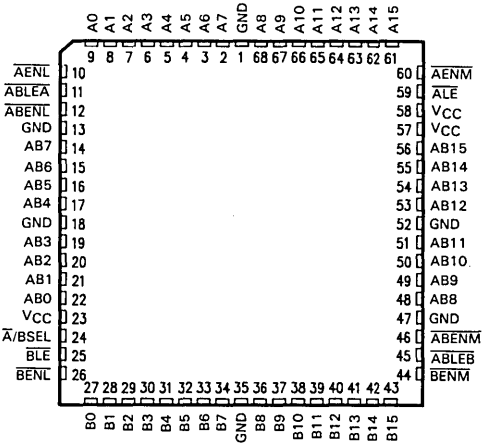
Three 16-bit I/O ports, A15-A0, B15-B0, and AB15-AB0 are available for address and/or data transfer. The $\overline{\text{AENM}}$, $\overline{\text{AENL}}$, $\overline{\text{BENM}}$, $\overline{\text{BENL}}$, $\overline{\text{ABENM}}$, and $\overline{\text{ABENL}}$ inputs control the bus transceiver functions. These control signals also allow byte-control of the most significant byte and least significant byte for each bus.

Address and/or data information can be stored using the internal storage latches. The $\overline{\text{ALE}}$, $\overline{\text{BLE}}$, $\overline{\text{ABLEA}}$, and $\overline{\text{ABLEB}}$ inputs are active low, and are used to control data storage. When the latch enable input is low, the latch is transparent. When the latch enable input goes high, the data present at the inputs is latched, and remains latched until the latch enable input is returned low.

SN74BCT2423 . . . FN PACKAGE
(TOP VIEW)



SN74BCT2424 . . . FN PACKAGE
(TOP VIEW)



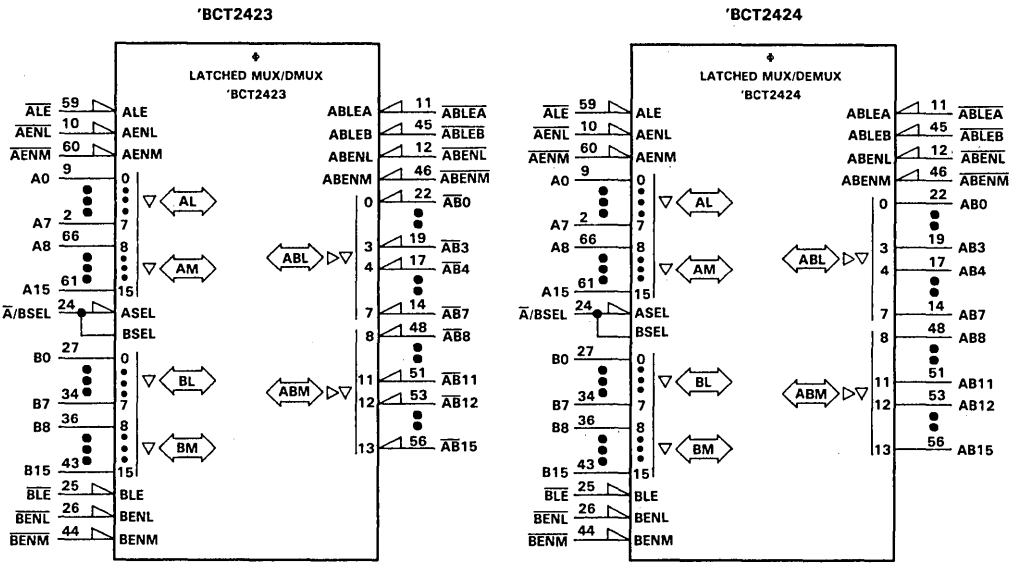
NuBus is a trademark of Texas Instruments Incorporated.

description (continued)

Data on the 'A' bus and 'B' bus are multiplexed onto the 'AB' bus via the $\overline{A}$/BSEL control line. When $\overline{A}$/BSEL is low, A15-A0 is mapped to the AB15-AB0 outputs. When $\overline{A}$/BSEL is high, B15-B0 is mapped to the AB15-AB0 outputs.

The SN74BCT2423 and SN74BCT2424 are characterized for operation from 0°C to 70°C.

logic symbols†



†These logic symbols are in accordance with ANSI/IEEE Std 91-1984.

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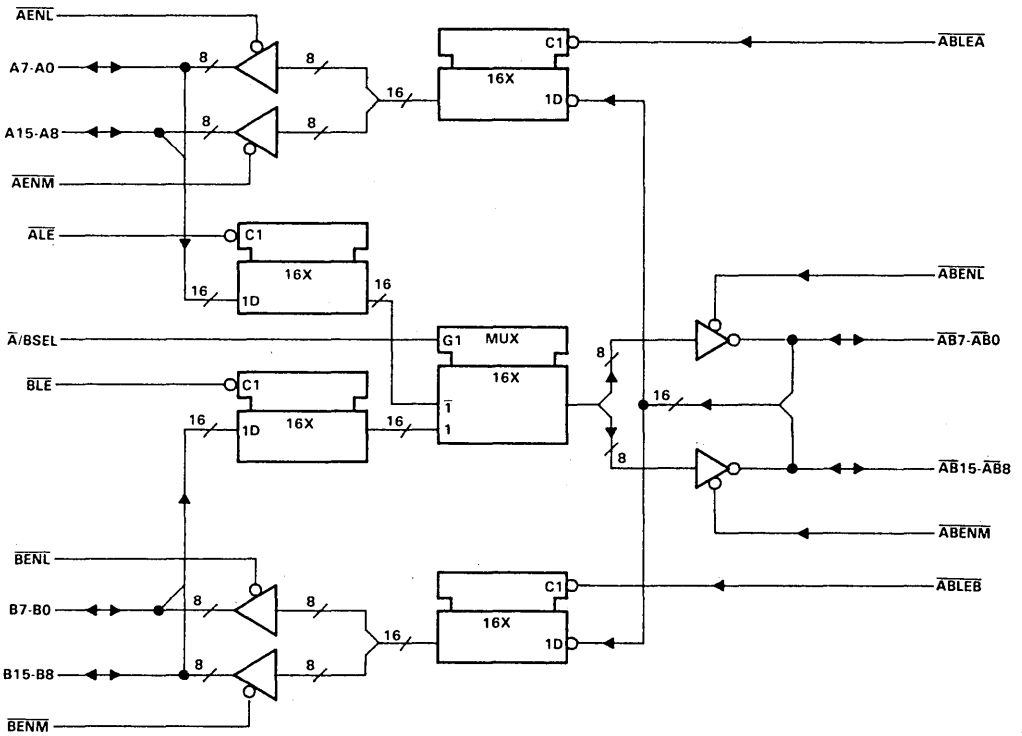
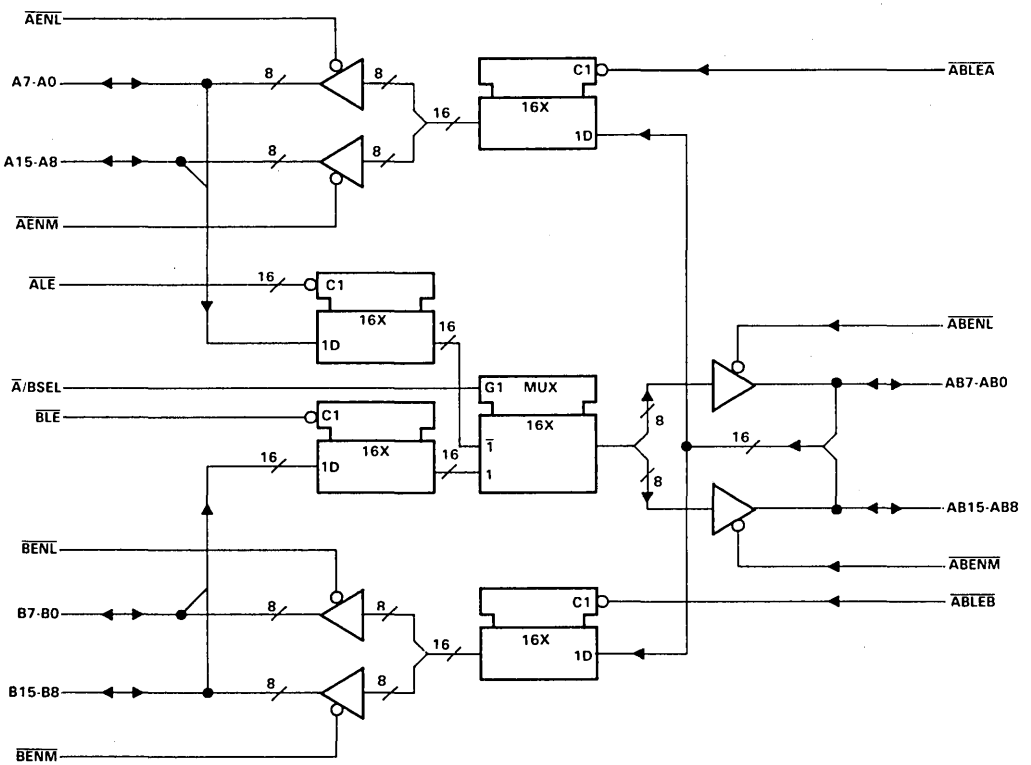
logic diagram (positive logic)



logic diagram (positive logic)



TEXAS INSTRUMENTS
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TERMINAL FUNCTIONS

PIN NAME	DESCRIPTION
A15-A0	A Bus. This 16-bit I/O port allows for transmission of data and/or address information to or from the AB bus. Information transfer between the A bus and the AB bus is inverting for the 'BCT2423 and noninverting for the 'BCT2424.
$\overline{AB}15$-$\overline{AB}0$ ('BCT2423) AB15-AB0 ('BCT2424)	AB Bus. This 16-bit I/O port allows for multiplexed transmission of data and/or address information to or from the A and B buses. Information transfer between the A, B and AB buses is inverting for the 'BCT2423 and noninverting for the 'BCT2424.
$\overline{ABENL}$	AB Bus Output Enable, Least Significant Byte. This active-low input is used to enable the AB7-AB0 outputs. When this input is high, the AB7-AB0 outputs are in the high-impedance state allowing for data input.
$\overline{ABENM}$	AB Bus Output Enable, Most Significant Byte. This active-low input is used to enable the AB15-AB8 outputs. When this input is high, the AB15-AB8 outputs are in the high-impedance state allowing for data input.
$\overline{ABLEA}$	AB Bus Latch Enable to A Bus. This active-low input is used to control the latch that holds data received from the AB bus (AB15-AB0) to be transferred to the A bus (A15-A0). When $\overline{ABLEA}$ is low, the latch is transparent. When $\overline{ABLEA}$ transitions to the high level, the data present at the AB15-AB0 inputs is latched, and remains latched while $\overline{ABLEA}$ is high.
$\overline{ABLEB}$	AB Bus Latch Enable to B Bus. This active-low input is used to control the latch that holds data received from the AB bus (AB15-AB0) to be transferred to the B bus (B15-B0). When $\overline{ABLEB}$ is low, the latch is transparent. When $\overline{ABLEB}$ transitions to the high level, the data present at the AB15-AB0 inputs is latched, and remains latched while $\overline{ABLEB}$ is high.
$\overline{A}$/BSEL	A/B Select Control. This input controls the A/B multiplexer. When the input is low, A15-A0 is selected as input to the AB15-AB0 outputs. When the input is high, B15-B0 is selected as input to the AB15-AB0 outputs.
$\overline{AENL}$	A Bus Output Enable, Least Significant Byte. This active-low input is used to enable the A7-A0 outputs. When this input is high, the A7-A0 outputs are in the high-impedance state allowing for data input.
$\overline{AENM}$	A Bus Output Enable, Most Significant Byte. This active-low input is used to enable the A15-A8 outputs. When this input is high, the A15-A8 outputs are in the high-impedance state allowing for data input.
$\overline{ALE}$	A Bus Latch Enable. This active-low input is used to control the latch that holds data received from the A bus (A15-A0). When $\overline{ALE}$ is low, the latch is transparent. When $\overline{ALE}$ transitions to the high level, the data present at the A15-A0 inputs is latched and remains latched while $\overline{ALE}$ is high.
B15-B0	B Bus. This 16-bit I/O port allows for transmission of data and/or address information to or from the AB bus. Information transfer between the B bus and the AB bus is inverting for the 'BCT2423 and noninverting for the 'BCT2424.
$\overline{BENL}$	B Bus Output Enable, Least Significant Byte. This active-low input is used to enable the B7-B0 outputs. When this input is high, B7-B0 outputs are in the high-impedance state allowing for data input.
$\overline{BENM}$	B Bus Output Enable, Most Significant Byte. This active-low input is used to enable the B15-B8 outputs. When this input is high, the B15-B8 outputs are in the high-impedance state allowing for data input.
$\overline{BLE}$	B Bus Latch Enable. This active-low input is used to control the latch that holds data received from the B bus (B15-B0). When $\overline{BLE}$ is low, the latch is transparent. When $\overline{BLE}$ transitions to the high level, the data present at the B15-B0 inputs is latched and remains latched while $\overline{BLE}$ is high.

FUNCTION TABLES

DIRECTION A OR B TO AB										
INPUTS							OUTPUTS			
							'BCT2423		'BCT2424	
Ax	Bx	$\overline{ALE}$	$\overline{BLE}$	A/BSEL	$\overline{ABENM}$	$\overline{ABENL}$	$\overline{AB}$15-8	$\overline{AB}$7-0	AB15-8	AB7-0
H	X	L	X	L	L	L	L		H	
L	X	L	X	L	L	L	H		L	
X	X	H	X	L	L	L	$\overline{AB}_0$		AB_0	
X	H	X	L	H	L	L	L		H	
X	L	X	L	H	L	L	H		L	
X	X	X	H	H	L	L	$\overline{AB}_0$		AB_0	
X	X	X	X	X	L	L	Active	Active	Active	Active
X	X	X	X	X	L	H	Active	Z	Active	Z
X	X	X	X	X	H	L	Z	Active	Z	Active
X	X	X	X	X	H	H	Z	Z	Z	Z

DIRECTION AB TO A OR B								
INPUTS					OUTPUTS			
$\overline{ABx}$			$\overline{AENL}$†	$\overline{BENL}$†	'BCT2423		'BCT2424	
ABx	$\overline{ABLEA}$	$\overline{ABLEB}$	$\overline{AENM}$†	$\overline{BENM}$†	Ax	Bx	Ax	Bx
H	L	L	L	L	L	L	H	H
L	L	L	L	L	H	H	L	L
H	L	H	L	L	L	B_0	H	B_0
L	L	H	L	L	H	B_0	L	B_0
H	H	L	L	L	A_0	L	A_0	H
L	H	L	L	L	A_0	H	A_0	L
X	H	H	L	L	A_0	B_0	A_0	B_0
X	X	X	L	L	Active	Active	Active	Active
X	X	X	L	H	Active	Z	Active	Z
X	X	X	H	L	Z	Active	Z	Active
X	X	X	H	H	Z	Z	Z	Z

H = high level, L = low level, X = irrelevant, Z = high impedence,
A_0, B_0, AB_0, $\overline{AB}_0$ = no change since the controlling latch enable went high
†The least significant bytes (A7-A0 and B7-B0) and the most significant bytes (A15-A8 and B15-B8) can be independently enabled and disabled, as was illustrated for the $\overline{AB}$ and AB bytes in the upper function table.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (all inputs and I/O ports) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

PARAMETER			SN74BCT2423			SN74BCT2424			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	Ax, Bx outputs			−15			−15	mA
		$\overline{AB}$x or AB$\overline{x}$ outputs			−15			−15	
I_{OL}	Low-level output current	Ax, Bx outputs			24			24	mA
		$\overline{AB}$x or AB$\overline{x}$ outputs			48			48	
t_w	Pulse duration	$\overline{ABLEA}$, $\overline{ABLEB}$ high or low	12.5			12.5			ns
		$\overline{ALE}$, $\overline{BLE}$ high or low	12.5			12.5			
t_{su}	Setup time	Data before $\overline{xLEx}$ ↑	10			10			ns
t_h	Hold time	Data after $\overline{xLEx}$ ↑	2			2			ns
T_A	Operating free-air temperature		0		70	0		70	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		SN74BCT2423			SN74BCT2424			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −400 μA	V_{CC}−1.5			V_{CC}−1.5			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.8	3.6		2.8	3.6		
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2			2			
V_{OL}	Ax, Bx outputs	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5		0.35	0.5	
	ABx, ABx outputs	V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.5		0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V			100			100	μA
I_{IH}§		V_{CC} = 5.5 V,	V_I = 2.7 V	−100		20	−100		20	μA
I_{IL}§		V_{CC} = 5.5 V,	V_I = 0.4 V			−200			−200	μA
I_O¶		V_{CC} = 5.5 V,	V_O = 0 V	−60		−225	−60		−225	mA
I_{CC}	Enabled	V_{CC} = 5.5 V,	V_{IL} = 0.5 V,			190			190	mA
	Disabled	V_{IH} = 3 V,	Outputs open			50			50	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§For I/O ports, the parameter I_{IH} and I_{IL} include the offstate output current.
¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

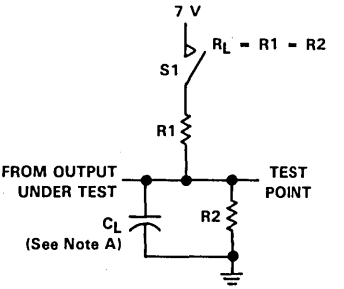
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS†	SN74BCT2423			SN74BCT2424			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	$\overline{AB}$x, ABx	Ax	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_1 = 500 Ω, R_2 = 500 Ω, T_A = MIN to MAX		10	18		10	18	ns
t_{pd}	$\overline{AB}$x, ABx	Bx			10	18		10	18	ns
t_{pd}	Ax	$\overline{AB}$x, ABx			10	18		10	18	ns
t_{pd}	Bx	$\overline{AB}$x, ABx			10	18		10	18	ns
t_{pd}	$\overline{ALE}$ ↓	$\overline{AB}$x, ABx			10	18		10	18	ns
t_{pd}	$\overline{BLE}$, ↓	$\overline{AB}$x, ABx			10	18		10	18	ns
t_{pd}	$\overline{ABLEA}$ ↓	Ax			10	18		10	18	ns
t_{pd}	$\overline{ABLEB}$ ↓	Bx			10	18		10	18	ns
t_{pd}	ABSEL	$\overline{AB}$x, ABx			10	18		8	15	ns
t_{en}	$\overline{AENM}$, $\overline{AENL}$	Ax			10	18		10	18	ns
t_{en}	$\overline{BENM}$, $\overline{BENL}$	Bx			10	18		10	18	ns
t_{en}	$\overline{ABENM}$, $\overline{ABENL}$	$\overline{AB}$x, ABx			10	18		10	18	ns
t_{dis}	$\overline{AENM}$, $\overline{AENL}$	Ax			5	10		5	10	ns
t_{dis}	$\overline{BENM}$, $\overline{BENL}$	Bx			5	10		5	10	ns
t_{dis}	$\overline{ABENM}$, $\overline{ABENL}$	$\overline{AB}$x, ABx			5	10		5	10	ns

†See Parameter Measurement Information for load circuits and voltage waveforms.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

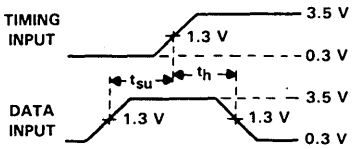
PARAMETER MEASUREMENT INFORMATION

SWITCH POSITION TABLE

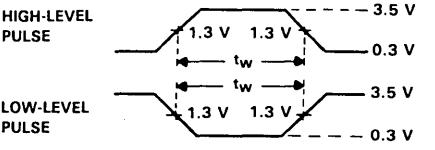
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



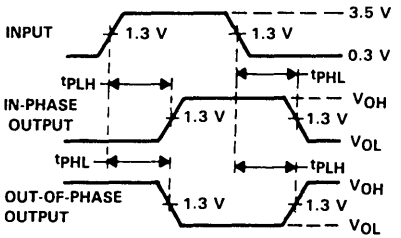
LOAD CIRCUIT



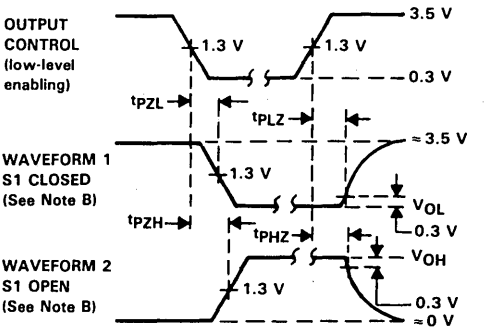
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

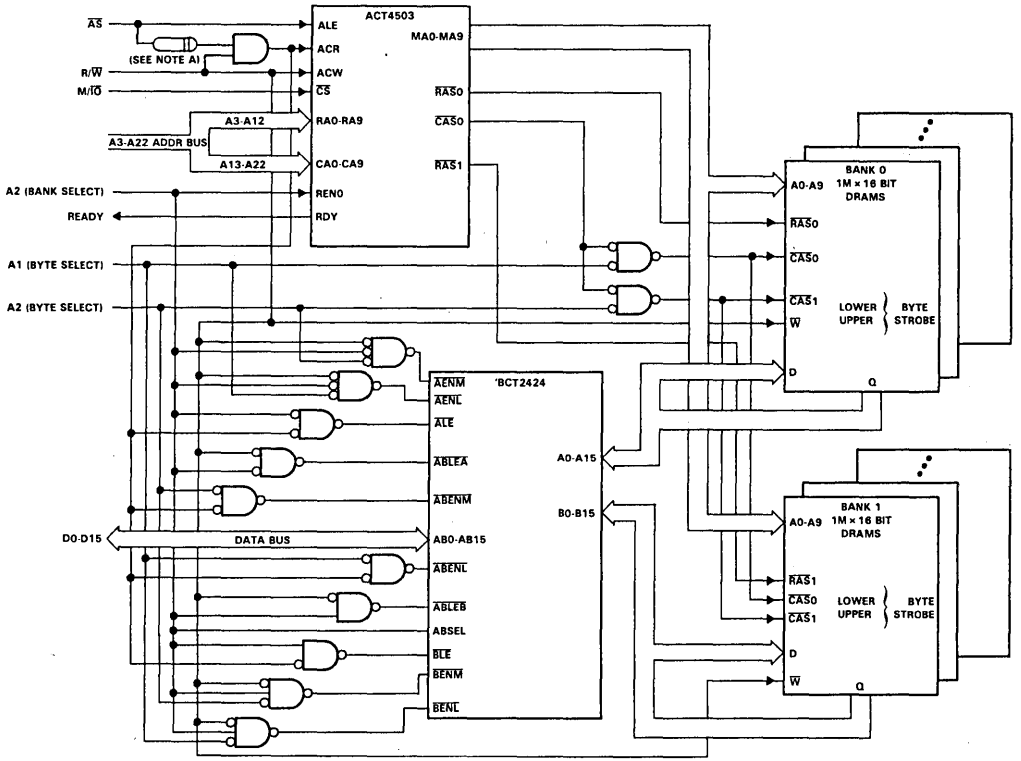


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
D. The outputs are measured one at a time with one transition per measurement.

FIGURE 1

APPLICATION INFORMATION



NOTE A: The value of this delay element is dependent on the speed of the microprocessor.

FIGURE 2. TYPICAL MEMORY INTERLEAVE APPLICATION

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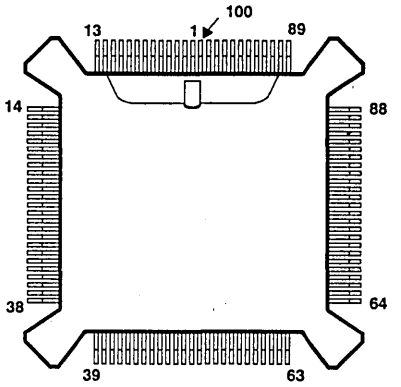
D3361, FEBRUARY 1990–REVISED JANUARY 1991

- **Designed to Support Apple Computer Macintosh Coprocessor Platform (MCP) Interface Applications**
- **Designed to Operate with the SN74ACT2441 MCP NuBus™ Interface Controller**
- **Includes NuBus™ Address and Data Path Circuitry Along with Memory Address Drivers**
- **Conforms to Apple Computer Macintosh II Family NuBus™ Interface Specifications**
- **BICMOS Design Substantially Reduces Standby Current**
- **Available in 100-pin Plastic Quad Flat Package**

PQ PACKAGE
(TOP VIEW)



description

The SN74BCT2425 consists of bus transceiver circuits, D-type flip-flops, memory drivers, and control circuitry arranged for multiplexed transmission of address and data information in Macintosh Coprocessor Platform (MCP) applications.

The MCP is a generic software and hardware foundation developed by Apple Computer and may be used in the development of add-in cards and software applications for the Macintosh II computer.

The MCP provides an intelligent NuBus™ interface that includes hardware support for an MC68000 processor, an application specific I/O processor, ROM, and dynamic memory. Software support for the MCP architecture consists of the A/ROSE operating system (Apple Real-time Operating System Enviroment). A/ROSE is downloaded onto the Macintosh II I/O card for execution by the on-board MC68000.

For a complete description of the Apple Macintosh NuBus™ implementation, see *Designing Cards and Drivers for Macintosh II and Macintosh SE* published by Addison Wesley, or contact the Apple Programmers and Developers Association (APDA). For additional information on MCP or A/ROSE, contact Apple Computer directly.

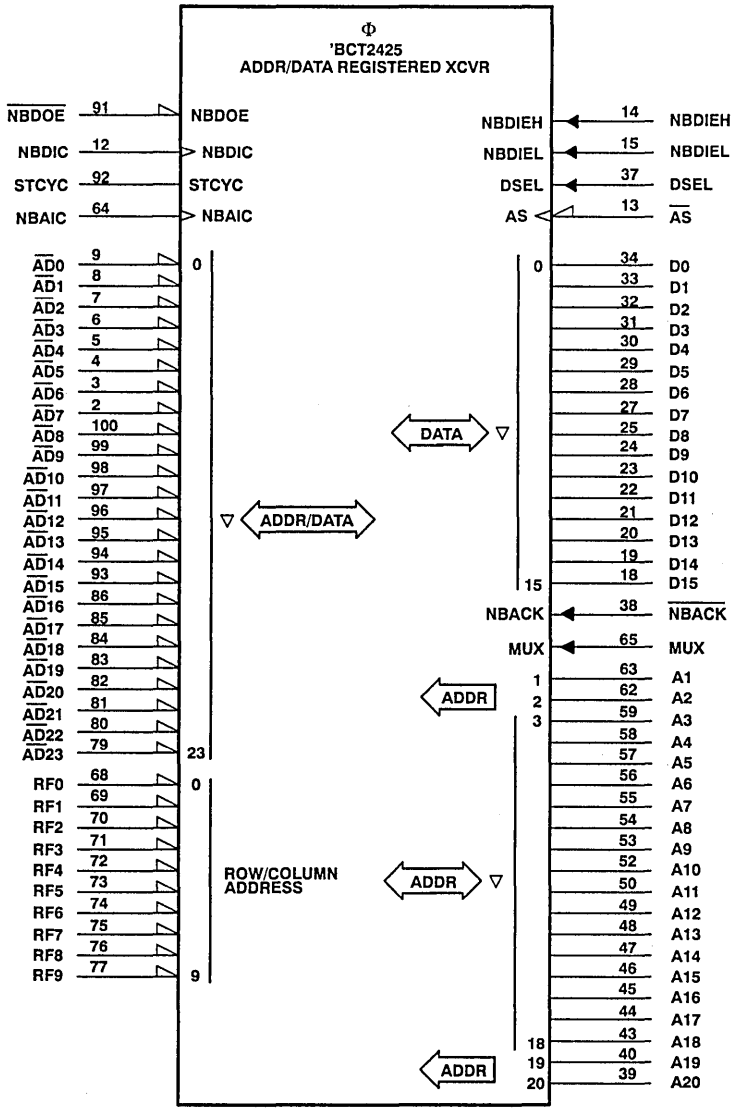
The SN74BCT2425 is characterized for operation from 0°C to 70°C.

NuBus is a trademark of Texas Instruments Incorporated.

Pin Assignments

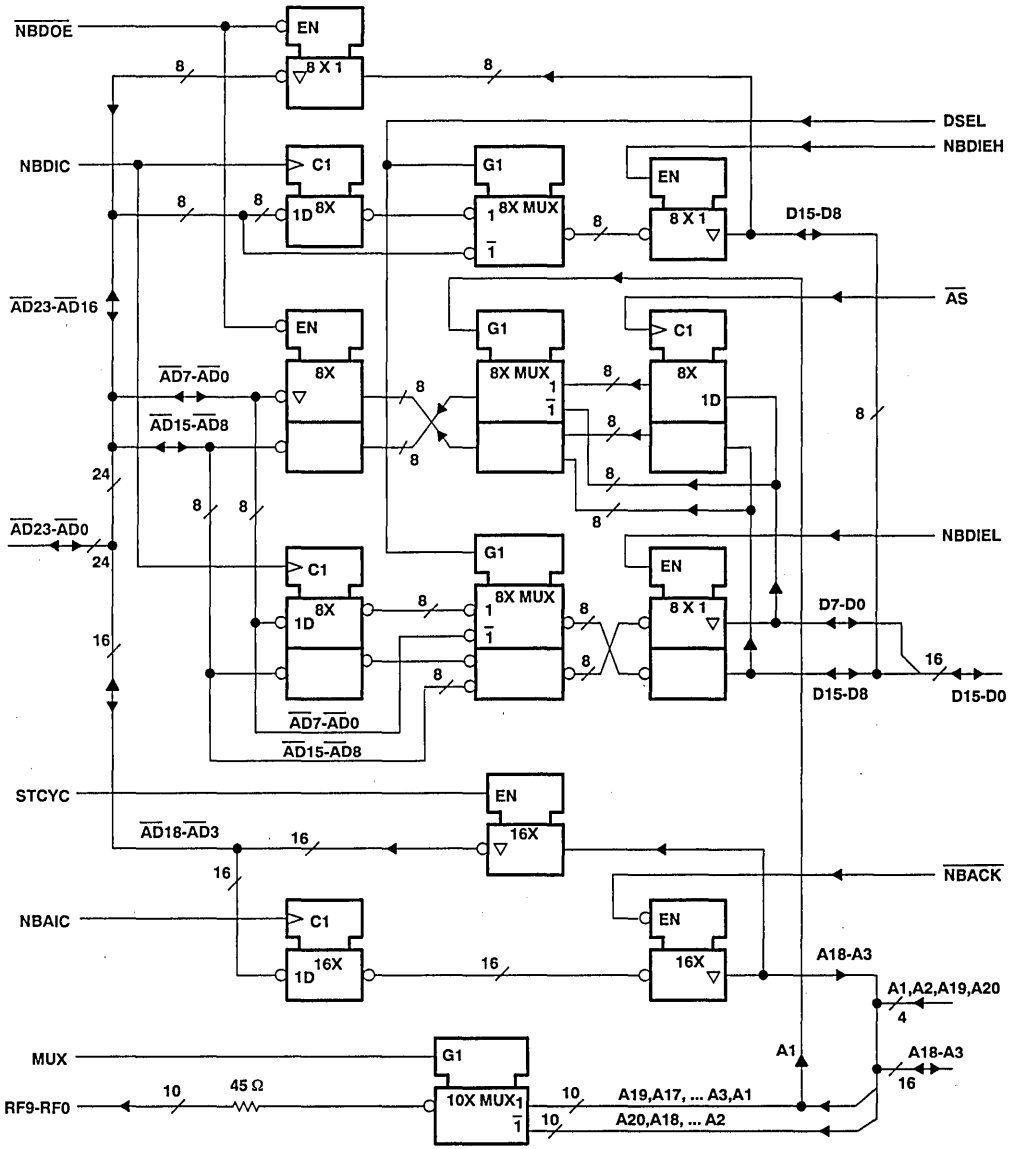
PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	GND	21	D12	41	V_{CC}	61	V_{CC}	81	$\overline{AD}$21
2	$\overline{AD}$7	22	D11	42	GND	62	A2	82	$\overline{AD}$20
3	$\overline{AD}$6	23	D10	43	A18	63	A1	83	$\overline{AD}$19
4	$\overline{AD}$5	24	D9	44	A17	64	NBAIC	84	$\overline{AD}$18
5	$\overline{AD}$4	25	D8	45	A16	65	MUX	85	$\overline{AD}$17
6	$\overline{AD}$3	26	GND	46	A15	66	V_{CC}	86	$\overline{AD}$16
7	$\overline{AD}$2	27	D7	47	A14	67	GND	87	GND
8	$\overline{AD}$1	28	D6	48	A13	68	RF0	88	V_{CC}
9	$\overline{AD}$0	29	D5	49	A12	69	RF1	89	V_{CC}
10	GND	30	D4	50	A11	70	RF2	90	GND
11	V_{CC}	31	D3	51	GND	71	RF3	91	$\overline{NBDOE}$
12	NBDIC	32	D2	52	A10	72	RF4	92	STCYC
13	$\overline{AS}$	33	D1	53	A9	73	RF5	93	$\overline{AD}$15
14	NBDIEH	34	D0	54	A8	74	RF6	94	$\overline{AD}$14
15	NBDIEL	35	GND	55	A7	75	RF7	95	$\overline{AD}$13
16	V_{CC}	36	V_{CC}	56	A6	76	RF8	96	$\overline{AD}$12
17	GND	37	DSEL	57	A5	77	RF9	97	$\overline{AD}$11
18	D15	38	$\overline{NBACK}$	58	A4	78	GND	98	$\overline{AD}$10
19	D14	39	A20	59	A3	79	$\overline{AD}$23	99	$\overline{AD}$9
20	D13	40	A19	60	GND	80	$\overline{AD}$22	100	$\overline{AD}$8

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

logic diagram



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TERMINAL FUNCTIONS

PIN NAME	DESCRIPTION
A20–A1	Local Address Bus. This 20-bit I/O port directly interfaces to the local address bus A23-A0.
$\overline{AD}23$-$\overline{AD}0$	Address/Data Port. This 24-bit active low I/O port directly interfaces to the NuBus™ address/data lines. These lines are multiplexed to carry address at the beginning of a NuBus™ cycle, and data information in the last portion of the NuBus™ cycle.
$\overline{AS}$	Address Strobe. This input is used for saving data information on the low-to-high transition of $\overline{AS}$. The $\overline{AS}$ input is typically connected to both the 'ACT2441 and the MC6800.
D15–D0	Data Address Bus. This 16-bit I/O port directly interfaces to the local data bus.
DSEL	Data Select. This input controls the data multiplexer for the local data bus. When this input is driven low, the NuBus™ addresses $\overline{AD}23$-$\overline{AD}0$ are selected as inputs to the output data buffer. When DSEL is driven high, the NuBus™ data saved in the data input registers are selected as inputs to the output data buffer.
MUX	Multiplex Row/Column Addresses. This input is used to select between row and column addresses when reading or writing to memory. This signal is driven by the 'ACT2441.
$\overline{NBACK}$	NuBus™ Acknowledge. This active-low input is used to enable NuBus™ address information, saved via the NBAIC input, onto the local A20-A1 address lines.
NBAIC	NuBus™ Address Input Clock. This input is used for saving the address portion of NuBus™ read or write cycles. Data present at the $\overline{AD}18$-$\overline{AD}3$ I/O port is clocked into the address register on the low-to-high transition of NBAIC.
NBDIC	NuBus™ Data Input Clock. This input is used for saving the data portion of NuBus™ read or write cycles. Data present at the $\overline{AD}23$-$\overline{AD}0$ I/O port is clocked into the data registers on the low-to-high transition of NBDIC.
NBDIEL	NuBus™ Data Input Enable Low. This active-high input is used to enable NuBus™ data information onto the local bus (D15-D0) for the lower 16-bits corresponding to $\overline{AD}15$-$\overline{AD}0$.
NBDIEH	NuBus™ Data Input Enable High. This active-high input is used to enable NuBus™ data information onto the local bus (D15-D8) for the upper 8-bits corresponding to $\overline{AD}23$-$\overline{AD}16$. The remaining 8-bits D7-D0, corresponding to $\overline{AD}31$-$\overline{AD}24$, are supplied by the 'ACT2441.
$\overline{NBDOE}$	NuBus™ Data Output Enable. This active-low input is used to enable the $\overline{AD}23$-$\overline{AD}0$ outputs. When $\overline{NBDOE}$ is taken inactive (high), the $\overline{AD}23$-$\overline{AD}0$ outputs are at high impedance (assuming STCYC is also inactive).
RF0-RF9	Memory Row/Column Addresses. These outputs are used for driving row and column address information onto the DRAM address bus. Each output has an internal 45-Ω resistor in series with the output pin for the purpose of supressing signal overshoot and undershoot.
STCYC	Start Cycle Active. This active-high input is used to enable the local bus address lines A18-A3 onto the NuBus™ $\overline{AD}18$-$\overline{AD}3$ bus lines. The remainder of the 24-bit address lines are driven directly from the 'ACT2441 MCP NuBus™ controller. When STCYC is taken inactive (low), the $\overline{AD}18$-$\overline{AD}3$ outputs are at high impedance.

Function Tables

DATA BUS PORT MODE

CONTROL INPUTS				DATA INPUTS			OUTPUTS	
DSEL	NBDIC	NBDIEL	NBDIEH	$\overline{AD23}$-$\overline{AD16}$	$\overline{AD15}$-$\overline{AD8}$	$\overline{AD7}$-$\overline{AD0}$	D15-D8	D7-D0
X	X	L	L	X	X	X	Z	Z
L	X	L	H	L	X	X	H	Z
				H	X	X	L	Z
L	X	H	L	X	H	L	H	L
				X	L	H	L	H
L	X	H	H	Unallowed input condition				
H	↑	L	H	L	X	X	H	Z
				H	X	X	L	Z
	No↑			X	X	X	NC	Z
H	↑	H	L	X	H	L	H	L
				X	L	H	L	H
	No↑			X	X	X	NC	NC
H	X	H	H	Unallowed input condition				

Inputs $\overline{AD15}$-$\overline{AD8}$ map to outputs D7-D0, and inputs $\overline{AD7}$-$\overline{AD0}$ map to outputs D15-D8, respectively, in the applicable mode.
Inputs $\overline{AD23}$-$\overline{AD16}$ map to outputs D15-D8, respectively, in the applicable mode.

NuBus™ PORT OUTPUT MODE

CONTROL INPUTS				DATA INPUTS			OUTPUTS			
A1	$\overline{AS}$	$\overline{NBDOE}$	STCYC	A18-A3	D15-D8	D7-D0	$\overline{AD23}$-$\overline{AD19}$	$\overline{AD18}$-$\overline{AD16}$	$\overline{AD15}$-$\overline{AD3}$	$\overline{AD2}$-$\overline{AD0}$
X	X	H	L	X	X	X	Z	Z	Z	Z
L	X	H	H	L	X	X	Z	H	H	Z
				H	X	X	Z	L	L	Z
L	X	L	L	X	L	L	H	H	H	H
				X	H	H	L	L	L	L
L	X	L	H	Unallowed input condition						
H	X	H	H	L	X	X	Z	H	H	Z
				H	X	X	Z	L	L	Z
H	↑	L	L	X	L	L	H	H	H	H
				X	H	H	L	L	L	L
H	No↑	L	L	X	L	L	H	H	NC	NC
				X	H	H	L	L	NC	NC
H	X	L	H	Unallowed input condition						

Inputs A18-A3 map to outputs $\overline{AD18}$-$\overline{AD3}$, respectively in the applicable mode.
Inputs D15-D8 map to outputs $\overline{AD23}$-$\overline{AD16}$, respectively in the applicable mode.
Inputs D7-D0 map to outputs $\overline{AD15}$-$\overline{AD8}$, and inputs D15-D8 map to outputs $\overline{AD7}$-$\overline{AD0}$, respectively in the applicable mode
H denotes a high level, L denotes a low level, Z denotes a high-impedance state, ↑ denotes a low-to-high logic level transition, NC denotes no change, and X denotes a level that does not affect the result.

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Function Tables

MEMORY DRIVER PORT

CONTROL	DATA INPUTS		OUTPUTS
MUX	A20, A18, A16, A14, A12, A10, A8, A6, A4, A2	A19, A17, A15, A13, A11, A9, A7, A5, A3, A1	RF9-RF0
L	L	X	H
	H	X	L
H	X	L	H
	X	H	L

Inputs A20, A18, A16, A14, A12, A10, A8, A6, A4, A2 map to outputs RF9-RF0, respectively.
Inputs A19, A17, A15, A13, A11, A9, A7, A5, A3, A1 map to outputs RF9-RF0, respectively.

ADDRESS PORT OUTPUT MODE

CONTROL		DATA INPUTS	OUTPUTS
NBAIC	$\overline{\text{NBACK}}$	$\overline{\text{AD18}}$-$\overline{\text{AD3}}$	A18–A3
X	H	X	Z
↑	L	L	H
↑		H	L
No ↑		X	NC

Inputs $\overline{\text{AD18}}$-$\overline{\text{AD3}}$ map to A18-A3, respectively.
H denotes a high level, L denotes a low level, Z denotes a high-impedance state, ↑ denotes a low-to-high logic level transition, NC denotes no change, and X denotes a level that does not affect the result.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage range, V_I ..... 5.5 V
Operating free-air temperature, T_A ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminal.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				– 15	mA
I_{OL}	Low-level output current	Ax, Dx, $\overline{\text{ADx}}$, outputs			24	mA
		RFx outputs			12	
t_w	Pulse duration	Clocks high	12.5			ns
		Clocks low	12.5			
t_{su}	Setup time		10			ns
t_h	Hold time		3			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = – 18 mA			– 1.2	V
V_{OH}		V_{CC} = 4.5 to 5.5 V,	I_{OH} = – 400 µA	V_{CC} – 1.5			V
		V_{CC} = 4.5 V,	I_{OH} = – 3 mA	2.8	3.6		
		V_{CC} = 4.5 V,	I_{OH} = – 15 mA	2			
V_{OL}	Ax, Dx, $\overline{ADx}$	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
	Ax, Dx, $\overline{ADx}$	V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
	RF	V_{CC} = 4.5 V,	I_{OL} = 1 mA		0.2	0.4	
	RF	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.8	1	
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V			100	µA
I_{OL}	RF	V_{CC} = 4.5 V,	V_O = 2 V	15			mA
I_{IH}‡	$\overline{NBACK}$, NBDIEL, $\overline{NBDOE}$	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
	All other inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			– 100	
I_{IL}‡	NBDIEL, NBDIEH, $\overline{NBDOE}$, STCYC	V_{CC} = 5.5 V,	V_I = 0.4 V			– 300	µA
	All other inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			– 200	
I_O§	Ax, Dx, $\overline{ADx}$	V_{CC} = 5.5 V,	V_O = 2.25 V	– 30		– 112	mA
	RF	V_{CC} = 5.5 V,	V_O = 2.25 V	– 20		– 50	
I_{CC}		V_{CC} = 5.5 V, V_{IH} = 3 V, V_{IL} = 0, Outputs open	Maximum number of outputs low		111	172	mA
			Maximum number of outputs disabled (high-Z)		40	68	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been selected to produce a current that closely approximates one half of the true short-circuit current I_{OS}.

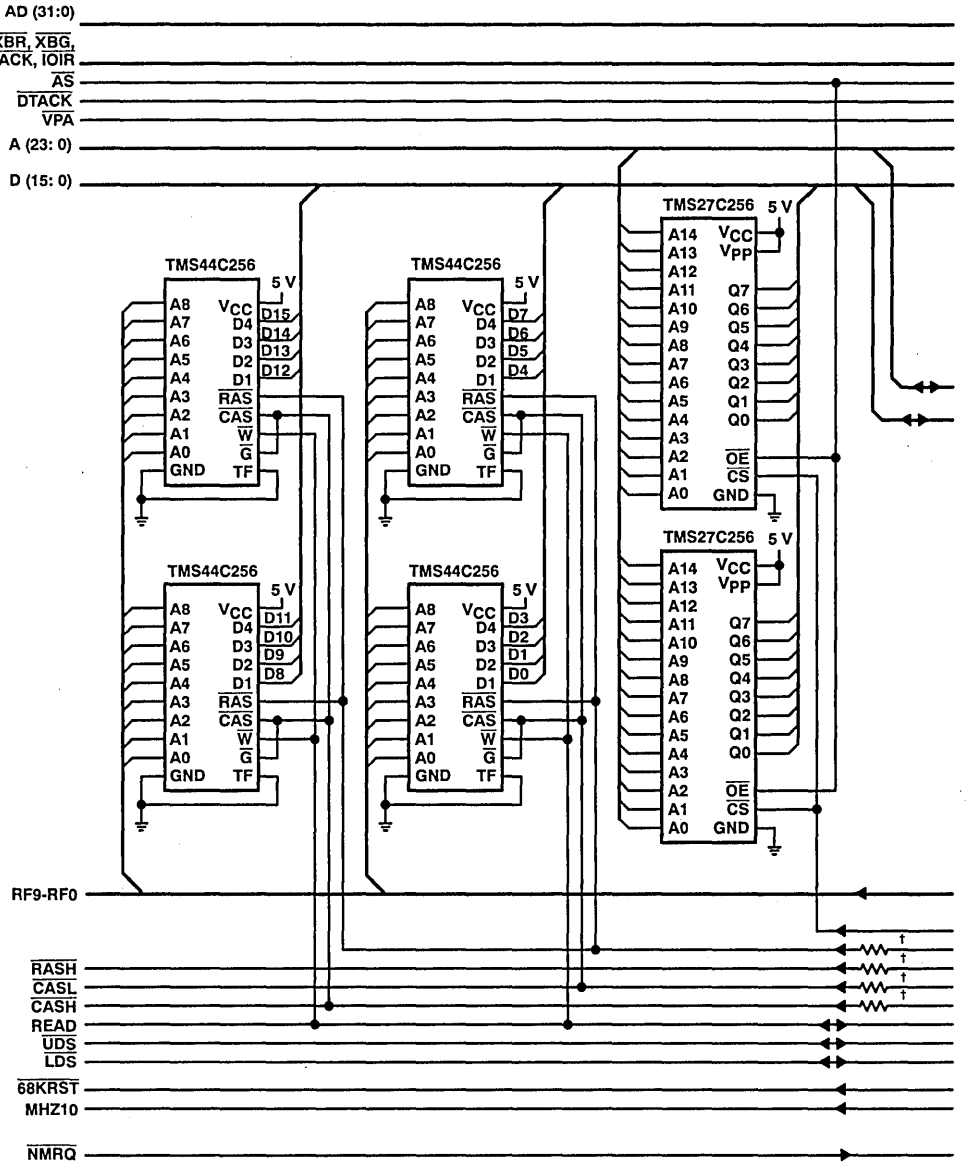
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)†

PARAMETER	FROM (INPUT)	TO (OUTPUT)†	TEST CONDITIONS				MIN	TYP‡	MAX	UNIT
			V_L (V)	R1 (Ω)	R2 (Ω)	C_L (pF)				
t_{pd}	A3-A18	$\overline{AD3}$-$\overline{AD18}$	V_{CC}	270	470	130		11	18	ns
t_{pd}	D0-D15	$\overline{AD0}$-$\overline{AD15}$						11	18	ns
t_{pd}	D8-D15	$\overline{AD16}$-$\overline{AD23}$						11	18	ns
t_{pd}	$\overline{AS}$↑	$\overline{AD0}$-$\overline{AD15}$						14	22	ns
t_{pd}	A1	$\overline{AD0}$-$\overline{AD15}$						14	22	ns
t_{pd}	$\overline{AD0}$-$\overline{AD23}$	D0-D15	open	open	500	50		9	16	ns
t_{pd}	NBDIC↑	D0-D15						12	21	ns
t_{pd}	DSEL	D0-D15						15	23	ns
t_{pd}	NBAIC↑	A3-A18						10	18	ns
t_{pd}	A1-A20	RF0-RF9	open	open	2 k	50		9	16	ns
t_{pd}	MUX	RF0-RF9						9	16	ns
t_{en}	$\overline{NBDOE}$	$\overline{AD0}$-$\overline{AD23}$	V_{CC}	270	470	130		12	20	ns
t_{en}	STCYC	$\overline{AD3}$-$\overline{AD18}$						14	22	ns
t_{en}	NBDIEL	D0-D15	7	500	500	50		11	22	ns
t_{en}	NBDIEH	D8-D15						11	22	ns
t_{en}	$\overline{NBACK}$	A3-A18						10	20	ns
t_{dis}	$\overline{NBDOE}$	$\overline{AD0}$-$\overline{AD23}$	V_{CC}	270	470	50		6	10	ns
t_{dis}	STCYC	$\overline{AD3}$-$\overline{AD18}$						6	10	ns
t_{dis}	NBDIEL	D0-D15	7	500	500	50		6	10	ns
t_{dis}	NBDIEH	D8-D15						6	10	ns
t_{dis}	$\overline{NBACK}$	A3-A18						6	10	ns

† The outputs are measured one at a time with one transition per measurement or in the PAD mode two outputs switching at one time.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

APPLICATION INFORMATION



† Series damping resistors are recommended but may not be required depending on system environment.

Figure 1. MacIntosh Coprocessor Platform (MCP) Architecture (configured with 1 row of 245K x 4 DRAMs)

APPLICATION INFORMATION

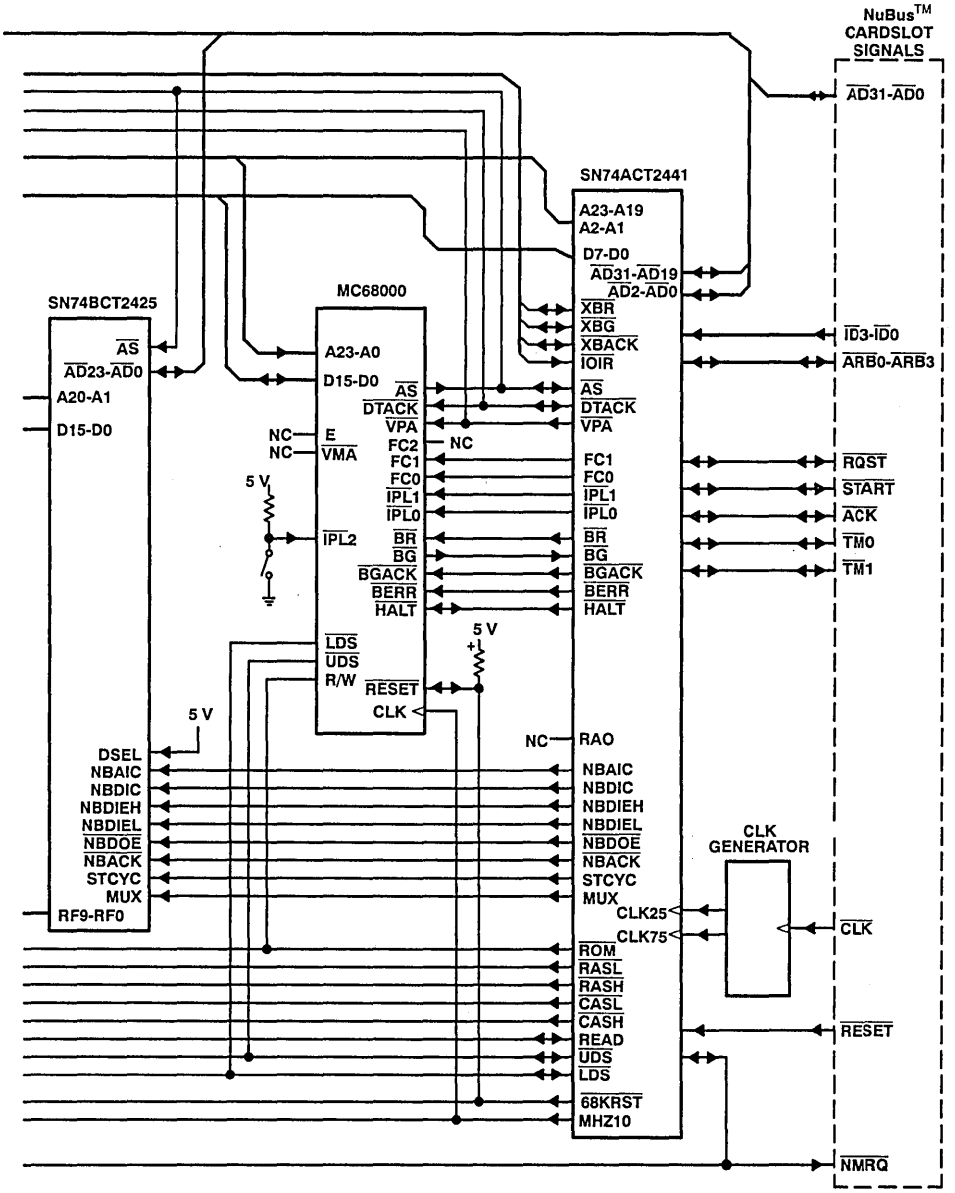
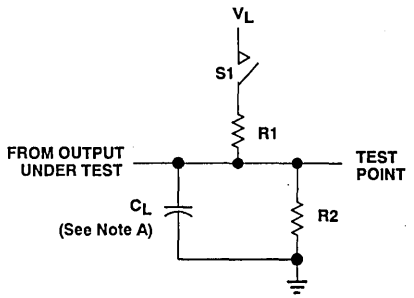


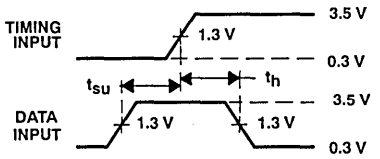
Figure 1. Macintosh Coprocessor Platform (MCP) Architecture (Continued)
(configured with 1 row of 245K x 4 DRAMs)

PARAMETER MEASUREMENT INFORMATION

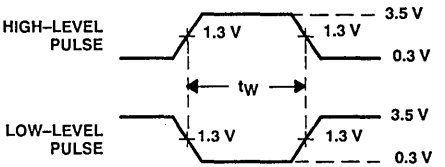
SWITCH POSITION TABLE

TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed

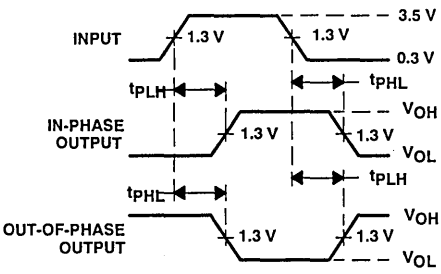




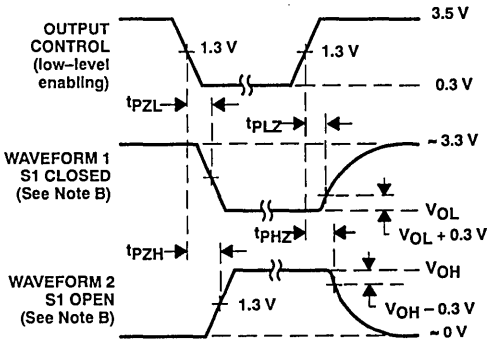
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2

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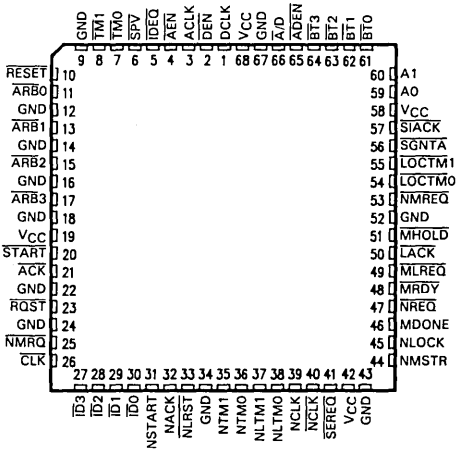
D3158, OCTOBER 1988–REVISED JANUARY 1991

- Designed for NuBus™ Interface Applications
- Supports Master, Slave, and Master/Slave Applications
- Conforms to ANSI/IEEE Std 1196-1987
- Designed to Operate with SN74BCT2420 NuBus™ Data/Address Interface Devices
- Supports NuBus™ 1987 Block Transfers with the Addition of the SN74ALS2442
- EPIC™ (Enhanced Performance Implanted CMOS) 1-μm Process
- Fully TTL-Compatible
- Dependable Texas Instruments Quality and Reliability

FN PACKAGE
(TOP VIEW)



description

The 'ACT2440 NuBus™ Controller handles NuBus™ signaling protocol in compliance with ANSI/IEEE Std 1196-1987. The device allows a simple connection to the NuBus™; typical configurations include master-only, slave-only, and master/slave. Additionally, it provides extra status and control lines to facilitate more sophisticated approaches. With the addition of the SN74ALS2442, slave block transfers can be supported by this device. For additional details on block transfers, consult the SN74ALS2442 data sheet and the application note titled *Supporting NuBus™ Block Slave Transfers Using Texas Instruments SN74ACT2440, SN74BCT2420, and SN74ALS2442.*

Figure 1 shows a typical NuBus™ interface using the 'ACT2440. Data and address buffering is handled via two SN74BCT2420s. The SN74BCT2420s are BiCMOS buffers designed specifically for supporting NuBus™ interfacing. The 'ACT2440 provides the buffer control signals needed to directly drive the SN74BCT2420s; however, in simpler applications, standard SSI and MSI buffers may be used in place of the 'BCT2420s.

The 'ACT2440 is comprised of five major signal groups: byte decode signals, data/address interface-control signals, master/slave input signals, NuBus™ card-slot signals, and NuBus™ status signals. Byte decode determines which type of NuBus™ cycle is being performed. Data/address interface control provides the buffering signals required to multiplex and de-multiplex the NuBus™ data/address lines. The master/slave inputs control the master- and slave-state machines. The NuBus™ card-slot signals interface with the NuBus™. The NuBus™ status signals indicate the status of the master/slave-state machines and provide buffered NuBus™ signals. Refer to Table 1 for additional details.

The SN74ACT2440 is characterized for operation from 0°C to 70°C.

NuBus is a trademark of Texas Instruments Incorporated.
EPIC is a trademark of Texas Instruments Incorporated.

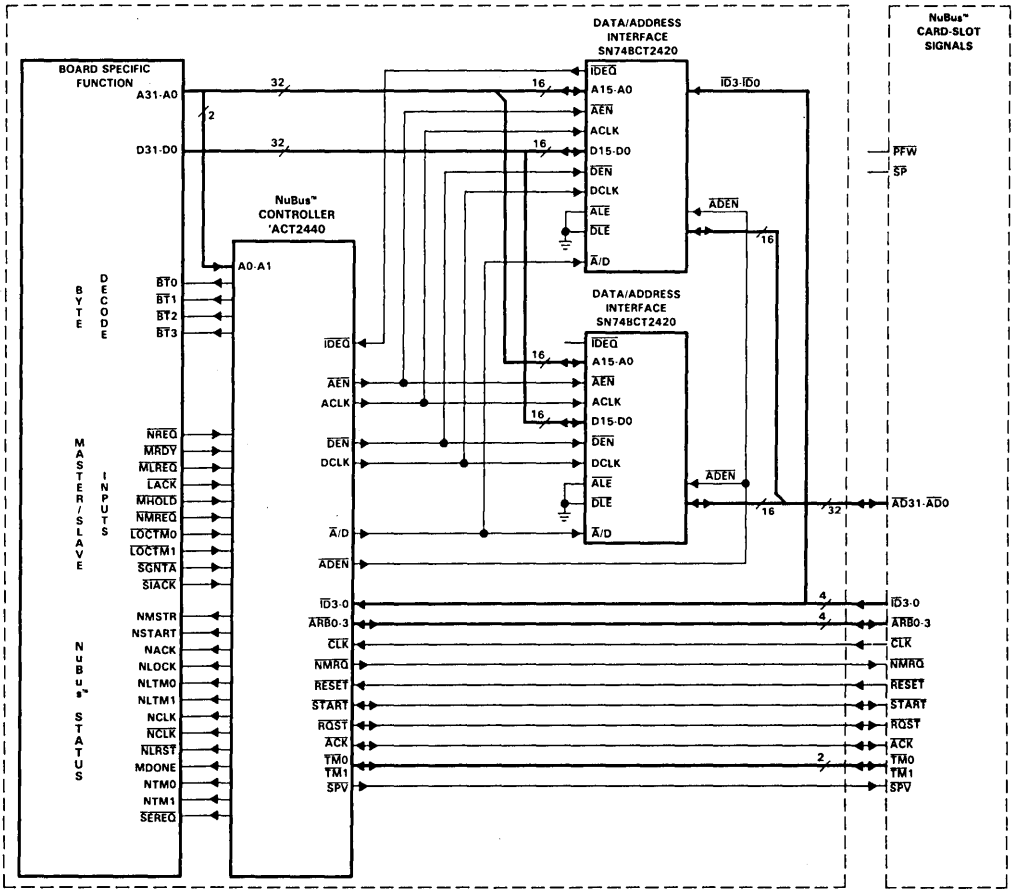


FIGURE 1. TYPICAL 'ACT2440 NuBus™ INTERFACE

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TERMINAL FUNCTIONS

As previously explained, the input and output signals on the 'ACT2440 can be functionally organized into five groups. The following tables briefly describe the controller signals in each group.

DATA/ADDRESS INTERFACE CONTROL SIGNALS

PIN NAME	PIN NO.	DESCRIPTION
ACLK	3	Address Clock. This output loads NuBus™ address information onto the local board. During both master and slave start cycles, this output changes on the sample edge (high-to-low) of the NuBus™ Clock signal ($\overline{CLK}$).
$\overline{A}$/D	66	Output Select. This normally high output controls the multiplexing function of address and data information onto the NuBus™. When low, address information is indicated. When high, data information is indicated. When the local board is the NuBus™ master, $\overline{A}$/D goes low on the driving edge (low-to-high) of start and remains low for one NuBus™ clock period.
$\overline{ADEN}$	65	Output Enable. This active-low output enables data or address information onto the NuBus™. $\overline{ADEN}$ is asserted on the driving edge (low-to-high) of the NuBus™ Clock signal ($\overline{CLK}$) under any of the following conditions: — The local board is the NuBus™ master performing a write cycle and continuing until an acknowledge ($\overline{ACK}$) is received from the NuBus™. — The local board is the NuBus™ master performing a read cycle and continuing for one NuBus™ clock cycle. — The local board is the selected NuBus™ slave during an acknowledge cycle and the current cycle is a read.
$\overline{AEN}$	4	Address Enable. This active-low output signal enables address information onto the local board. When selected as a NuBus™ slave, $\overline{AEN}$ goes low on the first sample edge after Slave Grant Access ($\overline{SGNTA}$) is asserted. $\overline{AEN}$ returns inactive on the first sample edge after $\overline{SGNTA}$ returns inactive. If $\overline{SGNTA}$ is active (low) before the first sample edge after $\overline{START}$, then address information is placed onto the local board on the first sample edge after $\overline{START}$.
DCLK	1	Data Clock. This output loads NuBus™ data onto the local board. This output changes on the sample edge (high-to-low) of the NuBus™ Clock signal ($\overline{CLK}$) under any of the following sets of conditions: — The local board is the NuBus™ master, the current cycle is a read, and an acknowledge ($\overline{ACK}$) or interim acknowledge ($\overline{TMO}$ during block transfers) has been received. — The local board is a NuBus™ slave, the current cycle is a write, and Slave Grant Access ($\overline{SGNTA}$) is asserted. — The local board is a NuBus™ slave and the current cycle is a block write. The first rising edge of DCLK will occur on the first sample edge after $\overline{SGNTA}$ is taken active (low) and will remain high for two clock cycles. If $\overline{SGNTA}$ is active (low) during the start cycle, DCLK will go active (high) on the first sample edge after $\overline{START}$. The $\overline{SIACK}$ input controls the remaining DCLK cycles with the exception of the last DCLK cycle. When the $\overline{SIACK}$ input is taken active (low), DCLK will go active on the following sample edge. DCLK will remain high for one clock cycle and return low, regardless of the $\overline{SIACK}$ input. The final DCLK cycle is controlled by the Local Acknowledge Input ($\overline{LACK}$), as on normal write cycles.
$\overline{DEN}$	2	Data Enable. This active-low output enables data to be placed onto the local board. $\overline{DEN}$ is asserted under either of the following conditions: The local board is the NuBus™ master performing a read cycle. ($\overline{DEN}$ goes low on the sample edge (high- to-low) of the acknowledge cycle and remains low until the first sample edge after $\overline{MHOLD}$ returns inactive.) The local board is the selected NuBus™ slave performing a write cycle. ($\overline{DEN}$ goes low on the first sample edge after Slave Grant Access ($\overline{SGNTA}$) is asserted and remains low until the first sample edge after $\overline{SGNTA}$ returns inactive.)

TERMINAL FUNCTIONS (continued)

MASTER/SLAVE INPUT SIGNALS

PIN NAME	PIN NO.	DESCRIPTION
$\overline{\text{IDEQ}}$	5	ID Equal. This active-low input signal is used by the slave-state machine to detect if the current NuBus™ cycle is addressing the local board. This input is interrogated on the sample edge (high-to-low) of the NuBus™ clock in the cycle following the start cycle. This input is asserted if slot and/or super-slot addresses are broadcast on the previous start cycle.
$\overline{\text{LACK}}$	50	Local Acknowledge. This active-low input signal controls the NuBus™ Acknowledge signal ($\overline{\text{ACK}}$) during slave cycles. When the local board is ready to respond to a NuBus™ transfer request, this input signal is driven low. The $\overline{\text{ACK}}$ output will go active (low) on the next driving edge after $\overline{\text{LACK}}$ is sampled.
$\overline{\text{LOCTM0}}$ $\overline{\text{LOCTM1}}$	54 55	Local Transfer-Mode Control. These input signals determine the sense of the NuBus™ Transfer-Mode signals, $\overline{\text{TM0}}$ and $\overline{\text{TM1}}$, during master start and slave acknowledge cycles. The controller latches these signals upon detecting the NuBus™ Request signal ($\overline{\text{NREQ}}$). During a NuBus™ slave acknowledge cycle, the NuBus™ TM lines reflect the current state of these inputs.
$\overline{\text{MHOLD}}$	51	Master Hold. This active-low input signal is used by the buffer control logic to hold data on the local board after the NuBus™ cycle terminates. If this signal is true when the acknowledge cycle is received (for a NuBus™ cycle initiated by this controller) and the current cycle is a NuBus™ read, then the Data Enable signal (DEN) remains true until $\overline{\text{MHOLD}}$ is unasserted. Additionally, the latched TM status lines (NLTM0, NLTM1) continue to reflect the TM information presented on the NuBus™ during the acknowledge cycle (this applies to both reads and writes). While the holding function is active, the controller inhibits the local master from issuing another NuBus™ start cycle when $\overline{\text{NREQ}}$ is not taken inactive after the acknowledge. In other words, $\overline{\text{MHOLD}}$ allows only one start cycle to occur.
$\overline{\text{MLREQ}}$	49	Master Lock Request. This active-low input signal, in conjunction with $\overline{\text{NREQ}}$, causes the controller to lock the NuBus™ by issuing an Attention Lock Resource cycle after winning arbitration. When $\overline{\text{MLREQ}}$ is taken inactive, the controller automatically issues a NuBus™ Attention Null cycle (regardless of the state of $\overline{\text{NREQ}}$). The Attention Null cycle signals the end of the locked resource tenure.
$\overline{\text{MRDY}}$	48	Master Ready. This active-low input signal indicates to the controller that the local board is ready to perform a NuBus™ master start cycle. The current state of the master-state machine determines this signal's effect. If the master-state machine enters the arbitration process (with no lock request) and wins mastership of the bus, this signal can delay issuing a start cycle for up to 16 NuBus™ clock periods. After this period, the master-state machine automatically issues a NuBus™ Attention Null cycle, returns to the idle state, and re-enters the arbitration process. If the master-state machine enters the arbitration process with lock request asserted, it issues an Attention Lock cycle immediately upon acquiring mastership of the bus. The master-state machine then waits for $\overline{\text{MRDY}}$ to be asserted before issuing a NuBus™ start cycle. There is no timer in the lock mode. If the master-state machine is parked on the bus, this signal is simply ANDed with the NuBus™ Request signal ($\overline{\text{NREQ}}$) to generate the start cycle.
$\overline{\text{NMREQ}}$	53	NonMaster Request. This nonsynchronous active-low input asserts the NuBus™ NonMaster Request signal ($\overline{\text{NMRQ}}$).
$\overline{\text{NREQ}}$	47	NuBus™ Request. This active-low input signal indicates to the controller that the local board wants access to the NuBus™. It initiates arbitration if the local board is not already the bus master.
$\overline{\text{SGNTA}}$	56	Slave Grant Access. This active-low input signal indicates to the slave-state machine that the local board resources are available. When this signal is asserted and an external request is pending, the slave-state machine issues the proper enable signals ($\overline{\text{AEN}}$ and $\overline{\text{DEN}}$). These enable signals remain active until $\overline{\text{SGNTA}}$ is unasserted.
$\overline{\text{SIACK}}$	57	Slave Interim Acknowledge. This active-low input signal indicates to the slave-state machine that an interim acknowledge (required for block transfers) should be issued on the NuBus™. The controller responds by asserting $\overline{\text{TM0}}$ during block transfers.

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TERMINAL FUNCTIONS (continued)

NuBus™ CARD-SLOT SIGNALS

PIN NAME	PIN NO.	DESCRIPTION
$\overline{ACK}$	21	Transfer Acknowledge. This bidirectional I/O pin signals the end of a transaction. It also signals attention cycles.
$\overline{ARB0}$	11	Arbitration Signals. These four I/O lines are bused and binary encoded in the same manner as the $\overline{ID3}$–$\overline{ID0}$ lines. During an arbitration contest, contending modules compare these lines with the binary value of their own $\overline{ID3}$–$\overline{ID0}$ lines. Each module drives the $\overline{ARB3}$–$\overline{ARB0}$ lines according to the rules of the distributed arbitration logic. The net effect of the arbitration contest is that the $\overline{ARB3}$–$\overline{ARB0}$ lines carry the binary-encoded number of the next NuBus™ owner.
$\overline{ARB1}$	13	
$\overline{ARB2}$	15	
$\overline{ARB3}$	17	
$\overline{CLK}$	26	Clock. The NuBus™ Clock signal is tied directly to the controller. Bus arbitration and data transfers are synchronized to this signal.
$\overline{ID0}$	30	Card-Slot Identification. These four input lines are not bused but are binary encoded at each card-slot position to specify the module's position on the backplane. The controller uses these inputs when requesting access to the NuBus™.
$\overline{ID1}$	29	
$\overline{ID2}$	28	
$\overline{ID3}$	27	
$\overline{NMRQ}$	25	NonMaster Request. This asynchronous output on the 'ACT2440 is controlled by the $\overline{NMRQ}$ input on the 'ACT2440 and can be used in applications where the local board is not capable of becoming a bus master but wishes to issue an interrupt. In systems that use the $\overline{NMRQ}$ line as a bused signal (all $\overline{NMRQ}$ signals tied common), the $\overline{NMRQ}$ output on the 'ACT2440 must first be buffered through an open-collector driver. In systems that use the $\overline{NMRQ}$ signal as an individual interrupt line, the $\overline{NMRQ}$ output on the 'ACT2440 does not have to be buffered with an open-collector driver.
$\overline{RESET}$	10	Reset. This asynchronous input monitors the NuBus™ $\overline{RESET}$ line. When taken active (low), it initializes the NuBus™ controller.
$\overline{RQST}$	23	Bus Request. This bidirectional I/O pin is asserted by the controller when the local board wants ownership of the bus.
$\overline{SPV}$	6	System Parity Valid. System Parity Valid signals the NuBus™ when parity has been generated for the $\overline{AD31}$–$\overline{AD0}$ lines. The controller drives this line inactive during master and slave cycles to indicate that no parity has been generated.
$\overline{START}$	20	Start. This bidirectional I/O pin is asserted at the start of a NuBus™ transaction and also initiates an arbitration contest. When asserted in conjunction with the $\overline{ACK}$ line, it denotes special nontransaction cycles called attention cycles.
$\overline{TM0}$	7	Transfer Mode. At the beginning of a transaction, these two lines indicate the type of transaction being initiated. Later in the transaction, the responding module uses them to indicate success or failure of the requested transaction.
$\overline{TM1}$	8	

BYTE DECODE SIGNALS

PIN NAME	PIN NO.	DESCRIPTION
A0	59	Inverted NuBus™ Address Inputs. These two controller inputs require inverted versions of the NuBus™ Address signals $\overline{AD0}$ and $\overline{AD1}$ (as provided from the 'BCT2420 data/address interface device). These signals, in conjunction with the NuBus™ Transfer-Mode signals ($\overline{TM0}$, $\overline{TM1}$), define the type of transfer cycle (i.e., byte, halfword, or block).
A1	60	
$\overline{BT0}$	61	Byte Control Outputs. These active-low outputs are decoded from the A0, A1, and $\overline{TM0}$ controller inputs. The NuBus™ signal $\overline{TM1}$ defines whether the current cycle is a read or a write. Refer to Table 1, Byte Decode Function Table, for additional details.
$\overline{BT1}$	62	
$\overline{BT2}$	63	
$\overline{BT3}$	64	

TERMINAL FUNCTIONS (continued)

NuBus™ STATUS SIGNALS

PIN NAME	PIN NO.	DESCRIPTION
MDONE	46	Master Done. This active-high output signal is asserted when the local board is the NuBus™ master and the responding slave's acknowledge ($\overline{ACK}$) has been received. Once asserted, it remains asserted until $\overline{MHOLD}$ is unasserted.
NACK	32	NuBus™ Acknowledge. This output is an inverted buffered version of the NuBus™ Acknowledge signal ($\overline{ACK}$).
NCLK	39	Inverted NuBus™ Clock. This output signal is an inverted buffered version of the NuBus™ Clock signal ($\overline{CLK}$).
$\overline{NCLK}$	40	Buffered Nubus Clock. This output signal is a buffered version of the NuBus™ Clock signal ($\overline{CLK}$).
NLOCK	45	NuBus™ Locked. This active-high output signal indicates to the local board that another master has generated an Attention Lock cycle and the local board is the requested slave. This output is asserted one clock after the NuBus™ start cycle on the sample edge (high-to-low) of the NuBus™ Clock signal ($\overline{CLK}$). NLOCK is active only during slave cycles. NLOCK is not active during master cycles.
$\overline{NLRST}$	33	NuBus™ Latched Reset. This active-low output is a synchronized (2-level) version of the asynchronous NuBus™ Reset signal ($\overline{RESET}$).
NLTM0 NLTM1	38 37	NuBus™ Latched Transfer Mode. These status signals are latched inverted versions of the NuBus™ $\overline{TM}$x signals. They are double-latched to allow the local board to continue using $\overline{TM}$x information. During NuBus™ master cycles, the transfer code is latched on the sample edge of the start cycle. The transfer code remains latched until a slave responds with an acknowledge cycle. The transfer status is latched on the sample edge of the acknowledge cycle. The transfer status remains latched as long as $\overline{MHOLD}$ is held active (low). After $\overline{MHOLD}$ returns inactive, the transfer status remains latched until the next NuBus™ start cycle. During slave cycles, the transfer code is latched on the sample edge of the start cycle. The transfer code remains latched as long as $\overline{SGNTA}$ is held active (low). After $\overline{SGNTA}$ returns inactive, the transfer code remains latched until the next NuBus™ start cycle.
NMSTR	44	NuBus™ Master. This active-high output indicates to the local board that the local board has won arbitration and is now the NuBus™ master. It is asserted on the sample edge (high-to-low) of the NuBus™ Clock signal ($\overline{CLK}$) after winning arbitration. NMSTR remains asserted until the local board loses mastership.
NTM0 NTM1	36 35	NuBus™ Buffered Transfer Mode. These outputs are inverted buffered versions of the NuBus™ $\overline{TM}$x lines ($\overline{TM0}$, $\overline{TM1}$).
$\overline{SEREQ}$	41	Slave External Request. This active-low output indicates that the local board is being requested on the NuBus™. The local board responds by driving Slave Grant Access ($\overline{SGNTA}$) active (low) when it is ready to service the request. In higher performance slave-only applications, $\overline{SGNTA}$ may be low going into the NuBus™ cycle.
NSTART	31	NuBus™ Start. This output is an inverted buffered version of the NuBus™ Start signal ($\overline{START}$).

TABLE 1. BYTE DECODE FUNCTION TABLE

$\overline{TM0}$	A1	A0	$\overline{BT0}$	$\overline{BT1}$	$\overline{BT2}$	$\overline{BT3}$	TYPE OF CYCLE
L	L	L	L	H	H	H	Byte 0
L	L	H	H	L	H	H	Byte 1
L	H	L	H	H	L	H	Byte 2
L	H	H	H	H	H	L	Byte 3
H	L	L	L	L	L	L	Full Word
H	L	H	L	L	H	H	1/2 Word 0
H	H	L	L	L	L	L	Block
H	H	H	H	H	L	L	1/2 Word 1

NOTE: $\overline{TM1}$ = L indicates a write cycle. $\overline{TM1}$ = H indicates a read cycle.

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cycle descriptions

master read cycles

When the local board wants to read data from another board connected to the NuBus™, it must first win mastership of the bus. The timing diagram in Figure 2 shows the simplest form of operation for a typical master read cycle with Master Ready ($\overline{\text{MRDY}}$) and Master Hold tied common with $\overline{\text{NREQ}}$. The process begins when the local board takes NuBus™ Request ($\overline{\text{NREQ}}$) active (low) which causes the local board to begin arbitrating for the bus by forcing $\overline{\text{RQST}}$ low.

On the first sample edge after $\overline{\text{NREQ}}$ is taken active (low), the Local Transfer-Mode input lines ($\overline{\text{LOCTM}}$x) are latched into the controller. Depending on the number of other masters competing for the bus, the requesting process can take a few clock cycles. Under the rules of fair arbitration, each requesting master is guaranteed to win ownership of the bus before a previous winner is allowed to re-arbitrate for the bus.

When the local board wins control of the bus, the controller signals the local board by taking NuBus™ Master (NMSTR) active (high). The controller immediately issues a start cycle (if $\overline{\text{MRDY}}$ is active) on the next driving edge by taking $\overline{\text{START}}$ low and placing the read address on the bus.

The accessed slave responds to the read request by placing the read data on the bus and driving NuBus™ Acknowledge ($\overline{\text{ACK}}$) low. The controller signals the local board that the transfer is complete by driving Master Done (MDONE) active (high). The local board responds to the MDONE signal by driving $\overline{\text{NREQ}}$, $\overline{\text{MRDY}}$, and $\overline{\text{MHOLD}}$ inactive (high) when it finishes using the read data. If no other masters are requesting the NuBus™, the controller parks on the bus, which is indicated by NMSTR remaining high (see Figure 2). The local board can issue another start cycle by simply taking $\overline{\text{NREQ}}$ low; it does not have to perform arbitration when the controller is parked on the bus. The controller remains parked on the bus until another master begins arbitrating for the bus. Refer to the section on NuBus™ cycles from the parked position for additional details.

master write cycles

When the local board wants to write data to another board connected to the NuBus™, it must first win mastership of the bus. Figure 3 shows the timing diagram of a typical master write cycle. The local board follows the same arbitration process as described in the master read cycle.

When the local board wins mastership of the bus, the controller signals the local board by driving NMSTR high. The controller immediately issues a start cycle (if $\overline{\text{MRDY}}$ is active) on the next driving edge by taking $\overline{\text{START}}$ low and placing the write address on the bus. At the end of the start cycle, the controller places the write data on the bus. The addressed slave responds to the write request by driving $\overline{\text{ACK}}$ low.

The controller signals the local board that the transfer is complete by driving Master Done (MDONE) active (high). The cycle is completed on the local board after $\overline{\text{NREQ}}$, $\overline{\text{MRDY}}$, and $\overline{\text{MHOLD}}$ return inactive. The same rules apply for parking on the bus as described in the master read cycle.

high-speed master read/write cycles

Figure 4 demonstrates a high-speed master read or master write cycle. The major difference between these cycles and the ones previously described is that $\overline{\text{MHOLD}}$ does not hold the controller after one master cycle. This feature allows the local board to generate additional start cycles quickly. This capability assumes that no other master has won ownership of the bus and the next transfer cycle (read or write) has not changed. If the transfer cycle has changed, the new transfer code must be latched into the 'ACT2440 by taking $\overline{\text{NREQ}}$ high for one clock cycle immediately after MDONE has been received.

If $\overline{\text{NREQ}}$ or $\overline{\text{MRDY}}$ are taken inactive (high) before the first sample clock edge after MDONE has been received, a new start cycle will not be automatically generated. Likewise, if $\overline{\text{MHOLD}}$ is taken active (low) before the first sample clock edge after $\overline{\text{ACK}}$ has been received, a new start cycle will not be automatically generated. The simplest form of interface ties $\overline{\text{MHOLD}}$ and $\overline{\text{MRDY}}$ in common with $\overline{\text{NREQ}}$, which guarantees that only one transfer cycle is generated every $\overline{\text{NREQ}}$ cycle. However, higher performance is achievable by using the above method.

When $\overline{\text{MHOLD}}$ is tied in common with $\overline{\text{NREQ}}$ and $\overline{\text{MRDY}}$, only one master cycle is generated. To generate another cycle, $\overline{\text{NREQ}}$, $\overline{\text{MRDY}}$, and $\overline{\text{MHOLD}}$ must be regenerated, which takes additional clock cycles. In the high-speed mode, the next start cycle is automatically generated. The advantage of this mode is that it produces faster read/write cycles. The disadvantage is that it shortens the time allowed for the local board to respond to read data and prepare for the next cycle.

master lock cycles

The 'ACT2440 is designed to support resource locking on the NuBus™. If the Master Lock Request input ($\overline{\text{MLREQ}}$) is taken active (low) when the NuBus™ Request input ($\overline{\text{NREQ}}$) is sampled, the controller issues an Attention Lock cycle after winning arbitration. An Attention Lock cycle warns all other modules connected to the bus that their local resources should be locked for the following transactions. The end of the locked sequence is signaled by an Attention Null cycle. The timing diagram in Figure 5 illustrates a typical locked sequence.

After the Attention Lock cycle is issued, normal NuBus™ master cycles can be performed. If the transfer type must be changed during a locked sequence, the new transfer code must be latched into the 'ACT2440 by taking NREQ high for one clock cycle, with $\overline{\text{MLREQ}}$ held low. The $\overline{\text{MLREQ}}$ input remains asserted for the entire lock tenure. The $\overline{\text{RQST}}$ output remains low for the entire lock cycle. When $\overline{\text{MLREQ}}$ is unasserted, the controller issues an Attention Null cycle. If no other masters are arbitrating for the bus, the controller parks on the NuBus™.

local resource conflict timing

In applications where the local circuitry can be both a master and a slave, conflicts for local resources may develop. For example, if the local circuitry starts the arbitration process as a master and loses to another master that in turn accesses the local circuit's slave resources, then the local circuitry must respond to the NuBus™ as a slave and immediately be ready to accomplish a master cycle.

The Master Ready input ($\overline{\text{MRDY}}$) provides a throttle mechanism to handle such situations. If this signal is inactive (high) when the master-state machine wins arbitration, the master-state machine freezes in the current state, maintaining all arbitration signals until $\overline{\text{MRDY}}$ is asserted low. The timing diagram in Figure 6 shows a situation where the local board has started arbitration as a master but loses to another master that is attempting to read or write data from the local resource.

The Slave External Request status output ($\overline{\text{SEREQ}}$) signals the local board that another master is accessing the local board. When the local board is ready to respond, it drives Slave Grant Access ($\overline{\text{SGNTA}}$) active (low), which enables data and/or address information to be placed onto the local board. When the local board is ready to respond, the Local Acknowledge input ($\overline{\text{LACK}}$) is driven active (low). This action causes the controller to issue an acknowledge cycle on the next driving clock edge. For additional details, refer to the section covering typical slave cycles.

When the local board finally wins the arbitration process, the NuBus™ Master Status signal (NMSTR) goes active (high). The local board responds by taking Master Ready ($\overline{\text{MRDY}}$) low, which causes the controller to execute a normal master read or master write cycle. In applications where the local board is only a master, $\overline{\text{MRDY}}$ can be tied in common with $\overline{\text{NREQ}}$ for simpler operation.

master timeout cycle

When Master Ready ($\overline{\text{MRDY}}$) is used to throttle the controller, a 16-state counter sets a maximum length of time that the controller will stay in the frozen state after winning arbitration. With $\overline{\text{NREQ}}$ low and $\overline{\text{MRDY}}$ high, this counter is enabled when the arbitration contest is won. When this timer reaches its maximum count (16), it forces the controller to issue a NuBus™ Attention Null cycle, which in turn signals all other masters on the bus to re-initiate arbitration. Figure 7 shows the timing diagram for the master timeout cycle.

On rare occasions, the local circuitry may give up on a NuBus™ request while still in the arbitration process. The controller detects this situation and issues a NuBus™ Attention Null cycle once it has won arbitration.

slave read/write cycles

The 'ACT2440 provides all the handshake signals required to facilitate a simple NuBus™ slave interface. In slave applications, the local board is either written to or read from. When a NuBus™ master wishes to access the local board as a slave, it places the slave's address on the bus during the start cycle. This action requires a compare function to identify when the NuBus™ address matches the 4-bit ID code associated with the local board. This function is provided in the 'BCT2420 or can be built using standard MSI comparator functions. The controller receives this input through the ID equal input ($\overline{IDEQ}$).

Figure 8 shows the timing diagram of a typical slave read cycle. Figure 9 shows the timing diagram for a typical slave write cycle. The Slave External Request status output ($\overline{SEREQ}$) signals that the local board is being accessed by another master. When the local board is ready to receive data and/or address information, it drives Slave Grant Access ($\overline{SGNTA}$) active (low). When the local board is ready to respond to a read or write request, it drives Local Acknowledge ($\overline{LACK}$) low. The controller then issues an acknowledge on the bus, which completes the transaction. Data and/or address information is enabled onto the local board as long as $\overline{SGNTA}$ is held low. $\overline{SEREQ}$ will not go inactive until the first sample edge after $\overline{SGNTA}$ goes inactive. Data and/or address information is disabled on the first sample edge after $\overline{SGNTA}$ returns inactive (high).

All slave external requests must be responded to with a local acknowledge. Allowing the NuBus™ to timeout will not reset the slave state machine.

higher performance slave cycles

Slave Grant Access ($\overline{SGNTA}$) and Local Acknowledge ($\overline{LACK}$) control the duration of slave cycles on the 'ACT2440. The simplest implementation, as previously explained, uses $\overline{SEREQ}$, $\overline{SGNTA}$, and $\overline{LACK}$ to form a simple handshake. Faster slave cycles are possible by taking $\overline{SGNTA}$ low before the first sample edge after $\overline{START}$, as shown in Figure 10. This mode of operation enables address and data information onto the local board on the first sample edge after $\overline{START}$. (Note: In slave-only applications, address information can be enabled onto the local board sooner by tying $\overline{AEN}$ low on the 'BCT2440's.) As previously described, $\overline{LACK}$ controls the completion of the slave cycle. Address and data information remains enabled onto the local board until $\overline{SGNTA}$ returns inactive.

If the Local Acknowledge ($\overline{LACK}$) and Slave Grant Access ($\overline{SGNTA}$) inputs are taken low before the first sample edge after $\overline{START}$, the Acknowlege output ($\overline{ACK}$) is generated on the next driving clock edge. This mode of operation offers the highest performance but places the greatest demand on local circuitry.

slave lock detection

NuBus™ Locked (NLOCK) is a special output provided on the 'ACT2440 that signals when the local board is being accessed by another master and an Attention Lock cycle has occurred. NLOCK informs the local board not to modify any of its local resources until an Attention Null cycle is received. Figure 11 shows the timing diagram for a slave lock-detection cycle. As shown in Figure 11, NLOCK goes active (high) when an Attention Lock cycle occurs on the bus and the local board is being requested by another master. NLOCK will remain high until the Attention Null cycle is received.

master block-transfer cycles

NuBus™ 1987 master block transfers are supported by the 'ACT2440. Figure 12 shows the timing diagram for a typical master block read. Figure 13 shows the timing diagram for a typical master block write.

A master block transfer consists of a start cycle, multiple data cycles to or from sequential address locations, and an acknowledge cycle. The master controls the number of data words transferred and communicates this information to the slave during the start cycle via address lines $\overline{AD5}$-$\overline{AD2}$. Table 2 shows the input code for master block-transfer cycles.

During master block transfers, the slave acknowledges intermediate data cycles via the $\overline{TM0}$ line. The 'ACT2440 detects these intermediate data cycles and generates the proper buffer control signals. The final data cycle, from the responding slave, is a standard acknowledge cycle.

Table 2. Master Block-Transfer Function Table

A5	A4	A3	A2	A1	A0	$\overline{LOCTM1}$	$\overline{LOCTM0}$	BLOCK SIZE	TYPE OF CYCLE
X	X	X	L	H	L	L	H	2	WRITE
X	X	L	H	H	L	L	H	4	WRITE
X	L	H	H	H	L	L	H	8	WRITE
L	H	H	H	H	L	L	H	16	WRITE
X	X	X	L	H	L	H	H	2	READ
X	X	L	H	H	L	H	H	4	READ
X	L	H	H	H	L	H	H	8	READ
L	H	H	H	H	L	H	H	16	READ

slave block-transfer cycles

The 'ACT2440 can support slave block-transfer cycles with the addition of the 'ALS2442. The first responsibility of a slave during block transfers is to determine the type and size of the block transfer. This information is provided by the requesting master and must be decoded from the TMx lines and the A5-A0 address lines (as provided by the 'ACT2420s). See Table 3 for additional details.

The Slave Interim Acknowledge input ($\overline{SIACK}$) generates the interim acknowledge cycles via $\overline{TM0}$. The Slave External Request output ($\overline{SEREQ}$) signals the local board when an interim acknowledge has occurred on the bus.

Figure 14 shows the timing diagram of a typical slave block read. Figure 15 shows the timing diagram of a typical slave block write. The beginning of these cycles looks like any other slave cycle; $\overline{SEREQ}$ goes active (low), signaling the local board that another master is requesting the local board. On the first sample edge after $\overline{SGNTA}$ is taken active (low), the $\overline{AEN}$ buffer signal is driven low, enabling the NuBus™ addresses onto the local board. The A0, A1, and TMx lines must be decoded as provided on the 'ALS2442 in order to generate a block-transfer signal (represented on the timing diagrams as BLOCK). When this signal goes active (high), it signals the local board that a block transfer has been requested. Decoding A5-A2 determines the number of words to be transferred. The final acknowledge cycle is generated by driving $\overline{LACK}$ low.

Table 3. Slave Block-Transfer Decode Table

A5	A4	A3	A2	A1	A0	NTM1	NTM0	BLOCK SIZE	TYPE OF CYCLE
X	X	X	L	H	L	H	L	2	WRITE
X	X	L	H	H	L	H	L	4	WRITE
X	L	H	H	H	L	H	L	8	WRITE
L	H	H	H	H	L	H	L	16	WRITE
X	X	X	L	H	L	L	L	2	READ
X	X	L	H	H	L	L	L	4	READ
X	L	H	H	H	L	L	L	8	READ
L	H	H	H	H	L	L	L	16	READ

maximum block-transfer performance

As a master, the 'ACT2440 is capable of supporting the maximum block transfer rate of 37.6M-bytes/second (one start cycle followed by 16 consecutive 100 ns data cycles). Figure 12 shows a more typical situation where the slave controls the block transfer rate via the intermediate acknowledge signal ($\overline{TM0}$). Note that the 'ACT2440 will generate a data clock (DCLK) every clock cycle that $\overline{TM0}$ is low. The final data cycle is a normal acknowledge cycle.

In slave block transfer mode, the 'ACT2440 has been designed to provide a simple handshake between the slave interum acknowledge ($\overline{SIACK}$) input and the slave external request ($\overline{SEREQ}$) output as shown in Figure 15. Note that each data clock (DCLK) cycle goes high for 100 ns as a result of the simple handshake

between $\overline{\text{SIACK}}$ and $\overline{\text{SEREQ}}$. In this simpler mode of operation, the maximum intermediate data transfer rate when using the 'ACT2441 is 200 ns, which equates to approximately 20M-bytes/second.

NuBus™ Cycles from the Parked Position

As long as $\overline{\text{RQST}}$ remains unasserted, the bus owner is considered to be "parked" on the bus, and may continue to use the bus without the necessity of going through an arbitration contest in which it is the only contender. The ANSI/IEEE 1196-1987 specification requires that as soon as another module drives the $\overline{\text{RQST}}$ line asserted, an arbitration contest is started and the present bus owner (currently parked on the bus) must not begin another transaction. The concept of bus parking reduces the average time needed to acquire the bus in systems with a small number of active contenders.

When using the 'ACT2440 NuBus™ controller from a parked position, the local board does not know if it remains the NuBus™ master and begins another transaction until the $\overline{\text{START}}$ signal has been generated. In other words, just because the local board has taken $\overline{\text{MRDY}}$ and $\overline{\text{NREQ}}$ active (low), does not mean the 'ACT2440 continues to own the bus and has generated a $\overline{\text{START}}$ cycle.

When the 'ACT2440 is in the parked position (NMSTR high) and no other masters are requesting the bus, a start cycle will be generated on the driving edge after $\overline{\text{NREQ}}$ and $\overline{\text{MRDY}}$ are taken active (low).

Figure 16 shows a situation where an old NuBus™ master is initially parked on the bus and is attempting to issue another $\overline{\text{START}}$ cycle (by taking $\overline{\text{MRDY}}$ low); but loses to a new master who is attempting to access data from resources that are available on the old master's board. In other words, the new master will win the bus and is trying to use the old master as a slave. This situation is similar to the local resource conflict timing diagram shown in Figure 6.

In Figure 16, the old master learns that it has lost the bus by detecting that NMSTR has gone inactive (low) during the start cycle. The new master, which has just won the bus and has generated a start cycle, is attempting to access data from the old master. The Slave External Request ($\overline{\text{SEREQ}}$) output on the old master will detect this access request by going active (low) on the first sample edge after the start cycle. At this time, the old master may want to take $\overline{\text{MRDY}}$ back to the inactive level (as shown in Figure 16) so that it will have control of the $\overline{\text{START}}$ signal after winning back the bus. If $\overline{\text{MRDY}}$ is not taken back to the inactive level (high) after losing the bus, then the 'ACT2440 will immediately issue a start cycle after the acknowledge cycle has been generated.

If the new master was directing the access cycle at a different slave, then the $\overline{\text{SEREQ}}$ output on the old master would remain inactive (high) and the $\overline{\text{MRDY}}$ input on the old master can be kept low in order to generate a start cycle as soon as the old master wins back the bus.

Notice from the timing diagram that if the old master takes $\overline{\text{MRDY}}$ low at the same time or in the following cycle, then the old master will lose to the new master.

If the old master takes $\overline{\text{MRDY}}$ low on the cycle before the new master takes $\overline{\text{RQST}}$ low, then the old master will retain the bus and complete its cycle.

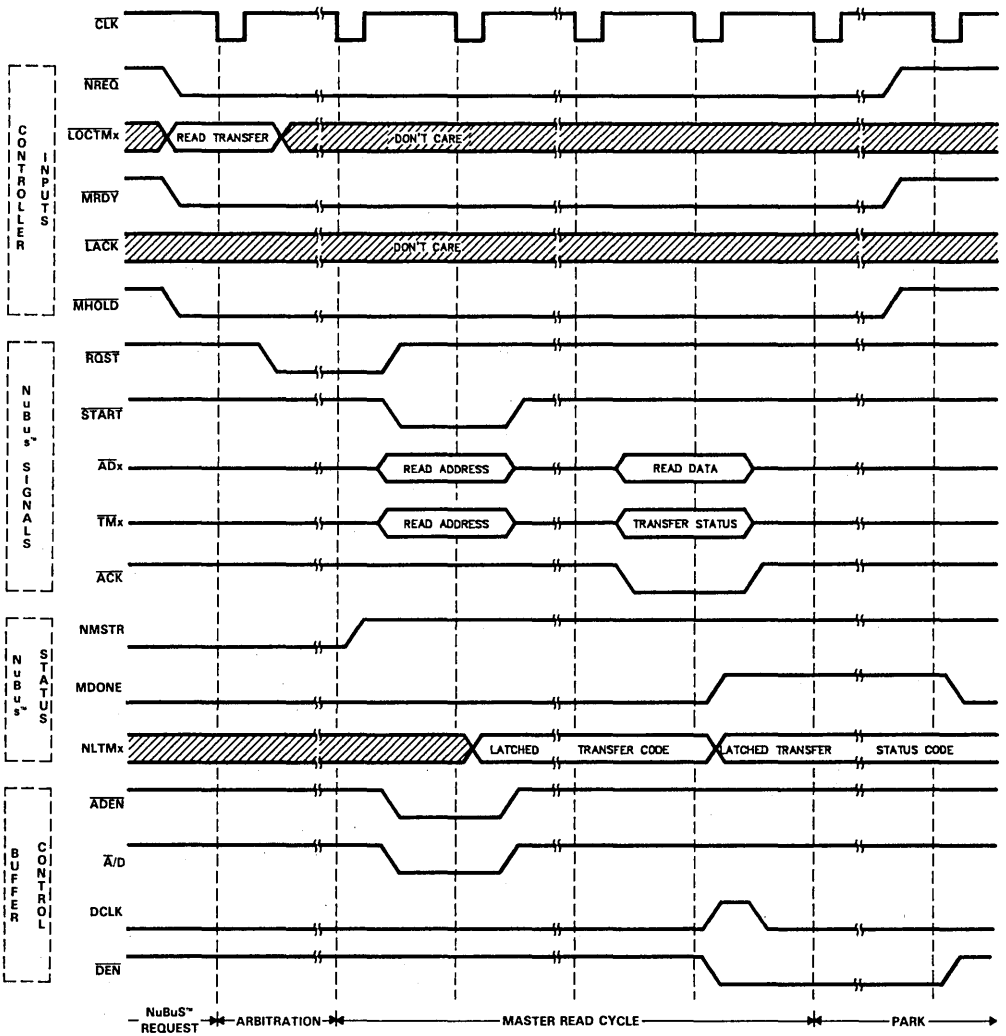

FIGURE 2. TYPICAL MASTER READ CYCLE

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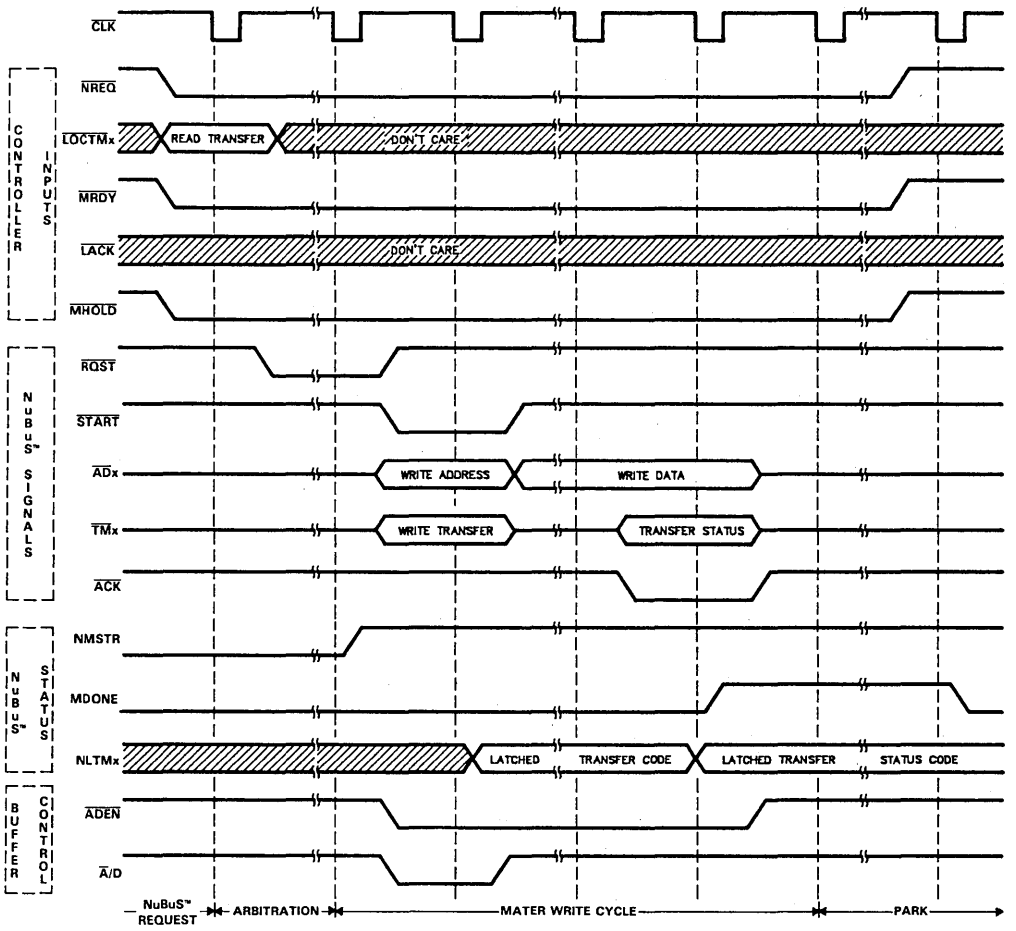

FIGURE 3. TYPICAL MASTER WRITE CYCLE

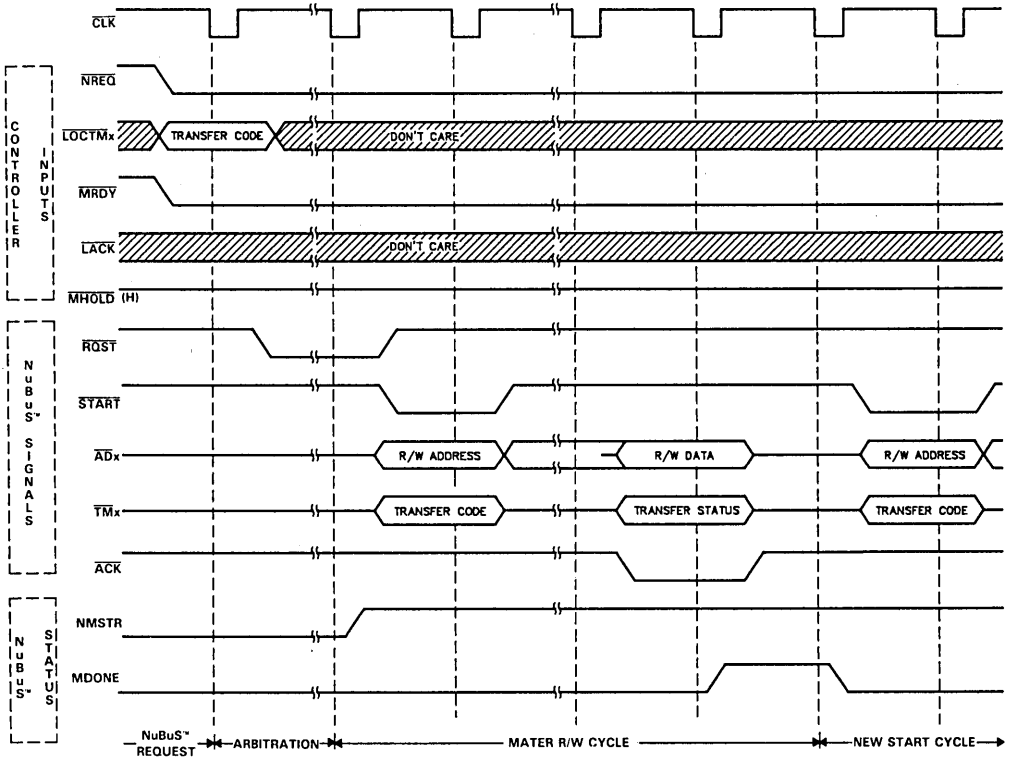

FIGURE 4. HIGH-SPEED MASTER READ/WRITE CYCLES (MHOLD LOGIC NOT USED)

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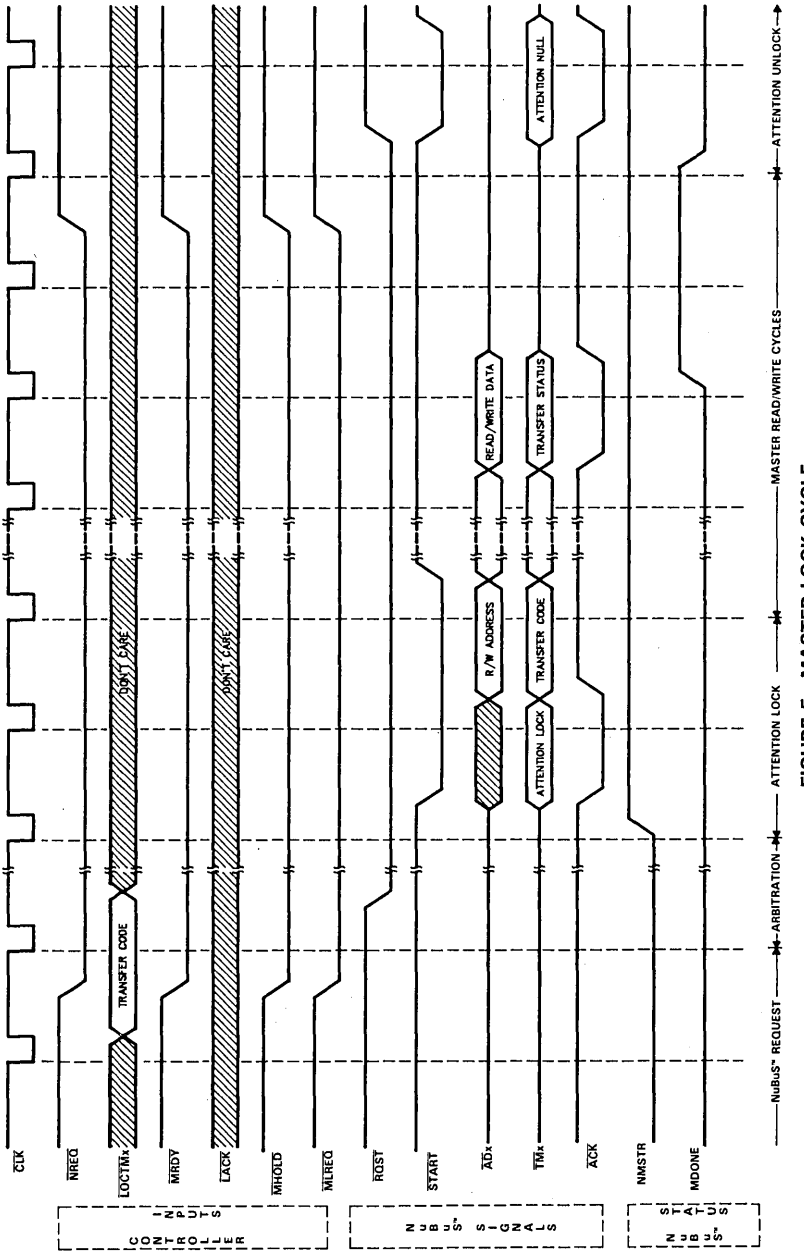

FIGURE 5. MASTER LOCK CYCLE

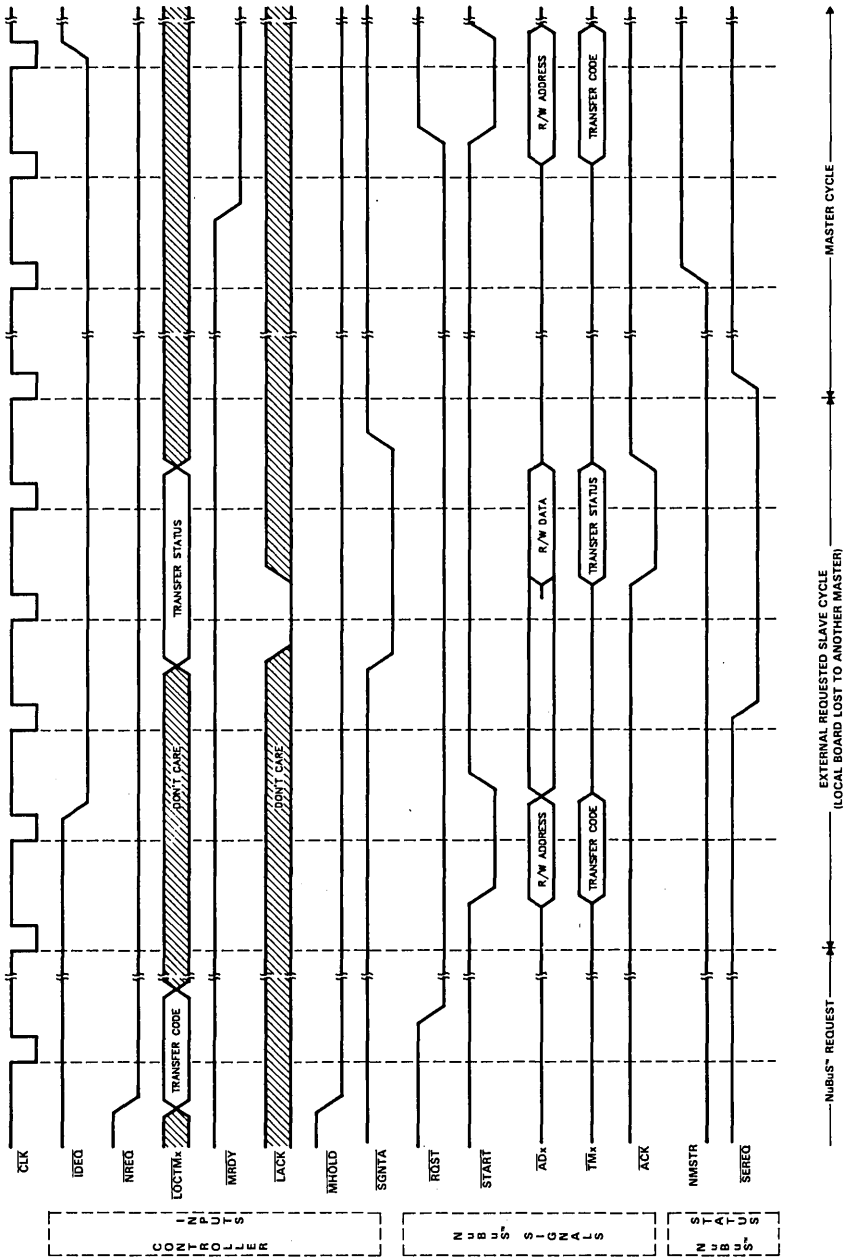

FIGURE 6. LOCAL RESOURCE CONFLICT TIMING

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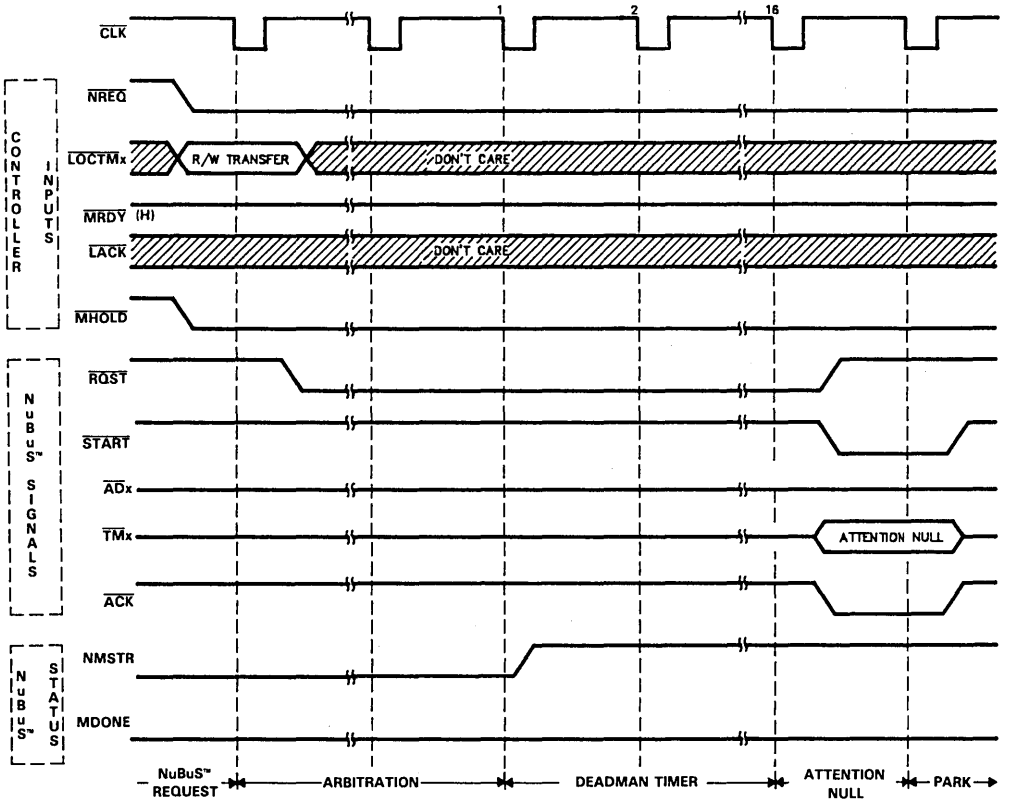

FIGURE 7. MASTER TIMEOUT CYCLE

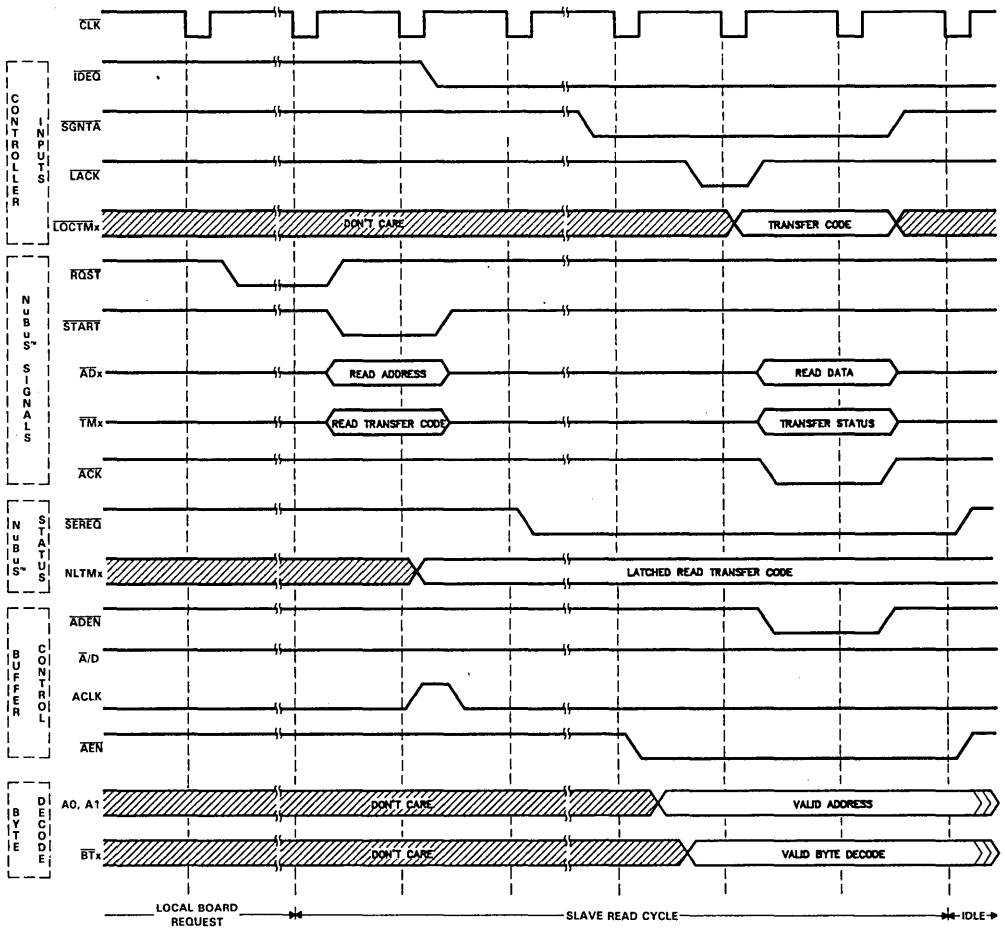

FIGURE 8. TYPICAL SLAVE READ CYCLE

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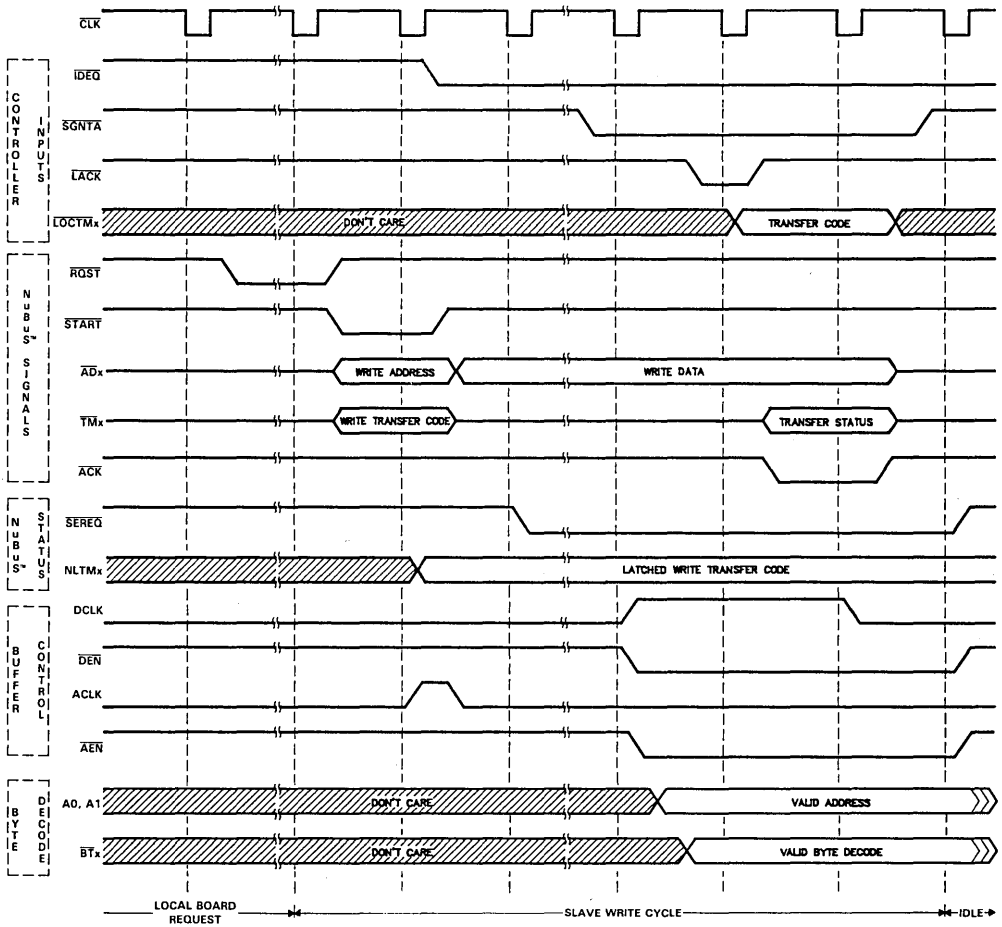

FIGURE 9. TYPICAL SLAVE WRITE CYCLE

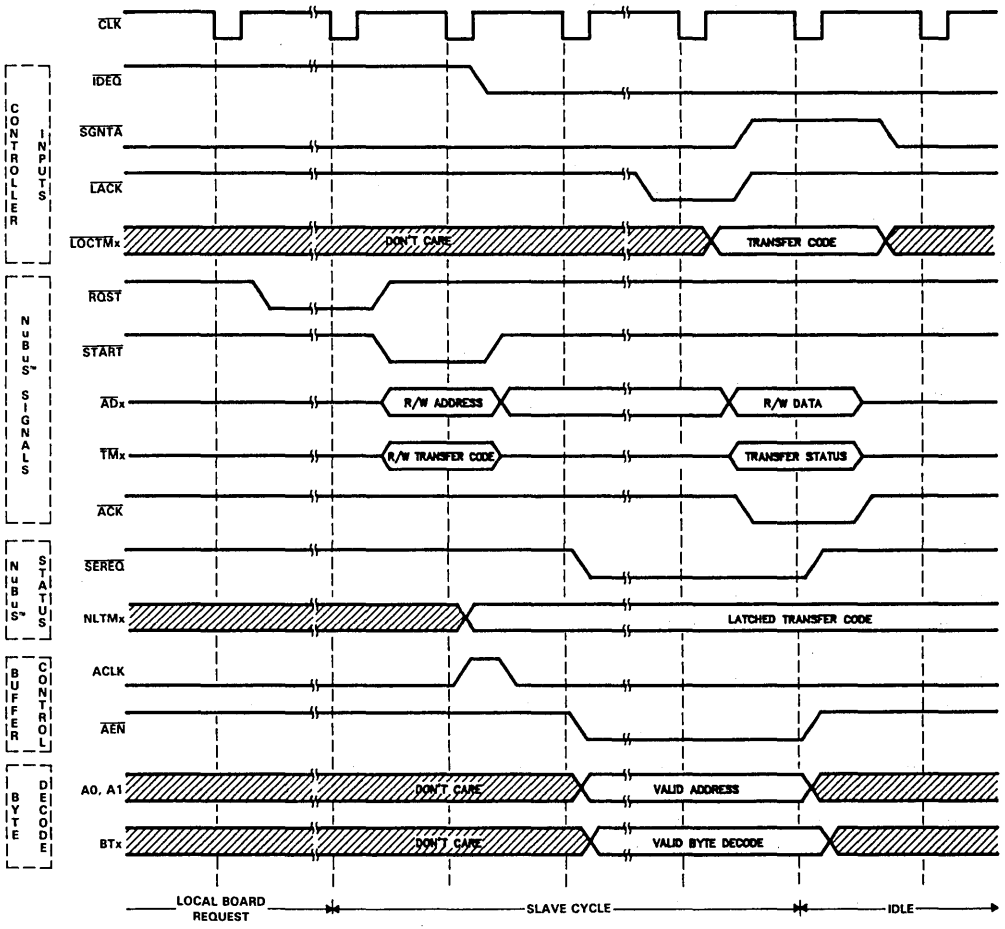

FIGURE 10. HIGHER-PERFORMANCE SLAVE CYCLES

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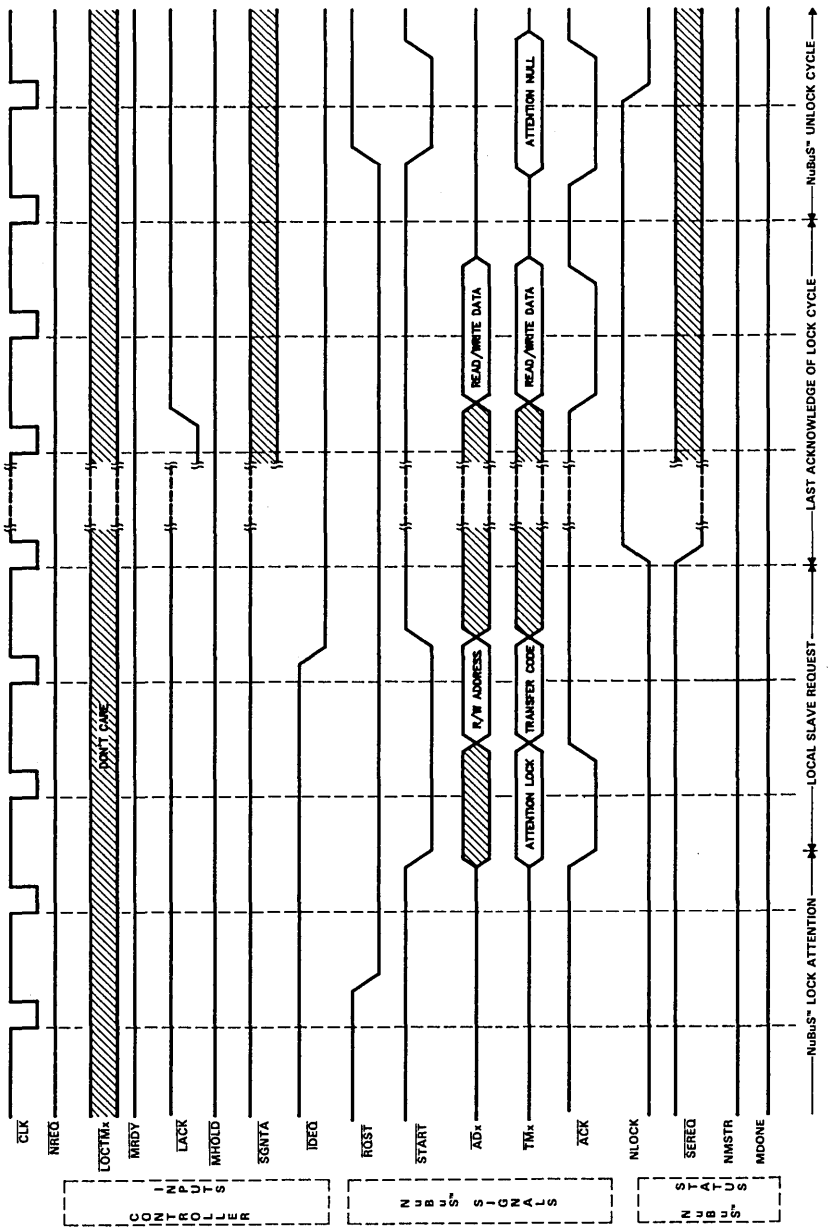


FIGURE 11. SLAVE LOCK-DETECTION CYCLE

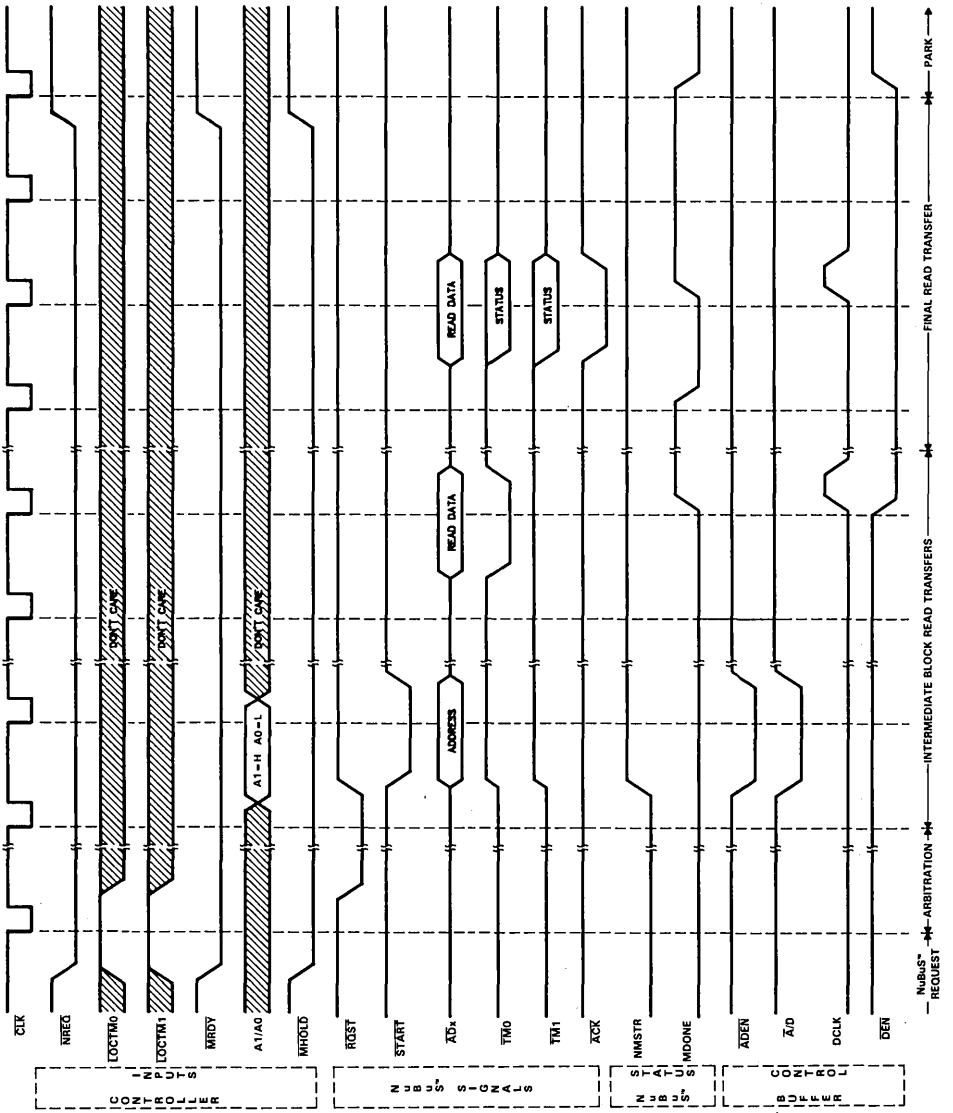


FIGURE 12. MASTER BLOCK-READ TRANSFER CYCLE

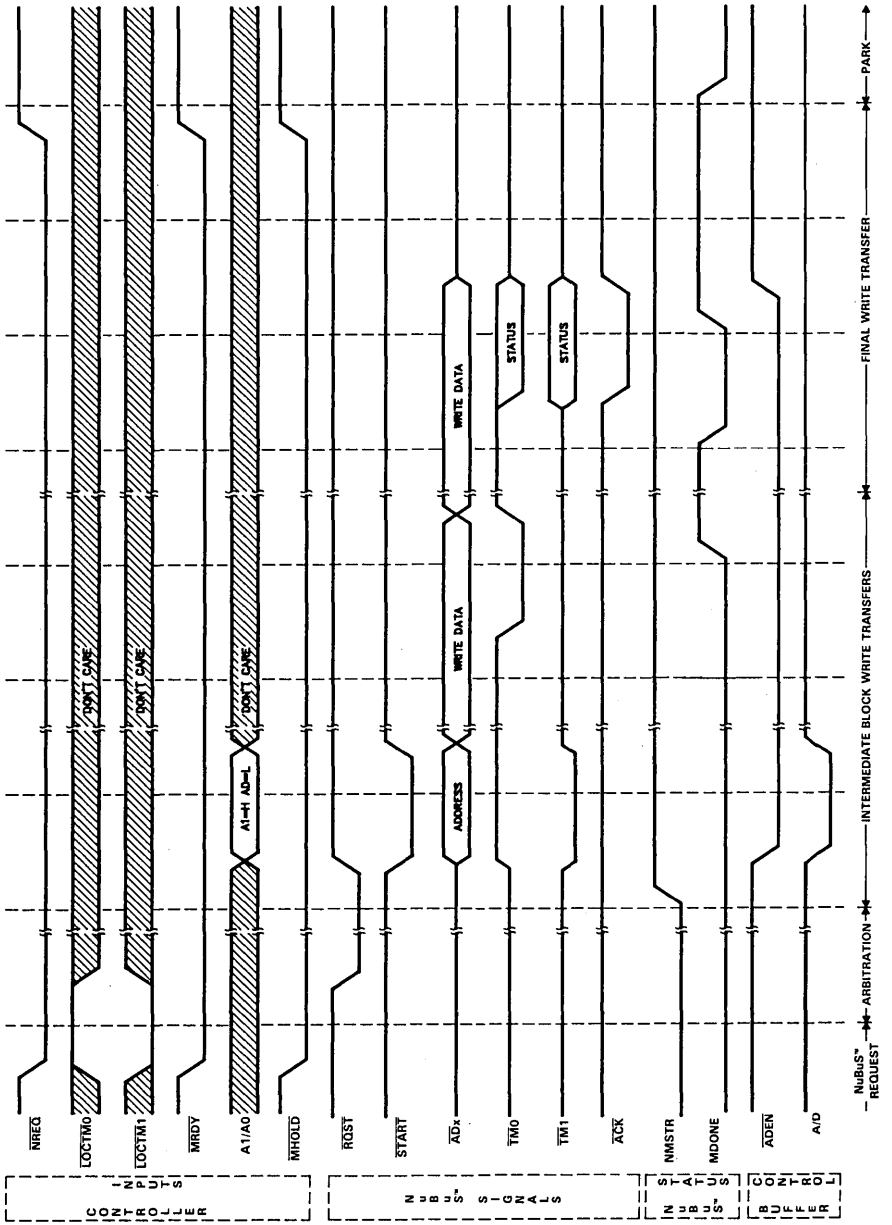
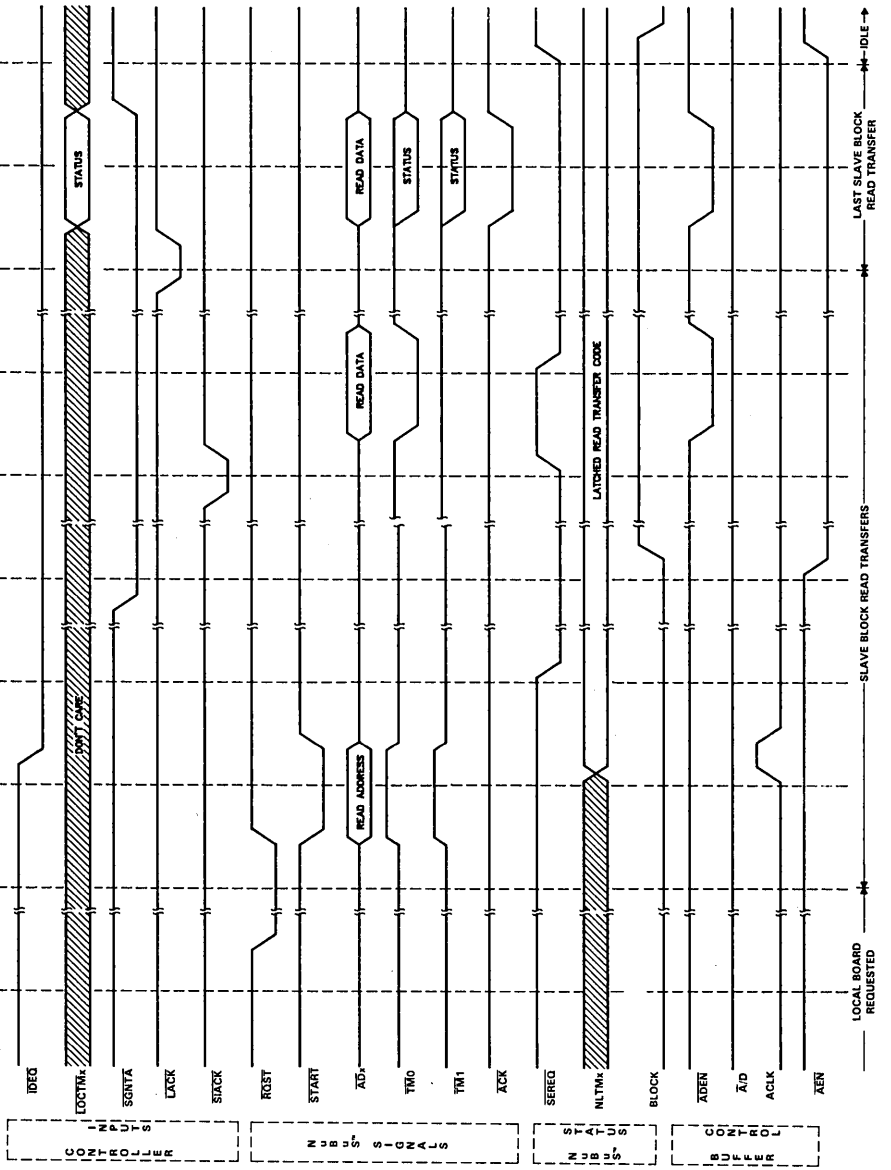


FIGURE 13. MASTER BLOCK-WRITE CYCLE



†The BLOCK signal must be supplied by external logic, such as from TI's SN74ALS2442.

FIGURE 14. SLAVE BLOCK-READ TRANSFER CYCLE

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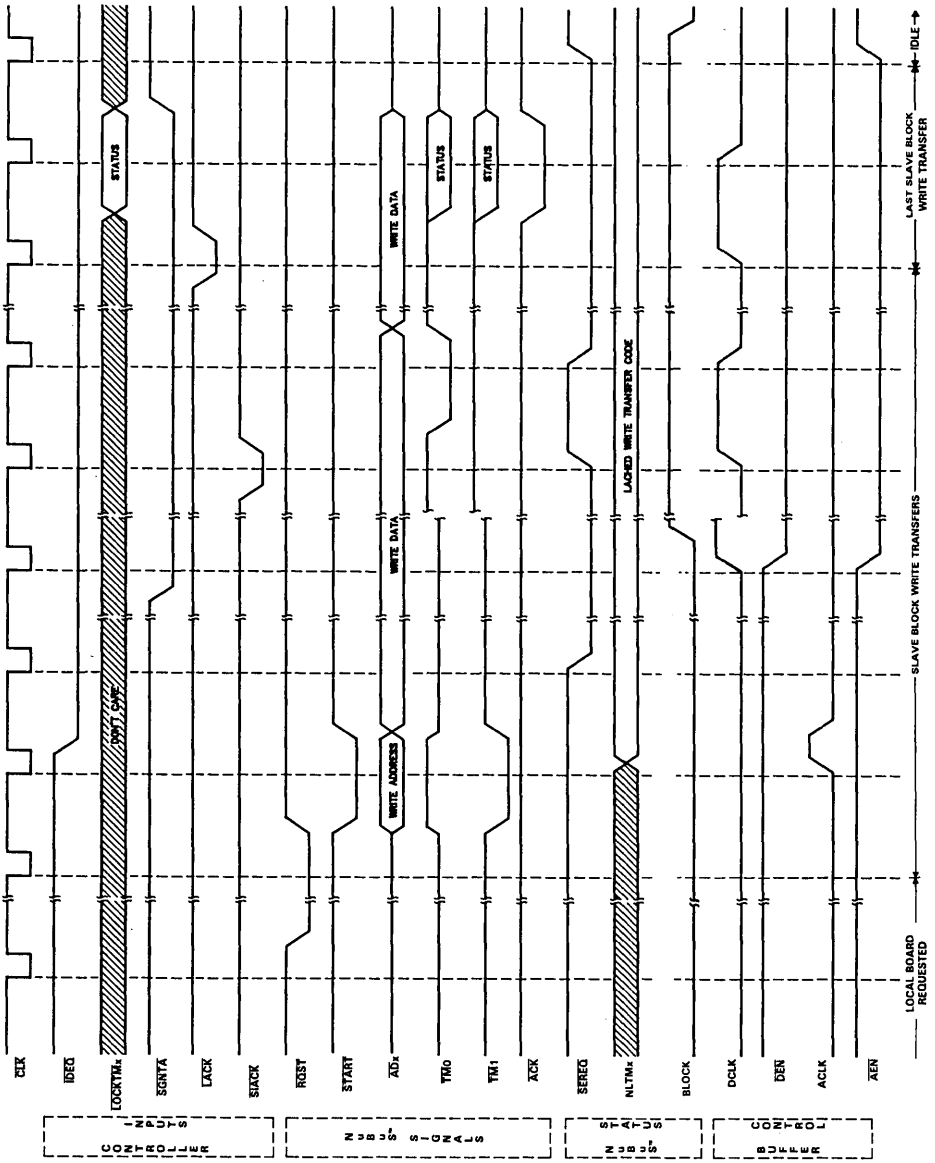

†The BLOCK signal must be supplied by external logic, such as from TI's SN74ALS2442.

FIGURE 15. SLAVE BLOCK-WRITE TRANSFER CYCLE

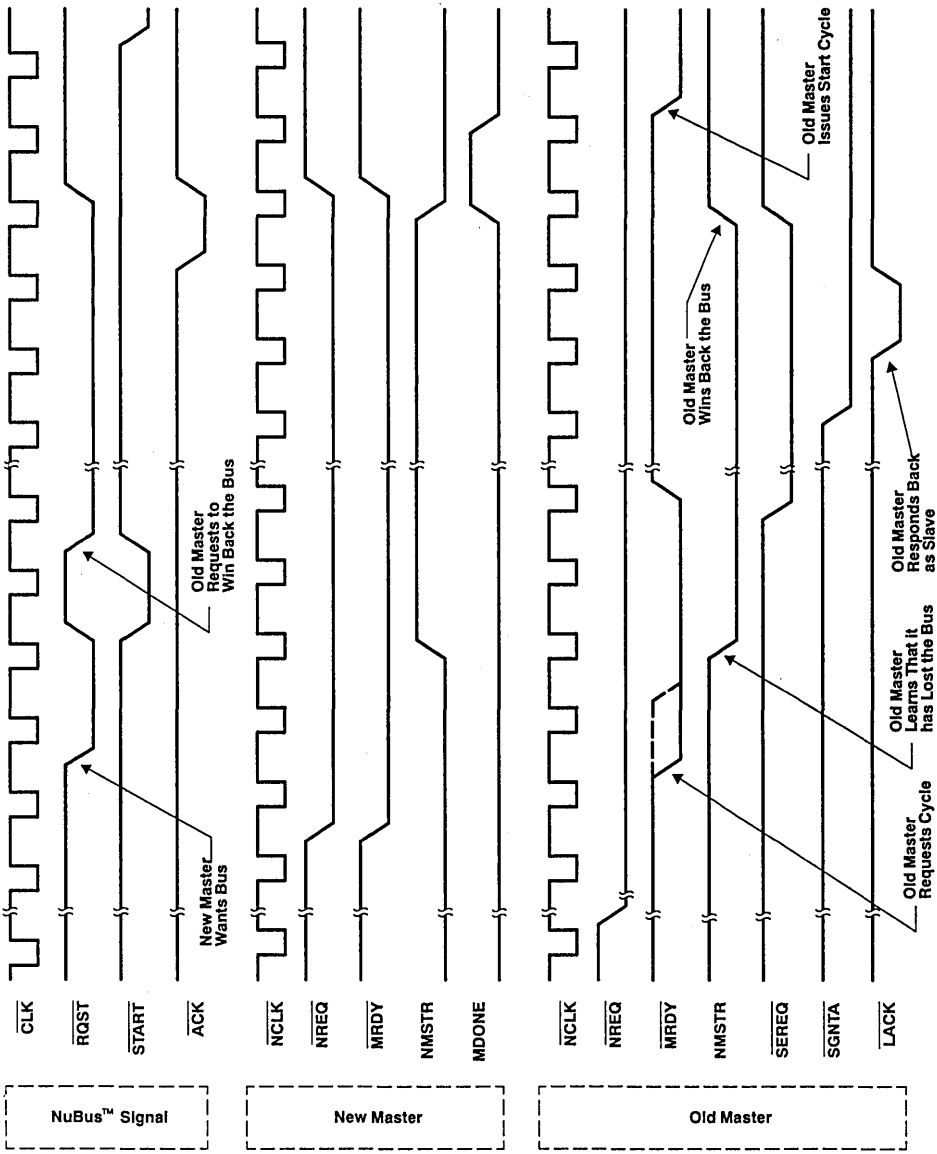

FIGURE 16. NuBus™ CYCLES FROM THE PARKED POSITION

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.5 to 7 V
Input voltage range, any input . . . . . −0.5 to 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 1: All voltage values are with respect to GND.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Status, buffer, and byte decode			−2	mA
		NuBus™ 3-state outputs			−1.6	
I_{OL}	Low-level output current	Status, buffer, and byte decode			6	mA
		NuBus™ 3-state outputs			24	
		NuBus™ open-collector outputs			80	
f_{clock}	Clock frequency		0		10	MHz
t_w	Pulse duration	$\overline{CLK}$ low	23			ns
		$\overline{CLK}$ high	73			
t_{su}	Setup time before $\overline{CLK}\downarrow$	$\overline{NREQ}$	15			ns
		$\overline{LOCTM}$x valid	15			
		$\overline{LACK}$	15			
		$\overline{MLREQ}$ and $\overline{NREQ}$ low	15			
		$\overline{MRDY}$ low	15			
		$\overline{SGNTA}$ low	15			
		$\overline{IDEQ}$ low	15			
		$\overline{SIACK}$ low	15			
t_h	Hold time after $\overline{CLK}\downarrow$	$\overline{NREQ}$ low	10			ns
		$\overline{LOCTM}$x valid	10			
		$\overline{SIACK}$ low	10			
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	Status, buffer, and byte decode	I_{OH} = 2 mA,	V_{CC} = 4.5 V	3	3.7		V
		NuBus™ 3-state outputs	I_{OH} = 1.6 mA,	V_{CC} = 4.5 V	3	3.7		
V_{OL}	Low-level output voltage	Status, buffer, and byte decode	I_{OL} = 6 mA,	V_{CC} = 4.5 V		0.3	0.4	V
		NuBus™ 3-state outputs	I_{OL} = 24 mA,	V_{CC} = 4.5 V		0.35	0.5	
		NuBus™ open drain	I_{OL} = 80 mA,	V_{CC} = 4.5 V		0.35	0.5	
I_{OZH}	High-impedance state output current		V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}	High-impedance state output current		V_{CC} = 5.5 V,	V_O = 0.4 V			20	μA
I_{IH}	High-level input current		V_{CC} = 5.5 V,	V_I = 5.5 V			20	μA
I_{IL}	Low-level input current	ID3-ID0	V_{CC} = 5.5 V,	V_I = 0			−750	μA
		All other inputs					−10	
I_{OS}	Short-circuit output current‡		V_O = 0,	V_{CC} = 5.5 V	−15		−225	mA
I_1	Active supply current		V_{CC} = 5.5 V, f_{clk} = 10 MHz	All inputs active,		6	15	mA
I_2	Average standby current		V_{CC} = 5.5 V, All inputs at V_{IL} or V_{IH}, f_{clk} = 10 MHz			2	5	mA
C_i	Input capacitance		V_I = 0 V,	f = 10 MHz		5		pF
C_o	Output capacitance		V_O = 0 V,	f = 1 MHz		10		pF

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡No more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	MIN	TYP	MAX	UNIT
f_{max}	Clock frequency, $\overline{CLK}$	10			MHz

NuBus™ card-slot signals, C_L = 300 pF†

	PARAMETER	LOAD	MIN	TYP‡	MAX	UNIT
t_{pd}	Propagation delay time, $\overline{CLK}$↑ to $\overline{START}$	R1 = 270 Ω, R2 = 470 Ω		20	32	ns
t_{pd}	Propagation delay time, $\overline{CLK}$↑ to $\overline{ACK}$	R1 = 270 Ω, R2 = 470 Ω		20	32	ns
t_{pd}	Propagation delay time, $\overline{CLK}$↑ to $\overline{TM}$x	R1 = 270 Ω, R2 = 470 Ω		20	32	ns
t_{pd}	Enable time, $\overline{NMREQ}$ to $\overline{NMRQ}$	R1 = 270 Ω, R2 = 470 Ω		20	32	ns
t_{en}	Enable time, $\overline{CLK}$↑ to $\overline{RQST}$	R1 = 91 Ω, R2 = 220 Ω		18	32	ns
t_{en}	Enable time, $\overline{CLK}$↑ to $\overline{START}$	R1 = 270 Ω, R2 = 470 Ω		18	32	ns
t_{en}	Enable time, $\overline{CLK}$↑ to $\overline{ACK}$	R1 = 270 Ω, R2 = 470 Ω		18	32	ns
t_{en}	Enable time, $\overline{CLK}$↑ to $\overline{TM}$x	R1 = 270 Ω, R2 = 470 Ω		18	32	ns
t_{en}	Enable time, $\overline{CLK}$↓ to $\overline{ARB}$x	R1 = 91 Ω, R2 = 220 Ω		20	35	ns
t_{en}	Enable time, $\overline{CLK}$↑ to $\overline{SPV}$	R1 = 270 Ω, R2 = 470 Ω		23	43	ns

NuBus™ card-slot signals, C_L = 50 pF†

	PARAMETER	LOAD	MIN	TYP‡	MAX	UNIT
t_{dis}	Disable time, $\overline{CLK}$↑ to $\overline{RQST}$	R1 = 91 Ω, R2 = 220 Ω		13	20	ns
t_{dis}	Disable time, $\overline{CLK}$↑ to $\overline{START}$	R1 = 270 Ω, R2 = 470 Ω		12	22	ns
t_{dis}	Disable time, $\overline{CLK}$↑ to $\overline{ACK}$	R1 = 270 Ω, R2 = 470 Ω		10	18	ns
t_{dis}	Disable time, $\overline{CLK}$↑ to $\overline{TM}$x	R1 = 270 Ω, R2 = 470 Ω		10	18	ns
t_{dis}	Disable time, $\overline{CLK}$↓ to $\overline{ARB}$x	R1 = 91 Ω, R2 = 220 Ω		13	24	ns
t_{dis}	Disable time, $\overline{CLK}$↑ to $\overline{SPV}$	R1 = 270 Ω, R2 = 470 Ω		10	18	ns

†See Parameter Measurement Information for load circuit and voltage waveforms.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

NuBus™ status signals, C_L = 50 pF†

	PARAMETER	LOAD	MIN	TYP‡	MAX	UNIT
t_{pd}	Propagation delay time, $\overline{CLK}$↓ to NMSTR	R_L = 500 Ω		13	21	ns
t_{pd}	Propagation delay time, $\overline{CLK}$↓ to MDONE	R_L = 500 Ω		13	21	ns
t_{pd}	Propagation delay time, $\overline{CLK}$↓ to $\overline{SEREQ}$	R_L = 500 Ω		13	21	ns
t_{pd}	Propagation delay time, $\overline{CLK}$↓ to NLTMx	R_L = 500 Ω		16	25	ns
t_{pd}	Propagation delay time, $\overline{CLK}$↓ to $\overline{NLRST}$	R_L = 500 Ω		11	21	ns
t_{pd}	Propagation delay time, $\overline{CLK}$↓ to NLOCK	R_L = 500 Ω		11	21	ns
t_{pd}	Propagation delay time, $\overline{CLK}$ to NCLK	R_L = 500 Ω		9	16	ns
t_{pd}	Propagation delay time, $\overline{CLK}$ to $\overline{NCLK}$	R_L = 500 Ω		10	18	ns
t_{pd}	Propagation delay time, $\overline{START}$ to NSTART	R_L = 500 Ω		8	14	ns
t_{pd}	Propagation delay time, $\overline{ACK}$ to NACK	R_L = 500 Ω		8	14	ns
t_{pd}	Propagation delay time, $\overline{TM}$x to NTMx	R_L = 500 Ω		8	14	ns

NuBus™ buffer, C_L = 50 pF†

	PARAMETER	LOAD	MIN	TYP‡	MAX	UNIT
t_{pd}	Propagation delay time, $\overline{CLK}$↓ to ACLK high	R_L = 500 Ω		12	20	ns
t_{pd}	Propagation delay time, $\overline{CLK}$↑ to ACLK low	R_L = 500 Ω		13	20	ns
t_{pd}	Propagation delay time, $\overline{CLK}$↓ to $\overline{AEN}$	R_L = 500 Ω		13	20	ns
t_{pd}	Propagation delay time, $\overline{CLK}$↓ to DCLK high	R_L = 500 Ω		12	20	ns
t_{pd}	Propagation delay time, $\overline{CLK}$↑ to DCLK low	R_L = 500 Ω		14	22	ns
t_{pd}	Propagation delay time, $\overline{CLK}$↓ to $\overline{DEN}$	R_L = 500 Ω		14	22	ns
t_{pd}	Propagation delay time, $\overline{CLK}$↑ to $\overline{ADEN}$	R_L = 500 Ω		9	14	ns
t_{pd}	Propagation delay time, $\overline{CLK}$↑ to $\overline{A/D}$	R_L = 500 Ω		9	14	ns

byte decode signals, C_L = 50 pF†

	PARAMETER	LOAD	MIN	TYP‡	MAX	UNIT
t_{pd}	Propagation delay time, A0, A1 to $\overline{BT}$x	R_L = 500 Ω		17	28	ns

propagation delay relationships, C_L = 50 pF†

	PARAMETER	LOAD	MIN	MAX	UNIT
t_{pd}§	Propagation delay time, MDONE, NLOCK, NMSTR, $\overline{SEREQ}$, $\overline{NLRST}$ before $\overline{NCLK}$↑	R_L = 500 Ω	15		ns
t_{pd}§	Propagation delay time, NLTM0, NLTM1 before $\overline{NCLK}$↑	R_L = 500 Ω	10		ns
t_{pd}¶	Propagation delay time NSTART, NACK, NTM0, NTM1 after $\overline{NCLK}$↑	R_L = 500 Ω	5		ns

†See Parameter Measurement Information for load circuit and voltage waveforms.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The propagation delay minimums ensure that the status signals generated by the 'ACT2440 from the NuBus clock signal ($\overline{CLK}$) will be valid before the rising edge of $\overline{NCLK}$.
¶This specification assumes the $\overline{START}$, $\overline{ACK}$, $\overline{TM0}$ and $\overline{TM1}$ NuBus signals have been generated by the 'ACT2440. During SLAVE cycles, this relationship is a function of the other MASTER driving these input signals.

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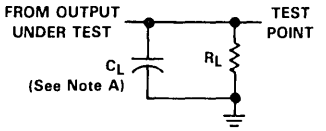
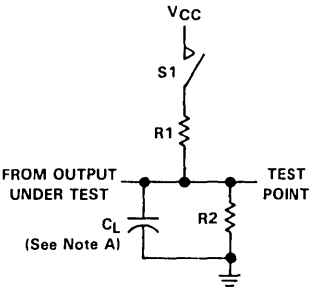
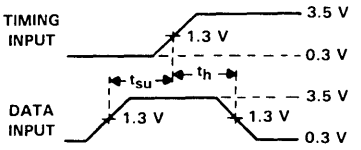
PARAMETER MEASUREMENT INFORMATION



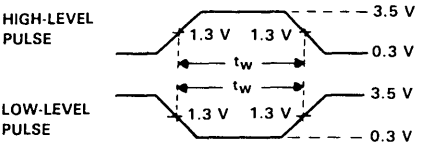
LOAD CIRCUIT FOR
NuBus™ STATUS, BUFFER, AND
BYTE DECODE



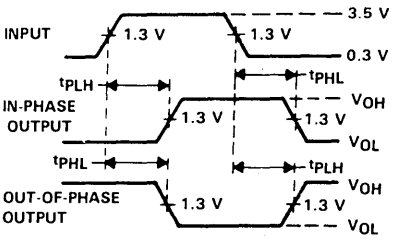
LOAD CIRCUIT FOR
NuBus™ INTERFACE



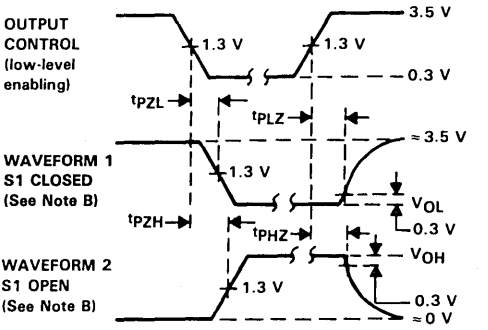
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

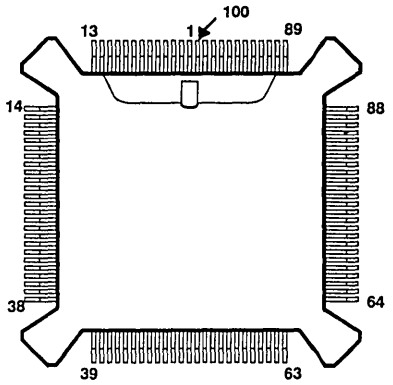
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%
D. The outputs are measured one at a time with one transition per measurement.

FIGURE 17

D3415, MARCH 1990–REVISED JANUARY 1991

- **Designed for Apple Computer Macintosh Coprocessor Platform Interface Applications**
- **Supports 16/8-Bit Master and 32/16/8-Bit Slave NuBus™ Applications for the Apple Computer Macintosh II Family of Computers**
- **Designed to Operate with the SN74BCT2425 NuBus™ Address/Data Transceivers and Registers**
- **May Be Used for Both Intelligent and Nonintelligent NuBus™ Card Designs**
- **Fully TTL Compatible**
- **Dependable Texas Instruments Quality and Reliability**

PQ PACKAGE
(TOP VIEW)



description

The Texas Instruments SN74ACT2441 Macintosh Coprocessor Platform (MCP) NuBus™ Controller provides 16/8-bit NuBus™ Master and 32/16/8-bit Slave signaling protocol in compliance with NuBus™ interfacing specifications supported by Apple Computer for the Macintosh II computer family (For a complete description of the Apple Macintosh NuBus™ implementation, see *Designing Cards and Drivers for Macintosh II and Macintosh SE* by Addison Wesley. Certain features of the NuBus™ architecture are not implemented in the Macintosh II, as noted in this reference manual).

Beyond the NuBus™ interface, the 'ACT2441 features a Motorola MC68000 processor interface, DRAM control, refresh, and multimaster bus arbitration. Other features include a programmable timer and DTACK/VPA generation. Finally, the 'ACT2441 conforms to the hardware requirements of the Apple Computer "Macintosh Coprocessor Platform" (MCP) architecture and the needs of the Macintosh "Apple Real-Time Operating System Environment" (A/ROSE). Using the 'ACT2441 reduces the hardware control functions into a single device and provides the services needed by the A/ROSE software interface.

Macintosh coprocessor platform

The Macintosh Coprocessor Platform is a hardware/software platform, developed by Apple Computer, which may be used as a framework for developing intelligent or nonintelligent NuBus™ I/O cards for the Macintosh II family of computers. The complete MCP platform defines an intelligent NuBus™ hardware interface along with the A/ROSE software (A/ROSE runs on the NuBus™ MCP card while A/ROSE PREP runs on the host Macintosh II computer). Hardware support is included for a MC68000 processor, an application-specific I/O processor, DRAM refresh, and many other functions.

A/ROSE is an operating system that is downloaded onto a Macintosh II I/O card for execution by an on-board MC68000 processor. A/ROSE PREP is a driver installed within the Macintosh II computer for communication with A/ROSE. The specifics of the Apple MCP architecture and the A/ROSE operating system may be obtained by companies enrolled in the Apple Computer Partners program directly from Apple Computer Developer Services.

Features such as the MC68000 or DRAM may be omitted from the I/O card and the NuBus™ interface can still be used for nonintelligent cards or cards whose intelligence is derived solely from an on-board application-specific processor.

NuBus is trademark of Texas Instruments Incorporated.

Macintosh coprocessor platform (continued)

The MCP hardware control portion of the device provides for a multimaster interface capability on the local Macintosh II NuBus™ expansion card with one of three devices assuming the master role on the local 16-bit MC68000 style local bus of the I/O card. The three masters allowed are the NuBus™ channel, the MC68000 processor onboard the I/O card, and a third bus master consisting of an application-specific I/O processor using MC68000 style bus arbitration.

In addition to bus master control functions, the 'ACT2441 provides zero-wait-state access to 120-ns DRAMs, $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ DRAM refresh, a programmable timer, programmable DTACK generation, and general-purpose I/O. Use of Texas Instruments SN74ACT2441 controller simplifies interfacing to the NuBus™ ADx lines (hereinafter "NuBus™") while providing a 16-bit, high-performance interface between NuBus™, a 16-bit local processor bus, local DRAM, and an intelligent I/O processor, all of which can reside on a single NuBus™ expansion card.

NuBus™ specification ordering and licensing requirements

A complete description of the Apple Macintosh NuBus™ implementation is described in *Designing Cards and Drivers for Macintosh II and Macintosh SE* by Addison Wesley,

The Institute of Electrical and Electronics Engineers (IEEE) standard, IEEE 1196, NuBus™-A Simple 32-Bit Backplane Bus, may be ordered from:

The Institute of Electrical and Electronics Engineers
345 East 47 Street
New York, NY 10017

Texas Instruments owns patents on the NuBus™. Those wishing to make devices that interface with NuBus™ machines need to obtain a NuBus™ license directly from Texas Instruments. Please contact Texas Instruments at the following address for more information.

Texas Instruments Incorporated
12501 Research Blvd.
Austin, TX 78759
Attention: NuBus™ Licensing, M/S 2151

controller communications and hardware requirements overview

data communication paths

As a multimaster bus controller providing the ability for multiple devices to communicate across NuBus™, the Texas Instruments 'ACT2441 supports the following bus-master devices on the local NuBus™ I/O card.

The data paths supported are:

1) NuBus™ to local bus RAM, I/O hardware, and 'ACT2441 control registers
2) Local MC68000 to local RAM, I/O hardware, ACT2441 control registers, and NuBus™
3) Application specific processor on local bus to RAM, I/O hardware, 'ACT2441 control registers, and NuBus™.

In use, any hardware available to the local expansion card processor, the MC68000, is also available to the NuBus™ channel and another optional application specific processor (also referred to as an auxiliary/external processor).

expected expansion card hardware

The Macintosh Coprocessor Platform, as defined by Apple Computer, would typically consist of the following minimum configuration for a NuBus™ expansion card interfacing to the Macintosh II family of computers:

1) NuBus™ communication control circuits and transceivers (SN74BCT2425)
2) An on-board processor, the Motorola MC68000, to provide the card with intelligence and the ability to run the A/ROSE operating system.
3) DRAM for loading the A/ROSE operating system and for data storage.
4) The application-specific circuits, either nonintelligent, such as a SCSI or UART connection, or intelligent, such as a TMS380 Token Ring LAN chipset or TMS320 family of digital signal processors.

The designer of a NuBus™ master/slave interface using the 'ACT2441 may elect to provide all these features or may delete item 2 and/or 3, the on-board MC68000 processor and DRAM.

Intelligent NuBus™ cards, where neither A/ROSE nor the MC68000 are required (but the application includes programmable features to initiate NuBus™ master transactions through the 'ACT2441), may omit the MC68000 and/or DRAM (as in the case of the application either not needing local RAM or containing RAM local to itself). This intelligent interface can easily make use of all the NuBus™ master/slave interfacing capabilities of the 'ACT2441 without requiring the addition of a coprocessor or local RAM resources on the NuBus™ expansion card.

For nonintelligent cards, all initialization and control of the 'ACT2441 must take place from the NuBus™ channel, either from the host processor or another NuBus™ card. For such nonintelligent NuBus™ I/O cards, the 'ACT2441 initialization code can be placed in the NuBus™ ID ROM and executed as part of the power-on configuration by the Macintosh II. Using the 'ACT2441 for a nonintelligent NuBus™ card will require that another NuBus™ card initiate a master transaction, with the expansion card containing the 'ACT2441 acting as the NuBus™ slave. The Mac II motherboard contains a Slot-0 NuBus™ interface capable of master/slave cycles. This NuBus™ master would communicate with the 'ACT2441 control registers and with the local bus to which the application specific circuits would be connected. Such a design would not make full use of the master/slave capabilities of the 'ACT2441, but could utilize the bus interface, programmable features, and DRAM control of the 'ACT2441 in a minimum system.

In all cases, it is necessary for the local application on the NuBus™ card to model the bus timing and DMA handshaking of the MC68000 when using the 'ACT2441 to facilitate a master interface to the NuBus™. This could require $\overline{BR}$ to be tied to $\overline{BG}$ on the 'ACT2441 for devices that cannot supply an MC68000-style $\overline{BG}$, and whose memory cycle time is quick enough to provide zero-wait-state memory access similar to an MC68000 running at 10 MHz.

transceiver connection to NuBus™

Connection to NuBus™ from the 'ACT2441 can be accomplished in two ways: using discrete drivers and multiplexers or with a custom part from Texas Instruments, the SN74BCT2425. The type of connection chosen is up to the designer and depends upon many factors, such as the type and amount of DRAM used on the expansion card, as well as cost and board space considerations.

discrete transceiver interface

Memory expansion up to 8M bytes is possible using discrete components external to the 'ACT2441. Figure 1 is an example of a discrete transceiver NuBus™ interface supporting up to 8M bytes of DRAM on the local board. This example requires the use of five SN74ALSALS651 octal bus transceivers and registers and three SN74ALS258quad 1-of-2 data selectors/multiplexers.

In the discrete interface example , one SN74ALS651 device sends/receives data between local data bus bits D15-D8 and byte lane 2 of the upper NuBus™ word (eight bits of data corresponding to AD23-AD16 of NuBus™ data). Another two SN74ALS651 devices send/receive data between the local data bus bits D15-D0 and the lower NuBus™ word, byte lanes 0 and 1 (lower 16 bits of data corresponding to AD15-AD0 of NuBus™ data).

discrete transceiver interface (continued)

Please note that for the lower NuBus™ word, byte lane 0 (AD0-AD7) connects to D8-D15 and byte lane 1 (AD8-AD15) connects to D0-D7, performing the byte swapping needed between the 68K bus and NuBus™ (the remaining byte lane swapping for the upper NuBus™ data word is performed by the first SN74ALS651 and the 'ACT2441). The first SN74ALS651 communicates with NuBus™ byte lane 2 while communication to/from NuBus™ on byte lane 3 (AD31-AD24) is performed directly from the 'ACT2441 MCP controller to the NuBus™ channel without the need for extra transceivers. The remaining two SN74ALS651 devices are used to interface address lines A18-A3 to/from the local MC68000 bus and AD18-AD3 of the NuBus™ channel.

The three SN74ALS258 multiplexers are used to create the RA10-RA0 row/column address lines for the local bus DRAM. When the discrete interface is used, series damping resistors of 47 Ω should be connected between each SN74ALS258 output and the DRAM address lines to provide dampening of signal ringing.

It is possible to reduce the number of SN74ASL258 multiplexers if memory configurations are choosen that do not need all the RAx lines, such as 128K bytes in one row or 256K bytes in two rows. In these configurations, only two multiplexers would be needed as only RA7-RA0 are used for DRAM addressing.

To fully support the DRAM refresh requirements of 4M-bit DRAMs, the 'ACT2441 provides a separate RAM read signal, RAMRD, which should be connected to the DRAM $\overline{WE}$ (write enable) line instead of using the 'ACT2441 READ signal. For a complete discussion of the possible memory expansion available, please refer to the section discussing RAM interfacing for additional information.

integrated transceiver interface using SN74BCT2425

An alternate method of bus connection when using the 'ACT2441 is to utilize the SN74BCT2425 companion data path part from TI. Such a design minimizes the parts count while allowing up to 8M bytes of DRAM to be supported. Figure 2 is an example of such an interface.

The SN74BCT2425 MCP Data Path part supplies all the functionality of the five SN74ASL651s and three SN74ALS258 devices required for an 8M-bytes discrete transceiver interface. Byte lane swapping is provided internal to the SN74BCT2425 to facilitate the required byte reordering between the NuBus™ channel and the local 68K processor bus. The SN74BCT2425 data path device also supplies the RA0 through RA9 memory address lines, complete with internal series damping resistors. The 'ACT2441 controller can also be configured to supply the RA10 memory address when using 1M bit by 1 or 1M bit by 4 DRAMs. The $\overline{RASH}$ line is converted to function as RA10 when using these types of memory.

To fully support the DRAM refresh requirements of 4M-bit DRAMs, the 'ACT2441 provides a separate RAM read signal (RAMRD), which should be connected to the DRAM $\overline{WE}$ (write enable) line instead of using the 'ACT2441 READ signal.

Please refer to the section on RAM interfacing for an explanation of how to connect lines for various RAM configurations. Also note that the RAM address lines on the SN74BCT2425 are labeled 'RFx' instead of 'RAx'. This reflects the 45-Ω series resistors contained in each SN74BCT2425 to provide dampening on each line.

Figure 4 shows a typical MCP style interface to the MC68000 processor, along with DRAM, using the SN74BCT2425 Data Path transceiver from Texas Instruments.

hardware overview

This section provides a brief overview of the hardware features of the MCP NuBus™ controller chip. Additional details about the usage of features is contained in the "Signal Overview and Description" and "Hardware Description Details" sections.

I/O processor

The 'ACT2441 provides the hardware interfacing required to allow a 10-MHz MC68000 processor to be directly attached to the controller, if desired. The 10-MHz processor clock is derived from the 10-MHz NuBus™ clock via the delayed NuBus™ clocks, CLK25 and CLK75. Accesses by the MC68000 utilize a 16-bit data bus, with byte mode also supported. When downloaded onto the expansion card DRAM, the MC68000 processor can execute the A/ROSE operating system defined and supported by Apple Computer.

ROM

I/O interfacing is provided for a ROM to be present on the NuBus™ expansion card. The ROM serves as "power-up" code for the MC68000, a place for user firmware, and storage of NuBus™ ID data for the card. When viewed from the NuBus™ , the 16-bit wide ROM appears as a full 32- bit wide device capable of supporting 8-bit, 16-bit, and 32-bit bus reads. One wait state is inserted during each ROM access from any origination source.

If the MC68000 is not used or if executing out of ROM is not desired, a single 8-bit NuBus™ ID ROM can be used to define the NuBus™ attributes of the card. The NuBus™ ROM resides in the memory space beginning at $FsFF FFFF ('s'= NuBus™ slot ID and $ denotes a hexidecimal number) and extends downward for the number of bytes required for the NuBus™ ID information, see Apple documentation for specifics. In the case of an 8-bit wide ROM, data will appear in every other byte lane. The slot manager will search all byte lanes for the ROM.

NOTE: The Macintosh II Slot Manager will automatically recognize this byte lane configuration and fetch NuBus™ data correctly.

DRAM

The MCP controller supports various DRAM configurations, providing zero-wait-state accesses with 120-ns DRAMs, using $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refreshing (where the DRAM ignores the external address and the refresh address is generated internal to the DRAM). The refresh mechanism on the 'ACT2441 assumes a maximum refresh rate of 4 ms per 256 rows and provides a refresh cycle every 13 µs. From the NuBus™ interface, all RAM appears as a full 32-bit wide device, supporting 8-bit, 16-bit, and 32-bit bus operations.

The DRAM configurations supported are shown in Table 1. Please note the configurations recommended by Apple Computer and Texas Instruments.

Table 1. DRAM Configurations Supported

DRAM TYPE	1 ROW	2 ROWS	COMMENTS
64K × 4	**128K**†	256K‡	A19 on the 'ACT2441 is tied to A17 on MC68000 bus for 256K configuration to be decoded properly.
256K × 1	512K	1M	Default mode
256K × 4	512K†	**1M**†	Default mode
1M × 1	2M	4M	Requires configuration software§
1M × 4	**2M**†	4M	Requires configuration software§
4M × 1	8M	N/A	Requires configuration software§

† Apple Computer/TI-recommended RAM configurations.
‡ Not a recommended configuration because of physical address-line modifications required to enable this mode's operation.
§ Configuration software of the final application will set control registers in the 'ACT2441.

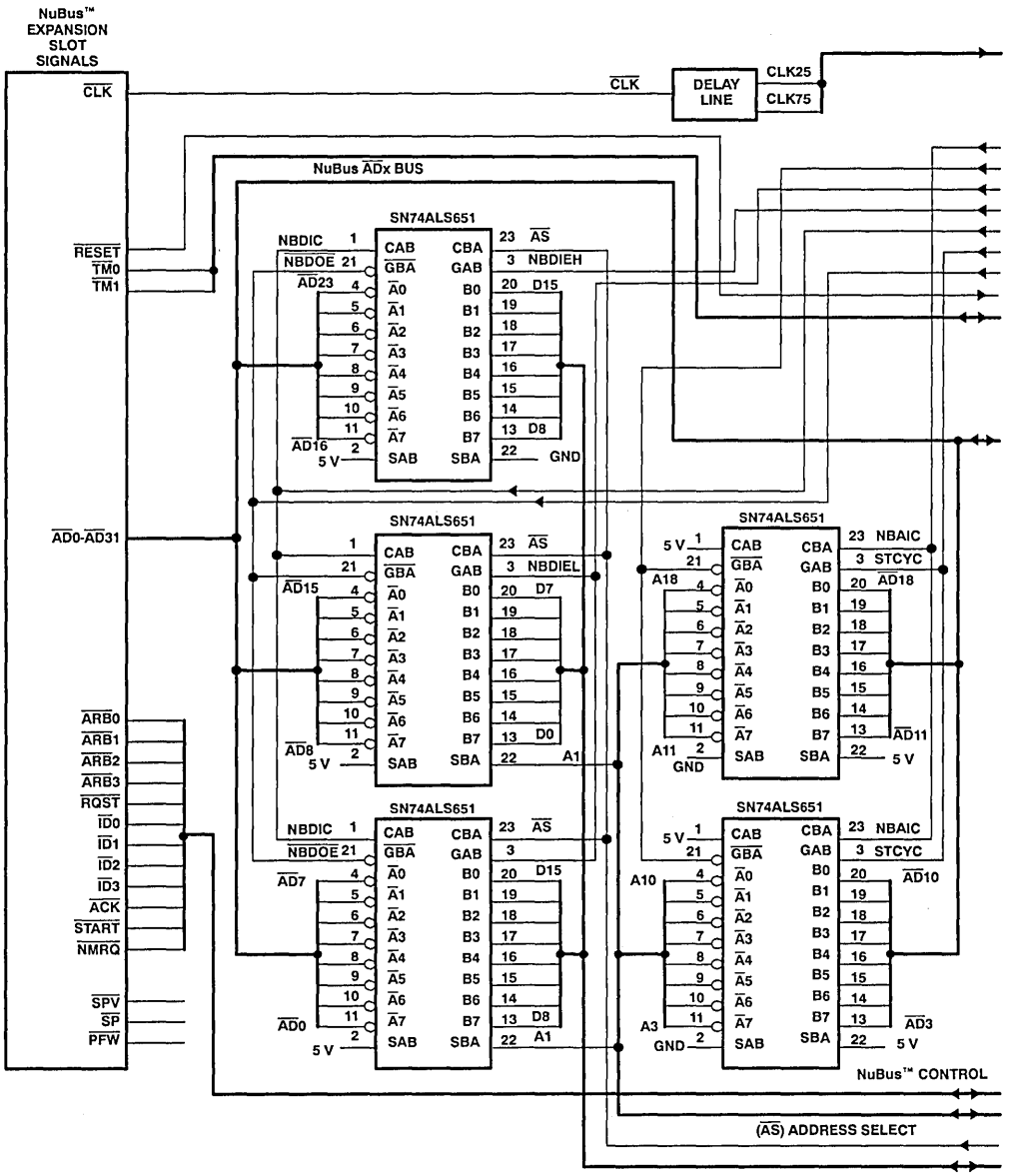


Figure 1. Discrete Transceiver Interface

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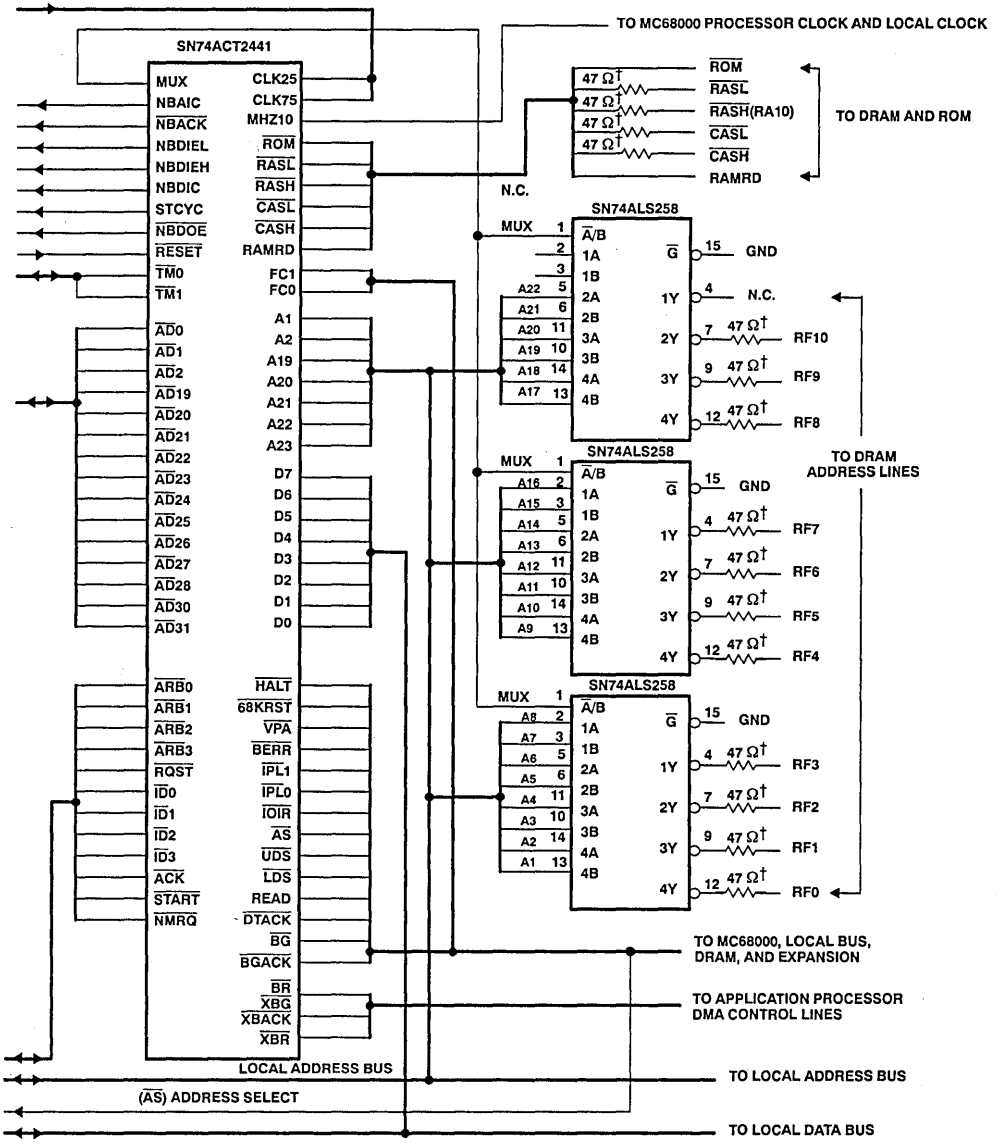
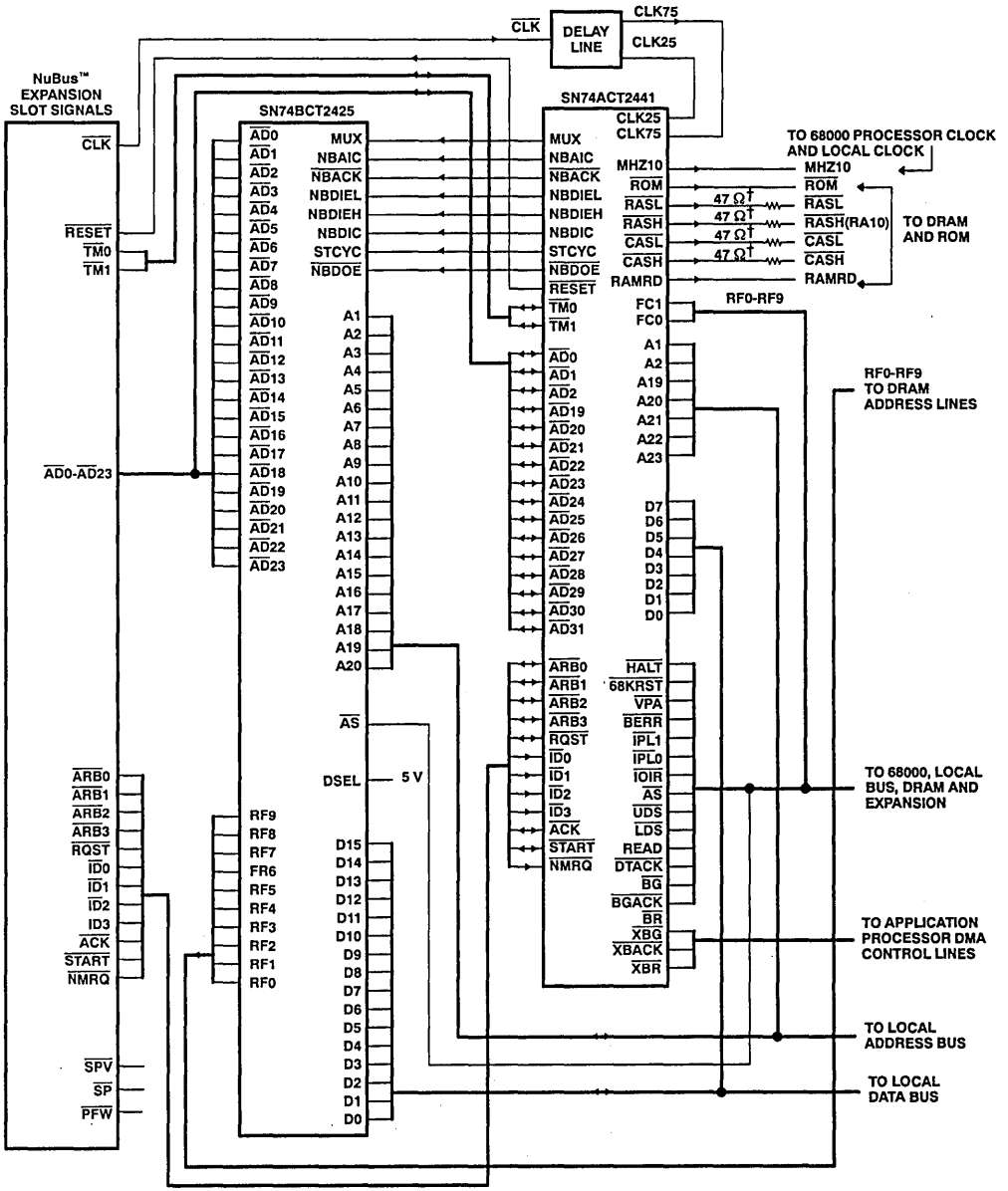


† Series damping resistors are recommended but may not be required, depending upon the system.

Figure 1. Discrete Transceiver Interface (Continued)



† Series damping resistors are recommended but may not be required, depending upon the system.

Figure 2. Integrated Transceiver Interface Using SN74BCT2425

NuBus™ Interface

The NuBus™ interface allows for either master or slave operation. In the master mode, the MC68000 makes an access to NuBus™ address space and waits until the operation is complete. In the slave mode, the MC68000 is "removed" from the internal bus while the NuBus™ access is taking place.

Since the MC68000 has an internal 16-bit bus, all bus cycles originating from the MC68000 can be either 8-bit or 16-bit operations. This includes both 8-bit and 16-bit NuBus™ operations if the MC68000 is the NuBus™ master.

Special hardware has been included so that 32-bit accesses coming in from NuBus™ will function correctly. The hardware performs two 16-bit bus operations on the MC68000 bus whenever NuBus™ requests a 32-bit operation. As a result, the card supports 8-bit, 16-bit, and 32-bit NuBus™ transfers.

NOTE: Since two MC68000 bus cycles are required for a 32-bit NuBus™ operation, using a 32-bit operation when only 16 bits are required should be avoided due to the increased amount of time required for the extra MC68000 bus cycle.

If the NuBus™ access cannot be completed, a bus error to the MC68000 is reported. The TM0 and TM1 value from the last ACK cycle to the card are saved in D6 and D7 of word CA000A for program usage in determining the type of NuBus™ error that occurred.

XBUS I/O processor

Hardware is provided on the 'ACT2441 to support a third local bus master through a set of DMA arbitration lines. The XBUS master (external bus master) is expected to perform R/W cycles and DMA operations that are compatible with a MC68000 processor cycles running at up to 10 MHz.

general-purpose I/O lines

An additional function of the XBUS control lines is to act as either memory-mapped decode or general-purpose I/O lines. The configuration of the XBUS is controlled via memory-mapped control registers within the 'ACT2441.

Interrupts

Hardware interrupt capability includes four sources: the internal timer, the NuBus™, the I/O Processor (also called IOP), and the IOP across NuBus™. Additional MC68000 interrupt levels can be added with the addition of an SN74LS148 8-line to 3-line priority encoder as shown in Figure 3.

timer

An internal 16-bit hardware timer is provided to allow programmable interrupts to be implemented with automatic reloading of initial values when zero is reached.

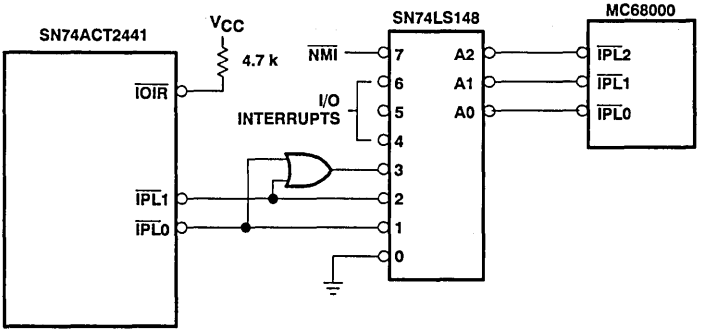
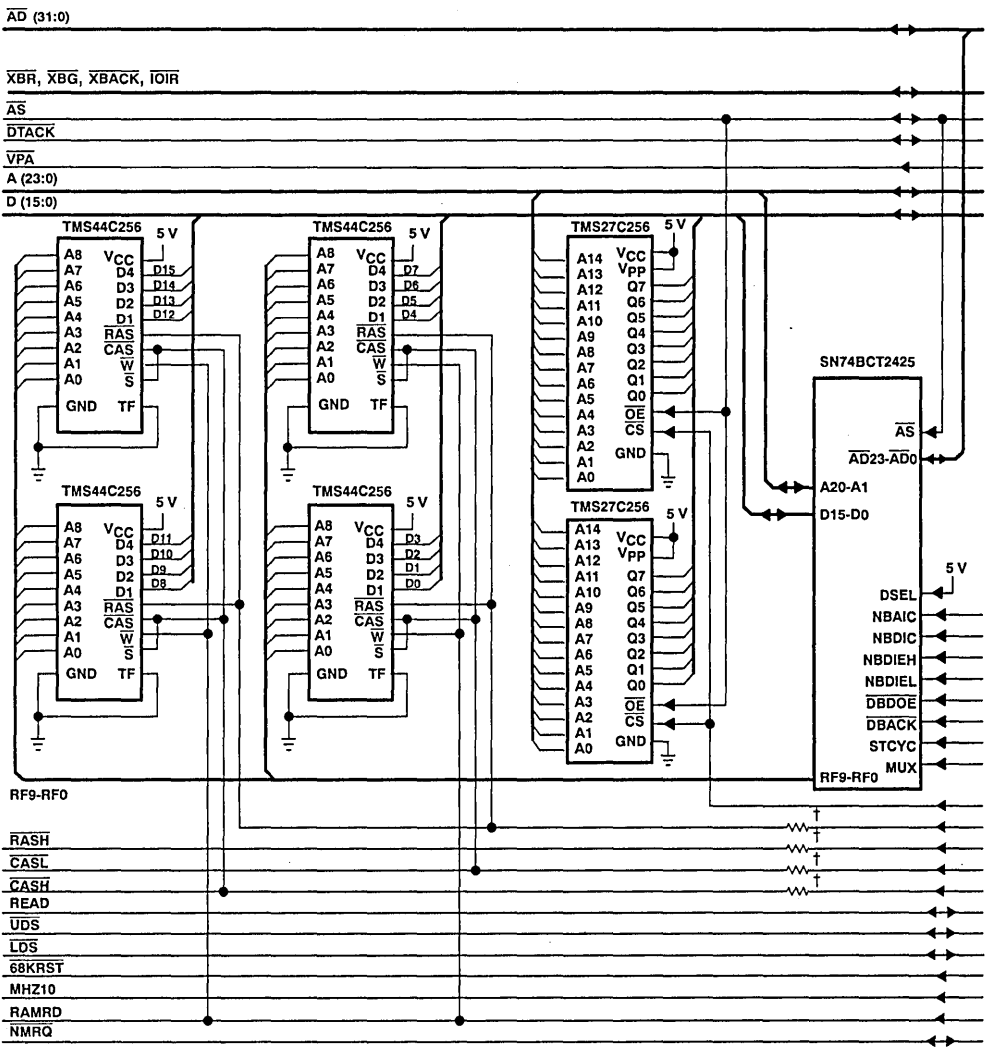


Figure 3. Expanding Interrupts to the MC68000

MCP architecture using 'ACT2441 and SN74BCT2425



† Series damping resistors are recommended but may not be required, depending upon the system.

Figure 4. System Implementation

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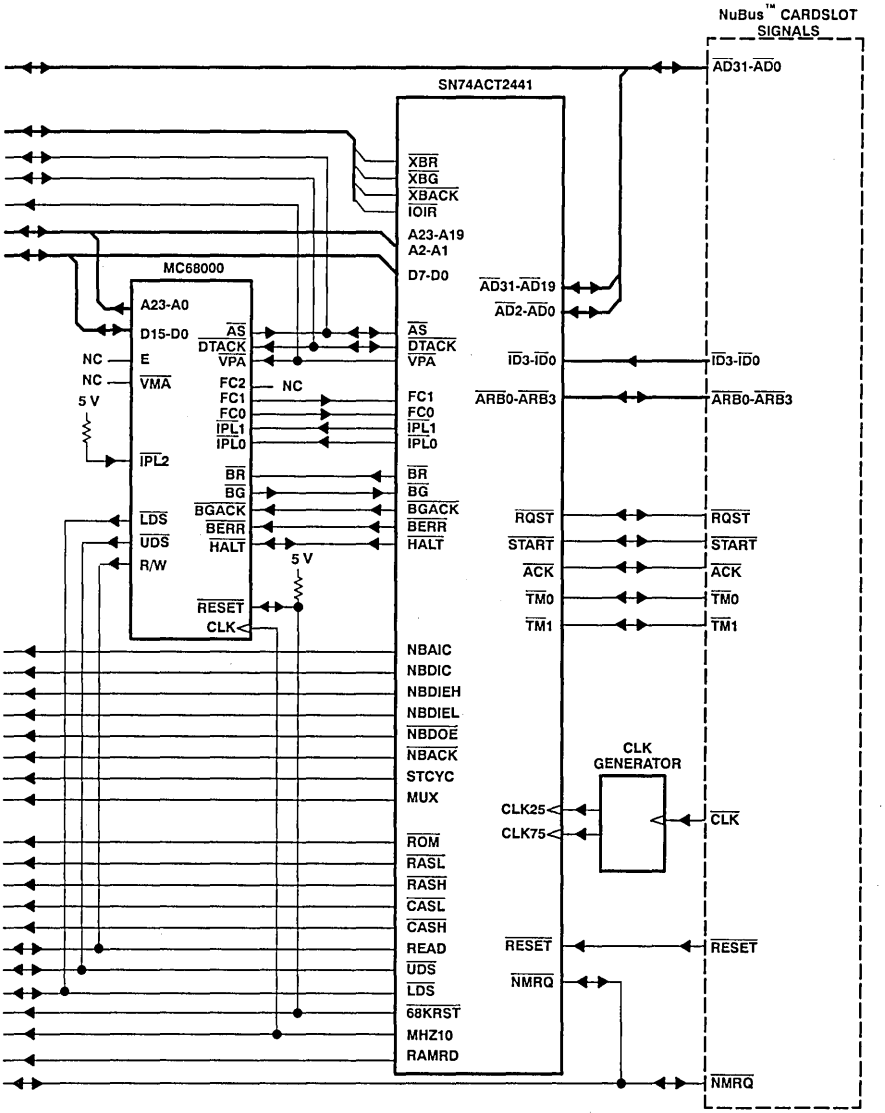

Figure 4. System Implementation (Continued)

signal overview and description

This section describes the functions of each signal on the 'ACT2441. Timing specifics for signals can be found in the section describing timing information.

PIN ASSIGNMENTS

PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
1	A22	26	$\overline{ID0}$	51	$\overline{AD19}$	76	GND
2	A21	27	GND	52	$\overline{AD2}$	77	$\overline{DTACK}$
3	A20	28	$\overline{RQST}$	53	GND	78	READ
4	A19	29	GND	54	$\overline{AD1}$	79	$\overline{LDS}$
5	A2	30	$\overline{ARB3}$	55	$\overline{AD0}$	80	$\overline{UDS}$
6	A1	31	$\overline{ARB2}$	56	V_{CC}	81	$\overline{AS}$
7	FC0	32	GND	57	$\overline{TM1}$	82	$\overline{IOIR}$
8	FC1	33	$\overline{ARB1}$	58	$\overline{TM0}$	83	$\overline{IPL0}$
9	RAMRD	34	$\overline{ARB0}$	59	$\overline{RESET}$	84	$\overline{IPL1}$
10	$\overline{CASH}$	35	GND	60	GND	85	$\overline{BERR}$
11	$\overline{CASL}$	36	$\overline{AD31}$	61	$\overline{NBDOE}$	86	$\overline{VPA}$
12	$\overline{RASH}$(RA10)	37	$\overline{AD30}$	62	STCYC	87	GND
13	$\overline{RASL}$	38	$\overline{AD29}$	63	NBDIC	88	$\overline{68KRST}$
14	$\overline{ROM}$	39	V_{CC}	64	NBDIEH	89	$\overline{HALT}$
15	MHZ10	40	$\overline{AD28}$	65	NBDIEL	90	V_{CC}
16	V_{CC}	41	GND	66	$\overline{NBACK}$	91	D0
17	CLK75	42	$\overline{AD27}$	67	NBAIC	92	D1
18	CLK25	43	$\overline{AD26}$	68	MUX	93	D2
19	GND	44	$\overline{AD25}$	69	V_{CC}	94	D3
20	$\overline{NMRQ}$	45	$\overline{AD24}$	70	$\overline{XBR}$	95	D4
21	$\overline{START}$	46	$\overline{AD23}$	71	$\overline{XBACK}$	96	D5
22	$\overline{ACK}$	47	GND	72	$\overline{XBG}$	97	D6
23	$\overline{ID3}$	48	$\overline{AD22}$	73	$\overline{BR}$	98	D7
24	$\overline{ID2}$	49	$\overline{AD21}$	74	$\overline{BGACK}$	99	GND
25	$\overline{ID1}$	50	$\overline{AD20}$	75	$\overline{BG}$	100	A23

TERMINAL FUNCTIONS

MC68000 and local bus interface lines

PIN NAME	I/O	DESCRIPTION
A23-A19, A2-A1	I/O	Address Bus Connections. These seven address bits correspond to the Motorola MC68000 16-bit processor address lines A23-A19 and A2-A1. Address information is conveyed to/from the chip via these bidirectional I/O lines. The lines are active high for both input and output.
$\overline{AS}$	I/O	Address Strobe. The $\overline{AS}$ control line is used to indicate that there is a valid address on the local address bus. When the controller is accessing local memory at the request of NuBus™ ('ACT2441 is the local master), this line goes active (low) when the address is valid. When the MC68000 is the master, the local bus is either reading or writing registers within the controller chip and this line signals the 'ACT2441 when the address is valid and may be used. When used with the SN74BCT2425, this line connects directly to the $\overline{AS}$ line of the SN74BCT2425 (as does the $\overline{AS}$ line of the MC68000 processor). When a discrete transceiver interface is used, this line is connected to the CBA line of the three SN74ALS651 devices that send/receive data between the local bus and the NuBus™ channel. This line is pulled up internally with a weak pullup resistor (95 μA).
$\overline{BERR}$	O	Bus Error Signaling. The $\overline{BERR}$ output signals a bus error condition to the MC68000 processor. The 'ACT2441 will drive $\overline{BERR}$ low when the 'ACT2441 is the NuBus™ master and a NuBus™ bus error (as signaled by $\overline{TM1}$ and $\overline{TM0}$) is received from the NuBus™ channel during the NuBus™ acknowledge cycle.
$\overline{HALT}$ (see Note 1)	O	$\overline{BERR}$ and $\overline{HALT}$ are used together to signal a relinquish-and-retry cycle to the MC68000 processor. This condition occurs when a NuBus™ transaction is coming onto the expansion card at the same time as the MC68000 is attempting to communicate with NuBus™. Incoming NuBus™ channel activity always takes priority over locally initiated NuBus™ transfers and $\overline{BERR}$ and $\overline{HALT}$ are both driven active low, signaling the MC68000 to relinquish the bus and retry later. Neither of these lines has an internal pullup resistor and should be pulled high externally.
$\overline{BG}$	I	DMA Bus Control. The Bus Grant ($\overline{BG}$) input signal is provided by the external MC68000 processor in response to a bus request. After the 'ACT2441 has requested bus mastership, it waits for this line to go active (low), indicating that the requesting device has been granted the bus.
$\overline{BGACK}$	O	DMA Bus Control. The Bus Grant Acknowledge ($\overline{BGACK}$) output informs the MC68000 that the 'ACT2441 has assumed bus mastership.
$\overline{BR}$	O	DMA Bus Control. The Bus Request ($\overline{BR}$) output IS NOT open-collector as is typical of devices driving the MC68000 $\overline{BR}$ input. It should be directly connected to the $\overline{BR}$ input on the MC68000 allowing centralized control of bus mastership. On an MCP style NuBus™ card, the 'ACT2441 resides between the MC68000 and all other bus masters that might request mastership of the local data bus. As such, it must be the ONLY line driving the $\overline{BR}$ input on the MC68000. When any device the 'ACT2441 services, such as NuBus™ or the XBUS I/O processor, needs to become the bus master, this line is driven active (low) by the chip. This signals the MC68000 that a device serviced by the MCP controller wishes to become the local bus master.
CLK25 CLK75	I I	Input Clocks. The two input clocks are 10-MHz signals that are used to generate an internal 20-MHz clock for the 'ACT2441 and the 10-MHz expansion board clock (MHZ10). CLK25 goes low at 0 ns and high at 25 ns while CLK75 goes low at 50 ns and high at 75 ns, thus the reason for their names. The figure below shows the CLK25 and CLK75 relationship to the 10-MHz NuBus™ clock ($\overline{CLK}$). These clocks should be created externally from the 10-MHz NuBus™ clock ($\overline{CLK}$) by delaying $\overline{CLK}$ through a delay-line circuit. (see Figure 5)
D7-D0	I/O	Data Bus. This 8-bit data bus provides a general-purpose bidirectional data path to/from the 'ACT2441 and the local bus on the MCP interface card. The lines are active high for both input and output.

NOTE 1: During relinquish-and-retry cycles to the 68K processor, the 'ACT2441 $\overline{HALT}$ line will remain active (low) until the ATTEN-NULL cycle has occurred. The $\overline{BERR}$ signal will go inactive (high) shortly after $\overline{AS}$ goes inactive (high). This slight variation from what is considered normal $\overline{BERR}$ and $\overline{HALT}$ activity, where $\overline{BERR}$ and $\overline{HALT}$ both go inactive (high) at about the same time just after $\overline{AS}$ goes inactive (high), ensures proper rearbitration for the NuBus™ will occur. The consequence of this variation on the normal relinquish-and-retry cycle is that an occasional NuBus™ arbitration cycle could occur where it is not absolutely necessary when the MC68000 processor retries a NuBus™ access. The possible effect of not holding $\overline{HALT}$ true until after the ATTEN-NULL cycle, though extremely unlikely, is a NuBus™ channel lockup, a much more catastrophic problem than an occasional NuBus™ rearbitration.

TERMINAL FUNCTIONS

MC68000 and local bus interface lines (continued)

PIN NAME	I/O	DESCRIPTION
$\overline{\text{DTACK}}$	I/O	Data Transfer Acknowledge. The $\overline{\text{DTACK}}$ line is used to indicate that a data transfer is complete. When the 'ACT2441 is accessing the local bus at the request of NuBus™, this line is an input. When the device being accessed (RAM or I/O devices) responds with an active (low) $\overline{\text{DTACK}}$ during a read operation, the data is latched and the bus cycle is terminated. When $\overline{\text{DTACK}}$ goes low during a write cycle from the 'ACT2441 to the local bus, the 'ACT2441 terminates the cycle. This line is pulled up internally with a weak pullup resistor (400 μA). When the local MC68000 (or external application) is reading or writing to the 'ACT2441 control registers or to NuBus™ through the 'ACT2441, this line is an output. When reading from the 'ACT2441 or NuBus™, the $\overline{\text{DTACK}}$ signal will go low to signal that the MC68000 should latch the data and terminate the cycle. When writing to the 'ACT2441 or NuBus™, the MC68000 should terminate the write cycle when $\overline{\text{DTACK}}$ is brought low by the 'ACT2441. $\overline{\text{DTACK}}$ may be configured for RAM or I/O usage within various address ranges. When configured for I/O space, the number of wait states required by the I/O device can be set using the 'ACT2441 control registers. Additionally, $\overline{\text{DTACK}}$ can be configured for either synchronous or asynchronous operation (the default is synchronous). Refer to hardware details for complete instructions on selecting these options.
FC1-FC0	I	Processor Status. The FC1 and FC0 lines are active high and are used to detect the status of the external I/O processor using standard MC68000 protocols. The only status monitored is the interrupt acknowledge cycle (FC1 and FC0 both high).
$\overline{\text{IOIR}}$	I	I/O Processor Interrupt. The $\overline{\text{IOIR}}$ input allows an external device to cause a level 3 interrupt to be issued from the $\overline{\text{IPL1}}$ and $\overline{\text{IPL0}}$ lines of the 'ACT2441, for signaling the MC68000 processor. This line is pulled up internally with a weak pullup resistor (95 μA).
$\overline{\text{IPL1}}$-$\overline{\text{IPL0}}$	O	Interrupt Control. These two active low outputs are used to provide encoded interrupt priority information to an external MC68000 processor. Three interrupt levels can be reported, 1 (from the internal timer), 2 (from NuBus™) and 3 (from the I/O interface). It is assumed that the third standard MC68000 interrupt line, $\overline{\text{IPL2}}$ (not provided by the 'ACT2441 interface) is pulled high to an inactive state during interrupt cycling by this device. Interrupts are encoded in an inverse-true pattern, i.e., level zero (all lines high) indicates that no interrupt is requested and level seven (all lines low) is the highest priority available to the external processor. These $\overline{\text{IPLx}}$ lines will remain stable until the external processor signals an interrupt acknowledge cycle (FC2-FC0 all high, of which only FC1-FC0 are inputs to this device).
LDS UDS	I/O I/O	Lower and Upper Data Strobe. These signals control the data flow on the 16-bit data bus of the local MCP card. The lower 8-bits, upper 8-bits, or both upper and lower 8-bits of data may be selected. When the controller is accessing local memory at the request of NuBus™, these lines are outputs and reflect the size of the data transfer needed (8 or 16 bits). When the local MC68000 is reading or writing registers within the controller, these lines are inputs, thus allowing the MC68000 to specify lower byte, upper byte, or word operations to the control registers of the 'ACT2441. Both lines are active low and are pulled up internally with a weak pullup resistor (95 μA).
MHZ10	O	Expansion Board Clock. This output is a TTL-compatible symmetrical 10-MHz clock to be used by on-board circuits communicating with the 'ACT2441, such as the MC68000 processor. The signal is derived internally from the CLK25 and CLK75 input clocks.
READ	I/O	Read/Write Selection. The READ line controls whether a read or write operation will occur. When the controller is accessing the local bus at the request of NuBus™, this line is an output and is normally connected to the read and/or write (R/W) line of static RAM, ROM, and I/O devices. When the local MC68000 processor is reading or writing to 'ACT2441 control registers or to NuBus™ through the 'ACT2441, this line is an input. A high level on READ indicates a read cycle and a low level signals a write cycle. This line is pulled up internally with a weak pullup resistor (95 μA). A special DRAM read line, RAMRD, is provided for connection to DRAM R/W lines. This signal is activated slightly different than READ in order to provide for proper refreshing of 4M-bit DRAM devices. Even when 4M-bit DRAMs will not be used, it is recommended that the RAMRD line be used exclusively for connection to DRAMs rather than the READ line.
$\overline{\text{VPA}}$	O	Valid Peripheral Address†. $\overline{\text{VPA}}$ indicates that the address being accessed on the expansion card local bus contains an MC6800-style peripheral device, as such data transfer should be synchronized with the enable (E) signal of the MC68000 processor. This line is pulled up internally with a weak pullup resistor (400 μA).

† 6800 cycles are not supported from NuBus™.

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TERMINAL FUNCTIONS

MC68000 and local bus interface lines (continued)

PIN NAME	I/O	DESCRIPTION
$\overline{\text{XBACK}}$	I/O	External DMA Bus Control, General-Purpose I/O, and Address Decode Lines. External Bus Grant Acknowledge – Bidirectional (Input for DMA) – When the chip is configured to use the XBUS as DMA control, this control signal is an input. After the external device receives the bus grant signal (through the $\overline{\text{XBG}}$ output) it acknowledges to the MCP controller that it has assumed bus mastership. The MCP controller in turn passes the state of this input back to the MC68000 through the $\overline{\text{BGACK}}$ output. This informs the MC68000 that the device requesting bus mastership has taken over the bus. (See WARNING) In addition to its usage as an external DMA control line, this signal may also be configured as a general-purpose I/O line or an active-low address decode line. Configuration of the available modes is set with data bits D2 and D3 in the XDMA Control Register at location CA0008 in the 'ACT2441. The line's current status can always be read in data bit D2 of the read word at location CA000A. This line is pulled up internally with a weak pullup resistor (95 μA).
$\overline{\text{XBG}}$	I/O	External DMA Bus Control, General-Purpose I/O, and Address Decode Lines. External Bus Grant – Bidirectional (Output for DMA) – When the 'ACT2441 is configured to use the XBUS lines as DMA control lines, this signal is an output. When the MC68000 grants the $\overline{\text{XBR}}$ of the controller, via the the $\overline{\text{BG}}$ input, the controller then passes the bus grant signal onto the $\overline{\text{XBG}}$ output. This signals the external device that it has been granted bus mastership. (See WARNING) In addition to its usage as an external DMA device control line, this line may also be configured as a general-purpose I/O line or an active-low address decode line. Configuration of the available modes is set with data bits D6 and D7 in the XDMA Control Register at location CA0008 on the 'ACT2441. The line's current status can always be read in data bit D1 of the read word at location CA000A. This line is pulled up internally with a weak pullup resistor (95 μA).
$\overline{\text{XBR}}$	I/O	External DMA Bus Control, General-Purpose I/O, and Address Decode Lines. External Bus Request ($\overline{\text{XBR}}$) – Bidirectional (Input for DMA) – When the 'ACT2441 is configured to use the XBUS lines as DMA control lines, this signal is an input. This line is connected to the $\overline{\text{BR}}$ output line of an external device that wishes to gain bus mastership. When the external device needs to become the bus master, this line is driven active (low) by the external device and is passed onto the MC68000 by the MCP controller using the 'ACT2441 $\overline{\text{BR}}$ output line. This signals the MC68000 that a device serviced by the MCP controller wishes to become the bus master of the local bus. (See WARNING) In addition to its usage as an external DMA control line, this line may also be configured as a general-purpose I/O line or an active-low address decode line. Configuration of the address decode is set with data bits D4 and D5 of the XDMA Control Register, at location CA0008 on the 'ACT2441. The line's current status can always be read in data bit D0 of the read word at location CA000A. This line is pulled up internally with a weak pullup resistor (95 μA).
$\overline{\text{68KRST}}$	O	MC68000 Reset Line. This line is intended for use as the reset line for the MC68000 coprocessor and other I/O devices residing on the NuBus™ expansion card. $\overline{\text{68KRST}}$ goes active (low) in response to either a hardware reset (the NuBus™ $\overline{\text{RESET}}$ line) or as the result of a software reset ("soft reset") by performing a ROM read at location F00000 from NuBus™. Please note that when $\overline{\text{68KRST}}$ is activated by means of the external hardware reset, it is delayed by four (4) 10-MHz clocks by an internal shift register. There is no such delay when activated via the soft reset. The $\overline{\text{68KRST}}$ signal may also be connected to any other device that needs to be reset at the same time as the MC68000. This line does not have an internal pullup resistor and should be pulled high externally.

WARNING: Since the Macintosh II NuBus™ times out if it does not gain access to the local bus, any external bus master MUST NOT tie up the local bus for an extended period of time (5 μs max is suggested). In addition, if the external bus master is going to transfer to NuBus™, it must handle relinquish and retry cycles (see MC68000 manual). If it cannot, it must expend bus errors and deal with them. The NuBus™-to-I/O card access takes priority over card-to-NuBus™ cycles. When a conflict arises, the 'ACT2441 issues a bus error to the current local bus master.

TERMINAL FUNCTIONS

DRAM and memory controls

PIN NAME	I/O	DESCRIPTION
$\overline{CASH}$ $\overline{CASL}$	O O	Column-Address Strobe Lines. These two outputs provide the column address strobes for the upper and lower bytes of the DRAM. $\overline{CASH}$ strobes the high byte (D15-D8) into the column address while $\overline{CASL}$ strobes the column address into the low byte (D7-D0). In addition to their usage in addressing memory, these lines also are active during the $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
MUX	O	Multiplex Row/Column Addresses to DRAM. The MUX output line is used to multiplex between row addresses and column addresses. This signal should be connected to either the MUX line of the 'BCT2425 or to the SELECT A/B line of the 'ALS258 multiplexers when using the discrete interface. The MUX output is high during row addresses and low during column addresses.
RAMRD	O	RAM Read. The RAMRD output functions as the R/$\overline{W}$ line for DRAM memories and should be connected to the R/$\overline{W}$ lines of all DRAM memories. RAMRD operates in a slightly different manner than does the generic read line (READ), in that RAMRD always remains in the read state (a high level) during $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles. This cycle variation ensures that the requirements of newer 4M-bit DRAM memories, which require their R/$\overline{W}$ line to remain in the read state during refresh, are satisfied. It is possible that the normal read line (READ) could be used for DRAMs smaller than 4M bits, but it is recommended that RAMRD be used exclusively for all DRAM R/W operations.
$\overline{RASH}$ (RA10) $\overline{RASL}$	O O	Row-Address Strobe Lines. These two outputs provide the row address strobes for two word-wide (16- bits) DRAM rows. $\overline{RASL}$ strobes the row address into the first row of the DRAM array while $\overline{RASH}$ strobes the row address into the DRAM address of a second, optional, row of DRAM memory. In addition to their usage in addressing memory, these lines are also active during $\overline{CAS}$-before-$\overline{RAS}$- refresh cycles as provided by the 'ACT2441. The default mode is that $\overline{RASH}$ acts as the $\overline{RAS}$ signal for the second row of DRAMs. Optionally, $\overline{RASH}$ can be configured via the DTACK Control Register 1 to act as an extra row address line, (RA10). This allows the use of one row of 4M-bit DRAMs in a fully expanded 8M-byte DRAM system using the 'ACT2441 controller. Optionally, the 'ACT2441 output pins for $\overline{RASH}$(RA10) and $\overline{RASL}$ can be swapped via bit 6 of the TI TEST CONFIGURATION REGISTER. The ability to swap the $\overline{RASH}$ and $\overline{RASL}$ allows configuration of 2.5M-bytes of contiguous DRAM expansion memory. For example, in the case where 512K bytes of DRAM is soldered onto the board in row 1 and 2M-bytes is socketed for future expansion in row 2. Without the ability to swap the $\overline{RASH}$ and $\overline{RASL}$ lines, each row would be configured for 2M-bytes of DRAM, with a gap of 1.5M-bytes between each section. The default mode for $\overline{RASH}$(RA10) and $\overline{RASL}$ is the same as shown in the pinout specifications. Please refer to the RAM section for further information about available RAM configurations.
$\overline{ROM}$	O	Read Only Memory Select. The $\overline{ROM}$ output will go active (low) when reading on-board ROM locations from F00000 to FFFFFF. This output should be tied to the $\overline{CS}$ input of the on-board ROMs.

NuBus™ interface and control signals

The following signals connect directly to the NuBus™ expansion connector and NuBus™ transceiver circuits.

PIN NAME	I/O	DESCRIPTION
$\overline{ACK}$	I/O	NuBus™ Transfer Acknowledge. The $\overline{ACK}$ line is used to signal the end of a NuBus™ transfer cycle. During read transfers, the NuBus™ slave will assert $\overline{ACK}$ active (low) when it has placed valid data on the $\overline{AD}$x lines. During write transactions, the NuBus™ slave asserts $\overline{ACK}$ when the incoming data has been accepted. This line is an input when the 'ACT2441 is a NuBus™ master and this line is an output when the device is a NuBus™ slave. In addition to the acknowledge function, this line is also used to signal a special attention cycle when asserted at the same time as $\overline{START}$. This line is pulled up internally with a weak pullup resistor (5 μA).
$\overline{AD}$31-$\overline{AD}$19 $\overline{AD}$2-$\overline{AD}$0	I/O	NuBus™ Multiplexed Address/Data Bus. These active-low lines carry the multiplexed NuBus™ address and data information to/from the NuBus™ channel. Only those addresses required by the 'ACT2441 controller are provided. The remaining $\overline{AD}$x lines are supplied by the the 'BCT2425 or a discrete implementation of the NuBus™ transceiver interface. During a NuBus™ start cycle, these lines contain address information and later carry data during the NuBus™ acknowledge cycle. The direction of the lines are changed as a group dependent upon the current NuBus™ transaction taking place, read/write or address/data. An additional usage of the $\overline{AD}$1-$\overline{AD}$0 lines are to convey two of the four bits of NuBus™ transfer mode information during the start cycle. Of these group of lines, $\overline{AD}$23-$\overline{AD}$19, and $\overline{AD}$2-$\overline{AD}$0 are used only to convey address and transfer mode information ($\overline{AD}$1-$\overline{AD}$0 along with $\overline{TM}$1-$\overline{TM}$0 define the transfer mode during the start cycle) when communicating with the 'ACT2441. $\overline{AD}$31-$\overline{AD}$24 convey both address and data information to/from the 'ACT2441. For data transfers to/from 'ACT2441 control registers in byte lane 3, $\overline{AD}$31-$\overline{AD}$24 contain the 8-bit register value during the data portion of the NuBus™ cycle.

TERMINAL FUNCTIONS

NuBus™ interface and control signals (continued)

PIN NAME	I/O	DESCRIPTION
$\overline{ARB3}$-$\overline{ARB0}$	I/O	NuBus™ Arbitration Lines. The arbitration lines $\overline{ARB3}$-$\overline{ARB0}$ are open-collector lines connected between all NuBus™ cards using the same binary coding as the $\overline{ID}$x lines. During a NuBus™ arbitration cycle, one or more cards may contend for mastership of the NuBus™ channel. If the 'ACT2441 is contending for the bus ('ACT2441 driving $\overline{RQST}$ low after determining that $\overline{RQST}$ was unasserted), the $\overline{ID}$x code is placed on the $\overline{ARB}$x bus, along with the $\overline{ID}$x values of all other cards that have asserted their $\overline{RQST}$ lines and are contending for the bus. The 'ACT2441 then competes with all other contending cards for ownership of the bus. After two clock periods, the arbitration is complete and the $\overline{ARB}$x lines are left with the slot ID of the card winning the arbitration contest (the card that had the highest ID code). These lines are pulled up internally with a weak pullup resistor (5 μA).
$\overline{ID3}$-$\overline{ID0}$	I	NuBus™ ID Lines. Identification lines $\overline{ID3}$ thru $\overline{ID0}$ are binary-coded inputs used to identify the NuBus™ card slot where the MCP card resides. The ID lines are typically hardwired with unique slot ID at the NuBus™ connector on the expansion chassis. The line coding is active low, which means that the lowest-numbered slot (0) is coded with all ID lines open. These lines are in turn pulled up with resistors to an inactive state of 1111. The highest slot ID (F) has all four lines wired low to read 0000. These lines are pulled up internally with a weak pullup resistor (5 μA).
$\overline{NMRQ}$	I/O	NuBus™ Non-Master Request. $\overline{NMRQ}$ is an active-low asynchronous interrupt mechanism allowing NuBus™ boards to interrupt the NuBus™ channel as a slave-only device. This line is connected to $\overline{NMRQ}$ on the NuBus™ channel. When the 'ACT2441 is placed in the 'NMRQ Master Mode', this line is an input, allowing an external slave-type device to interrupt the NuBus™ card with the 'ACT2441 acting as the NuBus™ master. When the 'ACT2441 is not in the master mode (i.e., is a slave NuBus™ interface, which is the normal NuBus™ operation) this line is an output, allowing the NuBus™ card built with the 'ACT2441 to interrupt the NuBus™ channel as a slave device. This line is internally pulled up with a weak resistor (5 μA).
$\overline{RESET}$	I	NuBus™ Reset. The $\overline{RESET}$ input is used to reset the 'ACT2441 device and place it in the powerup state. $\overline{RESET}$ is connected directly to the NuBus™ signal $\overline{RESET}$. All internal registers are cleared upon the application of this power-on-style hardware reset.
$\overline{RQST}$	I/O	NuBus™ Master Request Line. $\overline{RQST}$ is an open-collector line and is bused between all other NuBus™ slots. The line is asserted active (low) by any device wishing to gain ownership of the NuBus™. When the 'ACT2441 wishes to become the bus master, it first reads the status of this line, and upon finding it unasserted, drives the line active (low) to begin a NuBus™ arbitration cycle. According to this description, $\overline{RQST}$ is an input prior to making the decision to request mastership and is changed to an output during the request cycle. This line is pulled up internally with a weak pullup resistor (5 μA).
$\overline{START}$	I/O	NuBus™ Transfer Start Line. The $\overline{START}$ line is used to signal the beginning of a NuBus™ transfer. When the 'ACT2441 is the NuBus™ master, it will drive $\overline{START}$ low for one clock cycle at the beginning of the transfer, along with the appropriate address. When the 'ACT2441 is a NuBus™ slave, this line is used to sense when a NuBus™ transaction has occurred. In addition to signaling the start of a NuBus™ transaction, this line is used to initiate an arbitration contest between any cards requesting bus ownership. The $\overline{START}$ is also used for signaling attention cycles when asserted with $\overline{ACK}$. This line is pulled up internally with a weak pullup resistor (5 μA).
$\overline{TM1}$-$\overline{TM0}$	I/O	NuBus™ Transfer Mode Line. $\overline{TM1}$-$\overline{TM0}$ indicate to NuBus™ devices which type of transfer is occurring at the beginning of a NuBus™ transaction and later conveys success or failure of the transfer. The TMx lines (along with $\overline{AD1}$-$\overline{AD0}$) indicate the type (read or write) and size (byte, halfword or word) of the NuBus™ transaction during the NuBus™ start cycle. During NuBus™ acknowledge cycles ($\overline{ACK}$ low), the TMx lines provide status information to the current NuBus™ master concerning the success or failure of the NuBus™ transaction. A third usage of the TMx lines is during NuBus™ attention cycles ($\overline{START}$ and $\overline{ACK}$ both driven low), when the lines are used to identify the type of attention cycle. These lines are pulled up internally with a weak pullup resistor (5 μA).

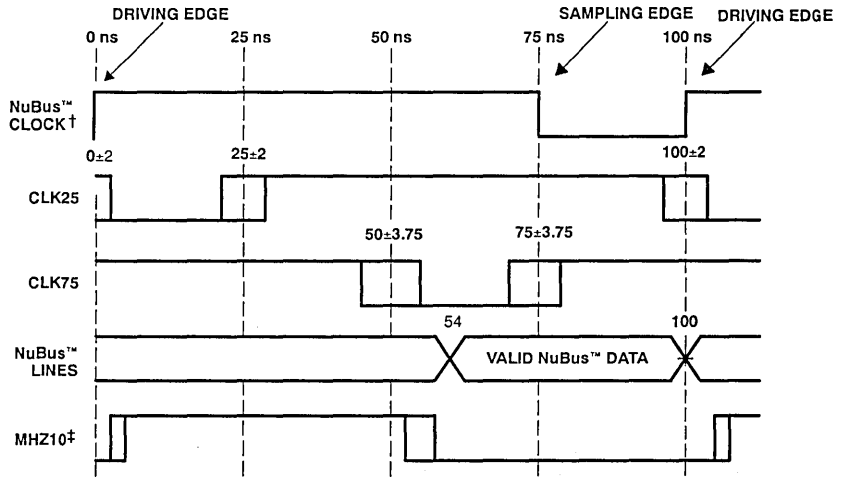
TERMINAL FUNCTIONS

NuBus™ transceiver interface (NBAIC, NBDIC, NBDIEH, NBDIEL, $\overline{\text{NBDOE}}$, $\overline{\text{NBACK}}$, and STCYC) – outputs

These lines are used for NuBus™ transceiver interface, either to the SN74BCT2425 or to a discrete transceiver interface.

PIN NAME	I/O	DESCRIPTION
$\overline{\text{NBACK}}$ (see Note 2)	O	NuBus™ Acknowledge. This active-low output is used to enable the NuBus™ transceivers to output the address to the local bus, as captured from the AD lines of NuBus™. When using the SN74BCT2425, this line connects directly to the $\overline{\text{NBACK}}$ line of the SN74BCT2425. When a discrete transceiver interface is used, this line is connected to the $\overline{\text{GBA}}$ 3-state control line on the two SN74ALS651 devices that send/receive address lines A18-A3 to/from the NuBus™ channel.
NBAIC	O	NuBus™ Address Clock. This output signals the NuBus™ transceiver to capture the incoming address portion of the NuBus™ address during read or write operations. When using the SN74BCT2425, this line connects directly to the NBAIC line of the SN74BCT2425. When a discrete transceiver interface is used, this line connects to the CBA line of the two SN74ALS651 devices that send/receive address information A18-A3 to/from the NuBus™ channel. The remainder of the 24-bit address from the local MC68000 bus to the NuBus™ are made directly from the SN74ACT2441 to NuBus™. This output will make a low-to-high transition on the sampling edge (high-to-low) of the NuBus™ clock during NuBus™ start cycles. This operation supplies address information to the local bus of the NuBus™ expansion card.
NBDIC	O	NuBus™ Data Clock. This output signals the NuBus™ transceiver to capture the incoming data portion of the NuBus™ transfer during read (master) or write (slave) operations. When using the SN74BCT2425, this line connects directly to the NBDIC line of the SN74BCT2425. When a discrete transceiver interface is used, this line is connected to the CAB line of the three SN74ALS651 devices that send/receive data between the local bus and the NuBus™ channel. This output will make a low-to-high transition on the sampling edge (high-to-low) of the NuBus™ clock when a data transfer to the local bus is occurring.
$\overline{\text{NBDOE}}$	O	NuBus™ Data Output Enable. $\overline{\text{NBODE}}$ is an active-low output used to enable the NuBus™ transceivers corresponding to the D0-D3 data portion of the local bus onto the NuBus™ AD lines. When using the SN74BCT2425, this line connects directly to the $\overline{\text{NBODE}}$ line of the SN74BCT2425. When a discrete transceiver interface is used, this line is connected to the $\overline{\text{GBA}}$ line of the three SN74ALS651 devices that send/receive data between the local bus and the NuBus™ channel.
NBDIEL	O	NuBus™ Data Enable Low. This active-high output is used to enable the input of NuBus™ data from the NuBus™ to the local bus for the low halfword (lower 16 bits). When using the SN74BCT2425, this line connects directly to the NBDIEL line of the SN74BCT2425. When a discrete transceiver interface is used, this line is connected to the GAB line of the two SN74ALS651 devices which send/receive data between the local data bus bits D15-D0 and the lower NuBus™ halfword, byte lanes 0 and 1 (lower 16 bits of data corresponding to AD15-AD0 of NuBus™ data).
NBDIEH	O	NuBus™ Data Enable High. This active-high output is used to enable the input of NuBus™ data from the NuBus™ AD lines to the local bus for the high halfword (upper 16 bits). When using the SN74BCT2425, this line connects directly to the NBDIEH line of the SN74BCT2425. When a discrete transceiver interface is used, this line is connected to the GAB line of the single SN74ALS651 device that sends/receives data between the local data bus (bits D15-D8) and byte lane 2 of the upper NuBus™ halfword (8 bits of data corresponding to AD23-AD16 of NuBus™ data). The remaining 8 bits (D7-D0 corresponding to D31-D24 of NuBus™ data, byte lane 3) of the upper halfword are supplied by direct connection of the 'ACT2441 MCP Controller to NuBus™.
STCYC (see Note 2)	O	Start Cycle Active. This active-high output is used to enable the address onto the NuBus™ AD bus from the local bus. In the situation where the designer has used the SN74BCT2425, STCYC would be connected to the signal of the same name. When a discrete transceiver interface is used, this line is connected to the GAB 3-state control line of the two SN74ALS651 devices that send/receive address lines A18-A3 to/from the NuBus™ channel. The remainder of the 24-bit address line connections from the local MC68000 bus to NuBus™ are made directly from the 'ACT2441.

NOTE: 2. When a discrete interface is used, it is assumed that the two SN74ALS651s used for address demultiplexing of A18-A3 use the 'A' side transceiver lines to connect to the MC68000 local bus address bus and that the 'B' side transceiver lines connect to the NuBus™.



† CLK25 and CLK75 are relative to a perfect 10-MHz NuBus™ Clock ($\overline{CLK}$).
‡ MHZ10 is derived from CLK25 and CLK75, see timing spec for offset specificaiton.

Figure 5. 'ACT2441 Input Clocks and MHZ10 Output Clock

hardware description details

This section provides an expanded discussion of the hardware features available from the 'ACT2441 MCP NuBus™ Controller. The method of selection and control of these features is documented here.

DRAM interfacing

The following information provides specifics about interfacing to various DRAM configurations. DRAMs supported must meet or exceed 120-ns speeds with 4-ms/256 rows of $\overline{CAS}$-before-$\overline{RAS}$ refreshing requirement.

Table 2. Apple Computer/TI Recommended DRAM Configurations

MEMORY AND DEVICE SIZE	NOTES
128K – one row 64K x 4 DRAMs	MCP A19 tied to local bus A19
512K – one row 256K x 4 DRAMs	Default mode
1 M – two rows 256K x 4 DRAMs	Default mode
2 M – one row 1M x 4 DRAMs	Requires setting registers in 'ACT2441

WARNING: When choosing DRAM configurations, the user must be careful not to exceed the capacitive loading specifications of the 'ACT2441 or speed problems may occur. This may mandate the use of by-4 DRAMs or external buffering.

The refresh method provided by the 'ACT2441 conforms to $\overline{CAS}$-before-$\overline{RAS}$-refreshing and assumes that the DRAM devices used ignore the external address lines and contain their own row counters to generate the refresh address internally.

interfacing to DRAM using SN74BCT2425

When using the SN74BCT2425 data path device, up to 8M bytes of DRAM may be accessed with proper configuration of the 'ACT2441. Table 3 shows the control-line requirements for interfacing the 'ACT2441 to the SN74BCT2425 data path device for all available memory configurations. When interfacing to 8M bytes of memory, the DRAM RA10 line must be supplied. This can be accomplished by using the SN74BCT2425 to create RA0-RA9 and using the 'ACT2441's $\overline{RASH}$(RA10) line as RA10 (Note: the $\overline{RASH}$(RA10) signal must be

configured via the DTACK Control Register 1). Please note that the lines on the SN74BCT2425 are actually labeled 'RFx' denoting their built-in series dampening resistors. It is recommended that a 47-Ω damping resistor be placed in series with RA10 to reduce signal ringing.

Table 3. Control Requirements for DRAM Interfacing

MEMORY SIZE	ROW ADDR NEEDED	'ACT2441 $\overline{\text{RASH}}$	NOTES
128K – one row 64K × 4 DRAM	**RA0-RA7**	**N.C.**	**MCP A19 tied to A19**
256K – two rows 64K × 4 DRAM	RA0-RA7	$\overline{\text{RASH}}$	MCP A19 to local bus A17
512K – one row 256K × 1 DRAM	RA0-RA8	N.C.	Supplied by SN74BCT2425
1M – two rows 256K × 1 DRAM	RA0-RA8	$\overline{\text{RASH}}$	
512K – one row 256K × 4 DRAM	**RA0-RA8**	**N.C.**	Supplied by SN74BCT2425
1M – two rows 256K × 4 DRAM	**RA0-RA8**	**$\overline{\text{RASH}}$**	
2M – one row 1M × 1 DRAM	RA0-RA9	N.C.	Supplied by SN74BCT2425
4M – two rows 1M × 1 DRAM	RA0-RA9	$\overline{\text{RASH}}$	
2M – one row 1M × 4 DRAM	**RA0-RA9**	**N.C.**	Supplied by SN74BCT2425
4M – two rows 1M × 4 DRAM	RA0-RA9	$\overline{\text{RASH}}$	
8M – one row 4M × 1 DRAM	RA0-RA10	RA10	Need to enable RA10 at 'ACT2441

NOTE: Items highlighted in **bold** are DRAM configurations recommended by Apple Computer and Texas Instruments for purposes of direct connection, ease of hookup, and meeting capacitive load requirements without the possible need for additional external buffers.

N.C. = no connection needed at either SN74BCT2425 A20-A19 lines or DRAM array.

A 'row' of DRAM indicates a 16-bit wide row of devices, while the total size of RAM is given in K-bytes (K) or M-bytes (M).

interfacing to DRAM using discrete transceiver components

The discrete transceiver interface diagram shown previously in Figure 1 will support up to 8M-byte total DRAM expansion as shown.

For 512K-byte, 1M-byte, 2M-byte or 4M-byte DRAM interfacing, configured in either one or two 16-bits rows, a third SN74ALS258 multiplexer is needed to supply the RA8 and RA9 signals. For an 8M-byte DRAM configuration in a single 16-bit row of DRAM, the third multiplexer can supply the RA8, RA9, and RA10 signals or the 'ACT2441 can optionally be configured to supply RA10 via the $\overline{\text{RASH}}$(RA10) line.

addressing 'ACT2441 control registers

The 'ACT2441 utilizes programmable registers for control of operations such as interrupts, programmable timer, and the 12-bit address extension registers for communicating with NuBus™. Some registers are read only while others contain read-back capability to allow the current value to be read. The address mapping of these control registers is shown in Table 4.

24-bit MC68000 and 32-bit NuBus™ addressing notes

24-bit MC68000 addressing is viewed on the local bus of the NuBus™ expansion card. Use this address when addressing the 'ACT2441 from the local bus. Only A23-A19, A2, and A1 are actually used for address decoding when the 'ACT2441 is addressed from the local bus.

32-bit NuBus™ addressing is viewed from the $\overline{\text{AD}}$x lines of the NuBus™. Use the provided addresses when addressing the 'ACT2441 through the NuBus™. Only $\overline{\text{AD}}$31-$\overline{\text{AD}}$19, and $\overline{\text{AD}}$2-$\overline{\text{AD}}$0 are actually used for address decoding when the 'ACT2441 is addressed from the NuBus™. Note that the $\overline{\text{TM}}$x lines (along with $\overline{\text{AD}}$1-$\overline{\text{AD}}$0) are used to specify byte and halfword lane requirements.

'Fs' defines the 32-bit mode of addressing the 'ACT2441 through the NuBus™. The value 'F' must always be present on $\overline{\text{AD}}$31-$\overline{\text{AD}}$28 for NuBus™ slot accesses in the Macintosh II memory map. The 's' equals the NuBus™ slot ID value placed on $\overline{\text{AD}}$27-$\overline{\text{AD}}$24 (a 4-bit value of $9 to $E on the Macintosh II) used to address each of the six slots in the Macintosh II chassis.

Table 4. 'ACT2441 Control Register Address Map

32-BIT ADDR	24-BIT	32-BIT ADDR	24-BIT	FUNCTION
$Fs†	$F00000-†	$Fs†	$FFFFFF†	ROM (with 2 256K ROMs, 64KB)
		$Fs	$F00000	ROM Write – Place MC68000 in soft RESET
$Fs	$E00000-‡	$Fs	$EFFFFF‡	Reserved for Apple Manufacturing Test ROM (off card) when Shared Register Enable = False (SRE bit = 0)
$Fs	$D00000-	$Fs	$EFFFFF	NuBus™ access via I/O Extension register set when Shared Register Enable = True (SRE bit = 1)
		$Fs	$CA000E	**Read UPPER Byte** – Set NMRQ master mode
		$Fs	$CA000C	**Read UPPER Byte** – Clear NMRQ master mode
		$Fs	$CA000A	**Read UPPER Byte** – Set Interrupt IOP request
		$Fs	$CA0008	**Read UPPER Byte** – Clear Interrupt IOP request
		$Fs	$C00006	**Read UPPER Byte** – Set Interrupt Host request
		$Fs	$C00004	**Read UPPER Byte** – Clear Interrupt Host request
		$Fs	$C00002	**Read UPPER Byte** – Clear Timer Interrupt
		$Fs	$C00000	**Read UPPER Byte** – Clear soft RESET
		$Fs	$CA000F	**R/W LOWER Byte** – DTACK Control Register 1
		$Fs	$CA000D	**R/W LOWER Byte** – DTACK Control Register 0
		$Fs	$CA000B	**R/W LOWER Byte** – Programmable timer high byte
		$Fs	$CA0009	**R/W LOWER Byte** – Programmable timer low byte
		$Fs	$C00007	**R/W LOWER Byte** – I/O Addr latch D4-D7 mapped to AD20-AD23
		$Fs	$C00005	**R/W LOWER Byte** – I/O Addr latch D0-D7 mapped to AD24-AD31
		$Fs	$C00003	**R/W LOWER Byte** – CPU Addr latch D4-D7 mapped to AD20-AD23
		$Fs	$C00001	**R/W LOWER Byte** – CPU Addr latch D0-D7 mapped to AD24-AD31
		$Fs	$CA000E	**Word** – undefined
		$Fs	$CA000C	**Word** – undefined
		$Fs	$CA000A	**Read Word** – MCP Status, XDMA pins (D0-D2), always low (D3), Status of programmed reset, through $\overline{68KRST}$ (D4), Status of NuBus™ RESET (D5) and last TMx (D6-D7)
		$Fs	$CA0008	**R/W Word** – DMA control byte in low byte
		$Fs	$C00006	**Read Word** – Current high byte timer value in low byte
		$Fs	$C00004	**Read Word** – Current low byte timer value in low byte
		$Fs	$C00002	**R/W Word** – TI Test Configuration register
		$Fs	$CA0000	**Read Word** – Int/Slot in low byte (4-bits each)
$Fs†	$A00000-	$Fs	$BFFFFF	NuBus™ (Within programmable DTACK range)
$Fs	$800000-	$Fs	$9FFFFF	I/O Interface Logic (Within program DTACK range)
$Fs	$600000-	$Fs	$7FFFFF	RAM / I/O Interface Logic (Within program DTACK range)
$Fs	$400000-	$Fs	$5FFFFF	RAM / I/O Interface Logic (Within program DTACK range)
$Fs	$200000-	$Fs	$3FFFFF	RAM / I/O Interface Logic (Within program DTACK range)
$Fs	$000000-	$Fs	$1FFFFF	RAM (2M DRAM). Never any WAIT STATES

† $ denotes a hexidecimal number.

‡ This address range is reserved by Apple Computer for an off-card manufacturing test ROM when the Shared Register Enable bit of the DMA Control register (R/W word at CA0008) is set false (SRE bit = 0).

WARNING: Please note the specific address and addressing methods used to access the 'ACT2441 control registers. There are differences in both the physical address used, $CAxxxx verses $C0xxxx, as well as the access size, Read UPPER Byte, R/W LOWER Byte, R/W WORD, etc. Both the address and the byte/word size determine which control register is finally accessed. Please note the ENTIRE method used to access a particular register when writing software. This will avoid accessing the wrong control register.

NOTE: While various methods of reading and writing 'ACT2441 control registers are used, all perform single 8-bit (byte) operations within the device. The various size R/W operations are used to allow separation of control functions without utilizing additional local address space.

Read, Write, or R/W Byte control register operations from NuBus™ always use NuBus™ byte lane 3 ($\overline{AD}1$ low, $\overline{AD}0$ low) for control register operations at the higher addressed location of a control pair (i.e., Address A1 high) and NuBus™ byte lane 1 ($\overline{AD}1$ high, $\overline{AD}0$ low) for the lower addressed location of a control pair (i.e., Address A1 low). When communicating with these registers, be sure to place the data in the proper byte lane for the NuBus™ transfer.

Read or R/W Word control register operations always use NuBus™ halfword 1 lane ($\overline{AD}1$ high, $\overline{AD}0$ low, upper 16-bits) for the the higher addressed location of a control pair (i.e., Address A1 high) and NuBus™ halfword 0 lane ($\overline{AD}1$ high, $\overline{AD}0$ low, lower 16-bits) for the lower addressed location of a control pair (i.e., Address A1 low). Data is always conveyed in the most-significant byte of the halfword (byte-3 for halfword-1 and byte-1 for halfword-0). When communicating with these registers, be sure to place the data in the most significant byte of the proper halfword lane for the NuBus™ transfer.

addressing value notes

Notice that the addresses provided to access 'ACT2441 registers are not quite consistent with the physical addressing bits used for decoding the 'ACT2441. There are good reasons for this:

The value of bit 19 is always duplicated in bit 3 and bit 17 in the table provided. An example of this can be seen in the address value for 'Set NMRQ master mode'. It is stated as $CA000E but could as easily have been decoded with $C80006 (bit 17 and bit 3 = 0).

The reason for duplicating bit 19 in bits 3 and 17 is two-fold:

a) By making bit 17 track bit 19, the address is already valid if the DRAM memory configuration of 256K bytes in two rows of 64Kx4 DRAM is used (where A19 of the 'ACT2441 must be tied to A17 of the MC68000 bus to properly decode the second row). However, this is a nonrecommended configuration, but it is there anyway.

b) By making bit 3 match bit 19, the table creates a unique control register address for all registers within a group, byte operations, or word operations. Without this addition, the address value itself would be duplicated within a group and the designer or technician would have to inspect the transfer mode to determine which register was being accessed. As shown, the unique value allows quicker identification of the register addressed.

Of course, the designer may delete the tracking of bit 19 for bits 17 and 3, if desired, as long as 256K DRAM in two rows will not be used.

data bus notes

Remember that the 'ACT2441 control registers are only addressed with 8 bits of data. When forming data values, be sure to read and write the 8-bit value in the proper byte lane (lane 3 or 1) as described above for both byte and halfword operations. Table 5 reviews NuBus™ data layout and the $\overline{AD}1$-$\overline{AD}0$ line values during byte or halfword transfers ($\overline{AD}1$-$\overline{AD}0$ along with $\overline{TM}1$-$\overline{TM}0$ define the NuBus™ transfer mode).

EXAMPLES

R/W lower Byte at $FsC0 0007 from NuBus™ uses byte lane 3 and $FsC0 0005 uses byte lane 1.

R/W Word at $FsC0 0002 from NuBus™ uses halfword 1 lane, byte-3 and Read Word $FsC0 0000 uses halfword 0 lane, byte 1.

Table 5. NuBus™ Data Addressing

Bit 31 … Bit 0

NuBus™ Word				
Control†	Halfword 1†		Halfword 0†	
	Byte 3†	Byte 2	Byte 1†	Byte 0
$\overline{AD1}$	L	L	H	H
$\overline{AD0}$	L	H	L	H

†The $\overline{AD1}$-$\overline{AD0}$ line values are the same value for byte-3/halfword-1 transfers and for byte-1/halfword-0 transfers. The complete transfer mode is defined by the $\overline{TM1}$-$\overline{TM0}$ lines along with $\overline{AD1}$-$\overline{AD0}$ lines defining Read or Write mode as well as byte, halfword, or word operations. Please refer to the NuBus™ specification for further details.

NuBus™ address space (CPU and I/O address extension latches)

Access to the 32-bit NuBus™ address space from the 'ACT2441 is provided by two 12-bit address extension registers. One set for I/O space device access to NuBus™ (I/O Address Latch) while the other is used as the extension register for CPU-initiated NuBus™ operations (CPU Address Latch). The most significant 12 bits of the NuBus™ address should be placed in these registers before accessing the NuBus™ address space. Control of which extension register is used for a particular address range is controlled by bit-0, Shared Register Enable, of the DMA Control Register at the word location $CA0008, discussed in a future section.

The registers are located at byte locations $C00001 and $C00003 for the CPU extension register and $C00005 and $C00007 for the I/O extension register (as viewed in 24-bit local bus mode). The lower 4 bits of each respective 12-bit extension register address is stored in bits 7-4 of the register at $C00003 and $C00007. The upper 8 bits of each respective 12-bit extension register address is stored in the bits 7-0 of the byte at locations $C00001 and $C00005. The I/O Processor (IOP, MC68000, or other I/O processor) provides a 20-bit address (Address bits 19-0) when addressing NuBus™, the 'ACT2441 12-bit extension registers fill in the remainder of the 32-bit NuBus™ address. Write to these registers to store the extension register values or read from them to obtain the currently programmed extension register values.

In addition, A20 in the address field (not used for the address calculation into the 'ACT2441 control registers) is used by the hardware to perform a read-modify-write cycle (RMW). Whenever a Test-and-Set (TAS) instruction is executed, A20 must be set true. A20 should be set false for all other operations.

NOTE: A DRAM refresh cycle is always performed between the read and the write operation of the RMW (read-modify-write) cycle of a Test-and-Set operation by the chip to NuBus™.

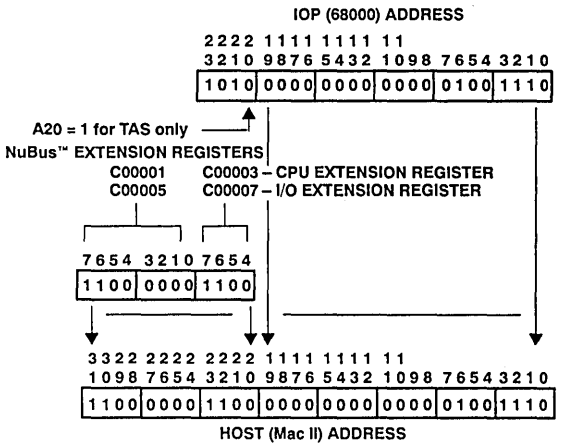


Figure 6. IOP (I/O Processor) to NuBus™ Address Translation

programmable timer

An internal 16-bit timer is provided on-chip and is decremented every 25.6 μs. When the counter reaches zero, it is reloaded with the value in the timer holding register on the next clock tick (25.6 μs) and a timer interrupt is generated. The action of this interrupt can be seen as a level-1 interrupt at the 'ACT2441 $\overline{IPL}$ lines and the upper nibble of the byte returned by a read word at location $C00000 (interrupt and slot record register). This interrupt is cleared by Clear Timer Interrupt via execution of a byte read of location $C00002.

NOTE: If this interrupt is ignored and the timer "ticks" (goes to zero) again, a clock tick is lost.

The 16-bit counter preload value is stored in locations $CA000B (high byte) and $CA0009 (low byte) of the 'ACT2441 using a Write Lower Byte operation. Remember that all data passed to/from the 'ACT2441 and the local bus are transferred on the lower byte data lines D7-D0.

The current value of the 16-bit countdown timer can be read in the low bytes of the word read of locations $C00006 (high byte) and $C00004 (low byte). These two registers are set to zero (0) upon the application of a hardware reset to the chip.

NOTE: The timer can change between the reading of either half of the timer value and reading the other half. Therefore, the values should be read twice (comparing for equal values) to ensure that the correct value is read. A suggested method is:

1) READ MSByte, save value
2) READ LSByte, save value
3) READ MSByte again
4) Compare saved MSByte value to most recent MSByte value
5) Do they match?
   YES: Continue with program
   NO: Go to step 1.

soft reset

The IOP (MC68000) can be placed in "soft reset" by writing a byte to location $F00000 from NuBus™ (any write to $FXXXXX will place the MC68000 in "soft reset", but only a byte write to $F00000 should be used (this is normally a ROM space write operation). The 'ACT2441 may be taken out of "soft reset" by executing an upper byte read at location $C00000 (any upper byte access to $CXXXXX will take the MC68000 out of "soft reset", but only an upper byte read of $C00000 should be used).

NOTE: When NuBus™ resets (i.e., $\overline{RESET}$ on NuBus™ goes low), the MC68000 comes out of "soft reset".

Upon power-on reset (NuBus™ reset), the first four accesses by the MC68000 (i.e., the execution address and the stack pointer) are fetched from the first four ROM locations. Under "soft reset", the address and stack pointer are fetched from RAM, starting at location $000000.

All internal registers are cleared upon power-on reset (via the NuBus™ reset signal $\overline{\text{RESET}}$ connected to the $\overline{\text{RESET}}$ line of the 'ACT2441), these registers are not altered by placing the chip in "soft reset".

NOTE: The start-up address vector in location 2 of the ROM must point to ROM address space ($F00000-$FFFFFF).

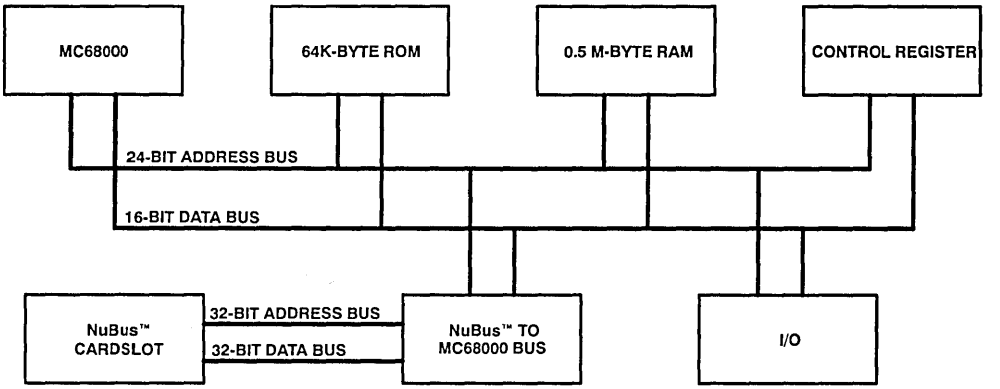


Figure 7. System Block Diagram Showing Data Paths

interrupts

Three local bus (MC68000) interrupts are provided in the 'ACT2441, one for the programmable timer, one for the NuBus™ interface, and one for the I/O interface. In addition, the IOP (I/O processor) may interrupt the NuBus™ channel. The priorities are as follows:

Interrupt	$\overline{\text{IPL}}$ Level
From the Programmable Timer	1
From NuBus™	2
From the I/O Interface	3
From the IOP	N/A (seen at NuBus™ $\overline{\text{NMRQ}}$ line)

Timer Interrupt: When the programmable timer's counter reaches zero, a timer interrupt is generated. This interrupt is cleared by Clear Timer Interrupt via execution of a byte read of location $C00002. The action of this interrupt can be seen as a level-1 interrupt at the 'ACT2441 $\overline{\text{IPL}}$ lines as well as reflected in the $\overline{\text{TMRIR}}$ bit of the upper nibble of the byte returned by a read word at location $C00000 (Interrupt and Slot ID register).

NuBus™ Interrupt: The host CPU (NuBus™ channel, in this case) can interrupt the IOP by executing Set Interrupt IOP Request by reading the upper byte at location $CA000A. This interrupt is cleared by the MC68000 Clear Interrupt IOP Request when reading the upper byte at location $CA0008. The action of this interrupt can be seen as a level-2 interrupt at the 'ACT2441 $\overline{\text{IPL}}$ lines as well as reflected in the $\overline{\text{IOPIR}}$ bit of the upper nibble of the byte returned by a read word at location $C00000 (Interrupt and Slot ID register).

I/O Interface Interrupt: The I/O interface can interrupt the MC68000 processor by asserting the $\overline{\text{IOIR}}$ interrupt to the 'ACT2441 (asserted externally on 'ACT2441 input $\overline{\text{IOIR}}$). $\overline{\text{IOIR}}$ must remain asserted until the software resets this interrupt request via the local bus hardware circuits asserting the interrupt. The action of this interrupt can only be seen as a level-3 interrupt at the 'ACT2441 $\overline{\text{IPL}}$ lines.

IOP Interrupting Host Across NuBus™: The IOP (68K or auxiliary processor) can interrupt the host (across NuBus™ via the 'ACT2441 asserting $\overline{\text{NMRQ}}$) by executing Set Interrupt Host Request, reading the upper byte at location $C00006. This interrupt is cleared via Clear Interrupt Host Request by the host reading the upper byte at location $C00004. The action of this interrupt can be seen at the NuBus™ $\overline{\text{NMRQ}}$ line as well as reflected in the $\overline{\text{HSTIR}}$ bit of the upper nibble of the byte returned by a read word at location $C00000 (Interrupt and Slot ID register).

NMRQ Master Mode: The IOP can be placed in NMRQ master mode via Set NMRQ Master Mode by executing an upper byte read of location $CA000E and taken out of this mode by executing an upper byte read of location $CA000C, Clear NMRQ Master Mode. The status of this mode is reflected in the NMRMD bit of the upper nibble of the byte returned by a read word at location $C00000 (Interrupt and Slot ID register).

When the IOP is placed in the NMRQ master mode (allowing NuBus™ to interrupt the IOP via the $\overline{\text{NMRQ}}$ line), a NuBus™ channel interrupt (level 2) is generated to the local bus when an external NuBus™ device asserts $\overline{\text{NMRQ}}$. NMRQ master mode allows a NuBus™ backplane-only system to operate with NMRQ interrupts, commonly used on unintelligent NuBus™ cards. The action of this interrupt can only be seen as a level-2 interrupt at the 'ACT2441 $\overline{\text{IPL}}$ lines. It cannot be seen in the status bits of the Interrupt and Slot ID register. Only the mode status is reflected in that bit.

Optionally, if both a Set Interrupt Host Request and Set NMRQ Master Mode are executed at the same time (by reading the upper byte at location $C00006 and $CA000E respectively) the IOP Interrupt bit of the Interrupt and Slot ID Register at word read location $C00000 will be set (made 'True', $\overline{\text{IOPIR}}$ = 0 in this case) by either external interrupt line $\overline{\text{IOIR}}$ or $\overline{\text{NMRQ}}$ of the 'ACT2441. This allows the user to use the $\overline{\text{IOPIR}}$ bit as a separate "soft" interrupt or as a polled interrupt when in NMRQ master mode. Please be aware that when this optional mode is invoked, the difference between the two interrupts cannot be identified. The $\overline{\text{IOPIR}}$ bit will be 'True' ($\overline{\text{IOPIR}}$ = 0) when either interrupt occurs.

NOTE: Due to the active-low operation of the interrupt status bits (upper nibble, bit 7-4 of the interrupt and slot ID register accessed by a read word at $C00000), confusion can result concerning the terms "set", "clear", "true", and "false". When an interrupt is "set" or made "true", the logic level of the inverted bit ($\overline{\text{NMRMD}}$, $\overline{\text{TMRIR}}$, $\overline{\text{IOPIR}}$, or $\overline{\text{HSTLR}}$) is "0". When an interrupt is "cleared" or "false", the inverted bit is "1".

Table 6 outlines the bit function of the Interrupt and Slot ID Register and Table 7 summarizes the interrupt modes available with the 'ACT2441 MCP NuBus™ Controller.

Table 6. Bit Functions of Interrupt and Slot ID Register

BIT	FUNCTION	NOTES
7	NMRQ Master Mode ($\overline{\text{NMRMD}}$)	Active-low, '0' = NMRQ Master Mode enabled
6	Timer Interrupt ($\overline{\text{TMRIR}}$)	Active-low, '0' = Timer Interrupt has occurred
5	IOP Interrupt ($\overline{\text{IOPIR}}$)	Active-low, '0' = IOP Interrupt has occurred
4	Host Interrupt ($\overline{\text{HSTIR}}$)	Active-low, '0' = Host Interrupt has occurred
3	NuBus™ slot ID bit 3	Active-high, current NuBus™ slot EXAMPLE: NuBus™ slot 6 reads 0110 binary
2	NuBus™ slot ID bit 2	
1	NuBus™ slot ID bit 1	
0	NuBus™ slot ID bit 0	

Table 7. Interrupt Possibilities

INTERRUPT TYPE	IPL INTR. LEVEL	INTR. STATUS	NOTES
Timer to IOP	1	TMRIR	
NuBus™ to IOP	2	IOPIR	
I/O Interface to IOP	3	None	
IOP to NuBus™	None	HSTIR	Also seen at NMRQ
NMRQ Master Mode (NuBus™ to IOP via NMRQ line)	2	NMRMD (mode only)	Cannot determine that NuBus™ caused NMRQ interrupt from Status Register bits
NMRQ Master Mode and SET INTR HOST REQ	2	NMRMD (mode only) IOPIR occurred	Cannot distinguish NMRQ and Set Intr Host Request and IOPIR or IOIR interrupts. This bit is good for interrupt polling.

acquiring the local bus

The following section discusses how to acquire the local memory bus on the NuBus™ expansion card. Access is gained via control registers within the MCP controller, which define how several programmable features are to operate, such as DTACK and the use of the XBUS lines.

DMA control register (R/W word at $CA0008)

The DMA Control Register (a read or write to the word at $CA0008) allows configuration of the two 12-bit NuBus™ extension registers and control over the XBR, XBG and XBGACK lines. The three external DMA pins (XBR, XBG, and XBACK) allow external devices to take over the local MC68000 bus as a third bus master. In addition to allowing a third local bus master, these pins can alternately be used for general-purpose I/O functions if the DMA feature is not required. When configured as external DMA lines (XDE control bit cleared to 0, the default), the alternative control settings for XBR, XBG, and XBACK are ignored. Table 8 describes the control bit positions within the DMA Control Register.

Table 8. DMA Control Register Summary (R/W) Word at $CA0008

BIT	FUNCTION	NOTES
7 6	XBG Mode	Input, output, or memory-mapped address decode for address range $800000-$9FFFFF
5 4	XBR Mode	Input, output, or memory-mapped address decode for address range $600000-$7FFFFF
3 2	XBACK Mode	Input, output, or memory-mapped address decode for address range $400000-$5FFFFF
1	XDE, External DMA Enable	Default = 0, enabled as DMA control lines
0	SRE, Shared Register Enable	Default = 0, nonshared mode

D0 – shared register enable (SRE)

Allows both sets of NuBus™ extension register to be accessed by both the MC68000 and the external bus master. When operating in the shared mode, the CPU Extension Register set (stored at locations $C00001 and $C00003) is always used for NuBus™ accesses to addresses $AXXXXX and $BXXXXX, the I/O Extension Register set (stored at locations $C00005 and $C00007) is always used for NuBus™ access to addresses $DXXXXX and $EXXXXX, independent of which local DMA master makes the access. In the nonshare mode (the default, bit D0=0), the CPU Extension Register set is always used for MC68000 accesses to NuBus™ and the I/O Extension Register set is always used for external DMA master accesses to NuBus™. In nonshared mode, the address range $E00000-$EFFFFF is reserved by Apple Computer for a manufacturing test ROM, residing off card, leaving the address range $D00000-$DFFFFF for external DMA master NuBus™ access using the I/O Extension register.

D1 – external DMA enable ($\overline{XDE}$)

Defines if the $\overline{XBR}$, $\overline{XBG}$ and $\overline{XBACK}$ lines are used to provide access to a third local bus master (NuBus™ and the MC68000 being the first two) or if the lines will be used as general-purpose I/O or address decode lines. The default mode is the $\overline{XDE}$ bit enabled (bit D1 = 0). When enabled, the $\overline{XBR}$, $\overline{XBG}$, and $\overline{XBACK}$ lines act as DMA access control lines. When external DMA is disabled ($\overline{XDE}$ bit D1 = 1), these three pins can be defined as inputs, outputs, or memory-mapped address-decode lines according to the following definitions of two control bits for each line as shown in Table 9.

Table 9. Controlling XDMA Mode Functions

BIT		MODE
MSB	LSB	
0	0	Line is an input
1	0	Address Range Decode Line
X	1	Output of level "X"

NOTE: MSB = most significant bit of the two-bit pair (bits 3, 5, and 7) and LSB = least significant bit of the two-bit control pair (bits 2, 4, and 6).

XBACK mode, bits D3 and D2

When the $\overline{XDE}$ control bit is set to 1, these two bits control how the XBACK bit will be used. Table 9 shows the possible configurations. The mode of this line is independent of the other two XDMA pins.

XBR mode, bits D5 and D4

When the $\overline{XDE}$ control bit is set to 1, these two bits control how the XBR bit will be used. Table 9 shows the possible configurations. The mode of this line is independent of the other two XDMA pins.

XBG mode, bits D7 and D6

When the $\overline{XDE}$ control bit is set to 1, these two bits control how the XBG bit will be used. Table 9 shows the possible configurations. The mode of this line is independent of the other two XDMA pins.

MCP status register (R/W word at $CA000A)

The status of the XDMA pins, as well as several other lines, may be read at any time (independent of the $\overline{XDE}$ bit mode) via the MCP Status register, the word read at location $CA000A. Table 10 shows the individual status bits available.

Table 10. MCP Status Register (Read Word at $CA000A)

BIT	FUNCTION	NOTES
7	Last $\overline{TM1}$ returned from NuBus™	Latched $\overline{TM1}$ value
6	Last $\overline{TM0}$ returned from NuBus™	Latched $\overline{TM0}$ value
5	Status of $\overline{RESET}$ from NuBus™	Actually delayed by four (4) 10-MHz clocks
4	Not used, always low (0)	
3	Not used, always low (0)	
2	Status of $\overline{XBACK}$ line	Current state of this line, 1 or 0
1	Status of $\overline{XBG}$ line	Current state of this line, 1 or 0
0	Status of $\overline{XBR}$ line	Current state of this line, 1 or 0

programmable DTACK/VPA generation (DTACK control Reg 1 and 0)

Two registers control the operation of DTACK (Data Transfer Acknowledge) and VPA (Valid Peripheral Address) when accessing the expansion card's application address space ($200000-$9FFFFF). The 16 bits of the two DTACK Control Registers (accessible by the lower byte read or write at locations $CA000D, DTACK Control Register 0, and $CA000F, DTACK Control Register 1) are divided into four groups of four bits each. Each group corresponds with a 2M-byte address space. Upon initial reset, both DTACK control registers are cleared. $\overline{\text{DTACK}}$ may be synchronous or asynchronous to the 10-MHz clock (MHz 10) and is controlled by bit 5 of the 'ACT2441 Test Configuration register. The default mode is for $\overline{\text{DTACK}}$ to be synchronous to MHz 10. Table 11 shows the bit and address range breakdown.

NOTE: When a 2M-byte range above the first 2M space ($000000-$1FFFFF) is programmed as RAM space, the number of WAIT states programmed in DTACK Control Register 0 and 1 are ignored for that range. When a 2M space is programmed for RAM usage rather than general-purpose I/O, the internal RAM DTACK generator takes over for the programmed DTACK generator.

The MSB (most significant bit of each control nibble) of the three lower addressed control groups ($200000-$7FFFFF) defines that space as RAM space if set true "1". If set false "0", RAM is not decoded in this space and the space can be used for external I/O. For I/O space configuration, the remaining 3 bits of each control nibble define the number of wait states to be inserted for that address range, 0–5 = waits states, 6 = VPA, 7 = no DTACK. For 120-ns DRAM, no wait states are used. For slower STATIC RAM or I/O devices, program the appropriate number of wait states required with the address space programmed for I/O usage.

NOTE: During VPA configuration, the 'ACT2441 DOES NOT issue a separate interrupt level on the $\overline{\text{IPL0}}$-$\overline{\text{IPL1}}$ lines, which effectively is a NO interrupt condition at the MC68000 processor. If control of interrupts during MC6800 style VPA cycles is desired, then interrupts should be expanded as shown in Figure 3 to allow the addition of non-'ACT2441 interrupt sources for interrupt levels 4, 5, or 6. Optionally, a level 3 interrupt could be issued in conjunction with a VPA cycle from the 'ACT2441 by programming one or more of the 2M-byte areas from $200000 to $9FFFFF to issue VPA cycles, using DTACK Control Registers 0 or 1, and by externally pulling the $\overline{\text{IOIR}}$ input, I/O Interface Interrupt line, of the 'ACT2441 low via hardware circuits.

VPA cycles are issued only for accesses in specific address ranges when the 'ACT2441 is programmed for VPA cycles in those ranges using DTACK Control Registers 0 and 1. VPA cycles are only supported when the programmed address ranges are accessed from the MC68000 processor side of the expansion card, NOT from the NuBus™ channel. A level 3 interrupt is issued from the 'ACT2441 only in response to an external device taking the $\overline{\text{IOIR}}$ input line low. VPA and interrupt level 3 are separate actions, which may or may not be used in conjunction with each other. Level 1 or 2 interrupts CANNOT be issued from the 'ACT2441 in conjunction with VPA cycles because levelss 1 and 2 are preassigned for programmable timer and NuBus™ channel purposes.

NOTE: "Decoded as RAM space" implies that $\overline{\text{CAS}}$x and $\overline{\text{RAS}}$x will be active in this address range.

For the highest addressed control group ($800000-$9FFFFF), the lower three bits also define the number of wait states to be inserted for this range: 0–5 = waits states, 6 = VPA, 7 = no DTACK. For this control group, the MSB of the control nibble defines a RAM output mode. If true "1", the 'ACT2441 RASH output becomes RA10 out for DRAM usage (allowing 4M-bit DRAMs to be used), if false "0", the default mode RASH is a second $\overline{\text{RAS}}$ output for a second row of DRAM. This address space cannot be internally decoded for RAM space. It is only available for I/O interface logic usage.

NOTE: If the 2M- to 4M-byte ($200000-$3FFFFF) address space is defined as RAM address space (D7 true), address line A21 will be used internally within the 'ACT2441 to decode RASL/RASH, thus allowing the use of by-1M DRAMs. If the 2M- to 4M-bytes ($200000-$3FFFFF) address space is not defined as RAM space (i.e., defined as I/O space, D7 false) RASL/RASH will be decoded off of A19, thus allowing the use of by- 256K DRAMs.

Table 11. Programmable DTACK Control Register

CONTROL REGISTER	'ACT2441 ADDRESS	ADDRESS RANGE AFFECTED	BITS USED	FUNCTION
1	$CA000F	$800000-$9FFFFF	D3-D0	
			D3	**Defines RAM output mode.** If true '1', RASH line of 'ACT2441 is used for DRAM RA10 address line output. If false '0' (the default mode) RASH line is a second RAS output for two rows of DRAM.
			D2-D0	**Define number of wait states** 0-5 = Number of wait states 6 = Do VPA cycle when accessed 7 = No DTACK for address range
0	$CA000D	$600000-$7FFFFF	D7-D4	
			D7	**Defines RAM or I/O Space** If '1' define address space as RAM, if '0' defines as I/O space.
			D6-D4	**Define number of wait states** 0-5 = Number of wait states 6 = Do VPA cycle when accessed 7 = No DTACK for address range
0	$CA000D	$400000-$5FFFFF	D3-D0	
			D3	**Defines RAM or I/O Space** If '1' define address space as RAM, if '0' defines as I/O space.
			D2-D0	**Define number of wait states** 0-5 = Number of wait states 6 = Do VPA cycle when accessed 7 = No DTACK for address range
1	$CA000F	$200000-$3FFFFF	D7-D4	
			D7	**Defines RAM or I/O Space** If '1' define address space as RAM, if '0' defines as I/O space.
			D6-D4	**Define number of wait states** 0-5 = Number of wait states 6 = Do VPA cycle when accessed 7 = No DTACK for address range

chipset design and programming considerations

The following is a list of special considerations when using the 'ACT2441 NuBus™ controller chip. Where appropriate, each of these items has been mentioned in a note with the chipset usage descriptions. Being aware of these design and programming considerations will ensure a smoother design with a minimum of problems.

1. The programmable timer registers are nonlatching registers. The value of the timer could change between the reading of either half of the timer value and reading the other half. Therefore, the values should be read twice (comparing for equal values) to ensure that a valid value is read. A suggested method is:

    6) READ MSByte, save value
    7) READ LSByte, save value
    8) READ MSByte again
    9) Compare saved MSByte value to most recent MSByte value
    10) Do they match?
        YES: Continue with program
        NO: Go to step 1

2. A hardware anomaly exists whereby the 'ACT2441 drives the AD19 and AD2-AD0 lines during the period when START and ACK are driven high after a NuBus™ ATTN-NULL cycle. This places the current logic levels of A19 and A2-A1, which are in the high-impedance state at that moment, onto the AD19 and AD2-AD0 lines for 100 ns during the period just following the ATTN- NULL time. There is no actual harm done by this anomaly but it is documented here for completeness.
3. When the $\overline{68KRST}$ line is activated via the "hardware" method, its output is delayed by four 10-MHz clock cycles from the NuBus™ $\overline{RESET}$ signal from which it is derived.
4. When accessing the programmable 'ACT2441 control registers, please note that there are differences in both the physical address used, $CAxxxx verses $C0xxxx, as well as the access size, Read UPPER Byte, R/W LOWER Byte, R/W WORD, etc. Both the address and the byte/word size determine which control register is finally accessed. Please note the ENTIRE method used to access a particular register when writing software. This will avoid accessing the wrong control register.
5. All control registers of the 'ACT2441 communicate via byte values, independent of the access method used (i.e., Lower Byte, Upper Byte, or Word). Depending upon which control register is accessed, the byte information is communicated on either byte lane 1 or byte lane 3. Be sure to review carefully the section on "Addressing 'ACT2441 Control Registers", "Addressing Value Notes", and "Data Bus Notes" to learn which byte lane is used for a particular control register.

testing

The 'ACT2441 has several programmable testing modes as shown in the Table 12. All modes, except when at high impedance, are controllable from software by performing a write word to the register at location $C00002. The current state of the test register bits may be read by a read word at the same location (as with all 'ACT2441 control registers, only a single byte of information is available at each location but various byte/word accesses are used to distinguish the individual control registers). More than one mode may be active at one time as all test modes are individually bit-controlled. Placing all outputs and bidirectional lines in a high-impedance state is controlled via a hardware line sequence, which should only be used within controlled tester environments.

3-state output

All the output and bidirectional lines of the 'ACT2441 can be placed in the high-impedance state by performing a simple hardware line toggle. If the 'ACT2441 $\overline{ID0}$ line's state is ever changed after powerup and resetting of the device, the 'ACT2441 outputs and bidirectional lines will be at high impedance (The change can be from either state, 1 to 0 or 0 to 1). The mode is cleared by performing a hardware reset of the device with the $\overline{ID0}$ line in a static state, by bringing the $\overline{RESET}$ line momentarily low.

Since NuBus™ $\overline{IDx}$ lines are normally hardwired high or low to each slot of a NuBus™ backplane, there should be no chance of this abnormal toggle mode occurring and activating this test mode in normal chip usage at the system level. For manufacturing testing, the $\overline{ID0}$ line can be controlled by a test fixture to force entry into this mode.

TI test configuration register

The normal mode of operation for the 'ACT2441 is for the TI test configuration register to be cleared (that is all zeros). This is the default after a hardware reset to the 'ACT2441. The user modifiable bits are shown in Table 12.

WARNING: Those modes marked RESERVED are reserved for TI chip-level testing and are not to be written to or modified. Failure to respect the reserved nature of these bits will result in erratic and unpredictable operation.

Table 12. TI Test Configuration Register Control Bits (R/W Word at $C00002)

BIT	FUNCTION	NOTES
7	Reserved	Default = 0, normal operation
6	Enables swapping of $\overline{\text{RASH}}$ and $\overline{\text{RASL}}$ physical output pins	Default = 0, normal operation, $\overline{\text{RASH}}$ and $\overline{\text{RASL}}$ output on pins as specified in 'ACT2441 data sheet. If set to '1', swaps the physical output pins on which $\overline{\text{RASH}}$(RA10) and $\overline{\text{RASL}}$ are output. Useful for configuration of contiguous DRAM when only 2.5M bytes of DRAM is installed in board.
5	Enables asynchronous operation of $\overline{\text{DTACK}}$ line	Default = 0, normal mode is synchronous $\overline{\text{DTACK}}$ operation. Synchronous $\overline{\text{DTACK}}$ is synchronous to the MHZ10 clock output. If set to '1', enables asynchronous $\overline{\text{DTACK}}$ operation.
4	Reserved	Default = 0, normal operation
3	Reserved	Default = 0, normal operation
2	Reserved	Default = 0, normal operation
1	Reserved	Default = 0, normal operation
0	Reserved	Default = 0, normal operation

IMPORTANT NOTICE

The SN74ACT2441 has been designed in cooperation with Apple Computer using Texas Instruments Standard Cell ASIC Process. Each cell used in the 'ACT2441 has been fully characterized and incorporated into the ASIC simulation library. As a result, most of the propagation delay relationships shown in this data sheet are derived from simulation and are not specifically tested in production. The specifications shown in this data sheet are intended for design purposes, but they do not imply production testing.

Texas Instruments will supply the 'ACT2441 to Apple third party developers with devices that meet the same quality and reliability standards as devices delivered to Apple Computer. Texas Instruments and Apple Computer reserve the right to make changes in device or device specifications identified in this publication without notice. TI advises its customers to obtain the latest version of the device specifications to verify, before placing orders, that the information being relied upon by the customer is current.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 3) ..... −0.5 V to 7 V
Input voltage, any input ..... −0.5 V to 7 V
Voltage applied to a diabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... −0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond thoses listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 3: All voltage values are with respect to GND.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	$\overline{START}$, $\overline{ACK}$, $\overline{TM1}$, $\overline{TM0}$, $\overline{AD31}$-$\overline{AD19}$, $\overline{AD2}$-$\overline{AD0}$			−12	mA
		D0-D7, $\overline{UDS}$, $\overline{LDS}$, READ, $\overline{AS}$, $\overline{DTACK}$, $\overline{RASL}$, STCYC, $\overline{RASH}$, $\overline{RA9}$, $\overline{CASH}$, $\overline{CASL}$, RA0, MHZ10, $\overline{NBDOE}$			−10	
		All other outputs			−4	
I_{OL}	Low-level output current	$\overline{RQST}$ open-drain			60	mA
		$\overline{ARB0}$-$\overline{ARB3}$ open-drain			48	
		$\overline{NMRQ}$ open-drain			24	
		$\overline{START}$, $\overline{ACK}$, $\overline{TM1}$, $\overline{TM0}$, $\overline{AD31}$-$\overline{AD19}$, $\overline{AD2}$-$\overline{AD0}$			24	
		D0-D7, $\overline{UDS}$, $\overline{LDS}$, READ, $\overline{AS}$, $\overline{DTACK}$, $\overline{RASL}$, STCYC, $\overline{RASH}$, $\overline{RA9}$, $\overline{CASH}$, $\overline{CASL}$, RA0, MHZ10, $\overline{NBDOE}$			10	
		All other outputs			4	
f_{clock}	Clock frequency		0		10	MHz
t_{su}	Setup time	Any NuBus™ input before CLK75 high	17			ns
		Any 68K or XBUS input before MHZ10	20			
t_h	Hold time	Any NuBus™ input after CLK25, CLK75	5			ns
		Any 68K or XBUS input after MHZ10	5			
T_A	Operating free-air temperature		0		70	°C

NOTE 4: The SN74ACT2441 has been designed to support the loading and drive requirements of a 6-slot Macintosh II chassis. Consequently, the 'ACT2441 has been specified using a relaxed capacitance value (130 pF) and a relaxed AC performance requirement over a standard 16-slot NuBus™ interface as specified by the IEEE 1196-1987 NuBus™ specification.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	START, ACK, TM1, TM0, AD31-AD19, AD2-AD0	V_{CC} = 4.5 V, I_{OH} = – 12 mA	3	3.7		V
	D0-D7, UDS, LDS, READ, AS, DTACK, RASL, STCYC, RASH, RA9, CASH, CASL, RA0, MHZ10, NBDOE	V_{CC} = 4.5 V, I_{OH} = – 10 mA	3	3.7		
	All other nonopen-drain outputs	V_{CC} = 4.5 V, I_{OH} = – 4 mA	3	3.7		
V_{OL}	RQST open-drain	V_{CC} = 4.5 V, I_{OL} = 60 mA		0.35	0.5	V
	ARB0-ARB3 open-drain	V_{CC} = 4.5 V, I_{OL} = 48 mA		0.35	0.5	
	NMRQ open-drain	V_{CC} = 4.5 V, I_{OL} = 24 mA		0.35	0.5	
	START, ACK, TM1, TM0, AD31-AD19, AD2-AD0	V_{CC} = 4.5 V, I_{OL} = 12 mA		0.35	0.5	
	D0-D7, UDS, LDS, READ, AS, DTACK, RASL, STCYC, RASH, RA9, CASH, CASL, MHZ10, NBDOE	V_{CC} = 4.5 V, I_{OL} = 10 mA		0.35	0.5	
	All other outputs	V_{CC} = 4.5 V, I_{OL} = 4 mA		0.35	0.5	
I_{IH}‡		V_{CC} = 5.5 V, V_I = 5.5 V			20	µA
I_{IL}‡	DTACK, VPA	V_{CC} = 5.5 V, V_I = 0			– 801	µA
	XBR, XBG, XBACK, UDS, LDS, AS, READ, IOIR	V_{CC} = 5.5 V, V_I = 0			– 191	
	ID3-ID0, ARB3-ARB0, ACK, RQST, START, TM1, TM0, NMRQ	V_{CC} = 5.5 V, V_I = 0			– 11	
	All other inputs	V_{CC} = 5.5 V, V_I = 0			– 1	
I_{CCQ}	See Note 5	V_{CC} = 5.5 V, CLK25 and CLK75 = 10 MHz			250	µA
C_i	ID-ID3, RESET, FC0-FC1, CLK25, CLK75, BG, IOIR	V_I = 0		5.6		pF
C_o	RQST	V_O = 0		17.8		pF
	ARB3-ARB0	V_O = 0		16.6		
	HALT, 68KRST	V_O = 0		8		
	START, ACK, TM1, TM0, NMRQ, D0-D7, UDS, LDS AD31-AD19, AD2-AD0, READ, AS, DTACK, XBR, XBG, XBACK, A23-A19, A2-A1	V_O = 0		15		
	All other outputs	V_O = 0		12.7		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

NOTE 5: I_{CCQ} is specified with the device conditioned to the standby mode; e.g., inputs with pullups or pulldowns will be at V_{CC} or 0 V, respectively.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

NuBus™ card-slot signals†, C_L = 50 pF‡ (see Note 6)

PARAMETER		MIN	TYP§	MAX	UNIT
t_{pd}	Propagation delay time, CLK25 low to $\overline{ARBx}$			42	ns
t_{pd}	Propagation delay time, CLK25 low to $\overline{START}$			42	ns
t_{pd}	Propagation delay time, CLK25 low to $\overline{ACK}$			42	ns
t_{pd}	Propagation delay time, CLK25 low to $\overline{TMx}$			42	ns
t_{pd}	Propagation delay time, CLK25 low to $\overline{RQST}$			42	ns
t_{pd}	Propagation delay time, CLK25 low to $\overline{ADxx}$			42	ns

NOTE 6: The following NuBus™ switching characteristics are production tested against a 42 ns maximum using a 50-pF capacitive load. This guarantees a 47 ns maximum at 130 pF which more closely approximates a fully loaded 6-slot Macintosh II chassis.

MC68000 interface signals†, C_L = 50 pF‡

PARAMETER		MIN	TYP§	MAX	UNIT
t_{pd}	Propagation delay time, $\overline{AS}$ low to D7-D0			200	ns
t_{pd}	Propagation delay time, MHZ10 low to D7-D0	10			ns
t_{pd}	Propagation delay time, MHZ10 low to $\overline{VPA}$ low	20			ns
t_{pd}	Propagation delay time, MHZ10 high to $\overline{UDS}$ low			55	ns
t_{pd}	Propagation delay time, MHZ10 high to $\overline{AS}$ low			55	ns
t_{pd}	Propagation delay time, MHZ10 low to $\overline{UDS}$ high			65	ns
t_{pd}	Propagation delay time, MHZ10 low to $\overline{AS}$ high			65	ns
t_{pd}	Propagation delay time, MHZ10 high to $\overline{LDS}$ low			55	ns
t_{pd}	Propagation delay time, MHZ10 high to $\overline{AS}$ low			55	ns
t_{pd}	Propagation delay time, MHZ10 low to $\overline{LDS}$ high			65	ns
t_{pd}	Propagation delay time, MHZ10 low to $\overline{AS}$ high			65	ns
t_{pd}	Propagation delay time, CLK25 low to READ			50	ns
t_{pd}	Propagation delay time, CLK25 low to $\overline{AS}$			40	ns
t_{pd}	Propagation delay time, CLK25 low to $\overline{DTACK}$ low			30	ns
t_{pd}	Propagation delay time, $\overline{AS}$ high to $\overline{DTACK}$ high			50	ns
t_{pd}	Propagation delay time, CLK25 low to $\overline{BERR}$			40	ns
t_{pd}	Propagation delay time, CLK25 low to $\overline{HALT}$			40	ns
t_{pd}	Propagation delay time, CLK25 low to $\overline{68KRST}$			40	ns
t_{pd}	Propagation delay time, CLK25 low to Ax			50	ns
t_{pd}	Propagation delay time, CLK25 or CLK75 low to $\overline{IPLx}$			50	ns
t_{pd}	Propagation delay time, CLK25 low to $\overline{BR}$			45	ns
t_{pd}	Propagation delay time, CLK25 low to $\overline{BGACK}$			45	ns
t_{pd}	Propagation delay time, CLK25 low to $\overline{NBACK}$			45	ns
t_{pd}	Propagation delay time, CLK25 low to $\overline{XBR}$			50	ns
t_{pd}	Propagation delay time, CLK25 low to $\overline{XBG}$			50	ns
t_{pd}	Propagation delay time, $\overline{BG}$ to $\overline{XBG}$			50	ns
t_{pd}	Propagation delay time, CLK25 low to $\overline{XBACK}$			45	ns
t_{pd}	Propagation delay time, CLK25 low to MHZ10 high			12	ns
t_{pd}	Propagation delay time, CLK75 low to MHZ10 low			15	ns

† For 3-state outputs, the maximum propagation delay times shown are also valid for t_{en} and t_{dis} switching characteristics.

‡ See Parameter Measurement Information for load circuit and voltage waveforms.

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

buffer interface signals†, C_L = 50 pF‡

	PARAMETER	MIN	TYP§	MAX	UNIT
t_{pd}	Propagation delay time, CLK25 low to NBDIEL			50	ns
t_{pd}	Propagation delay time, CLK25 low to NBDIEH			50	ns
t_{pd}	Propagation delay time, CLK25 low to $\overline{NBDOE}$			29	ns
t_{pd}	Propagation delay time, CLK75 high to NBAIC high			20	ns
t_{pd}	Propagation delay time, CLK75 high to NBAIC low			30	ns
t_{pd}	Propagation delay time, CLK75 high to NBDIC high			20	ns
t_{pd}	Propagation delay time, CLK75 high to NBDIC low			30	ns
t_{pd}	Propagation delay time, CLK75 low to STCYC			27	ns

memory control signals†, C_L = 50 pF‡

	PARAMETER	MIN	TYP§	MAX	UNIT
t_{pd}	Propagation delay time, $\overline{AS}$, A21-A23 to $\overline{ROM}$			30	ns
t_{pd}	Propagation delay time, CLK75 low to $\overline{RASL}$	15			ns
t_{pd}	Propagation delay time, $\overline{ASTRB}$ low to $\overline{RASL}$			25	ns
t_{pd}	Propagation delay time, CLK75 low to $\overline{RASH}$	15			ns
t_{pd}	Propagation delay time, A19, A20 to RA10			30	ns
t_{pd}	Propagation delay time, $\overline{CAS}$x low to RA10	10			ns
t_{pd}	Propagation delay time, $\overline{AS}$ low to $\overline{RASH}$			25	ns
t_{pd}	Propagation delay time, CLK75 low to $\overline{CASH}$			25	ns
t_{pd}	Propagation delay time, CLK75 low to $\overline{CASL}$			25	ns
t_{pd}	Propagation delay time, CLK75 low to MUX			25	ns

† For 3-state outputs, the maximum propagation delay times shown are also valid for t_{en} and t_{dis} switching characteristics.

‡ See Parameter Measurement Information for load circuit and voltage waveforms.

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

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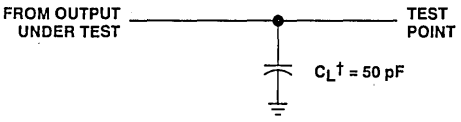
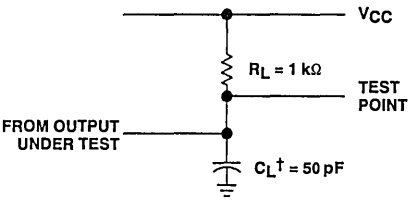
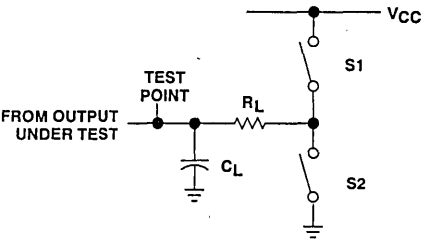
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT
TOTEM-POLE OUTPUTS

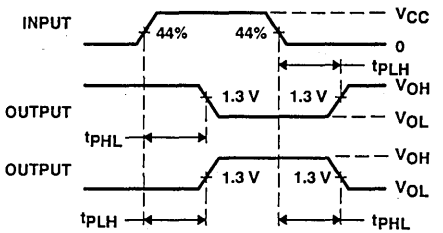


LOAD CIRCUIT
OPEN-DRAIN OUTPUTS

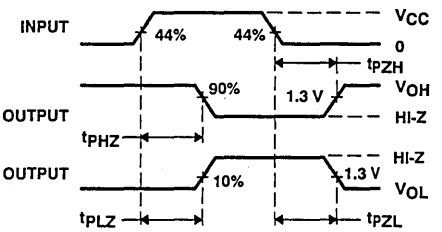


LOAD CIRCUIT
3-STATE OUTPUTS

PARAMETER		OUTPUT OR I/O		S1	S2
		R_L	C_L†		
t_{en}	t_{PZH}	1 kΩ	50 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Close
	t_{PLZ}			Closed	Open
t_{pd}	t_{PLH}	—	50 pF	Open	Open
	t_{PHL}				



OUTPUT AND 3-STATE BIDIRECTIONAL INPUT/OUTPUT
PROPAGATION DELAY TIME VOLTAGE WAVEFORMS

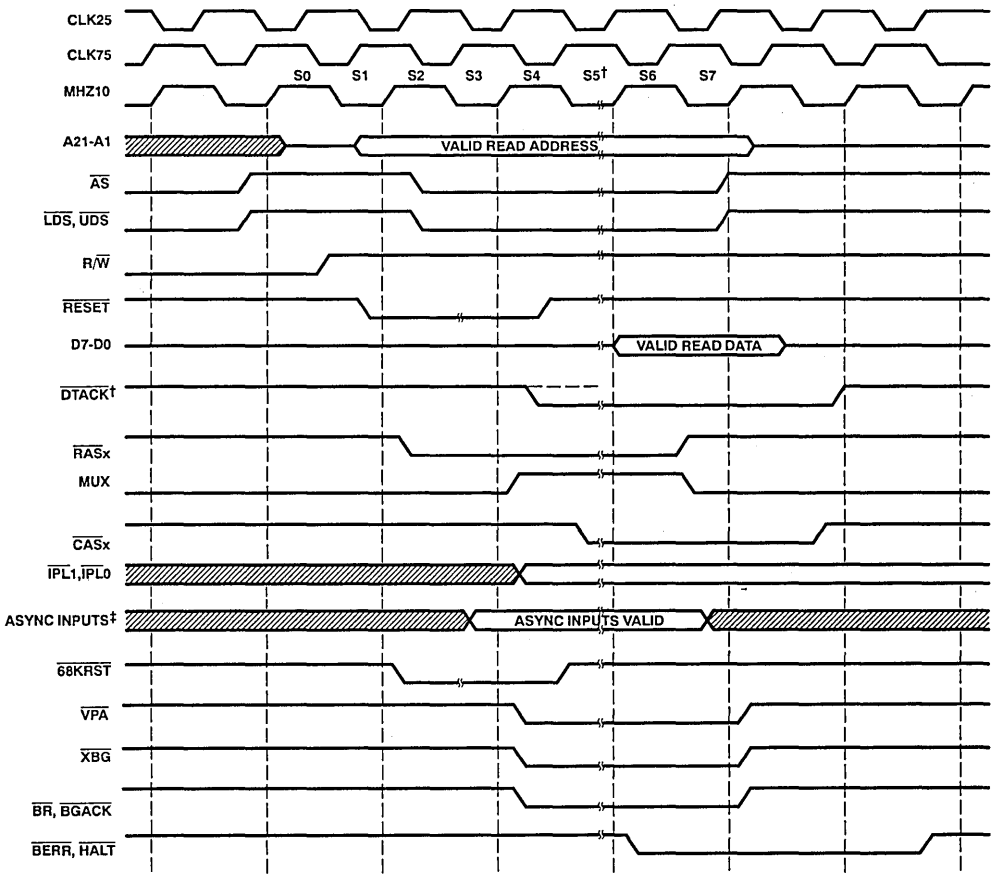


3-STATE
DISABLE AND ENABLE VOLTAGE WAVEFORMS

† C_L includes probe and test fixture capacitance.

Figure 8

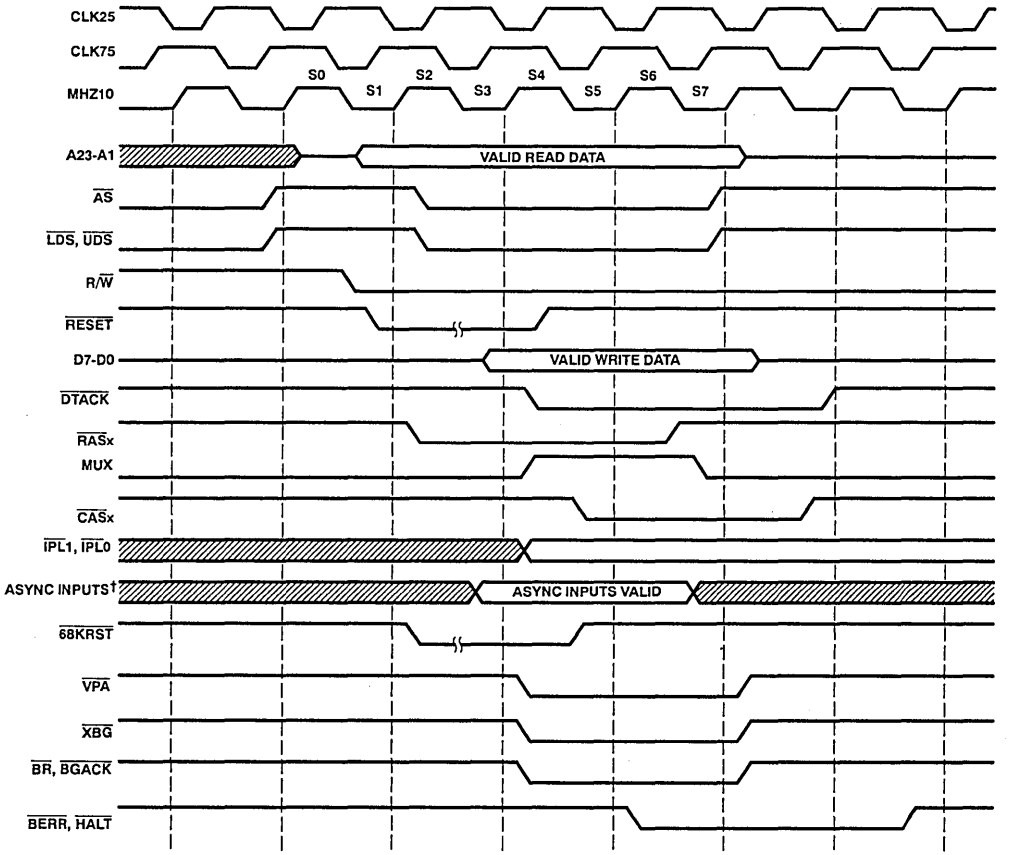
APPLICATION INFORMATION



† During ROM read cycles, one wait state is inserted by the 'ACT2441 MCP controller via DTACK.
‡ The timing diagram assumes the asynchronous inputs FC1-FC0, $\overline{BG}$, $\overline{XBR}$, $\overline{XBACK}$ and $\overline{IOIR}$ are recognized at the next falling CLK edge.

Figure 9. 68K Read Cycles

APPLICATION INFORMATION



† The timing diagram assumes the asynchronous inputs FC1-FC0, $\overline{BG}$, $\overline{XBR}$, $\overline{XBACK}$, and $\overline{IOIR}$ are recognized at the next falling CLK edge.

Figure 10. 68K Write Cycles

APPLICATION INFORMATION

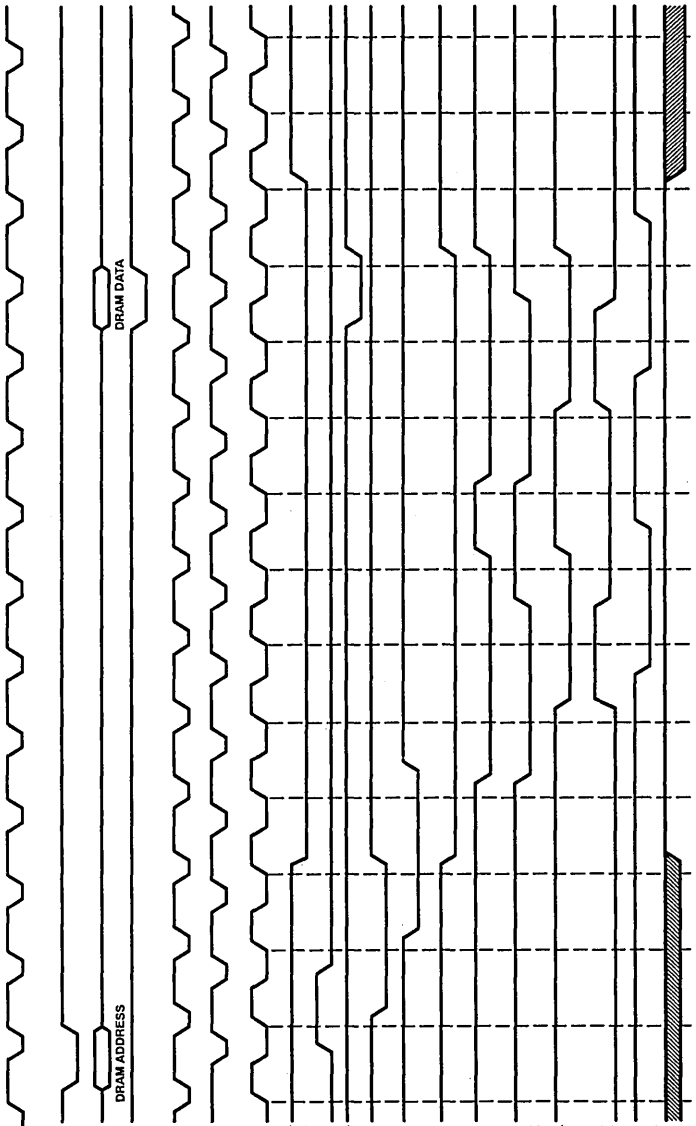


Figure 11. 32-Bit NuBus™ DRAM Read Cycle

APPLICATION INFORMATION

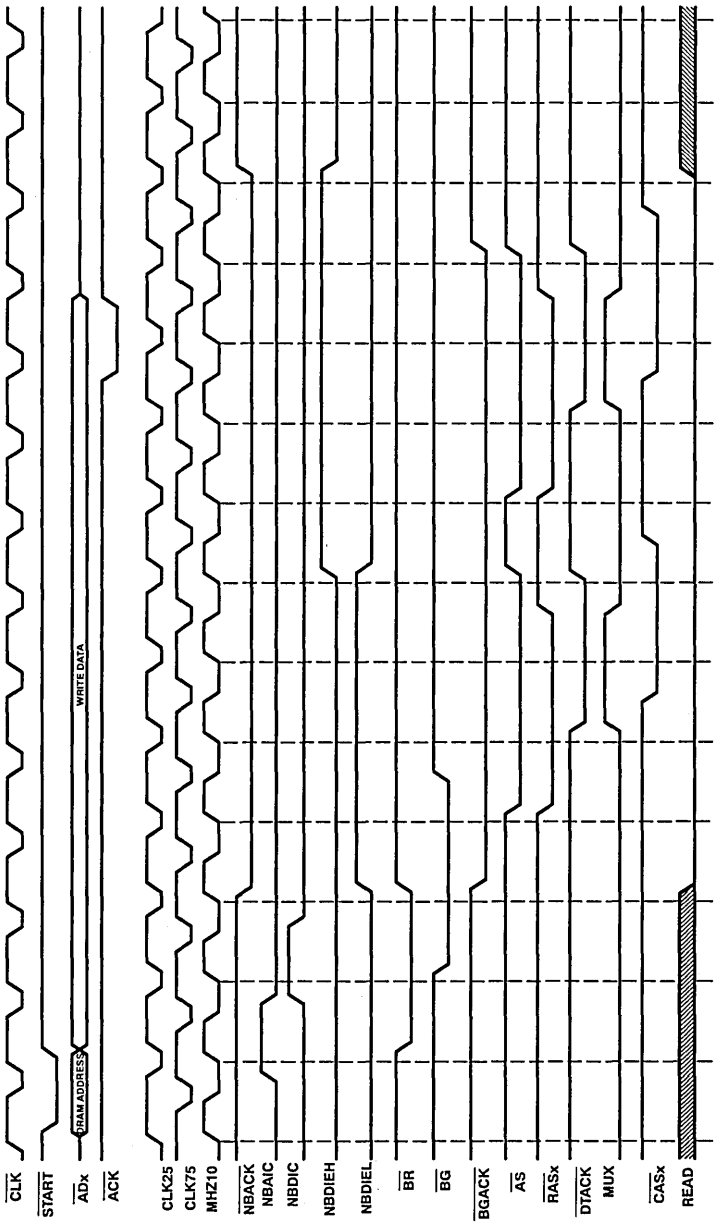


Figure 12. 32-Bit NuBus™ DRAM Write Cycle

APPLICATION INFORMATION

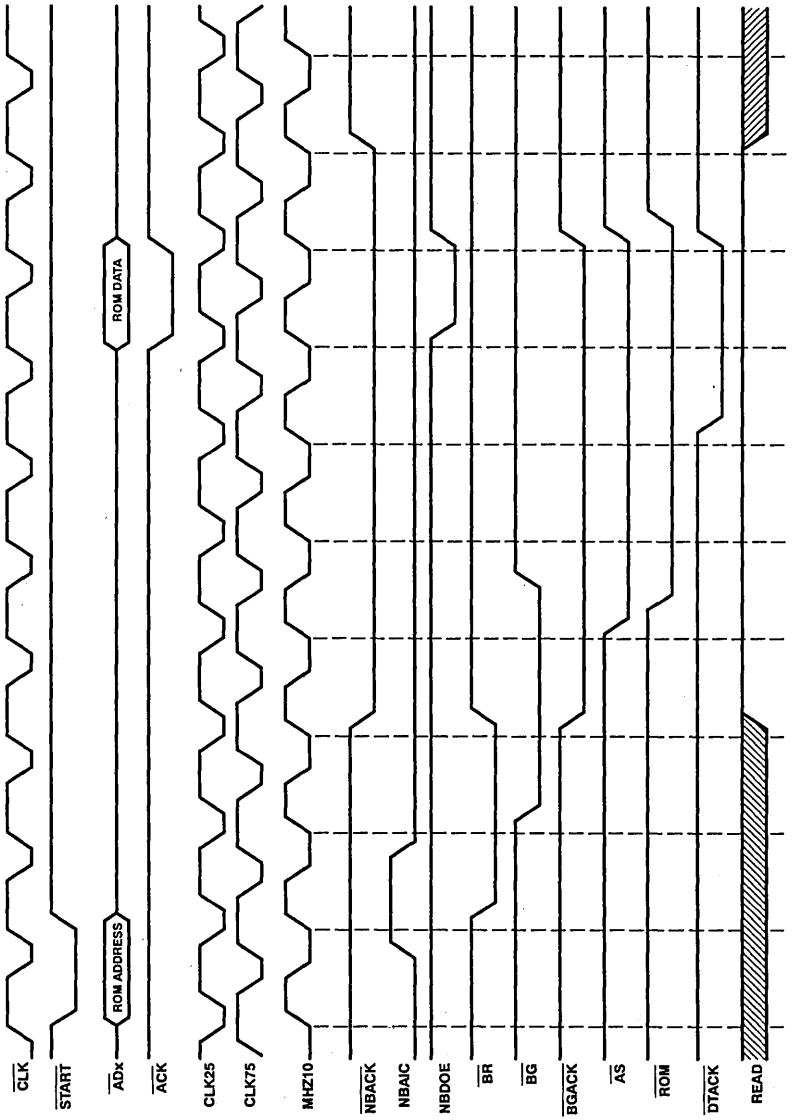


Figure 13. 16-Bit NuBus™ ROM Read Cycle

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APPLICATION INFORMATION

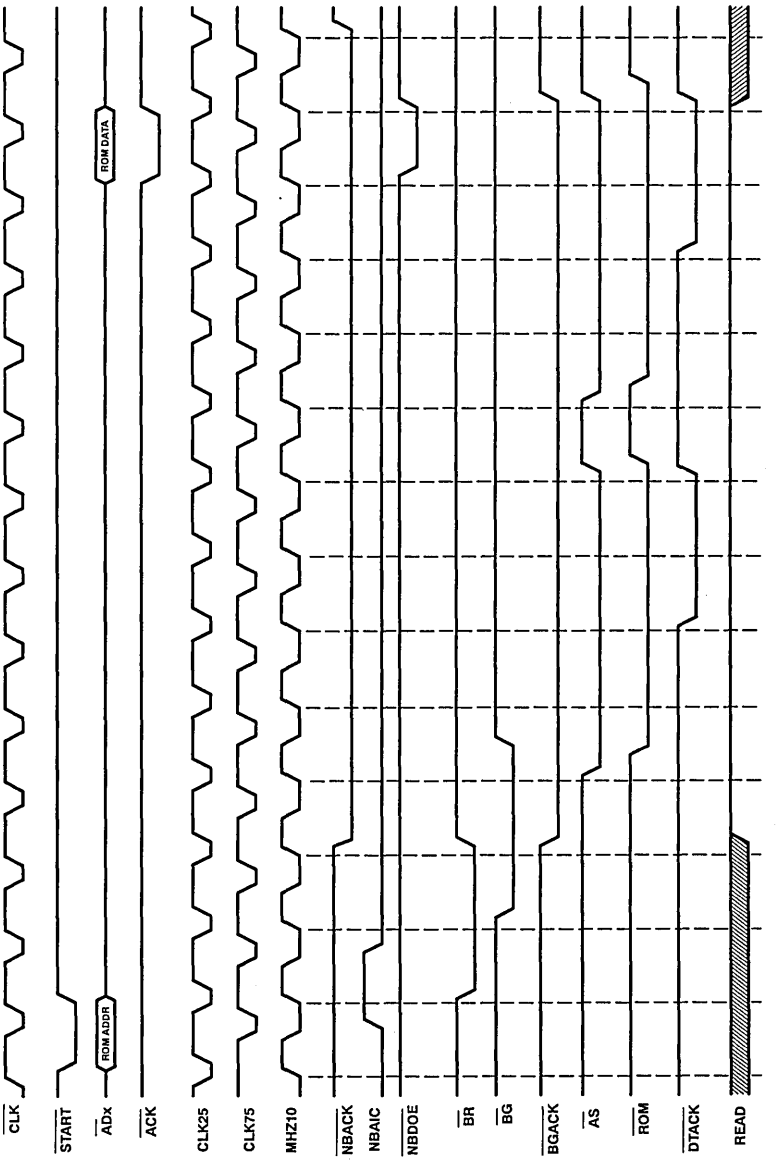


Figure 14. 32-Bit NuBus™ ROM Read Cycle

APPLICATION INFORMATION

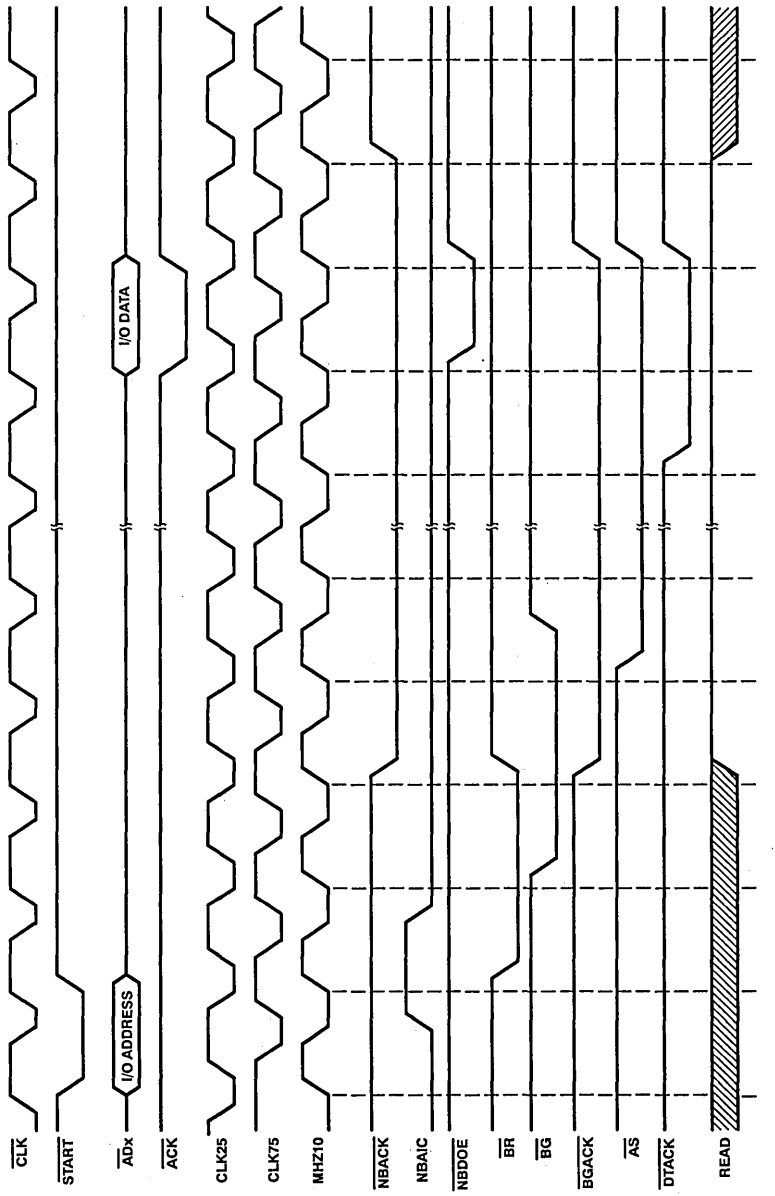


Figure 15. 16-Bit NuBus™ I/O Read Cycle

APPLICATION INFORMATION

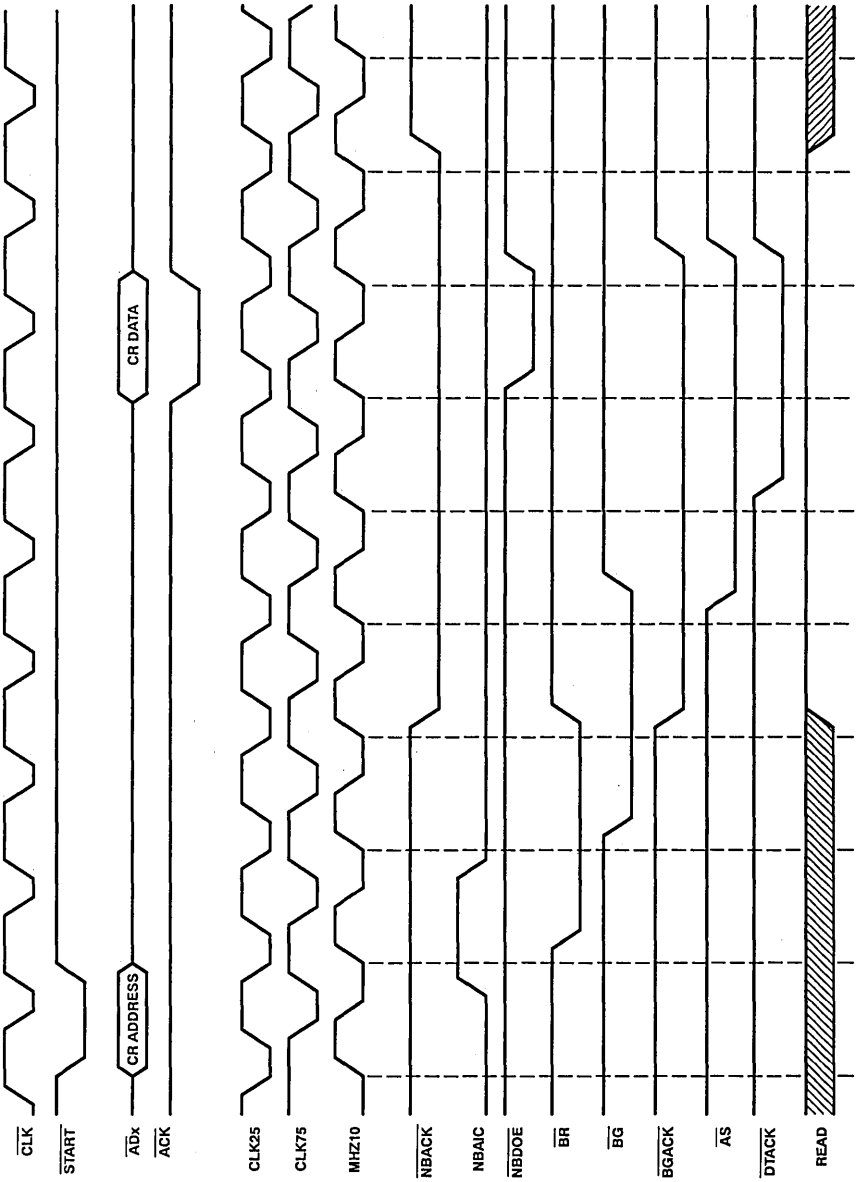


Figure 16. 8-Bit NuBus™ CR Read Cycle

APPLICATION INFORMATION

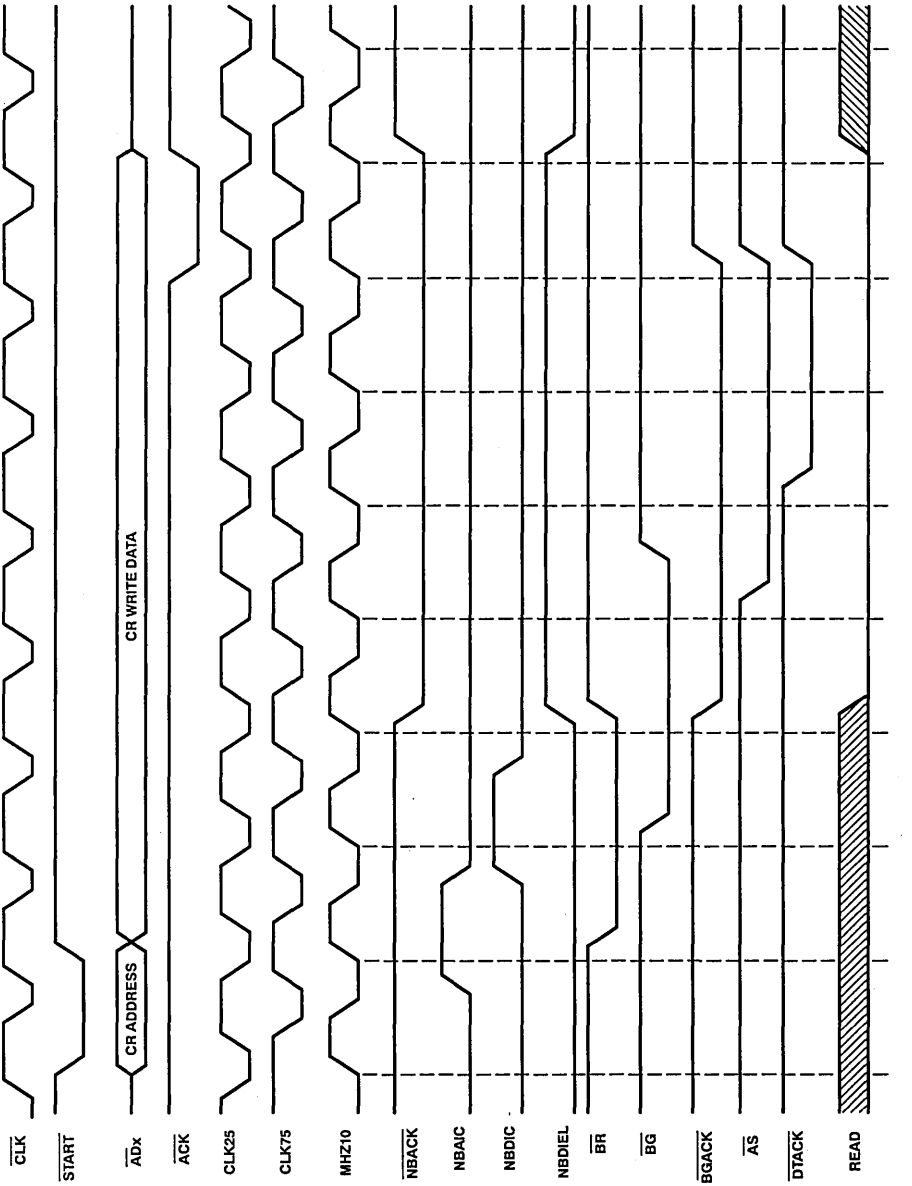


Figure 17. 8-Bit NuBus™ CR Write Cycle

APPLICATION INFORMATION

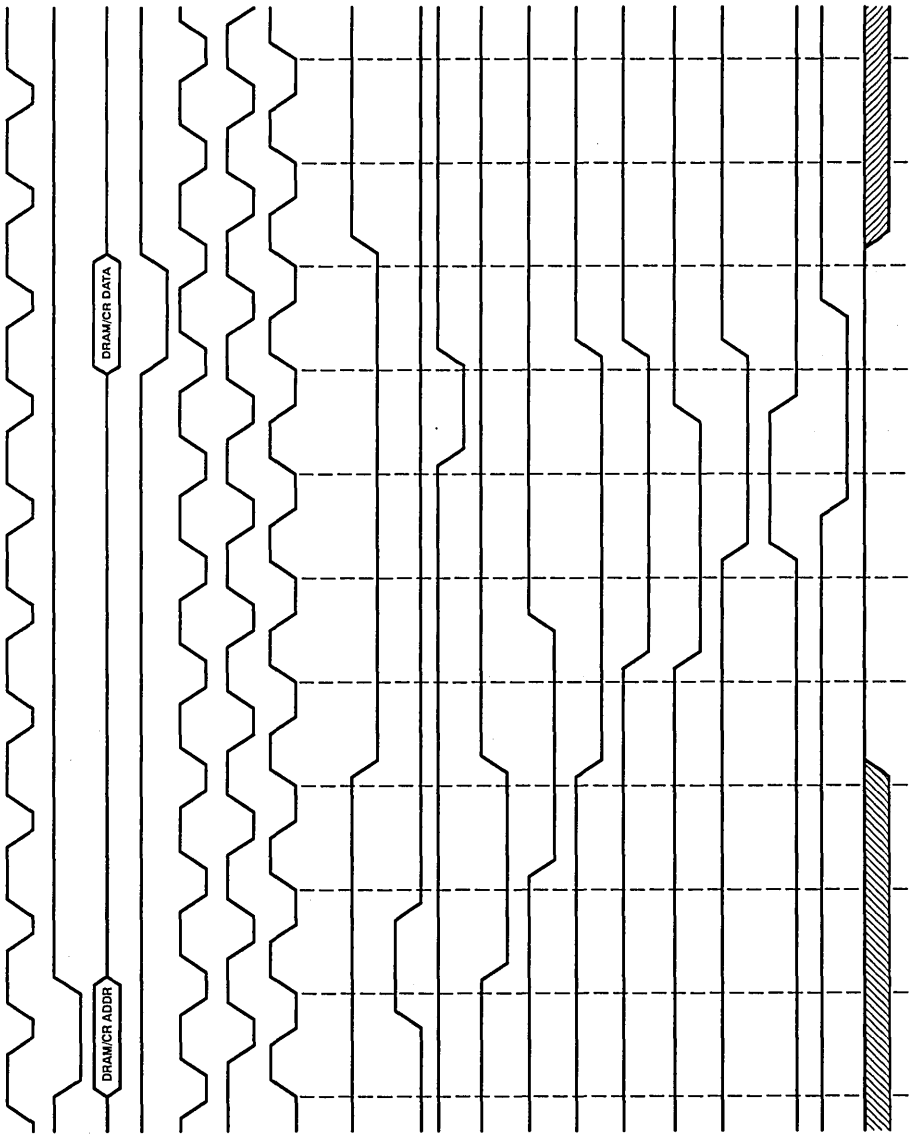


Figure 18. 16-Bit NuBus™ DRAM/CR Read Cycle

APPLICATION INFORMATION

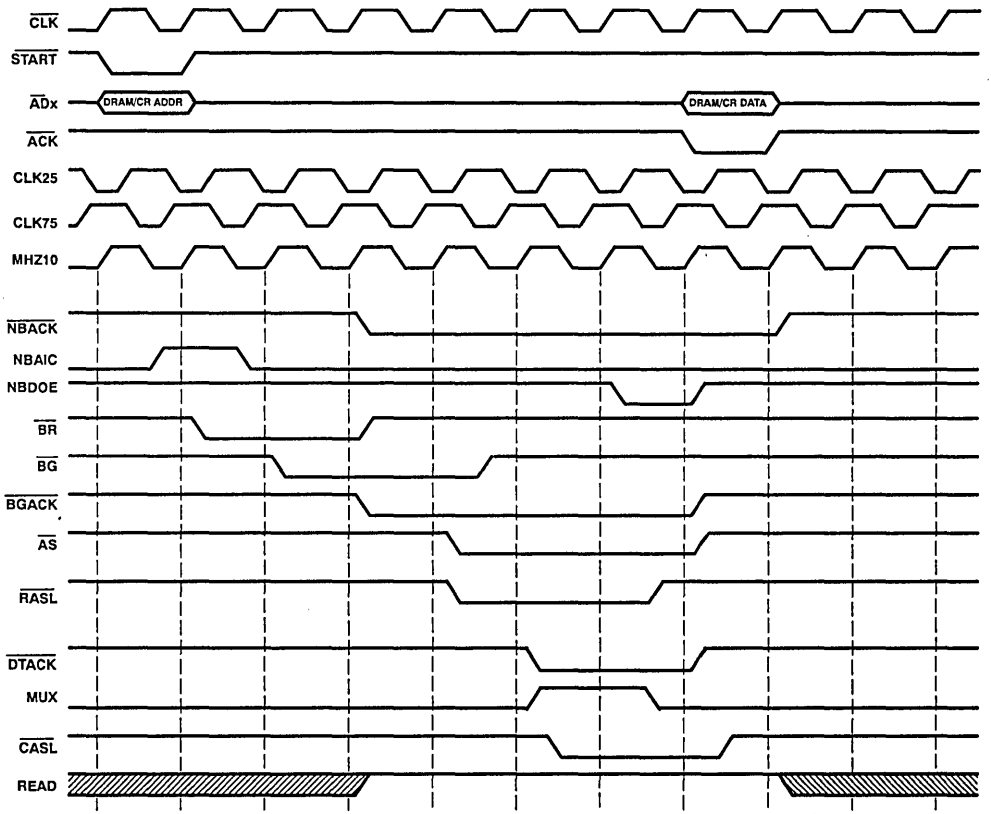


Figure 19. 8-Bit NuBus™ DRAM/CR Read Cycle

APPLICATION INFORMATION

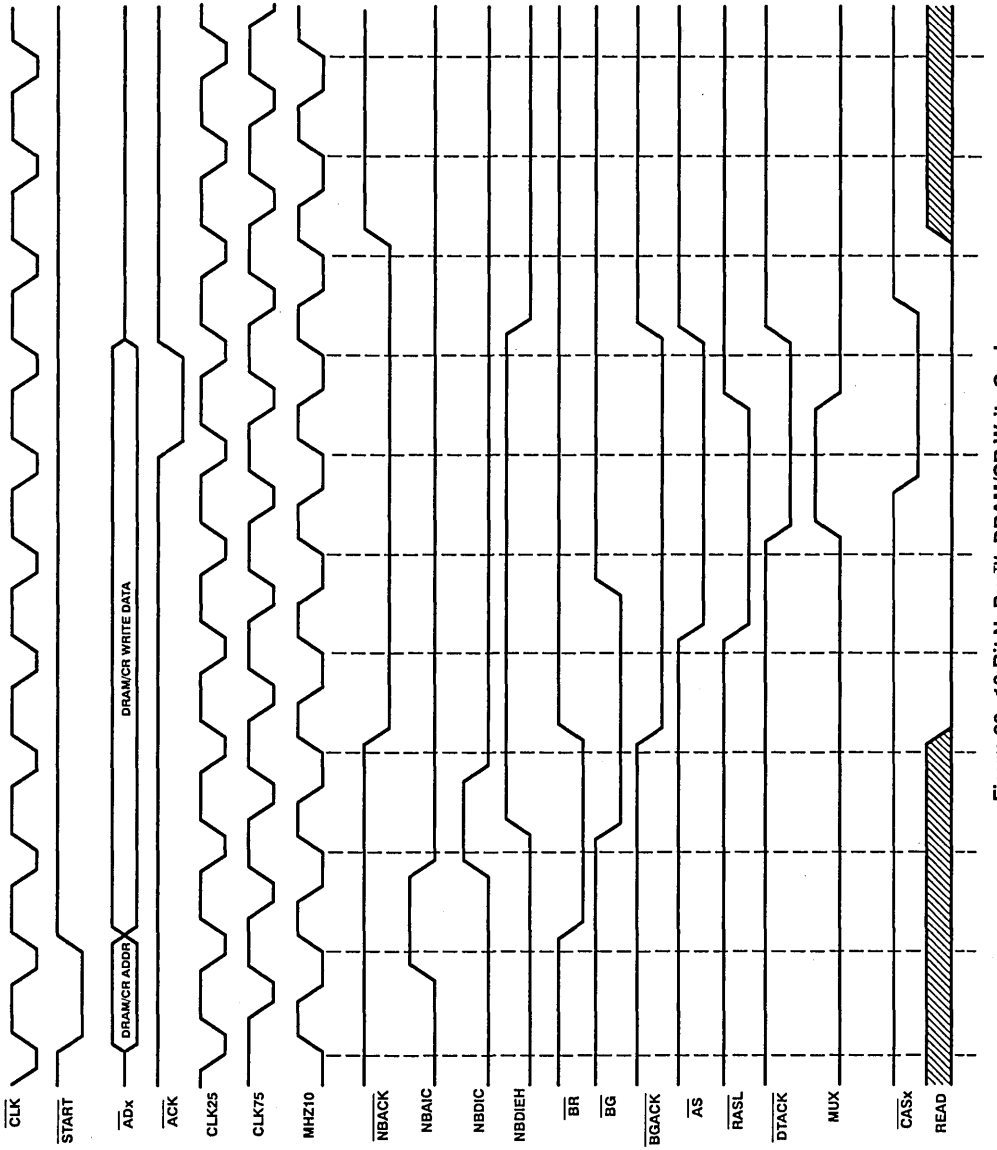


Figure 20. 16-Bit NuBus™ DRAM/CR Write Cycle

APPLICATION INFORMATION

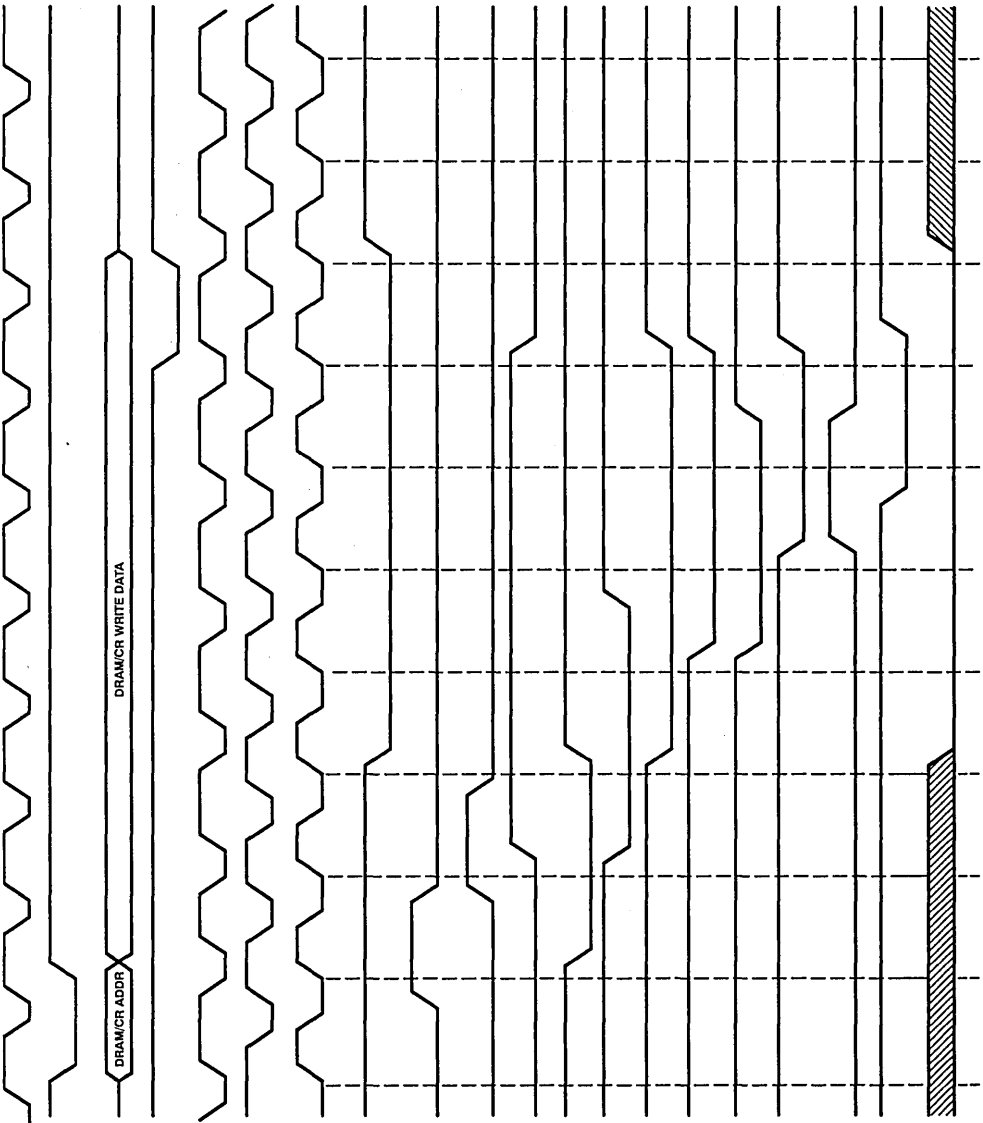


Figure 21. 8-Bit NuBus™ DRAM/CR Write Cycle

APPLICATION INFORMATION

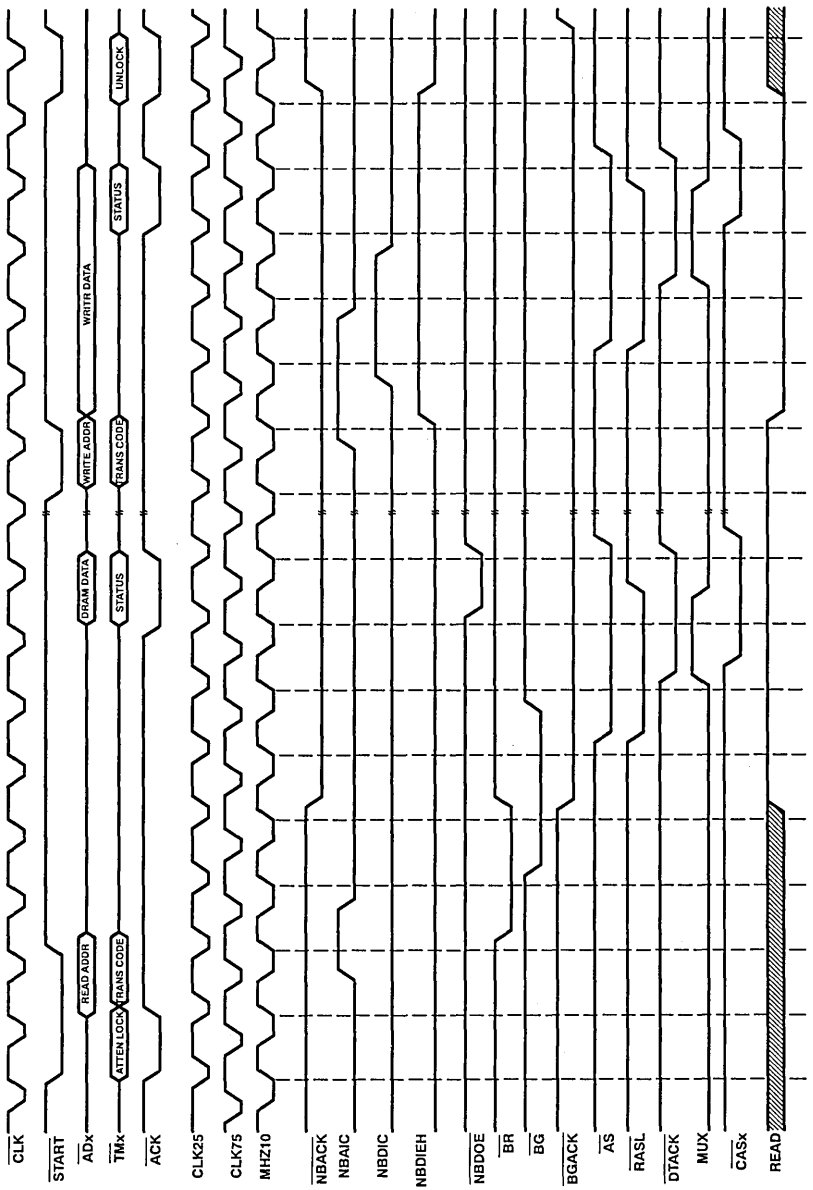
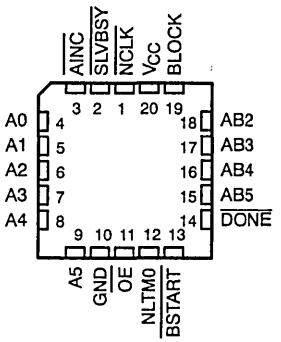


Figure 22. 16-Bit NuBus™ DRAM RMW Cycle

D3355, OCTOBER 1989–REVISED JANUARY 1991

- **Designed to Support NuBus™ Block Slave Address Generation as Defined by ANSI/IEEE Std 1196-1987**
- **Interfaces Directly to Texas Instruments 'ACT2440 (NuBus™ Controller) and 'BCT2420 (NuBus™ Transceivers)**
- **Package Options Include 20-Pin PLCC**

FN PACKAGE
(TOP VIEW)



description

A common method for improving NuBus™ transfer performance is through block transfers. A block transfer is a read or write transaction in which multiple data values are transferred during each NuBus™ ownership sequence. The IEEE specification for NuBus™ allows block transfers in lengths of 2, 4, 8, or 16 words.

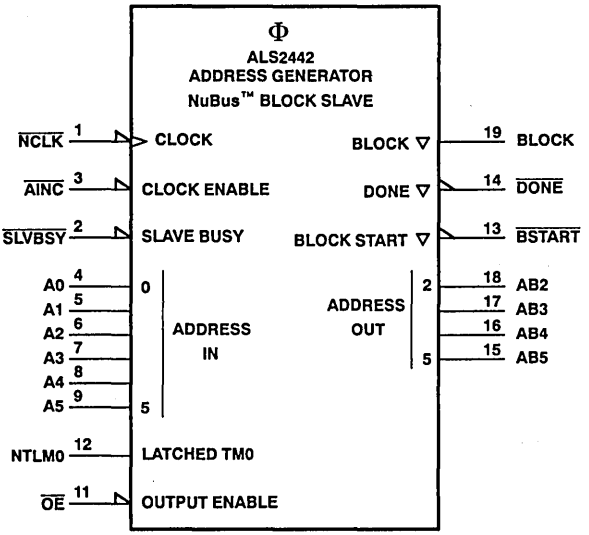
The 'ALS2442 is designed to support NuBus™ block slave transfers as defined by ANSI/IEEE Std 1196-1987. The 'ALS2442 interfaces directly with the 'ACT2440 NuBus™ controller and the 'BCT2420 NuBus™ transceivers. Figure 6 shows a typical NuBus™ interface when using the 'ALS2442 with the 'ACT2440 and 'BCT2420.

When a block read or block write request occurs on the NuBus™, the BLOCK output on the 'ALS2442 is driven high. If the block transfer is directed at the local board, as detected by the Slave External Request ($\overline{\text{SEREQ}}$) output on the 'ACT2440, the 'ALS2442 is then responsible for generating the starting block address and all additional addresses in the transfer sequence. If the transfer request is a normal nonblock cycle, then the 'ACT2442 simply passes the A5 through A2 addresses onto the local address bus.

Table 1 defines the block starting address and the count sequence as generated by the 'ALS2442. Figures 1 and 2 represent a typical timing diagram for a slave block-read and a slave block-write transfer cycle (4 words), respectively. Figures 3 and 4 represent a typical timing diagram for a normal nonblock read and a normal nonblock write transfer cycle, respectively. For additional details on block transfers, consult the Application Report, *Supporting NuBus™ Block Slave Transfers using Texas Instruments SN74ACT2440, SN74BCT2420, and SN74ALS2442*.

NuBus is a trademark of Texas Instruments Incorporated.

logic symbol †



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

TABLE 1. COUNTING SEQUENCE

BLOCK SIZE	INPUT CONDITIONS‡				STARTING ADDRESS				COUNT SEQUENCE‡			
	A5	A4	A3	A2	AB5	AB4	AB3	AB2				
2	X	X	X	L	A5	A4	A3	L	XXXL	XXXH		
4	X	X	L	H	A5	A4	L	L	XXLL	XXLH	XXHL	XXHH
8	X	L	H	H	A5	L	L	L	XLLL	XLLH	XLHL	XLHH
									XHLL	XHLH	XHHL	XHHH
16	L	H	H	H	L	L	L	L	LLLL	LLLH	LLHL	LLHH
									LHLL	LHLH	LHHL	LHHH
									HLLL	HLLH	HLHL	HLHH
									HHLL	HHLH	HHHL	HHHH

‡X denotes the value that was applied to the input terminal; i.e., the value of A5 is seen on AB5, and so on. Count sequence moves from left to right, then top to bottom.

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Terminal Functions

PIN NAME	DESCRIPTION
A5-A0	Buffered NuBus™ Address Inputs. These six address inputs are available from the 'BCT2420s and are used by the 'ALS2442 to decode the existence of and size of a NuBus™ block transfer. If the NuBus™ transfer is a normal read or write, the A5-A2 address inputs are simply passed to the AB5-AB2 outputs.
AB5-AB2	Block Address Outputs. These four address output lines provide the starting and additional block addresses during block transfers.
$\overline{\text{AINC}}$	Address Increment. This active-low input is used by the 'ALS2442 to control the address increment function during block transfers. When low, the block address will increment on each rising edge of $\overline{\text{NCLK}}$, assuming the BLOCK output is also high. During nonblock transfer's, this input has no effect.
BLOCK	Block. This active-high combinataional output is decoded from the A0, A1, and NLTM0 inputs (A0 = L, A1 = H, NLTM0 = L). When a block transfer is detected, this output will be high. When a nonblock transfer is detected, this output will be low.
$\overline{\text{BSTART}}$	Block Start. An active-low output that signals the occurrence of a block transfer sequence. When the $\overline{\text{SLVBSY}}$ input is driven low, this output will be driven low on the next low-to-high clock edge during block transfers . During nonblock transfers, this output will be inactive (high).
$\overline{\text{DONE}}$	Done. An active-low output that signals when the block transfer has reached its next-to-last address. During nonblock transfers (BLOCK = L), this output is active(low). This output is valid only during the transfer sequence and should be sampled only when $\overline{\text{SLVBSY}}$ is low.
$\overline{\text{NCLK}}$	Buffered NuBus™ Clock. This input clock signal is driven by the 'ACT2440 and transitions on the low-to-high clock edge.
NLTM0	NuBus™ Latched Transfer Mode. This input signal is used by the 'ALS2442, along with the A0 and A1 address inputs, to decode block transfers. The NLTM0 input is directly driven from the NLTM0 output on the 'ACT2440.
$\overline{\text{OE}}$	Output Enable. When active (low), AB5-AB2, $\overline{\text{DONE}}$, and $\overline{\text{BSTART}}$ outputs are enabled. When inactive (high), these same outputs will be at high impedance.
$\overline{\text{SLVBSY}}$	Slave Busy. This active-low input is used by the 'ALS2442 to indicate when the local board is ready to respond to the slave transfer request. This input is typically driven low after detecting the slave external request ($\overline{\text{SEREQ}}$) signal from the 'ACT2440 NuBus™ controller. The $\overline{\text{SLVBSY}}$ input should not be taken active (low) until the first rising clock edge after the BLOCK output is valid. This input should be held low until the last transfer has been completed as indicated by a NuBus™ acknowledge.

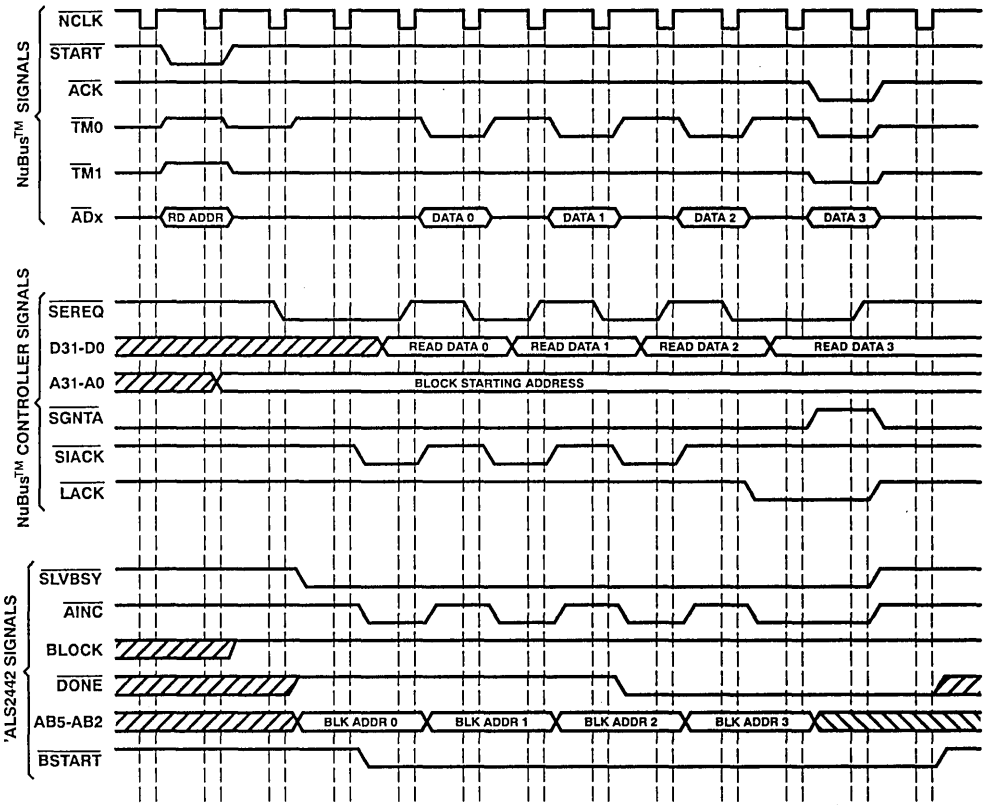

FIGURE 1. TYPICAL BLOCK READ TRANSFER (4 WORDS)

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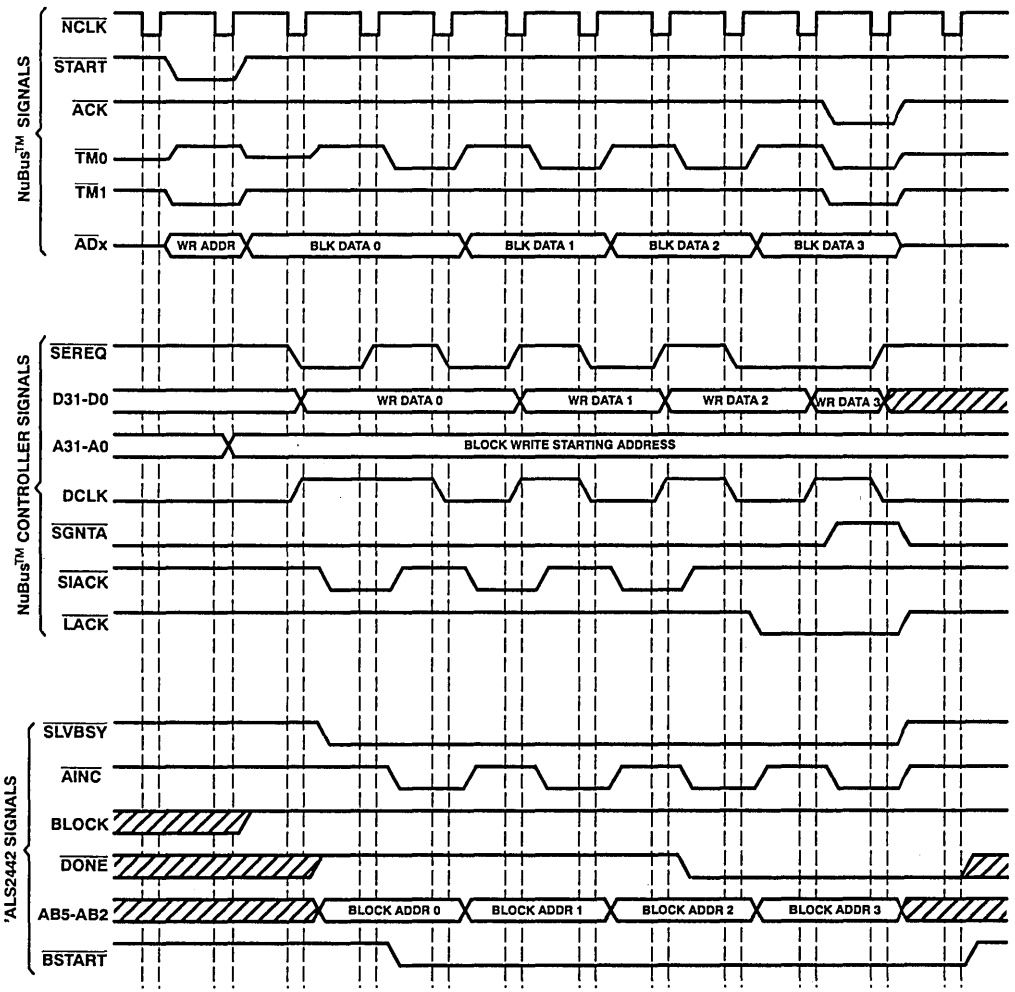

FIGURE 2. TYPICAL BLOCK WRITE TRANSFER (4 WORDS)

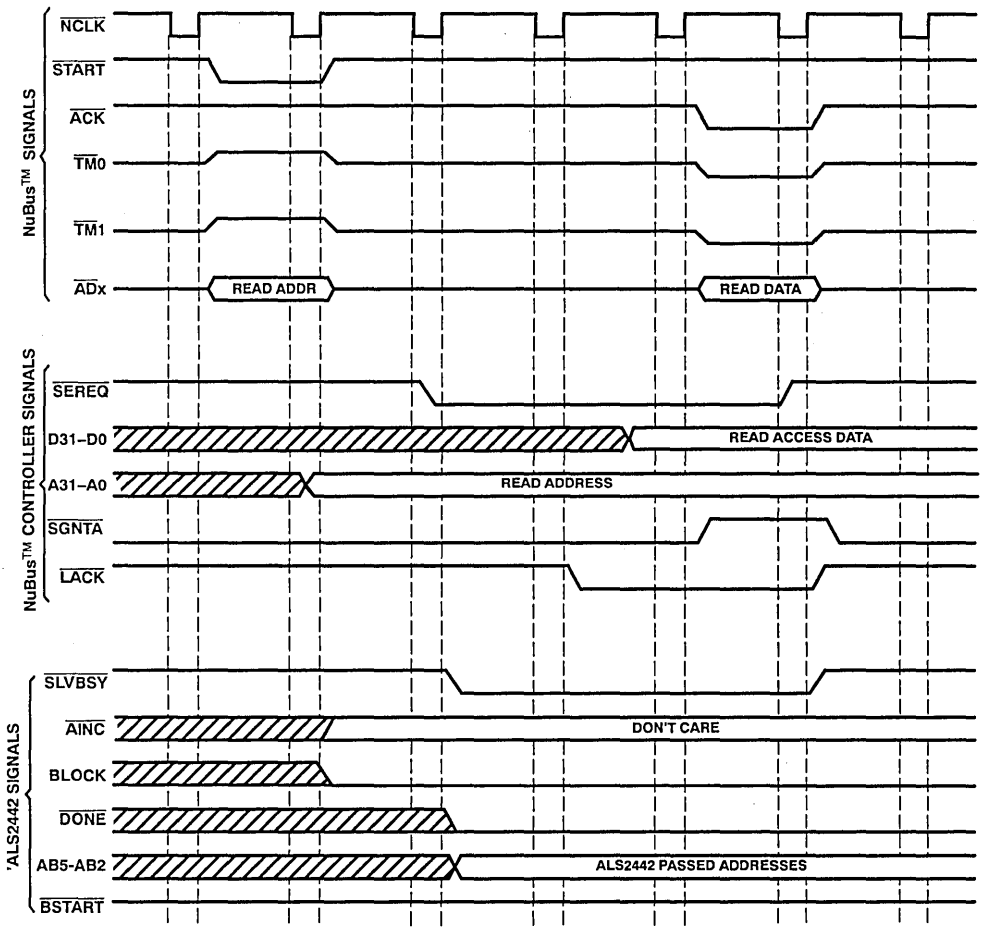

FIGURE 3. TYPICAL NONBLOCK READ TRANSFER CYCLE

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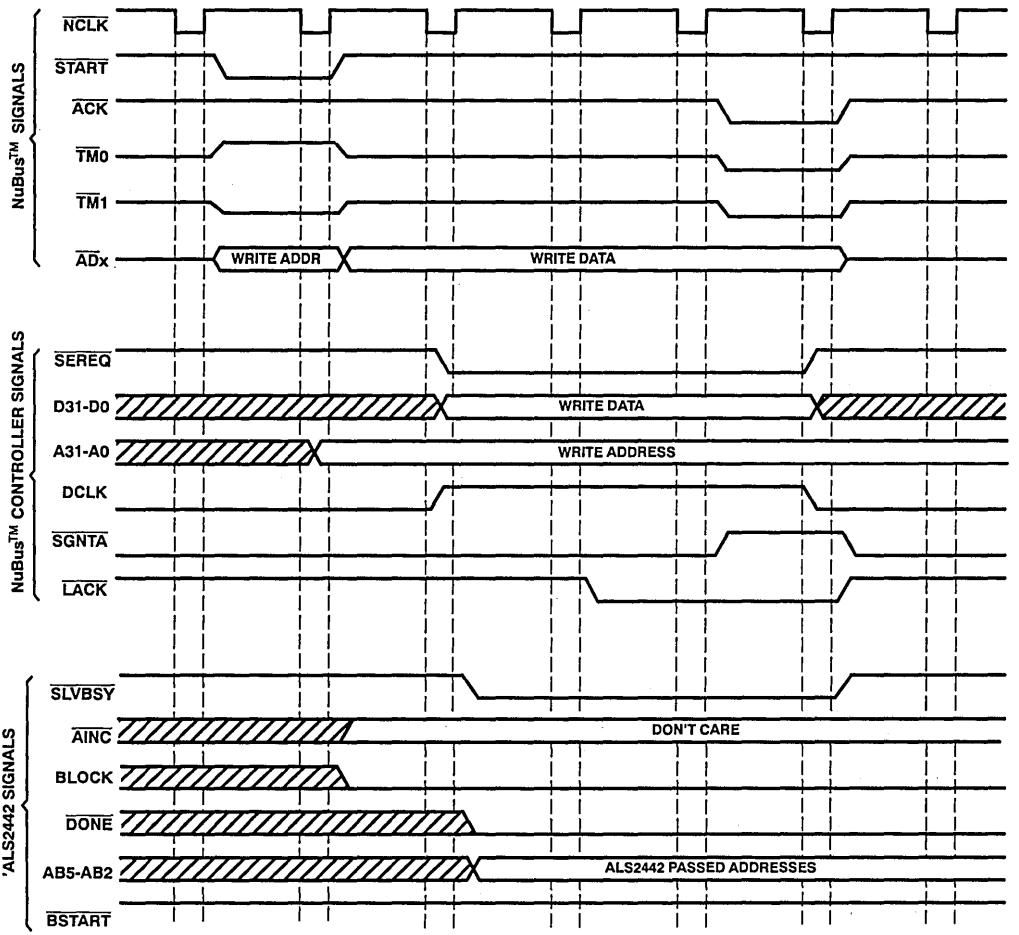


FIGURE 4. TYPICAL NONBLOCK WRITE TRANSFER CYCLE

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage ..... 5.5 V
Voltage applied to a disabled output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}				−3.2	mA
Low-level input current, I_{OL}				24	mA
Pulse duration, t_w	$\overline{NCLK}$ high	8			ns
	$\overline{NCLK}$ low	8			
Setup time, t_{su}	$\overline{SLVBSY}$, $\overline{AINC}$ before $\overline{NCLK}$ ↑	10			ns
	A5-A0, NLMTO before $\overline{NCLK}$ ↑	10			
Hold time, t_h	$\overline{SLVBSY}$, $\overline{AINC}$ after $\overline{NCLK}$ ↑	0			ns
	A5-A0, NLTMO after $\overline{NCLK}$ ↑	0			
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = −18 mA				−1.5	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = −3.2 mA		2.4	3		V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 24 mA			0.3	0.5	V
I_I	V_{CC} = 5.25 V,	V_I = 5.5 V				0.2	mA
I_{OZH}§	V_{CC} = 5.25 V,	V_O = 2.4 V				0.1	mA
I_{OZL}§	V_{CC} = 5.25 V,	V_O = 0.4 V				−0.1	mA
I_{IH}§	V_{CC} = 5.25 V,	V_I = 2.7 V				25	μA
I_{IL}§	V_{CC} = 5.25 V,	V_I = 0.4 V				−0.25	mA
I_O¶	V_{CC} = 5 V,	V_O = 0.5 V		−30		−130	mA
I_{CC}	V_{CC} = 5.25 V,	V_I = 0,	Outputs open		140	180	mA

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH}.

¶ This parameter approximates I_{OS}. The condition V_O = 0.5 V takes tester noise into account. Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

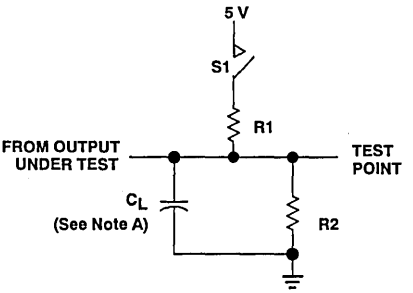
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
t_{pd}	A0, A1, NLTMO	BLOCK	R1 = 200 Ω, R2 = 390 Ω			10	ns
t_{pd}	$\overline{NCLK}$ ↑	ABx				8	ns
t_{pd}	$\overline{NCLK}$ ↑	$\overline{DONE}$				8	ns
t_{pd}	$\overline{NCLK}$ ↑	$\overline{BSTART}$				8	ns
t_{en}	$\overline{OE}$	ABx, $\overline{DONE}$, $\overline{BSTART}$				10	ns
t_{dis}	$\overline{OE}$	ABx, $\overline{DONE}$, $\overline{BSTART}$				10	ns

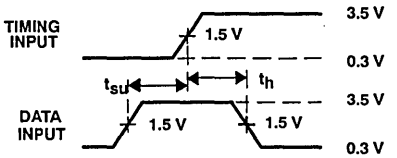
† See Parameter Measurement Information for load circuit and voltage waveforms.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

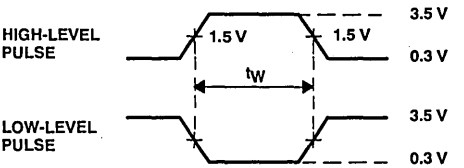
PARAMETER MEASUREMENT INFORMATION



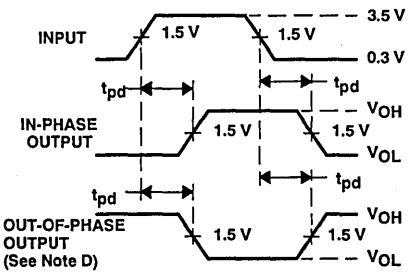
LOAD CIRCUIT FOR 3-STATE OUTPUTS



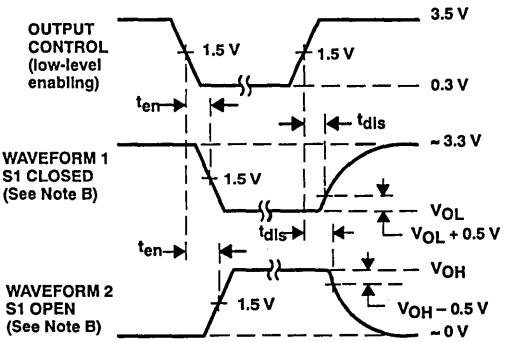
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLED TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

FIGURE 5

APPLICATION INFORMATION

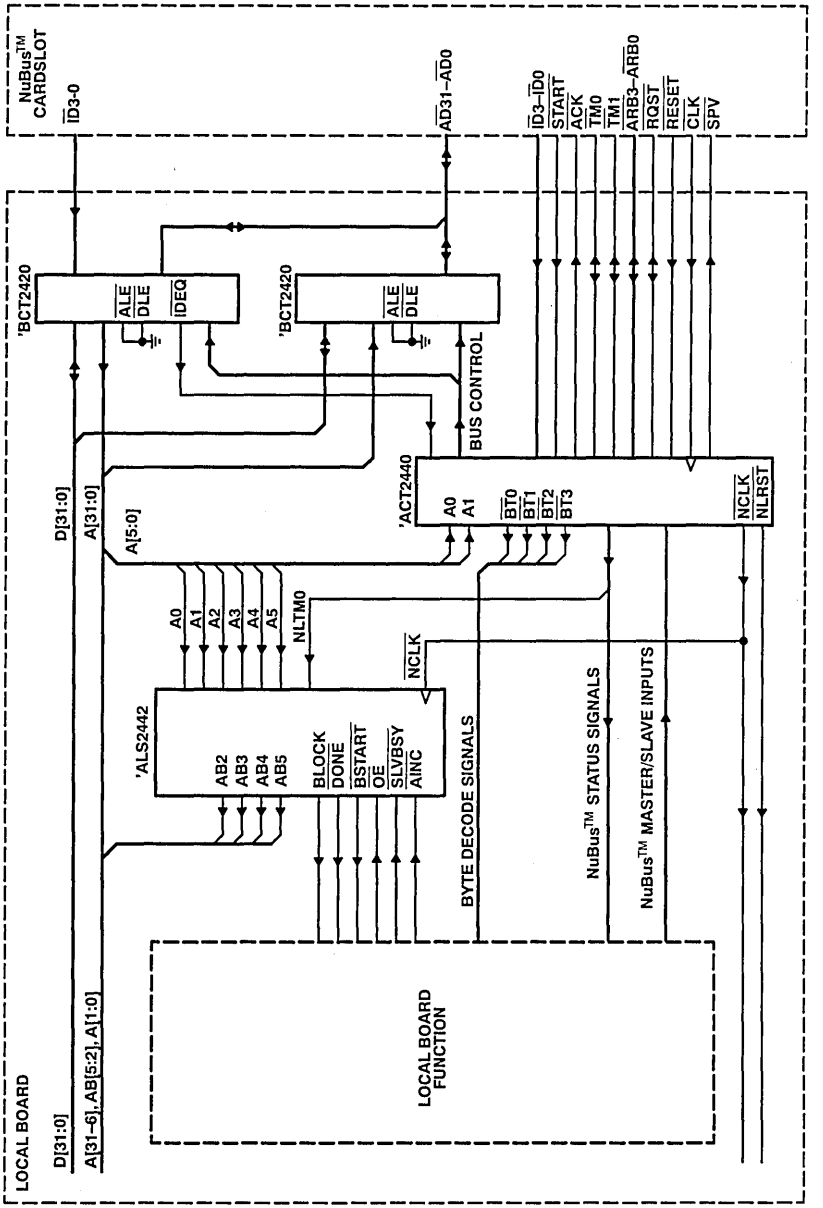


FIGURE 6. TYPICAL 'ALS2442 INTERFACE

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NuBus™ Device Data Sheets 2

Application Reports 3

Explanation of Logic Symbols 4

Mechanical Data 5

ESD Guidelines 6

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Supporting NuBus™ Block Slave Transfers

SN74ACT2440, SN74BCT2420, and SN74ALS2442

TEXAS
INSTRUMENTS

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Appendix

NuBus™ Block Transfer Slave PAL® **3-21**

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Introduction

A common method for improving NuBus™ transfer performance is via block transfers. A block transfer is a read or write transaction in which multiple data values are transferred during each NuBus™ ownership sequence. The IEEE specification for NuBus™ 1987 allows block transfers in lengths of 2, 4, 8, or 16 words.

The purpose of this application report is to demonstrate how block slave transfers can be supported using Texas Instruments 'ACT2440, 'BCT2420, and 'ALS2442 NuBus™ chipset.

In order for a NuBus™ slave to support block transfers, it must first be capable of detecting the type (read or write) and size of a block transfer as communicated by the NuBus™ master. The number of data words transferred is controlled by the master and is communicated during the start cycle via $\overline{AD5}$ – $\overline{AD2}$. The type of NuBus™ transfer is communicated via $\overline{TM1}$, $\overline{TM0}$, $\overline{AD1}$, and $\overline{AD0}$. Table 1 shows the block starting address and the required slave decoding as presented by the 'ACT2440 and 'BCT2420.

Block Slave Support

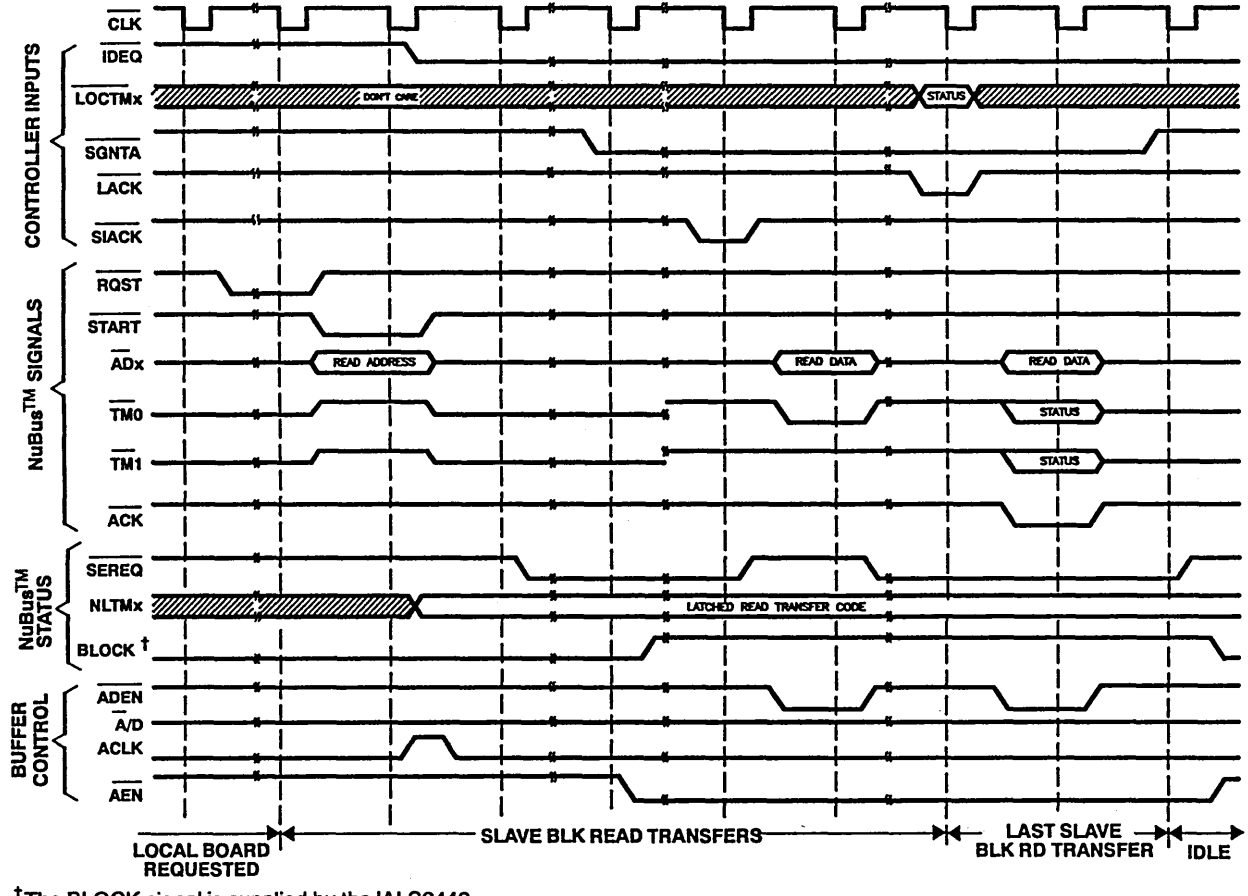
Table 1. Block Starting Address and Required Slave Decoding

A5	A4	A3	A2	A1	A0	NTM1	NTM0	BLOCK SIZE	CYCLE TYPE	STARTING ADDRESS		
X	X	X	L	H	L	H	L	2	WRITE	(A31-A3) 0	A1	A0
X	X	L	H	H	L	H	L	4	WRITE	(A31-A4) 00	A1	A0
X	L	H	H	H	L	H	L	8	WRITE	(A31-A5) 000	A1	A0
L	H	H	H	H	L	H	L	16	WRITE	(A31-A6) 0000	A1	A0
X	X	X	L	H	L	L	L	2	READ	(A31-A3) 0	A1	A0
X	X	L	H	H	L	L	L	4	READ	(A31-A4) 00	A1	A0
X	L	H	H	H	L	L	L	8	READ	(A31-A5) 000	A1	A0
L	H	H	H	H	L	L	L	16	READ	(A31-A6) 0000	A1	A0

During block transfers, intermediate data cycles (all except the last transfer) are acknowledged via $\overline{TM0}$. The 'ACT2440 NuBus™ controller has a special input called Slave Interim Acknowledge that is used for generating the interim acknowledge signal. Figures 1 and 2 show a typical timing diagram for a slave block read and a slave block write when using the 'ACT2440/'BCT2420 NuBus™ chipset.

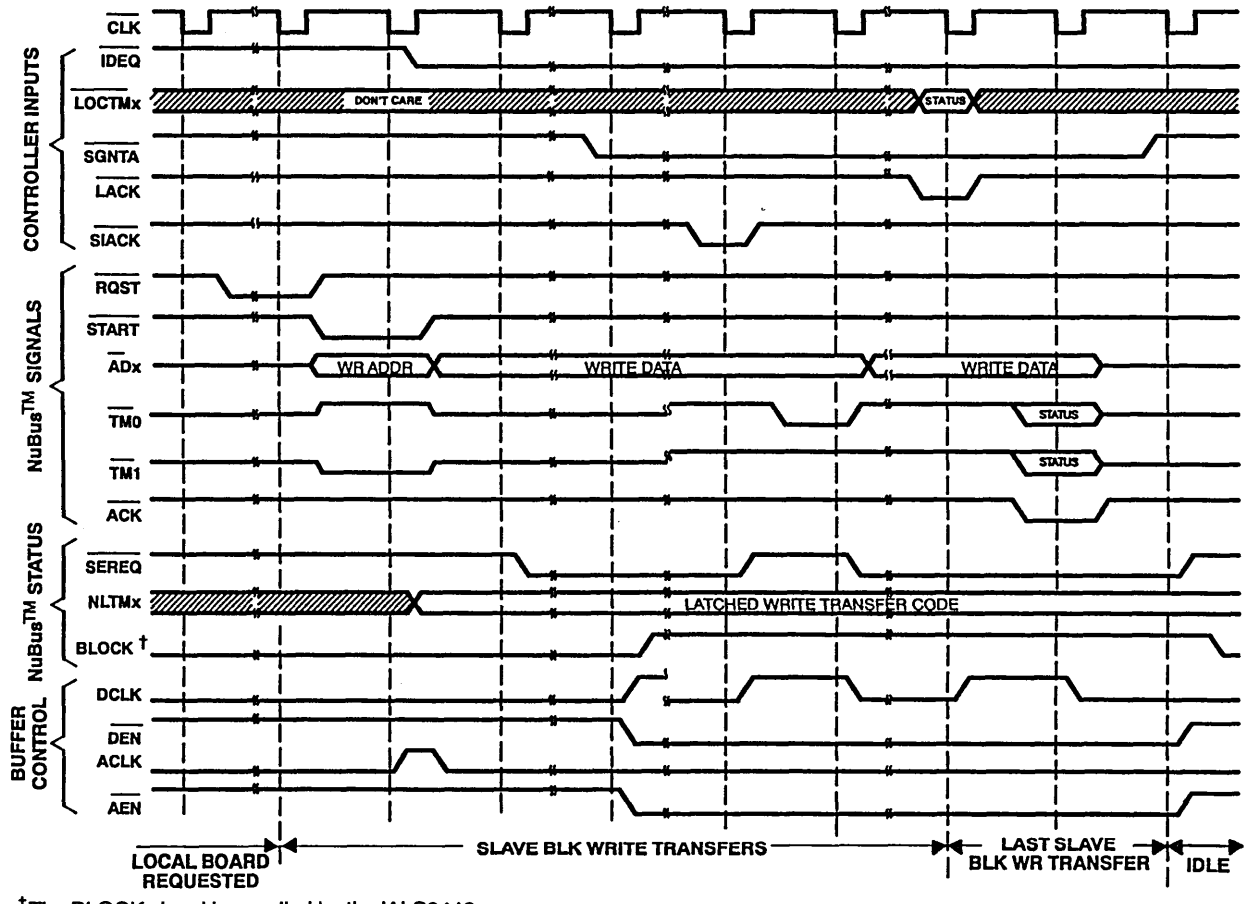
Notice from these timing diagrams that the Slave External Request output ($\overline{SEREQ}$) on the 'ACT2440 provides a handshake between the NuBus™ controller and the local board during interim acknowledge cycles. Also notice that the final data transfer ends with a normal acknowledge via the Local Acknowledge input ($\overline{LACK}$).

Figure 3 represents a typical NuBus™ block slave application. In this example, dynamic memory is addressable from a NuBus™ cardslot using either block or normal accesses. In addition to dynamic memory, 256 bytes of read-only-memory (ROM) is available for system configuration.



†The BLOCK signal is supplied by the 'ALS2442.

Figure 1. Typical NuBus™ Slave Block-Read Transfer Cycles Using 'ACT2420



†The BLOCK signal is supplied by the 'ALS2442.

Figure 2. Typical NuBus™ Slave Block-Write Transfer Cycles Using 'ACT2440

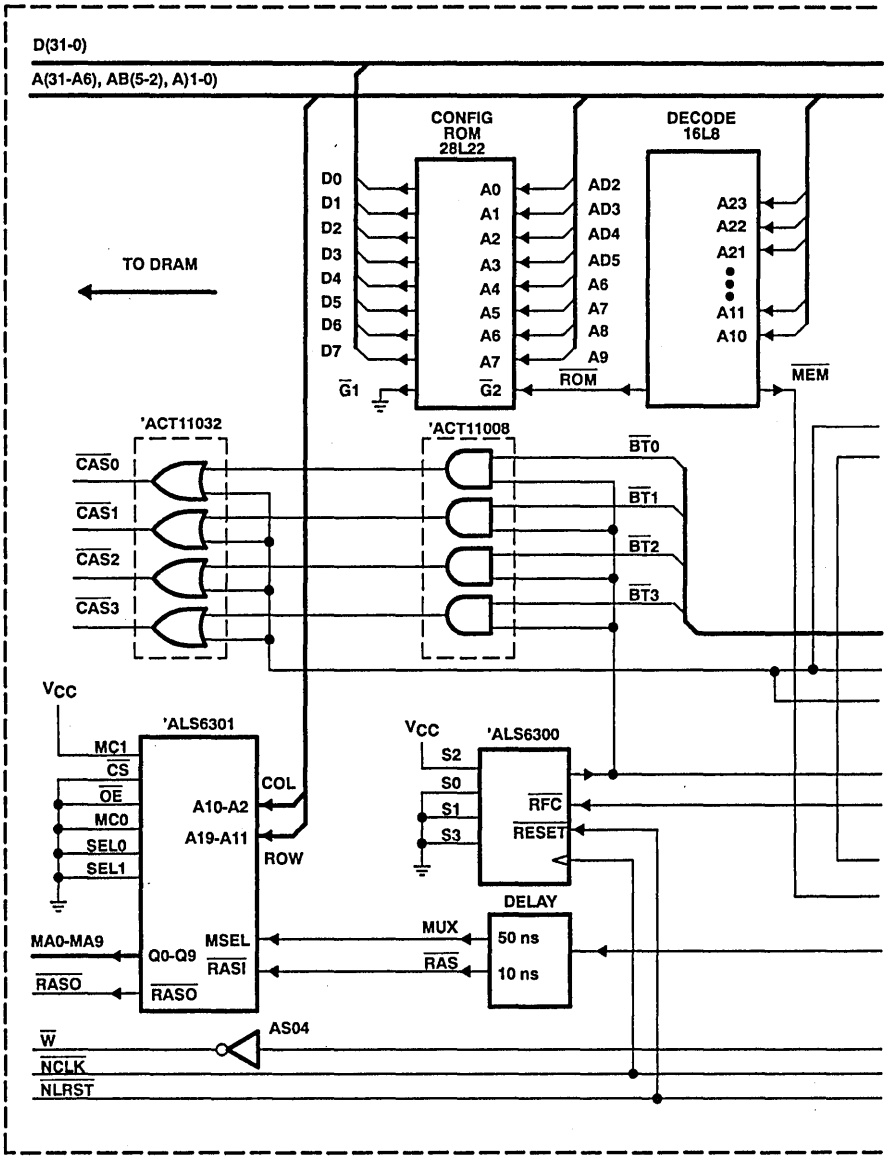


Figure 3. Typical NuBus™ Block Slave Application

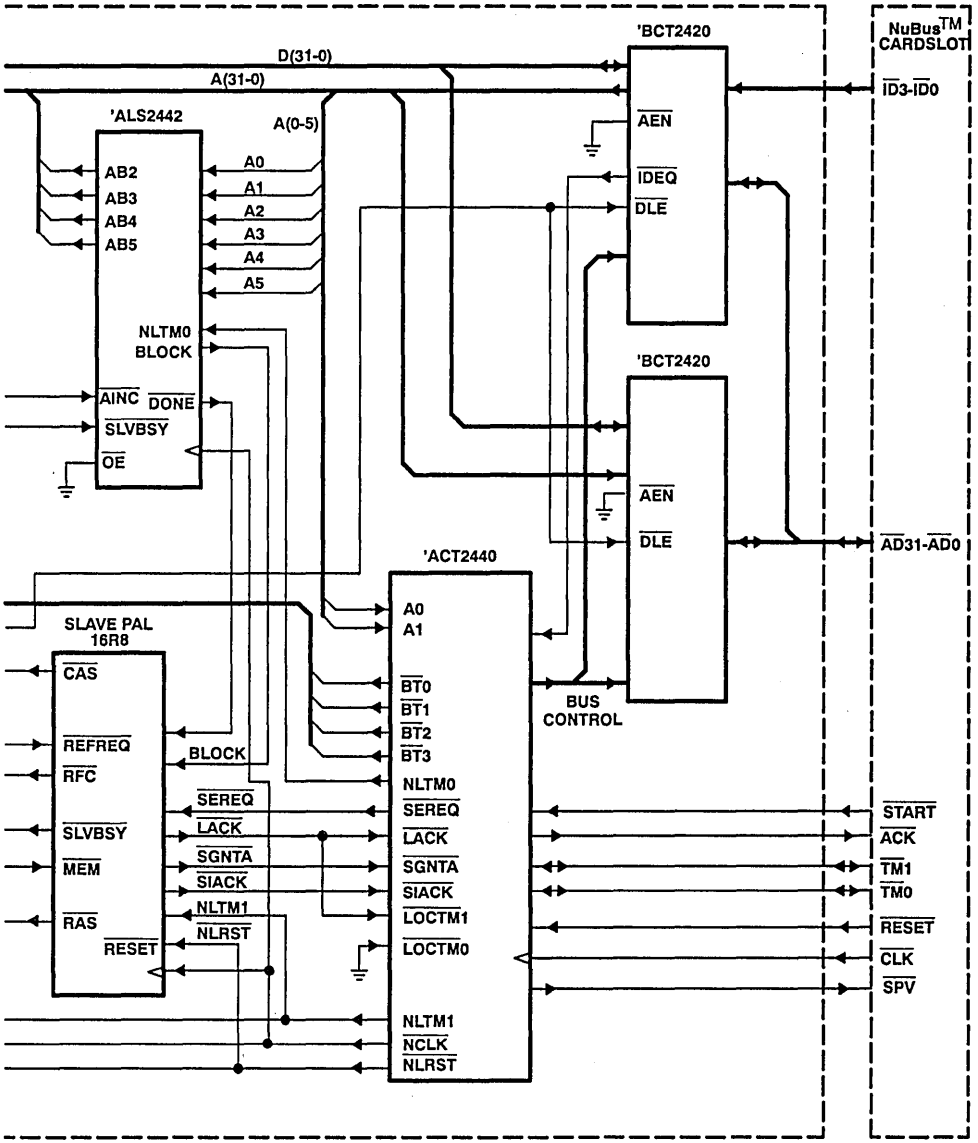


Figure 3. Typical NuBus™ Block Slave Application (continued)

Overview of Operation

The 'ALS2442 shown in Figure 3 is responsible for generating the starting block address and all additional addresses according to the block size communicated by the NuBus™ master. During normal read or write cycles (where only one word is transferred), the 'ALS2442 simply outputs the same address applied to the A5-A2 inputs. An output from the 'ALS2442 ($\overline{\text{DONE}}$) signals the Slave PAL® when a block transfer is complete.

The Slave PAL® shown in Figure 3 is responsible for detecting when a local NuBus™ request has occurred. Upon detecting a local NuBus™ request, the Slave PAL® proceeds to generate the appropriate sequence to carry out the transfer. The NuBus™ request may be a block read, block write, normal read, normal write, or simple ROM read. The Slave PAL® is also responsible for handling DRAM refresh cycles.

Table 2 will further explain the function of each control pin on the Slave PAL®.

Slave PAL® Details

Figures 4 through 9 represent timing diagrams for the six cycles supported by the Slave PAL®. Figure 10 shows a state diagram for the Slave PAL®. A listing of the ABEL file developed for the Slave PAL® is attached at the end of this application note. The ABEL file can be used to generate the JEDEC file required for programming the Slave PAL®.

Notice in Figure 3 that the $\overline{\text{RAS}}$ signal from the Slave PAL® is taken through a delay line before feeding into the 'ALS6301 Memory Controller. This helps ensure the row address setup time is met for the dynamic memory. A delay line is also used to generate the MUX control signal that is used for selecting between row and column addresses. These two delay times can be adjusted to match the particular DRAM specifications in use.

Notice from the timing diagram shown in Figure 9 that a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh sequence is being used. The type of DRAM selected must be capable of supporting this type of refresh cycle. Also notice that static column mode of operation is being used to improve transfer performance. The timing sequences developed for the Slave PAL® assume the DRAMs can support this type of timing, such as the Texas Instruments TMS44C256.

Table 2. Slave PAL® Pin Description

PIN NAME	DESCRIPTION
BLOCK	An active high input used by the Slave Pal® to signal the occurrence of a block transfer.
$\overline{CAS}$	Column Address Strobe. An active low output used to drive the DRAM $\overline{CAS}$ signal via the byte control circuitry and to enable the address increment function ($\overline{AINC}$) on the 'ALS2442. This $\overline{CAS}$ signal is also used by the 'BCT2420 to control the data latch enable function.
$\overline{DONE}$	An active low input generated by the 'ALS2442 that signals when the block transfer is one address from completion. During nonblock transfers, the 'ALS2442 drives this input low as long as a nonblock condition exists.
$\overline{LACK}$	Local Acknowledge. An active low output used to drive the local acknowledge input on the 'ACT2440. When low, the NuBus™ Controller ('ACT2440) issues an acknowledge on the NuBus™.
$\overline{MEM}$	Memory Decode. An active low input that identifies a DRAM access from a ROM access. When low, a DRAM access is indicated.
$\overline{NLTM1}$	NuBus™ Latched Transfer Mode 1. An input signal provided by the 'ACT2440 NuBus™ controller that is used by the Slave Pal® tto decode read or write cycles.
$\overline{RAS}$	Row Address Strobe. An active low output signal used to drive the DRAM $\overline{RAS}$ input signals.
$\overline{REFREQ}$	Refresh Request. An active low input generated by the 'ALS6300 refresh timer and used by the Slave Pal® tto signal when a refresh cycle is required.
$\overline{RESET}$	An active low input used to reset the Slave Pal® tstate machine during NuBus™ reset cycles.
$\overline{RFC}$	Refresh Complete. An active low output generated by the Slave Pal® to signal when it has completed a refresh cycle. The 'ALS6300 will respond to this signal by negating the refresh request signal ($\overline{REFREQ}$).
$\overline{SEREQ}$	Slave External Request. An active low input generated by the NuBus™ controller ('ACT2440) to signal the occurrence of a slave request to the local board from the NuBus™.
$\overline{SGNTA}$	Slave Grant Access. An active low output used to drive the slave grant access input ($\overline{SGNTA}$) on the 'ACT2440. When low, it informs the NuBus™ controller that slave resources are ready to respond to a transfer request. The input is typically held low on slave-only boards to maximize transfer performance; however, it must be cycled high each transfer sequence in order to negate the slave external request signal ($\overline{SEREQ}$) on the NuBus™ controller ('ACT2440).
$\overline{SIACK}$	Slave Interim Acknowledge. An active low output that drives the $\overline{SIACK}$ input on the 'ACT2440, which causes an interim acknowledge signal on the NuBus™.
$\overline{SLVBSY}$	Slave Busy. An active low output generated by the Slave Pal® tto signal the occurrence of a transfer request to the local board. The output will remain low until the transfer sequence is complete.

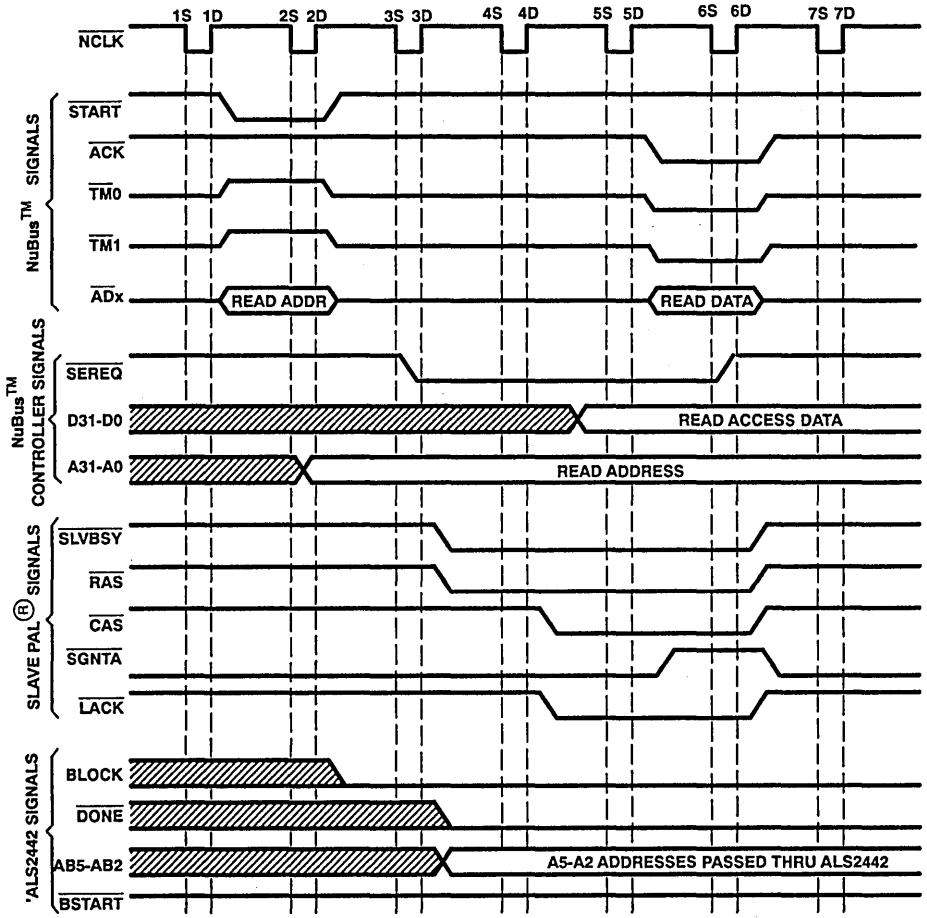


Figure 4. Normal (Nonblock) Read Cycle

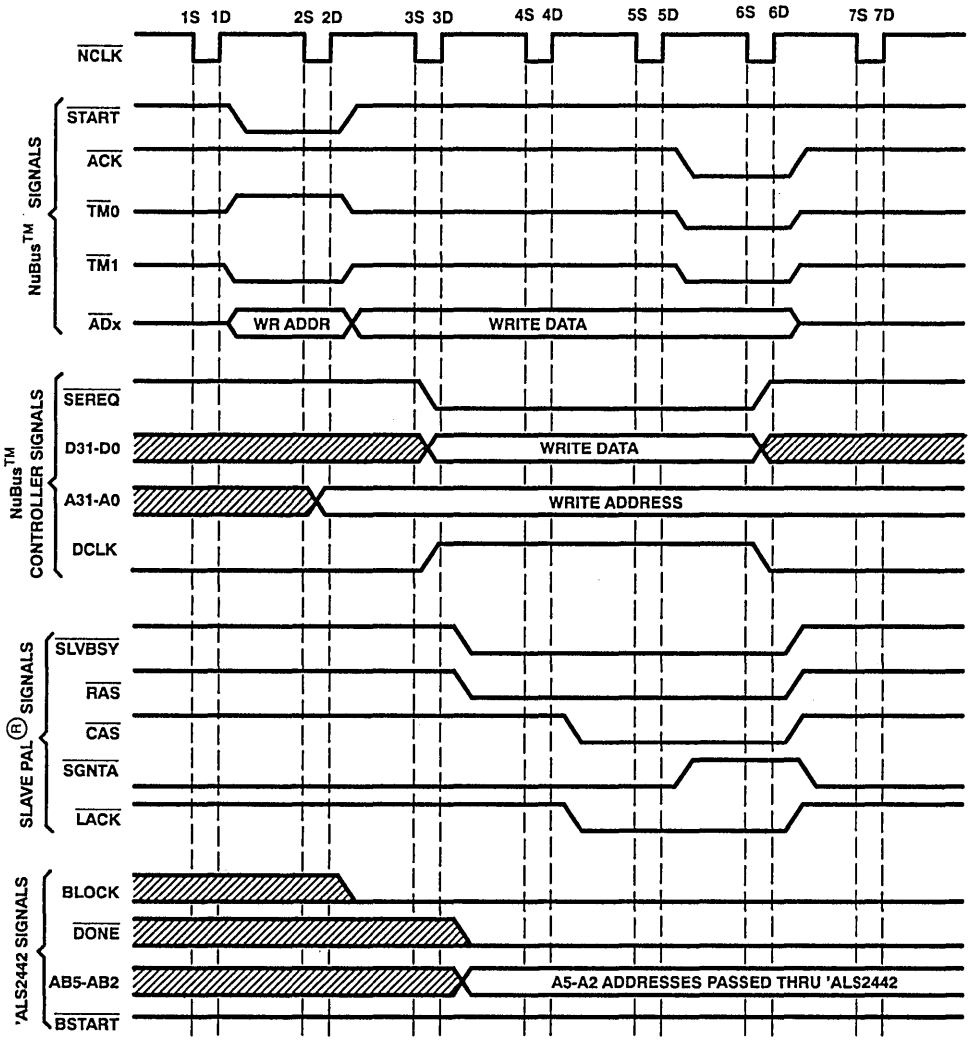


Figure 5. Normal (Nonblock) Write Cycle

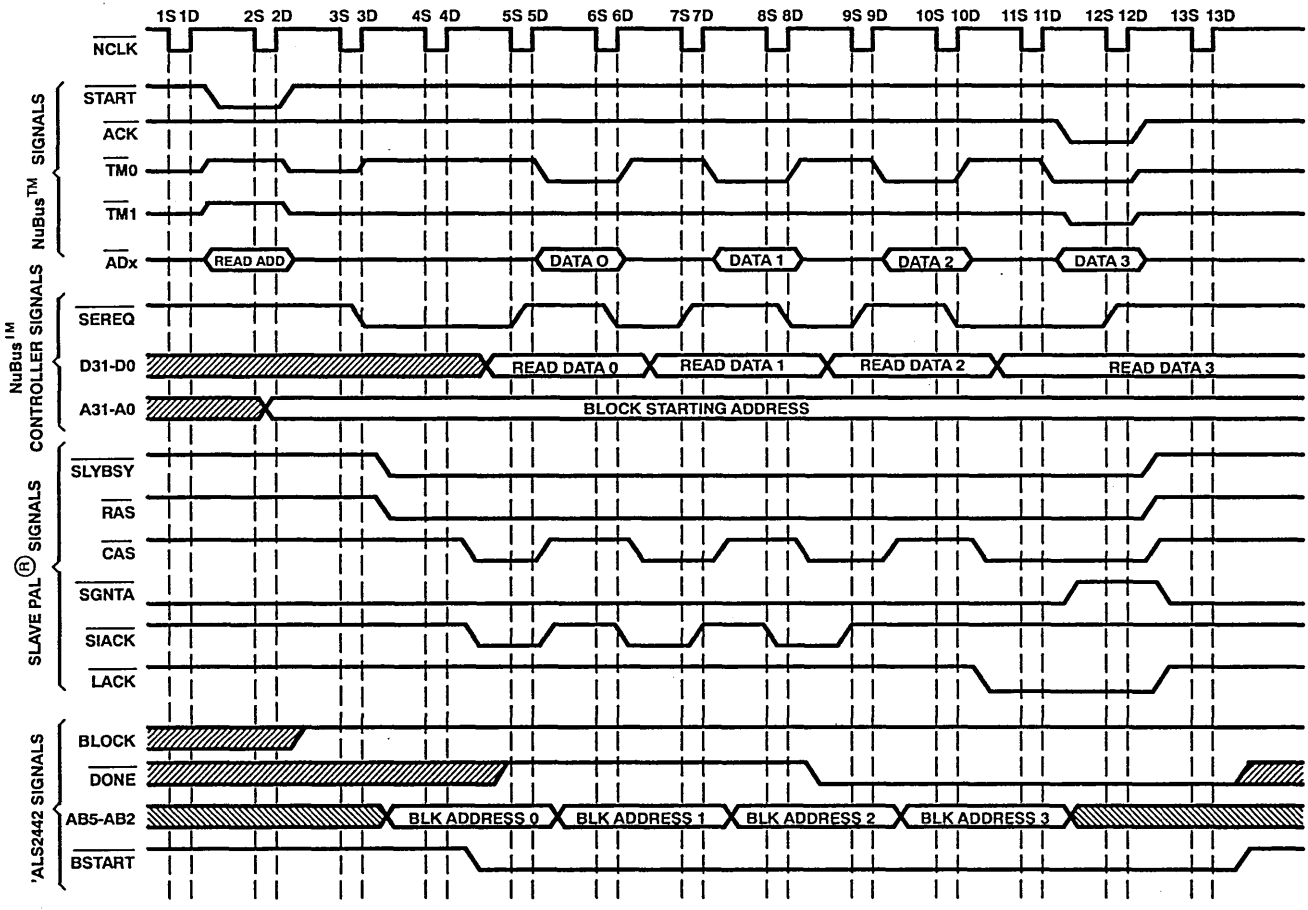


Figure 6. Block Read Transfer (4 Words)

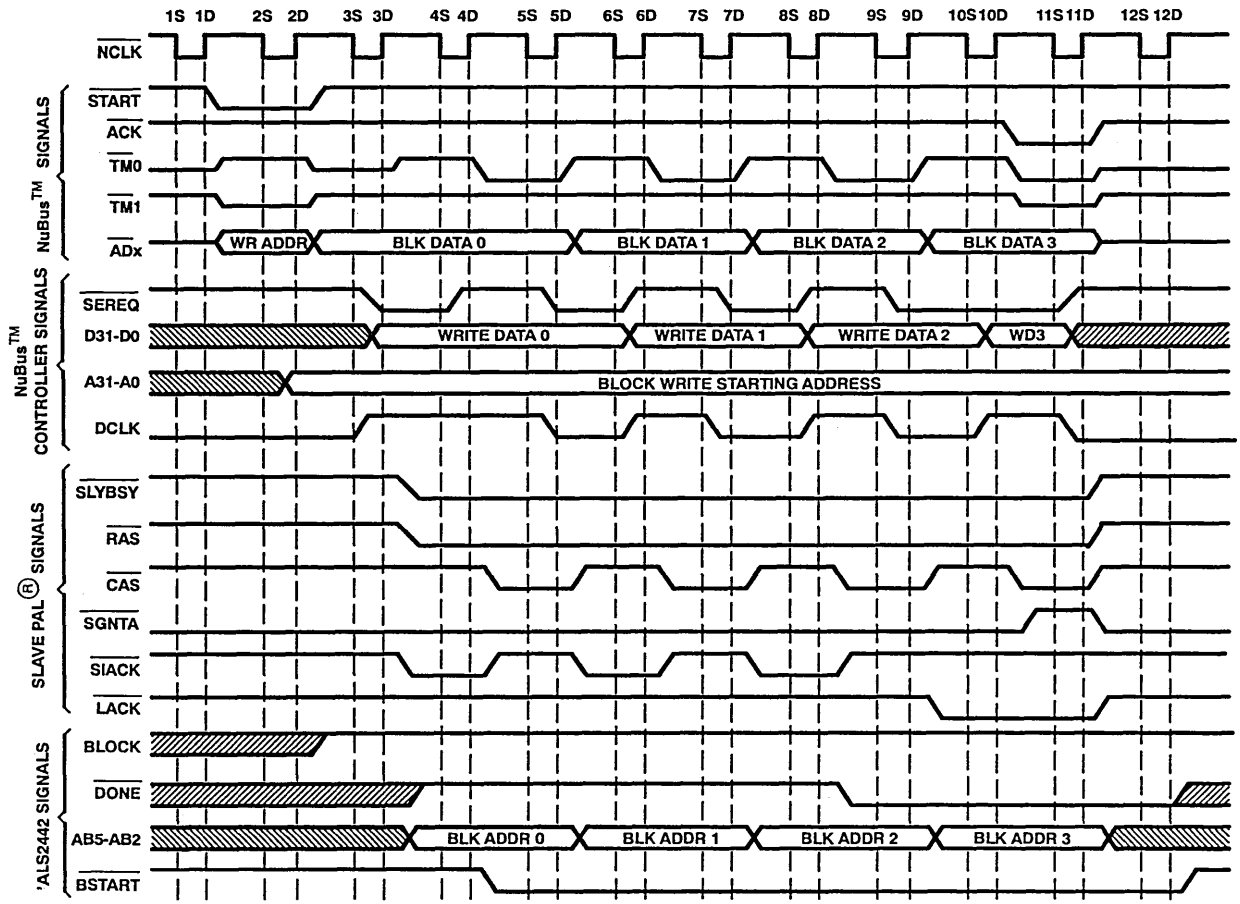


Figure 7. Block Write Transfer (4 Words)

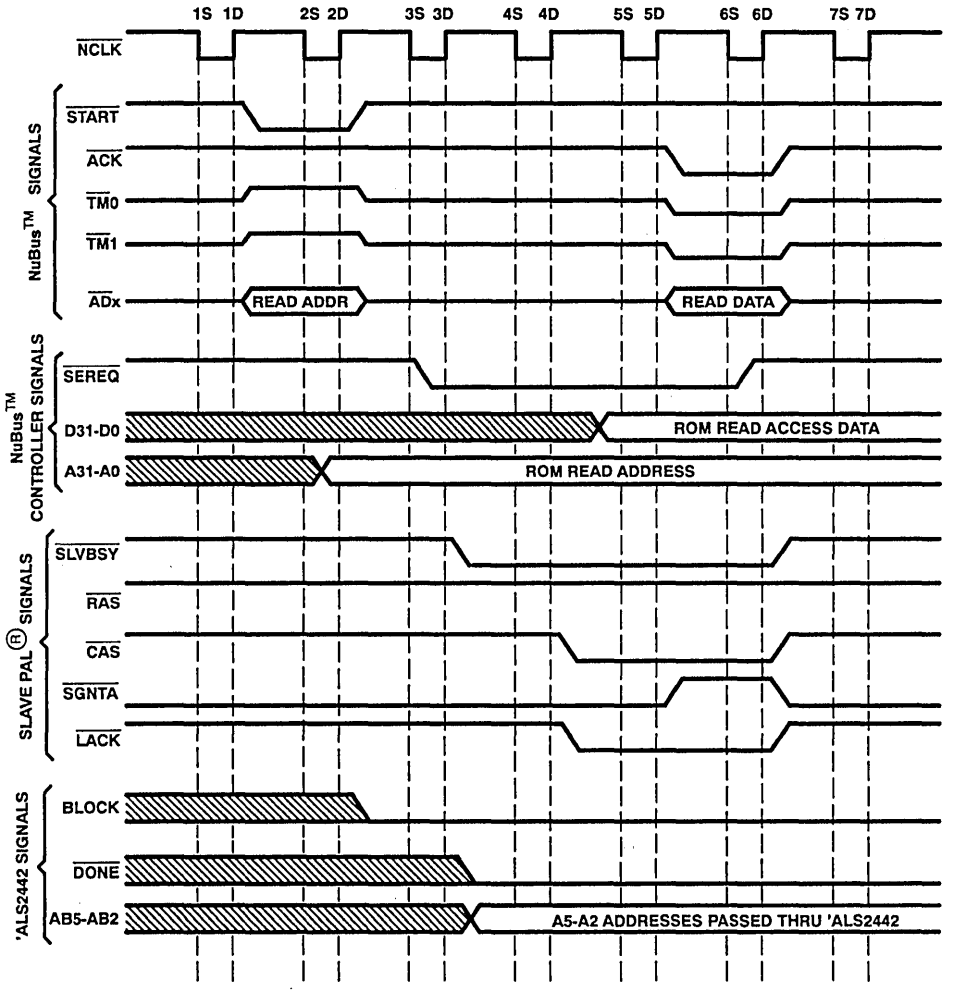


Figure 8. NuBus™ ROM Read Cycle

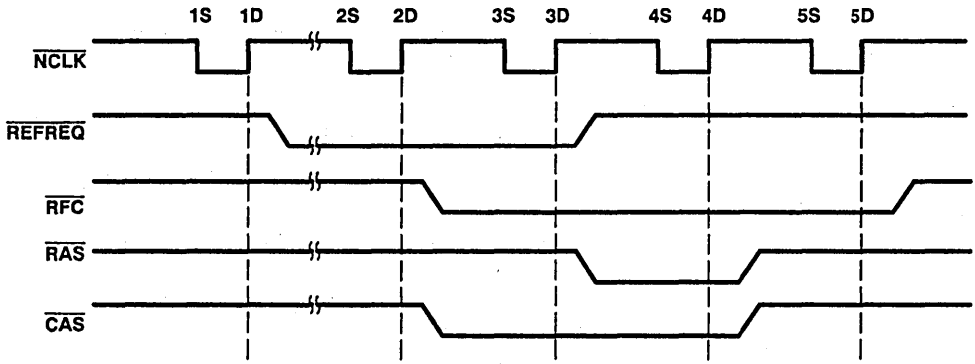


Figure 9. DRAM Refresh Sequence

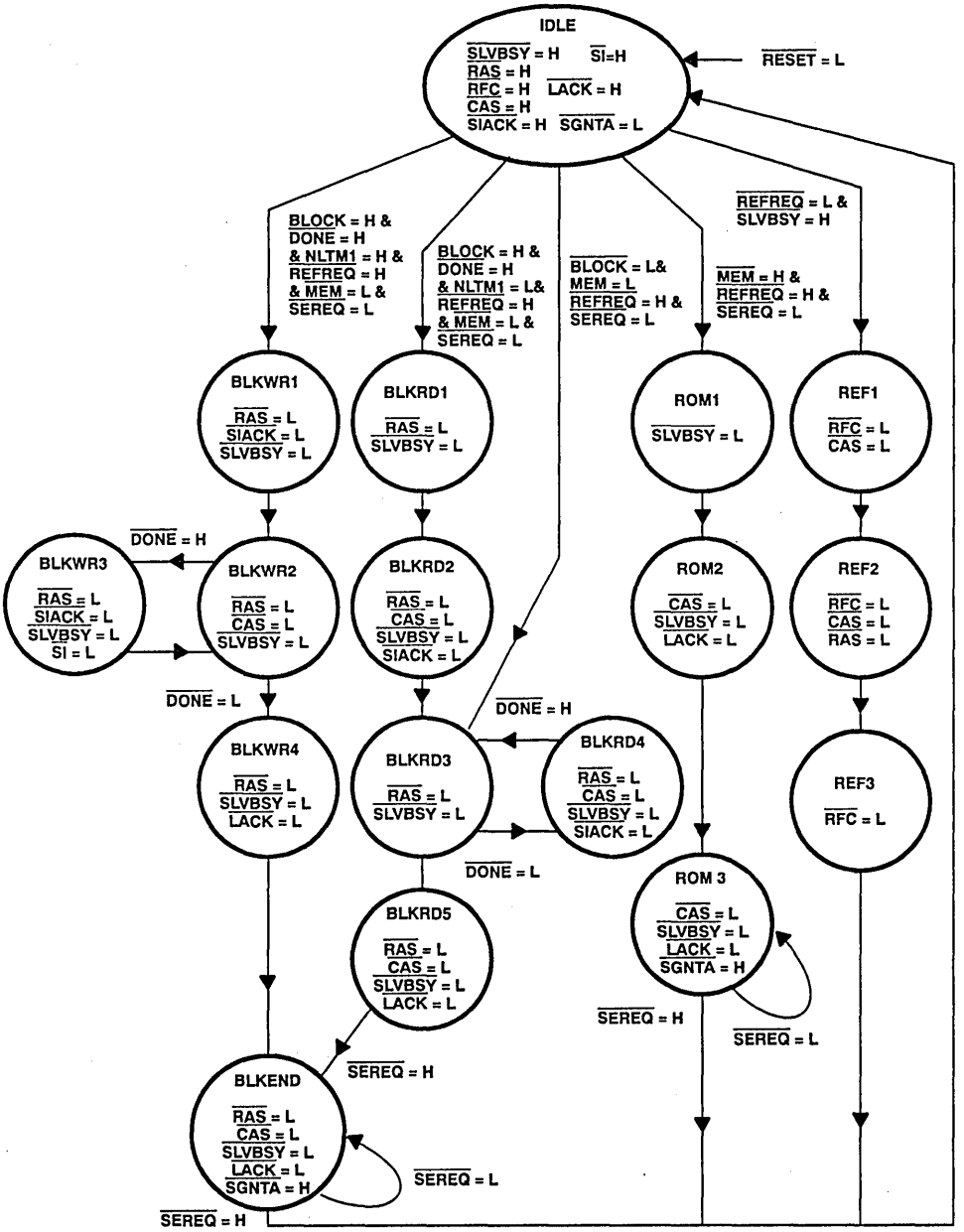


Figure 10. Slave PAL® State Diagram

Appendix A

```
Module SLAVEPAL flag '-r3'
       title 'NuBus Block Transfer SLAVE PAL
       Robert K. Breuninger, TEXAS INSTRUMENTS, APRIL 27, 1989'

       NBSLAVE device 'P16R8';

" input pin assignments

   NCLK_       PIN 1;      "Buffered NuBus clock
   RESET_      PIN 2;      "Buffered NuBus reset
   SEREQ_      PIN 3;      "Slave External Request
   DONE_       PIN 4;      "Transfer Complete
   MEM_        PIN 5;      "DRAM decode
   REFREQ_     PIN 6;      "Refresh Request
   BLOCK       PIN 7;      "Block transfer decode
   NLTM1       PIN 8;      "NuBus Latched TM1

" output pin assignments

   SGNTA_      PIN 12;     "Inverted Slave Grant Access
   LACK_       PIN 13;     "Local Acknowledge
   RFC_        PIN 14;     "Refresh Complete
   SIACK_      PIN 15;     "Slave Interim Acknowledge
   S1_         PIN 16;     "State Identifier
   CAS_        PIN 17;     "Column Address Strobe
   RAS_        PIN 18;     "Row Address Strobe
   SLVBSY_     PIN 19;     "Slave Busy

"intermediate declaration
   H,L,C,X = 1,0,.c.,.X.;

equations


  SGNTA_    :=  !RAS_ & !SLVBSY_ & S1_ & !LACK_ & !SGNTA_ & !MEM_ & RESET_
            #   RAS_ & !SLVBSY_ & S1_ & !LACK_ & !SGNTA_ & MEM_ & RESET_
            #   SGNTA_ & !LACK_ & !SEREQ_ & RESET_;

  !LACK_    :=  !SLVBSY_ & !DONE_ & !RAS_ & !CAS_ & SIACK_ & S1_ & LACK_ & RESET_
            #   !LACK_ & !SEREQ_ & RESET_
            #   !RAS_ & !SLVBSY_ & CAS_ & SIACK_ & S1_ & !DONE_ & RESET_
            #   !SLVBSY_ & RAS_ & CAS_ & SIACK_ & S1_ & LACK_ & RESET_
            #   !RAS_ & !SLVBSY_ & CAS_ & SIACK_ & S1_ & !LACK_ & RESET_;

  !RFC_     :=  !REFREQ_ & RFC_ & SLVBSY_ & RESET_
            #   !RFC_ & !CAS_ & RESET_;

  !SIACK_   :=  REFREQ_ & RFC_ & !SEREQ_ & BLOCK & !MEM_ & SLVBSY_ & NLTM1 & RESET_
            #   !RAS_ & !CAS_ & !SLVBSY_ & SIACK_ & LACK_ & DONE_ & RESET_
            #   !RAS_ & CAS_ & !SLVBSY_ & !S1_ & SIACK_ & LACK_ & RESET_
            #   !RAS_ & CAS_ & !SLVBSY_ & SIACK_ & DONE_ & LACK_ & RESET_;

  !S1_      :=  REFREQ_ & BLOCK & !SEREQ_ & !NLTM1 & S1_ & SLVBSY_ & !MEM_ & RFC_ & DONE_ & RESET_
            #   SIACK_ & !SLVBSY_ & !S1_ & !RAS_ & CAS_ & RESET_
            #   !RAS_ & !CAS_ & !SLVBSY_ & SIACK_ & S1_ & DONE_ & LACK_ & RESET_;
```

```
!CAS_     :=  !REFREQ_ & SLVBSY_ & CAS_ & RFC_ & RESET_
          #   !RFC_ & !CAS_ & RAS_ & RESET_
          #   !RAS_ & !SLVBSY_ & CAS_ & RESET_
          #   !CAS_ & !LACK_ & !SEREQ_ & RESET_
          #   !SLVBSY_ & RAS_ & CAS_ & S1_ & SIACK_ & RFC_ & RESET_;

!RAS_     :=  REFREQ_ & !SEREQ_ & !MEM_ & RFC_ & SLVBSY_ & RESET_
          #   !RAS_ & !SLVBSY_ & LACK_ & RESET_
          #   !RAS_ & !LACK_ & !SLVBSY_ & CAS_ & RESET_
          #   !RFC_ & RAS_ & !CAS_ & RESET_
          #   !RAS_ & !CAS_ & !LACK_ & !SLVBSY_ & S1_ & !SEREQ_ & RESET_;

!SLVBSY_  :=  RFC_ & REFREQ_ & !SEREQ_ & RESET_
          #   !SLVBSY_ & !SEREQ_ & RESET_
          #   !SLVBSY_ & LACK_ & RESET_
          #   !SLVBSY_ & !LACK_ & !RAS_ & CAS_ * S1_ & RESET_;


test_vectors 'RESET TEST'

([NCLK_,RESET_,SEREQ_,DONE_,MEM_,REFREQ_,BLOCK,NLTM1]->[SLVBSY_,RAS_,CAS_,SGNTA_,SIACK_,LACK_,RFC_,S1_])
[ C ,  L ,  X  ,  X ,  X ,   X  ,  X ,  X ]->[  H  , H , H , L  ,  H  ,  H , H , H ];
[ C ,  H ,  H  ,  H ,  X ,   H  ,  X ,  X ]->[  H  , H , H , L  ,  H  ,  H , H , H ];


test_vectors 'NORMAL NON-BLOCK DRAM READ TRANSFERS'

([NCLK_,RESET_,SEREQ_,DONE_,MEM_,REFREQ_,BLOCK,NLTM1]->[SLVBSY_,RAS_,CAS_,SGNTA_,SIACK_,LACK_,RFC_,S1_])
[ C ,  H ,  H  ,  X ,  X ,   H  ,  X ,  X ]->[  H  , H , H , L  ,  H  ,  H , H , H ];
[ C ,  H ,  L  ,  X ,  L ,   H  ,  L ,  L ]->[  L  , L , H , L  ,  H  ,  H , H , H ];
[ C ,  H ,  L  ,  L ,  L ,   H  ,  L ,  L ]->[  L  , L , L , L  ,  H  ,  L , H , H ];
[ C ,  H ,  L  ,  L ,  L ,   H  ,  L ,  L ]->[  L  , L , L , H  ,  H  ,  L , H , H ];
[ C ,  H ,  H  ,  L ,  L ,   H  ,  L ,  L ]->[  H  , H , H , L  ,  H  ,  H , H , H ];
[ C ,  H ,  H  ,  X ,  L ,   H  ,  L ,  L ]->[  H  , H , H , L  ,  H  ,  H , H , H ];


test_vectors 'NORMAL NON-BLOCK DRAM WRITE TRANSFERS'

([NCLK_,RESET_,SEREQ_,DONE_,MEM_,REFREQ_,BLOCK,NLTM1]->[SLVBSY_,RAS_,CAS_,SGNTA_,SIACK_,LACK_,RFC_,S1_])
[ C ,  H ,  H  ,  X ,  X ,   H  ,  X ,  X ]->[  H  , H , H , L  ,  H  ,  H , H , H ];
[ C ,  H ,  L  ,  X ,  L ,   H  ,  L ,  H ]->[  L  , L , H , L  ,  H  ,  H , H , H ];
[ C ,  H ,  L  ,  L ,  L ,   H  ,  L ,  H ]->[  L  , L , L , L  ,  H  ,  L , H , H ];
[ C ,  H ,  L  ,  L ,  L ,   H  ,  L ,  H ]->[  L  , L , L , H  ,  H  ,  L , H , H ];
[ C ,  H ,  H  ,  L ,  L ,   H  ,  L ,  H ]->[  H  , H , H , L  ,  H  ,  H , H , H ];
[ C ,  H ,  H  ,  X ,  L ,   H  ,  L ,  H ]->[  H  , H , H , L  ,  H  ,  H , H , H ];


test_vectors 'NORMAL NON-BLOCK ROM READ TRANSFERS'

([NCLK_,RESET_,SEREQ_,DONE_,MEM_,REFREQ_,BLOCK,NLTM1]->[SLVBSY_,RAS_,CAS_,SGNTA_,SIACK_,LACK_,RFC_,S1_])
[ C ,  H ,  H  ,  X ,  X ,   H  ,  X ,  X ]->[  H  , H , H , L  ,  H  ,  H , H , H ];
[ C ,  H ,  L  ,  X ,  H ,   H  ,  L ,  L ]->[  L  , H , H , L  ,  H  ,  H , H , H ];
[ C ,  H ,  L  ,  L ,  H ,   H  ,  L ,  L ]->[  L  , H , L , L  ,  H  ,  L , H , H ];
[ C ,  H ,  L  ,  L ,  H ,   H  ,  L ,  L ]->[  L  , H , L , H  ,  H  ,  L , H , H ];
[ C ,  H ,  H  ,  L ,  H ,   H  ,  L ,  L ]->[  H  , H , H , L  ,  H  ,  H , H , H ];
[ C ,  H ,  H  ,  X ,  H ,   H  ,  L ,  L ]->[  H  , H , H , L  ,  H  ,  H , H , H ];
```

```
test_vectors 'BLOCK READ TRANSFERS (2 WORDS)'

([NCLK_,RESET_,SEREQ_,DONE_,MEM_,REFREQ_,BLOCK,NLTM1]->[SLVBSY_,RAS_,CAS_,SGNTA_,SIACK_,LACK_,RFC_,S1_])
[ C , H , H , X , X , H , X , X ]->[ H , H , H , L , H , H , H , H ];
[ C , H , L , X , L , H , H , L ]->[ L , L , H , L , H , H , H , H ];
[ C , H , L , H , L , H , H , L ]->[ L , L , L , L , L , H , H , H ];
[ C , H , H , L , L , H , H , L ]->[ L , L , H , L , H , H , H , H ];
[ C , H , L , L , L , H , H , L ]->[ L , L , L , L , H , L , H , H ];
[ C , H , L , L , L , H , H , L ]->[ L , L , L , H , H , L , H , H ];
[ C , H , H , L , L , H , H , L ]->[ H , H , H , L , H , H , H , H ];
[ C , H , H , X , L , H , H , L ]->[ H , H , H , L , H , H , H , H ];

test_vectors 'BLOCK READ TRANSFERS (4 WORDS)'

([NCLK_,RESET_,SEREQ_,DONE_,MEM_,REFREQ_,BLOCK,NLTM1]->[SLVBSY_,RAS_,CAS_,SGNTA_,SIACK_,LACK_,RFC_,S1_])
[ C , H , H , X , X , H , X , X ]->[ H , H , H , L , H , H , H , H ];
[ C , H , L , X , L , H , H , L ]->[ L , L , H , L , H , H , H , H ];
[ C , H , L , H , L , H , H , L ]->[ L , L , L , L , L , H , H , H ];
[ C , H , H , H , L , H , H , L ]->[ L , L , H , L , H , H , H , H ];
[ C , H , L , H , L , H , H , L ]->[ L , L , L , L , L , H , H , H ];
[ C , H , H , H , L , H , H , L ]->[ L , L , H , L , H , H , H , H ];
[ C , H , L , H , L , H , H , L ]->[ L , L , L , L , L , H , H , H ];
[ C , H , H , L , L , H , H , L ]->[ L , L , H , L , H , H , H , H ];
[ C , H , L , L , L , H , H , L ]->[ L , L , L , L , L , H , L , H ];
[ C , H , H , L , L , H , H , L ]->[ H , H , H , L , H , H , H , H ];
[ C , H , H , X , L , H , H , L ]->[ H , H , H , L , H , H , H , H ];

test_vectors 'BLOCK WRITE TRANSFERS (2 WORDS)'

([NCLK_,RESET_,SEREQ_,DONE_,MEM_,REFREQ_,BLOCK,NLTM1]->[SLVBSY_,RAS_,CAS_,SGNTA_,SIACK_,LACK_,RFC_,S1_])
[ C , H , H , X , X , H , X , X ]->[ H , H , H , L , H , H , H , H ];
[ C , H , L , X , L , H , H , H ]->[ L , L , H , L , L , H , H , H ];
[ C , H , H , H , L , H , H , H ]->[ L , L , L , L , H , H , H , H ];
[ C , H , L , L , L , H , H , H ]->[ L , L , H , L , H , L , H , H ];
[ C , H , L , L , L , H , H , H ]->[ L , L , L , H , H , L , H , H ];
[ C , H , H , L , L , H , H , H ]->[ H , H , H , L , H , H , H , H ];
[ C , H , H , L , L , H , H , H ]->[ H , H , H , L , H , H , H , H ];
[ C , H , H , X , L , H , H , H ]->[ H , H , H , L , H , H , H , H ];

test_vectors 'BLOCK WRITE TRANSFERS (4 WORDS)'

([NCLK_,RESET_,SEREQ_,DONE_,MEM_,REFREQ_,BLOCK,NLTM1]->[SLVBSY_,RAS_,CAS_,SGNTA_,SIACK_,LACK_,RFC_,S1_])
[ C , H , H , X , X , H , X , X ]->[ H , H , H , L , H , H , H , H ];
[ C , H , L , X , L , H , H , H ]->[ L , L , H , L , L , H , H , H ];
[ C , H , H , H , L , H , H , H ]->[ L , L , L , L , H , H , H , H ];
[ C , H , L , H , L , H , H , H ]->[ L , L , H , L , L , H , H , L ];
[ C , H , H , H , L , H , H , H ]->[ L , L , L , L , H , H , H , H ];
[ C , H , L , H , L , H , H , H ]->[ L , L , H , L , L , H , H , L ];
[ C , H , H , H , L , H , H , H ]->[ L , L , L , L , H , H , H , H ];
[ C , H , L , L , L , H , H , H ]->[ L , L , H , L , H , L , H , H ];
[ C , H , L , L , L , H , H , H ]->[ L , L , L , H , H , L , H , H ];
[ C , H , H , L , L , H , H , H ]->[ H , H , H , L , H , H , H , H ];
[ C , H , H , L , L , H , H , H ]->[ H , H , H , L , H , H , H , H ];
[ C , H , H , X , L , H , H , H ]->[ H , H , H , L , H , H , H , H ];
```

```
test_vectors 'DRAM REFRESH CYCLES'

([NCLK_,RESET_,SEREQ_,DONE_,MEM_,REFREQ_,BLOCK,NLTM1]->[SLVBSY_,RAS_,CAS_,SGNTA_,SIACK_,LACK_,RFC_,S1_])
[ C , H , H , X , X , H , X , X ]->[ H , H , H , L , H , H , H , H ];
[ C , H , H , X , X , L , X , X ]->[ H , H , L , L , H , H , L , H ];
[ C , H , H , X , X , L , X , X ]->[ H , L , L , L , H , H , L , H ];
[ C , H , H , X , X , H , X , X ]->[ H , H , H , L , H , H , L , H ];
[ C , H , H , X , X , H , X , X ]->[ H , H , H , L , H , H , H , H ];

test_vectors 'SIMULTANEOUS REFRESH REQUEST/BLOCK READ (4 WORDS)'

([NCLK_,RESET_,SEREQ_,DONE_,MEM_,REFREQ_,BLOCK,NLTM1]->[SLVBSY_,RAS_,CAS_,SGNTA_,SIACK_,LACK_,RFC_,S1_])
[ C , H , H , X , X , H , X , X ]->[ H , H , H , L , H , H , H , H ];
[ C , H , L , X , L , L , H , L ]->[ H , H , L , L , H , H , L , H ];
[ C , H , L , H , L , L , H , L ]->[ H , L , L , L , H , H , L , H ];
[ C , H , L , H , L , H , H , L ]->[ H , H , H , L , H , H , L , H ];
[ C , H , L , H , L , H , H , L ]->[ H , H , H , L , H , H , H , H ];
[ C , H , L , H , L , H , H , L ]->[ L , L , H , L , H , H , H , L ];
[ C , H , L , H , L , H , H , L ]->[ L , L , L , L , L , H , H , L ];
[ C , H , H , H , L , H , H , L ]->[ L , L , H , L , H , H , H , H ];
[ C , H , L , H , L , H , H , L ]->[ L , L , L , L , L , H , H , H ];
[ C , H , H , H , L , H , H , L ]->[ L , L , H , L , H , H , H , H ];
[ C , H , L , H , L , H , H , L ]->[ L , L , L , L , L , H , H , H ];
[ C , H , H , L , L , H , H , L ]->[ L , L , H , L , H , H , H , H ];
[ C , H , L , L , L , H , H , L ]->[ L , L , L , L , H , L , H , H ];
[ C , H , L , L , L , H , H , L ]->[ L , L , L , H , H , L , H , H ];
[ C , H , H , L , L , H , H , L ]->[ H , H , H , L , H , H , H , H ];
[ C , H , H , X , L , H , H , L ]->[ H , H , H , L , H , H , H , H ];

test_vectors 'BLOCK WRITE TRANSFERS (4 WORDS)/REFRESH REQUEST'

([NCLK_,RESET_,SEREQ_,DONE_,MEM_,REFREQ_,BLOCK,NLTM1]->[SLVBSY_,RAS_,CAS_,SGNTA_,SIACK_,LACK_,RFC_,S1_])
[ C , H , H , X , X , H , X , X ]->[ H , H , H , L , H , H , H , H ];
[ C , H , L , X , L , H , H , H ]->[ L , L , H , L , L , H , H , H ];
[ C , H , H , H , L , L , H , H ]->[ L , L , L , L , H , H , H , H ];
[ C , H , L , H , L , L , H , H ]->[ L , L , H , L , L , H , H , L ];
[ C , H , H , H , L , L , H , H ]->[ L , L , L , L , H , H , H , H ];
[ C , H , L , H , L , L , H , H ]->[ L , L , H , L , L , H , H , L ];
[ C , H , H , H , L , L , H , H ]->[ L , L , L , L , H , H , H , H ];
[ C , H , L , L , L , L , H , H ]->[ L , L , H , L , H , L , H , H ];
[ C , H , L , L , L , L , H , H ]->[ L , L , L , H , H , L , H , H ];
[ C , H , H , L , L , L , H , H ]->[ H , H , H , L , H , H , H , H ];
[ C , H , H , X , X , L , X , X ]->[ H , H , L , L , H , H , L , H ];
[ C , H , H , X , X , L , X , X ]->[ H , L , L , L , H , H , L , H ];
[ C , H , H , X , X , H , X , X ]->[ H , H , H , L , H , H , L , H ];
[ C , H , H , X , X , H , X , X ]->[ H , H , H , L , H , H , H , H ];

END
```

Designing Simple NuBus™ Slave-Only Applications

Using TI's SN74ACT2440 and SN74BCT2420

Larry Moriarty, Robert K. Breuninger
with contributions from Kyle Neuman

TEXAS
INSTRUMENTS

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Introduction

With the recent introduction of 32-bit microprocessors, new 32-bit back-plane bus structures have also been developed. These new bus structures have been designed to exploit the higher performance offered by these new microprocessors. One such bus structure is found in the NuBus™ product family.

Texas Instruments has recently introduced two devices, the SN74ACT2440 and the SN74BCT2420, which have been designed to support the NuBus™ architecture. These devices are intended to allow a simple general-purpose interface to NuBus™ the architecture. Typical configurations include master-only, slave-only, and master/slave.

The purpose of this application report is to demonstrate a simple NuBus™ slave-only application that utilizes the 'BCT2420 and 'ACT2440. From this example, the reader will learn what type of logic is necessary to implement a NuBus™ slave-only card. In addition, this application report also highlights three new products from Texas Instruments: the TIBPAD18N8 Programmable Address Decoder, the TIB82S167 Programmable Logic Sequencer, and the SN74ACT4503 Dynamic RAM Controller.

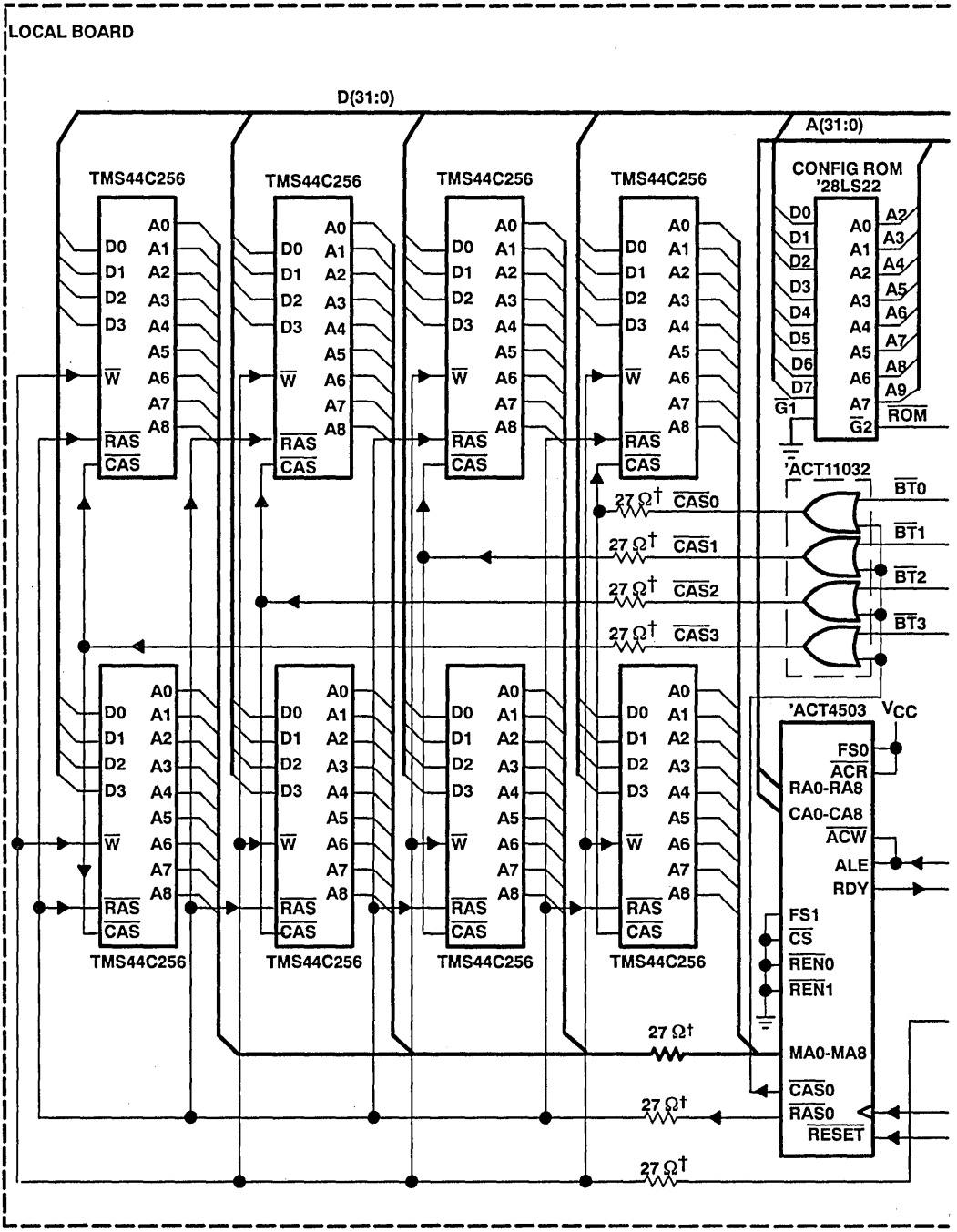
Slave-Only Example

When a NuBus™ application does not require ownership of the bus, it is said to be slave-only. The intended application is either written to or read from, but does not initiate a NuBus™ transaction. Figure 1 shows a typical NuBus™ slave-only application. In this example, 1M byte of dynamic memory (256K by 32-bits wide) is addressable from a NuBus™ card slot. In addition to DRAM memory, 1K byte of read-only-memory (ROM) is available for system configuration.

Overview of Operation

The 'ACT2440 NuBus™ controller is easily configured for slave-only applications and, as shown in Figure 1, requires very few interface signals. The 'TIB82S167 Programmable Logic Sequencer provides all the control signals necessary for interfacing the NuBus™ controller with DRAM or ROM.

The SN74ACT4503 Dynamic Memory Controller handles address multiplexing, access timing, and refresh arbitration for the DRAM memory. Address decoding is handled by the Programmable Address Decoder 'TIBPAD16N8. Byte control is implemented via the SN74ACT11032, in conjunction with the byte control signals provided by the 'ACT2440 NuBus™ Controller.



† Series damping resistors are recommended but may not be required, depending upon the system environment.

Figure 1. Typical NuBus ™ Slave Only Application

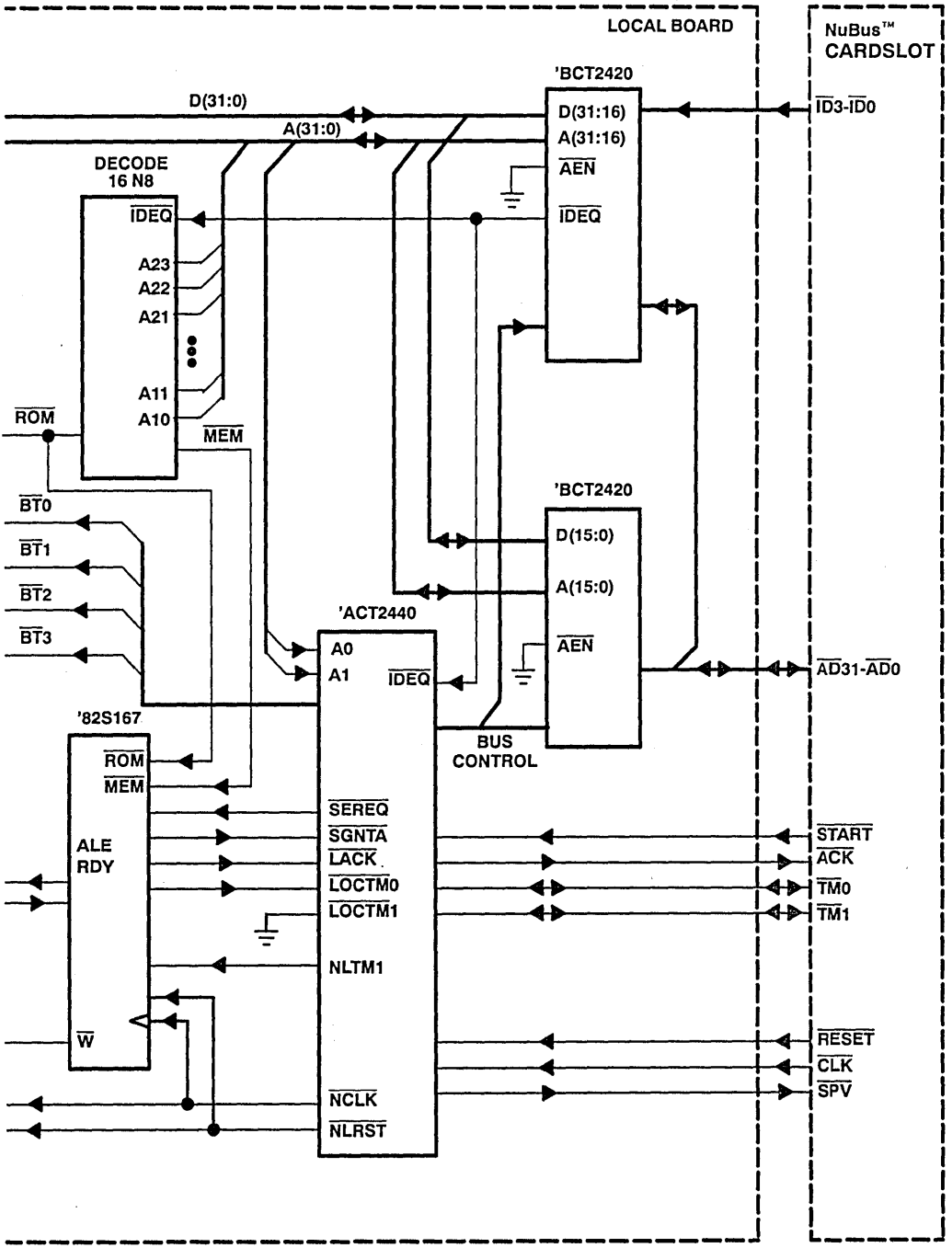


Figure 1. Typical NuBus™ Slave Only Application (continued)

Memory Decode

The NuBus™ architecture allows a full 32-bit address, which corresponds to 4G bytes of possible address space. The upper one-sixteenth (256 megabytes) of address space is normally referred to as super-slot space. Super-slot space is further divided into 16 regions of 16M bytes each. This address space is referred to as slot space. Each slot space is identified by a 4-bit ID code. NuBus™ addresses of the form $F(ID)xx xxxx refer to the slot space that belongs to each ID code.

All the circuitry required for decoding super-slot space and normal-slot space is contained on the 'ACT2420 NuBus™ Address/Data Transceivers. The $\overline{\text{IDEQ}}$ output is used for signaling the NuBus™ controller when it is being accessed by the NuBus™.

Table 1 shows the address decoding scheme used on the NuBus™ slave-only example shown in Figure 1.

Table 1. Address Decoding Scheme

DEVICE	ADDRESS RANGE	
	STARTING ADDRESS	FINAL ADDRESS
DRAM	F(ID)00 0000	F(ID)00 FFFF
ROM	F(ID)F8 0000	F(ID)F8 03FC
—	All other addresses invalid	

Addresses A0 and A1 are used by the 'ACT2440 for byte decoding. When a valid address has been presented on the NuBus™ $\overline{\text{AD}}$x lines, two outputs are provided by the 'TIBPAD16N8 Programmable Address Decoder for signaling the '82S167. The $\overline{\text{ROM}}$ output goes active (low) when ROM is being accessed. The $\overline{\text{MEM}}$ output goes active (low) when DRAM is being accessed. When both $\overline{\text{ROM}}$ and $\overline{\text{MEM}}$ are inactive, an invalid address is indicated.

Memory Controller

The 'ACT4503 Dynamic Memory Controller handles all of the address multiplexing, access timing, and refresh arbitration for the the DRAMs. The 'ACT4503 can be directly clocked by the buffered NuBus™ clock output signal ($\overline{\text{NCLK}}$) as provided by the 'ACT2440.

Refresh rate is selectable on the 'ACT4503 via the FS0 and FS1 input pins. In addition to selecting the refresh rate, the FS0 and FS1 input pins determine which clock edge is used for refresh/access arbitration. In order to guarantee refresh/access arbitration, the 'ACT4503 requires that the falling edge of access request (ALE) must not occur within 20 ns before to 0 ns after the arbitration clock edge. Since the NuBus™/memory controller ('82S167) generates the access request control signal (ALE) and operates off the same clock ($\overline{\text{NCLK}}$), then the best choice for the arbitration clock edge is low-to-high. This condition guarantees that the above requirement is not violated.

In the 'ACT4503, when FS0 is high and FS1 is low, refresh cycles are initiated internally and access arbitration occurs on the low-to high clock edge. Therefore, the best

choice for refresh rate, when using a 10-MHz clock, is with FS0 high and FS1 low. Since both refresh rate and access arbitration require the same input conditions, FS0 can be tied permanently high and FS1 can be tied permanently low. If these two input conditions were not the same, the '82S167 would have to generate the correct input signals during reset and normal operation.

When the ALE input is taken high-to-low, access cycles are generated on the 'ACT4503. Byte control signals are generated by gating the $\overline{CAS}$ output signal with the byte control signals (BT0-BT3) provided by the 'ACT2440. A Ready (RDY) output signal on the 'ACT4503 signals the occurrence of an access grant cycle. This type of cycle occurs when an internal refresh request and an access request occur simultaneously. In this situation, the RDY output goes low, indicating that the access cycle will be delayed until the refresh cycle is completed. When the refresh cycle has completed, RDY goes high.

NuBus™ Controller

As shown Figure 1, only three input signals $\overline{SGNTA}$, $\overline{LACK}$, and $\overline{LOCTM0}$ are used for controlling the 'ACT2440 and four outputs signals $\overline{SEREQ}$, NLTM1, $\overline{NLRST}$, and $\overline{NCLK}$ are used for monitoring NuBus™ status. As mentioned previously, the buffered NuBus™ clock output ($\overline{NCLK}$) is used for clocking the NuBus™/Memory controller ('82S167) and the DRAM controller ('ACT4503). Using the same clock synchronizes both devices to the NuBus™ memory and the NuBus™ controller. The significance of all seven signals will be covered in more detail under the NuBus™/Memory controller section.

Addresses A0 and A1 are decoded by the 'ACT2440 to generate the byte control signals $\overline{BT0}$ through $\overline{BT3}$. The $\overline{IDEQ}$ output from the 'BCT2420 is connected to the 'ACT2440. This identification signal informs the local board when it is being accessed by the NuBus™ controller. Refer to the Memory Decode section for additional information.

The NuBus™ buffer control signals ($\overline{ACLK}$, $\overline{DCLK}$, $\overline{DEN}$, $\overline{A/D}$, and $\overline{ADEN}$) required by the 'BCT2420s are automatically generated by the 'ACT2440 NuBus™ Controller. As shown in Figure 1, the Address Enables ($\overline{AEN}$) on the 'BCT2420s are tied permanently low instead of being driven by the 'ACT2440. In slave-only applications, addresses can be enabled onto the local board sooner by tying $\overline{AEN}$ low. This can be an advantage in applications which are sensitive to access time, such as dynamic memory. In NuBus™ master applications, the $\overline{AEN}$ pin must be controlled by the NuBus™ controller.

NuBus™/Memory Controller

The interface between DRAM memory and the NuBus™ interface controller is handled by the NuBus™/Memory controller ('82S167). The NuBus™/Memory controller samples all of the input control signals being supplied by the NuBus™ controller ('ACT2440), DRAM memory controller ('ACT4503), and the memory decoder ('TIBPAD16N8). The NuBus™/Memory controller then proceeds to generate the appropriate control signals as required by the type of access.

Figure 2 shows the state diagram for the NuBus™/Memory controller. When a reset occurs on the NuBus™, the 'ACT2440 will generate a latched version ($\overline{\text{NLRST}}$) of the NuBus™ $\overline{\text{RESET}}$ signal. The $\overline{\text{NLRST}}$ signal is used to reset the NuBus™/Memory controller and the DRAM memory controller. A reset signal applied to the NuBus™/Memory controller forces the device into the IDLE state (S0) as described in the flow chart. As long as $\overline{\text{NLRST}}$ remains active (low), the NuBus™/Memory Controller will be forced into this state.

After $\overline{\text{NLRST}}$ high, the NuBus™/Memory controller waits for one of four possible input conditions to occur, a DRAM read cycle, a DRAM write cycle, a ROM read cycle, or an invalid access. The following paragraphs provide a brief description of each type of access cycle.

DRAM Read Cycle

When the Slave External Request ($\overline{\text{SEREQ}}$) signal is driven low and the NuBus™ latched TM1 (NLTM1) signal is driven low, a DRAM read is indicated . The NuBus™/Memory controller knows it is a DRAM read because the memory decode signal ($\overline{\text{MEM}}$) has been driven low and the ROM decode signal ($\overline{\text{ROM}}$) has been driven high. When the above conditions are met, the NuBus™/Memory controller forces ALE low, which causes the 'ACT4503 to initiate a DRAM access cycle.

Before the NuBus™/Memory controller signals the NuBus™ controller to acknowledge the read request, the NuBus™/Memory controller checks the RDY line for a refresh cycle (RDY low). If a refresh cycle is not in progress, the read request is acknowledged by forcing the $\overline{\text{LACK}}$ output low. If a refresh cycle is in progress, then the NuBus™ controller holds until RDY goes high. Figure 3 is a detailed timing diagram of the DRAM read cycle.

DRAM Write Cycle

The DRAM write cycle is identical to the DRAM read cycle except that the latched TM1 (NLTM1) signal is driven high by the NuBus™ controller which indicates a NuBus™ write cycle. During DRAM write cycles, the NuBus™/Memory controller forces the write output pin ($\overline{\text{W}}$) low. During DRAM read cycles, this output remains high for the entire cycle. Figure 4 is a detailed timing diagram of the DRAM write cycle.

ROM Read Cycle

A ROM read cycle is indicated when the $\overline{\text{SEREQ}}$ control line goes low and the memory decode indicates a ROM access ($\overline{\text{ROM}}$ low, $\overline{\text{MEM}}$ high). The NLTM1 control line must also be low to indicate a read cycle. Figure 5 is a detailed timing diagram of the ROM read cycle.

Invalid Access

An invalid access can occur when another master issues a valid card-slot address but resources are not available on the local board to respond to the request. In this situation, the NuBus™/Memory controller must respond to the access request with an error message. An invalid access is indicated when the two memory decode lines are both high ($\overline{\text{ROM}}$ high and $\overline{\text{MEM}}$ high) or when a ROM write is requested ($\overline{\text{NLTM1}}$ high).

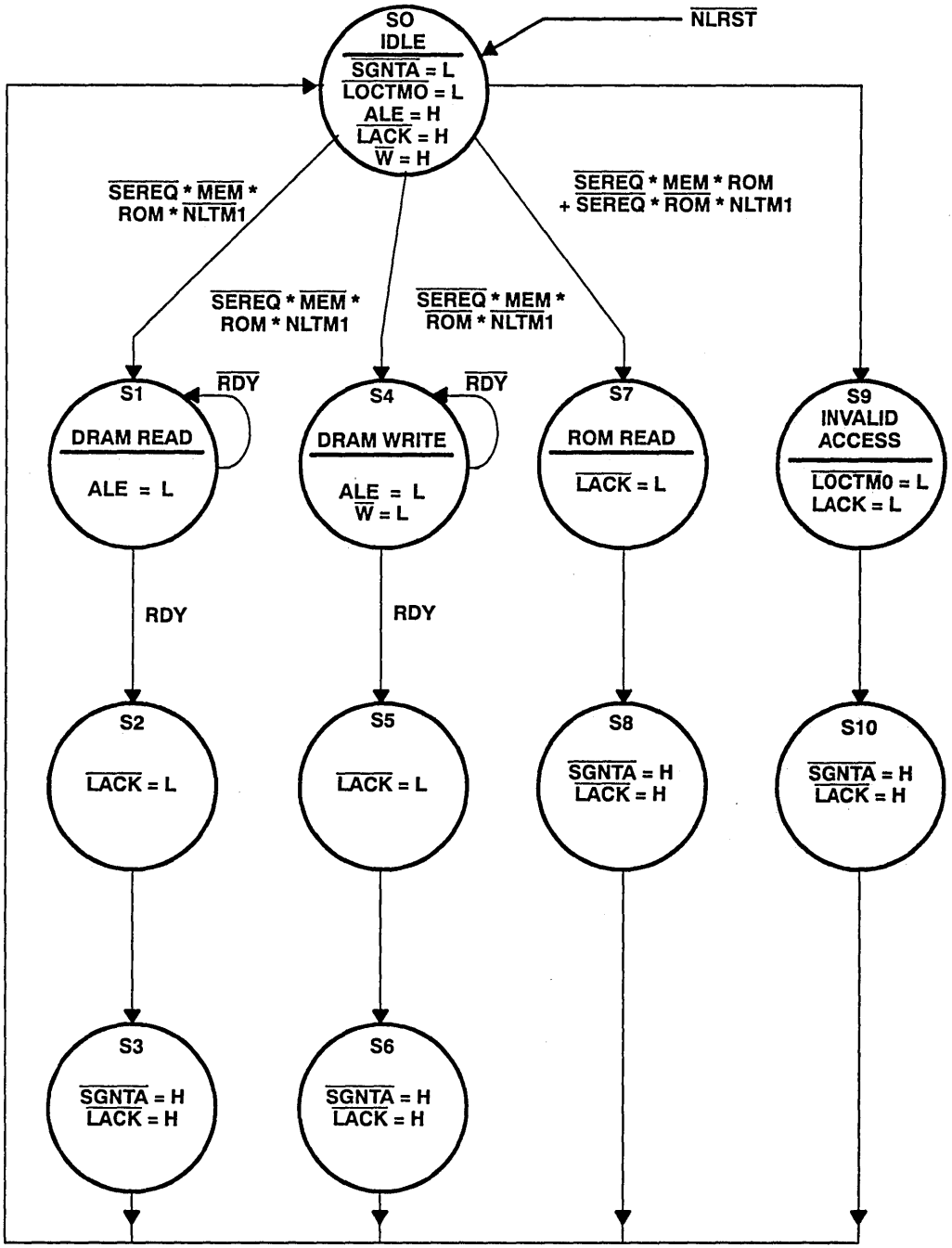


Figure 2. State Diagram for NuBus™/Memory Controller ('82S167)

When an invalid access occurs, the NuBus™ controller must acknowledge an error ($\overline{TM1}$ low and $\overline{TM0}$ high) on the NuBus™ ADx lines. Figure 6 is a detailed timing diagram of how the error message is communicated.

Software Support

The 'TIB82S167 and the 'TIBPAD16N8 are supported by two software packages. The software packages are CUPL, which is supported by Logical Devices Inc., and ABEL, which was created by and is supported by Future Net, a division of Data I/O Corp. Both of these software packages can be used to reduce equations and generate the fuse maps necessary to program the devices. Appendixes A and B show the CUPL source files, which can be used to generate the JEDEC files necessary for programming.

Summary

The NuBus™ architecture offers the system designer improved performance when expanding into the world of 32-bit microprocessors. By using the SN74ACT2440 and SN74BCT2420 NuBus™ chip set, a system designer can easily take advantage of the improved performance offered by the NuBus™ architecture. The example covered in this application report shows the type of logic that is necessary to implement a simple slave-only NuBus™ card.

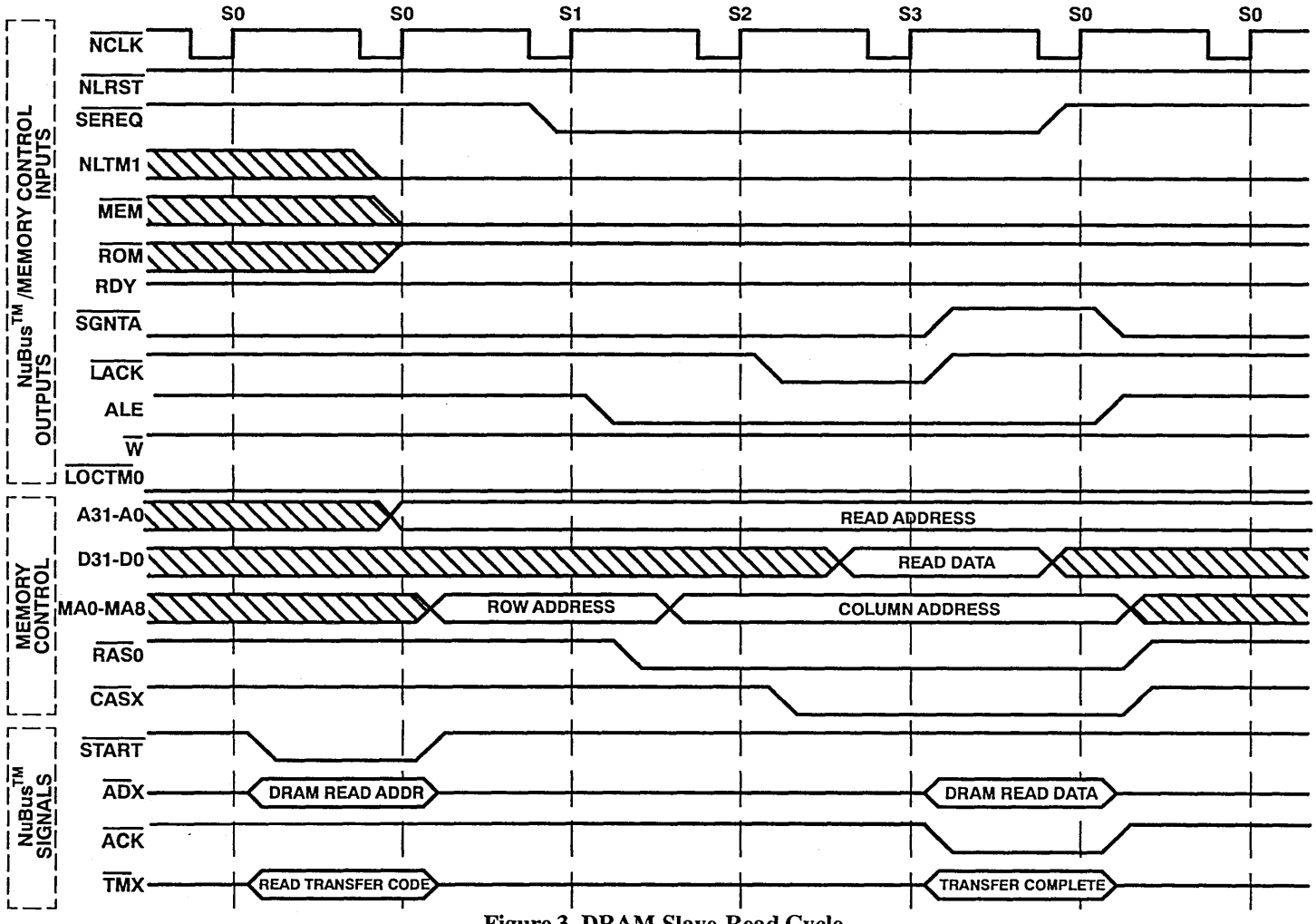


Figure 3. DRAM Slave-Read Cycle

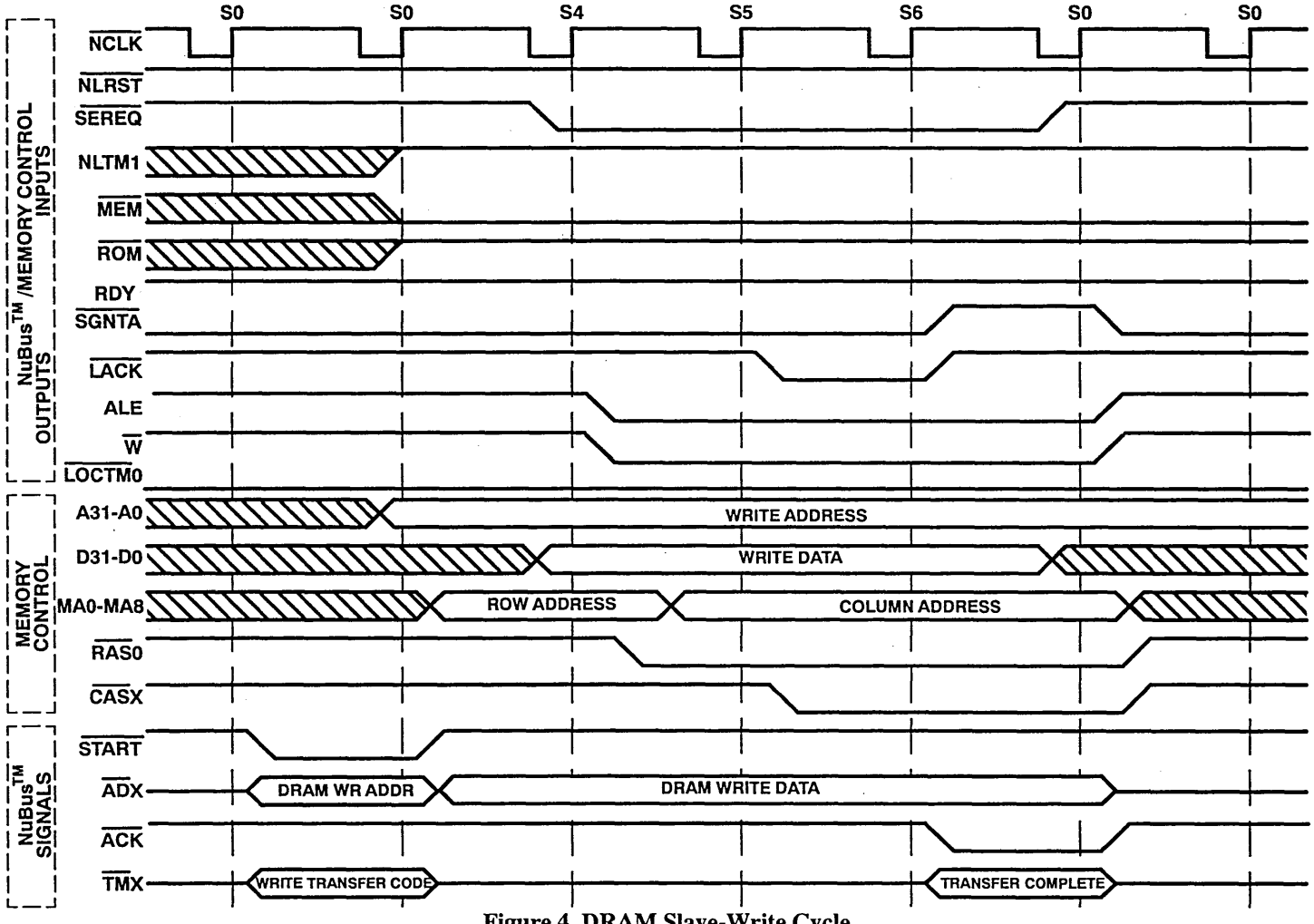


Figure 4. DRAM Slave-Write Cycle

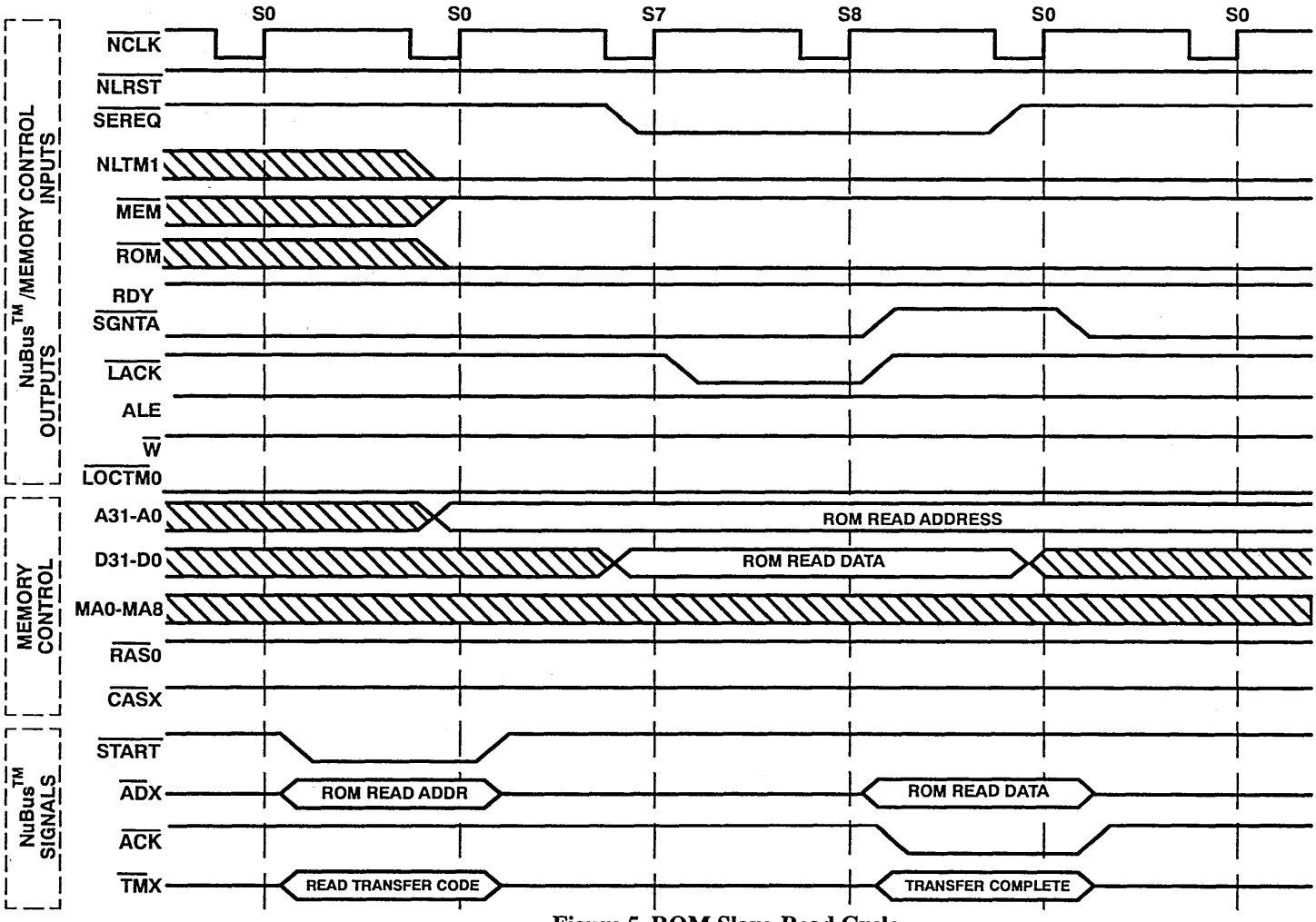


Figure 5. ROM Slave-Read Cycle

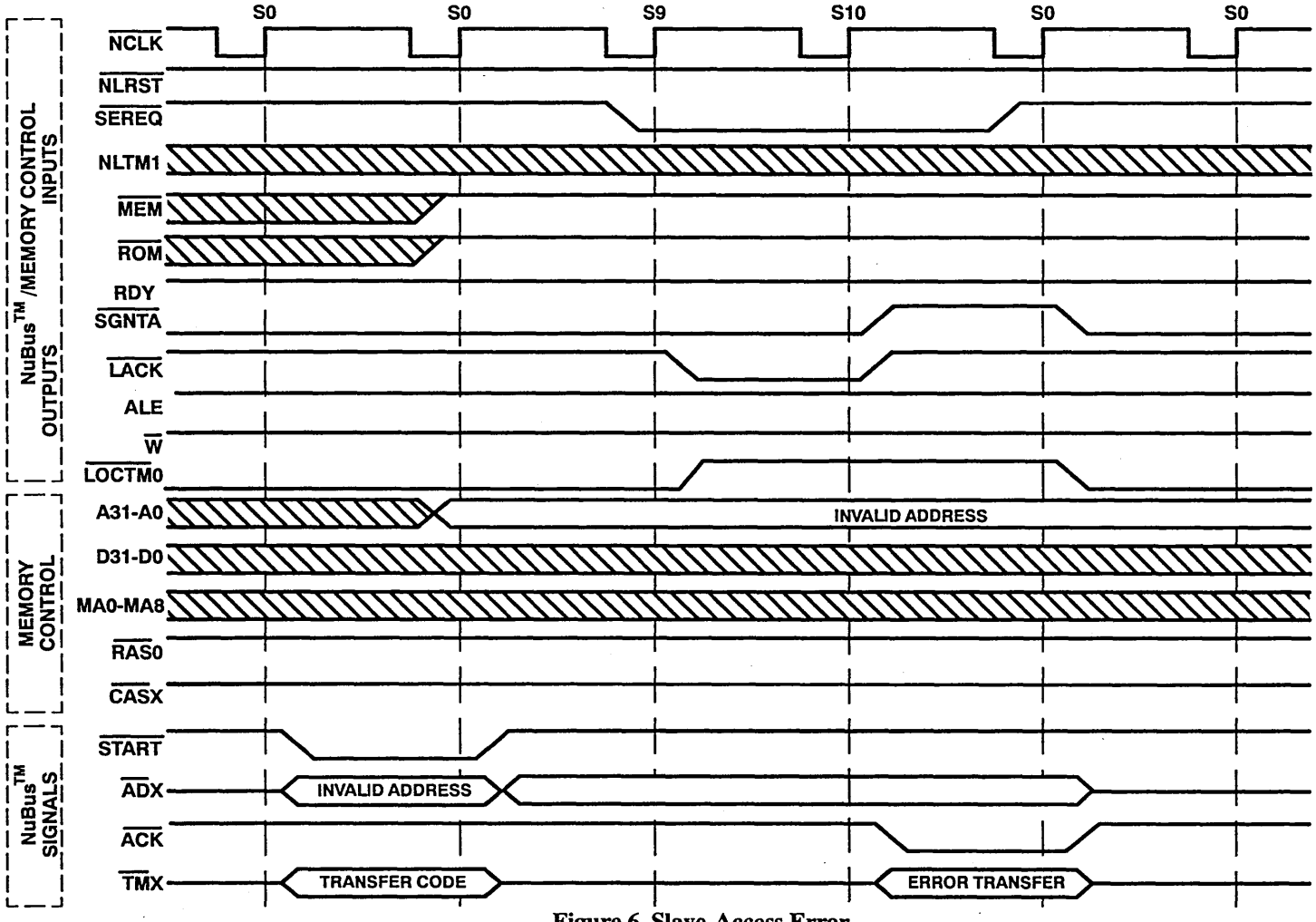


Figure 6. Slave-Access Error

Appendix A

```
*****************************************************************
                              DECODE
*****************************************************************
CUPL            2.50a Serial# MD-250-3238
Device          p16n8  Library DLIB-h-24-1
Created         Mon Nov 13 15:20:47 1989
Name            DECODE
Partno          TIBPAD16N8-7
Revision        01
Date            10/06/88
Designer        KYLE NEMAN
Company         TEXAS INSTRUMENTS
Assembly        None
Location        DALLAS, TEXAS

=================================================================
                      Expanded Product Terms
=================================================================
MEM_ =>
    !A20 & !A21 & !A22 & !A23 & !IDEQ_
ROM_ =>
    !A10 & !A11 & !A12 & !A13 & !A14 & !A15 & !A16 & !A17 & !A18 &
    A19 & A20 & A21 & A22 & A23 & !IDEQ_
A19.oe  =>
    0
A20.oe  =>
    0
A21.oe  =>
    0
A22.oe  =>
    0
A23.oe  =>
    0
IDEQ_.oe =>
    0
MEM_.oe =>
    1
ROM_.oe =>
    1
```

Symbol Table

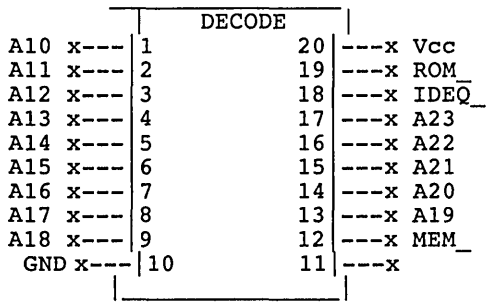
Pin Pol	Variable Name	Ext	Pin	Type	Pterms Used	Max Pterms	Min Level
	A10		1	V	-	-	-
	A11		2	V	-	-	-
	A12		3	V	-	-	-
	A13		4	V	-	-	-
	A14		5	V	-	-	-
	A15		6	V	-	-	-
	A16		7	V	-	-	-
	A17		8	V	-	-	-
	A18		9	V	-	-	-
	A19		13	V	-	-	-
	A20		14	V	-	-	-
	A21		15	V	-	-	-
	A22		16	V	-	-	-
	A23		17	V	-	-	-
	IDEQ_		18	V	-	-	-
	MEM_		12	V	1	1	1
	ROM_		19	V	1	1	1
	A19	oe	13	D	1	1	0
	A20	oe	14	D	1	1	0
	A21	oe	15	D	1	1	0
	A22	oe	16	D	1	1	0
	A23	oe	17	D	1	1	0
	IDEQ_	oe	18	D	1	1	0
	MEM_	oe	12	D	1	1	0
	ROM_	oe	19	D	1	1	0

LEGEND F : field D : default variable M : extended node
N : node I : intermediate variable T : function
V : variable X : extended variable U : undefined

```
=====================================================================
                          Fuse Plot
=====================================================================
Pin #19
 0000 --------------------------------
 0032 -x-x-x-x-xx--xx--xx--xx--xx--x--
Pin #18
 0064 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 0096 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #17
 0128 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 0160 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #16
 0192 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 0224 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #15
 0256 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 0288 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #14
 0320 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 0352 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #13
 0384 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 0416 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #12
 0448 --------------------------------
 0480 -------x---x---x---x---x--------

LEGEND    X : fuse not blown
          - : fuse blown
```

Chip Diagram



```
Partno    IBPAD16N8-7;
Name      DECODE;
Date1     0/06/88;
Revision  01;
Designer  KYLE NEMAN;
Company   TEXAS INSTRUMENTS;
Assembly  None;
Location  DALLAS, TEXAS;
/*****************************************************************/
/*        ADDRESS DECODER FOR NUBUS SLAVE APPLICATION            */
/*        USING ACT2440 AND BCT2420 NUBUS CONTROLLERS            */
/*****************************************************************/
/* TARGET DEVICE TYPE: TIBPAD16N8-7                              */
/*****************************************************************/

/** Inputs **/

pin [1..9]    = [A10..A18] ; /* ADDRESS LINES 10 THRU 18*  /
pin [13..17] = [A19..A23] ; /* ADDRESS LINES 19 THRU 23*  /
pin 18      = IDEQ_ ;       /* SIGNAL FROM BCT2420 TO SIGNAL /
                            /* NUBUS CONTROLLER WHEN BEING  */
                            /* ACCESSED BY NUBUS            */
/** Outputs **/

pin 12      = MEM_ ;        /* ACTIVE LOW FOR DRAM ACCESS   */
pin 19      = ROM_ ;        /* ACTIVE LOW FOR ROM ACCESS    */

/** Logic Equations **/

MEM_ = !(!A23 & !A22 & !A21 & !A20 & !IDEQ_) ;/* RAM DECODES AT
                                                 HEX 0    */
                                              /* (A23...A20) */
ROM_ = !(A23 &  A22 &  A21 &  A20 &  A19 & !A18
      & !A17 & !A16 & !A15 & !A14 & !A13 & !A12
      & !A11 & !A10 & !IDEQ_) ;/* ROM DECODES AT HEX 3E00 */
                               /* (A23...A10)             */
```

```
Partno   TIBPAD16N8-7;
Name     DECODE;
Date     10/06/88;
Revision 01;
Designer KYLE NEMAN;
Company  TEXAS INSTRUMENTS;
Assembly None;
Location DALLAS, TEXAS;
/*****************************************************************/
/*              DYNAMIC TIMING DECODER                           */
/*                 SIMULATION FILE                               */
/*           FOR NUBUS SLAVE APPLICATION                         */
/*****************************************************************/
/* Allowable Target Device Types: TIBPAD16N8-7                   */
/*****************************************************************/
ORDER:
A23,%3,A22,%3,A21,%3,A20,%3,A19,%3,A18,%3,A17,%3,A16,%3,A15,
%3,A14,%3,A13,%3,A12,%3,A11,%3,A10,%3,IDEQ_,%6,MEM_,%4,ROM_;
VECTORS:
$msg"------------INPUT----------------------------------------OUTP
UT-";
A23 A22 A21 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 IDEQ_ MEM_
ROM_";
-----------------------------------------------------------------
---";
/*MEM*/
0   0   0   0   0   0   0   0   0   0   0   0   0   0    0    L
H
/*ROM*/
1   1   1   1   1   0   0   0   0   0   0   0   0   0    0    H
L
0   0   0   0   0   0   0   0   0   0   0   0   0   0    1    H
H
1   1   1   1   1   0   0   0   0   0   0   0   0   0    1    H
H
0   0   0   1   0   0   0   0   0   0   0   0   0   0    0    H
H
1   1   0   1   1   0   0   0   0   0   0   0   0   0    0    H
H
```

Appendix B

```
*****************************************************************
                          NUBUS167
*****************************************************************
CUPL            2.50a Serial# MD-250-3238
Device          f167  Library DLIB-h-24-23
Created         Mon Nov 13 15:08:46 1989
Name            NUBUS167
Partno          82S167
Revision        01
Date            10/06/88
Designer        KYLE NEWMAN
Company         TEXAS INSTRUMENTS
Assembly        None
Location        DALLAS, TEXAS
```

```
Partno   82S167;
Name     NUBUS167;
Date     10/06/88;
Revision 01;
Designer KYLE NEWMAN;
Company  TEXAS INSTRUMENTS;
Assembly None;
Location DALLAS, TEXAS;
/*****************************************************************/
/*                  DYNAMIC MEMORY CONTROLLER                    */
/*                       USING ACT4503                           */
/*                  FOR NUBUS SLAVE APPLICATION                  */
/*****************************************************************/
/* Allowable Target Device Types: TIB82S167B                     */
/*****************************************************************/
/**  Inputs  **/
pin  1 =  NCLK_;
pin  2 =  RDY;
pin 19 =  SEREQ_;
pin 20 =  NLRST_;
pin 21 =  NLTM1_;
pin 22 =  MEM_;
pin 23 =  ROM_;
/**  Outputs  **/
pin  9 =  W_;
pin 10 =  ALE;
pin 11 =  LOCTM0_;         /** local transfer mode control **/
pin 13 =  LACK_;           /** local acknowledge  **/
pin 14 =  SGNTA_;          /** slave grant access  **/
/** Internal Node Group  -   STATE bits declared as nodes      **/
node [P3,P2,P1,P0];
/**  Intermediate Variable Definitions          **/
Field STATE  = [P3,P2,P1,P0];$define  ST0 'b'0000
$define  ST1 'b'0001
$define  ST2 'b'0010
$define  ST3 'b'0011
$define  ST4 'b'0100
$define  ST5 'b'0101
$define  ST6 'b'0110
$define  ST7 'b'0111
$define  ST8 'b'1000
$define  ST9 'b'1001
$define ST10 'b'1010/** Logic Equations **/Sequence STATE {
Present ST0  IF  NLRST_ & !SEREQ_ & !MEM_ & ROM_ &  !NLTM1_  NEXT
ST1
          OUT [!ALE];
IF  NLRST_ & !SEREQ_ & !MEM_ &  ROM_ &  NLTM1_  NEXT ST4
          OUT [!ALE,!W_];
IF  NLRST_ & !SEREQ_ &  MEM_ & !ROM_ & !NLTM1_  NEXT ST7
          OUT [!LACK_];
IF  NLRST_ & !SEREQ_ &  MEM_ &  ROM_
     # NLRST_ & !SEREQ_ & !ROM_  & NLTM1_  NEXT ST9
          OUT [!LOCTM0_,!LACK_];
IF !NLRST_           NEXT ST0;
DEFAULT NEXT ST0 OUT [!SGNTA_,!LOCTM0_,ALE,W_,LACK_];
/**  DRAM READ CYCLE        **/
Present ST1  IF !RDY & NLRST_ NEXT ST1 OUT [!ALE];
      IF !NLRST_  NEXT ST0;
      DEFAULT  NEXT ST2 OUT [!LACK_];
```

```
Present ST2  IF  !NLRST_ NEXT ST0;
     DEFAULT  NEXT ST3 OUT [LACK_,SGNTA_];
Present ST3  IF !NLRST_ NEXT ST0 ;
     DEFAULT NEXT ST0 OUT [!SGNTA_,!LOCTM0_,ALE,W_,LACK_];
/**  DRAM WRITE CYCLE      **/
Present ST4  IF  !RDY & NLRST_ NEXT ST4  OUT [!ALE,!W_];
     IF  !NLRST_ NEXT ST0;
     DEFAULT    NEXT ST5 OUT [!LACK_];
Present ST5  IF  !NLRST_ NEXT ST0;
     DEFAULT  NEXT ST6 OUT [LACK_,SGNTA_];
Present ST6  IF !NLRST_ NEXT ST0 ;
     DEFAULT NEXT ST0 OUT [!SGNTA_,!LOCTM0_,ALE,W_,LACK_];
/**  ROM READ CYCLE        **/
Present ST7  IF  !NLRST_ NEXT ST0;
     DEFAULT  NEXT ST8 OUT [SGNTA_,LACK_];
Present ST8  IF !NLRST_ NEXT ST0 ;
     DEFAULT NEXT ST0 OUT [!SGNTA_,!LOCTM0_,ALE,W_,LACK_];
/**  INVALID ACCESS CYCLE  **/
Present ST9  IF  !NLRST_ NEXT ST0;
     DEFAULT  NEXT ST10 OUT [SGNTA_,LACK_];
Present ST10 IF !NLRST_ NEXT ST0 ;
     DEFAULT NEXT ST0 OUT [!SGNTA_,!LOCTM0_,ALE,W_,LACK_];}
APPEND SGNTA_-R  = !NLRST_;
APPEND LOCTM0_-R = !NLRST_;
APPEND ALE.S     = !NLRST_;
APPEND W_.S      = !NLRST_;
APPEND LACK_.S   = !NLRST_;
APPEND P0.R      = !NLRST_;
APPEND P1.R      = !NLRST_;
APPEND P2.R      = !NLRST_;
APPEND P3.R       = !NLRST_;
```

```
Partno   82S167;
Name     NUBUS167;
Date     10/06/88;
Revision 01;
Designer KYLE NEWMAN;
Company  TEXAS INSTRUMENTS;
Assembly None;
Location DALLAS, TEXAS;
/*****************************************************************/
/*                DYNAMIC TIMING CONTROLLER                      */
/*                     SIMULATION FILE                           */
/*               FOR NUBUS SLAVE APPLICATION                     */
/*****************************************************************/
/* Allowable Target Device Types: TIB82S167B                     */
/*****************************************************************/
ORDER:
NCLK_,%3,RDY,%4,SEREQ_,%6,NLRST_,%6,NLTM1_,%5,MEM_,%3,ROM_,%4,
      W_,%3,ALE,%4,LOCTM0_,%7,LACK_,%5,SGNTA_,%6,STATE;
BASE: DECIMAL;VECTORS:
$msg" DRAM READ CYCLE";
$msg"     ";
$msg"-----------INPUT-----------------------------OUTPUT-------";
$msg"NCLK_ RDY SEREQ_ NLRST_ NLTM1_ MEM_ ROM_ W_ ALE LOCTM0_ LACK_
SGNTA_ STATE";
$msg"
-----------------------------------------------------------------";
/*RST*/ C   X    X      0      X     X    X    H   H    L     H   L
"0"
/*S0 */ C   X    0      1      0     0    1    *   L    *     *   *
"1"
/*S1 */ C   0    X      1      X     X    X    *   L    *     *   *
"1"
/*S1 */ C   1    X      1      X     X    X    *   *    *     L   *
"2"
/*S2 */ C   X    X      1      X     X    X    *   *    *     H   H
"3"
/*S3 */ C   X    X      1      X     X    X    H   H    L     H   L
"0"
/*S0 */ C   X    X      0      X     X    X    H   H    L     H   L
"0"

$msg" DRAM WRITE CYCLE";
$msg"     ";
$msg"-----------INPUT-----------------------------OUTPUT-------";
$msg"NCLK_ RDY SEREQ_ NLRST_ NLTM1_ MEM_ ROM_ W_ ALE LOCTM0_ LACK_
SGNTA_ STATE";
$msg"
-----------------------------------------------------------------";
/*S0 */ C   X    0    1      1     0    1    *   L    L     *     *
"4"
/*S4 */ C   0    X    1      X     X    X    *   L    L     *     *
"4"
/*S4 */ C   1    X    1      X     X    X    *   *    *     *     L
"5"
/*S5 */ C   X    X    1      X     X    X    *   *    *     H     H
"6"
/*S6 */ C   X    X    1      X     X    X    H   H    L     H     L
"0"
/*S0 */ C   X    X    0      X     X    X    H   H    L     H     L
```

```
"0"
$msg" ROM READ CYCLE";
$msg"      ";
$msg"------------INPUT-----------------------------OUTPUT-------";
$msg"NCLK_ RDY SEREQ_ NLRST_ NLTM1_ MEM_ ROM_ W_ ALE LOCTM0_ LACK_
SGNTA_ STATE";
$msg"
-------------------------------------------------------------------";
/*RST*/ C   X    X   0      X    X    X   H   H   L     H     L
 "0"
/*S0 */ C   X    0   1      0    1    0   *   *   *     L     *
 "7"
/*S7 */ C   X    X   1      X    X    X   *   *   *     H     H
 "8"
/*S8 */ C   X    X   1      X    X    X   H   H   L     H     L
 "0"
/*S0 */ C   X    X   0      X    X    X   H   H   L     H     L
 "0"
$msg" INVALID ACCESS CYCLE";
$msg"      ";
$msg"------------INPUT-----------------------------OUTPUT-------";
$msg"NCLK_ RDY SEREQ_ NLRST_ NLTM1_ MEM_ ROM_ W_ ALE LOCTM0_ LACK_
SGNTA_ STATE";
$msg"
-------------------------------------------------------------------";
/*RST*/ C   X    X   0      X    X    X   H   H   L     H     L
"0"
/*S0 */ C   X    0   1      X    1    1   *   *   L     L     *
"9"
/*S9 */ C   X    X   1      X    X    X   *   *   *     H     H
"10"
/*S10*/ C   X    X   1      X    X    X   H   H   L     H     L
"0"
/*S0 */ C   X    0   1      1    X    0   *   *   L     L     *
"9"
/*S9 */ C   X    X   1      X    X    X   *   *   *     H     H
"10"
/*S10*/ C   X    X   1      X    X    X   H   H   L     H     L
"0"
```

The SN74BCT2423 and SN74BCT2424 in Memory Interleave/Interface Applications

Bertrand Leigh

TEXAS
INSTRUMENTS

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Memory Interleave Applications

Memory interleaving is an organizing technique for Dynamic RAMs that results in significantly reduced memory access cycle times. When even-address words of memory are located in one bank of DRAM and odd-address words of memory are located in the other bank, sequential accesses from the memory will be requested from alternating banks. This organization scheme takes advantage of the fact that when memory banks are accessed alternatively, the access cycles can be overlapped to avoid the DRAM's $\overline{RAS}$ precharge time.

A typical access cycle timing of a 100-ns DRAM is shown in Figure 1. For this type of access cycle without memory interleave, the subsequent access cycle to the DRAM cannot begin until the $\overline{RAS}$ precharge time of 80 ns has expired. Based on this timing diagram, every access cycle takes 180 ns.

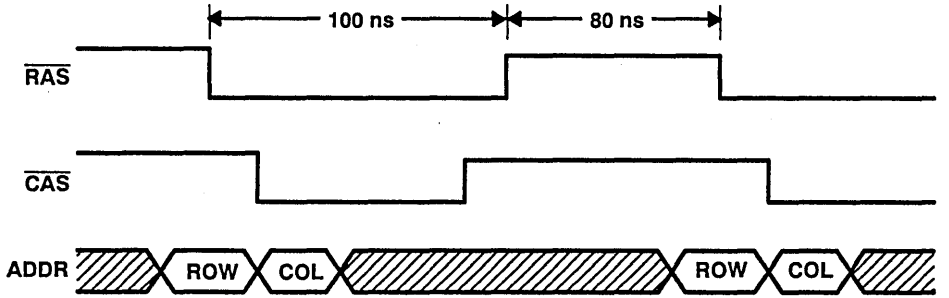


Figure 1. Typical DRAM Access Cycle Timing

In an interleaved memory organization, BANK0 of the DRAM is accessed by $\overline{RAS0}$ and $\overline{CAS0}$ signals and BANK1 is accessed by $\overline{RAS1}$ and $\overline{CAS1}$ signals as shown in Figure 2. When the DRAM banks are accessed alternatively, the access cycle to the next bank need not wait for the previous bank's $\overline{RAS}$ precharge time. Based on this timing, each access cycle takes 100 ns. The reduction in memory access time for this ideal case is:

$$\%\ time\ improvement\ \text{for}\ interleaving = \frac{180\ ns - 100\ ns}{180\ ns} = 44\%$$

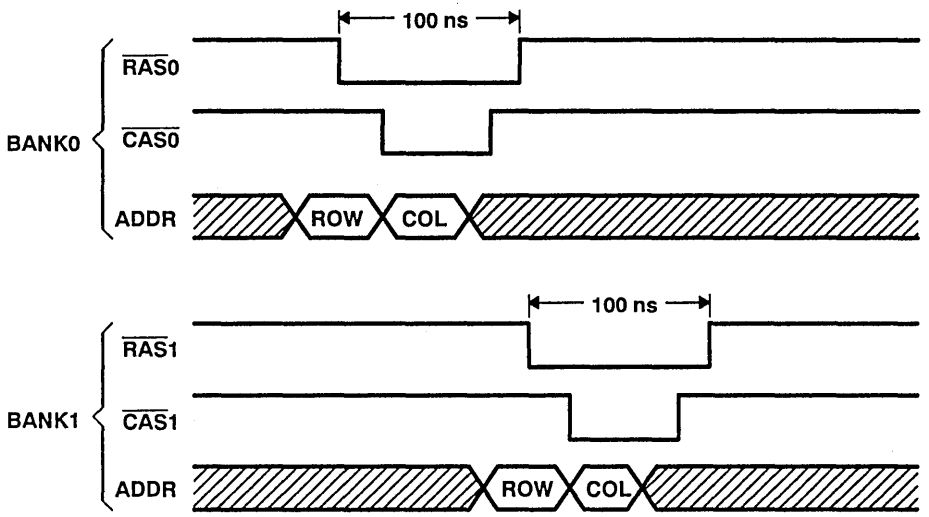


Figure 2. Two-Way DRAM Access Cycle Timing

Realistically, these two types of access cycles will be interspersed because of the sequential nature of the instruction fetches and random nature of the operand (data) accesses. A typical breakdown between these two types of access cycle is 50%. Under this assumption, the following calculations can be made:

$$\textit{Access cycles without interleave} = 180\ ns$$

$$\textit{Interspersed access cycles} = (180\ ns \times 50\%) + (100\ ns \times 50\%) = 140\ ns$$

$$\%\ \textit{time improvement for interleaving} = \frac{180\ ns - 140\ ns}{180\ ns} = 22\%$$

Figure 3 shows how the 'BCT2423/24 can be used to implement a memory interleave organization. Since the access cycles of the memory are overlapped, the need for latches arises. The 'BCT2423/24's input latches are available to meet this need. The multiplexed operation of the 'BCT2423/24 makes the device ideal for any memory interleave application where 2n banks of memory data must be multiplexed onto one bus. In addition to the multiplexing feature, 'BCT2423/24's large output drive capability eliminates the need for bus drivers to interface to the processor bus. The BiCMOS process used on 'BCT2423/24 greatly reduces the standby power of the device, which is an attractive feature when power consumption and noise problems are major concerns for the memory design.

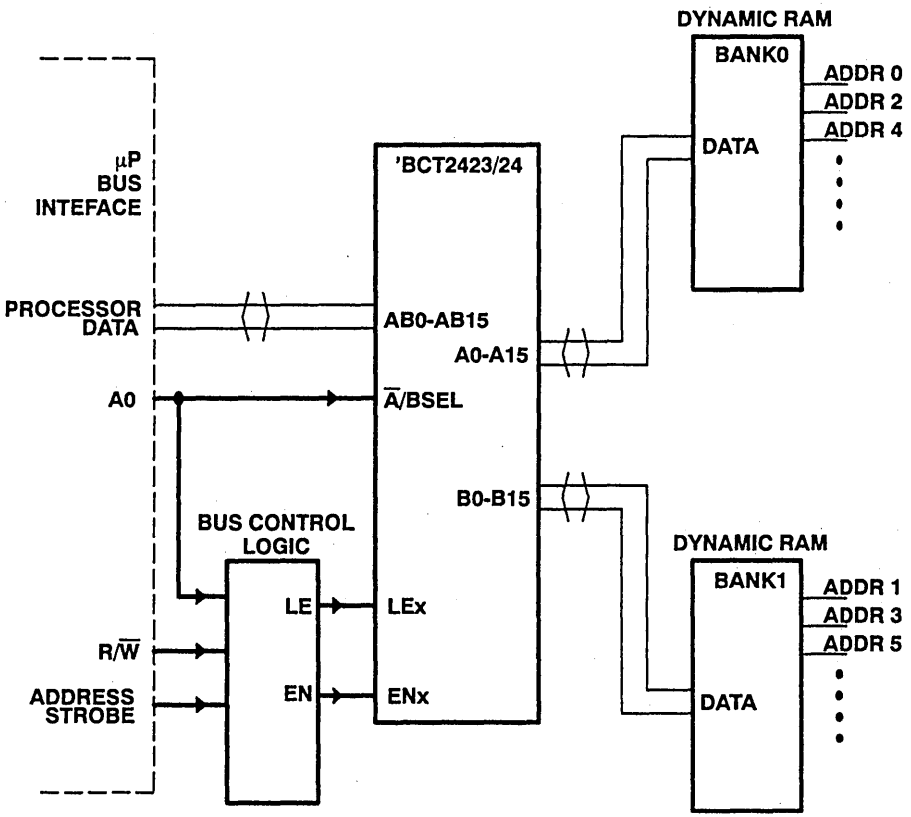
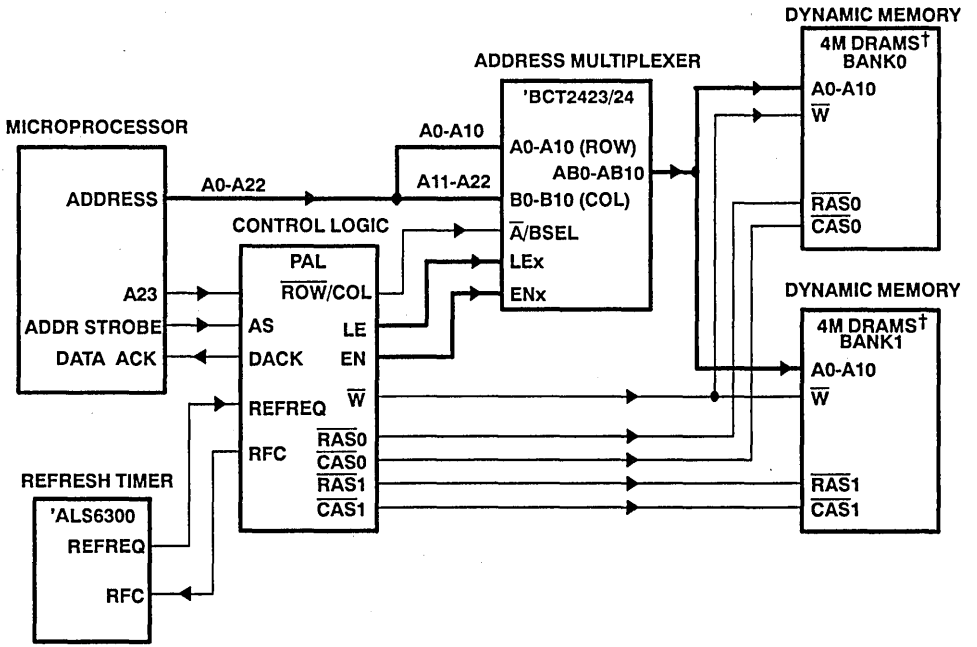


Figure 3. Memory Interleave System Interface

Memory Interface Applications

In addition to memory interleave application, the 'BCT2423's and 'BCT2424's multiplexing function can also be used to multiplex the memory address into row and column address of the DRAM. As the DRAM sizes get larger, more address signals are needed to access the memory. Figure 4 shows how the 'BCT2423 or 'BCT2424 is used in a typical address multiplexing of the 4M DRAMs in a discrete logic implementation of the DRAM control logic. To generate the refresh address that is normally provided by the counter internal to the multiplexer, one can make use of the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh feature of the DRAM, where refresh addresses are generated by the DRAM.



† Use the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh feature of the DRAM to take advantage of the DRAM's internal refresh counter.

Figure 4. Use of SN74BCT2423 and SN74BCT2424 in DRAM Interface Applications

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Explanation of Logic Symbols

by F.A. Mann

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Explanation of Logic Symbols†

1 Introduction

The International Electrotechnical Commission (IEC) has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic circuit to each output without showing explicitly the internal logic. At the heart of the system is dependency notation, which will be explained in section 4.

The system was introduced in the USA in a rudimentary form in IEEE/ANSI Standard Y32.14-1973. Lacking at that time a complete development of dependency notation, it offered little more than a substitution of rectangular shapes for the familiar distinctive shapes for representing the basic functions of AND, OR, negation, etc. This is no longer the case.

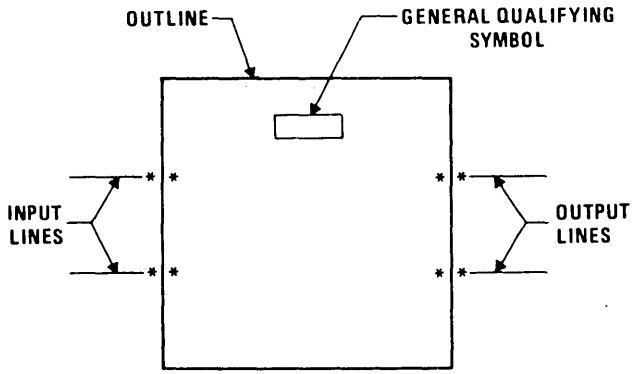
Internationally, IEC Technical Committee TC-3 has approved a new document (Publication 617-12) that consolidates the original work started in the mid 1960s and published in 1972 (Publication 117-15) and the amendments and supplements that have followed. Similarly for the USA, IEEE Committee SCC 11.9 has revised the publication IEEE Std 91/ANSI Y32.14. Now numbered simply IEEE Std 91-1984, the IEEE standard contains all of the IEC work that has been approved, and also a small amount of material still under international consideration. Texas Instruments is participating in the work of both organizations, and this document introduces new logic symbols in accordance with the new standards. When changes are made as the standards develop, future editions will take those changes into account.

The following explanation of the new symbolic language is necessarily brief and greatly condensed from what the standards publications now contain. This is not intended to be sufficient for those people who will be developing symbols for new devices. It is primarily intended to make possible the understanding of the symbols used in various data books and the comparison of the symbols with logic diagrams, functional block diagrams, and/or function tables to further help that understanding.

2 Symbol Composition

A symbol comprises an outline or a combination of outlines together with one or more qualifying symbols. The shape of the symbol is not significant. As shown in Figure 1, general qualifying symbols are used to tell exactly what logical operation is performed by the elements. Table 1 shows general qualifying symbols defined in the new standards. Input lines are placed on the left, and output lines are placed on the right. When an exception is made to that convention, the direction of signal flow is indicated by an arrow as shown in Figure 11.

† Written by F. A. Mann.



*Possible positions for qualifying symbols relating to inputs and outputs

Figure 1. Symbol Composition

All outputs of a single, unsubdivided element always have identical internal logic states determined by the function of the element except when otherwise indicated by an associated qualifying symbol or label inside the element.

The outlines of elements may be abutted or embedded in which case the following conventions apply. There is no logic connection between the elements when the line common to their outlines is in the direction of signal flow. There is at least one logic connection between the elements when the line common to their outlines is perpendicular to the direction of signal flow. The number of logic connections between elements will be clarified by the use of qualifying symbols, and this is discussed further under that topic. If no indications are shown on either side of the common line, it is assumed there is only one connection.

When a circuit has one or more inputs that are common to more than one element of the circuit, the common-control block may be used. This is the only distinctively shaped outline used in the IEC system. Figure 2 shows that, unless otherwise qualified by dependency notation, an input to the common-control block is an input to each of the elements below the common-control block.

A common output depending on all elements of the array can be shown as the output of a common-output element. Its distinctive visual feature is the double line at its top. In addition, the common-output element may have other inputs as shown in Figure 3. The function of the common-output element must be shown by use of a general qualifying symbol.

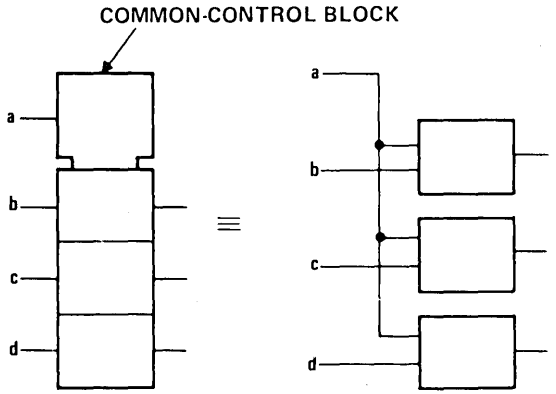


Figure 2. Common-Control Block

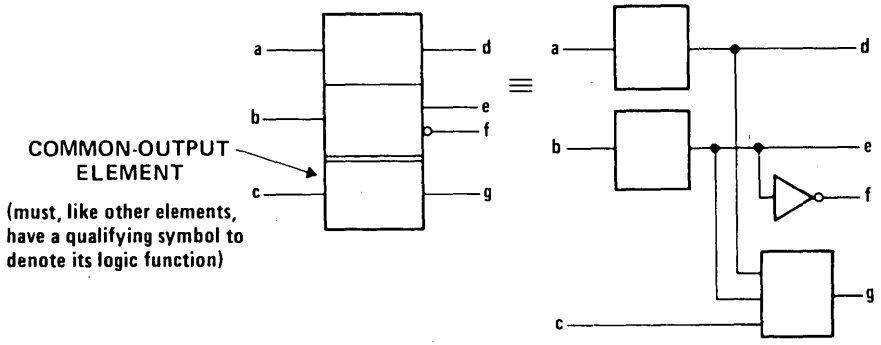


Figure 3. Common-Output Element

3 Qualifying Symbols

3.1 General Qualifying Symbols

Table 1 shows general qualifying symbols defined by IEEE Standard 91. These characters are placed near the top center or the geometric center of a symbol or symbol element to define the basic function of the device represented by the symbol or of the element.

Table 1. General Qualifying Symbols

SYMBOL	DESCRIPTION	CMOS EXAMPLE	TTL EXAMPLE
&	AND gate or function.	'HC00	SN7400
≥1	OR gate or function. The symbol was chosen to indicate that at least one active input is needed to activate the output.	'HC02	SN7402
=1	Exclusive OR. One and only one input must be active to activate the output.	'HC86	SN7486
=	Logic identity. All inputs must stand at the same state.	'HC86	SN74180
2k	An even number of inputs must be active.	'HC280	SN74180
2k + 1	An odd number of inputs must be active.	'HC86	SN74ALS86
1	The one input must be active.	'HC04	SN7404
▷ or ◁	A buffer or element with more than usual output capability (symbol is oriented in the direction of signal flow).	'HC240	SN74S436
⊓	Schmitt trigger; element with hysteresis.	'HC132	SN74LS18
X/Y	Coder, code converter (DEC/BCD, BIN/OCT, BIN/7-SEG, etc.).	'HC42	SN74LS347
MUX	Multiplexer/data selector.	'HC151	SN74150
DMUX or DX	Demultiplexer.	'HC138	SN74138
Σ	Adder.	'HC283	SN74LS385
P−Q	Subtracter.	†	SN74LS385
CPG	Look-ahead carry generator.	'HC182	SN74182
π	Multiplier.	†	SN74LS384
COMP	Magnitude comparator.	'HC85	SN74LS682
ALU	Arithmetic logic unit.	'HC181	SN74LS381
⊓	Retriggerable monostable.	'HC123	SN74LS422
1⊓	Nonretriggerable monostable (one-shot).	'HC221	SN74121
G ⊓⊓	Astable element. Showing waveform is optional.	†	SN74LS320
!G ⊓⊓	Synchronously starting astable.	†	SN74LS624
G! ⊓⊓	Astable element that stops with a completed pulse.	†	†
SRGm	Shift register. m = number of bits.	'HC164	SN74LS595
CTRm	Counter. m = number of bits; cycle length = 2^m.	'HC590	SN54LS590
CTR DIVm	Counter with cycle length = m.	'HC160	SN74LS668
RCTRm	Asynchronous (ripple-carry) counter; cycle length = 2^m.	'HC4020	†

† Not all of the general qualifying symbols have been used in TI's CMOS and TTL data books, but they are included here for the sake of completeness.

Table 1. General Qualifying Symbols (Continued)

SYMBOL	DESCRIPTION	CMOS EXAMPLE	TTL EXAMPLE
ROM	Read-only memory.	†	SN74187
RAM	Random-access read/write memory.	'HC189	SN74170
FIFO	First-in, first-out memory.	†	SN74LS222
I=0	Element powers up cleared to 0 state.	†	SN74AS877
I=1	Element powers up set to 1 state.	'HC7022	SN74AS877
Φ	Highly complex function; "gray box" symbol with limited detail shown under special rules.	'ACT2140	SN74LS608

†Not all of the general qualifying symbols have been used in TI's CMOS and TTL data books, but they are included here for the sake of completeness.

3.2 General Qualifying Symbols for Inputs and Outputs

Qualifying symbols for inputs and outputs are shown in Table 2, and many will be familiar to most users, a likely exception being the logic polarity symbol for directly indicating active-low inputs and outputs. The older logic negation indicator means that the external 0 state produces the internal 1 state. The internal 1 state means the active state. Logic negation may be used in pure logic diagrams; in order to tie the external 1 and 0 logic states to the levels H (high) and L (low), a statement of whether positive logic (1 = H, 0 = L) or negative logic (1 = L, 0 = H) is being used is required or must be assumed. Logic polarity indicators eliminate the need for calling out the logic convention and are used in various data books in the symbology for actual devices. The presence of the triangular polarity indicator indicates that the L logic level will produce the internal 1 state (the active state) or that, in the case of an output, the internal 1 state will produce the external L level. Note how the active direction of transition for a dynamic input is indicated in positive logic, negative logic, and with polarity indication.

The internal connections between logic elements abutted together in a symbol may be indicated by the symbols shown in Table 2. Each logic connection may be shown by the presence of qualifying symbols at one or both sides of the common line, and, if confusion can arise about the number of connections, use can be made of one of the internal connection symbols.

The internal (virtual) input is an input originating somewhere else in the circuit and is not connected directly to a terminal. The internal (virtual) output is likewise not connected directly to a terminal. The application of internal inputs and outputs requires an understanding of dependency notation, which is explained in section 4.

Table 2. Qualifying Symbols for Inputs and Outputs

Logic negation at input. External 0 produces internal 1.

Logic negation at output. Internal 1 produces external 0.

Active-low input. Equivalent to  in positive logic.

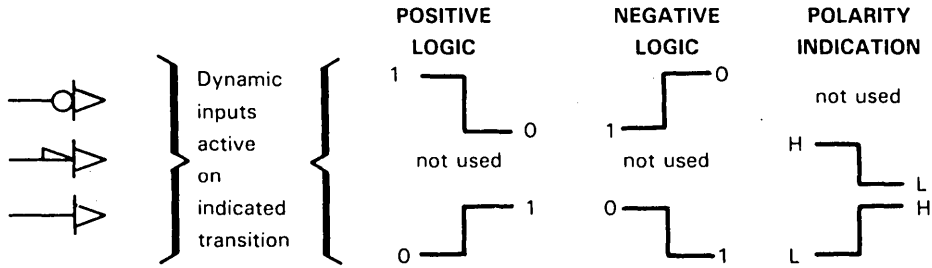
Active-low output. Equivalent to  in positive logic.

Active-low input in the case of right-to-left signal flow.

Active-low output in the case of right-to-left signal flow.

Signal flow from right to left. If not otherwise indicated, signal flow is from left to right.

Bidirectional signal flow.



Nonlogic connection. A label inside the symbol will usually define the nature of this pin.

Input for analog signals (on a digital symbol) (see Figure 3-14).

Input for digital signals (on an analog symbol) (see Figure 3-14).

Internal connection. 1 state on left produces 1 state on right.

Negated internal connection. 1 state on left produces 0 state on right.

Dynamic internal connection. Transition from 0 to 1 on left produces transitory 1 state on right.

Internal input (virtual input). It always stands at its internal 1 state unless affected by an overriding dependency relationship.

Internal output (virtual output). Its effect on an internal input to which it is connected is indicated by dependency notation.

In an array of elements, if the same general qualifying symbol and the same qualifying symbols associated with inputs and outputs would appear inside each of the elements of the array, then these qualifying symbols are usually shown only in the first element. This is done to reduce clutter and to save time in recognition. Similarly, large identical elements that are subdivided into smaller elements may each be represented by an unsubdivided outline. The SN54HC242 or SN54LS440 symbol illustrates this principle.

3.3 Symbols Inside the Outline

Table 3 shows some symbols used inside the outline. Note particularly that open-collector (open-drain), open-emitter (open-source), and 3-state outputs have distinctive symbols. An EN input affects all the external outputs of the element in which it is placed, plus the external outputs of any elements shown to be influenced by that element. It has no effect on inputs. When an enable input affects only certain outputs, affects outputs located outside the indicated influence of the element in which the enable input is placed, and/or affects one or more inputs, a form of dependency notation will indicate this (see 4.10). The effects of the EN input on the various types of outputs are shown.

It is particularly important to note that a D input is always the data input of a storage element. At its internal 1 state, the D input sets the storage element to its 1 state, and at its internal 0 state, it resets the storage element to its 0 state.

The binary grouping symbol will be explained more fully in section 8. Binary-weighted inputs are arranged in order, and the binary weights of the least significant and the most significant lines are indicated by numbers. In this document, weights of input and output lines will usually be represented by powers of two only when the binary grouping symbol is used; otherwise, decimal numbers will be used. The grouped inputs generate an internal number on which a mathematical function can be performed or that can be an identifying number for dependency notation (Figure 31). A frequent use is in addresses for memories.

Reversed in direction, the binary grouping symbol can be used with outputs. The concept is analogous to that for the inputs, and the weighted outputs will indicate the internal number assumed to be developed within the circuit.

Other symbols are used inside the outlines in accordance with the IEC/IEEE standards but are not shown here. Generally, these are associated with arithmetic operations and are self-explanatory.

When nonstandardized information is shown inside an outline, it is usually enclosed in square brackets [like these]. The square brackets are omitted when associated with a nonlogic input, which is indicated by an X superimposed on the connection line outside the symbol.

Table 3. Symbols Inside the Outline

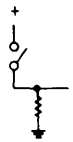
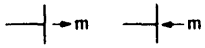
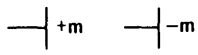
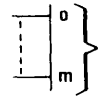
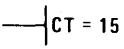
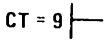
	Postponed output (of a pulse-triggered flip-flop). The output changes when input initiating change (e.g., a C input) returns to its initial external state or level. See paragraph 5.
	Bi-threshold input (input with hysteresis)
	N-P-N open-collector or similar output that can supply a relatively low-impedance L level when not turned off. Requires external pull-up. Capable of positive-logic wired-AND connection. 
	Passive-pull-up output is similar to N-P-N open-collector output but is supplemented with a built-in passive pull-up.
	N-P-N open-emitter or similar output that can supply a relatively low-impedance H level when not turned off. Requires external pull-down. Capable of positive-logic wired-OR connection. 
	Passive-pull-down output is similar to N-P-N open-emitter output but is supplemented with a built-in passive pull-down.
	Three-state output
	Output with more than usual output capability (symbol is oriented in the direction of signal flow).
	Enable input When at its internal 1-state, all outputs are enabled. When at its internal 0-state, open-collector and open-emitter outputs are off, three-state outputs are in the high-impedance state, and all other outputs (i.e., totem-poles) are at the internal 0-state.
J, K, R, S	Usual meanings associated with flip-flops (e.g., R = reset to 0, S = reset to 1).
	Toggle input causes internal state of output to change to its complement.
	Data input to a storage element equivalent to: 
	Shift right (left) inputs, m = 1, 2, 3, etc. If m = 1, it is usually not shown.
	Counting up (down) inputs, m = 1, 2, 3, etc. If m = 1, it is usually not shown.
	Binary grouping. m is highest power of 2.

Table 3. Symbols Inside the Outline (Continued)

	The contents-setting input, when active, causes the content of a register to take on the indicated value.
	The content output is active if the content of the register is as indicated.
	Input line grouping . . . indicates two or more terminals used to implement a single logic input. e.g., The paired expander inputs of SN7450. 
	Fixed-state output always stands at its internal 1 state. For example, see SN74185.

4 Dependency Notation

4.1 General Explanation

Dependency notation is the powerful tool that sets the IEC symbols apart from previous systems and makes compact, meaningful symbols possible. It provides the means of denoting the relationship between inputs, outputs, or inputs and outputs without actually showing all the elements and interconnections involved. The information provided by dependency notation supplements that provided by the qualifying symbols for an element's function.

In the convention for the dependency notation, use will be made of the terms "affecting" and "affected." In cases where it is not evident which inputs must be considered as being the affecting or the affected ones (e.g., if they stand in an AND relationship), the choice may be made in any convenient way.

So far, eleven types of dependency have been defined, and all of these are used in various TI data books. X dependency is used mainly with CMOS circuits. They are listed below in the order in which they are presented and are summarized in Table 4 at the end of section 4.

Section	Dependency Type or Other Subject
4.2	G, AND
4.3	General Rules for Dependency Notation
4.4	V, OR
4.5	N, Negate (Exclusive-OR)
4.6	Z, Interconnection
4.7	X, Transmission
4.8	C, Control
4.9	S, Set and R, Reset
4.10	EN, Enable
4.11	M, Mode
4.12	A, Address

4.2 G (AND) Dependency

A common relationship between two signals is to have them ANDed together. This has traditionally been shown by explicitly drawing an AND gate with the signals connected to the inputs of the gate. The 1972 IEC publication and the 1973 IEEE/ANSI standard showed several ways to show this AND relationship using dependency notation. While ten other forms of dependency have since been defined, the ways to invoke AND dependency are now reduced to one.

In Figure 4 input **b** is ANDed with input **a**, and the complement of **b** is ANDed with **c**. The letter G has been chosen to indicate AND relationships and is placed at input **b**, inside the symbol. A number considered appropriate by the symbol designer (1 has been used here) is placed after the letter G and also at each affected input. Note the bar over the 1 at input **c**.

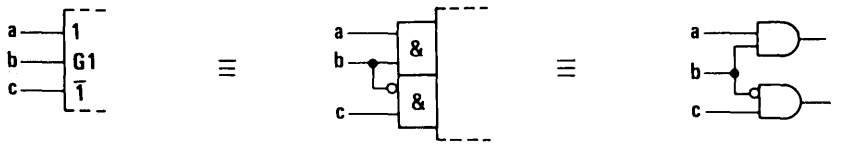


Figure 4. G Dependency Between Inputs

In Figure 5, output **b** affects input **a** with an AND relationship. The lower example shows that it is the internal logic state of **b**, unaffected by the negation sign, that is ANDed. Figure 6 shows input **a** to be ANDed with a dynamic input **b**.

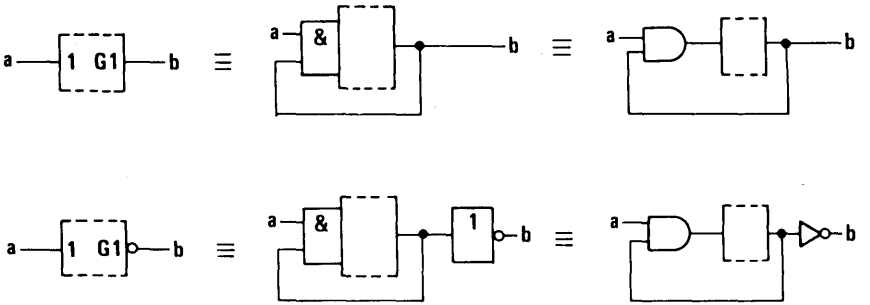


Figure 5. G Dependency Between Outputs and Inputs

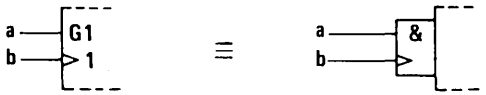


Figure 6. G Dependency with a Dynamic Input

The rules for G dependency can be summarized thus:

> When a G*m* input or output (*m* is a number) stands at its internal 1 state, all inputs and outputs affected by G*m* stand at their normally defined internal logic states. When the G*m* input or output stands at its 0 state, all inputs and outputs affected by G*m* stand at their internal 0 states.

4.3 Conventions for the Application of Dependency Notation in General

The rules for applying dependency relationships in general follow the same pattern as was illustrated for G dependency.

Application of dependency notation is accomplished by:

1) labeling the input (or output) *affecting* other inputs or outputs with the letter symbol indicating the relationship involved (e.g., G for AND) followed by an identifying number, appropriately chosen, and
2) labeling each input or output *affected* by that affecting input (or output) with that same number.

If it is the complement of the internal logic state of the affecting input or output that does the affecting, then a bar is placed over the identifying numbers at the affected inputs or outputs (Figure 4).

If two affecting inputs or outputs have the same letter and the same identifying number, they stand in an OR relationship to each other (Figure 7).

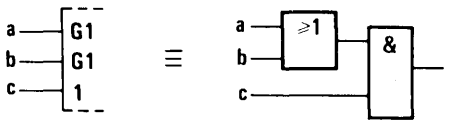


Figure 7. ORed Affecting Inputs

If the affected input or output requires a label to denote its function (e.g., "D"), this label will be *prefixed* by the identifying number of the affecting input (Figure 15).

If an input or output is affected by more than one affecting input, the identifying numbers of each of the affecting inputs will appear in the label

of the affected one, separated by commas. The normal reading order of these numbers is the same as the sequence of the affecting relationships (Figure 15).

If the labels denoting the functions of affected inputs or outputs must be numbers (e.g., outputs of a coder), the identifying numbers to be associated with both affecting inputs and affected inputs or outputs may be replaced by another character selected to avoid ambiguity, e.g., Greek letters (Figure 8).

Figure 8. Substitution for Numbers

4.4 V (OR) Dependency

The symbol denoting OR dependency is the letter V (Figure 9).

When a V*m* input or output stands at its internal 1 state, all inputs and outputs affected by V*m* stand at their internal 1 states. When the V*m* input or output stands at its internal 0 state, all inputs and outputs affected by V*m* stand at their normally defined internal logic states.

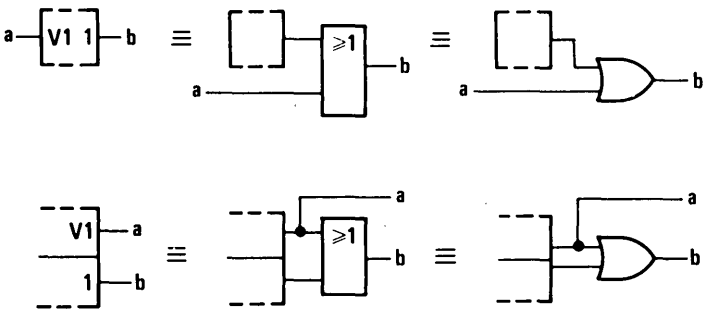
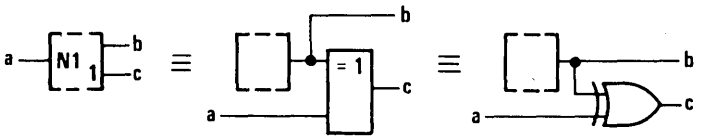


Figure 9. V (OR) Dependency

4.5 N (Negate) (Exclusive-OR) Dependency

The symbol denoting negate dependency is the letter N (Figure 10). Each input or output affected by an N*m* input or output stands in an Exclusive-OR relationship with the N*m* input or output.

When an N*m* input or output stands at its internal 1 state, the internal logic state of each input and each output affected by N*m* is the complement of what it would otherwise be. When an N*m* input or output stands at its internal 0 state, all inputs and outputs affected by N*m* stand at their normally defined internal logic states.



If a = 0, then c = b
If a = 1, then c = $\bar{b}$

Figure 10. N (Negate) (Exclusive-OR) Dependency

4.6 Z (Interconnection) Dependency

The symbol denoting interconnection dependency is the letter Z.

Interconnection dependency is used to indicate the existence of internal logic connections between inputs, outputs, internal inputs, and/or internal outputs.

The internal logic state of an input or output affected by a Z*m* input or output will be the same as the internal logic state of the Z*m* input or output, unless modified by additional dependency notation (Figure 11).

4.7 X (Transmission) Dependency

The symbol denoting transmission dependency is the letter X.

Transmission dependency is used to indicate controlled bidirectional connections between affected input/output ports (Figure 12).

When an X*m* input or output stands at its internal 1 state, all input-output ports affected by this X*m* input or output are bidirectionally connected together and stand at the same internal logic state or analog signal level. When an X*m* input or output stands at its internal 0 state, the connection associated with this set of dependency notation does not exist.

Although the transmission paths represented by X dependency are inherently bidirectional, use is not always made of this property. This is analogous to a piece of wire, which may be constrained to carry current in only one direction. If this is the case in a particular application, then the directional arrows shown in Figures 12, 13, and 14 are omitted.

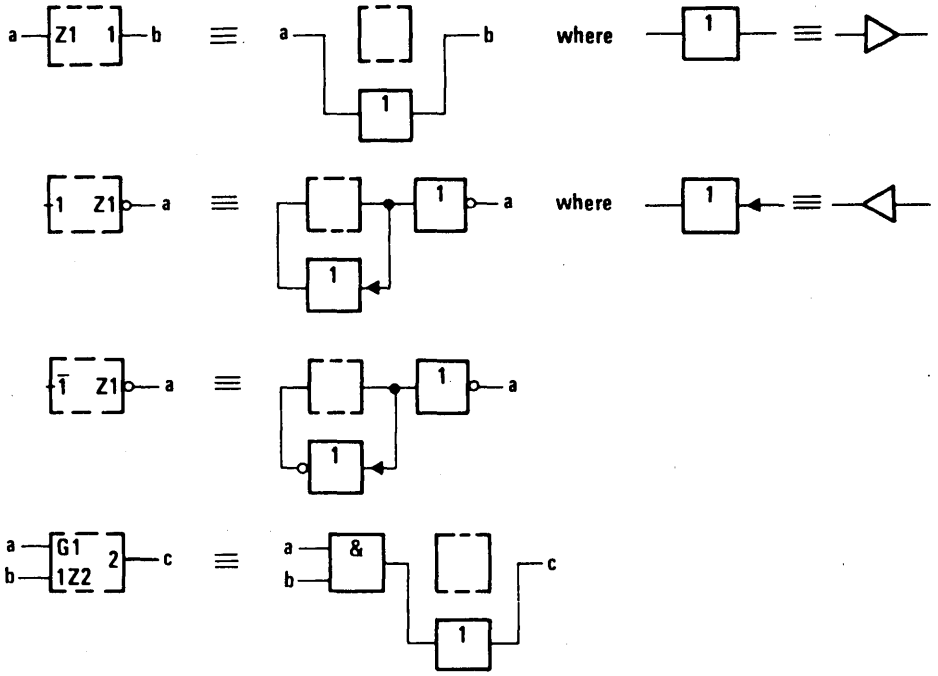
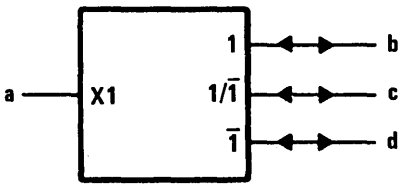


Figure 11. Z (Interconnection) Dependency



If a = 1, there is a bidirectional connection between b and c.

If a = 0, there is a bidirectional connection between c and d.

Figure 12. X (Transmission) Dependency

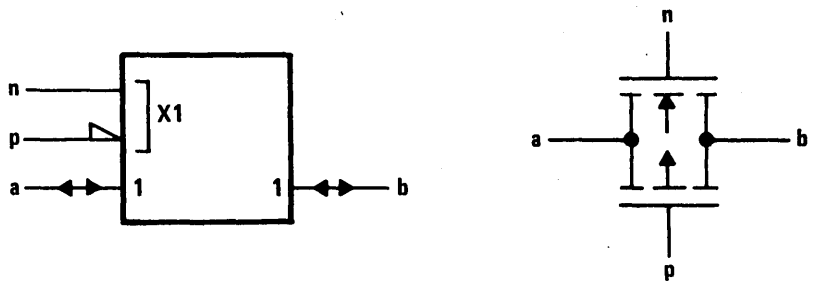


Figure 13. CMOS Transmission Gate Symbol and Schematic

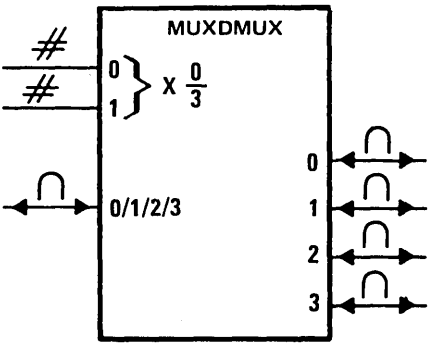


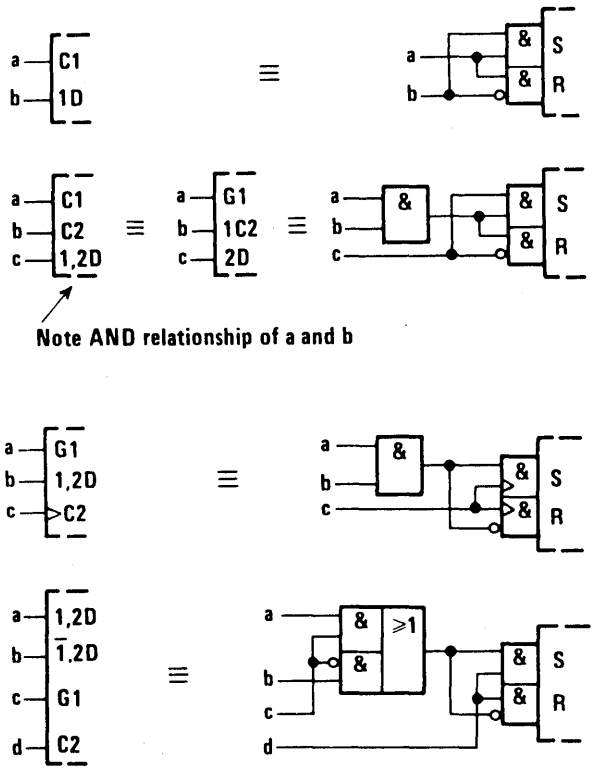
Figure 14. Analog Data Selector (Multiplexer/Demultiplexer)

4.8 C (Control) Dependency

The symbol denoting control dependency is the letter C.

Control inputs are usually used to enable or disable the data (D, J, K, R, or S) inputs of storage elements. They may take on their internal 1 states (be active) either statically or dynamically. In the latter case, the dynamic input symbol is used as shown in the third example of Figure 15.

When a C*m* input or output stands at its internal 1 state, the inputs affected by C*m* have their normally defined effect on the function of the element; i.e., these inputs are enabled. When a C*m* input or output stands at its internal 0 state, the inputs affected by C*m* are disabled and have no effect on the function of the element.



Input c selects which of a or b is stored when d goes low.

Figure 15. C (Control) Dependency

4.9 S (Set) and R (Reset) Dependencies

The symbol denoting set dependency is the letter S. The symbol denoting reset dependency is the letter R.

Set and reset dependencies are used if it is necessary to specify the effect of the combination R = S = 1 on a bistable element. Case 1 in Figure 16 does not use S or R dependency.

When an S*m* input is at its internal 1 state, outputs affected by the S*m* input will react, regardless of the state of an R input, as they normally would react to the combination S = 1, R = 0. See cases 2, 4, and 5 in Figure 16.

When an R*m* input is at its internal 1 state, outputs affected by the R*m* input will react, regardless of the state of an S input, as they normally would react to the combination S = 0, R = 1. See cases 3, 4, and 5 in Figure 16.

When an S*m* or R*m* input is at its internal 0 state, it has no effect.

Note that the noncomplementary output patterns in cases 4 and 5 are only pseudo stable. The simultaneous return of the inputs to S = R = 0 produces an unforeseeable stable and complementary output pattern.

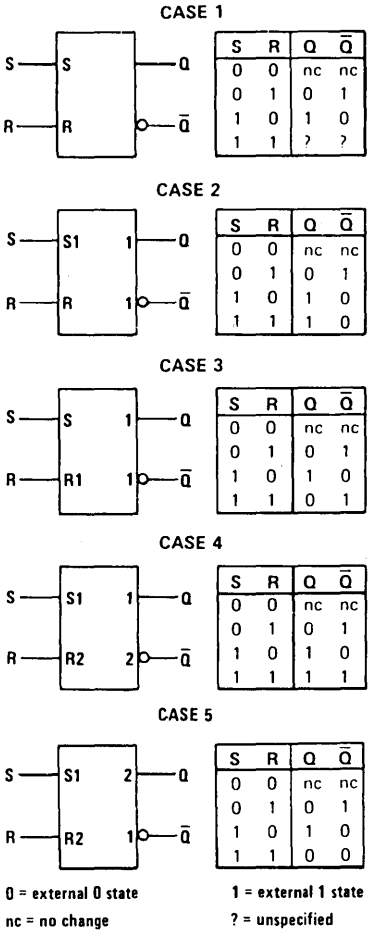
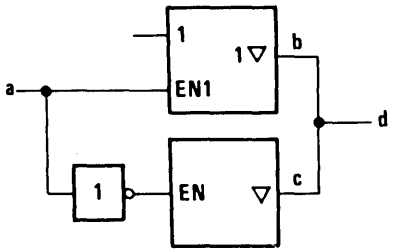


Figure 16. S (Set) and R (Reset) Dependencies

4.10 EN (Enable) Dependency

The symbol denoting enable dependency is the combination of letters EN.

An EN*m* input has the same effect on outputs as an EN input, see 3.3, but it affects only those outputs labeled with the identifying number *m*. It also affects those inputs labeled with the identifying number *m*. By contrast, an EN input affects all outputs and no inputs. The effect of an EN*m* input on an affected input is identical to that of a C*m* input (Figure 17).



If a = 0, b is disabled and d = c
If a = 1, c is disabled and d = b

Figure 17. EN (Enable) Dependency

When an EN*m* input stands at its internal 1 state, the inputs affected by EN*m* have their normally defined effect on the function of the element, and the outputs affected by this input stand at their normally defined internal logic states; i.e., these inputs and outputs are enabled.

When an EN*m* input stands at its internal 0 state, the inputs affected by EN*m* are disabled and have no effect on the function of the element, and the outputs affected by EN*m* are also disabled. Open-collector outputs are turned off, three-state outputs stand at their normally defined internal logic states but externally exhibit high impedance, and all other outputs (e.g., totem-pole outputs) stand at their internal 0 states.

4.11 M (MODE) Dependency

The symbol denoting mode dependency is the letter M.

Mode dependency is used to indicate that the effects of particular inputs and outputs of an element depend on the mode in which the element is operating.

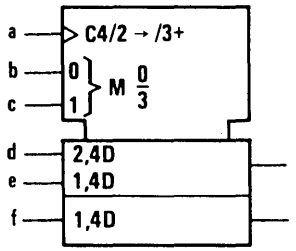
If an input or output has the same effect in different modes of operation, the identifying numbers of the relevant affecting M*m* inputs will appear in the label of that affected input or output between parentheses and separated by solidi (Figure 22).

4.11.1 M Dependency Affecting Inputs

M dependency affects inputs the same as C dependency. When an M*m* input or M*m* output stands at its internal 1 state, the inputs affected by this M*m* input or M*m* output have their normally defined effect on the function of the element; i.e., the inputs are enabled.

When an M*m* input or M*m* output stands at its internal 0 state, the inputs affected by this M*m* input or M*m* output have no effect on the function of the element. When an affected input has several sets of labels separated by solidi (e.g., C4/2→/3+), any set in which the identifying number of the M*m* input or M*m* output appears has no effect and is to be ignored. This represents disabling of some of the functions of a multifunction input.

The circuit in Figure 18 has two inputs, **b** and **c**, that control which one of four modes (0, 1, 2, or 3) will exist at any time. Inputs **d**, **e**, and **f** are D inputs subject to dynamic control (clocking) by the **a** input. The numbers 1 and 2 are in the series chosen to indicate the modes so inputs **e** and **f** are only enabled in mode 1 (for parallel loading), and input **d** is only enabled in mode 2 (for serial loading). Note that input **a** has three functions. It is the clock for entering data. In mode 2, it causes right shifting of data, which means a shift away from the control block. In mode 3, it causes the contents of the register to be incremented by one count.



Note that all operations are synchronous.

In MODE 0 (b = 0, c = 0), the outputs remain at their existing states as none of the inputs has an effect.

In MODE 1 (b = 1, c = 0), parallel loading takes place thru inputs e and f.

In MODE 2 (b = 0, c = 1), shifting down and serial loading thru input d take place.

In MODE 3 (b = c = 1), counting up by increment of 1 per clock pulse takes place.

Figure 18. M (Mode) Dependency Affecting Inputs

4.11.2 M Dependency Affecting Outputs

When an M*m* input or M*m* output stands at its internal 1 state, the affected outputs stand at their normally defined internal logic states; i.e., the outputs are enabled.

When an M*m* input or M*m* output stands at its internal 0 state, at each affected output any set of labels containing the identifying number of that M*m* input or M*m* output has no effect and is to be ignored. When an output has several different sets of labels separated by solidi (e.g., 2,4/3,5), only those sets in which the identifying number of this M*m* input or M*m* output appears are to be ignored.

Figure 19 shows a symbol for a device whose output can behave as either a 3-state output or an open-collector output depending on the signal applied to input **a**. Mode 1 exists when input **a** stands at its internal 1 state, and, in that case, the three-state symbol applies, and the open-element symbol has no effect. When **a** = 0, mode 1 does not exist so the three-state symbol has no effect, and the open-element symbol applies.

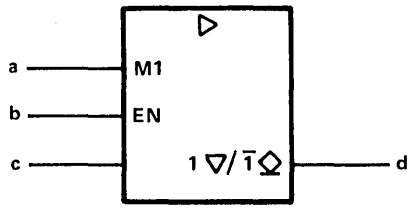


Figure 19. Type of Output Determined by Mode

In Figure 20, if input **a** stands at its internal 1 state establishing mode 1, output **b** will stand at its internal 1 state only when the content of the register equals 9. Since output **b** is located in the common-control block with no defined function outside of mode 1, the state of this output outside of mode 1 is not defined by the symbol.

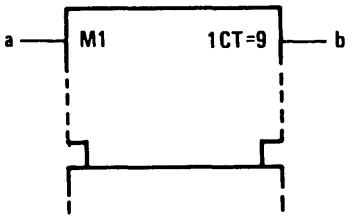


Figure 20. An Output of the Common-Control Block

In Figure 21, if input **a** stands at its internal 1 state establishing mode 1, output **b** will stand at its internal 1 state only when the content of the register equals 15. If input **a** stands at its internal 0 state, output **b** will stand at its internal 1 state only when the content of the register equals 0.

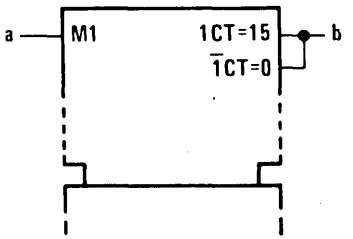


Figure 21. Determining an Output's Function

In Figure 22, inputs **a** and **b** are binary weighted to generate the numbers 0, 1, 2, or 3. This determines which one of the four modes exists.

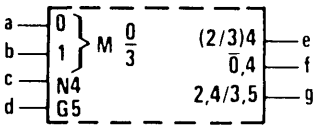


Figure 22. Dependent Relationships Affected by Mode

At output **e**, the label set causing negation (if **c** = 1) is effective only in modes 2 and 3. In modes 0 and 1, this output stands at its normally defined state as if it had no labels. At output **f**, the label set has effect when the mode is not 0 so output **e** is negated (if **c** = 1) in modes 1, 2, and 3. In mode 0, the label set has no effect so the output stands at its normally defined state. In this example, $\overline{0}$,4 is equivalent to (1/2/3)4. At output **g**, there are two label sets: the first set, causing negation (if **c** = 1), is effective only in mode 2; the second set, subjecting **g** to AND dependency on **d**, has effect only in mode 3.

Note that in mode 0 none of the dependency relationships has any effect on the outputs, so **e**, **f**, and **g** will all stand at the same state.

4.12 A (Address) Dependency

The symbol denoting address dependency is the letter A.

Address dependency provides a clear representation of those elements, particularly memories, that use address control inputs to select specified sections of a multidimensional array. Such a section of a memory array is usually called a word. The purpose of address dependency is to allow a symbolic presentation of the entire array. An input of the array shown at a particular element of this general section is common to the corresponding elements of all selected sections of the array. An output of the array shown at a particular element of this general section is the result of the OR function of the outputs of the corresponding elements of selected sections.

Inputs that are not affected by any affecting address input have their normally defined effect on all sections of the array, whereas inputs affected by an address input have their normally defined effect only on the section selected by that address input.

An affecting address input is labeled with the letter A followed by an identifying number that corresponds with the address of the particular section of the array selected by this input. Within the general section presented by the symbol, inputs and outputs affected by an A*m* input are labeled with the letter A, which stands for the identifying numbers, i.e., the addresses, of the particular sections.

Figure 23 shows a 3-word by 2-bit memory having a separate address line for each word and uses EN dependency to explain the operation. To select word 1, input **a** is taken to its 1 state, which establishes mode 1. Data can now be clocked into the inputs marked "1,4D." Unless words 2 and 3 are also selected, data cannot be clocked in at the inputs marked "2,4D" and "3,4D." The outputs will be the OR functions of the selected outputs; i.e., only those enabled by the active EN functions.

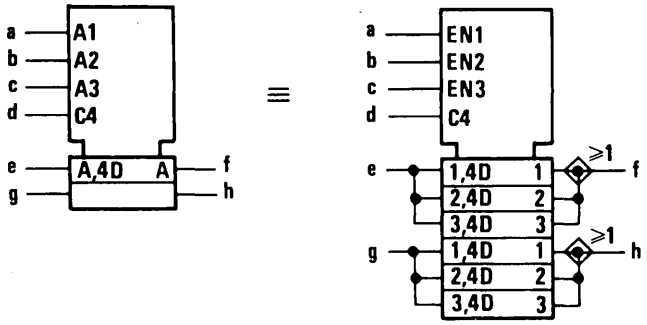


Figure 23. A (Address) Dependency

The identifying numbers of affecting address inputs correspond with the addresses of the sections selected by these inputs. They need not necessarily differ from those of other affecting dependency inputs (e.g., G, V, N, . . .), because, in the general section presented by the symbol, they are replaced by the letter A.

If there are several sets of affecting A*m* inputs for the purpose of independent and possibly simultaneous access to sections of the array, then the letter A is modified to 1A, 2A, ... Since they have access to the same sections of the array, these sets of A inputs may have the same identifying numbers. The symbols for 'HC170 or SN74LS170 make use of this.

Figure 24 is another illustration of the concept.

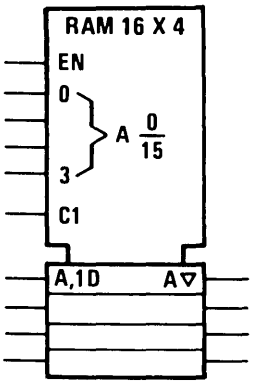


Figure 24. Array of 16 Sections of Four Transparent Latches with State Outputs Comprising a 16-Word × 4-Bit Random-Access Memory

Table 4. Summary of Dependency Notation

TYPE OF DEPENDENCY	LETTER SYMBOL*	AFFECTING INPUT AT ITS 1-STATE	AFFECTING INPUT AT ITS 0-STATE
Address	A	Permits action (address selected)	Prevents action (address not selected)
Control	C	Permits action	Prevents action
Enable	EN	Permits action	Prevents action of inputs ◇outputs off ▽outputs at external high impedance, no change in internal logic state Other outputs at internal 0 state
AND	G	Permits action	Imposes 0 state
Mode	M	Permits action (mode selected)	Prevents action (mode not selected)
Negate (Ex-OR)	N	Complements state	No effect
Reset	R	Affected output reacts as it would to S = 0, R = 1	No effect
Set	S	Affected output reacts as it would to S = 1, R = 0	No effect
OR	V	Imposes 1 state	Permits action
Transmission	X	Bidirectional connection exists	Bidirectional connection does not exist
Interconnection	Z	Imposes 1 state	Imposes 0 state

* These letter symbols appear at the AFFECTING input (or output) and are followed by a number. Each input (or output) AFFECTED by that input is labeled with that same number. When the labels EN, R, and S appear at inputs without the following numbers, the descriptions above do not apply. The action of these inputs is described under "Symbols Inside the Outline," see 3.3.

5 Bistable Elements

The dynamic input symbol, the postponed output symbol, and dependency notation provide the tools to differentiate four main types of bistable elements and make synchronous and asynchronous inputs easily recognizable (Figure 25). The first column shows the essential distinguishing features; the other columns show examples.

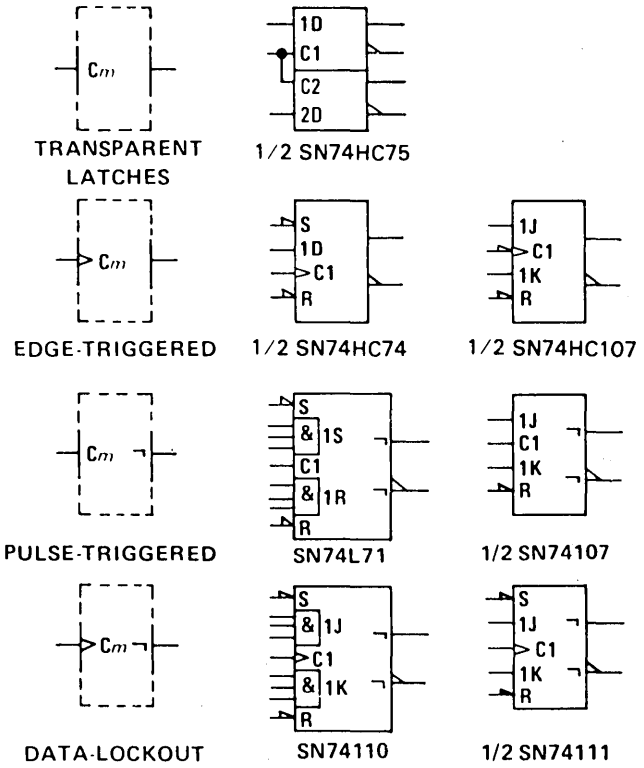


Figure 25. Four Types of Bistable Circuits

Transparent latches have a level-operated control input. The D input is active as long as the C input is at its internal 1 state. The outputs respond immediately. Edge-triggered elements accept data from D, J, K, R, or S inputs on the active transition of C. Pulse-triggered elements require the setup of data before the start of the control pulse; the C input is considered static since the data must be maintained as long as C is at its 1 state. The output is postponed until C returns to its 0 state. The data-lockout element is similar to the pulse-triggered version except that the C input is considered dynamic in that, shortly after C goes through its active transition, the data inputs are disabled, and data does not have to be held. However, the output is still postponed until the C input returns to its initial external level.

Notice that synchronous inputs can be readily recognized by their dependency labels (1D, 1J, 1K, 1S, 1R) compared to the asynchronous inputs (S, R), which are not dependent on the C inputs.

6 Coders

The general symbol for a coder or code converter is shown in Figure 26. X and Y may be replaced by appropriate indications of the code used to represent the information at the inputs and at the outputs, respectively.

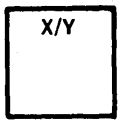


Figure 26. Coder General Symbol

Indication of code conversion is based on the following rule:

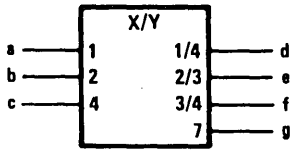
> Depending on the input code, the internal logic states of the inputs determine an internal value. This value is reproduced by the internal logic states of the outputs, depending on the output code.

The indication of the relationships between the internal logic states of the inputs and the internal value is accomplished by:

1) labeling the inputs with numbers. In this case, the internal value equals the sum of the weights associated with those inputs that stand at their internal 1-state, or by
2) replacing X by an appropriate indication of the input code and labeling the inputs with characters that refer to this code.

The relationships between the internal value and the internal logic states of the outputs are indicated by:

1) labeling each output with a list of numbers representing those internal values that lead to the internal 1-state of that output. These numbers shall be separated by solidi as in Figure 27. This labeling may also be applied when Y is replaced by a letter denoting a type of dependency



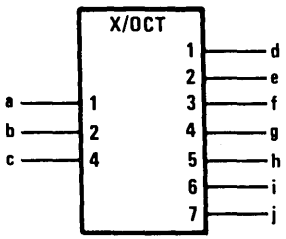
TRUTH TABLE

INPUTS			OUTPUTS			
c	b	a	g	f	e	d
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	1	0
0	1	1	0	1	1	0
1	0	0	0	1	0	1
1	0	1	0	0	0	0
1	1	0	0	0	0	0
1	1	1	1	0	0	0

Figure 27. An X/Y Code Converter

(see section 7). If a continuous range of internal values produces the internal 1 state of an output, this can be indicated by two numbers that are inclusively the beginning and the end of the range, with these two numbers separated by three dots (e.g., 4 . . . 9 = 4/5/6/7/8/9) or by

2) replacing Y by an appropriate indiction of the output code and labeling the outputs with characters that refer to this code as in Figure 28.



TRUTH TABLE

INPUTS			OUTPUTS						
c	b	a	j	i	h	g	f	e	d
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	0
0	1	1	0	0	0	0	1	0	0
1	0	0	0	0	0	1	0	0	0
1	0	1	0	0	1	0	0	0	0
1	1	0	0	1	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0

Figure 28. An X/Octal Code Converter

Alternatively, the general symbol may be used together with an appropriate reference to a table in which the relationship between the inputs and outputs is indicated. This is a recommended way to symbolize a PROM after it has been programmed.

7 Use of a Coder to Produce Affecting Inputs

It often occurs that a set of affecting inputs for dependency notation is produced by decoding the signals on certain inputs to an element. In such a case, use can be made of the symbol for a coder as an embedded symbol (Figure 29).

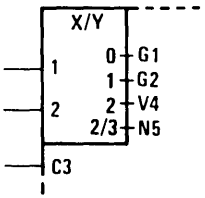


Figure 29. Producing Various Types of Dependencies

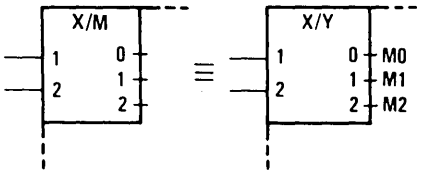


Figure 30. Producing One Type of Dependency

If all affecting inputs produced by a coder are of the same type as their identifying numbers shown at the outputs of the coder, Y (in the qualifying symbol X/Y) may be replaced by the letter denoting the type of dependency. The indications of the affecting inputs should then be omitted (Figure 30).

8 Use of Binary Grouping to Produce Affecting Inputs

If all affecting inputs produced by a coder are of the same type and have consecutive identifying numbers not necessarily corresponding with the numbers that would have been shown at the outputs of the coder, use can be made of the binary grouping symbol. k external lines effectively generate 2^k internal inputs. The bracket is followed by the letter denoting the type of dependency followed by m1/m2. The m1 is to be replaced by the smallest identifying number and the m2 by the largest one, as shown in Figure 31.

9 Sequence of Input Labels

If an input having a single functional effect is affected by other inputs, the qualifying symbol (if there is any) for that functional effect is preceded by the labels corresponding to the affecting inputs. The left-to-right order of these preceding labels is the order in which the effects or modifications must be applied. The affected input has no functional effect on the element if the logic state of any one of the affecting inputs, considered separately, would cause the affected input to have no effect, regardless of the logic states of other affecting inputs.

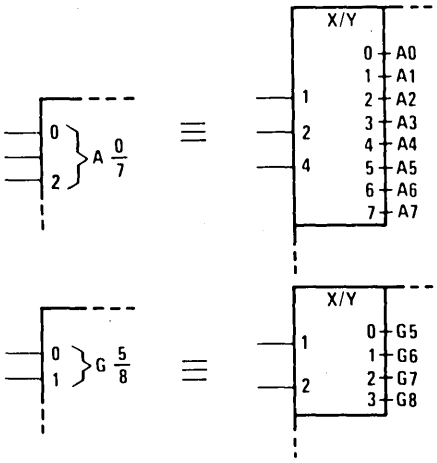


Figure 31. Use of the Binary Grouping Symbol

If an input has several different functional effects or has several different sets of affecting inputs, depending on the mode of action, the input may be shown as often as required. However, there are cases in which this method of presentation is not advantageous. In those cases, the input may be shown once with the different sets of labels separated by solidi (Figure 32). No meaning is attached to the order of these sets of labels. If one of the functional effects of an input is that of an unlabeled input to the element, a solidus will precede the first set of labels shown.

If all inputs of a combinational element are disabled (caused to have no effect on the function of the element), the internal logic states of the outputs of the element are not specified by the symbol. If all inputs of a sequential element are disabled, the content of this element is not changed, and the outputs remain at their existing internal logic states.

Labels may be factored using algebraic techniques (Figure 33).

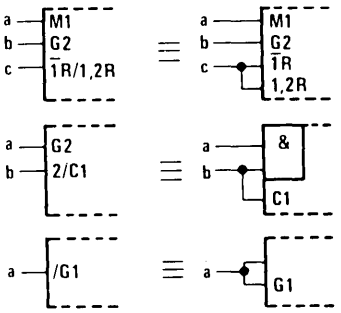


Figure 32. Input Labels

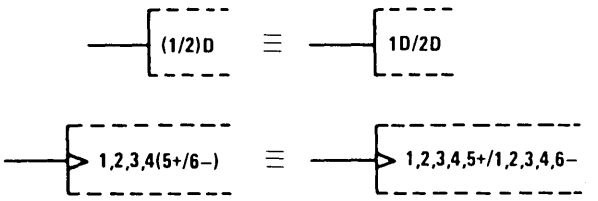


Figure 33. Factoring Input Labels

10 Sequence of Output Labels

If an output has a number of different labels, regardless of whether they are identifying numbers of affecting inputs or outputs or not, these labels are shown in the following order:

1) If the postponed output symbol has to be shown, this comes first, if necessary preceded by the indications of the inputs to which it must be applied
2) Followed by the labels indicating modifications of the internal logic state of the output, such that the left-to-right order of these labels corresponds with the order in which their effects must be applied
3) Followed by the label indicating the effect of the output on inputs and other outputs of the element.

Symbols for open-circuit or 3-state outputs, where applicable, are placed just inside the outside boundary of the symbol adjacent to the output line (Figure 34).

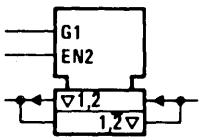


Figure 34. Placement of 3-State Symbols

If an output needs several different sets of labels that represent alternative functions (e.g., depending on the mode of action), these sets may be shown on different output lines that must be connected outside the outline. However, there are cases in which this method of presentation is not advantageous. In those cases, the output may be shown once with the different sets of labels separated by solidi (Figure 35).

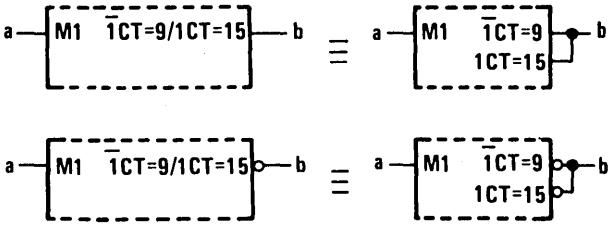


Figure 35. Output Labels

Two adjacent identifying numbers of affecting inputs in a set of labels that are not already separated by a nonnumeric character should be separated by a comma.

If a set of labels of an output not containing a solidus contains the identifying number of an affecting M*m* input standing at its internal 0 state, this set of labels has no effect on that output.

Labels may be factored using algebraic techniques (Figure 36).

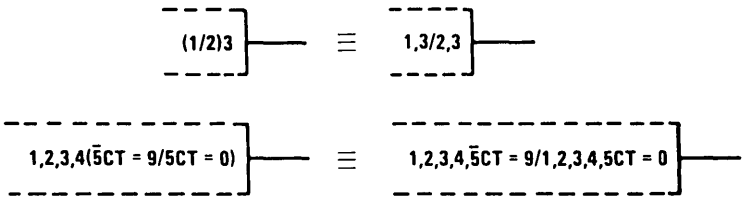


Figure 36. Factoring Output Labels

If you have questions on this Explantion of Logic Symbols, please contact:

Texas Instruments Incorporated
F.A. Mann, MS 3684
P.O. Box 655303
Dallas, Texas 75265

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IEEE Standards may be purchased from:

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Mechanical Data 5

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IC Sockets	5-9
Tape and Reel Program	5-21

Electrical characteristics presented in this data book, unless otherwise noted, apply for circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.

EXAMPLE: **SN** **74BCT2420** **FN**

Prefix

MUST CONTAIN TWO TO FOUR LETTERS

SN Standard Prefix

Unique Circuit Description

MUST CONTAIN SIX TO NINE CHARACTERS

Examples: 74BCT2420
74BCT2423
74BCT2424

Package

MUST CONTAIN ONE OR TWO LETTERS

FN (Leadless Plastic Chip Carriers)
PQ (Plastic Quad Flat Pack) (JEDEC)
(From pin-connection diagram on individual data sheet)

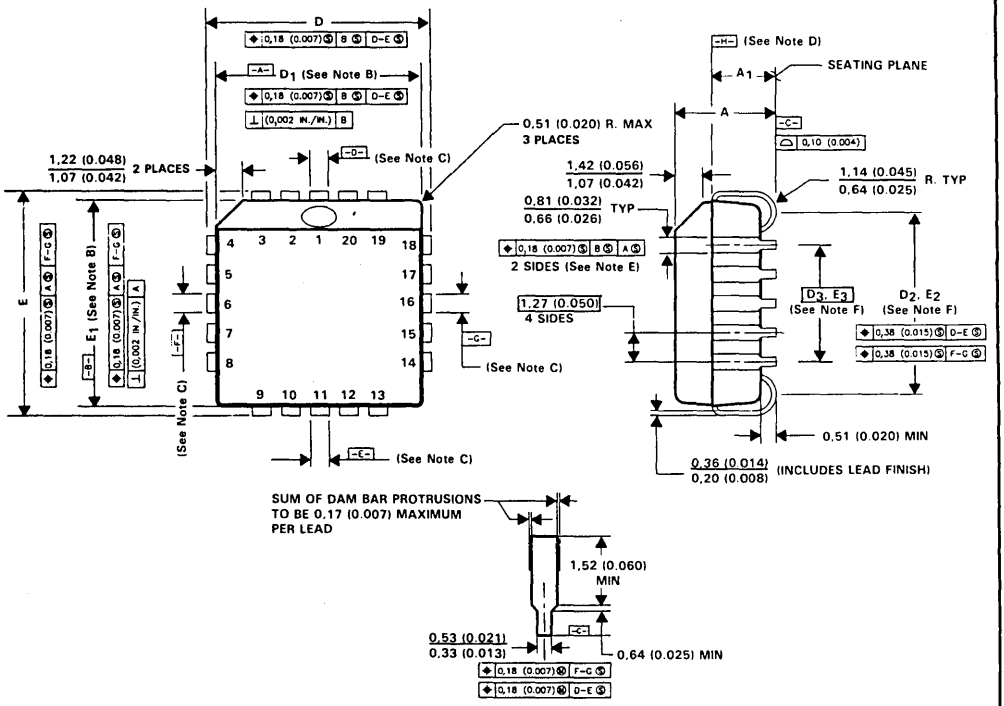
NuBus™ Product
Mechanical Data Cross-Reference

DEVICE	PACKAGE	
	PIN NO.	TYPE
SN74BCT2420	68	FN
SN74BCT2423	68	FN
SN74BCT2424	68	FN
SN74BCT2425	100	PQ
SN74ACT2440	68	FN
SN74ACT2441	100	PQ
SN74ALS2442	20	FN

FN020, FN028, FN044, FN052, FN068, and FN084 plastic chip carrier packages

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.

FN020, FN028, FN044, FN052, FN068, and FN084
(20-terminal package used for illustration)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. All dimensions conform to JEDEC Specification MO-047AA/AF. Dimensions and tolerancing are per ANSI Y14.5M–1982.

B. Dimensions D_1 and E_1 do not include mold flash protrusion. Protrusion shall not exceed 0,25 (0.010) on any side.

C. Datums D–E and F–G for center leads are determined at datum –H–

D. Datum –H– is located at top of leads where they exit plastic body.

E. Location to datums –A– and –B– to be determined at datum –H–

F. Determined at seating plane –C–

TEXAS INSTRUMENTS
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FN020, FN028, FN044, FN052, FN068, and FN084 plastic chip carrier packages (continued)

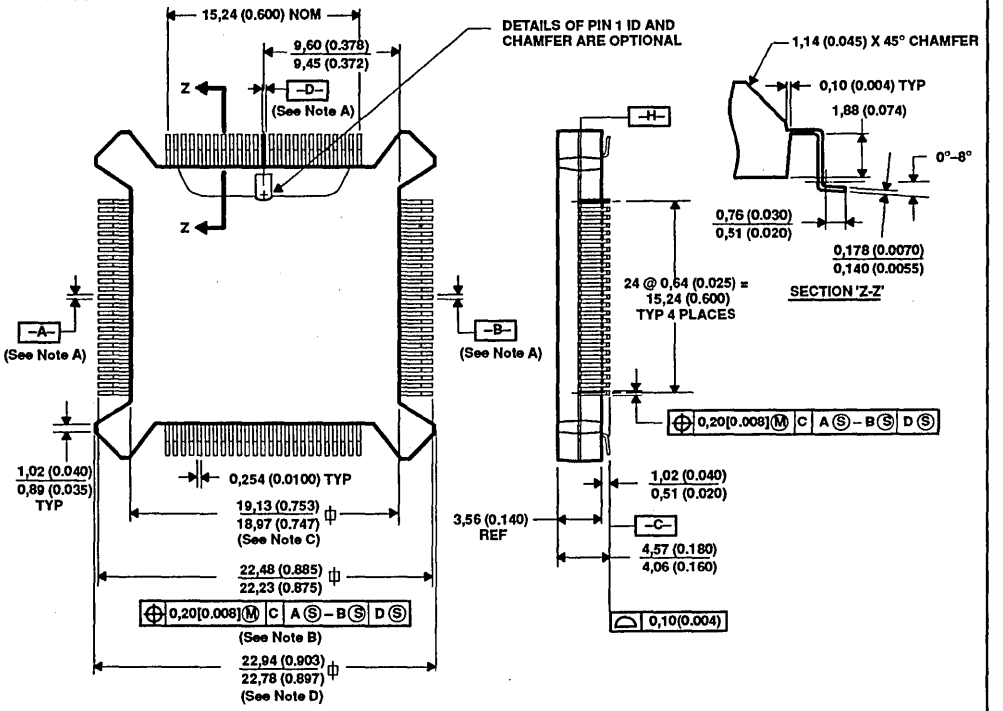
JEDEC OUTLINE	NO. OF PINS	A		A_1		D, E		D_1, E_1		D_2, E_2 (See Note F)		D_3, E_3 BASIC
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
MO-047AA	20	4,19 (0.165)	4,57 (0.180)	2,29 (0.090)	3,05 (0.120)	9,78 (0.385)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	7,37 (0.290)	8,38 (0.330)	5,08 (0.200)
MO-047AB	28	4,19 (0.165)	4,57 (0.180)	2,29 (0.090)	3,05 (0.120)	12,32 (0.485)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	9,91 (0.390)	10,92 (0.430)	7,62 (0.300)
MO-047AC	44	4,19 (0.165)	4,57 (0.180)	2,29 (0.090)	3,05 (0.120)	17,40 (0.685)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	14,99 (0.590)	16,00 (0.630)	12,70 (0.500)
MO-047AD	52	4,19 (0.165)	5,08 (0.200)	2,29 (0.090)	3,30 (0.130)	19,94 (0.785)	20,19 (0.795)	19,05 (0.750)	19,20 (0.756)	17,53 (0.690)	18,54 (0.730)	15,24 (0.600)
MO-047AE	68	4,19 (0.165)	5,08 (0.200)	2,29 (0.090)	3,30 (0.130)	25,02 (0.985)	25,27 (0.995)	24,13 (0.950)	24,33 (0.958)	22,61 (0.890)	23,62 (0.930)	20,32 (0.800)
MO-047AF	84	4,19 (0.165)	5,08 (0.200)	2,29 (0.090)	3,30 (0.130)	30,10 (1.185)	30,35 (1.195)	29,21 (1.150)	29,41 (1.158)	27,69 (1.090)	28,70 (1.130)	25,40 (1.000)

NOTES: A. All dimensions conform to JEDEC Specification MO-047AA/AF. Dimensions and tolerancing are per ANSI Y14.5M–1982.

F. Determined at seating plane $\boxed{-C-}$

PQ plastic quad flat package

This plastic package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The package is intended for surface mounting on solder leads on 0,64(0.025) centers. Leads require no additional cleaning or processing when used in solder assembly.



Falls Within JEDEC MO-069AD Dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Datums A–B and –D– to be determined where center leads exit plastic body at plane –H–.
B. Dimension to be determined at plane –C–.
C. Dimension to be determined at plane –H–.
D. Dimension to be determined at plane –H–, dimension does not include 0,254 (0.010) maximum mold protrusion per side.
E. Dimensions and tolerance per ANSI Y14.5M-1982.
F. Tolerances: X,XX ±0,12 (X.XXX ±0.005)
X,XXX ±0,050 (X.XXXX ±0.002) unless otherwise specified.

INTRODUCTION

Texas Instruments has developed solutions for today's high density packaging needs. The TI facility at Attleboro, Massachusetts (one of the world's largest suppliers of multimetal systems) provides leading-edge technology which, combined with reliable, high-volume, off-the-shelf interconnection products, allows TI to quickly meet volume commercial applications.

During the last decade, TI has produced one of the largest IC socket families. TI's sockets include every type and size socket in common use today and are available in a wide choice of contact materials and designs.

Our sockets are designed for:

- easy and efficient hand assembly
- compatibility with automatic assembly equipment
- maximum performance and board density

This section provides information on the following types of IC socket products.

PRODUCTION SOCKETS	TYPE
Plastic Leaded Chip Carrier	PLCC
Single-In-Line Packages	SIP
Pin-Grid Arrays	PGA
Dual-In-Line	DIP
Dual-In-Line 0.070-inch spacing	Shrink Pack
Quad-In-Line	QUIP

BURN-IN/TEST SOCKETS	TYPE
Plastic Leaded Chip Carrier	PLCC
Pin Grid Array	PGA
Small Outlilne	J Lead
Dual-In-Line	DIP
Dual-In-Line 0.070-inch spacing	Shrink Pack
Small Outline	Flat Pack
Quad	Flat Pack

Specially formulated alloys give the TI contact springs:

- Low Contact Resistance
- High Contact Strength (to stand up to repetitive insertions and withdrawals)
- High normal forces assure gas-tight reliability

A full line of reliable, readily available, low-cost interconnection systems means premium performance at an economical price.

Additional information on these and other TI products, including pricing and delivery quotations, may be obtained from your nearest authorized TI Distributor, TI Sales Representative or:

Texas Instruments Incorporated
Connector Systems Department, MS 14-3
Attleboro, Massachusetts 02703
Telephone: (508) 699-5242/5375
TELEX: 92-7708

PERFORMANCE SPECIFICATIONS

Mechanical

Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Vibration: 15 G max
Shock: 100 G max
Insertion force: 0.59 lbs per position typ
Withdrawal force: 0.25 lbs per position typ
Normal force: 200 g min, 450 g typ
Wipe: 0.075 in min
Durability: 5 cycles min
Contact retention: 1.5 lbs min

Electrical

Current carrying capacity: 1 A per contact
Insulation resistance: 5000 MΩ min
Dielectric withstanding voltage: 1000 V ac rms min
Capacitance: 1 pF max

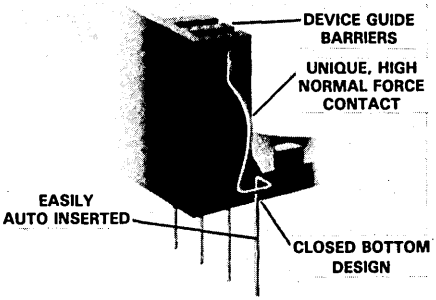
Environmental

Operating temperature:
Operating: – 40°C to 85°C
Storage: –40°C to 95°C
Temperature cycling with humidity: will conform to final EIA specifications

MATERIALS

Body — Ryton R-4 (40% glass) UL 94 V-0 rating
Contacts — CDA 510 spring temper
Contact finish — 90/10 tin/lead (200 μin –400 μin) over 40 μin copper

Extraction tool available, consult factory
Contact factory for detailed information

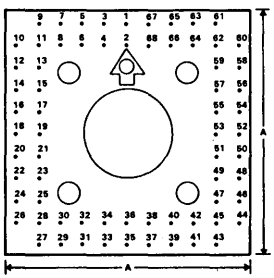


PART NUMBER SYSTEM

CPR PH XXX – X – X – O

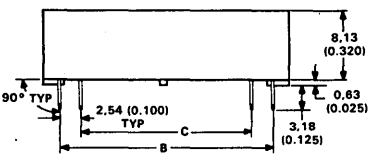
- O — Contact surface 1 — tin/lead plating
- X — Contact spacing 1 - 0.050 in
- XXX — Number of pos (044, 052, 068, 084)
- PH — Plated thru hole, solder tail
- CPR — TI socket Series
  Plastic leaded chip carrier

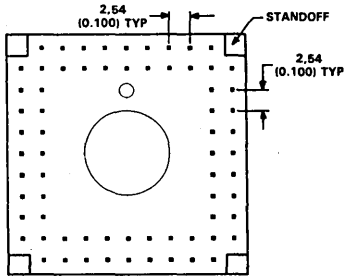
PLASTIC LEADED CHIP CARRIER CPR SERIES



68-Pin shown

NOTE: Socket electrical pin-out pattern represents component side of P.C.B. layout. (TYP. counter clockwise numbering pin-out system.)





Pos	A	B	C
44	21,43 (0.844)	17,78 (0.700)	12,70 (0.500)
52	23,98 (0.944)	20,32 (0.800)	15,24 (0.600)
68	29,06 (1.144)	25,40 (1.000)	20,32 (0.800)
84	34,14 (1.344)	30,48 (1.200)	25,40 (1.000)

Dimensions in parentheses are in inches

TEXAS INSTRUMENTS
34 Forest Street • Attleboro, Massachusetts 02703

PRODUCT FEATURES

Can be loaded by top actuated insertion or press-in insertion, either manually or automatically
High reliability due to high pressure contact point
Open body and high stand-off design provide high efficiency in heat dissipation
High durability up to 10,000 cycles
Compact design

PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads per specific IC device
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Durability: 10,000 cycles 10 mΩ max contact resistance change
Insertion force: Zero g
Withdrawal force: Zero g†

Electrical

Contact rating: 1 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1000 MΩ per MIL-STD 202, Method 302, Condition B
Dielectric withstanding voltage: 500 V ac rms per MIL-STD 202, Method 301

Environmental

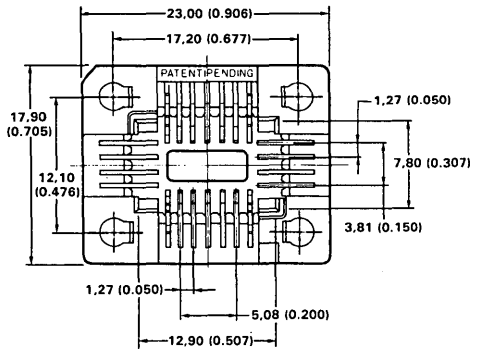
Thermal shock: 100 cycles, −25°C to +150°C
Temperature soak: 150°C for 48 hours
Operating temperature: −40°C to +150°C

MATERIALS

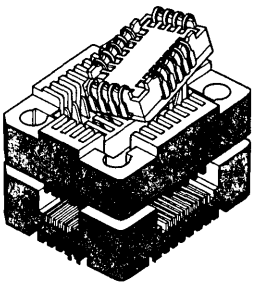
Body — ULTEM glass filled (UL 94 V-0)
Contact — copper alloy
Plating‡ — overall gold plate 4 μin over min 70 μin nickel plating

†After IC is unlocked from the socket
‡For additional plating options contact factory
For complete test report contact the factory

PLCC BURN-IN/TEST SOCKETS CPJ SERIES



Dimensions in parentheses are inches
Contact factory for detailed information

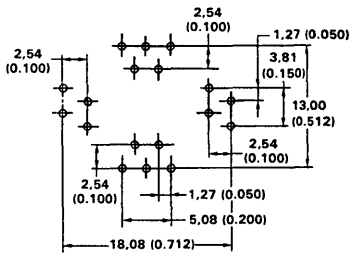


PART NUMBER SYSTEM

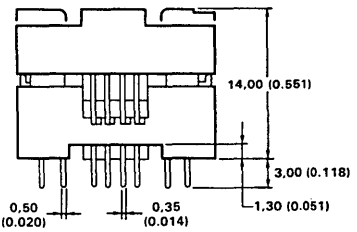
CPJ XX XX X – XXX – B

- CPJ — TI Burn-in PLCC series
- XX — Material: AA = copper alloy
- XX — Contact finish: 33 = overall gold plate
- X — Pitch: A = 0.050
- XXX — Number of contacts
- B

18 PIN FOOTPRINT SHOWN



SIZES: 18 PIN
22 PIN



PERFORMANCE SPECIFICATIONS†

Mechanical
Vibration: MIL-STD-202
Durability: 30 cycles
Insertion force: Zero g
Withdrawal force: Zero g‡
Contact (normal) force: 200 g min
Contact retention force: 2 lbs per circuit min

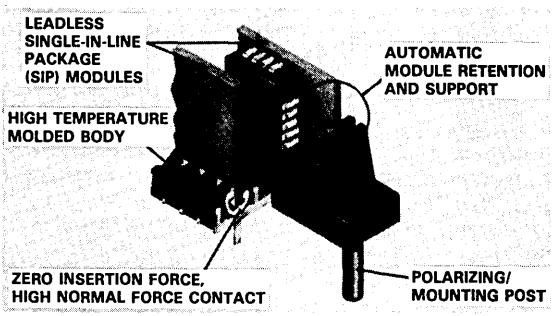
Electrical
Contact rating: 1 A
Contact resistance: 30 mΩ max initial
Insulation resistance: 1000 MΩ at 500 dc
Dielectric strength: 1500 V ac rms
Capacitance: 2 pF max

†Values may vary due to test sequence and SIP module configuration
‡After module is unlocked from the receptacle
For a complete test report, please contact factory

Environmental
(20 mΩ max contact resistance change after all tests)
Operating and storage temperature: −40°C to 100°C
Humidity: MIL-STD 202, Method 106D, 10 days
Temperature soak: 85°C for 160 hours
Thermal Shock: 5 cycles, −40°C to 85°C per MIL-STD 202, Method 107E

MATERIALS
Body — PES polyether sulfone, glass filled, UL 94 V-0
Contact — Beryllium copper C17000; phosphor bronze alloy CA510
Contact finishes — Post plate min 200 µin tin/lead over min 50µin nickel overall
Post plate min 30 µin hard gold over min 75 µin nickel overall

For additional plating options contact the factory.



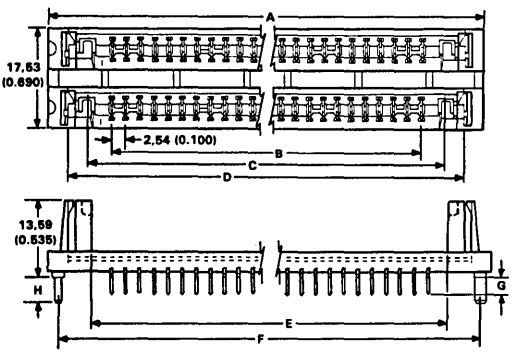
PART NUMBER SYSTEM

TS8X XX XX X −XX − XX

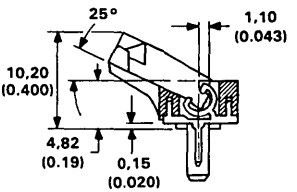
- XX (last): Variations — 00 — standard product
- XX: Size (number of contacts per row)
- X: Housing material — A — PES
- XX: Contact base material/plating
  - 01—C17000/30 µin gold
  - 02—CA510/30 µin gold
  - 03—C17000/200 µin tin/lead
  - 04—CA510/200 µin tin/lead
- XX: Configuration/row-to-row spacing
  - 01—single row/N/A
  - 03—dual row/0.300 in
  - 04—dual row/0.400 in
  - 05—dual row/0.500 in
- TS8X: Series number denotes
  - 0—0.100 in pitch, vertical mount
  - 1—0.100 in pitch, low-profile (25°) mount

Consult factory for availability of configurations, materials, and sizes.

DUAL ROW VERTICAL



SINGLE ROW LOW PROFILE



Ckt. Size	A	B	C	D	E	F	G	H
30	96,52 (3.800)	73,66 (2.900)	82,14 (3.234)	89,28 (3.515)	80,52 (3.170)	92,71 (3.650)	2,79 (0.110)	3,86 (0.152)

Contact factory for detailed information

Dimensions in parentheses are in inches

TEXAS INSTRUMENTS
34 Forest Street • Attleboro, Massachusetts 02703

PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads 0.015 in to 0.021 in diameter
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Recommended hole grid pattern: 0.100 in ± 0.002 in each direction
Vibration: 15 G, 10-2000 Hz per MIL-STD 1344A, Method 2005.1 Test Condition III
Shock: 100 G, sawtooth waveform, 2 shocks each direction per MIL-STD 202, Method 213, Test Condition I
Durability: 5 cycles, 10 mΩ max contact resistance change per MIL-STD 1344, Method 2016
Insertion force: 3.6 oz (102 g) per pin typ using 0.018 in diameter test pin
Withdrawal force: 0.5 oz (14 g) per pin min using 0.018 in diameter test pin

Electrical

Contact rating: 1 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1000 MΩ at 500 V dc per MIL-STD 1344, Method 3003.1
Dielectric withstanding voltage: 1000 V ac rms per MIL-STD 1344, Method 3001.1
Capacitance: 1 pF max per MIL-STD 202, Method 305

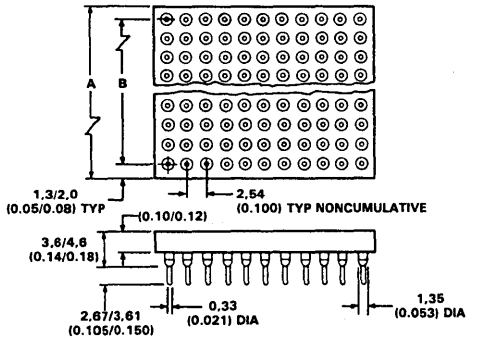
Environmental

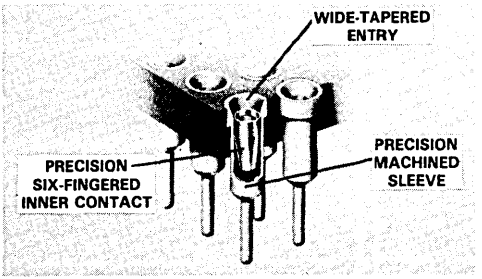
Operating temperature: −65°C to 125°C, gold; −40°C to 100°C, tin/lead
Corrosive atmosphere: 10 mΩ max contact resistance change when exposed to 22% ammonium sulfide for 4 hours
Gas tight: 10 mΩ max contact resistance change when exposed to nitric acid vapor for 1 hour
Temperature soak: 10 mΩ max contact resistance change when exposed to 105°C temperature for 48 hours

MATERIALS

Body — PBT polyester UL 94 V-0
On request, G10/FR4 or Mylar film
Outer sleeve — Machined Brass (QQ-B-626)
Inner contact — Beryllium copper (QQ-C-530) heat treated
Plating: (specified by part number)

PIN GRID ARRAY





Inner contact — 30 μin gold over 50 μin nickel or 100 μin tin/lead over 50 μin nickel
Outer sleeve — 10 μin gold over 50 μin nickel or 50 μin tin/lead over 50 μin nickel

PART NUMBER SYSTEM

C X G XX − XXX X X − X X

- Pin Length

WIRE WRAP	SOLDER TAIL
3-0.510 long	9-0.105/0.150

- Plating

P/N	Sleeve	Clip
0	Gold	Gold
5	Tin	Gold

- Body Style and Orientation
- Contact Loading Pattern
- Number of Pins 024 to 324
- Overall Grid Size 5×5=05 to 18×18=18
- BODY MATERIAL
  - G — Glass Filled Epoxy
  - P — PBT Polyester
- Pin Grid Array
- TI Socket

Insulator Size	A ±0.010	B ±0.005†
9×9	(0.950) 24,13	(0.800) 20,32
10×10	(1.050) 26,67	(0.900) 22,86
11×11	(1.150) 29,21	(1.000) 25,40
12×12	(1.250) 31,75	(1.100) 27,94
13×13	(1.350) 34,29	(1.200) 30,48
14×14	(1.450) 36,83	(1.300) 33,02
15×15	(1.550) 39,37	(1.400) 35,56
16×16	(1.650) 41,91	(1.500) 38,10
17×17	(1.750) 44,45	(1.600) 40,64
18×18	(1.850) 46,99	(1.700) 43,18

†Noncumulative
Dimensions in parentheses are inches
Consult factory for detailed information

PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads per specific IC device
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Durability: 10,000 cycles, 20 mΩ max contact resistance change
Insertion force: 1.3 oz per position max
Withdrawal force: 8.8 grams per position min

Electrical

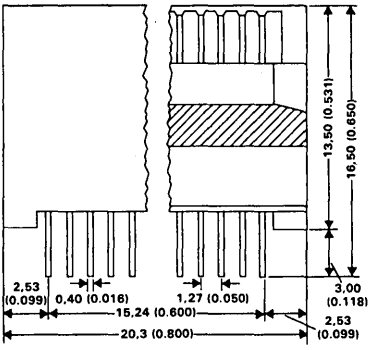
Contact rating: 1.0 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1000 MΩ per MIL-STD 202, Method 302, Condition B
Dielectric withstanding voltage: 700 V ac rms per MIL-STD 202, Method 301

Environmental

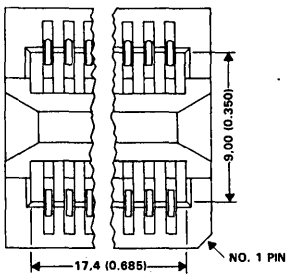
Thermal shock: 100 cycles, −25°C to +180°C, 1 hour
Temperature soak: 180°C for 1000 hours, 80 mΩ max change
Operating temperature: −65°C to +180°C

MATERIALS

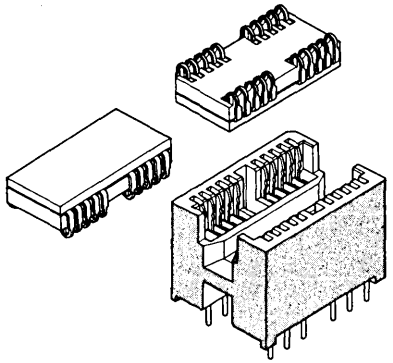
Body — PES glass filled UL 94 V-0
Contact — copper alloy
Plating — overall gold plate min 4 μin over min 70 μin nickel plating



02 VERSION SHOWN



Dimensions in parentheses are inches
Contact factory for detailed information



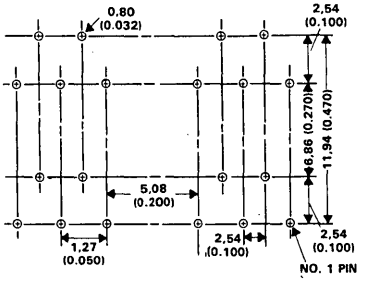
PART NUMBER SYSTEM

CSJT XXX – XX – XX X

- CSJT — TI SOJ series
- XXX — Number of Contacts
- XX — Contact Finish
  - 37 = Overall gold plate 4 μin
  - 38 = Overall gold plate 30 μin
  - 57 = Selective gold plate 4 μin
  - 58 = Selective gold plate 30 μin
- XX — Body Variation
  - 02 = Standard 1 forward/backward insertion
  - 03 = Special/orientation pin
  - 04 = Special/high standoff
  - 05 = Special/24-pin
  - 06 = Standard 2 forward insertion, BECU
- X — Body Material
  - Blank = G.F. PES
  - A = PPS R4-03
  - B = G.F. PEI

SIZES: 20 pin
26 pin

20-PIN (02 VERSION) FOOTPRINT SHOWN



TEXAS INSTRUMENTS
34 Forest Street • Attleboro, Massachusetts 02703

PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads 0.011 ± 0.003 in by 0.018 ± 0.003
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Recommended hole grid pattern: 0.100 in ± 0.003 in each direction
Vibration: 15 G, 10-2000 Hz per MIL-STD 1344A, Method 2005.1 Test Condition III.
Shock: 100 G, sawtooth waveform, 2 shocks each direction per MIL-STD 202, Method 213, Test Condition I
Durability: 5 cycles, 10 mΩ max contact resistance change per MIL-STD 1344, Method 2016
Insertion force (C7X and C86): 16 oz (454 g) per pin max
Withdrawal force: (40 g) per pin min

Electrical

Contact rating: 1 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1000 MΩ at 500 V dc per MIL-STD 1344, Method 3003
Dielectric withstanding voltage: 1000 V ac rms per MIL-STD 1344, Method 3001.1
Capacitance: 1 pF max per MIL-STD 202, Method 305

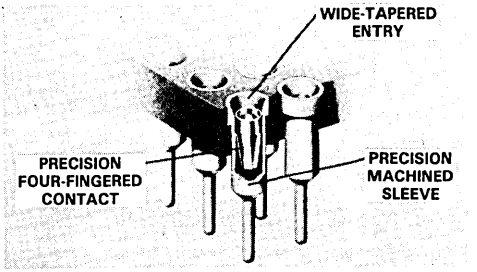
Environmental

Operating temperature: −55°C to 125°C, gold; −40°C to 100°C, tin
Corrosive atmosphere: 10 mΩ max contact resistance change when exposed to 22% ammonium sulfide for 4 hours
Gas tight: 10 mΩ max contact resistance change when exposed to nitric acid vapor for 1 hour
Temperature soak: 10 mΩ max contact resistance change when exposed to 105°C temperature for 48 hours

Materials (C7X and C86)

Body — PBT polyester UL 94 V-0
C7X Contacts — Outer sleeve: brass
Clip: BECU
Contact finish — clip 30 μin gold over 50 μin nickel or 50 μin tin/lead over 50 μin nickel
Specified by Part Number — sleeve 10 μin gold over 50 μin nickel or 50 μin tin/lead over 50 μin nickel
C86 Contacts — Phosphor bronze base metal
C86 Contact-finish — Tin plate 200 μin over copper flash

C7X SERIES — SCREW MACHINE

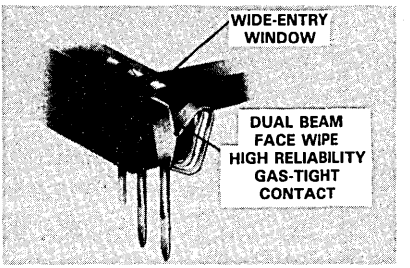


C7X SERIES — SCREW MACHINE PART NUMBER SYSTEM

C7X (X) XX − X X

- X: Variations
  - Solder Tail : 9 — Pin length 0.125 Typ
  - Wire Wrap : 3 — Pin length 0.510
- X: Plating (Sleeve/Clip)
  - 0 — Gold/Gold
  - 5 — Tin/Gold
- XX: Number of Positions
- (X): S — Single-in-line package (where applicable)
- C7X: Screw Machine Socket
  - 1 — wire wrap
  - 2 — solder tail

C86 SERIES — STAMPED AND FORMED

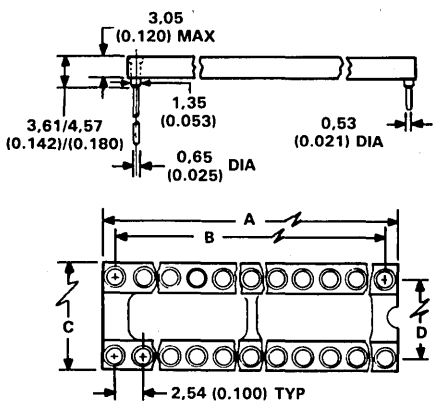


C86 SERIES PART NUMBER SYSTEM

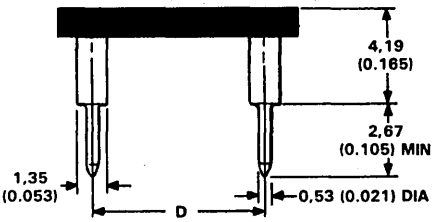
C 86 XX − 01

- 01: Variation
  - 01 — Standard product
- XX: Number of positions
- 86: Tin Dual Beam Face Wipe
- C: TI Socket Series

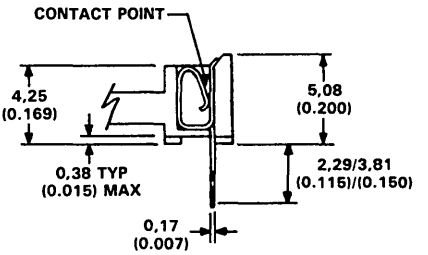
DUAL-IN-LINE
C7X AND C86 SERIES



C7X SERIES



C86 SERIES



DIPS

Positions	Dim A Max	Dim B ±0.005	Dim C Max	Dim D ±0.005	Positions	Dim A Max	Dim B ±0.005	Dim C Max	Dim D ±0.005
6	7,62 (0.300)	5,08 (0.200)	10,16 (0.400)	7,62 (0.300)	†24	30,48 (1.200)	27,94 (1.100)	12,76 (0.500)	10,16 (0.400)
8	10,16 (0.400)	7,62 (0.300)	10,16 (0.400)	7,62 (0.300)	28	35,56 (1.400)	33,02 (1.300)	17,78 (0.700)	15,24 (0.600)
14	17,78 (0.700)	15,24 (0.600)	10,16 (0.400)	7,62 (0.300)	32	40,64 (1.600)	38,10 (1.500)	17,78 (0.700)	15,24 (0.600)
16	20,32 (0.800)	17,78 (0.700)	10,16 (0.400)	7,62 (0.300)	34	45,72 (1.800)	43,18 (1.700)	17,78 (0.700)	15,24 (0.600)
18	22,86 (0.900)	20,32 (0.800)	10,16 (0.400)	7,62 (0.300)	40	50,80 (2.000)	48,26 (1.900)	17,78 (0.700)	15,24 (0.600)
20	25,40 (1.000)	22,86 (0.900)	10,16 (0.400)	7,62 (0.300)	48	60,96 (2.400)	58,42 (2.300)	17,78 (0.700)	15,24 (0.600)
22	27,94 (1.100)	25,40 (1.000)	12,76 (0.500)	10,16 (0.400)	50	63,50 (2.500)	60,96 (2.400)	25,40 (1.000)	7,62 (0.900)
24	30,48 (1.200)	27,94 (1.100)	17,78 (0.700)	15,24 (0.600)	64	81,28 (3.200)	78,74 (3.100)	25,40 (1.000)	22,86 (0.900)
†24	30,48 (1.200)	27,94 (1.100)	10,16 (0.400)	7,62 (0.300)					

†Nonstandard sizes
Not all sizes available in each series
Dimensions apply to all series

Dimensions in parentheses are inches
Contact factory for detailed information

TEXAS INSTRUMENTS
34 Forest Street • Attleboro, Massachusetts 02703

PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads 0.011 in by 0.018 in
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hold size range: 0.032 in to 0.042 in
Durability: 10K cycles — CM Series, 5K cycles — CP/CQ

Electrical

Contact rating: 1 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1000 MΩ at 500 V dc
Dielectric withstanding voltage: 1000 V ac rms
Capacitance: 1 pF max per MIL-STD 202, Method 305

Environmental

Operating temperature: −65°C to 170°C — CP/CM Series,
−65°C to 150°C — CQ Series
Humidity: 10 mΩ max contact resistance
Temperature Soak: 10 mΩ max contact resistance change

MATERIALS

Body — PPS (polyphenylen sulfide) UL 94 V-0
Contacts — Higher performance copper nickel alloy
Plating:† 4 μin of gold min over 100 μin of nickel min

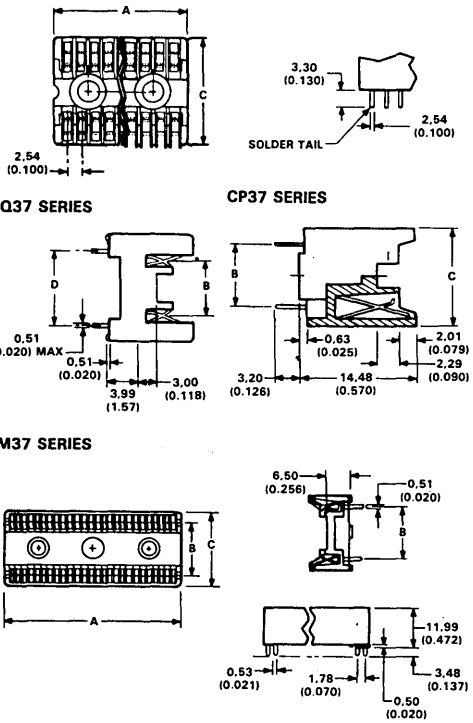
†For additional plating options consult the factory

PART NUMBER SYSTEM

C X 37 XX – 22 S X

- C — TI Socket Series
- X — Series Features: Q — Auto unloadable; P — High density mounting; M — Shrink 0.070 centers
- 37 — Overall gold plate
- XX — Number of positions
- 22 — Copper nickel alloy Soldertail
- S — PPS high temperature body material
- X — Pin to pin: A — 0.100 centers; B — 0.070 centers

BURN-IN/TEST DIP SOCKETS



CQ37 SERIES

Number of Positions	A ±0.01 Length	D ±0.02	C ±0.01 Width	B ±0.01 Contact
14	20,32 (0.800)			
16	22,35 (0.880)	12,70	15,24	7,62
18	24,89 (0.980)	(0.500)	(0.600)	(0.300)
20	27,43 (1.080)			
24	32,51 (1,280)			
28	37,59 (1.480)	19,05	22,86	15,24
40	52,83 (2.080)	(0.750)	(0.900)	(0.600)
42	55,37 (2.180)			

CP37 SERIES

Number of Positions	A max Length	B ±0.02	C max Width
8	11,68 (0.460)		
14	17,78 (0.700)		
16	20,32 (0.800)	7,62	12,70
18	22,86 (0.900)	(0.300)	(0.500)
20	25,40 (1.000)		
24	30,48 (1.200)		
28	35,56 (1.400)	15,24	20,32
40	50,80 (2.000)	(0.600)	(0.800)

CM37 SERIES

Number of Positions	A ±0.016 Length	B ±0.02	C ±0.016 Width
28	27,18 (1.070)	10,67 (0.420)	17,20 (0.677)
40	37,85 (1.490)		
42	39,62 (1.560)	16,51 (0.650)	23,11 (0.910)
54	50,29 (1.980)		
64	59,18 (2.330)	20,32 (0.800)	26,92 (1.060)

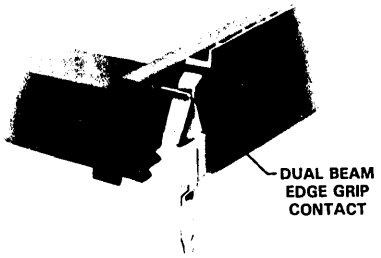
Dimensions in parentheses are inches
Contact factory for detailed information

PERFORMANCE SPECIFICATIONS

Insertion force: 16 oz (454 g) per pin max
Withdrawal force: 1.5 oz (42 g) per pin min
Operating temperature: −40°C to 100°C, tin/lead
Accommodates IC leads 0.011 ± 0.0003 in by 0.018 ± 0.003 in
Contact rating: 1 A per contact

MATERIALS

Body — PBT polyester UL 94 V-0
C4S & CxW Contacts — Copper alloy
Contact finish — Reflow tin plating, 40 μin min



PART NUMBER SYSTEM FOR CxW SERIES

C X W XX – 11

- XX: Number of contacts (42, 52, 64)
- W: Staggered leads
- X: 5 – 64 contacts; 6 – 42, 52 contacts
- C: TI Socket Series

QUAD-IN-LINE (CxW SERIES)

Product Number	A Max Length	B Row to Row	C Max Row to Row
C5W64-11	41,90 (1.65)	22,90 (0.950)	19,05 (0.750)
C6W42-11	27,90 (1.10)	22,90 (0.900)	17,80 (0.700)
C6W52-11	34,30 (1.35)	22,90 (0.900)	17,80 (0.700)

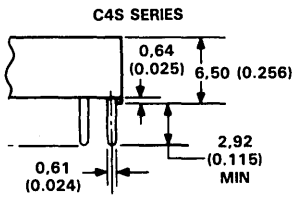
Dimensions in parentheses are inches
Contact factory for detailed information

PART NUMBER SYSTEM† FOR C4S SERIES

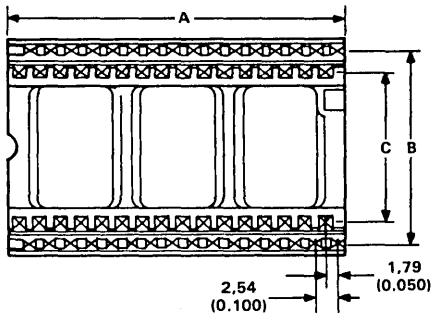
C 4 S XX – 02

- XX: Number of contacts 28, 40, 42, 52, 54, 64
- S: Shrink Pack (0.070 in pin-to-pin contact spacing)
- 4: Reflow tin plating
- C: TI Socket Series

†Also available in screw machine contacts



QUAD-IN-LINE (CxW SERIES)

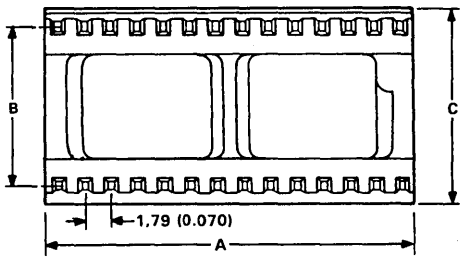


C4S SERIES

Positions	A Max Length	B Row to Row	C Max Width
28	25,02 (0.985)	10,16 (0.400)	13,00 (0.512)
40	35,69 (1.405)	15,24 (0.600)	17,98 (0.708)
64	57,07 (2.247)	19,05 (0.750)	21,62 (0.851)

Dimensions in parentheses are inches

SHRINK PACK DIP (C4S SERIES)



TEXAS INSTRUMENTS
34 Forest Street • Attleboro, Massachusetts 02703

PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads per specific IC device
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Durability: 5000 cycles, 10 mΩ max contact resistance change per MIL-STD 1344, Method 2016

Electrical

Contact rating: 1 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1 MΩ at 500 V dc per MIL-STD 1344, Method 3003.1
Dielectric withstanding voltage: 700 V ac rms per MIL-STD 1344, Method 3001.1
Capacitance: 1 pF max per MIL-STD 202, Method 305

Environmental

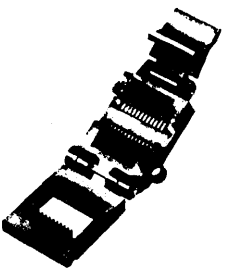
Operating temperature: −65°C to 170°C
Humidity: 10 mΩ max contact resistance change when tested per MIL-STD 202, Method 103B
Temperature soak: 10 mΩ max contact resistance change when exposed to 105°C temperature for 48 hours

MATERIALS

Body — CFP Series — PES (polyether sulfone) glass filled UL 94 V-0
Temperature: −65°C to 170°C
Contact — Beryllium copper
Plating:† Overall gold plate min 4 μin over min 70 μin nickel plating

†For additional plating option consult the factory.
Dimensional drawings available from factory.

SMALL OUTLINE FLAT PACK (CFPH/K SERIES)

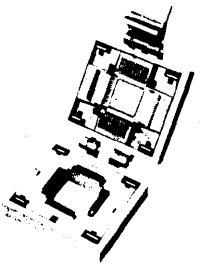


PART NUMBER SYSTEM

C XX X – XXX – XX – 01

- C — TI Series socket
- XX — Style FP — Flat pack
- X — Configuration
  - H — 14, 16, 18, 20 Positions
  - K — 24, 28 Positions
- XXX — Number of positions
- XX — Plating
  - 37 — overall gold plate
- 01

QUAD FLAT PACK (CFPM SERIES)

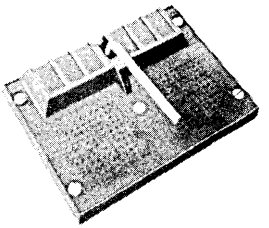


PART NUMBER SYSTEM

CXX X – XXX – XX – 01X

- CXX — TI socket
  - Style PF — Flat Pack
- X — Configuration
  - M — Quad pack
- XXX — Number of positions
- XX — Plating
  - 37 — overall gold plate
- 01X — Variations
  - A — 1.0 mm ℄ contact spacing
  - B — 0.8 mm ℄ contact spacing

PIN GRID ARRAY (CZFW SERIES)



PART NUMBER SYSTEM

C XX X – XXX – XX – 01

- C — TI Series socket
- XX — Style ZF — Zero force
- X — Configuration
  - W — 11 × 11 × 2
- XXX — Number of positions
- XX — Plating
  - 37 — overall gold plate
- 01

AVAILABLE SIZES

CFPH Series 14, 16, 18, 20 CFPK Series 24, 28	Small Outline Flat Pack
CFPM Series 64, 80	Quad Flat Pack
CZFW Series 11×11×2	Pin Grid Array

Contact factory for detailed information

For more information contact your local distributor or contact TI directly:

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D-8000 Muenchen 81
Phone: 011-49-89-915081

Introduction

A new packaging system, *SMti*™ Tape and Reel, has emerged along with the introduction of surface-mount semiconductor packages by Texas Instruments.

Benefits

SMti Tape and Reel not only offers a new shipping method that protects components from mechanical and electrical damage, but also includes the benefits of automated inventory control, ship to stock, and total compatibility with today's automated placement systems. *SMti* Tape and Reel continues the trend towards industry automation and cost reduction and contributes to the overall goal of electronic system quality and reliability.

Features

The features of *SMti* Tape and Reel packaging are as follows.

- *SMti* Tape and Reel packaging is in full compliance with EIA Standard 481-A, "Taping of Surface-Mount Components for Automatic Placement."
- Industry-compatible tape format allows second sourcing without costly and time-consuming equipment changeovers and record-keeping changes.
- Static-inhibiting materials, used in carrier tape manufacture, provide device protection from static damage.
- Rigid, dust-free polystyrene reels provide mechanical protection and clean room compatibility for optimum equipment operation and manufacturing yield.
- Completely compatible with dereeling equipment currently available on most high-speed automated placement systems.
- Medium-density Code 39 bar coding enables inventory and manufacturing automation, as well as complete component traceability prior to, during, and after system manufacture.
- Efficient packaging offers savings in storage space and manufacturing overhead.

General Description

***SMti* Tape and Reel offers users of surface-mounted semiconductor devices a new and efficient method of component handling. Tape and reel consists of three major elements: a carrier tape, a cover tape, and a reel.**

Carrier Tape

The carrier tape is a conductive material with custom-embossed pockets for a particular surface-mount package. Components are oriented in the embossed pockets per EIA 481-A specification "Taping of Surface-Mount Components for Automatic Placement."

Cover Tape

With each component in its embossment and protected from mechanical and static damage, a continuous opaque cover tape is heat sealed over the entire length of the carrier tape, isolating each component from the outside environment. This heat-sealing process guarantees sufficient seal strength to prevent components from falling from the pockets before use. The cover tape has a peel strength of 40 $\pm$ 30 grams in compliance with EIA 481-A and sufficient strength to ensure consistency during dereeling operations.

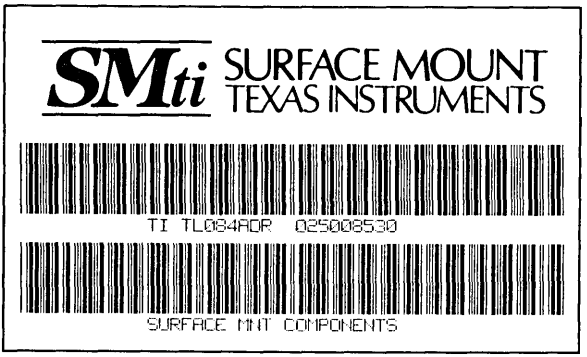
Reel

The entire assemblage is wound on a high-strength polystyrene based reel. The reel provides a means of easy storage and handling as well as a method for feeding large quantities of packages to high-speed placement systems. In addition, *SMti* Tape and Reel offers a factory-automation alternative through the use of medium-density Code 39 bar coding on all reel assemblies. The bar code provides source, part number, date code, and quantity.

Bar-Code Labeling

Each reel of *SMti* components is labeled with a "man-and-machine" readable label that uses a medium-density Code 39 bar code in combination with alphanumeric characters.

Figure 1 ***Bar-Code Label***

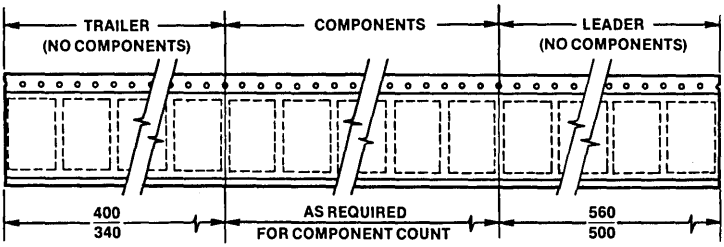


Notes

1. Sample labels are available for system compatibility testing.

SMti Tape and Reel components are available in formats that are compatible with most industry standard component loading and tape drive equipment. Figures 2 through 6 and Tables 1 through 6 provide information regarding these formats. All dimensions are given in millimeters.

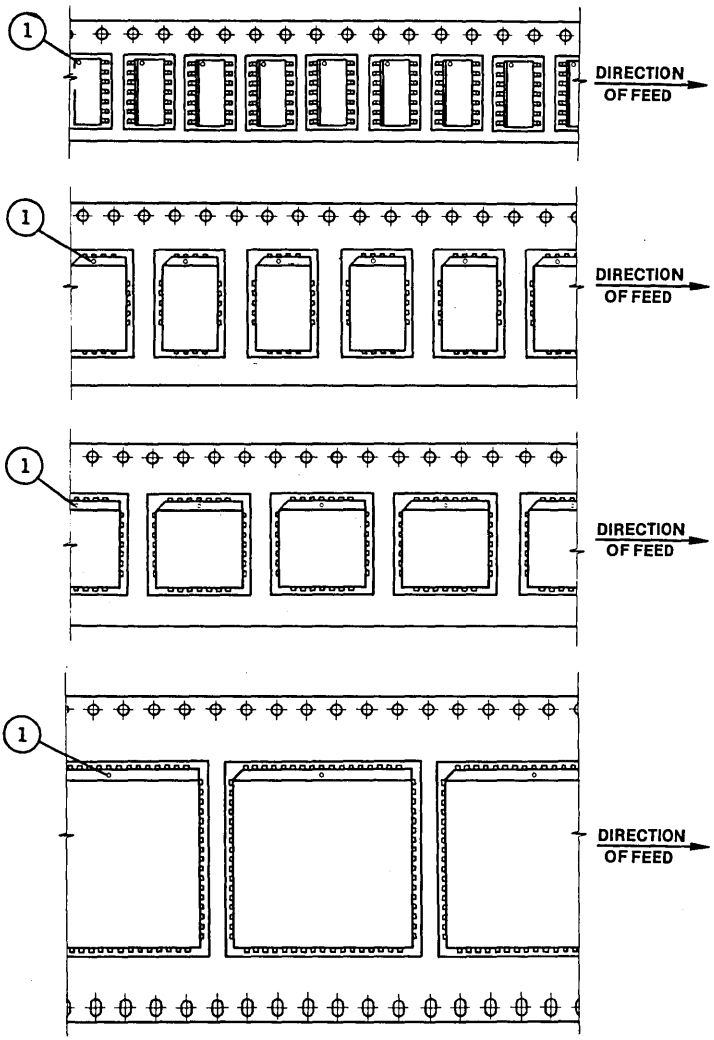
Figure 2 *Tape Format*



Notes

1. Carrier tape is conductive with a resistivity value of less than 1×10^5 ohms per square.
2. Cover tape is sealed over the entire length of the carrier tape.

Figure 3 ***Component Format*** (All components are packaged per Note 1.)

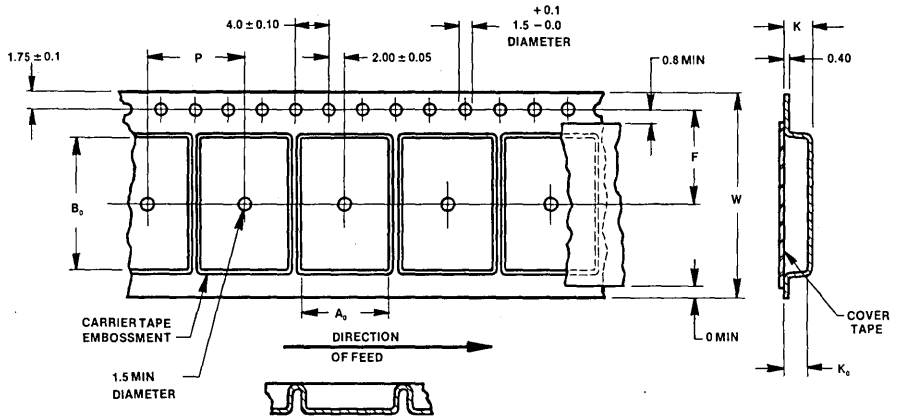


Note

1. Pin #1 orientation.

Variables are used in Figures 4 and 5 and Tables 1 and 2. The definitions for the variables are as follows: W is tape width, P is pocket pitch, A_0 is pocket width, B_0 is pocket length, K_0 is pocket depth, K is maximum tape depth, and F is the distance between the drive hole and the centerline of the pocket. All dimensions are given in millimeters.

Figure 4 ***Single-Sprocket Tape Dimensions***



Notes

1. Tape widths are 12, 16, and 24 mm.
2. Camber per EIA Standard 481-A.
3. Minimum bending radius per EIA Standard 481-A.

Variables are used in Figures 4 and 5 and Tables 1 and 2. The definitions for the variables are as follows: W is tape width, P is pocket pitch, A_0 is pocket width, B_0 is pocket length, K_0 is pocket depth, K is maximum tape depth, and F is the distance between the drive hole and the centerline of the pocket. All dimensions are given in millimeters.

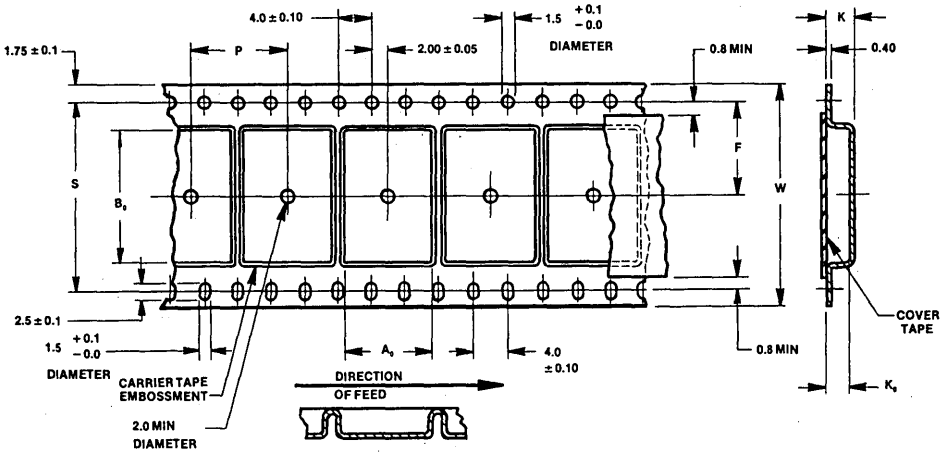
Table 1 *Single-Sprocket Variable Tape Dimensions*

Package Type	Package Designator	Dimension W	P	A_0	B_0	K_0	K	F
SO-8	D	12	8	6.4	5.2	2.1	2.5	5.5*
SO-14	D	16	8	6.5	9.5	2.1	2.5	7.5
SO-16	D	16	8	6.5	10.3	2.1	2.5	7.5
SO-16L	DW	16	12	10.9	10.7	3.0	3.4	7.5
SO-20L	DW	24	12	10.9	13.2	3.0	3.4	11.5
SO-24L	DW	24	12	10.9	15.8	3.0	3.4	11.5
SO-28L	DW	24	12	10.9	18.3	3.0	3.4	11.5
PLCC-18	FP**	24	12	8.7	12.2	3.75	4.1	11.5
PLCC-18	FM	24	12	8.7	13.9	3.75	4.1	11.5
PLCC-22	FM	24	12	8.7	13.9	3.75	4.1	11.5
PLCC-32	FM	24	16	12.9	15.5	3.75	4.1	11.5
PLCC-20	FN	16	12	10.3	10.3	4.9	5.3	7.5
PLCC-28	FN	24	16	13.0	13.0	4.9	5.3	11.5
Tolerance		±0.3	±0.1	±0.1	±0.1	±0.1	max	±0.1

*Tolerance for this part is: ±0.05.
**FP is a package designator for TMS4164 and TMS4416.

Variables are used in Figures 4 and 5 and Tables 1 and 2. The definitions for the variables are as follows: W is tape width, P is pocket pitch, A_0 is pocket width, B_0 is pocket length, K_0 is pocket depth, K is maximum tape depth, and F is the distance between the drive hole and the centerline of the pocket. All dimensions are given in millimeters.

Figure 5 ***Double-Sprocket Tape Dimensions***



Notes

1. Tape widths are 32, 44, and 56 mm.
2. Camber per EIA Standard 481-A.
3. Minimum bending radius per EIA Standard 481-A.

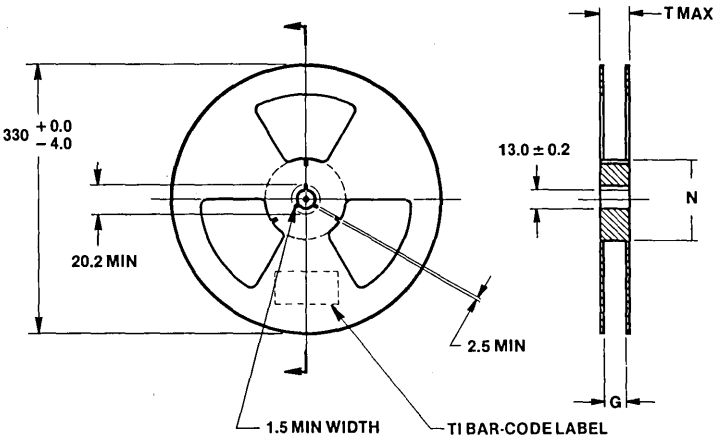
Variables are used in Figures 4 and 5 and Tables 1 and 2. The definitions for the variables are as follows: W is tape width, P is pocket pitch, A_0 is pocket width, B_0 is pocket length, K_0 is pocket depth, K is maximum tape depth, and F is the distance between the drive hole and the centerline of the pocket. All dimensions are given in millimeters.

Table 2 *Double-Sprocket Variable Tape Dimensions*

Package Type	Package Designator	Dimension W	P	A_0	B_0	K_0	K	F
PLCC-44	FN	32	24	18.0	18.0	4.9	5.3	14.2
PLCC-52	FN	32	24	20.5	20.5	5.3	5.7	14.2
PLCC-68	FN	44	32	25.6	25.6	5.3	5.7	20.2
PLCC-84	FN	44	36	30.7	30.7	5.3	5.7	20.2
PLCC-100	FN	56	40	35.8	35.8	5.3	5.7	26.2
PLCC-124	FN	56	48	43.4	43.4	5.3	5.7	26.2
Tolerance		±0.3	±0.1	±0.1	±0.1	±0.1	max	±0.1

Variables are used in Figure 6 and Table 3. The definitions for the variables are as follows: G is the distance between the flanges, T is the maximum reel width, and N is the diameter of the reel hub. All dimensions are given in millimeters.

Figure 6 *Reel Dimensions*



Variables are used in Figure 6 and Table 3. The definitions for the variables are as follows: G is the distance between the flanges, T is the maximum reel width, and N is the diameter of the reel hub. All dimensions are given in millimeters.

Table 3 ***Variable Reel Dimensions***

Package Type	Package Designator	Dimension G	T	N
SO-8	D	12.4	18.4	100
SO-14	D	16.4	22.4	100
SO-16	D	16.4	22.4	100
SO-16L	DW	16.4	22.4	100
SO-20L	DW	24.4	30.4	100
SO-24L	DW	24.4	30.4	100
SO-28L	DW	24.4	30.4	100
PLCC-18	FP*	24.4	30.4	100
PLCC-18	FM	24.4	30.4	100
PLCC-22	FM	24.4	30.4	100
PLCC-32	FM	24.4	30.4	100
PLCC-20	FN	16.4	22.4	100
PLCC-28	FN	24.4	30.4	100
PLCC-44	FN	32.4	40.4	100
PLCC-52	FN	32.4	40.4	100
PLCC-68	FN	44.4	52.4	150
PLCC-84	FN	44.4	52.4	150
PLCC-100	FN	56.4	64.4	150
PLCC-124	FN	56.4	64.4	150
Tolerance		+2.0	max	±2.0

*FP is a package designator for TMS4164 and TMS4416.

All dimensions are given in millimeters.

Table 4 ***Tape and Reel Format Summary***

Package Type	Package Designator	Tape Width	Package Pitch	Pocket Dimensions Width	Length	Depth	Reel Diameter	Reel Hub Diameter	Parts Per Reel
SO-8	D	12	8	6.4	5.2	2.1	330	100	2500
SO-14	D	16	8	6.5	9.0	2.1	330	100	2500
SO-16	D	16	8	6.5	10.3	2.1	330	100	2500
SO-16L	DW	16	12	10.9	10.7	3.0	330	100	1000
SO-20L	DW	24	12	10.9	13.2	3.0	330	100	1000
SO-24L	DW	24	12	10.9	15.8	3.0	330	100	1000
SO-28L	DW	24	12	10.9	18.3	3.0	330	100	1000
PLCC-18	FP*	24	12	8.7	12.2	3.75	330	100	1000
PLCC-18	FM	24	12	8.7	13.9	3.75	330	100	1000
PLCC-22	FM	24	12	8.7	13.9	3.75	330	100	1000
PLCC-32	FM	24	16	12.9	15.5	3.75	330	100	1000
PLCC-20	FN	16	12	10.3	10.3	4.9	330	100	1000
PLCC-28	FN	24	16	13.0	13.0	4.9	330	100	750
PLCC-44	FN	32	24	18.0	18.0	4.9	330	100	500
PLCC-52	FN	32	24	20.5	20.5	5.3	330	100	400
PLCC-68	FN	44	32	25.6	25.6	5.3	330	150	250
PLCC-84	FN	44	36	30.7	30.7	5.3	330	150	250
PLCC-100	FN	56	40	35.8	35.8	5.3	330	150	100
PLCC-124	FN	56	48	43.4	43.4	5.3	330	150	100

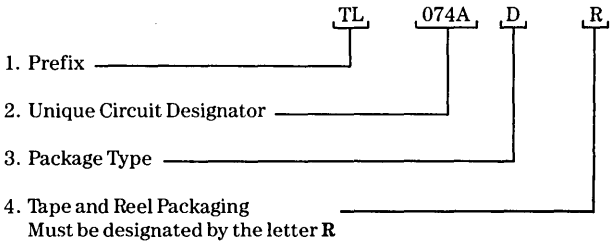
*FP is a package designator for TMS4164 and TMS4416.

Ordering Information

To order tape and reel components, you need to provide information about part numbers, quantities, shipping, and sample package applications.

Ordering by Part Number

When ordering tape and reel components, add the letter **R** as a suffix to the part number. An example of the ordering sequence follows.



Formats and Quantities

All orders for tape and reel packaging **must be for whole reels**. For example, if a customer requires 9,900 TL074's in Tape and Reel packaging, he needs to place the order for a quantity of 10,000 TL074's. The order will be filled and shipped on four reels containing 2,500 parts per reel.

Note: TI reserves the right to provide a smaller quantity of devices per reel to preserve date code integrity.

A list of package and tape formats and the quantity of devices per reel is provided in Table 5.

Shipping

Taped and reeled components are shipped in individual packing boxes measuring approximately 14″ × 14″. The depth of each box is tailored to the tape width. Individual boxes are packed in a larger box whose size depends on the quantity of components ordered.

All dimensions are given in millimeters.

Table 5 *Condensed Tape and Reel Formats*

Package Type	Package Designator	Tape Width	Package Pitch	Reel Diameter	Parts Per Reel
SO-8	D	12	8	330	2500
SO-14	D	16	8	330	2500
SO-16	D	16	8	330	2500
SO-16L	DW	16	12	330	1000
SO-20L	DW	24	12	330	1000
SO-24L	DW	24	12	330	1000
SO-28L	DW	24	12	330	1000
PLCC-18	FP*	24	12	330	1000
PLCC-18	FM	24	12	330	1000
PLCC-22	FM	24	12	330	1000
PLCC-32	FM	24	16	330	1000
PLCC-20	FN	16	12	330	1000
PLCC-28	FN	24	16	330	750
PLCC-44	FN	32	24	330	500
PLCC-52	FN	32	24	330	400
PLCC-68	FN	44	32	330	250
PLCC-84	FN	44	36	330	250
PLCC-100	FN	56	40	330	100
PLCC-124	FN	56	48	330	100

*FP is a package designator for TMS4164 and TMS4416.

Sample Package Applications

Sample components are available for a number of applications, such as standard mechanical sample packages, "daisy-chained" bars, and K-factor bars. Table 6 provides sample ordering information.

Table 6 ***Sample Package Applications***

Package Type	Package Designator	Mechanical Sample	Daisy Chain	K Factor
SO-8	D	SN102589	SN102590	N/A
SO-14	D	SN72197	SN200054	SN200060
SO-16	D	SN72198	SN200055	SN200061
SO-16L	DW	N/A	N/A	N/A
SO-20L	DW	SN72199	SN200056	SN200062
SO-24L	DW	SN72200	SN200057	SN200063
SO-28L	DW	N/A	N/A	N/A
PLCC-18	*	TMS1864MS	TMS1864DC	TMS1864KF
PLCC-18	*	TMS18256MS	TMS18256DC	TMS18256KF
PLCC-22	*	TMS22464MS	TMS22464DC	TMS22464KF
PLCC-32	FM	N/A	N/A	N/A
PLCC-20	FN	SN72201	SN200058	N/A
PLCC-28	FN	SN72202	SN200059	N/A
PLCC-44	FN	SN102767	SN102768	N/A
PLCC-52	FN	N/A	N/A	N/A
PLCC-68	FN	SN750002	SN750003	N/A
PLCC-84	FN	N/A	N/A	N/A
PLCC-100	FN	N/A	N/A	N/A
PLCC-124	FN	N/A	N/A	N/A

*The type of package is indicated by MS, DC, or KF at the end of the part number.

More Information

As a major manufacturer of SMCs, TI is committed to helping you make the transition to surface-mount as easy and as economical as possible. Getting started in SMT—switching from older and less efficient methods of PCB fabrication—means learning some new manufacturing techniques, and it entails some capital outlay. But in volume production it can actually reduce your capital and space costs by up to 50 percent.

Ship-to-Stock Eliminates Incoming Inspection

As your usage per surface-mount component (SMC) grows, TI can implement its ship-to stock program for you. With all the necessary quality-control procedures built into our standard testing process, your SMCs can be shipped directly to you in tape and reel or in factory-sealed boxes. Benefits to you:

- Incoming inspection, scrap, and rework reduced or eliminated.
- Inventory reduced.
- Quality levels maximized.

Learn by Doing

To help you realize the advantages of surface-mount technology (SMT), Texas Instruments maintains a surface-mount laboratory. There you can gain hands-on experience and guidance in building a surface-mount board from start to finish. To schedule an appointment, contact your TI Field Sales Engineer. Or call (800) 232-3200 for the address of the TI Field Sales Office nearest you. A description of the lab's equipment and services is available from TI (**see reply card**).

Outside Help Available

You can also find assistance among the growing number of SMT assembly houses, consultants, and associations. They can help you reduce the costs of converting to SMT, while supplying some valuable information on the latest technological advances and industry standards.

Suppliers of assembly equipment such as pick-and-place machines and soldering and test equipment can also help you make the transition to SMT board fabrication. A current list of these suppliers is available from TI (**see reply card**).

Want to Learn More?

How to Use Surface Mount Technology is available free of charge from Texas Instruments (**see reply card**). This technical summary includes chapters on the process and the tooling required to implement it; the wide variety of available SMCs; inspection, testing, and repair; quality and reliability; and how to mix SMCs with standard DIP packages.

For additional information on the availability of TI's growing line of SMCs, contact your local TI Field Sales Office or distributor.

If you would like to have your name placed on our mailing list for additional SMT information as it becomes available from TI, please complete and return the enclosed reply card, or write Texas Instruments Incorporated, Dept. SSP05, P.O. Box 809066, Dallas, Texas 75380-9066.

General Information 1

NuBus™ Device Data Sheets 2

Application Reports 3

Explanation of Logic Symbols 4

Mechanical Data 5

ESD Guidelines 6

Guidelines for Handling Electrostatic-Discharge Sensitive (ESDS) Devices and Assemblies

SCOPE

This specification establishes the requirements for methods and materials used to protect electronic parts, devices, and assemblies (items) susceptible to damage or degradation from electrostatic discharge (ESD). The electrostatic charges referred to in this specification are generated and stored on surfaces of ordinary plastics, most common textile garments, ungrounded people's bodies, and many other commonly unnoticed static generators. The passage of these charges through an electrostatic-sensitive part may result in catastrophic failure or performance degradation of the part.

The part types for which these requirements are applicable include, but are not limited to the following:

1) All discrete semiconductors and ICs
2) Hybrid microcircuits
3) Thin film passive devices.

Definitions

1. Antistatic material: ESD protective material which minimizes the generation of static charges when rubbed against or separated from itself or other similar materials.
2. Static dissipative material: ESD protective material having surface resistivity between 10^5 and 10^{12} Ω/square.
3. Conductive material: ESD protective material having a surface resistivity of 10^5 Ω/square maximum.
4. Electrostatic discharge (ESD): A transfer of electrostatic charge between bodies at different electrostatic potentials caused by direct contact or induced by an electrostatic field.
5. Surface resistivity: An inverse measure of the conductivity of a material and is the resistance of unit length and unit width of a surface. Note: Surface resistivity of a material is numerically equal to the surface resistance between two electrodes forming opposite sides of a square. The size of the square is immaterial. Surface resistivity applies to both surface and volume conductive materials and has the dimension of Ω/square.
6. Volume resistivity: Also referred to as bulk resistivity. It is normally determined by measuring the resistance (R) of a square of material (surface resistivity) and multiplying this value by the thickness (T).
7. Ionizer: Equipment that generates positive and negative ions, either by electrostatic means or by means of a radioactive energy source, in an airstream, and distributes a layer of low velocity ionized air over a work area to neutralize static charges.
8. Close proximity: For the purpose of this specification, is 6 inches or less.

Device Sensitivity per Test Circuit of Method 3015, MIL-STD-883

1. For the purpose of this specification, all microelectronic devices are considered to be ESDS Class 1. ESDS Class 1 devices require minimum protective packaging of a conductive container or an antistatic container within an electrostatic field shielding barrier.
2. Devices are to be protected from ESD damage from receipt at incoming inspection through assembly, test and shipment of completed equipment.

APPLICABLE REFERENCE DOCUMENTS

The following reference documents (of latest issue) can provide additional information on ESD controls:

1) MIL-M-38510 Microcircuits, General Specification
2) MIL-STD-883 Test Methods and Procedures for Microelectronics
3) MIL-S-19491 Semiconductor Devices, Packaging of
4) MIL-M-55565 Microcircuits, Packaging of

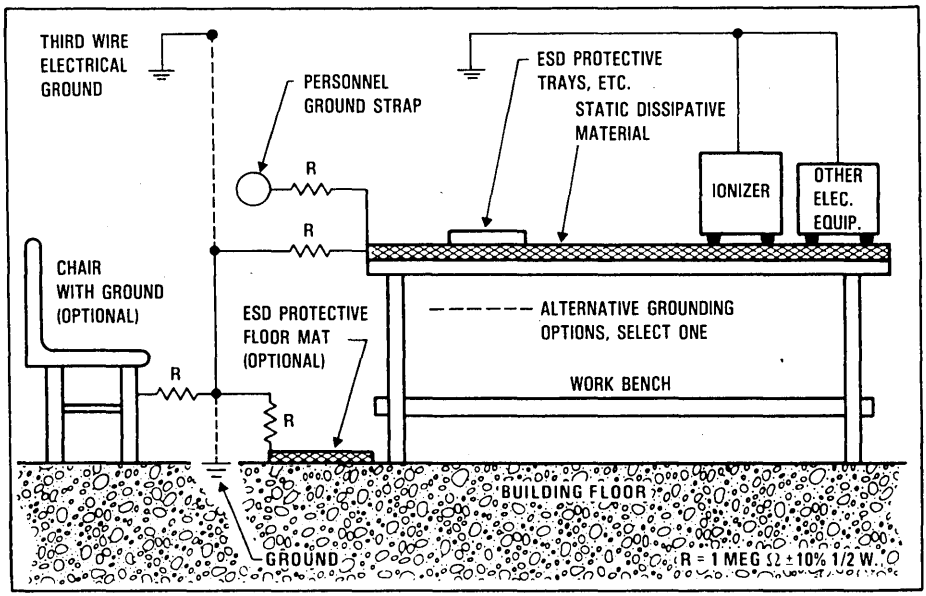
5) DOD-HDBK-263 Electrostatic Discharge Control Handbook for Protection
6) DOD-STD-1686 Electrostatic Discharge Control Program
7) NAVSEA SE 003-11-TRN-010 Electrostatic Discharge Training Manual
8) EIA-541 Packaging Material Standards for ESD Sensitive Items

FACILITIES FOR STATIC-FREE WORK STATION

The minimum acceptable static-free work station shall consist of the work surface covered with static dissipative material attached to ground through a 1 MΩ ±10% resistor, an attached grounding wrist strap with integral 1 MΩ ±10% resistor for each operator, and air ionizer(s) of sufficient capacity for each operator. If no insulator materials are present at the work station, operators may wear static dissipative smocks in lieu of using an ionizer. The wrist strap shall be connected to the static dissipative material at the same metallic button or contact used to ground the material. Ground must utilize either earth ground or third wire (green) electrical ground, refer to Figure 1. Conductive floor tile along with conductive shoes may be used in lieu of the conductive wrist straps for nonseated personnel. The Site Safety Engineer must review and approve all electrical connections at the static-free work station prior to its implementation.

Air ionizers shall be positioned so that the devices at the static-free work stations are within a 4-foot arc measured by a vertical line from the face of the ionizer and 45 degrees on each side of this line.

General grounding requirements are to be in accordance with Table 1.



All electrical equipment sitting on the static dissipative work surface must be hard grounded using a ground strap but must be isolated from the static dissipative work surface.

NOTE: Earth ground consists of a metal pipe or rod inserted at least three (3) feet into the earth.

Figure 1. Static-Free Work Station

Table 1. General Grounding Requirements

	ANTISTATIC, STATIC DISSIPATIVE OR CONDUCTIVE MATERIAL	GROUNDED TO COMMON POINT
Handling Eqipment/Handtools	X	
Metal Parts of Fixtures and Tools/Storage Racks		X
Handling Trays/Tubs	X	
Soldering Irons/Bath		X
Table Tops/Floor Mats	X	X
Personnel		X Using Wrist Strap*

*With 1 MΩ ± 10% resistor.

Usage of Antistatic Solution in Areas to Control the Generation of Static Charges

The use of antistatic chemicals (antistats) should be a supplemental part of an overall organized ESD program. Any antistatic chemical application shall be considered as a means to reduce or eliminate static charge generation on nonconductive materials in the manufacturing or storage areas.

The application of any antistatic chemical in a clean room of class 10,000 or less shall not be permitted. Accordingly, any user of antistatic solutions must consider the following precautions:

1. Do not apply antistatic spray or solutions in any form to energized electrical parts, assemblies, panels, or equipment.
2. Do not perform antistatic chemical applications in any area when bare chips, raw parts, packages, and/or personnel are exposed to spray mists and evaporation vapors.

The need for initial application and frequency of reapplication can only be established through routine electrostatic voltage measurements using an electrostatic voltmeter. The following durability schedule is a reasonable expectation:

1) Soft surfaces (carpet, fabric seats, foam padding, etc.): each 6 months or after cleaning, by spraying.
2) Hard abused surfaces (floors, table tops, tools, etc.): each week (or day for heavy use) and after cleaning, by wiping or mopping.
3) Hard unabused surfaces (cabinets, walls, fixtures, etc.): each 6 months or annually and after cleaning, by wiping or spraying.
4) Company-furnished and maintained clothing and smocks: after each cleaning, by spraying or adding antistatic concentrate to final rinse water when cleaned.

The use of antistatic chemicals, their application, and compliance with all appropriate specifications, precautions, and requirements shall be the responsibility of the Area Supervisor where antistatic chemicals are used.

ESD Labels and Signs in Work Areas

ESD caution signs at work stations and labels on static-sensitive parts and containers shall be consistent in color, symbols, class, voltage sensitivity identification, and appropriate instructions. Signs shall be posted at all work stations performing any handling operations with static-sensitive items. These signs shall contain the following information or its equivalent.

CAUTION

STATIC CAN DAMAGE COMPONENTS

Do not handle ESDS items unless grounding wrist strap is properly worn and grounded. Do not let clothing or plain plastic materials contact or come in close proximity to ESDS items.

Labels shall be affixed to all containers containing static-sensitive items at a place readily visible and proper for the intended purpose. Additionally, labels must be consistently placed on containers and packages at a standard location to eliminate mishandling. Use only QC accepted and approved signs and labels to identify static-sensitive products and work areas. The use of ESD signs and labels, and their information content shall be the responsibility of the Area Supervisor to assure consistency and compatibility throughout the static-sensitive routing.

Relative Humidity Control

Since relative humidity has a significant impact on the generation of static electricity, when possible, the work area should be maintained within the following relative humidity ranges: incoming/assembly/test/storage 40%-60%.

PREPARATION FOR WORKING AT STATIC-FREE WORK STATION

A work station with a static dissipative work surface connected to ground through a 1 MΩ ±10% resistor, a grounding wrist strap with the ground wire connected to the static dissipative work surface, and an ionizer constitute a static-free work station (Figure 1). An operator is properly grounded when the wrist strap is in snug (no slack) contact with the bare skin, usually positioned on the left wrist for a right-handed operator. The wrist strap must be worn the entire time an operator is at a static-free work station. If possible, operators should avoid touching leads or contacts even though grounded.

> **CAUTION**
>
> Personnel shall never be attached to ground without the presence of the 1 MΩ ±10% series resistor in the ground wire.

An operator's clothing should never make contact or come in close proximity with static-sensitive items. They must be especially careful to prevent any static-sensitive items (being handled) from touching their clothing. Long sleeves must be rolled up or covered with antistatic sleeve protector banded to the bare wrist which shall "cage" the sleeve at least as far up as the elbow. Only antistatic finger cots, cotton gloves, antistatic gloves or conductive gloves (free of reactive elements such as chlorine, phosphorus, etc.) may be used when handling static-sensitive items.

Any person not properly prepared, while at or near the work station, shall not touch or come in close proximity with any static-sensitive items. It is the responsibility of the operator and the Area Supervisor to ensure that the static-free work area is clear of unnecessary static hazards, including such personal items as plastic coated cups or wrappers, plastic cosmetic bottles or boxes, combs, tissue boxes, cigarette packages, and vinyl or plastic purses. All work-related items, including information sheets, fluid containers, tools, and parts carriers must be those approved for use at the static-free work station.

GENERAL HANDLING PROCEDURES AND REQUIREMENTS

1. All static-sensitive items must be received in an antistatic/conductive container and must not be removed from the container except at static-free work station. All protective folders or envelopes holding documentation (lot travelers, etc.) shall be made of nonstatic-generating material.
2. Each packing (outermost) container and package (internal or intermediate) shall have a warning label attached, stating the following information or equivalent:

   The warning label shall be legible and easily readable to normal vision at a distance of 3 feet.
3. Static-sensitive items are to remain in their protective containers except when actually in work at the static-free station.
4. Before removing the items from their protective container, the operator should place the container on the static dissipative bench top and make sure the wrist strap fits snugly around the wrist and is properly plugged into the ground receptacle.
5. All operations on the items should be performed with the items in contact with the static dissipative bench top as much as possible. Do not allow conductive magazine to touch hard grounded test gear on bench top.
6. Ordinary plastic solder-suckers and other plastic assembly aids shall not be used.
7. In cases where it is impossible or impractical to ground the operator with a wrist strap, a conductive shoe/heel strap may be used along with conductive tile/mats.

8. When the operator moves from any other place to the static-free station, the start-up procedure shall be the same as in PREPARATION FOR WORKING AT STATIC-FREE WORK STATION.
9. The ionizer shall be in operation prior to presenting any static-sensitive items to the static-free station, and shall be in operation during the entire time period the items are at the station. (See exception in FACILITIES FOR STATIC-FREE WORK STATION.)
10. "Plastic snow" polystyrene foam, "peanuts," or other high-dielectric materials shall never come in contact with or be used around electrostatic sensitive items, unless they have been treated with an antistat (as evidenced by pink color and generation of less than ± 100 volts).
11. Static-sensitive items shall not be transported or stored in trays, tote boxes, vials, or similar containers made of untreated plastic material unless items are protectively packaged in conductive material.

PACKAGING REQUIREMENTS

Packaging of static-sensitive items is to be in accordance with Device Sensitivity, item 1). The use of tape and plain plastic bags are prohibited. All outer and inner containers are to be marked as outlined in GENERAL HANDLING PROCEDURES AND REQUIREMENTS, item 2, and conductive magazines/boxes may be used in lieu of conductive bags.

SPECIFIC HANDLING PROCEDURES FOR STATIC-SENSITIVE ITEMS

Stockroom Operations

1. Containers of static-sensitive items are not to be accepted into stock unless adequately identified as containing static-sensitive items.
2. Items may be removed from the protective container (magazine/bag, etc.) for the purpose of subdividing for order issue only be a properly grounded operator at an approved static-free station as defined in FACILITIES FOR and PREPARATIONS FOR WORKING AT STATIC-FREE WORK STATIONS.
3. All subdivided lots must be carefully repackaged in protective containers (magazine/bag, etc.) prior to removal from the static-free work station and labeled to indicate that the package(s) contain static-sensitive items. If it is suspected that a static-sensitive item is not adequately protected, do not transfer it to another container, return it to the originator for disposition unless the originator is a Customer. In that case, the QC Engineer should contact the Customer and negotiate an appropriate disposition.
4. It is the responsibility of the Stockroom Supervisor to ensure that all personnel assigned to this operation are familiar with handling procedures as outlined in this specification. A copy of this specification is to be posted in the vicinity so that it is accessible to the operators. Stock handlers and all others who might have occasion to move stock are to be instructed to avoid direct contact with unprotected static-sensitive items.

Module and Subassembly Operations

1. Static-sensitive items are not to be received from a stockroom, kitting, or machine insertion area unless received in approved static-protective packaging, and properly labeled to indicate that its contents are static sensitive.
2. All single station, progressive line manual assembly operators, and visual inspectors prior to wave soldering operations are to be properly grounded with a grounding wrist strap when handling static-sensitive items.
3. Progressive lines used as single stations where operators will be working on a mix of boards, both static-sensitive and nonstatic-sensitive, will require that all operators working on the line be properly grounded. This is necessary to accommodate the sliding of static-sensitive boards along the assembly bench or across positions not engaged in the assembly of this type board.
4. It is the responsibility of the Area Supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding wrist straps properly (snugly in contact with bare skin).

Soldering and Lead-Forming Operations

1. All soldering machines, conveyors, cleaning machines, and equipment shall be electrically grounded to ensure that they are at the same ground potential as the grounded operators working on their stations. No machine surfaces exposed to static-sensitive items are to be above the ground potential.
2. All processing equipment shall be grounded, including all loading and unloading stations, that is, the stations before and after each piece of processing equipment.

3. All nonmetallic, static-generating components in the handling systems shall be treated to ensure protection from static.
4. All stations shall be identified by posting signs as outlined in **ESD Labels and Signs in Work Areas**.
5. Operators are to be properly grounded with a grounding wrist strap during any handling, loading, unloading, inspection, rework, or proximity to static-sensitive items.
6. Unloading operators working at a grounded station shall place static-sensitive items into approved static-protective bags or containers.
7. All manual soldering, repair, and touch-up work stations on the solder line are to be static protected. Operators are to wear grounding wrist straps when working on static-sensitive items. Only grounded-tip soldering/desoldering irons are allowed when working on static-sensitive items.
8. It is the responsibility of the Area Supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding wrist straps properly (comfortably snug in contact with bare skin).

Electrical Testing Operations

1. All electrical test stations shall be static protected. Operators shall be properly grounded when working on these items.
2. Reused antistatic magazines must be monitored for maintenance of antistatic characteristics.
3. Devices should be in an antistatic/conductive environment except at the moment when actually under test.
4. Devices should not be inserted into or removed from circuits or tester with the power on or with signals applied to inputs to prevent transient voltages from causing permanent damage.
5. All unused input leads should be biased if possible.
6. Device or module repairs must be performed at static-free stations with the operator attached to a grounding wrist strap. Grounded-tip soldering irons shall be used when working on static-sensitive items.
7. Static-sensitive items shall be handled through all electrical inspections in static protective containers. Removal of the items from the protective containers shall be done at a static-free work station as discussed in **PREPARATION FOR WORKING AT A STATIC-FREE WORK STATION**. The units must be returned to the containers before leaving the station.
8. All such items shall be shipped with an ESD warning label affixed as listed.
9. It is the responsibility of the Area Supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or possible degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding straps properly (snugly in contact with bare skin).

Packing Operations

1. Static-sensitive items are not to be accepted into the packing area unless they are contained in a static-protected bag or conductive container.
2. A static-sensitive item delivered to the packer within an approved container or bag and found to be in order regarding identification shall be packed in the standard shipping carton or other regular packaging material. Containers are to be labeled in accordance with **GENERAL HANDLING PROCEDURES AND REQUIREMENTS**, item 2.
3. Any void-fillers shall be made of an antistatic material.

Burn-In Operations

1. Burn-in board loading and unloading of static-sensitive items shall be done at a static-free station.
2. Shorting clips/shorted connectors shall be installed on the board plug-in tab prior to loading any units into the board sockets. The clip/connector shall be taken off just prior to plugging the board into the oven connector. The clip/connector shall be installed immediately upon removal of the board from the oven connector. Installation and removal of the clip/connector shall be done by a properly grounded operator.
3. All automatic or semiautomatic loading and unloading equipment shall be properly electrically grounded.
4. It is the responsibility of the Area Supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or possible degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding straps properly (snugly in contact with bare skin).

CUSTOMER RETURNED ITEM HANDLING PROCEDURE

Receipt of ESDS-labeled items is to be done at a static-free work station and handled in accordance with applicable sections within this guideline.

QUALITY CONTROL PROVISIONS

Sampling

Each manufacturing, stockroom, and testing operation handling ESDS devices will be audited a minimum of once each quarter for compliance with all terms of this specification by the responsible process control or QRA organization. Ground continuity and the presence of uncontrolled static voltages are considered critical and shall be checked more frequently as specified below.

Wrist Straps (once a day)

Wrist straps shall be checked for minimum resistance to provide operator safety and maximum resistance to insure that proper body contact is maintained to drain generated charges. A go-no-go tester may be used provided it checks to a minimum of no less than 500 kΩ and a maximum of no greater than 2 MΩ.

Ground Continuity (minimum of once a month)

Ground connections (grounding wrist strap, ground wires on cords, etc.) shall be checked for electrical continuity. The presence of a 1 MΩ $\pm 10\%$ resistor in the ground connections between both the operator wrist straps to the work surface and the work surface to ground connector must be verified.

Grounded Conditions (minimum of once a week)

A visual inspection shall be made to determine full compliance with this specification at static-free work stations during handling of static-sensitive items, including operator being grounded as required, static-sensitive items not being handled in unprotected or unauthorized areas, and no static-generating materials at the grounded work station.

Sleeve Protectors (minimum of once a week)

A visual check shall be made to determine that each operator wearing loose-fitting or long-sleeved clothing either has sleeves properly rolled or covered with sleeve protectors properly grounded to the bare skin at the wrist.

Static Voltage Levels (minimum of once a week)

In addition to the visual inspections, a sample inspection using an electrostatic voltmeter will be used to check for uncontrolled electrostatic voltages at or near electrostatic-controlled work stations.

Conductive Floor Tiles (minimum of once a month)

Conductive floors must have a resistance of not less than 100 kΩ from any point on the tile to earth ground. Also, resistance from any point-to-point on the tile floor 3 feet apart shall be not less than 100 kΩ. The test methods to be used are ASTM-F-150-72 and NFPA 99.

Records

Written records must be kept of all these QC audits.

TRAINING

Training is applicable for all areas where individuals come in contact with ESDS (Class 1) devices. It is the responsibility of each Area Supervisor to make sure that his/her people receive ESD training initially and every 12 months thereafter to maintain proficiency. Training should include static fundamentals, a review of applicable parts of this specification, and actual applications in the work area.

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