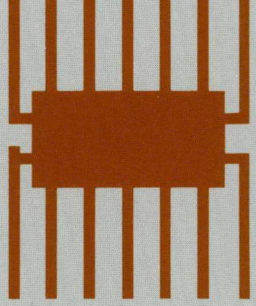


Digital Semiconductor Integrated Circuits

BULLETIN
SCA-1000

Contents

TEXAS INSTRUMENTS
INCORPORATED
13500 N. CENTRAL EXPRESSWAY
P. O. BOX 5012 • DALLAS 22, TEXAS

Products included in this bulletin are manufactured under one or more of the following U.S. Patents: 3,072,832; 3,115,581; 3,138,721; 3,138,743; 3,138,744; 3,138,747

SOLID CIRCUIT® digital semiconductor networks

SOLID CIRCUIT semiconductor networks are complete electronic circuits fabricated within monolithic bars of silicon, using diffusion techniques to form transistor, diode, resistor, and capacitor elements. Up to 85 elements are available in a single network bar. The elements needed for a particular circuit are interconnected by depositing a metallic lead pattern over the oxide-protected surface of the bar, making contact only where "windows" are left in the oxide.

Advantages of using TI integrated circuits include lower system cost, improved system reliability, and reduced size, weight, and power consumption. These benefits have been proved in hundreds of equipment applications ranging from the deep-space probe of NASA's IMP-A satellite to NAA/Autonetics' high-volume Minuteman II guidance system to Zenith's Micro-Lithic* hearing aid.

TI pioneered integrated-circuit technology, filing basic patents in the field as early as 1959. These patents were assigned to TI in 1964. Today, TI offers you the broadest line of semiconductor integrated circuits in the industry — more than 70 digital, linear and memory networks.

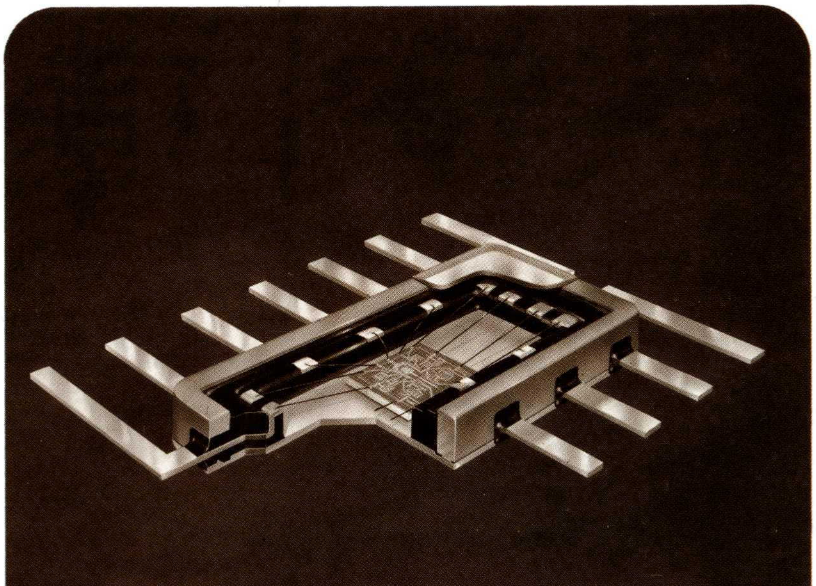
Special circuits for your particular application can be custom designed by TI's large and experienced engineering staff. TI has demonstrated competence in all the various logic configurations — TTL, DTL, RCTL, RTL, ECL, and DCTL — and presently uses all the different types of silicon planar structures:

- Triple diffused
- Quadruple diffused (NPN and PNP in same substrate)
- Single epitaxial
- Double epitaxial

With this broad technical capability, TI can provide the optimum combination of logic, structure and package to solve your design problem. Large, advanced manufacturing facilities are available to handle anything from prototype to high-volume requirements.

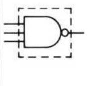
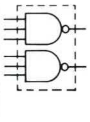
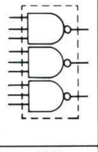
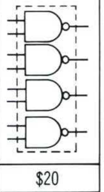
For additional information on any of the networks included in this bulletin, or for information on special circuits, contact your local TI Sales Engineer. His address and telephone number are listed inside the back cover. Most networks are available off-the-shelf from your local TI distributor.

**Zenith trademark*

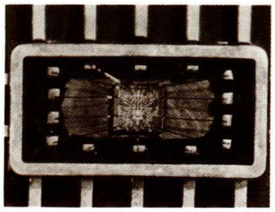


Cutaway view shows advanced construction features of SOLID CIRCUIT semiconductor networks

MULTI-FUNCTION APPROACH REDUCES SYSTEM COST, IMPROVES RELIABILITY

Network Package Content	Single Gate	Dual Gate	Triple Gate	Quad Gate
				
Value to User	$5	$10	$15	$20
Relative Network Manufacturing Cost	1.0	1.1	1.2	1.2
Cost per Circuit Function to User	$10	$5.50	**$4.00**	**$3.00**

TI's multi-function approach to network design and fabrication is extensively used in the digital families. Since several circuits can now be built simultaneously in a single bar with only a nominal cost increase over that required to build one circuit, the cost-per-circuit-function can be reduced by a substantial percentage — up to 70 percent in some cases. Other multi-function advantages include fewer packages to handle, fewer external interconnections, fewer circuit boards, and less back-panel wiring—plus significantly improved system reliability.



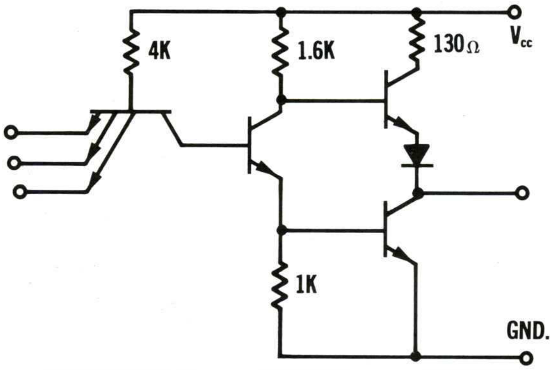
- High speed, low power dissipation
- High noise margin, high fan-out
- Excellent capacitance-driving capability
- Gold-to-gold contact system
- Multiple circuit functions per package
- Standard welded flat package

NEW—Series 54 TTL digital SOLID CIRCUIT

TYPICAL CHARACTERISTICS

Parameter	Basic Gate	Flip-flop
Propagation delay	15 nsec	40 nsec
Power dissipation	10 mw/gate	60 mw
Fan-out	10	10
D-c noise margin	1 v	1 v
Supply voltage	4.5 to 5.5 v	4.5 to 5.5 v
Temperature range	–55 to +125°C	–55 to +125°C

Typical circuit diagram for Series 54 Positive NAND gate



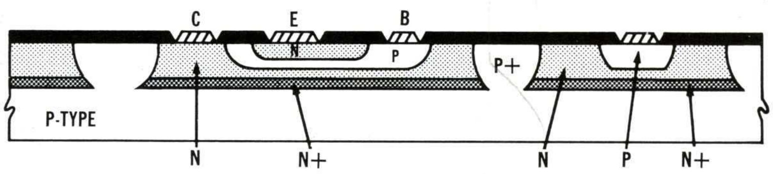
TTL logic fully exploits the inherent capabilities of integrated semiconductor structures. The use of additional transistors and multiple-emitter structures provides performance parameters that are virtually independent of temperature and loading.

High speed/low power operation is obtained by using very small transistor geometries (¼-mil emitters). Speed-limiting parasitic capacitances are minimized — both by high-resolution photo-masking techniques which permit reduced resistor areas, and by the double-epitaxial structure which provides low saturation resistance, $r_{CE(sat)}$, and thus smaller element geometries.

High noise margin for ground-line and signal-line noise is provided by strong overdrive to the output transistor and by the large V_{BE} drops obtained with small-geometry transistors.

Low noise susceptibility for capacitively coupled noise is provided by the low line-termination impedance in both the ON (12 ohms) and OFF (100 ohms) logic conditions.

Large-capacitance loads are driven at high speeds by the low output impedance of each circuit. Waveform integrity is preserved for capacitance loads of several hundred picofarads.

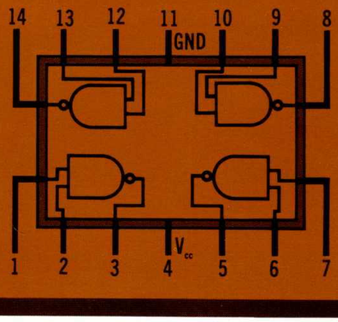


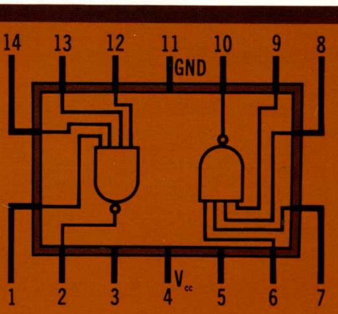
Diffused-planar, double-epitaxial structure used for Series 54 networks

SN5400

Quadruple 2-input Positive NAND Gate

Propagation delay — 13 nsec
Fan-out — 10 per gate
Power dissipation — 10 mw per gate





Dual 4-input Positive NAND "Power" Gate

Propagation delay—17.5 nsec
Fan-out — 30 per gate
Power dissipation — 10 mw per gate

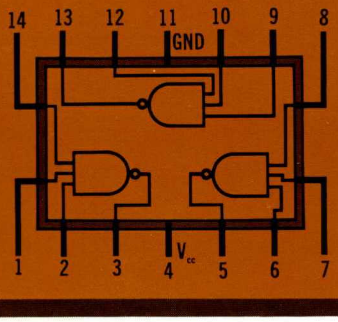
SN5440

semiconductor networks

SN5410

Triple 3-input
Positive NAND Gate

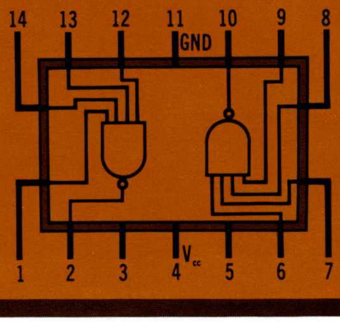
Propagation delay — 13 nsec
Fan-out — 10 per gate
Power dissipation — 10 mw
per gate



SN5420

Dual 4-input
Positive NAND Gate

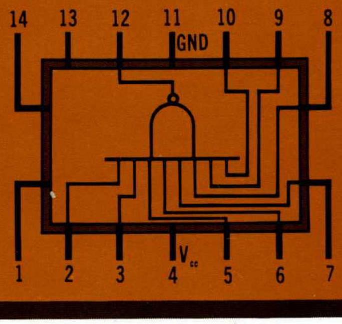
Propagation delay — 13 nsec
Fan-out — 10 per gate
Power dissipation — 10 mw
per gate

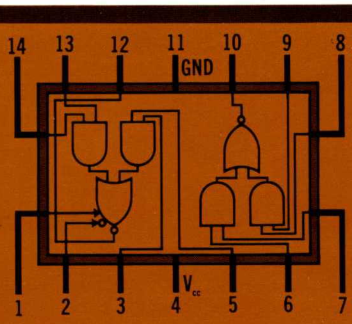


SN5430

8-input
Positive NAND Gate

Propagation delay — 15 nsec
Fan-out — 10
Power dissipation — 10 mw

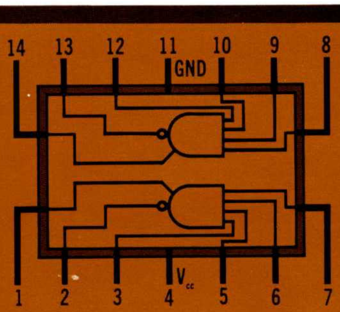




Dual EXCLUSIVE-OR Gate
with Expander Inputs

Propagation delay — 15 nsec
Fan-out — 10 per gate
Power dissipation — 10 mw
per gate

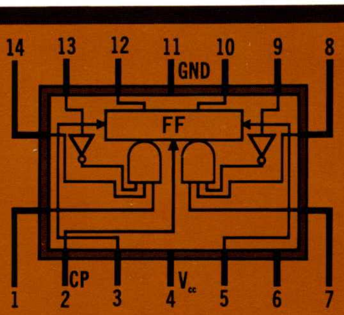
SN5450



Dual 4-input
Expander for SN5450

Fan-out (max number of
expanders connected to
SN5450) — 4
Power dissipation — 5 mw
per expander

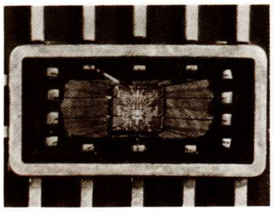
SN5460



Single-phase J-K Flip-flop

Propagation delay — 40 nsec
Fan-out — 10
Power dissipation — 65 mw

SN5470



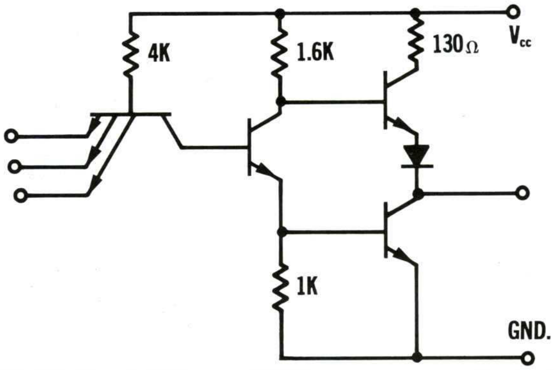
- High speed, low power dissipation
- High noise margin, high fan-out
- Excellent capacitance-driving capability
- Gold-to-gold contact system
- Multiple circuit functions per package
- Standard welded flat package

NEW—Series 54 TTL digital SOLID CIRCUIT

TYPICAL CHARACTERISTICS

Parameter	Basic Gate	Flip-flop
Propagation delay	15 nsec	40 nsec
Power dissipation	10 mw/gate	60 mw
Fan-out	10	10
D-c noise margin	1 v	1 v
Supply voltage	4.5 to 5.5 v	4.5 to 5.5 v
Temperature range	–55 to +125°C	–55 to +125°C

Typical circuit diagram for Series 54 Positive NAND gate



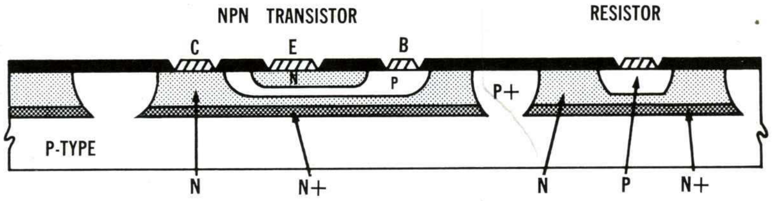
TTL logic fully exploits the inherent capabilities of integrated semiconductor structures. The use of additional transistors and multiple-emitter structures provides performance parameters that are virtually independent of temperature and loading.

High speed/low power operation is obtained by using very small transistor geometries (¼-mil emitters). Speed-limiting parasitic capacitances are minimized — both by high-resolution photo-masking techniques which permit reduced resistor areas, and by the double-epitaxial structure which provides low saturation resistance, $r_{CE(sat)}$, and thus smaller element geometries.

High noise margin for ground-line and signal-line noise is provided by strong overdrive to the output transistor and by the large V_{BE} drops obtained with small-geometry transistors.

Low noise susceptibility for capacitively coupled noise is provided by the low line-termination impedance in both the ON (12 ohms) and OFF (100 ohms) logic conditions.

Large-capacitance loads are driven at high speeds by the low output impedance of each circuit. Waveform integrity is preserved for capacitance loads of several hundred picofarads.

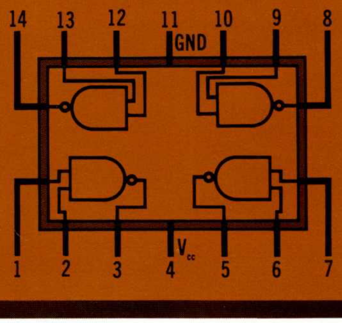


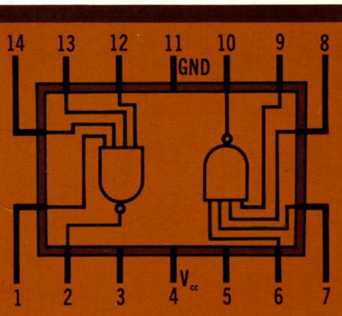
Diffused-planar, double-epitaxial structure used for Series 54 networks

SN5400

Quadruple 2-input Positive NAND Gate

Propagation delay — 13 nsec
Fan-out — 10 per gate
Power dissipation — 10 mw per gate

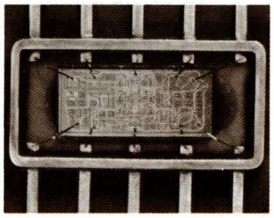




Dual 4-input Positive NAND "Power" Gate

Propagation delay—17.5 nsec
Fan-out — 30 per gate
Power dissipation — 10 mw per gate

SN5440

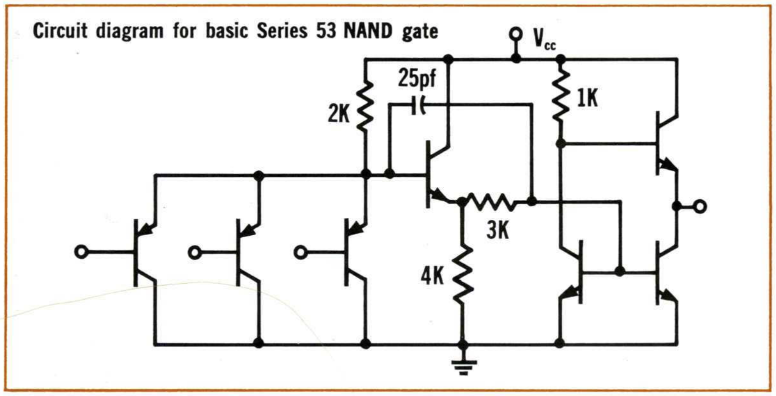


- Multiple circuit functions per package
- Highly flexible AND/OR/INVERT logic configuration
- High fan-out
- Medium speed, medium power dissipation
- Standard welded flat package
- For general-purpose digital applications

Series 53 Modified-DTL digital SOLID CIRCUIT

TYPICAL CHARACTERISTICS

Parameter	Basic AND Gate	Basic NAND Gate	Flip-flop
Propagation delay	5 nsec	25 nsec	45 nsec
Power dissipation	10 mw	10 mw	27 mw
D-c noise margin	200 mv	200 mv	200 mv
Fan-out	4	10	10
Supply voltage	3 to 4 v	3 to 4 v	3 to 4 v
Temperature range	–55 to +125°C	–55 to +125°C	–55 to +125°C


Circuit diagram for basic Series 53 NAND gate

Multi-function networks. Each Series 53 bar contains between 50 and 85 elements — making it possible to provide quadruple gate and inverter networks, dual EXCLUSIVE-OR networks, or two complete J-K flip-flops in a single network package. This reduces the number of networks required per system — reducing cost and improving reliability. Each flip-flop can be used either as a counter or shift register.

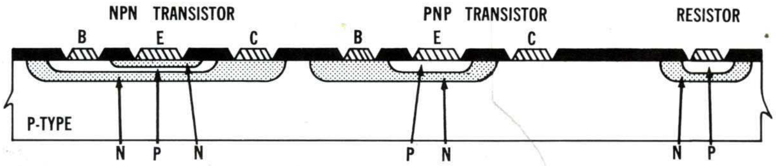
AND/OR/INVERT logic flexibility. Since transistors are used instead of input and output diodes, it is possible to fan-out from non-inverting gates. Availability of cascaded non-inverting gates, "wired OR" gates, and complementary inputs on the flip-flop make this the most flexible and powerful logic line in the industry.

J-K flip-flop operates on a single-phase clock. Complementary inputs have been provided so full J-K operation can be provided for both positive and negative logic.

Low noise susceptibility for capacitively coupled noise is provided by the low line-termination impedance in both the ON (50 ohms) and OFF (50 ohms) logic conditions.

Large-capacitance loads are easily driven at high speeds by the low-impedance output stage contained in each inverting network. Waveform integrity is preserved for capacitance loads of several hundred picofarads.

Master Slice capability. The Series 53 bar was designed to permit using "Master Slice" semi-custom interconnections. The large number of component elements on a network bar gives great latitude to designers.

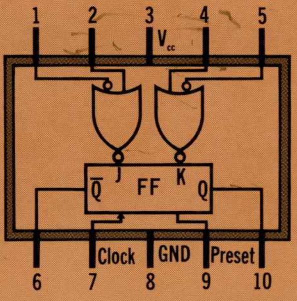


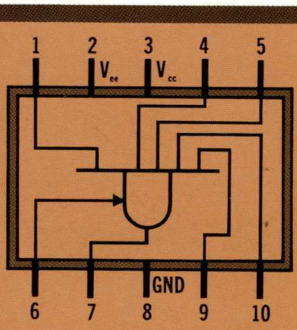
Triple-diffused structure used in Series 53 networks

SN530

Single-phase J-K Flip-flop

Propagation delay — 45 nsec
Fan-out — 10
Power dissipation — 27 mw





5-input AND/OR Gate or Expander

Propagation delay — 5 nsec
Fan-out — 4
Power dissipation — 10 mw

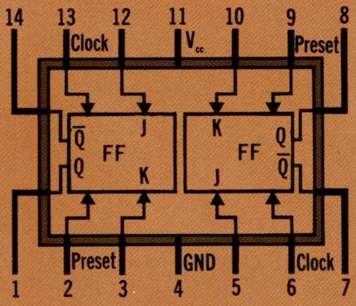
SN532

semiconductor networks

SN5302

Dual Single-phase J-K Flip-flop

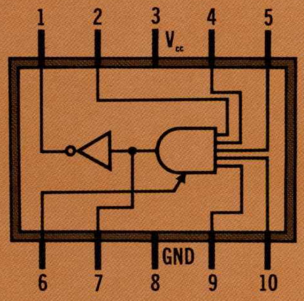
Propagation delay — 45 nsec
Fan-out — 10 per flip-flop
Power dissipation — 27 mw
per flip-flop



SN531

5-input NAND/NOR Gate

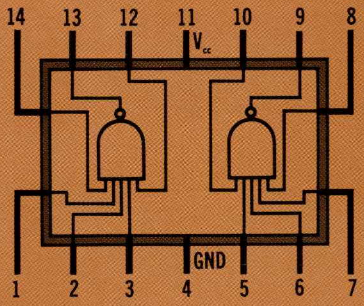
Propagation delay — 25 nsec
Fan-out
Inverting — 10
Non-inverting — 4
Power dissipation — 10 mw

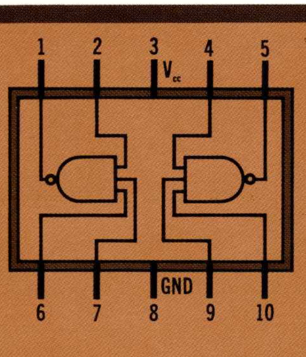


SN5311

Dual 5-input NAND/NOR Gate

Propagation delay — 25 nsec
Fan-out — 10 per gate
Power dissipation — 10 mw
per gate

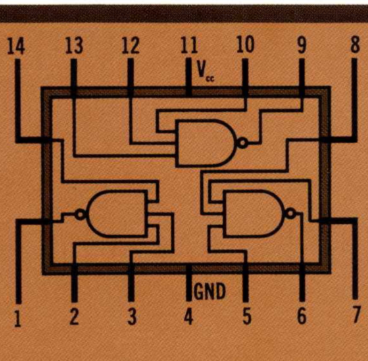




Dual 3-input NAND/NOR Gate

Propagation delay — 25 nsec
Fan-out — 10 per gate
Power dissipation — 10 mw
per gate

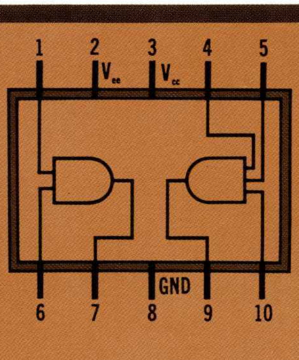
SN533



Triple 3-input NAND/NOR Gate

Propagation delay — 25 nsec
Fan-out — 10 per gate
Power dissipation — 10 mw
per gate

SN5331



Dual AND/OR Gate (2 and 3 Inputs)

Propagation delay — 5 nsec
Fan-out — 4 per gate
Power dissipation — 10 mw
per gate

SN534

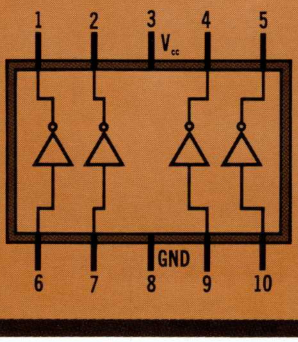
Series 53 continued on next page.

(Series 53 continued)

SN535

Quadruple Inverter/Driver

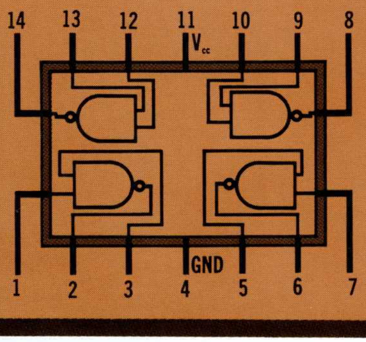
Propagation delay — 25 nsec
Fan-out — 10 per inverter
Power dissipation — 9 mw
per inverter



SN5360

Quadruple 2-input NAND/NOR Gate

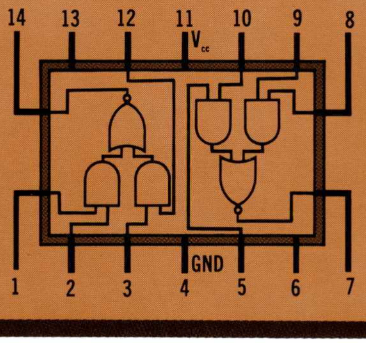
Propagation delay — 25 nsec
Fan-out — 10 per gate
Power dissipation — 10 mw
per gate

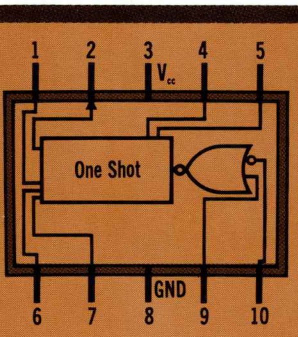


SN5370

Dual EXCLUSIVE-OR Gate

Propagation delay — 90 nsec
Fan-out — 10 per gate
Power dissipation — 20 mw
per gate

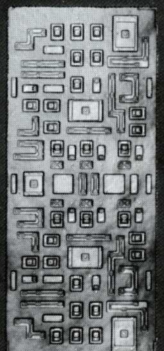




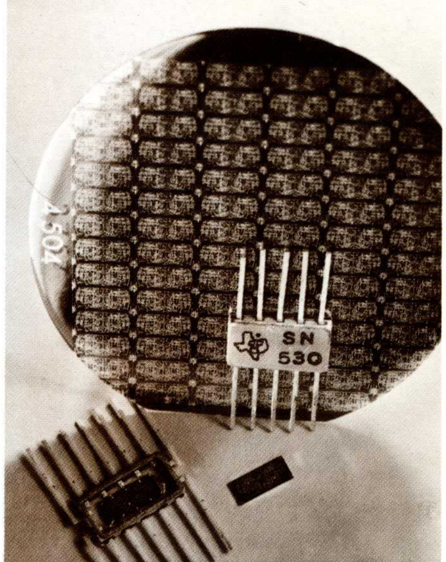
"One Shot" Monostable Multivibrator

Delay time — 100 nsec
Fan-out — 10
Power dissipation — 30 mw

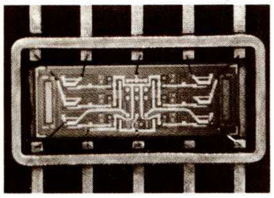
SN1005



Series 53 bar before metallic interconnection pattern is applied.



Series 53 Slice, bar, mounted bar, and completed network.



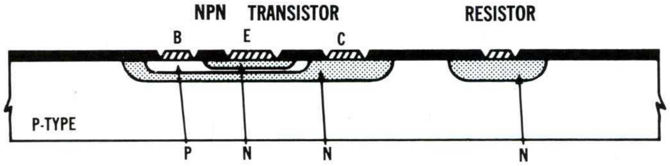
- Exceptionally low power dissipation, high fan-out
- Thoroughly proven reliability
- Master Slice capability
- Multiple circuit functions per package
- Familiar RCTL logic design
- Standard welded flat package

Series 51 RCTL digital SOLID CIRCUIT semiconductor networks

TYPICAL CHARACTERISTICS

Parameter	Basic Gate	Flip-flop
Propagation delay	130 nsec/gate @ 3 v 65 nsec/gate @ 6 v	300 nsec
Power dissipation	2 mw @ 3 v	2 mw @ 3 v
Fan-out	5, 25*	4, 20*
D-c noise margin	200 mv	200 mv
Supply voltage	3 to 6 v	3 to 6 v
Temperature range	—55 to +125°C	—55 to +125°C

*with emitter-follower outputs



Triple-diffused planar structure employed in Series 51 networks

This compatible line of monolithic semiconductor integrated circuits features the lowest power drain in the industry . . . typically 2 to 4 mw at 3 v. For this reason Series 51 networks are ideal for missile and space applications where size, weight, reliability, or power dissipation requirements are critical.

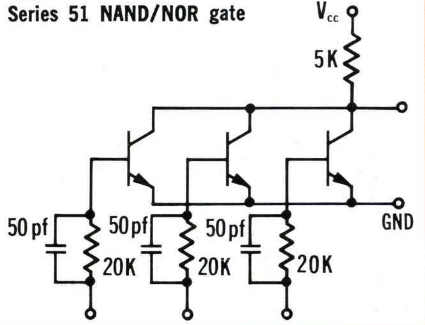
RCTL logic — familiar to designers —simplifies equipment design, as does the use of a single-phase clock. Series 51 networks have been used in systems employing clock rates well above 300 kc.

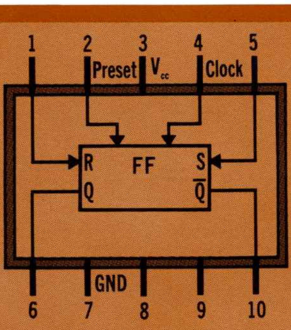
High fan-out. Emitter-follower outputs provide fan-out of 25 per gate, eliminating the need for external buffers.

Master Slice capability. Circuit variations can be provided quickly and economically by changing the deposited lead pattern on the Series 51 "Master Slice" bar. Available are 31 circuit elements, including 7 NPN transistors, 7 diodes, 3 resistors, 2 capacitors, and 6 R-C combinations which can be interconnected in scores of different configurations.

Proven Reliability. More than three years of successful manufacturing experience, hundreds of equipment applications, and millions of hours of reliability testing stand behind every Series 51 network.

Typical circuit for basic Series 51 NAND/NOR gate

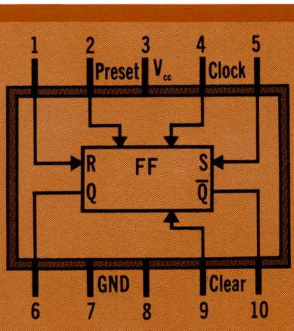




R-S Flip-flop/Counter

Fan-out — 4
Power diss — 2 mw @ 3 v
Propagation delay — 300 nsec

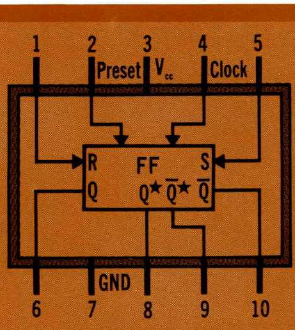
SN510A



R-S Flip-flop with Dual Presets

Fan-out — 4
Power diss — 2 mw @ 3 v
Propagation delay — 300 nsec

SN5101



R-S Flip-flop/Counter with Emitter-follower Output

Fan-out
  Collector output — 4
  Emitter-follower — 20
Power diss — 3 mw @ 3 v
Propagation delay — 300 nsec

SN511A

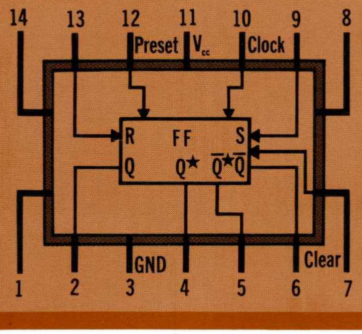
Series 51 continued on next page.

(Series 51 continued)

SN5111

R-S Flip-flop with Emitter-follower Output and Dual Presets

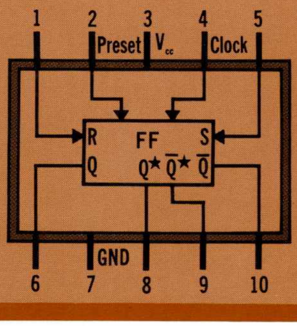
Fan-out
  Collector output — 4
  Emitter-follower — 20
Power diss — 3 mw @ 3 v
Propagation delay — 300 nsec



SN5112

Ripple-counter Flip-flop

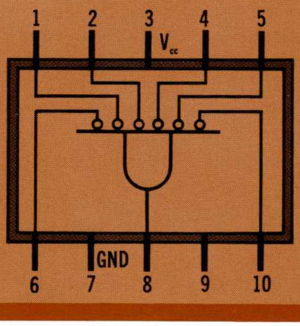
Fan-out
  Collector output, d-c — 4
  Emitter-follower, d-c — 16
  Collector output, a-c — 2
Power diss — 3 mw @ 3 v
Propagation delay — 300 nsec

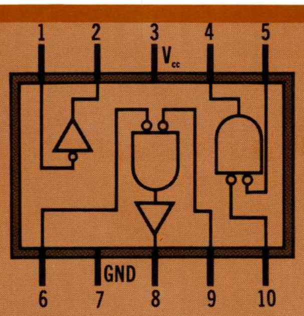


SN512A

6-input NAND/NOR Gate

Fan-out — 5
Power diss — 2 mw @ 3 v
Propagation delay — 65 nsec
  @ 6 v

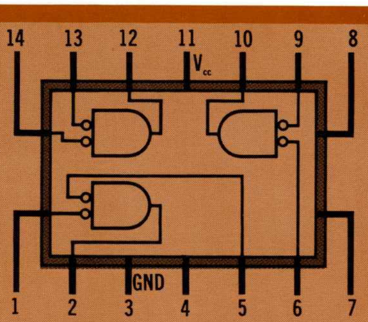




Dual 2-input NAND/NOR Gate and Inverter/Buffer

Fan-out
  Collector output —
    5 per gate
  Emitter-follower output —
    25 per gate
Power diss — 2 mw @ 3 v
Propagation delay — 65 nsec
  @ 6 v

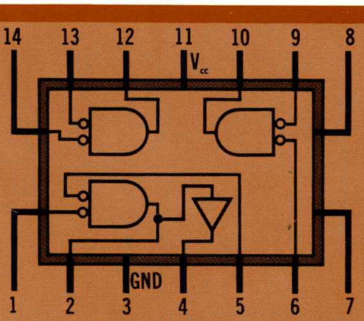
SN516A



Triple 2-input NAND/NOR Gate

Fan-out — 5 per gate
Power diss — 2 mw @ 3 v
Propagation delay — 65 nsec
  @ 6 v

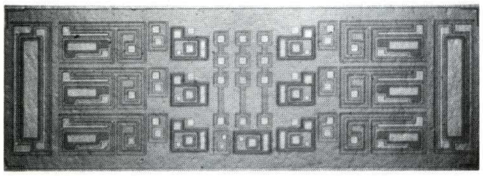
SN5161



Triple 2-input NAND/NOR Gate with Emitter-follower Output

Fan-out
  Collector output —
    5 per gate
  Emitter-follower output —
    25 per gate
Power diss — 2 mw @ 3 v
Propagation delay — 65 nsec
  @ 6 v

SN5162

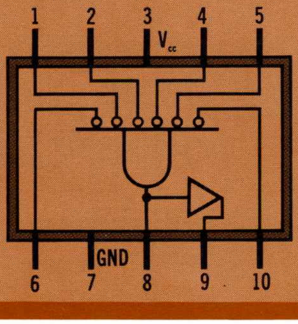


Series 51 bar before metallic interconnection pattern is applied

SN513A

6-input NAND/NOR Gate with Emitter-follower Output

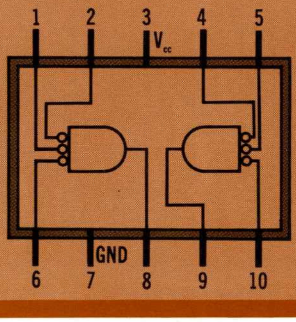
Fan-out
  Collector output — 5
  Emitter-follower — 25
Power diss — 3 mw @ 3 v
Propagation delay — 65 nsec @ 6 v



SN514A

Dual 3-input NAND/NOR Gate

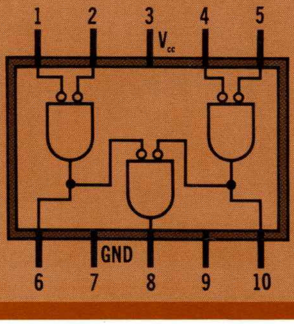
Fan-out — 5 per gate
Power diss — 2 mw @ 3 v
Propagation delay — 65 nsec @ 6 v

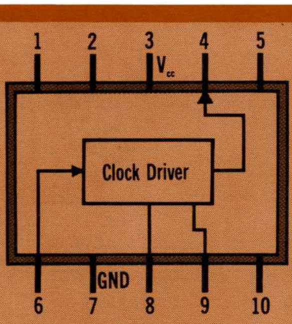


SN515A

EXCLUSIVE-OR Gate

Fan-out
  Auxiliary outputs — 4
  Exclusive-OR output — 5
Power diss — 3 mw @ 3 v
Propagation delay — 100 nsec @ 6 v

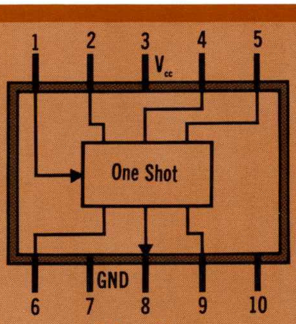




Clock Driver

Fan-out, a-c — 20
Power diss — 3 mw @ 3 v

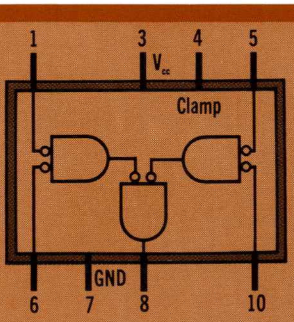
SN517A



"One Shot" Monostable Multivibrator

Fan-out — 5
Power diss — 2 mw @ 3 v
Pulse delay and pulse width adjustable by using internal and/or external R-C networks

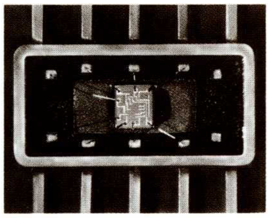
SN518A



Pulse EXCLUSIVE-OR Gate

Fan-out — 5
Power diss — 6 mw @ 3 v
Useful for up/down counter applications

SN5191



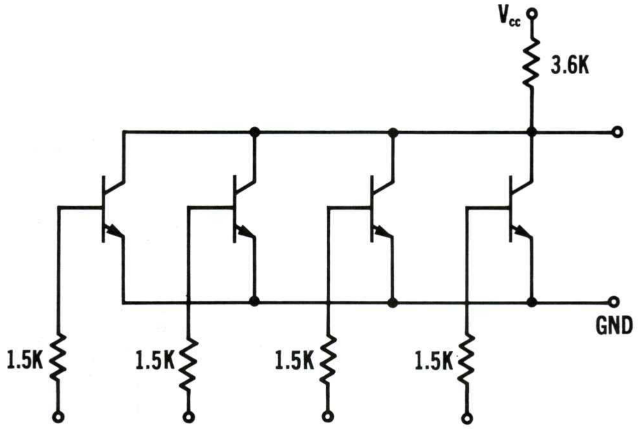
- Low power dissipation with moderate speed capability
- Choice of standard welded flat package or modified TO-5
- Gold-to-gold contact system
- Simple RTL logic configuration

NEW—Low-power RTL digital SOLID CIRCUIT

TYPICAL CHARACTERISTICS

Parameter	Basic Gate	Register
Propagation delay	35 nsec	70 nsec
Power dissipation	4 mw	15 mw
Fan-out	4	3
Supply voltage	3 v	3 v
Temperature range	—55 to +125°C	—55 to +125°C

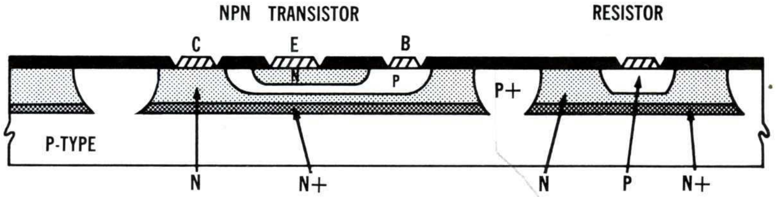
Typical circuit diagram for RTL Series NAND/NOR gate



This line of seven monolithic semiconductor integrated circuits combines low power dissipation with medium speed capabilities. The line is engineered and manufactured to the full-performance specifications of a sponsoring government agency. Compatibility is guaranteed through the full military temperature range of —55° to 125°C.

Choice of two packages. Equipment designers have a choice between TI's standard flat package and a modified TO-5 package with no price differential. The letter "A" after the type number designates units in TI flat packages. Type numbers without an alphabetical suffix indicate the low-profile TO-5 type package.

The register can be controlled either by a-c or d-c inputs. When the clocking input is high, control of the circuit is determined by d-c R and S inputs. For a-c operation, the register can be converted to a binary counter by simply connecting two leads externally.

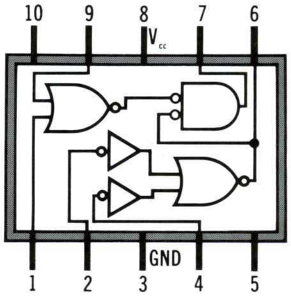


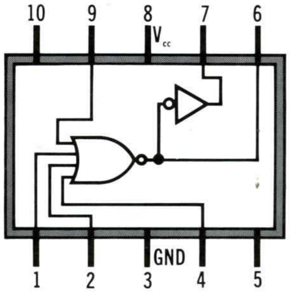
Planar diffused double-epitaxial structure used for RTL Series networks

SN729/SN729A

Adder

Propagation delay — 70 or 105 nsec
Power dissipation — 10 mw
Fan-out — 3 or 4





4-input Gate

Propagation delay — 35 or 70 nsec
Power dissipation — 4 mw
Fan-out — 3 or 4

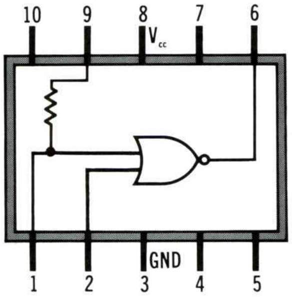
SN733/SN733A

semiconductor networks

SN730/SN730A

Buffer

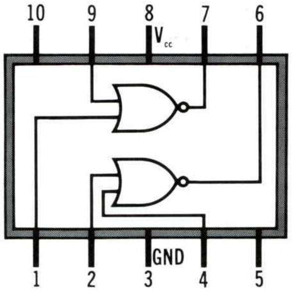
Propagation delay — 70 nsec
Power dissipation — 15 mw
Fan-out — 30



SN731/SN731A

Dual 2-input Gate

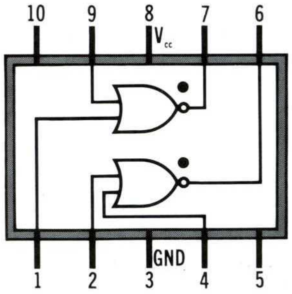
Propagation delay — 35 nsec
Power dissipation — 2 mw per gate
Fan-out — 4 per gate

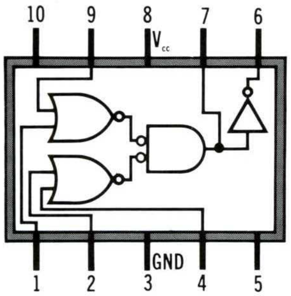


SN732/SN732A

Dual 2-input Expander Gate

Propagation delay — 35 nsec
Power dissipation — N/A
Fan-out — N/A

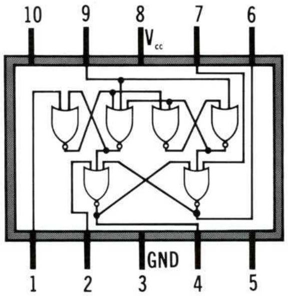




Half-adder

Propagation delay — 70 or 105 nsec
Power dissipation — 8 mw
Fan-out — 3 or 4

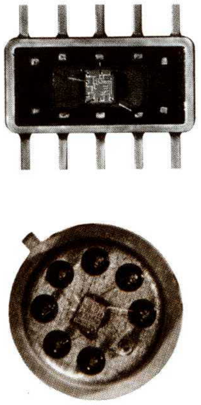
SN734/SN734A



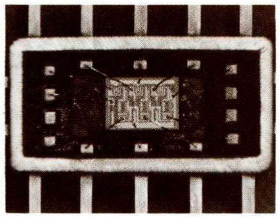
Register

Propagation delay — 70 nsec
Power dissipation — 15 mw
Fan-out — 3

SN735/SN735A



RTL networks are available both in standard ¼″ by ⅛″ flat packages and in modified TO-5 cases.



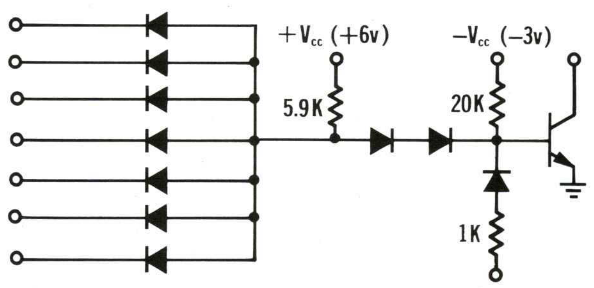
- Proven reliability in Minuteman II guidance and control-system applications
- Multiple circuit functions per package
- High noise immunity
- Linear and memory networks also available in Minuteman Series
- Standard welded flat package

Minuteman Series DTL digital SOLID CIRCUIT

TYPICAL CHARACTERISTICS

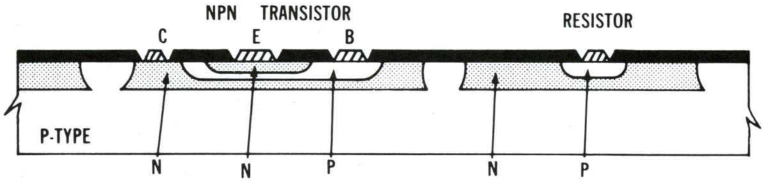
Parameters	Basic Gate	Flip-flop
Propagation delay	100 nsec	250 nsec
Power dissipation	20-40 mw	90 mw
Fan-out	12	12
D-c noise margin	500 mv	500 mv
Supply voltage	+6 v, —3 v	+6 v, —3 v
Temperature range	0° to +65°C	0° to +65°C

Circuit diagram for basic Minuteman Series NAND gate

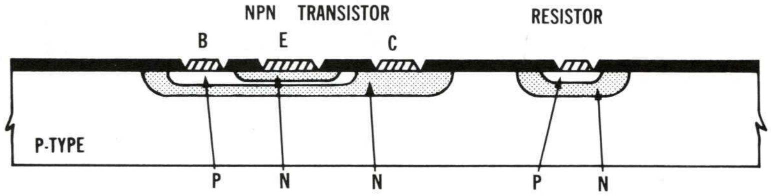


This compatible series of semiconductor integrated circuits was designed by Autonetics division of North American Aviation and TI. These digital units, along with linear units in the same series, perform more than 93 percent of the electronic functions in the guidance computer section of the Minuteman II missile.

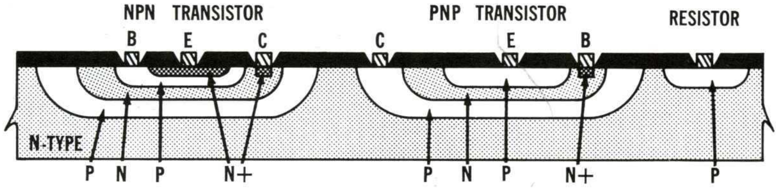
The NAND/NOR gates are conservatively designed for medium-speed operation with wide noise margins. A separate clock input is included in two of the gates — the SN341A and SN347A.



Diffused planar/epitaxial structure used for SN337A, SN344A



Triple-diffused planar structure used for SN341A, SN347A, SN359A



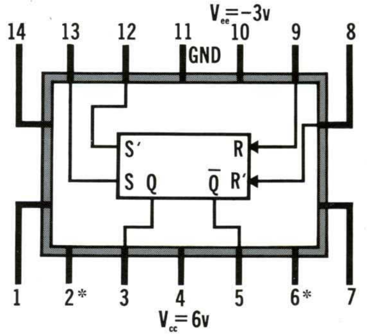
Quadruple-diffused planar structure used for SN343A, SN346A

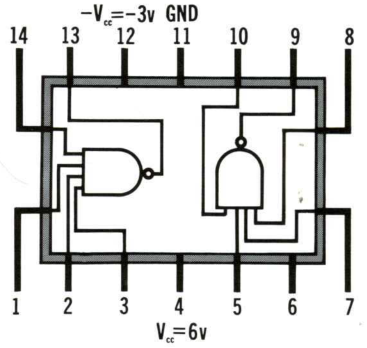
SN337A

Flip-flop

Propagation delay — 250 nsec
Fan-out — 12
Power dissipation — 90 mw

*Connection of lead 2 to lead 3 and lead 5 to lead 6 provides collector pull-up resistors for the Q and $\overline{Q}$ outputs.





Dual 4-input, Low-level NAND/NOR Gate (Unclocked)

Propagation delay — 140 nsec
Fan-out — 6 per gate
Power dissipation — 22 mw per gate

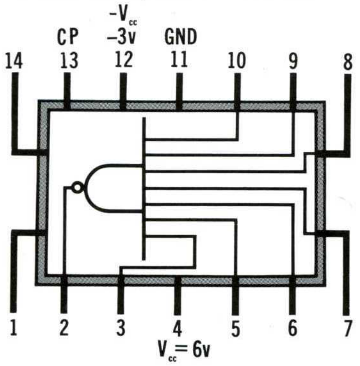
SN359A

semiconductor networks

SN341A

7-input NAND/NOR Gate (Clocked)

Propagation delay — 140 nsec
Fan-out — 6
Power dissipation — 12 mw

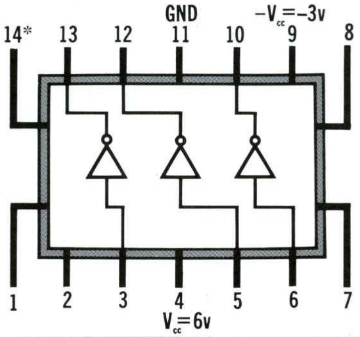


SN344A

Triple High-level NAND/NOR Gate

Propagation delay — 120 nsec
Fan-out — 12 per gate
Power diss — 85 mw per gate

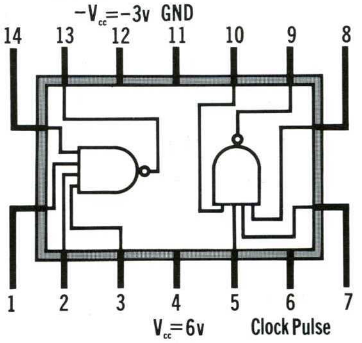
*Connection of lead 13 to lead 14 provides a collector pull-up resistor. Two other inverters have this collector resistor internally connected.

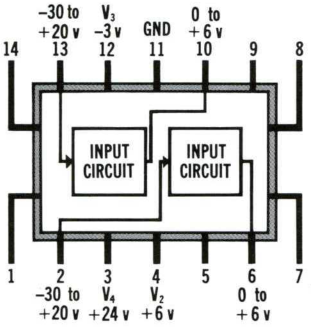


SN347A

Dual 4-input, Low-level NAND Gate (Clocked)

Propagation delay — 140 nsec
Fan-out — 6 per gate
Power dissipation — 22 mw per gate



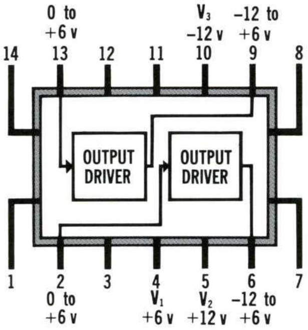


An inverting interface circuit that translates a large input voltage swing to a digital logic level.

Dual Input Network

Propagation delay — 500 nsec
Fan-out — 13
Power dissipation — 25 mw

SN343A

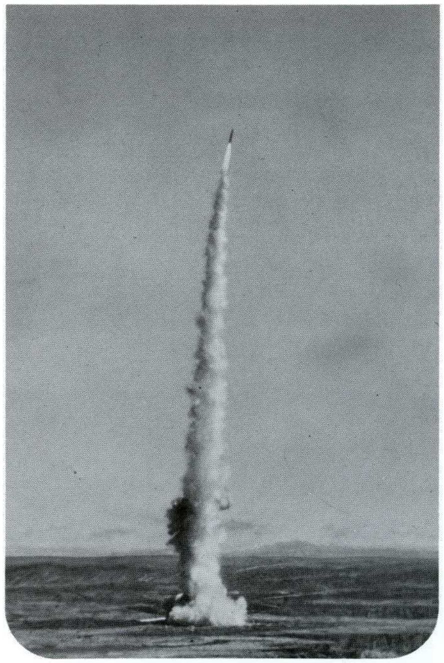


A non-inverting interface circuit that translates a digital logic level into a large output voltage swing.

Dual Output Driver

Propagation delay — 850 nsec
Fan-out — 11
Power dissipation — 160 mw

SN346A



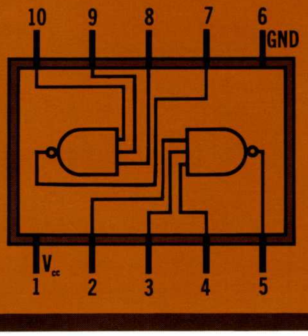
DTL Digital Special Gates

Special DTL gates that employ the multifunction approach feature low power drain and high d-c noise margin (1 v at 25°C). Operating temperature range is 0° to 125°C. Structures are diffused planar double-epitaxial. The gold-to-gold contact system is employed, and both networks are available in TI's standard welded flat package.

SN472

Dual 3-input Positive NAND Gate

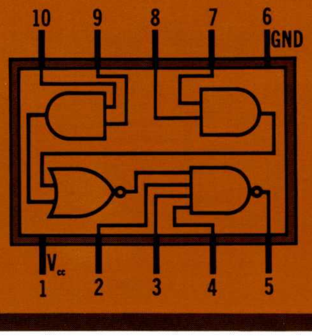
Propagation delay — 40 nsec
Power dissipation — 4 mw per gate
Fan-out — 5 per gate
D-c noise margin — 1 v
Supply voltage — 4 v



SN473

AND-NOR-NAND Gate

Propagation delay — 80 nsec
Power dissipation — 12 mw
Fan-out — 5
D-c noise margin — 1 v
Supply voltage — 4 v



Series 51R for severe-environment applications

For severe-environment military and aerospace applications, you can now specify a standard line of Series 51R semiconductor networks. This family of fifteen networks parallels TI's standard low-power Series 51 digital line.

Nearly four years' experience has thoroughly proved the reliability of Series 51 networks. Now you can get extra assurance of reliability through extra testing and processing. Each Series 51R network is subjected to:

- Centrifugal acceleration at 20,000 G in the Y_1 plane.
- Dynamic operation, burning-in each unit at 125°C for 168 hours.
- The radiographic inspection illustrated at right.

The complete list of networks available in the Series 51R family follows:

SNR510	R-S Flip-flop/Counter
SNR5101	R-S Flip-flop with Dual Presets
SNR511	R-S Flip-flop/Counter with Emitter-follower Output
SNR5111	R-S Flip-flop with Emitter-follower Output and Dual Presets
SNR5112	Ripple-counter Flip flop
SNR512	6-input NAND/NOR Gate
SNR513	6-input NAND/NOR Gate with Emitter-follower Output
SNR514	Dual 3-input NAND/NOR Gate
SNR515	EXCLUSIVE-OR Gate
SNR516	Dual 2-input NAND/NOR Gate and Inverter/Buffer
SNR5161	Triple 2-input NAND/NOR Gate
SNR5162	Triple 2-input NAND/NOR Gate with Emitter-follower Output
SNR517	Clock Driver
SNR518	"One Shot" Monostable Multivibrator
SNR5191	Pulse EXCLUSIVE-OR Gate

Radiographic inspection is performed on each Series 51R network, using TI's modern in-house X-ray facilities.

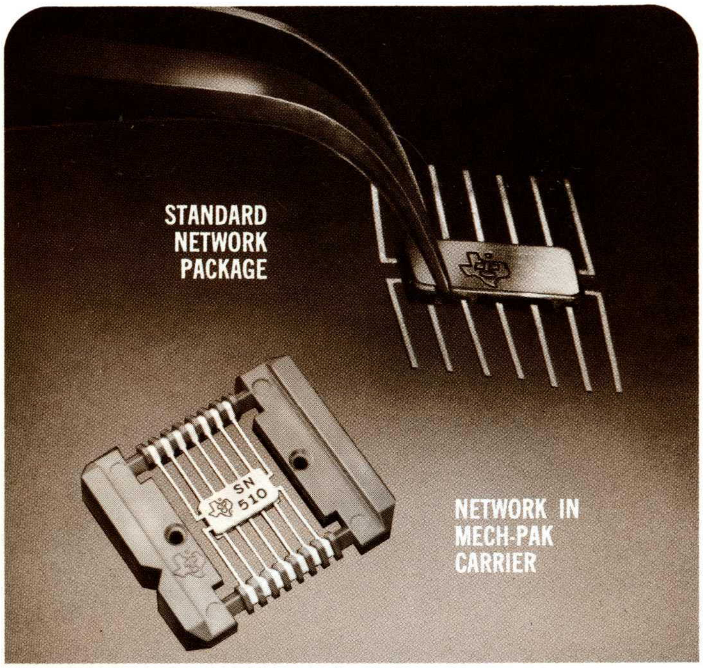
Package

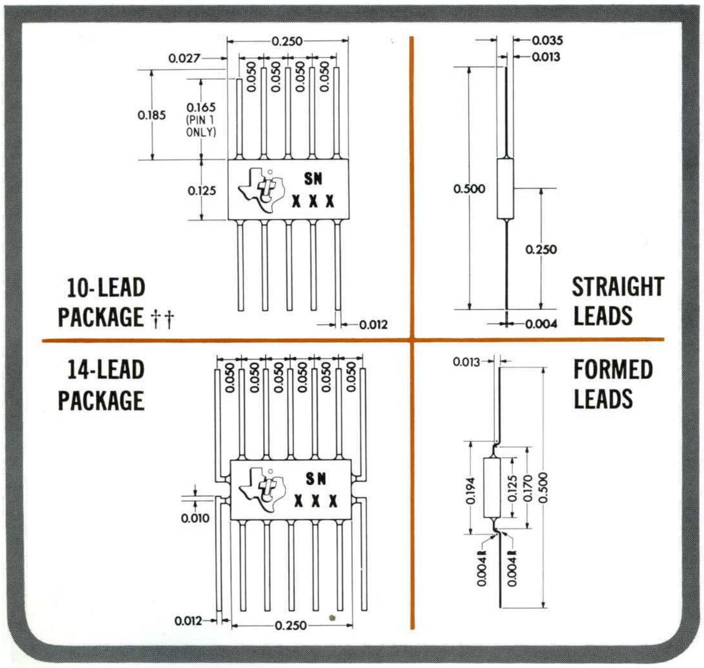
All TI networks are available in the standard 10- or 14-lead "flat-pack." The thin, rectangular configuration and lateral leads make this package suitable either for high-density equipment where size and weight are important or for mounted circuit-card assemblies where manufacturing cost and maintainability are major considerations.

The package — proved in field use over a four-year period — is all-welded construction, with a hermetic glass-to-metal seal. Leads are gold-plated F-15* alloy. The center-to-center lead spacing of 0.050 inches is a standard multiple of circuit-board interconnection spacings.

All external surfaces are metallic and are electrically insulated from leads and circuit. If requested, an insulator will be affixed to the bottom of the package. Thermal resistance (junction-to-case) of the package is 0.146°C per milliwatt (constant case temperature).

Other package configurations are available if required for your applications. These include the low-profile TO-5 type package with eight and ten leads, the low-profile, 8-lead, TO-47 type, and others.





Mech-Pak carrier. For your convenience, TI semiconductor networks are available in the Mech-Pak carrier — at no additional charge.

This exclusive plastic carrier simplifies handling and reduces costs of incoming inspection, testing, breadboarding, storage, and assembly. The carrier is particularly appropriate for mechanized assembly operations, and will withstand temperatures of 125°C for extended periods.

Insulators. Where printed-circuit conductors pass under the package, insulators are available to prevent the metallic base of the package from shorting the conductors. Semiconductor networks can be ordered with high-temperature Mylar† insulators permanently attached to the bottom of the package, at no additional charge. The insulator is 0.265 inches long, 0.140 inches wide, and 0.0025 inches thick.

Formed leads. For mounting convenience, semiconductor networks can be ordered with formed leads, as shown at the left. If formed leads are not specifically ordered, units will be shipped with straight leads.

Ordering instructions. Semiconductor networks may be ordered with Mech-Pak carrier, formed leads, insulators, or any combination thereof. Simply select the appropriate ordering suffix from the table below and place it after the standard part number.

Example: To order SN510A with Mech-Pak carrier, formed leads, and insulator, the network would be ordered as SN510A-5.

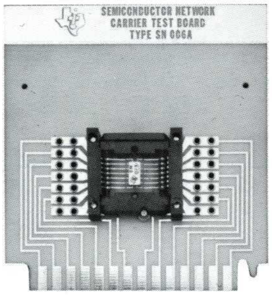
	Standard (No Mech-Pak Carrier)				Mech-Pak Carrier			
Lead Length	0.185 inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering SUFFIX	None (Standard)	— 6	— 7	— 1	— 2	— 3	— 4	— 5

**F-15 is the ASTM designation for a glass-sealing alloy containing nominally 29% nickel, 17% cobalt, and 53% iron.*

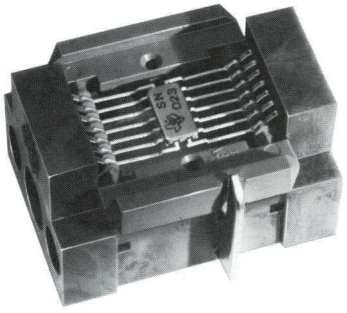
†DuPont trademark

††Two different lead-numbering systems are employed for 10-lead networks. Refer to individual logic diagrams for position of lead #1.

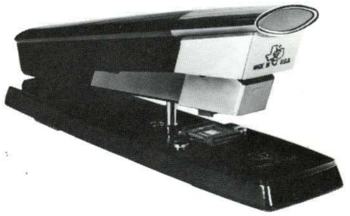
Accessory equipment



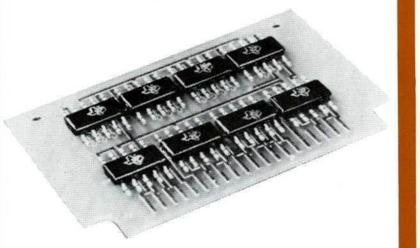
Test Board. SN006A is for incoming inspection and engineering breadboarding of networks in Mech-Pak carrier. Designed for extended use at 125°C. Uses Amphenol No. 143-015-01 printed-circuit connector or equivalent.



Test Socket. SN008 is designed for inspection and engineering breadboarding of networks in Mech-Pak carrier. Also, it is a convenient test fixture. Designed for extended use at 125°C.

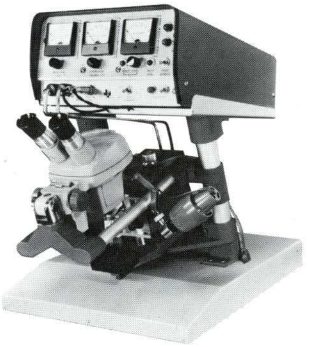


Shear-out Tool. This precision tool is used to shear the semiconductor network from the Mech-Pak carrier just before mounting. Standard dies are available for lead lengths of 0.080", 0.100", and 0.185".

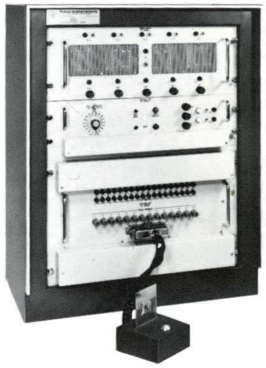


Printed-circuit Board. This superior weldable PC board consists of an epoxy-filled glass-fiber substrate clad on one or both sides with MULtiLAYER* clad metal foil. This board was specifically designed for use with semiconductor networks.

*Texas Instruments Trademark



Parallel-gap Welder. New dynamically controlled welder is designed to weld ribbon leads of semiconductor networks to selected printed-circuit materials . . . reducing cost and improving reliability of network-to-PC-board connections.



Integrated-circuit Testers. TI offers several types of high-speed automatically sequenced testers for production use. The Model 659A, for example, performs 36 tests in less than 1½ seconds.

Reliability

The table summarizes reliability information for semiconductor networks manufactured during 1964. Both long-term life tests and environmental tests are included. Based on this information, the present failure-rate estimate is 0.016% per 1000 hours at 55°C. This figure is the 60% upper confidence level (UCL) for one failure out of more than 12 million equivalent hours accrued on 1964 production.

Continued environmental testing demonstrates the ability of all semiconductor networks produced to substantially exceed the military requirements of MIL-S-19500.

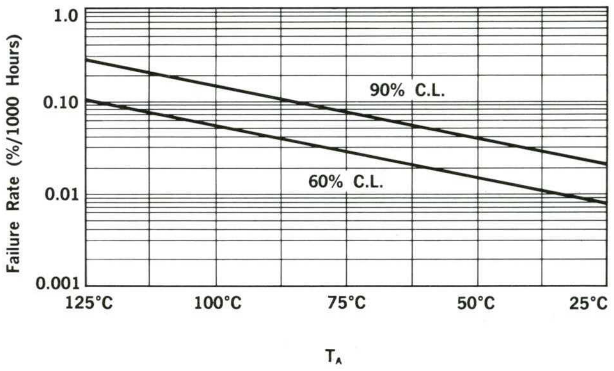
These data are only a small part of the total reliability information available. More than 33 million equivalent hours of circuit data have been accumulated on networks since early 1961. All reliability data is for networks mounted in the standard ¼″ x ⅛″ flat package.

In addition to reliability testing of the finished semiconductor networks, high reliability is assured by 100% processing of all semiconductor networks after final sealing through the following sequence:

- **Temperature Cycle:**
  10 cycles minimum; +125° C to —55° C
- **High-temperature Bake:**
  48 hours minimum
- **Gross-leak Test:**
  Hot-liquid immersion
- **Helium Leak Test:**
  50 x 10^{-8} cc/sec maximum
- **Final 100% Electrical Test:**
  at temperature extremes

Summary of network reliability data accumulated during 1964.

Test Series	Stress Level	Number of Units on Test	Number of Failures	Longest Clock Hours	Actual Test Hours	Equivalent 55°C Test Hours
Weekly-add-to	125°C Operating	358	1	5000	632,000	4,300,000
Weekly-add-to	150°C Storage	200	0	2000	287,000	2,290,000
USAF Hi-Rel	125°C Storage	48	0	5000	240,000	1,630,000
USAF Hi-Rel	200°C Storage	44	0	5000	220,000	4,120,000
TOTALS		650	1		1,379,000	12,340,000



This chart enables you to determine a failure rate for the particular temperature and confidence level appropriate to your own applications.

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Printed in U.S.A.