SDAD001

ALS/AS Logic Circuits Data Book

1983

Advanced Low-power Schottky/ Advanced Schottky

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ALS/AS LOGIC CIRCUITS DATA BOOK

Advanced Low-Power Schottky and Advanced Schottky Logic Circuits Data Book

TEXAS INSTRUMENTS

SDAD001
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Printed in U.S.A.

In memoriam

Dale Hunt
1932–1982
and
Robert P. Jones
1922–1982

IMPORTANT NOTICE

Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

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Information contained herein supersedes data published in the *Supplement to the TTL Data Book* LCC4162.

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INTRODUCTION

In this data book, Texas Instruments is pleased to present important technical information on the most advanced families of TTL integrated circuits, Advanced Low-Power Schottky (ALS), and Advanced Schottky (AS). Combined improvements in bar design, tooling production, and wafer fabrication culminate in circuits capable of twice the data throughput at only half the power requirements when compared to the existing LSTTL and STTL product spectrum. The efficiencies realized by ALS and AS are being offered to system designers in the following forms:

1. Pin-to-pin compatible, plug-in versions of most popular LSTTL and STTL functions.
2. Higher-density MSI and LSI functions with near-term extensions into products with VLSI complexities.

The ease of use of pin-to-pin compatible functions enables upgrading existing TTL based systems with the following benefits:

- Reduced system power requirements
- Enhanced critical system performance
- Improved system reliability

New system designs can capitalize on both the improved efficiency of the pin-compatible devices and the higher densities of the MSI/LSI series of devices with the following system benefits:

- Reduced system component count
- Expanded functional capabilities
- Improved levels of cost effectiveness
- Compatibility of use and full DC and AC specifications enable improved system design-in cycle times

ALS and AS devices utilize an advanced wafer fabrication process that includes ion-implanted transistors, oxide isolations, and composed mask sets. This process is coupled with circuit design techniques to implement the following:

- Improve input threshold and noise margins
- Improve line driving and receiving
- Maintain or increase drive capability
- Increase density into VLSI functions
- Implement universal logic solutions
- Take advantage of new packaging
  - 24-pin 300-mil DIP
  - Ceramic and plastic chip carriers

The ALS/AS family will grow to well over 200 devices through the end of 1983. Included among the new functions are:

- 16-bit by 16-bit universal multiplier
- 32-bit error detector and corrector
- High-performance ($14 \times 32 \times 6$) FPLA's
- 20-MHz 8-bit-slice universal processor element with on-board register file
- 20-MHz 14-bit controller with 9-word stack
- Many additional pin-compatible ALS devices

Included in this volume is a Functional Index to all bipolar digital device types available or under development showing the available technologies for each type (Standard TTL, Schottky, Low-Power Schottky, Advanced Low-Power Schottky, Advanced Schottky, etc.). Logic symbols prepared in anticipation of IEEE Std. 91-1982 and pin assignments for all bipolar devices are shown in the Product Guide section of this data book with typical performance data and chip carrier information where applicable. These additions to the data book should prove helpful to design and component engineers by providing ready access to TI's full line of bipolar digital device types and technologies. Package dimensions given in the Mechanical Data section of this book are in metric measurement (and parenthetically in inches), which should simplify board layout for designers involved in metric conversion and new designs.

While this volume offers design and specification data for bipolar Advanced Low-Power Schottky (ALS) and Advanced Schottky (AS) components, complete technical data for any TI semiconductor product is available from your nearest TI field sales office, local authorized TI distributor, or by writing direct to: Marketing and Information Services, Texas Instruments Incorporated, P.O. Box 225012, MS 308, Dallas, Texas 75265.

General Information

NUMERICAL INDEX

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NUMERICAL INDEX

INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

PART I — OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

f_{max} **Maximum clock frequency**
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

I_{CC} **Supply current**
The current into* the V_{CC} supply terminal of an integrated circuit.

I_{CCH} **Supply current, outputs high**
The current into* the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the high level.

I_{CCL} **Supply current, outputs low**
The current into* the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the low level.

I_{IH} **High-level input current**
The current into* an input when a high-level voltage is applied to that input.

I_{IL} **Low-level input current**
The current into* an input when a low-level voltage is applied to that input.

I_{OH} **High-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

I_{OL} **Low-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

I_{OS} **Short-circuit output current**
The current into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

I_{OZH} **Off-state (high-impedance-state) output current (of a three-state output) with high-level voltage applied**
The current flowing into* an output having three-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output and with a high-level voltage applied to the output.
NOTE: This parameter is measured with other input conditions established that would cause the output to be at a low level if it were enabled.

*Current out of a terminal is given as a negative value.

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I_{OZL} **Off-state (high-impedance-state) output current (of a three-state output) with low-level voltage applied**
The current flowing into* an output having three-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output and with a low-level voltage applied to the output.
NOTE: This parameter is measured with other input conditions established that would cause the output to be at a high level if it were enabled.

V_{IH} **High-level input voltage**
An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.
NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IK} **Input clamp voltage**
An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

V_{IL} **Low-level input voltage**
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.
NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{OH} **High-level output voltage**
The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a high level at the output.

V_{OL} **Low-level output voltage**
The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a low level at the output.

t_a **Access time**
The time interval between the application of a specific input pulse and the availability of valid signals at an output.

t_{dis} **Disable time (of a three-state output)**
The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state. (t_{dis} = t_{PHZ} or t_{PLZ}).

t_{en} **Enable time (of a three-state output)**
The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low). (t_{en} = t_{PZH} or t_{PZL}).

*Current out of a terminal is given as a negative value.

t_h **Hold time**
The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.
NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

t_{pd} **Propagation delay time**
The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. (t_{pd} = t_{PHL} or t_{PLH}).

t_{PHL} **Propagation delay time, high-to-low-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{PHZ} **Disable time (of a three-state output) from high level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

t_{PLH} **Propagation delay time, low-to-high-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PLZ} **Disable time (of a three-state output) from low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

t_{PZH} **Enable time (of a three-state output) to high level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

t_{PZL} **Enable time (of a three-state output) to low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

t_{sr} **Sense recovery time**
The time interval needed to switch a memory from a write mode to a read mode and to obtain valid data signals at the output.

t_{su} **Setup time**
The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.
NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

t_w **Pulse duration (width)**
The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

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PART II — CLASSIFICATION OF CIRCUIT COMPLEXITY

Gate Equivalent Circuit

A basic unit-of-measure of relative digital-circuit complexity. The number of gate equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

Large-Scale Integration, LSI

A concept whereby a complete major subsystem or system function is fabricated as a single microcircuit. In this context a major subsystem or system, whether digital or linear, is considered to be one that contains 100 or more equivalent gates or circuitry of similar complexity.

Medium-Scale Integration, MSI

A concept whereby a complete subsystem or system function is fabricated as a single microcircuit. The subsystem or system is smaller than for LSI, but whether digital or linear, is considered to be one that contains 12 or more equivalent gates or circuitry of similar complexity.

Small-Scale Integration, SSI

Integrated circuits of less complexity than medium-scale integration (MSI).

Very-Large-Scale Integration, VLSI

The description of any IC technology that is much more complex than large-scale integration (LSI), and involves a much higher equivalent gate count. At this time an exact definition including a minimum gate count has not been standardized by JEDEC or the IEEE.

The following symbols are used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
↶	=	value/level is re-entered
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state-output
a . . h	=	the level of steady-state inputs at inputs A through H respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$	=	complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑
⎍	=	one high-level pulse
⎎	=	one low-level pulse
TOGGLE	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑.

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, ⎍ or ⎎, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

Among the most complex function tables in this book are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

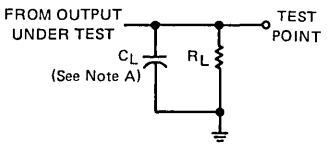
The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output Q_A, data entered at B will be at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

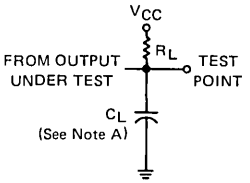
The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both mode inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

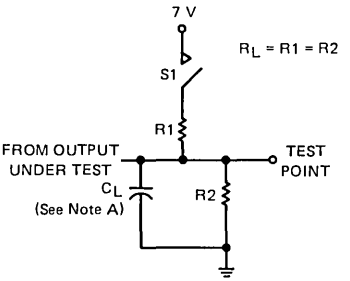
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

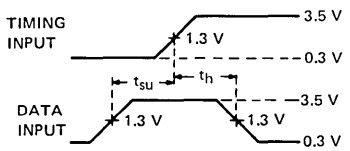


LOAD CIRCUIT FOR OPEN-COLLOCTOR OUTPUTS

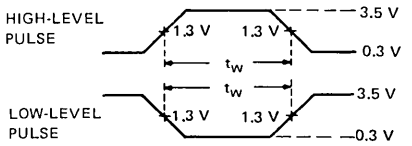


LOAD CIRCUIT FOR THREE-STATE OUTPUTS

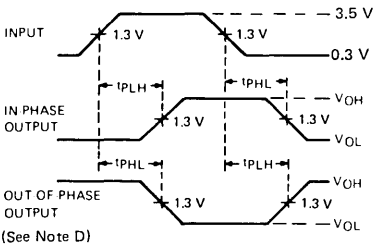
NOTE A. C_L includes probe and jig capacitance.



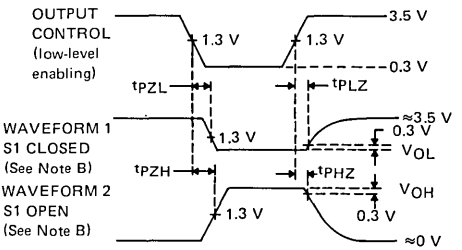
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cyle = 50%.

D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

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TYPICAL CHARACTERISTICS†

'ALS00A
PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

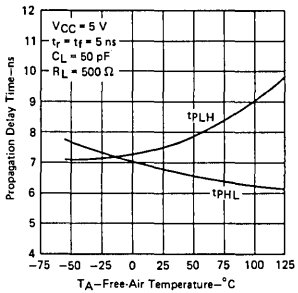

FIGURE 1

'ALS00A
PROPAGATION DELAY TIMES
vs
INPUT RISE & FALL TIMES

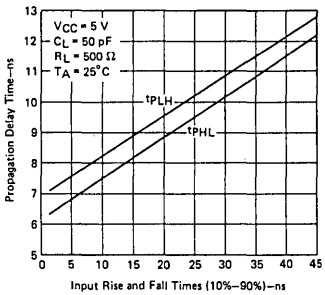

FIGURE 2

'ALS00AN
PROPAGATION DELAY TIMES
vs
LOAD CAPACITANCE

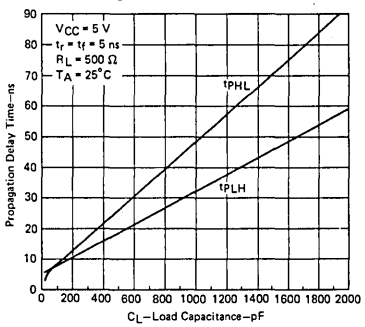

FIGURE 3

'ALS244
PROPAGATION DELAY TIMES
vs
LOAD CAPACITANCE

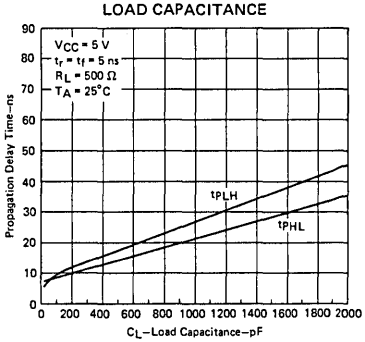

FIGURE 4

'ALS00A
POWER DISSIPATION PER GATE
vs
FREQUENCY

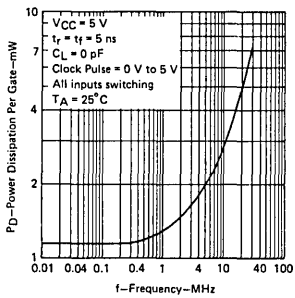

FIGURE 5

†Data for temperatures below 0°C and above 70°C are applicable for Series 54ALS circuits only.

TYPICAL CHARACTERISTICS†

'AS804A
PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

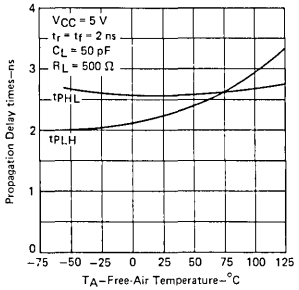

FIGURE 1

'AS804A
PROPAGATION DELAY TIMES
vs
INPUT RISE AND FALL TIMES

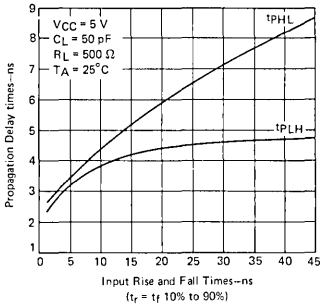

FIGURE 2

'AS804A
PROPAGATION DELAY TIMES
vs
LOAD CAPACITANCE

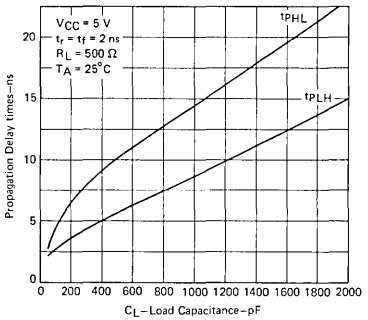

FIGURE 3

†Data for temperatures below 0°C and above 70°C are applicable for Series 54AS Circuits only.

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Advanced Low-Power Schottky and Advanced Schottky Circuits

D2661, APRIL 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

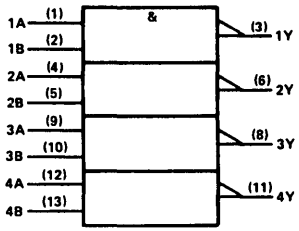
These devices contain four independent 2-input NAND gates. They perform the boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54ALS00A is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS00A is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each gate)

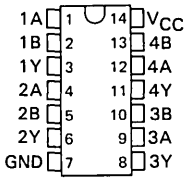
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol

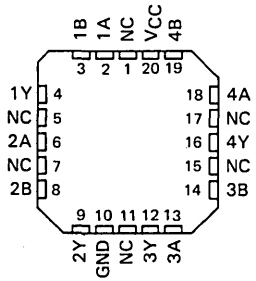


Pin numbers shown are for J and N packages.

SN54ALS00A . . . J PACKAGE
SN74ALS00A . . . N PACKAGE
(TOP VIEW)



SN54ALS00A . . . FH PACKAGE
SN74ALS00A . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS00A . . . . . −55°C to 125°C
SN74ALS00A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

2

recommended operating conditions

		SN54ALS00A			SN74ALS00A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4				mA
							8	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS00A			SN74ALS00A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4					V
	V_{CC} = 4.5 V	I_{OH} = −0.4 mA				2.7	3.4		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.5	0.85		0.5	0.85	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.5	3		1.5	3	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS00A	SN54ALS00A		SN74ALS00A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	4	3	14	3	11	ns
t_{PHL}	A or B	Y	3	2	10	2	8	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

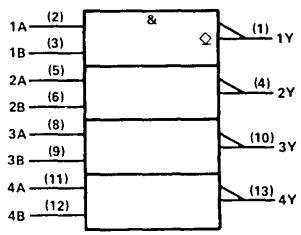
These devices contain four independent 2-input NAND gates. They perform the boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS01 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS01 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

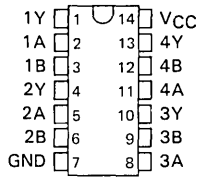
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol

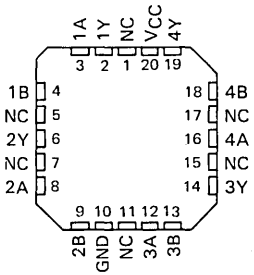


Pin numbers shown are for J and N packages.

SN54ALS01 . . . J PACKAGE
SN74ALS01 . . . N PACKAGE
(TOP VIEW)



SN54ALS01 . . . FH PACKAGE
SN74ALS01 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS01 . . . . . −55°C to 125°C
SN74ALS01 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS01			SN74ALS01			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4				mA
							8	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS01			SN74ALS01			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.43	0.85		0.43	0.85	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.62	3		1.62	3	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			'ALS01	SN54ALS01		SN74ALS01		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	20	23	59	23	54	ns
t_{PHL}	A or B	Y	12	8	29	8	28	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2661, APRIL 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

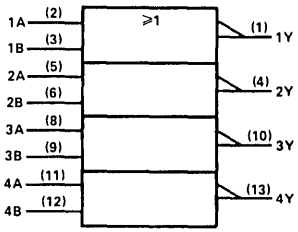
These devices contain four independent 2-input NOR gates. They perform the boolean functions $Y = \overline{A+B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN54ALS02 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS02 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

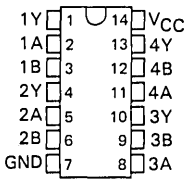
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol

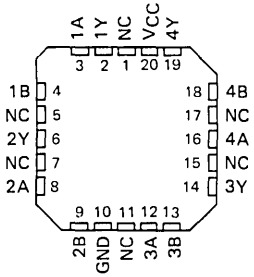


Pin numbers shown are for J and N packages.

SN54ALS02 . . . J PACKAGE
SN74ALS02 . . . N PACKAGE
(TOP VIEW)



SN54ALS02 . . . FH PACKAGE
SN74ALS02 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS02 . . . . . −55 °C to 125 °C
SN74ALS02 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

2

recommended operating conditions

		SN54ALS02			SN74ALS02			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4				mA
							8	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS02			SN74ALS02			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4					V
	V_{CC} = 4.5 V	I_{OH} = −0.4 mA				2.7	3.4		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.86	2.2		0.86	2.2	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		2.16	4		2.16	4	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25 °C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS02	SN54ALS02		SN74ALS02		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	6	3	14	3	12	ns
t_{PHL}	A or B	Y	5	3	11	3	10	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

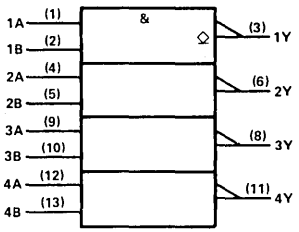
These devices contain four independent 2-input NAND gates. They perform the boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS03A is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS03A is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each gate)

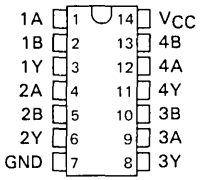
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol

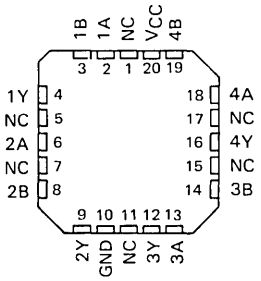


Pin numbers shown are for J and N packages.

SN54ALS03A . . . J PACKAGE
SN74ALS03A . . . N PACKAGE
(TOP VIEW)



SN54ALS03A . . . FH PACKAGE
SN74ALS03A . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS03A . . . . . −55°C to 125°C
SN74ALS03A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

2

recommended operating conditions

		SN54ALS03A			SN74ALS03A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4				mA
							8	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS03A			SN74ALS03A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.43	0.85		0.43	0.85	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.62	3		1.62	3	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			'ALS03A	SN54ALS03A		SN74ALS03A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	20	23	59	23	54	ns
t_{PHL}	A or B	Y	12	5	26	5	22	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

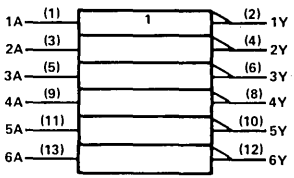
These devices contain six independent inverters. They perform the boolean function $Y = \overline{A}$.

The SN54ALS04 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS04 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each inverter)

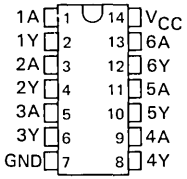
INPUT A	OUTPUT Y
H	L
L	H

logic symbol

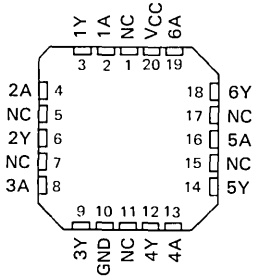


Pin numbers shown are for J and N packages.

SN54ALS04 . . . J PACKAGE
SN74ALS04 . . . N PACKAGE
(TOP VIEW)



SN54ALS04 . . . FH PACKAGE
SN74ALS04 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS04 . . . . . −55°C to 125°C
SN74ALS04 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

2

recommended operating conditions

		SN54ALS04			SN74ALS04			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4				mA
							8	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS04			SN74ALS04			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4					V
	V_{CC} = 4.5 V	I_{OH} = −0.4 mA				2.7	3.4		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.65	1.1		0.65	1.1	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		2.4	3.8		2.4	3.8	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX			UNIT
			'ALS04	SN54ALS04		SN74ALS04	
			TYP	MIN	MAX	MIN	MAX
t_{PLH}	A	Y	4	3	14	3	11	ns
t_{PHL}	A	Y	3	2	12	2	9	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54ALS05, SN74ALS05
HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

D2661, APRIL 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

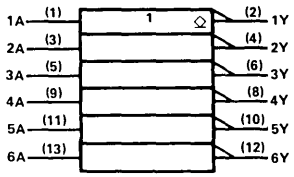
These devices contain six independent inverters. They perform the boolean function $Y = \overline{A}$. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS05 is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS05 is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each inverter)

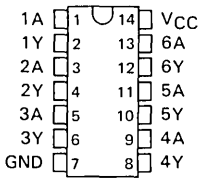
INPUT A	OUTPUT Y
H	L
L	H

logic symbol

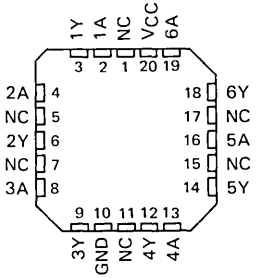


Pin numbers shown are for J and N packages.

SN54ALS05 . . . J PACKAGE
SN74ALS05 . . . N PACKAGE
(TOP VIEW)



SN54ALS05 . . . FH PACKAGE
SN74ALS05 . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS05 . . . . . −55°C to 125°C
SN74ALS05 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

2

recommended operating conditions

		SN54ALS05			SN74ALS05			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4				mA
							8	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS05			SN74ALS05			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.65	1.1		0.65	1.1	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		2.4	3.8		2.4	3.8	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			'ALS05	SN54ALS05		SN74ALS05		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	20	23	59	23	54	ns
t_{PHL}	A	Y	7	7	29	7	23	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

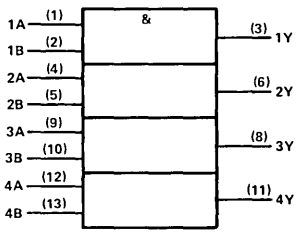
These devices contain four independent 2-input AND gates. They perform the boolean functions $Y = A \cdot B$ or $Y = \overline{\overline{A}+\overline{B}}$ in positive logic.

The SN54ALS08 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS08 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each gate)

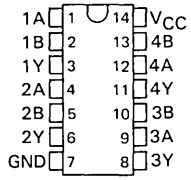
INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol

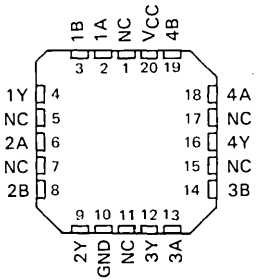


Pin numbers shown are for J and N packages.

SN54ALS08 . . . J PACKAGE
SN74ALS08 . . . N PACKAGE
(TOP VIEW)



SN54ALS08 . . . FH PACKAGE
SN74ALS08 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS08 . . . . . −55 °C to 125 °C
SN74ALS08 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

2

recommended operating conditions

		SN54ALS08			SN74ALS08			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4				mA
							8	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS08			SN74ALS08			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4					V
	V_{CC} = 4.5 V	I_{OH} = −0.4 mA				2.7	3.4		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.3	2.4		1.3	2.4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		2.2	4		2.2	4	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25 °C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS08	SN54ALS08		SN74ALS08		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	8	4	16	4	14	ns
t_{PHL}	A or B	Y	5	3	12	3	10	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

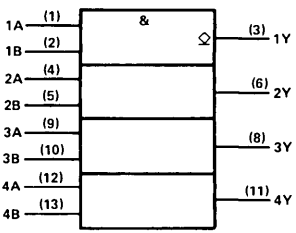
These devices contain four independent 2-input AND gates. They perform the boolean functions $Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS09 is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS09 is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each gate)

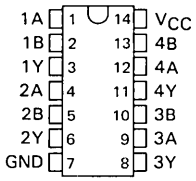
INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol

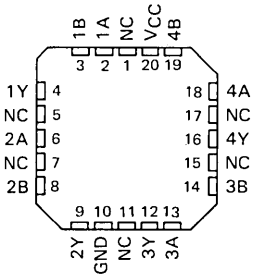


Pin numbers shown are for J and N packages.

SN54ALS09 . . . J PACKAGE
SN74ALS09 . . . N PACKAGE
(TOP VIEW)



SN54ALS09 . . . FH PACKAGE
SN74ALS09 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS09 . . . . . −55 °C to 125 °C
SN74ALS09 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

2

recommended operating conditions

		SN54ALS09			SN74ALS09			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4				mA
							8	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS09			SN74ALS09			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.35	2.4		1.35	2.4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		2.2	4		2.2	4	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25 °C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			'ALS09	SN54ALS09		SN74ALS09		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	20	23	59	23	54	ns
t_{PHL}	A or B	Y	10	5	17	5	15	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
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D2661, APRIL 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

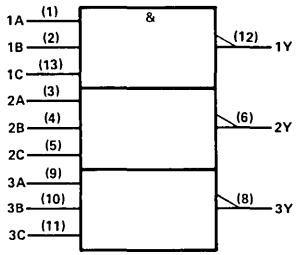
These devices contain three independent 3-input NAND gates. They perform the boolean functions $Y = \overline{A \cdot B \cdot C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

The SN54ALS10 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS10 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

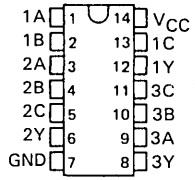
INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

logic symbol

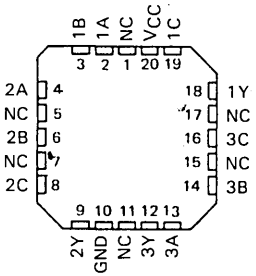


Pin numbers shown are for J and N packages.

SN54ALS10 . . . J PACKAGE
SN74ALS10 . . . N PACKAGE
(TOP VIEW)



SN54ALS10 . . . FH PACKAGE
SN74ALS10 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS10 . . . . . −55 °C to 125 °C
SN74ALS10 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

2

recommended operating conditions

		SN54ALS10			SN74ALS10			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4				mA
							8	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS10			SN74ALS10			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4					V
	V_{CC} = 4.5 V	I_{OH} = −0.4 mA				2.7	3.4		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.32	0.6		0.32	0.6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.2	2.2		1.2	2.2	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25 °C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS10	SN54ALS10		SN74ALS10		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	4	3	14	3	11	ns
t_{PHL}	Any	Y	10	4	21	4	18	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
INCORPORATED
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D2661, APRIL 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

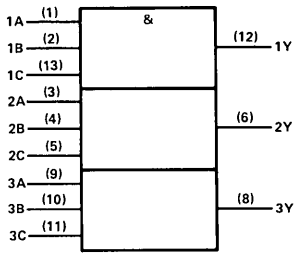
These devices contain three independent 3-input AND gates. They perform the boolean functions $Y = A \cdot B \cdot C$ or $Y = \overline{\overline{A}+\overline{B}+\overline{C}}$ in positive logic.

The SN54ALS11 is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS11 is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each gate)

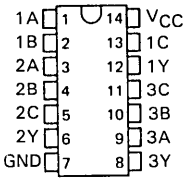
INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

logic symbol

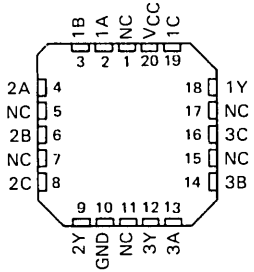


Pin numbers shown are for J and N packages.

SN54ALS11 . . . J PACKAGE
SN74ALS11 . . . N PACKAGE
(TOP VIEW)



SN54ALS11 . . . FH PACKAGE
SN74ALS11 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS11 . . . . . −55°C to 125°C
SN74ALS11 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

2

recommended operating conditions

		SN54ALS11			SN74ALS11			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4				mA
							8	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS11			SN74ALS11			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4					V
	V_{CC} = 4.5 V	I_{OH} = −0.4 mA				2.7	3.4		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		1	1.8		1	1.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		1.6	3		1.6	3	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS11	SN54ALS11		SN74ALS11		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	12	5	23	5	20	ns
t_{PHL}	Any	Y	6	3	12	3	10	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
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POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

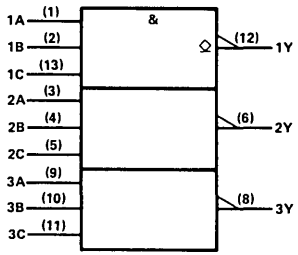
These devices contain three independent 3-input NAND gates with open-collector outputs. These gates perform the boolean functions $Y = \overline{A \cdot B \cdot C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS12 is characterized for operation over the full military range of −55°C to 125°C. The SN74ALS12 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

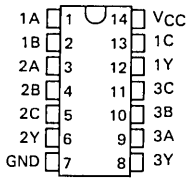
INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

logic symbol

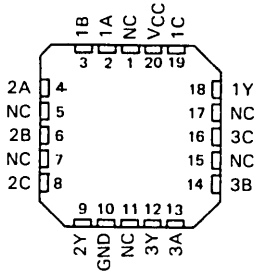


Pin numbers shown are for J and N packages.

SN54ALS12 . . . J PACKAGE
SN74ALS12 . . . N PACKAGE
(TOP VIEW)



SN54ALS12 . . . FH PACKAGE
SN74ALS12 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS12 . . . . . −55 °C to 125 °C
SN74ALS12 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS12			SN74ALS12			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4				mA
							8	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS12			SN74ALS12			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_{IL} = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.32	0.6		0.32	0.6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.2	2.2		1.2	2.2	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25 °C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			'ALS12	SN54ALS12		SN74ALS12		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	20	23	59	23	54	ns
t_{PHL}	Any	Y	15	9	37	9	30	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
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- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

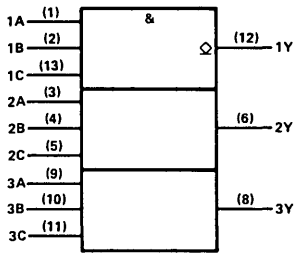
These devices contain three independent 3-input AND gates with open-collector outputs. These gates perform the boolean functions $Y = A \cdot B \cdot C$ or $Y = \overline{\overline{A}+\overline{B}+\overline{C}}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS15 is characterized for operation over the full military range of −55°C to 125°C. The SN74ALS15 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

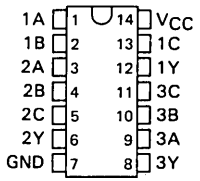
INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

logic symbol

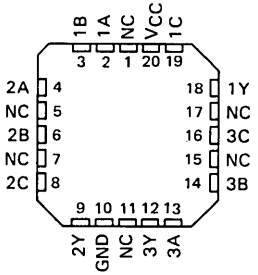


Pin numbers shown are for J and N packages.

SN54ALS15 . . . J PACKAGE
SN74ALS15 . . . N PACKAGE
(TOP VIEW)



SN54ALS15 . . . FH PACKAGE
SN74ALS15 . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS15 . . . . . −55°C to 125°C
SN74ALS15 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS15			SN74ALS15			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4				mA
							8	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS15			SN74ALS15			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_{IL} = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		1	1.8		1	1.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		1.66	3		1.66	3	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			'ALS15	SN54ALS15		SN74ALS15		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	20	23	59	23	54	ns
t_{PHL}	Any	Y	10	6	14	6	13	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

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- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

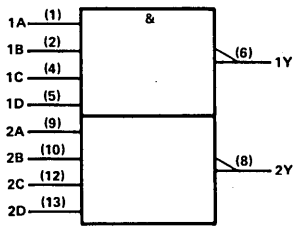
These devices contain two independent 4-input NAND gates. They perform the boolean functions $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

The SN54ALS20A is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS20A is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each gate)

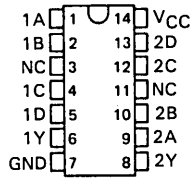
INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

logic symbol

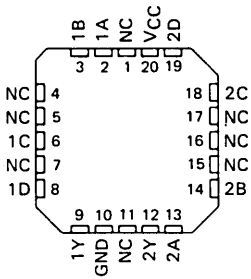


Pin numbers shown are for J and N packages.

SN54ALS20A . . . J PACKAGE
SN74ALS20A . . . N PACKAGE
(TOP VIEW)



SN54ALS20A . . . FH PACKAGE
SN74ALS20A . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS20A . . . . . −55 °C to 125 °C
SN74ALS20A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS20A			SN74ALS20A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4				mA
							8	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS20A			SN74ALS20A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4					V
	V_{CC} = 4.5 V	I_{OH} = −0.4 mA				2.7	3.4		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.22	0.4		0.22	0.4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		0.81	1.5		0.81	1.5	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25 °C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS20A	SN54ALS20A		SN74ALS20A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	4	3	13	3	11	ns
t_{PHL}	Any	Y	4	3	12	3	10	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
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- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

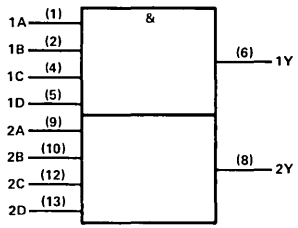
These devices contain two independent 4-input AND gates. They perform the boolean functions $Y = A \cdot B \cdot C \cdot D$ or $Y = \overline{\overline{A}+\overline{B}+\overline{C}+\overline{D}}$ in positive logic.

The SN54ALS21 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS21 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

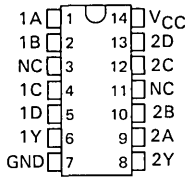
INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

logic symbol

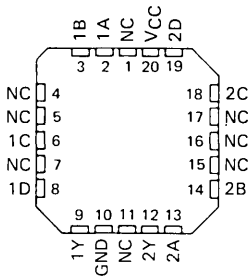


Pin numbers shown are for J and N packages.

SN54ALS21 . . . J PACKAGE
SN74ALS21 . . . N PACKAGE
(TOP VIEW)



SN54ALS21 . . . FH PACKAGE
SN74ALS21 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS21 . . . . . −55°C to 125°C
SN74ALS21 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

2

recommended operating conditions

		SN54ALS21			SN74ALS21			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4				mA
							8	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS21			SN74ALS21			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4					V
	V_{CC} = 4.5 V	I_{OH} = −0.4 mA				2.7	3.4		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_{IL} = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		0.67	1.2		0.67	1.2	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		1.1	2		1.1	2	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS21	SN54ALS21		SN74ALS21		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	12	6	30	6	26	ns
t_{PHL}	Any	Y	5	3	12	3	10	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54ALS22A, SN74ALS22A DUAL 4-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

D2661, APRIL 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

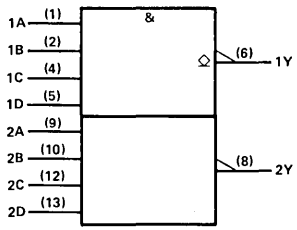
These devices contain two independent 4-input NAND gates. These gates perform the boolean functions $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS22A is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS22A is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each gate)

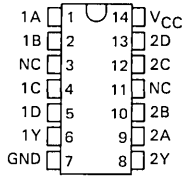
INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

logic symbol

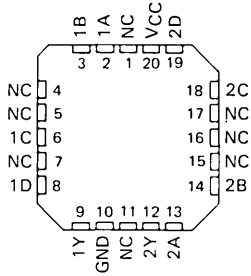


Pin numbers shown are for J and N packages.

SN54ALS22A . . . J PACKAGE
SN74ALS22A . . . N PACKAGE
(TOP VIEW)



SN54ALS22A . . . FH PACKAGE
SN74ALS22A . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS22A . . . . . −55°C to 125°C
SN74ALS22A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

2

recommended operating conditions

		SN54ALS22A			SN74ALS22A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4				mA
							8	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS22A			SN74ALS22A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_{IL} = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.22	0.4		0.22	0.4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		0.8	1.5		0.8	1.5	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			'ALS22A	SN54ALS22A		SN74ALS22A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	20	23	59	23	54	ns
t_{PHL}	Any	Y	13	6	24	6	20	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
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- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

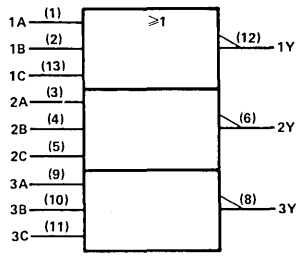
These devices contain three independent 3-input NOR gates. They perform the boolean functions $Y = \overline{A+B+C}$ or $Y = \overline{A}\cdot\overline{B}\cdot\overline{C}$ in positive logic.

The SN54ALS27 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS27 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

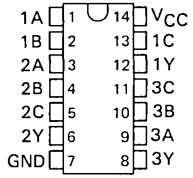
INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

logic symbol

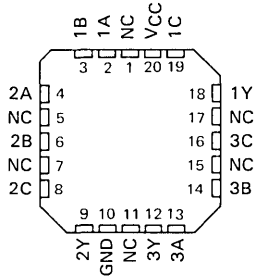


Pin numbers shown are for J and N packages.

SN54ALS27 . . . J PACKAGE
SN74ALS27 . . . N PACKAGE
(TOP VIEW)



SN54ALS27 . . . FH PACKAGE
SN74ALS27 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS27 . . . . . −55°C to 125°C
SN74ALS27 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

2

recommended operating conditions

		SN54ALS27			SN74ALS27			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4				mA
							8	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS27			SN74ALS27			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4					V
	V_{CC} = 4.5 V	I_{OH} = −0.4 mA				2.7	3.4		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_{IL} = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.97	1.8		0.97	1.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		2	4		2	4	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS27	SN54ALS27		SN74ALS27		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	9	4	22	4	15	ns
t_{PHL}	Any	Y	3	3	10	3	9	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
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- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

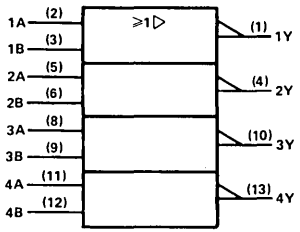
These devices contain four independent 2-input NOR buffer gates. They perform the boolean functions $Y = \overline{A+B}$ or $Y = \overline{A}\cdot\overline{B}$ in positive logic.

The SN54ALS28 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS28 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each gate)

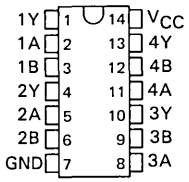
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol

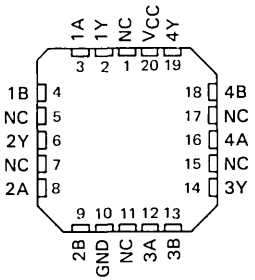


Pin numbers shown are for J and N packages.

SN54ALS28 . . . J PACKAGE
SN74ALS28 . . . N PACKAGE
(TOP VIEW)



SN54ALS28 . . . FH PACKAGE
SN74ALS28 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS28 . . . . . −55°C to 125°C
SN74ALS28 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS28			SN74ALS28			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS28			SN74ALS28			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_{IL} = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		1.7	2.8		1.7	2.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		4.8	8		4.8	8	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS28		SN74ALS28		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2	10	2	8	ns
t_{PHL}	A or B	Y	3	10	3	8	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
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POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain a single 8-input NAND gate and perform the following boolean functions in positive logic:

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H} \quad \text{OR}$$

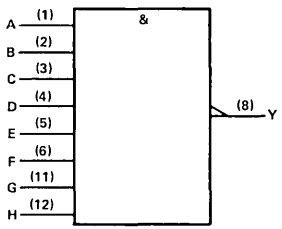
$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$$

The SN54ALS30 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS30 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

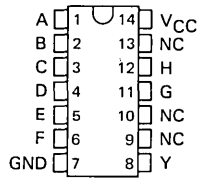
INPUTS A THRU H	OUTPUT Y
All inputs H	L
One or more inputs L	H

logic symbol

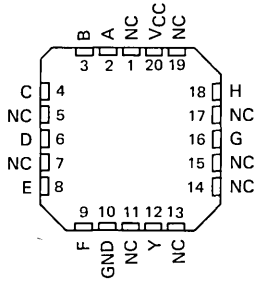


Pin numbers shown are for J and N packages.

SN54ALS30 . . . J PACKAGE
SN74ALS30 . . . N PACKAGE
(TOP VIEW)



SN54ALS30 . . . FH PACKAGE
SN74ALS30 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS30 . . . . . −55°C to 125°C
SN74ALS30 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

2

recommended operating conditions

		SN54ALS30			SN74ALS30			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4				mA
							8	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS30			SN74ALS30			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4					V
	V_{CC} = 4.5 V	I_{OH} = −0.4 mA				2.7	3.4		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_{IL} = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.22	0.36		0.22	0.36	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		0.54	0.9		0.54	0.9	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS30	SN54ALS30		SN74ALS30		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	4	3	12	3	10	ns
t_{PHL}	Any	Y	10	5	22	5	20	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
INCORPORATED
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- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

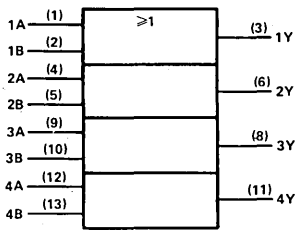
These devices contain four independent 2-input OR gates. They perform the boolean functions $Y = A+B$ or $Y = \overline{\overline{A}\cdot\overline{B}}$ in positive logic.

The SN54ALS32 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS32 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each gate)

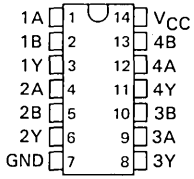
INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol

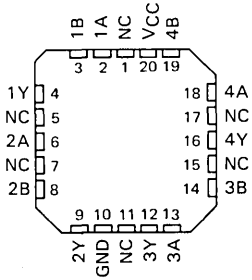


Pin numbers shown are for J and N packages.

SN54ALS32 . . . J PACKAGE
SN74ALS32 . . . N PACKAGE
(TOP VIEW)



SN54ALS32 . . . FH PACKAGE
SN74ALS32 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS32 . . . . . −55 °C to 125 °C
SN74ALS32 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

2

recommended operating conditions

		SN54ALS32			SN74ALS32			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4				mA
							8	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS32			SN74ALS32			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4					V
	V_{CC} = 4.5 V	I_{OH} = −0.4 mA				2.7	3.4		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.9	4		1.9	4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		2.6	4.9		2.6	4.9	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25 °C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS32	SN54ALS32		SN74ALS32		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	6	3	16	3	14	ns
t_{PHL}	A or B	Y	5	3	13	3	12	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
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D2661, APRIL 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

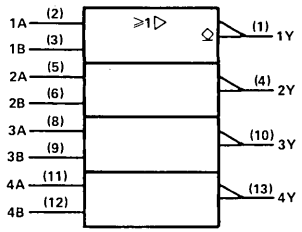
These devices contain four independent 2-input NOR buffer gates with open-collector outputs. Open-collector outputs require resistive pull-up to perform logically but can deliver higher V_{OH} levels and are commonly used in wired-AND applications. These devices perform the boolean functions $Y = \overline{A+B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN54ALS33 is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS33 is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each gate)

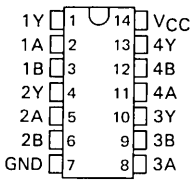
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol

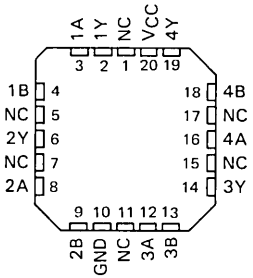


Pin numbers shown are for J and N packages.

SN54ALS33 . . . J PACKAGE
SN74ALS33 . . . N PACKAGE
(TOP VIEW)



SN54ALS33 . . . FH PACKAGE
SN74ALS33 . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS33 . . . . . −55°C to 125°C
SN74ALS33 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

2

recommended operating conditions

		SN54ALS33			SN74ALS33			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS33			SN74ALS33			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		1.7	2.8		1.7	2.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		4.8	8		4.8	8	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS33		SN74ALS33		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	10	40	10	33	ns
t_{PHL}	A or B	Y	7	21	7	18	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
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- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

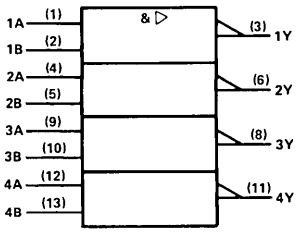
These devices contain four independent 2-input NAND buffer gates. They perform the boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54ALS37 is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS37 is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE
(each gate)

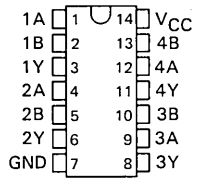
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol

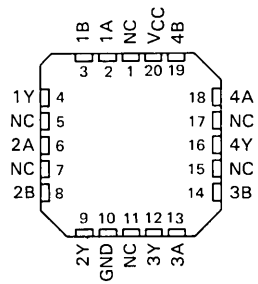


Pin numbers shown are for J and N packages.

SN54ALS37 . . . J PACKAGE
SN74ALS37 . . . N PACKAGE
(TOP VIEW)



SN54ALS37 . . . FH PACKAGE
SN74ALS37 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS37 . . . . . −55 °C to 125 °C
SN74ALS37 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS37			SN74ALS37			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS37			SN74ALS37			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_{IL} = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.86	1.6		0.86	1.6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		4	6.4		4	6.4	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS37		SN74ALS37		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2	10	2	8	ns
t_{PHL}	A or B	Y	3	10	3	8	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
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POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

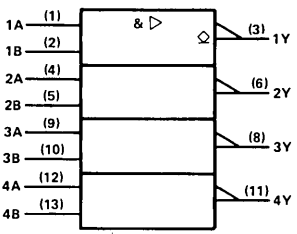
These devices contain four independent 2-input NAND buffer gates with open-collector outputs. These NAND buffers perform the boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS38 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS38 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

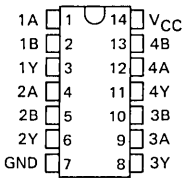
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol

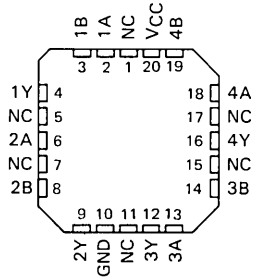


Pin numbers shown are for J and N packages.

SN54ALS38 . . . J PACKAGE
SN74ALS38 . . . N PACKAGE
(TOP VIEW)



SN54ALS38 . . . FH PACKAGE
SN74ALS38 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS38 . . . . . −55°C to 125°C
SN74ALS38 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

2

recommended operating conditions

		SN54ALS38			SN74ALS38			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS38			SN74ALS38			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_{IL} = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.86	1.6		0.86	1.6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		4	6.4		4	6.4	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS38		SN74ALS38		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	10	40	10	33	ns
t_{PHL}	A or B	Y	7	21	7	18	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
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POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

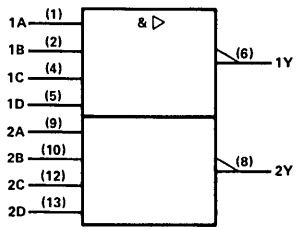
These devices contain two independent 4-input NAND buffer gates. They perform the boolean functions $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A}+\overline{B}+\overline{C}+\overline{D}$ in positive logic.

The SN54ALS40 is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS40 is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each gate)

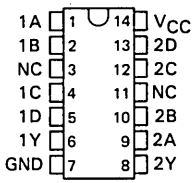
INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

logic symbol

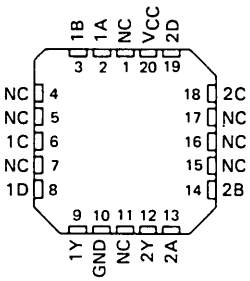


Pin numbers shown are for J and N packages.

SN54ALS40 . . . J PACKAGE
SN74ALS40 . . . N PACKAGE
(TOP VIEW)



SN54ALS40 . . . FH PACKAGE
SN74ALS40 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS40 . . . . . −55 °C to 125 °C
SN74ALS40 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS40			SN74ALS40			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS40			SN74ALS40			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_{IL} = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.43	0.8		0.43	0.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		2	3.2		2	3.2	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS40		SN74ALS40		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2	10	2	8	ns
t_{PHL}	A or B	Y	3	10	3	8	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
INCORPORATED
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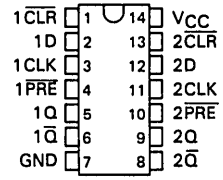
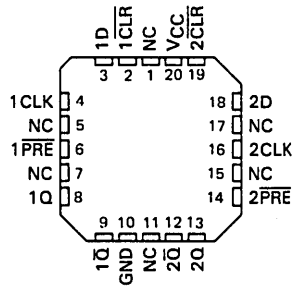
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY (C_L = 50 pF)	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'ALS74	50 MHz	6 mW
'AS74	Under development. Contact factory for latest information.	

SN54ALS74, SN54AS74 . . . J PACKAGE
SN74ALS74, SN74AS74 . . . N PACKAGE
(TOP VIEW)



SN54ALS74, SN54AS74 . . . FH PACKAGE
SN74ALS74, SN74AS74 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

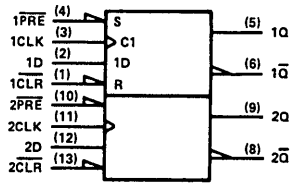
The SN54ALS74 and SN54AS74 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS74 and SN74AS74 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

*The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at Preset and Clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS74, SN54AS74 . . . . . −55°C to 125°C
SN74ALS74, SN74AS74 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS74			SN74ALS74			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4				mA
								8	
f_{clock}	Clock frequency		0		30	0		30	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	15			15			ns
		CLK high	14			12			
		CLK low	19			17			
t_{su}	Setup time before CLK↑	Data	15			15			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	10			10			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS74			SN74ALS74			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4					V
		V_{CC} = 4.5 V	I_{OH} = −0.4 mA				2.7	3.4		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	CLK or D	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	$\overline{PRE}$ or $\overline{CLR}$					0.2			0.2	
I_{IH}	CLK or D	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	CLK or D	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	$\overline{PRE}$ or $\overline{CLR}$					−0.4			−0.4	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−10		−60	−10		−60	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		2.4	4		2.4	4	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

NOTE 1: I_{CC} is measured with D, CLK, and $\overline{PRE}$ grounded, then with D, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS74			SN54ALS74		SN74ALS74		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			40	50		30		34		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$		6		3	15	3	13	ns
t_{PHL}				10		5	17	5	15	
t_{PLH}	CLK	Q or $\overline{Q}$		8		5	18	5	16	ns
t_{PHL}				12		7	20	7	18	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

ADVANCE INFORMATION

This page contains information on a new product. Specifications are subject to change without notice.

TEXAS INSTRUMENTS
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recommended operating conditions

			SN54AS74			SN74AS74			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0			0			MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↑	Data							ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive							
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS74			SN74AS74			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −2 mA	2.5	3.4		2.5	3.4		V
		V_{CC} = 4.75 V,	I_{OH} = −2 mA				2.7	3.4		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	V
I_I	CLK or D	V_{CC} = 5.5 V,	V_I = 7 V							mA
	$\overline{PRE}$ or $\overline{CLR}$									
I_{IH}	CLK or D	V_{CC} = 5.5 V,	V_I = 2.7 V							μA
	$\overline{PRE}$ or $\overline{CLR}$									
I_{IL}	CLK or D	V_{CC} = 5.5 V,	V_I = 0.4 V							mA
	$\overline{PRE}$ or $\overline{CLR}$									
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		10.5			10.5		mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Note 1: I_{CC} is measured with D, CLK, and $\overline{PRE}$ grounded, then with D, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			'AS74			SN54AS74			SN74AS74			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}							125			125		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$					4.5			4.5		ns
t_{PHL}							6			6		
t_{PLH}	CLK	Q or $\overline{Q}$					5.5			5.5		ns
t_{PHL}							6			6		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: For load circuit and voltage waveforms, see page . . . .

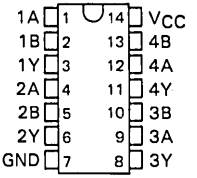
Additional information on these products can be obtained from the factory as it becomes available.

PRODUCT PREVIEW

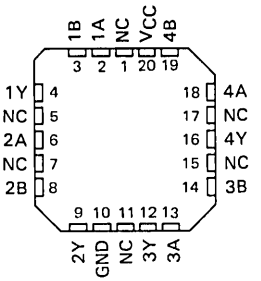
This page contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS86 . . . J PACKAGE
SN74ALS86 . . . N PACKAGE
(TOP VIEW)



SN54ALS86 . . . FH PACKAGE
SN74ALS86 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

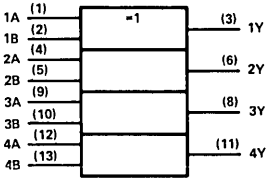
description

These devices contain four independent 2-input Exclusive-OR gates. They perform the boolean functions $Y = A \oplus B = \overline{A}B + A\overline{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

The SN54ALS86 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS86 is characterized for operation from 0°C to 70°C.

logic symbol



Pin numbers shown are for J and N packages.

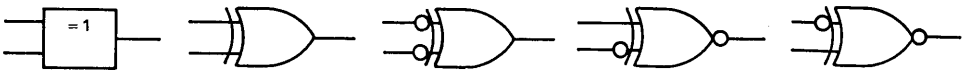
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

exclusive-OR logic

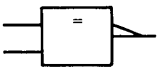
An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE-OR



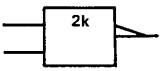
These are five equivalent Exclusive-OR symbols valid for an 'ALS86 gate in positive logic; negation may be shown at any two ports.

LOGIC IDENTITY ELEMENT



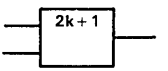
The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS86 . . . . . −55 °C to 125 °C
SN74ALS86 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS86			SN74ALS86			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4				mA
							8	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS86			SN74ALS86			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4					V
	V_{CC} = 4.5 V	I_{OH} = −0.4 mA				2.7	3.4		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_{IL} = 0.4 V			−0.1			−0.1	mA
I_O §	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V,	All inputs at 0 V							mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25 °C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX					UNIT
			'ALS86	SN54ALS86			SN74ALS86		
			TYP‡	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y								ns
t_{PHL}	(other input low)									
t_{PLH}	A or B	Y								ns
t_{PHL}	(other input high)									

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.
Additional information on these products can be obtained from the factory as it becomes available.

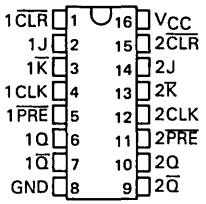
TYPES SN54ALS109, SN54AS109, SN74ALS109, SN74AS109
DUAL J-$\overline{K}$ POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

D2661, APRIL 1982

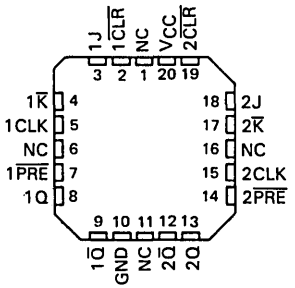
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'ALS109	50 MHz	6 mW
'AS109	Under development. Contact factory for latest information.	

SN54ALS109, SN54AS109 . . . J PACKAGE
SN74ALS109, SN74AS109 . . . N PACKAGE
(TOP VIEW)



SN54ALS109, SN54AS109 . . . FH PACKAGE
SN74ALS109, SN74AS109 . . . FN PACKAGE
(TOP VIEW)



NC – No Internal connection

description

These devices contain two independent J-$\overline{K}$ positive-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and $\overline{K}$ inputs meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and $\overline{K}$ inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding $\overline{K}$ and tying J high. They also can perform as D-type flip-flops if J and $\overline{K}$ are tied together.

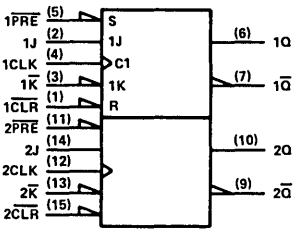
The SN54ALS109 and SN54AS109 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS109 and SN74AS109 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

*The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at Preset and Clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when Preset or Clear return to their inactive (high) level.

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS109, SN54AS109 . . . . . −55 °C to 125 °C
SN74ALS109, SN74AS109 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

			SN54ALS109			SN74ALS109			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4				mA
								8	
f_{clock}	Clock frequency		0		30	0		34	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	15			14.5			ns
		CLK high	16.5			14.5			
		CLK low	16.5			17			
t_{su}	Setup time before CLK↑	Data	15			15			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	10			10			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS109			SN74ALS109			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4					V
		V_{CC} = 4.5 V	I_{OH} = −0.4 mA				2.7	3.4		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	CLK, J, or $\overline{K}$	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	$\overline{PRE}$ or $\overline{CLR}$					0.2			0.2	
I_{IH}	CLK, J, or $\overline{K}$	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	CLK, J, or $\overline{K}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	$\overline{PRE}$ or $\overline{CLR}$					−0.4			−0.4	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−10		−60	−10		−60	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		2.4	4		2.4	4	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with J, $\overline{K}$, CLK, and $\overline{PRE}$ grounded, then with J, $\overline{K}$, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS109			SN54ALS109		SN74ALS109		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			40	50		30		34		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$		6		3	15	3	13	ns
t_{PHL}				10		5	17	5	15	
t_{PLH}	CLK	Q or $\overline{Q}$		8		5	18	5	16	ns
t_{PHL}				12		7	20	7	18	

NOTE 2: For load circuit and voltage waveforms, see page 1-12.

recommended operating conditions

			SN54AS109			SN74AS109			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0			0			MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↑	Data							ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive							
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS109			SN74AS109			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −2 mA	2.5	3.4		2.5	3.4		V
		V_{CC} = 4.75 V,	I_{OH} = −2 mA				2.7	3.4		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	V
I_I	CLK or D	V_{CC} = 5.5 V,	V_I = 7 V							mA
	$\overline{PRE}$ or $\overline{CLR}$									
I_{IH}	CLK or D	V_{CC} = 5.5 V,	V_I = 2.7 V							μA
	$\overline{PRE}$ or $\overline{CLR}$									
I_{IL}	CLK or D	V_{CC} = 5.5 V,	V_I = 0.4 V							mA
	$\overline{PRE}$ or $\overline{CLR}$									
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		11.5			11.5		mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Note 1: I_{CC} is measured with D, CLK, and $\overline{PRE}$ grounded, then with D, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			'AS109			SN54AS109			SN74AS109			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}							125			125		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$					4.5			4.5		ns
t_{PHL}							6			6		
t_{PLH}	CLK	Q or $\overline{Q}$					6			6		ns
t_{PHL}							6			6		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

TEXAS INSTRUMENTS
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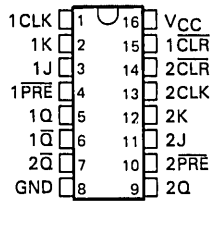
TYPES SN54ALS112A, SN54AS112, SN74ALS112A, SN74AS112
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

D2661, DECEMBER 1982

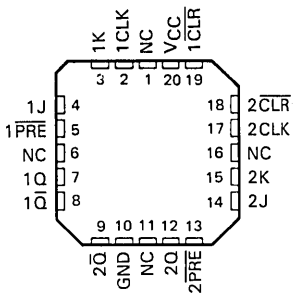
- Fully Buffered to Offer Maximum Isolation from External Disturbance
- Package Options Include Both Plastic and Ceramic Carriers in Addition to Plastic and Ceramic DIPs.
- Dependable Texas Instruments Quality and Reliability

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'ALS112A	50 MHz	6 mW
'AS112	175 MHz	95 mW

SN54ALS112A, SN54AS112 . . . J PACKAGE
SN74ALS112A, SN74AS112 . . . N PACKAGE
(TOP VIEW)



SN54ALS112A, SN54AS112 . . . FH PACKAGE
SN74ALS112A, SN74AS112 . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

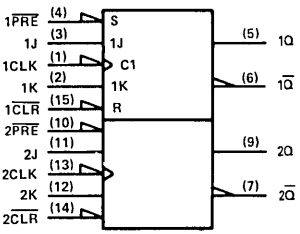
The SN54ALS112A and SN54AS112 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS112A and SN74AS112 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

*The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at Preset and Clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS112A, SN54AS112 . . . . . −55°C to 125°C
SN74ALS112A, SN74AS112 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

			SN54ALS112A			SN74ALS112A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		50	0		50	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	15			10			ns
		CLK high	20			16.5			
		CLK low	20			16.5			
t_{su}	Setup time before CLK↓	Data	25			22			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	22			20			
t_h	Hold time, data after CLK↓		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS112A			SN74ALS112A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = 0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	$\overline{PRE}$ or $\overline{CLR}$					0.2			0.2	
I_{IH}	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	$\overline{PRE}$ or $\overline{CLR}$					−0.4			−0.4	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		2.5	4.5		2.5	4.5	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with outputs open and J, K, CLK, and $\overline{PRE}$ grounded, then with J, K, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			'ALS112A			SN54ALS112A			SN74ALS112A			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			35	40		25			30			MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$		8		3		20	3		15	ns
t_{PHL}				13		4		22	4		18	
t_{PLH}	CLK	Q or $\overline{Q}$		8		3		18	3		15	ns
t_{PHL}				13		5		23	5		19	

NOTE 2: For load circuit and voltage waveforms, see page 1-12.

recommended operating conditions

			SN54AS112			SN74AS112			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0			0			MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↓	Data							ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive							
t_h	Hold time, data after CLK↓								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS112			SN74AS112			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −2 mA	2.5	3.4		2.5	3.4		V
		V_{CC} = 4.75 V,	I_{OH} = −2 mA				2.7	3.4		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	V
		V_{CC} = 4.75 V,	I_{OL} = 20 mA					0.25	0.5	
I_I	J or K	V_{CC} = 5.5 V,	V_I = 7 V							mA
	$\overline{PRE}$ or $\overline{CLR}$									
	CLK									
I_{IH}	J or K	V_{CC} = 5.5 V,	V_I = 2.7 V							μA
	$\overline{PRE}$ or $\overline{CLR}$									
	CLK									
I_{IL}	J or K	V_{CC} = 5.5 V,	V_I = 0.4 V		−1			−1		mA
	$\overline{PRE}$ or $\overline{CLR}$				−5.5			−5.5		
	CLK				−5			−5		
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		38			38		mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

NOTE 1: I_{CC} is measured with J, K, CLK, and $\overline{PRE}$ grounded, then with J, K, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			'AS112			SN54AS112			SN74AS112			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}				200			175			175		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$		2			3			3		ns
t_{PHL}				3			4			4		
t_{PLH}	CLK	Q or $\overline{Q}$		2			3			3		ns
t_{PHL}				3.5			4			4		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

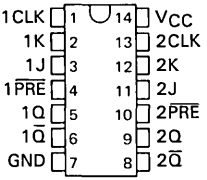
TYPES SN54ALS113A, SN54AS113, SN74ALS113A, SN74AS113
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

D2261, DECEMBER 1982

- **Fully Buffered to Offer Maximum Isolation from External Disturbance**
- **Package Options Include Both Plastic and Ceramic Carriers in Addition to Plastic and Ceramic DIPs.**
- **Dependable Texas Instruments Quality and Reliability**

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'ALS113A	40 MHz (C_L = 15 pF)	6 mW
'AS113	175 MHz (C_L = 50 pF)	95 mW

SN54ALS113A, SN54AS113 . . . J PACKAGE
SN74ALS113A, SN74AS113 . . . N PACKAGE
(TOP VIEW)

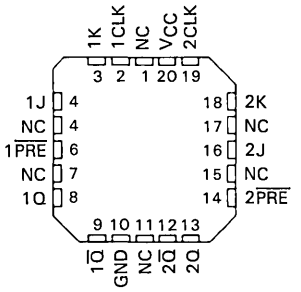


description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset input sets the outputs regardless of the levels of the other inputs. When Preset ($\overline{PRE}$) is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54ALS113A and SN54AS113 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS113A and SN74AS113 are characterized for operation from 0°C to 70°C.

SN54ALS113A, SN54AS113 . . . FH PACKAGE
SN74ALS113A, SN74AS113 . . . FN PACKAGE
(TOP VIEW)

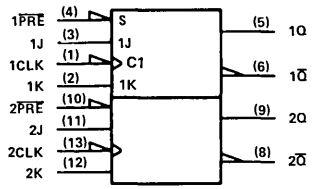


NC — No internal connection

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS113A, SN54AS113 . . . . . −55°C to 125°C
SN74ALS113A, SN74AS113 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

			SN54ALS113A			SN74ALS113A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		25	0		30	MHz
t_w	Pulse duration	PRE low	15			10			ns
		CLK high	20			16.5			
		CLK low	20			16.5			
t_{su}	Setup time before CLK↓	Data	25			22			ns
		PRE inactive	22			20			
t_h	Hold time, data after CLK↓		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS113A			SN74ALS113A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = 0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	$\overline{PRE}$					0.2			0.2	
I_{IH}	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{PRE}$					40			40	
I_{IL}	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	$\overline{PRE}$					−0.4			−0.4	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		2.5	4.5		2.5	4.5	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with J, K, CLK, and $\overline{PRE}$ grounded, then with J, K, and CLK grounded.

switching characteristics (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS113A			SN54ALS113A		SN74ALS113A		
			MIN	TYP‡	MAX	MIN	MAX	MIN	MAX	
f_{max}			35	40		25		30		MHz
t_{PLH}	$\overline{PRE}$	Q or $\overline{Q}$		8		3	17	3	14	ns
t_{PHL}				13		4	20	4	16	
t_{PLH}	CLK	Q or $\overline{Q}$		8		3	18	3	15	ns
t_{PHL}				13		5	23	5	19	

NOTE 2: For load circuit and voltage waveforms, see page 1-12.

recommended operating conditions

			SN54AS113			SN74AS113			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0			0			MHz
t_w	Pulse duration	$\overline{PRE}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↓	Data							ns
		$\overline{PRE}$ inactive							
t_h	Hold time, data after CLK↓								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS113			SN74AS113			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −2 mA	2.5	3.4		2.5	3.4		V
		V_{CC} = 4.75 V,	I_{OH} = −2 mA				2.7	3.4		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	V
		V_{CC} = 4.75 V,	I_{OL} = 20 mA					0.25	0.5	
I_I	J or K	V_{CC} = 5.5 V,	V_I = 7 V							mA
	$\overline{PRE}$									
	CLK									
I_{IH}	J or K	V_{CC} = 5.5 V,	V_I = 2.7 V							μA
	$\overline{PRE}$									
	CLK									
I_{IL}	J or K	V_{CC} = 5.5 V,	V_I = 0.4 V		−1			−1		mA
	$\overline{PRE}$				−5.5			−5.5		
	CLK				−5			−5		
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		38			38		mA

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with J, K, CLK, and $\overline{PRE}$ grounded, then with J, K, and CLK grounded.

switching characteristics (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			'AS113			SN54AS113			SN74AS113			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}				200			175			175		MHz
t_{PLH}	$\overline{PRE}$	Q or $\overline{Q}$		2			3			3		ns
t_{PHL}				3			4			4		
t_{PLH}	CLK	Q or $\overline{Q}$		2			3			3		ns
t_{PHL}				3.5			4			4		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: For load circuit and voltage waveforms, see page 1-12.
Additional information on these products can be obtained from the factory as it becomes available.

PRODUCT PREVIEW

 This page contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
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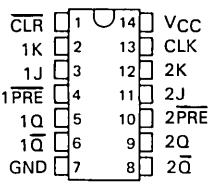
TYPES SN54ALS114A, SN54AS114, SN74ALS114A, SN74AS114
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

D2661, DECEMBER 1982

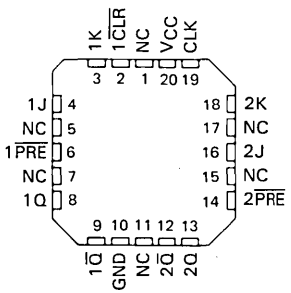
- Fully Buffered to Offer Maximum Isolation from External Disturbance
- Package Options Include Both Plastic and Ceramic Carriers in Addition to Plastic and Ceramic DIPs.
- Dependable Texas Instruments Quality and Reliability

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'ALS114A	40 MHz (C_L = 15 pF)	6 mW
'AS114	175 MHz (C_L = 50 pF)	95 mW

SN54ALS114A, SN54AS114 . . . J PACKAGE
SN74ALS114A, SN74AS114 . . . N PACKAGE
(TOP VIEW)



SN54ALS114A, SN54AS114 . . . FH PACKAGE
SN74ALS114A, SN74AS114 . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

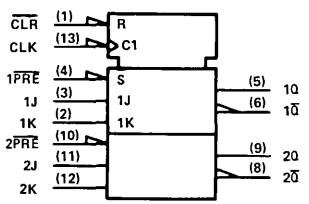
The SN54ALS114A and SN54AS114 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS114A and SN74AS114 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

* The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at Preset and Clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS114A, SN54AS114 . . . . . −55°C to 125°C
SN74ALS114A, SN74AS114 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS114A			SN74ALS114A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		25	0		30	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	15			10			ns
		CLK high	20			16.5			
		CLK low	20			16.5			
t_{su}	Setup time before CLK↓	Data	25			22			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	22			20			
t_h	Hold time, data after CLK↓		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS114A			SN74ALS114A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	$\overline{PRE}$ or $\overline{CLR}$					0.2			0.2	
I_{IH}	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	$\overline{PRE}$ or $\overline{CLR}$					−0.4			−0.4	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		2.5	4.5		2.5	4.5	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with J, K, CLK, and PRE grounded, then with J, K, CLK, and CLR grounded.

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switching characteristics (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS114A			SN54ALS114A		SN74ALS114A		
			MIN	TYP‡	MAX	MIN	MAX	MIN	MAX	
f_{max}			35	40		25		30		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$		8		3	20	3	15	ns
t_{PHL}				13		4	22	4	18	
t_{PLH}	CLK	Q or $\overline{Q}$		8		3	18	3	15	ns
t_{PHL}				13		5	23	5	19	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: For load circuit and voltage waveforms, see page 1-12.

recommended operating conditions

			SN54AS114			SN74AS114			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0			0			MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↓	Data							ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive							
t_h	Hold time, data after CLK↓								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS114			SN74AS114			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −2 mA	2.5	3.4		2.5	3.4		V
		V_{CC} = 4.75 V,	I_{OH} = −2 mA				2.7	3.4		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.75 V,	I_{OL} = 20 mA					0.35	0.5	
I_I	J or K	V_{CC} = 5.5 V,	V_I = 7 V							mA
	$\overline{PRE}$									
	$\overline{CLR}$									
	CLK									
I_{IH}	J or K	V_{CC} = 5.5 V,	V_I = 2.7 V							μA
	$\overline{PRE}$									
	$\overline{CLR}$									
	CLK									
I_{IL}	J or K	V_{CC} = 5.5 V,	V_I = 0.4 V		−1			−1		mA
	$\overline{PRE}$				−5.5			−5.5		
	$\overline{CLR}$				−11.5			−11.5		
	CLK				−10.5			−10.5		
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		38			38		mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

NOTE 1: I_{CC} is measured with J, K, CLK, and $\overline{PRE}$ grounded, then with J, K, CLK, and $\overline{CLR}$ grounded.

Additional information on these products can be obtained from the factory as it becomes available.

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POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

switching characteristics (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			'AS114			SN54AS114			SN74AS114			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}				200			175			175		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$		2			3			3		ns
t_{PHL}				3			4			4		
t_{PLH}	CLK	Q or $\overline{Q}$		2			3			3		ns
t_{PHL}				3.5			4			4		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: For load circuit and voltage waveforms, see page 1-12.

- **Combines Decoder and 3-Bit Address Register**
- **Incorporates 2 Enable Inputs to Simplify Cascading**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

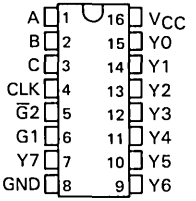
2

description

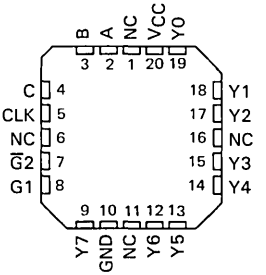
The 'ALS131 is a three-line to eight-line decoder/demultiplexer with registers on the three address inputs. When the clock input (CLK) goes from low to high, the 'ALS131 acts as a decoder/demultiplexer and the address present at the select inputs (A, B, and C) is stored in the registers. Further address changes are ignored until the next rising transition of CLK. The output enable controls, G1 and $\overline{G}2$, control the state of the outputs independently of the select or CLK inputs. All of the outputs are high unless G1 is high and $\overline{G}2$ is low. The 'ALS131 is ideally suited for implementing qlitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

The SN54ALS131 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS131 is characterized for operation from 0°C to 70°C.

SN54ALS131 . . . J PACKAGE
SN74ALS131 . . . N PACKAGE
(TOP VIEW)

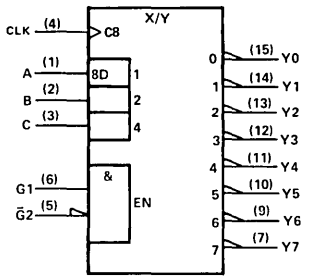


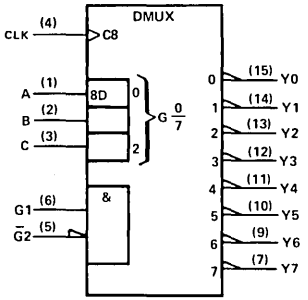
SN54ALS131 . . . FH PACKAGE
SN74ALS131 . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

logic symbols (alternatives)





Pin numbers shown are for J and N packages.

TEXAS INSTRUMENTS
INCORPORATED
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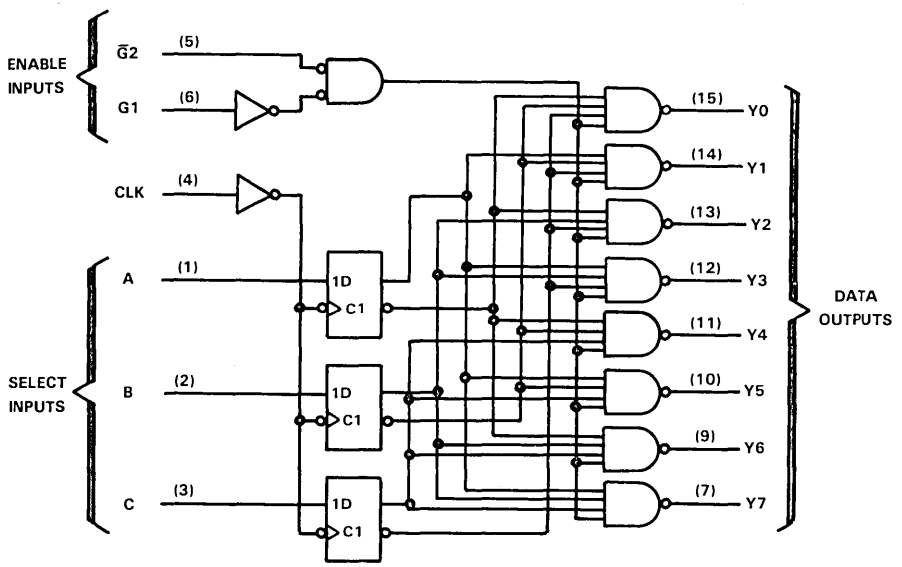
logic diagram (positive logic)



Pin numbers shown are for J and N packages.

FUNCTION TABLE

INPUTS						OUTPUTS							
CLK	ENABLE		SELECT										
	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
↑	H	L	L	L	L	L	H	H	H	H	H	H	H
↑	H	L	L	L	H	H	L	H	H	H	H	H	H
↑	H	L	L	H	L	H	H	L	H	H	H	H	H
↑	H	L	L	H	H	H	H	H	L	H	H	H	H
↑	H	L	H	L	L	H	H	H	H	L	H	H	H
↑	H	L	H	L	H	H	H	H	H	H	L	H	H
↑	H	L	H	H	L	H	H	H	H	H	H	L	H
↑	H	L	H	H	H	H	H	H	H	H	H	H	L
L or H	H	L	X	X	X	OUTPUTS CORRESPONDING TO STORED ADDRESS, L; ALL OTHERS, H							

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS131 . . . . . −55 °C to 125 °C
SN74ALS131 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS131			SN74ALS131			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4				mA
								8	
f_{clock}	Clock frequency		0		40	0		50	MHz
t_w	Pulse duration	CLK high	12.5			10			ns
		CLK low	12.5			10			
t_{su}	Setup time at A, B, and C before CLK↑		15			10			ns
t_h	Hold time at A, B, and C after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS131			SN74ALS131			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4					V
	V_{CC} = 4.5 V	I_{OH} = −0.4 mA				2.7	3.4		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			5	11		5	11	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS131			SN54ALS131		SN74ALS131		
			MIN	TYP‡	MAX	MIN	MAX	MIN	MAX	
f_{max}			60	70		40		50		MHz
t_{PLH}	CLK	Y		10		8	28	8	25	ns
t_{PHL}				7		7	24	7	20	
t_{PLH}	G1	Y		10		7	24	7	20	ns
t_{PHL}				10		6	20	6	17	
t_{PLH}	$\overline{G2}$	Y		7		5	18	5	15	ns
t_{PHL}				7		5	18	5	15	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
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- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain a single 13-input NAND gate. They perform the boolean functions in positive logic:

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M}$$

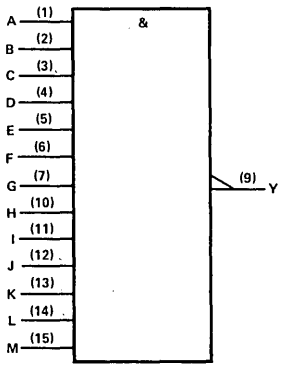
$$Y = \overline{A}+\overline{B}+\overline{C}+\overline{D}+\overline{E}+\overline{F}+\overline{G}+\overline{H}+\overline{I}+\overline{J}+\overline{K}+\overline{L}+\overline{M}$$

The SN54ALS133 is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS133 is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE

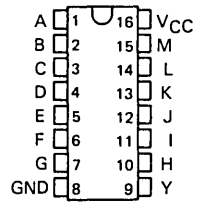
INPUTS A THRU M	OUTPUT Y
All inputs H	L
One or more inputs L	H

logic symbol

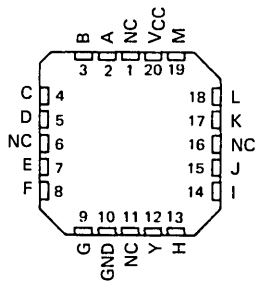


Pin numbers shown are for J and N packages.

SN54ALS133 . . . J PACKAGE
SN74ALS133 . . . N PACKAGE
(TOP VIEW)



SN54ALS133 . . . FH PACKAGE
SN74ALS133 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS133 . . . . . −55°C to 125°C
SN74ALS133 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS133			SN74ALS133			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4				mA
							8	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS133			SN74ALS133			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4					V
	V_{CC} = 4.5 V	I_{OH} = −0.4 mA				2.7	3.4		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_{IL} = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.24	0.34		0.24	0.34	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		0.56	0.8		0.56	0.8	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS133	SN54ALS133		SN74ALS133		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	6	3	14	3	11	ns
t_{PHL}	Any	Y	10	5	28	5	25	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
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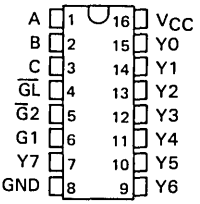
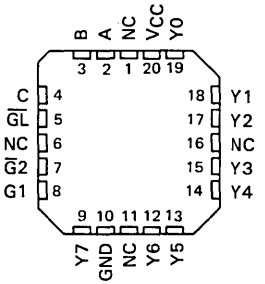
- **Combines Decoder and 3-Bit Address Latch**
- **Incorporates 2 Output Enables to Simplify Cascading**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS137 . . . J PACKAGE
SN74ALS137 . . . N PACKAGE
(TOP VIEW)



SN54ALS137 . . . FH PACKAGE
SN74ALS137 . . . FN PACKAGE
(TOP VIEW)



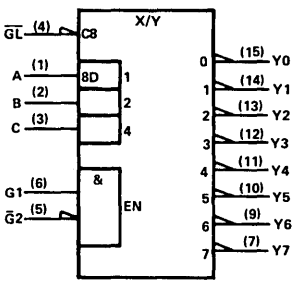
NC – No internal connection

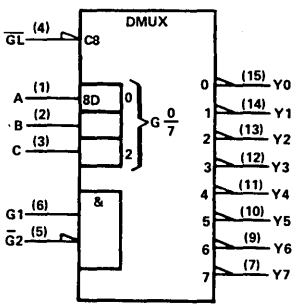
description

The 'ALS137 is a three-line to eight-line decoder/demultiplexer with latches on the three address inputs. When the latch-enable input ($\overline{GL}$) is low, the 'ALS137 acts as a decoder/demultiplexer. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B, and C) is stored in the latches. Further address changes are ignored as long as $\overline{GL}$ remains high. The output enable controls, G1 and $\overline{G2}$, control the outputs independently of the select or latch-enable inputs. All of the outputs are forced high if G1 is low or $\overline{G2}$ is high. The 'ALS137 is ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

The SN54ALS137 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS137 is characterized for operation from 0°C to 70°C.

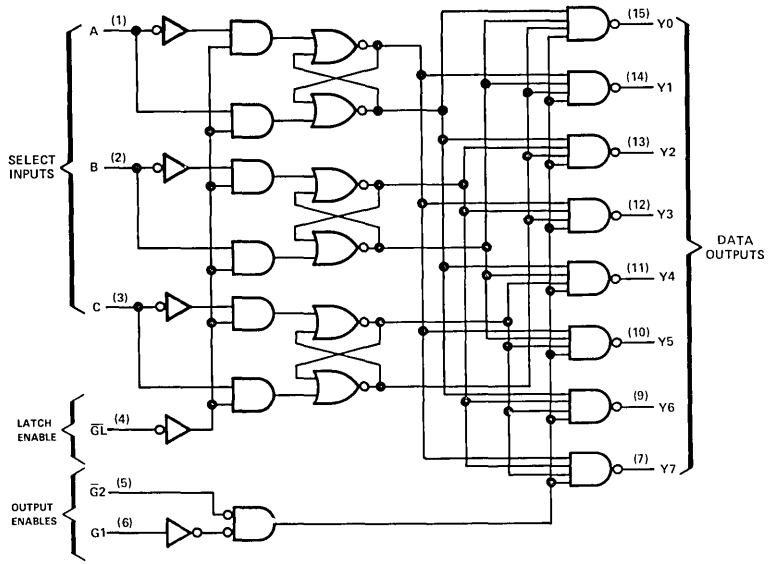
logic symbols (alternatives)





Pin numbers shown are for J and N packages.

logic diagram (positive logic)



Pin numbers shown are for J and N packages.

FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{G}L$	G1	$\overline{G}2$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address, L; all others, H							

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS137 . . . . . −55 °C to 125 °C
SN74ALS137 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS137			SN74ALS137			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4				mA
							8	
t_w	Pulse duration, $\overline{GL}$ low	15			10			ns
t_{su}	Setup time, A, B, and C before $\overline{GL}$↑	15			10			ns
t_h	Hold time, A, B, and C after $\overline{GL}$↑	5			5			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS137			SN74ALS137			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4					V
		V_{CC} = 4.5 V	I_{OH} = −0.4 mA				2.7	3.4		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	Enable	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A, B, C					0.2			0.2	
I_{IH}	Enable	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A, B, C					40			40	
I_{IL}	Enable	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A, B, C					−0.2			−0.2	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			5	11		5	11	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25 °C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS137	SN54ALS137		SN74ALS137		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C	Y	10.5	5	25	5	20	ns
t_{PHL}			11.5	6	25	6	20	
t_{PLH}	$\overline{G2}$	Y	7.5	4	15	4	12	ns
t_{PHL}			7.5	5	18	5	15	
t_{PLH}	G1	Y	10	5	21	5	17	ns
t_{PHL}			10	5	19	5	15	
t_{PLH}	$\overline{GL}$	Y	13	7	27	7	22	ns
t_{PHL}			13	7	25	7	20	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporates 3 Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

2

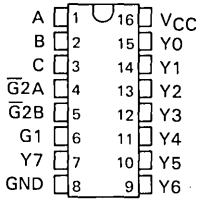
description

The 'ALS138 circuit is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

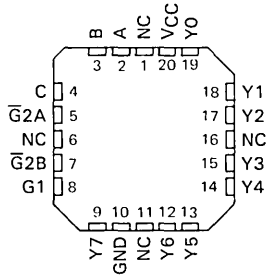
The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The SN54ALS138 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS138 is characterized for operation from 0°C to 70°C.

SN54ALS138 . . . J PACKAGE
SN74ALS138 . . . N PACKAGE
(TOP VIEW)

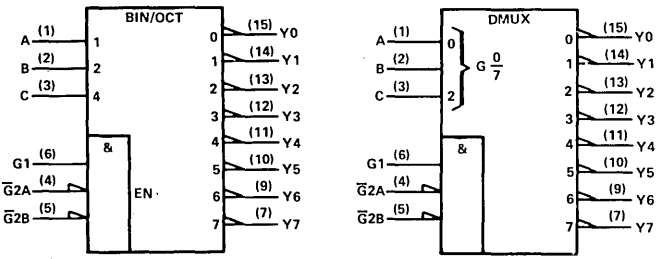


SN54ALS138 . . . FH PACKAGE
SN74ALS138 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbols (alternatives)



Pin numbers shown are for J and N packages.

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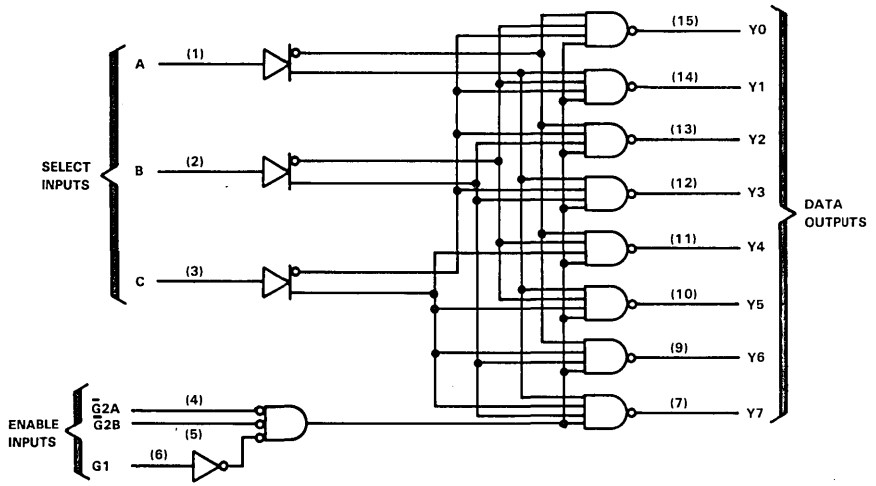
logic diagram (positive logic)



Pin numbers shown are for J and N packages.

FUNCTION TABLE

ENABLE INPUTS		SELECT INPUTS			OUTPUTS							
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*$\overline{G2} = \overline{G2A} + \overline{G2B}$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS138 . . . . . −55 °C to 125 °C
SN74ALS138 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS138			SN74ALS138			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4				mA
							8	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS138			SN74ALS138			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4					V
	V_{CC} = 4.5 V	I_{OH} = −0.4 mA				2.7	3.4		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_{IL} = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			5	10		5	10	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS138	SN54ALS138		SN74ALS138		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C	Any Y	9	6	27	6	22	ns
t_{PHL}			8	6	22	6	18	
t_{PLH}	Enable	Any Y	9	4	20	4	17	ns
t_{PHL}			9	5	20	5	17	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

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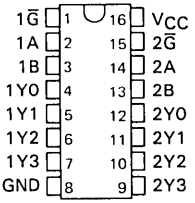
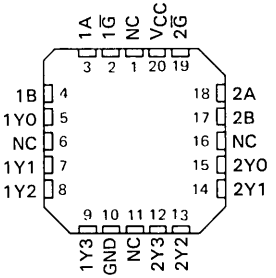
- Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems
- Incorporates 2 Enable Inputs to Simplify Cascading and/or Data Reception
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS139 . . . J PACKAGE
SN74ALS139 . . . N PACKAGE
(TOP VIEW)



SN54ALS139 . . . FH PACKAGE
SN74ALS139 . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

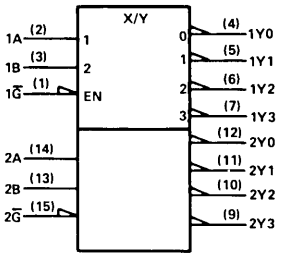
description

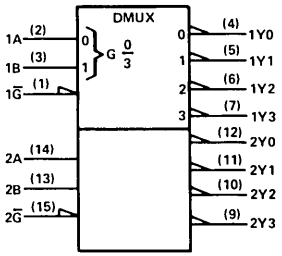
The 'ALS139 circuit is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast-enable circuit,the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The 'ALS139 is comprised of two individual two-line to four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

The SN54ALS139 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS139 is characterized for operation from 0°C to 70°C.

logic symbols (alternatives)





Pin numbers shown are for J and N packages

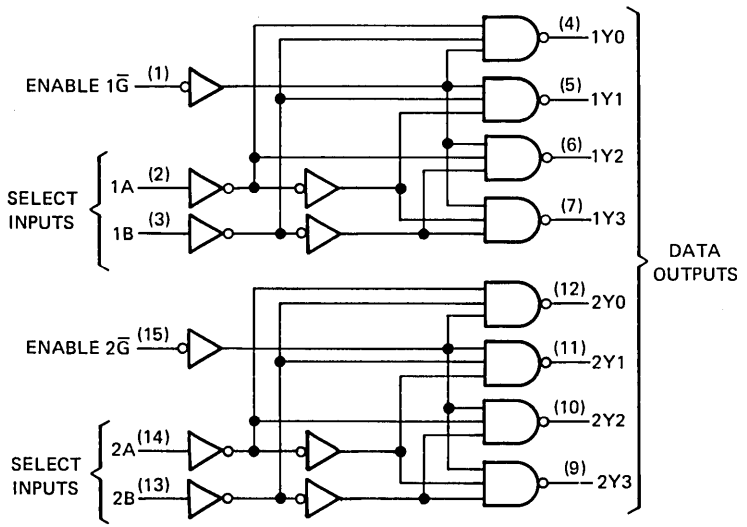
PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

FUNCTION TABLE

INPUTS			OUTPUTS			
ENABLE	SELECT					
$\overline{G}$	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

functional block diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS139 . . . . . −55°C to 125°C
SN74ALS139 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

TEXAS INSTRUMENTS
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recommended operating conditions

		SN54ALS139			SN74ALS139			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4				mA
							8	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS139			SN74ALS139			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4					V
	V_{CC} = 4.5 V	I_{OH} = −0.4 mA				2.7	3.4		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_{IL} = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V								mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			'ALS139			SN54ALS139			SN74ALS139			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y										ns
t_{PHL}												
t_{PLH}	$\overline{G}$	Y										ns
t_{PHL}												

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

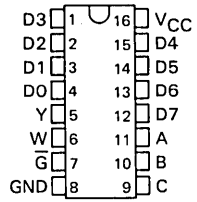
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

- 3-Line to 1-Line Multiplexers
  Can Perform As:
  - Boolean Function Generators
  - Parallel-to-Serial Converters
  - Data Source Selectors
- Input Clamping Diodes Simplify System Design
- Fully Compatible With Most TTL Circuits
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

2

SN54ALS151, SN54AS151 . . . J PACKAGE
SN74ALS151, SN74AS151 . . . N PACKAGE
(TOP VIEW)

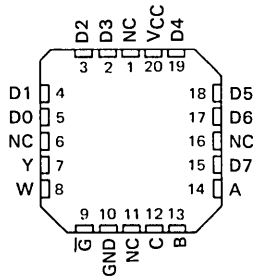


description

These monolithic data selectors/multiplexers provide full binary decoding to select one of eight data sources. The strobe input ($\overline{G}$) must be at a low logic level to enable the inputs. A high level at the strobe terminal forces the W output high and the Y output low.

The SN54ALS151 and SN54AS151 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS151 and SN74AS151 are characterized for operation from 0°C to 70°C.

SN54ALS151, SN54AS151 . . . FH PACKAGE
SN74ALS151, SN74AS151 . . . FN PACKAGE
(TOP VIEW)



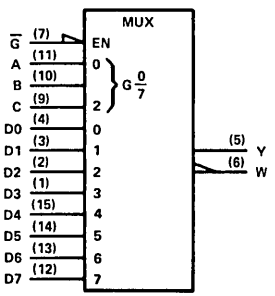
NC—No internal connection

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	$\overline{G}$	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high level, L = low level, X = irrelevant
D0, D1 . . . D7 = the level of the D respective input

logic symbol



Pin numbers shown are for J and N packages.

TEXAS INSTRUMENTS
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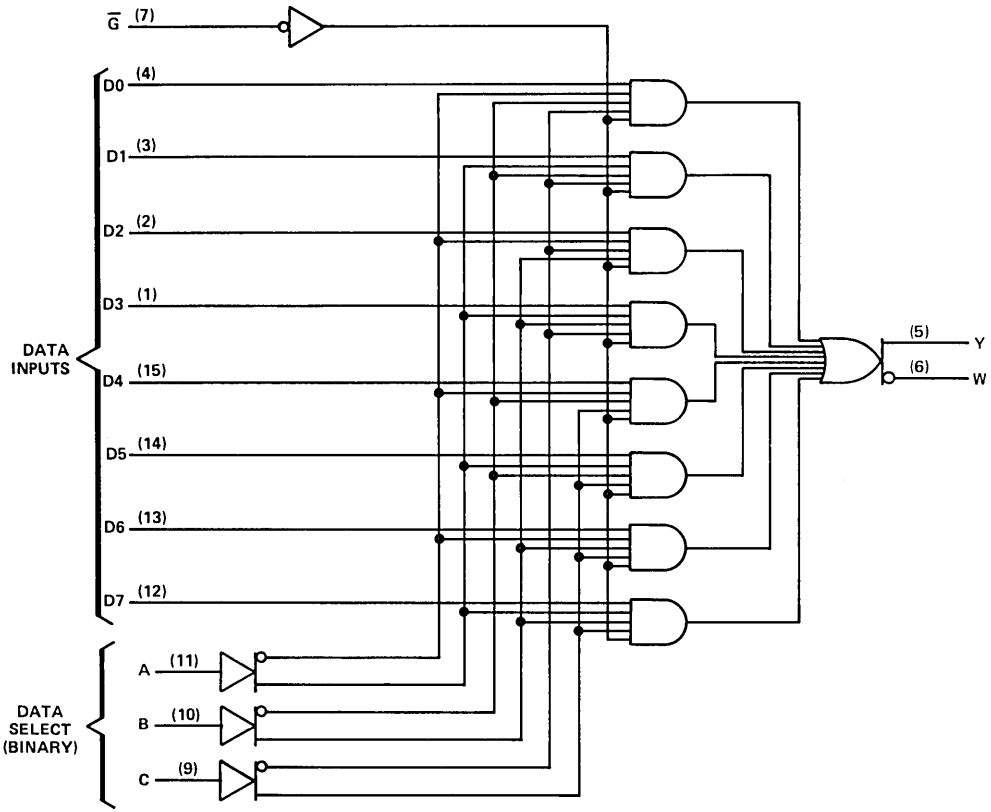
logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS151, SN54AS151 . . . . . −55 °C to 125 °C
SN74ALS151, SN74AS151 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150°C

recommended operating conditions

		SN54ALS151			SN74ALS151			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4				mA
							8	
T_A	Operating free-air temperature	−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS151			SN74ALS151			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4					V
	V_{CC} = 4.5 V	I_{OH} = −0.4 mA				2.7	3.4		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V,	Inputs at 4.5 V		6			6		mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX					UNIT
			'ALS151	SN54ALS151			SN74ALS151		
			TYP‡	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, or C	Y			7.5			7.5		ns
t_{PHL}					9			9		
t_{PLH}	A, B, or C	W			9			9		ns
t_{PHL}					9.5			9.5		
t_{PLH}	Any D	Y			4			4		ns
t_{PHL}					6			6		
t_{PLH}	Any D	W			6			6		ns
t_{PHL}					6			6		
t_{PLH}	$\overline{G}$	Y			4			4		ns
t_{PHL}					5			5		
t_{PLH}	$\overline{G}$	W			4			4		ns
t_{PHL}					5			5		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.
Additional information on these products can be obtained from the factory as it becomes available.

recommended operating conditions

		SN54AS151			SN74AS151			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−12	mA
							−15†	
I_{OL}	Low-level output current			32			32	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS151			SN74AS151			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2		2.4	3.2		V
		V_{CC} = 4.75 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5		0.25	0.5	V
		V_{CC} = 4.75 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	A, B	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	A, B	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	A, B	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.6			−0.6		mA
	All others				−0.3			−0.3		
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,			26			26		mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX					UNIT
			AS151	SN54AS151			SN74AS151		
			TYP‡	MIN	TYP‡	MAX	MIN	TYP‡	MAX
t_{PLH}	A, B, or C	Y			5			5		ns
t_{PHL}					5			5		
t_{PLH}	A, B, or C	W			4.5			4.5		ns
t_{PHL}					4.5			4.5		
t_{PLH}	Any D	Y			3			3		ns
t_{PHL}					4			4		
t_{PLH}	Any D	W			3			3		ns
t_{PHL}					2.5			2.5		
t_{PLH}	$\overline{G}$	Y			5			5		ns
t_{PHL}					5			5		
t_{PLH}	$\overline{G}$	W			4.5			4.5		ns
t_{PHL}					4.5			4.5		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

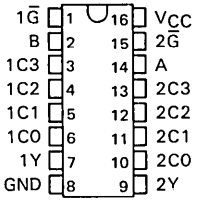
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

D2661, APRIL 1982

- Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N lines to n lines)
- Fully Compatible with Most TTL Circuits
- 'ALS253 and 'AS253 Are 3-State Versions of These Parts
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS153, SN54AS153 . . . J PACKAGE
SN74ALS153, SN74AS153 . . . N PACKAGE
(TOP VIEW)

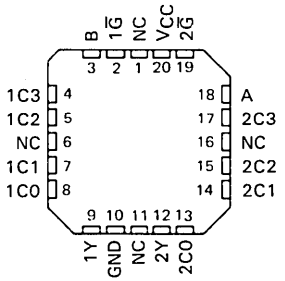


description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate strobe inputs (G) are provided for each of the two four-line sections.

The SN54ALS153 and SN54AS153 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS153 and SN74AS153 are characterized for operation from 0°C to 70°C.

SN54ALS153, SN54AS153 . . . FH PACKAGE
SN74ALS153, SN74AS153 . . . FN PACKAGE
(TOP VIEW)



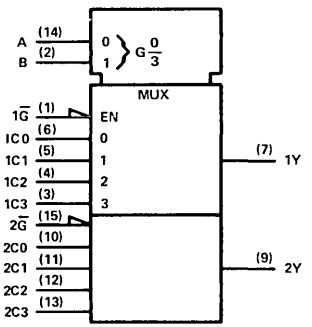
NC — No internal connection

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G̅	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

logic symbol



Pin numbers shown are for J and N packages.

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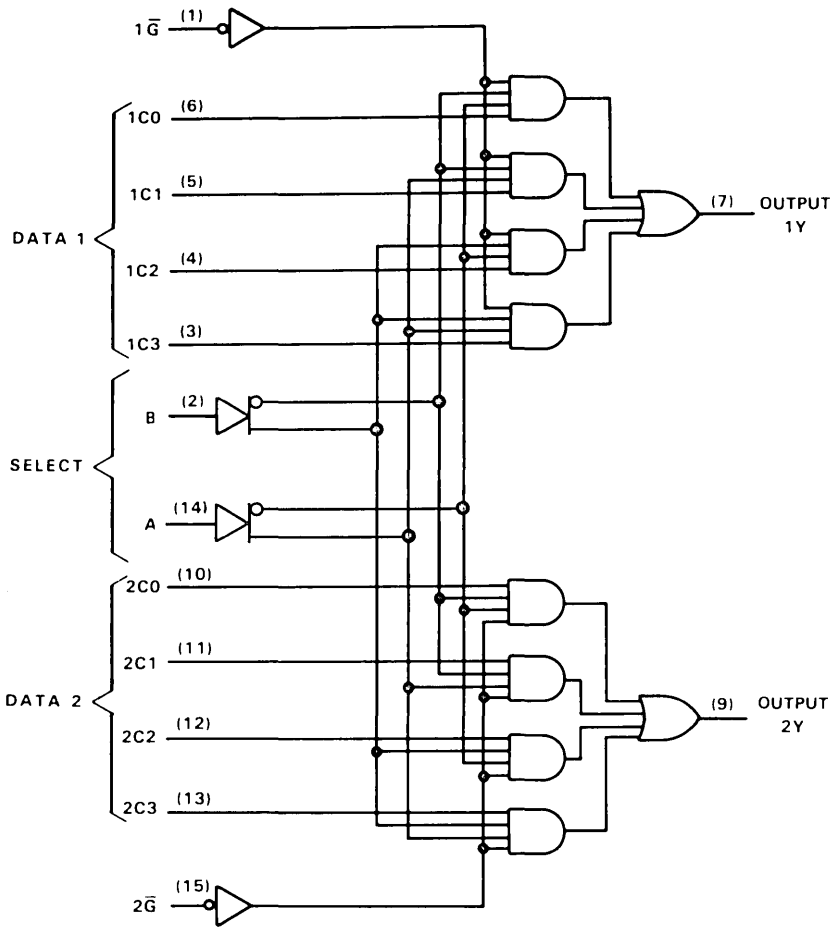
logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS153, SN54AS153 . . . . . −55 °C to 125 °C
SN74ALS153, SN74AS153 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS153			SN74ALS153			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS153			SN74ALS153			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
		V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	A, B	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	A, B	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	A, B	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	All others					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	All inputs at 4.5 V		6.3			6.3		mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS153			SN74ALS153			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y		7.5			7.5		ns
t_{PHL}				9			9		
t_{PLH}	Data (Any C)	Y		4			4		ns
t_{PHL}				6			6		
t_{PLH}	$\overline{G}$	Y		4			4		ns
t_{PHL}				5			5		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

recommended operating conditions

		SN54AS153			SN74AS153			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−12	mA
							−15†	
I_{OL}	Low-level output current			32			32	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS153			SN74AS153			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2		2.4	3.2		V
		V_{CC} = 4.75 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5		0.25	0.5	V
		V_{CC} = 4.75 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	A, B	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	A, B	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	A, B	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.6			−0.6		mA
	All others				−0.3			−0.3		
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		17			17		mA
			Outputs low		25			25		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX					UNIT
			'AS153	SN54AS153			SN74AS153		
			TYP‡	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y			5.5			5.5		ns
t_{PHL}					4.5			4.5		
t_{PLH}	Data (Any C)	Y			3.5			3.5		ns
t_{PHL}					3			3		
t_{PLH}	$\overline{G}$	Y			5.5			5.5		ns
t_{PHL}					4.5			4.5		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- **Buffered Inputs and Outputs**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

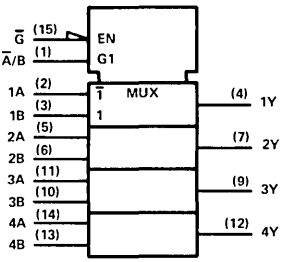
description

These monolithic data selectors/multiplexers contain inverters and drivers to supply full data selection to the four output gates. A separate strobe input ($\overline{G}$) is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The 'ALS157 presents true data whereas the 'ALS158 presents inverted data to minimize propagation delay time.

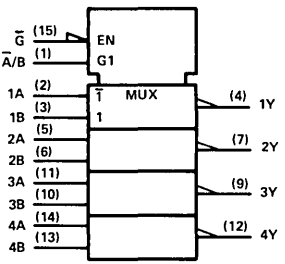
The SN54ALS157 and SN54ALS158 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS157 and SN74ALS158 are characterized for operation from 0 °C to 70 °C.

logic symbols

'ALS157

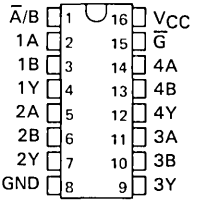


'ALS158

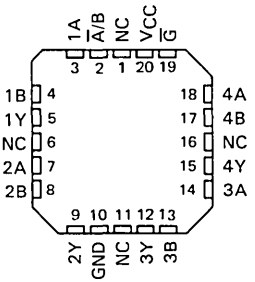


Pin numbers shown are for J and N packages.

SN54ALS157, SN54ALS158 . . . J PACKAGE
SN74ALS157, SN74ALS158 . . . N PACKAGE
(TOP VIEW)



SN54ALS157, SN54ALS158 . . . FH PACKAGE
SN74ALS157, SN74ALS158 . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

FUNCTION TABLE

INPUTS				OUTPUT Y	
STROBE G̅	SELECT A/B̅	DATA A	DATA B	'ALS157	'ALS158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

ADVANCE INFORMATION

This document contains information on a new product. Specifications are subject to change without notice.

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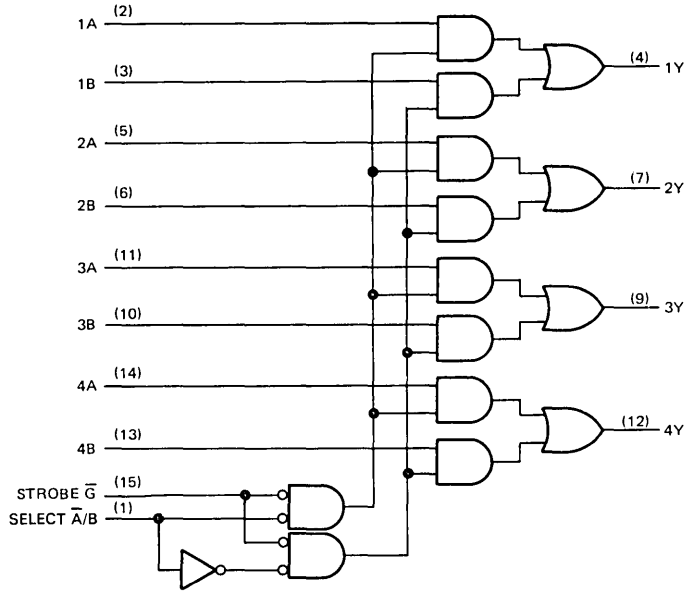
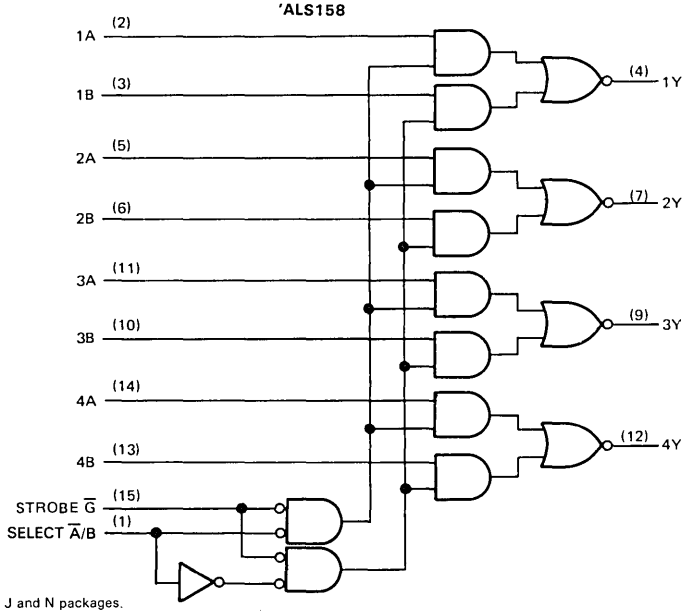
logic diagrams (positive logic)

'ALS157



'ALS158



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS157, SN54ALS158 . . . . . −55 °C to 125 °C
SN74ALS157, SN74ALS158 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

2

recommended operating conditions

		SN54ALS157 SN54ALS158			SN74ALS157 SN74ALS158			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS157 SN54ALS158			SN74ALS157 SN74ALS158			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
		V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	A or B	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	$\overline{A}/B$ or $\overline{G}$					0.2			0.2	
I_{IH}	A or B	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{A}/B$ or $\overline{G}$					40			40	
I_{IL}	A or B	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	$\overline{A}/B$ or $\overline{G}$					−0.2			−0.2	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS157	V_{CC} = 5.5 V			7.8			7.8		mA
	'ALS158				2.3			2.3		

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.

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'ALS157 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS157			SN74ALS157			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y		3.5			3.5		ns
t_{PHL}				5			5		
t_{PLH}	$\overline{A}$/B	Y		6			6		ns
t_{PHL}				6.5			6.5		
t_{PLH}	$\overline{G}$	Y		6			6		ns
t_{PHL}				6.5			6.5		

'ALS158 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS158			SN74ALS158			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y		3.5			3.5		ns
t_{PHL}				5			5		
t_{PLH}	$\overline{A}$/B	Y		6			6		ns
t_{PHL}				6.5			6.5		
t_{PLH}	$\overline{G}$	Y		6			6		ns
t_{PHL}				6.5			6.5		

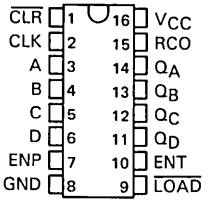
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

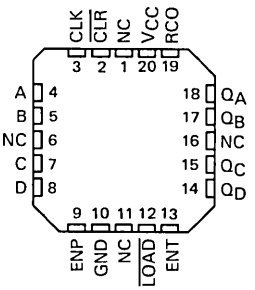
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Synchronous Counting**
- **Synchronously Programmable**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

2

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . N PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FH PACKAGE
SN74ALS', SN74AS' . . . FN PACKAGE
(TOP VIEW)



NC — no internal connection

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 'ALS160, 'ALS162, 'AS160, and 'AS162 are decade counters, and the 'ALS161, 'ALS163, 'AS161, and 'AS163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

The clear function for the 'ALS160, 'ALS161, 'AS160, and 'AS161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load, or enable inputs.

The clear function for the 'ALS162, 'ALS163, 'AS162, and 'AS163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (ENP and ENT) must be high to count, and ENT is fed forward to enable the ripple carry output. The ripple carry output (RCO) thus enabled will produce a high-level pulse while the count is maximum (9 or 15 with Q_A high). This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the ENP or ENT are allowed regardless of the level of the clock input.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

The SN54ALS160 through SN54ALS163 and SN54AS160 through SN54AS163 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS160 through SN74ALS163 and SN74AS160 through SN74AS163 are characterized for operation from 0°C to 70°C.

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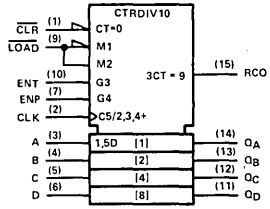
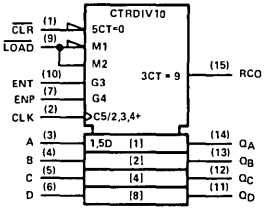
logic symbols

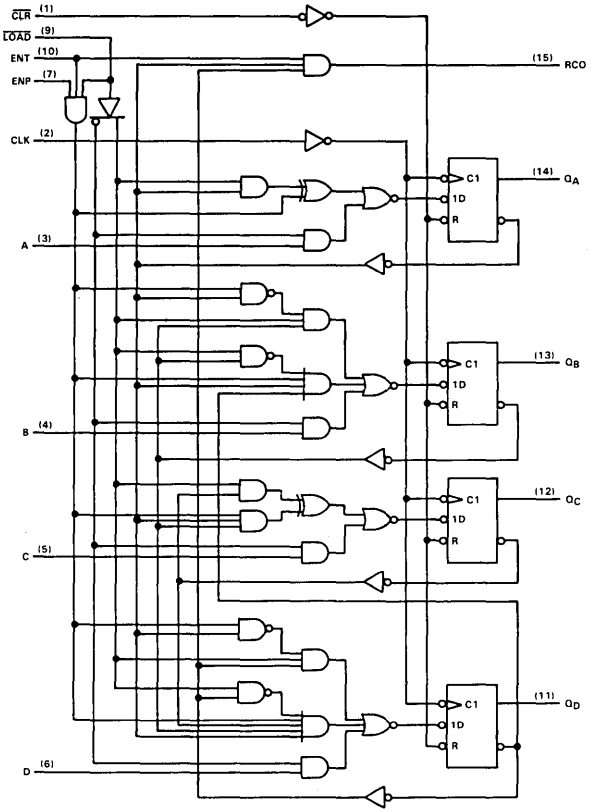
'ALS160 AND 'AS160 DECADE COUNTERS WITH DIRECT CLEAR



'ALS162 AND 'AS162 DECADE COUNTERS WITH SYNCHRONOUS CLEAR



'ALS160 logic diagram (positive logic)



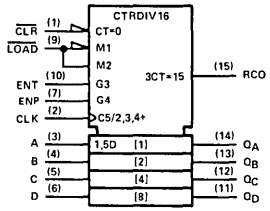
'ALS162 decade counter is similar; however the clear is synchronous as shown for the 'ALS163 binary counter on the following page.

Detailed logic diagrams for the 'AS versions have not yet been determined.

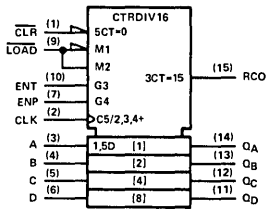
Pin numbers shown are for J and N packages.

logic symbols

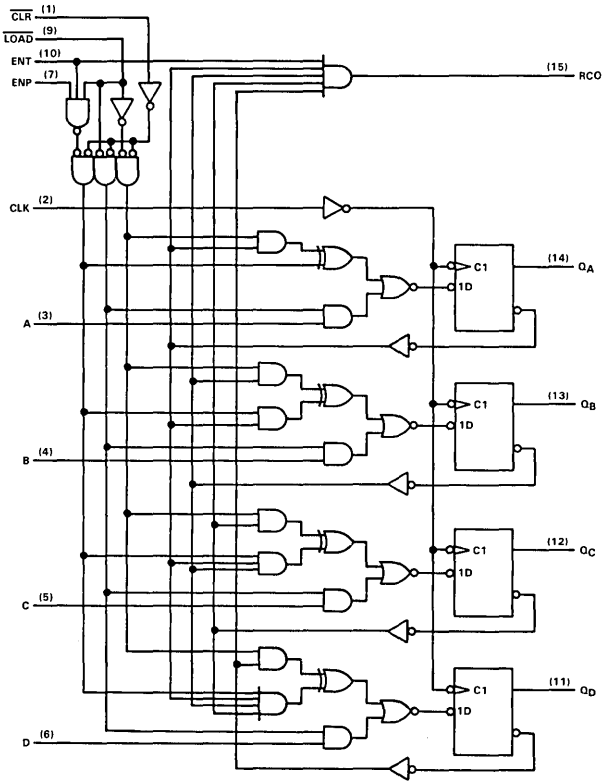
'ALS161 AND 'AS161 BINARY COUNTERS WITH DIRECT CLEAR



'ALS163 AND 'AS163 BINARY COUNTERS WITH SYNCHRONOUS CLEAR



'ALS163 logic diagram (positive logic)



'ALS161 synchronous binary counter is similar; however the clear is asynchronous as shown for the 'ALS160 decade counter on the preceding page.

Detailed logic diagrams for the 'AS versions have not yet been determined.

Pin numbers shown are for J and N packages.

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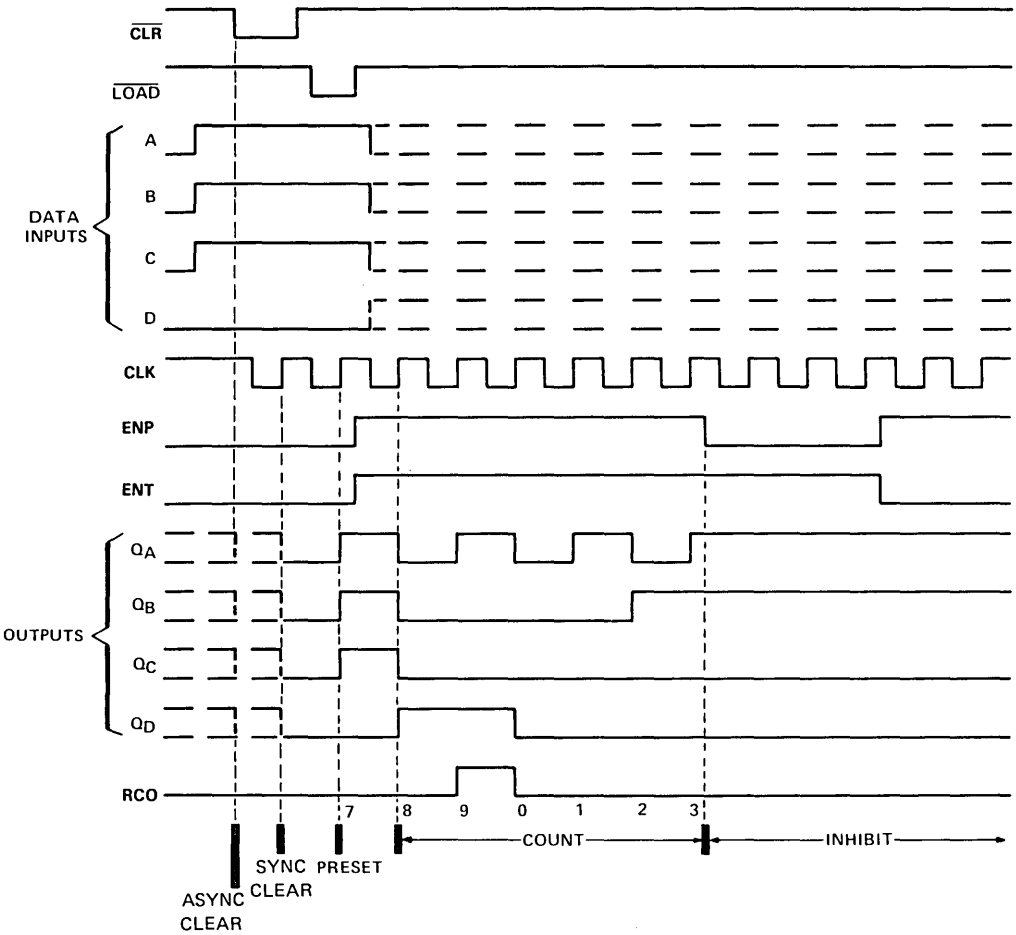
typical clear, preset, count, and inhibit sequences

'ALS160, 'AS160, 'ALS162, 'AS162

Illustrated below is the following sequence:

1. Clear outputs to zero ('ALS160 and 'AS160 are asynchronous; 'ALS162 and 'AS162 are synchronous)
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit

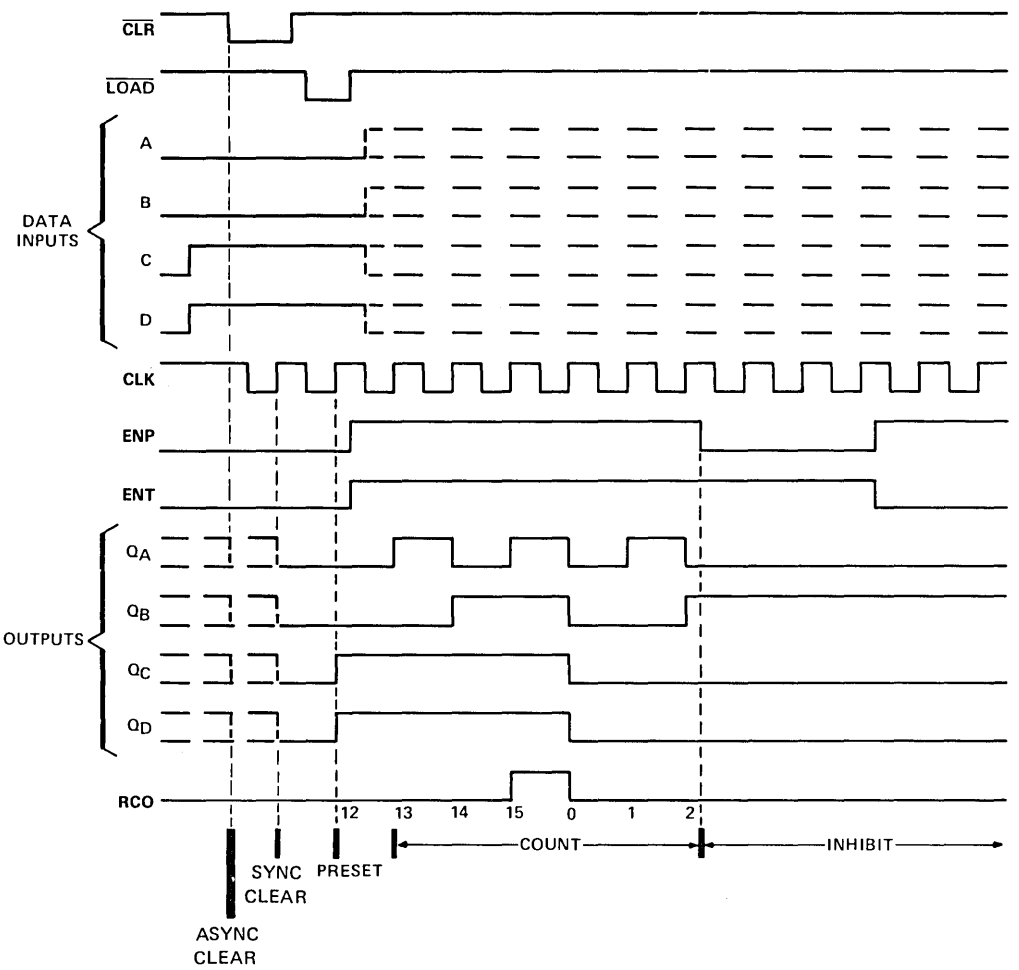


typical clear, preset, count, and inhibit sequences

'ALS161, 'AS161, 'ALS163, 'AS163

Illustrated below is the following sequence:

1. Clear outputs to zero ('ALS161 and 'AS161 are asynchronous; 'ALS163 and 'AS163 are synchronous)
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one, and two
4. Inhibit



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS160 thru SN54ALS163 . . . . . −55 °C to 125 °C
SN74ALS160 thru SN74ALS163 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

				SN54ALS160 THRU SN54ALS163			SN74ALS160 THRU SN74ALS163			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
I_{OH}	High-level output voltage					−0.4			−0.4	mA
I_{OL}	Low-level output current					4			8	mA
f_{clock}	Clock frequency	'ALS160, 'ALS162		0		25	0		30	MHz
		'ALS161, 'ALS163		0		25	0		30	
t_w	Pulse duration	CLK high or low	'ALS160, 'ALS162	20			15			ns
			'ALS161, 'ALS163	20			15			
		'ALS160, 'ALS161 $\overline{CLR}$ low		20			15			
t_{su}	Setup time before CLK↑	A, B, C, D		20			15			ns
		ENP, ENT	'ALS160, 'ALS161	25			20			
			'ALS162, 'ALS163	30			25			
		'ALS160, 'ALS161 $\overline{CLR}$ inactive		10			10			
		'ALS162, 'ALS163	$\overline{CLR}$ Low	20			15			
			$\overline{CLR}$ high (inactive)	10			10			
t_h	Hold time, all synchronous inputs after CLK↑			0			0			ns
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS160 THRU SN54ALS163			SN74ALS160 THRU SN74ALS163			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	$\overline{LOAD}$, CLK or ENT	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All other					0.1			0.1	
I_{IH}	$\overline{LOAD}$, CLK or ENT	V_{CC} = 5.5 V,	V_I = 0.4 V			40			40	μA
	All other					20			20	
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}		V_{CC} = 5.5 V			12	21		12	21	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS160, 'ALS161 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS160 SN54ALS161		SN74ALS160 SN74ALS161		
			MIN	MAX	MIN	MAX	
f_{max}	'ALS160		25		30		MHz
	'ALS161		25		30		
t_{PLH}	CLK	RCO	8	30	8	26	ns
t_{PHL}			7	25	7	23	
t_{PLH}	CLK	Any Q	4	18	4	15	ns
t_{PHL}			6	20	6	17	
t_{PLH}	ENT	RCO	5	20	5	17	ns
t_{PHL}			4	16	4	13	
t_{PHL}	$\overline{CLR}$	Any Q	8	27	8	24	ns
t_{PHL}	$\overline{CLR}$	RCO	11	31	11	28	ns

'ALS162, 'ALS163 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS162 SN54ALS163		SN74ALS162 SN74ALS163		
			MIN	MAX	MIN	MAX	
f_{max}	'ALS162		25		30		MHz
	'ALS163		25		30		
t_{PLH}	CLK	RCO	8	30	8	26	ns
t_{PHL}			7	25	7	23	
t_{PLH}	CLK	Any Q	4	18	4	15	ns
t_{PHL}			6	20	6	17	
t_{PLH}	ENT	RCO	5	20	5	17	ns
t_{PHL}			4	16	4	13	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS160 thru SN54AS163 . . . . . −55°C to 125°C
SN74AS160 thru SN74AS163 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

				SN54AS160 THRU SN54AS163			SN74AS160 THRU SN74AS163			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
I_{OH}	High-level output voltage					−2			−2	mA
I_{OL}	Low-level output current					20			20	mA
f_{clock}	Clock frequency	'AS160, 'AS162								MHz
		'AS161, 'AS163								
t_w	Pulse duration	CLK high or low	'AS160, 'AS162							ns
			'AS161, 'AS163							
		'AS160, 'AS161 $\overline{CLR}$ low								
t_{su}	Setup time before CLK↑	A, B, C, D								ns
		ENP, ENT								
		'AS160, 'AS161 $\overline{CLR}$ inactive								
		'AS162, 'ALS163	$\overline{CLR}$ Low							
			$\overline{CLR}$ high (inactive)							
t_h	Hold time, all synchronous inputs after CLK↑									ns
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS160 THRU SN54AS163			SN74AS160 THRU SN74AS163			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −2 mA	2.5	3.4		2.5	3.4		V
		V_{CC} = 4.75 V,	I_{OH} = −2 mA				2.7	3.4		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	V
I_I	$\overline{LOAD}$, CLK or ENT	V_{CC} = 5.5 V,	V_I = 7 V							mA
	All other									
I_{IH}	$\overline{LOAD}$, CLK or ENT	V_{CC} = 5.5 V,	V_I = 2.7 V							μA
	All other									
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V							mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V								mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
Additional information on these products can be obtained from the factory as it becomes available.

2

'AS160, 'AS161 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			'AS160 'AS161			SN54AS160 SN54AS161			SN74AS160 SN74AS161			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}	'AS160											MHz
	'AS161											
t_{PLH}	CLK	RCO										ns
t_{PHL}												
t_{PLH}	CLK	Any Q										ns
t_{PHL}												
t_{PLH}	ENT	RCO										ns
t_{PHL}												
t_{PHL}	$\overline{CLR}$	Any Q										ns
t_{PHL}	$\overline{CLR}$	RCO										ns

'AS162, 'AS163 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			'AS162 'AS163			SN54AS162 SN54AS163			SN74AS162 SN74AS163			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}	'AS162											MHz
	'AS163											
t_{PLH}	CLK	RCO										ns
t_{PHL}												
t_{PLH}	CLK	Any Q										ns
t_{PHL}												
t_{PLH}	ENT	RCO										ns
t_{PHL}												

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

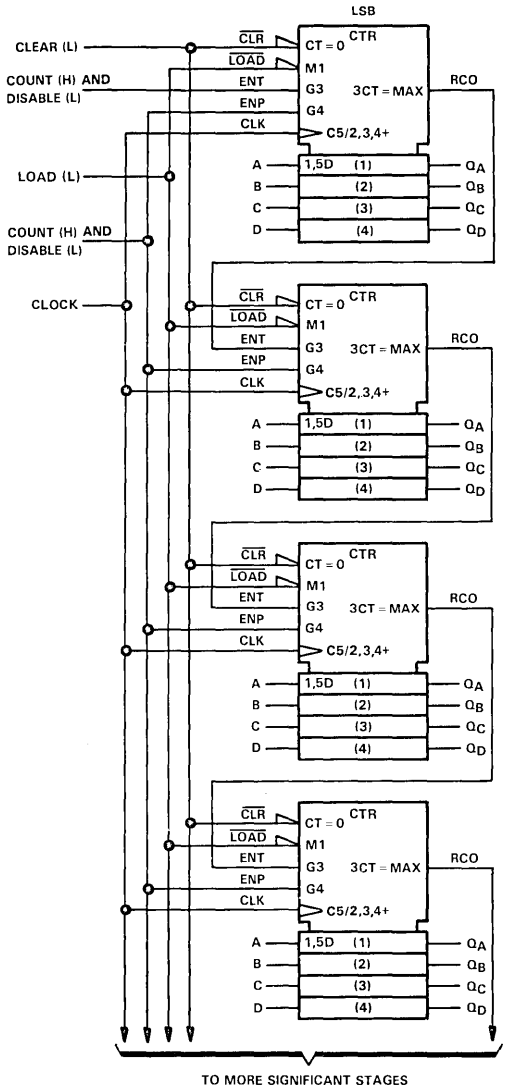
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

TYPICAL APPLICATION DATA

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 'ALS160, 'AS160, 'ALS162, and 'AS162 will count in BCD and the 'ALS161, 'AS161, 'ALS163 and 'AS163 will count in binary. Virtually any count mode (modulo-N, N_1-to-N_2, N_1-to-maximum) can be used with this fast look-ahead circuit.



- AND-Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Direct Clear
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

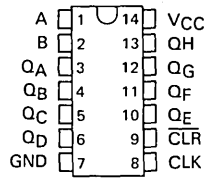
2

description

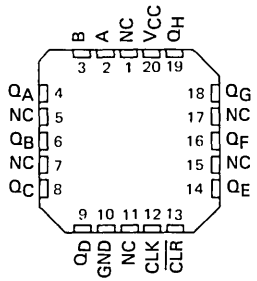
These 8-bit shift registers feature AND-gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

The SN54ALS164 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS164 is characterized for operation from 0°C to 70°C.

SN54ALS164 . . . J PACKAGE
SN74ALS164 . . . N PACKAGE
(TOP VIEW)



SN54ALS164 . . . FH PACKAGE
SN74ALS164 . . . FN PACKAGE
(TOP VIEW)



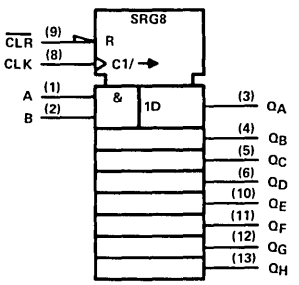
NC—No Internal connection

FUNCTION TABLE

INPUTS				OUTPUTS		
CLEAR	CLOCK	A	B	Q_A	$Q_B \ldots Q_H$	
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level.
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent ↑ transition of the clock; indicates a one-bit shift.

logic symbol



Pin numbers shown are for J and N packages.

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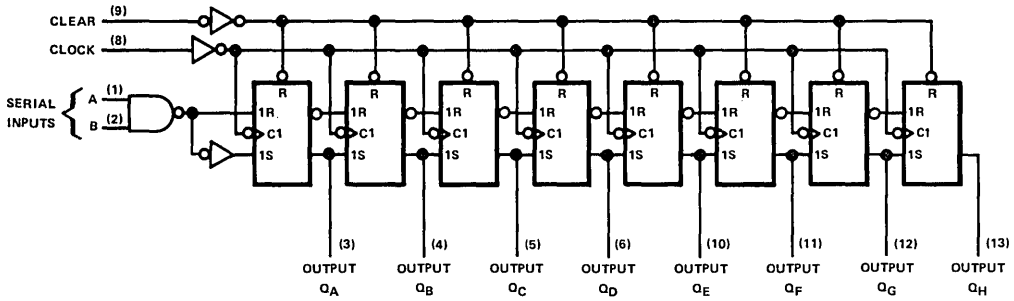
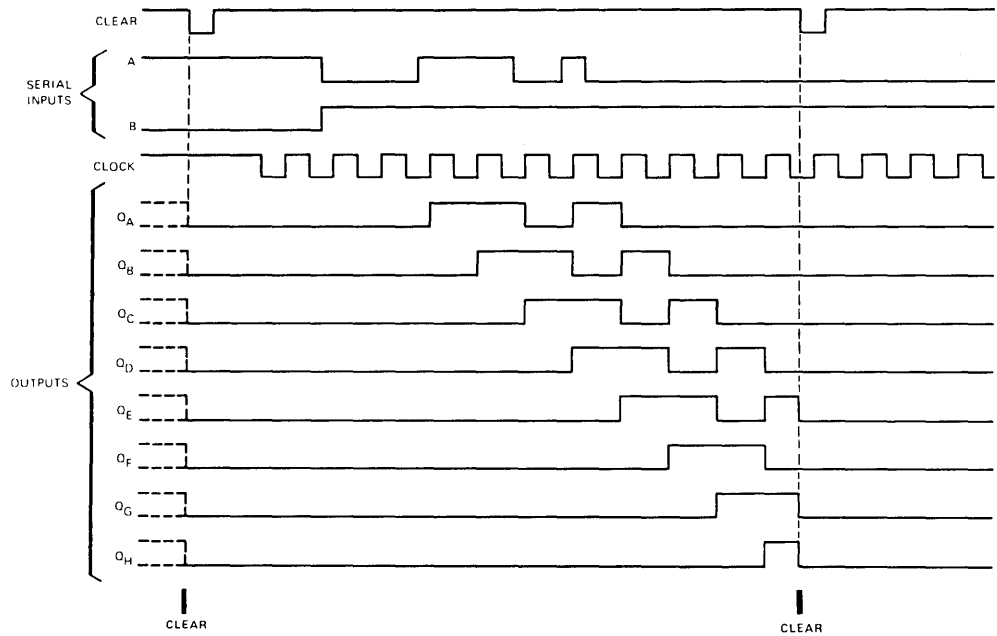
4

logic diagram (positive logic)



Pin numbers shown are for J and N packages.

typical clear, shift, and clear sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS164 . . . . . −55 °C to 125 °C
SN74ALS164 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS164			SN74ALS164			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4				mA
								8	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	$\overline{CLR}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↑	Data							ns
		$\overline{CLR}$ inactive							
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS164			SN74ALS164			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4					V
	V_{CC} = 4.5 V	I_{OH} = −0.4 mA				2.7	3.4		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 1							mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with serial inputs grounded, CLK input at 2.4 V, and a momentary ground, then 4.5 V, applied to $\overline{CLR}$.

switching characteristics (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			'ALS164			SN54ALS164			SN74ALS164			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}												MHz
t_{PHL}	$\overline{CLR}$	Any Q										ns
t_{PLH}	CLK	Any Q										ns
t_{PHL}												

‡All typical values are V_{CC} = 5 V, T_A = 25°C.
NOTE 2: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

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- Complementary Outputs
- Direct Overriding Load (Data) Inputs
- Gated Clock Inputs
- Parallel-to-Serial Data Conversion
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

The 'ALS165 is an 8-bit serial shift register that, when clocked, shifts the data toward serial output $\overline{Q}_H$. Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the SH/LD input. The 'ALS165 also features a clock inhibit function and a complemented serial output $\overline{Q}_H$.

Clocking is accomplished by a low-to-high transition of the CLK input while SH/$\overline{LD}$ is held high and CLK INH is held low. The functions of the CLK and CLK INH (clock inhibit) inputs are interchangeable. Since a low CLK input and a low-to-high transition of CLK INH will also accomplish clocking, CLK INH should be changed to the high level only while the CLK input is high. Parallel loading is inhibited when SH/$\overline{LD}$ is held high. The parallel inputs to the register are enabled while SH/$\overline{LD}$ is low independently of the levels of CLK, CLK INH, or SER inputs.

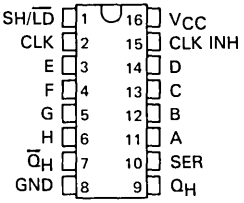
The SN54ALS165 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS165 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

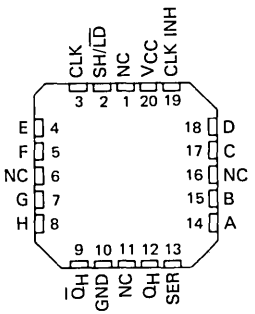
INPUTS			FUNCTION
SH/$\overline{LD}$	CLK	CLK INH	
L	X	X	PARALLEL LOAD
H	H	X	NO CHANGE
H	X	H	NO CHANGE
H	L	↑	SHIFT
H	↑	L	SHIFT

SHIFT – content of each internal register shifts toward serial output Q_H. Data at serial input is shifted into first register.

SN54ALS165 . . . J PACKAGE
SN74ALS165 . . . N PACKAGE
(TOP VIEW)

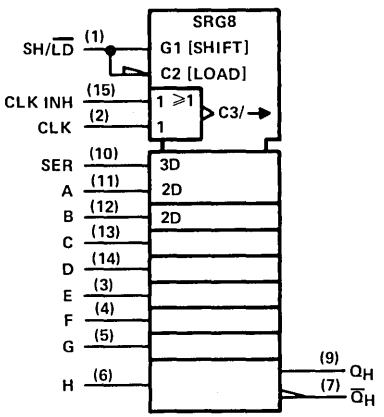


SN54ALS165 . . . FH PACKAGE
SN74ALS165 . . . FN PACKAGE
(TOP VIEW)



NC – no internal connection

logic symbol



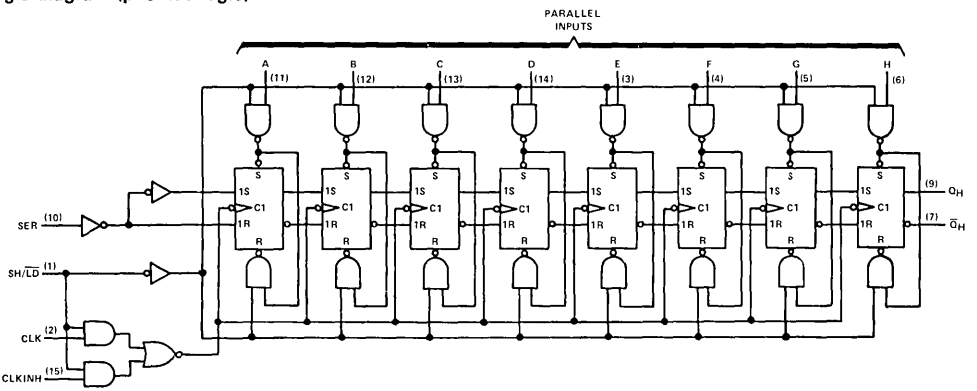
Pin numbers shown are for J and N packages.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

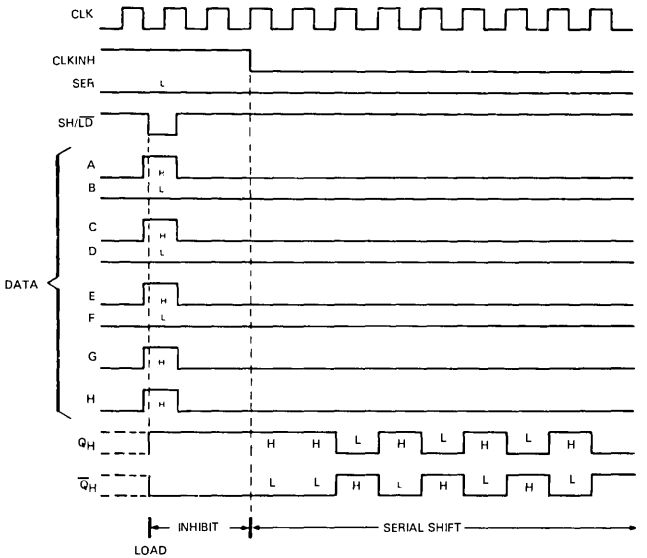
2

logic diagram (positive logic)



Pin numbers shown are for J and N packages

typical shift, load, and inhibit sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS165 . . . . . −55°C to 125°C
SN74ALS165 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

TEXAS INSTRUMENTS
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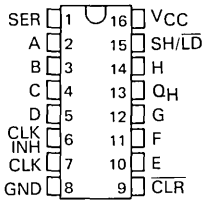
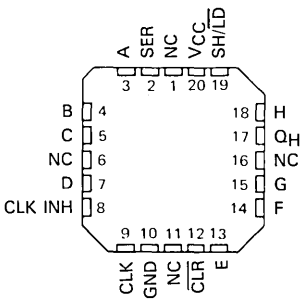
- Synchronous Load
- Direct Overriding Clear
- Parallel to Serial Conversion
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic And Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS166 . . . J PACKAGE
SN74ALS166 . . . N PACKAGE
(TOP VIEW)



SN54ALS166 . . . FH PACKAGE
SN74ALS166 . . . FN PACKAGE
(TOP VIEW)



NC – No Internal connection

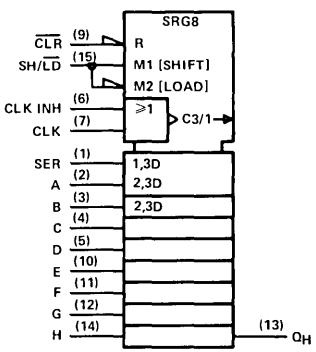
description

The 'ALS166 8-bit shift register is compatible with most other TTL logic families. All inputs are buffered to lower the drive requirements. Input clamping diodes minimize switching transients and simplify system design.

These parallel-in or serial-in, serial-out registers have a complexity of 77 equivalent gates on a monolithic chip. They feature gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This, of course, allows the system clock to be free-running and the register can be stopped on command with the clock input. The clock-inhibit input should be changed to the high level only when the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

The SN54ALS166 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS166 is characterized for operation from 0°C to 70°C.

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE

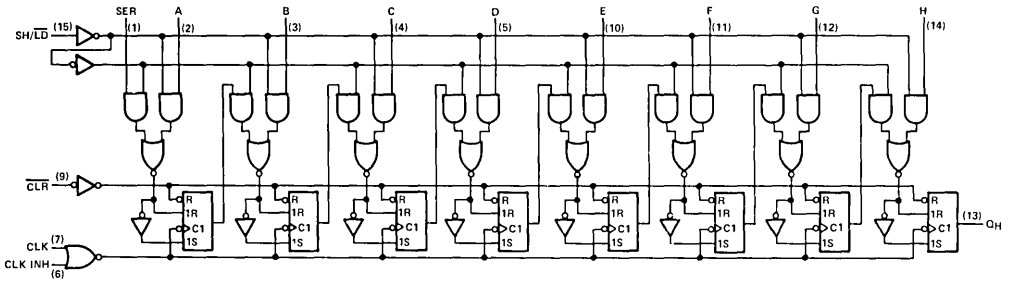
INPUTS						INTERNAL OUTPUTS		OUTPUT
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

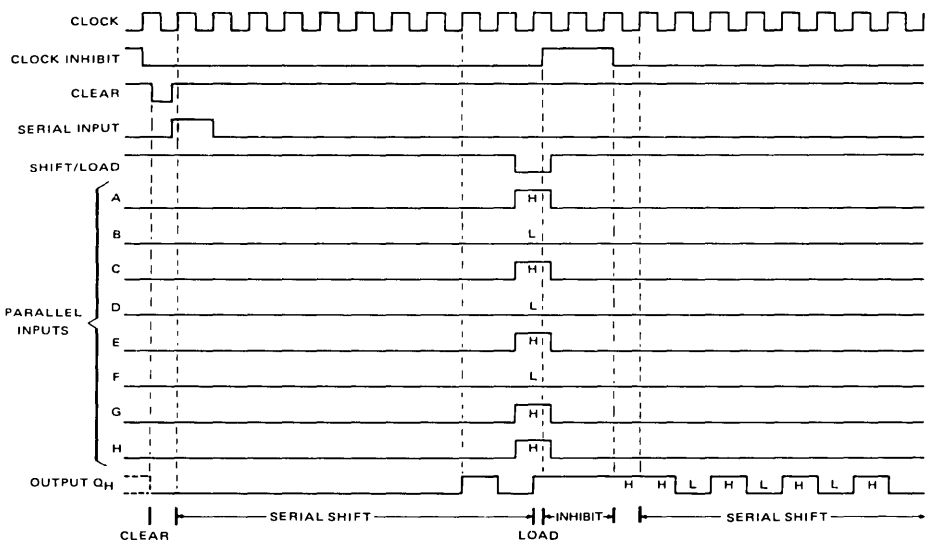
2

logic diagram (positive logic)



Pin numbers shown are for J and N packages.

typical clear, shift, load, inhibit, and shift sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS166 . . . . . −55 °C to 125 °C
SN74ALS166 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

TEXAS INSTRUMENTS
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recommended operating conditions

			SN54ALS166			SN74ALS166			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4				mA
								8	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	$\overline{CLR}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↑	SH/$\overline{LD}$							ns
		Data							
		$\overline{CLR}$ inactive							
t_h	Hold time, data after CLK↑								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS166			SN74ALS166			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4					V
	V_{CC} = 4.5 V	I_{OH} = −0.4 mA				2.7	3.4		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V,	See note 1							mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: With 4.5 volts applied to the serial input and all other inputs except the clock grounded, I_{CC} is measured after a clock transition from 0 to 4.5 volts.

switching characteristics (see note 1)

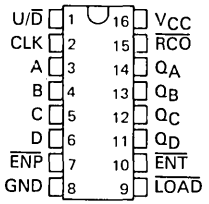
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			'ALS166			SN54ALS166			SN74ALS166			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}												MHz
t_{PHL}	$\overline{CLR}$	Q_H										ns
t_{PLH}	CLK	Q_H										ns
t_{PHL}												

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: For load circuit and voltage waveforms, see page 1-12.

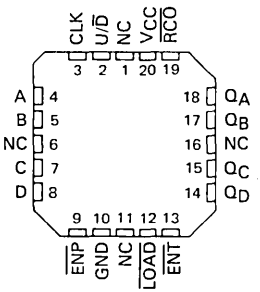
Additional information on these products can be obtained from the factory as it becomes available.

- Fully Synchronous Operation for Counting and Programming
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Fully Independent Clock Circuit
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . N PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FH PACKAGE
SN74ALS', SN74AS' . . . FN PACKAGE
(TOP VIEW)



NC – no internal connection.

descriptions

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The 'ALS168 and 'AS168 are decade counters and the 'ALS169 and 'AS169 are two 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

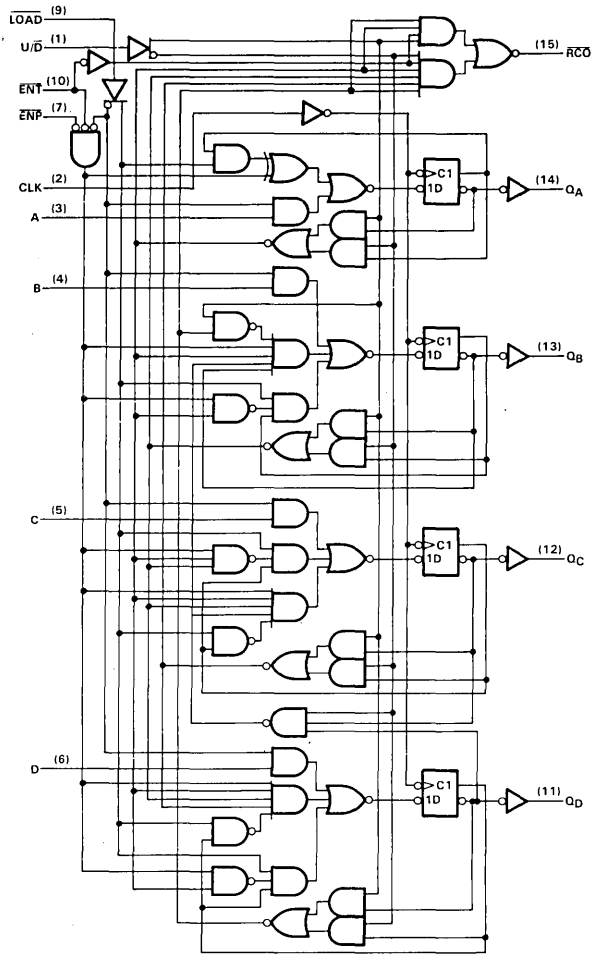
These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous application without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{ENP}$ and $\overline{ENT}$) must be low to count. The direction of the count is determined by the level of the U/$\overline{D}$ input. When U/$\overline{D}$ is high, the counter counts up; when low, it counts down. Input $\overline{ENT}$ is fed forward to enable the carry output. The ripple carry output ($\overline{RCO}$) thus enabled will produce a low-level pulse while the count is zero (all inputs low) counting down or maximum (9 or 15) counting up. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at $\overline{ENP}$ or $\overline{ENT}$ are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

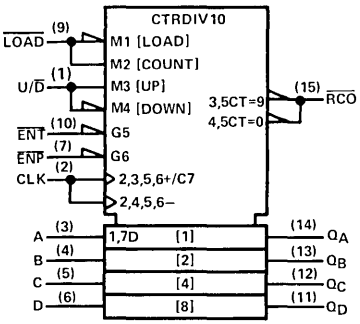
These counters feature a fully independent clock circuit. Changes at control inputs ($\overline{ENP}$, $\overline{ENT}$, $\overline{LOAD}$, U/$\overline{D}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

The SN54ALS168, SN54AS168, SN54ALS169, and SN54AS169 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS168, SN74AS168, SN74ALS169, and SN74AS169 are characterized for operation from 0 °C to 70 °C.

'ALS168 logic diagram (positive logic)

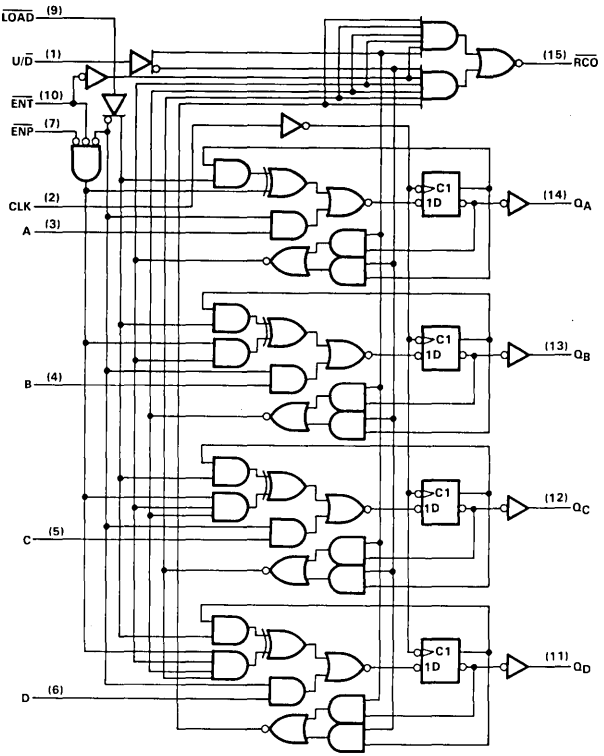


'ALS168, 'AS168 logic symbol

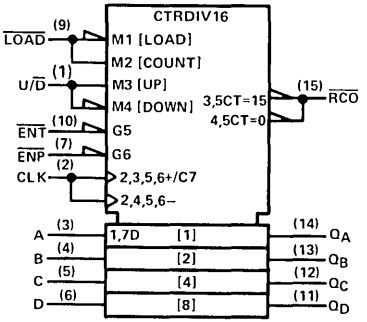


Detailed logic diagrams for the 'AS versions have not yet been determined.
Pin numbers shown are for J and N packages.

'ALS169 logic diagram (positive logic)



'ALS169, 'AS169 logic symbol



Detailed logic diagrams for the 'AS versions have not yet been determined.
Pin numbers shown are for J and N packages.

TEXAS INSTRUMENTS
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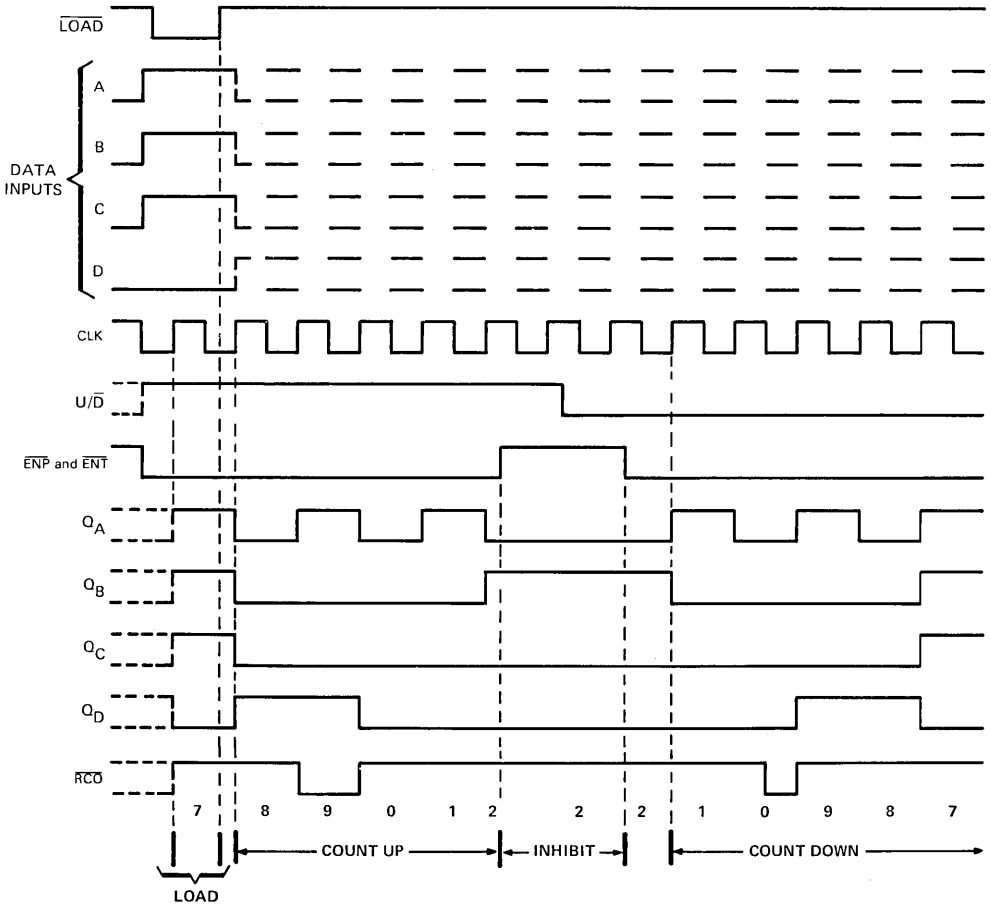
'ALS168, 'AS168 typical load, count, and inhibit sequences

Illustrated below is the following sequence:

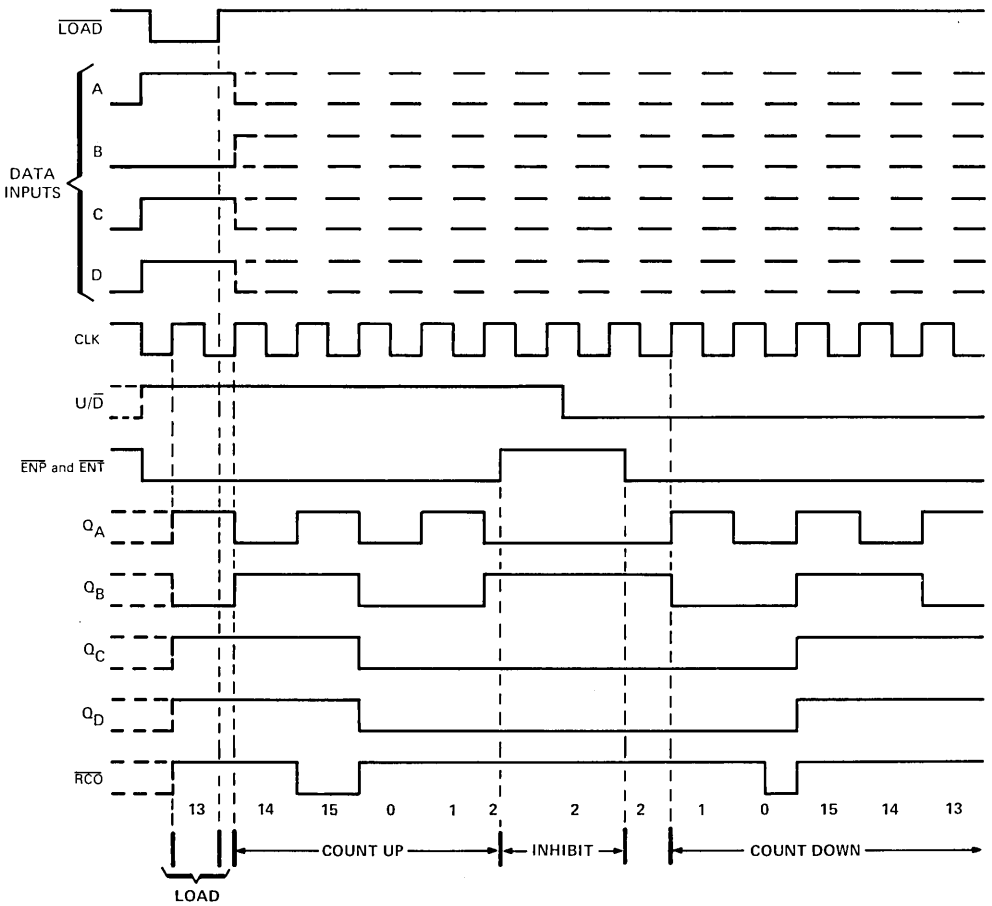
1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven



'ALS169, 'AS169 typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS168, SN54ALS169 . . . . . −55 °C to 125 °C
SN74ALS168, SN74ALS169 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS168 SN54ALS169			SN74ALS168 SN74ALS169			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		25	0		30	MHz
t_w	Pulse duration	CLK high or low	20			15			ns
t_{su}	Setup time before CLK↑	A, B, C, or D	20			15			ns
		$\overline{ENP}$ or $\overline{ENT}$	25			20			
		$\overline{LOAD}$	20			15			
		U/$\overline{D}$	20			15			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS168 SN54ALS169			SN74ALS168 SN74ALS169			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.8 V			−0.2			−0.2	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	V_{CC} = 5.5 V			15	25		15	25	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS168, 'ALS169 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS168 SN54ALS169		SN74ALS168 SN74ALS169		
			MIN	MAX	MIN	MAX	
f_{max}			25		30		MHz
t_{PLH}	CLK	$\overline{RCO}$	10	32	10	28	ns
t_{PHL}			6	22	6	18	
t_{PLH}	CLK	Any Q	5	19	5	16	ns
t_{PHL}			5	20	5	16	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	5	19	5	16	ns
t_{PHL}			3	16	3	13	
t_{PLH}	U/$\overline{D}$	$\overline{RCO}$	5	25	5	23	ns
t_{PHL}			5	23	5	19	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS168, SN54AS169 . . . . . −55°C to 125°C
SN74AS168, SN74AS169 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS168 SN54AS169			SN74AS168 SN74AS169			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	CLK high or low							ns
t_{su}	Setup time before CLK↑	A, B, C, or D							ns
		$\overline{ENP}$ or $\overline{ENT}$							
		$\overline{LOAD}$							
		$U/\overline{D}$							
t_h	Hold time, data after CLK↑								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS168 SN54AS169			SN74AS168 SN74AS169			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −2 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −2 mA				2.7	3.4		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V							mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V							mA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V							mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V								mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

'AS168, 'AS169 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, RL = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, RL = 500 Ω, T_A = MIN to MAX						UNIT
			'AS168 'AS169			SN54AS168 SN54AS169			SN74AS168 SN74AS169			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}												MHz
t_{PLH}	CLK	$\overline{RCO}$										ns
t_{PHL}												
t_{PLH}	CLK	Any Q										ns
t_{PHL}												
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$										ns
t_{PHL}												
t_{PLH}	U/$\overline{D}$	$\overline{RCO}$										ns
t_{PHL}												

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

TEXAS INSTRUMENTS
INCORPORATED
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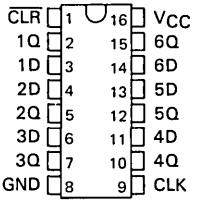
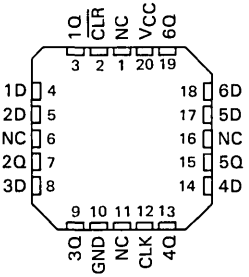
D2661, APRIL 1982

- **'ALS174 and 'AS174 Contain Six Flip-Flops with Single-Rail Outputs**
- **'ALS175 and 'AS175 Contain Four Flip-Flops with Double-Rail Outputs**
- **Buffered Clock and Direct Clear Inputs**
- **Applications Include:**
  Buffer/Storage Registers
  Shift Registers
  Pattern Generators
- **Fully Buffered Outputs for Maximum Isolation from External Disturbance ('AS only)**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

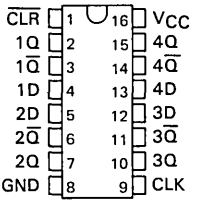
SN54ALS174, SN54AS174 . . . J PACKAGE
SN74ALS174, SN74AS174 . . . N PACKAGE
(TOP VIEW)



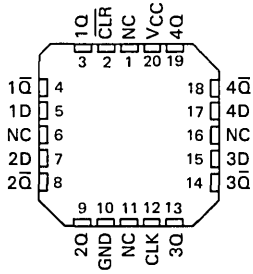
SN54ALS174, SN54AS174 . . . FH PACKAGE
SN74ALS174, SN74AS174 . . . FN PACKAGE
(TOP VIEW)



SN54ALS175, SN54AS175 . . . J PACKAGE
SN74ALS175, SN74AS175 . . . N PACKAGE
(TOP VIEW)



SN54ALS175, SN54AS175 . . . FH PACKAGE
SN74ALS175, SN74AS175 . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection.

description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input and the 'ALS175 and 'AS175 feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These circuits are fully compatible for use with most TTL circuits.

The SN54ALS174, SN54ALS175, SN54AS174, and SN54AS175 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS174, SN74ALS175, SN74AS174, and SN74AS175 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
$\overline{CLR}$	CLK	D	Q	$\overline{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

† 'ALS175 and 'AS175 only

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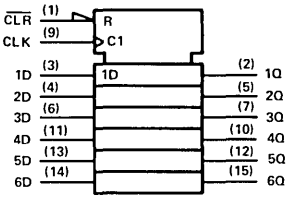
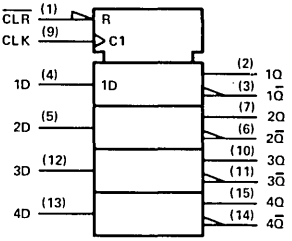
logic symbols

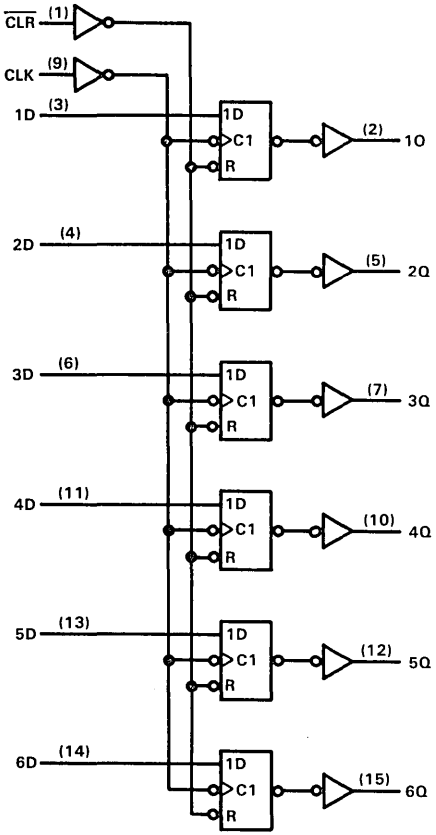
'ALS174, 'AS174

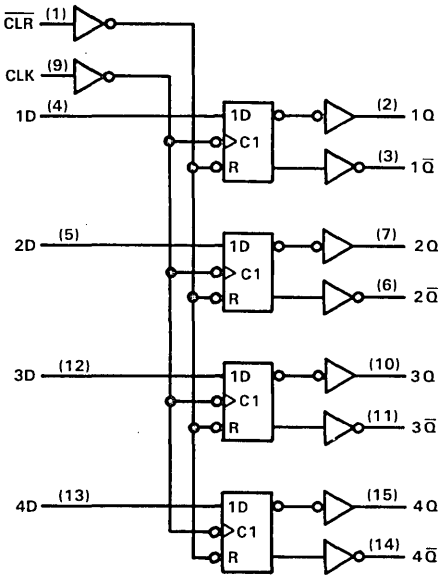


'ALS175, 'AS175



logic diagrams (positive logic)





Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS174, SN54ALS175 . . . . . −55°C to 125°C
SN74ALS174, SN74ALS175 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS174 SN54ALS175			SN74ALS174 SN74ALS175			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1				mA
								−2.6	
I_{OL}	Low-level output current				12				mA
								24	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	$\overline{CLR}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↑	Data							ns
		$\overline{CLR}$ inactive							
t_h	Hold time, data after CLK↑								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS174 SN54ALS175			SN74ALS174 SN74ALS175			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
		V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS174	V_{CC} = 5.5 V,	See Note 1		8			8		mA
	'ALS175				6			6		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with D inputs and CLK at 4.5 V, and $\overline{CLR}$ grounded.

Additional information on these products can be obtained from the factory as it becomes available.

switching characteristics (see note 2)

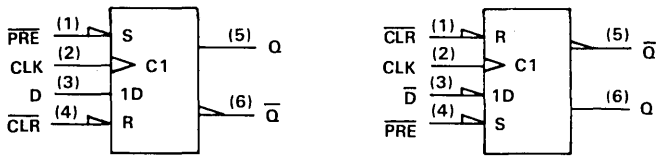
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS174 SN54ALS175			SN74ALS174 SN74ALS175			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}				80			80		MHz
t_{PLH}	$\overline{CLR}$	Any $\overline{Q}$ ('ALS175)		10			10		ns
t_{PHL}		Any Q		11			11		
t_{PLH}	CLK	Any Q (or $\overline{Q}$, 'ALS175)		9			9		ns
t_{PHL}				10			10		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: For load circuit and voltage waveforms, see page 1-12.

D flip-flop signal conventions

It is TI practice to name the outputs and other inputs of a D-type flip-flop and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.



Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (▷) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input D, but now both are considered active-low.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS174, SN54AS175 . . . . . −55°C to 125°C
SN74AS174, SN74AS175 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS174 SN54AS175			SN74AS174 SN74AS175			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	$\overline{CLR}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↑	Data							ns
		$\overline{CLR}$ inactive							
t_h	Hold time, data after CLK↑								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS174 SN54AS175			SN74AS174 SN74AS175			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −2 mA	2.5	3.4		2.5	3.4		V
		V_{CC} = 4.75 V,	I_{OH} = −2 mA				2.7	3.4		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	V
I_I	CLK	V_{CC} = 5.5 V,	V_I = 7 V							mA
	$\overline{CLR}$									
	Data									
I_{IH}	CLK	V_{CC} = 5.5 V,	V_I = 2.7 V							μA
	$\overline{CLR}$									
	Data									
I_{IL}	CLK	V_{CC} = 5.5 V,	V_I = 0.4 V							mA
	$\overline{CLR}$									
	Data									
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS174	V_{CC} = 5.5 V,	See Note 1		46			46		mA
	'AS175				33			33		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with D, CLK, and $\overline{PRE}$ grounded, then with D, CLK, and $\overline{CLR}$ grounded.

Additional information on these products can be obtained from the factory as it becomes available.

switching characteristics (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			'AS174 'AS175			SN54AS174 SN54AS175			SN74AS174 SN74AS175			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}							160			160		MHz
t_{PLH}	$\overline{CLR}$	Any $\overline{Q}$ ('AS175)					5			5		ns
t_{PHL}		Any Q					5.5			5.5		
t_{PLH}	CLK	Any Q (or $\overline{Q}$, 'AS175)					4			4		ns
t_{PHL}							4			4		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: For load circuit and voltage waveforms, see page 1-12.

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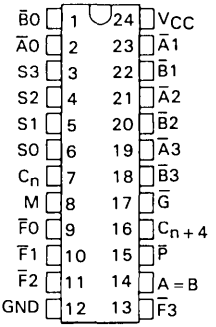
D2661, DECEMBER 1982

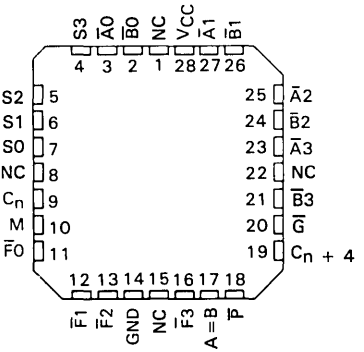
- Package Options Include the 'AS181A in Compact 300-mil or Standard 600-mil DIPs. The 'AS881A Is Offered in 300-mil DIPs. Both Devices Are Available in Both Plastic and Ceramic Chip Carriers
- Full Look-Ahead for High-Speed Operations on Long Words
- Arithmetic Operating Modes:
  - Addition
  - Subtraction
  - Shift Operand A One Position
  - Magnitude Comparison
  - Plus Twelve Other Arithmetic Operations
- Logic Function Modes
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - 'AS881A Provides Status Register Checks
  - Plus Ten Other Logic Operations
- Dependable Texas Instruments Quality and Reliability

SN54AS181A . . . J OR JT PACKAGE
SN54AS881A . . . . JT PACKAGE
SN74AS181A . . . . N OR NT PACKAGE
SN74AS881A . . . . NT PACKAGE
(TOP VIEW)



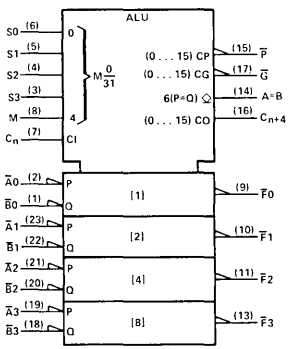
SN54AS181A, SN54AS881A . . . . FH PACKAGE
SN74AS181A, SN74AS881A . . . . FN PACKAGE

'AS181A, 'AS881A
(TOP VIEW)



NC – no internal connection

logic symbol



Pin numbers shown are J, JT, N and NT packages.

TYPICAL ADDITION TIMES (C_L = 15 pF, R_L = 280 Ω, T_A = 25°C)

NUMBER OF BITS	ADDITION TIMES USING 'AS881A AND 'AS882	ADDITION TIMES USING 'AS181A AND 'AS882	ADDITION TIMES USING 'S181 AND 'S182	PACKAGE COUNT ARITHMETIC LOGIC UNITS	PACKAGE COUNT LOOK-AHEAD CARRY GENERATORS	CARRY METHOD BETWEEN ALU's
1 to 4	5 ns	5 ns	11 ns	1		NONE
5 to 8	10 ns	10 ns	18 ns	2		RIPPLE
9 to 16	14 ns	14 ns	19 ns	3 or 4	1	FULL LOOK-AHEAD
17 to 64	19 ns	19 ns	28 ns	5 to 16	2 to 5	FULL LOOK-AHEAD

ADVANCE INFORMATION
This document contains information on a new product. Specifications are subject to change without notice.

description

The 'AS181A and 'AS881A are arithmetic logic units (ALU)/function generators that have a complexity of 75 and 77 equivalent gates respectively, on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the SN54AS882 or SN74AS882 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown previously illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading 'AS882 circuits with these ALU's to provide multi-level full carry look-ahead is illustrated under signal designations.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The 'AS181A and 'AS881A will accommodate active-high or active-low data if the pin designations are interpreted as follows:

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-low data (Table 1)	$\overline{A}0$	$\overline{B}0$	$\overline{A}1$	$\overline{B}1$	$\overline{A}2$	$\overline{B}2$	$\overline{A}3$	$\overline{B}3$	$\overline{F}0$	$\overline{F}1$	$\overline{F}2$	$\overline{F}3$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$
Active-high data (Table 2)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A − B − 1, which requires an end-around or forced carry to provide A − B.

The 'AS181A and 'AS881A can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU must be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

INPUT C_n	OUTPUT C_{n+4}	ACTIVE-LOW DATA (FIGURE 1)	ACTIVE-HIGH DATA (FIGURE 2)
H	H	A ≥ B	A ≤ B
H	L	A < B	A > B
L	H	A > B	A < B
L	L	A ≤ B	A ≥ B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

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description (continued)

The 'AS881A has the same pinout and same functionality as the 'AS181A except for the $\overline{P}$, $\overline{G}$, and C_{n+4} outputs when the device is in the logic mode (M = H).

In the logic mode the 'AS881 provides the user with a status check on the input words, A and B, and the output word F. While in the logic mode the $\overline{P}$, $\overline{G}$ and C_{n+4} outputs supply status information based upon the following logical combinations:

$\overline{P} = F0 + F1 + F2 + F3$
$\overline{G} = H$
$C_{n+4} = PC_n$

FUNCTION TABLE FOR INPUT BITS EQUAL/NOT EQUAL

S0 = S3 = H, S1 = S2 = L, and M = H

C_n	DATA INPUTS				OUTPUTS		
					$\overline{G}$	$\overline{P}$	C_{n+4}
H	A0 = B0	A1 = B1	A2 = B2	A3 = B3	H	L	H
L	A0 = B0	A1 = B1	A2 = B2	A3 = B3	H	L	L
X	A0 ≠ B0	X	X	X	H	H	L
X	X	A1 ≠ B1	X	X	H	H	L
X	X	X	A2 ≠ B2	X	H	H	L
X	X	X	X	A3 ≠ B3	H	H	L

FUNCTION TABLE FOR INPUT PAIRS HIGH/NOT HIGH

S0 = S1 = S3 = L, S2 = H, and M = H

C_n	DATA INPUTS				OUTPUTS		
					$\overline{G}$	$\overline{P}$	C_{n+4}
H	$\overline{A}0$ or $\overline{B}0$ = L	$\overline{A}1$ or $\overline{B}1$ = L	$\overline{A}2$ or $\overline{B}2$ = L	$\overline{A}3$ or $\overline{B}3$ = L	H	L	H
L	$\overline{A}0$ or $\overline{B}0$ = L	$\overline{A}1$ or $\overline{B}1$ = L	$\overline{A}2$ or $\overline{B}2$ = L	$\overline{A}3$ or $\overline{B}3$ = L	H	L	L
X	$\overline{A}0 = \overline{B}0$ = H	X	X	X	H	H	L
X	X	$\overline{A}1 = \overline{B}1$ = H	X	X	H	H	L
X	X	X	$\overline{A}2 = \overline{B}2$ = H	X	H	H	L
X	X	X	X	$\overline{A}3 = \overline{B}3$ = H	H	H	L

The combination of signals on the S3 through S0 control lines determine the operation performed on the data words to generate the output bits Fi. By monitoring the $\overline{P}$ and C_{n+4} outputs, the user can determine if all pairs of input bits are equal (see table above) or if any pair of inputs are both high (see table above). The 'AS881A has the unique feature of providing an A = B status while the exclusive-OR ($\oplus$) function is being utilized. When the control inputs (S3, S2, S1, S0) equal H, L, L, H; a status check is generated to determine whether all pairs (Ai, Bi) are equal in the following manner: $\overline{P} = (A0 \oplus B0) + (A1 \oplus B1) + (A2 \oplus B2) + (A3 \oplus B3)$. This unique bit-by-bit comparison of the data words which is available on the totem pole $\overline{P}$ output is particularly useful when cascading 'AS881's. As the A = B condition is sensed in the first stage the signal is propagated through the same ports used for carry generation in the arithmetic mode ($\overline{P}$ and $\overline{G}$). Thus the A = B status is transmitted to the second stage more quickly without the need for external multiplexing logic. The A = B open-collector output allows the user to check the validity of the bit-by-bit result by comparing the two signals for parity.

If the user wishes to check for any pair of data inputs ($\overline{A}i$, $\overline{B}i$) being high, it is necessary to set the control lines (S3,S2,S1,S0) to L, H, L, L. The data pairs will then be ANDed together and the results ORed in the following manner: $\overline{P} = \overline{A}0\overline{B}0 + \overline{A}1\overline{B}1 + \overline{A}2\overline{B}2 + \overline{A}3\overline{B}3$.

S3	S2	S1	S0	M	$\overline{P}$ =
L	H	L	L	H	$\overline{A}0\overline{B}0 + \overline{A}1\overline{B}1 + \overline{A}2\overline{B}2 + \overline{A}3\overline{B}3$
H	L	L	H	H	$(A0 \oplus B0) + (A1 \oplus B1) + (A2 \oplus B2) + (A3 \oplus B3)$

signal designations

In both Figures 1 and 2, the polarity indicators (⏥) indicate that the associated input or output is active-low with respect to the function shown inside the symbol and the symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data, and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accommodate the logic functions and arithmetic operations for the active-high data given in Table 2. The 'AS181 and 'AS881 together with the 'AS882 and 'S182 can be used with the signal designation of either Figure 1 or Figure 2.

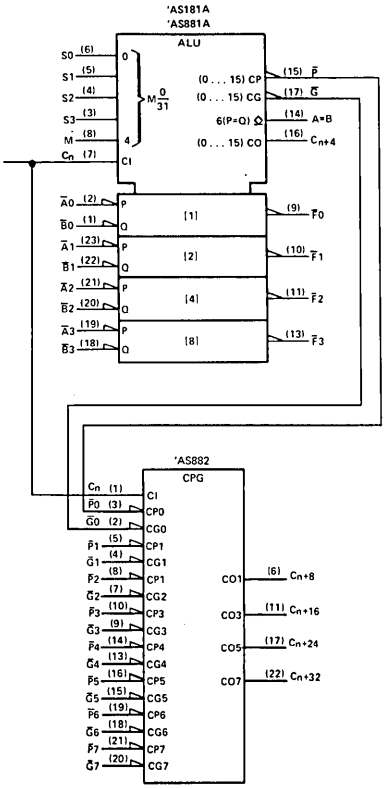

FIGURE 1
(USE WITH TABLE 1)

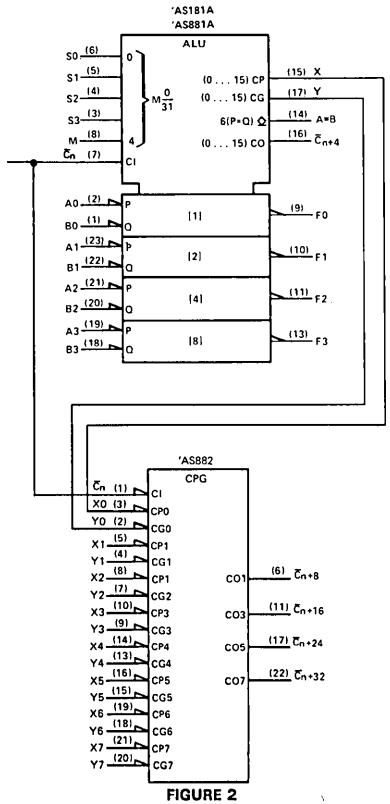

FIGURE 2
(USE WITH TABLE 2)

TABLE 1

SELECTION				ACTIVE-LOW DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A MINUS 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $\overline{A + B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H	L	L	L	F = $\overline{A}$B	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	F = A $\oplus$ B	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = A$\overline{B}$ PLUS (A + B)	F = A$\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B) PLUS 1	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	F = A$\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = A$\overline{B}$ PLUS A	F = A$\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

TABLE 2

SELECTION				ACTIVE-HIGH DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	$\overline{C}_n$ = H (no carry)	$\overline{C}_n$ = L (with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A PLUS 1
L	L	L	H	F = $\overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	F = $\overline{A}$B	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L	H	L	L	F = $\overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L	H	L	H	F = $\overline{B}$	F = (A + B) PLUS A$\overline{B}$	F = (A + B) PLUS A$\overline{B}$ PLUS 1
L	H	H	L	F = A $\oplus$ B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

*Each bit is shifted to the next more significant position.

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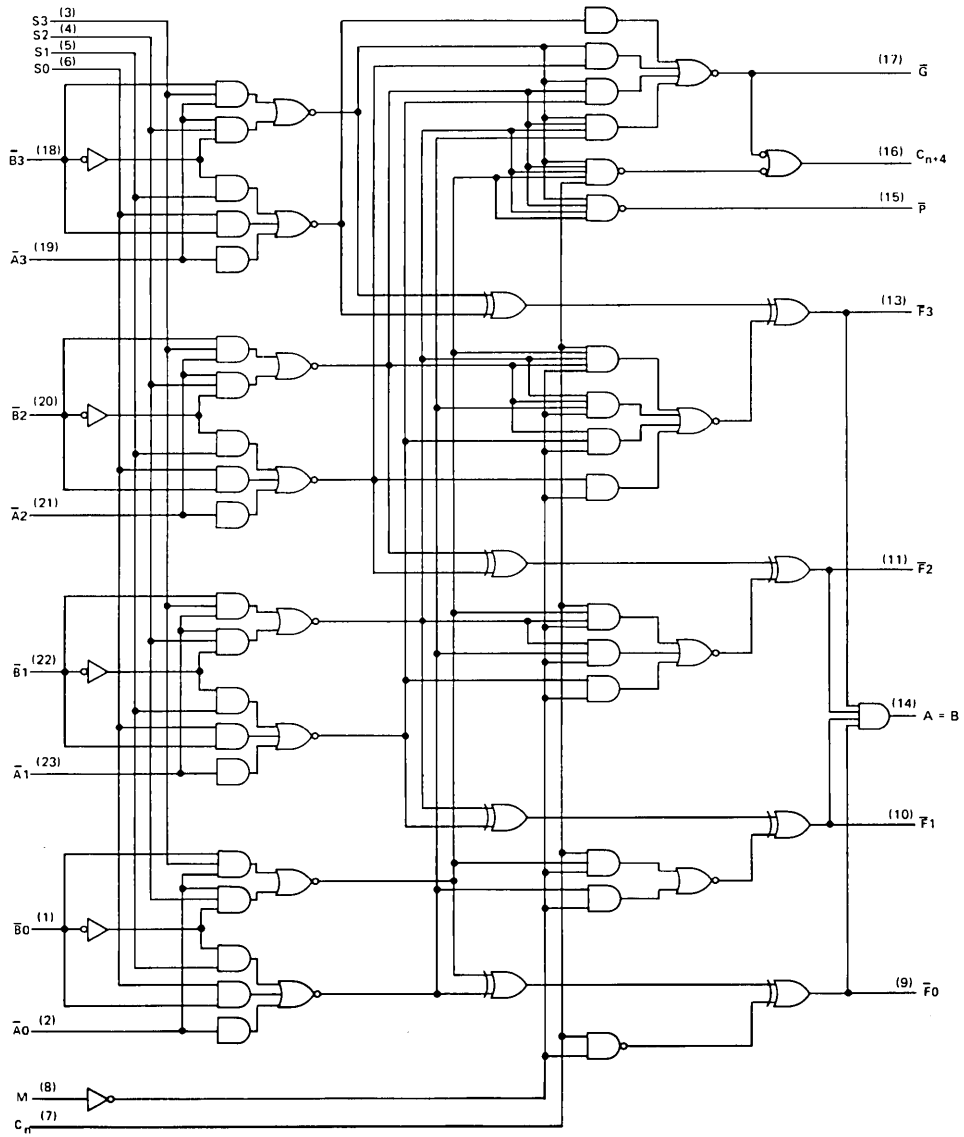
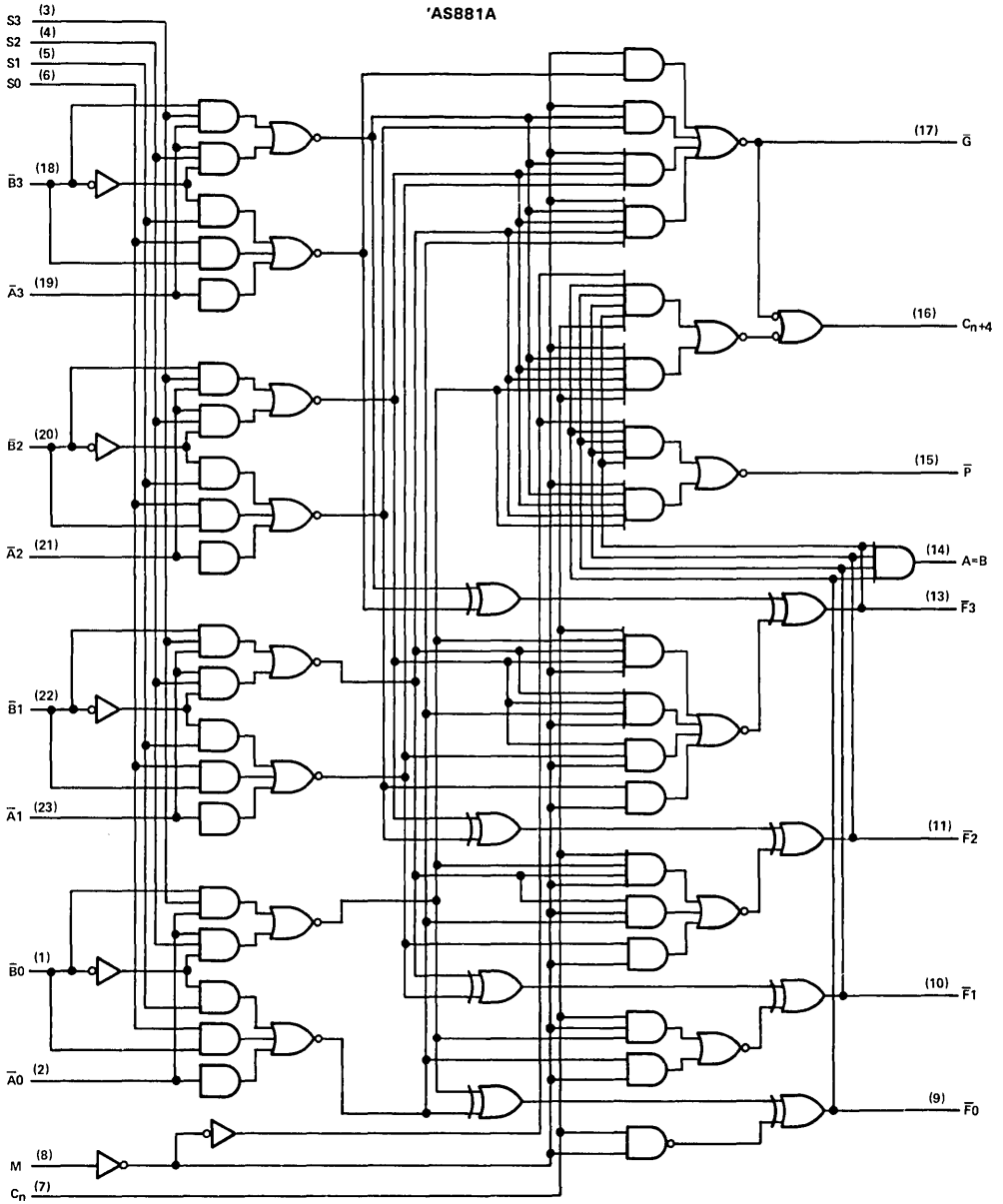
logic diagram (positive logic)

'AS181A



2

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage (A = B output only) . . . . . 7 V
Operating free-air temperature range: SN54AS181A, SN54AS881A . . . . . −55 °C to 125 °C
SN74AS181A, SN74AS881A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54AS'			SN74AS'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage	A = B output only			5.5			5.5	V
I_{OH}	High-level output current	All outputs except A = B and $\overline{G}$			−2			−2	mA
		$\overline{G}$			−3			−3	mA
I_{OL}	Low-level output current	All outputs except $\overline{G}$			20			20	mA
		$\overline{G}$			48			48	mA
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS'			SN74AS'			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	Any output except A=B	V_{CC} = 4.5 V,	I_{OH} = −2 mA	2.5	3.2		2.5	3.2		V
		V_{CC} = 4.75 V,	I_{OH} = −2 mA				2.7	3.2		V
	$\overline{G}$	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
I_{OH}	A=B	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	Any output except $\overline{G}$	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
	$\overline{G}$	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.4	0.5		0.4	0.5	V
I_I	M input	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	Any A or B input					0.3			0.3	
	Any S input					0.4			0.4	
	Carry input					0.6			0.6	
I_{IH}	M input	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	Any A or B input					60			60	
	Any S input					80			80	
	Carry input					120			120	
I_{IL}	M input	V_{CC} = 5.5 V,	V_I = 0.4 V			−2			−2	mA
	Any A or B input					−6			−6	
	Any S input					−8			−8	
	Carry input					−12			−12	
I_O§	All outputs except A = B and $\overline{G}$	V_{CC} = 5.5 V,	V_O = 2.25 V	−30	−45	−112	−30	−45	−112	mA
	$\overline{G}$				−165			−165		
I_{CC}		V_{CC} = 5.5 V	'AS181A		135	200		135	200	mA
			'AS881A		135	210		135	210	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

§The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

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switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω (280 Ω for A = B), T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF (15 pF for A = B), R_L = 500 Ω (280 Ω for A = B), T_A = MIN to MAX						UNIT
				'AS181A 'AS881A	SN54AS181A SN54AS881A			SN74AS181A SN74AS881A			
				MIN TYP† MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	C_n	C_{n+4}		5	2	7	11	2	7	9	ns
t_{pd}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	M = 0 V, S1 = S2 = 0 V, S0 = S3 = 4.5 V ($\overline{SUM}$ mode)	6	2	8	14	2	8	12	ns
t_{pd}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)	7	2	8	20	2	8	16	ns
t_{pd}	C_n	Any $\overline{F}$	M = 0 V ($\overline{SUM}$ or $\overline{DIFF}$ mode)	5	3	6	11	3	6	9	ns
t_{pd}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0 V, S1 = S2 = 0 V, S0 = S3 = 4.5 V ($\overline{SUM}$ mode)	4	2	5	9	2	5	7	ns
t_{pd}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)	5	2	6	12	2	6	9	ns
t_{pd}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0 V, S1 = S2 = 0 V, S0 = S3 = 4.5 V ($\overline{SUM}$ mode)	5	2	6	11	2	6	8	ns
t_{pd}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)	5	2	6	13	2	6	10	ns
t_{pd}	$\overline{A}i$ or $\overline{B}i$	$\overline{F}i$	M = 0 V, S1 = S2 = 0 V, S0 = S3 = 4.5 V ($\overline{SUM}$ mode)	5	2	5	11	2	5	8	ns
t_{pd}	$\overline{A}i$ or $\overline{B}i$	$\overline{F}i$	M = 0 V, S0 = S1 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)	5	2	6	12	2	6	10	ns
t_{pd}	$\overline{A}i$ or $\overline{B}i$	$\overline{F}i$	M = 4.5 V (LOGIC mode)	6	2	6	16	2	6	11	ns
t_{pd}	Any A or B	A = B	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)	12	4	14	26	4	14	21	ns

additional 'AS881A switching characteristics involving status checks (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
				'AS881A	SN54AS881A			SN74AS881A			
				MIN TYP† MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	C_n = 4.5V, M = 4.5 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V, Equality ($\overline{A}i = \overline{B}i$ or $\overline{A}i \neq \overline{B}i$)	8	2	10	19	2	10	15	ns
t_{pd}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	C_n = 4.5 V, M = 4.5 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V, Equality ($\overline{A}i = \overline{B}i$ or $\overline{A}i \neq \overline{B}i$)	10	2	12	24	2	12	18	ns
t_{pd}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	C_n = 4.5 V, M = 4.5 V, S2 = 4.5 V, S0 = S1 = S3 = 0 V, ($\overline{A}i = \overline{B}i$ = H or $\overline{A}i$ or $\overline{B}i$ = L)	8	2	10	19	2	10	15	ns
t_{pd}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	C_n = 4.5 V, M = 4.5 V, S2 = 4.5 V, S0 = S1 = S3 = 0 V, ($\overline{A}i = \overline{B}i$ = H or $\overline{A}i$ or $\overline{B}i$ = L)	11	2	13	25	2	13	19	ns

$t_{pd} = t_{PHL}$ or t_{PLH}

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

PARAMETER MEASUREMENT INFORMATION

$\overline{\text{SUM}}$ MODE TEST TABLE

FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH} / t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase

$\overline{\text{DIFF}}$ MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	Out-of Phase
t_{PLH} / t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4} or any $\overline{F}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	In -Phase

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
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PARAMETER MEASUREMENT INFORMATION

LOGIC MODE TEST TABLE
FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	Out-ot-Phase

INPUT BITS EQUAL/NOT EQUAL TEST TABLE
FUNCTION INPUTS: S0 = S3 = M = 4.5 V, S1 = S2 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	In-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	In-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	Out-of-Phase

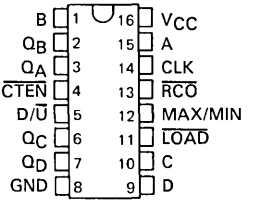
INPUT PAIRS HIGH/NOT HIGH TEST TABLE
FUNCTION INPUTS: S2 = M = 4.5 V, S0 = S1 = S3 = 0V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$, C_n	Remaining $\overline{B}$	$\overline{P}$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{P}$	In-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$, C_n	Remaining $\overline{B}$	C_{n+4}	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	C_{n+4}	Out-of-Phase

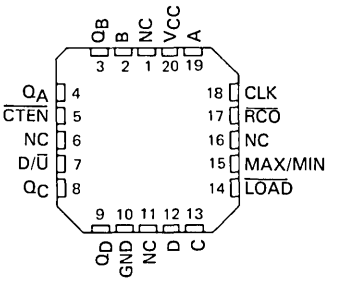
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- Single Down/Up Count Control Line
- Look-Ahead Circuitry Enhances Speed of Cascaded Counters
- Fully Synchronous in Count Modes
- Asynchronously Presettable with Load Control
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPS
- Dependable Texas Instruments Quality and Reliability

SN54ALS190, SN54ALS191 . . . J PACKAGE
SN74ALS190, SN74ALS191 . . . N PACKAGE
(TOP VIEW)



SN54ALS190, SN54ALS191 . . . FH PACKAGE
SN74ALS190, SN74ALS191 . . . FN PACKAGE
(TOP VIEW)



NC – no internal connection.

descriptions

The 'ALS190 and 'ALS191 are synchronous, reversible up/down counters. The 'ALS190 is a 4-bit decade counter and the 'ALS191 is a 4-bit binary counter. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input ($\overline{CTEN}$) is low. A high at $\overline{CTEN}$ inhibits counting. The direction of the count is determined by the level of the down/up (D/$\overline{U}$) input. When D/$\overline{U}$ is low, the counter counts up and when D/$\overline{U}$ is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs ($\overline{CTEN}$ and D/$\overline{U}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The CLK, D/$\overline{U}$, and $\overline{LOAD}$ inputs are buffered to lower the drive requirement, which significantly reduces the loading on, or current required by, clock drivers, etc., for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The ripple clock output produces a low-level output pulse under those same conditions but only while the clock input is low. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

The SN54ALS190 and SN54ALS191 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS190 and SN74ALS191 are characterized for operation from 0 °C to 70 °C.

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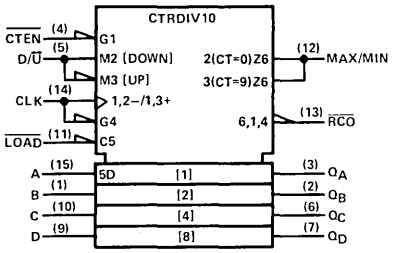
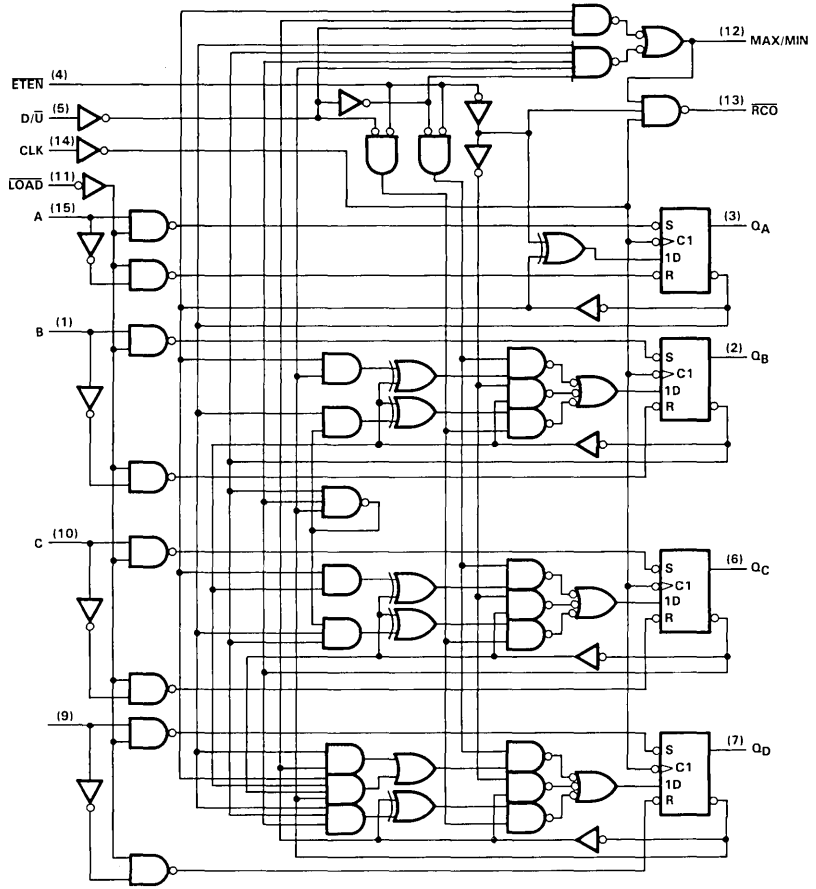
'ALS190 logic symbol

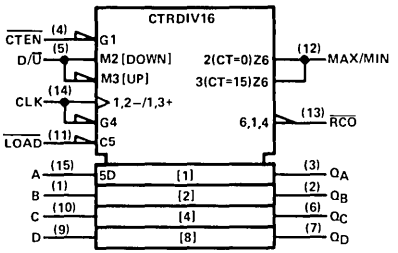


'ALS190 logic diagram (positive logic)

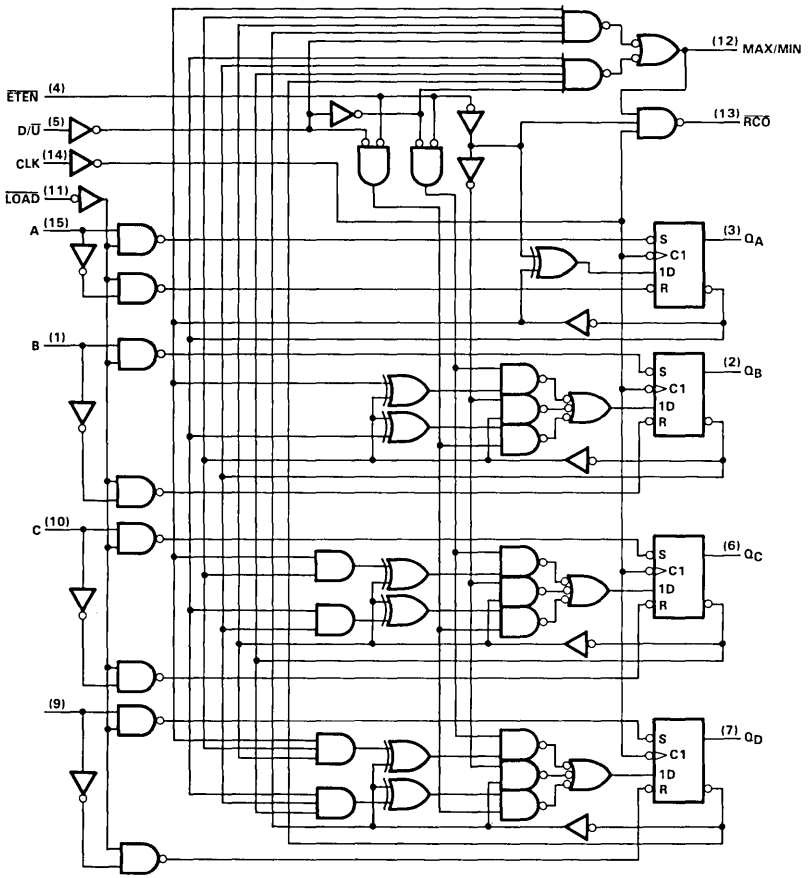


Pin numbers shown are for J and N packages.

'ALS191 logic symbol



'ALS191 logic diagram (positive logic)



Pin numbers shown are for J and N packages.

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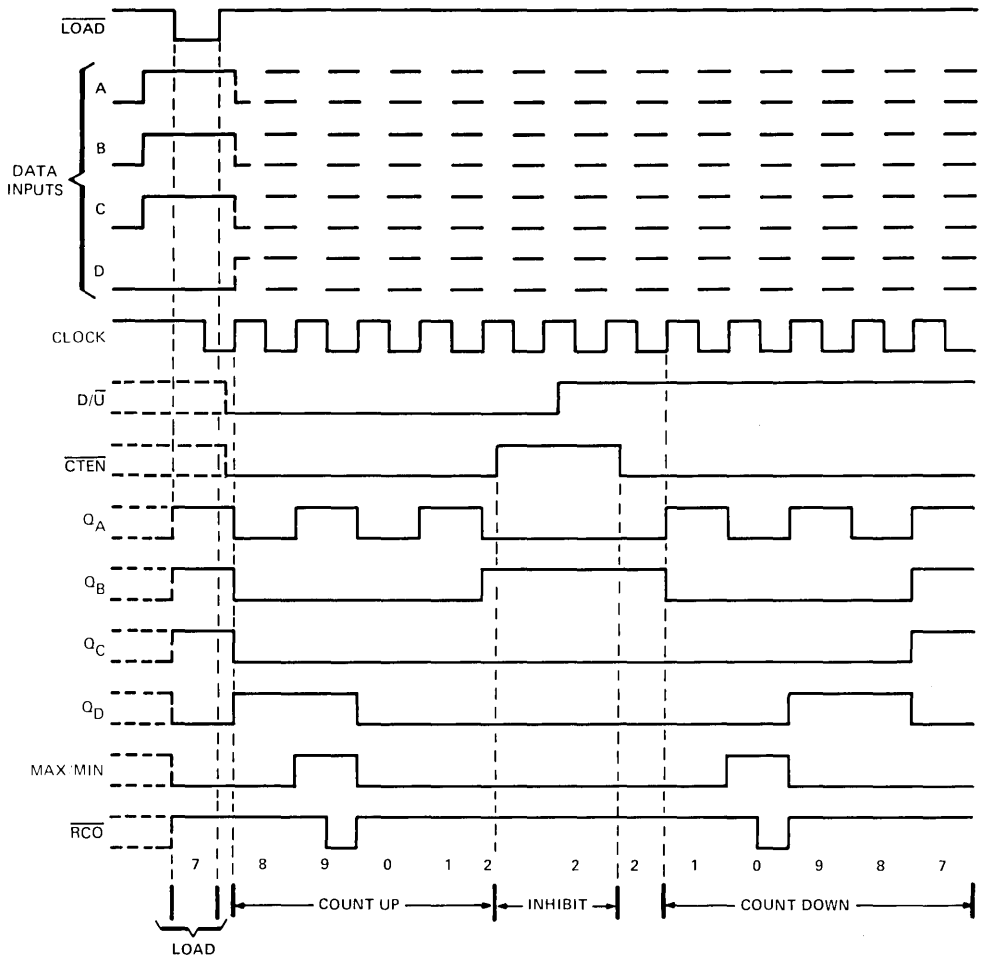
typical load, count, and inhibit sequences

'ALS190

Illustrated below is the following sequence:

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.

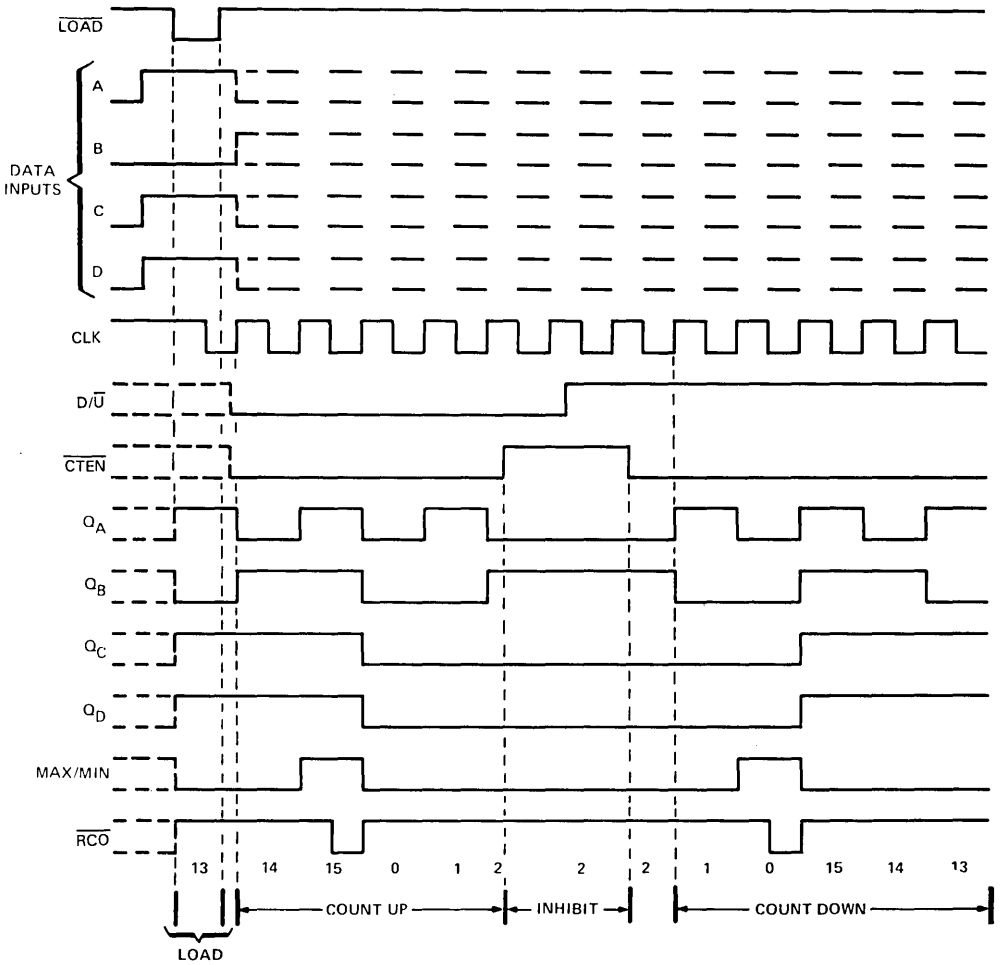


typical load, count, and inhibit sequences

'ALS191

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS190, SN54ALS191 . . . . . −55 °C to 125 °C
SN74ALS190, SN74ALS191 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS190 SN54ALS191			SN74ALS190 SN74ALS191			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4				mA
								8	
f_{clock}	Clock frequency	'ALS190	0		20	0		25	MHz
		'ALS191	0		25	0		30	
t_w	Pulse duration	CLK high	15			10			ns
		CLK low	15			10			
		$\overline{LOAD}$ low	25			20			
t_{su}	Setup time	Data before $\overline{LOAD}$↑	25			20			ns
		$\overline{CTEN}$ before CLK↑	20			20			
		D/$\overline{U}$ before CLK↑	20			20			
		$\overline{LOAD}$ inactive before CLK↑	20			20			
t_h	Hold time	Data after $\overline{LOAD}$↑	5			5			ns
		$\overline{CTEN}$ after CLK↑	0			0			
		D/$\overline{U}$ after CLK↑	0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS190 SN54ALS191			SN74ALS190 SN74ALS191			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4					V
		V_{CC} = 4.5 V	I_{OH} = −0.4 mA				2.7	3.4		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	$\overline{CTEN}$	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	All others					0.1			0.1	
I_{IH}	$\overline{CTEN}$	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	All others					20			20	
I_{IL}	$\overline{CTEN}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	All others					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}		V_{CC} = 5.5 V,	All inputs at 0 V		12	20		12	20	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS190 SN54ALS191		SN74ALS190 SN74ALS191		
			MIN	MAX	MIN	MAX	
f_{max}	'ALS190		20		25		MHz
	'ALS191		25		30		
t_{PLH}	$\overline{LOAD}$	Any Q	8	34	8	30	ns
t_{PHL}			8	34	8	30	
t_{PLH}	A, B, C, D	Any Q	4	25	4	21	ns
t_{PHL}			4	25	4	21	
t_{PLH}	CLK	$\overline{RCO}$	5	24	5	20	ns
t_{PHL}			5	24	5	20	
t_{PLH}	CLK	Any Q	3	22	3	18	ns
t_{PHL}			3	22	3	18	
t_{PLH}	CLK	MAX/MIN	8	34	8	31	ns
t_{PHL}			8	34	8	31	
t_{PLH}	D/$\overline{U}$	$\overline{RCO}$	15	42	15	37	ns
t_{PHL}			10	33	10	28	
t_{PLH}	D/$\overline{U}$	MAX/MIN	8	30	8	25	ns
t_{PHL}			8	30	8	25	
t_{PLH}	$\overline{CTEN}$	$\overline{RCO}$	4	21	4	18	ns
t_{PHL}			4	21	4	18	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

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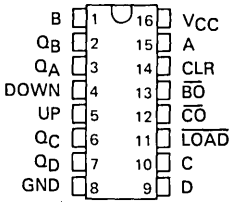
TYPES SN54ALS192, SN54ALS193, SN74ALS192, SN74ALS193
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

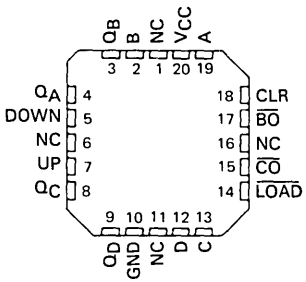
D2661, DECEMBER 1982

- **Look-Ahead Circuitry Enhances Cascaded Counters**
- **Fully Synchronous in Count Modes**
- **Parallel Asynchronous Load for Modulo-N Count Lengths**
- **Asynchronous Clear**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS192, SN54ALS193 . . . J PACKAGE
SN74ALS192, SN74ALS193 . . . N PACKAGE
(TOP VIEW)



SN54ALS192, SN54ALS193 . . . FH PACKAGE
SN74ALS192, SN74ALS193 . . . FN PACKAGE
(TOP VIEW)



NC — no internal connection.

description

The 'ALS192 and 'ALS193 are synchronous, reversible up/down counters. The 'ALS192 is a 4-bit decade counter and the 'ALS193 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered by a low-to-high-level transition of either count (clock) input (Up or Down). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs. The clock, count, and load inputs are buffered to lower the drive requirements. This significantly reduces the loading on clock drivers, etc., for long parallel words.

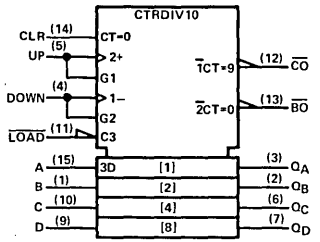
These counters were designed to be cascaded without the need for external circuitry. The borrow output (BO) produces a low-level pulse while the count is zero (all outputs low) and the count-down input is low. Similarly, the carry output ($\overline{CO}$) produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

The SN54ALS192 and SN54ALS193 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS192 and SN74ALS193 are characterized for operation from 0°C to 70°C.

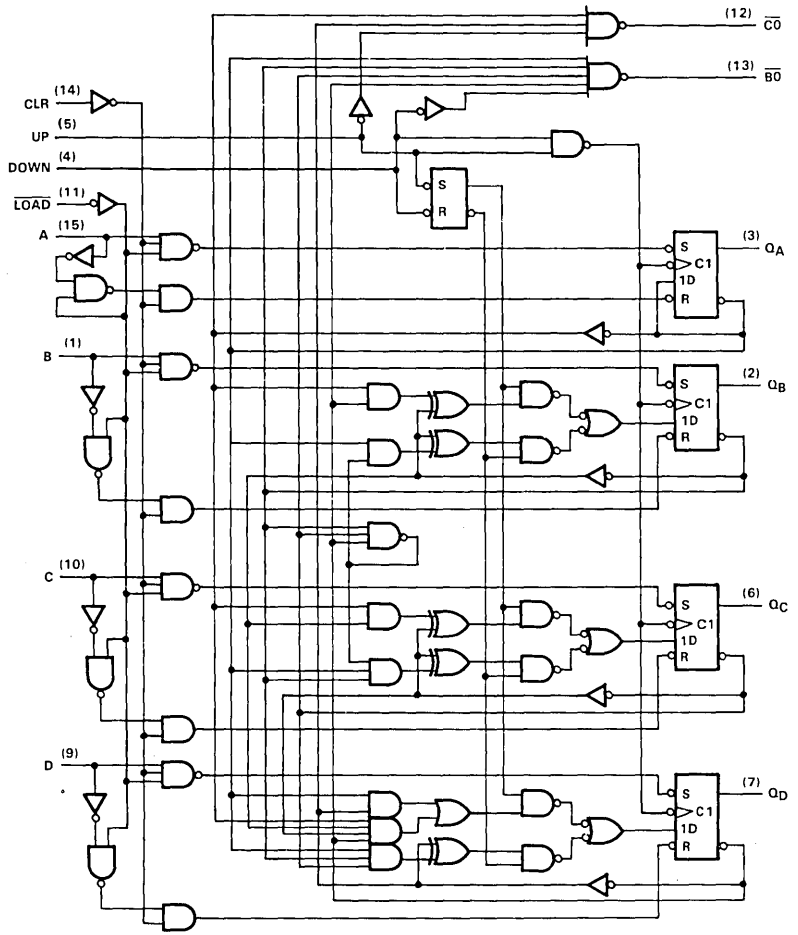
PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

'ALS192 logic symbol



'ALS192 logic diagram (positive logic)



Pin numbers shown are for J and N packages.

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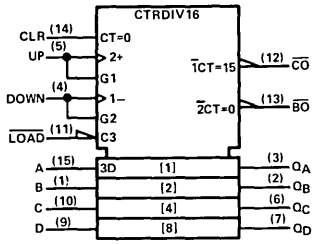
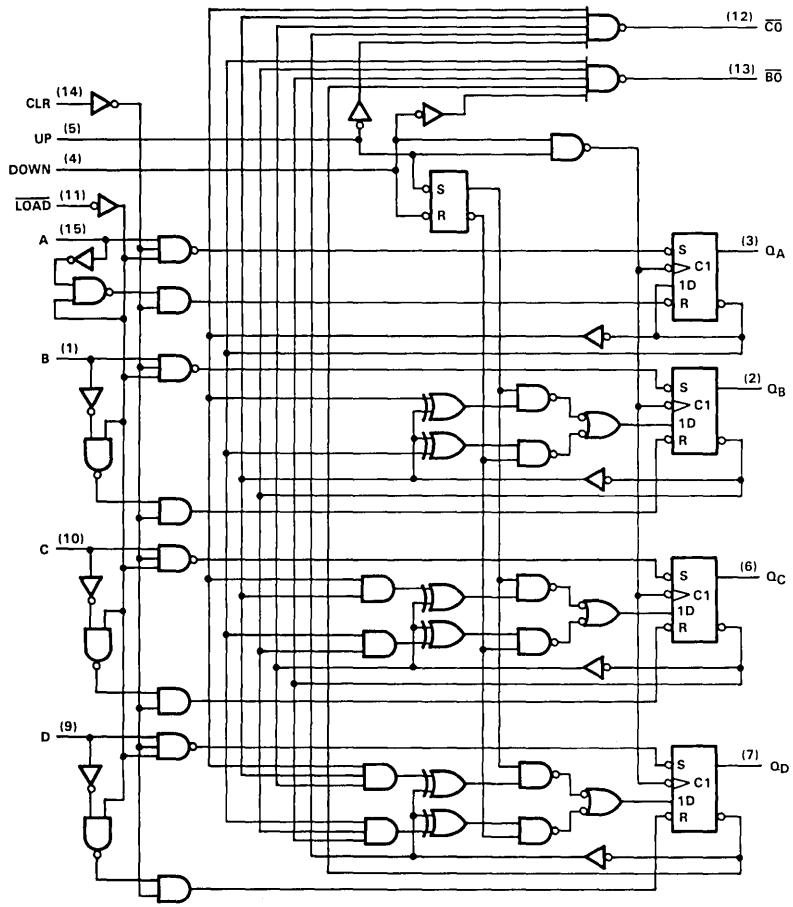
'ALS193 logic symbol



'ALS193 logic diagrams (positive logic)



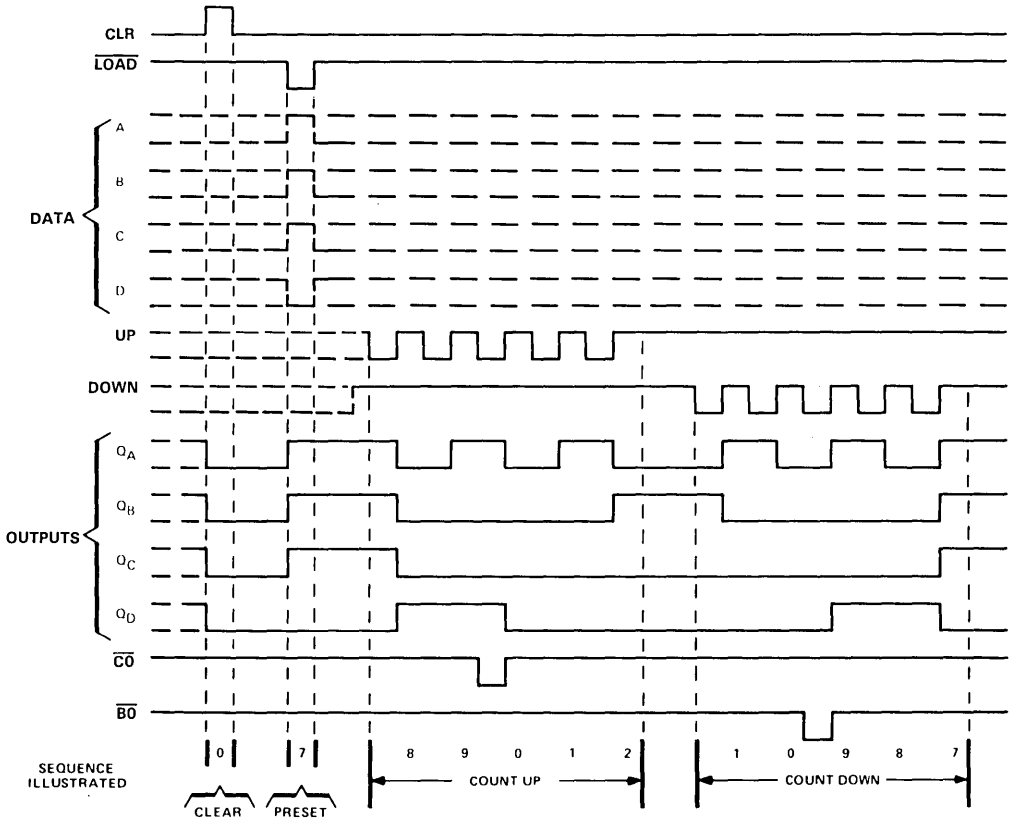
Pin numbers shown are for J and N packages.

typical clear, load, and count sequence

'ALS192

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

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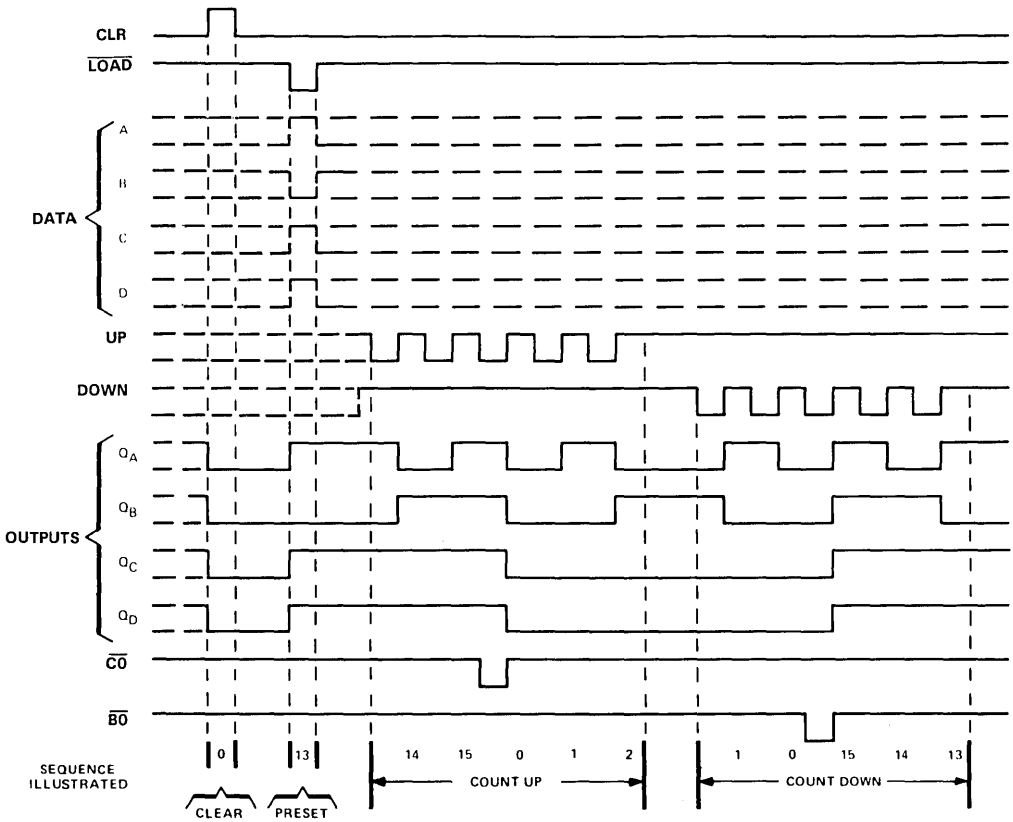
typical clear, load, and count sequences

'ALS193

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS192, SN54ALS193 . . . . . −55°C to 125°C
SN74ALS192, SN74ALS193 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS192 SN54ALS193			SN74ALS192 SN74ALS193			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency	'ALS192	0		20	0		25	MHz
		'ALS193	0		25	0		30	
t_w	Pulse duration	CLR high	10			10			ns
		$\overline{LOAD}$ low	25			20			
		Up or Down high	15			10			
		Up or Down low	15			10			
t_{su}	Setup time	Data before $\overline{LOAD}$↑	25			20			ns
		CLR inactive before Up↑ or Down↑	20			20			
		$\overline{LOAD}$ inactive before Up↑ or Down↑	20			20			
t_h	Hold time	Data after $\overline{LOAD}$↑	5			5			ns
		Up high after Down↑	0			0			
		Down high after Up↑	0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS192 SN54ALS193			SN74ALS192 SN74ALS193			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4					V
		V_{CC} = 4.5 V,	I_{OH} = −0.4 mA				2.7	3.4		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	Up, Down	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	All others					0.1			0.1	
I_{IH}	Up, Down	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	All others					20			20	
I_{IL}	Up, Down	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	All others					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		10	18		10	18	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with the clear and load inputs gounded, and all other inputs at 4.5 V.
Additional information on these products can be obtained from the factory as it becomes available.

TEXAS INSTRUMENTS
INCORPORATED
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switching characteristics (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS192 SN54ALS193		SN74ALS192 SN74ALS193		
			MIN	MAX	MIN	MAX	
f_{max}	'ALS192		20		25		MHz
	'ALS193		25		30		
t_{PLH}	Up	CO	4	19	4	16	ns
t_{PHL}			5	21	5	18	
t_{PLH}	Down	BO	4	19	4	16	ns
t_{PHL}			5	21	5	18	
t_{PLH}	Up or Down	Any Q	4	23	4	19	ns
t_{PHL}			4	20	4	17	
t_{PLH}	$\overline{LOAD}$	Any Q	8	35	8	30	ns
t_{PHL}			8	31	8	28	
t_{PHL}	CLR	Any Q	5	20	5	17	ns

NOTE 2: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

D2661, APRIL 1982

- **Choice of 64 × 4 or 32 × 8 Organization**
- **'ALS317 and 'ALS318 Are Open-Collector Versions of These Memories**
- **P-N-P Inputs and Buffer Outputs**
- **Full On-Chip Decoding and Fast Chip-Enable Simplify System Design**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These monolithic TTL memories feature Schottky clamping for high performance and a fast chip-select access time to enhance decoding at the system level.

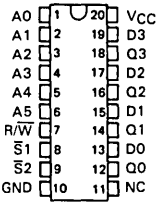
write cycle

Information to be stored in the memory is written into the location selected by the address inputs (A) when the chip-select ($\overline{S}1$ and $\overline{S}2$) and read-write (R/$\overline{W}$) inputs are low. While R/$\overline{W}$ is low, the memory outputs are in a high-impedance state. When a number of outputs are bus-connected, this high-impedance state neither loads nor drives the data bus; however, it permits the bus line to be driven by other active outputs or a passive pull-up.

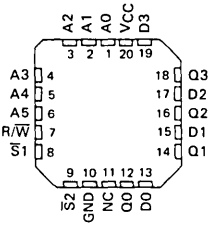
read cycle

Information stored in the memory is available at the outputs when R/$\overline{W}$ is high and $\overline{S}1$ and $\overline{S}2$ are low. When either chip-select input is high, the outputs are in a high-impedance state.

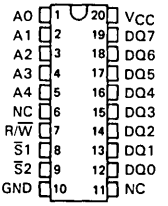
SN54ALS217 . . . J PACKAGE
SN74ALS217 . . . J OR N PACKAGE
(TOP VIEW)



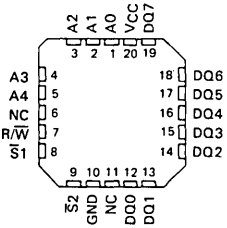
SN54ALS217 . . . FH PACKAGE
SN74ALS217 . . . FN PACKAGE
(TOP VIEW)



SN54ALS218 . . . J PACKAGE
SN74ALS218 . . . J OR N PACKAGE
(TOP VIEW)



SN54ALS218 . . . FH PACKAGE
SN74ALS218 . . . FN PACKAGE
(TOP VIEW)



NC — No internal connections

TEXAS INSTRUMENTS
INCORPORATED
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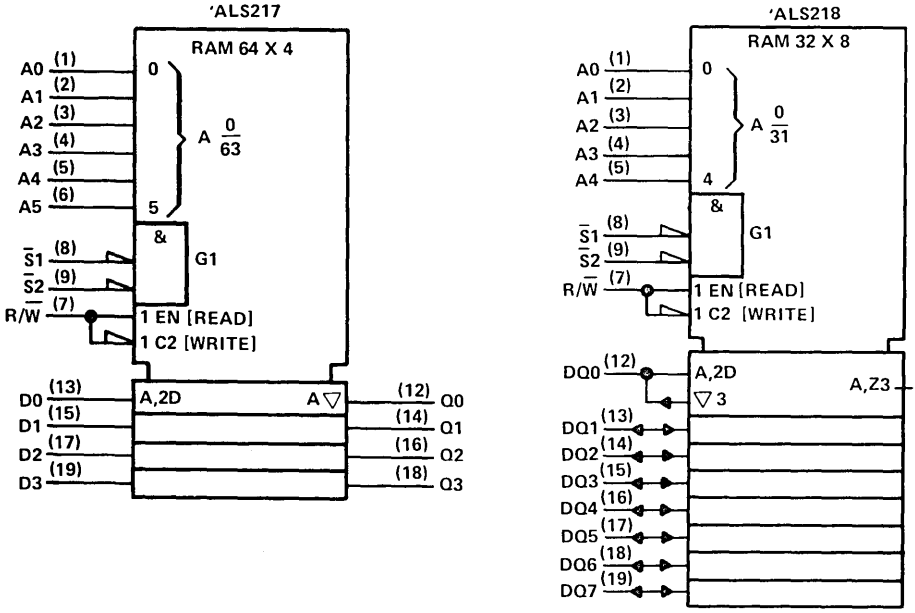
FUNCTION TABLE

FUNCTION	INPUTS $\overline{S1}$	$\overline{S2}$	R/$\overline{W}$	OUTPUTS
Write	L	L	L	Z
Read	L	L	H	Data stored
Inhibit	H	X	X	Z
	X	H	X	Z

2

logic symbols



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports of 'ALS218 . . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS217, SN54ALS218 . . . . . −55 °C to 125 °C
SN74ALS217, SN74ALS218 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS217 SN54ALS218			SN74ALS217 SN74ALS218			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1				mA
								−2.6	
I_{OL}	Low-level output current				12				mA
								24	
$t_{w(W)}$	Duration of write pulse		50			50			ns
t_{su}	Setup time	Address before R/$\overline{W}$↓	0			0			ns
		Data before R/$\overline{W}$↑	50			50			
		$\overline{S}$ low before R/$\overline{W}$↑	0			0			
t_h	Hold time after R/W↑	Address	0			0			ns
		Data	0			0			
		$\overline{S}$ low	0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS217 SN54ALS218			SN74ALS217 SN74ALS218			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.2					V
		V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	'ALS217 Q outputs	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	'ALS217 Q outputs	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	All inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	'ALS218 DQ ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	All inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	'ALS218 DQ ports▲					20			20	
I_{IL}	All inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	'ALS218 DQ ports▲					−0.2			−0.2	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			46			46		mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

▲For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

switching characteristics (see note 1)

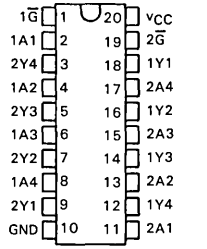
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS217 SN54ALS218			SN74ALS217 SN74ALS218			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(A)}$	A	Q or DQ		30			30		ns
$t_{a(S)}$	$\overline{S}$	Q or DQ		20			20		ns
t_{sr}	R/$\overline{W}$	Q or DQ		30			30		ns
$t_{dis(S)}$	$\overline{S}$	Q or DQ		14			14		ns
$t_{dis(R)}$	R/$\overline{W}$	Q or DQ		18			18		ns

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.

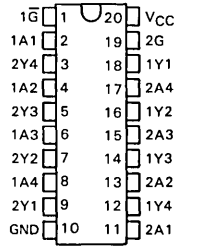
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- Included among the Package Options Are 20-Pin DIPs and Both Plastic and Ceramic Chip Carriers
- 'AS230 Has True and Complementary Outputs
- 'AS231 Has Complementary G and $\overline{G}$ Inputs
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- High Capacitive Drive Capability
- Current Sinking Capability Up to 64 mA
- Dependable Texas Instruments Quality and Reliability

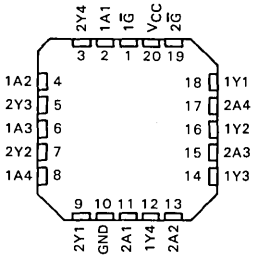
SN54AS230 . . . . J PACKAGE
SN74AS230 . . . . N PACKAGE
(TOP VIEW)



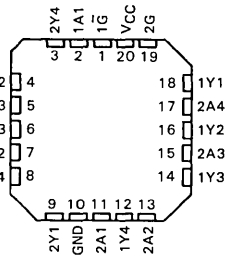
SN54AS231 . . . . J PACKAGE
SN74AS231 . . . . N PACKAGE
(TOP VIEW)



SN54AS230 . . . . FH PACKAGE
SN74AS230 . . . . FN PACKAGE
(TOP VIEW)



SN54AS231 . . . . FH PACKAGE
SN74AS231 . . . . FN PACKAGE
(TOP VIEW)



description

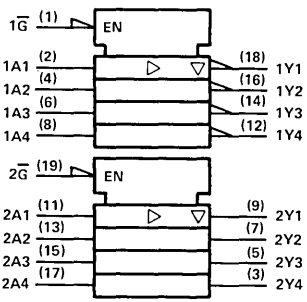
These octal buffers and line drivers are designed specifically to improve the performance of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs.

The SN74AS230 and SN74AS231 can be used to drive terminated lines down to 133 ohms.

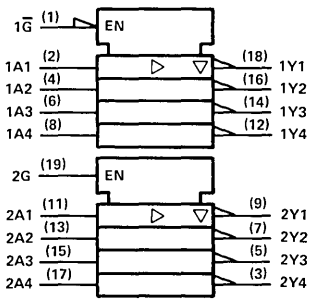
The SN54AS230 and SN54AS231 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS230 and SN74AS231 are characterized for operation from 0°C to 70°C.

logic symbols

'AS230



'AS231



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS230, SN54AS231 . . . . . −55°C to 125°C
SN74AS230, SN74AS231 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS230 SN54AS231			SN74AS230 SN74AS231			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−12	mA
							−15†	
I_{OL}	Low-level output current			48			48	mA
							64†	
T_A	Operating free-air temperature	−55		125	0		70	°C

† The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS230 SN54AS231			SN74AS230 SN74AS231			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2			2			
		V_{CC} = 4.75 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.55			0.55	V
		V_{CC} = 4.75 V,	I_{OL} = 64 mA						0.55	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.3			−0.3	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V			−115			−115	mA
I_{CC}	'AS230	V_{CC} = 5.5 V	Outputs high			12			12	mA
			Outputs low			50			50	
			Outputs disabled			28			28	
	'AS231	V_{CC} = 5.5 V	Outputs high			11			11	mA
			Outputs low			47			47	
			Outputs disabled			23			23	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 50 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS230			SN74AS230			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	1A	1Y		3.5			3.5		ns
t_{PHL}				3.5			3.5		
t_{PLH}	2A	2Y		4			4		ns
t_{PHL}				4			4		
t_{PZH}	$\overline{G}$	Y		6			6		ns
t_{PZL}				7			7		
t_{PHZ}				4			4		
t_{PLZ}				8			8		

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 50 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS231			SN74AS231			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y		3.5			3.5		ns
t_{PHL}				3.5			3.5		
t_{PZH}	$\overline{G}$	Y		6			6		ns
t_{PZL}				7			7		
t_{PHZ}				4			4		
t_{PLZ}				8			8		
t_{PZH}	G	Y		7			7		ns
t_{PZL}				8			8		
t_{PHZ}				7			7		
t_{PLZ}				9			9		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
INCORPORATED
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- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **P-N-P Inputs Reduce DC Loading**
- **Dependable Texas Instruments Quality and Reliability**

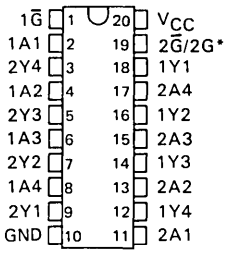
description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out and improved fan-in.

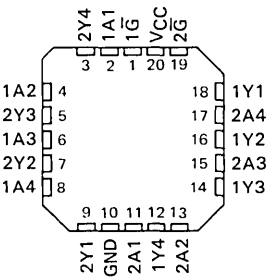
The -1 versions of the SN74ALS' parts are identical to their standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS' parts.

The SN54' family is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74' family is characterized for operation from 0 °C to 70 °C.

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . N PACKAGE
(TOP VIEW)



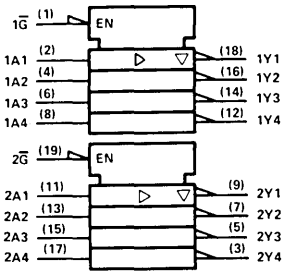
SN54ALS', SN54AS' . . . FH PACKAGE
SN74ALS', SN74AS' . . . FN PACKAGE
(TOP VIEW)



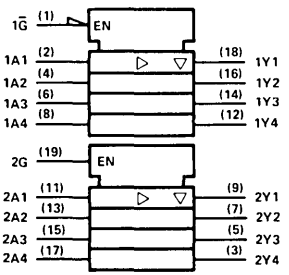
*$2\overline{G}$ for 'ALS240, 'AS240 or 2G for 'ALS241, 'AS241

logic symbols

'ALS240, 'AS240



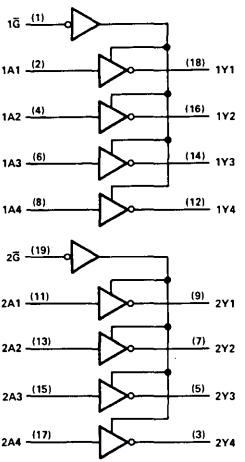
'ALS241, 'AS241



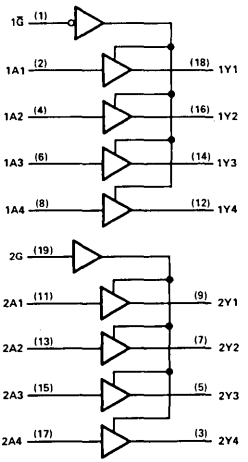
Pin numbers shown are for J and N packages.

logic diagrams (positive logic)

'ALS240, 'AS240



'ALS241, 'AS241



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS240, SN54ALS241 . . . . . −55°C to 125°C
SN74ALS240, SN74ALS241 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

2

recommended operating conditions

		SN54ALS240 SN54ALS241			SN74ALS240 SN74ALS241			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12				mA
							−15	
I_{OL}	Low-level output current			12				mA
							24	
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS240-1 and SN74ALS241-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS240 SN54ALS241			SN74ALS240 SN74ALS241			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V, I_{OH} = −3 mA		2.4	3.2		2.4	3.2		V
		V_{CC} = 4.5 V, I_{OH} = −12 mA		2						
		V_{CC} = 4.5 V, I_{OH} = −15 mA					2			
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 12 mA			0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, I_{OL} = 24 mA (I_{OL} = 48 mA for -1 versions)						0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V, V_O = 2.7 V				20			20	μA
I_{OZL}		V_{CC} = 5.5 V, V_O = 0.4 V				−20			−20	μA
I_I		V_{CC} = 5.5 V, V_I = 7 V				0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V, V_I = 2.7 V				20			20	μA
I_{IL}		V_{CC} = 5.5 V, V_I = 0.4 V				−0.1			−0.1	mA
I_O§		V_{CC} = 5.5 V, V_O = 2.25 V		−30		−112	−30		−112	mA
I_{CC}	'ALS240	V_{CC} = 5.5 V	Outputs high		4	10		4	10	mA
			Outputs low		13	22		13	22	
			Outputs disabled		14	25		14	25	
	'ALS241		Outputs high		9	15		9	15	
			Outputs low		15	26		15	26	
			Outputs disabled		17	30		17	30	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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'ALS240 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS240		SN74ALS240		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	12	3	10	ns
t_{PHL}			2	11	2	9	
t_{PZH}	$\overline{G}$	Y	5	15	5	13	ns
t_{PZL}			5	20	5	18	
t_{PHZ}	$\overline{G}$	Y	2	12	2	10	ns
t_{PLZ}			3	20	3	16	

'ALS241 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS241		SN74ALS241		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	14	3	11	ns
t_{PHL}			3	13	3	10	
t_{PZH}	$1\overline{G}$	Y	7	25	7	21	ns
t_{PZL}			7	25	7	21	
t_{PHZ}	$1\overline{G}$	Y	2	15	2	13	ns
t_{PLZ}			3	20	3	15	
t_{PZH}	2G	Y	7	25	7	21	ns
t_{PZL}			7	25	7	21	
t_{PHZ}	2G	Y	2	15	2	13	ns
t_{PLZ}			3	20	3	15	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS240, SN54AS241 . . . . . −55 °C to 125 °C
SN74AS240, SN74AS241 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS240 SN54AS241			SN74AS240 SN74AS241			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−12	mA
							−15†	
I_{OL}	Low-level output current			48			48	mA
							64†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS240 SN54AS241			SN74AS240 SN74AS241			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2			2			
		V_{CC} = 4.75 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.55			0.55	V
		V_{CC} = 4.75 V,	I_{OL} = 64 mA						0.55	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V		−0.3			−0.3		mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V		−115			−115		mA
I_{CC}	'AS240	V_{CC} = 5.5 V	Outputs high		11			11		mA
			Outputs low		47			47		
			Outputs disabled		23			23		
	'AS241		Outputs high		12			12		
			Outputs low		53			53		
			Outputs disabled		33			33		

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS240 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS240			SN74AS240			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y		3.5			3.5		ns
t_{PHL}				3.5			3.5		
t_{PZH}	$\overline{G}$	Y		6			6		ns
t_{PZL}				7			7		
t_{PHZ}	$\overline{G}$	Y		4			4		ns
t_{PLZ}				8			8		

'AS241 switching characteristics (see note 1)

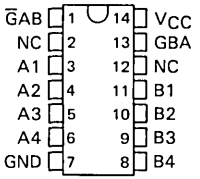
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS241			SN74AS241			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y		4			4		ns
t_{PHL}				4			4		
t_{PZH}	$1\overline{G}$	Y		6			6		ns
t_{PZL}				7			7		
t_{PHZ}	$1\overline{G}$	Y		4			4		ns
t_{PLZ}				8			8		
t_{PZH}	2G	Y		7			7		ns
t_{PZL}				8			8		
t_{PHZ}	2G	Y		6			6		ns
t_{PLZ}				9			9		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

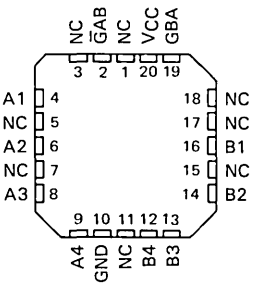
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- 2-Way Asynchronous Communication Between Data Buses
- P-N-P Inputs Reduce Loading
- Dependable Texas Instruments Quality and Reliability

SN54' . . . J PACKAGE
SN74' . . . N PACKAGE
(TOP VIEW)



SN54' . . . FH PACKAGE
SN74' . . . FN PACKAGE
(TOP VIEW)



NC—No Internal connection

description

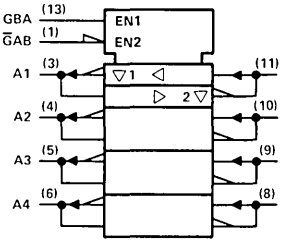
These four-data-line transceivers are designed for asynchronous two-way communications between data buses. The SN74' devices can be used to drive terminated lines down to 133 ohms.

The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS' parts.

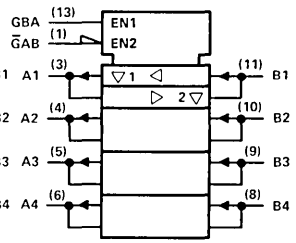
The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

logic symbol

'ALS242, 'AS242

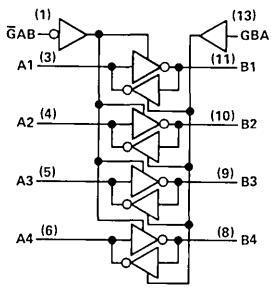


'ALS243, 'AS243

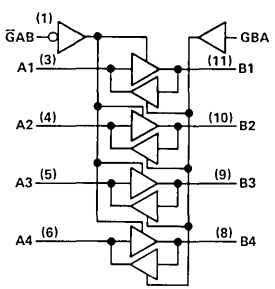


logic diagrams (positive logic)

'ALS242, 'AS242



'ALS243, 'AS243



Pin numbers shown are for J and N packages.

FUNCTION TABLE

INPUTS		'ALS242	'ALS243
GAB	GBA	'AS242	'AS243
L	L	$\overline{A}$ to B	A to B
H	H	$\overline{B}$ to A	B to A
H	L	Isolation	Isolation
L	H	Latch A and B ($A=\overline{B}$)	Latch A and B ($A=B$)

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS242, SN54ALS243 . . . . . −55°C to 125°C
SN74ALS242, SN74ALS243 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS242 SN54ALS243			SN74ALS242 SN74ALS243			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12				mA
							−15	
I_{OL}	Low-level output current			12				mA
							24	
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS242-1 and SN74ALS243-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS242 SN54ALS243			SN74ALS242 SN74ALS243			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for -1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports▲					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports▲					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS242	V_{CC} = 5.5 V	Outputs high		10	20		10	20	mA
			Outputs low		14	26		14	26	
			Outputs disabled		15	27		15	27	
	'ALS243		Outputs high		15	25		15	25	
			Outputs low		20	30		20	30	
			Outputs disabled		21	32		21	32	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
▲For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

'ALS242 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_1 = 500 Ω, R_2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS242		SN74ALS242		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	3	15	3	11	ns
t_{PHL}			2	14	2	10	
t_{PZH}	$\overline{G}$AB	B	4	22	4	18	ns
t_{PZL}			7	25	7	21	
t_{PHZ}	$\overline{G}$AB	B	2	16	2	14	ns
t_{PLZ}			4	28	4	22	
t_{PZH}	GBA	A	4	22	4	18	ns
t_{PZL}			7	25	7	21	
t_{PHZ}	GBA	A	2	16	2	14	ns
t_{PLZ}			4	28	4	22	

'ALS243 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_1 = 500 Ω, R_2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS243		SN74ALS243		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	4	15	4	11	ns
t_{PHL}			4	15	4	11	
t_{PZH}	$\overline{G}$AB	B	7	25	7	20	ns
t_{PZL}			7	25	7	20	
t_{PHZ}	$\overline{G}$AB	B	2	16	2	14	ns
t_{PLZ}			4	30	4	25	
t_{PZH}	GBA	A	7	25	7	20	ns
t_{PZL}			7	25	7	20	
t_{PHZ}	GBA	A	2	16	2	14	ns
t_{PLZ}			4	30	4	25	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54AS242, SN54AS243 . . . . . −55 °C to 125 °C
SN74AS242, SN74AS243 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS242 SN54AS243			SN74AS242 SN74AS243			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−12	mA
							−15†	
I_{OL}	Low-level output current			48			48	mA
							64†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS242 SN54AS243			SN74AS242 SN74AS243			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2			2			
		V_{CC} = 4.75 V,	I_{OH} = −15 mA				2			
		V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.55			0.55	
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 64 mA						0.55	V
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports▲									
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.1			−0.1		mA
	A or B ports▲				−0.1			−0.1		
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V		−115			−115		mA
I_{CC}	'AS242	V_{CC} = 5.5 V	Outputs high		18			18		mA
			Outputs low		36			36		
			Outputs disabled		24			24		
	'AS243		Outputs high		22			22		
			Outputs low		43			43		
			Outputs disabled		33			33		

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
▲For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

Additional information on these products can be obtained from the factory as it becomes available.

2

'AS242 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS242			SN74AS242			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	B or A		4			4		ns
t_{PHL}				4			4		
t_{PZH}	$\overline{G}$AB	B		6			6		ns
t_{PZL}				7			7		
t_{PHZ}	$\overline{G}$AB	B		4			4		ns
t_{PLZ}				8			8		
t_{PZL}	GBA	A		7			7		ns
t_{PZL}				8			8		
t_{PHZ}	GBA	A		6			6		ns
t_{PLZ}				9			9		

'AS243 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS243			SN74AS243			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	B or A		3.5			3.5		ns
t_{PHL}				3.5			3.5		
t_{PZH}	$\overline{G}$AB	B		7			7		ns
t_{PZL}				8			8		
t_{PHZ}	$\overline{G}$AB	B		6			6		ns
t_{PLZ}				9			9		
t_{PZH}	GBA	A		7			7		ns
t_{PZL}				8			8		
t_{PHZ}	GBA	A		6			6		ns
t_{PLZ}				9			9		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

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D2661, DECEMBER 1982

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce DC Loading
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

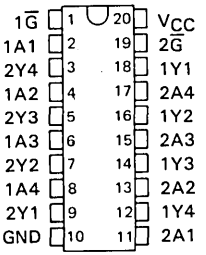
description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'ALS240, 'ALS241, 'AS240, and 'AS241, these devices provide the choice of selected combinations of inverting outputs, symmetrical $\overline{G}$ (active-low input control) inputs, and complementary G and $\overline{G}$ inputs.

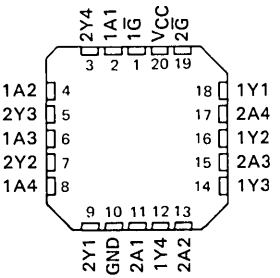
The -1 version of the SN74ALS244 is identical to the standard version except that the recommended maximum I_{OL} is increased to 48 milliamperes. There is no -1 version of the SN54ALS244.

The SN54ALS244 and SN54AS244 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS244 and SN74AS244 are characterized for operation from 0 °C to 70 °C.

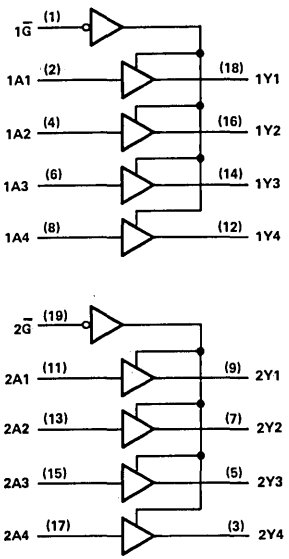
SN54ALS244, SN54AS244 . . . J PACKAGE
SN74ALS244, SN74AS244 . . . N PACKAGE
(TOP VIEW)



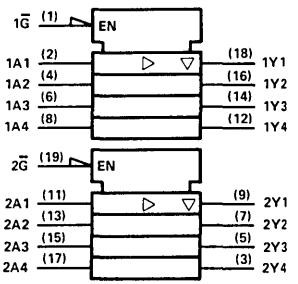
SN54ALS244, SN54AS244 . . . FH PACKAGE
SN74ALS244, SN74AS244 . . . FN PACKAGE
(TOP VIEW)



logic diagram (positive logic)



logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS244 . . . . . −55 °C to 125 °C
SN74ALS244 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

2

recommended operating conditions

		SN54ALS244			SN74ALS244			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12				mA
							−15	
I_{OL}	Low-level output current			12				mA
							24	
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS244-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS244			SN74ALS244			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		V
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V (I_{OL} = 48 mA for -1 version)	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		9	15		9	15	mA
		Outputs low		15	26		15	26	
		Outputs disabled		17	30		17	30	

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS244		SN74ALS244		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	14	3	11	ns
t_{PHL}			3	13	3	10	
t_{PZH}	$\overline{G}$	Y	7	25	7	21	ns
t_{PZL}			7	25	7	21	
t_{PHZ}	$\overline{G}$	Y	2	12	2	10	ns
t_{PLZ}			3	18	3	15	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS244 . . . . . −55°C to 125°C
SN74AS244 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

2

recommended operating conditions

		SN54AS244			SN74AS244			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−12	mA
							−15†	
I_{OL}	Low-level output current			48			48	mA
							64†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limit applies only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS244			SN74AS244			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2			2			
	V_{CC} = 4.75 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.55			0.55	V
	V_{CC} = 4.75 V,	I_{OL} = 64 mA						0.55	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.3			−0.3		mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V		−115			−115		mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		11			11		mA
		Outputs low		52			52		
		Outputs disabled		34			34		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

1

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switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS244			SN74AS244			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y		4			4		ns
t_{PHL}				4			4		
t_{PZH}	$\overline{G}$	Y		7			7		ns
t_{PZL}				8			8		
t_{PHZ}	$\overline{G}$	Y		6			6		ns
t_{PLZ}				9			9		

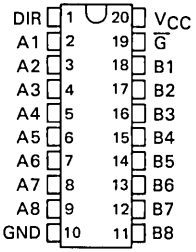
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

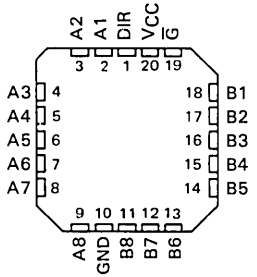
D2661, DECEMBER 1982

- 3-State Outputs Drive Bus Lines Directly
- P-N-P Inputs Reduce Dc Loading
- 'AS Version in Development. Data Will Be Provided As It Becomes Available. Contact the Factory for Latest Information
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS245, SN54AS245 . . . J PACKAGE
SN74ALS245, SN74AS245 . . . N PACKAGE
(TOP VIEW)



SN54ALS245, SN54AS245 . . . FH PACKAGE
SN74ALS245, SN74AS245 . . . FN PACKAGE
(TOP VIEW)



description

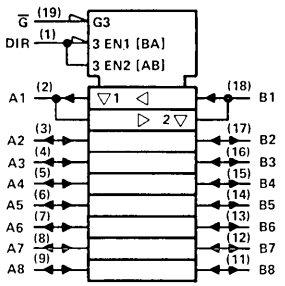
These octal bus transceivers are designed for synchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

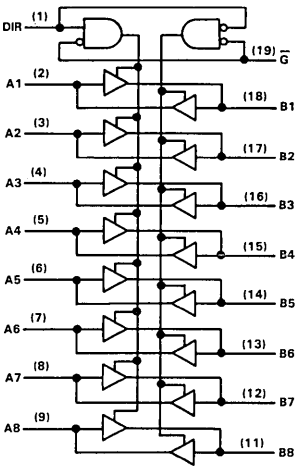
The -1 version of the SN74ALS245 is identical to the standard version except that the recommended maximum I_{OL} is increased to 48 milliamperes. There is no -1 version of the SN54ALS245.

The SN54ALS245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS245 is characterized for operation from 0°C to 70°C.

logic symbol



logic diagram (positive logic)



Pin numbers shown are for J and N packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS245 . . . . . −55°C to 125°C
SN74ALS245 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS245			SN74ALS245			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12				mA
							−15	
I_{OL}	Low-level output current			12				mA
							24	
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS245-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS245			SN74ALS245			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V, I_{OH} = −3 mA		2.4	3.2		2.4	3.2		V
		V_{CC} = 4.5 V, I_{OH} = −12 mA		2						
		V_{CC} = 4.5 V, I_{OH} = −15 mA					2			
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 12 mA			0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for -1 versions)						0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V, V_I = 7 V				0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V, V_I = 5.5 V				0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V, V_I = 2.7 V				20			20	μA
	A or B ports▲					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V, V_I = 0.4 V				−0.1			−0.1	mA
	A or B ports▲					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V, V_O = 2.25 V		−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		30	48		30	45	mA
			Outputs low		36	60		36	55	
			Outputs disabled		38	63		38	58	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
▲For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS245		SN74ALS245		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	3	15	3	10	ns
t_{PHL}			3	13	3	10	
t_{PZH}	$\overline{G}$	A or B	7	25	8	20	ns
t_{PZL}			10	30	10	26	
t_{PHZ}	$\overline{G}$	A or B	3	18	3	16	ns
t_{PLZ}			4	20	4	18	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
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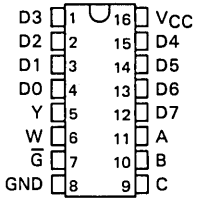
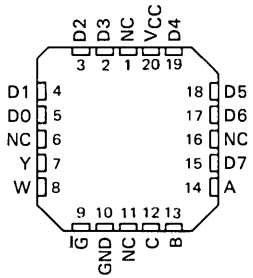
D2661, APRIL 1982

- **Three-State Versions of 'ALS151 and 'AS151**
- **Three-State Outputs Interface Directly with System Bus**
- **Performs Parallel-to-Serial Conversion**
- **Complementary Outputs Provide True and Inverted Data**
- **Fully Compatible with Most TTL Circuits**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS251, SN54AS251 . . . J PACKAGE
SN74ALS251, SN74AS251 . . . N PACKAGE
(TOP VIEW)



SN54ALS251, SN54AS251 . . . FH PACKAGE
SN74ALS251, SN74AS251 . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection.

description

These data selectors/multiplexers contain full binary decoding to select one-of-eight data sources and feature strobe-controlled complementary three-state outputs.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state), the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Both outputs are controlled by the strobe ($\overline{G}$). The outputs are disabled when $\overline{G}$ is high.

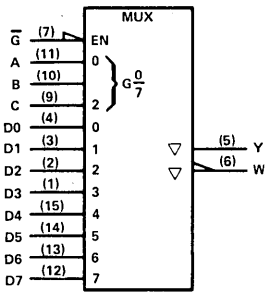
The SN54ALS251 and SN54AS251 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS251 and SN74AS251 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	$\overline{G}$		
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

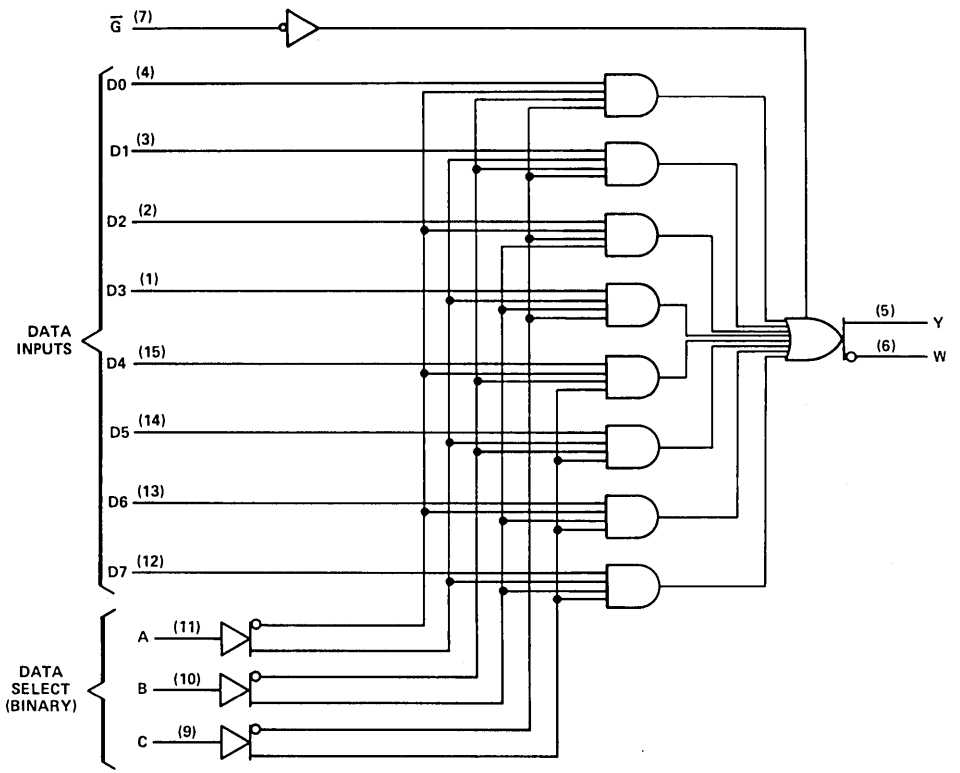
D0, D1 . . . D7 = the level of the respective D input

logic symbol



Pin numbers shown are for J and N packages.

logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS251, SN54AS251 . . . . . −55 °C to 125 °C
SN74ALS251, SN74AS251 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

		SN54ALS251			SN74ALS251			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS251			SN74ALS251			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
		V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	A, B, C	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	A, B, C	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	A, B, C	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	All others					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	Inputs at 4.5 V		7.5			7.5		mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS251			SN74ALS251			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, or C	Y		7.5			7.5		ns
t_{PHL}				10.5			10.5		
t_{PLH}	A, B, or C	W		10.5			10.5		ns
t_{PHL}				9.5			9.5		
t_{PLH}	Any D	Y		4			4		ns
t_{PHL}				6			6		
t_{PLH}	Any D	W		6			6		ns
t_{PHL}				6			6		
t_{PZH}	$\overline{G}$	Y		4			4		ns
t_{PZL}				5			5		
t_{PZH}	$\overline{G}$	W		4			4		ns
t_{PZL}				5			5		
t_{PHZ}	$\overline{G}$	Y		3.5			3.5		ns
t_{PLZ}				5			5		
t_{PHZ}	$\overline{G}$	W		3.5			3.5		ns
t_{PLZ}				5			5		

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

recommended operating conditions

		SN54AS251			SN74AS251			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−12	mA
							−15†	
I_{OL}	Low-level output current			32			32	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS251			SN74AS251			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2		2.4	3.2		V
	V_{CC} = 4.75 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5		0.25	0.5	V
	V_{CC} = 4.75 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.3			−0.3		mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			28			28		mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

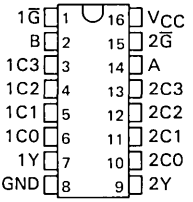
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX					UNIT
			'AS251	SN54AS251			SN74AS251		
			TYP‡	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, or C	Y			5			5		ns
t_{PHL}					5			5		
t_{PLH}	A, B, or C	W			4.5			4.5		ns
t_{PHL}					4.5			4.5		
t_{PLH}	Any D	Y			3			3		ns
t_{PHL}					4			4		
t_{PLH}	Any D	W			3			3		ns
t_{PHL}					2.5			2.5		
t_{PZH}	$\overline{G}$	Y			5			5		ns
t_{PZL}					6			6		
t_{PZH}	$\overline{G}$	W			5			5		ns
t_{PZL}					6			6		
t_{PHZ}	$\overline{G}$	Y			3			3		ns
t_{PLZ}					4			4		
t_{PHZ}	$\overline{G}$	W			3			3		ns
t_{PLZ}					4			4		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

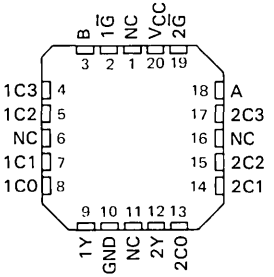
Additional information on these products can be obtained from the factory as it becomes available.

- **Three-State Versions of 'ALS153 and 'AS153**
- **Permits Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **Fully Compatible with Most TTL Circuits**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS253, SN54AS253 . . . J PACKAGE
SN74ALS253, SN74AS253 . . . N PACKAGE
(TOP VIEW)



SN54ALS253, SN54AS253 . . . FH PACKAGE
SN74ALS253, SN74AS253 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe ($\overline{G}$). The output is disabled when its strobe is high.

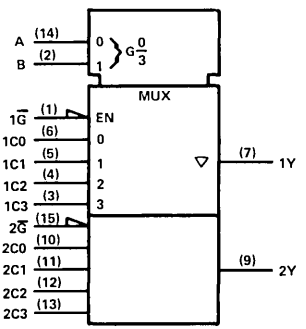
The SN54ALS253 and SN54AS253 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS253 and SN74AS253 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

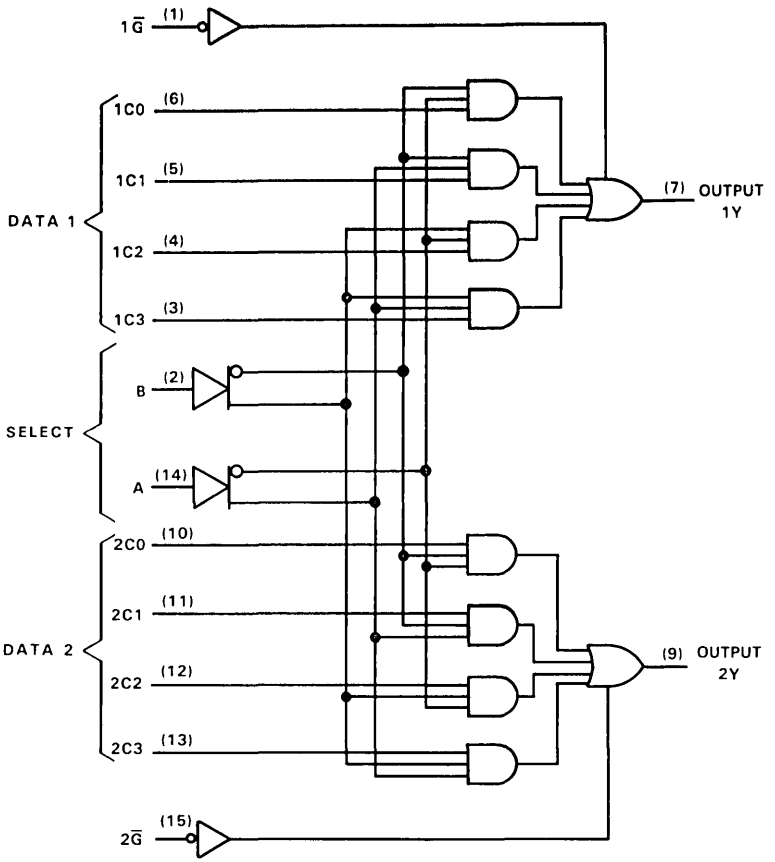
Address inputs A and B are common to both sections.

logic symbol



Pin numbers shown are for J and N packages.

logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS253, SN54AS253 . . . . . −55 °C to 125 °C
SN74ALS253, SN74AS253 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS253			SN74ALS253			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS253			SN74ALS253			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
		V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	A, B	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	A, B	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	A, B	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	All others					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		5			5		mA
			Outputs low		6.4			6.4		
			Outputs disabled		7.6			7.6		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS253			SN74ALS253			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Any Y		7.5			7.5		ns
t_{PHL}				9			9		
t_{PLH}	Data (Any C)	Any Y		4			4		ns
t_{PHL}				6			6		
t_{PZH}	$\overline{G}$	Any Y		4			4		ns
t_{PZL}				5			5		
t_{PHZ}	$\overline{G}$	Any Y		4			4		ns
t_{PLZ}				5			5		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

recommended operating conditions

		SN54AS253			SN74AS253			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−12	mA
							−15†	
I_{OL}	Low-level output current			32			32	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS253			SN74AS253			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2		2.4	3.2		V
		V_{CC} = 4.75 V,	I_{OH} = −15 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5		0.25	0.5	V
		V_{CC} = 4.75 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I	A, B	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	A, B	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	A, B	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.6			−0.6		mA
	All others				−0.3			−0.3		
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		17			17		mA
			Outputs low		25			25		
			Outputs disabled		28			28		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS253			SN74AS253			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y		6			6		ns
t_{PHL}				4.5			4.5		
t_{PLH}	Data (Any C)	Y		3.5			3.5		ns
t_{PHL}				3			3		
t_{PZH}	$\overline{G}$	Any Y		5			5		ns
t_{PZL}				6			6		
t_{PHZ}	$\overline{G}$	Any Y		3			3		ns
t_{PLZ}				4			4		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2661, APRIL 1982

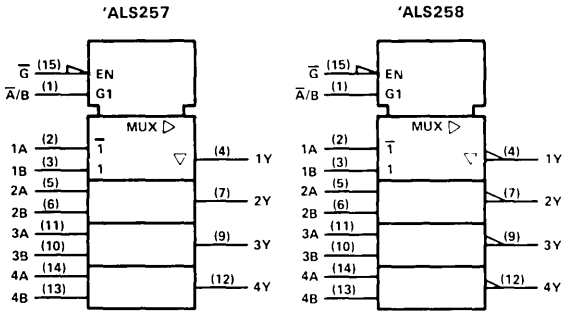
- **Three-State Outputs Interface Directly with System Bus**
- **Provides Bus Interface from Multiple Sources in High-Performance Systems**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices are designed to multiplex signals from four-bit data sources to four-output data lines in bus-organized systems. The 3-state outputs will not load the data lines when the output control pin ($\overline{G}$) is at a high-logic level.

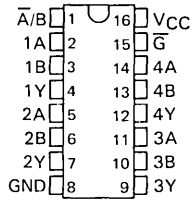
The SN54ALS257 and SN54ALS258 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS257 and SN74ALS258 are characterized for operation from 0 °C to 70 °C.

logic symbols

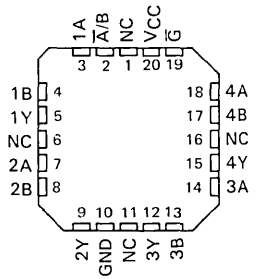


Pin numbers shown are for J and N packages.

SN54ALS257, SN54ALS258 . . . J PACKAGE
SN74ALS257, SN74ALS258 . . . N PACKAGE
(TOP VIEW)



SN54ALS257, SN54ALS258 . . . FH PACKAGE
SN74ALS257, SN74ALS258 . . . FN PACKAGE
(TOP VIEW)

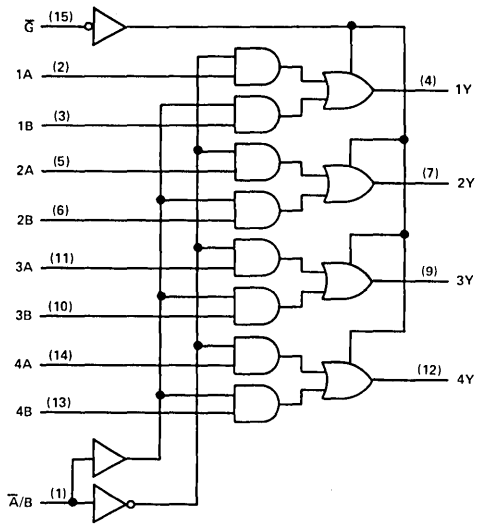


FUNCTION TABLE

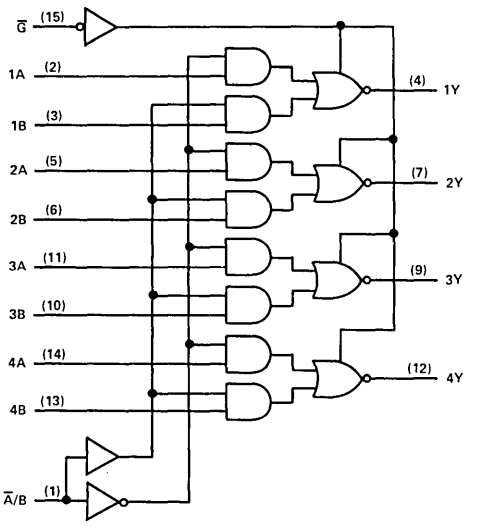
INPUTS				OUTPUT Y	
OUTPUT CONTROL $\overline{G}$	SELECT $\overline{A}$/B	DATA A	DATA B	'ALS257	'ALS258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

logic diagrams (positive logic)

'ALS257



'ALS258



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS257, SN54ALS258 . . . . . −55 °C to 125 °C
SN74ALS257, SN74ALS258 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

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recommended operating conditions

		SN54ALS257 SN54ALS258			SN74ALS257 SN74ALS258			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS257 SN54ALS258			SN74ALS257 SN74ALS258			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
		V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS257	V_{CC} = 5.5 V	Outputs high		2.6			2.6		mA
			Outputs low		8			8		
			Outputs disabled		9.5			9.5		
	'ALS258	V_{CC} = 5.5 V	Outputs high		2.4			2.4		
			Outputs low		7			7		
			Outputs disabled		8			8		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

2

'ALS257 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS257			SN74ALS257			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Any Y		3.5			3.5		ns
t_{PHL}				5			5		
t_{PLH}	$\overline{A}$/B	Any Y		6.5			6.5		ns
t_{PHL}				7			7		
t_{PZH}	G	Any Y		10			10		ns
t_{PZL}				5			5		
t_{PHZ}	G	Any Y		5			5		ns
t_{PLZ}				4			4		

'ALS258 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS258			SN74ALS258			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Any Y		3.5			3.5		ns
t_{PHL}				2.5			2.5		
t_{PLH}	$\overline{A}$/B	Any Y		5.5			5.5		ns
t_{PHL}				8			8		
t_{PZH}	G	Any Y		10			10		ns
t_{PZL}				5			5		
t_{PHZ}	G	Any Y		5			5		ns
t_{PLZ}				4			4		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
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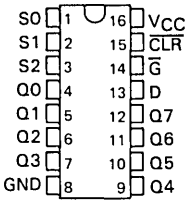
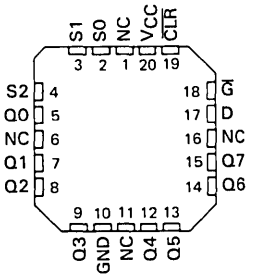
- 8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion with Storage
- Asynchronous Parallel Clear
- Active High Decoder
- Enable/Disable Input Simplifies Expansion
- Expandable for N-Bit Applications
- Four Distinct Functional Modes
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPS
- Dependable Texas Instruments Quality and Reliability

SN54ALS259 . . . J PACKAGE
SN74ALS259 . . . N PACKAGE
(TOP VIEW)



SN54ALS259 . . . FH PACKAGE
SN74ALS259 . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

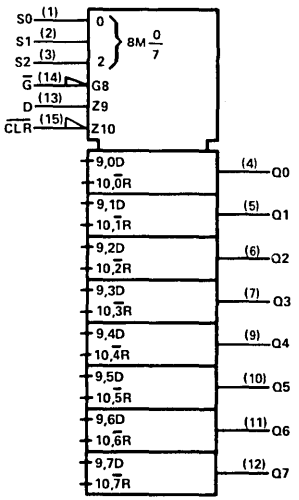
description

These 8-bit addressable latches are designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

Four distinct modes of operation are selectable by controlling the clear ($\overline{CLR}$) and enable ($\overline{G}$) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, enable $\overline{G}$ should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

The SN54ALS259 will be characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS259 will be characterized for operation from 0°C to 70°C.

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE

INPUTS $\overline{CLR}$	INPUTS $\overline{G}$	OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

D = the level at the data input.
Q_{i0} = the level of Q_i (i = 0, 1, ...7, as appropriate) before the indicated steady-state input conditions were established.

LATCH SELECTION TABLE

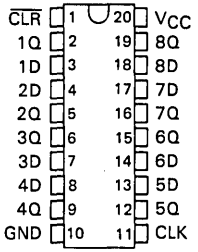
SELECT INPUTS S2	S1	S0	LATCH ADDRESSED
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

PRODUCT PREVIEW

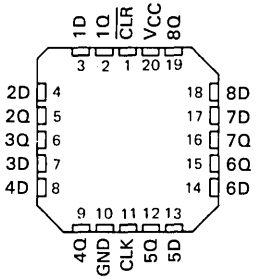
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

- Contains Eight Flip-Flops with Single-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS273 . . . J PACKAGE
SN74ALS273 . . . N PACKAGE
(TOP VIEW)



SN54ALS273 . . . FH PACKAGE
SN74ALS273 . . . FN PACKAGE
(TOP VIEW)



description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input.

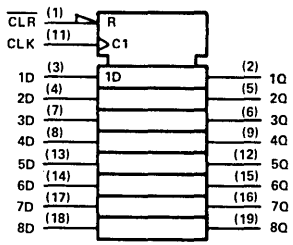
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

The SN54ALS273 is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS273 is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

logic symbol

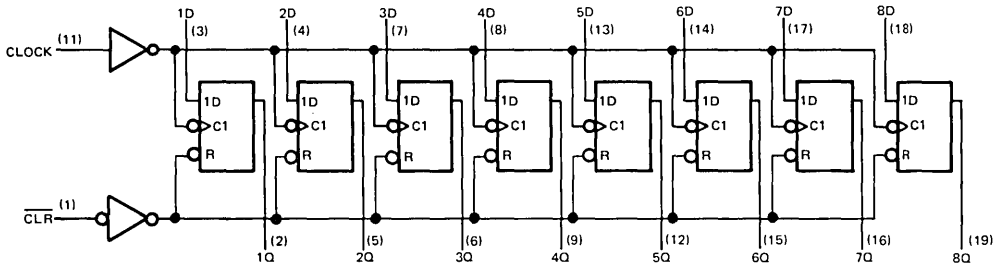


Pin numbers shown are for J and N packages.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS273 . . . . . −55 °C to 125 °C
SN74ALS273 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS273			SN74ALS273			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1				mA
								−2.6	
I_{OL}	Low-level output current				12				mA
								24	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	$\overline{CLR}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↑	Data							ns
		Clear inactive state							
t_h	Hold time, data after CLK↑								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

Additional information on these products can be obtained from the factory as it becomes available.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS273			SN74ALS273			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V			11			11		mA
I_{CCL}	V_{CC} = 5.5 V			19			19		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS273			SN74ALS273			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}				50			50		MHz
t_{PHL}	$\overline{CLR}$	Any Q		14			14		ns
t_{PLH}	CLK	Any Q		9			9		ns
t_{PHL}				9			9		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

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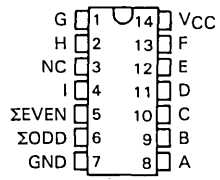
- Generates Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bits
- Can Be Used to Upgrade Existing Systems using MSI Parity Circuits
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

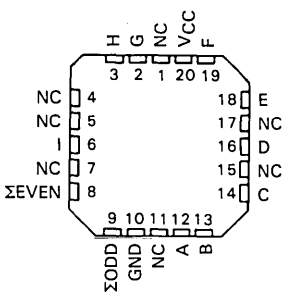
SN54AS280 . . . J PACKAGE
SN74AS280 . . . N PACKAGE
(TOP VIEW)



FUNCTION TABLE

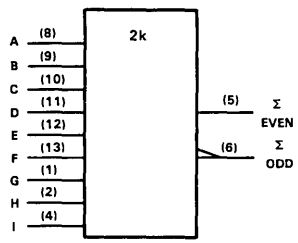
NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0,2,4,6,8	H	L
1,3,5,7,9	L	H

SN54AS280 . . . FH PACKAGE
SN74AS280 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

logic symbol



Pin numbers shown are for J and N packages.

description

These universal, monolithic, nine-bit parity generators/checkers utilize Advanced Schottky high-performance circuitry and feature odd and even outputs to facilitate operation of either odd or even parity application. The word-length capability is easily expanded by cascading.

These devices can be used to upgrade the performance of most systems utilizing the '180 parity generator/checker. Although the 'AS280 is implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4 and the absence of any internal connection at pin 3. This permits the 'AS280 to be substituted for the '180 in existing designs to produce an identical function even if 'AS280's are mixed with existing '180's.

All 'AS280 inputs are buffered to lower the drive requirements.

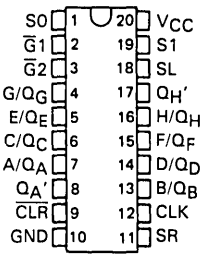
The SN54AS280 is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74AS280 is characterized for operation from 0 °C to 70 °C.

TYPES SN54ALS299, SN54ALS323, SN74ALS299, SN74ALS323
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

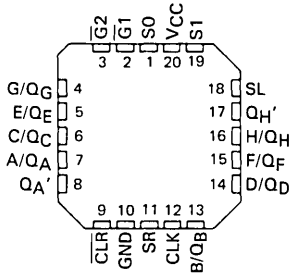
D2661, DECEMBER 1982

- Multiplexed I/O Ports Provide Improved Bit Density
- Four Modes of Operation: Hold (Store), Shift Right, Shift Left, and Load Data
- Operates with Outputs Enabled or at High Impedance
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- 'ALS299 Has Direct Overriding Clear
- 'ALS323 Has Synchronous Clear
- Application:
  Stacked or Push-Down Registers, Buffer Storage, and Accumulator Registers
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPS
- Dependable Texas Instruments Quality and Reliability

SN54ALS299, SN54ALS323 . . . J PACKAGE
SN74ALS299, SN74ALS323 . . . N PACKAGE
(TOP VIEW)



SN54ALS299, SN54ALS323 . . . FH PACKAGE
SN74ALS299, SN74ALS323 . . . FN PACKAGE
(TOP VIEW)



description

These eight-bit universal registers feature multiplexed I/O ports to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines S0 and S1 high. This places the three-state outputs in a high-impedance state and permits data that is applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs asynchronously on 'ALS299 and synchronously on 'ALS323 when $\overline{CLR}$ is low. Taking either of the output controls, $\overline{G}1$ or $\overline{G}2$, high disables the outputs but this has no effect on clearing, shifting, or storage of data.

The SN54ALS299 and SN54ALS323 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS299 and SN74ALS323 are characterized for operation from 0 °C to 70 °C.

1282

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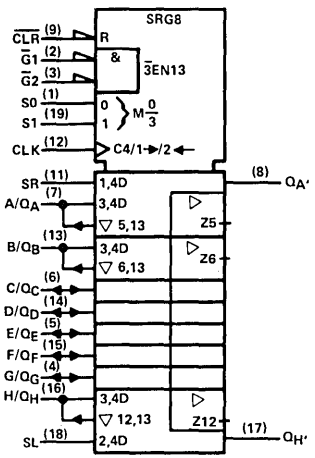
FUNCTION TABLE

MODE	INPUTS								I/O PORTS								OUTPUTS	
	$\overline{CLR}$	S1	S0	OUTPUT CONTROL $\overline{G1}$	OUTPUT CONTROL $\overline{G2}$	CLK	SL	SR	A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	Q_A'	Q_H'
Clear 'ALS299	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Clear 'ALS323	L	X	L	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	↑	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

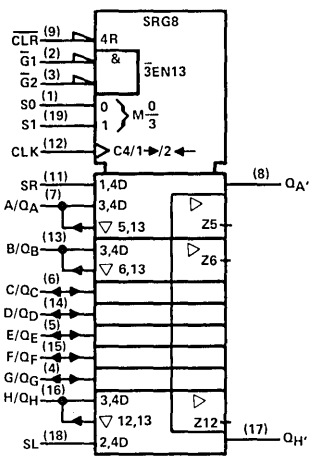
When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

logic symbols

'ALS299



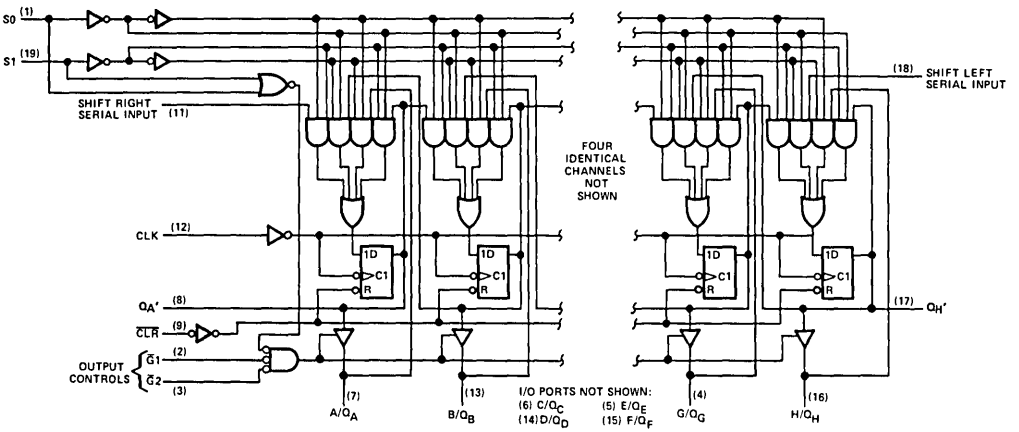
'ALS323



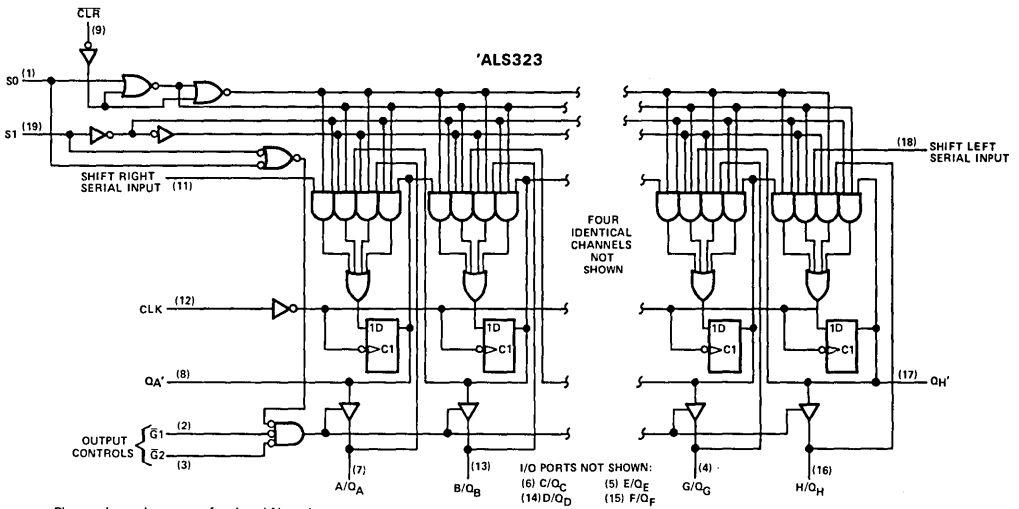
Pin numbers shown are for J and N packages.

logic diagrams (positive logic)

'ALS299



'ALS323



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS299, SN54ALS323 . . . . . −55 °C to 125 °C
SN74ALS299, SN74ALS323 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

TEXAS INSTRUMENTS
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recommended operating conditions

				SN54ALS299 SN54ALS323			SN74ALS299 SN74ALS323			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
I_{OH}	High-level output current	Q_A' or Q_H'				−0.4			−0.4	mA
		Q_A thru Q_H				−1				
									−2.6	
I_{OL}	Low-level output current	Q_A' or Q_H'				4				mA
									8	
		Q_A thru Q_H				12				
									24	
f_{clock}	Clock frequency (at 50% duty cycle)			0		20	0		30	MHz
t_w	Pulse duration	CLK high or low		25			16.5			ns
		$\overline{CLR}$ low ('ALS299)		10			10			
t_{su}	Setup time before CLK↑	Select		25			20			ns
		Serial or Parallel data	High level	18			16			
			Low level	7			6			
		$\overline{CLR}$ inactive ('ALS299)		15			15			
		$\overline{CLR}$ active ('ALS323)		25			20			
		$\overline{CLR}$ inactive ('ALS323)		18			16			
t_h	Hold time after CLK↑	Select		0			0			ns
		Serial or parallel data		0			0			
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS299 SN54ALS323			SN74ALS299 SN74ALS323			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	Q_A' or Q_H'	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
	Q_A thru Q_H	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	Q_A' or Q_H'	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
	Q_A thru Q_H	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	A thru H	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
	Any other	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	
I_{IH}▲		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}▲		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O§	Q_A', Q_H'	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−17	mA
	Q_A thru Q_H			−30		−112	−30		−112	
I_{CC}		V_{CC} = 5.5 V,	Outputs high		15	28		15	28	mA
			Outputs low		22	38		22	38	
			Outputs disabled		23	40		23	40	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
▲For I/O ports (Q_A through Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS299 SN54ALS323		SN74ALS299 SN74ALS323		
			MIN	MAX	MIN	MAX	
f_{max}			20		30		MHz
t_{PLH}	CLK	Q_A thru Q_H	4	15	4	13	ns
t_{PHL}			7	25	7	19	
t_{PLH}	CLK	Q_A' or Q_H'	5	20	5	15	ns
t_{PHL}			8	21	8	18	
t_{PHL}	$\overline{CLR}$ ('ALS299 only)	Q_A thru Q_H	6	29	6	22	ns
		Q_A' or Q_H'	6	29	6	22	
t_{PZH}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H	6	21	6	16	ns
t_{PZL}			8	26	8	22	
t_{PZH}	S0, S1	Q_A thru Q_H	7	21	7	17	ns
t_{PZL}			8	26	8	22	
t_{PHZ}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H	1	10	1	8	ns
t_{PLZ}			5	23	5	15	
t_{PHZ}	S0, S1	Q_A thru Q_H	3	18	3	16	ns
t_{PLZ}			8	30	8	25	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
INCORPORATED
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D2661, APRIL 1982

- Choice of 64 X 4 or 32 X 8 Organization
- 'ALS217 and 'ALS218 Are 3-State Versions of These Memories
- P-N-P Inputs and Buffer Outputs
- Full On-Chip Decoding and Fast Chip-Enable Simplify System Design
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These monolithic TTL memories feature Schottky clamping for high performance and a fast chip-select access time to enhance decoding at the system level.

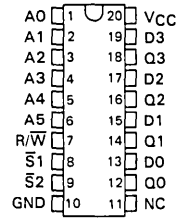
write cycle

Information to be stored in the memory is written into the location selected by the address inputs (A) when the chip-select (S1 and S2) and read-write (R/W) inputs are low. While R/W is low, the memory outputs are off. When a number of outputs are bus-connected, this off state neither loads nor drives the data bus; however, it permits the bus line to be driven by other active outputs or a passive pull-up.

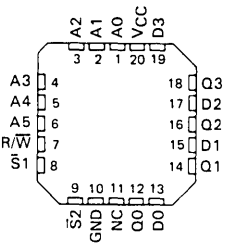
read cycle

Information stored in the memory is available at the outputs when R/W is high and S1 and S2 are low. When either chip-select input is high, the outputs are off.

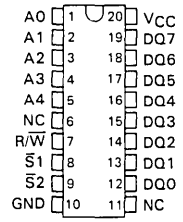
SN54ALS317 . . . J PACKAGE
SN74ALS317 . . . J or N PACKAGE
(TOP VIEW)



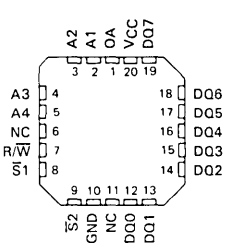
SN54ALS317 . . . FH PACKAGE
SN74ALS317 . . . FN PACKAGE
(TOP VIEW)



SN54ALS318 . . . J PACKAGE
SN74ALS318 . . . J or N PACKAGE
(TOP VIEW)



SN54ALS318 . . . FH PACKAGE
SN74ALS318 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
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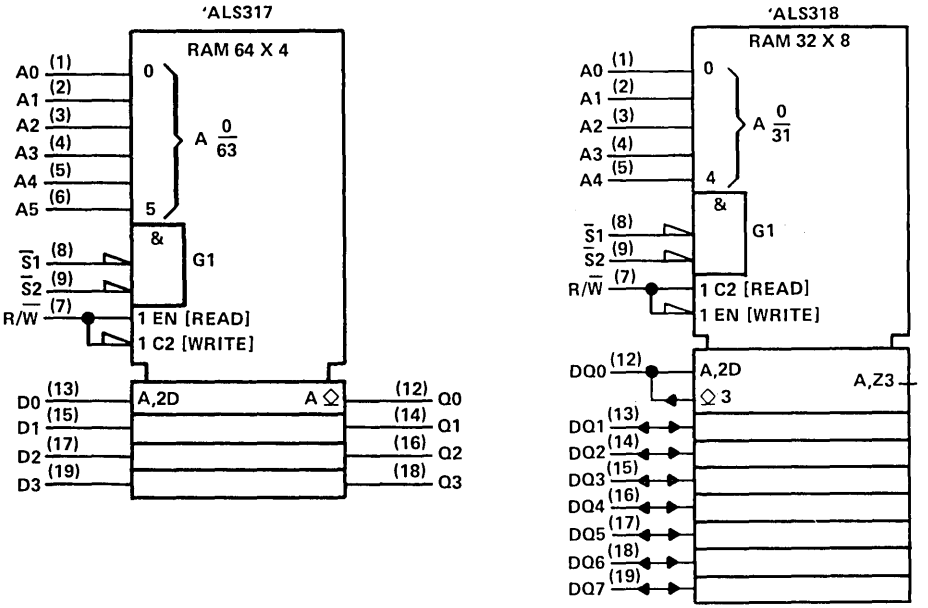
FUNCTION TABLE

FUNCTION	INPUTS			OUTPUTS
	$\overline{S1}$	$\overline{S2}$	R/$\overline{W}$	
Write	L	L	L	H
Read	L	L	H	Data stored
Inhibit	H	X	X	H
	X	H	X	H

2

logic symbols



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports of 'ALS318 . . . . . 5.5 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS317, SN54ALS318 . . . . . −55 °C to 125 °C
SN74ALS317, SN74ALS318 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

TEXAS INSTRUMENTS
INCORPORATED
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recommended operating conditions

			SN54ALS317 SN54ALS318			SN74ALS317 SN74ALS318			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage				5.5			5.5	V
I_{OL}	Low-level output current				12				mA
								24	
$t_{w(W)}$	Duration of write pulse		50			50			ns
t_{su}	Setup time	Address before R/$\overline{W}$↓	0			0			ns
		Data before R/$\overline{W}$↑	50			50			
		$\overline{S}$ low before R/$\overline{W}$↑	0			0			
t_h	Hold time after R/$\overline{W}$↑	Address	0			0			ns
		Data	0			0			
		$\overline{S}$ low	0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS317 SN54ALS318			SN74ALS317 SN74ALS318			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	All inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	'ALS318 DQ ports	V_{CC} = 5.5 V	V_I = 5.5 V			0.1			0.1	
I_{IH}	All inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	'ALS318 DQ ports▲					20			20	
I_{IL}	All inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	'ALS318 DQ ports▲					−0.2			−0.2	
I_{CC}		V_{CC} = 5.5 V			46			46		mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
▲For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS317 SN54ALS318			SN74ALS317 SN74ALS318			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(A)}$	A	Q or DQ		30			30		ns
$t_{a(S)}$	$\overline{S}$	Q or DQ		20			20		ns
t_{sr}	R/$\overline{W}$	Q or DQ		30			30		ns
$t_{dis(S)}$	$\overline{S}$	Q or DQ		14			14		ns
$t_{dis(R)}$	R/$\overline{W}$	Q or DQ		18			18		ns

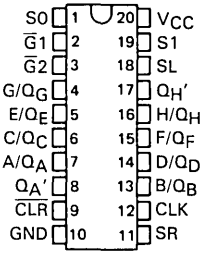
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TYPES SN54ALS299, SN54ALS323, SN74ALS299, SN74ALS323
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

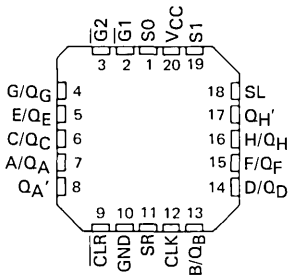
D2661, DECEMBER 1982

- Multiplexed I/O Ports Provide Improved Bit Density
- Four Modes of Operation: Hold (Store), Shift Right, Shift Left, and Load Data
- Operates with Outputs Enabled or at High Impedance
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- 'ALS299 Has Direct Overriding Clear
- 'ALS323 Has Synchronous Clear
- Application:
  Stacked or Push-Down Registers, Buffer Storage, and Accumulator Registers
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPS
- Dependable Texas Instruments Quality and Reliability

SN54ALS299, SN54ALS323 . . . J PACKAGE
SN74ALS299, SN74ALS323 . . . N PACKAGE
(TOP VIEW)



SN54ALS299, SN54ALS323 . . . FH PACKAGE
SN74ALS299, SN74ALS323 . . . FN PACKAGE
(TOP VIEW)



For complete information on the SN54ALS323 and the SN74ALS323, see page 2-196.

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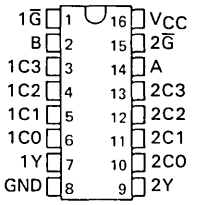
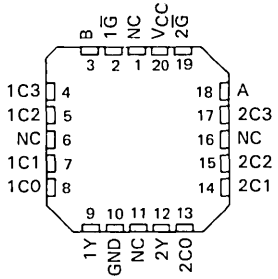
D2661, APRIL 1982

- Inverting Versions of 'ALS153 and 'AS153
- Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N Lines to n Lines)
- Typical 'ALS352 Power per Multiplexer . . . 16 mW
- Typical 'AS352 Average Propagation Delay Times
  Data Input to Output . . . 2.7 ns
  Strobe Input to Output . . . 4.5 ns
  Select Input to Output . . . 4.5 ns
- Fully Compatible with Most TTL Circuits
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS352, SN54AS352 . . . J PACKAGE
SN74ALS352, SN74AS352 . . . N PACKAGE
(TOP VIEW)



SN54ALS352, SN54AS352 . . . FH PACKAGE
SN74ALS352, SN74AS352 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs ($\overline{G}$) are provided for each of the two four-line sections.

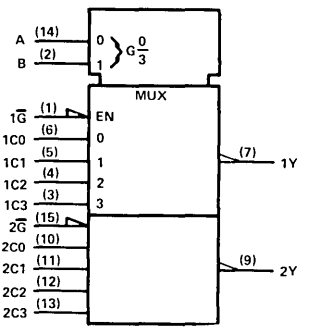
The SN54ALS352 and SN54AS352 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS352 and SN74AS352 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	H
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections.

logic symbol



Pin numbers shown are for J and N packages.

TEXAS INSTRUMENTS
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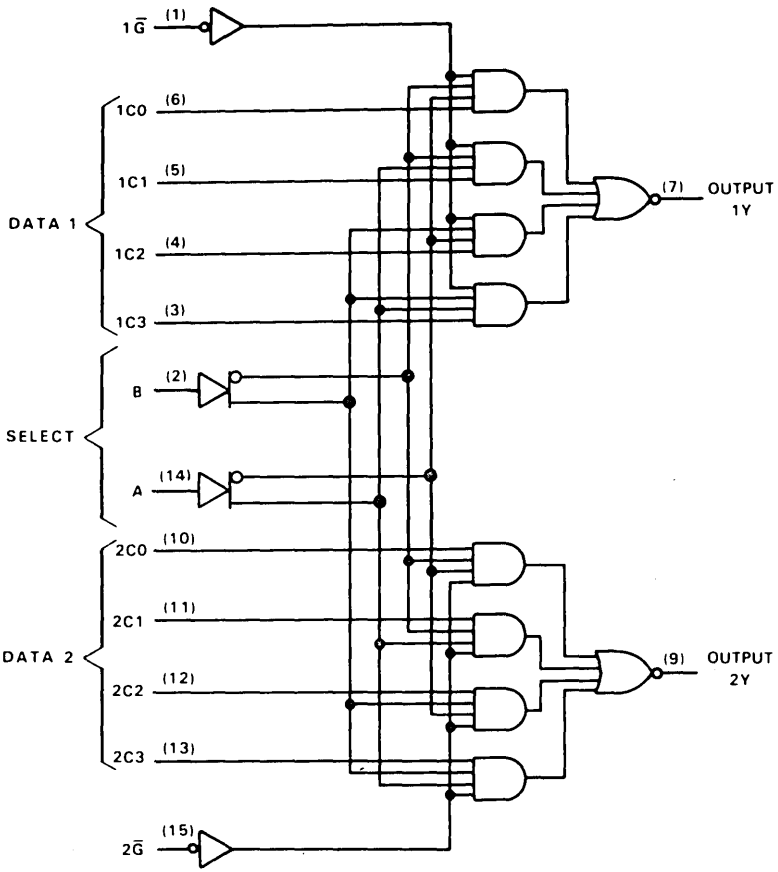
logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS352, SN54AS352 . . . . . −55 °C to 125 °C
SN74ALS352, SN74AS352 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS352			SN74ALS352			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS352			SN74ALS352			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
		V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	A or B	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	A or B	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	A or B	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	All others					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		6.5			6.5		mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with data and select inputs at 4.5 V, and $\overline{G}$ inputs grounded.

switching characteristics (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS352			SN74ALS352			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y		9			9		ns
t_{PHL}				9.5			9.5		
t_{PLH}	Data (Any C)	Y		6			6		ns
t_{PHL}				6			6		
t_{PLH}	$\overline{G}$	Y		4			4		ns
t_{PHL}				5			5		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: For load circuit and voltage waveforms, see page 1-12.

recommended operating conditions

		SN54AS352			SN74AS352			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−12	mA
							−15†	
I_{OL}	Low-level output current			32			32	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS352			SN74AS352			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2		2.4	3.2		V
	V_{CC} = 4.75 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5		0.25	0.5	V
	V_{CC} = 4.75 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.3			−0.3		mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		21			21		mA
		Outputs low		28			28		

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

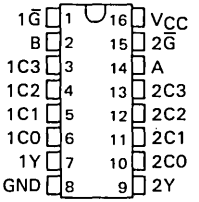
switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX					UNIT
			'AS352	SN54AS352			SN74AS352		
			TYP‡	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y			4.5			4.5		ns
t_{PHL}					4.5			4.5		
t_{PLH}	Data (Any C)	Y			3			3		ns
t_{PHL}					2.5			2.5		
t_{PLH}	$\overline{G}$	Y			4.5			4.5		ns
t_{PHL}					4.5			4.5		

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- **Inverting Versions of 'ALS253 and 'AS253**
- **Permits Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **Typical 'ALS353 Power per Multiplexer . . . 20 mW**
- **Fully Compatible with Most TTL Circuits**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS353, SN54AS353 . . . J PACKAGE
SN74ALS353, SN74AS353 . . . N PACKAGE
(TOP VIEW)



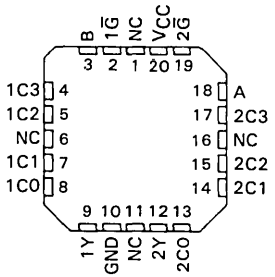
description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs ($\overline{G}$) are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe ($\overline{G}$). The output is disabled when its strobe is high.

The SN54ALS353 and SN54AS353 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS353 and SN74AS353 are characterized for operation from 0 °C to 70 °C.

SN54ALS353, SN54AS353 . . . FH PACKAGE
SN74ALS353, SN74AS353 . . . FN PACKAGE
(TOP VIEW)



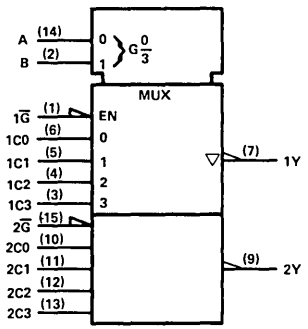
NC—No internal connection

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections.

logic symbol



Pin numbers shown are for J and N packages

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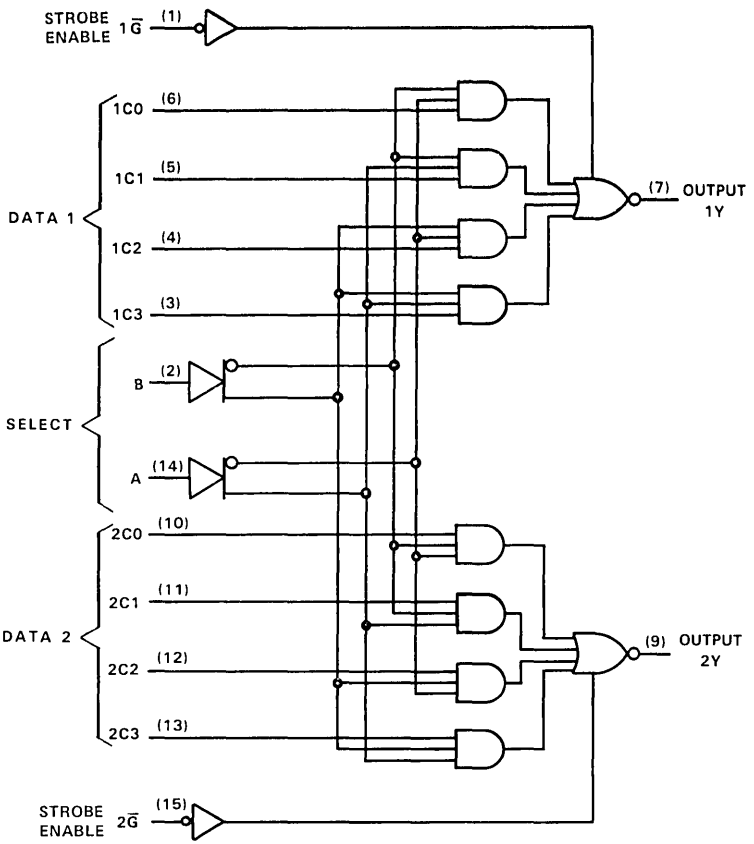
logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS353, SN54AS353 . . . . . −55 °C to 125 °C
SN74ALS353, SN74AS353 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS353			SN74ALS353			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS353			SN74ALS353			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
		V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	A, B	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	A, B	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	A, B	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	All others					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	All inputs at 4.5 V		8			8		mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS353			SN74ALS353			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y		9			9		ns
t_{PHL}				9.5			9.5		
t_{PLH}	Data (Any C)	Y		6			6		ns
t_{PHL}				6			6		
t_{PZH}	$\overline{G}$	Y		4			4		ns
t_{PZL}				5			5		
t_{PHZ}	$\overline{G}$	Y		4			4		ns
t_{PLZ}				5			5		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

recommended operating conditions

		SN54AS353			SN74AS353			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−12	mA
							−15†	
I_{OL}	Low-level output current			32			32	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS353			SN74AS353			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2		2.4	3.2		V
		V_{CC} = 4.75 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5		0.25	0.5	V
		V_{CC} = 4.75 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I	A, B	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	A, B	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	A, B	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.6			−0.6		mA
	All others				−0.3			−0.3		
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	Outputs high		21			21		mA
			Outputs low		28			28		
			Outputs disabled		29			29		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			'AS353	SN54AS353			SN74AS353			
			TYP‡	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y			4.5			4.5		ns
t_{PHL}					4.5			4.5		
t_{PLH}	Data (Any C)	Y			3			3		ns
t_{PHL}					2.5			2.5		
t_{PZH}	Strobe	Y			5			5		ns
t_{PZL}					6			6		
t_{PHZ}	Strobe	Y			3			3		ns
t_{PLZ}					4			4		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- 3-State Outputs Drive Bus Lines Or Buffer Memory Address Registers
- Choice of True or Inverting Outputs
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

'ALS365, 'ALS367	True Outputs
'ALS366, 'ALS368	Inverting Outputs

2

description

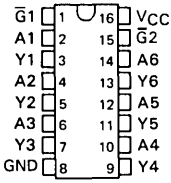
These Hex buffers and line drivers are designed specifically to improve both the performance and density of three state memory address drivers, clock drivers, and bus oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low control) inputs.

These devices feature high fan-out, and improved fan-in. The SN74ALS365 through SN74ALS368 can be used to drive terminated lines down to 133 ohms.

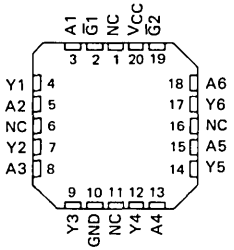
The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS' parts.

The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

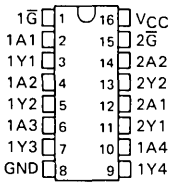
SN54ALS365, SN54ALS366 . . . J PACKAGE
SN74ALS365, SN74ALS366 . . . N PACKAGE
(TOP VIEW)



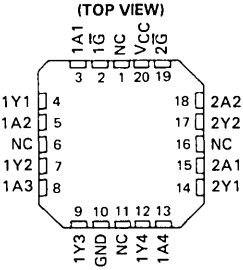
SN54ALS365, SN54ALS366 . . . FH PACKAGE
SN74ALS365, SN74ALS366 . . . FN PACKAGE
(TOP VIEW)



SN54ALS367, SN54ALS368 . . . J PACKAGE
SN74ALS367, SN74ALS368 . . . N PACKAGE
(TOP VIEW)



SN54ALS367, SN54ALS368 . . . FH PACKAGE
SN74ALS367, SN74ALS368 . . . FN PACKAGE
(TOP VIEW)



ADVANCE INFORMATION
This document contains information on a new product. Specifications are subject to change without notice.

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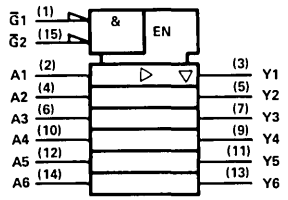
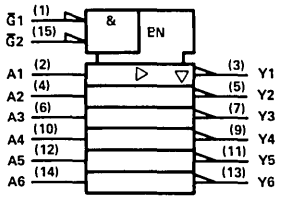
logic symbols

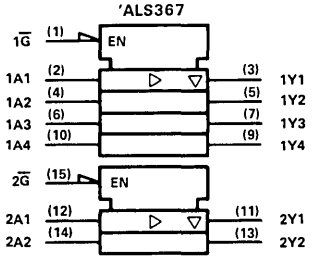
'ALS365



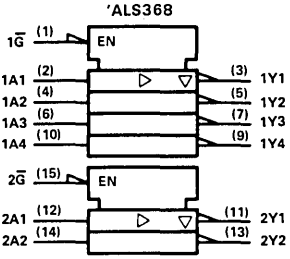
'ALS366



'ALS367

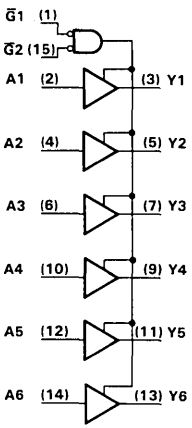


'ALS368

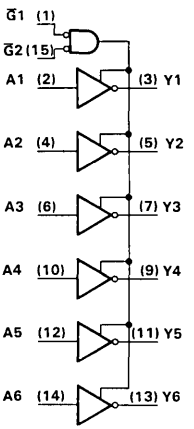


logic diagrams (positive logic)

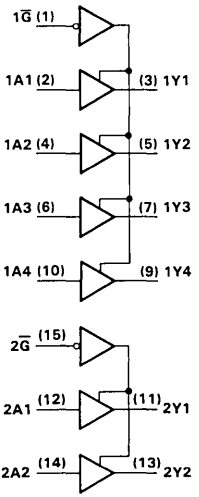
'ALS365



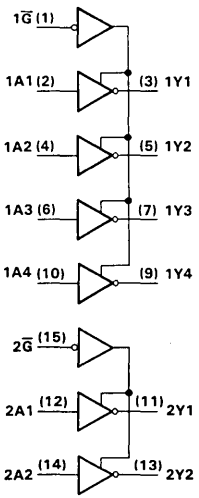
'ALS366



'ALS367



'ALS368



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS365 thru SN54ALS368 . . . . . −55°C to 125°C
SN74ALS365 thru SN74ALS368 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS365 THRU SN54ALS368			SN74ALS365 THRU SN74ALS368			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12				mA
							−15	
I_{OL}	Low-level output current			12				mA
							24	
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS365-1 thru SN74ALS368-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS365 THRU SN54ALS368			SN74ALS365 THRU SN74ALS368			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for -1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS365 'ALS367	V_{CC} = 5.5 V	Outputs high		7			7		mA
			Outputs low		12			12		
			Outputs disabled		13			13		
	'ALS366 'ALS368		Outputs high		3			3		
			Outputs low		10			10		
			Outputs disabled		11			11		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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'ALS365, 'ALS367 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS365 SN54ALS367			SN74ALS365 SN74ALS367			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y		7			7		ns
t_{PHL}				7			7		
t_{PZH}	$\overline{G}$	Y		14			14		ns
t_{PZL}				14			14		
t_{PHZ}	$\overline{G}$	Y		5			5		ns
t_{PLZ}				8			8		

'ALS366, 'ALS368 switching characteristics (see note 1)

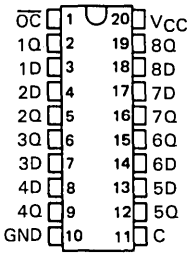
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS366 SN54ALS368			SN74ALS366 SN74ALS368			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y		6			6		ns
t_{PHL}				5			5		
t_{PZH}	$\overline{G}$	Y		10			10		ns
t_{PZL}				17			17		
t_{PHZ}	$\overline{G}$	Y		6			6		ns
t_{PLZ}				6			6		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

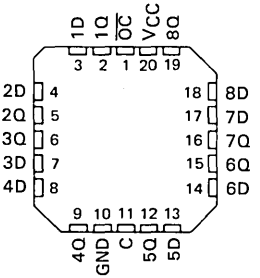
D2661, APRIL 1982

- 8 Latches in a Single Package
- 3-State Bus-Driving True Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- P-N-P Inputs Reduce D-C Loading on Data Lines
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS373, SN54AS373 . . . J PACKAGE
SN74ALS373, SN74AS373 . . . N PACKAGE
(TOP VIEW)



SN54ALS373, SN54AS373 . . . FH PACKAGE
SN74ALS373, SN74AS373 . . . FN PACKAGE
(TOP VIEW)



description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'ALS373 and 'AS373 are transparent D-type latches. While the enable (C) is high the Q outputs will follow the data (D) inputs. When the enable is taken low, the Q outputs will be latched at the levels that were set up at the D inputs.

A buffered output-control input ($\overline{OC}$) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control $\overline{OC}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54ALS373 and SN54AS373 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS373 and SN74AS373 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (EACH LATCH)

INPUTS			OUTPUT
$\overline{OC}$	ENABLE C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

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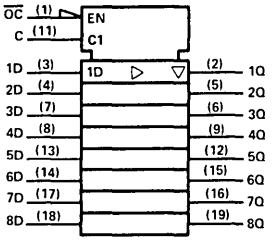
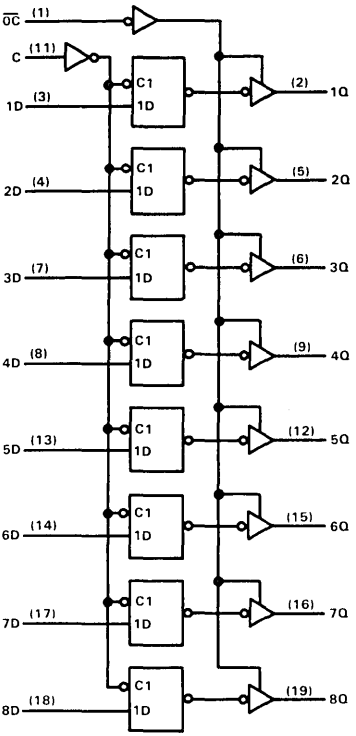
logic symbol



logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS373, SN54AS373 . . . . . −55 °C to 125 °C
SN74ALS373, SN74AS373 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS373			SN74ALS373			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							24	
t_w	Pulse duration, enable C high	10			10			ns
t_{su}	Setup time, data before enable C↓	10			10			ns
t_h	Hold time, data after enable C↓	7			7			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS373			SN74ALS373			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		9			9		mA
		Outputs low		16			16		
		Outputs disabled		17			17		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

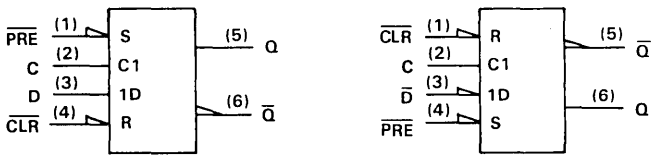
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS373			SN74ALS373			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	D	Q		8			8		ns
t_{PHL}				8			8		
t_{PLH}	C	Any Q		13			13		ns
t_{PHL}				13			13		
t_{PZH}	$\overline{OC}$	Any Q		10			10		ns
t_{PZL}				12			12		
t_{PHZ}	$\overline{OC}$	Any Q		7			7		ns
t_{PLZ}				9			9		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D latch signal conventions

It is TI practice to name the outputs and other inputs of a D-type latch and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.



Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (⊵) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input D, but now both are considered active-low.

recommended operating conditions

		SN54AS373			SN74AS373			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−12	mA
							−15†	
I_{OL}	Low-level output current			32			32	mA
							48†	
t_w	Pulse duration, enable C high							ns
t_{su}	Setup time, data before enable C↓							ns
t_h	Hold time, data after enable C↓							ns
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS373			SN74AS373			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2		2.4	3.2		V
	V_{CC} = 4.75 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5		0.25	0.5	V
	V_{CC} = 4.75 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.2			−0.2		mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		65			65		mA
		Outputs low							
		Outputs disabled		65			65		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25 °C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX					UNIT
			'AS373	SN54AS373			SN74AS373		
			TYP	MIN	TYP‡	MAX	MIN	TYP‡ MAX	
t_{PLH}	D	Q			4.5			4.5	ns
t_{PHL}					4			4	
t_{PLH}	C	Any Q			7			7	ns
t_{PHL}					5			5	
t_{PZH}	$\overline{OC}$	Any Q			3.5			3.5	ns
t_{PZL}					5			5	
t_{PHZ}	$\overline{OC}$	Any Q			3.5			3.5	ns
t_{PLZ}					5.5			5.5	

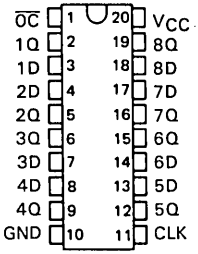
‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

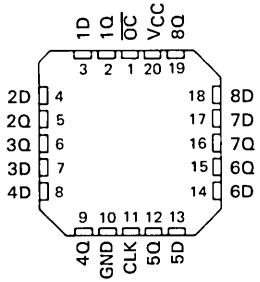
- 8 D-Type Flip-Flops In a Single Package
- 3-State Bus-Driving True Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- P-N-P Inputs Reduce D-C Loading on Data Lines
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

2

SN54ALS374, SN54AS374 . . . J PACKAGE
SN74ALS374, SN74AS374 . . . N PACKAGE
(TOP VIEW)



SN54ALS374, SN54AS374 . . . FH PACKAGE
SN74ALS374, SN74AS374 . . . FN PACKAGE
(TOP VIEW)



description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'ALS374 and 'AS374 are edge-triggered D-type flip-flops. On the positive transition of the clock the Q outputs will be set to the logic levels that were set up at the D inputs.

A buffered output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control ($\overline{OC}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS374 and SN54AS374 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS374 and SN74AS374 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

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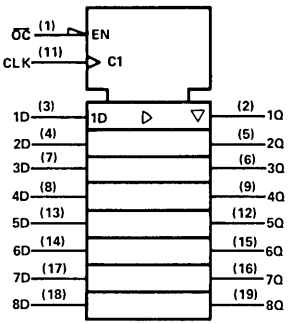
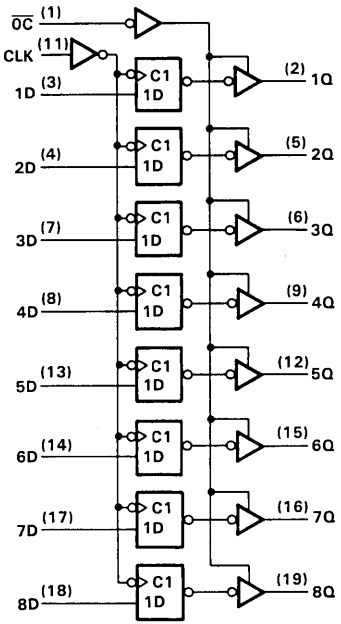
logic symbol



logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS374, SN54AS374 . . . . . −55 °C to 125 °C
SN74ALS374, SN74AS374 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS374			SN74ALS374			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1				mA
								−2.6	
I_{OL}	Low-level output current				12				mA
								24	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	CLK high							ns
		CLK low							
t_{su}	Setup time, data before CLK↑		10			10			ns
t_h	Hold time, data after CLK↑		4			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS374			SN74ALS374			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		11			11		mA
		Outputs low		19			19		
		Outputs disabled		20			20		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

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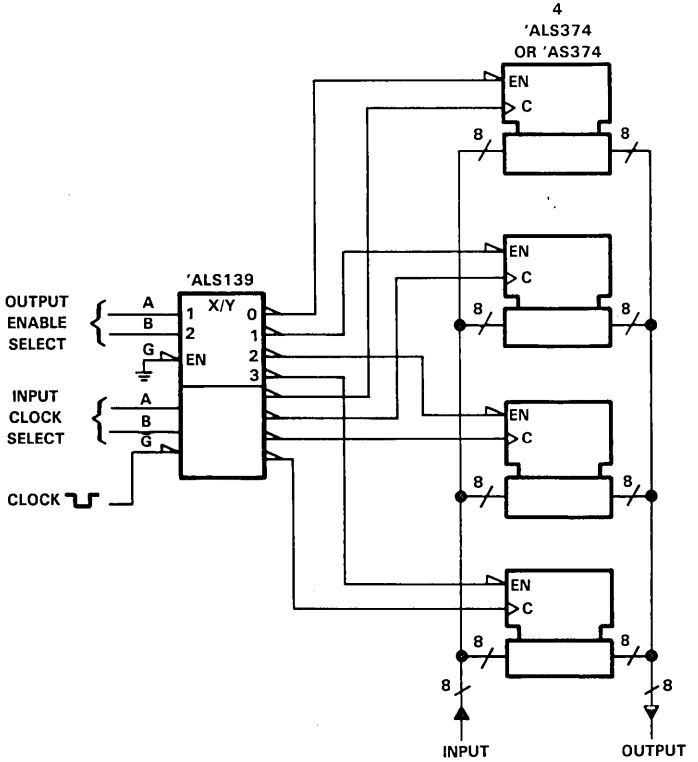
switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS374			SN74ALS374			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}				50			50		MHz
t_{PLH}	CLK	Q		8			8		ns
t_{PHL}				8			8		
t_{PZH}	$\overline{OC}$	Q		10			10		ns
t_{PZL}				12			12		
t_{PHZ}	$\overline{OC}$	Q		7			7		ns
t_{PLZ}				9			9		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TYPICAL APPLICATION DATA

EXPANDABLE 4-WORD BY 8-BIT GENERAL REGISTER FILE



recommended operating conditions

			SN54AS374			SN74AS374			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−12	mA
								−15†	
I_{OL}	Low-level output current				32			32	mA
								48†	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	CLK high							ns
		CLK low							
t_{su}	Setup time, data before CLK↑								ns
t_h	Hold time, data after CLK↑								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS374			SN74AS374			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2		2.4	3.2		V
		V_{CC} = 4.75 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5		0.25	0.5	V
		V_{CC} = 4.75 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	$\overline{OC}$, CLK	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.1			−0.1		mA
	Data				−1.3			−1.3		
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high							mA
			Outputs low		84			84		
			Outputs disabled		88			88		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

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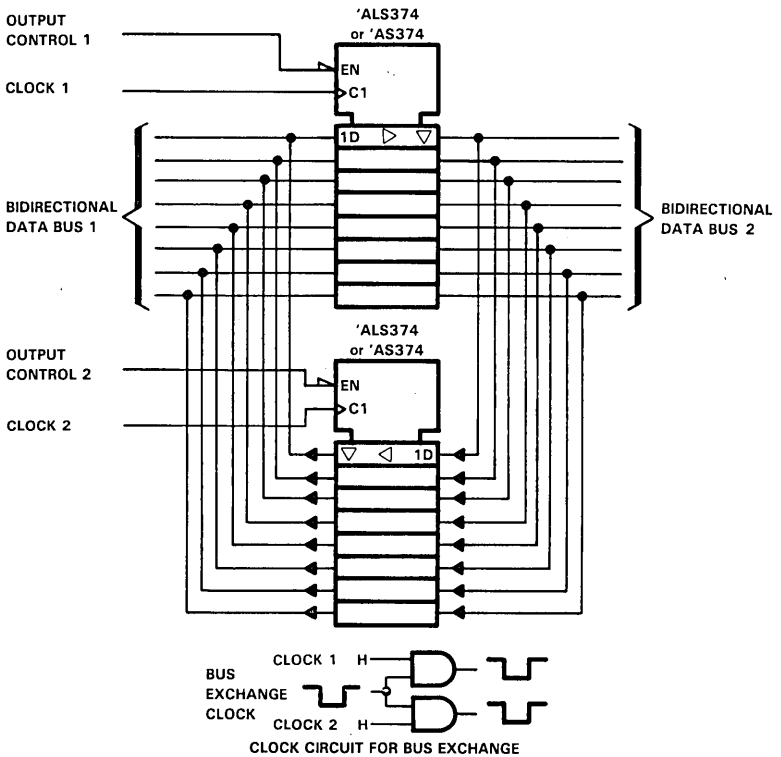
switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			'AS374			SN54AS374			SN74AS374			
			MIN	TYP	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}							165			165		MHz
t_{PLH}	CLK	Q					5.5			5.5		ns
t_{PHL}							6			6		
t_{PZH}	$\overline{OC}$	Q					3.5			3.5		ns
t_{PZL}							5			5		
t_{PHZ}	$\overline{OC}$	Q					3.5			3.5		ns
t_{PLZ}							5.5			5.5		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TYPICAL APPLICATION DATA

BIDIRECTIONAL BUS DRIVER



CLOCK CIRCUIT FOR BUS EXCHANGE

D2661, APRIL 1982

- **Mechanically and Functionally Interchangeable with DM71/81LS97 and DM71/81LS98**
- **P-N-P Inputs Reduce Bus Loading**
- **3-State Outputs Rated at I_{OL} of 12 mA and 24 mA for SN54ALS' and SN74ALS', Respectively**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

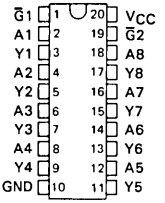
DEVICE	DATA PATH
'ALS465	True
'ALS466	Inverting
'ALS467	True
'ALS468	Inverting

description

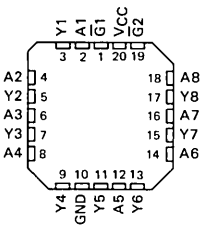
These octal buffers utilize the latest advanced low-power Schottky technology. The 'ALS465 and 'ALS466 have a two-input active-low AND enable gate controlling all eight data buffers. The 'ALS467 and 'ALS468 have two separate active-low enable inputs each controlling four data buffers. In each case, a high level on any $\overline{G}$ places the affected outputs at high impedance.

The SN54ALS465, SN54ALS466, SN54ALS467, and SN54ALS468 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS465, SN74ALS466, SN74ALS467, and SN74ALS468 are characterized for operation from 0°C to 70°C.

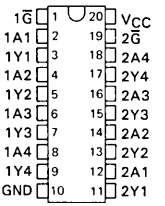
SN54ALS465, SN54ALS466 . . . J PACKAGE
SN74ALS465, SN74ALS466 . . . N PACKAGE
(TOP VIEW)



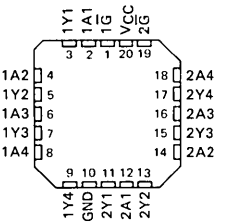
SN54ALS465, SN54ALS466 . . . FH PACKAGE
SN74ALS465, SN74ALS466 . . . FN PACKAGE
(TOP VIEW)



SN54ALS467, SN54ALS468 . . . J PACKAGE
SN74ALS467, SN74ALS468 . . . N PACKAGE
(TOP VIEW)



SN54ALS467, SN54ALS468 . . . FH PACKAGE
SN74ALS467, SN74ALS468 . . . FN PACKAGE
(TOP VIEW)



TEXAS INSTRUMENTS
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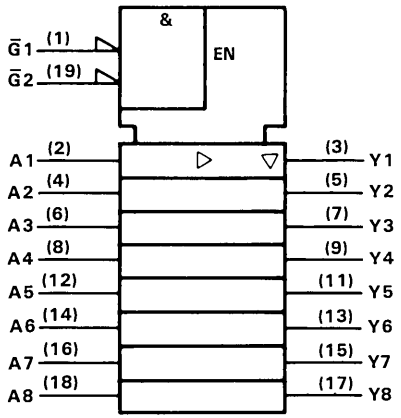
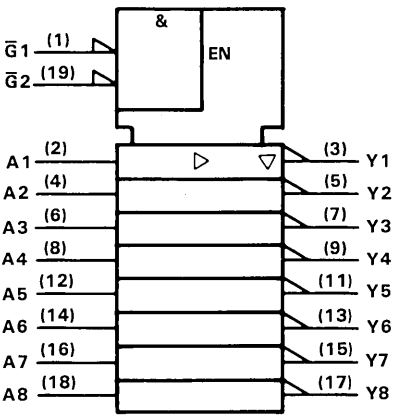
logic symbols

'ALS465

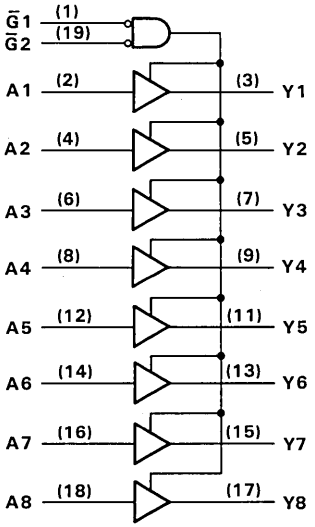


'ALS466

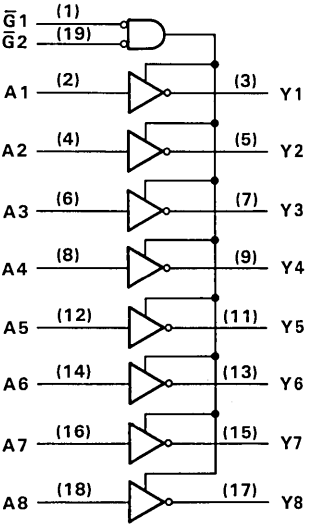


logic diagrams (positive logic)

'ALS465



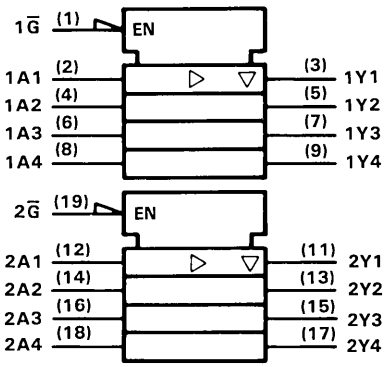
'ALS466



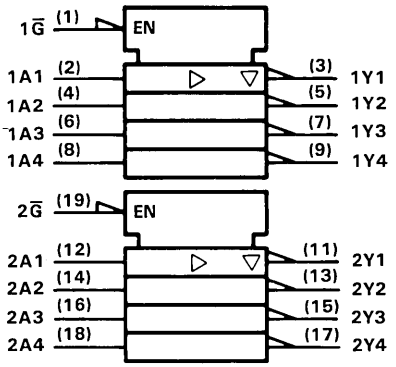
Pin numbers shown are for J and N packages.

logic symbols

'ALS467

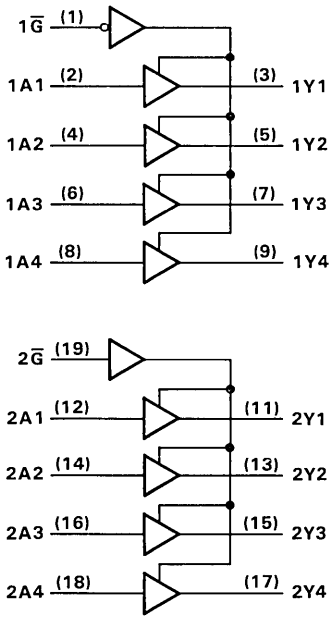


'ALS468

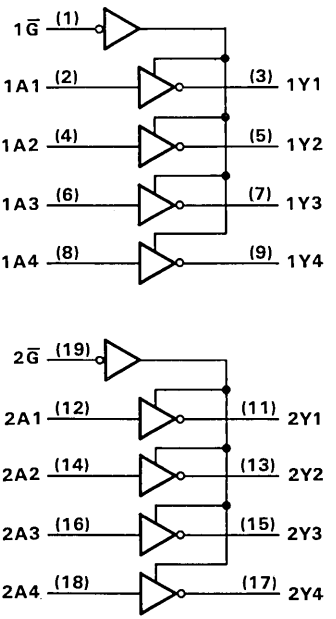


logic diagrams (positive logic)

'ALS467



'ALS468



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS465 THRU SN54ALS468 . . . . . −55 °C to 125 °C
SN74ALS465 THRU SN74ALS468 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS465 THRU SN54ALS468			SN74ALS465 THRU SN74ALS468			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12				mA
							−15	
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS465 THRU SN54ALS468			SN74ALS465 THRU SN74ALS468			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS465 'ALS467	V_{CC} = 5.5 V	Outputs high							mA
			Outputs low							
			Outputs disabled							
	'ALS466 'ALS468	V_{CC} = 5.5 V	Outputs high		6	11		6	10	mA
			Outputs low		13	25		13	22	
			Outputs disabled		17	28		17	25	

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
Additional information on these products can be obtained from the factory as it becomes available.

'ALS465, 'ALS467 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS465 SN54ALS467			SN74ALS465 SN74ALS467			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y							ns
t_{PHL}									
t_{PZH}	$\overline{G}$	Any Y							ns
t_{PZL}									
t_{PHZ}	$\overline{G}$	Any Y							ns
t_{PLZ}									

'ALS466, 'ALS468 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS466 SN54ALS468		SN74ALS466 SN74ALS468		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	15	3	13	ns
t_{PHL}			2	11	2	9	
t_{PZH}	$\overline{G}$	Any Y	4	21	4	16	ns
t_{PZL}			7	25	7	23	
t_{PHZ}	$\overline{G}$	Any Y	2	12	2	10	ns
t_{PLZ}			5	25	5	22	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

TEXAS INSTRUMENTS
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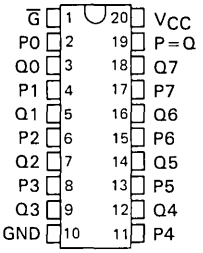
- Compares Two 8-Bit Words
- Choice of Totem-Pole or Open-Collector Outputs
- 'ALS518, 'ALS520, and 'ALS522 Have 20-kΩ Pull-up Resistors on Q Inputs
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

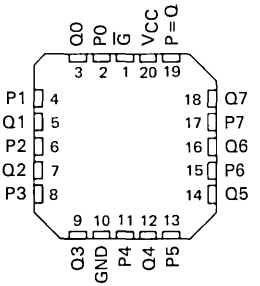
TYPE	INPUT PULL-UP RESISTOR	OUTPUT FUNCTION AND CONFIGURATION
'ALS518	Yes	P = Q open-collector
'ALS519	No	P = Q open-collector
'ALS520	Yes	$\overline{P=Q}$ totem-pole
'ALS521†	No	$\overline{P=Q}$ totem-pole
'ALS522	Yes	$\overline{P=Q}$ open-collector

†'ALS521 is identical to 'ALS688

SN54ALS' . . . J PACKAGE
SN74ALS' . . . N PACKAGE
(TOP VIEW)



SN54ALS' . . . FH PACKAGE
SN74ALS' . . . FN PACKAGE
(TOP VIEW)



*P = Q for 'ALS518 and 'ALS519, and $\overline{P=Q}$ for 'ALS520, 'ALS521, and 'ALS522.

NC — no internal connection.

description

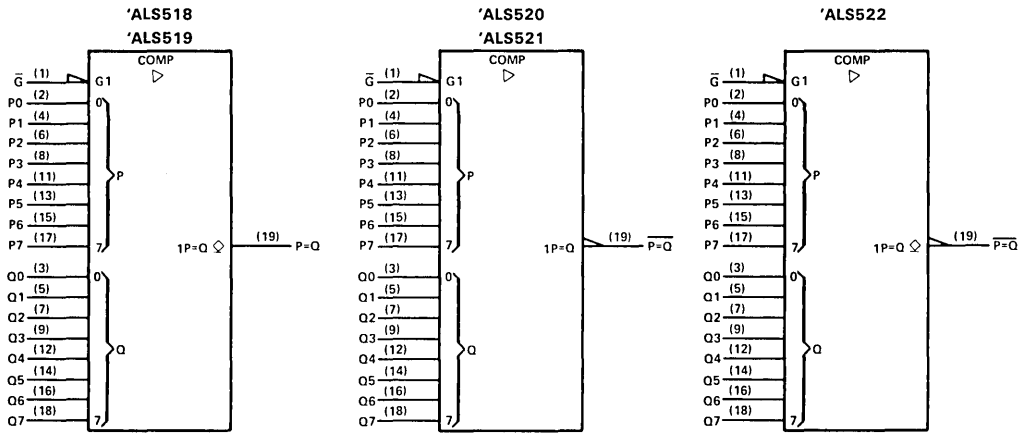
These identity comparators perfrom comparisons on two eight-bit binary or BCD words. The 'ALS518 and 'ALS519 provide P = Q outputs, while the 'ALS520, 'ALS521, and 'ALS522 provide $\overline{P=Q}$ outputs. The 'ALS518, 'ALS519, and 'ALS522 have open-collector outputs. The 'ALS518, 'ALS520, and 'ALS522 feature 20-kΩ pull-up termination resistors on the Q inputs for analog or switch data.

The SN54ALS518 through SN54ALS522 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS518 through SN74ALS522 are characterized for operation from 0 °C to 70 °C.

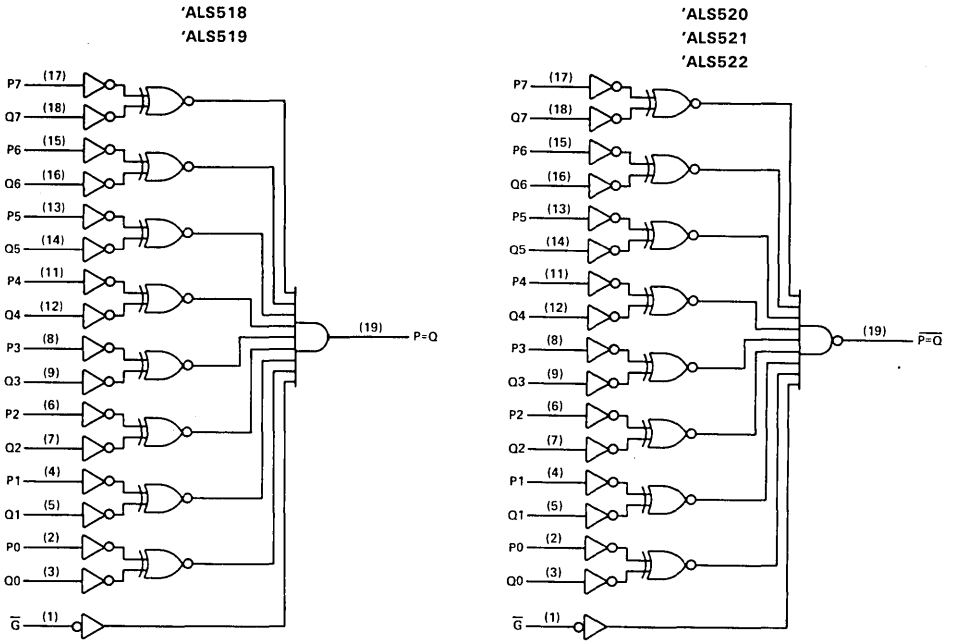
FUNCTION TABLE

INPUTS		OUTPUTS	
DATA P, Q	ENABLE $\overline{G}$	P = Q	$\overline{P=Q}$
P = Q	L	H	L
P > Q	L	L	H
P < Q	L	L	H
X	H	L	H

logic symbols



logic diagrams (positive logic)



Pin numbers shown are for J and N packages.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Q inputs of 'ALS518, 'ALS522 . . . . . V_{CC} + 0.5 V or 5.5 V, whichever is less
All other inputs . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS518, SN54ALS519, SN54ALS522 . . . . . −55 °C to 125 °C
SN74ALS518, SN74ALS519, SN74ALS522 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS518 SN54ALS519 SN54ALS522			SN74ALS518 SN74ALS519 SN74ALS522			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output current			5.5			5.5	V
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS518 SN54ALS519 SN54ALS522			SN74ALS518 SN74ALS519 SN74ALS522			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = −5.5 mA			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	'ALS518, 'ALS522 Q inputs	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
	All other inputs	V_{CC} = 5.5 V	V_I = 7 V			0.1			0.1	
I_{IH}	'ALS518, 'ALS522 Q inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			−0.2			−0.2	mA
	All other inputs					20			20	μA
I_{IL}	'ALS518, 'ALS522 Q inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.6			−0.6	mA
	All other inputs					−0.1			−0.1	
I_{CC}	'ALS518	V_{CC} = 5.5 V			11	17		11	17	mA
	'ALS519				11	17		11	17	
	'ALS522				9	15		9	15	

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.

Additional information on these products can be obtained from the factory as it becomes available.

ADVANCE INFORMATION

This page contains information on a new product. Specifications are subject to change without notice.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Q inputs of 'ALS520 . . . . . V_{CC} + 0.5 V or 5.5 V, whichever is less
All other inputs . . . . . 7 V
Operating free-air temperature range: SN54ALS520, SN54ALS521 . . . . . −55 °C to 125 °C
SN74ALS520, SN74ALS521 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

2

recommended operating conditions

		SN54ALS520 SN54ALS521			SN74ALS520 SN74ALS521			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS520 SN54ALS521			SN74ALS520 SN74ALS521			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −1 mA	24	3.3					V
		V_{CC} = 4.5 V	I_{OH} = 2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	'ALS520 Q inputs	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
	All other inputs	V_{CC} = 5.5 V	V_I = 7 V			0.1			0.1	
I_{IH}	'ALS520 Q inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			−0.2			−0.2	mA
	All other inputs					20			20	μA
I_{IL}	'ALS520 Q inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.6			−0.6	mA
	All other inputs					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS520	V_{CC} = 5.5 V			9	15		9	15	mA
	'ALS521				9	15		9	15	

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

TEXAS INSTRUMENTS
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'ALS518, 'ALS519 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS518 SN54ALS519		SN74ALS518 SN74ALS519		
			MIN	MAX	MIN	MAX	
t_{PLH}	P or Q	P=Q	15	37	15	33	ns
t_{PHL}			3	18	3	15	
t_{PLH}	$\overline{G}$	P=Q	15	37	15	33	ns
t_{PHL}			3	18	3	15	

'ALS522 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS522		SN74ALS522		
			MIN	MAX	MIN	MAX	
t_{PLH}	P or Q	$\overline{P=Q}$	10	30	10	25	ns
t_{PHL}			5	25	5	23	
t_{PLH}	$\overline{G}$	$\overline{P=Q}$	8	30	8	25	ns
t_{PHL}			8	30	8	23	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1. For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS520 SN54ALS521		SN74ALS520 SN74ALS521		
			MIN	MAX	MIN	MAX	
t_{PLH}	P or Q	$\overline{P=Q}$	3	16	3	12	ns
t_{PHL}			5	25	5	20	
t_{PLH}	G	$\overline{P=Q}$	2	15	2	12	ns
t_{PHL}			5	23	5	22	

NOTE 1. For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
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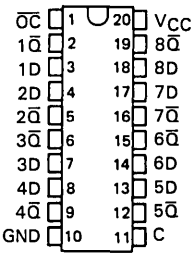
TYPES SN54ALS533, SN54AS533, SN74ALS533, SN74AS533
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

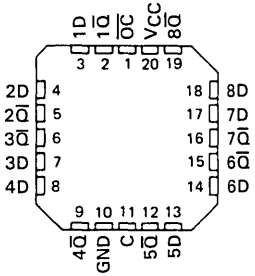
D2661, APRIL 1982

- 8-Latches In a Single Package
- 3-State Bus-Driving Inverting Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- P-N-P Inputs Reduce D-C Loading on Data Lines
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS533, SN54AS533 . . . J PACKAGE
SN74ALS533, SN74AS533 . . . N PACKAGE
(TOP VIEW)



SN54ALS533, SN54AS533 . . . FH PACKAGE
SN74ALS533, SN74AS533 . . . FN PACKAGE
(TOP VIEW)



description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'ALS533 and 'AS533 are transparent D-type latches. While the enable (C) is high, the $\overline{Q}$ outputs will follow the complements of the D inputs. When the enable is taken low, the $\overline{Q}$ outputs will be latched at the inverses of the levels that were set up at the D inputs. The 'ALS533 and 'AS533 are functionally equivalent to the 'ALS373 and 'AS373 except for having inverted outputs.

A buffered output-control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54ALS533 and SN54AS533 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS533 and SN74AS533 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH LATCH)

INPUTS			OUTPUT
$\overline{OC}$	ENABLE C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

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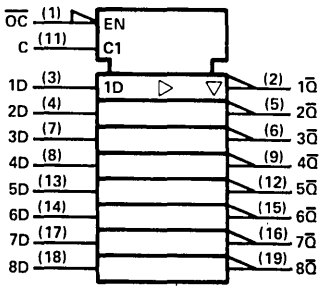
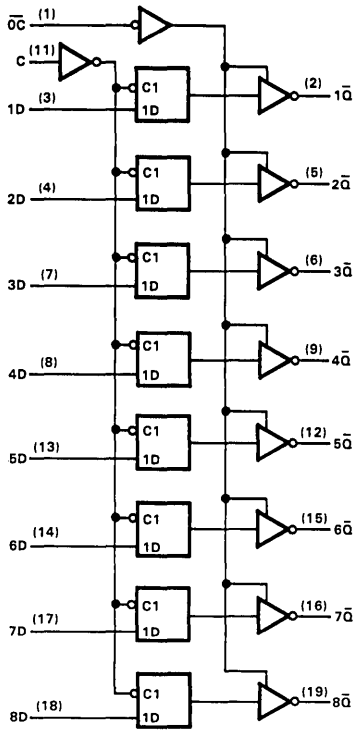
logic symbol



logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS533, SN54AS533 . . . . . −55 °C to 125 °C
SN74ALS533, SN74AS533 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

TEXAS INSTRUMENTS
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recommended operating conditions

		SN54ALS533			SN74ALS533			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							24	
t_w	Pulse duration, Enable C high							ns
t_{su}	Setup time, data before enable C↓							ns
t_h	Hold time, data after enable C↓							ns
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS533			SN74ALS533			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		10			10		mA
		Outputs low		17			17		
		Outputs disabled		18.5			18.5		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

switching characteristics (see note 1)

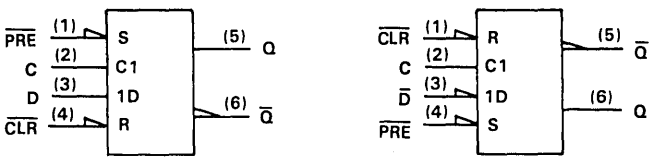
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS533			SN74ALS533			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	D	$\overline{Q}$		10			10		ns
t_{PHL}				10			10		
t_{PLH}	C	Any $\overline{Q}$		13			13		ns
t_{PHL}				13			13		
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$		10			10		ns
t_{PZL}				12			12		
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$		7			7		ns
t_{PLZ}				9			9		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D latch signal conventions

It is TI practice to name the outputs and other inputs of a D-type latch and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.



Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (⊵) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input D, but now both are considered active-low.

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recommended operating conditions

		SN54AS533			SN74AS533			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−12	mA
							−15†	
I_{OL}	Low-level output current			32			32	mA
							48†	
t_w	Pulse duration, enable C high							ns
t_{su}	Setup time, data before enable C↓							ns
t_h	Hold time, data after enable C↓							ns
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS533			SN74AS533			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2		2.4	3.2		V
	V_{CC} = 4.75 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5		0.25	0.5	V
	V_{CC} = 4.75 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.2			−0.2		mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		71			71		mA
		Outputs low							
		Outputs disabled							

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			'AS533			SN54AS533			SN74AS533			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	D	$\overline{Q}$					5.5			5.5		ns
t_{PHL}							4			4		
t_{PLH}	C	Any $\overline{Q}$					7			7		ns
t_{PHL}							5			5		
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$					3.5			3.5		ns
t_{PZL}							5			5.5		
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$					3.5			3.5		ns
t_{PLZ}							5.5			5.5		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

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- **3-State Bus-Driving Inverting Outputs**
- **Buffered Control Inputs**
- **P-N-P Inputs Reduce D-C Loading on Data Lines**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

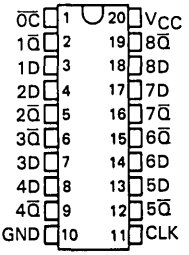
The eight flip-flops of the 'ALS534 and 'AS534 are edge-triggered D-type flip-flops. On the positive transition of the clock, the $\overline{Q}$ outputs will be set to the complement of the logic states that were set up at the D inputs. The 'ALS534 and 'AS534 are functionally equivalent to the 'ALS374 and 'AS374 except for having inverted outputs.

A buffered output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

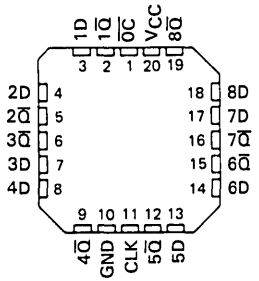
The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN54ALS534 and SN54AS534 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS534 and SN74AS534 are characterized for operation from 0°C to 70°C.

SN54ALS534, SN54AS534 . . . J PACKAGE
SN74ALS534, SN74AS534 . . . N PACKAGE
(TOP VIEW)



SN54ALS534, SN54AS534 . . . FH PACKAGE
SN74ALS534, SN74AS534 . . . FN PACKAGE
(TOP VIEW)



FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

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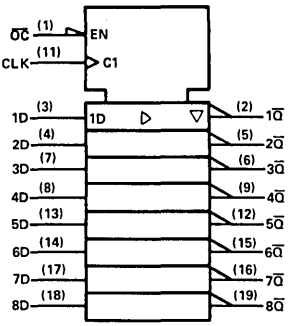
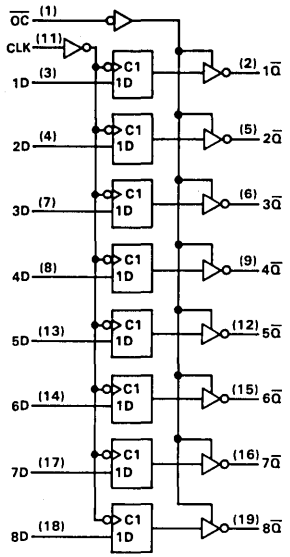
logic symbol



logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS534, SN54AS534 . . . . . −55 °C to 125 °C
SN74ALS534, SN74AS534 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

TEXAS INSTRUMENTS
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recommended operating conditions

			SN54ALS534			SN74ALS534			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1				mA
								−2.6	
I_{OL}	Low-level output current				12				mA
								24	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	CLK high							ns
		CLK low							
t_{su}	Setup time, data before CLK↑								ns
t_h	Hold time, data after CLK↑								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS534			SN74ALS534			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		11			11		mA
		Outputs low		19			19		
		Outputs disabled		20			20		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

switching characteristics (see note 1)

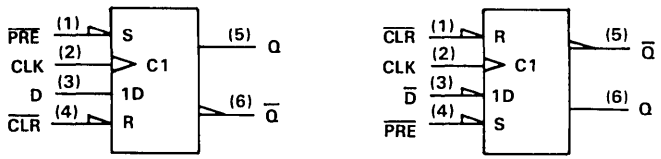
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS534			SN74ALS534			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}				50			50		MHz
t_{PLH}	CLK	Any $\overline{Q}$		8			8		ns
t_{PHL}				8			8		
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$		10			10		ns
t_{PZL}				12			12		
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$		7			7		ns
t_{PLZ}				9			9		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D flip-flop signal conventions

It is TI practice to name the outputs and other inputs of a D-type flip-flop and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.



Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (▷) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input D, but now both are considered active-low.

TEXAS INSTRUMENTS
INCORPORATED
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recommended operating conditions

			SN54AS534			SN74AS534			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−12	mA
								−15†	
I_{OL}	Low-level output current				32			32	mA
								48†	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	CLK high							ns
		CLK low							
t_{su}	Setup time, data before CLK↑								ns
t_h	Hold time, data after CLK↑								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS534			SN74AS534			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2		2.4	3.2		V
		V_{CC} = 4.75 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.75 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	$\overline{OC}$, CLK	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.2			−0.2		mA
	D				−1.3			−1.3		
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		84			84		mA
			Outputs low							
			Outputs disabled							

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			'AS534			SN54AS534			SN74AS534			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}							165			165		MHz
t_{PLH}	CLK	Any $\overline{Q}$					5.5			5.5		ns
t_{PHL}							6			6		
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$					3.5			3.5		ns
t_{PZL}							5			5		
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$					3.5			3.5		ns
t_{PLZ}							5.5			5.5		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

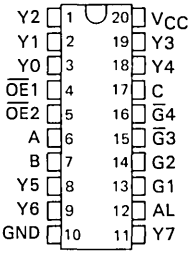
Additional information on these products can be obtained from the factory as it becomes available.

TYPES SN54ALS538, SN74ALS538
3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH 3-STATE OUTPUTS

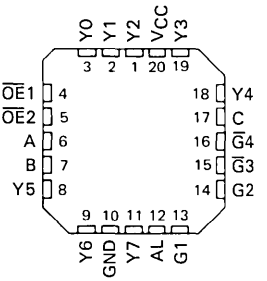
D2661, APRIL 1982

- 3-State Outputs
- Output Polarity Control
- Data Multiplexing Capability
- Multiple Enables for Expansion
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS538 . . . J PACKAGE
SN74ALS538 . . . N PACKAGE
(TOP VIEW)



SN54ALS538 . . . FH PACKAGE
SN74ALS538 . . . FN PACKAGE
(TOP VIEW)



description

The 'ALS538 decoder/demultiplexer accepts three address input signals (A, B, C) and decodes them to select one-of-eight mutually exclusive outputs. If the polarity control input (AL) is high, the outputs are active-low; if AL is low, the outputs are active-high. Two active-high and two active-low input enables are available for easy expansion to 1-of-32 decoding with four packages, or for data demultiplexing to 1-of-8 or 1-of-16 destinations. A high signal on either of the output enables ($\overline{OE}1$ and $\overline{OE}2$) forces all outputs to the high-impedance state.

The SN54ALS538 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS538 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH DECODER/DEMULTIPLEXER)

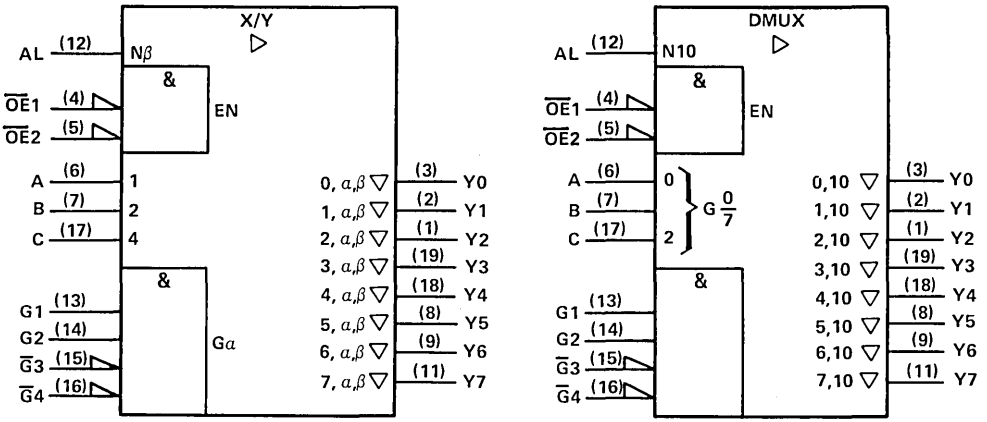
FUNCTION	INPUTS									OUTPUTS							
	$\overline{OE}1$	$\overline{OE}2$	G1	G2	$\overline{G}3$	$\overline{G}4$	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
High impedance (AL = X)	H	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
	X	H	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
Disable (AL = X)	L	L	L	X	X	X	X	X	X	All outputs same level as AL							
	L	L	X	L	X	X	X	X	X								
	L	L	X	X	H	X	X	X	X								
	L	L	X	X	X	H	X	X	X								
Active-High Output (AL = L)	L	L	H	H	L	L	L	L	L	H	L	L	L	L	L	L	L
	L	L	H	H	L	L	L	L	H	L	H	L	L	L	L	L	L
	L	L	H	H	L	L	L	H	L	L	L	H	L	L	L	L	L
	L	L	H	H	L	L	L	H	H	L	L	L	H	L	L	L	L
	L	L	H	H	L	L	H	L	L	L	L	L	L	H	L	L	L
	L	L	H	H	L	L	H	L	H	L	L	L	L	L	H	L	L
	L	L	H	H	L	L	H	H	L	L	L	L	L	L	L	H	L
	L	L	H	H	L	L	H	H	H	L	L	L	L	L	L	L	H
Active-Low Output (AL = H)	L	L	H	H	L	L	L	L	L	L	H	H	H	H	H	H	H
	L	L	H	H	L	L	L	L	H	H	L	H	H	H	H	H	H
	L	L	H	H	L	L	L	H	L	H	H	L	H	H	H	H	H
	L	L	H	H	L	L	L	H	H	H	H	H	L	H	H	H	H
	L	L	H	H	L	L	H	L	L	H	H	H	H	L	H	H	H
	L	L	H	H	L	L	H	L	H	H	H	H	H	H	L	H	H
	L	L	H	H	L	L	H	H	L	H	H	H	H	H	H	L	H
	L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	L

PRODUCT PREVIEW

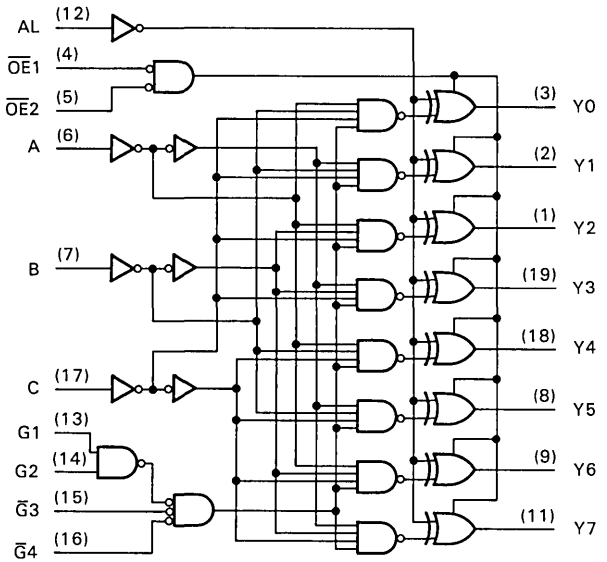
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

2

logic symbols (alternatives)



logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS538 . . . . . −55 °C to 125 °C
SN74ALS538 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

		SN54ALS538			SN74ALS538			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS538			SN74ALS538			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high							mA
		Outputs low							
		Outputs disabled							

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS538			SN74ALS538			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, C	Any Y							ns
t_{PHL}									
t_{PLH}	G1 or G2	Any Y							ns
t_{PHL}									
t_{PLH}	$\overline{G3}$ or $\overline{G4}$	Any Y							ns
t_{PHL}									
t_{PLH}	AL	Any Y							ns
t_{PHL}									
t_{PZH}	$\overline{OE}1$ or $\overline{OE}2$	Any Y							ns
t_{PZL}									
t_{PHZ}	$\overline{OE}1$ or $\overline{OE}2$	Any Y							ns
t_{PLZ}									

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

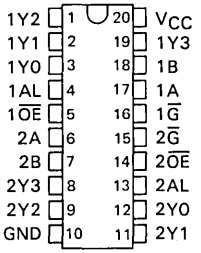
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54ALS539, SN74ALS539
DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS WITH 3-STATE OUTPUTS

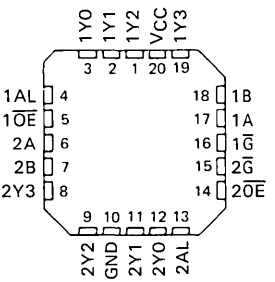
D2661, APRIL 1982

- **3-State Outputs**
- **Output Polarity Control**
- **Data Multiplexing Capability**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS539 . . . J PACKAGE
SN74ALS539 . . . N PACKAGE
(TOP VIEW)



SN54ALS539 . . . FH PACKAGE
SN74ALS539 . . . FN PACKAGE
(TOP VIEW)



description

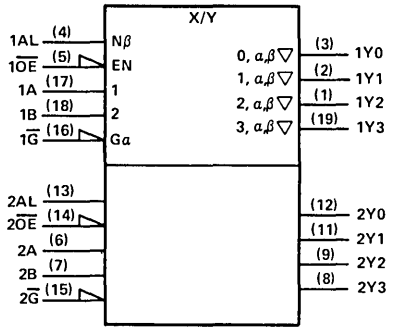
The 'ALS539 decoder/demultiplexer contains two independent decoders, each of which accepts two address input signals (A and B) and decodes them to select one of four mutually exclusive outputs. If the polarity-control input (AL) is high, the outputs are active-low; if AL is low, the outputs are active-high. An active-low input enable ($\overline{G}$) is available for data demultiplexing. Data is routed to the selected output in noninverting form in the active-low mode or in inverted form in the active-high mode. A high signal on the output enable ($\overline{OE}$) forces the 3-state outputs to the high-impedance state.

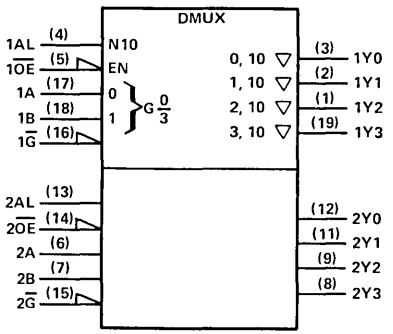
The SN54ALS539 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS539 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(EACH DECODER/DEMULTIPLEXER)

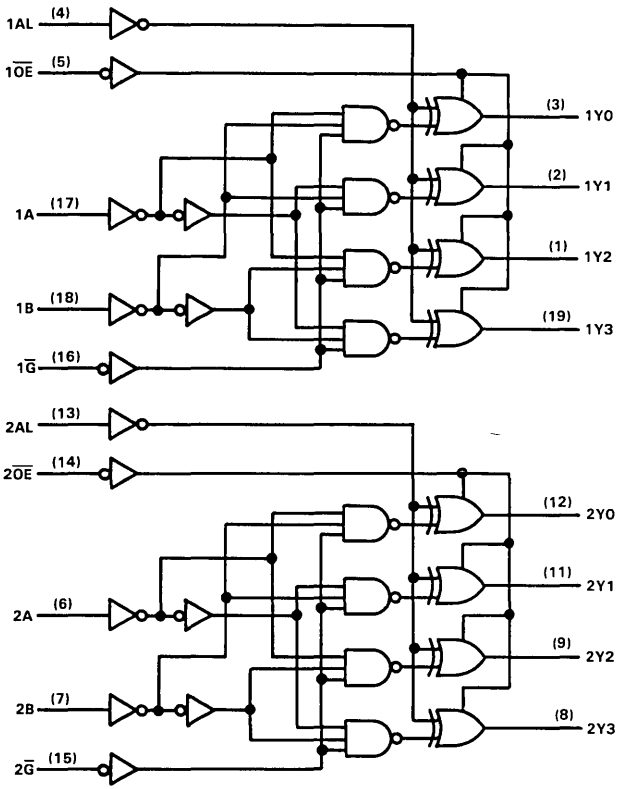
FUNCTION	INPUTS				OUTPUTS			
	$\overline{OE}$	$\overline{G}$	B	A	Y_0	Y_1	Y_2	Y_3
High Impedance	H	X	X	X	Z	Z	Z	Z
Disable	L	H	X	X	All outputs same level as AL			
Active-high Output (AL = L)	L	L	L	L	H	L	L	L
	L	L	L	H	L	H	L	L
	L	L	H	L	L	L	H	L
	L	L	H	H	L	L	L	H
Active-low Output (AL = H)	L	L	L	L	L	H	H	H
	L	L	L	H	H	L	H	H
	L	L	H	L	H	H	L	H
	L	L	H	H	H	H	H	L

logic symbols (alternatives)





logic diagram (positive logic)



Pin numbers shown are for J and N packages.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS539 . . . . . −55 °C to 125 °C
SN74ALS539 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS539			SN74ALS539			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS539			SN74ALS539			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high							mA
		Outputs low							
		Outputs disabled							

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS539			SN74ALS539			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y							ns
t_{PHL}									
t_{PLH}	$\overline{G}$	Y							ns
t_{PHL}									
t_{PLH}	P	Y							ns
t_{PHL}									
t_{PZH}	$\overline{OC}$	Y							ns
t_{PZL}									
t_{PHZ}	$\overline{OC}$	Y							ns
t_{PLZ}									

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

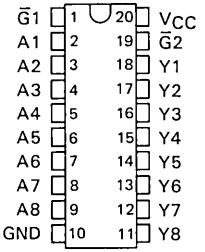
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54ALS540, SN54ALS541, SN74ALS540, SN74ALS541
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

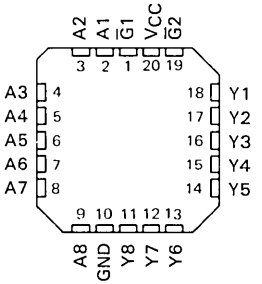
D2661, APRIL 1982

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **P-N-P Inputs Reduce D-C Loading**
- **Data Flow-Thru Pinout (All Inputs on Opposite Side from Outputs)**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS540, SN54ALS541 . . . J PACKAGE
SN74ALS540, SN74ALS541 . . . N PACKAGE
(TOP VIEW)



SN54ALS540, SN54ALS541 . . . FH PACKAGE
SN74ALS540, SN74ALS541 . . . FN PACKAGE
(TOP VIEW)



description

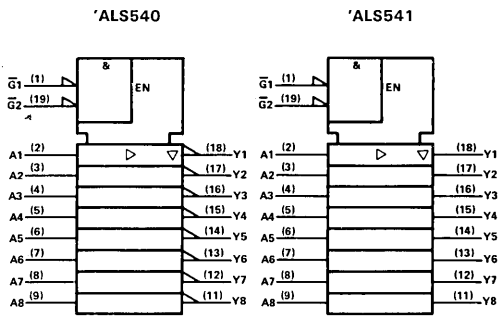
These octal buffers and line drivers are designed to have the performance of the popular SN54ALS240/SN74ALS240 series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout.

The three-state control gate is a 2-input NOR such that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high-impedance state.

The 'ALS540 provides inverted data and the 'ALS541 provides true data at the outputs.

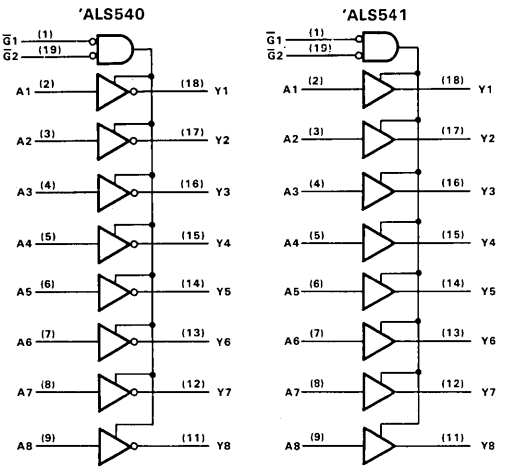
The SN54ALS540 and SN54ALS541 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS540 and SN74ALS541 are characterized for operation from 0 °C to 70 °C.

logic symbols



Pin numbers shown are for J and N packages

logic diagrams (positive logic)



ADVANCE INFORMATION

This page contains information on a new product. Specifications are subject to change without notice.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS540, SN54ALS541 . . . . . −55°C to 125°C
SN74ALS540, SN74ALS541 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

2

recommended operating conditions

		SN54ALS540 SN54ALS541			SN74ALS540 SN74ALS541			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12				mA
							−15	
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS540 SN54ALS541			SN74ALS540 SN74ALS541			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS540	V_{CC} = 5.5 V	Outputs high		15			15		mA
			Outputs low		18			18		
			Outputs disabled		19			19		
	'ALS541	V_{CC} = 5.5 V	Outputs high		15			15		mA
			Outputs low		18			18		
			Outputs disabled		19			19		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

TEXAS INSTRUMENTS
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'ALS540 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS540			SN74ALS540			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y		6			6		ns
t_{PHL}				6			6		
t_{PZH}	$\overline{G}$	Y		13			13		ns
t_{PZL}				18			18		
t_{PHZ}	$\overline{G}$	Y		7			7		ns
t_{PLZ}				11			11		

'ALS541 switching characteristics (see note 1)

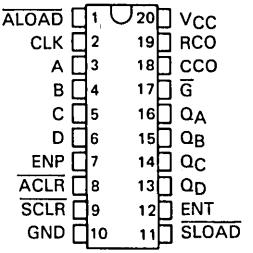
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS541			SN74ALS541			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y		6			6		ns
t_{PHL}				6			6		
t_{PZH}	$\overline{G}$	Y		13			13		ns
t_{PZL}				18			18		
t_{PHZ}	$\overline{G}$	Y		7			7		ns
t_{PLZ}				11			11		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

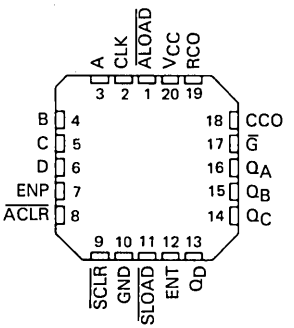
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- **Carry Output for n-Bit Cascading**
- **Buffer-Type Outputs Drive Bus Lines Directly**
- **Choice of Asynchronous or Synchronous Load or Clear**
- **Internal Look-Ahead for Fast Cascading**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS560, SN54ALS561 . . . J PACKAGE
SN74ALS560, SN74ALS561 . . . N PACKAGE
(TOP VIEW)



SN54ALS560, SN54ALS561 . . . FH PACKAGE
SN74ALS560, SN74ALS561 . . . FN PACKAGE
(TOP VIEW)



description

The 'ALS560 decade counters and 'ALS561 binary counters are programmable and offer synchronous and asynchronous clearing as well as synchronous and asynchronous loading. All synchronous functions are executed on the positive-going edge of the clock.

The clear function is initiated by applying a low level to either Asynchronous Clear ($\overline{ACLR}$) or Synchronous Clear ($\overline{SCLR}$). Asynchronous (direct) clearing overrides all other functions of the device, while synchronous clearing overrides only the other synchronous functions. Data is loaded from the A, B, C, and D inputs by applying a low level to Asynchronous Load ($\overline{ALOAD}$) or by the combination of a low level at Synchronous Load ($\overline{SLOAD}$) and a positive-going clock transition. The counting function is enabled only when Enable P (ENP), Enable T (ENT), $\overline{ACLR}$, $\overline{ALOAD}$, $\overline{SCLR}$, and $\overline{SLOAD}$ are all high.

A high level at the Output Enable ($\overline{G}$) forces the Q outputs into the high-impedance state, and a low level enables those outputs. Counting is independent of $\overline{G}$. ENT is fed forward to enable the Ripple Carry Output (RCO) to produce a high-level pulse while the count is maximum (9 or 15). The Clocked Carry Output (CCO) produces a high-level pulse for a duration equal to that of the low level of the clock when RCO is high and the counter is enabled (both ENP and ENT are high); otherwise, CCO is low. CCO does not have the glitches commonly associated with a ripple-carry output. Cascading is normally accomplished by connecting RCO or CCO of the first counter to ENT of the next counter. However, for very-high-speed counting, RCO should be used for cascading since CCO does not become active until the clock returns to the low level.

The SN54ALS560 and SN54ALS561 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS560 and SN74ALS561 are characterized for operation from 0°C to 70°C.

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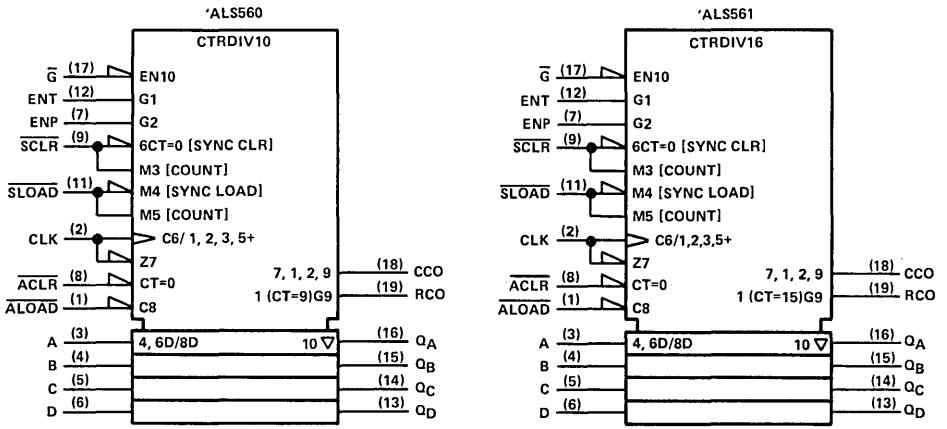
FUNCTION TABLE

INPUTS								OPERATION
$\overline{G}$	$\overline{ACLR}$	$\overline{ALOAD}$	$\overline{SCLR}$	$\overline{SLOAD}$	ENT	ENP	CLK	
H	X	X	X	X	X	X	X	Q Outputs Disabled
L	L	X	X	X	X	X	X	Asynchronous Clear
L	H	L	X	X	X	X	X	Asynchronous Load
L	H	H	L	X	X	X	↑	Synchronous Clear
L	H	H	H	L	X	X	↑	Synchronous Load
L	H	H	H	H	H	H	↑	Count
L	H	H	H	H	L	X	X	Inhibit Counting
L	H	H	H	H	X	L	X	Inhibit Counting

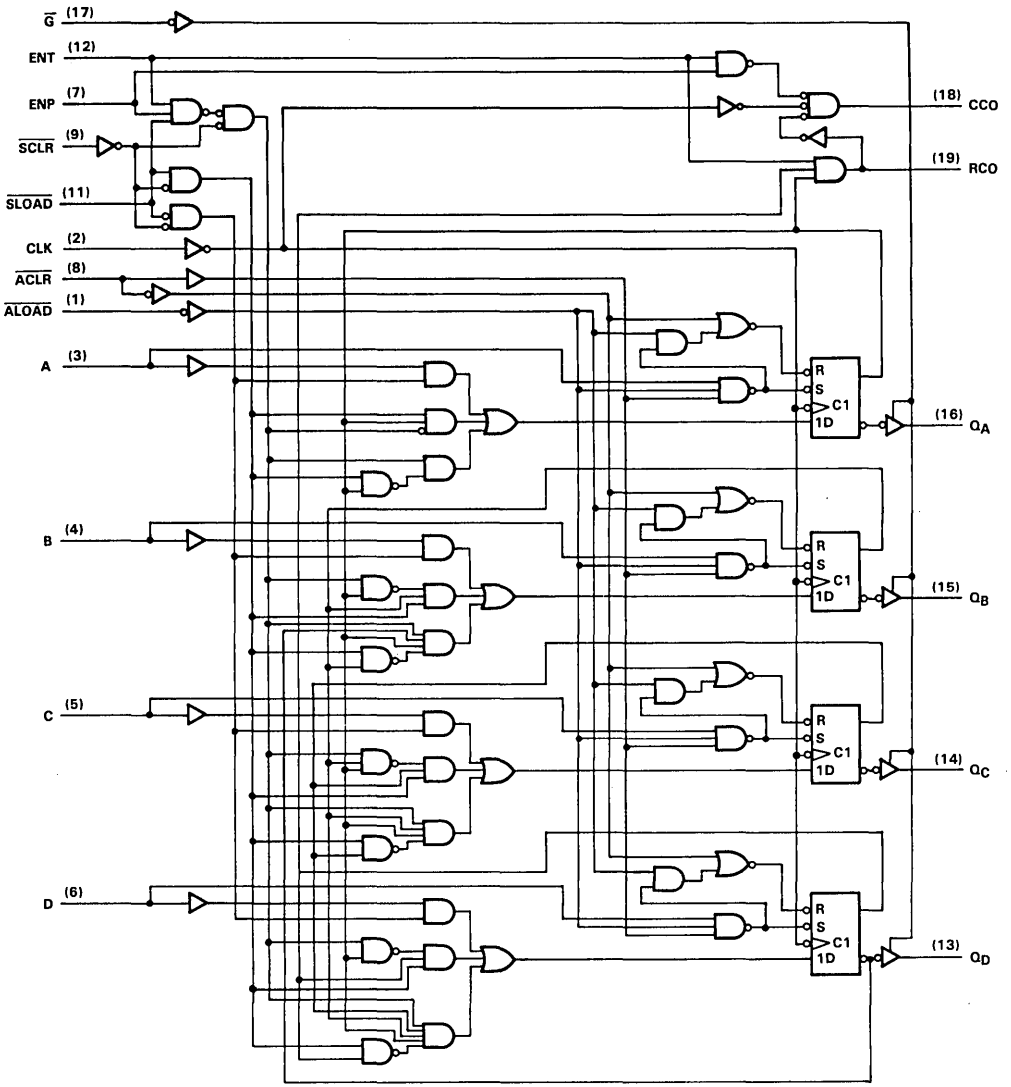
2

logic symbols



Pin numbers shown are for J and N packages.

'ALS560 logic diagram (positive logic)



Pin numbers shown are for J and N packages

TEXAS INSTRUMENTS
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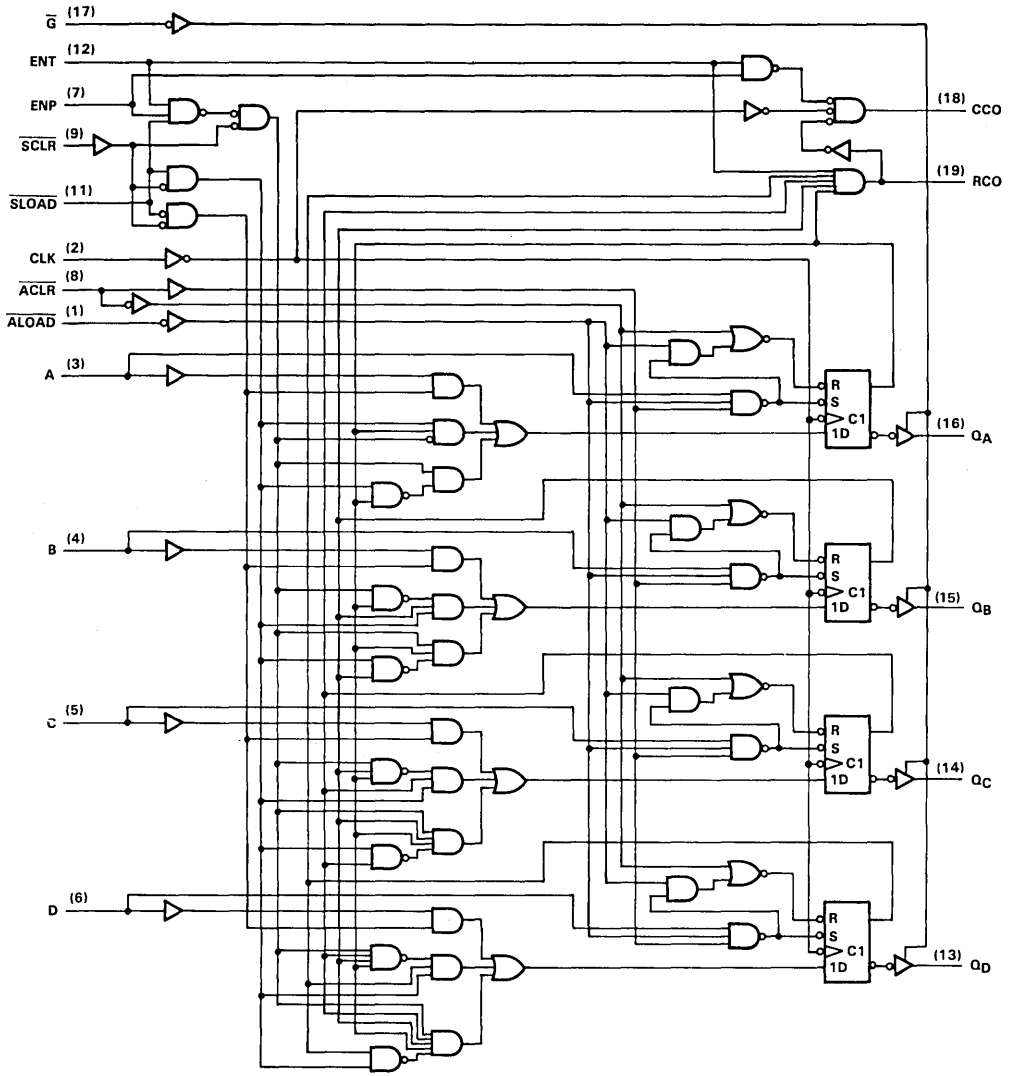
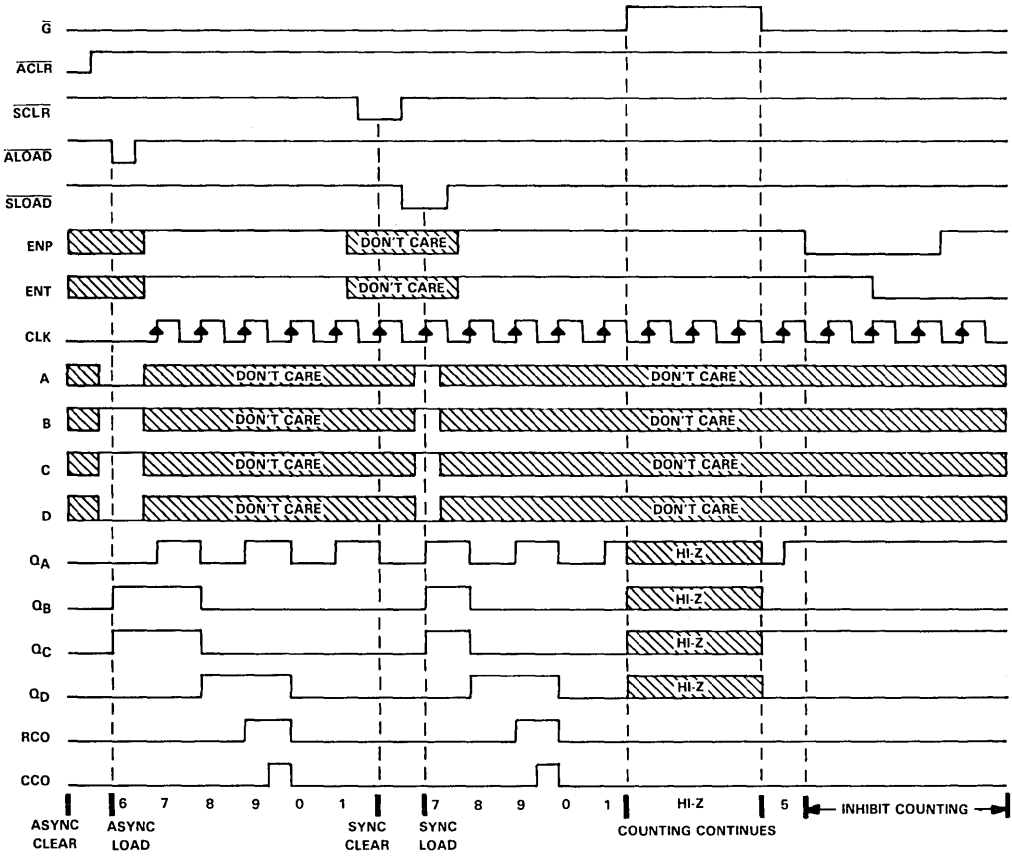
'ALS561 logic diagram (positive logic)



Pin numbers shown are for J and N packages

'ALS560 typical load, count, and inhibit sequences



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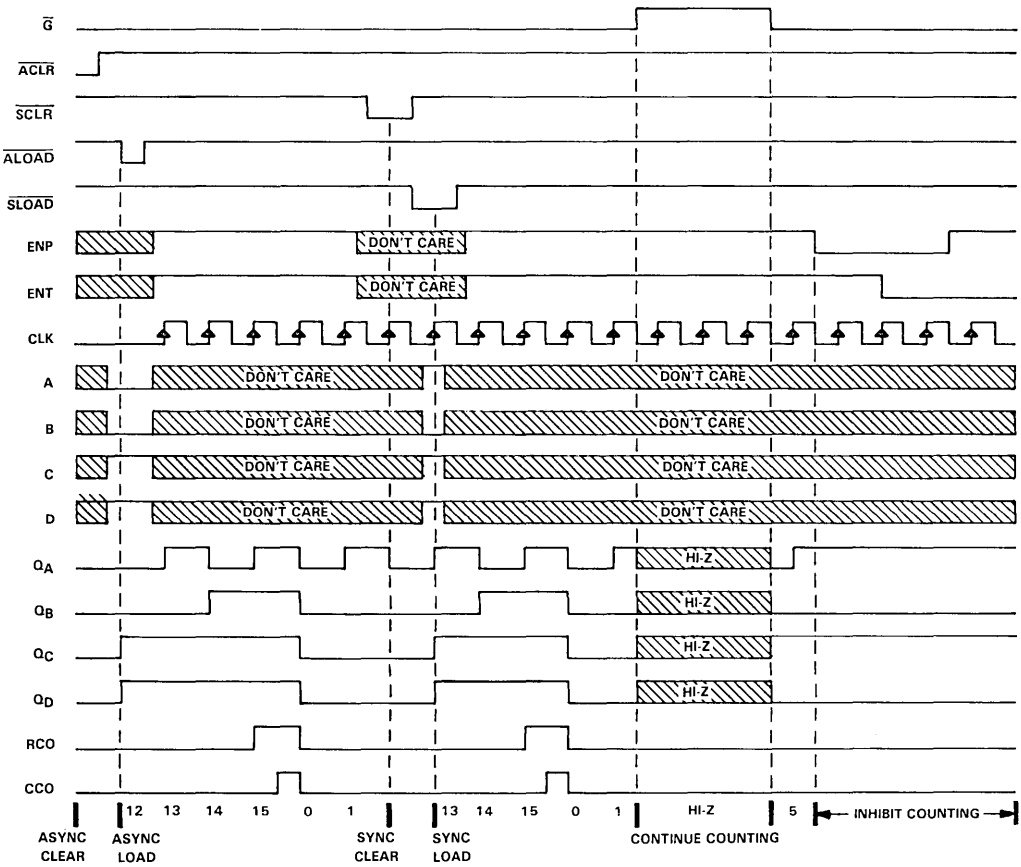
'ALS561 typical load, count, and inhibit sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS560, SN54ALS561 . . . . . −55 °C to 125 °C
SN74ALS560, SN74ALS561 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

				SN54ALS560 SN54ALS561			SN74ALS560 SN74ALS561			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
I_{OH}	High-level output voltage	Q outputs				−1			−2.6	mA
		CCO and RCO				−0.4			−0.4	
I_{OL}	Low-level output current	Q outputs				12			24	mA
		CCO and RCO				4			8	
f_{clock}	Clock frequency	'ALS560		0		18	0		20	MHz
		'ALS561		0		25	0		30	
t_w	Pulse duration	$\overline{ACLR}$ or $\overline{ALOAD}$ low		20			15			ns
		'ALS560	CLK high	27.5			25			
			CLK low	27.5			25			
		'ALS561	CLK high	20			16.5			
			CLK low	20			16.5			
t_{su}	Setup time before CLK↑	ENP, ENT	High	25			20			ns
			Low	25			20			
		Data at A, B, C, D		25			20			
		$\overline{SCLR}$	Low	21			15			
			High (inactive)	35			30			
		$\overline{SLOAD}$	Low	20			15			
			High (inactive)	35			30			
		$\overline{ACLR}$ or $\overline{ALOAD}$ inactive		10			10			
t_h	Hold time after CLK↑ for data, ENP, ENT, $\overline{SCLR}$, or $\overline{SLOAD}$			0			0			ns
T_A	Operating free-air temperature			−55		125	0	70		°C

TEXAS INSTRUMENTS
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS560 SN54ALS561			SN74ALS560 SN74ALS561			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	Q outputs	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
		V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
	CCO and RCO	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4					
		V_{CC} = 4.5 V	I_{OH} = −0.4 mA				2.7	3.4		
V_{OL}	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
	CCO and RCO	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	ENT and ENP	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	Other inputs					0.1			0.1	
I_{IH}	ENT and ENP	V_{CC} = 5.5 V,	V_I = 0.4 V			40			40	μA
	Other inputs					20			20	
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		17	27		17	27	mA
			Outputs low		21	33		21	33	
			Outputs disabled		22	36		22	36	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS560 SN54ALS561		SN74ALS560 SN74ALS561		
			MIN	MAX	MIN	MAX	
f_{max}	'ALS560		18		20		MHz
	'ALS561		25		30		
t_{PLH}	CLK	Any Q	4	15	4	12	ns
t_{PHL}			5	21	5	18	
t_{PLH}	CLK	RCO	9	35	9	29	ns
t_{PHL}			8	29	8	24	
t_{PLH}	CLK	CCO	8	31	8	26	ns
t_{PHL}			5	20	5	16	
t_{PLH}	$\overline{ALOAD}$	Any Q	10	38	10	35	ns
t_{PHL}			7	27	7	23	
t_{PLH}	$\overline{ALOAD}$	RCO	15	55	15	42	ns
t_{PHL}			12	35	12	30	
t_{PLH}	$\overline{ALOAD}$	CCO	25	65	25	55	ns
t_{PHL}			12	42	12	33	
t_{PLH}	A, B, C, or D	Any Q	8	35	8	30	ns
t_{PHL}			7	27	7	22	
t_{PLH}	ENT	RCO	5	20	5	16	ns
t_{PHL}			4	18	4	14	
t_{PLH}	ENT	CCO	12	35	12	32	ns
t_{PHL}			4	15	4	12	
t_{PLH}	ENP	CCO	5	22	5	18	ns
t_{PHL}			4	14	4	12	
t_{PHL}	$\overline{ACLR}$	Any Q	7	28	7	22	ns
t_{PZH}	$\overline{G}$	Any Q	5	24	5	19	ns
t_{PZL}			8	28	8	23	
t_{PHZ}	$\overline{G}$	Any Q	2	15	2	10	ns
t_{PLZ}			4	20	4	15	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
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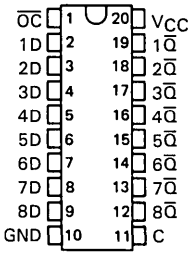
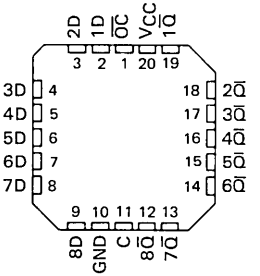
- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas instruments Quality and Reliability**

SN54ALS563 . . . J PACKAGE
SN74ALS563 . . . N PACKAGE
(TOP VIEW)



SN54ALS563 . . . FH PACKAGE
SN74ALS563 . . . FN PACKAGE
(TOP VIEW)



description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type latches. While the enable (C) is high the $\overline{Q}$ outputs will follow the complements of data (D) inputs. When the enable is taken low the output will be latched at the inverses of the levels that were set up at the D inputs.

A buffered output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased high-logic level provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control ($\overline{OC}$) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

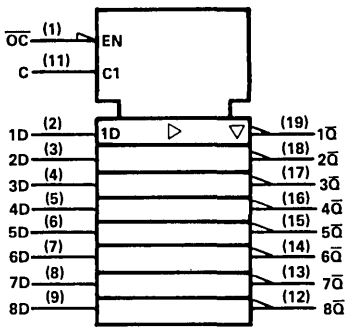
The SN54ALS563 is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS563 is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE
(Each Latch)

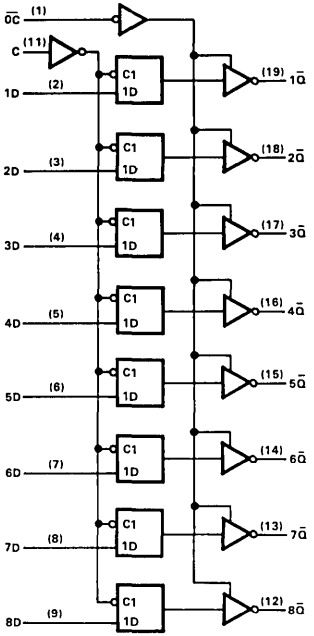
INPUTS			OUTPUT
ENABLE			
$\overline{OC}$	C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

2

logic symbol



logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS563 . . . . . −55 °C to 125 °C
SN74ALS563 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS563			SN74ALS563			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							24	
t_w	Pulse duration, enable C high	15			15			ns
t_{su}	Setup time, data before enable C↓	10			10			ns
t_h	Hold time, data after enable C↓	10			10			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

TEXAS INSTRUMENTS
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS563			SN74ALS563			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		10	17		10	17	mA
		Outputs low		15	24		15	24	
		Outputs disabled		16	27		16	27	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

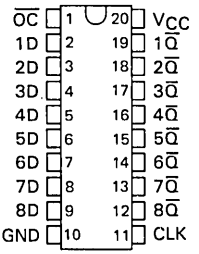
switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = MIN to MAX				UNIT
			SN54ALS563		SN74ALS563		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$	3	21	3	18	ns
t_{PHL}			3	15	3	14	
t_{PLH}	C	$\overline{Q}$	8	29	8	22	ns
t_{PHL}			8	22	8	21	
t_{PZH}	$\overline{OC}$	$\overline{Q}$	4	21	4	18	ns
t_{PZL}			4	21	4	18	
t_{PHZ}	$\overline{OC}$	$\overline{Q}$	2	10	2	8	ns
t_{PLZ}			3	15	3	13	

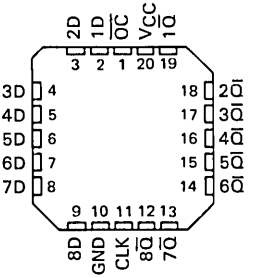
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- **3-State Buffer-Type Inverting Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Buffered Control Inputs**
- **Package Options include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS564 . . . J PACKAGE
SN74ALS564 . . . N PACKAGE
(TOP VIEW)



SN54ALS564 . . . FH PACKAGE
SN74ALS564 . . . FN PACKAGE
(TOP VIEW)



description

These 8-bit registers feature inverting three-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight-bit edge-triggered D-type flip-flops enter data on the low-to-high transition of the clock.

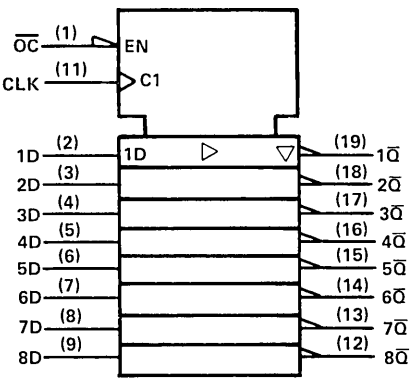
The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS564 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS564 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

logic symbol



Pin numbers shown are for J and N packages.

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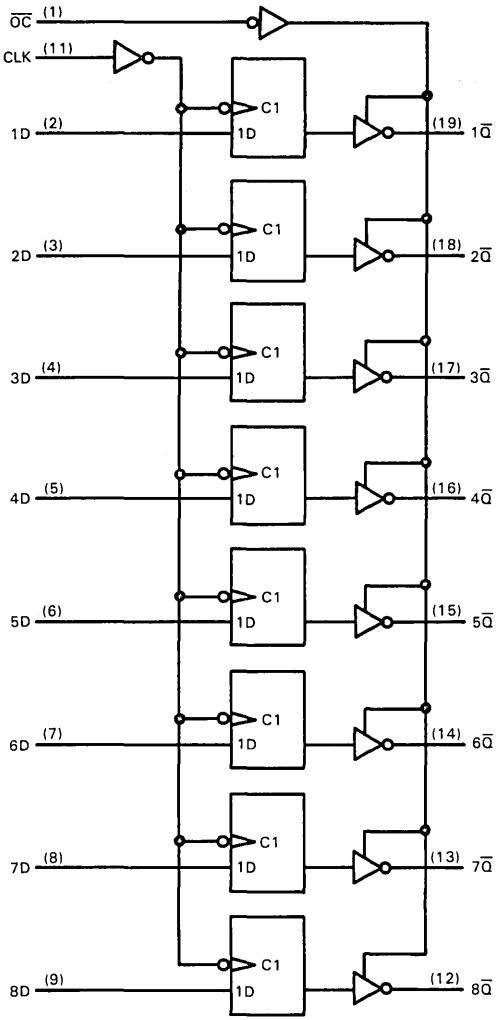
logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS564 . . . . . −55 °C to 125 °C
SN74ALS564 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS564			SN74ALS564			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1				mA
								−2.6	
I_{OL}	Low-level output current				12				mA
								24	
f_{clock}	Clock frequency		0		30	0		35	MHz
t_w	Pulse duration	CLK high	16.5			14			ns
		CLK low	16.5			14			
t_{su}	Setup time, data before CLK↑		10			10			ns
t_h	Hold time, data after CLK↑		4			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical charactoristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS564			SN74ALS564			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_{IL} = 0.4 V			−0.2			−0.2	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	V_{CC} = 5.5 V,	Outputs high		10	17		10	17	mA
		Outputs low		15	24		15	24	
		Outputs disabled		16	27		16	27	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS564		SN74ALS564		
			MIN	MAX	MIN	MAX	
f_{max}			30		35		MHz
t_{PLH}	CLK	$\overline{Q}$	4	15	4	14	ns
t_{PHL}			4	15	4	14	
t_{PZH}	$\overline{OC}$	$\overline{Q}$	4	21	4	18	ns
t_{PZL}			4	21	4	18	
t_{PHZ}	$\overline{OC}$	$\overline{Q}$	2	10	2	8	ns
t_{PLZ}			3	15	3	13	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

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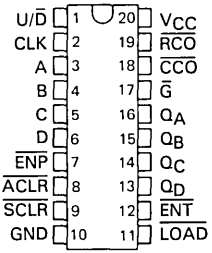
TYPES SN54ALS568, SN54ALS569, SN74ALS568, SN74ALS569 SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS WITH 3-STATE OUTPUTS

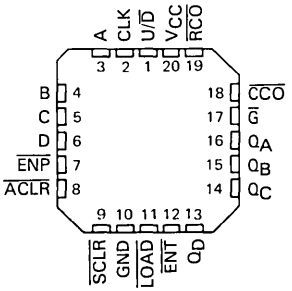
D2661, APRIL 1982

- 3-State Q Outputs Drive Bus Lines Directly
- Counter Operation Independent of 3-State Output
- Fully Synchronous Clear, Count, and Load
- Asynchronous Clear Also Provided
- Fully Cascadable
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS568, SN54ALS569 . . . J PACKAGE
SN74ALS568, SN74ALS569 . . . N PACKAGE
(TOP VIEW)



SN54ALS568, SN54ALS569 . . . FH PACKAGE
SN74ALS568, SN74ALS569 . . . FN PACKAGE
(TOP VIEW)



description

The 'ALS568 decade counters and 'ALS569 binary counters are programmable, count up or down, and offer both synchronous and asynchronous clearing. All synchronous functions are executed on the positive-going edge of the clock.

The clear function is initiated by applying a low level to either Asynchronous Clear ($\overline{ACLR}$) or Synchronous Clear ($\overline{SCLR}$). Asynchronous (direct) clearing overrides all other functions of the device, while synchronous clearing overrides only the other synchronous functions. Data is loaded from the A, B, C, and D inputs by holding Load ($\overline{LOAD}$) low during a positive-going clock transition. The counting function is enabled only when Enable P ($\overline{ENP}$) and Enable T ($\overline{ENT}$) are low and $\overline{ACLR}$, $\overline{SCLR}$, and $\overline{LOAD}$ are high. The Up/Down (U/$\overline{D}$) input controls the direction of the count. These counters count up when U/$\overline{D}$ is high and count down when U/$\overline{D}$ is low.

A high level at the Output Enable ($\overline{G}$) forces the Q outputs into the high-impedance state, and a low level enables those outputs. Counting is independent of of $\overline{G}$. $\overline{ENT}$ is fed forward to enable the Ripple Carry Output ($\overline{RCO}$) to produce a low-level pulse while the count is zero (all Q outputs low) when counting down or maximum (9 or 15) when counting up. The Clocked Carry Output ($\overline{CCO}$) produces a low level pulse for a duration equal to that of the low level of the clock when $\overline{RCO}$ is low and the counter is enabled (both $\overline{ENP}$ and $\overline{ENT}$ are low); otherwise, $\overline{CCO}$ is high. $\overline{CCO}$ does not have the glitches commonly associated with a ripple-carry output. Cascading is normally accomplished by connecting $\overline{RCO}$ or $\overline{CCO}$ of the first counter to $\overline{ENT}$ of the next counter. However, for very-high-speed counting, $\overline{RCO}$ should be used for cascading since $\overline{CCO}$ does not become active until the clock returns to the low level.

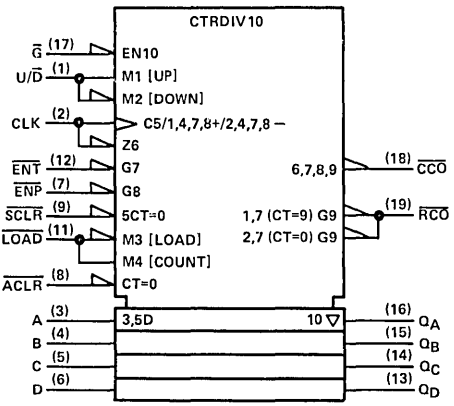
The SN54ALS568 and SN54ALS569 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS568 and SN74ALS569 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE

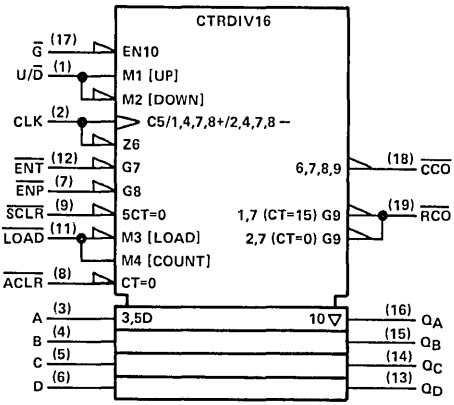
INPUTS								OPERATION
$\overline{G}$	$\overline{ACLR}$	$\overline{SCLR}$	$\overline{LOAD}$	$\overline{ENT}$	$\overline{ENP}$	U/$\overline{D}$	CLK	
H	X	X	X	X	X	X	X	Q Outputs Disabled
L	L	X	X	X	X	X	X	Asynchronous Clear
L	H	L	X	X	X	X	↑	Synchronous Clear
L	H	H	L	X	X	X	↑	Load
L	H	H	H	L	L	H	↑	Count Up
L	H	H	H	L	L	L	↑	Count Down
L	H	H	H	H	X	X	X	Inhibit Count
L	H	H	H	X	H	X	X	Inhibit Count

logic symbols

'ALS568



'ALS569



Pin numbers shown are for J and N packages.

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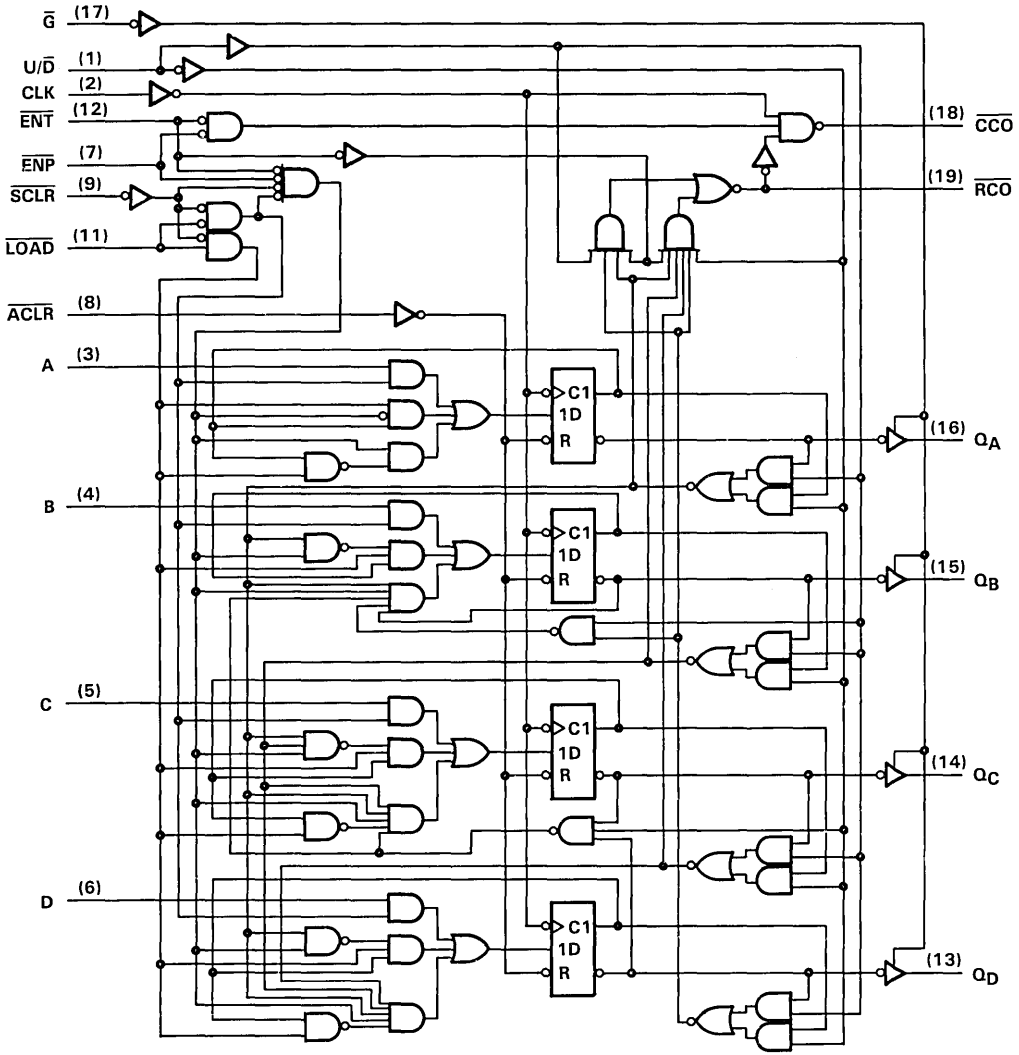
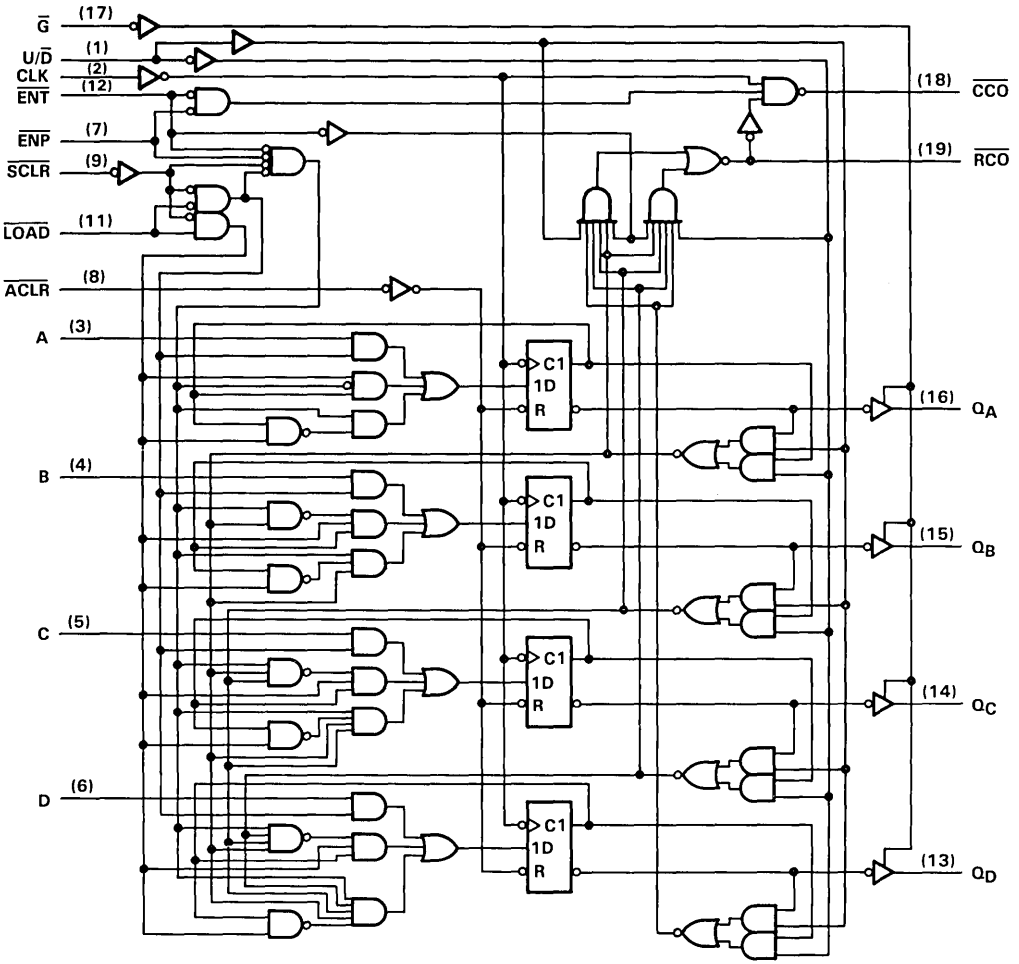
'ALS568 logic diagram (positive logic)



Pin numbers shown are for J and N packages

'ALS569 logic diagram (positive logic)



Pin numbers shown are for J and N packages

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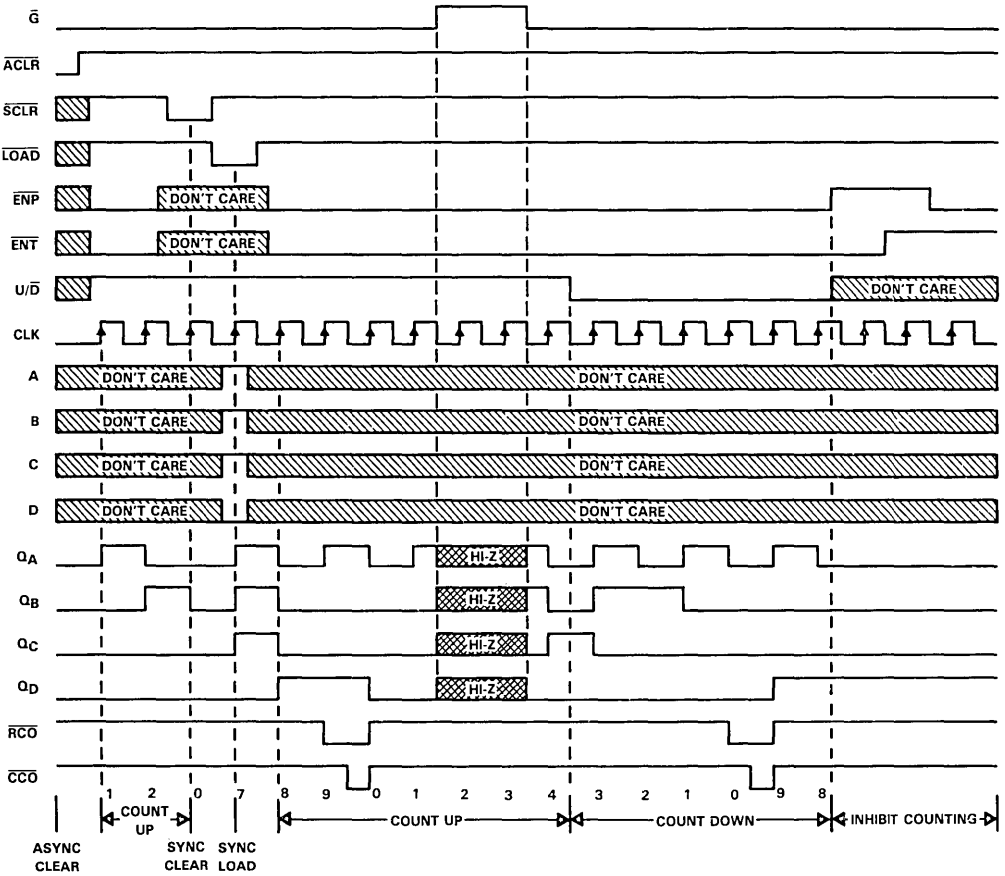
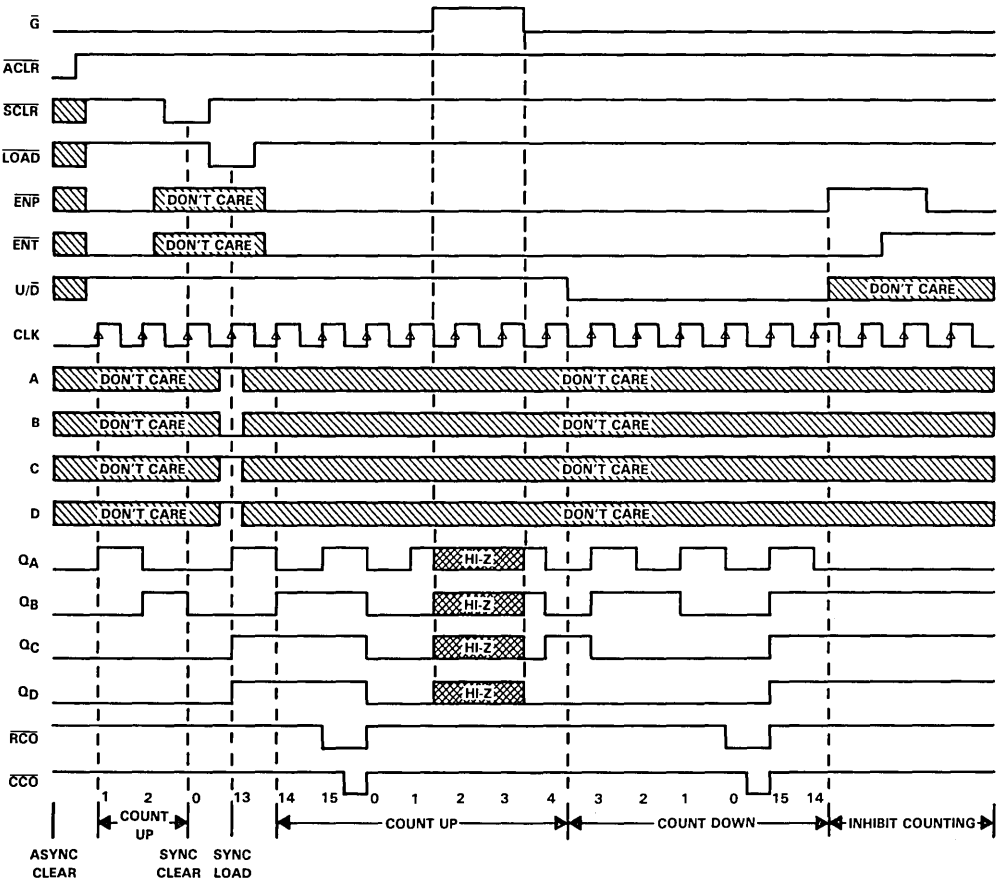
'ALS568 typical load, count, and inhibit sequences



'ALS569 typical load, count, and inhibit sequences



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS568, SN54ALS569 . . . . . −55°C to 125°C
SN74ALS568, SN74ALS569 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

2

recommended operating conditions

				SN54ALS568 SN54ALS569			SN74ALS568 SN74ALS569			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
I_{OH}	High-level output current	Q outputs				−1				mA
									−2.6	
		$\overline{CCO}$ and $\overline{RCO}$				−0.4			−0.4	
I_{OL}	Low-level output current	Q outputs				12				mA
									24	
		$\overline{CCO}$ and $\overline{RCO}$				4				
									8	
f_{clock}	Clock frequency	'ALS568		0		18	0		20	MHz
		'ALS569		0		25	0		30	
t_w	Pulse duration	$\overline{ACLR}$ or $\overline{LOAD}$ low		20			15			ns
		'ALS568	CLK high	27.5			25			
			CLK low	27.5			25			
		'ALS569	CLK high	20			16.5			
			CLK low	20			16.5			
t_{su}	Setup time before CLK↑	Data at A, B, C, D		25			20			ns
		$\overline{ENP}$, $\overline{ENT}$	High	35			30			
			Low	25			20			
		$\overline{SCLR}$	Low	20			15			
			High (inactive)	35			30			
		$\overline{LOAD}$	Low	20			15			
			High (inactive)	35			30			
		U/$\overline{D}$		35			30			
		$\overline{ACLR}$ inactive		10			10			
t_h	Hold time after CLK↑ for any input			0			0			ns
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS568 SN54ALS569			SN74ALS568 SN74ALS569			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	Q outputs	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
		V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
	$\overline{CCO}$ and $\overline{RCO}$	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4					
		V_{CC} = 4.5 V	I_{OH} = −0.4 mA				2.7	3.4		
V_{OL}	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
	$\overline{CCO}$ and $\overline{RCO}$	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 0.4 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		16	26		16	26	mA
			Outputs low		20	32		20	32	
			Outputs disabled		20	32		20	32	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

TEXAS INSTRUMENTS
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switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS568 SN54ALS569		SN74ALS568 SN74ALS569		
			MIN	MAX	MIN	MAX	
f_{max}	'ALS568		18		20		MHz
	'ALS569		25		30		
t_{PLH}	CLK	Any Q	4	17	4	13	ns
t_{PHL}			7	18	7	16	
t_{PLH}	CLK	$\overline{RCO}$	12	31	12	28	ns
t_{PHL}			10	22	10	19	
t_{PLH}	CLK	$\overline{CCO}$	5	15	5	13	ns
t_{PHL}			6	30	6	25	
t_{PLH}	U/$\overline{D}$	$\overline{RCO}$	9	25	9	23	ns
t_{PHL}			9	23	9	19	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	6	17	6	15	ns
t_{PHL}			4	17	4	13	
t_{PLH}	$\overline{ENT}$	$\overline{CCO}$	5	15	5	13	ns
t_{PHL}			9	28	9	23	
t_{PLH}	$\overline{ENP}$	$\overline{CCO}$	4	14	4	12	ns
t_{PHL}			5	17	5	14	
t_{PHL}	$\overline{ACLR}$	Any Q	9	22	9	20	ns
t_{PZH}	$\overline{G}$	Any Q	6	21	6	18	ns
t_{PZL}			11	29	11	24	
t_{PHZ}	$\overline{G}$	Any Q	1	8	1	8	ns
t_{PLZ}			3	19	3	13	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2661, DECEMBER 1982

- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Choice of True or Inverting Logic**

'ALS573, 'AS573	True Outputs
'ALS580, 'AS580	Inverting Outputs

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

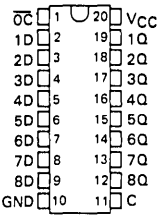
The eight latches are transparent D-type latches. While the enable (C) is high the outputs (Q or $\overline{Q}$) will respond to the data (D) inputs. When the enable is taken low the outputs will be latched to retain the data that was set up.

A buffered output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

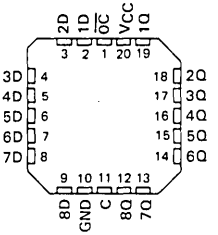
The output control ($\overline{OC}$) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are at high impedance.

The SN54ALS573, SN54AS573, SN54ALS580 and SN54AS580 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS573, SN74AS573, SN74ALS580, and SN74AS580 are characterized for operation from 0 °C to 70 °C.

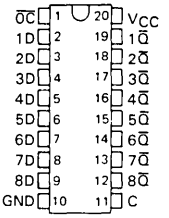
SN54ALS573, SN54AS573 . . . J PACKAGE
SN74ALS573, SN74AS573 . . . N PACKAGE
(TOP VIEW)



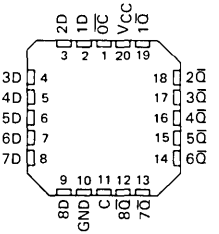
SN54ALS573, SN54AS573 . . . FH PACKAGE
SN74ALS573, SN74AS573 . . . FN PACKAGE
(TOP VIEW)



SN54ALS580, SN54AS580 . . . J PACKAGE
SN74ALS580, SN74AS580 . . . N PACKAGE
(TOP VIEW)



SN54ALS580, SN54AS580 . . . FH PACKAGE
SN74ALS580, SN74AS580 . . . FN PACKAGE
(TOP VIEW)



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FUNCTION TABLES

'ALS573, 'AS573
(EACH LATCH)

INPUTS			OUTPUT
ENABLE			
$\overline{OC}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

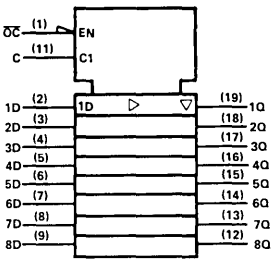
'ALS580, 'AS580
(EACH LATCH)

INPUTS			OUTPUT
ENABLE			
$\overline{OC}$	C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

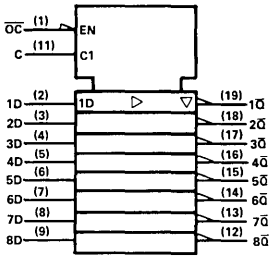
2

logic symbols

'ALS573, 'AS573

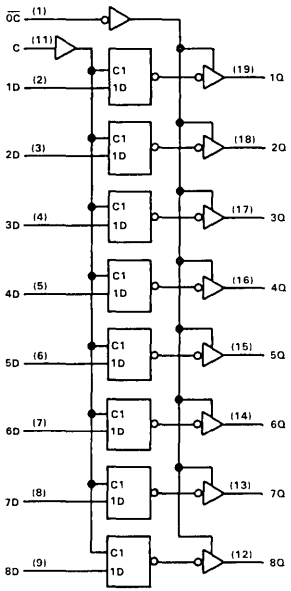


'ALS580, 'AS580

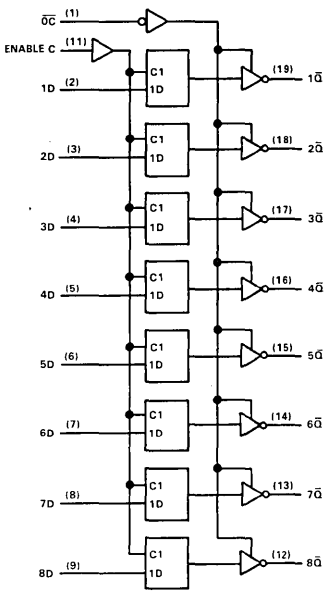


logic diagram (positive logic)

'ALS573, 'AS573



'ALS580, 'AS580



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS573, SN54ALS580 . . . . . −55 °C to 125 °C
SN74ALS573, SN74ALS580 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS573 SN54ALS580			SN74ALS573 SN74ALS580			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1				mA
								−2.6	
I_{OL}	Low-level output current				12				mA
								24	
t_w	Pulse duration, enable C high	'ALS573	10			10			ns
		'ALS580	15			15			
t_{su}	Setup time, data before enable C↓		10			10			ns
t_h	Hold time, data after enable C↓	'ALS573	7			7			ns
		'ALS580	10			10			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS573 SN54ALS580			SN74ALS573 SN74ALS580			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
		V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	'ALS573	V_{CC} = 5.5 V	Outputs high		10	17		10	17	mA
			Outputs low		15	24		15	24	
			Outputs disabled		16	27		16	27	
	'ALS580		Outputs high		10	17		10	17	
			Outputs low		15	24		15	24	
			Outputs disabled		16	27		16	27	

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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'ALS573 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS573		SN74ALS573		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	2	15	2	14	ns
t_{PHL}			2	15	2	14	
t_{PLH}	C	Q	8	27	8	20	ns
t_{PHL}			8	20	8	19	
t_{PZH}	$\overline{OC}$	Q	4	21	4	18	ns
t_{PZL}			4	21	4	18	
t_{PHZ}	$\overline{OC}$	Q	2	10	2	8	ns
t_{PLZ}			3	15	3	13	

'ALS580 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS580		SN74ALS580		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$	3	21	3	18	ns
t_{PHL}			3	15	3	14	
t_{PLH}	C	$\overline{Q}$	8	29	8	22	ns
t_{PHL}			8	22	8	21	
t_{PZH}	$\overline{OC}$	$\overline{Q}$	4	21	4	18	ns
t_{PZL}			4	21	4	18	
t_{PHZ}	$\overline{OC}$	$\overline{Q}$	2	10	2	8	ns
t_{PLZ}			3	15	3	13	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS573, SN54AS580 . . . . . −55 °C to 125 °C
SN74AS573, SN74AS580 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS573 SN54AS580			SN74AS573 SN74AS580			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−12	mA
							−15†	
I_{OL}	Low-level output current			32			32	mA
							48†	
t_w	Pulse duration, enable C high							ns
t_{su}	Setup time, data before enable C†							ns
t_h	Hold time, data after enable C†							ns
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS573 SN54AS580			SN74AS573 SN74AS580			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2		2.4	3.2		V
		V_{CC} = 4.75 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5		0.25	0.5	V
		V_{CC} = 4.75 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V							mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V							μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V							mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS573	V_{CC} = 5.5 V	Outputs high							mA
			Outputs low							
			Outputs disabled		65			65		
	'AS580		Outputs high							
			Outputs low							
			Outputs disabled		71			71		

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

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'AS573 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			'AS573			SN54AS573			SN74AS573			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	D	Q					4.5			4.5		ns
t_{PHL}							4			4		
t_{PLH}	C	Q					7			7		ns
t_{PHL}							5			5		
t_{PZH}	$\overline{OC}$	Q					3.5			3.5		ns
t_{PZL}							5			5		
t_{PHZ}	$\overline{OC}$	Q					3.5			3.5		ns
t_{PLZ}							5.5			5.5		

'AS580 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			'AS580			SN54AS580			SN74AS580			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	D	$\overline{Q}$					5.5			5.5		ns
t_{PHL}							4			4		
t_{PLH}	C	$\overline{Q}$					7			7		ns
t_{PHL}							5			5		
t_{PZH}	$\overline{OC}$	$\overline{Q}$					3.5			3.5		ns
t_{PZL}							5			5		
t_{PHZ}	$\overline{OC}$	$\overline{Q}$					3.5			3.5		ns
t_{PLZ}							5.5			5.5		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

D2661, JUNE 1982

- 3-State Buffer-Type Noninverting Outputs Drive Bus-Lines Directly
- Bus-Structured Pinout
- Buffered Control Inputs
- 'ALS575 and 'AS575 Have Synchronous Clear
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit registers feature three-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight edge-triggered D-type flip-flops enter data on the low-to-high transition of the clock. The 'ALS575 and 'AS575 may be synchronously cleared by taking the CLR input low.

The output-control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS' and SN54AS' devices are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS' and SN74AS' devices are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLES

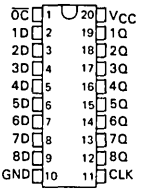
'ALS574, 'AS574
(EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

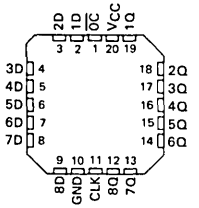
'ALS575, 'AS575
(EACH FLIP-FLOP)

INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	CLK	D	Q
L	L	↑	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q_0
H	X	X	X	Z

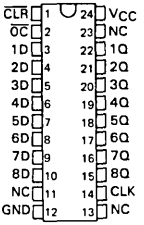
SN54ALS574, SN54AS574 . . . J PACKAGE
SN74ALS574, SN74AS574 . . . N PACKAGE
(TOP VIEW)



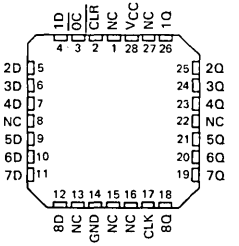
SN54ALS574, SN54AS574 . . . FH PACKAGE
SN74ALS574, SN74AS574 . . . FN PACKAGE
(TOP VIEW)



SN54ALS575, SN54AS575 . . . JT PACKAGE
SN74ALS575, SN74AS575 . . . NT PACKAGE
(TOP VIEW)



SN54ALS575, SN54AS575 . . . FH PACKAGE
SN74ALS575, SN74AS575 . . . FN PACKAGE



NC — No internal connection

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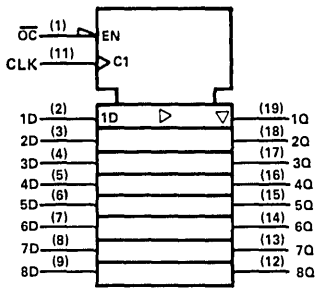
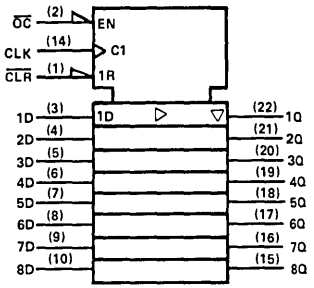
logic symbols

'ALS574, 'AS574

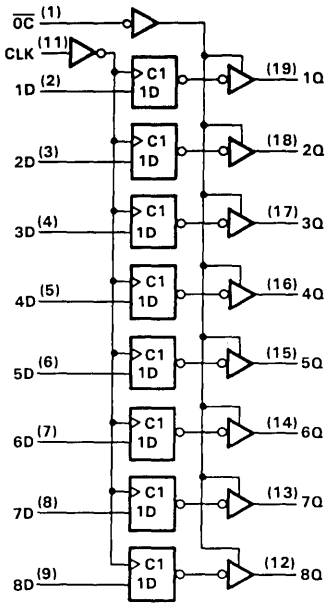


'ALS575, 'AS575



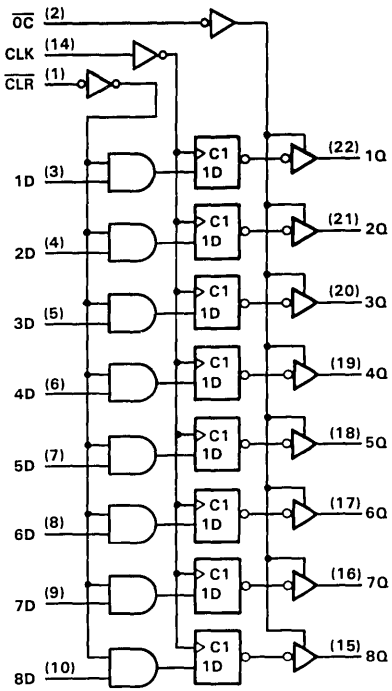
logic diagrams (positive logic)

'ALS574, 'AS574



Pin numbers shown are for J and N packages.

'ALS575, 'AS575



Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS574, SN54ALS575 . . . . . −55°C to 125°C
SN74ALS574, SN74ALS575 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

2

recommended operating conditions

				SN54ALS574 SN54ALS575			SN74ALS574 SN74ALS575			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
I_{OH}	High-level output current					−1				mA
									−2.6	
I_{OL}	Low-level output current					12				mA
									24	
f_{clock}	Clock frequency			0		30	0		35	MHz
t_w	Pulse duration	CLK high		16.5			14			ns
		CLK low		16.5			14			
t_{su}	Setup time before CLK↑	Data		15			15			ns
		'ALS575	$\overline{CLR}$ high	20			20			
			$\overline{CLR}$ low	15			15			
t_h	Hold time after CLK↑	Data		4			0			ns
		'ALS575	$\overline{CLR}$	0			0			
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS574 SN54ALS575			SN74ALS574 SN74ALS575			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		10	17		10	17	mA
		Outputs low		15	24		15	24	
		Outputs disabled		16	27		16	27	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

switching characteristics (see note 1)

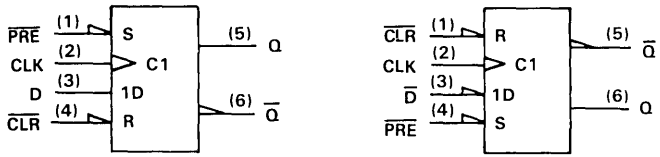
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS574 SN54ALS575		SN74ALS574 SN74ALS575		
			MIN	MAX	MIN	MAX	
f_{max}			30		35		MHz
t_{PLH}	CLK	Any Q	4	15	4	14	ns
t_{PHL}			4	15	4	14	
t_{PZH}	$\overline{OC}$	Any Q	4	21	4	18	ns
t_{PZL}			4	21	4	18	
t_{PHZ}	$\overline{OC}$	Any Q	2	10	2	8	ns
t_{PLZ}			3	15	3	13	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D flip-flop signal conventions

It is TI practice to name the outputs and other inputs of a D-type flip-flop and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.



Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (▷) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input D, but now both are considered active-low.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS574, SN54AS575 . . . . . −55 °C to 125 °C
SN74AS574, SN74AS575 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

2

recommended operating conditions

				SN54AS574 SN54AS575			SN74AS574 SN74AS575			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
I_{OH}	High-level output current					−12			−12	mA
									−15†	
I_{OL}	Low-level output current					32			32	mA
									48†	
f_{clock}	Clock frequency									MHz
t_w	Pulse duration	CLK high								ns
		CLK low								
t_{su}	Setup time before CLK↑	Data								ns
		'AS575	$\overline{CLR}$ high							
			$\overline{CLR}$ low							
t_h	Hold time after CLK↑	Data								ns
		$\overline{CLR}$								
T_A	Operating free-air temperature			−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS574 SN54AS575			SN74AS574 SN74AS575			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2		2.4	3.2		V
	V_{CC} = 4.75 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5		0.25	0.5	V
	V_{CC} = 4.75 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V							mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V							μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V							mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high							mA
		Outputs low							
		Outputs disabled		84			84		

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
Additional information on these products can be obtained from the factory as it becomes available.

682

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			'AS574 'AS575			SN54AS574 SN54AS575			SN74AS574 SN74AS575			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}							160			160		MHz
t_{PLH}	CLK	Any Q					5.5			5.5		ns
t_{PHL}							6			6		
t_{PZH}	$\overline{OC}$	Any Q					3.5			3.5		ns
t_{PZL}							5			5		
t_{PHZ}	$\overline{OC}$	Any Q					3.5			3.5		ns
t_{PLZ}							5.5			5.5		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TYPES SN54ALS576, SN54ALS577, SN54AS576, SN54AS577
SN74ALS576, SN74ALS577, SN74AS576, SN74AS577
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982

- 3-State Buffer-Type Inverting Outputs Drive Bus-Lines Directly
- Bus-Structured Pinout
- Buffered Control Inputs
- 'ALS577 and 'AS577 Have Synchronous Clear
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit registers feature three-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight-bit edge-triggered D-type flip-flops enter data on the low-to-high transition of the clock.

The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN54ALS' and SN54AS' devices are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS' and SN74AS' devices are characterized for operation from 0°C to 70°C.

FUNCTION TABLES

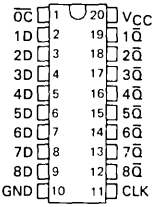
ALS576, AS576
(Each Flip-Flop)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

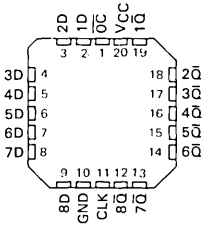
ALS577, AS577
(Each Flip-Flop)

INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	CLK	D	$\overline{Q}$
L	L	↑	X	H
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	$\overline{Q}_0$
H	X	X	X	Z

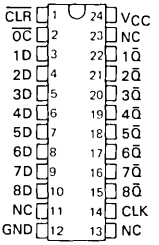
SN54ALS576, SN54AS576 . . . J PACKAGE
SN74ALS576, SN74AS576 . . . N PACKAGE
(TOP VIEW)



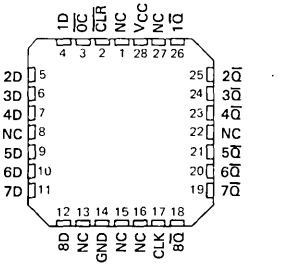
SN54ALS576, SN54AS576 . . . FH PACKAGE
SN74ALS576, SN74AS576 . . . FN PACKAGE
(TOP VIEW)



SN54ALS577, SN54AS577 . . . JT PACKAGE
SN74ALS577, SN74AS577 . . . NT PACKAGE
(TOP VIEW)



SN54ALS577, SN54AS577 . . . FH PACKAGE
SN74ALS577, SN74AS577 . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

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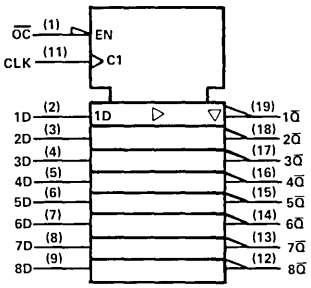
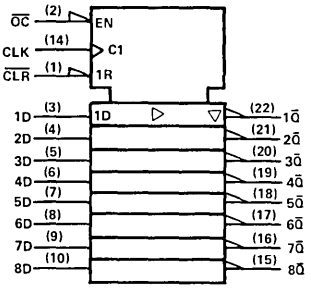
logic symbols

'ALS576, 'AS576

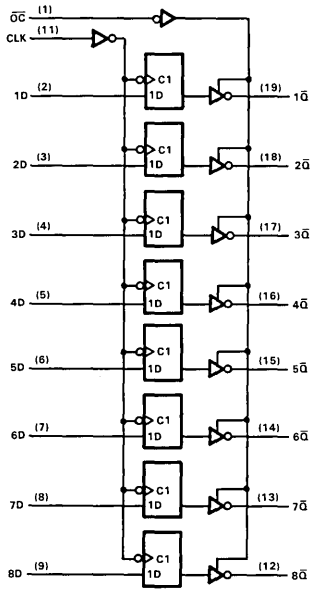


'ALS577, 'AS577



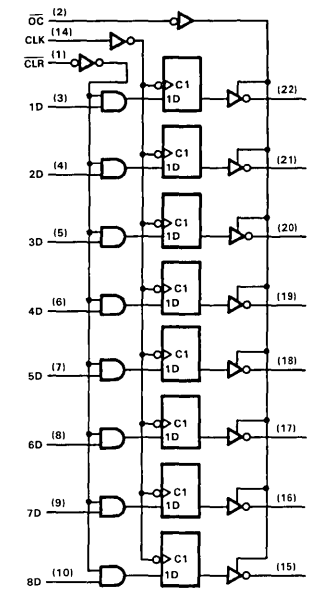
logic diagrams (positive logic)

'ALS576, 'AS576



Pin numbers shown are for J and N packages.

'ALS577, 'AS577



Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS', SN54AS' . . . . . −55 °C to 125 °C
SN74ALS', SN74AS' . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS576 SN54ALS577			SN74ALS576 SN74ALS577			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency		0		30	0		35	MHz
t_w	Pulse duration	CLK high	16.5			14			ns
		CLK low	16.5			14			
t_{su}	Setup time before CLK↑	Data	15			15			ns
		$\overline{CLR}$ ('ALS577)	15			15			
t_h	Hold time after CLK↑	Data	4			0			ns
		$\overline{CLR}$ ('ALS577)	4			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS576 SN54ALS577			SN74ALS576 SN74ALS577			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4				V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		10	17		10	17	mA
		Outputs low		15	24		15	24	
		Outputs disabled		16	27		16	27	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

TEXAS INSTRUMENTS
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POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS576 SN54ALS577		SN74ALS576 SN74ALS577		
			MIN	MAX	MIN	MAX	
f_{max}			30		35		MHz
t_{PLH}	CLK	Any Q or $\overline{Q}$	4	15	4	14	ns
t_{PHL}			4	15	4	14	
t_{PZH}	$\overline{OC}$	Any Q or $\overline{Q}$	4	21	4	18	ns
t_{PZL}			4	21	4	18	
t_{PHZ}	$\overline{OC}$	Any Q or $\overline{Q}$	2	10	2	8	ns
t_{PLZ}			3	15	3	13	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

recommended operating conditions

			SN54AS576 SN54AS577			SN74AS576 SN74AS577			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−12	mA
								−15†	
I_{OL}	Low-level output current				32			32	mA
								48†	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	CLK high							ns
		CLK low							
t_{su}	Setup time before CLK↑	Data							ns
		$\overline{CLR}$ ('AS577)							
t_h	Hold time after CLK↑	Data							ns
		$\overline{CLR}$ ('AS577)							
T_A	Operating free-air temperature		−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS576 SN54AS577			SN74AS576 SN74AS577			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2		2.4	3.2		V
	V_{CC} = 4.75 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5		0.25	0.5	V
	V_{CC} = 4.75 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V							μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V							μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V							mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V							μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V							mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high							mA
		Outputs low							
		Outputs disabled		84			84		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

TEXAS INSTRUMENTS
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switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX					UNIT
			'AS576 'AS577	SN54AS576 SN54AS577			SN74AS576 SN74AS577		
			TYP‡	MIN	TYP‡	MAX	MIN	TYP‡	MAX
f_{max}				160			160		MHz
t_{PLH}	CLK	Any Q or $\overline{Q}$		5.5			5.5		ns
t_{PHL}				6			6		
t_{PZH}	$\overline{OC}$	Any Q or $\overline{Q}$		3.5			3.5		ns
t_{PZL}				5			5		
t_{PHZ}	$\overline{OC}$	Any Q or $\overline{Q}$		3.5			3.5		ns
t_{PLZ}				5.5			5.5		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TYPES SN54ALS573, SN54ALS580, SN54AS573, SN54AS580
SN74ALS573, SN74ALS580, SN74AS573, SN74AS580
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982

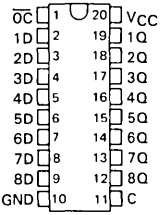
- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Choice of True or Inverting Logic**

  'ALS573, 'AS573 — True Outputs
  'ALS580, 'AS580 — Inverting Outputs

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

For complete information on the SN54ALS580 and the SN74ALS580, see page 2-288.

SN54ALS573, SN54AS573 . . . J PACKAGE
SN74ALS573, SN74AS573 . . . N PACKAGE
(TOP VIEW)



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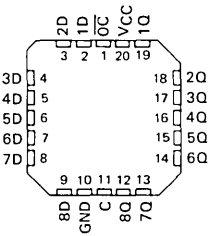
SN74ALS573, SN74AS573 . . . FN PACKAGE
(TOP VIEW)



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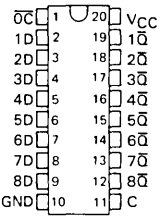
SN74ALS580, SN74AS580 . . . N PACKAGE
(TOP VIEW)



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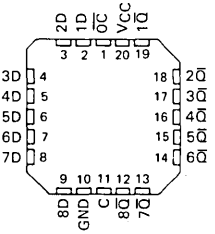
SN74ALS580, SN74AS580 . . . FN PACKAGE
(TOP VIEW)



TEXAS INSTRUMENTS
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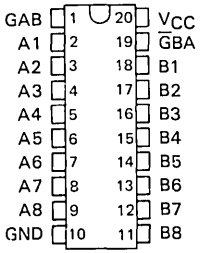
D2661, DECEMBER 1982

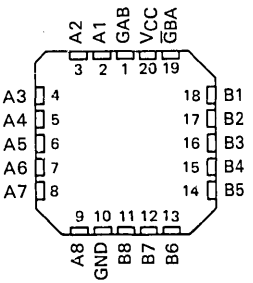
- **Bus Transceivers in High-Density 20-Pin DIP and the New Plastic and Ceramic Chip Carriers**
- **Local Bus-Latch Capability**
- **Choice of True or Inverting Logic**
- **Choice of 3-State or Open-Collector Outputs**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	OUTPUT	LOGIC
'ALS620	3-State	Inverting
'ALS621	Open-Collector	True
'ALS622	Open-Collector	Inverting
'ALS623	3-State	True

SN54ALS' . . . J PACKAGE
SN74ALS' . . . N PACKAGE
(TOP VIEW)



SN54ALS' . . . FH PACKAGE
SN74ALS' . . . FN PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 'ALS620 thru 'ALS623 the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the 'ALS621 and 'ALS623 or complementary for the 'ALS620 and 'ALS622.

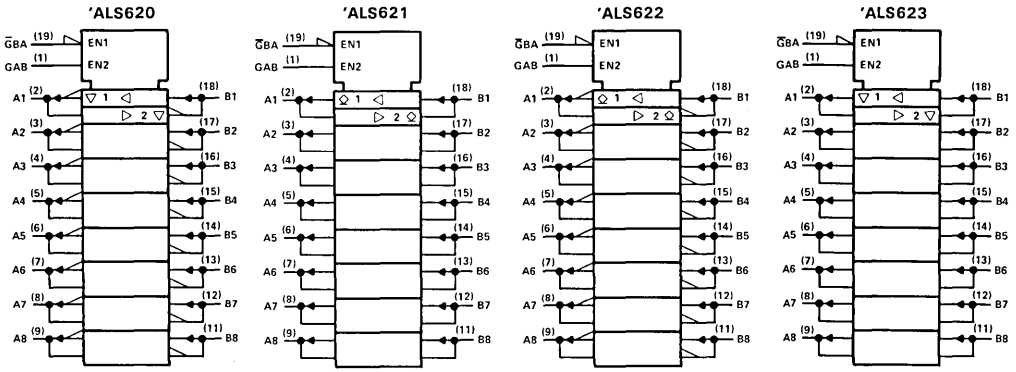
The -1 versions of the SN74ALS' parts are identical to their standard versions except that the recommended maximum I_{OL} is increased to 48 mA. There are no -1 versions of the SN54ALS' parts.

The SN54ALS620 thru SN54ALS623 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS620 thru SN74ALS623 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE

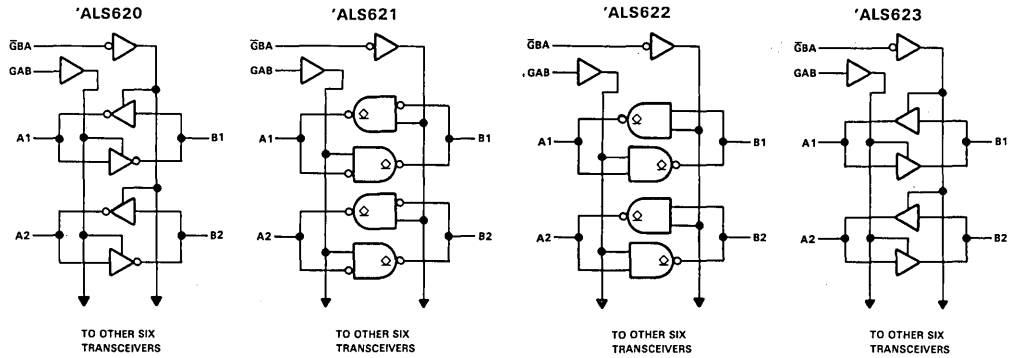
ENABLE INPUTS		OPERATION	
$\overline{G}$BA	GAB	'ALS620, 'ALS622	'ALS621, 'ALS623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Isolation	Isolation
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus	B data to A bus, A data to B bus

logic symbols



Pin numbers shown are for J and N packages.

logic diagrams (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS620, SN54ALS623 . . . . . −55 °C to 125 °C
SN74ALS620, SN74ALS623 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS620 SN54ALS623			SN74ALS620 SN74ALS623			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12				mA
							−15†	
I_{OL}	Low-level output current			12				mA
							24†	
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS620-1 and SN74ALS623-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS620 SN54ALS623			SN74ALS620 SN74ALS623			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for -1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports▲					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports▲					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS620	V_{CC} = 5.5 V	Outputs high		18	36		18	30	mA
			Outputs low		25	49		25	41	
			Outputs disabled		27	52		27	43	
	'ALS623	V_{CC} = 5.5 V	Outputs high		27	44		27	40	
			Outputs low		32	53		32	48	
			Outputs disabled		37	57		37	53	

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
▲For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

'ALS620 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS620			SN74ALS620			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	B	2		15	2		12	ns
t_{PHL}			2		15	2		12	
t_{PLH}	B	A	2		15	2		12	ns
t_{PHL}			2		15	2		12	
t_{PZH}	$\overline{G}$BA	A	5		24	5		20	ns
t_{PZL}			8		30	8		25	
t_{PHZ}	$\overline{G}$BA	A	5		24	5		20	ns
t_{PLZ}			8		30	8		25	
t_{PZH}	GAB	B	2		20	2		17	ns
t_{PZL}			8		40	8		34	
t_{PHZ}	GAB	B	2		20	2		17	ns
t_{PLZ}			8		40	8		34	

'ALS623 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS623		SN74ALS623		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	3	15	3	13	ns
t_{PHL}			3	13	3	11	
t_{PLH}	B	A	3	15	3	13	ns
t_{PHL}			3	13	3	11	
t_{PZH}	$\overline{G}$BA	A	7	25	7	22	ns
t_{PZL}			7	25	7	22	
t_{PHZ}	$\overline{G}$BA	A	2	25	2	21	ns
t_{PLZ}			3	30	3	26	
t_{PZH}	GAB	B	7	25	7	22	ns
t_{PZL}			7	25	7	22	
t_{PHZ}	GAB	B	2	25	2	21	ns
t_{PLZ}			3	30	3	26	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All Inputs and I/O ports . . . . . 7 V
Operating free-air temperature range: SN54ALS621, SN54ALS622 . . . . . −55 °C to 125 °C
SN74ALS621, SN74ALS622 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS621 SN54ALS622			SN74ALS621 SN74ALS622			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12				mA
							24	
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS621-1 and SN74ALS622-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS621 SN54ALS622			SN74ALS621 SN74ALS622			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.5			−1.5	V
I_{OH}		V_{CC} = 4.5 V, V_{OH} = 5.5 V				0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 12 mA			0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, I_{OL} = 24 mA (I_{OL} = 48 mA for -1 versions)						0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V, V_I = 7 V				0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V, V_I = 5.5 V				0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V, V_I = 2.7 V				20			20	μA
	A or B ports▲					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V, V_I = 0.4 V				−0.1			−0.1	mA
	A or B ports▲					−0.1			−0.1	
I_{CC}	'ALS621	V_{CC} = 5.5 V	Outputs high		24	40		24	37	mA
			Outputs low		30	50		30	45	
	'ALS622	V_{CC} = 5.5 V	Outputs high		9	15		9	13	
			Outputs low		16	28		16	25	

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
▲For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

'ALS621 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS621		SN74ALS621		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	10	45	10	33	ns
t_{PHL}			5	24	5	20	
t_{PLH}	B	A	10	45	10	33	ns
t_{PHL}			5	24	5	20	
t_{PLH}	$\overline{G}$BA	A	15	55	15	45	ns
t_{PHL}			12	40	12	35	
t_{PLH}	GAB	B	15	55	15	45	ns
t_{PHL}			12	40	12	35	

'ALS622 switching characteristics (see note 1)

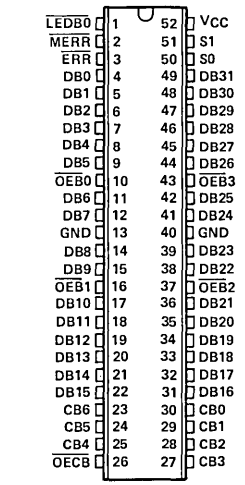
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS622		SN74ALS622		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	15	45	15	38	ns
t_{PHL}			5	23	5	19	
t_{PLH}	B	A	15	45	15	38	ns
t_{PHL}			5	23	5	19	
t_{PLH}	$\overline{G}$BA	A	15	45	15	40	ns
t_{PHL}			12	40	12	35	
t_{PLH}	GAB	B	15	50	15	45	ns
t_{PHL}			12	40	12	35	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

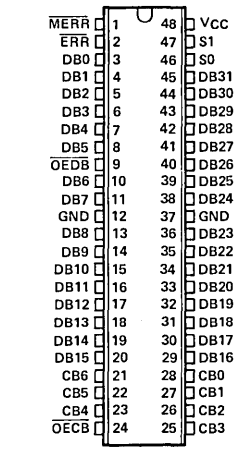
- Detects and Corrects Single-Bit Errors
- Detects and Flags Dual-Bit Errors
- Built-In Diagnostic Capability
- Fast Write and Read Cycle Processing Times
- Byte-Write Capability . . . 'ALS632 and 'ALS633
- Dependable Texas Instruments Quality and Reliability

DEVICE	PACKAGE	BYTE-WRITE	OUTPUT
'ALS632	52-pin	yes	3-State
'ALS633	52-pin	yes	Open-Collector
'ALS634	48-pin	no	3-State
'ALS635	48-pin	no	Open-Collector

'ALS632, 'ALS633, . . . JD PACKAGE
(TOP VIEW)



'ALS634, 'ALS635 . . . . JD PACKAGE
(TOP VIEW)



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CONTACT THE FACTORY

description

The 'ALS632 through 'ALS635 devices are 32-bit parallel error detection and correction circuits (EDACs) in 52-pin ('ALS632 and 'ALS633) or 48-pin ('ALS634 and 'ALS635), 600-mil packages. The EDACs use a modified Hamming code to generate a 7-bit check word from a 32-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 39-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

Single-bit errors in the 32-bit data word are flagged and corrected.

Single-bit errors in the 7-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 32-bit data word is not in error. The correction cycle will simply pass along the original 32-bit data word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These errors may occur in any two bits of the 39-bit word from memory (two errors in the 32-bit data word, two errors in the 7-bit check word, or one error in each word). The gross-error condition of all lows or all highs from memory will be detected. Otherwise, errors in three or more bits of the 39-bit word are beyond the capabilities of these devices to detect.

Read-modify-write (byte-control) operations can be performed with the 'ALS632 and 'ALS633 EDACs by using output latch enable, $\overline{\text{LEDBO}}$, and the individual $\overline{\text{OEB0}}$ thru $\overline{\text{OEB3}}$ byte control pins.

Diagnostics are performed on the EDACs by controls and internal paths that allow the user to read the contents of the DB and CB input latches. These will determine if the failure occurred in memory or in the EDAC.

PRODUCT PREVIEW

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TABLE 1 — WRITE CONTROL FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB CONTROL $\overline{OEB}$n OR $\overline{OEDB}$	DB OUTPUT LATCH ('ALS632,'ALS633) $\overline{LEDBO}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$
Write	Generate check word	L	L	Input	H	X	Output check bits†	L	H	H

†See Table 2 for details on check bit generation.

2

memory write cycle details

During a memory write cycle, the check bits (CB0 thru CB6) are generated internally in the EDAC by seven 16-input parity generators using the 32-bit data word as defined in Table 2. These seven check bits are stored in memory along with the original 32-bit data word. This 32-bit word will later be used in the memory read cycle for error detection and correction.

TABLE 2 — PARITY ALGORITHM

CHECK WORD BIT	32-BIT DATA WORD																													
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CB0	X		X	X		X					X		X	X	X			X			X		X	X	X	X		X				X
CB1				X		X		X		X		X		X	X	X				X		X		X		X		X		X	X	X
CB2	X		X			X	X		X			X	X			X	X		X			X	X		X			X	X			X
CB3			X	X	X				X	X	X				X	X			X	X	X				X	X	X				X	X
CB4	X	X							X	X	X	X	X	X			X	X							X	X	X	X	X	X		
CB5	X	X	X	X	X	X	X	X									X	X	X	X	X	X	X	X								
CB6	X	X	X	X	X	X	X	X																	X	X	X	X	X	X	X	X

The seven check bits are parity bits derived from the matrix of data bits as indicated by "X" for each bit.

error detection and correction details

During a memory read cycle, the 7-bit check word is retrieved along with the actual data. In order to be able to determine whether the data from memory is acceptable to use as presented to the bus, the error flags must be tested to determine if they are at the high level.

The first case in Table 3 represents the normal, no-error conditions. The EDAC presents highs on both flags. The next two cases of single-bit errors give a high on $\overline{MERR}$ and a low on $\overline{ERR}$, which is the signal for a correctable error, and the EDAC should be sent through the correction cycle. The last three cases of double-bit errors will cause the EDAC to signal lows on both $\overline{ERR}$ and $\overline{MERR}$, which is the interrupt indication for the CPU.

TABLE 3 — ERROR FUNCTION

Total Number of Errors		Error Flags		Data Correction
32-Bit Data Word	7-Bit Check Word	$\overline{ERR}$	$\overline{MERR}$	
0	0	H	H	Not applicable
1	0	L	H	Correction
0	1	L	H	Correction
1	1	L	L	Interrupt
2	0	L	L	Interrupt
0	2	L	L	Interrupt

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Error detection is accomplished as the 7-bit check word and the 32-bit data word from memory are applied to internal parity generators/checkers. If the parity of all seven groupings of data and check bits are correct, it is assumed that no error has occurred and both error flags will be high.

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set low. Any single error in the 32-bit data word will change the state of either three or five bits of the 7-bit check word. Any single error in the 7-bit check word changes the state of only that one bit. In either case, the single error flag ($\overline{ERR}$) will be set low while the dual error flag ($\overline{MERR}$) will remain high.

Any two-bit error will change the state of an even number of check bits. The two-bit error is not correctable since the parity tree can only identify single-bit errors. Both error flags are set low when any two-bit error is detected.

Three or more simultaneous bit errors can cause the EDAC to believe that no error, a correctable error, or an uncorrectable error has occurred and will produce erroneous results in all three cases. It should be noted that the gross-error conditions of all lows and all highs will be detected.

TABLE 4 — READ, FLAG, AND CORRECT FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB CONTROL $\overline{OEBn}$ OR $\overline{OEDB}$	DB OUTPUT LATCH ('ALS632,'ALS633) $\overline{LEDBO}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$ $\overline{MERR}$
Read	Read & flag	H	L	Input	H	X	Input	H	Enabled†
Read	Latch input data & check bits	H	H	Latched input data	H	L	Latched input check word	H	Enabled†
Read	Output corrected data & syndrome bits	H	H	Output corrected data word	L	X	Output syndrome bits‡	L	Enabled†

†See Table 3 for error description.
‡See Table 5 for error location.

As the corrected word is made available on the data I/O port (DB0 thru DB31), the check word I/O port (CB0 thru CB6) presents a 7-bit syndrome error code. This syndrome error code can be used to locate the bad memory chip. See Table 5 for syndrome decoding.

TABLE 5 — SYNDROME DECODING

SYNDROME BITS 6	5	4	3	2	1	0	ERROR
L	L	L	L	L	L	L	unc
L	L	L	L	L	L	H	2-bit
L	L	L	L	L	H	L	2-bit
L	L	L	L	L	H	H	unc
L	L	L	L	H	L	L	2-bit
L	L	L	L	H	L	H	unc
L	L	L	L	H	H	L	unc
L	L	L	L	H	H	H	2-bit
L	L	L	H	L	L	L	2-bit
L	L	L	H	L	L	H	unc
L	L	L	H	L	H	L	DB31
L	L	L	H	L	H	H	2-bit
L	L	L	H	H	L	L	unc
L	L	L	H	H	L	H	2-bit
L	L	L	H	H	H	L	2-bit
L	L	L	H	H	H	H	DB30
L	L	H	L	L	L	L	2-bit
L	L	H	L	L	L	H	unc
L	L	H	L	L	H	L	DB29
L	L	H	L	L	H	H	2-bit
L	L	H	L	H	L	L	DB28
L	L	H	L	H	L	H	2-bit
L	L	H	L	H	H	L	2-bit
L	L	H	L	H	H	H	DB27
L	L	H	H	L	L	L	DB26
L	L	H	H	L	L	H	2-bit
L	L	H	H	L	H	L	2-bit
L	L	H	H	L	H	H	DB25
L	L	H	H	H	L	L	2-bit
L	L	H	H	H	L	H	DB24
L	L	H	H	H	H	L	unc
L	L	H	H	H	H	H	2-bit

SYNDROME BITS 6	5	4	3	2	1	0	ERROR
L	H	L	L	L	L	L	2-bit
L	H	L	L	L	L	H	unc
L	H	L	L	L	H	L	DB7
L	H	L	L	L	H	H	2-bit
L	H	L	L	H	L	L	DB6
L	H	L	L	H	L	H	2-bit
L	H	L	L	H	H	L	2-bit
L	H	L	L	H	H	H	DB5
L	H	L	H	L	L	L	DB4
L	H	L	H	L	L	H	2-bit
L	H	L	H	L	H	L	2-bit
L	H	L	H	L	H	H	DB3
L	H	L	H	H	L	L	2-bit
L	H	L	H	H	L	H	DB2
L	H	L	H	H	H	L	unc
L	H	L	H	H	H	H	2-bit
L	H	H	L	L	L	L	DB0
L	H	H	L	L	L	H	2-bit
L	H	H	L	L	H	L	2-bit
L	H	H	L	L	H	H	unc
L	H	H	L	H	L	L	2-bit
L	H	H	L	H	L	H	DB31
L	H	H	L	H	H	L	unc
L	H	H	L	H	H	H	2-bit
L	H	H	H	L	L	L	2-bit
L	H	H	H	L	L	H	unc
L	H	H	H	L	H	L	unc
L	H	H	H	L	H	H	2-bit
L	H	H	H	H	L	L	unc
L	H	H	H	H	L	H	2-bit
L	H	H	H	H	H	L	2-bit
L	H	H	H	H	H	H	CB6

SYNDROME BITS 6	5	4	3	2	1	0	ERROR
H	L	L	L	L	L	L	2-bit
H	L	L	L	L	L	H	unc
H	L	L	L	L	H	L	unc
H	L	L	L	L	H	H	2-bit
H	L	L	L	H	L	L	unc
H	L	L	L	H	L	H	2-bit
H	L	L	L	H	H	L	2-bit
H	L	L	L	H	H	H	unc
H	L	L	H	L	L	L	unc
H	L	L	H	L	L	H	2-bit
H	L	L	H	L	H	L	2-bit
H	L	L	H	L	H	H	DB15
H	L	L	H	H	L	L	2-bit
H	L	L	H	H	L	H	unc
H	L	L	H	H	H	L	DB14
H	L	L	H	H	H	H	2-bit
H	L	H	L	L	L	L	unc
H	L	H	L	L	L	H	2-bit
H	L	H	L	L	H	L	2-bit
H	L	H	L	L	H	H	DB13
H	L	H	L	H	L	L	2-bit
H	L	H	L	H	L	H	DB12
H	L	H	L	H	H	L	DB11
H	L	H	L	H	H	H	2-bit
H	L	H	H	L	L	L	DB10
H	L	H	H	L	L	H	DB9
H	L	H	H	L	H	L	2-bit
H	L	H	H	L	H	H	DB8
H	L	H	H	H	L	L	2-bit
H	L	H	H	H	L	H	2-bit
H	L	H	H	H	H	L	2-bit
H	L	H	H	H	H	H	CB5

SYNDROME BITS 6	5	4	3	2	1	0	ERROR
H	H	L	L	L	L	L	unc
H	H	L	L	L	L	H	2-bit
H	H	L	L	L	H	L	2-bit
H	H	L	L	L	H	H	DB23
H	H	L	L	H	L	L	2-bit
H	H	L	L	H	L	H	DB22
H	H	L	L	H	H	L	DB21
H	H	L	L	H	H	H	2-bit
H	H	L	H	L	L	L	2-bit
H	H	L	H	L	L	H	DB20
H	H	L	H	L	H	L	DB19
H	H	L	H	L	H	H	2-bit
H	H	L	H	H	L	L	DB18
H	H	L	H	H	L	H	2-bit
H	H	L	H	H	H	L	2-bit
H	H	L	H	H	H	H	CB4
H	H	H	L	L	L	L	2-bit
H	H	H	L	L	L	H	DB16
H	H	H	L	L	H	L	unc
H	H	H	L	L	H	H	2-bit
H	H	H	L	H	L	L	DB17
H	H	H	L	H	L	H	2-bit
H	H	H	L	H	H	L	2-bit
H	H	H	L	H	H	H	CB3
H	H	H	H	L	L	L	unc
H	H	H	H	L	L	H	2-bit
H	H	H	H	L	H	L	2-bit
H	H	H	H	L	H	H	CB2
H	H	H	H	H	L	L	2-bit
H	H	H	H	H	L	H	CB1
H	H	H	H	H	H	L	CB0
H	H	H	H	H	H	H	none

CB X = error in check bit X
DB Y = error in data bit Y
2-bit = double-bit error
unc = uncorrectable multibit error

read-modify-write (byte control) operations

The 'ALS632 and 'ALS633 devices are capable of byte-write operations. The 39-bit word from memory must first be latched into the DB and CB input latches. This is easily accomplished by switching from the read and flag mode (S1 = H, S0 = L) to the latch input mode (S1 = H, S0 = H). The EDAC will then make any corrections, if necessary, to the data word and place it at the input of the output data latch. This data word must then be latched into the output data latch by taking $\overline{\text{LEDBO}}$ from a low to a high.

Byte control can now be employed on the data word through the $\overline{\text{OEB0}}$ through $\overline{\text{OEB3}}$ controls. $\overline{\text{OEB0}}$ controls DB0-DB7 (byte 0), $\overline{\text{OEB1}}$ controls DB8-DB15 (byte 1), $\overline{\text{OEB2}}$ controls DB16-DB23 (byte 2), and $\overline{\text{OEB3}}$ controls DB24-DB31 (byte 3). Placing a high on the byte control will disable the output and the user can modify the byte. If a low is placed on the byte control, then the original byte is allowed to pass onto the data bus unchanged. If the original data word is altered through byte control, a new check word must be generated before it is written back into memory. This is easily accomplished by taking control S1 and S0 low. Table 6 lists the read-modify-write functions.

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TABLE 6 — READ-MODIFY-WRITE FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S0	BYTEn†	$\overline{OEB}$n†	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL	ERROR FLAG $\overline{ERR}$	ERROR FLAG $\overline{MERR}$
Read	Read & Flag	H	L	Input	H	X	Input	H	Enabled	
Read	Latch input data & check bits	H	H	Latched Input data	H	L	Latched input check word	H	Enabled	
Read	Latch corrected data word into output latch	H	H	Latched output data word	H	H	Hi-Z	H	Enabled	
							Output Syndrome bits	L		
Modify /write	Modify appropriate byte or bytes & generate new check word	L	L	Input modified BYTE0	H	H	Output check word	L	H	H
				Output unchanged BYTE0	L					

†$\overline{OEB}$0 controls DB0-DB7 (BYTE0), $\overline{OEB}$1 controls DB8-DB15 (BYTE1), $\overline{OEB}$2 controls DB16-DB23 (BYTE2), $\overline{OEB}$3 controls DB24-DB31 (BYTE3).

diagnostic operations

The 'ALS632 thru 'ALS635 are capable of diagnostics that allow the user to determine whether the EDAC or the memory is failing. The diagnostic function tables will help the user to see the possibilities for diagnostic control.

In the diagnostic mode (S1 = L, S0 = H), the checkword is latched into the input latch while the data input latch remains transparent. This lets the user apply various data words against a fixed known checkword. If the user applies a diagnostic data word with an error in any bit location, the $\overline{ERR}$ flag should be low. If a diagnostic data word with two errors in any bit location is applied, the $\overline{MERR}$ flag should be low. After the checkword is latched into the input latch, it can be verified by taking $\overline{OECB}$ low. This outputs the latched checkword. With the 'ALS632 and 'ALS633, the diagnostic data word can be latched into the output data latch and verified. It should be noted that the 'ALS634 and 'ALS635 do not have this pass-through capability because they do not contain an output data latch. By changing from the diagnostic mode (S1 = L, S0 = H) to the correction mode (S1 = H, S0 = H), the user can verify that the EDAC will correct the diagnostic data word. Also, the syndrome bits can be produced to verify that the EDAC pinpoints the error location. Table 7 ('ALS632 and 'ALS633) and Table 8 ('ALS634 and 'ALS635) list the diagnostic functions.

TABLE 7 — 'ALS632, 'ALS633 DIAGNOSTIC FUNCTION

EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB BYTE CONTROL $\overline{OEBn}$	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$
Read & flag	H	L	Input correct data word	H	X	Input correct check bits	H	H	H
Latch input check word while data input latch remains transparent	L	H	Input diagnostic data word†	H	L	Latched input check bits	H	Enabled	
Latch diagnostic data word into output latch	L	H	Input diagnostic data word†	H	H	Output latched check bits	L	Enabled	
						Hi-Z	H		
Latch diagnostic data word into input latch	H	H	Latched input diagnostic data word	H	H	Output syndrome bits	L	Enabled	
						Hi-Z	H		
Output diagnostic data word & syndrome bits	H	H	Output diagnostic data word	L	H	Output syndrome bits	L	Enabled	
						Hi-Z	H		
Output corrected diagnostic data word & output syndrome bits	H	H	Output corrected diagnostic data word	L	L	Output syndrome bits	L	Enabled	
						Hi-Z	H		

†Diagnostic data is a data word with an error in one bit location except when testing the $\overline{MERR}$ error flag. In this case, the diagnostic data word will contain errors in two bit locations.

TABLE 8 — 'ALS634, 'ALS635 DIAGNOSTIC FUNCTION

EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB CONTROL $\overline{OEDB}$	CHECK I/O	DB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$
Read & flag	H	L	Input correct data word	H	Input correct check bits	H	H	H
Latch input check bits while data input latch remains transparent	L	H	Input diagnostic data word†	H	Latched input check bits	H	Enabled	
Output input check bits	L	H	Input diagnostic data word†	H	Output input check bits	H	Enabled	
Latch diagnostic data into input latch	H	H	Latched input diagnostic data word	H	Output syndrome bits	L	Enabled	
					Hi-Z	H		
Output corrected diagnostic data word	H	H	Output corrected diagnostic data word	L	Output syndrome bits	L	Enabled	
					Hi-Z	H		

†Diagnostic data is a data word with an error in one bit location except when testing the $\overline{MERR}$ error flag. In this case, the diagnostic data word will contain errors in two bit locations.

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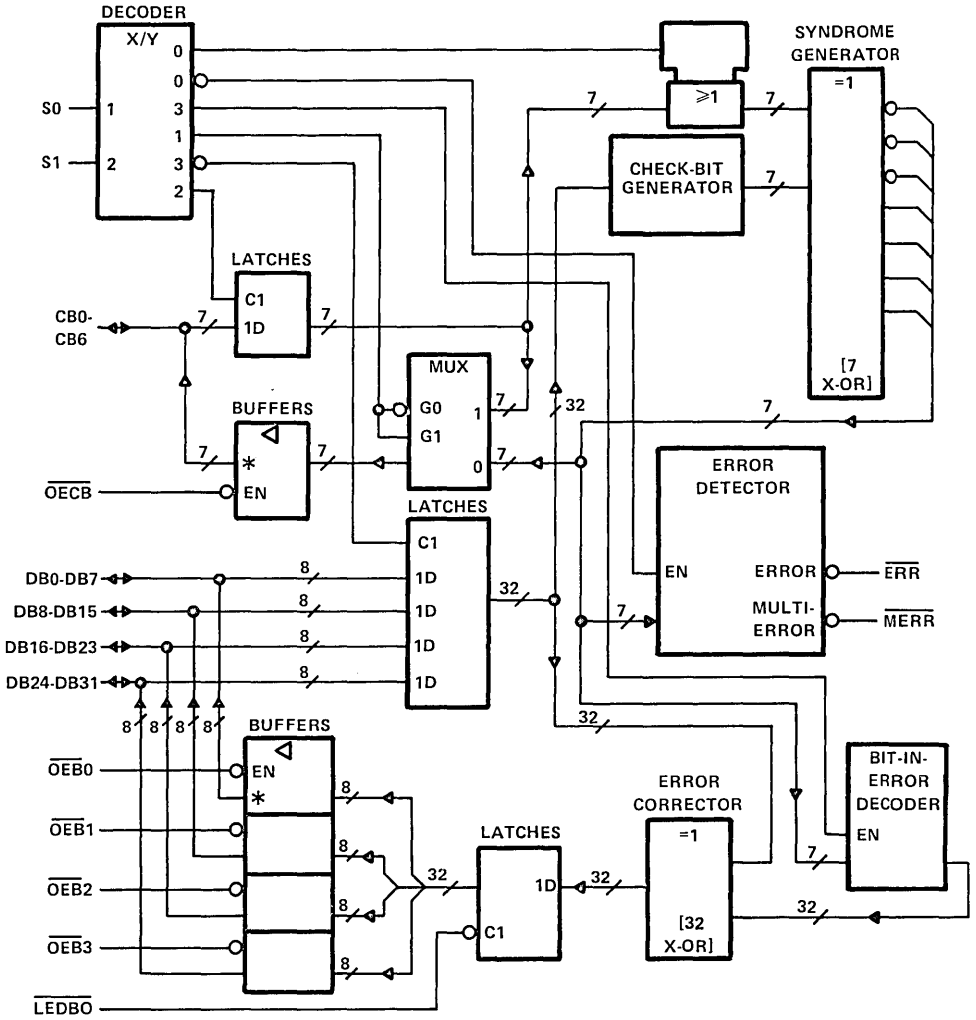
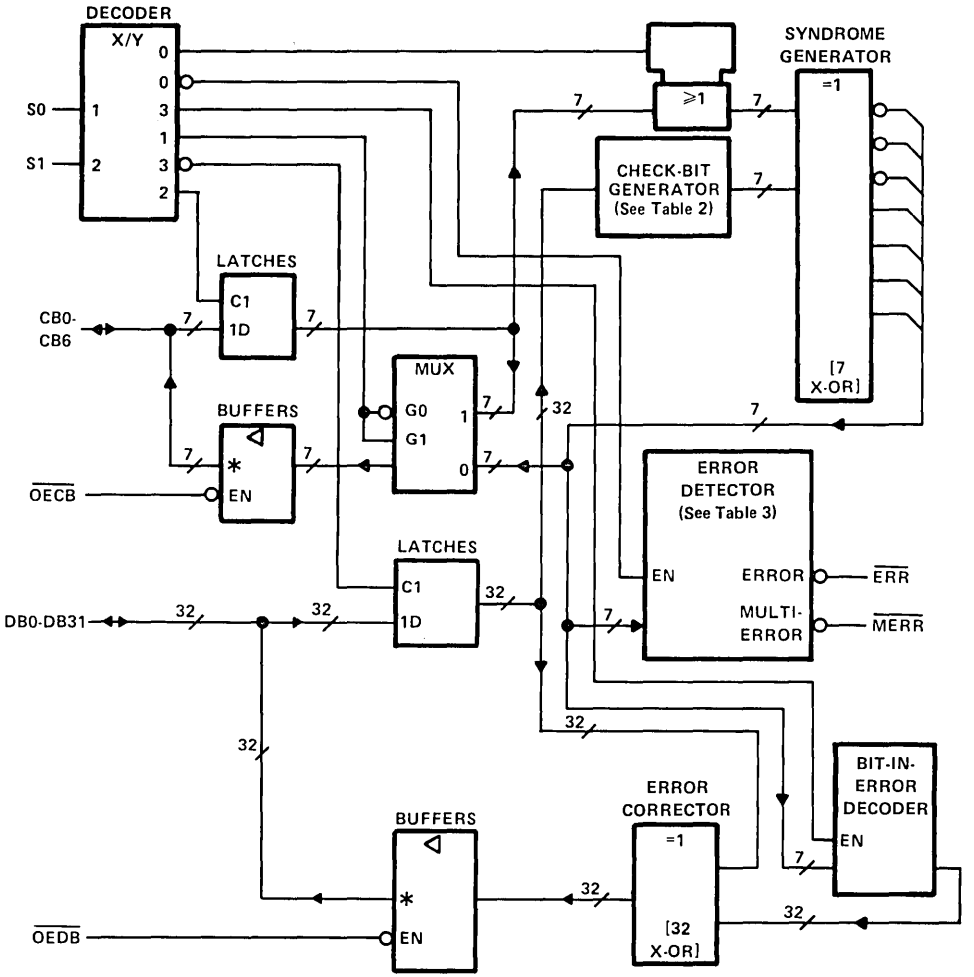
'ALS632, 'ALS633 logic diagram (positive logic)



* 'ALS632 has 3-state (▽) check-bit and data outputs.
'ALS633 has open-collector (◇) check-bit and data outputs.

'ALS634, 'ALS635 logic diagram (positive logic)



*'ALS634 has 3-state (▽) check-bit and data outputs.
'ALS635 has open-collector (◇) check-bit and data outputs.

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POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: CB and DB . . . . . 5.5 V
All others . . . . . 7 V
Operating free-air temperature range: SN54ALS632 thru SN54ALS635 . . . . . −55°C to 125°C
SN74ALS632 thru SN74ALS635 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS632 THRU SN54ALS635			SN74ALS632 THRU SN74ALS635			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	$\overline{ERR}$ or $\overline{MERR}$			−0.4			−0.4	mA
		DB or CB | 'ALS632, 'ALS634			−1			−2.6	
I_{OL}	Low-level output current	$\overline{ERR}$ or $\overline{MERR}$			4			8	mA
		DB or CB			12			24	
t_w	Pulse duration	$\overline{LEDBO}$ low							ns
t_{su}	Setup time	(1) Data and check word before S0↑ (S1 = H)							ns
		(2) S0 high before $\overline{LEDBO}$↑ (S1 = H)*							
		(3) $\overline{LEDBO}$ high before the earlier of S0↓ or S1↓*							
		(4) $\overline{LEDBO}$ high before S1↑ (S0 = H)							
		(5) Diagnostic data word before S1↑ (S0 = H)							
		(6) Diagnostic check word before the later of S1↓ or S0↑							
		(7) Diagnostic data word before $\overline{LEDBO}$ ↑ (S1 = L and S0 = H)†							
t_h	Hold time	(8) Read-mode, S0 low and S1 high							ns
		(9) Data and check word after S0↑ (S1 = H)							
		(10) Data word after S1↑ (S0 = H)							
		(11) Check word after the later of S1↓ or S0↑							
		(12) Diagnostic data word after $\overline{LEDBO}$↑ (S1 = L, S0 = H)†							
t_{corr}	Correction time (see Figure 1)								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

*These times ensure that corrected data is saved in the output data latch.
†These times ensure that the diagnostic data word is saved in the output data latch.

Additional information on these products can be obtained from the factory as it becomes available.

'ALS632, 'ALS634 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS632 SN54ALS634			SN74ALS632 SN74ALS634			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
	DB or CB	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
	DB or CB	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	S0 or S1	V_{CC} = 5.5 V,	V_I = 7 V							mA
	DB or CB	V_{CC} = 5.5 V,	V_I = 5.5 V							
I_{IH}	S0 or S1	V_{CC} = 5.5 V,	V_I = 2.7 V							μA
	DB or CB▲									
I_{IL}	S0 or S1	V_{CC} = 5.5 V,	V_I = 0.4 V							mA
	DB or CB▲									
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1							mA

'ALS633, 'ALS635 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS633 SN54ALS635			SN74ALS633 SN74ALS635			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
I_{OH}	DB or CB	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
	DB or CB	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	S0 or S1	V_{CC} = 5.5 V,	V_I = 7 V							mA
	DB or CB	V_{CC} = 5.5 V,	V_I = 5.5 V							
I_{IH}	S0 or S1	V_{CC} = 5.5 V,	V_I = 2.7 V							μA
	DB or CB▲									
I_{IL}	S0 or S1	V_{CC} = 5.5 V,	V_I = 0.4 V							mA
	DB or CB▲									
I_O§	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1							mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

▲For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

NOTE 1: I_{CC} is measured with S0 and S1 at 4.5 V and all CB and DB pins grounded.

Additional information on these products can be obtained from the factory as it becomes available.

TEXAS INSTRUMENTS
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'ALS632 switching characteristics, V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = MIN to MAX (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ALS632			SN74ALS632			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500 Ω							ns
	DB	$\overline{ERR}$	S1 = L, S0 = H, R_L = 500 Ω							
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500 Ω							ns
	DB	$\overline{MERR}$	S1 = L, S0 = H, R_L = 500 Ω							
t_{pd}	S0↓ and S1↓	CB	R1 = R2 = 500 Ω							ns
t_{pd}	DB	CB	S1 = L, S0 = L, R1 = R2 = 500 Ω							ns
t_{pd}	$\overline{LEDBO}$↓	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω							ns
t_{pd}	S1↑	CB	S0 = H, R1 = R2 = 500 Ω							ns
t_{en}	$\overline{OECB}$↓	CB	S0 = H, S1 = X, R1 = R2 = 500 Ω							ns
t_{dis}	$\overline{OECB}$↑	CB	S0 = H, S1 = X, R1 = R2 = 500 Ω							ns
t_{en}	$\overline{OEB0}$ thru $\overline{OEB3}$↓	DB	S0 = H, S1 = X, R1 = R2 = 500 Ω							ns
t_{dis}	$\overline{OEB0}$ thru $\overline{OEB3}$↑	DB	S0 = H, S1 = X, R1 = R2 = 500 Ω							ns

'ALS633 switching characteristics V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = MIN to MAX (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ALS633			SN74ALS633			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500 Ω							ns
	DB	$\overline{ERR}$	S1 = L, S0 = H, R_L = 500 Ω							
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500 Ω							ns
			S1 = L, S0 = H, R_L = 500 Ω							
t_{pd}	S0↓ and S1↓	CB	R_L = 680 Ω							ns
t_{pd}	DB	CB	S1 = L, S0 = L, R_L = 680 Ω							ns
t_{pd}	$\overline{LEDBO}$↓	DB	S1 = X, S0 = H, R_L = 680 Ω							ns
t_{pd}	S1↑	CB	S0 = H, R_L = 680 Ω							ns
t_{PLH}	$\overline{OECB}$↑	CB	S1 = X, S0 = H, R_L = 680 Ω							ns
t_{PHL}	$\overline{OECB}$↓	CB	S1 = X, S0 = H, R_L = 680 Ω							ns
t_{PLH}	$\overline{OEB0}$ thru $\overline{OEB3}$↑	DB	S1 = X, S0 = H, R_L = 680 Ω							ns
t_{PHL}	$\overline{OEB0}$ thru $\overline{OEB3}$↓	DB	S1 = X, S0 = H, R_L = 680 Ω							ns

Additional information on these products can be obtained from the factory as it becomes available.

'ALS634 switching characteristics, V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = MIN to MAX (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ALS634			SN74ALS634			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500 Ω							ns
			S1 = L, S0 = H, R_L = 500 Ω							
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500 Ω							ns
			S1 = L, S0 = H, R_L = 500 Ω							
t_{pd}	S0↓ and S1↓	CB	R1 = R2 = 500 Ω							ns
t_{pd}	DB	CB	S1 = L, S0 = L, R1 = R2 = 500 Ω							ns
t_{pd}	S1↑	CB	S0 = H, R1 = R2 = 500 Ω							ns
t_{en}	$\overline{OECB}$↓	CB	S1 = X, S0 = H, R1 = R2 = 500 Ω							ns
t_{dis}	$\overline{OECB}$↑	CB	S1 = X, S0 = H, R1 = R2 = 500 Ω							ns
t_{en}	$\overline{OECB}$↓	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω							ns
t_{dis}	$\overline{OECB}$↑	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω							ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

'ALS635 switching characteristics V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = MIN to MAX (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ALS635			SN74ALS635			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500 Ω							ns
	DB	$\overline{ERR}$	S1 = L, S0 = H, R_L = 500 Ω							
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500 Ω							ns
			S1 = L, S0 = H, R_L = 500 Ω							
t_{pd}	S0↓ and S1↓	CB	R_L = 680 Ω							ns
t_{pd}	DB	CB	S1 = L, S0 = L, R_L = 680 Ω							ns
t_{pd}	S1↑	DB	S0 = H, R_L = 680 Ω							ns
t_{PLH}	$\overline{OECB}$↑	CB	S1 = X, S0 = H, R_L = 680 Ω							ns
t_{PHL}	$\overline{OECB}$↓	CB	S1 = X, S0 = H, R_L = 680 Ω							ns
t_{PLH}	$\overline{OEDB}$↑	DB	S1 = X, S0 = H, R_L = 680 Ω							ns
t_{PHL}	$\overline{OEDB}$↓	DB	S1 = X, S0 = H, R_L = 680 Ω							ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

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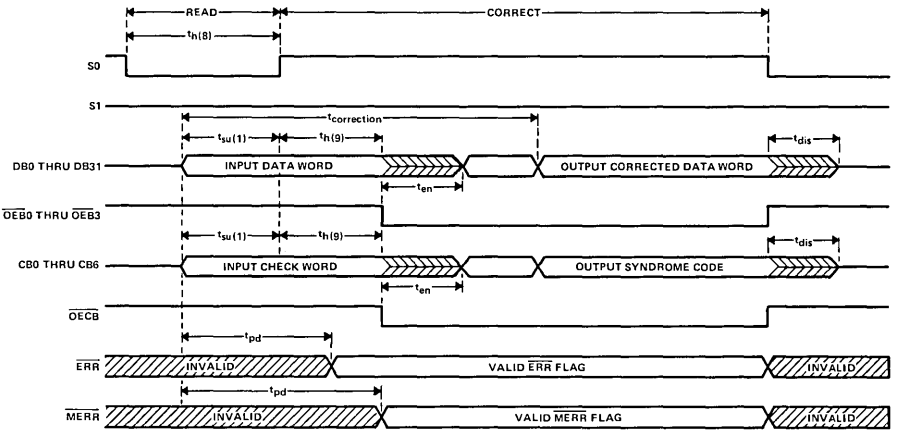

FIGURE 1–READ, FLAG, AND CORRECT MODE SWITCHING WAVEFORMS

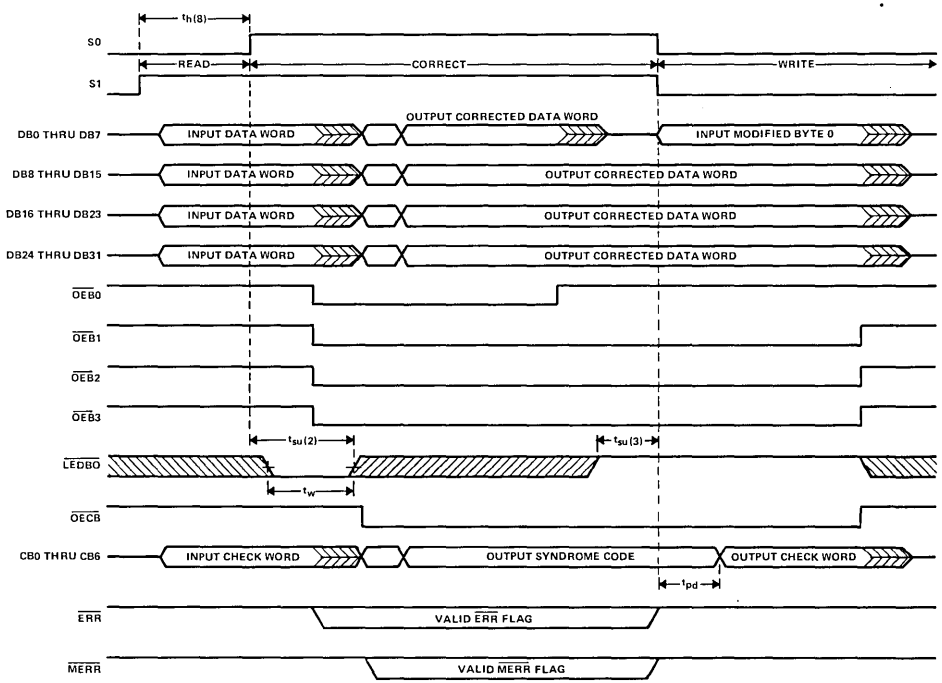

FIGURE 2–READ, CORRECT, MODIFY MODE SWITCHING WAVEFORMS

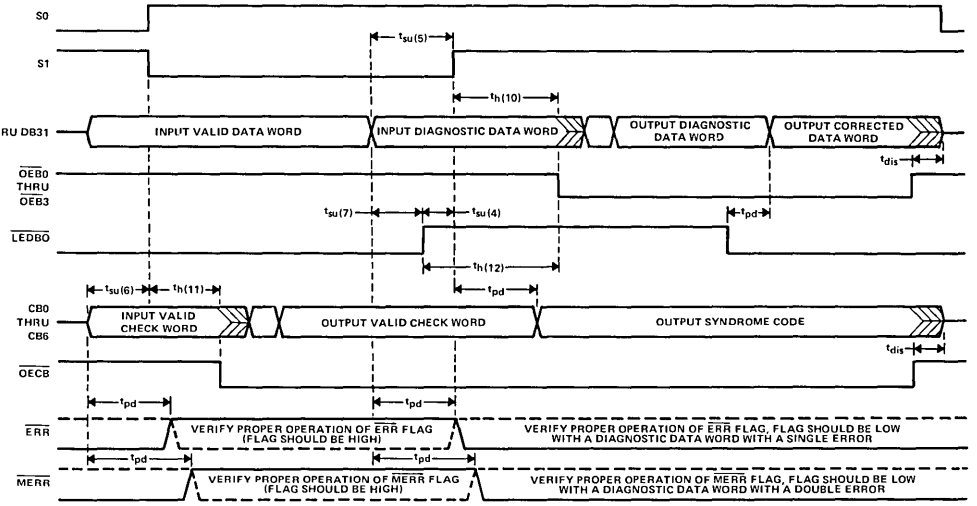

FIGURE 3–DIAGNOSTIC MODE SWITCHING WAVEFORM

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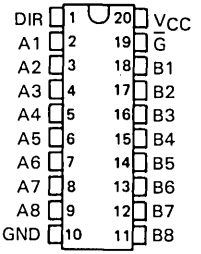
TYPES SN54ALS638, SN54ALS639, SN74ALS638, SN74ALS639
OCTAL BUS TRANSCEIVERS

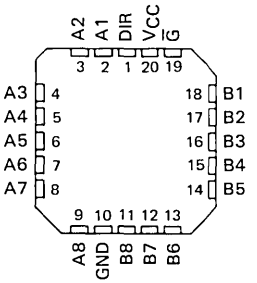
D2261, DECEMBER 1982

- Bidirectional Bus Transceivers in High-Density 20-Pin Packages
- Choice of True or Inverting Logic
- A Bus Outputs are Open-Collector; B Bus Outputs are 3-State
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPS
- Dependable Texas Instruments Quality and Reliability

SN54ALS638, SN54ALS639 . . . J PACKAGE
SN74ALS638, SN74ALS639 . . . N PACKAGE
(TOP VIEW)



SN54ALS638, SN54ALS639 . . . FH PACKAGE
SN74ALS638, SN74ALS639 . . . FN PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between open-collector and 3-state buses. The devices transmit data from the A bus (open-collector) to the B bus (3-state) or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so the buses are isolated.

DEVICE	A OUTPUT	B OUTPUT	LOGIC
'ALS638	Open-Collector	3-State	Inverting
'ALS639	Open-Collector	3-State	True

The -1 versions of the SN74ALS' parts are identical to the standard versions except that recommended maximum of I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS' parts.

The SN54ALS638 and SN54ALS639 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS638 and SN74ALS639 are characterized for operation from 0 °C to 70 °C.

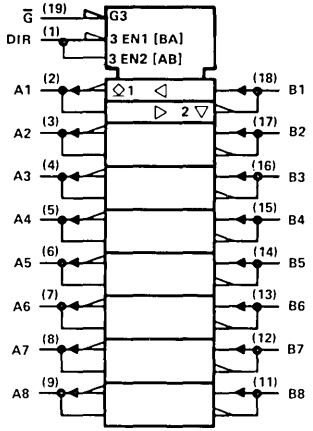
FUNCTION TABLE

CONTROL INPUTS		OPERATION	
$\overline{G}$	DIR	'ALS638	'ALS639
L	L	$\overline{B}$ data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus
H	X	Isolation	Isolation

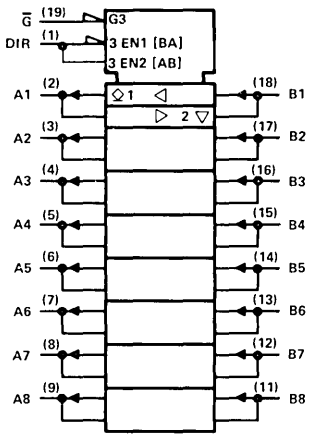
2

logic symbols

'ALS638

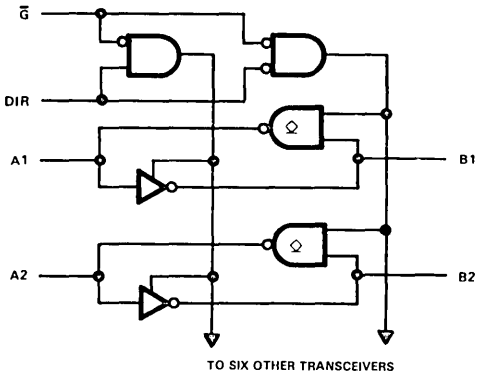


'ALS639

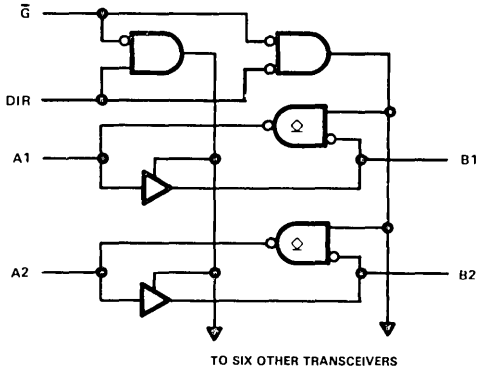


functional block diagrams (positive logic)

'ALS638



'ALS639



Pin numbers shown are for J and N packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
A bus I/O ports . . . . . 7 V
B bus I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS638, SN54ALS639 . . . . . −55°C to 125°C
SN74ALS638, SN74ALS639 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS638 SN54ALS639			SN74ALS638 SN74ALS639			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage	A ports			5.5			5.5	V
I_{OH}	High-level output current	B ports			−12				mA
								−15	
I_{OL}	Low-level output current	A or B ports			12				mA
								24	
								48†	
T_A	Operating free-air temperature		−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS638-1 and SN74ALS639-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS638 SN54ALS639			SN74ALS638 SN74ALS639			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	A ports	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OH}	B ports	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	A or B ports	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for -1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports▲					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports▲					−0.1			−0.1	
I_O§	B ports	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS638	V_{CC} = 5.5 V	Outputs high		18	36		18	30	mA
			Outputs low		25	48		26	41	
			Outputs disabled		16	35		16	30	
	'ALS639		Outputs high		25	45		25	40	
			Outputs low		30	55		30	50	
			Outputs disabled		33	60		33	54	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

2

'ALS638 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω (A outputs), R1 = R2 = 500 Ω (B outputs), T_A = MIN to MAX				UNIT
			SN54ALS638		SN74ALS638		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2	15	2	12	ns
t_{PHL}			2	15	2	12	
t_{PLH}	B	A	10	38	10	32	ns
t_{PHL}			10	40	10	36	
t_{PLH}	$\overline{G}$	A	10	42	10	40	ns
t_{PHL}			20	60	20	55	
t_{PZH}	$\overline{G}$	B	5	25	5	21	ns
t_{PZL}			5	30	5	25	
t_{PHZ}	$\overline{G}$	B	2	15	2	12	ns
t_{PLZ}			3	20	3	18	

'ALS639 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω (A outputs), R1 = R2 = 500 Ω (B outputs), T_A = MIN to MAX				UNIT
			SN54ALS639		SN74ALS639		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2	15	2	12	ns
t_{PHL}			2	15	2	12	
t_{PLH}	B	A	10	40	10	34	ns
t_{PHL}			5	30	5	25	
t_{PLH}	$\overline{G}$	A	15	55	15	47	ns
t_{PHL}			10	55	10	47	
t_{PZH}	$\overline{G}$	B	6	28	6	23	ns
t_{PZL}			8	30	8	25	
t_{PHZ}	$\overline{G}$	B	2	15	2	12	ns
t_{PLZ}			3	19	3	16	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

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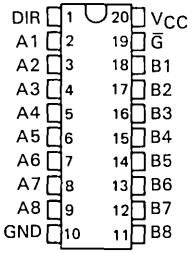
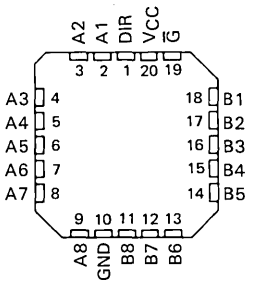
- **Bidirectional Bus Transceivers in High-Density 20-Pin Packages**
- **Choice of True or Inverting Logic**
- **Choice of 3-State or Open-Collector Outputs**
- **'AS Versions of 3-State Parts ('AS640, 'AS643, and 'AS645) in Development. Data Will Be Provided As It Becomes Available. Contact the Factory for Latest Information**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	OUTPUT	LOGIC
'ALS640	3-State	Inverting
'ALS641	Open-Collector	True
'ALS642	Open-Collector	Inverting
'ALS643	3-State	True and Inverting
'ALS644	Open-Collector	True and Inverting
'ALS645	3-State	True

SN54ALS' . . . J PACKAGE
SN74ALS' . . . N PACKAGE
(TOP VIEW)



SN54' . . . FH PACKAGE
SN74' . . . FN PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so the buses are effectively isolated.

The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS' parts.

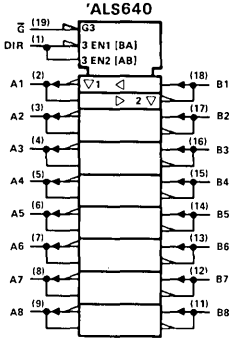
The SN54ALS640 thru SN54ALS645 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS640 thru SN74ALS645 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE

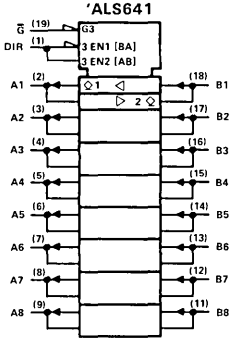
CONTROL INPUTS		OPERATION		
$\overline{G}$	DIR	'ALS640 'ALS642	'ALS641 'ALS645	'ALS643 'ALS644
L	L	$\overline{B}$ data to A bus	B data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus	$\overline{A}$ data to B bus
H	X	Isolation	Isolation	Isolation

logic symbols

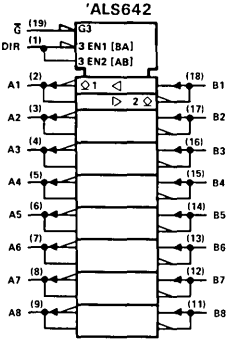
'ALS640



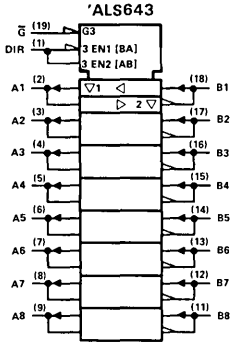
'ALS641



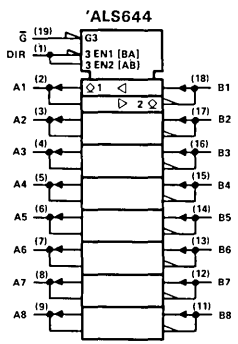
'ALS642



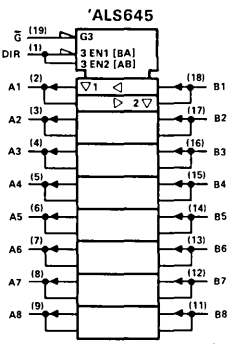
'ALS643



'ALS644

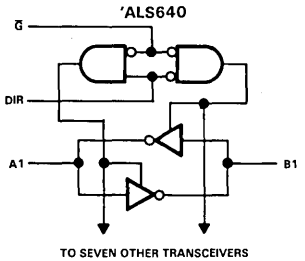


'ALS645

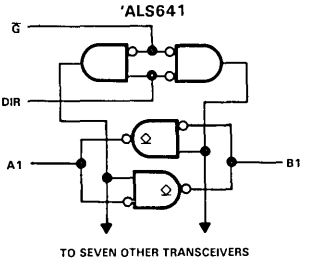


functional block diagrams (positive logic)

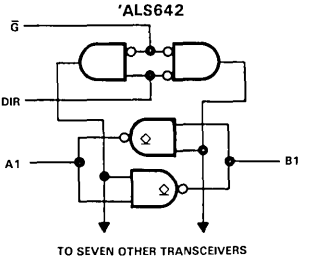
'ALS640



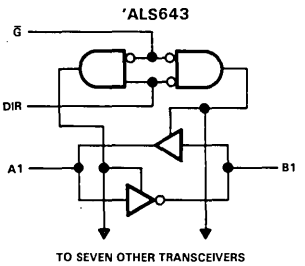
'ALS641



'ALS642



'ALS643



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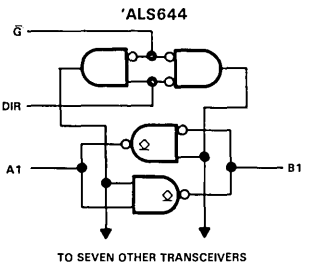

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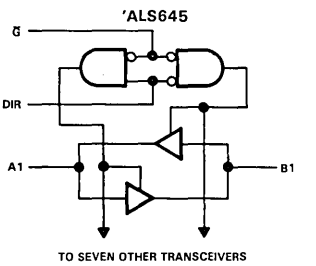

Pin numbers shown are for J and N packages.

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INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS640, SN54ALS643, SN54ALS645 . . . . . −55°C to 125°C
SN74ALS640, SN74ALS643, SN74ALS645 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS640 SN54ALS643 SN54ALS645			SN74ALS640 SN74ALS643 SN74ALS645			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12				mA
							−15	
I_{OL}	Low-level output current			12				mA
							24	
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS640-1, SN74ALS643-1, and SN74ALS645-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS'			SN74ALS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for -1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports▲					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports▲					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS640	V_{CC} = 5.5 V	Outputs high		19	36		19	32	mA
			Outputs low		27	45		27	40	
			Outputs disabled		28	48		28	43	
	'ALS643		Outputs high		27			27		
			Outputs low		35			35		
			Outputs disabled		37			37		
	'ALS645		Outputs high		30	48		30	45	
			Outputs low		36	60		36	55	
			Outputs disabled		38	63		38	58	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
▲For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

1282

ADVANCE INFORMATION

This page contains information on a new product. Specifications are subject to change without notice.

2

'ALS640 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS640		SN74ALS640		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	14	2	11	ns
t_{PHL}			2	13	2	10	
t_{PZH}	$\overline{G}$	A or B	5	25	5	21	ns
t_{PZL}			8	27	8	24	
t_{PHZ}	$\overline{G}$	A or B	3	15	3	12	ns
t_{PLZ}			4	20	4	18	

'ALS643 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS643			SN74ALS643			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	B		5			5		ns
t_{PHL}				5			5		
t_{PLH}	B	A		6			6		ns
t_{PHL}				6			6		
t_{PZH}	$\overline{G}$	A		14			14		ns
t_{PZL}				20			20		
t_{PHZ}	$\overline{G}$	A		7			7		ns
t_{PLZ}				11			11		
t_{PZH}	$\overline{G}$	B		11			11		ns
t_{PZL}				20			20		
t_{PHZ}	$\overline{G}$	B		7			7		ns
t_{PLZ}				11			11		

'ALS645 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS645		SN74ALS645		
			MIN	MAX	MIN	MAX	
t_{PLH}	B	A	3	15	3	10	ns
t_{PHL}			3	13	3	10	
t_{PZH}	$\overline{G}$	A or B	7	25	8	20	ns
t_{PZL}			10	30	10	26	
t_{PHZ}	$\overline{G}$	A or B	3	18	3	16	ns
t_{PLZ}			4	20	4	18	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage . . . . . 7 V
Input voltage: All inputs and I/O ports . . . . . 7 V
Operating free-air temperature range: SN54ALS641, SN54ALS642, SN54ALS644 . . . . . −55°C to 125°C
SN74ALS641, SN74ALS642, SN74ALS644 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS641 SN54ALS642 SN54ALS644			SN74ALS641 SN74ALS642 SN74ALS644			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12				mA
							24	
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS641-1, SN74ALS642-1, and SN74ALS644-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS641 SN54ALS642 SN54ALS644			SN74ALS641 SN74ALS642 SN74ALS644			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for -1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports▲					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports▲					−0.1			−0.1	
I_{CC}	'ALS641	V_{CC} = 5.5 V	Outputs high		24	37		24	33	mA
			Outputs low		30	45		30	40	
	'ALS642		Outputs high		8	15		8	15	
			Outputs low		13	28		13	28	
	'ALS644		Outputs high		16	32		16	29	
			Outputs low		25	45		25	40	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
▲For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

PRODUCT PREVIEW

'ALS641 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS641		SN74ALS641		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	10	37	10	30	ns
t_{PHL}			5	23	5	19	
t_{PLH}	$\overline{G}$ or DIR	A or B	13	40	13	35	ns
t_{PHL}			13	40	13	35	

'ALS642 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS642		SN74ALS642		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	15	50	15	41	ns
t_{PHL}			5	25	5	22	
t_{PLH}	$\overline{G}$ or DIR	A or B	15	45	15	40	ns
t_{PHL}			15	50	15	45	

Additional information on this product can be obtained from the factory as it becomes available.

'ALS644 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS644		SN74ALS644		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	15	50	15	41	ns
t_{PHL}			5	25	5	22	
t_{PLH}	B	A	15	45	15	37	ns
t_{PHL}			5	23	5	21	
t_{PLH}	$\overline{G}$	A	15	41	15	37	ns
t_{PHL}			13	37	13	35	
t_{PLH}	$\overline{G}$	B	12	35	12	33	ns
t_{PHL}			15	40	15	35	
t_{PLH}	DIR	A	10	33	10	30	ns
t_{PHL}			10	33	10	30	
t_{PLH}	DIR	B	20	48	20	45	ns
t_{PHL}			15	40	15	35	

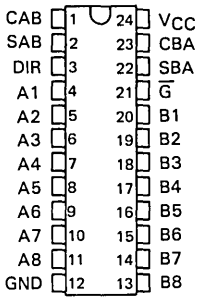
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2661, DECEMBER 1982

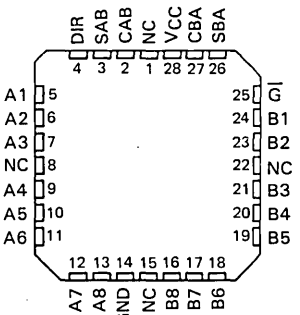
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True or Inverting Data Paths
- Choice of 3-State or Open-Collector Outputs
- Included Among the Package Options Are Compact 24-pin 300-mil Wide DIPs and Both 28-pin Plastic and Ceramic Chip Carriers
- Dependable Texas Instruments Quality and Reliability

DEVICE	OUTPUT	LOGIC
'ALS646	3-State	True
'ALS647	Open-Collector	True
'ALS648	3-State	Inverting
'ALS649	Open-Collector	Inverting

SN54ALS' . . . JT PACKAGE
SN74ALS' . . . NT PACKAGE
(TOP VIEW)

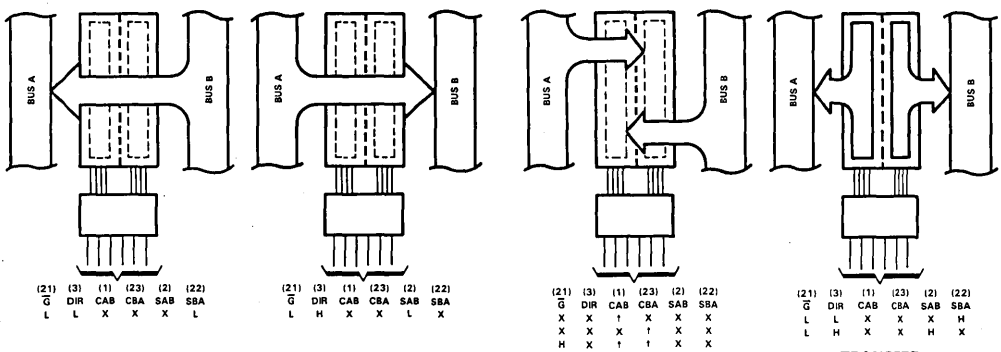


SN54ALS' . . . FH PACKAGE
SN74ALS' . . . FN PACKAGE
(TOP VIEW)



description

These devices consist of bus transceiver circuits with 3-state or open-collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'ALS646, 'ALS647, 'ALS648, or 'ALS649.



REAL-TIME TRANSFER BUS B TO BUS A

REAL-TIME TRANSFER BUS A TO BUS B

STORAGE FROM A, B, OR A AND B

TRANSFER STORED DATA TO A OR B

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

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Enable ($\overline{G}$) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when enable $\overline{G}$ is active (low). In the isolation mode (control $\overline{G}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS' parts.

The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

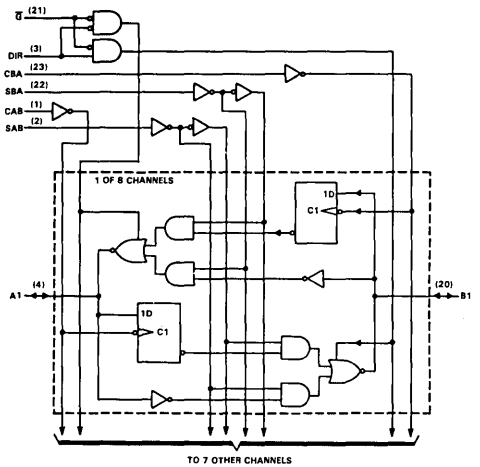
FUNCTION TABLE

INPUTS						DATA I/O*		OPERATION OR FUNCTION	
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'ALS646, 'ALS647	'ALS648, 'ALS649
X	X	↑	X	X	X	Input	Not specified	Store A, B unspecified	Store A, B unspecified
X	X	X	↑	X	X	Not specified	Input	Store B, A unspecified	Store B, A unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time $\overline{B}$ Data to A Bus
L	L	X	X	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\overline{A}$ Data to B Bus
L	H	X	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

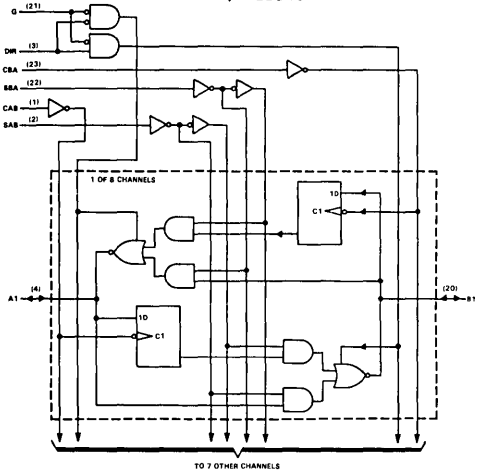
*The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

functional block diagrams (positive logic)

'ALS646, 'ALS647



'ALS648, 'ALS649



Pin numbers shown are for JT and NT packages.

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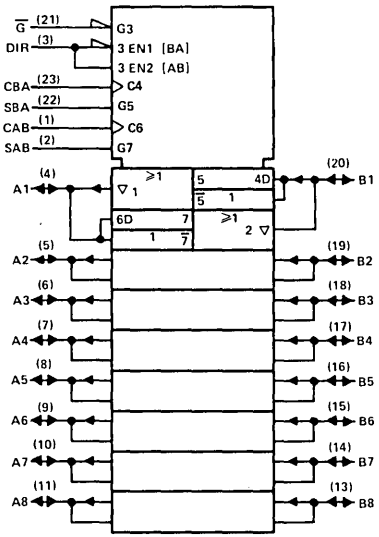
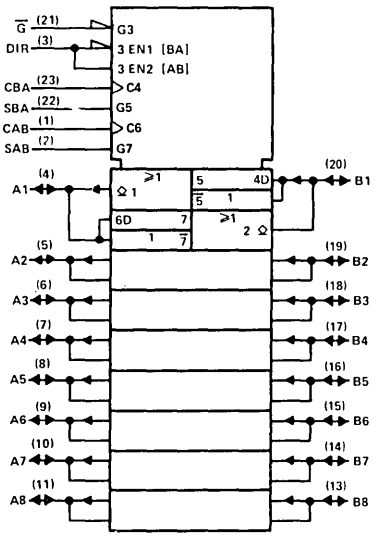
logic symbols

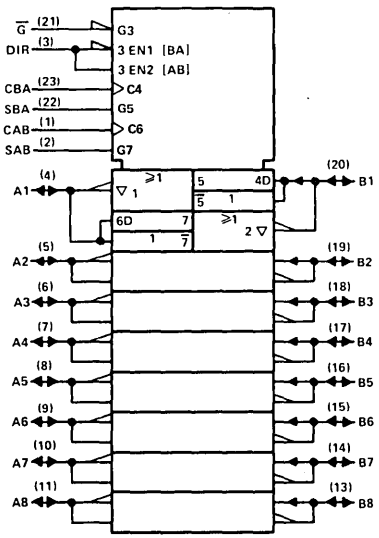
'ALS646



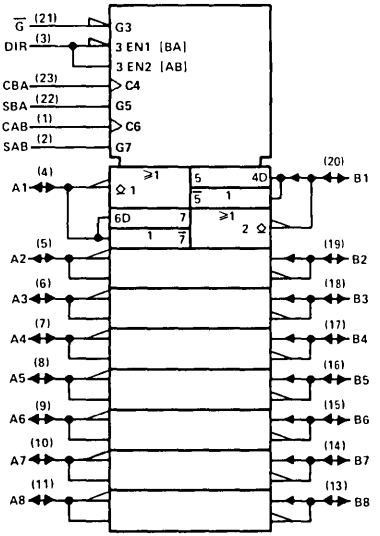
'ALS647



'ALS648



'ALS649



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Control inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS646, SN54ALS648 . . . . . −55°C to 125°C
SN74ALS646, SN74ALS648 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS646 SN54ALS648			SN74ALS646 SN74ALS648			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12				mA
							−15	
I_{OL}	Low-level output current			12				mA
							24	
							48†	
t_w	Pulse duration, clocks high or low							ns
t_{su}	Setup time, A before CAB† or B before CBA†							ns
t_h	Hold time, A after CAB† or B after CBA†							ns
T_A	Operating free-air temperature	−55		125	0		70	°C

The extended condition applies if V_{CC} is maintained between 4.75 and 5.25 V.
†The 48-mA limit applies for the SN74ALS646-1 and SN74ALS648-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS646 SN54ALS648			SN74ALS646 SN74ALS648			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for -1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports▲					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports▲					−0.2			−0.2	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS646	V_{CC} = 5.5 V	Outputs high							mA
			Outputs low							
			Outputs disabled							
	'ALS648		Outputs high							
			Outputs low							
			Outputs disabled							

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
▲For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
Additional information on these products can be obtained from the factory as it becomes available.

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'ALS646 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS646			SN74ALS646			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH} / t_{PHL}	CBA or CAB	A or B							ns
t_{PLH} / t_{PHL}	A or B	B or A							ns
t_{PLH} / t_{PHL}	SBA or SAB† (with A or B high)	A or B							ns
t_{PLH} / t_{PHL}	SBA or SAB† (with A or B low)	A or B							ns
t_{PZH} / t_{PZL}	$\overline{G}$	A or B							ns
t_{PHZ} / t_{PLZ}	$\overline{G}$	A or B							ns
t_{PZH} / t_{PZL}	DIR	A or B							ns
t_{PHZ} / t_{PLZ}	DIR	A or B							ns

'ALS648 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS648			SN74ALS648			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH} / t_{PHL}	CBA or CAB	A or B							ns
t_{PLH} / t_{PHL}	A or B	B or A							ns
t_{PLH} / t_{PHL}	SBA or SAB† (with A or B high)	A or B							ns
t_{PLH} / t_{PHL}	SBA or SAB† (with A or B low)	A or B							ns
t_{PZH} / t_{PZL}	$\overline{G}$	A or B							ns
t_{PHZ} / t_{PLZ}	$\overline{G}$	A or B							ns
t_{PZH} / t_{PZL}	DIR	A or B							ns
t_{PHZ} / t_{PLZ}	DIR	A or B							ns

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
Additional information on these products can be obtained from the factory as it becomes available.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS647, SN54ALS649 . . . . . −55°C to 125°C
SN74ALS647, SN74ALS649 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS647 SN54ALS649			SN74ALS647 SN74ALS649			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12				mA
							24	
							48†	
t_w	Pulse duration, clocks high or low							ns
t_{su}	Setup time, A before CABt or B before CBAt							ns
t_h	Hold time, A after CABt or B after CBAt							ns
T_A	Operating free-air temperature	−55		125	0		70	°C

The extended condition applies if V_{CC} is maintained between 4.75 and 5.25 V.
†The 48-mA limit applies for the SN74ALS646-1 and SN74ALS648-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS647 SN54ALS649			SN74ALS647 SN74ALS649			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4				V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for -1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	
I_{IH}	A or B ports▲	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	Control inputs					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports▲					−0.2			−0.2	
I_{CC}	'ALS647	V_{CC} = 5.5 V	Outputs high							mA
			Outputs low							
			Outputs disabled							
	'ALS649		Outputs high							
			Outputs low							
			Outputs disabled							

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
▲For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
Additional information on these products can be obtained from the factory as it becomes available.

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'ALS647 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX						UNIT
			SN54ALS647			SN74ALS647			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CBA or CAB	A or B							ns
t_{PHL}									
t_{PLH}	A or B	B or A							ns
t_{PHL}									
t_{PLH}	SBA or SAB† (with A or B high)	A or B							ns
t_{PHL}									
t_{PLH}	SBA or SAB† (with A or B low)	A or B							ns
t_{PHL}									
t_{PLH}	$\overline{G}$	A or B							ns
t_{PHL}									
t_{PLH}	DIR	A or B							ns
t_{PHL}									

'ALS649 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX						UNIT
			SN54ALS649			SN74ALS649			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CBA or CAB	A or B							ns
t_{PHL}									
t_{PLH}	A or B	B or A							ns
t_{PHL}									
t_{PLH}	SBA or SAB† (with A or B high)	A or B							ns
t_{PHL}									
t_{PLH}	SBA or SAB† (with A or B low)	A or B							ns
t_{PHL}									
t_{PLH}	$\overline{G}$	A or B							ns
t_{PHL}									
t_{PLH}	DIR	A or B							ns
t_{PHL}									

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

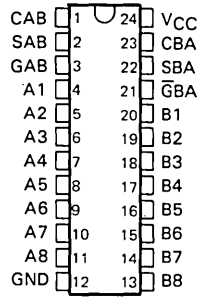
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

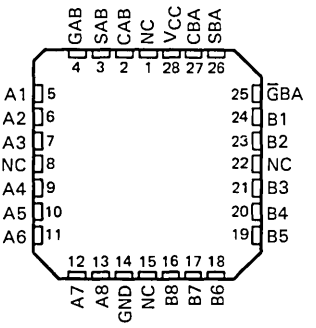
- Bus Transceivers/Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True and Inverting Data Paths
- Choice of 3-State or Open-Collector Outputs to A Bus
- Included Among the Package Options Are Compact 24-Pin 300-mil-Wide DIPs and Both 28-Pin Plastic and Ceramic Chip Carriers
- Dependable Texas Instruments Quality and Reliability

DEVICE	A OUTPUT	B OUTPUT	LOGIC
'ALS651	3-State	3-State	Inverting
'ALS652	3-State	3-State	True
'ALS653	Open-collector	3-State	Inverting
'ALS654	Open-collector	3-State	True

SN54ALS' . . . JT PACKAGE
SN74ALS' . . . NT PACKAGE
(TOP VIEW)



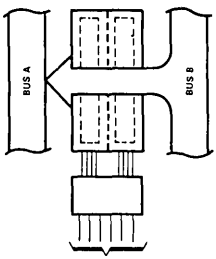
SN54ALS' . . . FC PACKAGE
SN74ALS' . . . FN PACKAGE
(TOP VIEW)



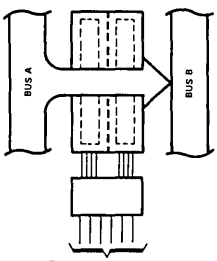
NC — No internal connection

description

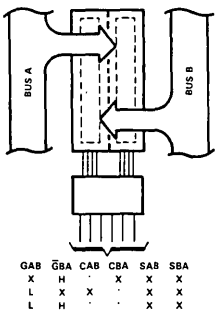
These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and $\overline{G}$BA are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'ALS651, 'ALS652, 'ALS653, and 'ALS654.



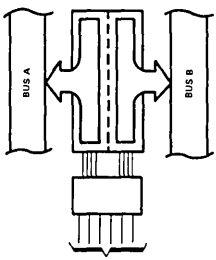
REAL-TIME TRANSFER
BUS B TO BUS A



REAL-TIME TRANSFER
BUS A TO BUS B



STORAGE FROM
A AND/OR B



TRANSFER
STORED DATA
TO A AND/OR B

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

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Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{G}$BA. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The -1 versions of the SN74ALS651 through SN74ALS654 are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS651 through SN54ALS654.

The SN54ALS651 through SN54ALS654 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS651 through SN74ALS654 are characterized for operation from 0°C to 70°C.

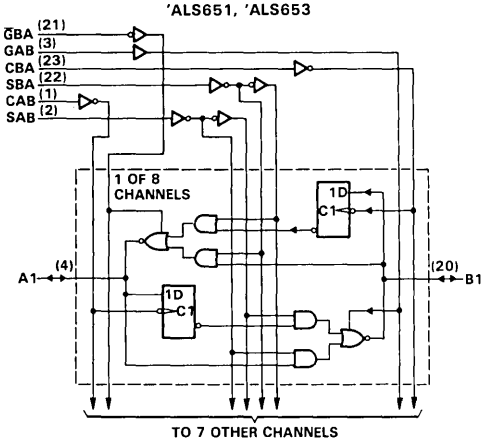
FUNCTION TABLE

INPUTS						DATA I/O*		OPERATION OR FUNCTION	
GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'ALS651, 'ALS653	'ALS652, 'ALS654
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B Data	Store A and B Data
X	H	↑	H or L	X	X	Input	Not specified	Store A, Hold B	Store A, Hold B
H	H	↑	↑	X	X	Input	Output	Store A in both registers	Store A in both registters
L	X	H or L	↑	X	X	Not specified	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

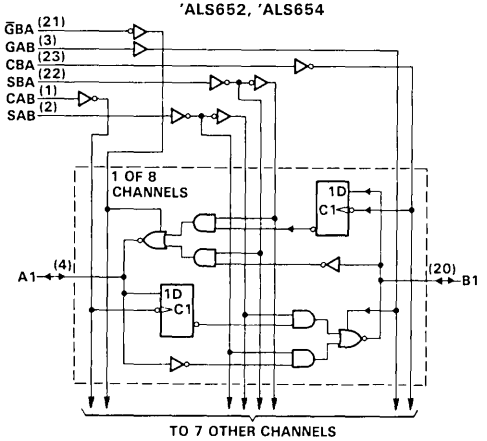
*The data output functions may be enabled or disabled by various signals at the GAB and $\overline{G}$BA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic diagrams (positive logic)

'ALS651, 'ALS653



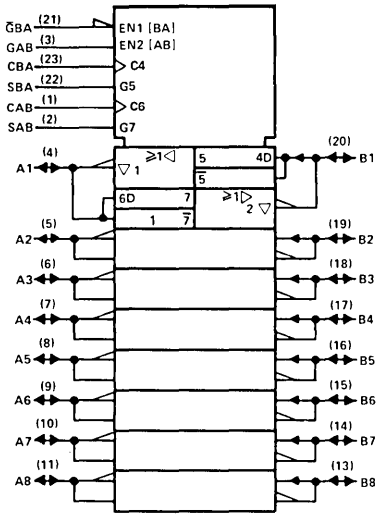
'ALS652, 'ALS654



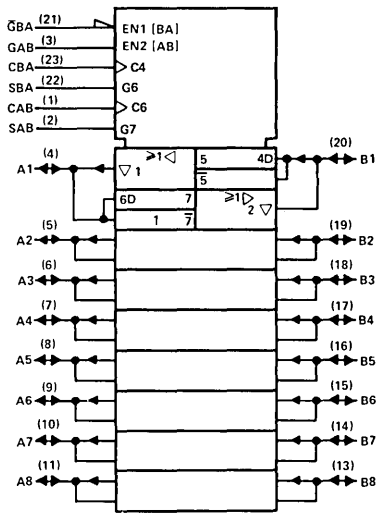
Pin numbers shown are for JT and NT packages.

logic symbols

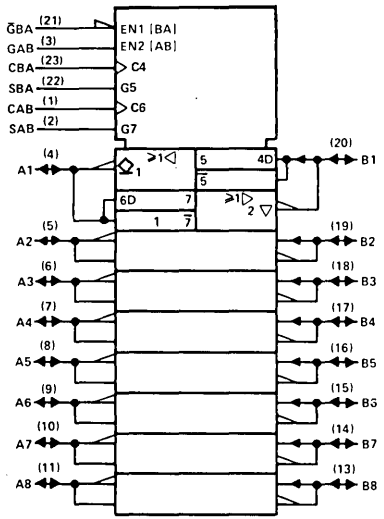
'ALS651



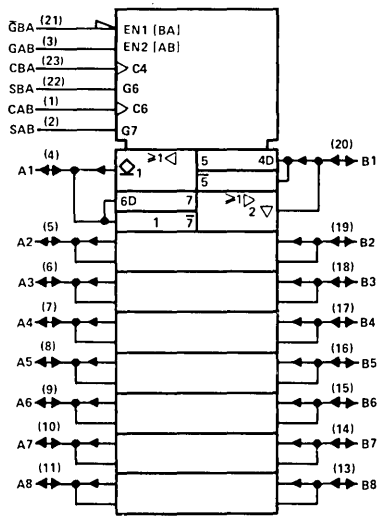
'ALS652



'ALS653



'ALS654



Pin numbers shown are for JT and NT packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Control inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS651, SN54ALS652 . . . . . −55 °C to 125 °C
SN74ALS651, SN74ALS652 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS651 SN54ALS652			SN74ALS651 SN74ALS652			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				12			24	mA
								48¶	
t_w	Pulse duration	CBA or CAB high							ns
		CBA or CAB low							
t_{su}	Setup time before CAB or CBA↑	SBA or SAB							ns
		A or B							
t_h	Hold time after CAB or CBA↑	SBA or SAB							ns
		A or B							
T_A	Operating free-air temperature		−55		125	0		70	°C

¶The 48 mA limit applies for the SN74ALS651-1 and SN74ALS652-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS651 SN54ALS652			SN74ALS651 SN74ALS652			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for -1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports▲					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports▲					−0.2			−0.2	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS651	V_{CC} = 5.5 V	Outputs high							mA
			Outputs low							
			Outputs disabled							
	'ALS652		Outputs high							
			Outputs low							
			Outputs disabled							

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
▲For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

'ALS651 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS651			SN74ALS651			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CBA or CAB	A or B							ns
t_{PHL}									
t_{PLH}	A or B	B or A							ns
t_{PHL}									
t_{PLH}	SBA or SAB† (with A or B high)	A or B							ns
t_{PHL}									
t_{PLH}	SBA or SAB† (with A or B low)	A or B							ns
t_{PHL}									
t_{PZH}	$\overline{G}$BA	A							ns
t_{PZL}									
t_{PHZ}	$\overline{G}$BA	A							ns
t_{PLZ}									
t_{PZH}	GAB	B							ns
t_{PZL}									
t_{PHZ}	GAB	B							ns
t_{PLZ}									

'ALS652 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS652			SN74ALS652			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CBA or CAB	A or B							ns
t_{PHL}									
t_{PLH}	A or B	B or A							ns
t_{PHL}									
t_{PLH}	SBA or SAB† (with A or B high)	A or B							ns
t_{PHL}									
t_{PLH}	SBA or SAB† (with A or B low)	A or B							ns
t_{PHL}									
t_{PZH}	$\overline{G}$BA	A							ns
t_{PZL}									
t_{PHZ}	$\overline{G}$BA	A							ns
t_{PHL}									
t_{PZH}	GAB	B							ns
t_{PZL}									
t_{PHZ}	GAB	B							ns
t_{PLZ}									

†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs and A I/O ports . . . . . 7 V
B I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS653, SN54ALS654 . . . . . −55°C to 125°C
SN74ALS653, SN74ALS654 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS653 SN54ALS654			SN74ALS653 SN74ALS654			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage	A ports			5.5			5.5	V
I_{OH}	High-level output current	B ports			−12			−15	mA
I_{OL}	Low-level output current				12			24	mA
								48¶	
t_w	Pulse duration	CBA or CAB high							ns
		CBA or CAB low							
t_{su}	Setup time before CAB or CBA↑	SBA or SAB							ns
		A or B							
t_h	Hold time after CAB or CBA↑	SBA or SAB							ns
		A or B							
T_A	Operating free-air temperature		−55		125	0		70	°C

¶The 48 mA limit applies for the SN74ALS653-1 and SN74ALS654-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS653 SN54ALS654			SN74ALS653 SN74ALS654			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	B ports	V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		V
		V_{CC} = 4.5 V	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V	I_{OH} = −15 mA				2			
I_{OH}	A ports	V_{CC} = 4.5 V,	V_{OH} = −5.5 mA			0.1			0.1	V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.75 V, (I_{OL} = 48 mA for -1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports▲					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports▲					−0.2			−0.2	
I_O§	B ports	V_{CC} = 5 V,	V_O = 2.25 V	−30		−112	−30		!112	mA
I_{CC}	'ALS653	V_{CC} = 5.5 V	Outputs high							mA
			Outputs low							
			Outputs disabled							
	'ALS654		Outputs high							
			Outputs low							
			Outputs disabled							

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
▲For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

'ALS653 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, (A outputs) R1 = R2 = 500 Ω, (B outputs) T_A = MIN to MAX						UNIT
			SN54ALS653			SN74ALS653			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CBA	A							ns
t_{PHL}									
t_{PLH}	CAB	B							ns
t_{PHL}									
t_{PLH}	A	B							ns
t_{PHL}									
t_{PLH}	B	A							ns
t_{PHL}									
t_{PLH}	SBA† (with B high)	A							ns
t_{PHL}									
t_{PLH}	SBA† (with B low)	A							ns
t_{PHL}									
t_{PLH}	SAB† (with A high)	B							ns
t_{PHL}									
t_{PLH}	SAB† (with A low)	B							ns
t_{PHL}									
t_{PLH}	$\overline{G}$BA	A							ns
t_{PHL}									
t_{PZH}	GAB	B							ns
t_{PZL}									
t_{PHZ}	GAB	B							ns
t_{PLZ}									

†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

'ALS654 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, (A outputs) R1 = R2 = 500 Ω, (B outputs) T_A = MIN to MAX						UNIT
			SN54ALS654			SN74ALS654			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CBA	A							ns
t_{PHL}									
t_{PLH}	CAB	B							ns
t_{PHL}									
t_{PLH}	A	B							ns
t_{PHL}									
t_{PLH}	B	A							ns
t_{PHL}									
t_{PLH}	SBA† (with B high)	A							ns
t_{PHL}									
t_{PLH}	SBA† (with B low)	A							ns
t_{PHL}									
t_{PLH}	SAB† (with A high)	B							ns
t_{PHL}									
t_{PLH}	SAB† (with A low)	B							ns
t_{PHL}									
t_{PZH}	$\overline{G}$BA	A							ns
t_{PZL}									
t_{PHZ}	GAB	B							ns
t_{PLZ}									
t_{PLH}	GAB	B							ns
t_{PHL}									

†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

- 'ALS677 is a 16-bit to 4-Bit Comparator with Enable
- 'ALS678 is a 16-Bit to 4-Bit Comparator with Latch
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

2

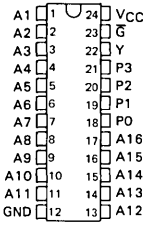
description

The 'ALS677 and 'ALS678 address comparators simplify addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 16 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A16 must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

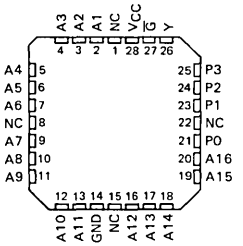
The 'ALS677 features an enable input (G). When G is low, the device is enabled. When G is high, the device is disabled and the output is high regardless of the A and P inputs. The 'ALS678 features a transparent latch and a latch enable input (C). When C is high, the device is in the transparent mode. When C is low, the previous logic state of Y is latched.

The SN54ALS677 and SN54ALS689 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN54ALS677 and SN74ALS678 are characterized for operation from 0°C to 70°C.

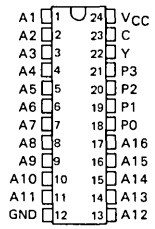
SN54ALS677 . . . JT PACKAGE
SN74ALS677 . . . .NT PACKAGE
(TOP VIEW)



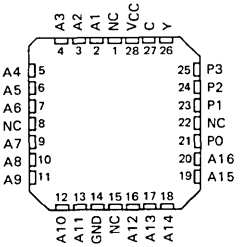
SN54ALS677 . . . FH PACKAGE
SN74ALS677 . . . FN PACKAGE



SN54ALS678 . . . JT PACKAGE
SN74ALS678 . . . NT PACKAGE
(TOP VIEW)



SN54ALS678 . . . FH PACKAGE
SN74ALS678 . . . FN PACKAGE
(TOP VIEW)

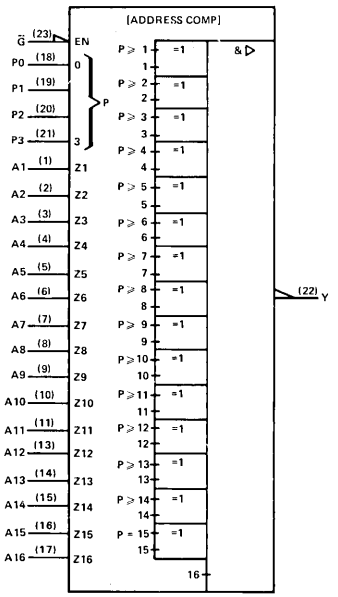


FUNCTION TABLE

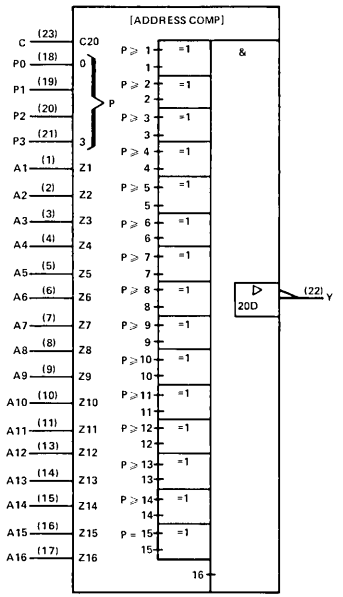
'ALS677	'ALS678	INPUTS COMMON TO 'ALS677 AND 'ALS678																				OUTPUT
$\overline{G}$	C	P3	P2	P1	P0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	Y
L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	L
L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L
L	H	H	L	L	H	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	L
L	H	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	L
L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L
L	H	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	L
L	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	L
L	H	All other combinations																				H
H		'ALS677: Any combination																				H
	L	'ALS678: Any combination																				Latched

logic symbols

'ALS677



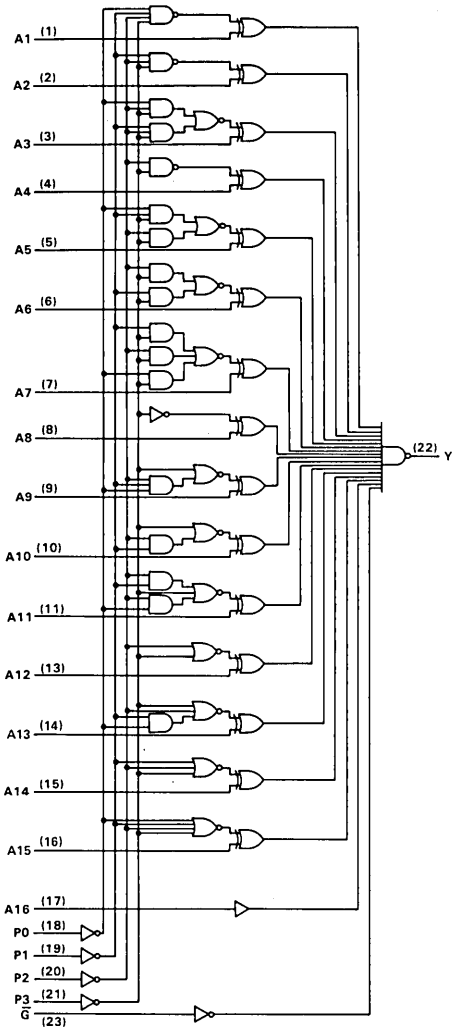
'ALS678



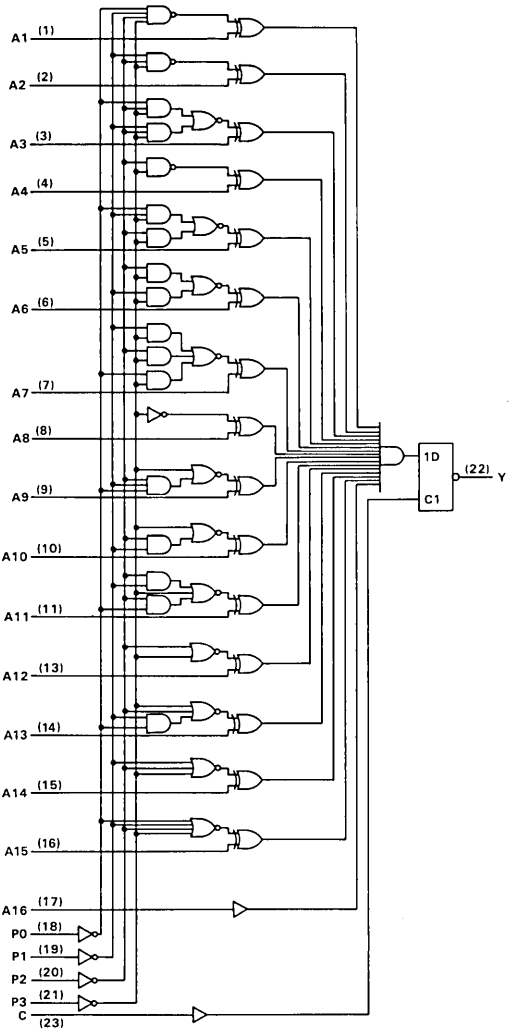
Pin numbers shown are for JT and NT packages.

logic diagrams (positive logic)

'ALS677



'ALS678



Pin numbers shown are for JT and NT packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS677, SN54ALS678 . . . . . −55°C to 125°C
SN74ALS677, SN74ALS678 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS677 SN54ALS678			SN74ALS677 SN74ALS678			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS677 SN54ALS678			SN74ALS677 SN74ALS678			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
		V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_{IL} = 0.4 V			−0.1			−0.1	mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS677	V_{CC} = 5.5 V								mA
	'ALS678									

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS677 SN54ALS678			SN74ALS677 SN74ALS678			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any P	Y							ns
t_{PHL}									
t_{PLH}	Any A	Y							ns
t_{PHL}									
t_{PLH}	$\overline{G}$ ('ALS677)	Y							ns
t_{PHL}									
t_{PLH}	C ('ALS678)	Y							ns
t_{PHL}									

‡All typical values are at V_{CC} = 5V, T_A = 25°C.
NOTE 2: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

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TYPICAL APPLICATION INFORMATION

The 'ALS677 and 'ALS678 can be wired to recognize any one of $2^{16}-1$ addresses. The number of "lows" in the address determines the input pattern for the P inputs. Then those system address lines that are low in the address to be recognized are connected to the lowest numbered A inputs of the address comparator and the system address lines that are high are connected to the highest numbered A inputs.

For example, assume the comparator is to enable a device when the 16-bit system address is:

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
H	H	L	L	H	H	L	L	H	H	L	L	H	H	H	H

Since the address contains 6 lows and 10 highs, the following connections are made:

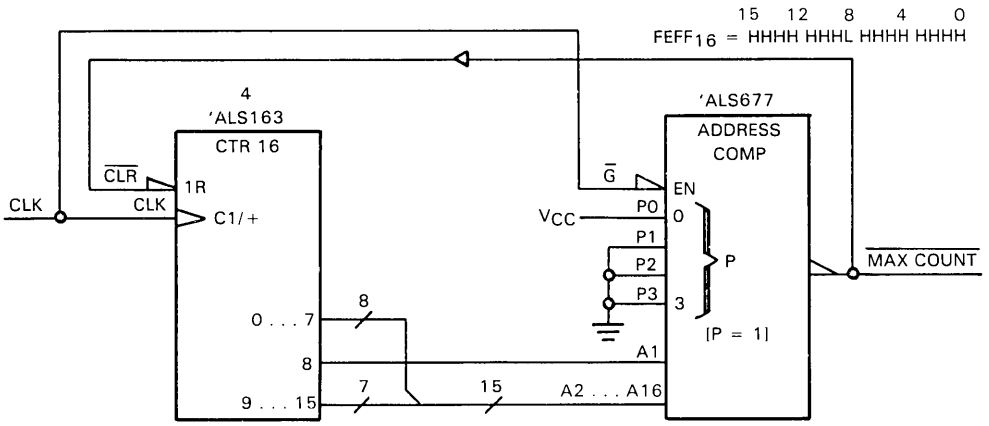
P3 to 0 V, P2 to V_{CC}, P1 to V_{CC}, and P0 to 0 V.

System address lines A13, A12, A9, A8, A5, and A4 to comparator inputs A1 through A6 in any convenient order.

The remaining ten system address lines to comparator inputs A7 through A16 in any convenient order.

The output provides an active-low enabling signal.

The following circuit is a modulc-N synchronous counter. The 'ALS163 is connected to provide a low-level clear signal when $N = FEFF_{16}$.



MODULO-N SYNCHRONOUS COUNTER

- **'ALS679 is a 12-Bit to 4-Bit Comparator With Enable**
- **'ALS680 is a 12-Bit to 4-Bit Comparator With Latch**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

2

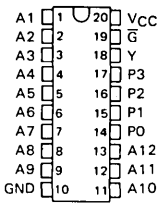
description

The 'ALS679 and 'ALS680 address comparators simplify addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 12 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A12 must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

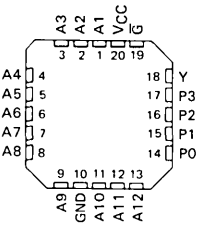
The 'ALS679 features an enable input ($\overline{G}$). When $\overline{G}$ is low, the device is enabled. When $\overline{G}$ is high, the device is disabled and the output is high regardless of the A and P inputs. The 'ALS680 features a transparent latch and a latch enable input (C). When C is high, the device is in the transparent mode. When C is low, the previous logical state of Y is latched.

The SN54ALS679 and SN54ALS680 are characterized for operation over the full military temperature of −55°C to 125°C. The SN74ALS679 and SN74ALS680 are characterized for operation from 0°C to 70°C.

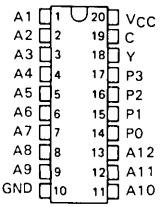
SN54ALS679 . . . J PACKAGE
SN74ALS679 . . . N PACKAGE
(TOP VIEW)



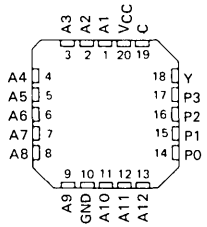
SN54ALS679 . . . FH PACKAGE
SN74ALS679 . . . FN PACKAGE
(TOP VIEW)



SN54ALS680 . . . J PACKAGE
SN74ALS680 . . . N PACKAGE
(TOP VIEW)



SN54ALS680 . . . FH PACKAGE
SN74ALS680 . . . FN PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
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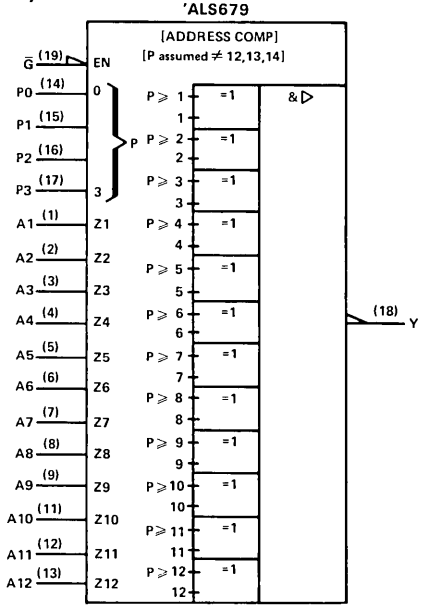
FUNCTION TABLE

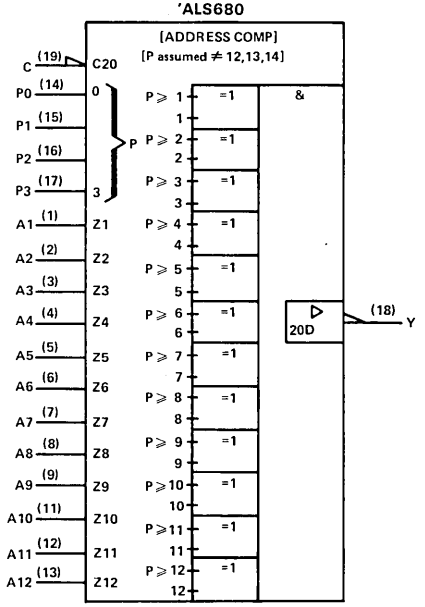
'ALS679	'ALS680	INPUTS COMMON TO 'ALS679 AND 'ALS680																OUTPUT
$\overline{G}$	C	P3	P2	P1	P0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	Y
L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L
L	H	L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	L
L	H	L	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	L
L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L
L	H	H	L	L	H	L	L	L	L	L	L	L	L	L	H	H	H	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	L
L	H	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	H	H	L	L	L	L	L	L	L	L	L	L	H	H	H	L	L*
L	H	H	H	L	H	L	L	L	L	L	L	L	L	L	H	H	L	L*
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L*
L	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	All other combinations																H
H		'ALS679: Any combination																H
	L	'ALS680: Any combination																Latched

logic symbols

'ALS679



'ALS680

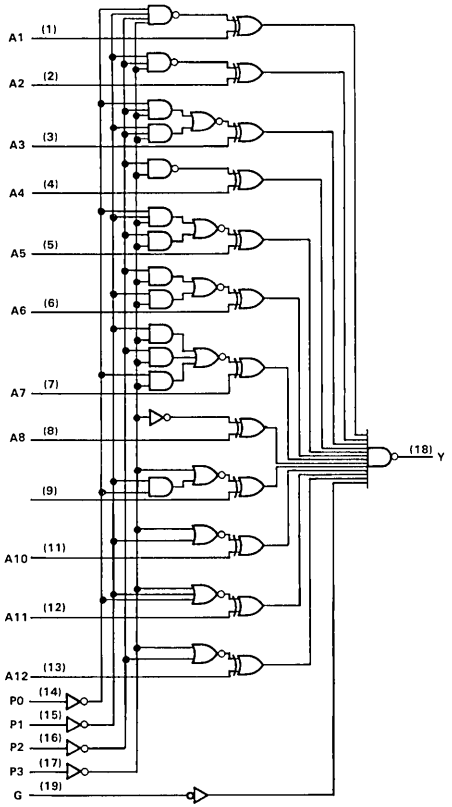


*The three shaded rows of the function table show combinations that would normally not be used in address comparator applications. The logic symbols above are not valid for these combinations in which P = 12, 13, and 14. If symbols valid for all combinations are required, starting with the fourth Exclusive-OR from the bottom, change P ≥ 9 to P = 9...11/13...15, P ≥ 10 to P = 10/11/14/15, and P ≥ 11 to P = 11/15.

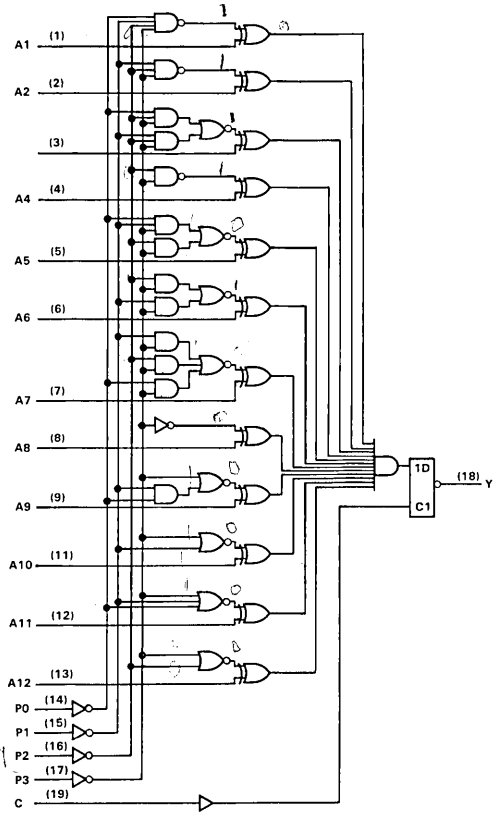
Pin numbers shown are for J and N packages.

logic diagrams (positive logic)

'ALS679



'ALS680



Pin numbers shown are for J and N packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS679, SN54ALS680 . . . . . −55 °C to 125 °C
SN74ALS679, SN74ALS680 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS679 SN54ALS680			SN74ALS679 SN74ALS680			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS679 SN54ALS680			SN74ALS679 SN74ALS680			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS679	V_{CC} = 5.5 V								mA
	'ALS680									

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS679 SN54ALS680			SN74ALS679 SN74ALS680			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any P	Y							ns
t_{PHL}									
t_{PLH}	Any A	Y							ns
t_{PHL}									
t_{PLH}	$\overline{G}$ ('ALS679)	Y							ns
t_{PHL}									
t_{PLH}	C ('ALS680)	Y							ns
t_{PHL}									

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

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TYPICAL APPLICATION INFORMATION

The 'ALS679 and 'ALS680 can be wired to recognize any one of 2^{12} addresses. The number of "lows" in the address determines the input pattern for the P inputs. Then those system address lines that are low in the address to be recognized are connected to the lowest numbered A inputs of the address comparator and the system address lines that are high are connected to the highest numbered A inputs.

For example, assume the comparator is to enable a device when the 12-bit system address is:

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
H	H	L	L	H	H	L	L	H	H	H	H

Since the address contains 4 lows and 8 highs, the following connections are made:

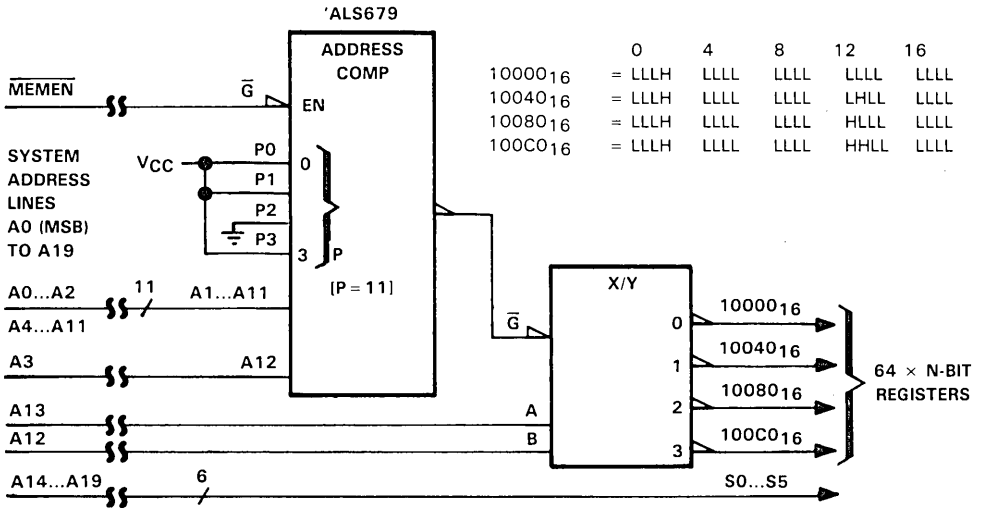
P3 to 0 V, P2 to V_{CC}, P1 to 0 V, and P0 to 0 V.

System address lines A9, A8, A5, and A4 to comparator inputs A1 through A4 in any convenient order.

The remaining eight system address lines to comparator inputs A5 through A12 in any convenient order.

The output provides an active-low enabling signal.

The following circuit is a register bank decoder that examines the 14 most significant bits (A0 through A13) of a 20-bit address to select banks corresponding to the hex addresses 10000, 10040, 10080, and 100C0.



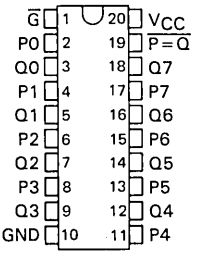
REGISTER BANK DECODER

- Compares Two Eight-Bit Words
- Choice of Totem-Pole or Open-Collector Outputs
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

TYPE	OUTPUT FUNCTION AND CONFIGURATION
'ALS688†	$\overline{P=Q}$ totem-pole
'ALS689	$\overline{P=Q}$ open-collector

†'ALS688 is identical to 'ALS521

SN54ALS688, SN54ALS689 . . . J PACKAGE
SN74ALS688, SN74ALS689 . . . N PACKAGE
(TOP VIEW)

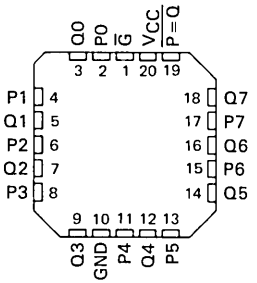


description

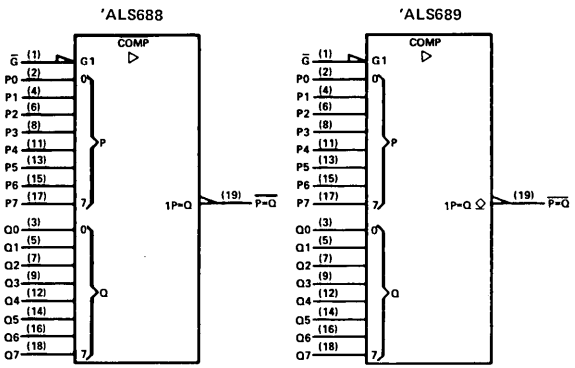
These identity comparators perform comparisons of two eight-bit binary or BCD words. The 'ALS688 and 'ALS689 provide P = Q outputs. The 'ALS688 has totem-pole outputs, while 'ALS689 has open-collector outputs.

The SN54ALS688 and SN54ALS689 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS688 and SN74ALS689 are characterized for operation from 0 °C to 70 °C.

SN54ALS688, SN54ALS689 . . . FH PACKAGE
SN74ALS688, SN74ALS689 . . . FN PACKAGE
(TOP VIEW)



logic symbols



Pin numbers shown are for J and N packages.

FUNCTION TABLE

INPUTS		OUTPUT
DATA P,Q	ENABLE $\overline{G}$	$\overline{P = Q}$
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

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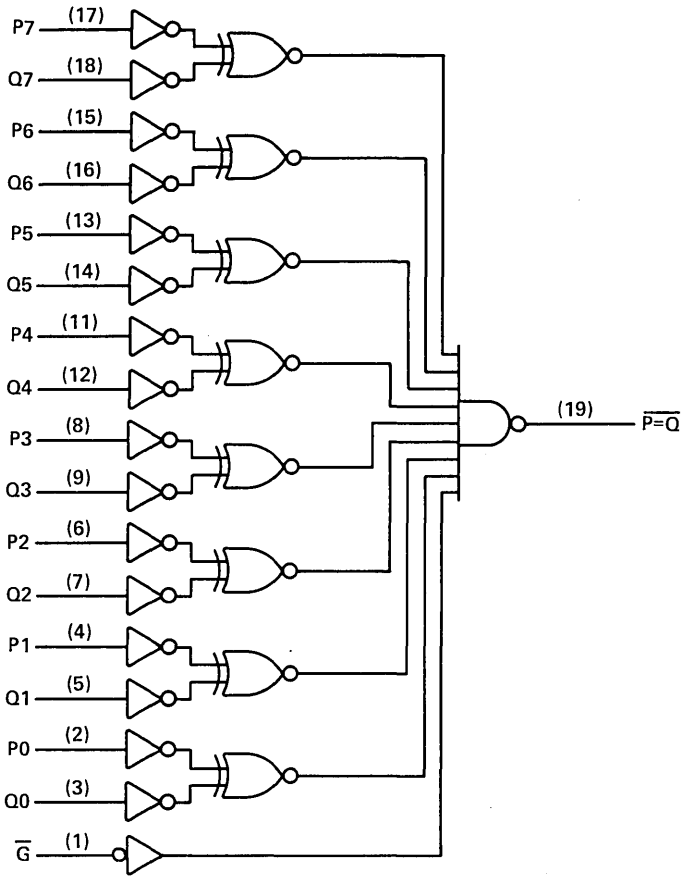
logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: . . . . . 7 V
Off-state output voltage: 'ALS689 . . . . . 7 V
Operating free-air temperature range: SN54ALS688, SN54AS689 . . . . . −55°C to 125°C
SN74ALS688, SN74AS689 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS688			SN74ALS688			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS688			SN74ALS688			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	24	3.3					V
	V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			9	15		9	15	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS688		SN74ALS688		
			MIN	MAX	MIN	MAX	
t_{PLH}	P	$\overline{P=Q}$	3	16	3	12	ns
t_{PHL}			5	25	5	20	
t_{PLH}	Q	$\overline{P=Q}$	3	16	3	12	ns
t_{PHL}			5	25	5	20	
t_{PLH}	$\overline{G}$	$\overline{P=Q}$	3	15	3	12	ns
t_{PHL}			5	25	5	22	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

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recommended operating conditions

		SN54ALS689			SN74ALS689			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS689			SN74ALS689			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.75 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_{CC}	V_{CC} = 5.5 V			9	15		9	15	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

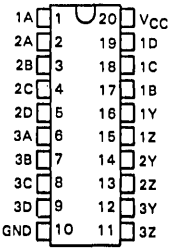
switching characteristics (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS689		SN74ALS689		
			MIN	MAX	MIN	MAX	
t_{PLH}	P	$\overline{P=Q}$	10	30	10	25	ns
t_{PHL}			5	25	5	23	
t_{PLH}	Q	$\overline{P=Q}$	10	30	10	25	ns
t_{PHL}			5	25	5	23	
t_{PLH}	$\overline{G}$	$\overline{P=Q}$	8	30	8	25	ns
t_{PHL}			8	30	8	25	

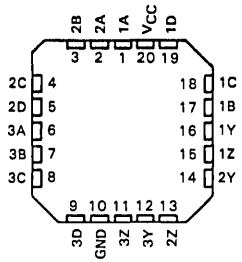
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- Less than 0.5 ns Skew between True and Complementary Outputs
- High Capacitive-Drive Capability
- Current-Sinking Capability Up to 48 mA
- Approximately 35% Improvement in AC Performance over Schottky TTL
- Package Options Include DIPs and Both Plastic and Ceramic Chip Carriers
- Suitable for Use in Applications such as:
  - Differential Line Drivers
  - Complementary Input Circuit for Decoders and Code Converters
  - Symmetrical Complementary Clock Generators
- Dependable Texas Instruments Quality and Reliability

SN54AS800 . . . . J PACKAGE
SN74AS800 . . . . N PACKAGE
(TOP VIEW)



SN54AS800 . . . . FH PACKAGE
SN74AS800 . . . . FN PACKAGE
(TOP VIEW)



description

The 'AS800 is especially suitable for symmetrical complementary clock-generator applications due to the delay time in either function (AND/NAND) being typically 4 ns with less than 0.5 ns skew between the true and complementary outputs. Elimination of decode spikes in symmetrical decoder and code converter applications, and the high capacitive-drive capability coupled with high current-sinking capability (48 mA), make the device useful for applications such as a decoder or differential line driver.

The SN54AS800 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS800 is characterized for operation from 0°C to 70°C.

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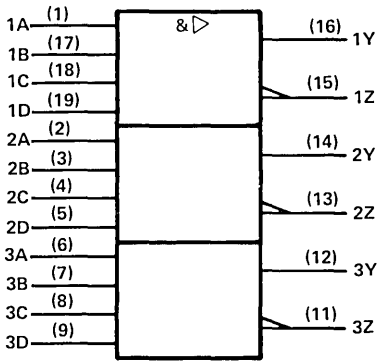
logic symbol



Pin numbers shown are for J and N packages.

positive logic: $Y = ABCD$
$Z = \overline{ABCD}$

absolute maximum ratings over free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS800 . . . . . −55°C to 125°C
SN74AS800 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS800			SN74AS800			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−40	mA
							−48†	mA
I_{OL}	Low-level output current			40			40	mA
							48†	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

† The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS800			SN74AS800			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA	2.4	3.2		2.4	3.2		V
	V_{CC} = 4.5 V, I_{OH} = −40 mA	2			2			V
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 40 mA		0.25	0.5		0.25	0.5	V
	V_{CC} = 4.75 V, I_{OL} = 48 mA					0.35	0.5	V
I_I	V_{CC} = 5.5 V, V_I = 7 V			100			100	μA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.4 V		−0.3			−0.3		mA
I_O§	V_{CC} = 5.5 V, V_O = 2.25 V		−150			−150		mA
I_{CC}	V_{CC} = 5.5 V		13			13		mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C

§The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			'AS800			SN54AS800			SN74AS800			
			MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A,B,C, or D	Z					3.5			3.5		ns
t_{PHL}							3.5			3.5		
t_{PLH}		Y					3			3		ns
t_{PHL}							4			4		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

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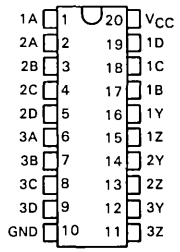
TYPES SN54AS802, SN74AS802
TRIPLE 4-INPUT OR/NOR LINE DRIVERS

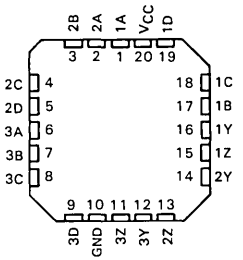
D2662, DECEMBER 1982

- True and Complementary Outputs
- High Capacitive Drive Capability
- 35% Improvement in AC Performance
- Current Sinking Capability Up to 48 mA
- Package Options Include Plastic and Ceramic DIPs as well as Both Plastic and Ceramic Chip Carriers
- Designed Specifically for Use in Applications such as:
  - Symmetrical Complementary Clock Generators
  - Complementary Input Circuit for Decoders and Code Converters
  - Differential Line Drivers
- Dependable Texas Instruments Quality and Reliability

SN54AS802 . . . . J PACKAGE
SN74AS802 . . . . N PACKAGE
(TOP VIEW)



SN54AS802 . . . . FH PACKAGE
SN74AS802 . . . . FN PACKAGE
(TOP VIEW)



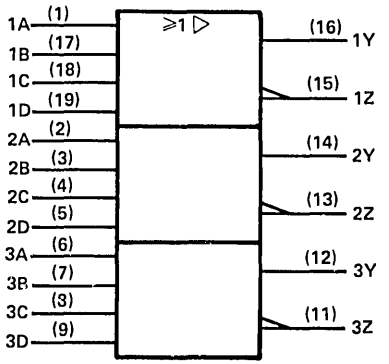
description

The 'AS802 is uniquely suitable for symmetrical complementary clock-generator applications due to the delay time in either function (OR/NOR) being typically 4 ns with less than 0.5 ns skew between the true and complementary outputs. Elimination of decode spikes in symmetrical decoder and code converter applications, and the high capacitive drive capability coupled with high current-sinking capability (48 mA), make the device useful for applications such as a decoder or differential line driver.

The SN54AS802 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS802 is characterized for operation from 0°C to 70°C.

PRODUCT PREVIEW
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

logic symbol



Pin numbers shown are for J and N packages.

positive logic: $Y = A + B + C + D$, $Z = \overline{A + B + C + D}$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS802 . . . . . −55°C to 125°C
SN74AS802 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS802			SN74AS802			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−40	mA
							−48†	mA
I_{OL}	Low-level output current			40			40	mA
							48†	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

† The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.

TEXAS INSTRUMENTS
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS802			SN74AS802			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA	2.4	3.2		2.4	3.2		V
	V_{CC} = 4.5 V, I_{OH} = −40 mA	2			2			V
	V_{CC} = 4.75 V, I_{OH} = −48 mA				2			V
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 40 mA		0.25	0.5		0.25	0.5	V
	V_{CC} = 4.75 V, I_{OL} = 48 mA					0.35	0.5	V
I_I	V_{CC} = 5.5 V, V_I = 7 V			100			100	μA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.4 V		−0.3			−0.3		mA
I_O§	V_{CC} = 5.5 V, V_O = 2.25 V		−150			−150		mA
I_{CC}	V_{CC} = 5.5 V		20			20		mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C

§The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			'AS802			SN54AS802			SN74AS802			
			MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A, B, C, D	Y					3.5			3.5		ns
t_{PHL}	A, B, C, D	Y					4.5			4.5		ns
t_{PLH}	A, B, C, D	Z					4			4		ns
t_{PHL}	A, B, C, D	Z					5			5		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

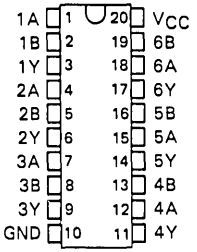
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TYPES SN54ALS804, SN54AS804A, SN74ALS804, SN74AS804A
HEX 2-INPUT NAND DRIVERS

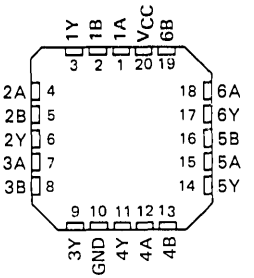
D2661, DECEMBER 1982

- High Capacitive Drive Capability
- 'ALS804 Has Typical Delay Time of 3 ns (C_L = 50 pF) and Typical Power Dissipation of 3.4 mW per Gate
- 'AS804A Has Typical Delay Time of 1.7 ns (C_L = 15 pF) and Typical Power Dissipation of Less than 9 mW per Gate
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS804, SN54AS804A . . . J PACKAGE
SN74ALS804, SN74AS804A . . . N PACKAGE
(TOP VIEW)



SN54ALS804, SN54AS804A . . . FH PACKAGE
SN74ALS804, SN74AS804A . . . FN PACKAGE
(TOP VIEW)



description

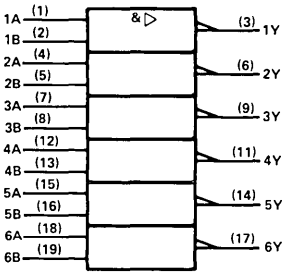
These devices contain six independent 2-input NAND drivers. They perform the boolean function $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54ALS804 and SN54AS804A are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS804 and SN74AS804A are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each driver)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol



Pin numbers shown are for J and N packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS804 . . . . . −55°C to 125°C
SN74ALS804 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS804			SN74ALS804			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS804			SN74ALS804			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.84			0.84		mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		7.2			7.2		mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS804			SN74ALS804			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y		3			3		ns
t_{PHL}				3			3		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

ADVANCE INFORMATION

This page contains information on a new product. Specifications are subject to change without notice.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS804A . . . . . −55°C to 125°C
SN74AS804A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS804A			SN74AS804A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40				mA
							−48	
I_{OL}	Low-level output current			40				mA
							48	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS804A			SN74AS804A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		V
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.05	−0.5		−0.05	−0.5	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V		−135			−135		mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		2.5	4		2.5	4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		16	27		16	27	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'AS804A	SN54AS804A		SN74AS804A		
			TYP‡	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.7	1	4.5	1	3.5	ns
t_{PHL}			1.6	1	4.5	1	3.5	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
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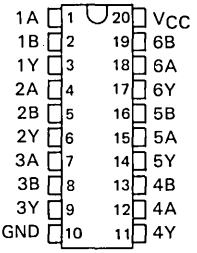
D2661, DECEMBER 1982

- **High Capacitive Drive Capability**
- **'ALS805 Has Typical Delay Time of 3.5 ns (C_L = 50 pF) and Typical Power Dissipation of 4.2 mW per Gate**
- **'AS805A Has Typical Delay Time of 1.7 ns (C_L = 15 pF) and Typical Power Dissipation of 12 mW per Gate**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS805, SN54AS805A . . . J PACKAGE
SN74ALS805, SN74AS805A . . . N PACKAGE
(TOP VIEW)

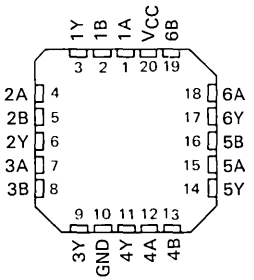


description

These devices contain six independent 2-input NOR drivers. They perform the boolean function $Y = \overline{A+B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN54ALS805 and SN54AS805A are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS805 and SN74AS805A are characterized for operation from 0 °C to 70 °C.

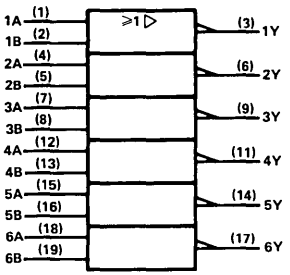
SN54ALS805, SN54AS805A . . . FH PACKAGE
SN74ALS805, SN74AS805A . . . FN PACKAGE
(TOP VIEW)



FUNCTION TABLE (each driver)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS805 . . . . . −55 °C to 125 °C
SN74ALS805 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

2

recommended operating conditions

		SN54ALS805			SN74ALS805			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS805			SN74ALS805			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		1.7			1.7		mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		8.4			8.4		mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS805			SN74ALS805			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y		3.4			3.4		ns
t_{PHL}				3.5			3.5		

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS805A . . . . . −55°C to 125°C
SN74AS805A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS805A			SN74AS805A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40				mA
							−48	
I_{OL}	Low-level output current			40				mA
							48	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS805A			SN74AS805A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		V
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.05	−0.5		−0.05	−0.5	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V		−135			−135		mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		5	9		5	9	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		18	32		18	32	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

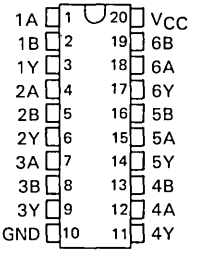
switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'AS805A	SN54AS805A		SN74AS805A		
			TYP‡	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.7	1	4.5	1	4	ns
t_{PHL}			1.6	1	4.5	1	4	

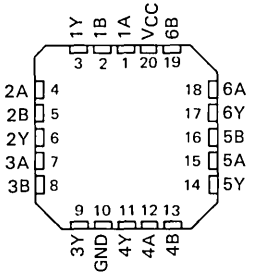
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- High Capacitive Drive Capability
- 'ALS808 Has Typical Delay Time of 4.3 ns (C_L = 50 pF) and Typical Power Dissipation of 4.5 mW per Gate
- 'AS808A Has Typical Delay Time of 2.5 ns (C_L = 15 pF) and Typical Power Dissipation of Less than 13 mW per Gate
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS808, SN54AS808A . . . J PACKAGE
SN74ALS808, SN74AS808A . . . N PACKAGE
(TOP VIEW)



SN54ALS808, SN54AS808A . . . FH PACKAGE
SN74ALS808, SN74AS808A . . . FN PACKAGE
(TOP VIEW)



description

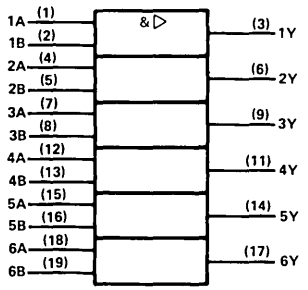
These devices contain six independent 2-input AND drivers. They perform the boolean function $Y = A \cdot B$ or $Y = \overline{\overline{A}+\overline{B}}$ in positive logic.

The SN54ALS808 and SN54AS808A are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS808 and SN74AS808A are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each driver)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol



Pin numbers shown are for J and N packages.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS808 . . . . . −55 °C to 125 °C
SN74ALS808 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS808			SN74ALS808			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS808			SN74ALS808			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		3.0			3.0		mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		7.8			7.8		mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS808			SN74ALS808			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y		4			4		ns
t_{PHL}				4.5			4.5		

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

ADVANCE INFORMATION

This page contains information on a new product. Specifications are subject to change without notice.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS808A . . . . . −55 °C to 125 °C
SN74AS808A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS808A			SN74AS808A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40				mA
							−48	
I_{OL}	Low-level output current			40				mA
							48	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS808A			SN74AS808A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		V
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.05	−0.5		−0.05	−0.5	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V		−135			−135		mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		6.5	11		6.5	11	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		19	32		19	32	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25 °C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'AS808A	SN54AS808A		SN74AS808A		
			TYP‡	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2.5	1	6	1	5	ns
t_{PHL}			2.4	1	6	1	5	

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

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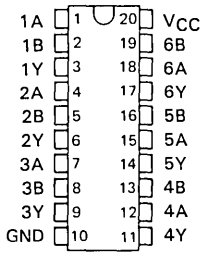
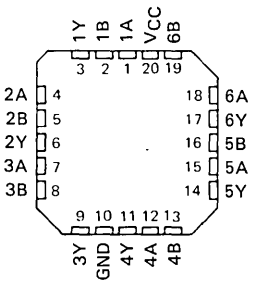
- High Capacitive Drive Capability
- 'ALS832 Has Typical Delay Time of 4 ns (C_L = 50 pF) and Typical Power Dissipation of 5.3 mW per Gate
- 'AS832A Has Typical Delay Time of 2.5 ns (C_L = 15 pF) and Typical Power Dissipation of Less than 17 mW per Gate
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS832, SN54AS832A . . . J PACKAGE
SN74ALS832, SN74AS832A . . . N PACKAGE
(TOP VIEW)



SN54ALS832, SN54AS832A . . . FH PACKAGE
SN74ALS832, SN74AS832A . . . FN PACKAGE
(TOP VIEW)



description

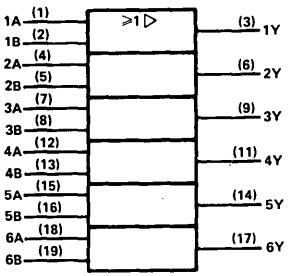
These devices contain six independent 2-input OR drivers. They perform the boolean function $Y = A+B$ or $Y = \overline{\overline{A}\cdot\overline{B}}$ in positive logic.

The SN54ALS832 and SN54AS832A are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS832 and SN74AS832A are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each driver)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS832 . . . . . −55°C to 125°C
SN74ALS832 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS832			SN74ALS832			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS832			SN74ALS832			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		4.2			4.2		mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		8.4			8.4		mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS832			SN74ALS832			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y		3			3		ns
t_{PHL}				5			5		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS832A . . . . . −55 °C to 125 °C
SN74AS832A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS832A			SN74AS832A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40				mA
							−48	
I_{OL}	Low-level output current			40				mA
							48	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS832A			SN74AS832A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		V
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.05	−0.5		−0.05	−0.5	mA
I_O §	V_{CC} = 5.5 V,	V_O = 2.25 V		−135			−135		mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		9	15		9	15	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		22	36		22	36	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

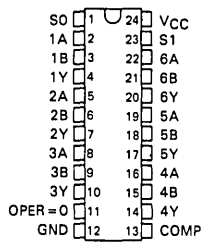
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25 °C 'AS832A	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
				SN54AS832A		SN74AS832A		
			TYP‡	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2.5	1	7	1	5.5	ns
t_{PHL}			2.4	1	6.5	1	5.5	

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2661, DECEMBER 1982

- **Selects True or Complementary Data**
- **Performs AND/NAND (masking) of A or B Operand**
- **Cascadable to Expand Number of Operands**
- **Detects Zeros on A or B Operands**
- **3-State Outputs Interface Directly with System Bus**
- **Included Among the Package Options Are 24-Pin, 300-Mil-Wide DIPs and Both 28-Pin Plastic and Ceramic Chip Carriers**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS857, SN54AS857 . . . JT PACKAGE
SN74ALS857, SN74AS857 . . . NT PACKAGE
(TOP VIEW)



SN54ALS857, SN54AS857 . . . FH PACKAGE
SN74ALS857, SN74AS857 . . . FN PACKAGE

For chip carrier information contact factory

description

The 'ALS857 and 'AS857 are hextuple 2-line to 1-line multiplexers with three-state outputs. The devices can provide either true (COMP low) or inverted (COMP high) data at the Y outputs. In addition, the 'ALS857 and 'AS857 perform the logical AND function (A·B) and the clear function as well. The four modes of operation are:

Select A data inputs,
Select B data inputs,
AND A inputs with B inputs,
Clear

In either of the first two modes, OPER = 0 is high if all the selected A or B inputs are low.

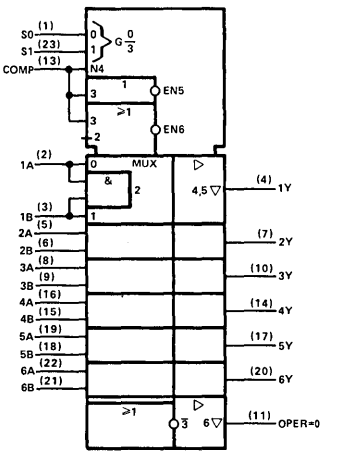
The six Y outputs and the OPER = 0 output are all three-state and rated at 12 mA and 24 mA I_{OL} for the SN54ALS857 and SN74ALS857, respectively, and at 32 mA and 48 mA I_{OL} for the SN54AS857 and SN74AS857, respectively. All outputs can be placed into the high-impedance state by applying a high level to the COMP, S0, and S1 inputs simultaneously. The complete function table is shown below.

The SN54ALS857 and SN54AS857 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS857 and SN74AS857 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE

COMP	S1	S0	Y OUTPUTS	OPER = ZERO
L	L	L	A	H = all A inputs L
L	L	H	B	H = all B inputs L
L	H	L	A·B	Z
L	H	H	L	L
H	L	L	$\overline{A}$	H = all A inputs L
H	L	H	$\overline{B}$	H = all B inputs L
H	H	L	$\overline{A \cdot B}$	Z
H	H	H	Z	Z

logic symbol



Pin numbers shown are for JT and NT packages.

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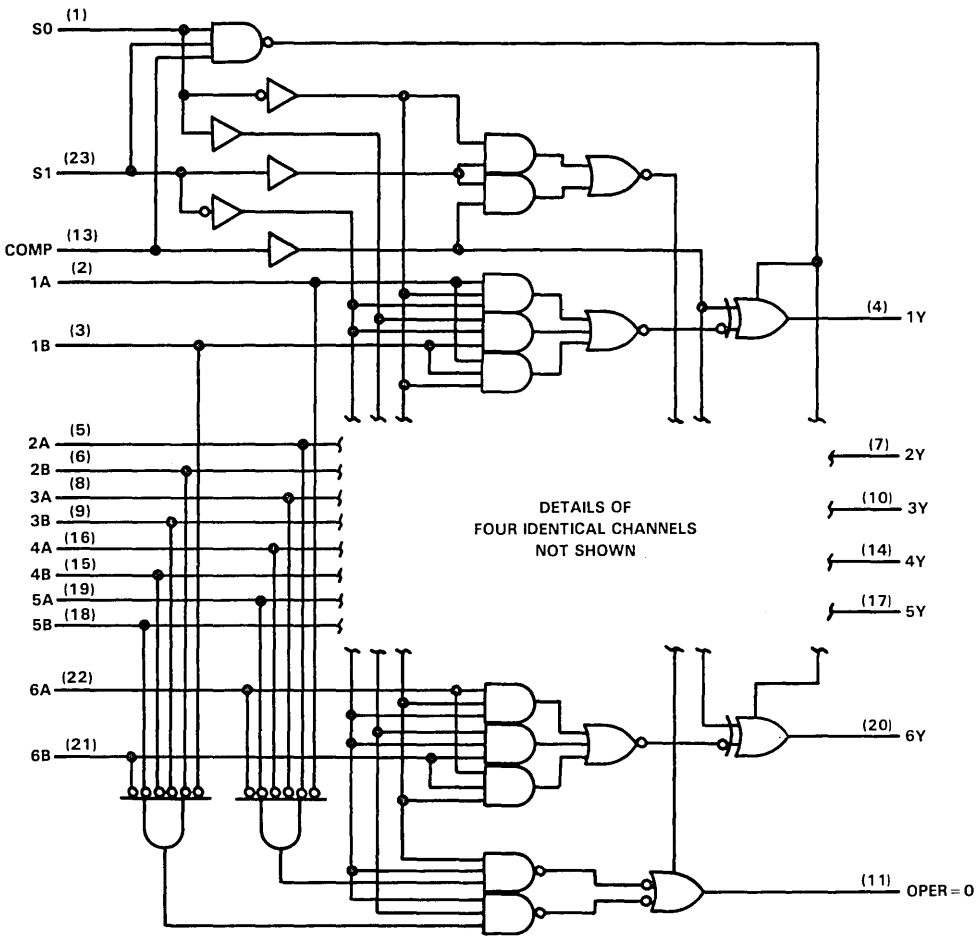
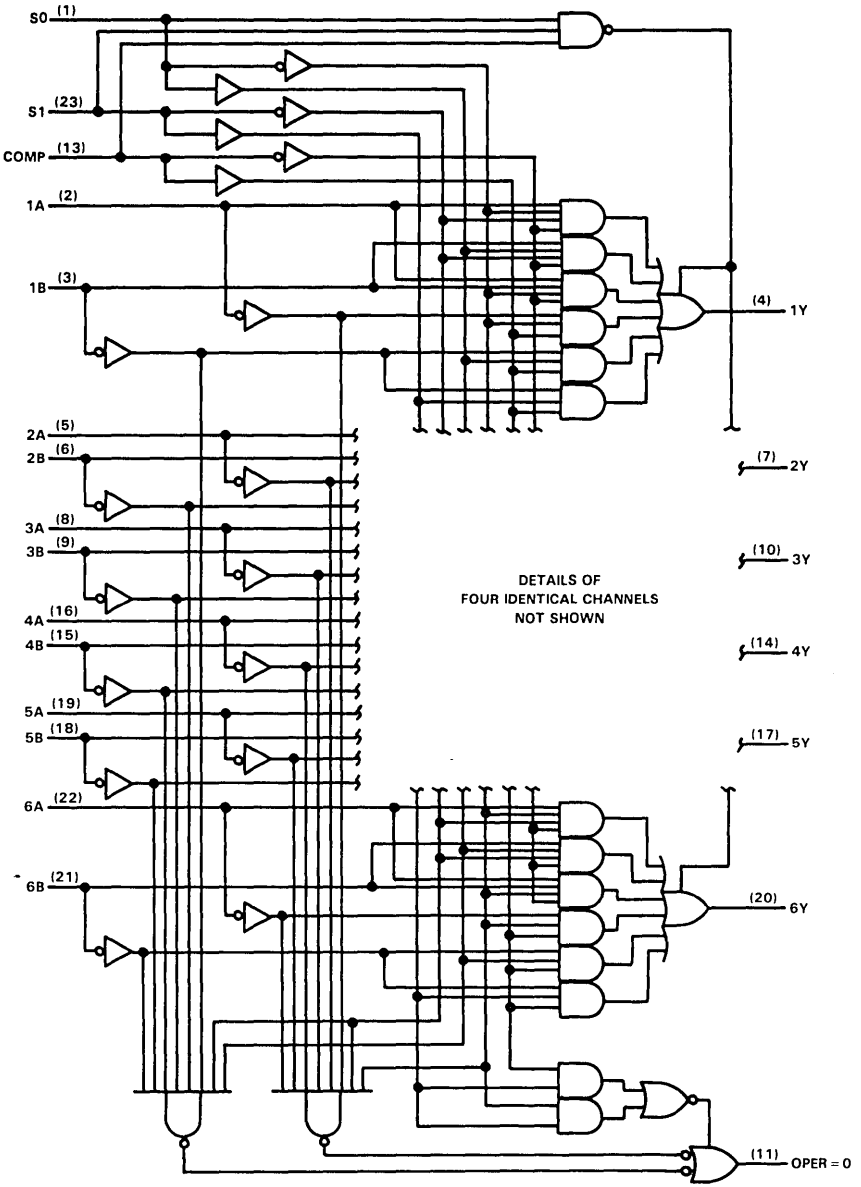
'ALS857 logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

'AS857 logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS857 . . . . . −55°C to 125°C
SN74ALS857 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS857			SN74ALS857			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							−24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS857			SN74ALS857			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	V_{CC} = 5.5 V, See Note 1	Outputs high		11	24		11	24	mA
		Outputs low		16	33		16	33	
		Outputs disabled		18	36		18	36	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with all possible inputs grounded while achieving the stated output conditions.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS857		SN74ALS857		
			MIN	MAX	MIN	MAX	
t_{pd}	A or B (COMP high)	Y (Inverting)	4	18	4	14	ns
t_{pd}	A or B (COMP low)	Y (Noninverting)	4	18	4	14	ns
t_{pd}	S0 or S1	Y	7	37	7	33	ns
t_{pd}	COMP	Y	6	22	6	18	
t_{pd}	A or B	OPER=0	5	45	5	37	
t_{pd}	S0 or S1	OPER=0	5	30	5	23	
t_{en}	S0 or S1	Y	7	38	7	35	ns
t_{dis}			2	29	2	23	
t_{en}	COMP	Y	8	27	8	24	ns
t_{dis}			6	27	6	21	
t_{en}	S0	OPER=0	6	24	6	20	ns
t_{dis}			11	34	11	27	
t_{en}	S1	OPER=0	6	28	6	25	ns
t_{dis}			3	23	3	19	
t_{en}	COMP	OPER=0	9	30	9	25	ns
t_{dis}			6	24	6	20	

$t_{pd} = t_{PLH}$ or t_{PHL}
$t_{en} = t_{PZH}$ or t_{PZL}
$t_{dis} = t_{PHZ}$ or t_{PLZ}
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS857 . . . . . −55 °C to 125 °C
SN74AS857 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54AS857			SN74AS857			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	Y Outputs			−12			−12	mA
								−15†	
		OPER=0			−2			−2	
I_{OL}	Low-level output current	Y Outputs			32			32	mA
								48†	
		OPER=0			20			20	
T_A	Operating free-air temperature		−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS857			SN74AS857			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	Y Outputs	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2		2.4	3.2		V
		V_{CC} = 4.75 V,	I_{OH} = −15 mA				2.4	3.3		
	OPER=0	V_{CC} = 4.5 V,	I_{OH} = −2 mA	2.5	3.4		2.5	3.4		
		V_{CC} = 4.75,	I_{OH} = −2 mA				2.7	3.4		
V_{OL}	Y Outputs	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.35	0.5		0.35	0.5	V
		V_{CC} = 4.75 V,	I_{OL} = 48 mA					0.35	0.5	
	OPER=0	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−2			−2	mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V, See Note 1	Outputs high							mA
			Outputs low							
			Outputs disabled							

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with all possible inputs grounded while achieving the stated output conditions.

Additional information on these products can be obtained from the factory as it becomes available.

PRODUCT PREVIEW

This page contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

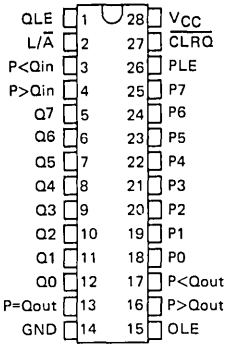
switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS857			SN74AS857			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	A or B (COMP high)	Y (Inverting)		5.5			5.5		ns
t_{pd}	A or B (COMP low)	Y (Noninverting)		4.5			4.5		ns
t_{pd}	S0 or S1	Y		7			7		ns
t_{pd}	COMP	Y		7			7		
t_{pd}	A or B	OPER = 0		7			7		
t_{pd}	S0 or S1	OPER = 0		7.5			7.5		
t_{en}	S0 or S1	Y		5			5		ns
t_{dis}				4.5			4.5		
t_{en}	COMP	Y		5			5		ns
t_{dis}				5			5		
t_{en}	S0	OPER = 0		9			9		ns
t_{dis}				8			8		
t_{en}	S1	OPER = 0		9			9		ns
t_{dis}				7			7		
t_{en}	COMP	OPER = 0		9			9		ns
t_{dis}				8			8		

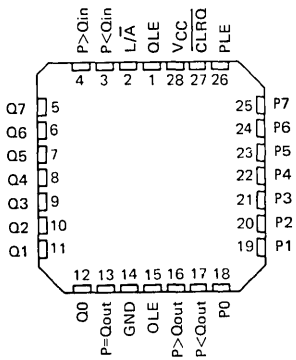
$t_{pd} = t_{PLH}$ or t_{PHL}
$t_{en} = t_{PZH}$ or t_{PZL}
$t_{dis} = t_{PHZ}$ or t_{PLZ}
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- Included among the Package Options Are 28-Pin DIPs and Both Plastic and Ceramic Chip Carriers
- Input and Output Latches with Active-High Enables
- Fast Compare to Zero
- Arithmetic and Logical Comparison
- Open-Collector P = Q Output
- Dependable Texas Instruments Quality and Reliability

SN54AS866 . . . JD PACKAGE
SN74AS866 . . . N PACKAGE
(TOP VIEW)



SN54AS866 . . . FH PACKAGE
SN74AS866 . . . FN PACKAGE
(TOP VIEW)



description

These Advanced Schottky devices are capable of performing high-speed arithmetic or logical comparisons on two 8-bit binary or two's complement words. Three fully decoded decisions about words P and Q are externally available at the outputs. These devices are fully expandable to any word length by connecting the totem pole P > Q and P < Q outputs of each stage to the P > Q and P < Q inputs of the next higher-order stage. The cascading paths are implemented with only a two-gate-level delay to reduce overall comparison times for long words. The open-collector P = Q outputs may be wire-ANDed together.

Both input words P and Q plus all three outputs (P > Q, P < Q, and P = Q) are equipped with latches to provide the designer with temporary data storage for avoiding race conditions. The enable circuitry is implemented with minimal delay times to enhance performance when the devices are cascaded for longer word lengths. Each latch is transparent when the appropriate latch enable, PLE, QLE, or OLE is high.

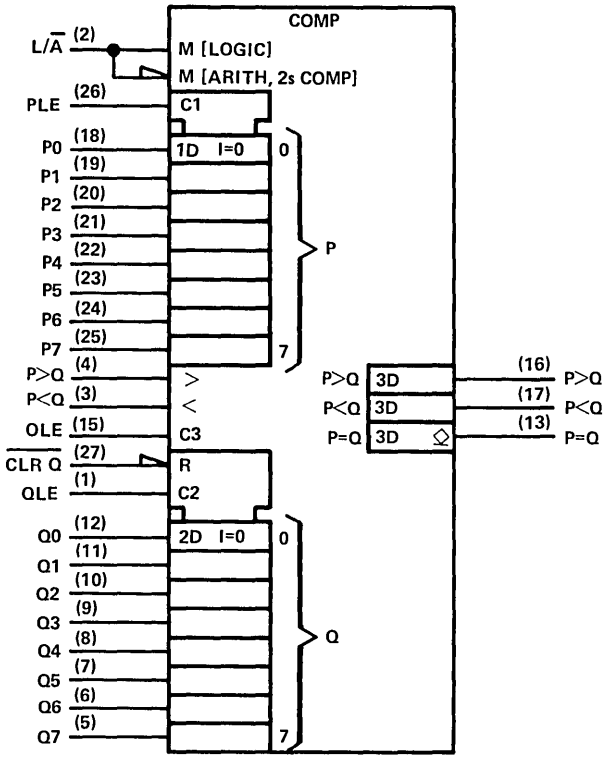
The enable inputs PLE and QLE and data inputs P and Q utilize p-n-p input transistors to reduce the low-level input current requirement to typically −0.25 mA, which minimizes loading effects.

The Q register may be cleared to zero for a fast comparison of the P word to zero.

The SN54AS866 is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74AS866 is characterized for operation from 0 °C to 70 °C.

2

logic symbol



Pin numbers shown are for JD and N packages.

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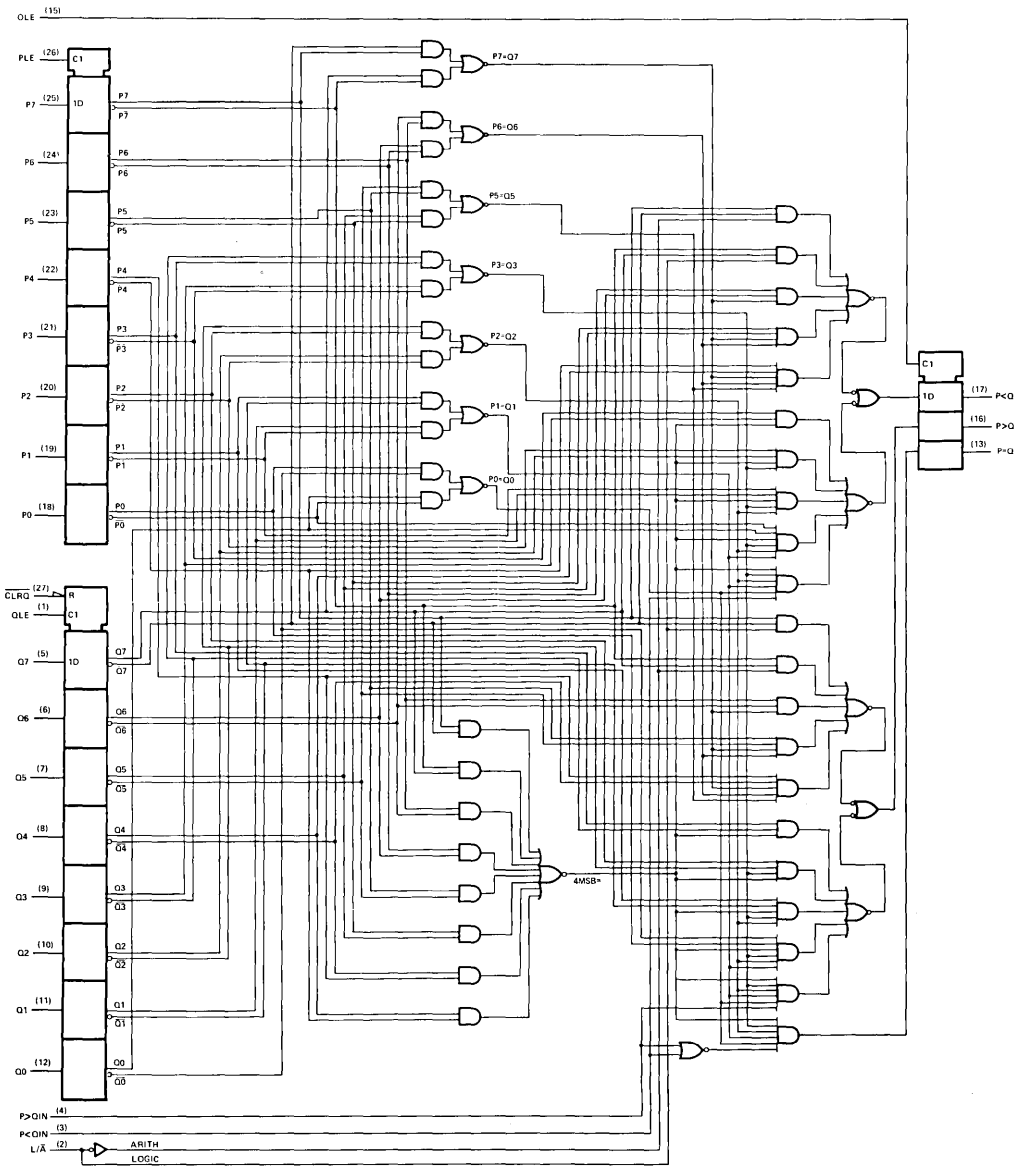
logic diagram (positive logic)



FUNCTION TABLE

COMPARISON	L/$\overline{A}$	DATA INPUTS P0-P7, Q0-Q7	INPUTS		OUTPUTS		
			P > Q	P < Q	P > Q	P < Q	P = Q
Logical	H	P > Q	X	X	H	L	L
Logical	H	P < Q	X	X	L	H	L
Logical	H	P = Q	L	L	L	L	H
Logical	H	P = Q	L	H	L	H	L
Logical	H	P = Q	H	L	H	L	L
Logical	H	P = Q	H	H	H	H	L
Arithmetic	L	P AG Q	X	X	H	L	L
Arithmetic	L	Q AG P	X	X	L	H	L
Arithmetic	L	P = Q	L	L	L	L	H
Arithmetic	L	P = Q	L	H	L	H	L
Arithmetic	L	P = Q	H	L	H	L	L
Arithmetic	L	P = Q	H	H	H	H	L

AG = arithmetically greater than

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage, P = Q output . . . . . 7 V
Operating free-air temperature range: SN54AS866 . . . . . −55 °C to 125 °C
SN74AS866 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

PARAMETER		SN54AS866			SN74AS866			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current, all outputs except P = Q			−2			−2	mA
V_{OH}	High-level output voltage, P = Q output			5.5			5.5	V
I_{OL}	Low-level output current			20			20	mA
t_{su}	Setup time to PLE, QLE, OLE↓	2			2			ns
t_h	Hold time after PLE, QLE, OLE↓	4			4			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS866			SN74AS866			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	P > Q, P < Q	V_{CC} = 4.5 V,	I_{OH} = −2 mA	2.5	3.4		2.5	3.4		V
		V_{CC} = 4.75 V,	I_{OH} = −2 mA				2.7	3.4		
I_{OH}	P = Q only	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			250			250	μA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	L/$\overline{A}$, OLE	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	Others					20			20	
I_{IL}	L/$\overline{A}$, OLE, P > Qin, P < Qin	V_{CC} = 5.5 V,	V_I = 0.4 V			−4			−4	mA
	$\overline{CLRQ}$					−2			−2	
	P, Q, PLE, QLE				−0.25	−1		−0.25	−1	
I_O‡		V_{CC} = 5.5 V	V_O = 2.25 V	−20		−115	−20		−115	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		160	240		160	240	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit, I_{OS}.
NOTE 1: I_{CC} is measured with all inputs high except L/$\overline{A}$, which is low.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			'AS866			SN54AS886			SN74AS866			
			MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	L/$\overline{A}$	P < Q, P > Q		6.5			8.5	14		8.5	13	ns
t_{PHL}				7.5			7.5	14		7.5	13	
t_{PLH}	P < Q, P > Q			4.5			5	10		5	8	ns
t_{PLH}				4.5			5.5	10		5.5	8	
t_{PHL}	Any P or Q Data Input			11.5			13.5	21		13.5	17.5	ns
t_{PHL}				9.5			10	17		10	15	
t_{PLH}	$\overline{CLRQ}$			6.5			16	21		16	20	ns
t_{PHL}				5.5			12	17		12	16	

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 280 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 280 Ω, T_A = MIN to MAX						UNIT
			'AS866			SN54AS886			SN74AS866			
			MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	P < Q, P > Q	P = Q		6.5			6.5	12		6.5	11	ns
t_{PHL}				5.5			8	14		8	13	
t_{PLH}	Any P or Q Data Input	P = Q		10			10	15		10	14	ns
t_{PHL}				9			9	14		9	13	
t_{PLH}	$\overline{CLRQ}$	P = Q		10			12	17		12	16	ns
t_{PHL}				11			13	18		13	17	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: For load circuit and voltage waveforms, see page 1-12.

TYPICAL APPLICATION DATA

This sequence of comparisons illustrates how the $\overline{CLRQ}$ function can be used to perform dual comparisons of the varying P terms (P0, P1, etc). When $\overline{CLRQ}$ is high, the P term is compared to the Q term. When $\overline{CLRQ}$ is taken low, the P term is compared to zero. This or similar sequences can enhance performance and reduce package count to perform value range checks.

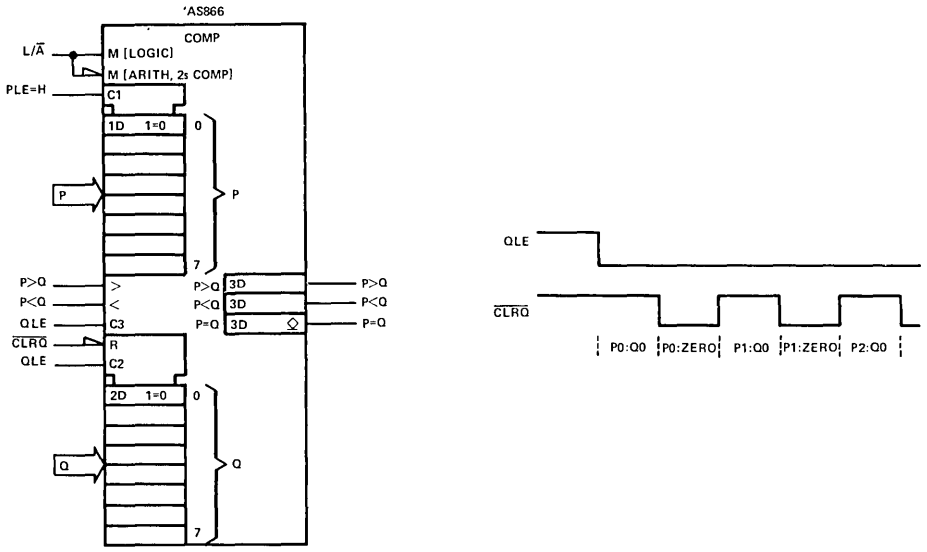

FIGURE 1 – MAGNITUDE COMPARISONS COMBINED WITH QUICK COMPARISONS TO ZERO (RANGE VERIFICATIONS)

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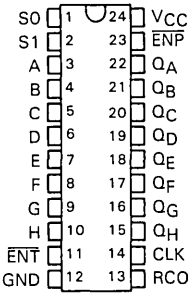
TYPES SN54AS867, SN54AS869, SN74AS867, SN74AS869
SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

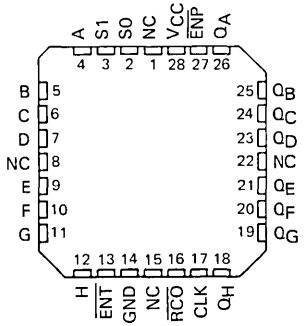
D2661, DECEMBER 1982

- Included among the Package Options Are Compact, 24-Pin, 300-mil-Wide Dips and Both 28-Pin Plastic and Ceramic Chip Carriers
- Fully Programmable with Synchronous Counting and Loading
- 'AS867 Has Asynchronous Clear, 'AS869 Has Synchronous Clear
- Fully Independent Clock Circuit Simplifies Use — Hold Times Not Required
- Ripple Carry Output for n-Bit Cascading
- Improved Performance Compared to Schottky TTL:
  - Typical Power Reduced by 38%
  - Maximum Count Frequency Is 25% Higher
- Dependable Texas Instruments Quality and Reliability

SN54AS867, SN54AS869 . . . . JT PACKAGE
SN74AS867, SN74AS869 . . . . NT PACKAGE
(TOP VIEW)



SN54AS867, SN54AS869 . . . . FH PACKAGE
SN74AS867, SN74AS869 . . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the eight flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load mode circuitry allows parallel loading of the cascaded counters. As loading is synchronous, selecting the load mode disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{ENP}$ and $\overline{ENT}$) must be low to count. The direction of the count is determined by the levels of the select inputs (see Function Table). Input $\overline{ENT}$ is fed forward to enable the carry output. The ripple carry output thus enabled will produce a low-level pulse while the count is zero (all inputs low) counting down or 255 counting up. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable $\overline{ENP}$ and $\overline{ENT}$ inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

PRODUCT PREVIEW

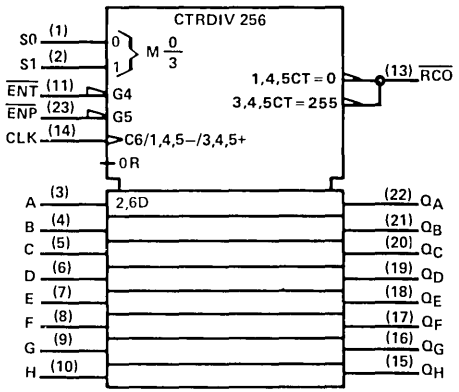
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

These counters feature a fully independent clock circuit. With the exception of the asynchronous clear on the 'AS867, changes at control inputs (S0, S1) that will modify the operating mode have no effect on the outputs until clocking occurs. Anytime the $\overline{ENP}$ and/or $\overline{ENT}$ is taken high, $\overline{RCO}$ will either go or remain high. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

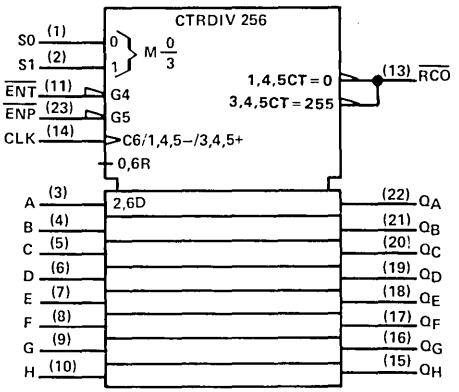
The SN54AS867 and SN54AS869 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS867 and SN74AS869 are characterized for operation from 0°C to 70°C.

logic symbols

'AS867



'AS869



Pin numbers shown are for JT and NT packages.

FUNCTION TABLE

S1	S0	FUNCTION
L	L	Clear
L	H	Count down
H	L	Load
H	H	Count up

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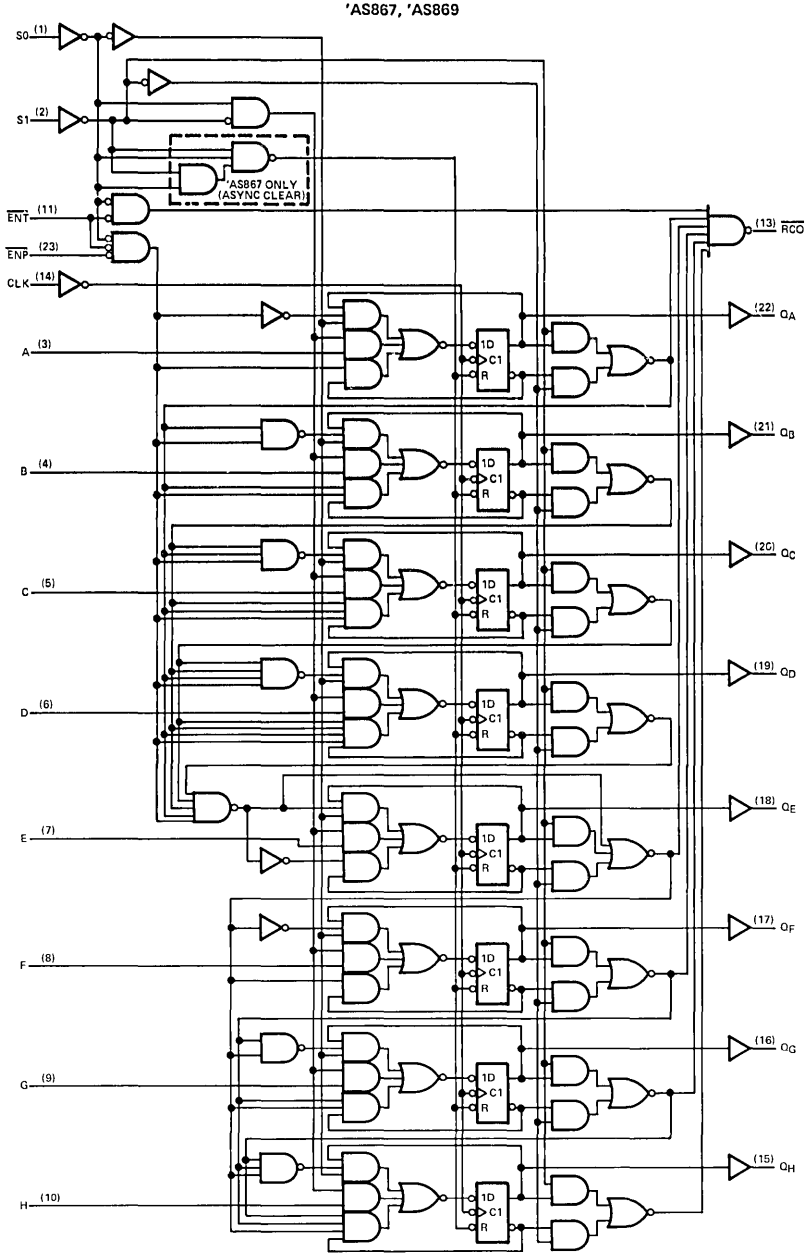
logic diagram (positive logic)

'AS867, 'AS869



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS867, SN54AS869 . . . . . −55°C to 125°C
SN74AS867, SN74AS869 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions.

			SN54AS867 SN54AS869			SN74AS867 SN74AS869			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		50	0		50	MHz
$t_{w(clock)}$	Duration of clock pulse		10			10			ns
$t_{w(clear)}$	Duration of clear pulse (S0 and S1 low)								ns
t_{su}	Setup time†	Data inputs A-H							ns
		Enable P ($\overline{ENP}$) or Enable T ($\overline{ENT}$)							ns
		S0 or S1 (load)							ns
		S0 or S1 (clear) ('AS869)							ns
		S0 or S1 (count down)							ns
		S0 or S1 (count up)							ns
t_h	Hold time at any input with respect to clock†		0			0			ns
t_{skew}	Skew time between S0 and S1 (maximum to avoid inadvertent clear)								ns
T_A	Operating free-air temperature		−55		−125	0		70	°C

Additional information on these products can be obtained from the factory as it becomes available.

TEXAS INSTRUMENTS
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54AS867 SN54AS869			SN74AS867 SN74AS869			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V, I_{OH} = −2 mA	2.5	3.4		2.5	3.4		V
		V_{CC} = 4.75 V, I_{OH} = −2 mA				2.7	3.4		
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 20 mA		0.34	0.5		0.34	0.5	V
I_I		V_{CC} = 5.5 V, V_I = 7 V			100			100	μA
I_{IH}	$\overline{ENT}$	V_{CC} = 5.5 V, V_I = 2.7 V			40			40	μA
	Other inputs				20			20	μA
I_{IL}	$\overline{ENT}$	V_{CC} = 5.5 V, V_I = 0.4 V			−4			−4	mA
	Other inputs				−2			−2	mA
I_O§		V_{CC} = 5.5 V, V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS867	V_{CC} = 5 V		134			134		mA
	'AS869			125			125		mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			'AS867, 'AS869			SN54AS'			SN74AS'			
			MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}						50	63		50	63		MHz
t_{PLH}	CLK	$\overline{RCO}$					11			11		ns
t_{PHL}							13			13		ns
t_{PLH}	CLK	Any Q					7.5			7.5		ns
t_{PHL}							9.5			9.5		ns
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$					7			7		ns
t_{PHL}							12			12		ns
t_{PHL}‡	Clear (S0, S1 low)	Any Q					12			12		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Applicable to 'AS867 only.
NOTE1: For load circuit and voltage waveforms, see page 1-12.

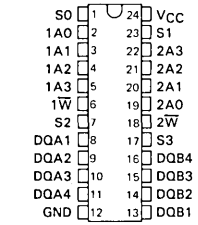
- 'AS870 in Compact 24-Pin, 300-mil DIP and Both Plastic and Ceramic 28-Pin Chip Carriers
- 'AS871 in 28-Pin 600-mil DIP and Both Plastic and Ceramic Chip Carriers
- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Typical Access Time Is 11 ns
- Each Register File Has Individual Write Enable Controls and Address Lines
- Designed Specifically for Multibus Architecture and Overlapping File Operations
- Prioritized B Input Port Prevents Write Conflicts During Dual Input Mode
- Dependable Texas Instruments Quality and Reliability

description

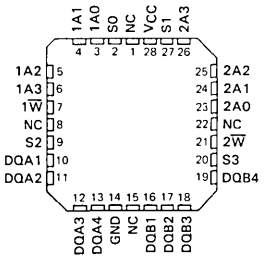
These devices feature two 16-word by 4-bit register files. Each register file has individual write-enable controls and address lines. The 'AS870 has two 4-bit data I/O ports (DQA1-DQA4 and DQB1-DQB4). The 'AS871 has one 4-bit data I/O port (DQB1-DQB4) with the other data port having individual data inputs (DA1-DA4) and data outputs (QA1-QA4). The data I/O ports can output to Bus A and Bus B, receive input from Bus A and Bus B, receive input from Bus A and output to Bus B, or output to Bus A and receive input from Bus B. To prevent writing conflicts in the dual-input mode, the B input port takes priority. Two select lines, S0 and S1, control which port has access to which register. S2 determines whether the A ports are in the input or the output modes and S3 does likewise for the B ports. The address lines (IA0-IA3 or 2A0-2A3) are decoded by an internal 1-of-16 decoder to select which register word is to be accessed. All outputs are 3-state buffer-type outputs designed specifically to drive bus lines directly.

The SN54AS870 and SN54AS871 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS870 and SN74AS871 are characterized for operation from 0°C to 70°C.

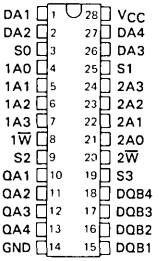
SN54AS870 . . . . JT PACKAGE
SN74AS870 . . . . NT PACKAGE
(TOP VIEW)



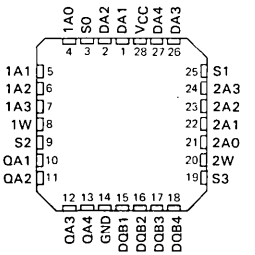
SN54AS870 . . . . FH PACKAGE
SN74AS870 . . . . FN PACKAGE
(TOP VIEW)



SN54AS871 . . . . JD PACKAGE
SN74AS871 . . . . N PACKAGE
(TOP VIEW)



SN54AS871 . . . . FH PACKAGE
SN74AS871 . . . . FN PACKAGE
(TOP VIEW)



NC — No internal connections

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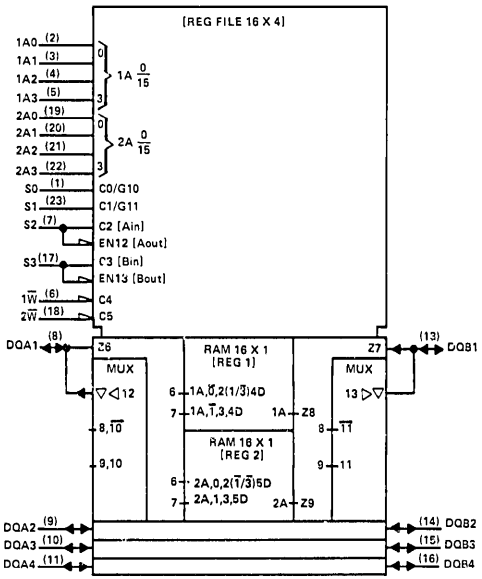
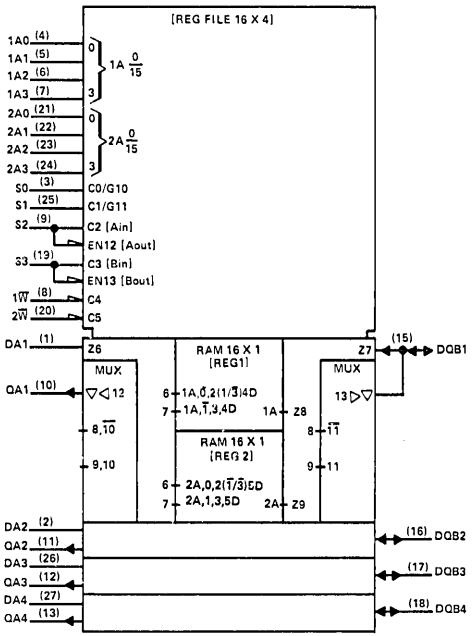
logic symbols

'AS870



'AS871



Pin numbers shown are for JD, JT, N, and NT packages.

FUNCTION TABLE

FILE SELECT			INPUT/OUTPUT		
S0	S1	FILE SEL	S2	S3	I/O SEL
L	L	1R TO A, 1R TO B	L	L	A OUT, B OUT
H	L	2R TO A, 1R TO B			
L	H	1R TO A, 2R TO B			
H	H	2R TO A, 2R TO B			
L	L	A TO 1R, 1R TO B	H	L	A IN, B OUT
H	L	A TO 2R, 1R TO B			
L	H	A TO 1R, 2R TO B			
H	H	A TO 2R, 2R TO B			
L	L	1R TO A, B TO 1R	L	H	A OUT, B IN
H	L	2R TO A, B TO 1R			
L	H	1R TO A, B TO 2R			
H	H	2R TO A, B TO 2R			
L	L	B TO 1R	H	H	A IN, B IN
H	L	A TO 2R, B TO 1R			
L	H	A TO 1R, B TO 2R			
H	H	B TO 2R			

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS870, SN54AS871 . . . . . −55 °C to 125 °C
SN74AS870, SN74AS871 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54AS870, SN54AS871			SN74AS870, SN74AS871			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−12	mA
								−15†	
I_{OL}	Low-level output current				32			32	mA
								48†	
t_w	Duration of write pulse								ns
t_{su}	Setup times	Address before write↑							ns
		Data before write↑							
		Select before write↑							
t_h	Hold times	Address after write↑							ns
		Data after write↑							
		Select after write↑							
T_A	Operating free-air temperature		−55		125	0		70	°C

† The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.

Additional information on these products can be obtained from the factory as it becomes available.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

'AS870 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54AS870			SN74AS870			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V, I_{OH} = −12 mA	2.4	3.2		2.4	3.2		V
		V_{CC} = 4.75 V, I_{OH} = −15 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 32 mA		0.25	0.5		0.25	0.5	V
		V_{CC} = 4.75 V, I_{OL} = 48 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V, V_I = 7 V			0.1			0.1	mA
	DQA and DQB ports	V_{CC} = 5.5 V, V_I = 5.5 V			0.2			0.2	
I_{IH}	W1 and W2	V_{CC} = 5.5 V, V_I = 2.7 V			20			20	µA
	Other control inputs				40			40	
	DQA and DQB ports ▲				70			70	
I_{IL}	Control inputs	V_{CC} = 5.5 V, V_I = 0.4 V		−0.1	−2		−0.1	−2	mA
	DQA and DQB ports ▲				−2			−2	
I_O§		V_{CC} = 5.5 V, V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V		125			125		mA

'AS871 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54AS871			SN74AS871			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V, I_{OH} = −12 mA	2.4	3.2		2.4	3.2		V
		V_{CC} = 4.75 V, I_{OH} = −15 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 32 mA		0.25	0.5		0.25	0.5	V
		V_{CC} = 4.75 V, I_{OL} = 48 mA					0.35	0.5	
I_{OZH}	QA outputs	V_{CC} = 5.5 V, V_O = 2.7 V			50			50	µA
I_{OZL}	QA outputs	V_{CC} = 5.5 V, V_O = 0.4 V			−50			−50	µA
I_I	Control and DA inputs	V_{CC} = 5.5 V, V_I = 7 V			0.1			0.1	mA
	DQB ports	V_{CC} = 5.5 V, V_I = 5.5 V			0.2			0.2	
I_{IH}	W1 and W2	V_{CC} = 5.5 V, V_I = 2.7 V			20			20	µA
	Other control and DA inputs				40			40	
	DQB ports				70			70	
I_{IL}	Control and DA inputs	V_{CC} = 5.5 V, V_I = 0.4 V		−0.1	−2		−0.1	−2	mA
	DQB ports				−2			−2	
I_O§		V_{CC} = 5.5 V, V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V		125			125		mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.
▲ For I/O ports, the parameters I_{IH} and I_{IL} include the output currents I_{OZH} and I_{OZL}, respectively.

2

'AS870 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			'AS870			SN54AS870			SN74AS870			
			MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A)}$	Any A	Any DQ					12			12		ns
$t_{a(S)}$	S0	Any DQA					10			10		ns
	S1	Any DQB					10			10		
t_{dis}	S2	Any DQA					5			5		ns
	S3	Any DQB					5			5		
t_{en}	S2	Any DQA					12			12		ns
	S3	Any DQB					12			12		
t_{pd}	$\overline{W}$	Any DQ					15			15		ns
	DQA	DQB					15			15		
	DQB	DQA					15			15		

'AS871 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			'AS871			SN54AS871			SN74AS871			
			MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A)}$	Any A	Any QA or DQB					12			12		ns
$t_{a(S)}$	S0	Any QA					10			10		ns
	S1	Any DQB					10			10		
t_{dis}	S2	Any QA					5			5		ns
	S3	Any DQB					5			5		
t_{en}	S2	Any QA					12			12		ns
	S3	Any DQB					12			12		
t_{pd}	$\overline{W}$	Any QA or DQB					15			15		ns
	DA	DQB					15			15		
	DQB	QA					15			15		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available

TEXAS INSTRUMENTS
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D2661, APRIL 1982

- 3-State Buffer-Type Outputs Drive Bus-Lines Directly
- Bus-Structured Pinout
- 'ALS880 and 'AS880 Are Alternative Versions with Inverting Outputs
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These dual 4-bit registers feature three-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

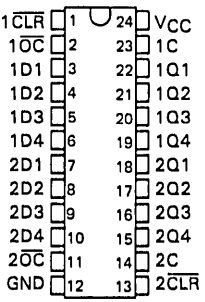
The dual 4-bit latches are transparent D-type. While the latch enable input (1C or 2C) is high, the Q outputs will follow the data (D) inputs in true form, according to the function table. When the latch enable input is taken low, the outputs will be latched. When $\overline{CLR}$ goes low, the Q outputs go low independently of the clock. The outputs are in a high-impedance state when $\overline{OC}$ (output control) is at a high logic level.

The SN54ALS873 and SN54AS873 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS873 and SN74AS873 are characterized for operation from 0 °C to 70 °C.

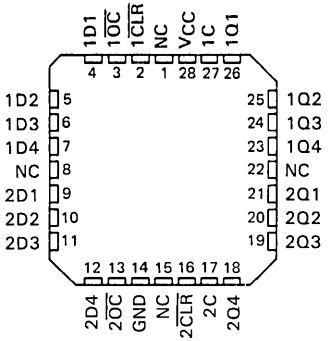
FUNCTION TABLE (EACH LATCH)

INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	ENABLE C	D	Q
L	L	X	X	L
L	H	H	H	H
L	H	H	L	L
L	H	L	X	Q_0
H	X	X	X	Z

SN54ALS873, SN54AS873 . . . JT PACKAGE
SN74ALS873, SN74AS873 . . . NT PACKAGE
(TOP VIEW)

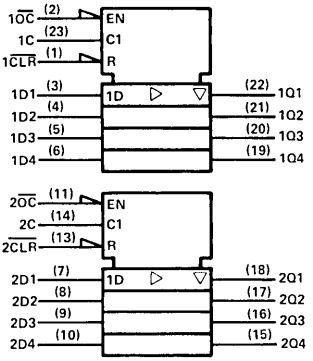


SN54ALS873, SN54AS873 . . . FH PACKAGE
SN74ALS873, SN74AS873 . . . FN PACKAGE
(TOP VIEW)

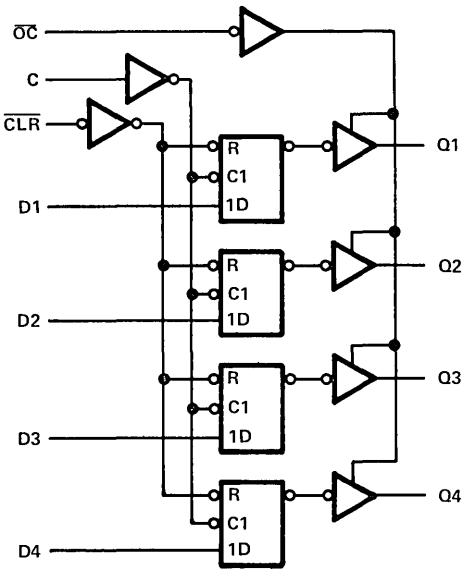


NC — No internal connection

logic symbol



functional block diagram (each quad latch, positive logic)



Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS873, SN54AS873 . . . . . −55 °C to 125 °C
SN74ALS873, SN74AS873 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

			SN54ALS873			SN74ALS873			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1				mA
								−2.6	
I_{OL}	Low-level output current				12				mA
								24	
t_w	Pulse duration	CLR low	15			15			ns
		Enable C high	10			10			
t_{su}	Setup time, data before enable C↓		10			10			ns
t_h	Hold time, data after enable C↓		7			7			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS873			SN74ALS873			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		10	21		10	21	mA
		Outputs low		15	29		15	29	
		Outputs disabled		16	31		16	31	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

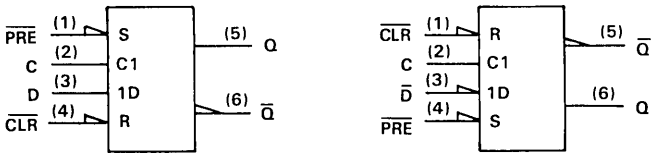
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS873			SN74ALS873			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	D	Q	2		15	2		14	ns
t_{PHL}			2		15	2		14	
t_{PLH}	C	Q	8		29	8		22	ns
t_{PHL}			8		22	8		21	
t_{PHL}	$\overline{CLR}$	Q	6		24	6		24	ns
t_{PZH}	$\overline{OC}$	Q	4		21	4		18	ns
t_{PZL}			4		21	4		18	
t_{PHZ}	$\overline{OC}$	Q	2		10	2		8	ns
t_{PLZ}			2		15	2		13	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D latch signal conventions

It is TI practice to name the outputs and other inputs of a D-type latch and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.



Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (⏥) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input D, but now both are considered active-low.

TEXAS INSTRUMENTS
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recommended operating conditions

			SN54AS873			SN74AS873			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−12	mA
								−15†	
I_{OL}	Low-level output current				32			32	mA
								48†	
t_w	Pulse duration	$\overline{CLR}$ low							ns
		Enable C high							
t_{su}	Setup time, data before enable C↓								ns
t_h	Hold time, data after enable C↓								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS873			SN74AS873			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2		2.4	3.2		V
	V_{CC} = 4.75 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5		0.25	0.5	V
	V_{CC} = 4.75 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.2			−0.2		mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high							mA
		Outputs low							
		Outputs disabled		80			80		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX					UNIT
			'AS873	SN54AS873			SN74AS873		
			TYP‡	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	D	Q			4.5			4.5		ns
t_{PHL}					4			4		
t_{PLH}	C	Q			7			7		ns
t_{PHL}					5			5		
t_{PHL}	$\overline{CLR}$	Q			6			6		ns
t_{PZH}	$\overline{OC}$	Q			3.5			3.5		ns
t_{PZL}					5			5		
t_{PHZ}	$\overline{OC}$	Q			3.5			3.5		ns
t_{PLZ}					5.5			5.5		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Choice of True or Inverting Logic**

'ALS874, 'AS874	True Outputs
'ALS876, 'AS876	Inverting Outputs

- **Asynchronous Clear**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

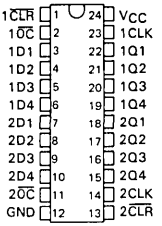
description

These dual four-bit registers feature three-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

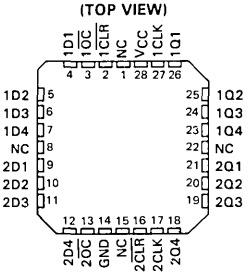
The edge-triggered flip-flops enter data on the low-to-high transition of the clock. The 'ALS874 and 'AS874 have $\overline{CLR}$ inputs and noninverting Q outputs; the 'ALS876 and 'AS876 have $\overline{PRE}$ inputs and inverting $\overline{Q}$ outputs. In each case, taking this input low causes the four Q or $\overline{Q}$ outputs to go low independently of the clock.

The SN54ALS874, SN54AS874, SN54ALS876 and SN54AS876 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS874, SN74AS874, SN74ALS876, and SN74AS876 are characterized for operation from 0°C to 70°C.

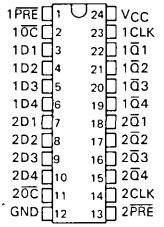
SN54ALS874, SN54AS874 . . . JT PACKAGE
SN74ALS874, SN74AS874 . . . NT PACKAGE
(TOP VIEW)



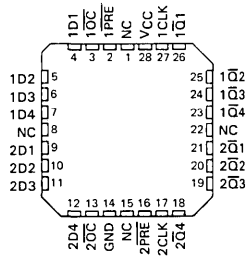
SN54ALS874, SN54AS874 . . . FH PACKAGE
SN74ALS874, SN74AS874 . . . FN PACKAGE
(TOP VIEW)



SN54ALS876, SN54AS876 . . . JT PACKAGE
SN74ALS876, SN74AS876 . . . NT PACKAGE
(TOP VIEW)



SN54ALS876, SN54AS876 . . . FH PACKAGE
SN74ALS876, SN74AS876 . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

FUNCTION TABLES

'ALS874, 'AS874 (EACH FLIP-FLOP)

INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	CLK	D	Q
L	L	X	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q_0
H	X	X	X	Z

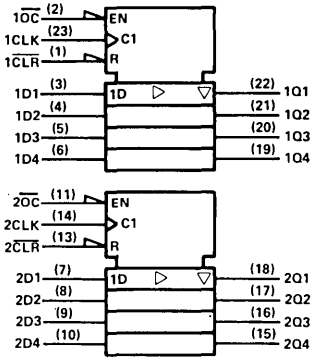
'ALS876, 'AS876 (EACH FLIP-FLOP)

INPUTS				OUTPUT
$\overline{OC}$	$\overline{PRE}$	CLK	D	$\overline{Q}$
L	L	X	X	L
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	$\overline{Q}_0$
H	X	X	X	Z

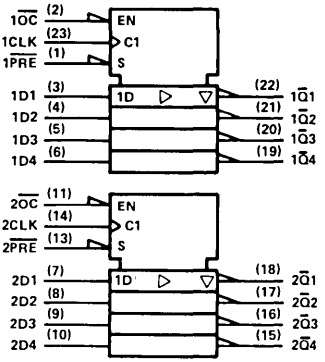
2

logic symbols

'ALS874, 'AS874

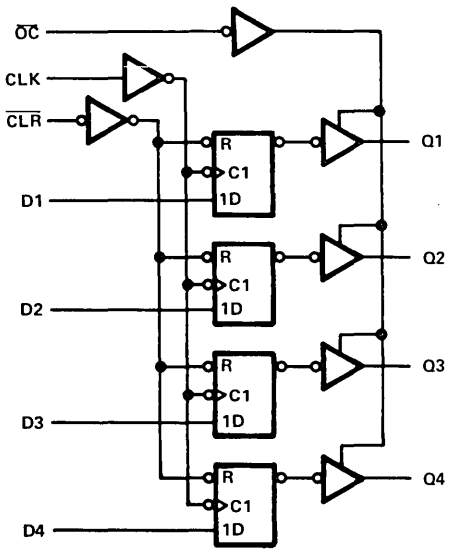


'ALS876, 'AS876

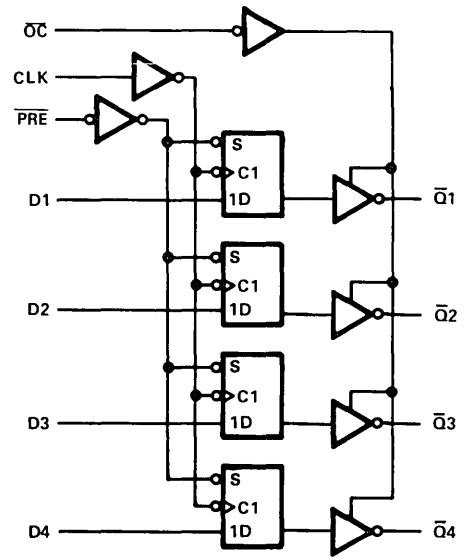


logic diagrams (positive logic)

'ALS874, 'AS874 (EACH QUAD FLIP-FLOP)



'ALS876, 'AS876 (EACH QUAD FLIP-FLOP)



Pin numbers shown are for JT and NT packages.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS874, SN54ALS876 . . . . . −55°C to 125°C
SN74ALS874, SN74ALS876 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS874 SN54ALS876			SN74ALS874 SN74ALS876			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level output voltage				0.8			0.8	V
I_{OH}	High-level output current				−1				mA
								−2.6	
I_{OL}	Low-level output current				12				mA
								24	
f_{clock}	Clock frequency		0		30	0		35	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	10			10			ns
		CLK high	16.5			14			
		CLK low	16.5			14			
t_{su}	Setup time before CLK↑	Data	10			10			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	10			10			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS874 SN54ALS876			SN74ALS874 SN74ALS876			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		14	21		14	21	mA
		Outputs low		18	29		18	29	
		Outputs disabled		20	31		20	31	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS874 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS874		SN74ALS874		
			MIN	MAX	MIN	MAX	
f_{max}			30		35		MHz
t_{PLH}	CLK	Any Q	4	15	4	14	ns
t_{PHL}			4	15	4	14	
t_{PHL}	$\overline{CLR}$	Any Q	6	22	6	19	ns
t_{PZH}	$\overline{OC}$	Any Q	4	21	4	18	ns
t_{PZL}			4	21	4	18	
t_{PHZ}	$\overline{OC}$	Any Q	2	10	2	8	ns
t_{PLZ}			3	15	3	13	

'ALS876 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS876		SN74ALS876		
			MIN	MAX	MIN	MAX	
f_{max}			30		35		MHz
t_{PLH}	CLK	Any $\overline{Q}$	4	15	4	14	ns
t_{PHL}			4	15	4	14	
t_{PHL}	$\overline{PRE}$	Any $\overline{Q}$	6	22	6	19	ns
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	4	21	4	18	ns
t_{PZL}			4	21	4	18	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$	2	10	2	8	ns
t_{PLZ}			3	15	3	13	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS874, SN54AS876 . . . . . −55°C to 125°C
SN74AS874, SN74AS876 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS874 SN54AS876			SN74AS874 SN74AS876			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−12	mA
								−15†	
I_{OL}	Low-level output current				32			32	mA
								48†	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK†	Data							ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive							
t_h	Hold time, data after CLK†								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

†The extended limit applies only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS874 SN54AS876			SN74AS874 SN74AS876			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2		2.4	3.2		V
	V_{CC} = 4.75 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5		0.25	0.5	V
	V_{CC} = 4.75 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V							mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V							μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V							mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high							mA
		Outputs low							
		Outputs disabled		100			100		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
Additional information on these products can be obtained from the factory as it becomes available.

'AS874 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			'AS874			SN54AS874			SN74AS874			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}							160			160		MHz
t_{PLH}	CLK	Any Q					5.5			5.5		ns
t_{PHL}							6			6		
t_{PHL}	$\overline{CLR}$	Any Q					7			7		ns
t_{PZH}	$\overline{OC}$	Any Q					3.5			3.5		ns
t_{PZL}							5			5		
t_{PHZ}	$\overline{OC}$	Any Q					3.5			3.5		ns
t_{PLZ}							5.5			5.5		

'AS876 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			'AS876			SN54AS876			SN74AS876			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}							160			160		MHz
t_{PLH}	CLK	Any $\overline{Q}$					5.5			5.5		ns
t_{PHL}							6			6		
t_{PHL}	$\overline{PRE}$	Any $\overline{Q}$					7			7		ns
t_{PZH}	OC	Any $\overline{Q}$					3.5			3.5		ns
t_{PZL}							5			5		
t_{PHZ}	OC	Any $\overline{Q}$					3.5			3.5		ns
t_{PLZ}							5.5			5.5		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
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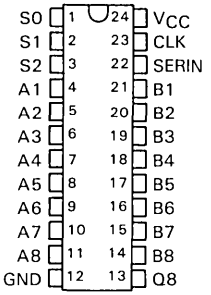
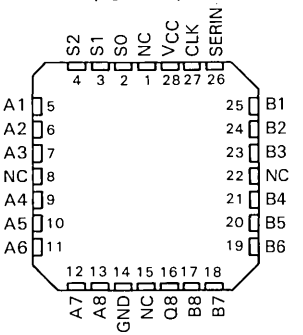
- Included among the Package Options Are Compact, 24-Pin, 300-mil-Wide Dips and Both 28-Pin Plastic and Ceramic Chip Carriers
- Buffered 3-State Outputs Drive Bus Lines Directly
- Cascadable to n-Bits
- Eight Selectable Transceiver/Port Functions:
  - A to B or B to A
  - Register to A or Register to B
  - Shifted to A or Shifted to B
  - Off-Line Shifts (A and B Ports in High-Impedance State)
  - Register Clear
- Particularly Suitable for Use in Signature-Analysis Circuitry
- Serial Register Provides:
  - Parallel Storage of Either A or B Input Data
  - Serial Transmission of Data from Either A or B Port
- Dependable Texas Instruments Quality and Reliability

SN54AS877 . . . . JT PACKAGE
SN74AS877 . . . . NT PACKAGE
(TOP VIEW)



SN54AS877 . . . . FH PACKAGE
SN74AS877 . . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AS877 features two 8-bit I/O ports (A1-A8 and B1-B8), an 8-bit parallel-load, serial-in, parallel-out shift register, and control logic. With these features, this device is capable of performing eight selectable transceiver or port functions, depending on the state of the three select lines S0, S1, and S2. These functions include: transferring data from port A to port B or vice versa (i.e., the transceiver function), transferring data from the register to either port, serial shifting data to either port, performing off-line shifts (with A and B ports in high-impedance state), and clearing the register. Synchronous parallel loading of the internal register can be accomplished from either port on the positive transition of the clock while serially shifting data in via the SERIN input. The 'AS877 is ideally suited for applications needing signature-analysis circuitry to enhance system verification and/or fault analysis. All serial data is shifted right. All outputs are buffer-type outputs designed specifically to drive bus lines directly and all are 3-state except for Q8, which is a totem-pole output.

The SN54AS877 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS877 is characterized for operation from 0°C to 70°C.

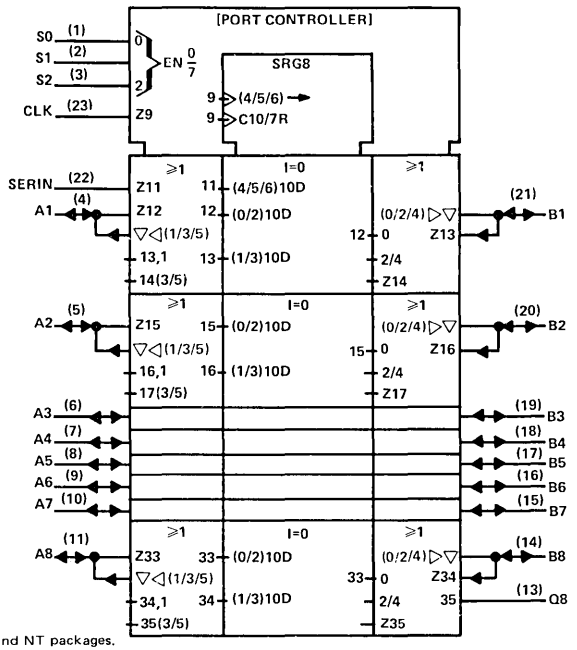
PRODUCT PREVIEW
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

FUNCTION TABLE

MODE S2 S1 S0	CLOCK	SERIN	A1 Q1 B1	A2 Q2 B2	A3 Q3 B3	A4 Q4 B4	A5 Q5 B5	A6 Q6 B6	A7 Q7 B7	A8 Q8 B8	PORT FUNCTION
L L L	H or L	X	Z Q_n A1	Z Q_n A2	Z Q_n A2	Z Q_n A4	Z Q_n A5	Z Q_n A6	Z Q_n A7	Z Q_n A8	A TO B
L L L	↑	X	Z A1 A1	Z A2 A2	Z A3 A3	Z A4 A4	Z A5 A5	Z A6 A6	Z A7 A7	Z A8 A8	
L L H	H or L	X	B1 Q_n Z	B2 Q_n Z	B3 Q_n Z	B4 Q_n Z	B5 Q_n Z	B6 Q_n Z	B7 Q_n Z	B8 Q_n Z	B TO A
L L H	↑	X	B1 B1 Z	B2 B2 Z	B3 B3 Z	B4 B4 Z	B5 B5 Z	B6 B6 Z	B7 B7 Z	B8 B8 Z	
L H L	H or L	X	X Q_n Q1	X Q_n Q2	X Q_n Q3	X Q_n Q4	X Q_n Q5	X Q_n Q6	X Q_n Q7	X Q_n Q8	Q_N TO B_N
L H L	↑	X	Z A1 A1	Z A2 A2	Z A3 A3	Z A4 A4	Z A5 A5	Z A6 A6	Z A7 A7	Z A8 A8	
L H H	H or L	X	Q1 Q_n X	Q2 Q_n X	Q3 Q_n X	Q4 Q_n X	Q5 Q_n X	Q6 Q_n X	Q7 Q_n X	Q8 Q_n X	Q_N TO A_N
L H H	↑	X	B1 B1 Z	B2 B2 Z	B3 B3 Z	B4 B4 Z	B5 B5 Z	B6 B6 Z	B7 B7 Z	B8 B8 Z	
H L L	H or L	X	Z Q_n Q1	Z Q_n Q2	Z Q_n Q3	Z Q_n Q4	Z Q_n Q5	Z Q_n Q6	Z Q_n Q7	Z Q_n Q8	SHIFT
H L L	↑	H	Z H H	Z Q1 Q1	Z Q2 Q2	Z Q3 Q3	Z Q4 Q4	Z Q5 Q5	Z Q6 Q6	Z Q7 Q7	TO
H L L	↑	L	Z L L	Z Q1 Q1	Z Q2 Q2	Z Q3 Q3	Z Q4 Q4	Z Q5 Q5	Z Q6 Q6	Z Q7 Q7	B
H L H	H or L	X	Q1 Q_n Z	Q2 Q_n Z	Q3 Q_n Z	Q4 Q_n Z	Q5 Q_n Z	Q6 Q_n Z	Q7 Q_n Z	Q8 Q_n Z	SHIFT
H L H	↑	H	H H Z	Q1 Q1 Z	Q2 Q2 Z	Q3 Q3 Z	Q4 Q4 Z	Q5 Q5 Z	Q6 Q6 Z	Q7 Q7 Z	TO
H L H	↑	L	L L Z	Q1 Q1 Z	Q2 Q2 Z	Q3 Q3 Z	Q4 Q4 Z	Q5 Q5 Z	Q6 Q6 Z	Q7 Q7 Z	A
H H L	H or L	X	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	
H H L	↑	H	Z H Z	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	SHIFT
H H L	↑	L	Z L Z	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	
H H H	H or L	X	Z Q_n Z	Z Qn Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	CLEAR
H H H	↑	X	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	

n = level of Q_n(n = 1, 2 . . . 8) established on most recent ↑ transition of CLK. Q1 thru Q8 are the shift register outputs; only Q8 is available externally. The double inversions that take place as data travels from port to port are ignored in this table.

logic symbol



Pin numbers shown are for JT and NT packages.

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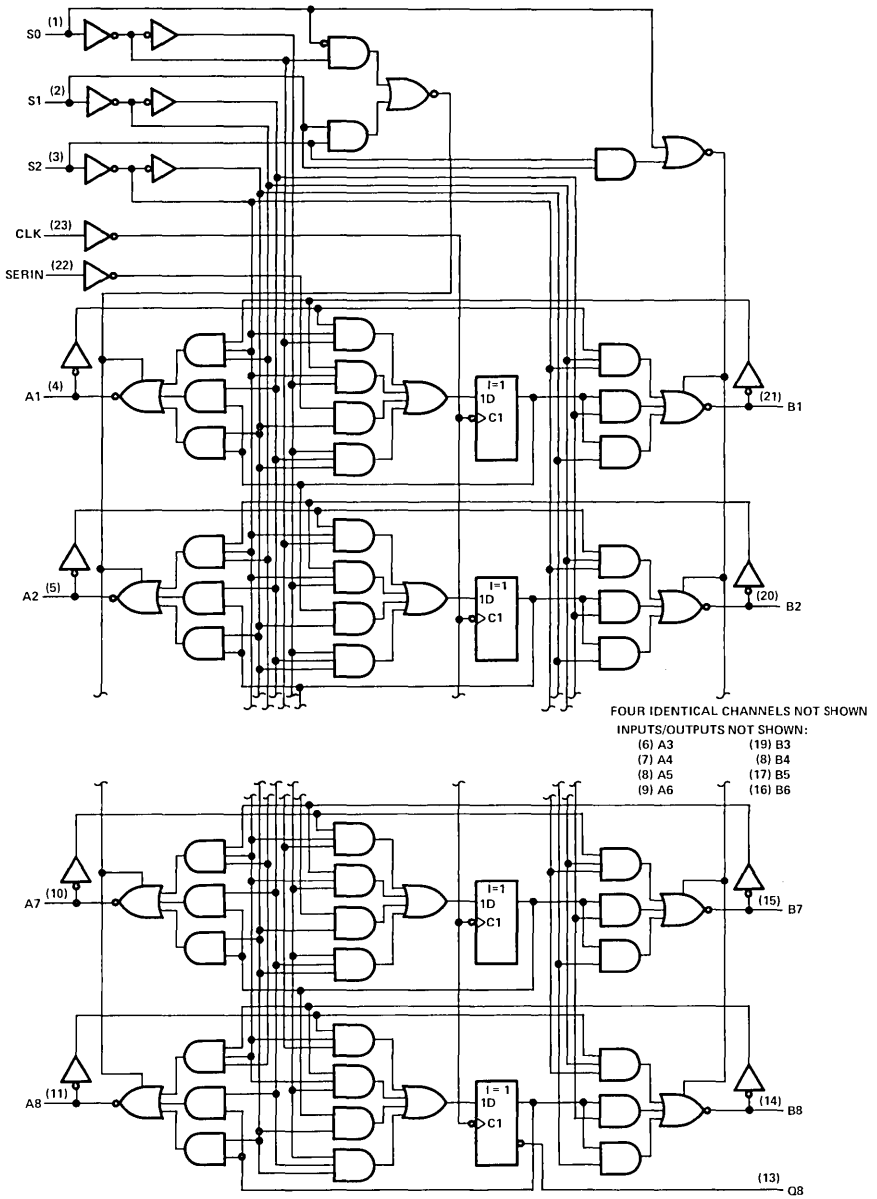
logic diagram (positive logic)



absolute maximum ratings over free-air temperature range

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS877 . . . . . −55°C to 125°C
SN74AS877 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

2

recommended operating conditions

			SN54AS877			SN74AS877			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	A1-A8, B1-B8			−12			−12	mA
								−15†	
		Q8			−2			−2	
I_{OL}	Low-level output current	A1-A8, B1-B8			32			32	mA
		Q8			20			20	
f_{clock}	Clock frequency								MHz
t_w	Duration of clock pulse								ns
t_{su}	Setup time before CLK↑	A1-A8, B1-B8, SERIN							ns
		S0,S1,S2							
t_h	Hold time, data after CLK↑	A1-A8, B1-B8, SERIN	0			0			ns
		S0,S1,S2	0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 and 5.25 V.

Additional information on these products can be obtained from the factory as it becomes available.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54AS877			SN74AS877			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	A1-A8 B1-B8	V_{CC} = 4.5 V, I_{OH} = −12 mA	2.4	3.2		2.4	3.2		V
		V_{CC} = 4.75 V, I_{OH} = −15 mA				2.4	3.3		
	Q8	V_{CC} = 4.5 V, I_{OH} = −2 mA	2.5	3.4		2.5	3.4		
		V_{CC} = 4.75 V, I_{OH} = −2 mA				2.7	3.4		
V_{OL}	All outputs except Q8	V_{CC} = 4.5 V, I_{OL} = 32 mA		0.25	0.5		0.25	0.5	V
	Q8	V_{CC} = 4.5 V, I_{OL} = 20 mA			0.5			0.5	
I_I	S0, S1, S3	V_{CC} = 5.5 V, V_I = 7 V			1			0.6	mA
	CLK and SERIN				0.1			0.1	
	A1-A8, B1-B8	V_{CC} = 5.5 V, V_I = 5.5 V			0.2			0.2	
I_{IH}	S0, S1, S3	V_{CC} = 5.5 V, V_I = 2.7 V			800			400	µA
	CLK and SERIN				20			20	
	A1-A8, B1-B8 ▲				70			70	
I_{IL}	S0, S1, S2	V_{CC} = 5.5 V, V_I = 0.4 V		−2			−2		mA
	CLK and SERIN			−0.3			−0.3		
	A1-A8, B1-B8 ▲			−0.35			−0.35		
I_O §	Except Q8	V_{CC} = 5.5 V, V_O = 2.25 V	−30		−112	−30		−112	mA
	Q8		−20		−112	−20		−112	
I_{CC}		V_{CC} = 5.5 V		136			136		mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

▲ For I/O ports, the parameters I_{IH} and I_{IL} include the output currents I_{OZH} and I_{OZL}, respectively.

§ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

switching characteristics (see note 1)

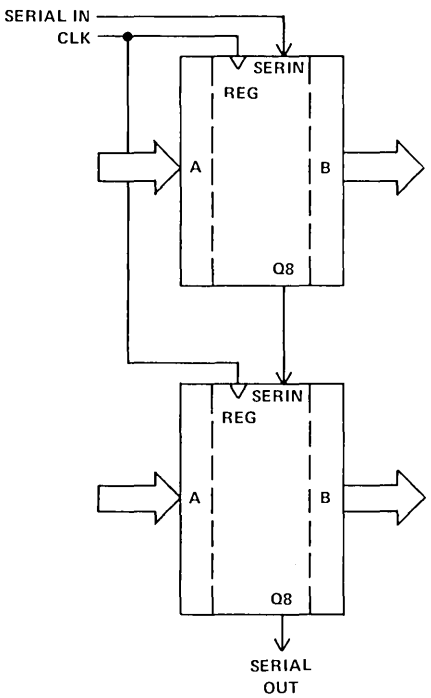
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_1 = 500 Ω, R_2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_1 = 500 Ω, R_2 = 500 Ω, T_A = MIN to MAX						UNIT
			'AS877			SN54AS877			SN74AS877			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}							75			75		MHz
t_{PLH}	Any A port	Any B port					9.5			9.5		ns
t_{PHL}							8			8		
t_{PLH}	Any B port	Any A port					9.5			9.5		ns
t_{PHL}							8			8		
t_{PLH}	S0, S1, S2	Any A or B port					12			12		ns
t_{PHL}							12			12		
t_{PLH}	CLK	Any A or B port					6.5			6.5		ns
t_{PHL}							12.5			12.5		
t_{PLH}	CLK	Q8					9			9		ns
t_{PHL}							9			9		
t_{PHZ}	S0, S1, S2	Any A or B port					6			6		ns
t_{PLZ}							6			6		
t_{PZH}							10			10		ns
t_{PZL}							10			10		

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

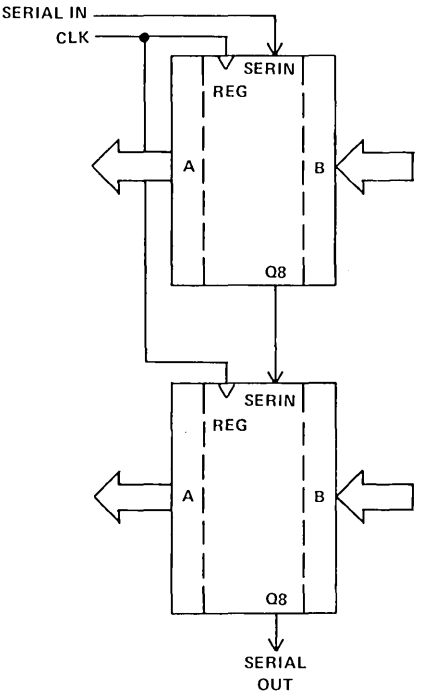
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TYPICAL APPLICATION DATA

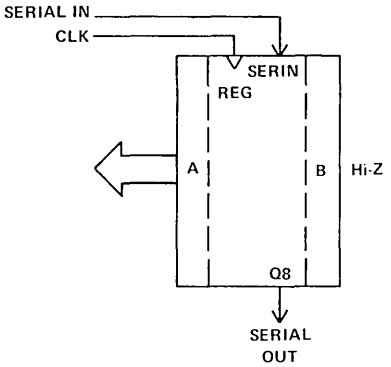
BUS A TO BUS B OR
SERIAL TRANSMISSION



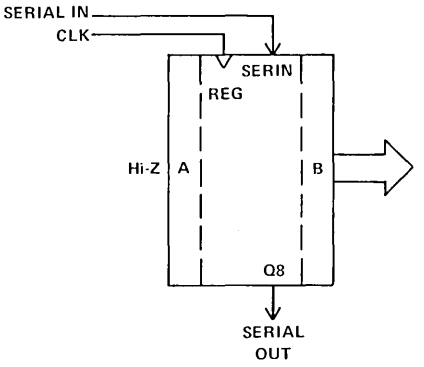
BUS B TO BUS A OR
SERIAL TRANSMISSION



SERIAL IN TO A PORT



SERIAL IN TO B PORT



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TYPES SN54ALS878, SN54ALS879, SN54AS878, SN54AS879
SN74ALS878, SN74ALS879, SN74AS878, SN74AS879
DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

D2661, APRIL 1982

- 3-State Bus-Driving Outputs
- Full Parallel-Access for Loading
- Buffered Control Inputs
- Choice of True or Inverting Logic
  - 'ALS878, 'AS878 True Outputs
  - 'ALS879, 'AS879 Inverting Outputs
- Synchronous Clear
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

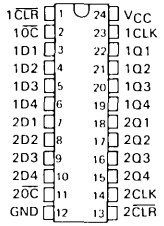
description

These dual 4-bit registers feature three-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

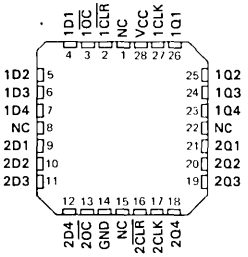
The dual 4-bit edge-triggered flip-flops enter data on the low-to-high transition of the clock (1CLK and 2CLK). All types have individual synchronous clear inputs and output control pins for each group of 4-bit registers.

The SN54ALS878, SN54ALS879, SN54AS878, and SN54AS879 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS878, SN74ALS879, SN74AS878, and SN74AS879 are characterized for operation from 0°C to 70°C.

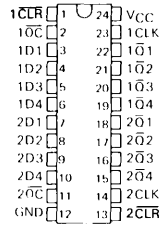
SN54ALS878, SN54AS878 . . . JT PACKAGE
SN74ALS878, SN74AS878 . . . NT PACKAGE
(TOP VIEW)



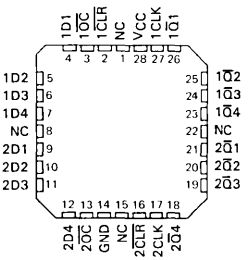
SN54ALS878, SN54AS878 . . . FH PACKAGE
SN74ALS878, SN74AS878 . . . FN PACKAGE
(TOP VIEW)



SN54ALS879, SN54AS879 . . . JT PACKAGE
SN74ALS879, SN74AS879 . . . NT PACKAGE
(TOP VIEW)



SN54ALS879, SN54AS879 . . . FH PACKAGE
SN74ALS879, SN74AS879 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

FUNCTION TABLES

'ALS878, 'AS878
(EACH FLIP-FLOP)

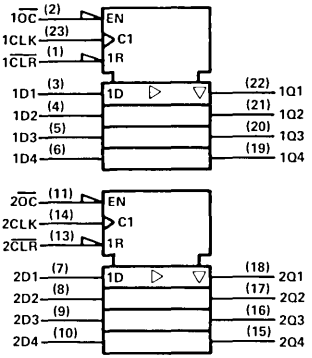
INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	CLK	D	Q
L	L	↑	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q_0
H	X	X	X	Z

'ALS879, 'AS879
(EACH FLIP-FLOP)

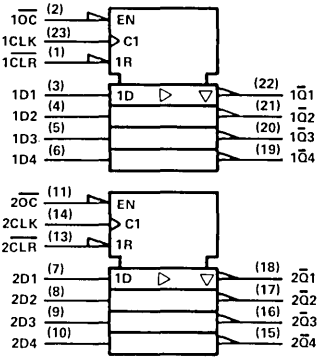
INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	CLK	D	$\overline{Q}$
L	L	↑	X	H
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	Q_0
H	X	X	X	Z

logic symbols

'ALS878, 'AS878

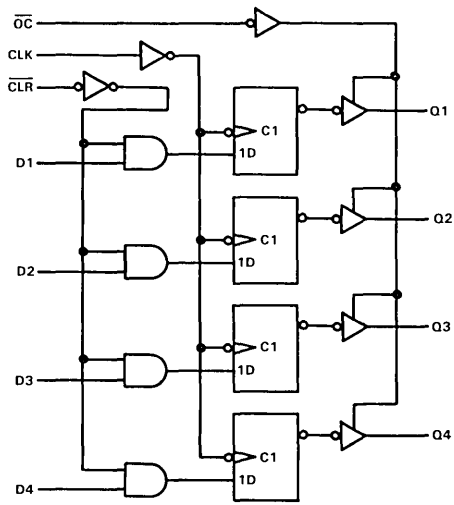


'ALS879, 'AS879

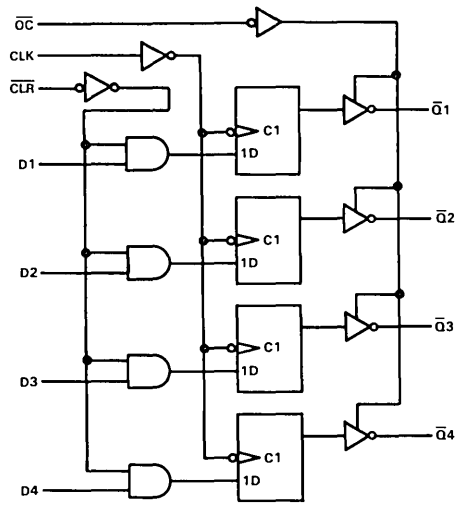


logic diagrams (positive logic)

'ALS878, 'AS878 (EACH QUAD FLIP-FLOP)



'ALS879, 'AS879 (EACH QUAD FLIP-FLOP)



Pin numbers shown are for JT and NT packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS878, SN54ALS879 . . . . . −55°C to 125°C
SN74ALS878, SN74ALS879 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS878 SN54ALS879			SN74ALS878 SN74ALS879			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1				mA
								−2.6	
I_{OL}	Low-level output current				12				mA
								24	
f_{clock}	Clock frequency		0		30	0		35	MHz
t_w	Pulse duration	CLK high	16.5			14			ns
		CLK low	16.5			14			
t_{su}	Setup time before CLK↑	Data	10			10			ns
		$\overline{CLR}$	20			20			
t_h	Hold time after CLK↑	Data	4			0			ns
		$\overline{CLR}$	0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS878 SN54ALS879			SN74ALS878 SN74ALS879			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	V_{CC} = 5.5 V,	Outputs high		14	21		14	21	mA
		Outputs low		18	29		18	29	
		Outputs disabled		20	31		20	31	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

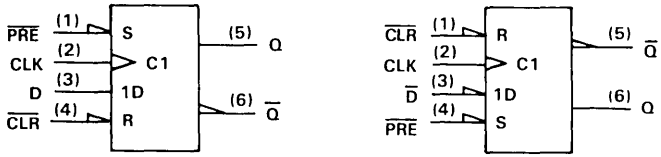
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS878 SN54ALS879		SN74ALS878 SN74ALS879		
			MIN	MAX	MIN	MAX	
f_{max}			30		35		MHz
t_{PLH}	CLK	Q ('ALS878) or $\overline{Q}$ ('ALS879)	4	15	4	14	ns
t_{PHL}			4	15	4	14	
t_{PZH}	$\overline{OC}$	Q ('ALS878) or $\overline{Q}$ ('ALS879)	4	21	4	18	ns
t_{PZL}			4	21	4	18	
t_{PHZ}	$\overline{OC}$	Q ('ALS878) or $\overline{Q}$ ('ALS879)	2	10	2	8	ns
t_{PLZ}			3	15	3	13	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D flip-flop signal conventions

It is TI practice to name the outputs and other inputs of a D-type flip-flop and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.



Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (▷) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input D, but now both are considered active-low.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS878, SN54AS879 . . . . . −55°C to 125°C
SN74AS878, SN74AS879 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS878 SN54AS879			SN74AS878 SN74AS879			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−12	mA
								−15†	
I_{OL}	Low-level output current				32			32	mA
								48†	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	CLK low							ns
		CLK high							
t_{su}	Setup time before CLK↑	Data							ns
		$\overline{CLR}$							
t_h	Hold time after CLK↑	Data							ns
		$\overline{CLR}$							
T_A	Operating free-air temperature		−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS878 SN54AS879			SN74AS878 SN74AS879			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2		2.4	3.2		V
	V_{CC} = 4.75 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5		0.25	0.5	V
	V_{CC} = 4.75 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V							mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V							μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V							mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V, See note 1	Outputs high							mA
		Outputs low							
		Outputs disabled		100			100		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with CLR and all D inputs grounded, and CLK and OC at 4.5 V.

Additional information on these products can be obtained from the factory as it becomes available.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX					UNIT
			'AS878 'AS879	SN54AS878 SN54AS879			SN74AS878 SN74AS879		
			TYP‡	MIN	TYP‡	MAX	MIN	TYP‡ MAX	
f_{max}					160			160	MHz
t_{PLH}	CLK	Q ('AS878) or $\overline{Q}$ ('AS879)			5.5			5.5	ns
t_{PHL}					6			6	
t_{PZH}	$\overline{OC}$	Q ('AS878) or $\overline{Q}$ ('AS879)			3.5			3.5	ns
t_{PZL}					5			5	
t_{PHZ}	$\overline{OC}$	Q ('AS878) or $\overline{Q}$ ('AS879)			3.5			3.5	ns
t_{PLZ}					5.5			5.5	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

- 3-State Buffer-Type Outputs Drive Bus-Lines Directly
- Bus-Structured Pinout
- 'ALS873 Is Alternative Version with Noninverting Outputs
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

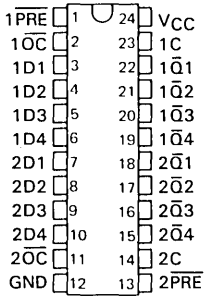
description

These dual 4-bit registers feature three-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

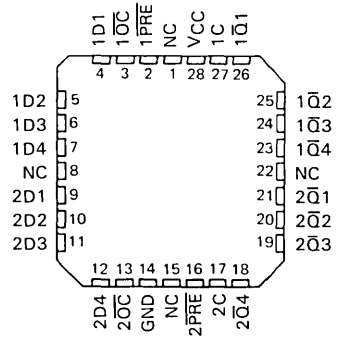
The dual 4-bit latches are transparent D-type. While the latch enable input (1C or 2C) is high, the $\overline{Q}$ outputs will follow the data (D) inputs in inverted form, according to the function table. When the latch enable input is taken low, the outputs will be latched. When $\overline{PRE}$ goes low, the $\overline{Q}$ outputs go low independently of the clock. The outputs are in a high-impedance state when $\overline{OC}$ (output control) is at a high logic level.

The SN54ALS880 and SN54AS880 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS880 and SN74AS880 are characterized for operation from 0 °C to 70 °C.

SN54ALS880, SN54AS880 . . . JT PACKAGE
SN74ALS880, SN74AS880 . . . NT PACKAGE
(TOP VIEW)



SN54ALS880, SN54AS880 . . . FH PACKAGE
SN74ALS880, SN74AS880 . . . FN PACKAGE
(TOP VIEW)

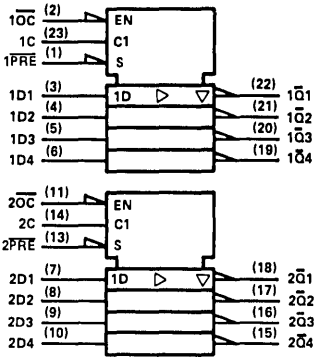


NC — No internal connection

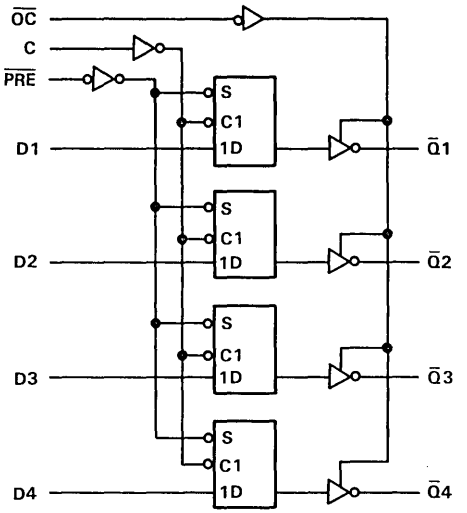
FUNCTION TABLES (EACH LATCH)

INPUTS				OUTPUT
$\overline{OC}$	$\overline{PRE}$	ENABLE C	D	$\overline{Q}$
L	L	X	X	L
L	H	H	H	L
L	H	H	L	H
L	H	L	X	$\overline{Q}_0$
H	X	X	X	Z

logic symbol



logic diagram (each quad latch, positive logic)



Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS880, SN54AS880 . . . . . −55 °C to 125 °C
SN74ALS880, SN74AS880 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

TEXAS INSTRUMENTS
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POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

			SN54ALS880			SN74ALS880			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1				mA
								−2.6	
I_{OL}	Low-level output current				12				mA
								24	
t_w	Pulse duration	$\overline{PRE}$ low	15			15			ns
		Enable C high	15			15			
t_{su}	Setup time, data before enable C↓		15			15			ns
t_h	Hold time, data after enable C↓		10			10			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS880			SN74ALS880			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		14	21		14	21	mA
		Outputs low		19	29		19	29	
		Outputs disabled		20	31		20	31	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

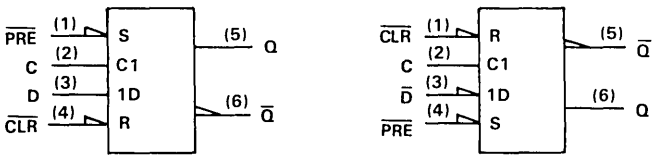
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS880		SN74ALS880		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$	3	23	3	20	ns
t_{PHL}			3	15	3	14	
t_{PLH}	C	$\overline{Q}$	8	31	8	24	ns
t_{PHL}			8	22	8	21	
t_{PHL}	$\overline{PRE}$	$\overline{Q}$	6	24	6	21	ns
t_{PZH}	$\overline{OC}$	$\overline{Q}$	4	21	5	18	ns
t_{PZL}			4	21	5	18	
t_{PHZ}	$\overline{OC}$	$\overline{Q}$	2	10	2	8	ns
t_{PLZ}			3	15	3	13	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D latch signal conventions

It is TI practice to name the outputs and other inputs of a D-type latch and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.



Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (⊵) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input D, but now both are considered active-low.

TEXAS INSTRUMENTS
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recommended operating conditions

			SN54AS880			SN74AS880			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−12	mA
								−15†	
I_{OL}	Low-level output current				32			32	mA
								48†	
t_w	Pulse duration	$\overline{PRE}$ low							ns
		Enable C high							
t_{su}	Setup time, data before enable C↓								ns
t_h	Hold time, data after enable C↓								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS880			SN74AS880			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2		2.4	3.2		V
	V_{CC} = 4.75 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5		0.25	0.5	V
	V_{CC} = 4.75 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.2			−0.2		mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high							mA
		Outputs low							
		Outputs disabled		86			86		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

PRODUCT PREVIEW

This page contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX					UNIT
			'AS880	SN54AS880			SN74AS880		
			TYP‡	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	D	$\overline{Q}$			5.5			5.5		ns
t_{PHL}					4			4		
t_{PLH}	C	$\overline{Q}$			7			7		ns
t_{PHL}					5			5		
t_{PHL}	$\overline{PRE}$	$\overline{Q}$			6			6		ns
t_{PZH}	$\overline{OC}$	$\overline{Q}$			3.5			3.5		ns
t_{PZL}					5			5		
t_{PHZ}	$\overline{OC}$	$\overline{Q}$			3.5			3.5		ns
t_{PLZ}					5.5			5.5		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

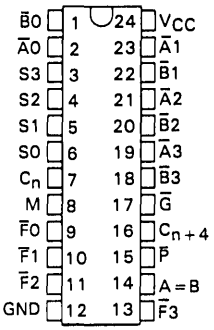
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

D2661, DECEMBER 1982

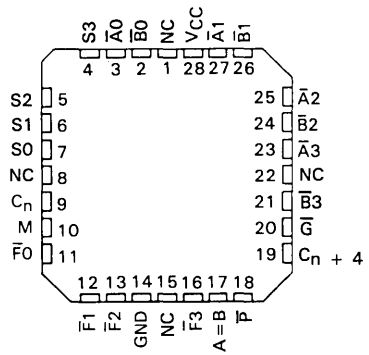
- Package Options Include the 'AS181A in Compact 300-mil or Standard 600-mil DIPs. The 'AS881A Is Offered in 300-mil DIPs. Both Devices Are Available in Both Plastic and Ceramic Chip Carriers
- Full Look-Ahead for High-Speed Operations on Long Words
- Arithmetic Operating Modes:
  - Addition
  - Subtraction
  - Shift Operand A One Position
  - Magnitude Comparison
  - Plus Twelve Other Arithmetic Operations
- Logic Function Modes
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - 'AS881A Provides Status
  - Register Checks
  - Plus Ten Other Logic Operations
- Dependable Texas Instruments Quality and Reliability

SN54AS181A . . . J OR JT PACKAGE
SN54AS881A . . . . JT PACKAGE
SN74AS181A . . . . N OR NT PACKAGE
SN74AS881A . . . . NT PACKAGE
(TOP VIEW)



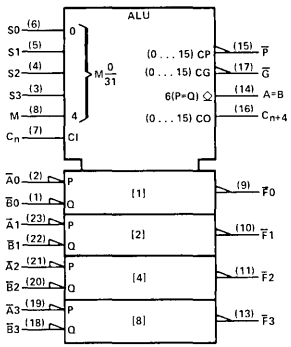
SN54AS181A, SN54AS881A . . . . FH PACKAGE
SN74AS181A, SN74AS881A . . . . FN PACKAGE

'AS181A, 'AS881A
(TOP VIEW)



NC – no internal connection

logic symbol



Pin numbers shown are J, JT, N and NT packages.

For complete information on the SN54AS881A and the SN74AS881A, see page 2-127.

ADVANCE INFORMATION
This document contains information on a new product. Specifications are subject to change without notice.

TEXAS INSTRUMENTS
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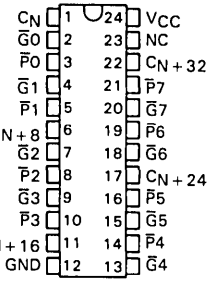
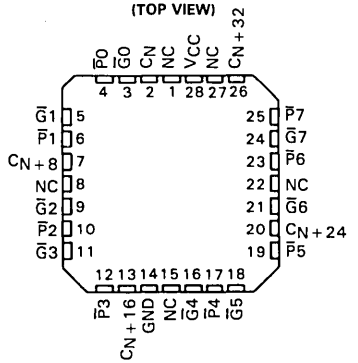
- **Directly Compatible with the New 'AS181A and 'AS881A ALU's**
- **Included among the Package Options Are Compact, 24-Pin, 300-mil-Wide DIPs and Both 28-Pin Plastic and Ceramic Chip Carriers**
- **Capable of Anticipating the Carry Across a Group of Eight 4-Bit Binary Adders**
- **Cascadable to Perform Look-Ahead Across n-Bit Adders**
- **Typical Carry Time, C_n to Any C_{n+i}, Is Less Than 6 ns (C_L = 15 pF)**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS882 . . . JT PACKAGE
SN74AS882 . . . NT PACKAGE
(TOP VIEW)



SN54AS882 . . . FH PACKAGE
SN74AS882 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AS882 is a high-speed look-ahead carry generator capable of anticipating the carry across a group of eight 4-bit adders permitting the designer to implement look-ahead for a 32-bit ALU with a single package or, by cascading 'AS882's, full look-ahead is possible across n-bit adders.

The SN54AS882 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS882 is characterized for operation from 0°C to 70°C.

'AS882 LOGIC EQUATIONS

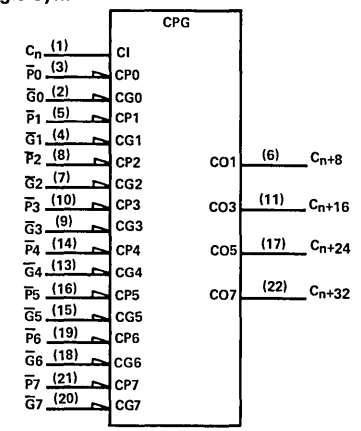
$$C_{n+8} = G1 + P1G0 + P1P0C_n$$

$$C_{n+16} = G3 + P3G2 + P3P2G1 + P3P2P1G0 + P3P2P1P0C_n$$

$$C_{n+24} = G5 + P5G4 + P5P4G3 + P5P4P3G2 + P5P4P3P2G1 + P5P4P3P2P1G0 + P5P4P3P2P1P0C_n$$

$$C_{n+32} = G7 + P7G6 + P7P6G5 + P7P6P5G4 + P7P6P5P4G3 + P7P6P5P4P3G2 + P7P6P5P4P3P2G1 + P7P6P5P4P3P2P1G0 + P7P6P5P4P3P2P1P0C_n$$

logic symbol



Pin numbers shown are for JT and NT packages.

ADVANCE INFORMATION
This document contains information on a new product. Specifications are subject to change without notice.

FUNCTION TABLE
FOR C_{n+32} OUTPUT

INPUTS																OUTPUT
$\overline{G}7$	$\overline{G}6$	$\overline{G}5$	$\overline{G}4$	$\overline{G}3$	$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}7$	$\overline{P}6$	$\overline{P}5$	$\overline{P}4$	$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+32}
L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	L	L	X	X	X	X	X	X	X	H
X	X	X	L	X	X	X	X	L	L	L	X	X	X	X	X	X	H
X	X	X	X	L	X	X	X	L	L	L	L	X	X	X	X	X	H
X	X	X	X	X	L	X	X	L	L	L	L	L	X	X	X	X	H
X	X	X	X	X	X	L	X	L	L	L	L	L	L	X	X	X	H
X	X	X	X	X	X	X	L	L	L	L	L	L	L	L	X	X	H
X	X	X	X	X	X	X	X	L	L	L	L	L	L	L	L	H	H
All other combinations																	L

FUNCTION TABLE
FOR C_{n+24} OUTPUT

INPUTS													OUTPUT
$\overline{G}5$	$\overline{G}4$	$\overline{G}3$	$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}5$	$\overline{P}4$	$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+24}
L	X	X	X	X	X	X	X	X	X	X	X	X	H
X	L	X	X	X	X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	L	L	X	X	X	X	X	H
X	X	X	L	X	X	L	L	L	X	X	X	X	H
X	X	X	X	L	X	L	L	L	L	X	X	X	H
X	X	X	X	X	L	L	L	L	L	L	X	X	H
X	X	X	X	X	X	L	L	L	L	L	L	H	H
All other combinations													L

FUNCTION TABLE
FOR C_{n+16} OUTPUT

INPUTS								OUTPUT
$\overline{G}3$	$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+16}
L	X	X	X	X	X	X	X	X	H
X	L	X	X	L	X	X	X	X	H
X	X	L	X	L	L	X	X	X	H
X	X	X	L	L	L	L	X	X	H
X	X	X	X	L	L	L	L	H	H
All other combinations									L

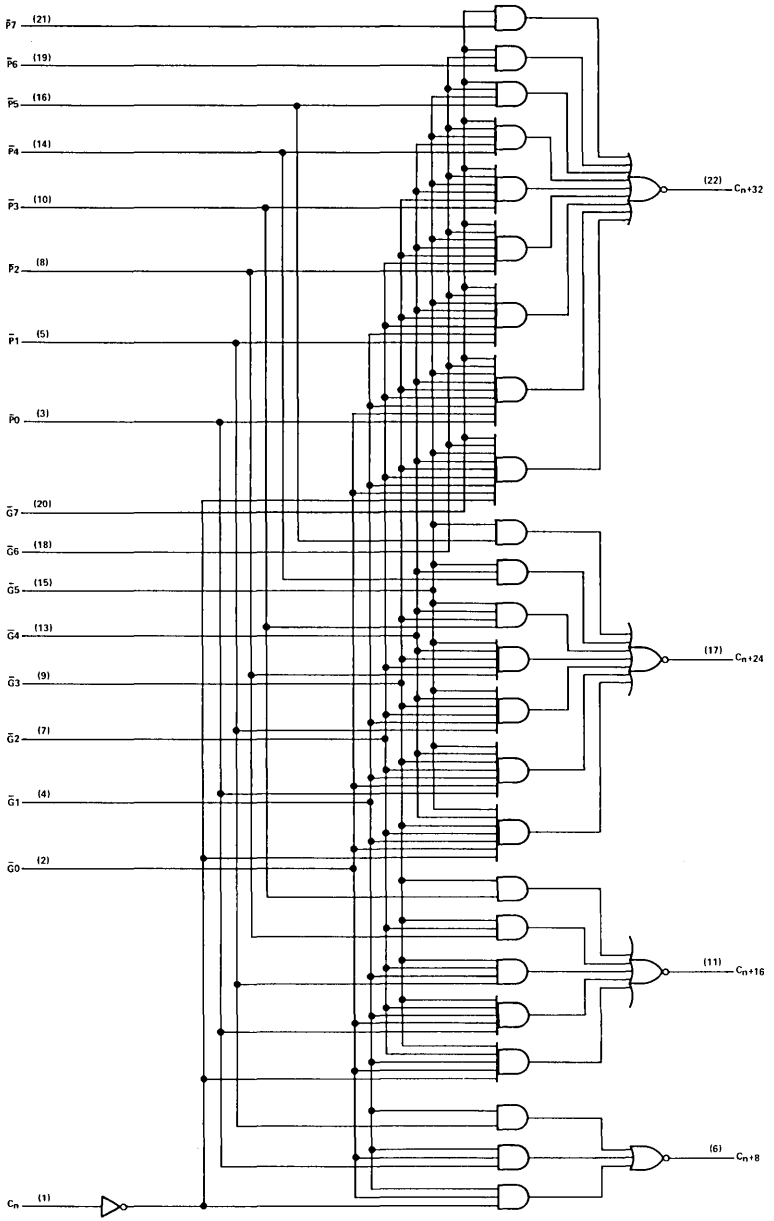
FUNCTION TABLE
FOR C_{n+8} OUTPUT

INPUTS					OUTPUT
$\overline{G}1$	$\overline{G}0$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+8}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

Any inputs not shown in a given table are irrelevant with respect to that output.

2

logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS882 . . . . . −55 °C to 125 °C
SN74AS882 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS882			SN74AS882			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54AS882			SN74AS882			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V, I_{OH} = −2 mA	2.5	3.2		2.5	3.2		V
		V_{CC} = 4.75 V, I_{OH} = −2 mA	2.7	3.2		2.7	3.2		
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I	C_n	V_{CC} = 5.5 V, V_I = 7 V			0.5			0.5	mA
	$\overline{G0},\overline{G6}$				4			4	
	$\overline{G1},\overline{G2},\overline{G4}$				6			6	
	$\overline{G3}$				7.5			7.5	
	$\overline{G5}$				7			7	
	$\overline{G7}$				4.5			4.5	
	$\overline{P0},\overline{P1}$				2			2	
	$\overline{P2},\overline{P3}$				1.5			1.5	
	$\overline{P4},\overline{P5}$				1			1	
	$\overline{P6},\overline{P7}$				0.5			0.5	
I_{IH}	C_n	V_{CC} = 5.5 V, V_I = 2.7 V			0.2			0.2	mA
	$\overline{G0},\overline{G6}$				1.6			1.6	
	$\overline{G1},\overline{G2},\overline{G4}$				2.4			2.4	
	$\overline{G3}$				3			3	
	$\overline{G5}$				2.8			2.8	
	$\overline{G7}$				1.8			1.8	
	$\overline{P0},\overline{P1}$				0.8			0.8	
	$\overline{P2},\overline{P3}$				0.6			0.6	
	$\overline{P4},\overline{P5}$				0.4			0.4	
	$\overline{P6},\overline{P7}$				0.2			0.2	
I_{IL}	C_n	V_{CC} = 5.5 V, V_I = 0.4 V			3			3	mA
	$\overline{G0}$				26			26	
	$\overline{G1}$				37			37	
	$\overline{G2}$				40			40	
	$\overline{G3}$				47			47	
	$\overline{G4}$				41			41	
	$\overline{G5}$				44			44	
	$\overline{G6},\overline{G7}$				28			28	
	$\overline{P0}$				13			13	
	$\overline{P1}$				11			11	
	$\overline{P2}$				9			9	
	$\overline{P3}$				8			8	
	$\overline{P4}$				5			5	
	$\overline{P5}$				4			4	
	$\overline{P6},\overline{P7}$				2			2	
I_O§		V_{CC} = 5.5 V, V_O = 2.25 V		−150			−150		mA
I_{CC}		V_{CC} = 5.5 V		72	105		72	105	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			'AS882			SN54AS882			SN74AS882			
			MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	C_n	Any output		6		4		15	4		14	ns
t_{pd}	$\overline{P}$ or $\overline{G}$	C_{n+8}		4		2		9	2		8	
t_{pd}	$\overline{P}$ or $\overline{G}$	C_{n+16}		6		2		9	2		8	
t_{pd}	$\overline{P}$ or $\overline{G}$	C_{n+24}		7		2		11	2		10	
t_{pd}	$\overline{P}$ or $\overline{G}$	C_{n+32}		10.5		2		13	2		12	

t_{pd} = t_{PHL} or t_{PLH}

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TYPICAL APPLICATION DATA

The application given in figure 1 illustrates how the 'AS882 can implement look-ahead carry for a 32-bit ALU (in this case, the popular 'AS881) with a single package. Typical carry times shown are derived using the standard Advanced Schottky load circuit with C_L = 15 pF.

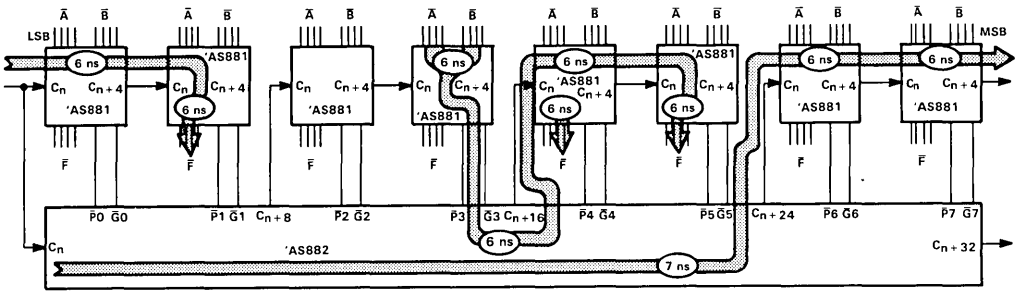
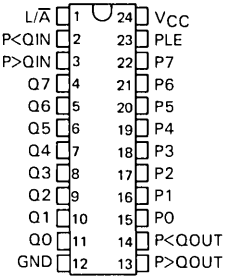


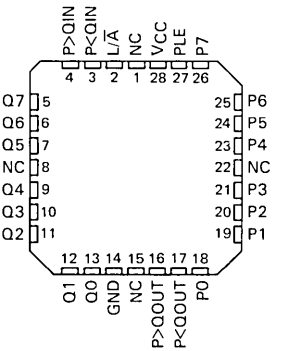
FIGURE 1 – 'AS881A ALU WITH 'AS882 LOOK-AHEAD CARRY GENERATORS

- Included among the Package Options Are Compact, 24-Pin, 300-mil DIPs and Both 28-Pin Ceramic and Plastic Chip Carriers
- Latchable P Input Ports with Power-Up Clear
- Choice of Logical or Arithmetic (2's Complement) Comparison
- Data and PLE Inputs Utilize P-N-P Input Transistors to Reduce DC Loading Effects
- Approximately 35% Improvement in AC Performance Over Schottky TTL while Performing More Functions
- Cascadable to n-Bits while Maintaining High Performance
- 10% Less Power than STTL for an 8-Bit Comparison
- Dependable Texas Instruments Quality and Reliability

SN54AS885 . . . . JT PACKAGE
SN74AS885 . . . . NT PACKAGE
(TOP VIEW)



SN54AS885 . . . . FH PACKAGE
SN74AS885 . . . . FN PACKAGE
(TOP VIEW)



description

These advanced Schottky devices are capable of performing high-speed arithmetic or logic comparisons on two 8-bit binary or two's complement words. Two fully decoded decisions about words P and Q are externally available at two outputs. These devices are fully expandable to any number of bits without external gates. The P > Q and P < Q outputs of a stage handling less-significant bits may be connected to the P > Q and P < Q inputs of the next stage handling more-significant bits to obtain comparisons of words of longer lengths. The cascading paths are implemented with only a two-gate-level delay to reduce overall comparison times for long words. Two alternative methods of cascading are shown in the typical application data.

The latch is transparent when P Latch Enable (PLE) is high; the P input port is latched when PLE is low. This provides the designer with temporary storage for the P data word. The enable circuitry is implemented with minimal delay times to enhance performance when cascaded for longer words. The PLE and P and Q data inputs utilize p-n-p input transistors to reduce the low-level current input requirement to typically −0.25 mA, which minimizes dc loading effects.

The SN54AS885 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS885 is characterized for operation from 0°C to 70°C.

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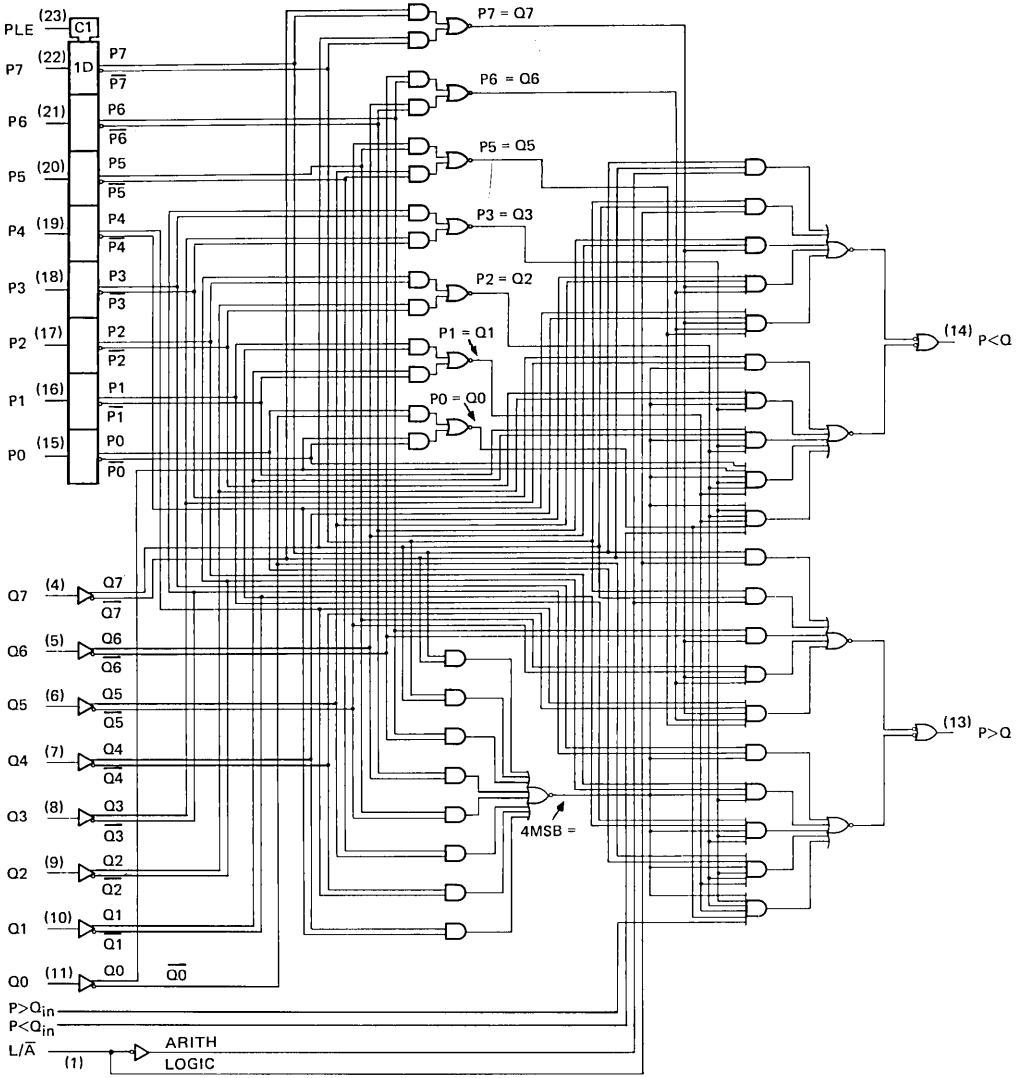
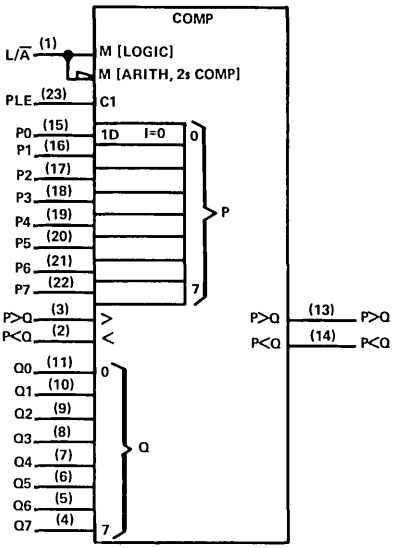
logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

logic symbol



Pin numbers shown are for JT and NT packages.

FUNCTION TABLE

COMPARISON	L/Ā	DATA INPUTS P0-P7, Q0-Q7	INPUT P>Q	INPUT P<Q	OUTPUTS P>Q	OUTPUTS P<Q
LOGICAL	H	P>Q	X	X	H	L
LOGICAL	H	P<Q	X	X	L	H
LOGICAL*	H	P=Q	H OR L	H OR L	H OR L	H OR L
ARITHMETIC	L	P AG Q	X	X	H	L
ARITHMETIC	L	Q AG P	X	X	L	H
ARITHMETIC*	L	P=Q	H OR L	H OR L	H OR L	H OR L

*In these cases the P>Q output will follow the P>Q input, and the P<Q output will follow the P<Q input.
AG — arithmetically greater than

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS885 . . . . . −55°C to 125°C
SN74AS885 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

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recommended operating conditions

PARAMETER		SN54AS885			SN74AS885			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
t_{su}	Setup time to PLE ↓	2			2			ns
t_h	Hold time after PLE ↓	4			4			
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54AS885			SN74AS885			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V, I_{OH} = −2 mA	2.5	3.4		2.5	3.4		V
		V_{CC} = 4.75 V, I_{OH} = −2 mA				2.7	3.4		
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I		V_{CC} = 5.5 V V_I = 7 V			100			100	µA
I_{IH}	$L/\overline{A}$	V_{CC} = 5.5 V V_I = 2.7 V			40			40	µA
	Others				20			20	
I_{IL}	$L/\overline{A}$	V_{CC} = 5.5 V, V_I = 0.4 V			−4			−4	mA
	$P>Q_{in}$ $P<Q_{in}$				−2			−2	
	P, Q, PLE				−1			−1	
I_O‡		V_{CC} = 5.5 V, V_O = 2.25 V	−20		−112	−20		−112	mA
I_{CC}		V_{CC} = 5.5 V, See Note 1		130	210		130	210	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.
NOTE 1: I_{CC} is measured with all inputs high except $L/\overline{A}$, which is low.

switching characteristics (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			'AS885			SN54AS885			SN74AS885			
			MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	$L/\overline{A}$	P<Q, P>Q		6.5			8.5	14		8.5	13	ns
t_{PHL}				7.5			7.5	14		7.5	13	
t_{PLH}	P<Q, P>Q			4.5			5	10		5	8	ns
t_{PHL}				4.5			5.5	10		5.5	8	
t_{PLH}	Any P or Q Data Input			11.5			13.5	21		13.5	17.5	ns
t_{PHL}				9.5			10	17		10	15	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: For load circuit and voltage waveforms, see page 1-12.

2

TYPICAL APPLICATION DATA

The 'AS885 can be cascaded to compare words longer than 8-bits. Figure 1 shows the comparison of two 32-bit words; however, the design is expandable to n-bits. Figure 1 shows the optimum cascading arrangement for comparing words of 32 bits or greater. Typical delay times shown are at V_{CC} = 5 V, T_A = 25°C, and use the standard Advanced Schottky load of R_L = 500 Ω, C_L = 50 pF.

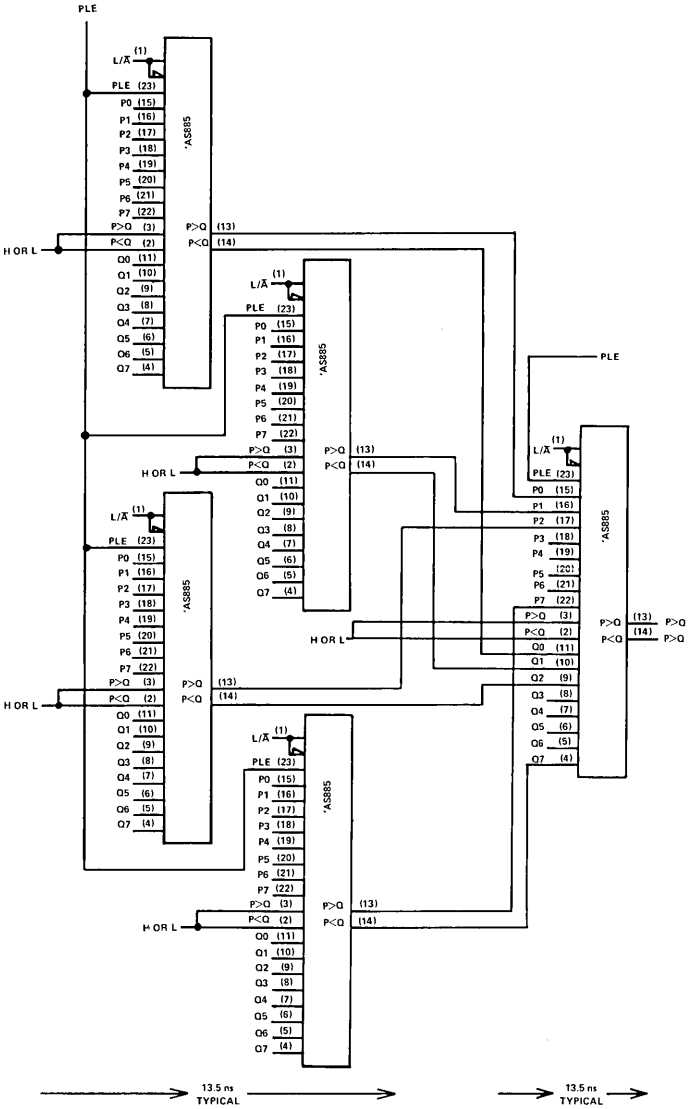

FIGURE 1 – 32-BIT TO 72 (N)-BIT MAGNITUDE COMPARATOR

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TYPICAL APPLICATION DATA

The method shown in Figure 2 is the fastest cascading arrangement for comparing 16-bit or 24-bit words. Typical delay times shown are at V_{CC} = 5 V, T_A = 25°C, and use the standard Advanced Schottky load of R_L = 500 Ω, C_L = 50 pF.

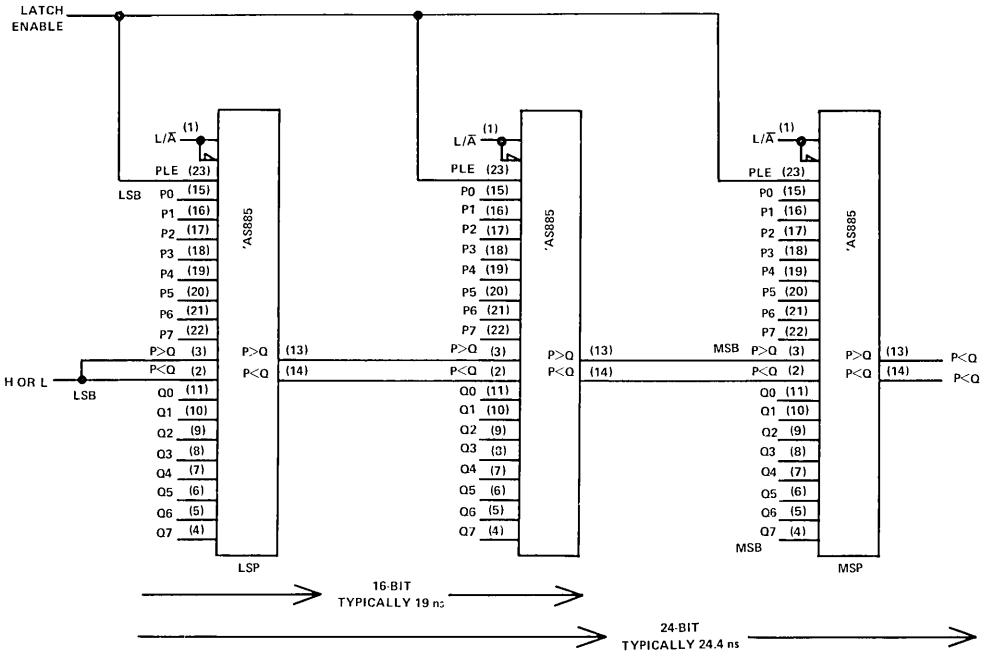


FIGURE 2

- **Buffer Version of 'ALS00A**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

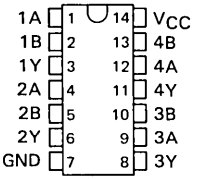
2

description

These devices contain four independent 2-input NAND buffers. They perform the boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54ALS1000 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1000 is characterized for operation from 0°C to 70°C.

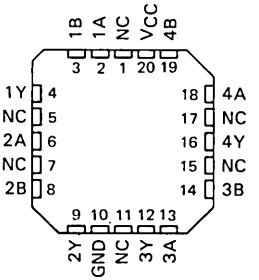
SN54ALS1000 . . . J PACKAGE
SN74ALS1000 . . . N PACKAGE
(TOP VIEW)



FUNCTION TABLE (each gate)

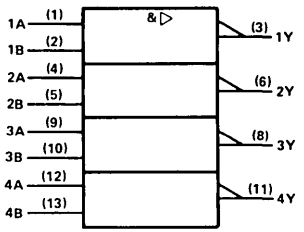
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

SN54ALS1000 . . . FH PACKAGE
SN74ALS1000 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

logic symbol



Pin numbers shown are for J and N packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1000 . . . . . −55 °C to 125 °C
SN74ALS1000 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS1000			SN74ALS1000			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1000			SN74ALS1000			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.86	1.6		0.86	1.6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		4	6.4		4	6.4	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

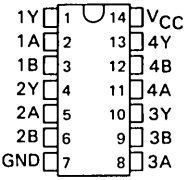
switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1000		SN74ALS1000		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2	10	2	8	ns
t_{PHL}			3	10	3	8	

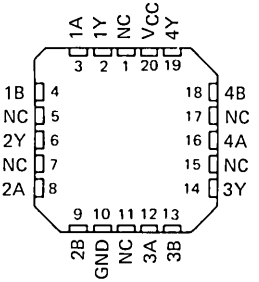
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- Quad Versions of 'ALS805
- Buffer Version of 'ALS02
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS1002, . . . J PACKAGE
SN74ALS1002, . . . N PACKAGE
(TOP VIEW)



SN54ALS1002 . . . FH PACKAGE
SN74ALS1002 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

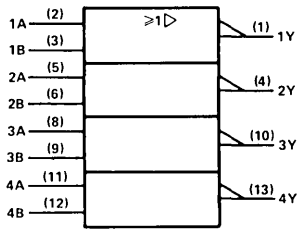
These devices contain four independent 2-input NOR buffers. They perform the boolean functions $Y = \overline{A+B}$ or $Y = \overline{A}\cdot\overline{B}$ in positive logic.

The SN54ALS1002 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1002 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol



Pin numbers shown are for J and N packages.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1002 . . . . . −55 °C to 125 °C
SN74ALS1002 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS1002			SN74ALS1002			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1002			SN74ALS1002			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		1.7	2.8		1.7	2.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		4.8	8		4.8	8	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1002		SN74ALS1002		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2	10	2	8	ns
t_{PHL}			3	10	3	8	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- **Buffer Version of 'ALS03A**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

2

description

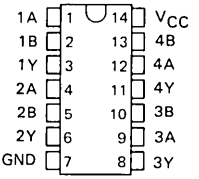
These devices contain four independent 2-input NAND buffers. They perform the boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS1003 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1003 is characterized for operation from 0°C to 70°C.

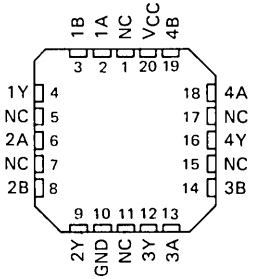
FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

SN54ALS1003 . . . J PACKAGE
SN74ALS1003 . . . N PACKAGE
(TOP VIEW)

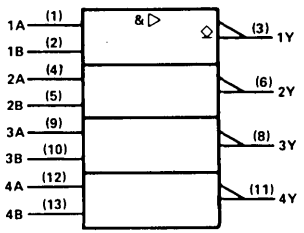


SN54ALS1003 . . . FH PACKAGE
SN74ALS1003 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

logic symbol



Pin numbers shown are for J and N packages.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1003 . . . . . −55 °C to 125 °C
SN74ALS1003 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS1003			SN74ALS1003			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1003			SN74ALS1003			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.86	1.6		0.86	1.6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		4	6.4		4	6.4	mA

‡ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1003		SN74ALS1003		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	10	40	10	33	ns
t_{PHL}			7	21	7	18	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- Buffer Version of 'ALS04
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

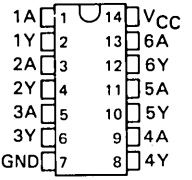
2

description

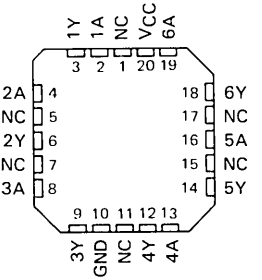
These devices contain six independent inverting buffers. They perform the boolean functions $Y = \overline{A}$.

The SN54ALS1004 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1004 is characterized for operation from 0°C to 70°C.

SN54ALS1004 . . . J PACKAGE
SN74ALS1004 . . . N PACKAGE
(TOP VIEW)



SN54ALS1004 . . . FH PACKAGE
SN74ALS1004 . . . FN PACKAGE
(TOP VIEW)

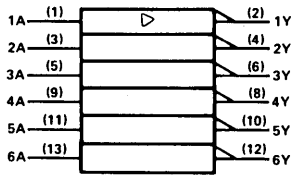


NC – No internal connection

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic symbol



Pin numbers shown are for J and N packages.

ADVANCE INFORMATION

This page contains information on a new product. Specifications are subject to change without notice.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1004 . . . . . −55 °C to 125 °C
SN74ALS1004 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS1004			SN74ALS1004			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1004			SN74ALS1004			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.84			0.84		mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		7.2			7.2		mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1004			SN74ALS1004			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y		3			3		ns
t_{PHL}				3			3		

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- **Buffer Version of 'ALS05**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

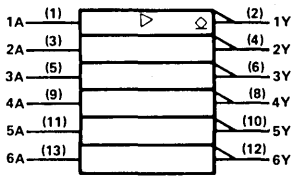
These devices contain six independent inverting buffers. They perform the boolean functions $Y = \overline{A}$. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS1005 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1005 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each inverter)

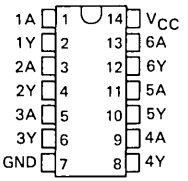
INPUT A	OUTPUT Y
H	L
L	H

logic symbol

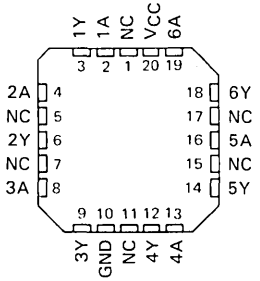


Pin numbers shown are for J and N packages.

SN54ALS1005 . . . J PACKAGE
SN74ALS1005 . . . N PACKAGE
(TOP VIEW)



SN54ALS1005 . . . FH PACKAGE
SN74ALS1005 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

ADVANCE INFORMATION

This document contains information on a new product. Specifications are subject to change without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1005 . . . . . −55 °C to 125 °C
SN74ALS1005 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS1005			SN74ALS1005			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1005			SN74ALS1005			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.9			0.9		mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		7.2			7.2		mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.

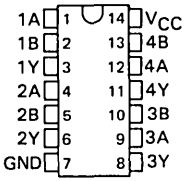
switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1005			SN74ALS1005			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y		20			20		ns
t_{PHL}				4.5			4.5		

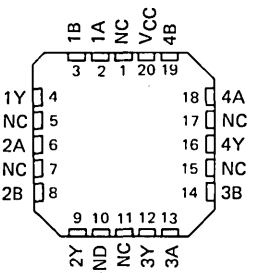
‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
NOTE 1. For load circuit and voltage waveforms, see page 1-12.

- **Quad Version of 'ALS808 and AS808A**
- **Buffer Version of 'ALS08**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS1008, SN54AS1008 . . . J PACKAGE
SN74ALS1008, SN74AS1008 . . . N PACKAGE
(TOP VIEW)



SN54ALS1008, SN54AS1008 . . . FH PACKAGE
SN74ALS1008, SN74AS1008 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

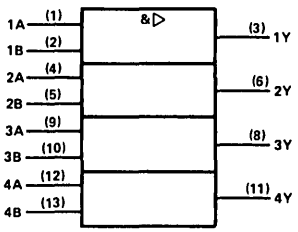
These devices contain four independent 2-input AND buffers. They perform the boolean functions $Y = A \cdot B$ or $Y = \overline{\overline{A}+\overline{B}}$ in positive logic.

The SN54ALS1008 and SN54AS1008 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1008 and SN74AS1008 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1008 . . . . . −55 °C to 125 °C
SN74ALS1008 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS1008			SN74ALS1008			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1008			SN74ALS1008			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4				V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.8	3		1.8	3	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		4.8	8		4.8	8	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1008		SN74ALS1008		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2	11	2	9	ns
t_{PHL}			3	11	3	9	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS1008 . . . . . −55°C to 125°C
SN74AS1008 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS1008			SN74AS1008			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40				mA
							−48	
I_{OL}	Low-level output current			40				mA
							48	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS1008			SN74AS1008			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		V
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5		0.25	0.5	V
	V_{CC} = 4.5 V	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.2			−0.2		mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V		−150			−150		mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		8			8		mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		22			22		mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

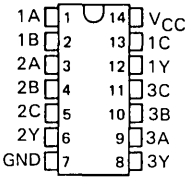
switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX					UNIT
			'AS1008	SN54AS1008			SN74AS1008		
			TYP‡	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y	2.5		3.3			3.3		ns
t_{PHL}	A or B	Y	2.4		3.0			3.0		ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- Buffer Version of 'ALS10
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS1010 . . . J PACKAGE
SN74ALS1010 . . . N PACKAGE
(TOP VIEW)



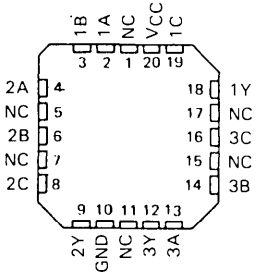
2

description

These devices contain three independent 3-input NAND buffers. They perform the boolean functions $Y = \overline{A \cdot B \cdot C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

The SN54ALS1010 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1010 is characterized for operation from 0°C to 70°C.

SN54ALS1010 . . . FH PACKAGE
SN74ALS1010 . . . FN PACKAGE
(TOP VIEW)

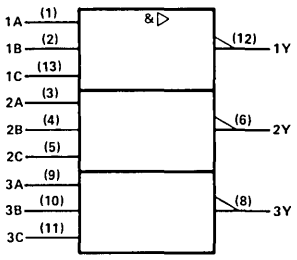


NC—No internal connection

FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1010 . . . . . −55 °C to 125 °C
SN74ALS1010 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS1010			SN74ALS1010			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1010			SN74ALS1010			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.65	1.2		0.65	1.2	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		3.6	6		3.6	6	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1010		SN74ALS1010		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	2	10	2	8	ns
t_{PHL}			3	10	3	8	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

- Buffer Version of 'ALS11
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

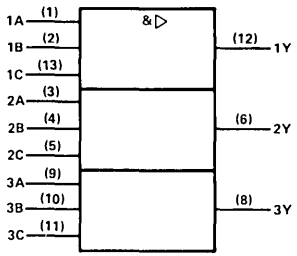
These devices contain three independent 3-input AND buffers. They perform the boolean functions $Y = A \cdot B \cdot C$ or $Y = \overline{\overline{A} + \overline{B} + \overline{C}}$ in positive logic.

The SN54ALS1011 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1011 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

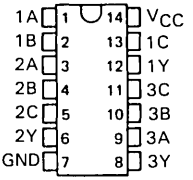
INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

logic symbol

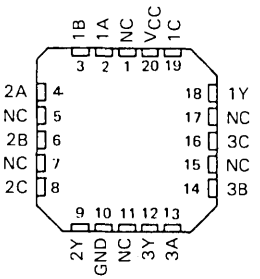


Pin numbers shown are for J and N packages.

SN54ALS1011 . . . J PACKAGE
SN74ALS1011 . . . N PACKAGE
(TOP VIEW)



SN54ALS1011 . . . FH PACKAGE
SN74ALS1011 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1011 . . . . . −55 °C to 125 °C
SN74ALS1011 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS1011			SN74ALS1011			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1011			SN74ALS1011			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.4	2.3		1.4	2.3	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		3.6	6		3.6	6	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1011		SN74ALS1011		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	2	12	2	10	ns
t_{PHL}			3	11	3	9	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

- Buffer Version of 'ALS20A
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

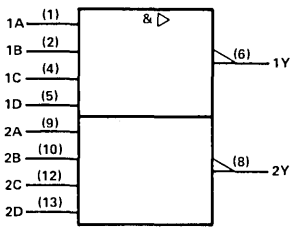
These devices contain two independent 4-input NAND buffers. They perform the boolean functions $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

The SN54ALS1020 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1020 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

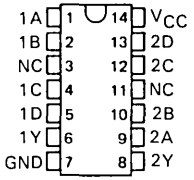
INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

logic symbol

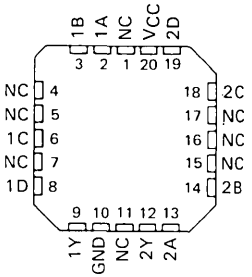


Pin numbers shown are for J and N packages.

SN54ALS1020 . . . J PACKAGE
SN74ALS1020 . . . N PACKAGE
(TOP VIEW)



SN54ALS1020 . . . FH PACKAGE
SN74ALS1020 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1020 . . . . . −55 °C to 125 °C
SN74ALS1020 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

2

recommended operating conditions

		SN54ALS1020			SN74ALS1020			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1020			SN74ALS1020			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.5	0.8		0.5	0.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		2	3.2		2	3.2	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1020		SN74ALS1020		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	2	10	2	8	ns
t_{PHL}			3	10	3	8	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

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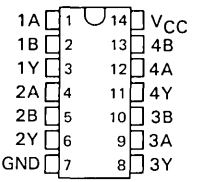
- Quad Versions of 'ALS832 and 'AS832
- Buffer Version of 'ALS32
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS1032, SN54AS1032 . . . J PACKAGE
SN74ALS1032, SN74AS1032 . . . N PACKAGE
(TOP VIEW)

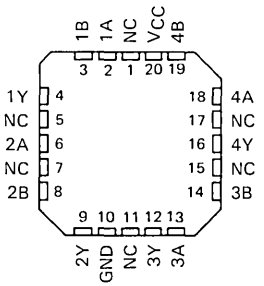


description

These devices contain four independent 2-input OR buffers. They perform the boolean functions $Y = A+B$ or $Y = \overline{\overline{A}\cdot\overline{B}}$ in positive logic.

The SN54ALS1032 and SN54AS1032 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1032 and SN74AS1032 are characterized for operation from 0°C to 70°C.

SN54ALS1032, SN54AS1032 . . . FH PACKAGE
SN74ALS1032, SN74AS1032 . . . FN PACKAGE
(TOP VIEW)

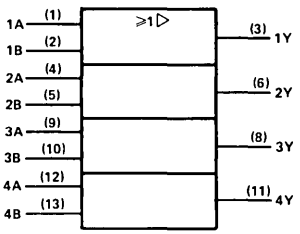


NC – No internal connection

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1032 . . . . . −55 °C to 125 °C
SN74ALS1032 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS1032			SN74ALS1032			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1032			SN74ALS1032			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		2.5	5		2.5	5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		5.5	10		5.5	10	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1032		SN74ALS1032		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2	12	2	10	ns
t_{PHL}			3	15	3	13	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS1032 . . . . . −55 °C to 125 °C
SN74AS1032 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS1032			SN74AS1032			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS1032			SN74AS1032			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		V
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.9 V		−0.2			−0.2		mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V		−150			−150		mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		15			15		mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		25			25		mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25 °C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX					UNIT
			'AS1032	SN54AS1032			SN74AS1032		
			TYP‡	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y	2.5		3.3			3.3		ns
t_{PHL}	A or B	Y	2.4		3.0			3.0		ns

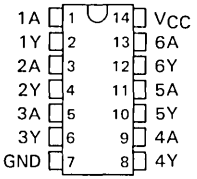
‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

PRODUCT PREVIEW

This page contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

- 'AS1034 Offers High Capacitive-Drive Capability
- Noninverting Buffers
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS1034, SN54AS1034 . . . J PACKAGE
SN74ALS1034, SN74AS1034 . . . N PACKAGE
(TOP VIEW)



description

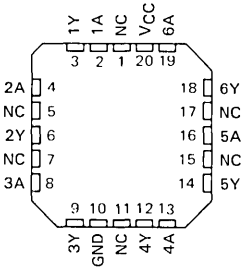
These devices contain six independent noninverting buffers. They perform the boolean functions Y = A.

The SN54ALS1034 and SN54AS1034 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS1034 and SN74AS1034 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each buffer)

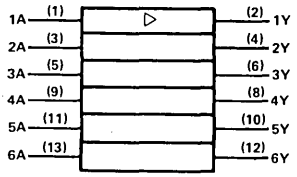
INPUT A	OUTPUT Y
H	H
L	L

SN54ALS1034, SN54AS1034 . . . FH PACKAGE
SN74ALS1034, SN74AS1034 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol



Pin numbers shown are for J and N packages.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1034 . . . . . −55°C to 125°C
SN74ALS1034 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1034			SN74ALS1034			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1				mA
							−2.6	
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1034			SN74ALS1034			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4				V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		3			3		mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		7.8			7.8		mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1034			SN74ALS1034			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y		4			4		ns
t_{PHL}				4.5			4.5		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

ADVANCE INFORMATION

This page contains information on a new product. Specifications are subject to change without notice.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS1034 . . . . . −55 °C to 125 °C
SN74AS1034 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS1034			SN74AS1034			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40				mA
							−48	
I_{OL}	Low-level output current			40				mA
							48	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS1034			SN74AS1034			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		V
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2			2			
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.4			−0.4		mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V		−150			−150		mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		3			3		mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		18			18		mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

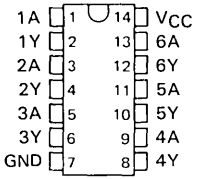
switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25 °C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX					UNIT
			'AS1034	SN54AS1034			SN74AS1034		
			TYP‡	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	1.7		2.6			2.6		ns
t_{PHL}			1.6		2.7			2.7		

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- Noninverting Buffers with Open-Collector Outputs
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS1035 . . . J PACKAGE
SN74ALS1035 . . . N PACKAGE
(TOP VIEW)



description

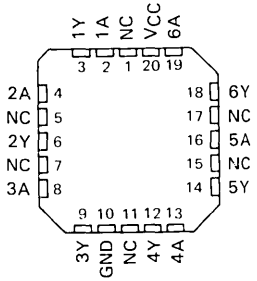
These devices contain six independent noninverting buffers. They perform the boolean functions Y = A. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS1035 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1035 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each buffer)

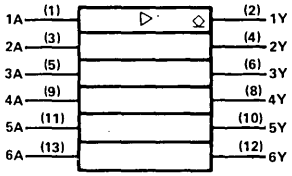
INPUT A	OUTPUT Y
H	H
L	L

SN54ALS1035 . . . FH PACKAGE
SN74ALS1035 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

logic symbol



Pin numbers shown are for J and N packages.

ADVANCE INFORMATION

This document contains information on a new product. Specifications are subject to change without notice.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1035 . . . . . −55 °C to 125 °C
SN74ALS1035 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

2

recommended operating conditions

		SN54ALS1035			SN74ALS1035			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12				mA
							24	
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1035			SN74ALS1035			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		3.2			3.2		mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		8.6			8.6		mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1035			SN74ALS1035			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y		20			20		ns
t_{PHL}	A	Y		5			5		ns

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

D2661, DECEMBER 1982

- **Low-Power Version of 'ALS240 and 'ALS241**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **P-N-P Inputs Reduce DC Loading**
- **Dependable Texas Instruments Quality and Reliability**

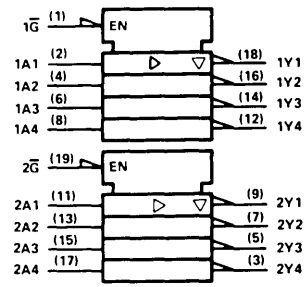
description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out and improved fan-in.

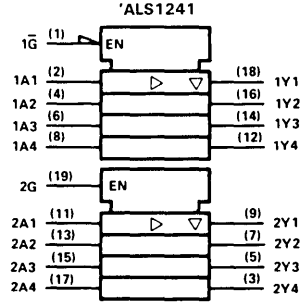
The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 24 milliamperes. There are no -1 versions of the SN54ALS' parts.

logic symbols

'ALS1240

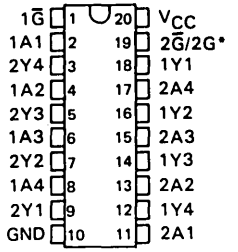


'ALS1241

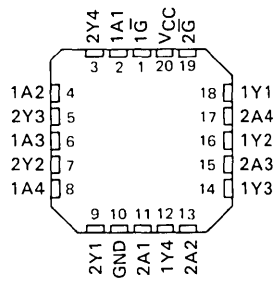


Pin numbers shown are for J and N packages.

SN54ALS1240, SN54ALS1241 . . . J PACKAGE
SN74ALS1240, SN74ALS1241 . . . N PACKAGE
(TOP VIEW)



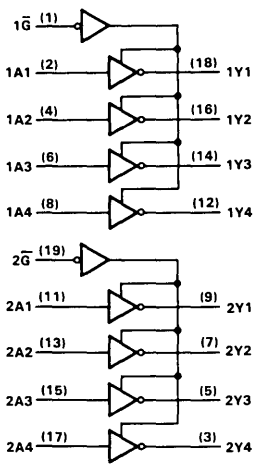
SN54ALS1240, SN54ALS1241 . . . FH PACKAGE
SN74ALS1240, SN74ALS1241 . . . FN PACKAGE
(TOP VIEW)



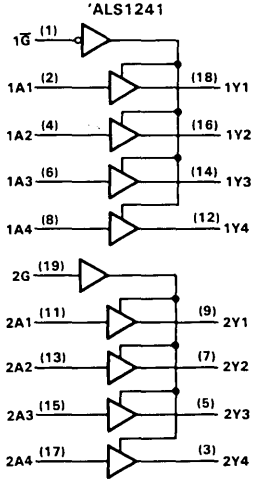
*$2\overline{G}$ for 'ALS1240 or 2G for 'ALS1241

functional block diagrams (positive logic)

'ALS1240



'ALS1241



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS1240, SN54ALS1241 . . . . . −55°C to 125°C
SN74ALS1240, SN74ALS1241 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

2

recommended operating conditions

		SN54ALS1240 SN54ALS1241			SN74ALS1240 SN74ALS1241			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12				mA
							−15	
I_{OL}	Low-level output current			8				mA
							16	
							24†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 24-mA limit applies for the SN74ALS1240-1 and SN74ALS1241-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1240 SN54ALS1241			SN74ALS1240 SN74ALS1241			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		V
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V, (I_{OL} = 24 mA for -1 versions)	I_{OL} = 16 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		6.5			6.5		mA
		Outputs low		10			10		
		Outputs disabled		12			12		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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'ALS1240 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1240			SN74ALS1240			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y		9			9		ns
t_{PHL}				9			9		
t_{PZH}	$\overline{G}$	Y		17			17		ns
t_{PZL}				19			19		
t_{PHZ}	$\overline{G}$	Y		7			7		ns
t_{PLZ}				6			6		

'ALS1241 switching characteristics (see note 1)

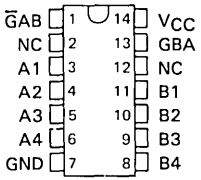
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1241			SN74ALS1241			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y		9			9		ns
t_{PHL}				9			9		
t_{PZH}	$\overline{G}$ or G	Y		17			17		ns
t_{PZL}				19			19		
t_{PHZ}	$\overline{G}$ or G	Y		7			7		ns
t_{PLZ}				6			6		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

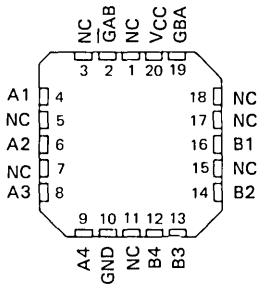
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- 2-Way Asynchronous Communication between Data Buses
- P-N-P Inputs Reduce DC Loading
- Low-Power Version of 'ALS242, and 'ALS243
- Three-State Outputs
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS1242, SN54ALS1243 . . . J PACKAGE
SN74ALS1242, SN74ALS1243 . . . N PACKAGE
(TOP VIEW)



SN54ALS1242, SN54ALS1243 . . . FH PACKAGE
SN74ALS1242, SN74ALS1243 . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These quadruple bus transceivers are designed for two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs (GBA and $\overline{G}AB$).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 'ALS1242 and 'ALS1243 the capability to store data by simultaneous enabling of $\overline{G}AB$ and GBA. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (8 in all) will remain at their last states. The 4-bit codes appearing on the two sets of buses will be complementary for the 'ALS1242 or identical for the 'ALS1243.

The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 24 milliamperes. There are no -1 versions of the SN54ALS' parts.

The SN54ALS1242 and SN54ALS1243 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS1242 and SN74ALS1243 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE

$\overline{G}AB$	GBA	'ALS1242	'ALS1243
L	L	$\overline{A}$ to B	A to B
H	H	$\overline{B}$ to A	B to A
H	L	Isolation	Isolation
L	H	Latch A and B ($A = \overline{B}$)	Latch A and B ($A = B$)

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

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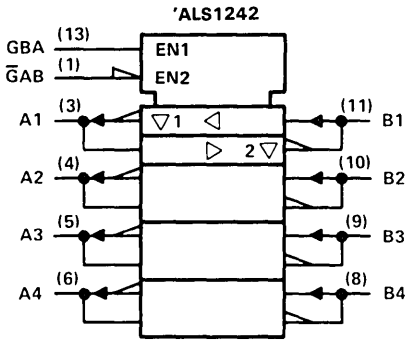
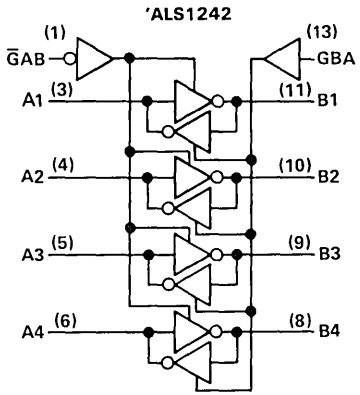
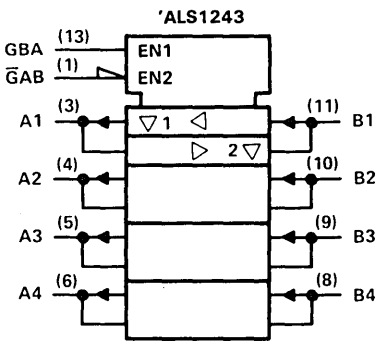
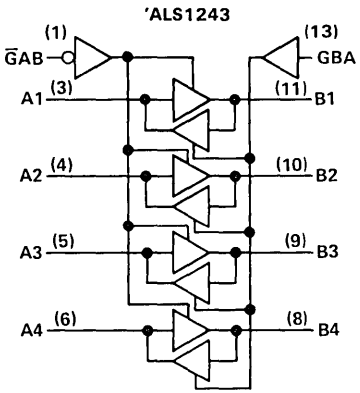
logic symbols



logic diagrams (positive logic)







Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54AS1242, SN54ALS1243 . . . . . −55°C to 125°C
SN74AS1242, SN74ALS1243 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1242 SN54ALS1243			SN74ALS1242 SN74ALS1243			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12				mA
							−15	
I_{OL}	Low-level output current			8				mA
							16	
							24†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 24-mA limit applies for the SN74ALS1242-1 and SN74ALS1243-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS1242 SN54ALS1243			SN74ALS1242 SN74ALS1243			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V (I_{OL} = 24 mA for -1 versions)	I_{OL} = 16 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports▲					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports▲					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS1242	V_{CC} = 5.5 V	Outputs high							mA
			Outputs low							
			Outputs disabled							
	'ALS1243		Outputs high							
			Outputs low							
			Outputs disabled							

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
▲For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
Additional information on these products can be obtained from the factory as it becomes available.

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'ALS1242 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1242			SN74ALS1242			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	B or A							ns
t_{PHL}									
t_{PZH}	$\overline{G}$AB	B							ns
t_{PZL}									
t_{PHZ}	$\overline{G}$AB	B							ns
t_{PLZ}									
t_{PZL}	GBA	A							ns
t_{PZL}									
t_{PHZ}	GBA	A							ns
t_{PLZ}									

'ALS1243 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1243			SN74ALS1243			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	B or A							ns
t_{PHL}									
t_{PZH}	$\overline{G}$AB	B							ns
t_{PZL}									
t_{PHZ}	$\overline{G}$AB	B							ns
t_{PLZ}									
t_{PZH}	GBA	A							ns
t_{PZL}									
t_{PHZ}	GBA	A							ns
t_{PLZ}									

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

PRODUCT PREVIEW

This page contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

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- Low-Power Version of 'ALS244
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce DC Loading
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

2

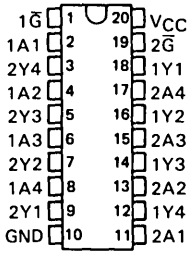
description

This octal buffer and line driver is designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'ALS1240 and 'ALS1241 this device provides the choice of selected combinations of inverting and noninverting outputs symmetrical $\overline{G}$ (active-low input control) inputs, and complementary G and $\overline{G}$ inputs.

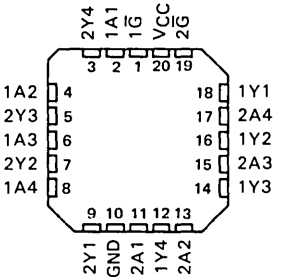
The -1 version of the SN74ALS1244 is identical to the standard version except that the recommended maximum I_{OL} is increased to 24 milliamperes. There is no -1 version of the SN54ALS1244.

The SN54ALS1244 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1244 is characterized for operation from 0°C to 70°C.

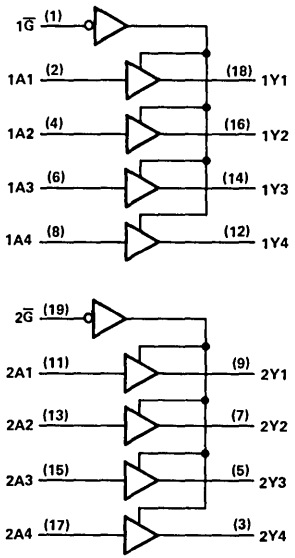
SN54ALS1244 . . . J PACKAGE
SN74ALS1244 . . . N PACKAGE
(TOP VIEW)



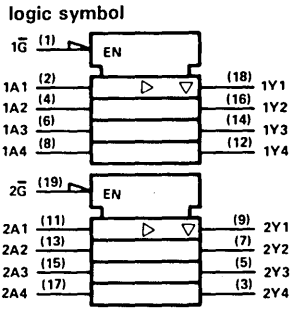
SN54ALS1244 . . . FH PACKAGE
SN74ALS1244 . . . FN PACKAGE
(TOP VIEW)



functional block diagram (positive logic)



logic symbol



Pin numbers shown are for J and N packages

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS1244 . . . . . −55°C to 125°C
SN74ALS1244 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1244			SN74ALS1244			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12				mA
							−15	
I_{OL}	Low-level output current			8				mA
							16	
							24†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 24-mA limit applies for the SN74ALS1244-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1244			SN74ALS1244			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		V
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V, (I_{OL} = 24 mA for −1 version)	I_{OL} = 16 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		6	12		6	11	mA
		Outputs low		10	18		10	17	
		Outputs disabled		11	22		11	20	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1244		SN74ALS1244		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	4	16	4	14	ns
t_{PHL}			4	16	4	14	
t_{PZH}	$\overline{G}$	Y	8	28	9	25	ns
t_{PZL}			10	35	11	32	
t_{PHZ}	$\overline{G}$	Y	2	12	2	10	ns
t_{PLZ}			3	21	3	16	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

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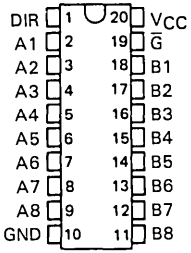
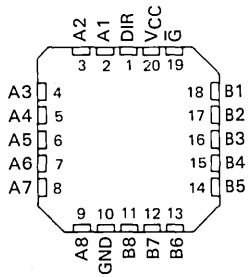
- 'Bidirectional Bus Transceivers in High-Density 20-Pin Packages
- Lower-Power Version of 'ALS245
- 'ALS1245 is Identical to 'ALS1645
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS1245 . . . J PACKAGE
SN74ALS1245 . . . N PACKAGE
(TOP VIEW)



SN54ALS1245 . . . FH PACKAGE
SN74ALS1245 . . . FN PACKAGE



description

This octal bus transceiver is designed for asynchronous two-way communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (G) can be used to disable the device so the buses are effectively isolated.

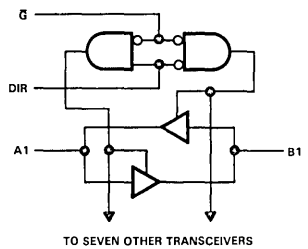
The -1 version of the SN74ALS1245 is identical to the standard versions except that the recommended maximum I_{OL} is increased to 24 milliamperes. There is no -1 version of the SN54ALS1245.

The SN54ALS1245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1245 is characterized for operation from 0°C to 70°C.

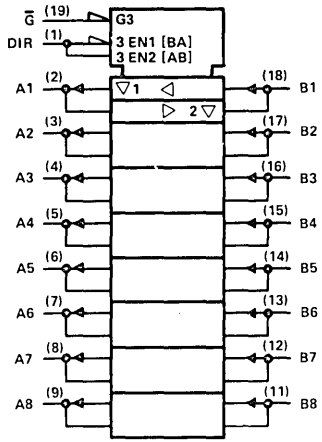
FUNCTION TABLE

CONTROL INPUTS		OPERATION
G	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



logic symbol



Pin numbers shown are for J and N packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS1245 . . . . . −55 °C to 125 °C
SN74ALS1245 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

2

recommended operating conditions

		SN54ALS1245			SN74ALS1245			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12				mA
							−15	
I_{OL}	Low-level output current			8				mA
							16	
							24†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limit applies only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 24-mA limit applies for the SN74ALS1245-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS1245			SN74ALS1245			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18mA				−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V, I_{OH} = −3 mA		2.4	3.2		2.4	3.2		V
		V_{CC} = 4.5 V, I_{OH} = −12 mA		2						
		V_{CC} = 4.5 V, I_{OH} = −15 mA					2			
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 8 mA			0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, I_{OL} = 16 mA (I_{OL} = 24 mA for −1 version)						0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V, V_I = 7 V				0.1			0.1	mA
	A or B ports▲	V_{CC} = 5.5 V, V_I = 5.5 V				0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V, V_I = 2.7 V				20			20	μA
	A or B ports▲					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V, V_I = 0.4 V				−0.1			−0.1	mA
	A or B ports▲					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V, V_O = 2.25 V		−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Output high		20	33		20	32	mA
			Output low		23	39		23	37	
			Output disabled		25	41		25	39	

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
▲For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

switching characteristics (see note 2)

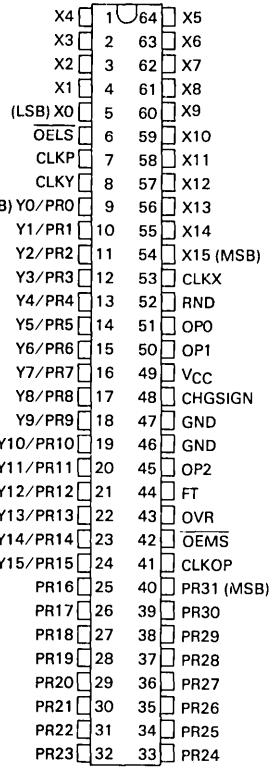
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1245		SN74ALS1245		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	4	15	4	13	ns
t_{PHL}			4	15	4	13	
t_{PZH}	$\overline{G}$	A or B	10	27	10	25	ns
t_{PZL}			13	32	13	29	
t_{PHZ}	$\overline{G}$	A or B	4	20	4	18	ns
t_{PLZ}			5	23	5	21	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2661, JUNE 1982

- Multiplies Any Combination of Unsigned, Signed, Integer, or Fractional Inputs
- Registered Inputs and Outputs
- Comparable to the TRW MPY-16HJ
- Choice of Single-Signed, Double-Signed, Unsigned, or Signed Fractionally Adjusted Outputs
- Overflow Detected if a Combination of Input Data and/or Output Formats Result in a Number that Cannot be Represented
- Rounding is Provided for Both Integer and Fractional Results
- Flexible Input-Output Format Aids in Expansion to Multiple Precision Results
- 55 ns Typical Unclocked Multiply Time
- Power Dissipation Approximately 1.5 W
- 3-State Outputs
- Ideal for Signal Processing, Including Digital Filters, FFTs, and Automatic Line Integration
- Expansion of the Arithmetic Capabilities of Mini and Micro Systems
- Output may be Complemented
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54AL1616, SN74ALS1616 . . . JD PACKAGE
(TOP VIEW)



SN54ALS1616...FH PACKAGE
SN74ALS1616...FN PACKAGE

For chip carrier information contact the factory

description

The SN54ALS1616 and SN74ALS1616 allow the user to generate fast 16 X 16 multiplications at low power. An input-output formatting scheme is available that allows combinations of unsigned, single-signed, or double-signed outputs. Binary adjustment is provided internally to allow 16N- X 16M-bit multiples to be easily implemented with an external adder. An overflow pin is provided and will become active (high) if an input data and output format combination produces a result that exceeds 32 bits. Rounding may be implemented for either fractional or integer outputs.

The 'ALS1616 is designed to match all unsigned and two's-complement number systems including:

Unsigned Integer
Unsigned Fractional
Signed Integer
Signed Fractional

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Multiplication may be performed in all eight combinations of these four number systems. Representations of numbers in these systems differ in the weight assigned to each data bit and placement of the binary point.

Registers are provided for the X inputs and Y outputs. If FT is high, the output registers are bypassed. If FT is low, the contents of the edge-triggered registers are fed to the output. The output registers will look like transparent registers if FT is tied to an inverted version of CLKP.

The 'ALS1616 consists of two input registers (X and Y), a control register, a multiplier array, a format shifter, an output register, and three-state output buffers. The two 16-bit binary numbers are received and stored in the X and Y input registers on the rising edge of clock input signals CLKX and CLKY. Operation codes (OP0 through OP2), change sign (CHGSIGN), and rounding (RND) are inputs to the control register and determine the input and output format, complementing function, and the rounding function. The control signals are stored in the control register on the rising edge of CLKOP. Table 1 provides the input and output format and rounding function for each operation code. The 32-bit product (PR0 through PR31) and an overflow indicator from the multiplier array are stored in the output register. The output register is divided into two parts; the most-significant half and the least-significant half. On the rising edge of clock input CLKP, product bits PR16 through PR31 are stored in the most-significant half and product bits PR0 through PR15 are stored in the least-significant half. In addition, the overflow indicator is stored in the output register. When high, the CHGSIGN input causes the output of the multiplier array, MPR31 through MPR01, to be the two's complement of the product specified by the operation code.

The most-significant product bits are output through the three-state outputs PR15 through PR0. These pins and the three-state overflow output (OVR) will all be in the high-impedance state when output enable $\overline{\text{OEMS}}$ is high. The least-significant product bits are multiplexed with the sixteen Y input bits through the three-state I/O ports Y15/P15 through Y0/PR0. These pins will be in the high-impedance (input) state when output enable $\overline{\text{OELS}}$ is high. Table 2 provides the pin names and signal functions for all 'ALS1616 pins.

The SN54ALS1616 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1616 is characterized for operation from 0°C to 70°C.

TABLE 1 — MULTIPLIER INPUT AND OUTPUT FORMAT

OP CODE	OP2	OP1	OP0	INPUT FORMAT	OUTPUT FORMAT	ROUND OPERATION*
0	L	L	L	unsigned X times unsigned Y	Unsigned output	Add 1 to MPR15
1	L	L	H	unsigned X times signed Y	Single signed	Add 1 to MPR15
2	L	H	L	signed X times unsigned Y	Single signed	Add 1 to MPR15
3	L	H	H	signed X times signed Y	Single signed	Add 1 to MPR15
4	H	L	L	signed X times signed Y	Single signed, fractionally adjusted	Add 1 to MPR14
5	H	L	H	unsigned X times signed Y	Single signed, fractionally adjusted	Add 1 to MPR14
6	H	H	L	signed X times signed Y	Double signed	Add 1 to MPR14
7	H	H	H	signed X times signed Y	Single signed, fractionally adjusted	Add 1 to MPR14

*The rounding operation is applied before the shift occurs and has the affect of incrementing the most-significant half of the product if the MSB of the least-significant half (disregarding double sign bit) is high.

TABLE 2 — PIN FUNCTION TABLE

PINS	PIN NAME	FUNCTIONAL DESCRIPTION
54-64, 1-5	X15 thru X0	X data inputs. X15 is the most-significant bit.
24-9	Y15/PR15 thru Y0/PR0	I/O ports for Y data in, less-significant product bits out. Y0/PR0 is the least-significant bit.
40-25	PR31 thru PR16	Outputs for the more-significant product bits. PR31 is the most-significant bit.
45, 50, 51	OP2 thru OP0	Operation-code inputs. See Table 1.
52	RND	Rounding input. When high, implements the rounding function per Table 1.
48	CHGSIGN	Change-sign input. When high, causes the output of the multiplier array to be the two's complement of the product specified by the operation code.
53	CLKX	X clock input. On the low-to-high transition, clocks data in from the X inputs.
8	CLKY	Y clock input. On the low-to-high transition, clocks data in from the Y inputs.
41	CLKOP	OP clock input. On the low-to-high transition, clocks data in from the OP, RND, and CHGSIGN inputs.
7	CLKP	P clock input. On the low-to-high transition, clocks product and overflow data from the multiplier array to the output registers.
44	FT	Feedthrough input. When high, causes product and overflow data to bypass the output registers.
43	OVR	Overflow output. When high, indicates that the input data is too large to be contained within the output format.
6	$\overline{OELS}$	Active-low output-enable input. When high, causes the PR15 through PR0 outputs to be in the high-impedance state.
42	$\overline{OEMS}$	Active-low output-enable input. When high, causes the PR31 through PR16 and OVR outputs to be in the high-impedance state.
49	V_{CC}	Connection for 5-volt power supply.
46, 47	GND	Device ground.

output formats

There are several ways to represent the outputs PR31-PR0 as a function of the outputs of the multiplier array MPR31-MPR0. When a double-signed output is initiated (operation code HHL), the following output format is produced. When X = Y = 8000_{16} an overflow exists.

MOST-SIGNIFICANT HALF OF PRODUCT		LEAST-SIGNIFICANT HALF OF PRODUCT		
PR31	PR30..... PR16	PR15	PR14..... PR1	PR0
MPR30	MPR29.....MPR15	MPR30	MPR14..... MPR1	MPR0

When an unsigned result or a single-signed output is initiated (operation code LLL, LLH, LHL, or LHH), the following output format is produced.

MOST-SIGNIFICANT HALF OF PRODUCT		LEAST-SIGNIFICANT HALF OF PRODUCT		
PR31	PR30 ..... PR16	PR15	PR14 ..... PR1	PR0
MPR31	MPR30 ... MPR16	MPR15	MPR14 .... MPR1	MPR0

When fractional adjust is initiated (operation code HLL, HLH, or HHH), the following output format is produced. When PR31 does not equal PR30, an overflow exists.

MOST-SIGNIFICANT HALF OF PRODUCT		LEAST-SIGNIFICANT HALF OF PRODUCT		
PR31	PR30 ..... PR16	PR15	PR14 ..... PR1	PR0
MPR30	MPR29 ... MPR15	MPR14	MPR13 .... MPR0	'0'

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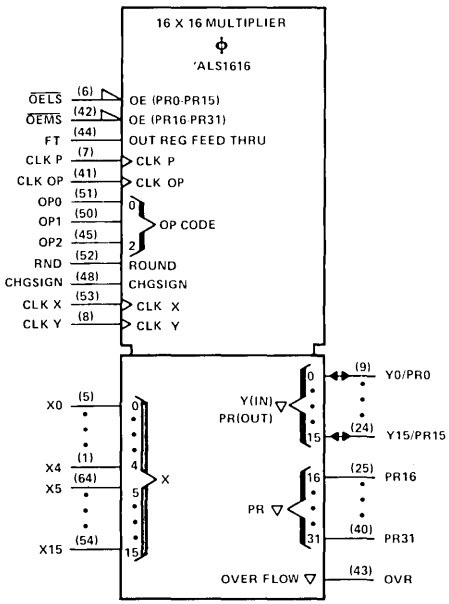
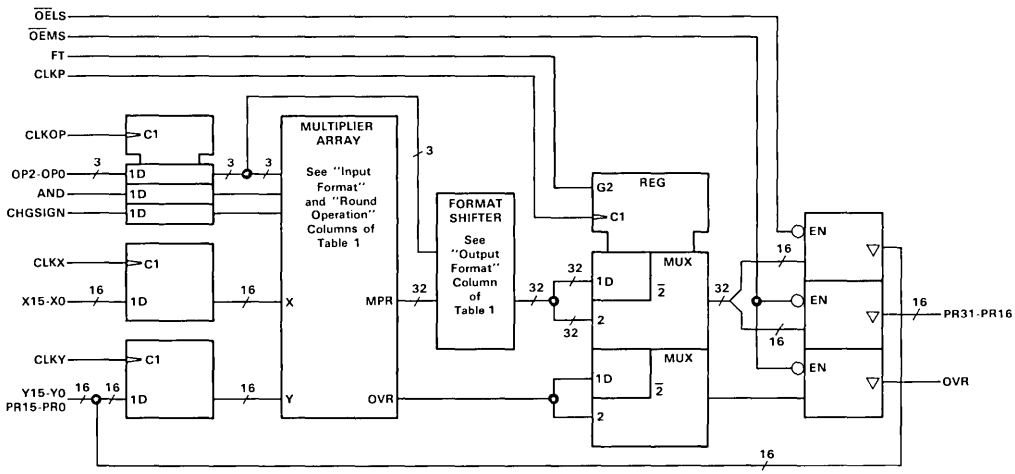
logic symbol



functional block diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Input voltage: All inputs ..... 7 V
I/O ports ..... 5.5 V
Operating free-air temperature range: SN54ALS1616 ..... −55°C to 125°C
SN74ALS1616 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

recommended operating conditions

			SN54ALS1616			SN74ALS1616			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
$t_{w(H)}$	Pulse duration, any clock high		20			20			ns
$t_{w(L)}$	Pulse duration, any clock low		20			20			ns
t_{su}	Setup time	Any X before CLKX ↑	20			20			ns
		Any Y before CLKY ↑	20			20			
		Any OP, CHGSIGN, or RND before CLKOP ↑	20			20			
t_h	Hold time, any input after its clock ↑		0			0			ns
$t_{ICH-OCH}$	Time delay, input clock (CLKX, CLKY, or CLKOP) ↑ to output clock (CLKP) ↑								ns
$t_{OCH-ICH}$	Time delay, output clock ↑ to input clock ↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

NOTE 1: To ensure that the current product is entered in the output registers, new data must not be entered into the input registers before the output registers have been clocked.

Additional information on these products can be obtained from the factory as it becomes available.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS1616			SN74ALS1616			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	PR16-PR31	V_{CC} = 5.5 V	V_O = 2.7 V			20			20	μA
I_{OZL}	PR16-PR31	V_{CC} = 5.5 V	V_O = 0.4 V			−20			−20	μA
I_I	All inputs	V_{CC} = 5.5 V	V_I = 7 V			0.1			0.1	mA
	I/O ports	V_{CC} = 5.5 V	V_I = 5.5 V			0.1			0.1	
I_{IH}	All inputs	V_{CC} = 5.5 V	V_I = 2.7 V			20			20	μA
	I/O ports ▲					20			20	
I_{IL}	All inputs	V_{CC} = 5.5 V	V_I = 0.4 V			−0.1			−0.1	mA
	I/O ports ▲					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_o = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	outputs high							mA
			outputs low							
			outputs disabled							

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

▲ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one-half the true short circuit current I_{OS}.

switching characteristics (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1616			SN74ALS1616			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{ICH-OCH}$min	CLKX, CLKY, or CLKOP	Any PR		40◆			40◆		ns
t_{pd}	CLKX, CLKY, or CLKOP	Any PR		55			55		ns
t_{pd}	CLKP	Any PR		15			15		ns
t_{PZH}	$\overline{OEMS}$	Any PR		10			10		ns
t_{PZL}				10			10		
t_{PHZ}	$\overline{OEMS}$	Any PR		5			5		ns
t_{PLZ}				5			5		
t_{PZH}	$\overline{OELS}$	Any PR		10			10		ns
t_{PZL}				10			10		
t_{PHZ}	$\overline{OELS}$	Any PR		5			5		ns
t_{PLZ}				5			5		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

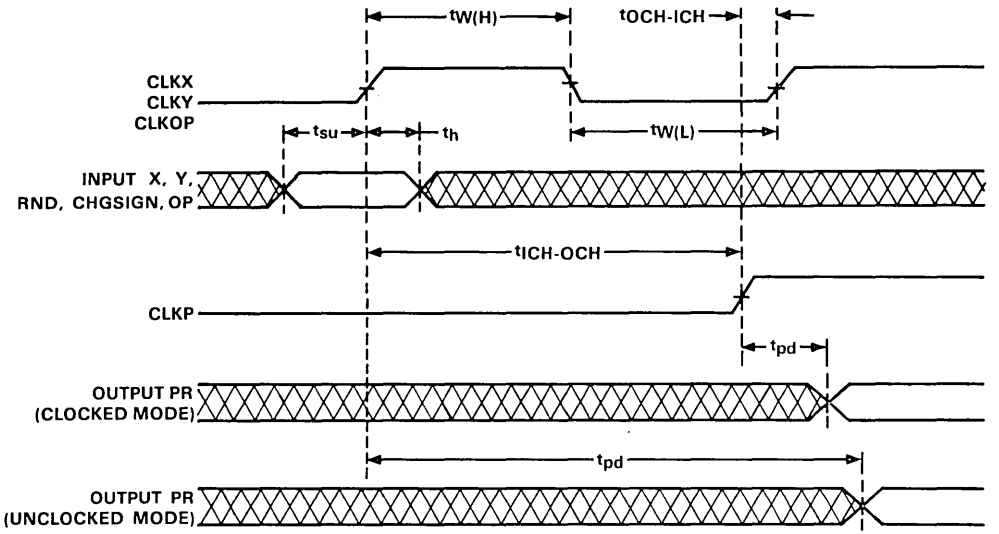
◆ This parameter is the shortest time interval between input clock and output clock for which correct operation occurs. The maximum value of this characteristic, when determined, will become the minimum value for $t_{ICH-OCH}$ under recommended operating characteristics.

NOTE 2: For load circuit and voltage waveforms, see page 1-12.

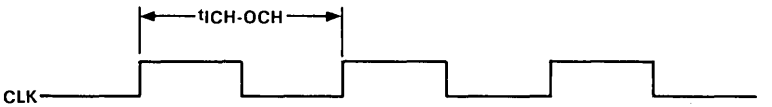
Additional information on these products can be obtained from the factory as it becomes available.

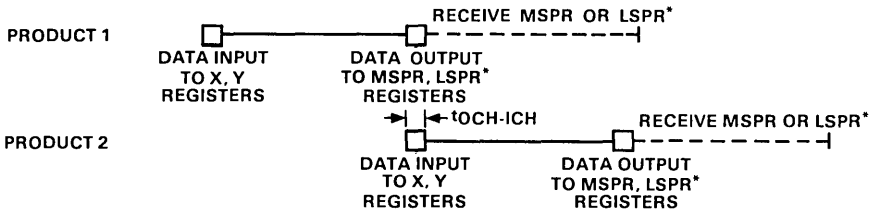
timing diagrams

DETAILED TIMING DIAGRAM



SIMPLIFIED TIMING DIAGRAM
(typical application of data overlap)





*MOST-SIGNIFICANT PRODUCT OR LEAST-SIGNIFICANT PRODUCT.

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TYPICAL APPLICATION INFORMATION

multiplication

The following are some of the functions involved in the multiplication of two 16-bit numbers (X and Y) to produce the product (PR). Table 3 provides multiplication examples.

TABLE 3: MULTIPLICATION EXAMPLES
(RESULTS OF VARIOUS FORMATS AND ROUNDING TECHNIQUES)

OP CODE	X	Y	RND = L CHGSIGN = L	RND = L CHGSIGN = H	RND = H CHGSIGN = L	RND = H CHGSIGN = H
0	AAAA	5555	38E31C72	C71CE38E	38E39C72	C71D638E
1	AAAA	5555	38E31C72	C71CE38E	38E39C72	C71D638E
2	AAAA	5555	E38E1C72	1C71E38E	E38E9C72	1C72638E
3	AAAA	5555	E38E1C72	1C71E38E	E38E9C72	1C72638E
4	AAAA	5555	C71C38E4	38E3C71C	C71CB8E4	38E4471C
5	AAAA	5555	71C638E4	8E39C71C	71C6B8E4	8E3A471C
6	AAAA	5555	C71C9C72	38E3638E	C71CDC72	38E4238
7	AAAA	5555	C71C38E4	38E3C71C	C71CB8E4	38E4471

multiplication of short words

There are several ways to configure a 16-bit multiplier to perform multiplication of smaller words. The sign bits must be guarded and, in the case of rounding, the proper binary point must be maintained. Three of the methods that can be used are as follows:

1. Left Justify and Zero Fill — In this method the product is confined to the most-significant half of the output register. This allows the Y port to always be in the input mode. The least-significant product is zero, RND is inactive, and OVR is inactive.

2. Right Justify and Sign Extend — In this method, the product is confined to the least-significant half of the output register. RND is grounded. If $FF80_{16}$ is multiplied by $FF80_{16}$ and a signed fractional output is desired, the result will overflow into the most-significant half of the output register.

3. Alignment for Rounding — To obtain the proper answer when rounding, the inputs should be right filled with four zeros and sign extended to the left. The product will be in positions PR8 through PR23 and the rounding will be correct. OVR occurs if the value of PR23 is not the same as the value of PR24.

extending word length

The multiplier (XO through X15) can be expanded to larger word lengths by generating 32-bit partial products. The partial products are summed, the proper binary weight is maintained, and the signs of signed partial products are extended.

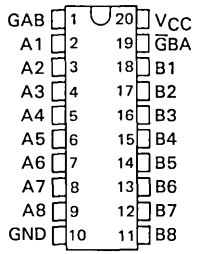
overflow condition

When the input values are too large, certain operations will produce an overflow condition. The overflow may occur when the output format is fractional or double-signed. When in these formats and the two most-significant bits out of the multiplier array are different, PR31 no longer contains the proper sign bit. The overflow output will also become active if CHGSIGN is high, both inputs are unsigned, and the unsigned product cannot be converted to a signed two's-complement number.

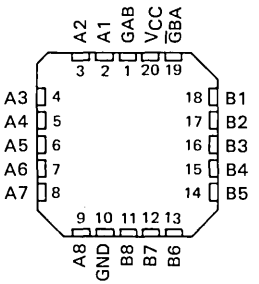
- **Bus Transceivers in High-Density 20-Pin DIPs and the New Plastic and Ceramic Chip Carriers Packages**
- **Local Bus Latch Capability**
- **Choice of True or Inverting Logic**
- **Dependable Texas Instruments Quality and Reliability**
- **Choice of 3-State or Open-Collector Outputs**

DEVICE	OUTPUT	LOGIC
'ALS1620	3-State	Inverting
'ALS1621	Open-Collector	True
'ALS1622	Open-Collector	Inverting
'ALS1623	3-State	True

SN54ALS' . . . J PACKAGE
SN74ALS' . . . N PACKAGE
(TOP VIEW)



SN54ALS' . . . FH PACKAGE
SN74ALS' . . . FN PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 'ALS1620 thru 'ALS1623 the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the 'ALS1621 and 'ALS1623 or complementary for the 'ALS1620 and 'ALS1622.

The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 24 mA. There are no -1 versions of the SN54ALS' parts.

The SN54ALS1620 thru SN54ALS1623 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1620 thru SN74ALS1623 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

ENABLE $\overline{G}$BA	INPUTS GAB	OPERATION 'ALS1620, 'ALS1622	OPERATION 'ALS1621, 'ALS1623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Isolation	Isolation
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus	B data to A bus, A data to B bus

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

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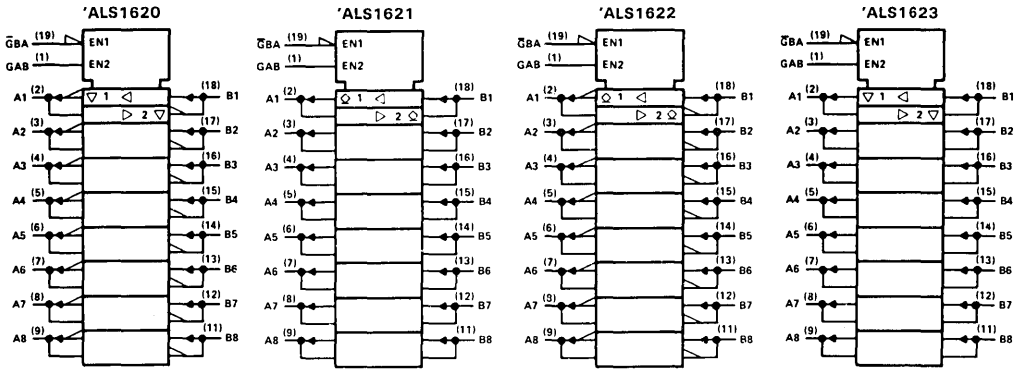
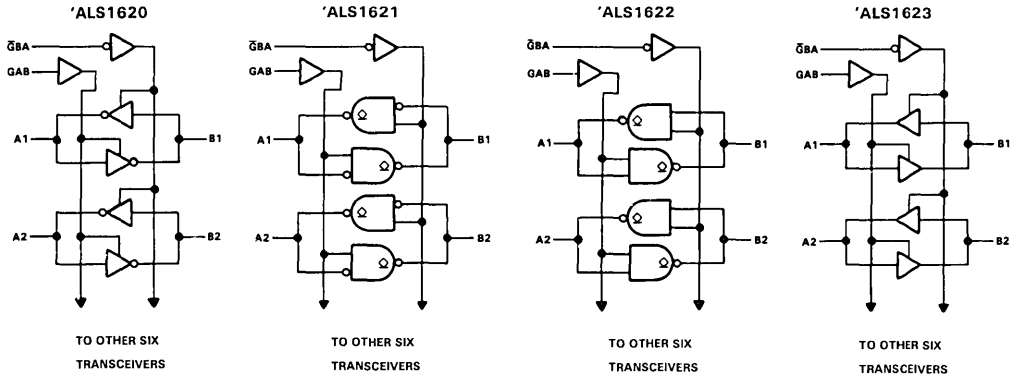
logic symbols



functional block diagrams (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS1620, SN54ALS1623 . . . . . −55°C to 125°C
SN74ALS1620, SN74ALS1623 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

2

recommended operating conditions

		SN54ALS1620 SN54ALS1623			SN74ALS1620 SN74ALS1623			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12				mA
							−15	
I_{OL}	Low-level output current			8				mA
							16	
							24†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 24-mA limit applies for the SN74ALS1620-1 and SN74ALS1623-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS1620 SN54ALS1623			SN74ALS1620 SN74ALS1623			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 24 mA for -1 versions)	I_{OL} = 16 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports▲					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports▲					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high							mA
			Outputs low							
			Outputs disabled							

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
▲For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
Additional information on these products can be obtained from the factory as it becomes available.

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'ALS1620 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1620			SN74ALS1620			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	B							ns
t_{PHL}									
t_{PLH}	B	A							ns
t_{PHL}									
t_{PZH}	$\overline{G}BA$	A							ns
t_{PZL}									
t_{PHZ}	$\overline{G}BA$	A							ns
t_{PLZ}									
t_{PZH}	GAB	B							ns
t_{PZL}									
t_{PHZ}	GAB	B							ns
t_{PLZ}									

'ALS1623 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1623			SN74ALS1623			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	B							ns
t_{PHL}									
t_{PLH}	B	A							ns
t_{PHL}									
t_{PZH}	$\overline{G}BA$	A							ns
t_{PZL}									
t_{PHZ}	$\overline{G}BA$	A							ns
t_{PLZ}									
t_{PZH}	GAB	B							ns
t_{PZL}									
t_{PHZ}	GAB	B							ns
t_{PLZ}									

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs and I/O ports . . . . . 7 V
Operating free-air temperature range: SN54ALS1621, SN54ALS1622 . . . . . −55 °C to 125 °C
SN74ALS1621, SN74ALS1622 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS1621 SN54ALS1622			SN74ALS1621 SN74ALS1622			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			8				mA
							16	
							24†	
T_A	Operating free-air temperature	−55		125	0		70	°C

† The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 24-mA limit applies for the SN74ALS1621-1 and SN74ALS1622-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS1621 SN54ALS1622			SN74ALS1621 SN74ALS1622			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 24 mA for -1 versions)	I_{OL} = 16 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports▲					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports▲					−0.1			−0.1	
I_{CC}		V_{CC} = 5.5 V	Outputs high							mA
			Outputs low							

‡ All typical values are at V_{CC} = 5 V, T_A = 25 °C.
▲ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

Additional information on these products can be obtained from the factory as it becomes available.

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'ALS1621 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1621			SN74ALS1621			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	B							ns
t_{PHL}									
t_{PLH}	B	A							ns
t_{PHL}									
t_{PLH}	$\overline{G}BA$	A							ns
t_{PHL}									
t_{PLH}	GAB	B							ns
t_{PHL}									

'ALS1622 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1622			SN74ALS1622			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	B							ns
t_{PHL}									
t_{PLH}	B	A							ns
t_{PHL}									
t_{PLH}	$\overline{G}BA$	A							ns
t_{PHL}									
t_{PLH}	GAB	B							ns
t_{PHL}									

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

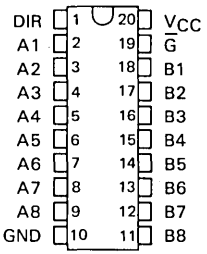
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

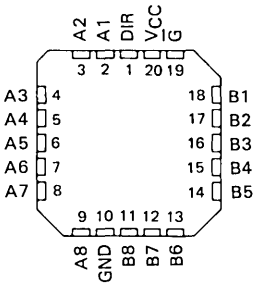
- **Bidirectional Bus Transceivers in High-Density 20-Pin Packages**
- **Low-Power Version of 'ALS638 and 'ALS639**
- **Choice of True or Inverting Logic**
- **A bus Outputs are Open-Collector; B Bus Outputs are 3-State**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

2

SN54ALS1638, SN54ALS1639 . . . J PACKAGE
SN74ALS1638, SN74ALS1639 . . . N PACKAGE
(TOP VIEW)



SN54ALS1638, SN54ALS1639 . . . FH PACKAGE
SN74ALS1638, SN74ALS1639 . . . FN PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between open-collector and 3-State buses. The devices transmit data from the A bus (open-collector) to the B bus (3-state) or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to enable the device so the buses are effectively isolated.

DEVICE	A OUTPUT	B OUTPUT	LOGIC
'ALS1638	Open-Collector	3-State	Inverting
'ALS1639	Open-Collector	3-State	True

The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 24 milliamperes. There are no -1 versions of the SN54ALS' parts.

The SN54ALS1638 and SN54ALS1639 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1638 and SN74ALS1639 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

CONTROL INPUTS		OPERATION	
$\overline{G}$	DIR	'ALS1638	'ALS1639
L	L	B data to A bus	B data to A bus
L	H	A data to B bus	A data to B bus
H	X	Isolation	Isolation

ADVANCE INFORMATION

This document contains information on a new product. Specifications are subject to change without notice.

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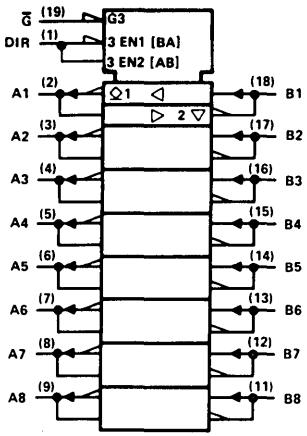
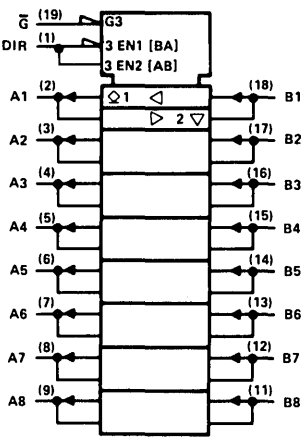
logic symbols

'ALS1638



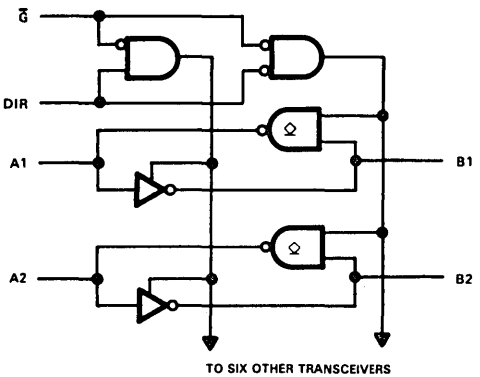
'ALS1639



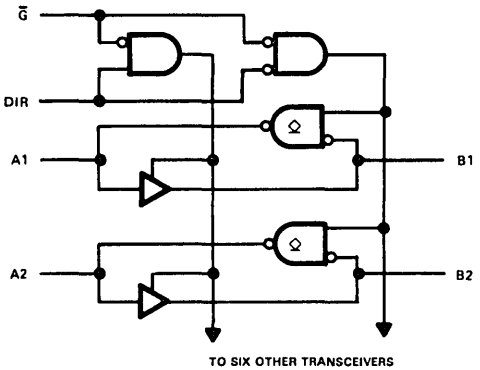
Pin numbers shown are for J and N packages.

functional block diagrams (positive logic)

'ALS1638



'ALS1639



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
A bus I/O ports . . . . . 7 V
B bus I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS1638, SN54ALS1639 . . . . . −55 °C to 125 °C
SN74ALS1638, SN74ALS1639 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

2

recommended operating conditions

			SN54ALS1638 SN54ALS1639			SN74ALS1638 SN74ALS1639			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level voltage	A ports			5.5			5.5	V
I_{OH}	High-level output current	B ports			−12				mA
								−15	
I_{OL}	Low-level output current	A or B ports			8				mA
								16	
								24†	
T_A	Operating free-air temperature		−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 24-mA limit applies for the SN74ALS1638-1 and SN74ALS1639-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS1638 SN54ALS1639			SN74ALS1638 SN74ALS1639			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	A ports	V_{CC} = 4.5 V,	V_O = 5.5 V			0.1			0.1	mA
V_{OH}	B ports	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	A or B ports	V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 24 mA for -1 versions)	I_{OL} = 16 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports▲					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports▲					−0.1			−0.1	
I_O§	B ports	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		21			21		mA
			Outputs low		23			23		
			Outputs disabled		25			25		

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
▲For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
Additional information on these products can be obtained from the factory as it becomes available.

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'ALS1638 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω (A outputs), R1 = R2 = 500 Ω (B outputs) T_A = MIN to MAX						UNIT
			SN54ALS1638			SN74ALS1638			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	B		6			6		ns
t_{PHL}				21			21		
t_{PLH}	B	A		6			6		ns
t_{PHL}				8			8		
t_{PLH}	$\overline{G}$, DIR	A		23			23		ns
t_{PHL}				17			17		
t_{PZH}	$\overline{G}$	B		12			12		ns
t_{PZL}				15			15		
t_{PHZ}	$\overline{G}$	B		6			6		ns
t_{PLZ}				7			7		

'ALS1639 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω (A outputs), R1 = R2 = 500 Ω (B outputs), T_A = MIN to MAX						UNIT
			SN54ALS1639			SN74ALS1639			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	B		7			7		ns
t_{PHL}				21			21		
t_{PLH}	B	A		7			7		ns
t_{PHL}				9			9		
t_{PLH}	$\overline{G}$, DIR	A		23			23		ns
t_{PHL}				19			19		
t_{PZH}	$\overline{G}$	B		14			14		ns
t_{PZL}				17			17		
t_{PHZ}	$\overline{G}$	B		7			7		ns
t_{PLZ}				9			9		

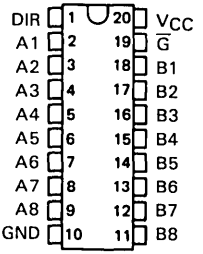
‡All typical values at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

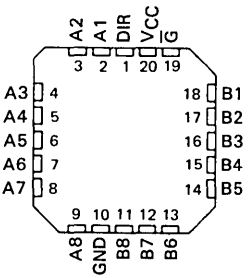
- **Bidirectional Bus Transceivers in High-Density 20-Pin Packages**
- **Lower-Power Versions of 'ALS640 Series**
- **Choice of True or Inverting Logic**
- **Choice of 3-State or Open-Collector Outputs**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	OUTPUT	LOGIC
'ALS1640	3-State	Inverting
'ALS1641	Open-Collector	True
'ALS1642	Open-Collector	Inverting
'ALS1643	3-State	True and Inverting
'ALS1644	Open-Collector	True and Inverting
'ALS1645	3-State	True

SN54ALS' . . . J PACKAGE
SN74ALS' . . . N PACKAGE
(TOP VIEW)



SN54' . . . FH PACKAGE
SN74' . . . FN PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so the buses are effectively isolated.

The -1 versions of the SN74ALS1640 thru SN74ALS1645 are identical to the standard versions except that the recommended maximum I_{OL} is increased to 24 milliamperes. There are no -1 versions of the SN54ALS1640 thru SN54ALS1645.

The SN54ALS1640 thru SN54ALS1645 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1640 thru SN74ALS1645 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

CONTROL INPUTS		OPERATION		
$\overline{G}$	DIR	'ALS1640 'ALS1642	'ALS1641 'ALS1645	'ALS1643 'ALS1644
L	L	$\overline{B}$ data to A bus	B data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus	$\overline{A}$ data to B bus
H	X	Isolation	Isolation	Isolation

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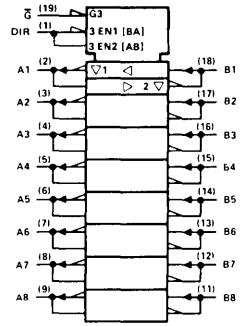
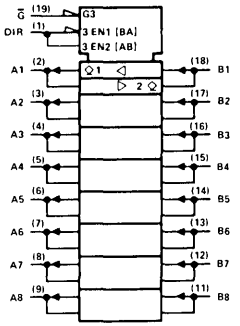
logic symbols

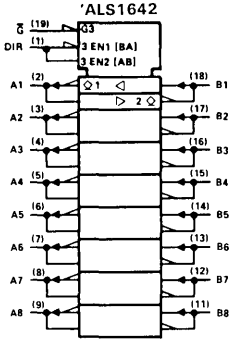
'ALS1640



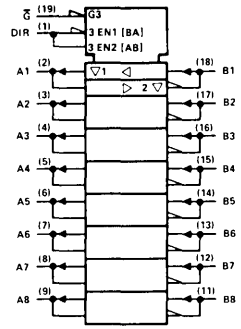
'ALS1641



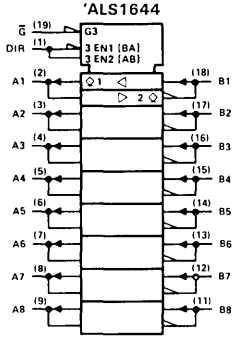
'ALS1642



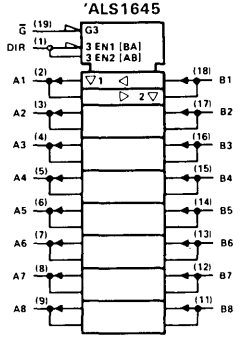
'ALS1643



'ALS1644

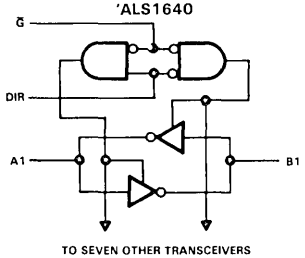


'ALS1645

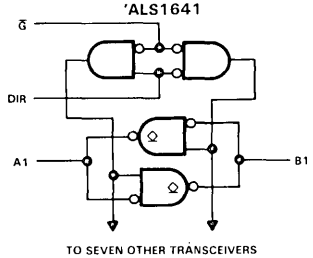


logic diagrams (positive logic)

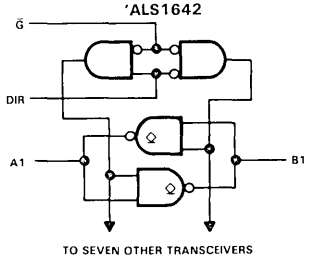
'ALS1640



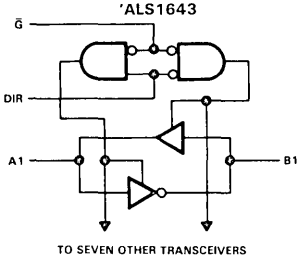
'ALS1641



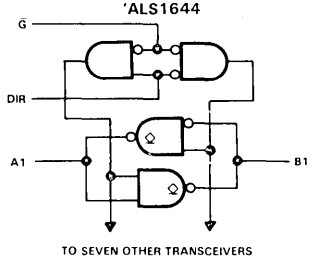
'ALS1642



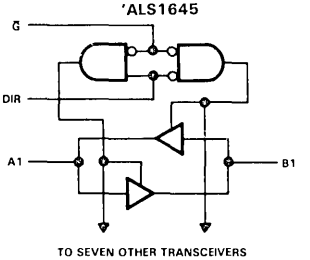
'ALS1643



'ALS1644



'ALS1645



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS1640, SN54ALS1643, SN54ALS1645 . . . . . −55 °C to 125 °C
SN74ALS1640, SN74ALS1643, SN74ALS1645 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS1640 SN54ALS1643 SN54ALS1645			SN74ALS1640 SN74ALS1643 SN74ALS1645			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12				mA
							−15	
I_{OL}	Low-level output current			8				mA
							16	
							24†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 24-mA limit applies for the SN74ALS1640-1, SN74ALS1643-1, and SN74ALS1645-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN54ALS1640 SN54ALS1643 SN54ALS1645			SN74ALS1640 SN74ALS1643 SN74ALS1645			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.4	3.2		2.4	3.2		V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA		2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA					2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 8 mA			0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 24 mA for -1 versions)	I_{OL} = 16 mA						0.35	0.5	
I_I	Control Inputs	V_{CC} = 5.5 V,	V_I = 7 V				0.1			0.1	mA
	A or B Ports	V_{CC} = 5.5 V,	V_I = 5.5 V				0.1			0.1	
I_{IH}	Control Inputs	V_{CC} = 5.5 V,	V_I = 2.7 V				20			20	μA
	A or B ports▲						20			20	
I_{IL}	Control Inputs	V_{CC} = 5.5 V,	V_I = 0.4 V				−0.1			−0.1	mA
	A or B ports▲						−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V		−30		−112	−30		−112	mA
I_{CC}	'ALS1640	V_{CC} = 5.5 V				18	32		18	25	mA
	'ALS1643					22			22		
	'ALS1645					23	41		23	39	

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
▲For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
Additional information on these products can be obtained from the factory as it becomes available.

ADVANCE INFORMATION

This page contains information on a new product. Specifications are subject to change without notice.

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'ALS1640 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1640			SN74ALS1640			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	B or A	5		21	5		17	ns
t_{PHL}			3		13	3		11	
t_{PZH}	$\overline{G}$	A or B	5		27	5		23	ns
t_{PZL}			10		30	10		27	
t_{PHZ}	$\overline{G}$	A or B	3		16	3		13	ns
t_{PLZ}			5		23	5		21	

'ALS1643 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1643			SN74ALS1643			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	B		7			7		ns
t_{PHL}				7			7		
t_{PLH}	B	A		8			8		ns
t_{PHL}				8			8		
t_{PZH}	$\overline{G}$	A		18			18		ns
t_{PZL}				21			21		
t_{PHZ}	$\overline{G}$	A		12			12		ns
t_{PLZ}				13			13		
t_{PZH}	$\overline{G}$	B		18			18		ns
t_{PZL}				21			21		
t_{PHZ}	$\overline{G}$	B		12			12		ns
t_{PLZ}				13			13		

'ALS1645 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1645		SN74ALS1645		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	4	15	4	13	ns
t_{PHL}			4	15	4	13	
t_{PZH}	$\overline{G}$	A or B	10	27	10	25	ns
t_{PZL}			13	32	13	29	
t_{PHZ}	$\overline{G}$	A or B	4	20	4	18	ns
t_{PLZ}			6	23	5	21	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

ADVANCE INFORMATION

This page contains information on a new product. Specifications are subject to change without notice.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs and I/O ports . . . . . 7 V
Operating free-air temperature range: SN54ALS1641, SN54ALS1642, SN54ALS1644 . . . . . −55°C to 125°C
SN74ALS1641, SN74ALS1642, SN74ALS1644 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

2

recommended operating conditions

		SN54ALS1641 SN54ALS1642 SN54ALS1644			SN74ALS1641 SN74ALS1642 SN74ALS1644			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			8				mA
							16	
							24†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 24-mA limit applies for the SN74ALS1641-1, SN74ALS1642-1, and SN74ALS1644-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS1641 SN54ALS1642 SN54ALS1644			SN74ALS1641 SN74ALS1642 SN74ALS1644			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 24 mA for -1 versions)	I_{OL} = 16 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports▲					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports▲					−0.1			−0.1	
I_{CC}	'ALS1641	V_{CC} = 5.5 V			23			23		mA
	'ALS1642				20			20		
	'ALS1644				22			22		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
▲For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

'ALS1641 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1641			SN74ALS1641			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	B or A							ns
t_{PHL}									
t_{PLH}	$\overline{G}$ or DIR	A or B							ns
t_{PHL}									

'ALS1642 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1642			SN74ALS1642			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	B or A							ns
t_{PHL}									
t_{PLH}	$\overline{G}$ or DIR	A or B							ns
t_{PHL}									

'ALS1644 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1644			SN74ALS1644			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	B							ns
t_{PHL}									
t_{PLH}	B	A							ns
t_{PHL}									
t_{PLH}	$\overline{G}$ or DIR	A							ns
t_{PHL}									
t_{PLH}	$\overline{G}$ or DIR	B							ns
t_{PHL}									

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

Programmable Logic Arrays

- Standard 20-Pin, 300-mil Packages
- Choice of Operating Speeds
  -1 Parts . . . 35 MHz Max
  -2 Parts . . . 25 MHz Max
- Plug-In Compatible with popular PAL16L8, PAL16R4, PAL16R6, PAL16R8 Arrays

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PL16L8	10	2	0	6
'PL16R4	8	0	4 (3-state)	4
'PL16R6	8	0	6 (3-state)	2
'PL16R8	8	0	8 (3-state)	0

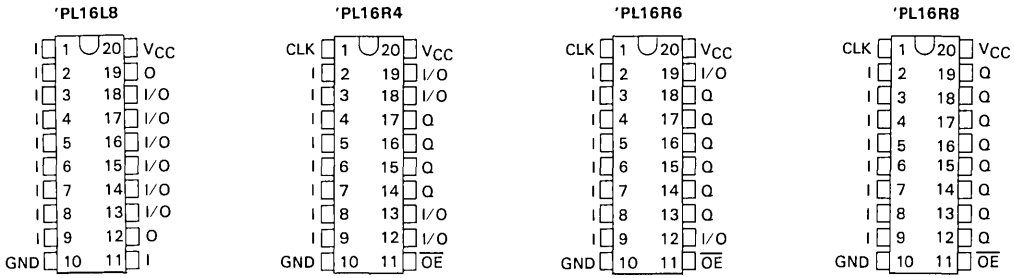
description

These fixed-OR arrays provide 3-state outputs for bus-oriented systems. They combine Advanced Low-Power Schottky technology with proven titanium-tungsten fuses for reliable, high-performance substitutes for conventional TTL logic. Standard arrays and programmability allow quick design of "custom" functions and more compact boards.

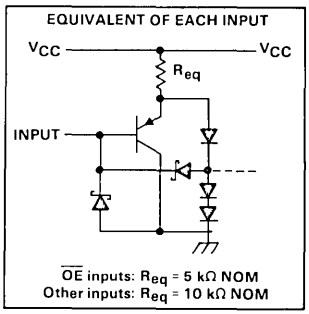
The SN54PL16' is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74PL16' is characterized for operation from 0°C to 70°C.

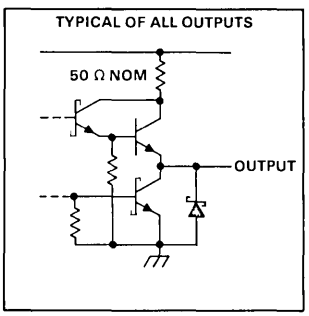
pin assignments in operating mode (voltages at pins 1 and 11 less than V_{IHH})

SN54PL' . . . J PACKAGE
SN74PL' . . . N PACKAGE
(TOP VIEWS)



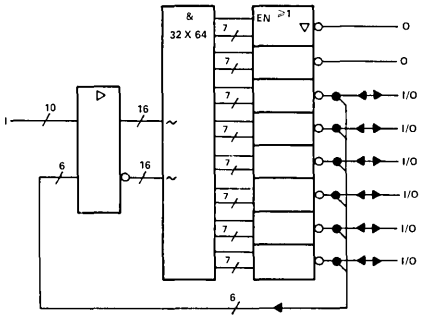
schematics of inputs and outputs



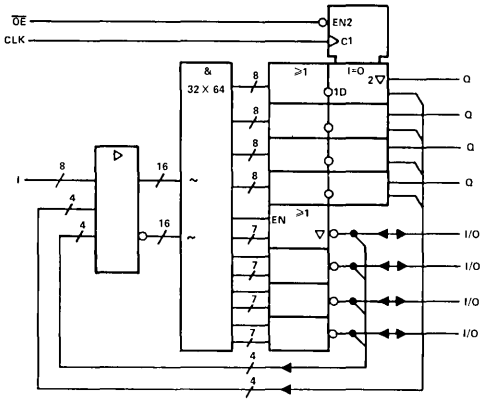


functional block diagrams (positive logic)

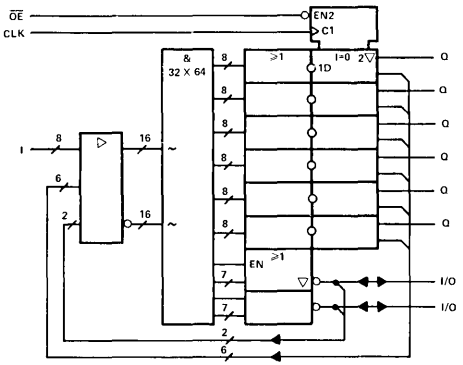
'PL16L8



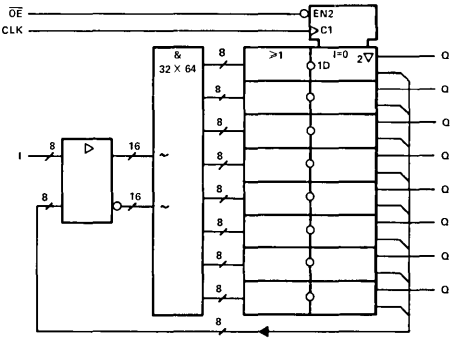
'PL16R4



'PL16R6



'PL16R8



~ denotes fused inputs

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage (see Note 1) ..... 5.5 V
Voltage applied to a disabled output (see Note 1) ..... 5.5 V
Operating free-air temperature range: SN54PL' ..... −55°C to 125°C
SN74PL' ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER		SN54PL16'			SN74PL16'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		5.5	2		5.5	V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output voltage			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics, over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS†		SN54PL16'			SN74PL16'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN,	I_{OH} = MAX	2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN,	I_{OL} = MAX		0.25	0.4		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX,	V_O = 2.7 V			20			20	μA
	I/O ports					100			100	
I_{OZL}	Outputs	V_{CC} = MAX,	V_O = 0.4 V			−20			−20	μA
	I/O ports					−250			−250	
I_I		V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	$\overline{OE}$ Input	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
	All others					−0.2			−0.2	
I_O		V_{CC} = MAX,	V_O = 2.25 V	−15	−33	−65	−15	−33	−65	mA
I_{CC}	−1 Parts	V_{CC} = MAX,	V_I = 0 V,		140	185		140	180	mA
	−2 Parts	Outputs open			60	95		60	90	

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

'PL16R4, 'PL16R6, 'PL16R8 timing requirements

		-1 PARTS			-2 PARTS			UNIT
		MIN	TYP*	MAX	MIN	TYP*	MAX	
f_{clock}	Clock frequency	0		35	0		25	MHz
t_w	Pulse duration, clock high or low	12			12			ns
t_{su}	Setup time, input or feedback before CLK↑	15			15			ns
t_h	Hold time, input or feedback after CLK↑	0			0			ns

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	-1 PARTS			-2 PARTS			UNIT
				MIN	TYP*	MAX	MIN	TYP*	MAX	
f_{max}			R_L = 500 Ω, C_L = 50 pf	35	45		25	35		MHz
t_{pd}	I, I/O	O, I/O			16	25		25	35	ns
t_{pd}	CLK↑	O, I/O			10	15		15	20	ns
t_{en}	$\overline{OE}$↓	Q			8	12		13	17	ns
t_{dis}	$\overline{OE}$↓	Q			6	10		10	14	ns
t_{en}	I, I/O	O, I/O			15	20		19	25	ns
t_{dis}	I, I/O	O, I/O			7	12		10	18	ns

*All typical values are at V_{CC} = 5 V, T_A = 25°C.

programming parameters

			MIN	NOM	MAX	UNIT
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
V_{IHH}	Program-pulse input voltage		10.25	10.5	10.75	V
I_{IHH}	Program-pulse input current	PO			50	mA
		PGM VERIFY, L/R			25	
		PGM ENABLE, PI, PA			5	
I_{CCHH}	Program-pulse supply current				400	mA
t_{w1}	Program-pulse duration at PO pins		10		50	μs
t_{w2}	Pulse duration at PGM VERIFY		100			ns
	Program-pulse duty cycle at PO pins				25	%
t_{su}	Setup time		100			ns
t_h	Hold time		100			ns
t_{d1}	Delay time from V_{CC} to 6 V to PGM VERIFY ↑		100			μs
t_{d2}	Delay time from PGM VERIFY ↑ to valid output		200			ns
	Input voltage at pins 1 and 13 to open verify-protect (security) fuse		20	21	22	V
	Input current to open verify-protect (security) fuse				400	mA
	Pulse duration to open verify-protect (security) fuse		20		50	ms

TEXAS INSTRUMENTS
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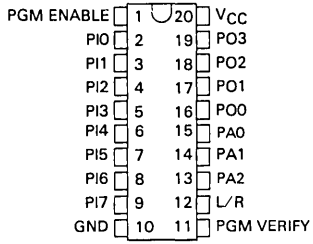
pin assignments in programming mode (PGM ENABLE, pin 1 or pin 11, at V_{IHH})

PRODUCT TERMS 0 THRU 31
(TOP VIEW)



PRODUCT TERMS 32 THRU 63
(TOP VIEW)

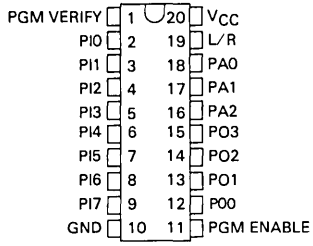


TABLE 1 — INPUT LINE SELECT

INPUT LINE NUMBER	PIN NAME								
	PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0	L/R
0	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	H	HH	HH	HH	HH	HH	HH	HH
28	L	HH	HH	HH	HH	HH	HH	HH	Z
29	H	HH	HH	HH	HH	HH	HH	HH	Z
30	L	HH	HH	HH	HH	HH	HH	HH	HH
31	H	HH	HH	HH	HH	HH	HH	HH	HH

TABLE 2 — PRODUCT LINE SELECT

PRODUCT LINE NUMBER	PIN NAME						
	PO0	PO1	PO2	PO3	PA2	PA1	PA0
0, 32	Z	Z	Z	HH	Z	Z	Z
1, 33	Z	Z	Z	HH	Z	Z	HH
2, 34	Z	Z	Z	HH	Z	HH	Z
3, 35	Z	Z	Z	HH	Z	HH	HH
4, 36	Z	Z	Z	HH	HH	Z	Z
5, 37	Z	Z	Z	HH	HH	Z	HH
6, 38	Z	Z	Z	HH	HH	HH	Z
7, 39	Z	Z	Z	HH	HH	HH	HH
8, 40	Z	Z	HH	Z	Z	Z	Z
9, 41	Z	Z	HH	Z	Z	Z	HH
10, 42	Z	Z	HH	Z	Z	HH	Z
11, 43	Z	Z	HH	Z	Z	HH	HH
12, 44	Z	Z	HH	Z	HH	Z	Z
13, 45	Z	Z	HH	Z	HH	Z	HH
14, 46	Z	Z	HH	Z	HH	HH	Z
15, 47	Z	Z	HH	Z	HH	HH	HH
16, 48	Z	HH	Z	Z	Z	Z	Z
17, 49	Z	HH	Z	Z	Z	Z	HH
18, 50	Z	HH	Z	Z	Z	HH	Z
19, 51	Z	HH	Z	Z	Z	HH	HH
20, 52	Z	HH	Z	Z	HH	Z	Z
21, 53	Z	HH	Z	Z	HH	Z	HH
22, 54	Z	HH	Z	Z	HH	HH	Z
23, 55	Z	HH	Z	Z	HH	HH	HH
24, 56	HH	Z	Z	Z	Z	Z	Z
25, 57	HH	Z	Z	Z	Z	Z	HH
26, 58	HH	Z	Z	Z	Z	HH	Z
27, 59	HH	Z	Z	Z	Z	HH	HH
28, 60	HH	Z	Z	Z	HH	Z	Z
29, 61	HH	Z	Z	Z	HH	Z	HH
30, 62	HH	Z	Z	Z	HH	HH	Z
31, 63	HH	Z	Z	Z	HH	HH	HH

L = V_{IL}, H = V_{IH}, HH = V_{IHH}, Z = high impedance (e.g., 10 kΩ to 5 V)

programming procedure for array fuses

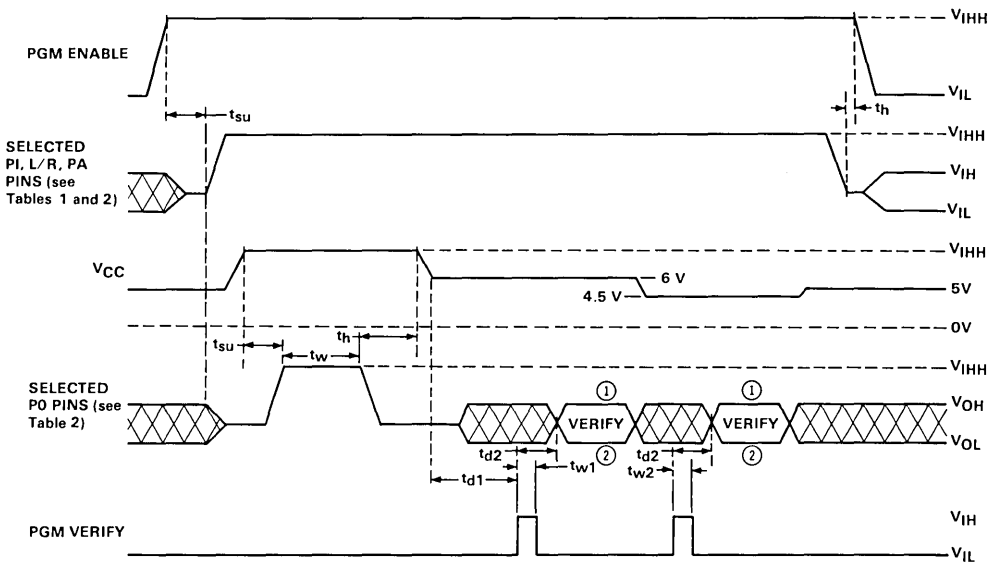
Array fuses are programmed using a linear select method. Each fuse can be opened by selecting the appropriate (one of 32) input line and then pulsing the correct (one of 64) product line. The levels for selecting input lines and product lines are shown in Tables 1 and 2.

Step 1	Raise PGM ENABLE to V_{IHH}.
Step 2	Select an input line by applying appropriate levels to L/R and PI pins.
Step 3	Begin selection of the output line with appropriate conditions on PA pins.
Step 4	Raise V_{CC} to V_{IHH}.
Step 5	Blow the fuse by pulsing the appropriate PO pin to V_{IHH} as shown in Table 2 for the product line.
Step 6	Lower V_{CC} to 6 volts and pulse PGM VERIFY. The PO pin selected in Step 4 will be less than V_{OL} if the fuse is open.
Step 7	Lower V_{CC} to 4.5 volts and pulse PGM VERIFY. The PO pin selected in Step 4 will be less than V_{OL} if the fuse is open.

Steps 1 through 7 may be repeated if the verification does not indicate that the fuse was successfully programmed (blown), but no more than four times. Verification is possible only with the verify-protect fuse intact.

To prevent further verification, two last fuses may be blown by raising pin 1 and pin 11 to Vp. V_{CC} is not required during this operation.

programming waveforms



① A high level during the verify interval indicates that programming has not been successful.
② A low level during the verify interval indicates that programming has been successful.

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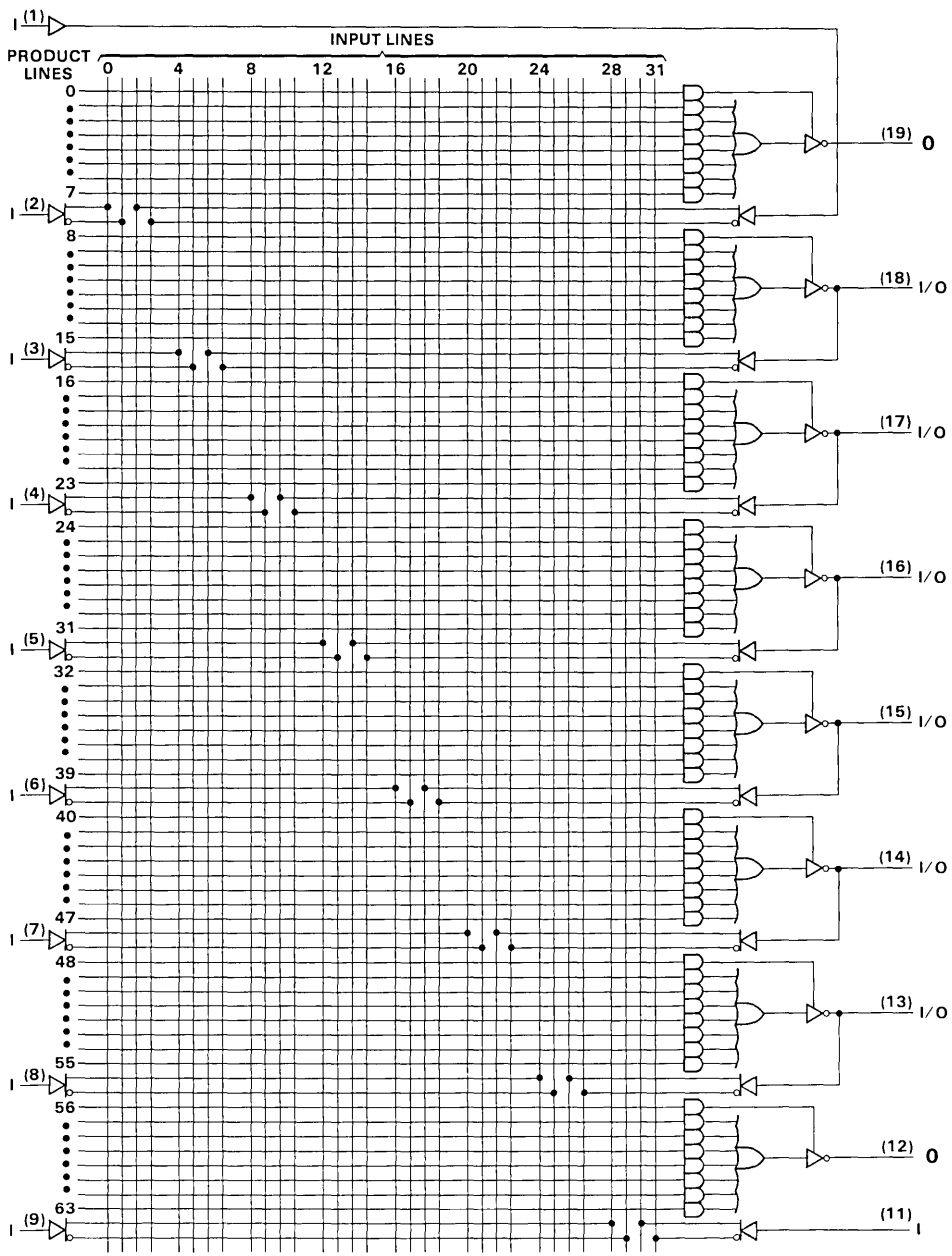
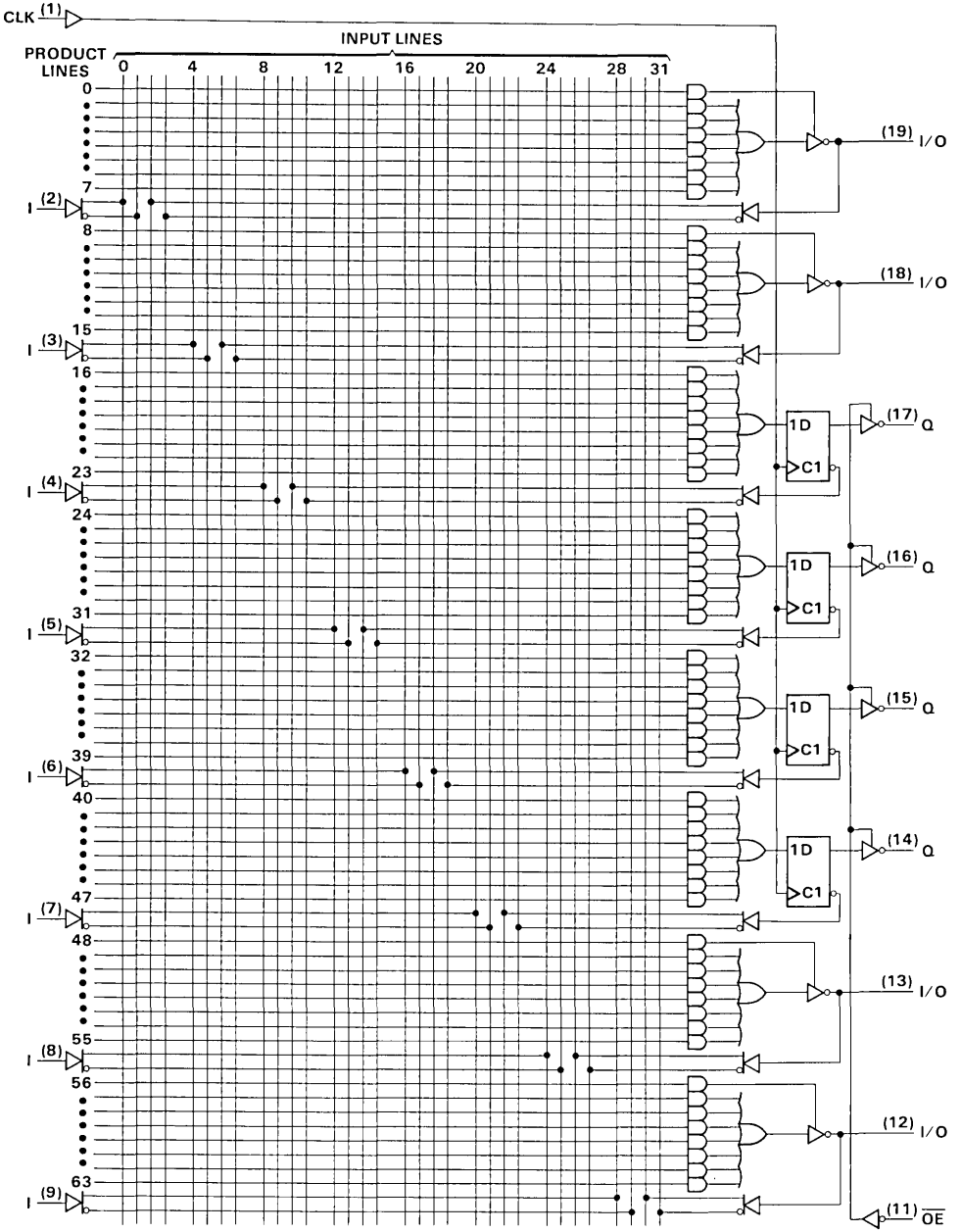
LOGIC DIAGRAM



LOGIC DIAGRAM



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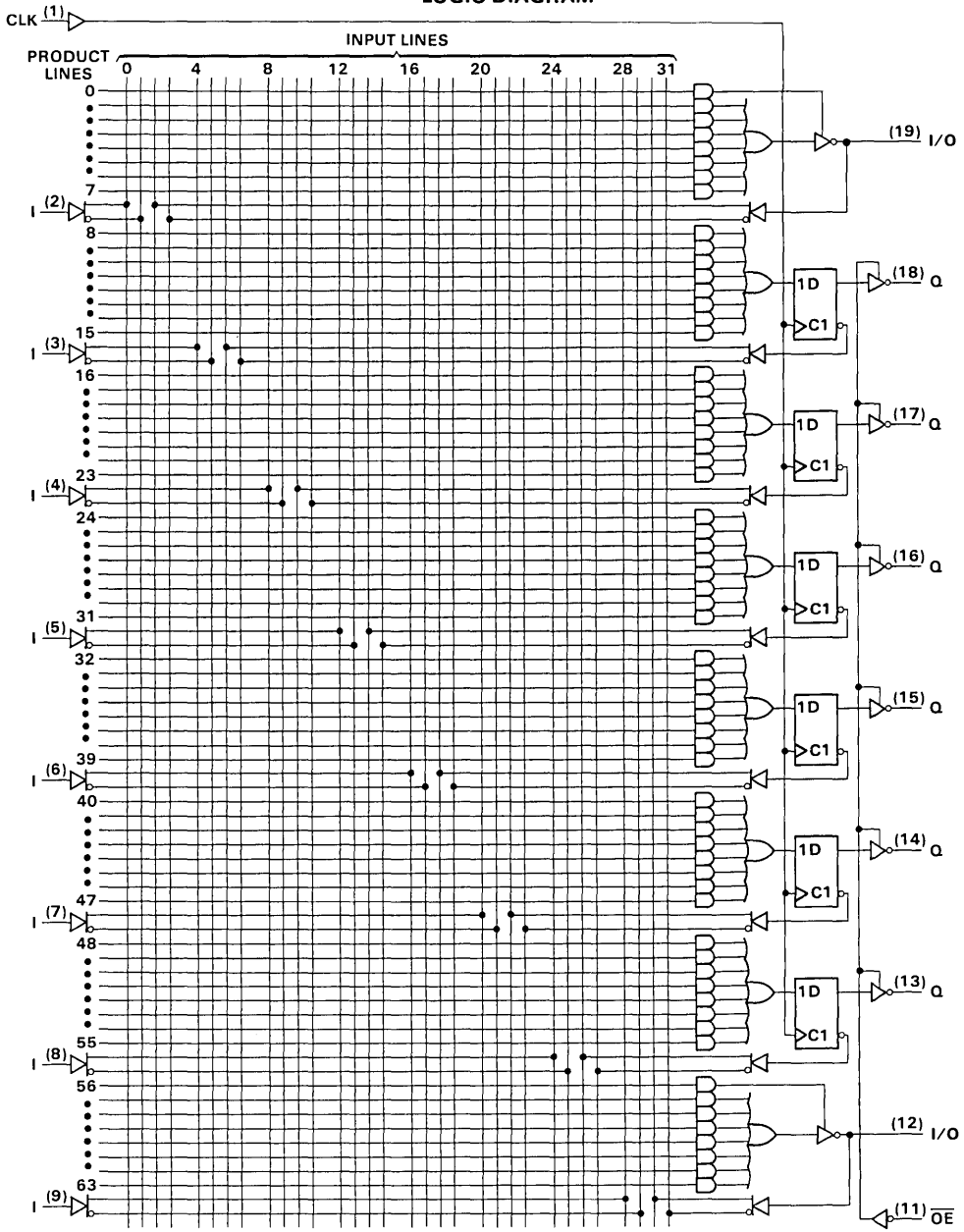
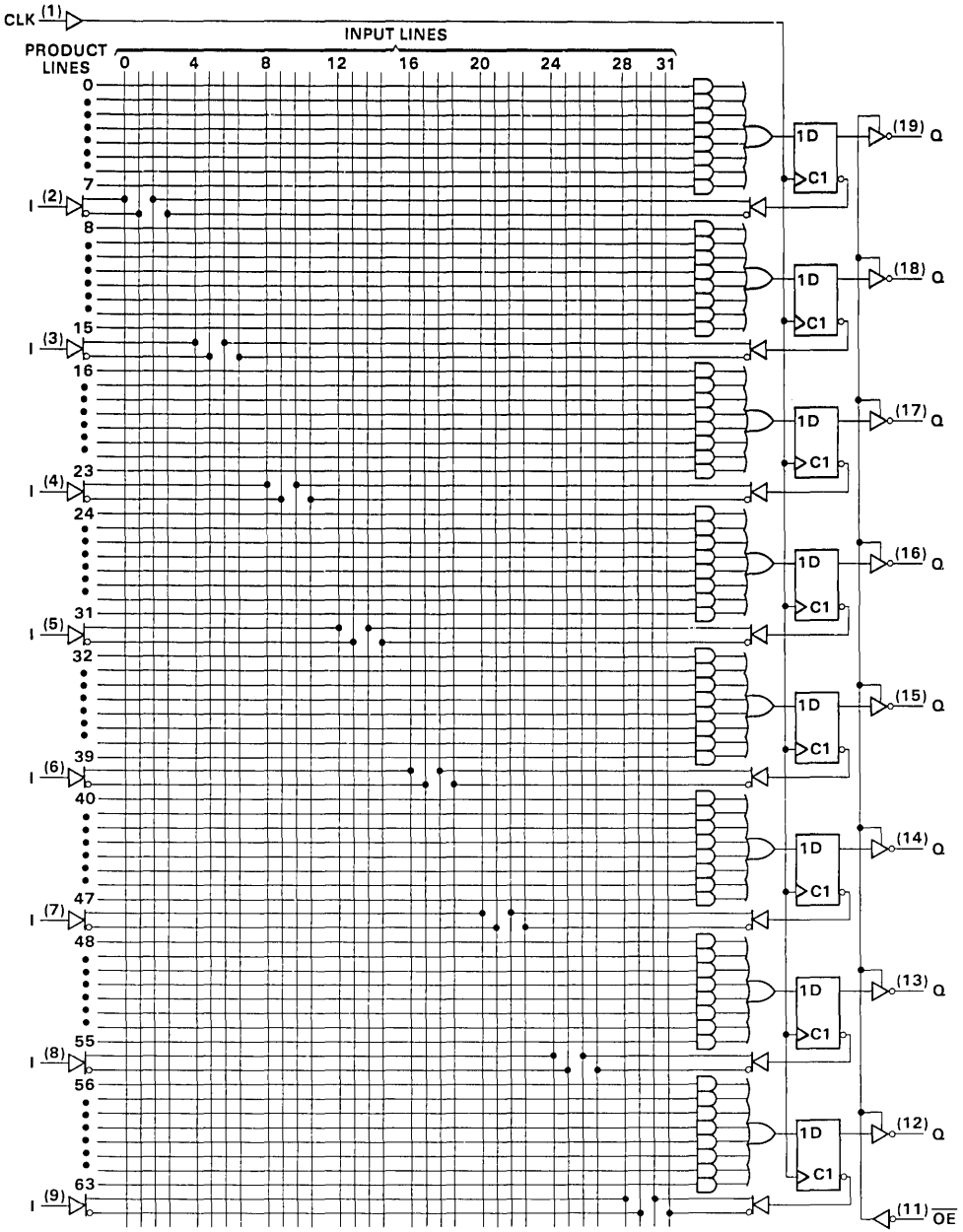
LOGIC DIAGRAM



LOGIC DIAGRAM



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TYPES SN54PL20L8, SN54PL20R4, SN54PL20R6, SN54PL20R8
SN74PL20L8, SN74PL20R4, SN74PL20R6, SN74PL20R8
FIXED-OR ARRAYS

D2706, DECEMBER 1982

- Standard 24-Pin, 300-mil Packages
- Output Registers Have Preload Capability
- Output Registers Automatically Clear During Power-Up
- Choice of Operating Speeds
  - -1 Parts . . . 30 MHz Max
  - -2 Parts . . . 20 MHz Max

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PL20L8	14	2	0	6
'PL20R4	12	0	4 (3-state buffers)	4
'PL20R6	12	0	6 (3-state buffers)	2
'PL20R8	12	0	8 (3-state buffers)	0

3

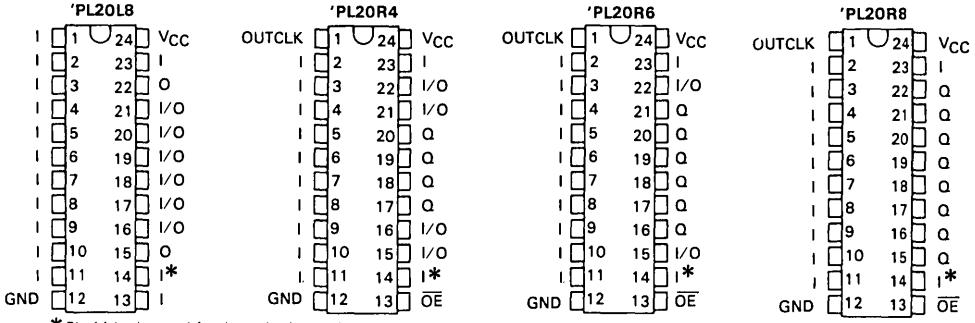
description

These fixed-OR arrays provide 3-state outputs for bus-oriented systems. The 'PL20L8, 'PL20R4, and 'PL20R6 have output registers that can be loaded from the I/O pins by a preload procedure. All the outputs are automatically set to a low level when power is applied. The -1 and -2 parts offer a choice of operating frequency and switching times.

The SN54PL20' is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74PL20' is characterized for operation from 0°C to 70°C.

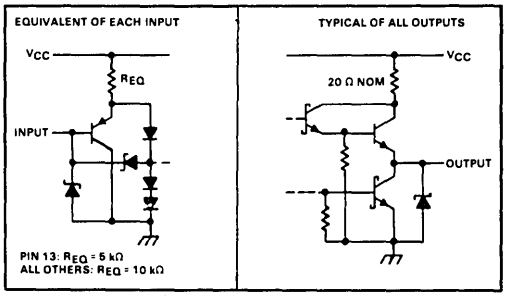
pin assignments in operating mode (voltages at pins 1 and 13 less than V_{IHH})

SN54' ... JT PACKAGE
SN74' ... NT PACKAGE
(TOP VIEW)



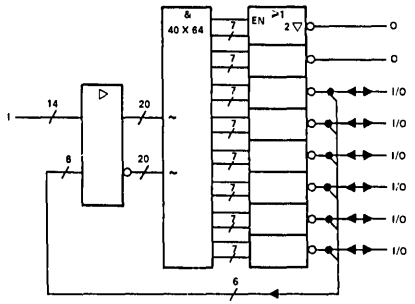
* Pin 14 is also used for the preload procedure on page 3-16.

schematics of inputs and outputs

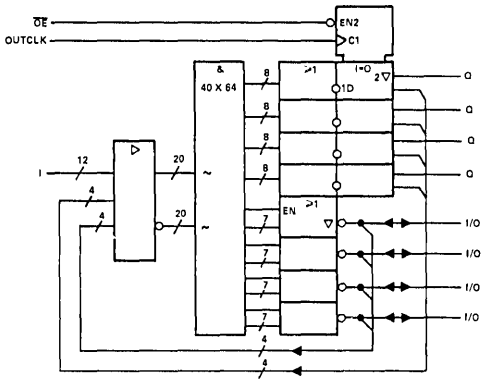


functional block diagrams (positive logic)

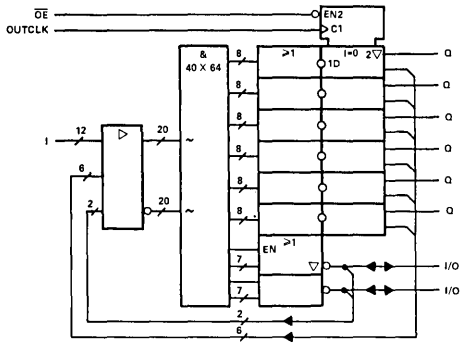
'PL20L8



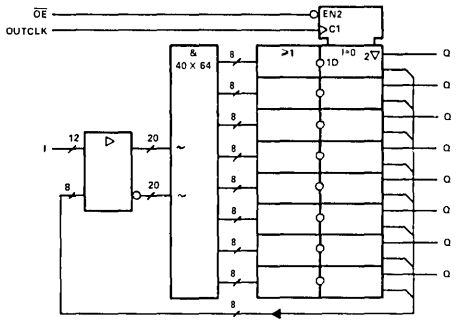
'PL20R4



'PL20R6



'PL20R8



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage (see Note 1) ..... 5.5 V
Voltage applied to a disabled output (see Note 1) ..... 5.5 V
Operating free-air temperature range: SN54PL' ..... −55°C to 125°C
SN74PL' ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during preload cycle.

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recommended operating conditions

		SN54PL19R'			SN74PL19R'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		5.5	2		5.5	V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS†		SN54PL20'			SN74PL20'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN,	I_{OH} = MAX	2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN,	I_{OL} = MAX		0.25	0.4		0.35	0.5	V
I_{OZH}	O, Q outputs	V_{CC} = MAX,	V_{IH} = 2.7 V			20			20	μA
	I/O ports					100			100	
I_{OZL}	O, Q outputs	V_{CC} = MAX,	V_{IH} = 0.4 V			−20			−20	μA
	I/O ports					−250			−250	
I_I	$\overline{OE}$ Input	V_{CC} = MAX,	V_I = 5.5 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	$\overline{OE}$ Input	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	$\overline{OE}$ Input	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
	All others					−0.2			−0.2	
I_O		V_{CC} = MAX,	V_O = 2.25 V	−15	−33	−65	−15	−33	−65	mA
I_{CC}		V_{CC} = MAX, Outputs open	V_I = 0 V, $\overline{OE}$ at V_{IH}		150	200		150	200	mA

†Conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

'PL20R4, 'PL20R6, 'PL20R8 timing requirements

		-1 PARTS		-2 PARTS		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	30	0	20	MHz
t_w	Pulse duration, clock high or low	12		12		ns
t_{su}	Setup time, input or feedback before OUTCLK↑	15	15			ns
t_h	Hold, input or feedback before OUTCLK↑	0		0		ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	-1 PARTS			-2 PARTS			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}			R_L = 500 Ω, C_L = 50 pF	30			20			MHz
t_{pd}	I, I/O	O, I/O			16			25		ns
t_{pd}	OUTCLK↑	O, I/O			12			20		ns
t_{en}	$\overline{OE}$↓	Q			8			15		ns
t_{dis}	$\overline{OE}$↑	Q			6			12		ns
t_{en}	I, I/O	O, I/O			18			25		ns
t_{dis}	I, I/O	O, I/O			13			20		ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

PRELOAD PROCEDURES

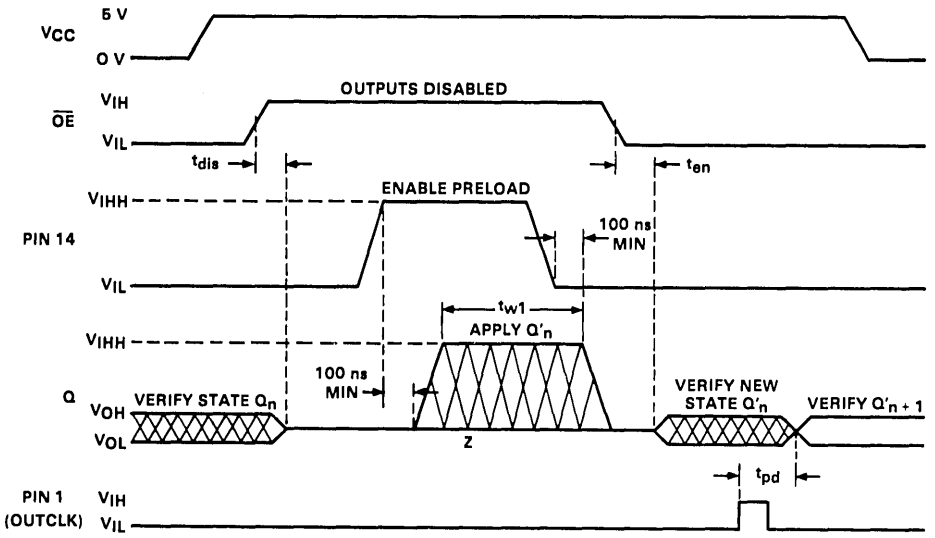

FIGURE 1—PRELOAD WAVEFORMS

preload procedure for registered outputs

Step 1	Pin 13 to V_{IH}, Pin 1 to V_{IL}, and V_{CC} to 5 volts.
Step 2	Pin 14 to V_{IHH} for 10 to 50 microseconds.
Step 3	Apply an open circuit for a low and V_{IHH} for a high at the Q outputs.
Step 4	Pin 14 to V_{IL}.
Step 5	Remove the voltages applied to the outputs.
Step 6	Pin 13 to V_{IL}.
Step 7	Check the output states to verify preload.

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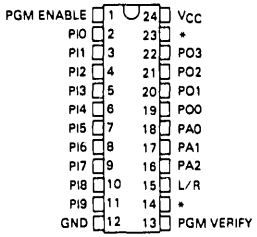
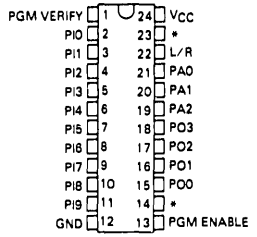
pin assignments in programming mode (PGM ENABLE at V_{IHH})

PRODUCT TERMS 0 THRU 31
(TOP VIEW)



PRODUCT TERMS 32 THRU 63
(TOP VIEW)



*Pin 14 has no programming function. Make no connection.

TABLE 1—INPUT LINE SELECT

INPUT LINE NUMBER	PIN NAME										
	PI9	PI8	PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0	L/R
0	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	HH
28	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	Z
29	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	Z
30	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	HH
31	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	HH
32	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	Z
33	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	Z
34	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	HH
35	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	HH
36	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
37	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
38	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH
39	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH

L = V_{IL}, H = V_{IH}, HH = V_{IHH}, Z = high impedance (e.g., 10 kΩ to 5 V)

TABLE 2—PRODUCT LINE SELECT

PRODUCT LINE NUMBER	PIN NAME						
	PO0	PO1	PO2	PO3	PA2	PA1	PA0
0, 32	Z	Z	Z	HH	Z	Z	Z
1, 33	Z	Z	Z	HH	Z	Z	HH
2, 34	Z	Z	Z	HH	Z	HH	Z
3, 35	Z	Z	Z	HH	Z	HH	HH
4, 36	Z	Z	Z	HH	HH	Z	Z
5, 37	Z	Z	Z	HH	HH	Z	HH
6, 38	Z	Z	Z	HH	HH	HH	Z
7, 39	Z	Z	Z	HH	HH	HH	HH
8, 40	Z	Z	HH	Z	Z	Z	Z
9, 41	Z	Z	HH	Z	Z	Z	HH
10, 42	Z	Z	HH	Z	Z	HH	Z
11, 43	Z	Z	HH	Z	Z	HH	HH
12, 44	Z	Z	HH	Z	HH	Z	Z
13, 45	Z	Z	HH	Z	HH	Z	HH
14, 46	Z	Z	HH	Z	HH	HH	Z
15, 47	Z	Z	HH	Z	HH	HH	HH
16, 48	Z	HH	Z	Z	Z	Z	Z
17, 49	Z	HH	Z	Z	Z	Z	HH
18, 50	Z	HH	Z	Z	Z	HH	Z
19, 51	Z	HH	Z	Z	Z	HH	HH
20, 52	Z	HH	Z	Z	HH	Z	Z
21, 53	Z	HH	Z	Z	HH	Z	HH
22, 54	Z	HH	Z	Z	HH	HH	Z
23, 55	Z	HH	Z	Z	HH	HH	HH
24, 56	HH	Z	Z	Z	Z	Z	Z
25, 57	HH	Z	Z	Z	Z	Z	HH
26, 58	HH	Z	Z	Z	Z	HH	Z
27, 59	HH	Z	Z	Z	Z	HH	HH
28, 60	HH	Z	Z	Z	HH	Z	Z
29, 61	HH	Z	Z	Z	HH	Z	HH
30, 62	HH	Z	Z	Z	HH	HH	Z
31, 63	HH	Z	Z	Z	HH	HH	HH

programming parameters

			MIN	NOM	MAX	UNIT
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{OH}	High-level output voltage				5.5	V
V_{IHH}	Program-pulse input voltage		10.25	10.5	10.75	V
I_{IHH}	Program-pulse input current	PO			50	mA
		PGM VERIFY, L/R			25	
		PGM ENABLE, PI, PA			5	
I_{CCHH}	Program-pulse supply current at V_{IHH}				400	mA
t_{w1}	Program-pulse duration at PO pins		10		50	μs
t_{w2}	Pulse duration at PGM VERIFY		100			ns
t_{su}	Setup time		100			ns
t_h	Hold time		100			ns
t_{d1}	Delay time from V_{CC} to 6 V to PGM VERIFY↑		100			μs
t_{d2}	Delay time from PGM VERIFY↑ to verification of output		200			ns
	Input voltage at pins 1 and 13 to open verify-protect (security) fuse		20	21	22	V
	Input current to open verify-protect (security) fuse				400	mA
	Pulse duration to open verify-protect (security) fuse		20		50	ms

PROGRAMMING PROCEDURES

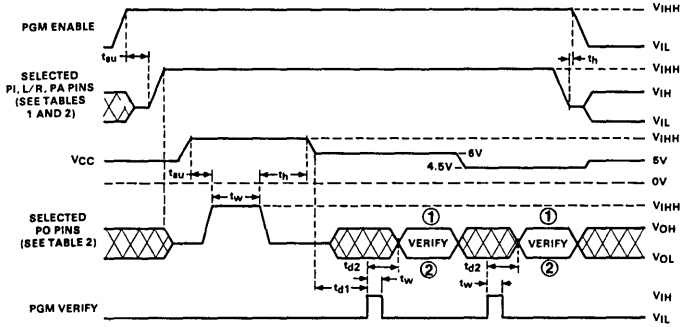


FIGURE 2—ARRAY PROGRAMMING WAVEFORMS

① A high level during the verify interval indicates that programming has not been successful.
② A low level during the verify interval indicates that programming has been successful.

programming procedure for array fuses

Array fuses are programmed using a linear select method. Each fuse can be opened by selecting the appropriate (one of 40) input line and then pulsing the correct (one of 64) product line. The levels for selecting input lines and product lines are shown in Tables 1 and 2.

Step 1 — Raise PGM ENABLE to V_{IHH}.
Step 2 — Select an input line by applying appropriate levels to L/R and PI pins.
Step 3 — Begin selection of the output line with appropriate conditions on PA pins.
Step 4 — Raise V_{CC} to V_{IHH}.
Step 5 — Blow the fuse by pulsing the appropriate PO pin to V_{IHH} as shown in Table 2 for the product line.
Step 6 — Lower V_{CC} to 6 volts and pulse PGM VERIFY. The PO pin selected in Step 4 will be less than V_{OL} if the fuse is open.
Step 7 — Lower V_{CC} to 4.5 volts and pulse PGM VERIFY. The PO pin selected in Step 4 will be less than V_{OL} if the fuse is open.

Steps 1 thru 7 may be repeated if the verification does not indicate that the fuse was successfully programmed (blown), but no more than 4 times. Verification is possible only with the verify-protect fuse intact.

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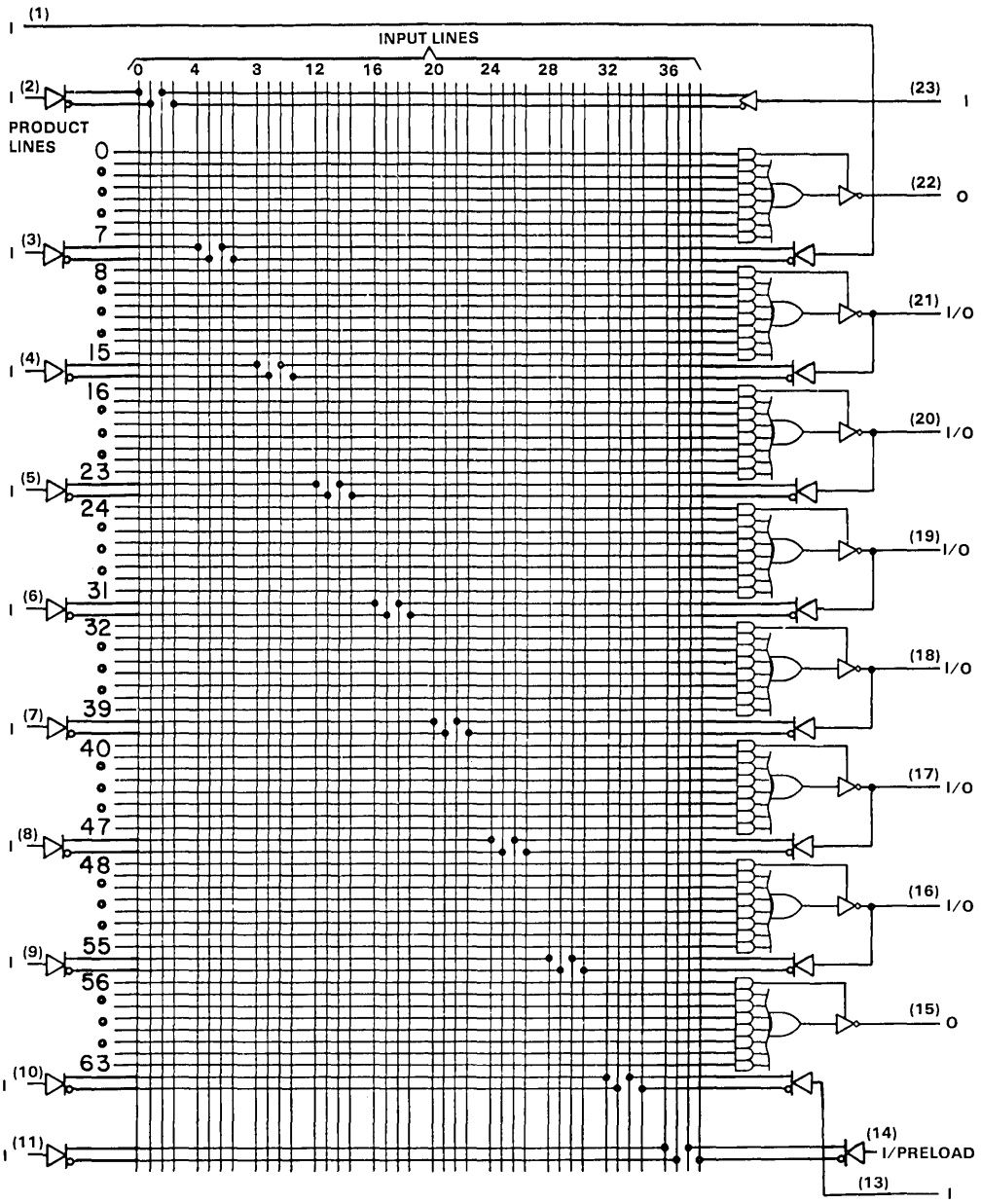
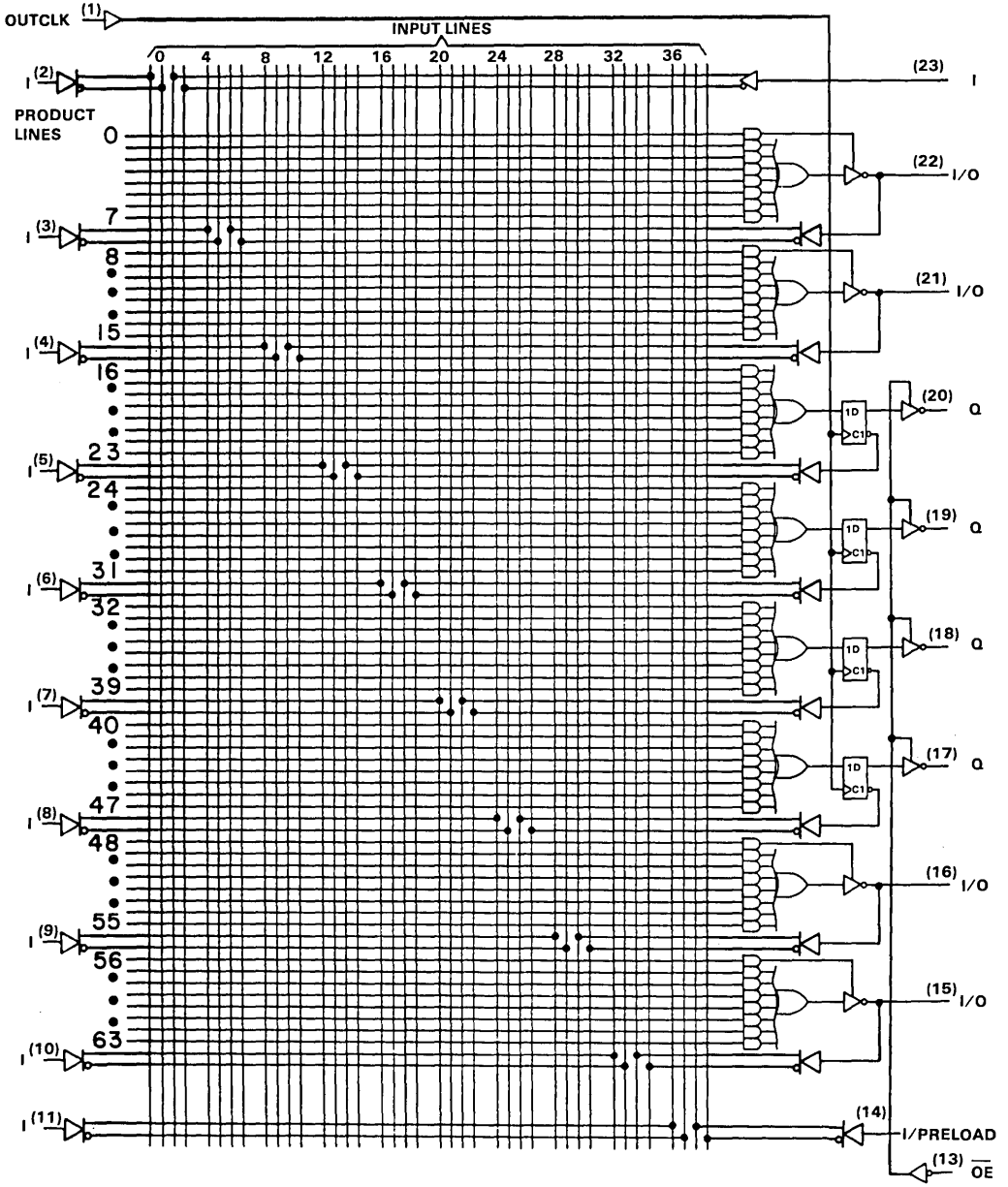

(1)
INPUT LINES
0 4 3 12 16 20 24 28 32 36
(2)
PRODUCT LINES
0
7
(3)
8
15
(4)
16
23
(5)
24
31
(6)
32
39
(7)
40
47
(8)
48
55
(9)
56
63
(10)
(11)
(23) I
(22) O
(21) I/O
(20) I/O
(19) I/O
(18) I/O
(17) I/O
(16) I/O
(15) O
(14) I/PRELOAD
(13) I



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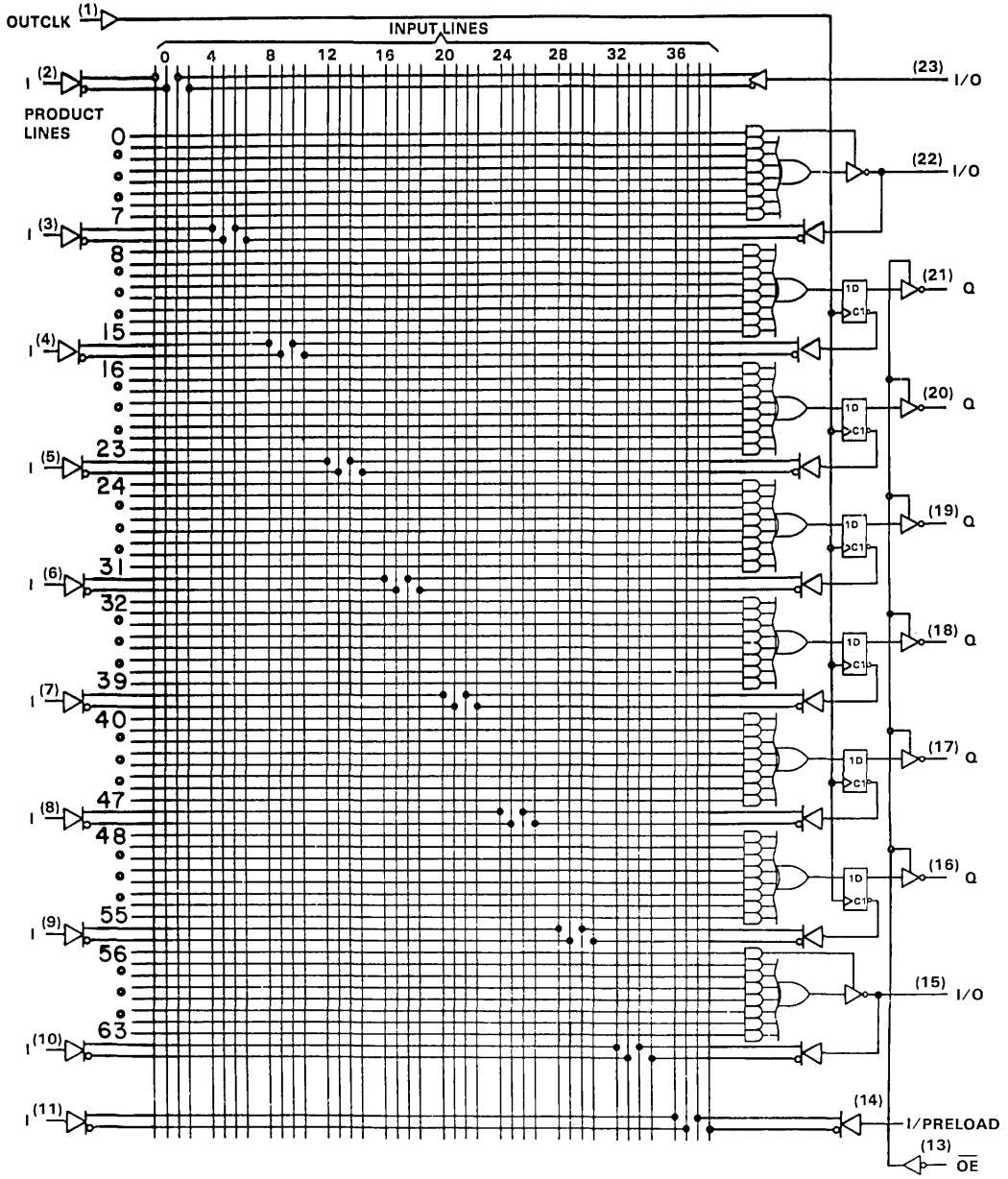
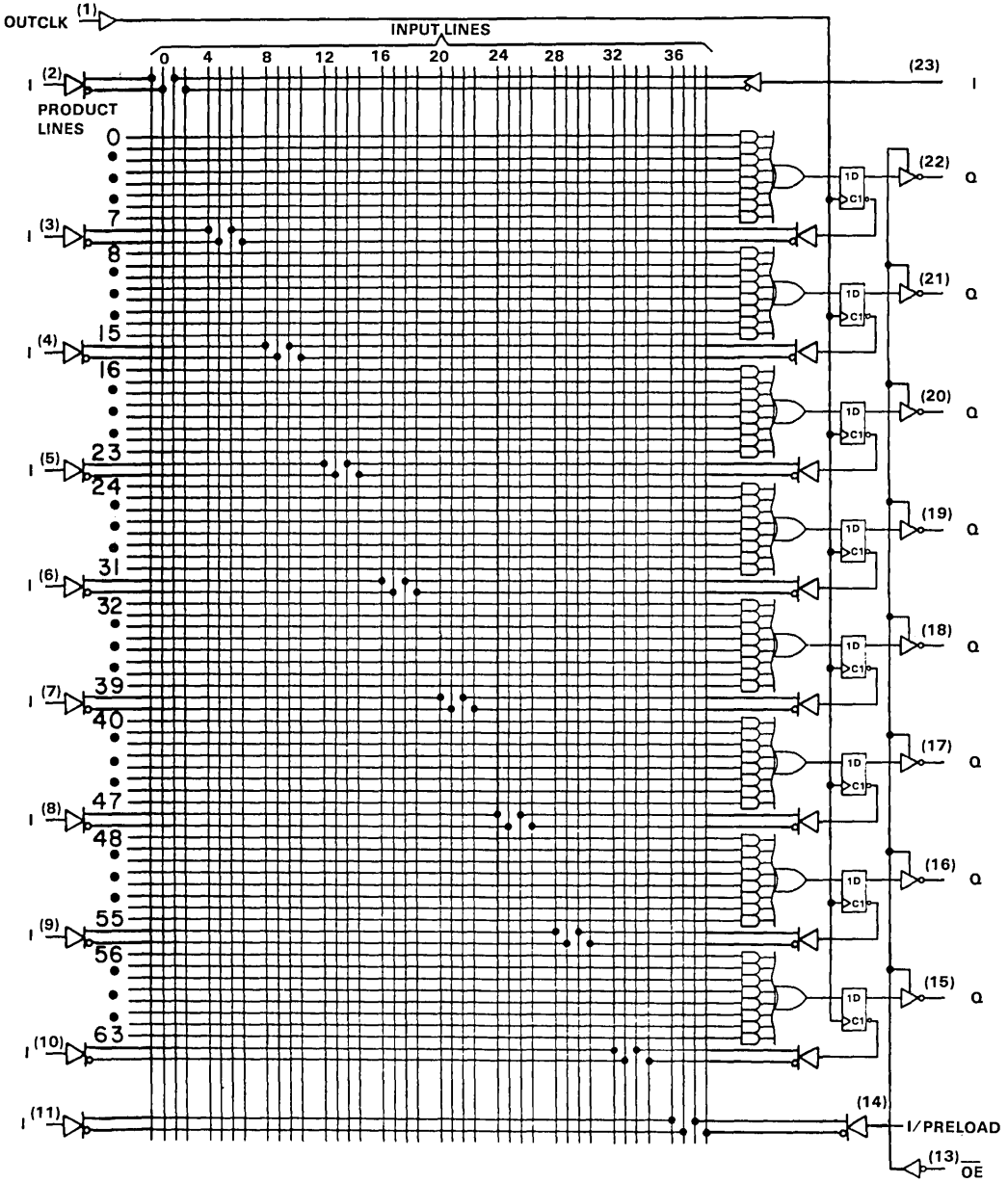

OUTCLK (1)
INPUT LINES
0 4 8 12 16 20 24 28 32 36
I (2)
PRODUCT LINES
0
7
I (3)
8
15
I (4)
16
23
I (5)
24
31
I (6)
32
39
I (7)
40
47
I (8)
48
55
I (9)
56
63
I (10)
I (11)
(23) I/O
(22) I/O
(21) Q
(20) Q
(19) Q
(18) Q
(17) Q
(16) Q
(15) I/O
(14) I/PRELOAD
(13) OE
1D
C1



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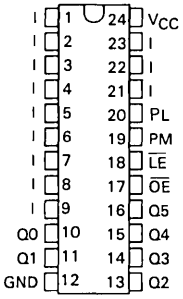
TYPES SN54PL333, SN54PL335, SN74PL333, SN74PL335 FIELD-PROGRAMMABLE LOGIC SEQUENCERS

D2707, DECEMBER 1982

- 24-Pin, 600-mil Packages
- Propagation Delay . . . 60 ns Typ
- 12 Inputs
- 32 Product-Term Outputs
- 6-Bit Output Latch
- 4-Bit State Register
- Low Power Dissipation . . . 450 mW Typ

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



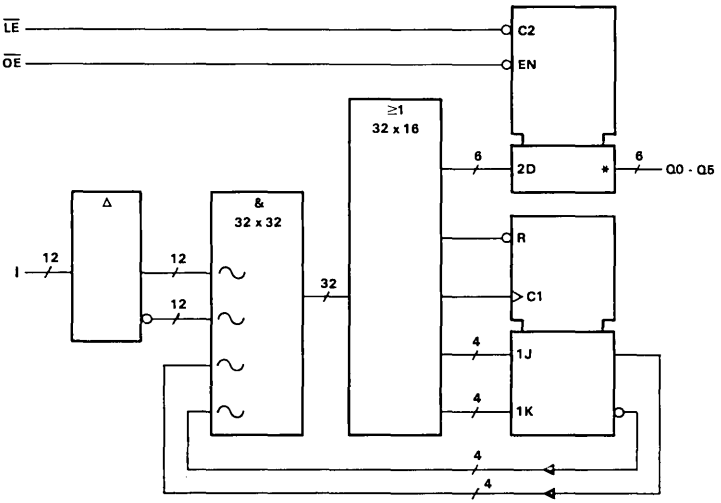
description

The 'PL333 (three-state outputs) and the 'PL335 (open-collector outputs) are low-power Schottky Bipolar TTL field-programmable logic sequencers designed to solve state-machine problems of the mealy type. They each contain four completely buried J-K flip-flops in the feedback path between the OR and AND matrices. The common clock and clear lines are also programmable by separate OR terms in addition to the four J inputs and K inputs.

The output-function levels are stored by a common asynchronous latch enable pin (LE) that controls the 6-bit output transparent latches. The program mode (PM) pin and the program latch (PL) pin are unique programming control inputs that simplify the programming procedure. These pins should be grounded during normal device operation.

The SN54PL333 and SN54PL335 are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74PL333 and SN74PL335 are characterized for operation from 0°C to 70°C.

functional block diagram (positive logic)



~ Denotes fused inputs.

*'PL333 has 3-state output, 'PL335 has open-collector outputs.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage ..... 5.5 V
Off-state output voltage ..... 5.5 V
Operating free-air temperature range: SN54PL' ..... −55°C to 125°C
SN74PL' ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

Note 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54PL'			SN74PL'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended free-air operating temperature range (unless otherwise stated)

PARAMETER		TEST CONDITIONS†	SN54PL'			SN74PL'			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	2.4	3.1		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX		0.25	0.4		0.35	0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current: PL, PM	V_{CC} = MAX, V_I = 0.4 V			−0.4			−0.4	mA
	Low-level input current: All others				−0.2			−0.2	
I_O	Output current	V_{CC} = MAX, V_O = 2.25 V	−15		−65	−15		−65	mA
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, $\overline{OE}$ at 2 V, V_O = 2.7 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, $\overline{OE}$ at 2 V, V_O = 0.4 V			−20			−20	μA
I_{CC}	Supply current	V_{CC} = MAX, $\overline{OE}$ at V_{IH}, All other inputs at V_{IL}		90	145		90	135	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

'PL333, 'PL335, timing requirements

		SN54PL'		SN74PL'		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	10	0	15	MHz
t_{w1}	Pulse duration, clock high or low	55		45		ns
t_{w2}	Pulse duration, internal clear	56		46		ns
t_{su1}	Setup time, input to clock	12		12		ns
t_{su2}	Setup time, input to $\overline{LE}$	55		48		ns
t_{h1}	Hold time, clock to input	9		9		ns
t_{h2}	Hold time, LE to input	0		0		ns

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switching characteristics over recommended operating free-air temperature range and supply voltages (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYPE	SN54PL'			SN74PL'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}		R_L = 667Ω, C_L = 45 pF	All	10	23		15	23		MHz
t_{pd}	Input to output		'PL333		52	78		52	69	ns
			'PL335		60	98		60	80	
t_{pd}	Clock to output		'PL333		100	150		100	130	ns
			'PL335		100	160		100	140	
t_{pd}	Clear to output		'PL333		90	135		90	115	ns
			'PL335		90	145		90	125	
t_{pd}	$\overline{LE}$ to output		'PL333		22	36		22	32	ns
			'PL335		35	69		35	58	
t_{en}	$\overline{OE}$ to output		All		20	30		20	28	ns
t_{dis}	$\overline{OE}$ to output		All		17	26		17	24	ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

programming parameters

	PARAMETER	MIN	NOM	MAX	UNIT
V_{IHH}	Program-level input voltage	10	10.5	11	V
I_{CCH}	Program-level supply current		300	400	mA
t_p	Width of program pulse	100		1000	us
	Program pulse duty cycle		25	35	%

PROGRAMMING PROCEDURES

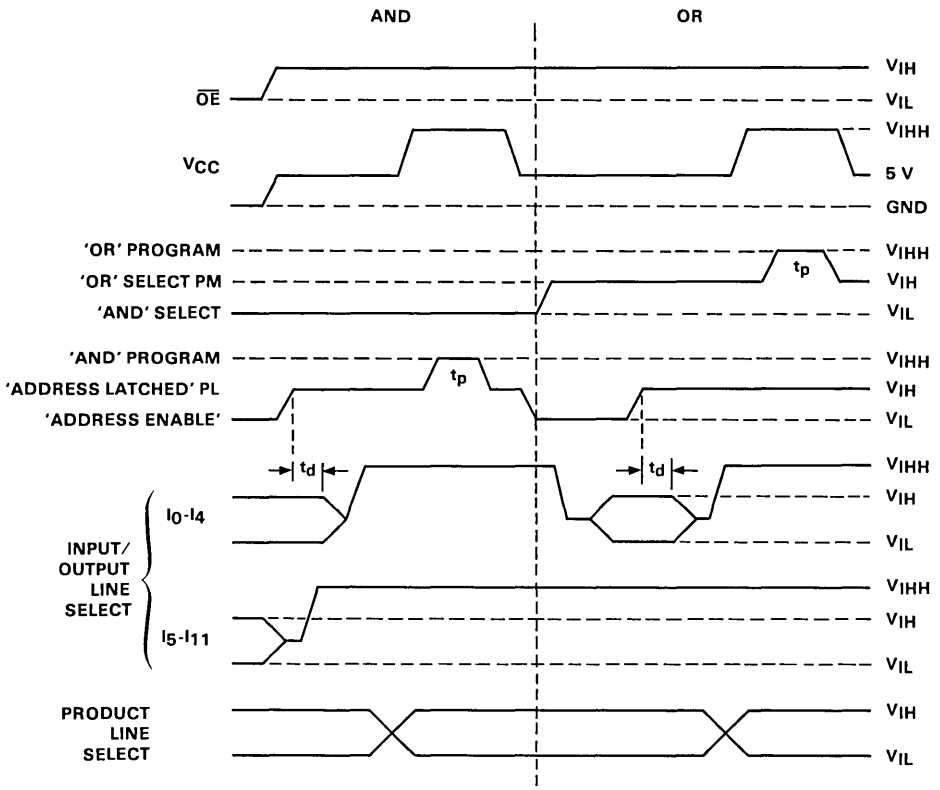
AND-matrix, input variables 0 thru 11 programming

Step 1 — Set V_{CC} and $\overline{OE}$ to 5V and PM, PL, and GND to 0 V.
Step 2 — Latch out F/F outputs by applying V_{IH} to I0 thru I4 and raising PL to 5 V.
Step 3 — Apply the true logic level to the input to be programmed and raise all remaining inputs to V_{IHH}.
Step 4 — Address the product term to be programmed (0 to 31). Address product term by applying its binary code to outputs Q5 to Q0 as LSB, 1 = V_{IH}, 0 = V_{IL}.
Step 5 — Ramp V_{CC} to V_{IHH} and then pulse PL to V_{IHH}. Return V_{CC} to 5 V.
Step 6 — Disable the programmed input with V_{IHH}.
Step 7 — Repeat steps 3 through 6 for all other input variables and product terms.

AND-matrix, feedback input lines programming

Step 1 — Set V_{CC} and $\overline{OE}$ to 5 V, and PM, PL, and GND to 0 V.
Step 2 — Select the F/F output to be programmed high by applying logic levels (1 = V_{IH}, 0 = V_{IL}) to inputs I0 through I4 using addresses in Table 1. Apply V_{IHH} to other inputs I5 through I11.
Step 3 — Raise PL to 5 V.
Step 4 — Disable inputs I0 to I4 with V_{IHH}.
Step 5 — Address the product term.
Step 6 — Ramp V_{CC} to V_{IHH} and then pulse PL to V_{IHH}. Return V_{CC} to 5 V.
Step 7 — Repeat steps 5 and 6 for each of the product terms.
Step 8 — Return PL to 0 V.
Step 9 — Repeat steps 2 through 8 for all other feedback F/F AND-outputs and product terms.

PROGRAMMING WAVEFORMS



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PROGRAMMING PROCEDURE

OR-matrix programming

Step 1 Set V_{CC}, PM, and OE to 5 V, and PL and GND to 0 V.

Step 2 Select the output function OR-F/F input line by applying logic levels (1 = V_{IH}, 0 = V_{IL}), to inputs I0 to I4 using the address in Table 2. Apply V_{IHH} to I5 through I11.

Step 3 Ramp PL to 5 V.

Step 4 Disable inputs I0 through I4 with V_{IHH}.

Step 5 Address the product term then raise V_{CC} to V_{IHH}. Pulse PM to V_{IHH} and return V_{CC} to 5 V.

Step 6 Repeat step 5 for each of the product terms to be low in the addressed output function OR-F/F input line.

Step 7 Return PL to 0 V.

Step 8 Repeat steps 2 through 7 for each output function and F/F input line.

3

TABLE 1—AND-MATRIX INPUT LINE SELECT

INPUT LINE NUMBER	PIN NAME											
	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
0	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH	L
1	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH	H
2	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	HH
5	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	HH
6	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	HH
7	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	HH
8	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	HH
9	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	HH
10	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	HH
11	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	HH
12	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	HH
13	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	HH
14	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	HH
15	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	HH
16	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	HH
17	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	HH
18	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	HH
19	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	HH
20	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH
21	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH
22	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH
23	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH
24	HH	HH	HH	HH	HH	HH	HH	L	L	L	L	H
25	HH	HH	HH	HH	HH	HH	HH	L	L	L	L	L
26	HH	HH	HH	HH	HH	HH	HH	L	L	L	H	H
27	HH	HH	HH	HH	HH	HH	HH	L	L	L	H	L
28	HH	HH	HH	HH	HH	HH	HH	L	L	H	L	H
29	HH	HH	HH	HH	HH	HH	HH	L	L	H	L	L
30	HH	HH	HH	HH	HH	HH	HH	L	L	H	H	H
31	HH	HH	HH	HH	HH	HH	HH	L	L	H	H	L

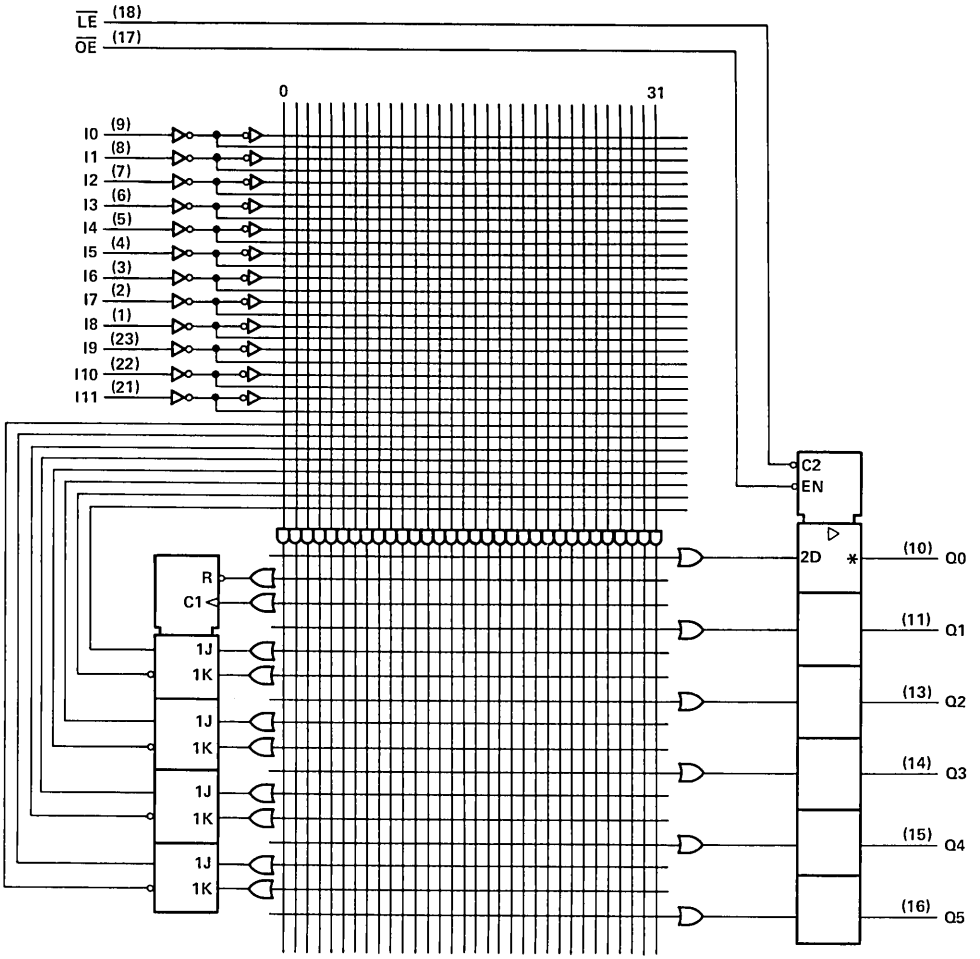
L = V_{IL}, H = V_{IH}, HH = V_{IHH}

TABLE 2—OR-MATRIX SUM TERM SELECT

PRODUCT TERM	PIN NAME											
	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
CLK	HH	HH	HH	HH	HH	HH	HH	L	L	L	L	L
CLR	HH	HH	HH	HH	HH	HH	HH	L	L	L	L	H
J4	HH	HH	HH	HH	HH	HH	HH	L	L	L	H	L
K4	HH	HH	HH	HH	HH	HH	HH	L	L	L	H	H
J3	HH	HH	HH	HH	HH	HH	HH	L	L	H	L	L
K3	HH	HH	HH	HH	HH	HH	HH	L	L	H	L	H
J2	HH	HH	HH	HH	HH	HH	HH	L	L	H	H	L
K2	HH	HH	HH	HH	HH	HH	HH	L	L	H	H	H
J1	HH	HH	HH	HH	HH	HH	HH	L	H	L	L	L
K1	HH	HH	HH	HH	HH	HH	HH	L	H	L	L	H
Q0	HH	HH	HH	HH	HH	HH	HH	L	H	L	H	L
Q1	HH	HH	HH	HH	HH	HH	HH	L	H	L	H	H
Q2	HH	HH	HH	HH	HH	HH	HH	L	H	H	L	L
Q3	HH	HH	HH	HH	HH	HH	HH	L	H	H	L	H
Q4	HH	HH	HH	HH	HH	HH	HH	L	H	H	H	L
Q5	HH	HH	HH	HH	HH	HH	HH	L	H	H	H	H
NONE	HH	HH	HH	HH	HH	HH	HH	H	H	H	H	H

2

LOGIC DIAGRAM



*'PL333 has 3-state outputs, 'PL335 has open-collector outputs.

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TYPES SN54PL839, SN54PL840, SN74PL839, SN74PL840
14 X 32 X 6 FIELD-PROGRAMMABLE LOGIC ARRAYS

- Input to Output Propagation Delay . . . 10 ns Typical
- 24-Pin, 300-mil Slim Line Packages
- Power Dissipation . . . 640 mW Typical
- Programmable Output Polarity

LOGIC FUNCTION

f(I) = P0 + P1 . . . P31 for polarity link intact

f(I) = $\overline{P0}$* $\overline{P1}$* . . . *$\overline{P31}$ for polarity link, open where P0 through P31 are product terms.

description

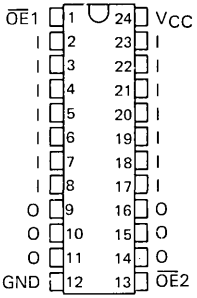
The 'PL839 (3-state outputs) and the 'PL840 (open-collector outputs) are TTL field-programmable logic arrays, containing 32 product terms (AND terms), and 6 sum terms (OR terms). Each of the 6 sum-of-products output functions can be programmed either high true or low true. The true condition of each output function is activated by the programmed logical minterms of 14 input variables. The outputs are controlled by two chip-enable pins to allow output inhibit and expansion of terms.

These devices provide high-speed data-path logic replacement where several conventional SSI functions can be designed into a single package.

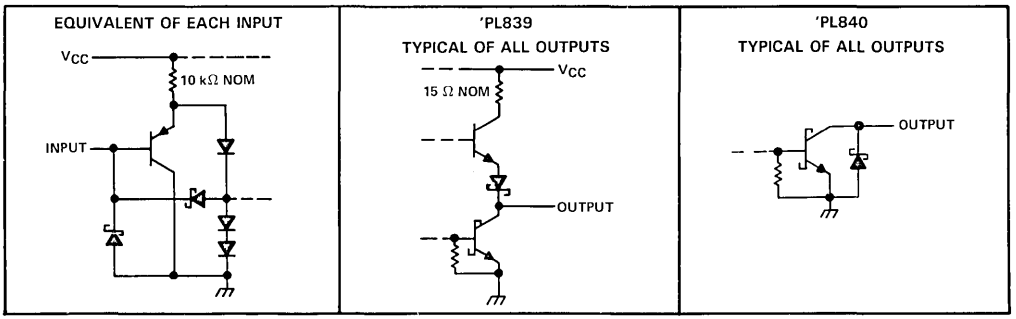
The SN54PL839 and SN54PL840 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74PL839 and SN74PL840 are characterized for operation from 0°C to 70°C.

pin assignments in operating mode (pin 1 is less than V_{IHH})

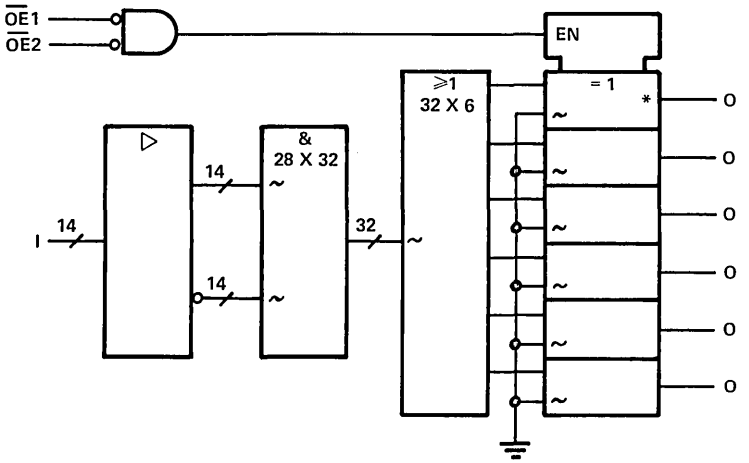
SN54PL' . . . JT PACKAGE
SN74PL' . . . NT PACKAGE
(TOP VIEW)



schematics of inputs and outputs



functional block diagram (positive logic)



~ denotes fused inputs.
*'PL839 has 3-state (▽) outputs; 'PL840 has open-collector (◇) outputs.

absolute maximum ratings

Supply Voltage, V_{CC}		7 V
Input Voltage		5.5 V
Off-State Output Voltage		5.5 V
Operating Free-air Temperature Range	SN54PL'	−55°C to 125°C
	SN74PL'	0°C to 70°C
Storage Temperature		−65°C to 150°C

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recommended operating conditions

	SN54PL'			SN74PL'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			−1			−2.6	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54PL'			SN74PL'			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.2		2.4	3		V
V_{OL}	V_{CC} = MIN,	I_{OL} = MAX		0.25	0.5		0.37	0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_O	V_{CC} = MAX,	V_O = 2.25 V	−30	−50	−112	−30	−50	−112	mA
I_{OZH}	V_{CC} = MAX,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.4 V			−20			−20	μA
I_{CC}	V_{CC} = MAX, $\overline{OE}$ inputs = V_{IH}	V_I = 0 V,		130	200		130	190	mA

†For conditions shown as MIN or MAX, use the appropriate condition specified under recommended operating conditions.

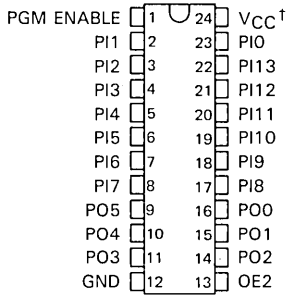
switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	SN54PL'			SN74PL'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	Input	Output	R_L = 500 to GND, C_L = 50 pF to GND		10	25		10	20	ns
t_{en}	Pin 1 or Pin 13	Output	R_{L1} = 500 to 7 V, R_{L2} = 500 to GND, C_L = 50 pF to GND		9	16		9	13	ns
t_{dis}					8	15		8	12	

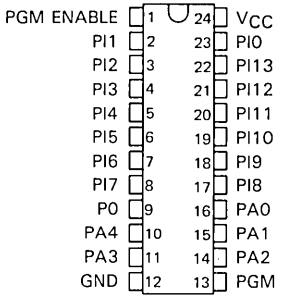
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

pin assignment in programming mode (pin 1 ≥ V_{IHH}) top views

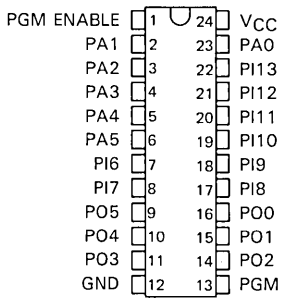
OUTPUT POLARITY
(PGM ENABLE = V_{ILL})



AND MATRIX
(V_{CC3})



OR MATRIX
(V_{CC1}, PA5 = V_{IL})



†V_{CC} = V_{CC2} for program and V_{CC1} for verify

programming parameters, T_A = 25°C

PARAMETER		MEASURED AT	PROGRAMMING MODE	MIN	TYP	MAX	UNIT
V_{IHH}	Program high-level input voltage	PGM ENABLE	AND, OR	16.5	17	17.5	V
		PO pins	Polarity				
V_{ILL}	Program low-level input voltage	PGM ENABLE	Any	0		0.4	V
I_{IHH}	Program-level input current	PO pins	Polarity		100		mA
		PGM ENABLE	AND, OR		150		
V_{IX}	Program-level input voltage	PO0 thru PO5	Polarity	9.5	10	10.5	V
		PGM	AND, OR				
I_{IX}	Program-level input current	PI pins	AND		0.6	2	mA
		$\overline{OE}$2	Polarity			5	
		PO0 thru PO5	OR		5	10	
V_{CC1}	Programming supply voltage	V_{CC}	OR	8.5	8.75	9	V
I_{CC1}	Programming supply current	V_{CC}	OR		250	400	mA
V_{CC2}	Programming supply voltage	V_{CC}	Polarity		0	0.4	V
V_{CC3}	Programming supply voltage	V_{CC}	AND	4.75	5	5.25	V
V_{IH}	High-level input voltage	Any	Any	2			
V_{IL}	Low-level input voltage	Any	Any	0		0.8	V
V_{OH}	High-level output voltage	Any	Any	2.4	3.2		V
V_{OL}	Low-level output voltage	Any	Any		0.25	0.5	V
t_w	Program pulse duration	PO0 thru PO5	Polarity		50	1000	μs
		PGM	AND, OR				
	Program pulse duty cycle	PO0 thru PO5	Polarity		10	50	%
		PGM	AND, OR				
t_d	Delay time	Any	Any	10			μs
t_r	Rise time	Any	Any		25		μs

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PROGRAMMING PROCEDURE

OUTPUT POLARITY

Program

Load all output pins with a 10-kΩ resistor to 5 V and set pin 12 (GND) to 0 V. Program the output polarity before programming either the AND matrix or the OR matrix. A virgin device has all 6 outputs set high. When the polarity link of an output is opened, the output function becomes low. Program one output at a time as follows:

Step 1: Set PGM ENABLE (pin 1) to V_{ILL}.
Step 2: Set V_{CC} (pin 24) to V_{CC2}; set $\overline{OE}2$ (pin 13) and PI0 through PI13 to V_{IX}.
Step 3: Pulse the appropriate output to V_{IHH} and remove after t_w.
Step 4: Repeat step 3 for each output to be programmed low.

Verify

Step 1: Set PGM ENABLE (pin 1) to V_{ILL}; set V_{CC} (pin 24) to V_{CC2}; set PI0 through PI13 to V_{IX}.
Step 2: Wait t_d and raise V_{CC} (pin 24) to V_{CC1}.
Step 3: Enable the device by applying V_{IL} to $\overline{OE}2$ (pin 13).
Step 4: Sense the logic state of all 6 outputs. An output at V_{OH} has been programmed low, while an output at V_{OL} has remained high.
Step 5: Remove V_{CC1}.

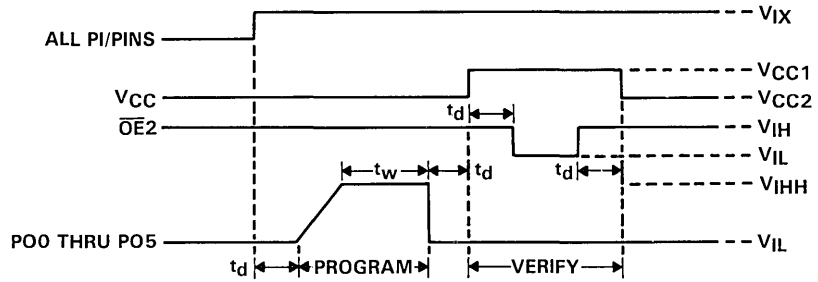

FIGURE 1 — OUTPUT POLARITY PROGRAMMING WAVEFORMS

AND MATRIX

Program

Program the output polarity before programming either the AND matrix or the OR matrix. Load all output pins with a 10-kΩ resistor to 5 V and set pin 12 (GND) to V_{IL}. Program each input separately for each product term, one fuse at a time. Unused terms do not require fusing, however, all input variables of a selected product term must be programmed either true, complement, or don't care (both links are blown), as follows:

Step 1: Set PGM ENABLE (pin 1) to V_{ILL}; set V_{CC} (pin 24) to V_{CC3}.
Step 2: Disable all outputs by applying V_{IH} to PGM (pin 13).
Step 3: Disable all inputs by applying V_{IX} to the I inputs.
Step 4: Address the product term to be programmed (0 through 31) by applying its binary code (V_{IH} for a high and V_{IL} for a low) to outputs PA0 through PA4 with PA0 as the least significant bit.

PROGRAMMING PROCEDURE

Step 5: Lower the voltage on the first input to V_{IH} for a true, or to V_{IL} for the complement.
Step 6: After t_d, raise PGM ENABLE to V_{IHH}.
Step 7: After additional t_d, pulse the PGM input to V_{IX} for t_w.
Step 8: After a t_D delay, lower PGM ENABLE to V_{ILL}.
Step 9: Disable programmed input by raising it back to V_{IX}.
Step 10: Repeat steps 5 through 9 for each input.
Step 11: Repeat steps 4 through 10 for each product term.

Verify

Step 1: Set PGM ENABLE (pin 1) to V_{ILL}; set V_{CC} (pin 24) to V_{CC3}.
Step 2: Enable PO output by setting PGM to V_{IX}.
Step 3: Disable all inputs by applying V_{IX} to the I inputs.
Step 4: Address the product term to be verified (0 through 31) by applying its binary code on outputs PA0 through PA4.
Step 5: Lower the input voltage on the first input to V_{IH} and check the logic level of output PO, then lower the same input to V_{IL} and again check the level of PO. The input variable state contained in the product term is determined from the following table. Two tests are required to verify the programmed state of each variable.

STATE	I	PO
TRUE	L	L
	H	H
COMPLEMENT	L	H
	H	L
DON'T CARE	L	H
	H	H
INACTIVE	L	L
	H	L

Step 6: Disable verified input by raising it back to V_{IX}.
Step 7: Repeat steps 5 and 6 for all other inputs.
Step 8: Repeat steps 4 through 7 for all other product terms.

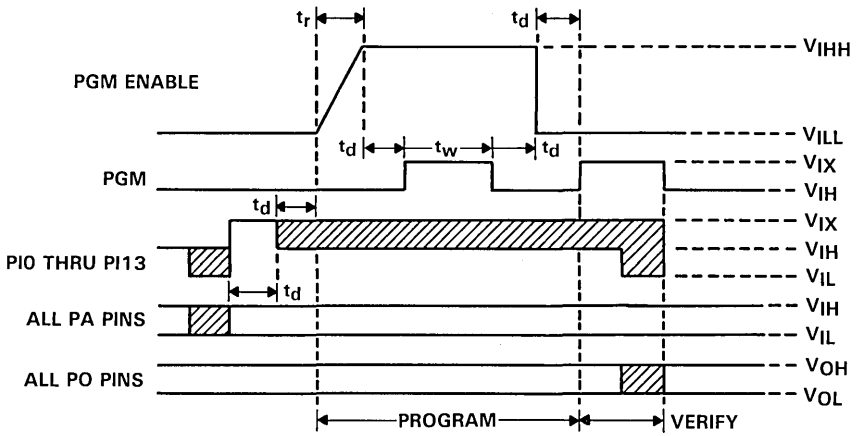

FIGURE 2— AND MATRIX PROGRAMMING WAVEFORMS

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PROGRAMMIMG PROCEDURE

OR MATRIX

Program

Program the output polarity before programming either the AND matrix or the OR matrix. Load all output pins with a 10-kΩ resistor to 5 V and set pin 12 (GND) to 0 V. If the product term is contained in the output function, no fusing is required. Unwanted terms are deleted by programming one at a time, as follows:

Step 1: Set PGM ENABLE (pin 1) to V_{ILL}. Disable the outputs by setting PGM (pin 13) to V_{IH}. Set V_{CC} to V_{CC3}. Set PI6 through PI13 and PA0 through PA5 to V_{IX}.
Step 2: Wait t_d and raise V_{CC} (pin 24) to the program level, V_{CC1}.
Step 3: Use the inputs PA0 through PA5 to address the product term (0 through 31) that is to be removed by applying the corresponding binary code with input PA0 as the least significant bit.
Step 4: Raise the output pin to V_{IX}.
Step 5: Wait t_d, then raise PGM ENABLE to V_{IHH}.
Step 6: Wait t_d, then pulse PGM to V_{IX} for a period of t_p.
Step 7: Wait t_d, then lower PGM ENABLE TO V_{ILL}.
Step 8: Wait t_d, then remove V_{IX} from output pin.
Step 9: Repeat steps 4 through 8 for all three output functions.
Step 10: Repeat steps 3 through 9 for all other product terms.
Step 11: Lower V_{CC} to V_{CC3}.

Verify

Step 1: Set PGM ENABLE (pin 1) to V_{ILL}. Disable the outputs by setting PGM (pin 13) to V_{IH}. Set V_{CC} to V_{CC3}. Set PI6 through PI13 and PA0 through PA5 to V_{IX}.
Step 2: Wait t_d and set V_{CC} (pin 24) to the verify level, V_{CC1}.
Step 3: Address the product term to be verified (0 through 31) by applying its binary code to inputs PA0 through PA5.
Step 4: Wait t_d, and set PGM (pin 13) to V_{IL}.
Step 5: Monitor the state of all 6 outputs (PO0 through PO5) and determine the status of the OR matrix from the following table:

OUTPUT		OR FUSE LINK
ACTIVE HIGH	ACTIVE LOW	
L	H	FUSED
H	L	PRESENT

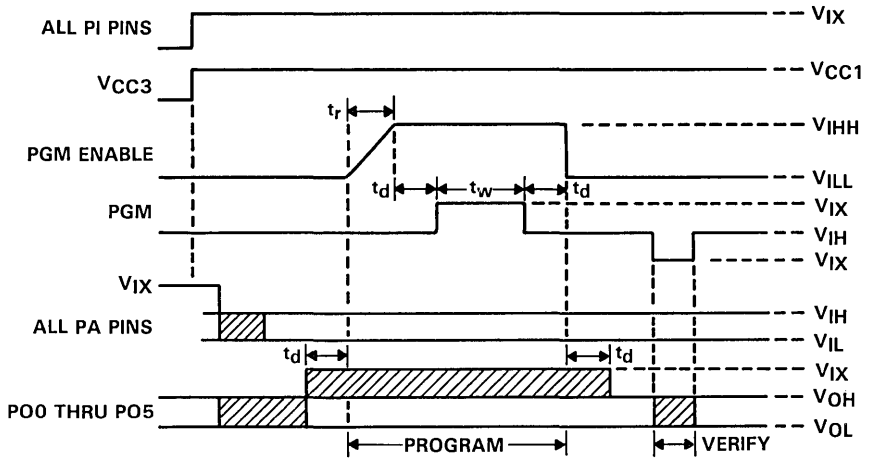
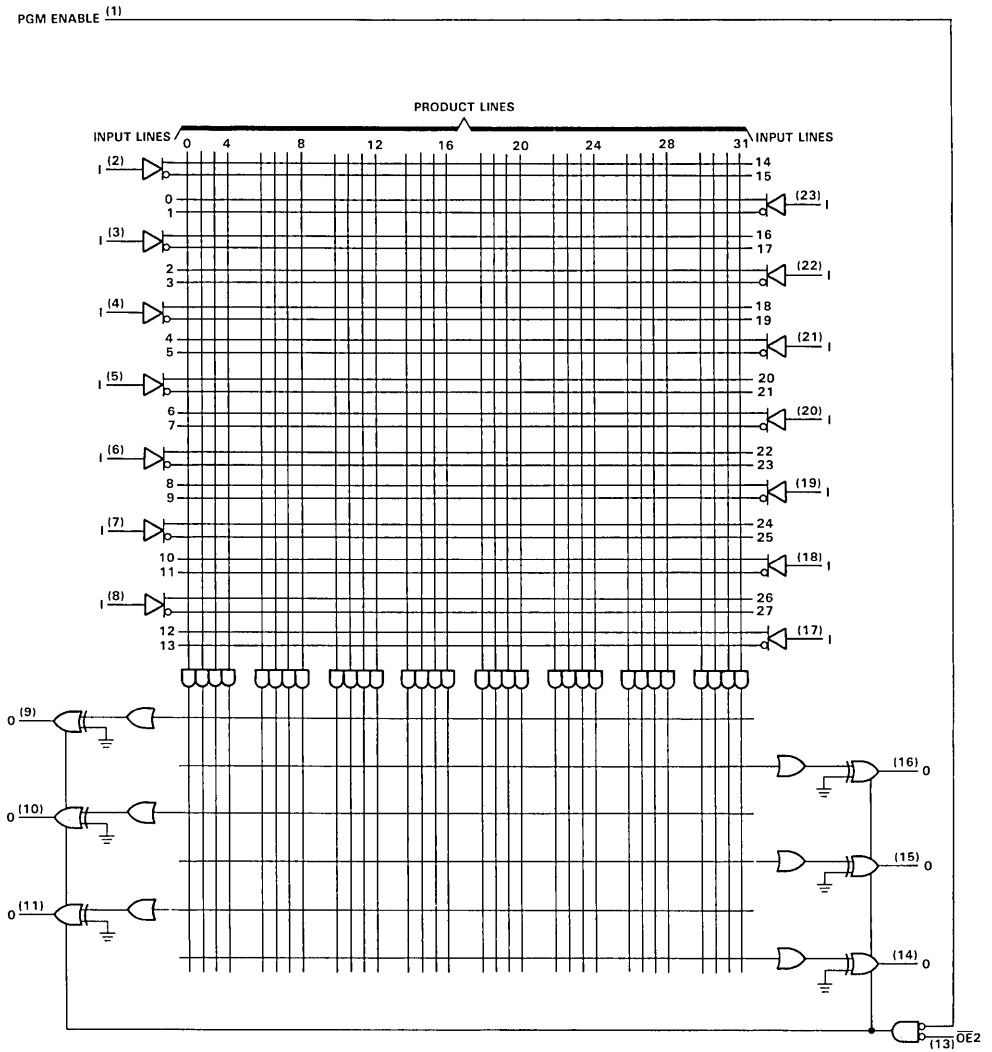


FIGURE 3– OR MATRIX PROGRAMMING WAVEFORMS

LOGIC DIAGRAM



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TYPES SN54PLR19L8, SN54PLR19R4, SN54PLR19R6, SN54PLR19R8
SN74PLR19L8, SN74PLR19R4, SN74PLR19R6, SN74PLR19R8
REGISTERED-INPUT FIXED-OR ARRAYS

D2709, DECEMBER 1982

- Standard 24-Pin, 300-mil Packages
- Output Registers Have Preload Capability
- Output Registers Automatically Clear During Power-Up
- Choice of Operating Speeds
  - -1 Parts . . . 30 MHz Max
  - -2 Parts . . . 20 MHz Max

DEVICE	I/D INPUTS	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PLR19L8	11	2	2	0	6
'PLR19R4	11	0	0	4 (3-state buffers)	4
'PLR19R6	11	0	0	6 (3-state buffers)	2
'PLR19R4	11	0	0	8 (3-state buffers)	0

3

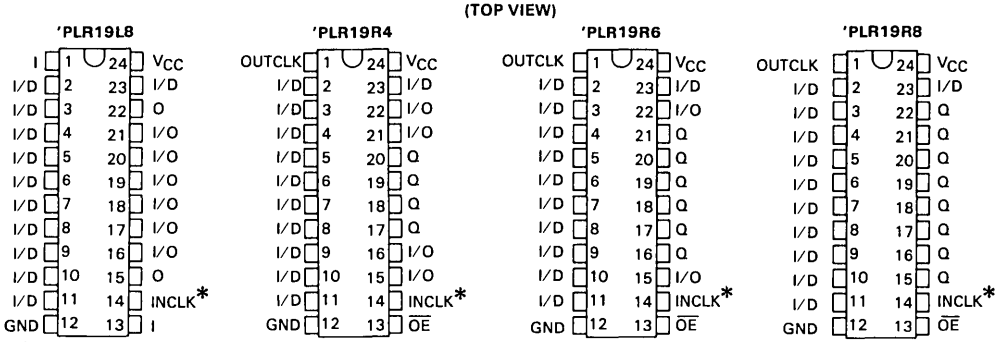
description

These fixed-OR arrays with eleven data inputs feature input registers that can be used as they are or be programmed into buffers. Some outputs of the 'PLR19R8, 'PLR19R6, and 'PLR19R4 have registers that can be loaded from the I/O pins by a preload procedure, while others are I/O ports and standard 3-state outputs. All the outputs are automatically set to a low level when power is applied. The -1 and -2 parts offer a choice of operating frequency and switching times.

The SN54PLR19' is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74PLR19' is characterized for operation from 0°C to 70°C.

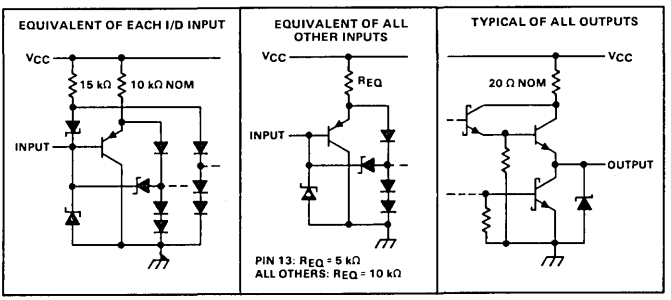
pin assignments in operating mode (voltages at pins 1 and 13 less than V_{IHH})

SN54' ... JT PACKAGE
SN74' ... NT PACKAGE
(TOP VIEW)



* Pin 14 is also used for the preload procedure on page 3-40.

schematics of inputs and outputs

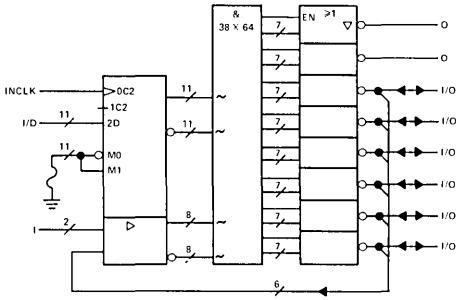


PRODUCT PREVIEW

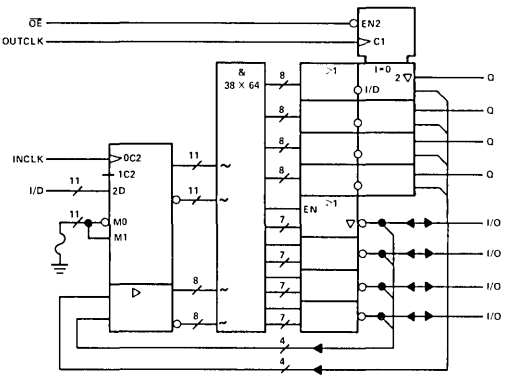
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

functional block diagrams (positive logic)

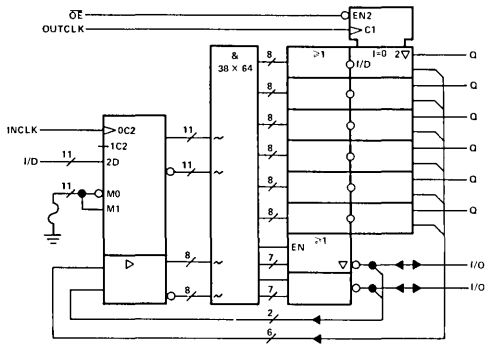
'PLR19L8



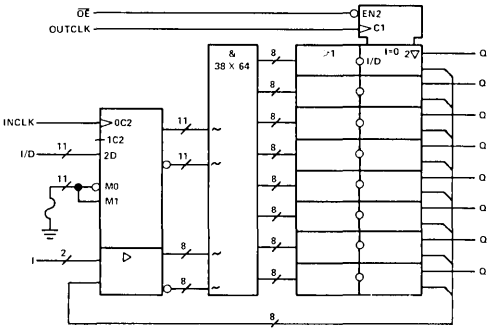
'PLR19R4



'PLR19R6



'PLR19R8



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage (see Note 1) ..... 5.5 V
Voltage applied to a disabled output (see Note 1) ..... 5.5 V
Operating free-air temperature range: SN54PLR' ..... −55°C to 125°C
SN74PLR' ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

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recommended operating conditions

		SN54PLR19'			SN74PLR19'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		5.5	2		5.5	V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS†		SN54PLR19'			SN74PLR19'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN,	I_{OH} = MAX	2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN,	I_{OL} = MAX		0.25	0.4		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX,	V_{IH} = 2.7 V			20			20	μA
	I/O ports					100			100	
I_{OZL}	Outputs	V_{CC} = MAX,	V_{IH} = 0.4 V			−20			−20	μA
	I/O ports					−250			−250	
I_I	OE Input	V_{CC} = MAX,	V_I = 5.5 V			0.2			0.2	mA
	I/D Inputs					0.1			0.1	
	All others					0.1			0.1	
I_{IH}	OE Input	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
	I/D Inputs					20			0.1	
	All others					20			0.1	
I_{IL}	OE Input	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
	I/D Inputs					−0.6			−o.6	
	All others					−0.2			−0.2	
I_O		V_{CC} = MAX,	V_O = 2.25 V	−15	−33	−65	−15	−33	−65	mA
I_{CC}		V_{CC} = MAX, Outputs open	V_I = 0 V,		150	200		150	200	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are V_{CC} = 5 V, T_A = 25°C.

input timing requirements

		MIN	MAX	UNIT
f_{clock}	Clock frequency	0	40	MHz
t_w	Clock pulse duration, clock high or low	10		ns
t_{su}	Setup time, I/D input before INCLK↑	12		ns
t_h	Hold time, I/D input before INCLK↑	0		ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

'PLR19R4, 'PLR19R6, 'PLR19R8 timing requirements

		MIN	MAX	UNIT
f_{clock}	Clock frequency	0	30	MHz
t_w	Clock pulse duration, clock high or low	12		ns
t_{su}	Setup time, input or feedback before OUTCLK↑	15		ns
t_h	Hold time, input or feedback before OUTCLK↑	0		ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	INPUT MODE	TEST CONDITIONS	−1 PARTS			−2 PARTS			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}			Either	R_L = 500Ω, C_L = 50 pF	30			20			MHz
t_{pd}	I, I/O	I/O, O	Either			16			25		ns
t_{pd}	OUTCLK ↑	Q	Either			12			20		ns
t_{en}	OE↑	Q	Either			8			15		ns
t_{dis}	OE↑	Q	Either			6			12		ns
t_{pd}	INCLK↑	I/O, O	Registered			23			32		ns
t_{en}	INCLK↑	I/O, O, Q	Registered			25			35		ns
t_{dis}	INCLK↑	I/O, O, Q	Registered			20			30		ns
t_{pd}	I/D	I/O, O	Buffered			20			30		ns
t_{en}	I/D, I/O	I/O	Buffered			22			32		ns
t_{dis}	I/D, I/O	I/O	Buffered			17			26		ns

‡All typical values are V_{CC} = 5 V, T_A = 25°C.

PRELOAD PROCEDURES

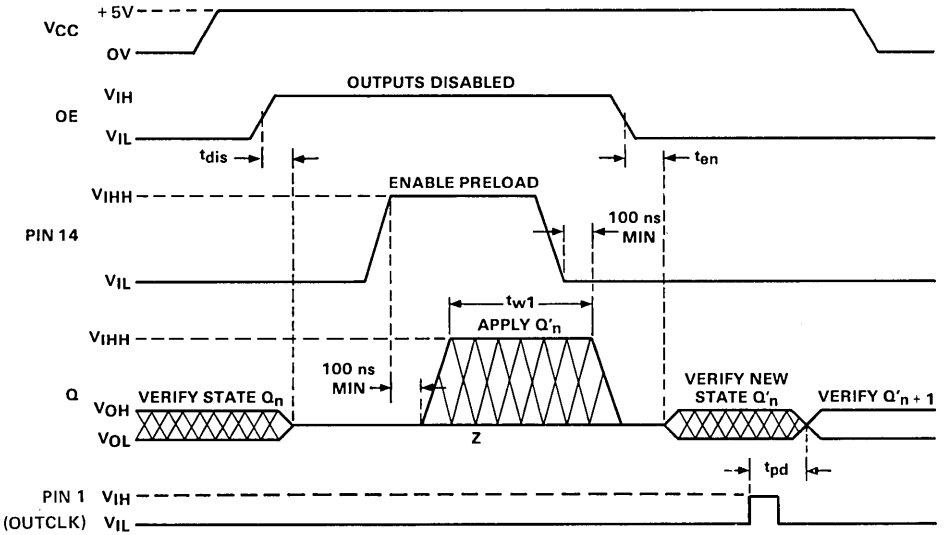

FIGURE 1—PRELOAD WAVEFORMS

preload procedure for registered outputs

Step 1	Pin 13 to V_{IH}, Pin 1 to V_{IL}, and V_{CC} to 5 volts.
Step 2	Pin 14 to V_{IHH}.
Step 3	Apply an open circuit for a low and V_{IHH} for a high at the Q outputs.
Step 4	Pin 14 to V_{IL}.
Step 5	Remove the voltages applied to the outputs.
Step 6	Pin 13 to V_{IL}.
Step 7	Check the output states to verify preload.

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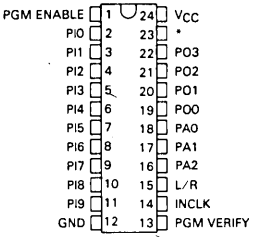
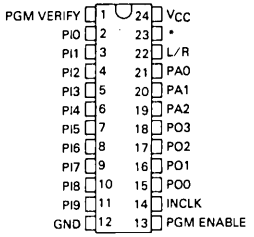
pin assignments in programming mode (PGM ENABLE, pin 1 or 13, at V_{IHH})

PRODUCT TERMS 0 THRU 31
(TOP VIEW)



PRODUCT TERMS 32 THRU 63
(TOP VIEW)



*No programming function. Make no connection.

TABLE 1—INPUT LINE SELECT

INPUT LINE NUMBER	PIN NAME										
	PI9	PI8	PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0	L/R
0	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	HH
28	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	Z
29	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	Z
30	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	HH
31	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	HH
32	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	Z
33	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	Z
34	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	HH
35	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	HH
36	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
37	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
38	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH
39	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH

TABLE 2—PRODUCT LINE SELECT

PRODUCT LINE NUMBER	PIN NAME						
	PO0	PO1	PO2	PO3	PA2	PA1	PA0
0, 32	Z	Z	Z	HH	Z	Z	Z
1, 33	Z	Z	Z	HH	Z	Z	HH
2, 34	Z	Z	Z	HH	Z	HH	Z
3, 35	Z	Z	Z	HH	Z	HH	HH
4, 36	Z	Z	Z	HH	HH	Z	Z
5, 37	Z	Z	Z	HH	HH	Z	HH
6, 38	Z	Z	Z	HH	HH	HH	Z
7, 39	Z	Z	Z	HH	HH	HH	HH
8, 40	Z	Z	HH	Z	Z	Z	Z
9, 41	Z	Z	HH	Z	Z	Z	HH
10, 42	Z	Z	HH	Z	Z	HH	Z
11, 43	Z	Z	HH	Z	Z	HH	HH
12, 44	Z	Z	HH	Z	HH	Z	Z
13, 45	Z	Z	HH	Z	HH	Z	HH
14, 46	Z	Z	HH	Z	HH	HH	Z
15, 47	Z	Z	HH	Z	HH	HH	HH
16, 48	Z	HH	Z	Z	Z	Z	Z
17, 49	Z	HH	Z	Z	Z	Z	HH
18, 50	Z	HH	Z	Z	Z	HH	Z
19, 51	Z	HH	Z	Z	Z	HH	HH
20, 52	Z	HH	Z	Z	HH	Z	Z
21, 53	Z	HH	Z	Z	HH	Z	HH
22, 54	Z	HH	Z	Z	HH	HH	Z
23, 55	Z	HH	Z	Z	HH	HH	HH
24, 56	HH	Z	Z	Z	Z	Z	Z
25, 57	HH	Z	Z	Z	Z	Z	HH
26, 58	HH	Z	Z	Z	Z	HH	Z
27, 59	HH	Z	Z	Z	Z	HH	HH
28, 60	HH	Z	Z	Z	HH	Z	Z
29, 61	HH	Z	Z	Z	HH	Z	HH
30, 62	HH	Z	Z	Z	HH	HH	Z
31, 63	HH	Z	Z	Z	HH	HH	HH

L = V_{IL}, H = V_{IH}, HH = V_{IHH}, Z = high impedance (e.g., 10 kΩ to 5V)

programming parameters

			MIN	NOM	MAX	UNIT
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage				5.5	V
V_{IHH}	Program-pulse input voltage		10.25	10.5	10.75	V
I_{IHH}	Program-pulse input current	PO			50	mA
		PGM VERIFY, L/R			25	
		PGM ENABLE, PI, PA			5	
I_{CCH}	Program-pulse supply current at V_{IHH}				550	mA
t_{w1}	Program-pulse duration at PO pins		10		50	μs
t_{w2}	Pulse duration at PGM VERIFY and INCLK		100			ns
t_{su}	Setup time		100			ns
t_h	Hold time		100			ns
t_{d1}	Delay time from V_{CC} to 6 V to PGM VERIFY↑		100			μs
t_{d2}	Delay time from PGM VERIFY↑ to verification of output		200			ns
	Input voltage at pins 1 and 13 to open verify-protect (security) fuse		20	21	22	V
	Input current to open verify-protect (security) fuse				400	mA
	Pulse duration to open verify-protect (security) fuse		20		50	ms

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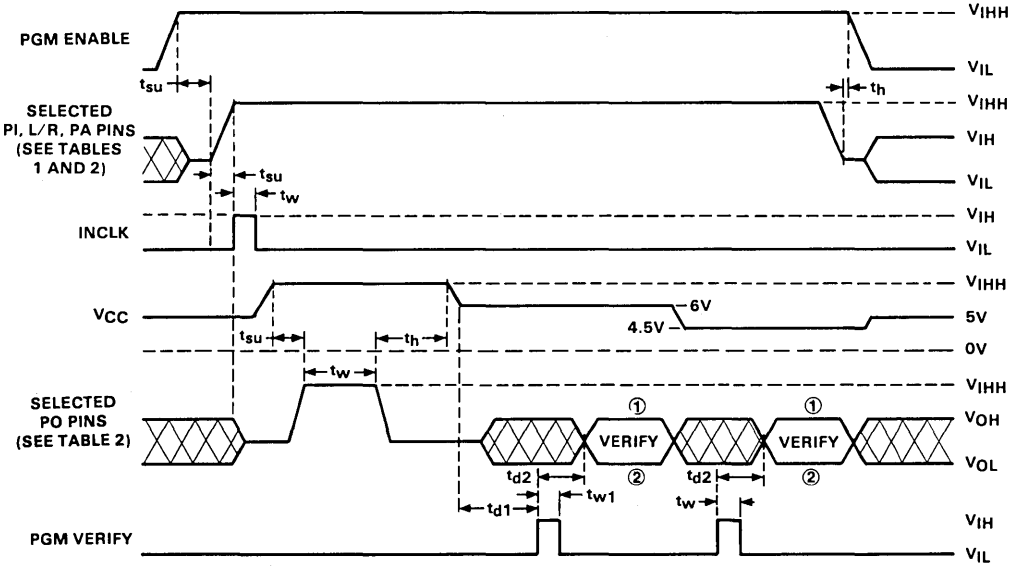

① A high level during the verify interval idicates that programming has not been successful.
② A low level during the verify interval indicates that programming has been successful.

FIGURE 2 — PROGRAMMING WAVEFORMS FOR ARRAY FUSES

programming procedure for array fuses

Array fuses are programmed using a linear select method. Each fuse can be opened by selecting the appropriate (one of 40) input line and then pulsing the correct (one of 64) product line. The levels for selecting input lines and product lines are shown in Tables 1 and 2.

Step 1	Raise PGM ENABLE to V_{IHH}.
Step 2	Select an input line by applying appropriate levels to L/R and PI pins.
Step 3	Begin selection of the output line with appropriate conditions on PA pins.
Step 4	Pulse INCLK to V_{IH}.
Step 5	Raise V_{CC} to V_{IHH}.
Step 6	Blow the fuse by pulsing the appropriate PO pin to V_{IHH} as shown in Table 2 for the product line.
Step 7	Lower V_{CC} to 6 volts and pulse PGM VERIFY. The PO pin selected in Step 4 will be less than V_{OL} if the fuse is open.
Step 8	Lower V_{CC} to 4.5 volts and pulse PGM VERIFY. The PO pin selected in Step 4 will be less than V_{OL} if the fuse is open.

Steps 1 thru 8 may be repeated if the verification does not indicate that the fuse was successfully programmed (blown), but no more than 4 times. Verification is possible only with the verify-protect fuse intact.

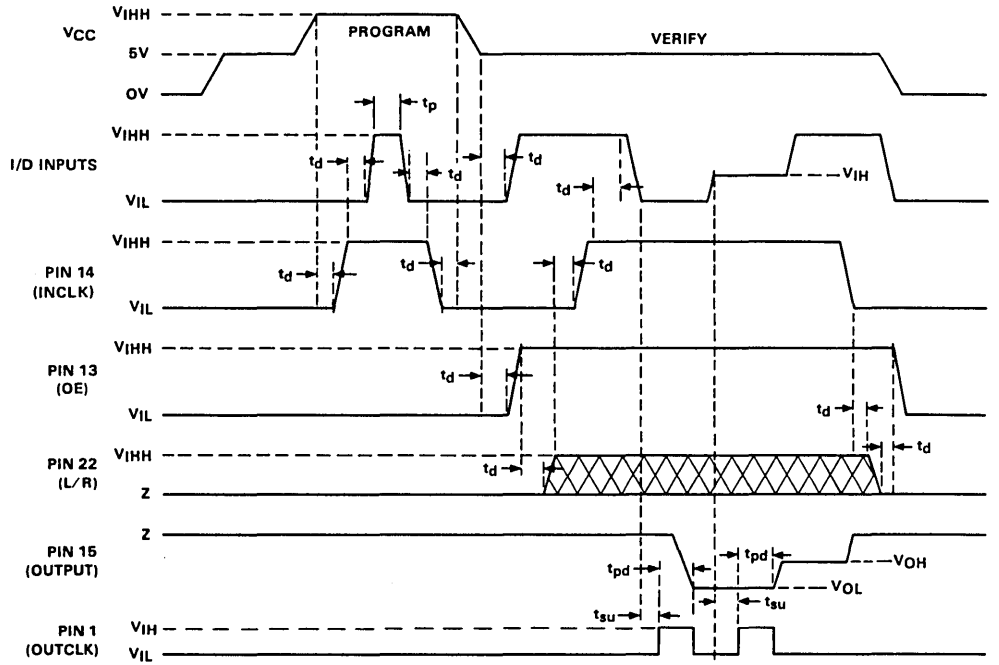

FIGURE 3 — ARCHITECTURAL FUSE PROGRAMMING WAVEFORMS

programming procedure for architectural fuses (see Note 2)

Step 1	Apply low levels to all I/D pins and 5 volts to the V_{CC} pin.
Step 2	Raise V_{CC} pin to V_{IHH}.
Step 3	Raise INCLK pin to V_{IHH}.
Step 4	To program a D input pin into an I input pin pulse the selected pin to V_{IHH}.
Step 5	Lower INCLK to V_{IL} and V_{CC} to 5 volts.
Step 6	Raise pin 13 and all I/D input pins to V_{IHH}.
Step 7	Set pin 22 to Z to select pins 2 thru 11 or set pin 22 to V_{IHH} to select pin 23.
Step 8	Raise INCLK to V_{IHH}.
Step 9	To verify that fuse has been blown, pulse selected I pin from V_{IHH} to V_{IL}, then to V_{IH} and back to V_{IHH} while clocking pin 1. If output at pin 15 follows the I input the fuse has been blown.
Step 10	Repeat above steps 1 thru 9 for each D input to be programmed into an I input.

NOTE 2: Refer to pin assignments in operating mode for programming selected I/D pins from D inputs to I inputs.

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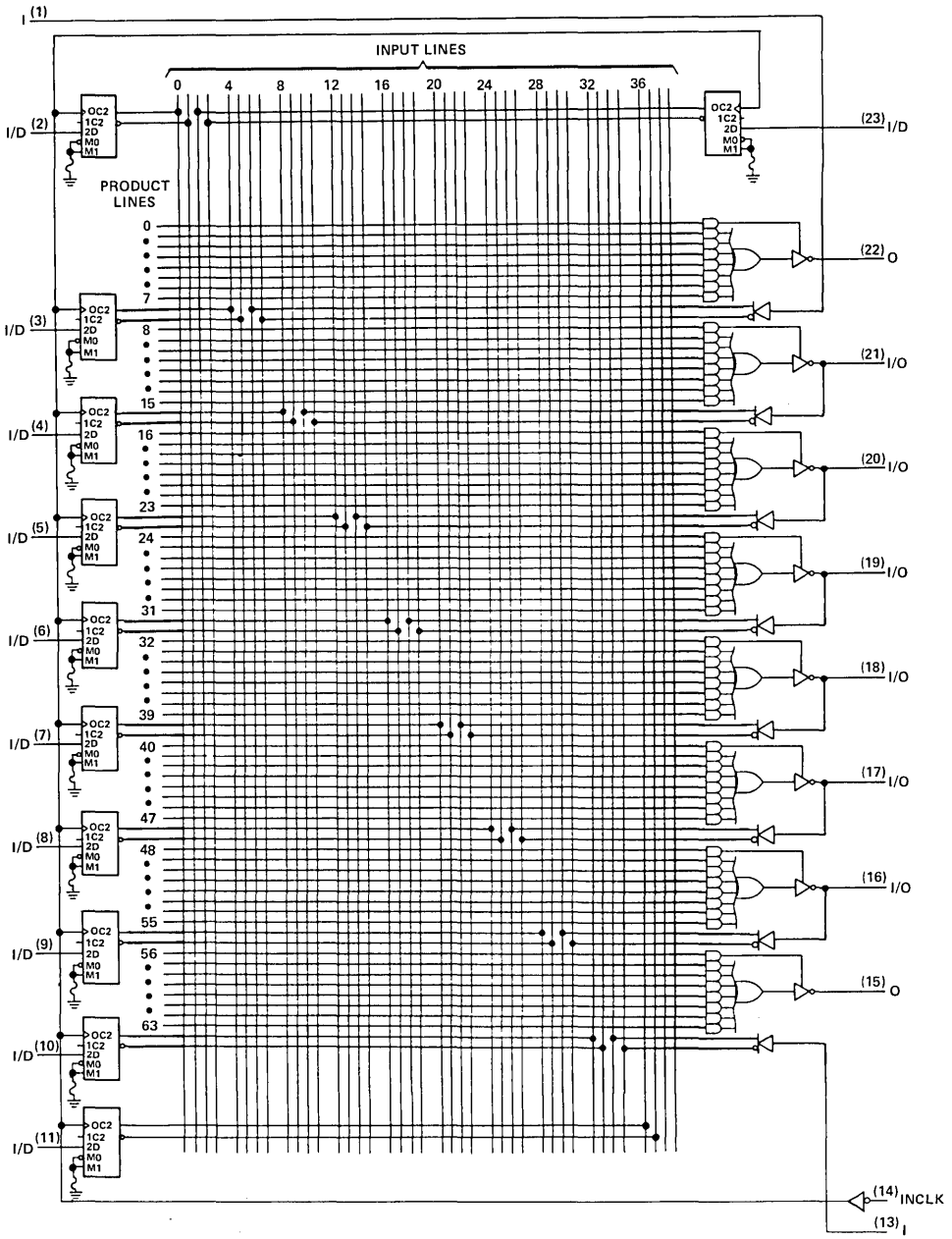
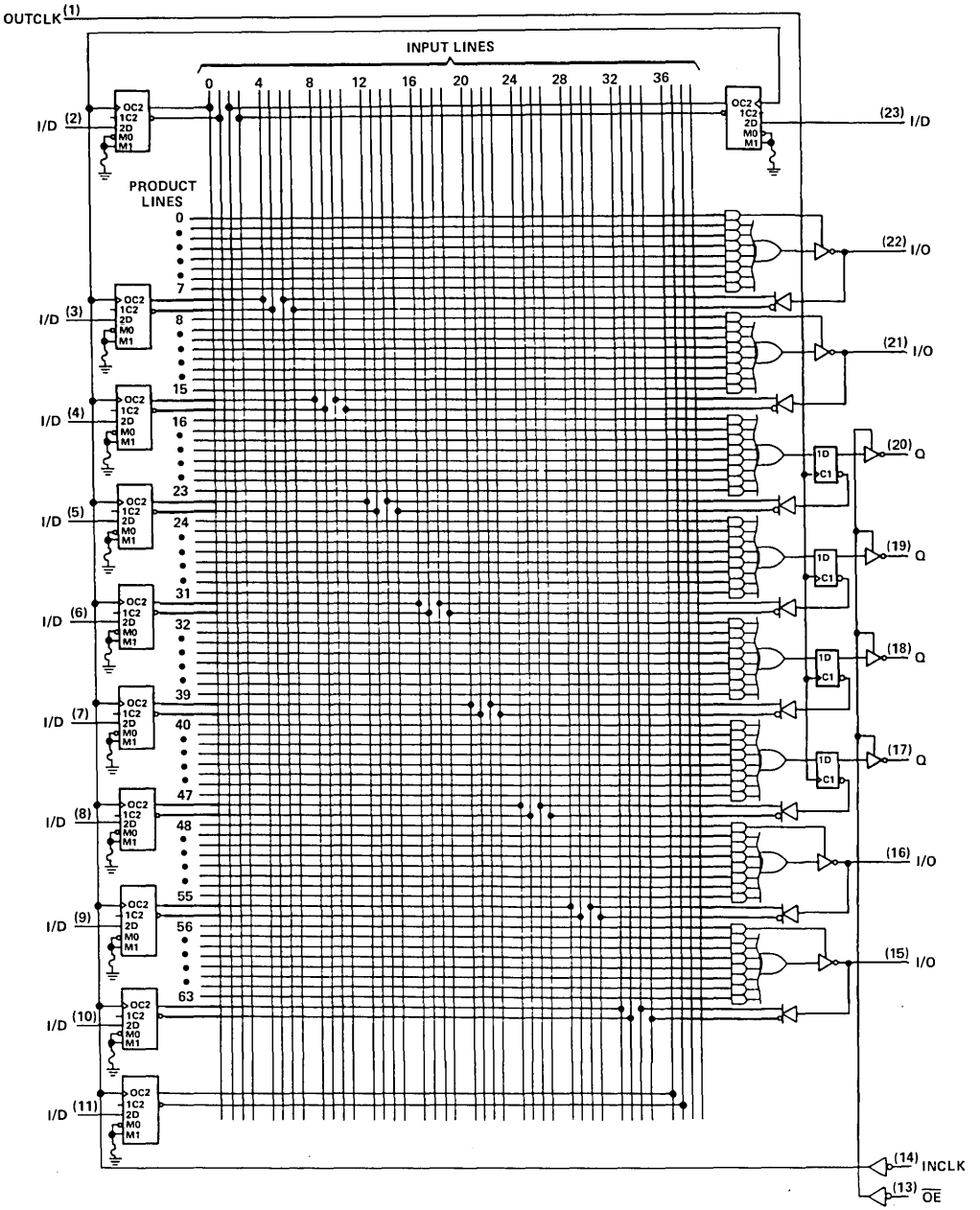

I (1)
INPUT LINES
0 4 8 12 16 20 24 28 32 36
I/D (2)
I/D (3)
I/D (4)
I/D (5)
I/D (6)
I/D (7)
I/D (8)
I/D (9)
I/D (10)
I/D (11)
OC2
1C2
2D
M0
M1
PRODUCT LINES
0
7
8
15
16
23
24
31
32
39
40
47
48
55
56
63
(23) I/D
(22) O
(21) I/O
(20) I/O
(19) I/O
(18) I/O
(17) I/O
(16) I/O
(15) O
(14) INCLK
(13) I



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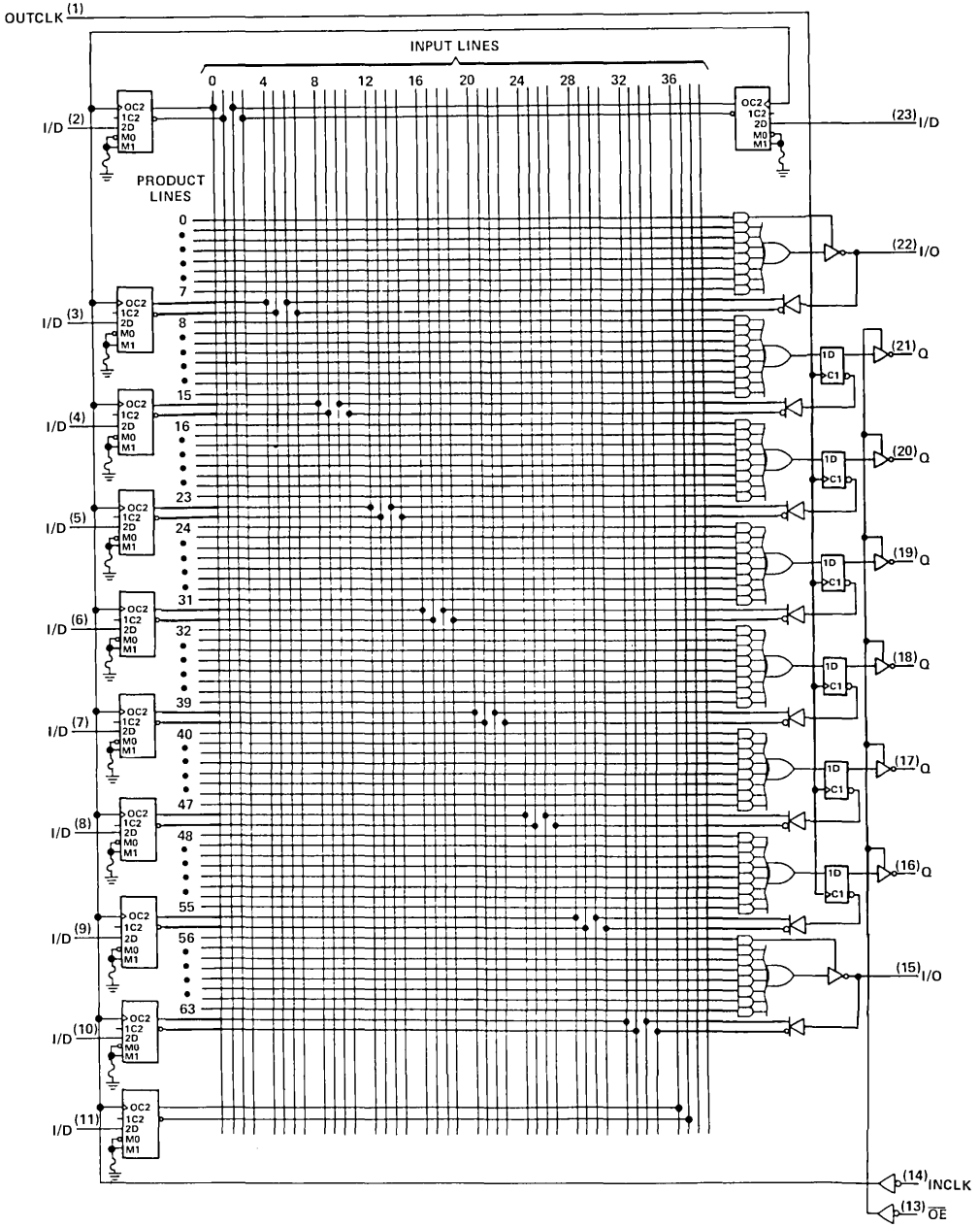
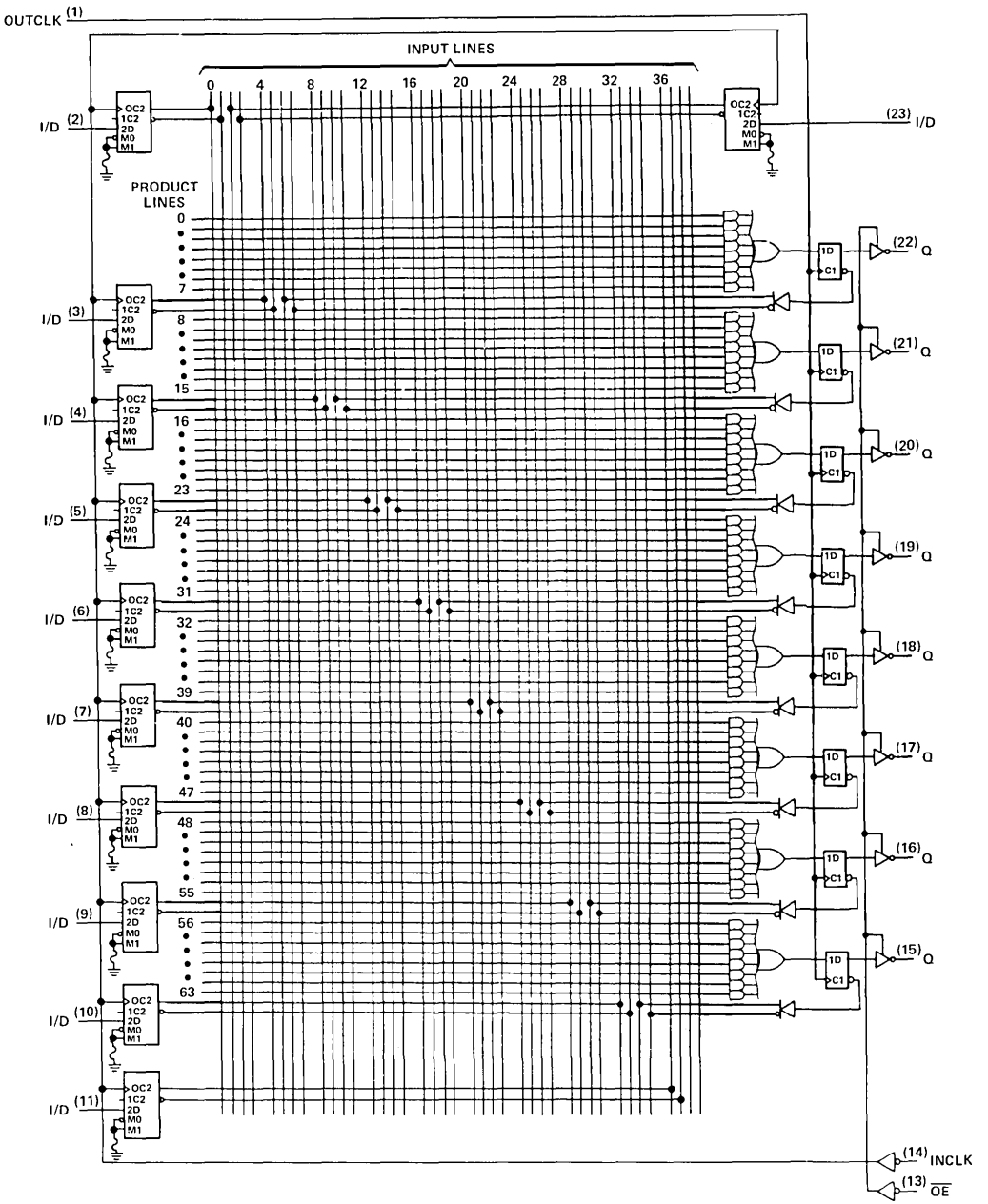

OUTCLK (1)
INPUT LINES
0 4 8 12 16 20 24 28 32 36
PRODUCT LINES
I/D (2)
I/D (3)
I/D (4)
I/D (5)
I/D (6)
I/D (7)
I/D (8)
I/D (9)
I/D (10)
I/D (11)
OC2 1C2 2D M0 M1
0 7 8 15 16 23 24 31 32 39 40 47 48 55 56 63
(23) I/D
(22) I/O
(21) Q
(20) Q
(19) Q
(18) Q
(17) Q
(16) Q
(15) I/O
1D C1
(14) INCLK
(13) OE



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TYPES SN54PLT19L8, SN54PLT19R4, SN54PLT19R6, SN54PLT19R8 SN74PLT19L8, SN74PLT19R4, SN74PLT19R6, SN74PLT19R8 LATCHED-INPUT FIXED-OR ARRAYS

D2710, DECEMBER 1982

- Standard 24-Pin, 300-mil Packages
- Output Registers Automatically Clear During Power-Up
- Output Registers Have Preload Capability
- Data Input Registers Programmable to Buffers
- Choice of Operating Speeds
  - -1 Parts . . . 30 MHz Max
  - -2 Parts . . . 20 MHz Max

DEVICE	I/D INPUTS	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PLT19L8	11	2	2	—	6
'PLT19R8	11	0	0	8 (3-state buffers)	0
'PLT19R6	11	0	0	6 (3-state buffers)	2
'PLT19R4	11	0	0	4 (3-state buffers)	4

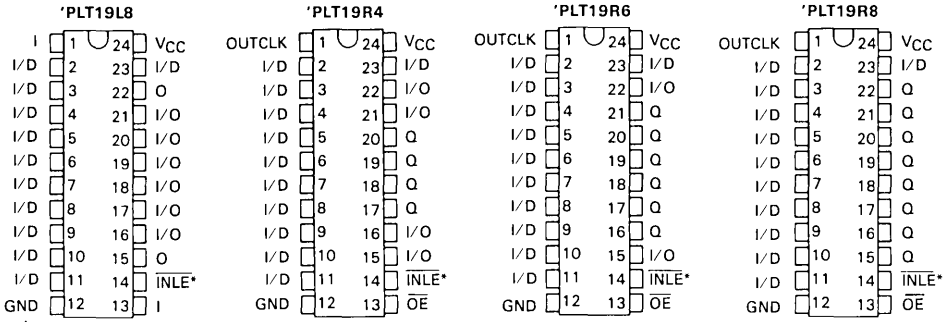
description

These fixed-OR arrays with eleven data inputs provide input registers that can be used as they are or be programmed into buffers. Some outputs of the 'PLT19R8, 'PLT19R6, and 'PLT19R4 have registers that can be loaded from the I/O pins by a preload procedure, while others are I/O ports and standard 3-state outputs. All the outputs are automatically set to a low level when power is applied. The -1 and -2 parts offer a choice of operating frequency and switching times.

The SN54PLT19' is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74PLT19' is characterized for operation from 0°C to 70°C.

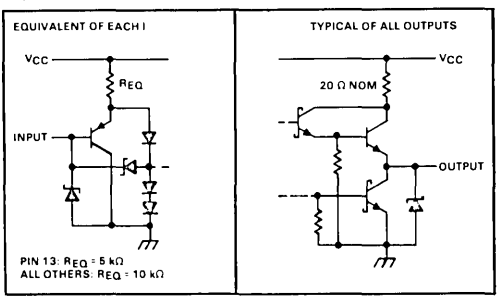
pin assignments in operating mode (voltages at pins 1 and 13 less than V_{IHH})

SN54' ... JT PACKAGE
SN74' ... NT PACKAGE
(TOP VIEW)



* Pin 14 is also used for the preload procedure on page 3-52.

schematics of inputs and outputs

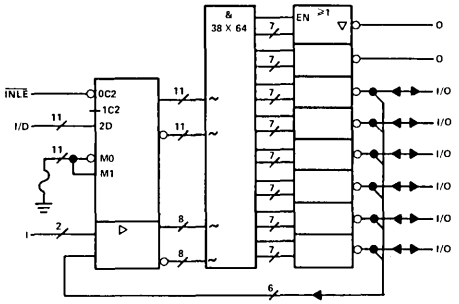


PRODUCT PREVIEW

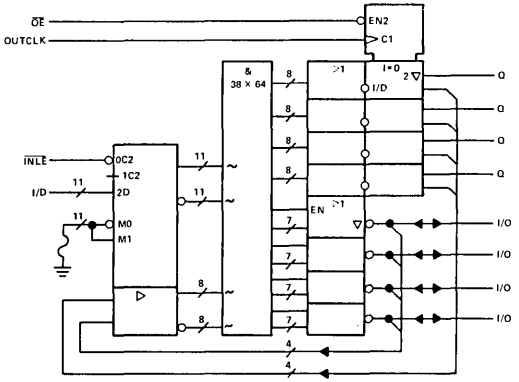
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

functional block diagrams

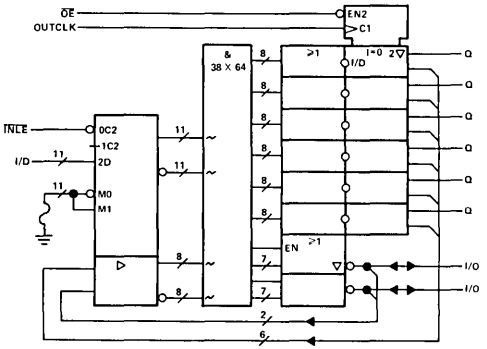
'PLT19L8



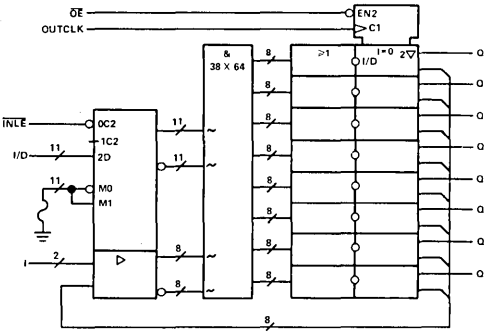
'PLT19R4



'PLT19R6



'PLT19R8



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage (see Note 1) ..... 5.5 V
Voltage applied to a disabled output (see Note 1) ..... 5.5 V
Voltage at any programming pin ..... 12 V
Operating free-air temperature range: SN54PLR' ..... −55°C to 125°C
SN74PLR' ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

		SN54PLT19'			SN74PLT19'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		5.5	2		5.5	V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS†		SN54PLT19'			SN74PLT19'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN,	I_{OH} = MAX	2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN,	I_{OL} = MAX		0.25	0.4		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX,	V_O = 2.7 V			20			20	μA
	I/O ports					100			100	
I_{OZL}	Outputs	V_{CC} = MAX,	V_O = 0.4 V			−20			−20	μA
	I/O ports					−250			−250	
I_I	$\overline{OE}$ Input	V_{CC} = MAX,	V_I = 5.5 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	$\overline{OE}$ Input	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
	All others					20			0.1	
I_{IL}	$\overline{OE}$ Input	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
	All others					−0.2			−0.2	
I_O		V_{CC} = MAX,	V_O = 2.25 V	−15	−33	−65	−15	−33	−65	mA
I_{CC}		V_{CC} = MAX, Outputs open	V_I = 0 V,		150	200		150	200	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

'PLT19R8, 'PLT19R6, 'PLT19R4 timing requirements

		-1 PARTS		-2 PARTS		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	30	0	30	MHz
t_w	Clock pulse duration, clock high or low	12		12		ns
t_{su}	Setup time, D input before $\overline{INLE}$↑					ns
t_{su}	Setup time, input or feedback before OUTCLK↑	15		15		ns
t_h	Hold time, input or feedback before OUTCLK↑	0		0		ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	INPUT MODE	TEST CONDITIONS	– 1 PARTS			– 2 PARTS			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}			Either		30			20			MHz
t_{pd}	I, I/O	I/O, O	Either			16			25		ns
t_{pd}	OUTCLK ↑	Q	Either			12			20		ns
t_{en}	$\overline{OE}$↓	Q	Either			8			15		ns
t_{dis}	$\overline{OE}$↑	Q	Either			6			12		ns
t_{pd}	$\overline{INLE}$	I/O, O	Latched			16			25		ns
t_{en}	$\overline{INLE}$	I/O, O, Q	Latched			25			35		ns
t_{dis}	$\overline{INLE}$	I/O, O, Q	Latched			20			30		ns
t_{pd}	I/D	I/O, O	Buffered			20			30		ns
t_{en}	I/D, I/O	I/O	Buffered			22			32		ns
t_{dis}	I/D, I/O	I/O	Buffered			17			26		ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

3

PRELOAD PROCEDURES

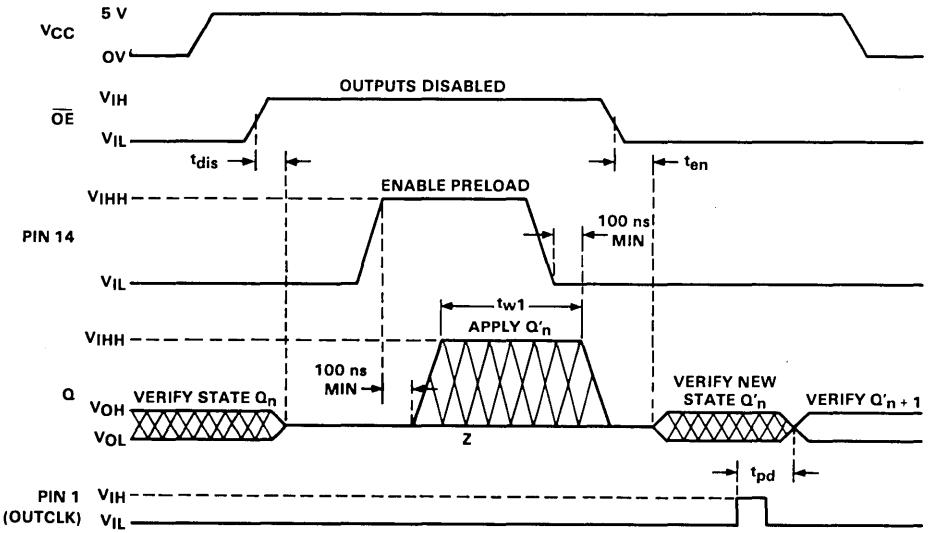


FIGURE 1—PRELOAD VOLTAGE WAVEFORMS

preload procedure for registered outputs

Step 1	Pin 13 to V_{IH}, Pin 1 to V_{IL}, and V_{CC} to 5 volts.
Step 2	Pin 14 to V_{IHH}.
Step 3	Apply an open circuit for a low and V_{IHH} for a high at the Q outputs.
Step 4	Pin 14 to V_{IL}.
Step 5	Remove the voltages applied to the outputs.
Step 6	Pin 13 to V_{IL}.
Step 7	Check the output states to verify preload.

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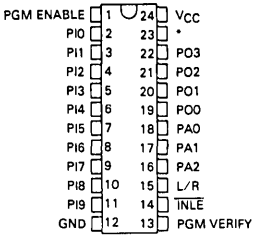
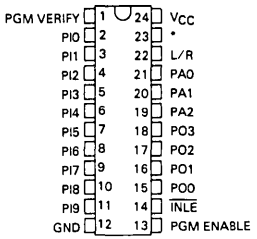
pin assignments in programming mode (PGM ENABLE, pin 1 or 11, at V_{IHH})

PRODUCT TERMS 0 THRU 31
(TOP VIEW)



PRODUCT TERMS 32 THRU 63
(TOP VIEW)



*No programming function. Make no connection.

3

TABLE 1—INPUT LINE SELECT

INPUT LINE NUMBER	PIN NAME										
	PI9	PI8	PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0	L/R
0	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	HH
28	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	Z
29	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	Z
30	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	HH
31	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	HH
32	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	Z
33	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	Z
34	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	HH
35	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	HH
36	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
37	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
38	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH
39	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH

L = V_{IL}, H = V_{IH}, HH = V_{IHH}, Z = high impedance (e.g., 10 kΩ to 5 V)

TABLE 2—PRODUCT LINE SELECT

PRODUCT LINE NUMBER	PIN NAME						
	PO0	PO1	PO2	PO3	PA2	PA1	PA0
0, 32	Z	Z	Z	HH	Z	Z	Z
1, 33	Z	Z	Z	HH	Z	Z	HH
2, 34	Z	Z	Z	HH	Z	HH	Z
3, 35	Z	Z	Z	HH	Z	HH	HH
4, 36	Z	Z	Z	HH	HH	Z	Z
5, 37	Z	Z	Z	HH	HH	Z	HH
6, 38	Z	Z	Z	HH	HH	HH	Z
7, 39	Z	Z	Z	HH	HH	HH	HH
8, 40	Z	Z	HH	Z	Z	Z	Z
9, 41	Z	Z	HH	Z	Z	Z	HH
10, 42	Z	Z	HH	Z	Z	HH	Z
11, 43	Z	Z	HH	Z	Z	HH	HH
12, 44	Z	Z	HH	Z	HH	Z	Z
13, 45	Z	Z	HH	Z	HH	Z	HH
14, 46	Z	Z	HH	Z	HH	HH	Z
15, 47	Z	Z	HH	Z	HH	HH	HH
16, 48	Z	HH	Z	Z	Z	Z	Z
17, 49	Z	HH	Z	Z	Z	Z	HH
18, 50	Z	HH	Z	Z	Z	HH	Z
19, 51	Z	HH	Z	Z	Z	HH	HH
20, 52	Z	HH	Z	Z	HH	Z	Z
21, 53	Z	HH	Z	Z	HH	Z	HH
22, 54	Z	HH	Z	Z	HH	HH	Z
23, 55	Z	HH	Z	Z	HH	HH	HH
24, 56	HH	Z	Z	Z	Z	Z	Z
25, 57	HH	Z	Z	Z	Z	Z	HH
26, 58	HH	Z	Z	Z	Z	HH	Z
27, 59	HH	Z	Z	Z	Z	HH	HH
28, 60	HH	Z	Z	Z	HH	Z	Z
29, 61	HH	Z	Z	Z	HH	Z	HH
30, 62	HH	Z	Z	Z	HH	HH	Z
31, 63	HH	Z	Z	Z	HH	HH	HH

programming parameters

			MIN	NOM	MAX	UNIT
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage				5.5	V
V_{IHH}	Program-pulse input voltage		11	11.5	12	V
I_{IHH}	Program-pulse input current	PO			50	mA
		PGM VERIFY, L/R			25	
		PGM ENABLE, PI, PA			5	
I_{CHH}	Program-pulse supply current				550	mA
t_{w1}	Program-pulse duration at PO pins		10		50	μs
t_{w2}	Pulse duration at PGM VERIFY		100			ns
t_{su}	Setup time		100			ns
t_h	Hold time		100			ns
t_{d1}	Delay time from V_{CC} to 6 V to PGM VERIFY†		100			μs
t_{d2}	Delay time from PGM VERIFY† to valid output		200			ns
	Input voltage at pins 1 and 13 to open verify-protect (security) fuse		20	21	22	V
	Input current to open verify-protect (security) fuse				400	mA
	Pulse duration to open verify-protect (security) fuse		20		50	ms

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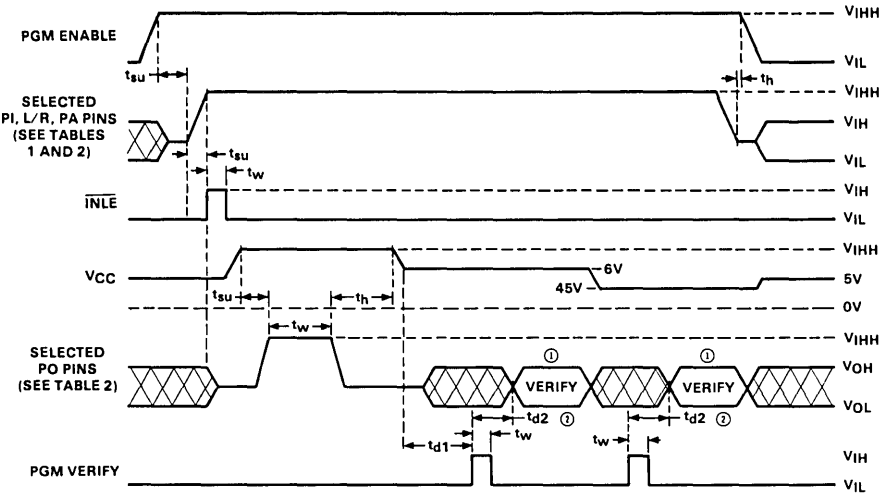

① A high level during the verify interval indicates that programming has not been successful.
② A low level during the verify interval indicates that programming has been successful.

FIGURE 2 — ARRAY PROGRAMMING WAVEFORMS

programming procedure for array fuses

Array fuses are programmed using a linear select method. Each fuse can be opened by selecting the appropriate (one of 40) input line and then pulsing the correct (one of 64) product line. The levels for selecting input lines and product lines are shown in Tables 1 and 2.

Step 1	Raise PGM ENABLE to V_{IHH}.
Step 2	Select an input line by applying appropriate levels to PI and L/R pins.
Step 3	Begin selection of the output line with appropriate conditions on PA pins (see Table 2).
Step 4	Pulse $\overline{INLE}$ to V_{IHH}.
Step 5	Raise V_{CC} to V_{IHH}.
Step 6	Blow the fuse by pulsing the appropriate PO pin to V_{IHH} as shown in Table 2 for the product line.
Step 7	Lower V_{CC} to 6 volts and pulse PGM VERIFY. The PO pin selected in Step 4 will be less than V_{OL} if the fuse is open.
Step 8	Lower V_{CC} to 4.5 volts and pulse PGM VERIFY. The PO pin selected in Step 4 will be less than V_{OL} if the fuse is open.

Steps 1 thru 8 may be repeated if the verification does not indicate that the fuse was successfully programmed (blown), but no more than 4 times. Verification is possible only with the verify-protect fuse intact.

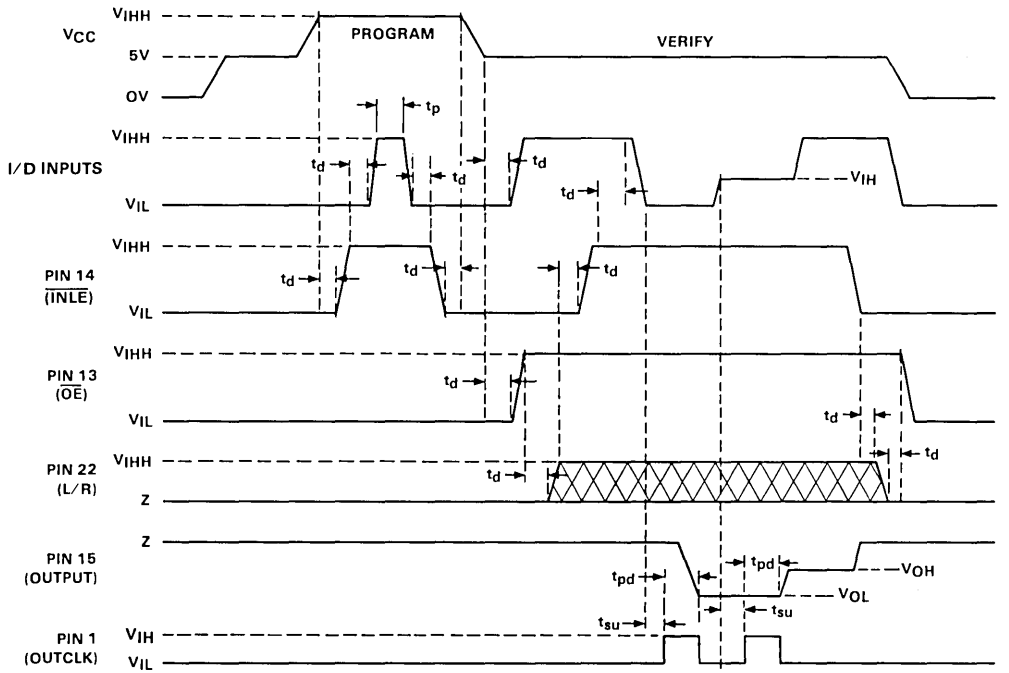

FIGURE 3 — ARCHITECTURAL FUSE PROGRAMMING WAVEFORMS

programming procedure for architectural fuses (see Note 2)

Step 1	Apply low levels to all I/D pins and 5 volts to the V_{CC} pin.
Step 2	Raise V_{CC} pin to V_{IHH}.
Step 3	Raise $\overline{INLE}$ pin to V_{IHH}.
Step 4	To program a D input pin into an I input pin pulse the selected pin to V_{IHH}.
Step 5	Lower $\overline{INLE}$ to V_{IL} and V_{CC} to 5 volts.
Step 6	Raise pin 13 and all I/D input pins to V_{IHH}.
Step 7	Set pin 22 to Z to select pins 2 thru 11 or set pin 22 to V_{IHH} to select pin 23.
Step 8	Raise $\overline{INLE}$ to V_{IHH}.
Step 9	To verify that fuse has been blown, pulse selected I pin from V_{IHH} to V_{IL}, then to V_{IH} and back to V_{IHH} while clocking pin 1. If output at pin 15 follows the I input the fuse has been blown.
Step 10	Repeat above steps 1 thru 9 for each D input to be programmed into an I input.

NOTE 2: Refer to pin assignments in operating mode for programming selected I/D pins from D inputs to I inputs.

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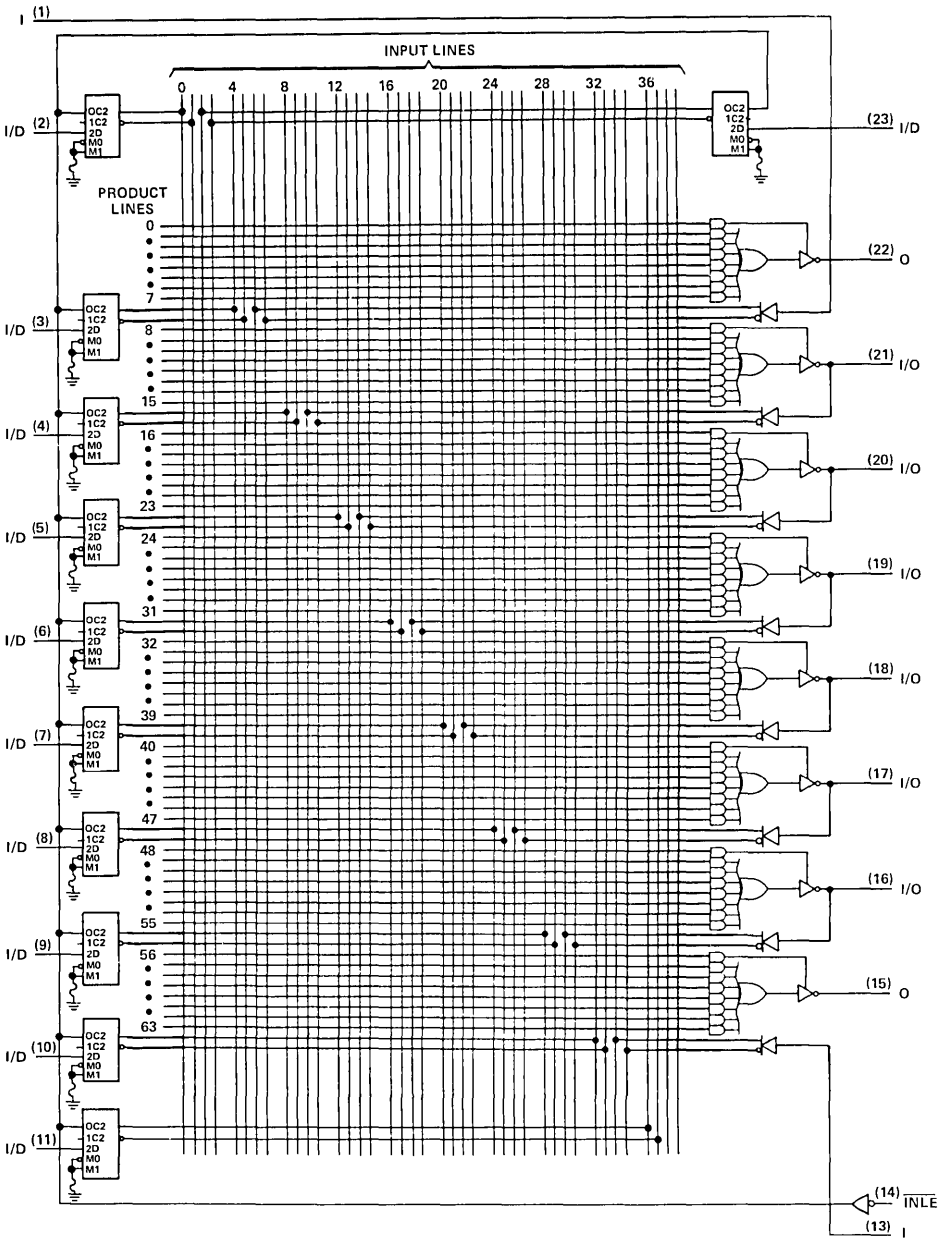
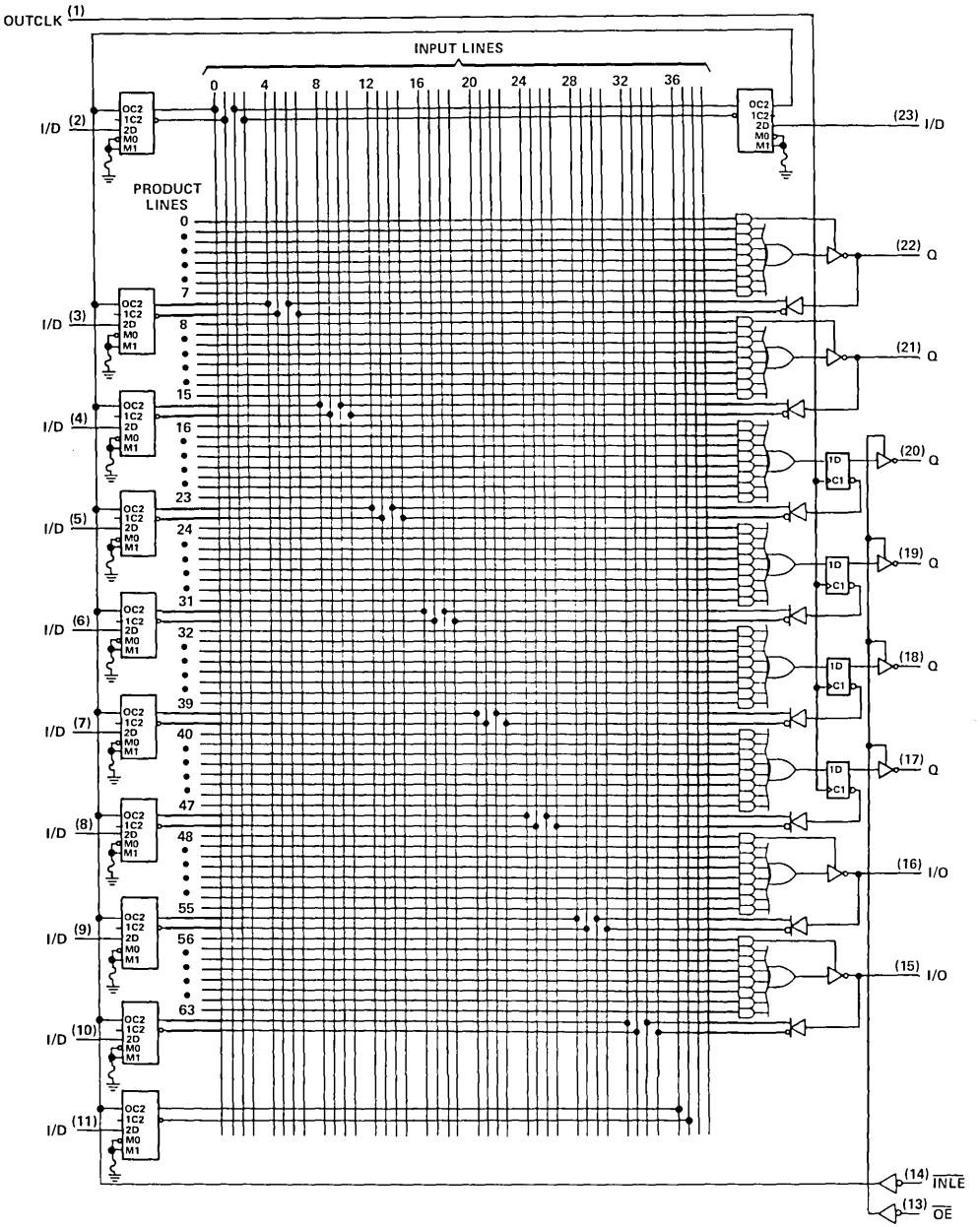

I (1)
INPUT LINES
0 4 8 12 16 20 24 28 32 36
I/D (2)
I/D (3)
I/D (4)
I/D (5)
I/D (6)
I/D (7)
I/D (8)
I/D (9)
I/D (10)
I/D (11)
OC2 1C2 2D M0 M1
PRODUCT LINES
0
7
8
15
16
23
24
31
32
39
40
47
48
55
56
63
(23) I/D
(22) O
(21) I/O
(20) I/O
(19) I/O
(18) I/O
(17) I/O
(16) I/O
(15) O
(14) INLE
(13) I



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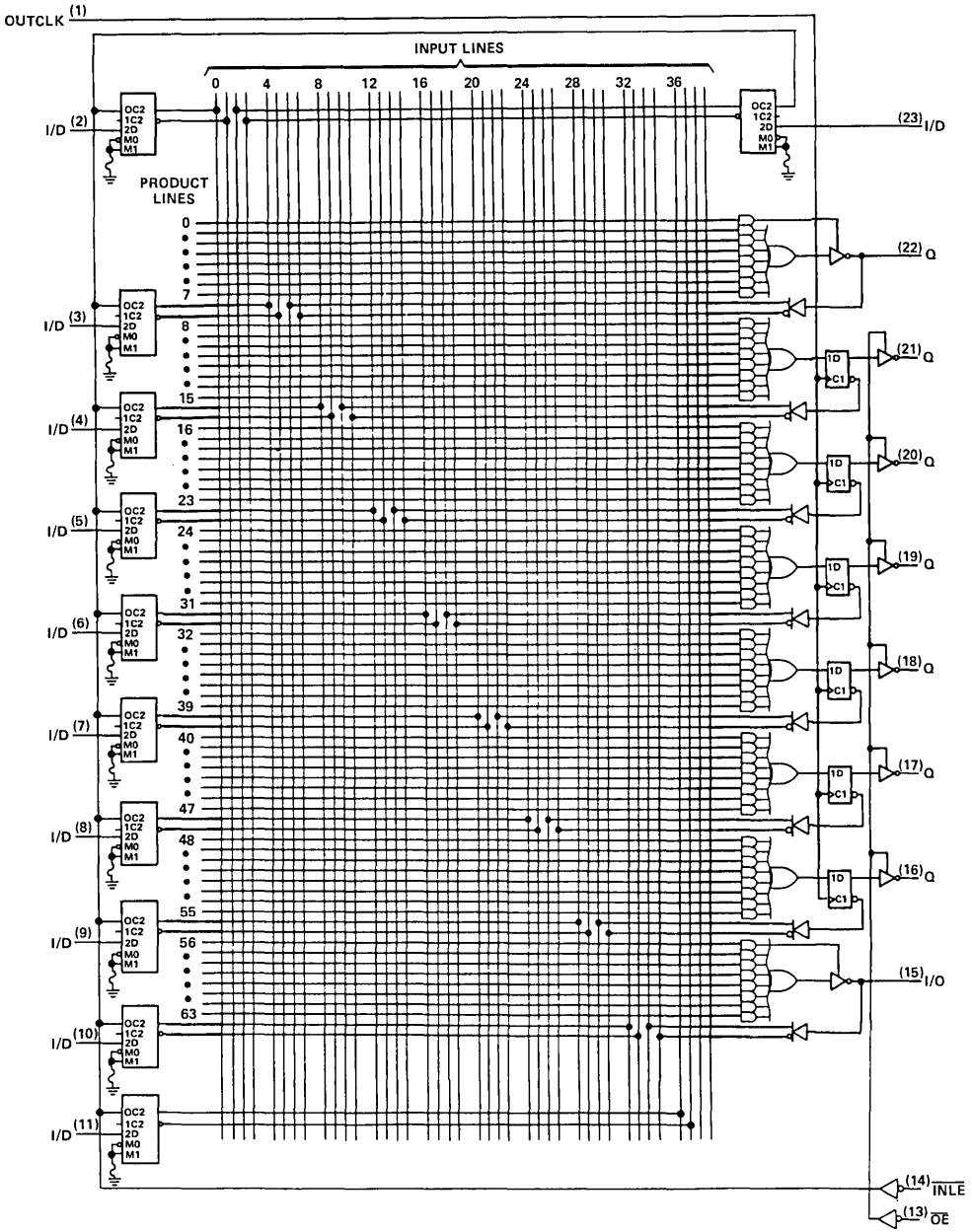
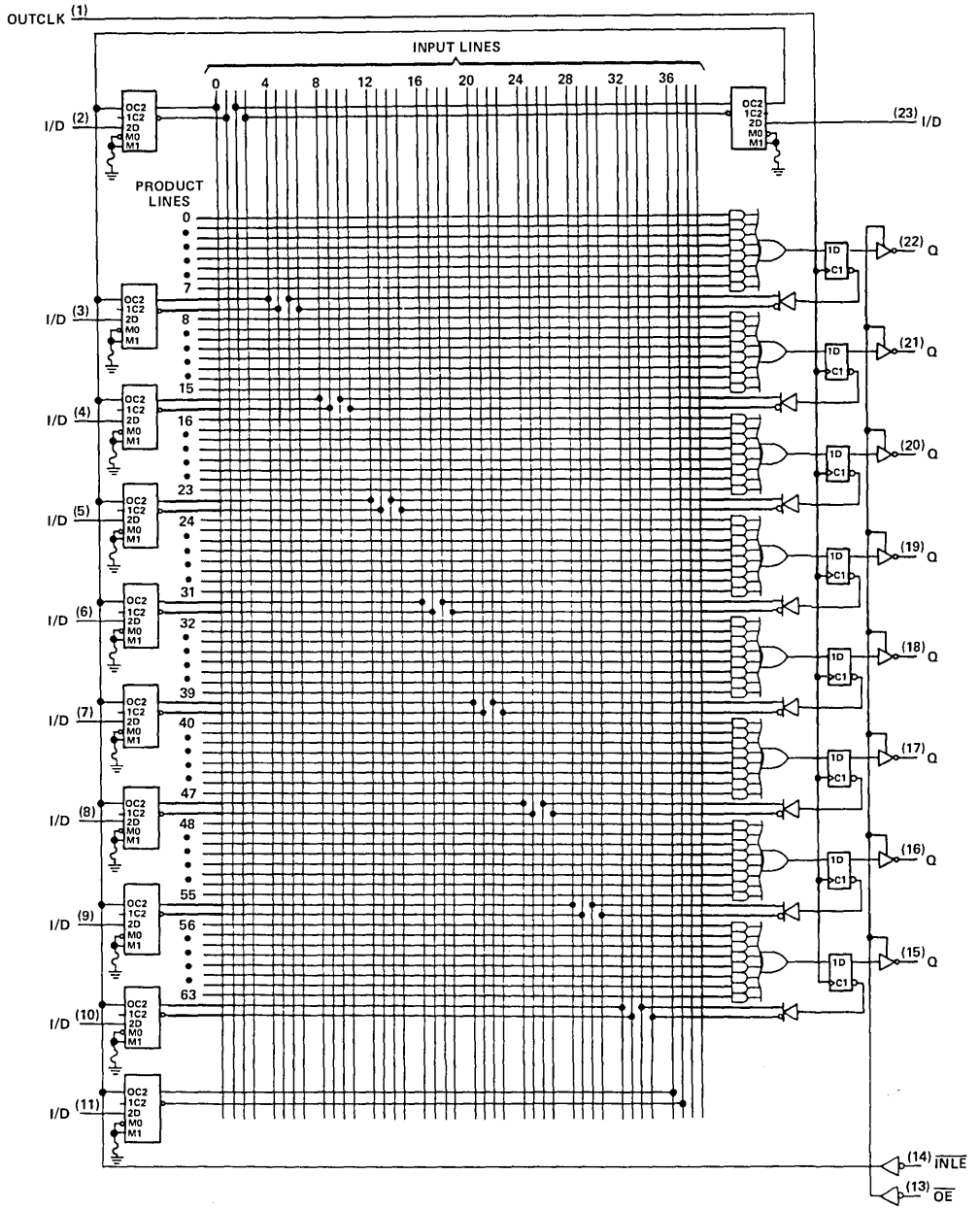

OUTCLK (1)
INPUT LINES
0 4 8 12 16 20 24 28 32 36
PRODUCT LINES
I/D (2)
I/D (3)
I/D (4)
I/D (5)
I/D (6)
I/D (7)
I/D (8)
I/D (9)
I/D (10)
I/D (11)
OC2 1C2 2D M0 M1
0 7 8 15 16 23 24 31 32 39 40 47 48 55 56 63
(23) I/D
(22) Q
(21) Q
(20) Q
(19) Q
(18) Q
(17) Q
(16) Q
(15) I/O
1D C1
(14) INLE
(13) OE



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PLA APPLICATIONS

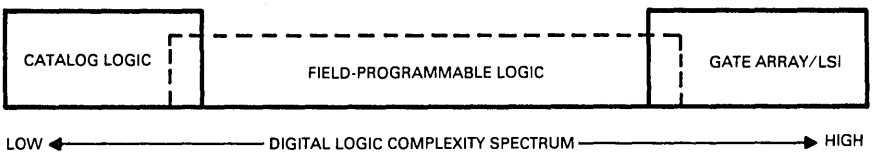
FIELD PROGRAMMABLE LOGIC

INTRODUCTION

Texas Instruments Field-Programmable Logic is the result of combining established Advanced Low-Power Schottky technology with the familiar Titanium-Tungsten (TiW) fuse-link technology used in PROMs to produce a family of powerful new user-programmed devices. Not everyone is familiar as yet with the Field-Programmable Fixed-OR Array (FOA), Logic Sequencer (FPLS), and Logic Array (FPLA). The highlights below are presented to start the process of familiarization by describing some of the unique advantages available to the designer who can create custom logic on demand to meet special requirements.

- *Package count reduction* compared to standard catalog SSI and MSI logic.
- *Lower cost* due to reduction in substrate or PC area, connectors, overall system size, and assembly labor.
- *Improved reliability* through fewer interconnects (IC bond wires, solder connections, through-holes in PC boards, connector contacts) and simplified substrate circuitry.
- *Circuit flexibility* that will adapt to custom applications.
- *Shorter design cycle* as compared to special-order devices.

Field-Programmable Logic is intended to integrate functions normally implemented with standard gates, flip-flops, and MSI. It can be used to reduce miscellaneous logic package count, or as "glue" around high-density LSI circuitry (i.e., microprocessors and gate arrays). It is positioned as a "gap filler" between standard catalog logic devices and large-scale integration.



DEFINITIONS AND SYMBOLOGY

Just as logic symbols simplified schematics, the new terms and symbology presented here will simplify array logic diagrams for programmable devices. New terms will be highlighted by italics throughout the text.

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SYMBOLOGY

All the products presented are variations of a basic two-array architecture. A typical Field-Programmable Logic device may have over 100 gates and in excess of 1000 fuses. Because of this, it is necessary to devise a shorthand symbology to simplify logic diagrams. The logic diagrams used in this data book will adhere to the symbology presented below.

First, view a conventional two-input AND gate. Inputs are designated as A and B. The output function of the AND gate is the product of the inputs (F = A·B).

FIGURE 1

Now redraw the same logic element using array symbology (Figure 2). Notice that the AND gate is represented as having a single input called a *product line*. The *input terms* are shown as lines perpendicular to the product line. The output (*product term*) is the product of the input terms.

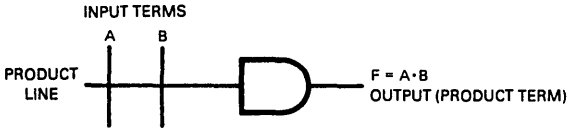

FIGURE 2

In the following figure we will extend the symbology to develop a simple programmable array element. First, notice that buffers have been added to the inputs. These buffers make available both true and complement states of any input to the product lines. Second, notice that another AND gate has been added. The intersection of the input terms and product lines form a 4 X 2 AND array.

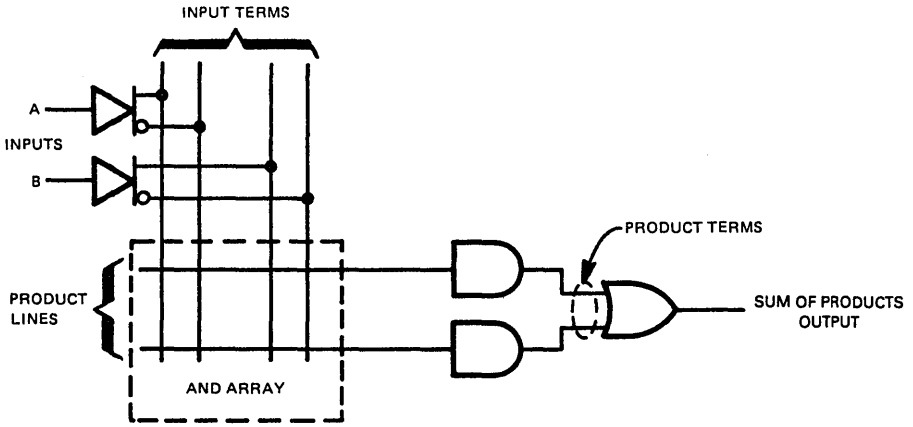

FIGURE 3

Third, the product terms of the AND gates are summed with an OR gate. The output function is now the sum of products of the input lines.

To make the structure in Figure 3 useful, provisions must be made to program the AND array. Programming is done by means of fusable TiW links. A fuse is located between the input term and the actual input to the AND gate (see Figure 4). In our special array symbology, a fuse is visualized to exist at each intersection of the input terms and product lines.

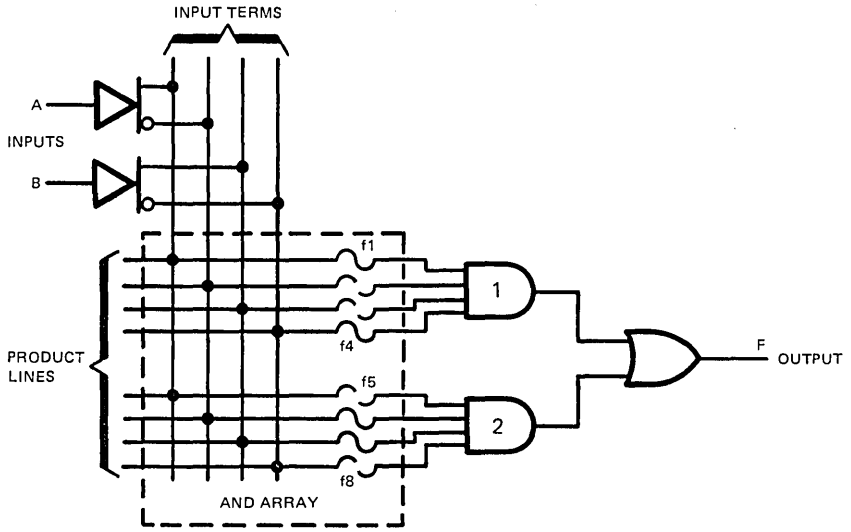

FIGURE 4

Now we can express the output function F in terms of the inputs. Notice that fuses f2, f3, f5, and f8 have been blown and A and $\overline{B}$ are still connected to AND gate #1 through fuses f1 and f4. Likewise, $\overline{A}$ and B are connected to AND gate #2 through fuses f6 and f7. The output can now be expressed as $F = A\overline{B} + \overline{A}B$.

A compact representation of the unprogrammed version of Figure 4 using the rules explained in Section 6 of this data book is shown in Figure 5.

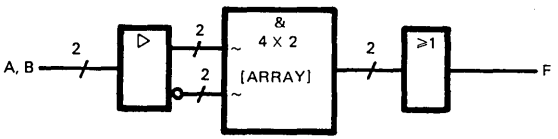

FIGURE 5

Figure 6 will further show how the function $F = A\overline{B} + \overline{A}B$ is represented in our array symbology and will present the convention used to show the fuse states in a programmed array. This convention simply places an X at the intersection of each input term and product line for which an intact fuse is required. Blown fuses will be represented by the absence of an X at the appropriate intersection.

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Unused product lines, where all fuses are left intact, can be noted with an X in the AND symbol. This product term will always be inactive (i.e., have no affect on any sum term in which it appears). If all fuses are blown on a product line, the output containing this product term will be disabled (i.e., forced high). Exercise care in programming to avoid this condition.

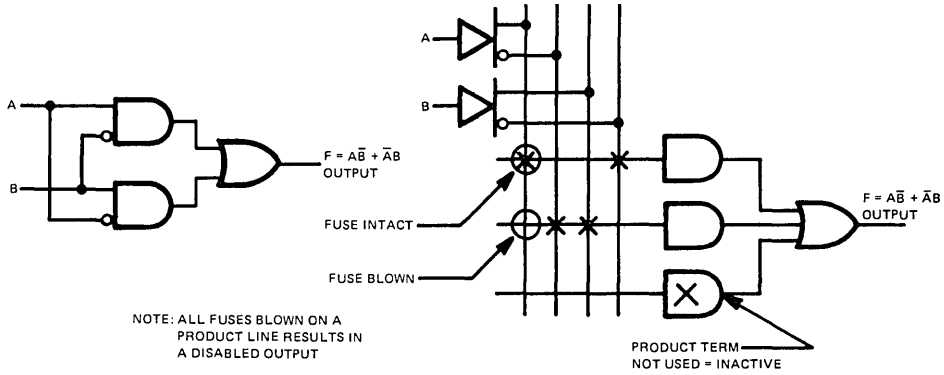

FIGURE 6

The symbology is further extended to include the two-array circuit structure, which is the basic Field-Programmable Logic architecture. Figure 7 is a two-array logic diagram. In earlier examples, the AND gates were summed in a single OR gate. In the two-array structure, the AND gate outputs enter a programmable OR array. The OR array allows any product term to be included in the sum term of any output or in all outputs.

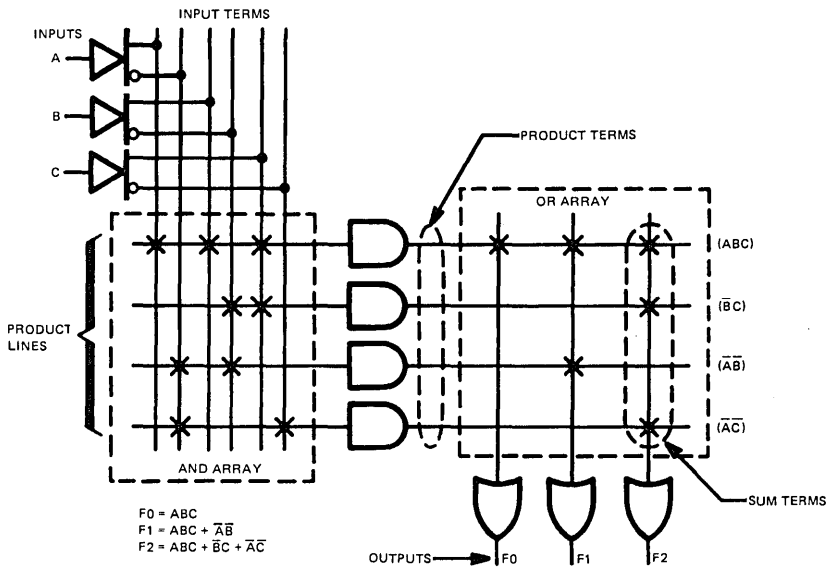

FIGURE 7

All of the Field Programmable Logic circuits described in this data book are variations of the two-array architecture. Variations will include output registers, internal feedback, feedback registers, and fixed OR arrays. Figures 8, 9, and 10 represent simplified versions of three specific families of Field-Programmable Logic.

FIELD-PROGRAMMABLE LOGIC ARRAY (FPLA)

The basic two-array structure developed in the symbology section is more commonly referred to as a *Field-Programmable Logic Array*. A useful addition to this structure would be an output-enable function as shown in the generalized FPLA diagram below.

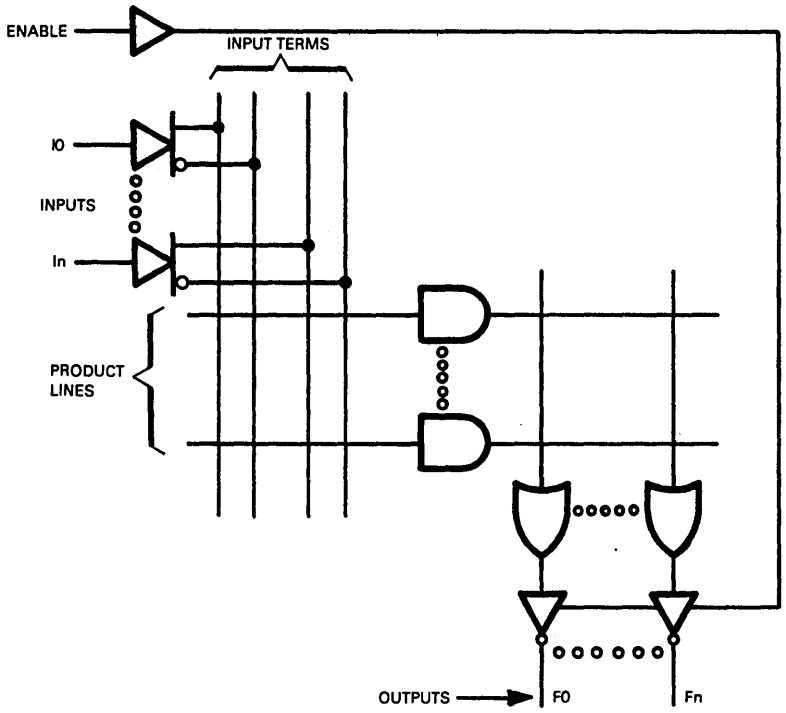

FIGURE 8

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FIELD-PROGRAMMABLE LOGIC SEQUENCER (FPLS)

Field-Programmable Logic Sequencers (FPLS) are designed to solve state-machine problems of the Mealy type. Based on the FPLA structure, they include flip-flop elements in feedback paths between the OR and AND arrays as shown in Figure 9. These flip-flop elements can be of the D type or J-K type. Logic levels from the OR array can also be stored in flip-flop elements in each output.

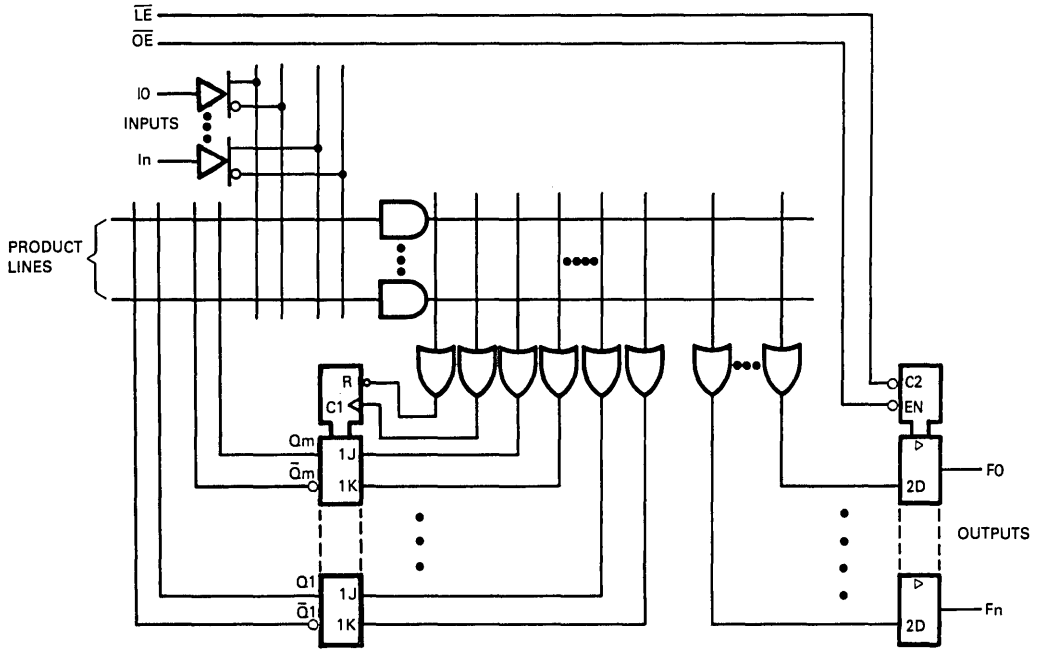

FIGURE 9

FIXED-OR ARRAYS (FOA)

The *Fixed-OR Array* is a special case of the FPLS that is capable of solving Mealy-type state-machine problems. The FOA does not have a Programmable-OR Array. Product terms are partitioned and allocated to specific outputs. All product terms allocated to an output are summed with a single OR gate. Output feedback, as well as registered inputs and outputs, are added to the structure to increase logic utility. Figure 10 includes generalized diagrams of various FOA structures.

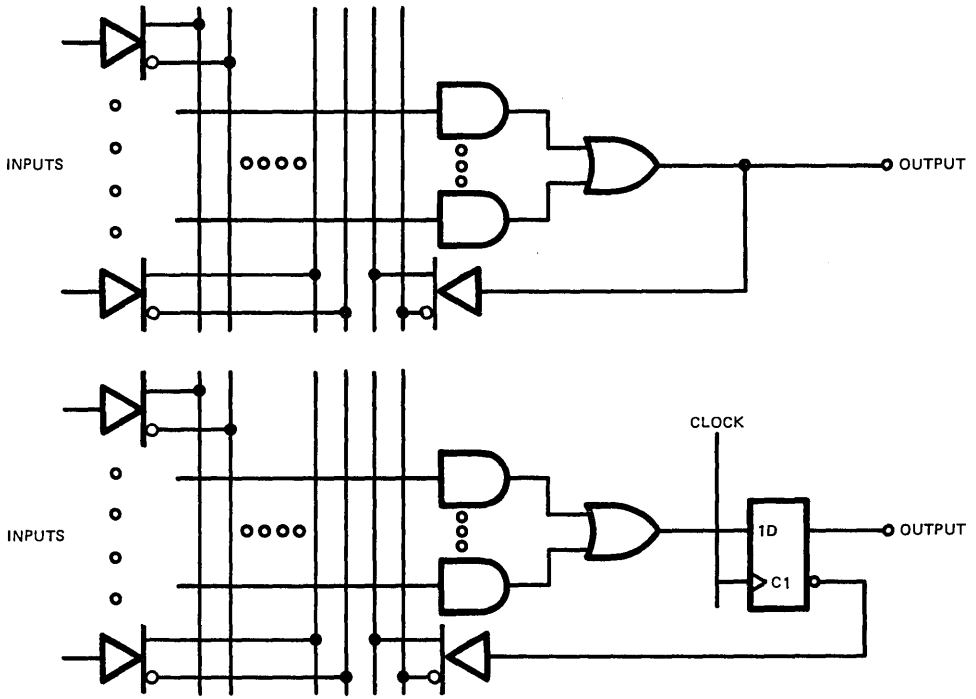

FIGURE 10

DESIGNING WITH FIELD-PROGRAMMABLE LOGIC ARRAYS

The basic logic implementation of Field-Programmable Logic devices is the previously developed AND-OR array. Additions to this structure provide unique functional capabilities. This section will review these logic structures.

INPUTS

All data inputs are configured to provide both true and complement components to the AND array. These inputs are either buffered or registered. Control pins also exist for enable and clock functions.

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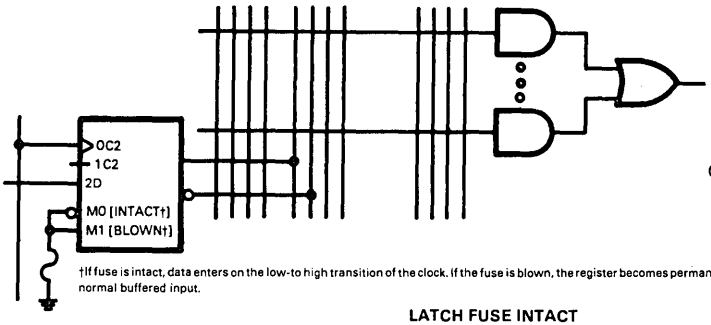
The normal array input is through a buffer with true and complement outputs of the buffer made available to each product line through a TiW fuse.

Some device types in the Field-Programmable Logic family have programmable latched inputs. With the latch fuse intact, the input acts as an edge-triggered D-type register or transparent latch depending on device type. The true and complement outputs of the input latch are made available to each product line through a latch fuse. With the latch fuse blown, the input latch is converted into a normal buffered input (see Figure 11).

REGISTER FUSE INTACT



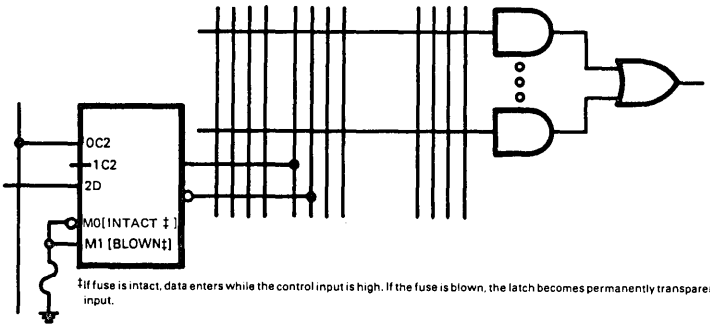
D-TYPE REGISTER FUNCTION TABLE

CLOCK	D	Q	$\overline{Q}$
↑	H	H	L
↑	L	L	H
L	X	Q_0	$\overline{Q}_0$

Q_0 = THE STATE OF Q BEFORE CLOCK ↑

†If fuse is intact, data enters on the low-to high transition of the clock. If the fuse is blown, the register becomes permanently transparent and is equivalent to a normal buffered input.

LATCH FUSE INTACT



TRANSPARENT LATCH FUNCTION TABLE

ENABLE	D	Q	$\overline{Q}$
H	L	L	H
H	H	H	L
L	X	Q_0	$\overline{Q}_0$

Q_0 = THE LEVEL OF Q BEFORE ENABLE ↓

‡If fuse is intact, data enters while the control input is high. If the fuse is blown, the latch becomes permanently transparent and is equivalent to a normal buffered input.

REGISTER/LATCH FUSE BLOWN

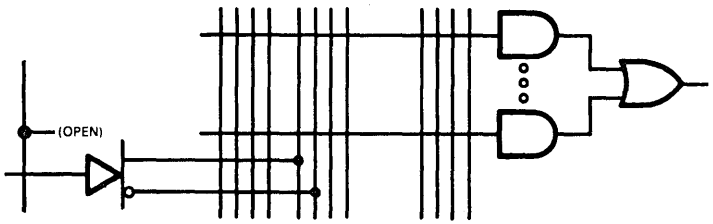


FIGURE 11

CONTROL PINS

Clock and latch-enable pins allow external control of input and output latches. Output enable controls the operation of the registered three-state outputs.

OUTPUTS

Various output configurations provide a design flexibility not previously available to the designer using catalog logic.

- PROGRAMMABLE I/O - The combinational output of the FOA incorporates 3-state drivers if the enable function is logically controlled by the AND array (see Figure 12). This allows the output to be programmed as an input, an output, or logic-controlled I/O.

- 3-STATE OUTPUTS - The FPLA and FPLS have output enable pins available for 3-state control, and the registered outputs of the FOA are controlled by a common output enable. Three-state control of the combinational outputs of the FOA is accomplished through programming as described earlier.

PROGRAMMABLE 3-STATE OPERATION
ALL FUSES BLOWN . . . NORMAL OUTPUT
ALL FUSES INTACT . . . OUTPUT IN HIGH-Z STATE
FUSES SELECTED . . . PROGRAMMED I/O

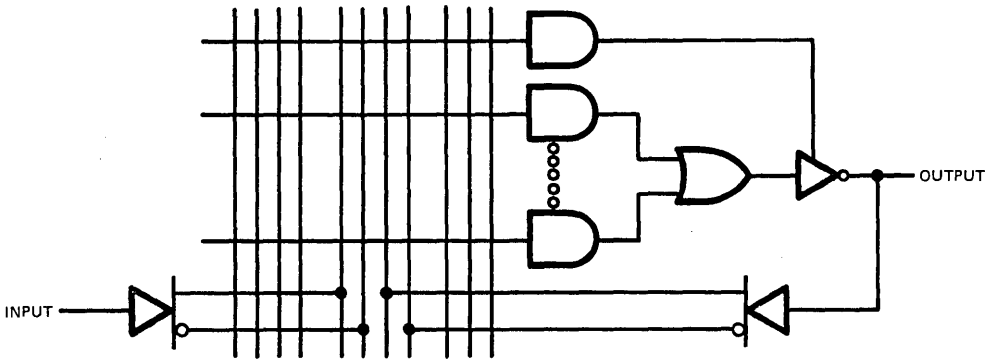


FIGURE 12

- REGISTERED OUTPUTS - The FPLS and some FOA's have latches on their outputs. The FPLS has a transparent latch on each of its 6 outputs. The output function levels are stored by a common asynchronous latch enable pin $\overline{LE}$.

TRANSPARENT LATCH
FUNCTION TABLE

$\overline{LE}$	D	Q
L	L	L
L	H	H
H	X	Q_0

Q_0 = THE LEVEL OF Q BEFORE $\overline{LE}$ ↑

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The output (D) latch on the FOA stores output levels with a low-to-high transition of the clock. This structure also provides feedback of Q through a true and complement buffer to the Programmable AND array.

- OPEN-COLLECTOR OUTPUTS - Some devices have open-collector outputs available. These outputs may be wire-ANDed (active-high) or wire-ORed (active-low). This feature requires no external logic, which would add to the component count and propagation delay.

- POLARITY SELECT - Circuitry provides a polarity select fuse for each FPLA output. The function of these fuses is shown in Figure 13.

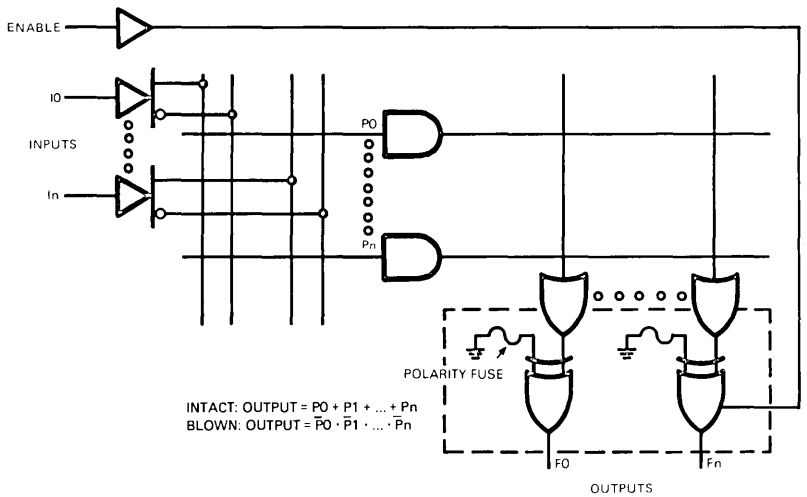
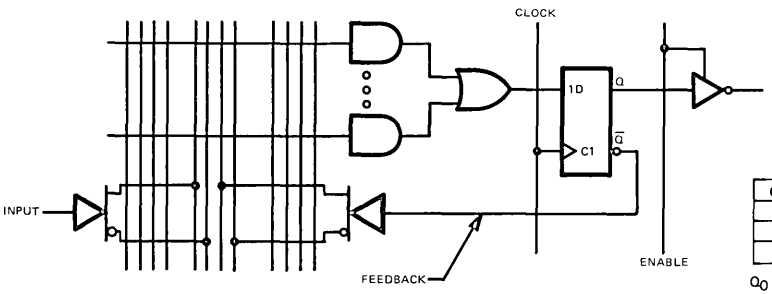


FIGURE 13

FEEDBACK PATHS

The $\overline{Q}$ feedback of the output register of the FOA (see Figure 14), provides the basis for implementing sequential functions. The FPLS (Figure 15), is designed to solve state-machine problems of the Mealy type. It contains four J-K flip-flops completely buried in the feedback path between the OR and AND arrays.



D-TYPE REGISTER FUNCTION TABLE

CLOCK	D	Q	$\overline{Q}$
↑	H	H	L
↑	L	L	H
L	X	Q_0	$\overline{Q}_0$

Q_0 = THE LEVEL OF Q BEFORE CLOCK ↑

FIGURE 14

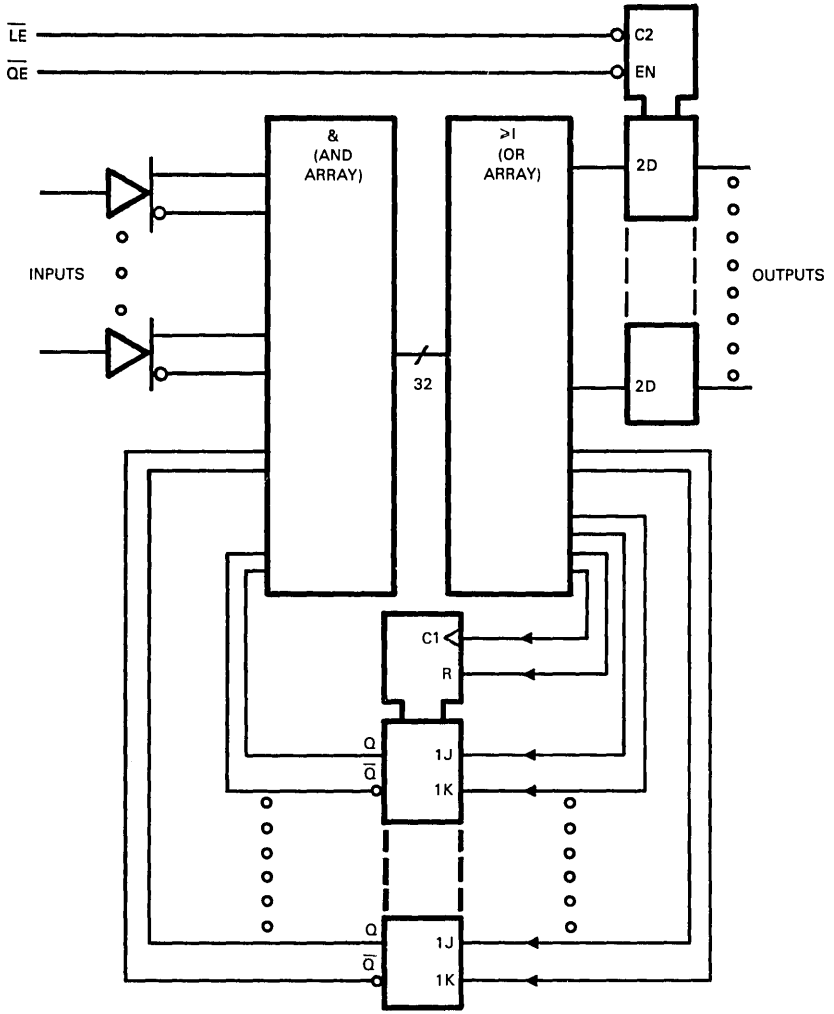


FIGURE 15

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LOGIC BLOCK EQUIVALENCE

Now that the individual circuit functions have been discussed, we will review the implementation of each of the basic logic functions (AND, OR, NAND, NOR, and exclusive OR). Figure 16 presents a comparison of basic logic function, the logical equivalent, and the implementing logic diagram for a nonregistered output.

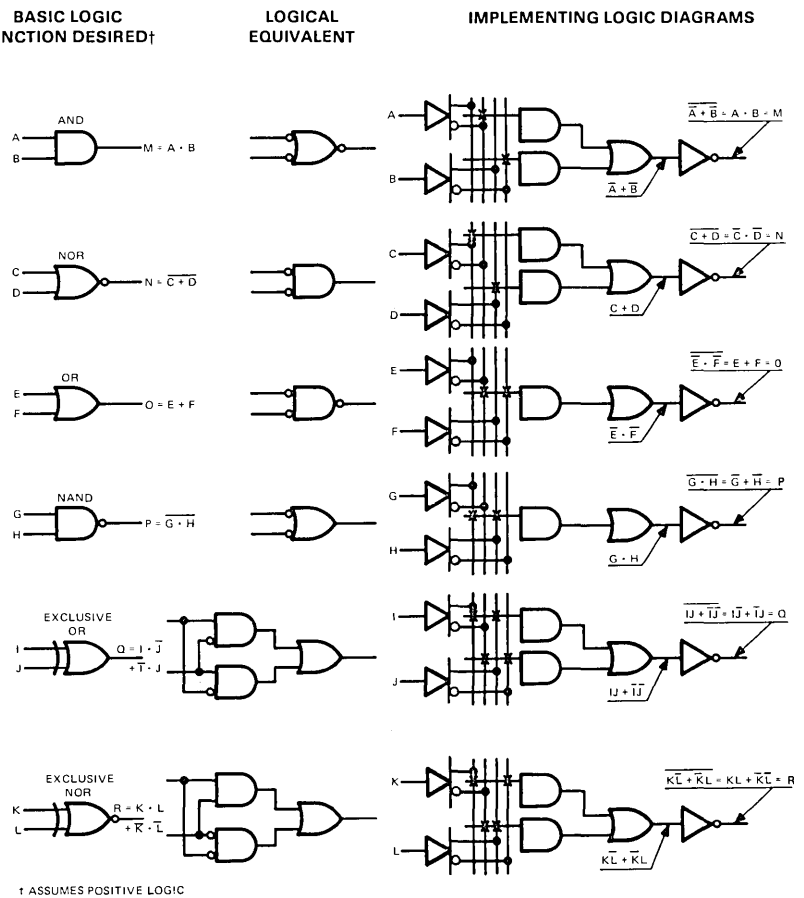

FIGURE 16. COMPARISON OF BASIC LOGIC FUNCTIONS

REFERENCE INFORMATION

Comprehensive comparisons of Low-Power Schottky (LS), Advanced Schottky (AS), and Advanced Low-Power Schottky (ALS), as well as details for circuit design, are presented in our Application Report Number B215, "Series 54ALS/74ALS Schottky TTL." Application Report B215, used in conjunction with the data sheets for the specific device, will allow confident designing with Field-Programmable Logic.

PROGRAMMING FIELD-PROGRAMMABLE LOGIC

Each device data sheet includes a programming procedure that defines the conditions for programming. Programmers are commercially available for most devices with equipment for future devices in development. Listed below are the manufacturers of programming equipment.

- Cybernetic PGM Systems
- Data I/O
- Kentron
- Pro-Log
- Stag Systems
- Structured Design
- Curtis Electro Devices

Device design has been coordinated with Data I/O and their Model 19 has been used throughout design and characterization. Therefore, the Model 19 with appropriate programming pack and socket adapter is presently the only certified programmer.

Programming FPLAs and FPLSs is largely manual. Computer-controlled programming capability currently exists for 20-pin Fixed-OR Arrays. Control is by means of Fortran IV computer software, which is included later in this data book. Software for 24-pin Fixed-OR Arrays is under development and will be included in later application notes.

PREPARATION AND PROGRAMMING

Regardless of the type of equipment to be used for actually programming devices (blowing fuses), the basic design and programming requirements are the same. Figure 17 presents a simplified flow chart of programming options.

Since the Fixed-OR Array affords the widest variety of parts and output options, it will be used for both the manual and computer-aided examples. First, we will describe the circuit selected for the example, then discuss the specific steps required prior to programming the parts.

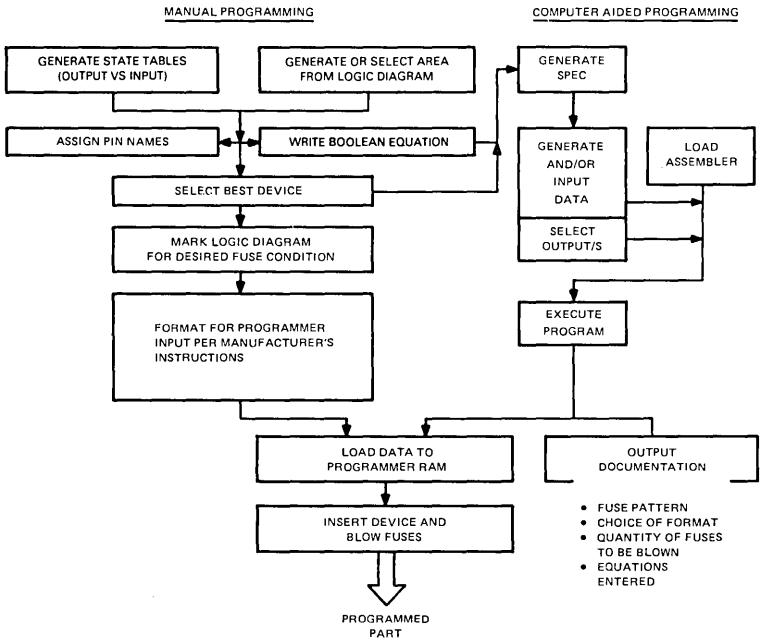

FIGURE 17. SIMPLIFIED FLOW CHART OF PROGRAMMING OPTIONS

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PROGRAMMED EXAMPLE

Figure 18 is a partial schematic of the decoding portion of a commercially used video controller as implemented with standard catalog SSI logic. Circuit analysis reveals that this circuit is primarily a waveform generator designed to decode the state of the 5-bit counter. The edge-triggered latches are clocked and cleared with respect to the clock (CK) input. Figure 19 is the timing diagram generated to establish the individual waveforms. The labeling defined in the legend of Figure 18 will help understand the partitioning used to implement this circuit using Fixed-OR-Arrays. Most of the original circuit can be implemented by a direct function for function conversion, however, some rearrangement is required to take full advantage of the flexibility of the Fixed-OR-Arrays. Since the FOA has a common clock and no clear, $\overline{I}$ must be developed as shown in Figure 20.

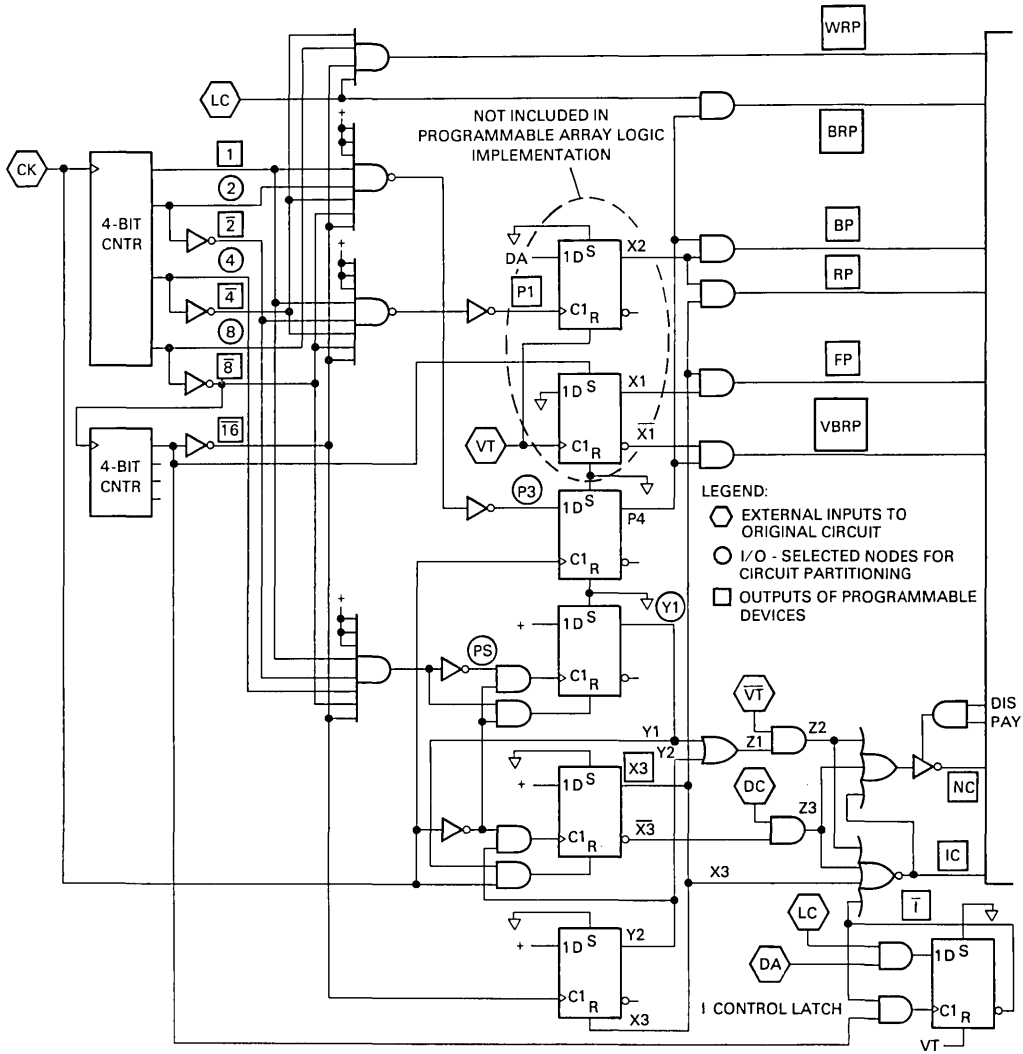

FIGURE 18. DECODING PORTION OF VIDEO CONTROLLER WITH STANDARD CATALOG LOGIC

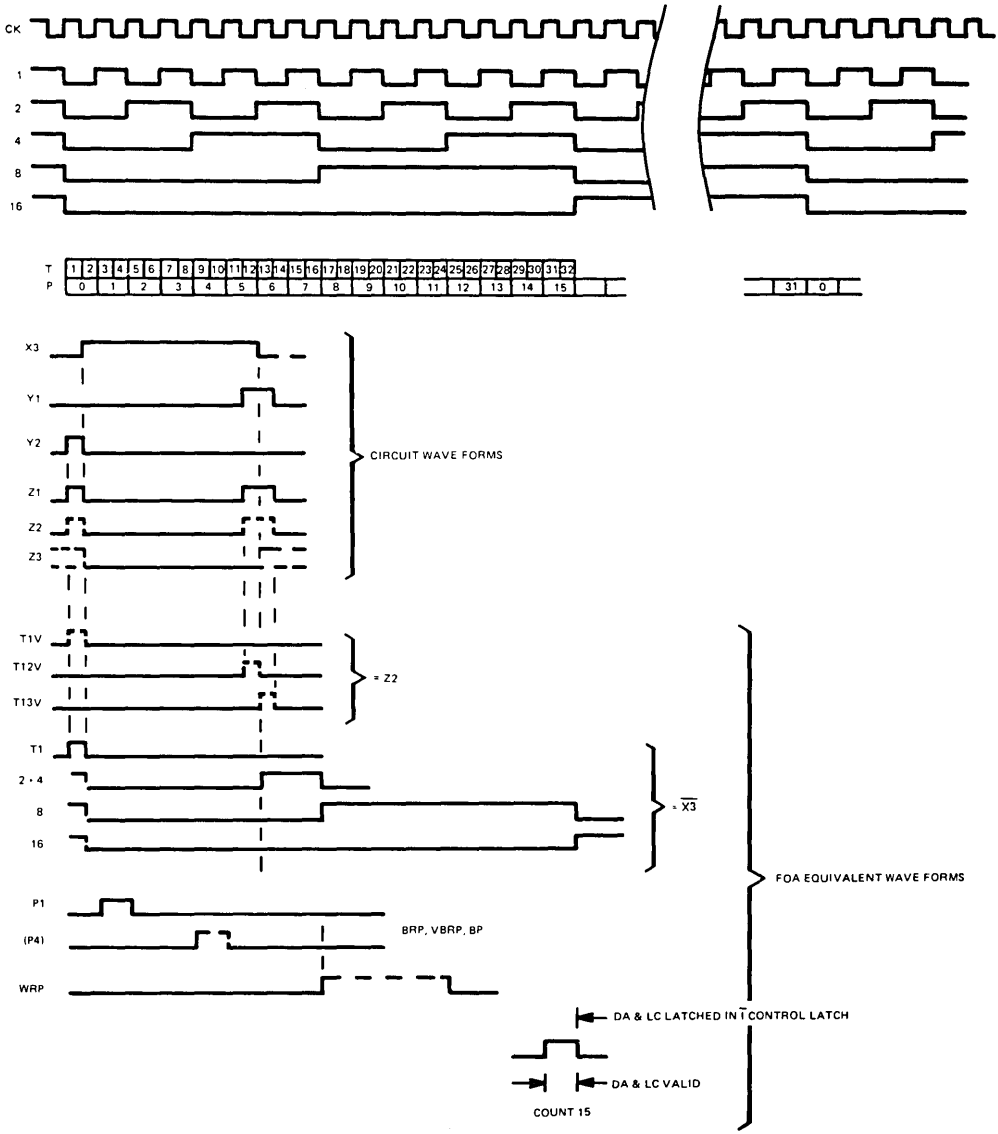

FIGURE 19. TIMING DIAGRAM FOR VIDEO CONTROLLER (SEE FIGURE 18)

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By partitioning the circuit as shown in Figure 18, a pin assignment can be made and the most suited Fixed-OR Array selected. In this example, the 'PL16R6 and 'PL16L8 have been selected. The logic diagram for the equivalent circuit as implemented using the selected devices are shown in Figure 20 and Figure 21 respectively. Figure 22 presents the detailed schematic of the counter. The counter implementation is a part of the 'PL16R6 represented in Figure 20. Figure 21 is included only to complete the conversion example (programming is not shown). The combination of (1) feedback buffers as inputs with true and complement, (2) input true and complement, (3) common clock for D latches and the selectable use of each input allows the entire circuit shown in Figure 18 (excluding the one device circled) to be replaced by two array-logic devices. This results in a part count reduction of 17 to 2 (88%) and an interconnect reduction of 83% plus the reduction in printed circuit board complexity and area.

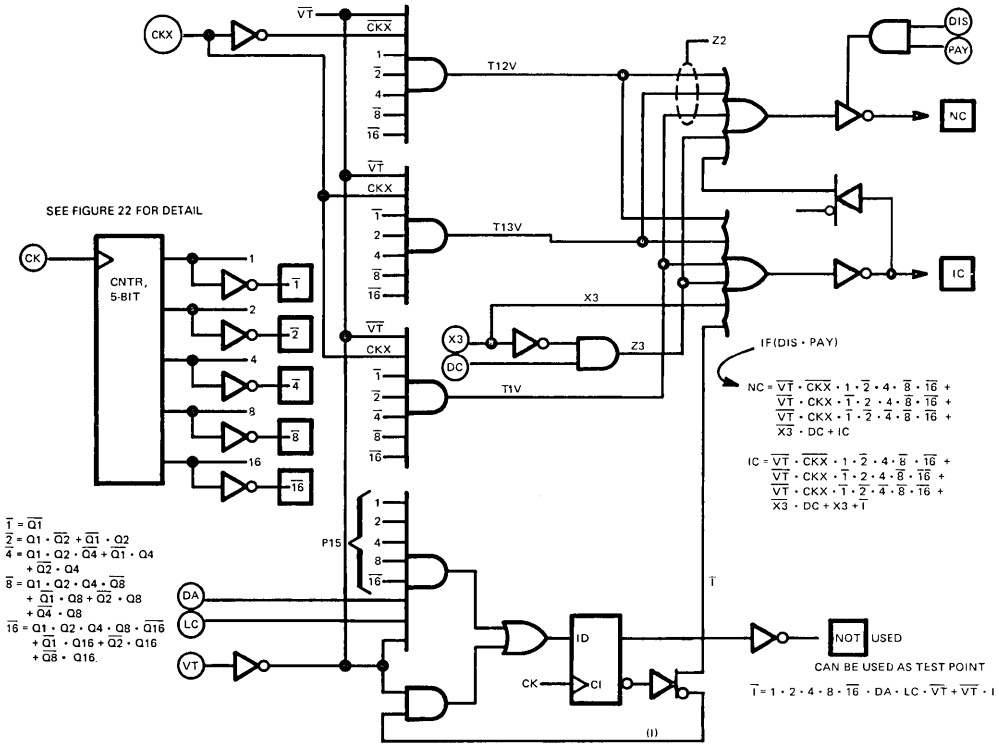

FIGURE 20. VIDEO CONTROLLER IMPLEMENTATION, DECODE NUMBER 1 FOR 'PL16R6

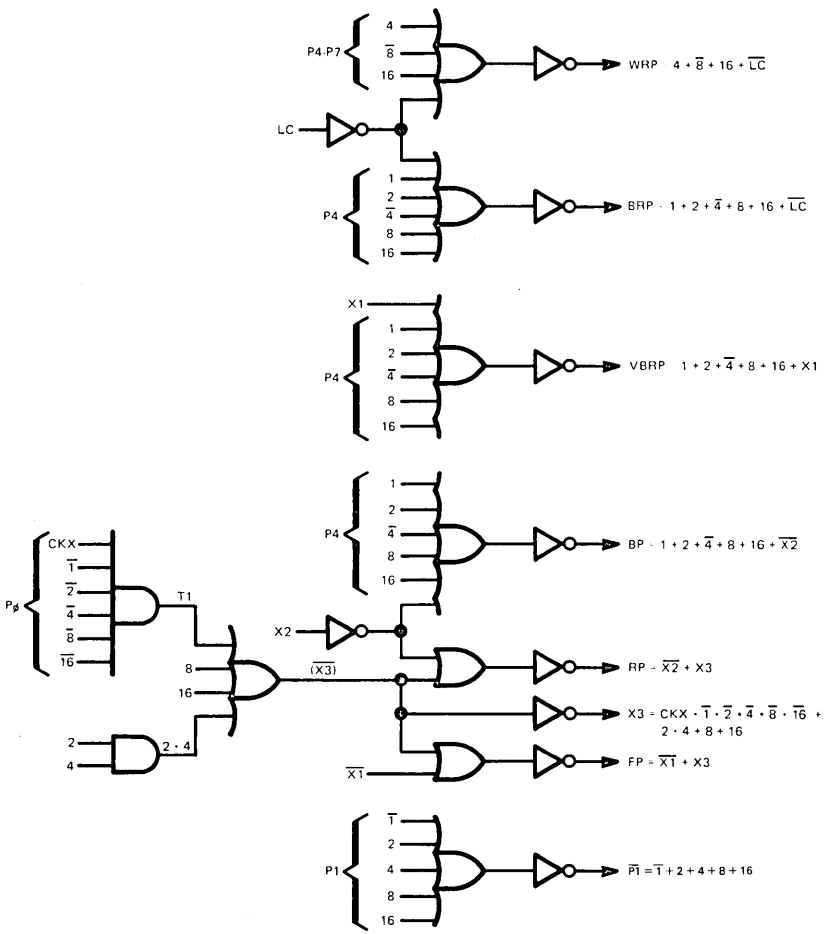

FIGURE 21. VIDEO CONTROLLER IMPLEMENTATION, DECODE NUMBER 2 FOR 'PL16L8

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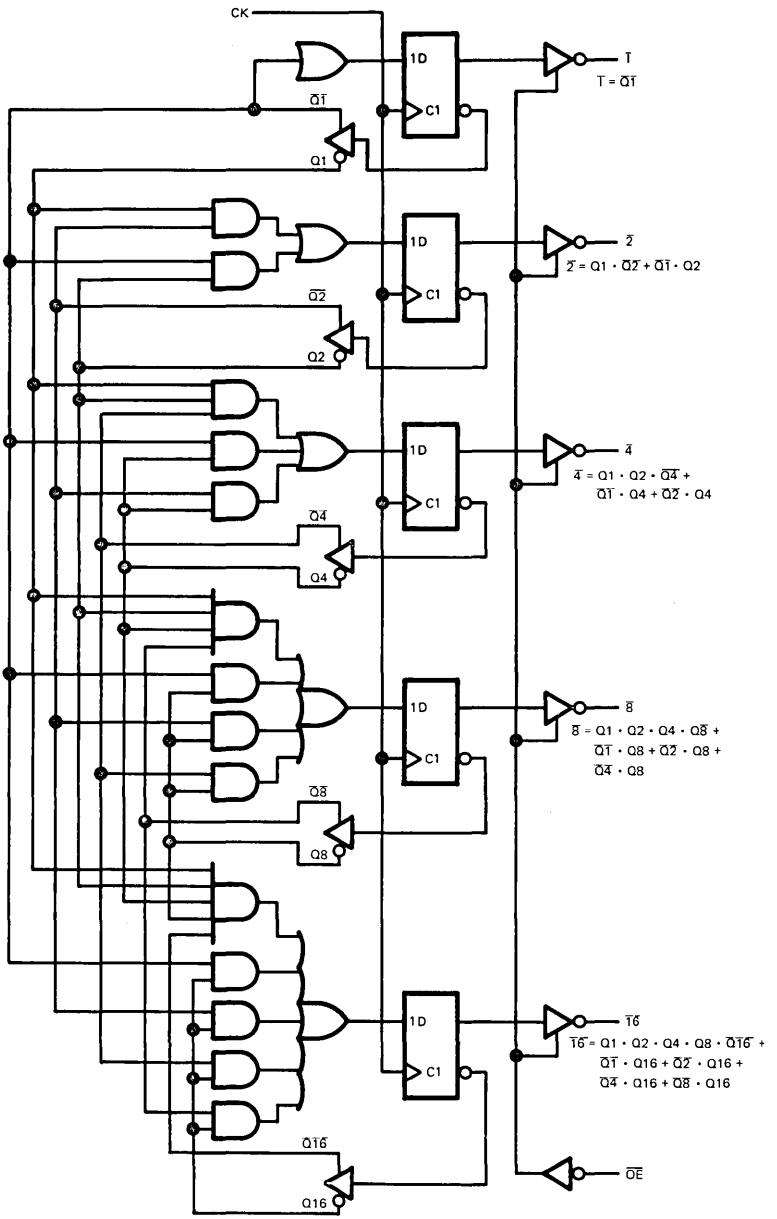

FIGURE 22. FIXED-OR ARRAY 5-BIT COUNTER IMPLEMENTATION

MANUAL PROGRAMMING EXAMPLE

Now that logic equations have been generated in Figure 20 and Figure 21 as a result of the analysis and restructuring of the circuit implementation, we are ready to prepare for programming the devices as follows:

1. Take a copy of the logic diagram for the selected device (see Figure 23).
2. Label each output.
3. Assign names to each input. In Figure 20 the inputs are circled and the outputs enclosed by a square.
4. Mark the location of each fuse required to implement the equations. Note that all inputs to the array for outputs $\overline{1}$ through $\overline{16}$ are from the feedback buffers. Example: $\overline{2}$ on pin 17 is fed back to input lines 10 and 11.

To implement the equation $\overline{2} = Q1 \cdot \overline{Q2} + \overline{Q1} \cdot Q2$, place an X at the intersection of

INPUT LINE	PRODUCT LINE
7($Q1$)	16
10($\overline{Q2}$)	16
6($\overline{Q1}$)	17
11($Q2$)	17

NOTE: The inputs DIS and PAY are not on the original schematic. They have been used here to demonstrate (1) the simplicity of programming for three-state control, (2) the IF statement for the computer-aided program, and (3) the device versatility.

5. The preparation for programming the device is now complete except for formatting the fuse locations to comply with the input requirement of a particular programmer. Since equipment manufacturers have not yet standardized on address and data input formats, refer to the programming instructions for your particular programmer.

COMPUTER-AIDED PROGRAMMING EXAMPLE

Programmers are available with interface packages that will allow the simplification of inputting data. Options vary from the ability to output from paper tape to direct terminal or computer control. Many data formats are also available for the remote controlled programmers. Examples of acceptable formats include HEX, BHLF, and BPNP.

The equations, part number, and pin assignment shown in Figure 20 (same used in manual programming example) are the only requirements for the computer program to generate the fuse pattern for our example as shown in Figure 26. However, a specification such as shown in Figure 25 is recommended not only to assist in inputting data but as a documentation tool to identify and describe the unique part created by programming. Examples of HEX and BLHF output formats are also included in Figure 26. Source code is provided after this example.

NOTE: Since the programming results cannot be verified after the security fuses are blown, a separate test fixture is required to blow these two fuses (see the data sheet for instructions).

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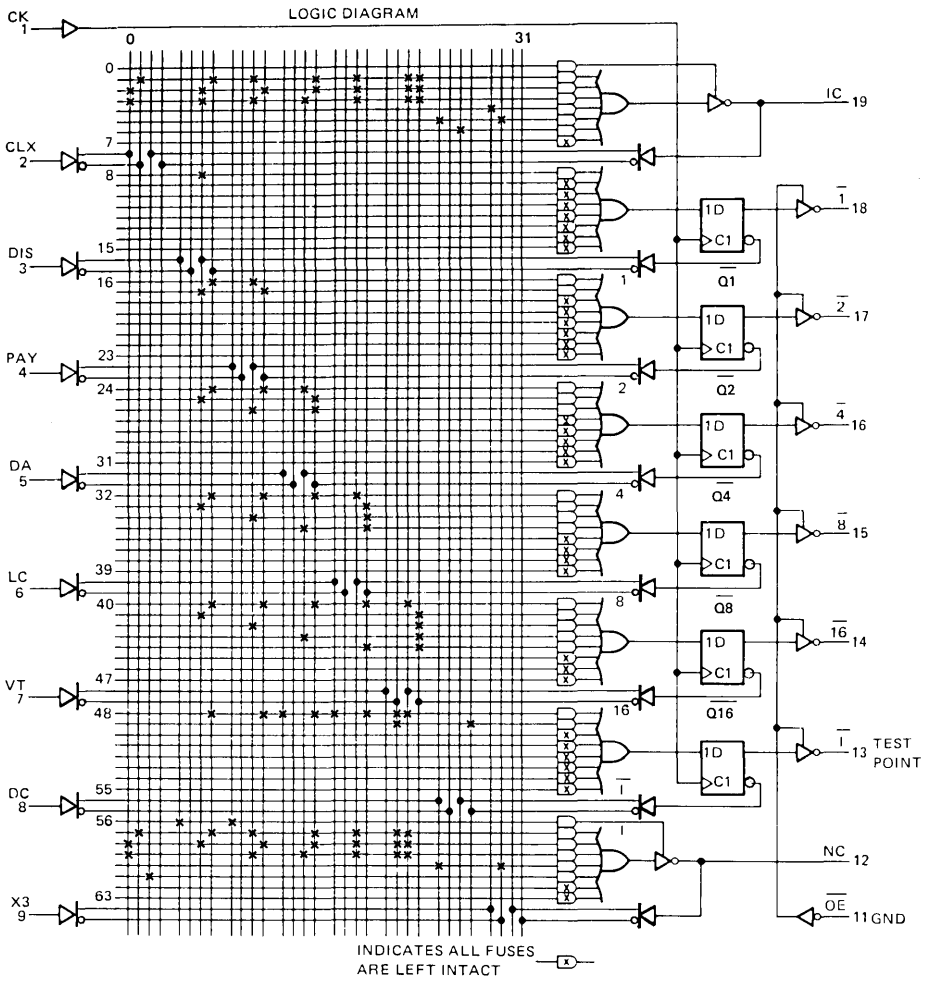

FIGURE 23. 'PL16R6 LOGIC DIAGRAM

COMPUTER-AIDED PROGRAMMING FOR 20-PIN FIXED-OR ARRAYS

The source program (requires a Fortran IV compiler) beginning on this page will produce an object program for translating specifications and Boolean equations into a hard-copy fuse map. The output is formatted for direct input to PROM programmers. A specification sheet completed according to the instructions below is given in the example.

- Device part number — 7 characters of which the last 4 must correspond to the part being programmed. Part number must be in column one of line one.
- Pin assignment — each of the 20 pins must be assigned a symbolic name. Each pin name must be separated by one or more spaces starting on line 5.
- Logic equations — the logic equations start on the first line following the pin assignments.

Recognized operators:

=	Equality
/	Complement
*	Product (AND)
+	Sum (OR)
()	Logic statement within parenthesis that must be true to enable output
:=	May be used in place of "equality" (=) to indicate "replaced by after clock"

Equation formats (blanks in the equation will be ignored).

O1 = I1 * I2 + I3	combinational logic
O2 := I2 + I3 * I4	registered logic
If (I4 * O2) O3 = I5 */I3 + I7	three-state control

****

COMPUTER-AIDED PROGRAM SPECIFICATIONS AND OUTPUTS FOR DECODE #1 (SEE FIGURE 20)

SPECIFICATION SHEET

PL16R6 — TI DESGN GP
PAT 0001 — APL GP 04/14/82
DECODE #1

```
CK CKX DIS PAY DA LC VT DC X3 GND /OE NC /I /16 /8 /4 /2 /1 IC VCC
IC =    /VT*/CKX*1*/2*4*/8*16+
        /VT*CKX*/1*2*4*/8*/16+
        /VT*CKX*/1*/2*/4*/8*/16+
        /X3*DC + X3 + /I
/1 =    /1
/2 =    1*/2 + /1*2
/4 =    1*2*/4 + /1*4 + /2*4
/8 =    1*2*4*/8 +/1*8 + /2*8 + /4*8
/16 =   1*2*4*8*/16 + /1*16 + /2*16 + /4*16 + /8*16
/I =    1*2*4*8*/16*DA*LC*/VT + /VT*I
IF(DIS*PAY)NC =     /VT*/CKX*1*/2*4*/8*/16+          Conditional Statement - three state
                    /VT*CKX*/1*2*4*/8*/16+
                    /VT*CKX*/1*/2*/4*/8*/16+
                    /X3*DC + IC
```

DESCRIPTION: 5 BIT COUNTER W/DECODE

****

X-PLOT
DECODE #1 XXXXXX *If the programmed part number is input as a part of the title, it will appear here.*

LEGEND: X = Fuse not blown - = Fuse blown

```
                 11 1111 1111 2222 2222 2233
   0123 4567 8901 2345 6789 0123 4567 8901

 0 ---- ---- ---- ---- ---- ---- ---- ----
 1 -X-- ---X --X- ---X --X- -X-X ---- ---- /VT*/CKX*1*/2*4*/8*16
 2 X--- --X- ---X ---X --X- -XX- ---- ---- /VT*CKX*/1*2*4*/8*/16
 3 X--- --X- --X- --X- --X- -XX- ---- ---- /VT*CKX*/1*/2*/4*/8*/16
 4 ---- ---- ---- ---- ---- ---- X--- -X-- /X3*DC
 5 ---- ---- ---- ---- ---- ---- ---- X--- X3
 6 ---- ---- ---- ---- ---- ---- --X- ---- /I
 7 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

 8 ---- --X- ---- ---- ---- ---- ---- ---- /1
 9 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
10 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
11 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
12 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
13 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
14 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
15 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

16 ---- ---X --X- ---- ---- ---- ---- ---- 1*/2
17 ---- --X- ---X ---- ---- ---- ---- ---- /1*2
18 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
19 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
20 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
21 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
22 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
23 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

24 ---- ---X ---X --X- ---- ---- ---- ---- 1*2*/4
25 ---- --X- ---- ---X ---- ---- ---- ---- /1*4
26 ---- ---- --X- ---X ---- ---- ---- ---- /2*4
27 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
28 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
29 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
30 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
31 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
```


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```
32 ---- ---X ---X ---X --X- ---- ---- ---- 1*2*4*/8
33 ---- --X- ---- ---- ---X ---- ---- ---- /1*8
34 ---- ---- --X- ---- ---X ---- ---- ---- /2*8
35 ---- ---- ---- --X- ---X ---- ---- ---- /4*8
36 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
37 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
38 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
39 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

40 ---- ---X ---X ---X ---X --X- ---- ---- 1*2*4*8*/16
41 ---- --X- ---- ---- ---- ---X ---- ---- /1*16
42 ---- ---- --X- ---- ---- ---X ---- ---- /2*16
43 ---- ---- ---- --X- ---- ---X ---- ---- /4*16
44 ---- ---- ---- ---- --X- ---X ---- ---- /8*16
45 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
46 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
47 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

48 ---- ---X ---X X--X X--X -XX- ---- ---- 1*2*4*8*/16*DA*LC*/VT
49 ---- ---- ---- ---- ---- -X-- ---X ---- /VT*I
50 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
51 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
52 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
53 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
54 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
55 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

56 ---- X--- X--- ---- ---- ---- ---- ---- DIS*PAY
57 -X-- ---X --X- ---X --X- -XX- ---- ---- /VT*/CKX*1*/2*4*/8*/16
58 X--- --X- ---X ---X --X- -XX- ---- ---- /VT*CKX*/1*2*4*/8*/16
59 X--- --X- --X- --X- --X- -XX- ---- ---- /VT*CKX*/1*/2*/4*/8*/16
60 ---- ---- ---- ---- ---- ---- X--- -X-- /X3*DC
61 --X- ---- ---- ---- ---- ---- ---- ---- IC
62 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
63 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
```

EXAMPLE OF HEX FORMAT
DECODE #1

```
F F F F F F D 3 F F B 7 F F 7 F F F F F F F F F F F F F F F F .
D C D D D D 1 C D D C 9 D D D 4 D D C D D C D C D D D D D D D D .
8 9 9 9 9 9 8 9 9 9 1 8 9 9 9 0 9 9 8 9 9 8 8 9 9 9 9 9 9 9 9 9 .
0 1 1 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 0 0 1 1 1 1 1 1 1 1 1 .
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 0 1 1 .
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 .
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
F F F F 7 F F 8 7 F F 8 B F F 8 B F E 9 F B 9 F F F F F F F F F .
F 7 F F F F C 7 F F 7 F F F F 7 F F 7 E F 3 7 D F F F B F F F F .
3 B B B B B 3 B B B 8 3 B B B 3 B B 3 A B 3 3 9 B B B B B B B B .
3 B B B B B 3 B B B 3 B B B 0 B B 3 B A B 3 3 9 B B B B B B B B .
A A A A A A A A A A A A A A A A A A 8 A A A A 8 2 A A A A 2 A A .
8 0 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
```

EXAMPLE OF BHLF FORMAT
DECODE #1

Legend:
- B = Begin data field
- H = High logic level
- L = Low logic level
- F = End data field

```
BHHHHFBHHHHFBHHHHFBHHHHFBHHHHFBHHHHFBHHLHFBLLHHF
BHHHHFBHHHHFBHLHHFBLHHHFBHHHHFBHHHHFBLHHHFBHHHHF
BHHHHFBHHHHFBHHHHFBHHHHFBHHHHFBHHHHFBHHHHFBHHHHF
BHHHHFBHHHHFBHHHHFBHHHHFBHHHHFBHHHHFBHHHHFBHHHHF
BHHLHFBHHLLFBHHLHFBHHLHFBHHLHFBHHLHFBLLLHFBHHLLF
BHHLHFBHHLHFBHHLLFBHLLHFBHHLHFBHHLHFBHHLHFBLHLLF
BHHLHFBHHLHFBHHLLFBHHLHFBHHLHFBHHLLFBHHLHFBHHLLF
BHHLHFBHHLHFBHHLHFBHHLHFBHHLHFBHHLHFBHHLHFBHHLHF
BHLLLFBHLLHFBHLLHFBHLLHFBHLLHFBHLLHFBHLLLFBHLLHF
BHLLHFBHLLHFBLLLHFBHLLLFBHLLHFBHLLHFBHLLHFBLLLLF
BHLLHFBHLLHFBHLLLFBHLLHFBHLLHFBHLLLFBHLLLFBHLLHF
BHLLHFBHLLHFBHLLHFBHLLHFBHLLHFBHLLHFBHLLHFBHLLHF
BLLLLFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHFBLLLLFBLLLHF
BLLLHFBLLLHFBLLLLFBLLLHFBLLLHFBLLLHFBLLLLFBLLLHF
BLLLHFBLLLHFBLLLLFBLLLHFBLLLHFBLLLLFBLLLLFBLLLHF
BLLLHFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHF
BLLLHFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHF
BLLLHFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHF
BLLLHFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHF
BLLLLFBLLLHFBLLLHFBLLLHFBLLLLFBLLLHFBLLLHF
BLLLHFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHF
```


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```
BLLLHFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHF
BLLLHFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHF
BLLLHFBLLLHFBLLLHFBLLLHFBLLLLFBLLLHFBLLLHFBLLLHF
BLLLHFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHF
BLLLHFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHF
BLLLHFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHF
BLLLHFBLLLHFBLLLLFBLLLHFBLLLHFBLLLHFBLLLHFBLLLHF
BLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLF
BLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLF
BLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLF
BLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLF
BHHHHFBHHHHFBHHHHFBHHHHFBLHHHFBHHHHFBHHHHFBHLLLF
BLHHHFBHHHHFBHHHHFBHLLLFBHLHHFBHHHHFBHHHHFBHLLLF
BHLHHFBHHHHFBHHHLFBHLLHFBHHHHFBHLHHFBHLLHFBHHHHF
BHHHHFBHHHHFBHHHHFBHHHHFBHHHHFBHHHHFBHHHHFBHHHHF
BHHHHFBLHHHFBHHHHFBHHHHFBHHHHFBHHHHFBHHLLFBLHHHF
BHHHHFBHHHHFBLHHHFBHHHHFBHHHHFBHHHHFBHHHHFBLHHHF
BHHHHFBHHHHFBLHHHFBHHHLFBHHHHFBLLHHFBLHHHFBHHLHF
BHHHHFBHHHHFBHHHHFBHLHHFBHHHHFBHHHHFBHHHHFBHHHHF
BLLHHFBHLHHFBHLHHFBHLHHFBHLHHFBHLHHFBLLHHFBHLHHF
BHLHHFBHLHHFBHLLLFBLLHHFBHLHHFBHLHHFBHLHHFBLLHHF
BHLHHFBHLHHFBLLHHFBHLHLFBHLHHFBLLHHFBLLHHFBHLLHF
BHLHHFBHLHHFBHLHHFBHLHHFBHLHHFBHLHHFBHLHHFBHLHHF
BLLHHFBHLHHFBHLHHFBHLHHFBHLHHFBHLHHFBLLHHFBHLHHF
BHLHHFBHLHHFBLLHHFBHLHHFBHLHHFBHLHHFBLLLLFBHLHHF
BHLHHFBHLHHFBLLHHFBHLHLFBHLHHFBHLHHFBLLHHFBHLLHF
BHLHHFBHLHHFBHLHHFBHLHHFBHLHHFBHLHHFBHLHHFBHLHHF
BHLHLFBHLHLFBHLHLFBHLHLFBHLHLFBHLHLFBHLHLFBHLHLF
BHLHLFBHLHLFBHLHLFBHLHLFBHLHLFBHLHLFBHLHLFBHLHLF
BHLHLFBHLHLFBHLLLFBHLHLFBHLHLFBHLHLFBHLHLFBHLLLF
BLLHLFBHLHLFBHLHLFBHLHLFBHLHLFBLLHLFBHLHLFBHLHLF
BHLLLFBHLLLFBLLLLFBHLLLFBHLLLFBHLLLFBHLLLFBHLLLF
BHLLLFBHLLLFBHLLLFBHLLLFBHLLLFBHLLLFBHLLLFBHLLLF
BHLLLFBHLLLFBHLLLFBHLLLFBHLLLFBHLLLFBHLLLFBHLLLF
BHLLLFBHLLLFBHLLLFBHLLLFBHLLLFBHLLLFBHLLLFBHLLLF
BLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLF
BLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLF
BLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLF
BLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLF
BLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLF
BLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLF
BLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLF
BLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLFBLLLLF
```

```
**********************************************************************************************************
C       MAIN PROGRAM
C
        COMMON LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT
        LOGICAL LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LFIRST,LFIX
        LOGICAL LFUSES(32,64),LPHASE(20),LBUF(20),LMATCH
        INTEGER TITLE(80),ILINE(80),ICOLUMN,ISYM(8,20),IBUF(8,20),C,H,R,P,
      C       S,M,Q,IBLOW
        DATA LFUSES/2048*.FALSE./,ICOLUM/O/,L/'L'/,H/'H'/,N/'N'/,P/'P'/,
      C     C/'C'/,R/'R'/,M/'M'/,Q/'Q'/,IBLOW/O/,S/'S'/
C
        READ(1,10) INOAI,IOT,INOO,TITLE,ILINE
   10   FORMAT(3X,I2,A1,I1,//,80A1,//,80A1)
        CALL INITLZ(INOAI,IOT,INOO,ITYPE,LFUSES,ILINE,ICOLUM)
        DO 20 J=1,20
   20     CALL GETSYM(LPHASE,ISYM,J,ILINE,ICOLUM,LFIX)
          IF(.NOT.(LEQUAL.OR.LLEFT.OR.LAND.OR.LOR.OR.LRIGHT)) GO TO 25
            WRITE(7,23)
   23       FORMAT( ' PIN LIST ERROR,LESS THAN 20 SYMBOLS')
   25   CALL GETSYM(LBUF,IBUF,1,ILINE,ICOLUM,LFIX)
   28     IF(.NOT.LEQUAL) GO TO 25
          CALL MATCH(IMATCH,IBUF,ISYM)
          IF( (IMATCH.LT.12) .OR. (IMATCH.GT.19) ) GO TO 100
          I88PRO=(19-IMATCH)*8 + 1
          IF( IOT.EQ.C ) I88PRO=25
          ICOLUM=0
   30      CALL INCR(ILINE,ICOLUM,LFIX)
           IF( .NOT. ( LEQUAL.OR.LLEFT ) ) GO TO 30
           IF(.NOT.LLEFT) CALL SLIP(LFUSES,I88PRO,INOAI,IOT,INOO,IBLOW)
          DO 70 I8PRO=1,16
            IPROD = I88PRO + I8PRO - 1
            LFIRST=.TRUE.
   50         CALL GETSYM(LBUF,IBUF,1,ILINE,ICOLUM,LFIX)
              IF(LFIX) GO TO 59
              CALL MATCH(IMATCH,IBUF,ISYM)
              IF(IMATCH.EQ.O) GO TO 100
              IF(IMATCH.EQ.99) GO TO 64
              IF(.NOT.LFIRST) GO TO 58
                  LFIRST=.FALSE.
                  DO 56 I=1,32
                      IBLOW = IBLOW + 1
   56                 LFUSES(I,IPROD)=.TRUE.
   58         IBUBL=0
              IF(((      LPHASE(IMATCH)).AND.(.NOT.LBUF(1))).OR.
      C     ((.NOT.LPHASE(IMATCH)).AND.(      LBUF(1))) IBUBL=1
              IINPUT=IXLATE(IMATCH,ITYPE)+IBUBL
              IF(IINPUT.LE.O) GO TO 60
              IBLOW = IBLOW - 1
              LFUSES(IINPUT,IPROD)=.FALSE.
              CALL PLOT(LBUF,IBUF,LFUSES,IPROD,TITLE,.FALSE.,ITYPE)
              GO TO 60
```


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```
   59          CALL FIXSYM(LBUF,IBUF,ILINE,ICOLUM,LFIRST,LFUSES,IPROD,
     C         LFIX)
   60          IF(LAND) GO TO 50
   64        IF( .NOT.LRIGHT ) GO TO 68
   66          CALL INCR(ILINE,ICOLUM,LFIX)
               IF( .NOT.LEQUAL ) GO TO 66
   68        IF(.NOT. (LOR.OR.LEQUAL) ) GO TO 74
   70        CONTINUE
   74    CALL GETSYM(LBUF,IBUF,1,ILINE,ICOLUM,LFIX)
         IF(LLEFT.OR.LEQUAL) GO TO 28
  100 IF((IBUF(1,1).EQ.C).AND.(IBUF(2,1).EQ.R).AND.(IBUF(4,1).EQ.P)
     C  .AND.(IBUF(8,1).EQ.N)) GO TO 102
      WRITE(7,101) (IBUF(I,1),I=1,8),ILINE
  101 FORMAT(' ERROR SYMBOL = ',8A1,/,80A1,/)
  102 IF(ITYPE.LE.4) CALL TWEEK(ITYPE,IOT,LFUSES)
      WRITE(7,104) IBLOW
  104 FORMAT(' NUMBER OF FUSES BLOWN = ',I4)
      WRITE(8,106)
  106 FORMAT(' OPERATION CODES: ',
     C 'P=PLOT H=HEX S=SHORT L=BHLF N=BPNF M=MAP Q=QUIT')
  108 WRITE(8,110)
  110 FORMAT(' ENTER OPERATION CODE')
      READ(5,120) IOP
  120 FORMAT(1A1)
      CALL IODC2
      IF(IOP.EQ.P) CALL PLOT(LBUF,IBUF,LFUSES,IPROD,TITLE,.TRUE.,ITYPE)
      IF(IOP.EQ.H) CALL HEX(LFUSES,H)
      IF(IOP.EQ.S) CALL HEX(LFUSES,S)
      IF(IOP.EQ.L) CALL BHLF(LFUSES,H,L)
      IF(IOP.EQ.N) CALL BHLF(LFUSES,P,N)
      CALL IODC4
      IF(IOP.NE.Q) GO TO 108
      STOP
      END
C
C ***************************************************************************************************
      SUBROUTINE INITLZ(INOAI,IOT,INOO,ITYPE,LFUSES,ILINE,ICOLUM,LFIX)
      INTEGER L,R,X,A
      LOGICAL LFIX
      DATA L/'L'/,R/'R'/,X/'X'/,A/'A'/
      IF( INOAI .LT. 16 )                                  ITYPE = (INOAI/2) - 4
      IF( (INOAI .EQ. 16)                 )                ITYPE = 4
      IF ( (INOAI .EQ. 16) .AND. (INOO .EQ. 8) )           ITYPE = 5
      IF( (IOT .EQ. R) .OR. (IOT .EQ. A) .OR. (IOT .EQ. X) )  ITYPE = 6
      CALL INCR(ILINE,ICOLUM,LFIX)
      RETURN
      END
C
```

```
C ***********************************************************************************************************
      SUBROUTINE GETSYM(LPHASE,ISYM,J,ILINE,ICOLUM,LFIX)
      COMMON LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT
      LOGICAL LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LPHASE(20),LFIX
      INTEGER ILINE(80),ISYM(8,20),IBLANK
      DATA IBLANK/' '/
      LFIX=.FALSE.
      IF( .NOT.(LLEFT.OR.LAND.OR.LOR.OR.LEQUAL.OR.LRIGHT) ) GO TO 10
      CALL INCR(ILINE,ICOLUM,LFIX)
      IF(LLEFT) GO TO 60
   10 LPHASE(J)=( .NOT. LSLASH )
      IF(LPHASE(J)) GO TO 15
      CALL INCR(ILINE,ICOLUM,LFIX)
   15 DO 20 I=1,8
   20     ISYM(I,J)=IBLANK
   25 DO 30 I=1,7
   30     ISYM(I,J)=ISYM(I+1,J)
      ISYM(8,J)=ILINE(ICOLUM)
      CALL INCR(ILINE,ICOLUM,LFIX)
      IF(LLEFT.OR.LBLANK.OR.LAND.OR.LOR.OR.LRIGHT.OR.LEQUAL ) GO TO 40
      GO TO 25
   40 CONTINUE
      WRITE(7,50) (ISYM(I,J), I=1,8)
   50 FORMAT(' ',8A1)
      RETURN
   60 LFIX=.TRUE.
      RETURN
      END
C
C ***********************************************************************************************************
      SUBROUTINE INCR(ILINE,ICOLUM,LFIX)
      COMMON LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT
      LOGICAL LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LFIX
      INTEGER ILINE(80),IBLANK,ILEFT,IAND,IOR,ISLASH,IEQUAL,IRIGHT,
     C        ICOLON
      DATA IBLANK/' '/,ILEFT/'('/,IAND/'*'/,IOR/'+'/,
     C        ISLASH/'/'/,IEQUAL/'='/,IRIGHT/')'/,ICOLON/':'/
      LBLANK=.FALSE.
   10 ICOLUM=ICOLUM+1
      IF(ICOLUM.LE.79) GO TO 30
      READ(1,20,ERR=70,END=70) ILINE
      ICOLUM=1
   20 FORMAT(80A1)
   30 IF( ILINE(ICOLUM) .EQ. IBLANK ) LBLANK=.TRUE.
      WRITE(7,50) ILINE(ICOLUM)
   50 FORMAT(' .',1A1)
      IF( ( ILINE(ICOLUM).EQ.IBLANK ) .OR.
```


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```
      C ((ILINE(ICOLUM).EQ.ICOLON).AND.(.NOT.LFIX))) GO TO 10
        LLEFT = (       ILINE(ICOLUM) .EQ. ILEFT)
        LAND =(         ILINE(ICOLUM) .EQ. IAND   )
        LOR =(          ILINE(ICOLUM) .EQ. IOR    )
        LSLASH=(        ILINE(ICOLUM) .EQ. ISLASH)
        LEQUAL=(        ILINE(ICOLUM) .EQ. IEQUAL)
        LRIGHT=(        ILINE(ICOLUM) .EQ. IRIGHT)
     60 RETURN
     70 LBLANK=.TRUE.
        RETURN
        END
C
C ***************************************************************************************************

        SUBROUTINE MATCH(IMATCH,IBUF,ISYM)
        INTEGER IBUF(8,20),ISYM(8,20),C,A,R,Y
        LOGICAL LMATCH
        DATA C/'C'/,A/'A'/,R/'R'/,Y/'Y'/
        IMATCH=0
        DO 20 J=1,20
            LMATCH=.TRUE.
            DO 10 I=1,8
     10         LMATCH=LMATCH.AND.(IBUF(I,1).EQ.ISYM(I,J) )
            IF(LMATCH) IMATCH=J
     20     CONTINUE
        IF((IBUF(3,1).EQ.C.).AND.
      C     (IBUF(4,1).EQ.A).AND.
      C     (IBUF(5,1).EQ.R).AND.
      C     (IBUF(6,1).EQ.R).AND.
      C     (IBUF(7,1).EQ.Y))   IMATCH=99
        RETURN
        END
C
C ***************************************************************************************************

        FUNCTION IXLATE(IMATCH,ITYPE)
        INTEGER ITABLE(20,6)
        DATA     ITABLE/
      C       3,1,5,9,13,17,21,25,29,-1,31,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,
      C       3,1,5,9,13,17,21,25,29,-1,31,27,-1,-1,-1,-1,-1,-1,7,-1,
      C       3,1,5,9,13,17,21,25,29,-1,31,27,23,-1,-1,-1,-1,11,7,-1,
      C       3,1,5,9,13,17,21,25,29,-1,31,27,23,19,-1,-1,15,11,7,-1,
      C       3,1,5,9,13,17,21,25,29,-1,31,-1,27,23,19,15,11,7,-1,-1,
      C       -1,1,5,9,13,17,21,25,29,-1,-1,31,27,23,19,15,11,7,3,-1/
        IXLATE=ITABLE(IMATCH,ITYPE)
        RETURN
        END
C
C ***************************************************************************************************

        SUBROUTINE FIXSYM(LBUF,IBUF,ILINE,ICOLUM,LFIRST,LFUSES,IPROD,LFIX)
        LOGICAL LBUF(20),LFUSES(32,64),LFIRST,LMATCH,LFIX
        INTEGER IBUF(8,20),ILINE(80),FIXBUF(8),A,B,ISLASH,IOR,IAND,N,Q,
```

```
      C       NO,N1,N2,N3,IBLANK,IRIGHT,TABLE(5,14)
        DATA A/'A'/,B/'B'/,ISLASH/'/'/,IOR/'+'/,IBLANK/' '/,IRIGHT/')'/,
      C       IAND/'*'/,N/'N'/,Q/'Q'/,NO/'0'/,N1/'1'/,N2/'2'/,N3/'3'/,
      C     ICOLON/':'/,
      C       TABLE    /       ' ','A','+','/','B',' ',' ','A','+','B',
      C     ' ',' ',' ',' ','A','/','A','+','/','B',' ',' ',' ',' ','/','B',
      C     'A',':','+',':','B',' ','A','*','/','B',' ',' ','/','A','+','B',
      C     'A',':','*',':','B',' ',' ',' ',' ',' ','B',' ',' ',' ','A','*','B',
      C     ' ',' ',' ',' ','/','A','/','A','*','/','B',' ',' ','/','A','*','B'/
        INPUT=0
        DO 20 I=1,8
            IBUF(I,1)=IBLANK
   20       FIXBUF(I)=IBLANK
   21   CALL INCR(ILINE,ICOLUM,LFIX)
        I=ILINE(ICOLUM)
        IF(I.EQ.IRIGHT) GO TO 40
        IF(I.EQ.NO) IINPUT=8
        IF(I.EQ.N1) IINPUT=12
        IF(I.EQ.N2) IINPUT=16
        IF(I.EQ.N3) IINPUT=20
        DO 24 J=1,7
   24       IBUF(J,1)=IBUF(J+1,1)
        IBUF(8,1)=I
        IF(.NOT. ( (I.EQ.A).OR.(I.EQ.B).OR.(I.EQ.ISLASH).OR.(I.EQ.IOR)
      C         .OR.(I.EQ.IAND).OR.(I.EQ.ICOLON) ) ) GO TO 21
        DO 30 I=1,4
   30       FIXBUF(I)=FIXBUF(I+1)
        FIXBUF(5)=ILINE(ICOLUM)
        GO TO 21
   40   IMATCH=0
        DO 60 J=1,14
            LMATCH=.TRUE.
            DO 50 I=1,5
   50           LMATCH=LMATCH .AND. ( FIXBUF(I).EQ.TABLE(I,J) )
   60       IF(LMATCH) IMATCH=J
        IF(IMATCH.EQ.0) GO TO 100
        IF(.NOT.LFIRST) GO TO 85
            LFIRST=.FALSE.
            DO 80 I=1,32
   80           LFUSES(I,IPROD)=.TRUE.
   85   DO 90 I=1,4
        IF( (IMATCH-7).GT.0 ) LFUSES(IINPUT+I,IPROD)=.FALSE.
        IF( (IMATCH-7).GT.0 ) IMATCH=IMATCH-8
   90   IMATCH=IMATCH+IMATCH
        LBUF(1)=.TRUE.
        CALL PLOT(LBUF,IBUF,LFUSES,IPROD,TITLE,.FALSE.,ITYPE)
  100   LFIX=.FALSE.
        CALL INCR(ILINE,ICOLUM,LFIX)
        RETURN
        END
C
```


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```
C ***************************************************************************************************************
      SUBROUTINE IODC2
C***  THIS ROUTINE IS OPTIONAL. IT MAY BE USED TO TURN PERIPHERALS ON.
      INTEGER DC2,BEL
      DATA DC2/Z12000000/,BEL/Z2F000000/
      WRITE(6,10) DC2,BEL
   10 FORMAT (' ',2A1)
      RETURN
      END
C
C ***************************************************************************************************************
      SUBROUTINE PLOT(LBUF,IBUF,LFUSES,IPROD,TITLE,LDUMP,ITYPE)
      INTEGER IBUF(8,20),IOUT(64),IBLANK,IAND,IOR,ISLASH,IDASH,X,
     C        ISAVE(64,32),TITLE(80)
      DATA IBLANK/' '/,IAND/'*'/,ISAVE/2048*' '/,
     C        IOR/'+'/,ISLASH/'/'/,X/'X'/,IDASH/'-'/
      LOGICAL LBUF(20),LFUSES(32,64),LDUMP
      IF(LDUMP) GO TO 60
      IF(ISAVE(IPROD,1).NE.IBLANK) RETURN
      IF( LBUF(1) ) GO TO 5
      DO 30 J=1,31
   30    ISAVE(IPROD,J)=ISAVE(IPROD,J+1)
      ISAVE(IPROD,32)=ISLASH
    5 DO 20 I=1,8
          IF( ISAVE(IPROD,1).NE.IBLANK ) RETURN
          IF( IBUF(I,1) .EQ. IBLANK ) GO TO 20
          DO 10 J=1,31
   10        ISAVE(IPROD,J)=ISAVE(IPROD,J+1)
          ISAVE(IPROD,32)=IBUF(I,1)
   20    CONTINUE
      IF(ISAVE(IPROD,1).NE.IBLANK) RETURN
   40 DO 50 J=1,31
   50    ISAVE(IPROD,J)=ISAVE(IPROD,J+1)
      ISAVE(IPROD,32)=IAND
      RETURN
   60 WRITE(6,62) TITLE
   62 FORMAT(////,' ',80A1,//,

     C '                    11 1111 11 11 2222 2222 2233',/,
     C '       0123 4567 8901 2345 6789 0123 4567 8901',/)
      DO 100  I88PRO=1,57,8
          DO 94 I8PRO=1,8
              IPROD=I88PRO+I8PRO-1
              ISAVE(IPROD,32)=IBLANK
              DO 70 I=1,32
                  IF( ISAVE(IPROD,1) .NE. IBLANK ) GO TO 70
                  DO 65 J=1,31
```

```
   65                ISAVE(IPROD,J)=ISAVE(IPROD,J+1)
                   ISAVE(IPROD,32)=IBLANK
   70              CONTINUE
                DO 80 I=1,32
                   IOUT(I)=X
                   IF( LFUSES(I,IPROD) ) IOUT(I)=IDASH
                   IOUT(I+32)=ISAVE(IPROD,I)
   80           CONTINUE
                IF( ITYPE .LE. 4 ) CALL FANTOM(ITYPE,IOUT,IPROD,I8PRO)
                IPROD=IPROD-1
                WRITE(6,90) IPROD,IOUT
   90           FORMAT(' ',I2,8(' ',4A1),' ',32A1)
   94           CONTINUE
                WRITE(6,96)
   96           FORMAT(1X)
  100           CONTINUE
          WRITE(6,110)
  110 FORMAT(/,
        C'LEGEND:     X : FUSE NOT BLOWN (L,N,O) - : FUSE BLOWN (H,P,1)')
          IF (ITYPE.LE.4) WRITE(6,111)
  111 FORMAT(
        C'          O : PHANTOM FUSE (L,N,O) O : PHANTOM FUSE (H,P,1)')
          WRITE(6,112)
  112 FORMAT(////)
          RETURN
          END
C
C ***************************************************************************************************************
          SUBROUTINE HEX(LFUSES,IOP)
          LOGICAL LFUSES(32,64)
          INTEGER ITEMP(64),S,H,IOP
          DATA STX/Z02000000/,BEL/Z2F000000/,SOH/Z01000000/,
        C       H/'H'/,S/'S'/
          IF(IOP.EQ.H) WRITE(6,10)
    10 FORMAT(//,'                                                                                .',//)
C***** NOTE: SOME PROM PROGRAMMERS NEED A START CHARACTER.
C*****         THIS PROGRAM OUTPUTS AN STX FOR THE DATA I/O MODEL 9
C*****         (USE SOH FOR MODEL 5)
          WRITE(6,5) BEL,BEL,BEL,BEL,BEL,BEL,BEL,STX,SOH
      5 FORMAT(9A1)
          DO 40 I=1,33,32
          INC=I-1
            DO 40 IPROD=1,7,2
              DO 20 J=1,2
                 DO 20 IINPUT=1,32
                 IHEX=0
                 IF(LFUSES(IINPUT,IPROD + J-1 + 0+INC)) IHEX=IHEX+1
                 IF(LFUSES(IINPUT,IPROD + J-1 + 8+INC)) IHEX=IHEX+2
                 IF(LFUSES(IINPUT,IPROD + J-1 +16+INC)) IHEX=IHEX+4
                 IF(LFUSES(IINPUT,IPROD + J-1 +24+INC)) IHEX=IHEX+8
    20           ITEMP(IINPUT + 32*(J-1) )=IHEX
            IF(IOP.EQ.H) WRITE(6,60) ITEMP
    40      IF(IOP.EQ.S) WRITE(6,61) ITEMP
```

```
   60      FORMAT(' ',32(Z1,' '),'.',/,' ',32(Z1,' '),'.')
   61      FORMAT(' ',64Z1)
        IF(IOP.EQ.H) WRITE(6,70)
   70 FORMAT(' ',//,'                                                          ',//)
        RETURN
        END
C
C *****************************************************************************************
        SUBROUTINE BHLF(LFUSES,H,L)
        LOGICAL LFUSES(32,64)
        INTEGER ITEMP(4,8),L,H
        WRITE(6,10)
   10 FORMAT(//,'                                                              ',//)
        DO 20 I=1,33,32
        INC=I-1
          DO 20 IPROD=1,8
               DO 20 J=1,25,8
                 DO 15 K=1,8
                   IINPUT=J+K-1
                   ITEMP(1,K)=L
                   ITEMP(2,K)=L
                   ITEMP(3,K)=L
                   ITEMP(4,K)=L
                   IF(LFUSES(IINPUT,IPROD+ 0+INC)) ITEMP(4,K)=H
                   IF(LFUSES(IINPUT,IPROD+ 8+INC)) ITEMP(3,K)=H
                   IF(LFUSES(IINPUT,IPROD+16+INC)) ITEMP(2,K)=H
                   IF(LFUSES(IINPUT,IPROD+24+INC)) ITEMP(1,K)=H
   15              CONTINUE
   20            WRITE(6,30) ITEMP
   30            FORMAT(' ',8('B',4A1,'F'))
        WRITE(6,10)
        RETURN
        END
C
C *****************************************************************************************
        SUBROUTINE IODC4
C*** THIS ROUTINE IS OPTIONAL. IT MAY BE USED TO TURN PERIPHERALS OFF.
        INTEGER DC3,DC4,BEL
        DATA DC3/Z37000000/,DC4/Z3C000000/,BEL/Z2F000000/
        WRITE(6,10) BEL,DC3,DC4
   10 FORMAT(' ',3A1)
        RETURN
        END
C
```

```
C ***************************************************************************************************************
      SUBROUTINE TWEEK(ITYPE,IOT,LFUSE)
      INTEGER L,C
      LOGICAL LFUSES(32,64)
      DATA L/'L'/,C/'C'/
      IF(ITYPE.GE.4) GO TO 20
      DO 10 IPROD=1,64
         LFUSES(15,IPROD)=.TRUE.
         LFUSES(16,IPROD)=.TRUE.
         LFUSES(19,IPROD)=.TRUE.
         LFUSES(20,IPROD)=.TRUE.
         IF(ITYPE.GE.3) GO TO 10
         LFUSES(11,IPROD)=.TRUE.
         LFUSES(12,IPROD)=.TRUE.
         LFUSES(23,IPROD)=.TRUE.
         LFUSES(24,IPROD)=.TRUE.
         IF(ITYPE.GE.2) GO TO 10
         LFUSES( 7,IPROD)=.TRUE.
         LFUSES( 8,IPROD)=.TRUE.
         LFUSES(27,IPROD)=.TRUE.
         LFUSES(28,IPROD)=.TRUE.
   10    CONTINUE
      DO 18 IINPUT=7,28
         DO 12 IPROD=1,57,8
            LFUSES(IINPUT,IPROD+4)=.FALSE.
            LFUSES(IINPUT,IPROD+5)=.FALSE.
            LFUSES(IINPUT,IPROD+6)=.FALSE.
   12       LFUSES(IINPUT,IPROD+7)=.FALSE.
         IF(ITYPE.GE.3) GO TO 18
         DO 14 IPROD=17,41,8
            LFUSES(IINPUT,IPROD+2)=.FALSE.
   14       LFUSES(IINPUT,IPROD+3)=.FALSE.
         IF(ITYPE.GE.2) GO TO 18
         DO 16 IPROD=1,57,8
            LFUSES(IINPUT,IPROD+2)=.FALSE.
   16       LFUSES(IINPUT,IPROD+3)=.FALSE.
   18 CONTINUE
   20 IF( (ITYPE.EQ.1) .OR.((ITYPE.EQ.4).AND.(IOT.EQ.L)) ) GO TO 100
      DO 99 IINPUT=1,32
         DO 30 IPROD=1,8
            LFUSES(IINPUT,IPROD+0)= (IOT.NE.L)
   30       IF(IOT.NE.C) LFUSES(IINPUT,IPROD+56)=(IOT.NE.L)
         IF(ITYPE.LE.2) GO TO 99
         DO 40 IPROD=1,8
            LFUSES(IINPUT,IPROD+ 8)= (IOT.NE.L)
   40       IF(IOT.NE.C) LFUSES(IINPUT,IPROD+48)= (IOT.NE.L)
         IF(ITYPE.LE.3) GO TO 99
         DO 50 IPROD=1,8
            LFUSES(IINPUT,IPROD+16)= (!OT.NE.L)
   50       IF(IOT.NE.C) LFUSES(IINPUT,IPROD+40)=(IOT.NE.L)
   99    CONTINUE
  100 RETURN
      END
```


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```
C
C ***************************************************************************************************************
      SUBROUTINE SLIP(LFUSES,I88PRO, IN0AI,IOT,IN00,IBLOW)
      LOGICAL LFUSES(32,64)
      INTEGER R
      DATA R/'R'/
      IF( (IN0AI.LT.16) .OR. (IN00.LT.4) .OR.
     C    ( (IOT.EQ.R).AND.(IN00.EQ.8) ) .OR.
     C    ( (I88PRO.GE.9).AND.(I88PRO.LE.49).AND.(IN00.EQ.6) ) .OR.
     C    ( (I88PRO.GE.17).AND.I88PRO.LE.41).AND.(IN00.EQ.4) ) ) RETURN
      DO 10 I=1,32
      IBLOW = IBLOW + 1
   10 LFUSES(I,I88PRO) = .TRUE.
      I88PRO = I88PRO + 1
      RETURN
      END
C
C ***************************************************************************************************************
      SUBROUTINE FANTOM(ITYPE,IOUT,IPROD,I8PRO)
      INTEGER ITYPE,IOUT(64),IPROD,I8PRO,X,IDASH,FX,FIDASH
      DATA X/'X'/,IDASH/'-'/,FX/'O'/,FIDASH/'O'/
      DO 10 I=1,32
         IF( IOUT(I).EQ.X     ) IOUT(I)=FX
   10    IF( IOUT(I).EQ.IDASH ) IOUT(I)=FIDASH
      IF((ITYPE.EQ.4).AND.((IPROD.LE.24).OR.(IPROD.GE.41))) GO TO 100
      IF((ITYPE.EQ.3).AND.((IPROD.LE.16).OR.(IPROD.GE.45))) GO TO 100
      IF((ITYPE.EQ.2).AND.((IPROD.LE. 8).OR.(IPROD.GE.53))) GO TO 100
      IF((ITYPE.LE.3).AND.(I8PRO.GE.5)) GO TO 100
      IF((ITYPE.LE.2).AND.(IPROD.GE.19).AND.(IPROD.LE.48).AND.
     C    (I8PRO.GE.3)) GO TO 100
      IF((ITYPE.EQ.1).AND.(I8PRO.GE.3)) GO TO 100
      DO 50 I=1,32
        IF(((I.EQ.15).OR.(I.EQ.16).OR.(I.EQ.19).OR.(I.EQ.20)).AND.
     C    (ITYPE.LE.3)) GO TO 50
        IF(((I.EQ.11).OR.(I.EQ.12).OR.(I.EQ.23).OR.(I.EQ.24)).AND.
     C    (ITYPE.LE.2)) GO TO 50
        IF(((I.EQ. 7).OR.(I.EQ. 8).OR.(I.EQ.27).OR.(I.EQ.28)).AND.
     C    (ITYPE.LE.1)) GO TO 50
        IF(IOUT(I).EQ.FX    ) IOUT(I)=X
      IF (IOUT(I).EQ.FIDASH) IOUT(I) = IDASH
   50 CONTINUE
  100 RETURN
      END
```

BETA
Bipolar Enhanced Throughput Architecture Products

'AS888 and 'AS889 8-Bit Processor Slices
'AS890 and 'AS891 Microsequencers

8-BIT PROCESSOR SLICES

TABLE OF CONTENTS

ADVANCE INFORMATION

This document contains information on a new product. Specifications are subject to change without notice.

TEXAS INSTRUMENTS
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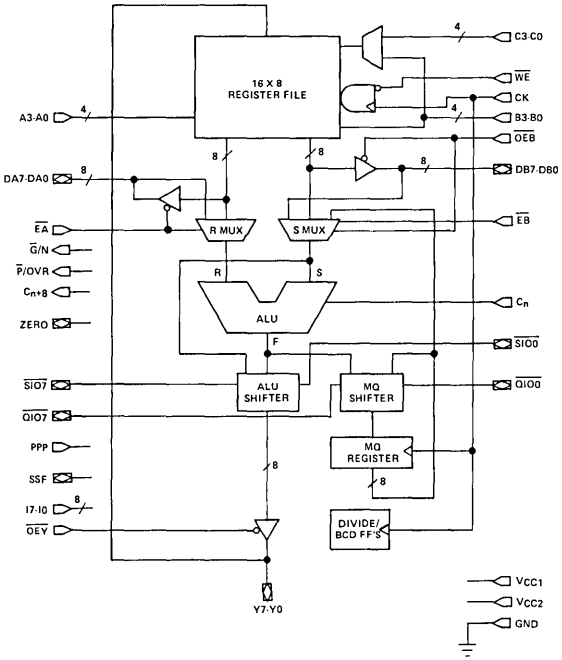
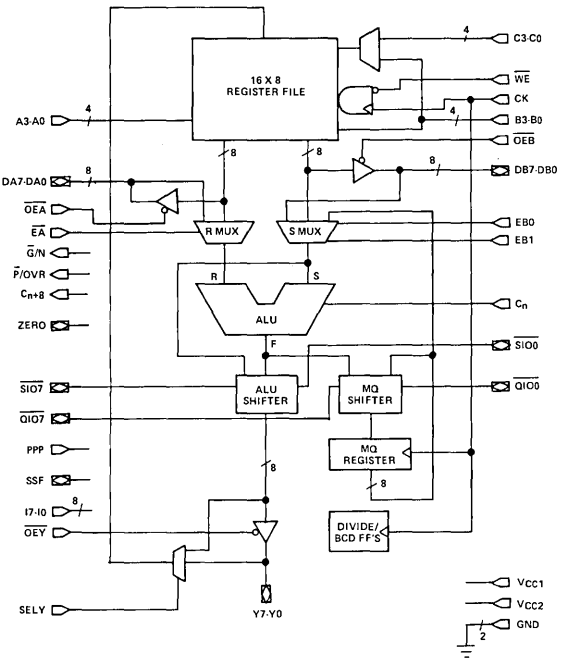
TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF TABLES



FUNCTIONAL BLOCK DIAGRAM FOR 'AS888



FUNCTIONAL BLOCK DIAGRAM FOR 'AS889

1182

'AS888 AND 'AS889 8-BIT PROCESSOR SLICES

1. INTRODUCTION

These 8-bit Advanced Schottky TTL integrated circuits are designed to implement high performance digital computers or controllers. An architecture and instruction set has been chosen that supports a fast system clock, a narrow micro-code word width, and a high system throughput. The powerful instruction set allows high-speed system architecture to be implemented and also allows an existing systems performance to be upgraded while protecting software investments. These processors are designed to be cascadable to any word width 16 bits or greater.

The SN54AS888 and SN54AS889 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74AS888 and SN74AS889 are characterized for operation from 0 °C to 70 °C.

The 'AS888 is supplied in a 64-pin dual-in-line ceramic package and the 'AS889 is supplied in a 68-pin plastic or ceramic chip carrier package.

1.1 DISTINCTIVE FEATURES

- STL-AS technology
- Parallel 8-bit ALU with expansion inputs and outputs
- 13 arithmetic and logic functions
- 8 conditional shifts (single and double length)
- 9 instructions that manipulate bytes
- 4 instructions that manipulate bits
- Add and subtract immediate instructions
- Absolute value instruction
- Signed magnitude to/from 2's complement conversion
- Polynomial code accumulation (CRC, FIRE, Computer Generated, etc.)
- Single- and double-length normalize
- Select functions
- Signed and unsigned divides with overflow detection; input does not need to be prescaled.
- Signed, mixed, and unsigned multiplies
- Three-operand, 16-word register file
- Full carry look ahead support
- Sign, carry out, overflow, and zero-detect status capabilities
- Excess-3 BCD arithmetic.

1.2 ARCHITECTURAL FEATURES

The internal architecture has been configured to provide for a high system throughput. Some unique features are:

- Internal shift multiplexers that eliminate the need for external shift control parts.
- An ALU bypass path to increase the speeds of multiply, divide, and normalize instructions and to provide new instructions such as Bit Set, Bit Reset, Bit Test, Byte Subtract, Byte Add, and Byte Logical.
- 3-operand register files to allow an operation and a move instruction to be combined.
- Byte select controlled by external 3-state buffers that may be eliminated if bit and byte manipulation are not needed.
- Bit and byte masks that are shared with register address fields to minimize control store word width.
- 3 data input/output paths maximize data throughput.

Functional descriptions of the pins and pin assignments for the 'AS888 and 'AS889 are given in Table 1 and Figure 1, and Table 2 and Figure 2, respectively.

1182

TABLE 1 – 'AS888 PIN DESCRIPTIONS

PIN NUMBER(S)	NAME	INPUT/OUTPUT	DESCRIPTION
1	$\overline{WE}$	Input	Register file (RF) write enable. Data is written into RF when $\overline{WE}$ is low and a low-to-high clock transition occurs. RF write is inhibited when $\overline{WE}$ is high.
2-5	B3-B0	Input	Register file B port read address select. (0 = LSB)
6	$\overline{EB}$	Input	ALU input operand select. High state selects MQ register as input. Low state selects either register file ($\overline{OEB}$ = 0) or external data ($\overline{OEB}$ = 1) as input.
7	$\overline{OEB}$	Input	DB bus enable, low active.
8-15	DB7-DB0	Input/Output	B port data bus. Outputs register data ($\overline{OEB}$ = 0) or used to input external data ($\overline{OEB}$ = 1). (0 = LSB)
16-23	Y7-Y0	Input/Output	Y port data bus. Outputs instruction results ($\overline{OEY}$ = 0) or used to input external data into register file ($\overline{OEY}$ = 1).
24	$\overline{OEY}$	Input	Y bus output enable, low active.
25	PPP	Input	Package position pin. Tri-level input used to define package significance during instruction execution. Leave open for intermediate positions, tie to V_{CC} for most significant package, and tie to GND for least significant package.
26	SSF	Input/Output	Special shift function. Used to transfer required information between packages during special instruction execution.
27	ZERO	Input/Output	Device zero detection, open collector. Input during certain special instructions.
28	$\overline{P}$/OVR	Output	ALU active low propagate/instruction overflow for most significant package.
29	$\overline{G}$/N	Output	ALU active low generate/negative result for most significant package.
30	C_{n+8}	Output	ALU ripple carry output.
31	$\overline{SIO7}$	Input/Output	Bidirectional shift pin, low active.
32	$\overline{QIO7}$	Input/Output	Bidirectional shift pin, low active.
33	$\overline{QIO0}$	Input/Output	Bidirectional shift pin, low active.
34	$\overline{SIO0}$	Input/Output	Bidirectional shift pin, low active.
35	C_n	Input	ALU carry input.
36-43	I0-I7	Input	Instruction inputs.
44	V_{CC2}		Low voltage power supply (2 V).
45	V_{CC1}		I/O interface supply voltage (5 V).
46	$\overline{EA}$	Input	ALU input operand select. High state selects external DA bus and low state selects register file.
47	GND		Ground pin.
48-55	DA0-DA7	Input/Output	A port data bus. Outputs register file data ($\overline{EA}$ = 0) or inputs external data ($\overline{EA}$ = 1).
56	CK	Input	Clocks all synchronous registers on positive edge.

TABLE 1 – 'AS888 PIN DESCRIPTIONS (Continued)

PIN NUMBER(S)	NAME	INPUT/OUTPUT	DESCRIPTION
57-60	C3-C0	Input	Register file write address select.
61-64	A3-A0	Input	Register file A port read address select.

TABLE 2 – 'AS889 PIN DESCRIPTIONS

PIN NUMBER(S)	NAME	INPUT/OUTPUT	DESCRIPTION
1	$\overline{WE}$	Input	Register file (RF) write enable. Data is written into RF when $\overline{WE}$ is low and a low-to-high clock transition occurs. RF write is inhibited when $\overline{WE}$ is high.
2-5	B3-B0	Input	Register file B port read address select. (0 = LSB)
7	$\overline{OEB}$	Input	DB bus enable, low active.
9-16	DB7-DB0	Input/Output	B port data bus. Outputs register data ($\overline{OEB}$ = 0) or used to input external data ($\overline{OEB}$ = 1). (0 = LSB)
18-25	Y7-Y0	Input/Output	Y port data bus. Outputs instruction results ($\overline{OEY}$ = 0) or used to input external data into register file ($\overline{OEY}$ = 1).
26	$\overline{OEY}$	Input	Y bus output enable, low active.
27	PPP	Input	Package position pin. Tri-level input used to define package significance during instruction execution. Leave open for intermediate positions, tie to V_{CC} for most significant package, and tie to GND for least significant package.
28	SSF	Input/Output	Special shift function. Used to transfer required information between packages during special instruction execution.
29	ZERO	Input/Output	Device zero detection, open collector. Input during certain special instructions.
30	$\overline{P}$/OVR	Output	ALU active low propagate/instruction overflow for most significant package.
31	$\overline{G}$/N	Output	ALU active low generate/negative result for most significant package.
32	C_{n+8}	Output	ALU ripple carry output.
33	$\overline{SIO7}$	Input/Output	Bidirectional shift pin, low active.
34	$\overline{QIO7}$	Input/Output	Bidirectional shift pin, low active.
35	$\overline{QIO0}$	Input/Output	Bidirectional shift pin, low active.
36	$\overline{SIO0}$	Input/Output	Bidirectional shift pin, low active.
37	C_n	Input	ALU carry input.
38-42,44-46	I0-I7	Input	Instruction inputs.
48	V_{CC2}		Low voltage power supply (2 V).
49	V_{CC1}		I/O interface supply voltage (5 V).
51	$\overline{EA}$	Input	ALU input operand select. High state selects external DA bus and low state selects register file.

1182

TABLE 2 – 'AS889 PIN DESCRIPTIONS (Continued)

PIN NUMBER(S)	NAME	INPUT/OUTPUT	DESCRIPTION
47	GND		Ground pin.
52-59	DA0-DA7	Input/Output	A port data bus. Outputs register file data ($\overline{EA}=0$) or inputs external data ($\overline{EA}=1$).
60	CK	Input	Clocks all synchronous registers on positive edge.
64-61	C3-C0	Input	Register file write address select.
68-65	A3-A0	Input	Register file A port read address select.
50	$\overline{OEA}$	Input	DA bus enable, low active.
17	SELY	Input	Y bus select, high active.
6,8	EB0, EB1	Input	ALU input operand selects. These inputs select the source of data that the S multiplexer provides for the S bus. Independent control of the DB bus and data path selection allow the user to isolate the DB bus while the R-ALU continues to process data.
43	GND		Ground pin.

4

SN54AS888, SN74AS888 . . . JD PACKAGE
(TOP VIEW)

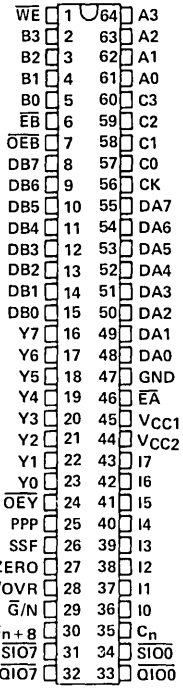


FIGURE 1 – 'AS888 PIN ASSIGNMENTS

SN54AS889, SN74AS889 . . . FN PACKAGE
(TOP VIEW)

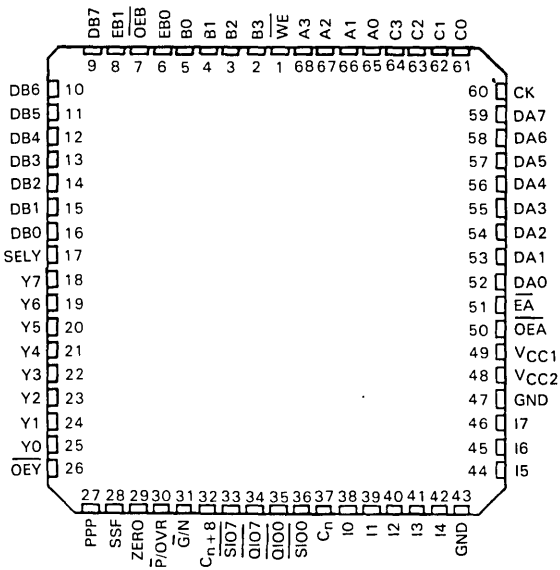


FIGURE 2 – 'AS889 PIN ASIGNMENTS

1182

1.3 ARCHITECTURAL ELEMENTS

3-PORT REGISTER FILE

Working registers consist of 128 storage elements organized into sixteen 8-bit words. These storage elements appear to the user as sixteen positive edge-triggered registers. The three port addresses, one write (C), and two reads (A and B), are completely independent of each other to implement a 3-operand register file. Data is written into the register file when $\overline{WE}$ is low and a low-to-high clock transition occurs. The ADD and SUBTRACT immediate instructions require only one source operand. The B address is used as the source address, and the bits of the A address are used to provide a constant field. The SET, RESET, and TEST BIT instructions use the B addressed register as both the source and destination register while the A and C address are used as masks. These instructions are explained in more detail in the instruction section.

S MULTIPLEXER

The shift instructions are summarized in Table 6 and illustrated in Figure 4. In Figure 4 and all succeeding figures that illustrate instruction execution the following definitions apply.

$\overline{OEB}$	$\overline{EB}$	S bus
Low	Low	RF data (RF data → DB)
Low	High	MQ data (RF data → DB)
High	Low	DB data (DB forced externally)
High	High	MQ data (DB is HI-Z)

The 'AS889 operates as follows:

EB1	EB0	S bus
Low	Low	RF data
Low	High	MQ data
High	Low	DB data
High	High	MQ data

DB PORT

Data is passed through the ALU or received from the register file on the 8-bit DB port. If $\overline{OEB}$ is low, the DB bus is active; if $\overline{OEB}$ is high, the DB bus is in the high impedance state. Notice that on the 'AS889 the DB port may be isolated at the same time that register file data is passed to the ALU.

R MULTIPLEXER

The R multiplexer selects the other operand of the ALU. Except for those instructions that require constants or masks, the R bus will contain DA if $\overline{EA}$ is high or the RF data pointed to by A if $\overline{EA}$ is low.

DA BUS

On the 'AS888, the DA bus is active (with register file data) if $\overline{EA}$ is low. On the 'AS889 package, the DA bus is active if $\overline{OEA}$ is low. Notice that the DA bus may be isolated on the 'AS889 while register file data is passed to the ALU.

ALU

The ALU can perform seven arithmetic and six logical instructions on two 8-bit operands. It also supports multiplication, division, normalization, bit set, reset, and test, byte operations, and excess-3 BCD arithmetic. These source operands are the outputs of the S and R multiplexers

ALU AND MQ SHIFTERS

ALU and MQ shifters perform all of the shift, multiply, divide, and normalize functions. Table 6 shows the value of the $\overline{SIO7}$ and $\overline{QIO7}$ pins of the most-significant package. The standard shifts may be made into conditional shifts and the serial data may be input or output with the aid of two three-state gates. These capabilities are discussed further in the arithmetic and logic section.

1182

MQ REGISTER

The multiplier-quotient (MQ) register has specific functions in multiplication, division, and normalization. This register may also be used as a temporary storage register. The MQ register may be loaded if the instruction code on pins I7-I0 is E1-E7 or E9-EE.

Y BUS

The Y bus contains the output of the ALU shifter if $\overline{OEY}$ is low, and is a high impedance input if $\overline{OEY}$ is high. On the 'AS888 , $\overline{OEY}$ must be low to pass the ALU shift result back to the register file. The 'AS889 will pass the internal ALU shift bus if SELY is low and pass the external Y bus to the register file if SELY is high.

STATUS

Four status pins are available on the most significant package, OVERFLOW (OVR), SIGN (N), CARRY OUT (C_{n+8}), and ZERO. The C_{n+8} line signifies the ALU result while the OVR, Z, and N refer the status after the ALU shift has occured. Notice that the Z pin cannot be used to detect whether an input placed on a high impedance Y bus is zero.

DIVIDE/BCD FLIP-FLOPS

The multiply-divide flip-flops contain the status of the previous multiply or divide instruction. They are affected by the following structions:

DIVIDE REMAINDER FIX
SIGNED DIVIDE QUOTIENT FIX
SIGNED MULTIPLY
SIGNED MULTIPLY TERMINATE
SIGNED DIVIDE INITIALIZE
SIGNED DIVIDE START
SIGNED DIVIDE ITERATE
UNSIGNED DIVIDE START
UNSIGNED DIVIDE ITERATE
UNSIGNED MULTIPLY
SIGNED DIVIDE TERMINATE
UNSIGNED DIVIDE TERMINATE

The excess-3 BCD flip-flops are affected by all instructions except NOP. The clear function clears these flip-flops. They preserve the carry from each nibble (4-bits) in excess – 3/BCD operations (see Sections 3 and 7.3).

PACKAGE POSITION PIN (PPP)

The position of the processor in the system is defined by the voltage level apply to the package position pin (PPP). Intermediate positions are selected by leaving the pin open. Tying the pin to V_{CC} makes the processor the most significant package and tying the pin to GND makes the processor the least significant package.

SPECIAL SHIFT FUNCTION (SSF) PIN

Conditional shifting algorithms may be implemented via control of the SSF pin. The applied voltage to this pin may be set as a function of a potential overflow condition (the two most significant bits are not equal) or any other condition (see Section 3).

2. 'AS888 AND 'AS889 INSTRUCTION SET

The 'AS888 and 'AS889 bit-slice processors use bits I7-I0 as instruction inputs. A combination of bits I3-I0 (Group 1 instructions) and bits I7-I4 (Group 2-5 instructions) are used to develop the 8-bit op-code for a specific instruction. A summary of the instruction set is given in Table 3.

TABLE 3 – 'AS888 AND 'AS889 INSTRUCTION SET

GROUP 1 INSTRUCTIONS		
INSTRUCTION BITS (I3-I0) HEX CODE	**MNEMONIC**	**FUNCTION**
0		Special (see Note 1)
1	ADD	$R+S+C_n$ (see Note 2)
2	SUBR	$\overline{R}+S+C_n$ (see Note 2)
3	SUBS	$R+\overline{S}+C_n$ (see Note 2)
4	INCS	$S+C_n$ (see Note 2)
5	INCNS	$\overline{S}+C_n$ (see Note 2)
6	INCR	$R+C_n$ (see Note 2)
7	INCNR	$\overline{R}+C_n$ (see Note 2)
8		Special (see Note 3)
9	XOR	R XOR S (see Note 2)
A	AND	R AND S (see Note 2)
B	OR	R OR S (see Note 2)
C	NAND	R NAND S (see Note 2)
D	NOR	R NOR S (see Note 2)
E	ANDNR	$\overline{R}$ AND S (see Note 2)
F		Special (see Note 4)
GROUP 2 INSTRUCTIONS		
INSTRUCTION BITS (I7-I4) HEX CODE	**MNEMONIC**	**FUNCTION**
0	SRA	Arithmetic Right Single
1	SRAD	Arithmetic Right Double
2	SRL	Logical Right Single
3	SRLD	Logical Right Double
4	SLA	Arithmetic Left Single
5	SLAD	Arithmetic Left Double
6	SLC	Circular Left Single
7	SLCD	Circular Left Double
8	SRC	Circular Right Single
9	SRCD	Circular Right Double
A	MQSRA	Pass (F→Y) and Arithmetic Right MQ
B	MQSRL	Pass (F→Y) and Logical Right MQ
C	MQSLL	Pass (F→Y) and Logical Left MQ
D	MQSLC	Pass (F→Y) and Circular Left MQ
E	LOADMQ	Pass (F→Y) and Load MQ (F=MQ)
F	PASS	Pass (F→Y)

NOTES:
1. Hex code 0 used to access Group 4 instructions.
2. Hex codes 1-7 and 9-E are used in conjunction with Group 2 shift instructions to perform arithmetic or logical functions plus a shift function in one instruction cycle.
3. Hex code 8 used to access Group 3 instructions.
4. Hex code F used to access Group 5 instructions.

TABLE 3 – 'AS888 and 'AS889 INSTRUCTION SET (Continued)

GROUP 3 INSTRUCTIONS		
INSTRUCTION BITS (I7-I4) HEX CODE	MNEMONIC	FUNCTION
0	SET1	Set Bit
1	SET0	Reset Bit
2	TB1	Test Bit (ONE)
3	TB0	Test Bit (ZERO)
4	ABS	Absolute Value
5	SMTC	Sign Magnitude/Two's Complement
6	ADDI	Add Immediate
7	SUBI	Subtract Immediate
8	BADD	Byte Add R to S
9	BSUBS	Byte Subtract S from R
A	BSUBR	Byte Subtract R from S
B	BINCS	Byte Increment S
C	BINCNS	Byte Increment Negative S
D	BXOR	Byte XOR R and S
E	BAND	Byte AND R and S
F	BOR	Byte OR R and S
GROUP 4 INSTRUCTIONS		
INSTRUCTION BITS (I7-I4) HEX CODE	MNEMONIC	FUNCTION
0	CRC	Cyclic Redundancy Character Accumulation
1	SEL	Select S/R
2	SNORM	Single Length Normalize
3	DNORM	Double Length Normalize
4	DIVRF	Divide Remainder FIX
5	SDIVQF	Signed Divide Quotient FIX
6	SMULI	Signed Multiply Iterate
7	SMULT	Signed Multiply Terminate
8	SDIVIN	Signed Divide Initialize
9	SDIVIS	Signed Divide Start
A	SDIVI	Signed Divide Iterate
B	UDIVIS	Unsigned Divide Start
C	UDIVI	Unsigned Divide Iterate
D	UMULI	Unsigned Multiply Iterate
E	SDIVIT	Signed Divide Terminate
F	UDIVIT	Unsigned Divide Terminate
GROUP 5 INSTRUCTIONS		
INSTRUCTION BITS (I7-I4) HEX CODE	MNEMONIC	FUNCTION
0	CLR	Clear
1	CLR	Clear
2	CLR	Clear
3	CLR	Clear
4	CLR	Clear
5	CLR	Clear
6	CLR	Clear
7	BCDBIN	BCD to Binary
8	EX3BC	Excess-3 Byte Correction
9	EX3C	Excess-3 Word Correction
A	CLR	Clear
B	CLR	Clear
C	CLR	Clear
D	BINEX3	Binary to Excess-3
E	CLR	Clear
F	NOP	No Operation

3. GROUP 1 INSTRUCTIONS

TABLE 4 – GROUP I INSTRUCTIONS

INSTRUCTION BITS (I3-I0) HEX CODE	MNEMONIC	FUNCTION
0		Special (see Note 1)
1	ADD	$R+S+C_n$ (see Note 2)
2	SUBR	$\overline{R}+S+C_n$ (see Note 2)
3	SUBS	$R+\overline{S}+C_n$ (see Note 2)
4	INCS	$S+C_n$ (see Note 2)
5	INCNS	$\overline{S}+C_n$ (see Note 2)
6	INCR	$R+C_n$ (see Note 2)
7	INCNR	$\overline{R}+C_n$ (see Note 2)
8		Special (see Note 3)
9	XOR	R XOR S (see Note 2)
A	AND	R AND S (see Note 2)
B	OR	R OR S (see Note 2)
C	NAND	R NAND S (see Note 2)
D	NOR	R NOR S (see Note 2)
E	ANDNR	$\overline{R}$ AND S (see Note 2)
F		Special (see Note 4)

NOTES:
1. Hex code 0 used to access Group 4 instructions.
2. Hex codes 1-7 and 9-E are used in conjunction with Group 2 shift instructions to perform arithmetic or logical functions plus a shift function in one instruction cycle.
3. Hex code 8 used to access Group 3 instructions.
4. Hex code F used to access Group 5 instructions.

Group 1 instructions (excluding hex codes 0, 8, and F) may be used in conjunction with Group 2 shift instructions to perform arithmetic or logical functions plus a shift function* in one instruction cycle (hex codes 0, 8, and F are used to access Group 4, 3, and 5 instructions, respectively). Each shift may be made into a conditional shift by forcing the special shift function (SSF) pin into the proper state. If the SSF pin is high or floating, the shifted ALU output will be sent to the output buffers. If the SSF pin is pulled low externally, the ALU result will be passed directly to the output buffers. Conditional shifting is useful for scaling inputs in data arrays or in signal processing algorithms. Use of this function sould only be attempted during processing of the Select S/R instruction.

These instructions set the BCD flip-flop for the excess-3 correct instruction (An explanation of BCD arithmetic is given in Section 7.3). The status is set with the following results (C_{n+8} is ALU carry out and is independent of shift operation, others are evaluated after shift operation).

CONDITION CODE

ARITHMETIC

N	→	MSB of result
OVR	→	Signed arithmetic overflow
C_{n+8}	→	CARRY OUT equal one
Z	→	RESULT equal zero

LOGIC

N	→	MSB of result
OVR	→	None (force to zero)
C_{n+8}	→	None (force to zero)
Z	→	RESULT equal zero

* Double precision shifts involve both the ALU and MQ register.

4. GROUP 2 INSTRUCTIONS

TABLE 5 – GROUP 2 INSTRUCTIONS

INSTRUCTION BITS (I7-I4) HEX CODE	MNEMONIC	FUNCTION
0	SRA	Arithmetic Right Single
1	SRAD	Arithmetic Right Double
2	SRL	Logical Right Single
3	SRLD	Logical Right Double
4	SLA	Arithmetic Left Single
5	SLAD	Arithmetic Left Double
6	SLC	Circular Left Single
7	SLCD	Circular Left Double
8	SRC	Circular Right Single
9	SRCD	Circular Right Double
A	MQSRA	Pass (F→Y) and Arithmetic Right MQ
B	MQSRL	Pass (F→Y) and Logical Right MQ
C	MQSLL	Pass (F→Y) and Logical Left MQ
D	MQSLC	Pass (F→Y) and Circular Left MQ
E	LOADMQ	Pass (F→Y) and Load MQ (F=MQ)
F	PASS	Pass (F→Y)

The processors shift instructions are implemented by a combination of Group 2 instructions and certain wired connections on the packages used. The following external connections are required.

On intermediate packages:

$\overline{SIO7}$ is connected to $\overline{SIO0}$ of the next-most-significant package

$\overline{QIO7}$ is connected to $\overline{QIO0}$ of the next-most-significant package

$\overline{SIO0}$ is connected to $\overline{SIO7}$ of the next-least-significant package

$\overline{QIO0}$ is connected to $\overline{QIO7}$ of the next-least-significant package

On the two end packages:

$\overline{SIO7}$ on the most-significant package is connected to $\overline{SIO0}$ of the least-significant package

$\overline{QIO7}$ on the most-significant package is connected to $\overline{QIO0}$ of the least-significant package

The connections are the same on all instructions including r ıltiply, divide, CRC, and normalization functions.

Single- and double-precision shifts are supported. Double-precision shifts assume the most-significant half has come through the ALU and will be placed (if $\overline{WE}$ is low) into the register file on the rising edge of the clock and the least-significant half lies in the MQ register. All Group 2 shifts may be made conditional (see Section 3).

- Arithmetic right shifts copy the sign of the number.
- Arithmetic left shifts do not retain the sign of the number if an overflow occurs. A zero is filled into the LSB if not forced externally.
- Logical right shifts fill a zero in the MSB position if not forced externally.
- Circular right shifts fill the LSB in the MSB position.
- Circular left shifts fill the MSB in the LSB position.
- Shifting left is defined as moving a bit position towards the MSB (doubling).
- Shifting right is defined as moving a bit towards the LSB (halving).

Serial input may be performed by using the circuitry shown in Figure 3. A single-/or double-precision arithmetic left or logical right shift that fills the complement of the data on the SIO0 or SIO7 into the LSB or MSB of the data word(s) implementing the serial input. Note that if SIO0 and SIO7 are floating (HI-Z), a zero will be filled as an end condition.

Serial output may be performed with the circular instructions.

The shift instructions are summarized in Table 6 and illustrated in Figure 4. In Figure 4 and all succeeding figures that illustrate instruction execution the following definitions apply:

CRF – CRC accumulator end fill
QBT – End fill for signed divide
MQF – End fill for unsigned divide.

TABLE 6 – SHIFT INSTRUCTIONS

OP CODE	SHIFT FUNCTION	SIO7 * SIO0 WIRED VALUE	QIO7 * QIO0 WIRED VALUE
ON	Arith Right Single	ALU-LSB Output	–
1N	Arith Right Double	MQ-LSB Output	ALU-LSB Output
2N	Log Right Single	Input to ALU-MSB	ALU-LSB Output
3N	Log Right Double	Input to ALU-MSB	ALU-LSB Output
4N	Arith Left Single	Input to ALU-LSB	ALU-MSB Output
5N	Arith Left Double	Input to MQ-LSB	MQ-MSB Output
6N	Cir Left Single	ALU-MSB Output	–
7N	Cir Left Double	ALU-MSB Output	MQ-MSB Output
8N	Cir Right Single	ALU-LSB Output	–
9N	Cir Right Double	MQ-LSB Output	ALU-LSB Output
AN	Arith Right (MQ only)	MQ-LSB Output	MQ-LSB Output
BN	Log Right (MQ only)	MQ-LSB Output	Input to MQ-MSB
CN	Log Left (MQ only)	Input to MQ-LSB	MQ-MSB Output
DN	Cir Left (MQ only)	MQ-MSB Output	MQ-MSB Output

NOTES: 1. Op Code N≠0, 8, or F; these select special instruction Tables 3, 4, and 5.
2. Shift I/O pins are active low. Therefore, inputs and outputs must be inverted if true logical values are required.

CONDITION CODE

N – RESULT MSB equal one
OVR – Signed arithmetic overflow
C_{n+8} – CARRY OUT equal one
Z – RESULT equal zero

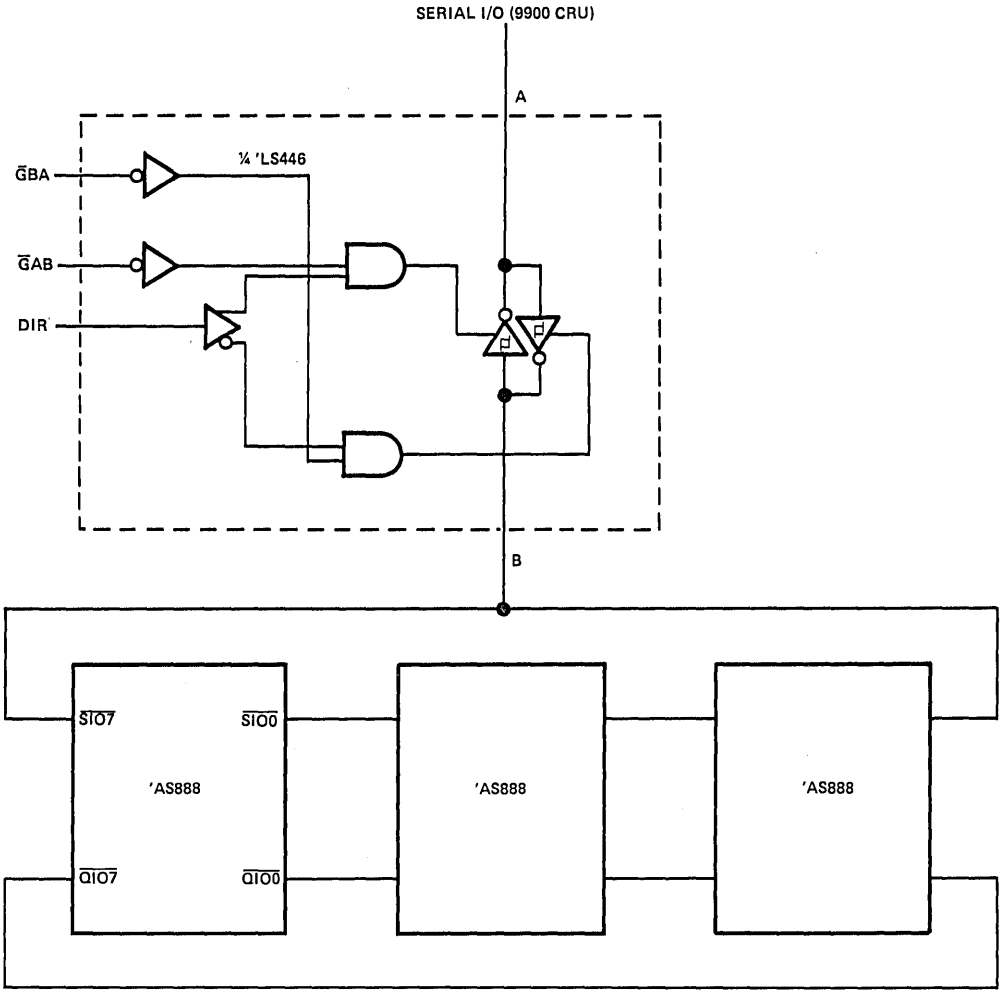


FIGURE 3 – SERIAL I/O

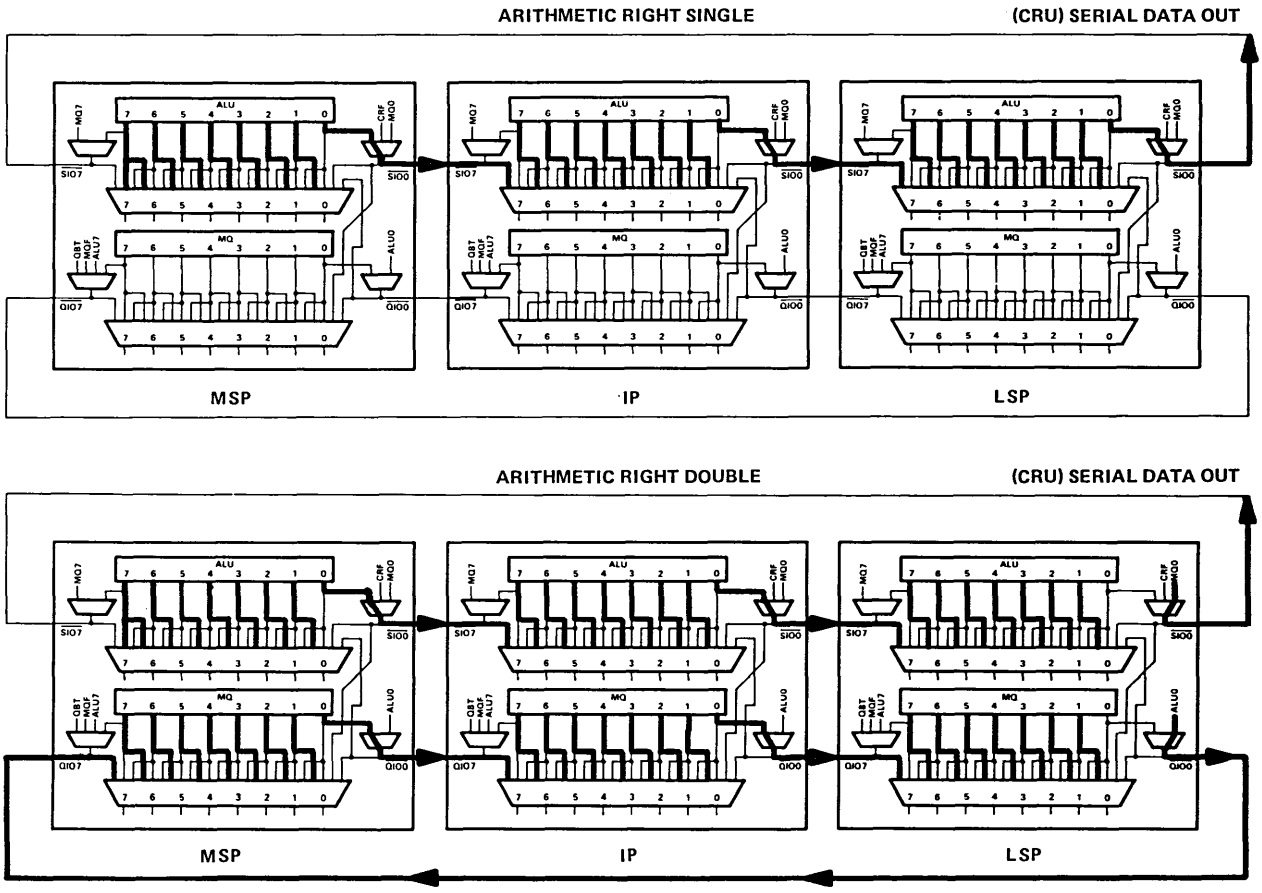


FIGURE 4 – SHIFT INSTRUCTIONS

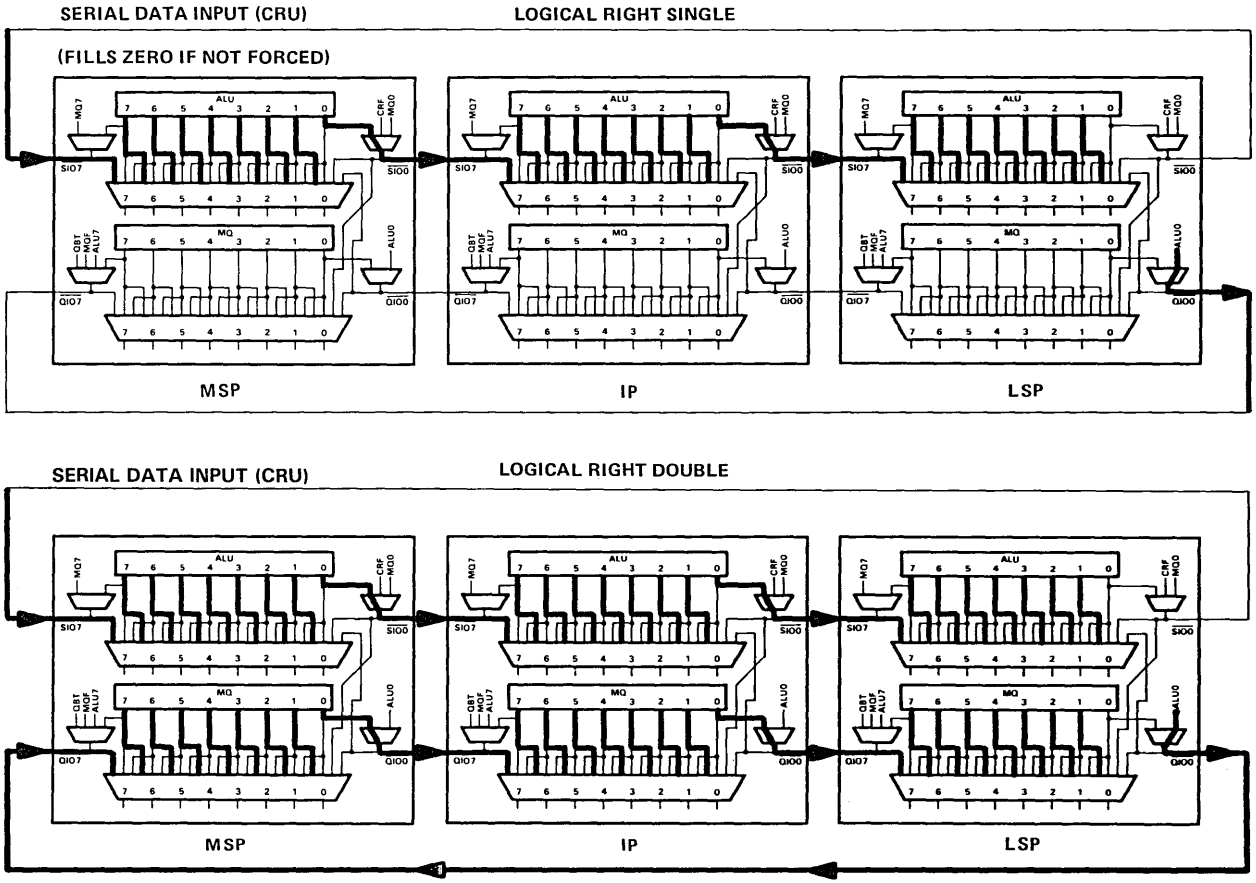


FIGURE 4 – SHIFT INSTRUCTIONS (Continued)

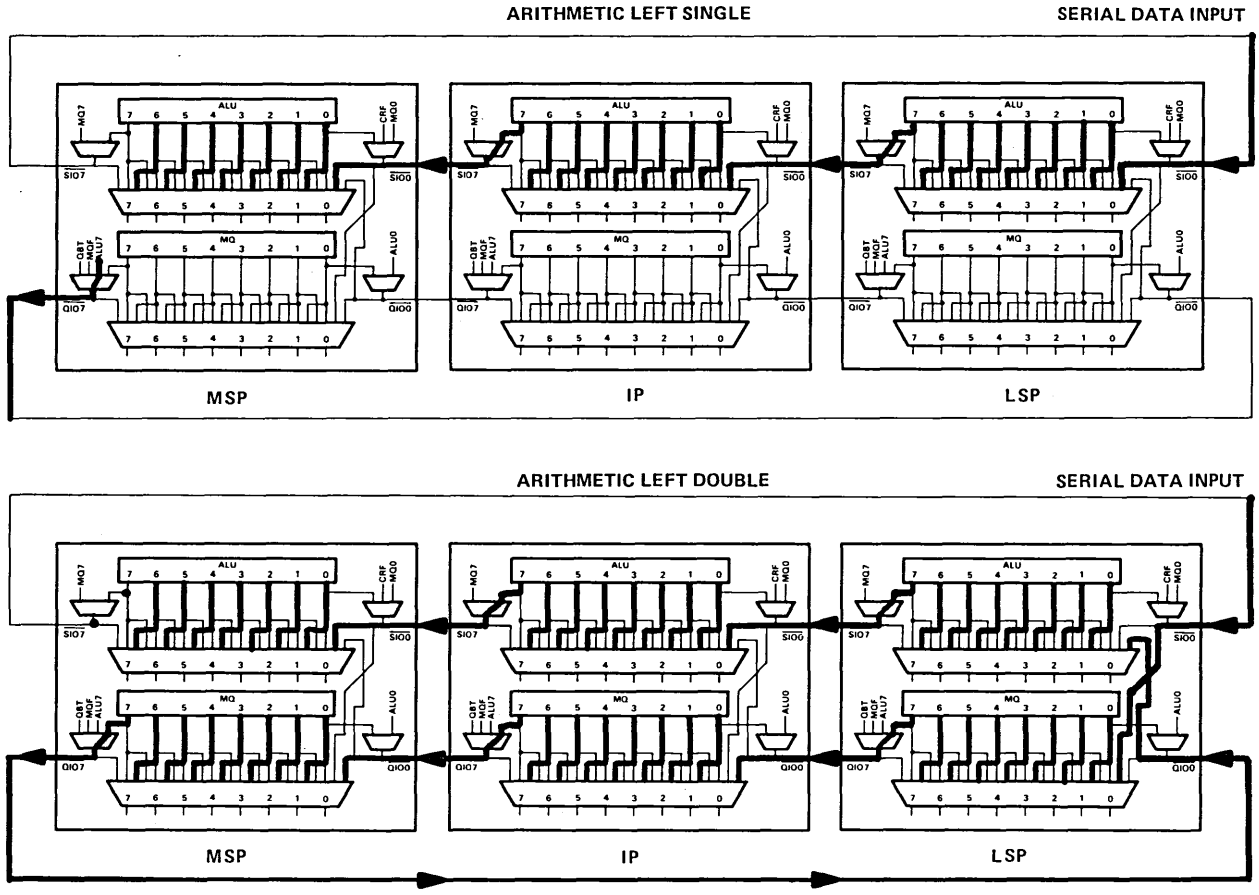
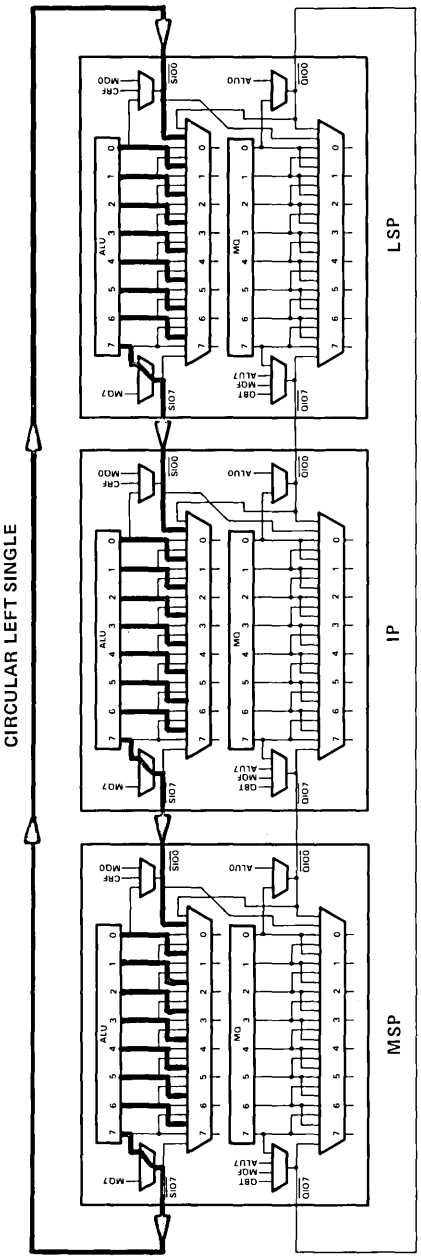


FIGURE 4 – SHIFT INSTRUCTIONS (Continued)



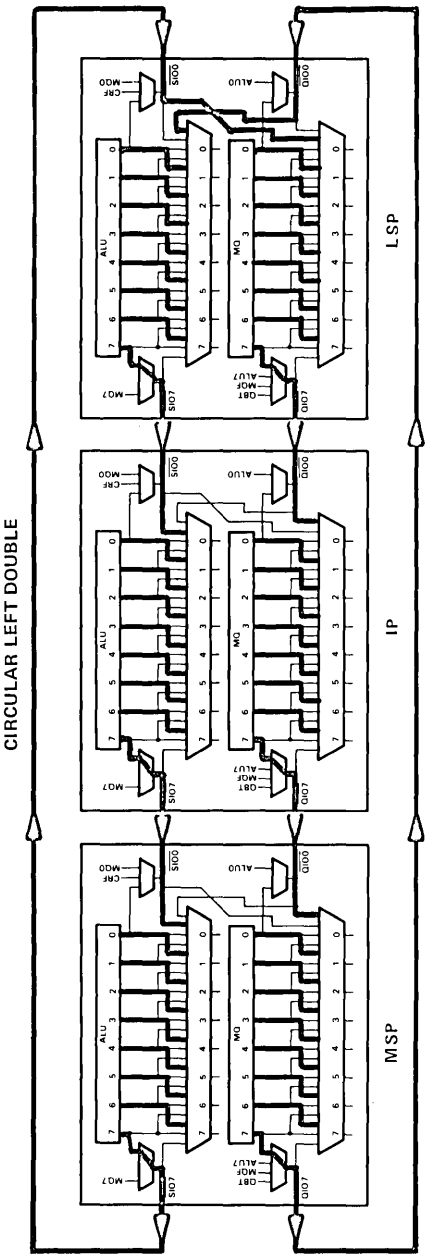


FIGURE 4 – SHIFT INSTRUCTIONS (Continued)

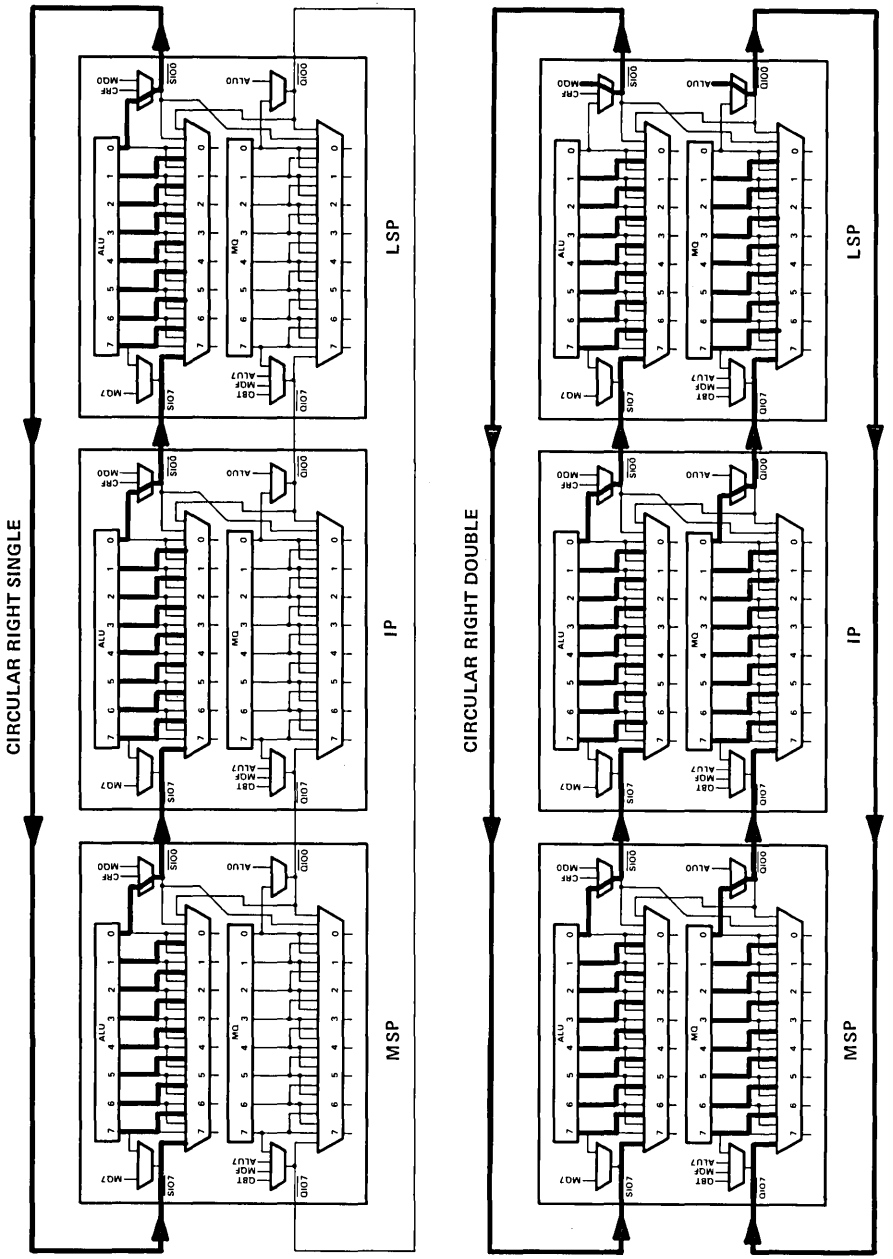


FIGURE 4 – SHIFT INSTRUCTIONS (Continued)

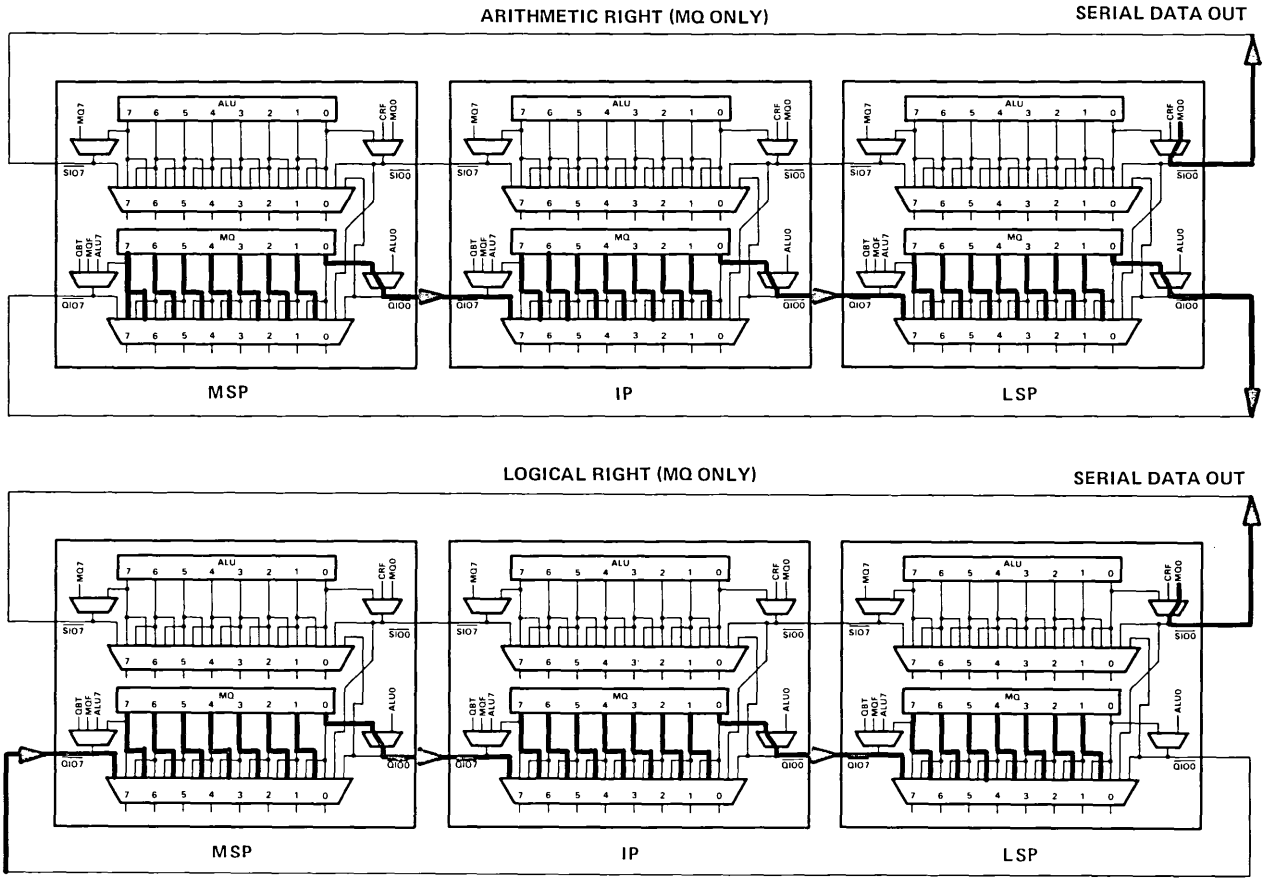


FIGURE 4 – SHIFT INSTRUCTIONS (Continued)

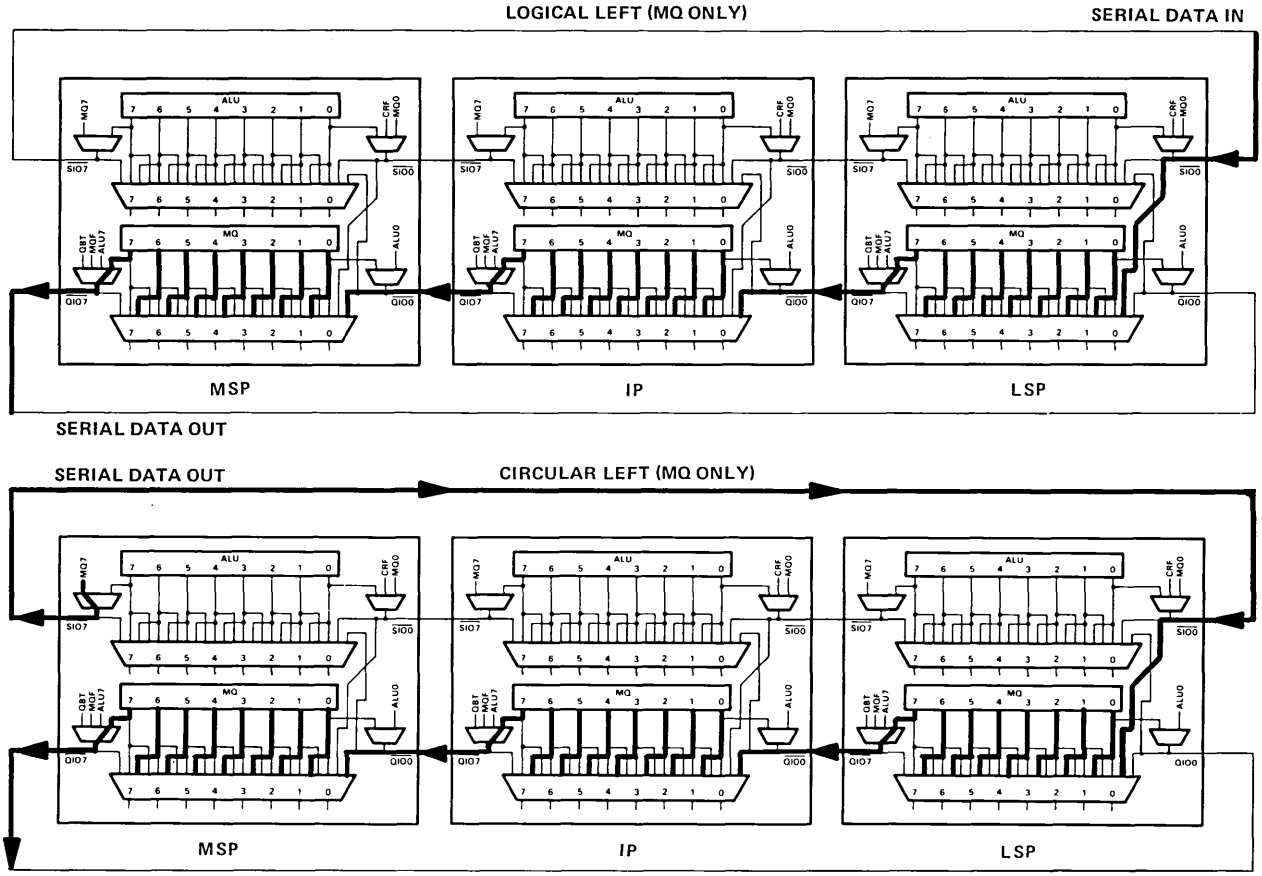


FIGURE 4 – SHIFT INSTRUCTIONS (Continued)

5. GROUP 3 INSTRUCTIONS

Hex code 8 of Group 1 instructions is used to access Group 3 instructions. Group 3 instructions are summarized in Table 7.

TABLE 7 – GROUP 3 INSTRUCTIONS

INSTRUCTION BITS (I7-I4) OP CODE (HEX)	MNEMONIC	FUNCTION
08	SET1	Set Bit
18	SET0	Reset Bit
28	TB1	Test Bit (one)
38	TB0	Test Bit (zero)
48	ABS	Absolute Value
58	SMTC	Sign Magnitude/Two's Complement
68	ADDI	Add Immediate
78	SUBI	Subtract Immediate
88	BADD	Byte Add R to S
98	BSUBS	Byte Subtract S from R
A8	BSUBR	Byte Subtract R from S
B8	BINCS	Byte Increment S
C8	BINCNS	Byte Increment Negative S
D8	BXOR	Byte XOR R and S
E8	BAND	Byte AND R and S
F8	BOR	Byte OR R and S

5.1 SET BIT INSTRUCTION (SET1): I7-I0 = 08_{16}

This instruction is used to force selected bits of a desired byte(s) to one (any combination of zero to eight bits). The desired bits are specified by an 8-bit mask (C3-C0)::(A3-A0)† consisting of register file address ports that are not required to support this instruction. All bits in the selected byte(s) that are in the same bit positions as ones in the mask are forced to a logical one. The B3-B0 address field is used for both source and destination of this instruction. The desired byte is specified by forcing SIO0 to a low value. Nonselected packages pass the byte thru unaltered. The S bus is the source word for this instruction.

CONDITION CODE

N	→	None (force to zero)
OVR	→	None (force to zero)
C_{n+8}	→	None (force to zero)
Z	→	RESULT equal zero

5.2 RESET BIT INSTRUCTION (SET0): I7-I0 = 18_{16}

This instruction is used to force selected bits of a desired byte(s) to zero (any combination of one to eight bits). The desired bits are specified by an 8-bit mask (C3-C0)::(A3-A0) consisting of register file address ports that are not required to support this instruction. All bits in the selected byte(s) that are in the same bit positions as ones in the mask are reset. The B3-B0 address field is used for both source and destination of this instruction. The desired byte is specified by forcing SIO0 to a low value. Nonselected packages pass the byte thru unaltered. The S bus is the source word for this instruction.

CONDITION CODE

N	→	None (force to zero)
OVR	→	None (force to zero)
C_{n+8}	→	None (force to zero)
Z	→	RESULT equal zero

1182 † The symbol '::' is concatenation operator.

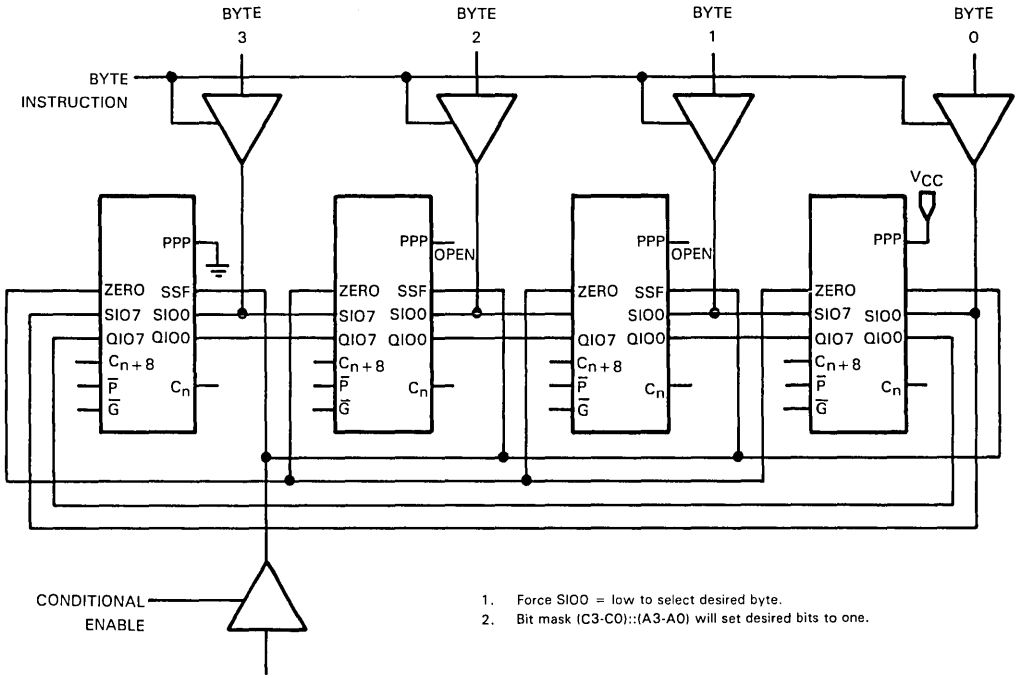


FIGURE 5 – SET BIT (OR RESET BIT) 'AS888 AND 'AS889

5.3 TEST BIT (ONE) INSTRUCTION (TB1): I7-I0 = 28_{16}

This instruction is used to test selected bits of a desired byte(s) (any combination of one to eight bits). Bits to be tested are specified by an 8-bit mask (C3-C0)::(A3-A0) consisting of register file address ports that are not required to support this instruction. Write Enable ($\overline{WE}$) is internally disabled during this instruction. The desired byte is specified by forcing SIO0 to a low value. The test will pass if the selected byte has zeroes at all bit locations specified by the one's of the mask. The S bus is the source word for this instruction.

CONDITION CODE

N	→	None (force to zero)
OVR	→	None (force to zero)
C_{n+8}	→	None (force to zero)
Z	→	Pass

5.4 TEST BIT (ZERO) INSTRUCTION (TB0): I7-I0 = 38_{16}

This instruction is used to test selected bits of a desired byte(s) (any combination of one to eight bits). Bits to be tested are specified by an 8-bit mask (C3-C0)::(A3-A0) consisting of register file address ports that are not required to support this instruction. Write Enable ($\overline{WE}$) is internally disabled during this instruction. The desired byte is specified by forcing SIO0 to a low value. The test will pass if the selected byte has one's at all bit locations specified by the one's of the mask. The S bus is the source word for this instruction.

CONDITION CODE

N	→	None (force to zero)
OVR	→	None (force to zero)
C_{n+8}	→	None (force to zero)
Z	→	Pass

1182

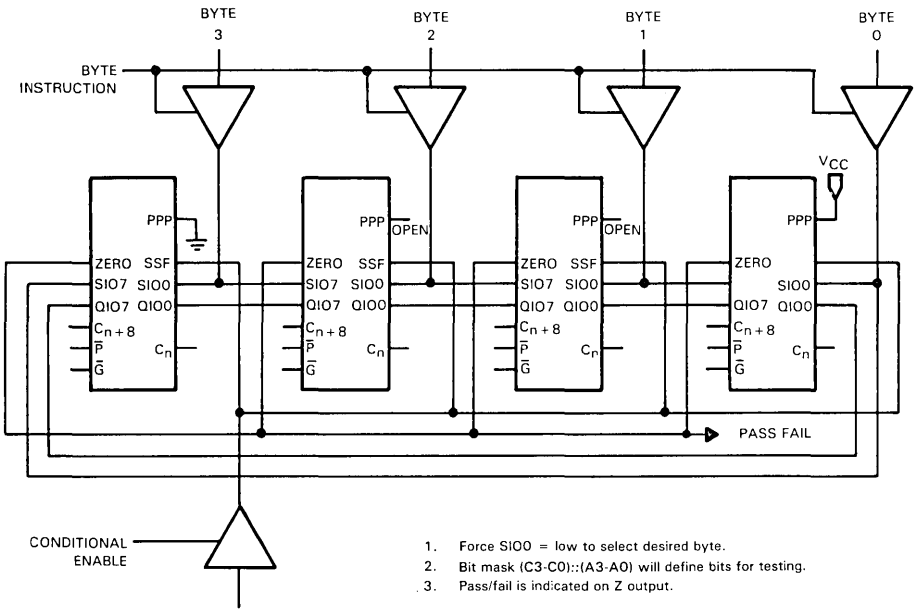


FIGURE 6 – TEST BIT 'AS888 AND 'AS889

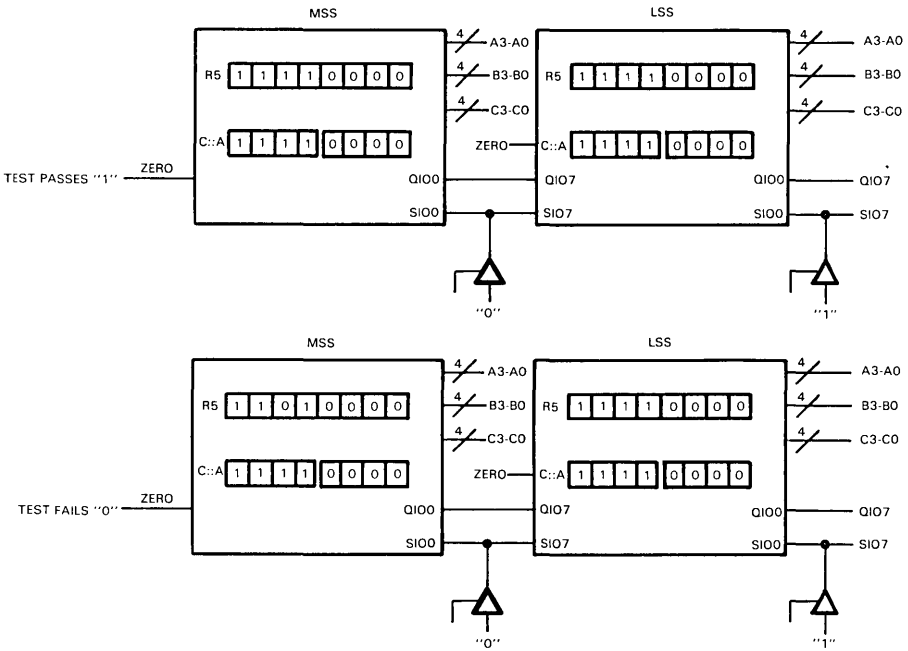


FIGURE 7 – TEST BIT ONE EXAMPLES

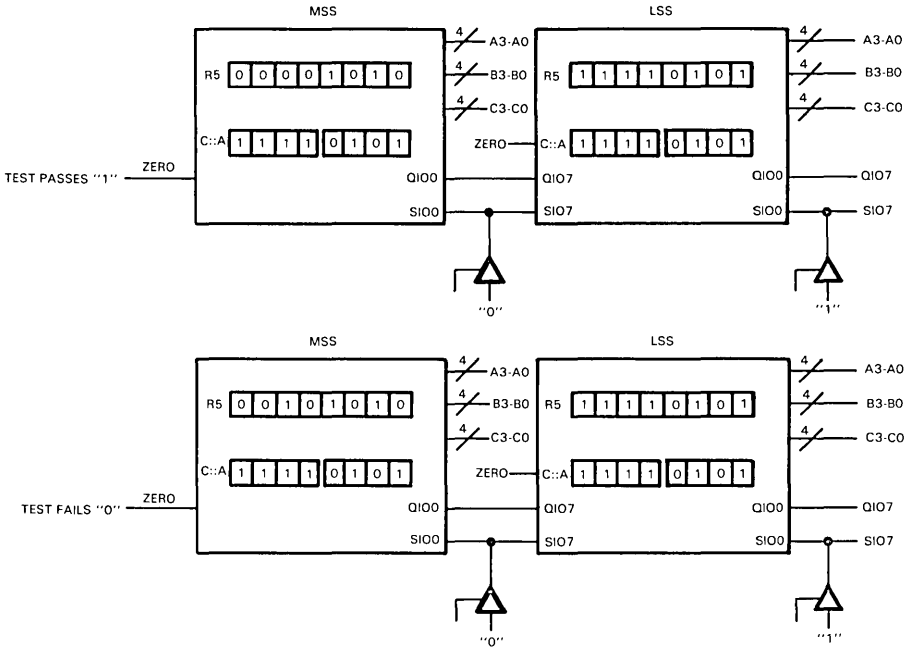


FIGURE 8 – TEST BIT ZERO EXAMPLES

5.5 ABSOLUTE VALUE INSTRUCTION (ABS): I7-I0 = 48_{16}

This instruction is used to convert two's complement numbers to their positive value. The operand placed on the S bus is the source for this instruction. The MSP will test the sign of the S bus and force the SSF pin tc the proper value. All other packages use the SSF pin as input to determine instruction execution (See Section 10.5 for special considerations involving the SSF pin).

CONDITION CODE

N	→	INPUT MSB equal one
OVR	→	INPUT equal 8000 (hex)
C_{n+8}	→	CARRY OUT equal one
Z	→	RESULT equal zero

5.6 SIGN MAGNITUDE/TWO'S COMPLEMENT INSTRUCTION (SMTC): I7-I0 = 58_{16}

This instruction allows conversion from two's complement representation to sign magnitude representation, or vice-versa, in one clock cycle. The operand placed on the S bus is the source for this instruction.

When the bit pattern 8000 (hex notation) is converted, the result is 0000 and the overflow condition (negative zero) the correct result is generated. Also, if the input is in two's complement notation, the overflow indicates an illegal conversion.

CONDITION CODE

N	→	RESULT MSB equal one
OVR	→	INPUT equal 8000 (hex)
C_{n+8}	→	INPUT equal 0000 (hex)
Z	→	RESULT equal zero

1182

5.7 ADD IMMEDIATE INSTRUCTION (ADDI): I7-I0 = 68_{16}

This instruction is used to add a specified constant value to the operand placed on the S bus. The constant will be between the values of 0 and 15. The constant value is specified by the un-used register file address (A port) not required to support this instruction. Forcing the carry input will add an additional one to the result.

(VALUE = A3-A0)

CONDITION CODE

N	→	RESULT MSB equal one
OVR	→	ARITHMETIC SIGNED OVERFLOW
C_{n+8}	→	CARRY OUT equal one
Z	→	RESULT equal zero

5.8 SUBTRACT IMMEDIATE INSTRUCTION (SUBI): I7-I0 = 78_{16}

This instruction is used to subtract a specified constant value from the operand placed on the S bus. The constant value is specified by the un-used register file address (A port) that is not required to support this instruction. The constant applied is the least significant four bits of a two's complement number. The device sign extends the constant over the entire word length. Therefore, the value of the constant is between -1_2 (1111) and -16_2 (0000) with $C_n=0$. Forcing $C_n=1_2$ adds one to each value, i.e., 0000 with $C_n=1_2$ adds -15_2 to the operand.

(VALUE = A3-A0)

CONDITION CODE

N	→	RESULT MSB equal one
OVR	→	ARITHMETIC SIGNED OVERFLOW
C_{n+8}	→	CARRY OUT equal one
Z	→	RESULT equal zero

5.9 BYTE INSTRUCTIONS

There are eight byte instructions included in Group 3 instructions. These instructions modify selected bytes of the operand selected on the S bus. A byte is selected by forcing SI00 to a low value (same as SET1, SET0, TB1, and TB0 instructions). Multiple bytes may be selected only if they are adjacent to one another.

NOTE: At least one byte must be nonselected during these instructions.

The nonselected bytes are passed through unaltered. Byte status is forced through the most-significant package except for the sign of the result (N), which is forced to zero (low).

CONDITION CODE

(Most-Significant Package)

N	→	None (force to zero)
OVR	→	BYTE signed overflow
C_{n+8}	→	BYTE carry out equal one
Z	→	BYTE result equal to zero

(Selected BYTES – other than MSP)

$\overline{G}$	→	Normal generate
$\overline{P}$	→	Normal propagate
C_{n+8}	→	Normal carry out
Z	→	RESULT equal to zero

(Nonselected BYTES – other than MSP)

$\overline{G}$	→	No generate (force to one)
$\overline{P}$	→	Propagate (force to zero)
C_{n+8}	→	C_n
Z	→	None (force to one)

6. GROUP 4 INSTRUCTIONS

Hex code 0 of Group 1 instructions is used to access Group 4 instructions. Group 4 instructions are summarized in Table 8.

TABLE 8 – GROUP 4 INSTRUCTIONS

INSTRUCTION BITS (I7-I0) OP CODE (HEX)	MNEMONIC	FUNCTION
00	CRC	Cyclic Redundancy Character Accumulation
10	SEL	Select S/R
20	SNORM	Single Length Normalize
30	DNORM	Double Length Normalize
40	DIVRF	Divide Remainder FIX
50	SDIVQF	Signed Divide Quotient FIX
60	SMULI	Signed Multiply Iterate
70	SMULT	Signed Multiply Terminate
80	SDIVIN	Signed Divide Initialize
90	SDIVIS	Signed Divide Start
A0	SDIVI	Signed Divide Iterate
B0	UDIVIS	Unsigned Divide Start
C0	UDIVI	Unsigned Divide Iterate
D0	UMULI	Unsigned Multiply Iterate
E0	SDIVIT	Signed Divide Terminate
F0	UDIVIT	Unsigned Divide Terminate

6.1 CYCLIC REDUNDANCY CHARACTER ACCUMULATION INSTRUCTION (CRC): I7-I0 = 00_{16}

Serial binary data which is transmitted over a channel is susceptible to error bursts. These bursts may be detected and corrected by standard encoding methods such as cyclic redundancy check codes, fire codes, or computer generated codes. These codes all divide the message vector by a generator polynominal to produce a remainder which contains parity information about the message vector. If a message vector of m bits (a(x)) is divided by a generator polynominal g(x) of order K-1, a K bit remainder r(x) is formed. The code vector c(x) consisting of m(x) and r(x) of length n = m + k is transmitted down the channel. The receiver divides the received vector by g(x). After m divide iterations, r(x) will be regenerated only if there is no error in the message bits. After K more iterations the result will be zero if and only if no error has occurred in either the message or the remainder.

The receiver performs the following operations (8N is the word length):

1) Load MQ with first 8N message bits of received vector c'(x).
2) Load Reg POLY with polynominal g(x).
3) Clear Reg SUM
4) CRC S port = SUM
   R port = POLY — Repeat 8N times
   F port = REMAINDER (Place into SUM)
5) Load MQ with next 8N digits.
6) Repeat steps 4 and 5 (n/8N-1) TIMES.
7) SUM now contains remainder r'(x) of c'(x).
8) Call syndrome generation routine if desired.

CONDITION CODE

N	→	None (force to zero)
OVR	→	None (force to zero)
C_{n+8}	→	None (force to zero)
Z	→	RESULT = zero

Note that the most significant bit of g(x) = $g^{k-1} \times^{k-1} + g^{k-2} \times^{k-2} + \cdots g^0 x^0$ is implied and that POLY (o) is set to zero if the length of g(x) requires less bits than are in the machine word width.

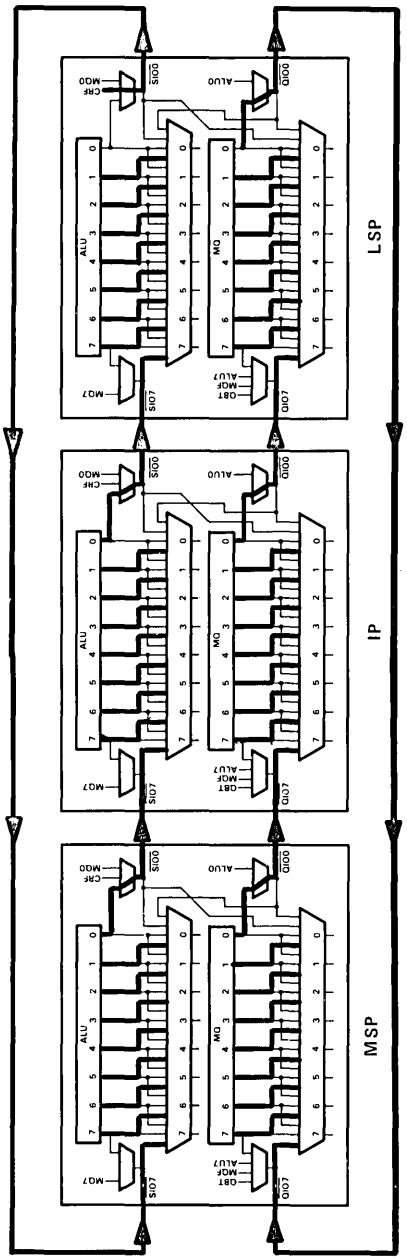


FIGURE 9 – CRC ACCUMULATION

6.2 SELECT S/R INSTRUCTION (SEL): I7-I0 = 10_{16}

This instruction is used to pass either the S bus or the R bus to the output depending on the state of the SSF input pin. Normally, the preceeding instruction would test the two operands and the resulting status information used to force the SSF input pin. SSF = 0 will output the R bus and SSF = 1 will output the S bus.

CONDITION CODE

N	→	RESULT MSB equal one
OVR	→	None (Force to zero)
C_{n+8}	→	None (Force to zero)
Z	→	RESULT equal zero

6.3 SINGLE-LENGTH NORMALIZE INSTRUCTION (SNORM): I7-I0 = 20_{16}

This instruction will cause the contents of the MQ register to shift toward the most-significant bit. Zeroes are shifted in via the QIOO input. The number of shifts performed can be counted and stored in one of the Register files by forcing a high at the C_n input. When the two most-significant bits are of opposite value, normalization is complete. This condition is indicated on the microcycle that completes the normalization at the OVF output. The same condition can be anticipated by testing the C_{n+8} output one microcycle sooner.

The chip contains conditional logic that inhibits the shift function (and also inhibits the register file increment) if the number within the MQ register is already normalized at the beginning of the instruction.

CONDITION CODE

N	→	MSB of result
OVR	→	MSB XOR 2nd MSB
C_{n+8}	→	CARRY OUT equal one
Z	→	RESULT equal zero

6.4 DOUBLE-LENGTH NORMALIZE INSTRUCTION (DNORM): I7-I0 = 30_{16}

This instruction will cause the contents of a double-length word (Register file contains the MS half and the MQ register contains the LS half), to shift toward the most-significant bit. Zeroes are shifted in via the QIOO input. When the two most-significant bits are of opposite value, normalization is complete. This condition is indicated on the microcycle that completes the normalization at the OVF output. The same condition can be anticipated by testing the C_{n+8} output one microcycle sooner.

The chip contains conditional logic which inhibits the shift function if the number is already normalized at the beginning of the instruction. The MS half of the operand must be placed on the S bus.

CONDITION CODE

N	→	MSB of result
OVR	→	MSB XOR 2nd MSB
C_{n+8}	→	None (Force to zero)
Z	→	RESULT equal zero

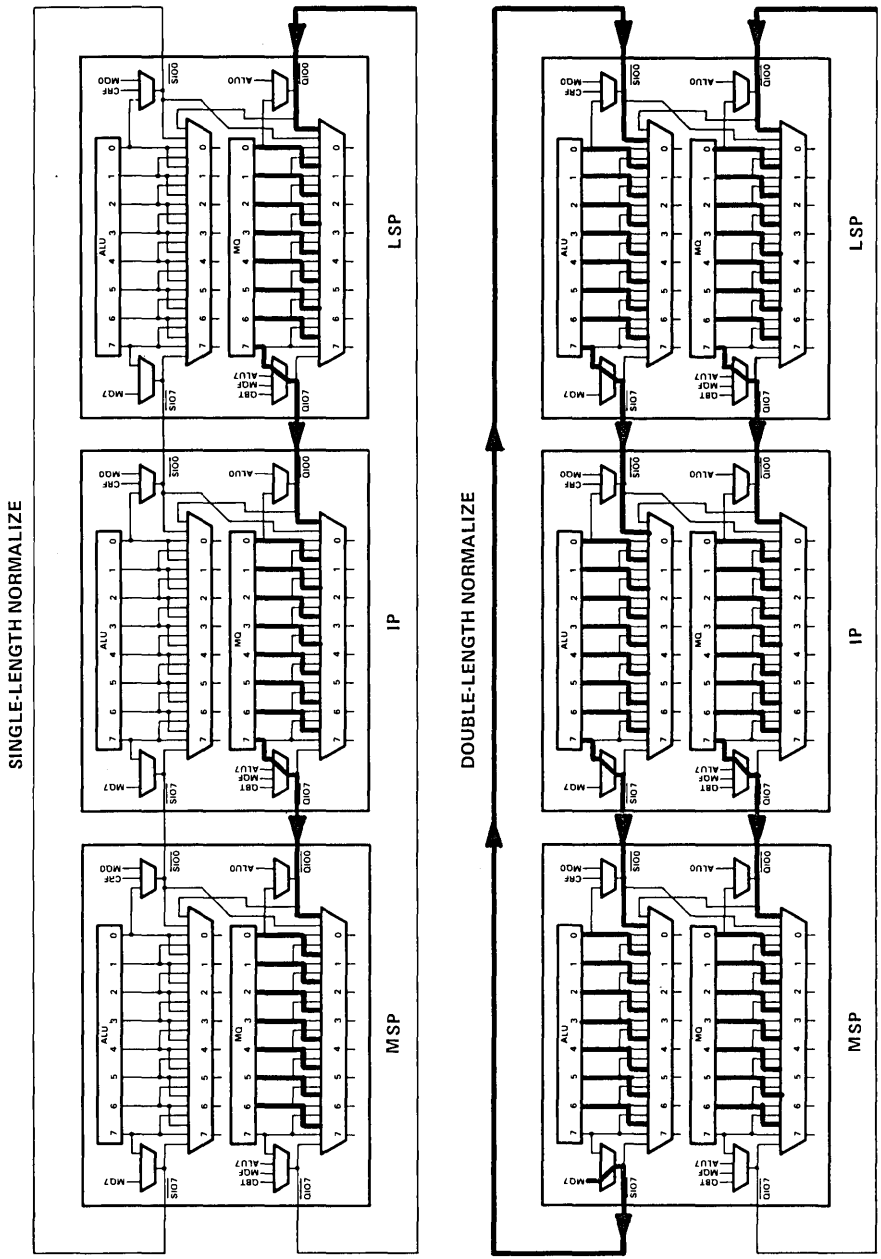


FIGURE 10 – SINGLE- AND DOUBLE-LENGTH NORMALIZE

6.5 MULTIPLY OPERATIONS

The ALU performs three unique types of N by N multiplies each of which produces a 2N-bit result. All three types of multiplication proceed via the following recursion:

P(J+1) = 2[P(J) = Multiplicand X M (8N-J)]

where P(J) = partial product at iteration number J

N = number of 'AS888 packages that are cascaded

P(J+1) = partial product at iteration number J+1

J varies from 0 to 8N [N = 2 for 16×16 multiply]

M (8N-J) = mode bit (unique to multiply type)

2 denotes some type of shift (unique to multiply)

Notice that by proper choice of mode terms and shifting operations signed, unsigned and mixed multiplies (signed times unsigned) may be performed.

All multiplies assume that the multiplier is stored in MQ before the operation begins (in the case of mixed multiply, the unsigned number must be the multiplier).

The processor has the following multiply instructions:

1. SIGNED MULTIPLY ITERATE (SMULI): I7-I0 = 60_{16}
2. SIGNED MULTIPLY TERMINATE (SMULT): I7-I0 = 70_{16}
3. UNSIGNED MULTIPLY ITERATE (UMULI): I7-I0 = $D0_{16}$

The signed multiply iterate (SMULI) instruction performs a signed times signed iteration. This instruction interprets M(8N-J) bit as the multiplier. The shift is a double-precision right shift one bit. This instruction is repeated 15 times for a 16×16 signed multiply. This instruction will also be used 16 consecutive times for a mixed multiplication.

The signed multiply terminate (SMULT) instruction provides correct (negative) weighting of the sign bit of a (negative) multiplier in signed multiplication. The instruction is identical to signed multiply iterate (SMULI) except that M(8N-J) is interpreted as −X8N (sign bit of the multiplier).

The unsigned multiply iterate (UMULI) performs an unsigned multiplication iteration. This instruction interprets M(8N-J) as the X(8N-J) bit of the multiplier. The shift is a double-precision right shift with the carry out from the [P(J)+Multiplicand X M(8N-J)] operation forced into bit 8N of P(J+1). This instruction is used in unsigned and mixed multiplication.

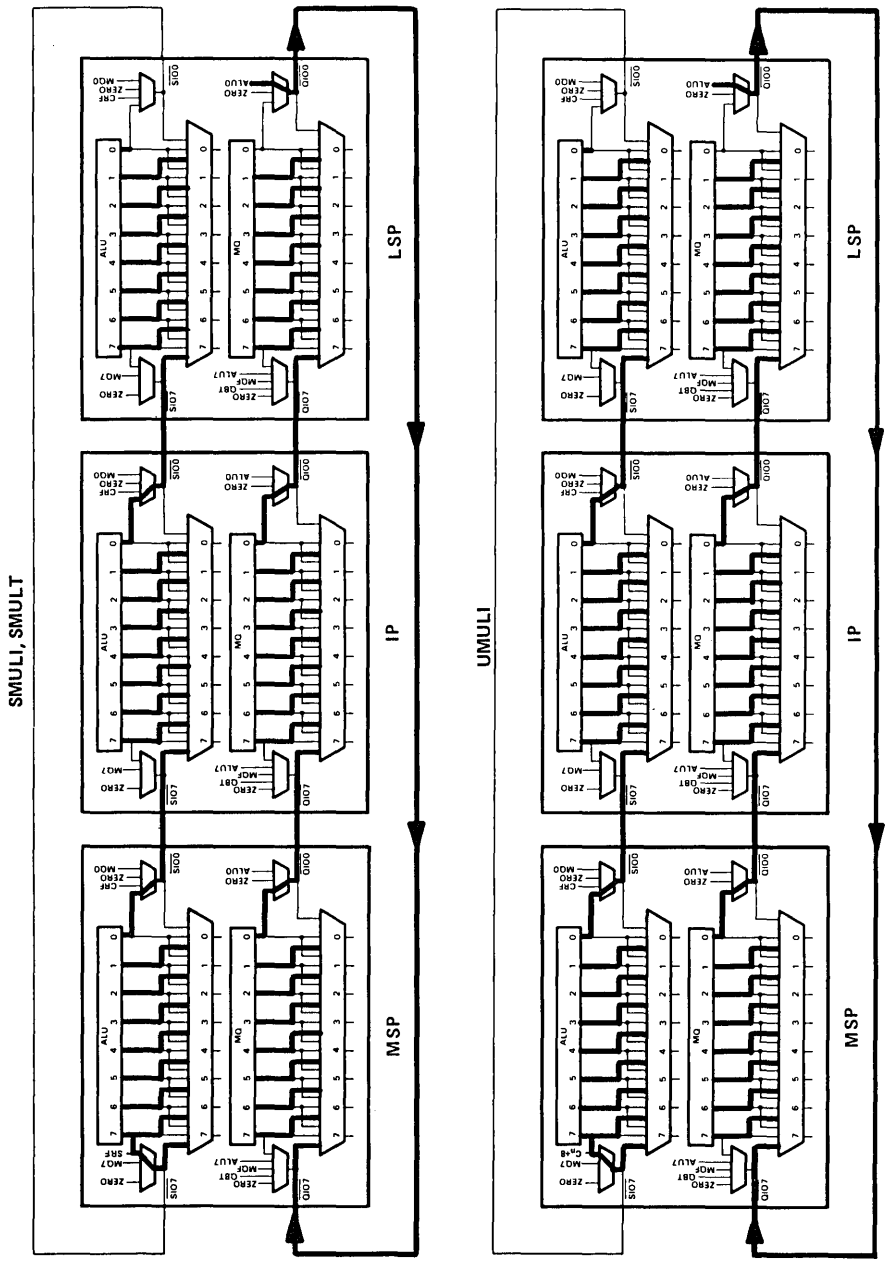


FIGURE 11 – MULTIPLICATION OPERATIONS

6.6 SIGNED MULTIPLICATION

Signed multiplication performs an 8N + 2 clock 2's complement multiply. The instructions necessary to produce an algebraically correct result proceed in the following manner:

Zero register to be used for accumulator

Load MQ with multiplier

SMULI (repeat 8N-1 times)	S port	=	Accumulator
	R port	=	Multiplicand
	F port	=	Iteration Result
SMULT	S port	=	Accumulator
	R port	=	Multiplicand
	F port	=	Product (MSH)

At completion, the accumulator will contain the 8N most-significant bits and the MQ contains the 8N least-significant bits of the product.

The status for the signed multiply iterate should not be used for any testing (overflow is not set by SMULI). The following status is set for the signed multiply terminate instruction:

N	→	RESULT MSB equal one
OVR	→	Forced to zero
C_{n+8}	→	Carry out equal to one
Z	→	Double precision result is zero

6.7 UNSIGNED MULTIPLICATION

Unsigned multiplication produces an unsigned times unsigned product in 8N + 2 clocks. The instructions necessary to produce an algebraically correct result proceed in the following manner:

Zero register to be used for accumulator

Load MQ with multiplier

UMULI 8N times)	S port	=	Accumulator
	R port	=	Multiplicand
	F port	=	Iteration result (product MSH on final result)

Upon completion, the accumulator will contain the 8N most-significant bits and the MQ contains the 8N least-significant bits of the product.

The status set by the unsigned multiply iteration is meaningless except on the final execution of the instruction. The status set by the unsigned multiply iteration instruction is as follows:

N	→	RESULT MSB equal one
OVR	→	Forced to zero
C_{n+8}	→	Carry out equal to one
Z	→	Double-precision result is zero

6.8 MIXED MULTIPLICATION

Mixed multiplication multiplies a signed multiplicand times an unsigned multiplier to produce a signed result in 8N + 2 clocks. The steps are as follows:

Zero register used for accumulator

Load MQ with unsigned multiplier

SMULI (8N times)

Upon completion, the accumulator will contain the 8N most-significant bits and the MQ contains the 8N least-significant bits of the product.

The following status is set by the last SMULI instruction:

N	–	RESULT MSB equal one
OVR	–	Forced to zero
C_{n+8}	–	Carry out equal to one
Z	–	Double-precision result is zero

6.9 DIVIDE OPERATIONS

The divide uses a nonrestoring technique to perform both signed and unsigned division of 16N bit integer dividend and a 8N bit integer divisor. It produces an 8N integer quotient and remainder.

The remainder and quotient will be such that the following equation is satisfied:

(Quotient) X (Divisor) + Remainder = Dividend

The processor has the following divide instructions:

1. UNSIGNED DIVIDE START (UDIVIS): I7-I0 = $B0_{16}$
2. UNSIGNED DIVIDE ITERATE (UDIVI): I7-I0 = $C0_{16}$
3. UNSIGNED DIVIDE TERMINATE (UDIVIT): I7-I0 = $F0_{16}$
4. SIGNED DIVIDE INITIALIZE (SDIVIN): I7-I0 = 80_{16}
5. SIGNED DIVIDE START (SDIVIS): I7-I0 = 90_{16}
6. SIGNED DIVIDE ITERATE (SDIVI): I7-I0 = $A0_{16}$
7. SIGNED DIVIDE TERMINATE (SDIVIT): I7-I0 = $E0_{16}$
8. DIVIDE REMAINDER FIX (DIVRF): I7-I0 = 40_{16}
9. SIGNED DIVIDE QUOTIENT FIX (SDIVQF): I7-I0 = 50_{16}

The unsigned divide iterate start (UDIVIS) instruction begins the iterate procedure while testing for overflow. Overflow is reported when the first subtraction of the divisor from the MSH of the dividend produces carry out. The test detects quotient overflow and divide by zero.

The unsigned divide iterate (UDIVI) instruction forms the quotient and remainder through iterative substract/add-shift operations of the divisor and dividend. One quotient bit is generated on each clock.

The unsigned divide iterate terminate (UDIVIT) instruction completes the iterate procedure generating the last quotient bit.

The signed divide initialize (SDIVIN) instruction prepares for iteration by shifting the dividend, and stores the sign of the dividend for use in the following instructions.

The signed divide iterate start (SDIVIS) instruction calculates the difference between the divisor and MSH of the dividend. Partial detection of overflow is also done during this instruction. Operations with like signs (positive quotient) and division by zero will overflow during this instruction (including zero divisor). Operations with unlike signs are tested for overflow during the signed divide quotient fix instruction (SDIVQF). Partial overflow results are saved and will be used during SDIVQF when overflow is reported.

The signed divide iterate terminate (SDIVIT) instruction completes the iterate procedure, generating the last quotient bit. It also tests for a remainder equal to zero, which determines the action to be taken in the following correction (fix) instructions.

The divide remainder fix (DIVRF) instruction corrects the remainder. If a zero remainder was detected by the previous instructions, the remainder is forced to zero. For non-zero remainder cases where the remainder and dividend have the same sign, the remainder is correct. When the remainder and dividend have unlike signs, a correction add/subtract of the divisor to the remainder is performed.

The signed divide quotient fix (SDIVQF) instruction corrects the quotient if necessary. This correction requires adding one to the incorrect quotient. An incorrect quotient results if the signs of the divisor and dividend differ and the remainder is non-zero. An incorrect quotient also results if the sign of the divisor was negative and the remainder is zero.

Overflow detection is completed during this instruction. Overflow may be generated for differing signs of the dividend and divisor. The partial overflow test result performed during SDIVIS is ORed with this test result to produce a true overflow indication.

6.10 SIGNED DIVIDE USAGE

The instructions necessary to perform an algebraically correct division of signed numbers are as follows:

Load MQ with the least-significant half of the dividend

SDIVIN	S port	=	MSH of dividend
	R port	=	Divisor
	F port	=	Intermediate result
SDIVIS	S port	=	Result of SDIVIN
	R port	=	Divisor
	F port	=	Intermediate result
SDIVI (8N-2 times)	S port	=	Result of SDIVIS (or SDIVI)
	R port	=	Divisor
	F port	=	Intermediate result
SDIVIT	S port	=	Result of last SDIVI
	R port	=	Divisor
	F port	=	Intermediate result
DIVRF	S port	=	Result of SDIVIT
	R port	=	Divisor
	F port	=	Remainder
SDIVQF	S port	=	MQ register
	R port	=	Divisor
	F port	=	Quotient

The status of all signed divide instructions except SDIVIN, DIVRF, and SDIVQF is as follows:

N	→	Forced to zero
OVR	→	Forced to zero
C_{n+8}	→	CARRY OUT equal to one
Z	→	Intermediate result is zero

The status of the SDIVIN instruction is as follows:

N	→	Forced to zero
OVR	→	Forced to zero
C_{n+8}	→	Forced to zero
Z	→	Divisor is zero

The status of the DIVRF instruction is as follows:

N	→	Forced to zero
OVR	→	Forced to zero
C_{n+8}	→	CARRY OUT equal to one
Z	→	Remainder is zero

The status of the SDIVQF instruction is as follows

N	→	Sign of quotient
OVR	→	Divide overflow
C_{n+8}	→	CARRY OUT equal to one
Z	→	Quotient is zero

The quotient is stored in the MQ register and the remainder is stored in the register file location that originally held the most significant word of the dividend. If fractions are divided, the quotient must be shifted right one bit, and the remainder right three bits to obtain the correct fractional representations.

The signed division algorithm is summarized in Table 9.

TABLE 9 – SIGNED DIVISION ALGORITHM

OP CODE	MNEMONIC	CLOCK CYCLES	INPUT S PORT	INPUT R PORT	OUTPUT F PORT
E4	LMQ	1	Dividend (LS Half)	–	Dividend (LS Half)
80	SDIVIN	1	Dividend (MS Half)	Divisor	Remainder (N)
90	SDIVIS	1	Remainder (N)	Divisor	Remainder (N)
A0	SDIVI	8N-2*	Remainder (N)	Divisor	Remainder (N)
E0	SDIVIT	1	Remainder (N)	Divisor	Remainder (Unfixed)
40	DIVRF	1	Remainder (Unfixed)	Divisor	Remainder
50	SDIVQF	1	MQ Register	Divisor	Quotient

* N – Number of 'AS888/'AS889 cascaded packages.

6.11 UNSIGNED DIVIDE USAGE

The instructions necessary to perform an algebraically correct division of unsigned numbers are as follows:

Load MQ with the least-significant half of the dividend

UDIVIS	S port	=	MSH of dividend
	R port	=	Divisor
	F port	=	Intermediate result
UDIVI	S port	=	Result of UDIVIS (OR UDIVI)
	R port	=	Divisor
	F port	=	Intermediate result
UDIVIT (8N-1 times)	S port	=	Result of last UDIVI
	R port	=	Divisor
	F port	=	Remainder (unfixed)
DIVRF	S port	=	Result of UDIVIT
	R port	=	Divisor
	F port	=	Remainder

The status of all unsigned divide instructions except UDIVIS is as follows:

N	→	Forced to zero
OVR	→	Forced to zero
C_{n+8}	→	CARRY OUT equal to one
Z	→	Intermediate result is zero

The status of the UDIVIS instruction is as follows:

N	→	Forced to zero
OVR	→	Divide overflow
C_{n+8}	→	CARRY OUT equal to one
Z	→	Intermediate result is zero

If fractions are divided, the remainder must be shifted right two bits to obtain the correct fractional representation. The quotient is correct as is. The quotient is stored in the MQ register at the completion of the divide.

The unsigned division algorithm is summarized in Table 10.

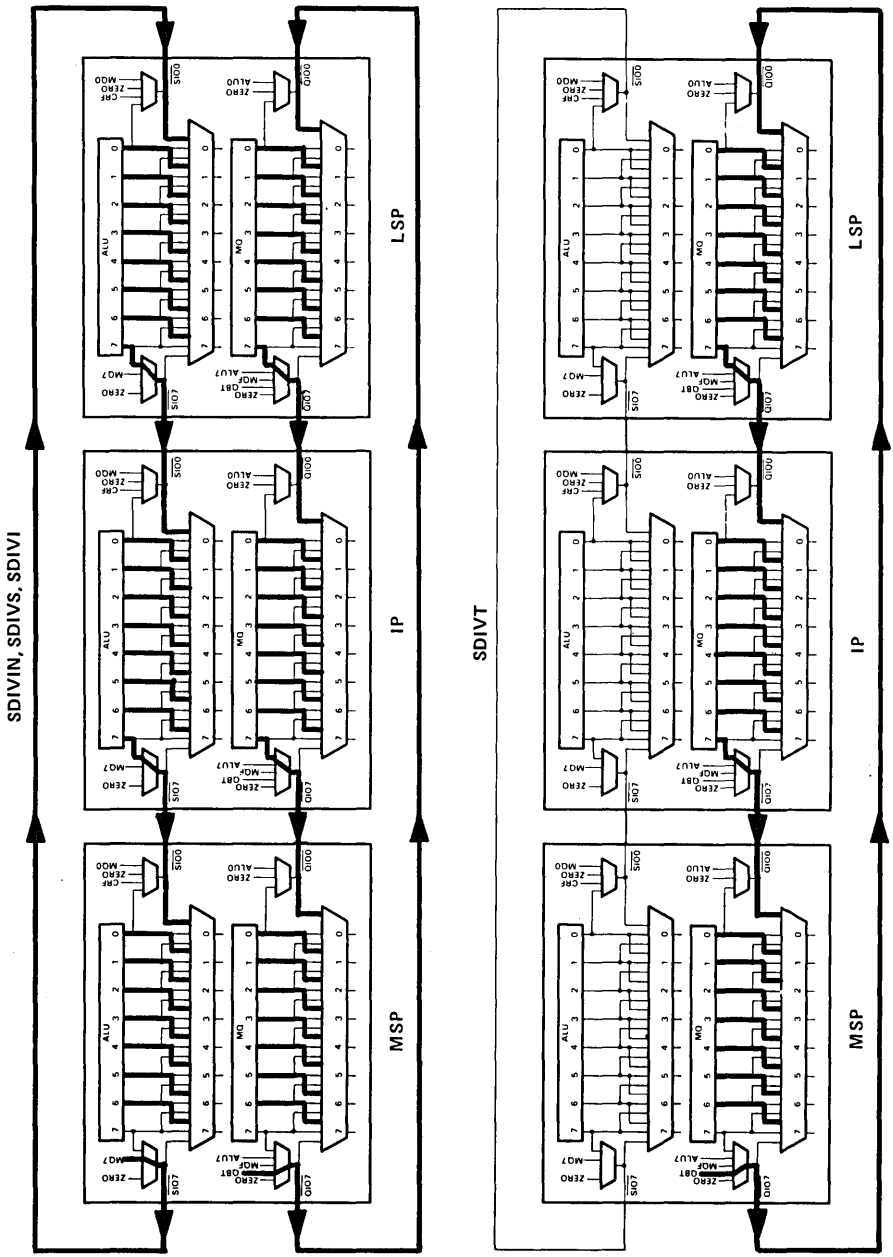


FIGURE 12 – DIVIDE OPERATIONS

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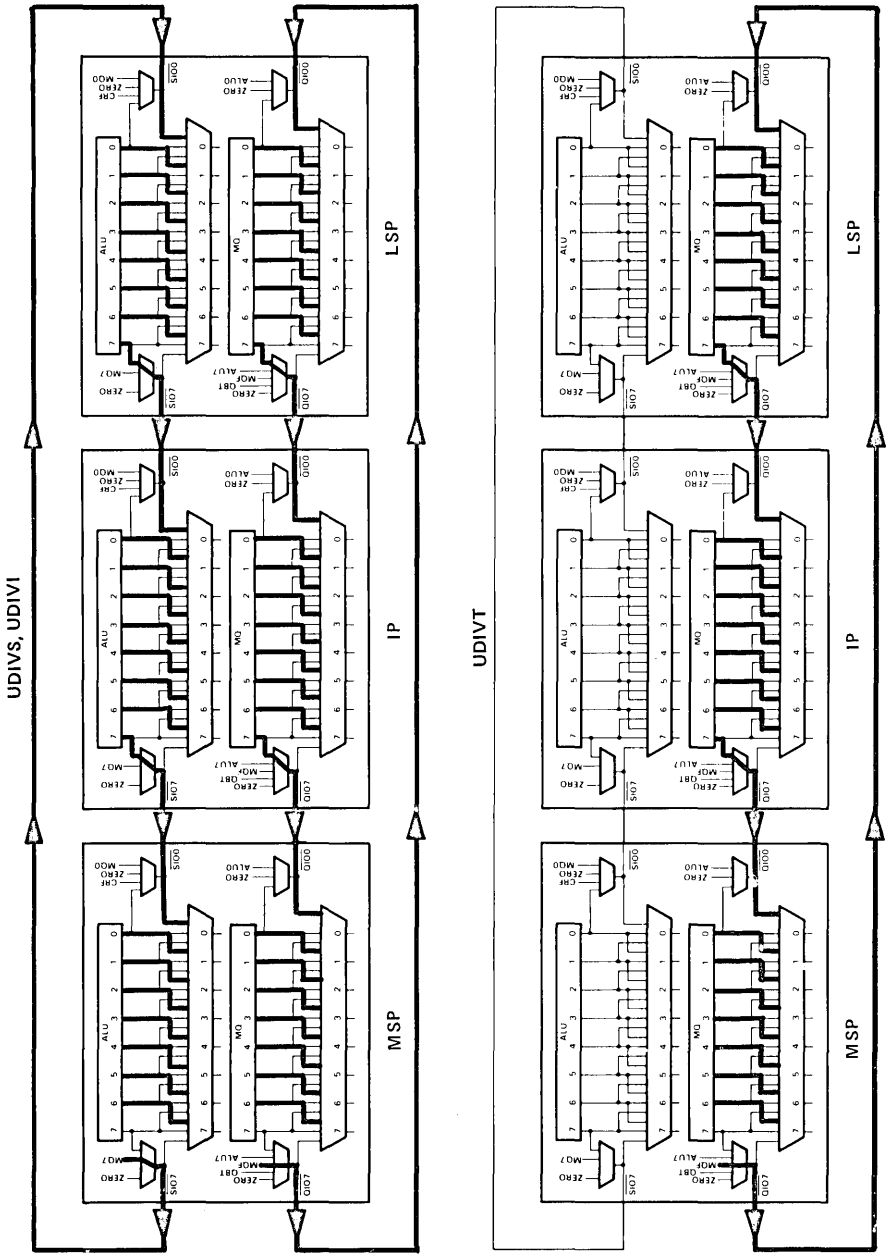


FIGURE 12 – DIVIDE OPERATIONS (Continued)

TABLE 10 – UNSIGNED DIVISION ALGORITHM

OP CODE	MNEMONIC	CLOCK CYCLES	INPUT S PORT	INPUT R PORT	OUTPUT F PORT
E4	LMQ	1	Dividend (LS Half)	–	Dividend (LS Half)
B0	UDIVIS	1	Dividend (MS Half)	Divisor	Remainder (N)
C0	UDIVI	8N-1*	Remainder (N)	Divisor	Remainder (N)
F0	UDIVIT	1	Remainder (N)	Divisor	Remainder (Unfixed)
40	DIVRF	1	Remainder (Unfixed)	Divisor	Remainder

*N = Number of 'AS888/'AS889 cascaded packages.

7. GROUP 5 INSTRUCTIONS

Hex code F of Group 1 instructions is used to access Group 5 instructions. Group 5 instructions are summarized in Table 11.

TABLE 11 – GROUP 5 INSTRUCTIONS

INSTRUCTION BITS (I7-I0) OP CODE (HEX)	MNEMONIC	FUNCTION
0F	CLR	Clear
1F	CLR	Clear
2F	CLR	Clear
3F	CLR	Clear
4F	CLR	Clear
5F	CLR	Clear
6F	CLR	Clear
7F	BCDBIN	BCD to Binary
8F	EX3BC	Excess-3 Byte Correction
9F	EX3C	Excess-3 Word Correction
AF	CLR	Clear
BF	CLR	Clear
CF	CLR	Clear
DF	BINEX3	Binary to Excess-3
EF	CLR	Clear
FF	NOP	No Operation

7.1 CLEAR INSTRUCTIONS (CLR)

There are eleven clear instructions listed in Table 11. The instructions force the ALU output to be zero and the BCD flip-flops to be cleared.

CONDITION CODE

N	→	None (force to zero)
OVR	→	None (force to zero)
C_{n+8}	→	None (force to zero)
Z	→	Active (one)

7.2 NO OPERATION INSTRUCTION (NOP): I7-I0 = FF_{16}

This instruction is identical to the clear instructions except that the BCD flip-flops retain their old value.

7.3 EXCESS-3 CORRECTION INSTRUCTIONS (EX3BC, EX3C)

There are two excess-3 correction instructions available:

1. Excess-3 byte correction (EX3BC): I7-I0 = $8F_{16}$
2. Excess-3 word correction (EX3C): I7-I0 = $9F_{16}$

One instruction supports the byte mode and the other supports the word mode. These instructions correct the excess-3 additions (subtractions) in either the byte or word mode. For correct excess-3 arithmetic, this instruction must follow each add/subtract. The operand must be on the S port.

NOTE: The previous arithmetic overflow should be ignored.

The status of the EX3C instruction is as follows:

CONDITION CODE

N	→	MSB or result
OVR	→	Signed overflow
C_{n+8}	→	CARRY OUT equal one
Z	→	None (Force to one)

The status of the EX3BC instruction is as follows:

CONDITION CODE

N	→	None (Force to zero)
OVR	→	Byte signed overflow
C_{n+8}	→	CARRY OUT equal one
Z	→	None (Force to one)

4

7.4 RADIX CONVERSIONS

Conversions between decimal and binary number representations are performed with the aid of two special instructions; BINEX3 and BCDBIN.

7.4.1 BCD To Binary Instructions (BCDBIN): I7-I0 = $7F_{16}$

This instruction allows the user to convert an N-digit BCD number to a 4N-bit binary number in 4N plus 4 clocks. This function sums the R bus, the S bus, and the CN bit, performs an arithmetic left shift on the ALU result, and simultaneously circular shifts the MQ left.

CONDITION CODE

N	→	MSB of result
OVR	→	Signed arithmetic overflow*
C_{n+8}	→	CARRY OUT equal one
Z	→	RESULT equal zero

*Overflow may be the result of an ALU operation or the arithmetic left shift operation.

The following code illustrates the BCD to binary conversion technique.

Let ACC be an accumulator register
Let NUM be the register which contains the BCD number
Let MSK be a mask register

```
M1:   LOADMQ NUM              ; LOAD MQ WITH BCD NUMBER
M2:   SUB ACC, ACC, SLCMQ     ; CLEAR ACC AND ALIGN MQ
M3:   SUB, MSK, MSK, SLCMQ    ; CLEAR MSK AND ALIGN MQ
M4:   SLCMQ                   ; ALIGN
M5:   SLCMQ                   ; ALIGN
M6:   ADDI ACC, MSK, 15(10)   ; MSK = 15(10)
L1:   AND MQ, MSK, R1, SLCMQ  ; EXTRACT ONE DIGIT
                              ; ALIGN MQ
L2:   ADD, ACC, R1, R1, SLCMQ ; ACC + DIGIT
                              ; IS STORED IN R1
                              ; ALIGN MQ
```

```
L3:     BCDBIN, R1, R1, ACC     ; 4 × ACC + 4 × DIGIT
                                ; IS STORED IN ACC
                                ; ALIGN MQ
L4:     BCDBIN, ACC, R1 ACC     ; 10 × ACC + 10 × DIGIT
                                ; IS STORED IN ACC
                                ; ALIGN MQ
                                ; REPEAT L1 THRU L4
                                ; N-1 TIMES
M7:     AND MQ, MSK, R1         ; FETCH LAST DIGIT
M8:     ACC + R1 → ACC          ; ADD IN LAST DIGIT
```

The previous code generates a binary number by executing the standard conversion formula for a BCD number (shown for 32 bits).

$$ABCD = ((A \times 10 + B) \times 10 + C) \times 10 + D$$

Notice that the conversion begins with the most-significant BCD digit and that the addition is performed in radix 2.

7.4.2 Binary To Excess-3 Instructions (BINEX3): I7-I0 = DF_{16}

This instruction allows the user to convert an N-bit binary number to a N/4-bit excess-3 number representation in 2N+3 clocks. The data on the R and S ports are summed with the MSB of the MQ register. The MQ register is simultaneously shifted left circularly.

CONDITION CODE

N	→	MSB of result
OVR	→	Signed arithmetic overflow
C_{n+8}	→	CARRY OUT equal one
Z	→	RESULT equal zero

The following illustrates the binary to excess-3 conversion technique.

Let NUM be a register containing an unsigned binary number
Let ACC be an accumulator

```
M1:     LOADMQ NUM              ; LOAD MQ WITH BINARY NUMBER
M2:     CLEAR ACC               ; CLEAR ACC
M3:     SET1 ACC H/33/          ; ACC ← HEX/3333 . . .
L1:     BINEX3 ACC, ACC, ACC    ; DOUBLE ACC AND ADD IN MSB OF MQ
                                ; ALIGN MQ
L2:     EX3C ACC                ; EXCESS 3 CORRECT
                                ; REPEAT L1 AND L2
                                ; N TIMES
```

The previous code generates an excess-3 number by executing the standard conversion formula for a binary number.

$$a_n 2^n + a_{n-1} 2^{n-1} + a_{n-2} 2^{n-2} + \ldots a_0 2^0 = [(2a_n + a_{n-1})2 + a_{n-2}]2 + \ldots a_0$$

Notice that the conversion begins with the most significant binary bit and that the addition is performed in radix-10 (excess-3).

8. DECIMAL ARITHMETIC

Decimal numbers are represented in excess-3 code. Excess-3 code numbers may be generated by adding three to each digit of a Binary Coded Decimal (BCD) number. The hardware necessary to implement excess-3 arithmetic is only slightly different from binary arithmetic. Carries from one digit to another during addition in BCD occur when the sum of the two digits plus the carry-in is greater than or equal to ten. If both numbers are excess-3, the sum will be excess-6, which will produce the proper carries. Therefore, every addition or subtraction operation may use the binary adder. To convert the result from excess-6 to excess-3, one must consider two cases resulting from a BCD digit add: (1) where a carry-out is produced, and (2) where a carry-out is not produced. If a carry-out is not produc- 1182

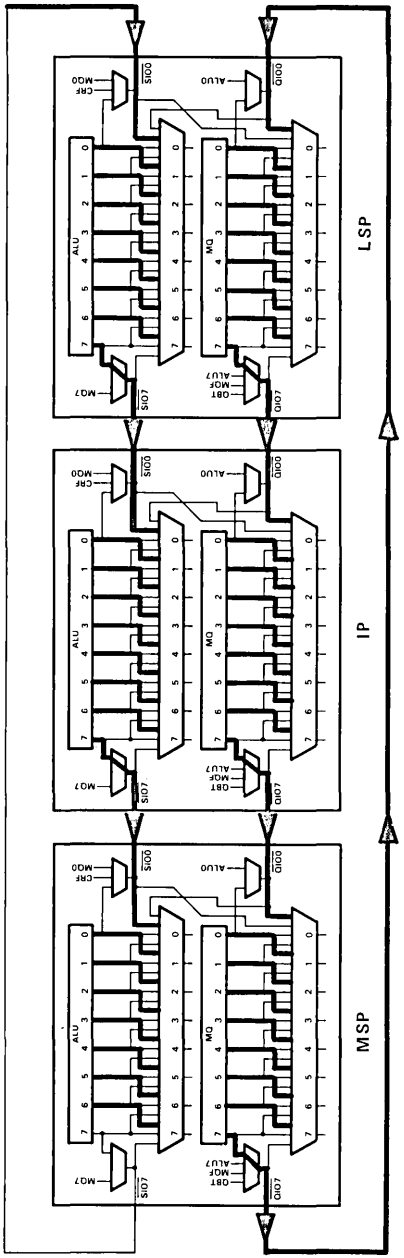


FIGURE 13 – BCD TO BINARY

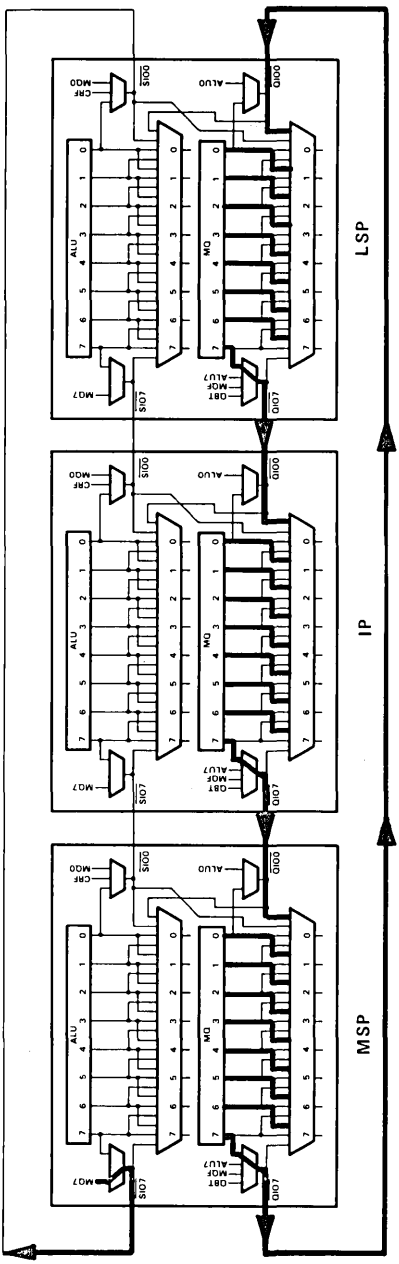


FIGURE 14 – BINARY TO EXCESS – 3

ed, three must be subtracted from the resulting digit. If a carry is produced, the digit is correct as a BCD number. For example, if BCD 5 is added to BCD 6, the excess-3 result would be 8+9 = 1 (with a carry). A carry rolls the number through the illegal BCD representations into a correct BCD representation. Binary 3 must be added to digit positions that produce a carry-out to correct the result to an excess-3 representation. Every addition and subtraction instruction stores the carry generated from each 4-bit digit location for use by the excess-3 correction functions. These correction instructions (word or byte) must be executed in the clock cycle immediately after the addition or subtraction operation.

Signed numbers may be represented in ten's complement form by complementing the excess-3 number. As an example, let's add the decimal number −423 to the decimal number 24, which will be represented by 8AA and 357 in excess-3 respectively.

8AA	
357	
C01	Sum
011	Carry
934	Excess-3 correct
−6CC	Complement
−399	Excess-3 to decimal

Complements of excess-3 numbers may be generated by subtracting the excess-3 number from an excess-3 zero followed by an excess-3 correct.

9. EXCESS-3 TO USASCII CONVERSION

Input/output devices or files represent numbers differently than high-speed central processing units. I/O devices handle all alphanumeric data similarly. CPU's handle more numeric data than alphabetic data and store numeric data in packed form to minimize calculation thoughput and reduce memory requirements. To represent the cost of a shirt that was $10.96, the I/O device would handle the six USASCII characters "$", "1", "0", ".", "9", "6", which would require 6 bytes of storage. In packed BCD, this number could be stored as 1046 in four bytes of data. The 'AS888/'AS889 may be programmed to perform data format conversions such as converting excess-3 BCD to USASCII.

The code below converts a packed word of excess-3 BCD to 2 unpacked words of USASCII code. Instruction "MAIN1" reads the input word from memory into Register 0 (R0). For illustrative purposes, suppose this data was 43C9, which represents the $10.96 shirt in excess-3 code. "MAIN2" and "MAIN3" generate a constant of $2D2D_{16}$, which is an offset constant to convert excess-3 numbers to USASCII. "MAIN4" copies R0 into R2 to set up the subroutine parameters and calls the subroutine "UNPACK". UNPACK2" strips off the upper byte leaving 00C9 in R2. "UNPACK2" and "UNPACK3" together shift the contents of R2 one character position and place and the result 0C90 into R3. "UNPACK4" performs a logical OR operation to produce 0CD9 in register 2. "UNPACK5" clears the most significant nibble in each byte to produce 0C09 in R2. "UNPACK6" adds the constant $2D2D_{16}$ to R2 to produce 3936 the ACSII representatation of the numerals 96 and returns program control to "MAIN5". "MAIN5" through "MAIN9" align the two remaining characters and call UNPACK and the process repeats. Finally the USASCII representation of 1096 is stored into memory. (Note that no attempt was made to pack the "$" or "." characters.)

Unpacking Excess-3 to USASCII:

```
MAIN1:   READ, RFA(0)                          ; READ IN PACKED EXCESS-3
MAIN2:   XOR, RFA(4), RFB(4), RFC(4)           ; CLEAR R4
MAIN3:   SET1, RFB(4), RDC(2), RFA(D), MSH, LSH ; GENERATE HEXIDECIMAL 2D2D16
MAIN4:   MOVE, RFA(0), RFC(2), JSR(UNPACK)     ; COPY RFA(0) INTO RFA(2), PROC CALL
MAIN5:   MOVE, RFA(2), RFC(1)                  ; TWO CHARACTERS IN R1
MAIN6:   ADDRS, RFB(0), RFA(0), RFC(0), SLC    ; R0 SHIFTED 2
MAIN7:   ADDRS, RFB(0), RFA(0), RFC(0), SLC    ; R0 SHIFTED 4
MAIN8:   ADDRS, RFB(0), RFA(0), RFC(0), SLC    ; R0 SHIFTED 6
MAIN9:   ADDRS, RFB(0), RFA(0), RFC(0), SLC,   ; R0 SHIFTED 8
         JSR (UNPACK)
MAIN10:  STORE, RFA(1)                         ; STORE USASCII, TWO CHARACTERS
                                               IN R2
MAIN11:  STORE, RFA(2)                         ; STORE USASCII
```

```
UNPACK1:  SET0, RFB(2), RFC(F), RFA(F), MSH        ; CLEAR MSH
UNPACK2:  ADDRS, RFB(2), RFA(2), RFC(3), SLC       ; SHIFT R2 TWO PLACES
UNPACK3:  ADDRS, RFB(3), RFA(3), RFC(3), SLC       ; SHIFT R3 TWO PLACES
UNPACK4:  OR, RFB(2), RFA(3), RFC(2)               ; OR R3 TO R2
UNPACK5:  SET0, RFB(2), RFC(F), RFA(0), LSH, MSH   ; CLEAR MOST SIGNIFICANT 4 BITS
                                                   IN EACH BYTE
UNPACK6:  ADDRS, RFB(2), RFB(4), RFC(2), RTS       ; ADD HEX 2D, RETURN
```

10. ELECTRICAL CHARACTERISTICS

10.1 ABSOLUTE MAXIMUM RATING OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

Supply voltage, V_{CC1} . . . . . 7 V
Supply voltage, V_{CC2} . . . . . 3 V
Input voltage . . . . . 7 V
High-level voltage applied to 3-state outputs . . . . . 5.5 V
Operating free-air temperature range: SN54AS' . . . . . −55 °C to 125 °C
SN74AS' . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

10.2 RECOMMENDED OPERATING CONDITIONS

			SN54AS'			SN74AS'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC1}	I/O supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{CC2}	STL internal logic supply voltage		1.8	2	2.2	1.8	2	2.2	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1			−1	mA
								−2.6†	
I_{OL}	Low-level output current	All outputs except $\overline{G}$			8			8	mA
		$\overline{G}$			16			16	
T_A	Operating free-air temperature		−55		125	0		70	°C

† The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.

Additional information on these products can be obtained from the factory as it becomes available.

10.3 ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

PARAMETER		TEST CONDITIONS		SN54AS'			SN74AS'			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC1} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC1} = 4.5 V,	I_{OH} = −1mA	2.4	3.4		2.4	3.4		V
		V_{CC1} = 4.75 V,	I_{OH} = −2.6 mA	2.4	3.4		2.4	3.4		
V_{OL}	All outputs except $\overline{G}$	V_{CC1} = 4.5 V,	I_{OL} = 8 mA			0.55			0.55	V
	$\overline{G}$	V_{CC1} = 4.5 V,	I_{OL} = 16 mA			0.55			0.55	
I_I		V_{CC1} = 5.5 V,	V_I = 7 V			100			100	μA
I_{IH}		V_{CC1} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	All inputs except $\overline{EA}$ and $\overline{OEB}$	V_{CC1} = 5.5 V,	V_I = 0.5 V			0.2			0.2	mA
	$\overline{EA}$ and $\overline{OEB}$	V_{CC1} = 5.5 V,	V_I = 0.5 V			0.4			0.4	
I_O§		V_{CC1} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{OZH}		V_{CC1} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC1} = 5.5 V,	V_O = 0.5 V			0.2			0.2	mA
I_{CC1}		V_{CC1} = 5.5 V	Outputs low		100			100		mA
			Outputs disabled							
I_{CC2}		V_{CC2} = 2.2 V	Outputs high							mA
			Outputs low		130			130		
			Outputs disabled							

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

10.4 TYPICAL SWITCHING CHARACTERISTICS

PARAMETER	FROM (INPUT)	TO (OUTPUT)										UNIT
		Y	C_{n+8}	$\overline{G}$,$\overline{P}$	Z	N	OVR	DA	DB	QI0	SI0	
t_{pd}	A3-A0, B3-B0	40	30	28	42	44	42	18	18	42	42	ns
	DA7-DA0, DB7-DB0	28	18	16	30	32	30	–	–	30	30	
	C_n	14	8	–	16	18	12	–	–	14	14	
	$\overline{EA}$	32	22	20	34	36	34	6	–	34	34	
	$\overline{EB}$	32	22	20	34	36	34	–	6	34	34	
	I7-I0	36	26	24	38	40	38	–	–	40	40	
	$\overline{OEB}$	–	–	–	–	–	–	–	6	–	–	
	$\overline{OEY}$	6	–	–	–	–	–	–	–	–	–	
	QI0 (n) Shift	10	–	–	12	14	–	–	–	–	–	
	SI0 (n) Shift	10	–	–	12	14	–	–	–	–	–	
	CK	40	30	28	42	44	42	18	18	42	42	

Additional information on these products can be obtained from the factory as it becomes available.

REGISTER FILE WRITE SETUP AND HOLD TIMES

PARAMETER		TYP	MAX	UNIT
t_{su}	C3-C0	8		ns
	DB†	14		
	I7-I4	16		
	I3-I0	22		
	$\overline{OEY}$	7		
	Y7-Y0	4		
	$\overline{WE}$	4		
t_h	C3-C0	0		
	DB†	0		
	I7-I4	0		
	I3-I0	0		
	$\overline{OEY}$	0		
	Y7-Y0	4		
	$\overline{WE}$	2		

†DB (during select instruction) through Y port.

Additional information on these products can be obtained from the factory as it becomes available.

10.5 SPECIAL INSTRUCTION SWITCHING CHARACTERISTICS

During various special instructions, the SSF pin is used to pass required information between the 'AS888 or 'AS889 packages which make up a total system.

For instance, during the multiplication process, the LSB of the multiplier determines whether an ADD/SHIFT or SHIFT operation is performed. During multiplication, the SSF pin of the least significant package (LSP) becomes an output pin while all other packages become input pins.

Similarly, during normalization, the required operation depends on whether the two data MSB's are the same or different. Therefore, during normalization the SSF pin of the most significant package (MSP) becomes an output pin while all other packages become input pins.

The following table lists the instructions which force the SSF pin during their execution. The propagation delay from various inputs are also shown. The parameter which limits normal system performance is indicated by an asterisk.

TABLE 12 – SSF PIN DELAYS AND SETUP TIMES

MNEMONIC	HEX CODE	SSF SOURCE		INPUT→SSF (ns)				SSF SETUP TIME (ns)
		LSP	MSP	C_n	$I_{(n)}$	CK	$B_{(n)}$	
CRC	00	X		–	18	17	26*	20
SNORM	20		X	–	18*	17	–	20
DNORM	30		X	–	18	26	26*	20
DIVRF	40		X	–	18*	17	–	20
SDIVQF	50		X	–	18*	17	–	18
SMULI	60	X		–	18*	17	–	0
SDIVIN	80		X	–	36	40	44*	0
SDIVIS	90		X	16*	36	40	44	0
SDIVI	A0		X	16*	36	40	44	0
UDIVIS	B0		X	12*	28	32	36	0
UDIVI	C0		X	12*	28	32	36	0
UMULI	D0	X		–	18*	17	–	0
SDIVIT	E0		X	16*	36	40	44	0
ABS	48		X	–	18	26	26*	20
SMTC	58		X	–	18	26	26*	20
BINEX3	DF		X	–	18*	17	–	18
LOADMQ (Arith)		X		14*	36	40	44	0
LOADMQ (Log)		X		–	28	32	36*	0
BADD	88	↑		16*	32	36	40	10
BSUBS	98	SOURCE		16*	32	36	40	10
BSUBR	A8	IS		16*	32	36	40	10
BINCS	B8	MOST		16*	32	36	40	10
BINCNS	C8	SIGNIFICANT		16*	32	36	40	10
BXOR	D8	BYTE		–	32	36	40*	10
BAND	E8	SELECTED		–	32	36	40*	10
BOR	F8			–	32	36	40*	10
EX3BC	8F	↓		–	32	36	40*	10

* This parameter limits normal system performance.

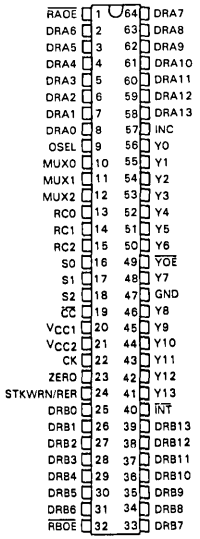
Additional information on these products can be obtained from the factory as it becomes available.

TYPES SN54AS890, SN54AS891, SN74AS890, SN74AS891 MICROSEQUENCERS

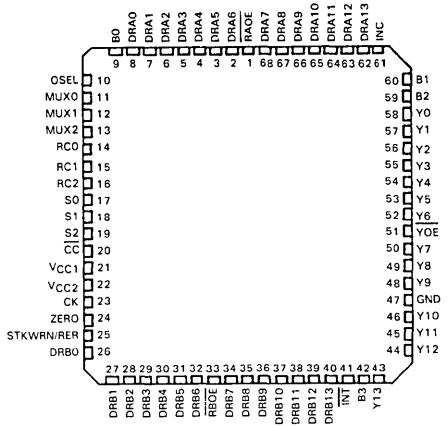
D2662 NOVEMBER 1982

- 14 Bits Wide – Addresses up to 16,384 Words of Microcode with One Chip
- Selects Address from One of Eight Sources
- STL-AS Technology
- Independent Read Pointer for Aid in Microcode Diagnostics
- Supports Real-Time Interrupts
- Two Independent Loop Counters
- Supports 64 Powerful Instructions
- Available in Popular 64-Pin DIP ('AS890) and in Space-Saving 68-Pin Chip Carrier ('AS891)
- Dependable Texas Instruments Quality and Reliability

SN54AS890, SN74AS890 . . . JD PACKAGE
(TOP VIEW)



SN54AS891, SN74AS891 . . . FN PACKAGE
(TOP VIEW)



description

The 'AS890 and 'AS891 are powerful microsequencers that are the result of the implementation of TI's Advanced Schottky and Schottky Transistor Logic. Approximately 2400 Schottky gate equivalents are used to construct this high-performance sequencer. The 'AS890 or 'AS891 can generate an address and provide register status in only 26 ns (preliminary data) while typically requiring only 1.5 watts of power. All internal STL logic in these devices operates on a 2-volt power supply that must be supplied externally. The information generated by the internal STL logic is communicated to the rest of the system via 5-volt Advanced Schottky TTL-compatible I/O ports.

The 'AS890 and 'AS891 select a 14-bit microaddress from one of eight sources to provide the proper microinstruction sequence for bit-slice processor or other microcode based systems. These high-performance devices are capable of addressing 16,384 control store memory locations either sequentially or via conditional branching algorithms. This multiway branching capability, coupled with a nine-word deep FILO (first in, last out) stack, allows the microprogrammer to arrange his code in blocks so that microprograms may be structured in the same fashion as such high-level languages as ALGOL, PASCAL, or ADA.

Both polled and real-time interrupt routines are supported by the 'AS890 and 'AS891 to enhance system throughput capability. Vectored interrupts may occur during any instruction, including PUSHes and POPs.

TEXAS INSTRUMENTS
INCORPORATED
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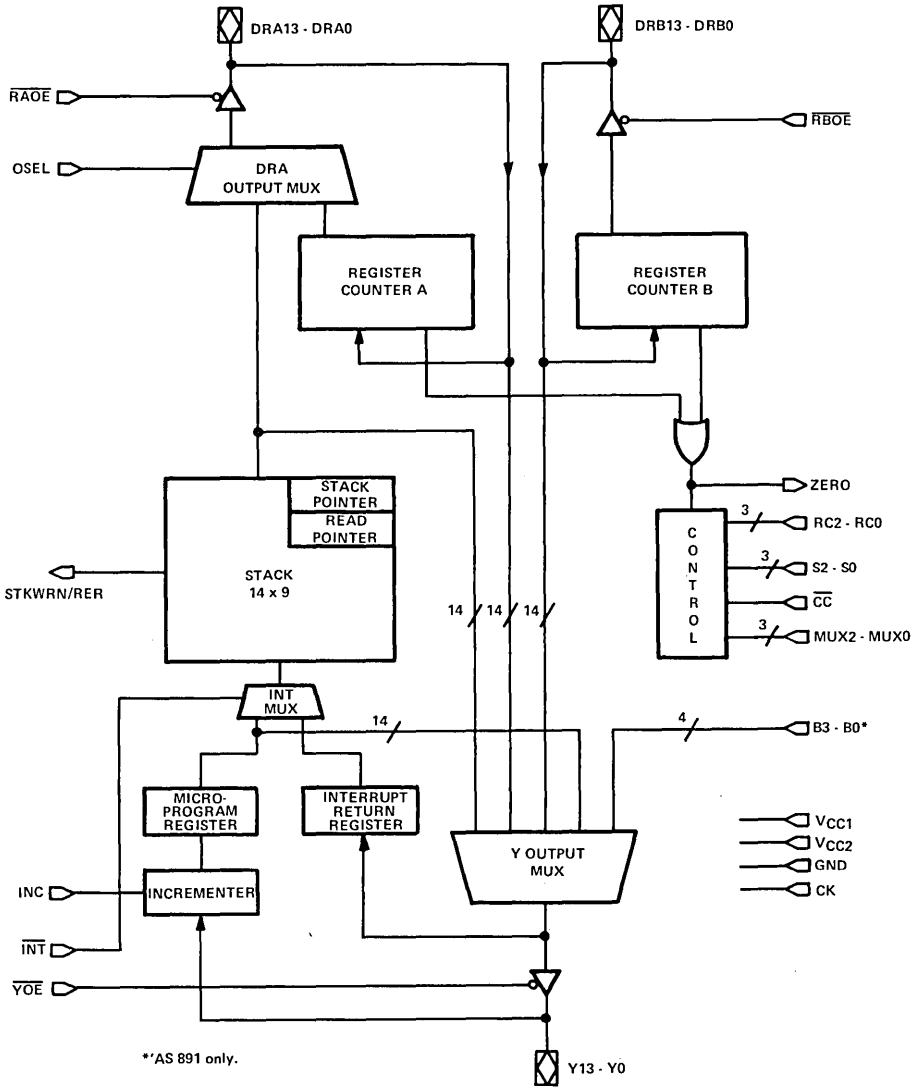
functional block diagram



TEXAS INSTRUMENTS
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pin descriptions

PIN NUMBER(S)		PIN NAME	I/O	PIN FUNCTION
'AS890	'AS891			
1	1	$\overline{RAOE}$	In	Enables DRA output, active low
2-8	2-8	DRA6-DRA0	In/Out	Seven LSBs of the A direct data I/O port
9	10	OSEL	In	MUX control for the source to DRA. Low selects RA, high selects stack.
10-12	11-13	MUX0-MUX2	In	MUX control for Y output bus (see Table 1)
13-15	14-16	RC0-RC2	In	Register/counter controls (see Table 3)
16-18	17-19	S0-S2	In	Stack control (see Table 2)
19	20	$\overline{CC}$	In	Condition code
20	21	V_{CC1}		5-volt supply for TTL compatible I/O
21	22	V_{CC2}		2-volt supply for internal STL
22	23	CK	In	Clock
23	24	ZERO	Out	Zero detect flag for register A and B
24	25	STKWRN/RER	Out	Stack overflow, underflow/read error flag
25-31	26-32	DRB0-DRB6	In/Out	Seven LSBs of the B direct data I/O port (0 = LSB)
32	33	$\overline{RBOE}$	In	Enables DRB output, active low
33-39	34-40	DRB7-DRB13	In/Out	Seven MSBs of the B direct data I/O port
40	41	$\overline{INT}$	In	Active low selects INT RT register to stack
41-46	43-46,48-49	Y13-Y8	In/Out	Six MSBs of bidirectional Y port
47	47	GND		Ground
48	50	Y7	In/Out	Seventh bit of bidirectional Y port
49	51	$\overline{YOE}$	In	Enables Y output bus, active low
50-56	52-58	Y6-Y0	In/Out	Seven LSBs of bidirectional Y port (0 = LSB)
57	61	INC	In	Incrementer control
58-64	62-68	DRA13-DRA7	In/Out	Seven MSBs of direct B data I/O port
	9,60,59,42	B0-B3	In	16-way branch inputs on 'AS891 only

description (continued)

Two 14-bit loadable registers/counters may be used for temporary storage of data or utilized as down counters for repetitive instructions such as multiplication and division or as loop counters when iterative routines are required.

The 'AS890 is available in a 64-pin sidebrazed DIP and the 'AS891 is available in a 68-pin chip carrier. The 68-pin version features a 4-bit port that appends four user-defineable bits to the DRA or DRB address value for support of 16-way branches for the execution of relative branch addressing schemes.

Y output multiplexer

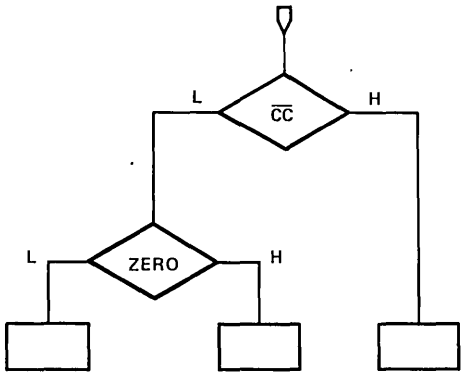
The Y output multiplexer of the 'AS890 or 'AS891 is capable of selecting the next branch address from one of eight locations. Addresses may be sourced from:

1. The top of the 14-bit by 9-word address stack
2. An external input on the DRA port, potentially a pipeline register
3. An external input on the DRB port, potentially a pipeline register
4. Internal register/counter A
5. Internal register/counter B
6. An internal microprogram counter (MPC register)
7. An external input onto the bidirectional Y output port
8. A 16-way branch – 4-bits appended to the DRA, DRB, A counter/register or B register/counter.

The source of the next address is dependent upon the previous state of the microsequencer, the MUX controls (MUX2-MUX0), the condition code ($\overline{CC}$) input, and the state of an internal status flag (status externally available at the ZERO output) that indicates that one of the on-chip registers is being decremented to zero.

The entire instruction set may be made conditional by manipulation of the condition code ($\overline{CC}$) input. Allowing the $\overline{CC}$ value to vary as a result of data or status provides for state-dependent or data-dependent branching. Unconditional branches may be achieved by forcing $\overline{CC}$ high when selecting control store addresses. Holding this pin low will provide for conditional or unconditional branches as dictated by the state of the zero-detect flag. The required control signals for selection of the Y output source are listed in Table 1. Note that the dependence of the 'AS890 and 'AS891 on two variables for conditional branches and jumps allows a conditional branch or conditional jump to subroutine in any clock cycle. Also note that all multiplexer inputs are overridden when all of the stack control inputs are pulled low. This instruction resets the stack and read pointers to zero and places all lines of the Y output bus at the low level.

TABLE 1 – Y OUTPUT CONTROL



MUX CONTROL			RESET*	Y OUTPUT SOURCE		Y OUTPUT SOURCE
MUX2	MUX1	MUX0		$\overline{CC}$ = L		$\overline{CC}$ = H
				ZERO = L	ZERO = H	
X	X	X	YES	ALL LOW	ALL LOW	ALL LOW
L	L	L	NO	STK	MPC	DRA
L	L	H	NO	STK	MPC	DRB
L	H	L	NO	STK	DRA	MPC
L	H	H	NO	STK	DRB	MPC
H	L	L	NO	DRA	MPC	DRB
H	L	H	NO	DRA' (16-WAY BRANCH)	MPC	DRB' (16-WAY BRANCH)
H	H	L	NO	DRA	STK	MPC
H	H	H	NO	DRB	STK	MPC

H = high level, L = low level, X = irrelevant.

* Reset command is implemented by setting S2-S0 = LLL.

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14-bit by 9-word address stack

The positive-edge-triggered 14-bit address stack supplies on-board storage of nine control store addresses that support up to nine nested levels of microsubroutine, looping, and real-time interrupt functions. The stack pointer (SP), which operates as an up-down counter, is updated after the execution of each PUSH operation and before each POP. In a PUSH operation, the address stored in the MPC register is loaded into the stack location addressed by the stack pointer, and the stack pointer is incremented. This address is available at the DRA port by enabling DRA ($\overline{RAOE}$ low and OSEL high).

A POP operation causes the stack pointer to be decremented on the first rising clock edge following the arrival of the POP instruction at the S2-S0 pins. The value that was indexed by the stack pointer is effectively removed from the top of the stack. All PUSH and POP instructions are conditionally dependent upon the stack control inputs (S2-S0), the condition code ($\overline{CC}$), the input value, and the zero-detect status. The desired option may be selected using the stack control inputs listed in Table 2.

TABLE 2 – STACK CONTROL

OSEL	S2	S1	S0	STACK OPERATION
X	L	L	L	RESET AND CLEAR SP AND RP
X	L	L	H	CLEAR SP AND RP IF $\overline{CC}$ = L AND ZERO = L
X	L	H	L	POP IF $\overline{CC}$ = H OR $\overline{CC}$ = L AND ZERO = H
X	L	H	H	POP IF $\overline{CC}$ = L AND ZERO = L
X	H	L	L	PUSH IF $\overline{CC}$ = H OR $\overline{CC}$ = L AND ZERO = H
X	H	L	H	PUSH IF $\overline{CC}$ = L AND ZERO = L
X	H	H	L	PUSH IF $\overline{CC}$ = H OR $\overline{CC}$ = L AND ZERO = L
H	H	H	H	HOLD SP AND READ
L	H	H	H	HOLD SP AND RP

The read pointer (RP) is a useful tool in debugging microcoded systems. A microprogrammer now has the ability to perform a nondestructive, sequential read of the stack contents from the DRA port. This capability provides the user with a method of backtracking through the address sequence to determine the cause of overflow without affecting program flow, the status of the stack-pointer or the internal data of the stack. Placing a high value on all of the stack inputs (S2-S0) and OSEL places the 'AS890 or 'AS891 into the read mode. At each low-to-high clock transition, the value pointed to by the read pointer is available at the DRA port and the read pointer is decremented. Microcode diagnostics are simplified by the ability of the 'AS890 or 'AS891 to sequentially dump the contents of its stack. The bottom of the stack is detected by monitoring the STKWRN/RER (stack warning/read error) pin. A high will appear when the stack contains one word and a READ instruction is applied to the S2-S0 pins. This signifies that the last address has been read. The stack pointer and stack contents are uneffected by the READ opertion. Under normal PUSH and POP operations the read pointer is updated with the stack pointer and contains identical information.

The STKWRN/RER pin alerts the system to a potential stack overflow or underflow condition. STKWRN/RER becomes active under two additional conditions. If seven of the nine stack locations (0-8) are full (the stack pointer is at 7) and a PUSH occurs, the STKWRN/RER pin will produce a high-level signal to warn that the stack is approaching its capacity, and will be full after one more PUSH. Knowledge that overflow potential exists allows bit-slice-based systems to continuously process real-time interrupt vectors. This signal will remain high, if HOLD, PUSH, or POP instructions occur, until the stack pointer is decremented to 7.

The user may be protected from attempting to POP an empty stack by monitoring STKWRN/RER before POP operations. A high level at this pin signifies that the last address has been removed from the stack (SP = 0). This condition remains until an address is pushed onto the stack and the stack pointer is incremented to one.

Clearing the stack and read pointer is accomplished by placing low levels onto the stack control lines (S2-S0). This function overrides all of the Y output MUX controls and places the Y bus into a low state.

register/counters

Two loadable 14-bit registers extend the looping and branching capabilities of the 'AS890 and 'AS891. Addresses may be loaded directy into register counter A (RA) and register counter B (RB) through the direct data ports DA13-DA0 and DB13-DB0. The values stored in these registers may either be held, decremented, or read as a result of the register control inputs (RC2-RC0), $\overline{\text{RAOE}}$, and $\overline{\text{RBOE}}$. All combinations of these functions are supported with the exception of a simultaneous decrement of both registers. Generation of iteration routines may be accomplished by loading RA and/or RB and operating them as a down counter. Loop termination is acknowledged by the ZERO output going high to indicate that a register contains a binary one and that a decrement is about to take place. Because of this facility, a "decrement and branch on loop" termination may be executed in the same clock cycle.

The contents of RA is accessable to the DRA port when OSEL is low and the output bus is enabled by $\overline{\text{RAOE}}$ being low. Data from RB is available when DRB is enabled by $\overline{\text{RBOE}}$ being low. Note that control of the registers is maintained while an external value is active on the DRA and DRB ports. A value being directed from the DRA and DRB busses to the output will not inhibit the decrement operation.

Register/counter controls are listed in Table 3.

4

TABLE 3 – REGISTER CONTROL

RC2	RC1	RC0	REG A	REG B
L	L	L	HOLD	HOLD
L	L	H	DEC	HOLD
L	H	L	LOAD	HOLD
L	H	H	DEC	LOAD
H	L	L	LOAD	LOAD
H	L	H	HOLD	DEC
H	H	L	HOLD	LOAD
H	H	H	LOAD	DEC

microprogram register and increment

The microprogram register (MPC) and the incrementer (INC) provide the means for generating the next microprogram address for sequential addressing operations. The MPC may be loaded with either the outgoing address on the Y bus or may receive an external address for processing interrupt vectors.

The current address on the Y bus is passed to the MPC at each rising clock edge, either unaltered (INC low) for repeating statements, or incremented by one (INC high) for addressing sequential control store locations.

The MPC may also be externally loaded for subroutine and interrupt functions. Taking $\overline{\text{YOE}}$ high and forcing the new address onto the bidirectional Y bus loads the MPC with the new address at the positive clock edge. This value may also be incremented prior to storage in the MPC for sequential addressing of subroutines or interrupt routines.

interrupts

Real-time vectored interrupt routines are supported for those applications where polling would impede system throughput. Any instruction, including PUSHes and POPs, may be interrupted. To process an interrupt, the following procedure should be followed:

1. The bidirectional Y bus is placed into the high-impedance state by forcing $\overline{\text{YOE}}$ high.
2. The interrupt entry point vector is then forced onto the Y bus and incremented to become the second microinstruction of the interrupt routine. This is accomplished by making INC high.

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3. At the following clock edge, the second microaddress is stored in the MPC and the interrupted address will be stored in the INT RT register which always contains the outgoing value on the Y bus. This edge also causes the processor to begin execution of the first instruction of the interrupt routine. This first instruction must PUSH the address stored in the INT RT register onto the stack so that the proper return linkage is maintained. This is accomplished by making $\overline{INT}$ low and performing a PUSH. If this instruction were to be interrupted, the process would be repeated and the proper return linkage preserved.

control inputs

A listing of the response of internal elements in the 'AS890 and 'AS891 to various control inputs is given in Table 4.

TABLE 4 – RESPONSE TO CONTROL INPUTS

PIN NAME	LOGIC LEVEL	
	HIGH	LOW
$\overline{RAOE}$	DRA output in high-Z state	DRA output is active
$\overline{RBOE}$	DRB output in high-Z state	DRB output is active
$\overline{YOE}$	Y output in high-Z state	Y output is active
$\overline{INT}$	MPC to stack	INT RT register to stack
OSEL	Stack to DRA buffer input	RA to DRA buffer input
INC	Adds one to Y output and stores in MPC	Passes Y output to MPC unaltered
MUX2-MUX0	Table 1	Table 1
S2-S0	Table 2	Table 2
RC2-RC0	Table 3	Table 3

instruction set

Sixty-four microsequencing instructions enable the 'AS890 and 'AS891 to generate micro-addresses for up to 16,384 locations. Any instruction can be made conditional depending upon the value of the externally applied condition code ($\overline{CC}$) and the value stored in either of the internal register/counters.

The required signals for selection of the Y output source were listed in Table 1. Suggested methods for implementing a few commonly used instructions are given in Table 5 and flowcharts showing execution examples are illustrated in Figure 1.

It should be noted that the term jump refers to a subroutine call that must be accompanied by a return instruction. The term branch implies that a deviation from the program flow is accomplished but no return is required.

TABLE 5 – 'AS890 AND 'AS891 INSTRUCTION SET

FUNCTION	MNEMONIC	MUX2	MUX1	MUX0	S2	S1	S0	CC	FIG
Continue	CONT	X	H	X	H	H	H	H	1A
Unconditional branch	BR	X	L	X	H	H	H	H	1B
Conditional branch (DEC disabled)	CBR	H	H	X	H	H	H	V	1C
Two-way branch (DEC enabled)	BR2W	H	L	L	H	H	H	V	1D
Conditional loop on stack (DEC enabled)	LOOPS	L	L	X	L	H	L	L	1E
Repeat (DEC disabled)	REPEAT	L	L	X	H	H	H	L	1F
Loop on stack with exit (DEC enabled)	LSWE	L	L	X	L	H	L	V	1G
Conditional jump to subroutine	CJSR	H	H	X	H	L	H	V	1H
Jump to subroutine (DEC disabled)	JSR	H	H	X	H	L	H	H	1I
Two-way jump to subroutine (DEC disabled)	JSR2W	H	L	L	H	H	L	V	1J
Repeat until (DEC disabled)	UNTIL	L	H	X	L	H	L	V	1K
Return from subroutine (DEC disabled)	RTS	L	H	X	L	H	H	L	1L
Conditional return from subroutine	CRTS	L	H	X	L	H	H	V	1M
Conditional return from subroutine or branch (DEC enabled)	CRTSB	L	H	X	L	H	H	V	1N
Conditional branch and PUSH (DEC enabled)	CBRP	H	H	X	H	L	H	V	1O
Conditional branch and POP (DEC disabled)	CBRPO	H	H	X	L	H	H	V	1P
PUSH and continue	PUSH	L	H	X	H	X	L	H	1Q
POP and continue	POP	L	H	X	L	H	L	H	1R
Exit from loop	EXITLP	L	L	X	L	H	L	V	1S
Reset and clear stack/read pointer	RESET	X	X	X	L	L	L	X	1T
32-way branch (DEC disabled)	BR32W	H	L	H	H	H	H	V	1U
Execute n times (DEC enabled)	NEX	L	L	X	L	H	L	L	1V

H = high level, L = low level, X = irrelevant, V = varies (condition code value is dependent upon machine and data status and will vary accordingly).

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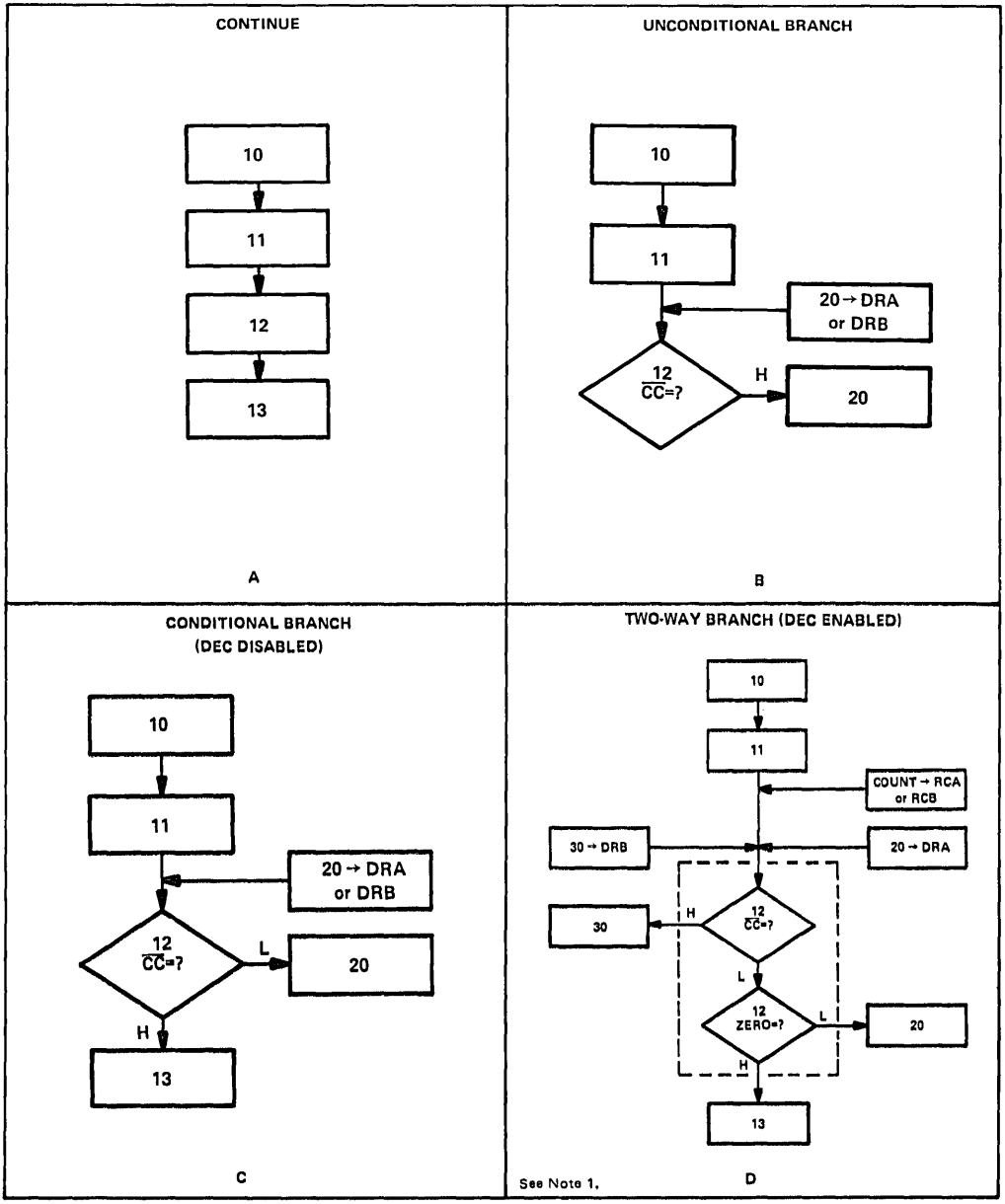
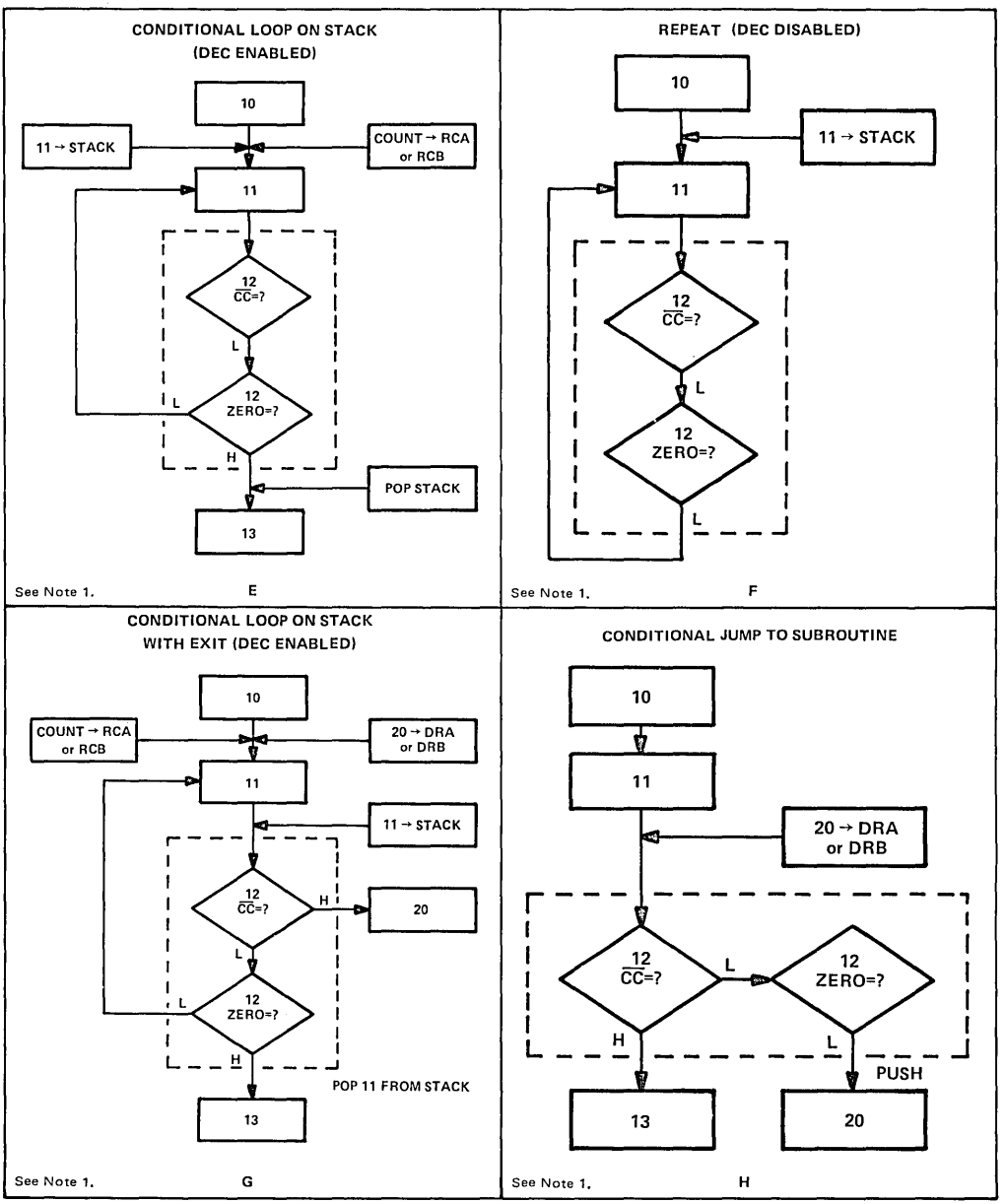


NOTES: 1. $\overline{CC}$ and ZERO are completed in the same clock cycle.
2. The least significant four bits of these addresses will be stripped off and four new bits appended to them from the B3-B0 port on 'AS891 only.

FIGURE 1 – 'AS890 AND 'AS891 INSTRUCTION SET FLOWCHARTS

1182



NOTES: 1. $\overline{CC}$ and ZERO are completed in the same clock cycle.
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FIGURE 1 – 'AS890 AND 'AS891 INSTRUCTION SET FLOWCHARTS

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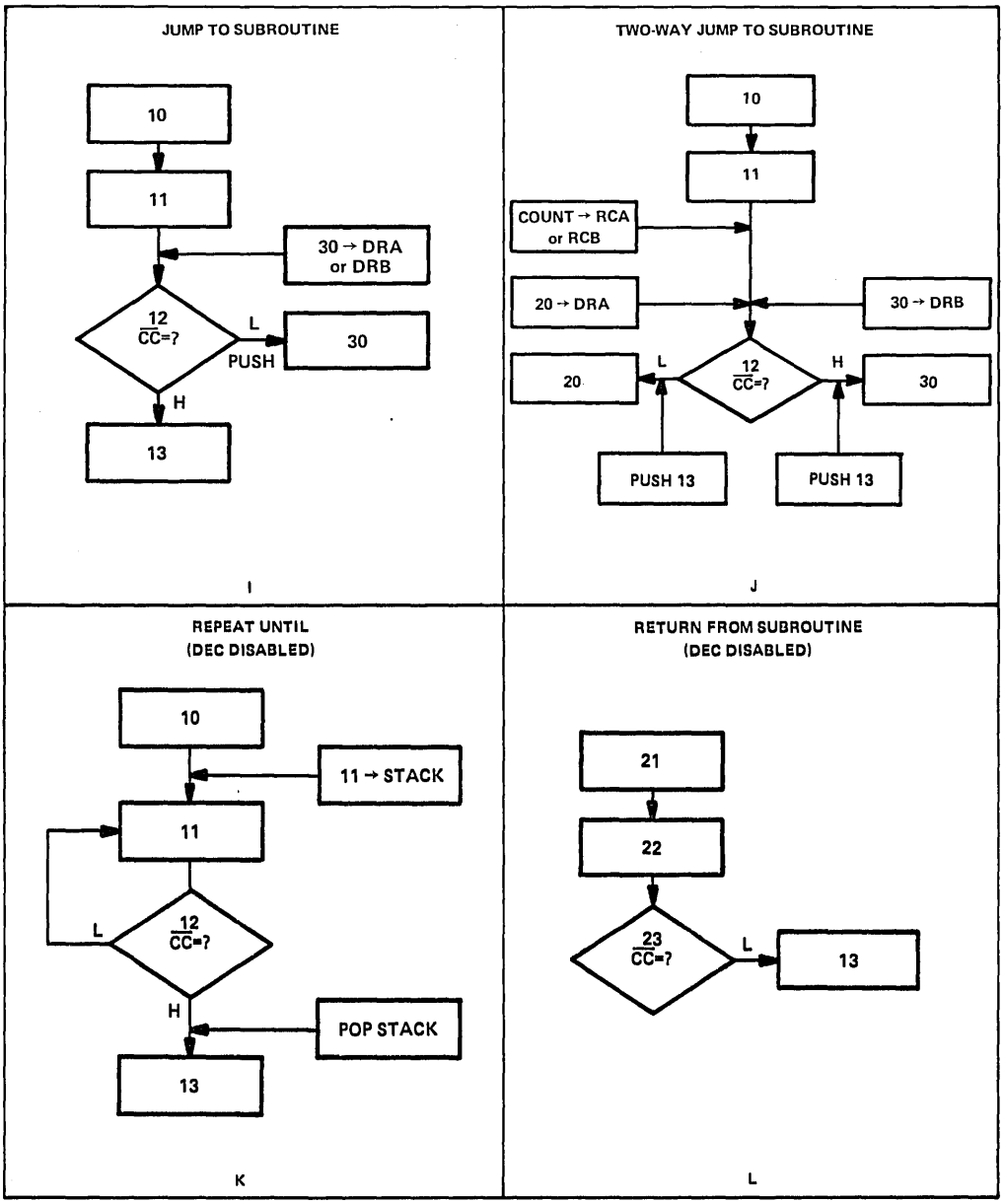
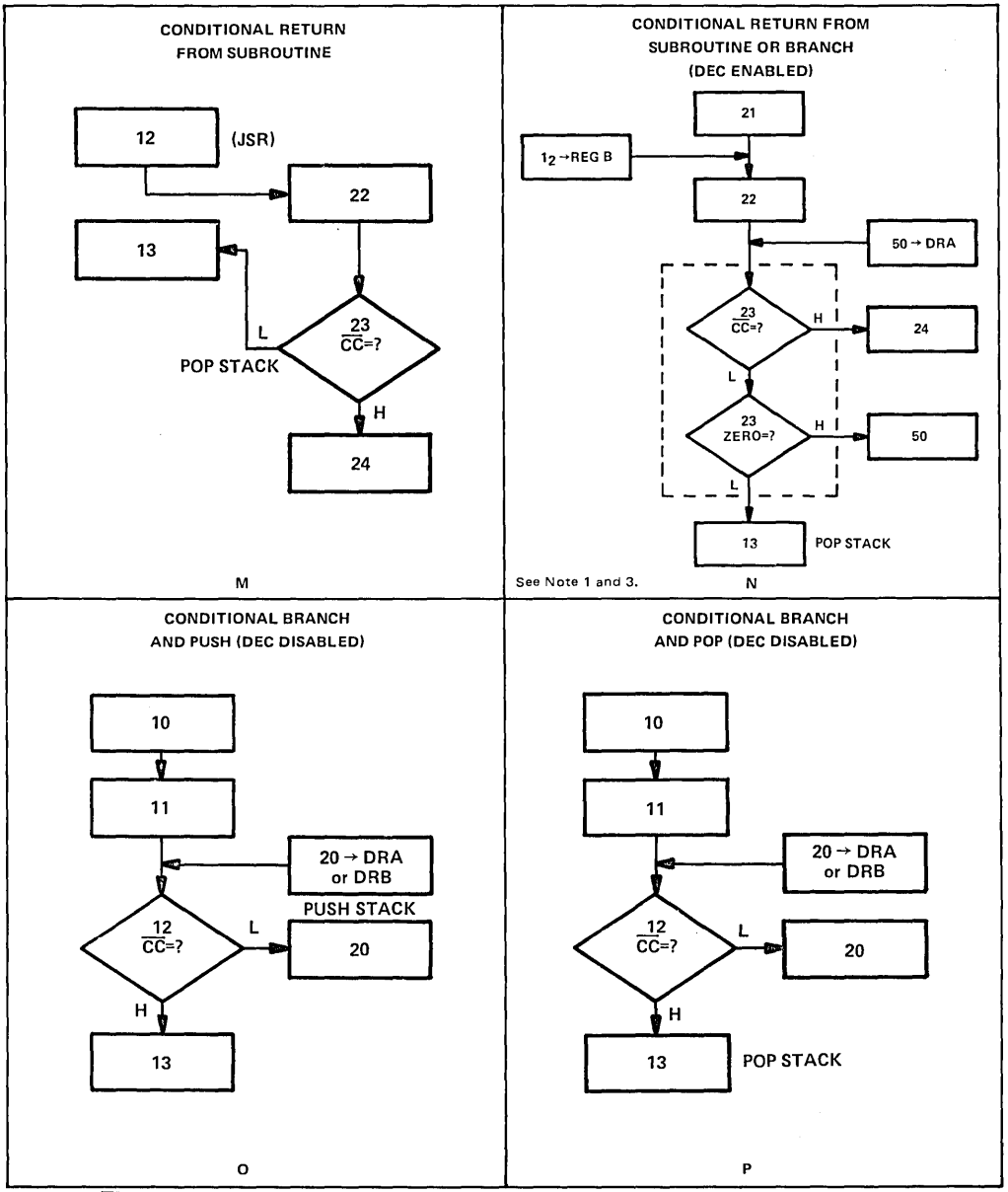


NOTES: 1. $\overline{CC}$ and ZERO are completed in the same clock cycle.
2. The least significant four bits of these addresses will be stripped off and four new bits appended to them from the B3-B0 port on 'AS891 only.

FIGURE 1 – 'AS890 AND 'AS891 INSTRUCTION SET FLOWCHARTS



NOTES: 1. $\overline{CC}$ and ZERO are completed in the same clock cycle.
2. The least significant four bits of these addreses will be stripped off and four new bits appended to them from the B3-B0 port on 'AS891 only.
3. "1_2" denotes that the value 1 is loadcd into the register B. It does not signify a microaddress value.

FIGURE 1 – 'AS890 AND 'AS891 INSTRUCTION SET FLOWCHARTS

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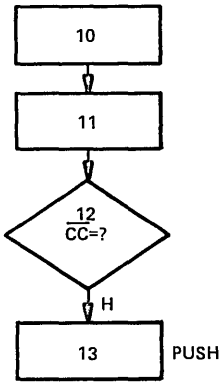
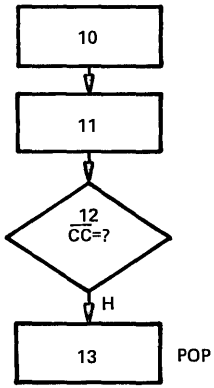
PUSH AND CONTINUE



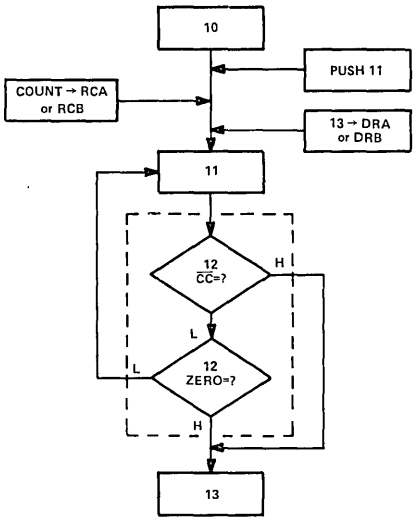
Q

POP AND CONTINUE



R

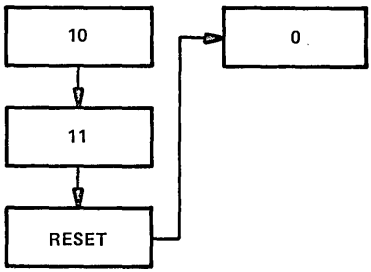
EXIT FROM LOOP



See Note 1.

S

RESET AND CLEAR

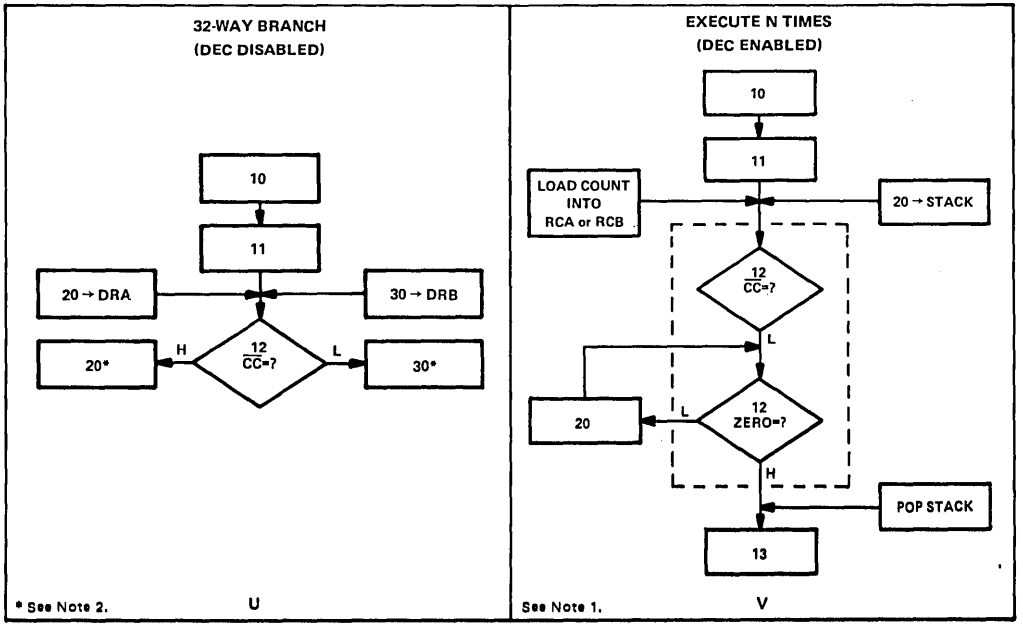


T

NOTES: 1. $\overline{CC}$ and ZERO are completed in the same clock cycle.
2. The least significant four bits of these addresses will be stripped off and four new bits appended to them from the B3-B0 port on 'AS891 only.

FIGURE 1 – 'AS890 AND 'AS891 INSTRUCTION SET FLOWCHARTS

1182



NOTES: 1. $\overline{CC}$ and ZERO are completed in the same clock cycle.
2. The least significant four bits of these addresses will be stripped off and four new bits appended to them from the B3-B0 port on 'AS891 only.

FIGURE 1 – 'AS890 AND 'AS891 INSTRUCTION SET FLOWCHARTS (Concluded)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} . . . . . 7 V
Supply voltage, V_{CC2} . . . . . 3 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54AS890, SN54AS891 . . . . . −55 °C to 125 °C
SN74AS890, SN74AS891 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

Additional information on these products can be obtained from the factory as it becomes available.

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recommended operating conditions

			SN54AS890 SN54AS891			SN74AS890 SN74AS891			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC1}	I/O supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{CC2}	STL internal logic supply voltage		1.8	2	2.2	1.8	2	2.2	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1			−1	mA
								−2.6†	
I_{OL}	Low-level output current	All outputs except Y13-Y0			8			8	mA
		Y13-Y0			12			12	
T_A	Operating free-air temperature		−55		125	0		70	°C

† The extended conditions apply only if V_{CC1} is maintained between 4.75 and 5.25V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS890 SN54AS891			SN74AS890 SN74AS891			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC1} = 4.5 V,	I_I = −18mA			−1.2			−1.2	V
V_{OH}		V_{CC1} = 4.5 V,	I_{OH} = −1 mA	2.4	3.4		2.4	3.4		V
		V_{CC1} = 4.75 V,	I_{OH} = −2.6 mA				2.4			
V_{OL}	All outputs except Y13-Y0	V_{CC1} = 4.5 V,	I_{OL} = 8 mA			0.55			0.55	V
	Y13-Y0	V_{CC1} = 4.5 V,	I_{OL} = 12 mA			0.55			0.55	
I_I	Inputs	V_{CC1} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	I/O ports	V_{CC1} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Inputs	V_{CC1} = 5.5 V,	V_I = 2.7 V			20			20	μA
	I/O ports ▲					40			40	
I_{IL}	$\overline{EA}$ and $\overline{OEB}$	V_{CC1} = 5.5 V,	V_I = 0.4 V			0.4			0.4	mA
	Other inputs					0.2			0.2	
	I/O ports ▲					0.4			0.4	
I_O§		V_{CC1} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC1}		V_{CC1} = 5.5 V	Outputs low		100			100		mA
			Outputs disabled							
I_{CC2}		V_{CC2} = 2.2 V	Outputs high		130			130		mA
			Outputs low							
			Outputs disabled							

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

▲ For I/O ports, the parameters I_{IH} and I_{IL} include output currents I_{OZH} and I_{OZL}, respectively.

Additional information on these products can be obtained from the factory as it becomes available.

typical switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)				UNIT
		Y	ZERO	DRA	DRB	
t_{pd}	$\overline{CC}$	12				ns
	CK	18		18	16	
		24†	26†			
	DRA13-DRA0	8				
	DRB13-DRB0	8				
	MUX2-MUX0	12				
	RC2-RC0	12	14			
	S2-S0	12				
	$\overline{YOE}$	8				

† Decrementing Register/Counter A or B and sensing a zero.

4

setup and hold times

PARAMETER	FROM (INPUT)	TO (DESTINATION)	TYP	MAX	UNIT
t_{su}	$\overline{CC}$	Stack (PUSH)	10		ns
		Stack (POP,READ)	26		
	DRA13-DRA0	RCA, RCB, INT RT	8		
	DRB13-DRB0	RCA, RCB, INT RT	8		
	INC	MPC	12		
	$\overline{INT}$	Stack (PUSH)	10		
	MUX2-MUX0	Stack (PUSH)	10		
		Stack (POP,READ)	26		
	RC2-RC0	Stack (PUSH)	10		
		Stack (POP,READ)	26		
		RCA, RCB	12		
	S2-S0	Stack (PUSH)	10		
		Stack (POP,READ)	26		
t_h	Any Input	Any Destination	0		

minimum clock requirements

PARAMETER		MIN	TYP	MAX	UNIT
$t_{wL(CK)}$	Pulse width, clock low	5			ns
$t_{wH(CK)}$	Pulse width, clock high	10			
$t_{c(CK)}$	Clock cycle time	40			

Additional information on these products can be obtained from the factory as it becomes available.

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Functional Index/Selection Guide

GATES AND INVERTERS

POSITIVE-NAND GATES AND INVERTERS

DESCRIPTION	TYPE	TECHNOLOGY							BOOK†	PAGE NO.
		STD TTL	ALS	AS	H	L	LS	S		
Hex 2-Input Gates	'804		▲	A					ADV	2-374
Hex Inverters	'04	●			●	●	●	●	TTL	5-7
			●						ADV	2-11
	'1004		▲						ADV	2-458
				▲					CF	
Quadruple 2-Input Gates	'00	●			●	●	●	●	TTL	5-6
			A						ADV	2-3
				▲					CF	
	'1000		●						ADV	2-452
				▲					CF	
Triple 3-Input Gates	'10	●			●	●	●	●	TTL	5-8
			●						ADV	2-19
				▲					CF	
	'1010		●						ADV	2-465
Dual 4-Input Gates	'20	●			●	●	●	●	TTL	5-10
			A						ADV	2-27
				▲					CF	
	'1020		●						ADV	2-469
8-Input Gates	'30	●			●	●	●	●	TTL	5-12
			●						ADV	2-37
				▲					CF	
13-Input Gates	'133							●	TTL	5-38
			●						ADV	2-71

POSITIVE-NAND GATES AND INVERTERS WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY							BOOK†	PAGE NO.
		STD TTL	ALS	AS	H	L	LS	S		
Hex Inverters	'05	●			●		●	●	TTL	5-7
			●						ADV	2-13
	'1005		▲						ADV	2-460
Quadruple 2-Input Gates	'01	●			●		●		TTL	5-7
			●						ADV	2 5
	'03	●				●	●	●	TTL	5-7
			A						ADV	2-9
	'1003		●						ADV	2-456
Triple 3-Input Gates	'12	●					●		TTL	5-9
			●						ADV	2-23
Dual 4-Input Gates	'22	●			●		●	●	TTL	5-11
			A						ADV	2-31

POSITIVE-AND GATES

DESCRIPTION	TYPE	TECHNOLOGY							BOOK†	PAGE NO.
		STD TTL	ALS	AS	H	LS	S			
Hex 2-Input Gates	'808		▲	A					ADV	2-380
Quadruple 2-Input Gates	'08	●				●	●		TTL	5-8
			●						ADV	2-15
				▲					CF	
	'1008		●	▲					ADV	2-462
Triple 3-Input Gates	'11				●	●	●		TTL	5-9
			●						ADV	2-21
				▲					CF	
	'1011		●						ADV	2-467
Dual 4-Input Gates	'21					●			TTL	5-11
			●						ADV	2-29
				▲					CF	
Triple 4-Input AND/NAND	'800			▲					ADV	2-368

POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY						BOOK†	PAGE NO.
		STD TTL	ALS	AS	H	LS	S		
Quadruple 2-Input Gates	'09	●				●	●	TTL	5-8
			●					ADV	2-17
Triple 3-Input Gates	'15				●	●	●	TTL	5-10
			●					ADV	2-25

POSITIVE-OR GATES

DESCRIPTION	TYPE	TECHNOLOGY					BOOK†	PAGE NO.
		STD TTL	ALS	AS	LS	S		
Hex 2-Input Gates	'832		▲	A			ADV	2-383
Quadruple 2-Input Gates	'32	●			●	●	TTL	5-13
			●				ADV	2-39
				▲			CF	
	'1032		●	▲			ADV	2-471
Triple 4-Input OR/NOR	'802			▲			ADV	2-371

POSITIVE-NOR GATES

DESCRIPTION	TYPE	TECHNOLOGY						BOOK†	PAGE NO.
		STD TTL	ALS	AS	L	LS	S		
Hex 2-Input Gates	'805		▲	A				ADV	2-377
Quadruple 2-Input Gates	'02	●			●	●	●	TTL	5-6
			●					ADV	2-7
				▲				CF	
	'1002		●					ADV	2-454
Triple 3-Input Gates	'27	●				●		TTL	5-12
			●					ADV	2-33
				▲				CF	
Dual 4-Input Gates with Strobe	'25	●						TTL	5-11
Dual 5-Input Gates	'260						●	TTL	5-57

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS

DESCRIPTION	TYPE	TECHNOLOGY					BOOK†	PAGE NO.
		STD TTL	ALS	AS	LS	S		
Hex Inverters	'14	●			●		TTL	5-9
	'19				●		SUP	17
Dual 4-Input Positive-NAND	'13	●			●		TTL	5-9
	'18				●		SUP	17
Quadruple 2-Input Positive-NAND	'24				●		SUP	17
	'132				●	●	TTL	5-37

CURRENT-SENSING GATES

DESCRIPTION	TYPE	TECHNOLOGY			BOOK†	PAGE NO.
		ALS	AS	LS		
Hex	'63			●	TTL	5-20

DELAY ELEMENTS

DESCRIPTION	TYPE	TECHNOLOGY			BOOK†	PAGE NO.
		ALS	AS	LS		
Inverting & Non-Inverting Elements, 2-Input NAND buffers	'31			●	CF	

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ADV = The Advanced Low-Power Schottky/Advanced Schottky Data Book.
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GATES, EXPANDERS, BUFFERS, DRIVERS, AND TRANSCEIVERS

AND-OR-INVERT GATES

DESCRIPTION	TYPE	TECHNOLOGY							BOOK†	PAGE NO.
		STD TTL	ALS	AS	H	L	LS	S		
2-Wide 4-Input	'55				●	●	●		TTL	5-19
4-Wide 4-2-3-2-Input	'64							●	TTL	5-20
4-Wide 2-2-3-2-Input	'54				●				TTL	5-18
4-Wide 2-Input	'54	●							TTL	5-18
4-Wide 2-3-3-2 Input	'54					●	●		TTL	5-18
Dual 2-Wide 2-Input	'51	●			●	●	●	●	TTL	5-16

AND-OR-INVERT GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY				BOOK†	PAGE NO.
		STD TTL	ALS	AS	S		
4-Wide 4-2-3-2-Input	'65				●	TTL	5-20

EXPANDABLE GATES

DESCRIPTION	TYPE	TECHNOLOGY						BOOK†	PAGE NO.
		STD TTL	ALS	AS	H	L	LS		
Dual 4-Input Positive-NOR With Strobe	'23	●						TTL	5-11
4-Wide AND-OR	'52				●			TTL	5-17
4-Wide AND-OR-INVERT	'53	●			●			TTL	5-17
2-Wide AND-OR-INVERT	'55				●	●	●	TTL	5-19
Dual 2-Wide AND-OR-INVERT	'50	●			●			TTL	5-16

EXPANDERS

DESCRIPTION	TYPE	TECHNOLOGY				BOOK†	PAGE NO.
		STD TTL	ALS	AS	H		
Dual 4-Input	'60	●			●	TTL	5-19
Triple 3-Input	'61				●	TTL	5-19
3-2-2-3-Input AND-OR	'62				●	TTL	5-20

BUFFER AND INTERFACE GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY					BOOK†	PAGE NO.
		STD TTL	ALS	AS	LS	S		
Hex	'07	●					TTL	5-8
	'17	●					TTL	5-10
	'1035		▲				ADV	2-477
Hex Inverter	'06	●					TTL	5-7
	'16	●					TTL	5-10
	'1005		▲				ADV	2-460
Quad 2-Input Positive-NAND	'26	●			●		TTL	5-12
	'38	●			●	●	TTL	5-13
			●				ADV	2-45
	'39	●					CF	
	'1003		●				ADV	2-456
Quad 2-Input Positive-NOR	'33	●			●		TTL	5-13
			●				ADV	2-41

GATES, BUFFERS, DRIVERS, AND BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY					BOOK†	PAGE NO.
		STD TTL	ALS	AS	LS	S		
Non-Inverting Octal Buffers/Drivers	'241		●	●			ADV	2-159
					●	●	TTL	5-54
	'244		●	▲			ADV	2-169
	'465				●		SUP	95
			▲				ADV	2-230
	'467				●		SUP	95
			▲				ADV	2-230
	'541				●		SUP	98
			▲				ADV	2-261
	'1241¶		▲				ADV	2-479
	'1244¶		●				ADV	2-486
Inverting Octal Buffers/Drivers	'231			▲			ADV	2-156
	'240				●	●	TTL	5-53
			●	●			ADV	2-159
	'466				●		SUP	95
			●				ADV	2-230
	'468				●		SUP	95
			●				ADV	2-230
	'540				●		SUP	98
			▲				ADV	2-261
	'1240¶		●				ADV	2-479
Inverting and Non-Inverting Octal Buffers/Drivers	'230			▲			ADV	2-155
Octal Transceivers	'245				●		TTL	7-349
			●	▲			ADV	2-174
	'1245		●				ADV	2-489
Non-Inverting Hex Buffers/Drivers	'365	A			A		TTL	5-66
			▲				ADV	2-214
	'367	A			A		TTL	5-66
			▲				ADV	2-214
Inverting Hex Buffers/Drivers	'366	A			A		TTL	5-66
			▲				ADV	2-214
	'368	A			A		TTL	5-66
			▲				ADV	2-214
Quad Buffers/Drivers with Independent Output Controls	'125	●			A		TTL	5-37
	'126	●			A		TTL	5-37
	'425	●					TTL	5-71
	'426	●					TTL	5-72
Non-Inverting Quad Transceivers	'243				●		TTL	5-54
			●	▲			ADV	2-164
	'12431		▲				ADV	2-482
Inverting Quad Transceivers	'242				●		TTL	5-54
			●	▲			ADV	2-164
	1242¶		▲				ADV	2-482
Quad Transceivers with Storage	'226					●	TTL	7-345
12-Input NAND Gate	'134					●	TTL	5-38
Controller and Bus Driver for 8080A System	'428					●	TTL	7-514
	'438					●	TTL	7-514

50-OHM/75-OHM LINE DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY				BOOK†	PAGE NO.
		STD TTL	ALS	AS	S		
Hex 2-Input Positive-NAND	'804		▲	A		ADV	2-374
Hex 2-Input Positive-NOR	'805		▲	A		ADV	2-377
Hex 2-Input Positive-AND	'808		▲	A		ADV	2-380
Hex 2-Input Positive-OR	'832		▲	A		ADV	2-383
Quad 2-Input Positive-NOR	'128	●				TTI	537
Dual 4-Input Positive-NAND	'140				●	TTL	5-39

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¶Denotes very low power.
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BUFFERS, DRIVERS, TRANSCEIVERS, AND CLOCK GENERATORS

BUFFERS, CLOCK/MEMORY DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY						BOOK†	PAGE NO.
		STD TTL	ALS	AS	H	LS	S		
Hex 2-Input Positive-NAND	'804		▲	A				ADV	2-374
Hex 2-Input Positive-NOR	'805		▲	A				ADV	2-377
Hex 2-Input Positive-AND	'808		▲	A				ADV	2-380
Hex 2-Input Positive-OR	'832		▲	A				ADV	2-383
Hex Inverter	'1004		▲					ADV	2-458
				▲				CF	
Hex Buffer	'1034		▲	▲				ADV	2-474
Quad 2-Input Positive-NAND	'37	●				●	●	TTL	5-13
			●					ADV	2-43
	'1000		●					ADV	2-452
				▲				CF	
Quad 2-Input Positive-NOR	'28	●				●		TTL	5-12
			●					ADV	2-35
	'1002		●					ADV	2-454
Quad 2-Input Positive-AND	'1008		●	▲				ADV	2-462
Quad 2-Input Positive-OR	'1032		●	▲				ADV	2-471
Triple 3-Input Positive-NAND	'1010		●					ADV	2-465
Triple 3-Input Positive-AND	'1011		●					ADV	2-467
Triple 4-Input AND-NAND	'800			▲				ADV	2-368
Triple 4-Input OR-NOR	'802			▲				ADV	2-371
Dual 4-Input Positive-NAND	'40	●			●	●	●	TTL	5-14
			●					ADV	2-47
	'1020		●					ADV	2-469
Line Driver/Memory Driver with Series Damping Resistor	'436						●	SUP	77
Line Driver/Memory Driver	'437						●	SUP	77

BI-/TRI-DIRECTIONAL BUS TRANSCEIVERS AND DRIVERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY				BOOK†	PAGE NO.
			ALS	AS	LS	S		
Quad with Bit Direction Controls	3-State	'446			●		SUP	89
	3-State	'449			●		SUP	89
Quad Tridirection	OC	'440			●		SUP	81
	OC	'441			●		SUP	81
	3-State	'442			●		SUP	81
	3-State	'443			●		SUP	81
	3-State	'444			●		SUP	81
	OC	'448			●		SUP	81
4-Bit with Storage	3-State	'226				●	TTL	7-345
Controller and Bus Driver for 8080A Systems		'428				●	TTL	7-514
		'438				●	TTL	7-514

OCTAL BI-/TRI-DIRECTIONAL BUS TRANSCEIVERS

DESCRIPTION		TYPE OF OUTPUT	TYPE	TECHNOLOGY			BOOK†	PAGE NO.
				ALS	AS	LS		
12 mA/24 mA/48 mA Sink, True Outputs	Low Power	3-State	'245	●	▲		ADV	2-174
						●	TTL	7-349
		OC	'621	●			ADV	2-307
						●	SUP	141
		3-State	'623	●			ADV	2-307
						●	SUP	141
					▲		CF	
		OC, 3-State	'639	●			ADV	2-327
						●	SUP	157
		3-State	'652	▲			ADV	2-344
						●	SUP	175
					▲		CF	
		OC, 3-State	'654	▲			ADV	2-344
						●	CF	
	Very Low Power	OC	'1621	▲			ADV	2-500
		3-State	'1623	▲			ADV	2-500
		OC, 3-State	'1639	▲			ADV	2-506
12 mA/24 mA/48 mA Sink, Inverting Outputs	Low Power	3-State	'620	●			ADV	2-307
						●	SUP	141
					▲		CF	
		OC	'622	●			ADV	2-307
						●	SUP	141
		OC, 3-State	'638	●			ADV	2-327
						●	SUP	157
		3-State	'651	▲			ADV	2-344
						●	SUP	175
					▲		CF	
		OC, 3-State	'653	▲			ADV	2-344
						●	CF	
	Very Low Power	3-State	'1620	▲			ADV	2-500
		OC	'1622	▲			ADV	2-500
		OC, 3-State	'1638	▲			ADV	2-506
12 mA/24 mA/48 mA Sink, True Outputs	Low Power	OC	'641	●			ADV	2-331
						●	SUP	161
		3-State	'645	●	▲		ADV	2-331
						●	SUP	161
	Very Low Power	OC	'1641	▲			ADV	2-510
		3-State	'1645	●			ADV	2-510
12 mA/24 mA/48 mA Sink, Inverting Outputs	Low Power	3-State	'640	●			ADV	2-331
						●	SUP	161
					▲		CF	
		OC	'642	●			ADV	2-331
						●	SUP	161
	Very Low Power	3-State	'1640	●			ADV	2-510
		OC	'1642	▲			ADV	2-510
12 mA/24 mA/48 mA Sink, True and Inverting Outputs	Low Power	3-State	'643	●			ADV	2-331
						●	SUP	161
					▲		CF	
		OC	'644	●			ADV	2-331
						●	SUP	161
	Very Low Power	3-State	'1643	▲			ADV	2-510
		OC	'1644	▲			ADV	2-510
Registered with Multiplexed 12 mA/24 mA/48 mA True Outputs		3-State	'646	▲			ADV	2-337
						●	SUP	168
					▲		CF	
		OC	'647	▲			ADV	2-337
						●	SUP	168
Registered with Multiplexed 12 mA/24 mA/48 mA Inverting Outputs		3-State	'648	▲			ADV	2-337
						●	SUP	168
					▲		CF	
		OC	'649	▲			ADV	2-337
						●	SUP	168
Universal Transceiver/ Port Controllers		3-State	'877		▲		ADV	2-421

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FLIP-FLOPS, LATCHES, AND MULTIVIBRATORS

DUAL AND SINGLE FLIP-FLOPS

DESCRIPTION	TYPE	TECHNOLOGY							BOOK†	PAGE NO.
		STD TTL	ALS	AS	H	L	LS	S		
Dual J-K Edge-Triggered	'73						A		TTL	5-22
	'76						A		TTL	5-23
	'78						A		TTL	5-24
	'103				●				TTL	5-31
	'106				●				TTL	5-32
	'107						A		TTL	5-32
	'108				●				TTL	5-32
	'109	●					A		TTL	5-33
			●	▲					ADV	2-54
	'112						A	●	TTL	5-34
			A	▲					ADV	2-57
	'113						A	●	TTL	5-34
			A	▲					ADV	2-60
	'114						A	●	TTL	5-34
			A	▲					ADV	2-63
Single J-K Edge-Triggered	'70	●							TTL	5-21
	'101				●				TTL	5-31
	'102				●				TTL	5-31
Dual Pulse-Triggered	'73	●			●	●			TTL	5-22
	'76	●			●				TTL	5-23
	'78				●	●			TTL	5-24
	'107	●							TTL	5-33
Single Pulse-Triggered	'71				●	●			TTL	5-21
	'72	●			●	●			TTL	5-22
Dual J-K With Data Lockout	'111	●							TTL	5-33
Single J-K With Data Lockout	'110	●							TTL	5-33
Dual D-Type	'74	●			●	●	A	●	TTL	5-33
			●	▲					ADV	2-49

QUAD LATCHES

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY					BOOK†	PAGE NO.
			STD TTL	ALS	AS	L	LS		
Dual 2-Bit Transparent	2-State	'75	●			●	●	TTL	7-35
	2-State	'77	●			●	●	TTL	7-35
	2-State	'375					●	TTL	7-478
S-R	2-State	'279	●				●	TTL	5-59

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

DESCRIPTION	TYPE	TECHNOLOGY					BOOK†	PAGE NO.
		STD TTL	ALS	AS	LS	L		
Single	'122	●			●	●	TTL	5-36
	'422				●		SUP	73
Dual	'123	●			●	●	TTL	5-36
	'423				●		SUP	73

QUAD AND HEX FLIP-FLOPS

DESCRIPTION	NO. FFs	OUT-PUTS	TYPE	TECHNOLOGY					BOOK†	PAGE NO.
				STD TTL	ALS	AS	LS	S		
D Type	6	Q	'174	●			●	●	TTL	7-253
					▲	▲			ADV	2-121
			'378				●		TTL	7-481
	4	Q,Q	'171				●		CF	
			'175	●			●	●	TTL	7-253
					▲	▲			ADV	2-121
			'379				●		TTL	7-481
J-K	4	Q	'276	●					TTL	7-401
			'376	●					TTL	7-479

OCTAL D-TYPE FLIP-FLOPS

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY					BOOK†	PAGE NO.
			STD TTL	ALS	AS	LS	S		
True Data	3-State	'374		▲	●			ADV	2-224
						●	●	TTL	7-471
	3-State	'574		●	▲			ADV	2-294
True Data with Clear	2-State	'273		▲				ADV	2-192
			●			●		TTL	7-338
	3-State	'575		●	▲			ADV	2-294
	3-State	'874		●	▲			ADV	2-415
	3-State	'878		●	▲			ADV	2-427
True w'th Enable	2-State	'377				●		TTL	7-481
Inverting	3-State	'534		▲	▲			ADV	2-247
	3-State	'564		●				ADV	2-278
	3-State	'576		●	▲			ADV	2-300
Inverting with Clear	3-State	'577		●	▲			ADV	2-300
	3-State	'879		●	▲			ADV	2-427
Inverting with Preset	3-State	'876		●	▲			ADV	2-415

OCTAL LATCHES

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY						BOOK†	PAGE NO.
			STD TTL	ALS	AS	L	LS	S		
Transparent	3-State	'373		▲	●				ADV	2-118
							●	●	TTL	7-471
	3-State	'573		●	▲				ADV	2-288
Dual 4-Bit Transparent	2-State	'100	●						TTL	7-113
	2-State	'116	●						TTL	7-115
	3-State	'873		●	▲				ADV	2-409
Inverting Transparent	3-State	'533		▲	▲				ADV	2-241
	3-State	'563		●					ADV	2-473
	3-State	'580		●	▲				ADV	2-288
Dual 4-Bit Inverting Transparent	3-State	'880		●	▲				ADV	2-433
2-Input Multiplexed	3-State	'604					●		SUP	124
	OC	'605					●		SUP	124
	3-State	'606					●		SUP	124
	OC	'607					●		SUP	124
Addressable	2-State	'259	●				●		TTL	7-376
				▲					ADV	2-191
Multi-Mode Buffered	3-State	'412						●	TTL	7-502

MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

DESCRIPTION	TYPE	TECHNOLOGY					BOOK†	PAGE NO.
		STD TTL	ALS	AS	LS	S		
Single	'121	●					TTL	5-35
Dual	'221	●			●		TTL	5-33

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REGISTERS AND PROGRAMMABLE LOGIC ARRAYS

SHIFT REGISTERS

DESCRIPTION	NO. OF BITS	MODES S/R†	MODES S/L†	MODES LOAD	MODES HOLD	TYPE	TECHNOLOGY STD TTL	TECHNOLOGY ALS	TECHNOLOGY AS	TECHNOLOGY L	TECHNOLOGY LS	TECHNOLOGY S	BOOK†	PAGE NO.
Sign-Protected		X		X	X	'322					A		SUP	47
Parallel-In, Parallel-Out, Bidirectional	8	X	X	X	X	'198	●						TTL	7-338
		X	X	X	X	'299					●	●	TTL	7-437
								●					ADV	2-196
		X	X	X	X	'323					●		TTL	7-443
								●					ADV	2-205
	4	X	X	X	X	'194	●				A	●	TTL	7-316
Parallel-In, Parallel-Out, Registered Outputs	4	X	X	X	X	'671					●		SUP	187
		X	X	X	X	'672					●		SUP	187
Parallel-In, Parallel-Out	8	X		X	X	'199	●						TTL	7-338
	5	X		X		'96	●			●	●		TTL	7-95
	4	X		X		'95	A			●	B		TTL	7-89
		X		X		'99				●			TTL	7-109
		X		X	X	'178	●						TTL	7-265
		X		X	X	'179	●						TTL	7-265
		X		X		'195	●				A	●	TTL	7-324
		X		X		'295					B		TTL	7-429
		X		X		'395					A		TTL	7-496
Serial-In, Parallel-Out	16	X		X	X	'673					●		SUP	193
	8	X				'164	●			●	●		TTL	7-206
								▲					ADV	2-104
Parallel-In, Serial-Out	16	X		X	X	'674					●		SUP	193
	8	X		X	X	'165	●				A		TTL	7-212
								▲					ADV	2-107
		X		X	X	'165	●				A		TTL	7-217
								▲					ADV	2-109
Serial-In, Serial-Out	8	X				'91	A			●	●		TTL	7-81
	4	X		X		'94	●						TTL	7-86

SHIFT REGISTERS WITH LATCHES

DESCRIPTION	NO. OF BITS	OUTPUTS	TYPE	TECHNOLOGY ALS	TECHNOLOGY AS	TECHNOLOGY LS	BOOK†	PAGE NO.
Parallel-In, Parallel-Out with Output Latches	4	3-State	'671			●	SUP	187
		3-State	'672			●	SUP	187
	16	2-State	'673			●	SUP	193
Serial-In, Parallel-Out with Output Latches	8	Buffered	'594			▲	CF	
		3-State	'595			▲	SUP	110
		OC	'596			▲	SUP	110
		OC	'599			▲	CF	
Parallel-In, Serial-Out, with Input Latches	8	2-State	'597			▲	SUP	114
Parallel I/O Ports with Input Latches, Multiplexed Serial Inputs	8	3-State	'598			▲	SUP	114

SIGN-PROTECTED REGISTERS

DESCRIPTION	NO. OF BITS	MODES S/R†	MODES S/L†	MODES LOAD	MODES HOLD	TYPE	TECHNOLOGY ALS	TECHNOLOGY AS	TECHNOLOGY LS	BOOK†	PAGE NO.
Sign-Protected Register	8	X		X	X	'322			A	SUP	47

REGISTER FILES

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY STD TTL	TECHNOLOGY ALS	TECHNOLOGY AS	TECHNOLOGY LS	BOOK†	PAGE NO.
8 Words X 2 Bits	3-State	'172	●				TTL	7-245
4 Words X 4 Bits	OC	'170	●			●	TTL	7-237
	3-State	'670				●	TTL	7-526
Dual 16 Words X 4 Bits	3-State	'870			▲		ADV	2-404
	3-State	'871			▲		ADV	2-404

OTHER REGISTERS

DESCRIPTION	TYPE	TECHNOLOGY STD TTL	TECHNOLOGY ALS	TECHNOLOGY AS	TECHNOLOGY L	TECHNOLOGY LS	TECHNOLOGY S	BOOK†	PAGE NO.
Quadruple Multiplexers With Storage	'98				●			TTL	7-107
	'298	●				●		TTL	7-432
	'3098					●		TTL	7-499
	'399					●		TTL	7-499
8-Bit Universal Shift Registers	'299					●	●	TTL	7-437
			●					ADV	2-196
Quadruple Bus-Buffer Registers	'173	●				A		TTL	7-249
Octal Storage Register	'396					●		SUP	71

PROGRAMMABLE LOGIC ARRAYS

DESCRIPTION	INPUTS	OUTPUTS NO.	OUTPUTS TYPE	TYPE NO.	NO. OF PINS	BOOK†	PAGE NO.
Fixed-OR Arrays	16	8	Active-Low	'PL16L8	20	ADV	
		8	Registered	'PL16R8			
		6		'PL16R6			
		4		'PL16R4			
	19 Registered ▲	8	Active-Low	'PLR19L8	24	ADV	
		8	Registered	'PLR19R8			
		6		'PLR19R6			
		4		'PLR19R4			
	19 Latched ▲	8	Active-Low	'PLT19L8	24	ADV	
		8	Registered	'PLT19R8			
		6		'PLT19R6			
		4		'PLT19R4			
	20 ▲	8	Active-Low	'PL20L8	24	ADV	
		8	Registered	'PL20R8			
		6		'PL20R6			
		4		'PL20R4			
Field-Programmable 14 × 32 × 6 Logic Arrays	14	6	3-State	'PL839	24	ADV	
			OC	'PL840			
Field-Programmable Logic Sequencers	11 or 12	6	3-State	'PL333		ADV	
			OC	'PL335			

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COUNTERS

SYNCHRONOUS COUNTERS – POSITIVE-EDGE TRIGGERED

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY						BOOK†	PAGE NO.
			STD TTL	ALS	AS	L	LS	S		
Decade	Sync	'160	●				A		TTL	7-190
				●	▲				ADV	2-94
	Sync	'162	●				A	●	TTL	7-190
				●	▲				ADV	2-94
	Sync	'560		●					ADV	2-264
	Sync	'668					●		SUP	179
	Sync	'690					●		SUP	211
	Sync	'692					●		SUP	211
Decade Up/Down	Sync	'168					B	●	TTL	7-226
				●	▲				ADV	2-112
	Async	'190	●				●		TTL	7-296
				●					ADV	2-138
	Async	'192	●			●	●		TTL	7-306
				●					ADV	2-145
	Sync	'568		●					ADV	2-279
	Sync	'696					●		SUP	217
	Sync	'698					●		SUP	217
Decade Rate Multiplier, $\frac{1}{N10}$	Async Set-to-9	'167	●						TTL	7-222
4-Bit Binary	Sync	'161	●				A		TTL	7-190
				●	▲				ADV	2-94
	Sync	'163	●				A	●	TTL	7-190
				●	▲				ADV	2-94
	Sync	'561		●					ADV	2-264
	Sync	'669					●		SUP	179
	Sync	'691					●		SUP	211
	Sync	'693					●		SUP	211
4-Bit Binary Up/Down	Sync	'169					B	●	TTL	7-226
				●	▲				ADV	2-112
	Async	'191	●				●		TTL	7-296
				●					ADV	2-138
	Async	193	●			●	●		TTL	7-306
				●					ADV	2-145
	Sync	'569		●					ADV	2-279
	Sync	'697					●		SUP	217
	Sync	'699					●		SUP	217
6-Bit Binary Rate Multiplier, $\frac{1}{N2}$		'97	●						TTL	7-102
8-Bit Up/Down	Async CLR	'867			●				ADV	2-399
	Sync CLR	'869			●				ADV	2-399

ASYNCHRONOUS COUNTERS (RIPPLE CLOCK) – NEGATIVE-EDGE TRIGGERED

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY						BOOK†	PAGE NO.
			STD TTL	ALS	AS	L	LS	S		
Decade	Set-To-9	'90	A			●	●		TTL	7-72
		'68					●		CF	
	Yes	'176	●						TTL	7-259
	Yes	'196	●				●	●	TTL	7-331
	Set-To-9	'290	●				●		TTL	7-423
4-Bit Binary	None	'93	A			●	●		TTL	7-72
		'69					●		CF	
	Yes	'177	●						TTL	7-259
	Yes	'197	●				●	●	TTL	7-331
	None	'293	●				●		TTL	7-423
Divide-By-12	None	'92	A				●		TTL	7-72
Dual Decade	None	'390	●				●		TTL	7-489
	Set-To-9	'490	●				●		TTL	7-520
Dual 4-Bit Binary	None	'393	●				●		TTL	7-489

8-BIT BINARY COUNTERS WITH REGISTERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY			BOOK†	PAGE NO.
			ALS	AS	LS		
Parallel Register	3-State	'590			●	SUP	101
Outputs	OC	'591			●	SUP	101
Parallel Register Inputs	2-State	'592			●	SUP	105
Parallel I/O	3-State	'593			●	SUP	105

FREQUENCY DIVIDERS, RATE MULTIPLIERS

DESCRIPTION	TYPE	TECHNOLOGY				BOOK†	PAGE NO.
		STD TTL	ALS	AS	LS		
50-to-1 Frequency Divider	'56				●	CF	
60-to-1 Frequency Divider	'57				●	CF	
6-Bit Binary Rate Multiplier,	'97	●				TTL	7-102
Decade Rate Multiplier,	'167	●				TTL	7-222

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DECODERS, ENCODERS, AND DATA SELECTORS/MULTIPLEXERS

DATA SELECTORS/MULTIPLEXERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY						BOOK†	PAGE NO.
			STD TTL	ALS	AS	L	LS	S		
16-to-1	2-State	'150	●						TTL	7-157
					▲				CF	
		'850			▲				CF	
Dual 8-to-1	3-State	'351	●						TTL	7-451
8-to-1	2-State	'151	A				●	●	TTL	7-157
				▲	▲				ADV	2-82
		'152	A				●		TTL	7-157
	3-State	'251	●				●	●	TTL	7-362
				▲	▲				ADV	2-177
	3-State	'354					●		SUP	53
	2-State	'355					●		SUP	53
	3-State	'356					●		SUP	53
	2-State	'357					●		SUP	53
Dual 4-to-1	2-State	'153	●			●	●	●	TTL	7-165
				▲	▲				ADV	2-86
	3-State	'253					●	●	TTL	7-369
				▲	▲				ADV	2-183
	2-State	'352					●		TTL	7-454
				▲	▲				ADV	2-206
	3-State	'353					●		TTL	7-457
				▲	▲				ADV	2-210
Octal 2-To-1 with Storage	3-State	'604					●		SUP	124
	OC	'605					●		SUP	124
	3-State	'606					●		SUP	124
	OC	'607					●		SUP	124
Quad 2-To-1 with Storage	2-State	'98				●			TTL	7-107
	2-State	'298	●				●		TTL	7-432
	2-State	'398					●		TTL	7-499
	2-State	'399					●		TTL	7-499
Quad 2-to-1	2-State	'157	●			●	●	●	TTL	7-181
				▲	▲				ADV	2-90
	2-State	'158					●	●	TTL	7-181
				▲	▲				ADV	2-90
	3-State	'257					A	●	TTL	7-372
				▲	▲				ADV	2-187
	3-State	'258					A	●	TTL	7-372
				▲	▲				ADV	2-187
6-to-1 Universal Multiplexer	3-State	'857		●	▲				ADV	2-386

DECODERS/DEMULTIPLEXERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY						BOOK†	PAGE NO.
			STD TTL	ALS	AS	L	LS	S		
4-To-16	2-State	'154	●			●			TTL	7-171
	OC	'159	●						TTL	7-188
4-To-10 BCD-to-Decimal	2-State	'42	A			●	●		TTL	7-15
4-To-10 Excess-3-To-Decimal	2-State	'43	A			●			TTL	7-15
4-To-10 Excess-3-Gray-To-Decimal	2-State	'44	A			●			TTL	7-15
3-To-8 with Address Latches		'131		●					ADV	2-68
	2-State	'137		●					ADV	2-73
							●		SUP	19
3-To-8	2-State	'138		●					ADV	2-76
							●	●	TTL	7-134
	3-State	'538		▲					ADV	2-253
Dual 2-To-4	2-State	'139		▲					ADV	2-79
							●	●	TTL	7-134
	2-State	'155	●				●		TTL	7-175
	OC	'156	●				●		TTL	7-175
Dual 1-To-4 Decoders	3-State	'539		▲					ADV	2-257

CODE CONVERTERS

DESCRIPTION	TYPE	TECHNOLOGY		BOOK†	PAGE NO.
		STD TTL	S		
6-Line-BCD To 6-Line Binary, Or 4-Line To 4-Line BCD 9's/BCD 10's Converters	'184	●		TTL	7-290
6-Bit-Binary To 6-Bit-BCD Converters	'185	A		TTL	7-290
BCD-To-Binary Converters	'484		●	BMC	2-71
Binary-To-BCD Converters	'485		●	BMC	2-71

PRIORITY ENCODERS/REGISTERS

DESCRIPTION	TYPE	TECHNOLOGY				BOOK†	PAGE NO.
		STD TTL	ALS	AS	LS		
Full BCD	'147	●			●	TTL	7-151
Cascadable Octal	'148	●			●	TTL	7-151
Cascadable Octal With 3-State Outputs	'348				●	TTL	7-448
4-Bit Cascadable With Registers	'278	●				TTL	7-403

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DISPLAY DECODERS/DRIVERS, MEMORY/MICROPROCESSOR CONTROLLERS, AND VOLTAGE-CONTROLLED OSCILLATORS

OPEN-COLLECTOR DISPLAY DECODERS/DRIVERS

DESCRIPTION	PFF-STATE OUTPUT VOLTAGE	TYPE	TECHNOLOGY					BOOK†	PAGE NO.
			STD TTL	ALS	AS	L	LS		
BCD-To-Decimal	30 V	'45	●					TTL	7-20
	60 V	'141	●					TTL	7-138
	15 V	'145	●				●	TTL	7-148
	7 V	'445					●	SUP	87
BCD-To-Seven-Segment	30 V	'46	A			●		TTL	7-22
	15 V	'47	A			●	●	TTL	7-22
	5.5 V	'48	●				●	TTL	7-22
	5.5 V	'49	●				●	TTL	7-22
	30 V	'246	●					TTL	7-351
	15 V	'247	●				●	TTL	7-351
	7 V	'347					●	SUP	51
	7 V	'447					●	SUP	93
	5.5 V	'248	●				●	TTL	7-351
	5.5 V	'249	●				●	TTL	7-351

OPEN COLLECTOR DISPOAY DECODERS/DRIVERS WITH COUNTERS/LATCHES

DESCRIPTION	TYPE	TECHNOLOGY			BOOK†	PAGE NO.
		STD TTL	ALS	AS		
BCD Counter/4-Bit Latch/BCD-To-Decimal Decoder/Driver	'142	●			TTL	7-143
BCD Counter/4-Bit Latch/BCD-To-Seven-Segment Decoder/Led Driver	'143	●			TTL	7-143
BCD Counter/4-Bit Latch/BCD-To-Seven-Segment Decoder/Lamp Driver	'144	●			TTL	7-143

VOLTAGE-CONTROLLED OSCILLATORS

DESCRIPTION						TYPE	TECHNOLOGY		BOOK†	PAGE NO.
No. VCO'S	COMP'L Z_{OUT}	ENABLE	RANGE INPUT	R_{ext}	f_{max} MHz		LS	S		
Single	Yes	Yes	Yes	No	20	'624	●		SUP	145
Single	Yes	Yes	Yes	Yes	20	'628	●		SUP	145
Dual	No	Yes	Yes	No	60	'124		●	TTL	7-123
Dual	Yes	No	No	No	20	'625	●		SUP	145
Dual	Yes	Yes	No	No	20	'626	●		SUP	145
Dual	No	No	No	No	20	'627	●		SUP	145
Dual	No	Yes	Yes	No	20	'629	●		SUP	145

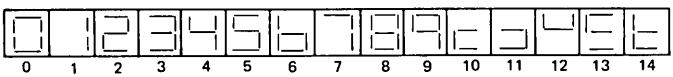
MEMORY/MICROPROCESSOR CONTROLLERS

DESCRIPTION			TYPE	TECHNOLOGY				BOOK†	PAGE NO.
				ALS	AS	LS	S		
System Controllers For 8080A			'428				●	TTL	7-514
			'438				●	TTL	7-514
System Controller, Universal			'482				●	BMC	3-57
System Controllers, Universal			'890		▲			ADV	4-51
(or For '888, '889)			'891		▲			ADV	4-51
Memory Refresh Controllers	Transparent, Burst Modes	4K, 16K	'600			A		SUP	119
		64K	'601			A		SUP	119
	Cycle Steal, Burst Modes	4K, 16K	'602			A		SUP	119
		64K	'603			A		SUP	119
Memory Cycle Controller			'608			●		SUP	128
Memory Mappers		3-State‡	'612			●		SUP	133
		OC‡	'613			●		SUP	133
Memory Mappers With Output Latches		3-State‡	'610			●		SUP	133
		OC‡	'611			●		SUP	133
Multi-Mode Latches (8080A Applications)			'412				●	TTL	7-502
Clock Elements (8080A Applications)			'424			●		CF	

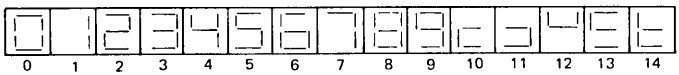
CLOCK GENERATOR CIRCUITS

DESCRIPTION	TYPE	TECHNOLOGY					BOOK†	PAGE NO.
		STD TTL	ALS	AS	LS	S		
Quadruple Complementary-Output Logic Elements	'265	●					TTL	5-57
Dual Pulse Synchronizers/Drivers	'120	●					TTL	7-118
Crystal-Controlled Oscillators	'320				●		SUP	44
	'321				●		SUP	44
Digital Phase-Lock Loop	'297				●		SUP	38
Programmable Frequency Dividers/Digital Timers	'292				●		SUP	31
	'294				●		SUP	31
Triple 4-Input AND/NAND Drivers	'800			▲			ADV	2-368
Triple 4-Input OR/NOR Drivers	'802			▲			ADV	2-371
Dual VCO	'124					●	TTL	2-123
Clock Element for 8080A Systems	'424				●		CF	

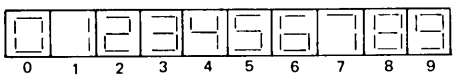
RESULTANT DISPLAYS USING '46A, '47A, '48, '49, 'L46, 'L47, 'LS47, 'LS48, 'LS49, 'LS347



RESULTANT DISPLAYS USING '246, '247, '248, '249, 'LS247, 'LS248, 'LS249, 'LS447



RESULTANT DISPLAYS USING '143, '144



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ARITHMETIC CIRCUITS, ERROR DETECTION CIRCUITS, AND PROCESSOR ELEMENTS

PARALLEL BINARY ADDERS

DESCRIPTION	TYPE	TECHNOLOGY						BOOK†	PAGE NO.
		STD TTL	ALS	AS	H	LS	S		
1-Bit Gated	'80	●						TTL	7-41
2-Bit	'82	●						TTL	7-49
4-Bit	'83	A				A		TTL	7-53
	'283	●				●	●	TTL	7-415
Dual 1-Bit Carry-Save	'183				●	●		TTL	7-287

ACCUMULATORS, ARITHMETIC LOGIC UNITS, LOOK-AHEAD CARRY GENERATORS

DESCRIPTION		TYPE	TECHNOLOGY					BOOK†	PAGE NO.
			STD TTL	ALS	AS	LS	S		
4-Bit Parallel Binary Accumulators		'281					●	TTL	7-410
		'681				●		SUP	197
4-Bit Arithmetic Logic Units/ Function Generators		'181	●			●	●	TTL	7-271
					A			ADV	2-127
		'381				A		CF	
							●	TTL	7-484
		'881			A			ADV	2-439
4-Bit Arithmetic Logic Unit with Ripple Carry		'382				●		SUP	60
Look-Ahead Carry Generators	16-Bit	'182	●				●	TTL	7-282
	32-Bit	'882			●			ADV	2-440
Quad Serial Adder/Subtractor		'385				●		SUP	69
4-Bit-Slice Elements		'481				●	●	BMC	3-3
8-Bit-Slice Elements		'888			▲			ADV	4-3
		'889			▲			ADV	4-3

MULTIPLIERS

DESCRIPTION	TYPE	TECHNOLOGY					BOOK†	PAGE NO.
		STD TTL	ALS	AS	LS	S		
2-Bit-By-4-Bit Parallel Binary Multipliers	'261				●		TTL	7-380
4-Bit-By-4-Bit Parallel Binary Multipliers	'274					●	TTL	7-391
	'284	●					TTL	7-420
	'285	●					TTL	7-420
7-Bit-Slice Wallace Trees	'275				●	●	TTL	7-391
25-MHz 6-Bit-Binary Rate Multipliers	'97	●					TTL	7-102
25-MHz Decade Rate Multipliers	'167	●					TTL	7-222
8-Bit X 1-Bit 2's Complement Multipliers	'384				●		SUP	65
16-Bit Parallel Multiplier	'1616		▲				ADV	2-492

OTHER ARITHMETIC OPERATORS

DESCRIPTION	TYPE	TECHNOLOGY							BOOK†	PAGE NO.
		STD TTL	ALS	AS	H	L	LS	S		
Quad 2-Input Exclusive-OR Gates With Totem-Pole Outputs	'86	●				●	●	●	TTL	7-65
			▲						ADV	2-52
	'386						●		TTL	7-487
Quad 2-Input Exclusive-OR Gates With Open-Collector Outputs	'136	●					●		TTL	7-131
Quad 2-Input Exclusive-NOR Gates	'266						●		TTL	7-386
Quad Exclusive OR/NOR Gates	'135							●	TTL	7-129
4-Bit True/Complement, Element	'87				●				TTL	7-70

4-BIT COMPARATORS

DESCRIPTION					TYPE	TECHNOLOGY				BOOK†	PAGE NO.
P=Q	P>Q	P<Q	OUTPUT	OUTPUT ENABLE		STD TTL	ALS	AS	L LS S		
Yes	Yes	No	2-State	Yes	'85	●			● ● ●	TTL	7-57

8-BIT COMPARATORS

DESCRIPTION							TYPE	TECHNOLOGY			BOOK†	PAGE NO.
INPUTS	P=Q	P=Q	P>Q	P<Q	OUTPUT	OUTPUT ENABLE		ALS	AS	LS		
20-kΩ Pull-Up	Yes	No	No	No	OC	Yes	'518	●			ADV	2-235
	No	Yes	No	No	2-State	Yes	'520	●			ADV	2-235
	No	Yes	No	No	OC	Yes	'522	●			ADV	2-235
	Yes	No	Yes	No	2-State	No	'682			●	SUP	203
	Yes	No	Yes	No	OC	No	'683			●	SUP	203
Standard	Yes	No	No	No	OC	Yes	'519	●			ADV	2-235
	No	Yes	No	No	2-State	Yes	'521	●			ADV	2-235
	Yes	No	Yes	No	2-State	No	'684			●	SUP	203
	Yes	No	Yes	No	OC	No	'685			●	SUP	203
	Yes	No	Yes	No	2-State	Yes	'686			●	SUP	203
	Yes	No	Yes	No	OC	Yes	'687			●	SUP	203
	No	Yes	No	No	2-State	Yes	'689	●			ADV	2-364
										●	SUP	203
	No	Yes	No		OC	Yes	'689	●			ADV	2-364
										●	SUP	203
Latched P	No	No	Yes	Yes	2-State	Yes	'885		●		ADV	2-446
Latched P and Q	Yes	No	Yes	Yes	Latched	Yes	'866		●		ADV	2-393

ADDRESS COMPARATORS

DESCRIPTION	OUTPUT ENABLE	LATCHED OUTPUT	TYPE	TECHNOLOGY		BOOK†	PAGE No.
				ALS	AS		
16-Bit to 4-Bit	Yes		'677	▲		ADV	2-352
		Yes	'678	▲		ADV	2-352
12-Bit to 4-Bit	Yes		'679	▲		ADV	2-358
		Yes	'680	▲		ADV	2-358

PARITY GENERATORS/CHECKERS, ERROR DETECTION AND CORRECTION CIRCUITS

DESCRIPTION		NO. OF BITS	TYPE	TECHNOLOGY					BOOK†	PAGE NO.
				STD TTL	ALS	AS	LS	S		
Odd/Even Parity Generators/Checkers		8	'180	●					TTL	7-269
		9	'280				●	●	TTL	7-406
						▲			ADV	2-195
Parallel Error Detection/Correction Circuits	3-State	8	'636				●		CF	
	OC	8	'637				●		CF	
	3-State	16	'630				●		SUP	151
	OC	16	'631				●		SUP	151
	3-State	32	'632		▲				ADV	2-313
	OC	32	'633		▲				ADV	2-313
	3-State	32	'634		▲				ADV	2-313
	OC	32	'635		▲				ADV	2-313

BIPOLAR BIT-SLICE PROCESSOR ELEMENTS

DESCRIPTION	CASCADABLE TO N-BITS	TYPE	TECHNOLOGY				BOOK†	PAGE NO.
			ALS	AS	LS	S		
4-Bit-Slice	Yes	'481			●	●	BMC	3-3
8-Bit-Slice	Yes	'888		▲			ADV	4-3
	Yes	'889		▲			ADV	4-3

† The books are identified as follows:
ADV = The ALS/AS Data Book
BMC = The Bipolar Microcomputer Components Data Book for Design Engineers, third edition
SUP = 1981 Supplement to the TTL Data Book for Design Engineers, second edition
TTL = The TTL Data Book for Design Engineers, second edition
CF = Data sheet is not presently available in a book. Contact the factory.

● Denotes available technology.

▲ Denotes planned new products.

A Denotes "A" suffix version available in the technology indicated.

MEMORIES

USER-PROGRAMMABLE READ-ONLY MEMORIES (PROM'S)

STANDARD PROM'S

DESCRIPTION	TYPE	ORGANIZATION	TYPE OUTPUT	BOOK†	PAGE NO.
16K-Bit Arrays	▲ TBP28S165A	2048W × 8B	3-State	CF	
	▲ TBP28S165A-35	2048W × 8B	3-State	CF	
	TBP28S166	2048W × 8B	3-State	BMC	2-13
	TBP28SA166	2048W × 8B	OC	BMC	2-13
	▲ TBP28S166-55	2048W × 8B	3-State	BMC	2-13
	▲ TBP28S166A	2048W × 8B	3-State	CF	
	▲ TBP28S166A-35	2048W × 8B	3-State	CF	
8K-Bit Arrays	TBP24S81	2048W × 4B	3-State	BMC	2-13
	‡ TBP24S81-55	2048W × 4B	3-State	BMC	2-13
	TBP24SA81	2048W × 4B	OC	BMC	2-13
	‡ TBP24SA81-55	2048W × 4B	OC	BMC	2-13
	TBP28S86A	1024W × 8B	3-State	CF	
	‡ TBP28S86A-50	1024W × 8B	3-State	CF	
	TBP28SA86A	1024W × 8B	OC	CF	
	‡ TBP28SA86A-50	1024W × 8B	OC	CF	
	TBP28S2708A	1024W × 8B	3-State	CF	
	▲ TBP28S85	1024W × 8B	3-State	BMC	2-13
4K-Bit Arrays	TBP28S42	512W × 8B	3-State	BMC	2-13
	TBP28SA42	512W × 8B	OC	BMC	2-13
	▲ TBP28S45	512W × 8B	3-State	BMC	2-13
	▲ TBP28SA45	512W × 8B	OC	CF	
	TBP28S46	512W × 8B	3-State	BMC	2-13
	TBP28SA46	512W × 8B	OC	BMC	2-13
	TBP24S41	1024W × 4B	3-State	BMC	2-13
	TBP24SA41	1024W × 4B	OC	BMC	2-13
1K-Bit Arrays	TBP24S10	256W × 4B	3-State	BMC	2-13
	TBP24SA10	256W × 4B	OC	BMC	2-13
256-Bit Arrays	TBP18S030	32W × 8B	3-State	BMC	2-7
	TBP18SA030	32W × 8B	OC	BMC	2-7

LOW-POWER PROM'S

DESCRIPTION	TYPE	ORGANIZATION	TYPE OUTPUT	BOOK†	PAGE NO.
16K-Bit Arrays	▲ TBP28L166A	2048W × 8B	3-State	CF	
8K-Bit Arrays	▲ TBP28L85A	1024W × 8B	3-State	CF	
	TBP28L86A	1024W × 8B	3-State	CF	
4K-Bit Arrays	TBP28L42	512W × 8B	3-State	BMC	2-13
	TBP28LA42	512W × 8B	OC	CF	
	▲ TBP28L45	512W × 8B	3-State	BMC	2-13
	TBP28L46	512W × 8B	3-State	BMC	2-13
	TBP28LA46	512W × 8B	OC	CF	
2K-Bit Arrays	TBP28L22	256W × 8B	3-State	BMC	2-13
	TBP28LA22	256W × 8B	OC	BMC	2-13

REGISTERED PROM'S

DESCRIPTION	TYPE	ORGANIZATION	TYPE OUTPUT	BOOK†	PAGE NO.
16K-Bit Arrays	▲ TBP28R166A	2048W × 8B	3-State	BMC	2-13
	▲ TBP28R165A	2048W × 8B	3-State	BMC	2-13
8K-Bit Arrays	▲ TBP28R86A	1024W × 8B	3-State	CF	
	▲ TBP28R85A	1024W × 8B	3-State	CF	
4K-Bit Arrays	▲ TBP28R46	512W × 8B	3-State	CF	
	▲ TBP28R45	512W × 8B	3-State	BMC	2-13

READ-ONLY MEMORIES (ROM'S)

DESCRIPTION	ORGANIZATION	TYPE OF OUTPUT	TYPE	TECHNOLOGY				BOOK†	PAGE NO.
				STD TTL	ALS	AS	S		
1024-Bit Arrays	256 × 4	OC	'187	●				TTL	5-49
256-Bit Arrays	32 × 8	OC	'88	A				TTL	5-27

RANDOM-ACCESS READ-WRITE MEMORIES (RAM'S)

DESCRIPTION	ORGANIZATION	TYPE OF OUTPUT	TYPE	TECHNOLOGY					BOOK†	PAGE NO.
				STD TTL	ALS	AS	LS	S		
256-Bit Arrays	256 × 1	3-State	'201					●	BMC	2-53
		OC	'301					●	BMC	2-53
	64 × 4	3-State	'217		●				ADD	2-152
		OC	'317		●				ADV	2-201
	32 × 8	3-State	'218		●				ADV	2-152
		OC	'318		●				ADV	2-201
64-Bit Arrays	16 × 4	OC	'89	●					BMC	2-41
		3-State	'189				A		BMC	2-45
								A	BMC	2-49
		3-State	'219				A		BMC	2-45
		OC	'289				A		BMC	2-45
								A	BMC	2-49
		OC	'319				A		BMC	2-45
16-Bit Arrays	16 × 1	OC	'81	A					BMC	2-35
			'84	A					BMC	2-35
16-Bit Multiple-Port Register File	8 × 2	3-State	'172	●					TTL	7-245
16-Bit Register File	4 × 4	OC	'170	●			●		TTL	7-237
		3-State	'670				●		TTL	7-526
Dual 64-Bit Register Files	16 × 4, 16 × 4	3-State	'870			▲			ADV	2-404
			'871			▲			ADV	2-404

FIRST-IN FIRST-OUT MEMORIES (FIFO'S)

DESCRIPTION		TYPE OF OUTPUT	TYPE	TECHNOLOGY				BOOK†	PAGE NO.
				ALS	AS	LS	S		
Asynchronous 16 × 5		3-State	'225				•	BMC	2-61
Asynchronous 16 × 4	Grated Input, Output Ready	3-State	'222			•		BMC	2-53
		3-State	'224			•		BMC	2-53
	Single Input, Output Ready	OC	'227			•		BMC	2-53
		OC	'228			•		BMC	2-53

†The books are identified as follows:
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- TTL = The TTL Data Book for Design Engineers, second edition
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Product Guide

00

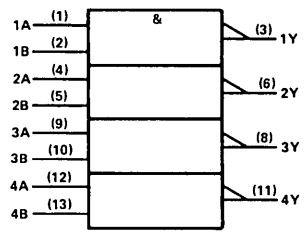
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

typical performance

TYPE	POWER	DELAY
'00	10 mW	10 ns
'ALS00A	1.25 mW	3.5 ns
'H00	22 mW	6 ns
'L00	1 mW	33 ns
'LS00	2 mW	9.5 ns
'S00	19 mW	3 ns

SN5400 (J,FH) SN7400 (J,N)
SN54ALS00A (J) SN74ALS00A (N,FN)
SN54H00 (J,FH) SN74H00 (J,N)
SN54L00 (J)
SN54LS00 (J,FH) SN74LS00 (J, N, FN)
SN54S00 (J,FH) SN74S00 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{AB}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3Y	1	nc	11	nc
2	1B	9	3A	2	1A	12	3Y
3	1Y	10	3B	3	1B	13	3A
4	2A	11	4Y	4	1Y	14	3B
5	2B	12	4A	5	nc	15	nc
6	2Y	13	4B	6	2A	16	4Y
7	GND	14	V_{CC}	7	nc	17	nc
				8	2B	18	4A
				9	2Y	19	4B
				10	GND	20	V_{CC}

01

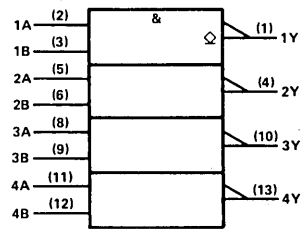
QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

typical performance

TYPE	POWER	DELAY
'01	10 mW	22 ns
'ALS01	1.28 mW	16 ns
'H01	22 mW	8 ns
'LS01	2 mW	16 ns

SN5401 (J,FH) SN7401 (J,N)
SN54ALS01 (J,FH) SN74ALS01 (N,FN)
SN54H01 (J) SN74H01 (J,N)
SN54LS01 (J,FH) SN74LS01 (J,N,FN)

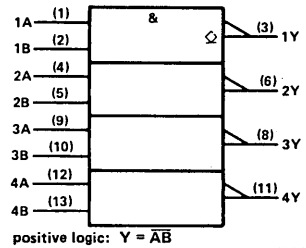
logic symbol, '01, 'ALS01, 'LS01†



pin assignments, '01, 'ALS01, 'LS01

J, N PACKAGES				FH, FN PACKAGES			
1	1Y	8	3A	1	nc	11	nc
2	1A	9	3B	2	1Y	12	3A
3	1B	10	3Y	3	1A	13	3B
4	2Y	11	4A	4	1B	14	3Y
5	2A	12	4B	5	nc	15	nc
6	2B	13	4Y	6	2Y	16	4A
7	GND	14	V_{CC}	7	nc	17	nc
				8	2A	18	4B
				9	2B	19	4Y
				10	GND	20	V_{CC}

logic symbol, 'H01†



positive logic: $Y = \overline{AB}$

pin assignments, 'H01

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3Y	1	nc	11	nc
2	1B	9	3A	2	1A	12	3Y
3	1Y	10	3B	3	1B	13	3A
4	2A	11	4Y	4	1Y	14	3B
5	2B	12	4A	5	nc	15	nc
6	2Y	13	4B	6	2A	16	4Y
7	GND	14	V_{CC}	7	nc	17	nc
				8	2B	18	4A
				9	2Y	19	4B
				10	GND	20	V_{CC}

02

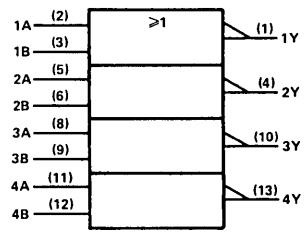
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

typical performance

TYPE	POWER	DELAY
'02	14 mW	10 ns
'ALS02	1.89 mW	5.5 ns
'L02	1.5 mW	33 ns
'LS02	2.75 mW	10 ns
'S02	29 mW	3.5 ns

SN5402 (J,FH) SN7402 (J,N)
SN54ALS02 (J,FH) SN74ALS02 (N,FN)
SN54L02 (J)
SN54LS02 (J,FH) SN74LS02 (J,N,FN)
SN54S02 (J,FH) SN74S02 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{A + B}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1Y	8	3A	1	nc	11	nc
2	1A	9	3B	2	1Y	12	3A
3	1B	10	3Y	3	1A	13	3B
4	2Y	11	4A	4	1B	14	3Y
5	2A	12	4B	5	nc	15	nc
6	2B	13	4Y	6	2Y	16	4A
7	GND	14	V_{CC}	7	nc	17	nc
				8	2A	18	4B
				9	2B	19	4Y
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection

03

QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

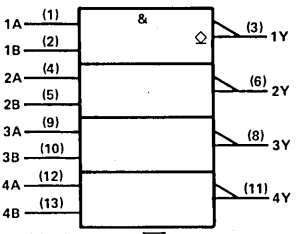
typical performance

TYPE	POWER	DELAY
'03	10 mW	22 ns
'ALS03A	1.28 mW	16 ns
'L03	1 mW	46 ns
'LS03	2 mW	16 ns
'S03	17.5 mW	16 ns

SN5403 (J,FH)
SN54ALS03A (J,FH)
SN54L03 (J)
SN54LS03 (J,FH)
SN54S03 (J,FH)

SN7403 (J,N)
SN74ALS03A (N,FN)
SN74LS03 (J,N,FN)
SN74S03 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{AB}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3Y	1	nc	11	nc
2	1B	9	3A	2	1A	12	3Y
3	1Y	10	3B	3	1B	13	3A
4	2A	11	4Y	4	1Y	14	3B
5	2B	12	4A	5	nc	15	nc
6	2Y	13	4B	6	2A	16	4Y
7	GND	14	V_{CC}	7	nc	17	nc
				8	2B	18	4A
				9	2Y	19	4B
				10	GND	20	V_{CC}

04

HEX INVERTERS

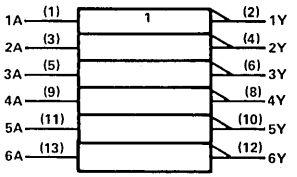
typical performance

TYPE	POWER	DELAY
'04	10 mW	10 ns
'ALS04	1.27 mW	3.5 ns
'H04	22 mW	6 ns
'L04	1 mW	33 ns
'LS04	2 mW	9.5 ns
'S04	19 mW	3 ns

SN5404 (J,FH)
SN54ALS04 (J,FH)
SN54H04 (J)
SN54L04 (J)
SN54LS04 (J,FH)
SN54S04 (J,FH)

SN7404 (J,N)
SN74ALS04 (N,FN)
SN74H04 (J,N)
SN74LS04 (J,N,FN)
SN74S04 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{A}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	4Y	1	nc	11	nc
2	1Y	9	4A	2	1A	12	4Y
3	2A	10	5Y	3	1Y	13	4A
4	2Y	11	5A	4	2A	14	5Y
5	3A	12	6Y	5	nc	15	nc
6	3Y	13	6A	6	2Y	16	5A
7	GND	14	V_{CC}	7	nc	17	nc
				8	3A	18	6Y
				9	3Y	19	6A
				10	GND	20	V_{CC}

05

HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

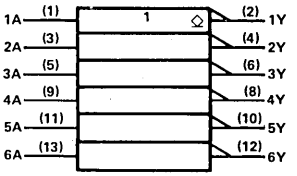
typical performance

TYPE	POWER	DELAY
'05	10 mW	24 ns
'ALS05	1.27 mW	13.5 ns
'H05	22 mW	8 ns
'LS05	2 mW	16 ns
'S05	17.5 mW	5 ns

SN5405 (J,FH)
SN54ALS05 (J,FH)
SN54H05 (J)
SN54LS05 (J,FH)
SN54S05 (J,FH)

SN7405 (J,N)
SN74ALS05 (N,FN)
SN74H05 (J,N)
SN74LS05 (J,N,FN)
SN74S05 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{A}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	4Y	1	nc	11	nc
2	1Y	9	4A	2	1A	12	4Y
3	2A	10	5Y	3	1Y	13	4A
4	2Y	11	5A	4	2A	14	5Y
5	3A	12	6Y	5	nc	15	nc
6	3Y	13	6A	6	2Y	16	5A
7	GND	14	V_{CC}	7	nc	17	nc
				8	3A	18	6Y
				9	3Y	19	6A
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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06

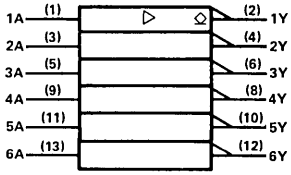
HEX INVERTER BUFFER/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

typical performance

TYPE	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	TYPICAL DELAY TIME	TYPICAL POWER PER GATE
SN54'	30 V	30 mA	12.5 ns	26 mW
SN74'	30 V	40 mA	12.5 ns	26 mW

SN5406 (J,FH) SN7406 (J,N)

logic symbol†



positive logic: $Y = \overline{A}$

pin assignments

J, N PACKAGES			
1	1A	8	4Y
2	1Y	9	4A
3	2A	10	5Y
4	2Y	11	5A
5	3A	12	6Y
6	3Y	13	6A
7	GND	14	V_{CC}

FH PACKAGE			
1	nc	11	nc
2	1A	12	4Y
3	1Y	13	4A
4	2A	14	5Y
5	nc	15	nc
6	2Y	16	5A
7	nc	17	nc
8	3A	18	6Y
9	3Y	19	6A
10	GND	20	V_{CC}

07

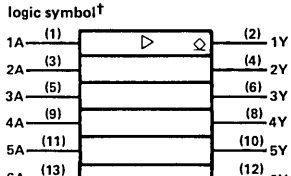
HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

typical performance

TYPE	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	TYPICAL DELAY TIME	TYPICAL POWER PER GATE
SN54'	30 V	30 mA	13 ns	21 mW
SN74'	30 V	40 mA	13 ns	21 mW

SN5407 (J,FH) SN7407 (J,N)

logic symbol†



positive logic: $Y = A$

pin assignments

J, N PACKAGES			
1	1A	8	4Y
2	1Y	9	4A
3	2A	10	5Y
4	2Y	11	5A
5	3A	12	6Y
6	3Y	13	6A
7	GND	14	V_{CC}

FH PACKAGE			
1	nc	11	nc
2	1A	12	4Y
3	1Y	13	4A
4	2A	14	5Y
5	nc	15	nc
6	2Y	16	5A
7	nc	17	nc
8	3A	18	6Y
9	3Y	19	6A
10	GND	20	V_{CC}

08

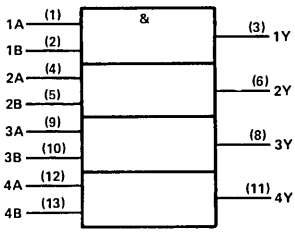
QUADRUPLE 2-INPUT POSITIVE-AND GATES

typical performance

TYPE	POWER	DELAY
'08	19 mW	15 ns
'ALS08	2.19 mW	6.5 ns
'LS08	4.25 mW	12 ns
'S08	32 mW	4.75 ns

SN5408 (J,FH) SN7408 (J,N)
SN54ALS08 (J,FH) SN74ALS08 (N,FN)
SN54LS08 (J,FH) SN74LS08 (J,N,FN)
SN54S08 (J,FH) SN74S08 (J,N,FN)

logic symbol†



positive logic: $Y = AB$

pin assignments

J, N PACKAGES			
1	1A	8	3Y
2	1B	9	3A
3	1Y	10	3B
4	2A	11	4Y
5	2B	12	4A
6	2Y	13	4B
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	3Y
3	1B	13	3A
4	1Y	14	3B
5	nc	15	nc
6	2A	16	4Y
7	nc	17	nc
8	2B	18	4A
9	2Y	19	4B
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

09

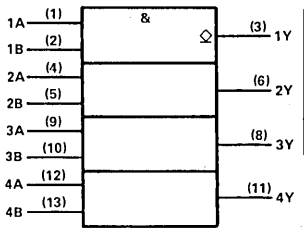
QUADRUPLE 2-INPUT POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

SN5409 (J,FH) SN7409 (J,N)
SN54ALS09 (J,FH) SN74ALS09 (N,FN)
SN54LS09 (J,FH) SN74LS09 (J,N,FN)
SN54S09 (J,FH) SN74S09 (J,N,FN)

typical performance

TYPE	POWER	DELAY
'09	19.4 mW	18.5 ns
'ALS09	2.22 mW	15 ns
'LS09	4.25 mW	20 ns
'S09	32 mW	6.5 ns

logic symbol†



positive logic: $Y = AB$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3Y	1	nc	11	nc
2	1B	9	3A	2	1A	12	3Y
3	1Y	10	3B	3	1B	13	3A
4	2A	11	4Y	4	1Y	14	3B
5	2B	12	4A	5	nc	15	nc
6	2Y	13	4B	6	2A	16	4Y
7	GND	14	V_{CC}	7	nc	17	nc
				8	2B	18	4A
				9	2Y	19	4B
				10	GND	20	V_{CC}

10

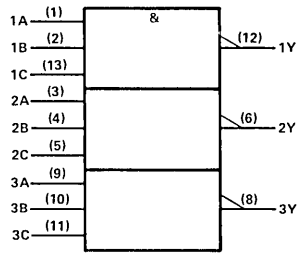
TRIPLE 3-INPUT POSITIVE-NAND GATES

SN5410 (J,FH) SN7410 (J,N)
SN54ALS10 (J,FH) SN74ALS10 (N,FN)
SN54H10 (J) SN74H10 (J,N)
SN54L10 (J)
SN54LS10 (J,FH) SN74LS10 (J,N,FN)
SN54S10 (J,FH) SN74S10 (J,N,FN)

typical performance

TYPE	POWER	DELAY
'10	10 mW	10 ns
'ALS10	1.27 mW	7 ns
'H10	22 mW	6 ns
'L10	1 mW	33 ns
'LS10	2 mW	9.5 ns
'S10	19 mW	3 ns

logic symbol†



positive logic: $Y = \overline{ABC}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3Y	1	nc	11	nc
2	1B	9	3A	2	1A	12	3Y
3	2A	10	3B	3	1B	13	3A
4	2B	11	3C	4	2A	14	3B
5	2C	12	1Y	5	nc	15	nc
6	2Y	13	1C	6	2B	16	3C
7	GND	14	V_{CC}	7	nc	17	nc
				8	2C	18	1Y
				9	2Y	19	1C
				10	GND	20	V_{CC}

11

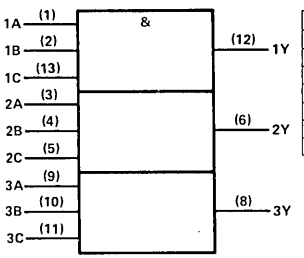
TRIPLE 3-INPUT POSITIVE-AND GATES

SN54ALS11 (J,FH) SN74ALS11 (N,FN)
SN54H11 (J) SN74H11 (J,N)
SN54LS11 (J,FH) SN74LS11 (J,N,FN)
SN54S11 (J,FH) SN74S11 (J,N,FN)

typical performance

TYPE	POWER	DELAY
'ALS11	2.17 mW	9 ns
'H11	40 mW	8.2 ns
'LS11	4.25 mW	12 ns
'S11	31 mW	4.75 ns

logic symbol†



positive logic: $Y = ABC$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3Y	1	nc	11	nc
2	1B	9	3A	2	1A	12	3Y
3	2A	10	3B	3	1B	13	3A
4	2B	11	3C	4	2A	14	3B
5	2C	12	1Y	5	nc	15	nc
6	2Y	13	1C	6	2B	16	3C
7	GND	14	V_{CC}	7	nc	17	nc
				8	2C	18	1Y
				9	2Y	19	1C
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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12

TRIPLE 3-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

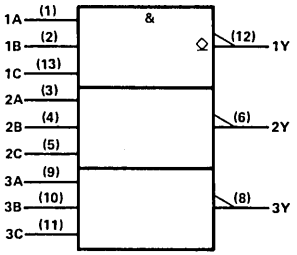
SN5412 (J,FH)
SN54ALS12 (J,FH)
SN54LS12 (J,FH)

SN7412 (J,N)
SN74ALS12 (N,FN)
SN74LS12 (J,N,FN)

typical performance

TYPE	POWER	DELAY
'12	10 mW	22 ns
'ALS12	1.27 mW	17.5 ns
'LS12	2 mW	16 ns

logic symbol†



positive logic: $Y = \overline{ABC}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3Y	1	nc	11	nc
2	1B	9	3A	2	1A	12	3Y
3	2A	10	3B	3	1B	13	3A
4	2B	11	3C	4	2A	14	3B
5	2C	12	1Y	5	nc	15	nc
6	2Y	13	1C	6	2B	16	3C
7	GND	14	V_{CC}	7	nc	17	nc
				8	2C	18	1Y
				9	2Y	19	1C
				10	GND	20	V_{CC}

13

DUAL 4-INPUT POSITIVE-NAND SCHMITT TRIGGERS

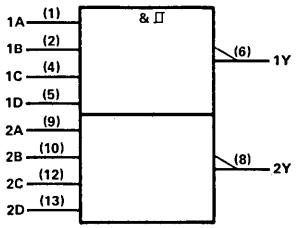
SN5413 (J,FH)
SN54LS13 (J,FH)

SN7413 (J,N)
SN74LS13 (J,N,FN)

typical performance

TYPE	HYSTERESIS	DELAY
'13	0.8 V	16.5 ns
'LS13	0.8 V	16.5 ns

logic symbol†



positive logic: $Y = \overline{ABCD}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	2Y	1	nc	11	nc
2	1B	9	2A	2	1A	12	2Y
3	nc	10	2B	3	1B	13	2A
4	1C	11	nc	4	nc	14	2B
5	1D	12	2C	5	nc	15	nc
6	1Y	13	2D	6	1C	16	nc
7	GND	14	V_{CC}	7	nc	17	nc
				8	1D	18	2C
				9	1Y	19	2D
				10	GND	20	V_{CC}

14

HEX SCHMITT-TRIGGER INVERTERS

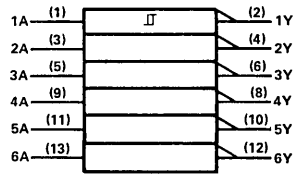
SN5414 (J,FH)
SN54LS14 (J,FH)

SN7414 (J,N)
SN74LS14 (J,N,FN)

typical performance

TYPE	HYSTERESIS	DELAY
'14	0.8 V	15 ns
'LS14	0.8 V	15 ns

logic symbol†



positive logic: $Y = \overline{A}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	4Y	1	nc	11	nc
2	1Y	9	4A	2	1A	12	4Y
3	2A	10	5Y	3	1Y	13	4A
4	2Y	11	5A	4	2A	14	5Y
5	3A	12	6Y	5	nc	15	nc
6	3Y	13	6A	6	2Y	16	5A
7	GND	14	V_{CC}	7	nc	17	nc
				8	3A	18	6Y
				9	3Y	19	6A
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

15

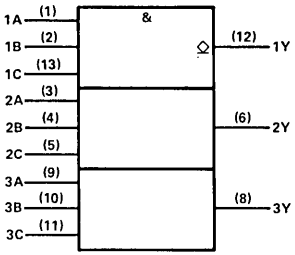
TRIPLE 3-INPUT POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

typical performance

TYPE	POWER	DELAY
'ALS15	2.22 mW	15 ns
'H15	38 mW	10.5 ns
'LS15	4.25 mW	15 ns
'S15	28 mW	15 ns

SN54ALS15 (J,FH) SN74ALS15 (N,FN)
SN54H15 (J) SN74H15 (J,N)
SN54LS15 (J,FH) SN74LS15 (J,N,FN)
SN54S15 (J,FH) SN74S15 (J,N,FN)

logic symbol†



positive logic: $Y = ABC$

pin assignments

J, N PACKAGES			
1	1A	8	3Y
2	1B	9	3A
3	2A	10	3B
4	2B	11	3C
5	2C	12	1Y
6	2Y	13	1C
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	3Y
3	1B	13	3A
4	2A	14	3B
5	nc	15	nc
6	2B	16	3C
7	nc	17	nc
8	2C	18	1Y
9	2Y	19	1C
10	GND	20	V_{CC}

16

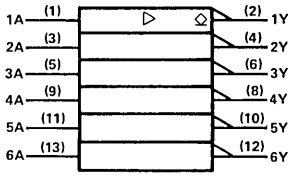
HEX INVERTER BUFFER/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

typical performance

TYPE	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	TYPICAL DELAY TIME	TYPICAL POWER PER GATE
SN74'	15 V	40 mA	12.5 ns	26 mW
SN54'	15 V	30 mA	12.5 ns	26 mW

SN5416 (J) SN7416 (J,N)

logic symbol†



positive logic: $Y = \overline{A}$

pin assignments

J, N PACKAGES			
1	1A	8	4Y
2	1Y	9	4A
3	2A	10	5Y
4	2Y	11	5A
5	3A	12	6Y
6	3Y	13	6A
7	GND	14	V_{CC}

17

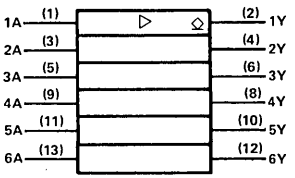
HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

typical performance

TYPE	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	TYPICAL DELAY TIME	TYPICAL POWER PER GATE
SN74'	15 V	40 mA	13 ns	21 mW
SN54'	15 V	30 mA	13 ns	21 mW

SN5417 (J) SN7417 (J,N)

logic symbol†



positive logic: $Y = A$

pin assignments

J, N PACKAGES			
1	1A	8	4Y
2	1Y	9	4A
3	2A	10	5Y
4	2Y	11	5A
5	3A	12	6Y
6	3Y	13	6A
7	GND	14	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

18

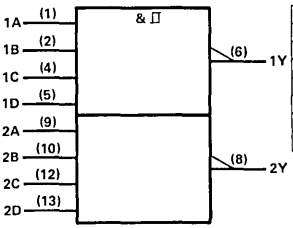
SCHMITT-TRIGGER POSITIVE-NAND GATES WITH TOTEM-POLE OUTPUTS

SN54LS18 (J,FH) SN74LS18 (J,N,FN)

typical performance

TYPE	HYSTERESIS	DELAY
'LS18	0.7 V	25 ns

logic symbol†



positive logic: $Y = \overline{ABCD}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	2Y	1	nc	11	nc
2	1B	9	2A	2	1A	12	2Y
3	nc	10	2B	3	1B	13	2A
4	1C	11	nc	4	nc	14	2B
5	1D	12	2C	5	nc	15	nc
6	1Y	13	2D	6	1C	16	nc
7	GND	14	V_{CC}	7	nc	17	nc
				8	1D	18	2C
				9	1Y	19	2D
				10	GND	20	V_{CC}

19

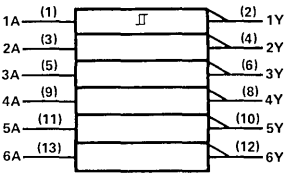
SCHMITT-TRIGGER INVERTERS WITH TOTEM-POLE OUTPUTS

SN54LS19 (J,FH) SN74LS19 (J,N,FN)

typical performance

TYPE	HYSTERESIS	DELAY
'LS19	0.7 V	16 ns

logic symbol†



positive logic: $Y = \overline{A}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	4Y	1	nc	11	nc
2	1Y	9	4A	2	1A	12	4Y
3	2A	10	5Y	3	1Y	13	4A
4	2Y	11	5A	4	2A	14	5Y
5	3A	12	6Y	5	nc	15	nc
6	3Y	13	6A	6	2Y	16	5A
7	GND	14	V_{CC}	7	nc	17	nc
				8	3A	18	6Y
				9	3Y	19	6A
				10	GND	20	V_{CC}

20

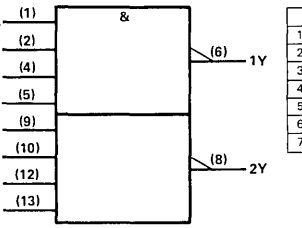
DUAL 4-INPUT POSITIVE-NAND GATES

SN5420 (J,FH) SN7420 (J,N)
SN54ALS20A (J,FH) SN74ALS20A (N,FN)
SN54H20 (J) SN74H20 (J,N)
SN54L20 (J)
SN54LS20 (J,FH) SN74LS20 (J,N,FN)
SN54S20 (J,FH) SN74S20 (J,N,FN)

typical performance

TYPE	POWER	DELAY
'20	10 mW	10 ns
'ALS20A	1.29 mW	4 ns
'H20	22 mW	6 ns
'L20	1 mW	33 ns
'LS20	2 mW	9.5 ns
'S20	19 mW	3 ns

logic symbol†



positive logic: $Y = \overline{ABCD}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	2Y	1	nc	11	nc
2	1B	9	2A	2	1A	12	2Y
3	nc	10	2B	3	1B	13	2A
4	1C	11	nc	4	nc	14	2B
5	1D	12	2C	5	nc	15	nc
6	1Y	13	2D	6	1C	16	nc
7	GND	14	V_{CC}	7	nc	17	nc
				8	1D	18	2C
				9	1Y	19	2D
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

21

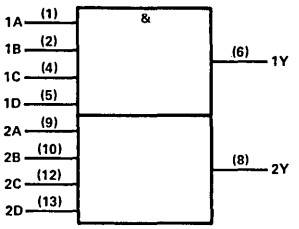
DUAL 4-INPUT POSITIVE-AND GATES

typical performance

TYPE	POWER	DELAY
'ALS21	2.21 mW	8.5 ns
'H21	40 mW	8.2 ns
'LS21	4.25 mW	12 ns

SN54ALS21 (J,FH) SN74ALS21 (N,FN)
SN54H21 (J) SN74H21 (J,N)
SN54LS21 (J,FH) SN74LS21 (J,N,FN)

logic symbol†



positive logic: $Y = ABCD$

pin assignments

J, N PACKAGES			
1	1A	8	2Y
2	1B	9	2A
3	nc	10	2B
4	1C	11	nc
5	1D	12	2C
6	1Y	13	2D
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	2Y
3	1B	13	2A
4	nc	14	2B
5	nc	15	nc
6	1C	16	nc
7	nc	17	nc
8	1D	18	2C
9	1Y	19	2D
10	GND	20	V_{CC}

22

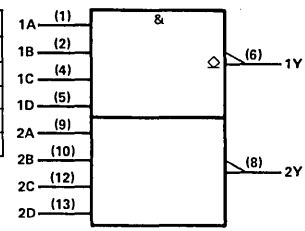
DUAL 4-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

typical performance

TYPE	POWER	DELAY
'22	10 mW	22 ns
'ALS22A	1.28 mW	16.5 ns
'H22	22 mW	8 ns
'LS22	2 mW	16 ns
'S22	17.5 mW	5 ns

SN5422 (J,FH) SN7422 (J,N)
SN54ALS22A (J,FH) SN74ALS22A (N,FN)
SN54H22 (J) SN74H22 (J,N)
SN54LS22 (J,FH) SN74LS22 (J,N,FN)
SN54S22 (J,FH) SN74S22 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{ABCD}$

pin assignments

J, N PACKAGES			
1	1A	8	2Y
2	1B	9	2A
3	nc	10	2B
4	1C	11	nc
5	1D	12	2C
6	1Y	13	2D
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	2Y
3	1B	13	2A
4	1C	14	2B
5	nc	15	nc
6	1C	16	nc
7	nc	17	nc
8	1D	18	2C
9	1Y	19	2D
10	GND	20	V_{CC}

23

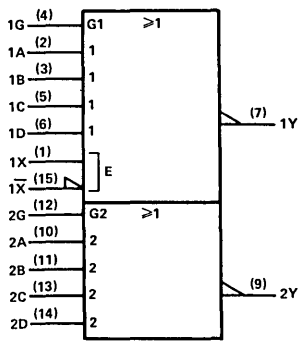
EXPANDABLE DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE

typical performance

TYPE	POWER	DELAY
'23	23 mW	10.5 ns

SN5423 (J,FH) SN7423 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	1X	9	2Y
2	1A	10	2A
3	1B	11	2B
4	1G	12	2G
5	1C	13	2C
6	1D	14	2D
7	1Y	15	$1\overline{X}$
8	GND	16	V_{CC}

FH PACKAGE			
1	nc	11	nc
2	1X	12	2Y
3	1A	13	2A
4	1B	14	2B
5	1G	15	2G
6	nc	16	nc
7	1C	17	2C
8	1D	18	2D
9	1Y	19	$1\overline{X}$
10	GND	20	V_{CC}

positive logic:
$1Y = \overline{1G\,(1A+1B+1C+1D)+X}$
$2Y = 2G\,\overline{(2A+2B+2C+2D)}$
X = output of SN5460/SN7460

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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24

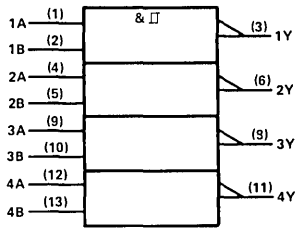
SCHMITT-TRIGGER POSITIVE-NAND GATES/INVERTERS WITH TOTEM POLE OUTPUTS

typical performance

TYPE	HYSTERESIS	DELAY
'LS24	0.7 V	19 ns

SN54LS24 (J,FH) SN74LS24 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{AB}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3Y	1	nc	11	nc
2	1B	9	3A	2	1A	12	3Y
3	1Y	10	3B	3	1B	13	3A
4	2A	11	4Y	4	1Y	14	3B
5	2B	12	4A	5	nc	15	nc
6	2Y	13	4B	6	2A	16	4Y
7	GND	14	V_{CC}	7	nc	17	nc
				8	2B	18	4A
				9	2Y	19	4B
				10	GND	20	V_{CC}

25

DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE

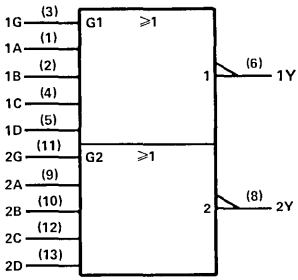
typical performance

TYPE	POWER	DELAY
'25	23 mW	10.5 ns

SN7425 (J,N)

SN5425 (J,FH) SN7425 (J,N)

logic symbol†



positive logic: $Y = \overline{G\,(A+B+C+D)}$

pin assignments

J, N PACKAGES				FH PACKAGE			
1	1A	8	2Y	1	nc	11	nc
2	1B	9	2A	2	1A	12	2Y
3	1G	10	2B	3	1B	13	2A
4	1C	11	2G	4	1G	14	2B
5	1D	12	2C	5	nc	15	nc
6	1Y	13	2D	6	1C	16	2G
7	GND	14	V_{CC}	7	nc	17	nc
				8	1D	18	2C
				9	1Y	19	2D
				10	GND	20	V_{CC}

26

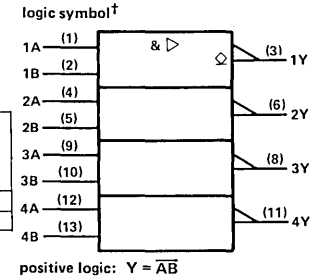
QUADRUPLE 2-INPUT HIGH-VOLTAGE INTERFACE POSITIVE-NAND GATES

typical performance

TYPE	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	POWER	DELAY
'26	15 V	16 mA	10 mW	13.5 ns
'LS26	15 V	4 mA	2 mW	16 ns

SN5426 (J,FH) SN7426 (J,N)
SN54LS26 (J,FH) SN74LS26 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{AB}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3Y	1	nc	11	nc
2	1B	9	3A	2	1A	12	3Y
3	1Y	10	3B	3	1B	13	3A
4	2A	11	4Y	4	1Y	14	3B
5	2B	12	4A	5	nc	15	nc
6	2Y	13	4B	6	2A	16	4Y
7	GND	14	V_{CC}	7	nc	17	nc
				8	2B	18	4A
				9	2Y	19	4B
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

27

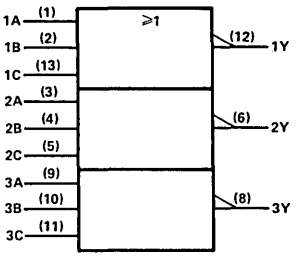
TRIPLE 3-INPUT POSITIVE-NOR GATES

typical performance

TYPE	POWER	DELAY
'27	22 mW	8.5 ns
'ALS27	2.48 mW	6 ns
'LS27	4.5 mW	10 ns

SN5427 (J,FH) SN7427 (J,N)
SN54ALS27 (J,FH) SN74ALS27 (N,FN)
SN54LS27 (J,FH) SN74LS27 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{A+B+C}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3Y	1	nc	11	nc
2	1B	9	3A	2	1A	12	3Y
3	2A	10	3B	3	1B	13	3A
4	2B	11	3C	4	2A	14	3B
5	2C	12	1Y	5	nc	15	nc
6	2Y	13	1C	6	2B	16	3C
7	GND	14	V_{CC}	7	nc	17	nc
				8	2C	18	1Y
				9	2Y	19	1C
				10	GND	20	V_{CC}

28

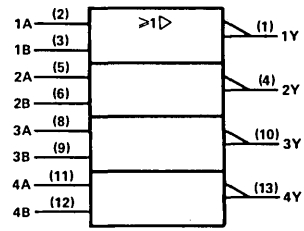
QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS

performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	POWER (TYP)	DELAY (TYP)
'28	48 mA	−2.4 mA	28 mW	7 ns
SN54ALS'	12 mA	−1 mA	4.06 mW	4 ns
SN74ALS'	24 mA	−2.6 mA	4.06 mW	4 ns
SN54LS'	12 mA	−1.2 mA	5.5 mW	12 ns
SN74LS'	24 mA	−1.2 mA	5.5 mW	12 ns

SN5428 (J,FH) SN7428 (J,N)
SN54ALS28 (J,FH) SN74ALS28 (N,FN)
SN54LS28 (J,FH) SN74LS28 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{A+B}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1Y	8	3A	1	nc	11	nc
2	1A	9	3B	2	1Y	12	3A
3	1B	10	3Y	3	1A	13	3B
4	2Y	11	4A	4	1B	14	3Y
5	2A	12	4B	5	nc	15	nc
6	2B	13	4Y	6	2Y	16	4A
7	GND	14	V_{CC}	7	nc	17	nc
				8	2A	18	4B
				9	2B	19	4Y
				10	GND	20	V_{CC}

30

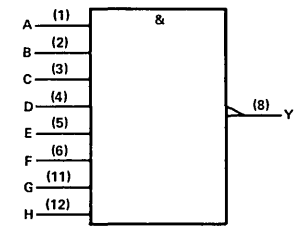
8-INPUT POSITIVE-NAND GATE

typical performance

TYPE	POWER	DELAY
'30	10 mW	10 ns
'ALS30	1.9 mW	7 ns
'H30	22 mW	6 ns
'L30	1 mW	33 ns
'LS30	2.4 mW	17 ns
'S30	19 mW	3 ns

SN5430 (J,FH) SN7430 (J,N)
SN54ALS30 (J,FH) SN74ALS30 (N, FN)
SN54H30 (J) SN74H30 (J,N)
SN54L30 (J)
SN54LS30 (J,FH) SN74LS30 (J,N,FN)
SN54S30 (J,FH) SN74S30 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{ABCDEFGH}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A	8	Y	1	nc	11	nc
2	B	9	nc	2	A	12	Y
3	C	10	nc	3	B	13	nc
4	D	11	G	4	C	14	nc
5	E	12	H	5	nc	15	nc
6	F	13	nc	6	D	16	G
7	GND	14	V_{CC}	7	nc	17	nc
				8	E	18	H
				9	F	19	nc
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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31

DELAY ELEMENTS
(delay elements for generating delay lines)

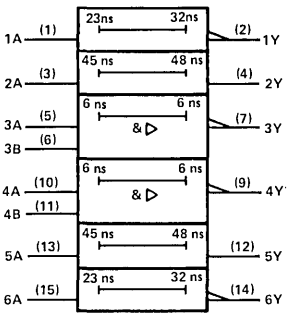
- Buffers 3 and 4 offer 3-fold increase in I_{OL} (12 mA/24 mA)
- Total power dissipation 38 mW

typical performance

DELAY ELEMENT	LOGIC	DELAY
Gates 1 and 6	Inverting	27.5 ns
Gates 2 and 5	Noninverting	46.5 ns
Buffers 3 and 4	2-Input NAND	6 ns

SN54LS31 (J,FH) SN74LS31 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	9	4Y	1	nc	11	nc
2	1Y	10	4A	2	1A	12	4Y
3	2A	11	4B	3	1Y	13	4A
4	2Y	12	5Y	4	2A	14	4B
5	3A	13	5A	5	2Y	15	5Y
6	3B	14	6Y	6	nc	16	nc
7	3Y	15	6A	7	3A	17	5A
8	GND	16	V_{CC}	8	3B	18	6Y
				9	3Y	19	6A
				10	GND	20	V_{CC}

32

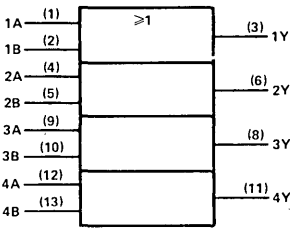
QUADRUPLE 2-INPUT POSITIVE-OR GATE

typical performance

TYPE	POWER	DELAY
'32	24 mW	12 ns
'ALS32	2.81 mW	5.5 ns
'LS32	5 mW	12 ns
'S32	35 mW	4 ns

SN5432 (J,FH) SN7432 (J,N)
SN54ALS32 (J,FH) SN74ALS32 (N,FN)
SN54LS32 (J,FH) SN74LS32 (J,N,FN)
SN54S32 (J,FH) SN74S32 (J,N,FN)

logic symbol†



positive logic: Y = A+B

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3Y	1	nc	11	nc
2	1B	9	3A	2	1A	12	3Y
3	1Y	10	3B	3	1B	13	3A
4	2A	11	4Y	4	1Y	14	3B
5	2B	12	4A	5	nc	15	nc
6	2Y	13	4B	6	2A	16	4Y
7	GND	14	V_{CC}	7	nc	17	nc
				8	2B	18	4A
				9	2Y	19	4B
				10	GND	20	V_{CC}

33

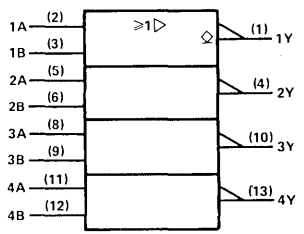
QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS WITH OPEN-COLLECTOR OUTPUTS

performance

TYPE	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	POWER (TYP)	DELAY (TYP)
'33	5.5 V	48 mA	28 mW	11 ns
SN54ALS'	5.5 V	12 mA	4.06 mW	14.5 ns
SN74ALS'	5.5 V	24 mA	4.06 mW	14.5 ns
SN54LS'	5.5 V	12 mA	5.45 mW	19 ns
SN74LS'	5.5 V	24 mA	5.45 mW	19 ns

SN5433 (J,FH) SN7433 (J,N)
SN54ALS33 (J,FH) SN74ALS33 (N,FN)
SN54LS33 (J,FH) SN74LS33 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{A+B}$

pin assignments

J, N PACKAGES			
1	1Y	8	3A
2	1A	9	3B
3	1B	10	3Y
4	2Y	11	4A
5	2A	12	4B
6	2B	13	4Y
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1Y	12	3A
3	1A	13	3B
4	1B	14	3Y
5	nc	15	nc
6	2Y	16	4A
7	nc	17	nc
8	2A	18	4B
9	2B	19	4Y
10	GND	20	V_{CC}

nc — no internal connection.
†Pin numbers shown on logic symbols are for J and N packages only.

37

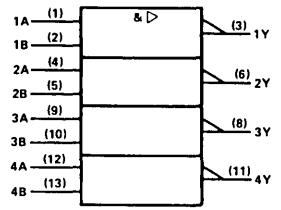
QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS

performance

TYPE	HIGH-LEVEL OUTPUT CURRENT	LOW-LEVEL OUTPUT CURRENT	POWER (TYP)	DELAY (TYP)
37	4.8 mA	−1.2 mA	27 mW	10.5 ns
SN54ALS'	12 mA	−1 mA	3.04 mW	4 ns
SN74ALS'	24 mA	−2.6 mA	3.04 mW	4 ns
SN54LS'	12 mA	−1.2 mA	4.3 mW	12 ns
SN74LS'	24 mA	−1.2 mA	4.3 mW	12 ns
'S37	60 mA	−3 mA	41 mW	4 ns

SN5437 (J,FH) SN7437 (J,N)
SN54ALS37 (J,FH) SN74ALS37 (N,FN)
SN54LS37 (J,FH) SN74LS37 (J,N,FN)
SN54S37 (J,FH) SN74S37 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{AB}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3Y	1	nc	11	nc
2	1B	9	3A	2	1A	12	3Y
3	1Y	10	3B	3	1B	13	3A
4	2A	11	4Y	4	1Y	14	3B
5	2B	12	4A	5	nc	15	nc
6	2Y	13	4B	6	2A	16	4Y
7	GND	14	V_{CC}	7	nc	17	nc
				8	2B	18	4A
				9	2Y	19	4B
				10	GND	20	V_{CC}

38

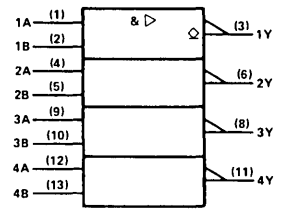
QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

performance

TYPE	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	POWER (TYP)	DELAY (TYP)
'38	5.5 V	48 mA	24.4 mW	12.5 ns
SN54ALS'	5.5 V	12 mA	3.04 mW	14.5 ns
SN74ALS'	5.5 V	24 mA	3.04 mW	14.5 ns
SN54ALS'	5.5 V	12 mA	4.3 mW	19 ns
SN74ALS'	5.5 V	24 mA	4.3 mW	19 ns
'S38	5.5 V	60 mA	41 mW	6.5 ns

SN5438 (J,FH) SN7438 (J,N)
SN54ALS38 (J,FH) SN74ALS38 (N,FN)
SN54LS38 (J,FH) SN74LS38 (J,N,FN)
SN54S38 (J,FH) SN74S38 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{AB}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3Y	1	nc	11	nc
2	1B	9	3A	2	1A	12	3Y
3	1Y	10	3B	3	1B	13	3A
4	2A	11	4Y	4	1Y	14	3B
5	2B	12	4A	5	nc	15	nc
6	2Y	13	4B	6	2A	16	4Y
7	GND	14	V_{CC}	7	nc	17	nc
				8	2B	18	4A
				9	2Y	19	4B
				10	GND	20	V_{CC}

39

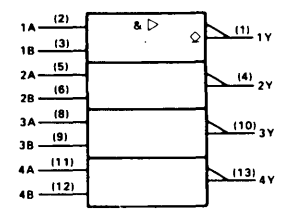
QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

performance

TYPE	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	POWER (TYP)	DELAY (TYP)
SN5439	5.5 V	60 mA	24.4 mW	12.5 ns
SN7439	5.5 V	80 mA	24.4 mW	12.5 ns

SN5439 (J,FH) SN7439 (J,N)

logic symbol†



positive logic: $Y = \overline{AB}$

pin assignments

J, N PACKAGES				FH PACKAGE			
1	1Y	8	3A	1	nc	11	nc
2	1A	9	3B	2	1Y	12	3A
3	1B	10	3Y	3	1A	13	3B
4	2Y	11	4A	4	1B	14	3Y
5	2A	12	4B	5	nc	15	nc
6	2B	13	4Y	6	2Y	16	4A
7	GND	14	V_{CC}	7	nc	17	nc
				8	2A	18	4B
				9	2B	19	4Y
				10	GND	20	V_{CC}

nc — no internal connection.
†Pin numbers shown on logic symbols are for J and N packages only.

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40

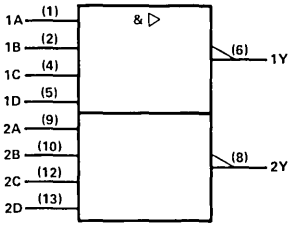
DUAL 4-INPUT POSITIVE NAND BUFFERS

performance

TYPE	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	POWER (TYP)	DELAY (TYP)
'40	48 mA	−1.2 mA	26 mW	10.5 ns
SN54ALS'	12 mA	−1 mA	3.04 mW	4 ns
SN74ALS'	24 mA	−2.6 mA	3.04 mW	4 ns
'H40	60 mA	−1.5 mA	44 mW	7.5 ns
SN54LS'	12 mA	−1.2 mA	4.3 mW	12 ns
SN74LS'	24 mA	−1.2 mA	4.3 mW	12 ns
'S40	60 mA	−3 mA	44 mW	4 ns

SN5440 (J,FH) SN7440 (J,N)
SN54ALS40 (J,FH) SN74ALS40 (N,FN)
SN54H40 (J) SN74H40 (J,N)
SN54LS40 (J,FH) SN74LS40 (J,N,FN)
SN54S40 (J,FH) SN74S40 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{ABCD}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	2Y	1	nc	11	nc
2	1B	9	2A	2	1A	12	2Y
3	nc	10	2B	3	1B	13	2A
4	1C	11	nc	4	nc	14	2B
5	1D	12	2C	5	nc	15	nc
6	1Y	13	2D	6	1C	16	nc
7	GND	14	V_{CC}	7	nc	17	nc
				8	1D	18	2C
				9	1Y	19	2D
				10	GND	20	V_{CC}

42

4-LINE TO 10-LINE DECODERS

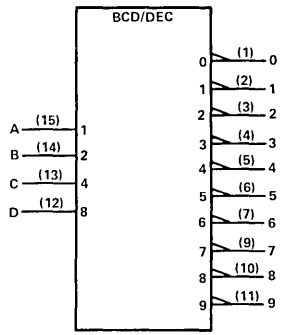
(BCD to decimal)

typical performance

TYPE	SELECT TIME	POWER
'42A	17 ns	140 mW
'L42	34 ns	70 mW
'LS42	17 ns	35 mW

SN5442A (J,FH) SN7442A (J,N)
SN54L42 (J)
SN54LS42 (J,FH) SN74LS42 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	0	9	7	1	nc	11	nc
2	1	10	8	2	0	12	7
3	2	11	9	3	1	13	8
4	3	12	D	4	2	14	9
5	4	13	C	5	3	15	D
6	5	14	B	6	nc	16	nc
7	6	15	A	7	4	17	C
8	GND	16	V_{CC}	8	5	18	B
				9	6	19	A
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

43

4-LINE TO 10-LINE DECODERS (EXCESS 3 TO DECIMAL)

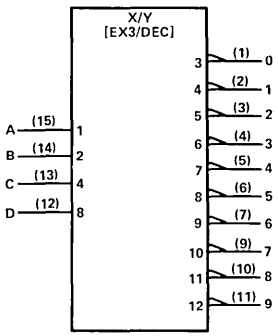
SN5443A (J,FH)
SN54L43 (J)

SN7443A (J,N)

typical performance

TYPE	SELECT TIME	POWER
'43A	17 ns	140 mW
'L43	34 ns	70 mW

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	0	9	7	1	nc	11	nc
2	1	10	8	2	0	12	7
3	2	11	9	3	1	13	8
4	3	12	D	4	2	14	9
5	4	13	C	5	3	15	D
6	5	14	B	6	nc	16	nc
7	6	15	A	7	4	17	C
8	GND	16	V_{CC}	8	5	18	B
				9	6	19	A
				10	GND	20	V_{CC}

44

4-LINE TO 10-LINE DECODERS (EXCESS 3-GRAY TO DECIMAL)

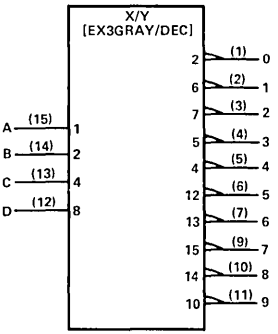
SN5444A (J,FH)
SN54L44 (J)

SN7444A (J,N)

typical performance

TYPE	SELECT TIME	POWER
'44A	17 ns	140 mW
'L44	34 ns	70 mW

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	0	9	7	1	nc	11	nc
2	1	10	8	2	0	12	7
3	2	11	9	3	1	13	8
4	3	12	D	4	2	14	9
5	4	13	C	5	3	15	D
6	5	14	B	6	nc	16	nc
7	6	15	A	7	4	17	C
8	GND	16	V_{CC}	8	5	18	B
				9	6	19	A
				10	GND	20	V_{CC}

45

BCD-TO-DECIMAL DECODER/DRIVER

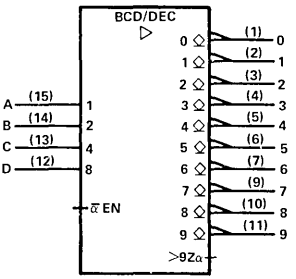
SN5445 (J,FH)

SN7445 (J,N)

typical performance

TYPE	OFF-STATE OUTPUT VOLTAGE	POWER
'45	30 V	215 mW

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	0	9	7	1	nc	11	nc
2	1	10	8	2	0	12	7
3	2	11	9	3	1	13	8
4	3	12	D	4	2	14	9
5	4	13	C	5	3	15	D
6	5	14	B	6	nc	16	nc
7	6	15	A	7	4	17	C
8	GND	16	V_{CC}	8	5	18	B
				9	6	19	A
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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46,47

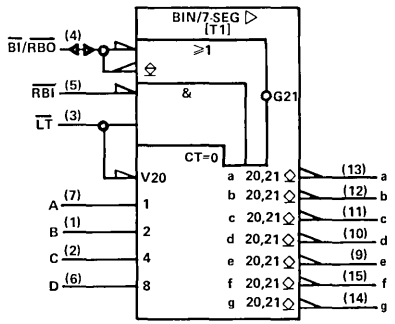
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS
(46 - 30 V OUTPUTS
47 - 15 V OUTPUTS)

typical performance

TYPE	OFF-STATE OUTPUT VOLTAGE	POWER
'46A	30 V	320 mW
'L46	30 V	133 mW
'47A	15 V	320 mW
'L47	15 V	133 mW
'LS47	15 V	35 mW

SN5446A (J,FH) SN7446A (J,N)
SN54L46 (J)
SN5447A (J,FH) SN7447A (J,N)
SN54L47 (J)
SN54LS47(J,FH) SN74LS47 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	B	9	e	1	nc	11	nc
2	C	10	d	2	B	12	e
3	$\overline{LT}$	11	c	3	C	13	d
4	$\overline{BI/RBO}$	12	b	4	$\overline{LT}$	14	c
5	$\overline{RBI}$	13	a	5	$\overline{BI/RBO}$	15	b
6	D	14	g	6	nc	16	nc
7	A	15	f	7	$\overline{RBI}$	17	a
8	GND	16	V_{CC}	8	D	18	g
				9	A	19	f
				10	GND	20	V_{CC}

48

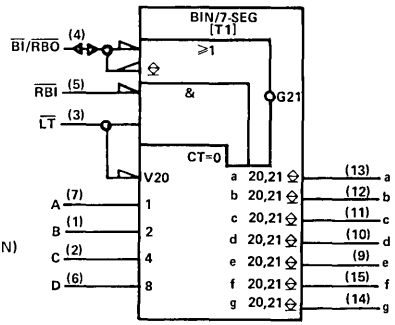
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

typical performance

TYPE	OFF-STATE OUTPUT VOLTAGE	POWER
'48	5.5 V	265 mW
'LS48	5.5 V	125 mW

SN5448 (J,FH) SN7448 (J,N)
SN54LS48 (J,FH) SN74LS48 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	B	9	e	1	nc	11	nc
2	C	10	d	2	B	12	e
3	$\overline{LT}$	11	c	3	C	13	d
4	$\overline{BI/RBO}$	12	b	4	$\overline{LT}$	14	c
5	$\overline{RBI}$	13	a	5	$\overline{BI/RBO}$	15	b
6	D	14	g	6	nc	16	nc
7	A	15	f	7	$\overline{RBI}$	17	a
8	GND	16	V_{CC}	8	D	18	g
				9	A	19	f
				10	GND	20	V_{CC}

49

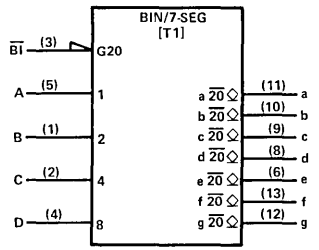
BCD TO SEVEN SEGMENT DECODERS/DRIVERS
(OPEN-COLLECTOR OUTPUTS)

typical performance

TYPE	OFF-STATE OUTPUT VOLTAGE	POWER
'49	5.5 V	165 mW
'LS49	5.5 V	40 mW

SN5449 (J,FH) SN7449 (J,N)
SN54LS49 (J,FH) SN74LS49 (J,N,FN)

logic symbol†

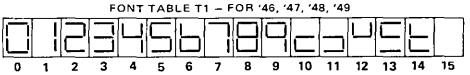


pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	B	8	d	1	nc	11	nc
2	C	9	c	2	B	12	d
3	$\overline{BI}$	10	b	3	C	13	c
4	D	11	a	4	$\overline{BI}$	14	b
5	A	12	g	5	nc	15	nc
6	e	13	f	6	D	16	a
7	GND	14	V_{CC}	7	nc	17	nc
				8	A	18	g
				9	e	19	f
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

FONT TABLE T1 – FOR '46, '47, '48, '49



50

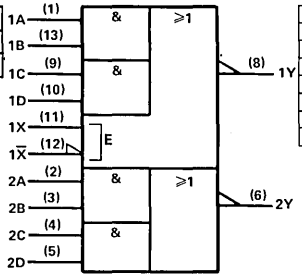
DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES (ONE GATE EXPANDABLE)

typical performance

TYPE	POWER	DELAY
'50	14 mW	10.5 ns
'H50	29 mW	6.5 ns

SN5450 (J,FH) SN7450 (J,N)
SN54H50 (J) SN74H50 (J,N)

logic symbol†



positive logic: $Y = \overline{AB+CD+X}$
'50: X = output of SN5460/SN7460
'H50: X = output of SN54H60/SN74H60 or SN54H62/SN74H62

pin assignments

J, N PACKAGES				FH PACKAGE			
1	1A	8	1Y	1	nc	11	nc
2	2A	9	1C	2	1A	12	1Y
3	2B	10	1D	3	2A	13	1C
4	2C	11	1X	4	2B	14	1D
5	2D	12	1X̄	5	nc	15	nc
6	2Y	13	1B	6	2C	16	1X
7	GND	14	V_{CC}	7	nc	17	nc
				8	2D	18	1X̄
				9	2Y	19	1B
				10	GND	20	V_{CC}

51

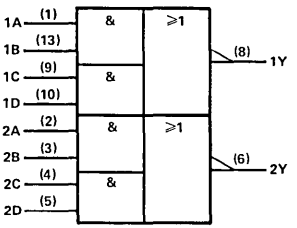
AND-OR INVERT GATES

typical performance

TYPE	POWER	DELAY
'51	14 mW	10.5 ns
'H51	29 mW	65 ns
'L51	1.5 mW	43 ns
'LS51	2.75 mW	12.5 ns
'S51	28 mW	3.5 ns

SN5451 (J,FH) SN7451 (J,N)
SN54H51 (J) SN74H51 (J,N)
SN54L51 (J)
SN54LS51 (J,FH) SN74LS51(J,N,FN)
SN54S51 (J,FH) SN74S51 (J,N,FN)

logic symbol, '51, 'H51, 'S51†

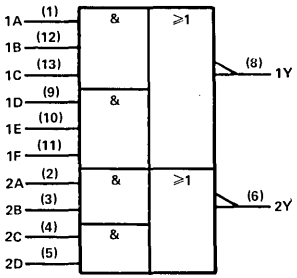


positive logic: $Y = \overline{AB+CD}$

pin assignments, '51, 'H51, 'S51

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	1Y	1	nc	11	nc
2	2A	9	1C	2	1A	12	1Y
3	2B	10	1D	3	2A	13	1C
4	2C	11	nu	4	2B	14	1D
5	2D	12	nu	5	nc	15	nc
6	2Y	13	1B	6	2C	16	nu
7	GND	14	V_{CC}	7	nc	17	nc
				8	2D	18	nu
				9	2Y	19	1B
				10	GND	20	V_{CC}

logic symbol, 'L51, 'LS51†



positive logic:

$1Y = \overline{(1A \cdot 1B \cdot 1C)+(1D \cdot 1E \cdot 1F)}$

$2Y = \overline{(2A \cdot 2B)+(2C \cdot 2D)}$

pin assignments, 'L51, 'LS51

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	1Y	1	nc	11	nc
2	2A	9	1D	2	1A	12	1Y
3	2B	10	1E	3	2A	13	1D
4	2C	11	1F	4	2B	14	1E
5	2D	12	1B	5	nc	15	nc
6	2Y	13	1C	6	2C	16	1F
7	GND	14	V_{CC}	7	nc	17	nc
				8	2D	18	1B
				9	2Y	19	1C
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.
nu — make no external connection.

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52

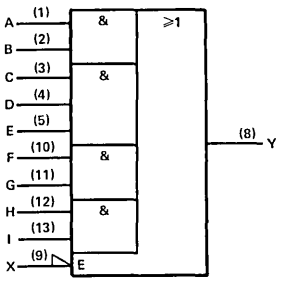
EXPANDABLE 4-WIDE AND-OR GATES

SN54H52 (J,FH) SN74H52 (J,N)

typical performance

TYPE	POWER	DELAY
'H52	88 mW	9.9 ns

logic symbol†



positive logic: Y = AB+CDE+FG+HI+X
X = output of SN54H61/SN74H61

pin assignments

J, N PACKAGES				FH PACKAGE			
1	A	8	Y	1	nc	11	nc
2	B	9	X	2	A	12	Y
3	C	10	F	3	B	13	X
4	D	11	G	4	C	14	F
5	E	12	H	5	nc	15	nc
6	nc	13	I	6	D	16	G
7	GND	14	V_{CC}	7	nc	17	nc
				8	E	18	H
				9	nc	19	I
				10	GND	20	V_{CC}

53

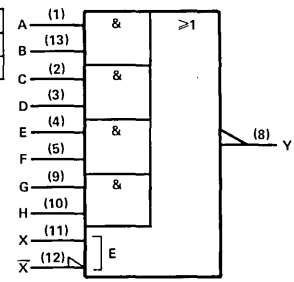
EXPANDABLE 4-WIDE AND-OR-INVERT GATES

SN5453 (J,FH) SN7453 (J,N)
SN54H53 (J) SN74H53 (J,N)

typical performance

TYPE	POWER	DELAY
'53	23 mW	10.5 ns
'H53	41 mW	6.6 ns

logic symbol, '53†

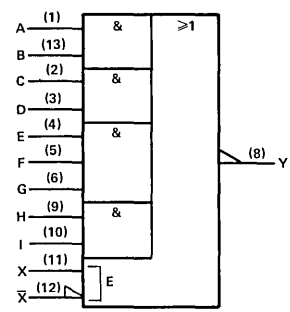


positive logic: $Y = \overline{AB+CD+EF+GH+X}$
X = output of SN5460/SN7460

pin assignments, '53

J, N PACKAGES				FH PACKAGE			
1	A	8	Y	1	nc	11	nc
2	C	9	G	2	A	12	Y
3	D	10	H	3	C	13	G
4	E	11	X	4	D	14	H
5	F	12	$\overline{X}$	5	nc	15	nc
6	nc	13	B	6	E	16	X
7	GND	14	V_{CC}	7	nc	17	nc
				8	F	18	$\overline{X}$
				9	nc	19	B
				10	GND	20	V_{CC}

logic symbol, 'H53†



positive logic: $Y = \overline{AB+CD+EFG+HI+X}$
X = output of SN54H60/SN74H60
or SN54H62/SN74H62

pin assignments, 'H53

J, N PACKAGES			
1	A	8	Y
2	C	9	H
3	D	10	I
4	E	11	X
5	F	12	$\overline{X}$
6	G	13	B
7	GND	14	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

54

4-WIDE AND-OR-INVERT GATES

typical performance

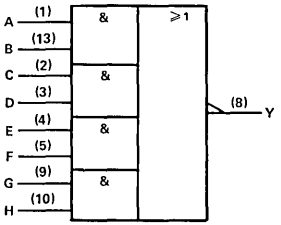
TYPE	POWER	DELAY
'54	23 mW	10.5 ns
'H54	41 mW	6.6 ns
'L54	1.5 mW	43 ns
'LS54	4.5 mW	12.5 ns

SN5454 (J,FH)
SN54H54 (J)
SN54L54 (J)
SN54LS54 (J,FH)

SN7454 (J,N)
SN74H54 (J,N)

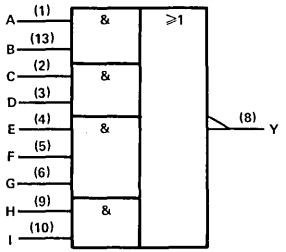
SN74LS54 (J,N,FN)

logic symbol, '54†



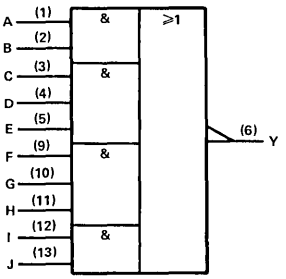
positive logic: $Y = \overline{AB+CD+EF+GH}$

logic symbol, 'H54†



positive logic: $Y = \overline{AB+CD+EFG+HI}$

logic symbol, 'L54, 'LS54†



positive logic: $Y = \overline{AB+CDE+FGH+IJ}$

pin assignments, '54

J, N PACKAGES				FH PACKAGE			
1	A	8	Y	1	nc	11	nc
2	C	9	G	2	A	12	Y
3	D	10	H	3	C	13	G
4	E	11	nu	4	D	14	H
5	F	12	nu	5	nc	15	nc
6	nc	13	B	6	E	16	nu
7	GND	14	V_{CC}	7	nc	17	nc
				8	F	18	nu
				9	nc	19	B
				10	GND	20	V_{CC}

pin assignments, 'H54

J, N PACKAGES			
1	A	8	Y
2	C	9	H
3	D	10	I
4	E	11	nu
5	F	12	nu
6	G	13	B
7	GND	14	V_{CC}

pin assignments, 'L54, 'LS54

J, N PACKAGES				FH, FN PACKAGES			
1	A	8	nc	1	nc	11	nc
2	B	9	F	2	A	12	nc
3	C	10	G	3	B	13	F
4	D	11	H	4	C	14	G
5	E	12	I	5	nc	15	nc
6	Y	13	J	6	D	16	H
7	GND	14	V_{CC}	7	nc	17	nc
				8	E	18	I
				9	Y	19	J
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.
nu — make no external connection.

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55

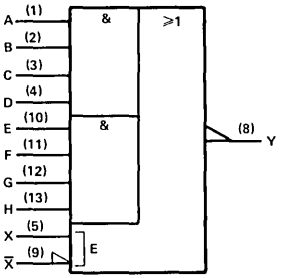
2-WIDE 4-INPUT AND-OR-INVERT GATES

typical performance

TYPE	POWER	DELAY
'H55	30 mW	6.8 ns
'L55	1.5 mW	43 ns
'LS55	2.75 mW	12.5 ns

SN54H55 (J) SN74H55 (J,N)
SN54L55 (J)
SN54LS55 (J,FH) SN74LS55 (J,N,FN)

X = Output of SN54H60/SN74H60 or SN54H62/SN74H62

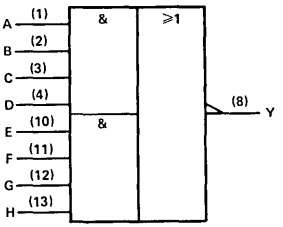


positive logic: $Y = \overline{ABCD+EFGH+X}$

pin assignments, 'H55

J, N PACKAGES			
1	A	8	Y
2	B	9	$\overline{X}$
3	C	10	E
4	D	11	F
5	X	12	G
6	nc	13	H
7	GND	14	V_{CC}

logic symbol, 'L55, 'LS55†



positive logic: $Y = \overline{ABCD+EFGH}$

pin assignments, 'L55, 'LS55

J, N PACKAGES			
1	A	8	Y
2	B	9	nc
3	C	10	E
4	D	11	F
5	nc	12	G
6	nc	13	H
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	A	12	Y
3	B	13	nc
4	C	14	E
5	nc	15	nc
6	D	16	F
7	nc	17	nc
8	nc	18	G
9	nc	19	H
10	GND	20	V_{CC}

56

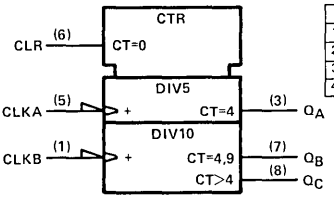
50-TO-1 FREQUENCY DIVIDER

typical performance

TYPE	CLOCK FREQUENCY	CLEAR	POWER
'LS56	25 MHz	HIGH	85 mW

SN54LS56 (JG) SN74LS56 (JG,P)

logic symbol†



pin assignments

JG, P PACKAGES			
1	CLKB	5	CLKA
2	V_{CC}	6	CLR
3	Q_A	7	Q_B
4	GND	8	Q_C

For chip carrier information, contact the factory.

†Pin numbers shown on logic symbols are for J, JG, N, and P packages only.
nc — no internal connection.

57

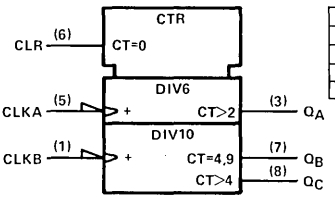
60-TO-1 FREQUENCY DIVIDER

typical performance

TYPE	CLOCK FREQUENCY	CLEAR	POWER
'LS57	25 MHz	HIGH	85 mW

SN54LS157 (JG) SN54LS157 (JG, P)

logic symbol†



pin assignments

JG, P PACKAGES			
1	CLKB	5	CLKA
2	V_{CC}	6	CLR
3	Q_A	7	Q_B
4	GND	8	Q_C

60

DUAL 4-INPUT EXPANDERS

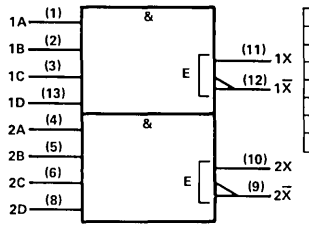
SN5460 (J) SN7460 (J,N)
SN54H60 (J) SN74H60 (J,N)

typical performance

TYPE	POWER
'60	4 mW
'H60	6 mW

'60 positive logic:
X = ABCD when connected to X and $\overline{X}$ inputs of SN5423/SN7423, SN5450/SN7450, or SN5453/SN7453
'H60 positive logic:
X = ABCD when connected to X and $\overline{X}$ inputs of SN54H50/SN74H50, SN54H53/SN74H53, or SN54H55/SN74H55

logic symbol†



pin assignments

J, N PACKAGES			
1	1A	8	2D
2	1B	9	2X̄
3	1C	10	2X
4	2A	11	1X
5	2B	12	1X̄
6	2C	13	1D
7	GND	14	V_{CC}

61

TRIPLE 3-INPUT EXPANDERS

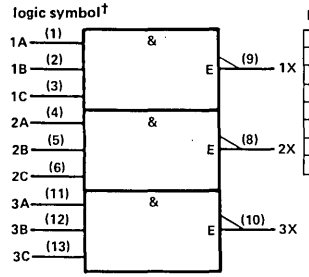
SN54H61 (J) SN74H61 (J,N)

typical performance

TYPE	POWER
'H61	13 mW

positive logic:
X = ABC when connected to X input of SN54H52/SN74H52

logic symbol†



pin assignments

J, N PACKAGES			
1	1A	8	2X
2	1B	9	1X
3	1C	10	3X
4	2A	11	3A
5	2B	12	3B
6	2C	13	3C
7	GND	14	V_{CC}

†Pin numbers shown on logic symbols are for J, JG, N, and P packages only.
nc — no internal connection.

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62

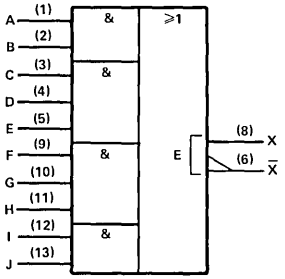
4-WIDE AND-OR EXPANDERS

typical performance

TYPE	POWER
'H62	25 mW

SN54H62 (J) SN74H62 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	A	8	X
2	B	9	F
3	C	10	G
4	D	11	H
5	E	12	I
6	X̄	13	J
7	GND	14	V_{CC}

63

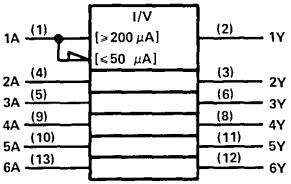
HEX CURRENT-SENSING INTERFACE GATES

typical performance

TYPE	POWER	DELAY
'LS63	3.3 mW	21 ns

SN54LS63 (J,FH) SN74LS63 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	1A	8	4Y
2	1Y	9	4A
3	2Y	10	5A
4	2A	11	5Y
5	3A	12	6Y
6	3Y	13	6A
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	4Y
3	1Y	13	4A
4	2Y	14	5A
5	nc	15	nc
6	2A	16	5Y
7	nc	17	nc
8	3A	18	6Y
9	3Y	19	6A
10	GND	20	V_{CC}

64,65

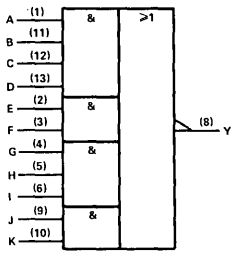
4-2-3-2 INPUT AND-OR-INVERT GATES

typical performance

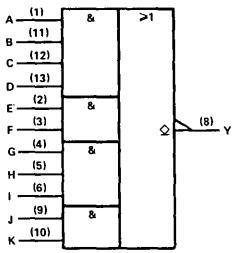
TYPE	OUTPUT	POWER	DELAY
'S64	TOTEM POLE	29 mW	3.5 ns
'S65	OPEN-COLLECTOR	36 mW	5.5 ns

SN54S64 (J,FH) SN74S64 (J,N,FN)
SN54S65 (J,FH) SN74S65 (J,N,FN)

logic symbol, 'S64†



logic symbol, 'S65†



positive logic: $Y = \overline{ABCD+EF+GHI+JK}$

pin assignments

J, N PACKAGES			
1	A	8	Y
2	E	9	J
3	F	10	K
4	G	11	B
5	H	12	C
6	I	13	D
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	A	12	Y
3	E	13	J
4	F	14	K
5	nc	15	nc
6	G	16	B
7	nc	17	nc
8	H	18	C
9	I	19	D
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

68

DUAL 4-BIT DECADE COUNTER

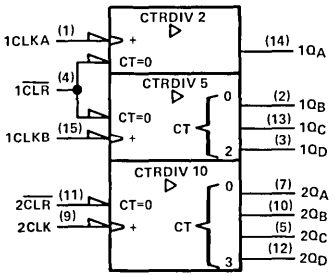
- High-drive outputs (I_{OL} rated at 8 mA/16 mA)

typical performance

COUNT FREQUENCY	CLEAR	POWER DISSIPATION
60 MHz	LOW	180 mW

SN54LS68 (J,FH) SN74LS68 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	1CLKA	9	2CLK
2	$1Q_B$	10	$2Q_B$
3	$1Q_D$	11	$2\overline{CLR}$
4	$1\overline{CLR}$	12	$2Q_D$
5	$2Q_C$	13	$1Q_C$
6	nc	14	$1Q_A$
7	$2Q_A$	15	1CLKB
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1CLKA	12	2CLK
3	$1Q_B$	13	$2Q_B$
4	$1Q_D$	14	$2\overline{CLR}$
5	$1\overline{CLR}$	15	$2Q_D$
6	nc	16	nc
7	$2Q_C$	17	$1Q_C$
8	nc	18	$1Q_A$
9	$2Q_A$	19	1CLKB
10	GND	20	V_{CC}

nc – no internal connection

6

69

DUAL 4-BIT BINARY COUNTER

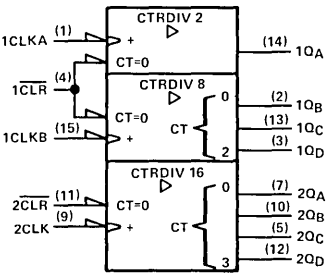
- High-drive outputs (I_{OL} rated at 8 mA/16 mA)

typical performance

COUNT FREQUENCY	CLEAR	POWER DISSIPATION
70 MHz	LOW	180 mW

SN54LS69 (J,FH) SN74LS69 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	1CLKA	9	2CLK
2	$1Q_B$	10	$2Q_B$
3	$1Q_D$	11	$2\overline{CLR}$
4	$1\overline{CLR}$	12	$2Q_D$
5	$2Q_C$	13	$1Q_C$
6	nc	14	$1Q_A$
7	$2Q_A$	15	1CLKB
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1CLKA	12	2CLK
3	$1Q_B$	13	$2Q_B$
4	$1Q_D$	14	$2\overline{CLR}$
5	$1\overline{CLR}$	15	$2Q_D$
6	nc	16	nc
7	$2Q_C$	17	$1Q_C$
8	nc	18	$1Q_A$
9	$2Q_A$	19	1CLKB
10	GND	20	V_{CC}

nc – no internal connection

†Pin numbers shown on logic symbols are for J, JT and NT packages only.
nc – no internal connection.

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70

AND-GATED J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS

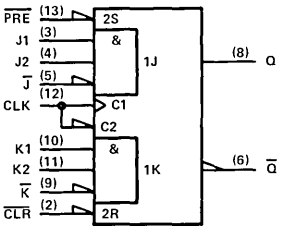
typical performance

TYPE	f_{max}	PWR/FF	SET-UP	HOLD
'70	35 MHz	65 mW	20 ns↑	5 ns↑

↑ Rising edge of clock pulse.
↓ Falling edge of clock pulse.

SN5470 (J,FH) SN7470 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	nc	8	Q
2	CLR	9	K
3	J1	10	K1
4	J2	11	K2
5	J	12	CLK
6	Q̄	13	PRE
7	GND	14	V_{CC}

FH PACKAGE			
1	nc	11	nc
2	nc	12	Q
3	CLR	13	K
4	J1	14	K1
5	nc	15	nc
6	J2	16	K2
7	nc	17	nc
8	J	18	CLK
9	Q̄	19	PRE
10	GND	20	V_{CC}

positive logic: $J = J1 \cdot J2 \cdot \overline{J}$
$K = K1 \cdot K2 \cdot \overline{K}$
If inputs J and K are not used, they must be grounded.
Preset or clear function can occur only when the clock input is low.

71

'H71: AND-OR-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET

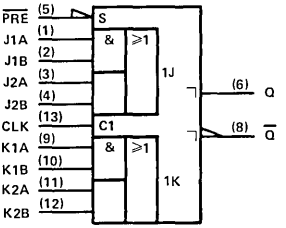
typical performance

TYPE	f_{max}	PWR/FF	SET-UP	HOLD
'H71	30 MHz	80 mW	0 ns↑	0 ns↓
'L71	30 MHz	3.8 mW	0 ns↑	0 ns↓

↑ Rising edge of clock pulse.
↓ Falling edge of clock pulse.

SN54H71 (J) SN74H71 (J,N)

logic symbol, 'H71†



positive logic: $J = (J1A \cdot J1B) + (J2A \cdot J2B)$
$K = (K1A \cdot K1B) + (K2A \cdot K2B)$

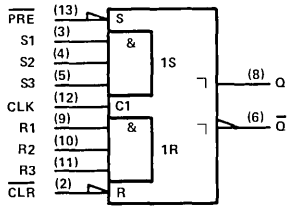
pin assignments, 'H71

J, N PACKAGES			
1	J1A	8	Q̄
2	J1B	9	K1A
3	J2A	10	K1B
4	J2B	11	K2A
5	PRE	12	K2B
6	Q	13	CLK
7	GND	14	V_{CC}

'L71: AND-GATED R-S MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

SN54L71 (J)

logic symbol, 'L71†



positive logic: $R = R1 \cdot R2 \cdot R3$
$S = S1 \cdot S2 \cdot S3$

pin assignments, 'L71

J, N PACKAGES			
1	nc	8	Q
2	CLR	9	R1
3	S1	10	R2
4	S2	11	R3
5	S3	12	CLK
6	Q̄	13	PRE
7	GND	14	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

72

AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

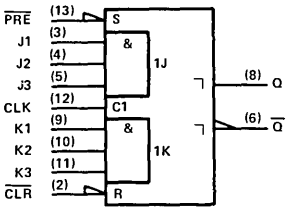
typical performance

TYPE	f_{max}	PWR/ FF	SET-UP	HOLD
'72	20 MHz	50 mW	0 ns↑	0 ns↓
'H72	30 MHz	80 mW	0 ns↑	0 ns↓
'L72	3 MHz	3.8 mW	0 ns↑	0 ns↓

↑ Rising edge of clock pulse.
↓ Falling edge of clock pulse.

SN5472 (J,FH)
SN54H72 (J)
SN54L72 (J)
SN7472 (J)
SN74H72 (J)

logic symbol†



positive logic: $J = J1 \cdot J2 \cdot J3$; $K1 \cdot K2 \cdot K3$

pin assignments

J, N PACKAGES			
1	nc	8	Q
2	$\overline{CLR}$	9	K1
3	J1	10	K2
4	J2	11	K3
5	J3	12	CLK
6	$\overline{Q}$	13	$\overline{PRE}$
7	GND	14	V_{CC}

FH PACKAGE			
1	nc	11	nc
2	nc	12	Q
3	$\overline{CLR}$	13	K1
4	J1	14	K2
5	nc	15	nc
6	J2	16	K3
7	nc	17	nc
8	J3	18	CLK
9	$\overline{Q}$	19	$\overline{PRE}$
10	GND	20	V_{CC}

73

DUAL J-K FLIP-FLOPS WITH CLEAR

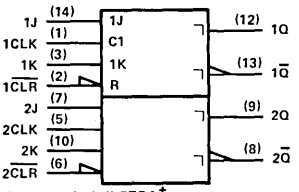
typical performance

TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'73	20 MHz	5 mW	0 ns↑	0 ns↓
'H73	30 MHz	80 mW	0 ns↑	0 ns↓
'L73	3 MHz	3.8 mW	0 ns↑	0 ns↓
'LS73A	45 MHz	10 mW	20 ns↓	0 ns↓

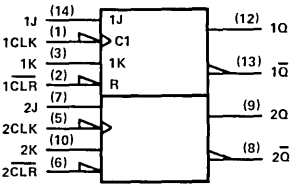
↑ Rising edge of clock pulse.
↓ Falling edge of clock pulse.

SN5473 (J)
SN54H73 (J)
SN54L73 (J)
SN54LS73A (J
SN7473 (J,N)
SN74H73 (J,N)
SN74LS73A (J,N)

logic symbol' '73, 'H73, 'L73†



logic symbol, 'LS73A†



pin assignments

J, N PACKAGES			
1	1CLK	8	2Q̄
2	1$\overline{CLR}$	9	2Q
3	1K	10	2K
4	V_{CC}	11	GND
5	2CLK	12	1Q
6	2$\overline{CLR}$	13	1Q̄
7	2J	14	1J

For chip carrier information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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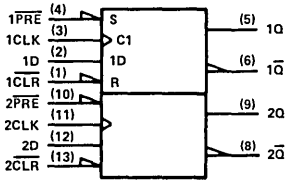
74

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1CLR	8	2Q̄	1	nc	11	nc
2	1D	9	2Q	2	1CLR	12	2Q̄
3	1CLK	10	2PRE	3	1D	13	2Q
4	1PRE	11	2CLK	4	1CLK	14	2PRE
5	1Q	12	2D	5	nc	15	nc
6	1Q̄	13	2CLR	6	1PRE	16	2CLK
7	GND	14	V_{CC}	7	nc	17	nc
				8	1Q	18	2D
				9	1Q̄	19	2CLR
				10	GND	20	V_{CC}

typical performance

TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'74	25 MHz	43 mW	20 ns†	5 ns†
'ALS74	50 MHz	6 mW	15 ns†	0 ns†
'AS74	125 MHz	26 mW		
'H74	43 MHz	75 mW	15 ns†	5 ns†
'L74	3 MHz	4 mW	50 ns†	15 ns†
'LS74A	33 MHz	10 mW	20 ns†	5 ns†
'S74	110 MHz	75 mW	3 ns†	2 ns†

† Rising edge of clock pulse.

SN5474 (J,FH)	SN7474 (J,N)
SN54ALS74 (J,FH)	SN74ALS74 (N,FN)
SN54AS74 (J,FH)	SN74AS74 (N,FN)
SN54H74 (J)	SN74H74 (J,N)
SN54L74 (J)	
SN54LS74A (J,FH)	SN74LS74A (J,N,FN)
SN54S74 (J,FH)	SN74S74 (J,N,FN)

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

75

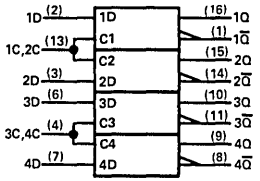
4-BIT BISTABLE LATCHES

typical performance

TYPE	OUTPUTS	DELAY	TOTAL POWER
'75	Q,$\overline{Q}$	15 ns	160 mW
'L75	Q,$\overline{Q}$	30 ns	80 mW
'LS75	Q,$\overline{Q}$	11 ns	32 mW

SN5475 (J) SN7475 (J,N)
SN54L75 (J)
SN54LS75 (J) SN74LS75 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	1Q̄	9	4Q
2	1D	10	3Q
3	2D	11	3Q̄
4	3C,4C	12	GND
5	V_{CC}	13	1C,2C
6	3D	14	2Q̄
7	4D	15	2Q
8	4Q̄	16	1Q

For chip carrier information, contact the factory.

76

DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR

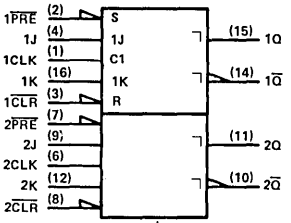
typical performance

TYPE	f_{max}	PWR/F-F	SET-UP	HOLD
'76	20 MHz	50 mW	0 ns↑	0 ns↓
'H76	30 MHz	80 mW	0 ns↑	0 ns↓
'LS76A	45 MHz	10 mW	20 ns↓	0 ns↓

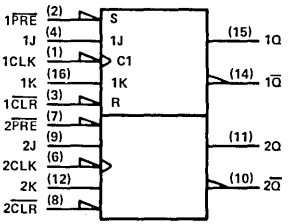
↑ Rising edge of clock pulse.
↓ Falling edge of clock pulse.

SN5476 (J) SN7476 (J,N)
SN54H76 (J) SN74H76 (J,N)
SN54LS76A (J) SN74LS76A (J,N)

logic symbol, '76, 'H76†



logic symbol, 'LS76A†



pin assignments

J, N PACKAGES			
1	1CLK	9	2J
2	1PRE	10	2Q̄
3	1CLR	11	2Q
4	1J	12	2K
5	V_{CC}	13	GND
6	2CLK	14	1Q̄
7	2PRE	15	1Q
8	2CLR	16	1K

For chip carrier information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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77

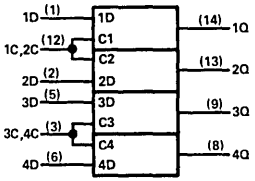
4-BIT BISTABLE LATCHES

typical performance

TYPE	OUTPUTS	DELAY	TOTAL POWER
'77	Q	15 ns	160 mW
'L77	Q	30 ns	80 mW
'LS77	Q	10 ns	35 mW

SN5477 (J)
SN54L77 (J)
SN54LS77 (J) SN74LS77 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	1D	8	4Q
2	2D	9	3Q
3	3C,4C	10	nc
4	V_{CC}	11	GND
5	3D	12	1C,2C
6	4D	13	2Q
7	nc	14	1Q

For chip carrier information, contact the factory.

78

DUAL J-K FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

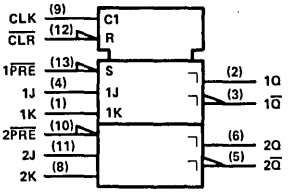
typical performance

TYPE	f_{max}	PWR/F-F	SET-UP	HOLD
'H78	30 MHz	80 mW	0 ns↑	0 ns↓
'L78	3 MHz	3.8 mW	0 ns↑	0 ns↓
'LS78A	45 MHz	10 mW	20 ns↓	0 ns↓

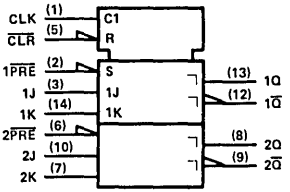
↑ Rising edge of clock pulse.
↓ Falling edge of clock pulse.

SN54H78 (J) SN74H78 (J,N)
SN54L78 (J)
SN54LS78A (J) SN74LS78A (J,N)

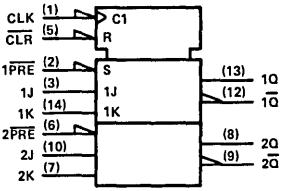
logic symbol, 'H78†



logic symbol, 'L78†



logic symbol, 'LS78A†



pin assignments, 'H78

J, N PACKAGES			
1	1K	8	2K
2	1Q	9	CLK
3	1Q̄	10	2PRE
4	1J	11	2J
5	2Q̄	12	CLR
6	2Q	13	1PRE
7	GND	14	V_{CC}

pin assignments, 'L78, 'LS78A

J, N PACKAGES			
1	CLK	8	2Q
2	1PRE	9	2Q̄
3	1J	10	2J
4	V_{CC}	11	GND
5	CLR	12	1Q̄
6	2PRE	13	1Q
7	2K	14	1K

For chip carrier information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

80

GATED FULL ADDERS

typical performance

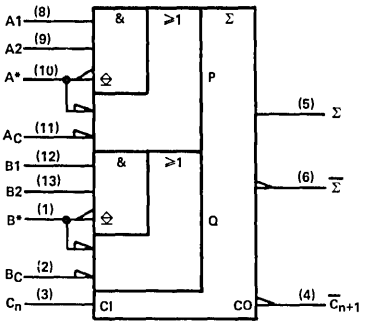
TYPE	CARRY TIME	ADD TIME	POWER PER BIT
'80	10.5 ns	52 ns	105 mW

SN5480 (J,FH) SN7480 (J,N)

NOTES: 1. $A = \overline{A_C} + \overline{A^*} + A1 \cdot A2$, $B = \overline{B_C} + \overline{B^*} + B1 \cdot B2$

2. When A* is used as an input, A1 or A2 must be low. When B* is used as an input, B1 or B2 must be low.
3. When A1 and A2 or B1 and B2 are used as inputs, A* or B*, respectively, must be open or used to perform dot-AND logic.

logic symbol†



pin assignments

J, N PACKAGES			
1	B*	8	A1
2	B_C	9	A2
3	C_n	10	A*
4	$\overline{C_{n+1}}$	11	A_C
5	Σ	12	B1
6	$\overline{\Sigma}$	13	B2
7	GND	14	V_{CC}

FH PACKAGE			
1	nc	11	nc
2	B*	12	A1
3	B_C	13	A2
4	C_n	14	A*
5	nc	15	nc
6	$\overline{C_{n+1}}$	16	A_C
7	nc	17	nc
8	Σ	18	B1
9	$\overline{\Sigma}$	19	B2
10	GND	20	V_{CC}

81

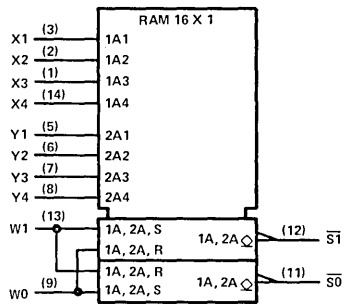
16-BIT RANDOM-ACCESS MEMORIES

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER PER BIT
'81A	15 ns	15 ns	14 mW

SN5481A (J) SN7481A (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	X3	8	Y4
2	X2	9	W0
3	X1	10	GND
4	V_{CC}	11	$\overline{S0}$
5	Y1	12	$\overline{S1}$
6	Y2	13	W1
7	Y3	14	X4

82

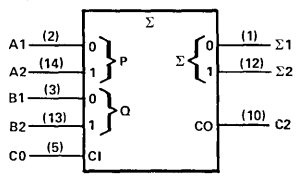
2-BIT BINARY FULL ADDERS

typical performance

TYPE	CARRY TIME	ADD TIME	POWER PER BIT
'82	14.5 ns	25 ns	87 mW

SN5482 (J) SN7482 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	Σ1	8	nc
2	A1	9	nc
3	B1	10	C2
4	V_{CC}	11	GND
5	C0	12	Σ2
6	nc	13	B2
7	nc	14	A2

For chip carrier information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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83

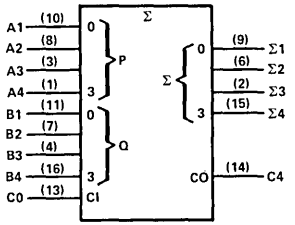
4-BIT BINARY FULL ADDERS WITH FAST CARRY

typical performance

TYPE	CARRY TIME	ADD TIME	POWER PER BIT
'83A	10 ns	16 ns	76 mW
'LS83A	10 ns	15 ns	24 mW

SN5483A (J) SN7483A (J,N)
SN54LS83A (J) SN74LS83A (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	A4	9	Σ1
2	ISI3	10	A1
3	A3	11	B1
4	B3	12	GND
5	V_{CC}	13	C0
6	Σ2	14	C4
7	B2	15	Σ4
8	A2	16	B4

For new chip carrier designs, use 'LS283 or 'S283.

84

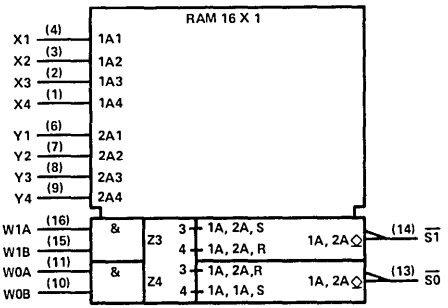
16-BIT RANDOM-ACCESS MEMORIES

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER PER BIT
'84A	15 ns	15 ns	14 mW

SN5484A (J) SN7484A (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	X4	9	Y4
2	X3	10	W0B
3	X2	11	W0A
4	X1	12	GND
5	V_{CC}	13	$\overline{S0}$
6	Y1	14	$\overline{S1}$
7	Y2	15	W1B
8	Y3	16	W1A

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

85

4-BIT MAGNITUDE COMPARATORS

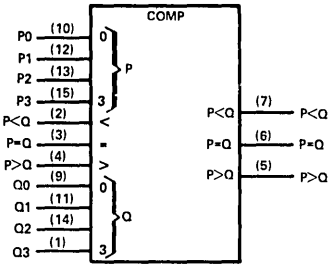
typical performance

TYPE	COMPARE TIME	POWER
'85	21 ns	275 mW
'L85	82 ns	20 mW
'LS85	23.5 ns	52 mW
'S85	11.5 ns	365 mW

SN5485 (J,FH)
SN54L85 (J)
SN54LS85 (J,FH)
SN54S85 (J,FH)

SN7485 (J,N)
SN74LS85 (J,N,FN)
SN74S85 (J,N,FN)

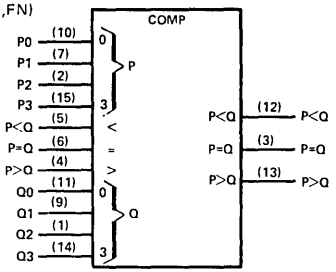
logic symbol, '85, 'LS85, 'S85†



pin assignments, '85, 'LS85, 'S85

J, N PACKAGES				FH, FN PACKAGES			
1	Q3	9	Q0	1	nc	11	nc
2	P<Qin	10	P0	2	Q3	12	Q0
3	P=Qin	11	Q1	3	P<Qin	13	P0
4	P>Qin	12	P1	4	P=Qin	14	Q1
5	P>Qout	13	P2	5	P>Qin	15	P1
6	P=Qout	14	Q2	6	nc	16	nc
7	P<Qout	15	P3	7	P>Qout	17	P2
8	GND	16	V_{CC}	8	P=Qout	18	Q2
				9	P<Qout	19	P3
				10	GND	20	V_{CC}

logic symbol, 'L85†



pin assignments, 'L85

J, N PACKAGES			
1	Q2	9	Q1
2	P2	10	P0
3	P=Qout	11	Q0
4	P>Qin	12	P<Qout
5	P<Qin	13	P>Qout
6	P=Qin	14	Q3
7	P1	15	P3
8	GND	16	V_{CC}

86

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

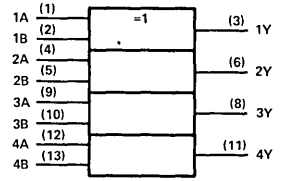
typical performance

TYPE	POWER	DELAY
'86	150 mW	14 ns
'ALS86		
'L86	15 mW	55 ns
'LS86	30 mW	10 ns
'S86	250 mW	7 ns

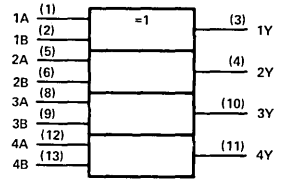
SN5486 (J,FH)
SN54ALS86 (J,FH)
SN54L86 (J)
SN54LS86 (J,FH)
SN54S86 (J,FH)

SN7486 (J,N)
SN74ALS86 (N,FN)
SN74LS86 (J,N,FN)
SN74S86 (J,N,FN)

logic symbol, '86, 'ALS86, 'LS86, 'S86†



logic symbol, 'L86†



positive logic: $Y = A \oplus B = \overline{A}B + A\overline{B}$

pin assignments, '86, 'ALS86, 'LS86, 'S86

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3Y	1	nc	11	nc
2	1B	9	3A	2	1A	12	3Y
3	1Y	10	3B	3	1B	13	3A
4	2A	11	4Y	4	1Y	14	3B
5	2B	12	4A	5	nc	15	nc
6	2Y	13	4B	6	2A	16	4Y
7	GND	14	V_{CC}	7	nc	17	nc
				8	2B	18	4A
				9	2Y	19	4B
				10	GND	20	V_{CC}

pin assignments, 'L86

J, N PACKAGES			
1	1A	8	3A
2	1B	9	3B
3	1Y	10	3Y
4	2Y	11	4Y
5	2A	12	4A
6	2B	13	4B
7	GND	14	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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87

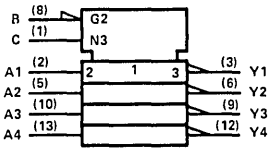
4-BIT TRUE/ COMPLEMENT, ZERO/ONE ELEMENTS

typical performance

TYPE	POWER	DELAY
'H87	270 mW	14 ns

SN54H87 (J) SN74H87 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	C	8	B
2	A1	9	Y3
3	Y1	10	A3
4	nc	11	nc
5	A2	12	Y4
6	Y2	13	A4
7	GND	14	V_{CC}

88

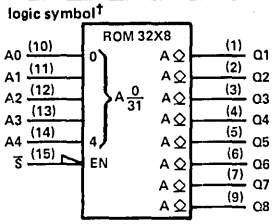
256-BIT READ-ONLY MEMORIES

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER PER BIT
'88A	26 ns	22 ns	1.1 mW

SN5488A (J) SN7488A (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	Q1	9	Q8
2	Q2	10	A0
3	Q3	11	A1
4	Q4	12	A2
5	Q5	13	A3
6	Q6	14	A4
7	Q7	15	$\overline{S}$
8	GND	16	V_{CC}

For chip carrier information, contact the factory.

89

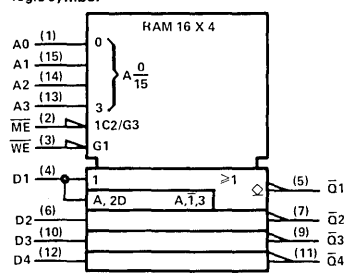
64-BIT READ/WRITE MEMORIES

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER PER BIT
'89	32 ns	30 ns	5.9 mW

SN7489 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	A0	9	$\overline{Q}3$
2	$\overline{ME}$	10	D3
3	$\overline{WE}$	11	$\overline{Q}4$
4	D1	12	D4
5	$\overline{Q}1$	13	A3
6	D2	14	A2
7	$\overline{Q}2$	15	A1
8	GND	16	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

90

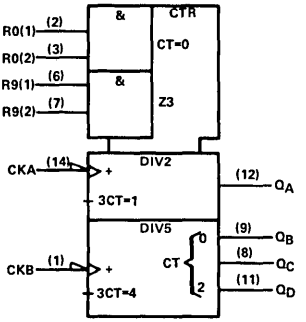
DECADE COUNTERS

typical performance

TYPE	COUNT FREQUENCY	CLEAR	TOTAL POWER
'90A	32 MHz	HIGH	160 mW
'L90	3 MHz	HIGH	20 mW
'LS90	32 MHz	HIGH	40 mW

SN5490A (J) SN7490A (J,N)
SN54L90 (J)
SN54LS90 (J) SN74LS90 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	CKB	8	Q_C
2	R0(1)	9	Q_B
3	R0(2)	10	GND
4	nc	11	Q_D
5	V_{CC}	12	Q_A
6	R9(1)	13	nc
7	R9(2)	14	CKA

For new chip carrier designs, use '290 or 'LS290.

91

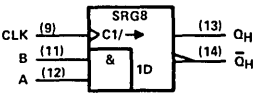
8-BIT SHIFT REGISTERS

typical performance

TYPE	SHIFT FREQUENCY	SERIAL DATA INPUT	TOTAL POWER
'91A	10 MHz	GATED D	175 mW
'L91	3 MHz	GATED D	17.5 mW
'LS91	25 MHz	GATED D	60 mW

SN5491A (J) SN7491A (J,N)
SN54L91 (J)
SN54LS91 (J) SN74LS91 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	nc	8	nc
2	nc	9	CLK
3	nc	10	GND
4	nc	11	B
5	V_{CC}	12	A
6	nc	13	QH
7	nc	14	$\overline{Q}_H$

For chip carrier information, contact the factory.

92

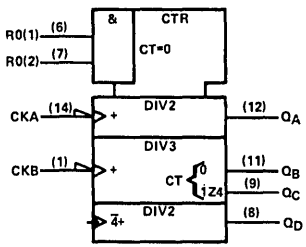
DIVIDE-BY-12 COUNTERS

typical performance

TYPE	COUNT FREQUENCY	CLEAR	TOTAL POWER
'92A	32 MHz	HIGH	160 mW
'LS92	32 MHz	HIGH	39 mW

SN5492A (J) SN7492A (J,N)
SN54LS92 (J) SN74LS92 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	CKB	8	Q_D
2	nc	9	Q_C
3	nc	10	GND
4	nc	11	Q_B
5	V_{CC}	12	Q_A
6	R0(1)	13	nc
7	R0(2)	14	CKA

For new chip carrier designs, use 'LS292.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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93

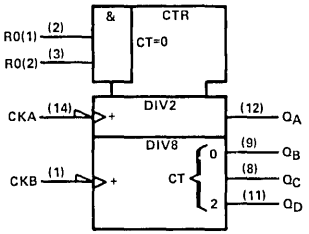
4-BIT BINARY COUNTERS

typical performance

TYPE	COUNT FREQUENCY	CLEAR	TOTAL POWER
'93A	32 MHz	HIGH	160 mW
'L93	3 MHz	HIGH	20 mW
'LS93	32 MHz	HIGH	39 mW

SN5493A (J) SN7493A (J,N)
SN54L93 (J)
SN54LS93 (J) SN74LS93 (J,N)

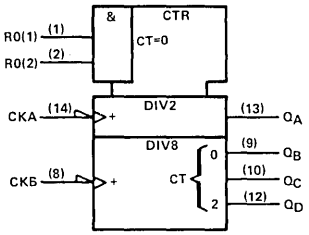
logic symbol, '93A, 'LS93†



pin assignments, '93A, 'LS93

J, N PACKAGES			
1	CKB	8	Q_C
2	R0(1)	9	Q_B
3	R0(2)	10	GND
4	nc	11	Q_D
5	V_{CC}	12	Q_A
6	nc	13	nc
7	nc	14	CKA

logic symbol, 'L93†



pin assignments, 'L93

J, N PACKAGES			
1	R0(1)	8	CKB
2	R0(2)	9	Q_B
3	nc	10	Q_C
4	V_{CC}	11	GND
5	nc	12	Q_D
6	nc	13	Q_A
7	nc	14	CKA

For new chip carrier designs, use '293 or 'LS293.

94

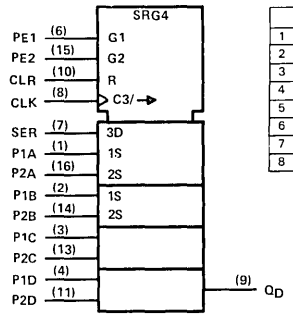
4-BIT SHIFT REGISTERS (DUAL ASYNCHRONOUS PRESETS)

typical performance

TYPE	SHIFT FREQUENCY	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'94	10 MHz	D	HIGH	175 mW

SN5494 (J) SN7494 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	P1A	9	Q_D
2	P1B	10	CLR
3	P1C	11	P2D
4	P1D	12	GND
5	V_{CC}	13	P2C
6	PE1	14	P2B
7	SER	15	PE2
8	CLK	16	P2A

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

95

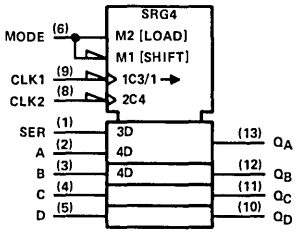
4-BIT SHIFT REGISTERS (PARALLEL IN/PARALLEL OUT, SHIFT RIGHT, SHIFT LEFT, SERIAL INPUT)

typical performance

TYPE	SHIFT FREQUENCY	SERIAL DATA INPUT	TOTAL POWER
'95A	25 MHz	D	195 mW
'L95	3 MHz	D	19 mW
'LS95B	30 MHz	D	65 mW

SN5495 A (J,FH) SN7495A (J,N)
SN54L95 (J)
SN54LS95B (J,FH) SN74LS95B (J,N,FN)

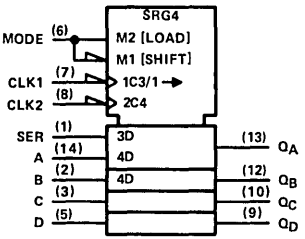
logic symbol, '95A, 'LS95B†



pin assignments, '95A, 'LS95B

J, N PACKAGES				FH, FN PACKAGES			
1	SER	8	CLK2	1	nc	11	nc
2	A	9	CLK1	2	SER	12	CLK2
3	B	10	Q_D	3	A	13	CLK1
4	C	11	Q_C	4	B	14	Q_D
5	D	12	Q_B	5	nc	15	nc
6	MODE	13	Q_A	6	C	16	Q_C
7	GND	14	V_{CC}	7	nc	17	nc
				8	D	18	Q_B
				9	MODE	19	Q_A
				10	GND	20	V_{CC}

logic symbol, 'L95†



pin assignments, 'L95

J, N PACKAGES			
1	SER	8	CLK2
2	B	9	Q_D
3	C	10	Q_C
4	V_{CC}	11	GND
5	D	12	Q_B
6	MODE	13	Q_A
7	CLK1	14	A

96

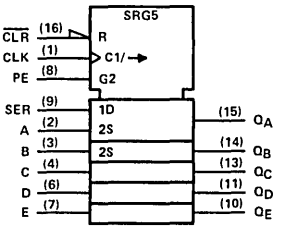
5-BIT SHIFT REGISTERS

typical performance

TYPE	SHIFT FREQUENCY	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'96	10 MHz	D	LOW	240 mW
'L96	5 MHz	D	LOW	120 mW
'LS96	10 MHz	D	LOW	60 mW

SN5496 (J) SN7496 (J,N)
SN54L96 (J)
SN54LS96 (J) SN74LS96 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	CLK	9	SER
2	A	10	Q_E
3	B	11	Q_D
4	C	12	GND
5	V_{CC}	13	Q_C
6	D	14	Q_B
7	E	15	Q_A
8	PE	16	$\overline{CLR}$

For chip carrier information, contact the factory.

97

SYNCHRONOUS 6-BIT BINARY RATE MULTIPLIERS

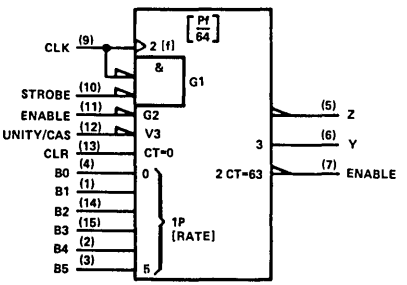
typical performance

TYPE	POWER	FREQ‡
'97	345 mW	32 MHz

‡ Maximum clock frequency

SN5497 (J,FH)
SN7497 (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	B1	9	CLK	1	nc	11	nc
2	B4	10	STRB	2	B1	12	CLK
3	B5	11	ENin	3	B4	13	STRB
4	B0	12	UNITY/CAS	4	B5	14	ENin
5	Z	13	CLR	5	B0	15	UNITY/CAS
6	Y	14	B2	6	nc	16	nc
7	ENout	15	B3	7	Z	17	CLR
8	GND	16	V_{CC}	8	Y	18	B2
				9	ENout	19	B3
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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98

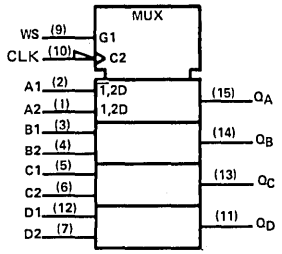
4-BIT DATA SELECTOR/ STORAGE REGISTERS

typical performance

TYPE	FREQUENCY	POWER
'L98	3 MHz	25 mW

SN54L98 (J)

logic symbol†



pin assignments

J, N PACKAGES			
1	A2	9	WS
2	A1	10	CLK
3	B1	11	Q_D
4	B2	12	D1
5	C1	13	Q_C
6	C2	14	Q_B
7	D2	15	Q_A
8	GND	16	V_{CC}

99

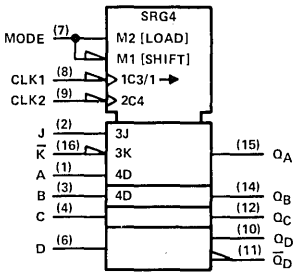
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

typical performance

TYPE	SHIFT FREQUENCY	SERIAL DATA INPUT	TOTAL POWER
'L99	3 MHz	$J\text{-}\overline{K}$	19 mW

SN54L99 (J)

logic symbol†



pin assignments

J, N PACKAGES			
1	A	9	CLK2
2	J	10	Q_D
3	B	11	$\overline{Q}_D$
4	C	12	Q_C
5	V_{CC}	13	GND
6	D	14	Q_B
7	MODE	15	Q_A
8	CLK1	16	$\overline{K}$

100

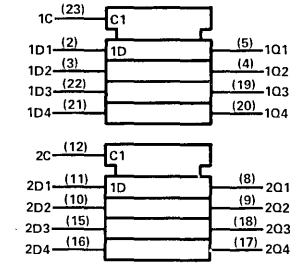
8-BIT BISTABLE LATCHES

typical performance

TYPE	DELAY	TOTAL POWER
'100	15 ns	320 mW

SN54100 (J) SN74100 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	nc	13	nc
2	1D1	14	nc
3	1D2	15	2D3
4	1Q2	16	2D4
5	1Q1	17	2Q4
6	nc	18	2Q3
7	GND	19	1Q3
8	2Q1	20	1Q4
9	2Q2	21	1D4
10	2D2	22	1D3
11	2D1	23	1C
12	2C	24	V_{CC}

For chip carrier information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

101

AND-OR-GATED J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

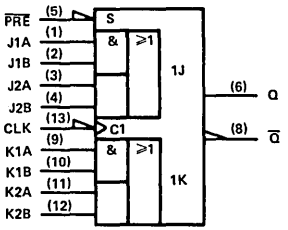
typical performance

TYPE	f_{max}	PWR	SET-UP	HOLD
'H101	50 MHz	100 mW	13 ns↓	0 ns↓

↓ Falling edge of clock pulse

SN54H101 (J) SN74H101 (J,N)

logic symbol†



positive logic: $J = (J1A \cdot J1B) + (J2A \cdot J2B)$

$K = (K1A \cdot K1B) + (K2A \cdot K2B)$

pin assignments

J, N PACKAGES			
1	J1A	8	Q̄
2	J1B	9	K1A
3	J2A	10	K1B
4	J2B	11	K2A
5	PRE	12	K2B
6	Q	13	CLK
7	GND	14	V_{CC}

102

AND-GATED J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

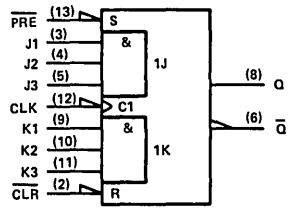
typical performance

TYPE	f_{max}	PWR	SET-UP	HOLD
'H102	50 MHz	100 mW	13 ns↓	0 ns↓

↓ Falling edge of clock pulse

SN54H102 (J) SN74H102 (J,N)

logic symbol†



positive logic: $J = J1 \cdot J2 \cdot J3$

$K = K1 \cdot K2 \cdot K3$

pin assignments

J, N PACKAGES			
1	nc	8	Q
2	CLR	9	K1
3	J1	10	K2
4	J2	11	K3
5	J3	12	CLK
6	Q̄	13	PRE
7	GND	14	V_{CC}

103

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR

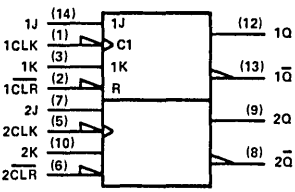
typical performance

TYPE	f_{max}	PWR/F-F	SET-UP	HOLD
'H103	50 MHz	100 mW	13 ns↓	0 ns↓

↓ Falling edge of clock pulse

SN54H103 (J) SN74H103 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	1CLK	8	2Q̄
2	1CLR	9	2Q
3	1K	10	2K
4	V_{CC}	11	GND
5	2CLK	12	1Q
6	2CLR	13	1Q̄
7	2J	14	1J

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

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106

DUAL J-K NEGATIVE-EDGE TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

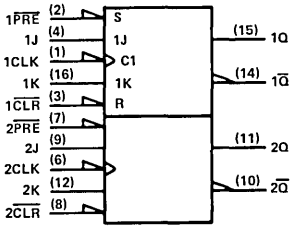
typical performance

TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'H106	50 MHz	100 mW	13 ns↓	0 ns↓

↓ Falling edge of clock pulse

SN54H106 (J) SN74H106 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	1CLK	9	2J
2	1PRE	10	2Q̄
3	1CLR	11	2Q
4	1J	12	2K
5	V_{CC}	13	GND
6	2CLK	14	1Q̄
7	2PRE	15	1Q
8	2CLR	16	1K

107

DUAL J-K FLIP-FLOPS WITH CLEAR

typical performance

TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'107	20 MHz	50 mW	0 ns↑	0 ns↓
'LS107A	45 MHz	10 mW	20 ns↓	0 ns↓

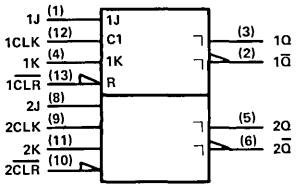
↑ Rising edge of clock pulse

↓ Falling edge of clock pulse

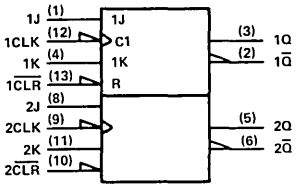
SN54107 (J,FH) SN74107 (J,N)

SN54LS107A (J,FH) SN74LS107A (J,N,FN)

logic symbol, '107†



logic symbol, 'LS107A†



pin assignments

J, N PACKAGES			
1	1J	8	2J
2	1Q̄	9	2CLK
3	1Q	10	2CLR
4	1K	11	2K
5	2Q	12	1CLK
6	2Q̄	13	1CLR
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1J	12	2J
3	1Q̄	13	2CLK
4	1Q	14	2CLR
5	nc	15	nc
6	1K	16	2K
7	nc	17	nc
8	2Q	18	1CLK
9	2Q̄	19	1CLR
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

108

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

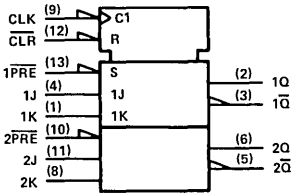
typical performance

TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'H108	50 MHz	100 mW	13 ns↓	0 ns↓

↓ Falling edge of clock pulse

SN54H108 (J) SN74H108 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	1K	8	2K
2	1Q	9	CLK
3	1Q̄	10	2PRE
4	1J	11	2J
5	2Q̄	12	CLR
6	2Q	13	1PRE
7	GND	14	V_{CC}

109

DUAL J-K̄ POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

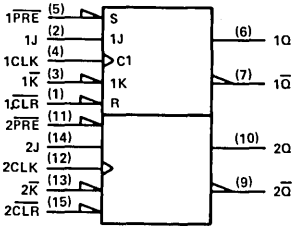
typical performance

TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'109	33 MHz	45 mW	10 ns†	6 ns†
'ALS109	50 MHz	6 mW	15 ns†	0 ns†
'AS109	125 MHz	29 mW		
'LS109A	33 MHz	10 mW	20 ns†	5 ns†

† Rising edge of clock pulse

SN54109 (J,FH) SN74109 (J,N)
SN54ALS109 (J,FH) SN74ALS109 (N,FN)
SN54AS109 (J,FH) SN74AS109 (N,FN)
SN54LS109A (J,FH) SN74LS109A (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	1CLR	9	2Q̄
2	1J	10	2Q
3	1K	11	2PRE
4	1CLK	12	2CLK
5	1PRE	13	2K
6	1Q	14	2J
7	1Q̄	15	2CLR
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1CLR	12	2Q̄
3	1J	13	2Q
4	1K	14	2PRE
5	1CLK	15	2CLK
6	nc	16	nc
7	1PRE	17	2K
8	1Q	18	2J
9	1Q̄	19	2CLR
10	GND	20	V_{CC}

110

AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH DATA LOCKOUT

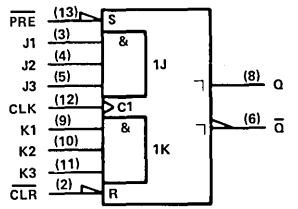
typical performance

TYPE	f_{max}	PWR	SET-UP	HOLD
'110	25 MHz	100 mW	20 ns†	5 ns†

† Rising edge of clock pulse

SN54110 (J) SN74110 (J,N)

logic symbol†



positive logic: $J = J1 \cdot J2 \cdot J3$
$K = K1 \cdot K2 \cdot K3$

pin assignments

J, N PACKAGES			
1	nc	8	Q
2	CLR	9	K1
3	J1	10	K2
4	J2	11	K3
5	J3	12	CLK
6	Q̄	13	PRE
7	GND	14	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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111

DUAL J-K MASTER-SLAVE FLIP-FLOPS WITH DATA LOCKOUT

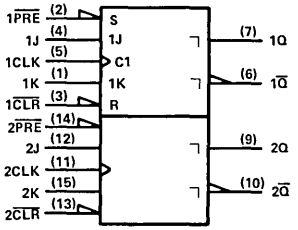
typical performance

TYPE	f_{max}	PWR/ FF	SET-UP	HOLD
'111	25 MHz	70 mW	0 ns↑	30 ns↑

↑ Rising edge of clock pulse

SN54111 (J) SN74111 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	1K	9	2Q
2	1PRE	10	2Q̄
3	1CLR	11	2CLK
4	1J	12	2J
5	1CLK	13	2CLR
6	1Q̄	14	2PRE
7	1Q	15	2K
8	GND	16	V_{CC}

112

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

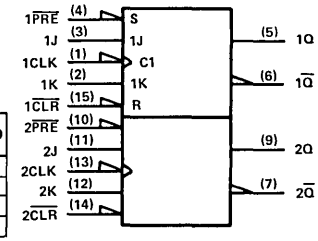
typical performance

TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'ALS112A	40 MHz	6 mW	25 ns↓	0 ns↓
'AS112	200 MHz	95 mW		
'LS112A	45 MHz	10 mW	20 ns↓	0 ns↓
'S112	125 MHz	75 mW	3 ns↓	0 ns↓

↓ Falling edge of clock pulse

SN54ALS112A (J,FH) SN74ALS112A (N,FN)
SN54AS112 (J,FH) SN74AS112 (N,FN)
SN54LS112A (J,FH) SN74LS112A (J,N,FN)
SN54S112 (J,FH) SN74S112 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	1CLK	9	2Q
2	1K	10	2PRE
3	1J	11	2J
4	1PRE	12	2K
5	1Q	13	2CLK
6	1Q̄	14	2CLR
7	2Q̄	15	1CLR
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1CLK	12	2Q
3	1K	13	2PRE
4	1J	14	2J
5	1PRE	15	2K
6	nc	16	nc
7	1Q	17	2CLK
8	1Q̄	18	2CLR
9	2Q̄	19	1CLR
10	GND	20	V_{CC}

113

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

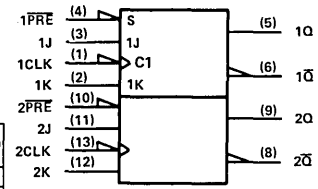
typical performance

TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'ALS113A	40 MHz	6 mW	25 ns↓	0 ns↓
'AS113	200 MHz	95 mW		
'LS113A	45 MHz	10 mW	20 ns↓	0 ns↓
'S113	125 MHz	75 mW	3 ns↓	0 ns↓

↓ Falling edge of clock pulse

SN54ALS113A (J,FH) SN74ALS113A (N,FN)
SN54AS113 (J,FH) SN74AS113 (N,FN)
SN54LS113A (J,FH) SN74LS113A (J,N,FN)
SN54S113 (J,FH) SN74S113 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	1CLK	8	2Q̄
2	1K	9	2Q
3	1J	10	2PRE
4	1PRE	11	2J
5	1Q	12	2K
6	1Q̄	13	2CLK
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1CLK	12	2Q̄
3	1K	13	2Q
4	1J	14	2PRE
5	nc	15	nc
6	1PRE	16	2J
7	nc	17	nc
8	1Q	18	2K
9	1Q̄	19	2CLK
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

114

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

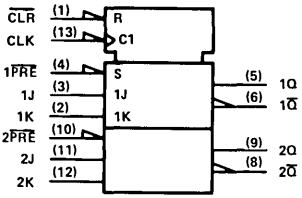
typical performance

TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'ALS114A	40 MHz	6 mW	25 ns↓	0 ns↓
'AS114	200 MHz	95 mW		
'LS114A	45 MHz	10 mW	20 ns↓	0 ns↓
'S114	125 MHz	75 mW	3 ns↓	0 ns↓

↓ Falling edge of clock pulse

SN54ALS114A (J,FH) SN74ALS114A (N,FN)
SN54AS114 (J,FH) SN74AS114 (N,FN)
SN54LS114A (J,FH) SN74LS114A (J,N,FN)
SN54S114 (J,FH) SN74S114 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1CLR	8	2Q̄	1	nc	11	nc
2	1K	9	2Q	2	1CLR	12	2Q̄
3	1J	10	2PRE	3	1K	13	2Q
4	1PRE	11	2J	4	1J	14	2PRE
5	1Q	12	2K	5	nc	15	nc
6	1Q̄	13	CLK	6	1PRE	16	2J
7	GND	14	V_{CC}	7	nc	17	nc
				8	1Q	18	2K
				9	1Q̄	19	CLK
				10	GND	20	V_{CC}

116

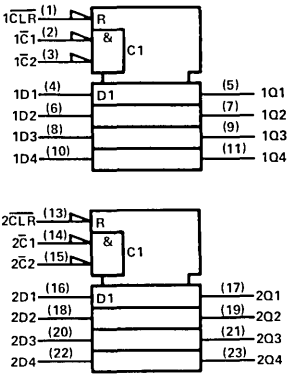
DUAL 4-BIT LATCHES

typical performance

TYPE	BITS	CLEAR	DELAY	TOTAL POWER
'116	8	LOW	11 ns	250 mW

SN54116 (J,FH) SN74116 (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	1CLR	13	2CLR	1	nc	15	nc
2	1C1	14	2C1	2	1CLR	16	2CLR
3	1C2	15	2C2	3	1C1	17	2C1
4	1D1	16	2D1	4	1C2	18	2C2
5	1Q1	17	2Q1	5	1D1	19	2D1
6	1D2	18	2D2	6	1Q1	20	2Q1
7	1Q2	19	2Q2	7	1D2	21	2D2
8	1D3	20	2D3	8	nc	22	nc
9	1Q3	21	2Q3	9	1Q2	23	2Q2
10	1D4	22	2D4	10	1D3	24	2D3
11	1Q4	23	2Q4	11	1Q3	25	2Q3
12	GND	24	V_{CC}	12	1D4	26	2D4
				13	1Q4	27	2Q4
				14	GND	28	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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120

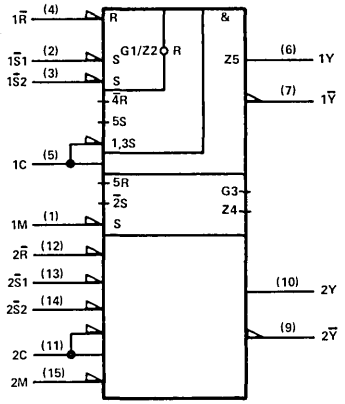
DUAL PULSE SYNCHRONIZERS/DRIVERS

typical performance

TYPE	ENABLE INPUT	COMP OUTPUT	FREQ RANGE	POWER
'120	YES	YES	DC to 30 MHz	255 mW

SN54120 (J,FH) SN74120 (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	1M	9	2Ȳ	1	nc	11	nc
2	1S̄1	10	2Y	2	1M	12	2Ȳ
3	1S̄2	11	2C	3	1S̄1	13	2Y
4	1R	12	2R̄	4	1S̄2	14	2C
5	1C	13	2S̄1	5	1R̄	15	2R̄
6	1Y	14	2S̄2	6	nc	16	nc
7	1Ȳ	15	2M	7	1C	17	2S̄1
8	GND	16	V_{CC}	8	1Ȳ	18	2S̄2
				9	1Y	19	2M
				10	GND	20	V_{CC}

121

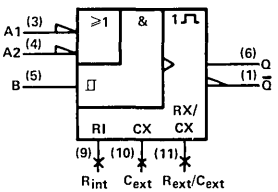
MONOSTABLE MULTIVIBRATORS

typical performance

TYPE	NO. OF INPUTS HI	NO. OF INPUTS LO	OUTPUT PULSE RANGE	TOTAL POWER
'121	1	2	40 ns-28 s	90 mW
'L121	1	2	40 ns-28 s	40 mW

SN54121 (J) SN74121 (J,N)
SN54L121 (J)

logic symbol†



pin assignments

J, N PACKAGES			
1	Q̄	8	nc
2	nc	9	R_{int}
3	A1	10	C_{ext}
4	A2	11	R_{ext}/C_{ext}
5	B	12	nc
6	Q	13	nc
7	GND	14	V_{CC}

'121 . . . R_{int} = 2 kΩ nominal
'L121 . . . R_{int} = 4 kΩ nominal

122

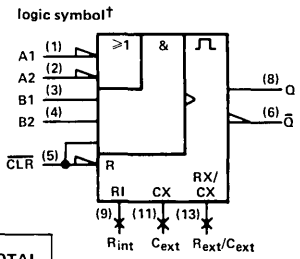
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

typical performance

TYPE	NO. OF INPUTS HI	NO. OF INPUTS LO	DIRECT CLEAR	OUTPUT PULSE RANGE	TOTAL POWER
'122	2	2	YES	45 ns-∞	115 mW
'L122	2	2	YES	90 ns-∞	55 mW
'LS122	2	2	YES	45 ns-∞	30 mW

SN54122 (J,FH) SN74122 (J,N)
SN54L122 (J)
SN54LS122 (J,FH) SN74LS122 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A1	8	Q	1	nc	11	nc
2	A2	9	R_{INT}	2	A1	12	Q
3	B1	10	nc	3	A2	13	R_{int}
4	B2	11	C_{EXT}	4	B1	14	nc
5	CLR	12	nc	5	nc	15	nc
6	Q̄	13	R_{ext}/C_{ext}	6	B2	16	C_{ext}
7	GND	14	V_{CC}	7	nc	17	nc
				8	CLR	18	nc
				9	Q̄	19	R_{ext}/C_{ext}
				10	GND	20	V_{CC}

'122 . . . R_{int} = 10 kΩ nominal
'L122 . . . R_{int} = 20 kΩ nominal
'LS122 . . . R_{int} = 10 kΩ nominal

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

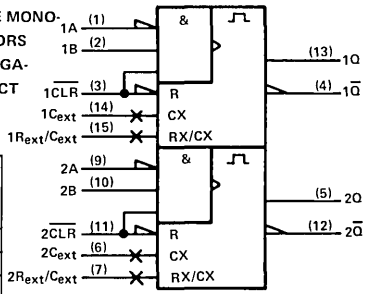
123

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH POSITIVE AND NEGATIVE INPUTS AND DIRECT CLEAR

typical performance

TYPE	OUTPUT PULSE RANGE	TOTAL POWER
'123	45 ns-∞	230 mW
'L123	90 ns-∞	115 mW
'LS123	45 ns-∞	60 mW

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	9	2A	1	nc	11	nc
2	1B	10	2B	2	1A	12	2A
3	1$\overline{CLR}$	11	2$\overline{CLR}$	3	1B	13	2B
4	1Q̄	12	2Q̄	4	1$\overline{CLR}$	14	2$\overline{CLR}$
5	2Q	13	1Q	5	1Q̄	15	2Q̄
6	$2C_{ext}$	14	$1C_{ext}$	6	nc	16	nc
7	$2R_{ext}/C_{ext}$	15	$1R_{ext}/C_{ext}$	7	2Q	17	1Q
8	GND	16	V_{CC}	8	$2C_{ext}$	18	$1C_{ext}$
				9	$2R_{ext}/C_{ext}$	19	$1R_{ext}/C_{ext}$
				10	GND	20	V_{CC}

SN54123 (J,FH) SN74123 (J,N)
SN54L123 (J)
SN54LS123 (J,FH) SN74LS123 (J,N,FN)

124

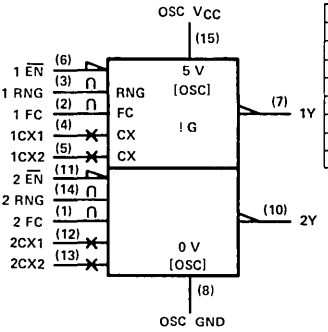
DUAL VOLTAGE-CONTROLLED OSCILLATORS WITH ENABLE INPUTS

typical performance

TYPE	FREQ RANGE	POWER
'S124	1 Hz to 60 MHz	525 mW

SN54S124 (J,FH) SN74S124 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	2FC	9	GND	1	nc	11	nc
2	1FC	10	2Y	2	2FC	12	GND
3	1RNG	11	2$\overline{EN}$	3	1FC	13	2Y
4	1CX1	12	2CX1	4	1RNG	14	2$\overline{EN}$
5	1CX2	13	2CX2	5	1CX1	15	2CX1
6	1$\overline{EN}$	14	2RNG	6	nc	16	nc
7	1Y	15	OSC V_{CC}	7	1CX2	17	2CX2
8	OSC GND	16	V_{CC}	8	1$\overline{EN}$	18	2RNG
				9	1Y	19	OSC V_{CC}
				10	OSC GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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125

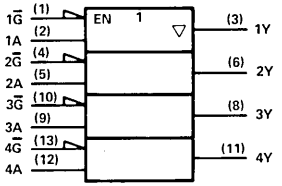
QUADRUPLE BUS BUFFER GATES WITH THREE-STATE OUTPUTS

typical performance

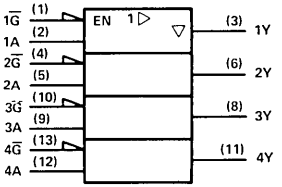
TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54125	10 ns	−2 mA	16 mA
SN74125	10 ns	−5.2 mA	16 mA
SN54LS125A	8 ns	−1 mA	12 mA
SN74LS125A	8 ns	−2.6 mA	24 mA

SN54125 (J,FH) SN74125 (J,N)
SN54LS125A (J,FH) SN74LS125A (J,N,FN)

logic symbol, '125†



logic symbol, 'LS125A†



positive logic: Y = A

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1G̅	8	3Y	1	nc	11	nc
2	1A	9	3A	2	1G̅	12	3Y
3	1Y	10	3G̅	3	1A	13	3A
4	2G̅	11	4Y	4	1Y	14	3G̅
5	2A	12	4A	5	nc	15	nc
6	2Y	13	4G̅	6	2G̅	16	4Y
7	GND	14	V_{CC}	7	nc	17	nc
				8	2A	18	4A
				9	2Y	19	4G̅
				10	GND	20	V_{CC}

126

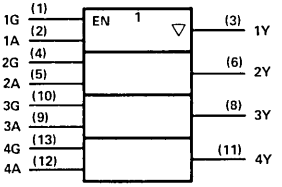
QUADRUPLE BUS BUFFER GATES WITH THREE-STATE OUTPUTS

typical performance

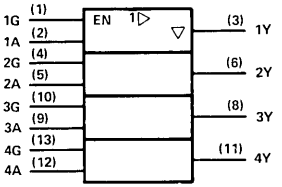
TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54126	10 ns	−2 mA	16 mA
SN74126	10 ns	−5.2 mA	16 mA
SN54LS126A	8.5 ns	−1 mA	12 mA
SN74LS126A	8.5 ns	−2.6 mA	24 mA

SN54126 (J,FH) SN74126 (J,N)
SN54LS126A (J,FH) SN74LS126A (J,N,FN)

logic symbol, '126†



logic symbol, 'LS126A†



positive logic: Y = A

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1G	8	3Y	1	nc	11	nc
2	1A	9	3A	2	1G	12	3Y
3	1Y	10	3G	3	1A	13	3A
4	2G	11	4Y	4	1Y	14	3G
5	2A	12	4A	5	nc	15	nc
6	2Y	13	4G	6	2G	16	4Y
7	GND	14	V_{CC}	7	nc	17	nc
				8	2A	18	4A
				9	2Y	19	4G
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

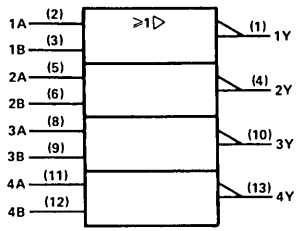
128

LINE DRIVERS
(SN54128 . . . 75 Ω DRIVER
SN74128 . . . 50 Ω DRIVER)
typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	DELAY
SN54128	48 mA	−29 mA	7 ns
SN74128	48 mA	−42.4 mA	7 ns

SN54128 (J,FH) SN74128 (J,N)

logic symbol†



positive logic: $Y = \overline{A + B}$

pin assignments

J, N PACKAGES				FH PACKAGE			
1	1Y	8	3A	1	nc	11	nc
2	1A	9	3B	2	1Y	12	3A
3	1B	10	3Y	3	1A	13	3B
4	2Y	11	4A	4	1B	14	3Y
5	2A	12	4B	5	nc	15	nc
6	2B	13	4Y	6	2Y	16	4A
7	GND	14	V_{CC}	7	nc	17	nc
				8	2A	18	4B
				9	2B	19	4Y
				10	GND	20	V_{CC}

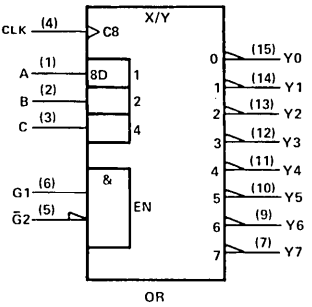
131

3- TO 8-LINE DECODERS/ DEMULTIPLEXERS WITH ADDRESS REGISTERS
(combines decoder and 3-bit address register and incorporates 2 enable inputs to simplify cascading)
typical performance

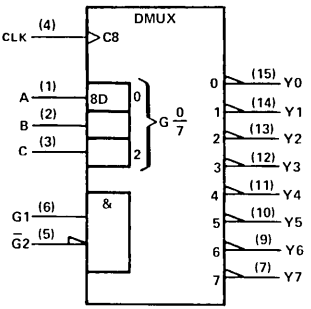
TYPE	CLOCK TO OUTPUT	ENABLE TIME	TOTAL POWER
'ALS131	8.5 ns	10 ns	25 mW

SN54ALS131 (J,FH) SN74ALS131 (N,FN)

logic symbols†



OR



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A	9	Y6	1	nc	11	nc
2	B	10	Y5	2	A	12	Y6
3	C	11	Y4	3	B	13	Y5
4	CLK	12	Y3	4	C	14	Y4
5	$\overline{G2}$	13	Y2	5	CLK	15	Y3
6	G1	14	Y1	6	nc	16	nc
7	Y7	15	YO	7	$\overline{G2}$	17	Y2
8	GND	16	V_{CC}	8	G1	18	Y1
				9	Y7	19	YO
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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132

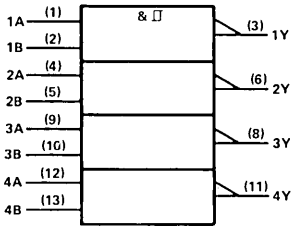
QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

typical performance

TYPE	HYSTERESIS	DELAY
'132	0.8 V	15 ns
'LS132	0.8 V	15 ns
'S132	0.55 V	8 ns

SN54132 (J,FH) SN74132 (J,N)
SN54LS132 (J,FH) SN74LS132 (J,N,FN)
SN54S132 (J,FH) SN74S132 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{AB}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3Y	1	nc	11	nc
2	1B	9	3A	2	1A	12	3Y
3	1Y	10	3B	3	1B	13	3A
4	2A	11	4Y	4	1Y	14	3B
5	2B	12	4A	5	nc	15	nc
6	2Y	13	4B	6	2A	16	4Y
7	GND	14	V_{CC}	7	nc	17	nc
				8	2B	18	4A
				9	2Y	19	4B
				10	GND	20	V_{CC}

133

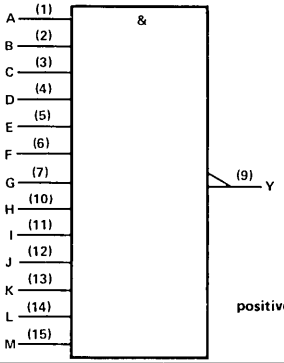
13-INPUT POSITIVE-NAND GATES

typical performance

TYPE	POWER	DELAY
'ALS133	2 mW	8 ns
'S133	19 mW	3 ns

SN54ALS133 (J,FH) SN74ALS133 (N,FN)
SN54S133 (J,FH) SN74S133 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{ABCDEFGHIJKLM}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A	9	Y	1	nc	11	nc
2	B	10	H	2	A	12	Y
3	C	11	I	3	B	13	H
4	D	12	J	4	C	14	I
5	E	13	K	5	D	15	J
6	F	14	L	6	nc	16	nc
7	G	15	M	7	E	17	K
8	GND	16	V_{CC}	8	F	18	L
				9	G	19	M
				10	GND	20	V_{CC}

134

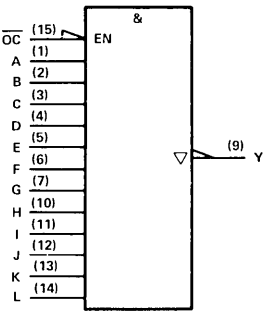
12-INPUT POSITIVE-NAND GATES WITH THREE-STATE OUTPUTS

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54S134	4.5 ns	−2 mA	20 mA
SN74S134	4.5 ns	−6.5 mA	20 mA

SN54S134 (J,FH) SN74S134 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{ABCDEFGHIJKL}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A	9	Y	1	nc	11	nc
2	B	10	H	2	A	12	Y
3	C	11	I	3	B	13	H
4	D	12	J	4	C	14	I
5	E	13	K	5	D	15	J
6	F	14	L	6	nc	16	nc
7	G	15	$\overline{OC}$	7	E	17	K
8	GND	16	V_{CC}	8	F	18	L
				9	G	19	$\overline{OC}$
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

135

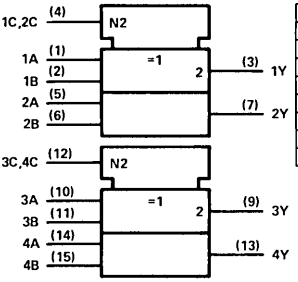
QUAD EXCLUSIVE OR/NOR GATES

SN54S135 (J,FH) SN74S135 (J,N,FN)

typical performance

TYPE	POWER	DELAY
'S135	325 mW	8 ns

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	9	3Y	1	nc	11	nc
2	1B	10	3A	2	1A	12	3Y
3	1Y	11	3B	3	1B	13	3A
4	1C,2C	12	3C,4C	4	1Y	14	3B
5	2A	13	4Y	5	1C,2C	15	3C,4C
6	2B	14	4A	6	nc	16	nc
7	2Y	15	4B	7	2A	17	4Y
8	GND	16	V_{CC}	8	2B	18	4A
				9	2Y	19	4B
				10	GND	20	V_{CC}

positive logic: $Y = A \oplus B \oplus C = A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C + ABC$

136

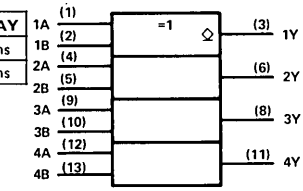
QUAD EXCLUSIVE-OR GATES WITH OPEN-COLLECTOR OUTPUTS

SN54136 (J,FH) SN74136 (J,N)
SN54LS136 (J,FH) SN74LS136 (J,N,FN)

typical performance

TYPE	POWER	DELAY
'136	150 mW	27 ns
'LS136	30 mW	18 ns

logic symbol†



positive logic: $Y = A \oplus B = A\bar{B} + \bar{A}B$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3Y	1	nc	11	nc
2	1B	9	3A	2	1A	12	3Y
3	1Y	10	3B	3	1B	13	3A
4	2A	11	4Y	4	1Y	14	3B
5	2B	12	4A	5	nc	15	nc
6	2Y	13	4B	6	2A	16	4Y
7	GND	14	V_{CC}	7	nc	17	nc
				8	2B	18	4A
				9	2Y	19	4B
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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137

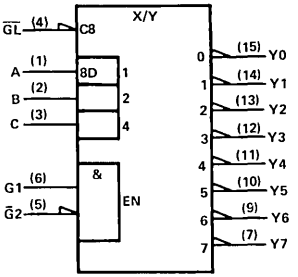
3- TO 8-LINE DECODERS/ DEMULTIPLEXERS WITH ADDRESS LATCHES

typical performance

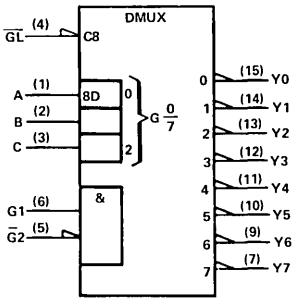
TYPE	SELECT TIME	ENABLE TIME	TOTAL POWER
'ALS137	11 ns	10 ns	25 mW
'LS137	17.5 ns	16 ns	55 mW

SN54ALS137 (J,FH) SN74ALS137 (N,FN)
SN54LS137 (J,FH) SN74LS137 (J,N,FN)

logic symbol†



OR



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A	9	Y6	1	nc	11	nc
2	B	10	Y5	2	A	12	Y6
3	C	11	Y4	3	B	13	Y5
4	$\overline{GL}$	12	Y3	4	C	14	Y4
5	$\overline{G2}$	13	Y2	5	$\overline{GL}$	15	Y3
6	G1	14	Y1	6	nc	16	nc
7	Y7	15	Y0	7	$\overline{G2}$	17	Y2
8	GND	16	V_{CC}	8	G1	18	Y1
				9	Y7	19	Y0
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

138

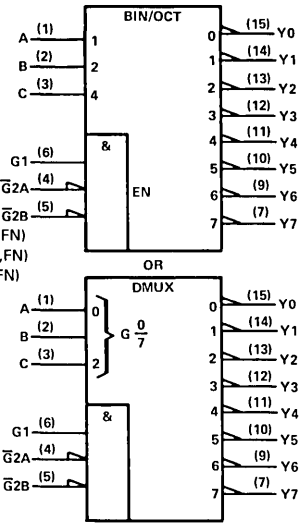
3- TO 8-LINE DECODERS/ DEMULTIPLEXERS

typical performance

TYPE	SELECT TIME	ENABLE TIME	TOTAL POWER
'ALS138	8.5 ns	9 ns	25 mW
'LS138	22 ns	21 ns	31 mW
'S138	8 ns	7 ns	245 mW

SN54ALS138 (J,FH) SN74ALS138 (N,FN)
SN54LS138 (J,FH) SN74LS138 (J,N,FN)
SN54S138 (J,FH) SN74S138 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A	9	Y6	1	nc	11	nc
2	B	10	Y5	2	A	12	Y6
3	C	11	Y4	3	B	13	Y5
4	$\overline{G}$2A	12	Y3	4	C	14	Y4
5	$\overline{G}$2B	13	Y2	5	$\overline{G}$2A	15	Y3
6	G1	14	Y1	6	nc	16	nc
7	Y7	15	Y0	7	$\overline{G}$2B	17	Y2
8	GND	16	V_{CC}	8	G1	18	Y1
				9	Y7	19	Y0
				10	GND	20	V_{CC}

139

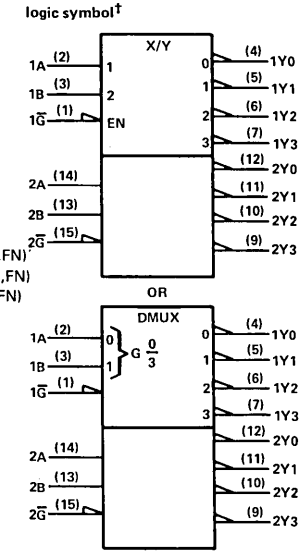
DUAL 2- TO 4-LINE DECODERS/DEMULTIPLEXERS

typical performance

TYPE	SELECT TIME	ENABLE TIME	TOTAL POWER
'ALS139			
'LS139	22 ns	19 ns	34 mW
'S139	7.5 ns	6 ns	300 mW

SN54ALS139 (J,FH) SN74ALS139 (N,FN)
SN54LS139 (J,FH) SN74LS139 (J,N,FN)
SN54S139 (J,FH) SN74S139 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1$\overline{G}$	9	2Y3	1	nc	11	nc
2	1A	10	2Y2	2	1$\overline{G}$	12	2Y3
3	1B	11	2Y1	3	1A	13	2Y2
4	1Y0	12	2Y0	4	1B	14	2Y1
5	1Y1	13	2B	5	1Y0	15	2Y0
6	1Y2	14	2A	6	nc	16	nc
7	1Y3	15	2$\overline{G}$	7	1Y1	17	2B
8	GND	16	V_{CC}	8	1Y2	18	2A
				9	1Y3	19	2$\overline{G}$
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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140

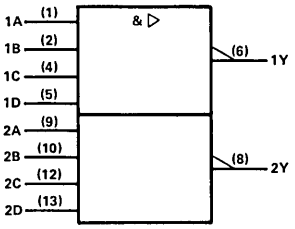
DUAL 4-INPUT POSITIVE-NAND 50-OHM LINE DRIVERS

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	DELAY	POWER PER GATE
'S140	60 mA	–40 mA	4 ns	44 mW

SN54S140 (J,FH) SN74S140 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{ABCD}$

pin assignments

J, N PACKAGES			
1	1A	8	2Y
2	1B	9	2A
3	nc	10	2B
4	1C	11	nc
5	1D	12	2C
6	1Y	13	2D
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	2Y
3	1B	13	2A
4	nc	14	2B
5	nc	15	nc
6	1C	16	nc
7	nc	17	nc
8	1D	18	2C
9	1Y	19	2D
10	GND	20	V_{CC}

141

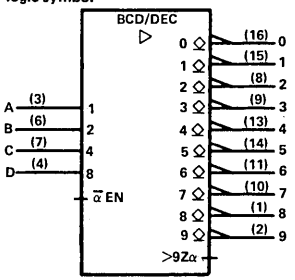
BCD-TO-DECIMAL DECODER/DRIVER

typical performance

TYPE	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TOTAL POWER
'141	7 mA	60 V	80 mW

SN74141 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	8	9	3
2	9	10	7
3	A	11	6
4	D	12	GND
5	V_{CC}	13	4
6	B	14	5
7	C	15	1
8	2	16	0

142

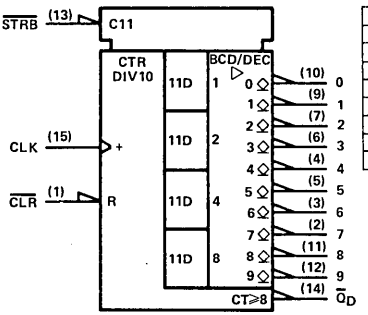
COUNTER/LATCH/DECODER/DRIVER

typical performance

TYPE	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TOTAL POWER
'142	7 mA	55 V	340 mW

SN74142 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	$\overline{CLR}$	9	1
2	7	10	0
3	6	11	8
4	4	12	9
5	5	13	STRB
6	3	14	$\overline{Q}_D$
7	2	15	CLK
8	GND	16	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

143,144

COUNTERS/LATCHES/ DECODERS/DRIVERS

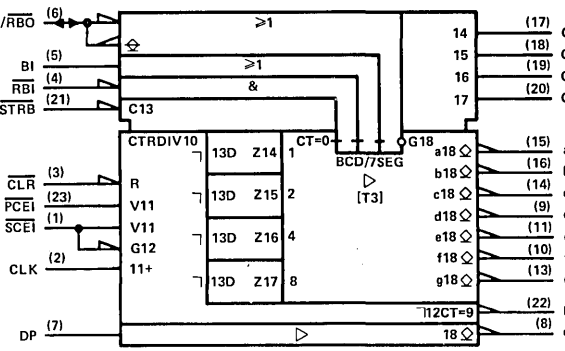
typical performance

TYPE	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE
SN54143	15 mA*	7 V
SN74143	15 mA*	7 V
SN54144	20 mA	15 V
SN74144	25 mA	15 V

SN54143 (J) SN74143 (J,N)
SN54144 (J) SN74144 (J,N)

* Constant current

logic symbol†



pin assignments

J, N PACKAGES			
1	SCEI	13	g
2	CLK	14	c
3	CLR	15	a
4	RBI	16	b
5	BI	17	QA
6	BI/RBO	18	QB
7	DP	19	QC
8	dp	20	QD
9	d	21	STRB
10	f	22	MAX
11	e	23	PCEI
12	GND	24	V_{CC}

145

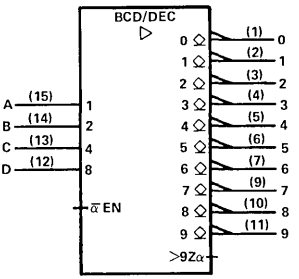
BCD-TO-DECIMAL DECODERS/ DRIVERS FOR LAMPS, RELAYS, MOS

typical performance

TYPE	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TOTAL POWER
'145	80 mA	15 V	215 mW
'54LS145	12 mA	15 V	35 mW
'74LS145	80 mA	15 V	35 mW

SN54145 (J,FH) SN74145 (J,N)
SN54LS145 (J,FH) SN74LS145 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	0	9	7	1	nc	11	nc
2	1	10	8	2	0	12	7
3	2	11	9	3	1	13	8
4	3	12	D	4	2	14	9
5	4	13	C	5	3	15	D
6	5	14	B	6	nc	16	nc
7	6	15	A	7	4	17	C
8	GND	16	V_{CC}	8	5	18	B
				9	6	19	A
				10	GND	20	V_{CC}

147

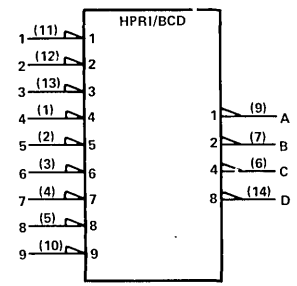
10-LINE DECIMAL TO 4-LINE BCD PRIORITY ENCODERS

typical performance

TYPE	POWER	DELAY
'147	225 mW	10 ns
'LS147	60 mW	15 ns

SN54147 (J,FH) SN74147 (J,N)
SN54LS147 (J,FH) SN74LS147 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	4	9	A	1	nc	11	nc
2	5	10	9	2	4	12	A
3	6	11	1	3	5	13	9
4	7	12	2	4	6	14	1
5	8	13	3	5	7	15	2
6	C	14	D	6	nc	16	nc
7	B	15	nc	7	8	17	3
8	GND	16	V_{CC}	8	C	18	D
				9	B	19	nc
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

FONT TABLE T3 — RESULTANT DISPLAYS USING '143, '144

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148

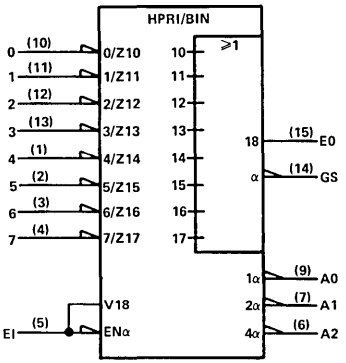
8- TO 3-LINE OCTAL PRIORITY ENCODERS

typical performance

TYPE	POWER	DELAY
'148	190 mW	12 ns
'LS148	60 mW	15 ns

SN54148 (J,FH) SN74148 (J,N)
SN54LS148 (J,FH) SN74LS148 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	4	9	A0	1	nc	11	nc
2	5	10	0	2	4	12	A0
3	6	11	1	3	5	13	0
4	7	12	2	4	6	14	1
5	E1	13	3	5	7	15	2
6	A2	14	GS	6	nc	16	nc
7	A1	15	E0	7	E1	17	3
8	GND	16	V_{CC}	8	A2	18	GS
				9	A1	19	E0
				10	GND	20	V_{CC}

150

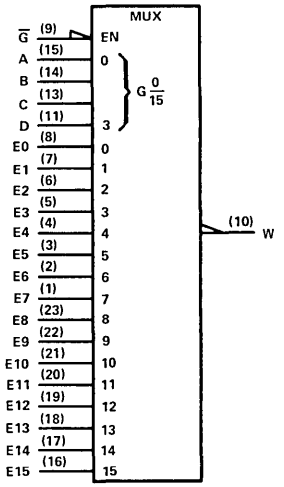
1-OF-16 DATA SELECTORS/ MULTIPLEXERS

typical performance

TYPE	DATA TO INV OUTPUT	FROM ENABLE	TOTAL POWER
'150	11 ns	18 ns	200 mW

SN54150 (J,FH) SN74150 (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	E7	13	C	1	nc	15	nc
2	E6	14	B	2	E7	16	C
3	E5	15	A	3	E6	17	B
4	E4	16	E15	4	E5	18	A
5	E3	17	E14	5	E4	19	E15
6	E2	18	E13	6	E3	20	E14
7	E1	19	E12	7	E2	21	E13
8	E0	20	E11	8	nc	22	nc
9	$\overline{G}$	21	E10	9	E1	23	E12
10	W	22	E9	10	E0	24	E11
11	D	23	E8	11	$\overline{G}$	25	E10
12	GND	24	V_{CC}	12	W	26	E9
				13	D	27	E8
				14	GND	28	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

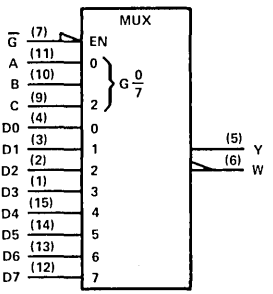
151

1-OF-8 DATA SELECTORS/MULTIPLEXERS
typical performance

TYPE	DELAY TIMES: DATA TO INV OUTPUT	DELAY TIMES: DATA TO NON-INV OUTPUT	DELAY TIMES: FROM ENABLE	TOTAL POWER
'151A	8 ns	16 ns	22 ns	145 mW
'ALS151	6 ns	5 ns	4.5 ns	30 mW
'AS151	3 ns	3.5 ns	5 ns	130 mW
'LS151	11 ns	18 ns	27 ns	30 mW
'S151	4.5 ns	8 ns	9 ns	225 mW

SN54151A (J,FH) SN74151A (J,N)
SN54ALS151 (J,FH) SN74ALS151 (N,FN)
SN54AS151 (J,FH) SN74AS151 (N,FN)
SN54LS151 (J,FH) SN74LS151 (J,N,FN)
SN54S151 (J,FH) SN74S151 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	D3	9	C	1	nc	11	nc
2	D2	10	B	2	D3	12	C
3	D1	11	A	3	D2	13	B
4	D0	12	D7	4	D1	14	A
5	Y	13	D6	5	D0	15	D7
6	W	14	D5	6	nc	16	nc
7	$\overline{G}$	15	D4	7	Y	17	D6
8	GND	16	V_{CC}	8	W	18	D5
				9	$\overline{G}$	19	D4
				10	GND	20	V_{CC}

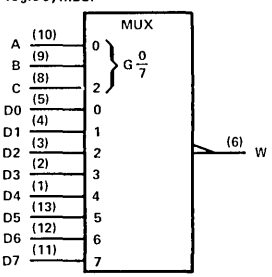
152

1-of-8 DATA SELECTORS/MULTIPLEXERS
typical performance

TYPE	DELAY TIMES: DATA TO INV OUTPUT	DELAY TIMES: FROM ENABLE	TOTAL POWER
'152A	8 ns		130 mW
'LS152	11 ns	18 ns	28 mW

SN54152A (J,FH)
SN54LS152 (J,FH) SN74LS152 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	D4	8	C	1	nc	11	nc
2	D3	9	B	2	D4	12	C
3	D2	10	A	3	D3	13	B
4	D1	11	D7	4	D2	14	A
5	D0	12	D6	5	nc	15	nc
6	W	13	D5	6	D1	16	D7
7	GND	14	V_{CC}	7	nc	17	nc
				8	D0	18	D6
				9	W	19	D5
				10	GND	20	V_{CC}

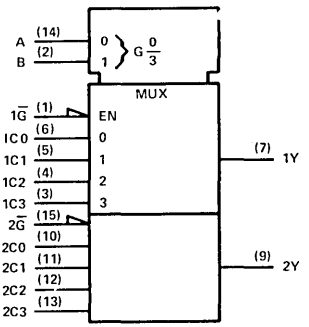
153

DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS
typical performance

TYPE	DELAY TIMES: DATA TO NON-INV OUTPUT	DELAY TIMES: FROM ENABLE	TOTAL POWER
'153	14 ns	17 ns	180 mW
'ALS153	5 ns	4.5 ns	31.5 mW
'AS153	3.5 ns	5 ns	105 mW
'L153	27 ns	34 ns	90 mW
'LS153	14 ns	17 ns	31 mW
'S153	6 ns	9.5 ns	225 mW

SN54153 (J,FH) SN74153 (J,N)
SN54ALS153 (J,FH) SN74ALS153 (N,FN)
SN54AS153 (J,FH) SN74AS153 (N,FN)
SN54L153 (J)
SN54LS153 (J,FH) SN74LS153 (J,N,FN)
SN54S153 (J,FH) SN74S153 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$1\overline{G}$	9	2Y	1	nc	11	nc
2	B	10	2C0	2	$1\overline{G}$	12	2Y
3	1C3	11	2C1	3	B	13	2C0
4	1C2	12	2C2	4	1C3	14	2C1
5	1C1	13	2C3	5	1C2	15	2C2
6	1C0	14	A	6	nc	16	nc
7	1Y	15	$2\overline{G}$	7	1C1	17	2C3
8	GND	16	V_{CC}	8	1C0	18	A
				9	1Y	19	$2\overline{G}$
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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154

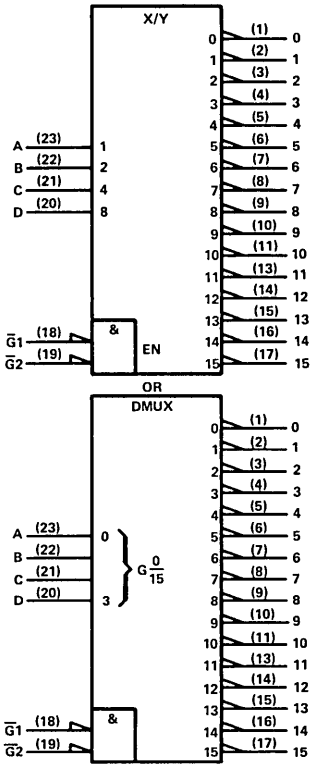
4-LINE TO 16-LINE DECODERS/ DEMULTIPLEXERS

typical performance

TYPE	SELECT TIME	ENABLE TIME	TOTAL POWER
'154	23 ns	19 ns	170 mW
'L154	46 ns	38 ns	85 mW

SN54154 (J,FH) SN74154 (J,N)
SN54L154 (J)

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	0	13	11	1	nc	15	nc
2	1	14	12	2	0	16	11
3	2	15	13	3	1	17	12
4	3	16	14	4	2	18	13
5	4	17	15	5	3	19	14
6	5	18	$\overline{G1}$	6	4	20	15
7	6	19	$\overline{G2}$	7	5	21	$\overline{G1}$
8	7	20	D	8	nc	22	nc
9	8	21	C	9	6	23	$\overline{G2}$
10	9	22	B	10	7	24	D
11	10	23	A	11	8	25	C
12	GND	24	V_{CC}	12	9	26	B
				13	10	27	A
				14	GND	28	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

155

DECODERS/DEMULTIPLEXERS

(totem pole outputs)

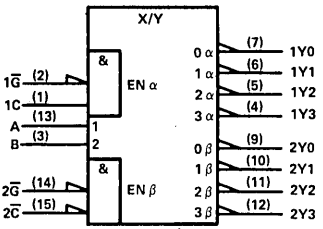
typical performance

TYPE	SELECT TIME	ENABLE TIME	TOTAL POWER
'155	21 ns	16 ns	125 mW
'LS155	18 ns	15 ns	30 mW

SN54155 (J,FH) SN74155 (J,N)
SN54LS155 (J,FH) SN74LS155 (J,N,FN)

logic symbol†

2-line to 4-line Decoder

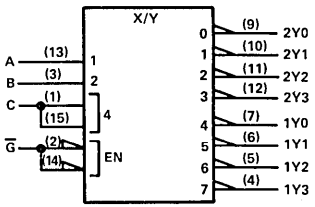


pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1C	9	2Y0	1	nc	11	nc
2	1$\overline{G}$	10	2Y1	2	1C	12	2Y0
3	B	11	2Y2	3	1$\overline{G}$	13	2Y1
4	1Y3	12	2Y3	4	B	14	2Y2
5	1Y2	13	A	5	1Y3	15	2Y3
6	1Y1	14	2$\overline{G}$	6	nc	16	nc
7	1Y0	15	2$\overline{C}$	7	1Y2	17	A
8	GND	16	V_{CC}	8	1Y1	18	2$\overline{G}$
				9	1Y0	19	2$\overline{C}$
				10	GND	20	V_{CC}

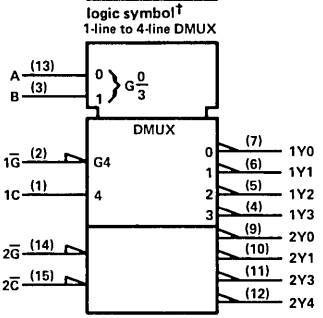
logic symbol†

3-line to 8-line Decoder



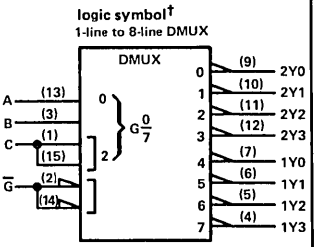
logic symbol†

1-line to 4-line DMUX



logic symbol†

1-line to 8-line DMUX



156

DECODERS/DEMULTIPLEXERS

(open-collector outputs)

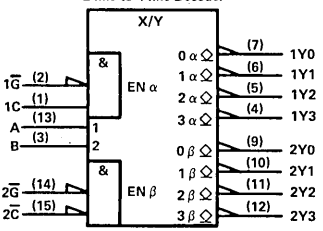
typical performance

TYPE	SELECT TIME	ENABLE TIME	TOTAL POWER
'156	23 ns	18 ns	125 mW
'LS156	33 ns	26 ns	31 mW

SN54156 (J,FH) SN74156 (J,N)
SN54LS156 (J,FH) SN74LS156 (J,N,FN)

logic symbol†

2-line to 4-line Decoder

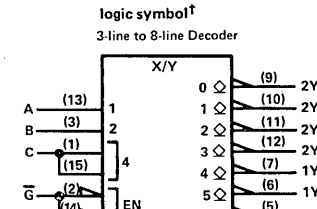


pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1C	9	2Y0	1	nc	11	nc
2	1$\overline{G}$	10	2Y1	2	1C	12	2Y0
3	B	11	2Y2	3	1$\overline{G}$	13	2Y1
4	1Y3	12	2Y3	4	B	14	2Y2
5	1Y2	13	A	5	1Y3	15	2Y3
6	1Y1	14	2$\overline{G}$	6	nc	16	nc
7	1Y0	15	2$\overline{C}$	7	1Y2	17	A
8	GND	16	V_{CC}	8	1Y1	18	2$\overline{G}$
				9	1Y0	19	2$\overline{C}$
				10	GND	20	V_{CC}

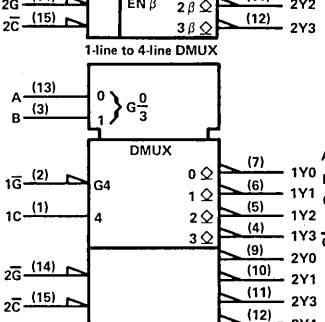
logic symbol†

3-line to 8-line Decoder



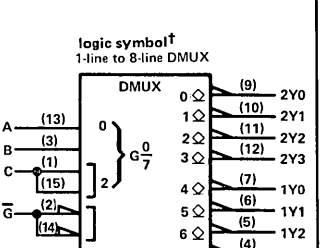
logic symbol†

1-line to 4-line DMUX



logic symbol†

1-line to 8-line DMUX



† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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157

QUAD 2- TO 1-LINE DATA SELECTORS/MULTIPLEXERS

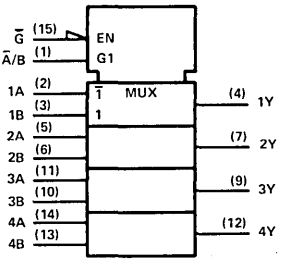
(non-inverted data outputs)

typical performance

TYPE	DELAY TIMES: DATA TO NON-INV OUTPUT	DELAY TIMES: FROM ENABLE	TOTAL POWER
'157	9 ns	14 ns	150 mW
'ALS157	5 ns	6.5 ns	39 mW
'L157	18 ns	27 ns	75 mW
'LS157	9 ns	14 ns	49 mW
'S157	5 ns	8 ns	250 mW

SN54157 (J,FH) SN74157 (J,N)
SN54ALS157 (J,FH) SN74ALS157 (N,FN)
SN54L157 (J)
SN54LS157 (J,FH) SN74LS157 (J,N,FN)
SN54S157 (J,FH) SN74S157 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A/B	9	3Y	1	nc	11	nc
2	1A	10	3B	2	A/B	12	3Y
3	1B	11	3A	3	1A	13	3B
4	1Y	12	4Y	4	1B	14	3A
5	2A	13	4B	5	1Y	15	4Y
6	2B	14	4A	6	nc	16	nc
7	2Y	15	G	7	2A	17	4B
8	GND	16	V_{CC}	8	2B	18	4A
				9	2Y	19	G
				10	GND	20	V_{CC}

158

QUAD 2- TO 1-LINE DATA SELECTORS/MULTIPLEXERS

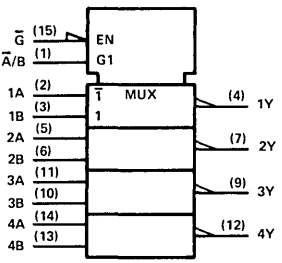
(inverted data outputs)

typical performance

TYPE	DELAY TIMES: DATA TO INV OUTPUT	DELAY TIMES: FROM ENABLE	TOTAL POWER
'ALS158	5 ns	6.5 ns	11.5 mW
'LS158	7 ns	12 ns	24 mW
'S158	4 ns	7 ns	195 mW

SN54'ALS158 (J,FH) SN74ALS158 (N,FN)
SN54LS158 (J,FH) SN74LS158 (J,N,FN)
SN54S158 (J,FH) SN74S158 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A/B	9	3Y	1	nc	11	nc
2	1A	10	3B	2	A/B	12	3Y
3	1B	11	3A	3	1A	13	3B
4	1Y	12	4Y	4	1B	14	3A
5	2A	13	4B	5	1Y	15	4Y
6	2B	14	4A	6	nc	16	nc
7	2Y	15	G	7	2A	17	4B
8	GND	16	V_{CC}	8	2B	18	4A
				9	2Y	19	G
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

159

4- TO 16-LINE DECODERS/ DEMULTIPLEXERS

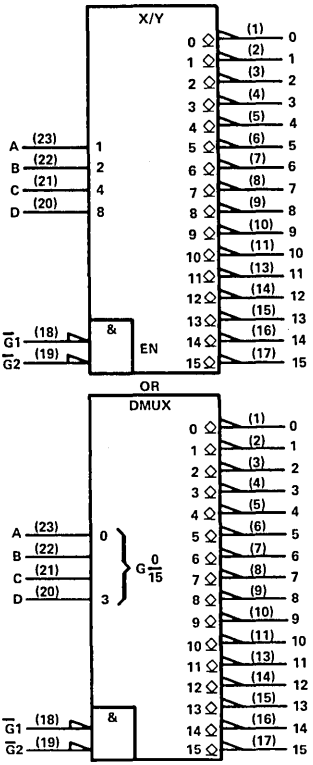
(open-collector outputs)

typical performance

TYPE	SELECT TIME	ENABLE TIME	TOTAL POWER
'159	24 ns	19 ns	170 mW

SN54159 (J,FH) SN74159 (J,N)

logic symbol, '159†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	0	13	11	1	nc	15	nc
2	1	14	12	2	0	16	11
3	2	15	13	3	1	17	12
4	3	16	14	4	2	18	13
5	4	17	15	5	3	19	14
6	5	18	$\overline{G1}$	6	4	20	15
7	6	19	$\overline{G2}$	7	5	21	$\overline{G1}$
8	7	20	D	8	nc	22	nc
9	8	21	C	9	6	23	$\overline{G2}$
10	9	22	B	10	7	24	D
11	10	23	A	11	8	25	C
12	GND	24	V_{CC}	12	9	26	B
				13	10	27	A
				14	GND	28	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

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160

SYNCHRONOUS 4-BIT COUNTERS

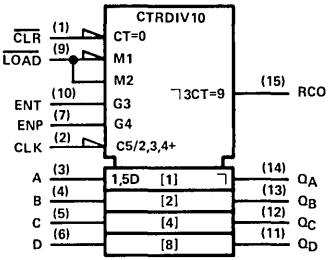
(decade, direct clear)

typical performance

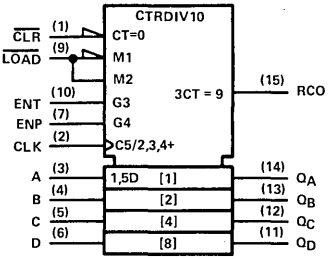
TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'160	25 MHz	ASYNC-L	305 mW
'ALS160	40 MHz	ASYNC-L	60 mW
'AS160		ASYNC-L	
'LS160A	25 MHz	ASYNC-L	93 mW

SN54160 (J,FH) SN74160 (J,N)
SN54ALS160 (J,FH) SN74ALS160 (N,FN)
SN54AS160 (J,FH) SN74AS160 (N,FN)
SN54LS160A (J,FH) SN74LS160A (J,N,FN)

logic symbol, '160†



logic symbol, 'LS160A†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{CLR}$	9	$\overline{LOAD}$	1	nc	11	nc
2	CLK	10	ENT	2	$\overline{CLR}$	12	$\overline{LOAD}$
3	A	11	Q_D	3	CLK	13	ENT
4	B	12	Q_C	4	A	14	Q_D
5	C	13	Q_B	5	B	15	Q_C
6	D	14	Q_A	6	nc	16	nc
7	ENP	15	RCO	7	C	17	Q_B
8	GND	16	V_{CC}	8	D	18	Q_A
				9	ENP	19	RCO
				10	GND	20	V_{CC}

161

SYNCHRONOUS 4-BIT COUNTERS

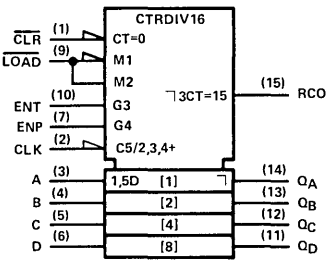
(binary, direct clear)

typical performance

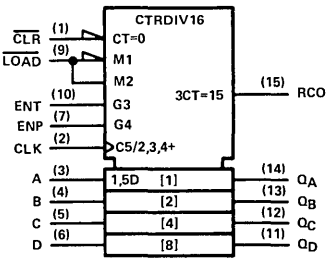
TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'161	25 MHz	ASYNC-L	305 mW
'ALS161	40 MHz	ASYNC-L	60 mW
'AS161		ASYNC-L	
'LS161A	25 MHz	ASYNC-L	93 mW

SN54161 (J,FH) SN74161 (J,N)
SN54ALS161 (J,FH) SN74ALS161 (N,FN)
SN54AS161 (J,FH) SN74AS161 (N,FN)
SN54LS161A (J,FH) SN74LS161A (J,N,FN)

logic symbol, '161†



logic symbol, 'LS161A†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{CLR}$	9	$\overline{LOAD}$	1	nc	11	nc
2	CLK	10	ENT	2	$\overline{CLR}$	12	$\overline{LOAD}$
3	A	11	Q_D	3	CLK	13	ENT
4	B	12	Q_C	4	A	14	Q_D
5	C	13	Q_B	5	B	15	Q_C
6	D	14	Q_A	6	nc	16	nc
7	ENP	15	RCO	7	C	17	Q_B
8	GND	16	V_{CC}	8	D	18	Q_A
				9	ENP	19	RCO
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

162

SYNCHRONOUS 4-BIT COUNTERS

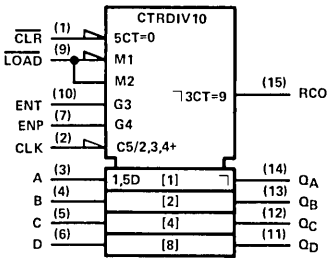
(decade, synchronous clear)

typical performance

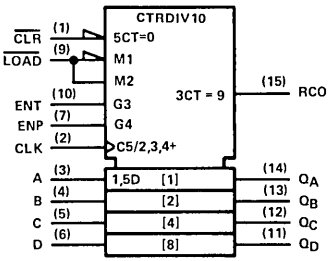
TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'162	25 MHz	SYNC-L	305 mW
'ALS162	40 MHz	SYNC-L	60 mW
'AS162		SYNC-L	
'LS162A	25 MHz	SYNC-L	93 mW
'S162	40 MHz	SYNC-L	475 mW

SN54162 (J,FH) SN74162 (J,N)
SN54ALS162 (J,FH) SN74ALS162 (N,FN)
SN54AS162 (J,FH) SN74AS162 (N,FN)
SN54LS162A (J,FH) SN74LS162A (J,N,FN)
SN54S162 (J,FH) SN74S162 (J,N,FN)

logic symbol, '162†



logic symbol, 'LS162A, 'S162†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	CLR	9	LOAD	1	nc	11	nc
2	CLK	10	ENT	2	CLR	12	LOAD
3	A	11	Q_D	3	CLK	13	ENT
4	B	12	Q_C	4	A	14	Q_D
5	C	13	Q_B	5	B	15	Q_C
6	D	14	Q_A	6	nc	16	nc
7	ENP	15	RCO	7	C	17	Q_B
8	GND	16	V_{CC}	8	D	18	Q_A
				9	ENP	19	RCO
				10	GND	20	V_{CC}

163

SYNCHRONOUS 4-BIT COUNTERS

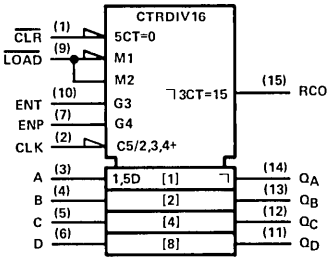
(binary, synchronous clear)

typical performance

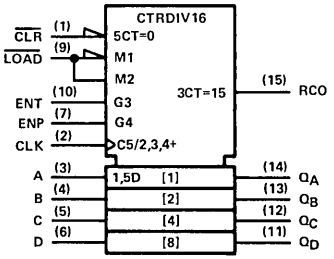
TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'163	25 MHz	SYNC-L	305 mW
'ALS163	40 MHz	SYNC-L	60 mW
'AS163		SYNC-L	
'LS163A	25 MHz	SYNC-L	93 mW
'S163	40 MHz	SYNC-L	475 mW

SN54163 (J,FH) SN74163 (J,N)
SN54ALS163 (J,FH) SN74ALS163 (N,FN)
SN54AS163 (J,FH) SN74AS163 (N,FN)
SN54LS163A (J,FH) SN74LS163A (J,N,FN)
SN54S163 (J,FH) SN74S163 (J,N,FN)

logic symbol, '163†



logic symbol, 'LS163A, 'S163†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	CLR	9	LOAD	1	nc	11	nc
2	CLK	10	ENT	2	CLR	12	LOAD
3	A	11	Q_D	3	CLK	13	ENT
4	B	12	Q_C	4	A	14	Q_D
5	C	13	Q_B	5	B	15	Q_C
6	D	14	Q_A	6	nc	16	nc
7	ENP	15	RCO	7	C	17	Q_B
8	GND	16	V_{CC}	8	D	18	Q_A
				9	ENP	19	RCO
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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164

8-BIT PARALLEL OUT SERIAL SHIFT REGISTERS

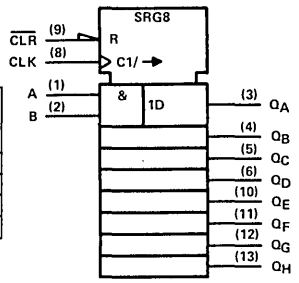
(asynchronous clear)

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'164	25 MHz	GATED D	LOW	167 mW
'ALS164		GATED D	LOW	
'L164	12 MHz	GATED D	LOW	84 mW
'LS164	25 MHz	GATED D	LOW	80 mW

SN54164 (J,FH) SN74164 (J,N)
SN54ALS164 (J,FH) SN74ALS164 (N,FN)
SN54L164 (J)
SN54LS164 (J,FH) SN74LS164 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A	8	CLK	1	nc	11	nc
2	B	9	$\overline{CLR}$	2	A	12	CLK
3	Q_A	10	Q_E	3	B	13	$\overline{CLR}$
4	Q_B	11	Q_F	4	Q_A	14	Q_E
5	Q_C	12	Q_G	5	nc	15	nc
6	Q_D	13	Q_H	6	Q_B	16	Q_F
7	GND	14	V_{CC}	7	nc	17	nc
				8	Q_C	18	Q_G
				9	Q_D	19	Q_H
				10	GND	20	V_{CC}

165

8-BIT SHIFT REGISTERS

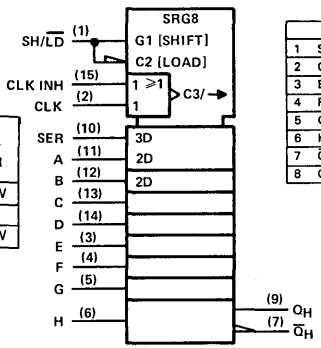
(parallel-load with complementary outputs)

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'165	25 MHz	D	NONE	210 mW
'ALS165				
'LS165	35 MHz	D	NONE	105 mW

SN54165 (J,FH) SN74165 (J,N)
SN54ALS165 (J,FH) SN74ALS165 (N,FN)
SN54LS165 (J,FH) SN74LS165 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	SH/$\overline{LD}$	9	Q_H	1	nc	11	nc
2	CLK	10	SER	2	SH/$\overline{LD}$	12	Q_H
3	E	11	A	3	CLK	13	SER
4	F	12	B	4	E	14	A
5	G	13	C	5	F	15	B
6	H	14	D	6	nc	16	nc
7	$\overline{Q}_H$	15	CLK INH	7	G	17	C
8	GND	16	V_{CC}	8	H	18	D
				9	$\overline{Q}_H$	19	CLK INH
				10	GND	20	V_{CC}

166

8-BIT SHIFT REGISTERS

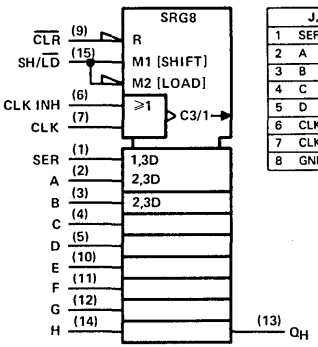
(parallel/serial input; serial output)

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'166	20 MHz	D	LOW	360 mW
'ALS166		D	LOW	
'LS166	35 MHz	D	LOW	110 mW

SN54166 (J,FH) SN74166 (J,N)
SN54ALS166 (J,FH) SN74ALS166 (N,FN)
SN54LS166 (J,FH) SN74LS166 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	SER	9	$\overline{CLR}$	1	nc	11	nc
2	A	10	E	2	SER	12	$\overline{CLR}$
3	B	11	F	3	A	13	E
4	C	12	G	4	B	14	F
5	D	13	Q_H	5	C	15	G
6	CLK INH	14	H	6	nc	16	nc
7	CLK	15	SH/$\overline{LD}$	7	D	17	Q_H
8	GND	16	V_{CC}	8	CLK INH	18	H
				9	CLK	19	SH/$\overline{LD}$
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc – no internal connection.

167

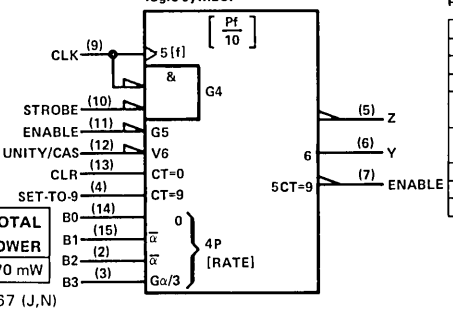
SYNCHRONOUS DECADE RATE MULTIPLIERS

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'167	25 MHz	ASYNC-H	270 mW

SN54167 (J,FH) SN74167 (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1 nc	9 CLK	1 nc	11 nc				
2 B2	10 STRB	2 nc	12 CLK				
3 B3	11 ENin	3 B2	13 STRB				
4 SET-TO-9	12 UNITY/CAS	4 B3	14 ENin				
5 Z	13 CLR	5 SET-TO-9	15 UNITY/CAS				
6 Y	14 BO	6 nc	16 nc				
7 ENout	15 B1	7 Z	17 CLR				
8 GND	16 V_{CC}	8 Y	18 BO				
		9 ENout	19 B1				
		10 GND	20 V_{CC}				

168

4-BIT UP/DOWN SYNCHRONOUS COUNTERS

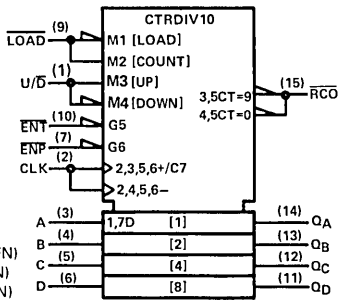
(decade)

typical performance

TYPE	COUNT FREQ	TOTAL POWER
'ALS168	40 MHz	75 mW
'AS168		
'S168	40 MHz	500 mW

SN54ALS168 (J,FH) SN74ALS168 (N,FN)
SN54AS168 (J,FH) SN74AS168 (N,FN)
SN54S168 (J,FH) SN74S168 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1 U/D	9 LOAD	1 nc	11 nc				
2 CLK	10 ENT	2 U/D	12 LOAD				
3 A	11 Q_D	3 CLK	13 ENT				
4 B	12 Q_C	4 A	14 Q_D				
5 C	13 Q_B	5 B	15 Q_C				
6 D	14 Q_A	6 nc	16 nc				
7 ENP	15 RCO	7 C	17 Q_B				
8 GND	16 V_{CC}	8 D	18 Q_A				
		9 ENP	19 RCO				
		10 GND	20 V_{CC}				

169

4-BIT UP/DOWN SYNCHRONOUS COUNTERS

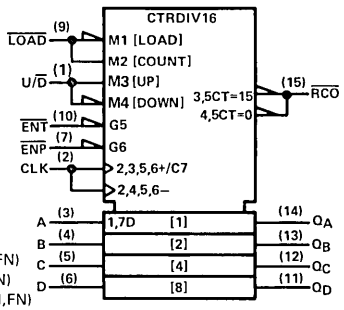
(binary)

typical performance

TYPE	COUNT FREQ	TOTAL POWER
'ALS169	40 MHz	75 mW
'AS169		
'LS169B	35 MHz	140 mW
'S169	40 MHz	500 mW

SN54ALS169 (J,FH) SN74ALS169 (N,FN)
SN54AS169 (J,FH) SN74AS169 (N,FN)
SN54LS169B (J,FH) SN74LS169B (J,N,FN)
SN54S169 (J,FH) SN74S169 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1 U/D	9 LOAD	1 nc	11 nc				
2 CLK	10 ENT	2 U/D	12 LOAD				
3 A	11 Q_D	3 CLK	13 ENT				
4 B	12 Q_C	4 A	14 Q_D				
5 C	13 Q_B	5 B	15 Q_C				
6 D	14 Q_A	6 nc	16 nc				
7 ENP	15 RCO	7 C	17 Q_B				
8 GND	16 V_{CC}	8 D	18 Q_A				
		9 ENP	19 RCO				
		10 GND	20 V_{CC}				

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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170

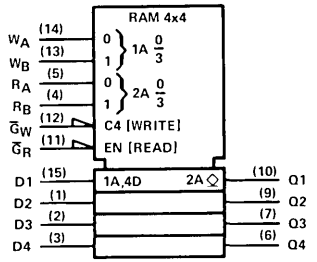
4-BY-4 REGISTER FILES

typical performance

TYPE	TYPE OF OUTPUT	ADDRESS TIME	POWER PER BIT
'170	O-C	30 ns	40 mW
'LS170	O-C	27 ns	7.8 mW

SN54170 (J,FH) SN74170 (J,N)
SN54LS170 (J,FH) SN74LS170 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	D2	9	Q2	1	nc	11	nc
2	D3	10	Q1	2	D2	12	Q2
3	D4	11	$\overline{G}_R$	3	D3	13	Q1
4	R_B	12	$\overline{G}_W$	4	D4	14	$\overline{G}_R$
5	R_A	13	W_B	5	R_B	15	$\overline{G}_W$
6	Q4	14	W_A	6	nc	16	nc
7	Q3	15	D1	7	R_A	17	W_B
8	GND	16	V_{CC}	8	Q4	18	W_A
				9	Q3	19	D1
				10	GND	20	V_{CC}

171

QUAD D-TYPE FLIP-FLOPS WITH CLEAR

- Double-Rail Outputs
- Buffered Clock and Clear Inputs
- Individual Data Inputs to Each Flip-Flop

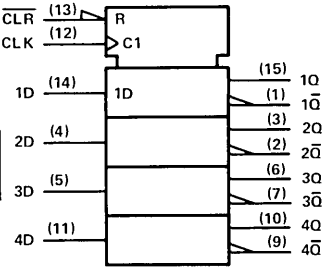
typical performance

TYPE	FREQ	POWER PER F-F	DELAY TIMES SETUP	DELAY TIMES HOLD
'LS171	30 MHz	17.5 mW	20 ns†	5 ns†

† Rising edge of clock pulse

SN54LS171 (J,FH) SN74LS171 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$1\overline{Q}$	9	$4\overline{Q}$	1	nc	11	nc
2	$2\overline{Q}$	10	4Q	2	$1\overline{Q}$	12	$4\overline{Q}$
3	2Q	11	4D	3	$2\overline{Q}$	13	4Q
4	2D	12	CLK	4	2Q	14	4D
5	3D	13	$\overline{CLR}$	5	2D	15	CLK
6	3Q	14	1D	6	nc	16	nc
7	$3\overline{Q}$	15	1Q	7	3D	17	$\overline{CLR}$
8	GND	16	V_{CC}	8	3Q	18	1D
				9	$3\overline{Q}$	19	1Q
				10	GND	20	V_{CC}

For chip carrier information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

172

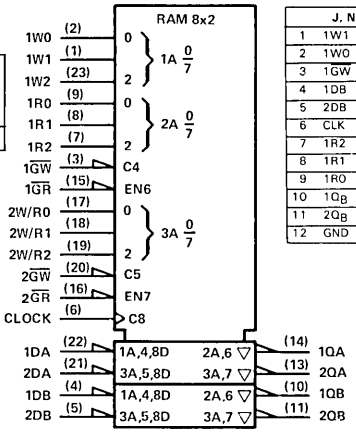
16-BIT REGISTER FILES

typical performance

TYPE	ORG	TYPE OF OUTPUT	ADDRESS TIME	POWER PER BIT
'172	8X2	3-State	33 ns	35 mW

SN74172 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	1W1	13	$2Q_A$
2	1W0	14	$1Q_A$
3	1GW	15	$1\overline{GR}$
4	1DB	16	$2\overline{GR}$
5	2DB	17	2W/R0
6	CLK	18	2W/R1
7	1R2	19	2W/R2
8	1R1	20	2GW
9	1R0	21	2DA
10	$1Q_B$	22	1DA
11	$2Q_B$	23	1W2
12	GND	24	V_{CC}

173

4-BIT D-TYPE REGISTERS

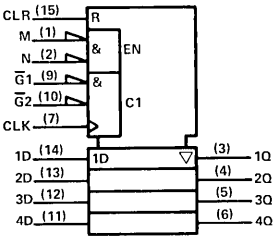
(3-state outputs)

typical performance

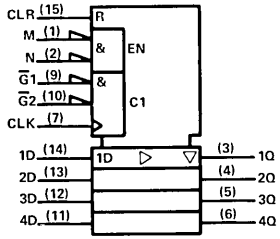
TYPE	FREQ	ASYNC CLEAR	TOTAL POWER
'173	25 MHz	HIGH	250 mW
'LS173A	50 MHz	HIGH	85 mW

SN54173 (J,FH) SN74173 (J,N)
SN54LS173A (J,FH) SN74LS173A (J,N,FN)

logic symbol, '173†



logic symbol, 'LS173A†



pin assignments

J, N PACKAGES			
1	M	9	$\overline{G1}$
2	N	10	$\overline{G2}$
3	1Q	11	4D
4	2Q	12	3D
5	3Q	13	2D
6	4Q	14	1D
7	CLK	15	CLR
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	M	12	$\overline{G1}$
3	N	13	$\overline{G2}$
4	1Q	14	4D
5	2Q	15	3D
6	nc	16	nc
7	3Q	17	2D
8	4Q	18	1D
9	CLK	19	CLR
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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174

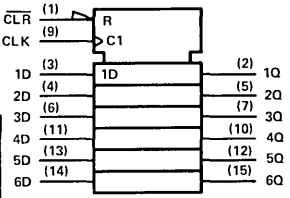
HEX D-TYPE FLIP-FLOPS
(single-rail outputs, common direct clear)
typical performance

TYPE	FREQ	POWER PER F-F	DELAY TIMES SETUP	DELAY TIMES HOLD
'174	35 MHz	38 mW	20 ns†	5 ns†
'ALS174	80 MHz	6.7 mW		
'AS174	175 MHz	38 mW		
'LS174	40 MHz	10.6 mW	20 ns†	5 ns†
'S174	110 MHz	75 mW	5 ns†	3 ns†

† Rising edge of clock pulse

SN54174 (J,FH) SN74174 (J,N)
SN54ALS174 (J,FH) SN74ALS174 (N,FN)
SN54AS174 (J,FH) SN74AS174 (N,FN)
SN54LS174 (J,FH) SN74LS174 (J,N,FN)
SN54S174 (J,FH) SN74S174 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{CLR}$	9	CLK	1	nc	11	nc
2	1Q	10	4Q	2	$\overline{CLR}$	12	CLK
3	1D	11	4D	3	1Q	13	4Q
4	2D	12	5Q	4	1D	14	4D
5	2Q	13	5D	5	2D	15	5Q
6	3D	14	6D	6	nc	16	nc
7	3Q	15	6Q	7	2Q	17	5D
8	GND	16	V_{CC}	8	3D	18	6D
				9	3Q	19	6Q
				10	GND	20	V_{CC}

175

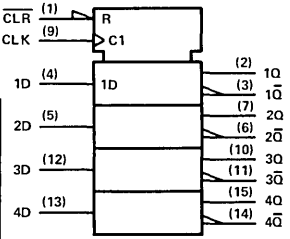
QUAD D-TYPE FLIP-FLOPS
(complementary outputs, common direct clear)
typical performance

TYPE	FREQ	POWER PER F-F	DELAY TIMES SETUP	DELAY TIMES HOLD
'175	35 MHz	38 mW	20 ns†	5 ns†
'ALS175	80 MHz	7.5 mW		
'AS175	175 MHz	41 mW		
'LS175	40 MHz	10.6 mW	20 ns†	5 ns†
'S175	110 MHz	75 mW	5 ns†	3 ns†

† Rising edge of clock pulse

SN54175 (J,FH) SN74175 (J,N)
SN54ALS175 (J,FH, SN74ALS175 (N,FN)
SN54AS175 (J,FH) SN74AS175 (N,FN)
SN54LS175 (J,FH) SN74LS175 (J,N,FN)
SN54S175 (J,FH) SN74S175 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{CLR}$	9	CLK	1	nc	11	nc
2	1Q	10	3Q	2	$\overline{CLR}$	12	CLK
3	1Q̄	11	3Q̄	3	1Q	13	3Q
4	1D	12	3D	4	1Q̄	14	3Q̄
5	2D	13	4D	5	1D	15	3D
6	2Q̄	14	4Q̄	6	nc	16	nc
7	2Q	15	4Q	7	2D	17	4D
8	GND	16	V_{CC}	8	2Q̄	18	4Q̄
				9	2Q	19	4Q
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

176

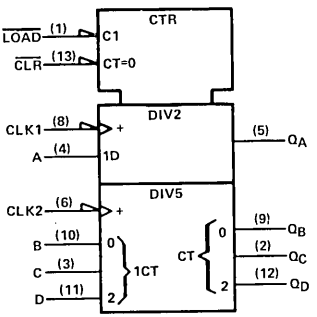
PRESETTABLE DECADE/ BIQUINARY COUNTERS

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'176	35 MHz	LOW	150 mW

SN54176 (J,FH) SN74176 (J,N)

logic symbol, '176†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	$\overline{LOAD}$	8	CLK1	1	nc	11	nc
2	Q_C	9	Q_B	2	$\overline{LOAD}$	12	CLK1
3	C	10	B	3	Q_C	13	Q_B
4	A	11	D	4	C	14	B
5	Q_A	12	Q_D	5	nc	15	nc
6	CLK2	13	$\overline{CLR}$	6	A	16	D
7	GND	14	V_{CC}	7	nc	17	nc
				8	Q_A	18	Q_D
				9	CLK2	19	$\overline{CLR}$
				10	GND	20	V_{CC}

177

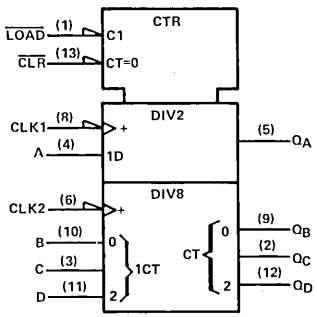
PRESETTABLE BINARY COUNTERS

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'177	35 MHz	LOW	150 mW

SN54177 (J,FH) SN74177 (J,N)

logic symbol, '177†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	$\overline{LOAD}$	8	CLK1	1	nc	11	nc
2	Q_C	9	Q_B	2	$\overline{LOAD}$	12	CLK1
3	C	10	B	3	Q_C	13	Q_B
4	A	11	D	4	C	14	B
5	Q_A	12	Q_D	5	nc	15	nc
6	CLK2	13	$\overline{CLR}$	6	A	16	D
7	GND	14	V_{CC}	7	nc	17	nc
				8	Q_A	18	Q_D
				9	CLK2	19	$\overline{CLR}$
				10	GND	20	V_{CC}

178

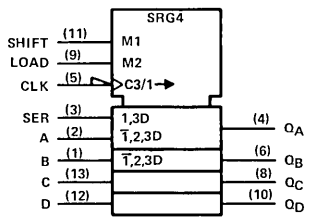
4-BIT UNIVERSAL SHIFT REGISTER

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'178	25 MHz	D	NONE	230 mW

SN54178 (J,FH) SN74178 (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	B	8	Q_C	1	nc	11	nc
2	A	9	LOAD	2	B	12	Q_C
3	SER	10	Q_D	3	A	13	LOAD
4	Q_A	11	SHIFT	4	SER	14	Q_D
5	CLK	12	D	5	nc	15	nc
6	Q_B	13	C	6	Q_A	16	SHIFT
7	GND	14	V_{CC}	7	nc	17	nc
				8	CLK	18	D
				9	Q_B	19	C
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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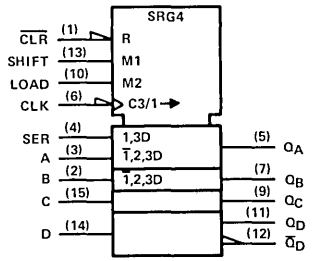
179

4-BIT UNIVERSAL SHIFT REGISTERS
(direct clear; Q_D complementary outputs)
typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'179	25 MHz	D	LOW	230 mW

SN54179 (J,FH) SN74179 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	$\overline{CLR}$	9	Q_C
2	B	10	LOAD
3	A	11	Q_D
4	SER	12	$\overline{Q}_D$
5	Q_A	13	SHIFT
6	CLK	14	D
7	Q_B	15	C
8	GND	16	V_{CC}

FH PACKAGE			
1	nc	11	nc
2	$\overline{CLR}$	12	Q_C
3	B	13	LOAD
4	A	14	Q_D
5	SER	15	$\overline{Q}_D$
6	nc	16	nc
7	Q_A	17	SHIFT
8	CLK	18	D
9	Q_B	19	C
10	GND	20	V_{CC}

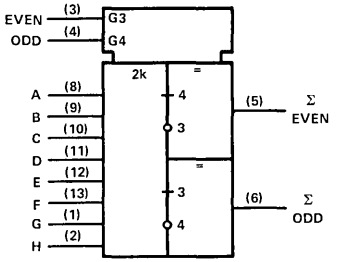
180

9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS
typical performance

TYPE	POWER	DELAY
'180	170 mW	35 ns

SN54180 (J,FH) SN74180 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	G	8	A
2	H	9	B
3	EVEN	10	C
4	ODD	11	D
5	ΣEVEN	12	E
6	ΣODD	13	F
7	GND	14	V_{CC}

FH PACKAGE			
1	nc	11	nc
2	G	12	A
3	H	13	B
4	EVEN	14	C
5	nc	15	nc
6	ODD	16	D
7	nc	17	nc
8	ΣEVEN	18	E
9	ΣODD	19	F
10	GND	20	V_{CC}

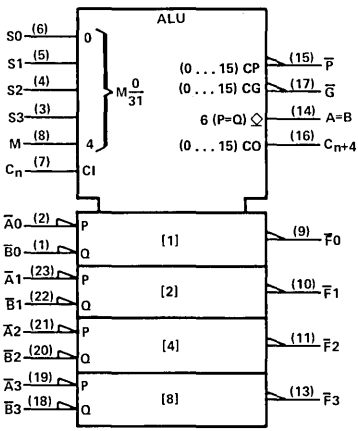
181

ARITHMETIC LOGIC UNITS/ FUNCTION GENERATORS
(16 arithmetic operations, 16 logic functions)
typical performance

TYPE	CARRY TIME	ADD TIME	TOTAL POWER
'181	12.5 ns	24 ns	455 mW
'AS181A	6 ns	5 ns	675 mW
'LS181	16 ns	24 ns	102 mW
'S181	7 ns	11 ns	600 mW

SN54181 (J,FH) SN74181 (J,N)
SN54AS181A (J,FH) SN74AS181A (N,FN)
SN54LS181 (J,FH) SN74LS181 (J,N,FN)
SN54S181 (J,FH) SN74S181 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	$\overline{B}0$	13	$\overline{F}3$
2	$\overline{A}0$	14	A=B
3	S3	15	$\overline{P}$
4	S2	16	C_{n+4}
5	S1	17	$\overline{G}$
6	S0	18	$\overline{B}3$
7	C_n	19	$\overline{A}3$
8	M	20	$\overline{B}2$
9	$\overline{F}0$	21	$\overline{A}2$
10	$\overline{F}1$	22	$\overline{B}1$
11	$\overline{F}2$	23	$\overline{A}1$
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	$\overline{B}0$	16	$\overline{F}3$
3	$\overline{A}0$	17	A=B
4	S3	18	$\overline{P}$
5	S2	19	C_{n+4}
6	S1	20	$\overline{G}$
7	S0	21	$\overline{B}3$
8	nc	22	nc
9	C_n	23	$\overline{A}3$
10	M	24	$\overline{B}2$
11	$\overline{F}0$	25	$\overline{A}2$
12	$\overline{F}1$	26	$\overline{B}1$
13	$\overline{F}2$	27	$\overline{A}1$
14	GND	28	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

182

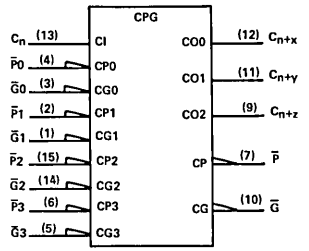
LOOK-AHEAD CARRY GENERATORS

typical performance

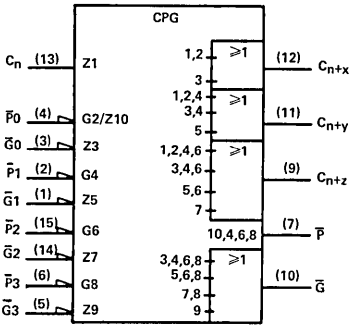
TYPE	POWER	CARRY TIME
'182	180 mW	13 ns
'S182	260 mW	7 ns

SN54182 (J,FH) SN74182 (J,N)
SN54S182 (J,FH) SN74S182 (J,N,FN)

logic symbols†



OR



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	G1	9	Cn+z	1	nc	11	nc
2	P1	10	G	2	G1	12	Cn+z
3	G0	11	Cn+y	3	P1	13	G
4	P0	12	Cn+x	4	G0	14	Cn+y
5	G3	13	Cn	5	P0	15	Cn+x
6	P3	14	G2	6	nc	16	nc
7	P	15	P2	7	G3	17	Cn
8	GND	16	VCC	8	P3	18	G2
				9	P	19	P2
				10	GND	20	VCC

183

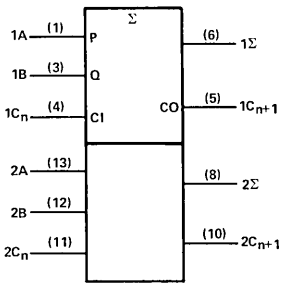
DUAL CARRY-SAVE FULL ADDERS

typical performance

TYPE	CARRY TIME	ADD TIME	POWER PER BIT
'H183	11 ns	11 ns	110 mW
'LS183	15 ns	15 ns	23 mW

SN54H183 (J,FH) SN74H183 (J,N)
SN54LS183 (J,FH) SN74LS183 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	2Σ	1	nc	11	nc
2	nc	9	nc	2	1A	12	2Σ
3	1B	10	2Cn+1	3	nc	13	nc
4	1Cn	11	2Cn	4	1B	14	2Cn+1
5	1Cn+1	12	2B	5	nc	15	nc
6	1Σ	13	2A	6	1Cn	16	2Cn
7	GND	14	VCC	7	nc	17	nc
				8	1Cn+1	18	2B
				9	1Σ	19	2A
				10	GND	20	VCC

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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184

CODE CONVERTERS

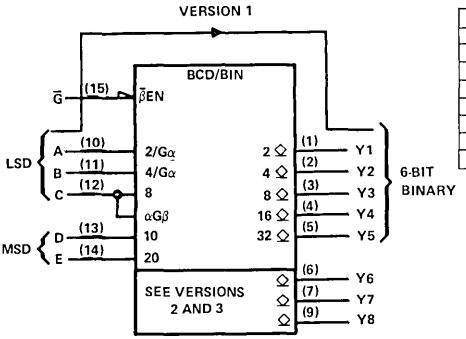
(BCD to binary)

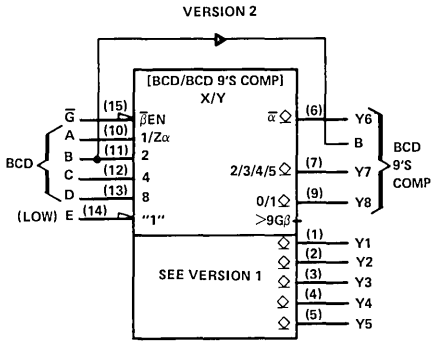
typical performance

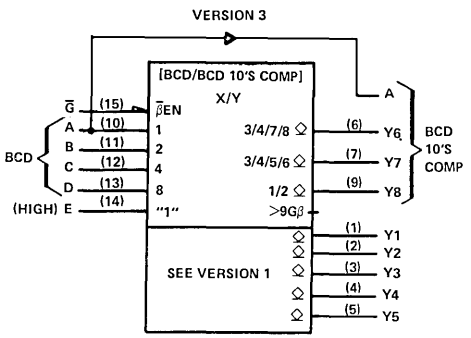
TYPE	POWER	DELAY
'184	280 mW	25 ns

SN54184 (J,FH) SN74184 (J,N)

logic symbols†







pin assignments

J, N PACKAGES				FH PACKAGE			
1	Y1	9	Y8	1	nc	11	nc
2	Y2	10	A	2	Y1	12	Y8
3	Y3	11	B	3	Y2	13	A
4	Y4	12	C	4	Y3	14	B
5	Y5	13	D	5	Y4	15	C
6	Y6	14	E	6	nc	16	nc
7	Y7	15	$\overline{G}$	7	Y5	17	D
8	GND	16	V_{CC}	8	Y6	18	E
				9	Y7	19	$\overline{G}$
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

185

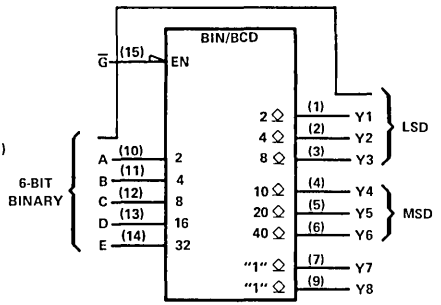
CODE CONVERTERS
(binary to BCD)

typical performance

TYPE	POWER	DELAY
'185A	280 mW	25 ns

SN54185A (J,FH) SN74185A (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	Y1	9	Y8	1	nc	11	nc
2	Y2	10	A	2	Y1	12	Y8
3	Y3	11	B	3	Y2	13	A
4	Y4	12	C	4	Y3	14	B
5	Y5	13	D	5	Y4	15	C
6	Y6	14	E	6	nc	16	nc
7	Y7	15	$\overline{G}$	7	Y5	17	D
8	GND	16	V_{CC}	8	Y6	18	E
				9	Y7	19	$\overline{G}$
				10	GND	20	V_{CC}

187

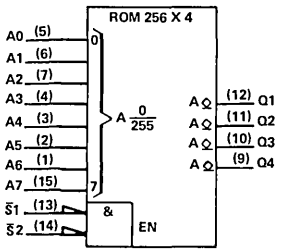
1024-BIT READ-ONLY MEMORIES
(256 4-bit words; open-collector outputs)

typical performance

TYPE	ACCESS TIMES	
	CHIP-SELECT	ADDRESS
'187	20 ns	40 ns

SN54187 (J,FH) SN74187 (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	A6	9	Q4	1	nc	11	nc
2	A5	10	Q3	2	A6	12	Q4
3	A4	11	Q2	3	A5	13	Q3
4	A3	12	Q1	4	A4	14	Q2
5	A0	13	$\overline{S}$1	5	A3	15	Q1
6	A1	14	$\overline{S}$2	6	nc	16	nc
7	A2	15	A7	7	A0	17	$\overline{S}$1
8	GND	16	V_{CC}	8	A1	18	$\overline{S}$2
				9	A2	19	A7
				10	GND	20	V_{CC}

188

256-BIT PROGRAMMABLE READ-ONLY MEMORIES

(This number has been changed to TBP18SA030. Product Guide information for this TTL circuit can be found at the end of this section.)

189

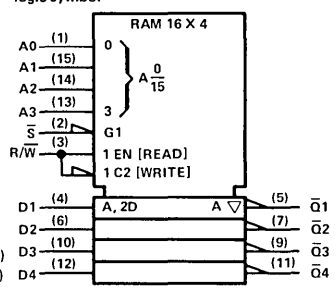
64-BIT RANDOM-ACCESS MEMORIES
(16 4-bit words; three-state outputs)

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER PER BIT
'LS189A	50 ns	35 ns	2.7 mW
'S189A	25 ns	12 ns	5.9 mW

SN54LS189A (J,FH) SN74LS189A (J,N,FN)
SN54S189A (J,FH) SN74S189A (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A0	9	$\overline{Q}$3	1	nc	11	nc
2	$\overline{S}$	10	D3	2	A0	12	$\overline{Q}$3
3	R/$\overline{W}$	11	$\overline{Q}$4	3	$\overline{S}$	13	D3
4	D1	12	D4	4	R/$\overline{W}$	14	$\overline{Q}$4
5	$\overline{Q}$1	13	A3	5	D1	15	D4
6	D2	14	A2	6	nc	16	nc
7	$\overline{Q}$2	15	A1	7	$\overline{Q}$1	17	A3
8	GND	16	V_{CC}	8	D2	18	A2
				9	$\overline{Q}$2	19	A1
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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190

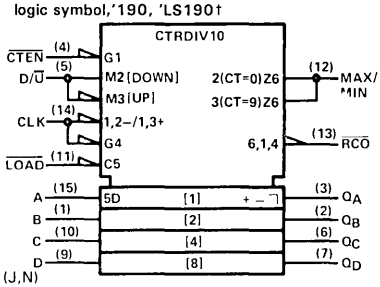
SYNCHRONOUS UP/DOWN COUNTERS (BCD)

typical performance

TYPE	COUNT FREQ	TOTAL POWER
'190	20 MHz	325 mW
'ALS190	35 MHz	60 mW
'LS190	20 MHz	100 mW

SN54190 (J,FH) SN74190 (J,N)
SN54ALS190 (J,FH) SN74ALS190 (N,FN)
SN54LS190 (J,FH) SN74LS190 (J,N,FN)

logic symbol,'190, 'LS190†

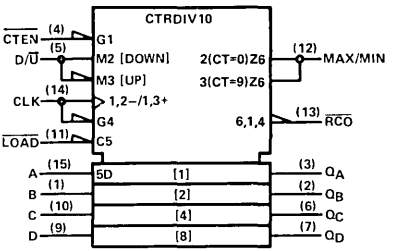


pin assignments

J, N PACKAGES			
1	B	9	D
2	Q_B	10	C
3	Q_A	11	$\overline{LOAD}$
4	$\overline{CTEN}$	12	MAX/MIN
5	$D/\overline{U}$	13	$\overline{RCO}$
6	Q_C	14	CLK
7	Q_D	15	A
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	B	12	D
3	Q_B	13	C
4	Q_A	14	$\overline{LOAD}$
5	$\overline{CTEN}$	15	MAX/MIN
6	nc	16	nc
7	$D/\overline{U}$	17	$\overline{RCO}$
8	Q_C	18	CLK
9	Q_D	19	A
10	GND	20	V_{CC}

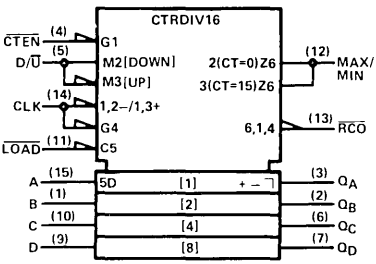
logic symbol, 'ALS190†



191

SYNCHRONOUS UP/DOWN COUNTERS (binary)

logic symbol,'191, 'LS191†



pin assignments

J, N PACKAGES			
1	B	9	D
2	Q_B	10	C
3	Q_A	11	$\overline{LOAD}$
4	$\overline{CTEN}$	12	MAX/MIN
5	$D/\overline{U}$	13	$\overline{RCO}$
6	Q_C	14	CLK
7	Q_D	15	A
8	GND	16	V_{CC}

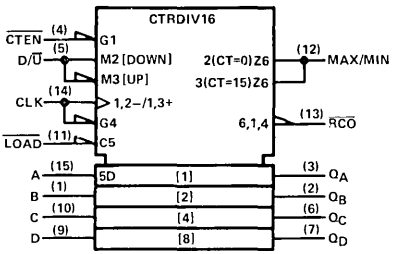
FH, FN PACKAGES			
1	nc	11	nc
2	B	12	D
3	Q_B	13	C
4	Q_A	14	$\overline{LOAD}$
5	$\overline{CTEN}$	15	MAX/MIN
6	nc	16	nc
7	$D/\overline{U}$	17	$\overline{RCO}$
8	Q_C	18	CLK
9	Q_D	19	A
10	GND	20	V_{CC}

typical performance

TYPE	COUNT FREQ	TOTAL POWER
'191	20 MHz	325 mW
'ALS191	35 MHz	60 mW
'LS191	20 MHz	90 mW

SN54191 (J,FH) SN74191 (J,N)
SN54ALS191 (J,FH) SN74ALS191 (N,FN)
SN54LS191 (J,FH) SN74LS191 (J,N,FN)

logic symbol, 'ALS191†



† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

192

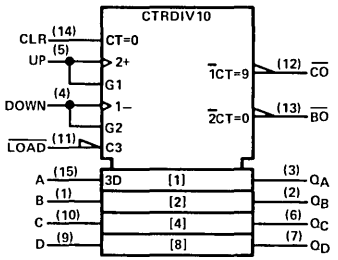
SYNCHRONOUS UP/DOWN DUAL CLOCK COUNTERS
(BCD with clear)

typical performance

TYPE	COUNT FREQ	TOTAL POWER
'192	25 MHz	325 mW
'ALS192	40 MHz	50 mW
'L192	3 MHz	42 mW
'LS192	25 MHz	85 mW

SN54192 (J,FH) SN74192 (J,N)
SN54L192 (J)
SN54LS192 (J,FH) SN74LS192 (J,N,FN)
SN54ALS192 (J,FH) SN74ALS192 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	B	9	D	1	nc	11	nc
2	Q_B	10	C	2	B	12	D
3	Q_A	11	$\overline{LOAD}$	3	Q_B	13	C
4	DOWN	12	CO	4	Q_A	14	$\overline{LOAD}$
5	UP	13	$\overline{BO}$	5	DOWN	15	CO
6	Q_C	14	CLR	6	nc	16	nc
7	Q_D	15	A	7	UP	17	$\overline{BO}$
8	GND	16	V_{CC}	8	Q_C	18	CLR
				9	Q_D	19	A
				10	GND	20	V_{CC}

193

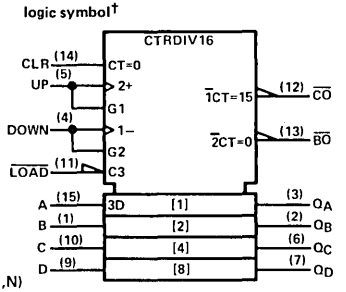
SYNCHRONOUS UP/DOWN DUAL CLOCK COUNTERS
(binary with clear)

typical performance

TYPE	COUNT FREQ	TOTAL POWER
'193	25 MHz	325 mW
'ALS193	40 MHz	50 mW
'L193	3 MHz	42 mW
'LS193	25 MHz	85 mW

SN54193 (J,FH) SN74193 (J,N)
SN54L193 (J)
SN54LS193 (J,FH) SN74LS193 (J,N,FN)
SN54ALS193 (J,FH) SN74ALS193 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	B	9	D	1	nc	11	nc
2	Q_B	10	C	2	B	12	D
3	Q_A	11	$\overline{LOAD}$	3	Q_B	13	C
4	DOWN	12	$\overline{CO}$	4	Q_A	14	$\overline{LOAD}$
5	UP	13	$\overline{BO}$	5	DOWN	15	$\overline{CO}$
6	Q_C	14	CLR	6	nc	16	nc
7	Q_D	15	A	7	UP	17	$\overline{BO}$
8	GND	16	V_{CC}	8	Q_C	18	CLR
				9	Q_D	19	A
				10	GND	20	V_{CC}

194

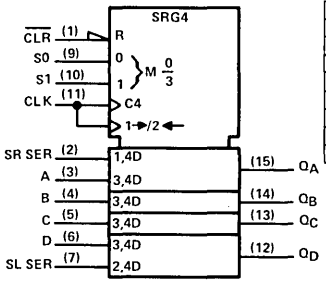
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	TOTAL POWER
'194	25 MHz	D	195 mW
'LS194A	25 MHz	D	75 mW
'S194	70 MHz	D	450 mW

SN54194 (J,FH) SN74194 (J,N,FN)
SN54LS194A (J,FH) SN74LS194A (J,N,FN)
SN54S194 (J,FH) SN74S194 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{CLR}$	9	S0	1	nc	11	nc
2	SR SER	10	S1	2	$\overline{CLR}$	12	S0
3	A	11	CLK	3	SR SER	13	S1
4	B	12	Q_D	4	A	14	CLK
5	C	13	Q_C	5	B	15	Q_D
6	D	14	Q_B	6	nc	16	nc
7	SL SER	15	Q_A	7	C	17	Q_C
8	GND	16	V_{CC}	8	D	18	Q_B
				9	SL SER	19	Q_A
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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195

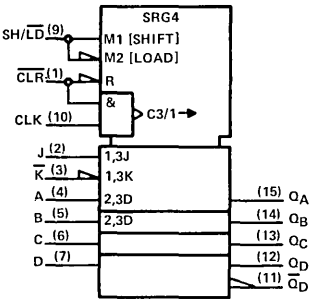
4-BIT PARALLEL-ACCESS SHIFT REGISTERS

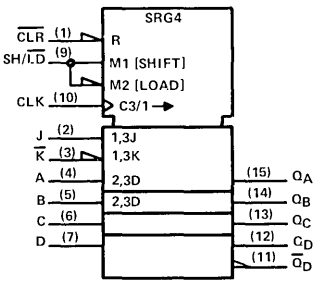
typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	TOTAL POWER
'195	30 MHz	J-$\overline{K}$	195 mW
'LS195A	30 MHz	J-$\overline{K}$	70 mW
'S195	70 MHz	J-$\overline{K}$	375 mW

SN54195 (J,FH) SN74195 (J,N)
SN54LS195A (J,FH) SN74LS195A (J,N,FN)
SN54S195 (J,FH) SN74S195 (J,N,FN)

logic symbol, '195†





pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{CLR}$	9	SH/$\overline{LD}$	1	nc	11	nc
2	J	10	CLK	2	$\overline{CLR}$	12	SH/$\overline{LD}$
3	$\overline{K}$	11	$\overline{Q}_D$	3	J	13	CLK
4	A	12	Q_D	4	$\overline{K}$	14	$\overline{Q}_D$
5	B	13	Q_C	5	A	15	Q_D
6	C	14	Q_B	6	nc	16	nc
7	D	15	Q_A	7	B	17	Q_C
8	GND	16	V_{CC}	8	C	18	Q_B
				9	D	19	Q_A
				10	GND	20	V_{CC}

196

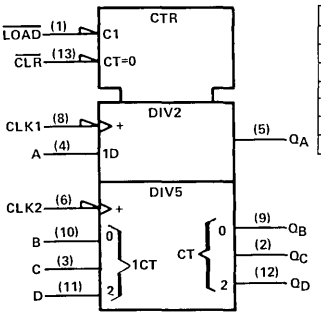
PRESETTABLE DECADE/ BIQUINARY COUNTERS/ LATCHES

typical performance

TYPE	COUNT FREQ	PARALLEL LOAD	CLEAR	TOTAL POWER
'196	50 MHz	YES	LOW	240 mW
'LS196	30 MHz	YES	LOW	60 mW
'S196	100 MHz	YES	LOW	375 mW

SN54196 (J,FH) SN74196 (J,N)
SN54LS196 (J,FH) SN74LS196 (J,N,FN)
SN54S196 (J,FH) SN74S196 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{LOAD}$	8	CLK1	1	nc	11	nc
2	Q_C	9	Q_B	2	$\overline{LOAD}$	12	CLK1
3	C	10	B	3	Q_C	13	Q_B
4	A	11	D	4	C	14	B
5	Q_A	12	Q_D	5	nc	15	nc
6	CLK2	13	$\overline{CLR}$	6	A	16	D
7	GND	14	V_{CC}	7	nc	17	nc
				8	Q_A	18	Q_D
				9	CLK2	19	$\overline{CLR}$
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc -- no internal connection.

197

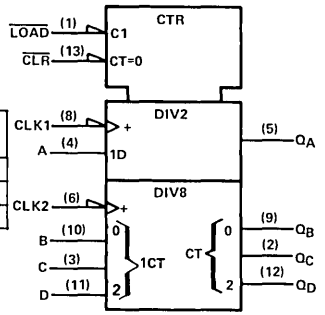
PRESETTABLE BINARY COUNTERS/LATCHES

typical performance

TYPE	COUNT FREQ	PARALLEL LOAD	CLEAR	TOTAL POWER
'197	50 MHz	YES	LOW	240 mW
'LS197	30 MHz	YES	LOW	60 mW
'S197	100 MHz	YES	LOW	375 mW

SN54197 (J,FH) SN74197 (J,N)
SN54LS197 (J,FH) SN74LS197 (J,N,FN)
SN54S197 (J,FH) SN74S197 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	$\overline{LOAD}$	8	CLK1
2	Q_C	9	Q_B
3	C	10	B
4	A	11	D
5	Q_A	12	Q_D
6	CLK2	13	$\overline{CLR}$
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	$\overline{LOAD}$	12	CLK1
3	Q_C	13	Q_B
4	C	14	B
5	nc	15	nc
6	A	16	D
7	nc	17	nc
8	Q_A	18	Q_D
9	CLK2	19	$\overline{CLR}$
10	GND	20	V_{CC}

198

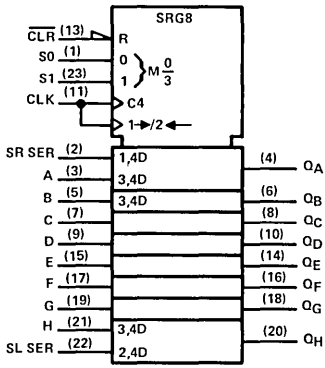
8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'198	25 MHz	D	LOW	360 mW

SN54198 (J,FH) SN74198 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	S0	13	$\overline{CLR}$
2	SR SER	14	Q_E
3	A	15	E
4	Q_A	16	Q_F
5	B	17	F
6	Q_B	18	Q_G
7	C	19	G
8	Q_C	20	Q_H
9	D	21	H
10	Q_D	22	SL SER
11	CLK	23	S1
12	GND	24	V_{CC}

FH PACKAGE			
1	nc	15	nc
2	S0	16	$\overline{CLR}$
3	SR SER	17	Q_E
4	A	18	E
5	Q_A	19	Q_F
6	B	20	F
7	Q_B	21	Q_G
8	nc	22	nc
9	C	23	G
10	Q_C	24	Q_H
11	D	25	H
12	Q_D	26	SL SER
13	CLK	27	S1
14	GND	28	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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199

8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

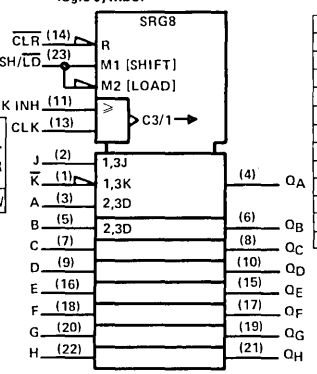
(J-$\overline{K}$ serial inputs)

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'199	25 MHz	J-$\overline{K}$	LOW	360 mW

SN54199 (J,FH) SN74199 (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	$\overline{K}$	13	CLK	1	nc	15	nc
2	J	14	$\overline{CLR}$	2	$\overline{K}$	16	CLK
3	A	15	Q_E	3	J	17	$\overline{CLR}$
4	Q_A	16	E	4	A	18	Q_E
5	B	17	Q_F	5	Q_A	19	E
6	Q_B	18	F	6	B	20	Q_F
7	C	19	Q_G	7	Q_B	21	F
8	Q_C	20	G	8	nc	22	nc
9	D	21	Q_H	9	C	23	Q_G
10	Q_D	22	H	10	Q_C	24	G
11	CLK INH	23	$SH/\overline{LD}$	11	D	25	Q_H
12	GND	24	V_{CC}	12	Q_D	26	H
				13	CLK INH	27	$SH/\overline{LD}$
				14	GND	28	V_{CC}

201

256-BIT RANDOM-ACCESS MEMORIES

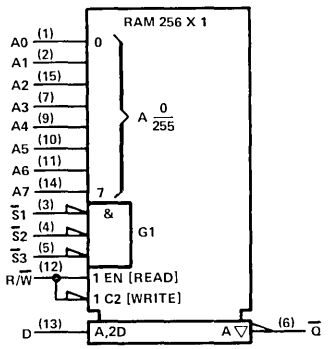
(256 1-bit words; three-state output)

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER/ BIT
'S201	42 ns	17 ns	1.9 mW

SN74S201 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	A0	9	A4
2	A1	10	A5
3	$\overline{S}1$	11	A6
4	$\overline{S}2$	12	R/$\overline{W}$
5	$\overline{S}3$	13	D
6	$\overline{Q}$	14	A7
7	A3	15	A2
8	GND	16	V_{CC}

217

256-BIT RANDOM-ACCESS MEMORIES WITH THREE-STATE OUTPUTS

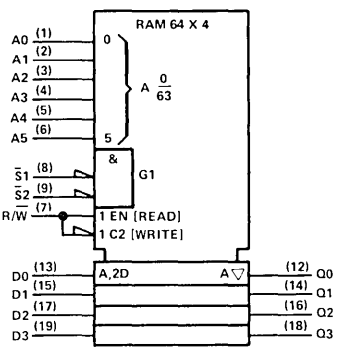
(64 words of 4 bits each)

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER/ BIT
'ALS217	30 ns	20 ns	0.9 mW

SN54ALS217 (J,FH) SN74ALS217 (N, FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A0	11	nc	1	A0	11	nc
2	A1	12	Q0	2	A1	12	Q0
3	A2	13	D0	3	A2	13	D0
4	A3	14	Q1	4	A3	14	Q1
5	A4	15	D1	5	A4	15	D1
6	A5	16	Q2	6	A5	16	Q2
7	R/$\overline{W}$	17	D2	7	R/$\overline{W}$	17	D2
8	$\overline{S}1$	18	Q3	8	$\overline{S}1$	18	Q3
9	$\overline{S}2$	19	D3	9	$\overline{S}2$	19	D3
10	GND	20	V_{CC}	10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

218

256-BIT RANDOM-ACCESS READ/WRITE MEMORIES WITH THREE-STATE OUTPUTS

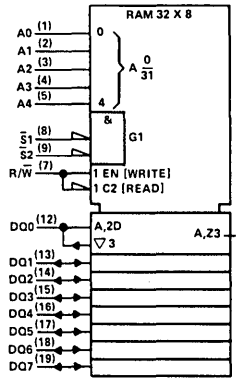
(32 words of 8 bits each)

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER/ BIT
'ALS218	30 ns	20 ns	0.9 mW

SN54ALS218 (J,FH) SN74ALS218 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A0	11	nc	1	A0	11	nc
2	A1	12	DQ0	2	A1	12	DQ0
3	A2	13	DQ1	3	A2	13	DQ1
4	A3	14	DQ2	4	A3	14	DQ2
5	A4	15	DQ3	5	A4	15	DQ3
6	nc	16	DQ4	6	nc	16	DQ4
7	R/W	17	DQ5	7	R/W	17	DQ5
8	S1	18	DQ6	8	S1	18	DQ6
9	S2	19	DQ7	9	S2	19	DQ7
10	GND	20	VCC	10	GND	20	VCC

219

64-BIT RANDOM-ACCESS MEMORIES

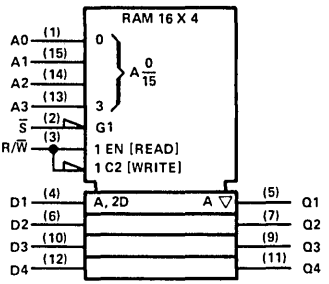
(16 words of 4 bits each; three-state non-inverting output)

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER/ BIT
'LS219A	50 ns	35 ns	2.7 mW

SN54LS219A (J,FH) SN74LS219A (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A0	9	Q3	1	nc	11	nc
2	S	10	D3	2	A0	12	Q3
3	R/W	11	Q4	3	S	13	D3
4	D1	12	D4	4	R/W	14	Q4
5	Q1	13	A3	5	D1	15	D4
6	D2	14	A2	6	nc	16	nc
7	Q2	15	A1	7	Q1	17	A3
8	GND	16	VCC	8	D2	18	A2
				9	Q2	19	A1
				10	GND	20	VCC

221

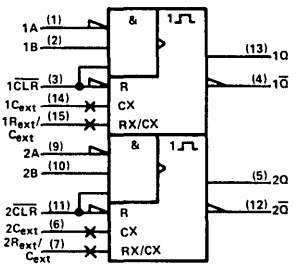
DUAL MONOSTABLE MULTIVIBRATORS

typical performance

TYPE	OUTPUT PULSE RANGE	TOTAL POWER
SN54221	20 ns - 21s	130 mW
SN74221	20 ns - 28s	130 mW
SN54LS221	20 ns - 49s	23 mW
SN74LS221	20 ns - 70 s	23 mW

SN54221 (J,FH) SN74221 (J,N)
SN54LS221 (J,FH) SN74LS221 (J,N,FN)

logic symbol†



pin assignments

J,N PACKAGES				FH, FN PACKAGES			
1	1A	9	2A	1	nc	11	nc
2	1B	10	2B	2	1A	12	2A
3	1CLR	11	2CLR	3	1B	13	2B
4	1Q	12	2Q	4	1CLR	14	2CLR
5	2Q	13	1Q	5	1Q	15	2Q
6	2Cext	14	1Cext	6	nc	16	nc
7	2Rext/Cext	15	1Rext/Cext	7	2Q	17	1Q
8	GND	16	VCC	8	2Cext	18	1Cext
				9	2Rext/Cext	19	1Rext/Cext
				10	GND	20	VCC

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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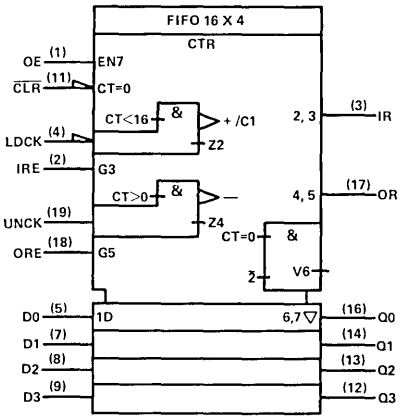
222

64-BIT FIFO MEMORIES
16 4-BIT WORDS
(input-ready enable, output-ready enable, and three-state output)
typical performance

TYPE	DELAY TIME FROM CLOCK	TOTAL POWER
'LS222	47 ns	433 mW

SN54LS222 (J) SN74LS222 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	OE	11	CLR
2	IRE	12	Q3
3	IR	13	Q2
4	LDCK	14	Q1
5	D0	15	nc
6	nc	16	Q0
7	D1	17	OR
8	D2	18	ORE
9	D3	19	UNCK
10	GND	20	V_{CC}

For chip carrier information, contact the factory.

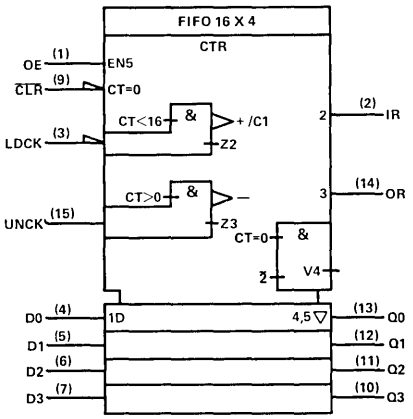
224

64-BIT FIFO MEMORIES
16 4-BIT WORDS
(three-state output)
typical performance

TYPE	DELAY TIME FROM CLOCK	TOTAL POWER
'LS224	47 ns	433 mW

SN54LS224 (J) SN74LS224 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	OE	9	CLR
2	IR	10	Q3
3	LDCK	11	Q2
4	D0	12	Q1
5	D1	13	Q0
6	D2	14	OR
7	D3	15	UNCK
8	GND	16	V_{CC}

For chip carrier information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

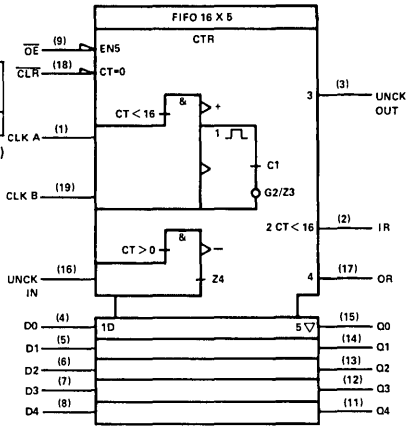
225

80-BIT FIFO MEMORIES
16 5-BIT WORDS
typical performance

OUTPUT	DELAY TIME FROM CLOCK	TOTAL POWER
3-State	50 ns	400 mW

SN74S225 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	CLK A	11	Q4
2	IR	12	Q3
3	UNCK OUT	13	Q2
4	D0	14	Q1
5	D1	15	Q0
6	D2	16	UNCK IN
7	D3	17	OR
8	D4	18	$\overline{CLR}$
9	$\overline{OE}$	19	CLK B
10	GND	20	V_{CC}

FN PACKAGES			
1	CLK A	11	Q4
2	IR	12	Q3
3	UNCK OUT	13	Q2
4	D0	14	Q1
5	D1	15	Q0
6	D2	16	UNCK IN
7	D3	17	OR
8	D4	18	$\overline{CLR}$
9	$\overline{OE}$	19	CLK B
10	GND	20	V_{CC}

6

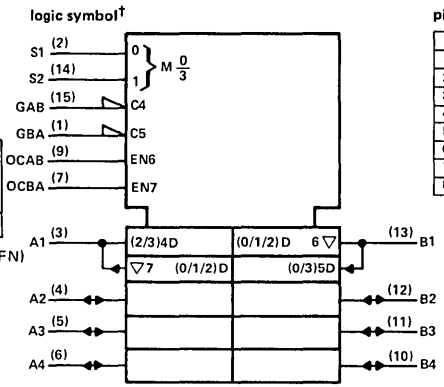
226

4-BIT PARALLEL LATCHED
BUS TRANSCEIVERS
(three-state outputs)
typical performance

TYPE	MAX SOURCE CURRENT	MAX SINK CURRENT
'S226	−6.5 mA	20 mA

SN54S226 (J,FH) SN74S226 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	GBA	9	OCAB	1	nc	11	nc
2	S1	10	B4	2	GBA	12	OCAB
3	A1	11	B3	3	S1	13	B4
4	A2	12	B2	4	A1	14	B3
5	A3	13	B1	5	A2	15	B2
6	A4	14	S2	6	nc	16	nc
7	OCBA	15	GAB	7	A3	17	B1
8	GND	16	V_{CC}	8	A4	18	S2
				9	OCBA	19	GAB
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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227

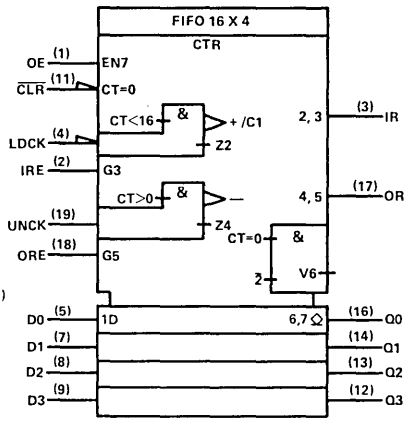
64-BIT FIFO MEMORIES
16 4-BIT WORDS
(input-ready enable, output-ready enable, open-collector outputs)

typical performance

TYPE	DELAY TIME FROM CLOCK	TOTAL POWER
'LS227	57.5 ns	433 mW

SN54LS227 (J) SN74LS227 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	OE	11	$\overline{CLR}$
2	IRE	12	Q3
3	IR	13	Q2
4	LDCK	14	Q1
5	D0	15	nc
6	nc	16	Q0
7	D1	17	OR
8	D2	18	ORE
9	D3	19	UNCK
10	GND	20	V_{CC}

For chip carrier information, contact the factory.

228

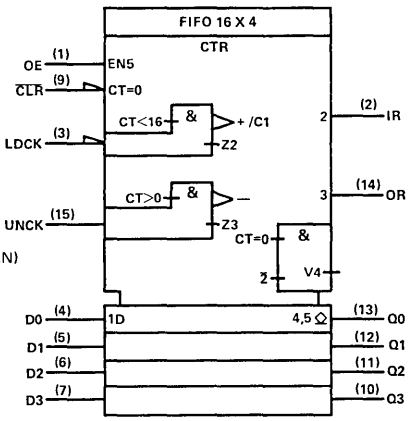
64-BIT FIFO MEMORIES
16 4-BIT WORDS
(open-collector outputs)

typical performance

TYPE	DELAY TIME FROM CLOCK	TOTAL POWER
'LS228	57.5 ns	433 mW

SN54LS228 (J) SN74LS228 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	OE	9	$\overline{CLR}$
2	IR	10	Q3
3	LDCK	11	Q2
4	D0	12	Q1
5	D1	13	Q0
6	D2	14	OR
7	D3	15	UNCK
8	GND	16	V_{CC}

For chip carrier information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

230,231

OCTAL BUFFERS AND LINE DRIVERS
(three-state outputs)

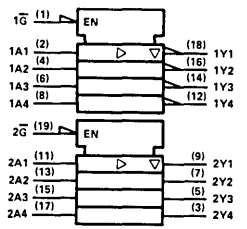
- 'AS230 has true and complementary outputs
- 'AS231 has complementary G and $\overline{G}$ inputs

typical performance

DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
3.5 ns	−15 mA	64 mA

SN54AS230 (J,FH) SN74AS230 (N,FN)
SN54AS231 (J,FH) SN74AS231 (N,FN)

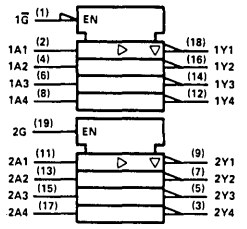
logic symbol, 'AS230†



pin assignments

J, N PACKAGES			
1	1G̅	11	2A1
2	1A1	12	1Y4
3	2Y4	13	2A2
4	1A2	14	1Y3
5	2Y3	15	2A3
6	1A3	16	1Y2
7	2Y2	17	2A4
8	1A4	18	1Y1
9	2Y1	19	2G̅
10	GND	20	V_{CC}

logic symbol, 'AS231†



FH, FN PACKAGES			
1	1G̅	11	2A1
2	1A1	12	1Y4
3	2Y4	13	2A2
4	1A2	14	1Y3
5	2Y3	15	2A3
6	1A3	16	1Y2
7	2Y2	17	2A4
8	1A4	18	1Y1
9	2Y1	19	2G̅
10	GND	20	V_{CC}

*2G on 'AS231

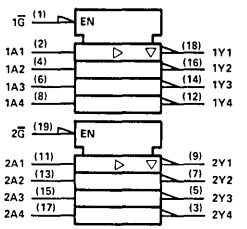
240

OCTAL BUFFERS/LINE
DRIVERS/LINE RECEIVERS
(inverted three-state outputs)
typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSIPATION
SN54ALS240	5.5 ns	−12 mA	12 mA	52 mW
SN74ALS240	5.5 ns	−15 mA	24 mA	
SN74ALS240-1	5.5 ns	−15 mA	48 mA	
SN54AS240	3.5 ns	−12 mA	48 mA	235 mW
SN74AS240	3.5 ns	−15 mA	64 mA	
SN54LS240	10 ns	−12 mA	12 mA	120 mW
SN74LS240	10 ns	−15 mA	24 mA	
SN54S240	5 ns	−12 mA	48 mA	467 mW
SN74S240	5 ns	−15 mA	64 mA	

SN54ALS240 (J,FH) SN74ALS240 (N,FN)
SN74ALS240-1 (N,FN)
SN54AS240 (J,FH) SN74AS240 (N,FN)
SN54LS240 (J,FH) SN74LS240 (J,N,FN)
SN54S240 (J,FH) SN74S240 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	1G̅	11	2A1
2	1A1	12	1Y4
3	2Y4	13	2A2
4	1A2	14	1Y3
5	2Y3	15	2A3
6	1A3	16	1Y2
7	2Y2	17	2A4
8	1A4	18	1Y1
9	2Y1	19	2G̅
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	1G̅	11	2A1
2	1A1	12	1Y4
3	2Y4	13	2A2
4	1A2	14	1Y3
5	2Y3	15	2A3
6	1A3	16	1Y2
7	2Y2	17	2A4
8	1A4	18	1Y1
9	2Y1	19	2G̅
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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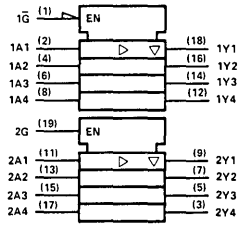
241

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS
(non-inverted three-state outputs)
typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSIPATION
SN54ALS241	7 ns	−12 mA	12 mA	68 mW
SN74ALS241	7 ns	−15 mA	24 mA	
SN74ALS241-1	7 ns	−15 mA	48 mA	
SN54AS241	4 ns	−12 mA	48 mA	
SN74AS241	4 ns	−15 mA	64 mA	
SN54LS241	10 ns	−12 mA	12 mA	127 mW
SN74LS241	10 ns	−15 mA	24 mA	
SN54S241	5 ns	−12 mA	48 mA	558 mW
SN74S241	5 ns	−15 mA	64 mA	

SN54ALS241 (J,FH) SN74ALS241 (N,FN)
SN74ALS241-1 (N,FN)
SN54AS241 (J,FH) SN74AS241 (N,FN)
SN54LS241 (J,FH) SN74LS241 (J,N,FN)
SN54S241 (J,FH) SN74S241 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	1G̅	11	2A1
2	1A1	12	1Y4
3	2Y4	13	2A2
4	1A2	14	1Y3
5	2Y3	15	2A3
6	1A3	16	1Y2
7	2Y2	17	2A4
8	1A4	18	1Y1
9	2Y1	19	2G̅
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	1G̅	11	2A1
2	1A1	12	1Y4
3	2Y4	13	2A2
4	1A2	14	1Y3
5	2Y3	15	2A3
6	1A3	16	1Y2
7	2Y2	17	2A4
8	1A4	18	1Y1
9	2Y1	19	2G̅
10	GND	20	V_{CC}

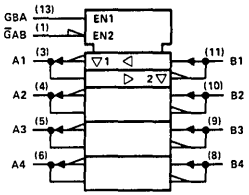
242

QUADRUPLE BUS TRANSCEIVERS
(inverted three-state outputs)
typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSIPATION
SN54ALS242	6 ns	−12 mA	12 mA	68 mW
SN74ALS242	6 ns	−15 mA	24 mA	
SN74ALS242-1	6 ns	−15 mA	48 mA	
SN54AS242	3.5 ns	−12 mA	48 mA	
SN74AS242	3.5 ns	−15 mA	64 mA	
SN54LS242	11 ns	−12 mA	12 mA	133 mW
SN74LS242	11 ns	−15 mA	24 mA	

SN54ALS242 (J,FH) SN74ALS242 (N,FN)
SN74ALS242-1 (N,FN)
SN54AS242 (J,FH) SN74AS242 (N,FN)
SN54LS242 (J,FH) SN74LS242 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	GAB̅	8	B4
2	nc	9	B3
3	A1	10	B2
4	A2	11	B1
5	A3	12	nc
6	A4	13	GBA
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	GAB̅	12	B4
3	nc	13	B3
4	A1	14	B2
5	nc	15	nc
6	A2	16	B1
7	nc	17	nc
8	A3	18	nc
9	A4	19	GBA
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

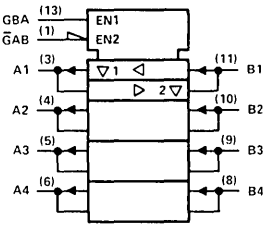
243

QUADRUPLE BUS TRANSCEIVERS
(non-inverted three-state outputs)
typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSIPATION
SN54ALS243	8 ns	−12 mA	12 mA	93 mW
SN74ALS243	8 ns	−15 mA	24 mA	
SN74ALS243-1	8 ns	−15 mA	48 mA	
SN54AS243	4.5 ns	−12 mA	48 mA	
SN74AS243	4.5 ns	−15 mA	64 mA	
SN54LS243	12 ns	−12 mA	12 mA	138 mW
SN74LS243	12 ns	−15 mA	24 mA	

SN54ALS243 (J,FH) SN74ALS243 (N,FN)
SN74ALS243-1 (N,FN)
SN54AS243 (J,FH) SN74AS243 (N,FN)
SN54LS243 (J,FH) SN74LS243 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	GAB	8	B4
2	nc	9	B3
3	A1	10	B2
4	A2	11	B1
5	A3	12	nc
6	A4	13	GBA
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	GAB	12	B4
3	nc	13	B3
4	A1	14	B2
5	nc	15	nc
6	A2	16	B1
7	nc	17	nc
8	A3	18	nc
9	A4	19	GBA
10	GND	20	V_{CC}

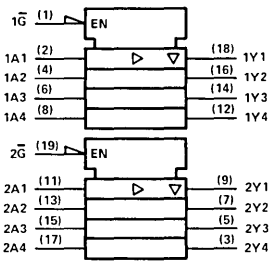
244

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS
(non-inverted three-state outputs)
typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSIPATION
SN54ALS244	7 ns	−12 mA	12 mA	68 mW
SN74ALS244	7 ns	−15 mA	24 mA	
SN74ALS244-1	7 ns	−15 mA	48 mA	
SN54AS244	4.5 ns	−12 mA	48 mA	235 mW
SN74AS244	4.5 ns	−15 mA	64 mA	
SN54LS244	12 ns	−12 mA	12 mA	127 mW
SN74LS244	12 ns	−15 mA	24 mA	
SN54S244	6 ns	−12 mA	48 mA	558 mW
SN74S244	6 ns	−15 mA	64 mA	

SN54ALS244 (J,FH) SN74ALS244 (N,FN)
SNALS244-1 (N,FN)
SN54AS244 (J,FH) SN74AS244 (N,FN)
SN54LS244 (J,FH) SN74LS244 (J,N,FN)
SN54S244 (J,FH) SN74S244 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	1G	11	2A1
2	1A1	12	1Y4
3	2Y4	13	2A2
4	1A2	14	1Y3
5	2Y3	15	2A3
6	1A3	16	1Y2
7	2Y2	17	2A4
8	1A4	18	1Y1
9	2Y1	19	2G
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	1G	11	2A1
2	1A1	12	1Y4
3	2Y4	13	2A2
4	1A2	14	1Y3
5	2Y3	15	2A3
6	1A3	16	1Y2
7	2Y2	17	2A4
8	1A4	18	1Y1
9	2Y1	19	2G
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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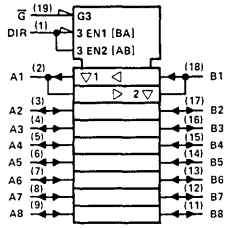
245

OCTAL BUS TRANSCEIVERS
(non-inverted three-state outputs)
typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSIPATION
SN54ALS245	6 ns	−12 mA	12 mA	173 mW
SN74ALS245	6 ns	−15 mA	24 mA	
SN74ALS245-1	6 ns	−15 mA	48 mA	
SN54LS245	8 ns	−12 mA	12 mA	290 mW
SN74LS245	8 ns	−15 mA	24 mA	

SN54ALS245 (J,FH) SN74ALS245 (N,FN)
SN74ALS245-1 (N,FN)
SN54LS245 (J,FH) SN74LS245 (J,N,FN)

logic symbol†



pin assignments

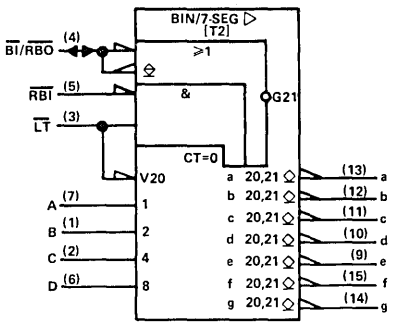
J, N PACKAGES			
1	DIR	11	B8
2	A1	12	B7
3	A2	13	B6
4	A3	14	B5
5	A4	15	B4
6	A5	16	B3
7	A6	17	B2
8	A7	18	B1
9	A8	19	$\overline{G}$
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	DIR	11	B8
2	A1	12	B7
3	A2	13	B6
4	A3	14	B5
5	A4	15	B4
6	A5	16	B3
7	A6	17	B2
8	A7	18	B1
9	A8	19	G
10	GND	20	V_{CC}

246
247

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS WITH RIPPLE BLANKING
(246-active-low, open-collector, 30-volt outputs)
(247-active-low, open-collector, 15-volt outputs)

logic symbol†



pin assignments

J, N PACKAGES			
1	B	9	e
2	C	10	d
3	$\overline{LT}$	11	c
4	$\overline{BI}/\overline{RBO}$	12	b
5	$\overline{RBI}$	13	a
6	D	14	g
7	A	15	f
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	B	12	e
3	C	13	d
4	$\overline{LT}$	14	c
5	$\overline{BI}/\overline{RBO}$	15	b
6	nc	16	nc
7	RBI	17	a
8	D	18	g
9	A	19	f
10	GND	20	V_{CC}

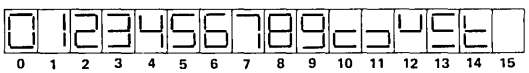
typical performance

TYPE	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TOTAL POWER
'246	40 mA	30 V	320 mW
'247	40 mA	15 V	320 mW
SN54LS247	12 mA	15 V	35 mW
SN74LS247	24 mA	15 V	35 mW

SN54246 (J,FH) SN74246 (J,N)
SN54247 (J,FH) SN74247 (J,N)
SN54LS247 (J,FH) SN74LS247 (J,N,FN)

† Pin numbers shown on logic symbols are for J and N packages only.
nc – no internal connection.

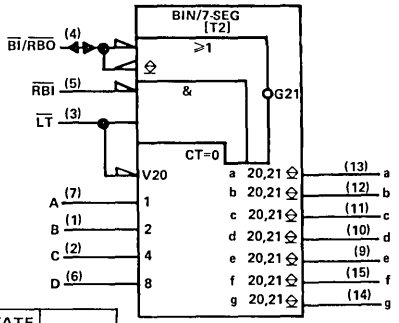
FONT TABLE T2 – RESULTANT DISPLAYS USING '246 AND '247



248

BCD-TO-SEVEN SEGMENT DECODERS/DRIVERS
(internal pull-up outputs)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	B	9	e	1	nc	11	nc
2	C	10	d	2	B	12	e
3	$\overline{LT}$	11	c	3	C	13	d
4	$\overline{BI/RBO}$	12	b	4	$\overline{LT}$	14	c
5	$\overline{RBI}$	13	a	5	$\overline{BI/RBO}$	15	b
6	D	14	g	6	nc	16	nc
7	A	15	f	7	$\overline{RBI}$	17	a
8	GND	16	V_{CC}	8	D	18	g
				9	A	19	f
				10	GND	20	V_{CC}

typical performance

TYPE	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TOTAL POWER
'248	6.4 mA	5.5 V	265 mW
SN54LS248	2 mA	5.5 V	125 mW
SN74LS248	6 mA	5.5 V	125 mW

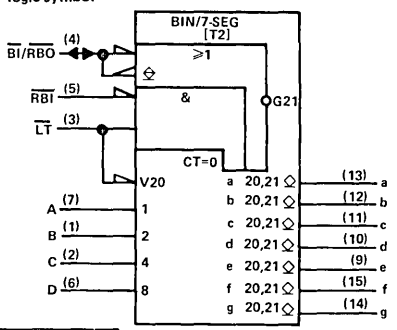
SN54248 (J,FH) SN74248 (J,N)
SN54LS248 (J,FH) SN74LS248 (J,N,FN)

6

249

BCD-TO-SEVEN SEGMENT DECODERS/DRIVERS
(open-collector outputs)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	B	9	e	1	nc	11	nc
2	C	10	d	2	B	12	e
3	$\overline{LT}$	11	c	3	C	13	d
4	$\overline{BI/RBO}$	12	b	4	$\overline{LT}$	14	c
5	$\overline{RBI}$	13	a	5	$\overline{BI/RBO}$	15	b
6	D	14	g	6	nc	16	nc
7	A	15	f	7	$\overline{RBI}$	17	a
8	GND	16	V_{CC}	8	D	18	g
				9	A	19	f
				10	GND	20	V_{CC}

typical performance

TYPE	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TOTAL POWER
'249	10 mA	5.5 V	265 mW
SN54LS249	4 mA	5.5 V	40 mW
SN74LS249	8 mA	5.5 V	40 mW

SN54249 (J,FH) SN74249 (J,N)
SN54LS249 (J,FH) SN74LS249 (J,N,FN)

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

FONT TABLE T2 — RESULTANT DISPLAYS USING '248 AND '249

TEXAS INSTRUMENTS
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251

DATA SELECTORS/ MULTIPLEXERS

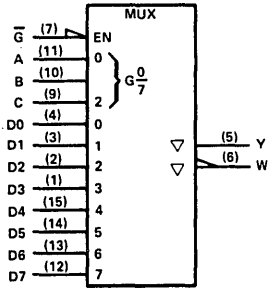
(true and inverted three-state outputs)

typical performance

TYPE	DELAY TIMES: DATA TO INV OUTPUT	DATA TO NON-INV OUTPUT	FROM ENABLE	TOTAL POWER
'251	17 ns	21 ns	21 ns	250 mW
'ALS251	6 ns	5 ns	4.5 ns	37.5 mW
'AS251	2.7 ns	3.5 ns	5.5 ns	140 mW
'LS251	17 ns	21 ns	21 ns	35 mW
'S251	4.5 ns	8 ns	14 ns	275 mW

SN54251 (J,FH) SN74251 (J,N)
SN54ALS251 (J,FH) SN74ALS251 (N,FN)
SN54AS251 (J,FH) SN74AS251 (N,FN)
SN54LS251 (J,FH) SN74LS251 (J,N,FN)
SN54S251 (J,FH) SN74S251 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	D3	9	C
2	D2	10	B
3	D1	11	A
4	D0	12	D7
5	Y	13	D6
6	W	14	D5
7	$\overline{G}$	15	D4
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	D3	12	C
3	D2	13	B
4	D1	14	A
5	D0	15	D7
6	nc	16	nc
7	Y	17	D6
8	W	18	D5
9	$\overline{G}$	19	D4
10	GND	20	V_{CC}

253

DUAL DATA SELECTORS/ MULTIPLEXERS

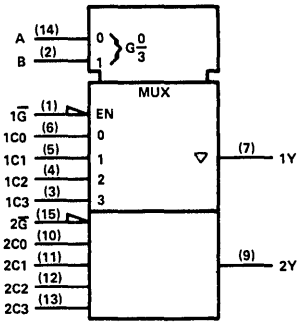
(three-state outputs)

typical performance

TYPE	DELAY TIMES: DATA TO NON-INV OUTPUT	FROM ENABLE	TOTAL POWER
'ALS253	5 ns	4.5 ns	32 mW
'AS253	3.3 ns	5.5 ns	117 mW
'LS253	12 ns	16 ns	35 mW

SN54ALS253 (J,FH) SN74ALS253 (N,FN)
SN54AS253 (J,FH) SN74AS253 (N,FN)
SN54LS253 (J,FH) SN74LS253 (J,N,FN)
SN54S253 (J,FH) SN74S253 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{1G}$	9	2Y	1	nc	11	nc
2	B	10	2C0	2	$\overline{1G}$	12	2Y
3	1C3	11	2C1	3	B	13	2C0
4	1C2	12	2C2	4	1C3	14	2C1
5	1C1	13	2C3	5	1C2	15	2C2
6	1C0	14	A	6	nc	16	nc
7	1Y	15	$\overline{2G}$	7	1C1	17	2C3
8	GND	16	V_{CC}	8	1C0	18	A
				9	1Y	19	$\overline{2G}$
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

257

QUAD DATA SELECTORS/ MULTIPLEXERS

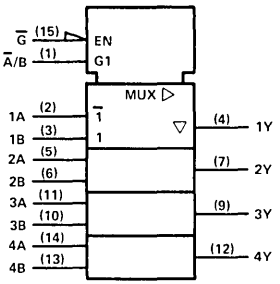
(non-inverted three-state outputs)

TYPE	DELAY TIMES: DATA TO NON-INV OUTPUT	DELAY TIMES: FROM ENABLE	TOTAL POWER
'ALS257	4.3 ns	7.5 ns	33.5 mW
'LS257	11 ns	18 ns	60 mW
'S257	5 ns	14 ns	320 mW

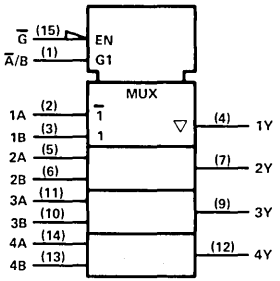
SN54ALS257 (J,FH)
SN54LS257 (J,FH)
SN54S257 (J,FH)

SN74ALS257 (N,FN)
SN74LS257 (J,N,FN)
SN74S257 (J,N,FN)

logic symbol, 'ALS257, 'LS257†



logic symbol, 'S257†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A/B	9	3Y	1	nc	11	nc
2	1A	10	3B	2	A/B	12	3Y
3	1B	11	3A	3	1A	13	3B
4	1Y	12	4Y	4	1B	14	3A
5	2A	13	4B	5	1Y	15	4Y
6	2B	14	4A	6	nc	16	nc
7	2Y	15	G	7	2A	17	4B
8	GND	16	V_{CC}	8	2B	18	4A
				9	2Y	19	G
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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258

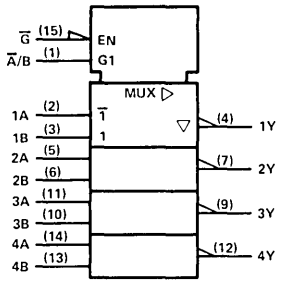
QUAD DATA SELECTORS/ MULTIPLEXERS
(inverted three-state outputs)

typical performance

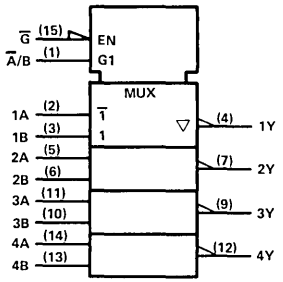
TYPE	DELAY TIMES: DATA TO INV OUTPUT	DELAY TIMES: FROM ENABLE	TOTAL POWER
'ALS258	3 ns	7.5 ns	29 mW
'LS258	11 ns	19 ns	60 mW
'S258	4 ns	14 ns	280 mW

SN54ALS258 (J,FH) SN74ALS258 (N,FN)
SN54LS258 (J,FH) SN74LS258 (J,N,FN)
SN54S258 (J,FH) SN74S258 (J,N,FN)

logic symbol, 'ALS258, 'LS258†



logic symbol, 'S258†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A/B	9	3Y	1	nc	11	nc
2	1A	10	3B	2	A/B	12	3Y
3	1B	11	3A	3	1A	13	3B
4	1Y	12	4Y	4	1B	14	3A
5	2A	13	4B	5	1Y	15	4Y
6	2B	14	4A	6	nc	16	nc
7	2Y	15	G	7	2A	17	4B
8	GND	16	VCC	8	2B	18	4A
				9	2Y	19	G
				10	GND	20	VCC

259

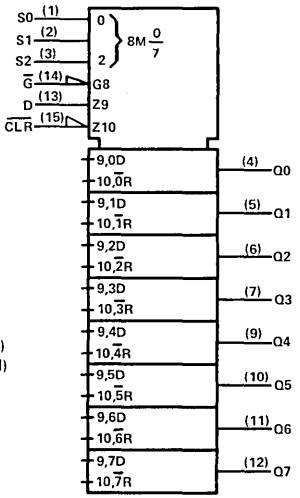
8-BIT ADDRESSABLE LATCHES

typical performance

TYPE	CLEAR	DELAY	TOTAL POWER
'259	LOW	12 ns	300 mW
'ALS259	LOW		
'LS259	LOW	17 ns	110 mW

SN54259 (J,FH) SN74259 (J,N)
SN54ALS259 (J,FH) SN74ALS259 (N,FN)
SN54LS259 (J,FH) SN74LS259 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	S0	9	Q4	1	nc	11	nc
2	S1	10	Q5	2	S0	12	Q4
3	S2	11	Q6	3	S1	13	Q5
4	Q0	12	Q7	4	S2	14	Q6
5	Q1	13	D	5	Q0	15	Q7
6	Q2	14	G	6	nc	16	nc
7	Q3	15	CLR	7	Q1	17	D
8	GND	16	VCC	8	Q2	18	G
				9	Q3	19	CLR
				10	GND	20	VCC

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

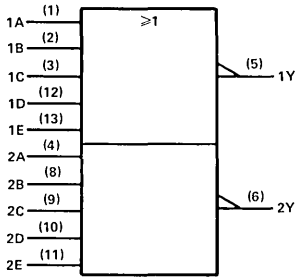
260

DUAL 5-INPUT POSITIVE-NOR GATES

TYPE	POWER/ GATE	DELAY
'S260	54 mW	4 ns

SN54S260 (J,FH) SN74S260 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	2B	1	nc	11	nc
2	1B	9	2C	2	1A	12	2B
3	1C	10	2D	3	1B	13	2C
4	2A	11	2E	4	1C	14	2D
5	1Y	12	1D	5	nc	15	nc
6	2Y	13	1E	6	2A	16	2E
7	GND	14	V_{CC}	7	nc	17	nc
				8	1Y	18	1D
				9	2Y	19	1E
				10	GND	20	V_{CC}

positive logic: $Y = \overline{ABCD}$

261

2-BIT BY 4-BIT PARALLEL BINARY MULTIPLIERS

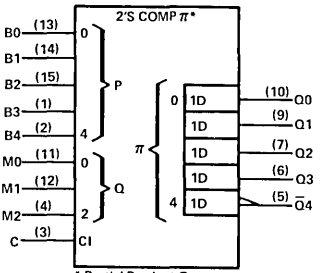
typical performance

TYPE	POWER	TIME**
'LS261	100 mW	25 ns

SN54LS261 (J,FH) SN74LS261 (J,N,FN)

** 5-Bit Product Time

logic symbol†



* Partial-Product Generator

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	B3	9	Q1	1	nc	11	nc
2	B4	10	Q0	2	B3	12	Q1
3	C	11	M0	3	B4	13	Q0
4	M2	12	M1	4	C	14	M0
5	Q̄4	13	B0	5	M2	15	M1
6	Q3	14	B1	6	nc	16	nc
7	Q2	15	B2	7	Q̄4	17	B0
8	GND	16	V_{CC}	8	Q3	18	B1
				9	Q2	19	B2
				10	GND	20	V_{CC}

265

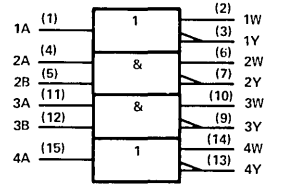
QUAD COMPLEMENTARY-OUTPUT ELEMENTS

typical performance

TYPE	POWER
'265	125 mW

SN54265 (J,FH) SN74265 (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	1A	9	3Y	1	nc	11	nc
2	1W	10	3W	2	1A	12	3Y
3	1Y	11	3A	3	1W	13	3W
4	2A	12	3B	4	1Y	14	3A
5	2B	13	4Y	5	2A	15	3B
6	2W	14	4W	6	nc	16	nc
7	2Y	15	4A	7	2B	17	4Y
8	GND	16	V_{CC}	8	2W	18	4W
				9	2Y	19	4A
				10	GND	20	V_{CC}

266

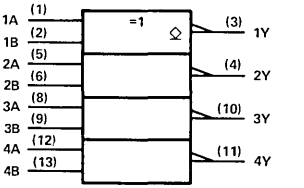
QUAD 2-INPUT EXCLUSIVE-NOR GATES WITH OPEN-COLLECTOR OUTPUTS

typical performance

TYPE	POWER	DELAY
'LS266	40 mW	18 ns

SN54LS266 (J,FH) SN74LS266 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{A} \oplus \overline{B} = AB + \overline{AB}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3A	1	nc	11	nc
2	1B	9	3B	2	1A	12	3A
3	1Y	10	3Y	3	1B	13	3B
4	2Y	11	4Y	4	1Y	14	3Y
5	2A	12	4A	5	nc	15	nc
6	2B	13	4B	6	2Y	16	4Y
7	GND	14	V_{CC}	7	nc	17	nc
				8	2A	18	4A
				9	2B	19	4B
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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270

2048-BIT READ-ONLY MEMORIES
(open-collector outputs, 512 4-bit words)

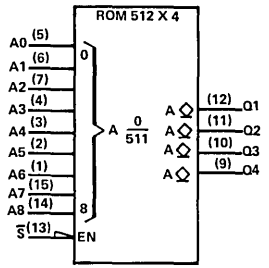
typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER/ BIT
'S270	45 ns	15 ns	0.26 mW

SN54S270 (J) SN74S270 (J,N)

This product is no longer in production.

logic symbol†



pin assignments

J, N PACKAGES			
1	A6	9	Q4
2	A5	10	Q3
3	A4	11	Q2
4	A3	12	Q1
5	A0	13	S̄
6	A1	14	A8
7	A2	15	A7
8	GND	16	V_{CC}

For chip carrier information, contact the factory.

271

2048-BIT READ-ONLY MEMORIES
(open-collector outputs, 256 8-bit words)

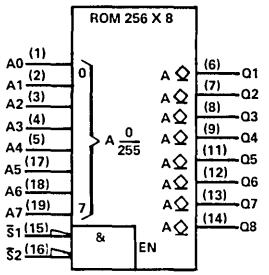
typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER/ BIT
'S271	45 ns	15 ns	0.26 mW

SN54S271 (J,FH) SN74S271 (J,N,FN)

This product in no longer in production.

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A0	11	Q5	1	A0	11	Q5
2	A1	12	Q6	2	A1	12	Q6
3	A2	13	Q7	3	A2	13	Q7
4	A3	14	Q8	4	A3	14	Q8
5	A4	15	S̄1	5	A4	15	S̄1
6	Q1	16	S̄2	6	Q1	16	S̄2
7	Q2	17	A5	7	Q2	17	A5
8	Q3	18	A6	8	Q3	18	A6
9	Q4	19	A7	9	Q4	19	A7
10	GND	20	V_{CC}	10	GND	20	V_{CC}

273

OCTAL D-TYPE FLIP-FLOPS
(common clock, single-rail outputs)

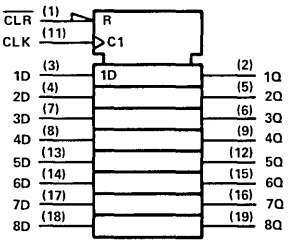
typical performance

TYPE	FREQ	POWER PER F-F	DATA TIMES SETUP	DATA TIMES HOLD
'273	40 MHz	39 mW	20 ns‡	5 ns‡
'ALS273	50 MHz	9.4 mW		
'LS273	40 MHz	10.6 mW	20 ns‡	5 ns‡

‡ Rising edge of clock pulse

SN54273 (J,FH) SN74273 (J,N)
SN54ALS273 (J,FH) SN74ALS273 (N,FN)
SN54LS273 (J,FH) SN74LS273 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	CLR	11	CLK	1	CLR	11	CLK
2	1Q	12	5Q	2	1Q	12	5Q
3	1D	13	5D	3	1D	13	5D
4	2D	14	6D	4	2D	14	6D
5	2Q	15	6Q	5	2Q	15	6Q
6	3Q	16	7Q	6	3Q	16	7Q
7	3D	17	7D	7	3D	17	7D
8	4D	18	8D	8	4D	18	8D
9	4Q	19	8Q	9	4Q	19	8Q
10	GND	20	V_{CC}	10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

274

4-BIT BY 4-BIT BINARY MULTIPLIERS

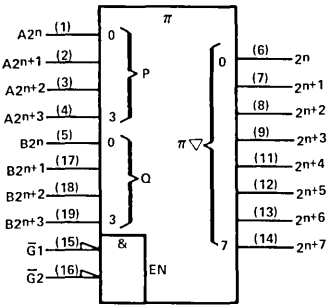
typical performance

TYPE	POWER	TIME*
'S274	525 mW	50 ns

SN54S274 (J,FH) SN74S274 (J,N,FN)

* 8-Bit Product Time

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$A2^n$	11	2^{n+4}	1	$A2^n$	11	2^{n+4}
2	$A2^{n+1}$	12	2^{n+5}	2	$A2^{n+1}$	12	2^{n+5}
3	$A2^{n+2}$	13	2^{n+6}	3	$A2^{n+2}$	13	2^{n+6}
4	$A2^{n+3}$	14	2^{n+7}	4	$A2^{n+3}$	14	2^{n+7}
5	$B2^n$	15	$\overline{G}1$	5	$B2^n$	15	$\overline{G}1$
6	2^n	16	$\overline{G}2$	6	2^n	16	$\overline{G}2$
7	2^{n+1}	17	$B2^{n+1}$	7	2^{n+1}	17	$B2^{n+1}$
8	2^{n+2}	18	$B2^{n+2}$	8	2^{n+2}	18	$B2^{n+2}$
9	2^{n+3}	19	$B2^{n+3}$	9	2^{n+3}	19	$B2^{n+3}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

275

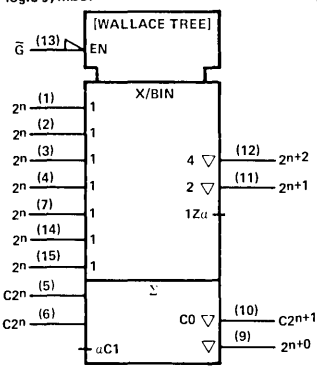
7-BIT-SLICE WALLACE TREES

typical performance

TYPE	POWER
'LS275	125 mW
'S275	525 mW

SN54LS275 (J,FH) SN74LS275 (J,N,FN)
SN54S275 (J,FH) SN74S275 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	2^n	9	2^{n+0}	1	nc	11	nc
2	2^n	10	$C2^{n+1}$	2	2^n	12	2^{n+0}
3	2^n	11	2^{n+1}	3	2^n	13	$C2^{n+1}$
4	2^n	12	2^{n+2}	4	2^n	14	2^{n+1}
5	$C2^n$	13	$\overline{G}$	5	2^n	15	2^{n+2}
6	$C2^n$	14	2^n	6	nc	16	nc
7	2^n	15	2^n	7	$C2^n$	17	$\overline{G}$
8	GND	16	V_{CC}	8	$C2^n$	18	2^n
				9	2^n	19	2^n
				10	GND	20	V_{CC}

276

QUAD J-$\overline{K}$ FLIP-FLOPS

(separate clocks, edge-triggering, common direct clear and preset)

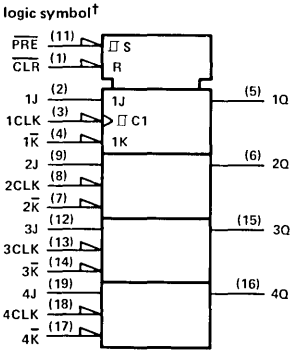
typical performance

TYPE	FREQ	POWER/ F-F	DATA TIMES	
			SETUP	HOLD
'276	50 MHz	75 mW	3 ns↓	10 ns↓

↓ Falling edge of clock pulse

SN54276 (J,FH) SN74276 (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	$\overline{CLR}$	11	$\overline{PRE}$	1	$\overline{CLR}$	11	$\overline{PRE}$
2	1J	12	3J	2	1J	12	3J
3	1CLK	13	3CLK	3	1CLK	13	3CLK
4	$1\overline{K}$	14	$3\overline{K}$	4	$1\overline{K}$	14	$3\overline{K}$
5	1Q	15	3Q	5	1Q	15	3Q
6	2Q	16	4Q	6	2Q	16	4Q
7	$2\overline{K}$	17	$4\overline{K}$	7	$2\overline{K}$	17	$4\overline{K}$
8	2CLK	18	4CLK	8	2CLK	18	4CLK
9	2J	19	4J	9	2J	19	4J
10	GND	20	V_{CC}	10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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278

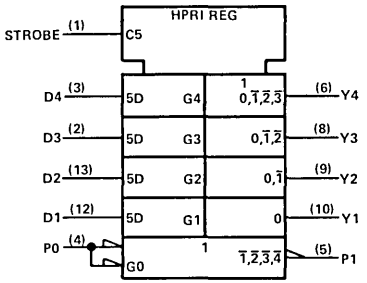
4-BIT CASCADABLE PRIORITY REGISTERS

typical performance

TYPE	POWER	DELAY
'278	275 mW	35 ns

SN54278 (J,FH) SN74278 (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	STRB	8	Y3	1	nc	11	nc
2	D3	9	Y2	2	STRB	12	Y3
3	D4	10	Y1	3	D3	13	Y2
4	P0	11	nc	4	D4	14	Y1
5	P1	12	D1	5	nc	15	nc
6	Y4	13	D2	6	P0	16	nc
7	GND	14	V_{CC}	7	nc	17	nc
				8	P1	18	D1
				9	Y4	19	D2
				10	GND	20	V_{CC}

279

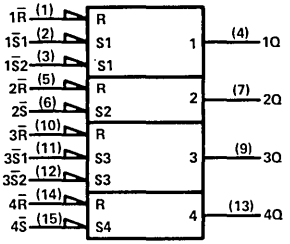
QUAD $\overline{S}$-$\overline{R}$ LATCHES

typical performance

TYPE	POWER	DELAY
'279	90 mW	12 ns
'LS279	19 mW	12 ns

SN54279 (J,FH) SN74279 (J,N,FN)
SN54LS279 (J,FH) SN74LS279 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1R̄	9	3Q	1	nc	11	nc
2	1S̄1	10	3R̄	2	1R̄	12	3Q
3	1S̄2	11	3S̄1	3	1S̄1	13	3R̄
4	1Q	12	3S̄2	4	1S̄2	14	3S̄1
5	2R̄	13	4Q	5	1Q	15	3S̄2
6	2S̄	14	4R̄	6	nc	16	nc
7	2Q	15	4S̄	7	2R̄	17	4Q
8	GND	16	V_{CC}	8	2S̄	18	4R̄
				9	2Q	19	4S̄
				10	GND	20	V_{CC}

280

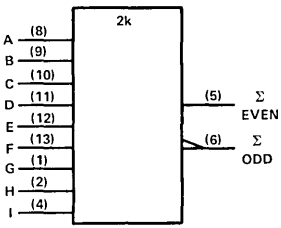
9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

typical performance

TYPE	POWER	DELAY
'AS280		
'LS280	80 mW	31 ns
'S280	335 mW	13 ns

SN54AS280 (J,FH) SN74AS280 (N,FN)
SN54LS280 (J,FH) SN74LS280 (J,N,FN)
SN54S280 (J,FH) SN74S280 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	G	8	A	1	nc	11	nc
2	H	9	B	2	G	12	A
3	nc	10	C	3	H	13	B
4	I	11	D	4	nc	14	C
5	ΣEVEN	12	E	5	nc	15	nc
6	ΣODD	13	F	6	I	16	D
7	GND	14	V_{CC}	7	nc	17	nc
				8	ΣEVEN	18	E
				9	ΣODD	19	F
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

281

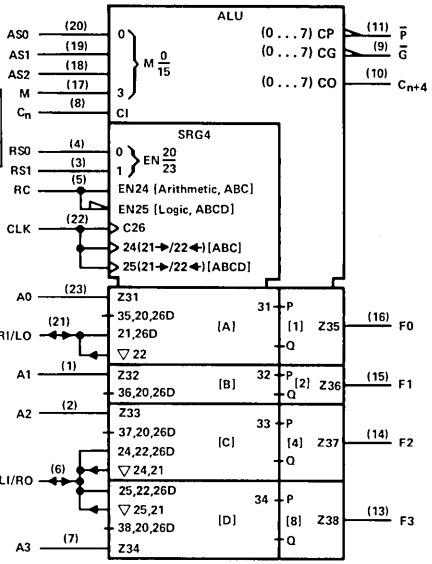
4-BIT PARALLEL BINARY ACCUMULATORS

typical performance

TYPE	ADD TIME	TOTAL POWER
'S281	20 ns	720 mW

SN54S281 (J,FH)
SN74S281 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A1	13	F3	1	nc	15	nc
2	A2	14	F2	2	A1	16	F3
3	RS1	15	F1	3	A2	17	F2
4	RS0	16	F0	4	RS1	18	F1
5	RC	17	M	5	RS0	19	F0
6	LI/RO	18	AS2	6	RC	20	M
7	A3	19	AS1	7	LI/RO	21	AS2
8	C_n	20	AS0	8	nc	22	nc
9	$\overline{G}$	21	RI/LO	9	A3	23	AS1
10	C_{n+4}	22	CLK	10	C_n	24	AS0
11	$\overline{P}$	23	A0	11	$\overline{G}$	25	RI/LO
12	GND	24	V_{CC}	12	C_{n+4}	26	CLK
				13	$\overline{P}$	27	A0
				14	GND	28	V_{CC}

283

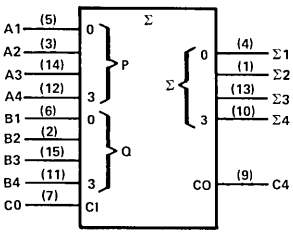
4-BIT BINARY FULL ADDERS

typical performance

TYPE	CARRY TIME	ADD TIME	POWER/ BIT
'283	10 ns	16 ns	76 mW
'LS283	10 ns	15 ns	24 mW
'S283	7 ns	11 ns	124 mW

SN54283 (J,FH)
SN54LS283 (J,FH)
SN54S283 (J,FH)
SN74283 (J,N)
SN74LS283 (J,N,FN)
SN74S283 (J,N,FN)

logic symbol†



typical performance

J, N PACKAGES				FH, FN PACKAGES			
1	Σ2	9	C4	1	nc	11	nc
2	B2	10	Σ4	2	Σ2	12	C4
3	A2	11	B4	3	B2	13	Σ4
4	Σ1	12	A4	4	A2	14	B4
5	A1	13	Σ3	5	Σ1	15	A4
6	B1	14	A3	6	nc	16	nc
7	C0	15	B3	7	A1	17	Σ3
8	GND	16	V_{CC}	8	B1	18	A3
				9	C0	19	B3
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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284

4-BIT BY 4-BIT PARALLEL BINARY MULTIPLIERS USED WITH '285

- MSB's for 4 X 4 multiplier ('285 provides LSB's)
- Use 'S274, 'LS275, 'S275 for new designs/larger multipliers

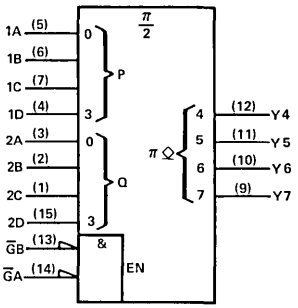
typical performance

TYPE	POWER	TIME*
'284	460 mW	40 ns

SN54284 (J,FH) SN74284 (J,N)

* 8-Bit Product Time

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	2C	9	Y7	1	nc	11	nc
2	2B	10	Y6	2	2C	12	Y7
3	2A	11	Y5	3	2B	13	Y6
4	1D	12	Y4	4	2A	14	Y5
5	1A	13	$\overline{GB}$	5	1D	15	Y4
6	1B	14	$\overline{GA}$	6	nc	16	nc
7	1C	15	2D	7	1A	17	$\overline{GB}$
8	GND	16	V_{CC}	8	1B	18	$\overline{GA}$
				9	1C	19	2D
				10	GND	20	V_{CC}

285

4-BIT BY 4-BIT PARALLEL BINARY MULTIPLIERS USED WITH '284

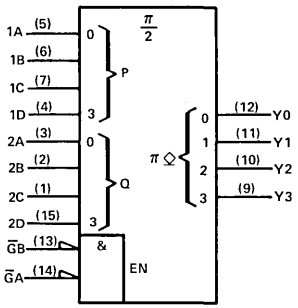
- LSB's for 4 X 4 multiplier ('284 provides MSB's)
- Use 'S274, 'LS275, 'S275 for new designs/larger multipliers

typical performance

TYPE	POWER
'285	460 mW

SN54285 (J,FH) SN74285 (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	2C	9	Y3	1	nc	11	nc
2	2B	10	Y2	2	2C	12	Y3
3	2A	11	Y1	3	2B	13	Y2
4	1D	12	Y0	4	2A	14	Y1
5	1A	13	$\overline{GB}$	5	1D	15	Y0
6	1B	14	$\overline{GA}$	6	nc	16	nc
7	1C	15	2D	7	1A	17	$\overline{GB}$
8	GND	16	V_{CC}	8	1B	18	$\overline{GA}$
				9	1C	19	2D
				10	GND	20	V_{CC}

287

(This number has been changed to TBP14S10. Product Guide information for this TTL circuit can be found at the end of this section.)

288

(This number has been changed to TBP18S030. Product Guide information for this TTL circuit can be found at the end of this section.)

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

289

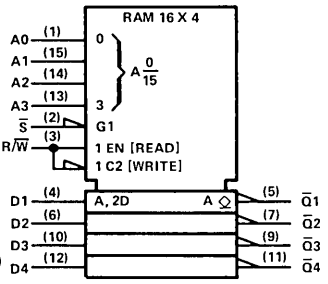
64-BIT RANDOM-ACCESS MEMORIES
(16 4-bit words, open-collector outputs)

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER/ BIT
'LS289A	50 ns	35 ns	2.7 mW
'S289A	25 ns	12 ns	5.9 mW

SN54LS289A (J,FH) SN74LS289A (J,N,FN)
SN54S289A (J,FH) SN74S289A (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A0	9	Q̄3	1	nc	11	nc
2	S̄	10	D3	2	A0	12	Q̄3
3	R/W̄	11	Q̄4	3	S̄	13	D3
4	D1	12	D4	4	R/W̄	14	Q̄4
5	Q̄1	13	A3	5	D1	15	D4
6	D2	14	A2	6	nc	16	nc
7	Q̄2	15	A1	7	Q̄1	17	A3
8	GND	16	V_{CC}	8	D2	18	A2
				9	Q̄2	19	A1
				10	GND	20	V_{CC}

290

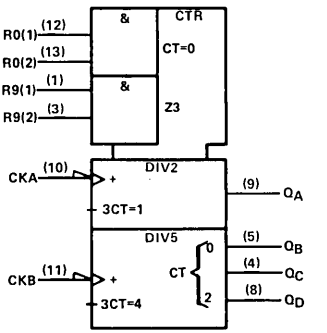
DECADE COUNTERS
(divide-by-two and divide-by-five)

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'290	32 MHz	HIGH	160 mW
'LS290	32 MHz	HIGH	40 mW

SN54290 (J,FH) SN74290 (J,N)
SN54LS290 (J,FH) SN74LS290 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	R9(1)	8	Q_D	1	nc	11	nc
2	nc	9	Q_A	2	R9(1)	12	Q_D
3	R9(2)	10	CKA	3	nc	13	Q_A
4	Q_C	11	CKB	4	R9(2)	14	CKA
5	Q_B	12	R0(1)	5	nc	15	nc
6	nc	13	R0(2)	6	Q_C	16	CKB
7	GND	14	V_{CC}	7	nc	17	nc
				8	Q_B	18	R0(1)
				9	nc	19	R0(2)
				10	GND	20	V_{CC}

292

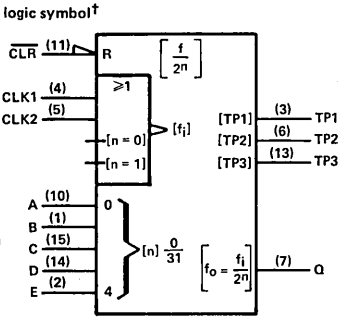
PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS
(digitally programmable from 2^2 to 2^{31})

typical performance

TYPE	POWER	f_{max}
'LS292	200 mW	50 MHz

SN54LS292 (J,FH) SN74LS292 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	B	9	nc	1	nc	11	nc
2	E	10	A	2	B	12	nc
3	TP1	11	CLR̄	3	E	13	A
4	CLK1	12	nc	4	TP1	14	CLR̄
5	CLK2	13	TP3	5	CLK1	15	nc
6	TP2	14	D	6	nc	16	nc
7	Q	15	C	7	CLK2	17	TP3
8	GND	16	V_{CC}	8	TP2	18	D
				9	Q	19	C
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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293

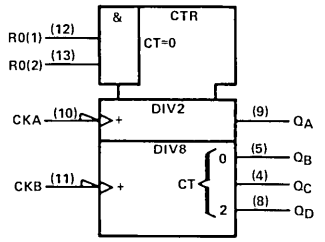
4-BIT BINARY COUNTERS
(divide-by-two and divide-by-eight)

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'293	32 MHz	HIGH	160 mW
'LS293	32 MHz	HIGH	39 mW

SN54293 (J,FH) SN74293 (J,N)
SN54LS293 (J,FH) SN74LS293 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	nc	8	Q_D	1	nc	11	nc
2	nc	9	Q_A	2	nc	12	Q_D
3	nc	10	CKA	3	nc	13	Q_A
4	Q_C	11	CKB	4	nc	14	CKA
5	Q_B	12	R0(1)	5	nc	15	nc
6	nc	13	R0(2)	6	Q_C	16	CKB
7	GND	14	V_{CC}	7	nc	17	nc
				8	Q_B	18	R0(1)
				9	nc	19	R0(2)
				10	GND	20	V_{CC}

294

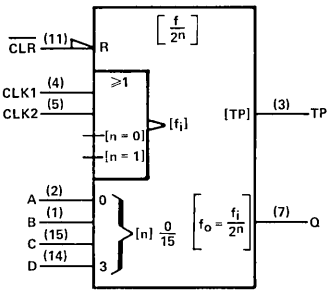
PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS
(digitally programmable from 2^2 to 2^{15})

typical performance

TYPE	POWER	f_{max}
'LS294	150 mW	50 MHz

SN54LS294 (J,FH) SN74LS294 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	B	9	nc	1	nc	11	nc
2	A	10	nc	2	B	12	nc
3	TP	11	$\overline{CLR}$	3	A	13	nc
4	CLK1	12	nc	4	TP	14	$\overline{CLR}$
5	CLK2	13	nc	5	CLK1	15	nc
6	nc	14	D	6	nc	16	nc
7	Q	15	C	7	CLK2	17	nc
8	GND	16	V_{CC}	8	nc	18	D
				9	Q	19	C
				10	GND	20	V_{CC}

295

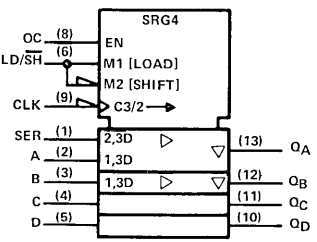
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	TOTAL POWER
'LS295B	30 MHz	D	70 mW

SN54LS295B (J,FH) SN74LS295B (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	SER	8	OC	1	nc	11	nc
2	A	9	CLK	2	SER	12	OC
3	B	10	Q_D	3	A	13	CLK
4	C	11	Q_C	4	B	14	Q_D
5	D	12	Q_B	5	nc	15	nc
6	LD/$\overline{SH}$	13	Q_A	6	C	16	Q_C
7	GND	14	V_{CC}	7	nc	17	nc
				8	D	18	Q_B
				9	LD/$\overline{SH}$	19	Q_A
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

297

DIGITAL PHASE-LOCKED-LOOP FILTERS
(cascadable for higher-order loops)

typical performance

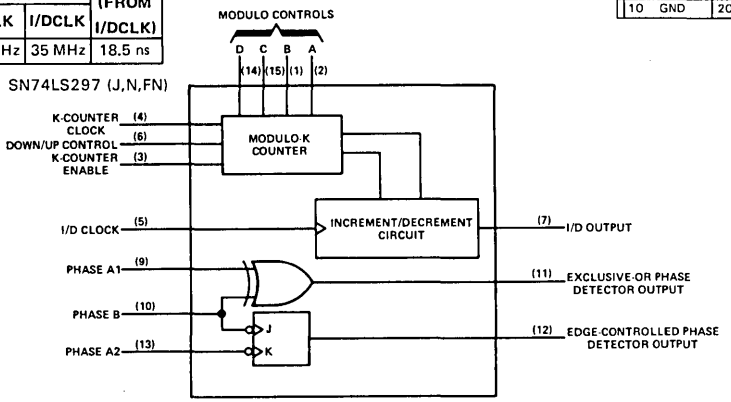
TYPE	POWER	f_{max}		DELAY (FROM I/DCLK)
		KCLK	I/DCLK	
'LS297	375 mW	50 MHz	35 MHz	18.5 ns

SN54LS297 (J,FH) SN74LS297 (J,N,FN)

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	B	9	ϕA1	1	nc	11	nc
2	A	10	ϕB	2	B	12	ϕA1
3	ENCTR	11	XOPRD	3	A	13	ϕB
4	K CLK	12	ECPD	4	ENCTR	14	XOPRD
5	I/D CLK	13	ϕA2	5	K CLK	15	ECPD
6	D/$\overline{U}$	14	D	6	nc	16	nc
7	I/D OUT	15	C	7	I/D CLK	17	ϕA2
8	GND	16	V_{CC}	8	D/$\overline{U}$	18	D
				9	I/D OUT	19	C
				10	GND	20	V_{CC}

simplified block diagram†



298

QUAD 2-INPUT MULTIPLEXERS WITH STORAGE

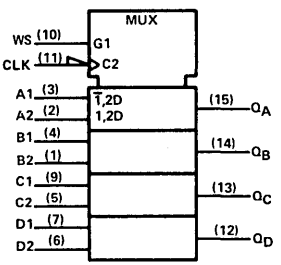
typical performance

TYPE	POWER	DELAY*
'298	195 mW	20 ns
'LS298	65 mW	20 ns

* From clock to non-inverted output

SN54298 (J,FH) SN74298 (J,N)
SN54LS298 (J,FH) SN74LS298 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	B2	9	C1	1	nc	11	nc
2	A2	10	WS	2	B2	12	C1
3	A1	11	CLK	3	A2	13	WS
4	B1	12	Q_D	4	A1	14	CLK
5	C2	13	Q_C	5	B1	15	Q_D
6	D2	14	Q_B	6	nc	16	nc
7	D1	15	Q_A	7	C2	17	Q_C
8	GND	16	V_{CC}	8	D2	18	Q_B
				9	D1	19	Q_A
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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299

8-BIT BIDIRECTIONAL UNIVERSAL SHIFT/STORAGE REGISTERS

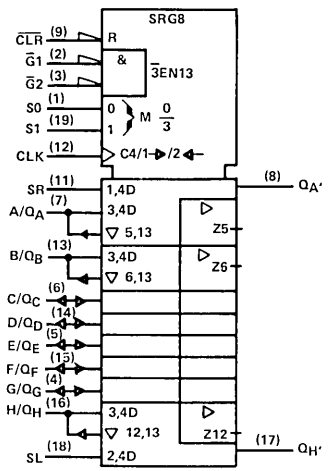
(three-state outputs)

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'ALS299	30 MHz	D	LOW	100 mW
'LS299	35 MHz	D	LOW	175 mW
'S299	50 MHz	D	LOW	750 mW

SN54ALS299 (J,FH) SN74ALS299 (N,FN)
SN54LS299 (J,FH) SN74LS299 (J,N,FN)
SN54S299 (J,FH) SN74S299 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	S0	11	SR
2	$\overline{G1}$	12	CLK
3	$\overline{G2}$	13	B/Q_B
4	G/Q_G	14	D/Q_D
5	E/Q_E	15	F/Q_F
6	C/Q_C	16	H/Q_H
7	A/Q_A	17	$Q_{H'}$
8	$Q_{A'}$	18	SL
9	$\overline{CLR}$	19	S1
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	S0	11	SR
2	$\overline{G1}$	12	CLK
3	$\overline{G2}$	13	B/Q_B
4	G/Q_G	14	D/Q_D
5	E/Q_E	15	F/Q_F
6	C/Q_C	16	H/Q_H
7	A/Q_A	17	$Q_{H'}$
8	$Q_{A'}$	18	SL
9	$\overline{CLR}$	19	S1
10	GND	20	V_{CC}

301

256-BIT RANDOM-ACCESS MEMORIES

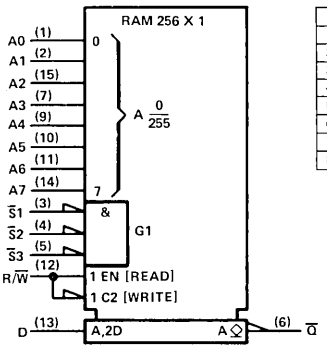
(256 1-bit words, open-collector output)

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER/ BIT
'S301	42 ns	13 ns	1.9 mW

SN74S301 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	A0	9	A4
2	A1	10	A5
3	$\overline{S1}$	11	A6
4	$\overline{S2}$	12	$R/\overline{W}$
5	$\overline{S3}$	13	D
6	$\overline{Q}$	14	A7
7	A3	15	A2
8	GND	16	V_{CC}

6

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

317

256-BIT RANDOM-ACCESS MEMORIES WITH OPEN-COLLECTOR OUTPUTS

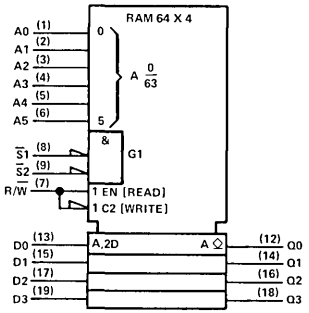
(64 words of 4 bits each)

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER/ BIT
'ALS317	30 ns	20 ns	0.9 mW

SN54ALS317 (J,FH) SN74ALS317 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A0	11	nc	1	A0	11	nc
2	A1	12	Q0	2	A1	12	Q0
3	A2	13	D0	3	A2	13	D0
4	A3	14	Q1	4	A3	14	Q1
5	A4	15	D1	5	A4	15	D1
6	A5	16	Q2	6	A5	16	Q2
7	R/$\overline{W}$	17	D2	7	R/$\overline{W}$	17	D2
8	$\overline{S}$1	18	Q3	8	$\overline{S}$1	18	Q3
9	$\overline{S}$2	19	D3	9	$\overline{S}$2	19	D3
10	GND	20	V_{CC}	10	GND	20	V_{CC}

318

256-BIT RANDOM-ACCESS MEMORIES WITH OPEN-COLLECTOR OUTPUTS

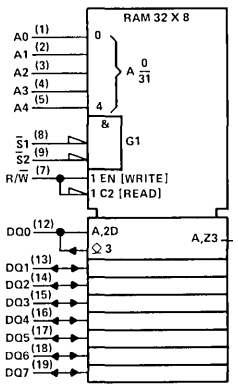
(32 words of 8 bits each)

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER/ BIT
'ALS318	30 ns	20 ns	0.9 mW

SN54ALS318 (J,FH) SN74ALS318 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A0	11	nc	1	A0	11	nc
2	A1	12	DQ0	2	A1	12	DQ0
3	A2	13	DQ1	3	A2	13	DQ1
4	A3	14	DQ2	4	A3	14	DQ2
5	A4	15	DQ3	5	A4	15	DQ3
6	nc	16	DQ4	6	nc	16	DQ4
7	R $\overline{W}$	17	DQ5	7	R $\overline{W}$	17	DQ5
8	$\overline{S}$1	18	DQ6	8	$\overline{S}$1	18	DQ6
9	$\overline{S}$2	19	DQ7	9	$\overline{S}$2	19	DQ7
10	GND	20	V_{CC}	10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

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319

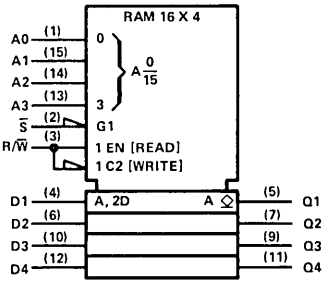
64-BIT RANDOM ACCESS MEMORIES
(16-four bit words, open-collector outputs)

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER/ BIT
'LS319A	50 ns	35 ns	2.7 mW

SN54LS319A (J,FH) SN74LS319A (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A0	9	Q3	1	nc	11	nc
2	S̄	10	D3	2	A0	12	Q3
3	R/W̄	11	Q4	3	S̄	13	D3
4	D1	12	D4	4	R/W̄	14	Q4
5	Q1	13	A3	5	D1	15	D4
6	D2	14	A2	6	nc	16	nc
7	Q2	15	A1	7	Q1	17	A3
8	GND	16	V_{CC}	8	D2	18	A2
				9	Q2	19	A1
				10	GND	20	V_{CC}

320

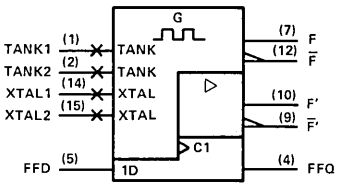
CRYSTAL-CONTROLLED OSCILLATORS

typical performance

TYPE	f_{max}	POWER
'LS320	30 MHz	210 mW

SN54LS320 (J) SN74LS320 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	TANK1	9	F̄'
2	TANK2	10	F'
3	GND1	11	$V_{CC'}$
4	FFQ	12	F̄
5	FFD	13	nc
6	nc	14	XTAL1
7	F	15	XTAL2
8	GND2	16	V_{CC}

For chip carrier information, contact the factory.

321

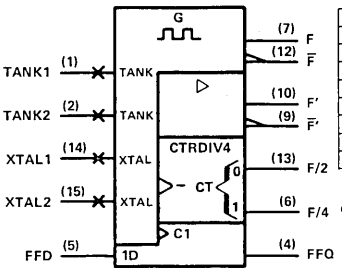
CRYSTAL-CONTROLLED OSCILLATORS
(with F/2 and F/4 count-down outputs)

typical performance

TYPE	FREQ	POWER
'LS321	30 MHz	235 mW

SN54LS321 (J) SN74LS321 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	TANK1	9	F̄'
2	TANK2	10	F'
3	GND1	11	$V_{CC'}$
4	FFQ	12	F̄
5	FFD	13	F/2
6	F/4	14	XTAL1
7	F	15	XTAL2
8	GND2	16	V_{CC}

For chip carrier information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

322

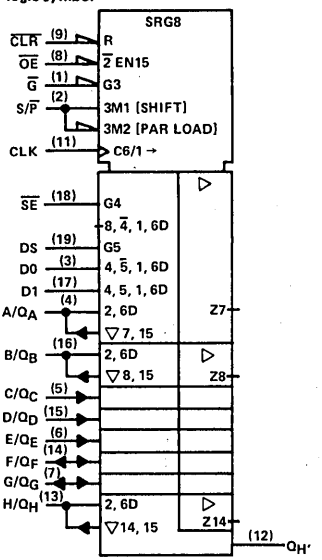
8-BIT SHIFT REGISTERS WITH SIGN EXTEND
(three-state outputs, multiplexed I/O)

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	POWER
'LS322A	35 MHz	D	LOW	175 mW

SN54LS322A (J,FH) SN74LS322A (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{G}$	11	CLK	1	$\overline{G}$	11	CLK
2	S/$\overline{P}$	12	$Q_{H'}$	2	S/$\overline{P}$	12	$Q_{H'}$
3	D0	13	H/Q_H	3	D0	13	H/Q_H
4	A/Q_A	14	F/Q_F	4	A/Q_A	14	F/Q_F
5	C/Q_C	15	D/Q_D	5	C/Q_C	15	D/Q_D
6	E/Q_E	16	B/Q_B	6	E/Q_E	16	B/Q_B
7	G/Q_G	17	D1	7	G/Q_G	17	D1
8	$\overline{OE}$	18	$\overline{SE}$	8	$\overline{OE}$	18	$\overline{SE}$
9	$\overline{CLR}$	19	DS	9	$\overline{CLR}$	19	DS
10	GND	20	V_{CC}	10	GND	20	V_{CC}

323

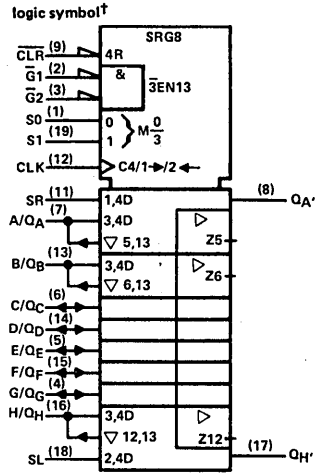
8-BIT BIDIRECTIONAL SHIFT/STORAGE REGISTERS
(three-state outputs)

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	POWER
'ALS323	30 MHz	D	100 mW
'LS323	35 MHz	D	175 mW

SN54ALS323 (J,FH) SN74ALS323 (N,FN)
SN54LS323 (J,FH) SN74LS323 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	S0	11	SR	1	S0	11	SR
2	$\overline{G}1$	12	CLK	2	$\overline{G}1$	12	CLK
3	$\overline{G}2$	13	B/Q_B	3	$\overline{G}2$	13	B/Q_B
4	G/Q_G	14	D/Q_D	4	G/Q_G	14	D/Q_D
5	E/Q_E	15	F/Q_F	5	E/Q_E	15	F/Q_F
6	C/Q_C	16	H/Q_H	6	C/Q_C	16	H/Q_H
7	A/Q_A	17	$Q_{H'}$	7	A/Q_A	17	$Q_{H'}$
8	$Q_{A'}$	18	SL	8	$Q_{A'}$	18	SL
9	$\overline{CLR}$	19	S1	9	$\overline{CLR}$	19	S1
10	GND	20	V_{CC}	10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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347

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

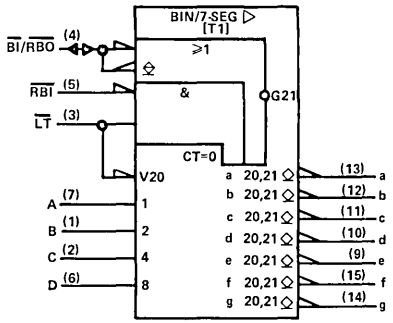
(open-collector outputs, low-voltage version of 'LS47)

typical performance

TYPE	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	POWER
SN54LS347	12 mA	7 V	35 mW
SN74LS347	24 mA	7 V	35 mW

SN54LS347 (J,FH) SN74LS347 (J,N, FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	B	9	e
2	C	10	d
3	$\overline{LT}$	11	c
4	$\overline{BI/RBO}$	12	b
5	$\overline{RBI}$	13	a
6	D	14	g
7	A	15	f
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	B	12	e
3	C	13	d
4	$\overline{LT}$	14	c
5	$\overline{BI/RBO}$	15	b
6	nc	16	nc
7	$\overline{RBI}$	17	a
8	D	18	g
9	A	19	f
10	GND	20	V_{CC}

348

8-LINE TO 3-LINE PRIORITY ENCODERS

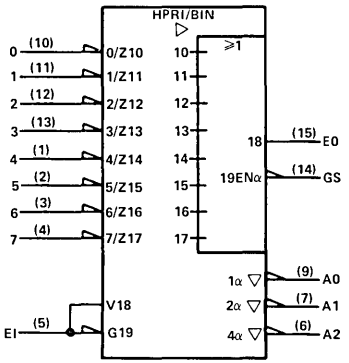
(with three-state outputs)

typical performance

TYPE	DELAY	POWER
'LS348	16 ns	63 mW

SN54LS348 (J,FH) SN74LS348 (J,N,FN)

logic symbol†



pin assignments

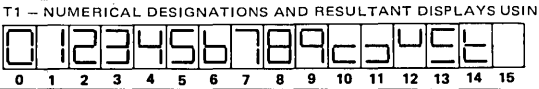
J, N PACKAGES			
1	4	9	A0
2	5	10	0
3	6	11	1
4	7	12	2
5	E1	13	3
6	A2	14	GS
7	A1	15	EO
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	4	12	A0
3	5	13	0
4	6	14	1
5	7	15	2
6	nc	16	nc
7	E1	17	3
8	A2	18	GS
9	A1	19	EO
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

FONT TABLE T1 — NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS USING 'LS347



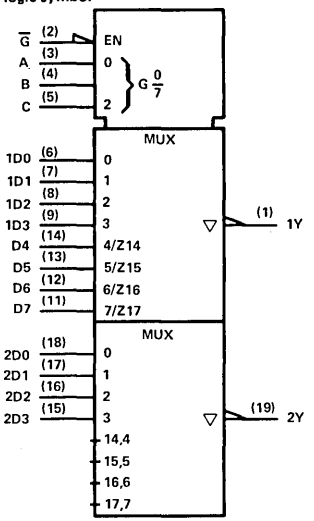
351

DUAL 8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS
(three-state outputs; four common data inputs)
typical performance

TYPE	DELAY TIMES		TOTAL POWER
	DATA TO INV OUTPUT	FROM ENABLE	
'351	10 ns	17 ns	220 mW

SN74351 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	1Y	11	D7
2	$\overline{G}$	12	D6
3	A	13	D5
4	B	14	D4
5	C	15	2D3
6	1D0	16	2D2
7	1D1	17	2D1
8	1D2	18	2D0
9	1D3	19	2Y
10	GND	20	V_{CC}

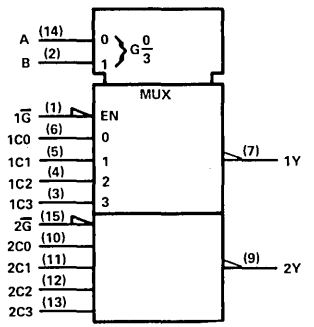
352

DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS
(inverting version of 'LS153)
typical performance

TYPE	DELAY TIMES		TOTAL POWER
	DATA TO INV OUTPUT	FROM ENABLE	
'ALS352	6 ns	4.5 ns	32.5 mW
'AS352	2.7 ns	4.5 ns	122.5 mW
'LS352	15 ns	18.5 ns	31 mW

SN54ALS352 (J,FH) SN74ALS352 (N,FN)
SN54AS352 (J,FH) SN74AS352 (N,FN)
SN54LS352 (J,FH) SN74LS352 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$1\overline{G}$	9	2Y	1	nc	11	nc
2	B	10	2C0	2	$1\overline{G}$	12	2Y
3	1C3	11	2C1	3	B	13	2C0
4	1C2	12	2C2	4	1C3	14	2C1
5	1C1	13	2C3	5	1C2	15	2C2
6	1C0	14	A	6	nc	16	nc
7	1Y	15	$2\overline{G}$	7	1C1	17	2C3
8	GND	16	V_{CC}	8	1C0	18	A
				9	1Y	19	$2\overline{G}$
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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353

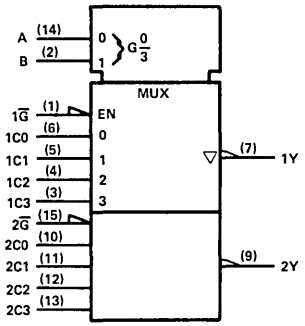
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS
(three-state outputs, inverting version of 'LS253

typical performance

TYPE	DELAY TIMES: DATA TO INV OUTPUT	DELAY TIMES: FROM ENABLE	TOTAL POWER
'ALS353	6 ns	4.5 ns	40 mW
'AS353	2.7 ns	5.5 ns	130 mW
'LS353	12 ns	13 ns	43 mW

SN54ALS353 (J,FH) SN74ALS353 (N,FN)
SN54AS353 (J,FH) SN74AS353 (N,FN)
SN54LS353 (J,FH) SN74LS353 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1$\overline{G}$	9	2Y	1	nc	11	nc
2	B	10	2C0	2	1$\overline{G}$	12	2Y
3	1C3	11	2C1	3	B	13	2C0
4	1C2	12	2C2	4	1C3	14	2C1
5	1C1	13	2C3	5	1C2	15	2C2
6	1C0	14	A	6	nc	16	nc
7	1Y	15	2$\overline{G}$	7	1C1	17	2C3
8	GND	16	V_{CC}	8	1C0	18	A
				9	1Y	19	2$\overline{G}$
				10	GND	20	V_{CC}

354

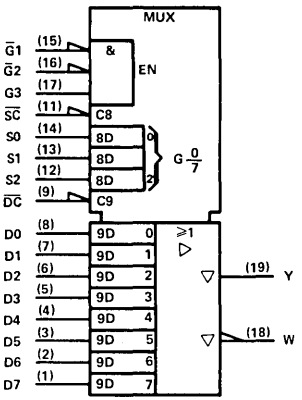
8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/ TRANSPARENT REGISTERS
(three-state outputs)

typical performance

TYPE	DELAY TIMES: DATA TO INV OUTPUT	DELAY TIMES: DATA TO NON-INV OUTPUT	DELAY TIMES: FROM ENABLE
'LS354	23.5 ns	23.5 ns	16 ns

SN54LS354 (J,FH) SN74LS354 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	D7	11	$\overline{SC}$	1	D7	11	$\overline{SC}$
2	D6	12	S2	2	D6	12	S2
3	D5	13	S1	3	D5	13	S1
4	D4	14	S0	4	D4	14	S0
5	D3	15	1$\overline{G}$	5	D3	15	1$\overline{G}$
6	D2	16	2$\overline{G}$	6	D2	16	2$\overline{G}$
7	D1	17	G3	7	D1	17	G3
8	D0	18	W	8	D0	18	W
9	$\overline{DC}$	19	Y	9	$\overline{DC}$	19	Y
10	GND	20	V_{CC}	10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

355

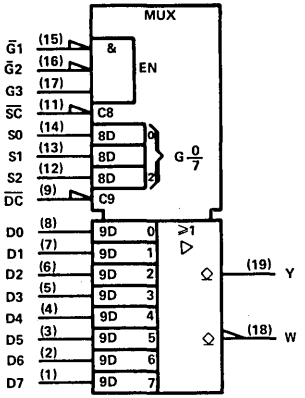
8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/ TRANSPARENT REGISTERS
(open-collector outputs)

typical performance

DELAY TIMES		
DATA TO INV OUTPUT	DATA TO NON-INV OUTPUT	FROM ENABLE
31.5 ns	30 ns	21.5 ns

SN54LS355 (J,FH) SN74LS355 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	D7	11	$\overline{SC}$	1	D7	11	$\overline{SC}$
2	D6	12	S2	2	D6	12	S2
3	D5	13	S1	3	D5	13	S1
4	D4	14	S0	4	D4	14	S0
5	D3	15	$\overline{G1}$	5	D3	15	$\overline{G1}$
6	D2	16	$\overline{G2}$	6	D2	16	$\overline{G2}$
7	D1	17	G3	7	D1	17	G3
8	D0	18	W	8	D0	18	W
9	$\overline{DC}$	19	Y	9	$\overline{DC}$	19	Y
10	GND	20	V_{CC}	10	GND	20	V_{CC}

356

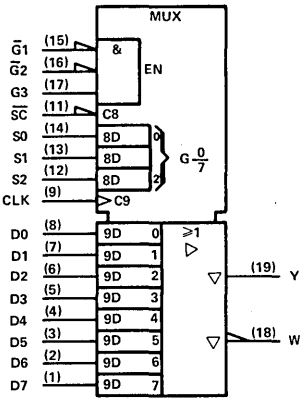
8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/ EDGE-TRIGGERED REGISTERS
(three-state output)

typical performance

DELAY TIMES		
DATA TO INV OUTPUT	DATA TO NON-INV OUTPUT	FROM ENABLE
23.5 ns	23.5 ns	16 ns

SN54LS356 (J,FH) SN74LS356 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	D7	11	$\overline{SC}$	1	D7	11	$\overline{SC}$
2	D6	12	S2	2	D6	12	S2
3	D5	13	S1	3	D5	13	S1
4	D4	14	S0	4	D4	14	S0
5	D3	15	$\overline{G1}$	5	D3	15	$\overline{G1}$
6	D2	16	$\overline{G2}$	6	D2	16	$\overline{G2}$
7	D1	17	G3	7	D1	17	G3
8	D0	18	W	8	D0	18	W
9	CLK	19	Y	9	CLK	19	Y
10	GND	20	V_{CC}	10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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357

8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/ EDGE-TRIGGERED REGISTERS

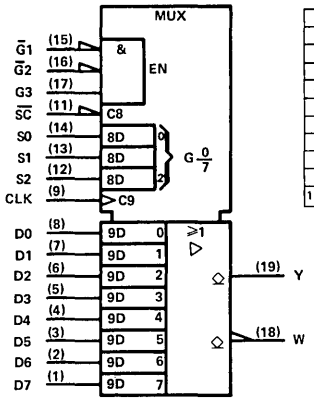
(open-collector outputs)

typical performance

DELAY TIMES		
DATA TO INV OUTPUT	DATA TO NON-INV OUTPUT	FROM ENABLE
31.5 ns	30 ns	25 ns

SN544LS357 (J,FH) SN74LS357 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	D7	11	$\overline{SC}$	1	D7	11	$\overline{SC}$
2	D6	12	S2	2	D6	12	S2
3	D5	13	S1	3	D5	13	S1
4	D4	14	S0	4	D4	14	S0
5	D3	15	$\overline{G1}$	5	D3	15	$\overline{G1}$
6	D2	16	$\overline{G2}$	6	D2	16	$\overline{G2}$
7	D1	17	G3	7	D1	17	G3
8	D0	18	W	8	D0	18	W
9	CLK	19	Y	9	CLK	19	Y
10	GND	20	V_{CC}	10	GND	20	V_{CC}

365

HEX BUS DRIVERS

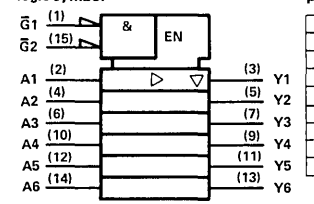
(non-inverted three-state outputs, gated enable inputs)

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSIPATION
SN54365A	12 ns	−2 mA	32 mA	325 mW
SN74365A	12 ns	−5.2 mA	32 mA	325 mW
SN54ALS365	7 ns	−12 mA	12 mA	53 mW
SN74ALS365	7 ns	−15 mA	24 mA	53 mW
SN74ALS365-1	7 ns	−15 mA	48 mA	53 mW
SN54LS365A	9.5 ns	−1 mA	12 mA	70 mW
SN74LS365A	9.5 ns	−2.6 mA	24 mA	70 mW

SN54365A (J,FH) SN74365A (J,N) SN74ALS365-1 (N,FN)
SN54ALS365 (J,FH) SN74ALS365 (N,FN) **SN54LS365A (J,FH)** SN74LS365A (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{G1}$	9	Y4	1	nc	11	nc
2	A1	10	A4	2	$\overline{G1}$	12	Y4
3	Y1	11	Y5	3	A1	13	A4
4	A2	12	A5	4	Y1	14	Y5
5	Y2	13	Y6	5	A2	15	A5
6	A3	14	A6	6	nc	16	nc
7	Y3	15	$\overline{G2}$	7	Y2	17	Y6
8	GND	16	V_{CC}	8	A3	18	A6
				9	Y3	19	$\overline{G2}$
				10	GND	20	V_{CC}

366

HEX BUS DRIVERS

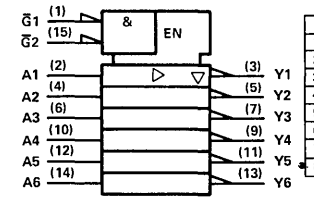
(inverted three-state outputs, gated enable inputs)

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSIPATION
SN54ALS366	5.5 ns	−12 mA	12 mA	40 mW
SN74ALS366	5.5 ns	−15 mA	24 mA	40 mW
SN74ALS366-1	5.5 ns	−15 mA	48 mA	40 mW
SN54366A	11 ns	−2 mA	32 mA	295 mW
SN74366A	11 ns	−5.2 mA	32 mA	295 mW
SN54LS366A	9.5 ns	−1 mA	12 mA	60 mW
SN74LS366A	9.5 ns	−2.6 mA	24 mA	60 mW

SN54366A (J,FH) SN74366A (J,N) SN74ALS366-1 (N,FN)
SN54ALS366 (J,FC) SN74ALS366 (N,FN) SN54LS366A (J,FH) SN74LS366A (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{G1}$	9	Y4	1	nc	11	nc
2	A1	10	A4	2	$\overline{G1}$	12	Y4
3	Y1	11	Y5	3	A1	13	A4
4	A2	12	A5	4	Y1	14	Y5
5	Y2	13	Y6	5	A2	15	A5
6	A3	14	A6	6	nc	16	nc
7	Y3	15	$\overline{G2}$	7	Y2	17	Y6
8	GND	16	V_{CC}	8	A3	18	A6
				9	Y3	19	$\overline{G2}$
				10	GND	20	V_{CC}

nc — no internal connection.
†Pin numbers shown on logic symbols are for J and N packages only.

367

HEX BUS DRIVERS

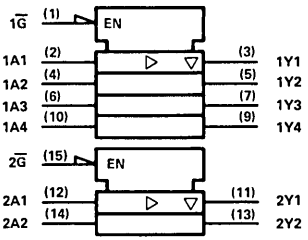
(non-inverted three-state outputs organized to facilitate handling of 4-bit data)

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSIPATION
SN54ALS367	7 ns	−12 mA	12 mA	53 mW
SN74ALS367	7 ns	−15 mA	24 mA	53 mW
SN74ALS367-1	7 ns	−15 mA	48 mA	53 mW
SN54367A	12 ns	−2 mA	32 mA	325 mW
SN74367A	12 ns	−5.2 mA	32 mA	325 mW
SN54LS367A	9.5 ns	−1 mA	12 mA	70 mW
SN74LS367A	9.5 ns	−2.6 mA	24 mA	70 mW

SN54367A (J,FH) SN74367A (J,N)
SN54ALS367 (J,FH) SN74ALS367 (N,FN)
SN74ALS367-1 (N,FN)
SN54LS367A (J,FH) SN74LS367A (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1G	9	1Y4	1	nc	11	nc
2	1A1	10	1A4	2	1G	12	1Y4
3	1Y1	11	2Y1	3	1A1	13	1A4
4	1A2	12	2A1	4	1Y1	14	2Y1
5	1Y2	13	2Y2	5	1A2	15	2A1
6	1A3	14	2A2	6	nc	16	nc
7	1Y3	15	2G	7	1Y2	17	2Y2
8	GND	16	V_{CC}	8	1A3	18	2A2
				9	1Y3	19	2G
				10	GND	20	V_{CC}

368

HEX BUS DRIVERS

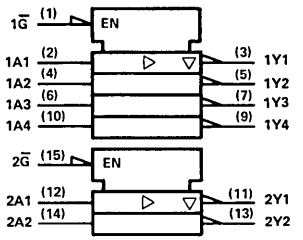
(inverted three-state outputs organized to facilitate handling of 4-bit data)

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSIPATION
SN54ALS368	5.5 ns	−12 mA	12 mA	40 mW
SN74ALS368	5.5 ns	−15 mA	24 mA	40 mW
SN74ALS368-1	5.5 ns	−15 mA	48 mA	40 mW
SN54368A	11 ns	−2 mA	32 mA	295 mW
SN74368A	11 ns	−5.2 mA	32 mA	295 mW
SN54LS368A	9.5 ns	−1 mA	12 mA	60 mW
SN74LS368A	9.5 ns	−2.6 mA	24 mA	60 mW

SN54368A (J,FH) SN74368A (J,N)
SN54ALS368 (J,FH) SN74ALS368 (N,FN)
SN74ALS368-1 (N,FN)
SN54LS368A (J,FH) SN74LS368A (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1G	9	1Y4	1	nc	11	nc
2	1A1	10	1A4	2	1G	12	1Y4
3	1Y1	11	2Y1	3	1A1	13	1A4
4	1A2	12	2A1	4	1Y1	14	2Y1
5	1Y2	13	2Y2	5	1A2	15	2A1
6	1A3	14	2A2	6	nc	16	nc
7	1Y3	15	2G	7	1Y2	17	2Y2
8	GND	16	V_{CC}	8	1A3	18	2A2
				9	1Y3	19	2G
				10	GND	20	V_{CC}

370

2048-BIT READ-ONLY MEMORIES

(512 4-bit words; three-state outputs)

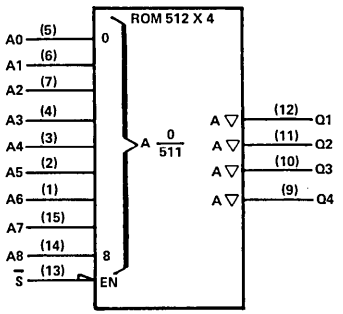
typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER/ BIT
'S370	45 ns	15 ns	0.26 mW

SN54S370 (J) SN74S370 (J,N)

This product is no longer in production.

logic symbol†



pin assignments

J, N PACKAGES			
1	A6	9	Q4
2	A5	10	Q3
3	A4	11	Q2
4	A3	12	Q1
5	A0	13	$\overline{S}$
6	A1	14	A8
7	A2	15	A7
8	GND	16	V_{CC}

For chip carrier information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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371

2048-BIT READ-ONLY MEMORIES
(256 8-bit words; three-state outputs)

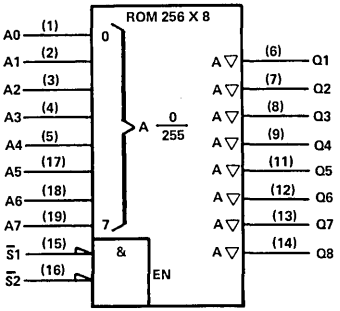
typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER/ BIT
'S371	45 ns	15 ns	0.26 mW

SN54S371 (J,FH) SN74S371 (J,N,FN)

This product is no longer in production.

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A0	11	Q5	1	A0	11	Q5
2	A1	12	Q6	2	A1	12	Q6
3	A2	13	Q7	3	A2	13	Q7
4	A3	14	Q8	4	A3	14	Q8
5	A4	15	S̄1	5	A4	15	S̄1
6	Q1	16	S̄2	6	Q1	16	S̄2
7	Q2	17	A5	7	Q2	17	A5
8	Q3	18	A6	8	Q3	18	A6
9	Q4	19	A7	9	Q4	19	A7
10	GND	20	V_{CC}	10	GND	20	V_{CC}

373

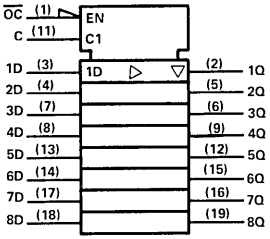
OCTAL D-TYPE LATCHES
(three-state outputs, common output control, common enable)

typical performance

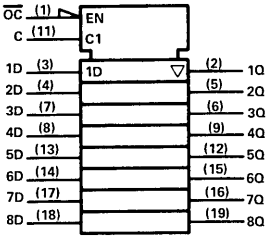
TYPE	OUTPUTS	DELAY	TOTAL POWER
'ALS373	Q	8 ns	70 mW
'AS373			
'LS373	Q	19 ns	120 mW
'S373	Q	7 ns	525 mW

SN54ALS373 (J,FH) SN74ALS373 (N,FN)
SN54AS373 (J,FH) SN74AS373 (N,FN)
SN54LS373 (J,FH) SN74LS373 (J,N,FN)
SN54S373 (J,FH) SN74S373 (J,N,FN)

logic symbol, 'LS373, 'ALS373, 'AS373†



logic symbol, 'S373†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	OC	11	C	1	OC	11	C
2	1Q	12	5Q	2	1Q	12	5Q
3	1D	13	5D	3	1D	13	5D
4	2D	14	6D	4	2D	14	6D
5	2Q	15	6Q	5	2Q	15	6Q
6	3Q	16	7Q	6	3Q	16	7Q
7	3D	17	7D	7	3D	17	7D
8	4D	18	8D	8	4D	18	8D
9	4Q	19	8Q	9	4Q	19	8Q
10	GND	20	V_{CC}	10	GND	20	V_{CC}

6

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

374

OCTAL D-TYPE FLIP-FLOPS
(three-state outputs, common output control, common clock)

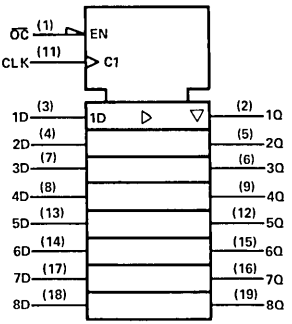
typical performance

TYPE	FREQ	POWER PER F-F	DATA TIMES SET-UP	DATA TIMES HOLD
'ALS374	50 MHz	10 mW		
'AS374				
'LS374	50 MHz	17 mW	20 ns†	0 ns†
'S374	100 MHz	56 mW	5 ns†	2 ns†

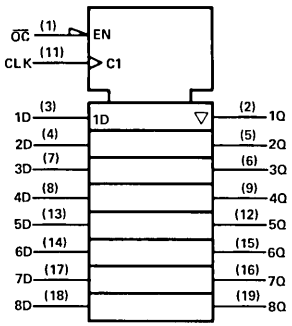
† Rising edge of clock pulse

SN54ALS374 (J,FH) SN74ALS374 (N,FN)
SN54AS374 (J,FH) SN74AS374 (N,FN)
SN54LS374 (J,FH) SN74LS374 (J,N,FN)
SN54S374 (J,FH) SN74S374 (J,N,FN)

logic symbol, 'LS374, 'ALS374, 'AS374



logic symbol, 'S374†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{OC}$	11	CLK	1	$\overline{OC}$	11	CLK
2	1Q	12	5Q	2	1Q	12	5Q
3	1D	13	5D	3	1D	13	5D
4	2D	14	6D	4	2D	14	6D
5	2Q	15	6Q	5	2Q	15	6Q
6	3Q	16	7Q	6	3Q	16	7Q
7	3D	17	7D	7	3D	17	7D
8	4D	18	8D	8	4D	18	8D
9	4Q	19	8Q	9	4Q	19	8Q
10	GND	20	V_{CC}	10	GND	20	V_{CC}

375

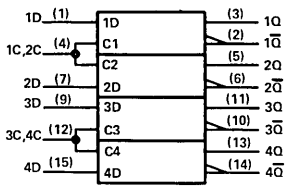
4-BIT BISTABLE LATCHES

typical performance

OUTPUTS	DELAY	TOTAL POWER
Q,$\overline{Q}$	12 ns	32 mW

SN54LS375 (J,FH) SN74LS375 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1D	9	3D	1	nc	11	nc
2	1Q̄	10	3Q̄	2	1D	12	3D
3	1Q	11	3Q	3	1Q̄	13	3Q̄
4	1C,2C	12	3C,4C	4	1Q	14	3Q
5	2Q	13	4Q	5	1C,2C	15	3C,4C
6	2Q̄	14	4Q̄	6	nc	16	nc
7	2D	15	4D	7	2Q	17	4Q
8	GND	16	V_{CC}	8	2Q̄	18	4Q̄
				9	2D	19	4D
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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376

QUAD J-$\overline{K}$ FLIP-FLOPS
(common clock, common clear)

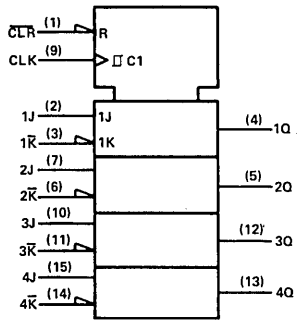
typical performance

FREQ	POWER PER F-F	DATA TIMES SET-UP	DATA TIMES HOLD
45 MHz	65 mW	0 ns†	20 ns†

† Rising edge of clock pulse

SN54376 (J,FH) SN74376 (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	$\overline{CLR}$	9	CLK	1	nc	11	nc
2	1J	10	3J	2	$\overline{CLR}$	12	CLK
3	1$\overline{K}$	11	3$\overline{K}$	3	1J	13	3J
4	1Q	12	3Q	4	1$\overline{K}$	14	3$\overline{K}$
5	2Q	13	4Q	5	1Q	15	3Q
6	2$\overline{K}$	14	4$\overline{K}$	6	nc	16	nc
7	2J	15	4J	7	2Q	17	4Q
8	GND	16	V_{CC}	8	2$\overline{K}$	18	4$\overline{K}$
				9	2J	19	4J
				10	GND	20	V_{CC}

377

OCTAL D-TYPE FLIP-FLOPS
(single-rail outputs, common enable, common clock)

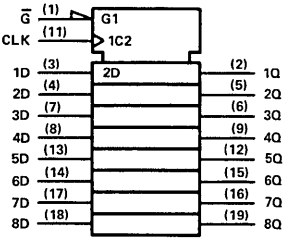
typical performance

FREQ	POWER PER F-F	DATA TIMES SET-UP	DATA TIMES HOLD
40 MHz	10.6 mW	20 ns†	5 ns†

† Rising edge of clock pulse

SN54LS377 (J,FH) SN74LS377 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{G}$	11	CLK	1	$\overline{G}$	11	CLK
2	1Q	12	5Q	2	1Q	12	5Q
3	1D	13	5D	3	1D	13	5D
4	2D	14	6D	4	2D	14	6D
5	2Q	15	6Q	5	2Q	15	6Q
6	3Q	16	7Q	6	3Q	16	7Q
7	3D	17	7D	7	3D	17	7D
8	4D	18	8D	8	4D	18	8D
9	4Q	19	8Q	9	4Q	19	8Q
10	GND	20	V_{CC}	10	GND	20	V_{CC}

378

HEX D-TYPE FLIP-FLOPS
(single-rail outputs, common enable, common clock)

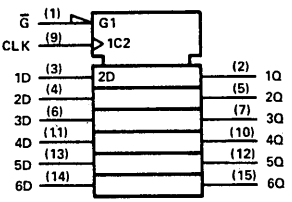
typical performance

FREQ	POWER PER F-F	DATA TIMES SET-UP	DATA TIMES HOLD
40 MHz	10.6 mW	20 ns†	5 ns†

† Rising edge of clock pulse

SN54LS378 (J,FH) SN74LS378 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{G}$	9	CLK	1	nc	11	nc
2	1Q	10	4Q	2	$\overline{G}$	12	CLK
3	1D	11	4D	3	1Q	13	4Q
4	2D	12	5Q	4	1D	14	4D
5	2Q	13	5D	5	2D	15	5Q
6	3D	14	6D	6	nc	16	nc
7	3Q	15	6Q	7	2Q	17	5D
8	GND	16	V_{CC}	8	3D	18	6D
				9	3Q	19	6Q
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

379

QUAD D-TYPE FLIP-FLOPS
(double-rail outputs, common enable, common clock)

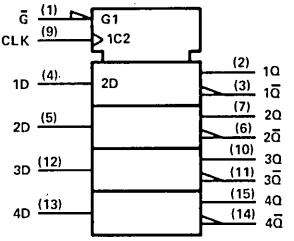
typical performance

FREQ	POWER PER F-F	DATA TIMES SET-UP	DATA TIMES HOLD
40 MHz	10.6 mW	20 ns†	5 ns†

† Rising edge of clock pulse

SN54LS379 (J,FH)
SN74LS379 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{G}$	9	CLK	1	nc	11	nc
2	1Q	10	3Q	2	$\overline{G}$	12	CLK
3	1$\overline{Q}$	11	3$\overline{Q}$	3	1Q	13	3Q
4	1D	12	3D	4	1$\overline{Q}$	14	3$\overline{Q}$
5	2D	13	4D	5	1D	15	3D
6	2$\overline{Q}$	14	4$\overline{Q}$	6	nc	16	nc
7	2Q	15	4Q	7	2D	17	4D
8	GND	16	V_{CC}	8	2$\overline{Q}$	18	4$\overline{Q}$
				9	2Q	19	4Q
				10	GND	20	V_{CC}

381

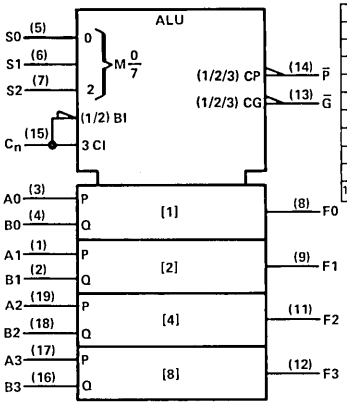
ARITHMETIC LOGIC UNITS/ FUNCTION GENERATORS
(8 binary functions, use 'S182 for look-ahead carry)

typical performance

TYPE	CARRY TIME	ADD TIME	TOTAL POWER
'LS381	16 ns	21 ns	175 mW
'S381	11 ns	20 ns	525 mW

SN54LS381 (J,FH)
SN54S381 (J,FH)
SN74LS381 (J,N,FN)
SN74S381 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A1	11	F2	1	A1	11	F2
2	B1	12	F3	2	B1	12	F3
3	A0	13	$\overline{G}$	3	A0	13	$\overline{G}$
4	B0	14	$\overline{P}$	4	B0	14	$\overline{P}$
5	S0	15	C_n	5	S0	15	C_n
6	S1	16	B3	6	S1	16	B3
7	S2	17	A3	7	S2	17	A3
8	F0	18	B2	8	F0	18	B2
9	F1	19	A2	9	F1	19	A2
10	GND	20	V_{CC}	10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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382

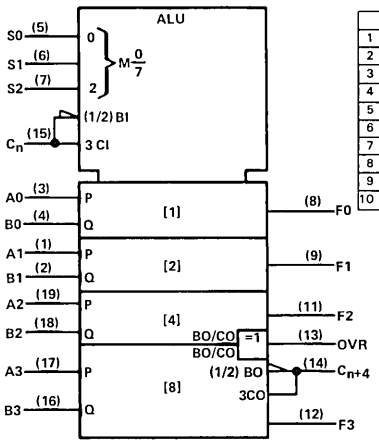
ARITHMETIC LOGIC UNITS/ FUNCTION GENERATORS
(ripple carry and overflow outputs)

typical performance

TYPE	CARRY TIME	ADD TIME	TOTAL POWER
'LS382	27 ns	18 ns	175 mW

SN54LS382 (J,FH)
SN74LS382 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A1	11	F2	1	A1	11	F2
2	B1	12	F3	2	B1	12	F3
3	A0	13	OVR	3	A0	13	OVR
4	B0	14	C_{n+4}	4	B0	14	C_{n+4}
5	S0	15	C_n	5	S0	15	C_n
6	S1	16	B3	6	S1	16	B3
7	S2	17	A3	7	S2	17	A3
8	F0	18	B2	8	F0	18	B2
9	F1	19	A2	9	F1	19	A2
10	GND	20	V_{CC}	10	GND	20	V_{CC}

384

8-BIT BY 1-BIT TWO'S-COMPLEMENT MULTIPLIERS

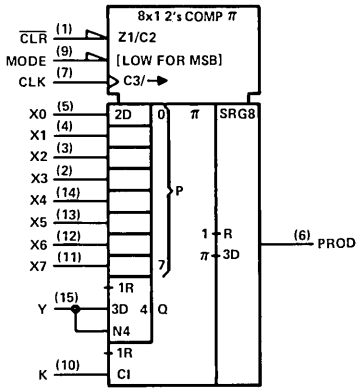
- Magnitude-only multiplication
- Cascadable for any number of bits
- Serial multiplier data input
- Serial data output for multiplication product
- 8-Bit parallel multiplicand data input
- 40 MHz typical max clock frequency

typical performance

MAX CLOCK FREQ	DELAY FROM CLOCK	DELAY FROM CLEAR	TOTAL POWER
40 MHz	15 ns	17 ns	455 mW

SN54LS384 (J,FH)
SN74LS384 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	CLR	9	MODE	1	nc	11	nc
2	X3	10	K	2	CLR	12	MODE
3	X2	11	X7	3	X3	13	K
4	X1	12	X6	4	X2	14	X7
5	X0	13	X5	5	X1	15	X6
6	PROD	14	X4	6	nc	16	nc
7	CLK	15	Y	7	X0	17	X5
8	GND	16	V_{CC}	8	PROD	18	X4
				9	CLK	19	Y
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

385

QUADRUPLE SERIAL ADDERS/ SUBTRACTORS

- Buffered clock, direct clear inputs
- Independent two's-complement addition/subtraction

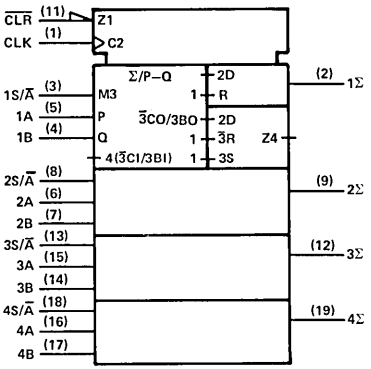
typical performance

f_{max}	DELAY	POWER
40 MHz	16 ns	240 mW

SN54LS385 (J,FH)

SN74LS385 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	CLK	11	CLR	1	CLK	11	CLR
2	1Σ	12	3Σ	2	1Σ	12	3Σ
3	1S/$\overline{A}$	13	3S/$\overline{A}$	3	1S/$\overline{A}$	13	3S/$\overline{A}$
4	1B	14	3B	4	1B	14	3B
5	1A	15	3A	5	1A	15	3A
6	2A	16	4A	6	2A	16	4A
7	2B	17	4B	7	2B	17	4B
8	2S/$\overline{A}$	18	4S/$\overline{A}$	8	2S/$\overline{A}$	18	4S/$\overline{A}$
9	2Σ	19	4Σ	9	2Σ	19	4Σ
10	GND	20	V_{CC}	10	GND	20	V_{CC}

386

QUAD 2-INPUT EXCLUSIVE-OR GATES

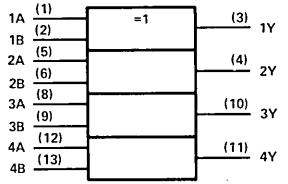
typical performance

TYPE	DELAY	TOTAL POWER
'LS386	10 ns	30 mW

SN54LS386 (J,FH)

SN74LS386 (J,N,FN)

logic symbol†



positive logic: $Y = A \oplus B = \overline{A}B + A\overline{B}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3A	1	nc	11	nc
2	1B	9	3B	2	1A	12	3A
3	1Y	10	3Y	3	1B	13	3B
4	2Y	11	4Y	4	1Y	14	3Y
5	2A	12	4A	5	nc	15	nc
6	2B	13	4B	6	2Y	16	4Y
7	GND	14	V_{CC}	7	nc	17	nc
				8	2A	18	4A
				9	2B	19	4B
				10	GND	20	V_{CC}

387

(This number has been changed to TBP14SA10. Product Guide information for this PROM can be found at the end of this section.)

† Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

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390

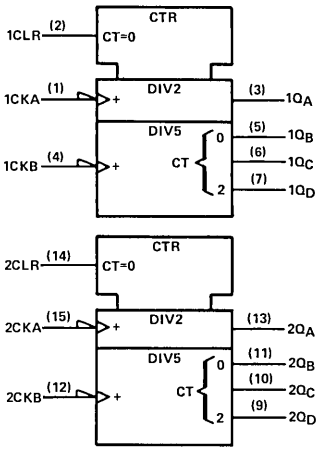
DUAL DECADE COUNTERS
(bi-quinary or bcd sequences)

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'390	25 MHz	HIGH	210 mW
'LS390	35 MHz	HIGH	75 mW

SN54390 (J,FH) SN74390 (J,N)
SN54LS390 (J,FH) SN74LS390 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1CKA	9	$2Q_D$	1	nc	11	nc
2	1CLR	10	$2Q_C$	2	1CKA	12	$2Q_D$
3	$1Q_A$	11	$2Q_B$	3	1CLR	13	$2Q_C$
4	1CKB	12	2CKB	4	$1Q_A$	14	$2Q_B$
5	$1Q_B$	13	$2Q_A$	5	1CKB	15	2CKB
6	$1Q_C$	14	2CLR	6	nc	16	nc
7	$1Q_D$	15	2CKA	7	$1Q_B$	17	$2Q_A$
8	GND	16	V_{CC}	8	$1Q_C$	18	2CLR
				9	$1Q_D$	19	2CKA
				10	GND	20	V_{CC}

393

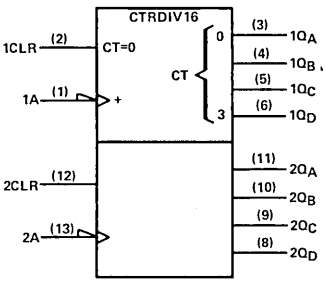
DUAL 4-BIT BINARY COUNTERS

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'393	25 MHz	HIGH	190 mW
'LS393	35 MHz	HIGH	75 mW

SN54393 (J,FH) SN74393 (J,N)
SN54LS393 (J,FH) SN74LS393 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	$2Q_D$	1	nc	11	nc
2	1CLR	9	$2Q_C$	2	1A	12	$2Q_D$
3	$1Q_A$	10	$2Q_B$	3	1CLR	13	$2Q_C$
4	$1Q_B$	11	$2Q_A$	4	$1Q_A$	14	$2Q_B$
5	$1Q_C$	12	2CLR	5	nc	15	nc
6	$1Q_D$	13	2A	6	$1Q_B$	16	$2Q_A$
7	GND	14	V_{CC}	7	nc	17	nc
				8	$1Q_C$	18	2CLR
				9	$1Q_D$	19	2A
				10	GND	20	V_{CC}

395

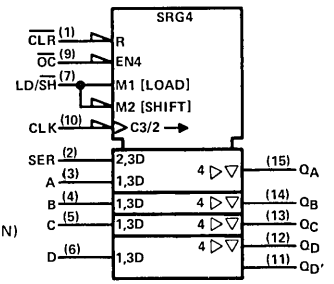
4-BIT UNIVERSAL SHIFT REGISTERS
(three-state outputs)

typical performance

SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
30 MHz	D	LOW	75 mW

SN54LS395A (J,FH) SN74LS395A (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{CLR}$	9	$\overline{OC}$	1	nc	11	nc
2	SER	10	CLK	2	$\overline{CLR}$	12	$\overline{OC}$
3	A	11	$Q_{D'}$	3	SER	13	CLK
4	B	12	Q_D	4	A	14	$Q_{D'}$
5	C	13	Q_C	5	B	15	Q_D
6	D	14	Q_B	6	nc	16	nc
7	LD/$\overline{SH}$	15	Q_A	7	C	17	Q_C
8	GND	16	V_{CC}	8	D	18	Q_B
				9	LD/$\overline{SH}$	19	Q_A
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

396

OCTAL STORAGE REGISTERS

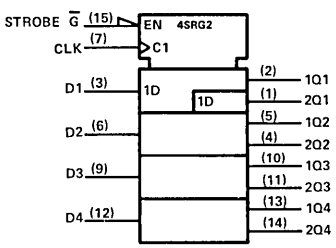
- Parallel access
- Applications:
  - N-bit storage files
  - HEX/BCD serial to parallel converters

typical performance

TYPE	MAX CLOCK FREQ	DELAY	POWER
'LS396	30 MHz	20 ns	120 mW

SN54LS396 (J,FH) SN74LS396 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	2Q1	9	D3	1	nc	11	nc
2	1Q1	10	1Q3	2	2Q1	12	D3
3	D1	11	2Q3	3	1Q1	13	1Q3
4	2Q2	12	D4	4	D1	14	2Q3
5	1Q2	13	1Q4	5	2Q2	15	D4
6	D2	14	2Q4	6	nc	16	nc
7	CLK	15	$\overline{G}$	7	1Q2	17	1Q4
8	GND	16	V_{CC}	8	D2	18	2Q4
				9	CLK	19	$\overline{G}$
				10	GND	20	V_{CC}

398

QUAD 2-INPUT MULTIPLEXERS WITH STORAGE

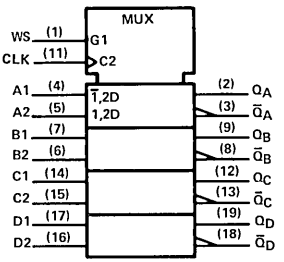
(double-rail outputs)

typical performance

TYPE	DELAY TIMES		TOTAL POWER
	CLOCK TO INV OUTPUT	CLOCK TO NON-INV OUTPUT	
'LS398	20 ns	20 ns	32 mW

SN54LS398 (J,FH) SN74LS398 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	WS	11	CLK	1	WS	11	CLK
2	Q_A	12	Q_C	2	Q_A	12	Q_C
3	$\overline{Q}_A$	13	$\overline{Q}_C$	3	$\overline{Q}_A$	13	$\overline{Q}_C$
4	A1	14	C1	4	A1	14	C1
5	A2	15	C2	5	A2	15	C2
6	B2	16	D2	6	B2	16	D2
7	B1	17	D1	7	B1	17	D1
8	$\overline{Q}_B$	18	$\overline{Q}_D$	8	$\overline{Q}_B$	18	$\overline{Q}_D$
9	Q_B	19	Q_D	9	Q_B	19	Q_D
10	GND	20	V_{CC}	10	GND	20	V_{CC}

399

QUAD 2-INPUT MULTIPLEXERS WITH STORAGE

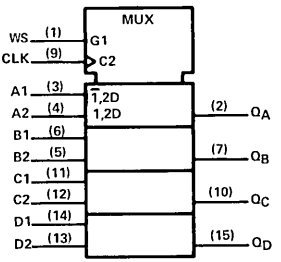
typical performance

TYPE	DELAY	TOTAL POWER
'LS399	20 ns*	37 mW

* From clock to output

SN54LS399 (J,FH) SN74LS399 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	WS	9	CLK	1	nc	11	nc
2	Q_A	10	Q_C	2	WS	12	CLK
3	A1	11	C1	3	Q_A	13	Q_C
4	A2	12	C2	4	A1	14	C1
5	B2	13	D2	5	A2	15	C2
6	B1	14	D1	6	nc	16	nc
7	Q_B	15	Q_D	7	B2	17	D2
8	GND	16	V_{CC}	8	B1	18	D1
				9	Q_B	19	Q_D
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

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412

MULTI-MODE BUFFERED 8-BIT LATCHES

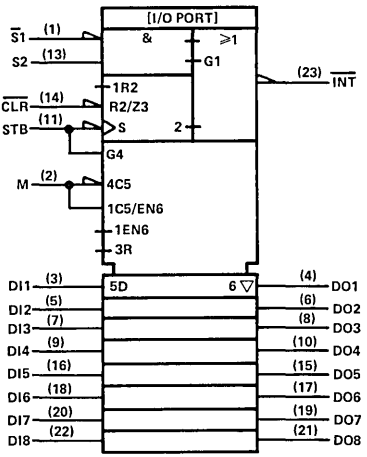
(three-state outputs; direct clear)

typical performance

CLEAR	OUTPUTS	DELAY	TOTAL POWER
LOW	Q	11 ns	410 mW

SN54S412 (J,FH) SN74S412 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{S1}$	13	S2	1	nc	15	nc
2	M	14	$\overline{CLR}$	2	$\overline{S1}$	16	S2
3	DI1	15	DO5	3	M	17	$\overline{CLR}$
4	DO1	16	DI5	4	DI1	18	DO5
5	DI2	17	DO6	5	DO1	19	DI5
6	DO2	18	DI6	6	DI2	20	DO6
7	DI3	19	DO7	7	DO2	21	DI6
8	DO3	20	DI7	8	nc	22	nc
9	DI4	21	DO8	9	DI3	23	DO7
10	DO4	22	DI8	10	DO3	24	DI7
11	STB	23	$\overline{INT}$	11	DI4	25	DO8
12	GND	24	V_{CC}	12	DO4	26	DI8
				13	STB	27	$\overline{INT}$
				14	GND	28	V_{CC}

422

RE-TRIGGERABLE MONOSTABLE MULTIVIBRATORS

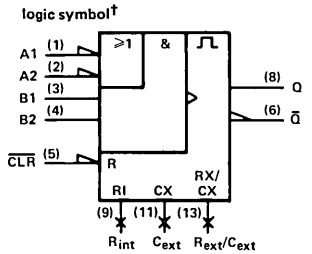
- Internal timing resistor
- Up to 100% duty cycle
- Will not trigger from clear

typical performance

NO. OF INPUTS		OUTPUT PULSE RANGE	TOTAL POWER
HIGH	LOW		
2	2	40 ns-∞	30 mW

SN54LS422 (J,FH) SN74LS422 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A1	8	Q	1	nc	11	nc
2	A2	9	R_{int}	2	A1	12	Q
3	B1	10	nc	3	A2	13	R_{int}
4	B2	11	C_{ext}	4	B1	14	nc
5	$\overline{CLR}$	12	nc	5	nc	15	nc
6	Q̄	13	R_{ext}/C_{ext}	6	B2	16	C_{ext}
7	GND	14	V_{CC}	7	nc	17	nc
				8	$\overline{CLR}$	18	nc
				9	Q̄	19	R_{ext}/C_{ext}
				10	GND	20	V_{CC}

423

RE-TRIGGERABLE MONOSTABLE MULTIVIBRATORS

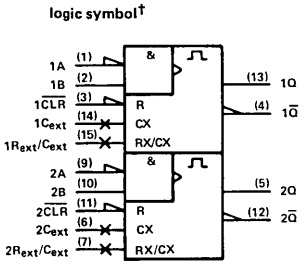
- Up to 100% duty cycle
- Will not trigger from clear

typical performance

NO. OF INPUTS		OUTPUT PULSE RANGE	TOTAL POWER
HIGH	LOW		
1	1	40 ns-∞	60 mW

SN54LS423 (J,FH) SN74LS423 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	9	2A	1	nc	11	nc
2	1B	10	2B	2	1A	12	2A
3	$1\overline{CLR}$	11	$2\overline{CLR}$	3	1B	13	2B
4	1Q̄	12	2Q̄	4	$1\overline{CLR}$	14	$2\overline{CLR}$
5	2Q	13	1Q	5	1Q̄	15	2Q̄
6	$2C_{ext}$	14	$1C_{ext}$	6	nc	16	nc
7	$2R_{ext}/C_{ext}$	15	$1R_{ext}/C_{ext}$	7	2Q	17	1Q
8	GND	16	V_{CC}	8	$2C_{ext}$	18	$1C_{ext}$
				9	$2R_{ext}/C_{ext}$	19	$1R_{ext}/C_{ext}$
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

425

QUAD GATES

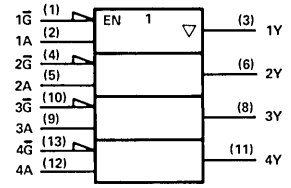
(three-state outputs, active-low enabling)

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54425	10 ns	−2 mA	16 mA
SN74425	10 ns	−5.2 mA	16 mA

SN54425 (J,FH) SN74425 (J,N)

logic symbol†



positive logic: Y = A

pin assignments

J, N PACKAGES				FH PACKAGE			
1	1G̅	8	3Y	1	nc	11	nc
2	1A	9	3A	2	1G̅	12	3Y
3	1Y	10	3G̅	3	1A	13	3A
4	2G̅	11	4Y	4	1Y	14	3G̅
5	2A	12	4A	5	nc	15	nc
6	2Y	13	4G̅	6	2G̅	16	4Y
7	GND	14	V_{CC}	7	nc	17	nc
				8	2A	18	4A
				9	2Y	19	4G̅
				10	GND	20	V_{CC}

426

QUAD GATES

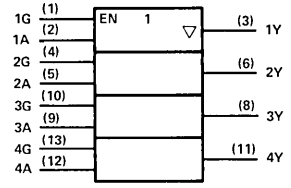
(three-state outputs, active-high enabling)

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54426	10 ns	−2 mA	16 mA
SN74426	10 ns	−5.2 mA	16 mA

SN54426 (J,FH) SN74426 (J,N)

logic symbol†



positive logic: Y = A

pin assignments

J, N PACKAGES				FH PACKAGE			
1	1G	8	3Y	1	nc	11	nc
2	1A	9	3A	2	1G	12	3Y
3	1Y	10	3G	3	1A	13	3A
4	2G	11	4Y	4	1Y	14	3G
5	2A	12	4A	5	nc	15	nc
6	2Y	13	4G	6	2G	16	4Y
7	GND	14	V_{CC}	7	nc	17	nc
				8	2A	18	4A
				9	2Y	19	4G
				10	GND	20	V_{CC}

428, 438

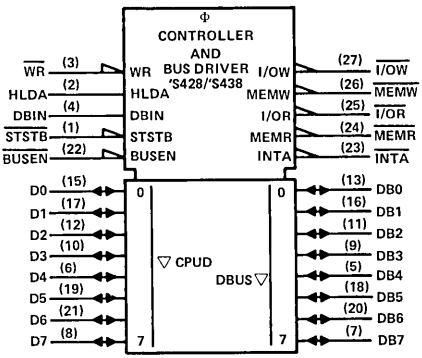
SYSTEM CONTROLLER FOR 8080A

typical performance

TYPE	POWER
'S428	700 mW
'S438	700 mW

SN74S428 (J,N,FN)
SN74S438 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FN PACKAGE			
1	STSTB	15	D0	1	STSTB	15	D0
2	HLDA	16	DB1	2	HLDA	16	DB1
3	WR	17	D1	3	WR	17	D1
4	DBIN	18	DB5	4	DBIN	18	DB5
5	DB4	19	D5	5	DB4	19	D5
6	D4	20	DB6	6	D4	20	DB6
7	DB7	21	D6	7	DB7	21	D6
8	D7	22	BUSEN	8	D7	22	BUSEN
9	DB3	23	INTA	9	DB3	23	INTA
10	D3	24	MEMR	10	D3	24	MEMR
11	DB2	25	I/OR	11	DB2	25	I/OR
12	D2	26	MEMW	12	D2	26	MEMW
13	DB0	27	I/OW	13	DB0	27	I/OW
14	GND	28	V_{CC}	14	GND	28	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

TEXAS INSTRUMENTS
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436, 437

LINE DRIVER/MEMORY DRIVER CIRCUITS – MOS MEMORY INTERFACE

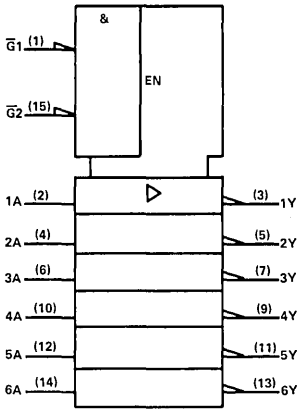
- Drives high-impedance loads
- Provides high-speed switching
- Requires minimum input current
- Damping output resistor for reducing transients ('436)
- Total power . . . 70 mW

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	DELAY
'S436	150 mA	–1 mA	5.5 ns
'S437	150 mA	–1 mA	5.5 ns

SN54S436 (J,FH) SN74S436 (J,N,FN)
SN54S437 (J,FH) SN74S437 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{G1}$	9	4Y	1	nc	11	nc
2	1A	10	4A	2	$\overline{G1}$	12	4Y
3	1Y	11	5Y	3	1A	13	4A
4	2A	12	5A	4	1Y	14	5Y
5	2Y	13	6Y	5	2A	15	5A
6	3A	14	6A	6	nc	16	nc
7	3Y	15	$\overline{G2}$	7	2Y	17	6Y
8	GND	16	V_{CC}	8	3A	18	6A
				9	3Y	19	$\overline{G2}$
				10	GND	20	V_{CC}

QUAD TRIDIRECTIONAL BUS TRANSCEIVERS

440 (OPEN-COLLECTOR OUTPUTS, NONINVERTED LOGIC)
441 (OPEN-COLLECTOR OUTPUTS, INVERTED LOGIC)
442 (THREE-STATE OUTPUTS, NONINVERTED LOGIC)
443 (THREE-STATE OUTPUTS, INVERTED LOGIC)
444 (THREE-STATE OUTPUTS, INVERTED AND NONINVERTED LOGIC)

ALSO SEE 'LS448

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54LS440	22 ns	–	12 mA
SN74LS440	22 ns	–	24 mA
SN54LS441	15 ns	–	12 mA
SN74LS441	15 ns	–	24 mA
SN54LS442	11.5 ns	–12 mA	12 mA
SN74LS442	11.5 ns	–15 mA	24 mA
SN54LS443	8 ns	–12 mA	12 mA
SN74LS443	8 ns	–15 mA	24 mA
SN54LS444	9 ns	–12 mA	12 mA
SN74LS444	9 ns	–15 mA	24 mA

SN54LS440 (J,FH) SN74LS440 (J,FN)
SN54LS441 (J,FH) SN74LS441 (J,FN)
SN54LS442 (J,FH) SN74LS442 (J,FN)
SN54LS443 (J,FH) SN74LS443 (J,FN)
SN54LS444 (J,FH) SN74LS444 (J,FN)

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{CS}$	11	S0	1	$\overline{CS}$	11	S0
2	B1	12	S1	2	B1	12	S1
3	C1	13	A4	3	C1	13	A4
4	C2	14	A3	4	C2	14	A3
5	B2	15	A2	5	B2	15	A2
6	B3	16	A1	6	B3	16	A1
7	C3	17	$\overline{GA}$	7	C3	17	$\overline{GA}$
8	C4	18	$\overline{GB}$	8	C4	18	$\overline{GB}$
9	B4	19	$\overline{GC}$	9	B4	19	$\overline{GC}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

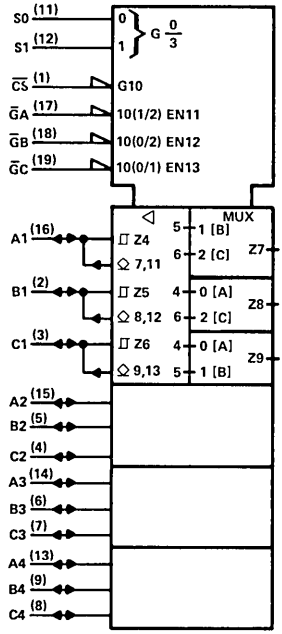
For logic symbols see next two pages.

† Pin numbers shown on logic symbols are for J and N packages only.
nc – no internal connection.

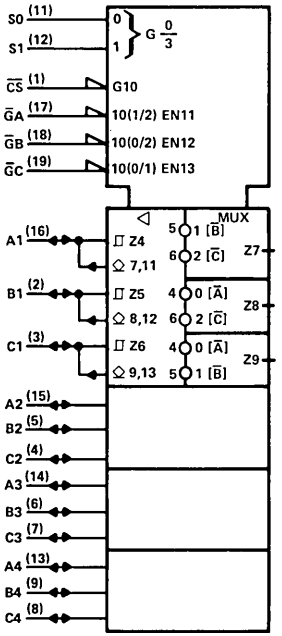
440, 441, 442, 443, 444 (continued)

logic symbol

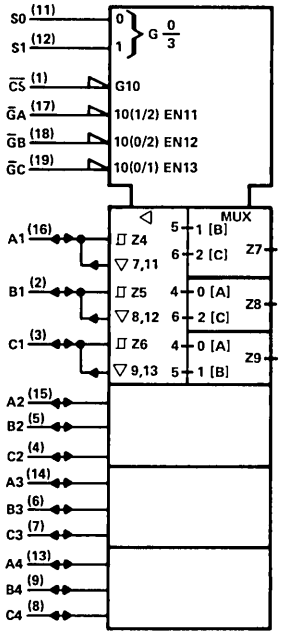
'LS440†



'LS441†



'LS442†



† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

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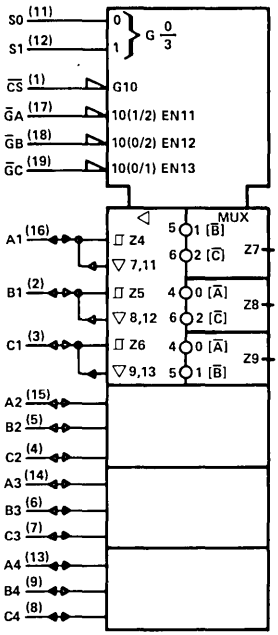
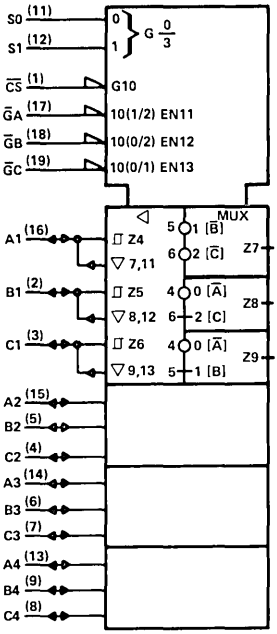
440, 441, 442, 443, 444 (continued)

'LS443†



'LS444†



445

BCD-TO-DECIMAL DECODERS/DRIVERS

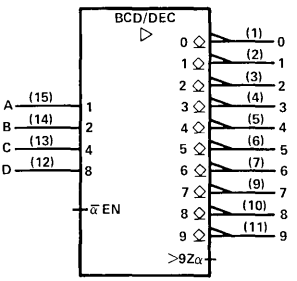
- Use as lamp, relay, or MOS driver
- Low-voltage version of 'LS145
- Full decoding of input logic
- All outputs off for invalid BCD input conditions

typical performance

OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TOTAL POWER
80 mA	7 V	35 mW

SN54LS445 (J,FH) SN74LS445 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	0	9	7	1	nc	11	nc
2	1	10	8	2	0	12	7
3	2	11	9	3	1	13	8
4	3	12	D	4	2	14	9
5	4	13	C	5	3	15	D
6	5	14	B	6	nc	16	nc
7	6	15	A	7	4	17	C
8	GND	16	V_{CC}	8	5	18	B
				9	6	19	A
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

446

QUAD BUS TRANSCEIVERS WITH DIRECTION CONTROLS

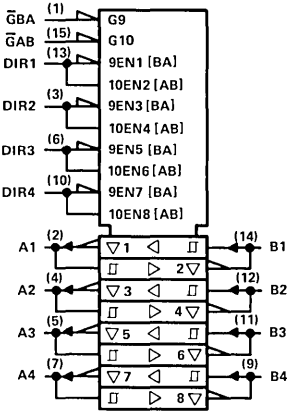
- Three-state outputs
- True ('LS449) and inverting ('LS446) outputs
- P-N-P inputs to reduce dc bus line loading

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54LS446	7.5 ns	−12 mA	12 mA
SN74LS446	7.5 ns	−15 mA	24 mA

SN54LS446 (J,FH) SN74LS446 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	G̅BA	9	B4	1	nc	11	nc
2	A1	10	DIR4	2	G̅BA	12	B4
3	DIR2	11	B3	3	A1	13	DIR4
4	A2	12	B2	4	DIR2	14	B3
5	A3	13	DIR1	5	A2	15	B2
6	DIR3	14	B1	6	nc	16	nc
7	A4	15	G̅AB	7	A3	17	DIR1
8	GND	16	V_{CC}	8	DIR3	18	B1
				9	A4	19	G̅AB
				10	GND	20	V_{CC}

447

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

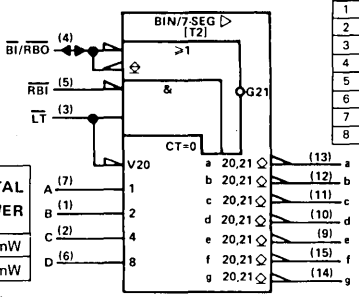
- Low-voltage version of 'LS247
- Open-collector outputs drive indicators directly
- Ripple blanking

typical performance

TYPE	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TOTAL POWER
SN54LS447	1.6 mA	7 V	35 mW
SN74LS447	3.2 mA	7 V	35 mW

SN54LS447 (J,FH) SN74LS447 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	B	9	e	1	nc	11	nc
2	C	10	d	2	B	12	e
3	L̅T̅	11	c	3	C	13	d
4	BI/R̅B̅O̅	12	b	4	L̅T̅	14	c
5	R̅B̅I̅	13	a	5	BI/R̅B̅O̅	15	b
6	D	14	g	6	nc	16	nc
7	A	15	f	7	RBI	17	a
8	GND	16	V_{CC}	8	D	18	g
				9	A	19	f
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

FONT TABLE T2 — NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS USING '447

448

QUAD TRIDIRECTIONAL BUS TRANSCEIVERS

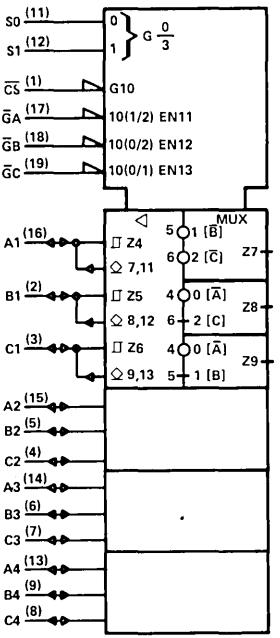
(OPEN-COLLECTOR OUTPUTS, INVERTED AND NONINVERTED LOGIC)

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54LS448	17.5 ns	–	12 mA
SN74LS448	17.5 ns	–	24 mA

SN54LS448 (J,FH) SN74LS448 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{CS}$	11	S0	1	$\overline{CS}$	11	S0
2	B1	12	S1	2	B1	12	S1
3	C1	13	A4	3	C1	13	A4
4	C2	14	A3	4	C2	14	A3
5	B2	15	A2	5	B2	15	A2
6	B3	16	A1	6	B3	16	A1
7	C3	17	$\overline{GA}$	7	C3	17	$\overline{GA}$
8	C4	18	$\overline{GB}$	8	C4	18	$\overline{GB}$
9	B4	19	$\overline{GC}$	9	B4	19	$\overline{GC}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

449

QUAD BUS TRANSCEIVERS WITH DIRECTION CONTROLS

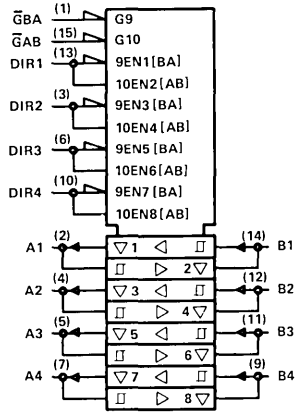
- Three-state outputs
- True ('LS449) and inverting ('LS446) outputs
- P-N-P inputs to reduce dc bus line loading

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54LS449	10.5 ns	−12 mA	12 mA
SN74LS449	10.5 ns	−15 mA	24 mA

SN54LS449 (J,FH) SN74LS449 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{GBA}$	9	B4	1	nc	11	nc
2	A1	10	DIR4	2	$\overline{GBA}$	12	B4
3	DIR2	11	B3	3	A1	13	DIR4
4	A2	12	B2	4	DIR2	14	B3
5	A3	13	DIR1	5	A2	15	B2
6	DIR3	14	B1	6	nc	16	nc
7	A4	15	$\overline{GAB}$	7	A3	17	DIR1
8	GND	16	V_{CC}	8	DIR3	18	B1
				9	A4	19	$\overline{GAB}$
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc – no internal connection.

6

465, 466

OCTAL BUFFERS WITH THREE-STATE OUTPUTS

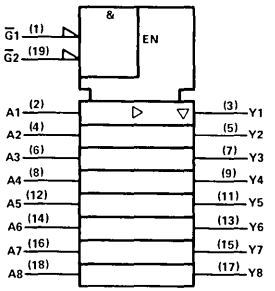
- P-N-P inputs reduce bus loading
- '465 true outputs
- '466 inverted outputs

typical performance

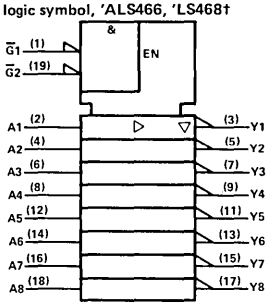
TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54ALS465		−12 mA	12 mA
SN74ALS465		−15 mA	24 mA
SN54ALS466	7 ns	−12 mA	12 mA
SN74ALS466	7 ns	−15 mA	24 mA
SN54LS465	11 ns	−1 mA	12 mA
SN74LS465	11 ns	−2.5 mA	24 mA
SN54LS466	8 ns	−1 mA	12 mA
SN74LS466	8 ns	−2.5 mA	24 mA

SN54ALS465 (J,FH) SN74ALS465 (N,FN)
SN54ALS466 (J,FH) SN74ALS466 (N,FN)
SN54LS465 (J) SN74LS465 (J,N)
SN74LS466 (J) SN74LS466 (J,N)

logic symbol, 'ALS465, 'LS465†



logic symbol, 'ALS466, 'LS468†



pin assignments

J, N PACKAGES			
1	G1	11	Y5
2	A1	12	A5
3	Y1	13	Y6
4	A2	14	A6
5	Y2	15	Y7
6	A3	16	A7
7	Y3	17	Y8
8	A4	18	A8
9	Y4	19	G2
10	GND	20	V_{CC}

'ALS465, 'ALS466

FH, FN PACKAGES			
1	G1	11	Y5
2	A1	12	A5
3	Y1	13	Y6
4	A2	14	A6
5	Y2	15	Y7
6	A3	16	A7
7	Y3	17	Y8
8	A4	18	A8
9	Y4	19	G2
10	GND	20	V_{CC}

For chip carrier information, contact the factory.

467, 468

OCTAL BUFFERS WITH THREE-STATE OUTPUTS

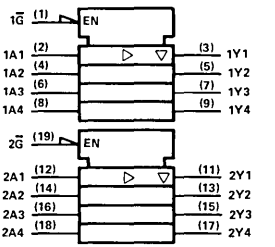
- P-N-P inputs reduce bus loading
- '467 true outputs
- '468 inverted outputs

typical performance

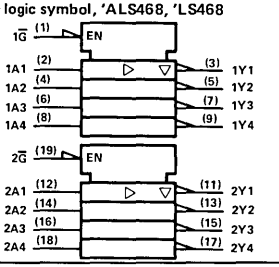
TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54ALS467		−12 mA	12 mA
SN74ALS467		−15 mA	24 mA
SN54ALS468	7 ns	−12 mA	12 mA
SN74ALS468	7 ns	−15 mA	24 mA
SN54LS467	11 ns	−1 mA	12 mA
SN74LS467	11 ns	−2.5 mA	24 mA
SN54LS468	8 ns	−1 mA	12 mA
SN74LS468	8 ns	−2.5 mA	24 mA

SN54ALS467 (J,FH) SN74ALS467 (N,FN)
SN54ALS468 (J,FH) SN74ALS468 (N,FN)
SN54LS467 (J) SN74LS467 (J,N)
SN54LS468 (J) SN74LS468 (J,N)

logic symbol, 'ALS467, 'LS467



logic symbol, 'ALS468, 'LS468



pin assignments

J, N PACKAGES			
1	1G	11	2Y1
2	1A1	12	2A1
3	1Y1	13	2Y2
4	1A2	14	2A2
5	1Y2	15	2Y3
6	1A3	16	2A3
7	1Y3	17	2Y4
8	1A4	18	2A4
9	1Y4	19	2G
10	GND	20	V_{CC}

'ALS467, 'ALS468

FH, FN PACKAGES			
1	1G	11	2Y1
2	1A1	12	2A1
3	1Y1	13	2Y2
4	1A2	14	2A2
5	1Y2	15	2Y3
6	1A3	16	2A3
7	1Y3	17	2Y4
8	1A4	18	2A4
9	1Y4	19	2G
10	GND	20	V_{CC}

For chip carrier information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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481

4-BIT-SLICE CASCADABLE PROCESSOR ELEMENTS

typical performance

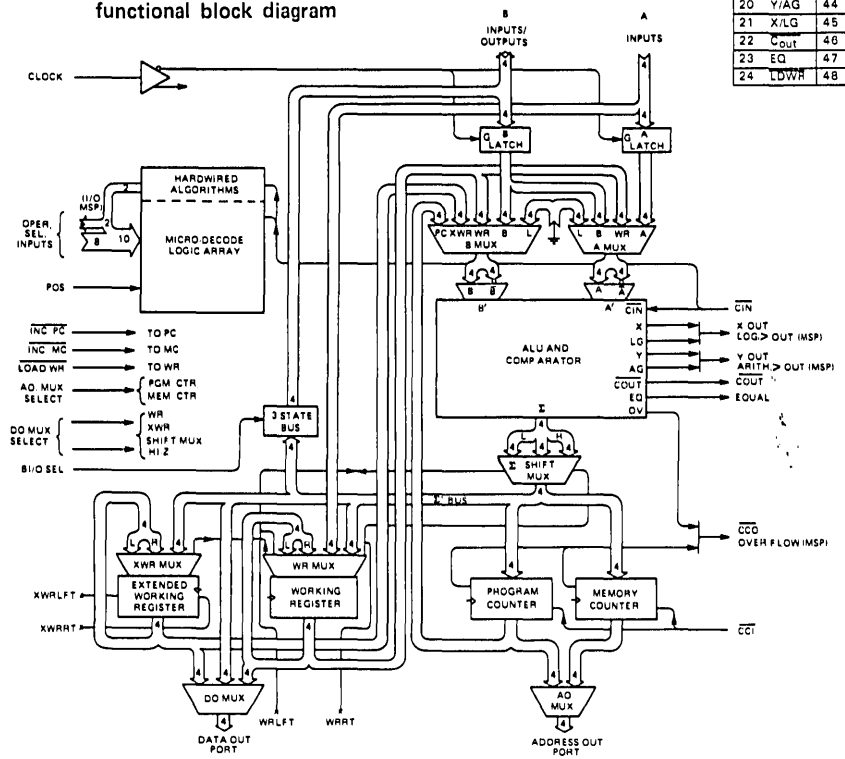
TYPE	OPERATION TIME
'LS481	120 ns
'S481	100 ns

SN74LS481 (J,N)
SN74S481 (J,N)

pin assignments

J, N PACKAGES			
1	B1/02	25	WRLFT
2	B1/03	26	WRRT
3	A13	27	XWRLFT
4	A12	28	XWRRT
5	A11	29	D0
6	A10	30	D1
7	OP0	31	DOP3
8	OP1	32	DOP2
9	OP2	33	DOP1
10	OP3	34	DOP0
11	OP7	35	$\overline{\text{INC MC}}$
12	V_{CC}	36	GND
13	OP6	37	$\overline{\text{CC0}}$/OV
14	OP5	38	AOP0
15	OP8	39	AOP1
16	PO9	40	AOP2
17	OP4	41	AOP3
18	$\overline{C_{in}}$	42	AOSEL
19	POS	43	$\overline{\text{INC PC}}$
20	Y/AG	44	$\overline{\text{CCI}}$
21	X/LG	45	CLK
22	$\overline{C_{out}}$	46	BI/OO
23	EQ	47	BI/01
24	$\overline{\text{LDWR}}$	48	BI/O SEL

functional block diagram



482

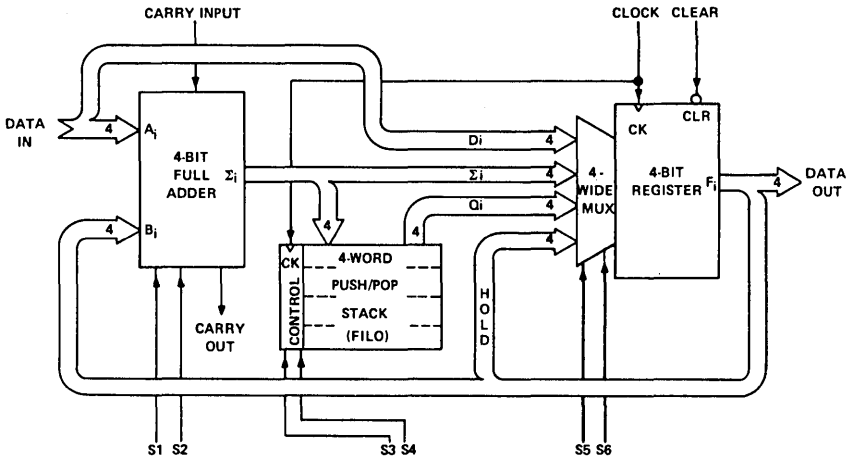
4-BIT-SLICE EXPANDABLE CONTROL ELEMENTS

SN54S482 (J,FH)
SN74S482 (J,N,FN)

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	S4	11	A0	1	S4	11	A0
2	S3	12	F3	2	S3	12	F3
3	C_{out}	13	F2	3	C_{out}	13	F2
4	C_{in}	14	F1	4	C_{in}	14	F1
5	S1	15	F0	5	S1	15	F0
6	S2	16	$\overline{CLR}$	6	S2	16	$\overline{CLR}$
7	A3	17	S6	7	A3	17	S6
8	A2	18	S5	8	A2	18	S5
9	A1	19	CLK	9	A1	19	CLK
10	GND	20	V_{CC}	10	GND	20	V_{CC}

functional block diagram



nc — no internal connection.

484, 485

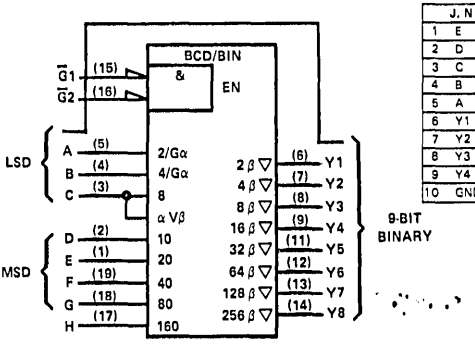
BCD-TO-BINARY AND BINARY-TO-BCD CODE CONVERTERS
('484 BCD-to-binary)
('485 binary-to-BCD)
typical performance

TYPE	DELAY TIME PER PKG LEVEL	TOTAL POWER
'S484	45 ns	525 mW
'S485	45 ns	525 mW

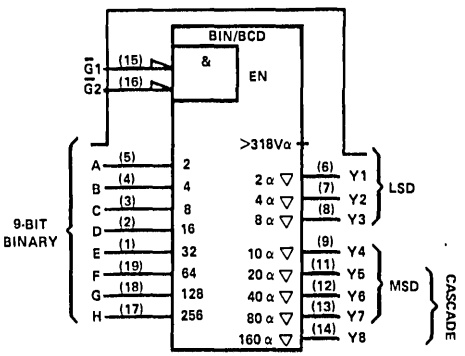
SN54S484 (J,FH)
SN54S485 (J,FH)

SN74S484 (J,N,FN)
SN74S485 (J,N,FN)

logic symbol 'S484†



logic symbol 'S485†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	E	11	Y5	1	E	11	Y5
2	D	12	Y6	2	D	12	Y6
3	C	13	Y7	3	C	13	Y7
4	B	14	Y8	4	B	14	Y8
5	A	15	$\overline{G1}$	5	A	15	$\overline{G1}$
6	Y1	16	$\overline{G2}$	6	Y1	16	$\overline{G2}$
7	Y2	17	H	7	Y2	17	H
8	Y3	18	G	8	Y3	18	G
9	Y4	19	F	9	Y4	19	F
10	GND	20	V_{CC}	10	GND	20	V_{CC}

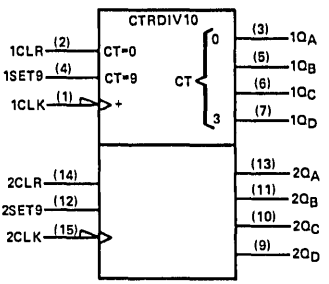
490

DUAL DECADE COUNTERS
typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'490	25 MHz	HIGH	225 mW
'LS490	35 MHz	HIGH	75 mW

SN54490 (J,FH)
SN54LS490 (J,FH)
SN74490 (J,N)
SN74LS490 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1CLK	9	$2Q_D$	1	nc	11	nc
2	1CLR	10	$2Q_C$	2	1CLK	12	$2Q_D$
3	$1Q_A$	11	$2Q_B$	3	1CLR	13	$2Q_C$
4	1SET9	12	2SET9	4	$1Q_A$	14	$2Q_B$
5	$1Q_B$	13	$2Q_A$	5	1SET9	15	2SET9
6	$1Q_C$	14	2CLR	6	nc	16	nc
7	$1Q_D$	15	2CLK	7	$1Q_B$	17	$2Q_A$
8	GND	16	V_{CC}	8	$1Q_C$	18	2CLR
				9	$1Q_D$	19	2CLK
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

518,519,520, 521,522

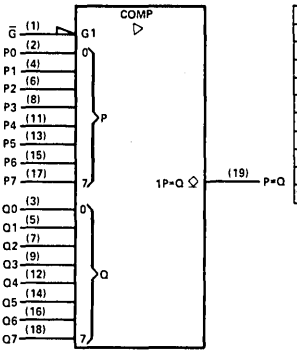
8-BIT MAGNITUDE COMPARATORS

- Compares two 8-bit words

TYPE	INPUT PULL-UP RESISTOR	OUTPUT FUNCTION AND CONFIGURATION	COMPARE TIME	POWER
ALS518	yes	P = Q open-collector	17.5 ns	50 mW
ALS519	no	P = Q open-collector	17.5 ns	37.5 mW
ALS520	yes	$\overline{P=Q}$ totem-pole	9 ns	50 mW
ALS521	no	$\overline{P=Q}$ totem-pole	9 ns	37.5 mW
ALS522	yes	$\overline{P=Q}$ open-collector	15.5 ns	50 mW

SN54ALS518(J,FH) SN74ALS518(N,FN)
SN54ALS519 (J,FH) SN74ALS519 (N,FN)
SN54ALS520 (J,FH) SN74ALS520 (N,FN)
SN54ALS521 (J,FH) SN74ALS521 (N,FN)
SN54ALS522 (J,FH) SN74ALS522 (N,FN)

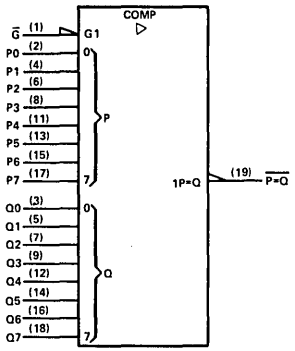
logic symbol 'ALS518, 'ALS519†



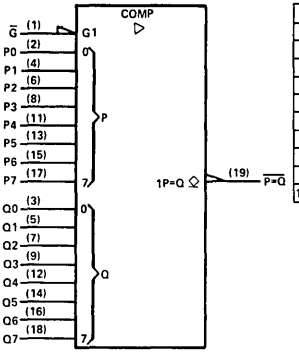
pin assignments, 'ALS518, 'ALS519

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{G}$	11	P4	1	$\overline{G}$	11	P4
2	P0	12	Q4	2	P0	12	Q4
3	Q0	13	P5	3	Q0	13	P5
4	P1	14	Q5	4	P1	14	Q5
5	Q1	15	P6	5	Q1	15	P6
6	P2	16	Q6	6	P2	16	Q6
7	Q2	17	P7	7	Q2	17	P7
8	P3	18	Q7	8	P3	18	Q7
9	Q3	19	P=Q	9	Q3	19	P=Q
10	GND	20	V_{CC}	10	GND	20	V_{CC}

logic symbol 'ALS520, 'ALS521†



logic symbol 'ALS522†



pin assignments, 'ALS520, 'ALS521, 'ALS522

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{G}$	11	P4	1	$\overline{G}$	11	P4
2	P0	12	Q4	2	P0	12	Q4
3	Q0	13	P5	3	Q0	13	P5
4	P1	14	Q5	4	P1	14	Q5
5	Q1	15	P6	5	Q1	15	P6
6	P2	16	Q6	6	P2	16	Q6
7	Q2	17	P7	7	Q2	17	P7
8	P3	18	Q7	8	P3	18	Q7
9	Q3	19	$\overline{P=Q}$	9	Q3	19	$\overline{P=Q}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

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533

OCTAL D-TYPE TRANSPARENT LATCHES

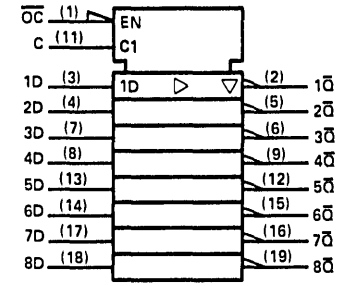
- Three-state buffer-type outputs drive bus lines directly
- Inverting outputs

typical performance

TYPE	OUTPUTS	DELAY	TOTAL POWER
ALS533	$\overline{Q}$	10 ns	60 mW
AS533	$\overline{Q}$	5 ns	

SN54ALS533 (J,FH) SN74ALS533 (N,FN)
SN54AS533 (J,FH) SN74AS533 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{OC}$	11	C	1	$\overline{OC}$	11	C
2	1$\overline{Q}$	12	5$\overline{Q}$	2	1$\overline{Q}$	12	5$\overline{Q}$
3	1D	13	5D	3	1D	13	5D
4	2D	14	6D	4	2D	14	6D
5	2$\overline{Q}$	15	6$\overline{Q}$	5	2$\overline{Q}$	15	6$\overline{Q}$
6	3$\overline{Q}$	16	7$\overline{Q}$	6	3$\overline{Q}$	16	7$\overline{Q}$
7	3D	17	7D	7	3D	17	7D
8	4D	18	8D	8	4D	18	8D
9	4$\overline{Q}$	19	8$\overline{Q}$	9	4$\overline{Q}$	19	8$\overline{Q}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

534

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

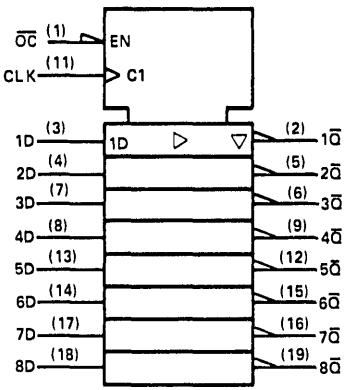
- Three-state buffer-type outputs drive bus lines directly
- Inverting outputs

typical performance

TYPE	F-MAX	PWR/F/F	DATA TIMES	
			SET-UP	HOLD
ALS534	50 MHz	10.4 mW		
AS534	165 MHz			

SN54ALS534 (J,FH) SN74ALS534 (N,FN)
SN54AS534 (J,FH) SN74AS534 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{OC}$	11	CLK	1	$\overline{OC}$	11	CLK
2	1$\overline{Q}$	12	5$\overline{Q}$	2	1$\overline{Q}$	12	5$\overline{Q}$
3	1D	13	5D	3	1D	13	5D
4	2D	14	6D	4	2D	14	6D
5	2$\overline{Q}$	15	6$\overline{Q}$	5	2$\overline{Q}$	15	6$\overline{Q}$
6	3$\overline{Q}$	16	7$\overline{Q}$	6	3$\overline{Q}$	16	7$\overline{Q}$
7	3D	17	7D	7	3D	17	7D
8	4D	18	8D	8	4D	18	8D
9	4$\overline{Q}$	19	8$\overline{Q}$	9	4$\overline{Q}$	19	8$\overline{Q}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

†Pin numbers shown on logic symbols are for J and N packages only.

538

3- TO 8-LINE DECODERS/ DEMULTIPLEXERS

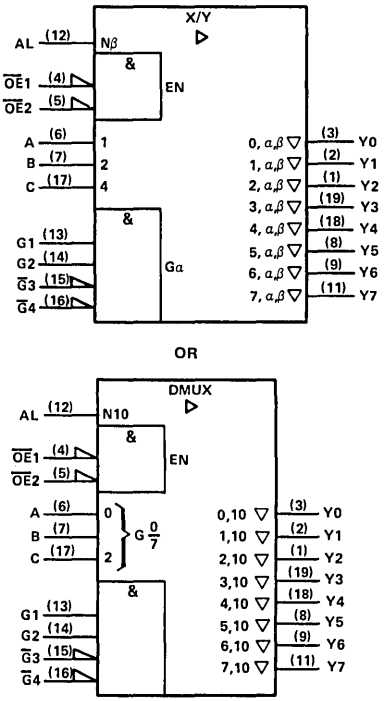
- Three-state outputs
- Output polarity control
- Multiple enables for expansion

typical performance

TYPE	SELECT TIME	ENABLE TIME	TOTAL POWER
'ALS538			

SN54ALS538 (J,FH) SN74ALS538 (N, FN)

logic symbol†



OR

pin assignments

J, N PACKAGES			
1	Y2	11	Y7
2	Y1	12	AL
3	Y0	13	G1
4	$\overline{OE}$1	14	G2
5	$\overline{OE}$2	15	$\overline{G}$3
6	A	16	$\overline{G}$4
7	B	17	C
8	Y5	18	Y4
9	Y6	19	Y3
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	Y2	11	Y7
2	Y1	12	AL
3	Y0	13	G1
4	$\overline{OE}$1	14	G2
5	$\overline{OE}$2	15	$\overline{G}$3
6	A	16	$\overline{G}$4
7	B	17	C
8	Y5	18	Y4
9	Y6	19	Y3
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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539

2- TO 4-LINE DECODERS/ DEMULTIPLEXERS

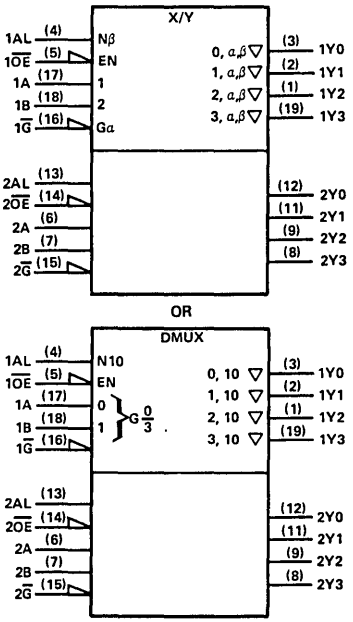
- Three-state outputs
- Output polarity control

typical performance

TYPE	SELECT TIME	ENABLE TIME	TOTAL POWER
'ALS539			

SN54ALS539 (J,FH) SN74ALS539 (N, FN)

logic symbols†



pin assignments

J, N PACKAGES			
1	1Y2	11	2Y1
2	1Y1	12	2Y0
3	1Y0	13	2AL
4	1AL	14	$2\overline{OE}$
5	$1\overline{OE}$	15	$2\overline{G}$
6	2A	16	$1\overline{G}$
7	2B	17	1A
8	2Y3	18	1B
9	2Y2	19	1Y3
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	1Y2	11	2Y1
2	1Y1	12	2Y0
3	1Y0	13	2AL
4	1AL	14	$2\overline{OE}$
5	$1\overline{OE}$	15	$2\overline{G}$
6	2A	16	$1\overline{G}$
7	2B	17	1A
8	2Y3	18	1B
9	2Y2	19	1Y3
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

540, 541

OCTAL BUFFERS AND LINE DRIVERS

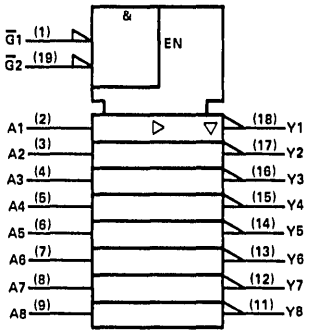
- Three-state output drives bus lines or buffer memory address registers
- 'LS540 for inverted data output
- 'LS541 for true data output

typical performance

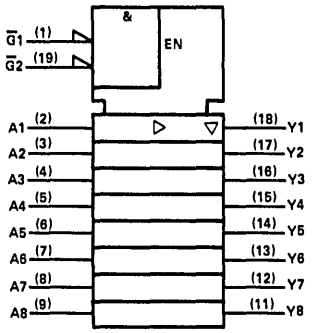
TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54ALS540	6 ns	−12 mA	12 mA
SN74ALS540	6 ns	−15 mA	24 mA
SN54ALS541	6 ns	−12 mA	12 mA
SN74ALS541	6 ns	−15 mA	24 mA
SN54LS540	9 ns	−12 mA	12 mA
SN74LS540	9.5 ns	−15 mA	24 mA
SN54LS541	9 ns	−12 mA	12 mA
SN74LS541	9.5 ns	−15 mA	24 mA

SN54ALS540 (J,FH) SN74ALS540 (N,FN)
SN54ALS541 (J,FH) SN74ALS541 (N,FN)
SN54LS540 (J,FH) SN74LS540 (J,N,FN)
SN54LS541 ((J,FH) SN74LS541 (J,N,FN)

logic symbol, 'LS540, 'ALS540†



logic symbol, 'LS541, 'ALS541†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{G}1$	11	Y8	1	$\overline{G}1$	11	Y8
2	A1	12	Y7	2	A1	12	Y7
3	A2	13	Y6	3	A2	13	Y6
4	A3	14	Y5	4	A3	14	Y5
5	A4	15	Y4	5	A4	15	Y4
6	A5	16	Y3	6	A5	16	Y3
7	A6	17	Y2	7	A6	17	Y2
8	A7	18	Y1	8	A7	18	Y1
9	A8	19	$\overline{G}2$	9	A8	19	$\overline{G}2$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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560

SYNCHRONOUS 4-BIT COUNTERS

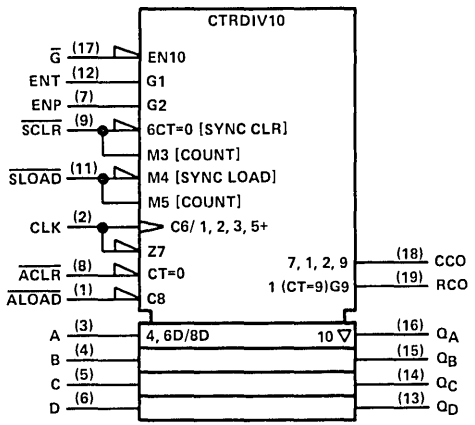
(decade, synchronous and asynchronous clear)

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'ALS560	30 MHz	Low	100 mW

SN54ALS560 (J,FH) SN74ALS560 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	ALOAD	11	SLOAD
2	CLK	12	ENT
3	A	13	Q_D
4	B	14	Q_C
5	C	15	Q_B
6	D	16	Q_A
7	ENP	17	G
8	ACLR	18	CCO
9	SCLR	19	RCO
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	ALOAD	11	SLOAD
2	CLK	12	ENT
3	A	13	Q_D
4	B	14	Q_C
5	C	15	Q_B
6	D	16	Q_A
7	ENP	17	G
8	ACLR	18	CCO
9	SCLR	19	RCO
10	GND	20	V_{CC}

561

SYNCHRONOUS 4-BIT COUNTERS

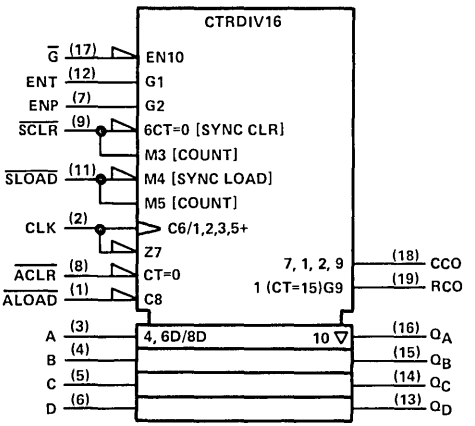
(binary, synchronous and asynchronous clear)

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'ALS561	40 MHz	Low	100 mW

SN54ALS561 (J,FH) SN74ALS561 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	ALOAD	11	SLOAD
2	CLK	12	ENT
3	A	13	Q_D
4	B	14	Q_C
5	C	15	Q_B
6	D	16	Q_A
7	ENP	17	G
8	ACLR	18	CCO
9	SCLR	19	RCO
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	ALOAD	11	SLOAD
2	CLK	12	ENT
3	A	13	Q_D
4	B	14	Q_C
5	C	15	Q_B
6	D	16	Q_A
7	ENP	17	G
8	ACLR	18	CCO
9	SCLR	19	RCO
10	GND	20	V_{CC}

Pin numbers shown on logic symbols are for J and N packages only.

563

OCTAL D-TYPE TRANSPARENT LATCHES WITH INVERTED OUTPUTS

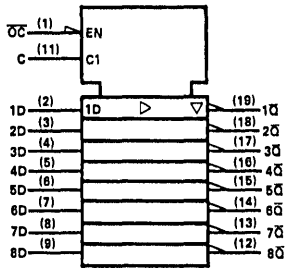
- Buffer-type outputs drive bus lines directly
- Inverted outputs

typical performance

TYPE	DELAY	TOTAL POWER
'ALS563	11 ns	67.5 mW

SN54ALS563 (J,FH) SN74ALS563 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	OC	11	C	1	OC	11	C
2	1D	12	8Q	2	1D	12	8Q
3	2D	13	7Q	3	2D	13	7Q
4	3D	14	6Q	4	3D	14	6Q
5	4D	15	5Q	5	4D	15	5Q
6	5D	16	4Q	6	5D	16	4Q
7	6D	17	3Q	7	6D	17	3Q
8	7D	18	2Q	8	7D	18	2Q
9	8D	19	1Q	9	8D	19	1Q
10	GND	20	V_{CC}	10	GND	20	V_{CC}

564

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

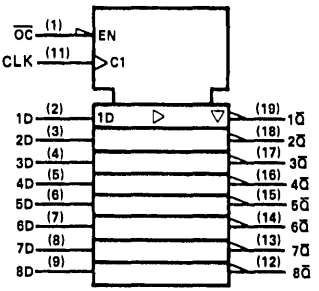
- Buffer-type outputs drive bus lines directly
- Inverted outputs

typical performance

TYPE	f_{max}	PWR/ F-F
'ALS564	50 MHz	8.4 mW

SN54ALS564 (J,FH) SN74ALS564 (N,FN)

logic symbol†



pin assignment

J, N PACKAGES				FH, FN PACKAGES			
1	OC	11	CLK	1	OC	11	CLK
2	1D	12	8Q	2	1D	12	8Q
3	2D	13	7Q	3	2D	13	7Q
4	3D	14	6Q	4	3D	14	6Q
5	4D	15	5Q	5	4D	15	5Q
6	5D	16	4Q	6	5D	16	4Q
7	6D	17	3Q	7	6D	17	3Q
8	7D	18	2Q	8	7D	18	2Q
9	8D	19	1Q	9	8D	19	1Q
10	GND	20	V_{CC}	10	GND	20	V_{CC}

†Pin numbers shown on logic symbols are for J and N packages only.

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568

SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

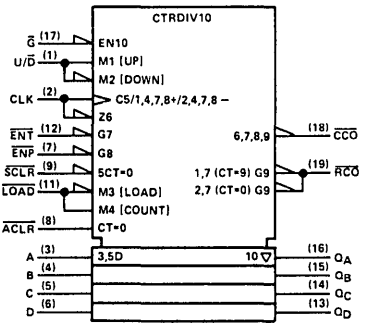
(decade, synchronous and asynchronous clear)

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'ALS568	30 MHz	Low	93 mW

SN54ALS568 (J,FH) SN74ALS568 (N,FN)

logic symbol†



pin assignment

J, N PACKAGES				FH, FN PACKAGES			
1	U/D	11	LOAD	1	U/D	11	LOAD
2	CLK	12	ENT	2	CLK	12	ENT
3	A	13	Q_D	3	A	13	Q_D
4	B	14	Q_C	4	B	14	Q_C
5	C	15	Q_B	5	C	15	Q_B
6	D	16	Q_A	6	D	16	Q_A
7	ENP	17	G	7	ENP	17	G
8	ACLR	18	CCO	8	ACLR	18	CCO
9	SCLR	19	RCO	9	SCLR	19	RCO
10	GND	20	V_{CC}	10	GND	20	V_{CC}

569

SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

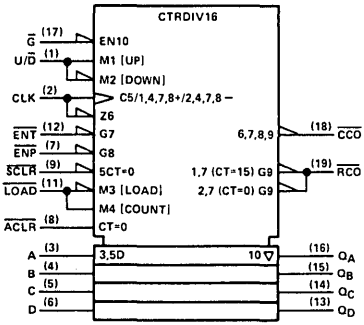
(binary, synchronous and asynchronous clear)

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'ALS569	40 MHz	Low	93 mW

SN54ALS569 (J,FH) SN74ALS569 (N,FN)

logic symbol†



pin assignment

J, N PACKAGES				FH, FN PACKAGES			
1	U/D	11	LOAD	1	U/D	11	LOAD
2	CLK	12	ENT	2	CLK	12	ENT
3	A	13	Q_D	3	A	13	Q_D
4	B	14	Q_C	4	B	14	Q_C
5	C	15	Q_B	5	C	15	Q_B
6	D	16	Q_A	6	D	16	Q_A
7	ENP	17	G	7	ENP	17	G
8	ACLR	18	CCO	8	ACLR	18	CCO
9	SCLR	19	RCO	9	SCLR	19	RCO
10	GND	20	V_{CC}	10	GND	20	V_{CC}

†Pin numbers shown on logic symbols are for J and N packages only.

573

OCTAL D-TYPE TRANSPARENT LATCHES

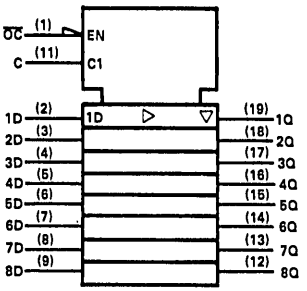
- Functionally equivalent to 'LS373 and 'S373
- Three-state buffer-type outputs drive bus lines directly
- Approximately half the power of 'LS373

typical performance

TYPE	OUTPUTS	DELAY	TOTAL POWER
'ALS573	Q	11 ns	67.5 mW
'AS573			

SN54ALS573 (J,FH) SN74ALS573 (N,FN)
SN54AS573 (J,FH) SN74AS573 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{OC}$	11	C	1	$\overline{OC}$	11	C
2	1D	12	8Q	2	1D	12	8Q
3	2D	13	7Q	3	2D	13	7Q
4	3D	14	6Q	4	3D	14	6Q
5	4D	15	5Q	5	4D	15	5Q
6	5D	16	4Q	6	5D	16	4Q
7	6D	17	3Q	7	6D	17	3Q
8	7D	18	2Q	8	7D	18	2Q
9	8D	19	1Q	9	8D	19	1Q
10	GND	20	V_{CC}	10	GND	20	V_{CC}

574

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

- Functionally equivalent to 'LS374 and 'S374
- Three-state buffer-type outputs drive bus lines directly
- Approximately half the power of 'LS374

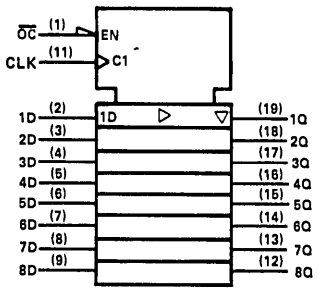
typical performance

TYPE	f_{max}	PWR/ F-F	DATA TIMES SET-UP	DATA TIMES HOLD
'ALS574	50 MHz	8.44 mW	10 ns	4 ns
'AS574				

† Rising edge of clock pulse

SN54ALS574 (J,FH) SN74ALS574 (N,FN)
SN54AS574 (J,FH) SN74AS574 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{OC}$	11	CLK	1	$\overline{OC}$	11	CLK
2	1D	12	8Q	2	1D	12	8Q
3	2D	13	7Q	3	2D	13	7Q
4	3D	14	6Q	4	3D	14	6Q
5	4D	15	5Q	5	4D	15	5Q
6	5D	16	4Q	6	5D	16	4Q
7	6D	17	3Q	7	6D	17	3Q
8	7D	18	2Q	8	7D	18	2Q
9	8D	19	1Q	9	8D	19	1Q
10	GND	20	V_{CC}	10	GND	20	V_{CC}

575

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

- 3-state buffer-type outputs drive bus-lines directly
- Noninverting outputs

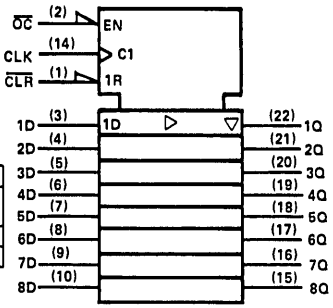
typical performance

TYPE	f_{max}	PWR/ F-F	DATA TIMES SET-UP	DATA TIMES HOLD
'ALS575	50 MHz	8.4 mW	10 nst	4 nst
'AS575				

†Rising edge of clock pulse

SN54ALS575 (J,FH) SN74ALS575 (N,FN)
SN54AS575 (J,FH) SN74AS575 (N,FN)

logic symbol, 'ALS575, 'AS575



pin assignment

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{CLR}$	13	nc	1	nc	15	nc
2	$\overline{OC}$	14	CLK	2	$\overline{CLR}$	16	nc
3	1D	15	8Q	3	$\overline{OC}$	17	CLK
4	2D	16	7Q	4	1D	18	8Q
5	3D	17	6Q	5	2D	19	7Q
6	4D	18	5Q	6	3D	20	6Q
7	5D	19	4Q	7	4D	21	5Q
8	6D	20	3Q	8	nc	22	nc
9	7D	21	2Q	9	5D	23	4Q
10	8D	22	1Q	10	6D	24	3Q
11	nc	23	nc	11	7D	25	2Q
12	GND	24	V_{CC}	12	8D	26	1Q
				13	nc	27	nc
				14	GND	28	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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576

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

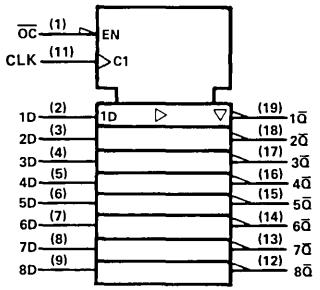
- Buffer-type outputs drive bus lines directly
- Inverted outputs

typical performance

TYPE	f_{max}	PWR/ F-F
'ALS576	50MHz	8.4 mW
'AS576		

SN54ALS576 (J,FH) SN74ALS576 (N,FN)
SN54AS576 (J,FH) SN74AS576 (N,FN)

logic symbol†



pin assignments

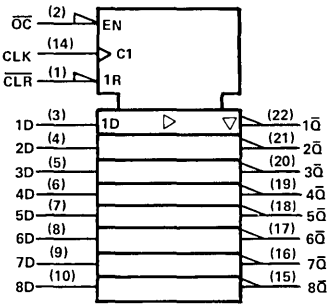
J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{OC}$	11	CLK	1	$\overline{OC}$	11	CLK
2	1D	12	$8\overline{Q}$	2	1D	12	$8\overline{Q}$
3	2D	13	$7\overline{Q}$	3	2D	13	$7\overline{Q}$
4	3D	14	$6\overline{Q}$	4	3D	14	$6\overline{Q}$
5	4D	15	$5\overline{Q}$	5	4D	15	$5\overline{Q}$
6	5D	16	$4\overline{Q}$	6	5D	16	$4\overline{Q}$
7	6D	17	$3\overline{Q}$	7	6D	17	$3\overline{Q}$
8	7D	18	$2\overline{Q}$	8	7D	18	$2\overline{Q}$
9	8D	19	$1\overline{Q}$	9	8D	19	$1\overline{Q}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

577

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

- Buffer-type outputs drive bus lines directly
- Inverted outputs
- Synchronous clear

logic symbol, 'ALS577, 'AS577



pin assignment

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{CLR}$	13	nc	1	nc	15	nc
2	$\overline{OC}$	14	CLK	2	$\overline{CLR}$	16	nc
3	1D	15	$8\overline{Q}$	3	$\overline{OC}$	17	CLK
4	2D	16	$7\overline{Q}$	4	1D	18	$8\overline{Q}$
5	3D	17	$6\overline{Q}$	5	2D	19	$7\overline{Q}$
6	4D	18	$5\overline{Q}$	6	3D	20	$6\overline{Q}$
7	5D	19	$4\overline{Q}$	7	4D	21	$5\overline{Q}$
8	6D	20	$3\overline{Q}$	8	nc	22	nc
9	7D	21	$2\overline{Q}$	9	5D	23	$4\overline{Q}$
10	8D	22	$1\overline{Q}$	10	6D	24	$3\overline{Q}$
11	nc	23	nc	11	7D	25	$2\overline{Q}$
12	GND	24	V_{CC}	12	8D	26	$1\overline{Q}$
				13	nc	27	nc
				14	GND	28	V_{CC}

typical performance

TYPE	f_{max}	POWER/ F-F	DATA TIMES	
			SET-UP	HOLD
'ALS577	50 MHz	8.4 mW	10 nst	4 nst
'AS577				

†Rising edge of clock pulse
SN54ALS577 (J,FH) SN74ALS577(N,FN)
SN54AS577 (J,FH) SN74AS577(N,FN)

†Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

580

OCTAL D-TYPE TRANSPARENT LATCHES WITH INVERTED OUTPUTS

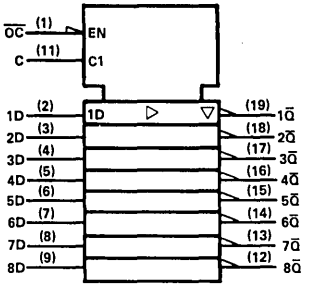
- Three-state buffer-type outputs drive bus lines directly

typical performance

TYPE	DELAY	TOTAL POWER
'ALS580	11 ns	67.5 mW
'AS580		

SN54ALS580 (J,FH) SN74ALS580 (N,FN)
SN54AS580 (J,FH) SN74AS580 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	OC	11	C
2	1D	12	8Q
3	2D	13	7Q
4	3D	14	6Q
5	4D	15	5Q
6	5D	16	4Q
7	6D	17	3Q
8	7D	18	2Q
9	8D	19	1Q
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	OC	11	C
2	1D	12	8Q
3	2D	13	7Q
4	3D	14	6Q
5	4D	15	5Q
6	5D	16	4Q
7	6D	17	3Q
8	7D	18	2Q
9	8D	19	1Q
10	GND	20	V_{CC}

590, 591

8-BIT BINARY COUNTERS WITH OUTPUT REGISTERS

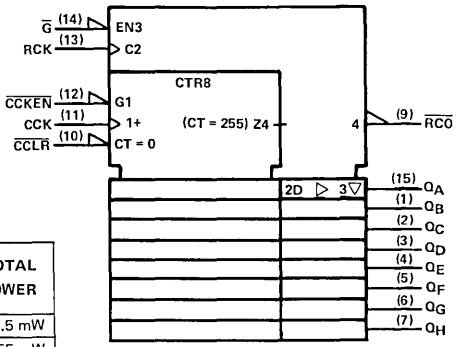
- 'LS590 has three-state register outputs
- 'LS591 has open-collector register outputs
- Counter has direct clear

typical performance

TYPE	MAX COUNT FREQ	PARALLEL LOAD	CLEAR	TOTAL POWER
'LS590	20 MHz	SYNC	SYNC-L	166.5 mW
'LS591	20 MHz	SYNC	SYNC-L	155 mW

SN54LS590 (J,FH) SN74LS590 (J,N,FN)
SN54LS591 (J,FH) SN74LS591 (J,N,FN)

logic symbol, 'LS590†

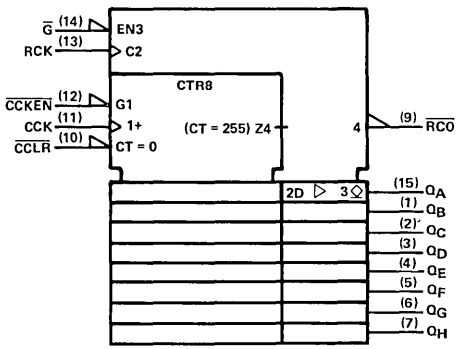


pin assignments

J, N PACKAGES			
1	Q_B	9	RCO
2	Q_C	10	CCLR
3	Q_D	11	CCK
4	Q_E	12	CCKEN
5	Q_F	13	RCK
6	Q_G	14	G
7	Q_H	15	Q_A
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	Q_B	12	RCO
3	Q_C	13	CCLR
4	Q_D	14	CCK
5	Q_E	15	CCKEN
6	nc	16	nc
7	Q_F	17	RCK
8	Q_G	18	G
9	Q_H	19	Q_A
10	GND	20	V_{CC}

logic symbol, 'LS591†



† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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592

8-BIT BINARY COUNTERS WITH INPUT REGISTERS

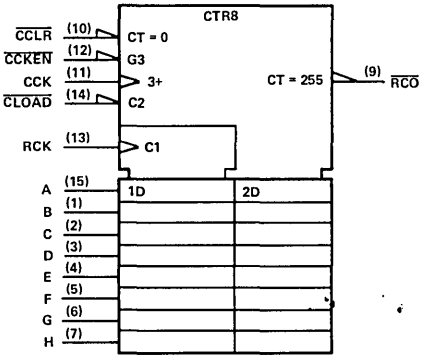
- Has parallel register inputs
- Counter has direct overriding load and clear
- Guaranteed counter frequency . . . dc to 20 MHz

typical performance

MAX COUNT FREQ	PARALLEL LOAD	CLEAR	TOTAL POWER
20 MHz	SYNC	SYNC-L	130 mW

SN54LS592 (J,FH)
SN74LS592 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	B	9	$\overline{RCO}$
2	C	10	$\overline{CCLR}$
3	D	11	CCK
4	E	12	$\overline{CCKEN}$
5	F	13	RCK
6	G	14	$\overline{CLOAD}$
7	H	15	A
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	B	12	$\overline{RCO}$
3	C	13	$\overline{CCLR}$
4	D	14	CCK
5	E	15	$\overline{CCKEN}$
6	nc	16	nc
7	F	17	RCK
8	G	18	$\overline{CLOAD}$
9	H	19	A
10	GND	20	V_{CC}

593

8-BIT BINARY COUNTERS WITH INPUT REGISTERS

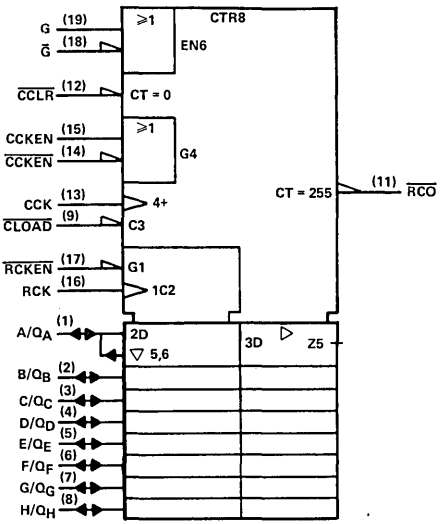
- Has parallel three-state I/O: register inputs/counter outputs
- Counter has direct overriding load and clear
- Guaranteed counter frequency . . . dc to 20 MHz

typical performance

MAX COUNT FREQ	PARALLEL LOAD	CLEAR	TOTAL POWER
20 MHz	SYNC	SYNC-L	177 mW

SN54LS593 (J,FH)
SN74LS593 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	A/Q_A	11	$\overline{RCO}$
2	B/Q_B	12	$\overline{CCLR}$
3	C/Q_C	13	CCK
4	D/Q_D	14	$\overline{CCKEN}$
5	E/Q_E	15	CCKEN
6	F/Q_F	16	RCK
7	G/Q_G	17	$\overline{RCKEN}$
8	H/Q_H	18	$\overline{G}$
9	$\overline{CLOAD}$	19	G
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	A/Q_A	11	$\overline{RCO}$
2	B/Q_B	12	$\overline{CCLR}$
3	C/Q_C	13	CCK
4	D/Q_D	14	$\overline{CCKEN}$
5	E/Q_E	15	CCKEN
6	F/Q_F	16	RCK
7	G/Q_G	17	$\overline{RCKEN}$
8	H/Q_H	18	$\overline{G}$
9	$\overline{CLOAD}$	19	G
10	GND	20	V_{CC}

6

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

594

8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

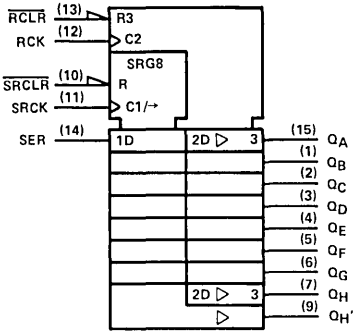
- Serial-in, parallel-out shift registers with storage
- Buffered outputs
- Guaranteed shift frequency . . . dc to 20 MHz

typical performance

TYPE	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'LS594	D	Low	

SN54LS594 (J,FH) SN74LS594 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	Q_B	9	$Q_{H'}$
2	Q_C	10	$\overline{SRCLR}$
3	Q_D	11	SRCK
4	Q_E	12	RCK
5	Q_F	13	$\overline{RCLR}$
6	Q_G	14	SER
7	Q_H	15	Q_A
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	Q_B	12	$Q_{H'}$
3	Q_C	13	$\overline{SRCLR}$
4	Q_D	14	SRCK
5	Q_E	15	RCK
6	nc	16	nc
7	Q_F	17	$\overline{RCLR}$
8	Q_G	18	SER
9	Q_H	19	Q_A
10	GND	20	V_{CC}

595, 596

8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

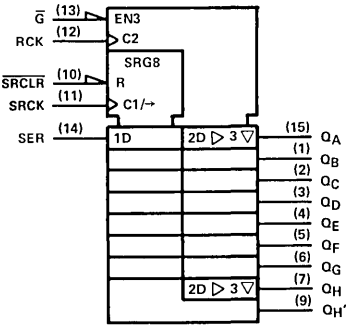
- Serial-in, parallel-out shift registers with storage
- 'LS595 has three-state parallel outputs
- 'LS596 has open-collector parallel outputs
- Guaranteed shift frequency . . . dc to 20 MHz

typical performance

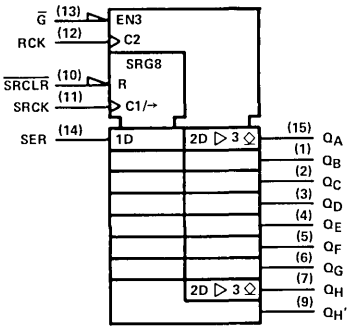
TYPE	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'LS595	D	LOW	167 mW
'LS596	D	LOW	160 mW

SN54LS595 (J,FH) SN74LS595 (J,N,FN)
SN54LS596 (J,FH) SN74LS596 (J,N,FN)

logic symbol, 'LS595†



logic symbol, 'LS596†



pin assignments

J, N PACKAGES			
1	Q_B	9	$Q_{H'}$
2	Q_C	10	$\overline{SRCLR}$
3	Q_D	11	$\overline{SRCK}$
4	Q_E	12	RCK
5	Q_F	13	$\overline{G}$
6	Q_G	14	SER
7	Q_H	15	Q_A
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	Q_B	12	$Q_{H'}$
3	Q_C	13	$\overline{SCLR}$
4	Q_D	14	SCK
5	Q_E	15	RCK
6	nc	16	nc
7	Q_F	17	$\overline{G}$
8	Q_G	18	SER
9	Q_H	19	Q_A
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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597

8-BIT SHIFT REGISTERS WITH INPUT LATCHES

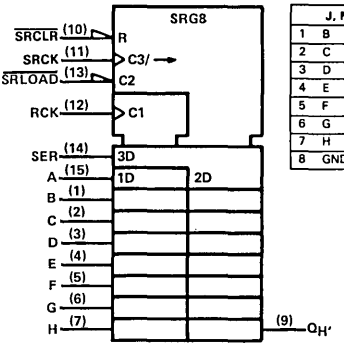
- Has parallel storage register inputs
- Shift register has direct overriding load and clear
- Guaranteed shift frequency . . . dc to 20 MHz

typical performance

TYPE	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'LS597	D	LOW	130 mW

SN54LS597 (J,FH) SN74LS597 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	B	9	$Q_{H'}$	1	nc	11	nc
2	C	10	SRCLR	2	B	12	$Q_{H'}$
3	D	11	SRCK	3	C	13	SRCLR
4	E	12	RCK	4	D	14	SRCK
5	F	13	SRLOAD	5	E	15	RCK
6	G	14	SER	6	nc	16	nc
7	H	15	A	7	F	17	SRLOAD
8	GND	16	V_{CC}	8	G	18	SER
				9	H	19	A
				10	GND	20	V_{CC}

598

8-BIT SHIFT REGISTERS WITH INPUT LATCHES

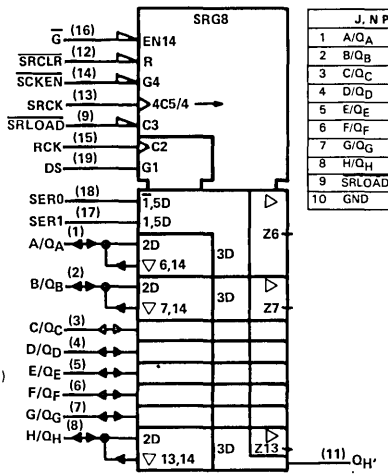
- Has parallel three-state I/O storage register inputs, shift register outputs
- Shift register has direct overriding load and clear
- Guaranteed shift frequency . . . dc to 20 MHz

typical performance

TYPE	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'LS598	D	LOW	177 mW

SN54LS598 (J,FH) SN74LS598 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A/Q_A	11	$Q_{H'}$	1	A/Q_A	11	$Q_{H'}$
2	B/Q_B	12	SRCLR	2	B/Q_B	12	SRCLR
3	C/Q_C	13	SRCK	3	C/Q_C	13	SRCK
4	D/Q_D	14	SRCKEN	4	D/Q_D	14	SCKEN
5	E/Q_E	15	RCK	5	E/Q_E	15	RCK
6	F/Q_F	16	G	6	F/Q_F	16	G
7	G/Q_G	17	SER1	7	G/Q_G	17	SER1
8	H/Q_H	18	SER0	8	H/Q_H	18	SER0
9	SRLOAD	19	DS	9	SRLOAD	19	DS
10	GND	20	V_{CC}	10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

599

8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

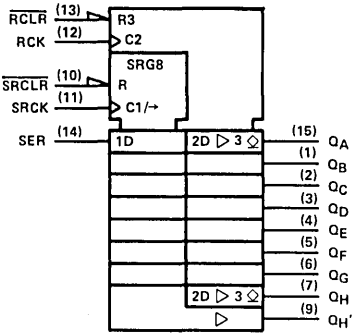
- Serial-in, parallel-out shift registers
- Open-collector outputs
- Guaranteed shift frequency
  . . . dc to 20 MHz

typical performance

TYPE	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'LS599	D	Low	

SN54LS599 (J,FH) SN74LS599 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	Q_B	9	$Q_{H'}$
2	Q_C	10	$\overline{SRCLR}$
3	Q_D	11	SRCK
4	Q_E	12	RCK
5	Q_F	13	$\overline{RCLR}$
6	Q_G	14	SER
7	Q_H	15	Q_A
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	Q_B	12	$Q_{H'}$
3	Q_C	13	$\overline{SRCLR}$
4	Q_D	14	SRCK
5	Q_E	15	RCK
6	nc	16	nc
7	Q_F	17	$\overline{RCLR}$
8	Q_G	18	SER
9	Q_H	19	Q_A
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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600

MEMORY REFRESH CONTROLLERS

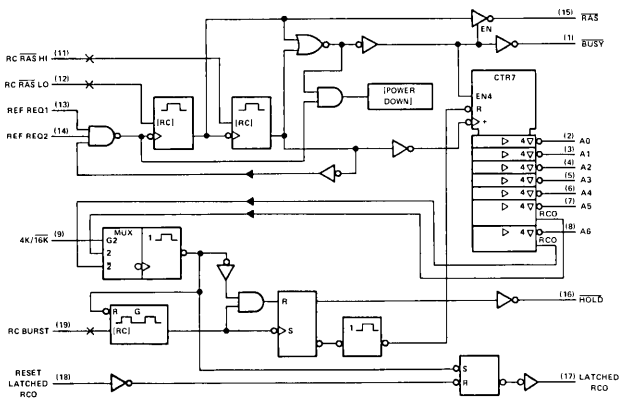
- Controls refresh cycle of 4K or 16K dynamic RAM's
- Three-state outputs drive bus lines directly
- Time to initiate refresh request is typically 30 ns
- Refresh modes: transparent, burst

SN54LS600A (J) SN74LS600A (J,N)

pin assignments

J,N PACKAGES			
1	BUSY	11	RC $\overline{RAS}$ HI
2	A0	12	RC $\overline{RAS}$ LO
3	A1	13	REF REQ1
4	A2	14	REF REQ2
5	A3	15	$\overline{RAS}$
6	A4	16	$\overline{HOLD}$
7	A5	17	LATCHED RCO
8	A6	18	RESET LATCHED RCO
9	4K/$\overline{16K}$	19	RC BURST
10	GND	20	V_{CC}

logic diagram†



For chip carrier information, contact the factory.

601

MEMORY REFRESH CONTROLLERS

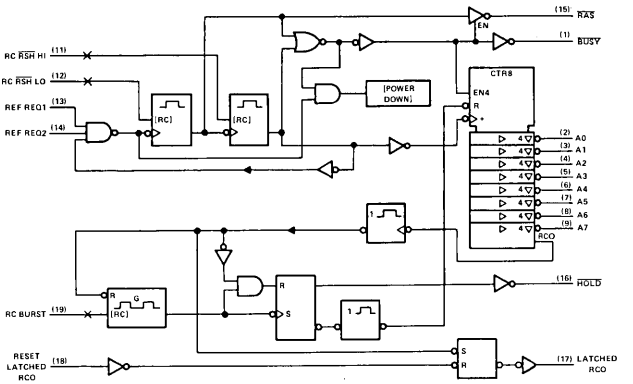
- Controls refresh cycle of 64K dynamic RAM's
- Three-state outputs drive bus lines directly
- Time to initiate refresh request is typically 30 ns
- Refresh modes: transparent, burst

SN54LS601A (J) SN74LS601A (J,N)

pin assignments

J,N PACKAGES			
1	BUSY	11	RC $\overline{RAS}$ HI
2	A0	12	RC $\overline{RAS}$ LO
3	A1	13	REF REQ1
4	A2	14	REF REQ2
5	A3	15	$\overline{RAS}$
6	A4	16	$\overline{HOLD}$
7	A5	17	LATCHED RCO
8	A6	18	RESET LATCHED RCO
9	A7	19	RC BURST
10	GND	20	V_{CC}

logic diagram†



For chip carrier information, contact the factory.

†Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

602

MEMORY REFRESH CONTROLLERS

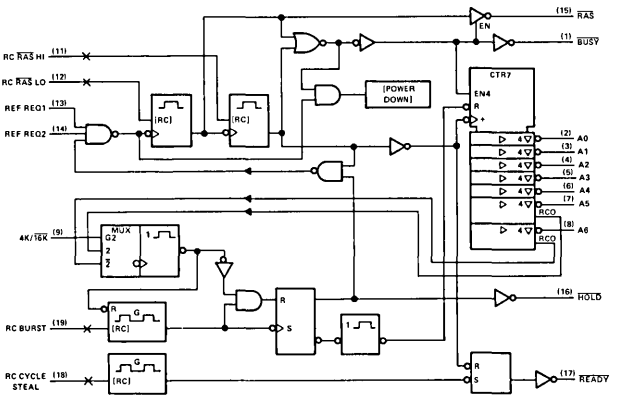
- Controls refresh cycle of 4K or 16K dynamic RAM's
- Three-state outputs drive bus lines directly
- Time to initiate refresh request is typically 30 ns
- Refresh modes: cycle steal, burst

SN54LS602A (J) SN74LS602A (J,N)

pin assignments

J, N PACKAGES			
1	$\overline{BUSY}$	11	RC $\overline{RAS}$ HI
2	A0	12	RC $\overline{RAS}$ LO
3	A1	13	REF REQ1
4	A2	14	REF REQ2
5	A3	15	$\overline{RAS}$
6	A4	16	$\overline{HOLD}$
7	A5	17	READY
8	A6	18	RC CYCLE STEAL
9	4K/16K	19	RC BURST
10	GND	20	V_{CC}

logic diagram†



For chip carrier information, contact the factory.

603

MEMORY REFRESH CONTROLLERS

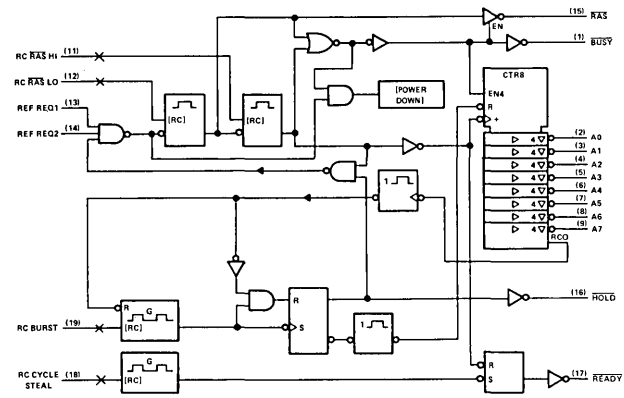
- Controls refresh cycle of 64K dynamic RAM's
- Three-state outputs drive bus lines directly
- Time to initiate refresh request is typically 30 ns
- Refresh modes: cycle steal, burst

SN54LS603A (J) SN74LS603A (J,N)

pin assignments

J, N PACKAGES			
1	$\overline{BUSY}$	11	RC $\overline{RAS}$ HI
2	A0	12	RC $\overline{RAS}$ LO
3	A1	13	REF REQ1
4	A2	14	REF REQ2
5	A3	15	$\overline{RAS}$
6	A4	16	$\overline{HOLD}$
7	A5	17	$\overline{READY}$
8	A6	18	RC CYCLE STEAL
9	A7	19	RC BURST
10	GND	20	V_{CC}

logic diagram†



For chip carrier information, contact the factory.

†Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

TEXAS INSTRUMENTS
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604, 605
606, 607

OCTAL 2-INPUT MULTIPLEXED REGISTERS

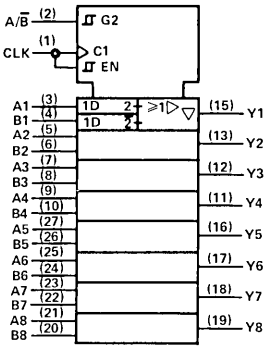
- 16 D-type registers — one for each data input
- 'LS604 and 'LS606 feature three-state outputs
- Multiplexers select stored data from either A or B bus
- Application-oriented:
  - max speed - ('LS604, 'LS605)
  - glitch-free operation - ('LS606, 'LS607)

typical performance

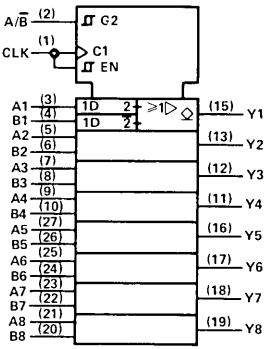
TYPE	DELAY	POWER
'LS604	23.5 ns	275 mW
'LS605	26 ns	200 mW
'LS606	31 ns	275 mW
'LS607	31 ns	200 mW

SN54LS604 (JD,FH) SN74LS604 (JD,N,FN)
SN54LS605 (JD,FH) SN74LS605 (JD,N,FN)
SN54LS606 (JD,FH) SN74LS606 (JD,N,FN)
SN54LS607 (JD,FH) SN74LS607 (JD,N,FN)

logic symbol, 'LS604, 'LS606†



logic symbol, 'LS605, 'LS607†



pin assignments

JD, N PACKAGES				FH, FN PACKAGES			
1	CLK	15	Y1	1	CLK	15	Y1
2	$A/\overline{B}$	16	Y5	2	$A/\overline{B}$	16	Y5
3	A1	17	Y6	3	A1	17	Y6
4	B1	18	Y7	4	B1	18	Y7
5	A2	19	Y8	5	A2	19	Y8
6	B2	20	B8	6	B2	20	B8
7	A3	21	A8	7	A3	21	A8
8	B3	22	B7	8	B3	22	B7
9	A4	23	A7	9	A4	23	A7
10	B4	24	B6	10	B4	24	B6
11	Y4	25	A6	11	Y4	25	A6
12	Y3	26	B5	12	Y3	26	B5
13	Y2	27	A5	13	Y2	27	A5
14	GND	28	V_{CC}	14	GND	28	V_{CC}

6

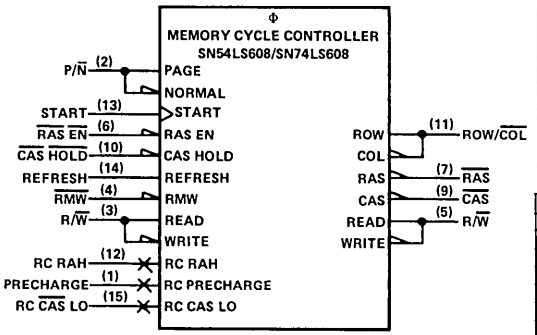
†Pin numbers shown on logic symbols are for JD and N packages only.

608

MEMORY CYCLE CONTROLLERS

- Read cycle
- Write cycle
- Read, modify, write cycle
- RAS only refresh cycle
- Page or normal modes
- Stand-alone controller for CPU-to-memory interface

logic symbol†



SN54LS608 (J,FH) SN74LS608 (J,N,FN)

pin assignments

J, N PACKAGES			
1	PRECHARGE	9	$\overline{CAS}$
2	P/$\overline{N}$	10	$\overline{CAS}$ $\overline{HOLD}$
3	R/$\overline{W}$ in	11	ROW/$\overline{COL}$
4	$\overline{RMW}$	12	RC RAH
5	R/$\overline{W}$ out	13	START
6	$\overline{RAS}$ $\overline{EN}$	14	REFRESH
7	$\overline{RAS}$	15	RC $\overline{CAS}$ LO
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	PRECHARGE	12	$\overline{CAS}$
3	P/$\overline{N}$	13	$\overline{CAS}$ $\overline{HOLD}$
4	R/$\overline{W}$ in	14	ROW/$\overline{COL}$
5	$\overline{RMW}$	15	RC RAH
6	nc	16	nc
7	R/$\overline{W}$ out	17	START
8	$\overline{RAS}$ $\overline{EN}$	18	REFRESH
9	$\overline{RAS}$	19	RC $\overline{CAS}$ LO
10	GND	20	V_{CC}

†Pin numbers shown on logic symbols are for J and N packages only.

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610, 611 612, 613

MEMORY MAPPERS

typical performance

TYPE	MAP OUTPUTS LATCHED	MAP OUTPUT TYPE
'LS610	Yes	3-State
'LS611	Yes	O-C
'LS612	No	3-State
'LS613	No	O-C

- Designed for paged memory mapping
- Expands four address lines to 12 address lines

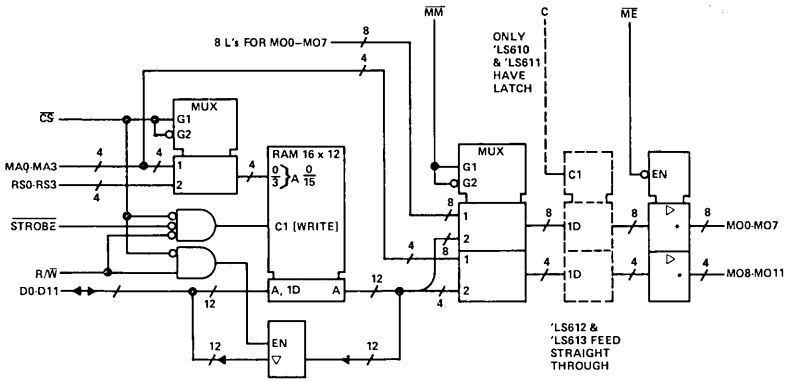
SN54LS610 (JD,FC) SN74LS610 (JD,N)
SN54LS611 (JD,FC) SN74LS611 (JD,N)
SN54LS612 (JD,FC) SN74LS612 (JD,N)
SN54LS613 (JD,FC) SN74LS613 (JD,N)

pin assignments

JD, N PACKAGES		FC PACKAGE	
1 RS2	21 $\overline{ME}$	1 RS2	23 $\overline{ME}$
2 MA3	22 MO6	2 MA3	24 MO6
3 RS3	23 MO7	3 RS3	25 MO7
4 $\overline{CS}$	24 MO8	4 $\overline{CS}$	26 MO8
5 $\overline{STROBE}$	25 MO9	5 $\overline{STROBE}$	27 MO9
6 R/$\overline{W}$	26 MO10	6 nc	28 nc
7 D0	27 MO11	7 R/$\overline{W}$	29 MO10
8 D1	28 ★	8 D0	30 MO11
9 D2	29 D6	9 D1	31 ★
10 D3	30 D7	10 D2	32 D6
11 D4	31 D8	11 D3	33 D7
12 D5	32 D9	12 D4	34 D8
13 $\overline{MM}$	33 D10	13 D5	35 D9
14 MO0	34 D11	14 $\overline{MM}$	36 D10
15 MO1	35 MA0	15 MO0	37 D11
16 MO2	36 RS0	16 MO1	38 MA0
17 MO3	37 MA1	17 nc	39 nc
18 MO4	38 RS1	18 MO2	40 RS0
19 MO5	39 MA2	19 MO3	41 MA1
20 GND	40 V_{CC}	20 MO4	42 RS1
		21 MO5	43 MA2
		22 GND	44 V_{CC}

★ C on 'LS610 and 'LS611
nc on 'LS612 and 'LS613

functional block diagram (positive logic)



*'LS610 and 'LS612 have 3-state (▽) map outputs.
'LS611 and 'LS613 have open-collector (◇) map outputs.

nc — no internal connection.

620, 621
622, 623

OCTAL BUS TRANSCEIVERS

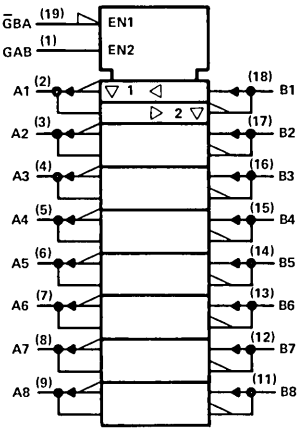
- Bidirectional bus transceivers
- Local bus latch capability

typical performance

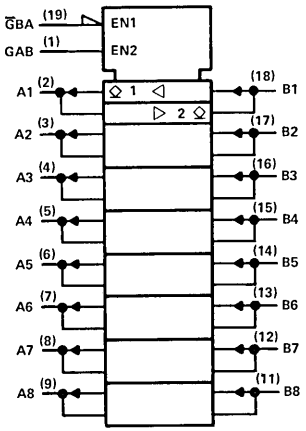
TYPE	OUTPUT	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54ALS620	3-State	−12 mA	12 mA
SN74ALS620	3-State	−15 mA	24 mA
SN74ALS620-1	3-State	−15 mA	48 mA
SN54ALS621	O-C	—	12 mA
SN74ALS621	O-C	—	24 mA
SN74ALS621-1	O-C	—	48 mA
SN54ALS622	O-C	—	12 mA
SN74ALS622	O-C	—	24 mA
SN74ALS622-1	O-C	—	48 mA
SN54ALS623	3-State	−12 mA	12 mA
SN74ALS623	3-State	−15 mA	24 mA
SN74ALS623-1	3-State	−15 mA	48 mA
SN54LS620	3-State	−12 mA	12 mA
SN74LS620	3-State	−15 mA	24 mA
SN54LS621	O-C	—	12 mA
SN74LS621	O-C	—	24 mA
SN54LS622	O-C	—	12 mA
SN74LS622	O-C	—	24 mA
SN54LS623	3-State	−12 mA	12 mA
SN74LS623	3-State	−15 mA	24 mA

SN54ALS620 (J,FH)	SN74ALS620 (N,FN) SN74ALS620-1 (N,FN)
SN54ALS621 (J,FH)	SN74ALS621 (N,FN) SN74ALS621-1 (N,FN)
SN54ALS622 (J,FH)	SN74ALS622 (N,FN) SN74ALS622-1 (N,FN)
SN54ALS623 (J,FH)	SN74ALS623 (N,FN) SN74ALS623-1 (N,FN)
SN54LS620 (J,FH)	SN74LS620 (J,N,FN)
SN54LS621 (J,FH)	SN74LS621 (J,N,FN)
SN54LS622 (J,FH)	SN74LS622 (J,N,FN)
SN54LS623 (J,FH)	SN74LS623 (J,N,FN)

logic symbol, 'ALS620, 'LS620†



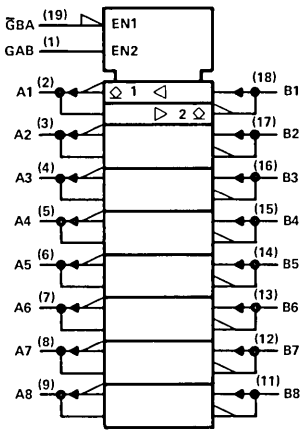
logic symbol, 'ALS621, 'LS621†



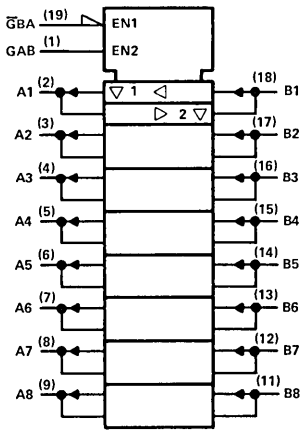
pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	GAB	11	B8	1	GAB	11	B8
2	A1	12	B7	2	A1	12	B7
3	A2	13	B6	3	A2	13	B6
4	A3	14	B5	4	A3	14	B5
5	A4	15	B4	5	A4	15	B4
6	A5	16	B3	6	A5	16	B3
7	A6	17	B2	7	A6	17	B2
8	A7	18	B1	8	A7	18	B1
9	A8	19	$\overline{GBA}$	9	A8	19	$\overline{GBA}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

logic symbol, 'ALS622, 'LS622†



logic symbol, 'ALS623, 'LS623†



† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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624

VOLTAGE-CONTROLLED OSCILLATORS

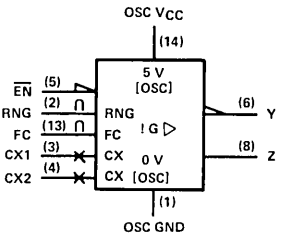
typical performance

TYPE	REPLACES
'LS624	'LS324

- Separate supply voltage pins for isolation of input/output signals
- Maximum output frequency = 20 MHz
- Improved version of original VCO family

SN54LS624 (J,FH) SN74LS624 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	OSC GND	8	Z
2	RNG	9	V_{CC}
3	CX1	10	nc
4	CX2	11	nc
5	$\overline{EN}$	12	nc
6	Y	13	FREQ CONT
7	GND	14	OSC V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	OSC GND	12	Z
3	RNG	13	V_{CC}
4	CX1	14	nc
5	nc	15	nc
6	CX2	16	nc
7	nc	17	nc
8	$\overline{EN}$	18	nc
9	Y	19	FREQ CONT
10	GND	20	OSC V_{CC}

625

VOLTAGE-CONTROLLED OSCILLATORS

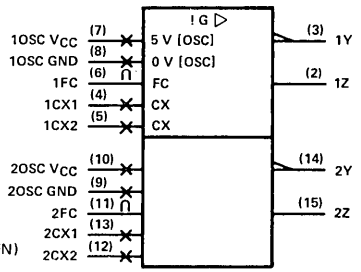
typical performance

TYPE	REPLACES
'LS625	'LS325

- Separate supply voltage pins for input/output isolation
- Maximum output frequency = 20 MHz
- Improved version of original family

SN54LS625 (J,FH) SN74LS625 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	GND	9	2OSC GND
2	1Z	10	2OSC V_{CC}
3	1Y	11	2FC
4	1CX1	12	2CX2
5	1CX2	13	2CX1
6	1FC	14	2Y
7	1OSC V_{CC}	15	2Z
8	1OSC GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	GND	12	2OSC GND
3	1Z	13	2OSC V_{CC}
4	1Y	14	2FC
5	1CX1	15	2CX2
6	nc	16	nc
7	1CX2	17	2CX1
8	1FC	18	2Y
9	1OSC V_{CC}	19	2Z
10	1OSC GND	20	V_{CC}

626

VOLTAGE-CONTROLLED OSCILLATORS

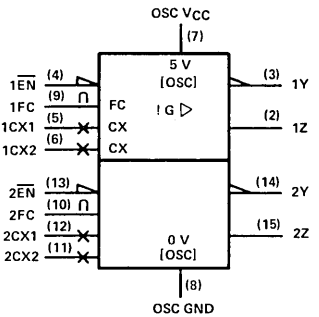
typical performance

TYPE	REPLACES
'LS626	'LS326

- Separate supply voltage pins for input/output isolation
- Maximum output frequency = 20 MHz
- Improved version of original family

SN54LS626 (J,FH) SN74LS626 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	GND	9	1FC
2	1Z	10	2FC
3	1Y	11	2CX2
4	$1\overline{EN}$	12	2CX1
5	1CX1	13	$2\overline{EN}$
6	1CX2	14	2Y
7	OSC V_{CC}	15	2Z
8	OSC GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	GND	12	1FC
3	1Z	13	2FC
4	1Y	14	2CX2
5	$1\overline{EN}$	15	2CX1
6	nc	16	nc
7	1CX1	17	$2\overline{EN}$
8	1CX2	18	2Y
9	OSC V_{CC}	19	2Z
10	OSC GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

627

VOLTAGE-CONTROLLED OSCILLATORS

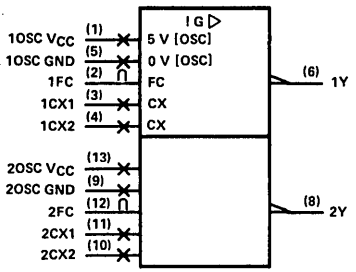
typical performance

TYPE	REPLACES
'LS627	'LS327

- Separate supply voltage pins for input/output isolation
- Maximum output frequency = 20 MHz
- Improved version of original family

SN54LS627 (J,FH)
SN74LS627 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1OSC VCC	8	2Y	1	nc	11	nc
2	1FC	9	2OSC GND	2	1OSC VCC	12	2Y
3	1CX1	10	2CX2	3	1FC	13	2OSC GND
4	1CX2	11	2CX1	4	1CX1	14	2CX2
5	1OSC GND	12	2FC	5	nc	15	nc
6	1Y	13	2OSC VCC	6	1CX2	16	2CX1
7	GND	14	VCC	7	nc	17	nc
				8	1OSC GND	18	2FC
				9	1Y	19	2OSC VCC
				10	GND	20	VCC

628

VOLTAGE-CONTROLLED OSCILLATORS

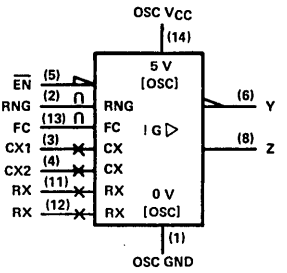
typical performance

TYPE	REPLACES
'LS628	'LS324

- Separate supply voltage pins for input/output oscillators
- Maximum output frequency = 20 MHz
- Improved version of original family

SN54LS628 (J,FH)
SN74LS628 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	OSC GND	8	Z	1	nc	11	nc
2	RNG	9	VCC	2	OSC GND	12	Z
3	CX1	10	nc	3	RNG	13	VCC
4	CX2	11	RX	4	CX1	14	nc
5	$\overline{EN}$	12	RX	5	nc	15	nc
6	Y	13	FC	6	CX2	16	RX
7	GND	14	OSC VCC	7	nc	17	nc
				8	$\overline{EN}$	18	RX
				9	Y	19	FC
				10	GND	20	OSC VCC

629

VOLTAGE-CONTROLLED OSCILLATORS

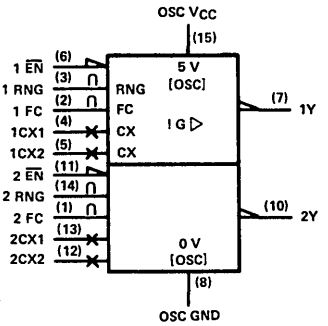
typical performance

TYPE	REPLACES
'LS629	'LS124

- Separate power supply pins for input/output isolation
- Maximum output frequency = 20 MHz
- Improved version of original family

SN54LS629 (J,FH)
SN74LS629 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	2FC	9	GND	1	nc	11	nc
2	1FC	10	2Y	2	2FC	12	GND
3	1RNG	11	2$\overline{EN}$	3	1FC	13	2Y
4	1CX1	12	2CX1	4	1RNG	14	2$\overline{EN}$
5	1CX2	13	2CX2	5	1CX1	15	2CX1
6	1$\overline{EN}$	14	2RNG	6	nc	16	nc
7	1Y	15	OSC VCC	7	1CX2	17	2CX2
8	OSC GND	16	VCC	8	1$\overline{EN}$	18	2RNG
				9	1Y	19	OSC VCC
				10	OSC GND	20	VCC

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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630, 631

16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

- Fast processing times:
  - Write cycle: generates check word in 45 ns typical
  - Read cycle: flags errors in 27 ns typical
- Detects and corrects single bit error
- Detects and flags dual-bit errors

typical performance

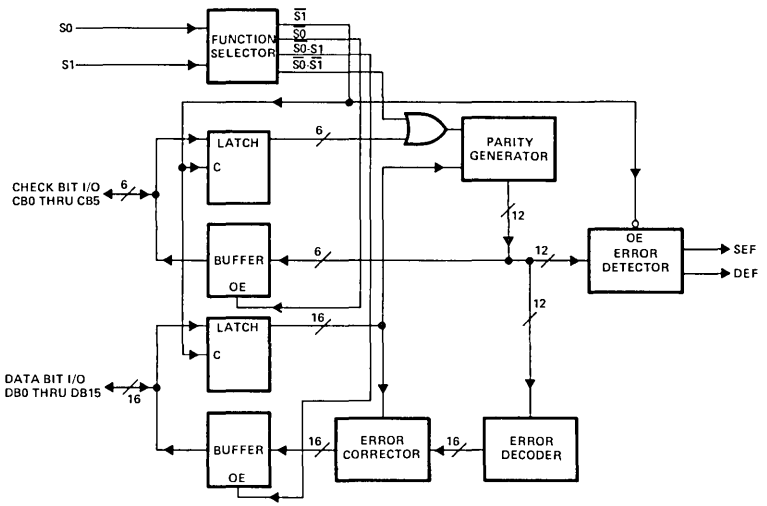
TYPE	OUTPUT	DELAY	POWER
'LS630	3-State	27 ns	715 mW
'LS631	O-C	28 ns	565 mW

SN54LS630 (JD,FH) SN74LS630 (JD,N,FN)
SN54LS631 (JD,FH) SN74LS631 (JD,N,FN)

pin assignments

JD, N PACKAGES				FH, FN PACKAGES			
1	DEF	15	DB12	1	DEF	15	DB12
2	DB0	16	DB13	2	DB0	16	DB13
3	DB1	17	DB14	3	DB1	17	DB14
4	DB2	18	DB15	4	DB2	18	DB15
5	DB3	19	CB5	5	DB3	19	CB5
6	DB4	20	CB4	6	DB4	20	CB4
7	DB5	21	CB3	7	DB5	21	CB3
8	DB6	22	CB2	8	DB6	22	CB2
9	DB7	23	CB1	9	DB7	23	CB1
10	DB8	24	CB0	10	DB8	24	CB0
11	DB9	25	SO	11	DB9	25	SO
12	DB10	26	S1	12	DB10	26	S1
13	DB11	27	SEF	13	DB11	27	SEF
14	GND	28	V_{CC}	14	GND	28	V_{CC}

functional block diagram



nc — no internal connection.

632, 633

32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

- Detects and Corrects Single-bit errors
- Detects and Flags dual-bit errors
- Fast processing times
- Byte-Write capability

typical performance

TYPE	OUTPUT	DELAY	POWER
'ALS632	3-State		
'ALS633	O-C		

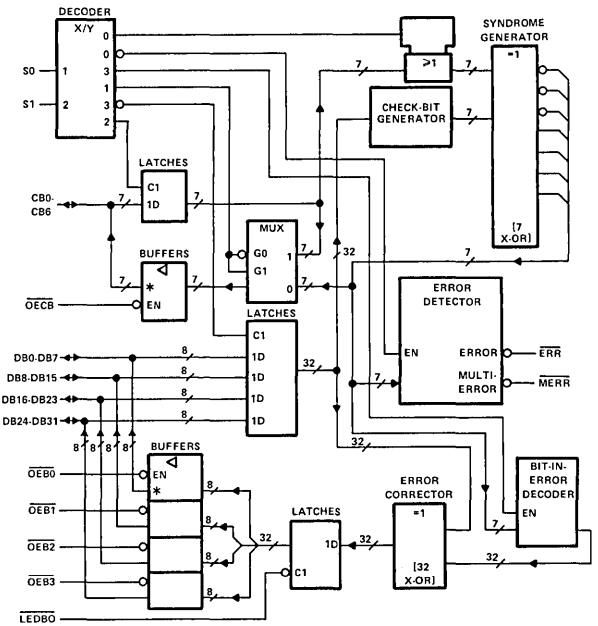
SN54ALS632 (JD) SN74ALS632 (N)
SN54ALS633 (JD) SN74ALS633 (N)

pin assignments

JD, N PACKAGES			
1	$\overline{\text{LEDBO}}$	27	CB3
2	$\overline{\text{MERR}}$	28	CB2
3	$\overline{\text{ERR}}$	29	CB1
4	DB0	30	CB0
5	DB1	31	DB16
6	DB2	32	DB17
7	DB3	33	DB18
8	DB4	34	DB19
9	DB5	35	DB20
10	$\overline{\text{OEB0}}$	36	DB21
11	DB6	37	$\overline{\text{OEB2}}$
12	DB7	38	DB22
13	GND	39	DB23
14	DB8	40	GND
15	DB9	41	DB24
16	$\overline{\text{OEB1}}$	42	DB25
17	DB10	43	$\overline{\text{OEB3}}$
18	DB11	44	DB26
19	DB12	45	DB27
20	DB13	46	DB28
21	DB14	47	DB29
22	DB15	48	DB30
23	CB6	49	DB31
24	CB5	50	S0
25	CB4	51	S1
26	$\overline{\text{OECB}}$	52	V_{CC}

For chip carrier information, contact the factory.

logic diagram (positive logic)



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634, 635

32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

- Detects and Corrects single-bit errors
- Detects and Flags dual-bit errors
- Fast processing times

typical performance

TYPE	OUTPUT	DELAY	POWER
'ALS634	3-State		
'ALS635	O-C		

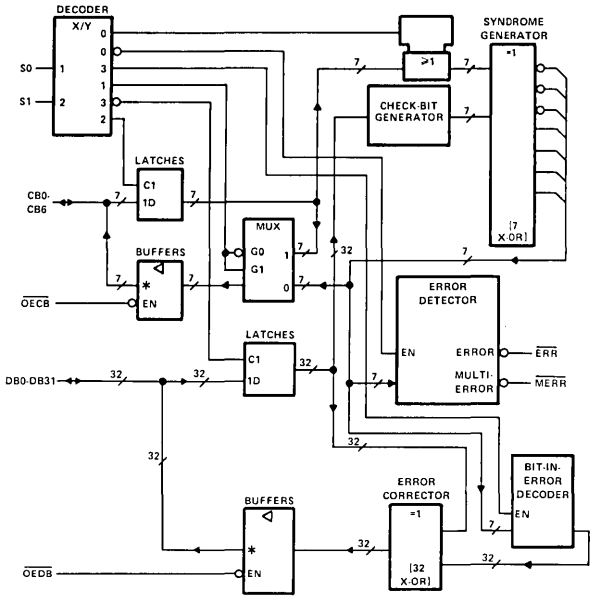
SN54ALS634 (JD) SN74ALS634 (N)
SN54ALS635 (JD) SN74ALS635 (N)

pin assignments

JD, N PACKAGES			
1	$\overline{MERR}$	25	CB3
2	$\overline{ERR}$	26	CB2
3	DB0	27	CB1
4	DB1	28	CB0
5	DB2	29	DB16
6	DB3	30	DB17
7	DB4	31	DB18
8	DB5	32	DB19
9	$\overline{OEDB}$	33	DB20
10	DB6	34	DB21
11	DB7	35	DB22
12	GND	36	DB23
13	DB8	37	GND
14	DB9	38	DB24
15	DB10	39	DB25
16	DB11	40	DB26
17	DB12	41	DB27
18	DB13	42	DB28
19	DB14	43	DB29
20	DB15	44	DB30
21	CB6	45	DB31
22	CB5	46	S0
23	CB4	47	S1
24	$\overline{OECB}$	48	V_{CC}

For chip carrier information, contact the factory.

logic diagram (positive logic)



636, 637

8-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

- Fast processing times:
  - Write cycle: generates check word in 45 ns typical
  - Read cycle: flags errors in 27 ns typical
- Detects and corrects single bit error
- Detects and flags dual-bit errors

typical performance

TYPE	OUTPUT	DELAY	POWER
'LS636	3-State	27 ns	500 mW
'LS637	O-C	28 ns	450 mW

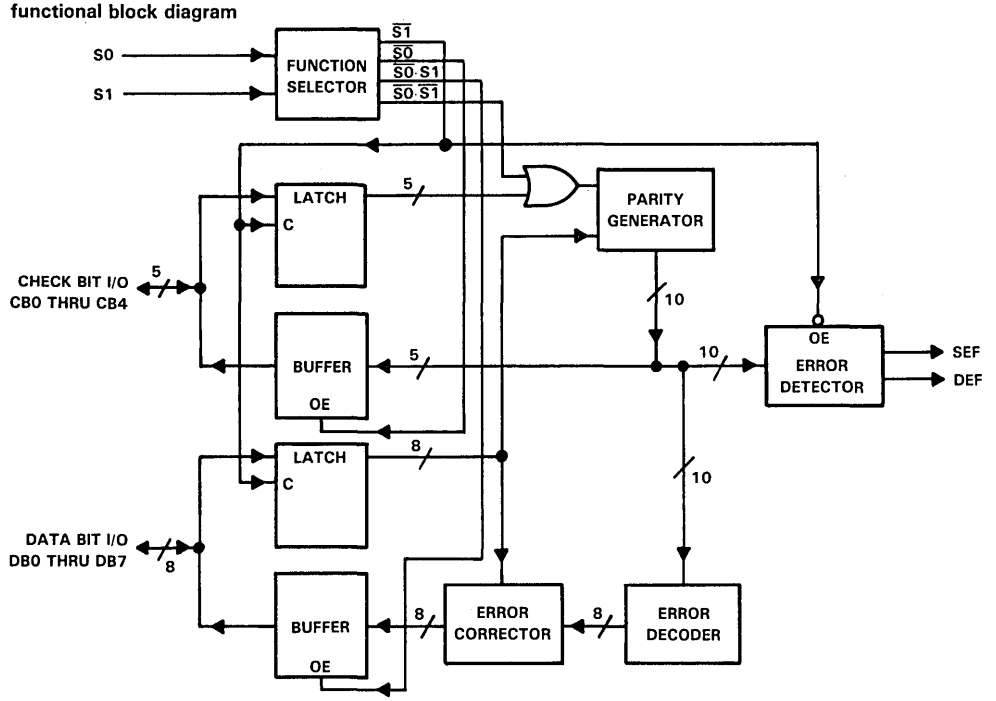
SN54LS636 (J) SN74LS636 (J,N)
SN54LS637 (J) SN74LS637 (J,N)

pin assignments

J, N PACKAGES			
1	DEF	11	CB4
2	DB0	12	nc
3	DB1	13	CB3
4	DB2	14	CB2
5	DB3	15	CB1
6	DB4	16	CB0
7	DB5	17	S0
8	DB6	18	S1
9	DB7	19	SEF
10	GND	20	V_{CC}

For chip carrier information, contact the factory.

functional block diagram



nc — no internal connection.

TEXAS INSTRUMENTS
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638, 639

OCTAL BUS TRANSCEIVERS

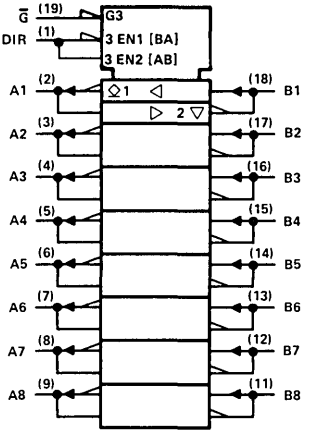
- Bidirectional bus transceivers
- "A" bus outputs are open-collector; "B" bus outputs are three-state
- 'ALS638, 'LS638 – inverting logic
- 'ALS639, 'LS639 – true logic

typical performance

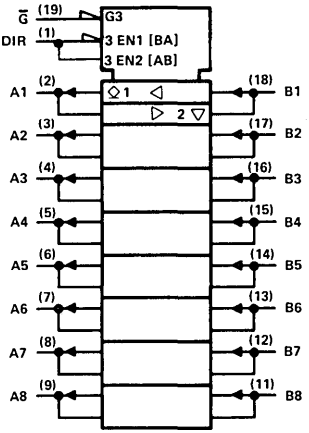
TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54ALS638	5 ns	−12 mA	12 mA
SN74ALS638	5 ns	−15 mA	24 mA
SN74ALS638-1	5 ns	−15 mA	48 mA
SN54ALS639	6 ns	−12 mA	12 mA
SN74ALS639	6 ns	−15 mA	24 mA
SN74ALS639-1	6 ns	−15 mA	48 mA
SN54LS638	11 ns	−12 mA	12 mA
SN74LS638	11 ns	−15 mA	24 mA
SN54LS639	13.5 ns	−12 mA	12 mA
SN74LS639	13.5 ns	−15 mA	24 mA

SN54ALS638 (J,FH) SN74ALS638 (N,FN)
SN74ALS638-1 (N,FN)
SN54ALS639 (J,FH) SN74ALS639 (N,FN)
SN74ALS639-1 (N,FN)
SN54LS638 (J,FH) SN74LS638 (J,N,FN)
SN54LS639 (J,FH) SN74LS639 (J,N,FN)

logic symbol, 'ALS638, 'LS638†



logic symbol, 'ALS639, 'LS639†



pin assignments

J, N PACKAGES			
1	DIR	11	B8
2	A1	12	B7
3	A2	13	B6
4	A3	14	B5
5	A4	15	B4
6	A5	16	B3
7	A6	17	B2
8	A7	18	B1
9	A8	19	$\overline{G}$
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	DIR	11	B8
2	A1	12	B7
3	A2	13	B6
4	A3	14	B5
5	A4	15	B4
6	A5	16	B3
7	A6	17	B2
8	A7	18	B1
9	A8	19	$\overline{G}$
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc – no internal connection.

640, 641, 642
643, 644, 645

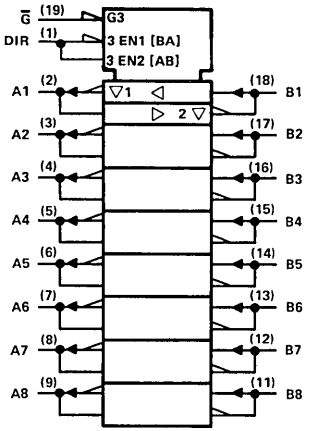
OCTAL BUS TRANSCEIVERS

TYPE	OUTPUT	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54ALS640	3-State	5 ns	−12 mA	12 mA
SN74ALS640	3-State	5 ns	−15 mA	24 mA
SN74ALS640-1	3-State	5 ns	−15 mA	48 mA
SN54ALS641	O-C	15 ns	N/A	12 mA
SN74ALS641	O-C	15 ns	N/A	24 mA
SN74ALS641-1	O-C	15 ns	N/A	48 mA
SN54ALS642	O-C	20 ns	N/A	12 mA
SN74ALS642	O-C	20 ns	N/A	24 mA
SN74ALS642-1	O-C	20 ns	N/A	48 mA
SN54ALS643	3-State	5 ns	−12 mA	12 mA
SN74ALS643	3-State	5 ns	−15 mA	24 mA
SN74ALS643-1	3-State	5 ns	−15 mA	48 mA
SN54ALS644	O-C	20 ns	N/A	12 mA
SN74ALS644	O-C	20 ns	N/A	24 mA
SN74ALS644-1	O-C	20 ns	N/A	48 mA
SN54ALS645	3-State	6 ns	−12 mA	12 mA
SN74ALS645	3-State	6 ns	−15 mA	24 mA
SN74ALS645-1	3-State	6 ns	−15 mA	48 mA
SN54LS640	3-State	7 ns	−12 mA	12 mA
SN74LS640	3-State	7 ns	−15 mA	24 mA
SN74LS640-1	3-State	7 ns	−15 mA	48 mA
SN54LS641	O-C	16.5 ns	N/A	12 mA
SN74LS641	O-C	16.5 ns	N/A	24 mA
SN74LS641-1	O-C	16.5 ns	N/A	48 mA
SN54LS642	O-C	16.5 ns	N/A	12 mA
SN74LS642	O-C	16.5 ns	N/A	24 mA
SN74LS642-1	O-C	16.5 ns	N/A	48 mA
SN54LS643	3-State	8.5 ns	−12 mA	12 mA
SN74LS643	3-State	8.5 ns	−15 mA	24 mA
SN74LS643-1	3-State	8.5 ns	−15 mA	48 mA
SN54LS644	O-C	16.5 ns	N/A	12 mA
SN74LS644	O-C	16.5 ns	N/A	24 mA
SN74LS644-1	O-C	16.5 ns	N/A	48 mA
SN54LS645	3-State	9.5 ns	−12 mA	12 mA
SN74LS645	3-State	9.5 ns	−15 mA	24 mA
SN74LS645-1	3-State	9.5 ns	−15 mA	48 mA

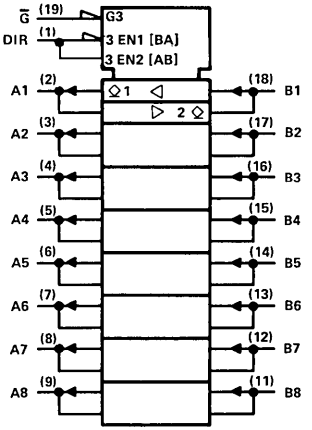
pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	DIR	11	B8	1	DIR	11	B8
2	A1	12	B7	2	A1	12	B7
3	A2	13	B6	3	A2	13	B6
4	A3	14	B5	4	A3	14	B5
5	A4	15	B4	5	A4	15	B4
6	A5	16	B3	6	A5	16	B3
7	A6	17	B2	7	A6	17	B2
8	A7	18	B1	8	A7	18	B1
9	A8	19	$\overline{G}$	9	A8	19	$\overline{G}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

logic symbol, 'ALS640, 'LS640†



logic symbol, 'ALS641, 'LS641†



SN54ALS640 (J,FH)
SN54ALS641 (J,FH)
SN54ALS642 (J,FH)
SN54ALS643 (J,FH)
SN54ALS644 (J,FH)
SN54ALS645 (J,FH)
SN54LS640 (J,FH)
SN54LS641 (J,FH)
SN54LS642 (J,FH)
SN54LS643 (J,FH)
SN54LS644 (J,FH)
SN54LS645 (J,FH)

SN74ALS640 (N,FN)
SN74ALS641 (N,FN)
SN74ALS642 (N,FN)
SN74ALS643 (N,FN)
SN74ALS644 (N,FN)
SN74ALS645 (N,FN)
SN74LS640 (J,N,FN)
SN74LS641 (J,N,FN)
SN74LS642 (J,N,FN)
SN74LS643 (J,N,FN)
SN74LS644 (J,N,FN)
SN74LS645 (J,N,FN)

SN74ALS640-1 (N,FN)
SN74ALS641-1 (N,FN)
SN74ALS642-1 (N,FN)
SN74ALS643-1 (N,FN)
SN74ALS644-1 (N,FN)
SN74ALS645-1 (N,FN)
SN74LS640-1 (J,N,FN)
SN74LS641-1 (J,N,FN)
SN74LS642-1 (J,N,FN)
SN74LS643-1 (J,N,FN)
SN74LS644-1 (J,N,FN)
SN74LS645-1 (J,N,FN)

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

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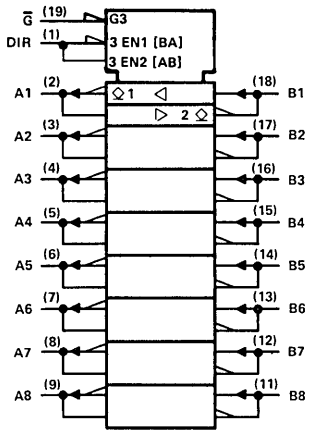
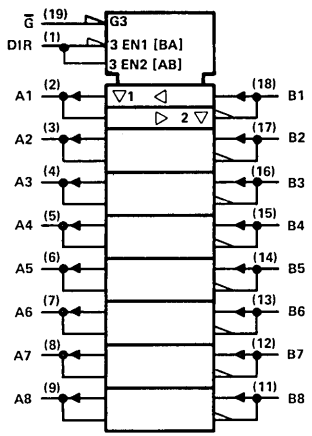
640, 641, 642
643, 644 645 continued

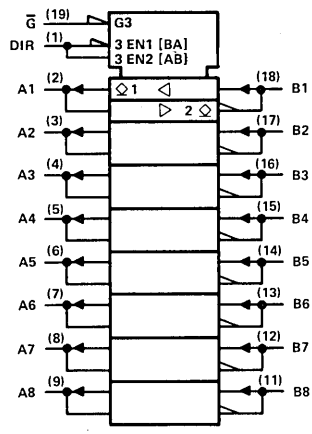
logic symbol, 'LS642†



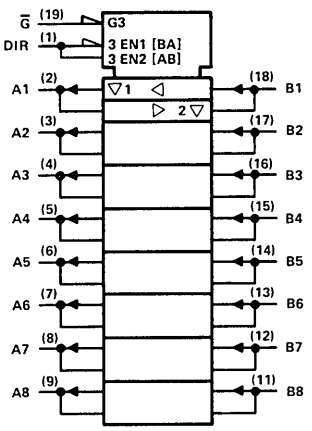
logic symbol, 'ALS643, 'LS643†



logic symbol, 'LS644†



logic symbol, 'ALS645, 'LS645†



† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

646, 647, 648, 649

OCTAL BUS TRANSCEIVERS AND REGISTERS

- Bidirectional
- Independent registers for A and B busses

typical performance

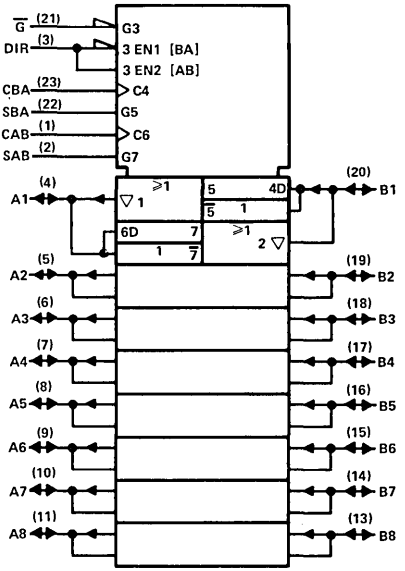
TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	OUTPUT TYPE	OUTPUT INV
SN54ALS646		−12 mA	12 mA	3-State	No
SN74ALS646		−15 mA	24 mA	3-State	No
SN74ALS646-1		−15 mA	48 mA	3-State	No
SN54ALS647		N/A	12 mA	O-C	No
SN74ALS647		N/A	24 mA	O-C	No
SN74ALS647-1		N/A	48 mA	O-C	No
SN54ALS648		−12 mA	12 mA	3-State	Yes
SN74ALS648		−15 mA	24 mA	3-State	Yes
SN74ALS648-1		−15 mA	48 mA	3-State	Yes
SN54ALS649		N/A	12 mA	O-C	Yes
SN74ALS649		N/A	24 mA	O-C	Yes
SN74ALS649-1		N/A	48 mA	O-C	Yes
SN54LS646	19 ns	−12 mA	12 mA	3-State	No
SN74LS646	19 ns	−15 mA	24 mA	3-State	No
SN74LS647	25 ns	N/A	12 mA	O-C	No
SN74LS647	25 ns	N/A	24 mA	O-C	No
SN54LS648	20.5 ns	−12 mA	12 mA	3-State	Yes
SN74LS648	20.5 ns	−15 mA	24 mA	3-State	Yes
SN54LS649	25 ns	N/A	12 mA	O-C	Yes
SN74LS649	25 ns	N/A	24 mA	O-C	Yes

pin assignments

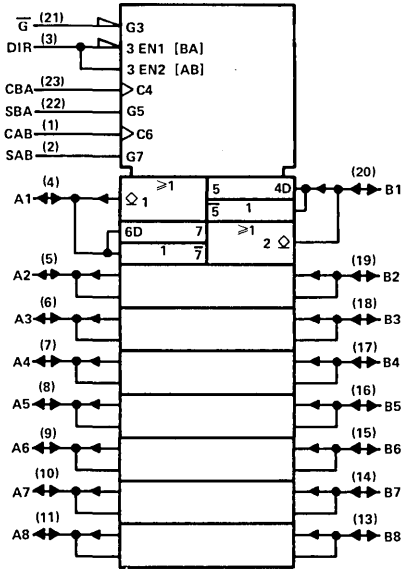
JT, NT PACKAGES				FH, FN PACKAGES			
1	CAB	13	B8	1	nc	15	nc
2	SAB	14	B7	2	CAB	16	B8
3	DIR	15	B6	3	SAB	17	B7
4	A1	16	B5	4	DIR	18	B6
5	A2	17	B4	5	A1	19	B5
6	A3	18	B3	6	A2	20	B4
7	A4	19	B2	7	A3	21	B3
8	A5	20	B1	8	nc	22	nc
9	A6	21	$\overline{G}$	9	A4	23	B2
10	A7	22	SBA	10	A5	24	B1
11	A8	23	CBA	11	A6	25	$\overline{G}$
12	GND	24	V_{CC}	12	A7	26	SBA
				13	A8	27	CBA
				14	GND	28	V_{CC}

SN54ALS646 (JT,FH) SN74ALS646 (NT,FN)
SN74ALS646-1 (NT,FN)
SN54ALS647 (JT,FH) SN74ALS647 (NT,FN)
SN74ALS647-1 (NT,FN)
SN54ALS648 (JT,FH) SN74ALS648 (NT,FN)
SN74ALS648-1 (NT,FN)
SN54ALS649 (JT,FH) SN74ALS649 (NT,FN)
SN74ALS649-1 (NT,FN)
SN54LS646 (JT,FH) SN74LS646 (JT,NT,FN)
SN54LS647 (JT,FH) SN74LS647 (JT,NT,FN)
SN54LS648 (JT,FH) SN74LS648 (JT,NT,FN)
SN54LS649 (JT,FH) SN74LS649 (JT,NT,FN)

logic symbol, 'ALS646, 'LS646†



logic symbol, 'ALS647, 'LS647†



†Pin numbers shown on logic symbols are for JT and NT packages only.
nc — no internal connection.

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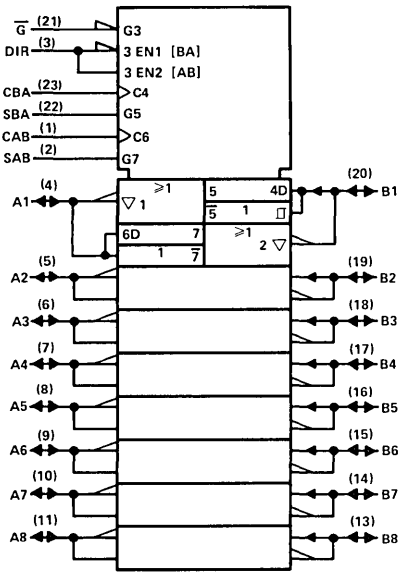
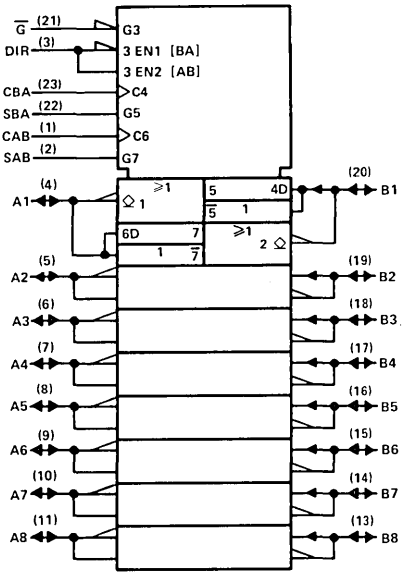
646, 647, 648, 649 continued

logic symbol, 'ALS648, 'LS648†



logic symbol, 'ALS649, 'LS649†



†Pin numbers shown on logic symbols are for JT and NT packages only.
nc — no internal connection.

651, 652

OCTAL BUS TRANSCEIVERS AND REGISTERS

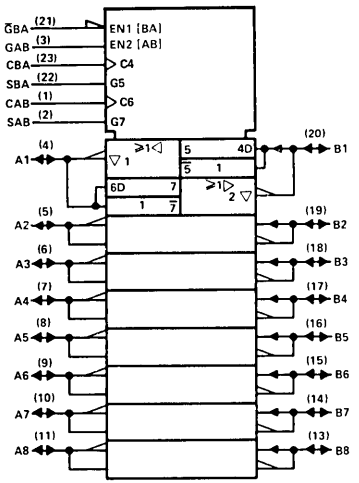
- Bidirectional
- Independent registers for A and B busses

typical performance

TYPE	MAX SOURCE CURRENT	MAX SINK CURRENT	OUTPUT TYPE A B	OUTPUT INV A,B
SN54ALS651	−12 mA	12 mA	3-State	Yes
SN54LS651	−12 mA	12 mA	3-State	Yes
SN74ALS651	−15 mA	24 mA	3-State	Yes
SN74ALS651-1	−15 mA	48 mA	3-State	Yes
SN74LS651	−15 mA	24 mA	3-State	Yes
SN54ALS652	−12 mA	12 mA	3-State	No
SN54LS652	−12 mA	12 mA	3-State	No
SN74ALS652	−15 mA	24 mA	3-State	No
SN74ALS652-1	−15 mA	48 mA	3-State	No
SN74LS652	−15 mA	24 mA	3-State	No

SN54ALS651 (JT,FH) SN74ALS651 (NT,FN)
SN74ALS651-1 (NT,FN)
SN54LS651 (JT,FH) SN74LS651 (JT,NT,FN)
SN54ALS652 (JT,FH) SN74ALS652 (NT,FN)
SN74ALS652-1 (NT,FN)
SN54LS652 (JT,FH) SN74LS652 (JT,NT,FN)

logic symbol, 'ALS651, 'LS651†

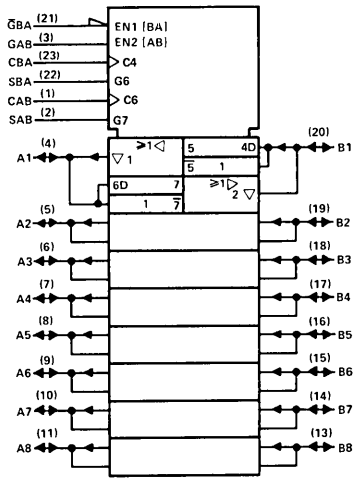


pin assignments

JT, NT PACKAGES			
1	CAB	13	B8
2	SAB	14	B7
3	GAB	15	B6
4	A1	16	B5
5	A2	17	B4
6	A3	18	B3
7	A4	19	B2
8	A5	20	B1
9	A6	21	G̅BA
10	A7	22	SBA
11	A8	23	CBA
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	CAB	16	B8
3	SAB	17	B7
4	GAB	18	B6
5	A1	19	B5
6	A2	20	B4
7	A3	21	B3
8	nc	22	nc
9	A4	23	B2
10	A5	24	B1
11	A6	25	G̅BA
12	A7	26	SBA
13	A8	27	CBA
14	GND	28	V_{CC}

logic symbol, 'ALS652, 'LS652†



†Pin numbers shown on logic symbols are for JT and NT packages only.
nc – no internal connection.

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653, 654

OCTAL BUS TRANSCEIVERS AND REGISTERS

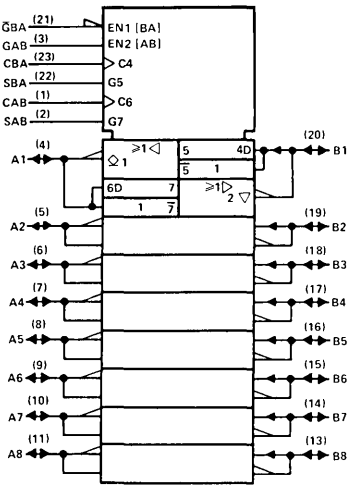
- Bidirectional
- Independent registers for A and B busses

typical performance

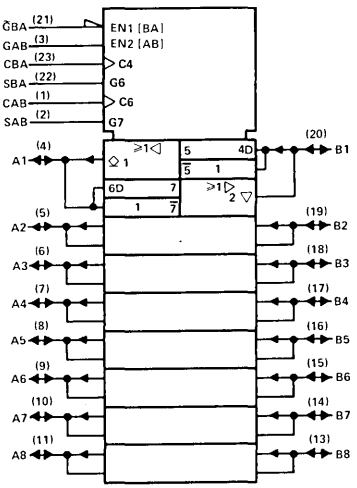
TYPE	MAX SOURCE CURRENT	MAX SINK CURRENT	OUTPUT TYPE A	OUTPUT TYPE B	INV A, B
SN54ALS653	−12 mA	12 mA	O-C	3-State	Yes
SN74ALS653	−15 mA	24 mA	O-C	3-State	Yes
SN74ALS653-1	−15 mA	48 mA	O-C	3-State	Yes
SN54ALS654	−12 mA	12 mA	O-C	3-State	No
SN74ALS654	−15 mA	24 mA	O-C	3-State	No
SN74ALS654-1	−15 mA	48 mA	O-C	3-State	No
SN54LS653	−12 mA	12 mA	O-C	3-State	Yes
SN74LS653	−15 mA	24 mA	O-C	3-State	Yes
SN54LS654	−12 mA	12 mA	O-C	3-State	No
SN74LS654	−15 mA	24 mA	O-C	3-State	No

SN54ALS653 (JT,FH) SN74ALS653 (NT,FN)
SN54ALS654 (JT,FH) SN74ALS653-1 (NT,FN)
SN74ALS654 (NT,FN)
SN74ALS654-1 (NT,FN)
SN54LS653 (JT,FH) SN74LS653 (JT,NT,FN)
SN54LS654 (JT,FH) SN74LS654 (JT,NT,FN)

logic symbol, 'ALS653, 'LS653†



logic symbol, 'ALS654, 'LS654†



pin assignments

JT, NT PACKAGES			
1	CAB	13	B8
2	SAB	14	B7
3	GAB	15	B6
4	A1	16	B5
5	A2	17	B4
6	A3	18	B3
7	A4	19	B2
8	A5	20	B1
9	A6	21	$\overline{\text{GBA}}$
10	A7	22	SBA
11	A8	23	CBA
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	CAB	16	B8
3	SAB	17	B7
4	GAB	18	B6
5	A1	19	B5
6	A2	20	B4
7	A3	21	B3
8	nc	22	nc
9	A4	23	B2
10	A5	24	B1
11	A6	25	$\overline{\text{GBA}}$
12	A7	26	SBA
13	A8	27	CBA
14	GND	28	V_{CC}

6

† Pin numbers shown on logic symbols are for JT and NT packages only.
nc – no internal connection.

668, 669

SYNCHRONOUS 4-BIT UP/ DOWN COUNTERS

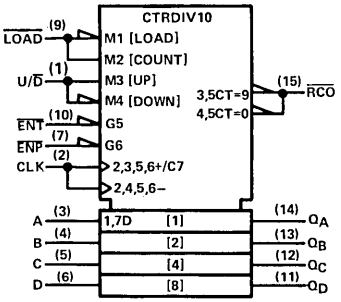
- Programmable, look-ahead
- Decade counter ('LS668)
- Binary counter ('LS669)

typical performance

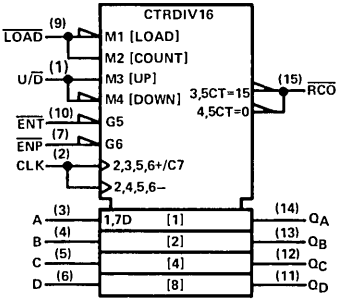
TYPE	COUNT FREQ	PARALLEL LOAD	TOTAL POWER
'LS668	32 MHz	Sync	100 mW
'LS669	32 MHz	Sync	100 mW

SN54LS668 (J,FH) SN74LS668 (J,N,FN)
SN54LS669 (J,FH) SN74LS669 (J,N,FN)

logic symbol, 'LS668†



logic symbol, 'LS669†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	U/D	9	LOAD	1	nc	11	nc
2	CLK	10	ENT	2	U/D	12	LOAD
3	A	11	Q_D	3	CLK	13	ENT
4	B	12	Q_C	4	A	14	Q_D
5	C	13	Q_B	5	B	15	Q_C
6	D	14	Q_A	6	nc	16	nc
7	ENP	15	RCO	7	C	17	Q_B
8	GND	16	V_{CC}	8	D	18	Q_A
				9	ENP	19	RCO
				10	GND	20	V_{CC}

670

4-BY-4 REGISTER FILES

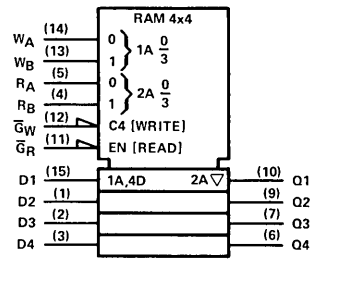
- 3-state outputs
- Simultaneous read/write
- Expandable to 1024 words

typical performance

ADDRESS TIME	ENABLE TIME	POWER/ BIT
24 ns	19 ns	9.3 mW

SN54LS670 (J,FH) SN74LS670 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	D2	9	Q2	1	nc	11	nc
2	D3	10	Q1	2	D2	12	Q2
3	D4	11	$\overline{G}_R$	3	D3	13	Q1
4	R_B	12	$\overline{G}_W$	4	D4	14	$\overline{G}_R$
5	R_A	13	W_B	5	R_B	15	$\overline{G}_W$
6	Q4	14	W_A	6	nc	16	nc
7	Q3	15	D1	7	R_A	17	W_B
8	GND	16	V_{CC}	8	Q4	18	W_A
				9	Q3	19	D1
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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671, 672

4-BIT UNIVERSAL SHIFT REGISTERS/LATCHES WITH THREE-STATE OUTPUTS

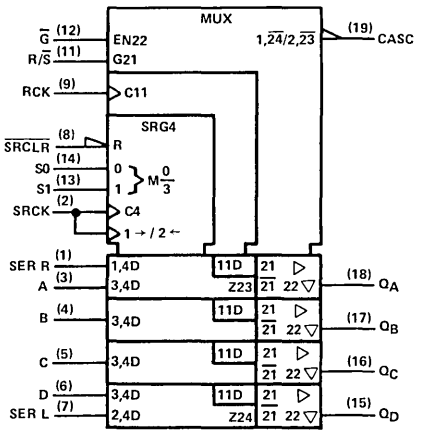
- '671 has direct SR clear
- '672 has synchronous SR clear
- Expandable to any word length
- Multiplexed outputs for shift register or latched data
- Four modes of shift register
  - Inhibit clock
  - Shift right
  - Shift left
  - Parallel load

typical performance

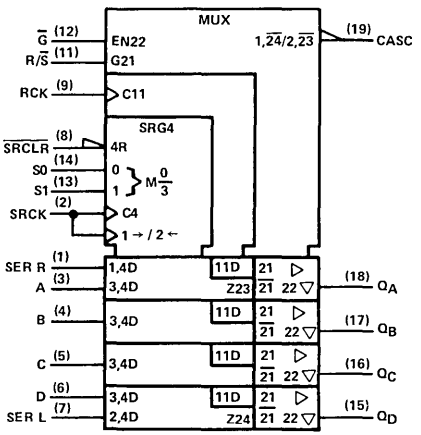
TYPE	TOTAL POWER
'LS671	170 mW
'LS672	170 mW

SN54LS671 (J,FH) SN74LS671 (J,N,FN)
SN54LS672 (J,FH) SN74LS672 (J,N,FN)

logic symbol, 'LS671†



logic symbol, 'LS672†



pin assignments

J, N PACKAGES			
1	SER R	11	R/S̅
2	SRCK	12	G̅
3	A	13	S1
4	B	14	S0
5	C	15	Q_D
6	D	16	Q_C
7	SER L	17	Q_B
8	SRCLR̅	18	Q_A
9	RCK	19	CASC
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	SER R	11	R/S̅
2	SRCK	12	G̅
3	A	13	S1
4	B	14	S0
5	C	15	Q_D
6	D	16	Q_C
7	SER L	17	Q_B
8	SRCLR̅	18	Q_A
9	RCK	19	CASC
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

673

16-BIT SHIFT REGISTERS

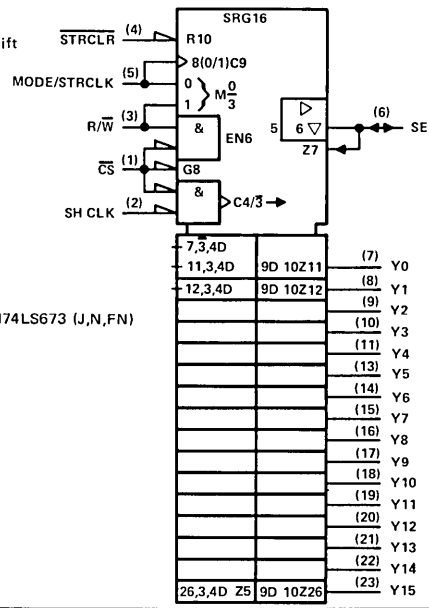
- 16-bit serial-in/serial-out shift register with three-state outputs
- 16-bit parallel-out storage register
- Converts serial to parallel data flow

typical performance

TYPE	SHIFT FREQ	TOTAL POWER
'LS673	20 MHz	255 mW

SN54LS673 (J,FH) SN74LS673 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	$\overline{CS}$	13	Y5
2	SH CLK	14	Y6
3	R/$\overline{W}$	15	Y7
4	$\overline{STRCLR}$	16	Y8
5	MODE/STRCLR	17	Y9
6	SER/Q15	18	Y10
7	Y0	19	Y11
8	Y1	20	Y12
9	Y2	21	Y13
10	Y3	22	Y14
11	Y4	23	Y15
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	$\overline{CS}$	16	Y5
3	SH CLK	17	Y6
4	R/$\overline{W}$	18	Y7
5	$\overline{STRCLR}$	19	Y8
6	MODE/STRCLR	20	Y9
7	SER/Q15	21	Y10
8	nc	22	nc
9	Y0	23	Y11
10	Y1	24	Y12
11	Y2	25	Y13
12	Y3	26	Y14
13	Y4	27	Y15
14	GND	28	V_{CC}

674

16-BIT SHIFT REGISTER

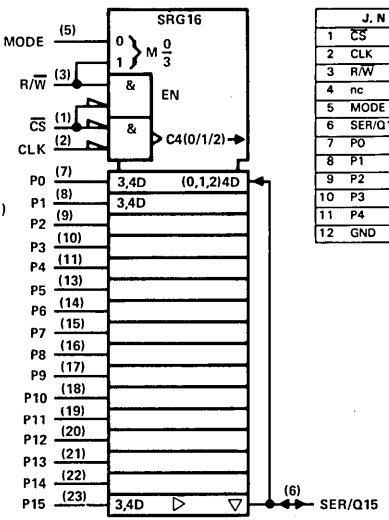
- Performs parallel to serial conversion
- Three-state outputs

typical performance

TYPE	SHIFT FREQ	TOTAL POWER
'LS674	20 MHz	125 mW

SN54LS674 (J,FH) SN74LS674 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	$\overline{CS}$	13	P5
2	CLK	14	P6
3	R/$\overline{W}$	15	P7
4	nc	16	P8
5	MODE	17	P9
6	SER/Q15	18	P10
7	P0	19	P11
8	P1	20	P12
9	P2	21	P13
10	P3	22	P14
11	P4	23	P15
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	$\overline{CS}$	16	P5
3	CLK	17	P6
4	R/$\overline{W}$	18	P7
5	nc	19	P8
6	MODE	20	P9
7	SER/Q15	21	P10
8	nc	22	nc
9	P0	23	P11
10	P1	24	P12
11	P2	25	P13
12	P3	26	P14
13	P4	27	P15
14	GND	28	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
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677, 678

ADDRESS COMPARATORS

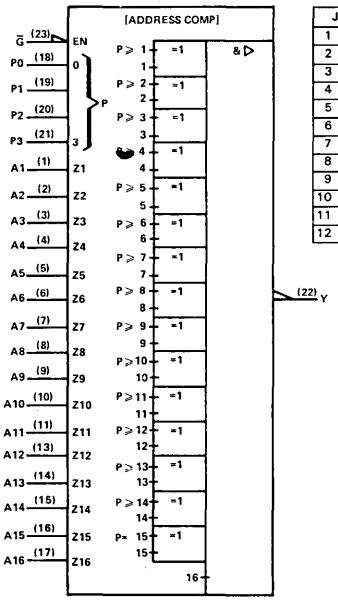
- 'ALS677 is a 16-bit to 4-bit comparator with enable
- 'ALS678 is a 16-bit to 4-bit comparator with latch

typical performance

TYPE	DELAY	POWER
'ALS677		
'ALS678		

SN54ALS677 (JT,FH) SN74ALS677 (NT,FN)
SN54ALS678 (JT,FH) SN74ALS678 (NT,FN)

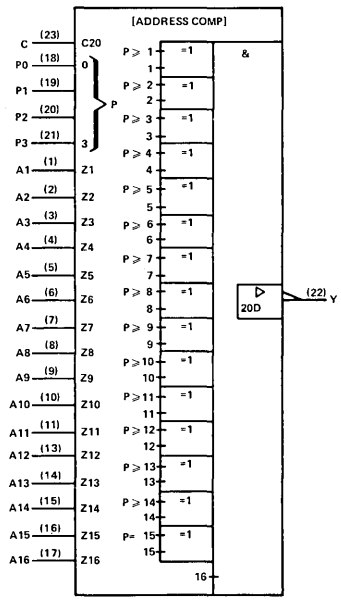
logic symbol, 'ALS677†



pin assignments, 'ALS677

JT, NT PACKAGES				FH, FN PACKAGES			
1	A1	13	A12	1	nc	15	nc
2	A2	14	A13	2	A1	16	A12
3	A3	15	A14	3	A2	17	A13
4	A4	16	A15	4	A3	18	A14
5	A5	17	A16	5	A4	19	A15
6	A6	18	P0	6	A5	20	A16
7	A7	19	P1	7	A6	21	P0
8	A8	20	P2	8	nc	22	nc
9	A9	21	P3	9	A7	23	P1
10	A10	22	Y	10	A8	24	P2
11	A11	23	$\overline{G}$	11	A9	25	P3
12	GND	24	V_{CC}	12	A10	26	Y
				13	A11	27	$\overline{G}$
				14	GND	28	V_{CC}

logic symbol, 'ALS678†



pin assignments, 'ALS678

JT, NT PACKAGES				FH, FN PACKAGES			
1	A1	13	A12	1	nc	15	nc
2	A2	14	A13	2	A1	16	A12
3	A3	15	A14	3	A2	17	A13
4	A4	16	A15	4	A3	18	A14
5	A5	17	A16	5	A4	19	A15
6	A6	18	P0	6	A5	20	A16
7	A7	19	P1	7	A6	21	P0
8	A8	20	P2	8	nc	22	nc
9	A9	21	P3	9	A7	23	P1
10	A10	22	Y	10	A8	24	P2
11	A11	23	C	11	A9	25	P3
12	GND	24	V_{CC}	12	A10	26	Y
				13	A11	27	C
				14	GND	28	V_{CC}

†Pin numbers shown on logic symbols are for JT and NT packages only.
nc — no internal connection.

679, 680

ADDRESS COMPARATORS

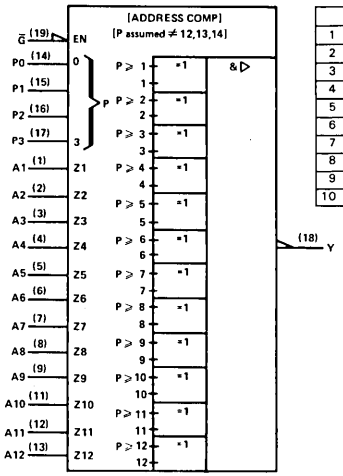
- 'ALS679 is a 12-bit to 4-bit comparator with enable
- 'ALS680 is a 12-bit to 4-bit comparator with latch

typical performance

TYPE	DELAY	POWER
'ALS679		
'ALS680		

SN54ALS679 (J,FH) SN74ALS679 (N,FN)
SN54ALS680 (J,FH) SN74ALS680 (N,FN)

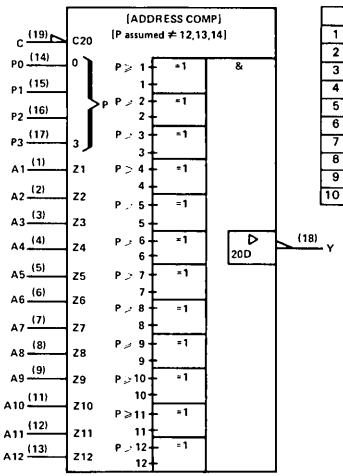
logic symbol, 'ALS679†



pin assignments, 'ALS679

J, N PACKAGES				FH, FN PACKAGES			
1	A1	11	A10	1	A1	11	A10
2	A2	12	A11	2	A2	12	A11
3	A3	13	A12	3	A3	13	A12
4	A4	14	P0	4	A4	14	P0
5	A5	15	P1	5	A5	15	P1
6	A6	16	P2	6	A6	16	P2
7	A7	17	P3	7	A7	17	P3
8	A8	18	Y	8	A8	18	Y
9	A9	19	$\overline{G}$	9	A9	19	$\overline{G}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

logic symbol, 'ALS680†



pin assignments, 'ALS680

J, N PACKAGES				FH, FN PACKAGES			
1	A1	11	A10	1	A1	11	A10
2	A2	12	A11	2	A2	12	A11
3	A3	13	A12	3	A3	13	A12
4	A4	14	P0	4	A4	14	P0
5	A5	15	P1	5	A5	15	P1
6	A6	16	P2	6	A6	16	P2
7	A7	17	P3	7	A7	17	P3
8	A8	18	Y	8	A8	18	Y
9	A9	19	C	9	A9	19	C
10	GND	20	V_{CC}	10	GND	20	V_{CC}

†Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
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681

4-BIT PARALLEL BINARY ACCUMULATORS

- Contains two synchronous registers
- B register frequency = 20 MHz
- Arithmetic operations include B minus A and A minus B
- Bus-driving I/O ports

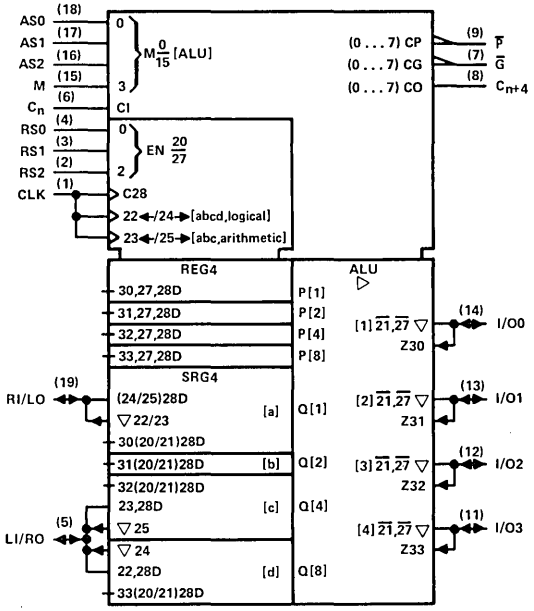
typical performance

TYPE	LOAD TIME	ACC TIME
'LS681	75 ns	50 ns

SN54LS681 (J,FH)

SN74LS681 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	CLK	11	I/O3
2	RS2	12	I/O2
3	RS1	13	I/O1
4	RS0	14	I/O0
5	LI/RO	15	M
6	C_n	16	AS2
7	$\overline{G}$	17	AS1
8	C_{n+4}	18	AS0
9	$\overline{P}$	19	RI/LO
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	CLK	11	I/O3
2	RS2	12	I/O2
3	RS1	13	I/O1
4	RS0	14	I/O0
5	LI/RO	15	M
6	C_n	16	AS2
7	$\overline{G}$	17	AS1
8	C_{n+4}	18	AS0
9	$\overline{P}$	19	RI/LO
10	GND	20	V_{CC}

†Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

682, 683, 684, 685

8-BIT MAGNITUDE COMPARATORS

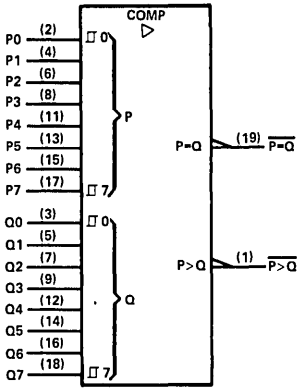
- Compares two 8-bit words
- 'LS682 and 'LS683 includes 20-kilohm pull-up resistor on Q inputs

typical performance

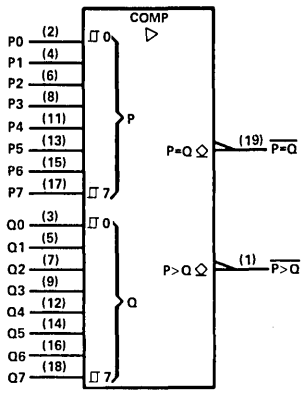
TYPE	COMPARE TIME	TYPE OUTPUT	TOTAL POWER
'LS682	14 ns	Totem Pole	210 mW
'LS683	24 ns	O-C	210 mW
'LS684	16 ns	Totem Pole	200 mW
'LS685	24 ns	O-C	200 mW

SN54LS682 (J,FH) SN74LS682 (J,N,FN)
SN54LS683 (J,FH) SN74LS683 (J,N,FN)
SN54LS684 (J,FH) SN74LS684 (J,N,FN)
SN54LS685 (J,FH) SN74LS685 (J,N,FN)

logic symbol, 'LS682, 'LS684†



logic symbol, 'LS683, 'LS685†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	P>Q	11	P4	1	P>Q	11	P4
2	P0	12	Q4	2	P0	12	Q4
3	Q0	13	P5	3	Q0	13	P5
4	P1	14	Q5	4	P1	14	Q5
5	Q1	15	P6	5	Q1	15	P6
6	P2	16	Q6	6	P2	16	Q6
7	Q2	17	P7	7	Q2	17	P7
8	P3	18	Q7	8	P3	18	Q7
9	Q3	19	P=Q	9	Q3	19	P=Q
10	GND	20	V_{CC}	10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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686, 687

8-BIT MAGNITUDE COMPARATORS

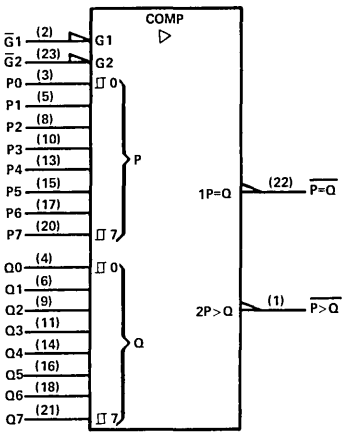
- Compares two 8-bit words

typical performance

TYPE	COMPARE TIME	TYPE OUTPUT	TOTAL POWER
'LS686	17 ns	Totem-Pole	220 mW
'LS687	22 ns	O-C	220 mW

SN54LS686 (JT,FH) SN74LS686 (JT,NT,FN)
SN54LS687 (JT,FH) SN74LS687 (JT,NT,FN)

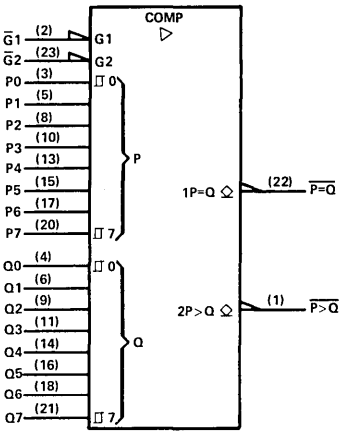
logic symbol, 'LS686†



pin assignments

JT, NT PACKAGES				FH, FN PACKAGES			
1	P>Q	13	P4	1	nc	15	nc
2	G1	14	Q4	2	P>Q	16	P4
3	P0	15	P5	3	G1	17	Q4
4	Q0	16	Q5	4	P0	18	P5
5	P1	17	P6	5	Q0	19	Q5
6	Q1	18	Q6	6	P1	20	P6
7	nc	19	nc	7	Q1	21	Q6
8	P2	20	P7	8	nc	22	nc
9	Q2	21	Q7	9	nc	23	nc
10	P3	22	P=Q	10	P2	24	P7
11	Q3	23	G2	11	Q2	25	Q7
12	GND	24	V_{CC}	12	P3	26	P=Q
				13	Q3	27	G2
				14	GND	28	V_{CC}

logic symbol, 'LS687†



†Pin numbers shown on logic symbols are for JT and NT packages only.
nc — no internal connection.

688, 689

8-BIT MAGNITUDE COMPARATORS

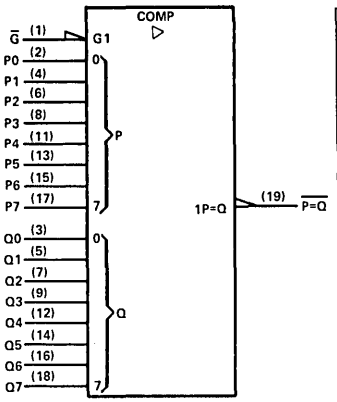
- Compares two 8-bit words

typical performance

TYPE	COMPARE TIME	TYPE OUTPUT	TOTAL POWER
'ALS688	9.5 ns	Totem-Pole	37.5 mW
'ALS689	15..5 ns	O-C	37.5 mW
'LS688	14.5 ns	Totem-Pole	200 mW
'LS689	23 ns	O-C	200 mW

SN54ALS688 (J,FH) SN74ALS688 (J,FN)
SN54ALS689 (J,FH) SN74ALS689 (N,FN)
SN54LS688 (J,FH) SN74LS688 (J,N,FN)
SN54LS689 (J,FH) SN74LS689 (J,N,FN)

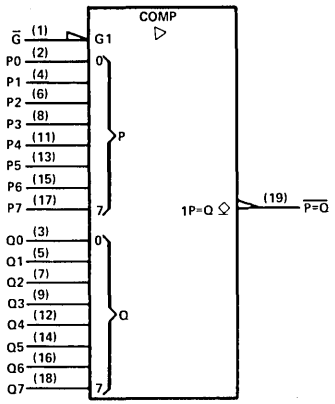
logic symbol, 'ALS688, 'LS688†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{G}$	11	P4	1	$\overline{G}$	11	P4
2	P0	12	Q4	2	P0	12	Q4
3	Q0	13	P5	3	Q0	13	P5
4	P1	14	Q5	4	P1	14	Q5
5	Q1	15	P6	5	Q1	15	P6
6	P2	16	Q6	6	P2	16	Q6
7	Q2	17	P7	7	Q2	17	P7
8	P3	18	Q7	8	P3	18	Q7
9	Q3	19	$\overline{P=Q}$	9	Q3	19	$\overline{P=Q}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

logic symbol, 'ALS689, 'LS689†



† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
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690, 691
692, 693

SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS

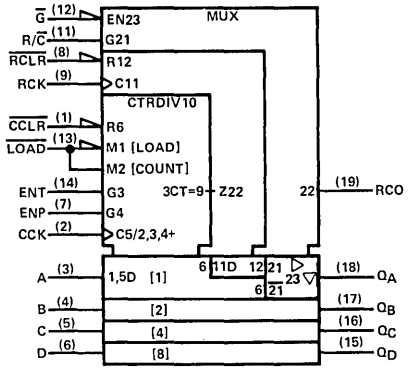
- Multiplexed three-state outputs
- 4-bit counters/registers
- 'LS690, 'LS692: Decade counters
- 'LS691, 'LS693: Binary counters

typical performance

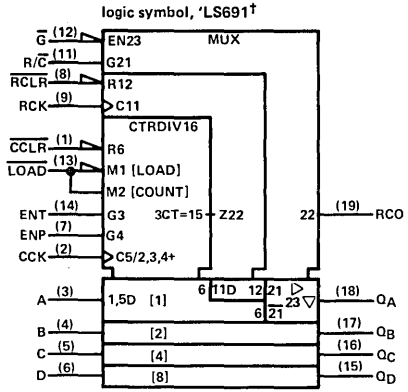
TYPE	CLEAR	MAX CLOCK FREQ	TOTAL POWER
'LS690	Direct	20 MHz	237 mW
'LS691	Direct	20 MHz	237 mW
'LS692	Sync-L	20 MHz	237 mW
'LS693	Sync-L	20 MHz	237 mW

SN54LS690 (J,FH) SN74LS690 (J,N,FN)
SN54LS691 (J,FH) SN74LS691 (J,N,FN)
SN54LS692 (J,FH) SN74LS692 (J,N,FN)
SN54LS693 (J,FH) SN74LS693 (J,N,FN)

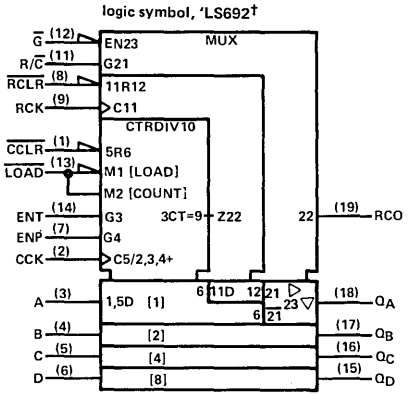
logic symbol, 'LS690†



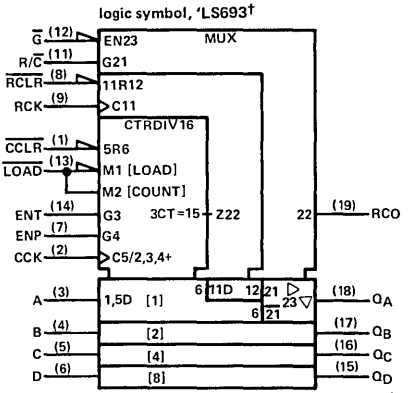
logic symbol, 'LS691†



logic symbol, 'LS692†



logic symbol, 'LS693†



pin assignments

J, N PACKAGES			
1	$\overline{CCLR}$	11	R/$\overline{C}$
2	CCK	12	$\overline{G}$
3	A	13	$\overline{LOAD}$
4	B	14	ENT
5	C	15	Q_D
6	D	16	Q_C
7	ENP	17	Q_B
8	$\overline{RCLR}$	18	Q_A
9	RCK	19	RCO
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	$\overline{CCLR}$	11	R/$\overline{C}$
2	CCK	12	$\overline{G}$
3	A	13	$\overline{LOAD}$
4	B	14	ENT
5	C	15	Q_D
6	D	16	Q_C
7	ENP	17	Q_B
8	$\overline{RCLR}$	18	Q_A
9	RCK	19	RCO
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

696, 697, 698, 699

SYNCHRONOUS UP/DOWN COUNTERS WITH OUTPUT REGISTERS, MULTIPLEXED THREE-STATE OUTPUTS

- 4-bit counters/registers
- 'LS696, 'LS698: Decade counters
- 'LS697, 'LS699: Binary counters

pin assignments

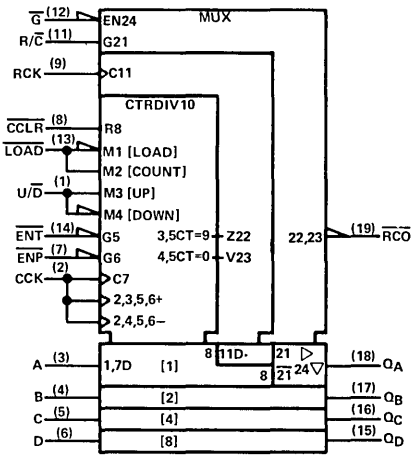
J, N PACKAGES				FH, FN PACKAGES			
1	U/$\overline{D}$	11	R/$\overline{C}$	1	U/D	11	R/$\overline{C}$
2	CCK	12	$\overline{G}$	2	CCK	12	$\overline{G}$
3	A	13	$\overline{LOAD}$	3	A	13	$\overline{LOAD}$
4	B	14	$\overline{ENT}$	4	B	14	$\overline{ENT}$
5	C	15	Q_D	5	C	15	Q_D
6	D	16	Q_C	6	D	16	Q_C
7	$\overline{ENP}$	17	Q_B	7	$\overline{ENP}$	17	Q_B
8	$\overline{CCLR}$	18	Q_A	8	$\overline{CCLR}$	18	Q_A
9	RCK	19	$\overline{RCO}$	9	RCK	19	$\overline{RCO}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

typical performance

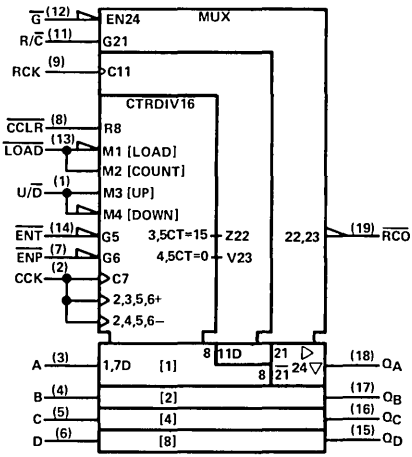
TYPE	MAX CLOCK FREQ	CLEAR	TOTAL POWER
'LS696	20 MHz	Async-L	237 mW
'LS697	20 MHz	Async-L	237 mW
'LS698	20 MHz	Sync-L	237 mW
'LS699	20 MHz	Sync-L	237 mW

SN54LS696 (J,FH) SN74LS696 (J,N,FN)
SN54LS697 (J,FH) SN74LS697 (J,N,FN)
SN54LS698 (J,FH) SN74LS698 (J,N,FN)
SN54LS699 (J,FH) SN74LS699 (J,N,FN)

logic symbol, 'LS696†



logic symbol, 'LS697†



† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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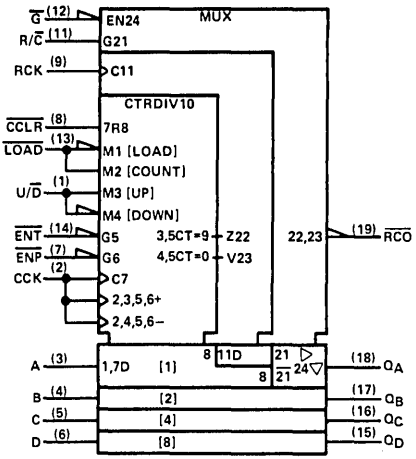
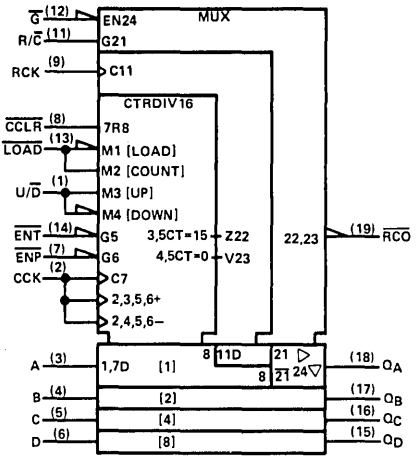
696, 697, 698, 699 continued

logic symbol, 'LS698†



logic symbol, 'LS699†



pin assignments

J, N PACKAGES			
1	U/D	11	R/C
2	CCK	12	G
3	A	13	LOAD
4	B	14	ENT
5	C	15	Q_D
6	D	16	Q_C
7	ENP	17	Q_B
8	CCLR	18	Q_A
9	RCK	19	RCO
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	U/D	11	R/C
2	CCK	12	G
3	A	13	LOAD
4	B	14	ENT
5	C	15	Q_D
6	D	16	Q_C
7	ENP	17	Q_B
8	CCLR	18	Q_A
9	RCK	19	RCO
10	GND	20	V_{CC}

800

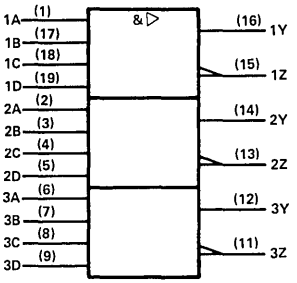
TRIPLE 4-INPUT AND/NAND DRIVERS

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	POWER/GATE
SN54AS800	40 mA	–40 mA	25 mW
SN74AS800	48 mA	–48 mA	25 mW

SN54AS800 (J,FH) SN74AS800 (N,FN)

logic symbol†



positive logic: $Y = ABCD$

$Z = \overline{ABCD}$

pin assignments

J, N PACKAGES			
1	1A	11	3Z
2	2A	12	3Y
3	2B	13	2Z
4	2C	14	2Y
5	2D	15	1Z
6	3A	16	1Y
7	3B	17	1B
8	3C	18	1C
9	3D	19	1D
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	1A	11	3Z
2	2A	12	3Y
3	2B	13	2Z
4	2C	14	2Y
5	2D	15	1Z
6	3A	16	1Y
7	3B	17	1B
8	3C	18	1C
9	3D	19	1D
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc – no internal connection.

802

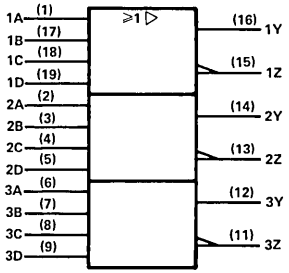
TRIPLE 4-INPUT OR/NOR LINE DRIVERS

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	POWER/GATE
SN54AS802	40 mA	−40 mA	25 mW
SN74AS802	48 mA	−48 mA	25 mW

SN54AS802 (J,FH) SN74AS802 (N,FN)

logic symbol†



positive logic: $Y = A+B+C+D$

$Z = \overline{A+B+C+D}$

pin assignments

J, N PACKAGES			
1	1A	11	3Z
2	2A	12	3Y
3	2B	13	2Z
4	2C	14	2Y
5	2D	15	1Z
6	3A	16	1Y
7	3B	17	1B
8	3C	18	1C
9	3D	19	1D
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	1A	11	3Z
2	2A	12	3Y
3	2B	13	2Z
4	2C	14	2Y
5	2D	15	1Z
6	3A	16	1Y
7	3B	17	1B
8	3C	18	1C
9	3D	19	1D
10	GND	20	V_{CC}

6

804

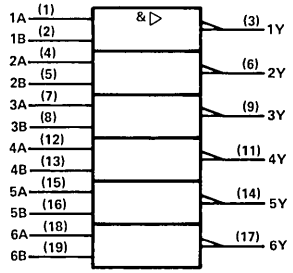
HEX 2-INPUT NAND DRIVERS

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	DELAY	POWER/GATE
SN54ALS804	12 mA	−12 mA	3 ns	3.4 mW
SN74ALS804	24 mA	−15 mA	3 ns	3.4 mW
SN54AS804A	40 mA	−40 mA	2.7 ns	9 mW
SN74AS804A	48 mA	−48 mA	2.7 ns	9 mW

SN54ALS804 (J,FH) SN74ALS804 (N,FN)
SN54AS804A (J,FH) SN74AS804A (N,FN)

logic symbol†



positive logic: $Y = \overline{AB}$

pin assignments

J, N PACKAGES			
1	1A	11	4Y
2	1B	12	4A
3	1Y	13	4B
4	2A	14	5Y
5	2B	15	5A
6	2Y	16	5B
7	3A	17	6Y
8	3B	18	6A
9	3Y	19	6B
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	1A	11	4Y
2	1B	12	4A
3	1Y	13	4B
4	2A	14	5Y
5	2B	15	5A
6	2Y	16	5B
7	3A	17	6Y
8	3B	18	6A
9	3Y	19	6B
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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805

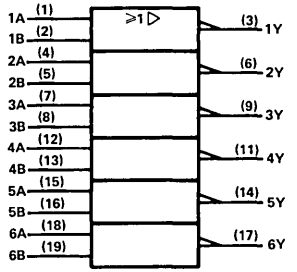
HEX 2-INPUT NOR DRIVERS

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	DELAY	POWER/GATE
SN54ALS805	12 mA	−12 mA	3.5 ns	4.2 mw
SN74ALS805	24 mA	−15 mA	3.5 ns	4.2 mW
SN54AS805A	40 mA	−40 mA	2.7 ns	12 mW
SN74AS805A	48 mA	−48 mA	2.7 ns	12 mW

SN54ALS805 (J,FH) SN74ALS805 (N,FN)
SN54AS805A (J,FH) SN74AS805A (N,FN)

logic symbol†



positive logic: $Y = \overline{A+B}$

pin assignments

J, N PACKAGES			
1	1A	11	4Y
2	1B	12	4A
3	1Y	13	4B
4	2A	14	5Y
5	2B	15	5A
6	2Y	16	5B
7	3A	17	6Y
8	3B	18	6A
9	3Y	19	6B
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	1A	11	4Y
2	1B	12	4A
3	1Y	13	4B
4	2A	14	5Y
5	2B	15	5A
6	2Y	16	5B
7	3A	17	6Y
8	3B	18	6A
9	3Y	19	6B
10	GND	20	V_{CC}

808

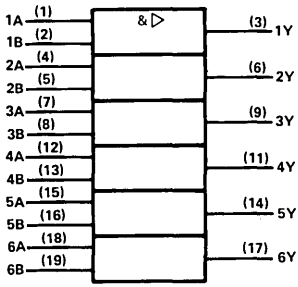
HEX 2-INPUT AND DRIVERS

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	DELAY	POWER/GATE
SN54ALS808	12 mA	−12 mA	4.3 ns	4.5 mW
SN74ALS808	24 mA	−15 mA	4.3 ns	4.5 mW
SN54AS808A	40 mA	−40 mA	3.2 ns	13 mW
SN74AS808A	48 mA	−48 mA	3.2 ns	13 mW

SN54ALS808 (J,FH) SN74ALS808 (N,FN)
SN54AS808A (J,FH) SN74AS808A (N,FN)

logic symbol†



positive logic: $Y = AB$

pin assignments

J, N PACKAGES			
1	1A	11	4Y
2	1B	12	4A
3	1Y	13	4B
4	2A	14	5Y
5	2B	15	5A
6	2Y	16	5B
7	3A	17	6Y
8	3B	18	6A
9	3Y	19	6B
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	1A	11	4Y
2	1B	12	4A
3	1Y	13	4B
4	2A	14	5Y
5	2B	15	5A
6	2Y	16	5B
7	3A	17	6Y
8	3B	18	6A
9	3Y	19	6B
10	GND	20	V_{CC}

6

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

832

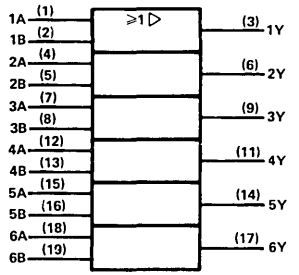
HEX 2-INPUT OR DRIVERS

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	DELAY	POWER/GATE
SN54ALS832	12 mA	−12 mA	4 ns	5.3 mW
SN74ALS832	24 mA	−15 mA	4 ns	5.3 mW
SN54AS832A	40 mA	−40 mA	3 ns	17 mW
SN74AS832A	48 mA	−48 mA	3 ns	17 mW

SN54ALS832 (J,FH) SN74ALS832 (N,FN)
SN54AS832A (J,FH) SN74AS832A (N,FN)

logic symbol†



positive logic: Y = A+B

pin assignments

J, N PACKAGES			
1	1A	11	4Y
2	1B	12	4A
3	1Y	13	4B
4	2A	14	5Y
5	2B	15	5A
6	2Y	16	5B
7	3A	17	6Y
8	3B	18	6A
9	3Y	19	6B
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	1A	11	4Y
2	1B	12	4A
3	1Y	13	4B
4	2A	14	5Y
5	2B	15	5A
6	2Y	16	5B
7	3A	17	6Y
8	3B	18	6A
9	3Y	19	6B
10	GND	20	V_{CC}

6

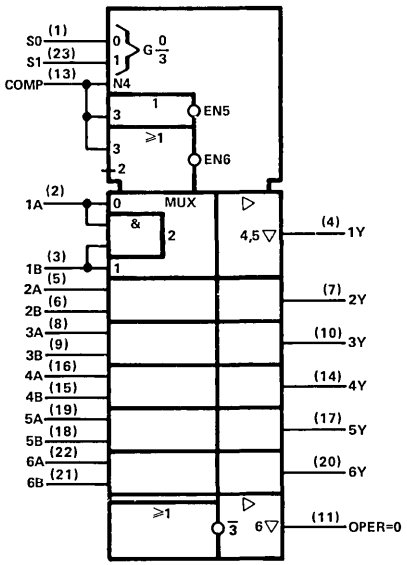
857

HEX 2-TO-1 UNIVERSAL MULTIPLEXER

- Three-state buffer-type outputs
- True or complementary data

SN54ALS857 (JT) SN74ALS857 (JT,NT)
SN54AS857 (JT,FH) SN74AS857 (NT,FN)

logic symbol†



pin assignments

JT, NT PACKAGES			
1	S0	13	COMP
2	1A	14	4Y
3	1B	15	4B
4	1Y	16	4A
5	2A	17	5Y
6	2B	18	5B
7	2Y	19	5A
8	3A	20	6Y
9	3B	21	6B
10	3Y	22	6A
11	OPER=0	23	S1
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	S0	16	COMP
3	1A	17	4Y
4	1B	18	4B
5	1Y	19	4A
6	2A	20	5Y
7	2B	21	5B
8	nc	22	nc
9	2Y	23	5A
10	3A	24	6Y
11	3B	25	6B
12	3Y	26	6A
13	OPER=0	27	S1
14	GND	28	V_{CC}

†Pin numbers shown on logic symbols are for J, JT, N, and NT packages only.
nc — no internal connection.

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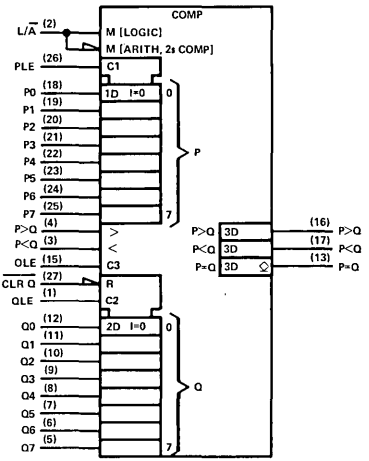
866

8-BIT MAGNITUDE COMPARATORS

- Fast compare to zero
- Arithmetic and logical comparison
- Open-collector output for P = Q

SN54AS866 (JD,FH) SN74AS866 (N,FN)

logic symbol†



pin assignments

JD, N PACKAGES			
1	OLE	15	OLE
2	L/$\overline{A}$	16	P>Qout
3	P<Qin	17	P<Qout
4	P>Qin	18	P0
5	Q7	19	P1
6	Q6	20	P2
7	Q5	21	P3
8	Q4	22	P4
9	Q3	23	P5
10	Q2	24	P6
11	Q1	25	P7
12	Q0	26	PLE
13	P = Qout	27	$\overline{CLRQ}$
14	GND	28	V_{CC}

FH, FN PACKAGES			
1	OLE	15	OLE
2	L/$\overline{A}$	16	P>Qout
3	P<Qin	17	P<Qout
4	P>Qin	18	P0
5	Q7	19	P1
6	Q6	20	P2
7	Q5	21	P3
8	Q4	22	P4
9	Q3	23	P5
10	Q2	24	P6
11	Q1	25	P7
12	Q0	26	PLE
13	P = Qout	27	$\overline{CLRQ}$
14	GND	28	V_{CC}

867, 869

8-BIT SYNCHRONOUS BIDIRECTIONAL COUNTERS

- 'AS867 has asynchronous clear
- 'AS869 has synchronous clear
- Ripple carry output for N-bit cascading
- Fully programmable with synchronous counting and loading

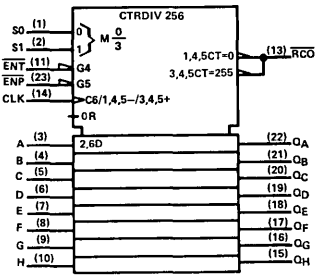
FUNCTION TABLE

S1	S0	FUNCTION
L	L	Clear
L	H	Count Down
H	L	Load
H	H	Count Up

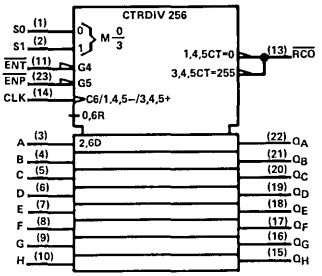
Supersedes table in *1981 Supplement to TTL Data Book*

SN54AS867 (JT,FH) SN74AS867 (NT,FN)
SN54AS869 (JT,FH) SN74AS869 (NT,FN)

logic symbol, 'AS867†



logic symbol, 'AS869†



pin assignments

JT, NT PACKAGES			
1	S0	13	$\overline{RCO}$
2	S1	14	CLK
3	A	15	Q_H
4	B	16	Q_G
5	C	17	Q_F
6	D	18	Q_E
7	E	19	Q_D
8	F	20	Q_C
9	G	21	Q_B
10	H	22	Q_A
11	$\overline{ENT}$	23	$\overline{ENP}$
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	S0	16	$\overline{RCO}$
3	S1	17	CLK
4	A	18	Q_H
5	B	19	Q_G
6	C	20	Q_F
7	D	21	Q_E
8	nc	22	nc
9	E	23	Q_D
10	F	24	Q_C
11	G	25	Q_B
12	H	26	Q_A
13	$\overline{ENT}$	27	$\overline{ENP}$
14	GND	28	V_{CC}

†Pin numbers shown on logic symbols are for JT and NT packages only.

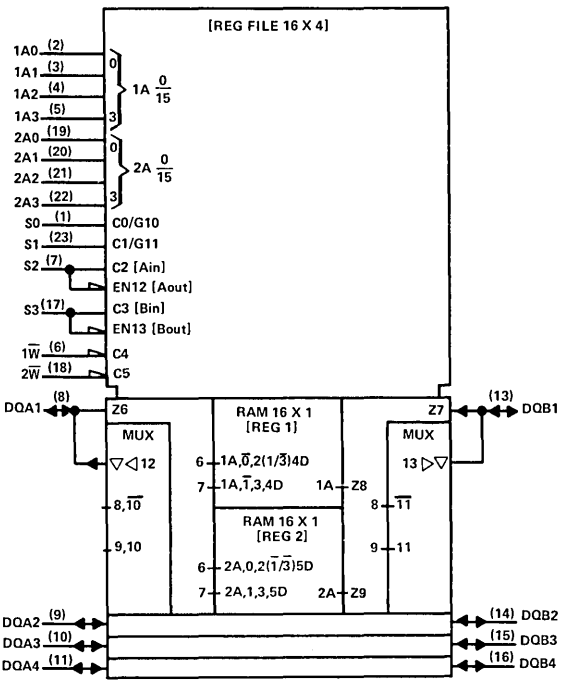
870

DUAL 16-BY-4 REGISTER FILES

- Each register file has individual write/enable controls and address lines
- Has two 4-bit data I/O ports
- 24-pin 300-mil package

SN54AS870 (JT,FH)
SN74AS870 (NT,FN)

logic symbol†



pin assignments

JT, NT PACKAGES			
1	S0	13	DQB1
2	1A0	14	DQB2
3	1A1	15	DQB3
4	1A2	16	DQB4
5	1A3	17	S3
6	$1\overline{W}$	18	$2\overline{W}$
7	S2	19	2A0
8	DQA1	20	2A1
9	DQA2	21	2A2
10	DQA3	22	2A3
11	DQA4	23	S1
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	S0	16	DQB1
3	1A0	17	DQB2
4	1A1	18	DQB3
5	1A2	19	DQB4
6	1A3	20	S3
7	$1\overline{W}$	21	$2\overline{W}$
8	nc	22	nc
9	S2	23	2A0
10	DQA1	24	2A1
11	DQA2	25	2A2
12	DQA3	26	2A3
13	DQA4	27	S1
14	GND	28	V_{CC}

†Pin numbers shown on logic symbols are for JT and NT packages only.
nc — no internal connection.

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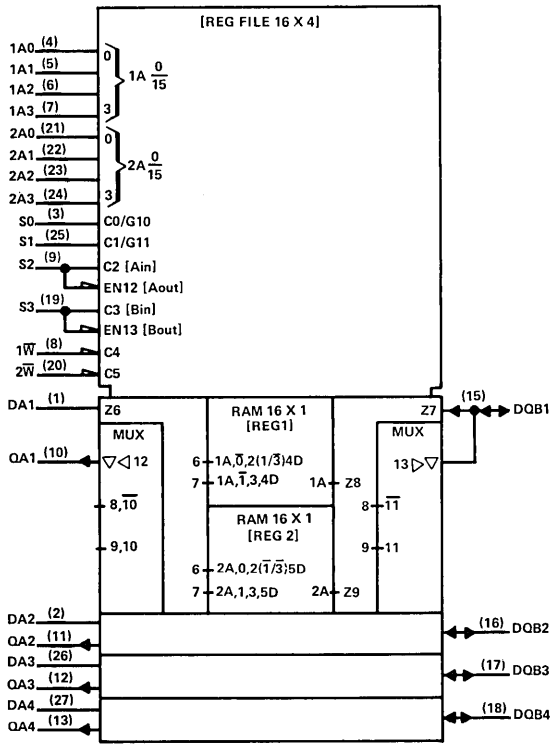
871

DUAL 16-BY-4 REGISTER FILES

- Each register file has individual write/enable controls and address lines
- Has one 4-bit data I/O port; the other 4-bit data word has individual data inputs and data outputs
- 28-pin, 600-mil package

SN54AS871 (J,FH)
SN74AS871 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	DA1	15	DQB1
2	DA2	16	DQB2
3	S0	17	DQB3
4	1A0	18	DQB4
5	1A1	19	S3
6	1A2	20	$\overline{2W}$
7	1A3	21	2A0
8	$\overline{1W}$	22	2A1
9	S2	23	2A2
10	QA1	24	2A3
11	QA2	25	S1
12	QA3	26	DA3
13	QA4	27	DA4
14	GND	28	V_{CC}

FH, FN PACKAGES			
1	DA1	15	DQB1
2	DA2	16	DQB2
3	S0	17	DQB3
4	1A0	18	DQB4
5	1A1	19	S3
6	1A2	20	$\overline{2W}$
7	1A3	21	2A0
8	$\overline{1W}$	22	2A1
9	S2	23	2A2
10	QA1	24	2A3
11	QA2	25	S1
12	QA3	26	DA3
13	QA4	27	DA4
14	GND	28	V_{CC}

6

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

873

DUAL 4-BIT D-TYPE LATCHES

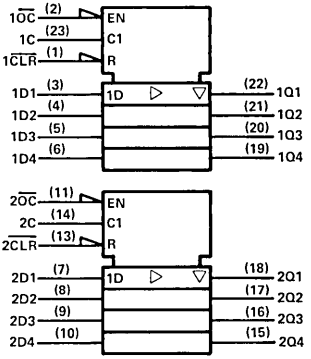
- Three-state buffer-type outputs drive bus lines directly
- Each 4-bit word has enable, clear, and output control inputs

typical performance

TYPE	CLEAR	OUTPUT	DELAY	POWER
'ALS873	LOW	Q	11 ns	67.5 mW

SN54ALS873 (JT,FH) SN74ALS873 (NT,FN)
SN54AS873 (JT,FH) SN74AS873 (NT,FN)

logic symbol†



pin assignments

JT, NT PACKAGES				FH, FN PACKAGES			
1	$1\overline{CLR}$	13	$2\overline{CLR}$	1	nc	15	nc
2	$1\overline{OC}$	14	2C	2	$1\overline{CLR}$	16	$2\overline{CLR}$
3	1D1	15	2Q4	3	$1\overline{OC}$	17	2C
4	1D2	16	2Q3	4	1D1	18	2Q4
5	1D3	17	2Q2	5	1D2	19	2Q3
6	1D4	18	2Q1	6	1D3	20	2Q2
7	2D1	19	1Q4	7	1D4	21	2Q1
8	2D2	20	1Q3	8	nc	22	nc
9	2D3	21	1Q2	9	2D1	23	1Q4
10	2D4	22	1Q1	10	2D2	24	1Q3
11	$2\overline{OC}$	23	1C	11	2D3	25	1Q2
12	GND	24	V_{CC}	12	2D4	26	1Q1
				13	$2\overline{OC}$	27	1C
				14	GND	28	V_{CC}

874

DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

- Three-state buffer-type outputs
- Each 4-bit word has clock, clear, and output control inputs

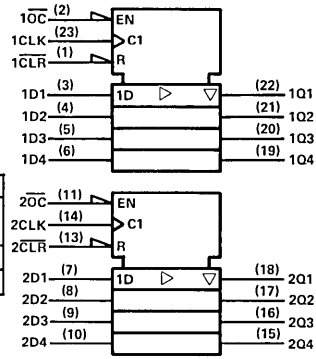
typical performance

TYPE	FREQ	POWER	DATA TIMES	
			SET-UP	HOLD
SN54ALS874	50 MHz	86.7 mW	10 ns↑	4 ns↑
SN74ALS874	50 MHz	86.7 mW	10 ns↑	0 ns↑

↑ Rising edge of clock pulse

SN54ALS874 (JT,FH) SN74ALS874 (NT,FN)
SN54AS874 (JT,FH) SN74AS874 (NT,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$1\overline{CLR}$	13	$2\overline{CLR}$	1	nc	15	nc
2	$1\overline{OC}$	14	2CLK	2	$1\overline{CLR}$	16	$2\overline{CLR}$
3	1D1	15	2Q4	3	$1\overline{OC}$	17	2CLK
4	1D2	16	2Q3	4	1D1	18	2Q4
5	1D3	17	2Q2	5	1D2	19	2Q3
6	1D4	18	2Q1	6	1D3	20	2Q2
7	2D1	19	1Q4	7	1D4	21	2Q1
8	2D2	20	1Q3	8	nc	22	nc
9	2D3	21	1Q2	9	2D1	23	1Q4
10	2D4	22	1Q1	10	2D2	24	1Q3
11	$2\overline{OC}$	23	1CLK	11	2D3	25	1Q2
12	GND	24	V_{CC}	12	2D4	26	1Q1
				13	$2\overline{OC}$	27	1CLK
				14	GND	28	V_{CC}

†Pin numbers shown on logic symbols are for JT and NT packages only.
nc — no internal connection.

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876

DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH INVERTED OUTPUTS

- Three-state buffer-type outputs drive bus lines directly
- Each 4-bit word has own clock, preset, and output control inputs

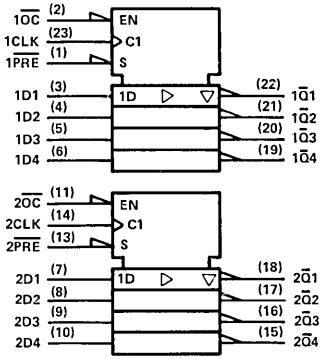
typical performance

TYPE	FREQ	POWER	DATA TIMES	
			SET-UP	HOLD
SN54ALS876	50 MHz	86.7 mW	10 ns†	4 ns†
SN74ALS876	50 MHz	86.7 mW	10 ns†	0 ns†

† Rising edge of clock pulse

SN54ALS876 (JT,FH)
SN54AS876 (JT,FH)
SN74ALS876 (NT,FN)
SN74AS876 (NT,FN)

logic symbol†



pin assignments

JT, NT PACKAGES			
1	1PRE	13	2PRE
2	1OC	14	2CLK
3	1D1	15	2Q4
4	1D2	16	2Q3
5	1D3	17	2Q2
6	1D4	18	2Q1
7	2D1	19	1Q4
8	2D2	20	1Q3
9	2D3	21	1Q2
10	2D4	22	1Q1
11	2OC	23	1CLK
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	1PRE	16	2PRE
3	1OC	17	2CLK
4	1D1	18	2Q4
5	1D2	19	2Q3
6	1D3	20	2Q2
7	1D4	21	2Q1
8	nc	22	nc
9	2D1	23	1Q4
10	2D2	24	1Q3
11	2D3	25	1Q2
12	2D4	26	1Q1
13	2OC	27	1CLK
14	GND	28	V_{CC}

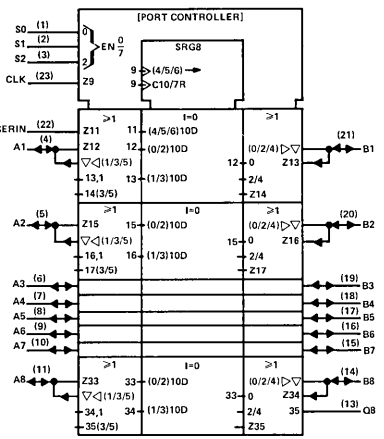
877

8-BIT UNIVERSAL TRANSCEIVER/PORT CONTROLLERS

- 8 selectable transceiver/port functions
- 3-state buffer-type outputs drive bus lines directly
- 24-pin 300-mil package

SN54AS877 (JT,FH)
SN74AS877 (NT,FN)

logic symbol†



pin assignments

JT, NT PACKAGES			
1	S0	13	Q8
2	S1	14	B8
3	S2	15	B7
4	A1	16	B6
5	A2	17	B5
6	A3	18	B4
7	A4	19	B3
8	A5	20	B2
9	A6	21	B1
10	A7	22	SERIN
11	A8	23	CLK
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	S0	16	Q8
3	S1	17	B8
4	S2	18	B7
5	A1	19	B6
6	A2	20	B5
7	A3	21	B4
8	nc	22	nc
9	A4	23	B3
10	A5	24	B2
11	A6	25	B1
12	A7	26	SERIN
13	A8	27	CLK
14	GND	28	V_{CC}

†Pin numbers shown on logic symbols are for JT and NT packages only.
nc — no internal connection.

878

DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

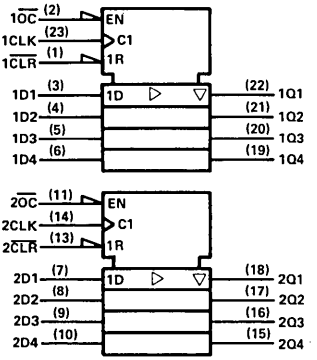
- Three-state buffer-type outputs
- Each 4-bit word has clock, clear, and output control inputs

typical performance

TYPE	FREQ	POWER	DATA TIMES	
			SET-UP	HOLD
SN54ALS878	50 MHz	86.7 mW	10 ns†	4 ns†
SN74ALS878	50 MHz	86.7 mW	10 ns†	0 ns†
SN54AS878				
SN74AS878				

†Rising edge of clock pulse
SN54ALS878 (JT,FH) SN74ALS878 (NT,FN)
SN54AS878 (JT,FH) SN74AS878 (NT,FN)

logic symbol, 'ALS878, 'AS878†



pin assignments

JT, NT PACKAGES			
1	1CLR	13	2CLR
2	1OC	14	2CLK
3	1D1	15	2Q4
4	1D2	16	2Q3
5	1D3	17	2Q2
6	1D4	18	2Q1
7	2D1	19	1Q4
8	2D2	20	1Q3
9	2D3	21	1Q2
10	2D4	22	1Q1
11	2OC	23	1CLK
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	1CLR	16	2CLR
3	1OC	17	2CLK
4	1D1	18	2Q4
5	1D2	19	2Q3
6	1D3	20	2Q2
7	1D4	21	2Q1
8	nc	22	nc
9	2D1	23	1Q4
10	2D2	24	1Q3
11	2D3	25	1Q2
12	2D4	26	1Q1
13	2OC	27	1CLK
14	GND	28	V_{CC}

879

DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH INVERTED OUTPUTS

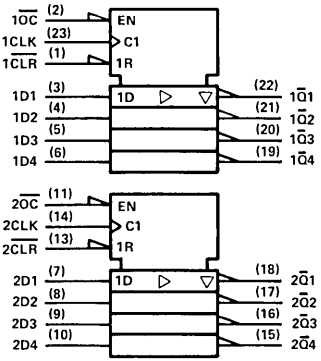
- Three state buffer-type outputs
- Each 4-bit word has clock, clear, and output control inputs.

typical performance

TYPE	FREQ	POWER	DATA TIMES	
			SET-UP	HOLD
SN54ALS879	50 MHz	86.7 mW	10 ns†	4 ns†
SN74ALS879	50 MHz	86.7 mW	10 ns†	0 ns†
SN54AS879				
SN74AS879				

†Rising edge of clock pulse
SN54ALS879 (JT,FH) SN74ALS879 (NT,FN)
SN54AS879 (JT,FH) SN74AS879 (NT,FN)

logic symbol, 'ALS879, 'AS879†



pin assignments

JT, NT PACKAGES			
1	1CLR	13	2CLR
2	1OC	14	2CLK
3	1D1	15	2Q4
4	1D2	16	2Q3
5	1D3	17	2Q2
6	1D4	18	2Q1
7	2D1	19	1Q4
8	2D2	20	1Q3
9	2D3	21	1Q2
10	2D4	22	1Q1
11	2OC	23	1CLK
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	1CLR	16	2CLR
3	1OC	17	2CLK
4	1D1	18	2Q4
5	1D2	19	2Q3
6	1D3	20	2Q2
7	1D4	21	2Q1
8	nc	22	nc
9	2D1	23	1Q4
10	2D2	24	1Q3
11	2D3	25	1Q2
12	2D4	26	1Q1
13	2OC	27	1CLK
14	GND	28	V_{CC}

†Pin numbers shown on logic symbols are for JT and NT packages only.
nc — no internal connection.

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880

DUAL 4-BIT D-TYPE LATCHES WITH INVERTED OUTPUTS

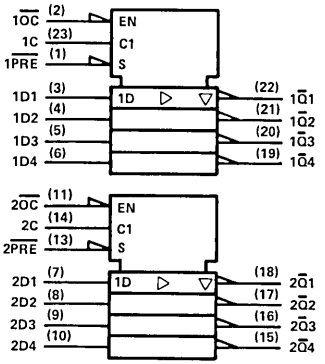
- Three-state buffer-type outputs drive bus lines directly
- Each 4-bit word has enable, preset, and output control inputs

typical performance

TYPE	OUTPUT	DELAY	POWER
'ALS880	$\overline{Q}$	11.5 ns	88 mW

SN54ALS880(JT,FH) SN74ALS880 (NT,FN)
SN54AS880 (JT,FH) SN74AS880 (NT,FN)

logic symbol†



pin assignments

JT, NT PACKAGES				FH, FN PACKAGES			
1	$1\overline{PRE}$	13	$2\overline{PRE}$	1	nc	15	nc
2	$1\overline{OC}$	14	2C	2	$1\overline{PRE}$	16	$2\overline{PRE}$
3	1D1	15	$2\overline{Q}4$	3	$1\overline{OC}$	17	2C
4	1D2	16	$2\overline{Q}3$	4	1D1	18	$2\overline{Q}4$
5	1D3	17	$2\overline{Q}2$	5	1D2	19	$2\overline{Q}3$
6	1D4	18	$2\overline{Q}1$	6	1D3	20	$2\overline{Q}2$
7	2D1	19	$1\overline{Q}4$	7	1D4	21	$2\overline{Q}1$
8	2D2	20	$1\overline{Q}3$	8	nc	22	nc
9	2D3	21	$1\overline{Q}2$	9	2D1	23	$1\overline{Q}4$
10	2D4	22	$1\overline{Q}1$	10	2D2	24	$1\overline{Q}3$
11	$2\overline{OC}$	23	1C	11	2D3	25	$1\overline{Q}2$
12	GND	24	V_{CC}	12	2D4	26	$1\overline{Q}1$
				13	$2\overline{OC}$	27	1C
				14	GND	28	V_{CC}

881

ARITHMETIC LOGIC UNITS/ FUNCTION GENERATORS

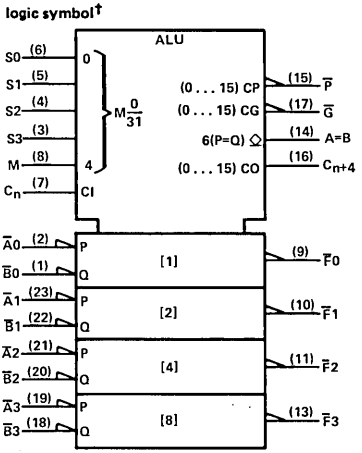
- 4-bit ALU's/Function Generators
- Same operating modes as 'AS181A, 'S181A expanded to include status register checks

typical performance

TYPE	CARRY TIME	16-BIT ADD TIME	TOTAL POWER
'AS881A	7.5 ns	20 ns	560 mW

SN54AS881A (JT,FH)
SN74AS881A (NT,FN)

logic symbol†



pin assignments

JT, NT PACKAGES			
1	$\overline{B}0$	13	$\overline{F}3$
2	$\overline{A}0$	14	A=B
3	S3	15	$\overline{P}$
4	S2	16	C_{n+4}
5	S1	17	$\overline{G}$
6	S0	18	$\overline{B}3$
7	C_n	19	$\overline{A}3$
8	M	20	$\overline{B}2$
9	$\overline{F}0$	21	$\overline{A}2$
10	$\overline{F}1$	22	$\overline{B}1$
11	$\overline{F}2$	23	$\overline{A}1$
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	$\overline{B}0$	16	$\overline{F}3$
3	$\overline{A}0$	17	A=B
4	S3	18	$\overline{P}$
5	S2	19	C_{n+4}
6	S1	20	$\overline{G}$
7	S0	21	$\overline{B}3$
8	nc	22	nc
9	C_n	23	$\overline{A}3$
10	M	24	$\overline{B}2$
11	$\overline{F}0$	25	$\overline{A}2$
12	$\overline{F}1$	26	$\overline{B}1$
13	$\overline{F}2$	27	$\overline{A}1$
14	GND	28	V_{CC}

†Pin numbers shown on logic symbols are for JT and NT packages only.
nc — no internal connection.

882

32-BIT LOOK-AHEAD CARRY GENERATORS

- Directly compatible with 'AS181, 'AS881, and 'S181 ALU's

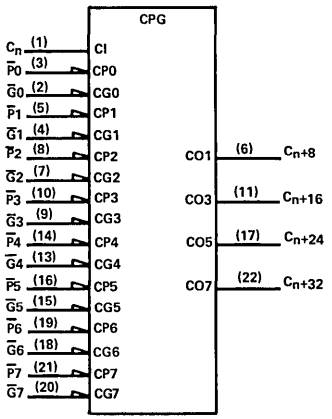
typical performance

TYPE	CARRY TIME	TOTAL POWER
'AS882	8 ns	325 mW

SN54AS882 (JT,FH)

SN74AS882 (NT,FN)

logic symbol†



pin assignments

JT, NT PACKAGES				FH, FN PACKAGES			
1	C_n	13	$\overline{G}4$	1	nc	15	nc
2	$\overline{G}0$	14	$\overline{P}4$	2	C_n	16	$\overline{G}4$
3	$\overline{P}0$	15	$\overline{G}5$	3	$\overline{G}0$	17	$\overline{P}4$
4	$\overline{G}1$	16	$\overline{P}5$	4	$\overline{P}0$	18	$\overline{G}5$
5	$\overline{P}1$	17	C_{n+24}	5	$\overline{G}1$	19	$\overline{P}5$
6	C_{n+8}	18	$\overline{G}6$	6	$\overline{P}1$	20	C_{n+24}
7	$\overline{G}2$	19	$\overline{P}6$	7	C_{n+8}	21	$\overline{G}6$
8	$\overline{P}2$	20	$\overline{G}7$	8	nc	22	nc
9	$\overline{G}3$	21	$\overline{P}7$	9	$\overline{G}2$	23	$\overline{P}6$
10	$\overline{P}3$	22	C_{n+32}	10	$\overline{P}2$	24	$\overline{G}7$
11	C_{n+16}	23	nc	11	$\overline{G}3$	25	$\overline{P}7$
12	GND	24	V_{CC}	12	$\overline{P}3$	26	C_{n+32}
				13	C_{n+16}	27	nc
				14	GND	28	V_{CC}

885

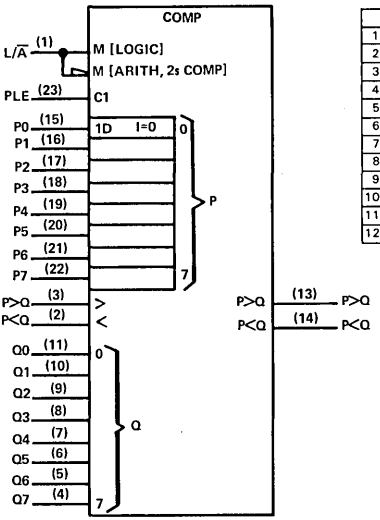
8-BIT MAGNITUDE COMPARATORS

- Choice of logical or arithmetic comparisons
- Latchable P input ports; power clear

SN54AS885 (JT,FH)

SN74AS885 (NT,FN)

logic symbol†



pin assignments

JT, NT PACKAGES				FH, FN PACKAGES			
1	$L/\overline{A}$	13	P>Qout	1	nc	15	nc
2	P<Qin	14	P<Qout	2	$L/\overline{A}$	16	P>Qout
3	P>Qin	15	P0	3	P<Qin	17	P<Qout
4	Q7	16	P1	4	P>Qin	18	P0
5	Q6	17	P2	5	Q7	19	P1
6	Q5	18	P3	6	Q6	20	P2
7	Q4	19	P4	7	Q5	21	P3
8	Q3	20	P5	8	nc	22	nc
9	Q2	21	P6	9	Q4	23	P4
10	Q1	22	P7	10	Q3	24	P5
11	Q0	23	PLE	11	Q2	25	P6
12	GND	24	V_{CC}	12	Q1	26	P7
				13	Q0	27	PLE
				14	GND	28	V_{CC}

†Pin numbers shown on logic symbols are for JT and NT packages only.

nc — no internal connection.

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1000

QUAD 2-INPUT NAND GATES

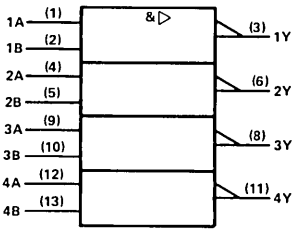
- Increased output drive capability over 'LS00

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	DELAY	POWER/GATE
SN54ALS1000	12 mA	−1 mA	4 ns	3 mW
SN74ALS1000	24 mA	−2.6 mA	4 ns	3 mW

SN54ALS1000 (J,FH) SN74ALS1000 (N,FN)

logic symbol†



positive logic: $Y = \overline{AB}$

pin assignments

J, N PACKAGES			
1	1A	8	3Y
2	1B	9	3A
3	1Y	10	3B
4	2A	11	4Y
5	2B	12	4A
6	2Y	13	4B
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	3Y
3	1B	13	3A
4	1Y	14	3B
5	nc	15	nc
6	2A	16	4Y
7	nc	17	nc
8	2B	18	4A
9	2Y	19	4B
10	GND	20	V_{CC}

1002

QUAD 2-INPUT NOR BUFFER GATES

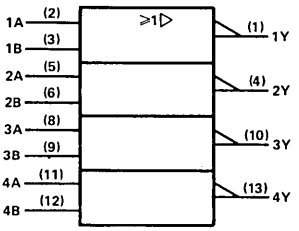
- Increased output drive capability over 'LS02

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	DELAY	POWER/GATE
SN54ALS1002	12 mA	−1 mA	4 ns	4 mW
SN74ALS1002	24 mA	−2.6 mA	4 ns	4 mW

SN54ALS1002 (J,FH) SN74ALS1002 (N,FN)

logic symbol†



positive logic: $Y = \overline{A+B}$

pin assignments

J, N PACKAGES			
1	1Y	8	3A
2	1A	9	3B
3	1B	10	3Y
4	2Y	11	4A
5	2A	12	4B
6	2B	13	4Y
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1Y	12	3A
3	1A	13	3B
4	1B	14	3Y
5	nc	15	nc
6	2Y	16	4A
7	nc	17	nc
8	2A	18	4B
9	2B	19	4Y
10	GND	20	V_{CC}

6

† Pin numbers shown on logic symbols are for J and N packages only.
nc – no internal connection.

1003

QUAD 2-INPUT NAND BUFFER GATES WITH OPEN-COLLECTOR OUTPUTS

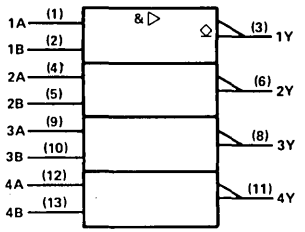
- Increased drive capability over 'LS03

typical performance

TYPE	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	DELAY	POWER/GATE
SN54ALS1003	5.5 V	12 mA	14.5 ns	3 mW
SN74ALS1003	5.5 V	24 mA	14.5 ns	3 mW

SN54ALS1003 (J,FH) SN74ALS1003 (N,FN)

logic symbol†



positive logic: $Y = \overline{AB}$

pin assignments

J, N PACKAGES			
1	1A	8	3Y
2	1B	9	3A
3	1Y	10	3B
4	2A	11	4Y
5	2B	12	4A
6	2Y	13	4B
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	3Y
3	1B	13	3A
4	1Y	14	3B
5	nc	15	nc
6	2A	16	4Y
7	nc	17	nc
8	2B	18	4A
9	2Y	19	4B
10	GND	20	V_{CC}

1004

HEX INVERTER BUFFER GATES

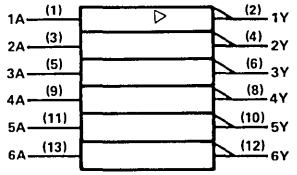
- Increased drive capability over LS04

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT
SN54ALS1004	12 mA	−1 mA
SN74ALS1004	24 mA	−2.6 mA

SN54ALS1004 (J,FH) SN74ALS1004 (N,FN)

logic symbol†



positive logic: $Y = \overline{A}$

pin assignments

J, N PACKAGES			
1	1A	8	4Y
2	1Y	9	4A
3	2A	10	5Y
4	2Y	11	5A
5	3A	12	6Y
6	3Y	13	6A
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	4Y
3	1Y	13	4A
4	2A	14	5Y
5	nc	15	nc
6	2Y	16	5A
7	nc	17	nc
8	3A	18	6Y
9	3Y	19	6A
10	GND	20	V_{CC}

1005

HEX INVERTER BUFFER GATES WITH OPEN-COLLECTOR OUTPUTS

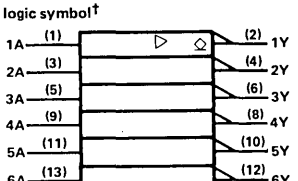
- Increased drive capability over LS05

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT
SN54ALS1005	12 mA	−1 mA
SN74ALS1005	24 mA	−2.6 mA

SN54ALS1005 (J,FH) SN74ALS1005 (N,FN)

logic symbol†



positive logic: $Y = \overline{A}$

pin assignments

J, N PACKAGES			
1	1A	8	4Y
2	1Y	9	4A
3	2A	10	5Y
4	2Y	11	5A
5	3A	12	6Y
6	3Y	13	6A
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	4Y
3	1Y	13	4A
4	2A	14	5Y
5	nc	15	nc
6	2Y	16	5A
7	nc	17	nc
8	3A	18	6Y
9	3Y	19	6A
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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1008

QUADRUPLE 2-INPUT POSITIVE-AND BUFFER GATES

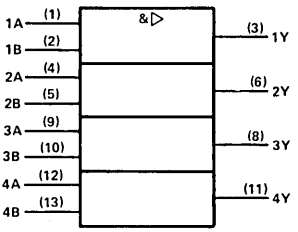
- Increased drive capability over LS08

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT
SN54ALS1008	12 mA	−1 MA
SN74ALS1008	24 mA	−2.6 mA
SN54AS1008		
SN74AS1008		

SN54ALS1008 (J,FH) SN74ALS1008 (N,FN)
SN54AS1008 (J,FH) SN74AS1008 (N,FN)

logic symbol†



positive logic: Y = AB

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3Y	1	nc	11	nc
2	1B	9	3A	2	1A	12	3Y
3	1Y	10	3B	3	1B	13	3A
4	2A	11	4Y	4	1Y	14	3B
5	2B	12	4A	5	nc	15	nc
6	2Y	13	4B	6	2A	16	4Y
7	GND	14	V_{CC}	7	nc	17	nc
				8	2B	18	4A
				9	2Y	19	4B
				10	GND	20	V_{CC}

1010

TRIPLE 3-INPUT POSITIVE-NAND BUFFER GATES

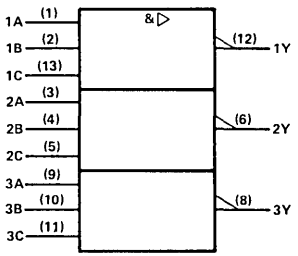
- Increased drive capability over LS10

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT
SN54ALS1010	12 mA	−1 mA
SN74ALS1010	24 mA	−2.6 mA

SN54ALS1010 (J,FH) SN74ALS1010 (N,FN)

logic symbol†



positive logic: $Y = \overline{ABC}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3Y	1	nc	11	nc
2	1B	9	3A	2	1A	12	3Y
3	2A	10	3B	3	1B	13	3A
4	2B	11	3C	4	2A	14	3B
5	2C	12	1Y	5	nc	15	nc
6	2Y	13	1C	6	2B	16	3C
7	GND	14	V_{CC}	7	nc	17	nc
				8	2C	18	1Y
				9	2Y	19	1C
				10	GND	20	V_{CC}

1011

TRIPLE 3-INPUT POSITIVE-AND BUFFER GATES

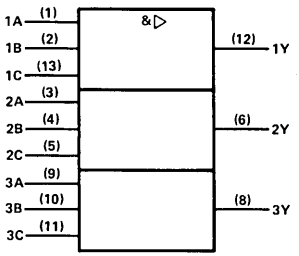
- Increased drive capability over LS11

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT
SN54ALS1011	12 mA	−1 mA
SN74ALS1011	24 mA	−2.6 mA

SN54ALS1011 (J,FH) SN74ALS1011 (N,FN)

logic symbol†



positive logic: Y = ABC

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3Y	1	nc	11	nc
2	1B	9	3A	2	1A	12	3Y
3	2A	10	3B	3	1B	13	3A
4	2B	11	3C	4	2A	14	3B
5	2C	12	1Y	5	nc	15	nc
6	2Y	13	1C	6	2B	16	3C
7	GND	14	V_{CC}	7	nc	17	nc
				8	2C	18	1Y
				9	2Y	19	1C
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

1020

DUAL 4-INPUT NAND BUFFER GATES

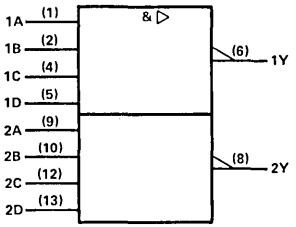
- Increased drive capability over LS20

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT
SN54ALS1020	12 mA	−1 mA
SN74ALS1020	24 mA	−2.6 mA

SN54ALS1020 (J,FH) SN74ALS1020 (N,FN)

logic symbol†



positive logic: $Y = \overline{ABCD}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	2Y	1	nc	11	nc
2	1B	9	2A	2	1A	12	2Y
3	nc	10	2B	3	1B	13	2A
4	1C	11	nc	4	nc	14	2B
5	1D	12	2C	5	nc	15	nc
6	1Y	13	2D	6	1C	16	nc
7	GND	14	V_{CC}	7	nc	17	nc
				8	1D	18	2C
				9	1Y	19	2D
				10	GND	20	V_{CC}

6

1032

QUADRUPLE 2-INPUT POSITIVE-OR BUFFER GATE

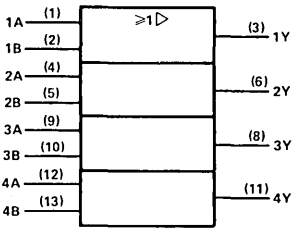
- Increased drive capability over LS32

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT
SN54ALS1032	12 mA	−1 mA
SN74ALS1032	24 mA	−2.6 mA
SN54AS1032		
SN74AS1032		

SN54ALS1032(J,FH) SN74ALS1032 (N,FN)
SN54AS1032 (J,FH) SN74AS1032 (N,FN)

logic symbol†



positive logic: Y = A+B

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3Y	1	nc	11	nc
2	1B	9	3A	2	1A	12	3Y
3	1Y	10	3B	3	1B	13	3A
4	2A	11	4Y	4	1Y	14	3B
5	2B	12	4A	5	nc	15	nc
6	2Y	13	4B	6	2A	16	4Y
7	GND	14	V_{CC}	7	nc	17	nc
				8	2B	18	4A
				9	2Y	19	4B
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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1034

HEX BUFFERS

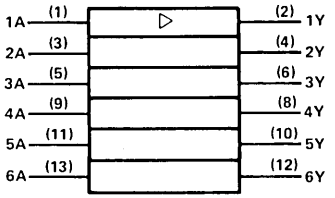
- Non-inverting outputs

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT
SN54ALS1034	12 mA	−1 mA
SN74ALS1034	24 mA	−2.6 mA
SN54AS1034		
SN74AS1034		

SN54ALS1034 (J,FH) SN74ALS1034 (N,FN)
SN54AS1034 (J,FH) SN74AS1034 (N,FN)

logic symbol†



positive logic Y = A

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	4Y	1	nc	11	nc
2	1Y	9	4A	2	1A	12	4Y
3	2A	10	5Y	3	1Y	13	4A
4	2Y	11	5A	4	2A	14	5Y
5	3A	12	6Y	5	nc	15	nc
6	3Y	13	6A	6	2Y	16	5A
7	GND	14	V_{CC}	7	nc	17	nc
				8	3A	18	6Y
				9	3Y	19	6A
				10	GND	20	V_{CC}

1035

HEX BUFFERS WITH OPEN-COLLECTOR OUTPUTS

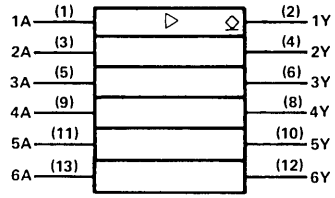
- Non-inverting outputs

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT VOLTAGE
SN54ALS1035	12 mA	5.5 V
SN74ALS1035	24 mA	5.5 V

SN54ALS1035 (J,FH) SN74ALS1035 (N,FN)

logic symbol†



Positive logic Y = A

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	4Y	1	nc	11	nc
2	1Y	9	4A	2	1A	12	4Y
3	2A	10	5Y	3	1Y	13	4A
4	2Y	11	5A	4	2A	14	5Y
5	3A	12	6Y	5	nc	15	nc
6	3Y	13	6A	6	2Y	16	5A
7	GND	14	V_{CC}	7	nc	17	nc
				8	3A	18	6Y
				9	3Y	19	6A
				10	GND	20	V_{CC}

6

†Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

1240

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS
(inverted three-state outputs)

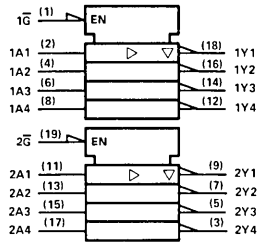
- Low power version of 'ALS240, AS240

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSIPATION
SN54ALS1240	9	−12 mA	8 mA	47.5 mW
SN74ALS1240	9	−15 mA	16 mA	
SN74ALS1240-1	9	−15 mA	24 mA	

SN54ALS1240 (J,FH) SN74ALS1240 (N, FN)
SN74ALS1240-1 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1G̅	11	2A1	1	1G̅	11	2A1
2	1A1	12	1Y4	2	1A1	12	1Y4
3	2Y4	13	2A2	3	2Y4	13	2A2
4	1A2	14	1Y3	4	1A2	14	1Y3
5	2Y3	15	2A3	5	2Y3	15	2A3
6	1A3	16	1Y2	6	1A3	16	1Y2
7	2Y2	17	2A4	7	2Y2	17	2A4
8	1A4	18	1Y1	8	1A4	18	1Y1
9	2Y1	19	2G̅	9	2Y1	19	2G̅
10	GND	20	V_{CC}	10	GND	20	V_{CC}

1241

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS
(non-inverted three-state outputs)

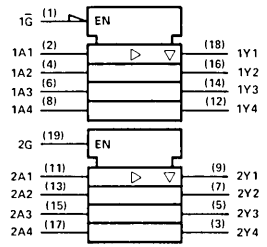
- Low power version of 'ASL241, LS241

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSIPATION
SN54ALS1241	9	−12 mA	8 mA	47.5 mW
SN74ALS1241	9	−15 mA	16 mA	
SN74ALS1241-1	9	−15 mA	24 mA	

SN54ALS1241 (J,FH) SN74ALS1241 (N,FN)
SN74ALS1241-1 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1G̅	11	2A1	1	1G̅	11	2A1
2	1A1	12	1Y4	2	1A1	12	1Y4
3	2Y4	13	2A2	3	2Y4	13	2A2
4	1A2	14	1Y3	4	1A2	14	1Y3
5	2Y3	15	2A3	5	2Y3	15	2A3
6	1A3	16	1Y2	6	1A3	16	1Y2
7	2Y2	17	2A4	7	2Y2	17	2A4
8	1A4	18	1Y1	8	1A4	18	1Y1
9	2Y1	19	2G	9	2Y1	19	2G
10	GND	20	V_{CC}	10	GND	20	V_{CC}

1242

QUADRUPLE BUS TRANSCEIVERS
(inverted three-state outputs)

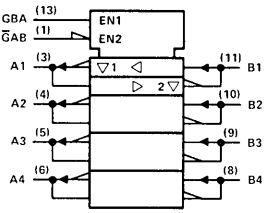
- Low power version of ALS242, LS242

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSIPATION
SN54ALS1242		−12 mA	8 mA	
SN74ALS1242		−15 mA	16 mA	
SN74ALS1242-1		−15 mA	24 mA	

SN54ALS1242 (J,FH) SN74ALS1242 (N, FN)
SN74ALS1242-1 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	G̅AB	8	B4	1	nc	11	nc
2	nc	9	B3	2	G̅AB	12	B4
3	A1	10	B2	3	nc	13	B3
4	A2	11	B1	4	A1	14	B2
5	A3	12	nc	5	nc	15	nc
6	A4	13	GBA	6	A2	16	B1
7	GND	14	V_{CC}	7	nc	17	nc
				8	A3	18	nc
				9	A4	19	GBA
				10	GND	20	V_{CC}

†Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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1243

QUADRUPLE BUS TRANSCEIVERS
(non-inverted three-state outputs)

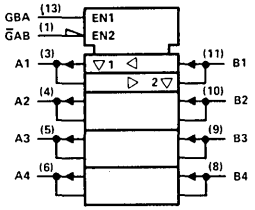
- Low power version of ALS243, LS243

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSIPATION
SN54ALS1243		−12 mA	8 mA	
SN74ALS1243		−15 mA	16 mA	
SN74ALS1243-1		−15 mA	24 mA	

SN54ALS1243 (J,FH) SN74ALS1243 (N,FN)
SN74ALS1243-1 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	GAB	8	B4	1	nc	11	nc
2	nc	9	B3	2	GAB	12	B4
3	A1	10	B2	3	nc	13	B3
4	A2	11	B1	4	A1	14	B2
5	A3	12	nc	5	nc	15	nc
6	A4	13	GBA	6	A2	16	B1
7	GND	14	V_{CC}	7	nc	17	nc
				8	A3	18	nc
				9	A4	19	GBA
				10	GND	20	V_{CC}

1244

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS
(non-inverted three-state outputs)

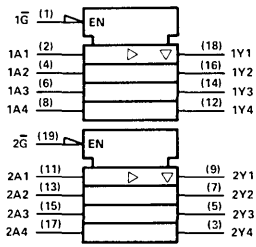
- Low power version of ALS244, LS244

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSIPATION
SN54ALS1244	9 ns	−12 mA	8 mA	
SN74ALs1244	9 ns	−15 mA	16 mA	45 mW
SN74ALS1244-1	9 ns	−15 mA	24 mA	

SN54ALS1244 (J,FH) SN74ALS1244 (N,FN)
SN74ALS1244-1 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$1\overline{G}$	11	2A1	1	$1\overline{G}$	11	2A1
2	1A1	12	1Y4	2	1A1	12	1Y4
3	2Y4	13	2A2	3	2Y4	13	2A2
4	1A2	14	1Y3	4	1A2	14	1Y3
5	2Y3	15	2A3	5	2Y3	15	2A3
6	1A3	16	1Y2	6	1A3	16	1Y2
7	2Y2	17	2A4	7	2Y2	17	2A4
8	1A4	18	1Y1	8	1A4	18	1Y1
9	2Y1	19	$2\overline{G}$	9	2Y1	19	$2\overline{G}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

1245

OCTAL BUS TRANSCEIVERS
(non-inverted three-state outputs)

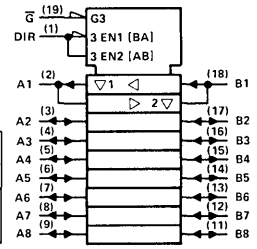
- Low power version of ALS245, LS245

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSIPATION
SN54ALS1245	8	−12 mA	8 mA	
SN74ALS1245	8	−15 mA	16 mA	113 mW
SN74ALS1245-1	8	−15 mA	24 mA	

SN54ALS1245 (J,FH) SN74ALS1245 (N,FN)
SN74ALS1245-1 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	DIR	11	B8	1	DIR	11	B8
2	A1	12	B7	2	A1	12	B7
3	A2	13	B6	3	A2	13	B6
4	A3	14	B5	4	A3	14	B5
5	A4	15	B4	5	A4	15	B4
6	A5	16	B3	6	A5	16	B3
7	A6	17	B2	7	A6	17	B2
8	A7	18	B1	8	A7	18	B1
9	A8	19	$\overline{G}$	9	A8	19	$\overline{G}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

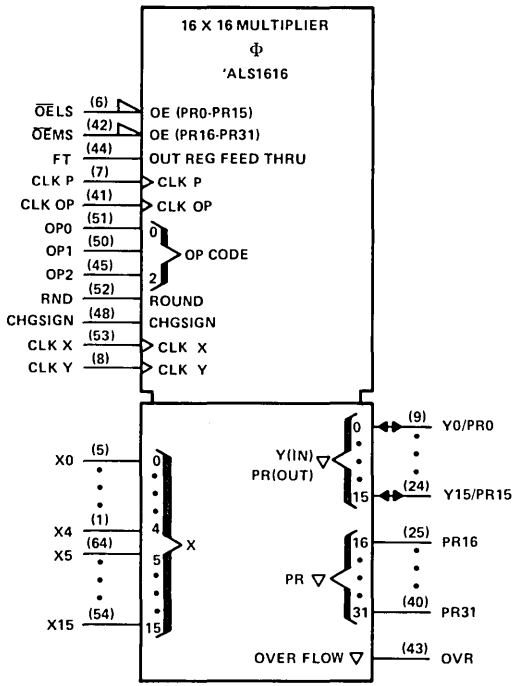
†Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

1616

16-×-16-BIT MULTIMODE MULTIPLIERS

- Multiplies Any Combination of Unsigned, Signed, Integer, or Fractional Inputs
- Registered Inputs and Outputs
- Comparable to TRW's MPY-16HJ
- Choice of Single-Signed, Double-Signed, Unsigned, or Signed Fractionally Adjusted Output
- Overflow Detected if a Combination of Input Data and/or Output Formats Result in a Number that Cannot be Represented
- Rounding is Provided for Both Integer and Fractional Results
- Flexible Input-Output Format Aids in Expansion to Multiple Precision Results
- 55 ns Typical Unclocked Multiply Time
- Power Dissipation Approximately 1.5 W
- 3-State Outputs
- Ideal for Signal Processing, Including Digital Filters, FFTs, and Automatic Line Integration
- Output may be Complemented
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

logic symbol



pin assignments

JD PACKAGE			
1	X4	33	PR24
2	X3	34	PR25
3	X2	35	PR26
4	X1	36	PR27
5	X0	27	PR28
6	OELS	38	PR29
7	CLKP	39	PR30
8	CLKY	40	PR31
9	Y0/PR0	41	CLKOP
10	Y1/PR1	42	OEMS
11	Y2/PR2	43	OVR
12	Y3/PR3	44	FT
13	Y4/PR4	45	OP2
14	Y5/PR5	46	GND
15	Y6/PR6	47	GND
16	Y7/PR7	48	CHGSIGN
17	Y8/PR8	49	V_{CC}
18	Y9/PR9	50	OP1
19	Y10/PR10	51	OP0
20	Y11/PR11	52	RND
21	Y12/PR12	53	CLKX
22	Y13/PR13	54	X15
23	Y14/PR14	55	X14
24	Y15/PR15	56	X13
25	PR16	57	X12
26	PR17	58	X11
27	PR18	59	X10
28	PR19	60	X9
29	PR20	61	X8
20	PR21	62	X7
31	PR22	63	X6
32	PR23	64	X5

For chip carrier information, contact the factory.

SN54ALS1616 (JD) SN74ALS1616 (JD)

TEXAS INSTRUMENTS
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1620, 1621, 1622, 1623

OCTAL BUS TRANSCEIVERS

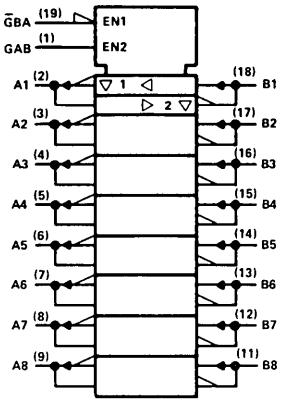
- Bidirectional bus transceivers
- Low power version of ALS 620, 621, 622, 623

typical performance

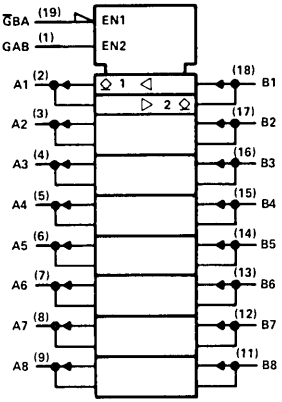
TYPE	OUTPUT	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54ALS1620	3-State	−12	8 mA
SN74ALS1620	3-State	−15	16 mA
SN74ALS1620-1	3-State	−15	24 mA
SN54ALS1621	O-C	N/A	8 mA
SN74ALS1621	O-C	N/A	16 mA
SN74ALS1621-1	O-C	N/A	24 mA
SN54ALS1622	O-C	N/A	8 mA
SN74ALS1622	O-C	N/A	16 mA
SN74ALS1622-1	O-C	N/A	24 mA
SN54ALS1623	3-State	−12	8 mA
SN74ALS1623	3-State	−15	16 mA
SN74ALS1623-1	3-State	−15	24 mA

SN54ALS1620 (J,FH) SN74ALS1620 (N,FN)
SN74ALS1620-1 (N,FN)
SN54ALS1621 (J,FH) SN74ALS1621 (N,FN)
SN74ALS1621-1 (N,FN)
SN54ALS1622 (J,FH) SN74ALS1622 (N,FN)
SN74ALS1622-1 (N,FN)
SN54ALS1623 (J,FH) SN74ALS1623 (N,FN)
SN74ALS1623-1 (N,FN)

logic symbol, 'ALS1620, 'LS1620†



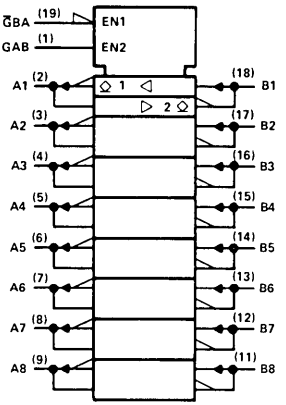
logic symbol, 'ALS1621, 'LS1621†



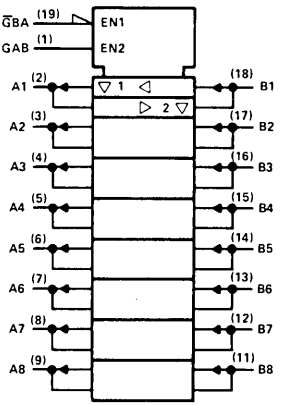
pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	GAB	11	B8	1	GAB	11	B8
2	A1	12	B7	2	A1	12	B7
3	A2	13	B6	3	A2	13	B6
4	A3	14	B5	4	A3	14	B5
5	A4	15	B4	5	A4	15	B4
6	A5	16	B3	6	A5	16	B3
7	A6	17	B2	7	A6	17	B2
8	A7	18	B1	8	A7	18	B1
9	A8	19	G̅BA	9	A8	19	G̅BA
10	GND	20	V_{CC}	10	GND	20	V_{CC}

logic symbol, 'ALS1622, 'LS1622†



logic symbol, 'ALS1623, 'LS1623†



†Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

1638, 1639

OCTAL BUS TRANSCEIVERS

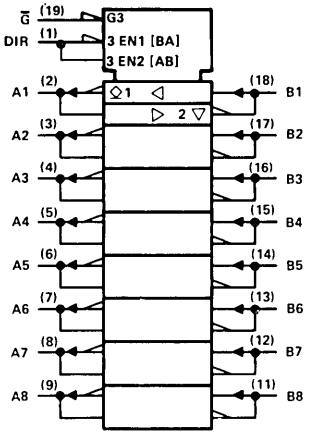
- Bidirectional bus transceivers
- "A" bus outputs are open-collector: "B" bus outputs are three-state
- 'ALS1638—inverting logic
- 'ALS1639—true logic
- Low power versions of 'ALS638, 'ALS639

typical performance

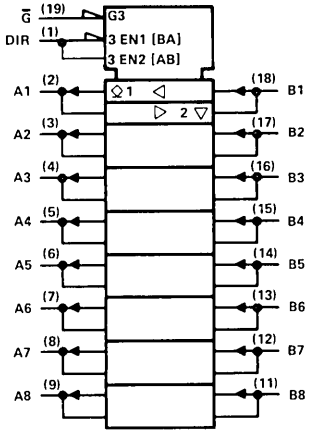
TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54ALS1638	7 ns	−12 mA	8 mA
SN74ALS1638	7 ns	−15 mA	16 mA
SN74ALS1638-1	7 ns	−15 mA	24 mA
SN54ALS1639	8 ns	−12 mA	8 mA
SN74ALS1639	8 ns	−15 mA	16 mA
SN74ALS1639-1	8 ns	−15 mA	24 mA

SN54ALS1638 (J,FH) SN74ALS1638 (N,FN)
SN54ALS1639 (J,FH) SN74ALS1639 (N,FN)
SN74ALS1638-1 (N,FN)
SN74ALS1639-1 (N,FN)

logic symbol, 'ALS1638†



logic symbol, 'ALS1639†



pin assignments

J, N PACKAGES			
1	DIR	11	B8
2	A1	12	B7
3	A2	13	B6
4	A3	14	B5
5	A4	15	B4
6	A5	16	B3
7	A6	17	B2
8	A7	18	B1
9	A8	19	$\overline{G}$
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	DIR	11	B8
2	A1	12	B7
3	A2	13	B6
4	A3	14	B5
5	A4	15	B4
6	A5	16	B3
7	A6	17	B2
8	A7	18	B1
9	A8	19	$\overline{G}$
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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1640, 1641, 1642
1643, 1644, 1645

OCTAL BUS TRANSCEIVERS

- Low power versions of 'ALS640, 'ALS641, 'ALS642 'ALS643, 'ALS644, 'ALS645

typical performance

TYPE	OUTPUT	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54ALS1640	3-State	7 ns	−12 mA	8 mA
SN74ALS1640	3-State	7 ns	−15 mA	16 mA
SN74ALS1640-1	3-State	7 ns	−15 mA	24 mA
SN54ALS1641	O-C		N/A	8 mA
SN74ALS1641	O-C		N/A	16 mA
SN74ALS1641-1	O-C		N/A	24 mA
SN54ALS1642	O-C		N/A	8 mA
SN74ALS1642	O-C		N/A	16 mA
SN74ALS1642-1	O-C		N/A	24 mA
SN54ALS1643	3-State		−12 mA	8 mA
SN74ALS1643	3-State		−15 mA	16 mA
SN74ALS1643-1	3-State		−15 mA	24 mA
SN54ALS1644	O-C		N/A	8 mA
SN74ALS1644	O-C		N/A	16 mA
SN74ALS1644-1	O-C		N/A	24 mA
SN54ALS1645	3-State	10 ns	−12 mA	8 mA
SN74ALS1645	3-State	10 ns	−15 mA	16 mA
SN74ALS1645-1	3-State	10 ns	−15 mA	24 mA

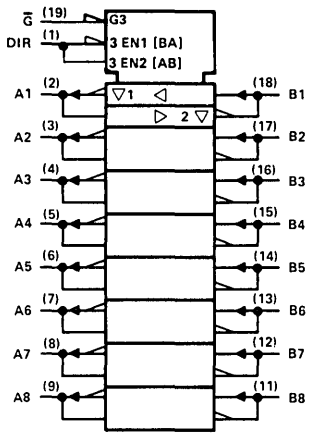
SN54ALS1640 (J,FH)
SN54ALS1641 (J,FH)
SN54ALS1642 (J,FH)
SN54ALS1643 (J,FH)
SN54ALS1644 (J,FH)
SN54ALS1645 (J,FH)

SN74ALS1640 (N,FN)
SN74ALS1641 (N,FN)
SN74ALS1642 (N,FN)
SN74ALS1643 (N,FN)
SN74ALS1644 (N,FN)
SN74ALS1645 (N,FN)
SN74ALS1640-1 (N,FN)
SN74ALS1641-1 (N,FN)
SN74ALS1642-1 (N,FN)
SN74ALS1643-1 (N,FN)
SN74ALS1644-1 (N,FN)
SN74ALS1645-1 (N,FN)

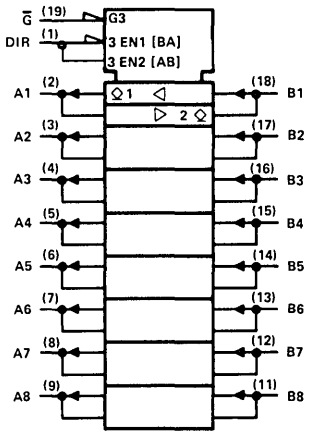
pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	DIR	11	B8	1	DIR	11	B8
2	A1	12	B7	2	A1	12	B7
3	A2	13	B6	3	A2	13	B6
4	A3	14	B5	4	A3	14	B5
5	A4	15	B4	5	A4	15	B4
6	A5	16	B3	6	A5	16	B3
7	A6	17	B2	7	A6	17	B2
8	A7	18	B1	8	A7	18	B1
9	A8	19	$\overline{G}$	9	A8	19	$\overline{G}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

logic symbol, 'ALS1640†



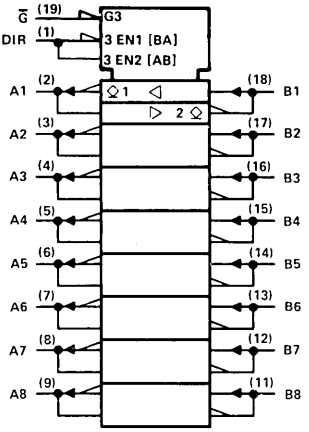
logic symbol, 'ALS1641†



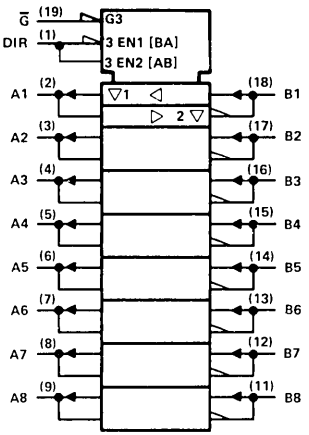
†Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

1640, 1641, 1642
1643, 1644, 1645 continued

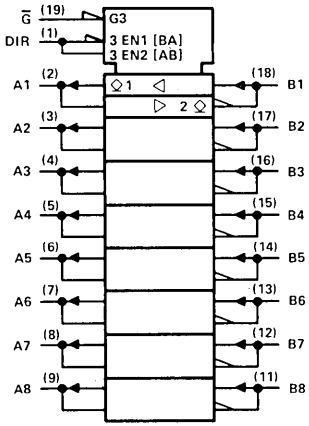
logic symbol, 'ALS1642†



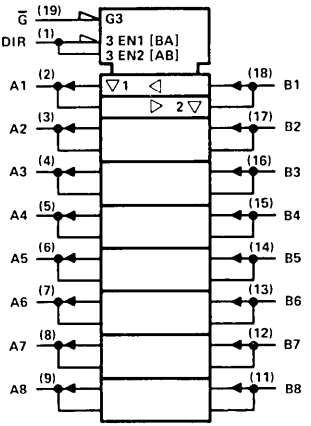
logic symbol, 'ALS1643†



logic symbol, 'ALS1644†



logic symbol, 'ALS1645†



†Pin numbers shown on logic symbols are for J and N packages only.

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'PL16L8

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

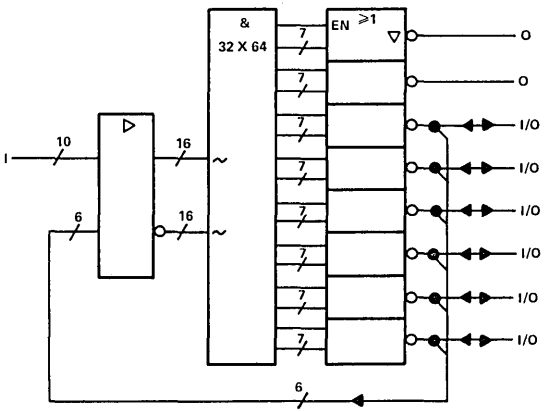
- Octal 16-input AND-OR-INVERT gate array

pin assignments

J, N PACKAGES			
1	I	11	I
2	I	12	O
3	I	13	I/O
4	I	14	I/O
5	I	15	I/O
6	I	16	I/O
7	I	17	I/O
8	I	18	I/O
9	I	19	O
10	GND	20	V_{CC}

SN54PL16L8 (J) SN74PL16L8 (J,N)

functional block diagram



~denotes fused inputs

'PL16R4

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

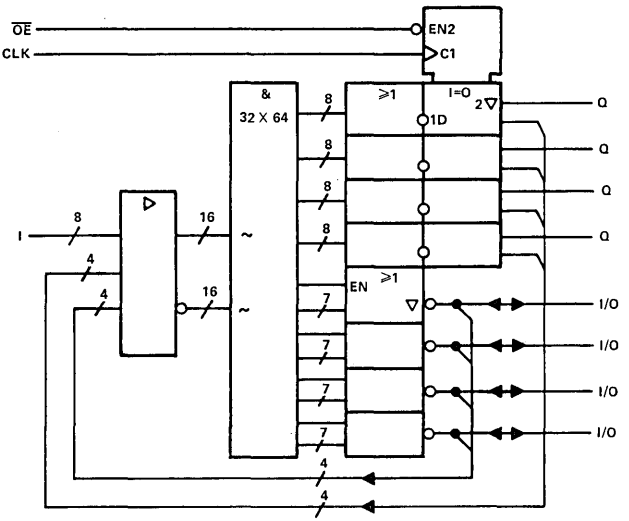
- Quad 16-input registered AND-OR gate array

pin assignments

J, N PACKAGES			
1	CLK	11	$\overline{OE}$
2	I	12	I/O
3	I	13	I/O
4	I	14	Q
5	I	15	Q
6	I	16	Q
7	I	17	Q
8	I	18	I/O
9	I	19	I/O
10	GND	20	V_{CC}

SN54ALS16R4 (J) SN74ALS16R4 (J,N)

functional block diagram



~denotes fused inputs

6

'PL16R6

FIELD-PROGRAMMABLE
LOGIC, FIXED-OR ARRAYS

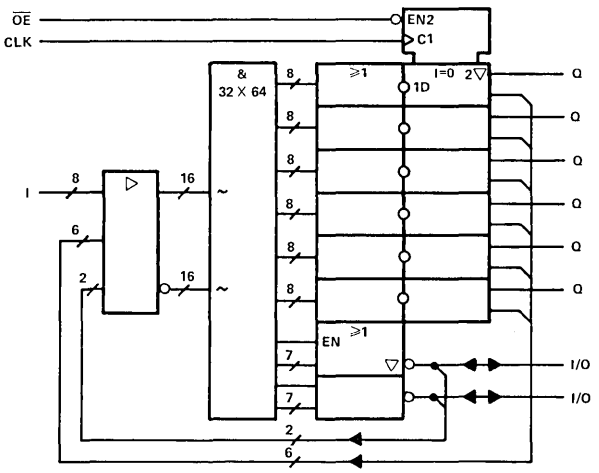
- Hex 16-input registered AND-OR gate array

pin assignments

J, N PACKAGES			
1	CLK	11	$\overline{OE}$
2	I	12	I/O
3	I	13	Q
4	I	14	Q
5	I	15	Q
6	I	16	Q
7	I	17	Q
8	I	18	Q
9	I	19	I/O
10	GND	20	V_{CC}

SN54PL16R6 (J) SN74PL16R6 (J,N)

functional block diagram



~denotes fused inputs

'PL16R8

FIELD-PROGRAMMABLE
LOGIC, FIXED-OR ARRAYS

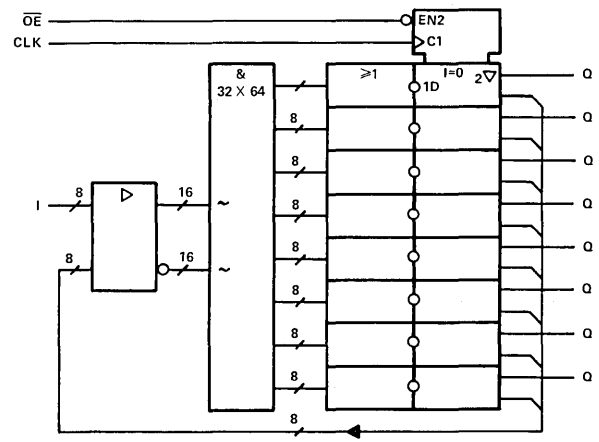
- Octal 16-input registered AND-OR gate array

pin assignments

J, N PACKAGES			
1	CLK	11	$\overline{OE}$
2	I	12	Q
3	I	13	Q
4	I	14	Q
5	I	15	Q
6	I	16	Q
7	I	17	Q
8	I	18	Q
9	I	19	Q
10	GND	20	V_{CC}

SN54PL16R8 (J) SN74PL16R8 (J,N)

functional block diagram



~denotes fused inputs

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'PL20L8

FIELD-PROGRAMMABLE
LOGIC, FIXED-OR ARRAYS

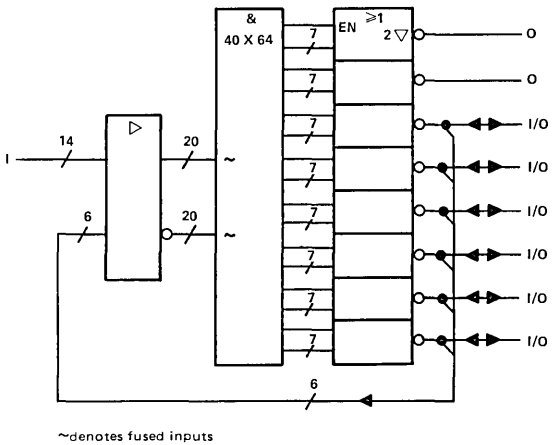
- Octal 20-input AND-OR-INVERT gate array

pin assignments

JT, NT PACKAGES			
1	I	13	I
2	I	14	I/PRELOAD
3	I	15	O
4	I	16	I/O
5	I	17	I/O
6	I	18	I/O
7	I	19	I/O
8	I	20	I/O
9	I	21	I/O
10	I	22	O
11	I	23	I
12	GND	24	V_{CC}

SN54PL20L8 (JT) SN74PL20LB (JT,NT)

functional block diagram



'PL20R4

FIELD-PROGRAMMABLE
LOGIC, FIXED-OR ARRAYS

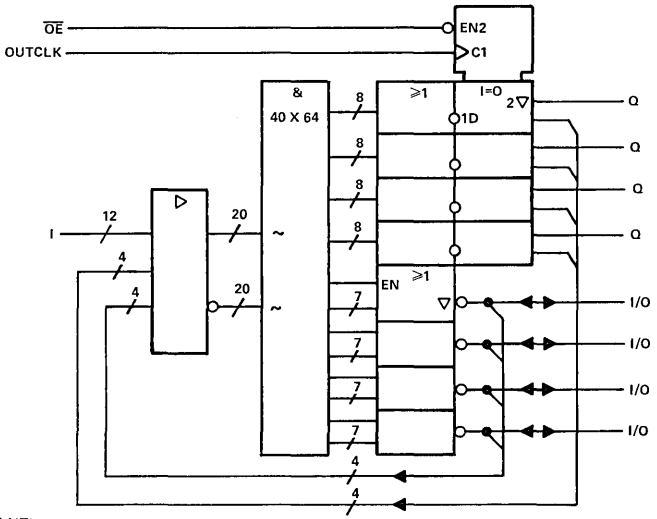
- Quad 20-input registered AND-OR gate array

pin assignments

JT, NT PACKAGES			
1	OUTCLK	13	$\overline{OE}$
2	I	14	I/PRELOAD
3	I	15	I/O
4	I	16	I/O
5	I	17	Q
6	I	18	Q
7	I	19	Q
8	I	20	Q
9	I	21	I/O
10	I	22	I/O
11	I	23	I
12	GND	24	V_{CC}

SN54PL20R4 (JT) SN74PL20R4 (JT,NT)

functional block diagram



'PL20R6

FIELD-PROGRAMMABLE
LOGIC, FIXED-OR ARRAYS

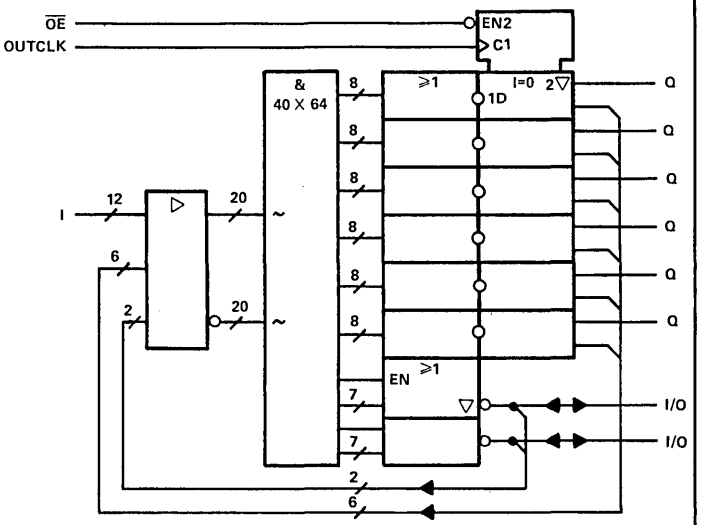
- Hex 20-input registered AND-OR gate array.

pin assignments

JT, NT PACKAGES			
1	OUT CLK	24	V_{CC}
2	I	23	I
3	I	22	I/O
4	I	21	Q
5	I	20	Q
6	I	19	Q
7	I	18	Q
8	I	17	Q
9	I	16	Q
10	I	15	I/O
11	I	14	I/PRELOAD
12	GND	13	$\overline{OE}$

SN54PL20R6 (JT) SN74PL20R6 (JT, NT)

functional block diagram



~ denotes fused inputs.

'PL20R8

FIELD-PROGRAMMABLE
LOGIC, FIXED-OR ARRAYS

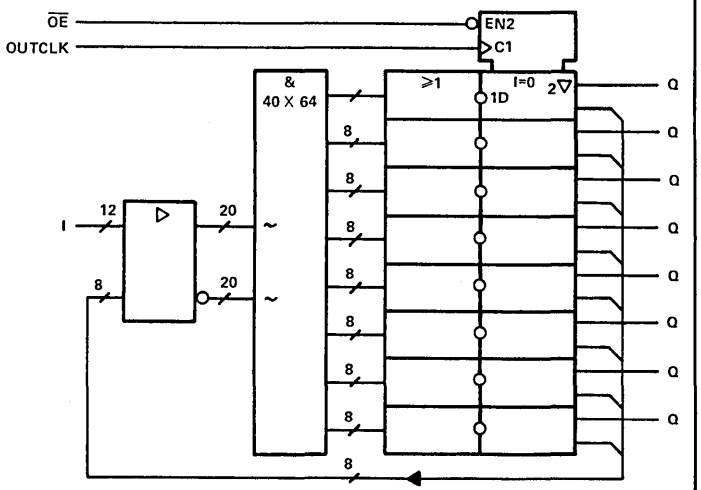
- Octal 20-input registered AND-OR gate array.

pin assignments

JT, NT PACKAGES			
1	OUT CLK	24	V_{CC}
2	I	23	I
3	I	22	Q
4	I	21	Q
5	I	20	Q
6	I	19	Q
7	I	18	Q
8	I	17	Q
9	I	16	Q
10	I	15	Q
11	I	14	I/PRELOAD
12	GND	13	$\overline{OE}$

SN54PL20R8 (JT) SN74PL20R8 (JT,NT)

functional block diagram



~ denotes fused inputs.

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'PL333, 'PL335

FIELD-PROGRAMMABLE LOGIC SEQUENCERS

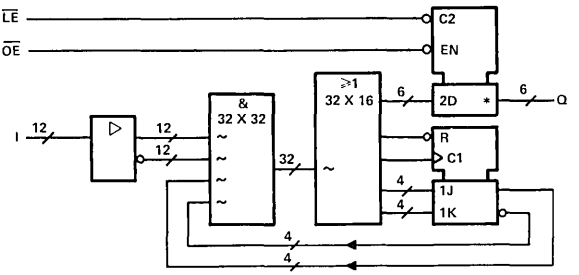
- 'PL333 – three-state outputs
- 'PL335 – open-collector outputs
- 12 input variables
- 32 product terms
- 6-bit output latch
- 4-bit state register

pin assignments

J, JT, NT PACKAGES			
1	I	13	Q
2	I	14	Q
3	I	15	Q
4	I	16	Q
5	I	17	$\overline{OE}$
6	I	18	$\overline{LE}$
7	I	19	PM
8	I	20	PL
9	I	21	I
10	Q	22	I
11	Q	23	I
12	GND	24	V_{CC}

SN54PL333 (J) SN74PL333 (JT,NT)
SN54PL335 (J) SN74PL335 (JT,NT)

functional block diagram



~ denotes fused inputs

- 'PL333 has 3-state (▽) outputs, 'PL335 has open-collector (◇) outputs.

nc – no internal connection.

'PL839, PL840

FIELD-PROGRAMMABLE LOGIC ARRAYS

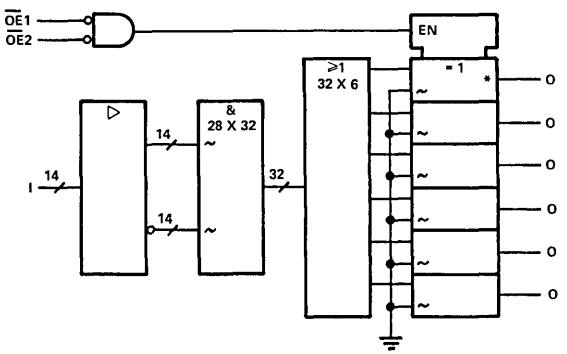
- 'PL839 — three-state outputs
- 'PL840 — open-collector outputs
- Programmable output polarity

pin assignments

J, JT, NT PACKAGES			
1	$\overline{OE1}$	13	$\overline{OE2}$
2	I	14	O
3	I	15	O
4	I	16	O
5	I	17	I
6	I	18	I
7	I	19	I
8	I	20	I
9	O	21	I
10	O	22	I
11	O	23	I
12	GND	24	V_{CC}

SN54PL839 (J) SN74PL839 (JT,NT)
SN54PL840 (J) SN74PL840 (JT,NT)

functional block diagram



~ denotes fused inputs.

* 'PL839 has 3-state (▽) outputs; 'PL840 has open-collector (◇) outputs.

nc — no internal connection.

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'PLR19L8

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

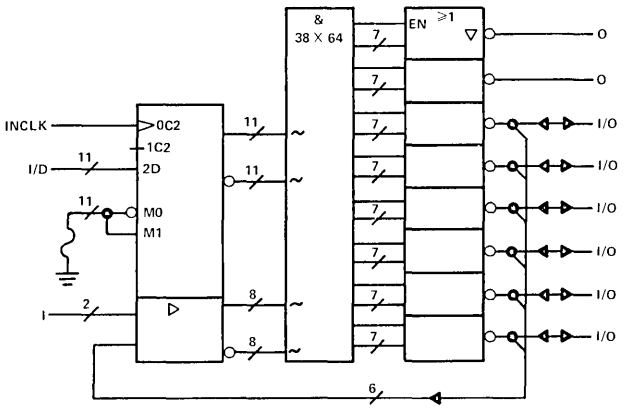
- Octal 19-input registered AND-OR-INVERT gate array

pin assignments

JT, NT PACKAGES			
1	I	13	I
2	I/D	14	INCLK/PRELOAD
3	I/D	15	O
4	I/D	16	I/O
5	I/D	17	I/O
6	I/D	18	I/O
7	I/D	19	I/O
8	I/D	20	I/O
9	I/D	21	I/O
10	I/D	22	O
11	I/D	23	I/D
12	GND	24	V_{CC}

SN54PLR19L8 (JT) SN74PLR19L8 (JT,NT)

functiona block diagram



'PLR19R4

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

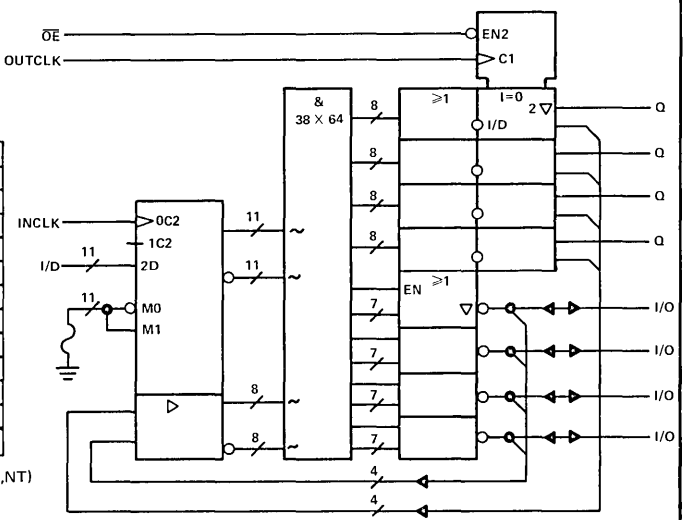
- Quad 19-input registered AND-OR gate array

pin assignments

JT, NT PACKAGES			
1	OUTCLK	13	$\overline{OE}$
2	I/D	14	INCLK/PRELOAD
3	I/D	15	I/O
4	I/D	16	I/O
5	I/D	17	Q
6	I/D	18	Q
7	I/D	19	Q
8	I/D	20	Q
9	I/D	21	I/O
10	I/D	22	I/O
11	I/D	23	I/D
12	GND	24	V_{CC}

SN54PLR19R4 (JT) SN74PLR19R4 (JT,NT)

functional block diagram



'PLR19R6

FIELD-PROGRAMMABLE
LOGIC, FIXED-OR ARRAYS

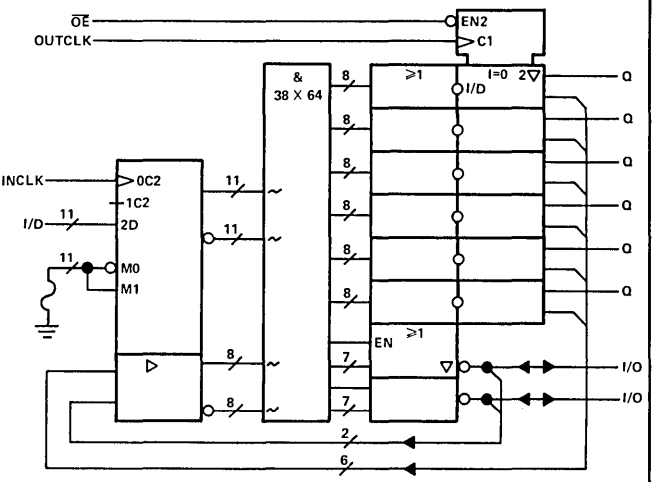
- Hex 19-input registered AND-OR gate array

pin assignments

JT, NT PACKAGES			
1	OUTCLK	13	$\overline{OE}$
2	I/D	14	INCLK/PRELOAD
3	I/D	15	I/O
4	I/D	16	Q
5	I/D	17	Q
6	I/D	18	Q
7	I/D	19	Q
8	I/D	20	Q
9	I/D	21	Q
10	I/D	22	I/O
11	I/D	23	I/D
12	GND	24	V_{CC}

SN54PLR19R6 (JT) SN74PLR19R6 (JT,NT)

functional block diagram



'PLR19R8

FIELD-PROGRAMMABLE
LOGIC, FIXED-OR ARRAYS

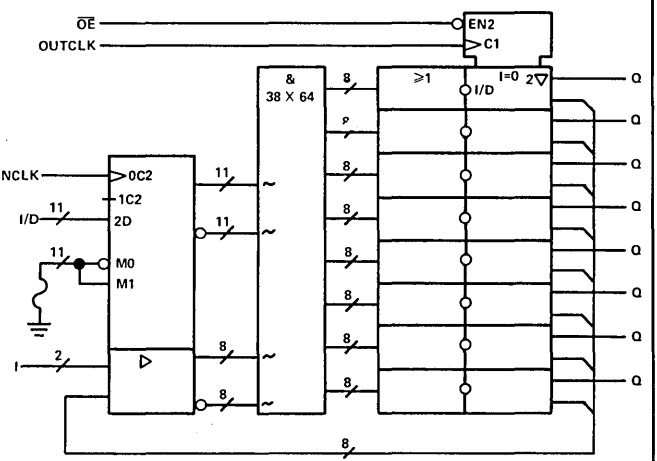
- Octal 19-input registered AND-OR gate array

pin assignments

JT, NT PACKAGES			
1	OUTCLK	13	$\overline{OE}$
2	I/D	14	INCLK/PRELOAD
3	I/D	15	Q
4	I/D	16	Q
5	I/D	17	Q
6	I/D	18	Q
7	I/D	19	Q
8	I/D	20	Q
9	I/D	21	Q
10	I/D	22	Q
11	I/D	23	I/D
12	GND	24	V_{CC}

SN54PLR19R8 (JT) SN74PLR19R8 (JT,NT)

functional block diagram



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'PLT19L8

FIELD-PROGRAMMABLE
LOGIC, FIXED-OR ARRAYS

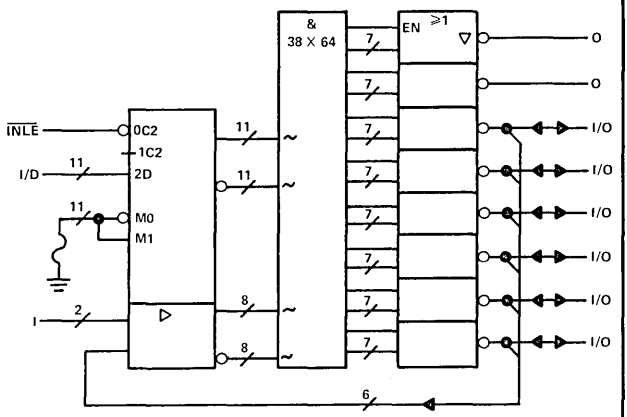
- Octal 19-input latched AND-OR-INVERT gate array

pin assignments

JT, NT PACKAGES			
1	I	13	I
2	I/D	14	$\overline{\text{INLE}}$/PRELOAD
3	I/D	15	O
4	I/D	16	I/O
5	I/D	17	I/O
6	I/D	18	I/O
7	I/D	19	I/O
8	I/D	20	I/O
9	I/D	21	I/O
10	I/D	22	O
11	I/D	23	I/D
12	GND	24	V_{CC}

SN54PLT19L8 (JT) SN74PLT19L8 (JT,NT)

functional block diagram



'PLT19R4

FIELD-PROGRAMMABLE
LOGIC, FIXED-OR ARRAYS

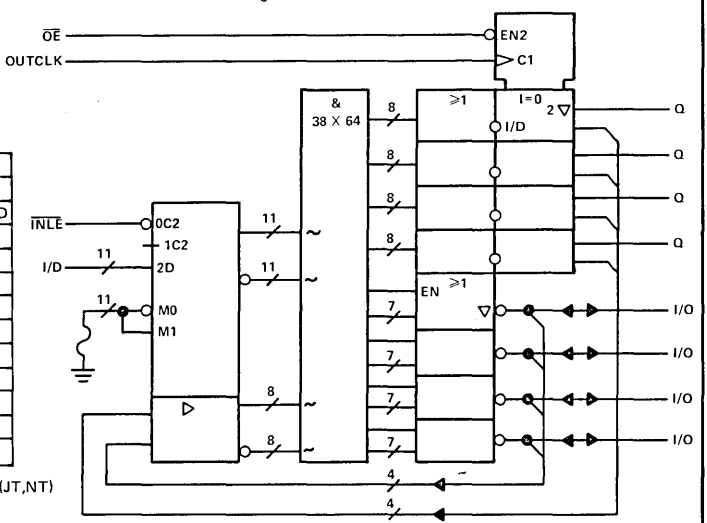
- Quad 19-input registered AND-OR gate array.

pin assignments

JT, NT PACKAGES			
1	OUTCLK	13	$\overline{\text{OE}}$
2	I/D	14	$\overline{\text{INLE}}$/PRELOAD
3	I/D	15	I/O
4	I/D	16	I/O
5	I/D	17	Q
6	I/D	18	Q
7	I/D	19	Q
8	I/D	20	Q
9	I/D	21	I/O
10	I/D	22	I/O
11	I/D	23	I/D
12	GND	24	V_{CC}

SN54PLT19R4 (JT) SN74PLT19R4 (JT,NT)

functional block diagram



'PLT19R6

FIELD-PROGRAMMABLE
LOGIC, FIXED-OR ARRAYS

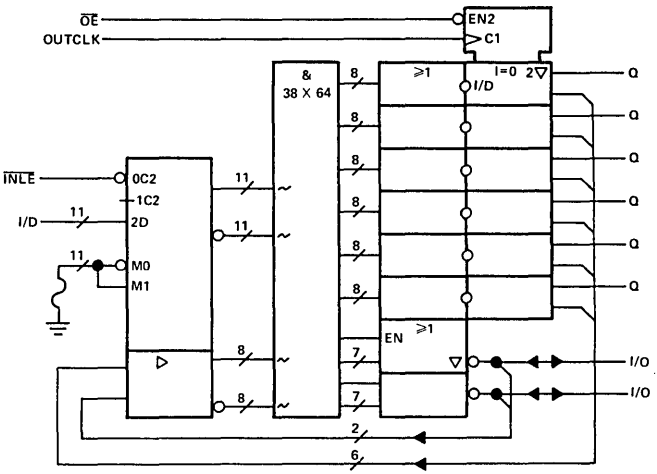
- Hex 19-input latched AND-OR gate array

pin assignments

JT, NT PACKAGES			
1	OUTCLK	13	$\overline{OE}$
2	I/D	14	$\overline{INLE}$/PRELOAD
3	I/D	15	I/O
4	I/D	16	Q
5	I/D	17	Q
6	I/D	18	Q
7	I/D	19	Q
8	I/D	20	Q
9	I/D	21	Q
10	I/D	22	I/O
11	I/D	23	I/D
12	GND	24	V_{CC}

SN54PLT19R6 (JT) SN74PLT19R6 (JT,NT)

functional block diagram



'PLT19R8

FIELD-PROGRAMMABLE
LOGIC, FIXED-OR ARRAYS

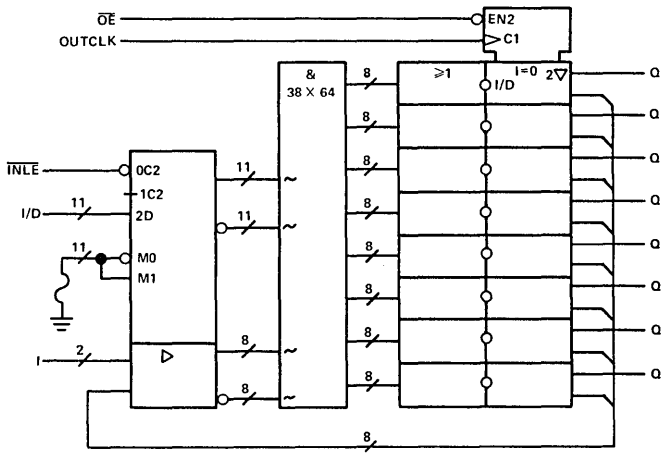
- Octal 19-input latched AND-OR gate array

pin assignments

JT, NT PACKAGES			
1	OUTCLK	13	$\overline{OE}$
2	I/D	14	$\overline{INLE}$/PRELOAD
3	I/D	15	Q
4	I/D	16	Q
5	I/D	17	Q
6	I/D	18	Q
7	I/D	19	Q
8	I/D	20	Q
9	I/D	21	Q
10	I/D	22	Q
11	I/D	23	I/D
12	GND	24	V_{CC}

SN54PLT19R8 (JT) SN74PLT19R8 (JT,NT)

functional block diagram



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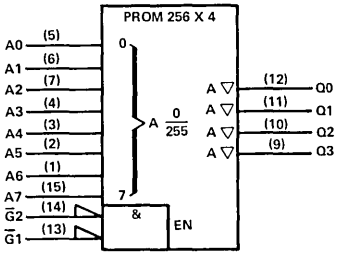
TBP14S10 ('S287)

PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 4
- Three-state outputs
- Typical address access time . . . 42 ns
- Typical power . . . 500 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A6	9 Q3
2 A5	10 Q2
3 A4	11 Q1
4 A3	12 Q0
5 A0	13 G1
6 A1	14 G2
7 A2	15 A7
8 GND	16 V_{CC}

For chip carrier options and information, contact the factory.

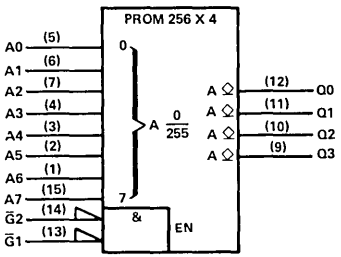
This product is no longer in production.
It is replaced by TBP24S10.

TBP14SA10 ('S387)

PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 4
- Open-collector outputs
- Typical address access time . . . 42 ns
- Typical power . . . 500 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A6	9 Q3
2 A5	10 Q2
3 A4	11 Q1
4 A3	12 Q0
5 A0	13 G1
6 A1	14 G2
7 A2	15 A7
8 GND	16 V_{CC}

For chip carrier options and information, contact the factory.

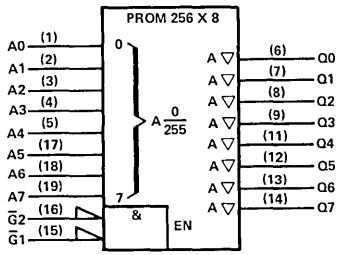
This product is no longer in production.
It is replaced by TBP24SA10.

TBP18S22 ('S471)

PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 8
- Three-state outputs
- Typical address access time . . . 50 ns
- Typical power . . . 550 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A0	11 Q4
2 A1	12 Q5
3 A2	13 Q6
4 A3	14 Q7
5 A4	15 $\overline{G1}$
6 Q0	16 $\overline{G2}$
7 Q1	17 A5
8 Q2	18 A6
9 Q3	19 A7
10 GND	20 V_{CC}

For chip carrier options and information, contact the factory.

This product is no longer in production.
It is replaced by TBP28L22.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

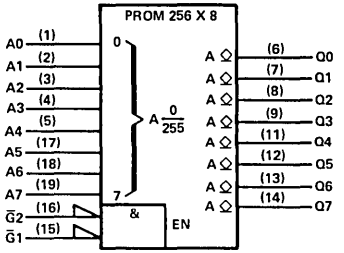
TBP18SA22 ('S470)

PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 8
- Open-collector outputs
- Typical address access time . . . 50 ns
- Typical power . . . 550 mW

This product is no longer in production. It is replaced by TBP28LA22.

logic symbol†



pin assignments

J, N PACKAGES	
1 A0	11 Q4
2 A1	12 Q5
3 A2	13 Q6
4 A3	14 Q7
5 A4	15 $\overline{G}1$
6 Q0	16 $\overline{G}2$
7 Q1	17 A5
8 Q2	18 A6
9 Q3	19 A7
10 GND	20 V_{CC}

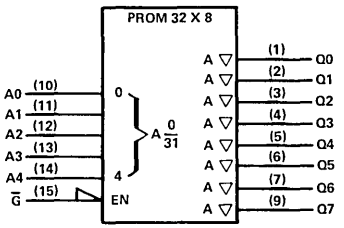
For chip carrier options and information, contact the factory.

TBP18S030 ('S288)

PROGRAMMABLE READ-ONLY MEMORIES

- 32 X 8
- Three-state outputs
- Typical address access time . . . 25 ns
- Typical power . . . 400 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 Q0	9 Q7
2 Q1	10 A0
3 Q2	11 A1
4 Q3	12 A2
5 Q4	13 A3
6 Q5	14 A4
7 Q6	15 $\overline{G}$
8 GND	16 V_{CC}

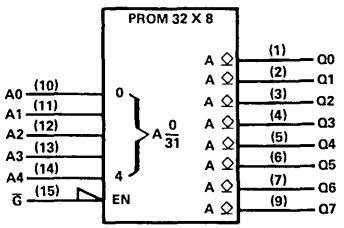
For chip carrier options and information, contact the factory.

TBP18SA030 ('S188)

PROGRAMMABLE READ-ONLY MEMORIES

- 32 X 8
- Open-collector outputs
- Typical address access time . . . 25 ns
- Typical power . . . 400 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 Q0	9 Q7
2 Q1	10 A0
3 Q2	11 A1
4 Q3	12 A2
5 Q4	13 A3
6 Q5	14 A4
7 Q6	15 $\overline{G}$
8 GND	16 V_{CC}

For chip carrier options and information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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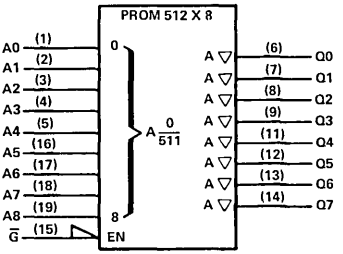
TBP18S42 ('S472)

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Typical address access time . . . 55 ns
- Typical power . . . 600 mW

This product is no longer in production.
It is replaced by TBP28S42.

logic symbol†



pin assignments

J, N PACKAGES	
1 A0	11 Q4
2 A1	12 Q5
3 A2	13 Q6
4 A3	14 Q7
5 A4	15 $\overline{G}$
6 Q0	16 A5
7 Q1	17 A6
8 Q2	18 A7
9 Q3	19 A8
10 GND	20 V_{CC}

For chip carrier options and information, contact the factory.

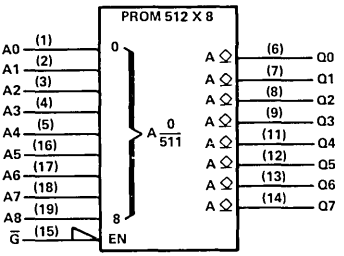
TBP18SA42 ('S473)

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Open-collector outputs
- Typical address access time . . . 55 ns
- Typical power . . . 600 mW

This product is no longer in production.
It is replaced by TBP28SA42.

logic symbol†



pin assignments

J, N PACKAGES	
1 A0	11 Q4
2 A1	12 Q5
3 A2	13 Q6
4 A3	14 Q7
5 A4	15 $\overline{G}$
6 Q0	16 A5
7 Q1	17 A6
8 Q2	18 A7
9 Q3	19 A8
10 GND	20 V_{CC}

For chip carrier options and information, contact the factory.

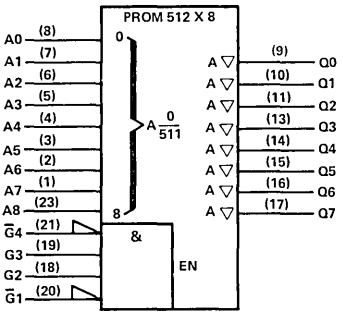
TBP18S46 ('S474)

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Typical address access time . . . 55 ns
- Typical power . . . 600 mW

This product is no longer in production.
It is replaced by TBP28S46.

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}1$
9 Q0	21 $\overline{G}4$
10 Q1	22 nc
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

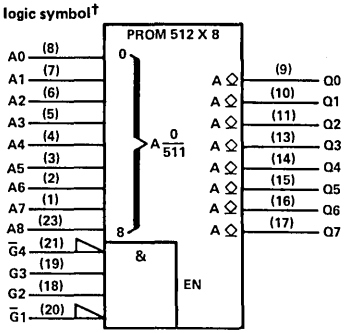
TBP18SA46 ('S475)

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Open-collector outputs
- Typical address access time . . . 55 ns
- Typical power . . . 600 mW

This product is no longer in production. It is replaced by TBP28SA46.

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G1}$
9 Q0	21 $\overline{G4}$
10 Q1	22 nc
11 Q2	23 A8
12 GND	24 V_{CC}

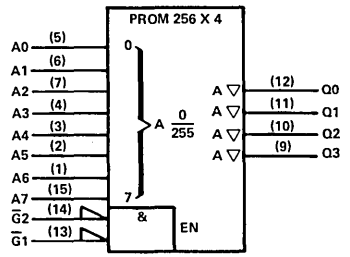
For chip carrier options and information, contact the factory.

TBP24S10

PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 4
- Three-state outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 375 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A6	9 Q3
2 A5	10 Q2
3 A4	11 Q1
4 A3	12 Q0
5 A0	13 G1
6 A1	14 G2
7 A2	15 A7
8 GND	16 V_{CC}

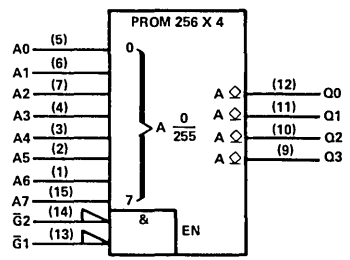
For chip carrier options and information, contact the factory.

TBP24SA10

PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 4
- Open-collector outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 375 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A6	9 Q3
2 A5	10 Q2
3 A4	11 Q1
4 A3	12 Q0
5 A0	13 G1
6 A1	14 G2
7 A2	15 A7
8 GND	16 V_{CC}

For chip carrier options and information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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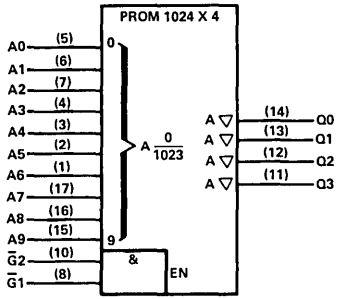
TBP24S41 ('S476)

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 4
- Three-state outputs
- Typical address access time . . . 40 ns
- Typical select time . . . 20 ns
- Typical power . . . 475 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	A6	10	$\overline{G}2$
2	A5	11	Q3
3	A4	12	Q2
4	A3	13	Q1
5	A0	14	Q0
6	A1	15	A9
7	A2	16	A8
8	$\overline{G}1$	17	A7
9	GND	18	V_{CC}

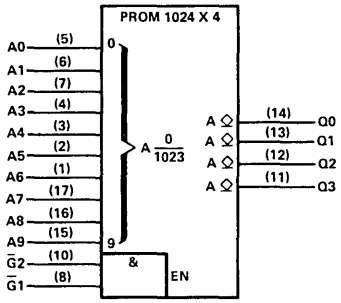
For chip carrier options and information, contact the factory.

TBP24SA41 ('S477)

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 4
- Open-collector outputs
- Typical address access time . . . 40 ns
- Typical select time . . . 20 ns
- Typical power . . . 475 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	A6	10	$\overline{G}2$
2	A5	11	Q3
3	A4	12	Q2
4	A3	13	Q1
5	A0	14	Q0
6	A1	15	A9
7	A2	16	A8
8	$\overline{G}1$	17	A7
9	GND	18	V_{CC}

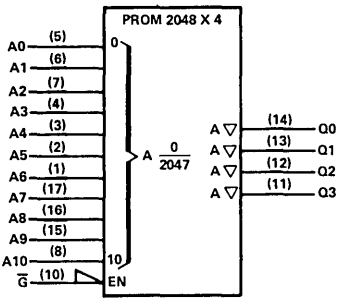
For chip carrier options and information, contact the factory.

TBP24S81 ('S454)
TBP24S81-55

PROGRAMMABLE READ-ONLY MEMORIES

- 2048 X 4
- Three-state outputs
- Typical address access time . . . 45 ns
- TBP24S81-55 maximum address access time . . . 55 ns
- Typical select time . . . 20 ns
- Typical power . . . 625 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	A6	10	$\overline{G}$
2	A5	11	Q3
3	A4	12	Q2
4	A3	13	Q1
5	A0	14	Q0
6	A1	15	A9
7	A2	16	A8
8	A10	17	A7
9	GND	18	V_{CC}

For chip carrier options and information, contact the factory.

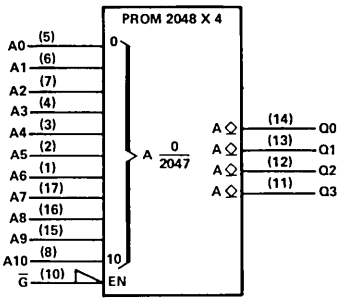
† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TBP24SA81 ('S455)
TBP24SA81-55

PROGRAMMABLE READ-ONLY MEMORIES

- 2048 X 4
- Open-collector outputs
- Typical address access time . . . 45 ns
- TBP24SA81-55 maximum address access time . . . 55 ns
- Typical select time . . . 20 ns
- Typical power . . . 625 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	A6	10	$\overline{G}$
2	A5	11	Q3
3	A4	12	Q2
4	A3	13	Q1
5	A0	14	Q0
6	A1	15	A9
7	A2	16	A8
8	A10	17	A7
9	GND	18	V_{CC}

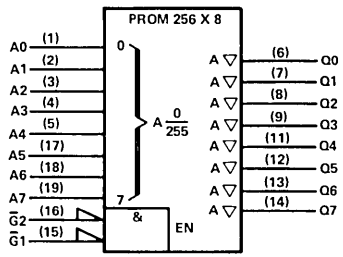
For chip carrier options and information, contact the factory.

TBP28L22

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 8
- Three-state outputs
- Typical address access time . . . 45 ns
- Typical select time . . . 20 ns
- Typical power . . . 375 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	A0	12	Q4
2	A1	13	Q5
3	A2	14	Q6
4	A3	15	Q7
5	A4	16	$\overline{G1}$
6	Q0	17	$\overline{G2}$
7	Q1	18	A5
8	Q2	19	A6
9	Q3	20	A7
10	GND		V_{CC}

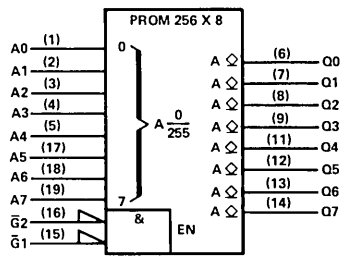
For chip carrier options and information, contact the factory.

TBP28LA22

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 8
- Open-collector outputs
- Typical address access time . . . 45 ns
- Typical select time . . . 20 ns
- Typical power . . . 375 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	A0	11	Q4
2	A1	12	Q5
3	A2	13	Q6
4	A3	14	Q7
5	A4	15	$\overline{G1}$
6	Q0	16	$\overline{G2}$
7	Q1	17	A5
8	Q2	18	A6
9	Q3	19	A7
10	GND	20	V_{CC}

For chip carrier options and information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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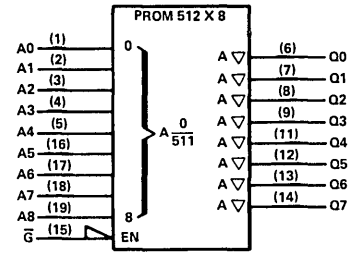
TBP28L42

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Typical address access time . . . 55 ns
- Typical select time . . . 25 ns
- Typical power . . . 275 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A0	11 Q4
2 A1	12 Q5
3 A2	13 Q6
4 A3	14 Q7
5 A4	15 $\overline{G}$
6 Q0	16 A5
7 Q1	17 A6
8 Q2	18 A7
9 Q3	19 A8
10 GND	20 V_{CC}

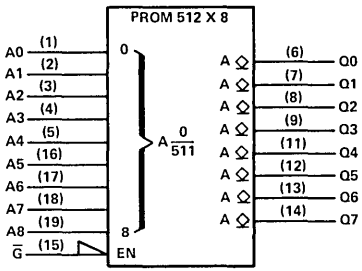
For chip carrier options and information, contact the factory.

TBP28LA42

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Open-collector outputs
- Typical address access time . . . 55 ns
- Typical select time . . . 25 ns
- Typical power . . . 275 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A0	11 Q4
2 A1	12 Q5
3 A2	13 Q6
4 A3	14 Q7
5 A4	15 $\overline{G}$
6 Q0	16 A5
7 Q1	17 A6
8 Q2	18 A7
9 Q3	19 A8
10 GND	20 V_{CC}

For chip carrier options and information, contact the factory.

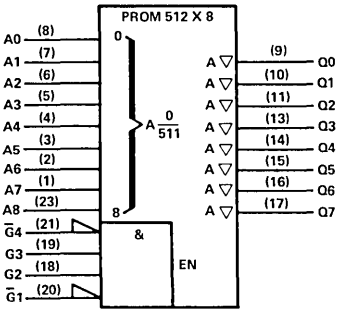
† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TBP28L45
TBP28L46

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Typical address access time . . . 55 ns
- Typical select time . . . 25 ns
- Typical power . . . 275 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G1}$
9 Q0	21 $\overline{G4}$
10 Q1	22 nc
11 Q2	23 A8
12 GND	24 V_{CC}

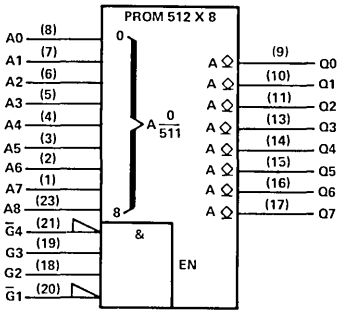
For chip carrier options and information, contact the factory.

TBP28LA45
TBP28LA46

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Open-collector outputs
- Typical address access time . . . 60 ns
- Typical select time . . . 30 ns
- Typical power . . . 250 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G1}$
9 Q0	21 $\overline{G4}$
10 Q1	22 nc
11 Q2	23 A8
12 GND	24 V_{CC}

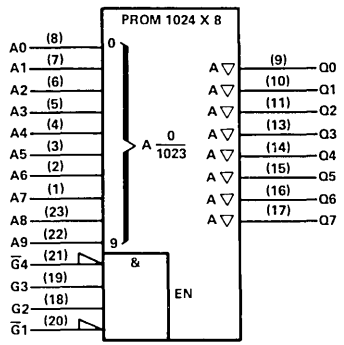
For chip carrier options and information, contact the factory.

TBP28L85A
TBP28L86A

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Three-state outputs
- Typical address access time . . . 65 ns
- Typical select time . . . 30 ns
- Typical power . . . 275 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G1}$
9 Q0	21 $\overline{G4}$
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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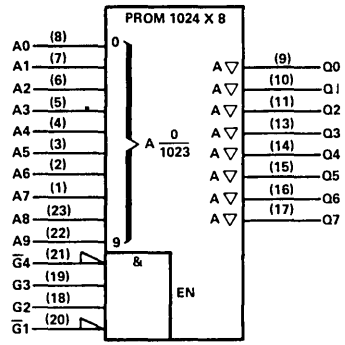
TBP28L86 ('LS478)

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Three-state outputs
- Typical address access address time . . . 80 ns
- Typical select time . . . 35 ns
- Typical power . . . 350 mW

TBP28L86 is no longer in production. It is replaced by TBP28L86A.

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}$1
9 Q0	21 $\overline{G}$4
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

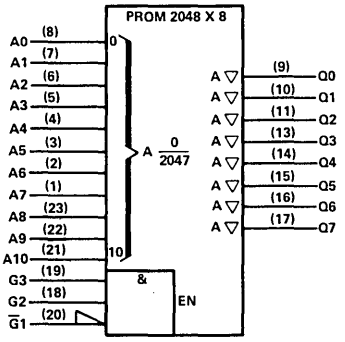
For chip carrier options and information, contact the factory.

TBP28L166A

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 2048 X 8
- Three-state outputs
- Typical address access time . . . 65 ns
- Typical select time . . . 30 ns
- Typical power . . . 350 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}$1
9 Q0	21 A10
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

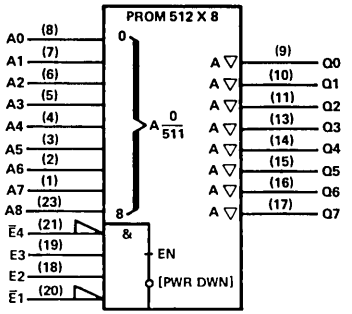
TBP28P45

POWER-DOWN PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Multiple enables
- Typical address access time . . . 35 ns
- Typical select time . . . 55 ns
- Typical power . . . 500/60 mW

See Page 2-13

logic symbol†



pin assignments

J, N PACKAGES			
1	A7	13	Q3
2	A6	14	Q4
3	A5	15	Q5
4	A4	16	Q6
5	A3	17	Q7
6	A2	18	E2
7	A1	19	E3
8	A0	20	$\overline{E1}$
9	Q0	21	$\overline{E4}$
10	Q1	22	nc
11	Q2	23	A8
12	GND	24	V_{CC}

For chip carrier options and information, contact the factory.

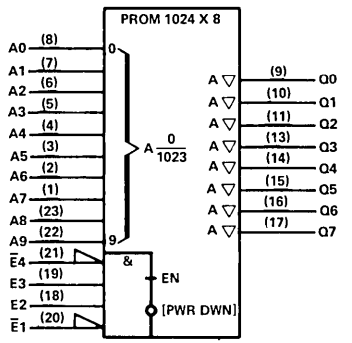
TBP28P85

POWER-DOWN PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Three-state outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 55 ns
- Typical power . . . 500/60 mW

See Page 2-13

logic symbol†



pin assignments

J, N PACKAGES			
1	A7	13	Q3
2	A6	14	Q4
3	A5	15	Q5
4	A4	16	Q6
5	A3	17	Q7
6	A2	18	E2
7	A1	19	E3
8	A0	20	$\overline{E1}$
9	Q0	21	$\overline{E4}$
10	Q1	22	A9
11	Q2	23	A8
12	GND	24	V_{CC}

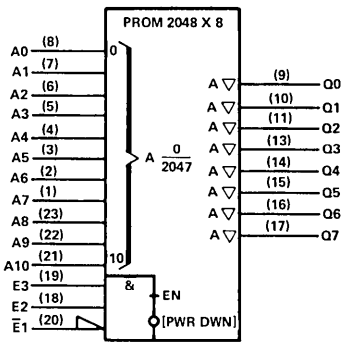
For chip carrier options and information, contact the factory.

TBP28P166

POWER-DOWN PROGRAMMABLE READ-ONLY MEMORIES

- 2048 X 8
- Three-state outputs
- Typical address access time . . . 35 ns
- Typical power . . . 650/125 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	A7	13	Q3
2	A6	14	Q4
3	A5	15	Q5
4	A4	16	Q6
5	A3	17	Q7
6	A2	18	E2
7	A1	19	E3
8	A0	20	$\overline{E1}$
9	Q0	21	A10
10	Q1	22	A9
11	Q2	23	A8
12	GND	24	V_{CC}

For chip carrier options and information, contact the factory.

See Page 2-13

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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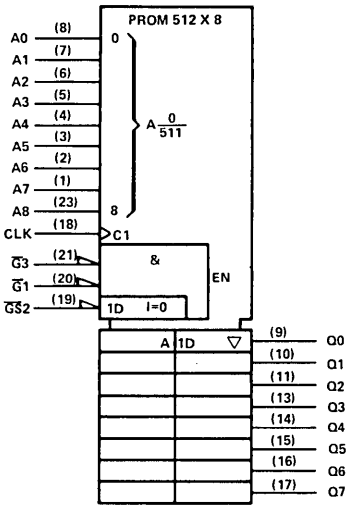
TBP28R45
TBP28R46

REGISTERED PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Typical clock-to-output time . . . 20 ns
- Typical address setup time . . . 20 ns
- Typical power . . . 550 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 CLK
7 A1	19 $\overline{GS2}$
8 A0	20 $\overline{G1}$
9 Q0	21 $\overline{G3}$
10 Q1	22 nc
11 Q2	23 A8
12 GND	24 V_{CC}

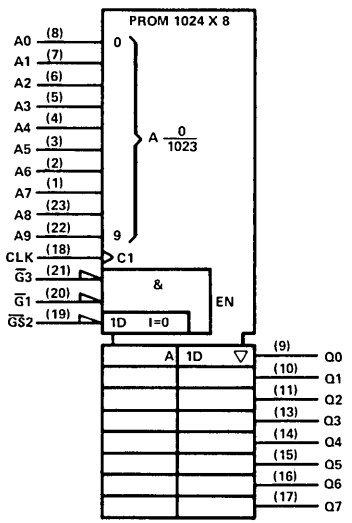
For chip carrier options and information, contact the factory.

TBP28R85A
TBP28R86A

REGISTERED PROGRAMMABLE READ-OUT MEMORIES

- 1024 X 8
- Three-state outputs
- Typical clock-to-output time . . . 20 ns
- Typical address setup time . . . 20 ns
- Typical power . . . 600 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 CLK
7 A1	19 $\overline{GS2}$
8 A0	20 $\overline{G1}$
9 Q0	21 $\overline{G3}$
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

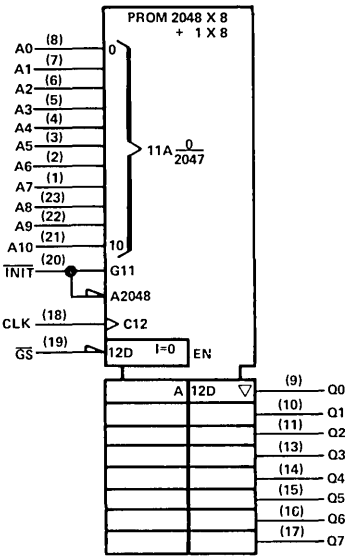
† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TBP28R165A
TBP28R166A

REGISTERED PROGRAMMABLE READ-ONLY MEMORIES WITH INITIALIZE

- Single dedicated input provides output initialize to user-programmed preset, clear, or any state
- 2048 X 8
- Three-state outputs
- Typical clock-to-output time . . . 20 ns
- Typical address setup time . . . 20 ns
- Typical power . . . 700 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 CLK
7 A1	19 $\overline{GS}$
8 A0	20 $\overline{INIT}$
9 Q0	21 A10
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

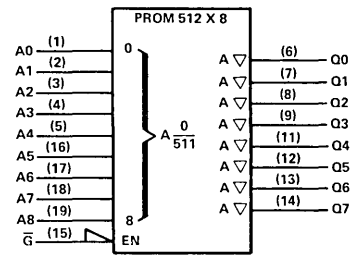
For chip carrier options and information, contact the factory.

TBP28S42

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 500 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A0	11 Q4
2 A1	12 Q5
3 A2	13 Q6
4 A3	14 Q7
5 A4	15 $\overline{G}$
6 Q0	16 A5
7 Q1	17 A6
8 Q2	18 A7
9 Q3	19 A8
10 GND	20 V_{CC}

For chip carrier options and information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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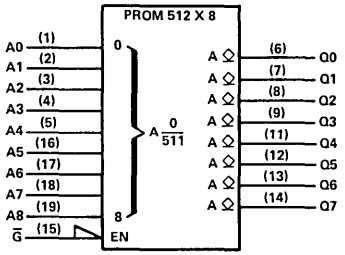
TBP28SA42

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Open-collector outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 500 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A0	11 Q4
2 A1	12 Q5
3 A2	13 Q6
4 A3	14 Q7
5 A4	15 $\overline{G}$
6 Q0	16 A5
7 Q1	17 A6
8 Q2	18 A7
9 Q3	19 A8
10 GND	20 V_{CC}

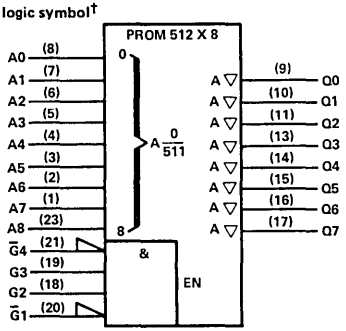
For chip carrier options and information, contact the factory.

TBP28S45
TBP28S46

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 500 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}$1
9 Q0	21 $\overline{G}$4
10 Q1	22 nc
11 Q2	23 A8
12 GND	24 V_{CC}

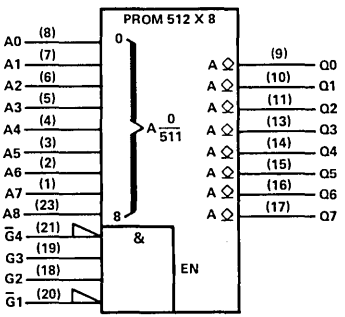
For chip carrier options and information, contact the factory.

TBP28SA45
TBP28SA45

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Open-collector outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 500 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}$1
9 Q0	21 $\overline{G}$4
10 Q1	22 nc
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

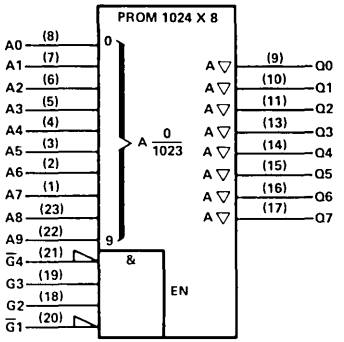
6

TBP28S85A
TBP28S85A-50

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Three-state outputs
- Typical address access time . . . 35 ns
- TBP28S85A-50 maximum address access time . . . 50 ns
- Typical select time . . . 20 ns
- Typical power . . . 550 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}1$
9 Q0	21 $\overline{G}4$
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

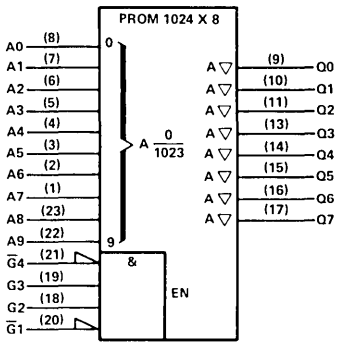
TBP28S86 ('S478)
TBP28S86-60

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Three-state outputs
- Typical address access time . . . 45 ns
- TBP28S86-60 maximum address access time . . . 60 ns
- Typical select time . . . 20 ns
- Typical power . . . 625 mW

These products are no longer in production. They are replaced by TBP28S86A and TBP28S86A-50.

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}1$
9 Q0	21 $\overline{G}4$
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

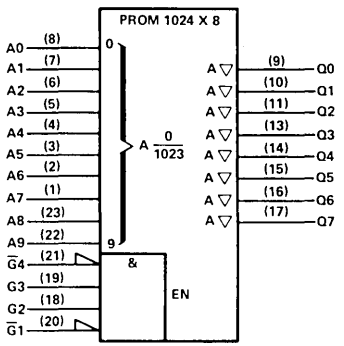
For chip carrier options and information, contact the factory.

TBP28S86A
TBP28S86A-50

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Three-state outputs
- Typical address access time . . . 35 ns
- TBP28S86A-50 maximum address access time . . . 50 ns
- Typical select time . . . 20 ns
- Typical power . . . 550 mw

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}1$
9 Q0	21 $\overline{G}4$
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc -- no internal connection.

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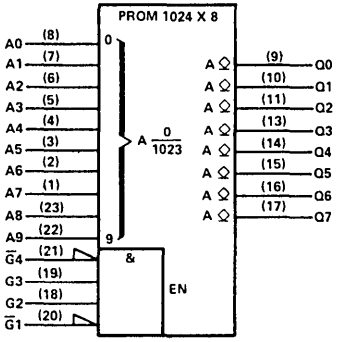
TBP28SA86 ('S479)
TBP28SA86-60

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Open-collector outputs
- Typical address access time . . . 45 ns
- TBP28SA86-60 maximum address access time . . . 60 ns
- Typical select time . . . 20 ns
- Typical power . . . 625 mW

These products are no longer in production. They are replaced by TBP28SA86A and TBP28SA86A-50.

logic symbol†



pin assignments

J, N PACKAGES			
1	A7	13	Q3
2	A6	14	Q4
3	A5	15	Q5
4	A4	16	Q6
5	A3	17	Q7
6	A2	18	G2
7	A1	19	G3
8	A0	20	$\overline{G}1$
9	Q0	21	$\overline{G}4$
10	Q1	22	A9
11	Q2	23	A8
12	GND	24	V_{CC}

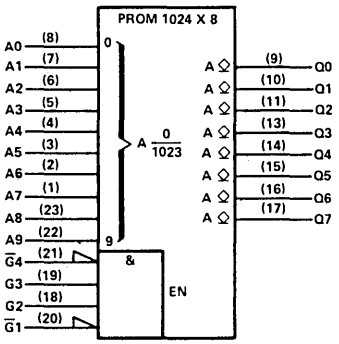
For chip carrier options and information, contact the factory.

TBP28SA86A
TBP28SA86A-50

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Open-collector outputs
- Typical address access time . . . 35 ns
- TBP28SA86A-50 maximum address access time . . . 50 ns
- Typical select time . . . 20 ns
- Typical power . . . 550 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	A7	13	Q3
2	A6	14	Q4
3	A5	15	Q5
4	A4	16	Q6
5	A3	17	Q7
6	A2	18	G2
7	A1	19	G3
8	A0	20	$\overline{G}1$
9	Q0	21	$\overline{G}4$
10	Q1	22	A9
11	Q2	23	A8
12	GND	24	V_{CC}

For chip carrier options and information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.

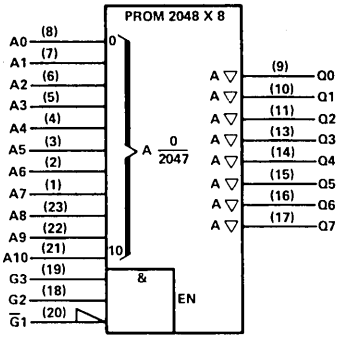
nc — no internal connection.

TBP28S165A
TBP28S165A-35
TBP28S166
TBP28S166A
TBP28S166A-35

PROGRAMMABLE READ-ONLY MEMORIES

- 2048 X 8
- Three-state outputs
- Typical select time . . . 15 ns

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G1}$
9 Q0	21 A10
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

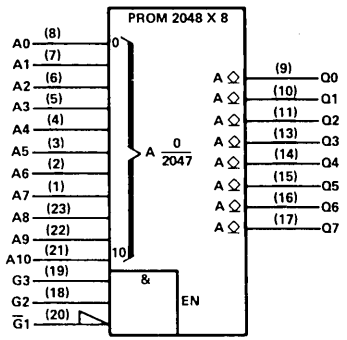
TYPE	PACKAGE ROW SPACING	TYPICAL ADDRESS ACCESS TIME	GUARANTEED MAXIMUM ACCESS TIME	TYPICAL POWER DISSIPATION
TBP28S165A	7.62 mm (0.300 in.)	25 ns		550 mW
TBP28S165A-35	7,62 mm (0.300 in.)	25 ns	35 ns	550 mW
TBP28S166	15,24 mm (0.600 in.)	35 ns		650 mW
TBP28S166A	15,24 mm (0.600 in.)	25 ns		50 mW
TBP28S166A-35	15,24 mm (0.600 in.)	25 ns	35 ns	550 mW

TBP28SA166 ('S453)

PROGRAMMABLE READ-ONLY MEMORIES

- 2048 X 8
- Open-collector outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 15 ns
- Typical power . . . 650 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G1}$
9 Q0	21 A10
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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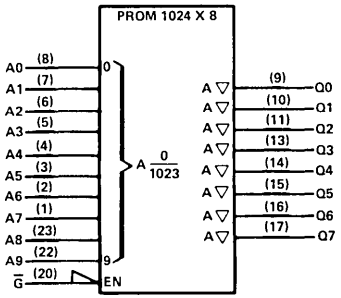
TBP28S2708 ('S2708)
TBP28S2708A

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Three-state outputs
- Typical select time . . . 20 ns

TBP28S2708 is no longer in production. It is replaced by TBP28S2708A.

logic symbol†



pin assignments

J, N PACKAGES			
1	A7	13	Q3
2	A6	14	Q4
3	A5	15	Q5
4	A4	16	Q6
5	A3	17	Q7
6	A2	18	nc
7	A1	19	nc
8	A0	20	$\overline{G}$
9	Q0	21	nc
10	Q1	22	A9
11	Q2	23	A8
12	GND	24	V_{CC}

For chip carrier options and information, contact the factory.

TYPE	TYPICAL ADDRESS ACCESS TIME	POWER POWER DISSIPATION
TBP28S2708	45 ns	625 mW
TBP28S2708A	35 ns	550 mW

† Pin numbers shown on logic symbols are for J and N packages only.
nc – no internal connection.

TIM8228	is the same as SN74S428
TIM8238	is the same as SN74S438
TIM9905	is the same as SN74LS251
TIM9906	is the same as SN74LS259
TIM9907	is the same as SN74148
TIM9908	is the same as SN74LS348

Explanation of New Logic Symbols

EXPLANATION OF NEW LOGIC SYMBOLS

TABLE OF CONTENTS

7

LIST OF TABLES

If you have questions on this Explanation of New Logic Symbols, please contact:

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Telephone (214) 995-2867

IEEE Standards may be purchased from:

Institute of Electrical and Electronics Engineers, In
345 East 47th Street
New York, N.Y. 10017

International Electrotechnical Commission (IEC) publications may be purchased from:

American National Standards Institute, Inc.
1430 Broadway
New York, N.Y. 10018

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by F. A. Mann

1 INTRODUCTION

The International Electrotechnical Commission (IEC) has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic circuit to each output without showing explicitly the internal logic. At the heart of the system is dependency notation, which will be explained in Section 4.

The system was introduced in the USA in a rudimentary form in IEEE/ANSI Standard Y32.14-1973. Lacking at that time a complete development of dependency notation, it offered little more than a substitution of rectangular shapes for the familiar distinctive shapes for representing the basic functions of AND, OR, negation, etc. This is no longer the case.

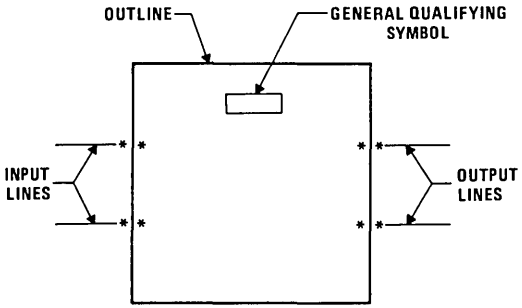
Internationally, Working Group 2 of IEC Technical Committee TC-3 is preparing a new document (Publication 617-12) that will consolidate the original work started in the mid 1960's and published in 1972 (Publication 117-15) and the amendments and supplements that have followed. Similarly for the USA, IEEE Committee SCC 11.9 is revising the publication IEEE Std 91/ANSI Y32.14. Texas Instruments is participating in the work of both organizations and this Data Book introduces new logic symbols in anticipation of the new standards. When changes are made as the standards develop, future editions will take those changes into account.

The following explanation of the new symbolic language is necessarily brief and greatly condensed from what the standards publications will finally contain. This is not intended to be sufficient for those people who will be developing symbols for new devices. It is primarily intended to make possible the understanding of the symbols used in this book; comparing the symbols with functional block diagrams and/or function tables will further help that understanding.

2 SYMBOL COMPOSITION

A symbol comprises an outline or a combination of outlines together with one or more qualifying symbols. The shape of the symbols is not significant. As shown in Figure 1, general qualifying symbols are used to tell exactly what logical operation is performed by the elements. Table I shows the general qualifying symbols used in this data book. Input lines are placed on the left and output lines are placed on the right. When an exception is made to that convention, the direction of signal flow is indicated by an arrow as shown in Figure 11.

All outputs of a single, unsubdivided element always have identical internal logic states determined by the function of the element except when otherwise indicated by an associated qualifying symbol or label inside the element.



*Possible positions for qualifying symbols relating to inputs and outputs

FIGURE 1 – SYMBOL COMPOSITION

The outlines of elements may be abutted or embedded in which case the following conventions apply. There is no logic connection between the elements when the line common to their outlines is in the direction of signal flow. There is at least one logic connection between the elements when the line common to their outlines is perpendicular to the direction of signal flow. The number of logic connections between elements will be clarified by the use of qualifying symbols and this is discussed further under that topic. If no indications are shown on either side of the common line, it is assumed there is only one connection.

When a circuit has one or more inputs that are common to more than one element of the circuit, the common-control block may be used. This is the only distinctively shaped outline used in the IEC system. Figure 2 shows that unless otherwise qualified by dependency notation, an input to the common-control block is an input to each of the elements below the common-control block.

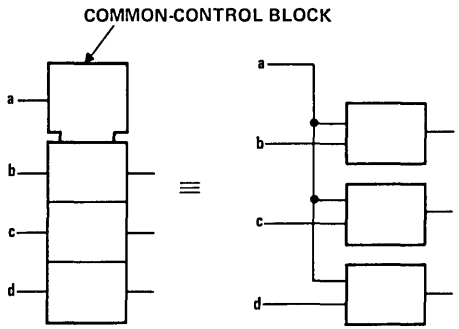


FIGURE 2 – ILLUSTRATION OF COMMON- CONTROL BLOCK

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A common output depending on all elements of the array can be shown as the output of a common-output element. Its distinctive visual feature is the double line at its top. In addition the common-output element may have other inputs as shown in Figure 3. The function of the common-output element must be shown by use of a general qualifying symbol.

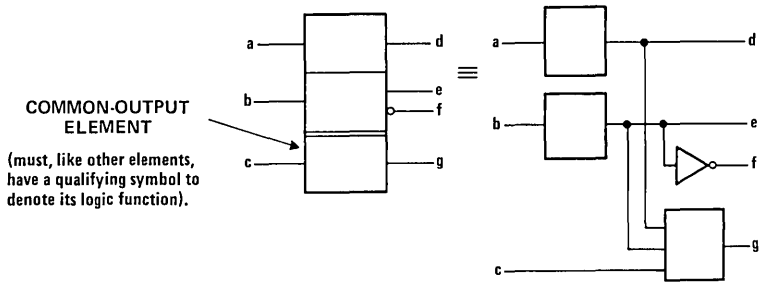

FIGURE 3 – ILLUSTRATION OF COMMON-OUTPUT ELEMENT

3 QUALIFYING SYMBOLS

3.1 General Qualifying Symbols

Table I shows the general qualifying symbols used in this data book. These characters are placed near the top center or the geometric center of a symbol or symbol element to define the basic function of the device represented by the symbol or of the element.

3.2 Qualifying Symbols for Inputs and Outputs

Qualifying symbols for inputs and outputs are shown in Table II and will be familiar to most users with the possible exception of the logic polarity and analog signal indicators. The older logic negation indicator means that the external 0 state produces the internal 1 state. The internal 1 state means the active state. Logic negation may be used in pure logic diagrams; in order to tie the external 1 and 0 logic states to the levels H (high) and L (low), a statement of whether positive logic (1 = H, 0 = L) or negative logic (1 = L, 0 = H) is being used is required or must be assumed. Logic polarity indicators eliminate the need for calling out the logic convention and are used in this data book in the symbology for actual devices. The presence of the triangular polarity indicator indicates that the L logic level will produce the internal 1 state (the active state) or that, in the case of an output, the internal 1 state will produce the external L level. Note how the active direction of transition for a dynamic input is indicated in positive logic, negative logic, and with polarity indication.

EXPLANATION OF NEW LOGIC SYMBOLS

TABLE I – GENERAL QUALIFYING SYMBOLS

SYMBOL	DESCRIPTION	EXAMPLE
&	AND gate or function.	SN7400
>1	OR gate or function. The symbol was chosen to indicate that at least one active input is needed to activate the output.	SN7402
=1	Exclusive OR. One and only one input must be active to activate the output.	SN7486
=	Logic identity. All inputs must stand at same state.	SN74180
2k	An even number of inputs must be active.	SN74180
2k+1	An odd number of inputs must be active.	SN74ALS86
1	The one input must be active.	SN7404
▷ or ◁	A buffer or element with more than usual output capability (symbol is oriented in the direction of signal flow).	SN74S436
⊓	Schmitt trigger; element with hysteresis.	SN74LS18
X/Y	Coder, code converter (DEC/BCD, BIN/OUT, BIN/7-SEG, etc.).	SN74LS347
MUX	Multiplexer/data selector.	SN74150
DMUX or DX	Demultiplexer.	SN74138
Σ	Adder.	SN74LS385
P–Q	Subtracter.	SN74LS385
CPG	Look-ahead carry generator.	SN74182
π	Multiplier.	SN74LS384
COMP	Magnitude comparator.	SN74LS682
ALU	Arithmetic logic unit.	SN74LS381
⎍	Retriggerable monostable.	SN74LS422
1⎍	Non-retriggerable monostable (one-shot).	SN74121
G⎍	Astable element. Showing waveform is optional.	SN74LS320
!G⎍	Synchronously starting astable.	SN74LS624
G!⎍	Astable element that stops with a completed pulse.	*
SRGm	Shift register. m = number of bits.	SN74LS595
CTRm	Counter. m = number of bits; cycle length = 2^m.	SN54LS590
CTR DIVm	Counter with cycle length = m.	SN74LS668
RCTRm	Asynchronous (ripple-carry) counter; cycle length = 2^m.	*
ROM	Read-only memory.	SN74187
RAM	Random-access read/write memory.	SN74170
FIFO	First-in, first-out memory.	SN74LS222
!=0	Element powers up cleared to 0 state.	SN74AS877
Φ	Highly complex function; "gray box" symbol with limited detail shown under special rules.	SN74LS608

*Not all of the general qualifying symbols have been used in this book, but they are included here for the sake of completeness.

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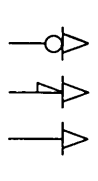
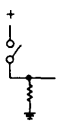
TABLE II – QUALIFYING SYMBOLS FOR INPUTS AND OUTPUTS

	Logic negation at input. External 0 produces internal 1.
	Logic negation at output. Internal 1 produces external 0.
	Active-low input. Equivalent to in positive logic.
	Active-low output. Equivalent to in positive logic.
	Active-low input in the case of right-to-left signal flow.
	Active-low output in the case of right-to-left signal flow.
	Signal flow from right to left. If not otherwise indicated, signal flow is from left to right.
	Bidirectional signal flow.
	
	Nonlogic connection. A label inside the symbol will usually define the nature of this pin.
	Input for analog signals.
	Internal connection. 1 state on left produces 1 state on right.
	Negated internal connection. 1 state on left produces 0 state on right.
	Dynamic internal connection. Transition from 0 to 1 on left produces transitory 1 state on right.
	Internal input (virtual input). It always stands at its internal 1 state unless affected by an overriding dependency relationship.
	Internal output (virtual output). Its effect on an internal input to which it is connected is indicated by dependency notation.

The internal connections between logic elements abutted together in a symbol may be indicated by the symbols shown. Each logic connection may be shown by the presence of qualifying symbols at one or both sides of the common line and if confusion can arise about the numbers of connections, use can be made of one of the internal connection symbols.

The internal (virtual) input is an input originating somewhere else in the circuit and is not connected directly to a terminal. The internal (virtual) output is likewise not connected directly to a terminal.

TABLE III – SYMBOLS INSIDE THE OUTLINE

¬	Postponed output (of a pulse-triggered flip-flop). The output changes when input initiating change (e.g., a C input) returns to its initial external state or level. See § 5.
⊓	Bi-threshold input (input with hysteresis)
◇	NPN open-collector or similar output that can supply a relatively low-impedance L level when not turned off. Requires external pull-up. Capable of positive-logic wired-AND connection. 
◈	Passive-pull-up output is similar to NPN open-collector output but is suplemented with a built-in passive pull-up.
◇	NPN open-emitter or similar output that can supply a relatively low-impedance H level when not turned off. Requires external pull-down. Capable of positive-logic wired-OR connection. 
◈	Passive-pull-down output is similar to NPN open-emitter output but is supplemented with a built-in passive pull-down.
▽	3-state output
▷	Output with more than usual output capability (symbol is oriented in the direction of signal flow).
EN	Enable input When at its internal 1-state, all outputs are enabled. When at its internal 0-state, open-collector and open-emitter outputs are off, three-state outputs are at normally defined internal logic states and at external high-impedance state, and all other outputs (e.g., totem-poles) are at the internal 0-state.
J, K, R, S, T	Usual meanings associated with flip-flops (e.g., R = reset, T = toggle)
D	Data input to a storage element equivalent to: 
→m ←m	Shift right (left) inputs, m = 1, 2, 3 etc. If m = 1, it is usually not shown.
+m −m	Counting up (down) inputs, m = 1, 2, 3 etc. If m = 1, it is usually not shown.
0 … m	Binary grouping. m is highest power of 2.
CT = 15	The contents-setting input, when active, causes the content of a register to take on the indicated value.
CT = 9	The content output is active if the content of the register is as indicated.
	Input line grouping . . . . indicates two or more terminals used to implement a single logic input. e.g., The paired expander inputs of SN7450. 
"1"	Fixed-state output always stands at its internal 1 state. For example, see SN74185.

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The application of internal inputs and outputs requires an understanding of dependency notation, which is explained in Section 4.

In an array of elements, if the same general qualifying symbol and the same qualifying symbols associated with inputs and outputs would appear inside each of the elements of the array, these qualifying symbols are usually shown only in the first element. This is done to reduce clutter and to save time in recognition. Similarly, large identical elements that are subdivided into smaller elements may each be represented by an unsubdivided outline. The SN54LS440 symbol illustrates this principle.

3.3 Symbols Inside the Outline

Table III shows some symbols used inside the outline. Note particularly that open-collector, open-emitter, and three-state outputs have distinctive symbols. Also note that an EN input affects all of the outputs of the circuit and has no effect on inputs. When an enable input affects only certain outputs and/or affects one or more inputs, a form of dependency notation will indicate this (see 4.9). The effects of the EN input on the various types of outputs are shown.

It is particularly important to note that a D input is always the data input of a storage element. At its internal 1 state, the D input sets the storage element to its 1 state, and at its internal 0 state it resets the storage element to its 0 state.

The binary grouping symbol will be explained more fully in Section 8. Binary-weighted inputs are arranged in order and the binary weights of the least-significant and the most-significant lines are indicated by numbers. In this data book weights of input and output lines will be represented by powers of two usually only when the binary grouping symbol is used, otherwise, decimal numbers will be used. The grouped inputs generate an internal number on which a mathematical function can be performed or that can be an identifying number for dependency notation. See Figure 28. A frequent use is in addresses for memories.

Reversed in direction, the binary grouping symbol can be used with outputs. The concept is analogous to that for the inputs and the weighted outputs will indicate the internal number assumed to be developed within the circuit.

Other symbols are used inside the outlines in this data book in accordance with the IEC/IEEE standards but are not shown here. Generally these are associated with arithmetic operations and are self-explanatory.

When nonstandardized information is shown inside an outline, it is usually enclosed in square brackets [like these].

4 DEPENDENCY NOTATION

4.1 General Explanation

Dependency notation is the powerful tool that sets the IEC symbols apart from previous systems and makes compact, meaningful, symbols possible. It provides the means of denoting the relationship between inputs, outputs, or inputs and outputs without actually showing all the elements and interconnections involved. The information provided by dependency notation supplements that provided by the qualifying symbols for an element's function.

In the convention for the dependency notation, use will be made of the terms "affecting" and "affected". In cases where it is not evident which inputs must be considered as being the affecting or the affected ones (e.g., if they stand in an AND relationship), the choice may be made in any convenient way.

So far, ten types of dependency have been defined and all of these are used in this data book. They are listed below in the order in which they are presented and are summarized in Table IV following 4.11.

Section	Dependency Type or Other Subject
4.2	G, AND
4.3	General rules for dependency notation
4.4	V, OR
4.5	N, Negate, (Exclusive OR)
4.6	Z, Interconnection
4.7	C, Control
4.8	S, Set and R, Reset
4.9	EN, Enable
4.10	M, Mode
4.11	A, Address

4.2 G (AND) Dependency

A common relationship between two signals is to have them ANDed together. This has traditionally been shown by explicitly drawing an AND gate with the signals connected to the inputs of the gate. The 1972 IEC publication and the 1973 IEEE/ANSI standard showed several ways to show this AND relationship using dependency notation. While nine other forms of dependency have since been defined, the ways to invoke AND dependency are now reduced to one.

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In Figure 4 input **b** is ANDed with input **a** and the complement of **b** is ANDed with **c**. The letter G has been chosen to indicate AND relationships and is placed at input **b**, inside the symbol. A number considered appropriate by the symbol designer (1 has been used here) is placed after the letter G and also at each affected input. Note the bar over the 1 at input **c**.

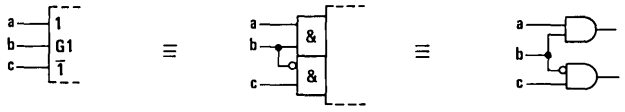

FIGURE 4 – G DEPENDENCY BETWEEN INPUTS

In Figure 5, output **b** affects input **a** with an AND relationship. The lower example shows that it is the internal logic state of **b**, unaffected by the negation sign, that is ANDed. Figure 6 shows input **a** to be ANDed with a dynamic input **b**.

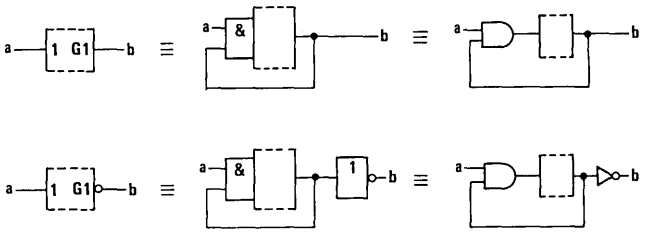

FIGURE 5 – G DEPENDENCY BETWEEN OUTPUTS AND INPUTS

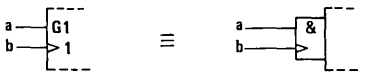

FIGURE 6 – G DEPENDENCY WITH A DYNAMIC INPUT

The rules for G dependency can be summarized thus:

When a G*m* input or output (*m* is a number) stands at its internal 1 state, all inputs and outputs affected by G*m* stand at their normally defined internal logic states. When the G*m* input or output stands at its 0 state, all inputs and outputs affected by G*m* stand at their internal 0 states.

4.3 Conventions for the Application of Dependency Notation in General

The rules for applying dependency relationships in general follow the same pattern as was illustrated for G dependency.

Application of dependency notation is accomplished by:

1) labeling the input (or output) *affecting* other inputs or outputs with the letter symbol indicating the relationship involved (e.g., G for AND) followed by an identifying number, appropriately chosen, and
2) labeling each input or output *affected* by that affecting input (or output) with that same number.

If it is the complement of the internal logic state of the affecting input or output that does the affecting, then a bar is placed over the identifying numbers at the affected inputs or outputs. See Figure 4.

If two affecting inputs or outputs have the same letter and same identifying number, they stand in an OR relationship to each other. See Figure 7.

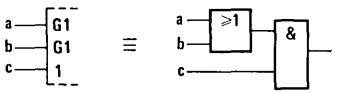

FIGURE 7 – OR'ED AFFECTING INPUTS

If the affected input or output requires a label to denote its function (e.g., "D"), this label will be *prefixed* by the identifying number of the affecting input. See Figure 12.

If an input or output is affected by more than one affecting input, the identifying numbers of each of the affecting inputs will appear in the label of the affected one, separated by commas. The normal reading order of these numbers is the same as the sequence of the affecting relationships. See Figure 12.

If the labels denoting the functions of affected inputs or outputs must be numbers, (e.g., outputs of a coder), the identifying numbers to be associated with both affecting inputs and affected inputs or outputs will be replaced by another character selected to avoid ambiguity, e.g., Greek letters. See Figure 8.

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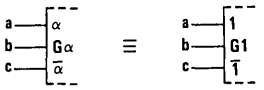


FIGURE 8 – SUBSTITUTION FOR NUMBERS

4.4 V (OR) Dependency

The symbol denoting OR dependency is the letter V. See Figure 9.

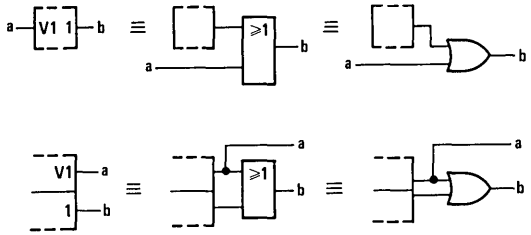
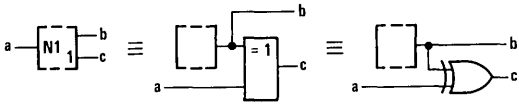


FIGURE 9 – V (OR) DEPENDENCY

When a V*m* input or output stands at its internal 1 state, all inputs and outputs affected by V*m* stand at their internal 1 states. When the V*m* input or output stands at its internal 0 state, all inputs and outputs affected by V*m* stand at their normally defined internal logic states.

4.5 N (Negate) (X-OR) Dependency

The symbol denoting negate dependency is the letter N. See Figure 10. Each input or output affected by an N*m* input or output stands in an exclusive-OR relationship with the N*m* input or output.



If a = 0, then c = b
If a = 1, then c = b

FIGURE 10 – N (NEGATE) (X-OR) DEPENDENCY

When an N*m* input or output stands at its internal 1 state, the internal logic state of each input and each output affected by N*m* is the complement of what it would otherwise be. When an N*m* input or output stands at its internal 0 state, all inputs and outputs affected by N*m* stand at their normally defined internal logic states.

4.6 Z (Interconnection) Dependency

The symbol denoting interconnection dependency is the letter Z.

Interconnection dependency is used to indicate the existence of internal logic connections between inputs, outputs, internal inputs, and/or internal outputs.

The internal logic state of an input or output affected by a Z*m* input or output will be the same as the internal logic state of the Z*m* input or output, unless modified by additional dependency notation. See Figure 11.

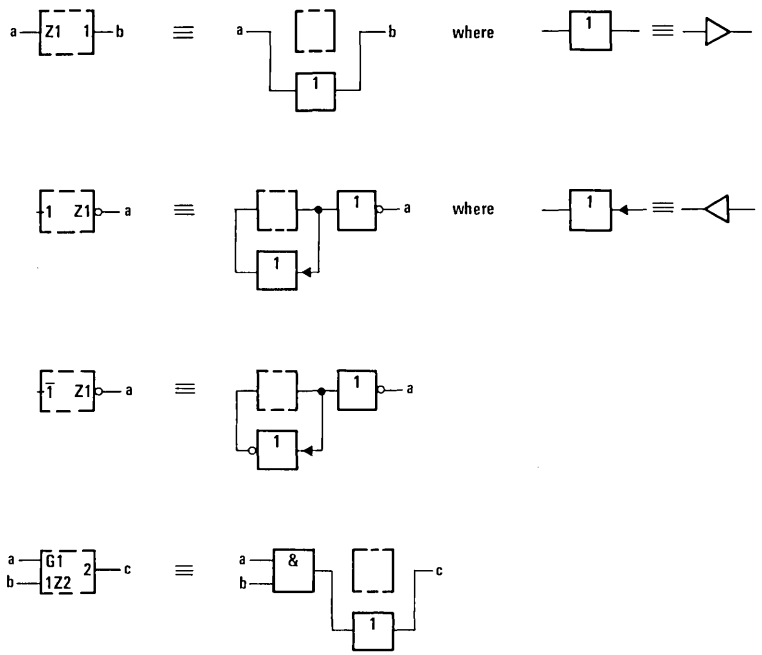


FIGURE 11 – Z (INTERCONNECTION) DEPENDENCY

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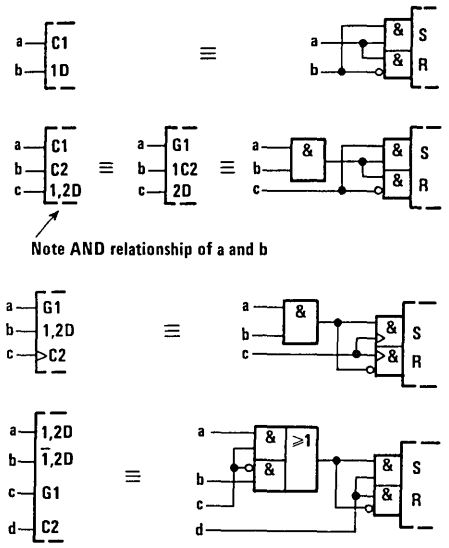
4.7 C (Control) Dependency

The symbol denoting control dependency is the letter C.

Control inputs are usually used to enable or disable the data (D, J, K, R, or S) inputs of storage elements. They may take on their internal 1 states (be active) either statically or dynamically. In the latter case the dynamic input symbol is used as shown in the third example of Figure 12.



Input c selects which of a or b is stored when d goes low.

FIGURE 12 – C (CONTROL) DEPENDENCY

When a C*m* input or output stands at its internal 1 state, the inputs affected by C*m* have their normally defined effect on the function of the element, i.e., these inputs are enabled. When a C*m* input or output stands at its internal 0 state, the inputs affected by C*m* are disabled and have no effect on the function of the element.

4.8 S (Set) and R (Reset) Dependencies

The symbol denoting set dependency is the letter S. The symbol denoting reset dependency is the letter R.

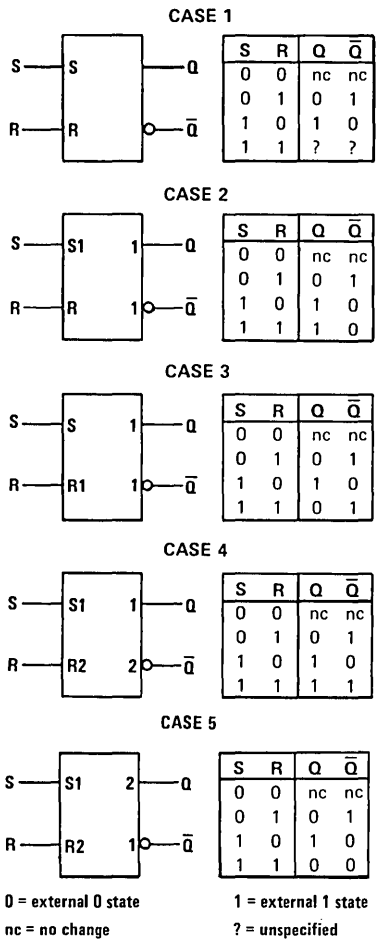
Set and reset dependencies are used if it is necessary to specify the effect of the combination R=S=1 on a bistable element. Case 1 in Figure 13 does not use S or R dependency.

When an S*m* input is at its internal 1 state, outputs affected by the Sm input will react, regardless of the state of an R input, as they normally would react to the combination S=1, R=0. See cases 2, 4, and 5 in Figure 13.

When an R*m* input is at its internal 1 state, outputs affected by the Rm input will react, regardless of the state of an S input, as they normally would react to the combination S=0, R=1. See cases 3, 4, and 5 in Figure 13.

When an S*m* or R*m* input is at its internal 0 state, it has no effect.

Note that the noncomplementary output patterns in cases 4 and 5 are only pseudo stable. The simultaneous return of the inputs to S=R=0 produces an unforeseeable stable and complementary output pattern.



S	R	Q	$\overline{Q}$
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	?	?

S	R	Q	$\overline{Q}$
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	1	0

S	R	Q	$\overline{Q}$
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	0	1

S	R	Q	$\overline{Q}$
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	1	1

S	R	Q	$\overline{Q}$
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	0	0

FIGURE 13 – S (SET) AND R (RESET) DEPENDENCIES

4.9 EN (Enable) Dependency

The symbol denoting enable dependency is the combination of letters EN.

An EN*m* input has the same effect on outputs as an EN input, see 3.1, but it effects only those outputs labeled with the identifying number *m*. It also affects those inputs labeled with the identifying number *m*. By contrast, an EN input affects all outputs and no inputs. The effect of an EN*m* input on an affected input is identical to that of a C*m* input. See Figure 14.

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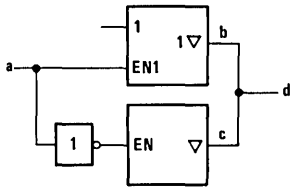
When an EN*m* input stands at its internal 1 state, the inputs affected by EN*m* have their normally defined effect on the function of the element and the outputs affected by this input stand at their normally defined internal logic states, i.e., these inputs and outputs are enabled.



If a = 0, b is disabled and d = c
If a = 1, c is disabled and d = b

FIGURE 14 – EN (ENABLE) DEPENDENCY

When an EN*m* input stands at its internal 0 state, the inputs affected by EN*m* are disabled and have no effect on the function of the element, and the outputs affected by EN*m* are also disabled. Open-collector outputs are turned off, three-state outputs stand at their normally defined internal logic states but externally exhibit high impedance, and all other outputs (e.g., totem-pole outputs) stand at their internal 0 states.

4.10 M (Mode) Dependency

The symbol denoting mode dependency is the letter M.

Mode dependency is used to indicate that the effects of particular inputs and outputs of an element depend on the mode in which the element is operating.

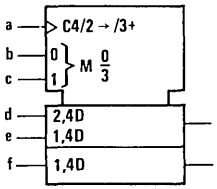
If an input or output has the same effect in different modes of operation, the identifying numbers of the relevant affecting M*m* inputs will appear in the label of that affected input or output between parentheses and separated by solidi. See Figure 19.

4.10.1 M Dependency Affecting Inputs

M dependency affects inputs the same as C dependency. When an M*m* input or M*m* output stands at its internal 1 state, the inputs affected by this M*m* input or M*m* output have their normally defined effect on the function of the element, i.e., the inputs are enabled.

When an M*m* input or M*m* output stands at its internal 0 state, the inputs affected by this M*m* input or M*m* output have no effect on the function of the element. When an affected input has several sets of labels separated by solidi (e.g., C4/2→/3+), any set in which the identifying number of the M*m* input or M*m* output appears has no effect and is to be ignored. This represents disabling of some of the functions of a multifunction input.

The circuit in Figure 15 has two inputs, **b** and **c**, that control which one of four modes (0, 1, 2, or 3) will exist at any time. Inputs **d**, **e**, and **f** are D inputs subject to dynamic control (clocking) by the **a** input. The numbers 1 and 2 are in the series chosen to indicate the modes so inputs **e** and **f** are only enabled in mode 1 (for parallel loading) and input **d** is only enabled in mode 2 (for serial loading). Note that input **a** has three functions. It is the clock for entering data. In mode 2, it causes right shifting of data, which means a shift away from the control block. In mode 3, it causes the contents of the register to be incremented by one count.



Note that all operations are synchronous.

In MODE 0 (b = 0, c = 0), the outputs remain at their existing states as none of the inputs has an effect.

In MODE 1 (b = 1, c = 0), parallel loading takes place thru inputs e and f.

In MODE 2 (b = 0, c = 1), shifting down and serial loading thru input d take place.

In MODE 3 (b = c = 1), counting up by increment of 1 per clock pulse takes place.

FIGURE 15 – M (MODE) DEPENDENCY AFFECTING INPUTS

7

4.10.2 M Dependency Affecting Outputs

When an M*m* input or M*m* output stands at its internal 1 state, the affected outputs stand at their normally defined internal logic states, i.e., the outputs are enabled.

When an M*m* input or M*m* output stands at its internal 0 state, at each affected output any set of labels containing the identifying number of that M*m* input or M*m* output has no effect and is to be ignored. When an output has several different sets of labels separated by solidi (e.g., 2,4/3,5), only those sets in which the identifying number of this M*m* input or M*m* output appears are to be ignored.

In Figure 16, mode 1 exists when the **a** input stands at its internal 1 state. The delayed output symbol is effective only in mode 1 (when input **a** = 1) in which case the device functions as a pulse-triggered flip-flop. See Section 5. When input **a** = 0, the device is not in mode 1 so the delayed output symbol has no effect and the device functions as a transparent latch.

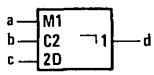


FIGURE 16 – TYPE OF FLIP-FLOP DETERMINED BY MODE

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In Figure 17, if input **a** stands at its internal 1 state establishing mode 1, output **b** will stand at its internal 1 state only when the content of the register equals 9. Since output **b** is located in the common-control block with no defined function outside of mode 1, the state of this output outside of mode 1 is not defined by the symbol.

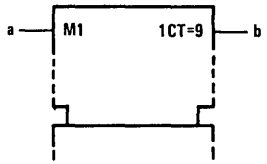

FIGURE 17 – DISABLING AN OUTPUT OF THE COMMON-CONTROL BLOCK

In Figure 18, if input **a** stands at its internal 1 state establishing mode 1, output **b** will stand at its internal 1 state only when the content of the register equals 15. If input **a** stands at its internal 0 state, output **b** will stand at its internal 1 state only when the content of the register equals 0.

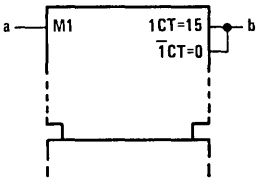

FIGURE 18 – DETERMINING AN OUTPUT'S FUNCTION

In Figure 19 inputs **a** and **b** are binary weighted to generate the numbers 0, 1, 2, or 3. This determines which one of the four modes exists.

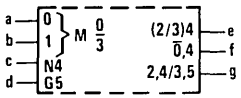

FIGURE 19 – DEPENDENT RELATIONSHIPS AFFECTED BY MODE

At output **e** the label set causing negation (if **c** = 1) is effective only in modes 2 and 3. In modes 0 and 1 this output stands at its normally defined state as if it had no labels. At output **f** the label set has effect when the mode is not 0 so output **e** is negated (if **c** = 1) in modes 1, 2, and 3. In mode 0 the label set has no effect so the output stands at its normally defined state. In this example 0,4 is equivalent to (1/2/3)4. At output **g** there are two label sets. The first set, causing negation (if **c** = 1), is effective only in mode 2. The second set, subjecting **g** to AND dependency on **d**, has effect only in mode 3.

Note that in mode 0 none of the dependency relationships has any effect on the outputs, so **e**, **f**, and **g** will all stand at the same state.

4.11 A (Address) Dependency

The symbol denoting address dependency is the letter A.

Address dependency provides a clear representation of those elements, particularly memories, that use address control inputs to select specified sections of a multidimensional array. Such a section of a memory array is usually called a word. The purpose of address dependency is to allow a symbolic presentation of the entire array. An input of the array shown at a particular element of this general section is common to the corresponding elements of all selected sections of the array. An output of the array shown at a particular element of this general section is the result of the OR function of the outputs of the corresponding elements of selected sections. If the label of an output of the array shown at a particular element of this general section indicates that this output is an open-circuit output or a three-state output, then this indication refers to the output of the array and not to those of the sections of the array.

Inputs that are not affected by any affecting address input have their normally defined effect on all sections of the array, whereas inputs affected by an address input have their normally defined effect only on the section selected by that address input.

An affecting address input is labelled with the letter A followed by an identifying number that corresponds with the address of the particular section of the array selected by this input. Within the general section presented by the symbol, inputs and outputs affected by an A*m* input are labelled with the letter A, which stands for the identifying numbers, i.e., the addresses, of the particular sections.

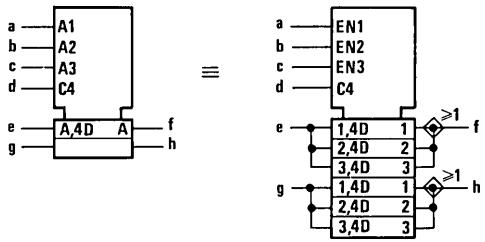

FIGURE 20 – A (ADDRESS) DEPENDENCY

Figure 20 shows a 3-word by 2-bit memory having a separate address line for each word and uses EN dependency to explain the operation. To select word 1, input **a** is taken to its 1 state, which establishes mode 1. Data can now be clocked into the inputs marked "1,4D". Unless words 2 and 3 are also selected, data cannot be clocked in at the inputs marked "2,4D" and "3,4D". The outputs will be the OR functions of the selected outputs, i.e., only those enabled by the active EN functions.

The identifying numbers of affecting address inputs correspond with the addresses of the sections selected by these inputs. They need not necessarily differ from those of other affecting dependency-inputs (e.g., G, V, N, . . .), because in the general section presented by the symbol they are replaced by the letter A.

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If there are several sets of affecting *Am* inputs for the purpose of independent and possibly simultaneous access to sections of the array, then the letter A is modified to 1A, 2A, . . . Because they have access to the same sections of the array, these sets of A inputs may have the same identifying numbers.

Figure 21 is another illustration of the concept.

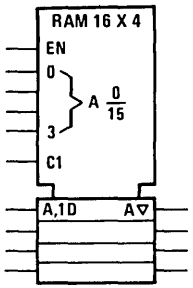

FIGURE 21

FIGURE 21 – ARRAY OF 16 SECTIONS OF FOUR TRANSPARENT LATCHES WITH 3-STATE OUTPUTS COMPRISING A 16-WORD X 4-BIT RANDOM-ACCESS MEMORY

TABLE IV – SUMMARY OF DEPENDENCY NOTATION

TYPE OF DEPENDENCY	LETTER SYMBOL*	AFFECTING INPUT AT ITS 1-STATE	AFFECTING INPUT AT ITS 0-STATE
Address	A	Permits action (address selected)	Prevents action (address not selected)
Control	C	Permits action	Prevents action
Enable	EN	Permits action	Prevents action of inputs. ◇outputs off. ▽outputs at external high impedance, no change in internal logic state. Other outputs at internal 0 state.
AND	G	Permits action	Imposes 0 state
Mode	M	Permits action (mode selected)	Prevents action (mode not selected)
Negate (X-OR)	N	Complements state	No effect
RESET	R	Affected output reacts as it would to S = 0, R = 1	No effect
SET	S	Affected output reacts as it would to S = 1, R = 0	No effect
OR	V	Imposes 1 state	Permits action
Interconnection	Z	Imposes 1 state	Imposes 0 state

*These letter symbols appear at the AFFECTING input (or output) and are followed by a number. Each input (or output) AFFECTED by that input is labeled with that same number. When the labels EN, R, and S appear at inputs without the following numbers, the descriptions above do not apply. The action of these inputs is described under "Symbols Inside The Outline", see 3.1.

BISTABLE ELEMENTS

The dynamic input symbol, the postponed output symbol, and dependency notation provide the tools to differentiate four main types of bistable elements and make synchronous and asynchronous inputs easily recognizable. See Figure 22. The first column shows the essential distinguishing features; the other columns show examples.

Transparent latches have a level-operated control input. The D input is active as long as the C input is at its internal 1 state. The outputs respond immediately. Edge-triggered elements accept data from D, J, K, R, or S inputs on the active transition of C. Pulse-triggered elements require the setup of data before the start of the control pulse; the C input is considered static since the data must be maintained as long as C is at its 1 state. The output is postponed until C returns to its 0 state. The data-lock-out element is similar to the pulse-triggered version except that the C input is considered dynamic in that shortly after C goes through its active transition, the data inputs are disabled and data does not have to be held. However, the output is still postponed until the C input returns to its initial external level.

Notice that synchronous inputs can be readily recognized by their dependency labels (1D, 1J, 1K, 1S, 1R) compared to the asynchronous inputs (S, R), which are not dependent on the C inputs.

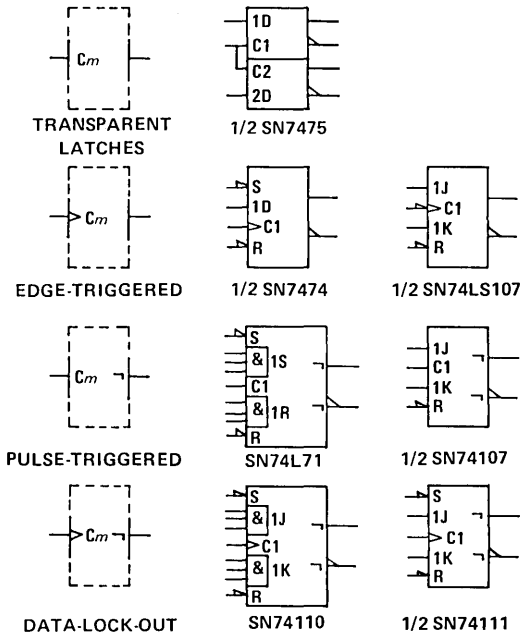

FIGURE 22 – FOUR TYPES OF BISTABLE CIRCUITS

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6 CODERS

The general symbol for a coder or code converter is shown in Figure 23. X and Y may be replaced by appropriate indications of the code used to represent the information at the inputs and at the outputs, respectively.

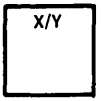


FIGURE 23 – CODER GENERAL SYMBOL

Indication of code conversion is based on the following rule:

> Depending on the input code, the internal logic states of the inputs determine an internal value. This value is reproduced by the internal logic states of the outputs, depending on the output code.

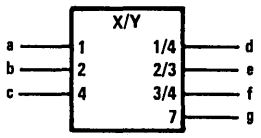
The indication of the relationships between the internal logic states of the inputs and the internal value is accomplished by:

1) labelling the inputs with numbers. In this case the internal value equals the sum of the weights associated with those inputs that stand at their internal 1-state, or by
2) replacing X by an appropriate indication of the input code and labelling the inputs with characters that refer to this code.

The relationships between the internal value and the internal logic states of the outputs are indicated by:

1) labelling each output with a list of numbers representing those internal values that lead to the internal 1-state of that output. These numbers shall be separated by solidi as in Figure 24. This labelling may also be applied when Y is replaced by a letter denoting a type of dependency (see Section 7). If a continuous range of internal values produces the internal 1 state of an output, this can be indicated by two numbers that are inclusively the beginning and the end of the range, with these two numbers separated by three dots, e.g., 4 . . . 9 = 4/5/6/7/8/9, or by
2) replacing Y by an appropriate indication of the output code and labelling the outputs with characters that refer to this code as in Figure 25.

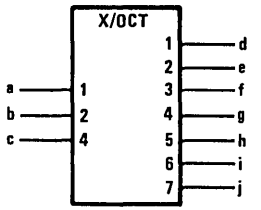
Alternatively, the general symbol may be used together with an appropriate reference to a table in which the relationship between the inputs and outputs is indicated. This is a recommended way to symbolize a PROM after it has been programmed.



TRUTH TABLE

INPUTS			OUTPUTS			
c	b	a	g	f	e	d
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	1	0
0	1	1	0	1	1	0
1	0	0	0	1	0	1
1	0	1	0	0	0	0
1	1	0	0	0	0	0
1	1	1	1	0	0	0

FIGURE 24 – AN X/Y CODE CONVERTER



TRUTH TABLE

INPUTS			OUTPUTS						
c	b	a	j	i	h	g	f	e	d
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	0
0	1	1	0	0	0	0	1	0	0
1	0	0	0	0	0	1	0	0	0
1	0	1	0	0	1	0	0	0	0
1	1	0	0	1	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0

FIGURE 25 – AN X/OCTAL CODE CONVERTER

7 USE OF A CODER TO PRODUCE AFFECTING INPUTS

It often occurs that a set of affecting inputs for dependency notation is produced by decoding the signals on certain inputs to an element. In such a case use can be made of the symbol for a coder as an embedded symbol. See Figure 26.

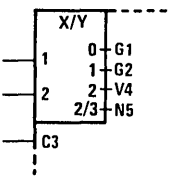


FIGURE 26 – PRODUCING VARIOUS TYPES OF DEPENDENCIES

If all affecting inputs produced by a coder are of the same type and their identifying numbers correspond with the numbers shown at the outputs of the coder, Y (in the qualifying symbol X/Y) may be replaced by the letter denoting the type of dependency. The indications of the affecting inputs should then be omitted. See Figure 27.

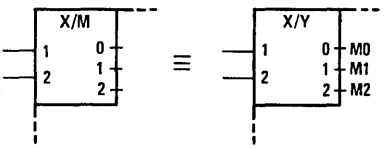


FIGURE 27 – PRODUCING ONE TYPE OF DEPENDENCY

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8 USE OF BINARY GROUPING TO PRODUCE AFFECTING INPUTS

If all affecting inputs produced by a coder are of the same type and have consecutive identifying numbers not necessarily corresponding with the numbers that would have been shown at the outputs of the coder, use can be made of the binary grouping symbol (see 3.1). k external lines effectively generate 2^k internal inputs. The bracket is followed by the letter denoting the type of dependency followed by $\frac{m1}{m2}$. The m1 is to be replaced by the smallest identifying number and the m2 by the largest one, as shown in Figure 28.

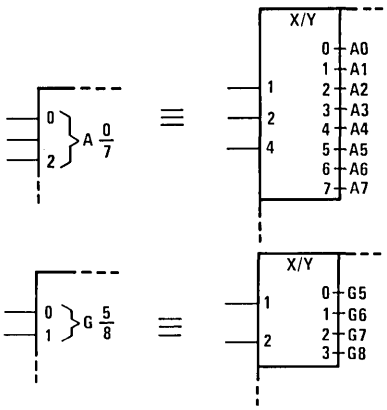

FIGURE 28 – USE OF THE BINARY GROUPING SYMBOL

9 SEQUENCE OF INPUT LABELS

If an input having a single functional effect is affected by other inputs, the qualifying symbol (if there is any) for that functional effect is preceded by the labels corresponding to the affecting inputs. The left-to-right order of these preceding labels is the order in which the effects or modifications must be applied. The affected input has no functional effect on the element if the logic state of any one of the affecting inputs, considered separately, would cause the affected input to have no effect, regardless of the logic states of other affecting inputs.

If an input has several different functional effects or has several different sets of affecting inputs, depending on the mode of action, the input may be shown as often as required. However, there are cases in which this method of presentation is not advantageous. In those cases the input may be shown once with the different sets of labels separated by solidi. See Figure 29. No meaning is attached to the order of these sets of labels. If one of the functional effects of an input is that of an unlabelled input of the element, a solidus will precede the first set of labels shown.

If all inputs of a combinational element are disabled (caused to have no effect on the function of the element), the internal logic states of the outputs of the element are not specified by the symbol. If all inputs of a sequential element are disabled, the content of this element is not changed and the outputs remain at their existing internal logic states.

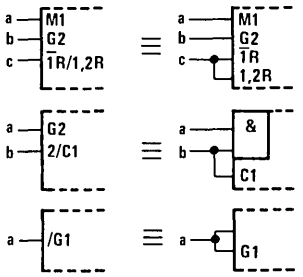

FIGURE 29 – INPUT LABELS

Labels may be factored using algebraic techniques.

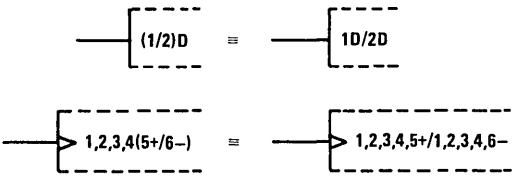

FIGURE 30 – FACTORING INPUT LABELS

10 SEQUENCE OF OUTPUT LABELS

If an output has a number of different labels, regardless of whether they are identifying numbers of affecting inputs or outputs or not, these labels are shown in the following order:

1) if the postponed output symbol has to be shown, this comes first, if necessary preceded by the indications of the inputs to which it must be applied;

2) followed by the labels indicating modifications of the internal logic state of the output, such that the left-to-right order of these labels corresponds with the order in which their effects must be applied;

3) followed by the label indicating the effect of the output on inputs and other outputs of the element.

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Symbols for open-circuit or three-state outputs, where applicable, are placed just inside the outside boundary of the symbol adjacent to the output line. See Figure 31.

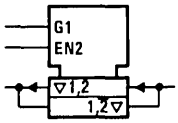

FIGURE 31 – PLACEMENT OF 3-STATE SYMBOLS

If an output needs several different sets of labels that represent alternative functions (e.g., depending on the mode of action), these sets may be shown on different output lines that must be connected outside the outline. However, there are cases in which this method of presentation is not advantageous. In those cases the output may be shown once with the different sets of labels separated by solidi. See Figure 32.

Two adjacent identifying numbers of affecting inputs in a set of labels that are not already separated by a nonnumeric character should be separated by a comma.

If a set of labels of an output not containing a solidus contains the identifying number of an affecting M*m* input standing at its internal 0 state, this set of labels has no effect on that output.

Labels may be factored using algebraic techniques.

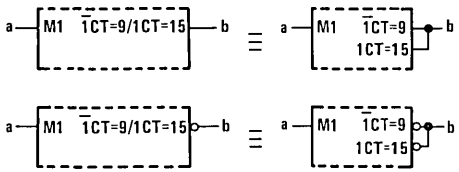

FIGURE 32 – OUTPUT LABELS

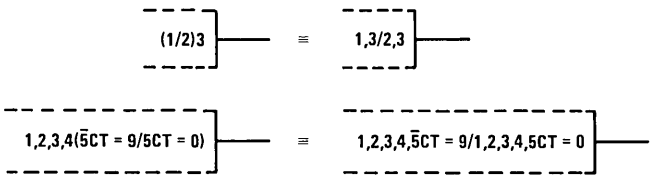

FIGURE 33 – FACTORING OUTPUT LABELS

If you have questions on this Explanation of New Logic Symbols, please contact:

F.A. Mann MS 49
Texas Instruments Incorporated
P.O. Box 225012
Dallas, Texas 75265
Telephone (214) 995-2867

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International Electrotechnical Commission (IEC) publications may be purchased from:

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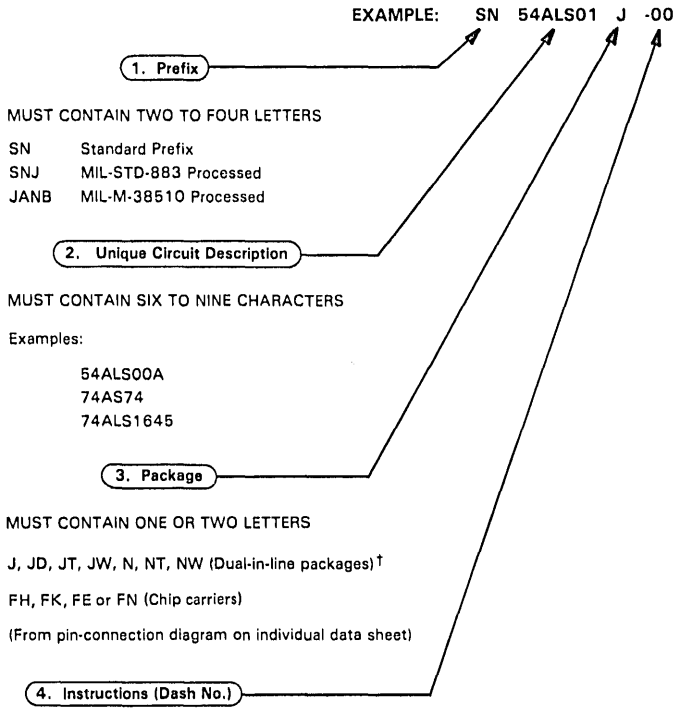
1430 Broadway
New York, N.Y. 10018

Ordering Instructions and Mechanical Data

ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.



† These circuits in dual-in-line packages are shipped in one of the carriers shown below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped in the most practical carrier. Please contact your TI sales representative for the method that will best suit your particular needs.

Dual-in-line (J, JD, JT, JW, N, NT, NW)

- Slide Magazines
- A-Channel Plastic Tubing
- Barnes Carrier (N only)
- Sectioned Cardboard Box
- Individual Plastic Box

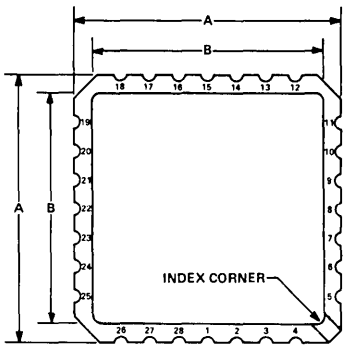
FH and FK ceramic chip carrier packages

Both versions of these hermetically sealed chip carrier packages have ceramic bases. The FH package has a single-layer base with a ceramic lid and glass seal. The FK package has a three-layer base with a metal lid and braze seal.

The packages are intended for surface mounting on solder lands on 1,27 (0.050-inch) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

FH and FK packages are identical to the FC and FD packages, respectively. The new designations are used to indicate devices whose terminal assignments conform to a forthcoming JEDEC Standard.

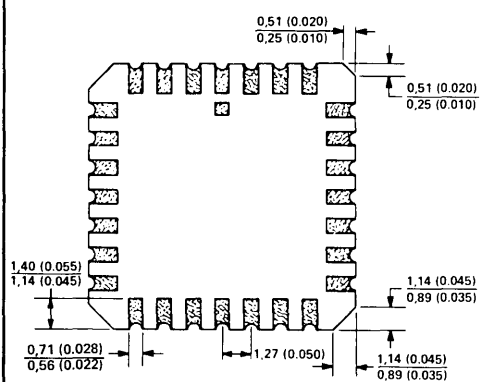
FH AND FK CERAMIC CHIP CARRIER PACKAGES
(28-terminal package shown)

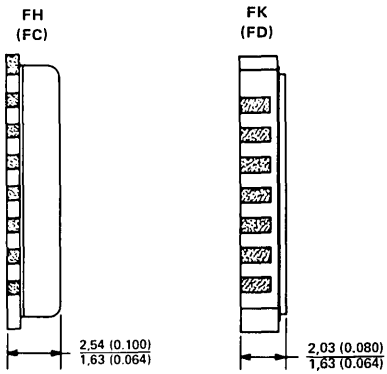


CERAMIC CHIP CARRIERS

JEDEC OUTLINE DESIGNATION*	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX
MS004CB	20	8,69 (0.342)	9,09 (0.358)	7,80 (0.307)	9,09 (0.358)
MS004CC	28	11,23 (0.442)	11,63 (0.458)	10,31 (0.406)	11,63 (0.458)
MS004CD	44	16,26 (0.640)	16,76 (0.660)	12,58 (0.495)	14,22 (0.560)
MS004CE	52	18,78 (0.739)	19,32 (0.761)	12,58 (0.495)	14,22 (0.560)
MS004CF	68	23,83 (0.938)	24,43 (0.962)	12,6 (0.495)	21,8 (0.862)
MS004CG	84	28,83 (1.135)	29,59 (1.165)	12,6 (0.495)	27,0 (1.065)

*All dimensions and notes for the specified JEDEC outline apply.





ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

TEXAS INSTRUMENTS
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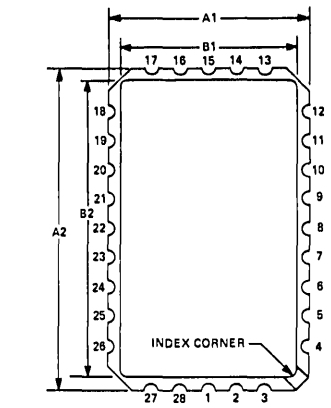
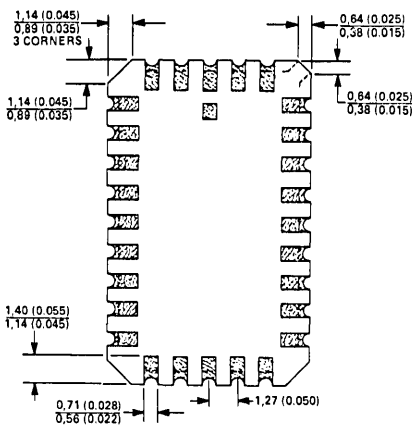
FE ceramic chip carrier packages

Each of these hermetically sealed leadless chip carrier packages has a metal cap, a 3-layer ceramic base, and a brazed seal. The packages are intended for surface mounting on solder lands on 1,27-mm (0.050-inch) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

RECTANGULAR FE CERAMIC CHIP CARRIER PACKAGE
(28-terminal package shown)



NUMBER OF TERMINALS	A1		A2		B1		B2		C2	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
28	8,76 (0.345)	9,02 (0.355)	13,84 (0.545)	14,10 (0.555)	7,80 (0.307)	7,95 (0.313)	12,88 (0.507)	13,03 (0.513)	1,65 (0.065)	2,01 (0.079)
32	11,30 (0.445)	11,56 (0.455)	13,84 (0.545)	14,10 (0.555)	10,34 (0.407)	13,03 (0.513)	12,88 (0.507)	13,03 (0.513)	1,65 (0.065)	2,01 (0.079)



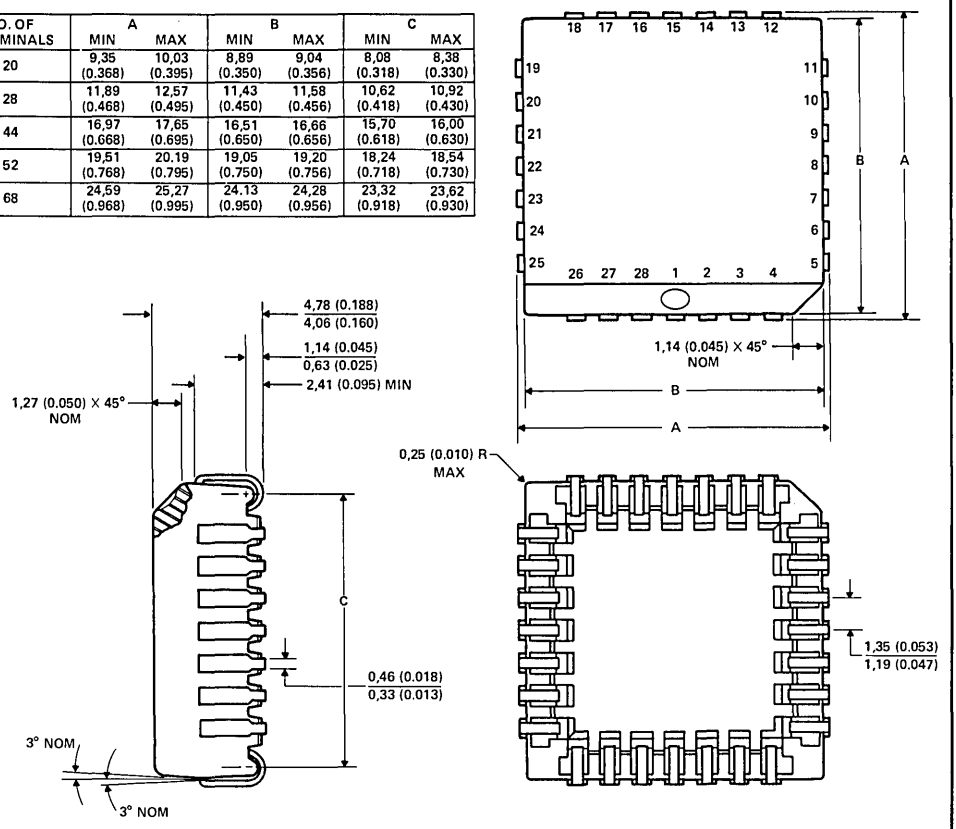
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

FN plastic chip carrier package

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 1,27-mm (0.050-inch) centers. Leads require no additional cleaning or processing when used in soldered assembly.

FN PLASTIC CHIP CARRIER PACKAGE
(28-terminal package shown)

NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
20	9,35 (0.368)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	8,08 (0.318)	8,38 (0.330)
28	11,89 (0.468)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	10,62 (0.418)	10,92 (0.430)
44	16,97 (0.668)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	15,70 (0.618)	16,00 (0.630)
52	19,51 (0.768)	20,19 (0.795)	19,05 (0.750)	19,20 (0.756)	18,24 (0.718)	18,54 (0.730)
68	24,59 (0.968)	25,27 (0.995)	24,13 (0.950)	24,28 (0.956)	23,32 (0.918)	23,62 (0.930)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

TEXAS INSTRUMENTS
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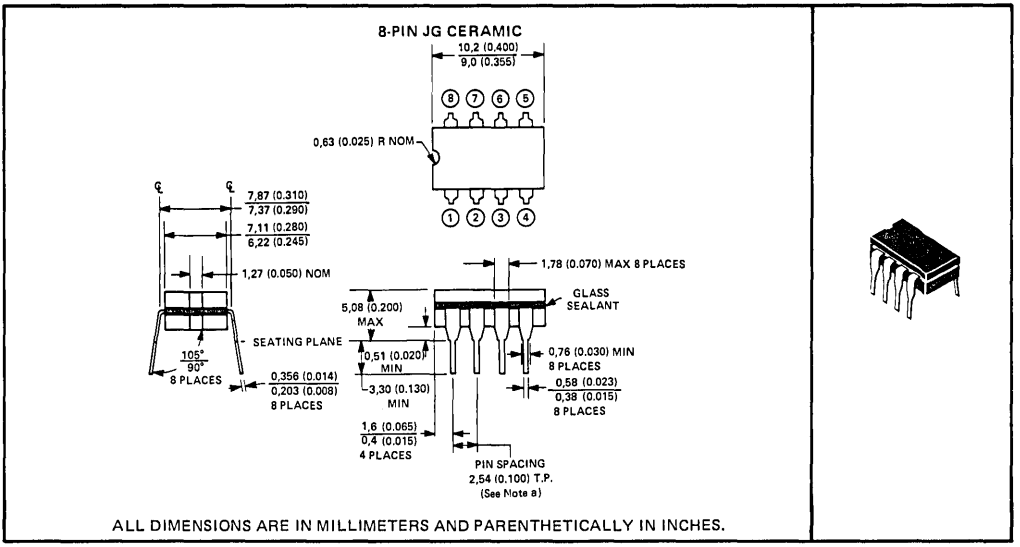
JG ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and 8-lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers (see Note a). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Non-shiny tin-plated leads require no additional cleaning or processing when used in soldered assembly.



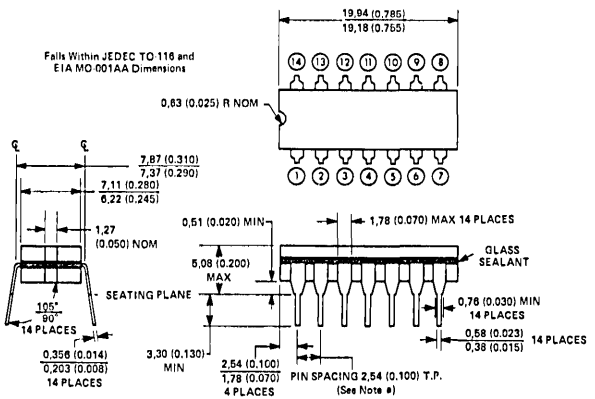
NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

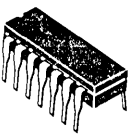
J ceramic packages (including JT and JW dual-in-line and JQ quad-in-line packages)

Each of these hermetically sealed dual-in-line packages consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The JT packages are intended for insertion in mounting-hole rows on 7,62 (0.300) centers, JW packages for mounting-hole rows on 15,24 (0.600) centers, and the JQ quad-in-line package for mounting-hole rows on 15,24 (0.600) and 20,32 (0.800) centers. Once the leads are compressed and inserted sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For the 14-, 16-, and 20-pin packages, the letter J is used by itself since these packages are available only in the 7,62 (0.300) row spacing. For the 24-pin packages, if no second letter or row spacing is specified, the package is assumed to have 15,24 (0.600) row spacing.

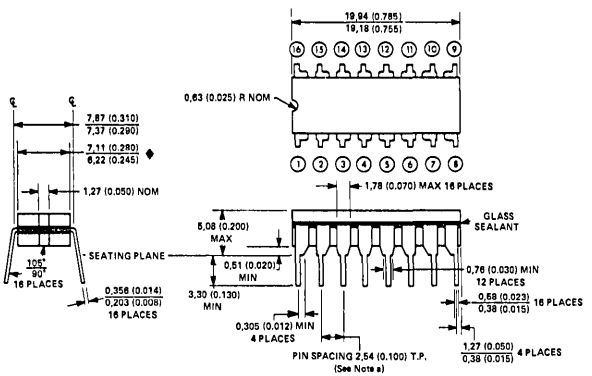
14-PIN J CERAMIC

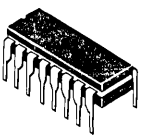




ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

16-PIN J CERAMIC





♦ For memories of 64 bits and up and a few MSI/LSI products in Series 54/74 and Series 54S/74S that are derived from memory circuit bars, this maximum is 7,62 (0.300). All other dimensions apply without modification.

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

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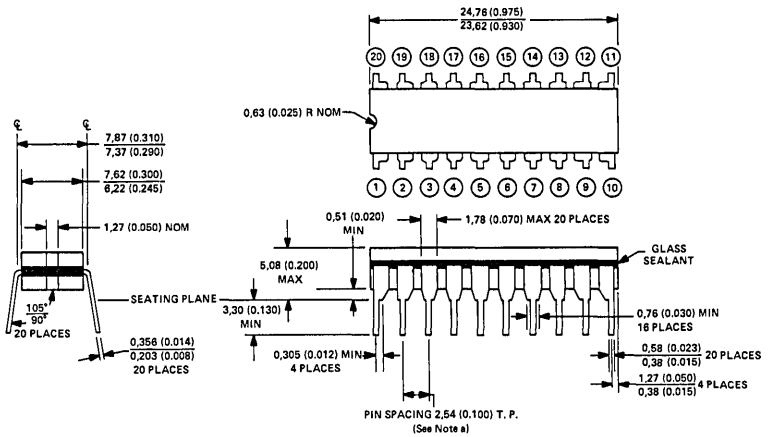
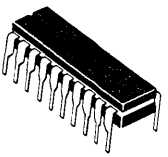
J ceramic dual-in-line packages (continued)

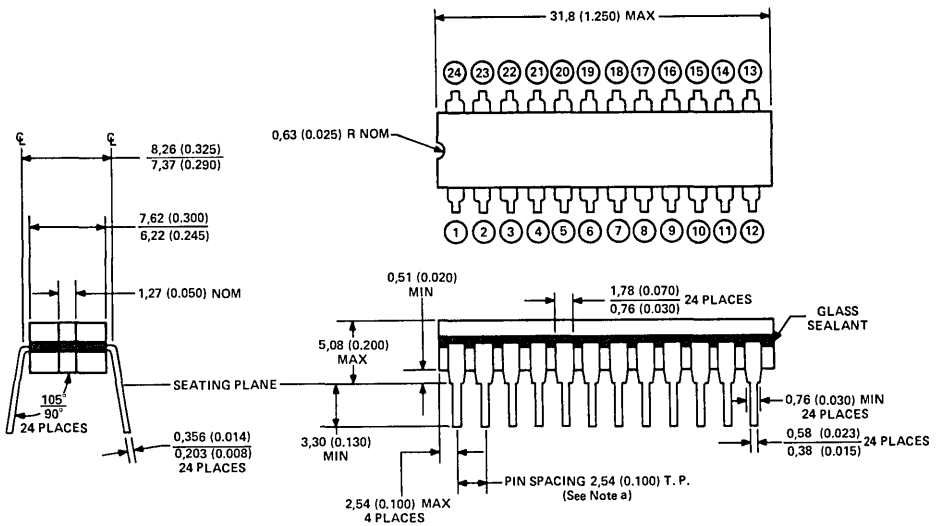
20-PIN J CERAMIC





ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

24-PIN JT CERAMIC, 0.300-INCH ROW SPACING

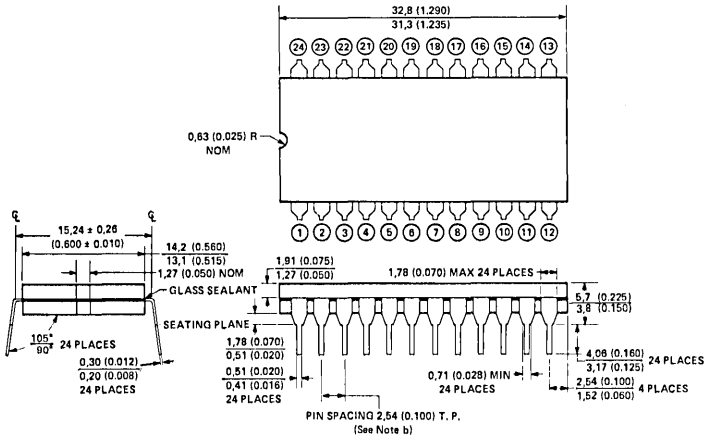


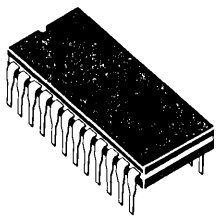
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

J ceramic dual-in-line packages (continued)

24-PIN JW CERAMIC





Falls within JEDEC MO-015AA dimensions

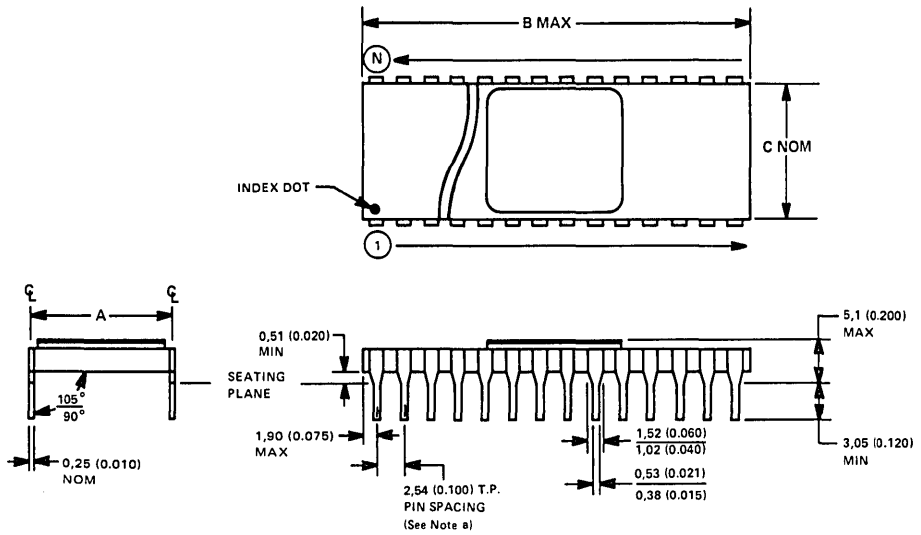
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

8

ceramic packages – side-braze (JD suffix)

This is a hermetically sealed ceramic package with a metal cap and side-brazed tin-plated leads.



DIM \ PINS	24	28	40	48	52	64
A ± 0,25 (0.010)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)	22,86 (0.900)
B MAX	31,8 (1.25)	36,8 (1.45)	52,1 (2.05)	62,2 (2.45)	67,3 (2.65)	82,6 (3.25)
C NOM	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	22,6 (0.890)

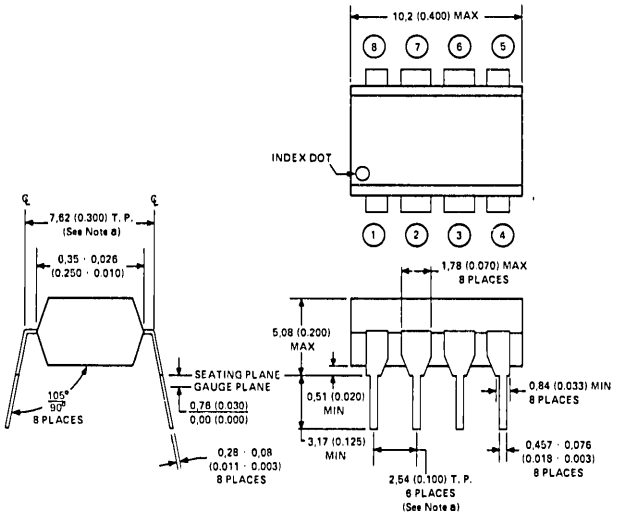
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

P plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on an 8-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62-mm (0.300) centers (see Note a). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Solder-plated leads require no additional cleaning or processing when used in soldered assembly.

8-PIN P PLASTIC



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTE: a. Each pin is within 0,13 (0.0005) radius of true position (TP) at the gauge plane with maximum material condition and unit installed.

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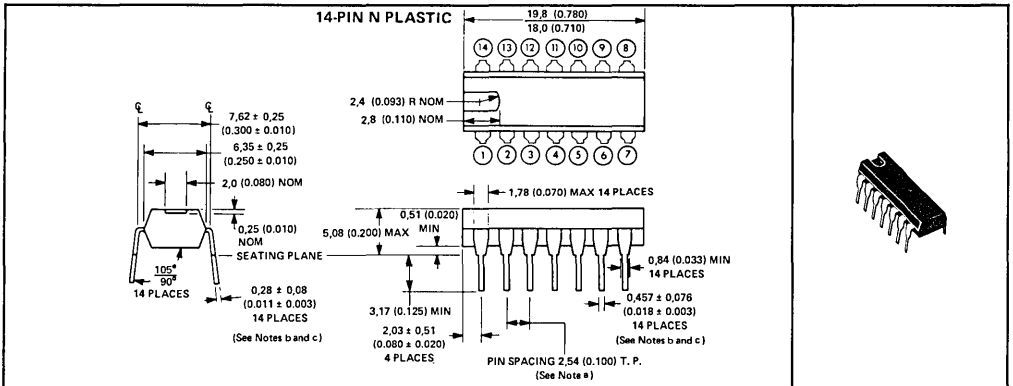
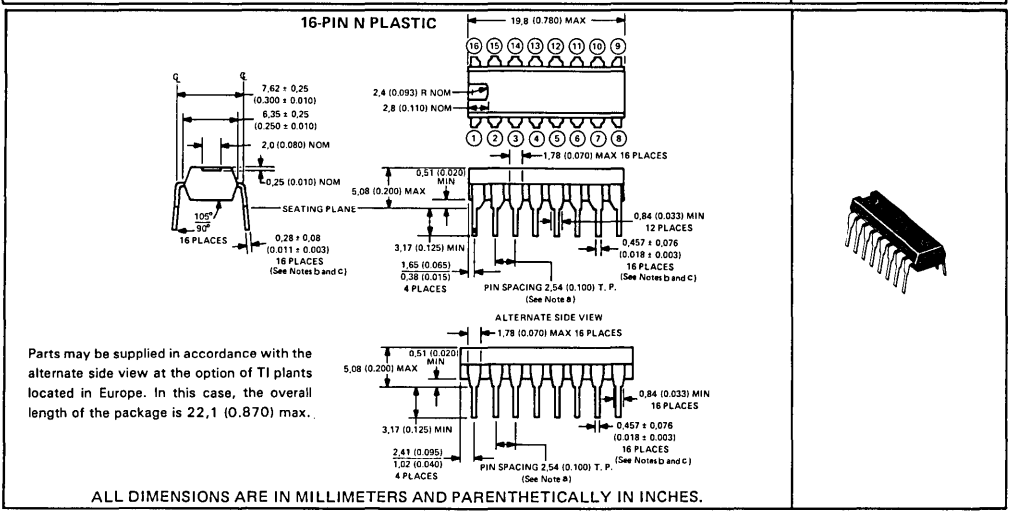
N plastic packages (including NT and NW dual-in-packages)

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300) centers for the NT packages and on 15,24 (0.600) centers for the NW packages. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For the 14-, 16-, 20-, and 28-pin packages, the letter N is used by itself since these packages are available in only one row-spacing width – 7,62 (0.300) for the 14-, 16-, 18-, and 20-pin packages and 15,24 (0.600) for the 28-pin package. For the 24-pin package, if no second letter or row spacing is specified, the package is assumed to have 15,24 (0.600) row spacing.

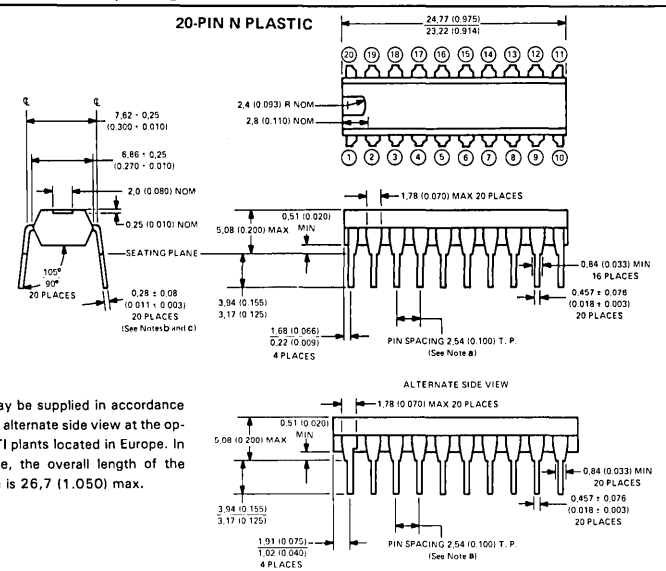


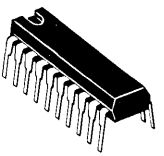


NOTES: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
b. This dimension does not apply for solder-dipped leads.
c. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N plastic dual-in-line packages (continued)

20-PIN N PLASTIC



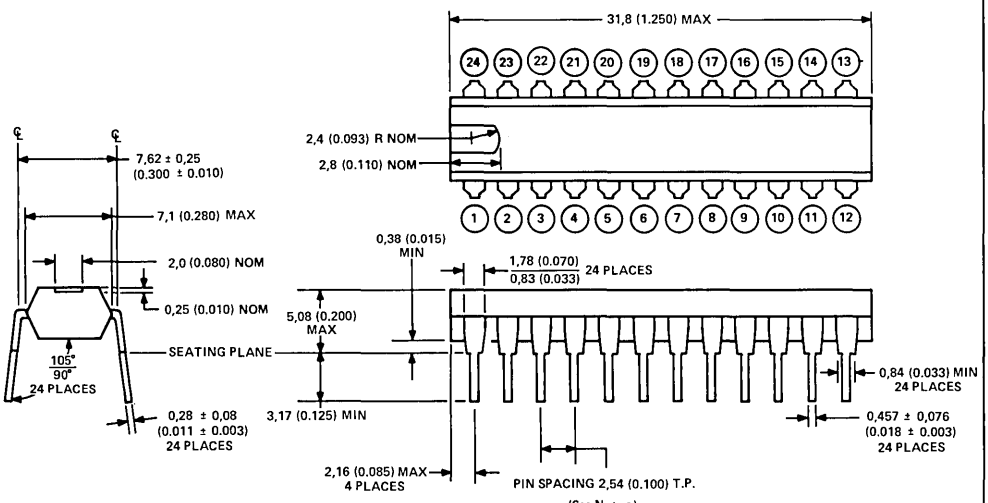


Parts may be supplied in accordance with the alternate side view at the option of TI plants located in Europe. In this case, the overall length of the package is 26,7 (1.050) max.

ALTERNATE SIDE VIEW

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

24-PIN NT PLASTIC, 0.300-INCH ROW SPACING



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTES: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
b. This dimension does not apply for solder-dipped leads.
c. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

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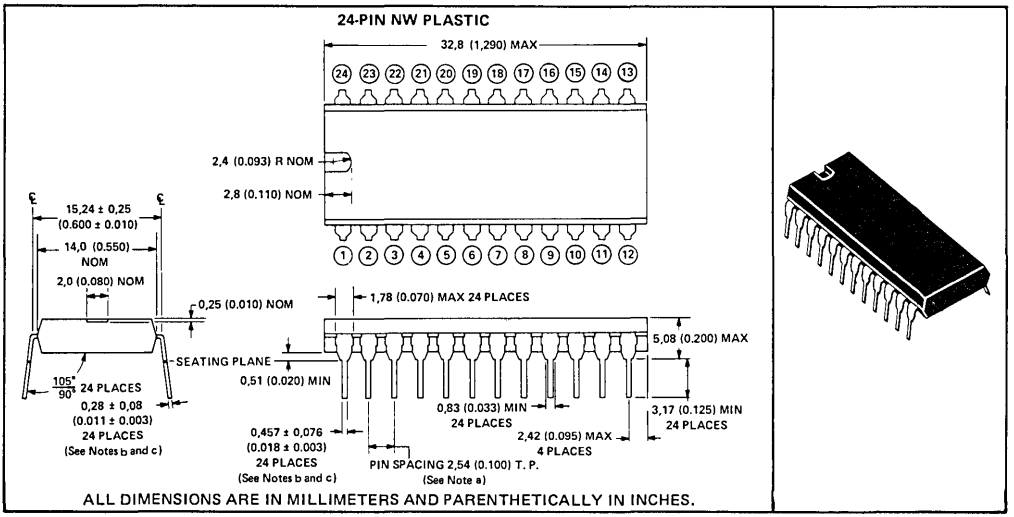
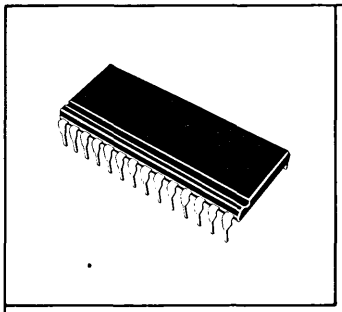
N plastic dual-in-line packages (continued)



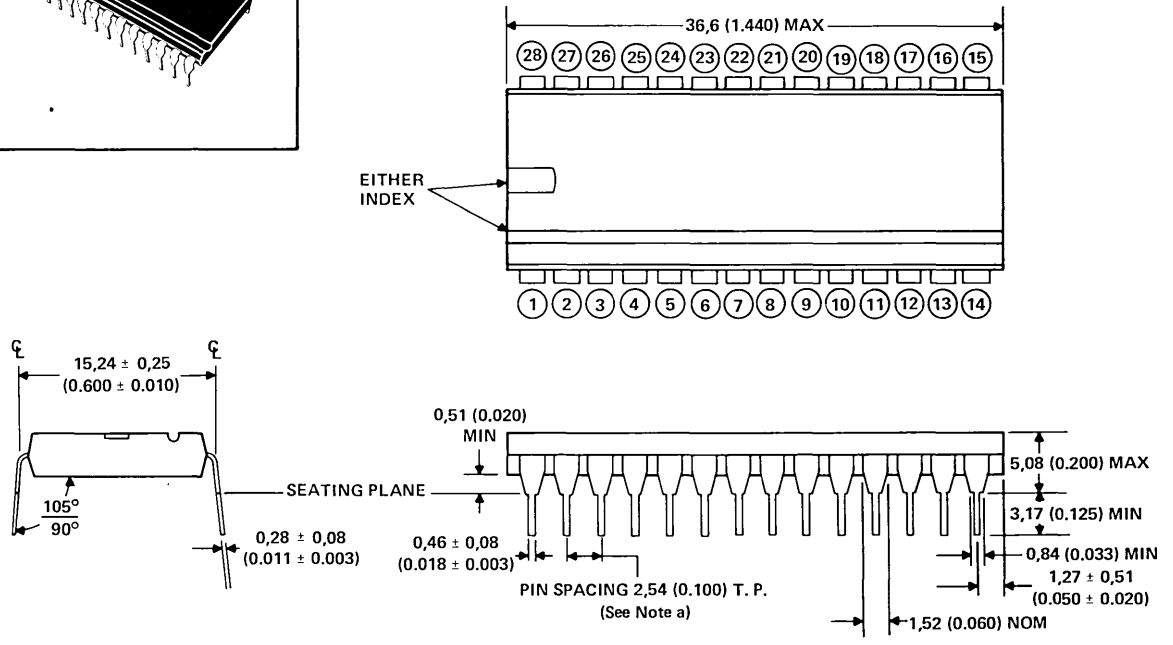
NOTES: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
b. This dimension does not apply for solder-dipped leads.
c. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

8

N plastic packages (continued)



28-PIN N PLASTIC



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

TEXAS INSTRUMENTS
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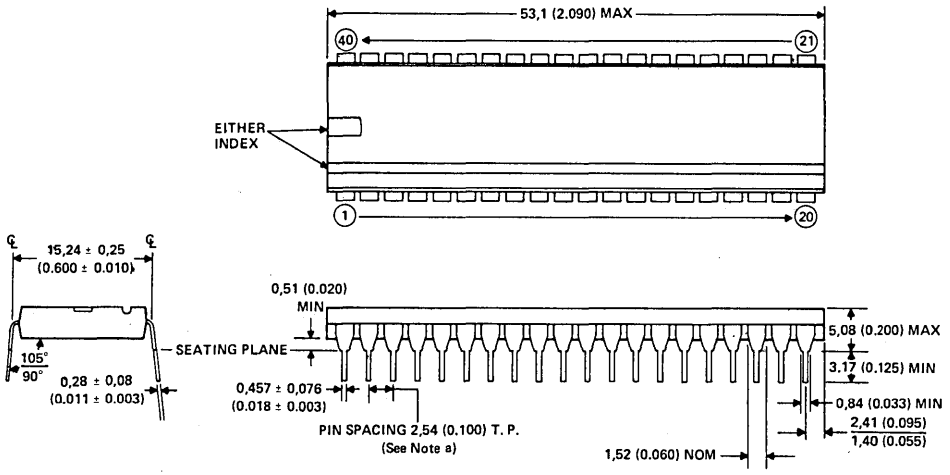
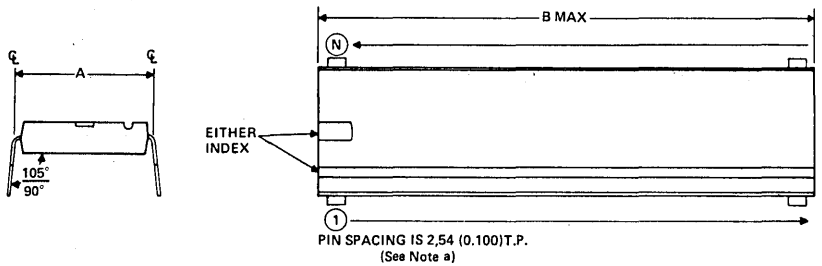
N plastic packages (continued)

40-PIN N PLASTIC



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

48-PIN, 52-PIN, AND 64-PIN N PLASTIC



DIM \ PINS	48	52	64
A ± 0,25 (0.010)	15,24 (0.600)	15,24 (0.600)	22,86 (0.900)
B MAX	62,2 (2.45)	67,3 (2.65)	81,3 (3.20)

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

IC Sockets

IC SOCKETS

Texas Instruments lines of off-the-shelf interconnection products are designed specifically to meet the performance needs of volume commercial applications. They provide both the economy of a standard product line and performance features developed after many year's experience with custom designs. Foremost among these is our ability to selectively bond a wrought gold stripe at the contact point. No waste. Reduced cost. Reliable contacts.

Wrought Gold Contact

Plate a contact with gold and you get a better contact. More reliable, longer lasting. Increase the gold, you improve the contact. But gold is precious, so improved performance has to be costly – right? Wrong. Because now you can get the gold only where it is needed – at the point of contact.

How? With selective metallurgical bonding; a gold stripe inlay. Not porous plating, but durable wrought gold bonded to the contact by the same technology used to produce clad coins and thermostat metals.

Texas Instruments, Attleboro, Massachusetts, is the world's largest producer of these multimetal systems. We also know our way around electronics. The result? A full line of reliable, low cost, interconnection systems featuring an extra measure of gold where it's needed. Premium performance at no premium in price.

IC Sockets

Texas Instruments family of IC sockets includes every type and size in common use today, and as wide a choice of contact materials as you'll find anywhere. Choose from open or closed entry *wire-wrapped*† sockets, standard or low profile solder tail sockets, cable plugs, and component platforms. Sizes from 8 to 40 pins.

Additional information including pricing and delivery quotations may be obtained from your nearest TI Distributor, TI Representative, or:

Texas Instruments Incorporated
Connector Systems Department
MS 14-3
Attleboro, Massachusetts 02703
Telephone: (617) 699-3800
TELEX: ABORA927708

†Registered trademark of Gardner-Denver

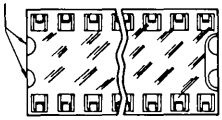
LOW PROFILE SOCKETS

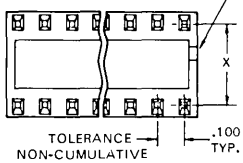
SOLDER TAIL

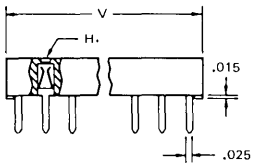
C-93 SERIES GOLD-CLAD CONTACTS

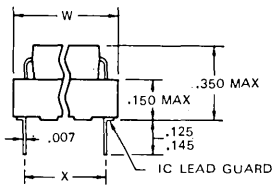
- Universal mounting and packaging
- Anti-wicking wafer
- Stand-off tabs on base for solder flush
- Redundant contact points for low contact resistance, high reliability and repetitive insertion
- Closed entry construction

SOLDER STANDOFF









MATERIAL:

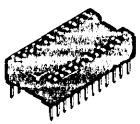
A. Body-glass filled nylon (GFN)
B. Contact-copper nickel alloy
C. Finish-see part number schedule

NOTES:

A. Sockets meet requirements of Texas Instruments test specification TS-0005 and test report TR-0003
B. Operating temperature −65°C to ±150°C
C. Contacts have redundant spring elements
D. Accommodates standard IC leads up to .024" square, rectangular, or .024" diameter
E. Contact is designed and oriented in the plastic body to generate maximum possible contact pressure
F. Socket is designed to achieve maximum density on boards
G. Sockets may be mounted end to end on .100" centers continuous line or on .400" centers row to row
H. Socket is designed to prevent IC leads from contacting P.C. board
I. Closed entry feature provided to facilitate automatic IC insertion and protects the IC leads against damage

	8 Pin	14 Pin	16 Pin	18 Pin	20 Pin	22 Pin	24 Pin	28 Pin	40 Pin
Dimension X ±.005	.300	.300	.300	.300	.300	.400	.600	.600	.600
Dimension V ±.010	.400	.700	.800	.900	1.000	1.100	1.200	1.400	2.000
Dimension W (max)	.400	.400	.400	.400	.400	.500	.700	.700	.700

PART NUMBER SCHEDULE



BLACK BODY

Pins	
8	C9308-02
14	C9314-02
16	C9316-02
18	C9318-02
20	C9320-02
22	C9322-02
24	C9324-02
28	C9328-02
40	C9340-02

CONTACT FINISH
50 microinch minimum gold strip inlay

STANDARD PROFILE SOCKET

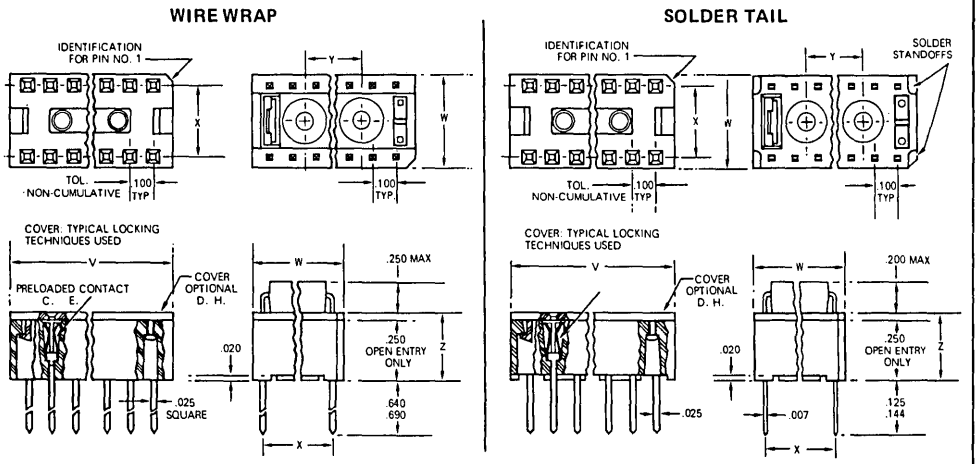
SOLDER TAIL

C-82 SERIES PLATED CONTACTS • C-92 SERIES GOLD CLAD CONTACTS

WIRE WRAP

C-81 SERIES PLATED CONTACTS • C-91 SERIES GOLD CLAD CONTACTS

- Designed for low cost, reliable, high density production packaging
- Universal mounting and packaging capabilities
- 8 to 40 pin lead configurations
- Contacts accommodate .015" through .024" rectangular or round dual-in-line leads
- Wire wrap posts held to true position of .015" providing a true position of .020" on boards for efficient automatic wire wrapping



MATERIAL:

A. Body-glass filled nylon (GFN)
B. Contact-phosphor bronze per QQ-B-750 (C-81) copper nickel alloy (C-91)
C. Finish-see part number schedule

NOTES:

A. Sockets meet requirements of Texas Instruments test specification TS-0003 and test report TR-0001
B. Contacts are replaceable
C. Contacts have redundant spring elements
D. Cover is removeable
E. Contact is designed and oriented in the plastic body to generate maximum possible contact pressure
F. Operating temperature –65°C to +150°C
G. Sockets are designed to achieve maximum density on boards and may be mounted .400" row to row centers
H. Closed entry cover is provided to facilitate automatic insertion and protect IC leads against damage
I. Accommodates standard IC leads up to .024" square, rectangular or .024" dia.
J. Contact retention – 7 lbs. min.
K. Sockets are capable of being automatically or semiautomatically wire wrapped

	8 Pin	14 Pin	16 Pin	18 Pin	20 Pin	24 Pin	28 Pin	36 Pin	40 Pin
Dimension V ±0.10	.465	.765	.865	.965	1.065	1.280	1.480	1.845	2.045
Dimension W (max)	.400	.400	.400	.400	.400	.700	.700	.700	.700
Dimension X ±.005	.300	.300	.300	.300	.300	.600	.600	.600	.600
Dimension Y ±0.10	NA	.400	.400	.400	.400	.500	.500	.800	1.000
Dimension Z ±.005	.280	.280	.280	.280	.280	.280	.280	.325	.325

WIRE WRAP

		OPEN ENTRY	CLOSED ENTRY
PART NUMBER SCHEDULE			
Contact Finish	**Pins**	**Black Body**	**Black Cover**
Series **C-81** 200-400 microinch min tin per MIL-T-10727	8	C810854	C810804
	14	C811454	C811404
	16	C811654	C811604
	18	C811854	C811804
	20	C812054	C812004
	24	C812454	C812404
	28	C812854	C812804
	36		C813604
	40		C814004
Series **C-91** 50 microinch min gold stripe inlay	8	C910850	C910800
	14	C911450	C911400
	16	C911650	C911600
	18	C911850	C911800
	20	C912050	C912000
	24	C912450	C912400
	28	C912850	C912800
	36		C913600
	40		C914000

SOLDER TAIL

		OPEN ENTRY	CLOSED ENTRY
PART NUMBER SCHEDULE			
Contact Finish	**Pins**	**Black Body**	**Black Cover**
Series **C-82** 30 microinch min gold per MIL-G-45204 over 50 microinch min nickel per QQ-N-290	8	C820850	C820800
	14	C821450	C821400
	16	C821650	C821600
	18	C821850	C821800
	24	C822450	C822400
	28	C822850	C822800
	36		C823600
	40		C824000
Series **C-82** 50 microinch min gold per MIL-G-45204 over 100 microinch min nickel per QQ-N-290	8	C820852	C820802
	14	C821452	C821402
	16	C821652	C821602
	18	C821852	C821802
	24	C822452	C822402
	28	C822852	C822802
	36		C823602
	40		C824002
Series **C-82** 200-400 microinch min tin per MIL-T-10727	8	C820854	C820804
	14	C821454	C821404
	16	C821654	C821604
	18	C821854	C821804
	24	C822454	C822404
	28	C822854	C822804
	36		C823604
	40		C824004
Series **C-92** 100-microinch min gold stripe inlay	8	C920850	C920800
	14	C921450	C921400
	16	C921650	C921600
	18	C921850	C921800
	24	C922450	C922400
	28	C922850	C922800
	36		C923600
	40		C924000

SINGLE BEAM SOCKETS

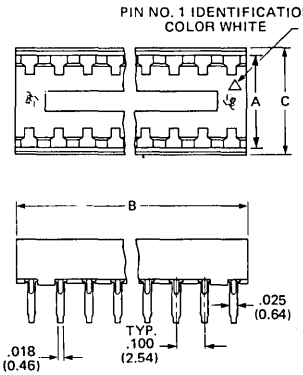
LOW PROFILE/HIGH RETENTION

C87 SERIES BERYLLIUM COPPER CONTACTS

The C87 socket utilizes a beryllium copper contact spring with a 200μ inch minimum tin alloy finish in the contact area. This contact system has been recognized as the standard high performance combination. The system maintains the highest withdrawal and normal forces, along with the ability to retain these properties after cycling.

C88 SERIES PHOSPHOR BRONZE CONTACTS

The C88 socket utilizes a specially processed high-strength copper alloy spring with a 200μ inch minimum tin alloy finish in the contact area. This uniquely engineered contact system has been designed to achieve the performance characteristics that normally require a beryllium copper spring. The device, available at a significantly lower cost than the beryllium copper version, offers the advantage of a substantial cost reduction without sacrificing critical performance requirements.



NOTES:

A. Operating temperature: -40°C to +105°C
B. Contact rating: 1 amp
C. Contact capacitance: 2 picofarads max.
D. Contact resistance: 20 milliohms max.
E. Dielectric withstanding voltage: 1000 V.A.C. min.
F. Insulation resistance: 100,000 megohms min.
G. Insertion force — 16 position "blunt IC" (.010 lead): .5#/lead nominal
H. Withdrawal force (.008 test blade)
   C87 Series
   Initial: 155 gm nominal
   After probing with a .014 blade: 98 gm nominal
   After probing with a .025 blade: 87 gm nominal
   C88 Series
   Initial: 112 gm nominal
   After probing 2 times with .014 blade: 82 gm nominal
   After probing 2 times with .025 blade: 29 gm nominal
I. Normal force (.010 deflection): 250 gm min.
J. Polarization identification: a white circle at the #1 position.
K. Full test reports, #TR 801015 for C87 Series and #TR 810112 for C88 Series, are available from your local sales office.

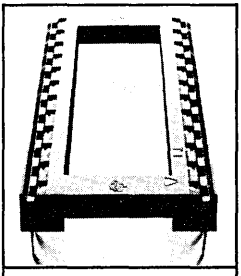
MATERIAL:

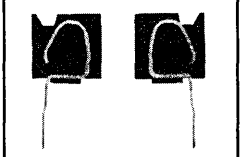
A. Body — Glass reinforced polyester UL rating 94V-0.
*B. Contacts — C87 Series, beryllium copper — C88 Series, phosphor bronze.
C. Contact finish — tin plate: 200μ micro inch min. thick in contact area.

	8 Pin	14 Pin	16 Pin	18 Pin	20 Pin	22 Pin	24 Pin	28 Pin	40 Pin
Dimension A	(7,62) .300	(7,62) .300	(7,62) .300	(7,62) .300	(7,62) .300	(10,16) .400	(15,24) .600	(15,24) .600	(15,24) .600
Dimension B	(10,16) .400	(17,78) .700	(20,32) .800	(22,86) .900	(25,40) 1.000	(27,90) 1.100	(30,48) 1.200	(35,36) 1.400	(50,80) 2.000
Dimension C	(9,40) .370	(9,40) .370	(9,40) .370	(9,40) .370	(9,40) .370	(11,94) .470	(17,02) .670	(17,02) .670	(17,02) .670

*Also available: C98-Gold Inlay, C89-Copper Alloy

PART NUMBER SCHEDULE





Pins	C87 SERIES	C88 SERIES
8	C8708-01	C8808-01
14	C8714-01	C8814-01
16	C8716-01	C8816-01
18	C8718-01	C8818-01
20	C8720-01	C8820-01
22	C8722-01	C8822-01
24	C8724-01	C8824-01
28	C8728-01	C8828-01
40	C8740-01	C8840-01

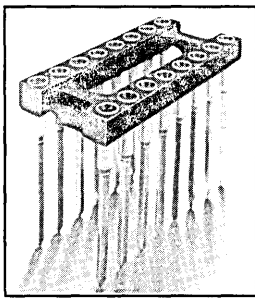
SCREW MACHINE SOCKETS

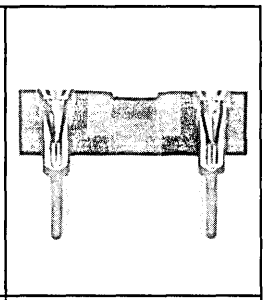
LOW PROFILE

C71 SERIES WIRE WRAP • C72 SERIES SOLDER TAIL

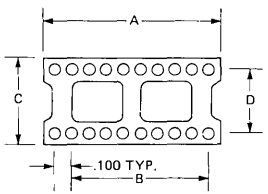
- Gold contacts with gold sleeve or tin sleeve

PART NUMBER SCHEDULE

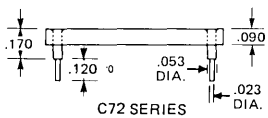




GOLD SLEEVES		
Pins	C71 Wire Wrap	C72 Solder Tail
6	C7106-03*	C7206-09*
8	C7108-03	C7208-09
14	C7114-03	C7214-09
16	C7116-03	C7216-09
18	C7118-03	C7218-09
20	C7120-03	C7220-09
22	C7122-03	C7222-09
24	C7124-03	C7224-09
28	C7128-03	C7228-09
40	C7140-03	C7240-09
64	C7164-03*	C7264-09*
TIN SLEEVES		
6	C7106-53*	C7206-59*
8	C7108-53	C7208-59
14	C7114-53	C7214-59
16	C7116-53	C7216-59
18	C7118-53	C7218-59
20	C7120-53	C7220-59
22	C7122-53	C7222-59
24	C7124-53	C7224-59
28	C7128-53	C7228-59
40	C7140-53	C7240-59
64	C7164-53*	C7264-59*



C71 SERIES



C72 SERIES

MATERIAL:

A. Body — Thermoplastic, meeting UL specification 94-V-O

B. Contact — Beryllium copper QQ-C-530, finish — gold over nickel per mil-G-45204

C. Sleeve — Brass QQ-B-626, finish — gold over nickel per mil-G-45204 or tin over nickel per mil-T-10727

NOTES:

A. Open body construction and high standoffs provide improved cleaning and heat dissipation

B. Accept standard I.C. leads .010± .003 x .018± .003 or .010 to .022 dia.

C. Accept I.C. lead lengths from .090 to .155

D. Operating temperatures:
Gold sleeve -65°C to 125°C
Tin sleeve -40°C to 100°C

E. Performance — meets req. of T.I. test spec. T.S. 0008 as shown in test report T.R. 1021.

	6 Pin	8 Pin	14 Pin	16 Pin	18 Pin	20 Pin	22 Pin	24 Pin	28 Pin	36 Pin	40 Pin	64 Pin
Dimension A max.	.300	.400	.700	.800	.900	1.000	1.100	1.200	1.400	1.800	2.000	3.200
Dimension B ±.005	.200	.300	.600	.700	.800	.900	1.000	1.100	1.300	1.700	1.900	3.100
Dimension C max.	.400	.400	.400	.400	.400	.400	.500	.700	.700	.700	.700	1.000
Dimension D ±.005	.300	.300	.300	.300	.300	.300	.400	.600	.600	.600	.600	.900

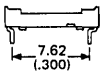
Note: Contacts for one- and two-level wire wrapping are also available. Contact the factory for details.

*Minimum order requirements on these parts. Alternate insulator materials may be used.

SPECIAL SOCKETS

SLIM PACKAGE

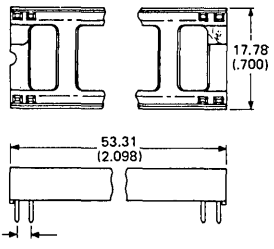
C8424-03 • C9324-03



.300 row to row spacing on the low profile edgegrip

42 POSITION

C4742-11



MATERIAL:

A. Body: 94V-0 glass filled polyester

B. Contact: Copper alloy

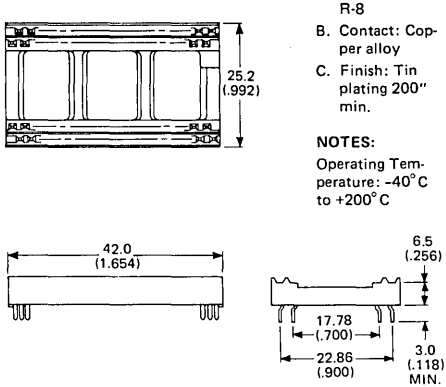
C. Finish: Tin plating: 120" min.

NOTES:

A. Operating temperature: -40°C to +100°C

QUAD PACKAGE

C4W64-11 SERIES 64 STAGGERED PINS



MATERIAL:

A. Body: Ryton R-8

B. Contact: Copper alloy

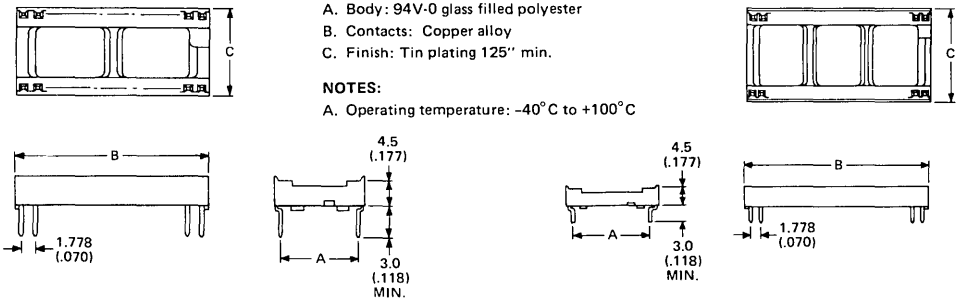
C. Finish: Tin plating 200" min.

NOTES:

Operating Temperature: -40°C to +200°C

SHRINK PACKAGE

C4S SERIES 28 AND 40 POSITIONS



MATERIALS:

A. Body: 94V-0 glass filled polyester

B. Contacts: Copper alloy

C. Finish: Tin plating 125" min.

NOTES:

A. Operating temperature: -40°C to +100°C

Part No.	Pos.	A	B	C
C4S28-02	28	10.16 (.400)	25.0 (.984)	13.0 (.512)
C4S40-02	40	15.24 (.600)	35.7 (1.406)	18.0 (.709)

TI Sales Offices

ALABAMA: Huntsville, 500 Wynn Drive, Suite 514, Huntsville, AL 35805, (205) 837-7530.

ARIZONA: Phoenix, P.O. Box 35160, 8102 N. 23rd Ave., Suite A, Phoenix, AZ 85021, (602) 995-1007.

CALIFORNIA: El Segundo, 831 S. Douglas St., El Segundo, CA 90245, (213) 973-2571; **Irvine,** 17891 Cartwright Rd., Irvine, CA 92714, (714) 660-1200; **Sacramento,** 1900 Point West Way, Suite 171, Sacramento, CA 95815, (916) 929-1521; **San Diego,** 4333 View Ridge Ave., Suite B., San Diego, CA 92123, (714) 278-9600; **Santa Clara,** 5353 Betsy Ross Dr., Santa Clara, CA 95054, (408) 980-9000; **Woodland Hills,** 21220 Erwin St., Woodland Hills, CA 91367, (213) 704-7759.

COLORADO: Denver, 9725 E. Hampden St., Suite 301, Denver, CO 80231, (303) 695-2800.

CONNECTICUT: Wallingford, 9 Barnes Industrial Park Rd., Barnes Industrial Park, Wallingford, CT 06492, (203) 269-0074.

FLORIDA: Clearwater, 2280 U.S. Hwy. 19 N., Suite 232, Clearwater, FL 33515, (813) 796-1926; **Ft. Lauderdale,** 2765 N.W. 62nd St., Ft. Lauderdale, FL 33309, (305) 973-8502; **Maitland,** 2601 Maitland Center Parkway, Maitland, FL 32751, (305) 646-9600.

GEORGIA: Atlanta, 3300 Northeast Expy., Building 9, Atlanta, GA 30341, (404) 452-4600.

ILLINOIS: Arlington Heights, 515 W. Algonquin, Arlington Heights, IL 60005, (312) 640-2934.

INDIANA: Ft. Wayne, 2020 Inwood Dr., Ft. Wayne, IN 46805, (219) 424-5174; **Indianapolis,** 2346 S. Lynhurst, Suite J-400, Indianapolis, IN 46241, (317) 248-8555.

IOWA: Cedar Rapids, 373 Collins Rd. NE, Suite 200, Cedar Rapids, IA 52402, (319) 395-9550.

MARYLAND: Baltimore, 1 Rutherford Pl., 7133 Rutherford Rd., Baltimore, MD 21207, (301) 944-8600.

MASSACHUSETTS: Waltham, 504 Totten Pond Rd., Waltham, MA 02154, (617) 890-7400.

MICHIGAN: Farmington Hills, 33737 W. 12 Mile Rd., Farmington Hills, MI 48018, (313) 553-1500.

MINNESOTA: Edina, 7625 Parklawn, Edina, MN 55435, (612) 830-1600.

MISSOURI: Kansas City, 8080 Ward Pkwy., Kansas City, MO 64114, (816) 523-2500; **St. Louis,** 11861 Westline Industrial Drive, St. Louis, MO 63141, (314) 569-7600.

NEW JERSEY: Clark, 292 Terminal Ave. West, Clark, NJ 07066, (201) 574-9800.

NEW MEXICO: Albuquerque, 5907 Alice NSE, Suite E., Albuquerque, NM 87110, (505) 265-8491.

NEW YORK: East Syracuse, 6700 Old Collamer Rd., East Syracuse, NY 13057, (315) 463-9291; **Endicott,** 112 Nanticoke Ave., P.O. Box 618, Endicott, NY 13760, (607) 754-3900; **Melville,** 1 Huntington Quadrangle, Suite 3C10, P.O. Box 2936, Melville, NY 11747, (516) 454-6600; **Poughkeepsie,** 201 South Ave., Poughkeepsie, NY 12601, (914) 473-2900; **Rochester,** 1210 Jefferson Rd., Rochester, NY 14623, (716) 424-5400.

NORTH CAROLINA: Charlotte, 8 Woodlawn Green, Woodlawn Rd., Charlotte, NC 28210, (704) 527-0930; **Raleigh,** 3000 Highwoods Blvd., Suite 118, Raleigh, NC 27625, (919) 876-2725.

OHIO: Beachwood, 23408 Commerce Park Rd., Beachwood, OH 44122, (216) 464-6100; **Dayton,** Kingsley Bldg., 4124 Linden Ave., Dayton, OH 45432, (513) 258-3877.

OKLAHOMA: Tulsa, 3105 E. Skelly Dr., Suite 110, Tulsa, OK 74105, (918) 749-9547.

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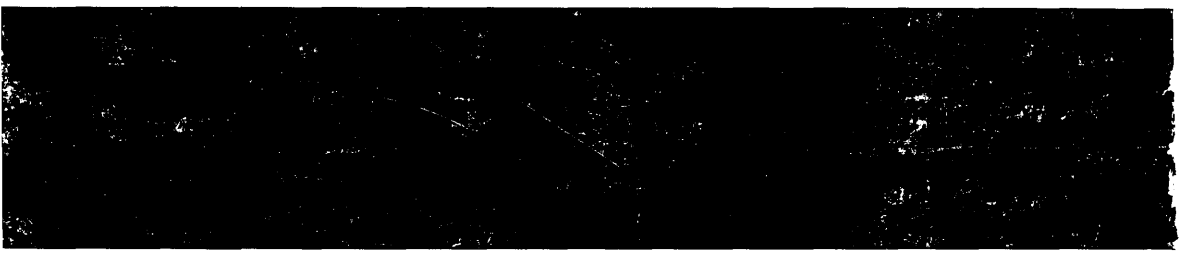

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