Radiation Hardened Circuits

10

Series RSN 54L Radiation Hardened Low Power TTL Now Available

RSN54L00 – Quadruple 2-Input Positive-NAND Gate
RSN54L10 – Triple 3-Input Positive-NAND Gate
RSN54L20 – Dual 4-Input Positive-NAND Gate
RSN54L57 – 3-3-3-2 AND-OR-INVERT Gate
RSN54L71 – R-S Master-Slave Flip-Flop
RSN54L72 – J-K Master-Slave Flip-Flop
RSN54L74 – Dual D-Type Edge-Triggered Flip-Flop
RSN54L122 – Retriggerable Monostable Multivibrator with Clear
RSN54L130 – Dual 3-Input Positive-NAND Gate
RSN54L131 – Dual Expandable 3-Input Positive-NAND Gate

Also Available From Texas Instruments:

Radiation Hardened Series 54, Series 54H, Linear Circuits And Diode Arrays.

INDEX

RSN SERIES
RADIATION-HARDENED INTEGRATED CIRCUITS

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SERIES RSN54 AND SERIES RSN54H
RADIATION-HARDENED TTL INTEGRATED CIRCUITS

SERIES RSN54 AND RSN54H
BULLETIN NO. DL-S 7111463, MARCH 1971

TTL INTEGRATED CIRCUITS WITH HIGH TOLERANCE
TO GAMMA AND NEUTRON IRRADIATION

- High Speed: Typical Gate Propagation Delay Times (C_L = 50 pF):
  Series RSN54 . . . 10 ns
  Series RSN54H . . . 7.5 ns
- High D-C Noise Margin . . . 1 Volt Typical
- Low Output Impedance Provides Low A-C Noise Susceptibility
- Waveform Integrity Maintained over Full Range of Loading and Temperature Conditions
- Normalized Fan-Out to Ten Loads
- Typical NAND Gate Power Dissipation at 50% Duty Cycle:
  Series RSN54 . . . 10 mW
  Series RSN54H . . . 23 mW

description

Series RSN54 and Series RSN54H TTL integrated circuits are specifically designed and fabricated for operation and survivability in nuclear-radiation environments. The basic Series 54/74 configuration, desirable for its "natural" hardness, has been coupled with a state-of-the-art circuit-hardening process. This technology, compatible for use in high-volume production, employs:

- dielectric isolation
- thin-film resistors
- small transistor geometries
- shallow base diffusions
- heavy gold doping
- minimum collector thickness and resistivity
- aluminum interconnection system

Series RSN54, RSN54H, and RSN54L logic families are completely compatible with one another and with most other TTL and DTL circuits. These circuits are designed to operate at the same supply voltages and logic levels with the high d-c noise margins which are characteristic of Texas Instruments Series 54/74 circuits. These families of radiation-hardened circuits include the gates and flip-flops needed to perform functions within present-day digital electronic systems. And, since these three families are compatible with one another, Series RSN54H high-speed circuits may be selectively used in system locations requiring minimal propagation delay times. In other locations where speed is not the limiting parameter, Series RSN54 or RSN54L circuits may be used.

Both Series RSN54 and Series RSN54H are designed for operation over the full military temperature range of −55°C to 125°C.

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CONTENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1)	7 V
Input voltage (See Note 1)	5.5 V
Operating free-air temperature range	−55°C to 125°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

input-current requirements

Input-current requirements reflect worst-case conditions for T_A = −55°C to 125°C and V_{CC} = 4.5 V to 5.5 V. Currents into the input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

a. Each input of the Series RSN54 multiple-emitter input transistors requires no more than a 1.6-mA flow out of the input at a low voltage level; therefore one normalized load (N = 1) is −1.6 mA maximum. Each input requires current into the input at a high voltage level. This current is 40 μA maximum (one normalized load) for each emitter input.

b. Each input of the Series RSN54H multiple-emitter input transistors requires no more than a 2-mA flow out of the input at a low voltage level; therefore, one normalized load (N = 1) is −2 mA maximum. Each input requires current into the input at a high voltage level. This current is 50 μA maximum (one normalized load) for each emitter input.

fan-out capability

Fan-out (N) reflects the ability of an output to sink current from a number of Series RSN54 or RSN54H loads at a low voltage level and to supply current at a high voltage level. Each output is capable of sinking current or supplying current to 10 normalized loads (N = 10) within the same series. In addition, Series RSN54H outputs will drive twelve Series RSN54 loads, or Series RSN54 outputs will drive eight Series RSN54H loads. Currents out of the output terminal are specified as negative values.

unused inputs

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For optimum switching times and minimum noise susceptibility, unused inputs should be maintained at a positive voltage greater than 2.4 V but not to exceed the absolute maximum rating of 5.5 V. This eliminates the distributed capacitance associated with the floating-input-transistor emitter, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times. Some possible ways of handling input emitters are:

a. Connect unused inputs to an independent supply voltage. Preferably, this voltage should be between 2.4 V and 3.5 V.

b. Connect unused inputs to a used input if maximum fan-out of the driving output will not be exceeded. Each input presents a full load to the driving output at a high-level voltage but adds no loading at a low-level voltage.

c. Connect unused inputs to V_{CC} through a 1-kΩ resistor so that if a transient which exceeds the 5.5-V maximum rating should occur, the impedance will be high enough to protect the input. One-to-25 unused inputs may be connected to each 1-kΩ resistor.

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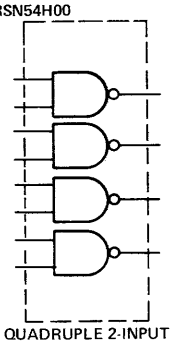
standard line summary

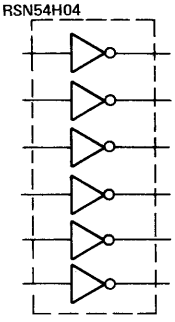
GATE CIRCUITS

RSN5400
RSN54H00



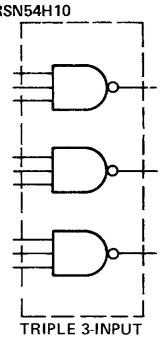
QUADRUPLE 2-INPUT
POSITIVE-NAND GATES

RSN5404
RSN54H04



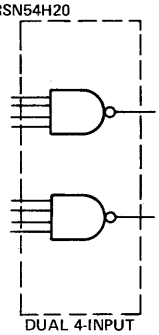
HEX INVERTERS

RSN5410
RSN54H10



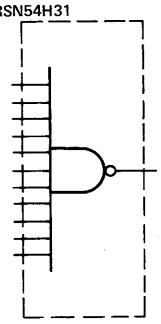
TRIPLE 3-INPUT
POSITIVE-NAND GATES

RSN5420
RSN54H20



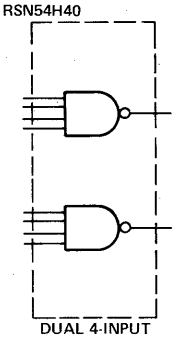
DUAL 4-INPUT
POSITIVE-NAND GATES

RSN5431
RSN54H31



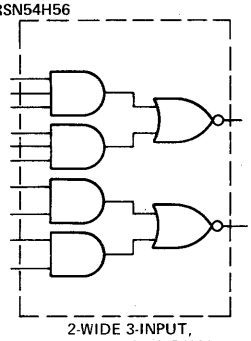
11-INPUT
POSITIVE-NAND GATES

RSN5440
RSN54H40



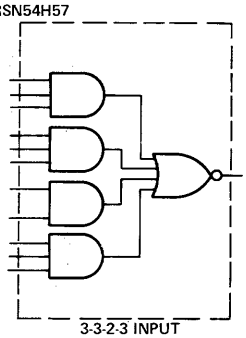
DUAL 4-INPUT
POSITIVE-NAND BUFFERS

RSN5456
RSN54H56



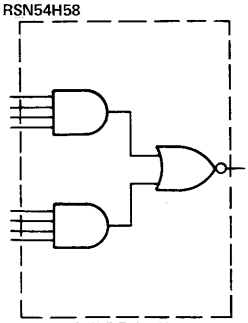
2-WIDE 3-INPUT,
2-WIDE 2-INPUT, DUAL
AND-OR-INVERT GATES

RSN5457
RSN54H57



3-3-2-3 INPUT
AND-OR-INVERT GATES

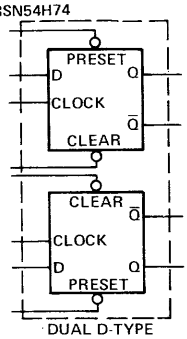
RSN5458
RSN54H58



2-WIDE 4 INPUT
AND-OR-INVERT GATES

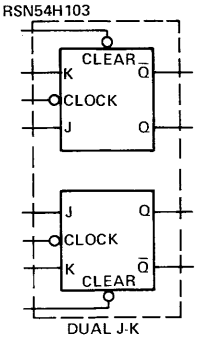
FLIP-FLOP CIRCUITS

RSN5474
RSN54H74



DUAL D-TYPE
EDGE-TRIGGERED FLIP-FLOPS

RSN54H103



DUAL J-K
EDGE-TRIGGERED FLIP-FLOP

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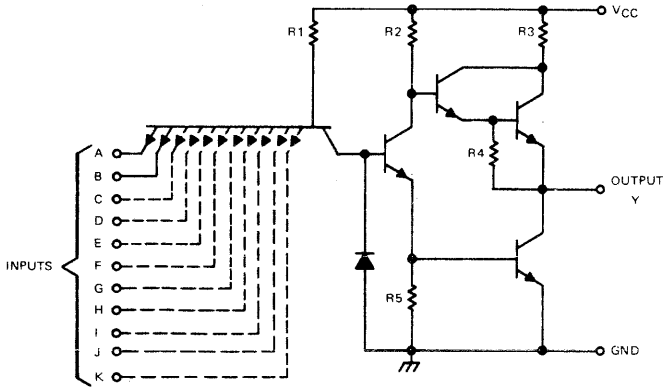
CIRCUIT TYPES RSN5400, RSN5410, RSN5420, RSN5431, RSN54H00, RSN54H10, RSN54H20, RSN54H31 POSITIVE-NAND GATES

schematic (each NAND gate)



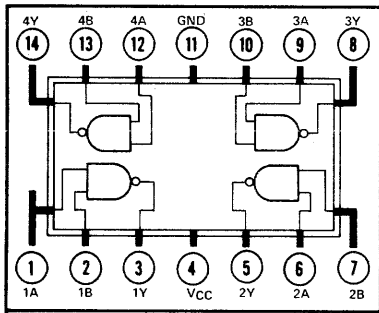
NOMINAL RESISTOR VALUES

RESISTOR	RSN5400 RSN5410 RSN5420 RSN5431	RSN54H00 RSN54H10 RSN54H20 RSN54H31
R1	4 kΩ	2.8 kΩ
R2	1.6 kΩ	760 Ω
R3	58 Ω	58 Ω
R4	1 kΩ	1 kΩ
R5	1 kΩ	470 Ω

logic

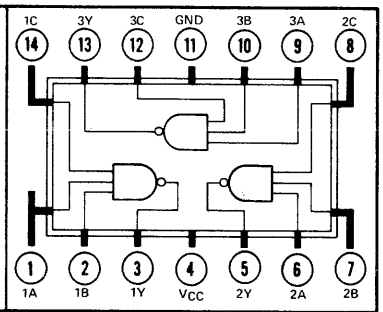
H FLAT PACKAGE (TOP VIEWS)

RSN5400, RSN54H00



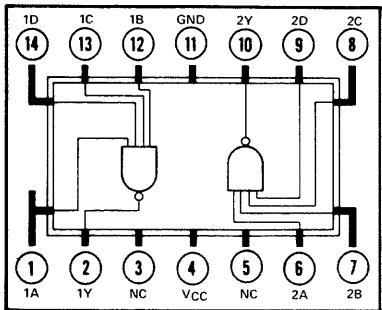
positive logic: $Y = \overline{AB}$

RSN5410, RSN54H10



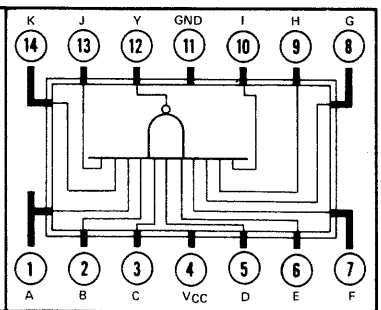
positive logic: $Y = \overline{ABC}$

RSN5420, RSN54H20



positive logic: $Y = \overline{ABCD}$

RSN5431, RSN54H31



positive logic: $Y = \overline{ABCDEFGHIJK}$

NC—No internal connection

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recommended operating conditions

	RSN5400 RSN5410 RSN5420 RSN5431			RSN54H00 RSN54H10 RSN54H20 RSN54H31			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
Normalized fan-out from each gate, N			10			10	
High-level output current, I_{OH}			−400			−500	μA
Low-level output current, I_{OL}			16			20	mA
Operating free-air temperature, T_A	−55		125	−55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	RSN5400 RSN5410 RSN5420 RSN5431		RSN54H00 RSN54H10 RSN54H20 RSN54H31		UNIT
				MIN	MAX	MIN	MAX	
V_{IH}	High-level input voltage	1		2		2		V
V_{IL}	Low-level input voltage	2			0.8		0.8	V
V_{OH}	High-level output voltage	2	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = MAX	2.4		2.4		V
V_{OL}	Low-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = MAX		0.4		0.4	V
I_I	Input current at maximum input voltage	3	V_{CC} = MAX, V_I = 5.5 V		1		1	mA
I_{IH}	High-level input current	3	V_{CC} = MAX, V_I = 2.4 V		40		50	μA
I_{IL}	Low-level input current	4	V_{CC} = MAX, V_I = 0.4 V		−1.6		−2	mA
I_{OS}	Short-circuit output current‡	5	V_{CC} = MAX	−40	−120	−40	−120	mA
I_{CCH}	Supply current, high-level output (average per gate)	6	V_{CC} = MAX, V_I = 0		1.75		2.5	mA
I_{CCL}	Supply current, low-level output (average per gate)	6	V_{CC} = MAX, V_I = 4.5 V		5.7		10.8	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡Not more than one output should be shorted at a time, and the duration of the short circuit test should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	RSN5400 RSN5410 RSN5420		RSN5431		RSN54H00 RSN54H10 RSN54H20		RSN54H31		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	29	C_L = 50 pF		18		18		12		12	ns
t_{PHL}	Propagation delay time, high-to-low-level output	29	C_L = 50 pF		15		25		12		20	ns

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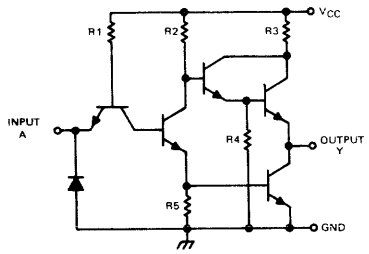
CIRCUIT TYPES RSN5404, RSN54H04
HEX INVERTERS

schematic (each inverter)

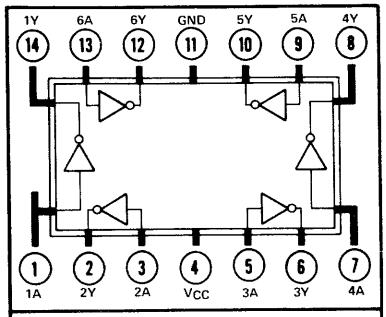


NOMINAL RESISTOR VALUES

RESISTOR	RSN5404	RSN54H04
R1	4 kΩ	2.8 kΩ
R2	1.6 kΩ	850 Ω
R3	58 Ω	58 Ω
R4	4 kΩ	4 kΩ
R5	1 kΩ	500 Ω

logic

H FLAT PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A}$

recommended operating conditions

	RSN5404			RSN54H04			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
Normalized fan-out from each output, N			10			10	
High-level output current, I_{OH}			−400			−500	μA
Low-level output current, I_{OL}			16			20	mA
Operating free-air temperature, T_A	−55		125	−55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	RSN5404		RSN54H04		UNIT
				MIN	MAX	MIN	MAX	
V_{IH}	High-level input voltage	7		2		2		V
V_{IL}	Low-level input voltage	8			0.8		0.8	V
V_{OH}	High-level output voltage	8	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = MAX	2.4		2.4		V
V_{OL}	Low-level output voltage	7	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = MAX		0.4		0.4	V
I_I	Input current at maximum input voltage	9	V_{CC} = MAX, V_I = 5.5 V		1		1	mA
I_{IH}	High-level input current	9	V_{CC} = MAX, V_I = 2.4 V		40		50	μA
I_{IL}	Low-level input current	10	V_{CC} = MAX, V_I = 0.4 V		−1.6		−2	mA
I_{OS}	Short-circuit output current‡	11	V_{CC} = MAX	−40	−120	−40	−120	mA
I_{CCH}	Supply current, high-level output (average per inverter)	12	V_{CC} = MAX, V_I = 0		3.2		3.8	mA
I_{CCL}	Supply current, low-level output (average per inverter)	12	V_{CC} = MAX, V_I = 4.5 V		5.6		9.7	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ Not more than one output should be shorted at a time, and the duration of the short-circuit test should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	RSN5404		RSN54H04		UNIT
				MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	29	C_L = 50 pF		18		12	ns
t_{PHL}	Propagation delay time, high-to-low-level output	29	C_L = 50 pF		15		12	ns

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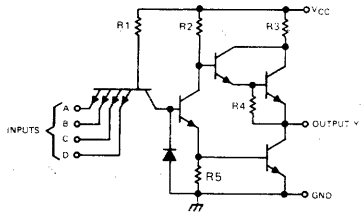
schematic (each NAND buffer)

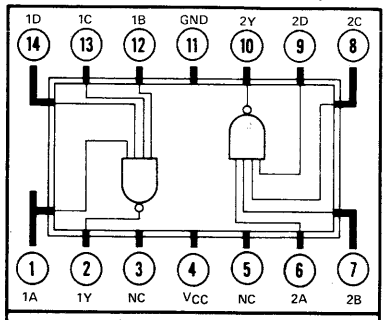


NOMINAL RESISTOR VALUES

RESISTOR	RSN5440	RSN54H40
R1	4 kΩ	1.4 kΩ
R2	600 Ω	390 Ω
R3	45 Ω	45 Ω
R4	1 kΩ	1 kΩ
R5	400 Ω	250 Ω

logic

H FLAT PACKAGE (TOP VIEW)



positive logic: $Y = \overline{ABCD}$

NC—No internal connection

recommended operating conditions

	RSN5440			RSN54H40			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
Normalized fan-out from each gate, N			30			30	
High-level output current, I_{OH}			−1.5			−3	mA
Low-level output current, I_{OL}			48			60	mA
Operating free-air temperature, T_A	−55		125	−55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	RSN5440		RSN54H40		UNIT
				MIN	MAX	MIN	MAX	
V_{IH}	High-level input voltage	1		2		2		V
V_{IL}	Low-level input voltage	2			0.8		0.8	V
V_{OH}	High-level output voltage	2	V_{CC} = MIN, V_{OL} = 0.8 V, I_{OH} = MAX	2.4		2.4		V
V_{OL}	Low-level output voltage	1	V_{CC} = MIN, V_{OH} = 2 V, I_{OL} = MAX		0.4		0.4	V
I_I	Input current at maximum input voltage	3	V_{CC} = MAX, V_I = 5.5 V		1		1	mA
I_{IH}	High-level input current	3	V_{CC} = MAX, V_I = 2.4 V		50		100	μA
I_{IL}	Low-level input current	4	V_{CC} = MAX, V_I = 0.4 V		−1.6		−4	mA
I_{OS}	Short-circuit output current‡	5	V_{CC} = MAX	−40	−125	−40	−125	mA
I_{CCH}	Supply current, high-level output (average per gate)	6	V_{CC} = MAX, V_I = 0		1.75		5	mA
I_{CCL}	Supply current, low-level output (average per gate)	6	V_{CC} = MAX, V_I = 4.5 V		12.6		21	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡Not more than one output should be shorted at a time, and the duration of the short-circuit test should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	RSN5440		RSN54H40		UNIT
				MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	29	C_L = 50 pF		18		12	ns
t_{PHL}	Propagation delay time, high-to-low-level output	29	C_L = 50 pF		15		12	ns

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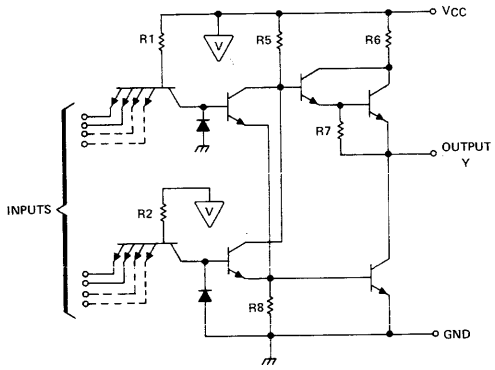
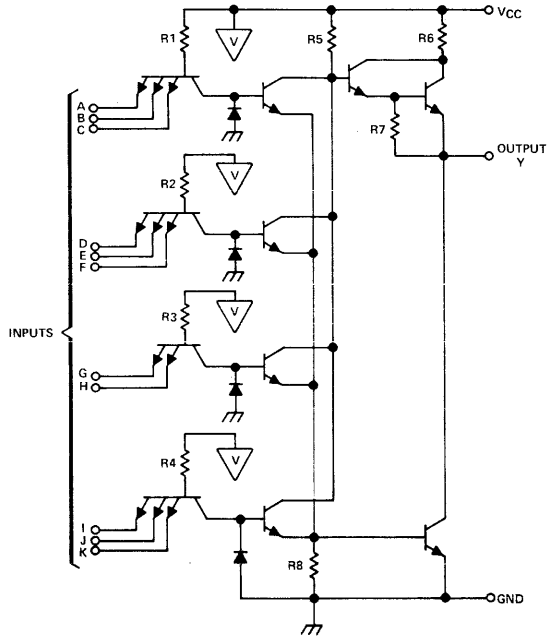
CIRCUIT TYPES RSN5456, RSN5457, RSN5458, RSN54H56, RSN54H57, RSN54H58 POSITIVE AND-OR-INVERT GATES

schematics

RSN5456, RSN5458, RSN54H56, RSN54H58



RSN5457, RSN54H57



NOMINAL RESISTOR VALUES

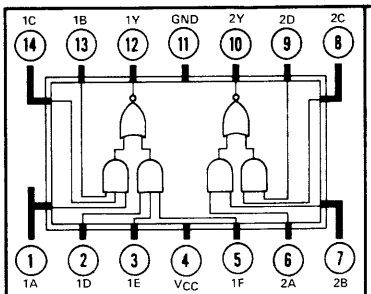
RESISTOR	RSN5456 RSN5457 RSN5458	RSN54H56 RSN54H57 RSN54H58
R1, R2, R3, R4,	4 kΩ	2.8 kΩ
R5	1.6 kΩ	760 Ω
R6	58 Ω	58 Ω
R7	1 kΩ	1 kΩ
R8	1 kΩ	470 Ω

▽ . . . V_{CC} bus

logic

H FLAT PACKAGE (TOP VIEWS)

RSN5456, RSN54H56

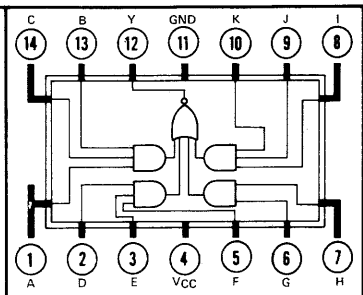


positive logic:

$1Y = \overline{(1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)}$

$2Y = \overline{(2A \cdot 2B) + (2C \cdot 2D)}$

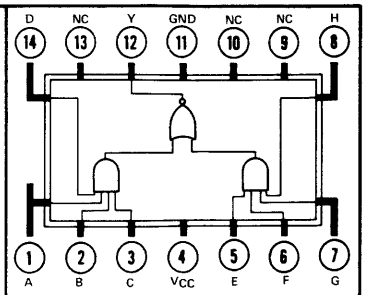
RSN5457, RSN54H57



positive logic:

$Y = \overline{(ABC) + (DEF) + (GH) + (IJK)}$

RSN5458, RSN54H58



positive logic:

$Y = \overline{(ABCD) + (EFGH)}$

NC—No internal connection

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recommended operating conditions

	SERIES RSN54			SERIES RSN54H			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
Normalized fan-out from each output, N			10			10	
High-level output current, I_{OH}			−400			−500	μA
Low-level output current, I_{OL}			16			20	mA
Operating free-air temperature, T_A	−55		125	−55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SERIES RSN54		SERIES RSN54H		UNIT
					MIN	MAX	MIN	MAX	
V_{IH}	High-level input voltage	13			2		2		V
V_{IL}	Low-level input voltage	14				0.8		0.8	V
V_{OH}	High-level output voltage	14	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = MAX		2.4		2.4		V
V_{OL}	Low-level output voltage	13	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = MAX			0.4		0.4	V
I_I	Input current at maximum input voltage	15	V_{CC} = MAX, V_I = 5.5 V			1		1	mA
I_{IH}	High-level input current	15	V_{CC} = MAX, V_I = 2.4 V			40		50	μA
I_{IL}	Low-level input current	16	V_{CC} = MAX, V_I = 0.4 V			−1.6		−2	mA
I_{OS}	Short-circuit output current‡	17	V_{CC} = MAX		−40	−120	−40	−120	mA
I_{CCH}	Supply current, high-level output	18	V_{CC} = MAX, V_I = 0	RSN5456		7			mA
				RSN5457		7			
				RSN5458		3.5			
				RSN54H56				10	
				RSN54H57				10	
				RSN54H58				5	
I_{CCL}	Supply current, low-level output	18	V_{CC} = MAX, V_I = 4.5 V	RSN5456		14			mA
				RSN5457		10			
				RSN5458		7			
				RSN54H56				25	
				RSN54H57				16	
				RSN54H58				13	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

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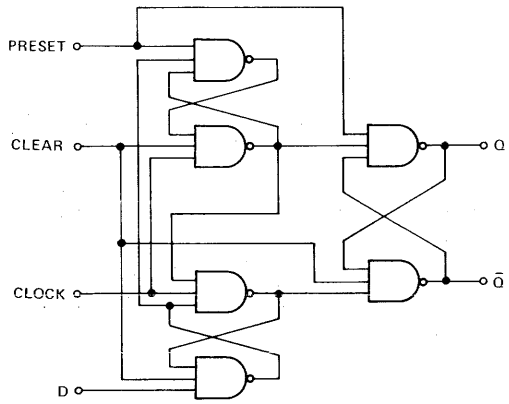
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	SERIES RSN54		SERIES RSN54H		UNIT
				MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	29	C_L = 50 pF		20		15	ns
t_{PHL}	Propagation delay time high-to-low-level output	29	C_L = 50 pF		15		12	ns

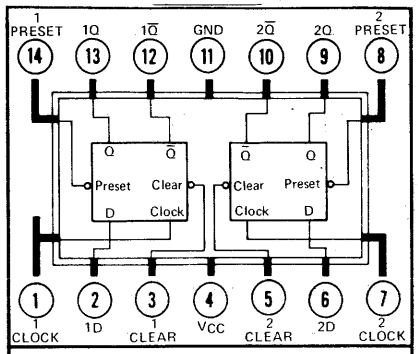
CIRCUIT TYPES RSN5474, RSN54H74
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

functional block diagram (each flip-flop)



logic

H FLAT PACKAGE (TOP VIEW)



positive logic:
Low input to preset sets Q to high level
Low input to clear resets Q to low level
Preset and clear are independent of clock

TRUTH TABLE
(Each Flip-Flop)

t_n	t_{n+1}	
INPUT	OUTPUT	
D	Q	Q̄
L	L	H
H	H	L

H = high level, L = low level
t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse

description

These monolithic, high-speed, dual, edge-triggered flip-flops utilize TTL circuitry to perform D-type flip-flop logic. Each flip-flop has individual clear and preset inputs, and also complementary Q and Q̄ outputs.

Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect.

recommended operating conditions

	RSN5474			RSN54H74			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
Normalized fan-out from each output, N			10			10	
High-level output current, I_{OH}			−400			−500	μA
Low-level output current, I_{OL}	0		16	0		20	mA
Clock frequency, f_{clock}			20			30	MHz
Width of clock pulse, $t_{w(clock)}$ (see Figure 30 or 31)	30			20			ns
Width of preset pulse, $t_{w(preset)}$ (see Figure 32)	30			20			ns
Width of clear pulse, $t_{w(clear)}$ (see Figure 32)	30			20			ns
Input setup time, t_{setup} (see Note 1 and Figures 30 and 31)	20			15			ns
Input hold time, t_{hold} (see Note 2 and Figures 30 and 31)	5			0			ns
Operating free-air temperature, T_A	−55		125	−55		125	°C

NOTES: 1. Setup time is the interval immediately preceding the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
2. Hold time is the interval immediately following the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS†	RSN5474 MIN	RSN5474 MAX	RSN54H74 MIN	RSN54H74 MAX	UNIT
V_{IH}	High-level input voltage		19 and 20		2		2		V
V_{IL}	Low-level input voltage		19 and 20			0.8		0.8	V
V_{OH}	High-level output voltage		19	V_{CC} = MIN, I_{OH} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V	2.4		2.4		V
V_{OL}	Low-level output voltage		20	V_{CC} = MIN I_{OL} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V		0.4		0.4	V
I_I	input current at maximum input voltage		21	V_{CC} = MAX, V_I = 5.5 V		1		1	mA
I_{IH}	High-level input current	D input	21	V_{CC} = MAX, V_I = 2.4 V		40		50	μA
		preset or clock				80		100	
		clear				120		150	
I_{IL}	Low-level input current	preset or D	21	V_{CC} = MAX, V_I = 0.4 V		−1.6		−2	mA
		clock or clear				−3.2		−4	
I_{OS}	Short-circuit output current‡		22	V_{CC} = MAX	−40	−120	−40	−120	mA
I_{CC}	Supply current		23	V_{CC} = 5 V,		28		45	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	RSN5474 MIN	RSN5474 MAX	RSN54H74 MIN	RSN54H74 MAX	UNIT
f_{max}	Maximum clock frequency	30 and 31	C_L = 50 pF	20		30		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clear or preset	32	C_L = 50 pF		25		20	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear or preset	32	C_L = 50 pF		35		30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock	30 and 31	C_L = 50 pF		25		20	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock	30 and 31	C_L = 50 pF		30		25	ns

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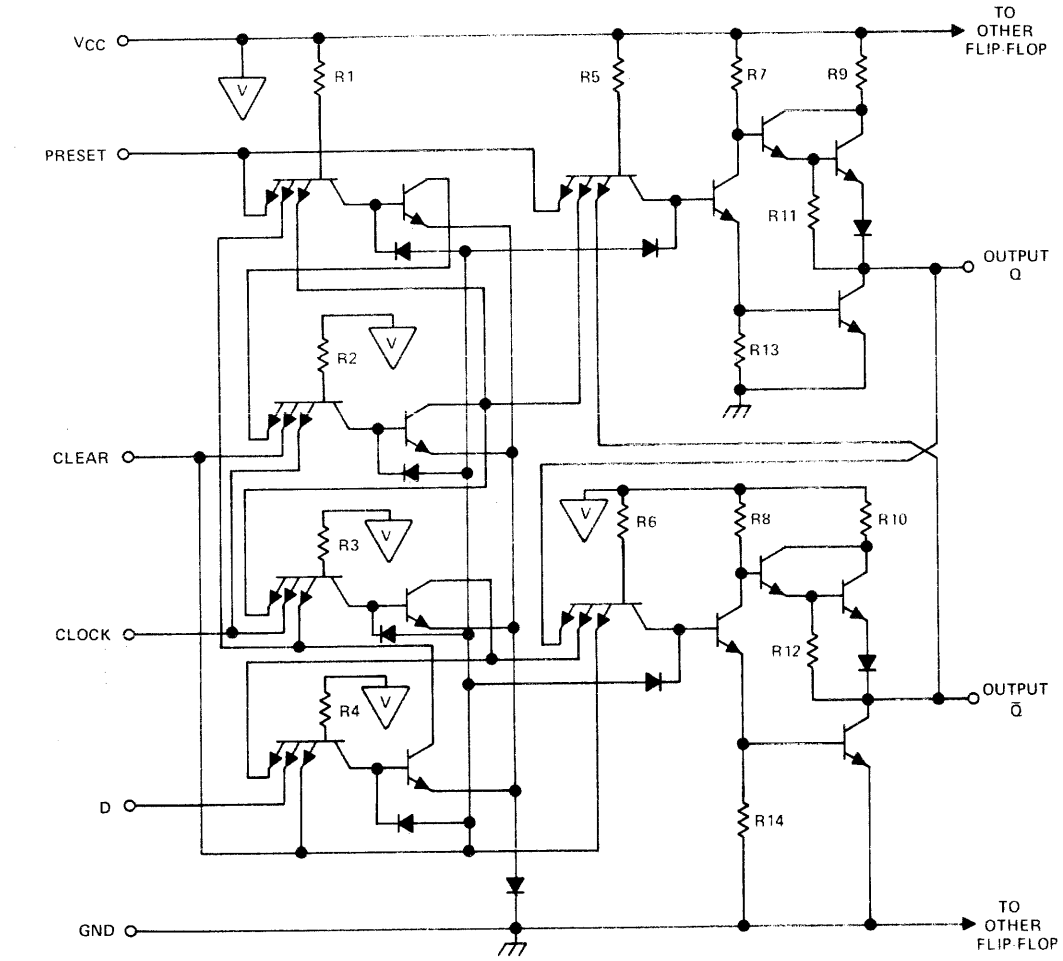
CIRCUIT TYPES RSN5474, RSN54H74
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

schematic (each flip-flop)



V . . . V_{CC} bus

NOMINAL RESISTOR VALUES

RESISTOR	RSN5474	RSN54H74
R1,R2,R3,R4,R5,R6	4 kΩ	2.8 kΩ
R7,R8,	1.6 kΩ	760 Ω
R9,R10	58 Ω	58 Ω
R11,R12	1 kΩ	1 kΩ
R13,R14	1 kΩ	470 Ω

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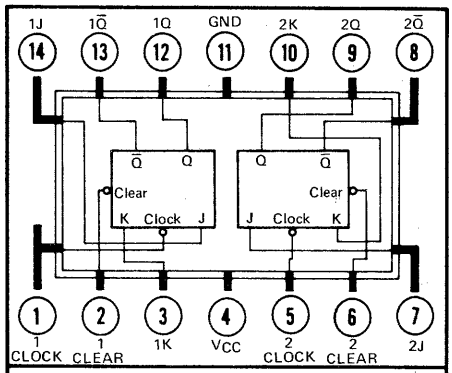
logic

TRUTH TABLE

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

H = high level, L = low level
t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse

H FLAT PACKAGE (TOP VIEW)



asynchronous input:
Low input to clear resets Q to low level.
Clear is independent of clock.

description

These monolithic J-K flip-flops are negative-edge triggered. The inputs are inhibited while the clock input is low; when the clock goes high the inputs are enabled and data will be accepted. The logic levels of the J and K inputs may be allowed to change when the clock input is high and the truth table will be observed as long as the minimum set-up times are maintained. Input data is transferred to the outputs on the negative edge of the clock pulse. A low input to clear resets Q to the low logic level independently of the clock.

recommended operating conditions

		RSN54H103			UNIT
		MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	V
Normalized fan-out from each output, N				10	
High-level output current, I_{OH}				−500	μA
Low-level output current, I_{OL}				20	mA
Clock frequency, f_{clock}		0		25	MHz
Width of clock pulse, $t_{w(clock)}$ (see Figure 33)		15			ns
Width of clear pulse, $t_{w(clear)}$ (see Figure 34)		15			ns
Input setup time, t_{setup} (see Note 1 and Figure 33)	High-level data	10			ns
	Low-level data	15			
Input hold time, t_{hold} (see Note 2 and Figure 33)		0			ns
High-to-low-level transition time of clock pulse, $t_{THL(clock)}$				150	ns
Operating free-air-temperature, T_A		−55		125	°C

NOTES: 1. Setup time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
2. Hold time is the interval immediately following the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.

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CIRCUIT TYPE RSN54H103
DUAL J-K EDGE-TRIGGERED FLIP-FLOP

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS†	RSN54H103 MIN	RSN54H103 MAX	UNIT
V_{IH}	High-level input voltage		24 and 25		2		V
V_{IL}	Low-level input voltage		24 and 25			0.8	V
V_{OH}	High-level output voltage		24	V_{CC} = MIN, I_{OH} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V	2.4		V
V_{OL}	Low-level output voltage		25	V_{CC} = MIN, I_{OL} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V		0.4	V
I_I	Input current at maximum input voltage		26	V_{CC} = MAX, V_I = 5.5 V		1	mA
I_{IH}	High-level input current	J or K input	26	V_{CC} = MAX, V_I = 2.4 V		50	μA
		clock or clear				100	
I_{IL}	Low-level input current	J or K input	26	V_{CC} = MAX, V_I = 0.4 V		−2	mA
		clock or clear				−4	
I_{OS}	Short-circuit output current‡		27	V_{CC} = MAX	−40	−100	mA
I_{CC}	Supply current		28	V_{CC} = MAX		52	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡No more than one output should be shorted at a time, and duration of the short-circuit test should not exceedone second. Only the $\overline{Q}$ outputs are tested.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	RSN54H103 MIN	RSN54H103 MAX	UNIT
f_{max}	Maximum clock frequency	33	C_L = 50 pF, R_L = 280 Ω	25		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clear to $\overline{Q}$	34	C_L = 50 pF, R_L = 280 Ω		15	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear to Q	34	C_L = 50 pF, R_L = 280 Ω		15	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock	33	C_L = 50 pF, R_L = 280 Ω		15	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock	33	C_L = 50 pF, R_L = 280 Ω		15	ns

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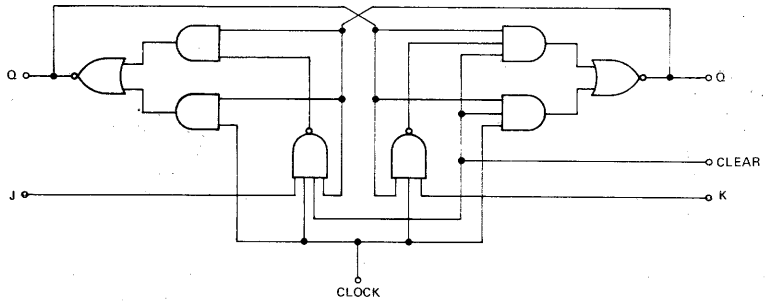
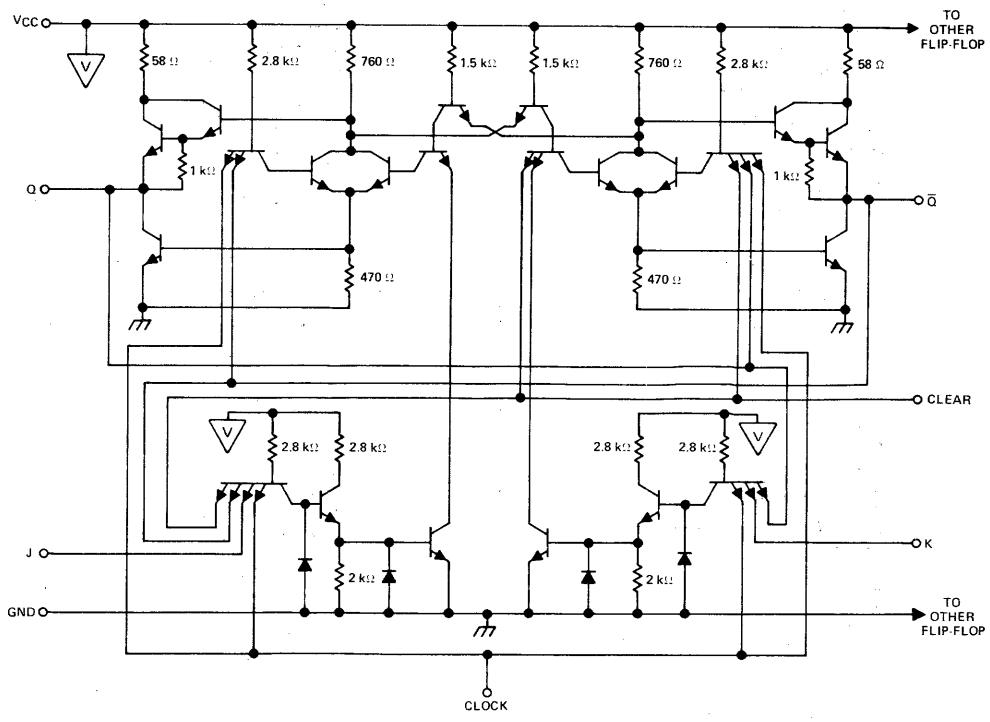
functional block diagram (each flip-flop)



schematic (each flip-flop)



▽ . . . V_{CC} bus
Resistor values shown are nominal.

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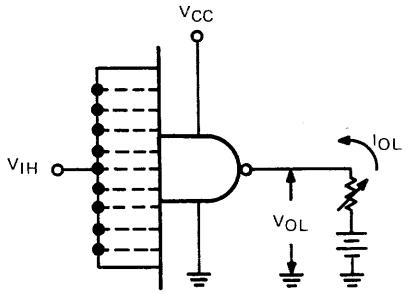
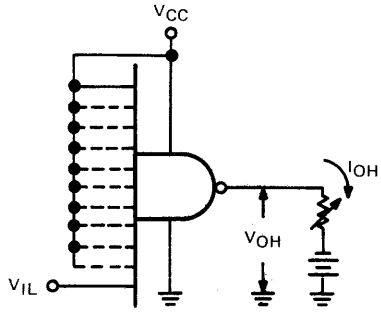
PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶



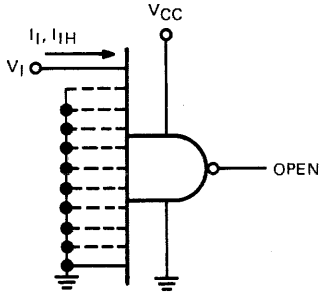
All inputs are tested simultaneously.

FIGURE 1–V_{IH}, V_{OL}



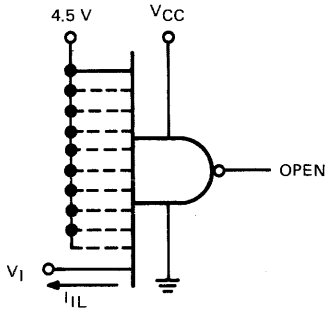
Each input is tested separately.

FIGURE 2–V_{IL}, V_{OH}



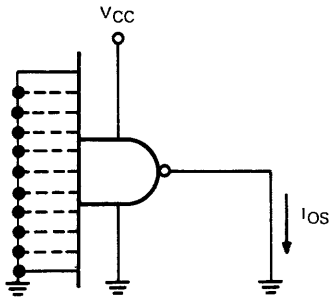
Each input is tested separately.

FIGURE 3–I_I, I_{IH}



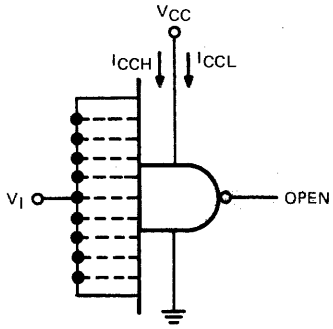
Each input is tested separately.

FIGURE 4–I_{IL}



Each gate is tested separately.

FIGURE 5–I_{OS}



All gates are tested simultaneously. Average-per-gate value = $\frac{I_{CC\ total}}{\text{number of gates in package}}$.

FIGURE 6–I_{CCH}, I_{CCL}

¶ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶ (continued)

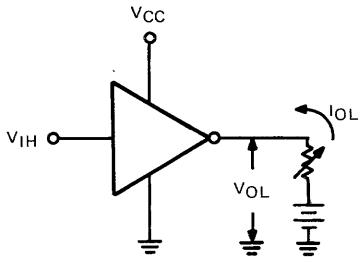


FIGURE 7–V_{IH}, V_{OL}

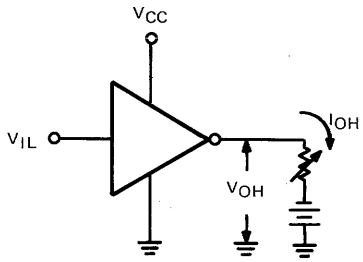


FIGURE 8–V_{IL}, V_{OH}

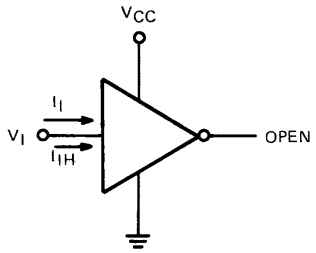


FIGURE 9–I_I, I_{IH}

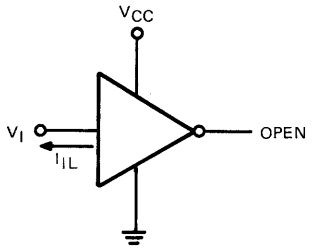
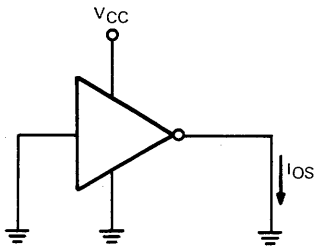
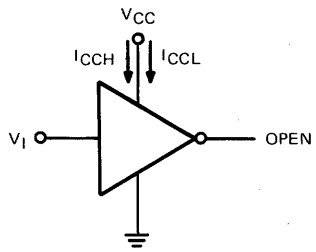


FIGURE 10–I_{IL}



Each inverter is tested separately.

FIGURE 11–I_{OS}



All inverters are tested simultaneously. Average-per-inverter value = $\frac{I_{CC\ total}}{\text{number of inverters in package}}$

FIGURE 12–I_{CCH}, I_{CCL}

¶ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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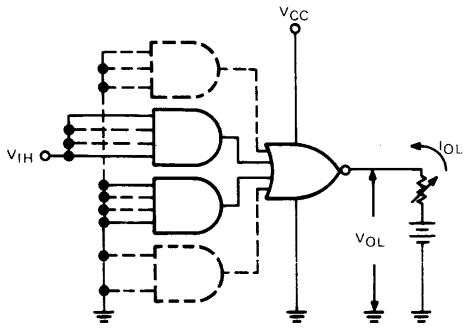
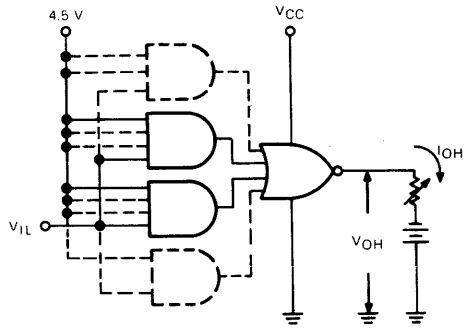
PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶ (continued)



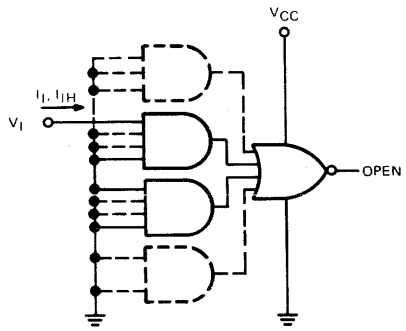
Each AND section is tested separately.

FIGURE 13–V_{IH}, V_{OL}



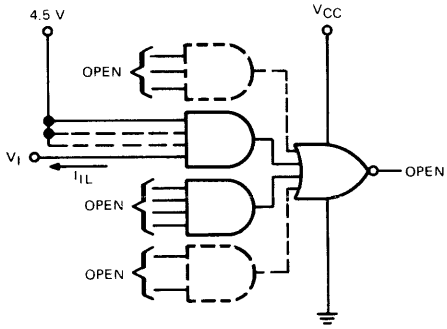
Each set of inputs is tested separately. A set comprises one input from each AND section.

FIGURE 14–V_{IL}, V_{OH}



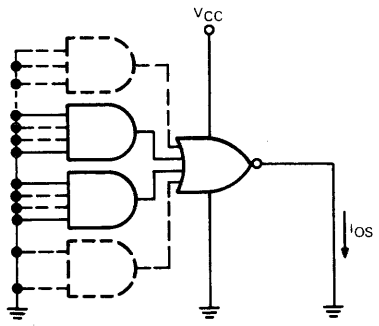
Each input is tested separately.

FIGURE 15–I_I, I_{IH}



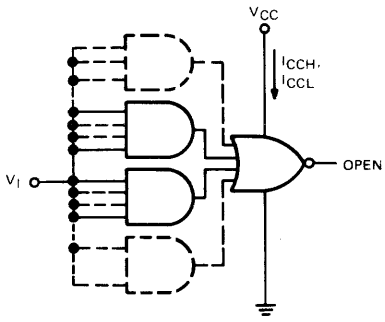
Each input is tested separately.

FIGURE 16–I_{IL}



Each output is tested separately.

FIGURE 17–I_{OS}



All gates are tested simultaneously. Average per-gate value = $\frac{I_{CC}\text{ total}}{\text{number of AOI gates in package}}$.

FIGURE 18–I_{CCH}, I_{CCL}

¶ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.
Dashed lines represent gates and/or inputs and outputs which are applicable to only some of the circuit types which reference these test circuits.

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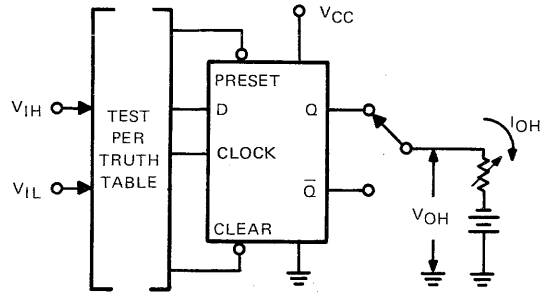
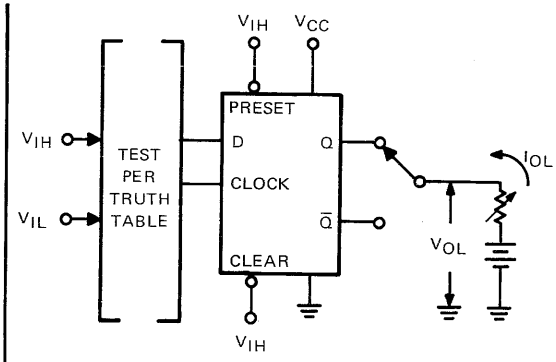
PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶ (continued)



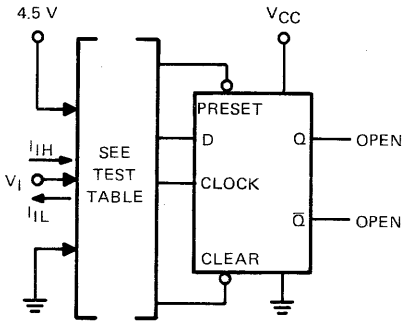
A. Each flip-flop is tested separately.
B. Each output is tested separately.
C. V_{OH} is also tested using clear and preset inputs.

FIGURE 19–V_{IH}, V_{IL}, V_{OH}



A. Each flip-flop is tested separately.
B. Each output is tested separately.

FIGURE 20–V_{IH}, V_{IL}, V_{OL}

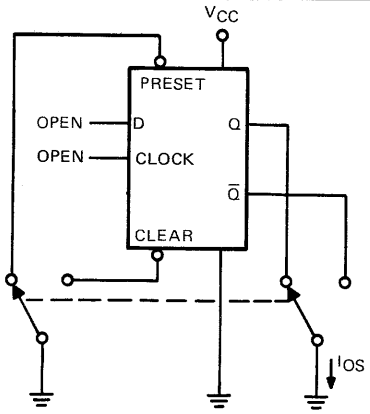


TEST TABLE

APPLY V_I MEASURE I_I, I_{IH}, I_{IL}	CONDITIONS ON OTHER INPUTS FOR I_I, I_{IH}		CONDITIONS ON OTHER INPUTS FOR I_{IL}	
	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND
Clock	Clear and D	Preset	Clear	Preset and D
Clock	Preset and D	Clear		
Preset	Clear and D	Clock (See Note B)	Clear	Clock and D
Clear	Preset	D and Clock (See Note B)	Clock, D, and Preset	None
Clear			D	Preset and Clock
D	Clock and Preset	Clear	Clock and Clear	Preset

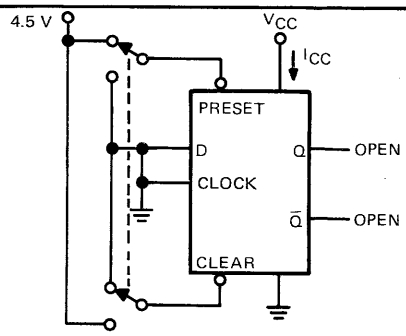
NOTES: A. Each input of each flip-flop is tested separately.
B. GND is momentarily applied to clock, then 4.5 V.

FIGURE 21–I_{IH}, I_{IL}



Each output is tested separately.

FIGURE 22–I_{OS}



I_{CC} is measured simultaneously for both flip-flops with D, clock, and preset at ground; then with D, clock, and clear at ground.

FIGURE 23–I_{CC}

¶ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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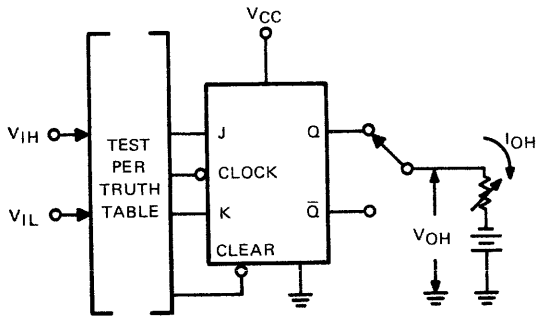
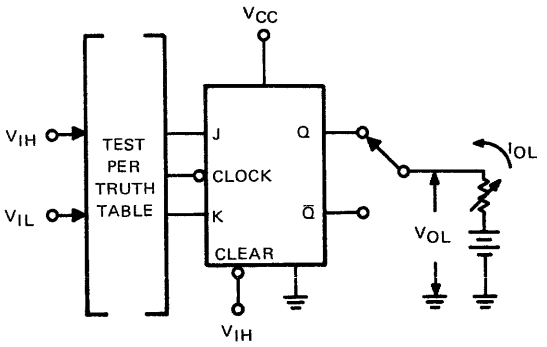
PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶ (continued)



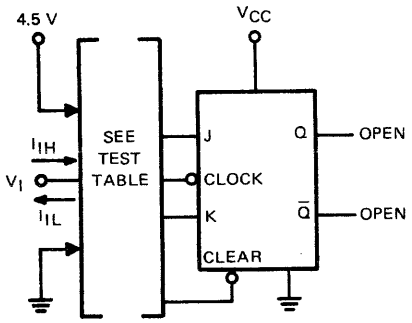
NOTES: A. Each flip-flop is tested separately.
B. Each output is tested separately.
C. V_{OH} at the $\overline{Q}$ output is also tested using the clear input.

FIGURE 24–V_{IH}, V_{IL}, V_{OH}



NOTES: A. Each flip-flop is tested separately.
B. Each output is tested separately.

FIGURE 25–V_{IH}, V_{IL}, V_{OL}



TEST TABLE

APPLY V_I, MEASURE I_{IH} OR I_{IL}	CONDITIONS ON OTHER INPUTS FOR I_{IH}			CONDITIONS ON OTHER INPUTS FOR I_{IL}	
	APPLY 4.5 V	APPLY MOMENTARY GND	APPLY GND	APPLY 4.5 V	APPLY MOMENTARY GND
Clock	Clear	$\overline{Q}$ (See Note C)	Clear, J, and K J and K	Clear, J, and K (See Note B)	
Clear		Clear (See Note D) $\overline{Q}$ (See Note C)	Clock and J Clock and J	Clock and J	
J			Clock and Clear	Clock and Clear	Q (See Note C)
K		Clear (See Note E)	Clock	Clock and Clear	$\overline{Q}$ (See Note C)

NOTES: A. Each input of each flip-flop is tested separately.
B. While maintaining all other conditions, the clock input is momentarily raised to 4.5 V, the V_I is reapplied, and a second measurement of I_{IL} is made.
C. After the application of momentary ground to the specified output, both Q and $\overline{Q}$ are left floating.
D. Apply momentary ground before V_I.
E. Apply momentary ground, then 4.5 V.

FIGURE 26–I_{IH}, I_{IL}

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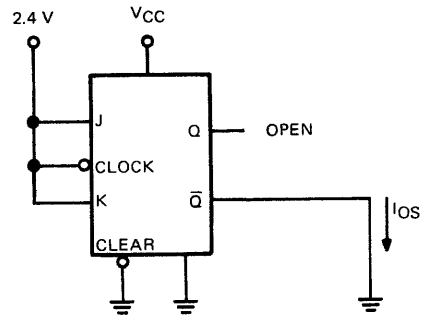
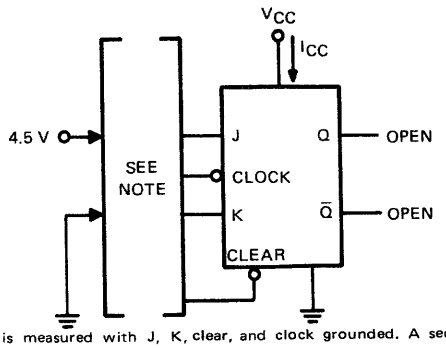


Each $\overline{Q}$ output is tested separately.

FIGURE 27–I_{OS}



I_{CC} is measured with J, K, clear, and clock grounded. A second measurement is made with K grounded, 4.5 V applied to J and clear, and momentary 4.5 V, then ground, applied to clock.

FIGURE 28–I_{CC}

¶Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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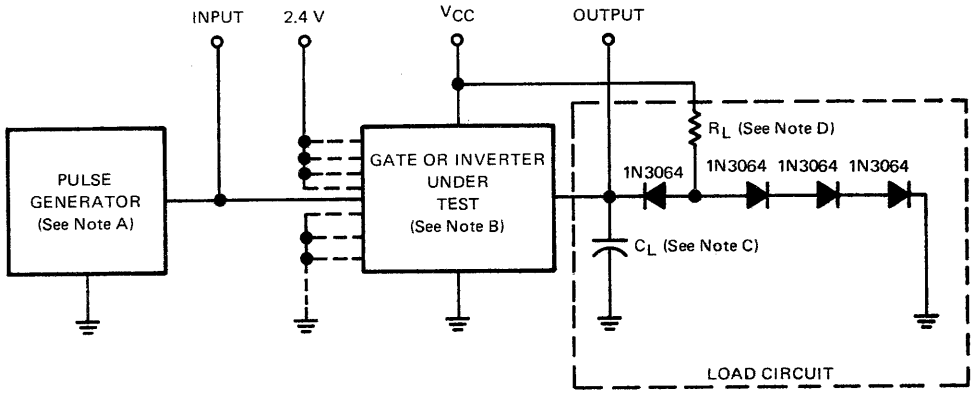
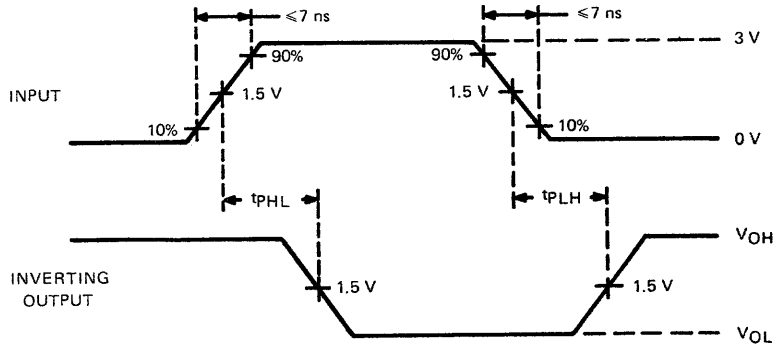
PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\ \Omega$.
B. Input conditions are established for each gate as follows:
1. Input pulse is applied to one input and 2.4 V is applied to all unused inputs of the NAND gates.
2. Input pulse is applied to one AND section, and 2.4 V is applied to all unused inputs of that AND section, and all inputs of all unused AND sections of the AND-OR-INVERT gates are grounded.
C. C_L includes probe and jig capacitance.
D. For Series RSN54 circuits, $R_L = 400\ \Omega$. For Series RSN54H circuits, $R_L = 280\ \Omega$.

FIGURE 29–GATE PROPAGATION DELAY TIMES

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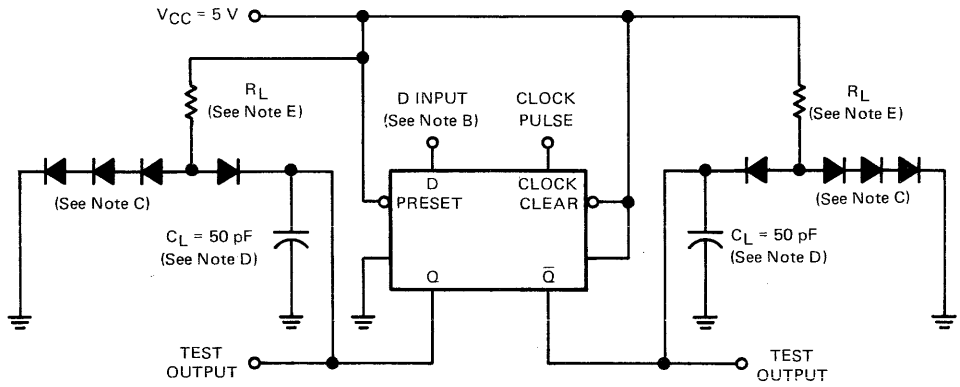
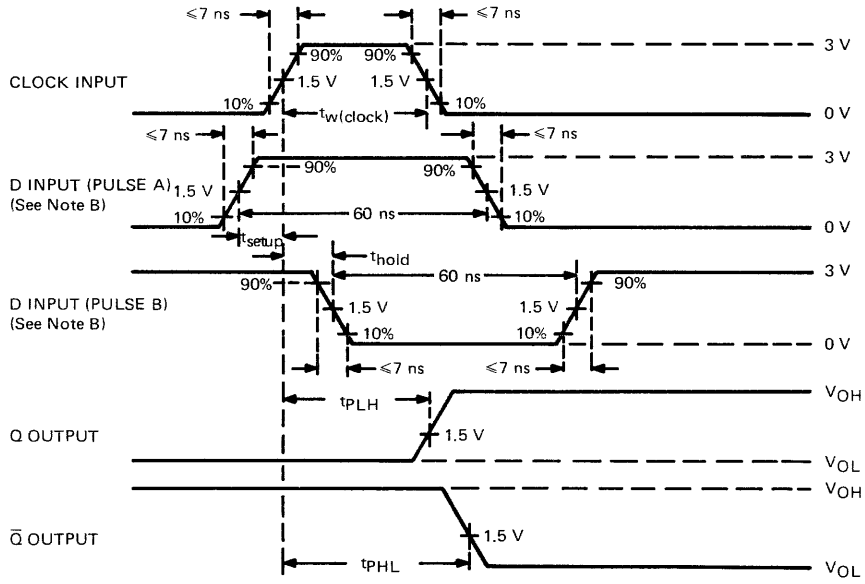
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. Clock input pulse has the following characteristics: $t_{w(clock)}$ = 30 ns for RSN5474 circuits, 20 ns for RSN54H74 circuits, and PRR = 1 MHz. When testing f_{clock}, vary PRR.

B. D input (pulse A) has the following characteristics: t_{setup} = 20 ns for RSN5474 circuits, 15 ns for RSN54H74 circuits, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: t_{hold} = 5 ns for RSN5474 circuits, 0 ns for RSN54H74 circuits, and PRR is 50% of the clock PRR.

C. All diodes are 1N3064.

D. C_L includes probe and jig capacitance.

E. For RSN5474 circuits, R_L = 400 Ω. For RSN54H74 circuits, R_L = 280 Ω.

FIGURE 30–SWITCHING CHARACTERISTICS, CLOCK AND SYNCHRONOUS INPUT OF D-TYPE FLIP-FLOPS (HIGH-LEVEL DATA)

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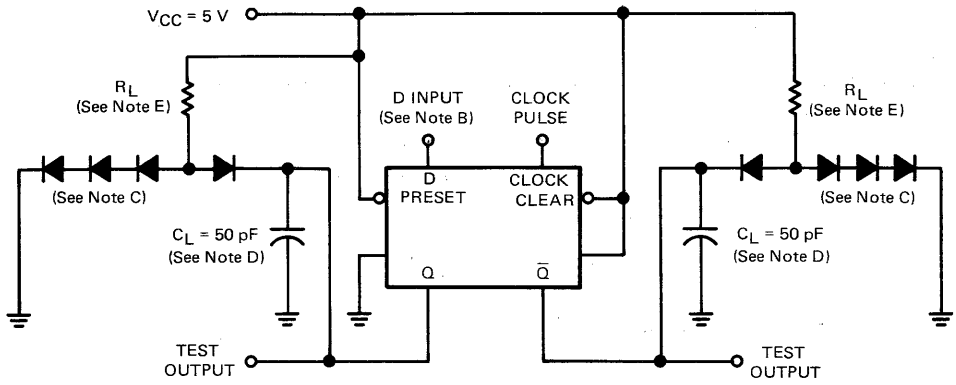
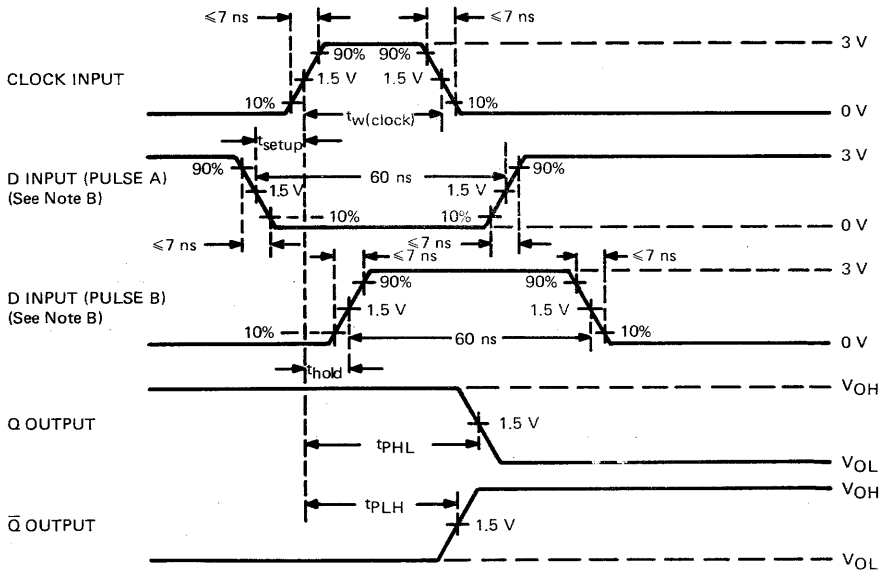
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. Clock input pulse has the following characteristics: t_w = 30 ns for RSN5474 circuits, 20 ns for RSN54H74 circuits, and PRR = 1 MHz. When testing f_{clock}, vary PRR.

B. D input (pulse A) has the following characteristics: t_{setup} = 20 ns for RSN5474 circuits, 15 ns for RSN54H74 circuits, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: t_{hold} = 5 ns for RSN5474 circuits, 0 ns for RSN54H74 circuits, t_w = 60 ns, and PRR is 50% of the clock PRR.

C. All diodes are 1N3064.

D. C_L includes probe and jig capacitance.

E. For RSN5474 circuits, R_L = 400 Ω. For RSN54H74 circuits, R_L = 280 Ω.

FIGURE 31–SWITCHING CHARACTERISTICS, CLOCK AND SYNCHRONOUS INPUTS OF D-TYPE FLIP-FLOPS (LOW-LEVEL DATA)

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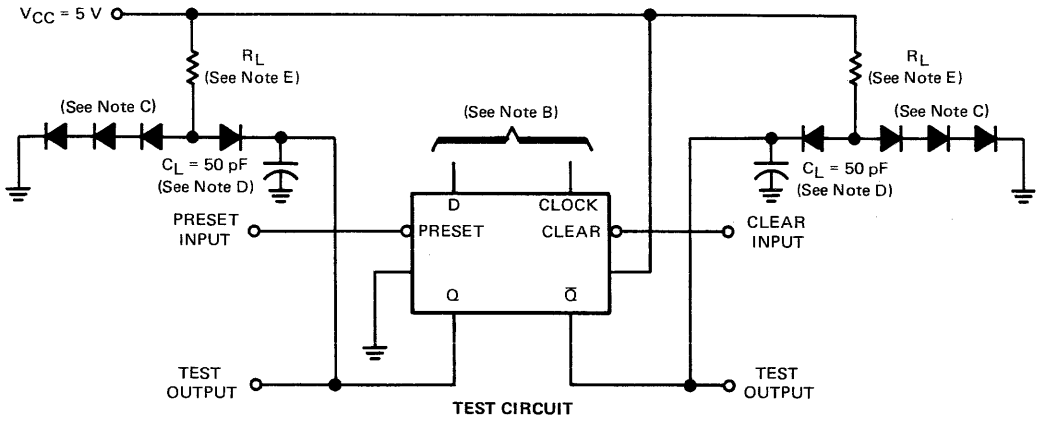
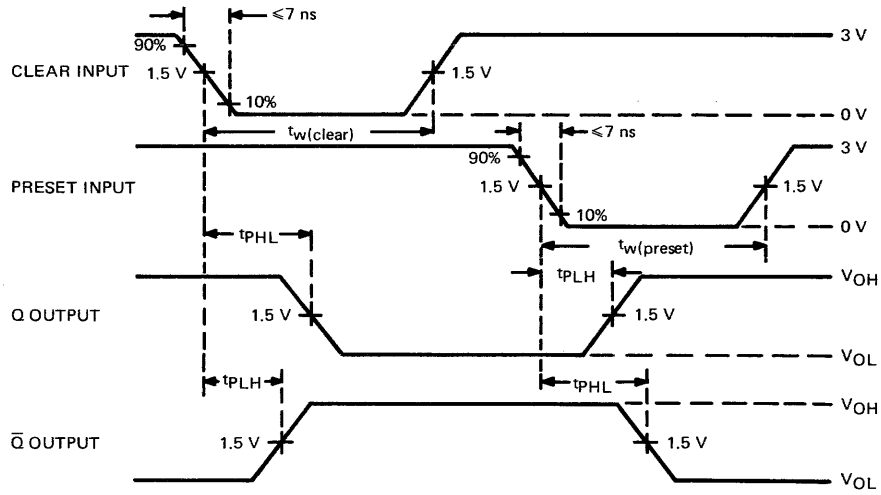
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. Clear or preset input pulse characteristics: $t_{w(clear)} = t_{(preset)}$ = 30 ns for RSN5474 circuits, 20 ns for RSN54H74 circuits, and PRR = 1 MHz.
B. Clear and preset inputs dominate regardless of the state of clock or D inputs.
C. All diodes are 1N3064.
D. C_L includes probe and jig capacitance.
E. For RSN5474 circuits, R_L = 400 Ω. For RSN54H74 circuits, R_L = 280 Ω.

FIGURE 32–SWITCHING CHARACTERISTICS, ASYNCHRONOUS INPUTS OF D-TYPE FLIP-FLOPS

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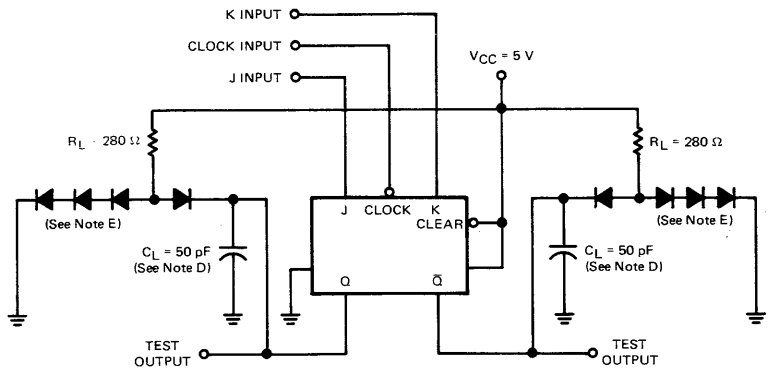
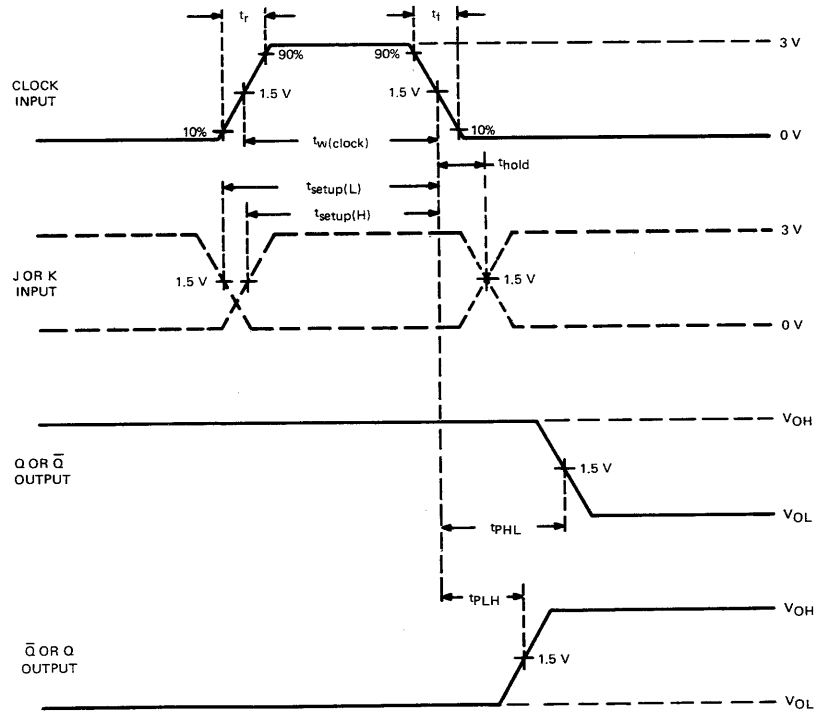
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. When testing propagation delay times from clock input, the clock input pulse characteristics are: $t_r \leqslant 7$ ns, $t_f \leqslant 7$ ns, $t_{w(clock)} = 20$ ns, PRR = 1 MHz.

B. When testing f_{max}, the clock input characteristics are: $t_r \leqslant 3$ ns, $t_f = \leqslant 3$ ns, $t_{w(clock)} = 12$ ns, PRR = 25 MHz.

C. Both J and K inputs are tested with the input not under test grounded. For the J or K input pulse, t_r or $t_f \leqslant 7$ ns, and t_{setup} is the minimum specified under recommended operating conditions.

D. C_L includes probe and jig capacitance.

E. All diodes are 1N3064.

FIGURE 33–SWITCHING CHARACTERISTICS, CLOCK AND SYNCHRONOUS INPUTS OF J-K FLIP-FLOPS

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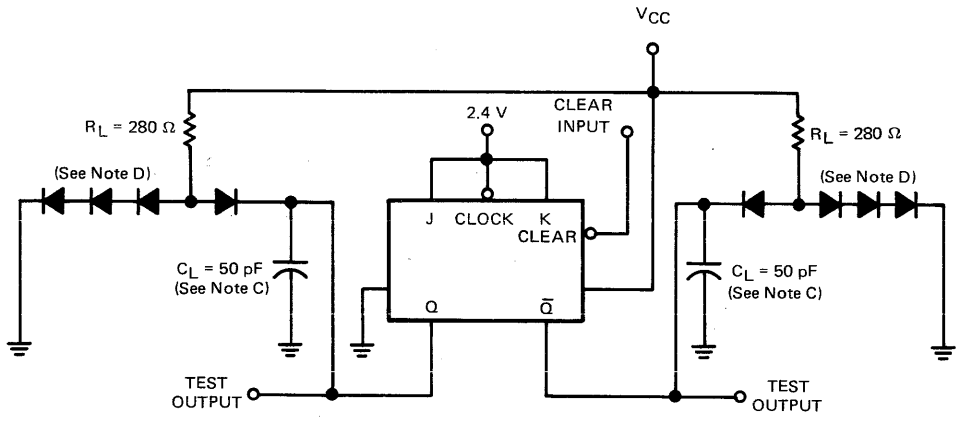
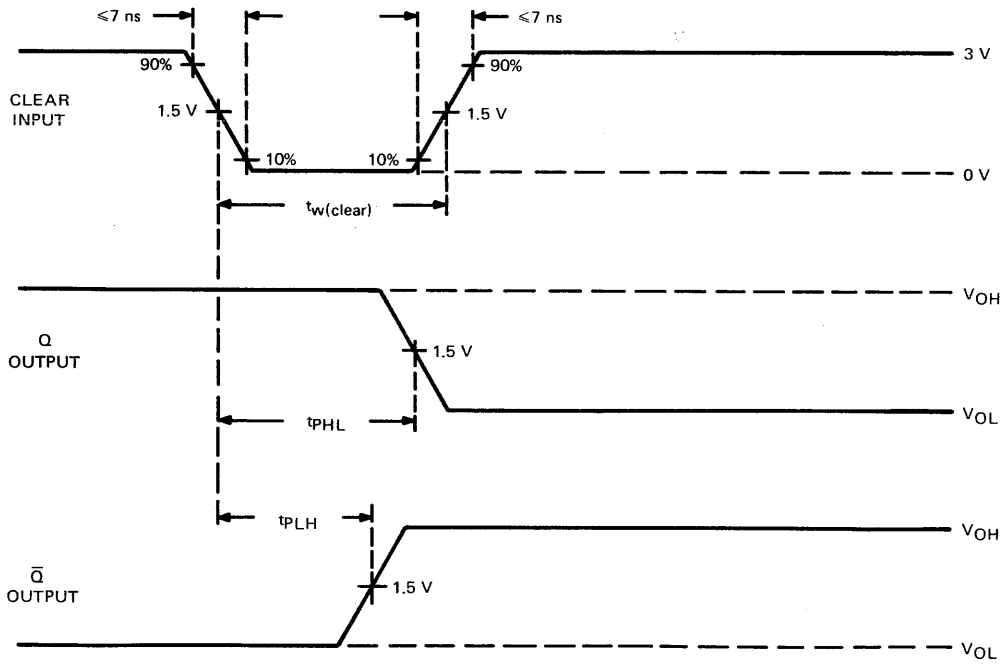
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The clear input pulse characteristics are: $t_{w(clear)}$ = 16 ns, PRR = 1 MHz.
B. Q output may be set to the high level with a clock pulse.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N3064.

FIGURE 34–SWITCHING CHARACTERISTICS, ASYNCHRONOUS INPUTS OF J-K FLIP-FLOPS

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SERIES RSN54L
RADIATION-HARDENED TTL INTEGRATED CIRCUITS

SERIES RSN54L
BULLETIN NO. DL-S 7111462, MARCH 1971

TTL INTEGRATED CIRCUITS WITH HIGH TOLERANCE TO GAMMA AND NEUTRON IRRADIATION

- Very Low Power Dissipation . . . 1 mW Per Gate Typical at 50% Duty Cycle
- High D-C Noise Margin . . . 1 Volt Typical
- Low Output Impedance Provides Low A-C Noise Susceptibility
- Waveform Integrity over Full Range of Loading and Temperature Conditions
- Normalized Fan-Out to Ten Loads
- Typical NAND Gate Propagation Delay Time (C_L = 50 pF) . . . 45 ns

description

Series RSN54L TTL integrated circuits are specifically designed and fabricated for operation and survivability in nuclear-radiation environments. The basic Series 54/74 configuration, desirable for its "natural" hardness, has been coupled with a state-of-the-art circuit-hardening process. This technology, compatible for use in high volume production, employs:

- dielectric isolation
- thin-film resistors
- small transistor geometries
- shallow base diffusions
- heavy gold doping
- minimum collector thickness and resistivity
- aluminum interconnection system

Series RSN54, RSN54H, and RSN54L logic families are completely compatible with one another and with most other TTL and DTL circuits. These circuits are designed to operate at the same supply voltages and logic levels with the high d-c noise margins which are characteristic of Texas Instruments Series 54/74 circuits. These families of radiation-hardened circuits include the gates and flip-flops needed to perform functions within present-day digital electronic systems. And since these three families are compatible with one another, Series RSN54L circuits may be selectively used to minimize power dissipation in system locations where speed is not the limiting parameter.

Series RSN54L circuits are designed for operation over the full military temperature range of −55°C to 125°C.

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CONTENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1)	7 V
Input voltage (See Notes 1 and 2)	5.5 V
Operating free-air temperature range	−55°C to 125°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

input-current requirements

Input-current requirements reflect worst-case conditions for T_A = −55°C to 125°C and V_{CC} = 4.5 V to 5.5 V. Currents into the input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

Each input of the Series RSN54L multiple-emitter input transistors requires no more than a 0.18-mA flow out of the input at a low voltage level; therefore one normalized load (N = 1) is −0.18 mA maximum. Each input requires current into the input at a high voltage level. This current is 10 μA maximum (one normalized load) for each emitter input.

fan-out capability

Fan-out (N) reflects the ability of an output to sink current from a number of Series RSN54L loads at a low voltage level and to supply current at a high voltage level. Each output is capable of sinking current or supplying current to 10 normalized loads (N = 10) within the same series. In addition, Series RSN54L outputs will drive one Series RSN54 load, plus two Series RSN54L loads or one Series RSN54H load. Currents out of the output terminal are specified as negative values.

unused inputs

For optimum switching times and minimum noise susceptibility, unused inputs should be maintained at a positive voltage greater than 2.4 V but not to exceed the absolute maximum rating of 5.5 V. This eliminates the distributed capacitance associated with the floating-input-transistor emitter, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times. Some possible ways of handling input emitters are:

a. Connect unused inputs to an independent supply voltage. Preferably this voltage should be between 2.4 V and 3.5 V.

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b. Connect unused inputs to a used input if maximum fan-out of the driving output will not be exceeded. Each input presents a full load to the driving output at a high-level voltage but adds no loading at a low-level voltage.

c. Connect unused inputs to V_{CC} through a 1-kΩ resistor so that if a transient which exceeds the 5.5-V maximum rating should occur, the impedance will be high enough to protect the input. One-to-25 unused inputs may be connected to each 1-kΩ resistor.

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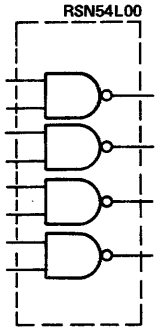
standard line summary

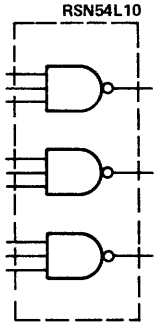
GATE CIRCUITS

RSN54L00



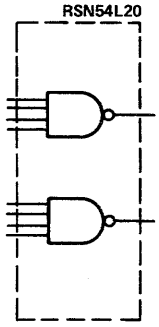
QUADRUPLE 2-INPUT
POSITIVE-NAND GATES

RSN54L10



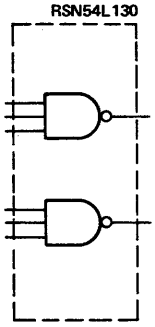
TRIPLE 3-INPUT
POSITIVE-NAND GATES

RSN54L20



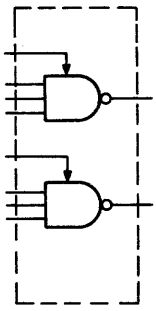
DUAL 4-INPUT
POSITIVE-NAND GATES

RSN54L130



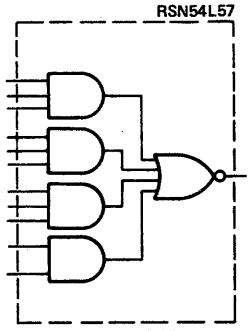
DUAL 3-INPUT
POSITIVE-NAND GATE

RSN54L131



DUAL EXPANDABLE 3-INPUT
POSITIVE-NAND GATE

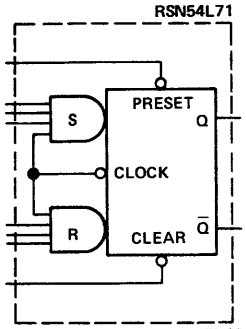
RSN54L57



3-3-3-2 INPUT
AND-OR-INVERT GATE

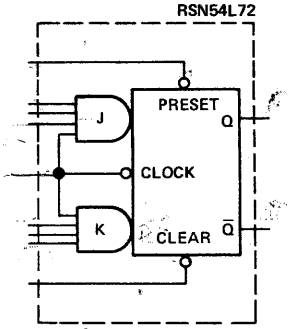
FLIP-FLOP CIRCUITS

RSN54L71



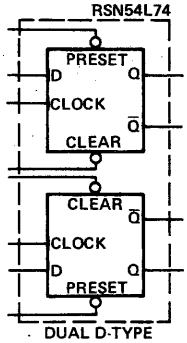
S-R MASTER SLAVE FLIP-FLOP

RSN54L72



J-K MASTER SLAVE FLIP-FLOP

RSN54L74



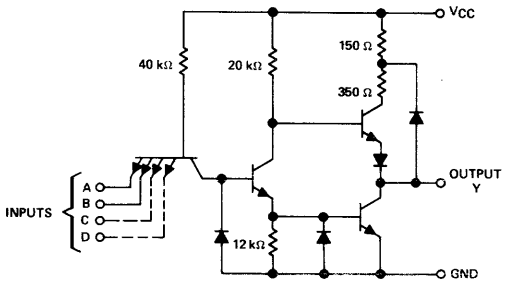
DUAL D-TYPE
EDGE-TRIGGERED FLIP-FLOPS

10

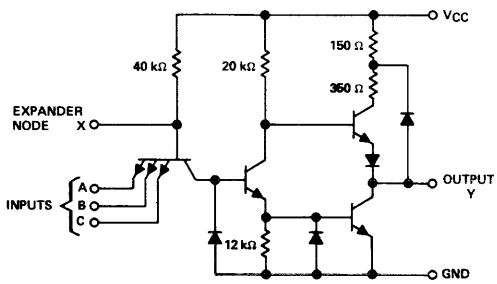
CIRCUIT TYPES RSN54L00, RSN54L10, RSN54L20, RSN54L130, RSN54L131
POSITIVE-NAND GATES

schematics (each gate)

RSN54L00, RSN54L10, RSN54L20, RSN54L130



RSN54L131

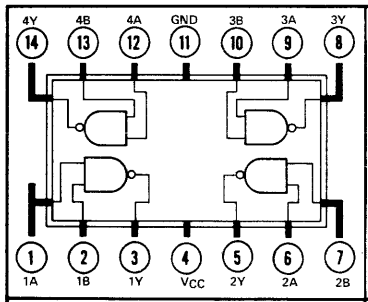


Component values shown are nominal.

logic

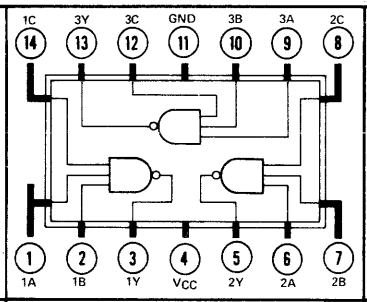
H FLAT PACKAGE (TOP VIEWS)

RSN54L00



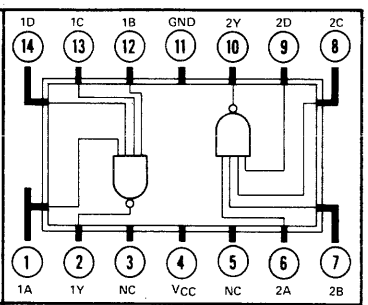
positive logic: $Y = \overline{AB}$

RSN54L10



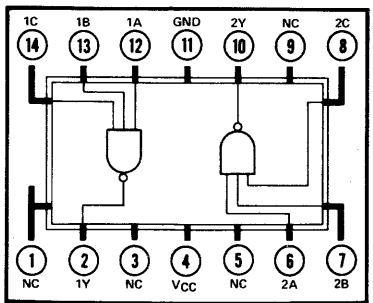
positive logic: $Y = \overline{ABC}$

RSN54L20



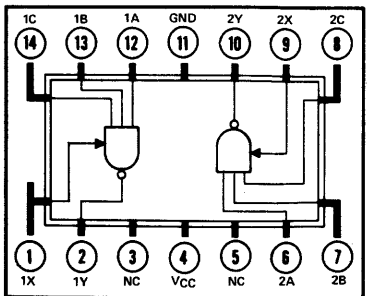
positive logic: $Y = \overline{ABCD}$

RSN54L130



positive logic: $Y = \overline{ABC}$

RSN54L131



positive logic: $Y = \overline{ABCX}$

NC—No internal connection

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recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Normalized fan-out from each gate, N			10	
Operating free-air temperature, T_A	−55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
V_{IH}	High-level input voltage	1		1.9		V
V_{IL}	Low-level input voltage	2			0.8	
V_{OH}	High-level output voltage	2	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −100 μA	2.4		V
V_{OL}	Low-level output voltage	1	V_{CC} = MIN, V_{IH} = 1.9 V, I_{OL} = 2 mA		0.3	V
I_I	Input current at maximum input voltage	3	V_{CC} = MAX, V_I = 5.5 V		100	μA
I_{IH}	High-level input current	3	V_{CC} = MAX, V_I = 2.4 V		10	μA
I_{IL}	Low-level input current	4	V_{CC} = MAX, V_I = 0.3 V		−0.18	mA
I_{OS}	Short-circuit output current	5	V_{CC} = MAX	−1	−15	mA
I_{CCH}	Supply current, high-level output (average per gate)	6	V_{CC} = MAX, V_I = 0		0.2	mA
I_{CCL}	Supply current, low-level output (average per gate)	6	V_{CC} = MAX, V_I = 4.5 V		0.51	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	28	C_L = 50 pF, R_L = 4 kΩ		60	ns
t_{PLH}	Propagation delay time, high-to-low-level output				60	ns

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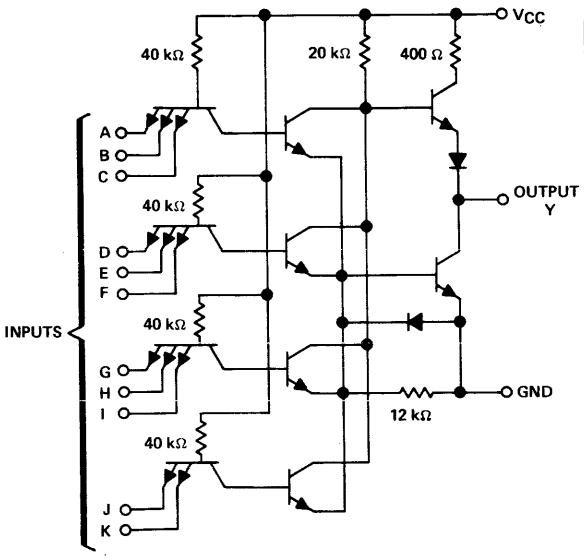
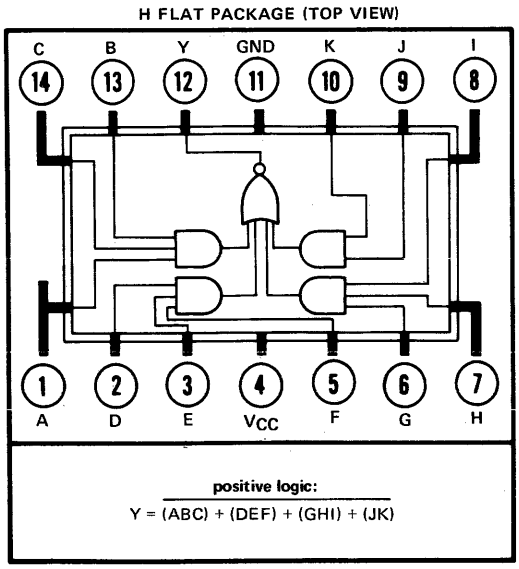
CIRCUIT TYPE RSN54L57
3-3-3-2-INPUT AND-OR-INVERT GATE

schematic



logic



recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Normalized fan-out from output, N			10	
Operating free-air temperature, T_A	−55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
V_{IH}	High-level input voltage	7		1.9		V
V_{IL}	Low-level input voltage	8			0.8	V
V_{OH}	High-level output voltage	8	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −100 μA	2.4		V
V_{OL}	Low-level output voltage	7	V_{CC} = MIN, I_{IH} = 1.9 V, I_{OL} = 2 mA		0.3	V
I_I	Input current at maximum input voltage	9	V_{CC} = MAX, V_I = 5.5 V		100	μA
I_{IH}	High-level input current	9	V_{CC} = MAX, V_I = 2.4 V		10	μA
I_{IL}	Low-level input current	10	V_{CC} = MAX, V_I = 0.3 V		−0.18	mA
I_{OS}	Short-circuit output current	11	V_{CC} = MAX	−1	−15	mA
I_{CCH}	Supply current, high-level output	12	V_{CC} = MAX, V_I = 0		0.8	mA
I_{CCL}	Supply current, low-level output	12	V_{CC} = MAX, V_I = 4.5 V		0.99	mA

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switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	28	C_L = 50 pF, R_L = 4 kΩ		90	ns
t_{PHL}	Propagation delay time, high-to-low-level output				60	ns

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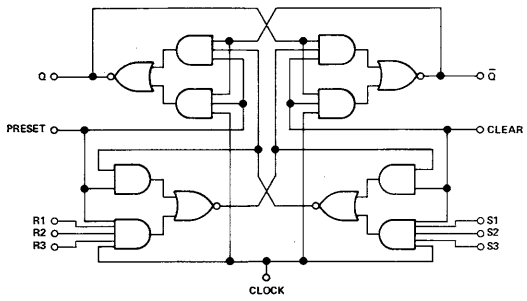
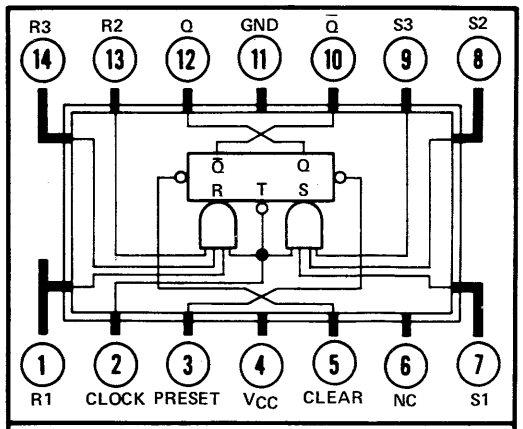
CIRCUIT TYPE RSN54L71
S-R MASTER-SLAVE FLIP-FLOP

functional block diagram



logic

H FLAT PACKAGE (TOP VIEW)



positive logic:
Low input to preset sets Q to high level
Low input to clear resets Q to low level
Preset and clear are independent of clock

NC—No internal connection

description

These S-R flip-flops are based on the master-slave principle. The AND-OR gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows:

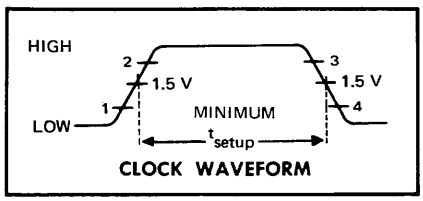
1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND-OR gate inputs
4. Transfer information from master to slave

Logic levels of S and R inputs must not be allowed to change when the clock pulse is in a high state.

TRUTH TABLE

INPUTS AT t_n		OUTPUTS AT t_{n+1}	
S	R	Q	$\bar{Q}$
L	L	Q_n	$\bar{Q}_n$
L	H	L	H
H	L	H	L
H	H	Indeterminate	

$S = S1 \cdot S2 \cdot S3$
$R = R1 \cdot R2 \cdot R3$
t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse
Q_n = level of output Q at t_n
$\bar{Q}_n$ = level of output $\bar{Q}$ at t_n



CLOCK WAVEFORM

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CIRCUIT TYPE RSN54L71
S-R MASTER-SLAVE FLIP-FLOP

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Normalized fan-out from each output, N			10	
Width of clock pulse, $t_{w(clock)}$	200			ns
Width of preset pulse, $t_{w(preset)}$	100			ns
Width of clear pulse, $t_{w(clear)}$	100			ns
Input setup time, t_{setup} (see Note 1)	100			ns
Input hold time, t_{hold} (see Note 2)	0			ns
Operating free-air temperature, T_A	−55		125	°C

NOTES: 1. Setup time is the interval immediately preceeding the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
2. Hold time is the interval immediately following the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
V_{IH}	High-level input voltage		13 and 14		1.9		V
V_{IL}	Low-level input voltage		13 and 14			0.8	V
V_{OH}	High-level output voltage		13	V_{CC} = MIN, V_{IH} = 1.9 V, V_{IL} = 0.8 V, I_{OH} = −100 μA	2.4		V
V_{OL}	Low-level output voltage		14	V_{CC} = MIN, V_{IH} = 1.9 V, V_{IL} = 0.8 V, I_{OL} = 2 mA		0.3	V
I_I	Input current at maximum input voltage	Any S or R	15	V_{CC} = MAX, V_I = 5.5 V		100	μA
		Preset, clear or clock				200	
I_{IH}	High-level input current	Any S or R	15	V_{CC} = MAX, V_I = 2.4 V		10	μA
		Preset, clear, or clock				20	
I_{IL}	Low-level input current	Any S or R	16	V_{CC} = MAX, V_I = 0.3 V		−0.18	mA
		Preset, clear, or clock				−0.4	
I_{OS}	Short-circuit output current		17	V_{CC} = MAX	−1	−15	mA
I_{CC}	Supply current		15	V_{CC} = MAX		1.44	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	29	C_L = 50 pF, R_L = 4 kΩ		3		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from preset or clear	30				75	ns
t_{PHL}	Propagation delay time, high-to-low-level output from preset or clear					150	
t_{PLH}	Propagation delay time, low-to-high-level output from clock	29		10		75	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			10		150	

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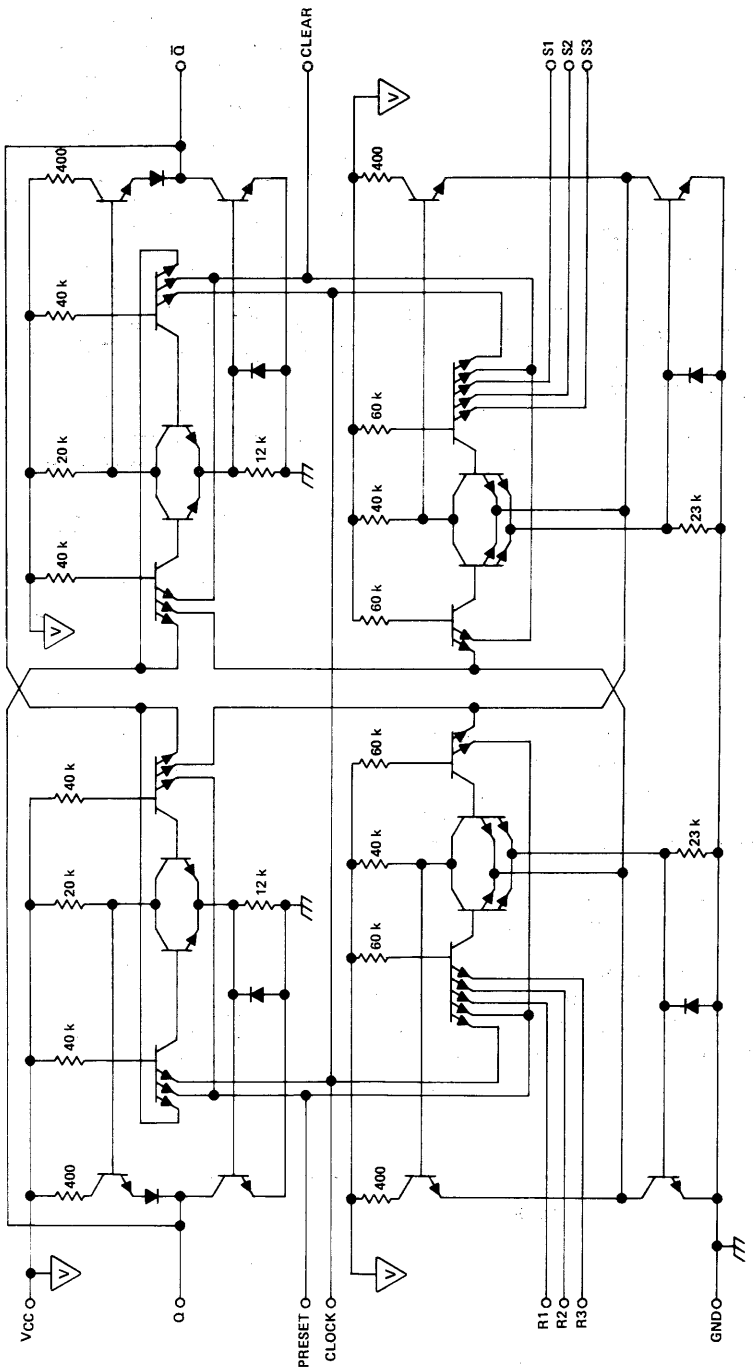
schematic



... V_{CC} bus
Resistor values are nominal in ohms.

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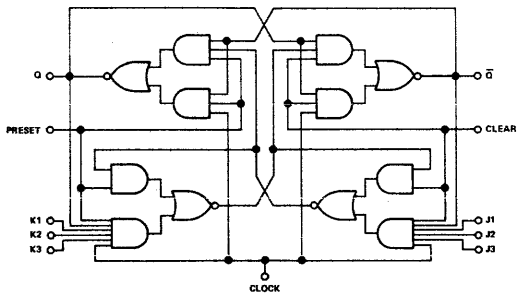
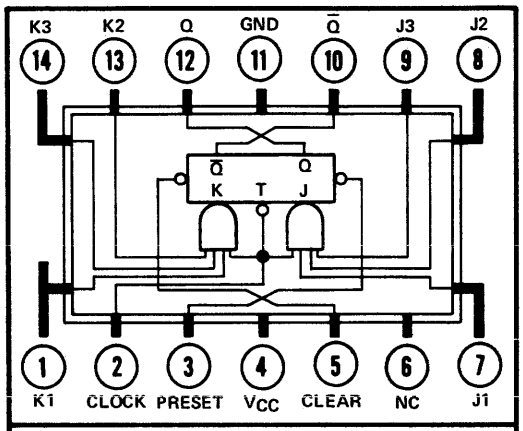
CIRCUIT TYPE RSN54L72
J-K MASTER-SLAVE FLIP-FLOP

functional block diagram



logic

H FLAT PACKAGE (TOP VIEW)



positive logic:
Low input to preset sets Q to high level
Low input to clear resets Q to low level
Preset and clear are independent of clock

NC—No internal connection

description

These J-K flip-flops are based on the master-slave principle. The AND-OR gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows:

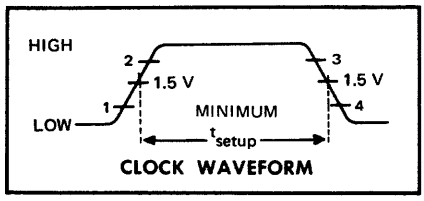
1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND-OR gate inputs
4. Transfer information from master to slave

Logic levels of J and K inputs must not be allowed to change when the clock pulse is in a high state.

TRUTH TABLE

INPUTS AT t_n		OUTPUTS AT t_{n+1}	
J	K	Q	$\overline{Q}$
L	L	Q_n	$\overline{Q}_n$
L	H	L	H
H	L	H	L
H	H	$\overline{Q}_n$	Q_n

$J = J1 \cdot J2 \cdot J3$
$K = K1 \cdot K2 \cdot K3$
t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse
Q_n = level of output Q at t_n
$\overline{Q}_n$ = complement of Q_n or level of output $\overline{Q}$ at t_n



CLOCK WAVEFORM

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recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Normalized fan-out from each output, N			10	
Width of clock pulse, $t_{w(clock)}$	200			ns
Width of preset pulse, $t_{w(preset)}$	100			ns
Width of clear pulse, $t_{w(clear)}$	100			ns
Input setup time, t_{setup} (see Note 1)	$t_{w(clock)}$			ns
Input hold time, t_{hold} (see Note 2)	0			ns
Operating free-air temperature, T_A	−55		125	°C

NOTES: 1. Setup time is the interval immediately preceeding the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
2. Hold time is the interval immediately following the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
V_{IH}	High-level input voltage		18 and 19		1.9		V
V_{IL}	Low-level input voltage		18 and 19			0.8	V
V_{OH}	High-level output voltage		18	V_{CC} = MIN, V_{IH} = 1.9 V, V_{IL} = 0.8 V, I_{OH} = −100 μA	2.4		V
V_{OL}	Low-level output voltage		19	V_{CC} = MIN, V_{IH} = 1.9 V, V_{IL} = 0.8 V, I_{OL} = 2 mA		0.3	V
I_I	Input current at maximum input voltage	Any J or K	20	V_{CC} = MAX, V_I = 5.5 V		100	μA
		Preset, clear or clock				200	
I_{IH}	High-level input current	Any J or K	20	V_{CC} = MAX, V_I = 2.4 V		10	μA
		Preset, clear, or clock				20	
I_{IL}	Low-level input current	Any J or K	21	V_{CC} = MAX, V_I = 0.3 V		−0.18	mA
		Preset, clear, or clock				−0.4	
I_{OS}	Short-circuit output current		22	V_{CC} = MAX	−1	−15	mA
I_{CC}	Supply current		20	V_{CC} = MAX		1.44	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

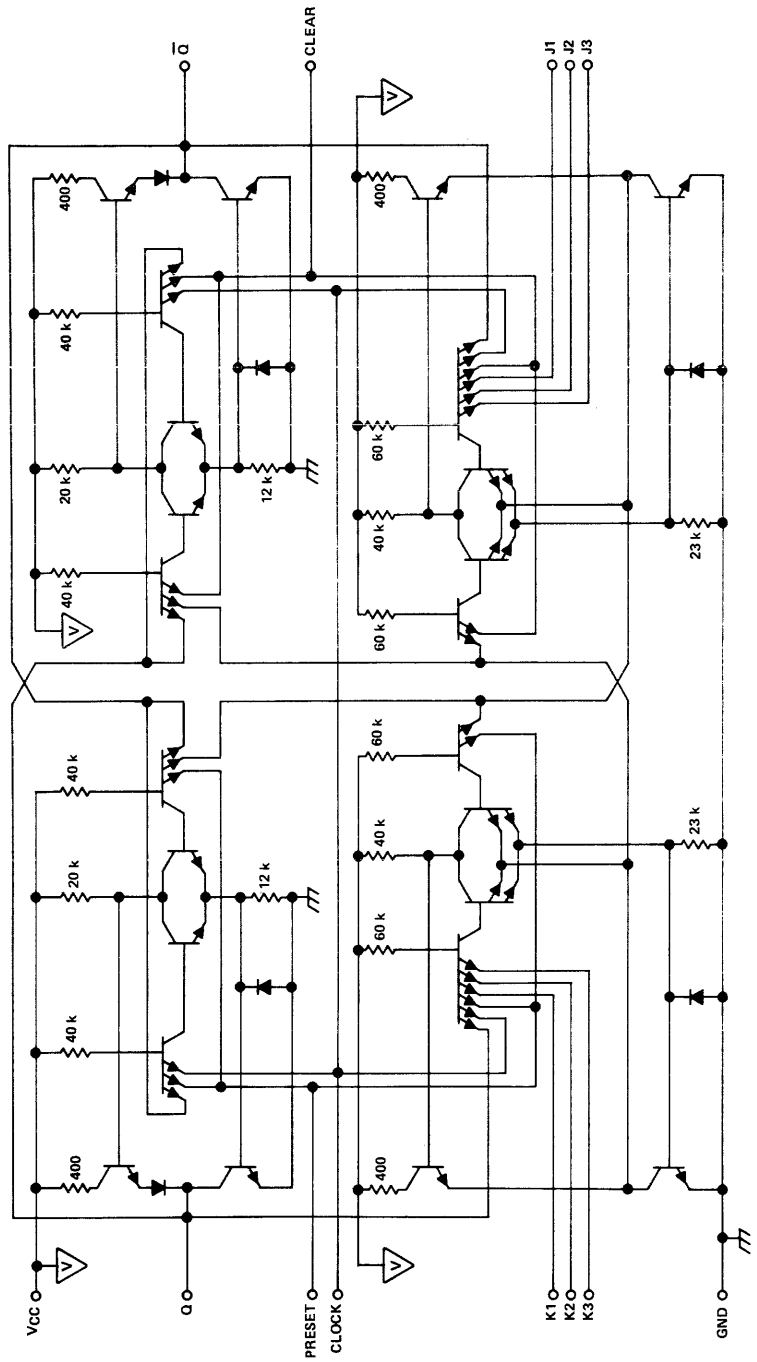
10

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	29	C_L = 50 pF, R_L = 4 kΩ		3		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from preset or clear	30				75	ns
t_{PHL}	Propagation delay time, high-to-low-level output from preset or clear					150	
t_{PLH}	Propagation delay time, low-to-high-level output from clock	29		10		75	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			10		150	

CIRCUIT TYPE RSN54L72
J-K MASTER-SLAVE FLIP-FLOP

schematic



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TEXAS INSTRUMENTS
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TRUTH TABLE

INPUT AT t_n	OUTPUTS AT t_{n+1}	
D	Q	$\overline{Q}$
L	L	H
H	H	L

H = high level, L = low level
t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse

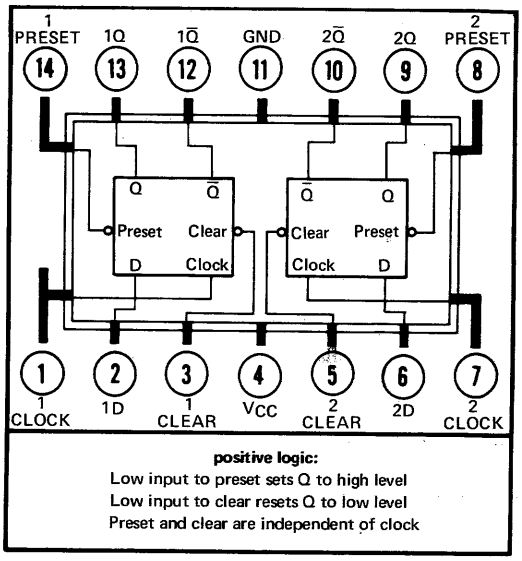
description

This monolithic, dual, low-power edge-triggered flip-flop utilizes TTL circuitry to perform D-type flip-flop logic. Each flip-flop has individual clear and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect.

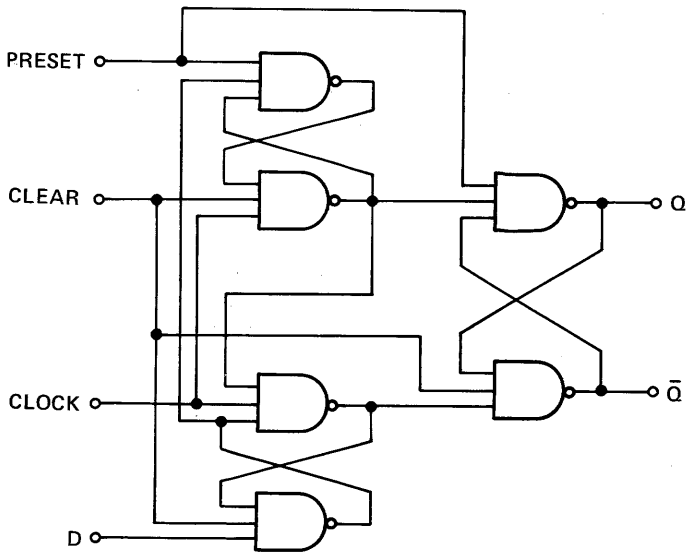
logic

H FLAT PACKAGE (TOP VIEW)



positive logic:
Low input to preset sets Q to high level
Low input to clear resets Q to low level
Preset and clear are independent of clock

functional block diagram (each flip-flop)



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CIRCUIT TYPE RSN54L74
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Normalized fan-out from each output, N			10	
Width of clock pulse, $t_{w(clock)}$	200			ns
Width of preset pulse, $t_{w(preset)}$	100			ns
Width of clear pulse, $t_{w(clear)}$	100			ns
Input setup time, t_{setup} (see Note 1)	30			ns
Input hold time, t_{hold} (see Note 2)	0			ns
Operating free-air temperature, T_A	−55		125	°C

NOTES: 1. Setup time is the interval immediately preceeding the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
2. Hold time is the interval immediately following the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
V_{IH}	High-level input voltage		23 and 24		1.9		V
V_{IL}	Low-level input voltage		23 and 24			0.8	V
V_{OH}	High-level output voltage		23	V_{CC} = MIN, V_{IH} = 1.9 V, V_{IL} = 0.8 V, I_{OH} = −100 μA	2.4		V
V_{OL}	Low-level output voltage		24	V_{CC} = MIN, V_{IH} = 1.9 V, V_{IL} = 0.8 V, I_{OL} = 2 mA		0.3	V
I_I	Input current at maximum input voltage	D input	25	V_{CC} = MAX, V_I = 5.5 V		0.1	mA
		Preset or clock				0.2	
		Clear				0.3	
I_{IH}	High-level input current	D input	25	V_{CC} = MAX, V_I = 2.4 V		10	μA
		Preset or clock				20	
		Clear				30	
I_{IL}	Low-level input current	D or preset	25	V_{CC} = MAX, V_I = 0.3 V		−0.18	mA
		Clear or clock				−0.36	
I_{OS}	Short-circuit output current		26	V_{CC} = MAX	−1	−15	mA
I_{CC}	Supply current (each flip-flop)		27	V_{CC} = MAX		1.5	mA

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†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	31 and 32	C_L = 50 pF, R_L = 4 kΩ		3		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from preset or clear	33			50	75	ns
t_{PHL}	Propagation delay time, high-to-low-level output from preset or clear				80	150	
t_{PLH}	Propagation delay time, low-to-high-level output from clock	31 and 32			60	100	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock				90	150	

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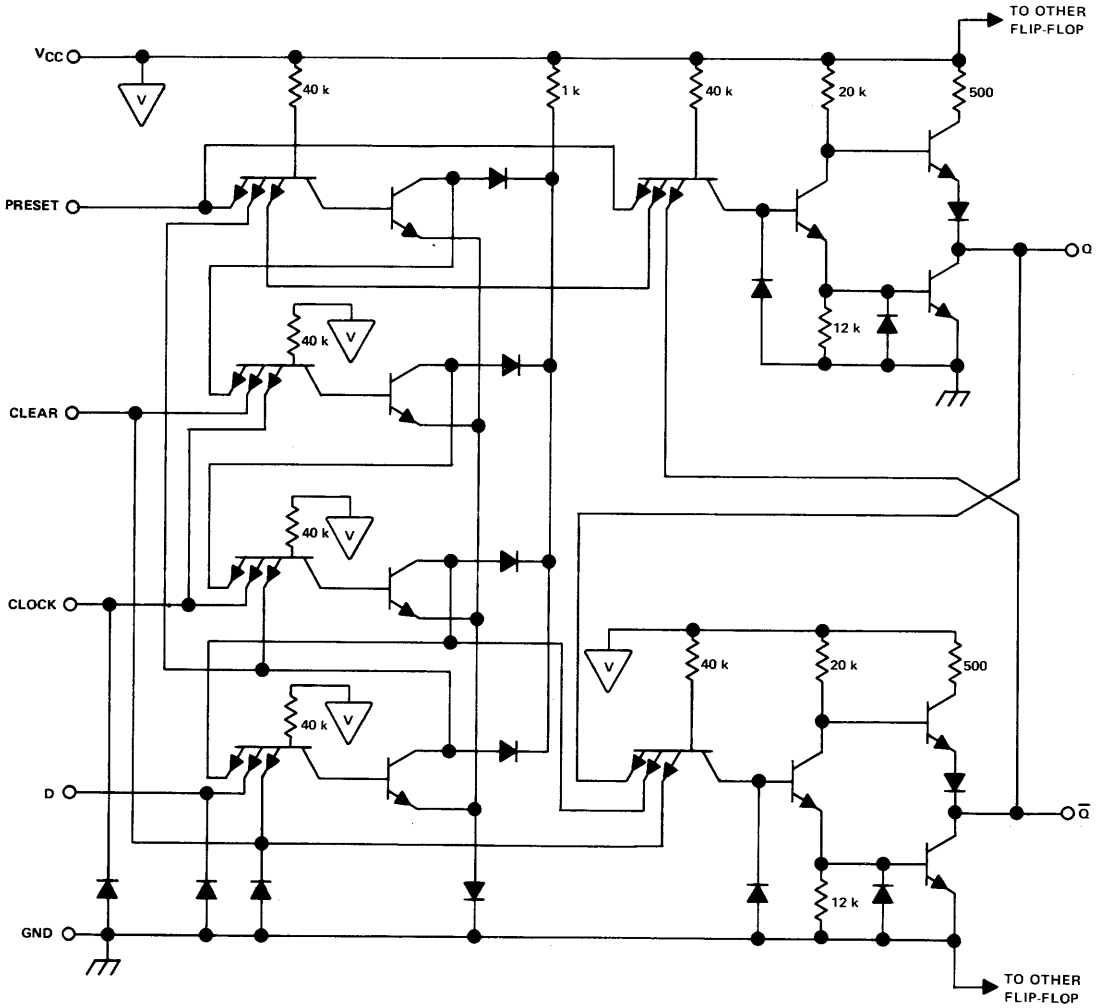
schematic

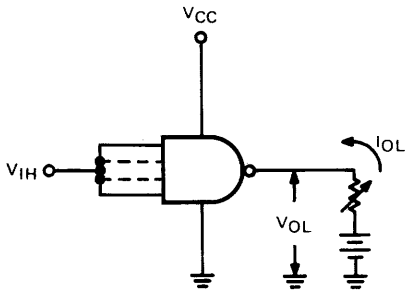


V ... V_{CC} bus
Resistor values are nominal in ohms.

10

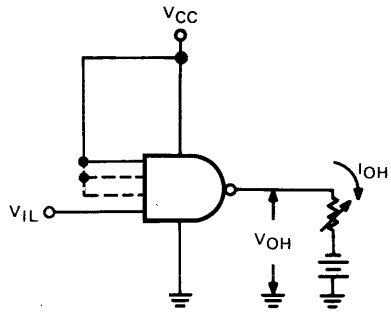
PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶



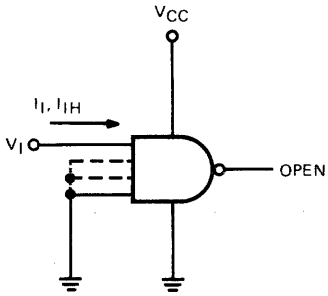
All inputs are tested simultaneously.

FIGURE 1–V_{IH}, V_{OL}



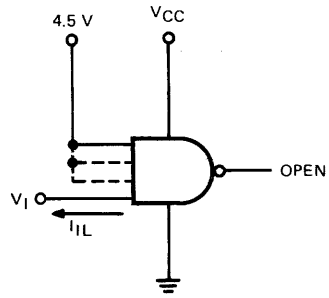
Each input is tested separately.

FIGURE 2–V_{IL}, V_{OH}



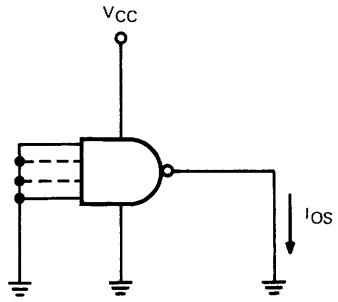
Each input is tested separately.

FIGURE 3–I_I, I_{IH}



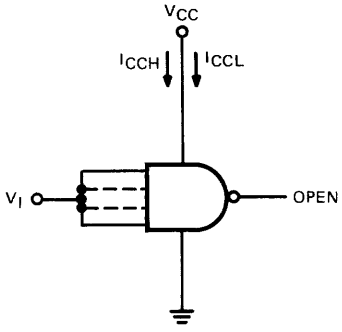
Each input is tested separately.

FIGURE 4–I_{IL}



Each gate is tested separately.

FIGURE 5–I_{OS}



All gates are tested simultaneously. Average-per-gate value = $\frac{I_{CC\ total}}{\text{number of gates in package}}$.

FIGURE 6–I_{CCH}, I_{CCL}

¶ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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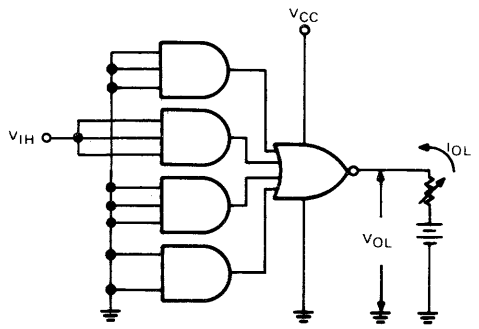
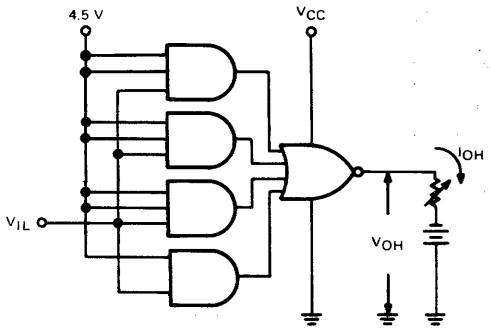
PARAMETER MEASUREMENT INFORMATION

d-c test circuits[¶] (continued)



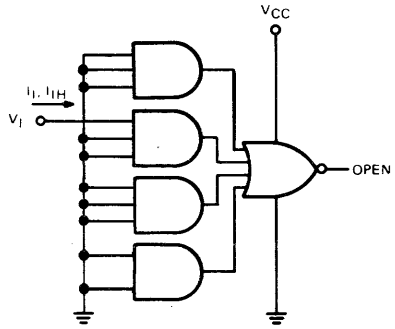
Each AND section is tested separately.

FIGURE 7–V_{IH}, V_{OL}



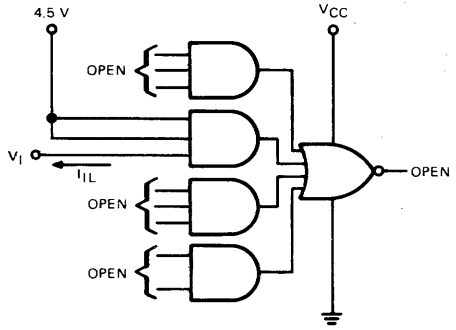
Each set of inputs is tested separately. A set comprises one input from each AND section.

FIGURE 8–V_{IL}, V_{OH}



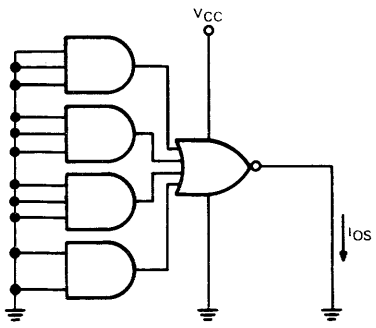
Each input is tested separately.

FIGURE 9–I_I, I_{IH}



Each input is tested separately.

FIGURE 10–I_{IL}



Each output is tested separately.

FIGURE 11–I_{OS}

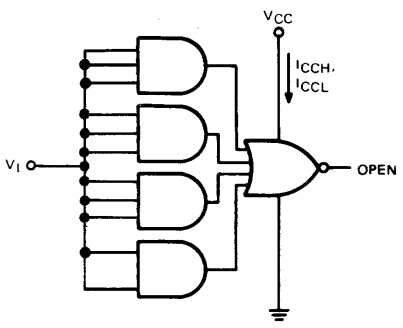


FIGURE 12–I_{CCH}, I_{CCL}

[¶] Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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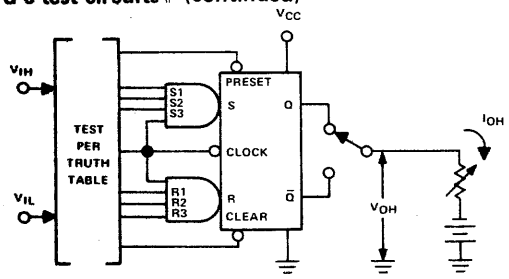
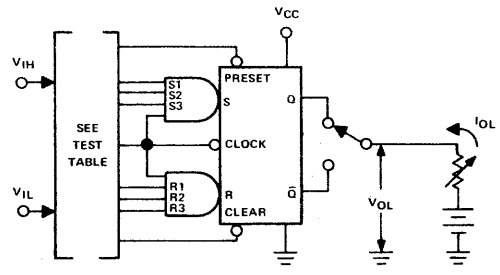
PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶ (continued)



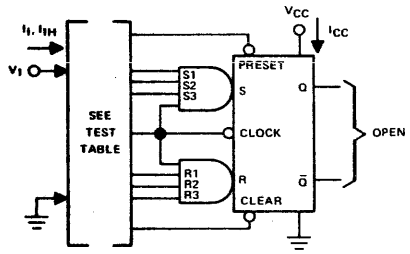
Each output is tested separately.

FIGURE 13–V_{IH}, V_{IL}, V_{OH}



Each input is tested separately.

FIGURE 14–V_{IH}, V_{IL}, V_{OL}

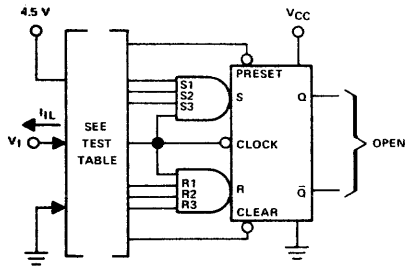


1. Each input is tested separately.
2. With all other inputs grounded, I_{CC} is measured first with clear, then preset, at 4.5 V.

TEST TABLE

APPLY V_I (TEST I_I, I_{IH})	GROUND
Clock	Preset, Clear, R1, R2, R3, S1, S2, and S3
Preset	Clock, R1, R2, and R3
Clear	Clock, S1, S2, and S3
R1	Clock, Preset, R2, and R3
R2	Clock, Preset, R1, and R3
R3	Clock, Preset, R1, and R2
S1	Clock, Clear, S2, and S3
S2	Clock, Clear, S1, and S3
S3	Clock, Clear, S1, and S2

FIGURE 15–I_I, I_{IH}, I_{CC}

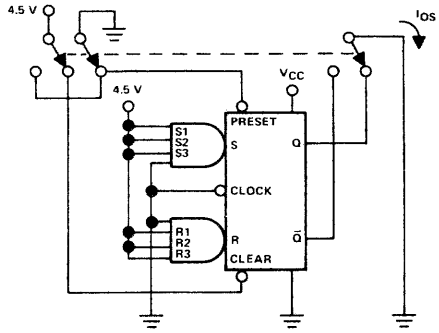


Each input is tested separately.

TEST TABLE

APPLY V_I (TEST I_{IL})	APPLY 4.5 V
Clock	Preset, R1, R2, R3, S1, S2, and S3
Clock	Clear, R1, R2, R3, S1, S2, and S3
Preset	R1, R2, R3, S1, S2, and S3
Clear	R1, R2, R3, S1, S2, and S3
R1	Preset, Clock, R2, and R3
R2	Preset, Clock, R1, and R3
R3	Preset, Clock, R1, and R2
S1	Clear, Clock, S2, and S3
S2	Clear, Clock, S1, and S3
S3	Clear, Clock, S1, and S2

FIGURE 16–I_{IL}



Each output is tested separately.

FIGURE 17–I_{OS}

¶ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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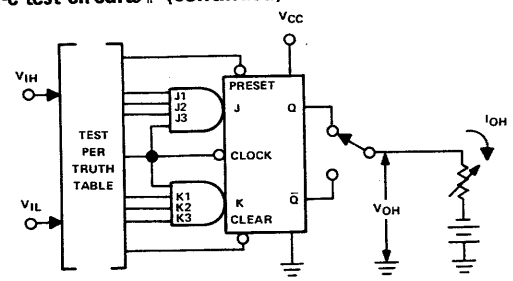
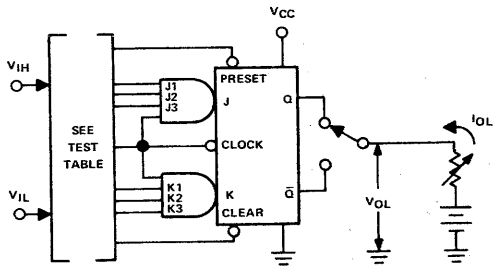
PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶ (continued)



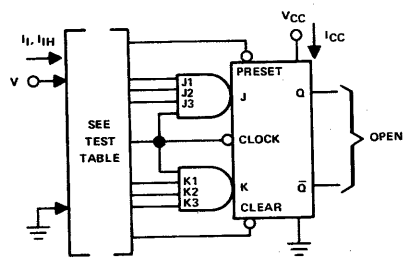
Each output is tested separately.

FIGURE 18–V_{IL}, V_{IH}, V_{OH}



Each output is tested separately.

FIGURE 19–V_{IL}, V_{IH}, V_{OL}

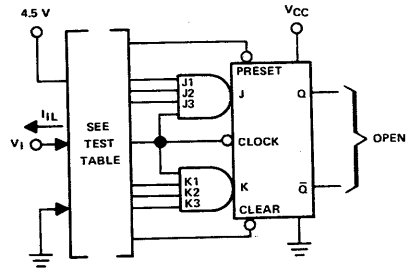


1. Each input is tested separately.
2. With all other inputs grounded, I_{CC} is measured first with clear, then preset, at 4.5 V.

TEST TABLE

APPLY V_I (TEST I_I, I_{IH})	GROUND
Clock	Preset, Clear, J1, J2, J3, K1, K2, and K3
Preset	Clock, K1, K2, and K3
Clear	Clock, J1, J2, and J3
J1	Clock, Clear, J2 and J3
J2	Clock, Clear, J1, and J3
J3	Clock, Clear, J1, and J2
K1	Clock, Preset, K2, and K3
K2	Clock, Preset, K1, and K3
K3	Clock, Preset, K1, and K2

FIGURE 20–I_I, I_{IH}, I_{CC}



Each input is tested separately.

TEST TABLE

APPLY V_I (TEST I_{IL})	APPLY MOMENTARY GND, THEN 4.5 V	APPLY 4.5 V
Clock	Preset	J1, J2, J3, K1, K2, and K3
Clock	Clear	J1, J2, J3, K1, K2, and K3
Preset	None	J1, J2, J3, K1, K2, and K3
Clear	None	J1, J2, J3, K1, K2, and K3
J1	Clear	Clock, J2, and J3
J2	Clear	Clock, J1, and J3
J3	Clear	Clock, J1, and J2
K1	Preset	Clock, K2, and K3
K2	Preset	Clock, K1, and K3
K3	Preset	Clock, K1, and K2

FIGURE 21–I_{IL}

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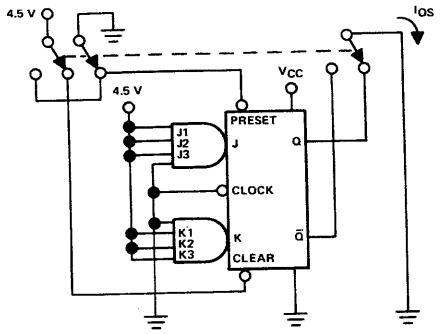


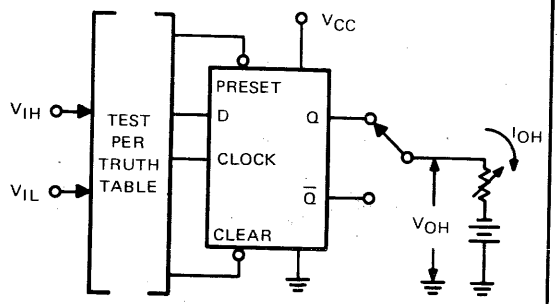
Each output is tested separately.

FIGURE 22–I_{OS}

¶ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

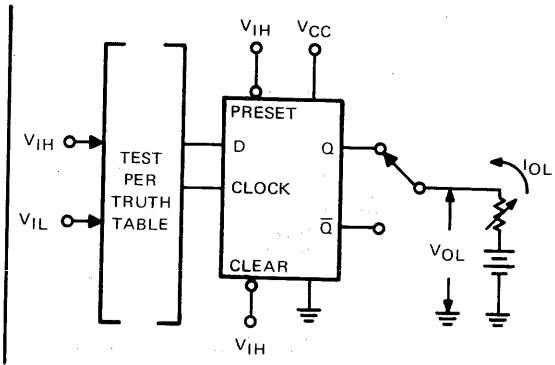
PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶ (continued)



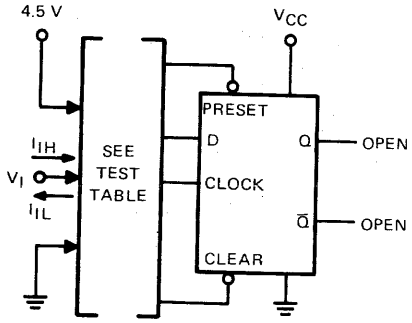
A. Each flip-flop is tested separately.
B. Each output is tested separately.
C. V_{OH} is also tested using clear and preset inputs.

FIGURE 23–V_{iH}, V_{iL}, V_{OH}



A. Each flip-flop is tested separately.
B. Each output is tested separately.

FIGURE 24–V_{IH}, V_{IL}, V_{OL}

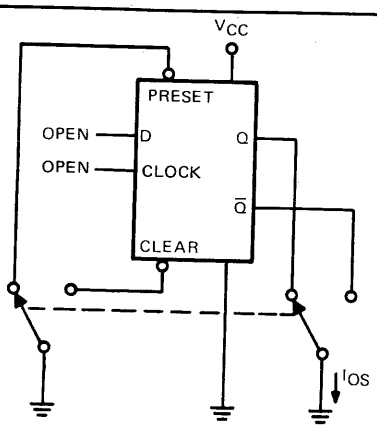


TEST TABLE

APPLY V_I MEASURE I_I, I_{IH}, I_{IL}	CONDITIONS ON OTHER INPUTS FOR I_I, I_{IH}		CONDITIONS ON OTHER INPUTS FOR I_{IL}	
	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND
Clock	Clear and D	Preset	Clear	Preset and D
Clock	Preset and D	Clear		
Preset	Clear and D	Clock (See Note B)	Clear	Clock and D
Clear	Preset	D and Clock (See Note B)	Clock, D, and Preset	None
Clear			D	Preset and Clock
D	Clock and Preset	Clear	Clock and Clear	Preset

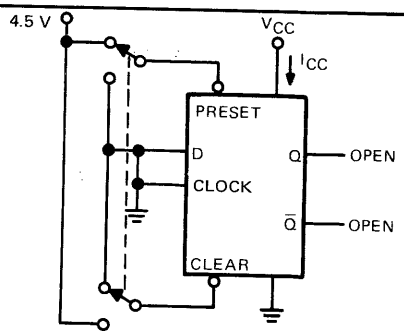
NOTES: A. Each input of each flip-flop is tested separately.
B. GND is momentarily applied to clock, then 4.5 V.

FIGURE 25–I_I, I_{IH}, I_{IL}



Each output is tested separately.

FIGURE 26–I_{OS}



I_{CC} is measured simultaneously for both flip-flops with D, clock, and preset at ground; then with D, clock, and clear at ground.

FIGURE 27–I_{CC}

¶ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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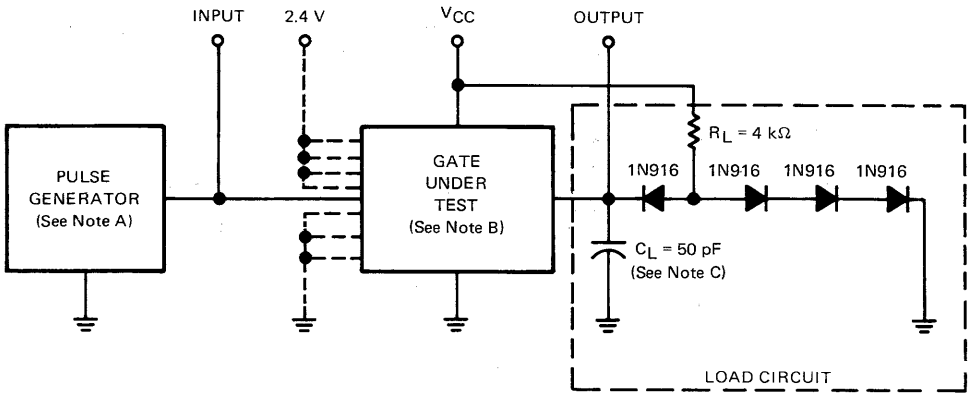
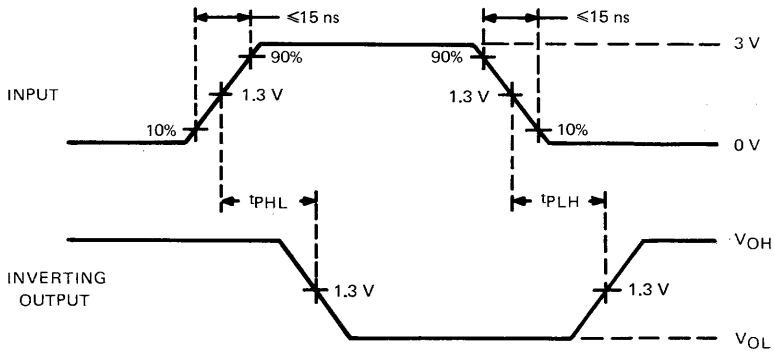
PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\ \Omega$.
B. Input conditions are established for each gate as follows:
1. Input pulse is applied to one input and 2.4 V is applied to all unused inputs of the NAND gates.
2. Input pulse is applied to one AND section, and 2.4 V is applied to all unused inputs of the AND section, and all inputs of all unused AND sections of the AND-OR-INVERT gate are grounded.
C. C_L includes probe and jig capacitance.

FIGURE 28–GATE PROPAGATION DELAY TIMES

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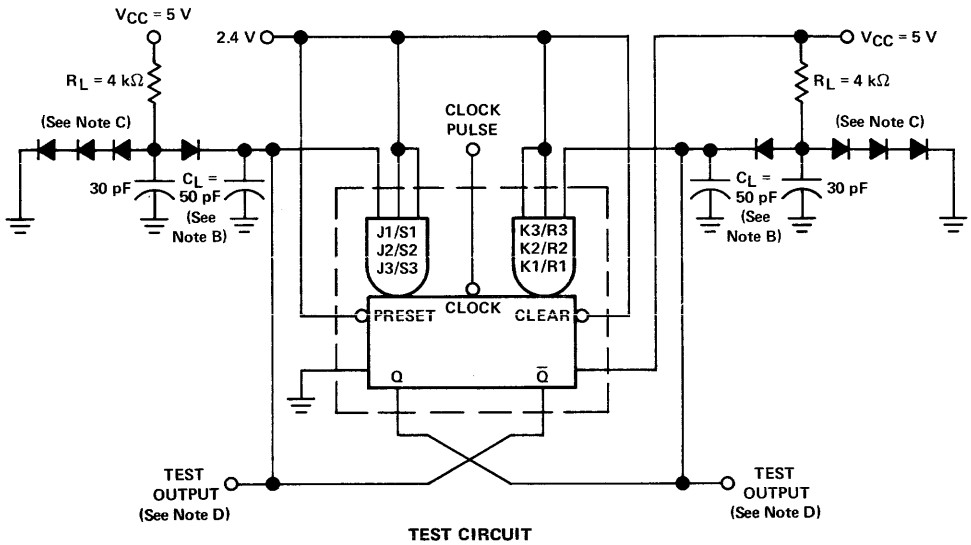
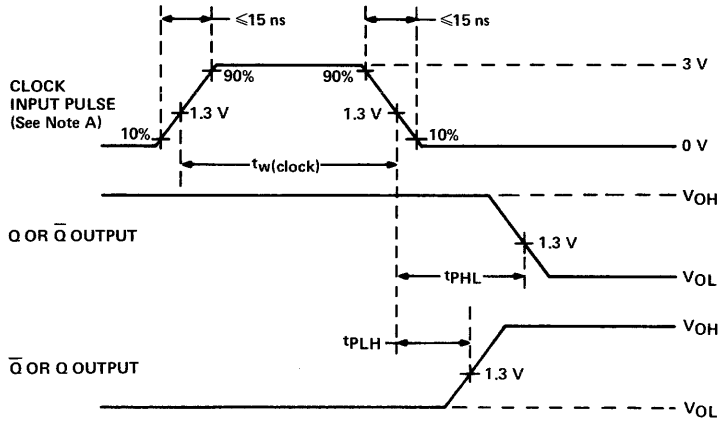
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. Clock input characteristics: t_w = 200 ns, and PRR = 500 kHz. When testing f_{max}, vary PRR.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916.
D. Load is applied only to output under test.

FIGURE 29–S-R AND J-K FLIP-FLOP SWITCHING TIMES FROM SYNCHRONOUS INPUTS

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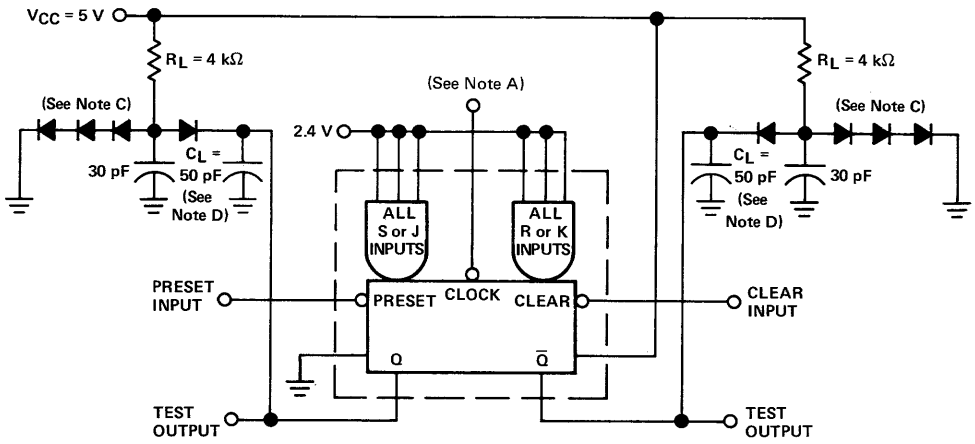
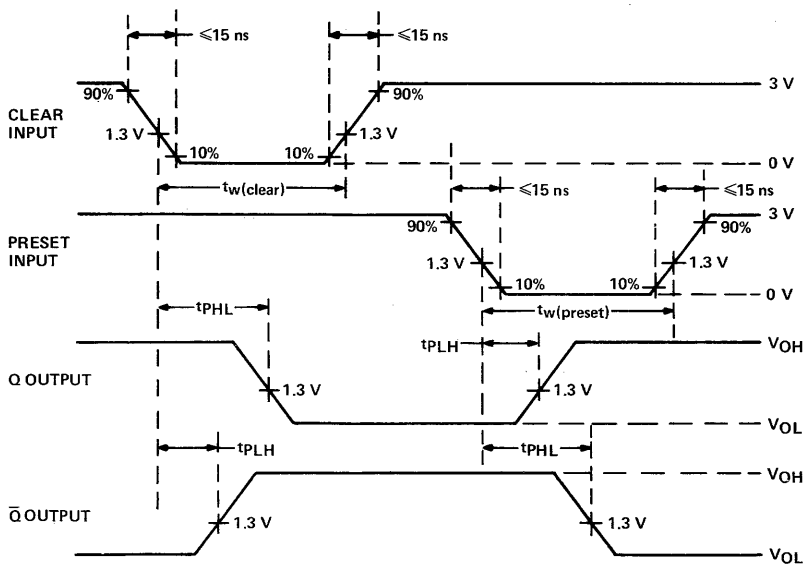
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. Clear or preset inputs dominate regardless of the state of clock or logic inputs.
B. Clear or preset input pulse characteristics: $t_{w(clear)}$ = 100 ns, $t_{w(preset)}$ = 100 ns, and PRR = 500 kHz.
C. All diodes are 1N916.
D. C_L includes probe and jig capacitance.

FIGURE 30–S-R AND J-K FLIP-FLOP SWITCHING TIMES FROM ASYNCHRONOUS INPUTS

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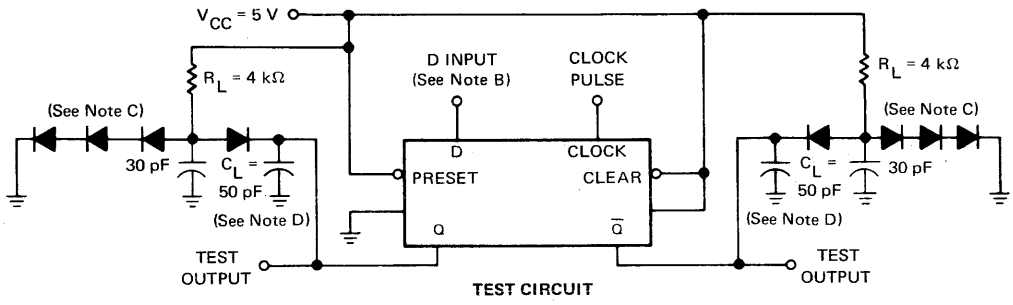
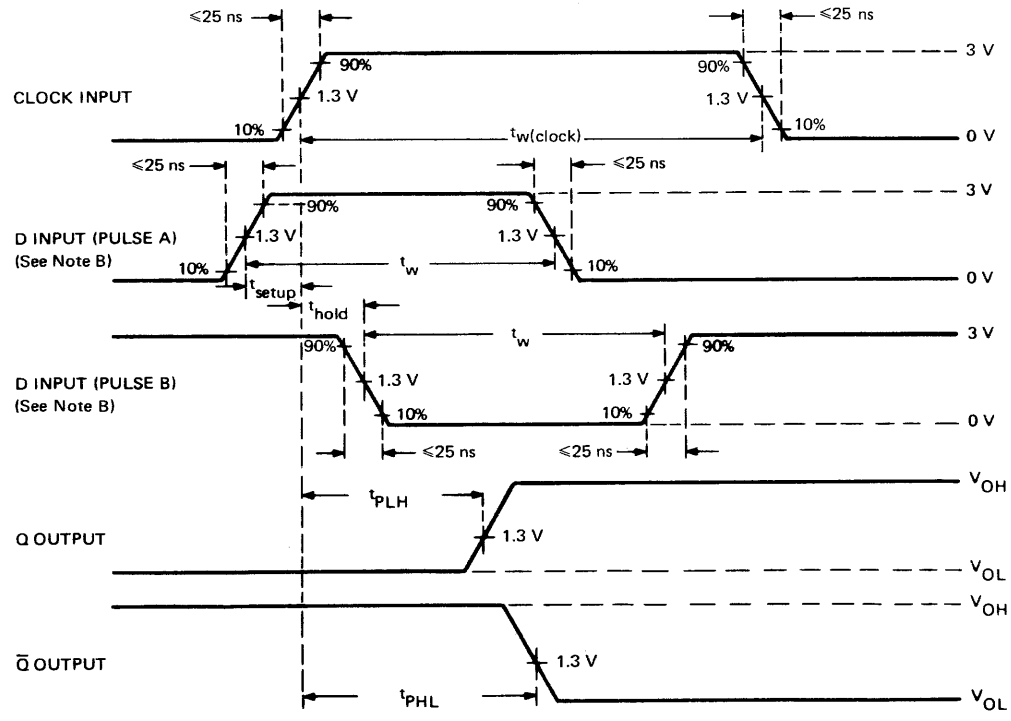
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. Clock input pulse has the following characteristics: $t_{w(clock)}$ = 200 ns and PRR = 500 kHz. When testing f_{max}, vary PRR.
B. D input (pulse A) has the following characteristics: t_{setup} = 30 ns, t_w = 100 ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: t_{hold} = 0 ns, t_w = 80 ns, and PRR is 50% of the clock PRR.
C. All diodes are 1N916.
D. C_L includes probe and jig capacitance.

FIGURE 31–SWITCHING CHARACTERISTICS, CLOCK AND SYNCHRONOUS INPUTS (HIGH-LEVEL DATA)

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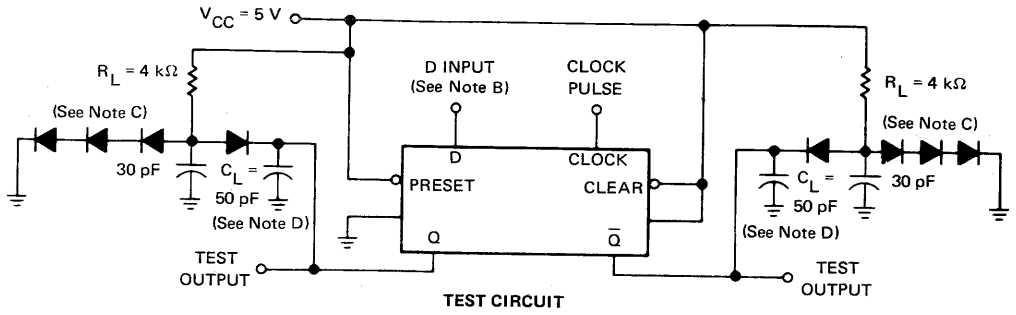
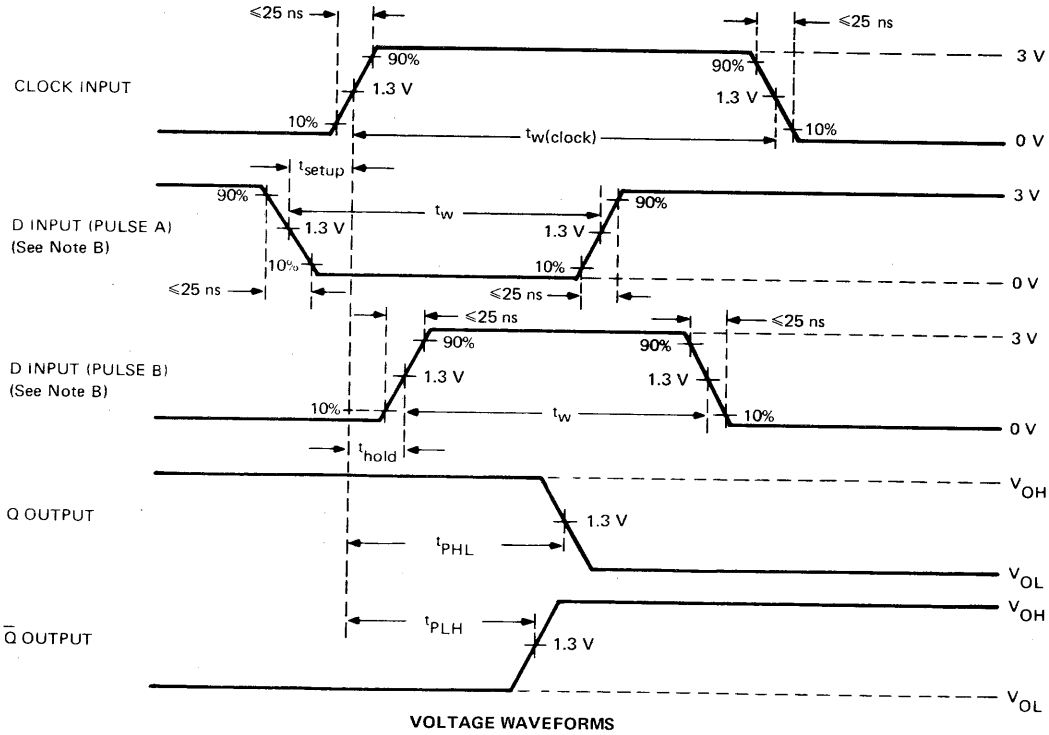
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. Clock input pulse has the following characteristics: t_w = 200 ns and PRR = 500 kHz. When testing f_{max}, vary PRR.
B. D input (pulse A) has the following characteristics: t_{setup} = 30 ns, t_w = 100 ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: t_{hold} = 0 ns, t_w = 80 ns, and PRR is 50% of the clock PRR.
C. All diodes are 1N916.
D. C_L includes probe and jig capacitance.

FIGURE 32–SWITCHING CHARACTERISTICS, CLOCK AND SYNCHRONOUS INPUTS (LOW-LEVEL DATA)

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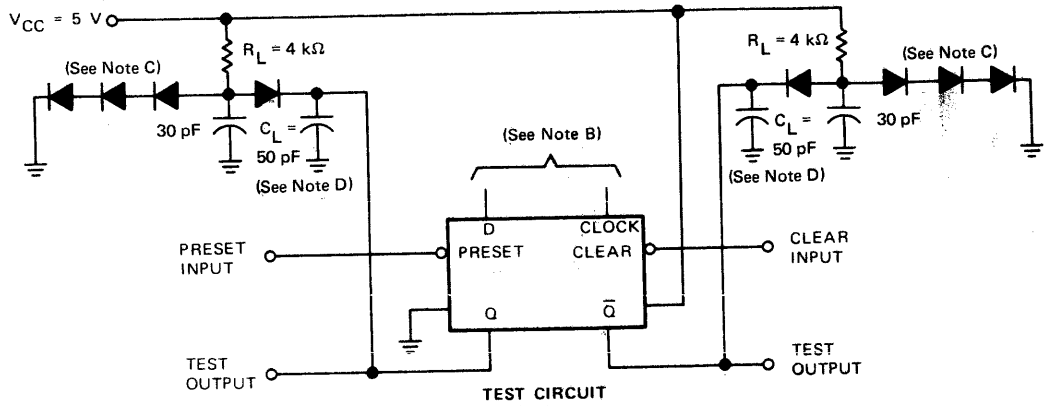
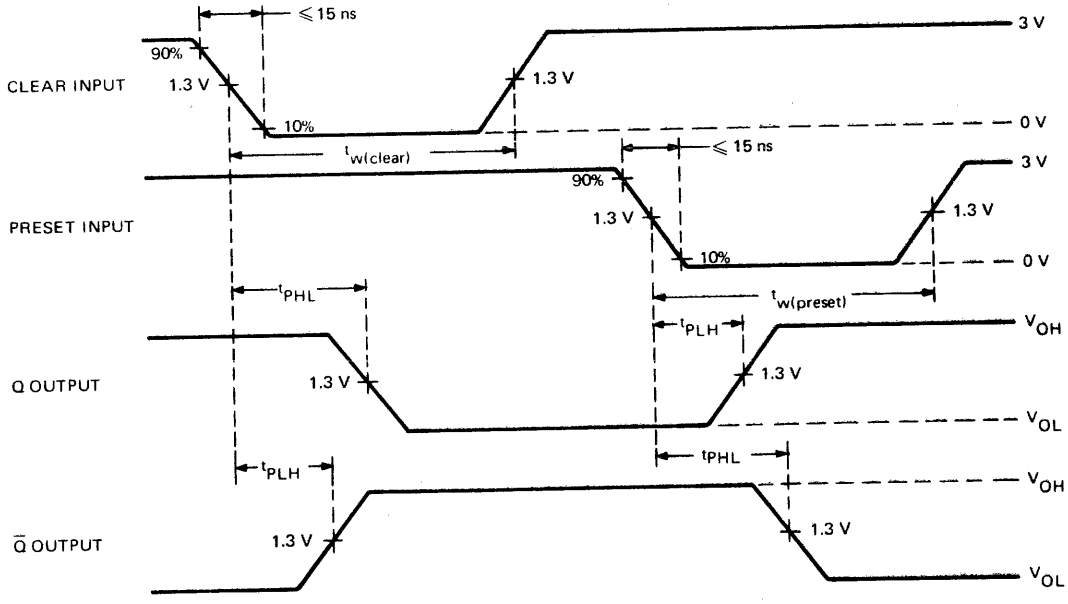
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. Clear or Preset input pulse characteristics: $t_{w(clear)} = t_{w(preset)} = 100$ ns, PRR = 500 kHz.
B. Clear and Preset inputs dominate regardless of the state of Clock or D inputs.
C. All diodes are 1N916.
D. C_L includes probe and jig capacitance.

FIGURE 33–ASYNCHRONOUS INPUTS SWITCHING CHARACTERISTICS

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RSN55900—DUAL-CHANNEL PREAMPLIFIER
RSN55910—SWITCHED BUFFER
RSN55920—D-C COUPLED 4-CHANNEL SENSE AMPLIFIER

RSN55900 electrical characteristics at 25°C free-air temperature

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
I_{IB}	Input bias current				25	μA
I_{SL}	Low-level strobe current	V_S = 0 V			4	mA
A_{VD}	Large-signal differential voltage amplification	V_{ID} = 10 mV	100		200	
V_{OPP}	Maximum peak-to-peak output voltage swing		7			V
V_{OC}	Common-mode output voltage	V_I = 0 V	5		7	V
I_{CC1}	Supply current from V_{CC1}	V_{CC1} = 12 V			12	mA
I_{CC2}	Supply current from V_{CC2}	V_{CC2} = 5 V			15	mA
I_{EE}	Supply current from V_{EE}	V_{EE} = −10 V			−17	mA
t_{PLH}	Propagation time, low-to-high-level output			15		ns

RSN55910 electrical characteristics at 25°C free-air temperature

PARAMETER		SUPPLY MODE	CONDITIONS	MIN	MAX	UNIT
$V_{OH(\bar{Y})}$	High-level $\bar{Y}$ output voltage	1	V_{ID} = 40 mV	4.5		V
		2	V_{ID} = 85 mV	4.5		
$V_{OL(\bar{Y})}$	Low-level $\bar{Y}$ output voltage	1	V_{ID} = 300 mV		0.5	V
		2	V_{ID} = 400 mV		0.5	
I_{CC1}	Supply current from V_{CC1}	1	V_{CC1} = 12 V		5	mA
I_{CC2}	Supply current from V_{CC2}	1	V_{CC2} = 5 V		20	mA
I_{EE}	Supply current from V_{EE}	1	V_{EE} = −10 V		−17	mA
$t_{PHL(\bar{Y})}$	Propagation time, high-to-low-level $\bar{Y}$ output	1		8	28	ns
		2		8	35	
$t_{PLH(\bar{Y})}$	Propagation time, low-to-high-level $\bar{Y}$ output	1		10	45	ns
		2		10	46	

SUPPLY MODE	V_{CC1}	V_{CC2}	V_{CC3}	V_{EE}
1	12 V	5 V	OPEN	−10 V
2	GND	5 V	5 V	−10 V

All voltage values, except differential voltages, are with respect to the network ground terminal.

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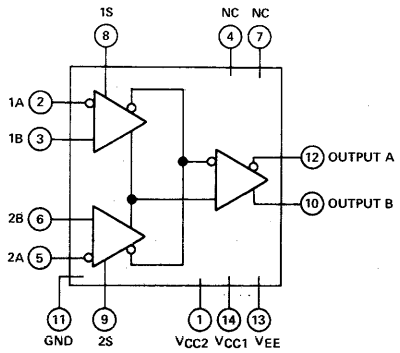
RSN55920 electrical characteristics at 25°C free-air temperature

PARAMETER		CONDITIONS	MIN	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1.4 V		2.5	mV
I_{IB}	Input bias current			100	μA
I_{SL}	Low-level strobe current	V_S = 0 V		1.38	mA
V_{OH}	High-level output voltage	V_{ID} = 50 mV	2.4		V
V_{OL}	Low-level output voltage	V_{ID} = −50 mV		0.45	V
I_{CC}	Supply current from V_{CC}	V_{CC} = 5.5 V		30	mA
I_{EE}	Supply current from V_{EE}	V_{EE} = −6.6 V		−19	mA

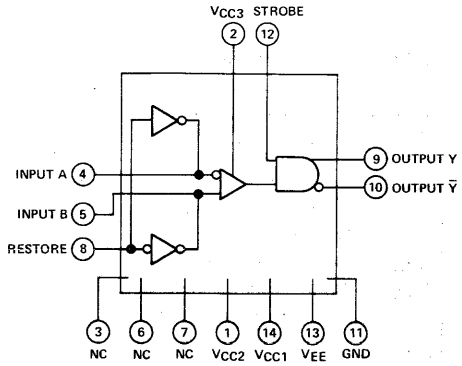
†All radiation tolerant integrated circuits are supplied in H flat packages. See Section 1 for dimensional drawings.

PRELIMINARY DATA: Supplementary data will be published at a later date.

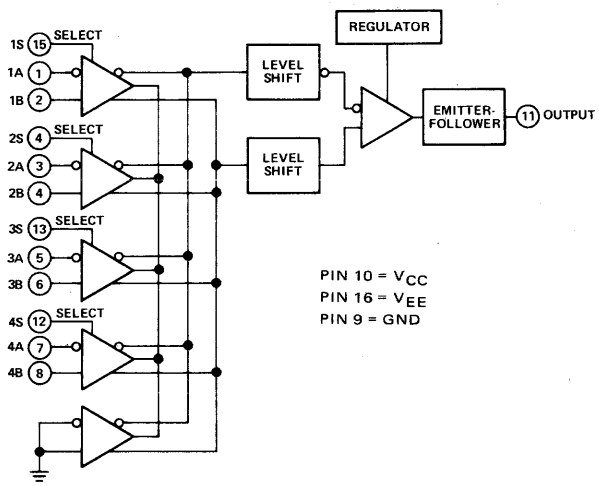
functional logic diagrams



RSN55900



RSN55910



RSN55920

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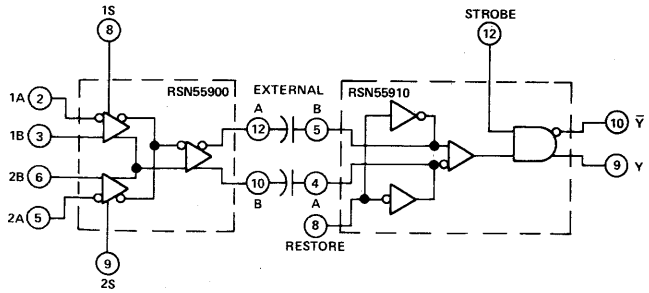
TYPICAL APPLICATION DATA



PIN	MIN	NOM	MAX
1	4.5 V	5 V	5.5 V
14	10.8 V	12 V	13.2 V
13	−11 V	−10 V	−9 V

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RADIATION TOLERANT DTL

These radiation-tolerant circuits are electrically similar to and functionally interchangeable with their Series 15930‡ counterparts. The terminal assignments are the same. They are mounted in the 14-pin H ceramic package and are intended for operation over the full military range of –55°C to 125°C.

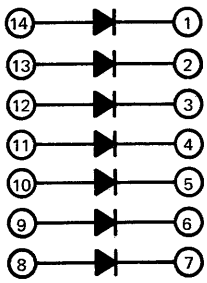
TYPE	FUNCTION
RSN15930	Expandable Dual 4-Input NAND Gate
RSN15932	Expandable Dual 4-Input NAND Buffer Gate
RSN15944	Expandable Dual 4-Input NAND Power Gate
RSN15945	J-K/R-S Flip-Flop
RSN15962	Triple 3-Input NAND Gate

typical characteristics at 25°C free-air temperature

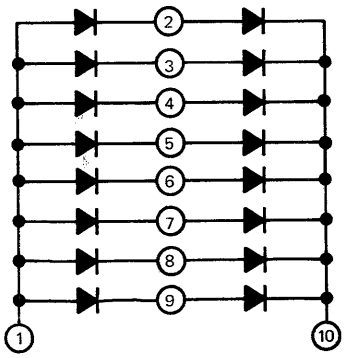
Propagation delay time	25 ns
Power dissipation	12 mW
D-c noise immunity	750 mV

RADIATION TOLERANT DIODE ARRAYS

RSN14925
7-DIODE ARRAY
14-PIN PACKAGE



RSN14097
16-DIODE ARRAY
10-PIN PACKAGE



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electrical characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)}$	Reverse Breakdown Voltage	I_R = 10 μA	40			V
I_R	Static Reverse Current	V_R = 40 V			500	nA
V_F	Static Forward Voltage	I_F = 500 mA			1.5	V
		I_F = 100 mA	0.7		1	
C_T	Total Capacitance	V_R = 0, f = 1 MHz		12		pF

†All radiation tolerant devices are supplied in H flat packages. See Section 1 for dimensional drawings.
‡Refer to Section 11 for more complete data on Series 15930.

PRELIMINARY DATA:
Supplementary data will be published at a later date.

LINEAR INTEGRATED CIRCUIT

CIRCUIT TYPE RSN52709 RADIATION-HARDENED HIGH-PERFORMANCE OPERATIONAL AMPLIFIER

featuring

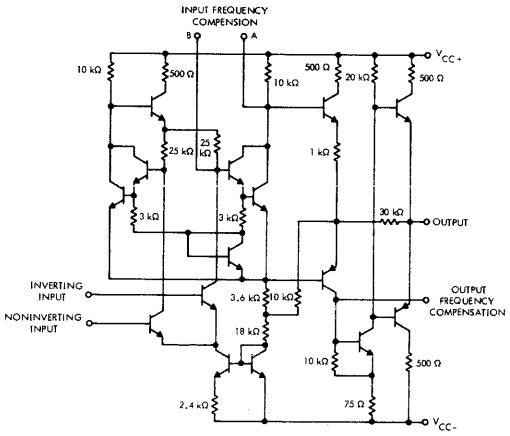
HIGH TOLERANCE TO GAMMA AND NEUTRON IRRADIATION

- **Input Voltage Range . . . ±8 V Min**
- **Maximum Peak-to-Peak Output Voltage Swing . . . 20 V Min**

description

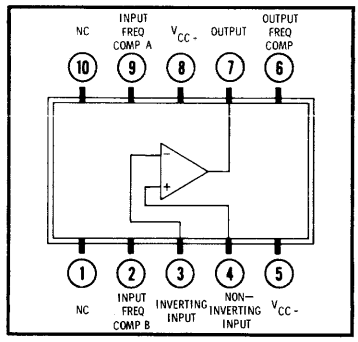
The RSN52 709 circuit is a radiation-hardened, high-performance operational amplifier specifically designed and fabricated for operation and survivability in a nuclear environment. Small-geometry transistors, shallow base diffusions, component matching, dielectric isolation, and thin-film resistors are utilized to improve performance and minimize sensitivity to gamma and neutron irradiation. Provisions are incorporated within the circuit whereby external components may be used to compensate the amplifier for stable operation under various feedback or load conditions. Definitive specifications are provided for electrical characteristics over the full military temperature range of -55°C to 125°C. Data on changes in device performance characteristics resulting from exposure to gamma or neutron irradiation is available at Texas Instruments upon demonstration of need-to-know and applicable security credentials.

schematic and terminal assignments



Component values shown are nominal.

H FLAT PACKAGE (TOP VIEW)



NC—No internal connection

For ordering instructions and mechanical data, refer to Section 1.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltages (See Note 1): V_{CC+} . . . . . 18 V
V_{CC-} . . . . . -18 V
Differential input voltage . . . . . ±5 V
Input voltage (either input, See Note 1) . . . . . ±10 V
Duration of short-circuit output current (T_A = 25°C) . . . . . 5 s
Continuous total power dissipation at (or below) 100°C free-air temperature (See Note 2) . . . . . 250 mW
Operating free-air temperature range (See Note 2) . . . . . -55°C to 125°C
Storage temperature range . . . . . -65°C to 150°C

NOTES: 1. These voltage values are with respect to the zero reference level of the supply voltage.
2. Derate linearly to 125°C free-air temperature at the rate of 5 mW/°C.

voltages specified

Unless otherwise noted, supply voltages specified in the following tables are V_{CC} = 9 V to 15 V, where a positive voltage within the specified range or of the specified value is applied to V_{CC+} and an equal negative voltage is applied to V_{CC-}. Unless otherwise noted, all voltages except V_{IO} are with respect to the zero reference level (ground) of the supply voltages.

electrical characteristics (unless otherwise noted, V_{CC} = 9 V to 15 V, T_A = 25°C)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IO}	Differential-input offset voltage	$R_s \leq 10$ kΩ,	T_A = -55°C to 125°C			6	mV
		$R_s \leq 10$ kΩ			1	5	mV
α_{VIO}	Differential-input offset voltage temperature coefficient	R_s = 50 Ω,	T_A = -55°C to 125°C		3		μV/°C
		$R_s \leq 10$ kΩ,	T_A = -55°C to 125°C		6		μV/°C
I_{IB}	Input bias current	V_{CC} = 15 V			100	500	nA
		V_{CC} = 15 V,	T_A = -55°C		120	1500	nA
I_{IO}	Differential-input offset current		T_A = 125°C		20	200	nA
					25	200	nA
			T_A = -55°C		30	500	nA
I_{IR}	Input reverse current	V_{ID} = 5 V				5	μA
V_{OPP}	Maximum peak-to-peak output voltage swing	V_{CC} = 15 V,	$R_L \geq 10$ kΩ, T_A = -55°C to 125°C	24			V
		V_{CC} = 15 V,	$R_L \geq 2$ kΩ, T_A = -55°C to 125°C	20			V
V_I	Input voltage range	V_{CC} = 15 V,	T_A = -55°C to 125°C	±8			V
A_{VD}	Large-signal open-loop differential voltage gain	V_{CC} = 15 V, V_O = ±10 V,	$R_L \geq 2$ kΩ, T_A = -55°C to 125°C	20,000	40,000‡	70,000	
CMRR	Common-mode rejection ratio	$R_s \leq 10$ kΩ,	T_A = -55°C to 125°C	70	90‡		dB
r_i	Input resistance		T_A = -55°C	40	100		kΩ
				150	400		kΩ
r_o	Output resistance				150		Ω
$\Delta V_{IO}/\Delta V_{CC}$	Supply voltage sensitivity	$R_s \leq 10$ kΩ,	T_A = -55°C to 125°C		25‡	150	μV/V
P_D	Total power dissipation	V_{CC} = 15 V,	V_O = 0		80	165	mW

† All typical values are at V_{CC} = 15 V.
‡ These typical values are at T_A = 25°C.

transient response, V_{CC} = 9 V to 15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_r	Rise time	V_{in} = 20 mV,	C_L = open			1.5	μs
	Overshoot	V_{in} = 20 mV,	$C_L \leq$ 100 pF			30%	

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