4

ECL Circuits

ECL INDEX
NUMERIC

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ultra-high speed: 2-3 ns

The ECL2500 Series is a compatible catalog family of ultra-high-speed (2-3 ns) ECL functions designed to fulfill the integrated-circuit requirements of next-generation computer systems. Twenty-eight device types perform both multifunction and complex logic, storage, and interface functions (up to 13 gates/package), all of which are offered in the economical industry-standard 16-pin plastic dual-in-line package.

summary of functions

	Gates/Pkg	Number of Types	Remarks
Logic			
Basic Gates and Multifunction Gates	1-6	18	Complementary Outputs High Fan-in High Fan-out Dotted Inputs/Outputs Multi-Output
Arithmetic and Decoder	5-12	3	Full Adder 3-Bit Decoder 5-Bit Group Carry
Interface			
Line Driver	2	1	Drives Two 50-Ω Lines
Line Receiver	2	1	High CMRR
High-Level-to-ECL Converter	2	1	Compatible with TTL, DTL, RTL
ECL-to-High-Level Converter	2	1	
Storage			
Multifunction Latch	4	1	Single-input gated
Complex Latch	9-13	2	2-input gated
Total Compatible Functions		28	

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absolute maximum ratings

Power Supply Voltage (V_{CC} to V_{EE})	6 V
Input Voltage (V_{in} @ V_{BB} = 0.0 V)	± 2 V
Output Source Current	40 mA d-c
Storage Temperature Range	−40°C to 150°C

recommended operating conditions

V_{CC} (Pin ③ and/or Pin ⑥)	1.32 V
V_{BB} (Pin ⑮)	OV (Gnd)
V_{EE} (Pin ⑩)	-3.2 V
Operating Temperature Range	0° to 75° C
System Impedance	50 Ω

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electrical characteristics of basic ECL gate

Test Conditions: V_{CC} = 1.32 V, V_{BB} = 0, V_{EE} = −3.2 V, T_A = 25°C

			Typical
Fan-out			1-10
Speed	Fan-out = 1	t_t (10% – 90% pts)	2.8 ns
		t_p (50% pts)*	2.3 ns
	Fan-out = 10	t_t *	4.3 ns
		t_p *	3.5 ns
Power Dissipation/Gate		Unterminated, P_{DU}	30 mW
		Terminated, P_{DT} **	60 mW
Logic Levels:			
	Logical "1"		400 mV
	Logical "0"		−400 mV
Noise Margin			200 mV

*See switching waveforms in figure 6.
**Complementary outputs driving 50 Ω to Gnd and 270 Ω to -3.2 V.

basic ECL gate

The basic ECL gate configuration is shown in figure 1. The high-speed performance results from the nonsaturating operation of the high-f_T transistor current switches. The high impedance of the load (input to differential amplifier) coupled with the low impedance of the driving source (emitter-follower output) allows high d-c fan-out. High-speed operation and high a-c fan-out are possible because all circuits are designed to operate in a 50-Ω system. When high-speed operation is a requirement, it is recommended that terminated 50-Ω transmission lines be utilized to interconnect circuits.

The basic ECL gate design of the ECL2500 Series provides both the output function Y and its complement Z; however, to maximize logic capability, some modules have only one output.

To minimize the number of packages to implement a system, and to reduce external connections, many units in the ECL2500 Series include logical connections between gates within the package. In-phase collector dotting (positive AND logic), out-of-phase emitter dotting (positive OR logic), and multiple inputs common to one package pin have been utilized to provide a very comprehensive logic family. An example of output dotting within the package is shown in figure 2. The positive logic WIRED-AND function is achieved by connecting in-phase collectors and the incorporation of an up-level clamp transistor. The positive logic WIRED-OR function within the package is accomplished by connecting out-of-phase-emitter-follower outputs. This inherent logic flexibility provides the system designer with a logic family with 1.6 times the logic/module density of conventional digital logic families.

figure 1. ECL gate

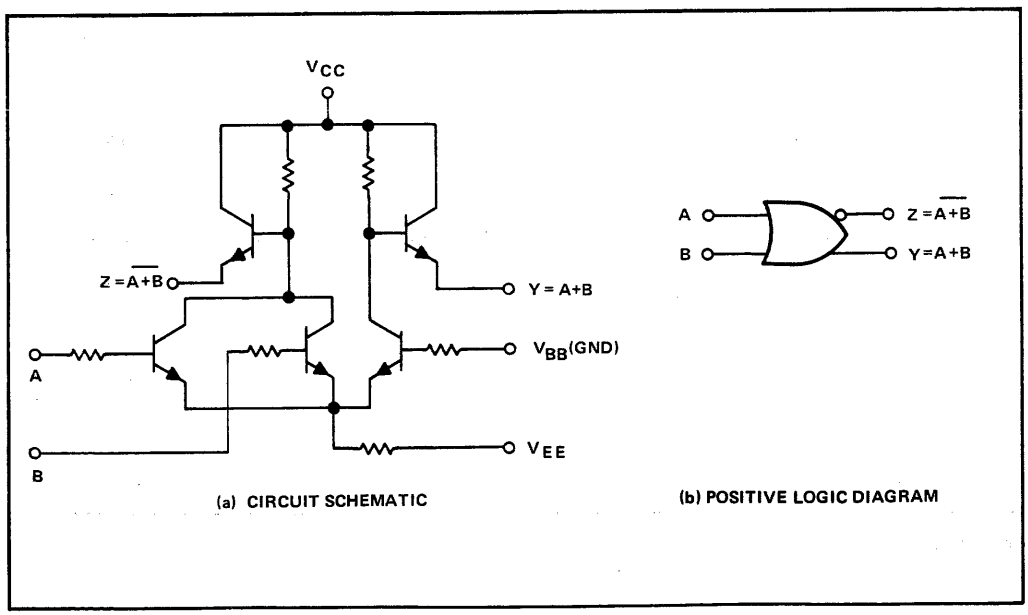

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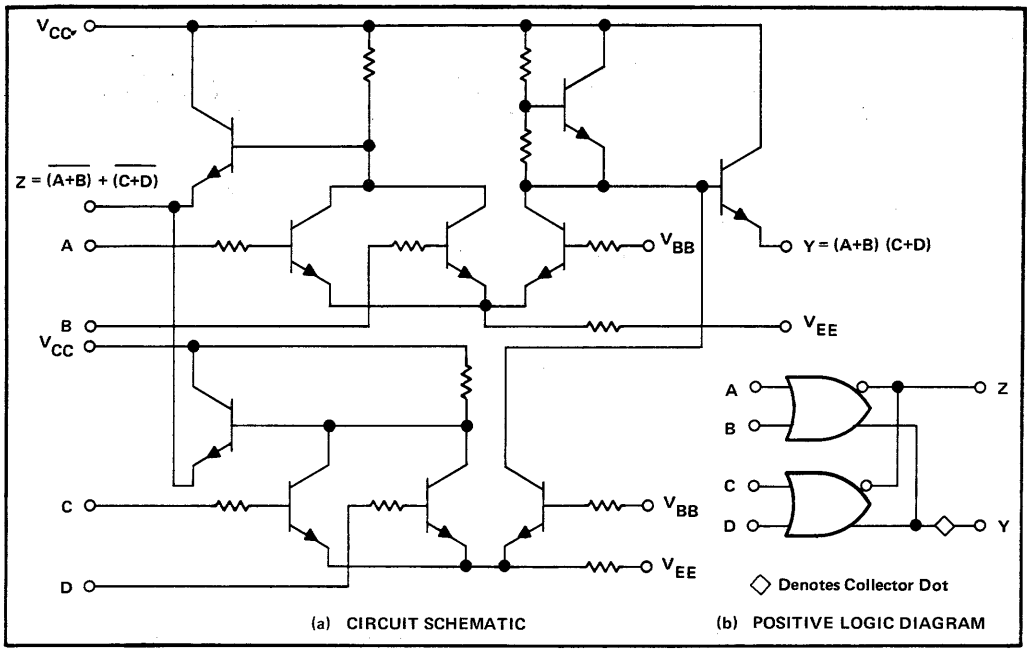
figure 2. ECL output dotting



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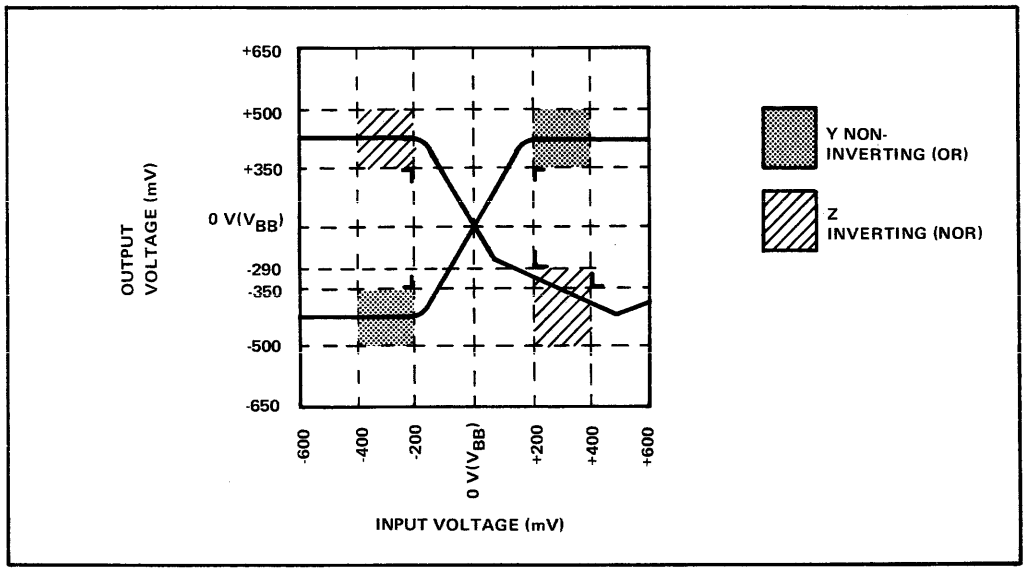
logic levels

Typical logic levels for the basic gate are 400 mV for a logical "1" and -400 mV for a logical "0" when operating with V_{CC}= 1.32 V, V_{EE}= −3.2 V, and V_{REF}= 0 V. Minimum levels when operating at 25° C free-air temperature and loaded with 50 Ω to ground and 270 Ω pulldown to −3.2 V are ± 350 mV. These logic levels are ensured with inputs at ±200 mV which provide 150 mV of d-c noise margin. Since the actual threshold is approximately 150 mV and typical output levels are 400 mV, typical d-c noise margin in excess of 200 mV can be expected. Transfer characteristics for the basic gate are shown in figure 3.

For gating functions which have emitter dots or parallel emitter followers, up levels will be increased by 50 mV to 450 mV. Likewise, down levels will increase by a similar amount to -350 mV.

figure 3. transfer characteristics-basic ECL gate



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loading

To minimize package dissipation and to permit the external WIRED-OR (positive logic) function, the emitter-follower outputs have been left unterminated. The emitter-follower output is capable of driving a load of up to 25 mA d-c, but requires an externally provided negative voltage source and termination. The recommended termination includes a 270-Ω resistive load (pulldown) to V_{EE} (−3.2 V) and 50 Ω to V_{BB} (GND). To utilize the high-speed characteristics (≈ 2-ns switching speeds) of the ECL2500 Series, transmission lines or other controlled-impedance systems should be utilized to accomplish interconnections. The 50 Ω to ground provide proper termination when a 50-Ω transmission line is used.

When operating in a controlled-impedance interconnection system, two general classes of fan-out loading are permitted. The first (cluster loading) involves loads which can be connected within two inches from any source (output). The measurement is made between package pins. (Seating plane is used as a reference point.) These loads, called source stubs, are treated as lumped-capacitance loads which increase switching times but cause no reflection problems.

Since ECL circuit outputs may be directly wired together (emitter "dotted") to provide an OR (positive logic) function, cluster loading constraints apply to each of the sources making up the WIRED-OR. Up to ten such outputs may be "dotted" provided no two are more than two inches apart.

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A second class of fan-out loading is commonly referred to as distributive loading. Such loads are greater than two inches from any source as measured between package pins (seating plane is used as reference point). These loads must be treated as lumped loads along a transmission line. The logic levels and switching speeds of the ECL2500 Series permit a maximum lumped load of 20 pF with less than a 20 per cent reflection coefficient for a 50-Ω printed-circuit line (e_r = 4.5). However, these loads must be 4.5 inches or more apart. Smaller lumped loads may be spaced closer together provided no more than 20 pF exists along any 4.5 inches of line measured outside the two-inch source stub.

Lumped loads may consist of circuit (gate) input capacitance and stub capacitance if used. Capacitances due to circuit inputs are ≈ 5.0 pF per input, while that attributed to stubs is dependent on the type of transmission line used. Figure 4 shows a typical distributive-loading arrangement.

Both cluster and distributive loads may be employed separately or in combination. Termination resistors for a load configuration involving only a cluster may be placed where convenient, but any other configuration requires termination at the end of the transmission line.

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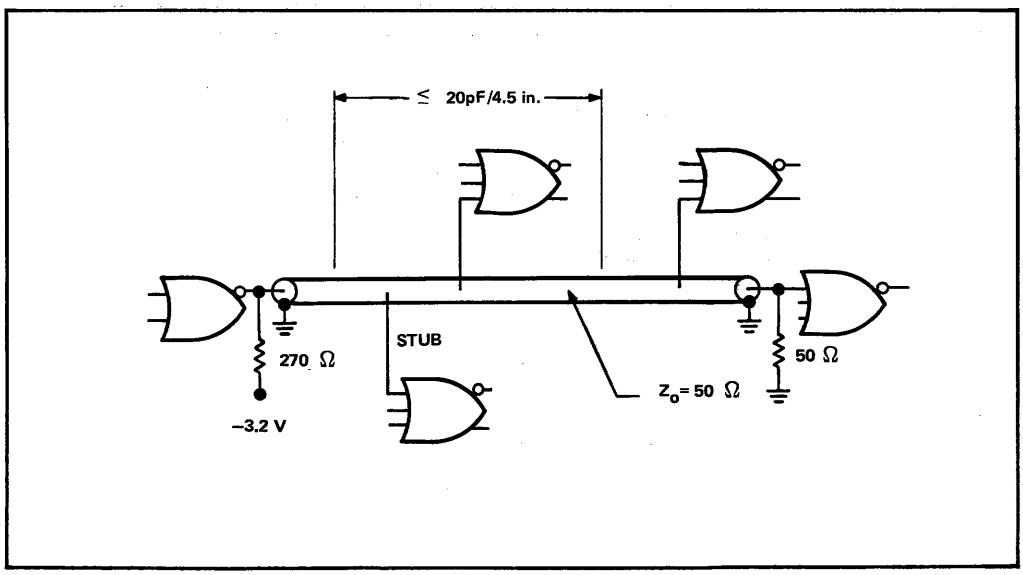
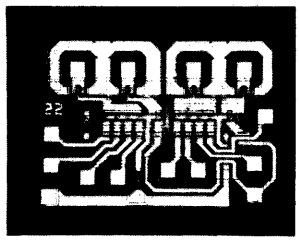
figure 4. typical distributive loading



ECL2500 SERIES EMITTER-COUPLED-LOGIC (ECL) BASIC GATES FOR APPLICATION IN ULTRA-HIGH-SPEED DIGITAL SYSTEMS

description

The ECL2500 series is a compatible family of ECL functions with basic gate delays of 2 to 3 ns per stage. The family is specifically designed for operation from 0°C to 75°C.



The ECL2500 family includes:

- **Basic Gate Modules**
- Multifunction Gate Modules
- Bistable Modules
- Arithmetic Modules
- Interface Modules
- Memory Module

family features

- High speed. . .typical gate propagation delay time of 2.5 ns
- Complementary OR/NOR outputs with capability for wired-OR connections
- Designed for use with transmission lines to ensure maximum signal transmission without noise. Characterized for 50-ohm lines
- High noise immunity: ±225 mV typical at 25°C

This data sheet covers the basic gate modules. Separate data sheets cover the balance of the ECL2500 modules.

ECL2500 series basic gates

The seven ECL2500 series modules that form the basic gate group are shown in the table below. These modules contain various combinations of the basic ECL gate shown in the schematic of Figure A and the logic diagrams of Figure B.

SUMMARY OF MODULES IN BASIC GATE GROUP

MODULE	GATES PER MODULE	INPUTS PER GATE	POSITIVE LOGIC	OUTPUTS PER GATE	
				Y (OR)	Z (NOR)
ECL2500	2	4	OR/NOR	1	1
ECL2501	1	9	OR/NOR	1	1
ECL2502	3	2	OR/NOR	1	1
ECL2503	4	2	NOR		1
ECL2504	4	1	OR/NOR	1	1
ECL2505	3	3	NOR		1
ECL2511	4	2 (1 common to each gate)	OR	1	

unused inputs

To ensure high-speed operation all unused inputs should be tied to -1.0 ± 0.5 V.

power dissipation

Basic gate power drain with outputs unterminated is between 22 mW and 34 mW under the following conditions:

V_{CC} = 1.32 V
V_{EE} = -3.2 V
V_{BB} = 0 V

All inputs at 400 mV

When terminated into 50 Ω to ground and 270 Ω to −3.2 V, each emitter-follower output will dissipate an additional 22 mW in the up-level state and approximately 8 mW in the down-level state. Therefore, a basic gate with terminated complementary outputs will dissipate approximately 60 mW.

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switching times

Switching-time performance at 25° C with various capacitive loadings is described in figure 5. This capacitive loading is directly relatable to a-c fan-out assuming 4-5 pF per gate input. Delay-time degradation with increasing fan-out approximates 75 ps per additional load. Switching-time waveform definitions and output terminations used for testing are shown in figure 6.

figure 5. switching time vs loading

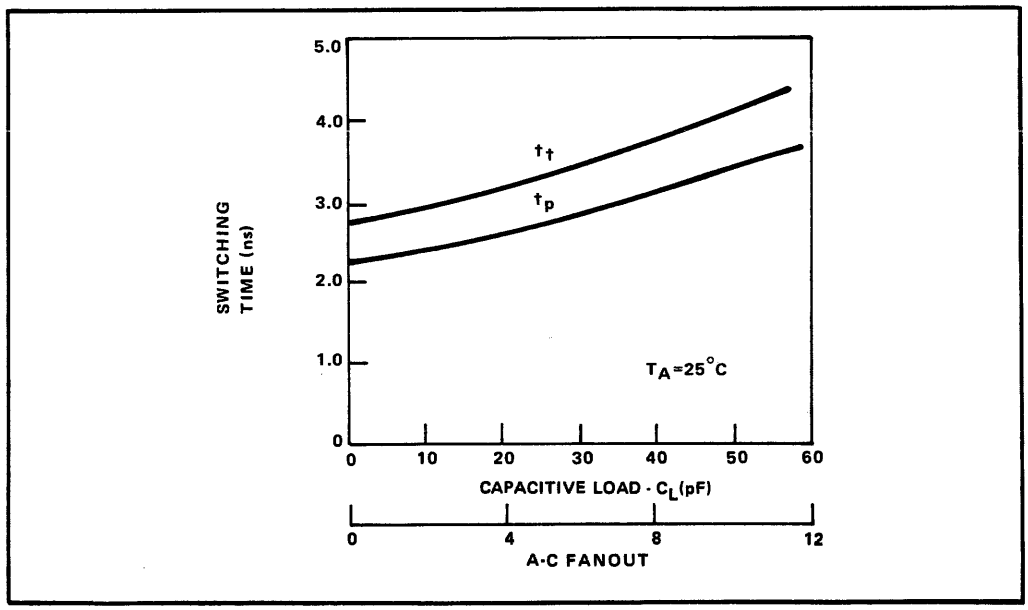

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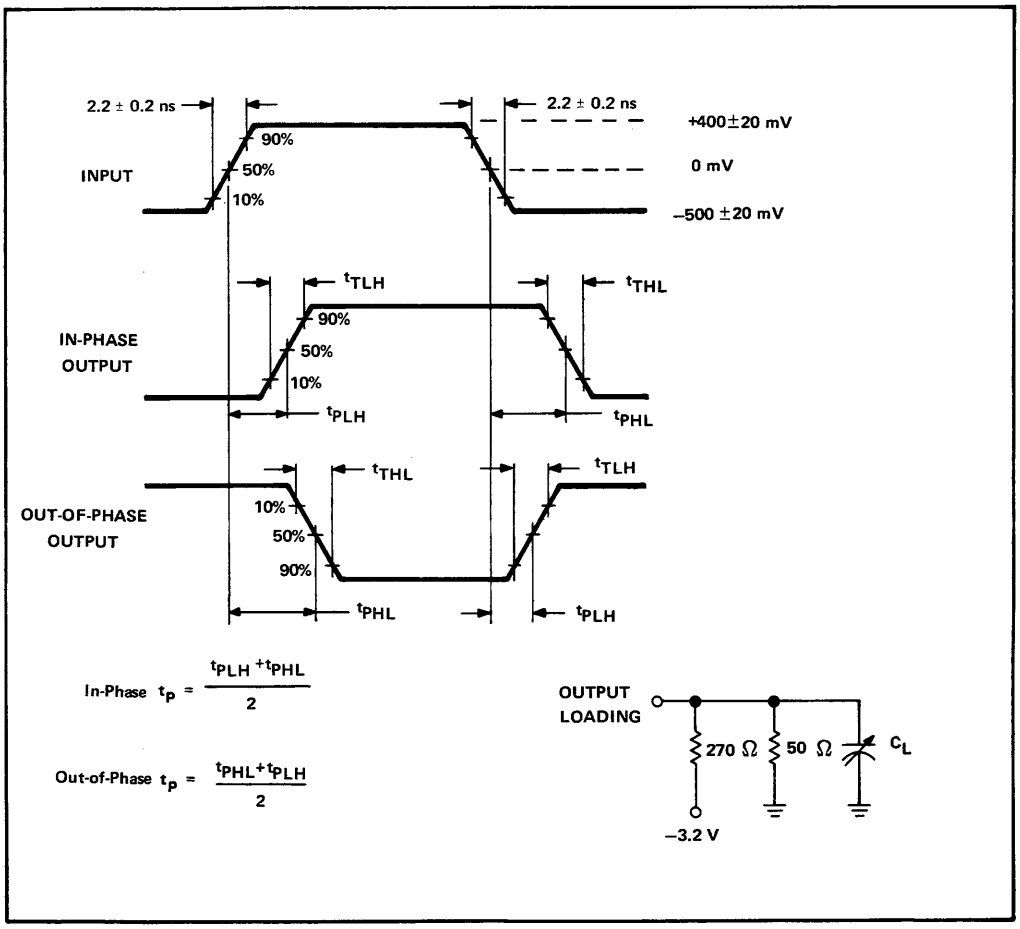
figure 6. switching time waveforms



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arithmetic and decoder

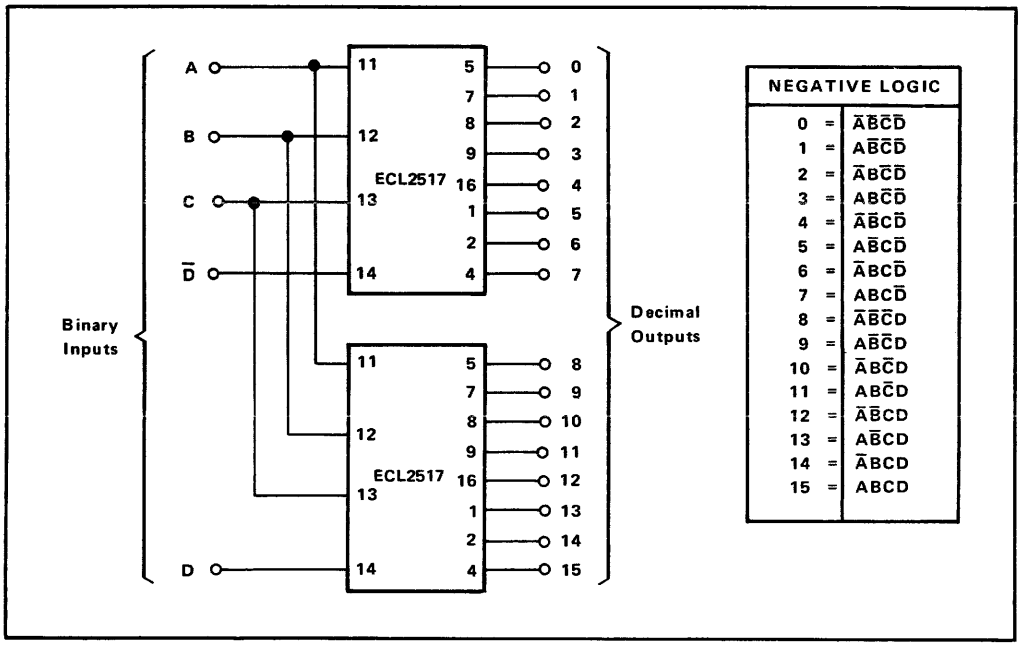
In addition to multifunction logic, more complex gating functions such as a 5-Bit Group Carry, Full Sum/Carry Adder, and 3-Bit Decoder have been included in the ECL2500 Series. Each of these modules will implement logic functions found in most large systems.

The 5-Bit Group Carry (ECL2515) is designed to provide the "look-ahead" carry feature required in high-speed adder applications. By utilizing this device and implementing the add function, significant reduction in addition delay time can be achieved as compared to ripple-through-carry addition.

The Full Sum-Carry Adder (ECL2516) produces the sum and carry outputs along with their complements for 1-bit additions. This addition can be accomplished in less than 3 ns.

The 3-Bit Decoder with Enable (ECL2517) generates a negative logical "1" on one of eight outputs dependent on the 3-bit binary input. The enable or 4th-bit input permits 4-bit binary decoding when two ECL2517 packages are utilized as shown in figure 7. Also shown is the binary decoding for the eight outputs of the ECL2517.

figure 7. 4-bit binary decode application



line driver

Each of the line drivers in the ECL2531 (2 per package) is designed to drive two 50-Ω transmission lines from both its in-phase and out-of-phase outputs. This permits fanning-out in two directions from each output.

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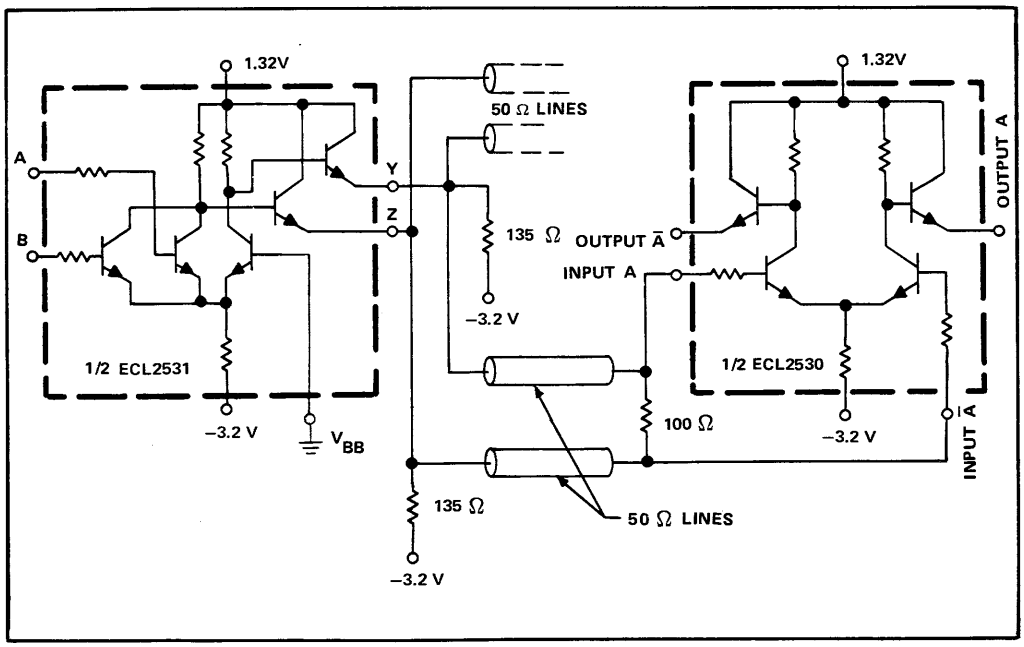
line receiver

The Dual Line Receiver (ECL2530) is designed to provide compatibility with the dual-line driver; however, it can be driven by any of the functions in the family. Its unique characteristics stem from optimization of the basic gate differential amplifier allowing input of a differential signal. Common-mode noise rejection of the Line Receiver permits transmission of logic signals over paths which are exposed to rather large noise transients and between areas in a machine which have devices operating at significantly different junction temperatures.

A typical connection arrangement is shown in figure 8.

figure 8. line driver/line receiver application



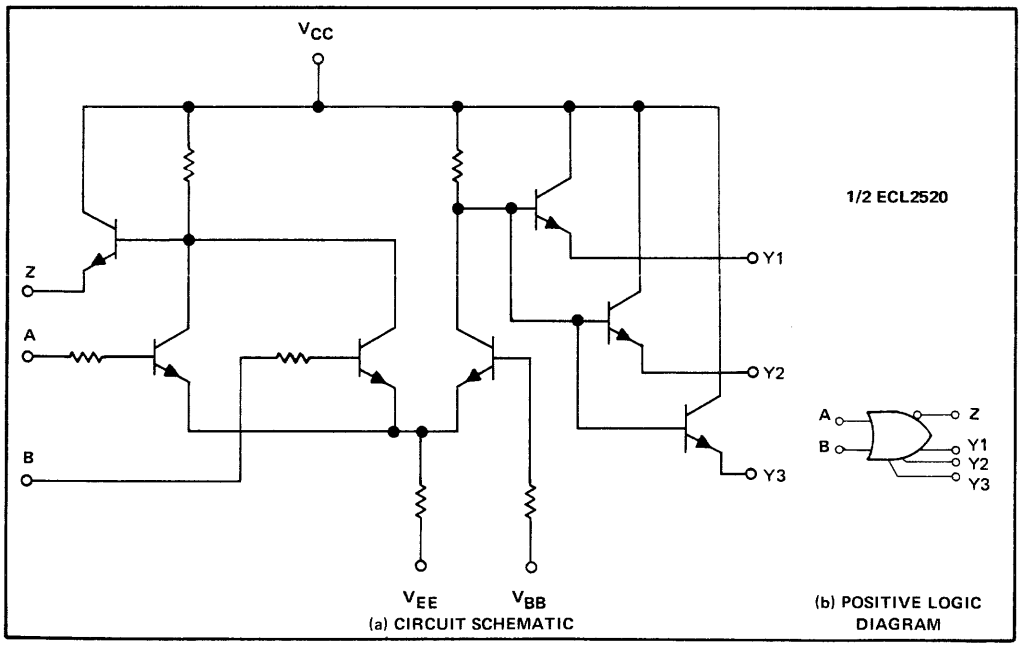
multi-output gates (drivers)

Additional fan-out or drive capability is provided in the ECL2500 Series through the use of gates with multiple emitter-follower outputs on either the in-phase or out-of-phase side of a basic gate. Additional logic flexibility can be obtained via external WIRED-OR connections of emitter-followers from these gates.

There are four dual-gate packages in the family which have gates with as many as four inputs or as many as four emitter-followers. Refer to the ECL2520 through ECL2523 for input/output combinations available.

The multiple emitter-follower circuit diagram and logic diagram is shown in figure 9.

figure 9. multi-output emitter-followers



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logic-level converters

Two Dual Logic-Level Converters are offered in the ECL2500 Series.

ECL2536	High-Level Logic to ECL
ECL2537	ECL to High-Level Logic (HLL)

The level converters are so designed that the High-Level-Logic inputs or outputs are compatible with standard saturated logic such as TTL, DTL and RTL.

The ECL2536 contains two HLL-to-ECL converters, each having an HLL input and an ECL input. The ECL input is most often used to inhibit the converter. Worst-case HLL-input levels must be $\geq$ 1.2 V and $\leq$ 0.5 V when operating with a V_{CC} of 5.0 V for the input stage.

The ECL2537 contains two ECL-to-HLL converters, each having two ECL inputs. When operating with a V_{CC} = 5.0 V and an external pulldown resistor, the output levels are:

Logical "1"	$\geq$ 3.4 V
Logical "0"	$\leq$ 0.4 V

The external pulldown resistor may be varied to satisfy the current-sinking requirement when driving TTL or DTL. Figure 10(b) shows a typical connection.

storage functions

Storage elements in the ECL2500 Series consist of three Dual "D" type flip-flops, commonly referred to as latches.

The ECL2540 is a dual latch which requires both a negative-going clock and its complement to store data presented at the data (D) input. Each latch has complementary outputs and dissipates the least amount of power ($\approx$ 60 mW) of the latches. Refer to the ECL2540 logic diagram for associated switching-time waveforms.

The ECL2541 and ECL2542 provide single-phase clock operation in addition to built-in gating features. Each latch in the ECL2541 has a single gated input, complementary outputs, plus multi-output emitter followers on one side of the latch. Multiple emitter-followers permit fan-out in two directions. Each latch in the ECL2542 has two gated inputs and a single output.

The ECL2541 and ECL2542 are defined for negative-logic inputs and upon application of a logical "1" (low level) clock the complement of the data presented at the $\overline{D}$ input will appear as output Q. Also, both devices have set and reset inputs which operate independent of the clock. The truth tables and switching waveforms applicable to these devices are shown on the data sheet.

figure 10 (a). TTL to ECL logic-level converter

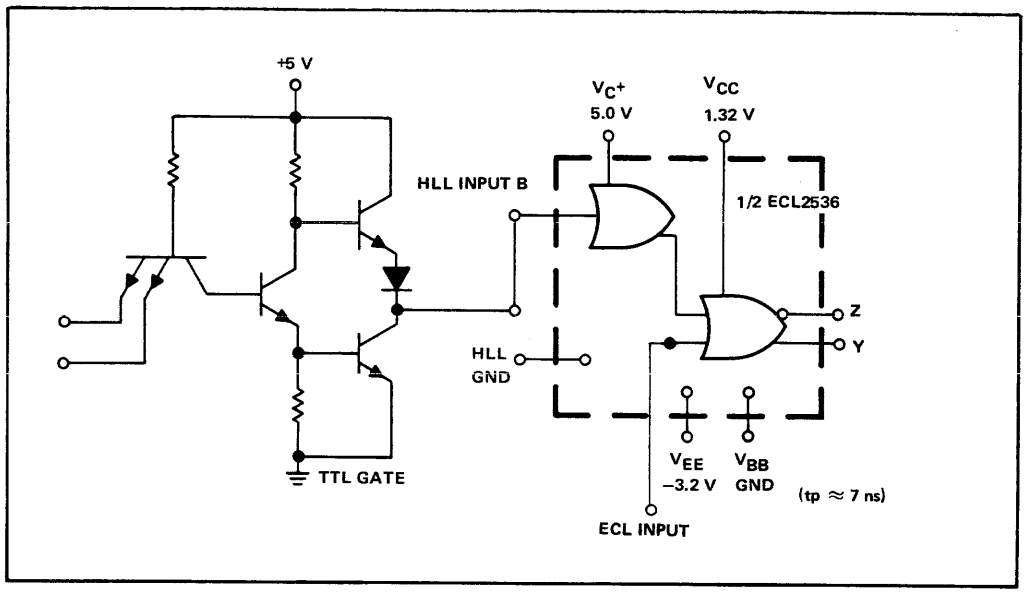
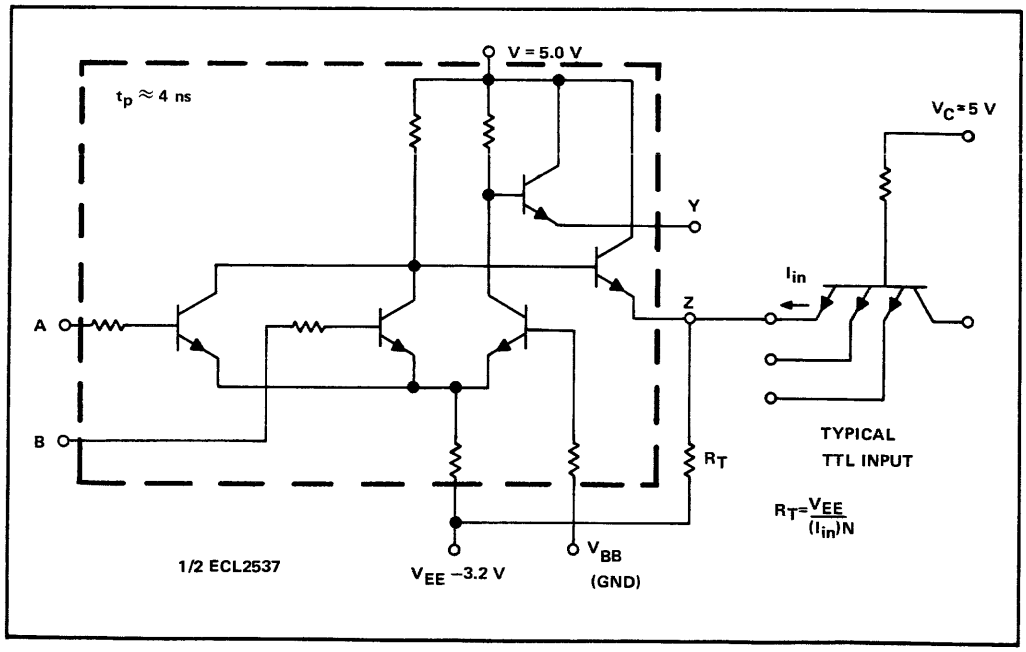


figure 10 (b). ECL to TTL logic-level converter



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TYPES ECL2500 THRU ECL2505, ECL2511
EMITTER-COUPLED-LOGIC GATES

schematic

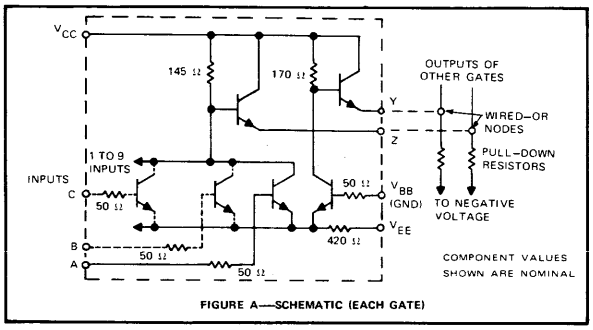

FIGURE A—SCHEMATIC (EACH GATE)

logic

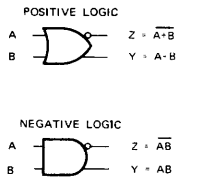

FIGURE B—TYPICAL LOGIC DIAGRAMS

Positive logic OR/NOR functions or negative logic AND/NAND functions are provided at the Y (OR) and Z (NOR) outputs, as shown.

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Emitter-follower outputs require external pull-down resistors. The wired-OR function can be obtained by connecting emitter-follower outputs of separate gates together. Only one pull-down resistor is required for each wired-OR node.

absolute maximum ratings (see note 1)

Terminal voltages and currents . . . . . See table below
Storage temperature range . . . . . −40°C to 150°C
Temperature range with supply and bias voltages applied . . . . . −40°C to 100°C

TERMINAL VOLTAGE AND/OR CURRENT, T_A = 0°C TO 75°C (SEE NOTES 2 AND 3)

TERMINAL	REMARKS	VOLTAGE		CURRENT
		CONTINUOUS	20-μs SURGE	
V_{CC}		2 V	4.5 V	
V_{EE}		−4 V	−7 V	
Each Input	All other inputs open	−3.5 V	−4 V	
		2 V	2 V	
Output Y	All inputs high			−40 mA
Output Z	All inputs low			−40 mA

recommended operating conditions

Supply voltage V_{CC} . . . . . 1.32 V ± 2%
Supply voltage V_{EE} . . . . . −3.2 V ± 2%
Reference voltage V_{BB} . . . . . 0 V (GND)
Reverse bias on unused inputs . . . . . −1 V ± 0.5 V
Normalized d-c fan-out . . . . . 0 to 35
Load on each output . . . . . characterized at 270 Ω to V_{EE}, 50 Ω to GND
Operating free-air temperature range . . . . . 0°C to 75°C

NOTES: 1. Absolute maximum ratings are limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing.
2. Maximum terminal conditions must be considered as mutually exclusive.
3. All voltages are referenced to V_{BB}, which is at GND.

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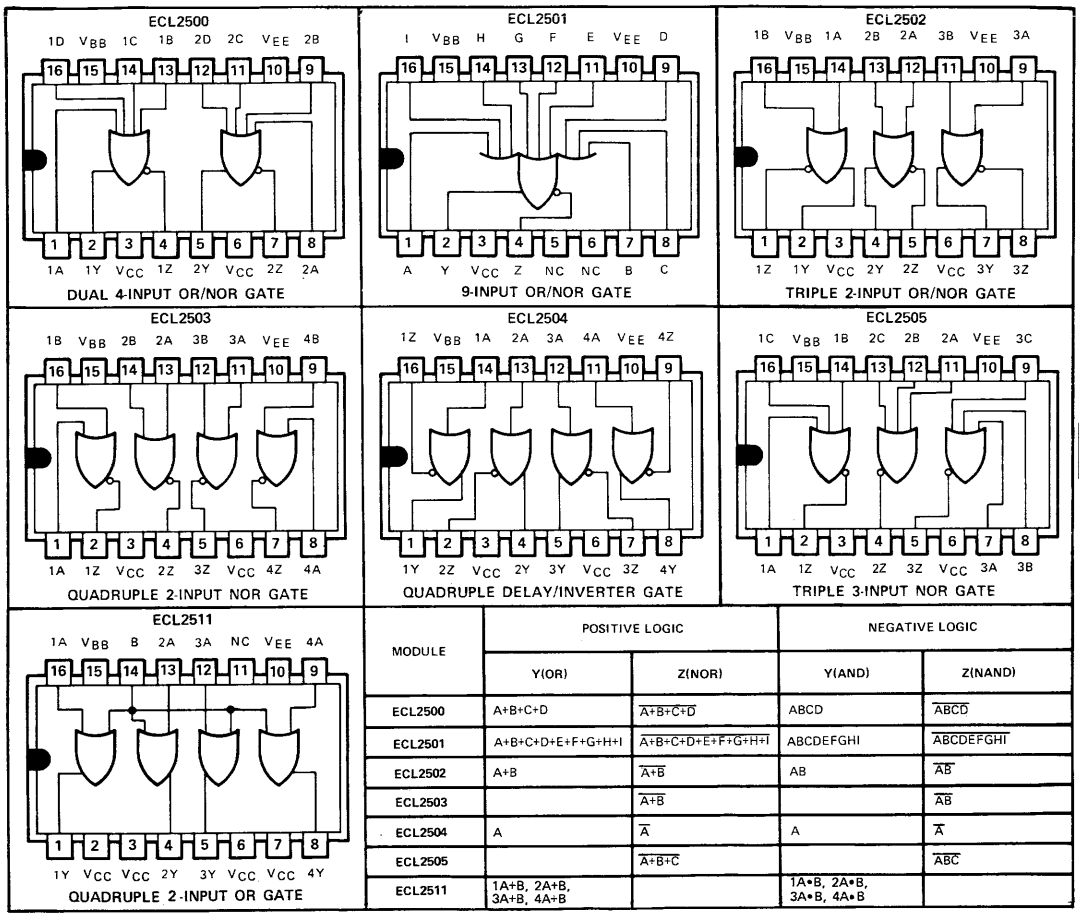
logic



MODULE	POSITIVE LOGIC		NEGATIVE LOGIC	
	Y(OR)	Z(NOR)	Y(AND)	Z(NAND)
ECL2500	A+B+C+D	$\overline{A+B+C+D}$	ABCD	$\overline{ABCD}$
ECL2501	A+B+C+D+E+F+G+H+I	$\overline{A+B+C+D+E+F+G+H+I}$	ABCDEFGHI	$\overline{ABCDEFGHI}$
ECL2502	A+B	$\overline{A+B}$	AB	$\overline{AB}$
ECL2503		$\overline{A+B}$		$\overline{AB}$
ECL2504	A	$\overline{A}$	A	$\overline{A}$
ECL2505		$\overline{A+B+C}$		$\overline{ABC}$
ECL2511	1A+B, 2A+B, 3A+B, 4A+B		1A•B, 2A•B, 3A•B, 4A•B	

NC—No internal connection

truth tables (for this series, H = positive voltage, L = negative voltage, X = irrelevant)

ECL2500

A	B	C	D	Y	Z
L	L	L	L	L	H
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
H	H	H	H	H	L

ECL2501

A	B	C	D	E	F	G	H	I	Y	Z
L	L	L	L	L	L	L	L	L	L	H
H	X	X	X	X	X	X	X	X	H	L
X	H	X	X	X	X	X	X	X	H	L
X	X	H	X	X	X	X	X	X	H	L
X	X	X	H	X	X	X	X	X	H	L
X	X	X	X	H	X	X	X	X	H	L
X	X	X	X	X	H	X	X	X	H	L
X	X	X	X	X	X	H	X	X	H	L
X	X	X	X	X	X	X	H	X	H	L
X	X	X	X	X	X	X	X	H	H	L
H	H	H	H	H	H	H	H	H	H	L

ECL2502

A	B	Y	Z
L	L	L	H
H	X	H	L
X	H	H	L
H	H	H	L

ECL2503

A	B	Z
L	L	H
H	X	L
X	H	L
H	H	L

ECL2504

A	Y	Z
L	L	H
H	H	L

ECL2505

A	B	C	Z
L	L	L	H
H	X	X	L
X	H	X	L
X	X	H	L
H	H	H	L

ECL2511

A	B	Y
L	L	L
H	X	H
X	H	H
H	H	H

electrical characteristics at specified free-air temperature

PARAMETER		TEST FIGURE	TEST CONDITIONS*		MODULE ECL2500	ECL2501	ECL2502	ECL2503	ECL2504	ECL2505	ECL2511	SEE NOTE 4 MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage			0°C	•	•	•	•	•	•	•	150		720	mV
				25°C								150		720	
				75°C								150		720	
V_{IL}	Low-level input voltage			0°C	•	•	•	•	•	•	•	−1500		−150	mV
				25°C								−1500		−150	
				75°C								−1500		−150	
$V_{OH(Y)}$	High-level output voltage at OR output	2	V_I = 0.2 V	0°C	•	•	•		•		•	315	390		mV
				25°C								350	425	500	
				75°C									495	580	
$V_{OL(Y)}$	Low-level output voltage at OR output	2	V_I = −0.2 V	0°C	•	•	•		•		•	−505	−445		mV
				25°C								−490	−425	−350	
				75°C									−385	−310	
$V_{OH(Z)}$	High-level output voltage at NOR output	2	V_I = −0.2 V	0°C	•	•	•	•	•	•		315	390		mV
				25°C								350	425	500	
				75°C									495	580	
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	V_I = 0.2 V	0°C	•	•	•	•	•	•			−385		mV
				25°C								−420	−365	−310	
				75°C									−325	−280	
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	V_I = 0.4 V	0°C	•	•	•	•	•	•		−505	−455		mV
				25°C								−490	−425		
				75°C									−380	−315	
$V_{OH(Y)}$	High-level output voltage at OR output	2	V_I = 0.15 V	0°C	•	•	•		•		•	290			mV
				25°C								325			
				75°C											
$V_{OL(Y)}$	Low-level output voltage at OR output	2	V_I = −0.15 V	0°C	•	•	•		•		•			−325	mV
				25°C										−290	
				75°C											
$V_{OH(Z)}$	High-level output voltage at NOR output	2	V_I = −0.15 V	0°C				•		•		290			mV
				25°C								325			
				75°C											
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	V_I = 0.15 V	0°C				•		•				−290	mV
				25°C										−260	
				75°C											
I_{IH}	High-level input current (each input)	3	V_I = 0.5 V	0°C	•	•	•	•	•	•	•			255	μA
				25°C										235	
				75°C										200	
I_{IL}	Low-level input current	4	V_I = −3.2 V	0°C	•	•	•	•	•	•	•			−0.5†	μA
				25°C										−0.6†	
				75°C										−0.9†	
I_{CC} or $-I_{EE}$	Supply current	5	V_I = −0.5 V	25°C	•							8		15	mA
						•						4		8	
							•					13		21	
								•				18		28	
									•			18		28	
										•		13		21	
											•	18		28	
C_{in}	Input capacitance (each input)		See Note 5	25°C	•	•	•	•	•	•	•		5		pF
z_{out}	Output impedance		See Note 6	25°C	•	•	•	•	•	•	•		5		Ω

* V_{BB} = GND, V_{CC} = 1.32 V ±1%, V_{EE} = −3.20 V ±1%.

† These are worst-case values for nine inputs in parallel. See Supplementary Parameter Measurement Information for each gate.

NOTES: 4. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.

5. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. C_{in} = Q/V.

6. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

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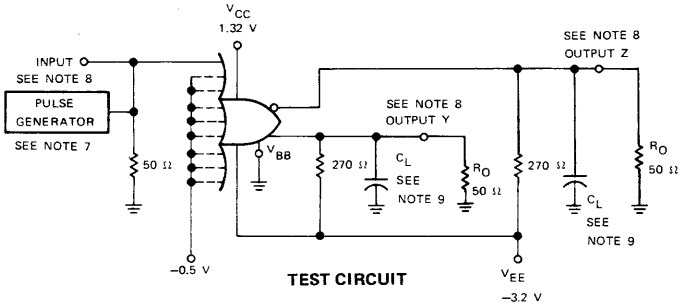
typical operating characteristics at specified free-air temperature (see figure 1)

PARAMETER		C_L	T_A	ECL2500 ECL2502 ECL2504	ECL2501		ECL2503 ECL2505	ECL2511		UNIT
				ANY OUTPUT	Y OUTPUT	Z OUTPUT	ANY OUTPUT	A INPUTS	B INPUT	
				TYP†	TYP†	TYP†	TYP†	TYP†	TYP†	
t_{PHL}	Propagation delay time, high-to-low-level output	4 pF	0°C	2.4	2.4	2.6	2.6	2.4	2.7	ns
			25°C	2.3	2.3	2.4	2.5	2.5	2.8	
	and/or		75°C	2.4	2.4	2.6	2.6	2.4	2.7	
t_{PLH}	Propagation delay time, low-to-high-level output	50 pF	0°C	3.5	3.5	3.8	3.8	3.4	3.4	ns
			25°C	3.3	3.3	3.5	3.5	3.6	3.7	
			75°C	3.5	3.5	3.8	3.8	3.4	3.4	
t_{THL}	Transition time, high-to-low-level output	4 pF	0°C	3.3	3.3	5.1	4.3	4.0	4.2	ns
			25°C	3.0	3.0	4.8	4.0	3.8	4.0	
	and/or		75°C	3.3	3.3	5.1	4.3	4.0	4.2	
t_{TLH}	Transition time, low-to-high-level output	50 pF	0°C	4.2	4.2	4.7	4.4	4.5	4.7	ns
			25°C	3.9	3.9	4.4	4.1	4.3	4.5	
			75°C	4.2	4.2	4.7	4.4	4.5	4.7	

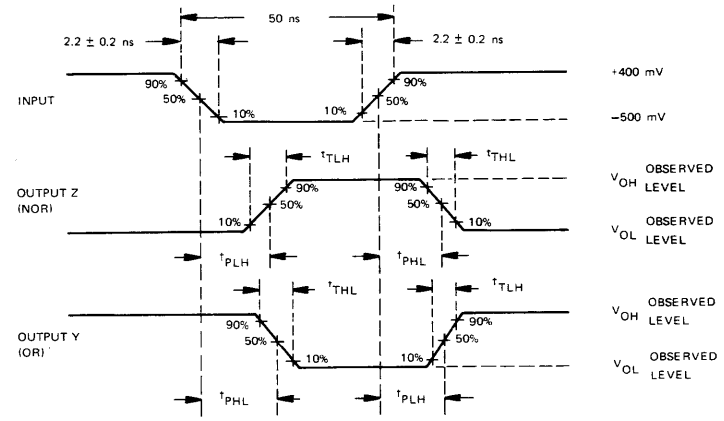
†See Supplementary Parameter Measurement Information for MIN and MAX values at T_A = 25°C.

4

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

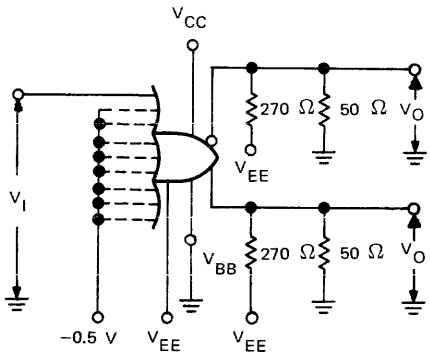
FIGURE 1—PROPAGATION DELAY AND TRANSITION TIMES

NOTES: 7. The generator has the following characteristics: Z_{out} = 50 Ω, PRR = 1 MHz.

8. The waveforms are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. Either a high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF, or a 50-Ω impedance system can be used. The 50-Ω resistors designated R_O are the oscilloscope input resistance in the 50-Ω system or discrete resistors with a high-impedance probe.

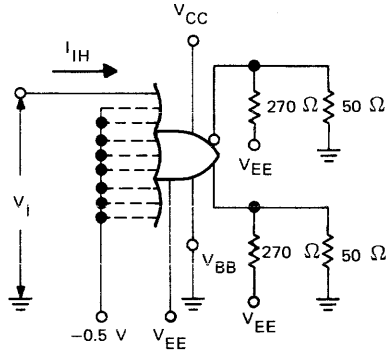
9. C_L includes probe and fixture capacitance. A capacitance of 50 pF can be used to approximate an a-c fan-out of 10.

PARAMETER MEASUREMENT INFORMATION†



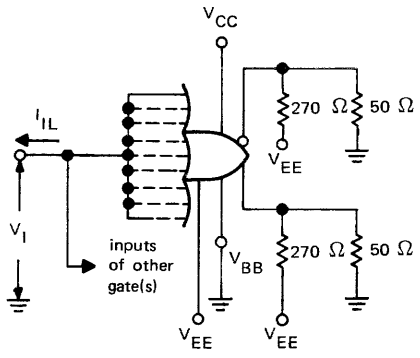
A. V_I is applied to each input separately.
B. Each output is tested separately.

FIGURE 2—V_{OH} AND V_{OL}



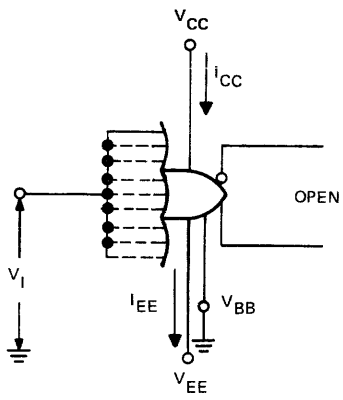
Each input is tested separately.

FIGURE 3—I_{IH}



All inputs of all gates are connected in parallel.

FIGURE 4—I_{IL}



A. All gates are tested simultaneously.
B. I_{CC} is the total current into all V_{CC} terminals.

FIGURE 5–I_{CC} OR I_{EE}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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PARAMETER (SEE NOTE 10)	TERMINALS TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATE(S)					
ECL2500	V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Y)}$	1,13,14,16	2	2	0.2 V	−0.5 V	−0.5 V	0°C 25°C 75°C	315 350	390 425 495	 500 580	mV
	8,9,11,12	5									
$V_{OL(Y)}$	1,13,14,16	2	2	−0.2 V	−0.5 V	−0.5 V	0°C 25°C 75°C	−505 −490	−445 −425 −385	−350 −310	mV
	8,9,11,12	5									
$V_{OH(Z)}$	1,13,14,16	4	2	−0.2 V	−0.5 V	−0.5 V	0°C 25°C 75°C	315 350	390 425 495	 500 580	mV
	8,9,11,12	7									
$V_{OL(Z)}$	1,13,14,16	4	2	0.2 V	−0.5 V	−0.5 V	0°C 25°C 75°C	−420	−385 −365 −325	−310 −280	mV
	8,9,11,12	7									
$V_{OL(Z)}$	1, 13, 14, 16	4	2	0.4 V	−0.5 V	−0.5 V	0°C 25°C 75°C	505 490	455 425 380	 315	mV
	8, 9, 11, 12	7									
$V_{OH(Y)}$	12	5	2	0.15 V	−0.5 V	−0.5 V	0°C 25°C 75°C	290 325			mV
$V_{OL(Y)}$	12	5	2	−0.15 V	−0.5 V	−0.5 V	0°C 25°C 75°C			−325 −290	mV
I_{IH}	1,13,14,16		3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			255 235 200	μA
	8,9,11,12										
I_{IL}	1,13,14,16		4	All inputs of both gates in parallel at −3.2 V			0°C 25°C 75°C			−0.5 −0.5 −0.8	μA
	8,9,11,12										
ECL2501	V_{BB} (pin 15) = GND, V_{CC} (pin 3) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Y)}$	1,7,8,9,11, 12,13,14,16	2	2	0.2 V	−0.5 V		0°C 25°C 75°C	315 350	390 425 495	 500 580	mV
$V_{OL(Y)}$	1,7,8,9,11, 12,13,14,16	2	2	−0.2 V	−0.5 V		0°C 25°C 75°C	−505 −490	−455 −425 −385	−350 −310	mV
$V_{OH(Z)}$	1,7,8,9,11, 12,13,14,16	4	2	−0.2 V	−0.5 V		0°C 25°C 75°C	315 350	390 425 495	500 580	mV
$V_{OL(Z)}$	1,7,8,9,11, 12,13,14,16	4	2	0.2 V	−0.5 V		0°C 25°C 75°C	420	385 365 325	310 280	mV
$V_{OL(Z)}$	1,7,8,9,11, 12,13,14,16	4	2	0.4 V	−0.5 V		0°C 25°C 75°C	505 490	455 425 380	 315	mV
$V_{OH(Y)}$	1	2	2	0.15 V	−0.5 V		0°C 25°C 75°C	290 325			mV
$V_{OL(Y)}$	1	2	2	−0.15 V	−0.5 V		0°C 25°C 75°C			−325 −290	mV
I_{IH}	1,7,8,9,11, 12,13,14,16		3	0.5 V	−0.5 V		0°C 25°C 75°C			255 235 200	μA
I_{IL}	1,7,8,9,11, 12,13,14,16		4	All inputs in parallel at −3.2 V			0°C 25°C 75°C			−0.5 −0.6 −0.9	μA

NOTES: 10. See page 4 for defining term associated with each symbol.
11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATES					
ECL2502	V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Y)}$	14,16	2	2	0.2 V	−0.5 V	−0.5 V	0°C	315	390		mV
	12,13	4					25°C	350	425	500	
	9,11	7					75°C		495	580	
$V_{OL(Y)}$	14,16	2	2	−0.2 V	−0.5 V	−0.5 V	0°C	−505	−445		mV
	12,13	4					25°C	−490	−425	−350	
	9,11	7					75°C		−385	−310	
$V_{OH(Z)}$	14,16	1	2	−0.2 V	−0.5 V	−0.5 V	0°C	315	390		mV
	12,13	5					25°C	350	425	500	
	9,11	8					75°C		495	580	
$V_{OL(Z)}$	14,16	1	2	0.2 V	−0.5 V	−0.5 V	0°C		−385		mV
	12,13	5					25°C	−420	−365	−310	
	9,11	8					75°C		−325	−280	
$V_{OL(Z)}$	14,16	1	2	0.4 V	−0.5 V	−0.5 V	0°C	−505	−455		mV
	12,13	5					25°C	−490	−425		
	9,11	8					75°C		−380	−315	
$V_{OH(Y)}$	11	7	2	0.15 V	−0.5 V	−0.5 V	0°C	290			mV
							25°C	325			
							75°C				
$V_{OL(Y)}$	11	7	2	−0.15 V	−0.5 V	−0.5 V	0°C				mV
							25°C			−325	
							75°C			−290	
I_{IH}	14,16		3	0.5 V	−0.5 V	−0.5 V	0°C			255	μA
	12,13						25°C			235	
	9,11						75°C			200	
I_{IL}	14,16		4	All inputs of all gates in parallel at −3.2 V			0°C			−0.5	μA
	12,13						25°C			−0.5	
	9,11						75°C			−0.6	
ECL2503	V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Z)}$	1,16	2	2	−0.2 V	−0.5 V	−0.5 V	0°C	315	390		mV
	13,14	4					25°C	350	425	500	
	11,12	5					75°C		495	580	
	8,9	7									
$V_{OL(Z)}$	1,16	2	2	0.2 V	−0.5 V	−0.5 V	0°C		−385		mV
	13,14	4					25°C	−420	−365	−310	
	11,12	5					75°C		−325	−280	
	8,9	7									
$V_{OL(Z)}$	1,16	2	2	0.4 V	−0.5 V	−0.5 V	0°C	−505	−455		mV
	13,14	4					25°C	−490	−425		
	11,12	5					75°C		−380	−315	
	8,9	7									
$V_{OH(Z)}$	9	7	2	−0.15 V	−0.5 V	−0.5 V	0°C	290			mV
							25°C	325			
							75°C				
$V_{OL(Z)}$	9	7	2	0.15 V	−0.5 V	−0.5 V	0°C				mV
							25°C			−290	
							75°C			−260	
I_{IH}	1,16		3	0.5 V	−0.5 V	−0.5 V	0°C			255	μA
	13,14						25°C			235	
	11,12						75°C			200	
	8,9										
I_{IL}	1,16		4	All inputs of all gates in parallel at −3.2 V			0°C			−0.5	μA
	13,14						25°C			−0.5	
	11,12						75°C			−0.8	
	8,9										

NOTES: 10. See page 4 for defining term associated with each symbol.

11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.

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PARAMETER (SEE NOTE 10)	TERMINALS TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATES					
ECL2504	V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Y)}$	14	1	2	0.2 V		−0.5 V	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
	13	4									
	12	5									
	11	8									
$V_{OL(Y)}$	14	1	2	−0.2 V		−0.5 V	0°C 25°C 75°C	−505 −490	−445 −425 −385	−350 −310	mV
	13	4									
	12	5									
	11	8									
$V_{OH(Z)}$	14	16	2	−0.2 V		−0.5 V	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
	13	2									
	12	7									
	11	9									
$V_{OL(Z)}$	14	16	2	0.2 V		−0.5 V	0°C 25°C 75°C	−420	−385 −365 −325	−310 −280	mV
	13	2									
	12	7									
	11	9									
$V_{OL(Z)}$	14	16	2	0.4 V		−0.5 V	0°C 25°C 75°C	−505 −490	−455 −425 −380	−315	mV
	13	2									
	12	7									
	11	9									
$V_{OH(Y)}$	13	4	2	0.15 V		−0.5 V	0°C 25°C 75°C	290 325			mV
$V_{OL(Y)}$	13	4	2	−0.15 V		−0.5 V	0°C 25°C 75°C			325 290	mV
I_{IH}	14		3	0.5 V		−0.5 V	0°C 25°C 75°C			255 235 200	μA
	13										
	12										
	11										
I_{IL}	14		4	Inputs of all gates in parallel at −3.2 V			0°C 25°C 75°C			−0.5 −0.5 −0.5	μA
	13										
	12										
	11										
ECL2505	V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Z)}$	1,14,16	2	2	−0.2 V	−0.5 V	−0.5 V	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
	11,12,13	4									
	7,8,9	5									
$V_{OL(Z)}$	1,14,16	2	2	0.2 V	−0.5 V	−0.5 V	0°C 25°C 75°C	−420	−385 −365 −325	−310 −280	mV
	11,12,13	4									
	7,8,9	5									
$V_{OL(Z)}$	1,14,16	2	2	0.4 V	−0.5 V	−0.5 V	0°C 25°C 75°C	−505 −490	−455 −425 −380	−315	mV
	11,12,13	4									
	7,8,9	5									
$V_{OH(Z)}$	9	5	2	−0.15 V	−0.5 V	−0.5 V	0°C 25°C 75°C	290 325			mV
$V_{OL(Z)}$	9	5	2	0.15 V	−0.5 V	−0.5 V	0°C 25°C 75°C			−290 −260	mV
I_{IH}	1,14,16		3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			255 235 200	μA
	11,12,13										
	7,8,9										
I_{IL}	1,14,16		4	All inputs of all gates in parallel at −3.2 V			0°C 25°C 75°C			−0.5 −0.6 −0.9	μA
	11,12,13										
	7,8,9										

NOTES: 10. See page 4 for defining term associated with each symbol.

11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATES					
ECL2511	V_{BB} (pin 15) = GND, V_{CC} (pin 2, pin 3, pin 6, and pin 7) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Y)}$	16,14	1	2	0.2 V	−0.5 V	−0.5 V	0°C	315	390		mV
	13,14	4					25°C	350	425	500	
	12,14	5					75°C		495	580	
	9,14	8									
$V_{OL(Y)}$	16,14	1	2	−0.2 V	−0.5 V	−0.5 V	0°C	−505	−445		mV
	13,14	4					25°C	−490	−425	−350	
	12,14	5					75°C		−385	−310	
	9,14	8									
$V_{OH(Y)}$	16	1	2	0.15 V	−0.5 V	−0.5 V	0°C	290			mV
							25°C	325			
							75°C				
$V_{OL(Y)}$	16	1	2	−0.15 V	−0.5 V	−0.5 V	0°C				mV
							25°C			−325	
							75°C			−290	
I_{IH}	16		3	0.5 V	−0.5 V	−0.5 V	0°C			255	mV
	13						25°C			235	
	12						75°C			200	
	9										
	14		3	0.5 V	−0.5 V		0°C			1020	μA
							25°C			940	
							75°C			800	
I_{IL}	16		4	All inputs of all gates in parallel at −3.2 V			0°C			−0.5	μA
	13						25°C			−0.5	
	12						75°C			−0.8	
	9										
	14										

NOTES: 10. See page 4 for defining term associated with each symbol.

11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.

GENERAL APPLICATION INFORMATION

Multiple V_{CC} terminals have been supplied to reduce crosstalk noise. All V_{CC} terminals should be connected even if all gates in a module are not used.

Applications of the ECL2500 basic gates at other than data sheet conditions are covered in a separate family application document.

General loading for fan-out may be divided into two classes:

CLASS I — **Short-Line or Cluster Loading.**
Loads which can be connected within two inches of any source can be treated as lumped capacitive loads which include the gate inputs and stub-line capacitances. Switching times can be interpolated accordingly. No two dotted outputs can be more than two inches apart for this case.

CLASS II — **Long-Line or Distributive Loading.**
These loads must be treated as lumped loads along a transmission line and termination should be at the end of the transmission chain. No more than 20 pF of load is recommended per 4.5 inches of 50-ohm printed line (with dielectric constant of 4.5) in order that the reflection coefficient be no greater than 20%. If the loads are lumped loads of 20 pF, they must be 4.5 inches apart. If individual gates and CLASS I loads are distributed, they must not exceed the 20 pF per 4.5 inches of line.

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SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

operating characteristics at specified free-air temperature (see figure 1)

TERMINALS TO BE TESTED (SEE NOTES 12, 13, AND 14)				C_L	t_{PHL} and/or t_{PLH} PROPAGATION TIMES—ns						t_{THL} and/or t_{TLH} TRANSITION TIMES—ns					
					$T_A = 0°C$			$T_A = 25°C$			$T_A = 75°C$			$T_A = 0°C$			$T_A = 25°C$			$T_A = 75°C$		
INPUT	OUTPUT	INPUT	OUTPUT	INPUT	OUTPUT	INPUT	OUTPUT	pF	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
ECL2500																										
1, 13, 14, 16	2, 4	8, 9, 11, 12	5, 7					4		2.4			1.5	2.3	3.3		2.4			3.3			1.7	3.0	4.7		3.3
								50		3.5			2.4	3.3	4.4		3.5			4.2			2.5	3.9	6.5		4.2
ECL2501																										
1,7,8, 9,11, 12,13, 14,16	2							4		2.4			1.5	2.3	3.3		2.4			3.3			1.7	3.0	4.7		3.3
								50		3.5			2.4	3.3	4.4		3.5			4.2			2.5	3.9	6.5		4.2
1,7,8, 9,11, 12,13, 14,16	4							4		2.6			1.6	2.4	3.4		2.6			5.1			2.8	4.8	6.5		5.1
								50		3.8			2.4	3.5	4.5		3.8			4.7			2.8	4.4	6.5		4.7
ECL2502																										
2, 14,16	1	4, 12,13	5	7, 9,11	8			4		2.4			1.5	2.3	3.3		2.4			3.3			1.7	3.0	4.7		3.3
								50		3.5			2.4	3.3	4.4		3.5			4.2			2.5	3.9	6.5		4.2
ECL2503																										
1, 16	2	13, 14	4	11, 12	5	8, 9	7	4		2.6			1.7	2.5	3.5		2.6			4.3			2.8	4.0	5.6		4.3
								50		3.8			2.4	3.5	4.5		3.8			4.4			2.8	4.1	6.5		4.4
ECL2504																										
14	1, 16	13	4, 2	12	5, 7	11	8, 9	4		2.4			1.5	2.3	3.3		2.4			3.3			1.7	3.0	4.7		3.3
								50		3.5			2.4	3.3	4.4		3.5			4.2			2.5	3.9	6.5		4.2
ECL2505																										
1, 14, 16	2	11, 12, 13	4	7, 8, 9	5			4		2.6			1.7	2.5	3.5		2.6			4.3			2.8	4.0	5.6		4.3
								50		3.8			2.4	3.5	4.5		3.8			4.4			2.8	4.1	6.5		4.4
ECL2511																										
16	1	13	4	12	5	9	8	4		2.4			1.7	2.5	3.5		2.4			4.0			2.6	3.8	5.2		4.0
								50		3.4			2.4	3.6	4.5		3.4			4.5			2.6	4.3	6.5		4.5
14	1	14	4	14	5	14	8	4		2.7			1.9	2.8	3.7		2.7			4.2			2.6	4.0	5.4		4.2
								50		3.4			2.7	3.7	4.9		3.4			4.7			2.6	4.5	6.5		4.7

NOTES: 12. Each gate is tested separately.

13. The input pulse is measured as it is applied sequentially to each input of the gate under test and a waveform measurement is made at each of the outputs of that gate. Times are as defined in Figure 1.

14. Bias voltages and loads for the gate under test are shown in Figure 1. Unused gates have inputs biased to −0.5 V, outputs under load, and power applied.

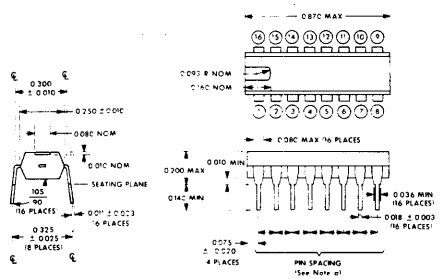
4

mechanical data

The circuit bars are mounted on a 16-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

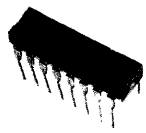
The plastic case is electrically nonconductive.

16-PIN PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



NOTES a. The true position pin spacing is 0.100 between center lines. Each pin centerline is located within 0.010 of its true longitudinal position relative to pins 1 and 16.

b. All dimensions are in inches unless otherwise noted.



terminal designations

Pin assignments are shown in the table below and correspond to the logic diagrams on page 3.
Outputs are denoted Y or Z. Inputs are denoted A, B, C, etc.
Respective inputs and outputs are identified by a gate number preceding the pin symbol.
Power is supplied via the V_{CC}, V_{EE}, and V_{BB} terminals.
V_{BB} is a reference voltage.
NC indicates no internal connection.

PIN ASSIGNMENTS

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ECL2500	1A	1Y	V_{CC}	1Z	2Y	V_{CC}	2Z	2A	2B	V_{EE}	2C	2D	1B	1C	V_{BB}	1D
ECL2501	A	Y	V_{CC}	Z	NC	NC	B	C	D	V_{EE}	E	F	G	H	V_{BB}	I
ECL2502	1Z	1Y	V_{CC}	2Y	2Z	V_{CC}	3Y	3Z	3A	V_{EE}	3B	2A	2B	1A	V_{BB}	1B
ECL2503	1A	1Z	V_{CC}	2Z	3Z	V_{CC}	4Z	4A	4B	V_{EE}	3A	3B	2A	2B	V_{BB}	1B
ECL2504	1Y	2Z	V_{CC}	2Y	3Y	V_{CC}	3Z	4Y	4Z	V_{EE}	4A	3A	2A	1A	V_{BB}	1Z
ECL2505	1A	1Z	V_{CC}	2Z	3Z	V_{CC}	3A	3B	3C	V_{EE}	2A	2B	2C	1B	V_{BB}	1C
ECL2511	1Y	V_{CC}	V_{CC}	2Y	3Y	V_{CC}	V_{CC}	4Y	4A	V_{EE}	NC	3A	2A	B	V_{BB}	1A

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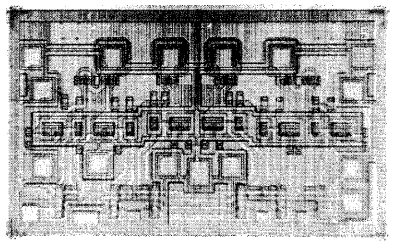
TYPES ECL2506 THRU ECL2510, ECL2512, ECL2513 MULTIFUNCTION EMITTER-COUPLED-LOGIC GATES

ECL2500 SERIES EMITTER-COUPLED-LOGIC (ECL) MULTIFUNCTION GATES FOR APPLICATION IN ULTRA-HIGH-SPEED DIGITAL SYSTEMS



description

The ECL2500 series is a compatible family of ECL functions with basic gate delays of 2 to 3 ns per stage. The family is specifically designed for operation from 0°C to 75°C.

The ECL2500 family includes:

- Basic Gate Modules
- **Multifunction Gate Modules**
- Bistable Modules
- Arithmetic Modules
- Interface Modules
- Memory Module

family features

- High speed . . . typical gate propagation delay time of 2.5 ns
- Complementary OR/NOR outputs with capability for wired-OR connections
- Designed for use with transmission lines to ensure maximum signal transmission without noise. Characterized for 50-ohm lines
- High noise immunity: ±225 mV typical at 25°C

This data sheet covers the multifunction-gate modules. Separate data sheets cover the balance of the ECL2500 modules.

ECL2500 series multifunction gates

The seven ECL2500 series modules that form the multifunction gate group are shown in the table below. These modules contain various combinations of the multifunction ECL circuit shown in the schematic of Figure A and the logic diagrams of Figure B.

SUMMARY OF MODULES IN MULTIFUNCTION GATE GROUP

MODULE	GATES PER MODULE	INPUTS PER GATE	POSITIVE LOGIC	OUTPUTS PER MODULE	
				Y	Z
ECL2506	4	3	NOR-OR		1
ECL2507	5	2	NOR-OR		1
ECL2508	6	2	NOR-OR		1
ECL2509	4	2	OR-AND/NOR-OR	1	1
ECL2510	4	3,3,3,2	OR-AND/NOR-OR	1	1
ECL2512	6	2 (1 common to each 2 gates)	NOR-OR		2
ECL2513	4	2 (1 common to 2 gates)	OR-AND/NOR-OR	2	2

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schematic

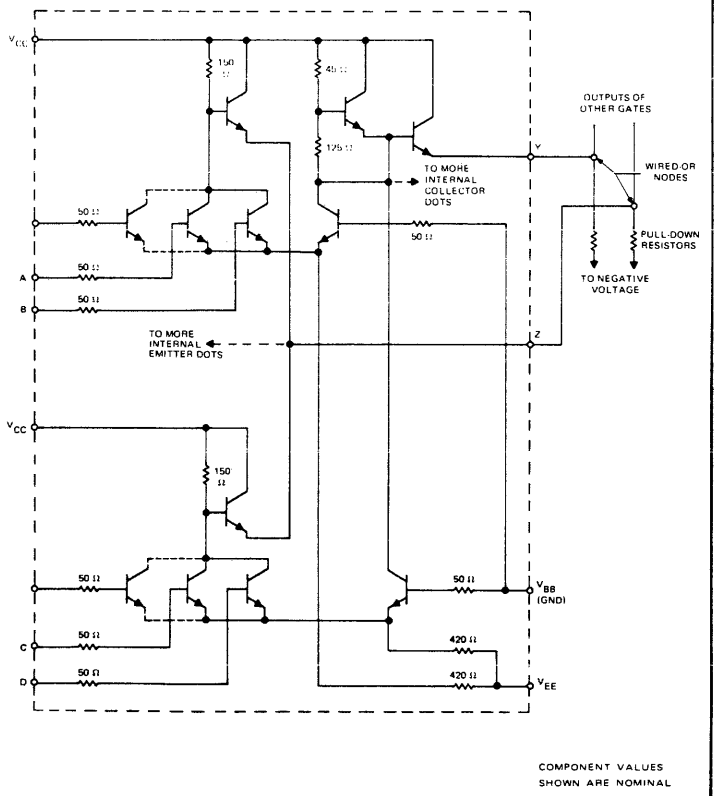

FIGURE A – TYPICAL SCHEMATIC

logic

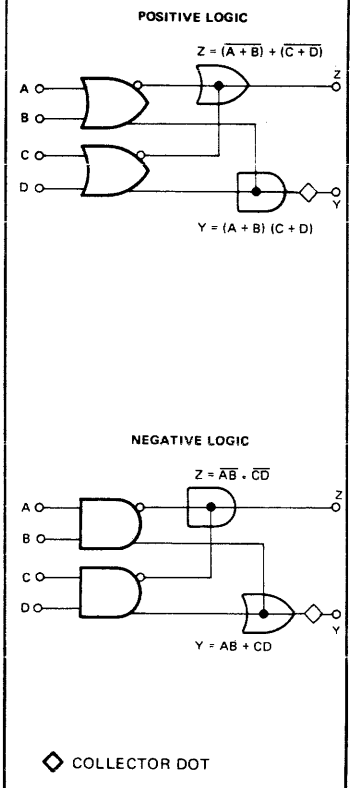

FIGURE B – TYPICAL LOGIC DIAGRAMS

Positive logic OR-AND/NOR-OR functions or negative logic AND-OR/NAND-AND functions are provided at the Y and Z outputs, as shown.

Emitter-follower outputs require an external pull-down resistor. The wired-OR function can be obtained by connecting emitter-follower outputs of separate gates together. Only one pull-down resistor is required for each wired-OR node.

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truth tables (for this series, H = positive voltage, L = negative voltage, X = irrelevant)

ECL2506

INPUTS												OUTPUT
A	B	C	D	E	F	G	H	I	J	K	L	Z
L	L	L	X	X	X	X	X	X	X	X	X	H
X	X	X	L	L	L	X	X	X	X	X	X	H
X	X	X	X	X	X	L	L	L	X	X	X	H
X	X	X	X	X	X	X	X	X	L	L	L	H
For a LOW output, at least one input of each gate must be HIGH												
H	X	X	H	X	X	H	X	X	H	X	X	L
X	H	X	X	H	X	X	H	X	X	H	X	L
X	X	H	X	X	H	X	X	H	X	X	H	L

ECL2507

INPUTS										OUTPUT
A	B	C	D	E	F	G	H	I	J	Z
L	L	X	X	X	X	X	X	X	X	H
X	X	L	L	X	X	X	X	X	X	H
X	X	X	X	L	L	X	X	X	X	H
X	X	X	X	X	X	L	L	X	X	H
X	X	X	X	X	X	X	X	L	L	H
For a LOW output, at least one input of each gate must be HIGH										
H	X	H	X	H	X	H	X	H	X	L
X	H	X	H	X	H	X	H	X	H	L

ECL2508

INPUTS												OUTPUT
A	B	C	D	E	F	G	H	I	J	K	L	Z
L	L	X	X	X	X	X	X	X	X	X	X	H
X	X	L	L	X	X	X	X	X	X	X	X	H
X	X	X	X	L	L	X	X	X	X	X	X	H
X	X	X	X	X	X	L	L	X	X	X	X	H
X	X	X	X	X	X	X	X	L	L	X	X	H
X	X	X	X	X	X	X	X	X	X	L	L	H
For a LOW output, at least one input of each gate must be HIGH												
H	X	H	X	H	X	H	X	H	X	H	X	L
X	H	X	H	X	H	X	H	X	H	X	H	L

ECL2509

INPUTS								OUTPUTS	
A	B	C	D	E	F	G	H	Y	Z
L	L	X	X	X	X	X	X	L	H
X	X	L	L	X	X	X	X	L	H
X	X	X	X	L	L	X	X	L	H
X	X	X	X	X	X	L	L	L	H
For a HIGH Y and LOW Z, at least one input of each gate must be HIGH									
H	X	H	X	H	X	H	X	H	L
X	H	X	H	X	H	X	H	H	L

ECL2510

INPUTS										OUTPUTS	
A	B	C	D	E	F	G	H	I	J	K	Y	Z
L	L	X	X	X	X	X	X	X	X	X	L	H
X	X	L	L	L	X	X	X	X	X	X	L	H
X	X	X	X	X	L	L	L	X	X	X	L	H
X	X	X	X	X	X	X	X	L	L	L	L	H
For a HIGH Y and LOW Z, at least one input of each gate must be HIGH												
H	X	H	X	X	H	X	X	H	X	X	H	L
X	H	X	H	X	X	H	X	X	H	X	H	L
X	H	X	X	H	X	X	H	X	X	H	H	L

ECL2512

INPUTS												OUTPUTS	
1A	D	1B	E	1C	F	2A	D	2B	E	2C	F	1Z	2Z
L	L	X	X	X	X		L					H	Determined
X	X	L	L	X	X			L				H	by inputs
X	X	X	X	L	L					L		H	2A,2B,2C,
H	X	H	X	H	X							L	D,E, and F.
X	H	X	H	X	H		H		H		H	L	(See below)
	L					L	L	X	X	X	X	Determined	H
		L				X	X	L	L	X	X	by inputs	H
				L		X	X	X	X	L	L	1A,1B,1C,	H
						H	X	H	X	H	X	D,E, and F.	L
	H		H		H	X	H	X	H	X	H	(See above)	L
For a LOW output from either section, at least one input of each gate in that section must be HIGH													

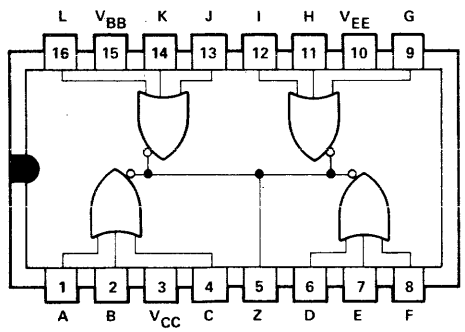
ECL2513

INPUTS								OUTPUTS	
1A	1B	1C	D	2A	2B	2C	D	1Y 1Z	2Y 2Z
L	L	X	X					L H	Determined
X	X	L	L				L	L H	by inputs
H	X	H	X					H L	2A,2B,2C, and D.
X	H	X	H				H	H L	(See below)
				L	L	X	X	Determined	L H
			L	X	X	L	L	by inputs	L H
				H	X	H	X	1A,1B,1C, and D.	H L
			H	X	H	X	H	(See above)	H L
For a HIGH Y and LOW Z from either section, at least one input of each gate in that section must be HIGH									

4

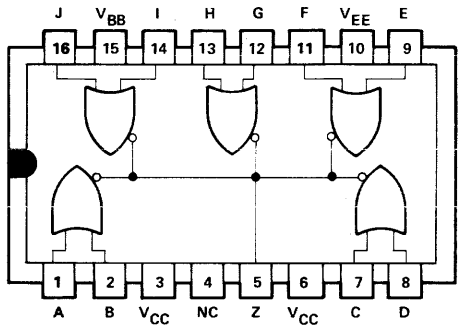
logic

ECL2506



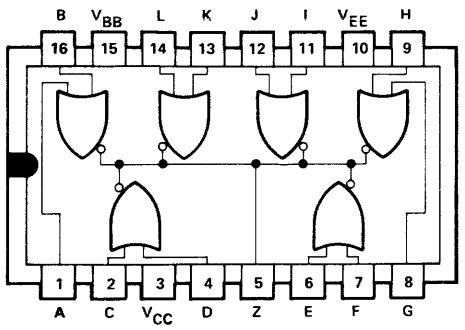
4-WIDE 3-INPUT NOR-OR GATE

ECL2507



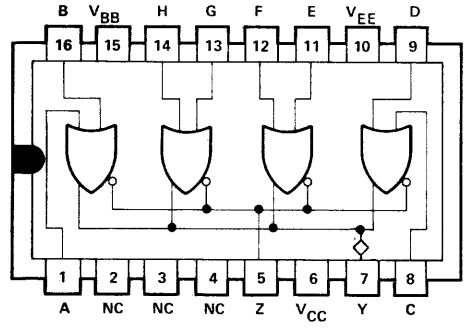
5-WIDE 2-INPUT NOR-OR GATE

ECL2508



6-WIDE 2-INPUT NOR-OR GATE

ECL2509



4-WIDE 2-INPUT
OR-AND/NOR-OR GATE

NC—No internal connection

◇ — Collector Dot

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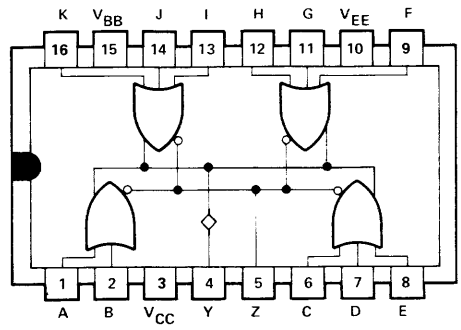
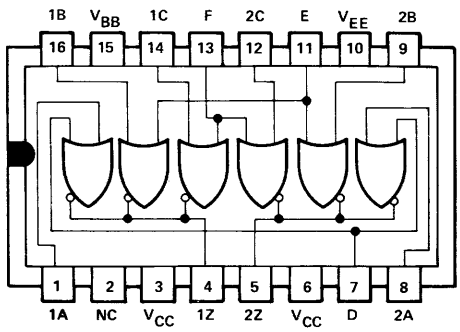
ECL2510



4-WIDE 3-3-3-2 INPUT
OR-AND/NOR-OR GATE

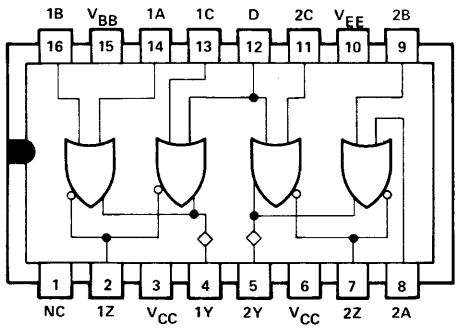
ECL2512



DUAL 3-WIDE 2-INPUT NOR-OR GATE
WITH COMMON INPUTS

4

ECL2513



DUAL 2-WIDE 2-INPUT OR-AND/NOR-OR GATE
WITH COMMON INPUT

MODULE	POSITIVE LOGIC		NEGATIVE LOGIC	
	Y	Z	Y	Z
ECL2506		$\overline{A+B+C} + \overline{D+E+F} + \overline{G+H+I} + \overline{J+K+L}$		$\overline{ABC} \cdot \overline{DEF} \cdot \overline{GHI} \cdot \overline{JKL}$
ECL2507		$\overline{A+B} + \overline{C+D} + \overline{E+F} + \overline{G+H} + \overline{I+J}$		$\overline{AB} \cdot \overline{CD} \cdot \overline{EF} \cdot \overline{GH} \cdot \overline{IJ}$
ECL2508		$\overline{A+B} + \overline{C+D} + \overline{E+F} + \overline{G+H} + \overline{I+J} + \overline{K+L}$		$\overline{AB} \cdot \overline{CD} \cdot \overline{EF} \cdot \overline{GH} \cdot \overline{IJ} \cdot \overline{KL}$
ECL2509	(A+B) (C+D) (E+F) (G+H)	$\overline{A+B} + \overline{C+D} + \overline{E+F} + \overline{G+H}$	AB + CD + EF + GH	$\overline{AB} \cdot \overline{CD} \cdot \overline{EF} \cdot \overline{GH}$
ECL2510	(A+B) (C+D+E) (F+G+H) (I+J+K)	$\overline{A+B} + \overline{C+D+E} + \overline{F+G+H} + \overline{I+J+K}$	AB + CDE + FGH + IJK	$\overline{AB} \cdot \overline{CDE} \cdot \overline{FGH} \cdot \overline{IJK}$
ECL2512		$\overline{A+D} + \overline{B+E} + \overline{C+F}$		$\overline{AD} \cdot \overline{BE} \cdot \overline{CF}$
ECL2513	(A+B) (C+D)	$\overline{A+B} + \overline{C+D}$	AB + CD	$\overline{AB} \cdot \overline{CD}$

NC—No internal connection ◇— Collector Dot

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GENERAL APPLICATION INFORMATION

Multiple V_{CC} terminals have been supplied to reduce crosstalk noise. All V_{CC} terminals should be connected even if all gates in a module are not used.

Applications of the multifunction gates at other than data sheet conditions are covered in a separate ECL2500 series application document.

The multifunction gates divide into two groups with internal wired connections as follows:

MODULE	COLLECTOR DOTS	EMITTER DOTS
ECL2513†	2	2
ECL2509	4	4
ECL2510	4	4

†Each half

MODULE	EMITTER DOTS
ECL2512†	3
ECL2506	4
ECL2507	5
ECL2508	6

†Each half

General loading for fan-out may be divided into two classes:

CLASS I **Short-Line or Cluster Loading.**

Loads which can be connected within two inches of any source can be treated as lumped capacitive loads which include the gate inputs and stub-line capacitances. Switching times can be interpolated accordingly. No two dotted outputs can be more than two inches apart for this case.

CLASS II **Long-Line or Distributive Loading.**

These loads must be treated as lumped loads along a transmission line and termination should be at the end of the transmission chain. No more than 20 pF of load is recommended per 4.5 inches of 50-ohm printed line (with dielectric constant of 4.5) in order that the reflection coefficient be no greater than 20%. If the loads are lumped loads of 20 pF, they must be 4.5 inches apart. If individual gates and CLASS I loads are distributed, they must not exceed the 20 pF per 4.5 inches of line.

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absolute maximum ratings (see note 1)

Terminal voltages and currents . . . . . See table below
Storage temperature range . . . . . −40°C to 150°C
Temperature range with supply and bias voltages applied . . . . . −40°C to 100°C

TERMINAL VOLTAGE AND/OR CURRENT, T_A = 0°C TO 75°C (SEE NOTES 2 AND 3)

TERMINAL	REMARKS	VOLTAGE		CURRENT
		CONTINUOUS	20-μs SURGE	
V_{CC}		2 V	4.5 V	
V_{EE}		−4 V	−7 V	
Each Input	All other inputs open	−3.5 V	−4 V	
		2 V	2 V	
Output Y	All inputs high			−40 mA
Output Z	All inputs low			−40 mA

4

recommended operating conditions

Supply voltage V_{CC} . . . . . 1.32 V ± 2%
Supply voltage V_{EE} . . . . . −3.2 V ± 2%
Reference voltage V_{BB} . . . . . 0 V (GND)
Reverse bias on unused inputs . . . . . −1 V ± 0.5 V
Normalized d-c fan-out . . . . . 0 to 35
Load on each output . . . . . characterized at 270 Ω to V_{EE}, 50 Ω to GND
Operating free-air temperature range . . . . . 0°C to 75°C

NOTES: 1. Absolute maximum ratings are limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing.
2. Maximum terminal conditions must be considered as mutually exclusive.
3. All voltages are referenced to V_{BB}, which is at GND.

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electrical characteristics at specified free-air temperature

PARAMETER		TEST FIGURE	TEST CONDITIONS*		MODULE							SEE NOTE 4			UNIT
					ECL2506	ECL2507	ECL2508	ECL2509	ECL2510	ECL2512	ECL2513	MIN	TYP	MAX	
V_{IH}	High-level input voltage			0°C 25°C 75°C	• • •	• • •	• • •	• • •	• • •	• • •	• • •	150 150 150		720 720 720	mV
V_{IL}	Low-level input voltage			0°C 25°C 75°C	• • •	• • •	• • •	• • •	• • •	• • •	• • •	−1500 −1500 −1500		−150 −150 −150	mV
$V_{OH(Y)}$	High-level output voltage at Y output	2	V_I = 0.2 V	0°C 25°C 75°C				• •	• •		• •	315 350	390 425 495	500 580	mV
$V_{OL(Y)}$	Low-level output voltage at Y output	2	V_I = −0.2 V	0°C 25°C 75°C				• •	• •		• •	−505 −490	−450 −410 −290	−350 −230	mV
$V_{OH(Z)}$	High-level output voltage at Z output	2	V_I = −0.2 V	0°C 25°C 75°C	• • •	• • •	• • •	• • •	• • •	• • •	• • •	315 350	390 425 495	500 580	mV
$V_{OL(Z)}$	Low-level output voltage at Z output	2	V_I = 0.2 V	0°C 25°C 75°C	• • •	• • •	• • •	• • •	• • •	• • •	• • •	−440	−385 −365 −325	−310 −280	mV
$V_{OL(Z)}$	Low-level output voltage at Z output	2	V_I = 0.4 V	0°C 25°C 75°C	• • •	• • •	• • •	• • •	• • •	• • •	• • •	−505 −490	−455 −425 −380	−315	mV
$V_{OH(Z)}$	High-level output voltage at Z output	2	V_I = −0.5 V	0°C 25°C 75°C	• • •	• • •	• • •	• • •	• • •	• • •	• • •			630† 700†	mV
$V_{OH(Y)}$	High-level output voltage at Y output	2	V_I = 0.15 V	0°C 25°C 75°C				• •	• •		• •	290 325			mV
$V_{OL(Y)}$	Low-level output voltage at Y output	2	V_I = −0.15 V	0°C 25°C 75°C				• •	• •		• •			−335 −215	mV
$V_{OH(Z)}$	High-level output voltage at Z output	2	V_I = −0.15 V	0°C 25°C 75°C	• • •	• • •	• • •			• •		290 325			mV
$V_{OL(Z)}$	Low-level output voltage at Z output	2	V_I = 0.15 V	0°C 25°C 75°C	• • •	• • •	• • •			• •				−290 −260	mV
I_{IH}	High-level input current (each input)	3	V_I = 0.5 V	0°C 25°C 75°C	• • •	• • •	• • •	• • •	• • •	• • •	• • •			255 235 200	μA
I_{IL}	Low-level input current	4	V_I = −3.2 V	0°C 25°C 75°C	• • •	• • •	• • •	• • •	• • •	• • •	• • •			−0.6‡ −0.8‡ −1.2‡	μA
I_{CC} or $-I_{EE}$	Supply current	5	V_I = −0.5 V	25°C	• • • • • • •	• • • • • • •	• • • • • • •	• • • • • • •	• • • • • • •	• • • • • • •	• • • • • • •	17 23 27 17 17 27 17		28 35 42 28 28 42 28	mA
C_{in}	Input capacitance (each input)		See Note 5	25°C	•	•	•	•	•	•	•		5		pF
z_{out}	Output impedance		See Note 6	25°C	•	•	•	•	•	•	•		5		Ω

*V_{BB} = GND, V_{CC} = 1.32 V ± 1%, V_{EE} = −3.20 V ± 1%.

†These are worst case values for ECL2508 which has six emitters dotted. See Supplementary Parameter Measurement Information for each module.

‡These are worst-case values for twelve inputs in parallel. See Supplementary Parameter Measurement Information for each module.

NOTES: 4. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.

5. C_{in} is measured using peak current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. C_{in} = Q/V.

6. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

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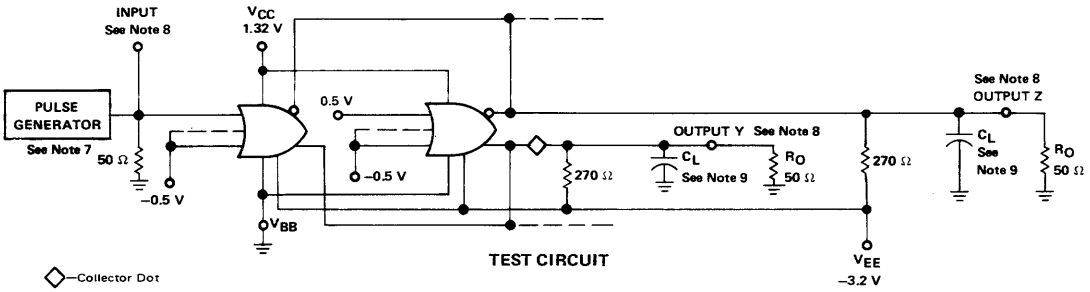
operating characteristics at specified free-air temperature (see figure 1)

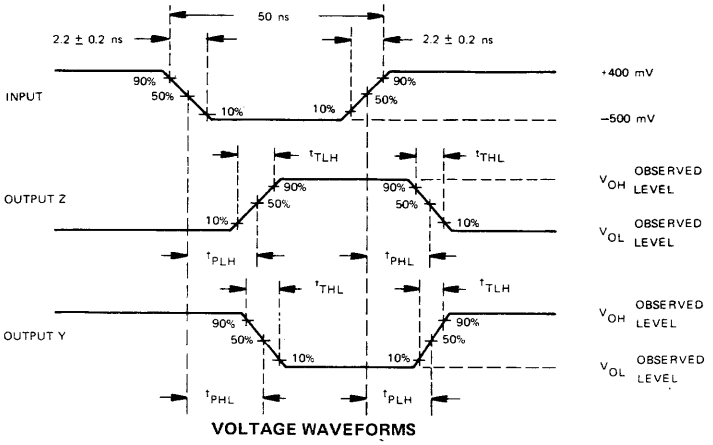
PARAMETER		C_L	T_A	ECL2506 THRU ECL2508, ECL2512			ECL2509, ECL2510, ECL2513			UNIT
				Z OUTPUTS			ANY OUTPUT			
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation delay time, high-to-low-level output and/or	4 pF	0°C		2.6			2.6		ns
			25°C	1.7	2.6	3.5	1.6	2.6	4.1	
			75°C		2.6			2.6		
t_{PLH}	Propagation delay time, low-to-high-level output	50 pF	0°C		3.6			3.5		ns
			25°C	2.4	3.6	4.5	2.5	3.5	4.6	
			75°C		3.6			3.6		
t_{THL}	Transition time, high-to-low-level output and/or	4 pF	0°C		4.0			3.4		ns
			25°C	2.8	4.0	5.6	2.0	3.4	6.3	
			75°C		4.1			3.5		
t_{TLH}	Transistion time, low-to-high-level output	50 pF	0°C		4.5			4.4		ns
			25°C	2.8	4.5	6.5	2.5	4.3	6.5	
			75°C		4.4			4.1		

4

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

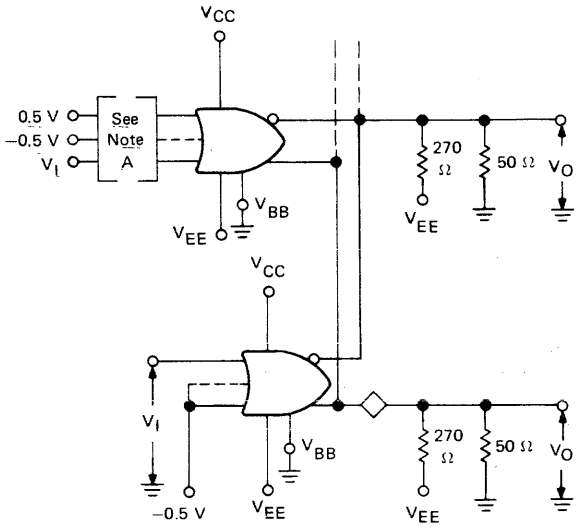


VOLTAGE WAVEFORMS

FIGURE 1—PROPAGATION DELAY AND TRANSITION TIMES

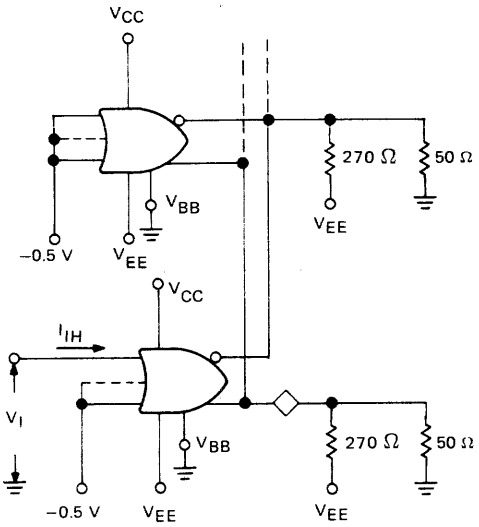
NOTES: 7. The generator has the following characteristics: Z_{out} = 50 Ω, PRR = 1 MHz.
8. The waveforms are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. Either a high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF, or a 50-Ω impedance system can be used. The 50-Ω resistors designated R_O are the oscilloscope input resistance in the 50-Ω system or discrete resistors with a high-impedance probe.
9. C_L includes probe and fixture capacitance. A capacitance of 50 pF can be used to approximate an a-c fan-out of 10.

PARAMETER MEASUREMENT INFORMATION†



A. The particular input voltages for each module are shown in the Supplementary Parameter Measurement Information Section.
B. V_I is applied to each input separately except where Note 13 applies.
C. Each output is tested separately.

FIGURE 2–V_{OH} and V_{OL}



Each input is tested separately.

FIGURE 3–I_{IH}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

◇ – Collector Dot

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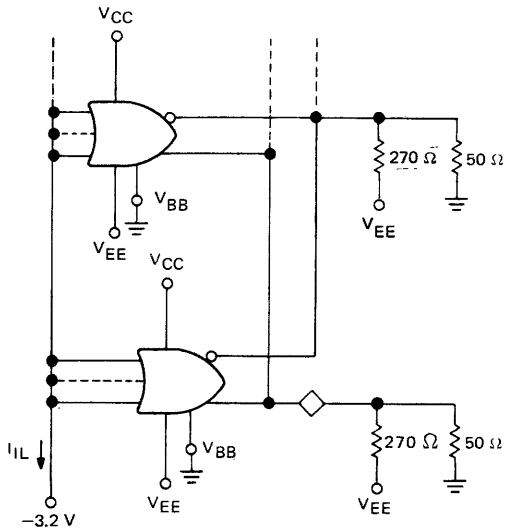
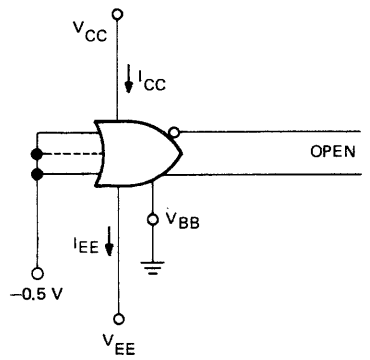
PARAMETER MEASUREMENT INFORMATION†



All inputs of all gates are connected in parallel.

FIGURE 4–I_{IL}



A. All gates are tested simultaneously.
B. I_{CC} is the total current into all V_{CC} terminals.

FIGURE 5–I_{CC} or I_{EE}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

◇ – Collector Dot

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATE(S)					
ECL2506	**V_{BB} (pin 15) = GND, V_{CC} (pin 3) = 1.32 V, V_{EE} (pin 10) = −3.2 V**										
$V_{OH(Z)}$	1, 2, 4 6, 7, 8 9, 11, 12 13, 14, 16	5	2	−0.2 V	−0.5 V	See Note 12	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
$V_{OL(Z)}$	1, 2, 4 6, 7, 8 9, 11, 12 13, 14, 16	5	2	0.2 V	−0.5 V	See Note 13	0°C 25°C 75°C	−440	−385 −365 −325	−310 −280	mV
$V_{OL(Z)}$	1, 2, 4 6, 7, 8 9, 11, 12 13, 14, 16	5	2	0.4 V	−0.5 V	See Note 13	0°C 25°C 75°C	−505 −490	−455 −425 −380	 −315	mV
$V_{OH(Z)}$	1, 2, 4 6, 7, 8 9, 11, 12 13, 14, 16	5	2	All inputs of all gates in parallel at −0.5 V			0°C 25°C 75°C			615 685	mV
$V_{OH(Z)}$	4	5	2	−0.15 V	−0.5 V	See Note 12	0°C 25°C 75°C	290 325			mV
$V_{OL(Z)}$	4	5	2	0.15 V	−0.5 V	See Note 13	0°C 25°C 75°C			−290 −260	mV
I_{IH}	1, 2, 4 6, 7, 8 9, 11, 12 13, 14, 16		3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			255 235 200	μA
I_{IL}	1, 2, 4, 6, 7, 8, 9, 11, 12, 13, 14, 16		4	All inputs of all gates in parallel at −3.2 V			0°C 25°C 75°C			−0.6 −0.8 −1.2	μA

NOTES: 10. See page 8 for defining term associated with each symbol.
11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.
12. At least one input of each other gate must be at 0.5 V. Other inputs are biased to −0.5 V.
13. One input of each gate must be at V_I. Other inputs are biased to −0.5 V.

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SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATE(S)					
ECL2507	**V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V**										
$V_{OH(Z)}$	1, 2 7, 8 9, 11 12, 13 14, 16	5	2	−0.2 V	−0.5 V	See Note 12	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
$V_{OL(Z)}$	1, 2 7, 8 9, 11 12, 13 14, 16	5	2	0.2 V	−0.5 V	See Note 13	0°C 25°C 75°C	−440	−385 −365 −325	−310 −280	mV
$V_{OL(Z)}$	1, 2 7, 8 9, 11 12, 13 14, 16	5	2	0.4 V	−0.5 V	See Note 13	0°C 25°C 75°C	−505 −490	−455 −425 −380	 −315	mV
$V_{OH(Z)}$	1, 2 7, 8 9, 11 12, 13 14, 16	5	2	All inputs of all gates in parallel at −0.5 V			0°C 25°C 75°C			 625 695	mV
$V_{OH(Z)}$	2	5	2	−0.15 V	−0.5 V	See Note 12	0°C 25°C 75°C	290 325			mV
$V_{OL(Z)}$	2	5	2	0.15 V	−0.5 V	See Note 13	0°C 25°C 75°C			−290 −260	mV
I_{IH}	1, 2 7, 8 9, 11 12, 13 14, 16		3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			255 235 200	μA
I_{IL}	1, 2, 7, 8, 9, 11, 12, 13, 14, 16		4	All inputs of all gates in parallel at −3.2 V			0°C 25°C 75°C			−0.5 −0.7 −1.0	μA

NOTES: 10. See page 8 for defining term associated with each symbol.
11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.
12. At least one input of each other gate must be at 0.5 V. Other inputs are biased to −0.5 V.
13. One input of each gate must be at V_I. Other inputs are biased to −0.5 V.

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATE(S)					
ECL2508	V_{BB} (pin 15) = GND, V_{CC} (pin 3) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Z)}$	1, 16 2, 4 6, 7 8, 9 11, 12 13, 14	5	2	−0.2 V	−0.5 V	See Note 12	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
$V_{OL(Z)}$	1, 16 2, 4 6, 7 8, 9 11, 12 13, 14	5	2	0.2 V	−0.5 V	See Note 13	0°C 25°C 75°C	−440	−385 −365 −325	−310 −280	mV
$V_{OL(Z)}$	1, 16 2, 4 6, 7 8, 9 11, 12 13, 14	5	2	0.4 V	−0.5 V	See Note 13	0°C 25°C 75°C	−505 −490	−455 −425 −380	 −315	mV
$V_{OH(Z)}$	1, 16 2, 4 6, 7 8, 9 11, 12 13, 14	5	2	All inputs of all gates in parallel at −0.5 V			0°C 25°C 75°C			 630 700	mV
$V_{OH(Z)}$	11	5	2	−0.15 V	−0.5 V	See Note 12	0°C 25°C 75°C	290 325			mV
$V_{OL(Z)}$	11	5	2	0.15 V	−0.5 V	See Note 13	0°C 25°C 75°C			 −290 −260	mV
I_{IH}	1, 16 2, 4 6, 7 8, 9 11, 12 13, 14		3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			255 235 200	μA
I_{IL}	1, 2, 4, 6, 7, 8, 9, 11, 12, 13, 14, 16		4	All inputs of all gates in parallel at −3.2 V			0°C 25°C 75°C			−0.6 −0.8 −1.2	μA

NOTES: 10. See page 8 for defining term associated with each symbol.
11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.
12. At least one input of each other gate must be at 0.5 V. Other inputs are biased to −0.5 V.
13. One input of each gate must be at V_I. Other inputs are biased to −0.5 V.

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SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATE(S)					
ECL2509	V_{BB} (pin 15) = GND, V_{CC} (pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Y)}$	1, 16 8, 9 11, 12 13, 14	7	2	0.2 V	−0.5 V	0.5 V	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
$V_{OL(Y)}$	1, 16 8, 9 11, 12 13, 14	7	2	−0.2 V	−0.5 V	See Note 12	0°C 25°C 75°C	−505 −490	−450 −410 −290	−350 −230	mV
$V_{OH(Z)}$	1, 16 8, 9 11, 12 13, 14	5	2	−0.2 V	−0.5 V	See Note 12	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
$V_{OL(Z)}$	1, 16 8, 9 11, 12 13, 14	5	2	0.2 V	−0.5 V	See Note 13	0°C 25°C 75°C	−440	−385 −365 −325	−310 −280	mV
$V_{OL(Z)}$	1, 16 8, 9 11, 12 13, 14	5	2	0.4 V	−0.5 V	See Note 13	0°C 25°C 75°C	−505 −490	−455 −425 −380	−315	mV
$V_{OH(Z)}$	1, 16 8, 9 11, 12 13, 14	5	2	All inputs of all gates in parallel at −0.5 V			0°C 25°C 75°C			615 685	mV
$V_{OH(Y)}$	8	7	2	0.15 V	−0.5 V	See Note 13	0°C 25°C 75°C	290 325			mV
$V_{OL(Y)}$	8	7	2	−0.15 V	−0.5 V	See Note 12	0°C 25°C 75°C			−335 −215	mV
I_{IH}	1, 16 8, 9 11, 12 13, 14		3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			255 235 200	μA
I_{IL}	1, 8, 9, 11, 12, 13, 14, 16		4	All inputs of all gates in parallel at −3.2 V			0°C 25°C 75°C			−0.5 −0.6 −0.8	μA

NOTES: 10. See page 8 for defining term associated with each symbol.
11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.
12. At least one input of each other gate must be at 0.5 V. Other inputs are biased to −0.5 V.
13. One input of each gate must be at V_I. Other inputs are biased to −0.5 V.

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SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATE(S)					
ECL2510	**V_{BB} (pin 15) = GND, V_{CC} (pin 3) = 1.32 V, V_{EE} (pin 10) = −3.2 V**										
$V_{OH(Y)}$	1, 2 6, 7, 8 9, 11, 12 13, 14, 16	4	2	0.2 V	−0.5 V	0.5 V	0°C 25°C 75°C	315 350	390 425 495	 500 580	mV
$V_{OL(Y)}$	1, 2 6, 7, 8 9, 11, 12 13, 14, 16	4	2	−0.2 V	−0.5 V	See Note 12	0°C 25°C 75°C	−505 −490	−450 −410 −290	 −350 −230	mV
$V_{OH(Z)}$	1, 2 6, 7, 8 9, 11, 12 13, 14, 16	5	2	−0.2 V	−0.5 V	See Note 12	0°C 25°C 75°C	315 350	390 425 495	 500 580	mV
$V_{OL(Z)}$	1, 2 6, 7, 8 9, 11, 12 13, 14, 16	5	2	0.2 V	−0.5 V	See Note 13	0°C 25°C 75°C	−440	−385 −365 −325	 −310 −280	mV
$V_{OL(Z)}$	1, 2 6, 7, 8 9, 11, 12 13, 14, 16	5	2	0.4 V	−0.5 V	See Note 13	0°C 25°C 75°C	−505 −490	−455 −425 −380	 −315	mV
$V_{OH(Z)}$	1, 2 6, 7, 8 9, 11, 12 13, 14, 16	5	2	All inputs of all gates in parallel at −0.5 V			0°C 25°C 75°C			 615 685	mV
$V_{OH(Y)}$	2	4	2	0.15 V	−0.5 V	See Note 13	0°C 25°C 75°C	290 325			mV
$V_{OL(Y)}$	2	4	2	−0.15 V	−0.5 V	See Note 12	0°C 25°C 75°C			 −335 −215	mV
I_{IH}	1, 2 6, 7, 8 9, 11, 12 13, 14, 16		3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			255 235 200	μA
I_{IL}	1, 2, 6, 7, 8, 9, 11, 12, 13, 14, 16		4	All inputs of all gates in parallel at −3.2 V			0°C 25°C 75°C			−0.6 −0.8 −1.1	μA

NOTES: 10. See page 8 for defining term associated with each symbol.
11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.
12. At least one input of each other gate must be at 0.5 V. Other inputs are biased to −0.5 V.
13. One input of each gate must be at V_I. Other inputs are biased to −0.5 V.

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	REMAINING INPUTS OF OTHER GATE(S)					
ECL2512	V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Z)}$	1, 7 11, 16 13, 14	4	2	−0.2 V	−0.5 V	0.5 V	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
	7, 8 9, 11 12, 13	5									
$V_{OL(Z)}$	1, 7 11, 16 13, 14	4	2	0.2 V	−0.5 V	See Note 13	0°C 25°C 75°C	−440	−385 −365 −325	−310 −280	mV
	7, 8 9, 11 12, 13	5									
$V_{OL(Z)}$	1, 7 11, 16 13, 14	4	2	0.4 V	−0.5 V	See Note 13	0°C 25°C 75°C	−505 −490	−455 −425 −380	−315	mV
	7, 8 9, 11 12, 13	5									
$V_{OH(Z)}$	1, 7 11, 16 13, 14	4	2	All inputs of all gates in parallel at −0.5 V			0°C 25°C 75°C			600 670	mV
	7, 8 9, 11 12, 13	5									
$V_{OH(Z)}$	8	5	2	−0.15 V	−0.5 V	0.5 V	0°C 25°C 75°C	290 325			mV
$V_{OL(Z)}$	8	5	2	0.15 V	−0.5 V	See Note 13	0°C 25°C 75°C			−290 −260	mV
I_{IH}	1 16 14 8 9 12		3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			255 235 200	μA
	7, 11, 13		3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			510 470 400	μA
I_{IL}	1, 7, 8, 9, 11, 12, 13, 14, 16		4	All inputs of all gates in parallel at −3.2 V			0°C 25°C 75°C			−0.6 −0.8 −1.2	μA

NOTES: 10. See page 8 for defining term associated with each symbol.
11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.
13. One input of each gate must be at V_I. Other inputs are biased to −0.5 V.

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	REMAINING INPUTS OF OTHER GATE(S)					
ECL2513	V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Y)}$	14, 16	4	2	0.2 V	−0.5 V	0.5 V	0°C	315	390		mV
	12, 13						25°C	350	425	500	
	8, 9	5					75°C		495	580	
	11, 12										
$V_{OL(Y)}$	14, 16	4	2	−0.2 V	−0.5 V	0.5 V	0°C	−505	−450		mV
	12, 13						25°C	−490	−410	−350	
	8, 9	5					75°C		−290	−230	
	11, 12										
$V_{OH(Z)}$	14, 16	2	2	−0.2 V	−0.5 V	0.5 V	0°C	315	390		mV
	12, 13						25°C	350	425	500	
	8, 9	7					75°C		495	580	
	11, 12										
$V_{OL(Z)}$	14, 16	2	2	0.2 V	−0.5 V	See Note 13	0°C		−385		mV
	12, 13						25°C	−440	−365	−310	
	8, 9	7					75°C		−325	−280	
	11, 12										
$V_{OL(Z)}$	14, 16	2	2	0.4 V	−0.5 V	See Note 13	0°C	−505	−455		mV
	12, 13						25°C	−490	−425		
	8, 9	7					75°C		−380	−315	
	11, 12										
$V_{OH(Z)}$	14, 16	2	2	All inputs of all gates in parallel at −0.5 V			0°C				mV
	12, 13						25°C			580	
	8, 9	7					75°C			650	
	11, 12										
$V_{OH(Y)}$	13	4	2	0.15 V	−0.5 V	0.5 V	0°C	290			mV
							25°C	325			
							75°C				
$V_{OL(Y)}$	13	4	2	−0.15 V	−0.5 V	0.5 V	0°C				mV
							25°C			−335	
							75°C			−215	
I_{IH}	14, 16		3	0.5 V	−0.5 V	−0.5 V	0°C			255	μA
	13						25°C			235	
	8, 9						75°C			200	
	11										
	12		3	0.5 V	−0.5 V	−0.5 V	0°C			510	μA
							25°C			470	
							75°C			400	
I_{IL}	8, 9, 11, 12, 13, 14, 16		4	All inputs of all gates in parallel at −3.2 V			0°C			−0.5	μA
							25°C			−0.6	
							75°C			−0.8	

NOTES: 10. See page 8 for defining term associated with each symbol.
11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.
13. One input of each gate must be at V_I. Other inputs are biased to −0.5 V.

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SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

operating characteristics at specified free-air temperature (see figure 1)

TERMINALS TO BE TESTED (SEE NOTES 16, 17, 18, AND 19)								C_L	t_{PHL} and/or t_{PLH} PROPAGATION TIMES—ns						t_{THL} and/or t_{TLH} TRANSITION TIMES—ns					
									$T_A = 0°C$			$T_A = 25°C$			$T_A = 75°C$			$T_A = 0°C$			$T_A = 25°C$			$T_A = 75°C$		
INPUT		OUTPUT		INPUT		OUTPUT		pF	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
ECL2506																										
1		6		9		13		4		2.6		1.7	2.6	3.5		2.6			4.0		2.8	4.0	5.6		4.1	
2	5	7	5	11	5	14	5																			
4		8		12		16		50		3.6		2.4	3.6	4.5		3.6			4.5		2.8	4.5	6.5		4.4	
ECL2507																										
1	5	7	5	9	5	12	5	4		2.6		1.7	2.6	3.5		2.6			4.0		2.8	4.0	5.6		4.1	
2		8		11		13		50		3.6		2.4	3.6	4.5		3.6			4.5		2.8	4.5	6.5		4.4	
14	5							4		2.6		1.7	2.6	3.5		2.6			4.0		2.8	4.0	5.6		4.1	
16								50		3.6		2.4	3.6	4.5		3.6			4.5		2.8	4.5	6.5		4.4	
ECL2508																										
1	5	2	5	6	5	8	5	4		2.6		1.7	2.6	3.5		2.6			4.0		2.8	4.0	5.6		4.1	
16		4		7		9		50		3.6		2.4	3.6	4.5		3.6			4.5		2.8	4.5	6.5		4.4	
11	5	13	5					4		2.6		1.7	2.6	3.5		2.6			4.0		2.8	4.0	5.6		4.1	
12		14						50		3.6		2.4	3.6	4.5		3.6			4.5		2.8	4.5	6.5		4.4	
ECL2509																										
1	7	8	7	11	7	13	7	4		2.6		1.6	2.6	4.1		2.6			3.4		2.0	3.4	6.3		3.5	
16	5	9	5	12	5	14	5	50		3.5		2.5	3.5	4.6		3.6			4.4		2.5	4.3	6.5		4.1	
ECL2510																										
1	4	6	4	9	4	13	4	4		2.6		1.6	2.6	4.1		2.6			3.4		2.0	3.4	6.3		3.5	
		7		11		14																				
2	5	8	5	12	5	16	5	50		3.5		2.5	3.5	4.6		3.6			4.4		2.5	4.3	6.5		4.1	
ECL2512																										
1	4	11	4	13	4	7	5	4		2.6		1.7	2.6	3.5		2.6			4.0		2.8	4.0	5.6		4.1	
7		16		14		8		50		3.6		2.4	3.6	4.5		3.6			4.5		2.8	4.5	6.5		4.4	
9	5	12	5					4		2.6		1.7	2.6	3.5		2.6			4.0		2.8	4.0	5.6		4.1	
11		13						50		3.6		2.4	3.6	4.5		3.6			4.5		2.8	4.5	6.5		4.4	
ECL2513																										
14	4	12	4	8	5	11	5	4		2.6		1.6	2.6	4.1		2.6			3.4		2.0	3.4	6.3		3.5	
16	2	13	2	9	7	12	7	50		3.5		2.5	3.5	4.6		3.6			4.4		2.5	4.3	6.5		4.1	

NOTES: 16. Each gate is tested separately. At least one input of each of the other gates (excluding the inactive half of the ECL2512 or ECL2513) must be at 0.5 V with the other inputs at −0.5 V.

17. The input pulse is measured as it is applied sequentially to each input of the gate under test, and a waveform measurement is made at each of the outputs of that gate. Times are as defined in Figure 1.

18. Other inputs of the same gate as input under test are at −0.5 V.

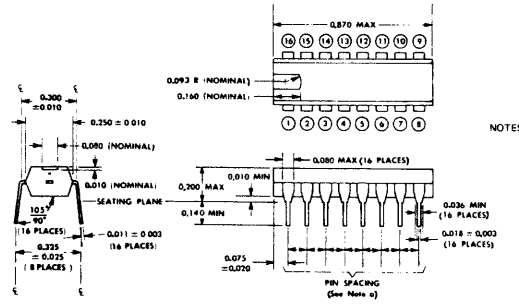
19. Bias voltages and loads for the half of the ECL2512 and ECL2513 under test are shown in Figure 1. The inactive half has remaining inputs biased to −0.5 V, outputs under load, and power applied.

mechanical data

The circuit bars are mounted on a 16-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

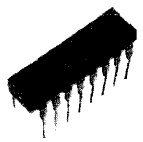
The plastic case is electrically nonconductive.

16-PIN PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



NOTES: a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within 0.010 of its true longitudinal position relative to pins 1 and 16.

b. All dimensions are in inches unless otherwise noted.



terminal designations

Pin assignments are shown in the table below and correspond to the logic diagrams on pages 4 and 5.

Outputs are denoted by Y or Z. Inputs are denoted by A, B, C, etc.

Respective inputs and outputs are identified by a gate number preceding the pin symbol.

Power is supplied via the V_{CC}, V_{EE}, and V_{BB} terminals.

V_{BB} is a reference voltage.

NC indicates no internal connection.

PIN ASSIGNMENTS

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ECL2506	A	B	V_{CC}	C	Z	D	E	F	G	V_{EE}	H	I	J	K	V_{BB}	L
ECL2507	A	B	V_{CC}	NC	Z	V_{CC}	C	D	E	V_{EE}	F	G	H	I	V_{BB}	J
ECL2508	A	C	V_{CC}	D	Z	E	F	G	H	V_{EE}	I	J	K	L	V_{BB}	B
ECL2509	A	NC	NC	NC	Z	V_{CC}	Y	C	D	V_{EE}	E	F	G	H	V_{BB}	B
ECL2510	A	B	V_{CC}	Y	Z	C	D	E	F	V_{EE}	G	H	I	J	V_{BB}	K
ECL2512	1A	NC	V_{CC}	1Z	2Z	V_{CC}	D	2A	2B	V_{EE}	E	2C	F	1C	V_{BB}	1B
ECL2513	NC	1Z	V_{CC}	1Y	2Y	V_{CC}	2Z	2A	2B	V_{EE}	2C	D	1C	1A	V_{BB}	1B

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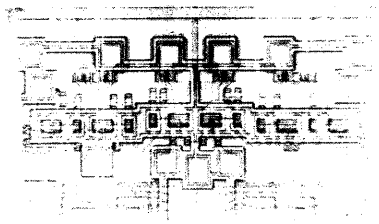
TYPES ECL2515, ECL2516 EMITTER-COUPLED-LOGIC ARITHMETIC MODULES

TYPES ECL2515, ECL2516
BULLETIN NO. DL-S 7011295, JANUARY 1970

ECL2500 SERIES EMITTER-COUPLED-LOGIC (ECL) ARITHMETIC MODULES FOR APPLICATION IN ULTRA-HIGH-SPEED DIGITAL SYSTEMS



description

The ECL2500 series is a compatible family of ECL functions with basic gate delays of 2 to 3 ns per stage. The family is specifically designed for operation from 0°C to 75°C.

The ECL2500 family includes:

- Basic Gate Modules
- Multifunction Gate Modules
- Bistable Modules
- **Arithmetic Modules**
- Interface Modules
- Memory Module

family features

- High speed. . .typical gate propagation delay time of 2.5 ns
- Complementary OR/NOR outputs with capability for wired-OR connections
- Designed for use with transmission lines to ensure maximum signal transmission without noise. Characterized for 50-ohm lines
- High noise immunity: ±225 mV typical at 25°C

This data sheet covers the arithmetic modules.
Separate data sheets cover the balance of the ECL2500 modules.

ECL2500 series arithmetic modules

The ECL2500 series arithmetic modules are summarized in the table below. These modules contain the multifunction ECL circuits shown in the schematics of Figures A and B. The basic principle of collector dotting and emitter dotting, used in both modules, is the shown in Figure C. Logic diagrams of ECL2515 and ECL2516 are shown on page 4.

SUMMARY OF ARITHMETIC MODULES

MODULE	GATES PER MODULE	INPUTS PER GATE	POSITIVE LOGIC	OUTPUTS OF MODULE
ECL2515 GROUP CARRY	5	1, 2, 3, 4, 5	OR-AND/NOR-OR	Y and Z
ECL2516 FULL SUM-CARRY ADDER	7	2, 2, 2, 3, 3, 3, 3	OR-AND/NOR-OR	Σ, $\overline{\Sigma}$, C_O, and $\overline{C}_O$

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schematic

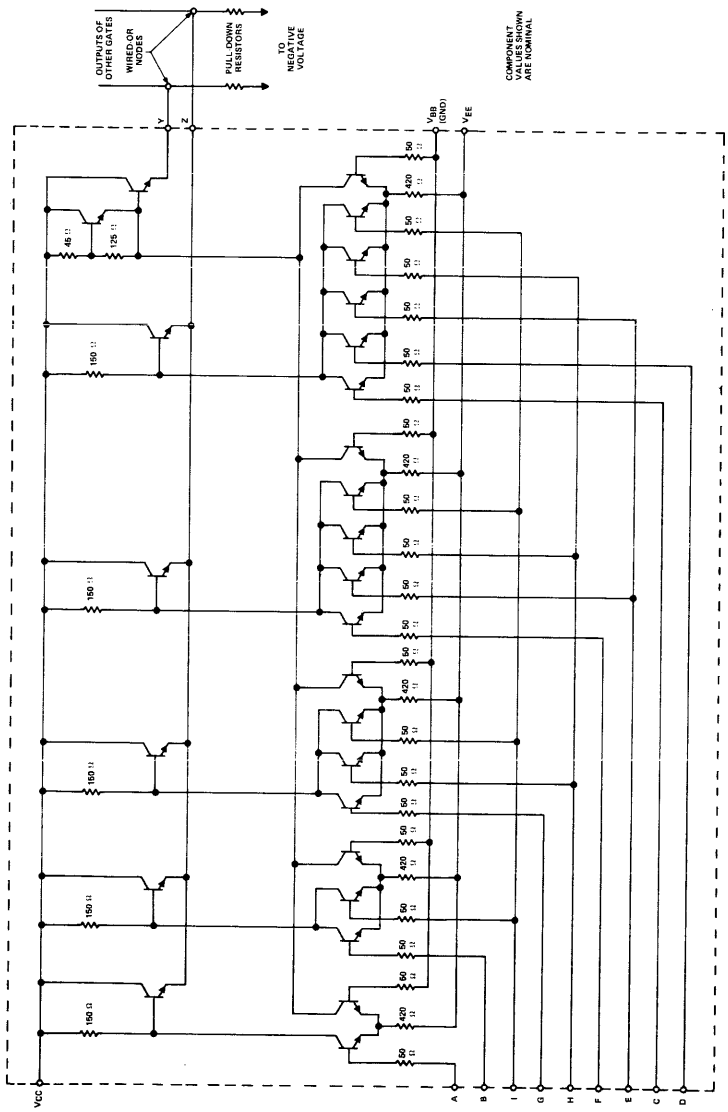

FIGURE A–SCHEMATIC OF ECL2515

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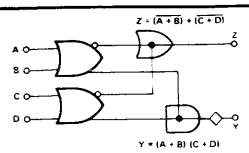
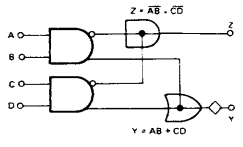
logic



POSITIVE LOGIC

◇ —Collector dot
For ECL2516:
$Y = \Sigma$ or C_O
$Z = \overline{\Sigma}$ or $\overline{C_O}$



NEGATIVE LOGIC

FIGURE C—WIRED-OR/AND LOGIC DIAGRAM

schematic

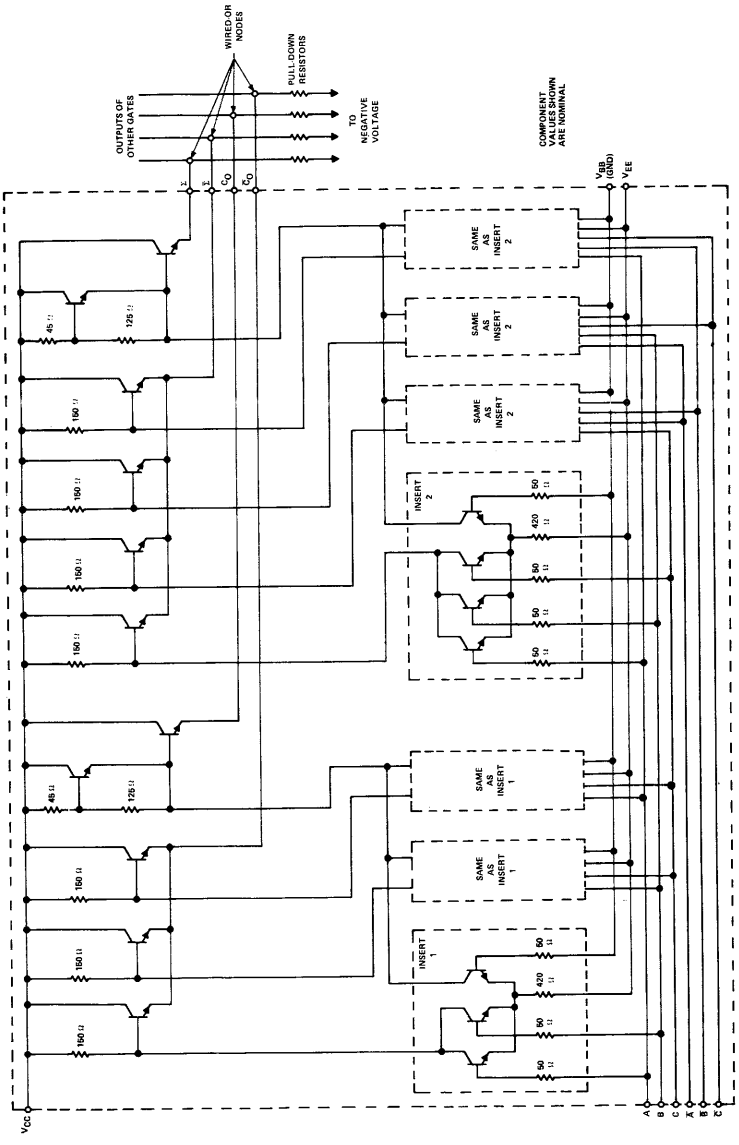


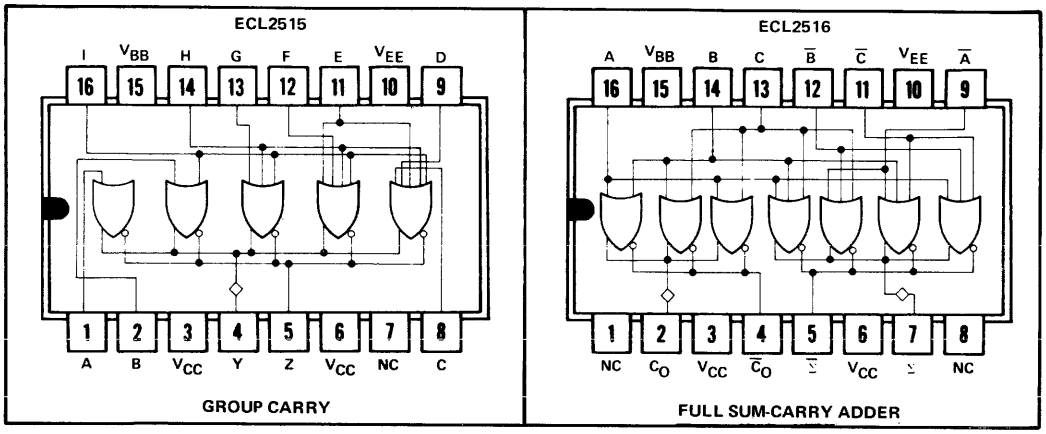
FIGURE B—SCHEMATIC OF ECL2516

Positive logic OR-AND/NOR-OR functions or negative logic AND-OR/NAND-AND functions are provided at the various outputs of ECL2515 and ECL2516 as shown in the logic table.
Emitter-follower outputs require an external pull-down resistor. The wired-OR function can be obtained by connecting emitter-follower outputs of other modules together. Only one pull-down resistor is required for each wired-OR node. Each output of a module can be wired-OR connected independently of the other outputs of the module.

4

TYPES ECL2515, ECL2516
EMITTER-COUPLED-LOGIC ARITHMETIC MODULES

logic



4

◇—Collector dot
NC—No internal connection

MODULE	POSITIVE LOGIC		NEGATIVE LOGIC	
	IN-PHASE OUTPUT	OUT-OF-PHASE OUTPUT	IN-PHASE OUTPUT	OUT-OF-PHASE OUTPUT
ECL2515	$Y = A(B+I)(G+H+I) \cdot (E+F+H+I)(C+D+E+H+I)$	$\bar{Z} = \bar{A}+\bar{B}\bar{I}+\bar{G}\bar{H}\bar{I}+\overline{E+F+H+I}+\overline{C+D+E+H+I}$	$Y = A+BI+GHI+EFHI+CDEHI$	$Z = \bar{A} \cdot \bar{B}\bar{I} \cdot \bar{G}\bar{H}\bar{I} \cdot \overline{EFHI} \cdot \overline{CDEHI}$
ECL2516	$\Sigma = (A+B+C)(\bar{A}+\bar{B}+C) \cdot (\bar{A}+B+\bar{C})(A+\bar{B}+\bar{C})$	$\bar{\Sigma} = \overline{A+B+C}+\overline{\bar{A}+\bar{B}+C}+\overline{A+B+\bar{C}}+\overline{A+\bar{B}+\bar{C}}$	$\Sigma = ABC+\bar{A}\bar{B}C+\bar{A}B\bar{C}+A\bar{B}\bar{C}$	$\bar{\Sigma} = \overline{ABC} \cdot \overline{\bar{A}\bar{B}C} \cdot \overline{\bar{A}B\bar{C}} \cdot \overline{A\bar{B}\bar{C}}$
	$C_O = (A+B)(B+C)(A+C)$	$\bar{C}_O = \overline{A+B}+\overline{B+C}+\overline{A+C}$	$C_O = AB+BC+AC$	$\bar{C}_O = \overline{AB} \cdot \overline{BC} \cdot \overline{AC}$

truth tables (for this series, H = positive voltage, L = negative voltage, X = irrelevant)

ECL2515

INPUTS									OUTPUTS	
A	B	C	D	E	F	G	H	I	Y	Z
L	X	X	X	X	X	X	X	X	L	H
X	L	X	X	X	X	X	X	L	L	H
X	X	X	X	X	X	L	L	L	L	H
X	X	X	X	L	L	X	L	L	L	H
X	X	L	L	L	X	X	L	L	L	H
For a LOW Y and HIGH Z, all inputs to at least one gate must be LOW. For a HIGH Y and LOW Z, at least one input of each gate must be HIGH.										
H	X	X	X	X	X	X	X	H	H	L
H	H	X	X	X	X	X	H	X	H	L
H	H	X	X	H	X	H	X	X	H	L
H	H	X	H	X	H	H	X	X	H	L
H	H	H	X	X	H	H	X	X	H	L

ECL2516

INPUTS						OUTPUTS			
A	B	C	Ā	B̄	C̄	Σ	Σ̄	C_O	$\bar{C}_O$
L	L	L	H	H	H	L	H	L	H
L	L	H	H	H	L	H	L	L	H
L	H	L	H	L	H	H	L	L	H
L	H	H	H	L	L	L	H	H	L
H	L	L	L	H	H	H	L	L	H
H	L	H	L	H	L	L	H	H	L
H	H	L	L	L	H	L	H	H	L
H	H	H	L	L	L	H	L	H	L

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absolute maximum ratings (see note 1)

Terminal voltages and currents	See table below
Storage temperature range	−40°C to 150°C
Temperature range with supply and bias voltages applied	−40°C to 100°C

TERMINAL VOLTAGE AND/OR CURRENT, T_A = 0°C TO 75°C (SEE NOTES 2 AND 3)

TERMINAL	REMARKS	VOLTAGE		CURRENT
		CONTINUOUS	20-μs SURGE	
V_{CC}		2 V	4.5 V	
V_{EE}		−4 V	−7 V	
Each Input	All other inputs open	−3.5 V	−4 V	
		2 V	2 V	
Output Y†	All inputs high			−40 mA
Output Z†	All inputs low			−40 mA

†For ECL2516: Y = Σ or C_o, Z = $\overline{\Sigma}$ or $\overline{C}_o$

recommended operating conditions

Supply voltage V_{CC}	1.32 V ± 2%
Supply voltage V_{EE}	−3.2 V ± 2%
Reference voltage V_{BB}	0 V (GND)
Reverse bias on unused inputs	−1 V ± 0.5 V
Normalized d-c fan-out	0 to 35
Load on each output	characterized at 270 Ω to V_{EE}, 50 Ω to GND
Operating free-air temperature range	0°C to 75°C

NOTES: 1. Absolute maximum ratings are limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing.
2. Maximum terminal conditions must be considered as mutually exclusive.
3. All voltages are referenced to V_{BB}, which is at GND.

ECL2515 electrical characteristics at specified free-air temperature

PARAMETER		TEST FIGURE	TEST CONDITIONS* TERMINALS (SEE NOTE 4) INPUTS	TEST CONDITIONS* TERMINALS (SEE NOTE 4) OUTPUTS Y	Z	TEST CONDITIONS* INPUT CONDITIONS: INPUT UNDER TEST, V_I	OTHER INPUT(S) OF SAME GATE	REMAINING INPUTS OF OTHER GATES	T_A	MIN (SEE NOTE 5)	TYP (SEE NOTE 5)	MAX (SEE NOTE 5)	UNIT
V_{IH}	High-level input voltage								0°C	150		720	mV
									25°C	150		720	
									75°C	150		720	
V_{IL}	Low-level input voltage								0°C	−1500		−150	mV
									25°C	−1500		−150	
									75°C	−1500		−150	
$V_{OH(Y)}$	High-level output voltage at Y output	2	1	4		0.2 V	−0.5 V	0.5 V	0°C	315	390		mV
			2, 16						25°C	350	425	500	
			13, 14, 16						75°C		495	580	
			11, 12, 14, 16										
			8, 9, 11, 14, 16										
$V_{OL(Y)}$	Low-level output voltage at Y output	2	Same as for $V_{OH(Y)}$ above			−0.2 V	−0.5 V	0.5 V	0°C	−505	−450		mV
									25°C	−490	−410	−350	
									75°C		−290	−230	
$V_{OH(Z)}$	High-level output voltage at Z output	2	1	5		−0.2 V	−0.5 V	0.5 V	0°C	315	390		mV
			2, 16						25°C	350	425	500	
			13, 14, 16						75°C		495	580	
			11, 12, 14, 16										
			8, 9, 11, 14, 16										
$V_{OL(Z)}$	Low-level output voltage at Z output	2	Same as for $V_{OH(Z)}$ above			0.2 V	−0.5 V	See Note 6	0°C		−385		mV
									25°C	−440	−365	−310	
									75°C		−325	−280	
$V_{OL(Z)}$	Low-level output voltage at Z output	2	Same as for $V_{OH(Z)}$ above			0.4 V	−0.5 V	See Note 6	0°C	−505	−455		mV
									25°C	−490	−425		
									75°C		−380	−315	
$V_{OH(Z)}$	High-level output voltage at Z output	2	Same as for $V_{OH(Z)}$ above			All inputs of all gates in parallel at −0.5 V			0°C				mV
									25°C			625	
									75°C			695	
$V_{OH(Y)}$	High-level output voltage at Y output	2	1	4		0.15 V	−0.5 V	0.5 V	0°C	290			mV
									25°C	325			
									75°C				
$V_{OL(Y)}$	Low-level output voltage at Y output	2	1	4		−0.15 V	−0.5 V	0.5 V	0°C				mV
									25°C			−335	
									75°C			−215	
I_{IH}	High-level input current (each input)	3	1, 2, 8, 9, 12, 13			0.5 V	0.5 V	−0.5 V	0°C			255	μA
			11, 14, 16 See Note 7						25°C			235	
									75°C			200	
I_{IL}	Low-level input current (all inputs)	4	1, 2, 8, 9, 11, 12, 13, 14, 16			All inputs of all gates in parallel at −3.2 V			0°C			−0.8	μA
									25°C			−1	
									75°C			−1.5	
I_{CC} or I_{EE}	Supply current	5				All inputs of all gates in parallel at −0.5 V			25°C	20		36	mA
C_{in}	Input capacitance (see Note 8)								25°C		5		pF
z_{out}	Output impedance (see Note 9)			4	5				25°C		5		Ω

*V_{BB} (pin 15) = GND, V_{CC} (pins 3 and 6) = 1.32 V ±1%, V_{EE} (pin 10) = −3.20 V ±1%.

NOTES:
4. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.
5. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.
6. One input of each gate must be at V_I. Other inputs are biased to −0.5 V.
7. Terminals 11, 14, and 16 are internally connected to 2, 3, and 4 gates respectively, and maximum I_{IH} for these terminals at each temperature can be determined by multiplying the value given for I_{IH} by 2, 3, or 4 respectively.
8. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. C_{in} = Q/V. When a terminal is an input to more than one gate, multiply the value given by the number of gates to which this terminal is an input.
9. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

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ECL2516 electrical characteristics at specified free-air temperature†

PARAMETER		TEST CONDITIONS*						T_A	MIN	TYP	MAX	UNIT
		TEST FIGURE	TERMINALS (SEE NOTE 4)		INPUT CONDITIONS					(SEE NOTE 5)		
			INPUTS	OUTPUTS Y Z	INPUT UNDER TEST, V_I	OTHER INPUT(S) OF SAME GATE	REMAINING INPUTS OF OTHER GATES					
V_{IH}	High-level input voltage							0°C	150		720	mV
								25°C	150		720	
								75°C	150		720	
V_{IL}	Low-level input voltage							0°C	−1500		−150	mV
								25°C	−1500		−150	
								75°C	−1500		−150	
$V_{OH(Y)}$	High-level output voltage at Y output	2	16, 14 / 14, 13 / 16, 13	2	0.2 V	−0.5 V	0.5 V	0°C	315	390		mV
			16, 14, 13 / 9, 12, 13 / 9, 14, 11 / 16, 12, 11	7				25°C	350	425	500	
								75°C		495	580	
$V_{OL(Y)}$	Low-level output voltage at Y output	2	Same as for $V_{OH(Y)}$ above		−0.2 V	−0.5 V	0.5 V	0°C	−505	−450		mV
								25°C	−490	−410	−350	
								75°C		−290	−230	
$V_{OH(Z)}$	High-level output voltage at Z output	2	16, 14 / 14, 13 / 16, 13	4	−0.2 V	−0.5 V	0.5 V	0°C	315	390		mV
			16, 14, 13 / 9, 12, 13 / 9, 14, 11 / 16, 12, 11	5				25°C	350	425	500	
								75°C		495	580	
$V_{OL(Z)}$	Low-level output voltage at Z output	2	Same as for $V_{OH(Z)}$ above		0.2 V	−0.5 V	See Note 6	0°C		−385		mV
								25°C	−440	−365	−310	
								75°C		−325	−280	
$V_{OL(Z)}$	Low-level output voltage at Z output	2	Same as for $V_{OH(Z)}$ above		0.4 V	−0.5 V	See Note 6	0°C	−505	−455		mV
								25°C	−490	−425		
								75°C		−380	−315	
$V_{OH(Z)}$	High-level output voltage at Z output	2	16, 14 / 14, 13 / 16, 13	4	All inputs of all gates in parallel at −0.5 V			0°C				mV
								25°C			600	
								75°C			670	
			16, 14, 13 / 9, 12, 13 / 9, 14, 11 / 16, 12, 11	5				0°C				
								25°C			615	
								75°C			685	
$V_{OH(Y)}$	High-level output voltage at Y output	2	13	7	0.15 V	−0.5 V	0.5 V	0°C	290			mV
								25°C	325			
								75°C				
$V_{OL(Y)}$	Low-level output voltage at Y output	2	13	7	−0.15 V	−0.5 V	0.5 V	0°C				mV
								25°C			−335	
								75°C			−215	
I_{IH}	High-level input current (each input)	3	9 / 11 / 12		0.5 V	−0.5 V	−0.5 V	0°C			510	μA
								25°C			470	
								75°C			400	
			13 / 14 / 16					0°C			1020	μA
								25°C			940	
								75°C			800	
I_{IL}	Low-level input current (all inputs)	4	9, 11, 12, 13, 14, 16		All inputs of all gates in parallel at −3.2 V			0°C			−0.9	μA
								25°C			−1.2	
								75°C			−1.8	
I_{CC} or $-I_{EE}$	Supply current	5			All inputs of all gates in parallel at −0.5 V			25°C	30		45	mA
C_{in}	Input capacitance (see Note 8)							25°C		5		pF
z_{out}	Output impedance (see Note 9)							25°C		5		Ω

*V_{BB} (pin 15) = GND, V_{CC} (pins 3 and 6) = 1.32 V ± 1%, V_{EE} (pin 10) = −3.20 V ± 1%.
†Y = Σ or C_O; Z = $\overline{\Sigma}$ or $\overline{C_O}$.

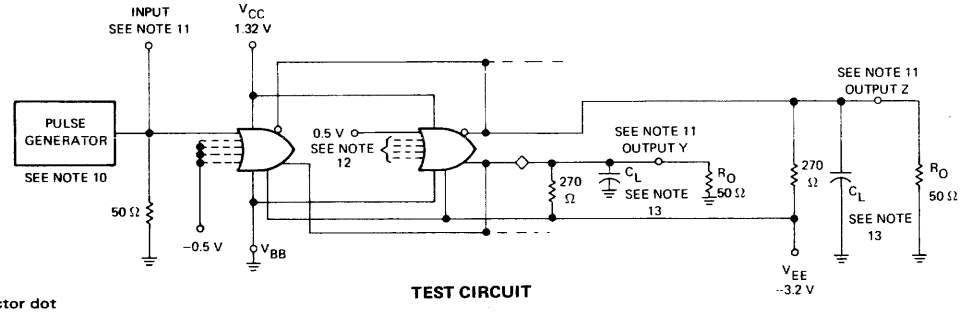
NOTES: 4. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.
5. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.
6. One input of each gate must be at V_I. Other inputs are biased to −0.5 V.
8. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. C_{in} = Q/V. When a terminal is an input to more than one gate, multiply the value given by the number of gates to which this terminal is an input.
9. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

operating characteristics at specified free-air temperature (see figure 1)

PARAMETER		C_L	T_A	ECL2515 EITHER OUTPUT			ECL2516 ANY OUTPUT			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation delay time, high-to-low level output and/or Propagation delay time low-to-high-level output	4 pF	0°C		2.6			2.6		ns
			25°C	1.5	2.6	4.1	1.5	2.6	4.1	
			75°C		2.6			2.6		
t_{PLH}		50 pF	0°C		3.5			3.5		ns
			25°C	2.4	3.5	4.8	2.4	3.5	4.8	
			75°C		3.5			3.5		
t_{THL}	Transition time, high-to-low-level output and/or Transition time, low-to-high-level output	4 pF	0°C		4.0			4.0		ns
			25°C	1.6	4.0	6.6	1.6	4.0	6.6	
			75°C		4.1			4.1		
t_{TLH}		50 pF	0°C		4.7			4.7		ns
			25°C	1.9	4.6	6.9	1.9	4.6	6.9	
			75°C		4.4			4.4		

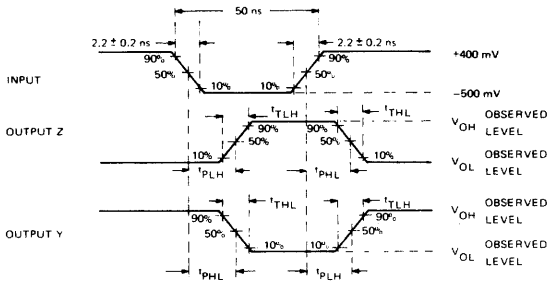
4

PARAMETER MEASUREMENT INFORMATION†



TEST CIRCUIT

◇—Collector dot



VOLTAGE WAVEFORMS

FIGURE 1–PROPAGATION DELAY AND TRANSITION TIMES

†For ECL2516: Y = Σ or C_O; Z = $\overline{\Sigma}$ or $\overline{C}_O$.

NOTES: 10. The generator has the following characteristics: Z_{out} = 50 Ω, PRR = 1 MHz.

11. The waveforms are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. Either a high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF, or a 50-Ω impedance system can be used. The 50-Ω resistors designated R_O are the oscilloscope input resistance in the 50-Ω system or discrete resistors with a high-impedance probe.

12. This test circuit shows only the principle of measuring propagation delay times and transition times; i.e., no internal connection of the input terminals is shown. See Table I for ECL2515 or Table II for ECL2516 for voltages to be applied to input terminals for each test.

13. C_L includes probe and fixture capacitance. A capacitance of 50 pF can be used to approximate an a-c fan-out of 10.

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PARAMETER MEASUREMENT INFORMATION

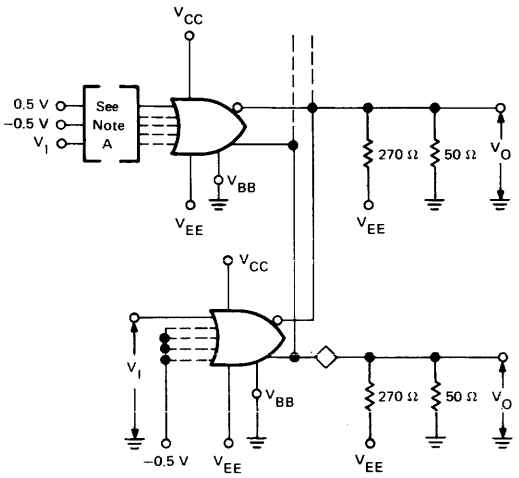
TEST TABLE I—ECL2515

INPUT TERMINAL CONDITIONS			OUTPUT UNDER TEST
PULSE GENERATOR	0.5 V	−0.5 V	
1	16	2, 8, 9, 11, 12, 13, 14	4, 5
2	1, 14	8, 9, 11, 12, 13, 16	4, 5
16		2, 8, 9, 11, 12, 13	
13	1, 2, 11	8, 9, 12, 14, 16	4, 5
14		8, 9, 12, 13, 16	
16		8, 9, 12, 13, 14	
11	1, 2, 9, 13	8, 12, 14, 16	4, 5
12		8, 11, 14, 16	
14		8, 11, 12, 16	
16		8, 11, 12, 14	
8	1, 2, 12, 13	9, 11, 14, 16	4, 5
9		8, 11, 14, 16	
11		8, 9, 14, 16	
14		8, 9, 11, 16	
16		8, 9, 11, 14	

TEST TABLE II—ECL2516

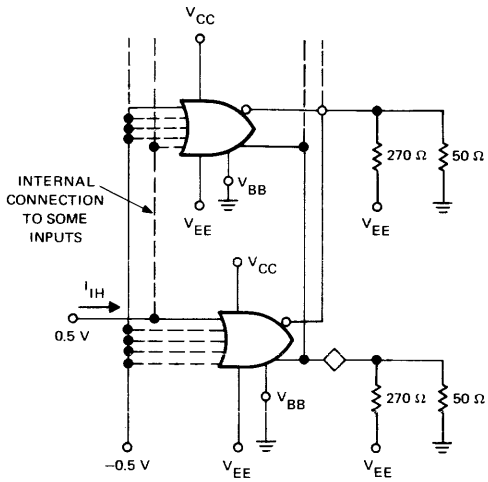
INPUT TERMINAL CONDITIONS			OUTPUT UNDER TEST
PULSE GENERATOR	0.5 V	−0.5 V	
16	11, 13	9, 12, 14	2, 4
14		9, 12, 16	
14	9, 16	11, 12, 13	2, 4
13		11, 12, 14	
16	12, 14	9, 11, 13	2, 4
13		9, 11, 16	
16	9, 11	12, 13, 14	7, 5
14		12, 13, 16	
13		12, 14, 16	
9	14, 16	11, 12, 13	7, 5
12		9, 11, 13	
13		9, 11, 12	
9	12, 13	11, 14, 16	7, 5
14		9, 11, 16	
11		9, 14, 16	
16	9, 14	11, 12, 13	7, 5
12		11, 13, 16	
11		12, 13, 16	

PARAMETER MEASUREMENT INFORMATION†



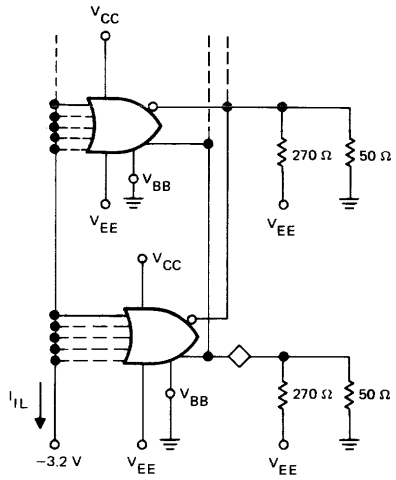
A. The particular input voltages for each module are shown in the electrical characteristics tables.
B. V_I is applied to each input separately except where Note 6 applies.
C. Each output is tested separately.

FIGURE 2–V_{OH} and V_{OL}



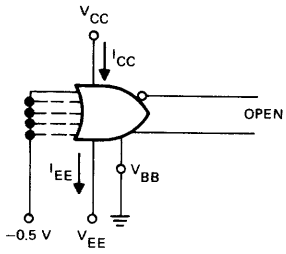
Each input is tested separately.

FIGURE 3–I_{IH}



All inputs of all gates are connected in parallel.

FIGURE 4–I_{IL}



A. All gates are tested simultaneously.
B. I_{CC} is the total current into all V_{CC} terminals.

FIGURE 5–I_{CC} or I_{EE}

◇—Collector dot

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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APPLICATION INFORMATION

ECL2515

The ECL2515 module is designed to provide the logic function for carry look-ahead in high-speed binary adders. In carry look-ahead, bit positions for binary numbers added together produce "generate" terms and "propagate" terms for the carry and sum logic equations.

The ECL2515 produces a "generate" term for 5 bits in one level of logic with a typical propagation delay of 3.0 nanoseconds with a fan-out of 4.

ECL2516

The ECL2516 is a full adder for two binary bits and carry-in that produces a sum and carry-out. The binary bits and their complements, along with carry-in and its complement, are required as inputs.

The sum and its complement and the carry-out and its complement are both produced in one level of logic with a typical propagation delay of 3.0 nanoseconds with a fan-out of 4.

general

Multiple V_{CC} terminals have been supplied to reduce crosstalk noise. All V_{CC} terminals should be connected even if all gates in a module are not used.

Applications of the arithmetic modules at other than data sheet conditions are covered in a separate ECL2500 series application document.

General loading for fan-out may be divided into two classes:

CLASS I **Short-Line or Cluster Loading.**
Loads which can be connected within two inches of any source can be treated as lumped capacitive loads which include the gate inputs and stub-line capacitances. Switching times can be interpolated accordingly. No two dotted outputs can be more than two inches apart for this case.

CLASS II **Long-Line or Distributive Loading.**
These loads must be treated as lumped loads along a transmission line and termination should be at the end of the transmission chain. No more than 20 pF of load is recommended per 4.5 inches of 50-ohm printed line (with dielectric constant of 4.5) in order that the reflection coefficient be no greater than 20%. If the loads are lumped loads of 20 pF, they must be 4.5 inches apart. If individual gates and **CLASS I** loads are distributed, they must not exceed the 20 pF per 4.5 inches of line.

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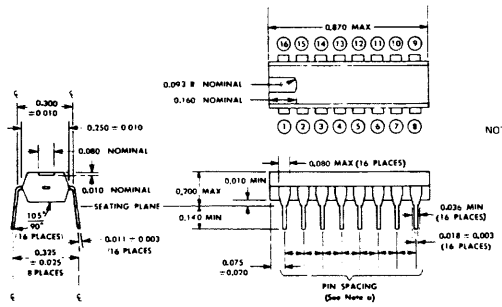
mechanical data

The circuit bars are mounted on a 16-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

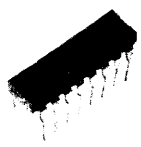
The plastic case is electrically nonconductive.

16-PIN PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



NOTES: a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within 0.010 of its true longitudinal position relative to pins 1 and 16.

b. All dimensions are in inches unless otherwise noted.



terminal designations

Pin assignments are shown in the table below and correspond to logic diagrams on page 4.
Outputs are denoted by Y and Z for ECL2515 and by Σ, $\overline{\Sigma}$, C_O, and $\overline{C}_O$ for ECL2516.
Inputs are denoted by A through I for ECL2515 and by A, B, C, $\overline{A}$, $\overline{B}$, and $\overline{C}$ for ECL2516.
Power is supplied via the V_{CC}, V_{EE}, and V_{BB} terminals.
V_{BB} is a reference voltage.
NC indicates no internal connection.

PIN ASSIGNMENTS

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ECL2515	A	B	V_{CC}	Y	Z	V_{CC}	NC	C	D	V_{EE}	E	F	G	H	V_{BB}	I
ECL2516	NC	C_O	V_{CC}	$\overline{C}_O$	$\overline{\Sigma}$	V_{CC}	Σ	NC	$\overline{A}$	V_{EE}	$\overline{C}$	$\overline{B}$	C	B	V_{BB}	A

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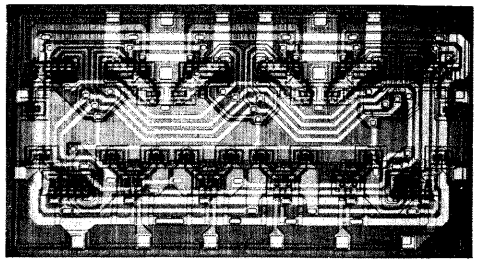
CIRCUIT TYPE ECL2517
EMITTER-COUPLED-LOGIC DECODER

ECL2500 SERIES EMITTER-COUPLED-LOGIC (ECL) DECODER MODULE FOR APPLICATION IN ULTRA-HIGH-SPEED DIGITAL SYSTEMS



description

The ECL2500 series is a compatible family of ECL functions with basic gate delays of 2 to 3 ns per stage. The family is specifically designed for operation from 0°C to 75°C.

The ECL2500 family includes:

- Basic Gate Modules
- **Multifunction Gate Modules**
- Bistable Modules
- Arithmetic Modules
- Interface Modules
- Memory Module

family features

- High speed. . .typical gate propagation delay time of 2.5 ns
- Complementary OR/NOR outputs with capability for wired-OR connections
- Designed for use with transmission lines to ensure maximum signal transmission without noise. Characterized for 50-ohm lines
- High noise immunity: ± 225 mV typical at 25°C

This data sheet covers the decoder module. Separate data sheets cover the balance of the ECL2500 modules.

ECL2500 series 3-bit-to-8-line decoder with enable

The ECL2500 series decoder module is summarized in the table below. The schematic diagram of this module is shown in Figure A.

SUMMARY OF DECODER MODULE

MODULE	GATES PER MODULE	INPUTS PER MODULE	OUTPUTS PER MODULE
ECL2517	12 (4 input, 8 output)	4 (3 bits plus enable)	8 (1 per output gate)

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CIRCUIT TYPE ECL2517
EMITTER-COUPLED-LOGIC DECODER

schematic

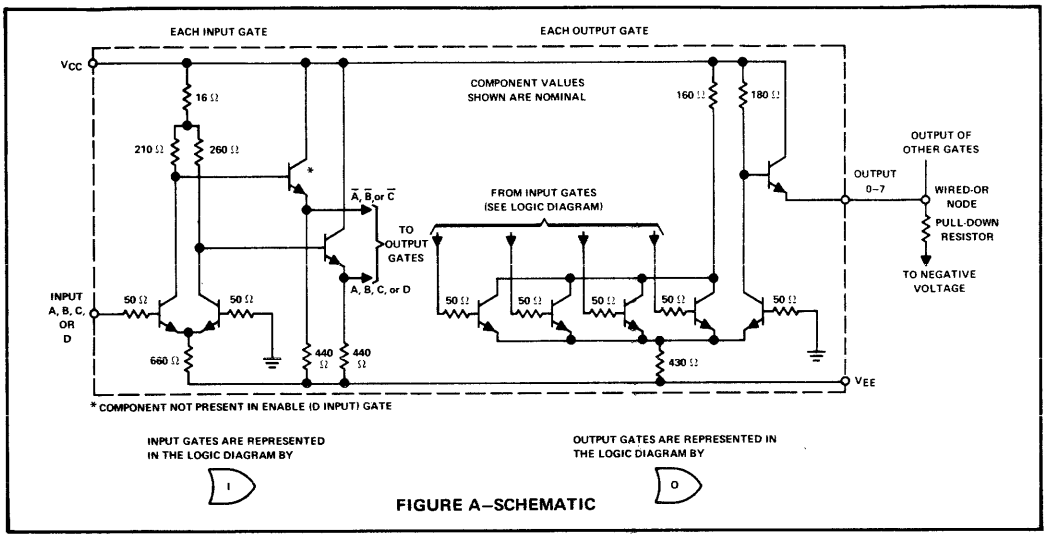

FIGURE A–SCHEMATIC

Emitter-follower outputs require external pull-down resistors. The wired-OR function can be obtained by connecting emitter-follower outputs of other gates to any of the outputs. Only one pull-down resistor is required for each wired-OR node.

absolute maximum ratings (see note 1)

Terminal voltages and currents	See table below
Storage temperature range	−40°C to 150°C
Temperature range with supply and bias voltage applied	−40°C to 100°C

TERMINAL VOLTAGE AND/OR CURRENT, T_A = 0°C TO 75°C (SEE NOTES 2 AND 3)

TERMINAL	REMARKS	VOLTAGE		CURRENT
		CONTINUOUS	20-μs SURGE	
V_{CC}		2 V	4.5 V	
V_{EE}		−4 V	−7 V	
Each Input	All other inputs open	−3.5 V	−4 V	
		2 V	2 V	
Any output	All inputs high			−40 mA

recommended operating conditions

Supply voltage V_{CC}	1.32 V ± 2%
Supply voltage V_{EE}	−3.2 V ± 2%
Reference voltage V_{BB}	0 V (GND)
Reverse bias on unused inputs	−1 V ± 0.5 V
Normalized d-c fan-out	0 to 35
Load on each output	characterized at 270 Ω to V_{EE}, 50 Ω to GND
Operating free-air temperature range	0°C to 75°C

NOTES: 1. Absolute maximum ratings are limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing.
2. Maximum terminal conditions must be considered as mutually exclusive.
3. All voltages are referenced to V_{BB}, which is at GND.

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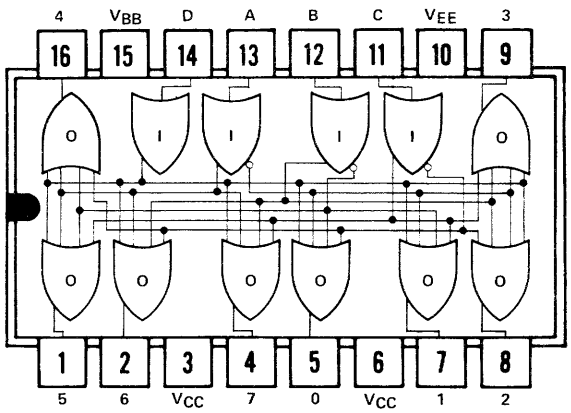
logic



OUTPUT LINE	POSITIVE LOGIC	NEGATIVE LOGIC
0	$\overline{A}+\overline{B}+\overline{C}+D$	$\overline{A}\overline{B}\overline{C}D$
1	$\overline{A}+\overline{B}+C+D$	$\overline{A}\overline{B}CD$
2	$\overline{A}+B+\overline{C}+D$	$\overline{A}B\overline{C}D$
3	$\overline{A}+B+C+D$	$\overline{A}BCD$
4	$A+\overline{B}+\overline{C}+D$	$A\overline{B}\overline{C}D$
5	$A+\overline{B}+C+D$	$A\overline{B}CD$
6	$A+B+\overline{C}+D$	$AB\overline{C}D$
7	$A+B+C+D$	$ABCD$

INPUT GATE

OUTPUT GATE

4

truth table (for this module, H = positive voltage, L = negative voltage, X = irrelevant)

INPUTS				OUTPUT LINES							
A	B	C	D	0	1	2	3	4	5	6	7
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	L
L	L	H	L	H	H	H	H	H	H	L	H
L	H	L	L	H	H	H	H	H	L	H	H
L	H	H	L	H	H	H	H	L	H	H	H
H	L	L	L	H	H	H	L	H	H	H	H
H	L	H	L	H	H	L	H	H	H	H	H
H	H	L	L	H	L	H	H	H	H	H	H
H	H	H	L	L	H	H	H	H	H	H	H

CIRCUIT TYPE ECL2517
EMITTER-COUPLED-LOGIC DECODER

electrical characteristics at specified free-air temperature*

PARAMETER		TEST FIGURE	INPUT CONDITIONS TERMINAL 13 $V_{I(A)}$	12 $V_{I(B)}$	11 $V_{I(C)}$	14 $V_{I(D)}$	OUTPUT TERMINAL	T_A	MIN (SEE NOTE 4)	TYP (SEE NOTE 4)	MAX (SEE NOTE 4)	UNIT
V_{IH}	High-level input voltage							0°C	150		720	mV
								25°C	150		720	
								75°C	150		720	
V_{IL}	Low-level input voltage							0°C	−1500		−150	mV
								25°C	−1500		−150	
								75°C	−1500		−150	
$V_{OH(0)}$	High-level output voltage at line 0	1	0.5 V	0.5 V	0.5 V	0.2 V	5	0°C	290	365		mV
								25°C	325	400	500	
								75°C		470	570	
$V_{OL(0)}$	Low-level output voltage at line 0	1	0.5 V	0.5 V	0.5 V	−0.2 V	5	0°C	−505	−445		mV
								25°C	−490	−425	−350	
								75°C		−385	−310	
$V_{OH(1)}$	High-level output voltage at line 1	1	0.5 V	−0.2 V	−0.5 V	−0.5 V	7	0°C	290	365		mV
								25°C	325	400	500	
								75°C		470	570	
$V_{OL(1)}$	Low-level output voltage at line 1	1	0.5 V	0.2 V	−0.5 V	−0.5 V	7	0°C	−505	−445		mV
								25°C	−490	−425	−350	
								75°C		−385	−310	
$V_{OH(2)}$	High-level output voltage at line 2	1	0.5 V	0.2 V	0.5 V	−0.5 V	8	0°C	290	365		mV
								25°C	325	400	500	
								75°C		470	570	
$V_{OL(2)}$	Low-level output voltage at line 2	1	0.5 V	−0.2 V	0.5 V	−0.5 V	8	0°C	−505	−445		mV
								25°C	−490	−425	−350	
								75°C		−385	−310	
$V_{OH(3)}$	High-level output voltage at line 3	1	−0.2 V	−0.5 V	−0.5 V	−0.5 V	9	0°C	290	365		mV
								25°C	325	400	500	
								75°C		470	570	
$V_{OL(3)}$	Low-level output voltage at line 3	1	0.2 V	−0.5 V	−0.5 V	−0.5 V	9	0°C	−505	−445		mV
								25°C	−490	−425	−350	
								75°C		−385	−310	
$V_{OH(4)}$	High-level output voltage at line 4	1	0.2 V	0.5 V	0.5 V	−0.5 V	16	0°C	290	365		mV
								25°C	325	400	500	
								75°C		470	570	
$V_{OL(4)}$	Low-level output voltage at line 4	1	−0.2 V	0.5 V	0.5 V	−0.5 V	16	0°C	−505	−445		mV
								25°C	−490	−425	−350	
								75°C		−385	−310	
$V_{OH(5)}$	High-level output voltage at line 5	1	−0.5 V	0.5 V	0.2 V	−0.5 V	1	0°C	290	365		mV
								25°C	325	400	500	
								75°C		470	570	
$V_{OL(5)}$	Low-level output voltage at line 5	1	−0.5 V	0.5 V	−0.2 V	−0.5 V	1	0°C	−505	−445		mV
								25°C	−490	−425	−350	
								75°C		−385	−310	
$V_{OH(6)}$	High-level output voltage at line 6	1	−0.5 V	−0.5 V	−0.2 V	−0.5 V	2	0°C	290	365		mV
								25°C	325	400	500	
								75°C		470	570	
$V_{OL(6)}$	Low-level output voltage at line 6	1	−0.5 V	−0.5 V	0.2 V	−0.5 V	2	0°C	−505	−445		mV
								25°C	−490	−425	−350	
								75°C		−385	−310	
V_{OH}	High-level output voltage at all lines	1	−0.5 V	−0.5 V	−0.5 V	0.15 V	1, 2, 4, 5, 7, 8, 9, 16	0°C	290	365		mV
								25°C	325	400	500	
								75°C		470	570	
$V_{OL(7)}$	Low-level output voltage at line 7	1	−0.5 V	−0.5 V	−0.5 V	−0.15 V	4	0°C	−505	−445		mV
								25°C	−490	−425	−350	
								75°C		−385	−310	
I_{IH}	High-level input current	2	Input under test at 0.5 V, other inputs at −0.5 V					0°C			165	μA
								25°C			150	
								75°C			125	
I_{IL}	Low-level input current (all inputs)	3	All inputs in parallel at −3.2 V					0°C			−0.5	μA
								25°C			−0.5	
								75°C			−0.5	
I_{CC} or $-I_{EE}$	Supply current	4	All inputs in parallel at −0.5 V					25°C	84		133	mA
C_{in}	Input capacitance (see Note 5)							25°C		5		pF
z_{out}	Output impedance (see Note 6)							25°C		5		Ω

*V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V ± 1%, V_{EE} (pin 10) = −3.20 V ± 1%.

NOTES: 4. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.

5. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. $C_{in} = Q/V$.

6. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

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operating characteristics at specified free-air temperature (see figure 5)

TERMINALS TO BE TESTED (SEE NOTE 7)		C_L	t_{PHL} and/or t_{PLH} PROPAGATION TIMES—ns						t_{THL} and/or t_{TLH} TRANSITION TIMES—ns					
			T_A = 0°C			T_A = 25°C			T_A = 75°C			T_A = 0°C			T_A = 25°C			T_A = 75°C		
INPUT	OUTPUT	pF	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
14	5	4		4.8		3	4.8	6.6		5.0			3.6		2.3	3.7	5.5		3.6	
14	7																			
14	8																			
14	9																			
14	16																			
14	1																			
14	2																			
14	4																			
14	5	50		5.9		3.9	5.8	7.7		5.8			4.5		2.5	4.3	6.5		4.2	
14	7																			
14	8																			
14	9																			
14	16																			
14	1																			
14	2																			
14	4																			

NOTE: 7. The eight combinations of voltages at input terminals A, B, and C shown in the table of Figure 5, are applied sequentially. With each combination of input voltages, the enable input, D, is pulsed from the high level to the low level to give a low-level output at the particular output line shown in the table. The input pulse is measured as it is applied with each combination of input voltages and a waveform measurement is made at the corresponding output.

GENERAL APPLICATION INFORMATION

Multiple V_{CC} terminals have been supplied to reduce crosstalk noise. All V_{CC} terminals should be connected.

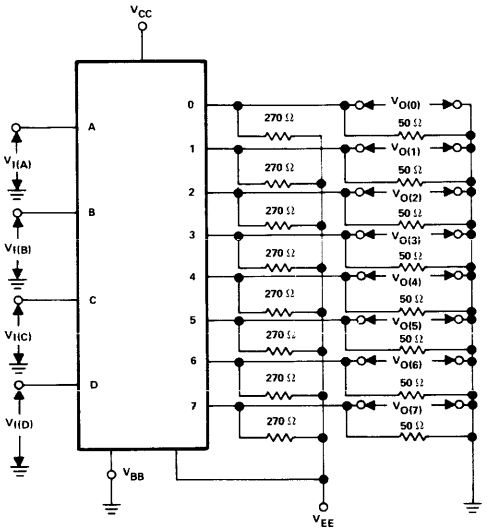
Applications of the ECL2517 decoder module at other than data sheet conditions are covered in a separate ECL2500 series application document.

General loading for fan-out may be divided into two classes:

CLASS I **Short-Line or Cluster Loading.**
Loads which can be connected within two inches of any source can be treated as lumped capacitive loads which include the gate inputs and stub-line capacitances. Switching times can be interpolated accordingly. No two dotted outputs can be more than two inches apart for this case.

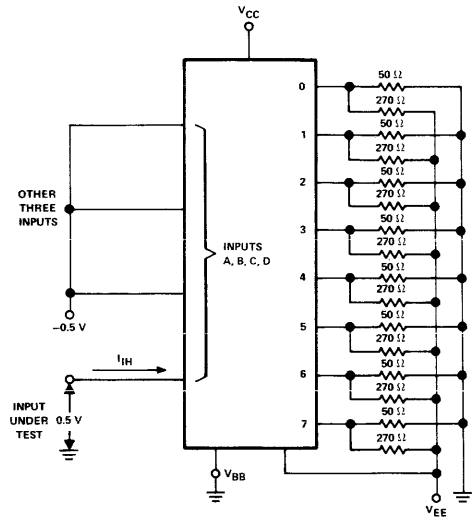
CLASS II **Long-Line or Distributive Loading.**
These loads must be treated as lumped loads along a transmission line and termination should be at the end of the transmission chain. No more than 20 pF of load is recommended per 4.5 inches of 50-ohm printed line (with dielectric constant of 4.5) in order that the reflection coefficient be no greater than 20%. If the loads are lumped loads of 20 pF, they must be 4.5 inches apart. If individual gates and **CLASS I** loads are distributed, they must not exceed the 20 pF per 4.5 inches of line.

PARAMETER MEASUREMENT INFORMATION†



V_I is applied to each input as specified in the electrical characteristics table.

FIGURE 1–V_{OH} AND V_{OL}



Each input is tested separately.

FIGURE 2–I_{IH}

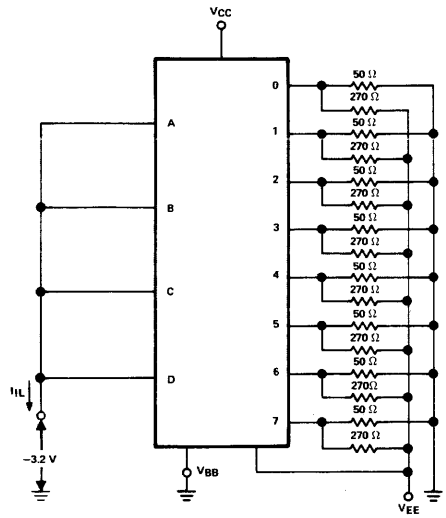
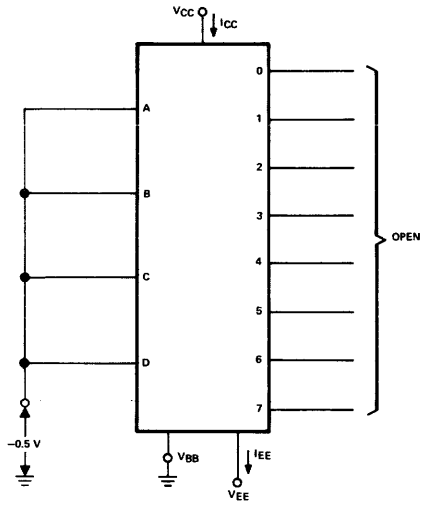


FIGURE 3–I_{IL}



I_{CC} is the total current into both V_{CC} terminals.

FIGURE 4–I_{CC} OR I_{EE}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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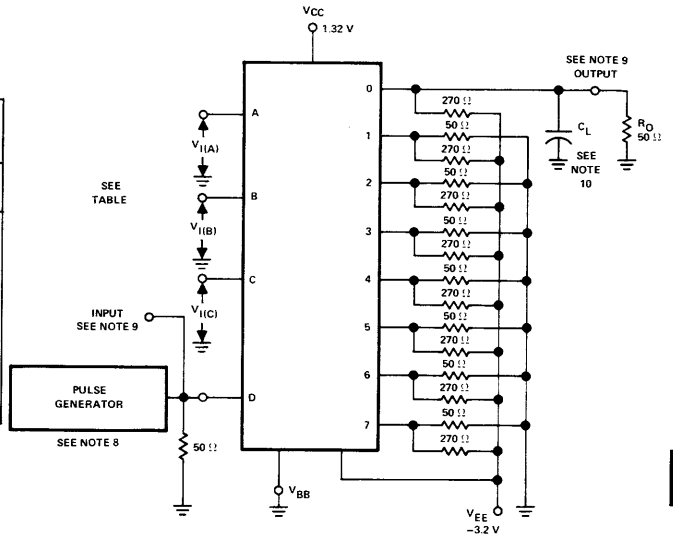
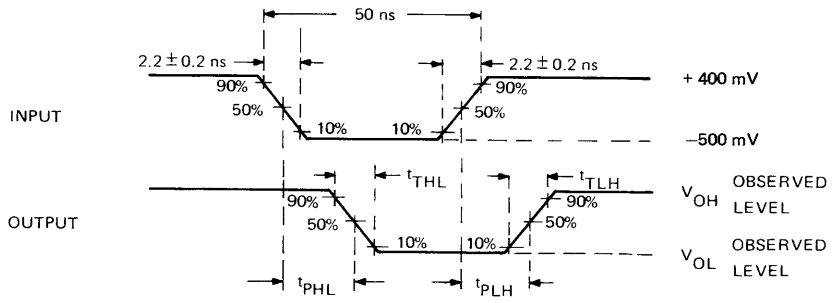
PARAMETER MEASUREMENT INFORMATION

INPUT TERMINAL			OUTPUT UNDER TEST	
13	12	11		
$V_{I(A)}$	$V_{I(B)}$	$V_{I(C)}$	LINE	TERMINAL
0.5 V	0.5 V	0.5 V	0	5
0.5 V	0.5 V	−0.5 V	1	7
0.5 V	−0.5 V	0.5 V	2	8
0.5 V	−0.5 V	−0.5 V	3	9
−0.5 V	0.5 V	0.5 V	4	16
−0.5 V	0.5 V	−0.5 V	5	1
−0.5 V	−0.5 V	0.5 V	6	2
−0.5 V	−0.5 V	−0.5 V	7	4

SEE NOTE 7



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 5—PROPAGATION DELAY AND TRANSITION TIMES

NOTES:
7. The eight combinations of voltages at input terminals A, B, and C shown in the table of Figure 5, are applied sequentially. With each combination of input voltages, the enable input, D, is pulsed from the high level to the low level to give a low-level output at the particular output line shown in the table. The input pulse is measured as it is applied with each combination of input voltages and a waveform measurement is made at the corresponding output.
8. The generator has the following characteristics: Z_{out} = 50 Ω, PRR = 1 MHz.
9. The waveforms are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. Either a high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF, or a 50-Ω impedance system can be used. The 50-Ω resistor designated R_O is the oscilloscope input resistance in the 50-Ω system or a discrete resistor with a high-impedance probe.
10. C_L includes probe and fixture capacitance. A capacitance of 50 pF can be used to approximate an a-c fan-out of 10.

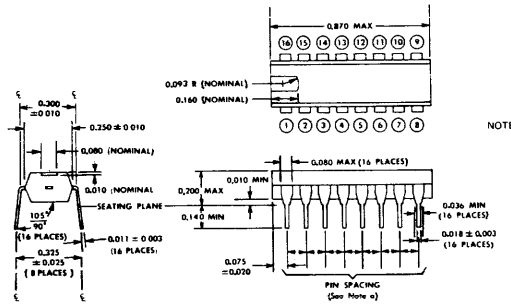
CIRCUIT TYPE ECL2517
EMITTER-COUPLED-LOGIC DECODER

mechanical data

The circuit bars are mounted on a 16-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

The plastic case is electrically nonconductive.

16-PIN PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



NOTES a. The true position pin spacing is 0.100 between center lines. Each pin centerline is located within 0.010 of its true longitudinal position relative to pins 1 and 16.

b. All dimensions are in inches unless otherwise noted.

terminal designations

Pin assignments are shown in the table below and correspond to the logic diagram on page 3.
Outputs are denoted by the numbers 0 through 7. Inputs are denoted by A, B, C, and D.
Power is supplied via the V_{CC}, V_{EE}, and V_{BB} terminals.
V_{BB} is a reference voltage.

PIN ASSIGNMENTS

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ECL2517	5	6	V_{CC}	7	0	V_{CC}	1	2	3	V_{EE}	C	B	A	D	V_{BB}	4

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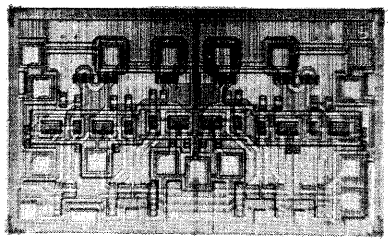
TYPES ECL2520 THRU ECL2523
DUAL PARALLEL EMITTER-FOLLOWER GATES

ECL2500 SERIES DUAL EMITTER-COUPLED-LOGIC (ECL) PARALLEL EMITTER-FOLLOWER GATES FOR APPLICATION IN ULTRA-HIGH-SPEED DIGITAL SYSTEMS

description

The ECL2500 series is a compatible family of ECL functions with basic gate delays of 2 to 3 ns per stage. The family is specifically designed for operation from 0°C to 75°C.



The ECL2500 family includes:

- Basic Gate Modules
- **Multifunction Gate Modules**
- Bistable Modules
- Arithmetic Modules
- Interface Modules
- Memory Modules

family features

- High speed . . . typical gate propagation delay time of 2.5 ns
- Complementary OR/NOR outputs with capability for wired-OR connections
- Designed for use with transmission lines to ensure maximum signal transmission without noise. Characterized for 50-ohm lines
- High noise immunity: ± 225 mV typical at 25°C

This data sheet covers the parallel emitter-follower modules.
Separate data sheets cover the balance of the ECL2500 modules.

ECL2500 series parallel emitter-follower gates

The four ECL2500 series modules that form the dual parallel emitter-follower gate group are shown in the table below. These modules contain various combinations of the ECL circuit shown in the schematic of Figure A and the logic diagrams of Figure B.

SUMMARY OF MODULES IN PARALLEL EMITTER-FOLLOWER GATE GROUP

MODULE	GATES PER MODULE	INPUTS PER GATE	POSITIVE LOGIC	OUTPUTS PER GATE	
				Y(OR)	Z(NOR)
ECL2520	2	2	OR/NOR	3	1
ECL2521	2	3	OR	3	
ECL2522	2	4	NOR		2
ECL2523	2	3	NOR		3

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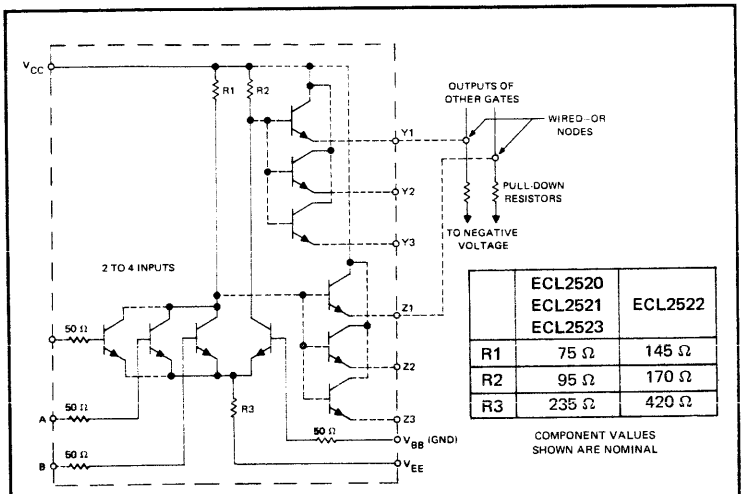
TYPES ECL2520 THRU ECL2523
DUAL PARALLEL EMITTER-FOLLOWER GATES

schematic



	ECL2520 ECL2521 ECL2523	ECL2522
R1	75 Ω	145 Ω
R2	95 Ω	170 Ω
R3	235 Ω	420 Ω

COMPONENT VALUES SHOWN ARE NOMINAL

FIGURE A—TYPICAL SCHEMATIC (EACH GATE)

logic

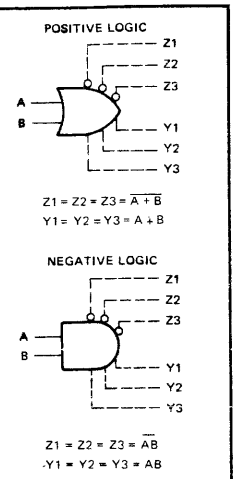


FIGURE B
TYPICAL LOGIC DIAGRAMS

4

Positive logic OR/NOR functions or negative logic AND/NAND functions are provided at the Y (OR) and Z (NOR) outputs, as shown.

Emitter-follower outputs require an external pull-down resistor. The wired-OR function can be obtained by connecting emitter-follower outputs of separate gates together. Only one pull-down resistor is required for each wire-OR node. Each output of a gate can be wire-OR connected independently of the other outputs of that gate.

absolute maximum ratings (see note 1)

Terminal voltages and currents . . . . . See table below
Storage temperature range . . . . . −40°C to 150°C
Temperature range with supply and bias voltages applied . . . . . −40°C to 100°C

TERMINAL VOLTAGE AND/OR CURRENT, T_A = 0°C TO 75°C (SEE NOTES 2 AND 3)

TERMINAL	REMARKS	VOLTAGE		CURRENT
		CONTINUOUS	20-μs SURGE	
V_{CC}		2 V	4.5 V	
V_{EE}		−4 V	−7 V	
Each Input	All other inputs open	−3.5 V	−4 V	
		2 V	2 V	
Output Y	All inputs high			−40 mA
Output Z	All inputs low			−40 mA

NOTES: 1. Absolute maximum ratings are limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing.
2. Maximum terminal conditions must be considered as mutually exclusive.
3. All voltages are referenced to V_{BB}, which is at GND.

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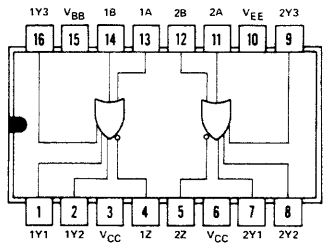
recommended operating conditions

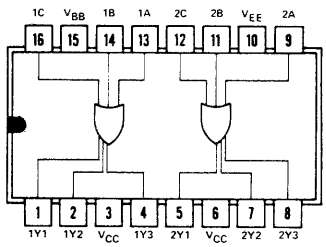
Supply voltage V_{CC}	1.32 V ± 2%
Supply voltage V_{EE}	−3.2 V ± 2%
Reference voltage V_{BB}	0 V (GND)
Reverse bias on unused inputs	−1 V ± 0.5 V
Normalized d-c fan-out	0 to 35
Load on each output	characterized at 270 Ω to V_{EE}, 50 Ω to GND
Operating free-air temperature range	0°C to 75°C

ECL2520



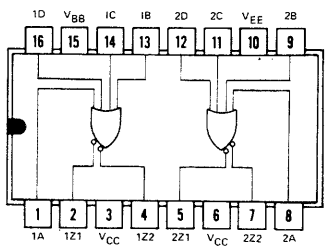
DUAL 2-INPUT OR/NOR GATE
(1 NOR, 3 OR OUTPUTS PER GATE)

ECL2521



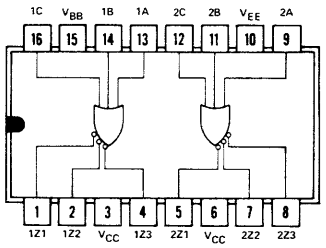
DUAL 3-INPUT OR GATE
(3 OR OUTPUTS PER GATE)

ECL2522



DUAL 4-INPUT NOR GATE
(2 NOR OUTPUTS PER GATE)

ECL2523



DUAL 3-INPUT NOR GATE
(3 NOR OUTPUTS PER GATE)

MODULE	POSITIVE LOGIC OUTPUT		NEGATIVE LOGIC OUTPUT	
	Y(OR)	Z(NOR)	Y (AND)	Z (NAND)
ECL2520	A+B	$\overline{A+B}$	AB	$\overline{AB}$
ECL2521	A+B+C		ABC	
ECL2522		$\overline{A+B+C+D}$		$\overline{ABCD}$
ECL2523		$\overline{A+B+C}$		$\overline{ABC}$

truth tables (for this series, H = positive voltage, L = negative voltage, X = irrelevant)

ECL2520

INPUTS		OUTPUTS			
A	B	Y1	Y2	Y3	Z
L	L	L	L	L	H
X	H	H	H	H	L
H	X	H	H	H	L
H	H	H	H	H	L

ECL2521

INPUTS			OUTPUTS		
A	B	C	Y1	Y2	Y3
L	L	L	L	L	L
H	X	X	H	H	H
X	H	X	H	H	H
X	X	H	H	H	H
H	H	H	H	H	H

ECL2522

INPUTS				OUTPUTS	
A	B	C	D	Z1	Z2
L	L	L	L	H	H
H	L	L	L	L	L
X	H	X	X	L	L
X	X	H	X	L	L
X	X	X	H	L	L
H	H	H	H	L	L

ECL2523

INPUTS			OUTPUTS		
A	B	C	Z1	Z2	Z3
L	L	L	H	H	H
H	X	X	L	L	L
X	H	X	L	L	L
X	X	H	L	L	L
H	H	H	L	L	L

electrical characteristics at specified free-air temperature

PARAMETER		TEST FIGURE	TEST CONDITIONS*		MODULE ECL2520	MODULE ECL2521	MODULE ECL2522	MODULE ECL2523	MIN (SEE NOTE 4)	TYP (SEE NOTE 4)	MAX (SEE NOTE 4)	UNIT
V_{IH}	High-level input voltage			0°C	•	•	•	•	150		720	mV
				25°C					150		720	
				75°C					150		720	
V_{IL}	Low-level input voltage			0°C	•	•	•	•	−1500		−150	mV
				25°C					−1500		−150	
				75°C					−1500		−150	
$V_{OH(Y)}$	High-level output voltage at OR output	2	V_I = 0.2 V	0°C	•	•			290	365		mV
				25°C					325	400	500	
				75°C						470	580	
$V_{OL(Y)}$	Low-level output voltage at OR output	2	V_I = −0.2 V	0°C	•	•			−505	−445		mV
				25°C					−490	−425	−350	
				75°C						−385	−310	
$V_{OH(Z)}$	High-level output voltage at NOR output	2	V_I = −0.2 V	0°C	•				340	415		mV
				25°C					375	450	525	
				75°C						520	605	
				0°C			•		280	355		mV
				25°C					315	390	500	
				75°C						460	580	
				0°C				•	290	365		mV
				25°C					325	400	500	
				75°C						470	580	
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	V_I = 0.2 V	0°C	•		•	•		−385		mV
				25°C					−420	−365	−310	
				75°C						−325	−280	
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	V_I = 0.4 V	0°C	•		•	•	−505	−455		mV
				25°C					−490	−425		
				75°C						−380	−315	
$V_{OH(Y)}$	High-level output voltage at OR output	2	V_I = 0.15 V	0°C	•	•			265			mV
				25°C					300			
				75°C								
$V_{OL(Y)}$	Low-level output voltage at OR output	2	V_I = −0.15 V	0°C	•	•					−325	mV
				25°C							−290	
				75°C								
$V_{OH(Z)}$	High-level output voltage at NOR output	2	V_I = −0.15 V	0°C			•		255			mV
				25°C					290			
				75°C								
				0°C				•	265			mV
				25°C					300			
				75°C								
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	V_I = 0.15 V	0°C			•	•			−290	mV
				25°C							−260	
				75°C								
I_{IH}	High-level input current	3	V_I = 0.5 V	0°C	•	•	•	•			510†	μA
				25°C							470†	
				75°C							400†	
I_{IL}	Low-level input current	4	V_I = −3.2 V	0°C	•	•	•	•			−0.5‡	μA
				25°C							−0.6‡	
				75°C							−0.8‡	
I_{CC} or $-I_{EE}$	Supply current	5	V_I = −0.5 V	25°C	•				15		27	mA
						•			15		27	
							•		8		15	
								•	15		27	
C_{in}	Input capacitance		See Note 5	25°C	•	•	•	•		6		pF
z_{out}	Output impedance		See Note 6	25°C	•	•	•	•		5		Ω

*V_{BB} = GND, V_{CC} = 1.32 V ± 1%, V_{EE} = −3.20 V ± 1%.
†These are worst-case values. See Supplementary Parameter Measurement Information for each gate.
‡These are worst-case values for eight inputs in parallel. See Supplementary Parameter Measurement Information for each gate.

NOTES: 4. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.
5. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. C_{in} = Q/V.
6. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

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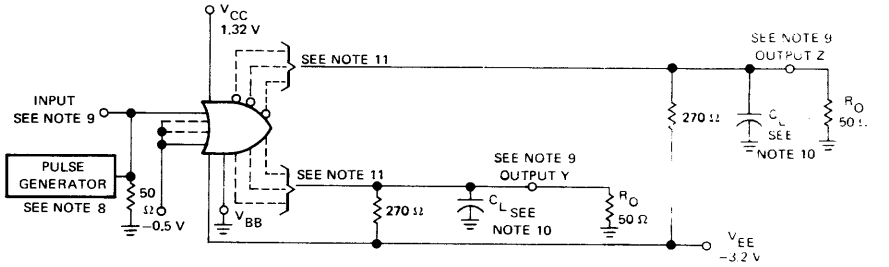
operating characteristics at specified free-air temperature (see figure 1)

PARAMETER		C_L	T_A	ECL2520						ECL2521			ECL2522 ECL2523			UNIT
				Y OUTPUTS			Z OUTPUTS			Y OUTPUTS			Z OUTPUTS			
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation delay time, high-to-low-level output and/or	4 pF	0°C		3.2			2.1			3.2			3.3		
			25°C	2.2	3.2	4.3	1.3	2.1	3.1	2.2	3.2	4.3	2.2	3.2	4.3	ns
			75°C		3.2			2.1			3.2			3.3		
t_{PLH}	Propagation delay time, low-to-high-level output	50 pF	0°C		4.3			3.1			4.3			4.5		
			25°C	3.2	4.3	5.6	2.1	3.1	4.2	3.2	4.3	5.6	3.2	4.3	5.6	ns
			75°C		4.3			3.1			4.3			4.5		
t_{THL}	Transition time high-to-low-level output and/or	4 pF	0°C		5.1			2.6			5.1			5.3		
			25°C	2.8	5.2	6.5	1.7	2.6	3.9	2.8	5.2	6.5	2.8	5.2	6.5	ns
			75°C		5.1			2.6			5.1			5.1		
t_{TLH}	Transition time, low-to-high-level output	50 pF	0°C		4.9						4.9			4.9		
			25°C	2.8	4.8	6.5	See Note 7			2.8	4.8	6.5	2.8	4.8	6.5	ns
			75°C		4.7						4.7			4.7		

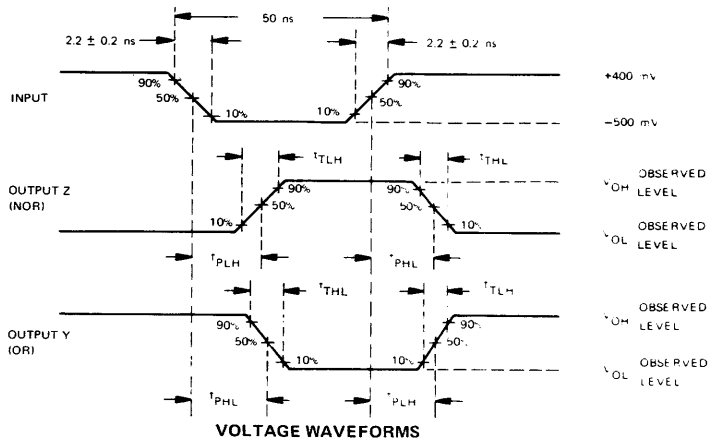
NOTE: 7. The transition times for the Z output at C_L = 50 pF are:
t_{THL} values are the same as for the Y output at 50 pF;
t_{TLH} values are the same as for the Z output at 4 pF.

4

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

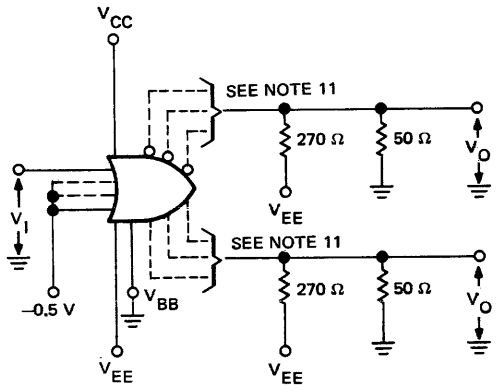


VOLTAGE WAVEFORMS

FIGURE 1–PROPAGATION DELAY AND TRANSITION TIMES

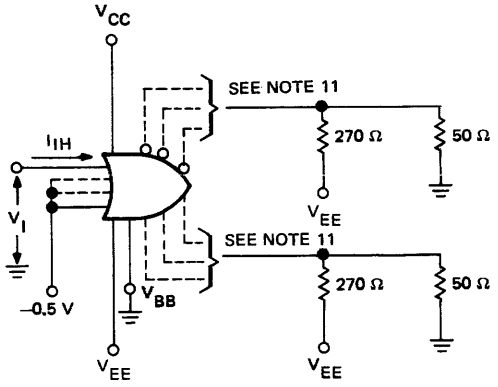
NOTES: 8. The generator has the following characteristics: Z_{out} = 50 Ω, PRR = 1 MHz.
9. The waveforms are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. Either a high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF, or a 50-Ω impedance system can be used. The 50-Ω resistors designated R_O are the oscilloscope input resistance in the 50-Ω system or discrete resistors with a high-impedance probe.
10. C_L includes probe and fixture capacitance. A capacitance of 50 pF can be used to approximate an a-c fan-out of 10.
11. Each of the output terminals is loaded as shown.

PARAMETER MEASUREMENT INFORMATION†



A. V_I is applied to each input separately.
B. Each output is tested separately.

FIGURE 2–V_{OH} and V_{OL}



Each input is tested separately.

FIGURE 3–I_{IH}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

NOTE: 11. Each of the output terminals is loaded as shown.

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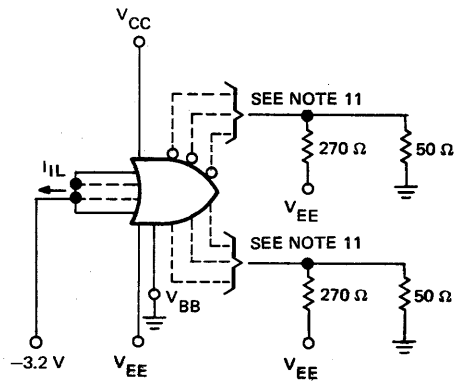
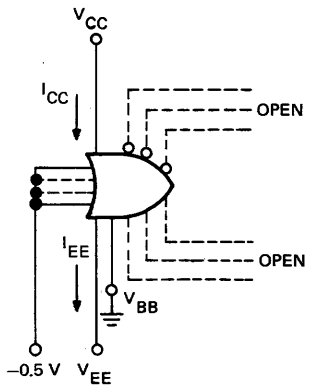
PARAMETER MEASUREMENT INFORMATION†



All inputs of both gates are connected in parallel.

FIGURE 4—I_{IL}



A. Both gates are tested simultaneously.
B. I_{CC} is the total current into both V_{CC} terminals.

FIGURE 5—I_{CC} or I_{EE}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.
NOTE: 11. Each of the output terminals is loaded as shown.

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 12)	TERMINALS TO BE TESTED (SEE NOTE 13)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y	OUTPUTS Z	INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATE(S)					
ECL2520 V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V											
$V_{OH(Y)}$	13, 14	1, 2, 16		2	0.2 V	−0.5 V	−0.5 V	0°C	290	365		mV
	11, 12	7, 8, 9						25°C	325	400	500	
								75°C		470	580	
$V_{OL(Y)}$	13, 14	1, 2, 16		2	−0.2 V	−0.5 V	−0.5 V	0°C	−505	−445		mV
	11, 12	7, 8, 9						25°C	−490	−425	−350	
								75°C		−385	−310	
$V_{OH(Z)}$	13, 14		4	2	−0.2 V	−0.5 V	−0.5 V	0°C	340	415		mV
	11, 12		5					25°C	375	450	525	
								75°C		520	605	
$V_{OL(Z)}$	13, 14		4	2	0.2 V	−0.5 V	−0.5 V	0°C		−385		mV
	11, 12		5					25°C	−440	−365	−310	
								75°C		−325	−280	
$V_{OL(Z)}$	13, 14		4	2	0.4 V	−0.5 V	−0.5 V	0°C	−505	−455		mV
	11, 12		5					25°C	−490	−425		
								75°C		−380	−315	
$V_{OH(Y)}$	11, 12	7		2	0.15 V	−0.5 V	−0.5 V	0°C	265			mV
								25°C	300			
								75°C				
$V_{OL(Y)}$	11, 12	7		2	−0.15 V	−0.5 V	−0.5 V	0°C				mV
								25°C			−325	
								75°C			−290	
I_{IH}	13, 14			3	0.5 V	−0.5 V	−0.5 V	0°C			510	μA
	11, 12							25°C			470	
								75°C			400	
I_{IL}	11, 12, 13, 14			4	All inputs of both gates in parallel at −3.2 V			0°C			−0.5	μA
								25°C			−0.5	
								75°C			−0.5	
ECL2521 V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V												
$V_{OH(Y)}$	9, 11, 12	5, 7, 8		2	0.2 V	−0.5 V	−0.5 V	0°C	290	365		mV
	13, 14, 16	1, 2, 4						25°C	325	400	500	
								75°C		470	580	
$V_{OL(Y)}$	9, 11, 12	5, 7, 8		2	−0.2 V	−0.5 V	−0.5 V	0°C	−505	−445		mV
	13, 14, 16	1, 2, 4						25°C	−490	−425	−350	
								75°C		−385	−310	
$V_{OH(Y)}$	13, 14, 16	1		2	0.15 V	−0.5 V	−0.5 V	0°C	265			mV
								25°C	300			
								75°C				
$V_{OL(Y)}$	13, 14, 16	1		2	−0.15 V	−0.5 V	−0.5 V	0°C				mV
								25°C			−325	
								75°C			−290	
I_{IH}	9, 11, 12			3	0.5 V	−0.5 V	−0.5 V	0°C			510	μA
	13, 14, 16							25°C			470	
								75°C			400	
I_{IL}	9, 11, 12, 13, 14, 16			4	All inputs of both gates in parallel at −3.2 V			0°C			−0.5	μA
								25°C			−0.5	
								75°C			−0.6	

NOTES: 12. See page 4 for defining term associated with each symbol.
13. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.

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SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 12)	TERMINALS TO BE TESTED (SEE NOTE 13)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATE(S)					
ECL2522 V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V											
$V_{OH(Z)}$	1, 13, 14, 16	2, 4	2	−0.2 V	−0.5 V	−0.5V	0°C	280	355		mV
	8, 9, 11, 12	5, 7					25°C	315	390	500	
							75°C		460	580	
$V_{OL(Z)}$	1, 13, 14, 16	2, 4	2	0.2 V	−0.5 V	−0.5 V	0°C		−385		mV
	8, 9, 11, 12	5, 7					25°C	−440	−365	−310	
							75°C		−325	−280	
$V_{OL(Z)}$	1, 13, 14, 16	2, 4	2	0.4 V	−0.5 V	−0.5 V	0°C	−505	−455		mV
	8, 9, 11, 12	5, 7					25°C	−490	−425		
							75°C		−380	−315	
$V_{OH(Z)}$	1, 13, 14, 16	2	2	−0.15 V	−0.5 V	−0.5 V	0°C	255			mV
							25°C	290			
							75°C				
$V_{OL(Z)}$	1, 13, 14, 16	2	2	0.15 V	−0.5 V	−0.5 V	0°C				mV
							25°C			−290	
							75°C			−260	
I_{IH}	1, 13, 14, 16		3	0.5 V	−0.5 V	−0.5 V	0°C			255	μA
	8, 9, 11, 12						25°C			235	
							75°C			200	
I_{IL}	1, 8, 9, 11, 12, 13, 14, 16		4	All inputs of both gates in parallel at −3.2 V			0°C			−0.5	μA
							25°C			−0.6	
							75°C			−0.8	
ECL2523 V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V											
$V_{OH(Z)}$	13, 14, 16	1, 2, 4	2	−0.2 V	−0.5 V	−0.5 V	0°C	290	365		mV
	9, 11, 12	5, 7, 8					25°C	325	400	500	
							75°C		470	580	
$V_{OL(Z)}$	13, 14, 16	1, 2, 4	2	0.2 V	−0.5 V	−0.5 V	0°C		−385		mV
	9, 11, 12	5, 7, 8					25°C	−440	−365	−310	
							75°C		−325	−280	
$V_{OL(Z)}$	9, 11, 12	5	2	0.4 V	−0.5 V	−0.5 V	0°C	−505	−455		mV
							25°C	−490	−425		
							75°C		−380	−315	
$V_{OH(Z)}$	9, 11, 12	5	2	−0.15 V	−0.5 V	−0.5 V	0°C	265			mV
							25°C	300			
							75°C				
$V_{OL(Z)}$	9, 11, 12	5	2	0.15 V	−0.5 V	−0.5 V	0°C				mV
							25°C			−290	
							75°C			−260	
I_{IH}	13, 14, 16		3	0.5 V	−0.5 V	−0.5 V	0°C			510	μA
	9, 11, 12						25°C			470	
							75°C			400	
I_{IL}	9, 11, 12, 13, 14, 16		4	All inputs of both gates in parallel at −3.2 V			0°C			−0.5	μA
							25°C			−0.5	
							75°C			−0.6	

NOTES: 12. See page 4 for defining term associated with each symbol.
13. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

operating characteristics at specified free-air temperature (see figure 1)

TERMINALS TO BE TESTED (SEE NOTES 14, 15, 16)				C_L	t_{PHL} and/or t_{PLH} PROPAGATION TIMES—ns									t_{THL} and/or t_{TLH} TRANSITION TIMES—ns								
					T_A = 0°C			T_A = 25°C			T_A = 75°C			T_A = 0°C			T_A = 25°C			T_A = 75°C		
INPUT	OUTPUT	INPUT	OUTPUT	pF	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
ECL2520																						
13, 14	1, 2, 16	11, 12	7, 8, 9	4		3.2		2.2	3.2	4.3		3.2			5.1		2.8	5.2	6.5		5.1	
				50		4.3		3.2	4.3	5.6		4.3			4.9		2.8	4.8	6.5		4.7	
13, 14	4	11, 12	5	4		2.1		1.3	2.1	3.1		2.1			2.6		1.7	2.6	3.9		2.6	
				50		3.1		2.1	3.1	4.2		3.1			2.6† 4.9‡		1.7† 2.8‡	2.6† 4.8‡	3.9† 6.5‡		2.6† 4.7‡	
ECL2521																						
13, 14, 16	1, 2, 4	9, 11, 12	5, 7, 8	4		3.2		2.2	3.2	4.3		3.2			5.1		2.8	5.2	6.5		5.1	
				50		4.3		3.2	4.3	5.6		4.3			4.9		2.8	4.8	6.5		4.7	
ECL2522																						
1, 13, 14, 16	2, 4	8, 9, 11, 12	5, 7	4		3.3		2.2	3.2	4.3		3.3			5.3		2.8	5.2	6.5		5.1	
				50		4.5		3.2	4.3	5.6		4.5			4.9		2.8	4.8	6.5		4.7	
ECL2523																						
13, 14, 16	1, 2, 4	9, 11, 12	5, 7, 8	4		3.3		2.2	3.2	4.3		3.3			5.3		2.8	5.2	6.5		5.1	
				50		4.5		3.2	4.3	5.6		4.5			4.9		2.8	4.8	6.5		4.7	

†For t_{TLH} only.
‡For t_{THL} only.

NOTES: 14. Each gate is tested separately.
15. The input pulse is measured as it is applied sequentially to each input of the gate under test, and a waveform measurement is made at each of the outputs of that gate. Times are as defined in Figure 1.
16. Bias voltages and loads for the gate under test are shown in Figure 1. The unused gate has inputs biased to −0.5 V, outputs under load, and power applied.

GENERAL APPLICATION INFORMATION

Multiple V_{CC} terminals have been supplied to reduce crosstalk noise. All V_{CC} terminals should be connected even if all gates in a module are not used.

Applications of the parallel emitter-follower gates at other than data sheet conditions are covered in a separate ECL2500 Series application document.

General loading for fan-out may be divided into two classes:

CLASS I Short-Line or Cluster Loading.

Loads which can be connected within two inches of any source can be treated as lumped capacitive loads which include the gate inputs and stub-line capacitances. Switching times can be interpolated accordingly. No two dotted outputs can be more than two inches apart for this case.

CLASS II Long-Line or Distributive Loading.

These loads must be treated as lumped loads along a transmission line and termination should be at the end of the transmission chain. No more than 20 pF of load is recommended per 4.5 inches of 50-ohm printed line (with dielectric constant of 4.5) in order that the reflection coefficient be no greater than 20%. If the loads are lumped loads of 20 pF, they must be 4.5 inches apart. If individual gates and **CLASS I** loads are distributed, they must not exceed the 20 pF per 4.5 inches of line.

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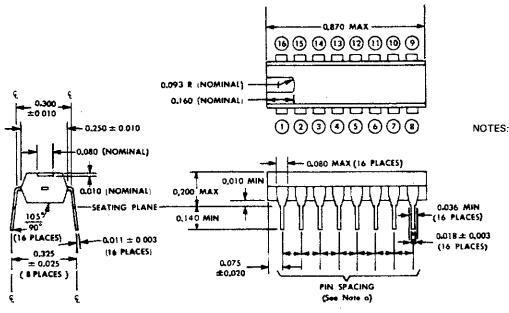
mechanical data

The circuit bars are mounted on a 16-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

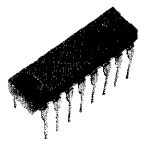
The plastic case is electrically nonconductive.

16-PIN PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



NOTES: a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within 0.010 of its true longitudinal position relative to pins 1 and 16.

b. All dimensions are in inches unless otherwise noted.



4

terminal designations

Pin assignments are shown in the table below and correspond to the logic diagrams on page 3.
Outputs are denoted by Y or Z. Inputs are denoted by A, B, C, etc.
Respective inputs and outputs are identified by a gate number preceding the pin symbol.
Power is supplied via the V_{CC}, V_{EE}, and V_{BB} terminals.
V_{BB} is a reference voltage.

PIN ASSIGNMENTS

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ECL2520	1Y1	1Y2	V_{CC}	1Z	2Z	V_{CC}	2Y1	2Y2	2Y3	V_{EE}	2A	2B	1A	1B	V_{BB}	1Y3
ECL2521	1Y1	1Y2	V_{CC}	1Y3	2Y1	V_{CC}	2Y2	2Y3	2A	V_{EE}	2B	2C	1A	1B	V_{BB}	1C
ECL2522	1A	1Z1	V_{CC}	1Z2	2Z1	V_{CC}	2Z2	2A	2B	V_{EE}	2C	2D	1B	1C	V_{BB}	1D
ECL2523	1Z1	1Z2	V_{CC}	1Z3	2Z1	V_{CC}	2Z2	2Z3	2A	V_{EE}	2B	2C	1A	1B	V_{BB}	1C

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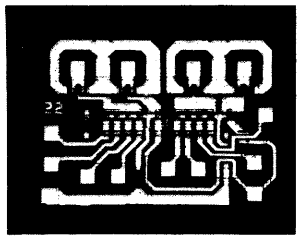
TYPES ECL2530, ECL2531
DUAL LINE RECEIVER AND DUAL LINE DRIVER

TYPES ECL2530, ECL2531
BULLETIN NO. DL-S 6911250, NOVEMBER 1969

ECL2500 SERIES EMITTER-COUPLED-LOGIC (ECL) DUAL LINE RECEIVER AND DUAL LINE DRIVER FOR APPLICATION IN ULTRA-HIGH-SPEED DIGITAL SYSTEMS

description



The ECL2500 series is a compatible family of ECL functions with basic gate delays of 2 to 3 ns per stage. The family is specifically designed for operation from 0°C to 75°C.

The ECL2500 family includes:

- Basic Gate Modules
- Multifunction Gate Modules
- Bistable Modules
- Arithmetic Modules
- **Interface Modules**
- Memory Module

family features

- High speed . . . typical gate propagation delay time of 2.5 ns
- Complementary OR/NOR outputs with capability for wired-OR connections
- Designed for use with transmission lines to ensure maximum signal transmission without noise. Characterized for 50-ohm lines
- High noise immunity: ± 225 mV typical at 25°C

This data sheet covers the line receiver and the line driver modules.
Separate data sheets cover the balance of the ECL2500 modules.

ECL2500 series line receiver and line driver

The ECL2500 series dual line receiver and dual line driver modules are shown in the tables below. These modules contain various combinations of the ECL circuit shown in the schematic of Figure A and the logic diagrams of Figure B.

SUMMARY OF LINE RECEIVER AND LINE DRIVER MODULES

MODULE	DIFFERENTIAL AMPLIFIERS PER MODULE	DIFFERENTIAL INPUTS PER AMPLIFIER	POSITIVE LOGIC	DIFFERENTIAL OUTPUTS PER AMPLIFIER	
				A	$\overline{A}$
ECL2530 Line Receiver	2	2	NOR/OR	1	1

MODULE	GATES PER MODULE	INPUTS PER GATE	POSITIVE LOGIC	OUTPUTS PER GATE	
				Y (OR)	Z (NOR)
ECL2531 Line Driver	2	2	NOR/OR	1	1

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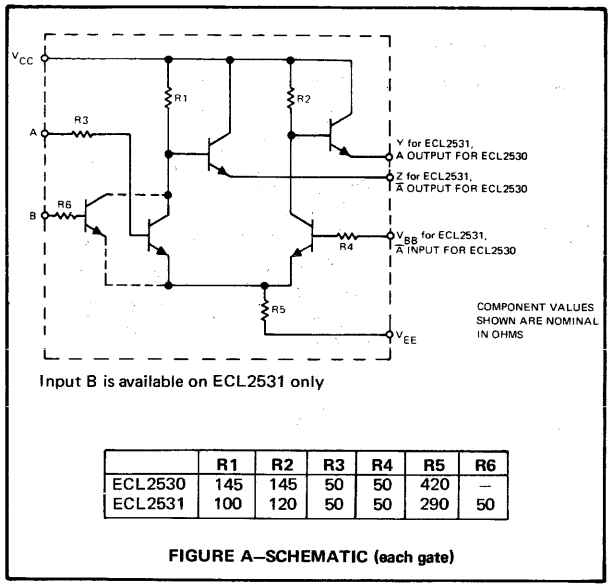
schematic



Input B is available on ECL2531 only

	R1	R2	R3	R4	R5	R6
ECL2530	145	145	50	50	420	—
ECL2531	100	120	50	50	290	50

FIGURE A—SCHEMATIC (each gate)

logic

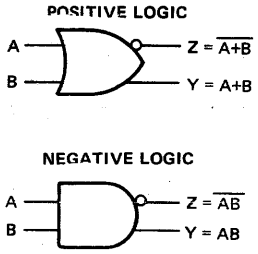


FIGURE B—ECL2531 LOGIC DIAGRAMS

Positive logic OR/NOR functions or negative logic AND/NAND functions are provided at the Y (OR) and Z (NOR) outputs, as shown. When the $\overline{A}$ input of the ECL2530 is connected to V_{BB}, the A and $\overline{A}$ outputs function as OR (Y) and NOR (Z) outputs respectively; and vice versa when the A input is connected to V_{BB}.

Emitter-follower outputs require an external pull-down resistor. The wired-OR function can be obtained by connecting emitter-follower outputs of separate gates together. Only one pull-down resistor is required for each wired-OR node.

absolute maximum ratings (see note 1)

Terminal voltages and currents . . . . . See table below
Storage temperature range . . . . . −40°C to 150°C
Temperature range with supply and bias voltage applied . . . . . −40°C to 100°C

TERMINAL VOLTAGE AND/OR CURRENT, T_A = 0°C to 75°C (SEE NOTES 2 AND 3)

TERMINAL	REMARKS	VOLTAGE		CURRENT	
		CONTINUOUS	20-μs SURGE	ECL2530	ECL2531
V_{CC}		2 V	4.5 V		
V_{EE}		−4 V	−7 V		
Each Input	Other input of ECL2530 at V_{BB},	−3.5 V	−4 V		
	all other inputs of ECL2531 open	2 V	2 V		
Output Y	All inputs (input A of ECL2530) high			−40 mA	−50 mA
Output Z	All inputs (input A of ECL2530) low			−40 mA	−50 mA

NOTES: 1. Absolute maximum ratings are limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing.
2. Maximum terminal conditions must be considered as mutually exclusive.
3. All voltages are referenced to V_{BB}, which is at GND.

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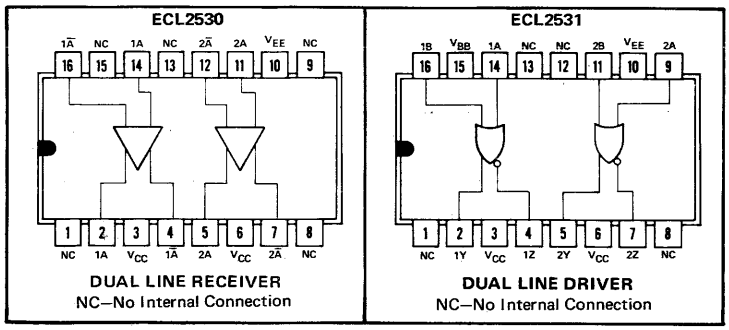
logic



ECL2530†

POSITIVE LOGIC		NEGATIVE LOGIC	
A (OR)	$\overline{A}$ (NOR)	A (AND)	$\overline{A}$ (NAND)
A	$\overline{A}$	A	$\overline{A}$

†With $\overline{A}$ input at V_{BB}

ECL2531

POSITIVE LOGIC		NEGATIVE LOGIC	
Y (OR)	Z (NOR)	Y (AND)	Z (NAND)
A + B	$\overline{A+B}$	AB	$\overline{AB}$

truth tables (for this series, H = positive voltage, L = negative voltage, X = irrelevant)

ECL2530			
INPUTS		OUTPUTS	
A	$\overline{A}$	A	$\overline{A}$
L	V_{BB}	L	H
H	V_{BB}	H	L
V_{BB}	L	H	L
V_{BB}	H	L	H

ECL2531			
INPUTS		OUTPUTS	
A	B	Y	Z
L	L	L	H
H	X	H	L
X	H	H	L
H	H	H	L

recommended operating conditions

Supply voltage V_{CC}	1.32 V ± 2%
Supply voltage V_{EE}	−3.2 V ± 2%
Reference voltage V_{BB}	0 V (GND)
Reverse bias on unused inputs	−1 V ± 0.5 V
Normalized d-c fan-out	0 to 35
Load on each output	ECL2530 characterized at 270 Ω to V_{EE}, 50 Ω to GND ECL2531 characterized at 135 Ω to V_{EE}, 25 Ω to GND
Operating free-air temperature range	0°C to 75°C

GENERAL APPLICATION INFORMATION

Multiple V_{CC} terminals have been supplied to reduce crosstalk noise. All V_{CC} terminals should be connected even if all gates in a module are not used.

Applications of the line receiver and the line driver modules at other than data sheet conditions are covered in a separate ECL2500 series application document.

General loading for fan-out may be divided into two classes:

CLASS I **Short-Line or Cluster Loading.**
Loads which can be connected within two inches of any source can be treated as lumped capacitive loads which include the gate inputs and stub-line capacitances. Switching times can be interpolated accordingly. No two dotted outputs can be more than two inches apart for this case.

CLASS II **Long-Line or Distributive Loading.**
These loads must be treated as lumped loads along a transmission line and termination should be at the end of the transmission chain. No more than 20 pF of load is recommended per 4.5 inches of 50-ohm printed line (with dielectric constant of 4.5) in order that the reflection coefficient be no greater than 20%. If the loads are lumped loads of 20 pF, they must be 4.5 inches apart. If individual gates and **CLASS I** loads are distributed, they must not exceed the 20 pF per 4.5 inches of line.

electrical characteristics at specified free-air temperature

	PARAMETER (SEE NOTE 4)	TEST FIGURE	TEST CONDITIONS*		ECL2530 MIN	ECL2530 TYP	ECL2530 MAX	ECL2531 MIN	ECL2531 TYP	ECL2531 MAX	UNIT
					(SEE NOTE 5)			(SEE NOTE 5)			
V_{IH}	High-level input voltage			0°C	150		720	150		720	mV
				25°C	150		720	150		720	
				75°C	150		720	150		720	
V_{IL}	Low-level input voltage			0°C	−1500		−150	−1500		−150	mV
				25°C	−1500		−150	−1500		−150	
				75°C	−1500		−150	−1500		−150	
$V_{OH(Y)}$	High-level output voltage at OR output	2	V_I = 0.2 V	0°C				290	365		mV
				25°C				325	400	475	
				75°C					470	560	
$V_{OL(Y)}$	Low-level output voltage at OR output	2	V_I = −0.2 V	0°C				−505	−450		mV
				25°C				−495	−430	−355	
				75°C					−390	−310	
$V_{OH(Z)}$	High-level output voltage at NOR output	2	V_I = −0.2 V	0°C	315	390		290	365		mV
				25°C	350	425	500	325	400	475	
				75°C		495	580		470	560	
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	V_I = 0.2 V	0°C		−385			−400		mV
				25°C	−440	−365	−310	−450	−380	−310	
				75°C		−325	−280		−340	−280	
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	V_I = 0.4 V	0°C	−505	−455		−505	−460		mV
				25°C	−490	−425		−495	−430		
				75°C		−380	−315		−385	−315	
$V_{OH(Y)}$	High-level output voltage at OR output	2	V_I = 0.15 V	0°C				270			mV
				25°C				305			
				75°C							
$V_{OL(Y)}$	Low-level output voltage at OR output	2	V_I = −0.15 V	0°C							mV
				25°C						−330	
				75°C						−290	
$V_{OH(Z)}$	High-level output voltage at NOR output	2	V_I = −0.15 V	0°C	290						mV
				25°C	325						
				75°C							
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	V_I = 0.15 V	0°C							mV
				25°C			−290				
				75°C			−260				
I_{IH}	High-level input current	3	V_I = 0.5 V	0°C			255			385	μA
				25°C			235			350	
				75°C			200			300	
I_{IL}	Low-level input current	4	V_I = −3.2 V	0°C			−0.5			−0.5	μA
				25°C			−0.5			−0.5	
				75°C			−0.5			−0.5	
I_{CC} or I_{EE}	Supply current	5	V_I = −0.5 V	25°C	8		15	12		22	mA
C_{in}	Input capacitance		See Note 6	25°C		5			5		pF
z_{out}	Output impedance		See Note 7	25°C		5			5		Ω

*V_{BB} = GND, V_{CC} = 1.32 V ± 1%, V_{EE} = −3.20 V ± 1%.

NOTES: 4. When the $\overline{A}$ input of the ECL2530 is connected to V_{BB}, the A and $\overline{A}$ outputs function as OR (Y) and NOR (Z) outputs respectively; and vice versa when the A input is connected to V_{BB}.

5. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e. g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.

6. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied and the input current waveform is integrated with respect to time to determine Q. C_{in} = Q/V.

7. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

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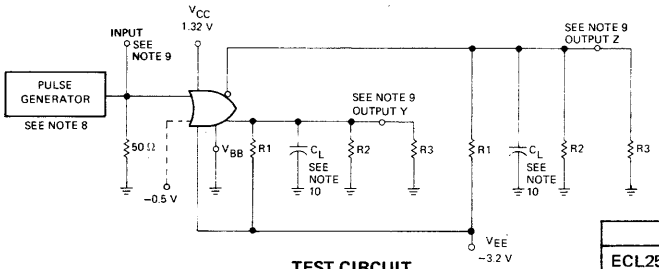
operating characteristics at specified free-air temperature (see figure 1)

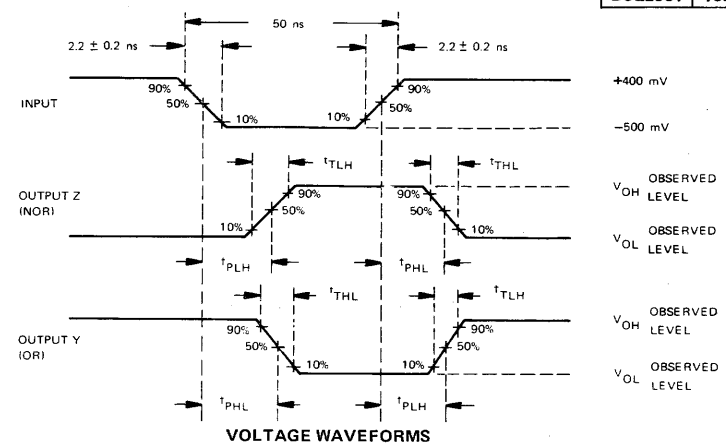
PARAMETER		C_L	T_A	ECL2530 ANY OUTPUT			ECL2531 ANY OUTPUT			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation delay time, high-to-low-level output and/or Propagation delay time, low-to-high-level output	4 pF	0°C	1.3	2.1	3	1.8	2.7	3.7	ns
			25°C		2.1			2.7		
			75°C		2.2			2.8		
t_{PLH}		50 pF	0°C	2.3	3.1	4.2	2.6	3.5	4.6	ns
			25°C		3.1			3.5		
			75°C		3.1			3.5		
t_{THL}	Transition time, high-to-low-level output and/or Transition time, low-to-high-level output	4 pF	0°C	1.6	2.7	4.2	2.5	3.8	5	ns
			25°C		2.9			3.8		
			75°C		2.8			3.9		
t_{TLH}		50 pF	0°C	2.2	3.6	6	2.5	3.7	5	ns
			25°C		3.6			3.7		
			75°C		3.6			3.7		

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

	R1	R2	R3
ECL2530	270 Ω	Not Used	50 Ω
ECL2531	135 Ω	50 Ω	50 Ω

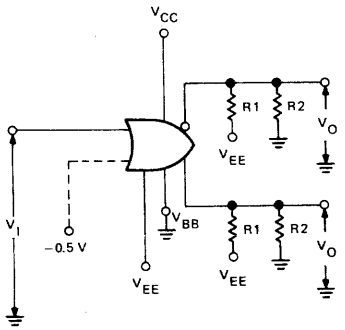


VOLTAGE WAVEFORMS

FIGURE 1–PROPAGATION DELAY AND TRANSITION TIMES

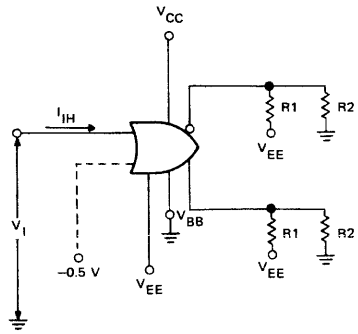
NOTES:
8. The generator has the following characteristics: Z_{out} = 50 Ω, PRR = 1 MHz.
9. The waveforms are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. Either a high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF or a 50-Ω impedance system can be used. Resistors R3 are the oscilloscope input resistance in the 50-Ω system or discrete resistors with a high-impedance probe.
10. C_L includes probe and fixture capacitance. A capacitance of 50 pF can be used to approximate an a-c fan-out of 10.

PARAMETER MEASUREMENT INFORMATION†



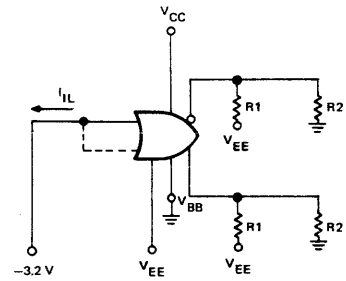
A. V_I is applied to each input separately.
B. Each output is tested separately.
C. For ECL2530, R1 = 270 Ω and R2 = 50 Ω.
For ECL2531, R1 = 135 Ω and R2 = 25 Ω.

FIGURE 2–V_{OH} AND V_{OL}



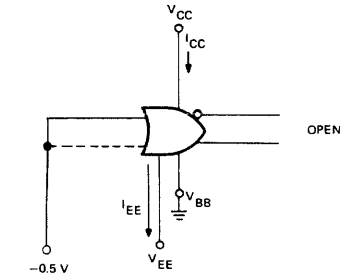
A. Each input is tested separately.
B. For ECL2530, R1 = 270 Ω and R2 = 50 Ω.
For ECL2531, R1 = 135 Ω and R2 = 25 Ω.

FIGURE 3–I_{IH}



A. All inputs of both gates are connected in parallel.
B. For ECL2530, R1 = 270 Ω and R2 = 50 Ω.
For ECL2531, R1 = 135 Ω and R2 = 25 Ω.

FIGURE 4–I_{IL}



A. Both gates are tested simultaneously.
B. I_{CC} is the total current into both V_{CC} terminals.

FIGURE 5–I_{CC} or I_{EE}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

terminal designations

Pin assignments are shown in the table below and correspond to the logic diagrams of page 3.
Outputs are denoted by A and $\overline{A}$ for ECL2530, Y and Z for ECL2531. Inputs are denoted by A, $\overline{A}$, or B.
Respective inputs and outputs are identified by a gate number preceding the pin symbol.
Power is supplied via the V_{CC}, V_{EE}, and V_{BB} terminals.
V_{BB} is a reference voltage.
NC indicates no internal connection.

PIN ASSIGNMENTS

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ECL2530	NC	1A (OUT)	V_{CC}	$1\overline{A}$ (OUT)	2A (OUT)	V_{CC}	$2\overline{A}$ (OUT)	NC	NC	V_{EE}	2A (IN)	$2\overline{A}$ (IN)	NC	1A (IN)	NC	$1\overline{A}$ (IN)
ECL2531	NC	1Y	V_{CC}	1Z	2Y	V_{CC}	2Z	NC	2A	V_{EE}	2B	NC	NC	1A	V_{BB}	1B

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SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTES 4 AND 11)	TERMINALS TO BE TESTED (SEE NOTE 12)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATE(S)		(SEE NOTE 5)			
ECL2530 V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V											
$V_{OH(Z)}$	14	4	2	−0.2 V	GND	OPEN	0°C	315	390		mV
	16	2					25°C	350	425	500	
	11	7					75°C		495	580	
	12	5									
$V_{OL(Z)}$	14	4	2	0.2 V	GND	OPEN	0°C		−385		mV
	16	2					25°C	−440	−365	−310	
	11	7					75°C		−325	−280	
	12	5									
$V_{OL(Z)}$	14	4	2	0.4 V	GND	OPEN	0°C	−505	−455		mV
	16	2					25°C	−490	−425		
	11	7					75°C		−380	−315	
	12	5									
$V_{OH(Z)}$	11	7	2	−0.15 V	GND	OPEN	0°C	290			mV
							25°C	325			
							75°C				
$V_{OL(Z)}$	11	7	2	0.15 V	GND	OPEN	0°C				mV
							25°C			−290	
							75°C			−260	
I_{IH}	14		3	0.5 V	GND	OPEN	0°C			255	μA
	16						25°C			235	
	11						75°C			200	
	12										
I_{IL}	11, 12, 14, 16		4	All inputs of both gates in parallel at −3.2 V			0°C			−0.5	μA
							25°C			−0.5	
							75°C			−0.5	
ECL2531 V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V											
$V_{OH(Y)}$	14, 16	2	2	0.2 V	−0.5 V	−0.5 V	0°C	290	365		mV
	9, 11	5					25°C	325	400	475	
							75°C		470	560	
$V_{OL(Y)}$	14, 16	2	2	−0.2 V	−0.5 V	−0.5 V	0°C	−505	−450		mV
	9, 11	5					25°C	−495	−430	−355	
							75°C		−390	−310	
$V_{OH(Z)}$	14, 16	4	2	−0.2 V	−0.5 V	−0.5 V	0°C	290	365		mV
	9, 11	7					25°C	325	400	475	
							75°C		470	560	
$V_{OL(Z)}$	14, 16	4	2	0.2 V	−0.5 V	−0.5 V	0°C		−400		mV
	9, 11	7					25°C	−450	−380	−310	
							75°C		−340	−280	
$V_{OL(Z)}$	14, 16	4	2	0.4 V	−0.5 V	−0.5 V	0°C	−505	−460		mV
	9, 11	7					25°C	−495	−430		
							75°C		−385	−315	
$V_{OH(Y)}$	9	5	2	0.15 V	−0.5 V	−0.5 V	0°C	270			mV
							25°C	305			
							75°C				
$V_{OL(Y)}$	9	5	2	−0.15 V	−0.5 V	−0.5 V	0°C				mV
							25°C			−330	
							75°C			−290	
I_{IH}	14, 16		3	0.5 V	−0.5 V	−0.5 V	0°C			385	μA
	9, 11						25°C			350	
							75°C			300	
I_{IL}	9, 11, 14, 16		4	All inputs of both gates in parallel at −3.2 V			0°C			−0.5	μA
							25°C			−0.5	
							75°C			−0.5	

NOTES: 4. When the $\overline{A}$ input of the ECL2530 is connected to V_{BB}, the A and $\overline{A}$ outputs function as OR (Y) and NOR (Z) outputs respectively; and vice versa when the A input is connected to V_{BB}.

5. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.

11. See page 4 for defining term associated with each symbol.

12. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

operating characteristics at specified free-air temperature (see figure 1)

TERMINALS TO BE TESTED (SEE NOTES 13, 14, 15)				C_L	t_{PHL} and/or t_{PLH} PROPAGATION TIMES—ns									t_{THL} and/or t_{TLH} TRANSITION TIMES—ns								
					T_A = 0°C			T_A = 25°C			T_A = 75°C			T_A = 0°C			T_A = 25°C			T_A = 75°C		
INPUT	OUTPUT	INPUT	OUTPUT	pF	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
ECL2530 (See Note 16)																						
14	2	16	4	4		2.1		1.3	2.1	3		2.2			2.7		1.6	2.9	4.2		2.8	
	4		2	50		3.1		2.3	3.1	4.2		3.1			3.6		2.2	3.6	6		3.6	
11	5	12	7	4		2.1		1.3	2.1	3		2.2			2.7		1.6	2.9	4.2		2.8	
	7		5	50		3.1		2.3	3.1	4.2		3.1			3.6		2.2	3.6	6		3.6	
ECL2531																						
14, 16	2, 4	9, 11	5, 7	4		2.7		1.8	2.7	3.7		2.8			3.8		2.5	3.8	5		3.9	
				50		3.5		2.6	3.5	4.6		3.5			3.7		2.5	3.7	5		3.7	

4

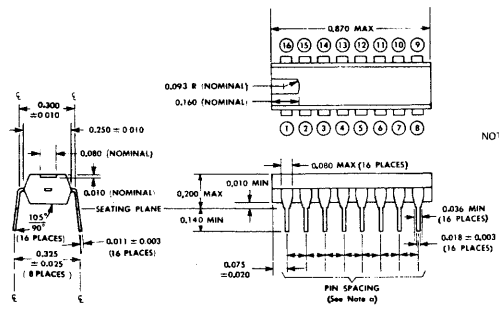
NOTES: 13. Each gate is tested separately.
14. The input pulse is measured as it is applied sequentially to each input of the gate under test and a waveform measurement is made at each of the outputs of that gate. Times are as defined in Figure 1.
15. Bias voltages and loads for the gate under test are shown in Figure 1. The unused gate has inputs biased to −0.5 V, outputs under load, and power applied.
16. When an input pulse is applied to pin 11, pin 12 is at GND, and vice versa. The same relationship holds true between pins 14 and 16.

mechanical data

The circuit bars are mounted on a 16-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

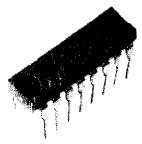
The plastic case is electrically nonconductive.

16-PIN PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



NOTES: a. The true position pin spacing is 0.100 between centerlines. Each pin centerline is located within 0.010 of its true longitudinal position relative to pins 1 and 16.

b. All dimensions are in inches unless otherwise noted.



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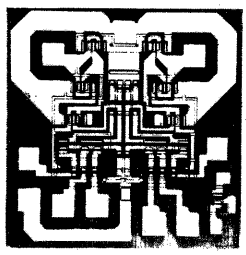
TYPES ECL2536, ECL2537
BULLETIN NO. DL-S 6911286, DECEMBER 1969

ECL2500 SERIES EMITTER-COUPLED-LOGIC (ECL) LEVEL CONVERTERS FOR APPLICATION IN ULTRA-HIGH-SPEED DIGITAL SYSTEMS



description

The ECL2500 series is a compatible family of ECL functions with basic gate delays of 2 to 3 ns per stage. The family is specifically designed for operation from 0°C to 75°C.

The ECL2500 family includes:

- Basic Gate Modules
- Multifunction Gate Modules
- Bistable Modules
- Arithmetic Modules
- **Interface Modules**
- Memory Module

family features

- High speed . . . typical gate propagation delay time of 2.5 ns
- Complementary OR/NOR outputs with capability for wired-OR connections
- Designed for use with transmission lines to ensure maximum signal transmission without noise. Characterized for 50-ohm lines
- High noise immunity: ± 225 mV typical at 25°C

This data sheet covers the ECL-to-HLL and HLL-to-ECL converter modules.
Separate data sheets cover the balance of the ECL2500 modules.

ECL2500 series ECL-to-HLL and HLL-to-ECL converters

The ECL2536 contains two high-level-logic-to-emitter-coupled-logic converters each having an HLL input (B*) and an ECL input (A). Each converter has complementary ECL outputs. The ECL input (A) is provided to be used as an INHIBIT/ENABLE control. When input A is low, the converter is enabled and the output state is determined by input B*. When input A is high, output Y is high and output Z is low regardless of the state of input B*.

The ECL2537 contains two emitter-coupled-logic-to-high-level-logic converters. Each converter has two ECL inputs and complementary HLL outputs.

The ECL2536 and ECL2537 are summarized in the table below, shown schematically in Figure A, and shown logically in Figure B.

SUMMARY OF HLL-TO-ECL AND ECL-TO-HLL CONVERTERS

MODULE	GATES PER MODULE	INPUTS PER GATE	POSITIVE LOGIC	OUTPUTS PER GATE	
				Y (OR)	Z (NOR)
ECL2536 DUAL HLL-TO-ECL CONVERTER	2	1 HLL input 1 ECL inhibit input	OR/NOR	1	1
ECL2537 DUAL ECL-TO-HLL CONVERTER	2	2	OR/NOR	1	1

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TYPES ECL2536, ECL2537
HLL-TO-ECL AND ECL-TO-HLL CONVERTERS

schematic

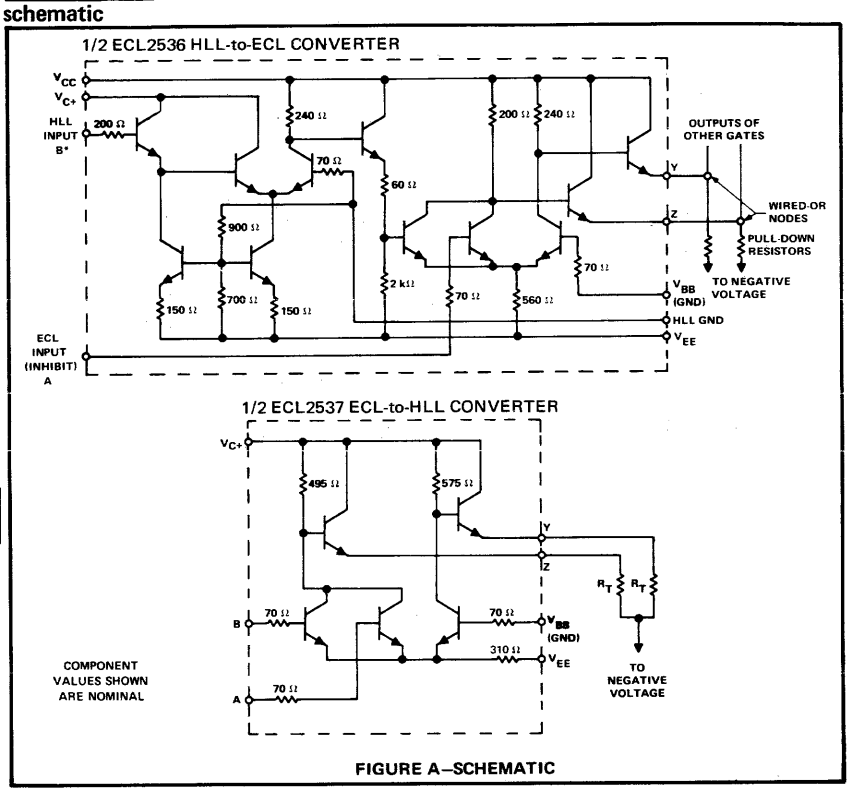


FIGURE A—SCHEMATIC

logic

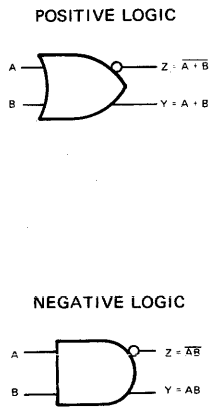
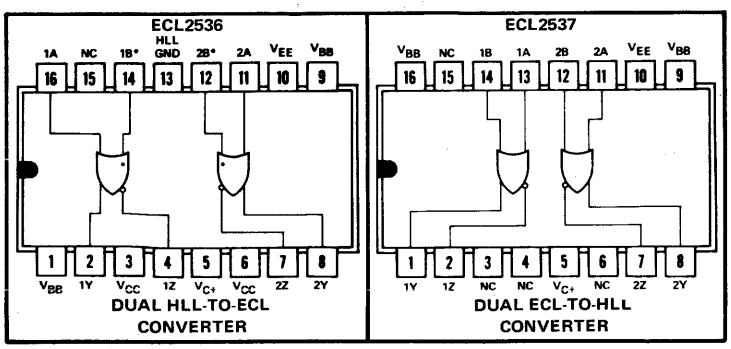


FIGURE B
LOGIC DIAGRAMS

Positive logic OR/NOR functions or negative logic AND/NAND functions are provided at the Y (OR) and Z (NOR) outputs, as shown.

Emitter-follower outputs require an external pull-down resistor. For ECL2536 only, the wired-OR function can be obtained by connecting emitter-follower outputs of separate gates together. Only one pull-down resistor is required for each wired-OR node. ECL2537 outputs require pull-down resistors (R_T in schematic above) to sink the low-level input current of the driven HLL inputs. ECL2537 cannot have wired-OR connections.

logic



NC—No internal connection

MODULE	POSITIVE LOGIC		NEGATIVE LOGIC	
	Y (OR)	Z (NOR)	Y (AND)	Z (NAND)
ECL2536	A+B*	$\overline{A+B}$*	AB*	$\overline{AB}$*
ECL2537	A+B	$\overline{A+B}$	AB	$\overline{AB}$

B* is the HLL input of the ECL2536.

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truth tables

(For HLL inputs, H = high-level positive voltage, L = low-level positive voltage. For ECL inputs, H = positive voltage, L = negative voltage)

ECL2536

INPUTS		OUTPUTS	
A	B*	Y (OR)	Z (NOR)
L	L	L	H
L	H	H	L
H	L	H	L
H	H	H	L

B* is the HLL input of the ECL2536.

ECL2537

INPUTS		OUTPUTS	
A	B	Y (OR)	Z (NOR)
L	L	L	H
L	H	H	L
H	L	H	L
H	H	H	L

absolute maximum ratings (see note 1)

Terminal voltages and currents . . . . . See table below
Storage temperature range . . . . . −40°C to 150°C
Temperature range with supply and bias voltages applied . . . . . −40°C to 100°C

4

TERMINAL VOLTAGE AND/OR CURRENT, T_A = 0°C to 75°C (SEE NOTES 2 AND 3)

TERMINAL	REMARKS	VOLTAGE		CURRENT
		CONTINUOUS	20-μs SURGE	
V_{C+}		6 V	7 V	
V_{CC} (ECL2536)		2 V	4.5 V	
V_{EE}		−4 V	−7 V	
Each ECL input (ECL2536 and ECL2537)	All other inputs open	−3.5 V	−4 V	
		2 V	2 V	
Each HLL input (ECL2536 only)		−1.25 V	−1.5 V	
		4.5 V	5 V	
Output Y (ECL2536)	A input low, B* input high			−40 mA
Output Y (ECL2537)	All inputs high			−40 mA
Output Z	All inputs low			−40 mA

recommended operating conditions

Supply voltage V_{C+} . . . . . 4.8 V ± 1%
Supply voltage V_{CC} (ECL2536 only) . . . . . 1.32 V ± 2%
Supply voltage V_{EE} . . . . . −3.2 V ± 2%
Reference voltage V_{BB} . . . . . 0 V (GND)
Reverse bias on unused ECL inputs . . . . . −1 V ± 0.5 V
Low-level bias on unused HLL inputs . . . . . 0 V (GND)
Normalized d-c fan-out: ECL2536 . . . . . 0 to 35
ECL2537 . . . . . 0 to 8 loads, each requiring 1.6 mA
Load on each output: ECL2536 . . . . . characterized at 270 Ω to V_{EE}, 50 Ω to GND
ECL2537 . . . . . characterized at 300 Ω to V_{EE}
Operating free-air temperature range . . . . . 0°C to 75°C

NOTES: 1. Absolute maximum ratings are limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing.
2. Maximum terminal conditions must be considered as mutually exclusive.
3. All voltages are referenced to V_{BB}, which is at GND.

ECL2536 electrical characteristics using HLL inputs

PARAMETER		TEST CONDITIONS*						MIN	TYP	MAX	UNIT
		TEST FIGURE	TERMINALS (SEE NOTE 4)		INPUT CONDITIONS		T_A	(SEE NOTE 5)			
			INPUTS	OUTPUTS Y	OUTPUTS Z	INPUT UNDER TEST, V_I	HLL INPUT OF OTHER GATE					
V_{IH}	High-level input voltage		14					0°C	1.05		4.5	V
			12					25°C	1.05		4.5	
								75°C	1.05		4.5	
V_{IL}	Low-level input voltage		14					0°C	−1		0.65	V
			12					25°C	−1		0.65	
								75°C	−1		0.65	
$V_{OH(Y)}$	High-level output voltage at OR output	2	14	2		1.2 V	0 V	0°C	315	410		mV
			12	8				25°C	350	450	525	
								75°C		520	600	
$V_{OL(Y)}$	Low-level output voltage at OR output	2	14	2		0.5 V	0 V	0°C	−505	−470		mV
			12	8				25°C	−505	−450	−350	
								75°C		−410	−310	
$V_{OH(Z)}$	High-level output voltage at NOR output	2	14		4	0.5 V	0 V	0°C	315	410		mV
			12		7			25°C	350	450	525	
								75°C		520	600	
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	14		4	1.2 V	0 V	0°C	−505	−470		mV
			12		7			25°C	−505	−450	−350	
								75°C		−410	−315	
$V_{OH(Y)}$	High-level output voltage at OR output	2	14	2		1.05 V	0 V	0°C	315	410		mV
			12	8				25°C	350	450	525	
								75°C		520	600	
$V_{OL(Y)}$	Low-level output voltage at OR output	2	14	2		0.65 V	0 V	0°C	−505	−470		mV
			12	8				25°C	−505	−450	−350	
								75°C		−410	−310	
$V_{OH(Z)}$	High-level output voltage at NOR output	2	14		4	0.65 V	0 V	0°C	315	410		mV
			12		7			25°C	350	450	525	
								75°C		520	600	
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	14		4	1.05 V	0 V	0°C	−505	−470		mV
			12		7			25°C	−505	−450	−350	
								75°C		−410	−315	
I_{IH}	High-level input current	3	14			2.8 V	0 V	0°C			220	μA
			12					25°C			200	
								75°C			170	
I_{IL}	Low-level input current	3	12, 14			0 V	0 V	0°C			220	μA
								25°C			200	
								75°C			170	
I_{C+}	Supply current from V_{C+}	4				Both HLL inputs at 2.4 V		25°C	10		17.5	mA
I_{CC}	Supply current from V_{CC}	4				Both HLL inputs at 2.4 V		25°C	9		16	mA
I_{EE}	Supply current from V_{EE}	4				Both HLL inputs at 2.4 V		25°C	−22		−38	mA
C_{in}	Input capacitance (see Note 6)		14									pF
			12					25°C		2		
z_{out}	Output impedance (see Note 7)			2	4			25°C		5		Ω
				8	7							

*ECL inputs (pins 11 and 16) biased to −0.5 V, V_{BB} (pins 1 and 9) = GND, V_{CC} (pins 3 and 6) = 1.32 V ± 1%, V_{EE} (pin 10) = −3.2 V ±1%, V_{C+} (pin 5) = 4.8 V ± 1%.

NOTES: 4. Each gate is tested separately unless otherwise noted. See referenced test figure for output terminations.

5. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.

6. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. $C_{in} = Q/V$.

7. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

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ECL2536 electrical characteristics using ECL inputs

PARAMETER		TEST CONDITIONS*						MIN	TYP	MAX	UNIT
		TEST FIGURE	TERMINALS (SEE NOTE 4)		INPUT CONDITIONS		T_A	(SEE NOTE 5)			
			INPUTS	OUTPUTS Y	OUTPUTS Z	INPUT UNDER TEST, V_I	ECL INPUT OF OTHER GATE					
V_{IH}	High-level input voltage		16					0°C	150		720	mV
			11					25°C	150		720	
								75°C	150		720	
V_{IL}	Low-level input voltage		16					0°C	−1500		−150	mV
			11					25°C	−1500		−150	
								75°C	−1500		−150	
$V_{OH(Y)}$	High-level output voltage at OR output	2	16	2		0.2 V	−0.5 V	0°C	315	410		mV
			11	8				25°C	350	450	525	
								75°C		520	600	
$V_{OL(Y)}$	Low-level output voltage at OR output	2	16	2		−0.2 V	−0.5 V	0°C	−505	−470		mV
			11	8				25°C	−505	−450	−350	
								75°C		−410	−310	
$V_{OH(Z)}$	High-level output voltage at NOR output	2	16		4	−0.2 V	−0.5 V	0°C	315	410		mV
			11		7			25°C	350	450	525	
								75°C		520	600	
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	16		4	0.2 V	−0.5 V	0°C		−410		mV
			11		7			25°C		−390	−310	
								75°C		−350	−280	
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	16		4	0.4 V	−0.5 V	0°C	−505	−470		mV
			11		7			25°C	−505	−450		
								75°C		−410	−315	
$V_{OH(Y)}$	High-level output voltage at OR output	2	11	8		0.15 V	−0.5 V	0°C	290			mV
								25°C	325			
								75°C				
$V_{OL(Y)}$	Low-level output voltage at OR output	2	11	8		−0.15 V	−0.5 V	0°C				mV
								25°C			−325	
								75°C			−290	
I_{IH}	High-level input current	3	16			0.5 V	−0.5 V	0°C			255	μA
			11					25°C			235	
								75°C			200	
I_{IL}	Low-level input current (both ECL inputs)	5	11, 16			Both ECL inputs at −3.2 V		0°C			−0.5	μA
								25°C			−0.5	
								75°C			−0.5	
I_{C+}	Supply current from V_{C+}	4				Both ECL inputs at −0.5 V		25°C	5		8.5	mA
I_{CC}	Supply current from V_{CC}	4				Both ECL inputs at −0.5 V		25°C	13		22	mA
I_{EE}	Supply current from V_{EE}	4				Both ECL inputs at −0.5 V		25°C	−20		−35	mA
C_{in}	Input capacitance (see Note 6)		16					25°C		5		pF
			11									
z_{out}	Output impedance (see Note 7)			2	4			25°C		5		Ω
				8	7							

*HLL inputs (pins 12 and 14) grounded, V_{BB} (pins 1 and 9) = GND, V_{CC} (pins 3 and 6) = 1.32 V ± 1%, V_{EE} (pin 10) = −3.2 V ± 1%, V_{C+} (pin 5) = 4.8 V ± 1%.

NOTES: 4. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination.
5. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.
6. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. $C_{in} = Q/V$.
7. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

ECL2537 electrical characteristics

PARAMETER (SEE NOTE 8)	TEST FIGURE	TEST CONDITIONS* TERMINALS (SEE NOTE 4) INPUTS	OUTPUTS Y	OUTPUTS Z	INPUT CONDITIONS: INPUT UNDER TEST, V_I	OTHER INPUT OF SAME GATE	INPUTS OF OTHER GATE	T_A	MIN (SEE NOTE 5)	TYP (SEE NOTE 5)	MAX (SEE NOTE 5)	UNIT
V_{IH}		13, 14						0°C	150		720	mV
		11, 12						25°C	150		720	
								75°C	150		720	
V_{IL}		13, 14						0°C	−1500		−150	mV
		11, 12						25°C	−1500		−150	
								75°C	−1500		−150	
$V_{OH(Y)}$	6	13, 14	1		0.2 V	−0.5 V	−0.5 V	0°C	3	3.4		V
		11, 12	8					25°C	3.2	3.6		
								75°C		3.8		
$V_{OL(Y)}$	6	13, 14	1		−0.2 V	−0.5 V	−0.5 V	0°C	−0.8	−0.35		V
		11, 12	8					25°C	−0.7	−0.25	0.2	
								75°C		−0.15	0.3	
$V_{OH(Z)}$	6	13, 14		2	−0.2 V	−0.5 V	−0.5 V	0°C	3	3.4		V
		11, 12		7				25°C	3.2	3.6		
								75°C		3.8		
$V_{OL(Z)}$	6	13, 14		2	0.2 V	−0.5 V	−0.5 V	0°C	−0.7	−0.2		V
		11, 12		7				25°C	−0.6	−0.1	0.2	
								75°C		0.0	0.3	
$V_{OL(Z)}$	6	13, 14		2	0.4 V	−0.5 V	−0.5 V	0°C	−1	−0.35		V
		11, 12		7				25°C	−0.9	−0.25	0.2	
								75°C		−0.15	0.3	
$V_{OH(Y)}$	6	13, 14	1		0.15 V	−0.5 V	−0.5 V	0°C	2.9			V
		11, 12	8					25°C	3.1			
								75°C				
$V_{OL(Y)}$	6	13, 14	1		−0.15 V	−0.5 V	−0.5 V	0°C				V
		11, 12	8					25°C			0.3	
								75°C			0.4	
I_{IH}	7	13, 14			0.5 V	−0.5 V	−0.5 V	0°C			510	μA
		11, 12						25°C			470	
								75°C			400	
I_{IL} (all inputs)	8	11, 12, 13, 14			Both inputs of both gates in parallel at −3.2 V			0°C			−0.5	μA
								25°C			−0.5	
								75°C			−0.5	
I_{C+}	9				All inputs at −0.5 V			25°C	8		17	mA
I_{EE}	9				All inputs at −0.5 V			25°C	−8		−17	mA
C_{in} (see Note 6)		13, 14						25°C		5		pF
		11, 12										
z_{out} (see Note 7)			1	2				25°C		10		Ω
			8	7								

*V_{BB} (pins 9 and 16) = GND, V_{C+} (pin 5) = 4.8 V ± 1%, V_{EE} (pin 10) = −3.2 V ± 1%.

NOTES: 4. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination.
5. The algebraic convention where the most positive limit is designated at maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.
6. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. $C_{in} = Q/V$.
7. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.
8. See pages 4 or 5 for defining term associated with each symbol.

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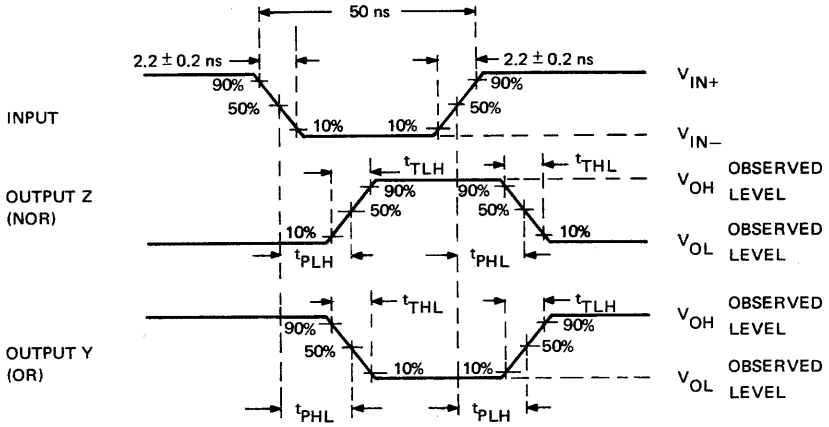
operating characteristics at specified free-air temperature (see figure 1)

TERMINALS TO BE TESTED (SEE NOTES 9, 10, and 11)				C_L	t_{PHL} and/or t_{PLH} PROPAGATION TIMES–ns									t_{THL} and/or t_{TLH} TRANSITION TIMES–ns								
					T_A = 0°C			T_A = 25°C			T_A = 75°C			T_A = 0°C			T_A = 25°C			T_A = 75°C		
INPUT	OUTPUT	INPUT	OUTPUT	pF	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
ECL2536 using HLL inputs (see figure 10)																						
14	2, 4	12	8, 7	4	4.0			2.8	3.9	5.5	4.0			3.9			2.5	4.0	6.5	4.2		
				50	5.0			3.7	5.0	6.5	5.2			4.3			2.5	4.4	7	4.3		
ECL2536 using ECL inputs (see figure 11)																						
16	2, 4	11	8, 7	4	2.5			1.3	2.4	3.7	2.5			4.1			2.5	4.0	6.5	4.1		
				50	3.4			2.2	3.5	4.8	3.4			4.4			2.5	4.4	7	4.3		
ECL2537 (see figure 12)																						
13 14	1, 2	11 12	8, 7	15	3.4			2.2	3.5	5	3.6			3.7			2.2	3.7	6.5	3.8		



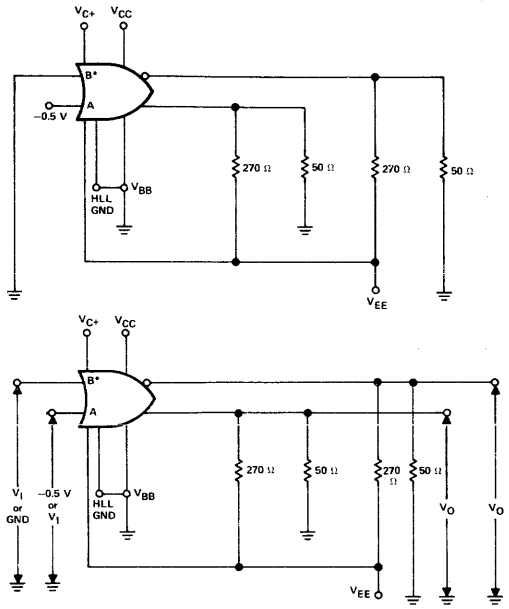
VOLTAGE WAVEFORMS

MODULE	V_{IN+} (V)	V_{IN-} (V)
ECL2536 (HLL)	1.40 ± 0.05	0 ± 0.05
ECL2536 (ECL)	0.40 ± 0.02	−0.50 ± 0.02
ECL2537	0.40 ± 0.05	−0.50 ± 0.05

FIGURE 1–PROPAGATION DELAY AND TRANSITION TIMES

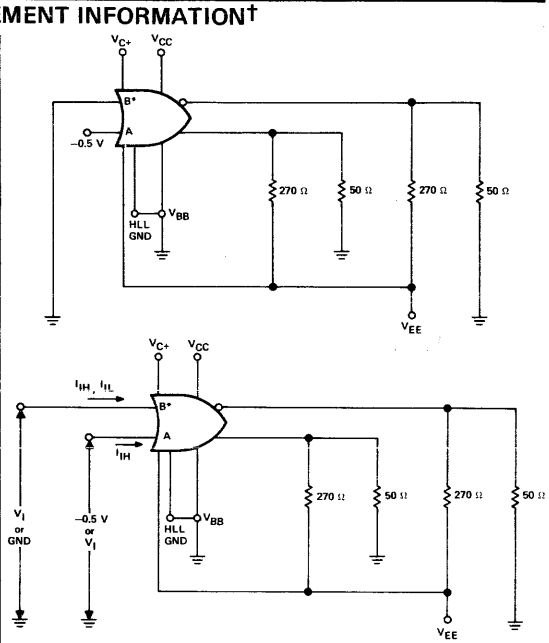
NOTES: 9. Each gate is tested separately.
10. The input pulse is measured as it is applied sequentially to each input of the gate under test and a waveform measurement is made at each of the outputs of that gate.
11. Bias voltages and loads for the gate under test are shown in Figures 10 through 12. Unused gates have inputs biased as shown in Figure 2 for the ECL2536 or Figure 6 for the ECL2537, outputs under load, and power applied.

PARAMETER MEASUREMENT INFORMATION†



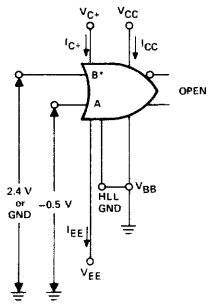
A. V_I is first applied to each HLL input separately (other HLL input grounded) with both ECL inputs at −0.5 V; then V_I is applied to each ECL input separately (other ECL input at −0.5 V) with both HLL inputs at ground.
B. Each output is tested separately.

FIGURE 2–V_{OH} AND V_{OL}



V_I is first applied to each HLL input separately (other HLL input grounded) with both ECL inputs at −0.5 V; then V_I is applied to each ECL input separately (other ECL input at −0.5 V) with both HLL inputs at ground.

FIGURE 3–I_{IH} AND I_{IL}



A. The supply currents are measured with both the HLL inputs first at 2.4 V, then at GND.
B. Both gates are tested simultaneously. I_{CC} is the total current into the two V_{CC} terminals.

FIGURE 4–I_{C+}, I_{CC}, AND I_{EE}

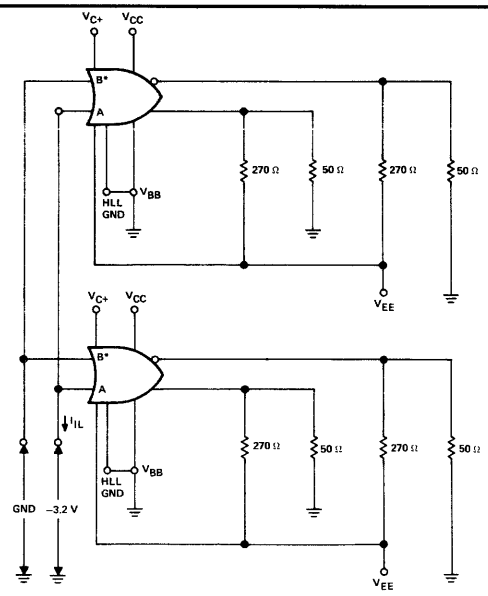


FIGURE 5–I_{IL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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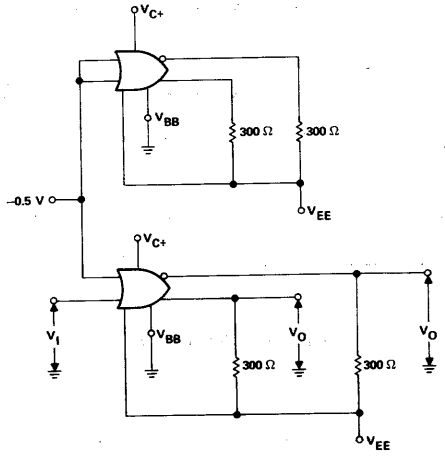
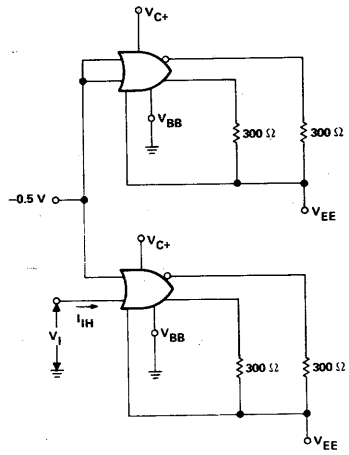
PARAMETER MEASUREMENT INFORMATION†



A. V_I is applied to each input separately.
B. Each output is tested separately.

FIGURE 6—V_{OH} AND V_{OL}



Each input is tested separately.

FIGURE 7—I_{IH}

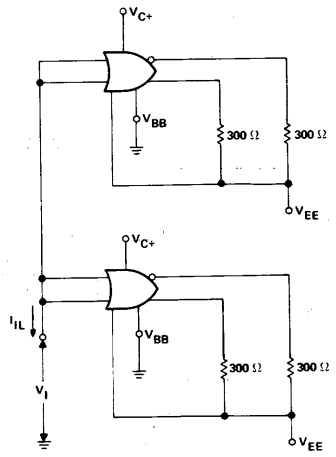
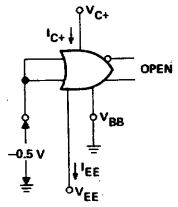


FIGURE 8—I_{IL}



Both gates are tested simultaneously.

FIGURE 9—I_{C+} OR I_{EE}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

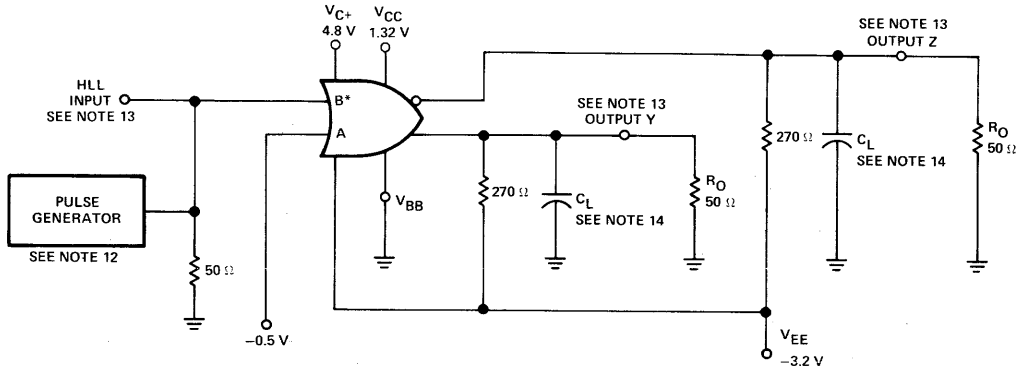


FIGURE 10–ECL2536 PROPAGATION DELAY AND TRANSITION TIMES (HLL INPUT)

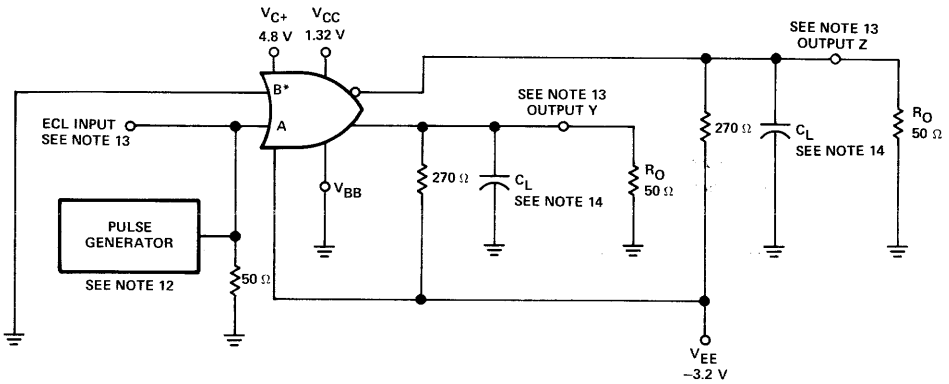


FIGURE 11–ECL2536 PROPAGATION DELAY AND TRANSITION TIMES (ECL INPUT)

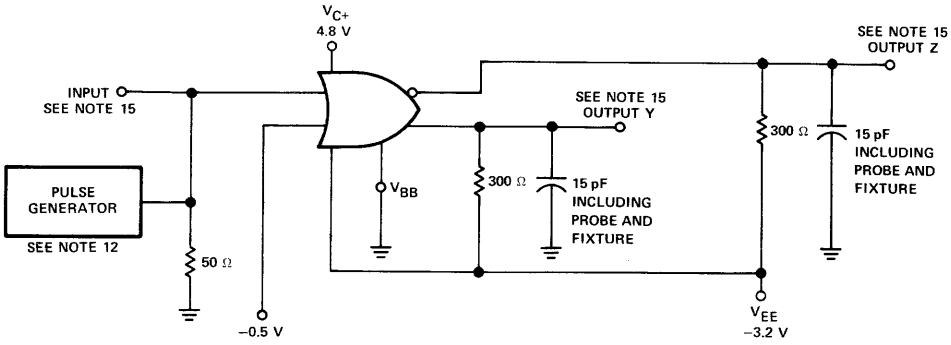


FIGURE 12–ECL2537 PROPAGATION DELAY AND TRANSITION TIMES

NOTES: 12. The generator has the following characteristics: Z_{out} = 50 Ω, PRR = 1 MHz. See waveform details in Figure 1.
13. The waveforms for ECL2536 are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. Either a high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF, or a 50-Ω impedance system can be used. The 50-Ω resistors designated R_O are the oscilloscope input resistance in the 50-Ω system or discrete resistors with a high-impedance probe.
14. C_L includes probe and fixture capacitance. A capacitance of 50 pF can be used to approximate an a-c fan-out of 10.
15. The waveforms for ECL2537 are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. A high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF is used.

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GENERAL APPLICATION INFORMATION

ECL2536

input conditions

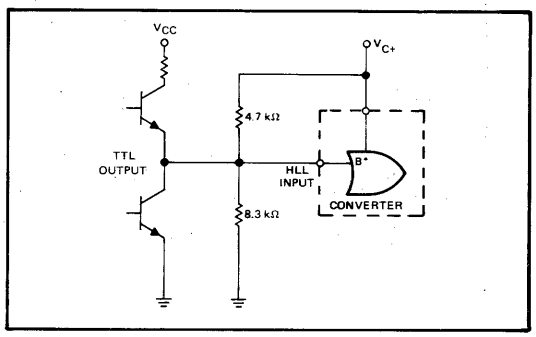
The ECL2536 converts high-level-logic inputs to ECL2500-logic-level outputs.

A control INHIBIT/ENABLE ECL input is provided to lock out data presented at the HLL input. A high-level (H) input voltage inhibits the converter outputs in a stable state such that signals on the HLL input are not transmitted through the converter. A low-level (L) input voltage enables the converter and the output levels are determined by the logic level of the HLL input.

The output feeding the HLL input should have an H level $\geq$ 1.2 V and an L level $\leq$ 0.5 V in order to maintain at least a 150-mV noise margin.

driving by TTL

The HLL input requires up to 220 μA of current to be supplied with both H-level and L-level voltage inputs. TTL outputs are designed to sink current in the low state, not to supply current. To assure reliable performance with all types of TTL circuits, it is recommended that a resistor divider be placed at the HLL input external to the package. The divider has 4.7 kΩ from the HLL input to V_{C+} and 8.3 kΩ to ground, as shown.



ECL output loading

General loading for fan-out from the ECL outputs may be divided into two classes:

CLASS I **Short-Line or Cluster Loading**
Loads which can be connected within two inches of any source can be treated as lumped capacitive loads which include the gate inputs and stub-line capacitances. Switching times can be interpolated accordingly. No two dotted outputs can be more than two inches apart for this case.

CLASS II **Long-Line or Distributive Loading**
These loads must be treated as lumped loads along a transmission line and termination should be at the end of the transmission chain. No more than 20 pF of load is recommended per 4.5 inches of 50-ohm printed line (with dielectric constant of 4.5) in order that the reflection coefficient be no greater than 20%. If the loads are lumped loads of 20 pF, they must be 4.5 inches apart. If individual gates and **CLASS I** loads are distributed, they must not exceed the 20 pF per 4.5 inches of line.

ECL2537

The ECL2537 converts ECL2500-logic-level inputs to high-level-logic outputs.

An external pull-down resistor to a negative voltage must be provided on the HLL output terminals. The size of the resistor is determined by the current it must sink in order to maintain the correct low-level voltage with the DTL or TTL fan-out being driven.

Characterization is with a pull-down resistor of 300 Ω to -3.2 V which represents a fan-out of five Texas Instruments Series 54/74 TTL logic gates.

No wired-OR connection is allowed on the HLL outputs because an emitter-follower junction breakdown may occur if one converter output is high and this forces another output to be high which would otherwise be low.

The V_{C+} power supply must be held at 4.8 V $\pm$ 1%. Otherwise, the output voltage specifications for maximum V_{OL} or minimum V_{OH} may be exceeded.

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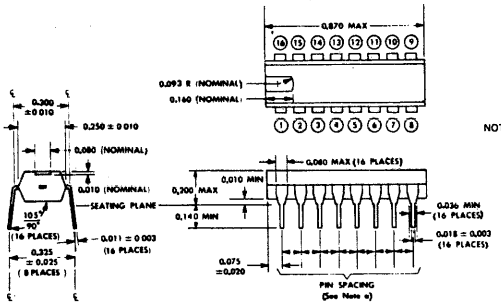
TYPES ECL2536, ECL2537
HLL-TO-ECL AND ECL-TO-HLL CONVERTERS

mechanical data

The circuit bars are mounted on a 16-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

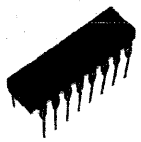
The plastic case is electrically nonconductive.

16-PIN PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



NOTES: a. The true-position pin spacing is 0.100 between center-lines. Each pin centerline is located within 0.010 of its true longitudinal position relative to pins 1 and 16.

b. All dimensions are in inches unless otherwise noted.



4

terminal designations

Pin assignments are shown in the table below and correspond to the logic diagrams on page 2.
Outputs are denoted Y or Z. Inputs are denoted A, B, or B*.
Respective inputs and outputs are identified by a gate number preceding the pin symbol.
Power is supplied via the V_{C+}, V_{CC}, V_{EE}, and V_{BB} terminals.
V_{BB} is a reference voltage.
NC indicates no internal connection.

PIN ASSIGNMENTS

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ECL2536	V_{BB}	1Y	V_{CC}	1Z	V_{C+}	V_{CC}	2Z	2Y	V_{BB}	V_{EE}	2A	2B*	HLL GND	1B*	NC	1A
ECL2537	1Y	1Z	NC	NC	V_{C+}	NC	2Z	2Y	V_{BB}	V_{EE}	2A	2B	1A	1B	NC	V_{BB}

*HLL input

Multiple V_{CC} terminals have been supplied to reduce cross-talk noise. Multiple V_{BB} terminals are also provided. All V_{BB} and V_{CC} terminals should be connected even if all gates in the module are not used.

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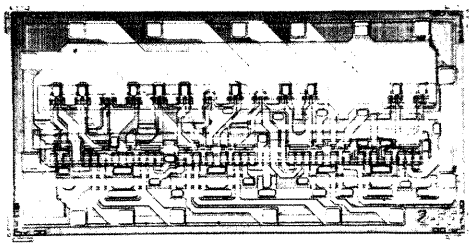
TYPES ECL2540 THRU ECL2542
EMITTER-COUPLED-LOGIC BISTABLE MODULES

ECL2500 SERIES EMITTER-COUPLED-LOGIC (ECL) BISTABLE MODULES FOR APPLICATION IN ULTRA-HIGH-SPEED DIGITAL SYSTEMS



description

The ECL2500 series is a compatible family of ECL functions with basic gate delays of 2 to 3 ns per stage. The family is specifically designed for operation from 0°C to 70°C.

The ECL2500 family includes:

- Basic Gate Modules
- Multifunction Gate Modules
- **Bistable Modules**
- Arithmetic Modules
- Interface Modules
- Memory Module

family features

- High speed . . . typical gate propagation delay time of 2.5 ns
- Complementary OR/NOR outputs with capability for wired-OR connections
- Designed for use with transmission lines to ensure maximum signal transmission without noise. Characterized for 50-ohm lines
- High noise immunity: ±225 mV typical at 25°C

This data sheet covers the bistable modules.
Separate data sheets cover the balance of the ECL2500 modules.

ECL2500 series bistable modules

The ECL2500 series bistable modules are summarized in the table below. These modules contain the ECL circuits shown in the schematics of Figures A, B, and C on pages 6 and 7. Logic diagrams of ECL2540 through ECL2542 are shown on page 4.

SUMMARY OF BISTABLE MODULES

MODULE	GATES PER MODULE	LATCHES PER MODULE	OUTPUTS PER BISTABLE CIRCUIT	
			Q (LATCH)	$\overline{Q}$ (LATCH COMPLEMENT)
ECL2540	4	2	1	1
ECL2541	9	2	1	2
ECL2542	13	2		1

APPLICATION INFORMATION

general

The bistable modules specified in this data sheet contain dual latches. Each half of the ECL2540 is a latch with a separate data input. Two clock inputs, C and C′, feed both latches. Q and $\overline{Q}$ outputs are provided from each latch. Each half of the ECL2541 is a latch with additional circuitry which provides a data input and a gate input to control the input data. Common clock, set, and reset inputs are included. One Q and two $\overline{Q}$ outputs are provided for each latch. Each half of the ECL2542 is a latch with additional circuitry which provides two data inputs each with a gate input to control the input data. Common clock, set, and reset inputs serve both latches. Only $\overline{Q}$ outputs are provided.

Each latch has the possibility to operate in the following modes:

Register – The mode in which the data input controls the state of the latch. Q is high when data is high.

Storage – The mode in which the latch stores data received during the register mode. Input data is locked out from changing the latch state.

Set – The mode whereby Q is set high (or $\overline{Q}$ low) which is normally done when the clock is high.

Reset – The mode whereby Q is set low (or $\overline{Q}$ high) which is normally done when the clock is high (low for ECL2540).

The ECL2541 and ECL2542 have the register mode subdivided:

Register Mode/Clock Control – The mode whereby the gate input is low, allowing the data to set the latch when the clock goes low.

Register Mode/Gate Control – The mode whereby the clock input is low, allowing the data to set the latch when the gate is low.

Each Q and $\overline{Q}$ output must be terminated in a pull-down resistor.

The Q terminal of the ECL2541 must have a termination resistor (in addition to the pull-down resistor) on the output at all times (whether the output is used for fan-out or not), because internal feedback occurs from this point.

For full-temperature-range operation of all devices, data must be present before the clock pulse and the minimum width of the clock pulse is 4.5 ns. For the ECL2541 and ECL2542, the data pulse must extend beyond the clock pulse to allow for the delay associated with the clock-buffering gate.

For the ECL2540, latching occurs on either the leading or trailing edge of the C or C′ pulse. For the ECL2541 and ECL2542, latching occurs on the leading edge of the clock pulse.

Multiple V_{CC} terminals have been supplied to reduce crosstalk noise. All V_{CC} terminals should be connected even if all gates in a module are not used.

General loading for fan-out may be divided into two classes:

CLASS I **Short-Line or Cluster Loading.**
Loads which can be connected within two inches of any source can be treated as lumped capacitive loads which include the gate inputs and stub-line capacitances. Switching times can be interpolated accordingly. No two dotted outputs can be more than two inches apart for this case.

CLASS II **Long-Line or Distributive Loading.**
These loads must be treated as lumped loads along a transmission line and termination should be at the end of the transmission chain. No more than 20 pF of load is recommended per 4.5 inches of 50-ohm printed line (with dielectric constant of 4.5) in order that the reflection coefficient be no greater than 20%. If the loads are lumped loads of 20 pF, they must be 4.5 inches apart. If individual gates and **CLASS I** loads are distributed, they must not exceed the 20 pF per 4.5 inches of line.

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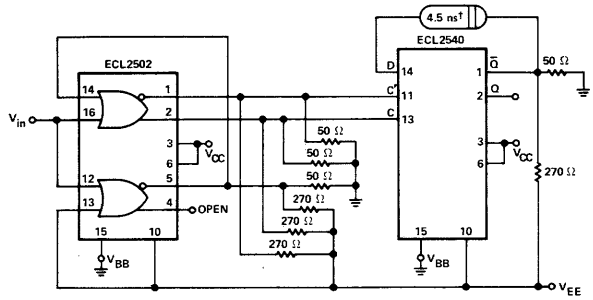
APPLICATION INFORMATION

ECL2540

The ECL2540 requires two clock inputs. Faulty operation occurs if the C′ input lags behind C by more than 0.5 ns. The interval between the transition of the two clocks is referred to as skew. C′ can be skewed ahead of C by as much as 1.5 ns.

The ECL2540 can be used as a toggle as shown in Figure 1. However, the delay from $\overline{Q}$ to D must be greater than the clock pulse width. Thus, when pulse widths are very long, this becomes impractical unless a technique such as that shown in Figure 1 is used. This technique uses two gates of an ECL2502 as a pulse-shaping network to allow operation of a toggle from 100 megacycles per second down to cycles per second.



†Delay between $\overline{Q}$ and D must be greater than 4.5 ns based on the propagation delay characteristics of the ECL2502 and its feedback loop.

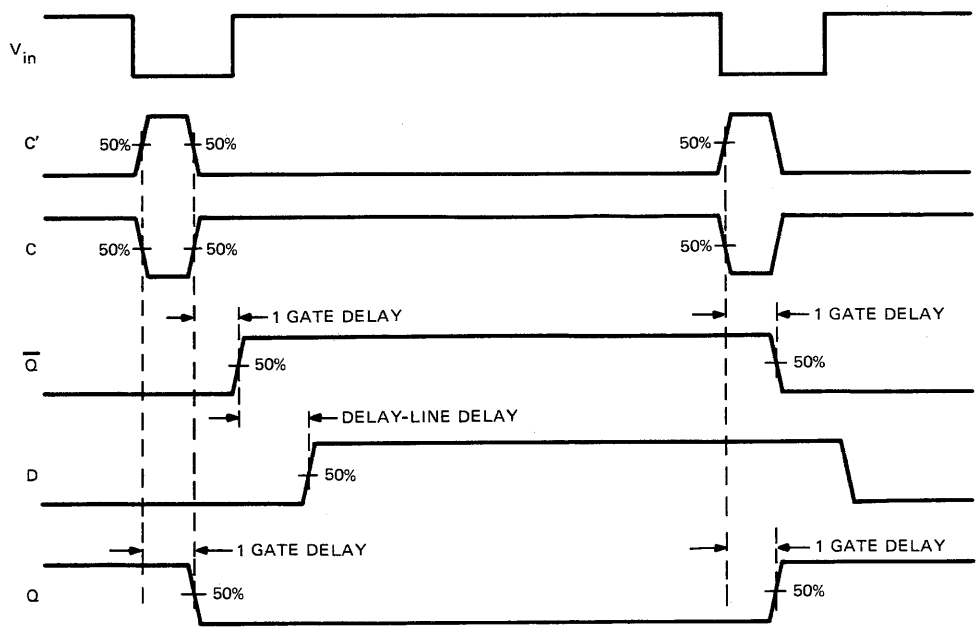
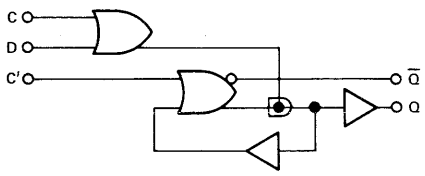


FIGURE 1–ECL2540 USED AS A TOGGLE (WITHOUT SKEW)

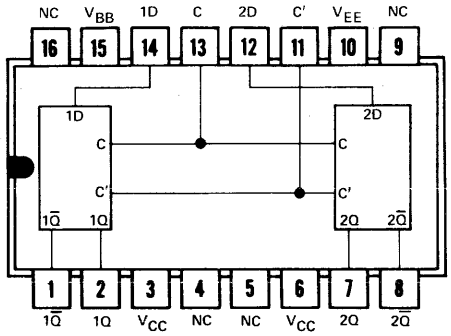
TYPES ECL2540 THRU ECL2542
EMITTER-COUPLED-LOGIC BISTABLE MODULES

logic†

ECL2540



$$Q_{n+1} = (C+D)(Q_n+C')$$
$$\bar{Q}_{n+1} = (\bar{C}\bar{D}+\bar{Q}_n)\bar{C}'$$



NC—No internal connection

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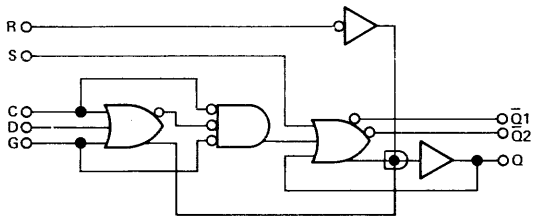
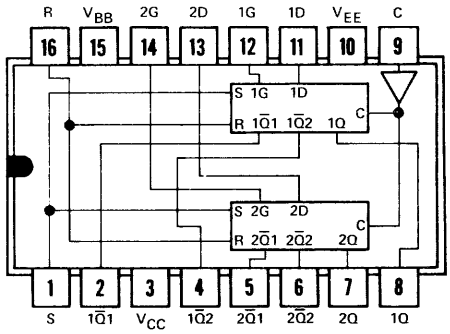
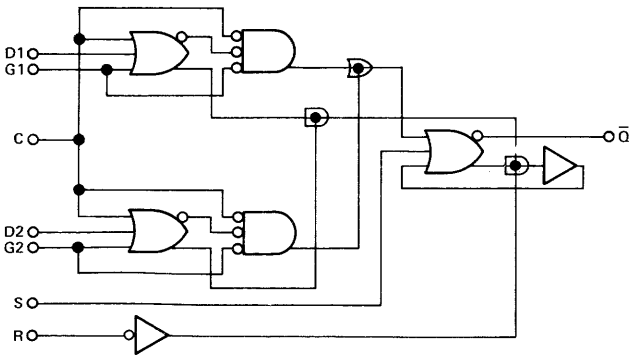
ECL2541



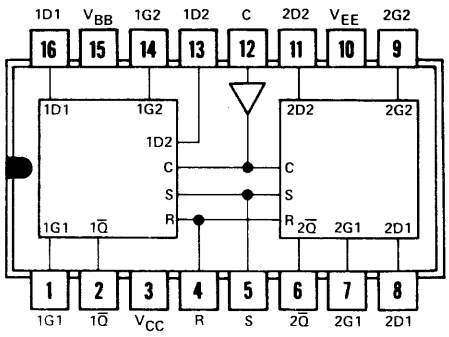
$$Q_{n+1} = \bar{R}[(C+D+G)(Q_n+S)+\bar{C}D\bar{G}]$$
$$\bar{Q}_{n+1} = \bar{S}(C+\bar{D}+G)(\bar{Q}_n+R+\bar{C}\bar{D}\bar{G})$$



ECL2542



$$\bar{Q}_{n+1} = \bar{S}[C+(\bar{D}1+G1)(\bar{D}2+G2)]\,[\bar{Q}_n+R+\bar{C}(\bar{D}1\bar{G}1+\bar{D}2\bar{G}2)]$$



†One half of each bistable module is shown in the logic diagrams.

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truth tables (for this series, H = positive voltage, L = negative voltage, X = irrelevant)

ECL2540

MODE	INPUTS			OUTPUTS	
	CLOCK		DATA	LATCH	LATCH COMPLEMENT
	C	C′	D	Q_{n+1}	$\overline{Q}_{n+1}$
Register	L	H	H	H	L
	L	H	L	L	(L)†
Clock-controlled storage	H	L	X	Q_n	$\overline{Q}_n$
Set	H	H	X	H	L
Reset	L	L	L	L	H
Forbidden (see Note 1)	L	L	H	Q_n	$\overline{Q}_n$

ECL2541

MODE	INPUTS					OUTPUTS	
	SET	RESET	CLOCK	GATE	DATA	LATCH	LATCH COMPLEMENT
	S	R	C	G	D	Q_{n+1}	$\overline{Q}_{n+1}$
Register	L	L	L	L	H	H	L
	L	L	L	L	L	L	H
Clock-controlled storage	L	L	H	X	X	Q_n	$\overline{Q}_n$
Gate-controlled storage	L	L	X	H	X	Q_n	$\overline{Q}_n$
Set	H	L	H	X	X	H	L
	H	L	X	H	X	H	L
Reset	L	H	H	X	X	L	H
	L	H	X	H	X	L	H
Forbidden	H	L	L	L	H	H	L
	H	L	L	L	L	L	L
	L	H	L	L	H	L	L
	L	H	L	L	L	L	H
	H	H	X	X	X	L	L

ECL2542

MODE	INPUTS							OUTPUT
	SET	RESET	CLOCK	GATE		DATA		LATCH COMPLEMENT
	S	R	C	G1	G2	D1	D2	$\overline{Q}_{n+1}$
Register	L	L	L	H	L	X	D2	$\overline{D2}$
	L	L	L	L	H	D1	X	$\overline{D1}$
	L	L	L	L	L	D1	D2	$\overline{D1 \cdot D2}$
Clock-controlled storage	L	L	H	X	X	X	X	$\overline{Q}_n$
Gate-controlled storage	L	L	X	H	H	X	X	$\overline{Q}_n$
Set	H	L	H	X	X	X	X	L
	H	L	X	H	H	X	X	L
Reset	L	H	H	X	X	X	X	H
	L	H	X	H	H	X	X	H
Forbidden	H	L	L	L	X	X	X	See Note 2
	H	L	L	X	L	X	X	
	L	H	L	L	X	X	X	
	L	H	L	X	L	X	X	
	H	H	X	X	X	X	X	

†$\overline{Q}$ is made low by C′ being high. When C′ returns to its normal state (low) following the clock pulse, $\overline{Q}$ goes high (the complement of data)

NOTES: 1. This condition is data-controlled storage, whereas only clock-controlled storage is desired in the ECL2540. Hence, this condition is placed in the forbidden category.

2. The forbidden input combinations for ECL2542 may produce pseudo-stable output states which do not persist when a storage mode is subsequently selected or may produce outputs not in harmony with the normally used input patterns.

schematics

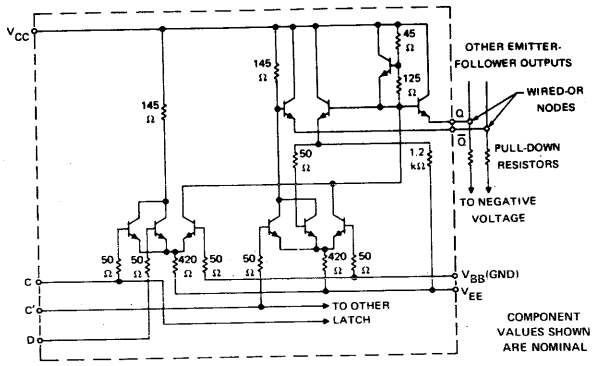

FIGURE A–SCHEMATIC OF HALF OF ECL2540

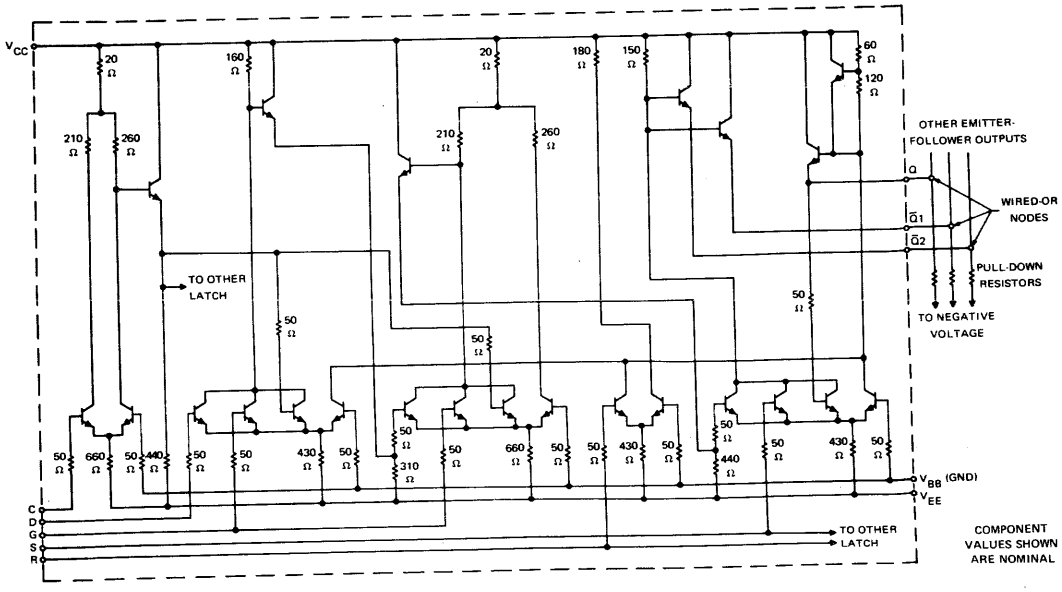

FIGURE B–SCHEMATIC OF HALF OF ECL2541

Emitter-follower outputs require an external pull-down resistor. The wired-OR function can be obtained by connecting the emitter-follower outputs of a bistable module to the emitter-follower outputs of other gates or other bistable modules. Only one pull-down resistor is required for each wire-OR node.

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schematic

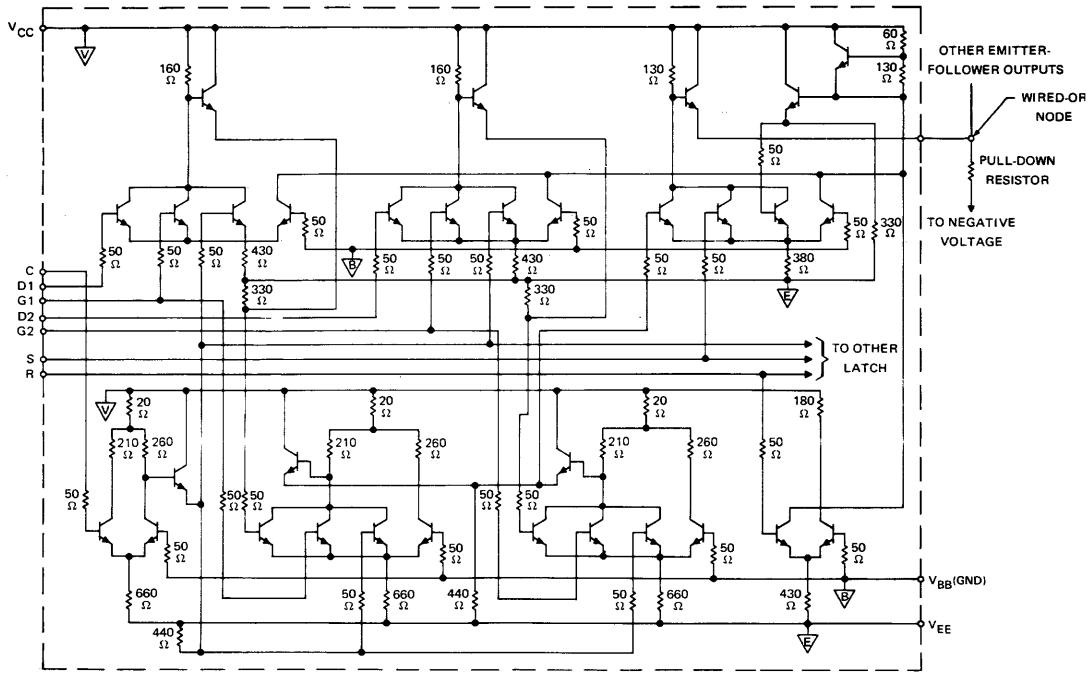

FIGURE C–SCHEMATIC OF HALF OF ECL2542

COMPONENT VALUES SHOWN ARE NOMINAL

▽ –V_{CC} bus
▽ –V_{BB} bus
▽ –V_{EE} bus (substrate)

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absolute maximum ratings (see note 3)

Terminal voltages and currents . . . . . See table below
Storage temperature range . . . . . −40°C to 150°C
Free-air temperature range with supply and bias voltages applied . . . . . −40°C to 100°C

TERMINAL VOLTAGE AND/OR CURRENT, T_A = 0°C TO 75°C (SEE NOTES 4 AND 5)

TERMINAL	REMARKS	VOLTAGE		CURRENT
		CONTINUOUS	20-μs SURGE	
V_{CC}		2 V	4.5 V	
V_{EE}		−4 V	−7 V	
Each Input	All other inputs open	−3.5 V	−4 V	
		2 V	2 V	
Output Q	At high level			−40 mA
Output $\overline{Q}$	At high level			−40 mA

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recommended operating conditions

Supply voltage V_{CC} . . . . . 1.32 V ± 2%
Supply voltage V_{EE} . . . . . −3.2 V ± 2%
Reference voltage V_{BB} . . . . . 0 V (GND)
Reverse bias on unused inputs . . . . . −1 V ± 0.5 V
Normalized d-c fan-out . . . . . 0 to 35
Load on each output . . . . . characterized at 270 Ω to V_{EE}, 50 Ω to GND
Operating free-air temperature range . . . . . 0°C to 75°C

NOTES: 3. Absolute maximum ratings are limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing.
4. Maximum terminal conditions must be considered as mutually exclusive.
5. All voltages are referenced to V_{BB}, which is at GND.

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ECL2540 electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS*									MIN	TYP	MAX	UNIT
		TEST FIGURE	INITIAL CONDITIONS (SEE TABLE I)	VOLTAGE AT INPUT UNDER TEST	INPUT(S) UNDER TEST	OTHER INPUT TERMINALS 0.5 V	OTHER INPUT TERMINALS −0.5 V	OUTPUT TERMINAL Q	OUTPUT TERMINAL $\bar{Q}$	T_A	(SEE NOTE 6)			
V_{IH}	High-level input voltage									0°C 25°C 75°C	150 150 150		720 720 720	mV
V_{IL}	Low-level input voltage									0°C 25°C 75°C	−1500 −1500 −1500		−150 −150 −150	mV
$V_{OH(Q)}$	High-level output voltage at Q output, register mode	4	X	0.2 V	14 12	11 11	13 13	2 7		0°C 25°C 75°C	280 315			mV
$V_{OL(Q)}$	Low-level output voltage at Q output, register mode	4	X	−0.2 V	14 12	11 11	13 13	2 7		0°C 25°C 75°C			−330 −210	mV
$V_{OH(Q)}$	High-level output voltage at Q output, storage mode	4	S	0.2 V	13 13		11, 14 11, 12	2 7		0°C 25°C 75°C	280 315	365 400 470	500 580	mV
$V_{OL(Q)}$	Low-level output voltage at Q output, storage mode	4	R	−0.2 V	11 11	13, 14 13, 12		2 7		0°C 25°C 75°C	−505 −480	−440 −400 −280	−330 −210	mV
$V_{OH(\bar{Q})}$	High-level output voltage at $\bar{Q}$ output, storage mode	4	R	−0.2 V	11 11	13, 14 13, 12			1 8	0°C 25°C 75°C	280 315	365 400 470	500 580	mV
$V_{OL(\bar{Q})}$	Low-level output voltage at $\bar{Q}$ output, storage mode	4	S	0.2 V	13 13		11, 14 11, 12		1 8	0°C 25°C 75°C	−505 −490	−440 −425 −390	−350 −315	mV
$V_{OH(Q)}$	High-level output voltage at Q output, set mode	4	R	0.2 V	11, 13 11, 13		14 12	2 7		0°C 25°C 75°C	280 315			mV
$V_{OL(Q)}$	Low-level output voltage at Q output, reset mode	4	S	−0.2 V	11, 13 11, 13		14 12	2 7		0°C 25°C 75°C			−330 −210	mV
I_{IH}	High-level input current	5	X	0.5 V	14 12		11, 12, 13 11, 13, 14			0°C 25°C 75°C			255 235 200	μA
			X	0.5 V	11 13		12, 13, 14 11, 12, 14			0°C 25°C 75°C			510 470 400	μA
I_{IL}	Low-level input current	6	X	All inputs in parallel at −3.2 V						0°C 25°C 75°C			−0.5 −0.5 −0.6	μA
I_{CC} or $-I_{EE}$	Supply current	7	X	All inputs in parallel at −0.5 V						25°C	20		34	mA
C_{in}	Input capacitance (see Note 7)		X		Each					25°C		5		pF
Z_{out}	Output impedance (see Note 8)		X					2, 7	1, 8	25°C		5		Ω

NOTES: 6. The algebraic convention where the most-positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more-negative voltages.

7. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. C_{in} = Q/V. When a terminal is an input to more than one gate, multiply the value given by the number of gates to which this terminal is an input.

8. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

TABLE I—INITIAL CONDITIONS

Several of the parameters require the application of conditions which cause the outputs to assume definite states prior to applying test conditions specified above.

SYMBOL	DESCRIPTION	INPUT TERMINALS* 0.5 V	INPUT TERMINALS* −0.5 V
X	Irrelevant		
S	Set 1Q and 2Q high, $1\bar{Q}$ and $2\bar{Q}$ low	11, 13	14, 12
R	Reset 1Q and 2Q low, $1\bar{Q}$ and $2\bar{Q}$ high		11, 12, 13, 14

*V_{BB} (pin 15) = GND, V_{CC} (pins 3 and 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V. Input and output terminals are open except as specified in these tables and in the d-c test figures.

ECL2541 electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS*																UNIT
		TEST FIGURE	INITIAL CONDITIONS (SEE TABLE II)	VOLTAGE AT INPUT UNDER TEST	INPUT(S) UNDER TEST	OTHER INPUT TERMINALS		OUTPUT TERMINAL		T_A	MIN	TYP (SEE NOTE 6)	MAX	
						0.5 V	−0.5 V	Q	$\bar{Q}$					
V_{IH}	High-level input voltage									0°C	150		720	mV
										25°C	150		720	
										75°C	150		720	
V_{IL}	Low-level input voltage									0°C	−1500		−150	mV
										25°C	−1500		−150	
										75°C	−1500		−150	
$V_{OH(Q)}$	High-level output voltage at Q output, register mode	4	X	0.2 V	11		1, 9, 12, 16	8		0°C	280			mV
					13		1, 9, 14, 16	7						
				−0.2 V	12	11	1, 9, 16	8		25°C	315			
					14	13	1, 9, 16	7						
				−0.2 V	9	11	1, 12, 16	8		75°C				
					9	13	1, 14, 16	7						
$V_{OL(Q)}$	Low-level output voltage at Q output, register mode	4	X	−0.2 V	11		1, 9, 12, 16	8		0°C			−330	mV
					13		1, 9, 14, 16	7						
				−0.2 V	12		1, 9, 11, 16	8		25°C			−210	
					14		1, 9, 13, 16	7						
				−0.2 V	9		1, 11, 12, 16	8		75°C				
					9		1, 13, 14, 16	7						
$V_{OH(Q)}$	High-level output voltage at Q output, storage mode	4	S	0.2 V	12		1, 9, 11, 16	8		0°C	280	365		mV
					14		1, 9, 13, 16	7			315	400	500	
				0.2 V	9		1, 11, 12, 16	8		25°C		470	580	
					9		1, 13, 14, 16	7		75°C				
$V_{OL(Q)}$	Low-level output voltage at Q output, storage mode	4	R	0.2 V	12	11	1, 9, 16	8		0°C	−505	−440		mV
					14	13	1, 9, 16	7		25°C	−480	−400	−330	
				0.2 V	9	11	1, 12, 16	8		75°C		−280	−210	
					9	13	1, 14, 16	7						
$V_{OH(\bar{Q})}$	High-level output voltage at $\bar{Q}$ output, storage mode	4	R	0.2 V	12	11	1, 9, 16		2, 4	0°C	280	365		mV
					14	13	1, 9, 16		5, 6	25°C	315	400	500	
				0.2 V	9	11	1, 12, 16		2, 4	75°C		470	580	
					9	13	1, 14, 16		5, 6					
$V_{OL(\bar{Q})}$	Low-level output voltage at $\bar{Q}$ output, storage mode	4	S	0.2 V	12		1, 9, 11, 16		2, 4	0°C	−505	−440		mV
					14		1, 9, 13, 16		5, 6	25°C	−490	−425	−350	
				0.2 V	9		1, 11, 12, 16		2, 4	75°C		−390	−315	
					9		1, 13, 14, 16		5, 6					
$V_{OH(Q)}$	High-level output voltage at Q output, set mode	4	R	0.2 V	1	9	16	8		0°C	280			mV
					1	9	16	7		25°C	315			
										75°C				
$V_{OL(Q)}$	Low-level output voltage at Q output, reset mode	4	S	0.2 V	16	9	1	8		0°C			−330	mV
					16	9	1	7		25°C			−210	
										75°C				

(Continued on page 11)

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ECL2541 electrical characteristics at specified free-air temperature (continued)

PARAMETER		TEST CONDITIONS*							MIN	TYP	MAX	UNIT
		TEST FIGURE	INITIAL CONDITIONS (SEE TABLE II)	VOLTAGE AT INPUT UNDER TEST	INPUT(S) UNDER TEST	OTHER INPUT TERMINALS 0.5 V	OTHER INPUT TERMINALS −0.5 V	OUTPUT TERMINAL Q / Q̄	T_A	(SEE NOTE 6)		
I_{IH}	High-level input current	5	X	0.5 V	9		1, 11, 12, 13, 14, 16		0°C		255	µA
					11		1, 9, 12, 13, 14, 16		25°C		235	
					13		1, 9, 11, 12, 14, 16		75°C		200	
					1		9, 11, 12, 13, 14, 16		0°C		510	µA
					12		1, 9, 11, 13, 14, 16		25°C		470	
					14		1, 9, 11, 12, 13, 16		75°C		400	
					16		1, 9, 11, 12, 13, 14					
I_{IL}	Low-level input current	6	X	All inputs in parallel at −3.2 V					0°C		−0.6	µA
									25°C		−0.8	
									75°C		−1.1	
I_{CC} or $-I_{EE}$	Supply current	7	X	All inputs in parallel at −0.5 V					25°C	60	124	mA
C_{in}	Input capacitance (see Note 7)		X		Each				25°C		5	pF
Z_{out}	Output impedance (see Note 8)		X					7, 8 / 2, 4, 5, 6	25°C		5	Ω

*V_{BB} (pin 15) = GND, V_{CC} (pin 3) = 1.32 V, V_{EE} (pin 10) = −3.2 V. Input and output terminals are open except as specified in these tables and in the d-c test figures.

NOTES: 6. The algebraic convention where the most-positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more-negative voltages.

7. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Z. C_{in} = Q/V. When a terminal is an input to more than one gate, multiply the value given by the number of gates to which this terminal is an input.

8. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

TABLE II—INITIAL CONDITIONS

Several of the parameters require the application of conditions which cause the outputs to assume definite states prior to applying test conditions specified above.

SYMBOL	DESCRIPTION	INPUT TERMINALS* 0.5 V	INPUT TERMINALS* −0.5 V
X	Irrelevant		
S	Set 1Q and 2Q high, $1\bar{Q}1$, $1\bar{Q}2$, $2\bar{Q}1$, and $2\bar{Q}2$ low	1, 9	16
R	Reset 1Q and 2Q low, $1\bar{Q}1$, $1\bar{Q}2$, $2\bar{Q}1$, and $2\bar{Q}2$ high	9, 16	1

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ECL2542 electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS*									MIN	TYP	MAX	UNIT
		TEST FIGURE	INITIAL CONDITIONS (SEE TABLE III)	VOLTAGE AT INPUT UNDER TEST	INPUT(S) UNDER TEST	OTHER INPUT TERMINALS 0.5 V	OTHER INPUT TERMINALS −0.5 V	OUTPUT TERMINAL $\overline{Q}$	T_A		(SEE NOTE 6)			
V_{IH}	High-level input voltage								0°C		150		720	mV
									25°C		150		720	
									75°C		150		720	
V_{IL}	Low-level input voltage								0°C		−1500		−150	mV
									25°C		−1500		−150	
									75°C		−1500		−150	
V_{OH}	High-level output voltage, register mode	4	X	−0.2 V	13	1, 16	4, 5, 12, 14	2	0°C		280			mV
					11	7, 8	4, 5, 9, 12	6						
					14	1, 16	4, 5, 12, 13	2						
					9	7, 8	4, 5, 11, 12	6						
					12	1, 16	4, 5, 13, 14	2	0°C		280			
					12	7, 8	4, 5, 9, 11	6	25°C		315			
					16	13, 14	1, 4, 5, 12	2	25°C					
					8	9, 11	4, 5, 7, 12	6	75°C					
					1	13, 14	4, 5, 12, 16	2						
					7	9, 11	4, 5, 8, 12	6						
					12	13, 14	1, 4, 5, 16	2						
					12	9, 11	4, 5, 7, 8	6						
V_{OL}	Low-level output voltage, register mode	4	X	0.2 V	13	1	4, 5, 12, 14, 16	2	0°C				−350	mV
					11	7	4, 5, 8, 9, 12	6						
				−0.2 V	14	1, 13	4, 5, 12, 16	2						
					9	7, 11	4, 5, 8, 12	6						
				−0.2 V	12	1, 13	4, 5, 14, 16	2	0°C					
					12	7, 11	4, 5, 8, 9	6	25°C					
				0.2 V	16	14	1, 4, 5, 12, 13	2	25°C				−315	
					8	9	4, 5, 7, 11, 12	6	75°C					
				−0.2 V	1	14, 16	4, 5, 12, 13	2						
					7	8, 9	4, 5, 11, 12	6						
				−0.2 V	12	14, 16	1, 4, 5, 13	2						
					12	8, 9	4, 5, 7, 11	6						
					14	1, 13	4, 5, 12, 16	2						
V_{OH}	High-level output voltage, storage mode	4	R	0.2 V	9	7, 11	4, 5, 8, 12	6	0°C		280	365		mV
					1	14, 16	4, 5, 12, 13	2	25°C		315	400	500	
					7	8, 9	4, 5, 11, 12	6	75°C			470	580	
					12		1, 4, 5, 13, 14, 16	2						
					12		4, 5, 7, 8, 9, 11	6						
V_{OL}	Low-level output voltage, storage mode	4	S	0.2 V	14	1	4, 5, 12, 13, 16	2						
					9	7	4, 5, 8, 11, 12	6	0°C		−505	−440		mV
					1	14	4, 5, 12, 13, 16	2	25°C		−490	−425	−350	
					7	9	4, 5, 8, 11, 12	6	75°C			−390	−315	
					12		1, 4, 5, 13, 14, 16	2						
					12		4, 5, 7, 8, 9, 11	6						
V_{OL}	Low-level output voltage, set mode	4	R	0.2 V	5	12	4	2	0°C				−350	mV
					5	12	4	6	25°C				−315	
									75°C					
V_{OH}	High-level output voltage, reset mode	4	S	0.2 V	4	12	5	2	0°C		280			mV
					4	12	5	6	25°C		315			
									75°C					

(Continued on page 13)

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ECL2542 electrical characteristics at specified free-air temperature (continued)

PARAMETER		TEST CONDITIONS*							MIN	TYP (SEE NOTE 6)	MAX	UNIT
		TEST FIGURE	INITIAL CONDITIONS (SEE TABLE III)	VOLTAGE AT INPUT UNDER TEST	INPUT(S) UNDER TEST	OTHER INPUT TERMINALS: 0.5 V	OTHER INPUT TERMINALS: −0.5 V	OUTPUT TERMINAL $\overline{Q}$	T_A			
I_{IH}	High level input current	5	X	0.5 V	8		1, 4, 5, 7, 9, 11, 12, 13, 14, 16		0°C		255	μA
					11		1, 4, 5, 7, 8, 9, 12, 13, 14, 16		25°C		235	
					12		1, 4, 5, 7, 8, 9, 11, 13, 14, 16		75°C		200	
					13		1, 4, 5, 7, 8, 9, 11, 12, 14, 16					
					16		1, 4, 5, 7, 8, 9, 11, 12, 13, 14					
					1		4, 5, 7, 8, 9, 11, 12, 13, 14, 16		0°C		510	μA
					4		1, 5, 7, 8, 9, 11, 12, 13, 14, 16		25°C		470	
					5		1, 4, 7, 8, 9, 11, 12, 13, 14, 16		75°C		400	
					7		1, 4, 5, 8, 9, 11, 12, 13, 14, 16					
					9		1, 4, 5, 7, 8, 11, 12, 13, 14, 16					
					14		1, 4, 5, 7, 8, 9, 11, 12, 13, 16					
I_{IL}	Low-level input current	6	X	0.5 V	All inputs in parallel at −3.2 V				0°C		−0.9	μA
									25°C		−1.2	
									75°C		−1.7	
I_{CC} or $-I_{EE}$	Supply current	7	X	0.5 V	All inputs in parallel at −0.5 V				25°C	81	165	mA
C_{in}	Input capacitance (see Note 7)		X		Each				25°C		5	pF
Z_{out}	Output impedance (see Note 8)		X					2, 6	25°C		5	Ω

*V_{BB} (pin 15) = GND, V_{CC} (pin 3) = −1.3 V, V_{EE} (pin 10) = −3.2 V. Input and output terminals are open except as specified in these tables and in the d-c test figures.

NOTES: 6. The algebraic convention where the most-positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more-negative voltages.

7. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. $C_{in} = Q/V$. When a terminal is an input to more than one gate, multiply the value given by the number of gates to which this terminal is an input.

8. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

TABLE III—INITIAL CONDITIONS

Several of the parameters require the application of conditions which cause the outputs to assume definite states prior to applying test conditions specified above.

SYMBOL	DESCRIPTION	INPUT TERMINALS* 0.5 V	INPUT TERMINALS* −0.5 V
X	Irrelevant		
S	Set 1$\overline{Q}$ and 2$\overline{Q}$ low	5, 12	4
R	Reset 1$\overline{Q}$ and 2$\overline{Q}$ high	4, 12	5

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operating characteristics at specified free-air temperature

MODE	C_L	t_{PHL} and/or t_{PLH} PROPAGATION TIMES—ns									t_{THL} and/or t_{TLH} TRANSITION TIMES—ns								
		T_A = 0°C			T_A = 25°C			T_A = 75°C			T_A = 0°C			T_A = 25°C			T_A = 75°C		
	pF	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
ECL2540 (see Figure 2 and Table IV)																			
Register	4		2.5		1.6	2.4	3.5		2.5			3.8		2	3.7	5.2		3.9	
	50		3.6		2.4	3.6	4.5		3.6			4.7		2.5	4.6	6.7		4.4	
ECL2541 (see Figure 3 and Table V)																			
Register (Clock Controlled)	4		6.3		4.2	6.2	7.7		6.5			4.6		2	4.7	6.9		4.7	
	50		7.7		5.5	7.8	10.8		8.0			5.9		2.7	5.8	8.6		5.5	
Register (Gate Controlled)	4		4.3		2.3	4.2	5.8		4.3			4.6		2.3	4.6	6.5		4.6	
	50		5.6		3.4	5.7	8.5		5.7			5.6		2.7	5.4	7.8		5.1	
Set	4		2.7		1.9	2.7	3.5		2.8			4.5		2.9	4.5	6		4.6	
	50		3.8		2.7	3.8	4.7		3.8			4.7		2.7	4.6	7		4.5	
Reset	4		3.8		2.3	3.8	5.8		4.1			4.4		2.3	4.3	6.5		4.6	
	50		6.0		3.4	5.9	8.5		6.0			7.1		4.6	7.0	8.6		6.4	
ECL2542 (see Figure 3 and Table VI)																			
Register (Clock Controlled)	4		7.0		5.5	7.0	8.1		7.1			4.6		3	4.5	5.7		4.5	
	50		8.2		6.7	8.1	9.4		8.3			4.8		3	4.8	6.9		4.7	
Register (Gate Controlled)	4		4.5		3.3	4.4	5.7		4.4			4.2		3	4.1	5.7		4.1	
	50		5.7		4.5	5.6	6.8		5.5			4.7		3	4.7	6.9		4.6	
Set	4		2.9		1.7	2.7	3.1		2.6			4.6		3	4.5	5.7		4.6	
	50		4.0		3.2	4.0	4.7		3.9			5.4		4	5.6	6.9		5.5	
Reset	4		4.4		3.3	4.3	5.8		4.6			4.2		3	4.2	5.7		4.4	
	50		5.4		4.5	5.4	6.8		5.4			3.9		3	4.0	5		4.0	

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PARAMETER MEASUREMENT INFORMATION

TABLE IV—ECL2540

INPUT TERMINALS		OUTPUT UNDER TEST		PARAMETER MEASURED
DATA GENERATOR	−0.5 V			
14	12	2	Q	t_{PLH}, t_{TLH}, t_{PHL}, and t_{THL}
14	12	1	$\overline{Q}$	
12	14	7	Q	
12	14	8	$\overline{Q}$	

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PARAMETER MEASUREMENT INFORMATION

TABLE V—ECL2541

MODE	INPUT TERMINAL CONDITIONS				OUTPUT UNDER TEST	WAVEFORM	PARAMETER MEASURED
	PULSE GENERATOR NO. 1	PULSE GENERATOR NO. 2	0.5 V	−0.5 V			
REGISTER (Clock Controlled)	16	9	11	1, 12	8	LH	t_{PLH}, t_{TLH}
	1			11, 12, 16	8	HL	t_{PHL}, t_{THL}
	1			11, 12, 16	2, 4	LH	t_{PLH}, t_{TLH}
	16		11	1, 12	2, 4	HL	t_{PHL}, t_{THL}
	16	9	13	1, 14	7	LH	t_{PLH}, t_{TLH}
	1			13, 14, 16	7	HL	t_{PHL}, t_{THL}
	1			13, 14, 16	5, 6	LH	t_{PLH}, t_{TLH}
	16		13	1, 14	5, 6	HL	t_{PHL}, t_{THL}
REGISTER (Gate Controlled)	16	12	11	1, 9	8	LH	t_{PLH}, t_{TLH}
	1			9, 11, 16	8	HL	t_{PHL}, t_{THL}
	1			9, 11, 16	2, 4	LH	t_{PLH}, t_{TLH}
	16		11	1, 9	2, 4	HL	t_{PHL}, t_{THL}
	16	14	13	1, 9	7	LH	t_{PLH}, t_{TLH}
	1			9, 13, 16	7	HL	t_{PHL}, t_{THL}
	1			9, 13, 16	5, 6	LH	t_{PLH}, t_{TLH}
	16		13	1, 9	5, 6	HL	t_{PHL}, t_{THL}
SET TIME	16	1	9	All other input terminals open	8	LH	t_{PLH}, t_{TLH}
					2, 4	HL	t_{PHL}, t_{THL}
					7	LH	t_{PLH}, t_{TLH}
					5, 6	HL	t_{PHL}, t_{THL}
RESET TIME	1	16	9		2, 4	LH	t_{PLH}, t_{TLH}
					8	HL	t_{PHL}, t_{THL}
					5, 6	LH	t_{PLH}, t_{TLH}
					7	HL	t_{PHL}, t_{THL}

TABLE VI—ECL2542

MODE	INPUT TERMINAL CONDITIONS				OUTPUT UNDER TEST	WAVEFORM	PARAMETER MEASURED
	PULSE GENERATOR NO. 1	PULSE GENERATOR NO. 2	0.5 V	−0.5 V			
REGISTER (Clock Controlled)	5	12	1, 16	4, 13, 14	2	LH	t_{PLH}, t_{TLH}
			13, 14	1, 4, 16		LH	t_{PLH}, t_{TLH}
	4		1, 13, 16	5, 14		HL	t_{PHL}, t_{THL}
			13, 14, 16	1, 5		HL	t_{PHL}, t_{THL}
	5	12	7, 8	4, 9, 11	6	LH	t_{PLH}, t_{TLH}
			9, 11	4, 7, 8		LH	t_{PLH}, t_{TLH}
	4		7, 8, 11	5, 9		HL	t_{PHL}, t_{THL}
			8, 9, 11	5, 7		HL	t_{PHL}, t_{THL}
REGISTER (Gate Controlled)	5	14	1, 16	4, 12, 13	2	LH	t_{PLH}, t_{TLH}
		1	13, 14	4, 12, 16		LH	t_{PLH}, t_{TLH}
	4	14	1, 13, 16	5, 12		HL	t_{PHL}, t_{THL}
		1	13, 14, 16	5, 12		HL	t_{PHL}, t_{THL}
	5	9	7, 8	4, 11, 12	6	LH	t_{PLH}, t_{TLH}
		7	9, 11	4, 8, 12		LH	t_{PLH}, t_{TLH}
	4	9	7, 8, 11	5, 12		HL	t_{PHL}, t_{THL}
		7	8, 9, 11	5, 12		HL	t_{PHL}, t_{THL}
SET TIME	4	5	12	All other input terminals open	2, 6	HL	t_{PHL}, t_{THL}
RESET TIME	5	4	12		2, 6	LH	t_{PLH}, t_{TLH}

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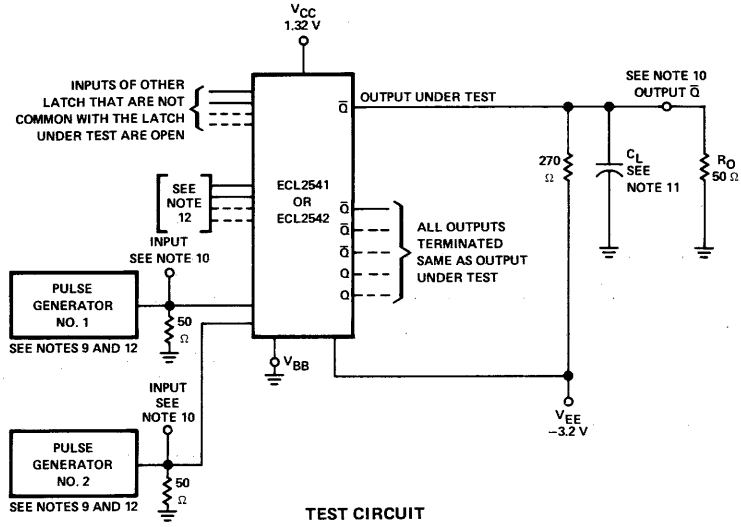
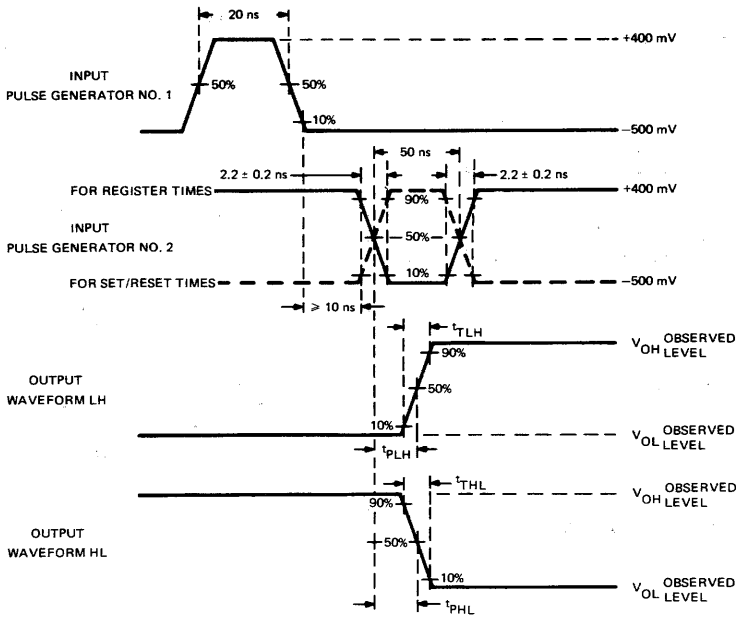
PARAMETER MEASUREMENT INFORMATION
ECL2541 AND ECL2542



TEST CIRCUIT

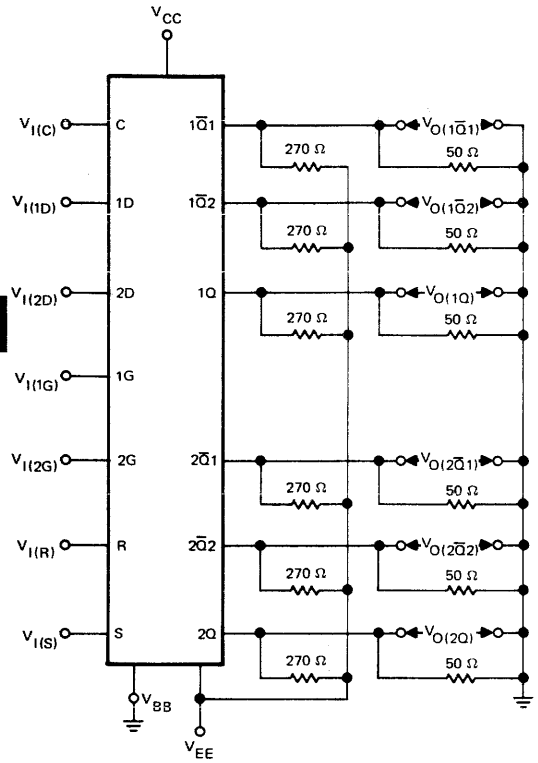


VOLTAGE WAVEFORMS

FIGURE 3—ECL2541 AND ECL2542 PROPAGATION DELAY AND TRANSITION TIMES

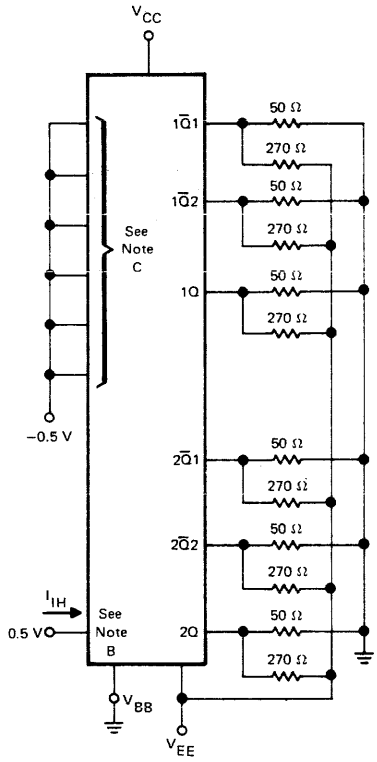
NOTES:
9. Each generator has a 50-Ω output impedance.
10. The waveforms are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. Either a high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF, or a 50-Ω impedance system can be used. The 50-Ω resistor designated R_O is the oscilloscope input resistance in the 50-Ω system or a discrete resistor with a high-impedance probe.
11. C_L includes probe and fixture capacitance. A capacitance of 50 pF can be used to approximate an a-c fan-out of 10.
12. See Table V (ECL2541) or Table VI (ECL2542) for voltages to be applied to input terminals for each test.

PARAMETER MEASUREMENT INFORMATION†
ECL2541
(See Note 13)



V_I is applied to each input as specified in the electrical characteristics table.

FIGURE 4–V_{OH} AND V_{OL}



A. Each input is tested separately.
B. Any one of the following seven inputs: C, 1D, 1G, 2D, 2G, R, and S.
C. Other six inputs listed in note B that are not under test.

FIGURE 5–I_{IH}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.
NOTE 13: ECL2540 and ECL2542 are tested in a manner similar to that shown for ECL2541.

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PARAMETER MEASUREMENT INFORMATION†
ECL2541
(See Note 13)

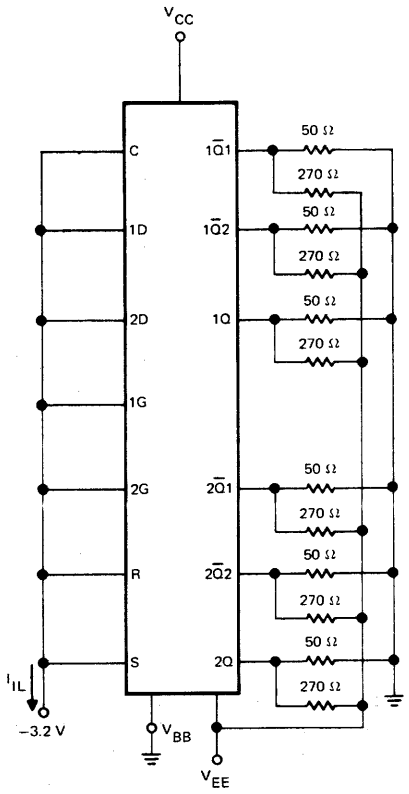


FIGURE 6–I_{IL}

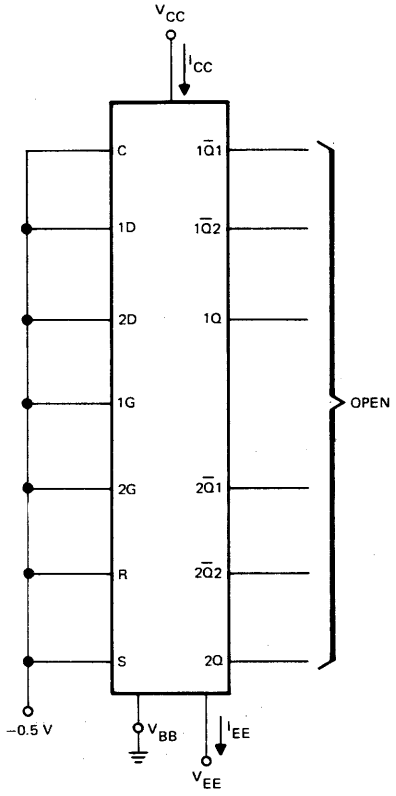


FIGURE 7–I_{CC} OR I_{EE}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

NOTE 13: ECL2540 and ECL2542 are tested in a manner similar to that shown for ECL2541.

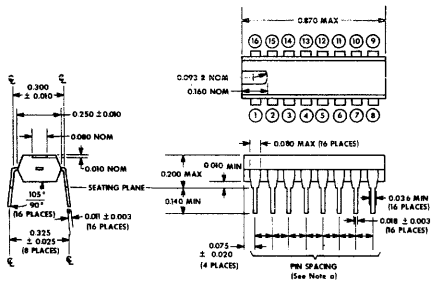
TYPES ECL2540 THRU ECL2542
EMITTER-COUPLED-LOGIC BISTABLE MODULES

mechanical data

The circuit bars are mounted on a 16-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

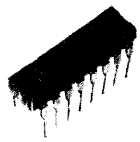
The plastic case is electrically nonconductive.

16-PIN PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



NOTES: a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within 0.010 of its true longitudinal position relative to pins 1 and 16.

b. All dimensions are in inches unless otherwise noted.



terminal designations

Pin assignments are shown in the table below and correspond to the logic diagrams on pages 2 and 3. Outputs are denoted by 1Q, $1\overline{Q}$, 2Q, $2\overline{Q}$, 1Q1, $1\overline{Q}2$, $2\overline{Q}1$, and $2\overline{Q}2$. Inputs are denoted by C, C', 1D, 2D, 1D1, 1D2, 2D1, 2D2, 1G, 2G, 1G1, 1G2, 2G1, 2G2, S and R. The number preceding the letter denotes whether the input (or output) is part of the first or second latch. The number (if any) following the letter distinguishes inputs (or outputs) of the same latch from each other.

Power is supplied via the V_{CC}, V_{EE}, and V_{BB} terminals.

V_{BB} is a reference voltage.

NC indicates no internal connection.

PIN ASSIGNMENTS

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ECL2540	$1\overline{Q}$	1Q	V_{CC}	NC	NC	V_{CC}	2Q	$2\overline{Q}$	NC	V_{EE}	C'	2D	C	1D	V_{BB}	NC
ECL2541	S	$1\overline{Q}1$	V_{CC}	$1\overline{Q}2$	$2\overline{Q}1$	$2\overline{Q}2$	2Q	1Q	C	V_{EE}	1D	1G	2D	2G	V_{BB}	R
ECL2542	1G1	$1\overline{Q}$	V_{CC}	R	S	$2\overline{Q}$	2G1	2D1	2G2	V_{EE}	2D2	C	1D2	1G2	V_{BB}	1D1

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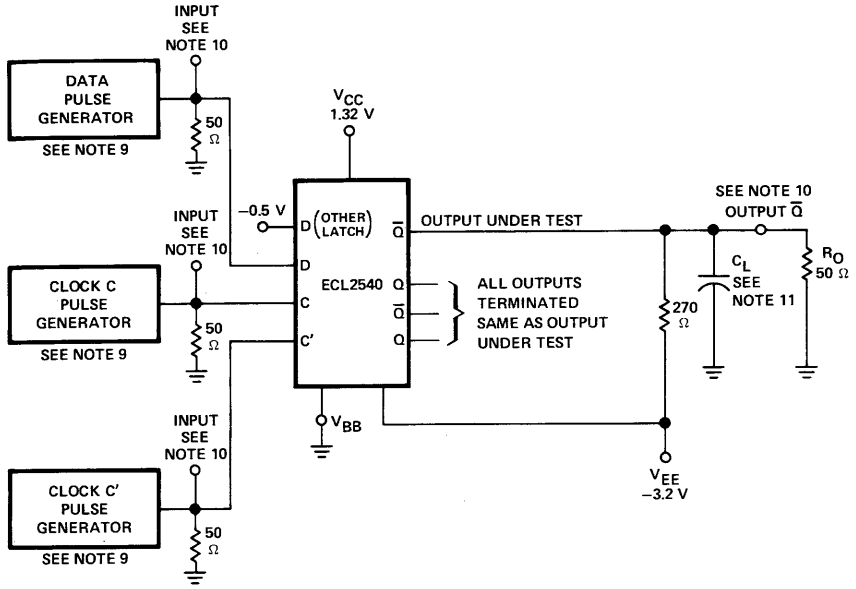
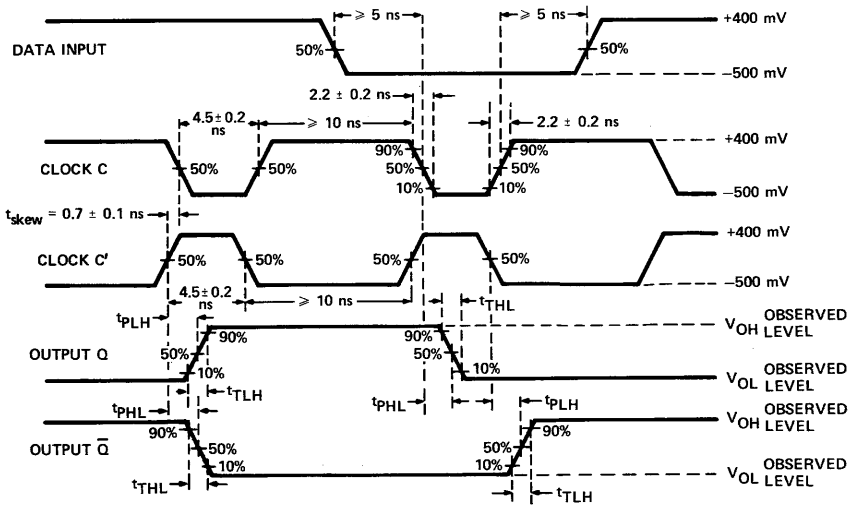
PARAMETER MEASUREMENT INFORMATION
ECL2540



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 2–ECL2540 PROPAGATION DELAY AND TRANSITION TIMES (WITH SKEW)

NOTES:
9. Each generator has a 50-Ω output impedance.
10. The waveforms are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. Either a high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF, or a 50-Ω impedance system can be used. The 50-Ω resistor designated R_O is the oscilloscope input resistance in the 50-Ω system or a discrete resistor with a high-impedance probe.
11. C_L includes probe and fixture capacitance. A capacitance of 50 pF can be used to approximate an a-c fan-out of 10.