3

Linear Circuits

INDEX

FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*					SEC.-PAGE
	−55°C to 125°C	0°C to 70°C	Dual-In-Line			Plug-In	Flat	
OPERATIONAL AMPLIFIERS								
General Purpose Operational Amplifiers	SN52702A			N		L	S	3-18
	SN52702	SN72702		N		L	S	3-18
High-Performance Operational Amplifiers	SN52101A	SN72301A	J	N	P	L	Z	3-5
	SN52107	SN72307	J	N	P	L	Z	3-9
	SN52709A			N	P	L	S	3-27
	SN52709	SN72709		N	P	L	S	3-27
	SN52741	SN72741	J	N	P	L	Z	3-34
	SN52748	SN72748	J	N	P	L	Z	3-43
	SN52770	SN72770	J	N	P	L	Z	3-47
	SN52771	SN72771	J	N	P	L	Z	3-53
Dual High-Performance Operational Amplifiers	SN52558	SN72558			P	L		3-13
	SN52747	SN72747	J	N				3-39
DIFFERENTIAL COMPARATORS								
Differential Comparators	SN52710	SN72710	J	N		L	S	3-68
	SN52810	SN72810	J	N	P	L	Z	3-79
Differential Comparators with Strobes	SN52510	SN72510	J	N	P	L	Z	3-60
Dual-Channel Differential Comparators with Strobes	SN52711	SN72711	J	N		L	S	3-72
	SN52811	SN72811	J	N		L		3-85
Dual Differential Comparators		SN72720		N				3-77
	SN52820	SN72820	J	N				3-91
Dual Differential Comparators with Strobes	SN52514	SN72514	J	N				3-66
VIDEO AMPLIFIERS								
Differential Video Amplifiers	SN52733	SN72733		N		L		3-94
	SN5510					L	F	3-101
		SN7510				L	F	3-108
	SN5511	SN7511		N		L	F	3-115
	SM5512	SM7512				L		3-121
	SN5514	SN7514				L		3-121
LINE CIRCUITS								
Dual Line Drivers	SN55109		J					3-130
		SN75109	J	N				3-130
	SN55110		J					3-130
		SN75110	J	N				3-130
Dual Line Receivers	SN55107A		J					3-130
		SN75107A	J	N				3-130
	SN55108A		J					3-130
		SN75108A	J	N				3-130
		SN75150	J	N	P			3-149
Dual Differential Line Receiver		SN75100L				L		3-126
Quadruple Line Receiver		SN75154	J	N				3-153

*For outline drawings of all packages, see Section 1.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*					SEC.-PAGE
	−55°C to 125°C	0°C to 70°C	Dual-In-Line		Plug-In		Flat	
SENSE AMPLIFIERS								
Dual-Channel Sense Amplifiers		SN7522	J	N				3-166
		SN7523	J	N				3-166
Dual-Channel Sense Amplifiers with Complementary Outputs		SN7520	J	N				3-164
		SN7521	J	N				3-164
Dual-Channel Sense Amplifiers with Output Registers		SN7526	J	N				3-172
		SN7527	J	N				3-172
Dual Sense Amplifiers		SN7524	J	N				3-170
		SN7525	J	N				3-170
		SN75234	J	N				3-176
		SN75235	J	N				3-176
Dual Sense Amplifiers with Preamplifier Test Points		SN7528	J	N				3-174
		SN7529	J	N				3-174
		SN75238	J	N				3-178
		SN75239	J	N				3-178
MEMORY AND PERIPHERAL DRIVERS								
2 X 4 Transistor Arrays		SN75303		N			S	3-212
		SN75308	J	N				3-217
Memory Driver		SN75325						3-230
Memory Driver with Decode Inputs		SN75324						3-222
Dual Peripheral Drivers		SN75450A		N				3-247
		SN75451A			P			3-249
		SN75452		P	P			3-250
		SN75453			P			3-251
		SN75454			P			3-252
Diode Arrays	TID21A Series			N			F	3-264
VOLTAGE REGULATOR								
Voltage Regulator		SN72400		N		L		3-270
COMMUNICATIONS CIRCUITS								
Logarithmic Amplifiers	SN56502	SN76502	J	N				3-277
Balanced Mixers	SN56514	SN76514	J	N		L		3-284
CONSUMER CIRCUITS								
Consumer Circuits Summary								3-289
Stereo Demodulator		SN76110		N				3-290

*For outline drawings of all packages, see Section 1.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

OPERATIONAL AMPLIFIER SELECTION GUIDE

Series 52

TYPE	SN52702	SN52709	SN52741	SN52747	SN52748	SN52770	SN52771	SN52558	SN52101A	SN52107	
FEATURES	Wide BW, General Purpose	General Purpose	Internally Compensated Gen. Pur.	Dual SN52741	Extended BW, Gen. Pur.	Super β	Super β	Dual 741 in 8-pin Package	Precision Op Amp	Internally Compensated	UNIT
Input Offset Voltage, Max	5	5	5	5	5	4	4	5	2	2	mV
Input Offset Current, Max	500	200	200	200	200	2	2	200	10	10	nA
Temperature Coefficient of Input Offset Voltage, Typ	10	6	7	7	7	10	10	7	3	3	μV/°C
Input Bias Current, Max	10,000	500	500	500	500	15	15	500	75	75	nA
Voltage Amplification, Min	1.4	25	50	50	50	50	50	50	50	50	V/mV
Slew Rate at Unity Gain, Typ	1.7	0.3	0.5	0.5	0.5	2.5	2.5	0.5	0.5	0.5	V/μs
Unity-Gain Bandwidth, Typ	30	5	1	1	1	1.3	1.3	1	1	1	MHz
Min Supply Voltage	+6, −3	±9	±5	±5	±5	±3	±3	±5	±3	±3	V
Max Supply Voltage	+14, −7	±18	±22	±22	±22	±22	±22	±22	±22	±22	V
Input Voltage Range, Min	0.5 to −4	±8	±12	±12	±12	±12	±12	±12	±15	±15	V
Differential Input Voltage Rating	±5	±5	±30	±30	±30	±30	±30	±30	±30	±30	V
Internal Compensation	No	No	Yes	Yes	No	No	Yes	Yes	No	Yes	
Offset Adjust	No	No	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	
Input Protection	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
Output Protection	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	

3

Series 72

TYPE	SN72702	SN72709	SN72741	SN72747	SN72748	SN72770	SN72771	SN72558	SN72301A	SN72307	
FEATURES	Wide BW, General Purpose	General Purpose	Internally Compensated, Gen. Pur.	Dual SN72741	Extended BW, Gen. Pur.	Super β	Super β	Dual 741 in 8-pin Package	Precision Op Amp	Internally Compensated	UNIT
Input Offset Voltage, Max	5	7.5	6	6	6	10	10	6	7.5	7.5	mV
Input Offset Current, Max	500	500	200	200	200	10	10	200	50	50	nA
Temperature Coefficient of Input Offset Voltage, Typ	5	6	7	7	7	10	10	7	6	6	μV/°C
Input Bias Current, Max	15,000	1500	500	500	500	30	30	500	250	250	nA
Voltage Amplification, Min	1	15	20	20	20	35	35	20	25	25	V/mV
Slew Rate at Unity Gain, Typ	1.7	0.3	0.5	0.5	0.5	2.5	2.5	0.5	0.5	0.5	V/μs
Unity-Gain Bandwidth, Typ	30	5	1	1	1	1.3	1.3	1	1	1	MHz
Min Supply Voltage	+6, −3	±9	±5	±5	±5	±3	±3	±5	±3	±3	V
Max Supply Voltage	+14, −7	±18	±18	±18	±18	±18	±18	±18	±18	±18	V
Input Voltage Range, Min	0.5 to −4	±8	±12	±12	±12	±11	±11	±12	±12	±12	V
Differential Input Voltage Rating	±5	±5	±30	±30	±30	±30	±30	±30	±30	±30	V
Internal Compensation	No	No	Yes	Yes	No	No	Yes	Yes	No	Yes	
Offset Adjust	No	No	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	
Input Protection	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
Output Protection	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	

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CIRCUIT TYPES SN52101A, SN72301A
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

- Low Input Currents
- Low Input Offset Parameters
- Frequency and Transient Response Characteristics Adjustable
- Short-Circuit Protection
- Offset-Voltage Null Capability
- Designed to be Interchangeable with National Semiconductor LM101A and LM301A
- No Latch-Up
- Large Common-Mode and Differential Voltage Ranges
- Same Pin Assignments as SN52709 and SN72709

description

The SN52101A and SN727301A are high-performance operational amplifiers, featuring very low input bias current and input offset voltage and current to improve the accuracy of high-impedance circuits using these devices.

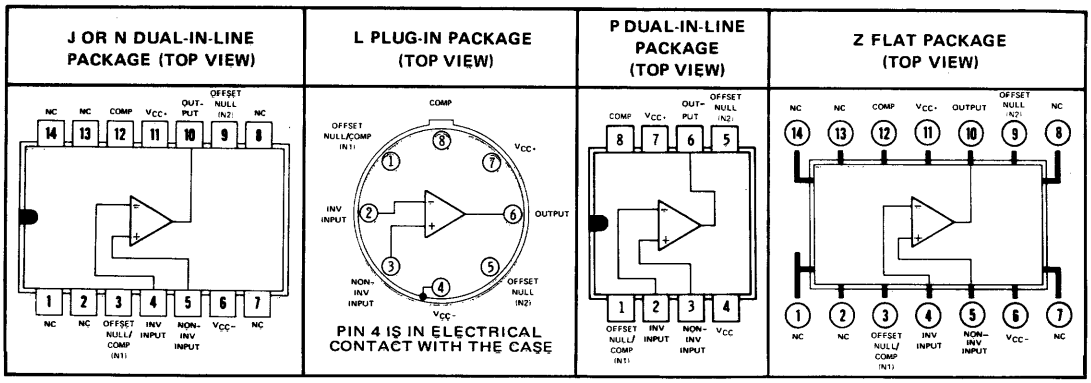
The high common-mode input voltage range and the absence of latch-up make the SN52101A and SN72301A ideal for voltage-follower applications. The devices are protected to withstand short-circuits at the output. The external compensation of the SN52101A and the SN72301A allows the changing of the frequency response (when the closed-loop gain is greater than unity) for applications requiring wider bandwidth or higher slew rate.

A potentiometer may be connected between the offset-null inputs (N1 and N2), as shown in Figure 8, to null out the offset voltage.

The SN52101A is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72301A is characterized for operation from 0°C to 70°C.

3

terminal assignments



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52101A	SN72301A	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		−0.5 to 2	−0.5 to 2	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total power dissipation at (or below) 55°C free-air temperature (see Note 5)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, L, or Z Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P Package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the SN52101A only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 55°C free-air temperature, refer to Dissipation Derating Curve, Figure 1.

TEXAS INSTRUMENTS
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voltages specified

Throughout this data sheet, supply voltages are specified either as a range or as a specific value. A positive voltage within the specified range (or of the specified value) is applied to V_{CC+}, and an equal negative voltage is applied to V_{CC-}.

electrical characteristics at specified free-air temperature (see note 6)

PARAMETER		TEST CONDITIONS†		SN52101A			SN72301A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50 kΩ	25°C		0.6	2		2.0	7.5	mV
			Full range			3			10	
α_{VIO}	Average temperature coefficient of input offset voltage		Full range		3	15		6	30	μV/°C
I_{IO}	Input offset current		25°C		1.5	10		3	50	nA
			Full range			20			70	
α_{IIO}	Average temperature coefficient of input offset current	T_A = −55°C to 25°C			0.02	0.2				nA/°C
		T_A = 25°C to 125°C			0.01	0.1				
		T_A = 0°C to 25°C						0.02	0.6	
		T_A = 25°C to 70°C						0.01	0.3	
I_{IB}	Input bias current		25°C		30	75		70	250	nA
			Full range			100			300	
V_I	Input voltage range	See Note 7	Full range	±15			±12			V
V_{OPP}	Maximum peak-to-peak output voltage swing	$V_{CC\pm}$ = ±15 V, R_L = 10 kΩ	25°C	24	28		24	28		V
			Full range	24			24			
		$V_{CC\pm}$ = ±15 V, R_L = 2 kΩ	25°C	20	26		20	26		
			Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±15 V, V_O = ±10 V, $R_L \geq$ 2 kΩ	25°C	50,000	200,000		25,000	200,000		
			Full range	25,000			15,000			
r_i	Input resistance		25°C	1.5	4		0.5	2		MΩ
CMRR	Common-mode rejection ratio	R_S = 50 kΩ	25°C	80	98		70	90		dB
			Full range	80			70			
$\Delta V_{CC}/\Delta V_{IO}$	Power supply rejection ratio	R_S = 50 kΩ	25°C	80	98		70	96		dB
			Full range	80			70			
I_{CC}	Supply current	No load, No signal, See Note 7	25°C		1.8	3		1.8	3	mA
			125°C		1.2	2.5				

†All characteristics are specified under open-loop operation. Full range for SN52101A is −55°C to 125°C and for SN72301A is 0°C to 70°C.

NOTES: 6. Unless otherwise noted, $V_{CC\pm}$ = ±5 V to ±20 V for SN52101A and $V_{CC\pm}$ = ±5 V to ±15 V for SN72301A. All typical values are at $V_{CC\pm}$ = ±15 V.
7. For SN52101A, $V_{CC\pm}$ = ±20 V. For SN72301A, $V_{CC\pm}$ = ±15 V.

For ordering instructions and mechanical data, see the SN52741/SN72741 data sheet dated November 1970.

TEXAS INSTRUMENTS
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DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to zero. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO}) The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left| \frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at zero volts.

Average Temperature Coefficient Of Input Offset Current (α_{IIO}) The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{IIO} = \left| \frac{(I_{IO} @ T_{A(1)}) - (I_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at zero volts.

Input Voltage Range (V_I) The range of voltage which, if exceeded at either input terminal, will cause the amplifier to cease functioning properly.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage which can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the peak-to-peak output voltage swing to the change in differential input voltage required to drive the output.

Input Resistance (r_i) The resistance between the input terminals with either input grounded.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Supply Voltage Rejection Ratio ($\Delta V_{CC}/\Delta V_{IO}$) The ratio of the change in power supply voltages to the change in input offset voltage. For these devices, both supply voltages are varied symmetrically.

THERMAL INFORMATION

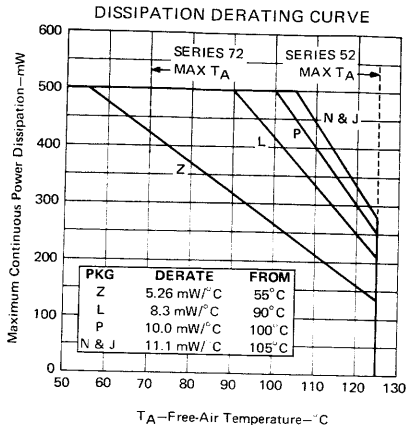


FIGURE 1

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

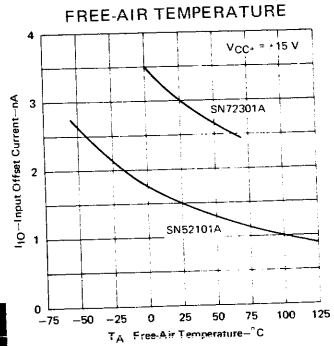


FIGURE 2

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

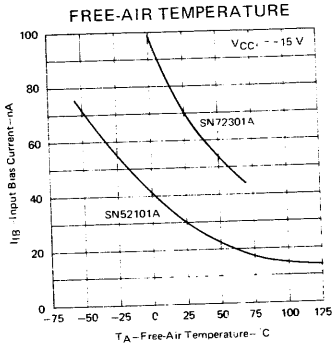


FIGURE 3

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE (WITH
SINGLE-POLE COMPENSATION)
vs FREQUENCY

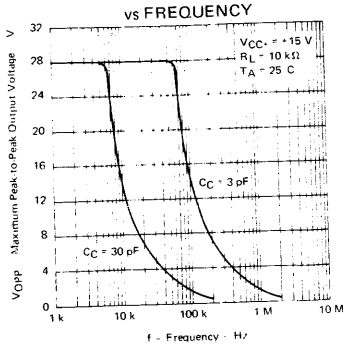


FIGURE 4

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

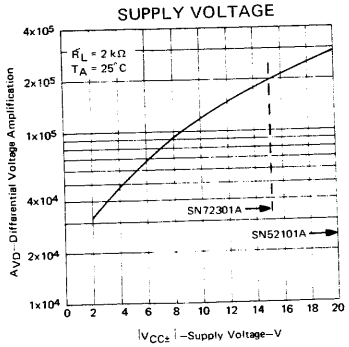


FIGURE 5

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY

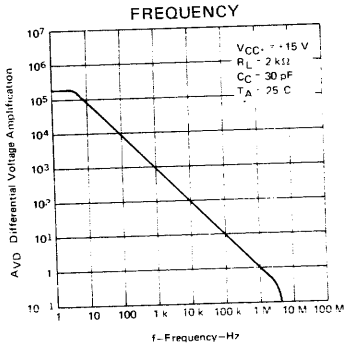


FIGURE 6

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

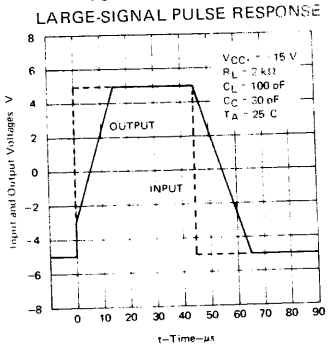
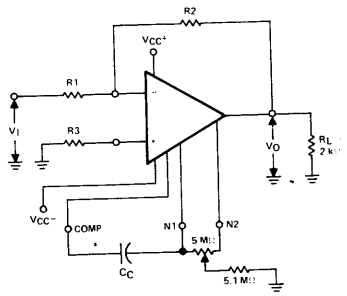


FIGURE 7

TYPICAL APPLICATION DATA



$$\frac{V_O}{V_I} = -\frac{R2}{R1}$$

$$C_C \geq \frac{R1 \cdot 30\ pF}{R1+R2}$$

$$R3 = \frac{R1 \cdot R2}{R1+R2}$$

FIGURE 8 – INVERTING CIRCUIT WITH ADJUSTABLE GAIN, SINGLE-POLE COMPENSATION, AND OFFSET ADJUSTMENT

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CIRCUIT TYPES SN52107, SN72307
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

- Low Input Currents
- No Frequency Compensation Required
- Offset-Voltage Null Capability
- Low Input Offset Parameters
- Designed to be Interchangeable with National Semiconductor LM107 and LM307
- Short-Circuit Protection
- No Latch-Up
- Large Common-Mode and Differential Voltage Ranges
- Same Pin Assignments as SN52741 and SN72741

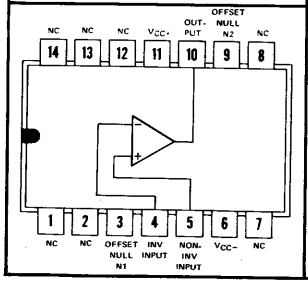
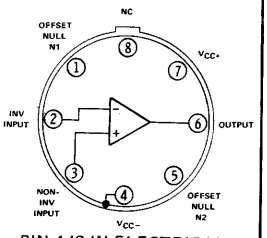
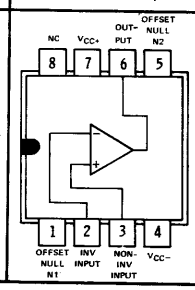
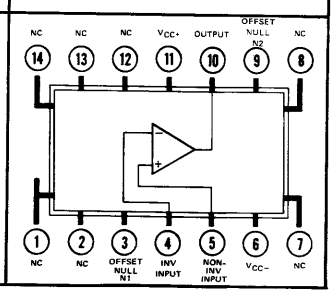
description

The SN52107 and SN72307 are high-performance operational amplifiers, featuring very low input bias current and input offset voltage and current to improve the accuracy of high-impedance circuits using these devices.

The high common-mode input voltage range and the absence of latch-up make the SN52107 and SN72307 ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components. A low-value potentiometer may be connected between the offset-null inputs, as shown in Figure 2, to null out the offset voltage.

The SN52107 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72307 is characterized for operation from 0°C to 70°C.

terminal assignments

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)	L PLUG-IN PACKAGE (TOP VIEW)	P DUAL-IN-LINE PACKAGE (TOP VIEW)	Z FLAT PACKAGE (TOP VIEW)
			

NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52107	SN72307	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		±0.5	±0.5	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation at (or below) 55°C free-air temperature (see Note 5)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, L, or Z Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P Package	260	260	°C

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the SN52107 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 55°C free-air temperature, refer to Dissipation Derating Curve, Figure 1.

voltages specified

Throughout this data sheet, supply voltages are specified either as a range or as a specific value. A positive voltage within the specified range (or of the specified value) is applied to V_{CC+}, and an equal negative voltage is applied to V_{CC-}.

electrical characteristics at specified free-air temperature (see note 6)

PARAMETER		TEST CONDITIONS†		SN52107			SN72307			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50 kΩ	25°C		0.6	2		2	7.5	mV
			Full range			3			10	
α_{VIO}	Average temperature coefficient of input offset voltage		Full range		3	15		6	30	μV/°C
I_{IO}	Input offset current		25°C		1.5	10		3	50	nA
			Full range			20			70	
α_{IIO}	Average temperature coefficient of input offset current	T_A = −55°C to 25°C			0.02	0.2				nA/°C
		T_A = 25°C to 125°C			0.01	0.1				
		T_A = 0°C to 25°C						0.02	0.6	
		T_A = 25°C to 70°C						0.01	0.3	
I_{IB}	Input bias current		25°C		30	75		70	250	nA
			Full range			100			300	
V_I	Input voltage range	See Note 7	Full range	±15			±12			V
V_{OPP}	Maximum peak-to-peak output voltage swing	$V_{CC\pm}$ = ±15 V, R_L = 10 kΩ	25°C	24	28		24	28		V
			Full range	24			24			
		$V_{CC\pm}$ = ±15 V, R_L = 2 kΩ	25°C	20	26		20	26		
			Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±15 V, V_O = ±10 V, $R_L \geq$ 2 kΩ	25°C	50,000	200,000		25,000	200,000		
			Full range	25,000			15,000			
r_i	Input resistance		25°C	1.5	4		0.5	2		MΩ
CMRR	Common-mode rejection ratio	R_S = 50 kΩ	25°C	80	98		70	90		dB
			Full range	80			70			
$\Delta V_{CC}/\Delta V_{IO}$	Power supply rejection ratio	R_S = 50 kΩ	25°C	80	98		70	96		dB
			Full range	80			70			
I_{CC}	Supply current	No load, No signal, See Note 7	25°C		1.8	3		1.8	3	mA
			125°C		1.2	2.5				

† All characteristics are specified under open-loop operation. Full range for SN52107 is −55°C to 125°C and for SN72307 is 0°C to 70°C.

NOTES: 6. Unless otherwise noted $V_{CC\pm}$ = ±5 V to ±20 V for SN52107 and $V_{CC\pm}$ = ±5 V to ±15 V for SN72307. All typical values are at $V_{CC\pm}$ = ±15 V.
7. For SN52107, $V_{CC\pm}$ = ±20 V. For SN72307, $V_{CC\pm}$ = ±15 V.

For ordering instructions and mechanical data, see the SN52741/SN72741 data sheet dated November 1970.

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DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to zero. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO}) The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left| \frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right| \quad \text{where } T_{A(1)} \text{ and } T_{A(2)} \text{ are the specified temperature extremes.}$$

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at zero volts.

Average Temperature Coefficient Of Input Offset Current (α_{IIO}) The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{IIO} = \left| \frac{(I_{IO} @ T_{A(1)}) - (I_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right| \quad \text{where } T_{A(1)} \text{ and } T_{A(2)} \text{ are the specified temperature extremes.}$$

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at zero volts.

Input Voltage Range (V_I) The range of voltage which, if exceeded at either input terminal, will cause the amplifier to cease functioning properly.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage which can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the peak-to-peak output voltage swing to the change in differential input voltage required to drive the output.

Input Resistance (r_i) The resistance between the input terminals with either input grounded.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Supply Voltage Rejection Ratio ($\Delta V_{CC}/\Delta V_{IO}$) The ratio of the change in power supply voltages to the change in input offset voltage. For these devices, both supply voltages are varied symmetrically.

3

THERMAL INFORMATION

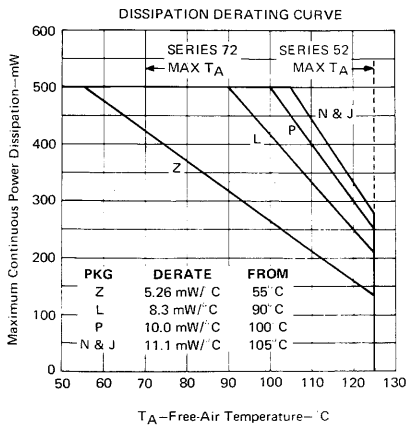

FIGURE 1

TYPICAL APPLICATION DATA

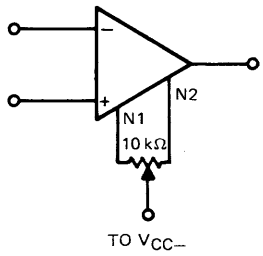

FIGURE 2—INPUT OFFSET VOLTAGE NULL CIRCUIT

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

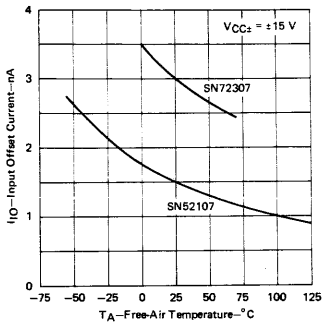

FIGURE 3

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

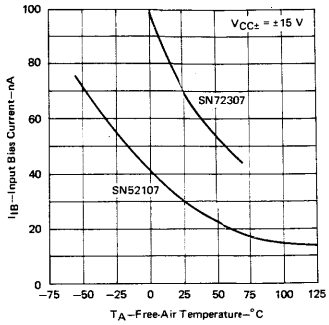

FIGURE 4

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

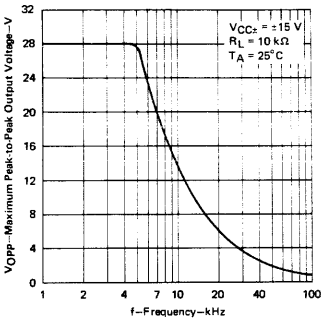

FIGURE 5

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

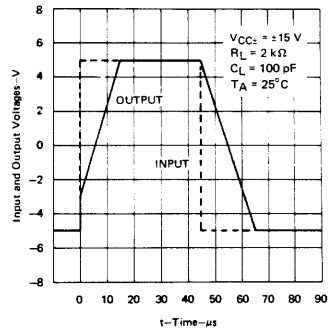

FIGURE 6

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

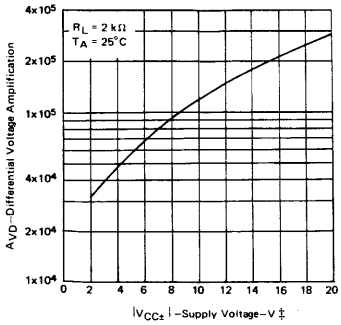

FIGURE 7

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY

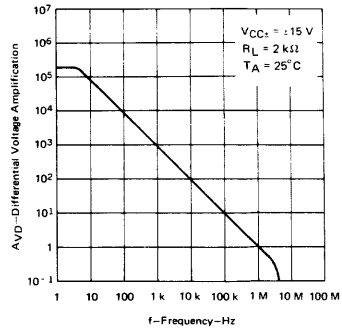

FIGURE 8

‡ Data for supply voltages greater than 15 V is applicable to SN52107 circuits only.

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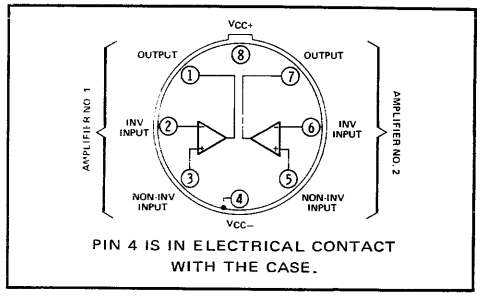
CIRCUIT TYPES SN52558, SN72558
DUAL HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

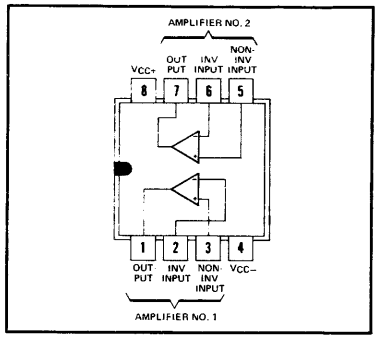
- Short-Circuit Protection
- Large Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-up
- Designed to be Interchangeable with Motorola MC1558/MC1458 and Signetics S5558/N5558

L PLUG-IN PACKAGE
(TOP VIEW)



PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE.

P DUAL-IN-LINE PACKAGE
(TOP VIEW)



3

description

The SN52558 and SN72558 are dual high-performance operational amplifiers with each half electrically similar to SN52741/SN72741 except that offset null capability is not provided.

The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensator ensures stability without external components.

The SN52558 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72558 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52558	SN72558	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation at (or below) 70°C free-air temperature (see Note 5)	Each amplifier	500	500	mW
	Total package	680	680	
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	L Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	P Package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the SN52558 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation of SN52558 above 70°C free-air temperature, refer to Dissipation Derating Curve, Figure 1.

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		SN52558			SN72558			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 10\ k\Omega$	25°C		1	5		1	6	mV
			Full range			6			7.5	
I_{IO}	Input offset current		25°C		20	200		20	200	nA
			Full range			500			300	
I_{IB}	Input bias current		25°C		80	500		80	500	nA
			Full range			1500			800	
V_I	Input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L = 10 kΩ	25°C	24	28		24	28		V
		$R_L \geq$ 10 kΩ	Full range	24			24			
		R_L = 2 kΩ	25°C	20	26		20	26		
		$R_L \geq$ 2 kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq$ 2 kΩ, V_O = ±10 V	25°C	50,000	200,000		20,000	200,000		
			Full range	25,000			15,000			
B_{OM}	Maximum-output-swing bandwidth (closed-loop)	R_L = 2 kΩ, $V_O \geq$ ±10 V, A_{VD} = 1, THD ≤ 5%	25°C		14			14		kHz
B_1	Unity-gain bandwidth		25°C		1			1		MHz
ϕ_m	Phase margin	A_{VD} = 1	25°C		65°			65°		
A_m	Gain margin		25°C		11			11		dB
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	V_O = 0, See Note 5	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
z_{ic}	Common-mode input impedance	f = 20 Hz	25°C		200			200		MΩ
CMRR	Common-mode rejection ratio	$R_S \leq 10\ k\Omega$	25°C	70	90		70	90		dB
			Full range	70			70			
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 10\ k\Omega$	25°C		30	150		30	150	μV/V
			Full range			150			150	
e_n	Equivalent input noise voltage (closed-loop)	A_{VD}=100, R_S = 0, f = 1 kHz, BW = 1 Hz	25°C		45			45		$nV/\sqrt{Hz}$
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current (Both amplifiers)	No load, No signal	25°C		3.4	5.6		3.4	5.6	mA
			Full range			6.6			6.6	
P_D	Total power dissipation (Both amplifiers)	No load, No signal	25°C		100	170		100	170	mW
			Full range			200			200	
V_{o1}/V_{o2}	Channel separation		25°C		120			120		dB

†All characteristics are specified under open-loop operation, unless otherwise noted. Full range for SN52558 is −55°C to 125°C and for SN72558 is 0°C to 70°C.

NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN52558			SN72558			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF, See Figure 2		0.3			0.3		μs
	Overshoot			5%			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, See Figure 2		0.5			0.5		V/μs

For mechanical data and ordering instructions, see the SN52741/SN72741 data sheet dated November 1970.

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DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to zero. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at zero volts.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at zero volts.

Input Voltage Range (V_I) The range of voltage which if exceeded at either input terminal will cause the amplifier to cease functioning properly.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage which can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the peak-to-peak output voltage swing to the change in differential input voltage required to drive the output.

Maximum-Output-Swing Bandwidth (B_{OM}) The range of frequencies within which the maximum output voltage swing is above a specified value.

Unity-Gain Bandwidth (B_1) The range of frequencies within which the voltage amplification is greater than unity.

Phase Margin (ϕ_m) A figure equal to 180° minus the absolute value of the phase shift measured around the loop at that frequency at which the magnitude of the loop gain is unity.

Gain Margin (A_m) The reciprocal of the differential voltage amplification at that frequency where the absolute value of the phase shift measured around the loop is 180°.

Input Resistance (r_i) The resistance between the input terminals with either input grounded.

Output Resistance (r_o) The resistance between the output terminal and ground.

Input Capacitance (C_i) The capacitance between the input terminals with either input grounded.

Common-Mode Input Impedance (z_{ic}) The parallel sum of the small-signal impedances between each input terminal and ground.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Power Supply Sensitivity ($\Delta V_{IO}/\Delta V_{CC}$) The ratio of the change in input offset voltage to the change in supply voltages producing it. For these devices, both supply voltages are varied symmetrically.

Short-Circuit Output Current (I_{OS}) The maximum output current available from the amplifier with the output shorted to ground or to either supply.

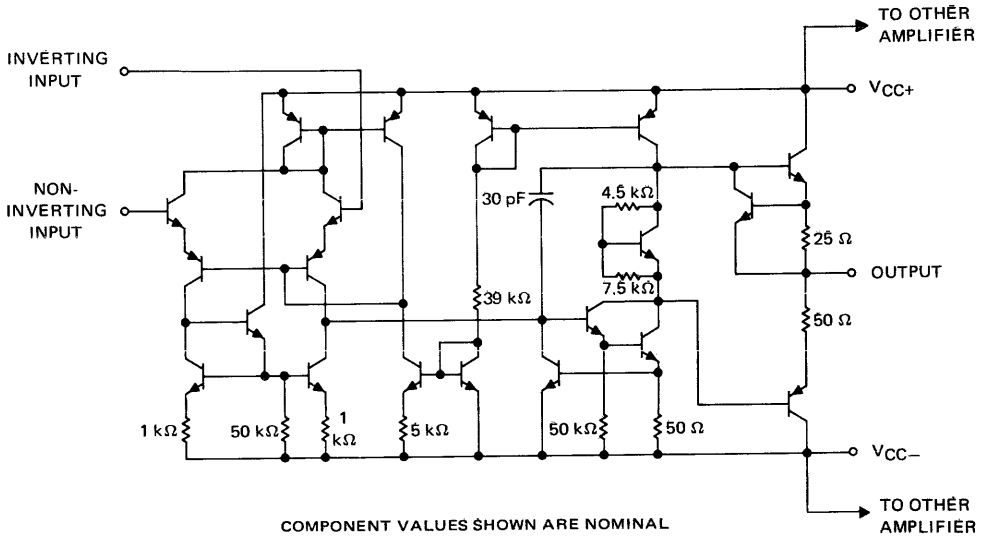
Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Rise Time (t_r) The time required for an output voltage step to change from 10% to 90% of its final value.

Overshoot The quotient of: (1) the largest deviation of the output signal value from its steady-state value after a step-function change of the input signal, and (2) the difference between the output signal values in the steady state before and after the step-function change of the input signal.

Slew Rate (SR) The average time rate of change of the closed-loop amplifier output voltage for a step-signal input. Slew rate is measured between specified output levels (0 and 10 volts for this device) with feedback adjusted for unity gain.

schematic (each amplifier)



COMPONENT VALUES SHOWN ARE NOMINAL

THERMAL INFORMATION

DISSIPATION DERATING CURVE

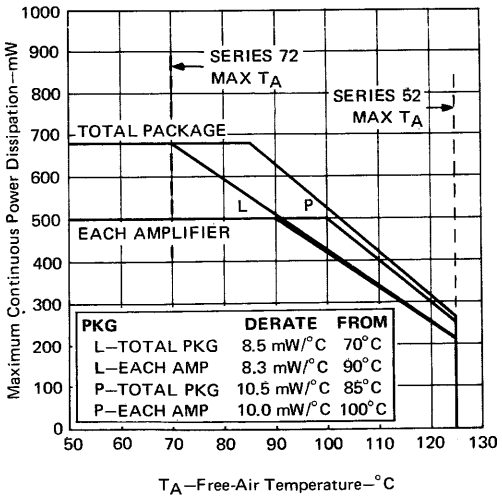
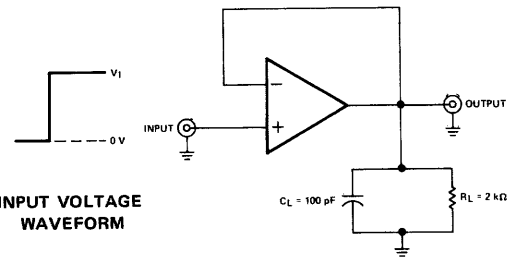


FIGURE 1

PARAMETER MEASUREMENT INFORMATION



INPUT VOLTAGE WAVEFORM

TEST CIRCUIT

FIGURE 2–RISE TIME, OVERSHOOT, AND SLEW RATE

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TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

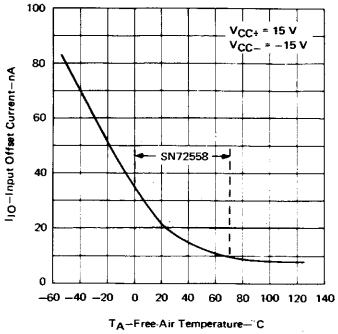

FIGURE 3

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

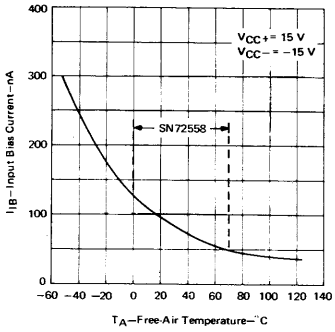

FIGURE 4

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
LOAD RESISTANCE

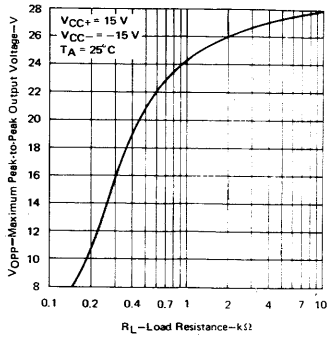

FIGURE 5

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

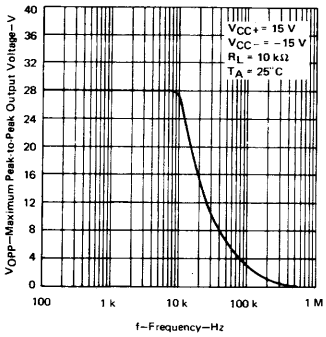

FIGURE 6

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

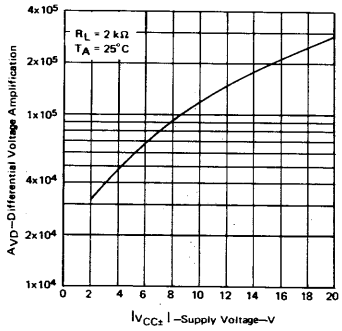

FIGURE 7

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY

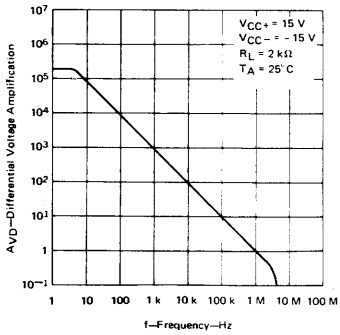

FIGURE 8

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

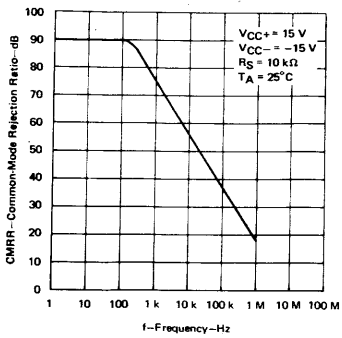

FIGURE 9

OUTPUT VOLTAGE
vs
ELAPSED TIME

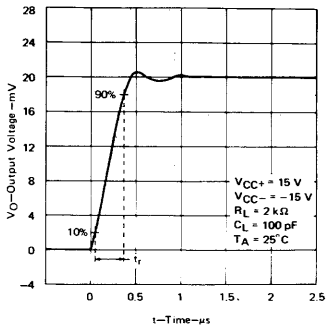

FIGURE 10

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

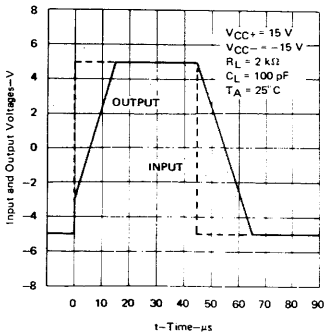

FIGURE 11

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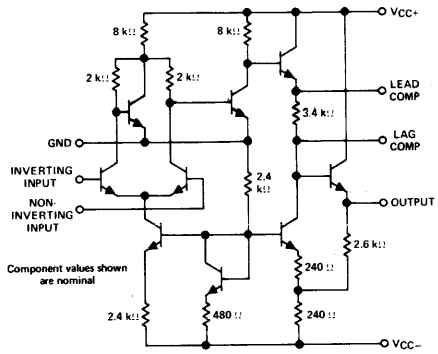
CIRCUIT TYPES SN52702A, SN52702, SN72702 GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

SN52702A features

- Open-Loop Voltage Amplification . . . 3600 Typ
- Designed to be Interchangeable With Fairchild μA702A
- CMRR . . . 100 dB Typ

schematic



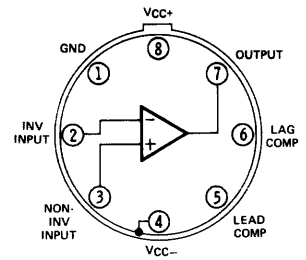
description

The SN52702A, SN52702 and SN72702 circuits are high-gain, wideband operational amplifiers, each having differential inputs and single-ended emitter-follower outputs. Provisions are incorporated within the circuit whereby external components may be used to compensate the amplifier for stable operation under various feedback or load conditions. Component matching, inherent in silicon monolithic circuit-fabrication techniques, produces an amplifier with low-drift and low-offset characteristics. The SN52702A is an improved version of the SN52702. These amplifiers are particularly useful for applications requiring transfer or generation of linear and non-linear functions up to a frequency of 30 MHz.

The SN52702A and SN52702 circuits are characterized for operation over the full military temperature range of −55°C to 125°C. The SN72702 circuit is characterized for operation over the temperature range of 0°C to 70°C.

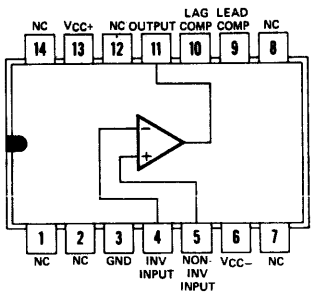
terminal assignments

L PLUG-IN PACKAGE (TOP VIEW)

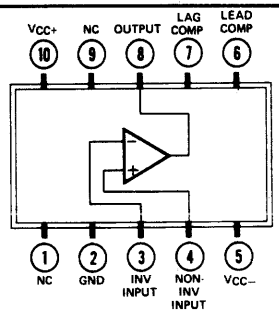


PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

N DUAL-IN-LINE PACKAGE (TOP VIEW)



S FLAT PACKAGE (TOP VIEW)



PIN 5 IS IN ELECTRICAL CONTACT WITH THE CASE

NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52702A, SN52702	SN72702	UNIT
Supply voltage V_{CC+} (see Note 1)		14	14	V
Supply voltage V_{CC-} (see Note 1)		−7	−7	V
Differential input voltage (see Note 2)		±5	±5	V
Input voltage (either input, see Notes 1 and 3)		−6 to 1.5	−6 to 1.5	V
Peak output current ($t_w \leq 1$ S)		50	50	mA
Continuous total dissipation at (or below) 70°C free-air temperature (see Note 4)		300	300	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	L or S Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N Package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the lesser of the two supply voltages.
4. For operation of SN52702A and SN52702 above 70°C free-air temperature, refer to Dissipation Derating Curve, Figure 3.

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SN52702A

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS†			SN52702A V_{CC+} = 12 V, V_{CC-} = −6 V MIN	SN52702A V_{CC+} = 12 V, V_{CC-} = −6 V TYP	SN52702A V_{CC+} = 12 V, V_{CC-} = −6 V MAX	SN52702A V_{CC+} = 6 V, V_{CC-} = −3 V MIN	SN52702A V_{CC+} = 6 V, V_{CC-} = −3 V TYP	SN52702A V_{CC+} = 6 V, V_{CC-} = −3 V MAX	UNIT
V_{IO}	Input offset voltage	$R_S \leq 2\ k\Omega$		25°C		0.5	2		0.7	3	mV
				Full range			3			4	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S = 50\ \Omega$		−55°C to 25°C		2	10		3	15	μV/°C
				25°C to 125°C		2.5	10		3.5	15	
I_{IO}	Input offset current			25°C		0.2	0.5		0.12	0.5	μA
				−55°C		0.4	1.5		0.3	1.5	
				125°C		0.08	0.5		0.05	0.5	
α_{IIO}	Average temperature coefficient of input offset current			−55°C to 25°C		3	16		2	13	nA/°C
				25°C to 125°C		1	5		0.7	4	
I_{IB}	Input bias current			25°C		2	5		1.2	3.5	μA
				−55°C		4.3	10		2.6	7.5	
V_I	Input voltage range	Positive swing		25°C	0.5	1		0.5	1		V
		Negative swing			−4	−5		−1.5	−2		
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L \geq 100\ k\Omega$		25°C	10	10.6		5	5.4		V
				Full range	10			5			
		$R_L = 10\ k\Omega$		25°C	7	8		3	4		
		$R_L \geq 10\ k\Omega$		Full range	7			3			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 100\ k\Omega$	$V_O = \pm 5$ V	25°C	2500	3600	6000				
				Full range	2000		7000				
			$V_O = \pm 2.5$ V	25°C				600	900	1500	
				Full range				500		1750	
r_i	Input resistance			25°C	16	40		22	67		kΩ
				Full range	6			8			
r_o	Output resistance	V_O = 0,	See Note 3	25°C		200	500		300	700	Ω
CMRR	Common-mode rejection ratio	$R_S \leq 2\ k\Omega$		25°C	80	100		80	100		dB
				Full range	70			70			
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 2\ k\Omega$		25°C		75			75		μV/V
				Full range			200			200	
I_{CC}	Supply current	No load,	No signal	25°C		5	6.7		2.1	3.3	mA
				−55°C		5	7.5		2.1	3.9	
				125°C		4.4	6.7		1.7	3.3	
P_D	Total power dissipation	No load,	No signal	25°C		90	120		19	30	mW
				−55°C		90	135		19	35	
				125°C		80	120		15	30	

†All characteristics are specified under open-loop operation. Full range for SN52702A is −55°C to 125°C.

NOTE 3: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

SN52702

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS†			SN52702 V_{CC+} = 12 V, V_{CC-} = −6 V			SN52702 V_{CC+} = 6 V, V_{CC-} = −3 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 2\ k\Omega$		25°C		2	5		2	5	mV
				Full range			6			6	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S = 50\ \Omega$		−55°C to 25°C		10			10		μV/°C
				25°C to 125°C		5			5		
I_{IO}	Input offset current			25°C		0.5	2		0.3	2	μA
				−55°C		1	3			3	
				125°C		0.2	3			3	
α_{IIO}	Average temperature coefficient of input offset current			−55°C to 25°C		6			5		nA/°C
				25°C to 125°C		3			2		
I_{IB}	Input bias current			25°C		4	10		2.5	7	μA
				−55°C		6.5	20			14	
V_I	Input voltage range	Positive swing		25°C	0.5	1		0.5	1		V
		Negative swing			−4	−5		−1.5	−2		
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L \geq 100\ k\Omega$			10	10.6		5	5.4		V
		$R_L = 10\ k\Omega$				8			4		
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 100\ k\Omega$	$V_O = \pm 5$ V	25°C	1400	2600					
				Full range	1000						
			$V_O = \pm 2.5$ V	25°C				380	700		
r_i	Input resistance			25°C	8	25		12	40		kΩ
				Full range	3			4			
r_o	Output resistance	$V_O = 0$,	See Note 3	25°C		200	500		300	700	Ω
CMRR	Common-mode rejection ratio	$R_S \leq 2\ k\Omega$		25°C	70	80		70	80		dB
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 2\ k\Omega$		25°C		60	300		60	300	μV/V
I_{CC}	Supply current	No load,	No signal	25°C		5	6.7		2.1	3.9	mA
P_D	Total power dissipation	No load,	No signal	25°C		90	120		19	35	mW

† All characteristics are specified under open-loop operation. Full range for SN52702 is −55°C to 125°C.

NOTE 3: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

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SN72702

electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V

PARAMETER		TEST CONDITIONS†			SN72702 MIN	SN72702 TYP	SN72702 MAX	UNIT
V_{IO}	Input offset voltage	$R_S \leq 2\ k\Omega$		25°C		5	10	mV
				Full Range			15	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S = 50\ \Omega$		Full Range		5		μV/°C
I_{IO}	Input offset current			25°C		0.5	5	μA
				Full Range			7.5	
α_{IIO}	Average temperature coefficient of input offset current			0°C to 25°C		5		nA/°C
				25°C to 70°C		3		
I_{IB}	Input bias current			25°C		4	15	μA
				0°C		4.5	20	
V_I	Input voltage range	Positive swing		25°C	0.5	1		V
		Negative swing			−4	−5		
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L \geq 100\ k\Omega$		25°C	10	10.6		V
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 100\ k\Omega$,	$V_O = \pm 5$ V	25°C	1000	2600		
				Full Range	800			
r_i	Input resistance			25°C	6	25		kΩ
				Full Range	3.5			
r_o	Output resistance	V_O = 0,	See Note 3	25°C		200	600	Ω
CMRR	Common-mode rejection ratio	$R_S \leq 2\ k\Omega$		25°C	65	80		dB
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 2\ k\Omega$		25°C		60	300	μV/V
I_{CC}	Supply current	No load,	No signal	25°C		5	7	mA
P_D	Total power dissipation	No load,	No signal	25°C		90	125	mW

†All characteristics are specified under open-loop operation. Full range for SN72702 is 0°C to 70°C.
NOTE 3: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

SN52702A, SN52702, SN72702

operating characteristics V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		ALL TYPES MIN	ALL TYPES TYP	ALL TYPES MAX	UNIT
t_r	Rise time	1	V_I = 10 mV,	C_L = 0		25	120	ns
		2	V_I = 1 mV			10	30	ns
	Overshoot	1	V_I = 10 mV,	C_L = 100 pF		10%	50%	
		2	V_I = 1 mV			20%	40%	
SR	Slew rate	1	V_I = 6 V,	C_L = 100 pF		1.7		V/μs
		2	V_I = 100 mV			11		

PARAMETER MEASUREMENT INFORMATION

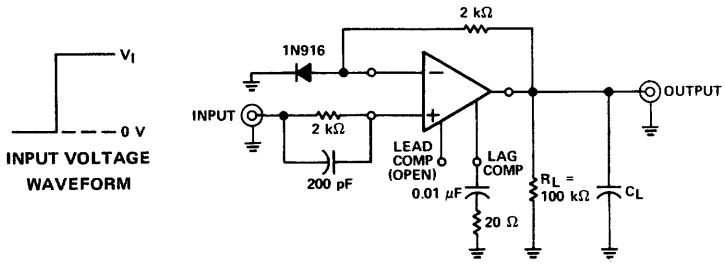

FIGURE 1–UNITY-GAIN AMPLIFIER

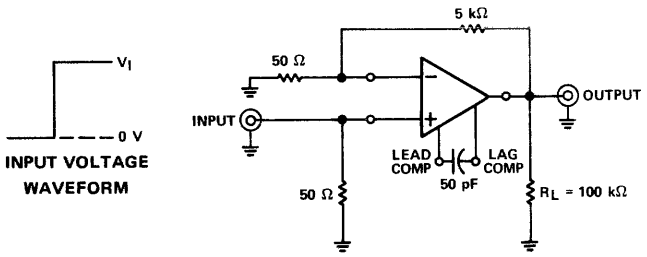

FIGURE 2–GAIN-OF-100 AMPLIFIER

THERMAL INFORMATION

SN52702A, SN52702
DISSIPATION DERATING CURVE

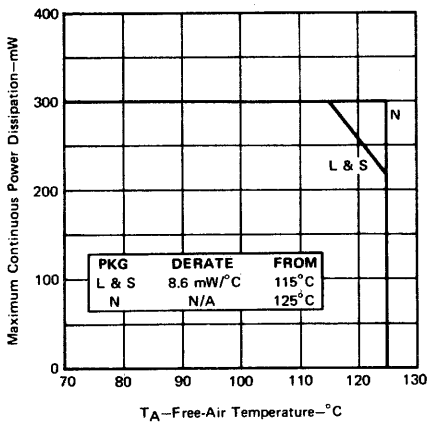

FIGURE 3

TEXAS INSTRUMENTS
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DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to zero. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO}) The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left| \frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right| \text{ where } T_{A(1)} \text{ and } T_{A(2)} \text{ are the specified temperature extremes.}$$

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at zero volts.

Average Temperature Coefficient Of Input Offset Current (α_{IIO}) The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{IIO} = \left| \frac{(I_{IO} @ T_{A(1)}) - (I_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right| \text{ where } T_{A(1)} \text{ and } T_{A(2)} \text{ are the specified temperature extremes.}$$

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at zero volts.

Input Voltage Range (V_I) The range of voltage which if exceeded at either input terminal will cause the amplifier to cease functioning properly.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage which can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the peak-to-peak output voltage swing to the change in differential input voltage required to drive the output.

Input Resistance (r_i) The resistance between the input terminals with either input grounded.

Output Resistance (r_o) The resistance between the output terminal and ground.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Power Supply Sensitivity ($\Delta V_{IO}/\Delta V_{CC}$) The ratio of the change in input offset voltage to the change in supply voltages producing it. For these devices, both supply voltages are varied symmetrically.

Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Rise Time (t_r) The time required for an output voltage step to change from 10% to 90% of its final value.

Overshoot The quotient of: (1) the largest deviation of the output signal value from its steady-state value after a step-function change of the input signal, and (2) the difference between the output signal values in the steady state before and after the step-function change of the input signal.

Slew Rate (SR) The average time rate of change of the closed-loop amplifier output voltage for a step-signal input. Slew rate is measured between specified output levels (0 and 10 volts for this device) with feedback adjusted for unity gain.

TYPICAL CHARACTERISTICS

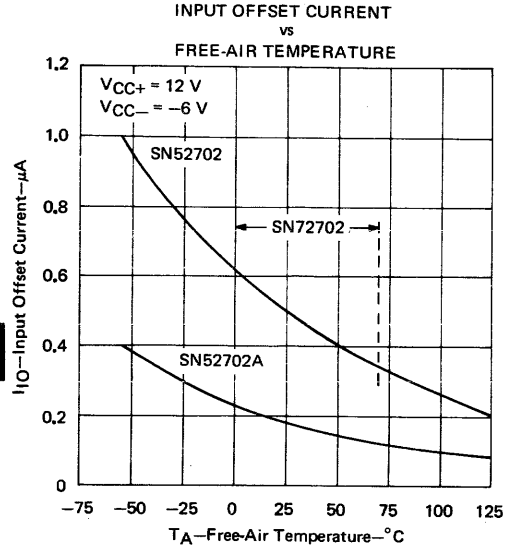


FIGURE 4

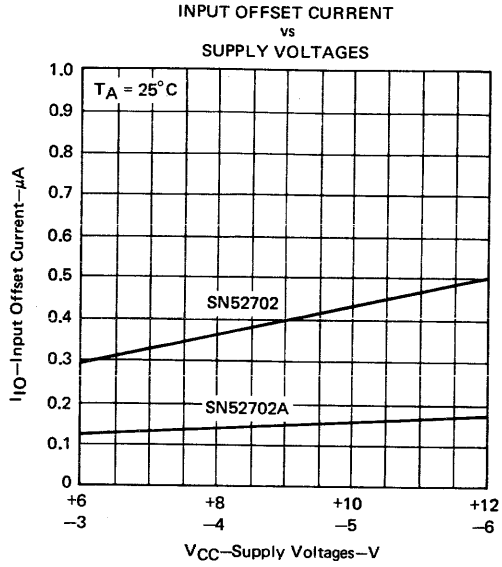


FIGURE 5

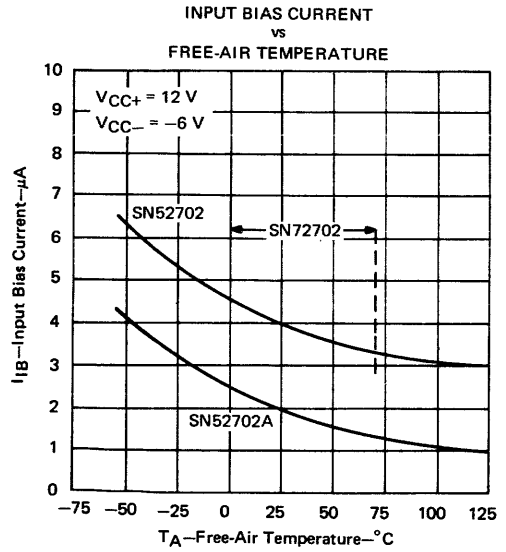


FIGURE 6

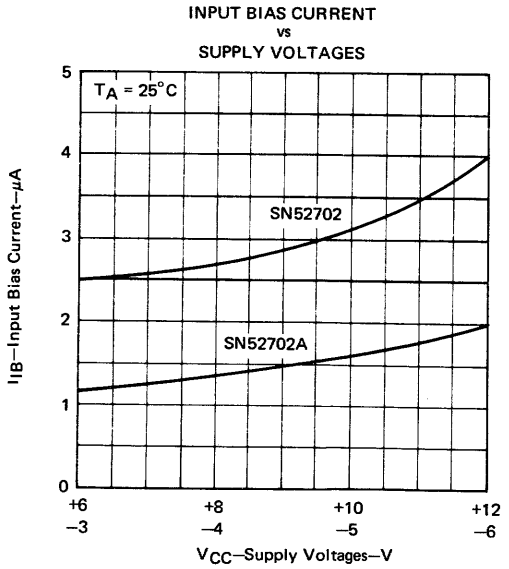


FIGURE 7

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY
(for various lag compensations)

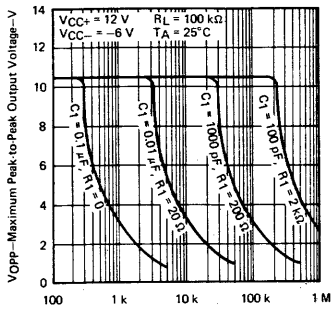
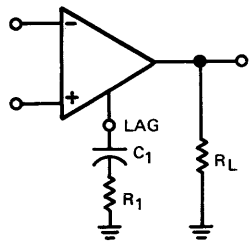


FIGURE 8



LAG COMPENSATION CIRCUIT
FOR FIGURES 8, 9, AND 10

SN52709A
LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY

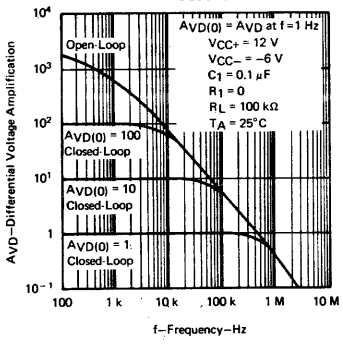


FIGURE 9

SN52702A
LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY
(for various lag compensations)

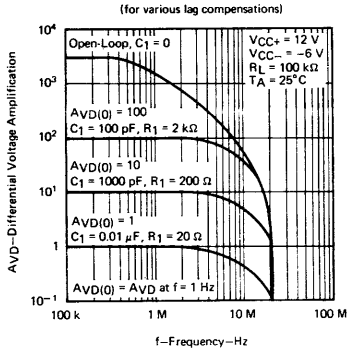


FIGURE 10

SN52702A
LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY
(for various lag compensations)

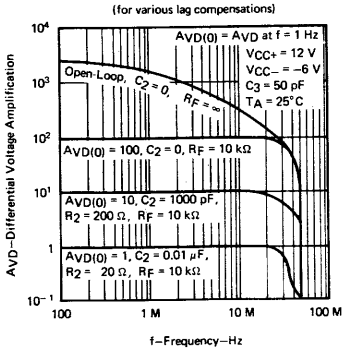
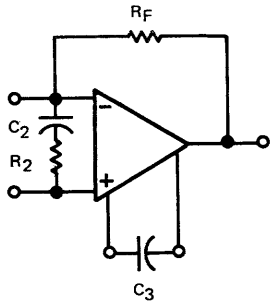


FIGURE 11



LEAD-LAG COMPENSATION CIRCUIT
FOR FIGURE 11

3

TYPICAL CHARACTERISTICS

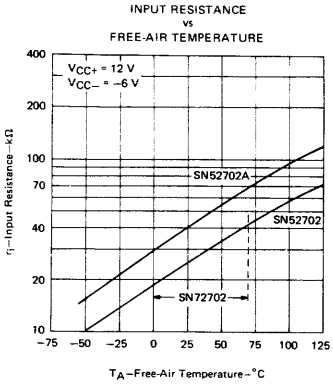


FIGURE 12

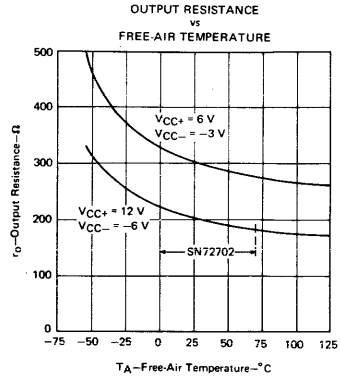


FIGURE 13

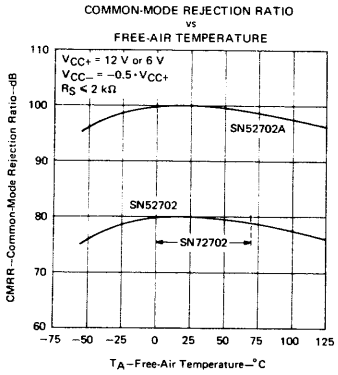


FIGURE 14

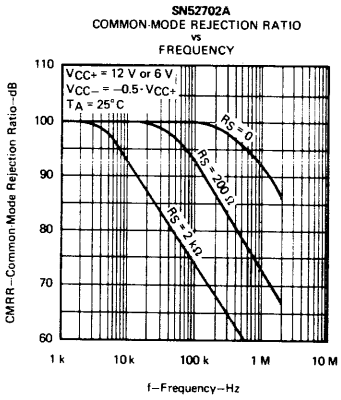


FIGURE 15

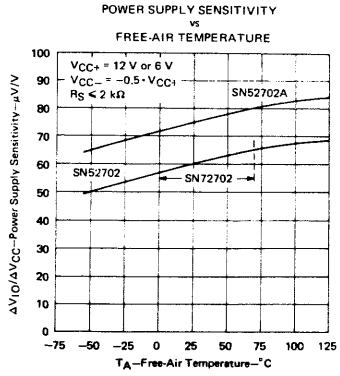


FIGURE 16

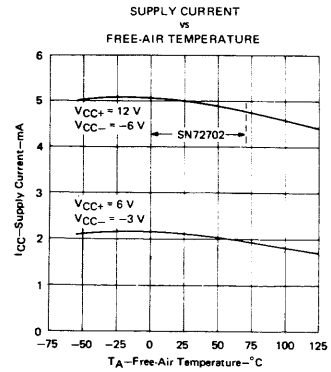


FIGURE 17

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CIRCUIT TYPES SN52709A, SN52709, SN72709 HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

SERIES 52/72 OPERATIONAL AMPLIFIERS
featuring

- Common-Mode Input Range . . . ±10 V Typical
- Designed to be Interchangeable with Fairchild μA709A, μA709, and μA709C
- Maximum Peak-to-Peak Output Voltage Swing . . . 28 V Typical with 15 V Supplies

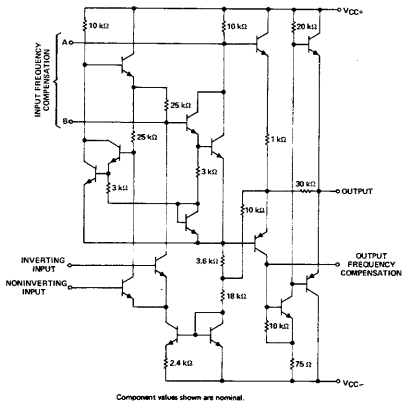
description

These circuits are high-performance operational amplifiers, each having high-impedance differential inputs and a low-impedance output. Component matching, inherent with silicon monolithic circuit-fabrication techniques, produces an amplifier with low-drift and low-offset characteristics. Provisions are incorporated within the circuit whereby external components may be used to compensate the amplifier for stable operation under various feedback or load conditions. These amplifiers are particularly useful for applications requiring transfer or generation of linear or nonlinear functions.

The SN52709A circuit features improved offset characteristics, reduced input-current requirements, and lower power dissipation when compared to the SN52709 circuit. In addition, maximum values of the average temperature coefficients of offset voltage and current are guaranteed.

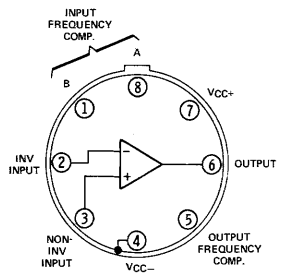
The SN52709A and SN52709 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN72709 is characterized for operation from 0°C to 70°C.

schematic

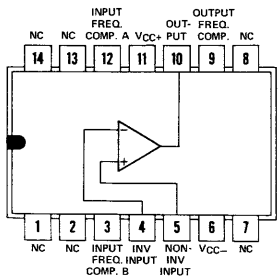


terminal assignments

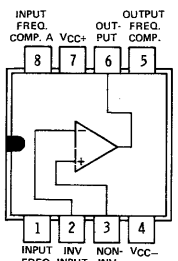
L — PLUG-IN PACKAGE (TOP VIEW)



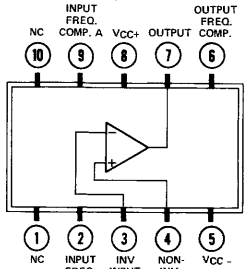
N — DUAL-IN-LINE PACKAGE (TOP VIEW)



P — DUAL-IN-LINE PACKAGE (TOP VIEW)



S — FLAT PACKAGE (TOP VIEW)



NC—No internal connection

voltages specified

Throughout this data sheet, supply voltages are specified either as a range or as a specific value. A positive voltage within the specified range (or of the specified value) is applied to V_{CC+}, and an equal negative voltage is applied to V_{CC-}.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52709A, SN52709	SN72709	UNIT
Supply voltage V_{CC+} (see Note 1)		18	18	V
Supply voltage V_{CC-} (see Note 1)		−18	−18	V
Differential input voltage (see Note 2)		±5	±5	V
Input voltage (either input, see Notes 1 and 3)		±10	±10	V
Duration of output short-circuit (see Note 4)		5	5	s
Continuous total dissipation at (or below) 70°C free-air temperature (see Note 5)		300	300	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	L or S Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P Package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 10 volts, whichever is less.
4. The output may be shorted to ground or either power supply.
5. For operation of SN52709A and SN52709 above 70°C free-air temperature, refer to Dissipation Derating Curve, Figure 1.

3

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±9 V to ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN52709A MIN	SN52709A TYP‡	SN52709A MAX	SN52709 MIN	SN52709 TYP‡	SN52709 MAX	UNIT
V_{IO}	Input offset voltage	$R_S \leq 10$ kΩ	25°C		0.6	2		1	5	mV
			Full range			3			6	
α_{VIO}	Average temperature coefficient of input offset voltage	R_S = 50 Ω	Full range		1.8	10		3		µV/°C
		R_S = 10 kΩ	−55°C to 25°C		4.8	25		6		
			25°C to 125°C		2	15		6		
I_{IO}	Input offset current		25°C		10	50		50	200	nA
			−55°C		40	250		100	500	
			125°C		3.5	50		20	200	
α_{IIO}	Average temperature coefficient of input offset current		−55°C to 25°C		0.45	2.8				nA/°C
			25°C to 125°C		0.08	0.5				
I_{IB}	Input bias current		25°C		0.1	0.2		0.2	0.5	µA
			−55°C		0.3	0.6		0.5	1.5	
V_I	input voltage range	$V_{CC\pm}$ = ±15 V	25°C	±8	±10		±8	±10		V
			Full range	±8			±8			
V_{OPP}	Maximum peak-to-peak output voltage swing	$V_{CC\pm}$ = ±15 V, $R_L \geqslant 10$ kΩ	25°C	24	28		24	28		V
			Full range	24			24			
		$V_{CC\pm}$ = ±15 V, R_L = 2 kΩ	25°C	20	26		20	26		
		$V_{CC\pm}$ = ±15 V, $R_L \geqslant 2$ kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±15 V, $R_L \geqslant 2$ kΩ, V_O = ±10 V	25°C		45,000			45,000		
			Full range	25,000		70,000	25,000		70,000	
r_i	Input resistance		25°C	350	750		150	400		kΩ
			−55°C	85	185		40	100		
r_o	Output resistance	V_O = 0, See Note 6	25°C		150			150		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 10$ kΩ	25°C	80	110		70	90		dB
			Full range	80			70			
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 10$ kΩ	25°C		40	100		25	150	µV/V
			Full range			100			150	
I_{CC}	Supply current	$V_{CC\pm}$ = ±15 V, No load, No signal	25°C		2.5	3.6		2.6	5.5	mA
			−55°C		2.7	4.5				
			125°C		2.1	3				
P_D	Total power dissipation	$V_{CC\pm}$ = ±15 V, No load, No signal	25°C		75	108		78	165	mW
			−55°C		81	135				
			125°C		63	90				

†All characteristics are specified under open-loop operation. Full range for SN52709A and SN52709 is −55°C to 125°C.

‡All typical values are at $V_{CC\pm}$ = ±15 V.

Note 6: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

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electrical characteristics at specified free-air temperature (unless otherwise noted $V_{CC\pm} = \pm 15$ V)

PARAMETER		TEST CONDITIONS†			SN72709 MIN	SN72709 TYP	SN72709 MAX	UNIT
V_{IO}	Input offset voltage	$V_{CC\pm} = \pm 9$ V to ± 15 V, $R_S \leq 10$ kΩ		25°C		2	7.5	mV
				Full range			10	
I_{IO}	Input offset current	$V_{CC\pm} = \pm 9$ V to ± 15 V		25°C		100	500	nA
				Full range			750	
I_{IB}	Input bias current	$V_{CC\pm} = \pm 9$ V to ± 15 V		25°C		0.3	1.5	μA
				Full range			2	
V_I	Input voltage range			25°C	±8	±10		V
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L \geq 10$ kΩ		25°C	24	28		V
				Full range	24			
		$R_L = 2$ kΩ		25°C	20	26		
		$R_L \geq 2$ kΩ		Full range	20			
A_{VD}	Large-signal differential voltage amplification	$R_L \leq 2$ kΩ,	$V_O = \pm 10$ V	25°C	15,000	45,000		
				Full range	12,000			
r_i	Input resistance			25°C	50	250		kΩ
				Full range	35			
r_o	Output resistance	$V_O = 0$,	See Note 6	25°C		150		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 10$ kΩ		25°C	65	90		dB
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 10$ kΩ		25°C		25	200	μV/V
P_D	Total power dissipation	No load,	No signal	25°C		80	200	mW

†All characteristics are specified under open-loop operation. Full range for SN72709 is 0°C to 70°C.

NOTE 6: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics $V_{CC\pm} = \pm 9$ V to ± 15 V, $T_A = 25$°C

PARAMETER		TEST CONDITIONS		SN52709A SN52709 SN72709 MIN	TYP	MAX	UNIT
t_r	Rise time	$V_I = 20$ mV, $R_L = 2$ kΩ, See Figure 2	$C_L = 0$		0.3	1	μs
	Overshoot		$C_L = 100$ pF		6%	30%	

THERMAL INFORMATION

SN52709A, SN52709

DISSIPATION DERATING CURVE

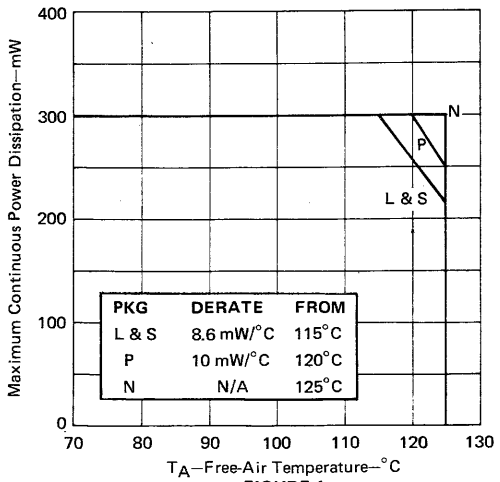

FIGURE 1

PARAMETER MEASUREMENT INFORMATION

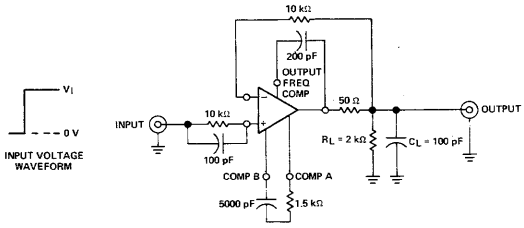

FIGURE 2—RISE TIME AND SLEW RATE

DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to zero. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO}) The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left|\frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}}\right| \text{ where } T_{A(1)} \text{ and } T_{A(2)} \text{ are the specified temperature extremes.}$$

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at zero volts.

Average Temperature Coefficient Of Input Offset Current (α_{IIO}) The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{IIO} = \left|\frac{(I_{IO} @ T_{A(1)}) - (I_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}}\right| \text{ where } T_{A(1)} \text{ and } T_{A(2)} \text{ are the specified temperature extremes.}$$

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at zero volts.

Input Voltage Range (V_I) The range of voltage which if exceeded at either input terminal will cause the amplifier to cease functioning properly.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage which can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the peak-to-peak output voltage swing to the change in differential input voltage required to drive the output.

Input Resistance (r_i) The resistance between the input terminals with either input grounded.

Output Resistance (r_o) The resistance between the output terminal and ground.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Power Supply Sensitivity ($\Delta V_{IO}/\Delta V_{CC}$) The ratio of the change in input offset voltage to the change in supply voltages producing it. For these devices, both supply voltages are varied symmetrically.

Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Rise Time (t_r) The time required for an output voltage step to change from 10% to 90% of its final value.

Overshoot The quotient of: (1) the largest deviation of the output signal value from its steady-state value after a step-function change of the input signal, and (2) the difference between the output signal values in the steady state before and after the step-function change of the input signal.

Slew Rate (SR) The average time rate of change of the closed-loop amplifier output for a step-signal input. Slew rate is measured between specified output levels (0 and 10 volts for this device) with feedback adjusted for unity gain.

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TYPICAL CHARACTERISTICS
(unless designated maximum or minimum)

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

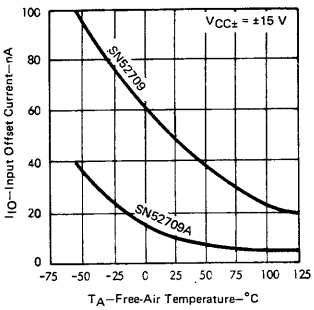


FIGURE 3

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

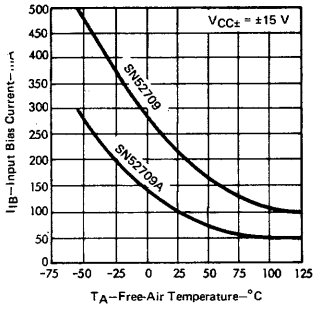


FIGURE 4

INPUT BIAS CURRENT
vs
SUPPLY VOLTAGE

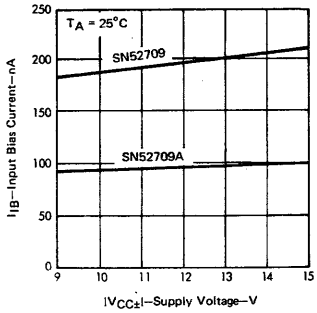


FIGURE 5

INPUT VOLTAGE RANGE
vs
SUPPLY VOLTAGE

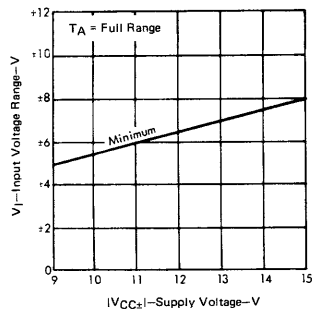


FIGURE 6

INPUT RESISTANCE
vs
FREE-AIR TEMPERATURE

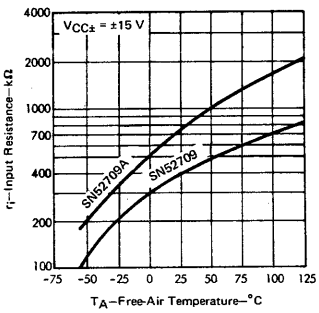


FIGURE 7

SN52709A
COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

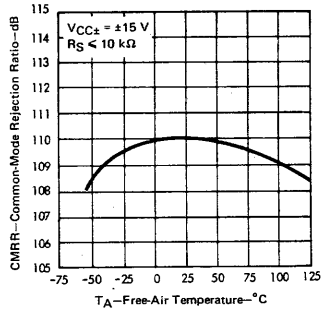


FIGURE 8

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

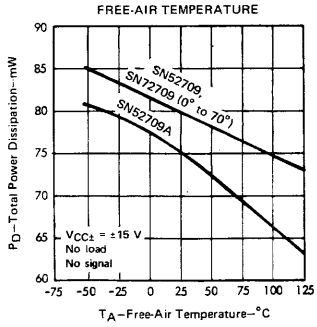


FIGURE 9

SN52709A
TOTAL POWER DISSIPATION
vs
SUPPLY VOLTAGE

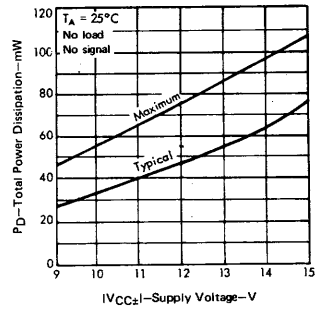


FIGURE 10

SN52709, SN72709
TOTAL POWER DISSIPATION
vs
SUPPLY VOLTAGE

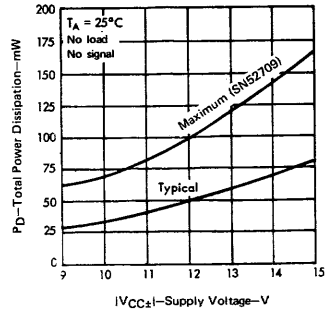


FIGURE 11

TYPICAL CHARACTERISTICS
(unless designated maximum or minimum)

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

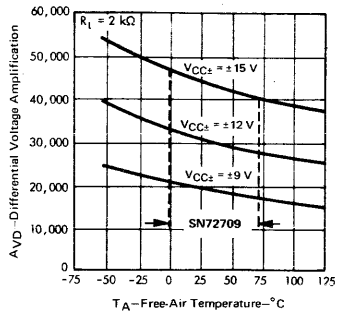


FIGURE 12

SN52709A, SN52709
OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

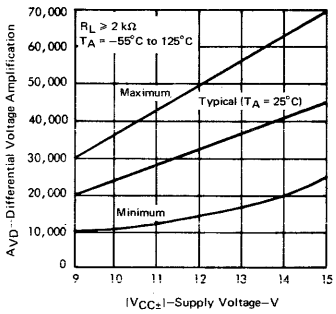


FIGURE 13

SN72709
OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

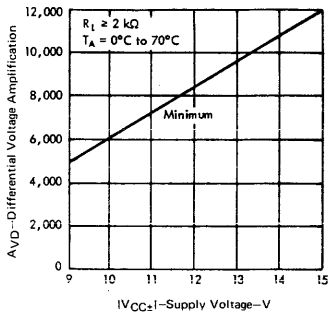


FIGURE 14

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

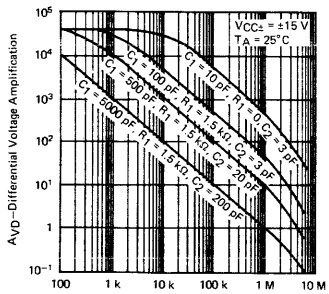


FIGURE 15

CLOSED-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

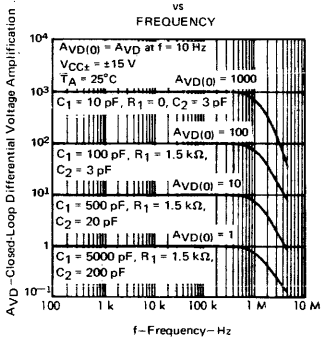
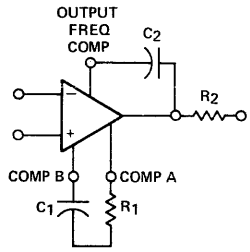


FIGURE 16



When the amplifier is operated with capacitive loading, R_2 = 50 Ω.

FREQUENCY COMPENSATION CIRCUIT FOR FIGURES 15, 16, AND 19

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

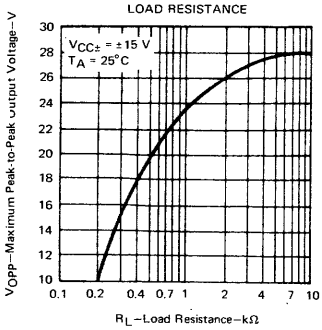


FIGURE 17

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

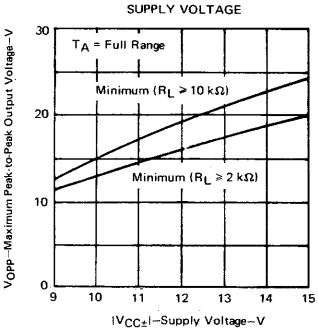


FIGURE 18

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

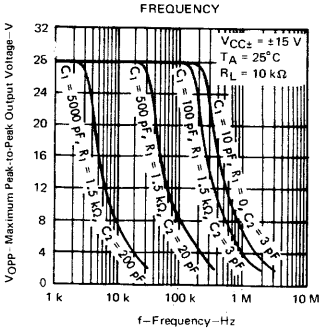


FIGURE 19

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TYPICAL CHARACTERISTICS

SN52709A, SN52709
VOLTAGE TRANSFER CHARACTERISTICS

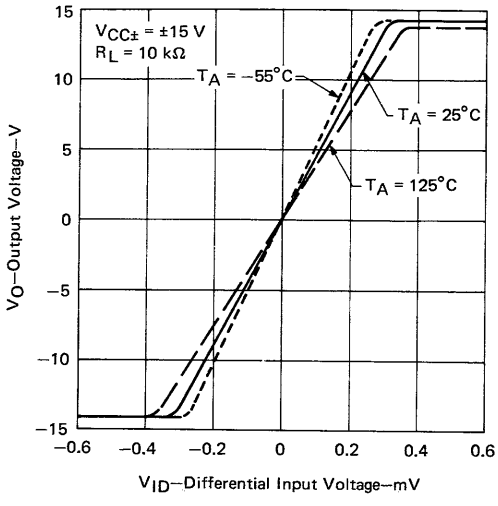

FIGURE 20

SN72709
VOLTAGE TRANSFER CHARACTERISTICS

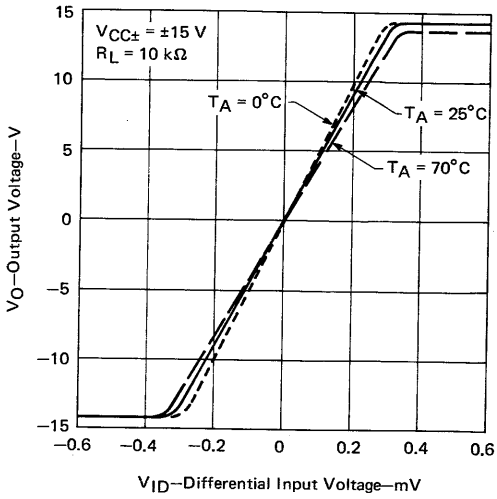

FIGURE 21

RELATIVE OUTPUT SWING vs ELAPSED TIME

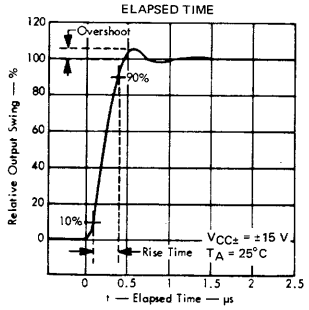

FIGURE 22

SLEW RATE vs CLOSED-LOOP DIFFERENTIAL VOLTAGE AMPLIFICATION

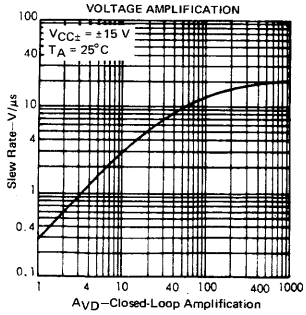

FIGURE 23

NORMALIZED FREQUENCY CHARACTERISTICS vs FREE-AIR TEMPERATURE

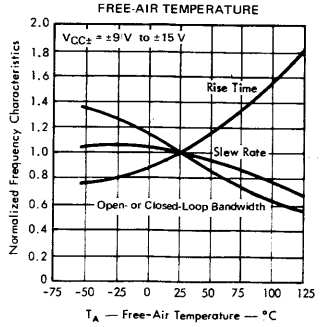

FIGURE 24

NORMALIZED FREQUENCY CHARACTERISTICS vs SUPPLY VOLTAGE

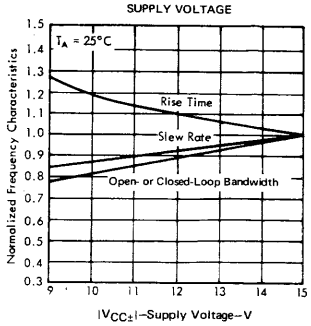

FIGURE 25

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CIRCUIT TYPES SN52741, SN72741
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

- Short-Circuit Protection
- Offset-Voltage Null Capability
- Large Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-up
- Same Pin Assignments as SN52709/SN72709

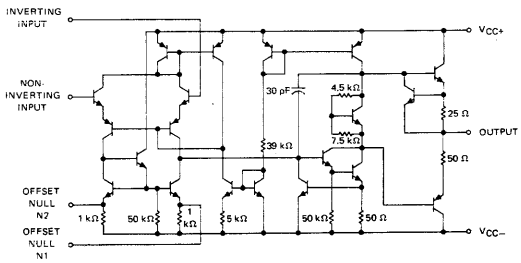
description

The SN52741 and SN72741 are high-performance operational amplifiers, featuring offset-voltage null capability.

The high common-mode input voltage range and the absence of latch-up make the amplifier ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components. A low-value potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 11.

The SN52741 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72741 is characterized for operation from 0°C to 70°C.

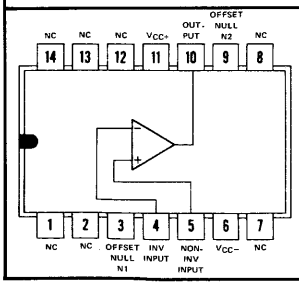
schematic



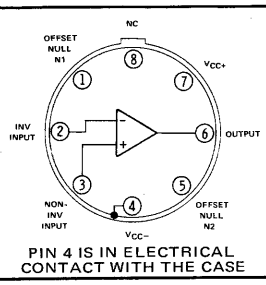
COMPONENT VALUES SHOWN ARE NOMINAL

terminal assignments

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)

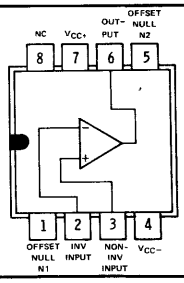


L PLUG-IN PACKAGE (TOP VIEW)

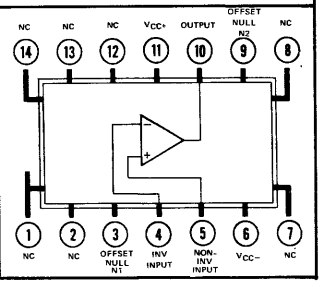


PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

P DUAL-IN-LINE PACKAGE (TOP VIEW)



Z FLAT PACKAGE (TOP VIEW)



NC—No internal connection

1170

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52741	SN72741	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		±0.5	±0.5	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total power dissipation at (or below) 55°C free-air temperature (see Note 5)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, L, or Z Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P Package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the SN52741 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 55°C free-air temperature, refer to Dissipation Derating Curve, Figure 12.

3

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		SN52741			SN72741			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 10$ kΩ	25°C		1	5		1	6	mV
			Full range			6			7.5	
$\Delta V_{IO(adj)}$	Offset voltage adjust range		25°C		±15			±15		mV
I_{IO}	Input offset current		25°C		20	200		20	200	nA
			Full range			500			300	
I_{IB}	Input bias current		25°C		80	500		80	500	nA
			Full range			1500			800	
V_I	Input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L = 10 kΩ	25°C	24	28		24	28		V
		$R_L \geq$ 10 kΩ	Full range	24			24			
		R_L = 2 kΩ	25°C	20	26		20	26		
		$R_L \geq$ 2 kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq$ 2 kΩ, V_O = ±10 V	25°C	50,000	200,000		20,000	200,000		
			Full range	25,000			15,000			
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	V_O = 0 V, See Note 5	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	$R_S \leq 10$ kΩ	25°C	70	90		70	90		dB
			Full range	70			70			
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 10$ kΩ	25°C		30	150		30	150	μV/V
			Full range			150			150	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current	No load, No signal	25°C		1.7	2.8		1.7	2.8	mA
			Full range			3.3			3.3	
P_D	Total power dissipation	No load, No signal	25°C		50	85		50	85	mW
			Full range			100			100	

†All characteristics are specified under open-loop operation. Full range for SN52741 is −55°C to 125°C and for SN72741 is 0°C to 70°C.
NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN52741			SN72741			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ,		0.3			0.3		μs
	Overshoot	C_L = 100 pF, See Figure 1		5%			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.5			0.5		V/μs

DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to zero. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at zero volts.

3

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at zero volts.

Input Voltage Range (V_I) The range of voltage which, if exceeded at either input terminal, will cause the amplifier to cease functioning properly.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage which can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the peak-to-peak output voltage swing to the change in differential input voltage required to drive the output.

Input Resistance (r_i) The resistance between the input terminals with either input grounded.

Output Resistance (r_o) The resistance between the output terminal and ground.

Input Capacitance (C_i) The capacitance between the input terminals with either input grounded.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Power Supply Sensitivity ($\Delta V_{IO}/\Delta V_{CC}$) The ratio of the change in input offset voltage to the change in supply voltages producing it. For these devices, both supply voltages are varied symmetrically.

Short-Circuit Output Current (I_{OS}) The maximum output current available from the amplifier with the output shorted to ground or to either supply.

Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Rise Time (t_r) The time required for an output voltage step to change from 10% to 90% of its final value.

Overshoot The quotient of: (1) the largest deviation of the output signal value from its steady-state value after a step-function change of the input signal, and (2) the difference between the output signal values in the steady state before and after the step-function change of the input signal.

Slew Rate (SR) The average time rate of change of the closed-loop amplifier output voltage for a step-signal input. Slew rate is measured between specified output levels (0 and 10 volts for this device) with feedback adjusted for unity gain.

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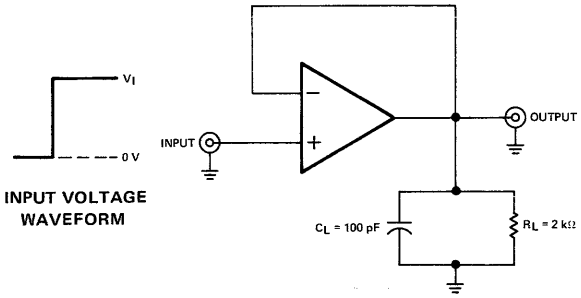
PARAMETER MEASUREMENT INFORMATION



INPUT VOLTAGE WAVEFORM

TEST CIRCUIT

FIGURE 1–RISE TIME, OVERSHOOT, AND SLEW RATE

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

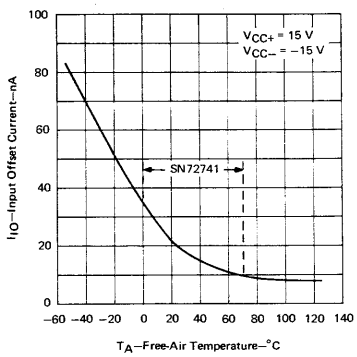


FIGURE 2

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

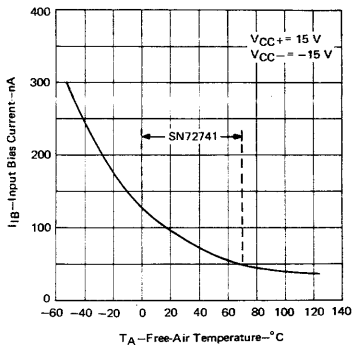


FIGURE 3

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

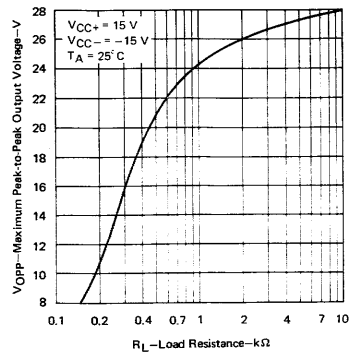


FIGURE 4

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

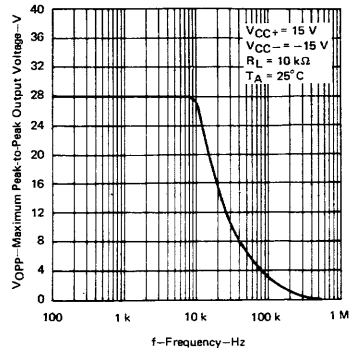


FIGURE 5

TYPICAL CHARACTERISTICS

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

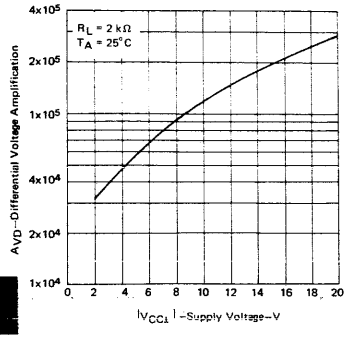


FIGURE 6

COMMON-MODE REJECTION RATIO vs FREQUENCY

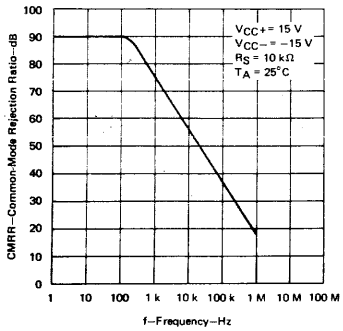


FIGURE 8

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

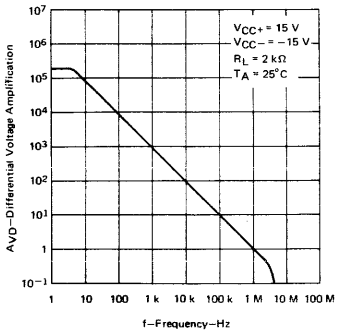


FIGURE 7

OUTPUT VOLTAGE vs ELAPSED TIME

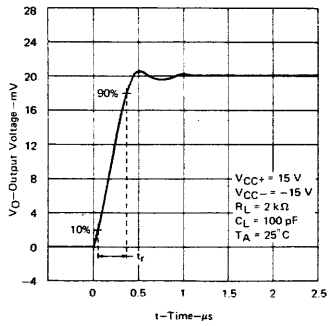


FIGURE 9

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

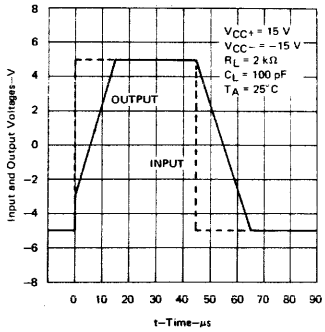


FIGURE 10

TYPICAL APPLICATION DATA

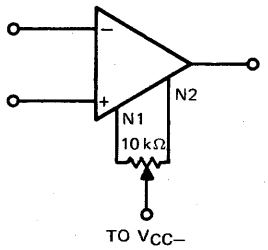
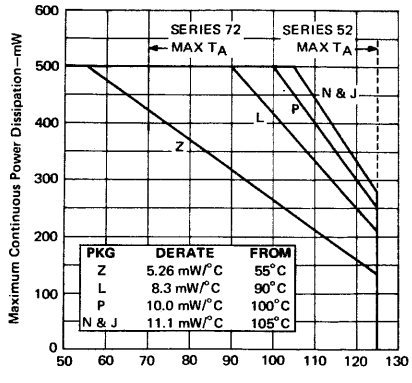


FIGURE 11–INPUT OFFSET VOLTAGE NULL CIRCUIT

THERMAL INFORMATION

DISSIPATION DERATING CURVE



PKG	DERATE	FROM
Z	5.26 mW/°C	55°C
L	8.3 mW/°C	90°C
P	10.0 mW/°C	100°C
N & J	11.1 mW/°C	105°C

FIGURE 12

TEXAS INSTRUMENTS
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CIRCUIT TYPES SN52747, SN72747
DUAL HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

- No frequency Compensation Required
- Low Power Consumption
- Short-Circuit Protection
- Offset-Voltage Null Capability
- Large Common-Mode and Differential Voltage Ranges
- No Latch-up
- Designed to be Interchangeable with Fairchild μA747 and μA747C

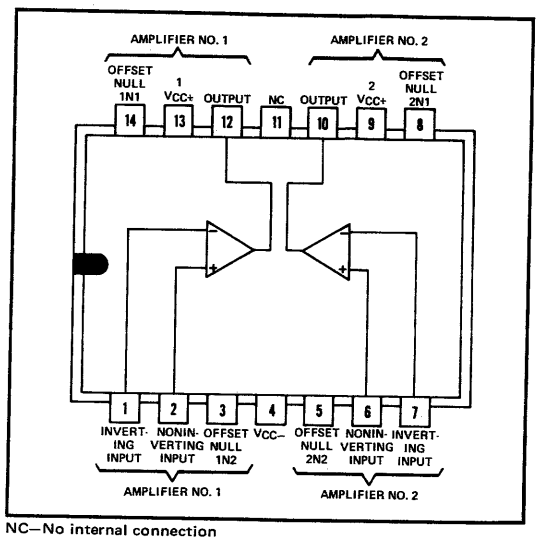
description

The SN52747 and SN72747 are dual high-performance operational amplifiers, featuring offset-voltage null capability. Each half is electrically similar to SN52741/SN72741.

The high common-mode input voltage range and the absence of latch-up make the amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components. A low-value potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 3.

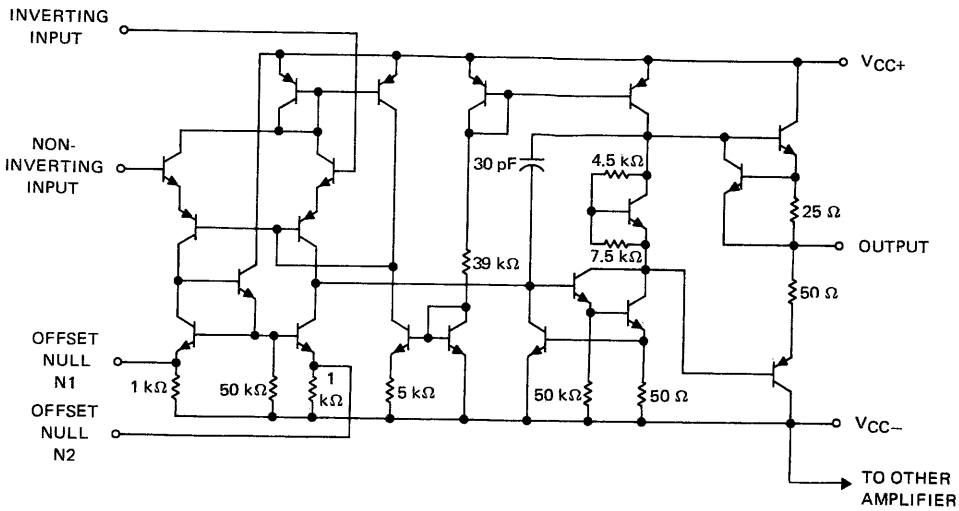
The SN52747 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72747 is characterized for operation from 0°C to 70°C.

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection

schematic (each amplifier)



Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52747	SN72747	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		±0.5	±0.5	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation at (or below) 70°C free-air temperature (see Note 5)	Each amplifier	500	500	mW
	Total package	800	800	
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the SN52747 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation of SN52747 above 70°C free-air temperature, refer to Dissipation Derating Curve, Figure 2.

3

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		SN52747 MIN	SN52747 TYP	SN52747 MAX	SN72747 MIN	SN72747 TYP	SN72747 MAX	UNIT
V_{IO}	Input offset voltage	$R_S \leq 10\ k\Omega$	25°C		1	5		1	6	mV
			Full range			6			7.5	
$\Delta V_{IO(adj)}$	Offset voltage adjust range		25°C		±15			±15		mV
I_{IO}	Input offset current		25°C		20	200		20	200	nA
			Full range			500			300	
I_{IB}	Input bias current		25°C		80	500		80	500	nA
			Full range			1500			800	
V_I	Input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L = 10 kΩ	25°C	24	28		24	28		V
		$R_L \geq$ 10 kΩ	Full range	24			24			
		R_L = 2 kΩ	25°C	20	26		20	26		
		$R_L \geq$ 2 kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq$ 2 kΩ, V_O = ±10 V	25°C	50,000	200,000		50,000	200,000		
			Full range	25,000			25,000			
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	V_O = 0 V, See Note 5	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	$R_S \leq 10\ k\Omega$	25°C	70	90		70	90		dB
			Full range	70			70			
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 10\ k\Omega$	25°C		30	150		30	150	μV/V
			Full range			150			150	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current	No load, No signal	25°C		1.7	2.8		1.7	2.8	mA
			Full range			3.3			3.3	
P_D	Power dissipation (each amplifier)	No load, No signal	25°C		50	85		50	85	mW
			Full range			100			100	
V_{o1}/V_{o2}	Channel separation		25°C		120			120		dB

† All characteristics are specified under open-loop operation. Full range for SN52747 is −55°C to 125°C and for SN72747 is 0°C to 70°C.
NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.
For definitions of terms, mechanical data, and ordering instructions, see the SN52741/SN72741 data sheet dated November 1970.

TEXAS INSTRUMENTS
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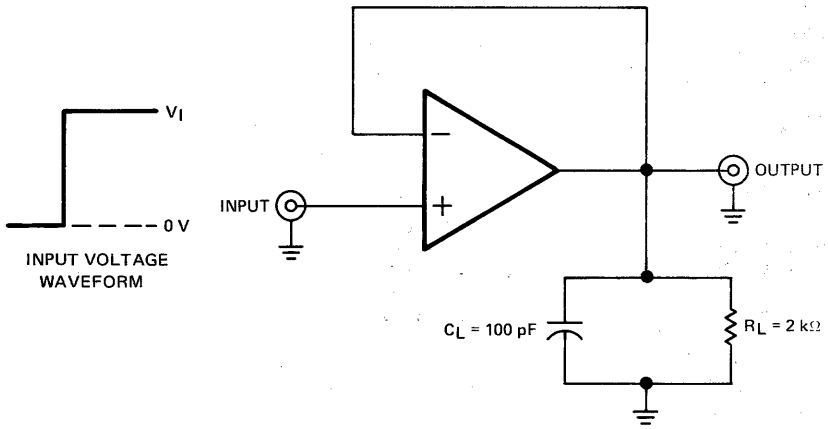
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN52747			SN72747			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ,		0.3			0.3		μs
	Overshoot	C_L = 100 pF, See Figure 1		5%			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.5			0.5		V/μs

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

FIGURE 1–RISE TIME, OVERSHOOT, AND SLEW RATE

THERMAL INFORMATION

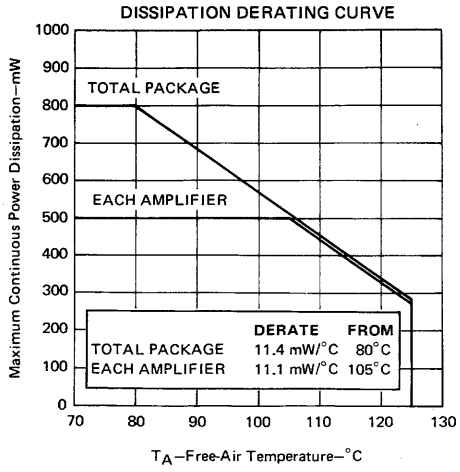


FIGURE 2

TYPICAL APPLICATION DATA

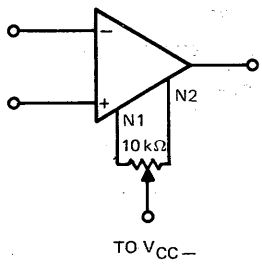


FIGURE 3–INPUT OFFSET VOLTAGE NULL CIRCUIT

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

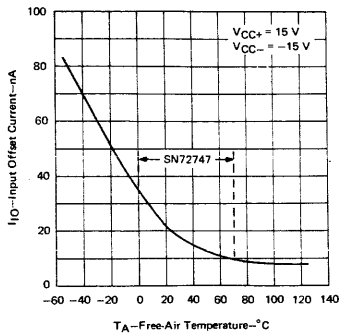


FIGURE 4

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

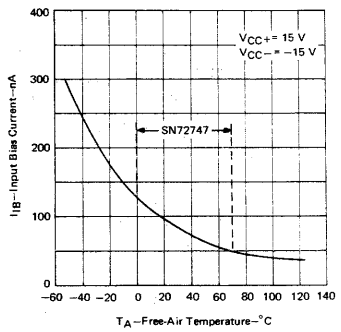


FIGURE 5

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
LOAD RESISTANCE

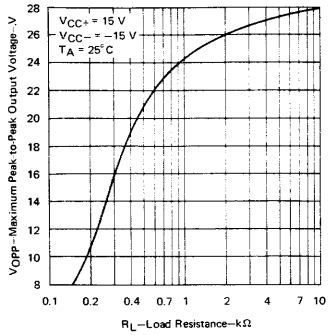


FIGURE 6

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

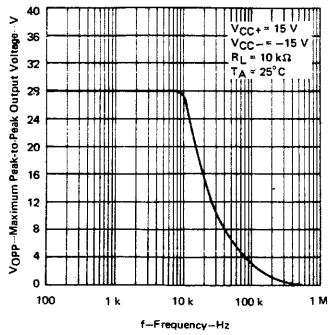


FIGURE 7

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

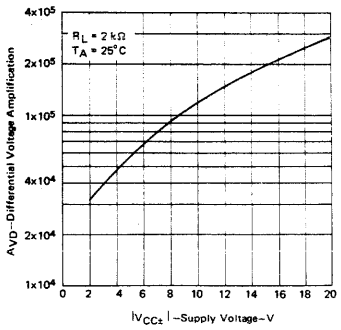


FIGURE 8

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY

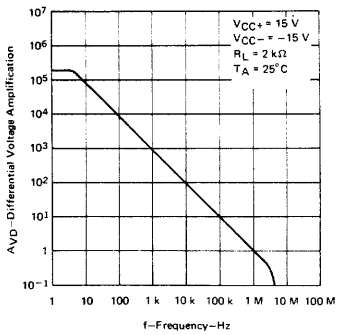


FIGURE 9

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

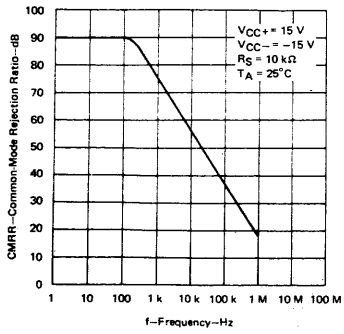


FIGURE 10

OUTPUT VOLTAGE
vs
ELAPSED TIME

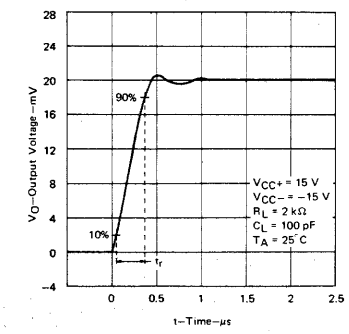


FIGURE 11

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

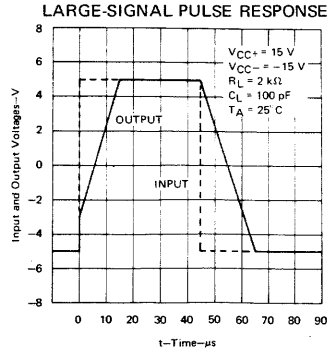


FIGURE 12

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CIRCUIT TYPES SN52748, SN72748
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

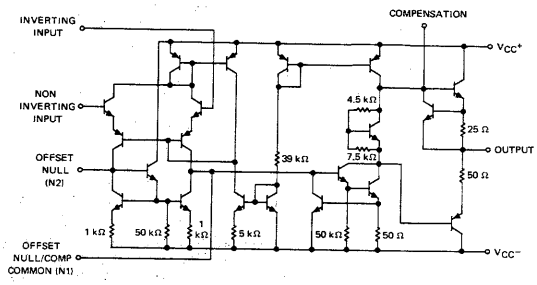
- Frequency and Transient Response Characteristics Adjustable
- Short-Circuit Protection
- Offset-Voltage Null Capability
- Large Common-Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch-up
- Same Pin Assignments as SN52709/SN72709

description

The SN52748 and SN72748 are high-performance operational amplifiers. They offer the same advantages and desirable features as the SN52741 and SN72741 with the exception of internal compensation. The external compensation of the SN52748 and SN72748 allows the changing of the frequency response (when the closed-loop gain is greater than unity) for applications requiring wider bandwidth or higher slew rate. These circuits feature high gain, large differential and common-mode input voltage range, output short-circuit protection, and may be compensated under unity-gain conditions with a single 30-pF capacitor. A potentiometer may be connected between the offset null inputs, as shown in Figure 12, to null out the offset voltage.

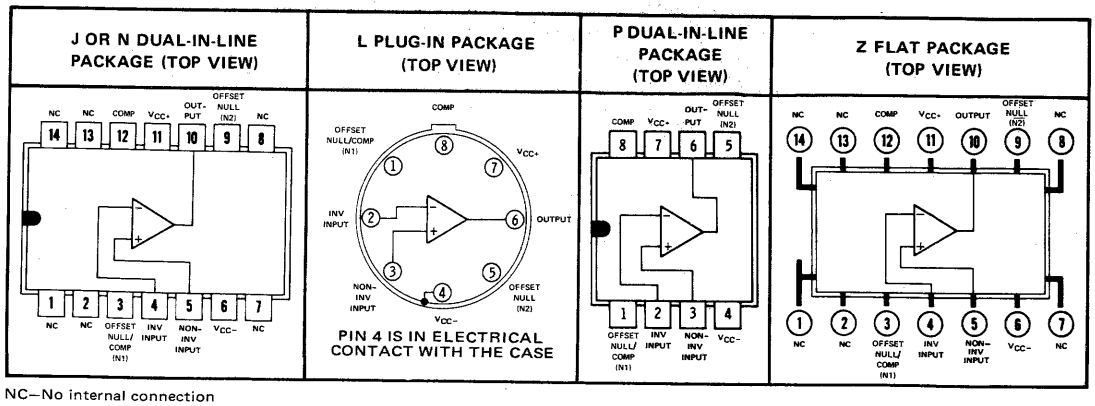
The SN52748 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72748 is characterized for operation from 0°C to 70°C.

schematic



COMPONENT VALUES SHOWN ARE NOMINAL

terminal assignments



NC—No internal connection

CIRCUIT TYPES SN52748, SN72748
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52748	SN72748	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		−0.5 to 2	−0.5 to 2	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total power dissipation at (or below) 55°C free-air temperature (see Note 5)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, L, or Z Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P Package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the SN52748 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 55°C free-air temperature, refer to Dissipation Derating Curve, Figure 13.

3

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		SN52748			SN72748			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 10$ kΩ	25°C		1	5		1	6	mV
			Full range			6			7.5	
I_{IO}	Input offset current		25°C		20	200		20	200	nA
			Full range			500			300	
I_{IB}	Input bias current		25°C		80	500		80	500	nA
			Full range			1500			800	
V_I	Input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L = 10 kΩ	25°C	24	28		24	28		V
		$R_L \geq$ 10 kΩ	Full range	24			24			
		R_L = 2 kΩ	25°C	20	26		20	26		
		$R_L \geq$ 2 kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq$ 2 kΩ, V_O = ±10 V	25°C	50,000	200,000		50,000	200,000		
			Full range	25,000			25,000			
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	V_O = 0 V, See Note 5	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	$R_S \leq 10$ kΩ	25°C	70	90		70	90		dB
			Full range	70			70			
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 10$ kΩ	25°C		30	150		30	150	μV/V
			Full range			150			150	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current	No load, No signal	25°C		1.7	2.8		1.7	2.8	mA
			Full range			3.3			3.3	
P_D	Total power dissipation	No load, No signal	25°C		50	85		50	85	mW
			Full range			100			100	

† All characteristics are specified under open-loop operation. Full range for SN52748 is −55°C to 125°C and for SN72748 is 0°C to 70°C.
NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

For definitions of terms, mechanical data, and ordering instructions, see SN52741/SN72741 data sheet dated November, 1970.

2

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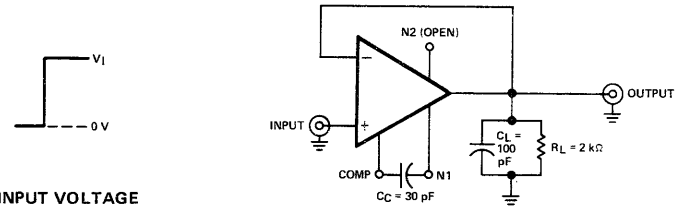
operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	SN52748			SN72748			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	$V_I = 20$ mV, $R_L = 2$ kΩ, $C_L = 100$ pF, $C_C = 30$ pF, See Figure 1		0.3			0.3		μs
	Overshoot			5%			5%		
SR	Slew rate at unity gain	$V_I = 10$ V, $R_L = 2$ kΩ, $C_L = 100$ pF, $C_C = 30$ pF, See Figure 1		0.5			0.5		V/μs

PARAMETER MEASUREMENT INFORMATION



INPUT VOLTAGE WAVEFORM

TEST CIRCUIT

FIGURE 1–RISE TIME, OVERSHOOT, AND SLEW RATE

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

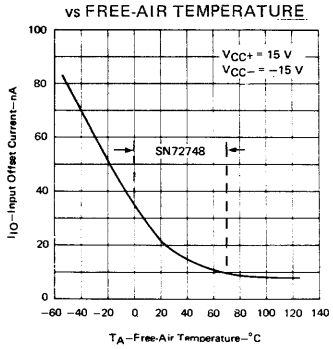


FIGURE 2

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

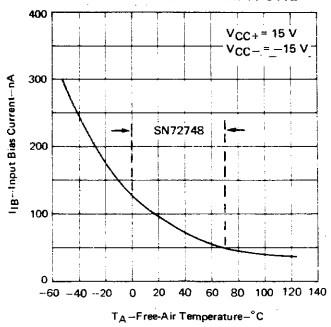


FIGURE 3

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

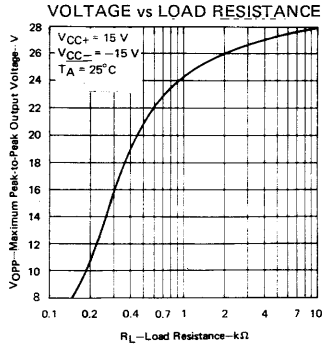


FIGURE 4

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

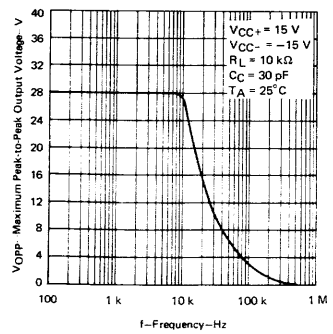


FIGURE 5

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

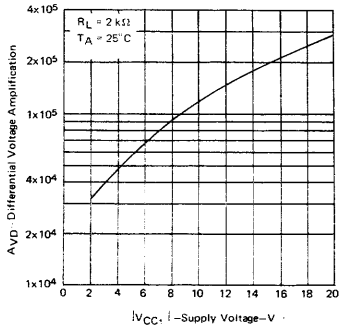


FIGURE 6

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

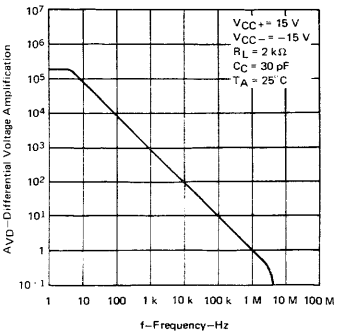


FIGURE 7

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO vs FREQUENCY

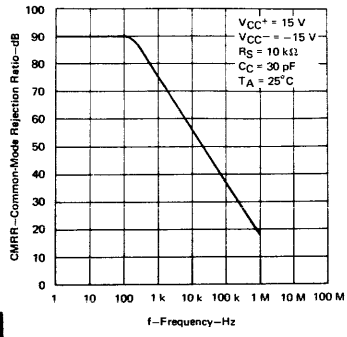


FIGURE 8

OUTPUT VOLTAGE vs ELAPSED TIME

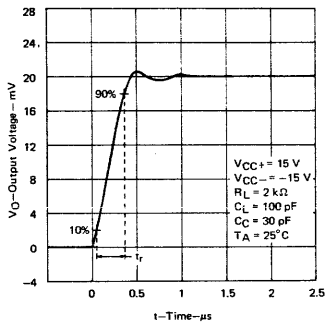


FIGURE 9

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

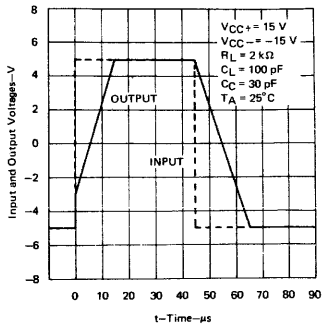
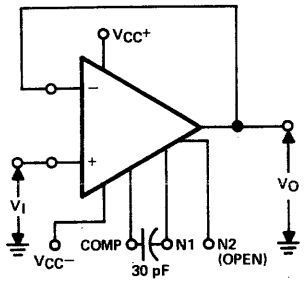


FIGURE 10

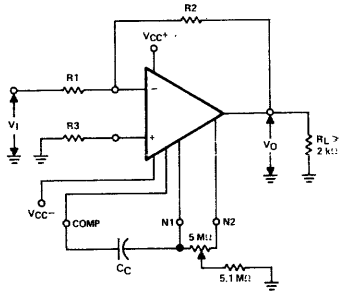
3

TYPICAL APPLICATION DATA



r_i = 400 MΩ, r_o < 1 Ω,
C_i = 1 pF, BW = 1 MHz

FIGURE 11–UNITY-GAIN VOLTAGE FOLLOWER



$$\frac{V_O}{V_I} = -\frac{R2}{R1}$$

$$C_C \geq \frac{R1 \cdot 30\ pF}{R1+R2}$$

$$R3 = \frac{R1 \cdot R2}{R1+R2}$$

FIGURE 12–INVERTING CIRCUIT WITH ADJUSTABLE GAIN, COMPENSATION, AND OFFSET ADJUSTMENT

THERMAL INFORMATION

DISSIPATION DERATING CURVE

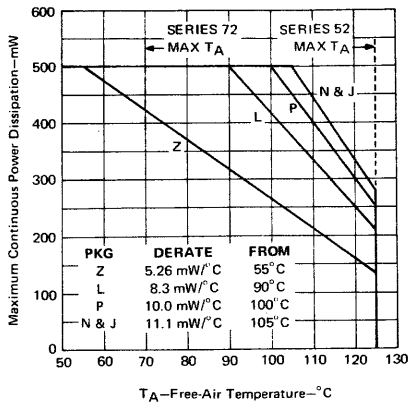


FIGURE 13

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CIRCUIT TYPES SN52770, SN72770
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

- Adjustable Frequency and Transient Response Characteristics
- Offset-Voltage Null Capability
- No Latch-Up
- Low Power Consumption
- High Slew Rates
- Very Low Input Bias Currents
- Very Low Input Offset Parameters
- Short-Circuit Protection
- Large Common-Mode and Differential Voltage Ranges

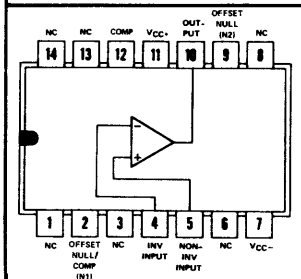
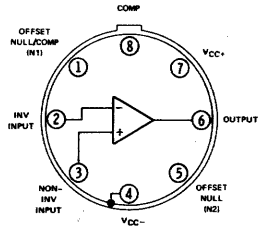
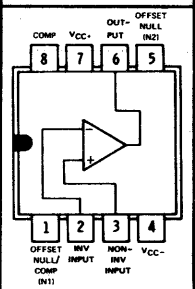
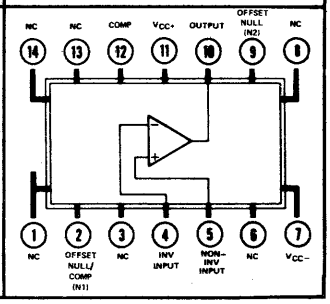
description

The SN52770 and SN72770 are high-performance general purpose integrated-circuit operational amplifiers. They offer the same advantages and desirable features as the SN52771 and SN72771 with the exception of internal compensation. The external compensation of the SN52770 and SN72770 allows the changing of the frequency response (when the closed-loop gain is greater than unity) for applications requiring wider bandwidth or higher slew rate. Unity-gain compensation is accomplished by means of a single 30-pF capacitor, and for higher gains, smaller capacitors may be used to obtain increased slew rate and bandwidth. High slew rate makes these amplifiers ideal for fast-rise-time signals, or large signals at high frequency. Very low input currents make them ideal for sample and hold, logarithmic amplifiers, and other low-level applications. A potentiometer may be connected between the offset null inputs, as shown in Figure 12, to null out the offset voltage.

The SN52770 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72770 is characterized for operation from 0°C to 70°C.

3

terminal assignments

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)	L PLUG-IN PACKAGE (TOP VIEW)	P DUAL-IN-LINE PACKAGE (TOP VIEW)	Z FLAT PACKAGE (TOP VIEW)
			

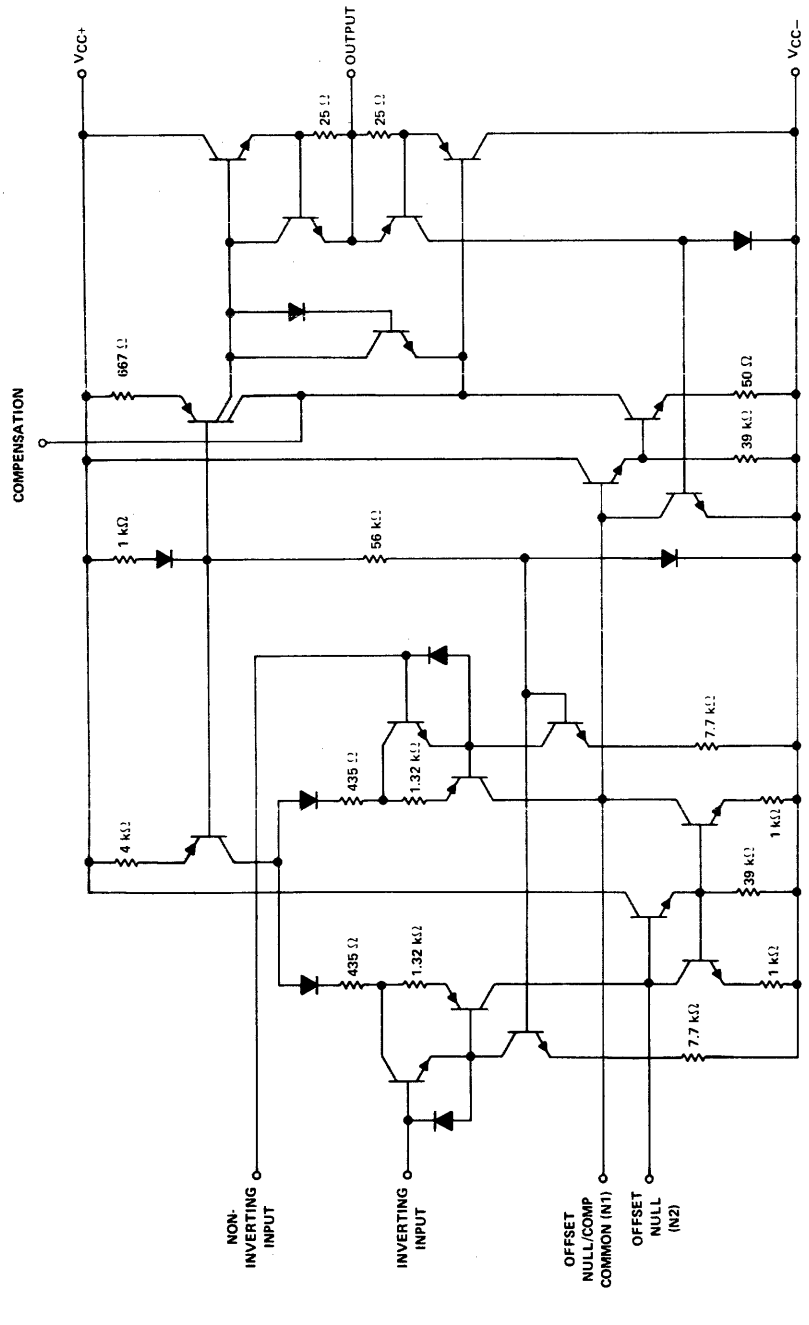
NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52770	SN72770	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		−0.5 to 2	−0.5 to 2	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation at (or below) 55°C free-air temperature (see Note 5)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, L, or Z Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P Package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the SN52770 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 55°C free-air temperature, refer to Dissipation Derating Curve, Figure 1.

schematic



Component values shown are nominal.

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electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		SN52770			SN72770			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 10$ kΩ	25°C		2	4		5	10	mV
			Full range			7			14	
I_{IO}	Input offset current		25°C		1	2		5	10	nA
			Full range			5			14	
I_{IB}	Input bias current		25°C		8	15		15	30	nA
			Full range			35			40	
V_{ICR}	Common-mode input voltage range		25°C	±12	±14		±11			V
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L = 2 kΩ	25°C	24	26.5		22	26.5		
		$R_L \geq$ 2 kΩ	Full range	24			22			
A_{VD}	Large-signal differential voltage amplification	R_L = 2 kΩ, V_O = ±10 V	25°C	50,000	100,000		35,000	100,000		
		$R_L \geq$ 2 kΩ, V_O = ±10 V	Full range	25,000			25,000			
B_{OM}	Maximum-output-swing bandwidth (closed loop)	R_L = 2 kΩ, $V_O \geq$ ± 10 V, A_{VD} = 1, THD ≤ 5%	25°C		40			40		kHz
B_1	Unity-gain bandwidth		25°C		1.3			1.3		MHz
r_{id}	Differential input resistance		25°C		100			100		MΩ
z_{ic}	Common-mode input impedance	f = 10 Hz	25°C		500			500		MΩ
z_o	Output impedance	f = 10 Hz	25°C		2			2		kΩ
CMRR	Common-mode rejection ratio	$R_S \leq$ 10 kΩ	25°C	80	100		70	100		dB
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq$ 10 kΩ	25°C		80	150			200	μV/V
e_n	Equivalent input noise voltage (closed loop)	A_{VD} = 100, BW = 1 Hz, f = 1 kHz	25°C		40			40		$nV/\sqrt{Hz}$
I_{OS}	Short-circuit output current	To V_{CC+}	25°C		24			24		mA
		To V_{CC-}			−20			−20		
I_{CC}	Supply current	No load, No signal	25°C		1.3	2		1.7	4	mA
P_D	Total power dissipation	No load, No signal	25°C		40	60		50	120	mW

†All characteristics are specified under open-loop operation unless otherwise noted. Full range for SN52770 is −55°C to 125°C and for SN72770 is 0°C to 70°C.

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN52770			SN72770			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 200 mV, R_L = 2 kΩ, C_L = 200 pF, C_C = 30 pF, See Figure 2		130			130		ns
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 200 pF, C_C = 30 pF, See Figure 2		2.5			2.5		V/μs

3

DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to zero. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at zero volts.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at zero volts.

Common-Mode Input Voltage Range (V_{ICR}) The range of common-mode voltage which if exceeded will cause the amplifier to cease functioning properly.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage which can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

3

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the peak-to-peak output voltage swing to the change in differential input voltage required to drive the output.

Maximum-Output-Swing Bandwidth (B_{OM}) The range of frequencies within which the maximum output voltage swing is above a specified value.

Unity-Gain Bandwidth (B_1) The range of frequencies within which the voltage amplification is greater than unity.

Differential Input Resistance (r_{id}) The small-signal resistance between the two ungrounded input terminals.

Common-Mode Input Impedance (z_{ic}) The parallel sum of the small-signal impedances between each input terminal and ground.

Output Impedance (z_o) The small-signal impedance between the output terminal and ground.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Power Supply Sensitivity ($\Delta V_{IO}/\Delta V_{CC}$) The ratio of the change in input offset voltage to the change in supply voltages producing it. For these devices, both supply voltages are varied symmetrically.

Short-Circuit Output Current (I_{OS}) The maximum output current available from the amplifier with the output shorted to the specified supply.

Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Rise Time (t_r) The time required for an output voltage step to change from 10% to 90% of its final value.

Slew Rate (SR) The average time rate of change of the closed-loop amplifier output voltage for a step-signal input. Slew rate is measured between specified output levels (0 and 10 volts for this device) with feedback adjusted for unity gain.

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THERMAL INFORMATION

DISSIPATION DERATING CURVE

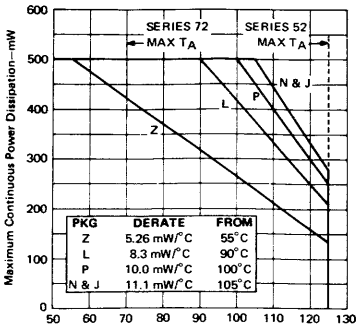


FIGURE 1

PARAMETER MEASUREMENT INFORMATION

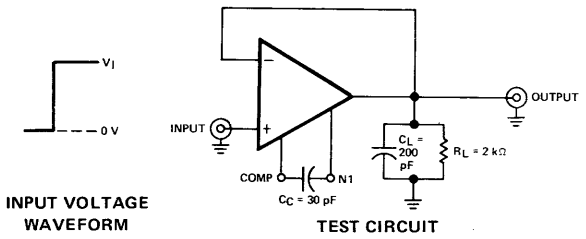


FIGURE 2–BANDWIDTH, RISE TIME, AND SLEW RATE

3

TYPICAL CHARACTERISTICS

SN72770
COMMON-MODE INPUT VOLTAGE RANGE
vs
SUPPLY VOLTAGE

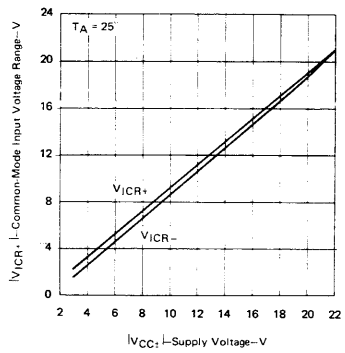


FIGURE 3

MAXIMUM OUTPUT VOLTAGE SWING
vs
SUPPLY VOLTAGE

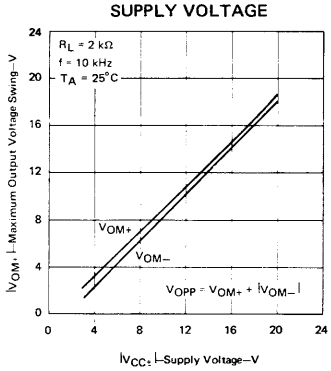


FIGURE 4

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE SWING
vs
FREQUENCY

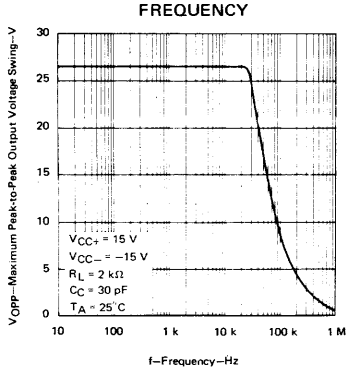


FIGURE 5

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

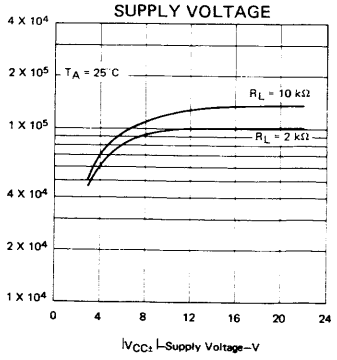


FIGURE 6

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY

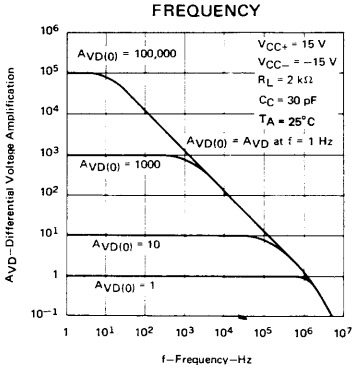


FIGURE 7

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

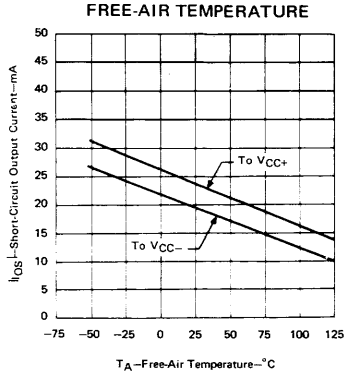


FIGURE 8

TYPICAL CHARACTERISTICS

TOTAL POWER DISSIPATION
vs
SUPPLY VOLTAGE

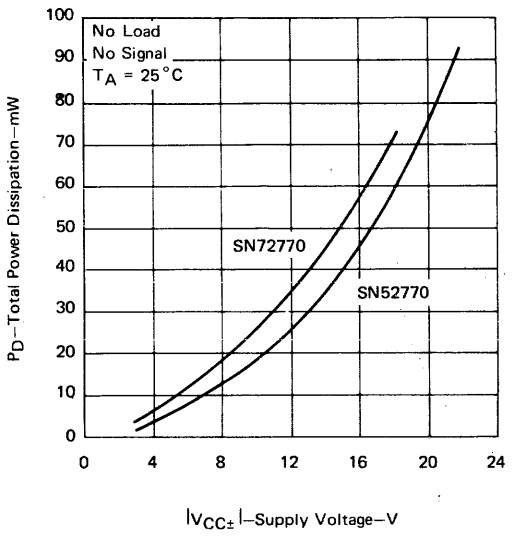


FIGURE 9

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

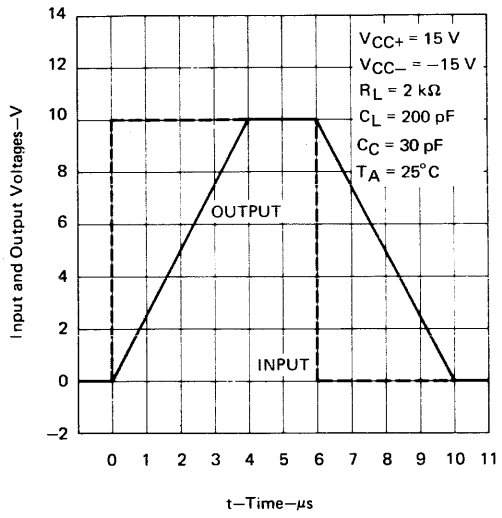
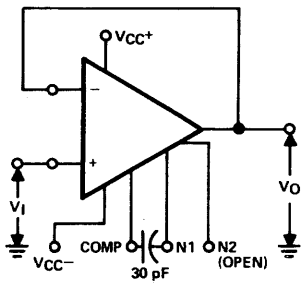


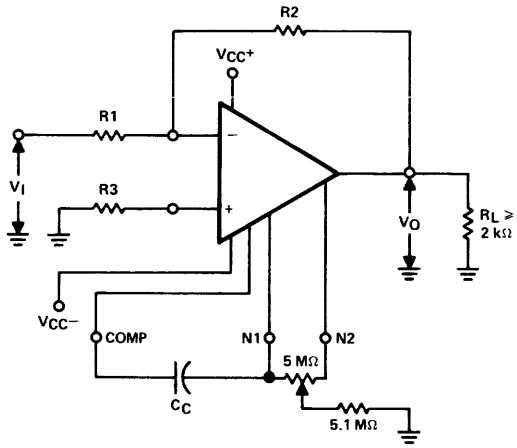
FIGURE 10

TYPICAL APPLICATION DATA



$r_i \approx 5{,}000$ MΩ at 10 Hz $r_o << 1$ Ω
$C_L \approx 1.5$ pF $B_1 \approx 1.3$ MHz

FIGURE 11–UNITY-GAIN VOLTAGE FOLLOWER



$$R3 = \frac{R1 \cdot R2}{R1 + R2} \qquad \frac{V_O}{V_1} = -\frac{R2}{R1} \qquad C_C \geq \frac{R1 \cdot 30\text{ pF}}{R1 + R2}$$

FIGURE 12–INVERTING CIRCUIT WITH ADJUSTABLE GAIN, COMPENSATION, AND OFFSET ADJUSTMENT

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CIRCUIT TYPES SN52771, SN72771
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

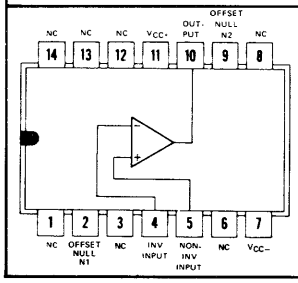
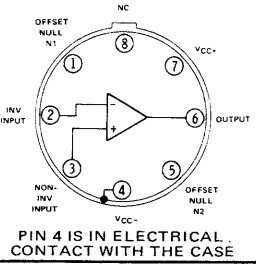
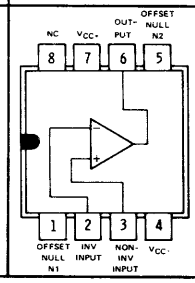
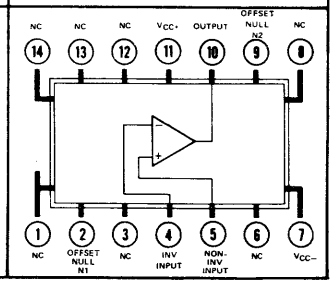
- Very Low Input Bias Currents
- 6-dB Roll-Off Insures Stability
- No Frequency Compensation Required
- Offset-Voltage Null Capability
- Low Power Consumption
- High Slew Rates
- Very Low Input Offset Parameters
- Short-Circuit Protection
- No Latch-Up
- Large Common-Mode and Differential Voltage Ranges

description

The SN52771 and SN72771 are high-performance general purpose integrated-circuit operational amplifiers. Very low input currents make these amplifiers ideal for sample and hold, logarithmic amplifiers, and other low-level applications. High slew rate makes them ideal for fast-rise-time signals, or large signals at high frequency. Internal compensation provides a 6-dB roll-off for stability under all closed-loop conditions. A potentiometer may be connected between the offset null inputs, as shown in Figure 11, to null out the offset voltage.

The SN52771 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72771 is characterized for operation from 0°C to 70°C.

terminal assignments

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)	L PLUG-IN PACKAGE (TOP VIEW)	P DUAL-IN-LINE PACKAGE (TOP VIEW)	Z FLAT PACKAGE (TOP VIEW)
			

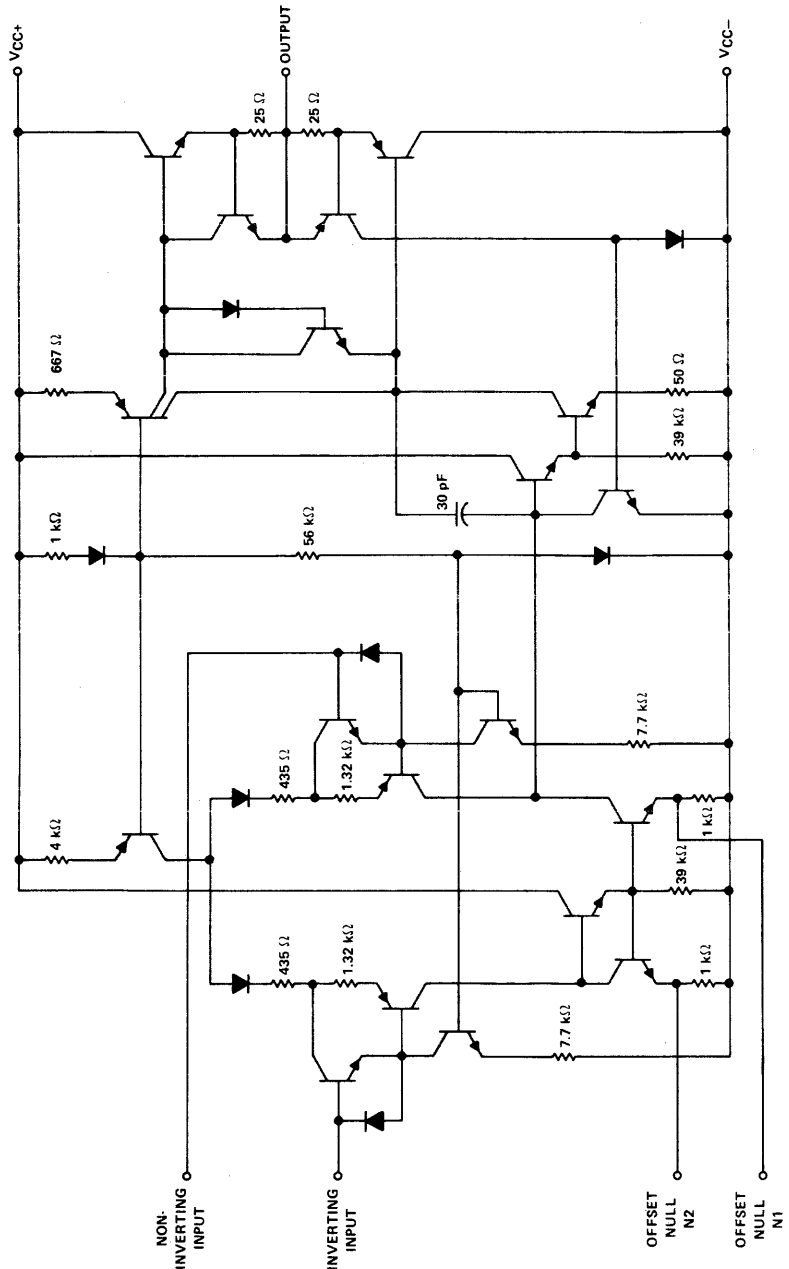
NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52771	SN72771	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		±0.5	±0.5	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation at (or below) 55°C free-air temperature (see Note 5)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, L, or Z Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P Package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the SN52771 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 55°C free-air temperature, refer to Dissipation Derating Curve, Figure 1.

schematic



Component values shown are nominal.

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electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		SN52771			SN72771			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 10$ kΩ	25°C		2	4		5	10	mV
			Full range			7			14	
I_{IO}	Input offset current		25°C		1	2		5	10	nA
			Full range			5			14	
I_{IB}	Input bias current		25°C		8	15		15	30	nA
			Full range			35			40	
V_{ICR}	Common-mode input voltage range		25°C	±12	±14		±11			V
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L = 2 kΩ	25°C	24	26.5		22	26.5		
		$R_L \geq 2$ kΩ	Full range	24			22			
A_{VD}	Large-signal differential voltage amplification	R_L = 2 kΩ, V_O = ±10 V	25°C	50,000	100,000		35,000	100,000		
		$R_L \geq 2$ kΩ, V_O = ±10 V	Full range	25,000			25,000			
B_{OM}	Maximum-output-swing bandwidth (closed loop)	R_L = 2 kΩ, $V_O \geq$ ±10 V, A_{VD} = 1, THD ≤ 5%	25°C		40			40		kHz
B_1	Unity-gain bandwidth		25°C		1.3			1.3		MHz
r_{id}	Differential input resistance		25°C		100			100		MΩ
z_{ic}	Common-mode input impedance	f = 10 Hz	25°C		500			500		MΩ
z_o	Output impedance	f = 10 Hz	25°C		2			2		kΩ
CMRR	Common-mode rejection ratio	$R_S \leq 10$ kΩ	25°C	80	100		70	100		dB
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 10$ kΩ	25°C		80	150			200	μV/V
e_n	Equivalent input noise voltage (closed loop)	A_{VD} = 100, BW = 1 Hz, f = 1 kHz	25°C		40			40		nV/√Hz
I_{OS}	Short-circuit output current	To V_{CC+}	25°C		24			24		mA
		To V_{CC-}			−20			−20		
I_{CC}	Supply current	No load, No signal	25°C		1.3	2		1.7	4	mA
P_D	Total power dissipation	No load, No signal	25°C		40	60		50	120	mW

†All characteristics are specified under open-loop operation unless otherwise noted. Full range for SN52771 is −55°C to 125°C and for SN72771 is 0°C to 70°C.

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN52771			SN72771			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 200 mV, R_L = 2 kΩ, C_L = 200 pF, C_C = 30 pF, See Figure 2		130			130		ns
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 200 pF, C_C = 30 pF, See Figure 2		2.5			2.5		V/μs

For ordering instructions and mechanical data, refer to Section 1.

DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to zero. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at zero volts.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at zero volts.

Common-Mode Input Voltage Range (V_{ICR}) The range of common-mode voltage which if exceeded will cause the amplifier to cease functioning properly.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage which can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

3

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the peak-to-peak output voltage swing to the change in differential input voltage required to drive the output.

Maximum-Output-Swing Bandwidth (B_{OM}) The range of frequencies within which the maximum output voltage swing is above a specified value.

Unity-Gain Bandwidth (B_1) The range of frequencies within which the voltage amplification is greater than unity.

Differential Input Resistance (r_{id}) The small-signal resistance between the two ungrounded input terminals.

Common-Mode Input Impedance (z_{ic}) The parallel sum of the small-signal impedances between each input terminal and ground.

Output Impedance (z_o) The impedance between the output terminal and ground.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Power Supply Sensitivity ($\Delta V_{IO}/\Delta V_{CC}$) The ratio of the change in input offset voltage to the change in supply voltages producing it. For these devices, both supply voltages are varied symmetrically.

Short-Circuit Output Current (I_{OS}) The maximum output current available from the amplifier with the output shorted to the specified supply.

Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Rise Time (t_r) The time required for an output voltage step to change from 10% to 90% of its final value.

Slew Rate (SR) The average time rate of change of the closed-loop amplifier output voltage for a step-signal input. Slew rate is measured between specified output levels (0 and 10 volts for this device) with feedback adjusted for unity gain.

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THERMAL INFORMATION

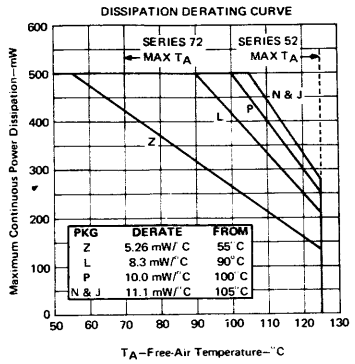


FIGURE 1

PARAMETER MEASUREMENT INFORMATION

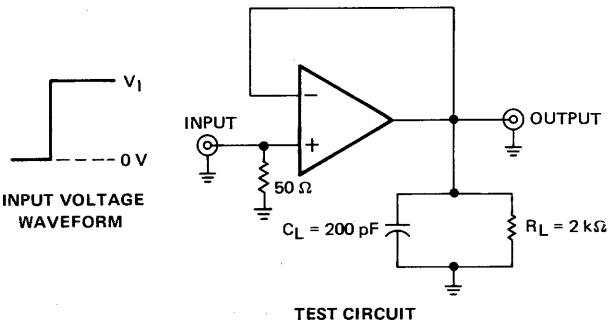


FIGURE 2—BANDWIDTH, RISE TIME, AND SLEW RATE

3

TYPICAL CHARACTERISTICS

SN52771

COMMON-MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

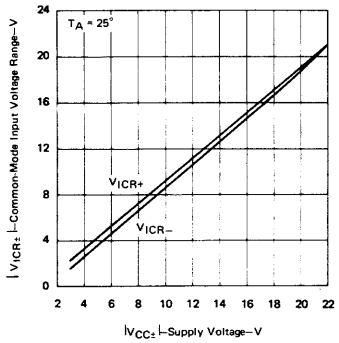


FIGURE 3

MAXIMUM OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE

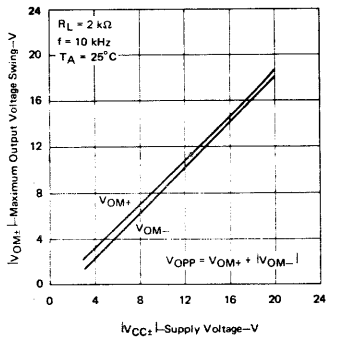


FIGURE 4

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE SWING vs FREQUENCY

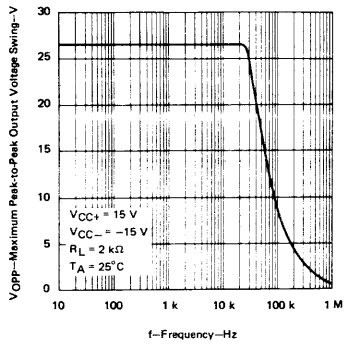


FIGURE 5

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

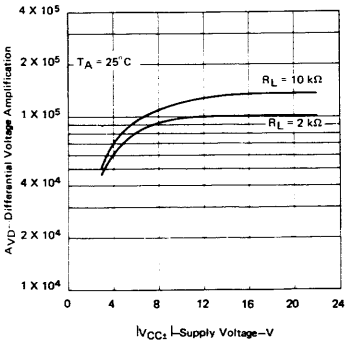


FIGURE 6

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

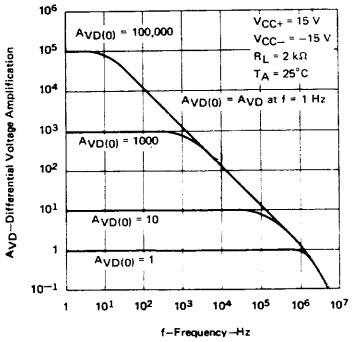


FIGURE 7

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

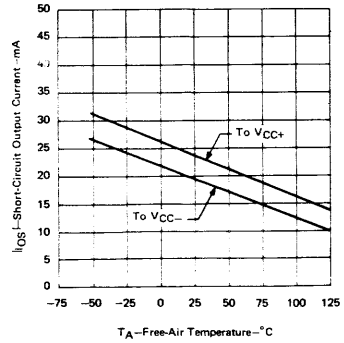


FIGURE 8

TYPICAL CHARACTERISTICS

TOTAL POWER DISSIPATION
vs
SUPPLY VOLTAGE

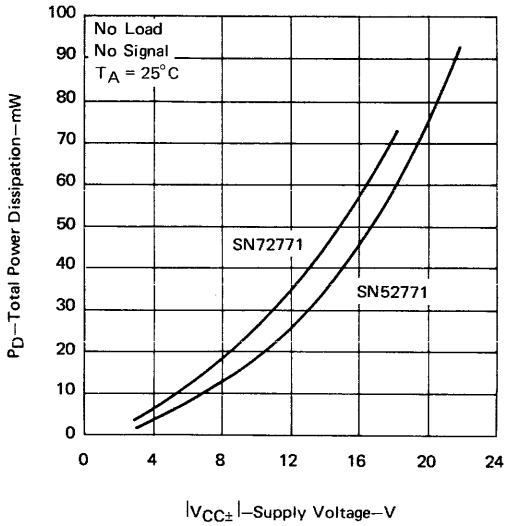


FIGURE 9

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

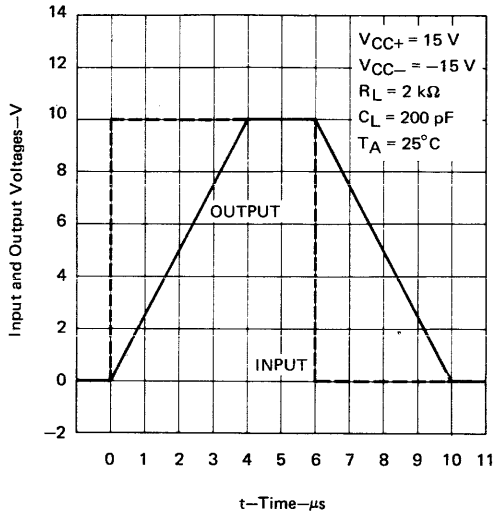
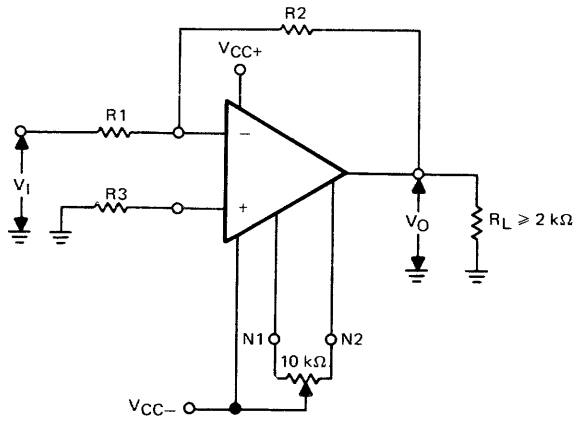


FIGURE 10

TYPICAL APPLICATION DATA



$$R3 = \frac{R1 \cdot R2}{R1 + R2} \qquad \frac{V_O}{V_I} = -\frac{R2}{R1}$$

FIGURE 11—INVERTING CIRCUIT WITH ADJUSTABLE GAIN, COMPENSATION, AND OFFSET ADJUSTMENT

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Series 52 and Series 55

TYPE	SINGLE				DUAL CHANNEL		DUAL				UNIT
	SN52710	SN52510	SN52810	SN52106*	SN52711	SN52811	SN52820	SN52514	SN52506*	SN55107A†	
Input Offset Voltage, Max	5	2	2	2	3.5	3.5	2	2	2	25	mV
Input Offset Current, Max	10	3	3	3	10	3	3	3	3	10	μA
Input Bias Current, Max	75	15	15	20	75	20	15	15	20	75	μA
Voltage Amplification, Min	750	12,500	12,500	40,000 Typ	750	12,500	12,500	12,500	40,000 Typ		
Common-Mode Input Voltage Range, Min	±5	±5	±5	±5	±5	±5	±5	±5	±5	±3	V
Output Sink Current, Min	1.6	2	2	100 Typ	0.5	0.5	2	2	100 Typ	16	mA
Input-Output Response Time, Typ	40	30	30	40	40	33	30	30	40	17	ns
Fan-Out to Series 54 TTL	1	1	1	10	1	1	1	1	10	10	
Power Supplies Required	12	12	12	12	12	12	12	12	12	5	V_{CC+}
	6	6	6	3 to 12	6	6	6	6	3 to 12	5	V_{CC-}
Packages	J, L, N, S	J, L, N, P, Z	J, L, N, P, Z	J, L, N, Z	J, L, N, S	J, L, N	J, N, Z	J, N, Z	N, J, Z	J, N	

3

Series 72 and Series 75

TYPE	SINGLE				DUAL CHANNEL		DUAL					UNIT
	SN72710	SN72510	SN72810	SN72306*	SN72711	SN72811	SN72720	SN72820	SN72514	SN72506*	SN75107A†	
Input Offset Voltage, Max	7.5	3.5	5	5	5	5	7.5	3.5	3.5	5	25	mV
Input Offset Current, Max	15	5	5	5	15	5	15	5	5	5	10	μA
Input Bias Current, Max	100	20	20	25	100	30	100	20	20	25	75	μA
Voltage Amplification, Min	700	10,000	10,000	40,000 Typ	700	10,000	700	10,000	10,000	40,000 Typ		
Common-Mode Input Voltage Range, Min	±5	±5	±5	±5	±5	±5	±5	±5	±5	±5	±3	V
Output Sink Current, Min	1.6	1.6	1.6	100 Typ	0.5	0.5		1.6	1.6	100	16	mA
Input-Output Response Time, Typ	40	30	30	40	40	33	40	30	30	40	17	ns
Fan-Out to Series 74 TTL	1	1	1	10	1	1	1	1	1	10	10	
Power Supplies Required	12	12	12	12	12	12	12	12	12	12	5	V_{CC+}
	6	6	6	3 to 12	6	6	6	6	6	3 to 12	5	V_{CC-}
Packages	J, L, N, S	J, L, N, P, Z	J, L, N, P, Z	J, L, N, Z	J, L, N, S	J, L, N	N	J, N, Z	J, N, Z	J, N, Z	J, N	

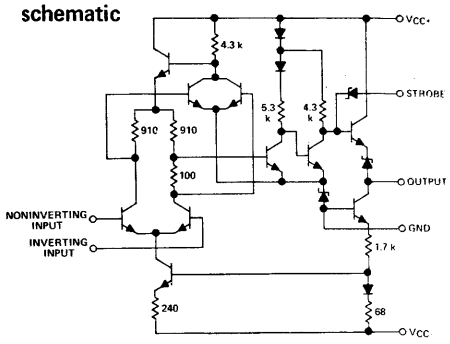
*To be announced soon

†Data sheet in the line circuits section.

CIRCUIT TYPES SN52510, SN72510 DIFFERENTIAL COMPARATORS WITH STROBE

- Low Offset Characteristics
- High Differential Voltage Amplification
- Fast Response Times
- Output Compatible with Most TTL and DTL Circuits

schematic



Resistor values are nominal in ohms.

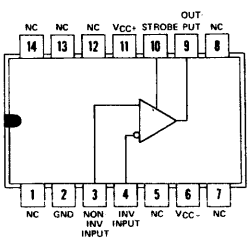
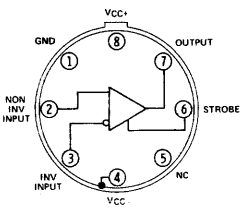
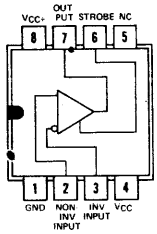
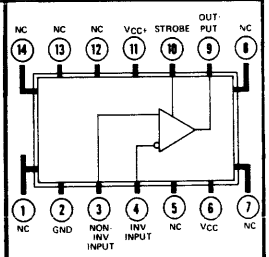
description

The SN52510 and SN72510 monolithic high-speed voltage comparators are improved versions of the SN52710 and SN72710 with an extra stage added to increase voltage amplification and accuracy, and a strobe input for greater flexibility. Typical voltage amplification is 33,000. Since the output cannot be more positive than the strobe, a low-level input at the strobe will cause the output to go low regardless of the differential input. Component matching, inherent in integrated circuit fabrication techniques, produces a comparator with low-drift and low-offset characteristics. These circuits are particularly useful for applications requiring an amplitude discriminator, memory sense amplifier, or a high-speed limit detector.

3

The SN52510 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72510 is characterized for operation from 0°C to 70°C.

terminal assignments

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)	L PLUG-IN PACKAGE (TOP VIEW)	P DUAL-IN-LINE PACKAGE (TOP VIEW)	Z FLAT PACKAGE (TOP VIEW)
	 PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE		

NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	14 V
Supply voltage V_{CC-} (see Note 1)	−7 V
Differential input voltage (see Note 2)	±5 V
Input voltage (either input, see Note 1)	±7 V
Strobe Voltage (see Note 1)	6 V
Peak output current ($t_w \leq 1$ s)	10 mA
Continuous total power dissipation at (or below) 70°C free-air temperature (see Note 3)	300 mW
Operating free-air temperature range: SN52510 Circuits	−55°C to 125°C
SN72510 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J, L, or Z package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N or P package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. For operation of the SN52510 above 70°C free-air temperature, refer to Dissipating Derating Curve, Figure 13.

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electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN52510			SN72510			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$, See Note 4	25°C		0.6	2		1.6	3.5	mV
			Full range			3			4.5	
α_{VIO}	Average temperature coefficient of input offset voltage	R_S = 50 Ω, See Note 4	MIN to 25°C		3	10		3	20	μV/°C
			25°C to MAX		3	10		3	20	
I_{IO}	Input offset current	See Note 4	25°C		0.75	3		1.8	5	μA
			MIN		1.8	7			7.5	
			MAX		0.25	3			7.5	
α_{IIO}	Average temperature coefficient of input offset current	See Note 4	MIN to 25°C		15	75		24	100	nA/°C
			25°C to MAX		5	25		15	50	
I_{IB}	Input bias current	See Note 4	25°C		7	15		7	20	μA
			MIN		12	25		9	30	
I_{SH}	High-level strobe current	$V_{(strobe)}$ = 5 V, V_{ID} = −5 mV	25°C			±100			±100	μA
I_{SL}	Low-level strobe current	$V_{(strobe)}$ = −100 mV, V_{ID} = 5 mV	25°C		−1	−2.5		−1	−2.5	mA
V_{ICR}	Common-mode input voltage range	V_{CC-} = −7 V	Full range	±5			±5			V
V_{ID}	Differential input voltage range		Full range	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	No load, V_O = 0 to 2.5 V	25°C	12,500	33,000		10,000	33,000		
			Full range	10,000			8,000			
V_{OH}	High-level output voltage	V_{ID} = 5 mV, I_{OH} = 0	Full range		4§	5		4§	5	V
		V_{ID} = 5 mV, I_{OH} = −5 mA	Full range	2.5	3.6§		2.5	3.6§		
V_{OL}	Low-level output voltage	V_{ID} = −5 mV, I_{OL} = 0	Full range	−1	−0.5§	0‡	−1	−0.5§	0‡	V
		$V_{(strobe)}$ = 0.3 V, V_{ID} = 5 mV, I_{OL} = 0	Full range	−1		0‡	−1		0‡	V
I_{OL}	Low-level output current	V_{ID} = −5 mV, V_O = 0	25°C	2	2.4		1.6	2.4		mA
			MIN	1	2.3		0.5	2.4		
			MAX	0.5	2.3		0.5	2.4		
r_o	Output resistance	V_O = 1.4 V	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$	Full range	80	100§		70	100§		dB
I_{CC+}	Supply current from V_{CC+}	V_{ID} = −5 mV, No load	Full range		5.5§	9		5.5§	9	mA
I_{CC-}	Supply current from V_{CC-}		Full range		−3.5§	−7		−3.5§	−7	mA
P_D	Total power dissipation		Full range		90§	150		90§	150	mW

†Unless otherwise noted, all characteristics are measured with the strobe open. Full range (MIN to MAX) for SN52510 is −55°C to 125°C and for the SN72510 is 0°C to 70°C.

‡The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

§These typical values are at T_A = 25°C.

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52510, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1V at T_A = 125°C; for SN72510, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at 25°C, and V_O = 1.2 V at T_A = 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Response time	R_L = ∞,	C_L = 5 pF,	See Note 5		30	80	ns
Strobe release time	R_L = ∞,	C_L = 5 pF,	See Note 6		5	25	ns

NOTES: 5. The response time specified is for a 100-mV input step with 5-mV overdrive.

6. For testing purposes, the input bias conditions are selected to produce an output voltage of 1.4 V. A 5-mV overdrive is then added to the input bias voltage to produce an output voltage which rises above 1.4 V. The time interval is measured from the 50% point of the strobe voltage curve to the point where the overdriven output voltage crosses the 1.4 V level.

DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to the specified level. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO}) The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left| \frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at the specified level.

Average Temperature Coefficient of Input Offset Current (α_{IIO}) The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

3

$$\alpha_{IIO} = \left| \frac{(I_{IO} @ T_{A(1)}) - (I_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at the specified level.

High-Level Strobe Current (I_{SH}) The current flowing into or out of the strobe at a high-level voltage.

Low-Level Strobe Current (I_{SL}) The current flowing out of the strobe at a low-level voltage.

Common-Mode Input Voltage Range (V_{ICR}) The range of common-mode voltage which if exceeded will cause the amplifier to cease functioning properly.

Differential Input Voltage Range (V_{ID}) The range of voltage between the two input terminals which if exceeded will cause the comparator to cease functioning properly.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the change in output voltage to the change in differential input voltage producing it.

High-Level Output Voltage (V_{OH}) The voltage at the output with the specified input conditions applied which should establish a high level at the output.

Low-Level Output Voltage (V_{OL}) The voltage at the output with the specified input conditions applied which should establish a low level at the output.

Low-Level Output Current (I_{OL}) The current flowing into the output at a specified low-level output voltage.

Output Resistance (r_o) The resistance between the output terminal and ground.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Response Time The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial condition sufficient to saturate the output to an input level just barely in excess of that required to bring the output back to the logic threshold voltage. This excess is referred to as the voltage overdrive.

Strobe Release Time The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the low logic level to the high logic level. Appropriate input conditions are assumed.

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TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

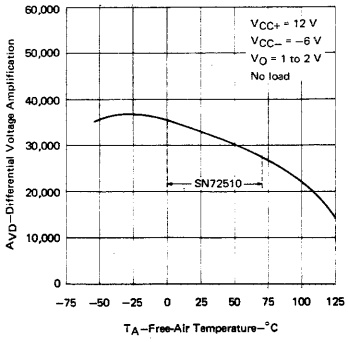


FIGURE 1

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

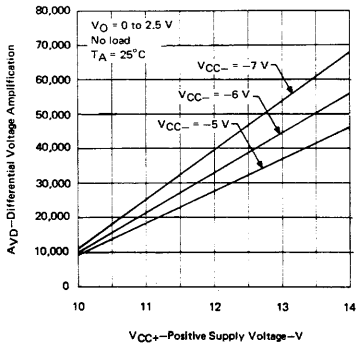


FIGURE 2

OUTPUT VOLTAGE LEVELS vs FREE-AIR TEMPERATURE

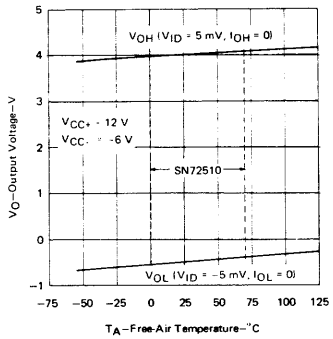


FIGURE 3

LOW-LEVEL OUTPUT CURRENT vs FREE-AIR TEMPERATURE

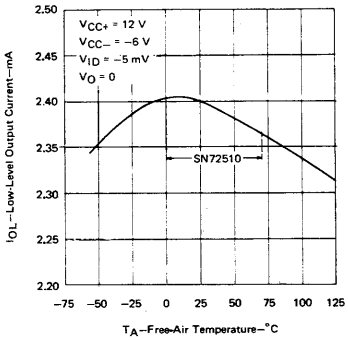


FIGURE 4

SN52510
VOLTAGE TRANSFER CHARACTERISTICS

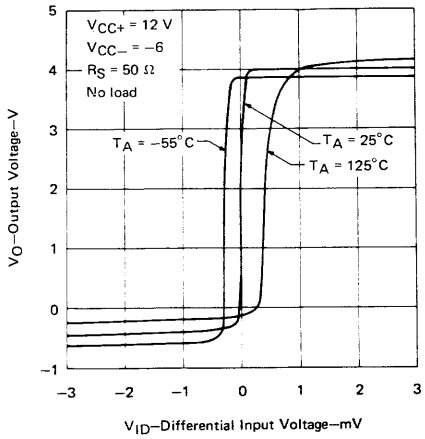


FIGURE 5

SN72510
VOLTAGE TRANSFER CHARACTERISTICS

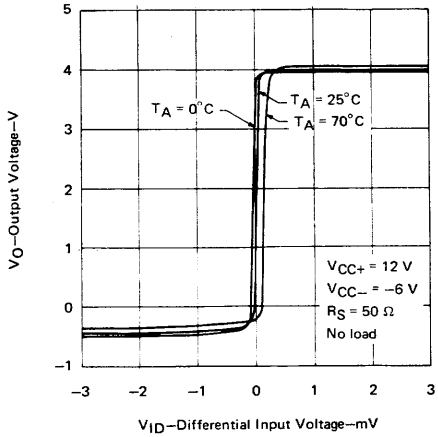


FIGURE 6

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

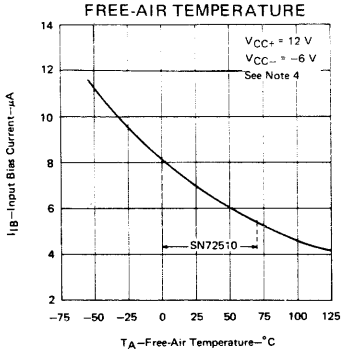


FIGURE 7

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

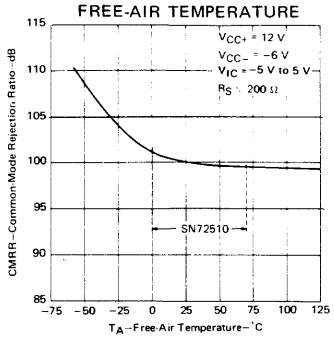


FIGURE 8

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

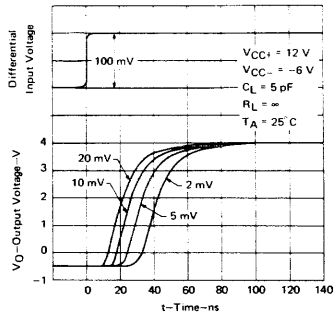


FIGURE 9

STROBE RELEASE TIME
FOR VARIOUS INPUT OVERDRIVES

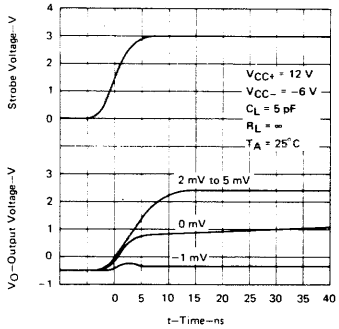


FIGURE 10

COMMON-MODE PULSE RESPONSE

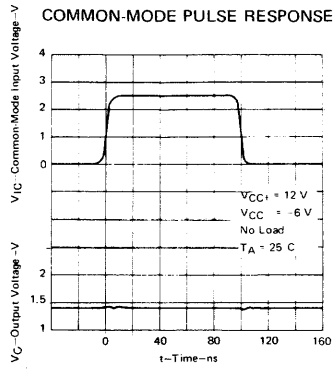
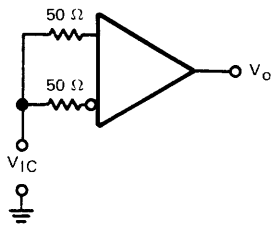


FIGURE 11



TEST CIRCUIT
FOR FIGURE 11

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52510, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1V at T_A = 125°C; for SN72510, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at 25°C, and V_O = 1.2 V at T_A = 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

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TYPICAL CHARACTERISTICS

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

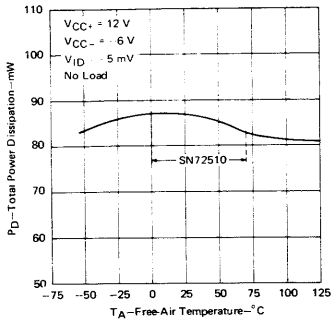
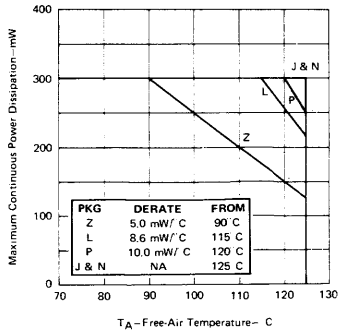


FIGURE 12

3

THERMAL INFORMATION

SN52510
DISSIPATION DERATING CURVE



PKG	DERATE	FROM
Z	5.0 mW/°C	90°C
L	8.6 mW/°C	115°C
P	10.0 mW/°C	120°C
J & N	NA	125°C

FIGURE 13

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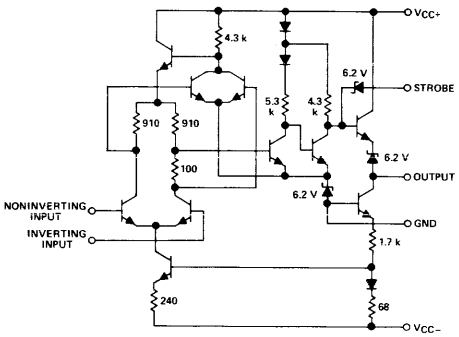
CIRCUIT TYPES SN52514, SN72514
DUAL DIFFERENTIAL COMPARATORS WITH STROBES

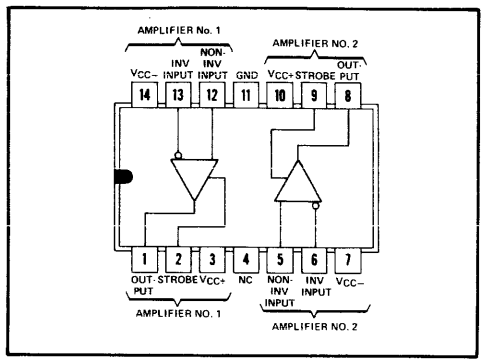
- Fast Response Times
- High Differential Voltage Amplification
- Low Offset Characteristics
- Outputs Compatible with Most TTL and DTL Circuits

schematic (each comparator)



Resistor values are in ohms.
Component values shown are nominal.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection

description

The SN52514 and SN72514 are improved versions of the SN72720 dual high-speed voltage comparator. When compared with the SN72720, these circuits feature higher amplification (typically 33,000) due to an extra amplification stage, increased accuracy because of lower offset characterisitcs, and greater flexibility with the addition of a strobe to each comparator. Since the output cannot be more positive than the strobe, a low-level input at the strobe will cause the output to go low regardless of the differential input.

These circuits are especially useful in applications requiring an amplitude discriminator, memory sense amplifier, or a high-speed limit detector. The SN52514 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72514 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	14 V
Supply voltage V_{CC-} (see Note 1)	−7 V
Differential input voltage (see Note 2)	±5 V
Input voltage (either input, see Note 1)	±7 V
Strobe voltage (see Note 1)	6 V
Peak output current ($t_w \leqslant 1$ s)	10 mA
Continuous total power dissipation: each comparator	300 mW
total package (see Note 3)	600 mW
Operating free-air temperature range: SN52514 Circuits	−55°C to 125°C
SN72714 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. For SN52514, this rating applies at (or below) 95°C free-air temperature. For operation above this temperature, derate linearly at the rate of 10.9 mW/°C. For SN72514, this rating applies at (or below) 70°C free-air temperature without derating.

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electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN52514			SN72514			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$, See Note 4	25°C		0.6	2		1.6	3.5	mV
			Full range			3			4.5	
α_{VIO}	Average temperature coefficient of input offset voltage	R_S = 50 Ω, See Note 4	MIN to 25°C		3	10		3	20	μV/°C
			25°C to MAX		3	10		3	20	
I_{IO}	Input offset current	See Note 4	25°C		0.75	3		1.8	5	μA
			MIN		1.8	7			7.5	
			MAX		0.25	3			7.5	
α_{IIO}	Average temperature coefficient of input offset current	See Note 4	MIN to 25°C		15	75		24	100	nA/°C
			25°C to MAX		5	25		15	50	
I_{IB}	Input bias current	See Note 4	25°C		7	15		7	20	μA
			MIN		12	25		9	30	
I_{SH}	High-level strobe current	$V_{(strobe)}$ = 5 V, V_{ID} = −5 mV	25°C			±100			±100	μA
I_{SL}	Low-level strobe current	$V_{(strobe)}$ = −100 mV, V_{ID} = 5 mV	25°C		−1	−2.5		−1	−2.5	mA
V_{ICR}	Common-mode input voltage range	V_{CC-} = −7 V	Full range	±5			±5			V
V_{ID}	Differential input voltage range		Full range	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	No load, V_O = 0 to 2.5 V	25°C	12,500	33,000		10,000	33,000		
			Full range	10,000			8,000			
V_{OH}	High-level output voltage	V_{ID} = 5 mV, I_{OH} = 0	Full range		4§	5		4§	5	V
		V_{ID} = 5 mV, I_{OH} = −5 mA	Full range	2.5	3.6§		2.5	3.6§		
V_{OL}	Low-level output voltage	V_{ID} = −5 mV, I_{OL} = 0	Full range	−1	−0.5§	0‡	−1	−0.5§	0‡	V
		$V_{(strobe)}$ = 0.3 V, V_{ID} = 5 mV, I_{OL} = 0	Full range	−1		0‡	−1		0‡	V
I_{OL}	Low-level output current	V_{ID} = −5 mV, V_O = 0	25°C	2	2.4		1.6	2.4		mA
			MIN	1	2.3		0.5	2.4		
			MAX	0.5	2.3		0.5	2.4		
r_o	Output resistance	V_O = 1.4 V	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$	Full range	80	100§		70	100§		dB
I_{CC+}	Supply current from V_{CC+} ¶	V_{ID} = −5 mV, No load	Full range		5.5§	9		5.5§	9	mA
I_{CC-}	Supply current from V_{CC-} ¶		Full range		−3.5§	−7		−3.5§	−7	mA
P_D	Total power dissipation ¶		Full range		90§	150		90§	150	mW

†Unless otherwise noted, all characteristics are measured with the strobe open. Full range (MIN to MAX) for SN52514 is −55°C to 125°C and for the SN72514 is 0°C to 70°C.

‡The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

§These typical values are at T_A = 25°C.

¶Suppy current and power dissipation limits apply for each comparator.

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52514, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1V at T_A = 125°C; for SN72514, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at 25°C, and V_O = 1.2 V at T_A = 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Response time	R_L = ∞,	C_L = 5 pF,	See Note 5		30	80	ns
Strobe release time	R_L = ∞,	C_L = 5 pF,	See Note 6		5	25	ns

NOTES: 5. The response time specified is for a 100-mV input step with 5-mV overdrive.

6. For testing purposes, the input bias conditions are selected to produce an output voltage of 1.4 V. A 5-mV overdrive is then added to the input bias voltage to produce an output voltage which rises above 1.4 V. The time interval is measured from the 50% point of the strobe voltage curve to the point where the overdriven output voltage crosses the 1.4 V level.

For definition of terms and typical characteristic curves, see the SN52510/SN72510 data sheet on page 3-60.

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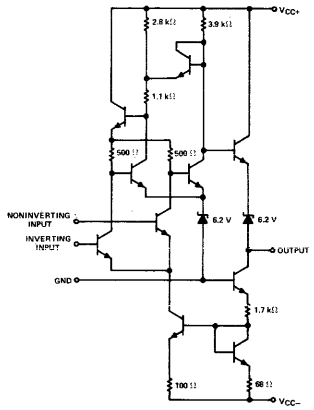
CIRCUIT TYPES SN52710, SN72710
DIFFERENTIAL COMPARATORS

- Fast Response Times
- Low Offset Characteristics
- Output Compatible with Most TTL and DTL Circuits

description

The SN52710 and SN72710 are monolithic high-speed comparators having differential inputs and a low-impedance output. Component matching, inherent in silicon integrated circuit fabrication techniques, produces a comparator with low-drift and low-offset characteristics. These circuits are especially useful for applications requiring an amplitude discriminator, memory sense amplifier, or a high-speed voltage comparator. The SN52710 is characterised for operation over the full military temperature range of −55°C to 125°C; the SN72710 is characterized for operation from 0°C to 70°C.

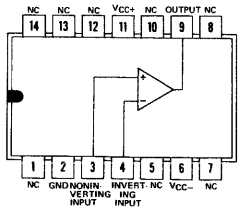
schematic



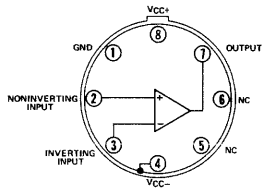
Component values shown are nominal.

terminal assignments

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

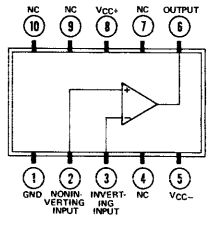


L
PLUG-IN PACKAGE (TOP VIEW)



PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

S
FLAT PACKAGE (TOP VIEW)



PIN 5 IS IN ELECTRICAL CONTACT WITH THE CASE

NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52710	SN72710	UNIT
Supply voltage V_{CC+} (see Note 1)		14	14	V
Supply voltage V_{CC-} (see Note 1)		−7	−7	V
Differential input voltage (see Note 2)		±5	±5	V
Input voltage (either input, see Note 1)		±7	±7	V
Peak output current ($t_w \leq 1$ s)		10	10	mA
Continuous total power dissipation at (or below) 70°C free-air temperature (see Note 3)		300	300	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, L, or S package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N package	260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. For operation of the SN52710 above 70°C free-air temperature, refer to Dissipation Derating Curve, Figure 8.

TEXAS INSTRUMENTS
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electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN52710			SN72710			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$, See Note 4	25°C		2	5		2	7.5	mV
			Full range			6			10	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S \leq 200\ \Omega$, See Note 4	Full range		5			7.5		μV/°C
I_{IO}	Input offset current	See Note 4	25°C		1	10		1	15	μA
			Full range			20			25	
I_{IB}	Input bias current	See Note 4	25°C		25	75		25	100	μA
			Full range			150			150	
V_I	Input voltage range	V_{CC-} = −7 V	25°C	±5			±5			V
V_{ID}	Differential input voltage range		25°C	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	No load, See Note 4	25°C	750	1500		700	1500		
			Full range	500			500			
V_{OH}	High-level output voltage	V_{ID} = 15 mV, I_{OH} = −0.5 mA	25°C	2.5	3.2	4	2.5	3.2	4	V
V_{OL}	Low-level output voltage	V_{ID} = −15 mV, I_{OL} = 0	25°C	−1	−0.5	0‡	−1	−0.5	0‡	V
I_{OL}	Low-level output current	V_{ID} = −15 mV, V_O = 0	25°C	1.6	2.5					mA
r_o	Output resistance	V_O = 1.4 V	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$	25°C	70	90		65	90		dB
I_{CC+}	Supply current from V_{CC+}	V_{ID} = −5 V to 5 V (−10 mV for typ), No load	25°C		5.4	10.1		5.4		mA
I_{CC-}	Supply current from V_{CC-}		25°C		−3.8	−8.9		−3.8		mA
P_D	Total power dissipation		25°C		88	175		88		mW

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52710, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1 V at T_A = 125°C; for SN72710, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1.2 V at T_A = 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

†Full range for SN52710 is −55°C to 125°C and for SN72710 is 0°C to 70°C.

‡The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	SN52710	SN72710	UNIT
		TYP	TYP	
Response time	No load, See Note 5	40	40	ns

NOTE 5: The response time specified is for a 100-mV input step with 5-mV overdrive.

For definitions of terms, mechanical data and ordering instructions, see SN52711/SN72711 data sheet dated February 1971.

TYPICAL CHARACTERISTICS

OUTPUT RESPONSE FOR VARIOUS
INPUT OVERDRIVES

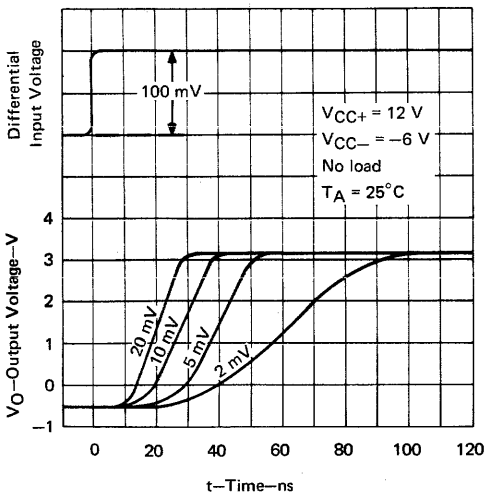

FIGURE 1

OUTPUT RESPONSE FOR VARIOUS
INPUT OVERDRIVES

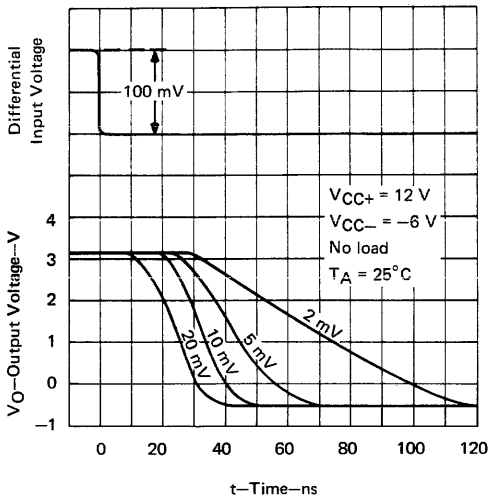

FIGURE 2

COMMON-MODE PULSE RESPONSE
vs
ELAPSED TIME

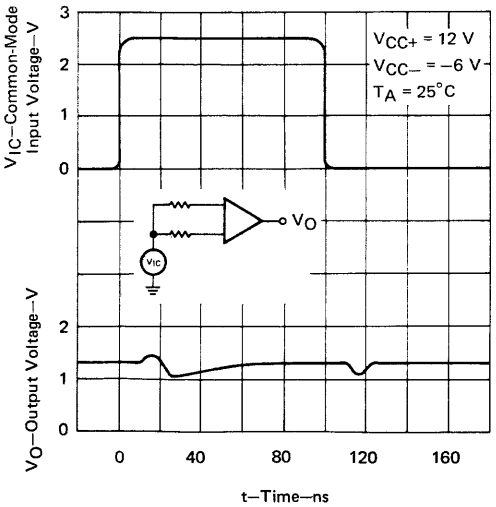

FIGURE 3

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

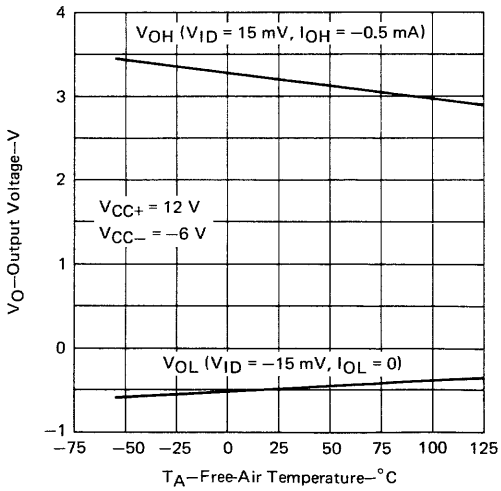

FIGURE 4

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TYPICAL CHARACTERISTICS

SN52710
VOLTAGE TRANSFER CHARACTERISTICS

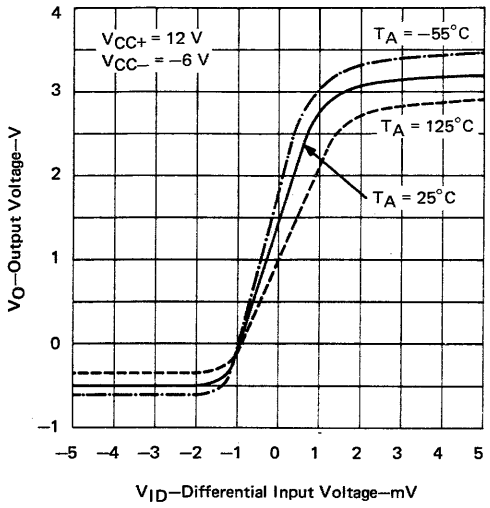


FIGURE 5

SN72710
VOLTAGE TRANSFER CHARACTERISTICS

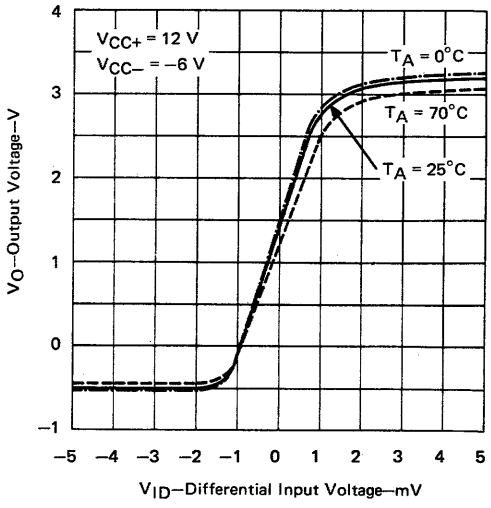


FIGURE 6

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

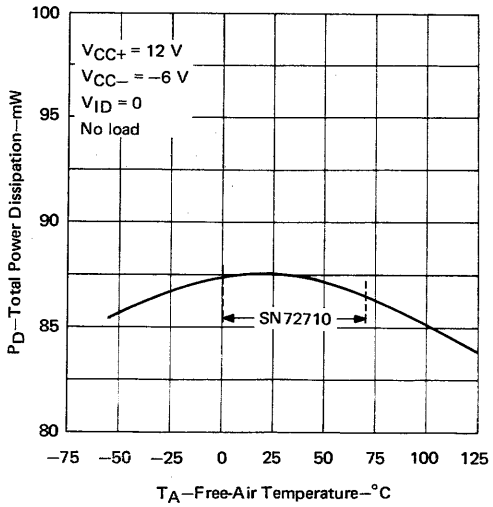


FIGURE 7

THERMAL INFORMATION

DISSIPATION DERATING CURVE

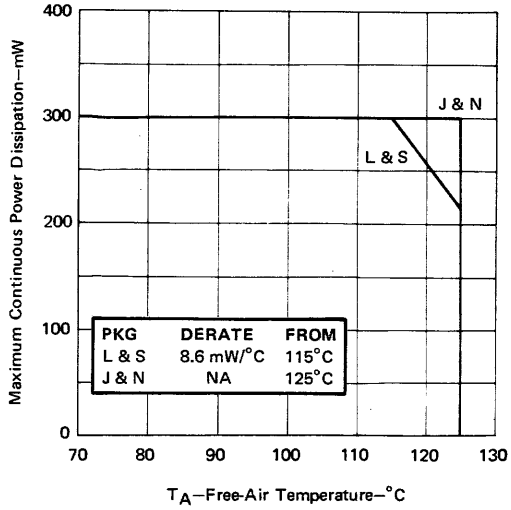


FIGURE 8

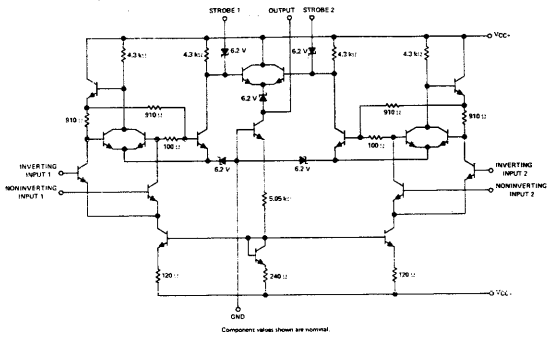
CIRCUIT TYPES SN52711, SN72711 DUAL-CHANNEL DIFFERENTIAL COMPARATORS WITH STROBES

- Fast Response Times
- Low Offset Characteristics
- Output Compatible with Most TTL and DTL Circuits
- Designed to be Interchangeable with Fairchild μA711 and μA711C

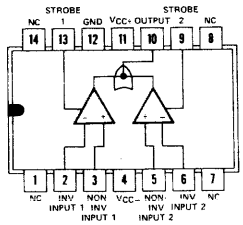
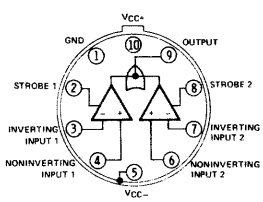
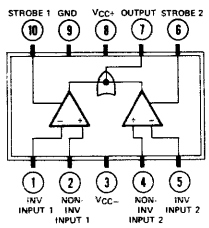
description

The SN52711 and SN72711 circuits are high-speed dual-channel comparators with differential inputs and a low-impedance output. Component matching, inherent with silicon monolithic circuit fabrication techniques, produces a comparator circuit with low-drift and low-offset characteristics. An independent strobe input is provided for each of the two channels, which when taken low, inhibits the associated channel. If both strobes are simultaneously low, the output will be low regardless of the conditions applied to the differential inputs. The comparator output puise width may be "stretched" by varying the capacitive loading. These dual comparators are particularly useful for applications requiring an amplitude-discriminating sense amplifier with an adjustable threshold voltage. The SN52711 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72711 is characterized for operation from 0°C to 70°C.

schematic



terminal assignments

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)	L PLUG-IN PACKAGE (TOP VIEW)	S FLAT PACKAGE (TOP VIEW)
		
	PIN 5 IS IN ELECTRICAL CONTACT WITH THE CASE	PIN 3 IS IN ELECTRICAL CONTACT WITH THE CASE

NC—No Internal Connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52711	SN72711	UNIT
Supply voltage V_{CC+} (see Note 1)		14	14	V
Supply voltage V_{CC-} (see Note 1)		−7	−7	V
Differential input voltage (see Note 2)		±5	±5	V
Input voltage (either input, see Note 1)		±7	±7	V
Strobe voltage (see Note 1)		6	6	V
Peak output current ($t_w \leq 1$ s)		50	50	mA
Continuous total power dissipation at (or below) 70°C free-air temperature (see Note 3)		300	300	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, L, or S package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N package	260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. For operation of SN52711 above 70°C free-air temperature, refer to Dissipation Derating Curve, Figure 9.

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electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN52711			SN72711			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$, V_{IC} = 0, See Note 4	25°C		1	3.5		1	5	mV
			Full range			4.5			6	
		$R_S \leq 200\ \Omega$, See Note 4	25°C		1	5		1	7.5	
			Full range			6			10	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S \leq 200\ \Omega$, V_{IC} = 0, See Note 4	Full range		5			5		μV/°C
I_{IO}	Input offset current	See Note 4	25°C		0.5	10		0.5	15	μA
			Full range			20			25	
I_{IB}	Input bias current	See Note 4	25°C		25	75		25	100	μA
			Full range			150			150	
I_{SL}	Low-level strobe current	$V_{(strobe)}$ = 0, V_{ID} = 10 mV	25°C		−1.2	−2.5		−1.2	−2.5	mA
V_I	Input voltage range	V_{CC-} = −7 V	25°C	±5			±5			V
V_{ID}	Differential input voltage range		25°C	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	No load, V_O = 0 to 2.5 V	25°C	750	1500		700	1500		
			Full range	500			500			
V_{OH}	High-level output voltage	V_{ID} = 10 mV, I_{OH} = 0	25°C		4.5	5		4.5	5	V
		V_{ID} = 10 mV, I_{OH} = −5 mA	25°C	2.5	3.5		2.5	3.5		
V_{OL}	Low-level output voltage	V_{ID} = −10 mV, I_{OL} = 0	25°C	−1	−0.5	0‡	−1	−0.5	0‡	V
		V_{ID} = 10 mV, $V_{(strobe)}$ = 0.3 V, I_{OL} = 0	25°C	−1		0‡	−1		0‡	
I_{OL}	Low-level output current	V_{ID} = −10 mV, V_O = 0	25°C	0.5	0.8		0.5	0.8		mA
r_o	Output resistance	V_O = 1.4 V	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$	25°C	70	90		65	90		dB
I_{CC+}	Supply current from V_{CC+}	V_{ID} = −5 V to 5 V (−10 mV for typ), Strobes alternately grounded, No load	25°C		9			9		mA
I_{CC-}	Supply current from V_{CC-}		25°C		−4			−4		mA
P_D	Total power dissipation		25°C		130	200		130	230	mW

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52711, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1 V at T_A = 125°C; for SN72711, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1.2 V at 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

†Unless otherwise noted, all characteristics are measured with the strobe of the channel under test open. The strobe of the other channel is grounded. Full range for SN52711 is −55°C to 125°C and for the SN72711 is 0°C to 70°C.

‡The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		SN52711			SN72711			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Response time	No load,	See Note 5		40	80		40		ns
Strobe release time	No load,	See Note 6		7	25		7		ns

NOTES: 5. The response time specified is for a 100-mV input step with 5-mV overdrive.

6. For testing purposes, the input bias conditions are selected to produce an output voltage of 1.4 V. A 5-mV overdrive is then added to the input bias voltage to produce an output voltage which rises above 1.4 V. The time interval is measured from the 50% point of the strobe voltage curve to the point where the overdriven output voltage crosses the 1.4 V level.

DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to the specified level. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO}) The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left| \frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at the specified level.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at the specified level.

3

Low-Level Strobe Current (I_{SL}) The current flowing out of the strobe at a low-level voltage.

Input Voltage Range (V_I) The range of voltage which if exceeded at either input terminal will cause the comparator to cease functioning properly.

Differential Input Voltage Range (V_{ID}) The range of voltage between the two input terminals which if exceeded will cause the comparator to cease functioning properly.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the change in output voltage to the change in differential input voltage producing it.

High-Level Output Voltage (V_{OH}) The voltage at the output with the specified input conditions applied which should establish a high level at the output.

Low-Level Output Voltage (V_{OL}) The voltage at the output with the specified input conditions applied which should establish a low level at the output.

Low-Level Output Current (I_{OL}) The current flowing into the output at a specified low-level output voltage.

Output Resistance (r_o) The resistance between the output terminal and ground.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Response Time The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial condition sufficient to saturate the output to an input level just barely in excess of that required to bring the output back to the logic threshold voltage. This excess is referred to as the voltage overdrive.

Strobe Release Time The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the low logic level to the high logic level. Appropriate input conditions are assumed.

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TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

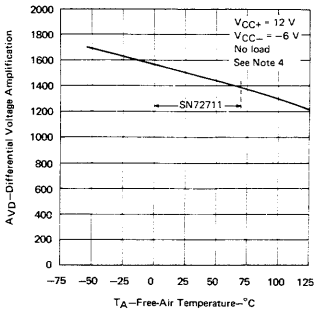

FIGURE 1

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

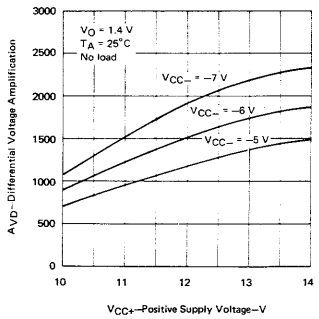

FIGURE 2

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

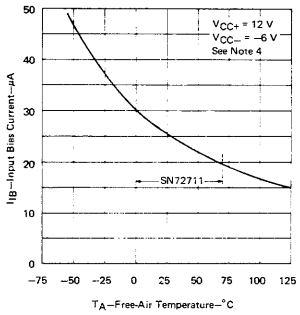

FIGURE 3

TOTAL POWER DISSIPATION vs FREE-AIR TEMPERATURE

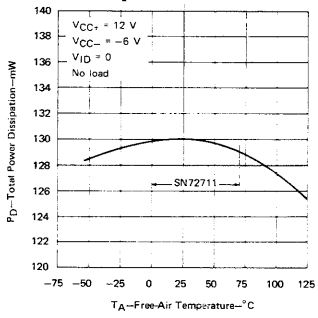

FIGURE 4

SN52711 VOLTAGE TRANSFER CHARACTERISTICS

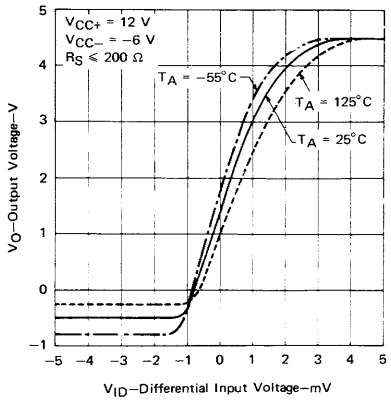

FIGURE 5

SN72711 VOLTAGE TRANSFER CHARACTERISTICS

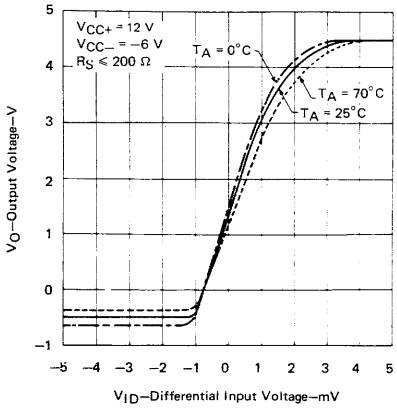

FIGURE 6

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52711, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1 V at T_A = 125°C; for SN72711, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1.2 V at 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

TYPICAL CHARACTERISTICS

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

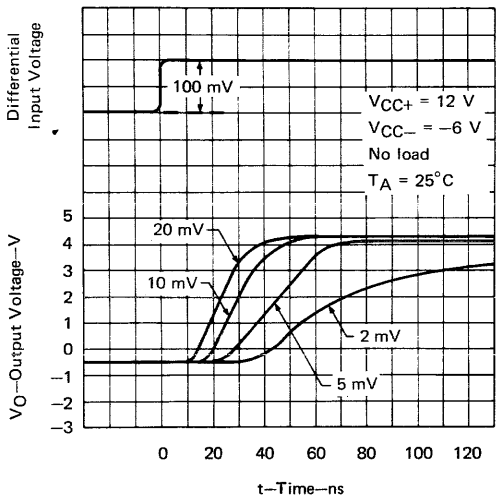

FIGURE 7

STROBE RELEASE TIME
FOR VARIOUS INPUT OVERDRIVES

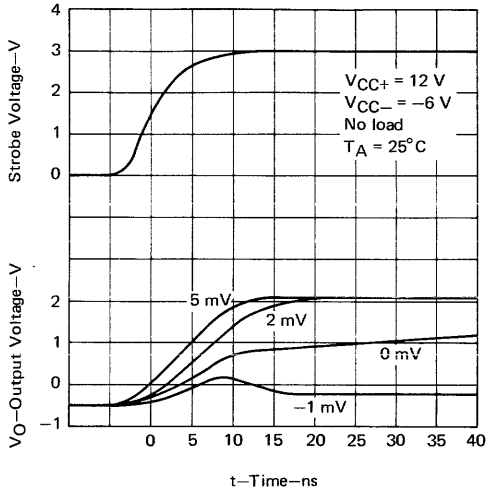

FIGURE 8

THERMAL INFORMATION

SN52711
DISSIPATION DERATING CURVE

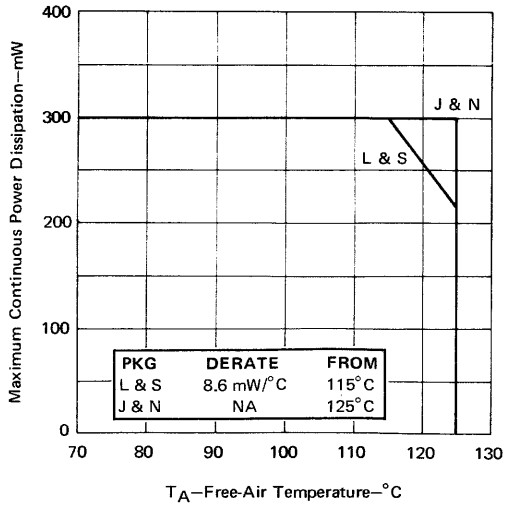

FIGURE 9

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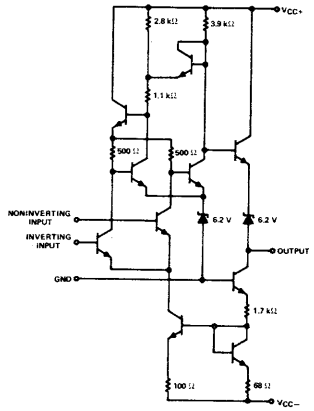
CIRCUIT TYPE SN72720
DUAL DIFFERENTIAL COMPARATORS

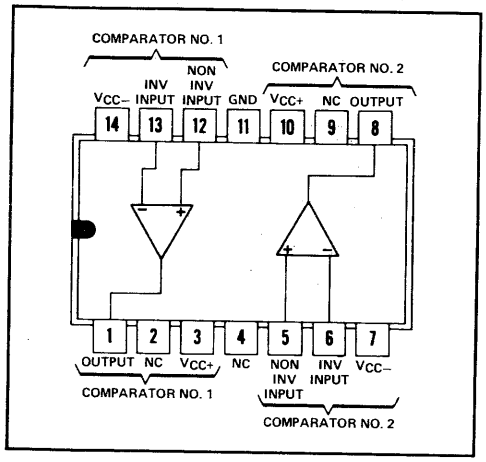
- Fast Response Times
- Low Offset Characteristics
- Output Compatible with Most TTL and DTL Circuits

schematic (each comparator)



Component values shown are nominal.

N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection

description

The SN72720 is two high-speed comparators in a single package, each electrically identical to the SN72710 and having differential inputs and a low-impedance output. Component matching, inherent in silicon monolithic circuit fabrication techniques, produces a comparator with low-drift and low-offset characteristics. This circuit is especially useful for applications requiring an amplitude discriminator, memory sense amplifier, or a high-speed voltage comparator. The SN72720 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	14 V
Supply voltage V_{CC-} (see Note 1)	−7 V
Differential input voltage (see Note 2)	±5 V
Input voltage (either input, see Note 1)	±7 V
Peak output current, each comparator ($t_W \leq 1$ s)	10 mA
Continuous total power dissipation: each comparator	300 mW
total package	600 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 10 seconds	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.

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CIRCUIT TYPE SN72720
DUAL DIFFERENTIAL COMPARATORS

electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$, See Note 3	25°C		2	7.5	mV
			0°C to 70°C			10	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S \leq 200\ \Omega$, See Note 3	0°C to 70°C		7.5		μV/°C
I_{IO}	Input offset current	See Note 3	25°C		1	15	μA
			0°C to 70°C			25	
I_{IB}	Input bias current	See Note 3	25°C		25	100	μA
			0°C to 70°C			150	
V_I	Input voltage range	V_{CC-} = −7 V	25°C	±5			V
V_{ID}	Differential input voltage range		25°C	±5			V
A_{VD}	Large-signal differential voltage amplification	No load, See Note 3	25°C	700	1500		
			0°C to 70°C	500			
V_{OH}	High-level output voltage	V_{ID} = 15 mV, I_{OH} = −0.5 mA	25°C	2.5	3.2	4	V
V_{OL}	Low-level output voltage	V_{ID} = −15 mV, I_{OL} = 0	25°C	−1	−0.5	0‡	V
r_o	Output resistance	V_O = 1.4 V	25°C		200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$	25°C	65	90		dB
I_{CC+}	Supply current from V_{CC+} (each comparator)	V_{ID} = −5 V to 5 V (−10 mV for typ), No load	25°C		5.4		mA
I_{CC-}	Supply current from V_{CC-} (each comparator)		25°C		−3.8		mA
P_D	Total power dissipation (each comparator)		25°C		88		mW

NOTE 3: These characteristics are verified by measurements at the following temperatures and output voltage levels: V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1.2 V at T_A = 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

‡The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
Response time	No load, See Note 4	40	ns

NOTE 4: The response time specified is for a 100-mV input step with 5-mV overdrive.

For definition of terms, refer to page of the SN52711/SN72711 data sheet. Typical characteristic curves on the SN72710 data sheet, pages 3-70 and 3-71, are applicable for the SN72720.

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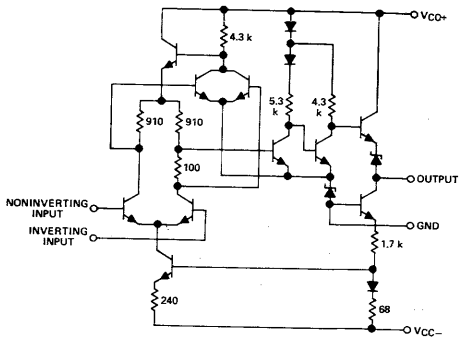
CIRCUIT TYPES SN52810, SN72810
DIFFERENTIAL COMPARATORS

- Low Offset Characteristics
- High Differential Voltage Amplification
- Fast Response Times
- Output Compatible with Most TTL and DTL Circuits

schematic



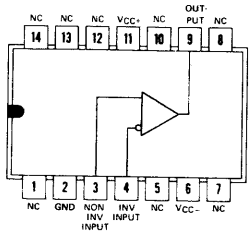
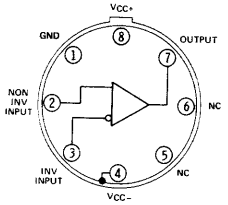
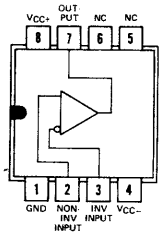
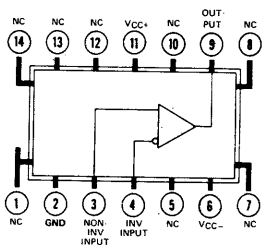
Resistor values are nominal in ohms.

description

The SN52810 and SN72810 are improved versions of the SN52710 and SN72710 high-speed voltage comparators with an extra stage added to increase voltage amplification and accuracy. Typical amplification is 33,000. Component matching, inherent in monolithic integrated circuit fabrication techniques, produces a comparator with low-drift and low-offset characteristics. These circuits are particularly useful for applications requiring an amplitude discriminator, memory sense amplifier, or a high-speed limit detector.

The SN52810 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72810 is characterized for operation from 0°C to 70°C.

terminal assignments

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)	L PLUG-IN PACKAGE (TOP VIEW)	P DUAL-IN-LINE PACKAGE (TOP VIEW)	Z FLAT PACKAGE (TOP VIEW)
	 PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE		

NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	14 V
Supply voltage V_{CC-} (see Note 1)	−7 V
Differential input voltage (see Note 2)	±5 V
Input voltage (either input, see Note 1)	±7 V
Peak output current ($t_w \leq 1$ s)	10 mA
Continuous total power dissipation at (or below) 70°C free-air temperature (see Note 3)	300 mW
Operating free-air temperature range: SN52810 Circuits	−55°C to 125°C
SN72810 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J, L, or Z package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N or P package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. For operation of the SN52810 above 70°C free-air temperature, refer to Dissipating Derating Curve, Figure 1.

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electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN52810 MIN	SN52810 TYP	SN52810 MAX	SN72810 MIN	SN72810 TYP	SN72810 MAX	UNIT
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$, See Note 4	25°C		0.6	2		1.6	3.5	mV
			Full range			3			4.5	
α_{VIO}	Average temperature coefficient of input offset voltage	R_S = 50 Ω, See Note 4	MIN to 25°C		3	10		3	20	μV/°C
			25°C to MAX		3	10		3	20	
I_{IO}	Input offset current	See Note 4	25°C		0.75	3		1.8	5	μA
			MIN		1.8	7			7.5	
			MAX		0.25	3			7.5	
α_{IIO}	Average temperature coefficient of input offset current	See Note 4	MIN to 25°C		15	75		24	100	nA/°C
			25°C to MAX		5	25		15	50	
I_{IB}	Input bias current	See Note 4	25°C		7	15		7	20	μA
			MIN		12	25		9	30	
V_{ICR}	Common-mode input voltage range	V_{CC-} = −7 V	Full range	±5			±5			V
V_{ID}	Differential input voltage range		Full range	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	No load, V_O = 0 to 2.5 V	25°C	12,500	33,000		10,000	33,000		
			Full range	10,000			8,000			
V_{OH}	High-level output voltage	V_{ID} = 5 mV, I_{OH} = 0	Full range		4§	5		4§	5	V
		V_{ID} = 5 mV, I_{OH} = −5 mA	Full range	2.5	3.6§		2.5	3.6§		
V_{OL}	Low-level output voltage	V_{ID} = −5 mV, I_{OL} = 0	Full range	−1	−0.5§	0‡	−1	−0.5§	0‡	V
I_{OL}	Low-level output current	V_{ID} = −5 mV, V_O = 0	25°C	2	2.4		1.6	2.4		mA
			MIN	1	2.3		0.5	2.4		
			MAX	0.5	2.3		0.5	2.4		
r_o	Output resistance	V_O = 1.4 V	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$	Full range	80	100§		70	100§		dB
I_{CC+}	Supply current from V_{CC+}	V_{ID} = −5 mV, No load	Full range		5.5§	9		5.5§	9	mA
I_{CC-}	Supply current from V_{CC-}		Full range		−3.5§	−7		−3.5§	−7	mA
P_D	Total power dissipation		Full range		90§	150		90§	150	mW

†Full range (MIN to MAX) for SN52810 is −55°C to 125°C and for the SN72810 is 0°C to 70°C.

‡The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

§These typical values are at T_A = 25°C.

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52810, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1V at T_A = 125°C; for SN72810, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at 25°C, and V_O = 1.2 V at T_A = 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Response time	R_L = ∞,	C_L = 5 pF,	See Note 5		30	80	ns

NOTE 5: The response time specified is for a 100-mV input step with 5-mV overdrive.

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DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to the specified level. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO}) The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left| \frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at the specified level.

Average Temperature Coefficient of Input Offset Current (α_{IIO}) The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{IIO} = \left| \frac{(I_{IO} @ T_{A(1)}) - (I_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

3

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at the specified level.

Input Voltage Range (V_I) The range of voltage which if exceeded at either input terminal will cause the comparator to cease functioning properly.

Differential Input Voltage Range (V_{ID}) The range of voltage between the two input terminals which if exceeded will cause the comparator to cease functioning properly.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the change in output voltage to the change in differential input voltage producing it.

High-Level Output Voltage (V_{OH}) The voltage at the output with the specified input conditions applied which should establish a high level at the output.

Low-Level Output Voltage (V_{OL}) The voltage at the output with the specified input conditions applied which should establish a low level at the output.

Low-Level Output Current (I_{OL}) The current flowing into the output at a specified low-level output voltage.

Output Resistance (r_o) The resistance between the output terminal and ground.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Response Time The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial condition sufficient to saturate the output to an input level just barely in excess of that required to bring the output back to the logic threshold voltage. This excess is referred to as the voltage overdrive.

THERMAL INFORMATION

SN52810
DISSIPATION DERATING CURVE

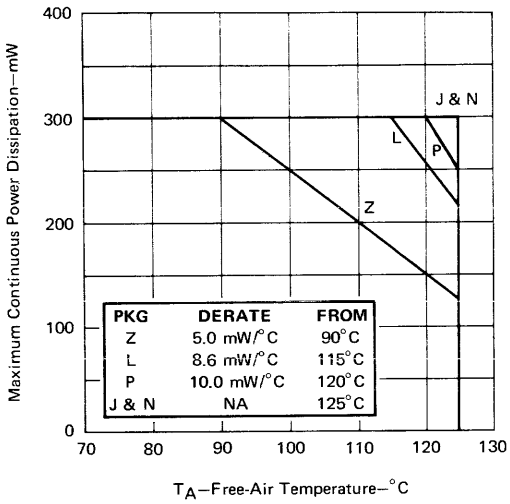

FIGURE 1

TYPICAL CHARACTERISTICS

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

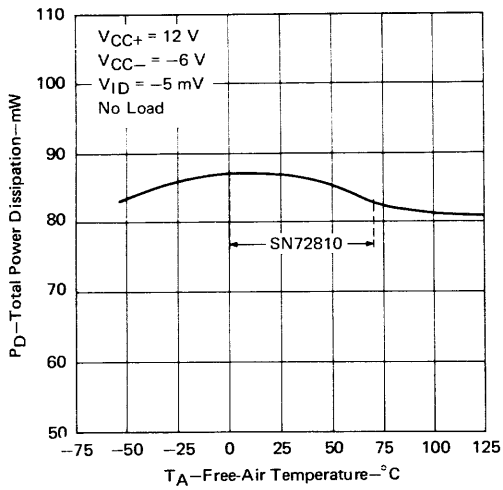

FIGURE 2

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TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

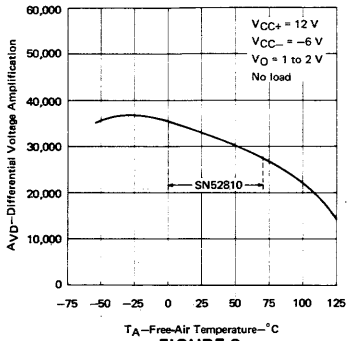


FIGURE 3

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

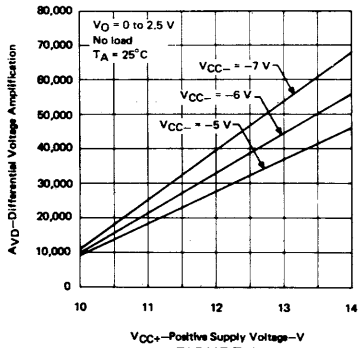


FIGURE 4

OUTPUT VOLTAGE LEVELS vs FREE-AIR TEMPERATURE

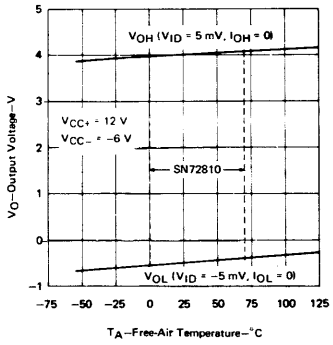


FIGURE 5

LOW-LEVEL OUTPUT CURRENT vs FREE-AIR TEMPERATURE

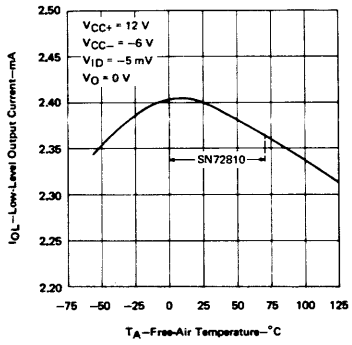


FIGURE 6

SN52810 VOLTAGE TRANSFER CHARACTERISTICS

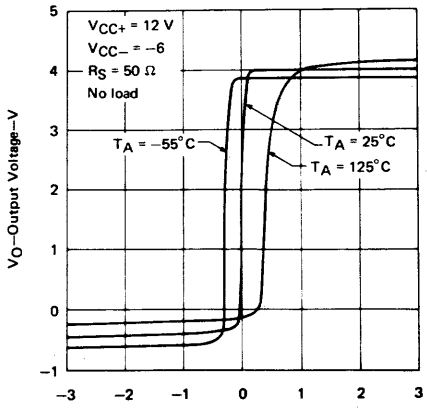


FIGURE 7

SN72810 VOLTAGE TRANSFER CHARACTERISTICS

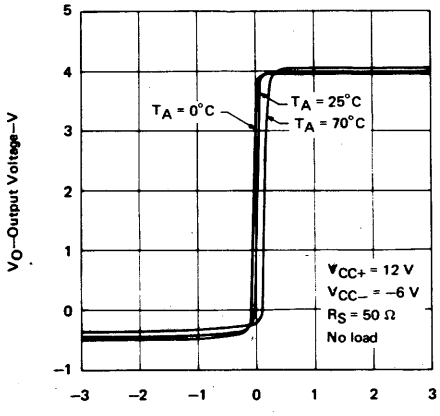


FIGURE 8

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

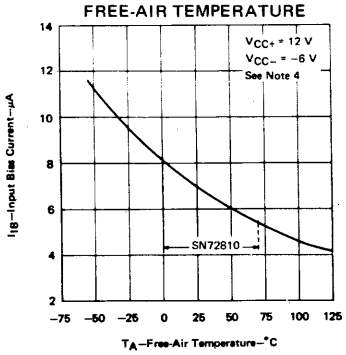


FIGURE 9

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

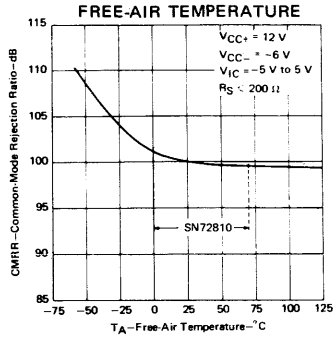


FIGURE 10

3

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

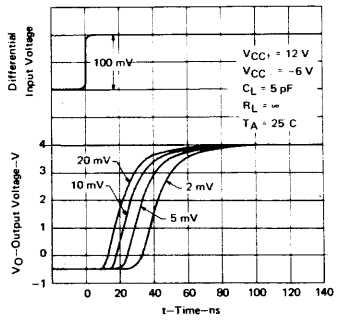


FIGURE 11

COMMON-MODE PULSE RESPONSE

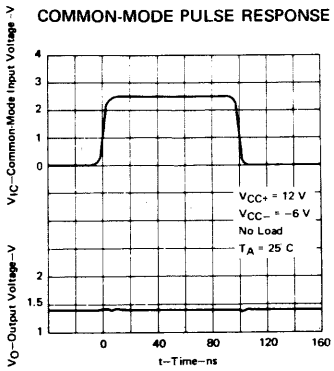
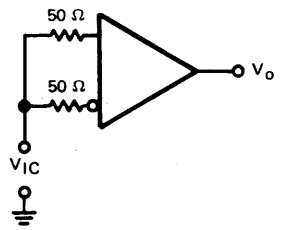


FIGURE 12



TEST CIRCUIT
FOR FIGURE 12

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52810, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1V at T_A = 125°C; for SN72810, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at 25°C, and V_O = 1.2 V at T_A = 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

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CIRCUIT TYPES SN52811, SN72811
DUAL-CHANNEL DIFFERENTIAL COMPARATORS WITH STROBES

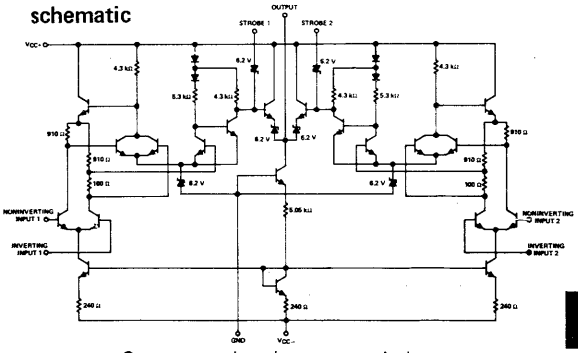
- Fast Response Times
- Improved Voltage Amplification and Offset Characteristics
- Output Compatible with Most TTL and DTL Circuits

description

The SN52811 and SN72811 are improved versions of the SN52711 and SN72711 high-speed dual-channel voltage comparators. Voltage amplification is higher (typically 17,500) due to an extra stage, increasing the comparator accuracy. The output pulse width may be "stretched" by varying the capacitive loading.

Each channel has differential inputs, a strobe input, and an output in common with the other channel. When either strobe is taken low, it inhibits the associated channel. If both strobes are simultaneously low, the output will be low regardless of the conditions applied to the differential inputs.

schematic



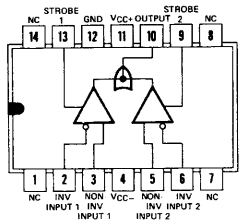
Component values shown are nominal.

These dual-channel voltage comparators are particularly attractive for applications requiring an amplitude-discriminating sense amplifier with an adjustable threshold voltage.

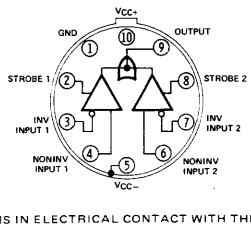
The SN52811 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72811 is characterized for operation from 0°C to 70°C.

terminal assignments

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

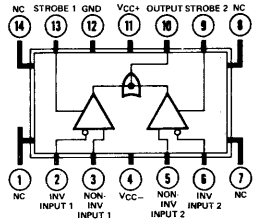


L
PLUG-IN PACKAGE (TOP VIEW)



PIN 5 IS IN ELECTRICAL CONTACT WITH THE CASE

Z FLAT PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	14 V
Supply voltage V_{CC-} (see Note 1)	−7 V
Differential input voltage (see Note 2)	±5 V
Input voltage (either input, see Note 1)	±7 V
Strobe Voltage (see Note 1)	6 V
Peak output current ($t_w \leq 1$ s)	50 mA
Continuous total power dissipation at (or below) 70°C free-air temperature (see Note 3)	300 mW
Operating free-air temperature range: SN52811 Circuits	−55°C to 125°C
SN72811 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J, L, or Z package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. For operation of the SN52811 above 70°C free-air temperature, refer to Dissipating Derating Curve, Figure 10.

electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN52811			SN72811			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$, V_{IC} = 0, See Note 4	25°C		1	3.5		1	5	mV
			Full range			4.5			6	
		$R_S \leq 200\ \Omega$, See Note 4	25°C		1	5		1	7.5	
			Full range			6			10	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S \leq 200\ \Omega$, V_{IC} = 0, See Note 4	Full range		5			5		μV/°C
I_{IO}	Input offset current	See Note 4	25°C		0.5	3		0.5	5	μA
			Full range			5			10	
I_{IB}	Input bias current	See Note 4	25°C		7	20		7	30	μA
			Full range			30			50	
I_{SL}	Low-level strobe current	$V_{(strobe)}$ = −100 mV	25°C		−1.2	−2.5		−1.2	−2.5	mA
V_{ICR}	Common-mode input voltage range	V_{CC-} = −7 V	25°C	±5			±5			V
V_{ID}	Differential input voltage range		25°C	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	V_O = 0 to 2.5 V, No load	25°C	12,500	17,500		10,000	17,500		
			Full range	8,000			5,000			
V_{OH}	High-level output voltage	V_{ID} = 10 mV, I_{OH} = 0	25°C		4	5		4	5	V
		V_{ID} = 10 mV, I_{OH} = −5 mA	25°C	2.5	3.6		2.5	3.6		
V_{OL}	Low-level output voltage	V_{ID} = −10 mV, I_{OL} = 0	25°C	−1	−0.4	0‡	−1	−0.4	0‡	V
		V_{ID} = 10 mV, $V_{(strobe)}$ = 0.3 V, I_{OL} = 0	25°C	−1		0‡	−1		0‡	
I_{OL}	Low-level output current	V_{ID} = −10 mV, V_O = 0	25°C	0.5	0.8		0.5	0.8		mA
r_o	Output resistance	V_O = 1.4 V	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$	25°C	70	90		65	90		dB
I_{CC+}	Supply current from V_{CC+}	V_{ID} = −5 to 5 V (−10 mV for typ),	25°C		6.5			6.5		mA
I_{CC-}	Supply current from V_{CC-}		25°C		−2.7			−2.7		mA
P_D	Total power dissipation	No load, See Note 5	25°C		94	150		94	200	mW

†Unless otherwise noted, all characteristics are measured with the strobe of the channel under test open, the strobe of the other channel is grounded. Full range for SN52811 is −55°C to 125°C and for the SN72811 is 0°C to 70°C.

‡The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

NOTES: 4. These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52811, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1 V at T_A = 125°C; for SN72811, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1.2 V at 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

5. The strobes are alternately grounded.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	SN52811			SN72811			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Response time	R_L = ∞, C_L = 5 pF, See Note 6		33	80		33		ns
Strobe release time	R_L = ∞, C_L = 5 pF, See Note 7		5	25		5		ns

NOTES: 6. The response time specified is for a 100-mV input step with 5-mV overdrive.

7. For testing purposes, the input bias conditions are selected to produce an output voltage of 1.4 V. A 5-mV overdrive is then added to the input bias voltage to produce an output voltage which rises above 1.4 V. The time interval is measured from the 50% point of the strobe voltage curve to the point where the overdriven output voltage crosses the 1.4 V level.

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DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to the specified level. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO}) The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left| \frac{(V_{IO} \text{ @ } T_{A(1)}) - (V_{IO} \text{ @ } T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at the specified level.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at the specified level.

Low-Level Strobe Current (I_{SL}) The current flowing out of the strobe at a low-level voltage.

3

Common-Mode Input Voltage Range (V_{ICR}) The range of common-mode voltage which if exceeded will cause the amplifier to cease functioning properly.

Differential Input Voltage Range (V_{ID}) The range of voltage between the two input terminals which if exceeded will cause the comparator to cease functioning properly.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the change in output voltage to the change in differential input voltage producing it.

High-Level Output Voltage (V_{OH}) The voltage at the output with the specified input conditions applied which should establish a high level at the output.

Low-Level Output Voltage (V_{OL}) The voltage at the output with the specified input conditions applied which should establish a low level at the output.

Low-Level Output Current (I_{OL}) The current flowing into the output at a specified low-level output voltage.

Output Resistance (r_o) The resistance between the output terminal and ground.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Response Time The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial condition sufficient to saturate the output to an input level just barely in excess of that required to bring the output back to the logic threshold voltage. This excess is referred to as the voltage overdrive.

Strobe Release Time The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the low logic level to the high logic level. Appropriate input conditions are assumed.

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TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

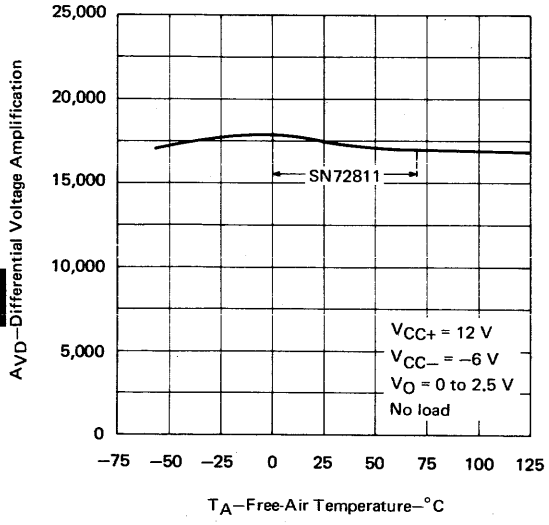

FIGURE 1

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

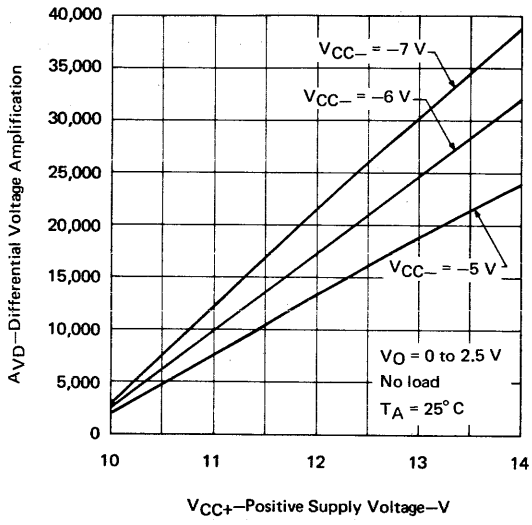

FIGURE 2

SN52811
VOLTAGE TRANSFER CHARACTERISTICS

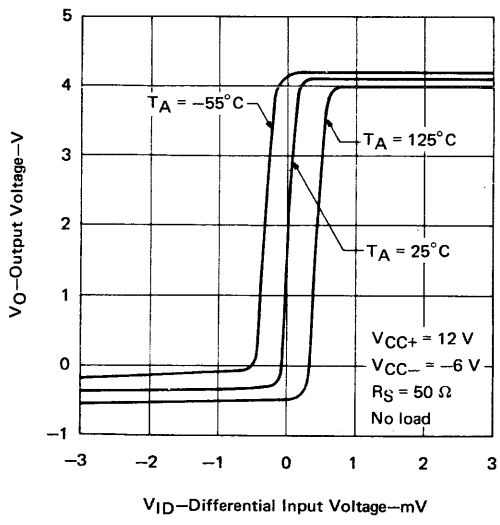

FIGURE 3

SN72811
VOLTAGE TRANSFER CHARACTERISTICS

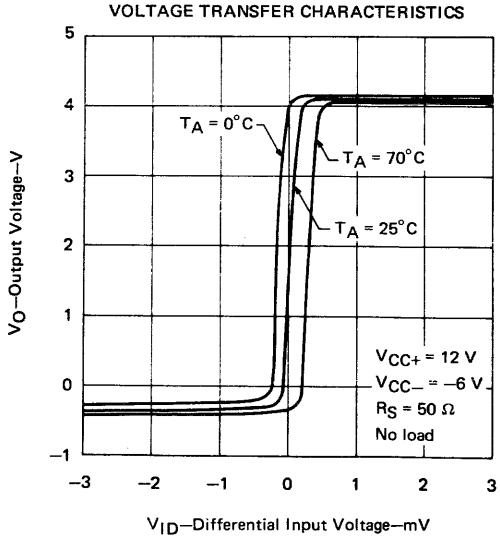

FIGURE 4

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

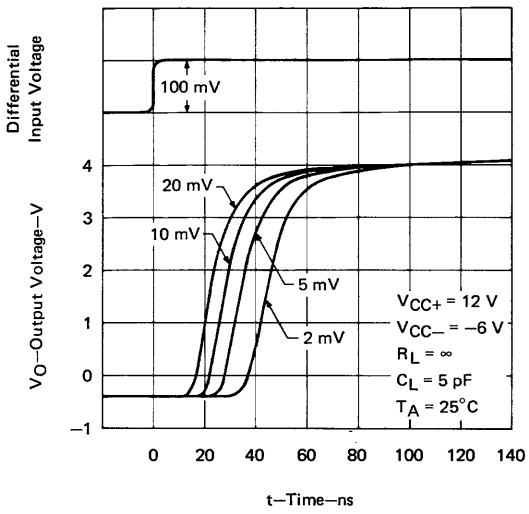


FIGURE 5

STROBE RELEASE TIME
FOR VARIOUS INPUT OVERDRIVES

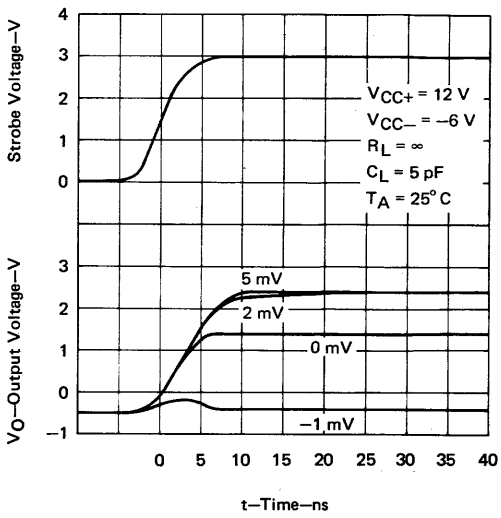


FIGURE 6

COMMON-MODE PULSE RESPONSE

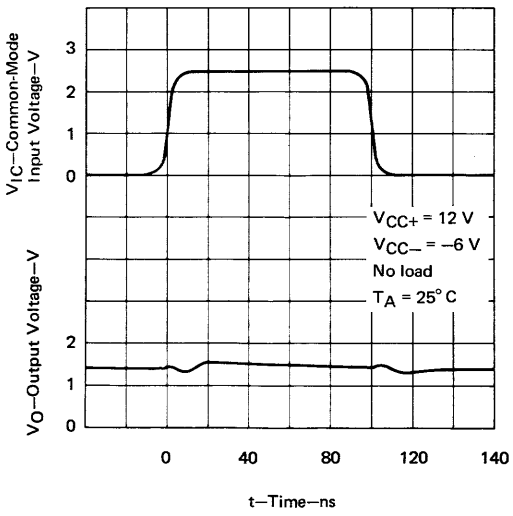
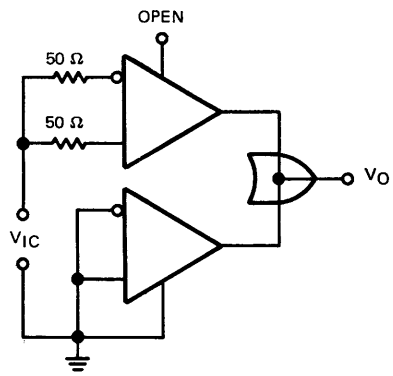


FIGURE 7



TEST CIRCUIT
FOR FIGURE 7

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

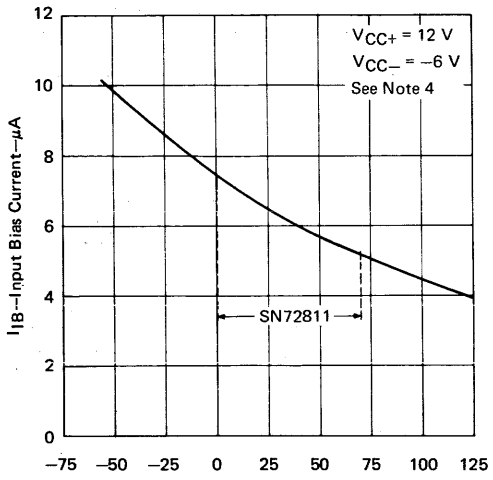


FIGURE 8

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

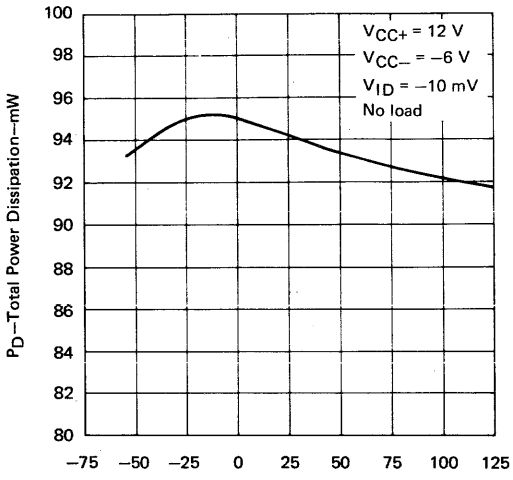


FIGURE 9

NOTE 4. These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52811, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1 V at T_A = 125°C; for SN72811, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1.2 V at 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

THERMAL INFORMATION

SN52811
DISSIPATION DERATING CURVE

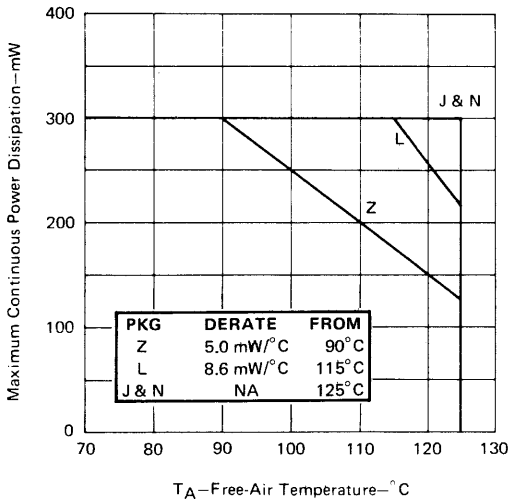
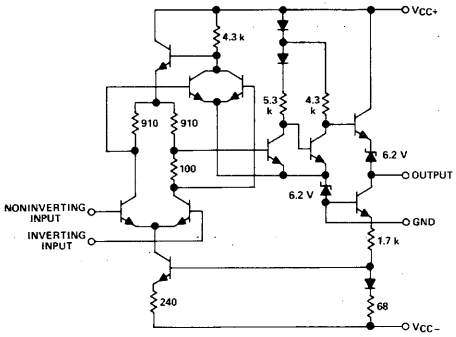


FIGURE 10

CIRCUIT TYPES SN52820, SN72820
DUAL DIFFERENTIAL COMPARATORS

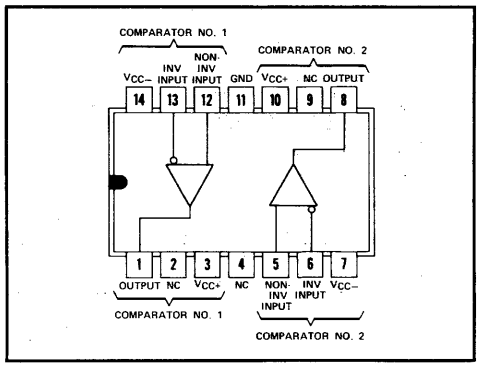
- Fast Response Times
- High Differential Voltage Amplification
- Low Offset Characteristics
- Outputs Compatible with Most TTL and DTL Circuits

schematic (each comparator)



Resistor values are in ohms.
Component values shown are nominal.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection

description

The SN52820 and SN72820 are improved versions of the SN72720 dual high-speed voltage comparator. Each comparator has differential inputs and a low-impedance output. When compared with the SN72720, these circuits feature higher amplification (typically 33,000) due to an extra amplification stage and increased accuracy because of lower offset characteristics. They are particularly useful in applications requiring an amplitude discriminator, memory sense amplifier, or a high-speed limit detector. The SN52820 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72820 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	14 V
Supply voltage V_{CC-} (see Note 1)	−7 V
Differential input voltage (see Note 2)	±5 V
Input voltage (either input, see Note 1)	±7 V
Peak output current ($t_w \leq 1$ s)	10 mA
Continuous total power dissipation: each comparator	300 mW
total package, (see Note 3)	600 mW
Operating free-air temperature range: SN52820 Circuits	−55°C to 125°C
SN72820 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. For SN52820, this rating applies at (or below) 95°C free-air temperature. For operation above this temperature, derate linearly at the rate of 10.9 mW/°C. For SN72820, this rating applies at (or below) 70°C free-air temperature without derating.

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electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN52820			SN72820			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$, See Note 4	25°C		0.6	2		1.6	3.5	mV
			Full range			3			4.5	
α_{VIO}	Average temperature coefficient of input offset voltage	R_S = 50 Ω, See Note 4	MIN to 25°C		3	10		3	20	μV/°C
			25°C to MAX		3	10		3	20	
I_{IO}	Input offset current	See Note 4	25°C		0.75	3		1.8	5	μA
			MIN		1.8	7			7.5	
			MAX		0.25	3			7.5	
α_{IIO}	Average temperature coefficient of input offset current	See Note 4	MIN to 25°C		15	75		24	100	nA/°C
			25°C to MAX		5	25		15	50	
I_{IB}	Input bias current	See Note 4	25°C		7	15		7	20	μA
			MIN		12	25		9	30	
V_{ICR}	Common-mode input voltage range	V_{CC-} = −7 V	Full range	±5			±5			V
V_{ID}	Differential input voltage range		Full range	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	No load, V_O = 0 to 2.5 V	25°C	12,500	33,000		10,000	33,000		
			Full range	10,000			8,000			
V_{OH}	High-level output voltage	V_{ID} = 5 mV, I_{OH} = 0	Full range		4§	5		4§	5	V
		V_{ID} = 5 mV, I_{OH} = −5 mA	Full range	2.5	3.6§		2.5	3.6§		
V_{OL}	Low-level output voltage	V_{ID} = −5 mV, I_{OL} = 0	Full range	−1	−0.5§	0‡	−1	−0.5§	0‡	V
I_{OL}	Low-level output current	V_{ID} = −5 mV, V_O = 0	25°C	2	2.4		1.6	2.4		mA
			MIN	1	2.3		0.5	2.4		
			MAX	0.5	2.3		0.5	2.4		
r_o	Output resistance	V_O = 1.4 V	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$	Full range	80	100§		70	100§		dB
I_{CC+}	Supply current from V_{CC+} (each comparator)	V_{ID} = −5 mV, No load	Full range		5.5§	9		5.5§	9	mA
I_{CC-}	Supply current from V_{CC-} (each comparator)		Full range		−3.5§	−7		−3.5§	−7	mA
P_D	Total power dissipation (each comparator)		Full range		90§	150		90§	150	mW

†Full range (MIN to MAX) for SN52820 is −55°C to 125°C and for the SN72820 is 0°C to 70°C.

‡The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

§These typical values are at T_A = 25°C.

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52820, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1V at T_A = 125°C; for SN72820, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at 25°C, and V_O = 1.2 V at T_A = 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Response time	R_L = ∞, C_L = 5 pF, See Note 5		30	80	ns

NOTE 5: The response time specified is for a 100-mV input step with 5-mV overdrive.

For definition of terms and typical characteristic curves, see the SN52810/SN72810 data sheet on page 3-79.

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TYPE	SN52733, SN72733	SN5510, SN7510	SN5511, SN7511	SN5512, SN7512	SN5514, SN7514	UNIT
Differential Voltage Amplification, Typ	10 to 400 (Adjustable)	93	3000	300	300	
Bandwidth (−3 dB), Typ	200 (Gain of 10)	40	3	80	80	MHz
Bandwidth (Unity-Gain), Typ	400	300	100	400	400	MHz
Input Offset Current, Typ	0.4	3	0.6	1	1	μA
Input Offset Voltage, Typ	1.5 (Gain of 400)	5	1	1 (can be nulled)	1	mV
Output Voltage Swing, Typ	4.7	4	5	3.4	3.4	V p-p
Packages	L, N	F, L	F, L, N	L	L	

CIRCUIT TYPES SN52733, SN72733
DIFFERENTIAL VIDEO AMPLIFIERS

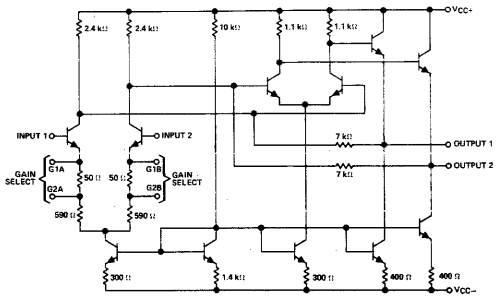
- 200 MHz Bandwidth
- 250 kΩ Input Resistance
- Selectable Nominal Amplification of 10, 100, or 400
- No Frequency Compensation Required

description

The SN52733 and SN72733 are monolithic two-stage video amplifiers with differential inputs and differential outputs.

Internal series-shunt feedback provides wide bandwidth, low phase distortion, and excellent gain stability. Emitter-follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios.

schematic



Component values shown are nominal

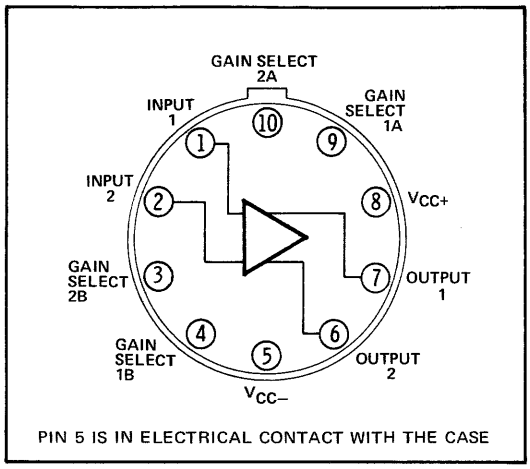
Fixed differential amplification of 10, 100, or 400 may be selected without external components, or amplification may be adjusted from 10 to 400 by the use of a single external resistor connected between G1A and G1B. No external frequency-compensating components are required for any gain option.

The device is particularly useful in magnetic-tape or disc-file systems using phase or NRZ encoding and in high-speed thin-film or plated-wire memories. Other applications include general purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

The SN52733 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72733 is characterized for operation from 0°C to 70°C.

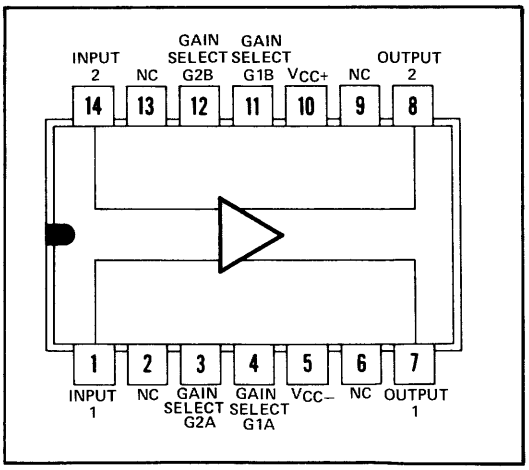
terminal assignments

L PLUG-IN-PACKAGE
(TOP VIEW)



PIN 5 IS IN ELECTRICAL CONTACT WITH THE CASE

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52733	SN72733	UNIT
Supply voltage V_{CC+} (See Note 1)		8	8	V
Supply voltage V_{CC-} (See Note 1)		−8	−8	V
Differential input voltage		±5	±5	V
Common-mode input voltage		±6	±6	V
Output current		10	10	mA
Continuous total power dissipation (See Note 2 on the following page)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16" from case for 60 seconds	L package	300	300	°C
Lead temperature 1/16" from case for 10 seconds	N package	260	260	°C

NOTE 1: All voltage values, except differential input voltages, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.

electrical characteristics, T_A = 25°C, V_{CC+} = 6 V, V_{CC-} = −6 V

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN† SELECT	SN52733 MIN	SN52733 TYP	SN52733 MAX	SN72733 MIN	SN72733 TYP	SN72733 MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	V_{OD} = 1 V	1	300	400	500	250	400	600	
				2	90	100	110	80	100	120	
				3	9	10	11	8	10	12	
BW	Bandwidth	2	R_S = 50 Ω	1		50			50		MHz
				2		90			90		
				3		200			200		
I_{IO}	Input offset current			Any		0.4	3		0.4	5	μA
I_{IB}	Input bias current			Any		9	20		9	30	μA
V_I	Input voltage range	1		Any	±1			±1			V
V_{OC}	Common-mode output voltage	1		Any	2.4	2.9	3.4	2.4	2.9	3.4	V
V_{OO}	Output offset voltage	1		1		0.6	1.5		0.6	1.5	V
				2 & 3		0.35	1		0.35	1.5	
V_{OPP}	Maximum peak-to-peak output voltage swing	1		Any	3	4.7		3	4.7		V
r_i	Input resistance	3	$V_{OD} \leq$ 1 V	1		4			4		kΩ
				2	20	24		10	24		
				3		250			250		
r_o	Output resistance					20			20		Ω
C_i	Input capacitance	3	$V_{OD} \leq$ 1 V	2		2			2		pF
CMRR	Common-mode rejection ratio	4	V_{IC} = ±1 V, f ≤ 100 kHz	2	60	86		60	86		dB
			V_{IC} = ±1 V, f = 5 MHz	2		70			70		
$\Delta V_{CC}/\Delta V_{IO}$	Supply voltage rejection ratio	1	ΔV_{CC+} = ± 0.5 V, ΔV_{CC-} = ± 0.5 V	2	50	70		50	70		dB
V_n	Broadband equivalent input noise voltage	5	BW = 1 kHz to 10 MHz	Any		12			12		μV
t_{pd}	Propagation delay time	2	R_S = 50 Ω, Output voltage step = 1 V	1		7.5			7.5		ns
				2		6.0	10		6.0	10	
				3		3.6			3.6		
t_r	Rise time	2	R_S = 50 Ω, Output voltage step = 1 V	1		10.5			10.5		ns
				2		4.5	10		4.5	12	
				3		2.5			2.5		
$I_{sink(max)}$	Maximum output sink current			Any	2.5	3.6		2.5	3.6		mA
I_{CC}	Supply current		No load, no signal	Any		16	24		16	24	mA

† The gain selection is made as follows:
Gain 1 . . . Gain Select pin G1A is connected to pin G1B, and pins G2A and G2B are open.
Gain 2 . . . Gain Select pin G1A and pin G1B are open, pin G2A is connected to pin G2B.
Gain 3 . . . All four gain-select pins are open.

DEFINITION OF TERMS

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the change in voltage between the output terminals to the change in voltage between the input terminals producing it.

Bandwidth (BW) The range of frequencies within which the differential gain of the amplifier is not more than 3 dB below its low-frequency value.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the inputs grounded.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the inputs grounded.

Input Voltage Range (V_I) The range of voltage which if exceeded at either input terminal will cause the amplifier to cease functioning properly.

Common-Mode Output Voltage (V_{OC}) The average of the d-c voltages at the two output terminals.

Output Offset Voltage (V_{OO}) The difference between the d-c voltages at the two output terminals when the input terminals are grounded.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage swing that can be obtained without clipping. This includes the unbalance caused by output offset voltage.

Input Resistance (r_i) The resistance between the input terminals with either input grounded.

Output Resistance (r_o) The resistance between either output terminal and ground.

Input Capacitance (C_i) The capacitance between the input terminals with either input grounded.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in output offset voltage referred to the input.

Supply Voltage Rejection Ratio ($\Delta V_{CC}/\Delta V_{IO}$) The ratio of the change in power supply voltages to the change in output offset voltage referred to the input. For these devices, both supply voltages are varied symmetrically.

Propagation Delay Time (t_{pd}) The interval between the application of an input voltage step and its arrival at either output, measured at 50% of the final value.

Rise Time (t_r) The time required for an output voltage step to change from 10% to 90% of its final value.

Maximum Output Sink Current ($I_{sink(max)}$) The maximum available current into either output terminal when that output is at its most negative potential.

Supply Current (I_{CC}) The average of the magnitudes of the two supply currents.

NOTE 2: For SN52733 in the L package, this rating applies at (or below) 90°C free-air temperature with derating above that temperature at the rate of 8.3 mW/°C. For SN52733 in the N package, this rating applies at (or below) 105°C free-air temperature with derating above that temperature at the rate of 11.1 mW/°C. For SN72733 in either package, this rating applies at (or below) 70°C free-air temperature without derating.

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PARAMETER MEASUREMENT INFORMATION

test circuits

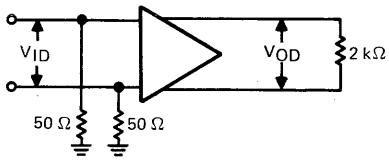


FIGURE 1

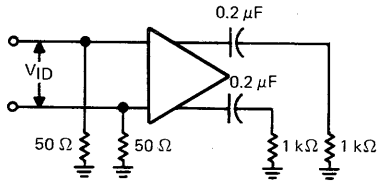


FIGURE 2

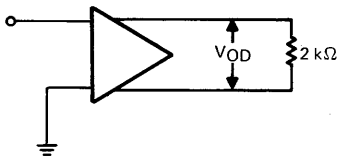


FIGURE 3

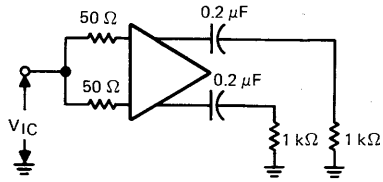


FIGURE 4

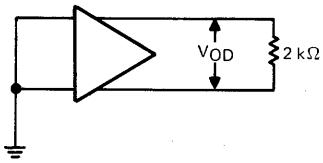
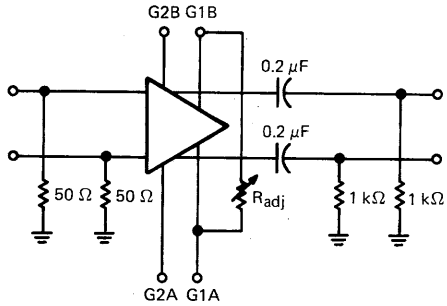


FIGURE 5



VOLTAGE AMPLIFICATION ADJUSTMENT

FIGURE 6

TYPICAL CHARACTERISTICS

PHASE SHIFT
vs
FREQUENCY

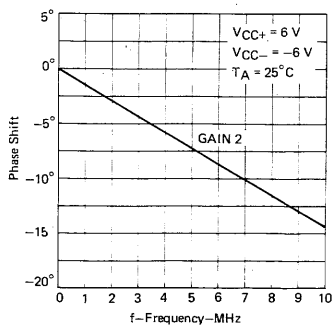


FIGURE 7

PHASE SHIFT
vs
FREQUENCY

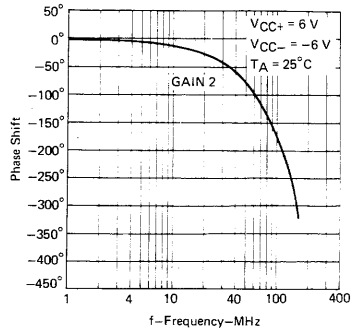


FIGURE 8

TYPICAL CHARACTERISTICS

VOLTAGE AMPLIFICATION
(SINGLE-ENDED OR DIFFERENTIAL)
vs
TEMPERATURE

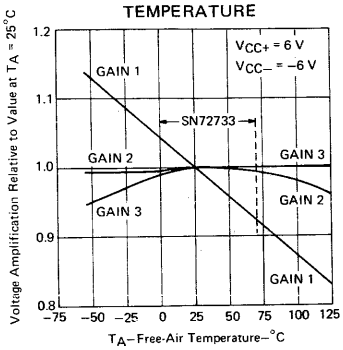


FIGURE 9

VOLTAGE AMPLIFICATION
(SINGLE-ENDED OR DIFFERENTIAL)
vs
SUPPLY VOLTAGE

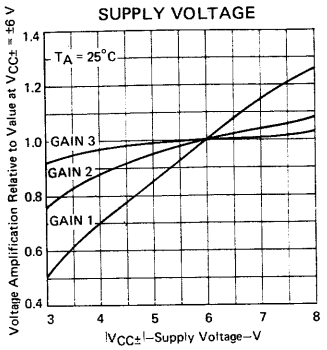


FIGURE 10

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
RESISTANCE BETWEEN G1A AND G1B

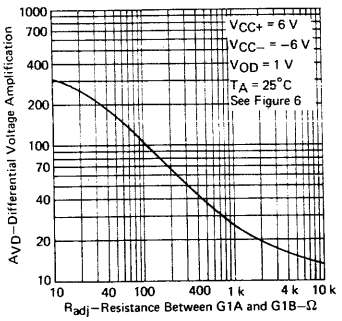


FIGURE 11

SINGLE-ENDED VOLTAGE AMPLIFICATION
vs
FREQUENCY

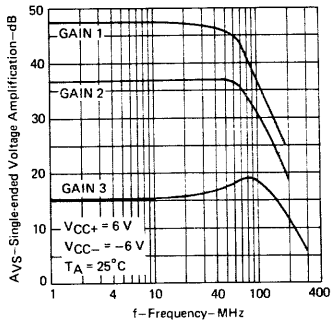


FIGURE 12

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

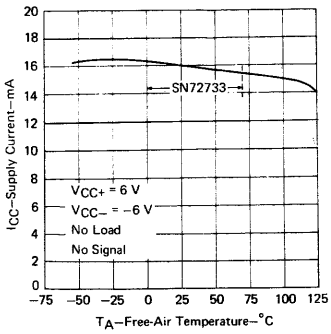


FIGURE 13

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

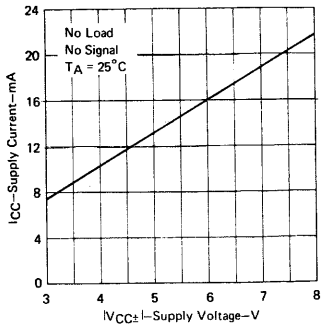


FIGURE 14

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TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

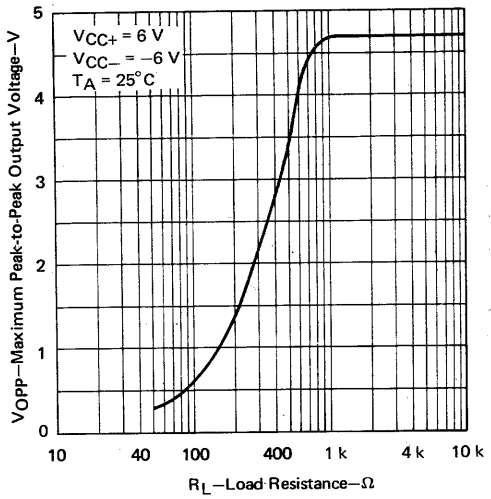

FIGURE 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

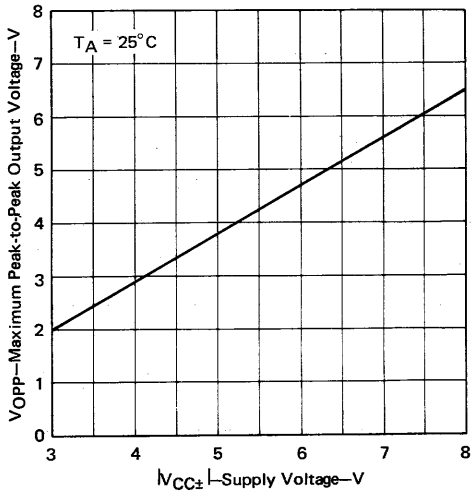

FIGURE 16

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

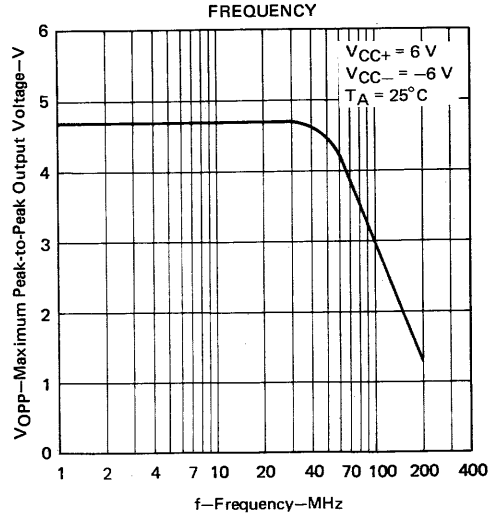

FIGURE 17

INPUT RESISTANCE
vs
FREE-AIR TEMPERATURE

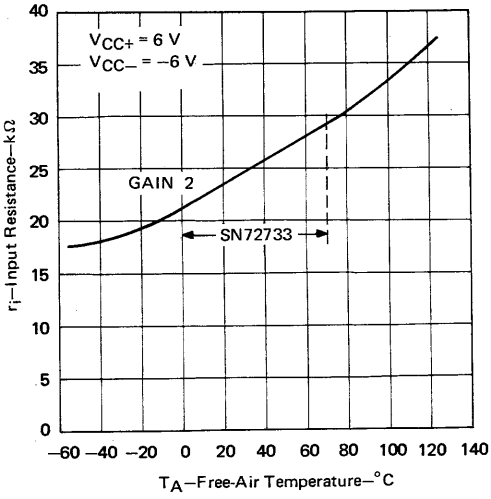

FIGURE 18

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TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

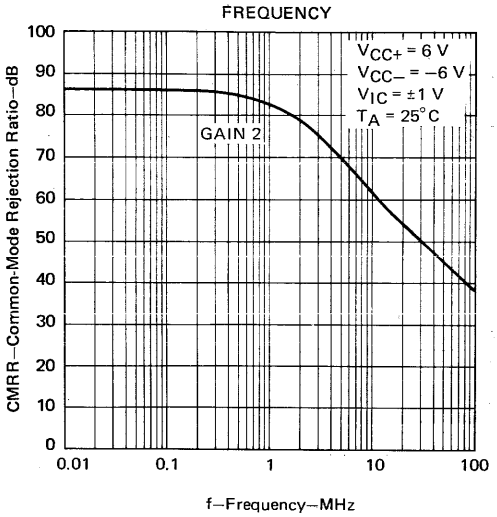


FIGURE 19

DIFFERENTIAL INPUT OVERLOAD RECOVERY TIME
vs
DIFFERENTIAL INPUT VOLTAGE

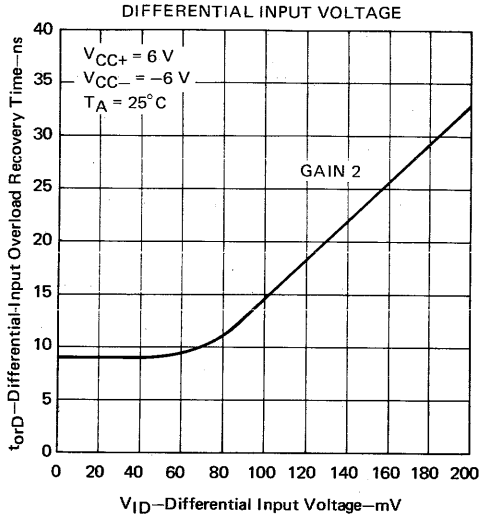


FIGURE 20

PULSE RESPONSE
AS A FUNCTION OF
SUPPLY VOLTAGE

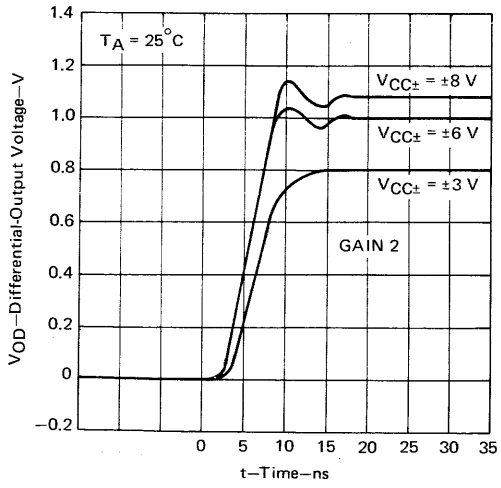


FIGURE 21

PULSE RESPONSE
AS A FUNCTION OF GAIN

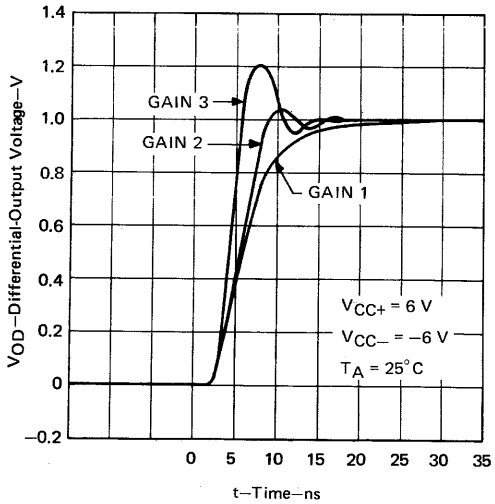


FIGURE 22

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPE SN5510
DIFFERENTIAL VIDEO AMPLIFIER

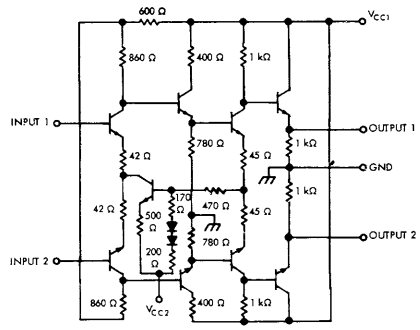
WIDE-BAND VIDEO AMPLIFIER
FEATURING
Flat Frequency Response with Low Phase-Shift from DC to 40 MHz

description

This wide-band video amplifier features a flat frequency response and low phase-shift from dc to 40 MHz. Differential inputs and outputs are provided which permit it to be used as a high-frequency differential amplifier.

Elements of the SN5510 video-amplifier bar include transistors with transition frequency as high as 1.2 GHz under low-current and low-V_{CE} conditions. Circuit frequency response from dc to greater than 100 MHz is possible.

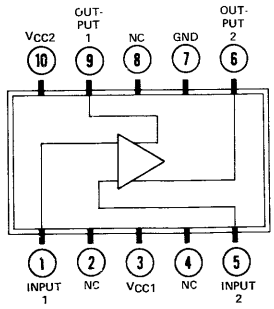
schematic



Component values shown are nominal.

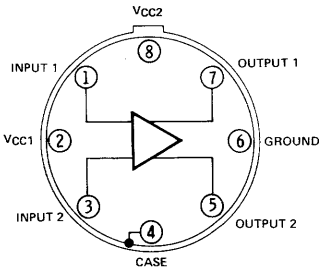
terminal assignments

F
FLAT PACKAGE (TOP VIEW)



THE CIRCUIT IS ELECTRICALLY INSULATED FROM THE CASE

L
PLUG-IN PACKAGE (TOP VIEW)



THE CIRCUIT IS ELECTRICALLY INSULATED FROM THE CASE

NC—No internal connection

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPE SN5510
DIFFERENTIAL VIDEO AMPLIFIER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltages (See Note 1): V_{CC1} . . . . . +8 V
V_{CC2} . . . . . −8 V
Differential input voltage . . . . . 5 V
Positive input voltage (See Note 1) . . . . . V_{CC1}
Negative input voltage (See Note 1) . . . . . V_{CC2}
Operating free-air temperature ranges: SN5510F . . . . . −55°C to 70°C
SN5510L . . . . . −55°C to 100°C
Operating case temperature ranges: SN5510F . . . . . −55°C to 100°C
SN5510L . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These voltage values are with respect to network ground.

3

electrical characteristics, $T_A = 25°C$, $V_{CC1} = +6$ V, $V_{CC2} = -6$ V

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DO}	Differential-output offset voltage	1			0.5	1.3	V
$V_{CMO(av)}$	Average common-mode output offset voltage	1		2.6	3.1	3.5	V
I_{in}	Input current	1			40	80	μA
I_{DI}	Differential-input offset current	1			3	20	μA
D_S	Single-ended output distortion	2	Load resistance = 5 kΩ, input distortion < 0.2%, V_{out} = 1 V rms, f = 10 kHz		1.5	5	%
$V_{N(in)}$	Equivalent average input noise voltage	3	Single-ended, R_S = 0, f = 10 Hz to 500 kHz		5		μV
V_{CMIM}	Maximum common-mode input voltage				±1		V
A_{vs}	Small-signal voltage gain	2	Single-ended, load resistance = 5 kΩ, f = 100 kHz	75	93	110	
A_{vcm}	Common-mode-input voltage gain	4	Single-ended, load resistance = 5 kΩ, V_{in} = 0.3 V rms, f = 100 kHz		−45	−30	dB
CMRR	Common-mode rejection ratio	4	Load resistance = 5 kΩ, f = 100 kHz		85		dB
BW	Bandwidth (−3 dB)	2			40		MHz
r_{in}	Input resistance	5	f = 100 kHz		6		kΩ
C_{in}	Input capacitance	5	f = 100 kHz		7		pF
z_{out}	Output impedance	5	f = 100 kHz		35		Ω
P_T	Total power dissipation	1	No input signal, no external load		165	220	mW
t_r	Rise time	6	Single-ended, V_{in} = 5 mV		9	12	ns
t_f	Fall time	6	Single-ended, V_{in} = 5 mV		9	12	ns

TEXAS INSTRUMENTS
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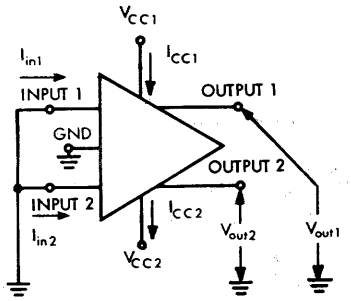
letter symbol and parameter definitions

V_{DO}	The d-c differential voltage that exists between the output terminals when the input terminals are at ground.
$V_{CMO(av)}$	The average of the d-c output voltages with respect to ground when the input terminals are grounded.
I_{DI}	The difference in the currents into the two input terminals.
V_{CMIM}	The maximum common-mode voltage that can be impressed on the input terminals while maintaining differential operation.
CMRR	The ratio of the differential-mode voltage gain to the common-mode voltage gain.
BW	The range of frequencies within which the open-loop voltage gain is within 3 dB of the mid-frequency value.

3

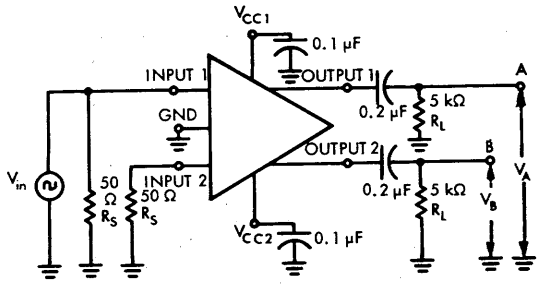
PARAMETER MEASUREMENT INFORMATION

test circuits



1. $V_{DO} = |V_{out1} - V_{out2}|$
2. $V_{CMO(av)} = \dfrac{V_{out1} + V_{out2}}{2}$
3. $I_{DI} = |I_{in1} - I_{in2}|$
4. $P_T = |V_{CC1} \bullet I_{CC1}| + |V_{CC2} \bullet I_{CC2}|$

FIGURE 1



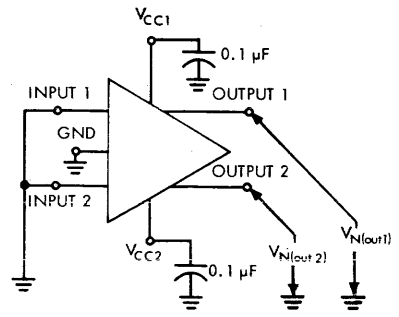
1. Single-ended output distortion is measured at A or B with V_A or V_B = 1 V rms, input distortion < 0.2%, and f = 10 kHz.
2. $A_{VS} = \left|\dfrac{V_A \text{ or } V_B}{V_{in}}\right|$

where: V_{in} = 1 mV rms and f = 100 kHz.

FIGURE 2

PARAMETER MEASUREMENT INFORMATION

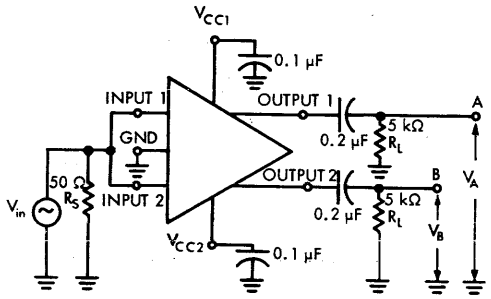
test circuits (continued)



1. $V_{\overline{N(in)}} = \frac{V_{\overline{N(out1)}} \text{ or } V_{\overline{N(out2)}}}{A_{VS}}$

where: $V_{\overline{N(out)}}$ = true rms broad-band noise voltage from 10 Hz to 500 kHz.

FIGURE 3



1. $A_{vcm} = 20 \text{ Log} \left| \frac{V_A \text{ or } V_B}{V_{in}} \right|$

where: V_{in} = 0.3 V rms and f = 100 kHz.

2. CMRR = 20 Log $A_{VS} - A_{vcm}$

FIGURE 4

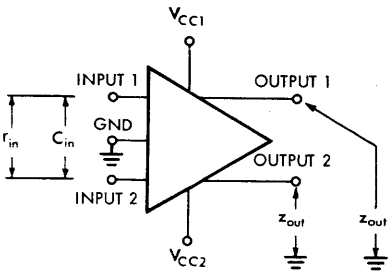
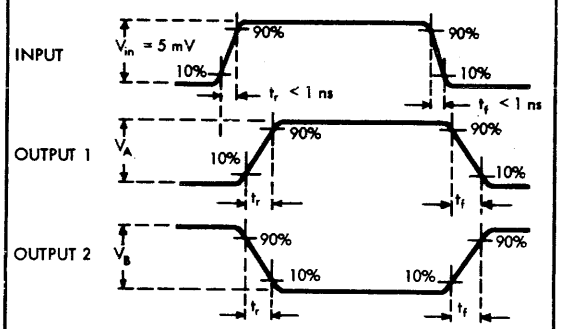


FIGURE 5



1. Test circuit is identical to that shown in Figure 2.

FIGURE 6 — t_r and t_f VOLTAGE WAVEFORMS

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TYPICAL CHARACTERISTICS†

AVERAGE COMMON-MODE OUTPUT OFFSET VOLTAGE
vs
FREE-AIR TEMPERATURE

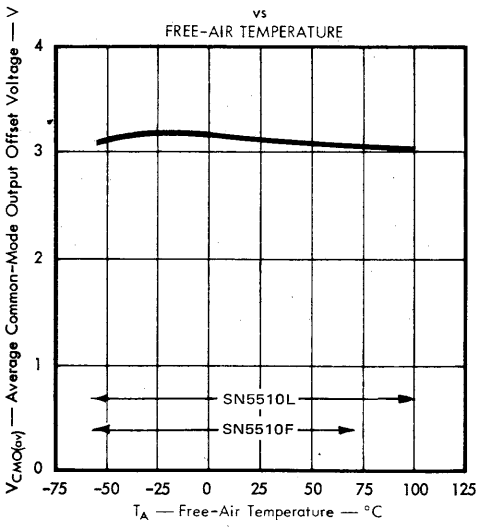

FIGURE 7

INPUT CURRENT
vs
FREE-AIR TEMPERATURE

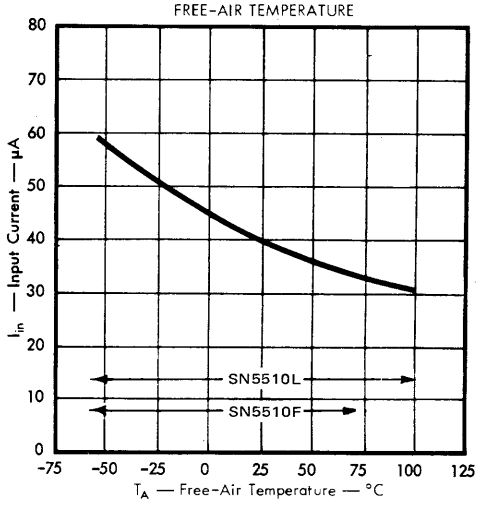

FIGURE 8

PEAK-TO-PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

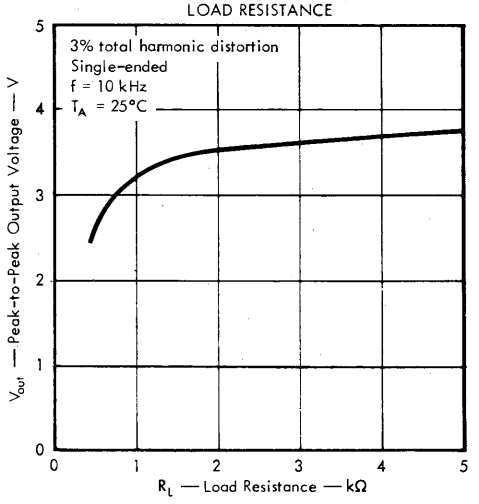

FIGURE 9

PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

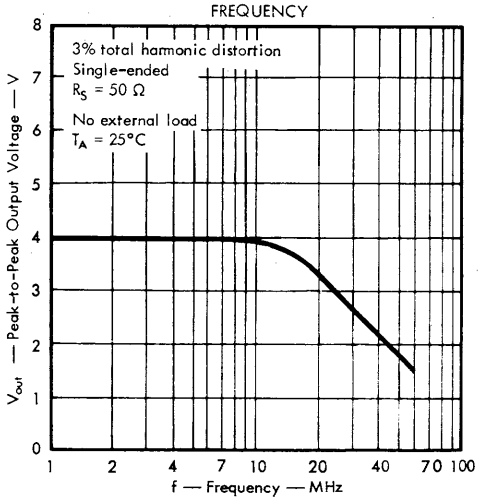

FIGURE 10

†Unless otherwise noted $V_{CC1} = +6$ V, $V_{CC2} = -6$ V.

TYPICAL CHARACTERISTICS†

SMALL-SIGNAL VOLTAGE GAIN
vs
FREE-AIR TEMPERATURE

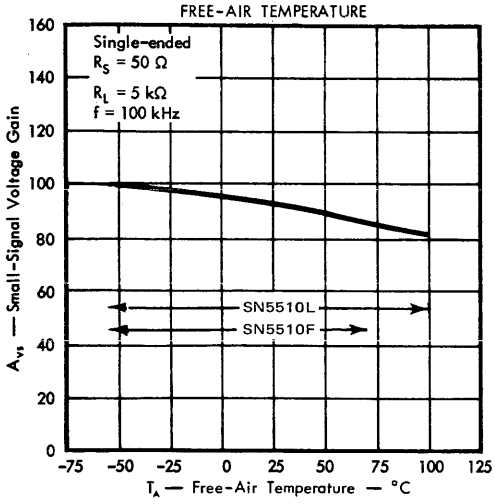

FIGURE 11

SMALL-SIGNAL VOLTAGE GAIN VARIATION
vs
SUPPLY VOLTAGE

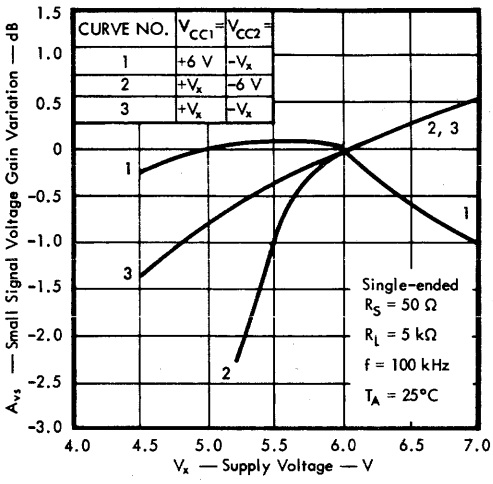

FIGURE 12

SMALL-SIGNAL VOLTAGE GAIN
vs
FREQUENCY

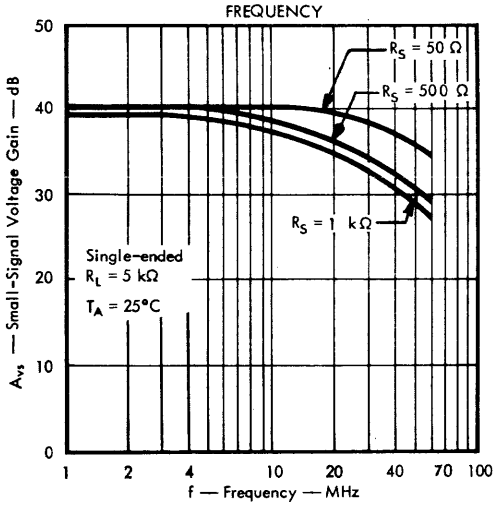

FIGURE 13

SMALL-SIGNAL VOLTAGE GAIN
vs
FREQUENCY

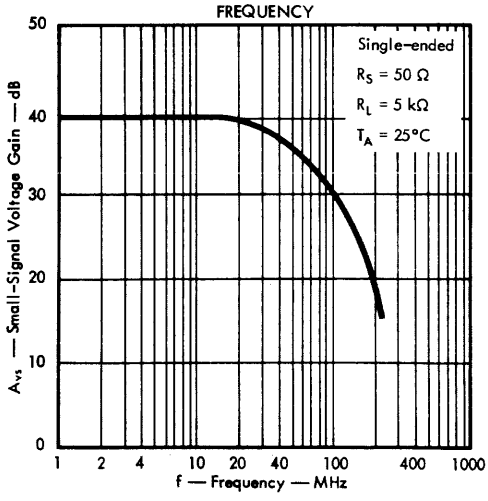

FIGURE 14

†Unless otherwise noted V_{CC1} = +6 V, V_{CC2} = −6 V.

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TYPICAL CHARACTERISTICS†

PHASE SHIFT
vs
FREQUENCY

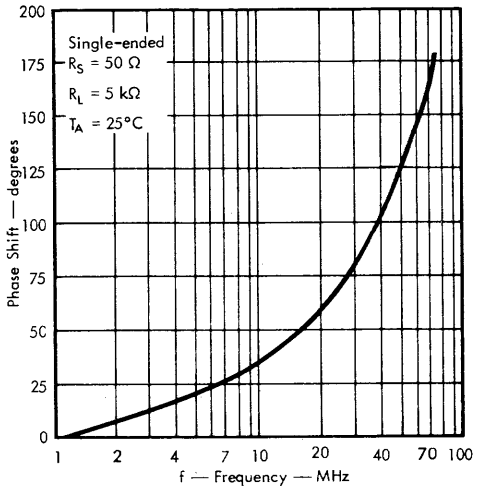


FIGURE 15

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

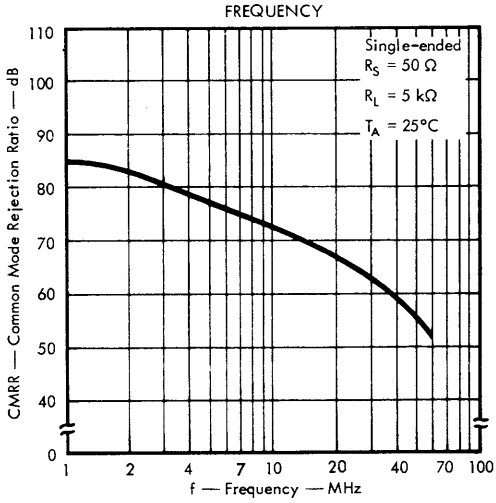
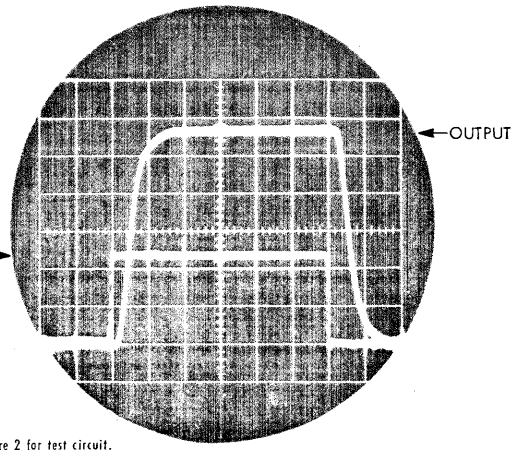


FIGURE 16

†V_{CC1} = +6 V and V_{CC2} = −6 V.



SCALES
Horizontal: 10 ns/division
Vertical: Output = 200 mV/division
Input = 5 mV/division

NOTE: See Figure 2 for test circuit.

FIGURE 17 — OSCILLOSCOPE PRESENTATION OF PULSE RESPONSE

CIRCUIT TYPE SN7510
DIFFERENTIAL VIDEO AMPLIFIER

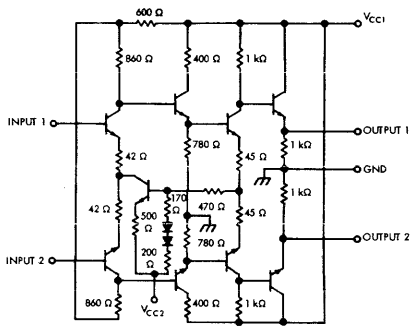
WIDE-BAND VIDEO AMPLIFIER
FEATURING
Flat Frequency Response with Low Phase-Shift from DC to 40 MHz

description

This wide-band video amplifier features a flat frequency response and low phase-shift from dc to 40 MHz. Differential inputs and outputs are provided which permit it to be used as a high-frequency differential amplifier.

Elements of the SN7510 video-amplifier bar include transistors with transition frequency as high as 1.2 GHz under low-current and low-V_{CE} conditions. Circuit frequency response from dc to greater than 100 MHz is possible.

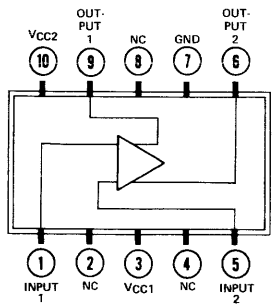
schematic



Component values shown are nominal.

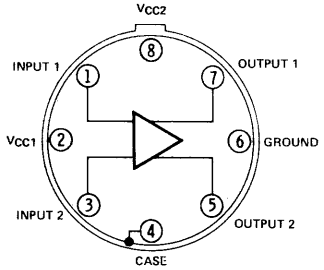
terminal assignments

F
FLAT PACKAGE (TOP VIEW)



THE CIRCUIT IS ELECTRICALLY INSULATED FROM THE CASE

L
PLUG-IN PACKAGE (TOP VIEW)



THE CIRCUIT IS ELECTRICALLY INSULATED FROM THE CASE

NC—No internal connection

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltages (See Note 1): V_{CC1} . . . . . ±8 V
V_{CC2} . . . . . −8 V
Differential input voltage . . . . . 5 V
Positive input voltage (See Note 1) . . . . . V_{CC1}
Negative input voltage (See Note 1) . . . . . V_{CC2}
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These voltage values are with respect to network ground.

3

electrical characteristics, $T_A = 25°C$, $V_{CC1} = +6$ V, $V_{CC2} = -6$ V

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DO}	Differential-output offset voltage	1			0.5	2	V
$V_{CMO(av)}$	Average common-mode output offset voltage	1		2	3	4	V
I_{in}	Input current	1			50	100	μA
I_{DI}	Differential-input offset current	1			5	30	μA
V_{OM}	Maximum peak-to-peak output voltage	2	Single-ended, load resistance = 5 kΩ, f = 100 kHz, V_{in} = 20 mV rms		4.5		V
D_S	Single-ended output distortion	2	Load resistance = 5 kΩ, input distortion < 0.2%, V_{out} = 1 V rms, f = 10 kHz		2		%
$V_{N(in)}$	Equivalent average input noise voltage	3	Single-ended, R_S = 0, f = 10 Hz to 500 kHz		5		μV
V_{CMIM}	Maximum common-mode input voltage				±1		V
A_{vs}	Small-signal voltage gain	2	Single-ended, load resistance = 5 kΩ, f = 100 kHz	60	90	120	
A_{vcm}	Common-mode-input voltage gain	4	Single-ended, load resistance = 5 kΩ, V_{in} = 0.3 V rms, f = 100 kHz		−40	−20	dB
CMRR	Common-mode rejection ratio	4	Load resistance = 5 kΩ, f = 100 kHz		85		dB
BW	Bandwidth (−3 dB)	2			40		MHz
r_{in}	Input resistance	5	f = 100 kHz		6		kΩ
C_{in}	Input capacitance	5	f = 100 kHz		7		pF
z_{out}	Output impedance	5	f = 100 kHz		35		Ω
P_T	Total power dissipation	1	No input signal, no external load		165	220	mW
t_r	Rise time	6	Single-ended, V_{in} = 5 mV		10	15	ns
t_f	Fall time	6	Single-ended, V_{in} = 5 mV		10	15	ns

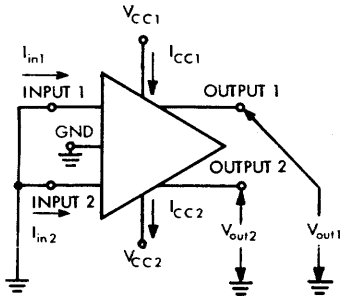
letter symbol and parameter definitions

V_{DO}	The d-c differential voltage that exists between the output terminals when the input terminals are at ground.
$V_{CMO(av)}$	The average of the d-c output voltages with respect to ground when the input terminals are grounded.
I_{DI}	The difference in the currents into the two input terminals.
V_{OM}	The maximum peak-to-peak output voltage swing that can be obtained without clipping.
V_{CMIM}	The maximum common-mode voltage that can be impressed on the input terminals while maintaining differential operation.
CMRR	The ratio of the differential-mode voltage gain to the common-mode voltage gain.
BW	The range of frequencies within which the open-loop voltage gain is within 3 dB of the mid-frequency value.

3

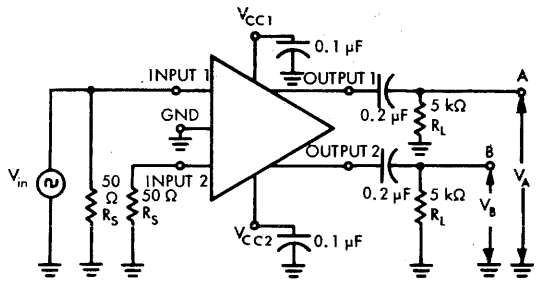
PARAMETER MEASUREMENT INFORMATION

test circuits



1. $V_{DO} = |V_{out1} - V_{out2}|$
2. $V_{CMO(av)} = \dfrac{V_{out1} + V_{out2}}{2}$
3. $I_{DI} = |I_{in1} - I_{in2}|$
4. $P_T = |V_{CC1} \bullet I_{CC1}| + |V_{CC2} \bullet I_{CC2}|$

FIGURE 1



1. Single-ended output distortion is measured at A or B with V_A or V_B = 1 V rms, input distortion < 0.2%, and f = 10 kHz.
2. $A_{VS} = \left|\dfrac{V_A \text{ or } V_B}{V_{in}}\right|$
   where: V_{in} = 1 mV rms and f = 100 kHz.
3. $V_{OM} = V_A$ or V_B

FIGURE 2

TEXAS INSTRUMENTS
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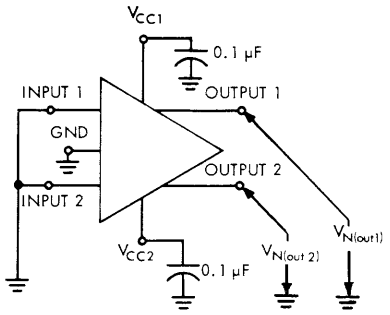
PARAMETER MEASUREMENT INFORMATION

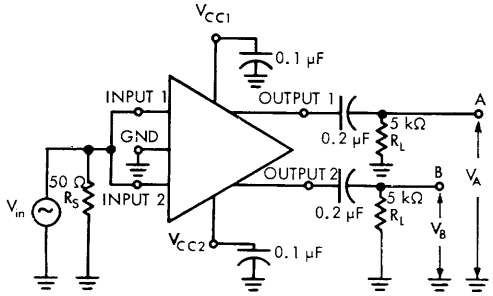
test circuits (continued)



1. $V_{\overline{N(in)}} = \frac{V_{\overline{N(out1)}} \text{ or } V_{\overline{N(out2)}}}{A_{VS}}$

where: $V_{\overline{N(out)}}$ = true rms broad-band noise voltage from 10 Hz to 500 kHz.

FIGURE 3



1. $A_{vcm} = 20 \text{ Log} \left| \frac{V_A \text{ or } V_B}{V_{in}} \right|$

where: V_{in} = 0.3 V rms and f = 100 kHz.

2. CMRR = 20 Log $A_{VS} - A_{vcm}$

FIGURE 4

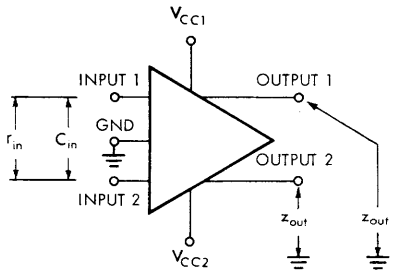
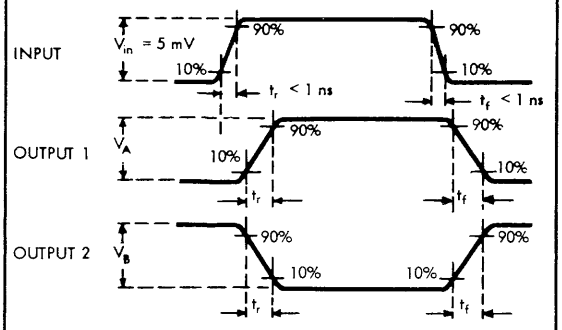


FIGURE 5



1. Test circuit is identical to that shown in Figure 2.

FIGURE 6 — t_r and t_f VOLTAGE WAVEFORMS

3

TYPICAL CHARACTERISTICS†

AVERAGE COMMON-MODE OUTPUT OFFSET VOLTAGE
vs
FREE-AIR TEMPERATURE

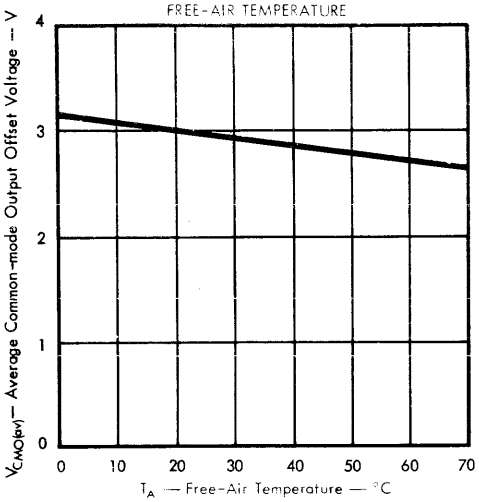


FIGURE 7

INPUT CURRENT
vs
FREE-AIR TEMPERATURE

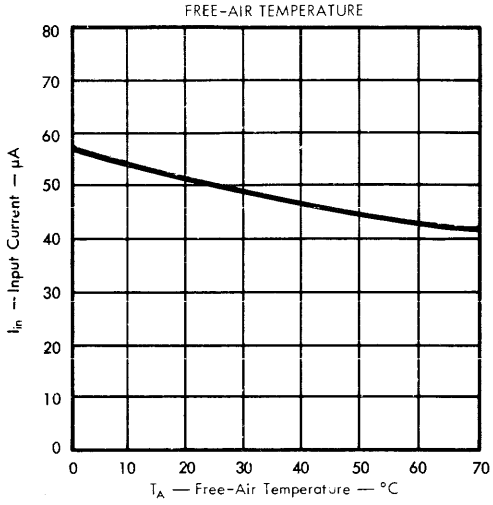


FIGURE 8

PEAK-TO-PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

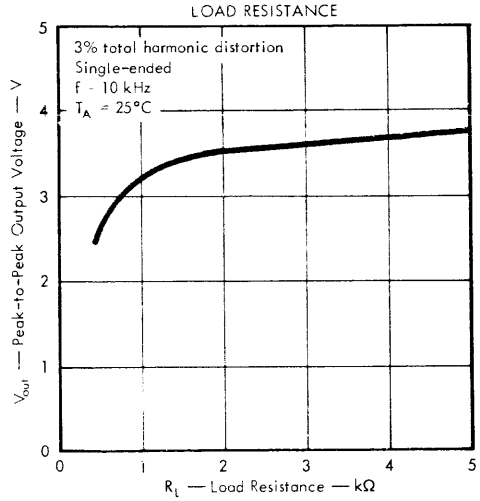


FIGURE 9

PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

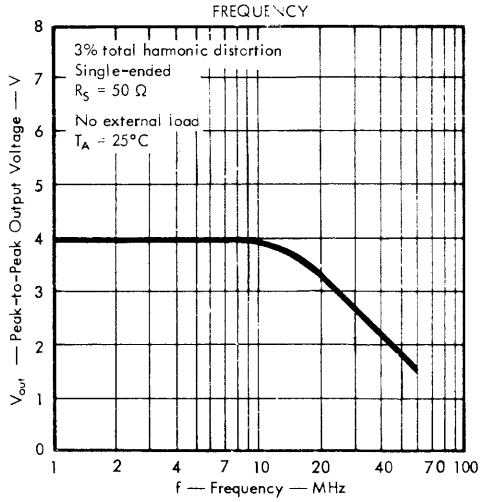


FIGURE 10

† Unless otherwise noted V_{CC1} = +6 V, V_{CC2} = −6 V.

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TYPICAL CHARACTERISTICS†

SMALL-SIGNAL VOLTAGE GAIN
vs
FREE-AIR TEMPERATURE

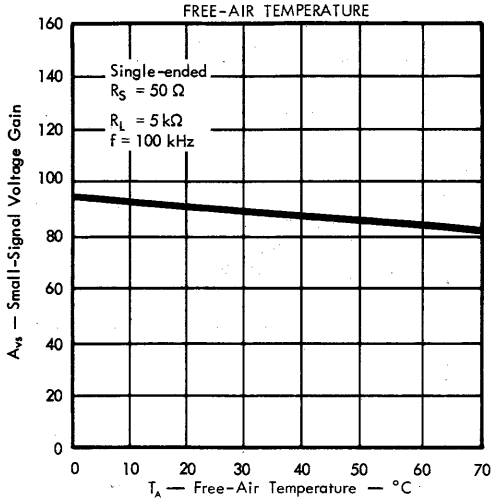

FIGURE 11

SMALL-SIGNAL VOLTAGE GAIN VARIATION
vs
SUPPLY VOLTAGE

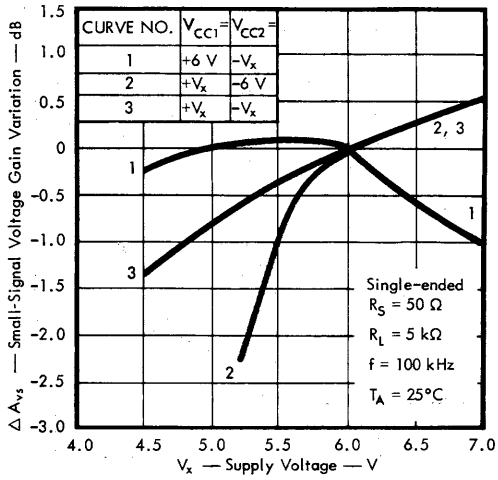

FIGURE 12

SMALL-SIGNAL VOLTAGE GAIN
vs
FREQUENCY

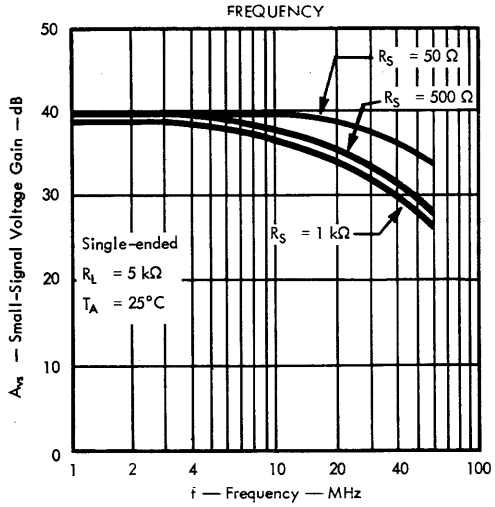

FIGURE 13

SMALL-SIGNAL VOLTAGE GAIN
vs
FREQUENCY

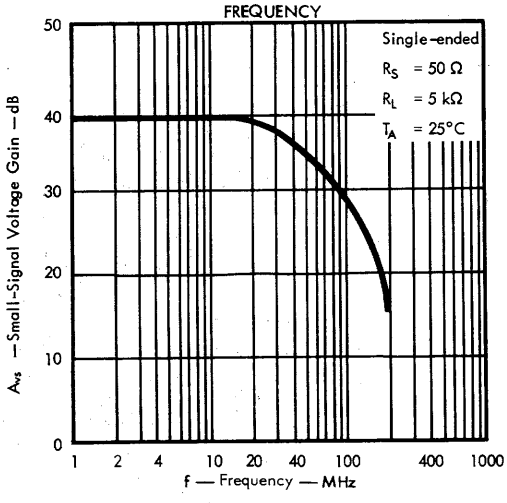

FIGURE 14

† Unless otherwise noted $V_{CC1} = +6$ V, $V_{CC2} = -6$ V.

TYPICAL CHARACTERISTICS†

PHASE SHIFT
vs
FREQUENCY

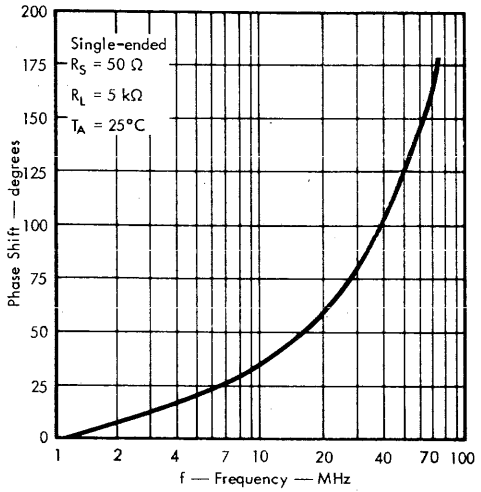

FIGURE 15

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

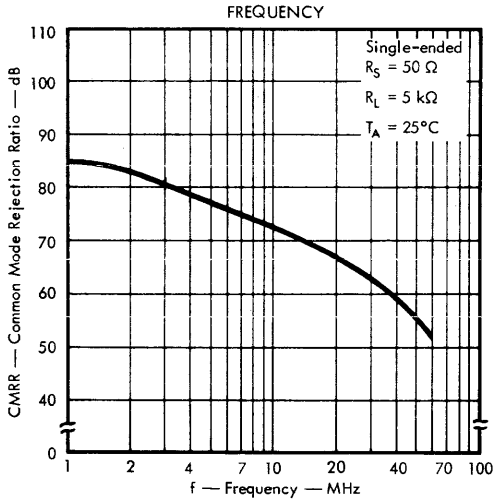

FIGURE 16

† V_{CC1} = +6 V and V_{CC2} = −6 V.

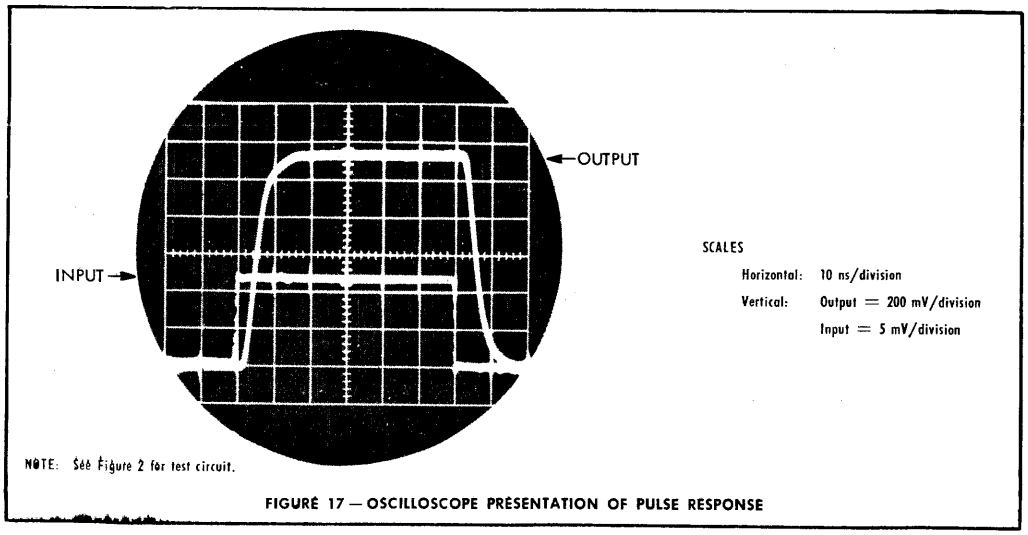

FIGURE 17 — OSCILLOSCOPE PRESENTATION OF PULSE RESPONSE

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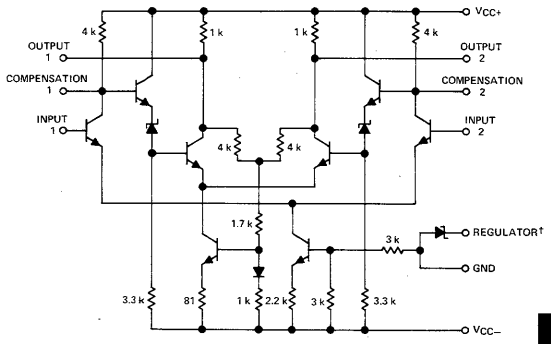
CIRCUIT TYPES SN5511, SN7511
DIFFERENTIAL VIDEO AMPLIFIERS

- Low Common-Mode Offset Voltage
- High Common-Mode Rejection Ratio
- High Gain-Bandwidth Product

schematic



Resistor values are nominal in ohms.

† Regulator terminal is used only with single supply. See description.

description

The SN5511 and SN7511 are wide-band amplifiers with differential inputs and outputs. High gain and low offset voltage permit use in applications requiring feedback. Frequency characteristics are such that a stable closed-loop configuration with 30-dB gain results in a 30-MHz bandwidth.

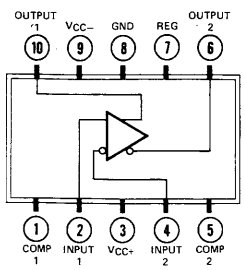
Accessibility to first-stage collectors makes offset balancing and frequency compensation possible with minimal effect on input and frequency characteristics.

The base of the first-stage current-source transistor is made available to permit operation from either a single 12-volt power supply or two 6-volt power supplies. For the latter, leave the regulator terminal open and connect the positive terminal of one supply to V_{CC+}, the negative terminal of the other supply to V_{CC-}, and the remaining terminals of the two supplies to the device ground terminal. For operation from a single 12-volt supply, connect the positive terminal of the supply to both the V_{CC+} and regulator terminals and connect the negative terminal to V_{CC-}. In either case, the device ground terminal is the reference for single-ended input and output voltages.

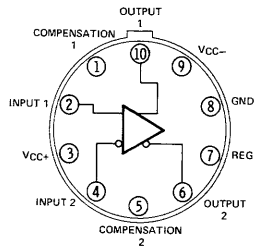
The wide bandwidth and high gain allow this amplifier to be used in a variety of applications where a stable differential video amplifier is required. Low common-mode offset voltage extends possible uses to comparators and direct-coupled amplifiers. The SN5511 is characterized for operation over the full military temperature range of –55°C to 125°C; the SN7511 is characterized for operation from 0°C to 70°C.

terminal assignments

F
FLAT PACKAGE (TOP VIEW)

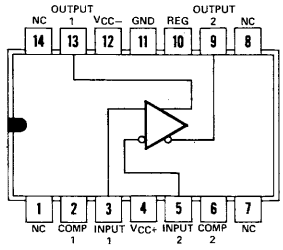


L
PLUG-IN PACKAGE (TOP VIEW)



ALL LEADS ARE ELECTRICALLY INSULATED FROM THE CASE

N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC – No internal connection

3

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1) . . . . . 8 V
Supply voltage V_{CC-} (see Note 1) . . . . . −8 V
Input voltage, either input to ground . . . . . ±6 V
Differential input voltage . . . . . ±6 V
Continuous total power dissipation at (or below) 55°C free-air temperature (see Note 2) . . . . . 500 mW
Operating free-air temperature range: SN5511 Circuits . . . . . −55°C to 125°C
SN7511 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds, F and L packages . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds, N package . . . . . 260°C

NOTES: 1. All voltage values, unless otherwise specified, are with respect to the network ground terminal.
2. For operation above 55°C free-air temperature, refer to Dissipation Derating Curve, Figure 1.

3

electrical characteristics, V_{CC+} = 6 V, V_{CC-} = −6 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS†	SN5511 MIN	SN5511 TYP	SN5511 MAX	SN7511 MIN	SN7511 TYP	SN7511 MAX	UNIT
A_{VD}	Large-signal differential voltage amplification		1	f ≤ 1 kHz, No load		3000					
				f ≤ 1 kHz, R_L = 5 kΩ		1200			600		
A_{VS}	Large-signal single-ended voltage amplification		2	f ≤ 1 kHz, R_L = 5 kΩ	400	600		250	300		
BW	Bandwidth	−3 dB		R_S = 500 Ω, No load		3			3		MHz
		Unity gain				100			100		
V_{IO}	Input offset voltage					1	5		1	5	mV
α_{VIO}	Average temperature coefficient of input offset voltage			T_A = −55°C to 25°C		4					μV/°C
				T_A = 25°C to 125°C		2					
				T_A = 0°C to 25°C					4		
				T_A = 25°C to 70°C					2		
I_{IO}	Input offset current					0.6	7		0.6	10	μA
I_{IB}	Input bias current					10	15		15	20	μA
V_I	Input voltage range		3		+2.5 −2			±1			V
V_{OO}	Output offset voltage			No load		0.35			0.35		V
				R_L = 500 Ω		0.17			0.17		
V_{OPP}	Maximum peak-to-peak output voltage swing		2	f ≤ 1 kHz, R_L = 5 kΩ	2.5	5		1.5	3		V
				f ≤ 1 kHz, R_L = 500 Ω		3			2		
z_{id}	Differential input impedance			f = 1 kHz		5			5		kΩ
z_{os}	Single-ended output impedance			f = 1 kHz		800			800		Ω
CMRR	Common-mode rejection ratio		3	f ≤ 100 kHz, No load, See Note 3	59	95		52	90		dB
P_D	Total power dissipation			No load, No signal		180			180		mW

NOTE 3: For SN5511, V_{IC} = +2.5 V to −2 V; for SN7511, V_{IC} = + 1 V to −1 V.
†Unless otherwise specified, V_{IO} is applied and the regulator terminal is open.

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DEFINITION OF TERMS

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the change in voltage between the output terminals to the change in voltage between the input terminals producing it.

Large-Signal Single-Ended Voltage Amplification (A_{VS}) The ratio of the change in single-ended output voltage to the change in single-ended input voltage.

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c differential output voltage to zero.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO}) The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left|\frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}}\right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the inputs grounded.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the inputs grounded.

Input Voltage Range (V_I) The range of voltage which if exceeded at either input terminal will cause the amplifier to cease functioning properly.

3

Output Offset Voltage (V_{OO}) The difference between the d-c voltages at the two output terminals when the input terminals are grounded.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage swing that can be obtained without clipping. This includes the unbalance caused by output offset voltage.

Differential Input Impedance (z_{id}) The small-signal impedance between the two input terminals.

Single-Ended Output Impedance (z_{os}) The small-signal impedance between one output terminal and ground.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in output offset voltage referred to the input.

Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load; $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

THERMAL INFORMATION

DISSIPATION DERATING CURVE

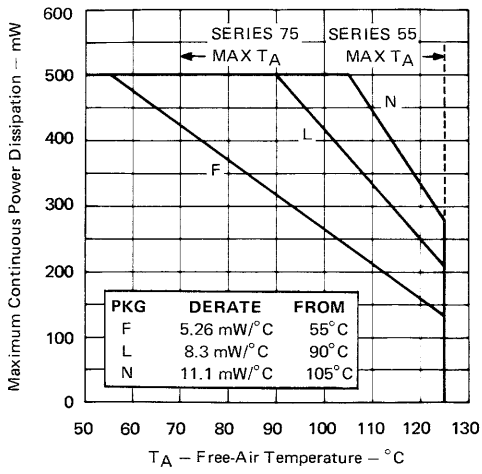

FIGURE 1

PARAMETER MEASUREMENT INFORMATION

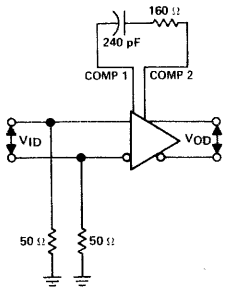

FIGURE 2 – A_{VD}

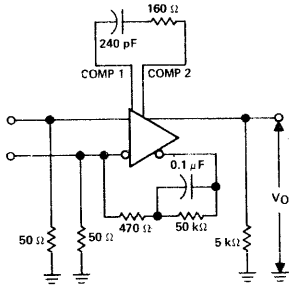

FIGURE 3 – A_{VS}, V_{OPP}

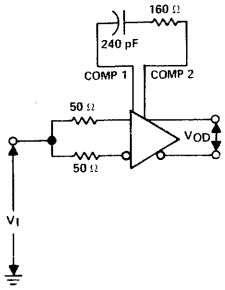

FIGURE 4 – V_I, CMRR

TYPICAL CHARACTERISTICS

3

SN5511
SINGLE-ENDED OPEN-LOOP
VOLTAGE AMPLIFICATION
vs
FREQUENCY

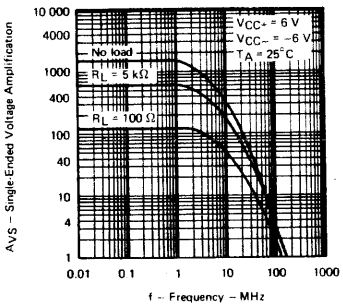

FIGURE 5

SN5511
SINGLE-ENDED OPEN-LOOP
VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

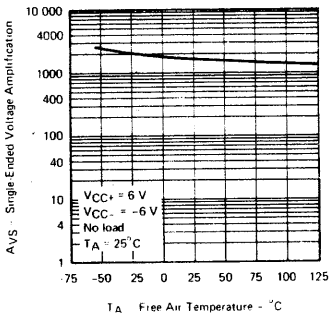

FIGURE 6

SN5511
SINGLE-ENDED OPEN-LOOP
VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGES

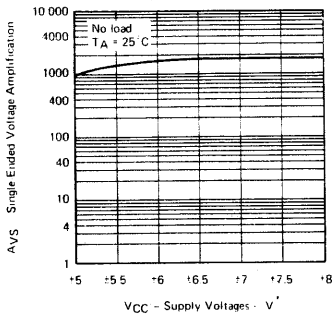

FIGURE 7

SN5511
INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

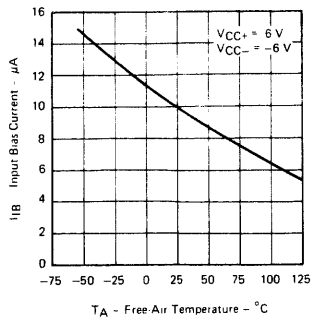

FIGURE 8

SN5511
MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE (OPEN-LOOP)
vs
LOAD RESISTANCE

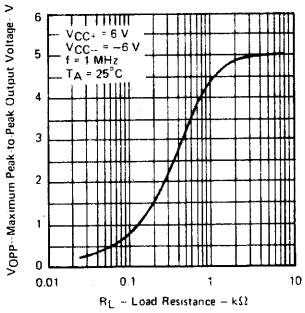

FIGURE 9

SN5511
MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE (OPEN-LOOP)
vs
FREQUENCY

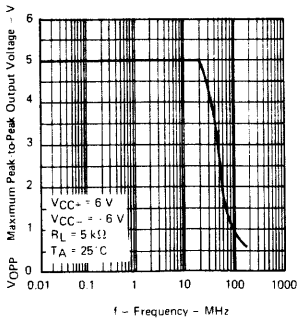

FIGURE 10

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TYPICAL CHARACTERISTICS

SN5511
SINGLE-ENDED CLOSED-LOOP
VOLTAGE AMPLIFICATION
vs
FREQUENCY

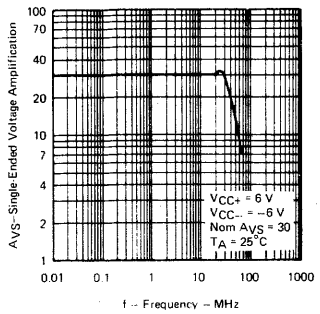
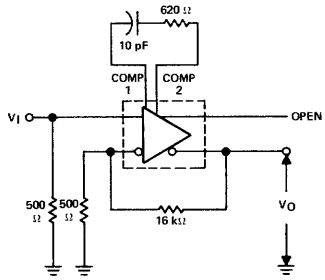


FIGURE 11

NOMINAL AMPLIFICATION OF 30



TEST CIRCUIT
FOR FIGURES 11 AND 12

SN5511
MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE (CLOSED-LOOP)
vs
FREQUENCY

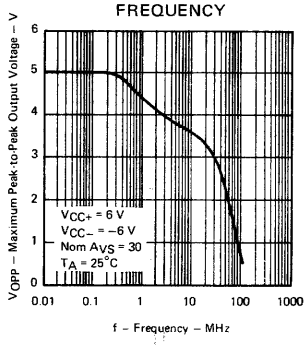


FIGURE 12

3

SN5511
SINGLE-ENDED CLOSED-LOOP
VOLTAGE AMPLIFICATION
vs
FREQUENCY

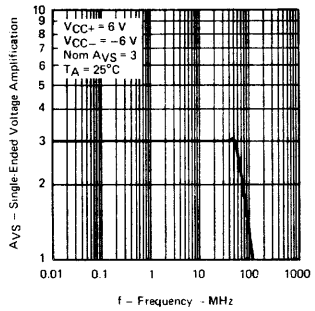
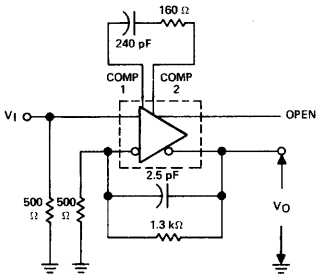


FIGURE 13

NOMINAL AMPLIFICATION OF 3



TEST CIRCUIT
FOR FIGURES 13 AND 14

SN5511
MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE (CLOSED-LOOP)
VS
FREQUENCY

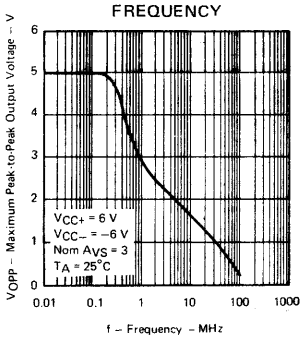


FIGURE 14

SN5511
SINGLE-ENDED CLOSED-LOOP
VOLTAGE AMPLIFICATION
vs
FREQUENCY

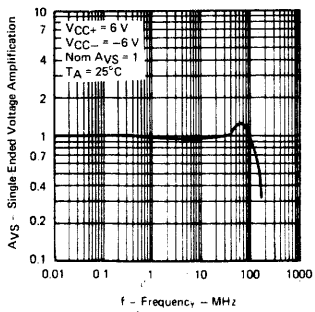
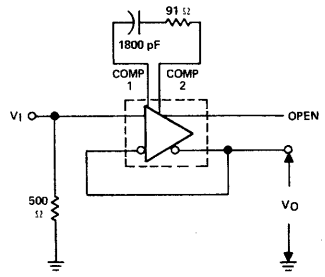


FIGURE 15

NOMINAL AMPLIFICATION OF 1



TEST CIRCUIT
FOR FIGURES 15 AND 16

SN5511
MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE (CLOSED-LOOP)
vs
FREQUENCY

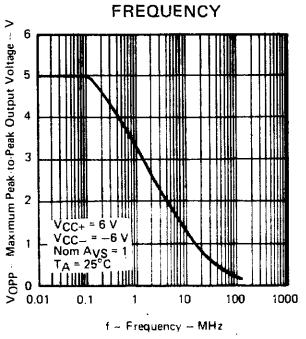


FIGURE 16

TYPICAL CHARACTERISTICS

INPUT IMPEDANCE
vs
FREE-AIR TEMPERATURE

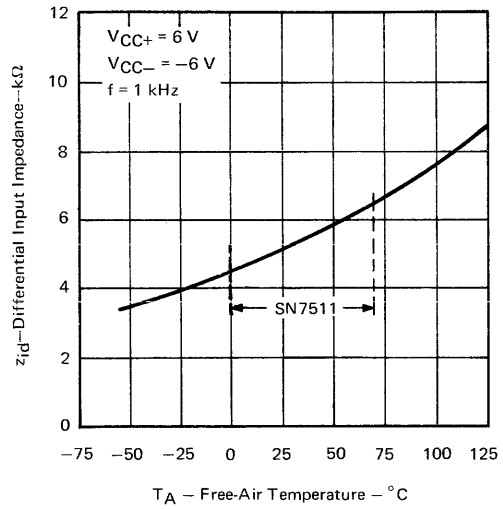


FIGURE 17

SN5511

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

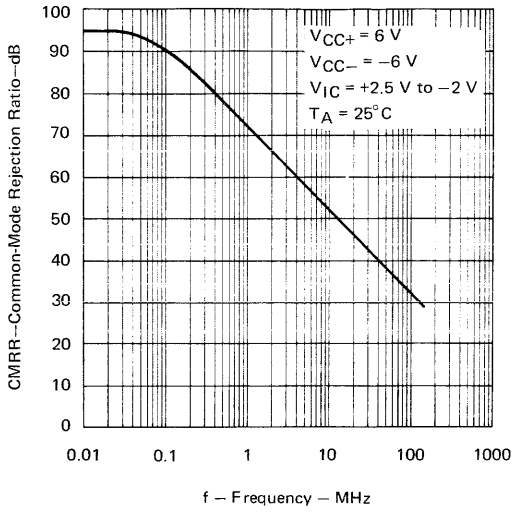


FIGURE 18

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

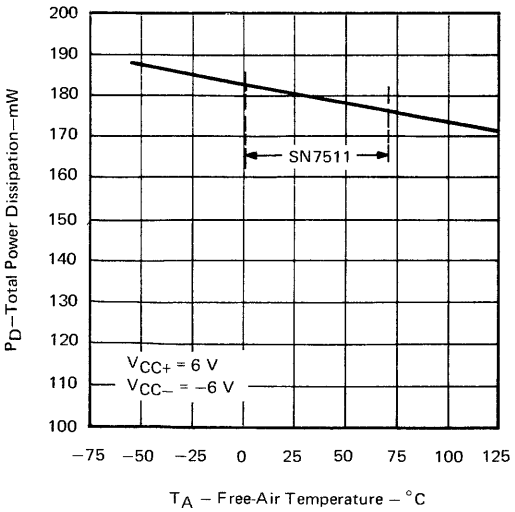


FIGURE 19

SPOT NOISE FIGURE
vs
FREQUENCY

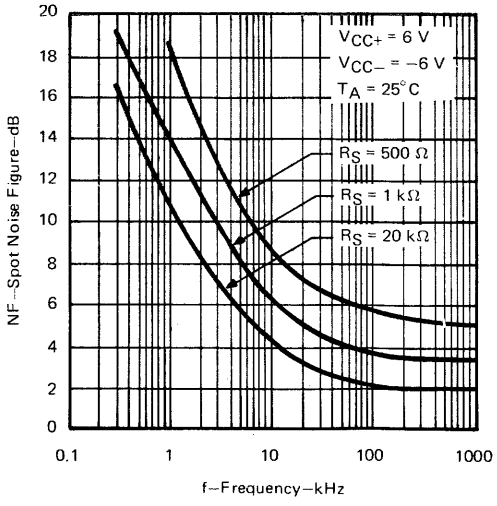


FIGURE 20

TEXAS INSTRUMENTS
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CIRCUIT TYPES SN5512, SN5514, SN7512, SN7514
DIFFERENTIAL VIDEO AMPLIFIERS

- 80-MHz Bandwidth
- No Frequency Compensation Required
- Typical Differential Voltage Amplification of 300
- SN5512 and SN7512 Have Offset-Voltage Null Capability

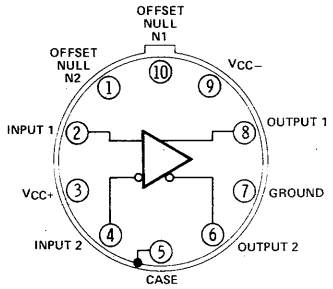
description

Each of these wide-band video amplifiers feature a flat frequency response and low phase distortion from dc to typically 80 MHz. Emitter-follower outputs enable the devices to drive capacitive loads. A low-value potentiometer may be connected between the offset null inputs of the SN5512 and SN7512, as shown in Figure 7, to null out the offset voltage.

These circuits are designed for use as sense amplifiers in high-speed thin-film or plated-wire memories, as magnetic tape-read amplifiers, or as general purpose pulse or video amplifiers.

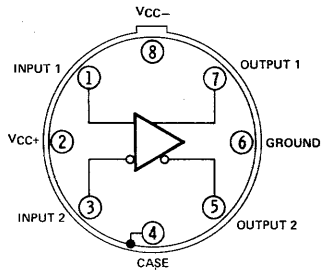
terminal assignments

SN5512, SN7512
L PLUG-IN PACKAGE
(TOP VIEW)



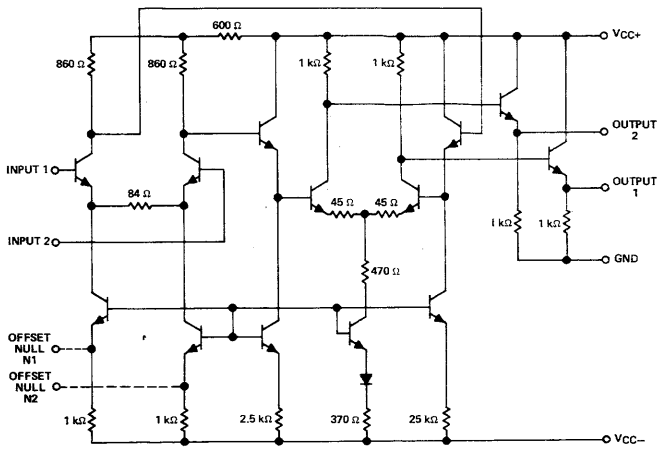
THE CIRCUIT IS ELECTRICALLY INSULATED FROM THE CASE

SN5514, SN7514
L PLUG-IN PACKAGE
(TOP VIEW)



THE CIRCUIT IS ELECTRICALLY INSULATED FROM THE CASE

schematic



NOTES: 1. Component values shown are nominal.
2. Offset null terminals (shown with dashed lines) are provided on the SN5512 and SN7512 only.

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN5512 SN5514	SN7512 SN7514	UNIT
Supply voltage V_{CC+} (See Note 3)	8	8	V
Supply voltage V_{CC-} (See Note 3)	−8	−8	V
Differential input voltage	±5	±5	V
Common-mode input voltage	±6	±6	V
Voltage between either offset null terminal (N1/N2) and V_{CC-} (SN5512 and SN7512)	±0.5	±0.5	V
Output current	10	10	mA
Continuous total power dissipation at (or below) 65°C free-air temperature (See Note 4)	500	500	mW
Operating free-air temperature range	−55 to 125	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Lead temperature 1/16" from case for 60 seconds	300	300	°C

NOTES: 3. All voltage values, except differential input voltages, are with respect to the network ground terminal.
4. For operation above 65°C free-air temperature, refer to Dissipation Derating Curve, Figure 6.

3

electrical characteristics, T_A = 25°C, V_{CC+} = 6 V, V_{CC-} = −6 V

PARAMETER		TEST FIGURE	TEST CONDITIONS	SN5512 SN5514			SN7512 SN7514			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
A_{VD}	Large-signal differential voltage amplification	1	V_{OD} = 1 V	250	300	350	200	300	400	
BW	Bandwidth	2	R_S = 50 Ω		80			80		MHz
I_{IO}	Input offset current				1	3		1	5	μA
I_{IB}	Input bias current				50	80		50	80	μA
V_I	Input voltage range	1		±1			±1			V
V_{OC}	Common-mode output voltage	1		2.4	2.7	3.4	2.4	2.7	3.4	V
V_{OO}	Output offset voltage	1			0.5	1.3		0.5	1.3	V
V_{OPP}	Maximum peak-to-peak output voltage swing	3		3	5		3	5		V
r_i	Input resistance	3	$V_{OD} \leq 1$ V		6			6		kΩ
r_o	Output resistance				35			35		Ω
C_i	Input capacitance	3	$V_{OD} \leq 1$ V		7			7		pF
CMRR	Common-mode rejection ratio	4	V_{IC} = ± 1 V, f ≤ 100 kHz		84			84		dB
$\Delta V_{CC}/\Delta V_{IO}$	Supply voltage rejection ratio	1	ΔV_{CC+} = from 6 V to 5.5 V ΔV_{CC-} = from −6 V to −5.5 V	50	80		50	80		dB
V_n	Broadband equivalent input noise voltage	5	See Note 5		3			3		μV
t_{pd}	Propagation delay time	2	R_S = 50 Ω, Output voltage step = 0 to 1 V		6			6		ns
t_r	Rise time	2	R_S = 50 Ω, Output voltage step = 0 to 1 V		5			5		ns
$I_{sink(max)}$	Maximum output sink current			2.5	3.2		2.5	3.2		mA
I_{CC+}	Supply current from V_{CC+}		No load, No signal		19	25		19	25	mA
I_{CC-}	Supply current from V_{CC-}		No load, No signal		−13	−20		−13	−20	mA

NOTE 5: This parameter is measured in a system with response down 3 dB at 10 Hz and 500 kHz with a 6-dB/octave rolloff.

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DEFINITION OF TERMS

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the change in voltage between the output terminals to the change in voltage between the input terminals producing it.

Bandwidth (BW) The range of frequencies within which the differential gain of the amplifier is not more than 3 dB below its low-frequency value.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the inputs grounded.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the inputs grounded.

Input Voltage Range (V_I) The range of voltage which if exceeded at either input terminal will cause the amplifier to cease functioning properly.

Common-Mode Output Voltage (V_{OC}) The average of the d-c voltages at the two output terminals.

Output Offset Voltage (V_{OO}) The difference between the d-c voltages at the two output terminals when the input terminals are grounded.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage swing that can be obtained without clipping. This includes the unbalance caused by output offset voltage.

Input Resistance (r_i) The resistance between the input terminals with either input grounded.

Output Resistance (r_o) The resistance between either output terminal and ground.

Input Capacitance (C_i) The capacitance between the input terminals with either input grounded.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in output offset voltage referred to the input.

Supply Voltage Rejection Ratio ($\Delta V_{CC}/\Delta V_{IO}$) The ratio of the change in power supply voltages to the change in output offset voltage referred to the input. For these devices, both supply voltages are varied symmetrically.

Propagation Delay Time (t_{pd}) The interval between the application of an input voltage step and its arrival at either output, measured at 50% of the final value.

Rise Time (t_r) The time required for an output voltage step to change from 10% to 90% of its final value.

Maximum Output Sink Current ($I_{sink(max)}$) The maximum available current into either output terminal when that output is at its most negative potential.

PARAMETER MEASUREMENT INFORMATION

test circuits

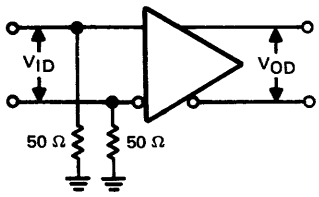

FIGURE 1

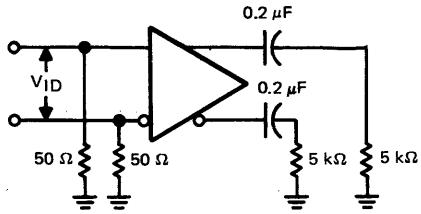

FIGURE 2

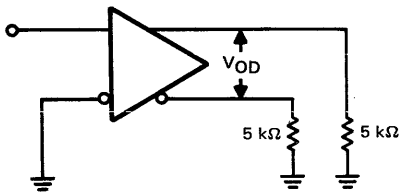

FIGURE 3

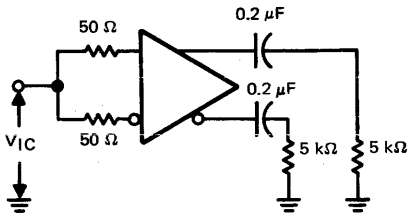

FIGURE 4

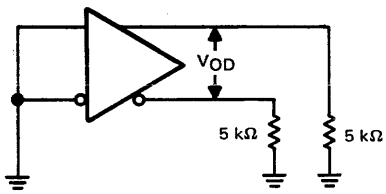

FIGURE 5

THERMAL INFORMATION

DISSIPATION DERATING CURVE

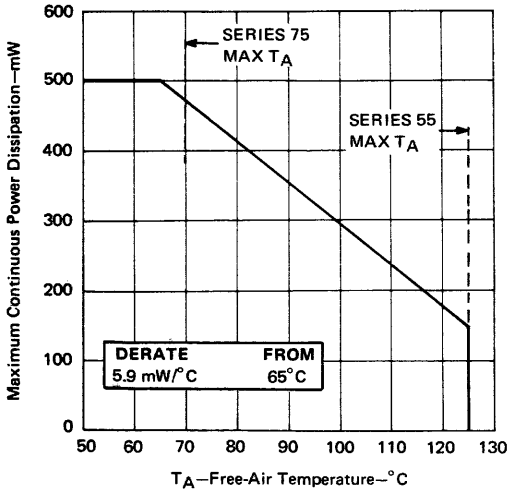

FIGURE 6

TYPICAL APPLICATION DATA

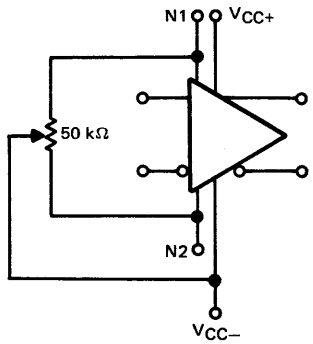

FIGURE 7—SN5512/SN7512
INPUT-OFFSET-VOLTAGE NULL CIRCUIT

TEXAS INSTRUMENTS
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line drivers

TYPE	SN55109, SN75109	SN55110, SN75110	SN75113*	SN75114*	SN75150†	SN75450A
• Operating Frequency	> 10 MHz	> 10 MHz	> 10 MHz	> 10 MHz	10 kHz at 2500-pF Load	< 1 MHz
• Type of Lines	Balanced or Single-Ended	Balanced or Single-Ended	Balanced or Single-Ended	Balanced or Single-Ended	Single-Ended	Balanced or Single-Ended
• Length of Line	Up to 5,000'	Up to 10,000'	Up to 1,000'	Up to 1,000'	Up to 500'	Up to 500'
• Input	TTL	TTL	TTL	TTL	TTL	TTL
• Output	Current Mode	Current Mode	Voltage Mode	Voltage Mode	Voltage Mode	Current Mode
• Party Line Operation	Yes	Yes	Yes	Yes	No	Yes
• Strobe Control	Yes	Yes	Yes	No	No	
• Power Supply	+5 V and −5 V	+5 V and −5 V	+5 V	+5 V	+12 V and −12 V	+5 V
Packages	J, N	J, N	J, N	J, N	J, N, P	N
Application Notes	CA130: Line Drivers and Receivers CA146: Data Transmission					CA150-Peripheral Interface Circuits

3

line receivers

TYPE	SN55107A, SN75107A	SN55108A, SN75108A	SN55115,* SN75115*	SN75154*
• Input Sensitivity, Max	25 mV	25 mV	0.5 V	
• Switching Time, Max	25 ns	25 ns	50 ns	50 ns
• Strobe Capability	Yes	Yes	Yes	No
• Output	TTL, Active Pull-Up	TTL, Open-Collector	TTL, Open-Collector With Active Pull-Up Option	TTL, Active Pull-Up
• Fan-Out to Series 54	10	10	10	10
• Power Supply	+5 V and −5 V	+5 V and −5 V	+5 V	+5 V or +12 V
Packages	J, N	J, N	J, N	J, N
Application Notes	CA130: Line Drivers and Receivers CA146: Data Transmission			

*To be announced soon

†Satisfies requirements of EIA standard RS-232-C

TYPE SN75100L
DUAL DIFFERENTIAL LINE RECEIVER

SERIES 75 LINE RECEIVER

featuring

- **High Input Impedance**
- **Fast Switching Speed**
- **Good Small-Signal Sensitivity**
- **TTL and DTL Compatible Outputs**
- **Wire-OR Output Capability**

description

The SN75100L is a monolithic, dual line receiver which consists of two independent discriminator/buffer circuits in a single package. Each line receiver is composed of a voltage-sensitive, differential-input comparator which drives an open-collector, saturated-logic buffer. This device is designed to operate throughout the temperature range of 0°C to 70°C with a maximum switching time of 40 nanoseconds. The buffer output is at a logical 1 voltage level when the voltage at the signal input is at least 100 millivolts more positive than the reference voltage applied at V_{ref}. The output is at a logical 0 level when the voltage at the signal input is at least 100 millivolts more negative than the reference voltage applied at V_{ref}.

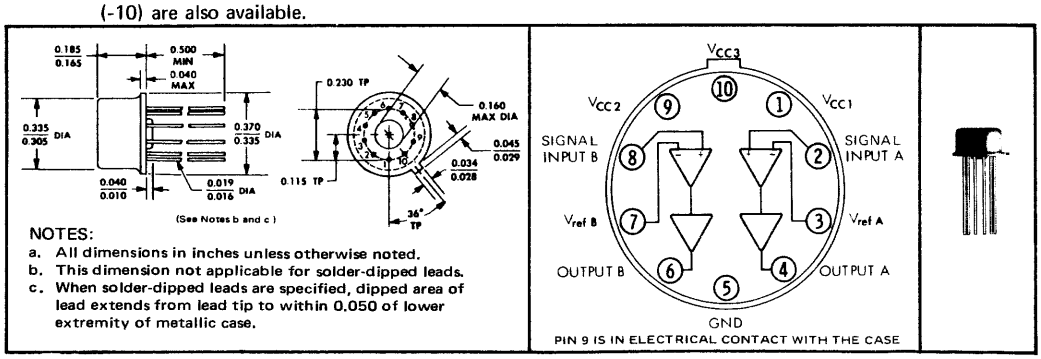
The line receiver has a common-mode input voltage range of -1.5 volts to 1.5 volts which means that both inputs can withstand common voltages of as much as 1.5 volts above or below ground. The buffer output will produce the correct logic-level output for a minimum difference in voltage of 100 millivolts between the differential inputs.

For normal single-ended operation, the data transmission line is connected to the signal input with a fixed d-c voltage between -1.5 volts and 1.5 volts applied at V_{ref}. For maximum noise immunity, the d-c voltage level at V_{ref} should be set midway between the logical 0 and logical 1 voltage levels of the input signal. Alternatively, the functions of the signal and reference-voltage inputs may be interchanged.

When the line receiver is used in a differential mode with balanced two-wire lines, one wire is connected to the signal input and the other wire is connected to V_{ref}. Since a maximum difference of 100 millivolts between the signal input and V_{ref} will assure a given logical level at the buffer output, a trade-off between input sensitivity and common-mode rejection can be made by using external voltage dividers at the inputs.

mechanical data

The SN75100L package outline is the same as JEDEC TO-100 except for diameter of standoff. Gold-plated leads (-00) require no additional cleaning or processing for use in soldered assembly. Solder-dipped leads (-10) are also available.



NOTES:
a. All dimensions in inches unless otherwise noted.
b. This dimension not applicable for solder-dipped leads.
c. When solder-dipped leads are specified, dipped area of lead extends from lead tip to within 0.050 of lower extremity of metallic case.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltages (See Note 1): V_{CC1} . . . . . 10 V
V_{CC2} . . . . . -10 V
V_{CC3} . . . . . 6 V
Differential input voltage, V_{inD} (See Note 2) . . . . . ±5 V
Input voltage, V_{in} or V_{ref} (See Note 1) . . . . . ±5.5 V
Maximum current into the output, I_{sink} . . . . . 60 mA
Continuous power dissipation at (or below) 25°C free-air temperature (See Note 3) . . . . . 680 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . -65°C to 150°C

recommended operating conditions

Supply voltages (See Note 1): V_{CC1} . . . . . 8 V ± 10%
V_{CC2} . . . . . -8 V ± 10%
V_{CC3} . . . . . 4 V ± 10%
Reference voltage, V_{ref} . . . . . -1.5 V to 1.5 V

3

NOTES: 1. These voltage values are with respect to network ground terminal.
2. These voltage values are with respect to the other differential-input terminal.
3. Derate linearly to 435 mW at 70°C free-air temperature at the rate of 5.4 mW/°C.

electrical characteristics (unless otherwise noted, V_{CC1} = 8 V, V_{CC2} = -8 V, V_{CC3} = 4 V, T_A = 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{inD(0)}$	Logical 0 input voltage at the signal input, with respect to V_{ref}, required to ensure logical 0 level at the output	1	V_{ref} = -1.5 V to 1.5 V	-100			mV
$V_{inD(1)}$	Logical 1 input voltage at the signal input, with respect to V_{ref}, required to ensure logical 1 level at the output	1	V_{ref} = -1.5 V to 1.5 V	100			mV
$V_{out(0)}$	Logical 0 output voltage	2	V_{in} = -2 V to 1.4 V, V_{ref} = 1.5 V, I_{sink} = 40 mA		0.25	0.5	V
			V_{in} = -2 V to -1.6 V, V_{ref} = -1.5 V, I_{sink} = 40 mA		0.25	0.5	V
$I_{out(1)}$	Output reverse current	2	V_{in} = -1.4 V to 3.5 V, V_{ref} = -1.5 V, V_{out} = 5.5 V			250	μA
I_{in}	Input current into the signal input	3	V_{ref} = -1.5 V, See Note 4		20	50	μA
$I_{in(ref)}$	Input current into V_{ref}	3	V_{ref} = 1.5 V, See Note 4		20	50	μA
I_{CC1}	V_{CC1} supply current	4	V_{CC1} = 8.8 V		15	22	mA
I_{CC2}	V_{CC2} supply current	4	V_{CC2} = -8.8 V		-13	-17	mA
I_{CC3}	V_{CC3} supply current	4	V_{CC3} = 4.4 V		10	20	mA

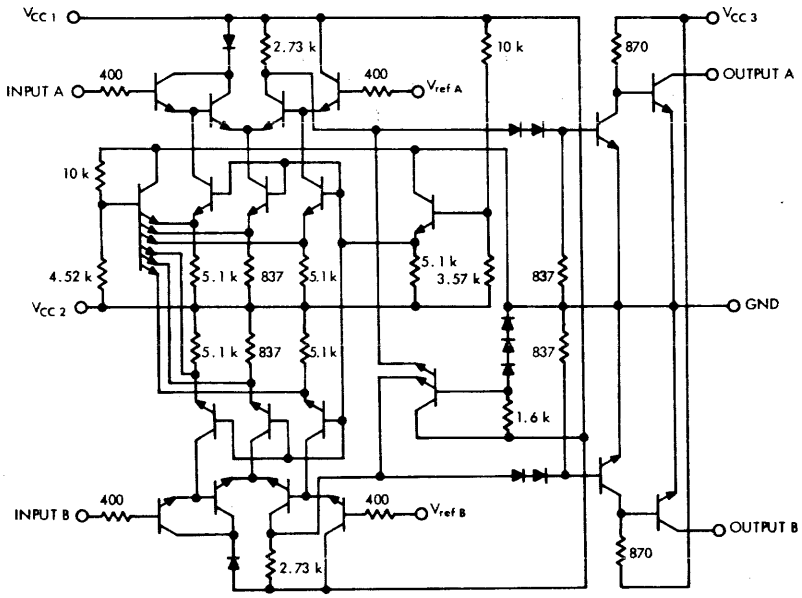
†All typical values are at 25°C.

NOTE: 4. The maximum value specified is also applicable under any combination of the following conditions:
a. V_{CC1} is open, grounded, or at 8 V ± 10%.
b. V_{CC2} is open, grounded, or at -8 V ± 10%.
c. V_{CC3} is open, grounded, or at 4 V.
d. V_{in} = 2 V to 4.4 V.

switching characteristics, V_{CC1} = 8 V, V_{CC2} = -8 V, V_{CC3} = 4 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd(1)}$	Propagation delay time to logical 1 level	5	R_L = 100 Ω, C_L = 20 pF, V_L = 4 V, f = 1 MHz		20	40	ns
$t_{pd(0)}$	Propagation delay time to logical 0 level	5			20	40	ns

schematic diagram



NOTE: All resistor values are in ohms.

PARAMETER MEASUREMENT INFORMATION †

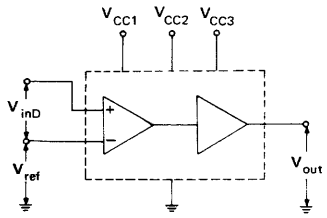


FIGURE 1–$V_{inD(0)}$ and $V_{inD(1)}$

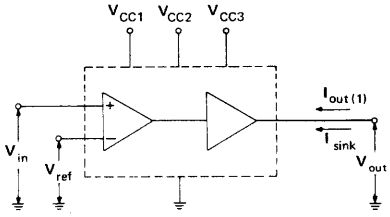


FIGURE 2–$V_{out(0)}$ and $I_{out(1)}$

†Arrows indicate direction of current flow.

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PARAMETER MEASUREMENT INFORMATION †

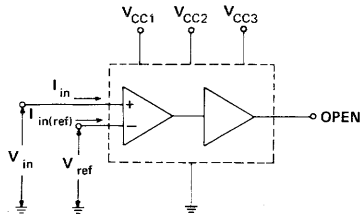


FIGURE 3—I_{in} and $I_{in(ref)}$

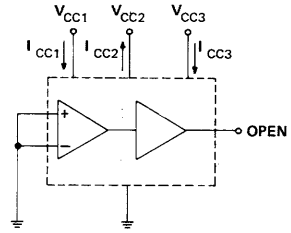
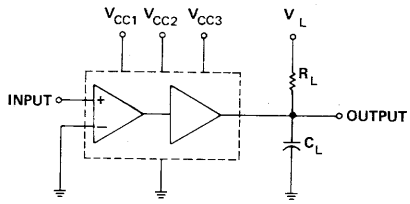
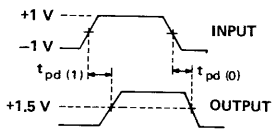


FIGURE 4—I_{CC1}, I_{CC2}, and I_{CC3}



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 5—$t_{pd(1)}$ and $t_{pd(0)}$

†Arrows indicate direction of current flow.

3

TYPICAL APPLICATION DATA

The SN75100L is ideally suited for use as a differential or single-ended line receiver. Maximum flexibility is ensured by the high-impedance inputs and open-collector outputs. The outputs are compatible for driving TTL or DTL digital circuits and may be combined to perform the wire-OR function.

When used in a single-ended "party line" data-transmission system, transmission lines may be either a twisted pair or coaxial cable. See Figure A.

By terminating the transmission line at each end, a two-way signal path may be utilized. The SN75100L provides very little loading to the transmission line due to its high input impedance. Therefore, transmitter/receiver pairs may be tied into the line anywhere along its length without disturbing the impedance level of the line.

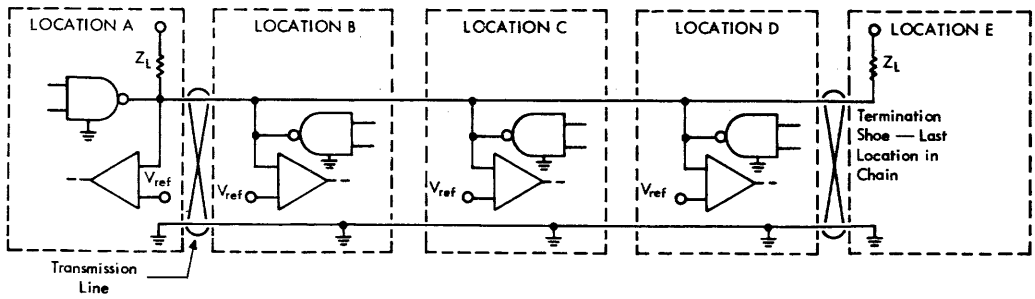


FIGURE A

CIRCUIT TYPES SN55107A, SN55108A, SN55109, SN55110, SN75107A, SN75108A, SN75109, SN75110 DUAL LINE RECEIVERS AND DRIVERS

SERIES 55/75107A LINE CIRCUITS
featuring

• High Speed • Standard Supply Voltages • Dual Channels

additional features of line receivers

- high common-mode rejection ratio
- high input impedance
- high input sensitivity
- differential input common-mode voltage range of ± 3 V
- differential input common-mode voltage range of more than ±15 V using external attenuator
- strobe inputs for receiver selection
- gate inputs for logic versatility
- TTL or DTL drive capability
- high d-c noise margins

–55°C to 125°C J Package	0°C to 70°C J or N Package	CIRCUIT FUNCTION	OUTPUT FUNCTION
SN55107A	SN75107A	Dual Line Receiver	Active Pull-Up
SN55108A	SN55108A	Dual Line Receiver	Open Collector
SN55109	SN75109	Dual Line Driver	6-mA Current Switch
SN55110	SN75110	Dual Line Driver	12-mA Current Switch

additional features of line drivers

- TTL input compatibility
- current-mode output (6 mA or 12 mA typical)
- high output impedance
- high common-mode output voltage range (–3 V to 10 V)
- inhibitor available for driver selection

description

The Series 55/75107 circuits are TTL/DTL compatible high-speed line receivers and drivers. Each is a monolithic dual circuit featuring two independent channels.

The SN55107A, SN55108A, SN75107A, and SN75108A line receivers are designed for general use as well as such specific applications as data comparators and balanced, unbalanced, and party-line transmission systems. These devices are unilaterally interchangeable with and replace SN55107, SN55108, SN75107, and SN75108, respectively, but offer diode-clamped inputs to simplify circuit design.

The SN55109, SN55110, SN75109, and SN75110 line drivers are designed to be used in many categories of applications in balanced, unbalanced, and party-line systems and as level converters.

The SN55107A, SN55108A, SN55109, and SN55110 are characterized for operation over the full military temperature range of –55°C to 125°C, and are available in the ceramic dual-in-line (J) package. The SN75107A, SN75108A, SN75109, and SN75110 are characterized for operation from 0°C to 70°C and are available either in the ceramic dual-in-line (J) package or in the plastic dual-in-line (N) package.

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CIRCUIT TYPES SN55107A, SN55108A, SN55109, SN55110, SN75107A, SN75108A, SN75109, SN75110 DUAL LINE RECEIVERS AND DRIVERS

design characteristics

Series 55/75107A Line Circuits are TTL-compatible dual circuits intended for use in high-speed data-transmission systems. The drivers are designed to drive balanced, terminated transmission lines, such as twisted-pair, at normal line impedances without high power dissipation. The receivers are designed to detect low-level differential signals in the presence of common-mode noise and variations of temperature and supplies. Either driver may be used with either receiver. Specifications reflect worst-case conditions of temperature, supply voltages, and input voltages.

line receivers - SN55/75107A, SN55/75108A

The SN55/75107A and SN55/75108A are dual line receivers featuring independent channels with common voltage supply and ground terminals. The SN55/75107A circuit features a TTL-compatible active pull-up (totem-pole) output. The SN55/75108A circuit is also TTL-compatible, but features an open-collector output configuration that permits the dot-OR logic connection with similar outputs (such as the SN54/74101 TTL gate or other SN55/75108A line receivers). This permits a level of logic to be implemented without extra delay. All other features of the line receivers are identical.

The SN55/75107A and SN55/75108A line circuits are designed to detect input signals of 25 millivolts (or greater) amplitude and convert the polarity of the signal into appropriate TTL-compatible output logic levels.

The SN55/75107A and SN55/75108A feature high input impedance and low input currents which induce very little loading on the transmission line. This makes these devices especially useful in party-line systems. The excellent input sensitivity (3 millivolts typical) is particularly important when data is to be detected at the end of a long transmission line and the amplitude of the data has been deteriorated due to cable losses.

The receiver input common-mode voltage range is ±3 volts. This is adequate for application in most systems. In systems with requirements for greater common-mode voltage range, input attenuators may be used to decrease the noise to an acceptable level at the receiver-input terminals.

The receivers feature individual strobe inputs for each channel and a strobe input common to both channels for logic versatility. The strobe inputs are tested to guarantee 400 millivolts of d-c noise margin when interfaced with Series 54/74 TTL.

line drivers - SN55/75109, SN55/75110

The SN55/75109 and SN55/75110 are dual line drivers featuring independent channels with common voltage supply and ground terminals. The significant difference between the two drivers is in the output-current specification. The driver circuits feature a constant output current that is switched to either of two output terminals by the appropriate logic levels at the input terminals. The output current can be switched off (inhibited) by appropriate logic levels on the inhibit inputs. The output current is nominally 6 milliamperes for the SN55/75109 and 12 milliamperes for the SN55/75110. System design determines which driver is best suited to a particular application.

The inhibit feature is provided so the circuits can be used in party-line or data-bus applications. A strobe or inhibitor, common to both drivers, is included for increased driver-logic versatility. The output current in the inhibited mode, $I_{O(off)}$, is specified so that minimum line loading is induced when the driver is used in a party-line system with other drivers. The output impedance of the driver in the inhibited mode is very high—the output impedance of a transistor biased to cutoff.

The driver outputs have a common-mode voltage range of −3 volts to +10 volts, allowing common-mode voltage on the line without affecting driver performance.

The logic and inhibit inputs of the drivers are designed to satisfy TTL-system requirements. The logic inputs are tested at 2.0 volts for high-logic-level conditions and 0.8 volt for low-logic-level conditions. These tests guarantee 400 millivolts of noise margin when interfaced with Series 54/74 TTL.

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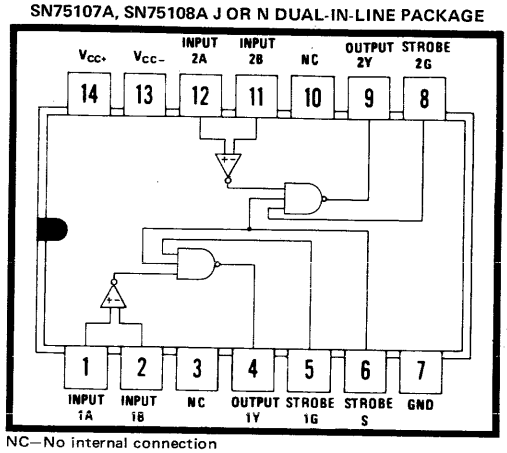
CIRCUIT TYPES SN55107A, SN55108A, SN75107A, SN75108A
DUAL LINE RECEIVERS

logic

TRUTH TABLE

DIFFERENTIAL INPUTS A-B	STROBES G	STROBES S	OUTPUT Y
$V_{ID} \geq 25$ mV	L or H	L or H	H
-25 mV $< V_{ID} < 25$ mV	L or H	L	H
	L	L or H	H
	H	H	INDETERMINATE
$V_{ID} \leq -25$ mV	L or H	L	H
	L	L or H	H
	H	H	L

SN55107A, SN55108A J DUAL-IN-LINE PACKAGE
SN75107A, SN75108A J OR N DUAL-IN-LINE PACKAGE



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

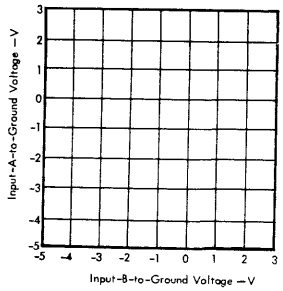
Supply voltage V_{CC+} (See Note 1) . . . . . 7 V
Supply voltage V_{CC-} (See Note 1) . . . . . −7 V
Differential input voltage (See Note 2) . . . . . ±6 V
Common-mode input voltage (See Note 1) . . . . . ±5 V
Strobe input voltage (See Note 1) . . . . . 5.5 V
Operating free-air temperature range, Series 55 . . . . . −55°C to 125°C
Series 75 . . . . . 0°C to 70°C
Storage temperature range, ceramic dual-in-line (J) package . . . . . −65°C to 150°C
plastic dual-in-line (N) package . . . . . −55°C to 150°C

recommended operating conditions (see note 3)

	SN55107A, SN55108A MIN	NOM	MAX	SN75107A, SN75108A MIN	NOM	MAX	UNIT
Supply voltage V_{CC+} (See Note 1)	4.5	5	5.5	4.75	5	5.25	V
Supply voltage V_{CC-} (See Note 1)	−4.5	−5	−5.5	−4.75	−5	−5.25	V
Output sink current			−16			−16	mA
Differential input voltage (See Notes 2 and 4)	−5†		5	−5†		5	V
Common-mode input voltage (See Notes 1 and 4)	−3†		3	−3†		3	V
Input voltage range, any differential input to ground (See Note 4)	−5†		3	−5†		3	V
Operating free-air temperature range	−55		125	0		70	°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. These voltage values are at the noninverting (+) terminal with respect to the inverting (−) terminal.
3. When using only one channel of the line receiver, the inputs of the other channel should be grounded.
4. The recommended combinations of input voltages fall within the shaded area of the figure at the right.

RECOMMENDED COMBINATIONS OF INPUT VOLTAGES FOR LINE RECEIVERS



†The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic voltage levels only.

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definition of input logic levels†

		TEST FIGURE	MIN	MAX	UNIT
V_{IDH}	High-level input voltage between differential inputs	1	0.025	5	V
V_{IDL}	Low-level input voltage between differential inputs	1	−5	−0.025	V
$V_{IH(S)}$	High-level input voltage at strobe inputs	3	2	5.5	V
$V_{IL(S)}$	Low-level input voltage at strobe inputs	3	0	0.8	V

†The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS‡		SN55107A, SN75107A			SN55108A, SN75108A			UNIT
					MIN	TYP§	MAX	MIN	TYP§	MAX	
I_{IH}	High-level input current into 1A or 2A	2	V_{CC+} = MAX, V_{ID} = 0.5 V,	V_{CC-} = MAX, V_{IC} = −3 V to 3 V		30	75		30	75	μA
I_{IL}	Low-level input current into 1A or 2A	2	V_{CC+} = MAX, V_{ID} = −2 V,	V_{CC-} = MAX, V_{IC} = −3 V to 3 V			−10			−10	μA
I_{IH}	High-level input current into 1G or 2G	4	V_{CC+} = MAX, $V_{IH(S)}$ = 2.4 V	V_{CC-} = MAX,			40			40	μA
			V_{CC+} = MAX, $V_{IH(S)}$ = MAX V_{CC+}	V_{CC-} = MAX,			1			1	mA
I_{IL}	Low-level input current into 1G or 2G	4	V_{CC+} = MAX, $V_{IL(S)}$ = 0.4 V	V_{CC-} = MAX,			−1.6			−1.6	mA
I_{IH}	High-level input current into S	4	V_{CC+} = MAX, $V_{IH(S)}$ = 2.4 V	V_{CC-} = MAX,			80			80	μA
			V_{CC+} = MAX, $V_{IH(S)}$ = MAX V_{CC+}	V_{CC-} = MAX,			2			2	mA
I_{IL}	Low-level input current into S	4	V_{CC+} = MAX, $V_{IL(S)}$ = 0.4 V	V_{CC-} = MAX,			−3.2			−3.2	mA
V_{OH}	High-level output voltage	3	V_{CC+} = MIN, I_{load} = −400 μA,	V_{CC-} = MIN, V_{IC} = −3 V to 3 V	2.4						V
V_{OL}	Low-level output voltage	3	V_{CC+} = MIN, I_{sink} = 16 mA,	V_{CC-} = MIN, V_{IC} = −3 V to 3 V			0.4			0.4	V
I_{OH}	High-level output current	3	V_{CC+} = MIN, V_{OH} = MAX V_{CC+}	V_{CC-} = MIN,						250	μA
I_{OS}	Short-circuit output current	5	V_{CC+} = MAX,	V_{CC-} = MAX	−18		−70				mA
I_{CCH+}	High-logic-level supply current from V_{CC+}	6	V_{CC+} = MAX, V_{ID} = 25 mV,	V_{CC-} = MAX, T_A = 25°C		18	30		18	30	mA
I_{CCH-}	High-logic-level supply current from V_{CC-}	6	V_{CC+} = MAX, V_{ID} = 25 mV,	V_{CC-} = MAX, T_A = 25°C		−8.4	−15		−8.4	−15	mA

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

§ All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

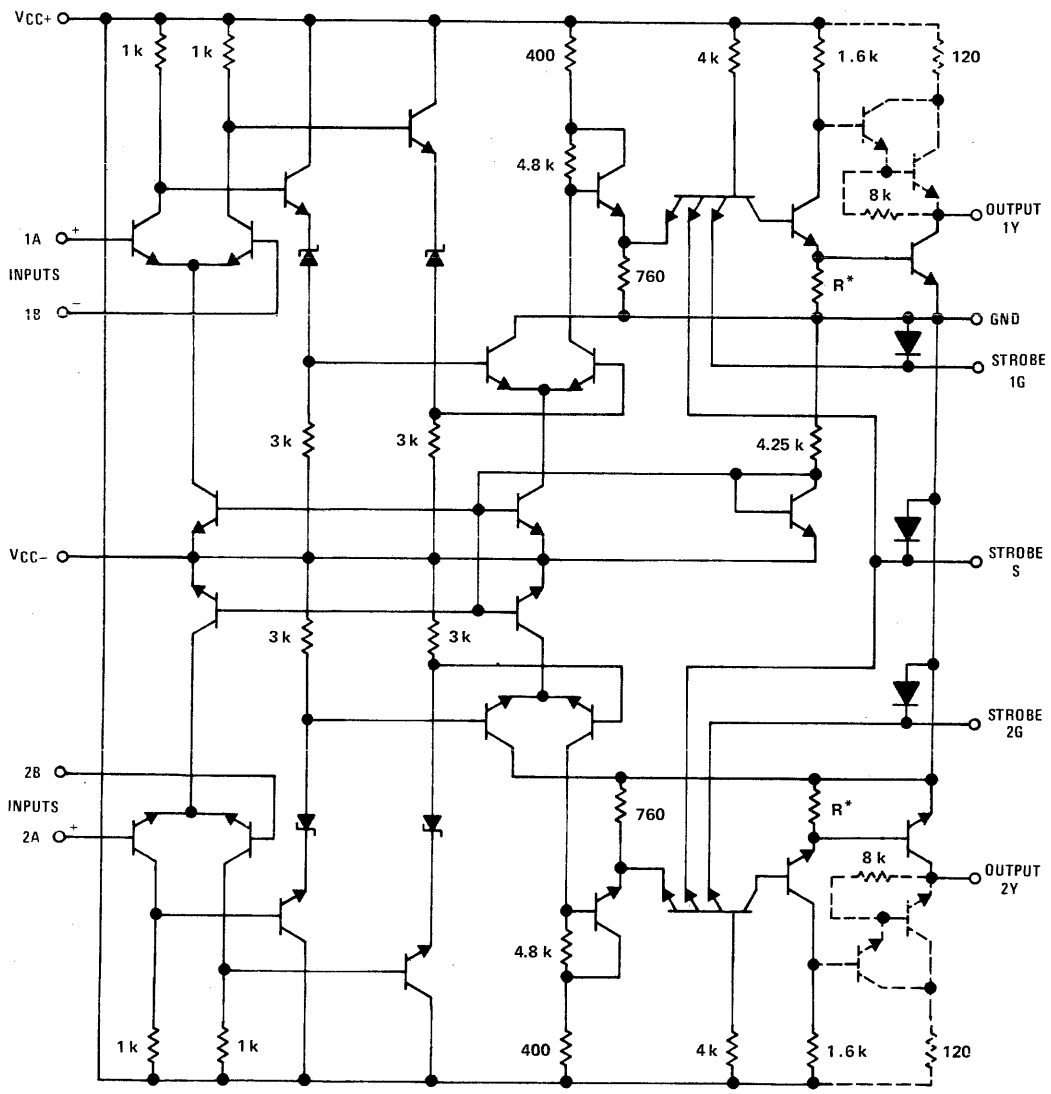
¶ Not more than one output should be shorted at a time.

switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		SN55107A, SN75107A			SN55108A, SN75108A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
$t_{PLH(D)}$	Propagation delay time, low-to-high level, from differential inputs A and B to output	7	R_L = 390 Ω,	C_L = 50 pF		17	25				ns
			R_L = 390 Ω,	C_L = 15 pF					19	25	
$t_{PHL(D)}$	Propagation delay time, high-to-low level, from differential inputs A and B to output	7	R_L = 390 Ω,	C_L = 50 pF		17	25				ns
			R_L = 390 Ω,	C_L = 15 pF					19	25	
$t_{PLH(S)}$	Propagation delay time, low-to-high level, from strobe input G or S to output	7	R_L = 390 Ω,	C_L = 50 pF		10	15				ns
			R_L = 390 Ω,	C_L = 15 pF					13	20	
$t_{PHL(S)}$	Propagation delay time, high-to-low level, from strobe input G or S to output	7	R_L = 390 Ω,	C_L = 50 pF		8	15				ns
			R_L = 390 Ω,	C_L = 15 pF					13	20	

3

schematic



R* = 1 kΩ for SN55107A and SN75107A, 750 Ω for SN55108A and SN75108A.

NOTES: 1. Component values shown are nominal.
2. Resistance values are in ohms.
3. Components shown with dashed lines are applicable to the SN55107A and SN75107A only.

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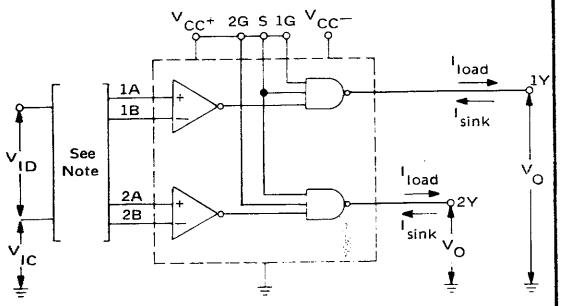
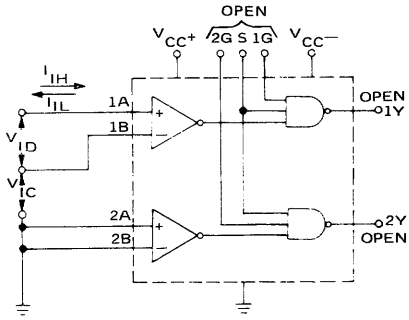
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



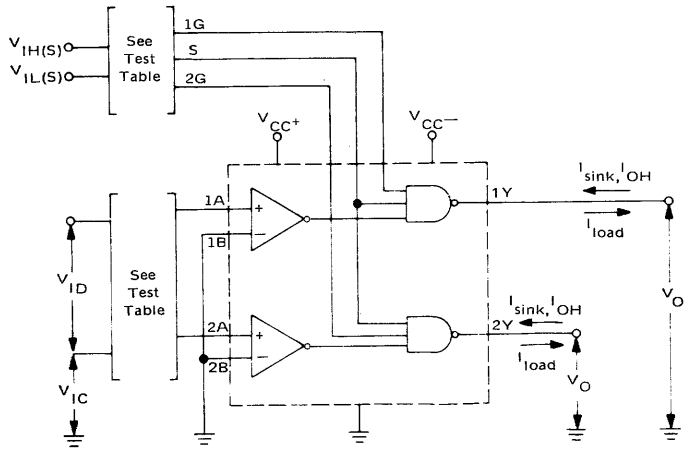
NOTE: When testing one channel, the inputs of the other channel are grounded.

FIGURE 1–V_{IDH} and V_{IDL}



NOTE: Each pair of differential inputs is tested separately. The inputs of the other pair are grounded.

FIGURE 2–I_{IH} and I_{IL}



TEST TABLE

SN55107A SN75107A	SN55108A SN75108A	V_{ID}	STROBE 1G or 2G	STROBE S
TEST		APPLY		
V_{OH}	I_{OH}	+25 mV	$V_{IH(S)}$	$V_{IH(S)}$
V_{OH}	I_{OH}	-25 mV	$V_{IL(S)}$	$V_{IH(S)}$
V_{OH}	I_{OH}	-25 mV	$V_{IH(S)}$	$V_{IL(S)}$
V_{OL}	V_{OL}	-25 mV	$V_{IH(S)}$	$V_{IH(S)}$

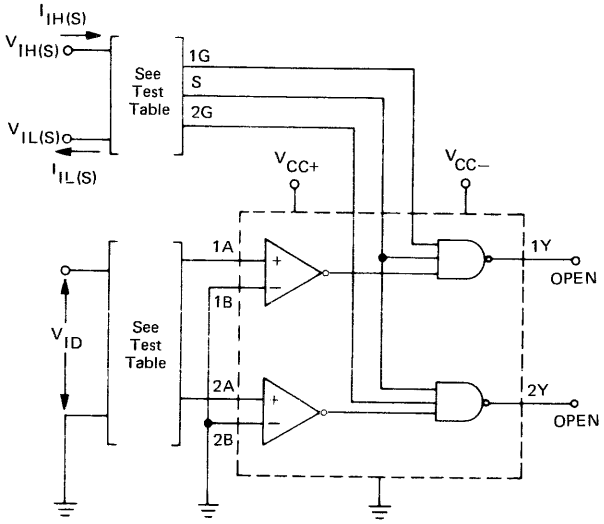
NOTES: 1. V_{IC} = −3 V to 3 V.
2. When testing one channel, the inputs of the other channel should be grounded.

FIGURE 3–$V_{IH(S)}$, $V_{IL(S)}$, V_{OH}, V_{OL}, and I_{OH}

† Arrows indicate actual direction of current flow.

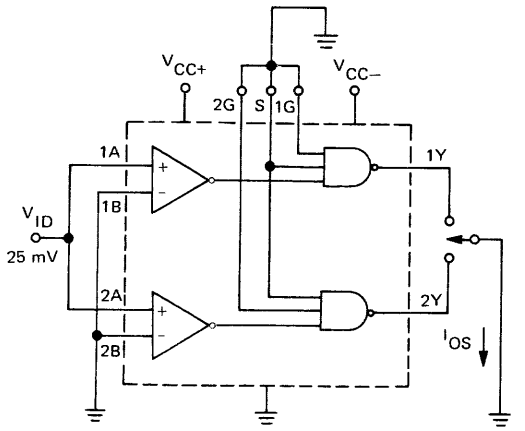
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST	INPUT 1A	INPUT 2A	STROBE 1G	STROBE S	STROBE 2G
I_{IH} at Strobe 1G	+25 mV	Gnd	$V_{IH(S)}$	Gnd	Gnd
I_{IH} at Strobe 2G	Gnd	+25 mV	Gnd	Gnd	$V_{IH(S)}$
I_{IH} at Strobe S	+25 mV	+25 mV	Gnd	$V_{IH(S)}$	Gnd
I_{IL} at Strobe 1G	−25 mV	Gnd	$V_{IL(S)}$	4.5 V	Gnd
I_{IL} at Strobe 2G	Gnd	−25 mV	Gnd	4.5 V	$V_{IL(S)}$
I_{IL} at Strobe S	−25 mV	−25 mV	4.5 V	$V_{IL(S)}$	4.5 V

FIGURE 4 – $I_{IH(G)}$, $I_{IL(G)}$, $I_{IH(S)}$, and $I_{IL(S)}$



NOTES: 1. Each channel is tested separately.
2. Not more than one output should be grounded at a time.

FIGURE 5–I_{OS}

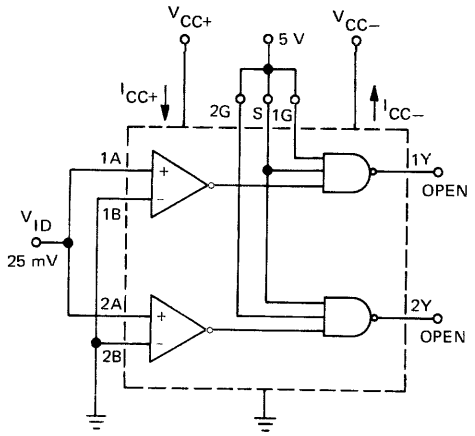


FIGURE 6–I_{CC+} and I_{CC-}

† Arrows indicate actual direction of current flow.

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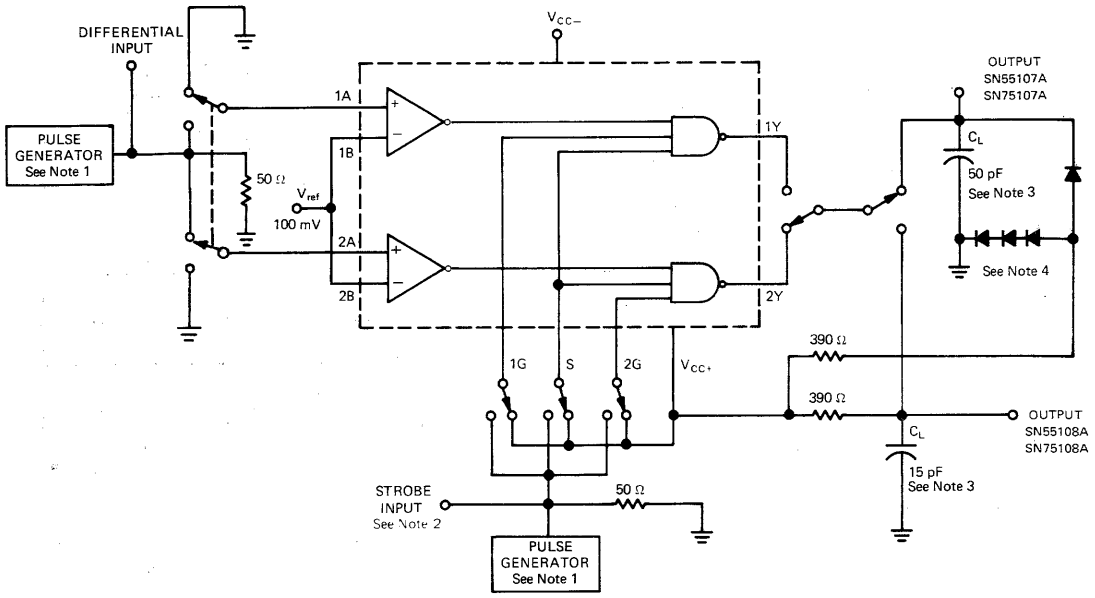
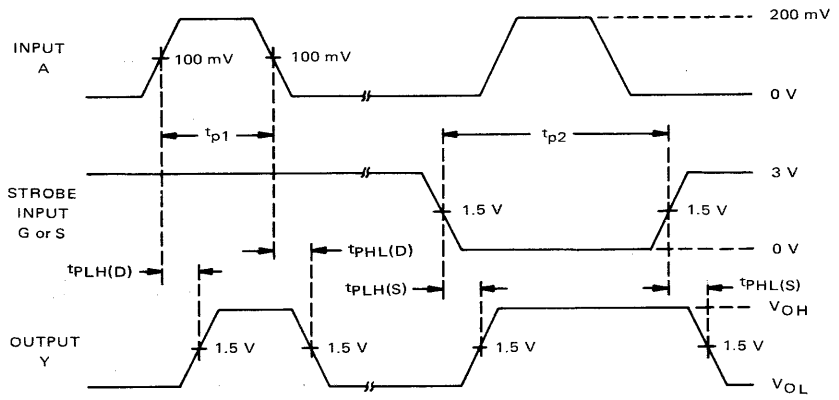
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f = 10 \pm 5$ ns, t_{p1} = 500 ns, PRR = 1 MHz, t_{p2} = 1 ms, PRR = 500 kHz.
2. Strobe input pulse is applied to Strobe 1G when inputs 1A-1B are being tested, to Strobe S when inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A-2B are being tested.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N916.

FIGURE 7—PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

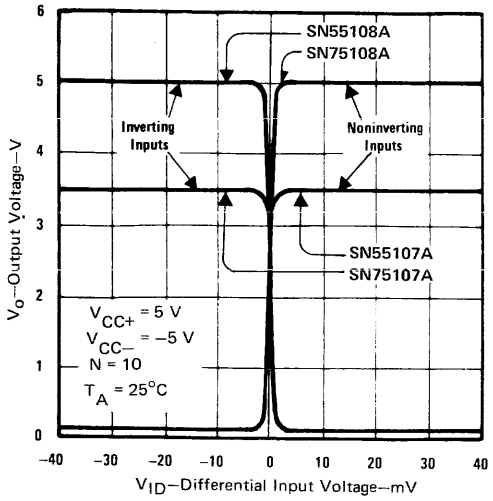


FIGURE 8

HIGH-LEVEL INPUT CURRENT
INTO 1A or 2A
vs
FREE-AIR TEMPERATURE

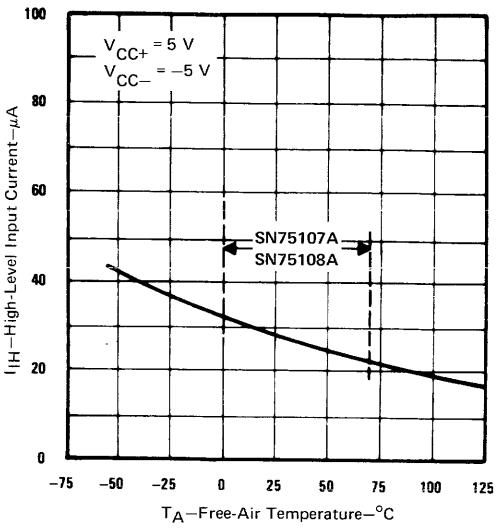


FIGURE 9

HIGH-LOGIC-LEVEL SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

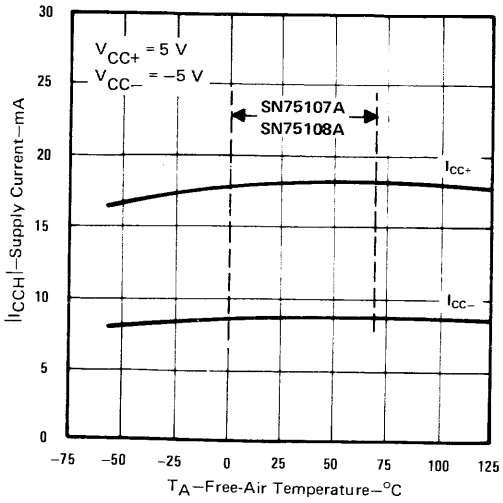


FIGURE 10

SN55107A, SN75107A
PROPAGATION DELAY TIME
(DIFFERENTIAL INPUTS)
vs
FREE-AIR TEMPERATURE

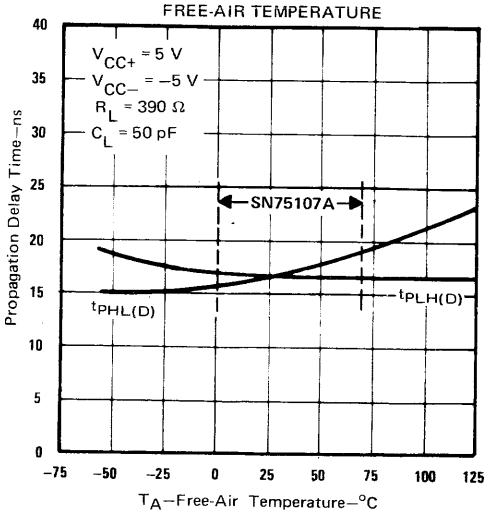


FIGURE 11

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TYPICAL CHARACTERISTICS

SN55108A, SN75108A
PROPAGATION DELAY TIME
LOW-TO-HIGH LEVEL
(DIFFERENTIAL INPUTS)
vs
FREE-AIR TEMPERATURE

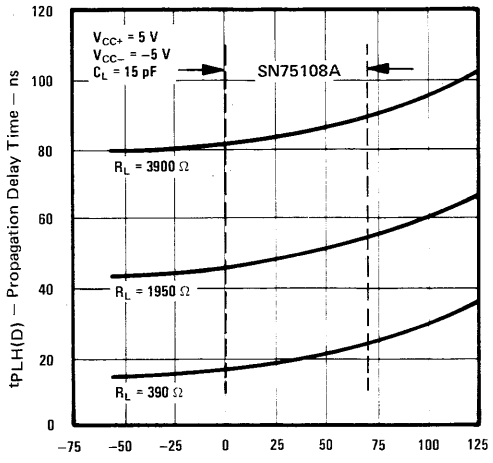


FIGURE 12

SN55108A, SN75108A
PROPAGATION DELAY TIME
HIGH-TO-LOW LEVEL
(DIFFERENTIAL INPUTS)
vs
FREE-AIR TEMPERATURE

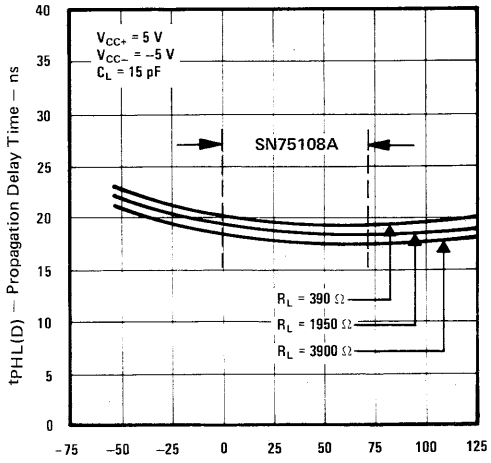


FIGURE 13

SN55107A, SN75107A
PROPAGATION DELAY TIME
(STROBE INPUTS)
vs
FREE-AIR TEMPERATURE

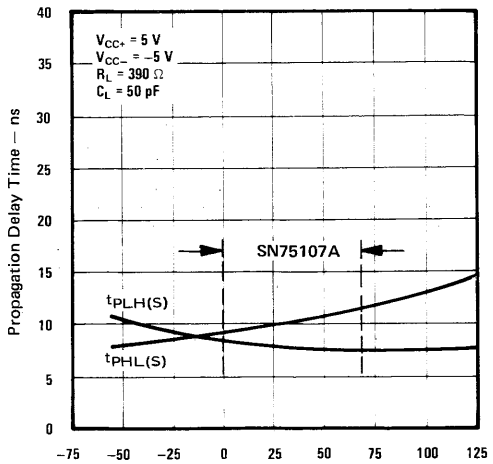


FIGURE 14

SN55108A, SN75108A
PROPAGATION DELAY TIME
(STROBE INPUTS)
vs
FREE-AIR TEMPERATURE

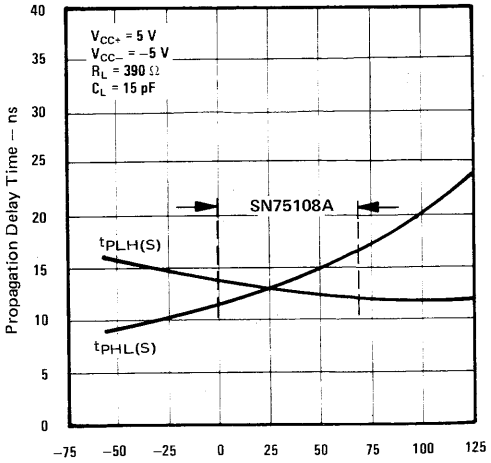
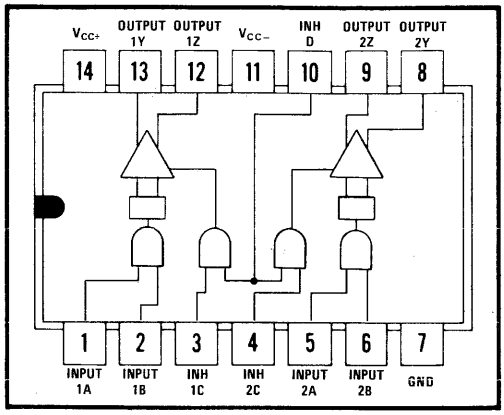


FIGURE 15

3

CIRCUIT TYPES SN55109, SN55110, SN75109, SN75110
DUAL LINE DRIVERS

SN55109, SN55110 J DUAL-IN-LINE PACKAGE
SN75109, SN75110 J OR N DUAL-IN-LINE PACKAGE



logic

TRUTH TABLE

LOGIC INPUTS		INHIBITOR INPUTS		OUTPUTS	
A	B	C	D	Y	Z
L or H	L or H	L	L or H	H	H
L or H	L or H	L or H	L	H	H
L	L or H	H	H	L	H
L or H	L	H	H	L	H
H	H	H	H	H	L

Low output represents the on state

High output represents the off state

3

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (See Note 1) . . . . . 7 V
Supply voltage V_{CC-} (See Note 1) . . . . . −7 V
Logic and inhibitor input voltages (See Note 1) . . . . . 5.5 V
Common-mode output voltage (See Note 1) . . . . . −5 to 12 V
Operating free-air temperature range, Series 55 . . . . . −55°C to 125°C
Series 75 . . . . . 0°C to 70°C
Storage temperature range, ceramic dual-in-line (J) package . . . . . −65°C to 150°C
plastic dual-in-line (N) package . . . . . −55°C to 150°C

recommended operating conditions (see note 2)

	SN55109, SN55110			SN75109, SN75110			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC+} (See Note 1)	4.5	5	5.5	4.75	5	5.25	V
Supply voltage V_{CC-} (See Note 1)	−4.5	−5	−5.5	−4.75	−5	−5.25	V
Positive common-mode output voltage (See Note 1)	0		10	0		10	V
Negative common-mode output voltage (See Note 1)	0		−3	0		−3	V
Operating free-air temperature range	−55		125	0		70	°C

NOTES: 1. These voltage values are with respect to the network ground terminal.
2. When using only one channel of the line drivers, the other channel should be inhibited and/or its outputs grounded.

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definition of input logic levels†

		TEST FIGURE	MIN	MAX	UNIT
V_{IH}	High-level input voltage at any input	16, 17	2	5.5	V
V_{IL}	Low-level input voltage at any input	16, 17	0	0.8	V

†The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS‡	SN55109, SN75109 MIN	SN55109, SN75109 TYP§	SN55109, SN75109 MAX	SN55110, SN75110 MIN	SN55110, SN75110 TYP§	SN55110, SN75110 MAX	UNIT
$I_{IH(L)}$	High-level input current into 1A, 1B, 2A or 2B	16	V_{CC+} = MAX, V_{CC-} = MAX, $V_{IH(L)}$ = 2.4 V			40			40	μA
			V_{CC+} = MAX, V_{CC-} = MAX, $V_{IH(L)}$ = MAX V_{CC+}			1			1	mA
$I_{IL(L)}$	Low-level input current into 1A, 1B, 2A or 2B	16	V_{CC+} = MAX, V_{CC-} = MAX, $V_{IL(L)}$ = 0.4 V			−3			−3	mA
$I_{IH(I)}$	High-level input current into 1C or 2C	17	V_{CC+} = MAX, V_{CC-} = MAX, $V_{IH(I)}$ = 2.4 V			40			40	μA
			V_{CC+} = MAX, V_{CC-} = MAX, $V_{IH(I)}$ = MAX V_{CC+}			1			1	mA
$I_{IL(I)}$	Low-level input current into 1C or 2C	17	V_{CC+} = MAX, V_{CC-} = MAX, $V_{IL(I)}$ = 0.4 V			−3			−3	mA
$I_{IH(I)}$	High-level input current into D	17	V_{CC+} = MAX, V_{CC-} = MAX, $V_{IH(I)}$ = 2.4 V			80			80	μA
			V_{CC+} = MAX, V_{CC-} = MAX, $V_{IH(I)}$ = MAX V_{CC+}			2			2	mA
$I_{IL(I)}$	Low-level input current into D	17	V_{CC+} = MAX, V_{CC-} = MAX, $V_{IL(I)}$ = 0.4 V			−6			−6	mA
$I_{O(on)}$	On-state output current	18	V_{CC+} = MAX, V_{CC-} = MAX			−7			−15	mA
			V_{CC+} = MIN, V_{CC-} = MAX	−3.5			−6.5			mA
$I_{O(off)}$	Off-state output current	18	V_{CC+} = MIN, V_{CC-} = MIN			100			100	μA
$I_{CC+(on)}$	Supply current from V_{CC+} with driver enabled	19	$V_{IL(L)}$ = 0.4 V, $V_{IH(I)}$ = 2 V		18	30		23	35	mA
$I_{CC-(on)}$	Supply current from V_{CC-} with driver enabled	19	$V_{IL(L)}$ = 0.4 V, $V_{IH(I)}$ = 2 V		−18	−30		−34	−50	mA
$I_{CC+(off)}$	Supply current from V_{CC+} with driver inhibited	19	$V_{IL(L)}$ = 0.4 V, $V_{IL(I)}$ = 0.4 V		18			21		mA
$I_{CC-(off)}$	Supply current from V_{CC-} with driver inhibited	19	$V_{IL(L)}$ = 0.4 V, $V_{IL(I)}$ = 0.4 V		−10			−17		mA

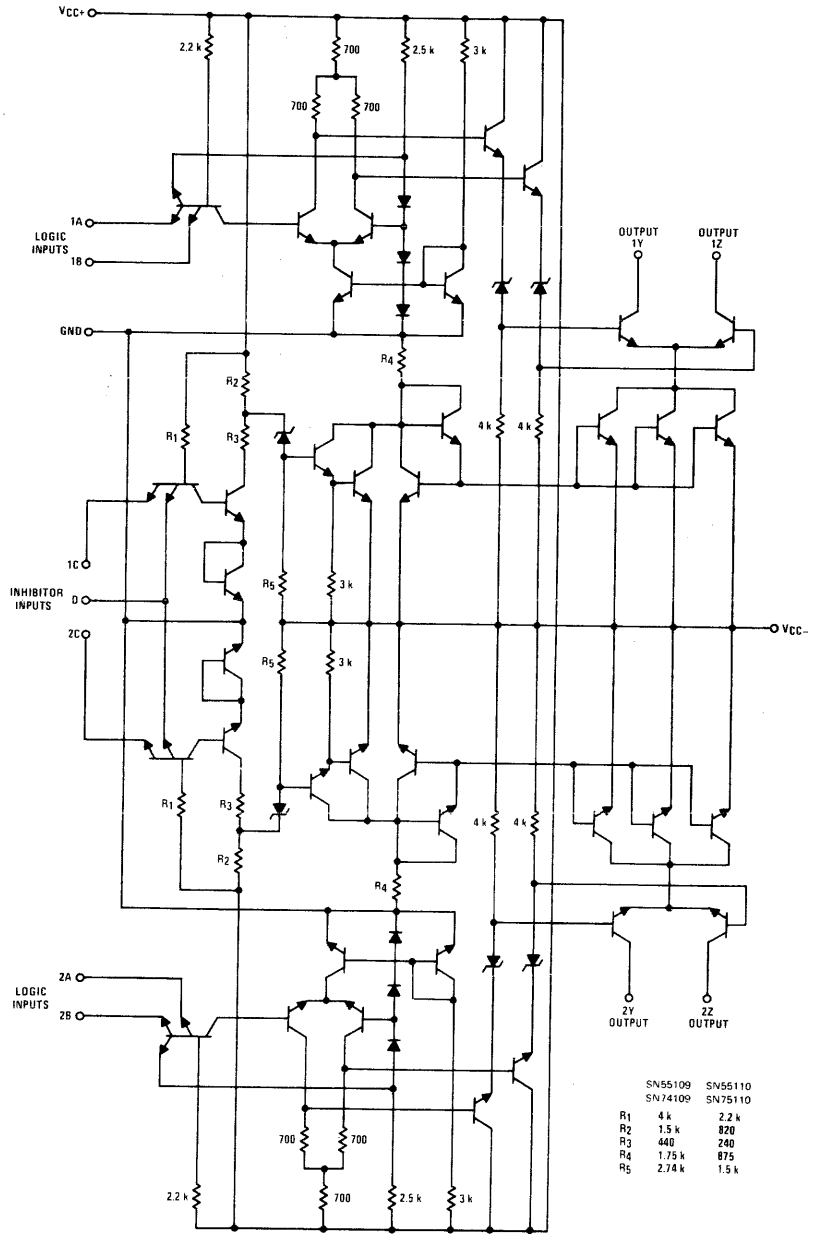
‡For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions for the applicable device type.

§All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

switching characteristics, V_{CC+} = 5 V, V_{CC-} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH(L)}$	Propagation delay time, low-to-high level, from logic input A or B to output Y or Z	20	R_L = 50 Ω, C_L = 40 pF		9	15	ns
$t_{PHL(L)}$	Propagation delay time, high-to-low level, from logic input A or B to output Y or Z	20	R_L = 50 Ω, C_L = 40 pF		9	15	ns
$t_{PLH(I)}$	Propagation delay time, low-to-high level, from inhibitor input C or D to output Y or Z	20	R_L = 50 Ω, C_L = 40 pF		16	25	ns
$t_{PHL(I)}$	Propagation delay time, high-to-low level, from inhibitor input C or D to output Y or Z	20	R_L = 50 Ω, C_L = 40 pF		13	25	ns

schematic



	SN55109 SN74109	SN55110 SN75110
R_1	4 k	2.2 k
R_2	1.5 k	820
R_3	440	240
R_4	1.75 k	875
R_5	2.74 k	1.5 k

NOTES: 1. Component values shown are nominal.
2. Resistance values are in ohms.

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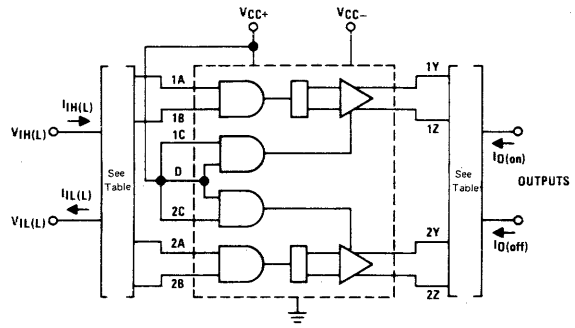
PARAMETER MEASUREMENT INFORMATION

d-c test circuits †

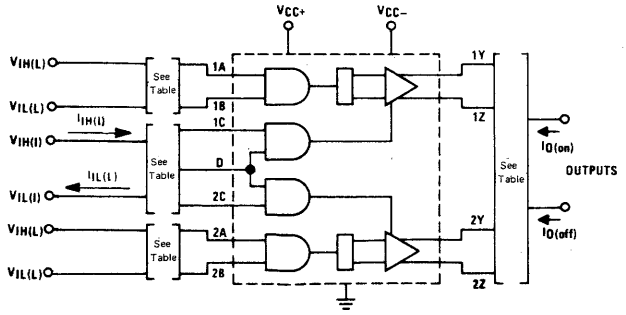


TEST TABLE

TEST AT ANY LOGIC INPUT	LOGIC INPUTS NOT UNDER TEST	ALL INHIBITOR INPUTS	OUTPUT 1Y or 2Y	OUTPUT 1Z or 2Z
$V_{IH(L)}$	Open	$V_{IH(I)}$	H (See Note 1)	L (See Note 1)
$V_{IL(L)}$	V_{CC+}	$V_{IH(I)}$	L (See Note 1)	H (See Note 1)
$I_{IH(L)}$	Gnd	$V_{IH(I)}$	Gnd	Gnd
$I_{IL(L)}$	4.5 V	$V_{IH(I)}$	Gnd	Gnd

NOTES: 1. Low output represents the on state, high output represents the off state.
2. Each input is tested separately.

FIGURE 16 – $V_{IH(L)}$, $V_{IL(L)}$, $I_{IH(L)}$, and $I_{IL(L)}$



TEST TABLE

TEST AT ANY INHIBITOR INPUT	ALL LOGIC INPUTS	INHIBITOR INPUTS NOT UNDER TEST	OUTPUT 1Y or 2Y	OUTPUT 1Z or 2Z
$V_{IH(I)}$	$V_{IH(L)}$	Open	H (See Note 1)	L (See Note 1)
	$V_{IL(L)}$	Open	L (See Note 1)	H (See Note 1)
$V_{IL(I)}$	$V_{IH(L)}$	V_{CC+}	H (See Note 1)	H (See Note 1)
	$V_{IL(L)}$	V_{CC+}	H (See Note 1)	H (See Note 1)
$I_{IH(I)}$	Gnd	Gnd	Gnd	Gnd
$I_{IL(I)}$	Gnd	4.5 V	Gnd	Gnd

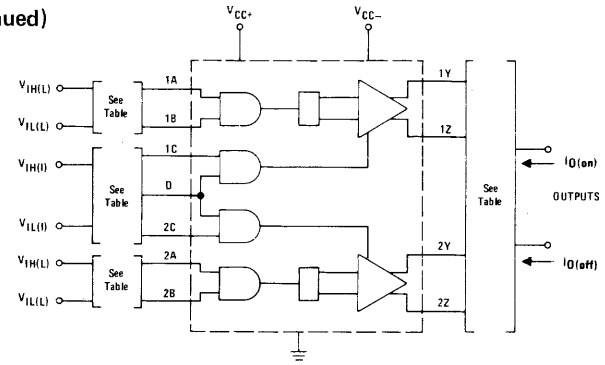
NOTES: 1. Low output represents the on state, high output represents the off state.
2. Each input is tested separately.

FIGURE 17 – $V_{IH(I)}$, $V_{IL(I)}$, $I_{IH(I)}$, $I_{IL(I)}$

† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

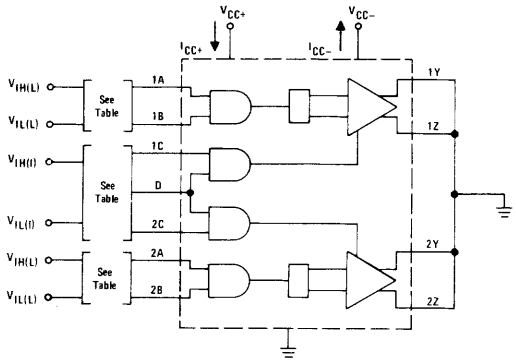


3

TEST TABLE

TEST		LOGIC INPUTS		INHIBITOR INPUTS	
		1A or 2A	1B or 2B	1C or 2C	D
$I_{O(on)}$	at output 1Y or 2Y	$V_{IL(L)}$	$V_{IL(L)}$	$V_{IH(I)}$	$V_{IH(I)}$
		$V_{IL(L)}$	$V_{IH(L)}$		
		$V_{IH(L)}$	$V_{IL(L)}$		
$I_{O(on)}$	at output 1Z or 2Z	$V_{IH(L)}$	$V_{IH(L)}$	$V_{IH(I)}$	$V_{IH(I)}$
$I_{O(off)}$	at output 1Y or 2Y	$V_{IH(L)}$	$V_{IH(L)}$	$V_{IH(I)}$	$V_{IH(I)}$
$I_{O(off)}$	at output 1Z or 2Z	$V_{IL(L)}$	$V_{IL(L)}$	$V_{IH(I)}$	$V_{IH(I)}$
		$V_{IL(L)}$	$V_{IH(L)}$		
		$V_{IH(L)}$	$V_{IL(L)}$		
$I_{O(off)}$	at output 1Y, 2Y, 1Z, or 2Z	Either state	Either state	$V_{IL(I)}$	$V_{IL(I)}$
				$V_{IL(I)}$	$V_{IH(I)}$
				$V_{IH(I)}$	$V_{IL(I)}$

FIGURE 18 – $I_{O(on)}$ and $I_{O(off)}$



TEST TABLE

TEST		ALL LOGIC INPUTS	ALL INHIBITOR INPUTS
$I_{CC+(on)}$	Driver enabled	$V_{IL(L)}$	$V_{IH(I)}$
$I_{CC-(on)}$	Driver enabled	$V_{IL(L)}$	$V_{IH(I)}$
$I_{CC+(off)}$	Driver inhibited	$V_{IL(L)}$	$V_{IL(I)}$
$I_{CC-(off)}$	Driver inhibited	$V_{IL(L)}$	$V_{IL(I)}$

FIGURE 19 – I_{CC+} and I_{CC-}

† Arrows indicate actual direction of current flow.

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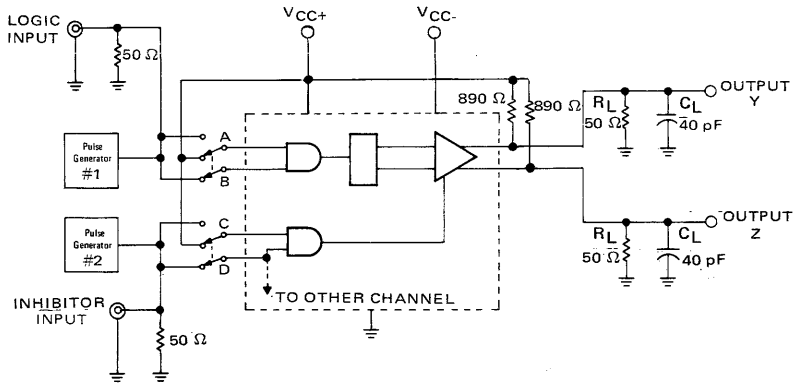
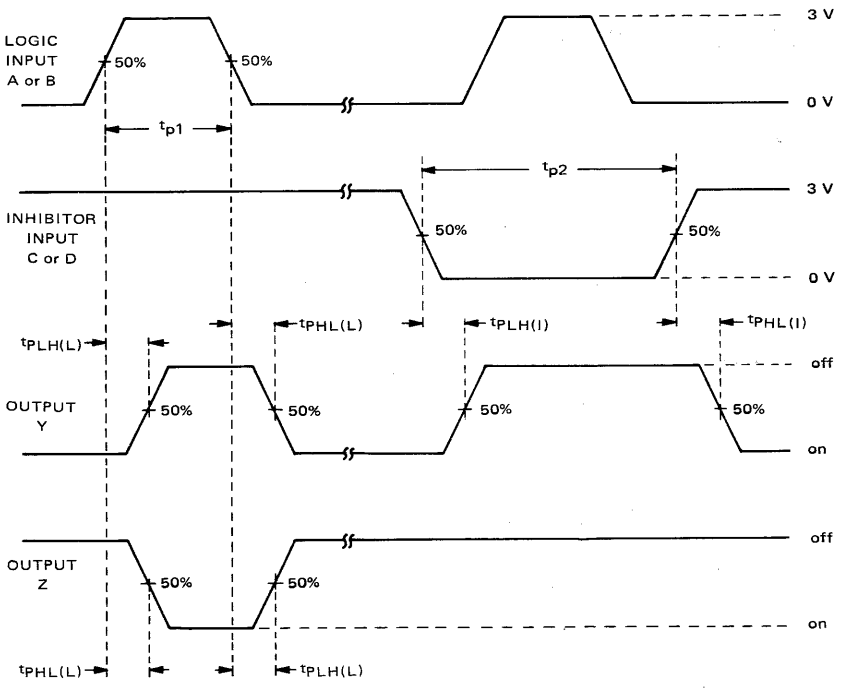
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f = 10 \pm 5$ ns, t_{p1} = 500 ns, PRR = 1 MHz, t_{p2} = 1 ms, PRR = 500 kHz.
2. C_L includes probe and jig capacitance.
3. For simplicity, only one channel and the inhibitor connections are shown.

FIGURE 20–PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS

SN55109, SN75109
OUTPUT CURRENT
vs
LOGIC INPUT VOLTAGE

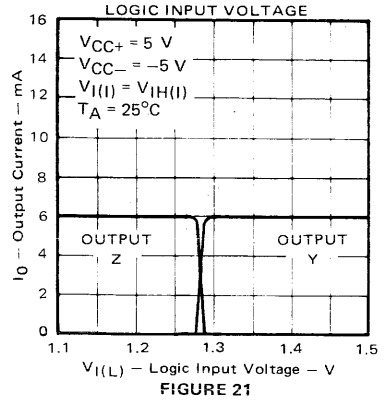


FIGURE 21

SN55110, SN75110
OUTPUT CURRENT
vs
LOGIC INPUT VOLTAGE

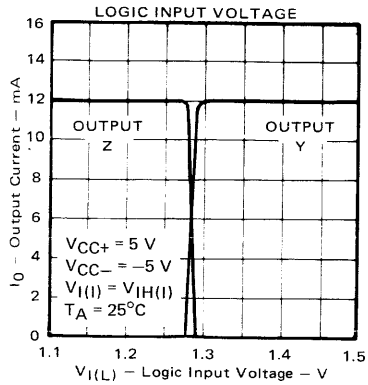


FIGURE 22

SN55109, SN75109
SUPPLY CURRENT WITH DRIVER ENABLED
vs
FREE-AIR TEMPERATURE

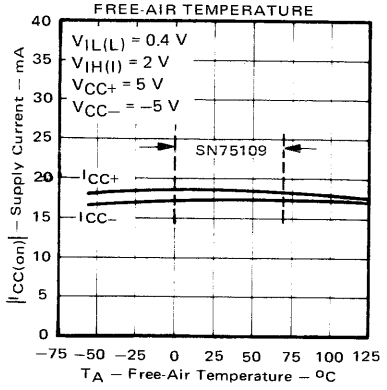


FIGURE 23

SN55110, SN75110
SUPPLY CURRENT WITH DRIVER ENABLED
vs
FREE-AIR TEMPERATURE

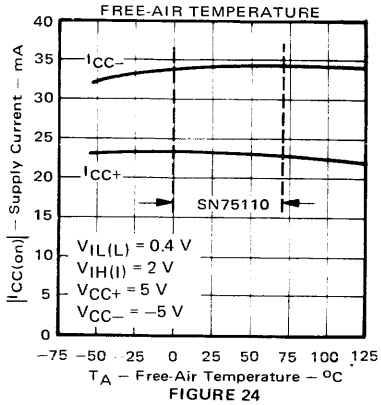


FIGURE 24

PROPAGATION DELAY TIME
(LOGIC INPUTS)
vs
FREE-AIR TEMPERATURE

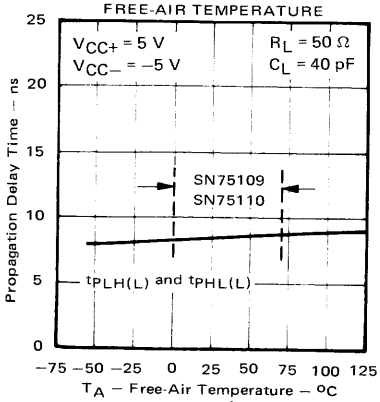


FIGURE 25

PROPAGATION DELAY TIME
(INHIBITOR INPUTS)
vs
FREE-AIR TEMPERATURE

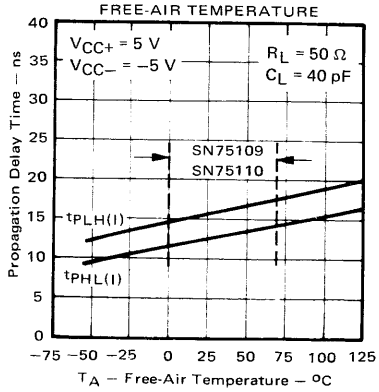


FIGURE 26

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TYPICAL APPLICATION DATA

BASIC BALANCED-LINE TRANSMISSION SYSTEM

Series 55/75107A dual line circuits are designed specifically for use in high-speed data transmission systems that utilize balanced, terminated transmission lines such as twisted-pair lines. The system operates in the balanced mode, so that noise induced on one line is also induced on the other. The noise appears common-mode at the receiver input terminals where it is rejected. The ground connection between the line driver and receiver is not part of the signal circuit so that system performance is not affected by circulating ground currents.

The unique driver-output circuit allows terminated transmission lines to be driven at normal line impedances. High-speed system operation is ensured since line reflections are virtually eliminated when terminated lines are used. Cross-talk is minimized by low signal amplitudes and low line impedances.

The typical data delay in a system is approximately (30 + 1.3 L) nanoseconds, where L is the distance in feet separating the driver and receiver. This delay includes one gate delay in both the driver and receiver.

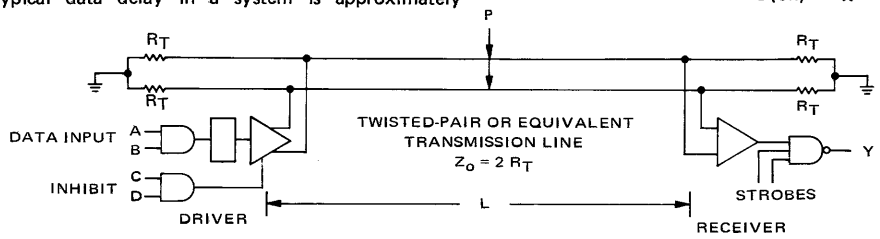
Data is impressed on the balanced-line system by unbalancing the line voltages with the driver output current. The driven line is selected by appropriate driver-input logic levels. The voltage difference is approximately:

$$V_{DIFF} \simeq 1/2\ I_{O(on)} \cdot R_T.$$

High series line resistance will cause degradation of the signal. The receivers, however, will detect signals as low as 25 mV (or less). For normal line resistances, data may be recovered from lines of several thousand feet in length.

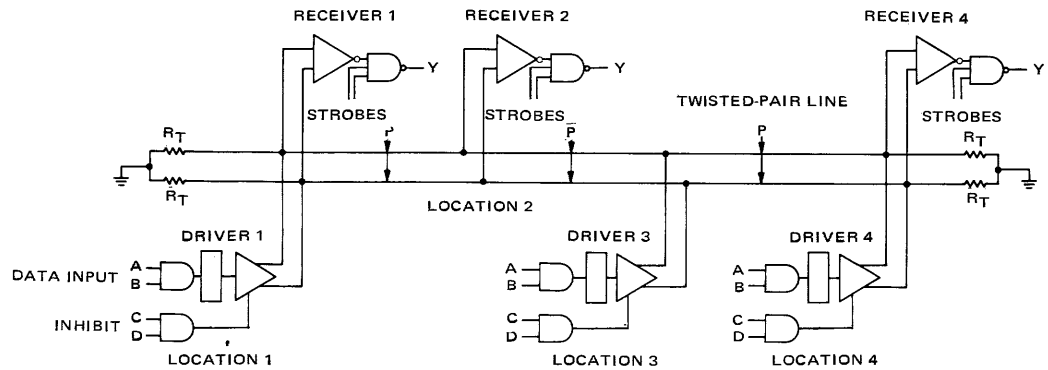
Line-termination resistors (R_T) are required only at the extreme ends of the line. For short lines, termination resistors at the receiver only may prove adequate. The signal amplitude will then be approximately:

$$V_{DIFF} \simeq I_{O(on)} \cdot R_T.$$



DATA-BUS OR PARTY-LINE SYSTEM

The strobe feature of the receivers and the inhibit feature of the drivers allow the Series 55/75107A dual line circuits to be used in data-bus or party-line systems. In these applications, several drivers and receivers may share a common transmission line. An enabled driver transmits data to all enabled receivers on the line while other drivers and receivers are disabled. Data is thus time-multiplexed on the transmission line. Series 55/75107A device specifications allow widely varying thermal and electrical environments at the various driver and receiver locations. The data-bus system offers maximum performance at minimum cost.



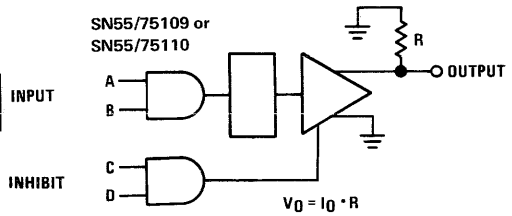
TYPICAL APPLICATION DATA

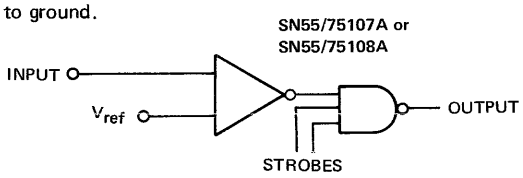
UNBALANCED OR SINGLE-LINE SYSTEMS

Series 55/75107A dual line circuits may also be used in unbalanced or single-line systems. Although these systems do not offer the same performance as balanced systems for long lines, they are adequate for very short lines where environmental noise is not severe.

The receiver threshold level is established by applying a d-c reference voltage to one receiver input terminal. The signal from the transmission line is applied to the remaining input. The reference voltage should be optimized so that signal swing is symmetrical about it for maximum noise margin. The reference voltage should be in the range of −3 volts to +3 volts. It can be provided by a voltage supply or by a voltage divider from an available supply voltage.

A single-ended output from a driver may be used in single-line systems. Coaxial or shielded line is preferred for minimum noise and cross-talk problems. For large signal swings, the high output current (12 mA) of the SN55/75110 is recommended. Drivers may be parallelled for higher current. The unused driver output must be tied to ground.





PRECAUTIONS IN THE USE OF SERIES 55/75107A LINE CIRCUITS

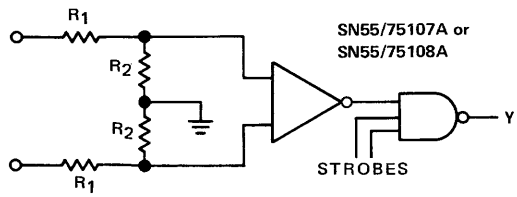
The following precautions should be observed when using or testing Series 55/75107A line circuits:

(1) Drivers, SN55/75109 and SN55/75110
When only one driver in a package is being used, the outputs of the other driver must either be grounded or inhibited in order to prevent excess power dissipation.

(2) Receivers, SN55/75107A and SN55/75108A
When only one receiver in a package is being used, at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3 volts and +3 volts, preferably at ground. Failure to do so will cause improper operation of the unit being used because of common bias circuitry for the current sources of the two receivers.

INCREASING COMMON-MODE INPUT VOLTAGE RANGE OF RECEIVER

The SN55/75107A and SN55/75108A line receivers feature a common-mode input voltage range of ±3 volts. This satisfies the requirements for all but the noisiest system applications. For these severe noise environments, the common-mode range can be extended by the use of external input attenuators. Common-mode input voltages can in this way be reduced to ±3 volts at the receiver input terminals. Differential data signals will be reduced proportionately. Input sensitivity, input impedance, and delay times will be adversely affected.

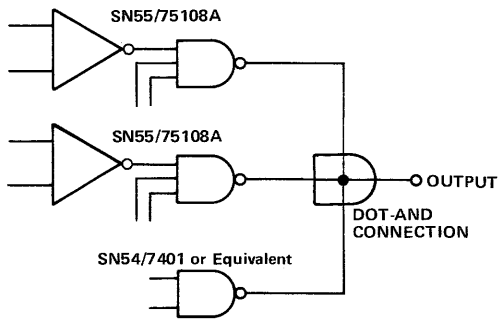


For balanced, terminated lines,
$Z_o = 2R_1 + 2R_2$

SN55/75108A DOT-AND OUTPUT CONNECTIONS

The SN55/75108A line receivers feature an open-collector-output circuit that can be connected in the DOT-AND logic configuration with other SN55/75108A outputs, SN5401/7401 outputs, or other similar outputs. This allows a level of logic to be implemented without additional logic delay.

For rules for such DOT-AND connections, refer to the SN5401 or SN7401 data sheet.



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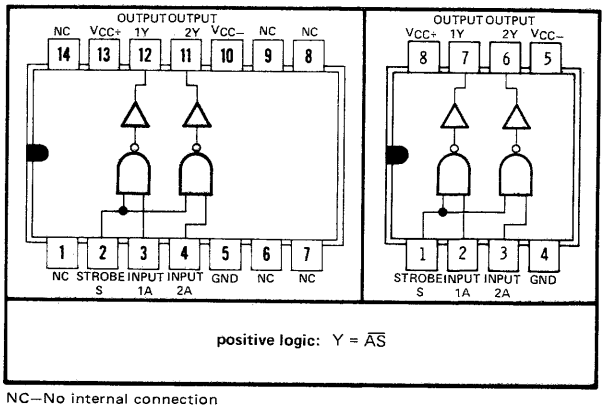
CIRCUIT TYPE SN75150
DUAL LINE DRIVER

SATISFIES REQUIREMENTS OF EIA STANDARD RS-232-C

- Withstands Sustained Output Short-Circuit to any Low-Impedance Voltage between −25 V and 25 V
- 2 μs Max Transition Time through the +3 V to −3 V Transition Region under Full 2500-pF Load
- Inputs Compatible with Most TTL and DTL Families
- Common Strobe Input
- Inverting Output
- Slew Rate can be Controlled with an External Capacitor at the Output
- Standard Supply Voltages . . . ±12 V

J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)

P
DUAL-IN-LINE PACKAGE
(TOP VIEW)

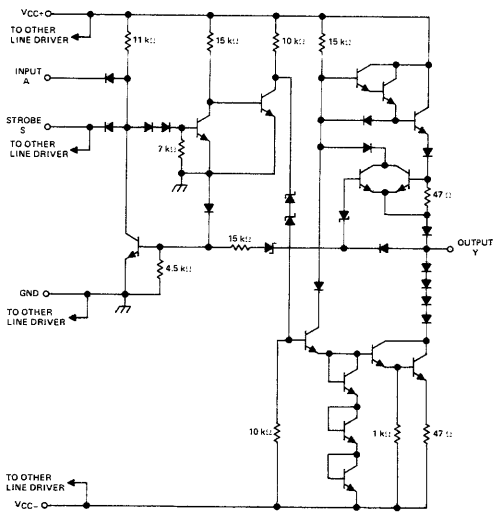


NC—No internal connection

description

The SN75150 is a monolithic dual line driver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232-C. A rate of 20,000 bits per second can be transmitted with a full 2500-pF load. Other applications are in data-transmission systems using relatively short single lines, in level translators, and for driving MOS devices. The logic input is compatible with most TTL and DTL families. Operation is from +12-volt and −12-volt power supplies. The SN75150 is characterized for operation from 0°C to 70°C.

schematic (each line driver)



Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	15 V
Supply voltage V_{CC-} (see Note 1)	−15 V
Input voltage (see Note 1)	15 V
Applied output voltage (see Note 1)	±25 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

CIRCUIT TYPE SN75150
DUAL LINE DRIVER

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage V_{CC+}	10.8	12	13.2	V
Supply voltage V_{CC-}	−10.8	−12	−13.2	V
Input voltage, V_I	0		5.5	V
Applied output voltage, V_O			±15	V
Operating free-air temperature, T_A	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP†	MAX (SEE NOTE 2)	UNIT
V_{IH}	High-level input voltage	1			2			V
V_{IL}	Low-level input voltage	2					0.8	V
V_{OH}	High-level output voltage	2	V_{CC+} = 10.8 V, V_{CC-} = −13.2 V, V_{IL} = 0.8 V, R_L = 3 kΩ to 7 kΩ		5	8		V
V_{OL}	Low-level output voltage	1	V_{CC+} = 10.8 V, V_{CC-} = −10.8 V, V_{IH} = 2 V, R_L = 3 kΩ to 7 kΩ			−8	−5	V
I_{IH}	High-level input current	3	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V, V_I = 2.4 V	Data input		1	10	μA
				Strobe input		2	20	
I_{IL}	Low-level input current	3	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V, V_I = 0.4 V	Data input		−1	−1.6	mA
				Strobe input		−2	−3.2	
I_{OS}	Short-circuit output current	4	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V	V_O = 25 V		2		mA
				V_O = −25 V		−3		
				V_O = 0 V, V_I = 3 V		15		
				V_O = 0 V, V_I = 0 V		−15		
I_{CCH+}	Supply current from V_{CC+}, high-level output	5	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V, V_I = 0 V, R_L = 3 kΩ, T_A = 25°C			10	22	mA
I_{CCH-}	Supply current from V_{CC-}, high-level output					−1	−10	mA
I_{CCL+}	Supply current from V_{CC+}, low-level output	5	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V, V_I = 3 V, R_L = 3 kΩ, T_A = 25°C			8	17	mA
I_{CCL-}	Supply current from V_{CC-}, low-level output					−9	−20	mA

NOTE 2: The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when −5 V is the maximum, the typical value is a more-negative voltage.

† All typical values are at V_{CC+} = 12 V, V_{CC-} = −12 V, T_A = 25°C.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −12 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{TLH}	Transition time, low-to-high-level output	6	C_L = 2500 pF, R_L = 3 kΩ to 7 kΩ	0.2	1.4	2	μs
t_{THL}	Transition time, high-to-low-level output			0.2	1.5	2	μs
t_{TLH}	Transition time, low-to-high-level output	6	C_L = 15 pF, R_L = 7 kΩ		40		ns
t_{THL}	Transition time, high-to-low-level output				20		ns
t_{PLH}	Propagation delay time, low-to-high-level output	6	C_L = 15 pF, R_L = 7 kΩ		60		ns
t_{PHL}	Propagation delay time, high-to-low-level output				45		ns

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PARAMETER MEASUREMENT INFORMATION

d-c test circuits‡

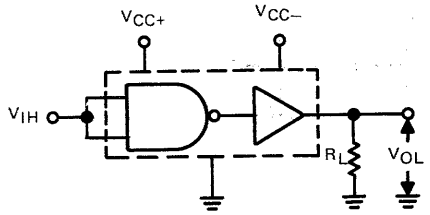
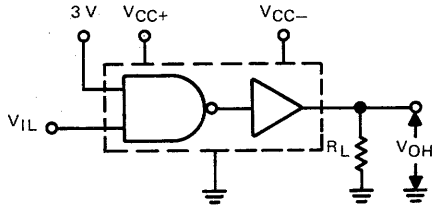
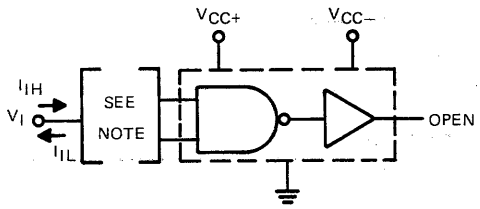


FIGURE 1–V_{IH}, V_{OL}



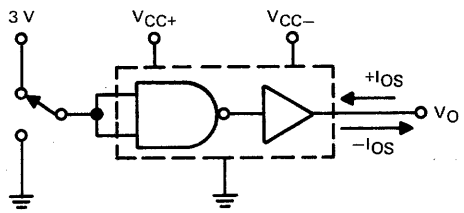
Each input is tested separately.

FIGURE 2–V_{IL}, V_{OH}



NOTE: When testing I_{IH}, the other input is at 3 V; when testing I_{IL}, the other input is open.

FIGURE 3–I_{IH}, I_{IL}



I_{OS} is tested for both input conditions at each of the specified output conditions.

FIGURE 4–I_{OS}

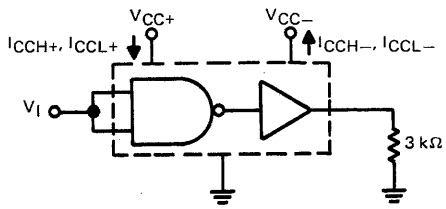
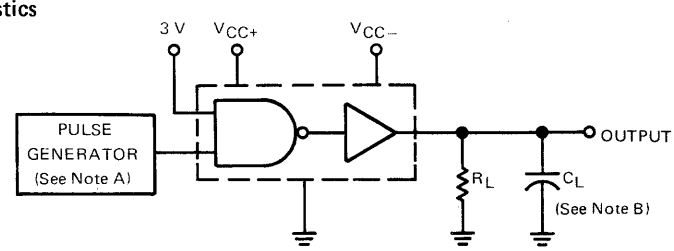


FIGURE 5–I_{CCH+}, I_{CCH-}, I_{CCL+}, I_{CCL-}

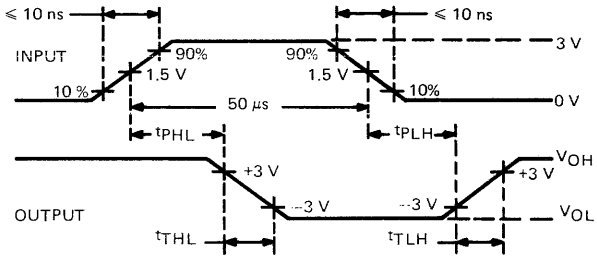
‡Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 6–SWITCHING CHARACTERISTICS

TYPICAL CHARACTERISTICS

OUTPUT CURRENT
vs
APPLIED OUTPUT VOLTAGE

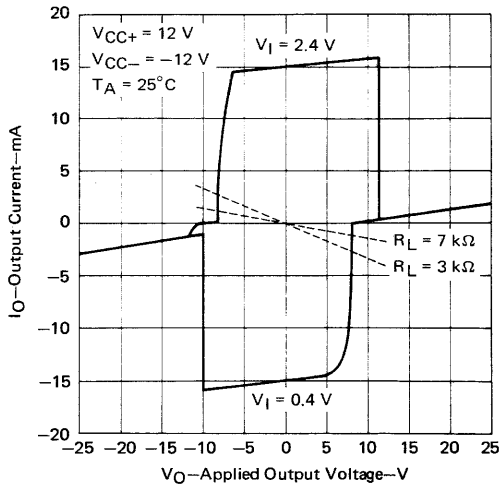


FIGURE 7

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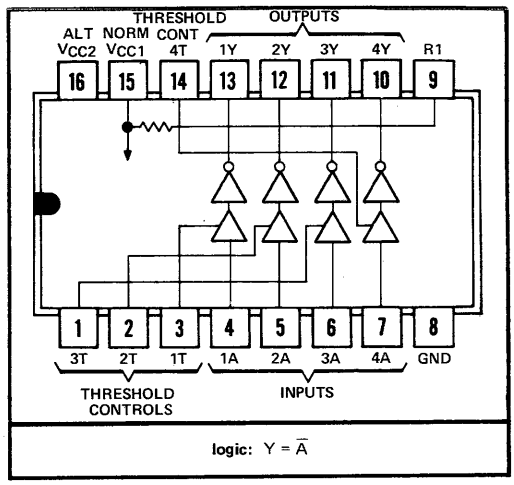
CIRCUIT TYPE SN75154
QUADRUPLE LINE RECEIVER

SATISFIES REQUIREMENTS OF EIA STANDARD RS-232-C

- Input Resistance . . . 3 kΩ to 7 kΩ over Full RS-232-C Voltage Range
- Input Threshold Adjustable to Meet "Fail-Safe" Requirements Without Using External Components
- Built-In Hysteresis for Increased Noise Immunity
- Inverting Output Compatible with DTL or TTL
- Output with Active Pull-Up for Symmetrical Switching Speeds
- Standard Supply Voltages . . . 5 V or 12 V

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The SN75154 is a monolithic quadruple line receiver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232C. Other applications are for relatively short, single-line, point-to-point data transmission and for level translators. Operation is normally from a single five-volt supply; however, a built-in option allows operation from a 12-volt supply without the use of additional components. The output is compatible with most TTL and DTL circuits when either supply voltage is used.

In normal operation, the threshold-control terminals are connected to the V_{CC1} terminal, pin 15, even if power is being supplied via the alternate V_{CC2} terminal, pin 16. This provides a wide hysteresis loop which is the difference between the positive-going and negative-going threshold voltages. See typical characteristics. In this mode of operation, if the input voltage goes to zero, the output voltage will remain at the low or high level as determined by the previous input.

For fail-safe operation, the threshold-control terminals are open. This reduces the hysteresis loop by causing the negative-going threshold voltage to be above zero. The positive-going threshold voltage remains above zero as it is unaffected by the disposition of the threshold terminals. In the fail-safe mode, if the input voltage goes to zero or an open-circuit condition, the output will go to the high level regardless of the previous input condition.

The SN75154 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Normal supply voltage (pin 15), V_{CC1} (see Note 1)	7 V
Alternate supply voltage (pin 16), V_{CC2} (see Note 1)	14 V
Input voltage (see Note 1)	±25 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Normal supply voltage (pin 15), V_{CC1}	4.5	5	5.5	V
Alternate supply voltage (pin 16), V_{CC2}	10.8	12	13.2	V
Input voltage			±15	V
Normalized fan-out from each output, N			10	
Operating free-air temperature, T_A	0	25	70	°C

CIRCUIT TYPE SN75154
QUADRUPLE LINE RECEIVER

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX (SEE NOTE 2)	UNIT
V_{IH}	High-level input voltage		1		3			V
V_{IL}	Low-level input voltage		1				−3	V
V_{T+}	Positive-going threshold voltage	Normal operation	1		0.8	2.2	3	V
		Fail-safe operation			0.8	2.2	3	
V_{T-}	Negative-going threshold voltage	Normal operation	1		−3	−1.1	0	V
		Fail-safe operation			0.8	1.4	3	
$V_{T+}-V_{T-}$	Hysteresis	Normal operation	1		0.8	3.3	6	V
		Fail-safe operation			0	0.8	2.2	
V_{OH}	High-level output voltage		1	I_{OH} = −400 μA	2.4	3.5		V
V_{OL}	Low-level output voltage		1	I_{OL} = 16 mA		0.23	0.4	V
r_I	Input resistance		2	ΔV_I = −25 V to −14 V	3	5	7	kΩ
				ΔV_I = −14 V to −3 V	3	5	7	
				ΔV_I = −3 V to 3 V	3	6		
				ΔV_I = 3 V to 14 V	3	5	7	
				ΔV_I = 14 V to 25 V	3	5	7	
$V_{I(open)}$	Open-circuit input voltage		3	I_I = 0	0	0.2	2	V
I_{OS}	Short-circuit output current†		4	V_{CC1} = 5.5 V, V_I = −5 V	−10	−20	−40	mA
I_{CC1}	Supply current from V_{CC1}		5	V_{CC1} = 5.5 V, T_A = 25°C		20	35	mA
I_{CC2}	Supply current from V_{CC2}			V_{CC2} = 13.2 V, T_A = 25°C		23	40	

†Not more than one output should be shorted at a time.

‡ All typical values are at V_{CC1} = 5 V, T_A = 25°C.

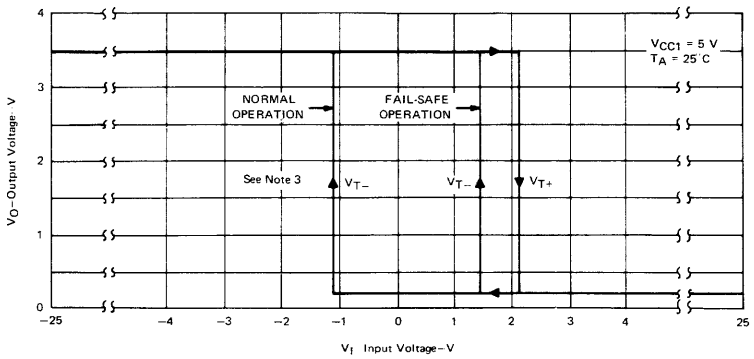
NOTE 2: The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic and threshold levels only, e.g., when −3 V is the maximum, the minimum limit is a more-negative voltage.

switching characteristics, V_{CC1} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	6	C_L = 50 pF, R_L = 390 Ω		22		ns
t_{PHL}	Propagation delay time, high-to-low-level output				20		ns
t_{TLH}	Transition time, low-to-high-level output				9		ns
t_{THL}	Transition time, high-to-low-level output				6		ns

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs INPUT VOLTAGE



NOTE 3: For normal operation, the threshold controls are connected to V_{CC1}, pin 15. For fail-safe operation, the threshold controls are open.

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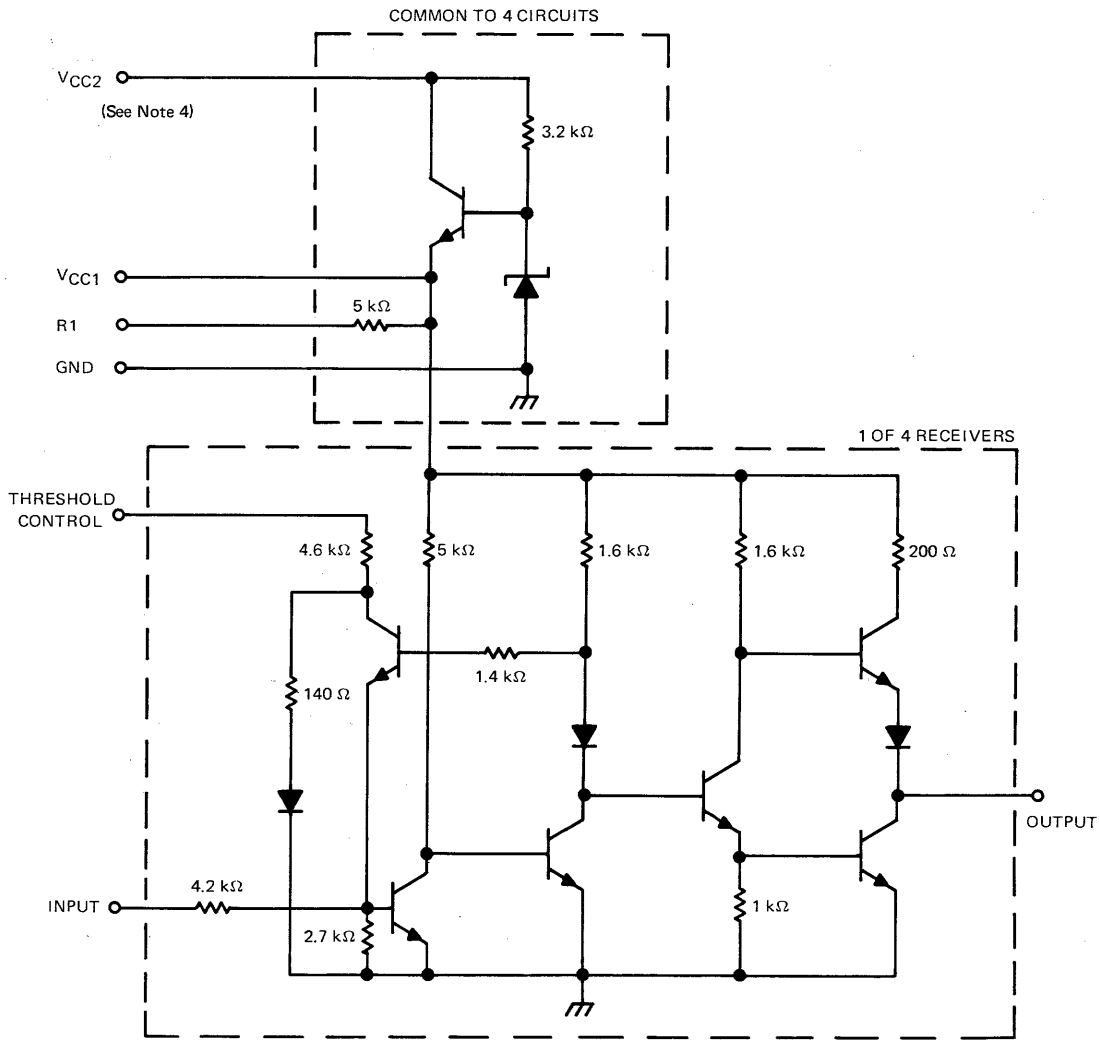
schematic



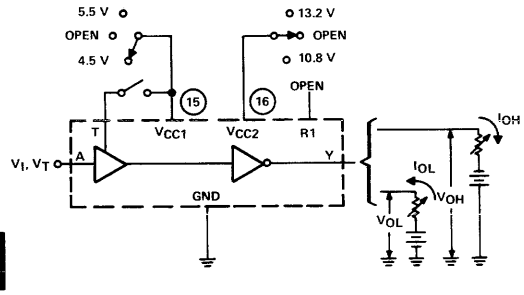
Component values shown are nominal

⏚ . . . Substrate

NOTE 4: When using V_{CC1} (pin 15), V_{CC2} (pin 16) may be left open or shorted to V_{CC1}. When using V_{CC2}, V_{CC1} must be left open or connected to the threshold control pins.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

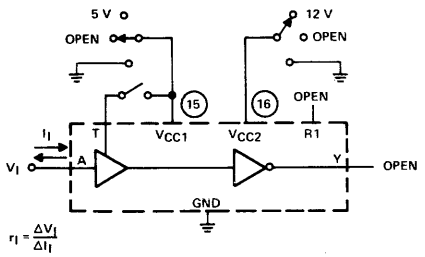


NOTES: A. Momentarily apply −5 V, then 0.8 V.
B. Momentarily apply 5 V, then ground.

TEST TABLE

TEST	MEASURE	A	T	Y	V_{CC1} (PIN 15)	V_{CC2} (PIN 16)
Open-circuit input (fail safe)	V_{OH}	Open	Open	I_{OH}	4.5 V	Open
	V_{OH}	Open	Open	I_{OH}	Open	10.8 V
V_{T+} min, V_{T-} min (fail safe)	V_{OH}	0.8 V	Open	I_{OH}	5.5 V	Open
	V_{OH}	0.8 V	Open	I_{OH}	Open	13.2 V
V_{T+} min (normal)	V_{OH}	Note A	Pin 15	I_{OH}	5.5 V and T	Open
	V_{OH}	Note A	Pin 15	I_{OH}	T	13.2 V
V_{IL} max, V_{T-} min (normal)	V_{OH}	−3 V	Pin 15	I_{OH}	5.5 V and T	Open
	V_{OH}	−3 V	Pin 15	I_{OH}	T	13.2 V
V_{IH} min, V_{T+} max, V_{T-} max (fail safe)	V_{OL}	3 V	Open	I_{OL}	4.5 V	Open
	V_{OL}	3 V	Open	I_{OL}	Open	10.8 V
V_{IH} min, V_{T+} max (normal)	V_{OL}	3 V	Pin 15	I_{OL}	4.5 V and T	Open
	V_{OL}	3 V	Pin 15	I_{OL}	T	10.8 V
V_{T-} max (normal)	V_{OL}	Note B	Pin 15	I_{OL}	5.5 V and T	Open
	V_{OL}	Note B	Pin 15	I_{OL}	T	13.2 V

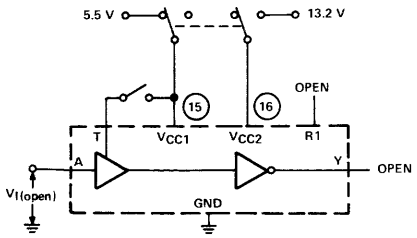
FIGURE 1 – V_{IH}, V_{IL}, V_{T+}, V_{T-}, V_{OH}, V_{OL}



TEST TABLE

T	V_{CC1} (PIN 15)	V_{CC2} (PIN 16)
Open	5 V	Open
Open	GND	Open
Open	Open	Open
Pin 15	T and 5 V	Open
GND	GND	Open
Open	Open	12 V
Open	Open	GND
Pin 15	T	12 V
Pin 15	T	GND
Pin 15	T	Open

FIGURE 2–r_I



TEST TABLE

T	V_{CC1} (PIN 15)	V_{CC2} (PIN 16)
Open	5.5 V	Open
Pin 15	5.5 V	Open
Open	Open	13.2 V
Pin 15	T	13.2 V

FIGURE 3–$V_{I(open)}$

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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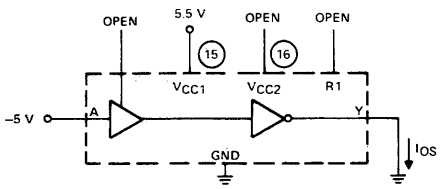
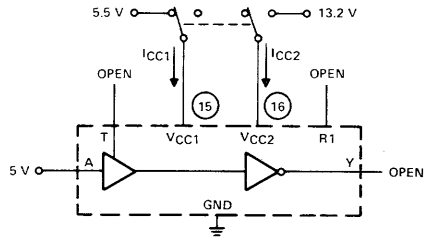
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



Each output is tested separately.

FIGURE 4–I_{OS}



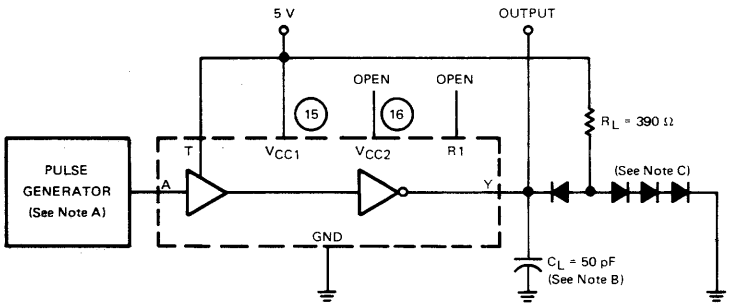
All four line receivers are tested simultaneously.

FIGURE 5–I_{CC}

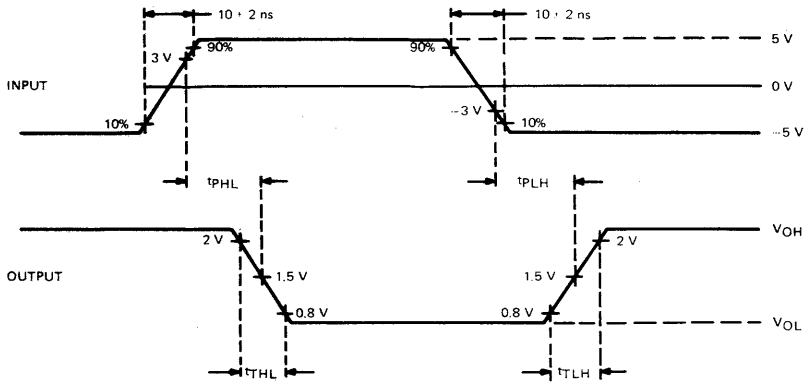
†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

3

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, t_w = 200 ns, duty cycle ≤ 20%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 6–SWITCHING TIMES

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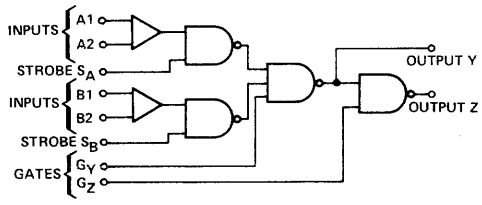
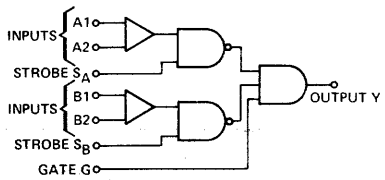
SENSE AMPLIFIER SELECTION GUIDE

TYPE	SN7520, SN7521	SN7522, SN7523	SN7524, SN7525 SN75234, SN75235†	SN7526, SN7527	SN7528, SN7529 SN75238, SN75239†
Features	• Provide Memory Data Register • Complementary Outputs	• Open-Collector Output Stage • High Fan-Out	• Dual Sense Channels • Independent Strobes	• Complete Memory Data Function • Effective Strobe Width of Less than 10 ns	• Test Points for Strobe Timing Adjustment • Dual Sense Channels
Packages	J, N	J, N	J, N	J, N	J, N
Applications	Large Memories	Large Memories	General Purpose Sense Amplifiers	High-Performance Sense Amplifiers	General Purpose Sense Amplifiers
Application Notes	CA-101: Operating and Use of Series 7520N Sense Amplifiers				

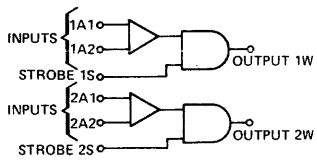
3 block diagrams



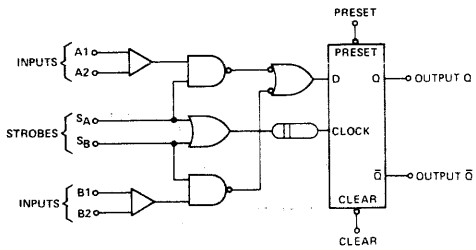
SN7520, SN7521



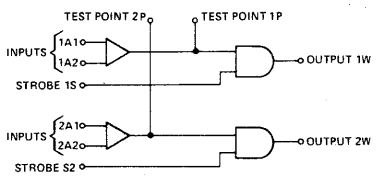
SN7522, SN7523



SN7524, SN7525
SN75234, SN75234†



SN7526, SN7527



SN7528, SN7529
SN75238, SN75239†

†Types SN75234, SN75235, SN75238, and SN75239 are indentical to types SN7524, SN7525, SN7528, and SN7529, respectively, except that an additional stage has been added to the output gate to provide an inverted output.

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HIGH-SPEED SENSE AMPLIFIERS FOR CONVERSION OF COINCIDENT-CURRENT MEMORY READOUT TO SATURATED DIGITAL-LOGIC LEVELS

performance features

- high speed and fast recovery time
- time and amplitude signal discrimination
- adjustable input threshold voltage levels
- narrow region of threshold voltage uncertainty
- multiple differential-input preamplifiers
- high d-c noise margin—typically one volt
- good fan-out capability

ease-of-design features

- choice of output circuit function
- TTL or DTL drive capability
- standard logic supply voltages
- plug-in configuration ideal for flow-soldering techniques
- pins on 100-mil grid spacings for industrial-type circuit boards

3

description

Series 7520 monolithic sense amplifiers are designed for use with high-speed memory systems. These sense amplifiers detect bipolar differential-input signals from the memory and provide the interface circuitry between the memory and the logic section. Low-level pulses originating in the memory are transformed into logic levels compatible with standard transistor-transistor-logic (TTL) and diode-transistor-logic (DTL) circuits.

These sense amplifiers feature multiple, differential-input preamplifiers and versatile gating and output circuits, permitting a significant reduction in the circuitry required to accomplish the sensing function. A unique circuit design provides inherent stability of the input threshold level over a wide range of power-supply voltage levels and temperature ranges. Independent strobing of each of the dual sense-input channels ensures maximum versatility and permits detection to occur when the signal-to-noise ratio is at a maximum. The gate and strobe inputs and the outputs are compatible with standard TTL and DTL digital logic circuits.

The SN7520 and SN7521 circuits may be used to perform the functions of a flip-flop or register which responds to the sense and strobe input conditions.

The SN7522 and SN7523 circuits feature a high-fan-out, single-ended, open-collector output stage. In addition, they may be used to expand the inputs to an SN7520 or SN7521 circuit, or to perform the wired-AND function.

The SN7524 and SN7525 circuits provide for independent, dual-channel sensing with separate outputs.

The SN7526 and SN7527 circuits have a D-type flip-flop output with external clear and preset inputs.

The SN7528 and SN7529 circuits are similar to the SN7524 and SN7525 except that the output of each preamplifier is available as a test point.

CONTENTS

	PAGE
DESIGN CHARACTERISTICS, CIRCUIT OPERATION, AND OTHER GENERAL INFORMATION	3-159
MAXIMUM RATINGS AND RECOMMENDED OPERATING CONDITIONS	3-163
DEFINITIVE SPECIFICATIONS:	
CIRCUIT TYPES SN7520, SN7521	3-164
CIRCUIT TYPES SN7522, SN7523	3-166
CIRCUIT TYPES SN7524, SN7525	3-170
CIRCUIT TYPES SN7526, SN7527	3-172
CIRCUIT TYPES SN7528, SN7529	3-174
CIRCUIT TYPES SN75234, SN75235	3-176
CIRCUIT TYPES SN75238, SN75239	3-178
D-C TEST CIRCUITS	3-180
SWITCHING TIME TEST CIRCUITS AND VOLTAGE WAVEFORMS	3-197
TYPICAL CHARACTERISTICS	3-207
TYPICAL APPLICATIONS	3-209

1

design characteristics

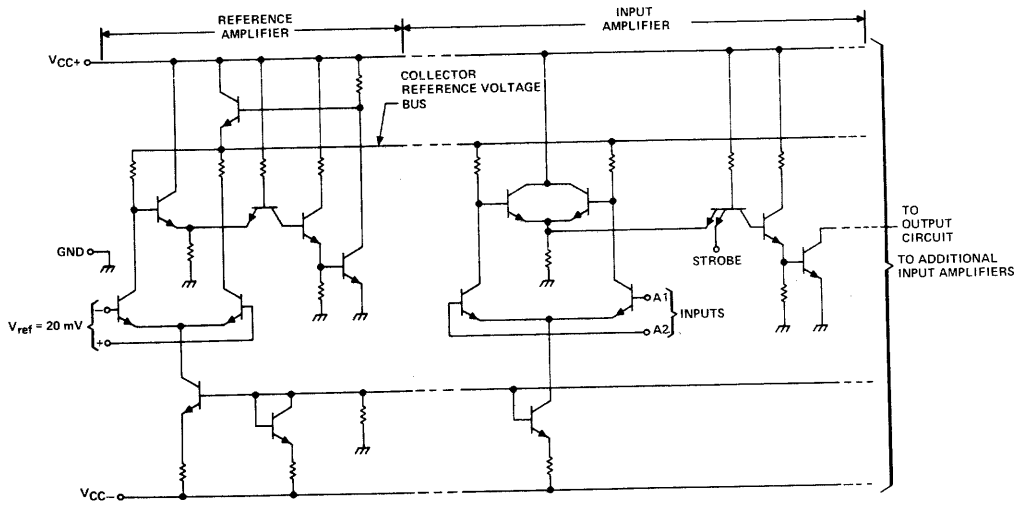
Series 7520 sense amplifiers are completely d-c coupled. Previous designs have resulted in circuits in which the threshold level could not be closely controlled because they were highly sensitive to changes in the d-c levels throughout the amplifier. This was due primarily to the required tolerances on the absolute value of resistors and the resistor temperature coefficients. The "matched-amplifier" design of Series 7520 circuits depends on resistor ratios rather than absolute values. In this design, excellent stability of the threshold level can be maintained despite component variations and changes in bias levels. The capability of multiple-input amplifiers increases the versatility of the design.

The basic circuit is used to implement several sense amplifier designs. Additional logic circuitry is added to the strobe-gate output to provide versatile sensing functions. The outputs of two or more input amplifiers can be combined to implement multiple-input amplifiers, a function not previously available in integrated form. The d-c coupled design eliminates many of the problems associated with overload recovery time and threshold shift (with high input repetition rates) usually encountered in sense amplifier designs that use reactive coupling components.

circuit operation

The basic Series 7520 sense amplifier strobe and threshold circuit is shown in Figure A. The design uses a "matched-amplifier" concept which takes advantage of the inherent excellent component matching and thermal tracking characteristics of monolithic integrated circuits. A reference amplifier is used to generate the collector reference voltage which is distributed to the input amplifiers. Application of an external reference voltage, V_{ref}, establishes the input-amplifier threshold voltage level, V_T. The design is such that there is 1:1 correspondence between the applied reference voltage, V_{ref}, and the nominal threshold voltage level, V_T. The reference and input amplifiers use identical circuit configurations; therefore, changes in bias levels introduced into the input amplifier, through changes in temperature or power-supply voltage levels, are compensated by similar changes in the reference amplifier.

The collector reference voltage, supplied by the reference amplifier, can be used to control the threshold-voltage level of more than one input amplifier, thereby establishing equal threshold levels to all of the input sense channels simultaneously.



Patent pending

FIGURE A—BASIC SERIES 7520 SENSE-AMPLIFIER CIRCUIT

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circuit operation (continued)

The second stage of the input amplifier is a TTL gate. The gate provides the threshold action for the input sense channel and provides a convenient point in the circuit to accomplish the strobe function. The differential-input sense signal switches the output of the TTL gate only when the strobe input voltage is higher than the logic input threshold voltage. The strobe input, therefore, provides the sense amplifier with the capability of time discrimination, allowing the input signal to be detected when the signal-to-noise ratio is at a maximum.

The logic inputs (i.e., gate and strobe) of Series 7520 sense amplifiers are designed to be compatible with Series 74 TTL digital integrated circuits. The multiple-emitter transistors are utilized to provide inherent switching-time advantages over other saturated-logic schemes. The same guaranteed noise margin and logic threshold voltage as for Series 74 are assured each of the gate and strobe inputs. This is accomplished by testing each logic input under standard Series 74 test conditions, i.e., 2 volts for high-level input condition and 0.8 volt for low-level input conditions. Since the guaranteed minimum high-level output voltage is 2.4 volts and the guaranteed maximum low-level output voltage is 0.4 volt, a minimum noise margin of 0.4 volt is assured at each input.

SN7520 and SN7521 circuit

This circuit is a dual-channel sense amplifier with the preamplifiers connected to a common output stage and a complementary output stage. The output circuit is composed of two cascaded NAND gates, each with external gate inputs. External connection of the Z output and the G_Y input results in a flip-flop

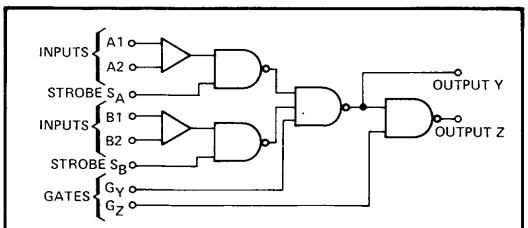

FIGURE B
SN7520/SN7521 LOGIC DIAGRAM

logic: $Y = \overline{G}_Y + A \cdot S_A + B \cdot S_B$
$Z = \overline{G}_Z + \overline{Y}$
$Z = \overline{G}_Z + G_Y (\overline{A} + \overline{S}_A)(\overline{B} + \overline{S}_B)$

SN7520 and SN7521 circuit (continued)

or register that is set by signals at the differential-input terminals. Reset of the register is performed at the G_Z input. Capacitive coupling from output Z to G_Y results in output pulse stretching. In either connection, complementary output levels are available. The gate and strobe inputs and the outputs are compatible with standard TTL logic. The input function of SN7520/SN7521 can be expanded by connecting the Y output of SN7522/SN7523 to the G_Y input of the circuit being expanded.

SN7522 and SN7523 circuit

This circuit is a dual-channel sense amplifier with the preamplifiers connected to a common output stage. The output circuit features an open-collector output which permits two or more of these outputs to be connected in the wire-AND configuration. Each package includes a load resistor that may be used as the output pull-up resistor. High sink-current capability is a feature of this design, and a separate ground terminal is used for the output circuitry. These devices can also be used as input expanders for the SN7520/SN7521 circuit.

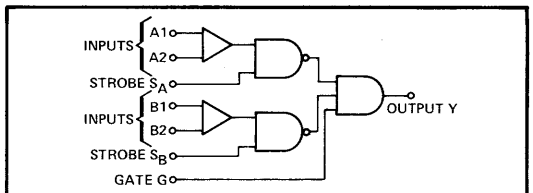

FIGURE C
SN7522/SN7523 LOGIC DIAGRAM

logic: $Y = G(\overline{A} + \overline{S}_A)(\overline{B} + \overline{S}_B)$

SN7524 and SN7525 circuit

This circuit features two completely independent sense amplifiers in a single package. Each channel features high fan-out capability.

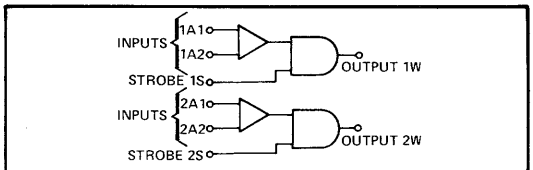

FIGURE D
SN7524/SN7525 LOGIC DIAGRAM
SN75234/SN75235 SAME EXCEPT INVERTED OUTPUT

logic: W = AS for SN7524 and SN7525
$W = \overline{AS}$ for SN75234 and SN75235

SN7526 and SN7527 circuit

This circuit is a dual-channel sense amplifier with the preamplifiers connected to a D-type flip-flop with external clear and preset inputs. A delay between the strobe input terminals and the clock input of the flip-flop ensures that data is set up at the D input of the flip-flop prior to clocking.

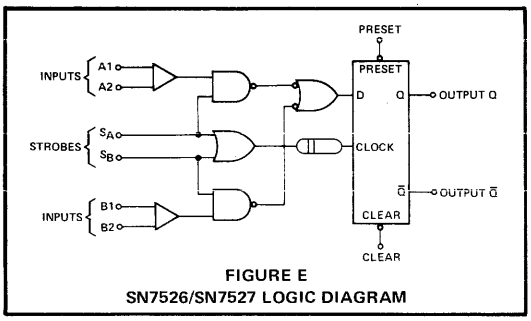

FIGURE E
SN7526/SN7527 LOGIC DIAGRAM

logic: See truth table on page 14.

SN7528 and SN7529 circuit

This circuit features two separate single-preamplifier sense amplifiers in a single package. The output of each preamplifier is available as a test point. These test points can be used to observe the amplified core signal to facilitate accurate strobe timing. When using this device, care should be taken to avoid coupling the strobe signal or other stray signals to the test point. Excessive loading of the test point is also to be avoided. The result of either coupling or loading will be a change in the threshold voltage of the device. The output circuit of each channel features a simple TTL gate configuration with a high fan-out capability.

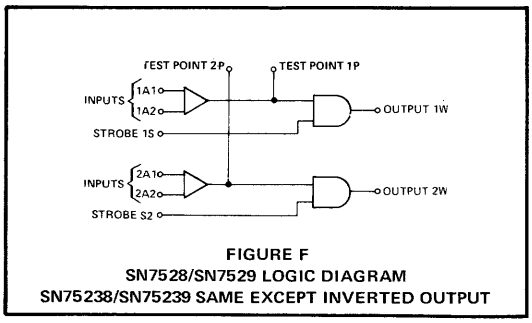

FIGURE F
SN7528/SN7529 LOGIC DIAGRAM
SN75238/SN75239 SAME EXCEPT INVERTED OUTPUT

logic: W = AS for SN7528 and SN7529
W = $\overline{AS}$ for SN75238 and SN75239

SN75234, SN75235, SN75238, SN75239 circuits

These dual sense amplifier circuits are the same as SN7524, SN7525, SN7528, and SN7529, respectively, except that an additional stage has been added to the output gate to provide an inverted output. Compared to using a separate gate for inversion, not only is package count reduced, but less propagation delay is added.

reference voltage considerations

These sense amplifiers feature a variable-threshold voltage level with simultaneous adjustment of both sense channels or both sense amplifiers by a single reference voltage. The operating threshold voltage level of the input amplifiers is established by and is approximately equal to the applied reference input voltage, V_{ref}. Several methods may be used to supply this reference voltage; however, methods given here will be limited to the discussion of fundamental design considerations. These sense amplifiers are recommended for use in systems requiring threshold voltage levels of ±15 to ±40 mV.

A simple method of generating the reference voltage is the use of a resistor voltage divider from either the positive (V_{CC+}) or negative (V_{CC-}) voltage supplies. See Figure G. This type of voltage divider may be used to supply an individual reference amplifier or to supply a number of paralleled reference amplifiers. The bias current required at the reference amplifier input is low (nominally 30 μA); therefore, voltage dividers of this type may normally be operated with very low current requirements. In noisy environments, the use of a filter capacitor across the inputs is recommended. By locating the capacitor as close to the device terminals as possible, noise and stray signals will be presented common-mode to the reference amplifier and thus be rejected.

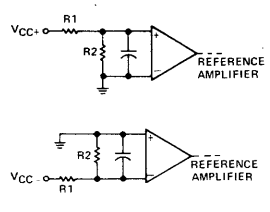

FIGURE G

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input line layout considerations

Input sensitivity and device speed require adequate precautions in the routing of signal input and reference lines to prevent noise pickup. Bypassing of supply and reference inputs at the device with low-inductance disc ceramic capacitors, and use of a good ground plane to separate strobe and output lines from sense and reference input lines, is recommended.

sense-input termination resistor considerations

Termination resistors are intentionally omitted from the sense-input terminals so the designer may select resistor values which will be compatible with the particular application. Matched termination resistors, (R_T, Figure H), normally in the range of 25 Ω to 200 Ω each, are required not only to terminate the sense line in a desired impedance but also to provide a d-c path for the sense-input bias currents. Careful matching of the resistor pairs should be observed or effective common-mode rejection will be reduced.

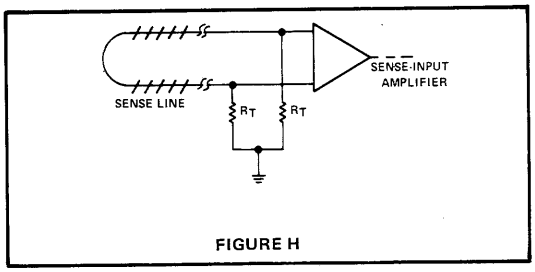

FIGURE H

3

output drive capability

The output circuits of these sense amplifiers feature the ability to sink or supply load current, This capability permits direct use with both TTL- and DTL-type loads. The open-collector output of the SN7522/SN7523 circuit may be connected to similar outputs to perform the wire-AND function. Load currents (out of the output terminal) are specified as negative values. Arrows on the d-c test circuit indicate the actual direction of current flow.

logic input current requirements

Logic input current requirements are specified at worst-case power-supply conditions over the operating free-air temperature range of 0°C to 70°C. The logic input currents are identical to and compatible with Series 74 TTL digital integrated circuits. Each logic input of the multiple-emitter input transistors requires no more than a 1.6-mA flow out of the input at a low logic level. Each input emitter requires current into the input when it is at a high-logic level. This current is 40 μA maximum. Currents into the input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

absolute maximum ratings (over free-air temperature range unless otherwise noted)

Supply voltages (see Note 1)	
V_{CC+}	7 V
V_{CC-}	−7 V
Differential input voltage, V_{ID} or V_{ref}	±5 V
Voltage from any input to ground (see Note 2)	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	−55°C to 150°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC+} (see Note 1)	4.75	5	5.25	V
V_{CC-} (see Note 1)	−4.75	−5	−5.25	V
V_{ref}	15		40	mV

NOTES: 1. These voltage values are with respect to network ground terminal.
2. Strobe and gate input voltages must be zero or positive with respect to network ground terminal.

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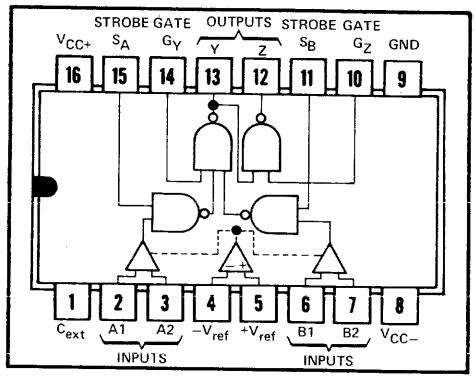
CIRCUIT TYPES SN7520,SN7521
DUAL-CHANNEL SENSE AMPLIFIERS WITH COMPLEMENTARY OUTPUTS

TRUTH TABLE

INPUTS						OUTPUTS	
A	B	G_Y	G_Z	S_A	S_B	Y	Z
X	X	L	X	X	X	H	$\overline{G}_Z$
H	X	X	X	H	X	H	$\overline{G}_Z$
X	H	X	X	X	H	H	$\overline{G}_Z$
L	L	H	X	X	X	L	H
L	X	H	X	X	L	L	H
X	L	H	X	L	X	L	H
X	X	H	X	L	L	L	H
X	X	X	L	X	X	X	H

J OR N

DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{G}_Y + A \cdot S_A + B \cdot S_B$

$Z = \overline{G}_Z + \overline{Y}$

$Z = \overline{G}_Z + G_Y(\overline{A} + \overline{S}_A)(\overline{B} + \overline{S}_B)$

3

definition of logic levels

INPUT	H	L	X
A or B†	$V_{ID} \geq V_T$ max	$V_{ID} \leq V_T$ min	Irrelevant
Any G or S	$V_I \geq V_{IH}$ min	$V_I \leq V_{IL}$ max	Irrelevant

†A and B are differential voltages (V_{ID}) between A1 and A2 or B1 and B2, respectively. For these circuits, V_{ID} is considered positive regardless of which terminal of each pair is positive with respect to the other.

electrical characteristics (unless otherwise noted V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_T	Differential input threshold voltage (see Note 3, page 17)	1	V_{ref} = 15 mV	SN7520	11	15	19	mV
				SN7521	8	15	22	
			V_{ref} = 40 mV	SN7520	36	40	44	
				SN7521	33	40	47	
V_{ICF}	Common-mode input firing voltage (see Note 4, page 17)	none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-mode input pulse:* $t_r \leq 15$ ns, $t_f \leq 15$ ns, t_w = 50 ns			±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			30	75	μA
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			0.5		μA
V_{IH}	High-level input voltage (strobe and gate inputs)	3			2			V
V_{IL}	Low-level input voltage (strobe and gate inputs)	3					0.8	V
V_{OH}	High-level output voltage	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OH} = −400 μA		2.4	4		V
V_{OL}	Low-level output voltage	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA			0.25	0.4	V
I_{IH}	High-level input current (strobe and gate inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V				40	μA
			V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V				1	mA
I_{IL}	Low-level input current (strobe and gate inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V			−1	−1.6	mA
$I_{OS(Y)}$	Short-circuit output current into Y	5	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V		−3		−5	mA
$I_{OS(Z)}$	Short-circuit output current into Z	5	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V		−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			28	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			−14	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

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switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geqslant$ 100 pF, T_A = 25°C

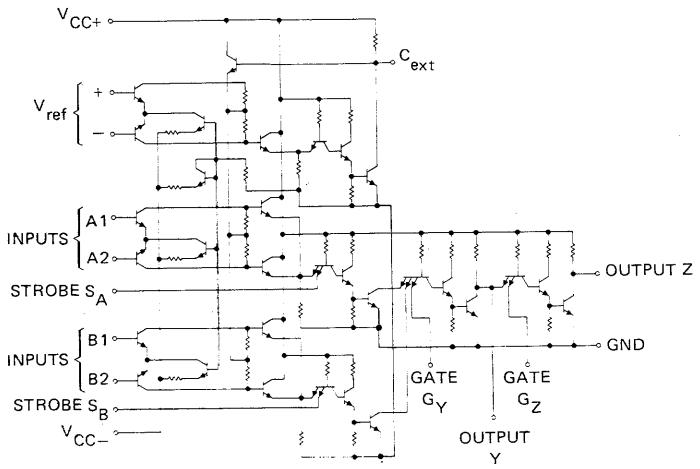
PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(DY)}$	A1-A2 OR B1-B2	Y	32	C_L = 15 pF, R_L = 288 Ω		25	40	ns
$t_{PHL(DY)}$						20		
$t_{PLH(DZ)}$	A1-A2 OR B1-B2	Z	32	C_L = 15 pF, R_L = 288 Ω		30		ns
$t_{PHL(DZ)}$						35	55	
$t_{PLH(SY)}$	STROBE A OR B	Y	32	C_L = 15 pF, R_L = 288 Ω		15	30	ns
$t_{PHL(SY)}$						20		
$t_{PLH(SZ)}$	STROBE A OR B	Z	32	C_L = 15 pF, R_L = 288 Ω		30		ns
$t_{PHL(SZ)}$						35	55	
$t_{PLH(GY, Y)}$	GATE G_Y	Y	33	C_L = 15 pF, R_L = 288 Ω		15	25	ns
$t_{PHL(GY, Y)}$						10		
$t_{PLH(GY, Z)}$	GATE G_Y	Z	33	C_L = 15 pF, R_L = 288 Ω		15		ns
$t_{PHL(GY, Z)}$						20	30	
$t_{PLH(GZ, Z)}$	GATE G_Z	Z	34	C_L = 15 pF, R_L = 288 Ω		15		ns
$t_{PHL(GZ, Z)}$						10	20	

typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geqslant$ 100 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 5)	*Differential Input Pulse:* V_{ID} = 2 V, $t_r = t_f$ = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery (see Note 6)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 5. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.
6. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

schematic

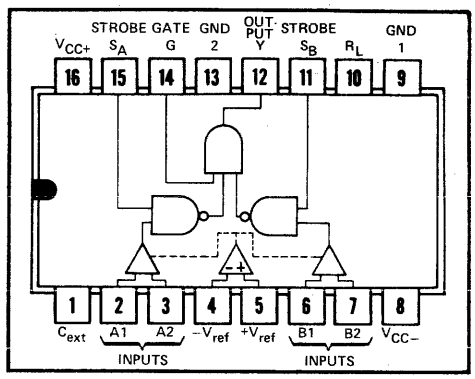


CIRCUIT TYPES SN7522, SN7523
DUAL-CHANNEL SENSE AMPLIFIERS

TRUTH TABLE

INPUTS					OUTPUT
A	B	G	S_A	S_B	Y
L	L	H	X	X	H
L	X	H	X	L	H
X	L	H	L	X	H
X	X	H	L	L	H
X	X	L	X	X	L
H	X	X	H	X	L
X	H	X	X	H	L

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = G(\overline{A} + \overline{S}_A)(\overline{B} + \overline{S}_B)$

definition of logic levels

INPUT	H	L	X
A or B†	$V_{ID} \geq V_T$ max	$V_{ID} \leq V_T$ min	Irrelevant
Any G or S	$V_I \geq V_{IH}$ min	$V_I \leq V_{IL}$ max	Irrelevant

†A and B are differential voltages (V_{ID}) between A1 and A2 or B1 and B2, respectively. For these circuits, V_{ID} is considered positive regardless of which terminal of each pair is positive with respect to the other.

3

electrical characteristics (unless otherwise noted $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $T_A = 0°C$ to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_T	Differential input threshold voltage (see Note 3, page 17)	7	V_{ref} = 15 mV	SN7522	11	15	19	mV
				SN7523	8	15	22	
			V_{ref} = 40 mV	SN7522	36	40	44	
				SN7523	33	40	47	
V_{ICF}	Common-mode input firing voltage (see Note 4, page 17)	none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-mode input pulse:* $t_r \leq 15$ ns, $t_f \leq 15$ ns, $t_w = 50$ ns			±2.5		V
I_{IB}	Differential-input bias current	2	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{ID} = 0$			30	75	μA
I_{IO}	Differential-input offset current	2	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{ID} = 0$			0.5		μA
V_{IH}	High-level input voltage (strobe and gate inputs)	8			2			V
V_{IL}	Low-level input voltage (strobe and gate inputs)	8					0.8	V
V_{OH}	High-level output voltage	8	$V_{CC+} = 4.75$ V, $V_{CC-} = -4.75$ V, $I_{OH} = -400$ μA		2.4	4		V
V_{OL}	Low-level output voltage	8	$V_{CC+} = 4.75$ V, $V_{CC-} = -4.75$ V, $I_{OL} = 16$ mA			0.25	0.4	V
I_{IH}	High-level input current (strobe and gate inputs)	9	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{IH} = 2.4$ V				40	μA
			$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{IH} = 5.25$ V				1	mA
I_{IL}	Low-level input current (strobe and gate inputs)	9	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{IL} = 0.4$ V			−1	−1.6	mA
I_{OH}	High-level output current	10	$V_{CC+} = 4.75$ V, $V_{CC-} = -4.75$ V, $V_O = 5.25$ V				250	μA
I_{OS}	Short-circuit output current	11	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V		−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $T_A = 25°C$			27	40	mA
I_{CC-}	Supply current from V_{CC-}	6	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $T_A = 25°C$			−15	−20	mA

‡All typical values are at $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $T_A = 25°C$.

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switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geq$ 100 pF, T_A = 25°C

PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(D)}$	A1-A2 OR B1-B2	Y	35	C_L = 15 pF, R_L = 288 Ω		20		ns
$t_{PHL(D)}$						30	45	
$t_{PLH(S)}$	STROBE A OR B	Y	35	C_L = 15 pF, R_L = 288 Ω		20		ns
$t_{PHL(S)}$						20	40	
$t_{PLH(G)}$	GATE	Y	36	C_L = 15 pF, R_L = 288 Ω		10		ns
$t_{PHL(G)}$						15	25	

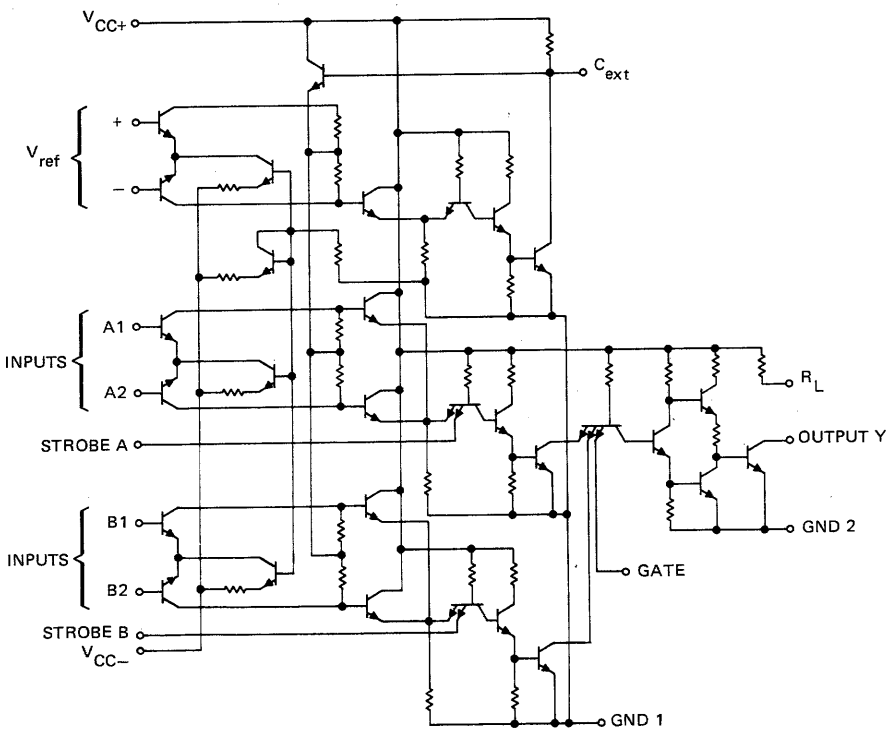
typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geq$ 100 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 5)	*Differential Input Pulse:* V_{ID} = 2 V, $t_r = t_f$ = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery (see Note 6)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 5. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential input-overload signal prior to the strobe-enable signal.
6. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

3

schematic



APPLICATION DATA

combined fan-out and wire-AND capabilities

The open-collector TTL gate, when supplied with a proper load resistor (R_L), may be paralleled with other similar TTL gates to perform the wire-AND function, and simultaneously, will drive from one to nine Series 54/74 loads. When no other open-collector gates are paralleled, this gate may be used to drive ten Series 54/74 loads. For any of these conditions an appropriate load resistor value must be determined for the desired circuit configuration. A maximum resistor value must be determined which will ensure that sufficient load current (to TTL loads) and off current (through paralleled outputs) will be available while the output is high. A minimum resistor value must be determined which will ensure that current through this resistor and sink current from the TTL loads will not cause the output voltage to rise above the low level even if one of the paralleled outputs is sinking all the current.

In both conditions (low and high level) the value of R_L is determined by:

$$R_L = \frac{V_{RL}}{I_{RL}}$$

where V_{RL} is the voltage drop in volts, and I_{RL} is the current in amperes.

high-level (off-state) circuit calculations (see figure I)

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_{CC} applied and the V_{OH} level required at the load:

$$V_{RL} = V_{CC} - V_{OH\,min}$$

The total current through the load resistor (I_{RL}) is the sum of the load currents (I_{IH}) and off-state reverse currents (I_{OH}) through each of the wire-AND-connected outputs:

$$I_{RL} = \eta \cdot I_{OH} + N \cdot I_{IH} \text{ to TTL loads}$$

Therefore, calculations for the maximum value of R_L would be:

$$R_{L(max)} = \frac{V_{CC} - V_{OH\,min}}{\eta \cdot I_{OH} + N \cdot I_{IH}}$$

where η = number of gates wire-AND-connected, and N = number of TTL loads.

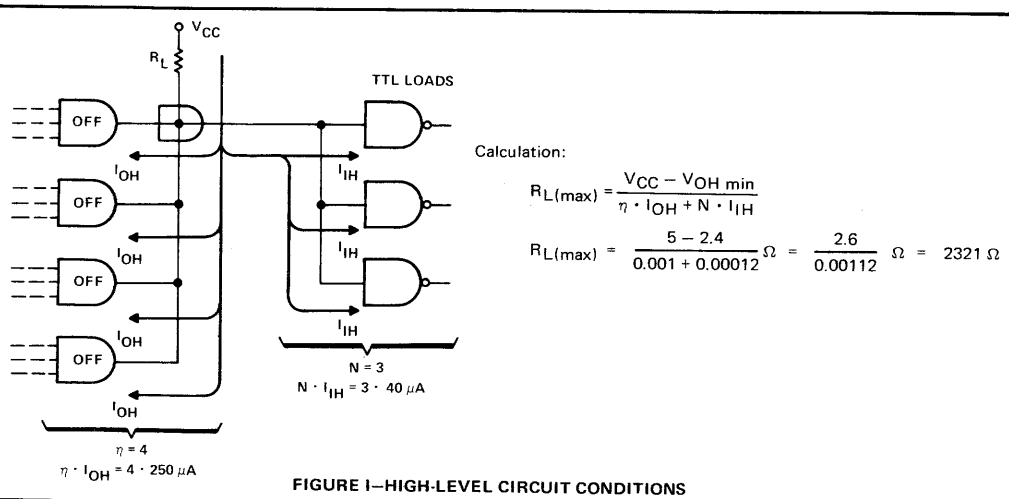


FIGURE I—HIGH-LEVEL CIRCUIT CONDITIONS

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APPLICATION DATA

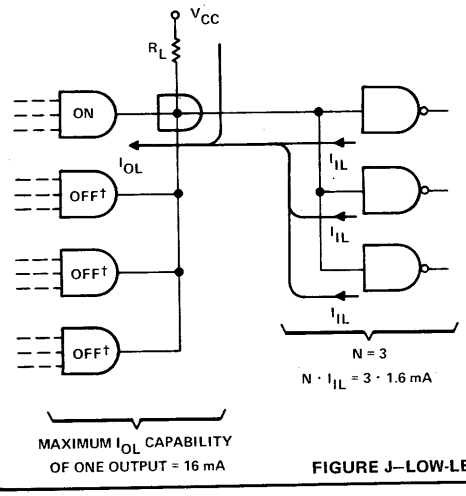
low-level (on-state) circuit calculations (see figure J)

The current through the resistor must be limited to the maximum sink-current of one output transistor. Note that if several output transistors are wire-AND connected, the current through R_L may be shared by those paralleled transistors. However, unless it can be absolutely guaranteed that more than one transistor will be on during low-level periods, the current must be limited to 16 mA, the maximum current which will ensure a low-level maximum of 0.4 volt.

Also, fan-out must be considered. Part of the 16 mA will be supplied from the inputs which are being driven. This reduces the amount of current which can be allowed through R_L.

Therefore, the equation used to determine the minimum value of R_L would be:

$$R_{L(min)} = \frac{V_{CC} - V_{OL\ max}}{I_{OL\ capability} - N \cdot I_{IL}}$$



Calculation:

$$R_{L(min)} = \frac{V_{CC} - V_{OL\ max}}{I_{OL\ capability} - N \cdot I_{OL}}$$

$$R_{L(min)} = \frac{5 - 0.4}{0.016 - 0.0048}\ \Omega = \frac{4.6}{0.0112}\ \Omega = 410\ \Omega$$

†Current into OFF outputs is negligible at the low logic level.

FIGURE J–LOW-LEVEL CIRCUIT CONDITIONS

driving series 54/74 loads and combining outputs

Table 1 provides minimum and maximum resistor values, calculated from equations shown above, for driving one to ten Series 54/74 loads and wire-AND connecting two to seven parallel outputs. Each value shown for one wire-AND output is determined by the fan-out plus the cutoff current of a single output transistor. Extension beyond seven wire-AND connections is permitted with fan-outs of seven or less if a valid minimum and maximum R_L is possible. When fanning-out to ten Series 54/74 loads, the calculation for the minimum value of R_L indicates that an infinite resistance should be used ($V_{RL} \div 0 = \infty$); however, the use of a 4-kΩ resistor in this case will satisfy the high-level condition and limit the low level to less than 0.43 volt.

TABLE 1

FAN-OUT TO TTL LOADS	WIRE-AND OUTPUTS							
	1	2	3	4	5	6	7	1 to 7
1	8965	4814	3291	2500	2015	1688	1452	319
2	7878	4482	3132	2407	1954	1645	1420	359
3	7027	4193	2988	2321	1897	1604	1390	410
4	6341	3939	2857	2241	1843	1566	1361	479
5	5777	3714	2736	2166	1793	1529	1333	575
6	5306	3513	2626	2096	1744	1494	1306	718
7	4905	3333	2524	2031	1699	1460	1280	958
8	4561	3170	2429	1969	1656	X	X	1437
9	4262	3023	X	X	X	X	X	2875
10	4000	X	X	X	X	X	X	4000§
	MAXIMUM							MIN
	LOAD RESISTOR VALUE IN OHMS							

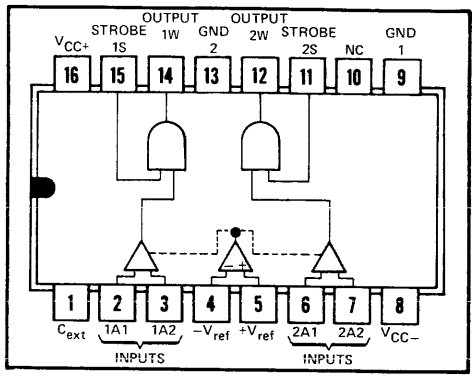
‡–All values shown in the table are based on:
High-level conditions: V_{CC} = 5 V, $V_{OH\ min}$ = 2.4 V
Low-level conditions: V_{CC} = 5 V, $V_{OL\ max}$ = 0.4 V
X–Not recommended or not possible.
§–The theoretical value is ∞. See explanation in text.

CIRCUIT TYPES SN7524, SN7525
DUAL SENSE AMPLIFIERS

TRUTH TABLE

INPUTS		OUTPUT
A	S	W
H	H	H
L	X	L
X	L	L

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: W = AS

NC—No internal connection

definition of logic levels

INPUT	H	L	X
A†	$V_{ID} \geq V_{T\ max}$	$V_{ID} \leq V_{T\ min}$	Irrelevant
S	$V_I \geq V_{IH\ min}$	$V_I \leq V_{IL\ max}$	Irrelevant

3

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

electrical characteristics (unless otherwise noted $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $T_A = 0°C$ to $70°C$)

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_T	Differential-input threshold voltage (see Note 3, page 17)	12	V_{ref} = 15 mV	SN7524	11	15	19	mV
				SN7525	8	15	22	
			V_{ref} = 40 mV	SN7524	36	40	44	
				SN7525	33	40	47	
V_{ICF}	Common-mode input firing voltage (see Note 4, page 17)	none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-Mode Input Pulse:* $t_r \leq 15$ ns, $t_f \leq 15$ ns, $t_w = 50$ ns			±2.5		V
I_{IB}	Differential-input bias current	2	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{ID} = 0$			30	75	μA
I_{IO}	Differential-input offset current	2	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{ID} = 0$			0.5		μA
V_{IH}	High-level input voltage (strobe inputs)	13			2			V
V_{IL}	Low-level input voltage (strobe inputs)	13					0.8	V
V_{OH}	High-level output voltage	13	$V_{CC+} = 4.75$ V, $V_{CC-} = -4.75$ V, $I_{OH} = -400$ μA		2.4	4		V
V_{OL}	Low-level output voltage	13	$V_{CC+} = 4.75$ V, $V_{CC-} = -4.75$ V, $I_{OL} = 16$ mA			0.25	0.4	V
I_{IH}	High-level input current (strobe inputs)	14	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{IH} = 2.4$ V				40	μA
			$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{IH} = 5.25$ V				1	mA
I_{IL}	Low-level input current (strobe inputs)	14	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{IL} = 0.4$ V			−1	−1.6	mA
I_{OS}	Short-circuit output current	15	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V		−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $T_A = 25°C$			25	40	mA
I_{CC-}	Supply current from V_{CC-}	6	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $T_A = 25°C$			−15	−20	mA

‡All typical values are at $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $T_A = 25°C$.

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switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geqslant$ 100 pF, T_A = 25°C

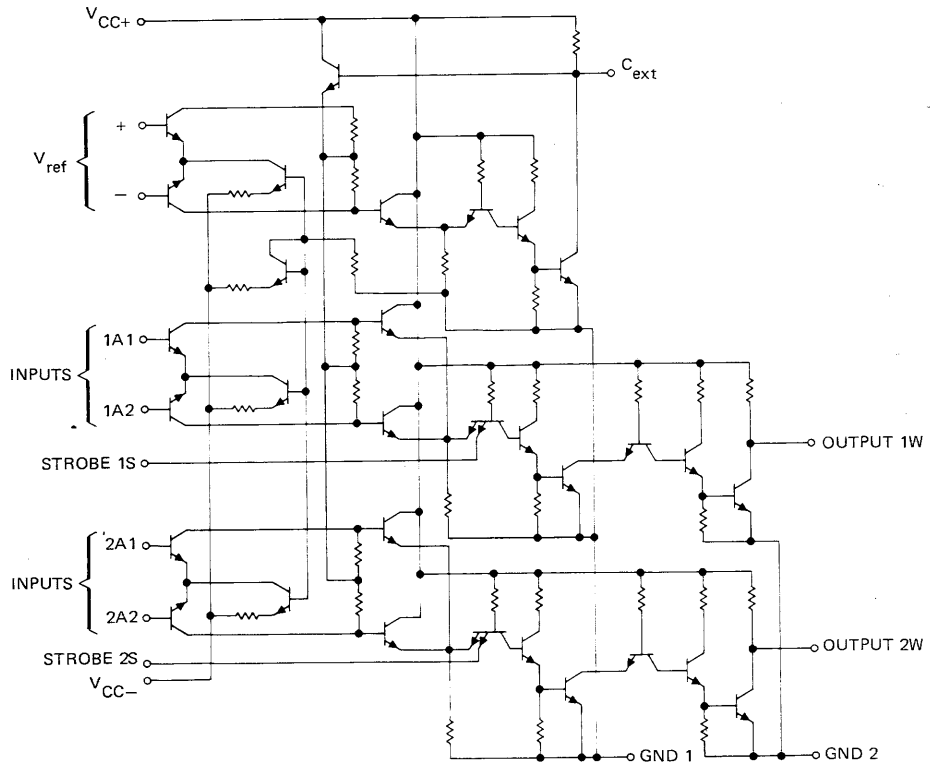
PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(D)}$	A1–A2	W	37	C_L = 15 pF, R_L = 288 Ω		25	40	ns
$t_{PHL(D)}$						20		
$t_{PLH(S)}$	STROBE	W	37	C_L = 15 pF, R_L = 288 Ω		15	30	ns
$t_{PHL(S)}$						20		

typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geqslant$ 100 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 5)	*Differential Input Pulse:* V_{ID} = 2 V, $t_r = t_f$ = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 6)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 5. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.
6. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

schematic



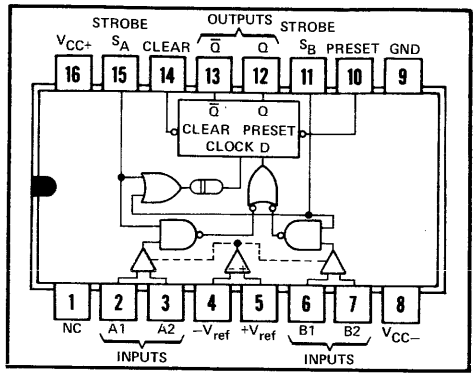
CIRCUIT TYPES SN7526, SN7527
DUAL-CHANNEL SENSE AMPLIFIERS WITH OUTPUT DATA REGISTERS

TRUTH TABLE

INPUTS AT TIME OF STROBE TRANSITION				OUTPUTS	
A	B	S_A	S_B	Q	$\overline{Q}$
H	X	↑	L	H	L
H	X	↑	↑	H	L
X	H	L	↑	H	L
X	H	↑	↑	H	L
L	L	↑	↑	L	H
L	X	↑	L	L	H
X	L	L	↑	L	H
X	X	H	↑	No Change	
X	X	↑	H	No Change	

NOTES: A. H = high level (steady state), L = low level (steady state), ↑ = transition from low level to high level, X = irrelevant.
B. Information at the inputs is transferred to the outputs on the positive-going edge of the strobe pulse.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Low input to preset sets Q to high level.
Low input to clear resets Q to low level.
Preset and clear dominate all other inputs.

NC—No internal connection

definition of logic levels

INPUT	H	L
A or B†	$V_{ID} \geq V_T$ max	$V_{ID} \leq V_T$ min
S_A or S_B	$V_I \geq V_{IH}$ min	$V_I \leq V_{IL}$ max

†A and B are differential voltages (V_{ID}) between A1 and A2 or B1 and B2, respectively. For these circuits, V_{ID} is considered positive regardless of which terminal of each pair is positive with respect to the other.

recommended operating conditions¶

	MIN	MAX	UNIT
Width of clear or preset pulse, t_w	30		ns
Width of strobe pulse, t_w	30		ns
Input setup time, t_{setup}◇	20		ns
Input hold time, t_{hold}□	5		ns

electrical characteristics (unless otherwise noted V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 0°C to 70°C)

PARAMETER			TEST FIGURE	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_T	Differential input threshold voltage (see Note 3, page 17)		16	V_{ref} = 15 mV	SN7526	11	15	19	mV
					SN7527	8	15	22	
				V_{ref} = 40 mV	SN7526	36	40	44	
					SN7527	33	40	47	
V_{ICF}	Common-mode input firing voltage (see Note 4, page 17)		none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-Mode Input Pulse:* $t_r \leq 15$ ns, $t_f \leq 15$ ns, t_w = 50 ns			±2.5		V
I_{IB}	Differential input bias current		2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			30	75	μA
I_{IO}	Differential input offset current		2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			0.5		μA
V_{IH}	High-level input voltage at strobe, preset, and clear inputs		17			2			V
V_{IL}	Low-level input voltage at strobe, preset, and clear inputs		17					0.8	V
V_{OH}	High-level output voltage		17	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OH} = −400 μA		2.4	3.6		V
V_{OL}	Low-level output voltage		17	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA			0.26	0.4	V
I_{IH}	High-level input current	clear and strobe inputs	19	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V				80	μA
		preset input						120	
		clear and strobe inputs	19	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V				2	mA
		preset input						3	
I_{IL}	Low-level input current	clear and strobe inputs	19	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V			−2	−3.2	mA
		preset input					−3	−4.8	
I_{OS}	Short-circuit output current§		18	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V		−18		−57	mA
I_{CC+}	Supply current from V_{CC+}		6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			27	40	mA
I_{CC-}	Supply current from V_{CC-}		6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			−10	−20	mA

¶These are in addition to the conditions on Page 5. See waveforms in Figure 30.
◇Setup time is the interval immediately preceding the positive-going edge of the strobe pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
□Hold time is the interval immediately following the positive-going edge of the strobe pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.
‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

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switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

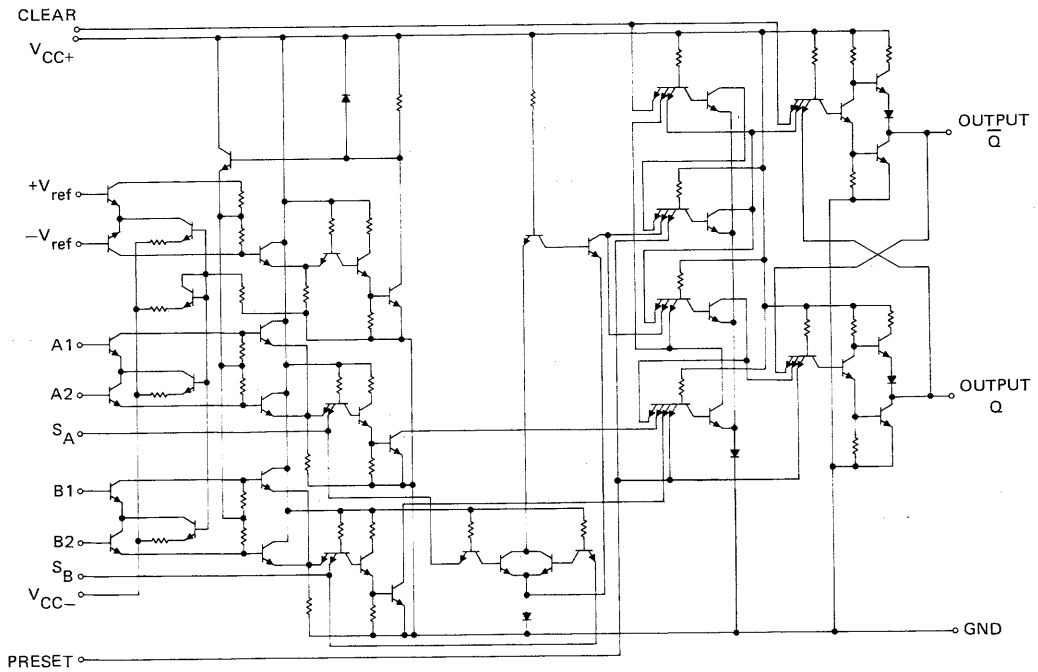
PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(SQ)}$	STROBE S_A or S_B	Q	38	C_L = 15 pF, R_L = 288 Ω		25	45	ns
$t_{PHL(SQ)}$						30	45	
$t_{PLH(S\overline{Q})}$	STROBE S_A or S_B	$\overline{Q}$	38	C_L = 15 pF, R_L = 288 Ω		25	45	ns
$t_{PHL(S\overline{Q})}$						30	45	
$t_{PLH(CQ)}$	CLEAR	$\overline{Q}$	38	C_L = 15 pF, R_L = 288 Ω		15	25	ns
$t_{PHL(CQ)}$		Q				20	40	
$t_{PLH(PQ)}$	PRESET	Q	38	C_L = 15 pF, R_L = 288 Ω		15	25	ns
$t_{PHL(P\overline{Q})}$		$\overline{Q}$				20	40	

typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 5)	*Differential Input Pulse:* V_{ID} = 2 V, $t_r = t_f$ = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 6)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 5. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.
6. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

schematic

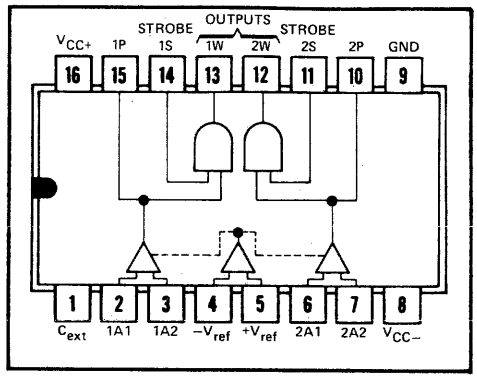


CIRCUIT TYPES SN7528, SN7529
DUAL SENSE AMPLIFIERS WITH PREAMPLIFIER TEST POINTS

TRUTH TABLE

INPUTS A	INPUTS S	OUTPUT W
H	H	H
L	X	L
X	L	L

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: W = AS

definition of logic levels

INPUT	H	L	X
A†	$V_{ID} \geq V_T$ max	$V_{ID} \leq V_T$ min	Irrelevant
S	$V_I \geq V_{IH}$ min	$V_I \leq V_{IL}$ max	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

3

electrical characteristics (unless otherwise noted V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_T	Differential-input threshold voltage (see Note 3, page 17)	20	V_{ref} = 15 mV	SN7528	11	15	19	mV
				SN7529	8	15	22	
			V_{ref} = 40 mV	SN7528	36	40	44	
				SN7529	33	40	47	
V_{ICF}	Common-mode input firing voltage (see Note 4, page 17)	none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-Mode Input Pulse:* $t_r \leq 15$ ns, $t_f \leq 15$ ns, t_w = 50 ns			±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			30	75	μA
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			0.5		μA
V_{IH}	High-level input voltage (strobe inputs)	21			2			V
V_{IL}	Low-level input voltage (strobe inputs)	21					0.8	V
V_{OH}	High-level output voltage	21	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OH} = −400 μA		2.4	4		V
V_{OL}	Low-level output voltage	21	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA			0.25	0.4	V
I_{IH}	High-level input current (strobe inputs)	22	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V				40	μA
			V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V				1	mA
I_{IL}	Low-level input current (strobe inputs)	22	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V			−1	−1.6	mA
I_{OS}	Short-circuit output current	23	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V		−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			25	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			−15	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

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switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(D)}$	A1–A2	W	39	C_L = 15 pF, R_L = 288 Ω		25	40	ns
$t_{PHL(D)}$						20		ns
$t_{PLH(S)}$	STROBE	W	39	C_L = 15 pF, R_L = 288 Ω		15	30	ns
$t_{PHL(S)}$						20		ns

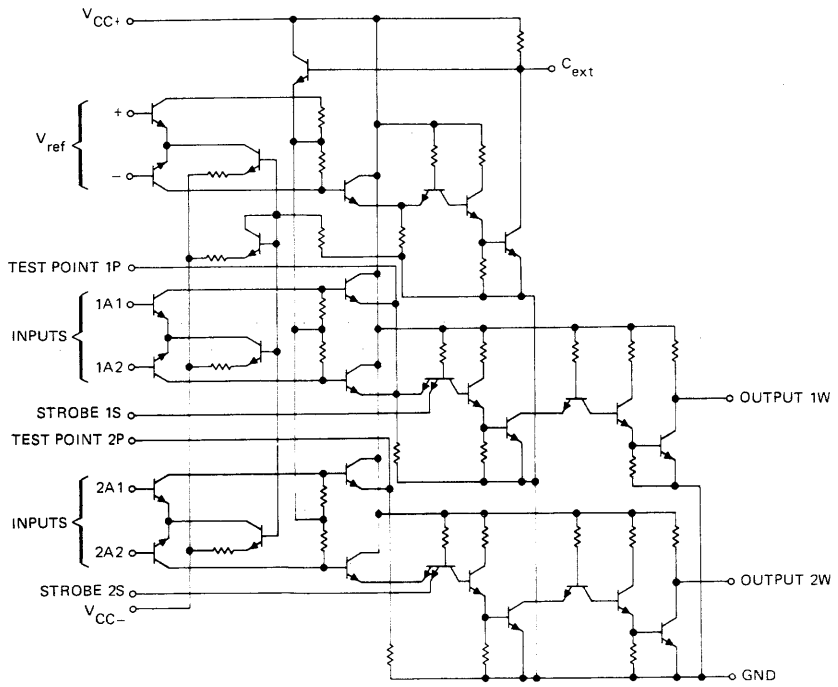
typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 5)	*Differential Input Pulse:* V_{ID} = 2 V, t_f = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 6)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 3. The differential-input threshold voltage (V_T) is defined as the d-c differential-input voltage (V_{ID}) required to force the output of the sense amplifier to the logic gate threshold voltage level.

4. Common-mode input firing voltage is the minimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common-mode input signal is applied with a strobe-enable present.
5. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input overload signal prior to the strobe-enable signal.
6. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

schematic

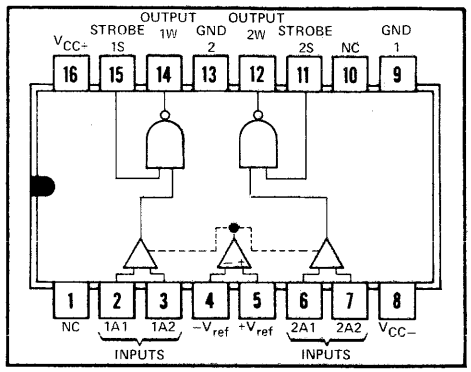


CIRCUIT TYPES SN75234, SN75235
DUAL SENSE AMPLIFIERS

TRUTH TABLE

INPUTS		OUTPUT
A	S	W
H	H	L
L	X	H
X	L	H

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $W = \overline{AS}$

NC—No internal connection

definition of logic levels

INPUT	H	L	X
A†	$V_{ID} \geq V_T$ max	$V_{ID} \leq V_T$ min	Irrelevant
S	$V_I \geq V_{IH}$ min	$V_I \leq V_{IL}$ max	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

3

electrical characteristics (unless otherwise noted $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $T_A = 0°C$ to $70°C$)

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_T	Differential-input threshold voltage (see Note 3, page 17)	24	V_{ref} = 15 mV	SN75234	11	15	19	mV
				SN75235	8	15	22	
			V_{ref} = 40 mV	SN75234	36	40	44	
				SN75235	33	40	47	
V_{ICF}	Common-mode input firing voltage (see Note 4, page 17)	none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-Mode Input Pulse:* $t_r \leq 15$ ns, $t_f \leq 15$ ns, $t_w = 50$ ns			±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			30	75	μA
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			0.5		μA
V_{IH}	High-level input voltage (strobe inputs)	25			2			V
V_{IL}	Low-level input voltage (strobe inputs)	25					0.8	V
V_{OH}	High-level output voltage	25	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OH} = −400 μA		2.4	4		V
V_{OL}	Low-level output voltage	25	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA			0.25	0.4	V
I_{IH}	High-level input current (strobe inputs)	26	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V				40	μA
			V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V				1	mA
I_{IL}	Low-level input current (strobe inputs)	26	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V			−1	−1.6	mA
I_{OS}	Short-circuit output current	27	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V		−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, $T_A = 25°C$			25	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, $T_A = 25°C$			−15	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, $T_A = 25°C$.

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switching characteristics, V_{CC+} = 5 V, V_{CC-} = –5 V, T_A = 25°C

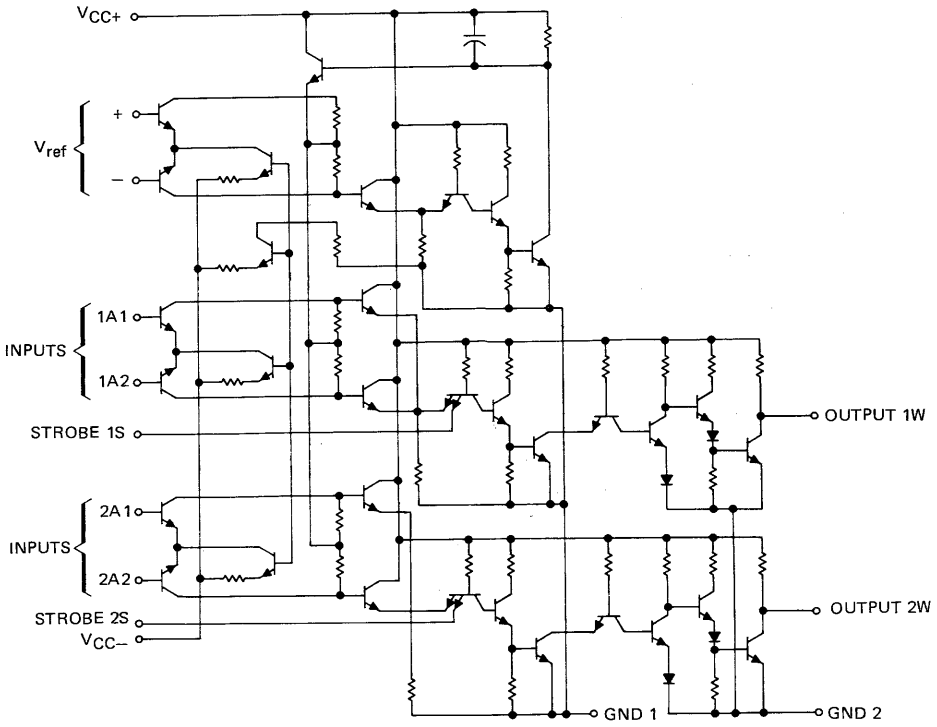
PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(D)}$	A1–A2	W	40	C_L = 15 pF, R_L = 288 Ω		25		ns
$t_{PHL(D)}$						25	40	
$t_{PLH(S)}$	STROBE	W	40	C_L = 15 pF, R_L = 288 Ω		25		ns
$t_{PHL(S)}$						15	30	

typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = –5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 5)	*Differential Input Pulse:* V_{ID} = 2 V, $t_r = t_f$ = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 6)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 5. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.
6. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

schematic

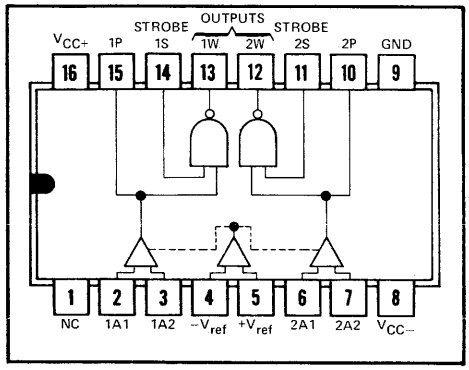


CIRCUIT TYPES SN75238, SN75239
DUAL SENSE AMPLIFIERS WITH PREAMPLIFIER TEST POINTS

TRUTH TABLE

INPUTS		OUTPUT
A	S	W
H	H	L
L	X	H
X	L	H

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $W = \overline{AS}$

NC—No internal connection

definition of logic levels

INPUT	H	L	X
A†	$V_{ID} \geq V_T$ max	$V_{ID} \leq V_T$ min	Irrelevant
S	$V_I \geq V_{IH}$ min	$V_I \leq V_{IL}$ max	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

3

electrical characteristics (unless otherwise noted $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $T_A =$ 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_T	Differential-input threshold voltage (see Note 3, page 17)	28	V_{ref} = 15 mV	SN75238	11	15	19	mV
				SN75239	8	15	22	
			V_{ref} = 40 mV	SN75238	36	40	44	
				SN75239	33	40	47	
V_{ICF}	Common-mode input firing voltage (see Note 4, page 17)	none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-Mode Input Pulse:* $t_r \leq 15$ ns, $t_f \leq 15$ ns, $t_w = 50$ ns			±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			30	75	μA
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			0.5		μA
V_{IH}	High-level input voltage (strobe inputs)	29			2			V
V_{IL}	Low-level input voltage (strobe inputs)	29					0.8	V
V_{OH}	High-level output voltage	29	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OH} = −400 μA		2.4	4		V
V_{OL}	Low-level output voltage	29	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA			0.25	0.4	V
I_{IH}	High-level input current (strobe inputs)	30	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V				40	μA
			V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V				1	mA
I_{IL}	Low-level input current (strobe inputs)	30	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V			−1	−1.6	mA
I_{OS}	Short-circuit output current	31	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V		−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			25	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			−15	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

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switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(D)}$	A1–A2	W	41	C_L = 15 pF, R_L = 288 Ω		25		ns
$t_{PHL(D)}$						25	40	ns
$t_{PLH(S)}$	STROBE	W	41	C_L = 15 pF, R_L = 288 Ω		25		ns
$t_{PHL(S)}$						15	30	ns

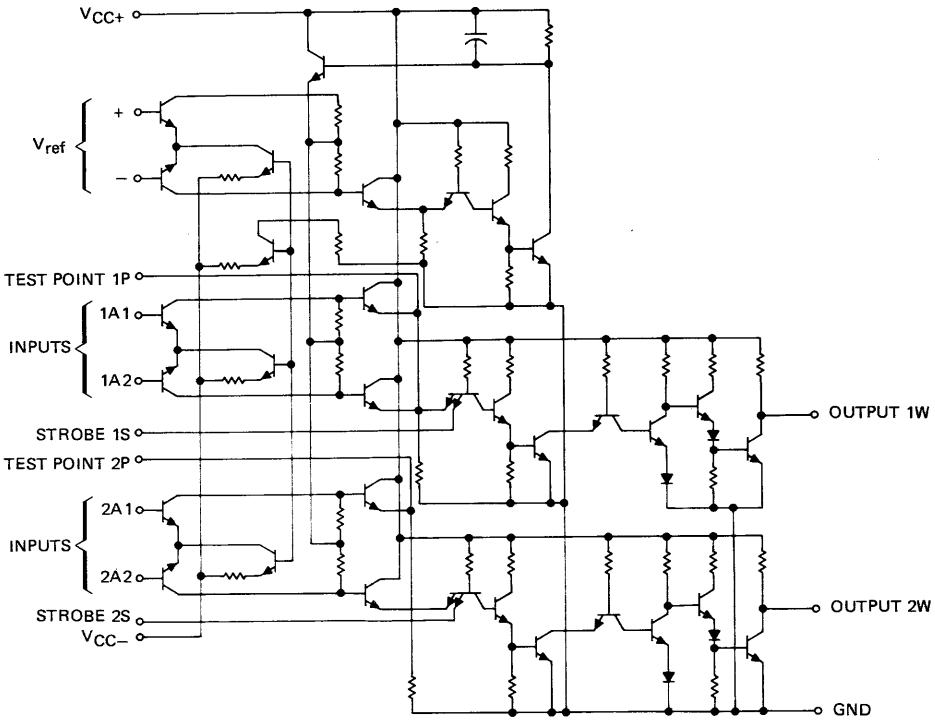
typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 5)	*Differential Input Pulse:* V_{ID} = 2 V, t_f = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 6)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 3. The differential-input threshold voltage (V_T) is defined as the d-c differential-input voltage (V_{ID}) required to force the output of the sense amplifier to the logic gate threshold voltage level.

4. Common-mode input firing voltage is the minimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common-mode input signal is applied with a strobe-enable present.
5. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input overload signal prior to the strobe-enable signal.
6. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

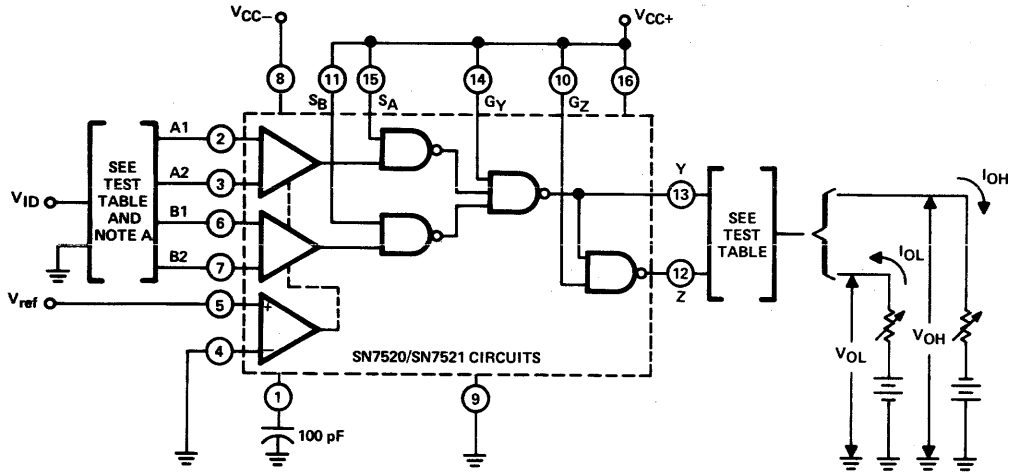
schematic



3

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT Y			OUTPUT Z		
				V_O	I_{OH}	I_{OL}	V_O	I_{OH}	I_{OL}
SN7520	A1-A2 or B1-B2	15 mV	≤11 mV	≤0.4 V		16 mA	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	15 mV	≥19 mV	≥2.4 V	−400 μA		≤0.4 V		16 mA
	A1-A2 or B1-B2	40 mV	≤36 mV	≤0.4 V		16 mA	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	40 mV	≥44 mV	≥2.4 V	−400 μA		≤0.4 V		16 mA
SN7521	A1-A2 or B1-B2	15 mV	≤ 8 mV	≤0.4 V		16 mA	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	15 mV	≥22 mV	≥2.4 V	−400 μA		≤0.4 V		16 mA
	A1-A2 or B1-B2	40 mV	≤33 mV	≤0.4 V		16 mA	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	40 mV	≥47 mV	≥2.4 V	−400 μA		≤0.4 V		16 mA

NOTE A: Each pair of differential inputs is tested separately with the other pair grounded.

FIGURE 1–V_T

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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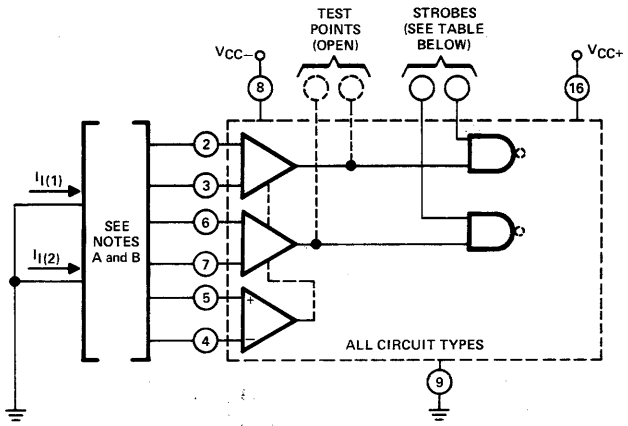
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



NOTES: A. Each preamplifier is tested separately. Inputs not under test are grounded.
B. $I_{IB} = I_{I(1)}$ and/or $I_{I(2)}$; $I_{IO} = I_{I(1)} - I_{I(2)}$; $I_{I(1)}$ and $I_{I(2)}$ are the currents into the two inputs of the pair under test.

PIN CONNECTIONS (OTHER THAN THOSE SHOWN ABOVE)

CIRCUIT TYPES	100 pF to GND	APPLY V_{CC+}	APPLY GND	LEAVE OPEN	OTHER
SN7520, SN7521	C_{ext} (1)	G_Y, G_Z, S_A, S_B (14)(10)(15)(11)		Y, Z (13)(12)	
SN7522, SN7523	C_{ext} (1)	G, S_A, S_B (14)(15)(11)	GND 2 (13)		R_L, Y (10)(12)
SN7524, SN7525	C_{ext} (1)	1S, 2S (15)(11)	GND 2 (13)	1W, 2W (14)(12)	
SN7526, SN7527		PRESET, CLEAR, S_A, S_B (10)(14)(15)(11)		Q, $\overline{Q}$ (12)(13)	
SN7528, SN7529	C_{ext} (1)	1S, 2S (14)(11)		1P, 2P, 1W, 2W (15)(10)(13)(12)	
SN75234, SN75235		1S, 2S (15)(11)	GND 2 (13)	1W, 2W (14)(12)	
SN75238, SN75239		1S, 2S (14)(11)		1P, 2P, 1W, 2W (15)(10)(13)(12)	

FIGURE 2–I_{IB}, I_{IO}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

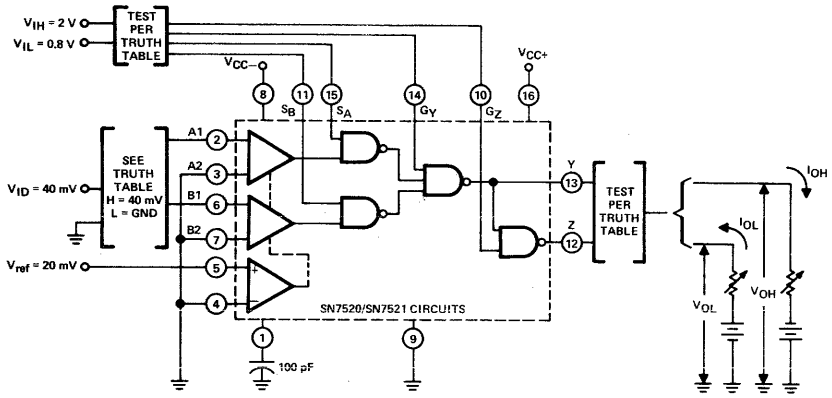
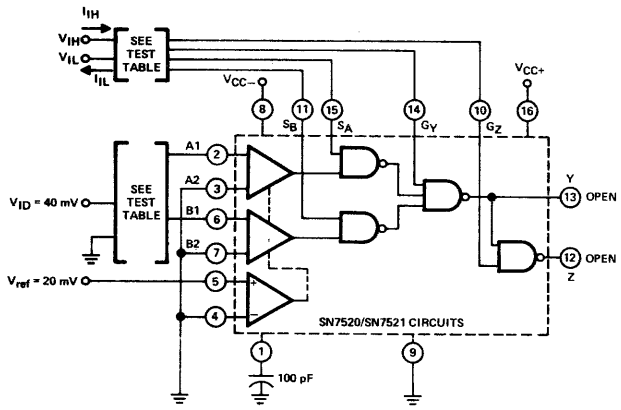


FIGURE 3–V_{IH}, V_{IL}, V_{OH}, V_{OL}



TEST TABLE

TEST	INPUT A1	INPUT B1	STROBE S_A	STROBE S_B	GATE G_Y	GATE G_Z
I_{IH} at STROBE S_A	GND	GND	V_{IH}	V_{IL}	V_{IL}	V_{IL}
I_{IH} at STROBE S_B	GND	GND	V_{IL}	V_{IH}	V_{IL}	V_{IL}
I_{IH} at GATE G_Y	V_{ID}	V_{ID}	V_{IH}	V_{IH}	V_{IH}	V_{IL}
I_{IH} at GATE G_Z	GND	GND	V_{IL}	V_{IL}	V_{IH}	V_{IH}
I_{IL} at STROBE S_A	V_{ID}	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at STROBE S_B	GND	V_{ID}	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at GATE G_Y	GND	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at GATE G_Z	GND	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}

FIGURE 4–I_{IH}, I_{IL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

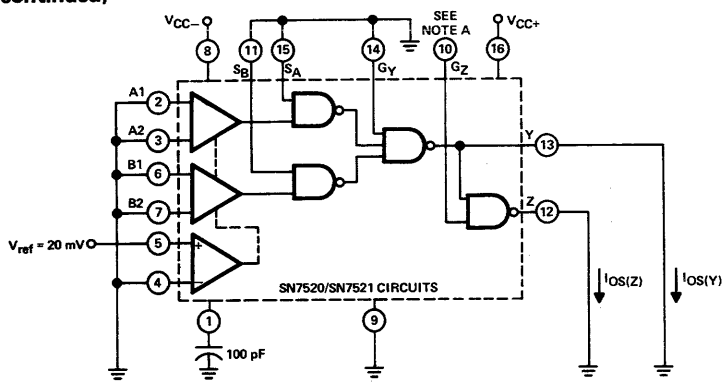
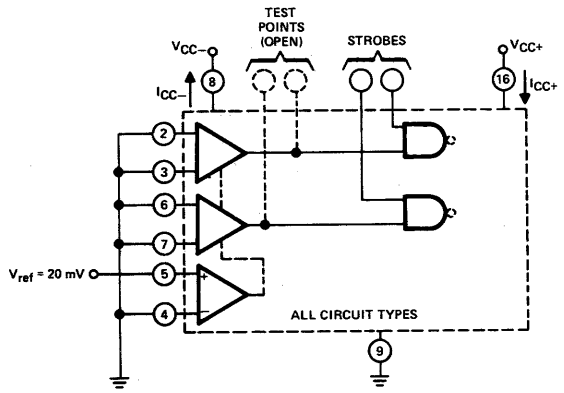


FIGURE 5–I_{OS}

NOTE A: When testing $I_{OS(Y)}$, Pin 10 is open; when testing $I_{OS(Z)}$, Pin 10 is grounded.



PIN CONNECTIONS (OTHER THAN THOSE SHOWN ABOVE)

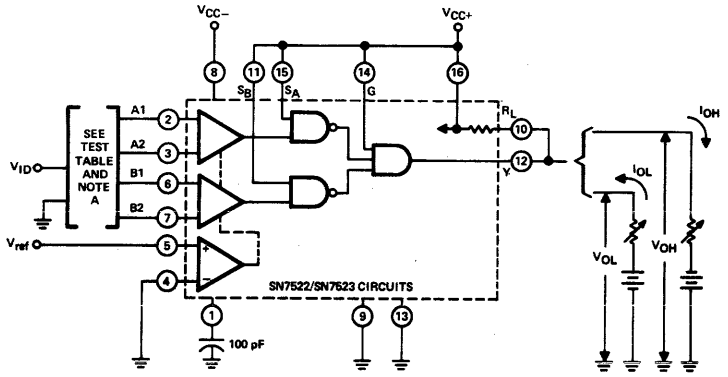
CIRCUIT TYPES	100 pF to GND	APPLY GND	LEAVE OPEN
SN7520, SN7521	C_{ext} (1)	G_Y, G_Z, S_A, S_B (14)(10)(15)(11)	Y, Z (13)(12)
SN7522, SN7523	C_{ext} (1)	G, S_A, S_B, GND 2 (14)(15)(11)(13)	R_L, Y (10)(12)
SN7524, SN7525	C_{ext} (1)	1S, 2S, GND 2 (15)(11)(13)	1W, 2W (14)(12)
SN7526, SN7527		S_A, S_B (15)(11)	PRESET, CLEAR, Q, $\overline{Q}$ (10)(14)(12)(13)
SN7528, SN7529	C_{ext} (1)	1S, 2S (14)(11)	1P, 2P, 1W, 2W (15)(10)(13)(12)
SN75234, SN75235		1S, 2S, GND 2 (15)(11)(13)	1W, 2W (14)(12)
SN75238, SN75239		1S, 2S (14)(11)	1P, 2P, 1W, 2W (15)(10)(13)(12)

FIGURE 6–I_{CC+}, I_{CC-}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT		
				V_O	I_{OH}	I_{OL}
SN7522	A1-A2 or B1-B2	15 mV	≤11 mV	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	15 mV	≥19 mV	≤0.4 V		16 mA
	A1-A2 or B1-B2	40 mV	≤36 mV	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	40 mV	≥44 mV	≤0.4 V		16 mA
SN7523	A1-A2 or B1-B2	15 mV	≤ 8 mV	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	15 mV	≥22 mV	≤0.4 V		16 mA
	A1-A2 or B1-B2	40 mV	≤33 mV	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	40 mV	≥47 mV	≤0.4 V		16 mA

NOTE A: Each pair of differential inputs is tested separately with the other pair grounded.

FIGURE 7–V_T

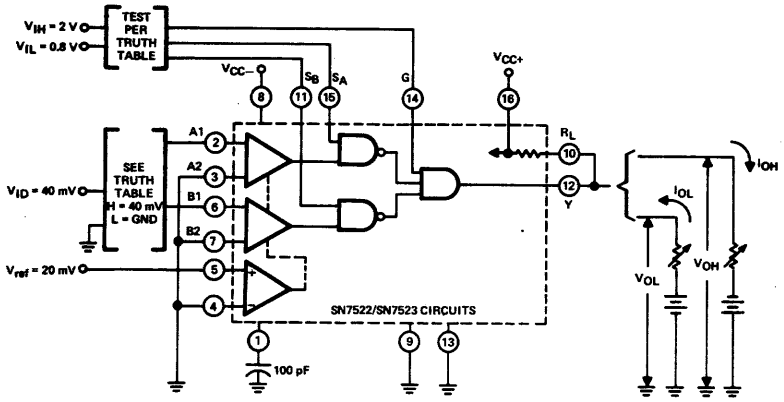


FIGURE 8–V_{IH}, V_{IL}, V_{OH}, V_{OL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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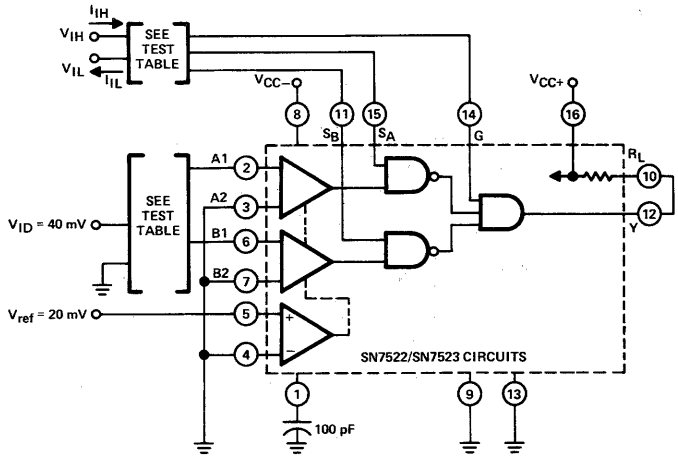
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

TEST	INPUT A1	INPUT B1	STROBE S_A	STROBE S_B	GATE G
I_{IH} at STROBE S_A	GND	GND	V_{IH}	V_{IL}	V_{IH}
I_{IH} at STROBE S_B	GND	GND	V_{IL}	V_{IH}	V_{IH}
I_{IH} at GATE	V_{ID}	V_{ID}	V_{IH}	V_{IH}	V_{IH}
I_{IL} at STROBE S_A	V_{ID}	GND	V_{IL}	V_{IL}	V_{IH}
I_{IL} at STROBE S_B	GND	V_{ID}	V_{IL}	V_{IL}	V_{IH}
I_{IL} at GATE	GND	GND	V_{IL}	V_{IL}	V_{IL}

FIGURE 9–I_{IH}, I_{IL}

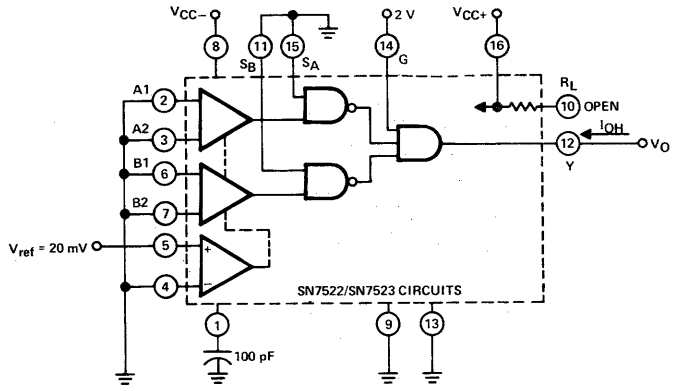


FIGURE 10–I_{OH}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

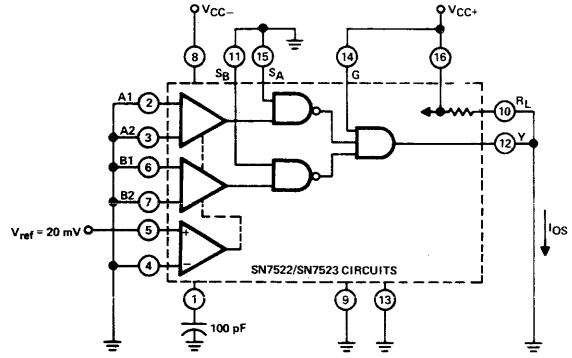
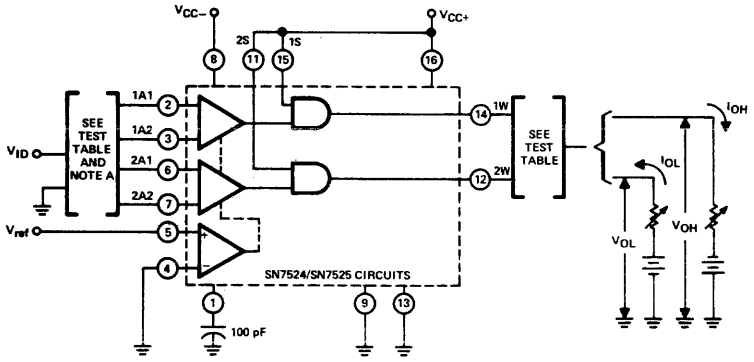


FIGURE 11–I_{OS}



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT		
				V_O	I_{OH}	I_{OL}
SN7524	A1-A2	15 mV	≤11 mV	≤0.4 V		16 mA
	A1-A2	15 mV	≥19 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≤36 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≥44 mV	≥2.4 V	−400 μA	
SN7525	A1-A2	15 mV	≤ 8 mV	≤0.4 V		16 mA
	A1-A2	15 mV	≥22 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≤33 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≥47 mV	≥2.4 V	−400 μA	

NOTE A: Each pair of differential inputs is tested separately with its corresponding output.

FIGURE 12–V_T

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

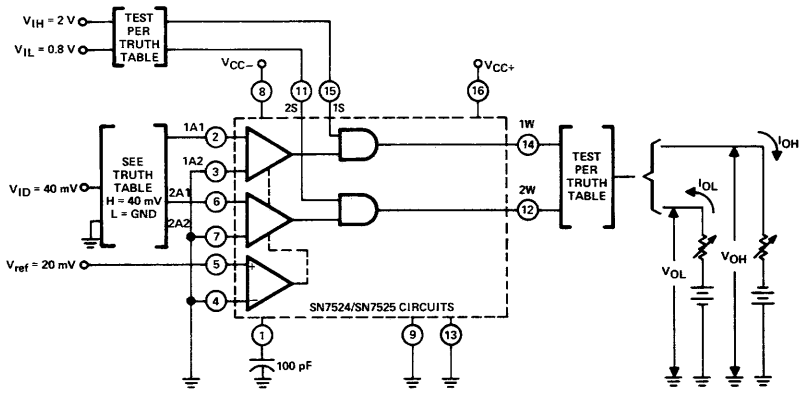
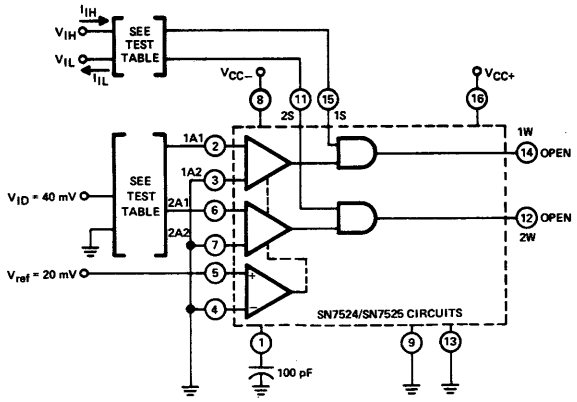


FIGURE 13–V_{IH}, V_{IL}, V_{OH}, V_{OL}



TEST TABLE

TEST	INPUT 1A1	INPUT 2A1	STROBE 1S	STROBE 2S
I_{IH} at STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} at STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} at STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

FIGURE 14–I_{IH}, I_{IL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

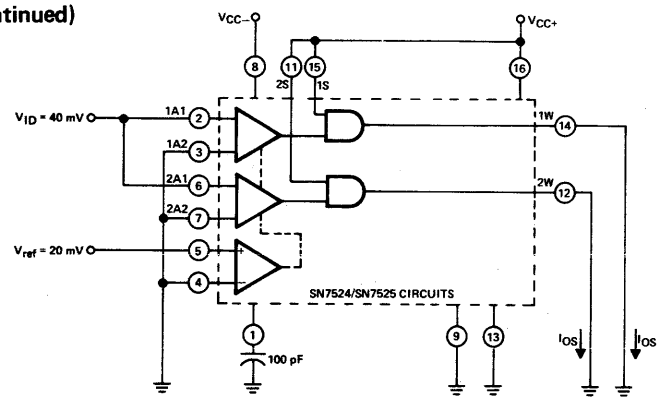
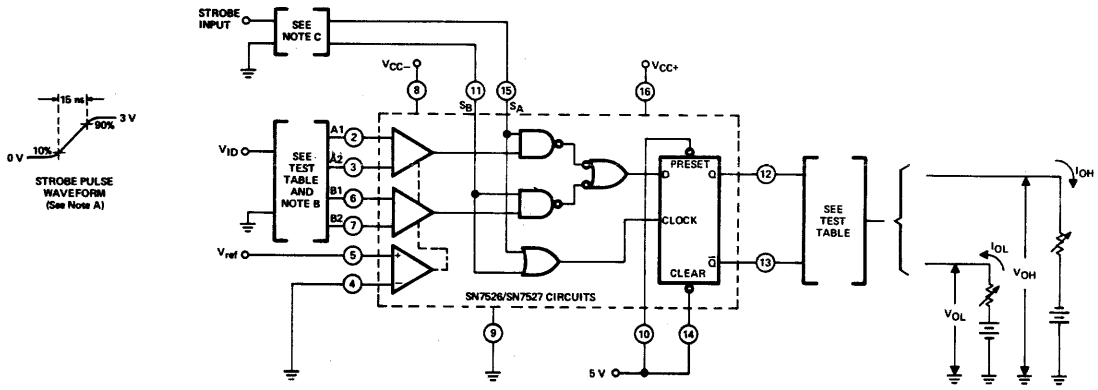


FIGURE 15–I_{OS}



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT Q			OUTPUT $\overline{Q}$		
				V_O	I_{OH}	I_{OL}	V_O	I_{OH}	I_{OL}
SN7526	A1-A2 or B1-B2	15 mV	≤11 mV	≤0.4 V		16 mA	≥2.4 V		16 mA
	A1-A2 or B1-B2	15 mV	≥19 mV	≥2.4 V	−400 μA		≤0.4 V	−400 μA	
	A1-A2 or B1-B2	40 mV	≤36 mV	≤0.4 V		16 mA	≥2.4 V		16 mA
	A1-A2 or B1-B2	40 mV	≥44 mV	≥2.4 V	−400 μA		≤0.4 V	−400 μA	
SN7527	A1-A2 or B1-B2	15 mV	≤ 8 mV	≤0.4 V		16 mA	≥2.4 V		16 mA
	A1-A2 or B1-B2	15 mV	≥22 mV	≥2.4 V	−400 μA		≤0.4 V	−400 μA	
	A1-A2 or B1-B2	40 mV	≤33 mV	≤0.4 V		16 mA	≥2.4 V		16 mA
	A1-A2 or B1-B2	40 mV	≥47 mV	≥2.4 V	−400 μA		≤0.4 V	−400 μA	

NOTES: A. The strobe input pulse is supplied by a generator with the following characteristics: Z_O = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_w = 500 ns, PRR = 1 MHz.

B. Each pair of differential inputs is tested separately with the other pair grounded.

C. Strobe input pulse is applied to Strobe A when inputs A1-A2 are being tested and to Strobe B when inputs B1-B2 are being tested. In each case, the other strobe input is grounded.

FIGURE 16–V_T

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

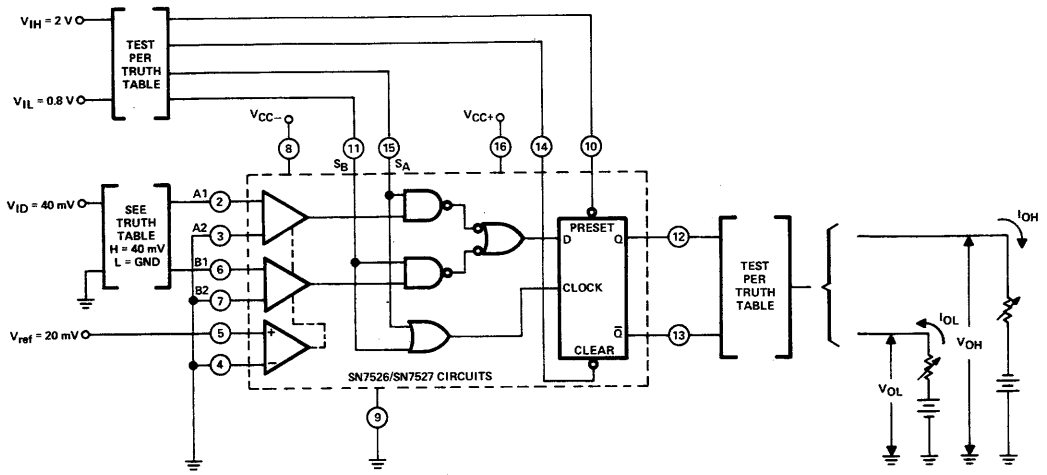
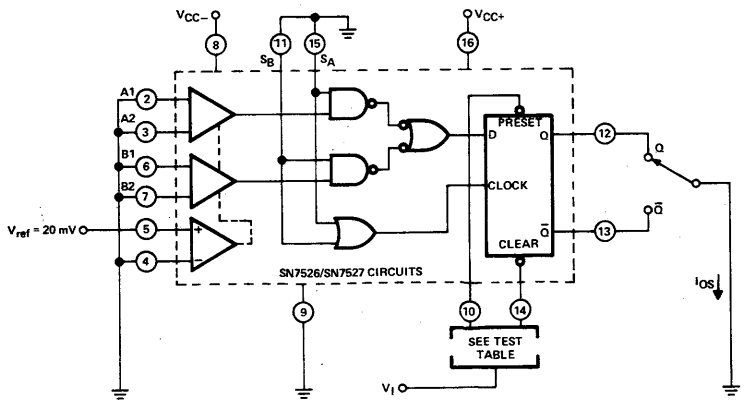


FIGURE 17–V_{IH}, V_{IL}, V_{OH}, V_{OL}



TEST TABLE

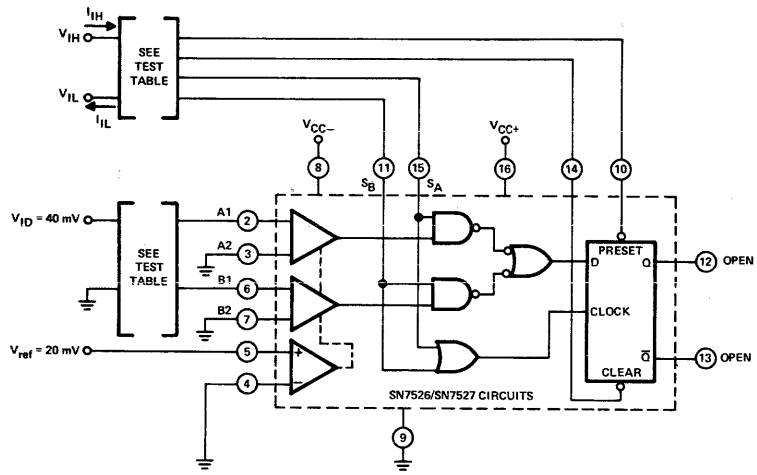
PARAMETER	PRESET	CLEAR
I_{OS} at OUTPUT Q	V_{IL}	V_{IH}
I_{OS} at OUTPUT $\overline{Q}$	V_{IH}	V_{IL}

FIGURE 18–I_{OS}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



3

TEST TABLE

PARAMETER	INPUT A1	INPUT B1	STROBE S_A	STROBE S_B	PRESET	CLEAR
I_{IH} at STROBE S_A	GND	GND	V_{IH}	V_{IL}	OPEN	OPEN
I_{IH} at STROBE S_B	GND	GND	V_{IL}	V_{IH}	OPEN	OPEN
I_{IH} at PRESET	GND	V_{ID}	V_{IL}	NOTE B	V_{IH}	V_{IH}
I_{IH} at CLEAR	GND	GND	V_{IL}	NOTE B	V_{IH}	V_{IH}
I_{IL} at STROBE S_A	V_{ID}	GND	V_{IL}	V_{IH}	OPEN	OPEN
I_{IL} at STROBE S_B	GND	V_{ID}	V_{IH}	V_{IL}	OPEN	OPEN
I_{IL} at PRESET	GND	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at PRESET	V_{ID}	GND	V_{IH}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at CLEAR	V_{ID}	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}

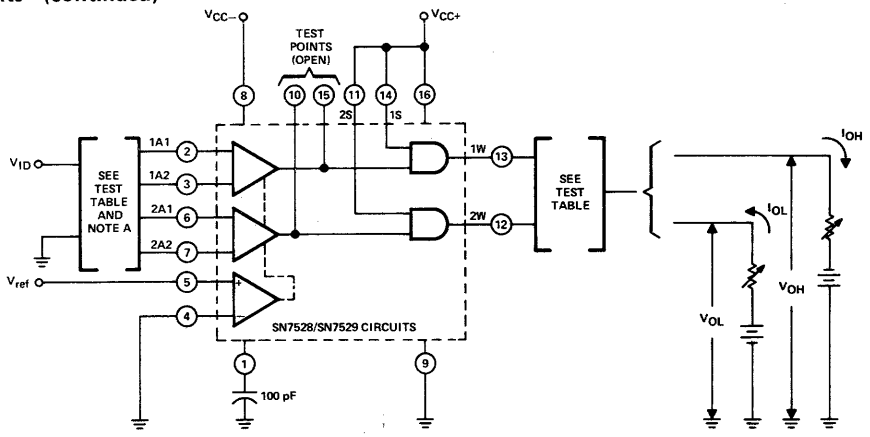
NOTES: A. Each input is tested separately.
B. Momentary ground, then V_{IH}.

FIGURE 19–I_{IH}, I_{IL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT		
				V_O	I_{OH}	I_{OL}
SN7528	A1-A2	15 mV	⩽11 mV	⩽0.4 V		16 mA
	A1-A2	15 mV	⩾19 mV	⩾2.4 V	−400 μA	
	A1-A2	40 mV	⩽36 mV	⩽0.4 V		16 mA
	A1-A2	40 mV	⩾44 mV	⩾2.4 V	−400 μA	
SN7529	A1-A2	15 mV	⩽ 8 mV	⩽0.4 V		16 mA
	A1-A2	15 mV	⩾22 mV	⩾2.4 V	−400 μA	
	A1-A2	40 mV	⩽33 mV	⩽0.4 V		16 mA
	A1-A2	40 mV	⩾47 mV	⩾2.4 V	−400 μA	

NOTE A: Each pair of inputs is tested separately with its corresponding output.

FIGURE 20–V_T

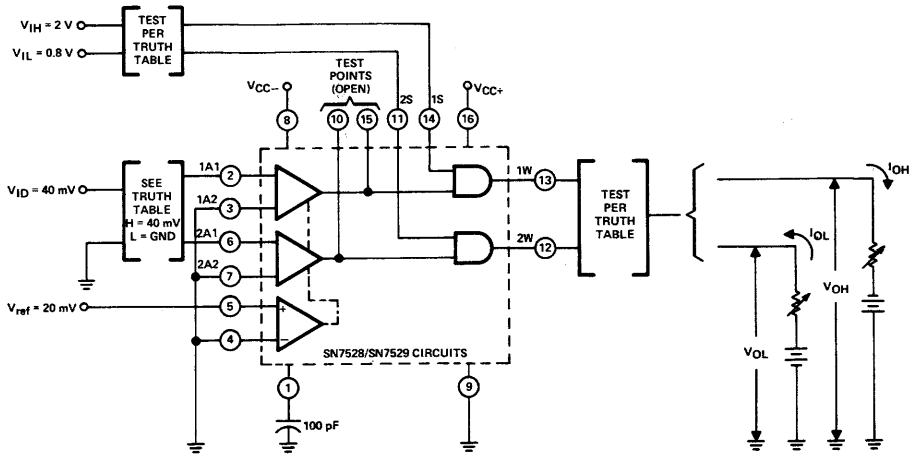
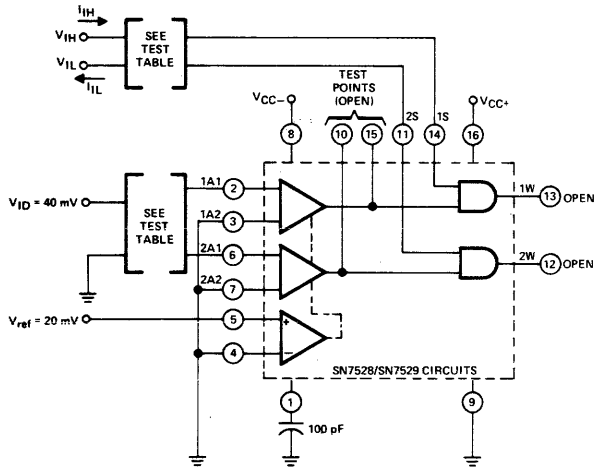


FIGURE 21–V_{IH}, V_{IL}, V_{OH}, V_{OL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

TEST	INPUT 1A1	INPUT 2A1	STROBE 1S	STROBE 2S
I_{IH} at STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} at STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} at STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

FIGURE 22–I_{IH}, I_{IL}

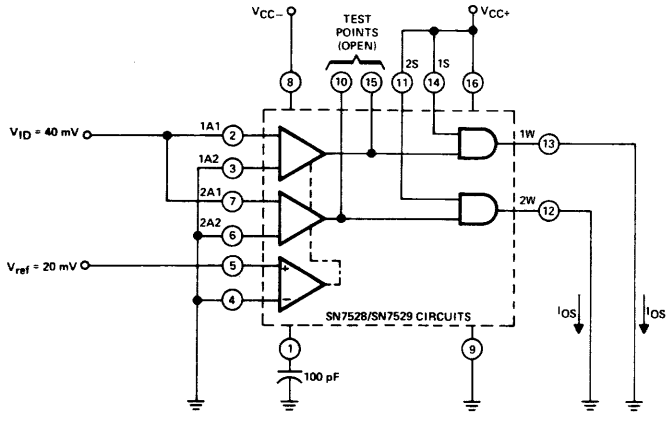


FIGURE 23–I_{OS}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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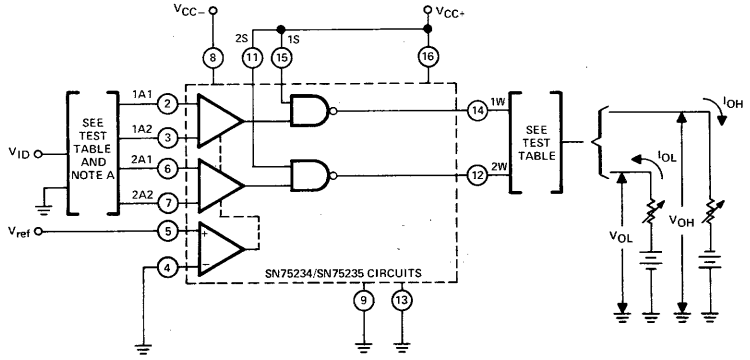
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT		
				V_O	I_{OH}	I_{OL}
SN75234	A1-A2	15 mV	⩽11 mV	⩾2.4 V	−400 μA	
	A1-A2	15 mV	⩾19 mV	⩽0.4 V		16 mA
	A1-A2	40 mV	⩽36 mV	⩾2.4 V	−400 μA	
	A1-A2	40 mV	⩾44 mV	⩽0.4 V		16 mA
SN75235	A1-A2	15 mV	⩽ 8 mV	⩾2.4 V	−400 μA	
	A1-A2	15 mV	⩾22 mV	⩽0.4 V		16 mA
	A1-A2	40 mV	⩽33 mV	⩾2.4 V	−400 μA	
	A1-A2	40 mV	⩾47 mV	⩽0.4 V		16 mA

NOTE A: Each pair of differential inputs is tested separately with its corresponding output.

FIGURE 24–V_T

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

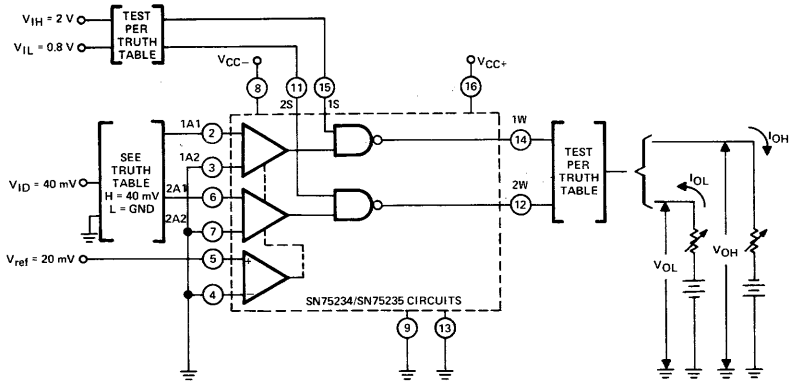
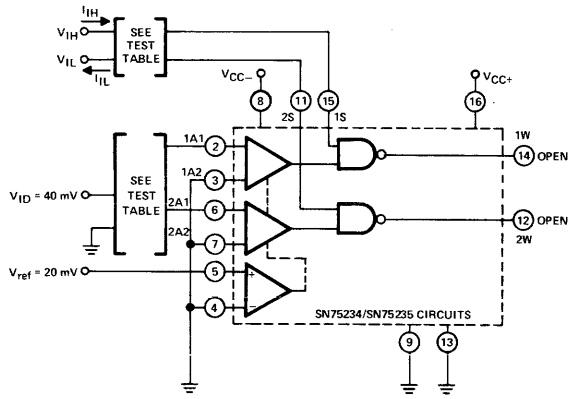


FIGURE 25–V_{IH}, V_{IL}, V_{OH}, V_{OL}

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

TEST	INPUT 1A1	INPUT 2A1	STROBE 1S	STROBE 2S
I_{IH} at STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} at STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} at STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

FIGURE 26–I_{IH}, I_{IL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

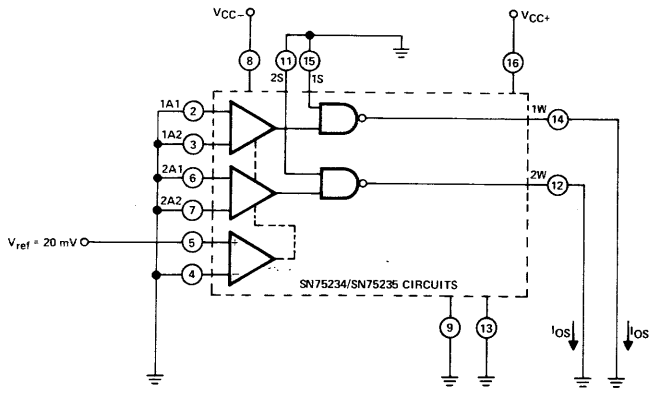


FIGURE 27–I_{OS}

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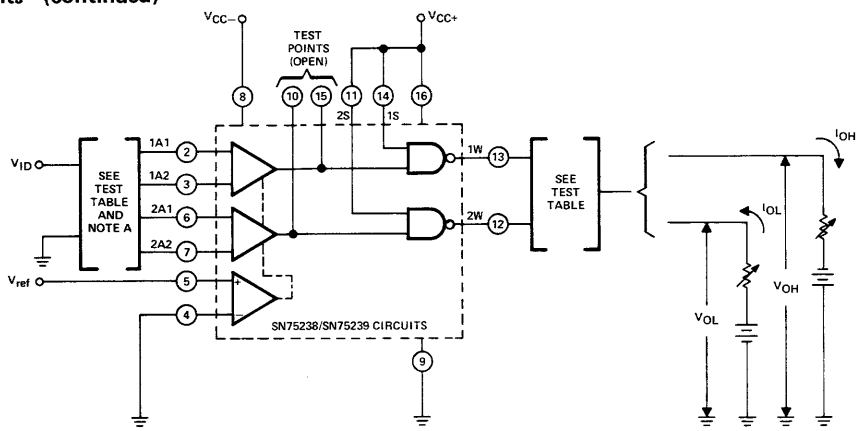
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT		
				V_O	I_{OH}	I_{OL}
SN75238	A1-A2	15 mV	≤11 mV	≥2.4 V	−400 μA	
	A1-A2	15 mV	≥19 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≤36 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≥44 mV	≤0.4 V		16 mA
SN75239	A1-A2	15 mV	≤ 8 mV	≥2.4 V	−400 μA	
	A1-A2	15 mV	≥22 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≤33 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≥47 mV	≤0.4 V		16 mA

NOTE A: Each pair of inputs is tested separately with its corresponding output.

FIGURE 28–V_T

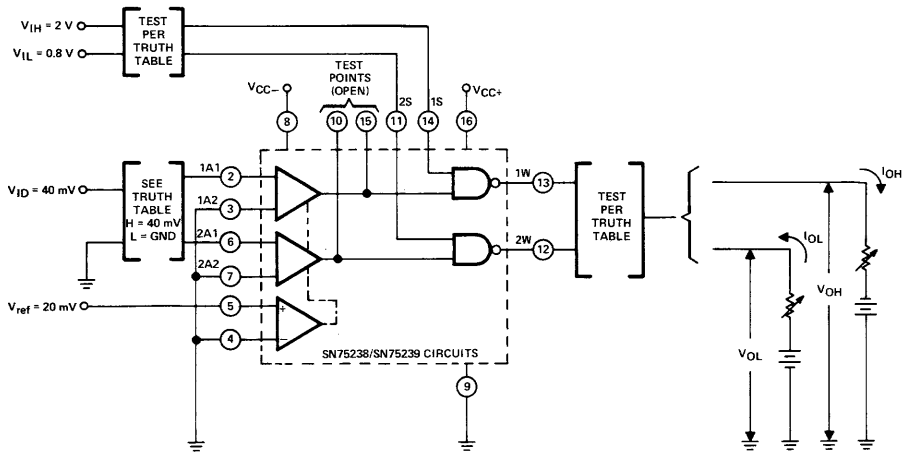
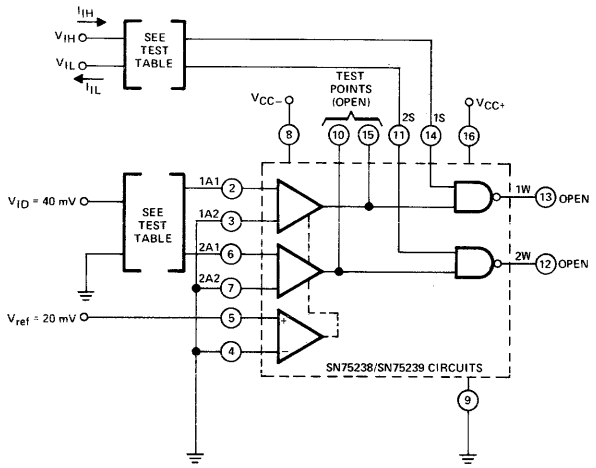


FIGURE 29–V_{IH}, V_{IL}, V_{OH}, V_{OL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

TEST	INPUT 1A1	INPUT 2A1	STROBE 1S	STROBE 2S
I_{IH} at STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} at STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} at STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

FIGURE 30–I_{IH}, I_{IL}

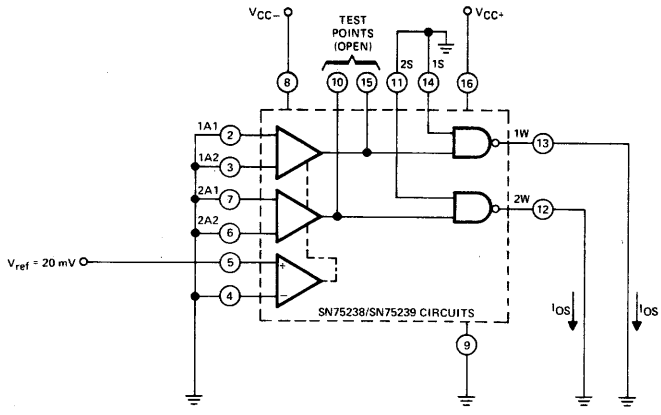
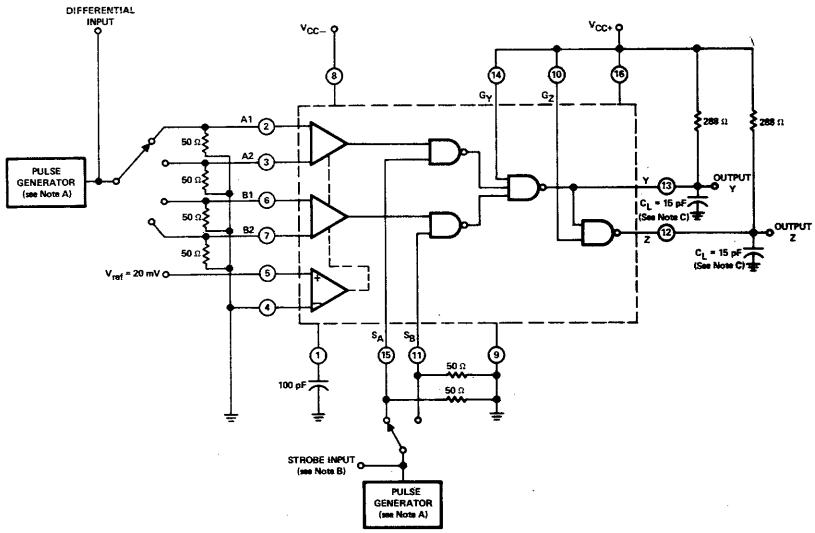


FIGURE 31–I_{OS}

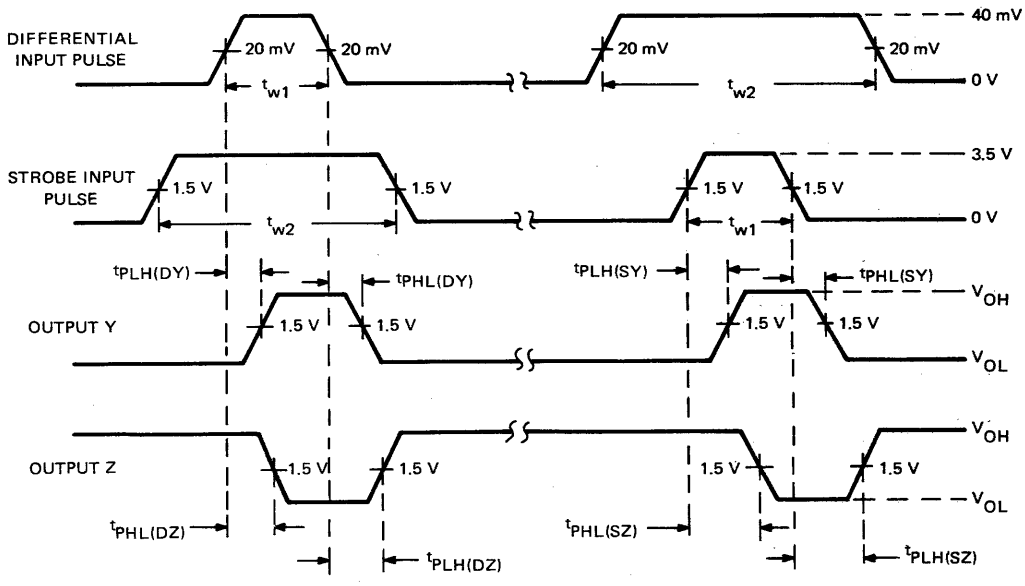
†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.

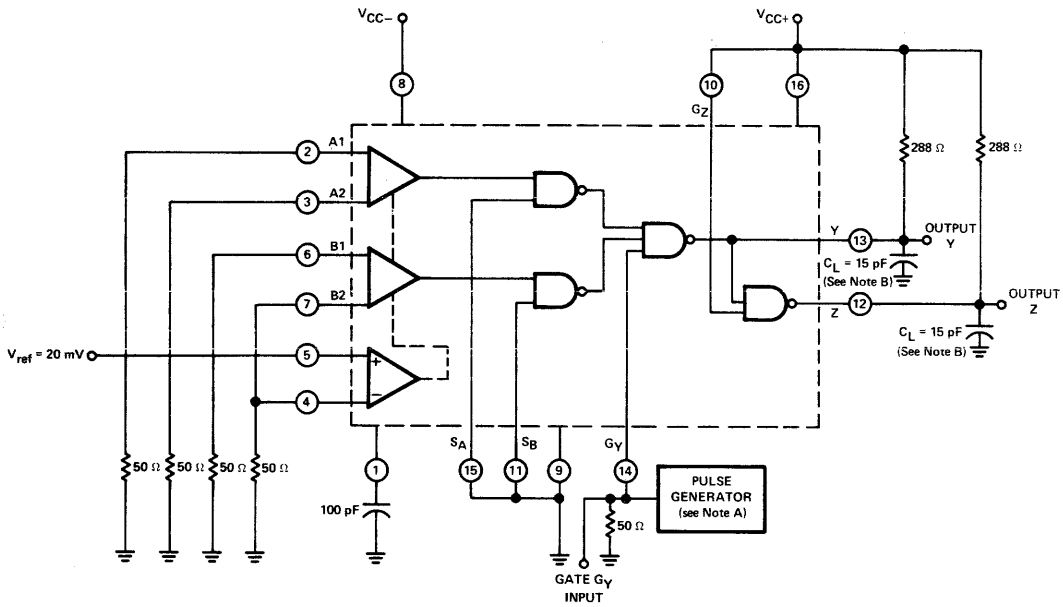
B. The strobe input pulse is applied to Strobe S_A when inputs A1-A2 are being tested and to Strobe S_B when inputs B1-B2 are being tested.

C. C_L includes probe and jig capacitance.

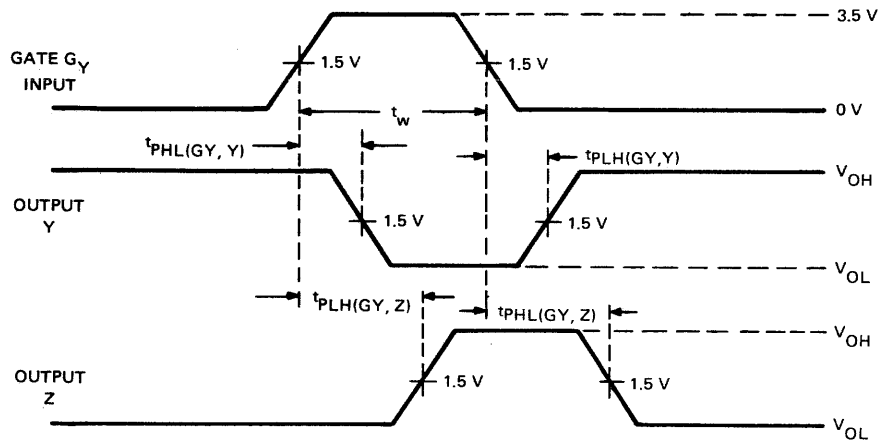
FIGURE 32–SN7520/SN7521 PROPAGATION DELAY TIMES FROM DIFFERENTIAL AND STROBE INPUTS

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_w = 100 ns, and PRR = 1 MHz.
B. C_L includes probe and jig capacitance.

FIGURE 33–SN7520/SN7521 PROPAGATION DELAY TIMES FROM GATE GY

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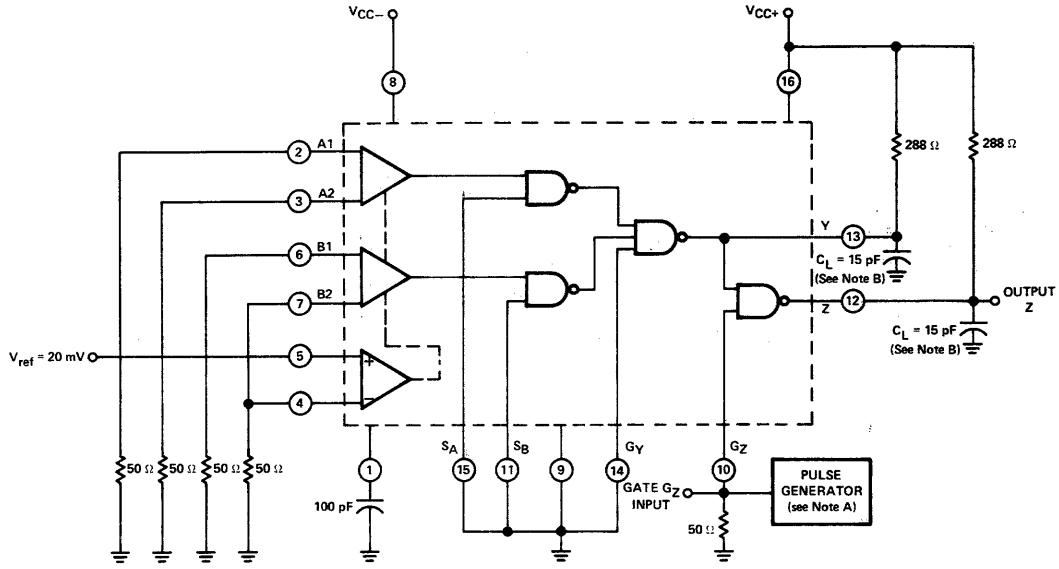
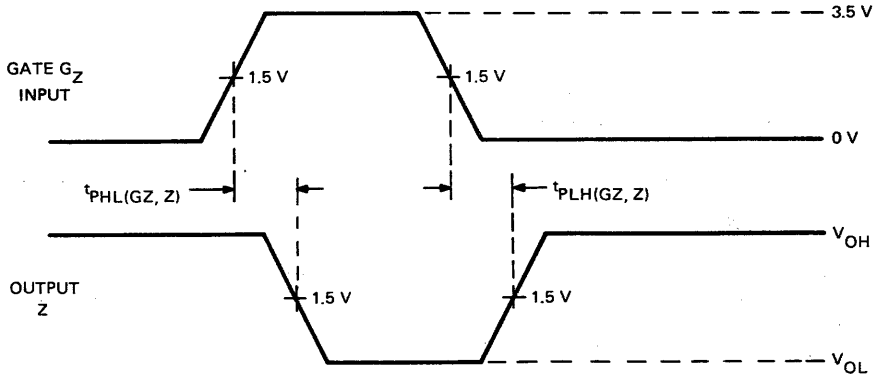
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



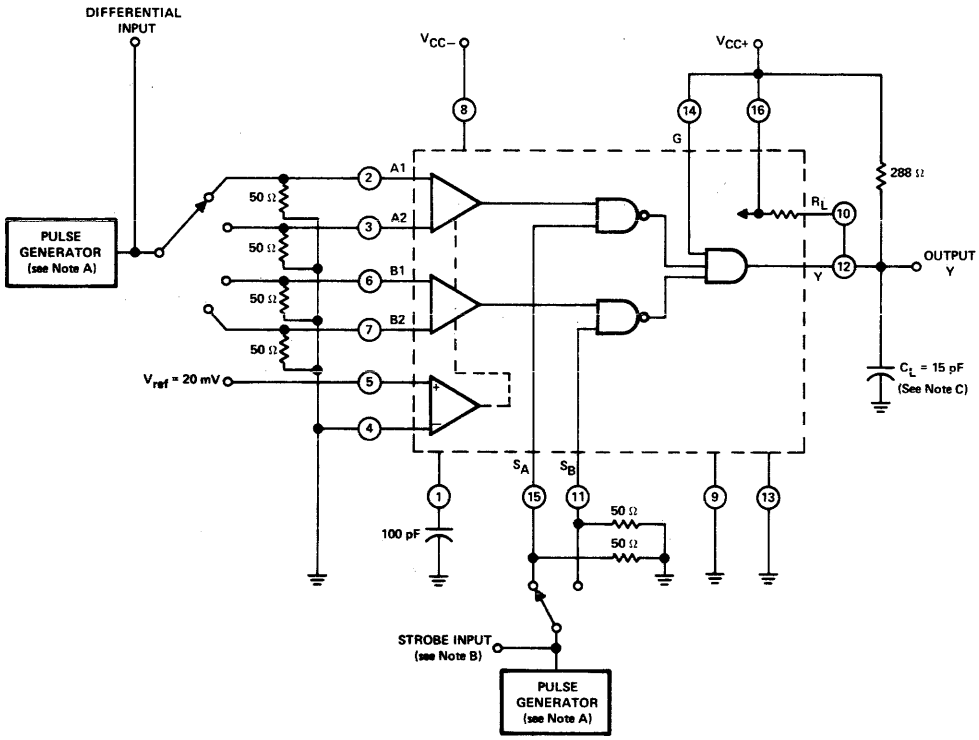
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_w = 100 ns, and PRR = 1 MHz.
B. C_L includes probe and jig capacitance.

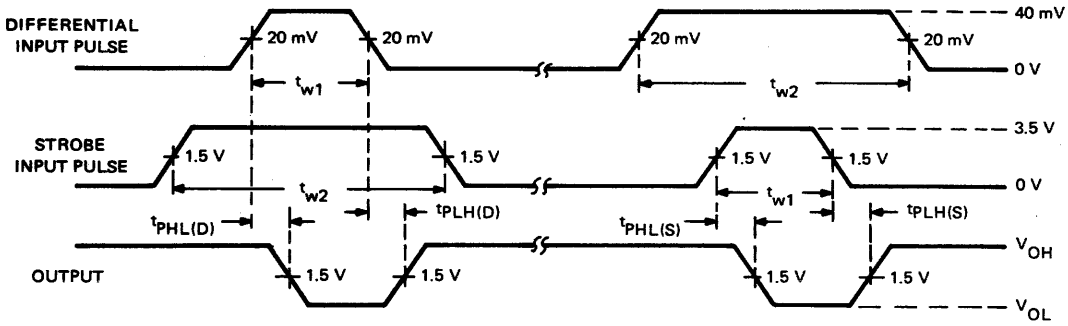
FIGURE 34–SN7520/SN7521 PROPAGATION DELAY TIMES FROM GATE G_Z

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$, $t_r = t_f = 15 \pm 5$ ns, $t_{w1} = 100$ ns, $t_{w2} = 300$ ns, PRR = 1 MHz.

B. The strobe input pulse is applied to Strobe S_A when testing inputs A1-A2 and to Strobe S_B when testing inputs B1-B2.

C. C_L includes probe and jig capacitance.

FIGURE 35–SN7522/SN7523 PROPAGATION DELAY TIMES FROM DIFFERENTIAL AND STROBE INPUTS

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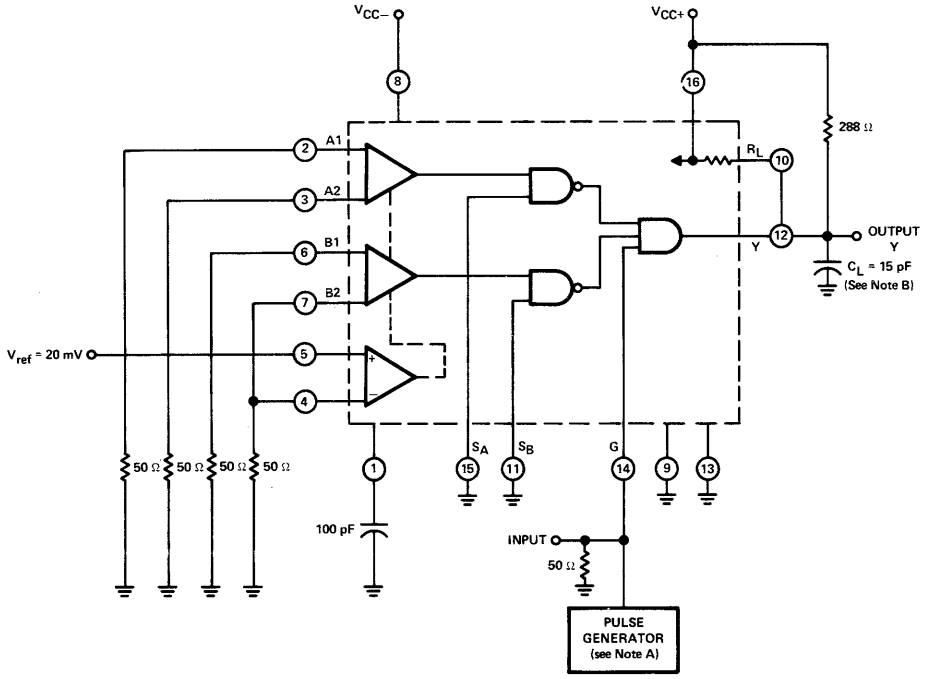
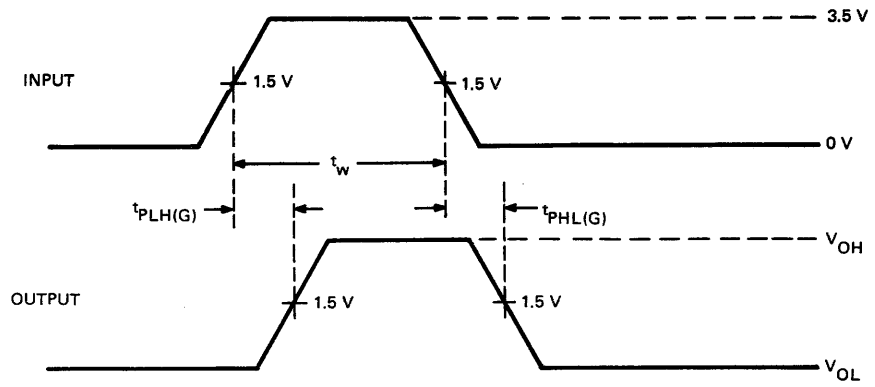
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

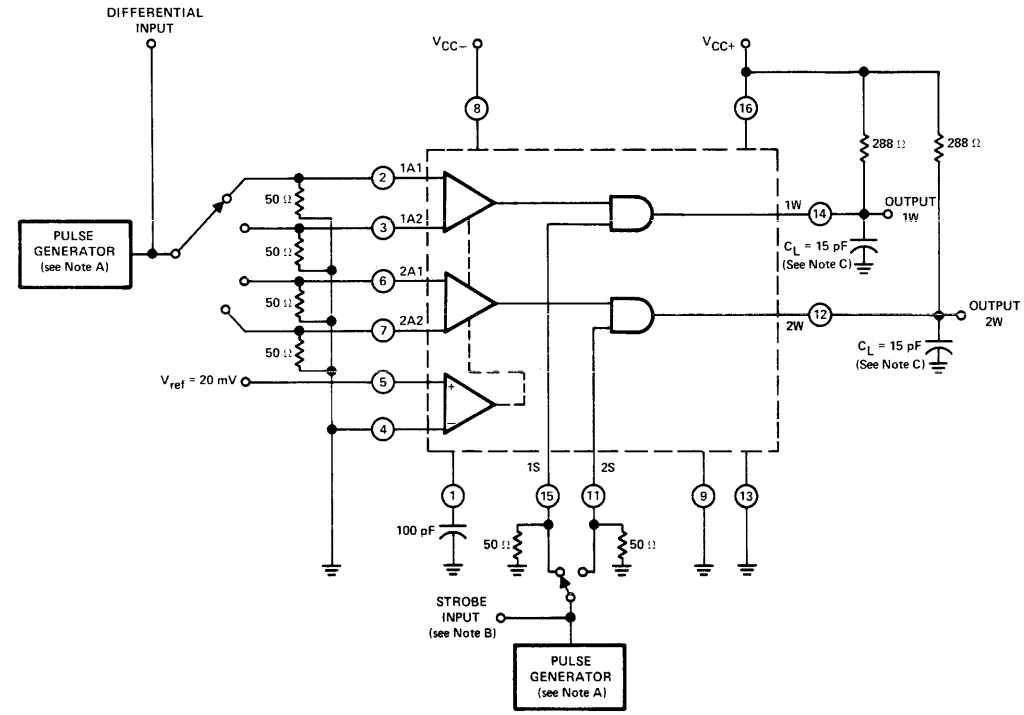
NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_{p1} = 100 ns, t_{p2} = 300 ns, t_{p3} = 0.8 μs, PRR = 1 MHz.

B. C_L includes probe and jig capacitance.

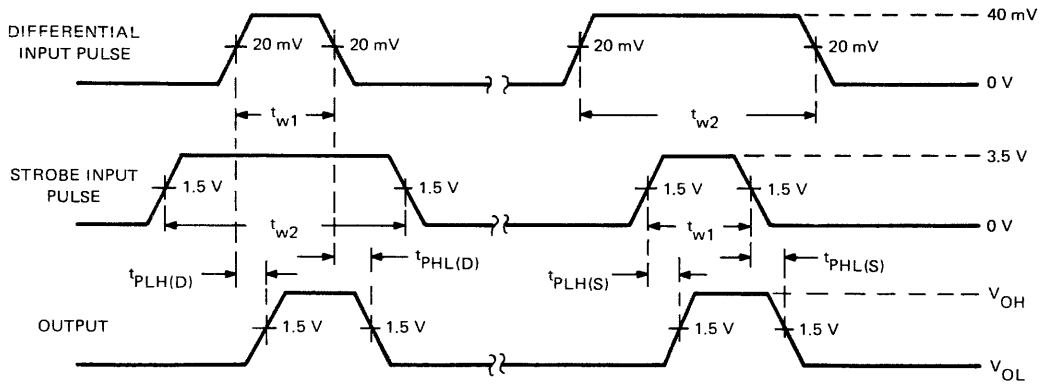
FIGURE 36–SN7522/SN7523 PROPAGATION DELAY TIMES FROM GATE INPUT

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.

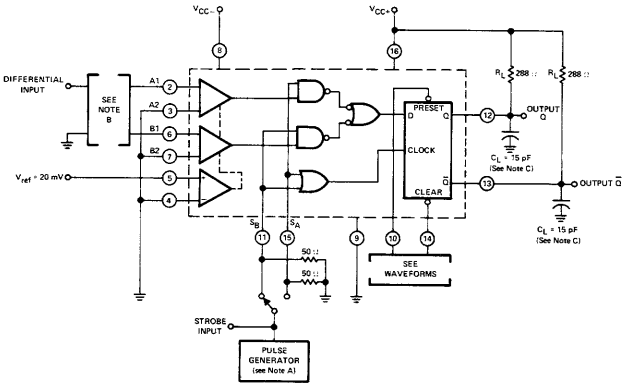
B. The strobe input pulse is applied to Strobe 1S when inputs 1A1-1A2 are being tested and to Strobe 2S when inputs 2A1-2A2 are being tested.

C. C_L includes probe and jig capacitance.

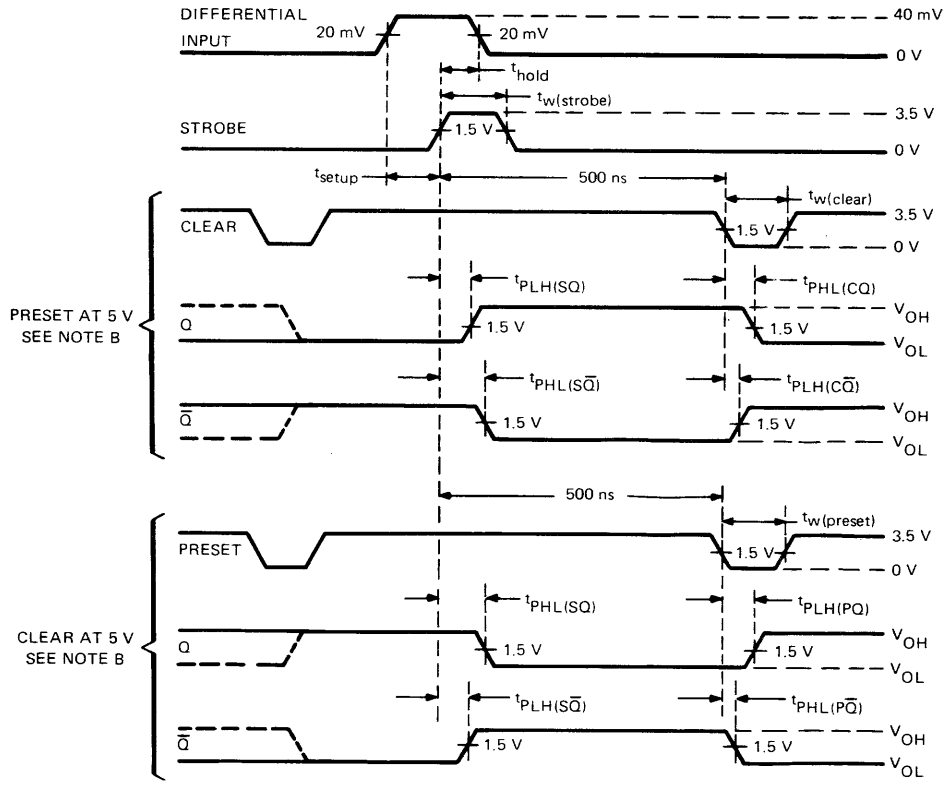
FIGURE 37—SN7524/SN7525 PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



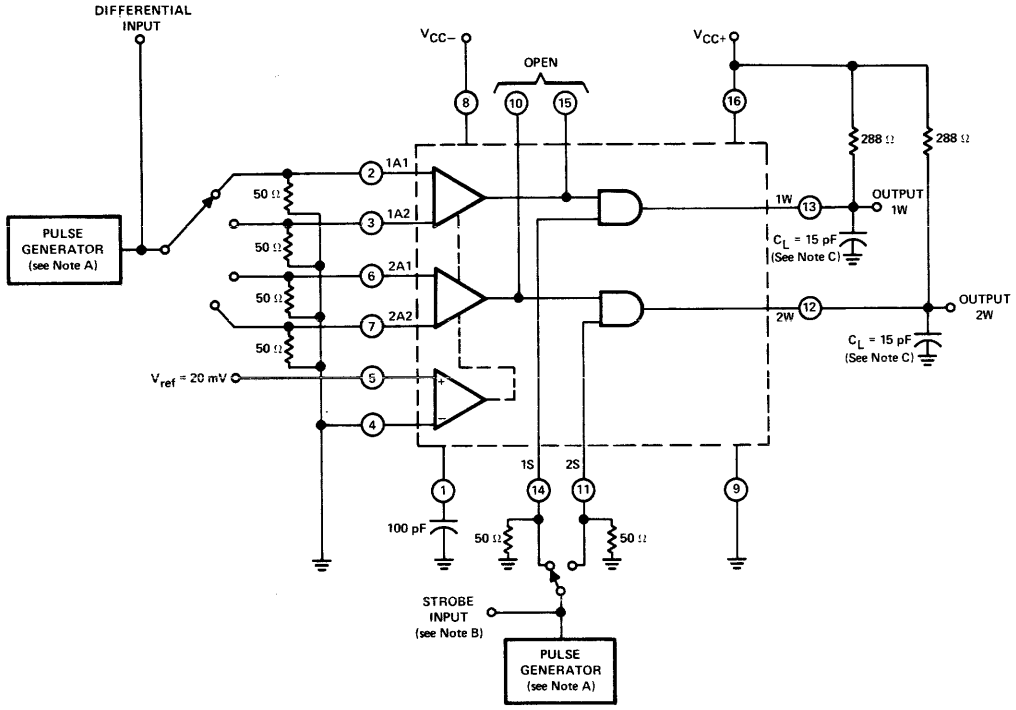
VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_w = 50 ns, and PRR = 1 MHz.
B. Each preamplifier is tested separately. Apply 40-mV pulse to input A1 when testing Strobe S_A and to B1 when testing Strobe S_B.
C. C_L includes probe and jig capacitance.

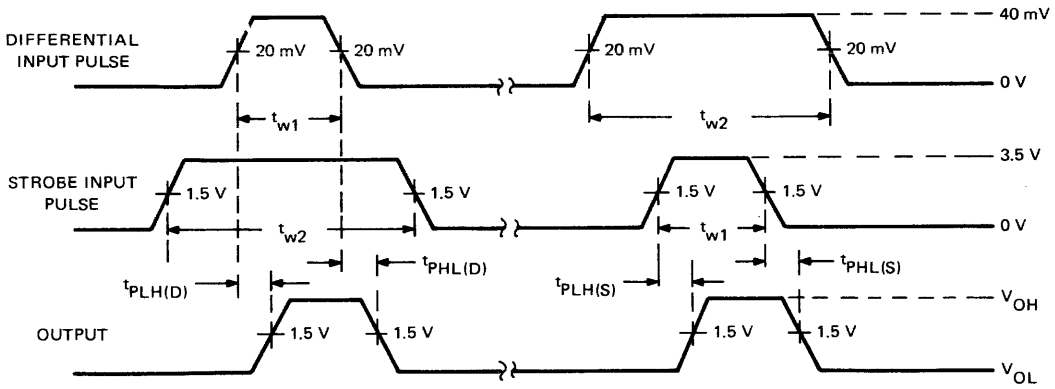
FIGURE 38–SN7526/SN7527 PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.

B. The strobe input pulse is applied to Strobe 1S when inputs 1A1-1A2 are being tested and to Strobe 2S when inputs 2A1-2S2 are being tested.

C. C_L includes probe and jig capacitance.

FIGURE 39—SN7528/SN7529 PROPAGATION DELAY TIMES

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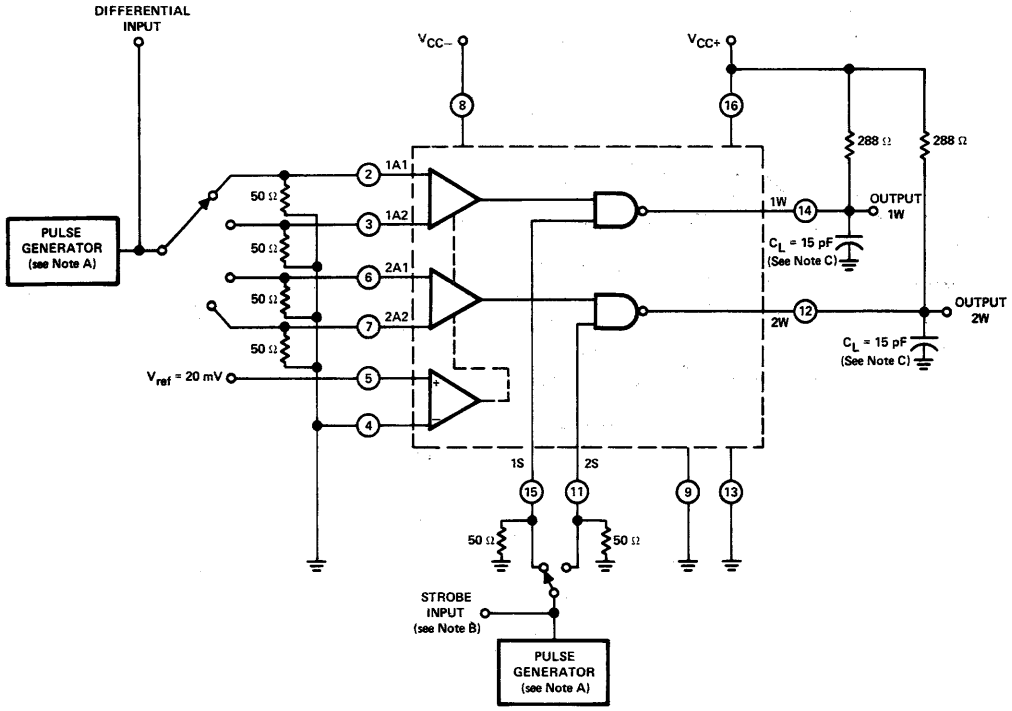
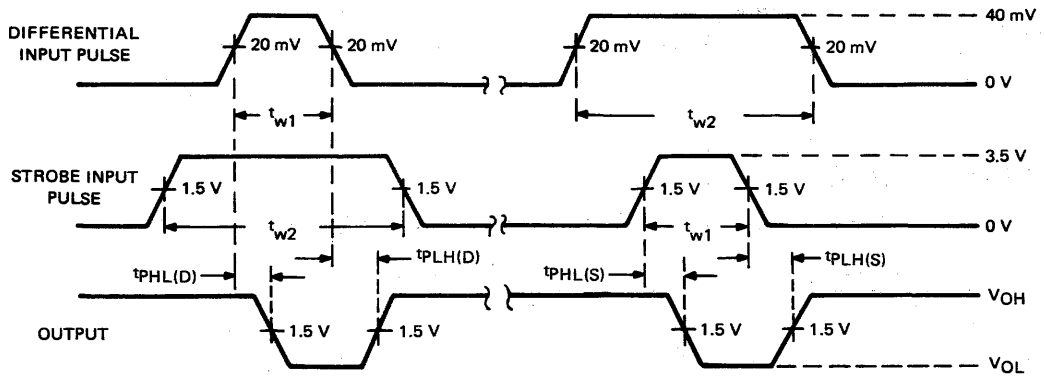
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.

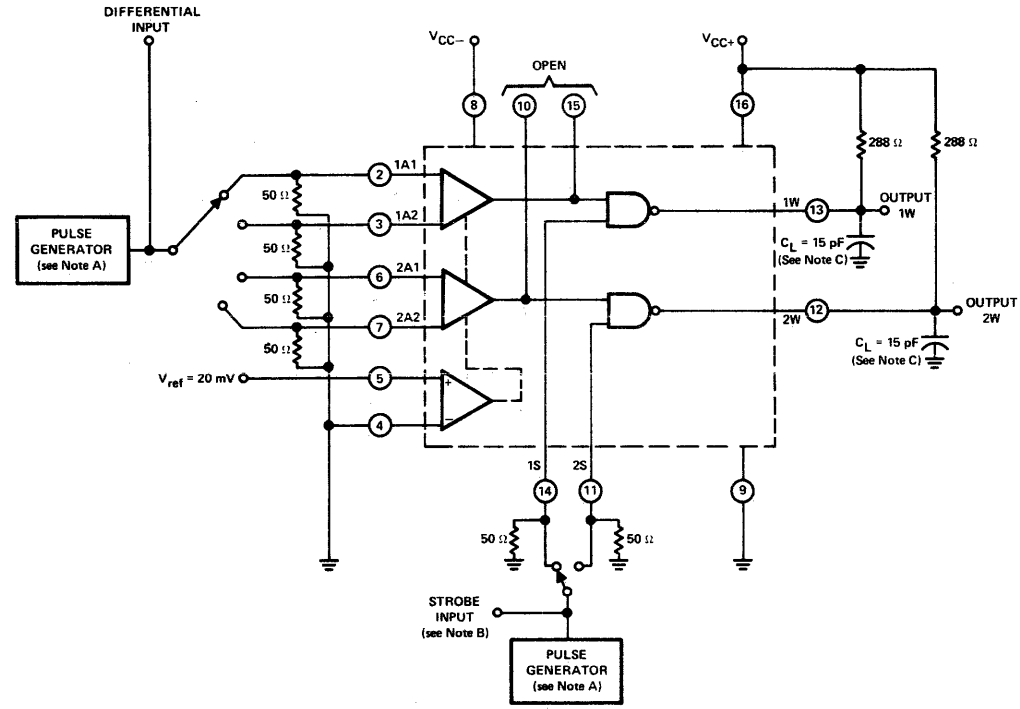
B. The strobe input pulse is applied to Strobe 1S when inputs 1A1-1A2 are being tested and to Strobe 2S when inputs 2A1-2A2 are being tested.

C. C_L includes probe and jig capacitance.

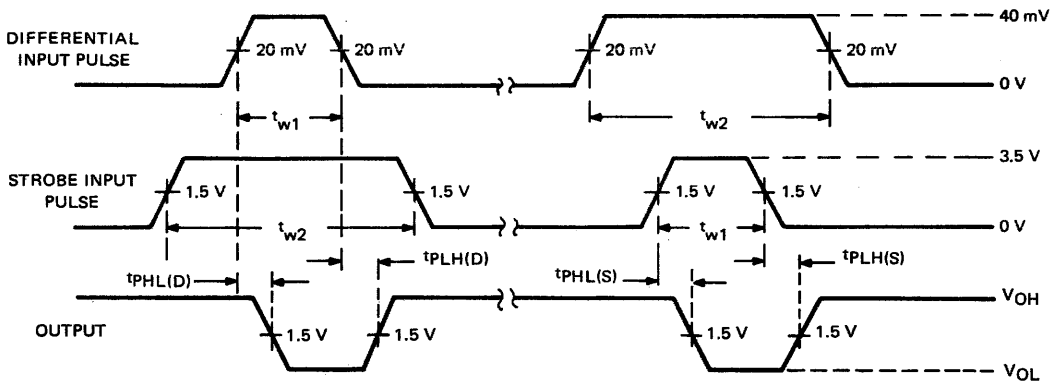
FIGURE 40–SN75234/SN75235 PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.

B. The strobe input pulse is applied to Strobe 1S when inputs 1A1-1A2 are being tested and to Strobe 2S when inputs 2A1-2S2 are being tested.

C. C_L includes probe and jig capacitance.

FIGURE 41–SN75238/SN75239 PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS

THRESHOLD VOLTAGE
vs
REFERENCE VOLTAGE

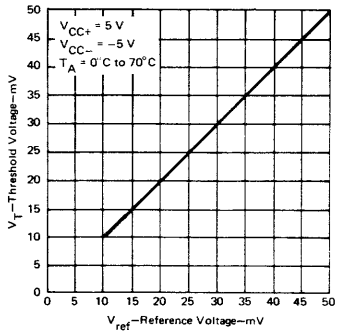


FIGURE 42

THRESHOLD VOLTAGE
vs
SUPPLY VOLTAGE

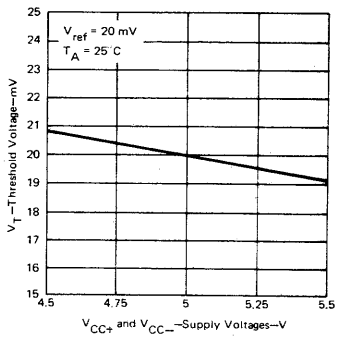


FIGURE 43

NORMALIZED THRESHOLD VOLTAGE
vs
PULSE REPETITION RATE

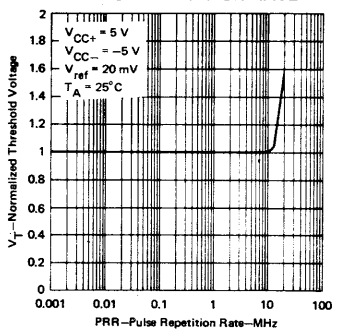


FIGURE 44

COMMON-MODE FIRING VOLTAGE
vs
FREE-AIR TEMPERATURE

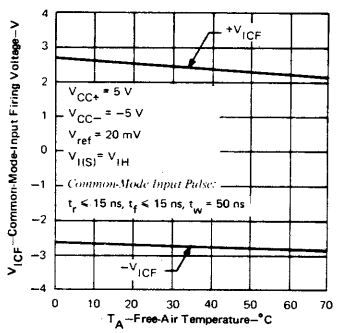


FIGURE 45

DIFFERENTIAL-INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

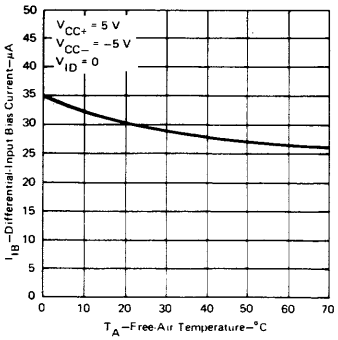


FIGURE 46

DIFFERENTIAL-INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

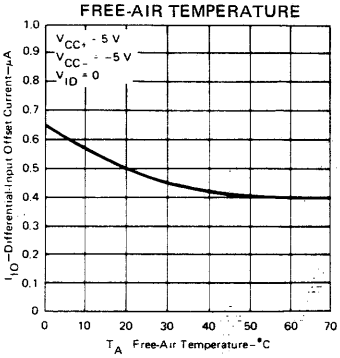


FIGURE 47

3

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TYPICAL CHARACTERISTICS

HIGH-LEVEL INPUT CURRENT
vs
INPUT VOLTAGE

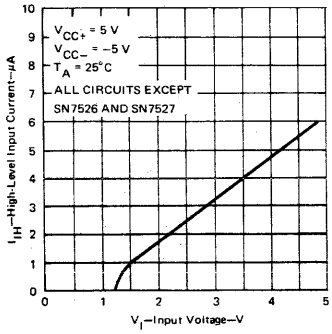

FIGURE 48

LOW-LEVEL INPUT CURRENT
vs
INPUT VOLTAGE

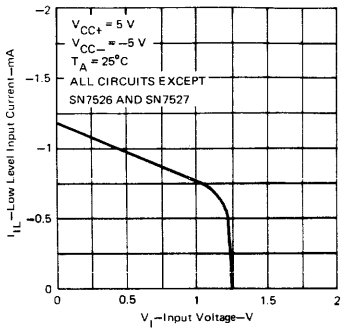

FIGURE 49

OUTPUT VOLTAGE
vs
DIFFERENTIAL-INPUT VOLTAGE

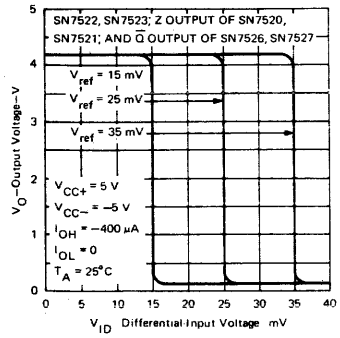

FIGURE 50

OUTPUT VOLTAGE
vs
DIFFERENTIAL-INPUT VOLTAGE

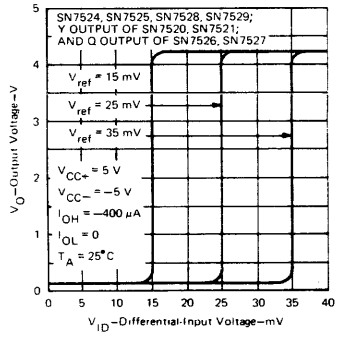

FIGURE 51

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

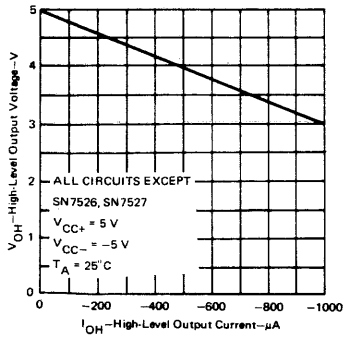

FIGURE 52

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

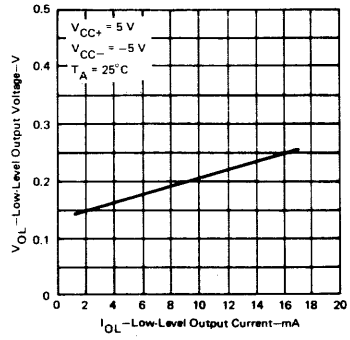

FIGURE 53

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TYPICAL APPLICATIONS

small memory systems

This application demonstrates an improved method of sensing data from relatively small memory systems. Two individual core planes, usually consisting of 4096 cores each, can be interfaced by each of the dual-channel SN7524 or SN7525 sense amplifiers, see Figure K. Standard TTL or DTL integrated circuits, driven directly from the compatible sense-amplifier outputs, may be selected to serve as the memory data register (MDR).

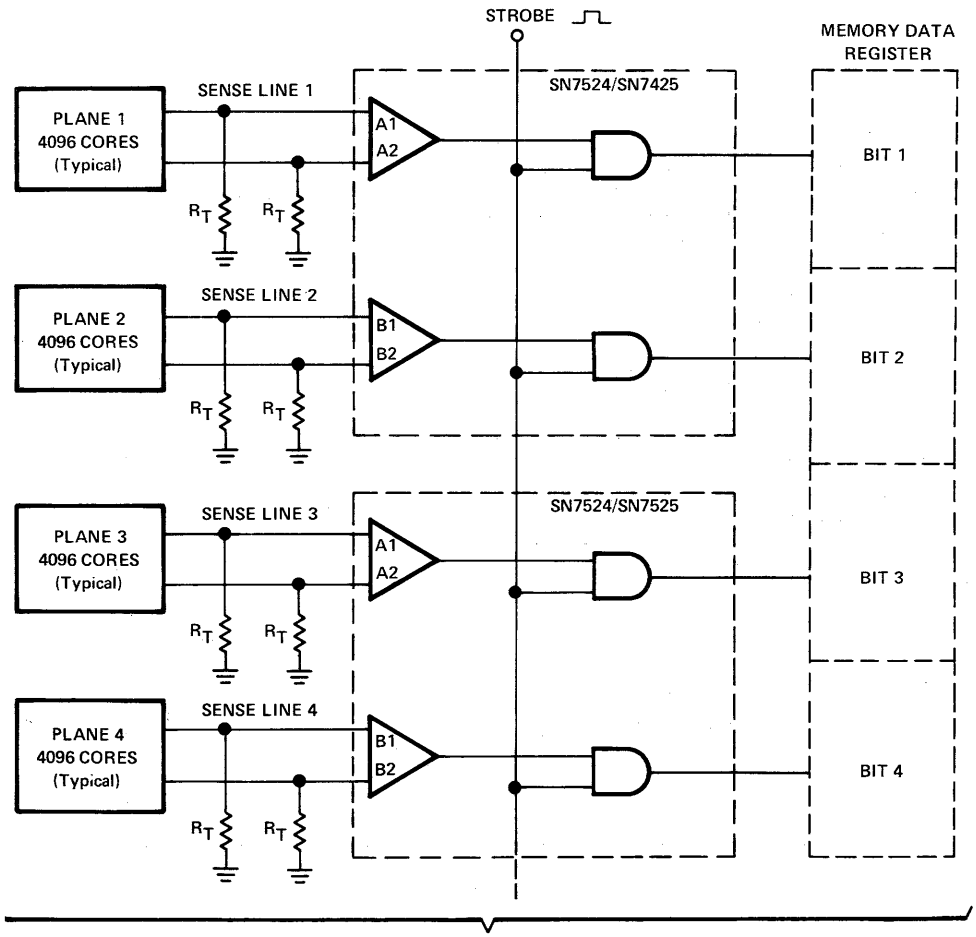

FIGURE K–SENSING SMALL MEMORY SYSTEMS

TYPICAL APPLICATIONS (continued)

large memory systems

This application demonstrates an improved method of sensing data from large memory systems. The signal-to-noise ratio can be increased by sectioning the large core planes as illustrated in Figure L. Two segments, usually consisting of 4096 cores each, can be interfaced by each of the dual-input channels of the SN7420/SN7421 or SN7422/SN7423 sense amplifiers. The cascaded output gates of the SN7520/SN7521 circuits may be connected to serve as the memory data register (MDR). A number of SN7522/SN7523 sense amplifiers may be wire-AND connected to expand the input function of the MDR to interface all the segments of the plane. Complementary outputs, clear, and preset functions are provided for the MDR. Rules for combined fan-out and wire-AND capabilities must be observed.

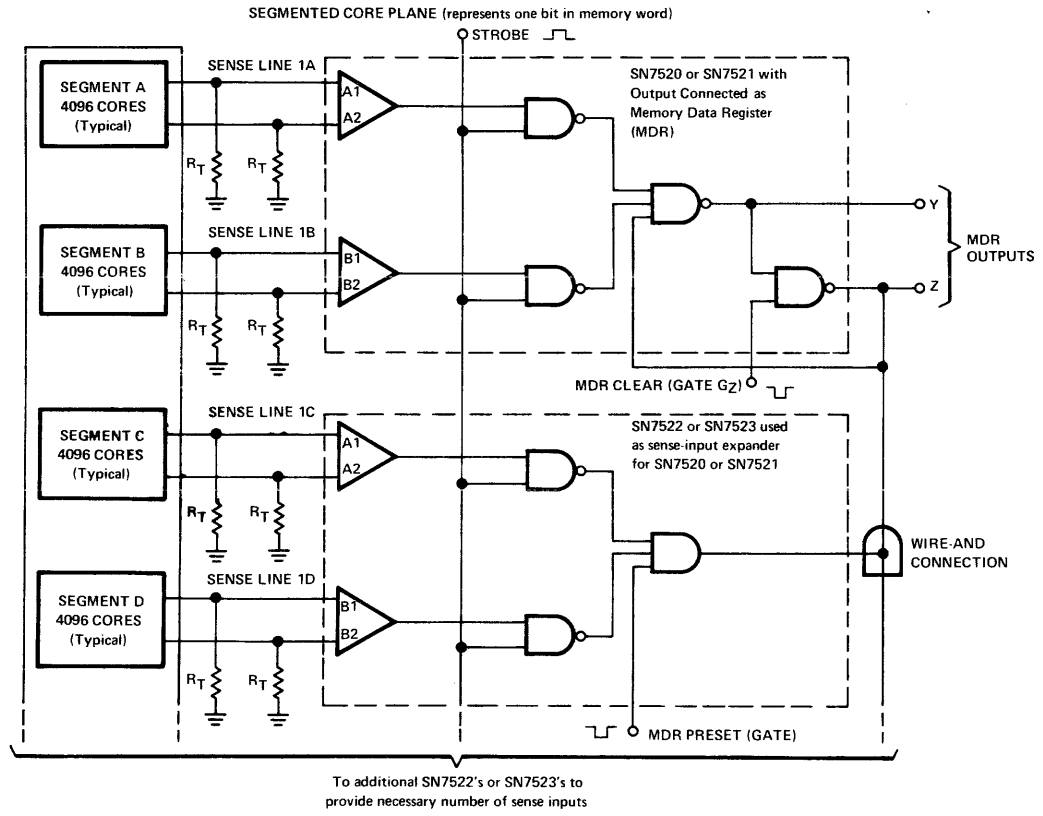

FIGURE L–SENSING LARGE MEMORY SYSTEMS

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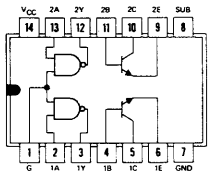
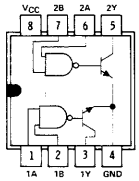
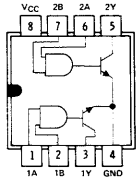
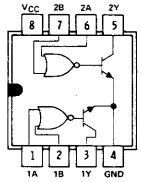
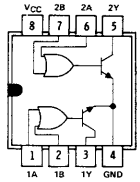
peripheral drivers

TYPE	SN75450A	SN75451A	SN75452	SN75453	SN75454
Block Diagrams		 Y = AB	 Y = $\overline{AB}$	 Y = A+B	 Y = $\overline{A+B}$
Features	Two TTL gates and two high current transistors on one chip. Each transistor sinks 300 mA of current and has a minimum collector-emitter breakdown voltage of 30 V.				
	• Two Uncommitted Transistors	• 8-pin Package	• AND Gates	• NOR Gates	• OR Gates
Applications	• Lamp Driver • Relay Driver • MOS Driver • Line Driver	• Lamp Driver • Relay Driver	• Lamp Driver • Relay Driver	• Lamp Driver • Relay Driver	• Lamp Driver • Relay Driver
Package	N	P	P	P	P

3

memory drivers

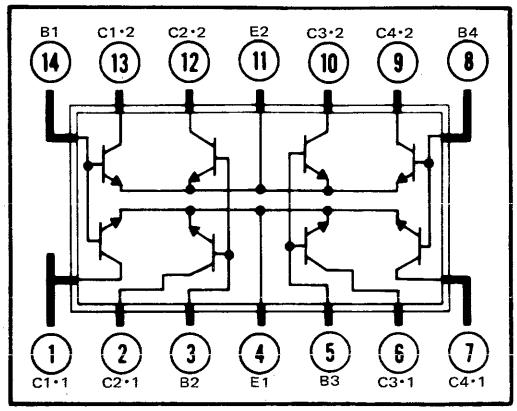
TYPE	SN75303 4 X 2 TRANSISTOR ARRAY	SN75308 2 X 4 TRANSISTOR ARRAY	SN75324 DRIVER WITH DECODE INPUTS	SN75325 DRIVER WITH DECODE INPUT
Features	• Eight 150-mA Monolithic Transistors • $V_{(BR)CBO}$ = 25 V Min • $V_{(BR)CEO}$ = 18 V Min • $V_{CE(sat)}$ = 0.75 V Max at I_C = 150 mA • t_{PHL} = 14 ns Typ • t_{PLH} = 18 ns Typ	• Eight 600-mA Monolithic Transistors • $V_{(BR)CBO}$ = 25 V Min • $V_{(BR)CEO}$ = 10 V Min • $V_{CE(sat)}$ = 0.55 V Typ at I_C = 500 mA • t_{on} = 36 ns Typ • t_{off} = 23 ns Typ	• Four 400-mA Transistors • TTL-Compatible Inputs • Internal Decoding and Timing Gates • Single 14-V Supply	• Four 600-mA Transistors • TTL-Compatible Inputs • Internal Decoding • 5-V Supply
Application	• Core Memories • Read-Only Memories	• Core Memories • Read-Only Memories • Plated-Wire Memories	• Core Memories	• Core Memories • Plated-Wire Memories • Hammer Driver
Package	N, S	J, N	N, S	J, N
Application Notes			CA-107: SN75324 Monolithic Memory Driver	

CIRCUIT TYPE SN75303
2 X 4 TRANSISTOR ARRAY

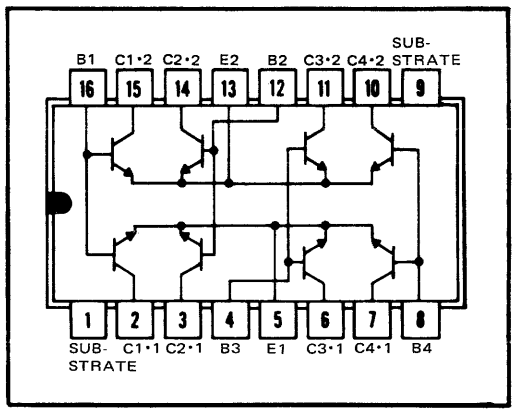
150-mA MEMORY DRIVER

- Maximum $V_{CE(sat)}$ of 750 mV at 150 mA I_C
- Maximum V_{BE} of 1.1 V at 150 mA I_C
- Minimum h_{FE} of 15 at 150 mA I_C

S FLAT PACKAGE (TOP VIEW)



N DUAL-IN-LINE PACKAGE (TOP VIEW)



3 description

Each SN75303 is a monolithic array of eight n-p-n transistors designed for use in core, thin-film, and plated-wire memories as a medium-current word-line driver. Selection is by base-emitter activation. The SN75303 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Collector-base voltage	25 V
Collector-emitter voltage (see Note 1)	18 V
Emitter-base voltage	5 V
Continuous collector current	200 mA
Continuous total package dissipation	250 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: This value applies when the base-emitter diode is open-circuited.

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electrical characteristics at 25°C free-air temperature (unless otherwise noted)†

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)CBO}$	Collector-base breakdown voltage	I_C = 10 μA,	I_E = 0		25			V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	I_C = 10 mA,	I_B = 0,	See Note 2	18			V
$V_{(BR)CES}$	Collector-emitter breakdown voltage	I_C = 1 mA,	V_{BE} = 0		25			V
$V_{(BR)EBO}$	Emitter-base breakdown voltage	I_E = 10 μA,	I_C = 0		5			V
h_{FE}	Static forward current transfer ratio	V_{CE} = 2 V,	I_C = 30 mA	See Note 2	20	35		
		V_{CE} = 2 V, T_A = 0°C	I_C = 30 mA,	See Note 2	15			
		V_{CE} = 2 V,	I_C = 150 mA	See Note 2	15	25		
V_{BE}	Base-emitter voltage	I_B = 3 mA,	I_C = 30 mA	See Note 2	0.7	0.8	0.9	V
		I_B = 3 mA, T_A = 0°C to 70°C	I_C = 30 mA,	See Note 2	0.65		0.95	V
		I_B = 15 mA,	I_C = 150 mA	See Note 2	0.8	1	1.1	V
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_B = 3 mA,	I_C = 30 mA	See Note 2		0.2	0.4	V
		I_B = 3 mA, T_A = 70°C	I_C = 30 mA,	See Note 2			0.45	V
		I_B = 15 mA,	I_C = 150 mA	See Note 2		0.5	0.75	V
C_{obo}	Common-base open-circuit output capacitance (1 transistor)	V_{CB} = 5 V, See Note 3	I_E = 0,	f = 140 kHz,		5		pF
C_{ibo}	Common-base open-circuit input capacitance (4 transistors in parallel)	V_{EB} = 0.5 V, See Note 4	I_C = 0,	f = 140 kHz,		40		pF

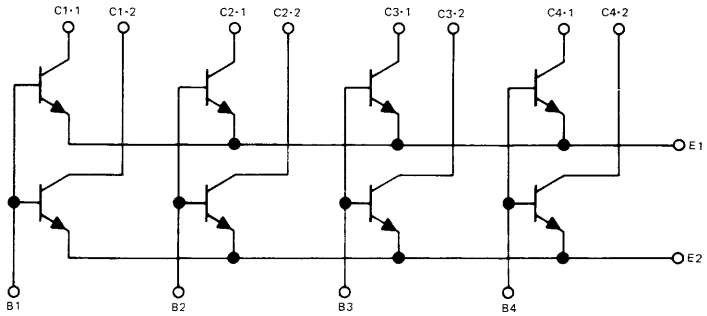
NOTES: 2. These parameters must be measured using pulse techniques, t_w = 300 μs, duty cycle ≤ 2%.
3. For measuring C_{obo}, the emitter of the transistor under test and all terminals of the other transistors are open.
4. For measuring C_{ibo}, the four base terminals are connected in parallel. The emitter terminal of the transistors not under test and all the collector terminals are open.

switching characteristics at 25°C free-air temperature†

PARAMETER		TEST CONDITIONS‡			MIN	TYP	MAX	UNIT
t_{THL}	Transition time, high-to-low-level output	I_C = 100 mA, $V_{BE(off)}$ = 0, C_L ≤ 15 pF,	$I_{B(1)}$ = 10 mA, R_L = 43 Ω, See Figure 1			8	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output					14	22	ns
t_{TLH}	Transition time, low-to-high-level output	I_C = 100 mA, $I_{B(2)}$ = −10 mA, C_L ≤ 15 pF,	$I_{B(1)}$ = 10 mA, R_L = 43 Ω, See Figure 2			6	12	ns
t_{PLH}	Propagation delay time, low-to-high-level output					18	30	ns

†Test conditions and limits apply separately to each transistor unless otherwise noted. The terminals of the transistors not under test are open during the measurement of these characteristics.
‡Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

schematic



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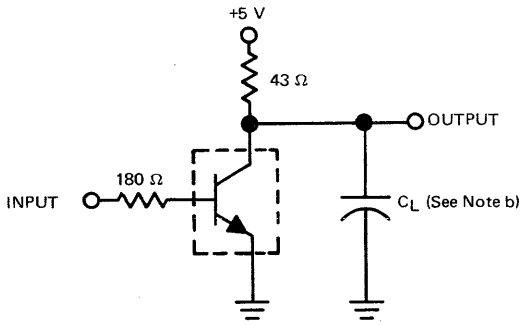
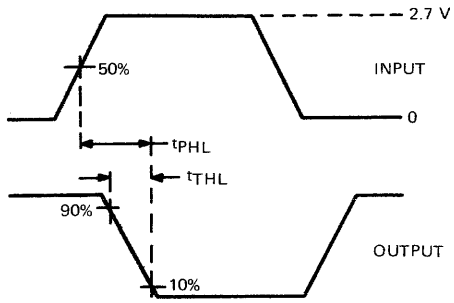
PARAMETER MEASUREMENT INFORMATION

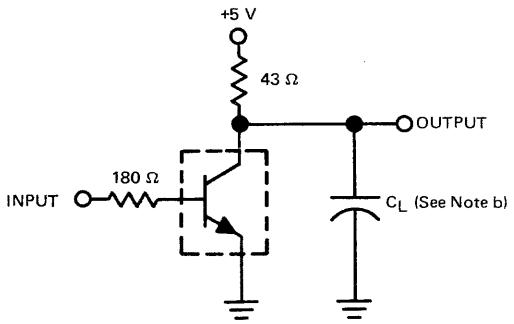


TEST CIRCUIT

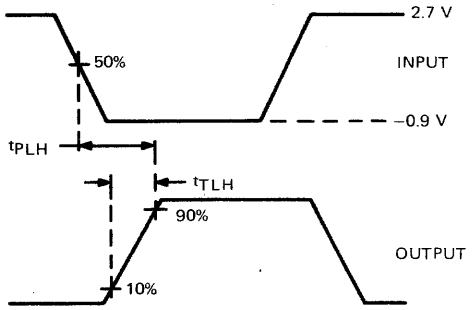


VOLTAGE WAVEFORMS

FIGURE 1–t_{THL} and t_{PHL}



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 2–t_{TLH} and t_{PLH}

NOTES: a. The input waveforms are supplied by a generator with the following characteristics: Z_{out} = 50 Ω, $t_r \leq$ 2 ns, $t_w \approx$ 70 ns, duty cycle ≤ 2%.
b. C_L includes probe and jig capacitance.

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TYPICAL CHARACTERISTICS

BASE-EMITTER VOLTAGE
vs
COLLECTOR CURRENT

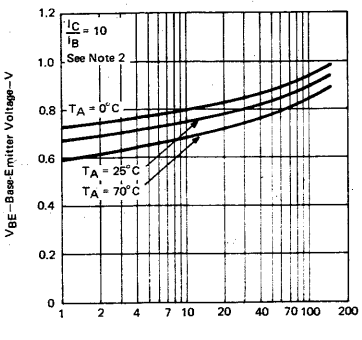

FIGURE 3

COLLECTOR-EMITTER SATURATION VOLTAGE
vs
COLLECTOR CURRENT

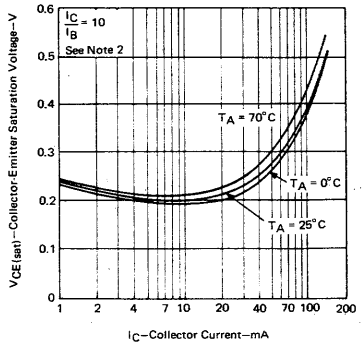

FIGURE 4

STATIC FORWARD
CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

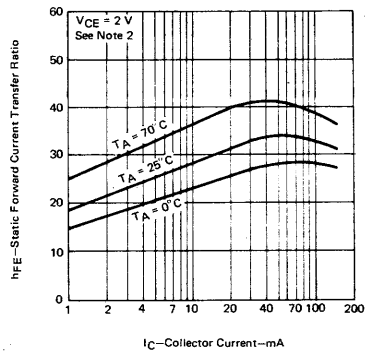

FIGURE 5

TURN-ON TIME
vs
FREE-AIR TEMPERATURE

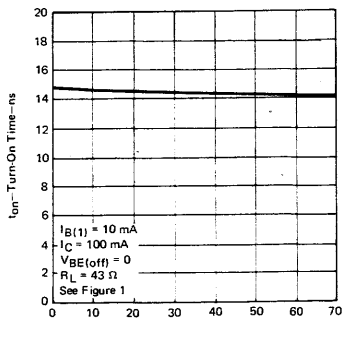

FIGURE 6

TURN-OFF TIME
vs
FREE-AIR TEMPERATURE

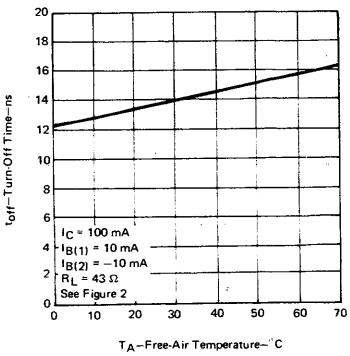

FIGURE 7

NOTE 2: These parameters must be measured using pulse techniques, t_w = 300 μs, duty cycle ≤ 2%.

TYPICAL APPLICATION DATA

Use of the SN75303 in High-Speed Read-Only Memories

Significant advantages result from the use of a high-speed, read-only memory (ROM) in computers and calculators. This ROM is used for control, as a function generator, or for performing highly repetitive routines such as multiplying, dividing , or calculating square roots. The read-only memory has permanently stored data and usually operates with a very fast cycle time. It can perform repetitive operations much more efficiently and faster than the larger and slower read-write memory in the computer or calculator.

The SN75303 two-by-four transistor array is designed to perform the word-line drive or select function for medium current, high-speed, read-only memories organized in the word-oriented (2D) or linear-select configuration. Such memories use magnetic memory elements such as plated wires, planar thin-films, transformers (as in a braided-wire memory), or ferrite switch cores. They also may utilize passive elements such as resistors, capacitors, or diodes. The typical organization of a word-oriented ROM is shown in the figure below.

3

Information is read from the ROM by selecting the desired word line. This is accomplished by appropriate activiation of one base-select and one emitter-select line. The transistor in the SN75303 array at the intersection of the selected base and emitter lines will be activated, thus sinking current from the word-line load resistor, R_L, connected to its collector. Energy is coupled from the selected word line to the sense lines by the memory elements (ME) located at the intersections of the word line and the sense lines. The presence of an ME can represent a stored logic 1 bit of information while the absence of an ME represents a stored logic 0 bit. (The desired information is stored in such a memory during fabrication and is not electrically alterable.)

The stored word is read out at the sense-amplifier outputs. The selection of a sense amplifier will depend on the type of ME used in the memory and may take the form of a special amplifier, a comparator, or a logic gate.

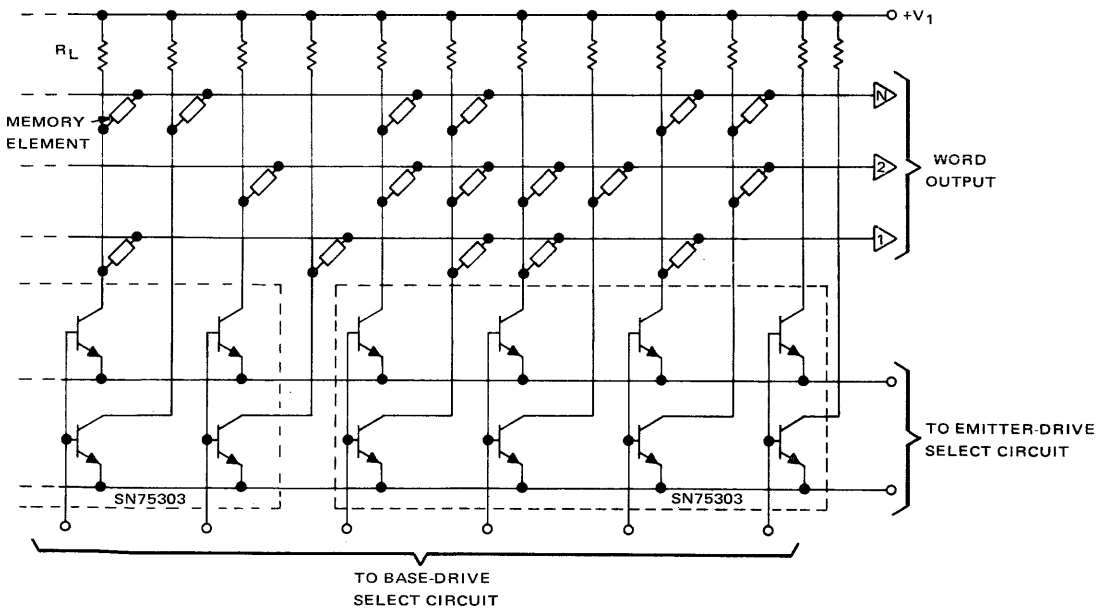

FIGURE 8

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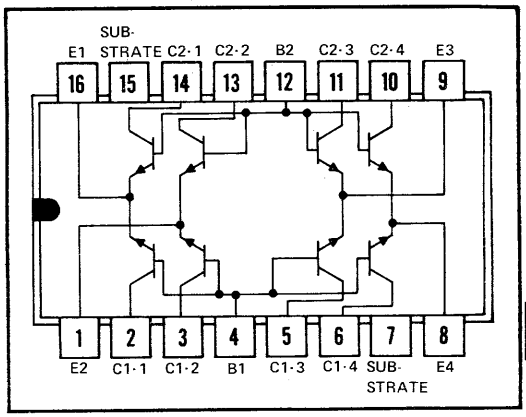
CIRCUIT TYPE SN75308
2 X 4 TRANSISTOR ARRAY

CIRCUIT TYPE SN75308
BULLETIN NO. DL-S 7111439, FEBRUARY 1971

- For High-Current Switching . . . to 600 mA Rated Collector Current
- Low Storage Time . . . 13 ns Typical
- Cross-Coupled Bases and Emitters Arranged for Selection

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The SN75308 is an array of eight high-current (600 mA max) n-p-n transistors designed for use in linear select (2D) memory designs utilizing ferrite cores, plated wire, planar film, diodes, resistors, or other memory elements. One of eight transistors can be switched by selection of the appropriate base and emitter inputs. Drive of the base and emitter inputs can be provided by available circuits such as the SN7440, SN75450, and SN75451. The SN75308 transistors feature fast switching times.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Collector-base voltage	25 V
Collector-emitter voltage (see Note 1)	25 V
Collector-emitter voltage (see Note 2)	10 V
Emitter-base voltage	4.5 V
Continuous current, each collector	600 mA
Continuous total package dissipation (see Note 3)	800 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. This value applies when the base-emitter diode is short-circuited.
2. This value applies between 100 μA and 10 mA collector current when the base-emitte diode is open-circuited.
3. This value applies for any combination provided the ratings of single transistors are not exceeded.

electrical characteristics for each transistor at 25°C free-air temperature†

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)CBO}$	Collector-base breakdown voltage	I_C = 100 μA,	I_E = 0		25			V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	I_C = 10 mA,	I_B = 0,	See Note 4	10			V
$V_{(BR)CES}$	Collector-emitter breakdown voltage	I_C = 100 μA,	V_{BE} = 0		25			V
$V_{(BR)EBO}$	Emitter-base breakdown voltage	I_E = 100 μA,	I_C = 0		5			V
$V_{(BR)CU}$	Collector-substrate breakdown voltage	I_C = 100 μA,	I_B = 0,	I_E = 0	25			V
h_{FE}	Static forward current transfer ratio	V_{CB} = 1 V,	I_E = 30 mA	See Note 4	15			
		V_{CB} = 1 V,	I_E = 100 mA		20			
		V_{CB} = 1 V,	I_E = 500 mA		20			
V_{BE}	Base-emitter voltage	I_B = 3 mA,	I_C = 30 mA	See Note 4		0.73	1	V
		I_B = 10 mA,	I_C = 100 mA			0.82	1.1	
		I_B = 30 mA,	I_C = 300 mA			1.0	1.2	
		I_B = 50 mA,	I_C = 500 mA			1.1	1.3	
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_B = 3 mA,	I_C = 30 mA	See Note 4		0.15	0.3	V
		I_B = 10 mA,	I_C = 100 mA			0.2	0.4	
		I_B = 30 mA,	I_C = 300 mA			0.36	0.6	
		I_B = 50 mA,	I_C = 500 mA			0.55	0.8	
$\lvert h_{fe} \rvert$	Small-signal common-emitter forward current transfer ratio	V_{CE} = 10 V,	I_C = 100 mA,	f = 100 MHz		2		
C_{obo}	Common-base open-circuit output capacitance (1 transistor)	V_{CB} = 10 V, See Note 5	I_E = 0,	f = 140 kHz,		18		pF
C_{ibo}	Common-base open-circuit input capacitance (2 transistors in parallel)	V_{EB} = 0.5 V, See Note 6	I_C = 0,	f = 140 kHz,		65		pF

NOTES: 4. These parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle ≤ 2%.
5. For measuring C_{obo}, the emitter terminal of the transistor under test and all terminals of the other transistors are open.
6. For measuring C_{ibo}, the base terminals are connected in parallel. The emitter terminals of the transistors not under test and all the collector terminals are open.

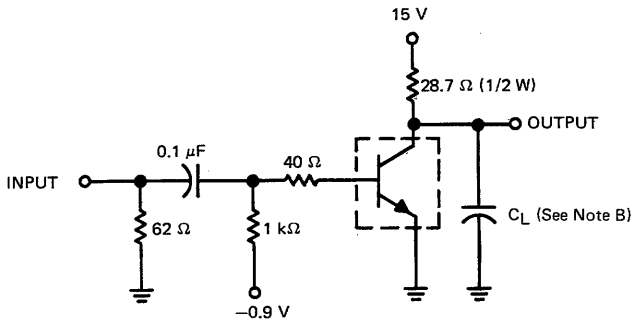
switching characteristics at 25°C free-air temperature†

PARAMETER		TEST CONDITIONS‡			TYP	UNIT
t_d	Delay time	I_C = 500 mA,	$I_{B(1)}$ = 50 mA,		16	ns
t_r	Rise time	$V_{BE(off)}$ = −0.9 V,	R_L = 28.7 Ω,		20	
t_{on}	Turn-on time	C_L = 15 pF,	See Figure 1		36	
t_s	Storage time	I_C = 500 mA,	$I_{B(1)}$ = 50 mA,		13	
t_f	Fall time	$I_{B(2)}$ = −50 mA,	R_L = 28.7 Ω,		10	
t_{off}	Turn-off time	C_L = 15 pF,	See Figure 1		23	

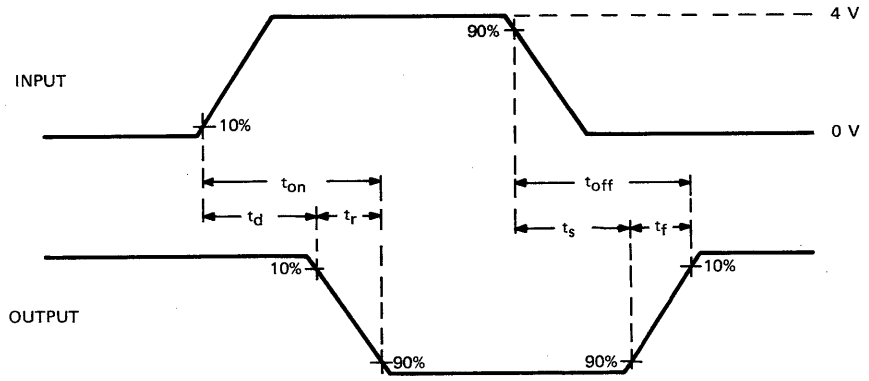
†Test conditions and limits apply separately to each transistor unless otherwise noted. The terminals of the transistors not under test are open during the measurement of these characteristics.

‡Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input waveform is supplied by a generator with the following characteristics: Z_{out} = 50 Ω, $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w \approx 100$ ns, duty cycle ≤ 2%.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING CHARACTERISTICS

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
vs
EMITTER CURRENT

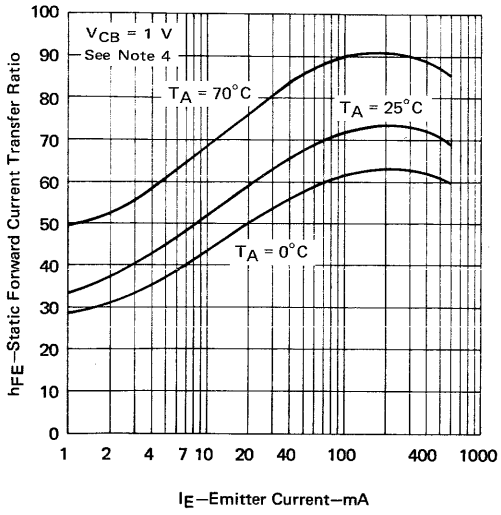


FIGURE 2

BASE-EMITTER VOLTAGE
vs
COLLECTOR CURRENT

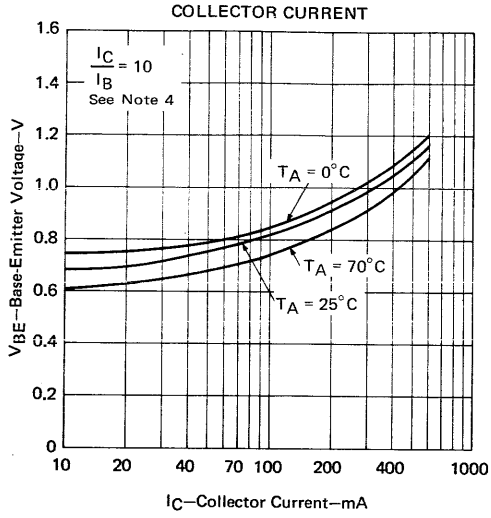


FIGURE 3

COLLECTOR-EMITTER SATURATION VOLTAGE
vs
COLLECTOR CURRENT

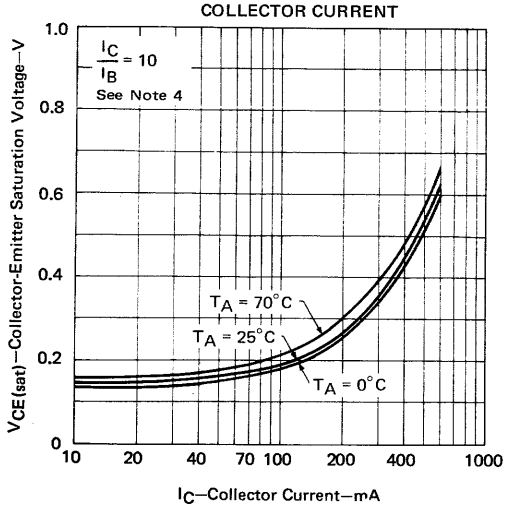


FIGURE 4

NORMALIZED COLLECTOR-EMITTER
BREAKDOWN VOLTAGE
vs
BASE-EMITTER RESISTANCE

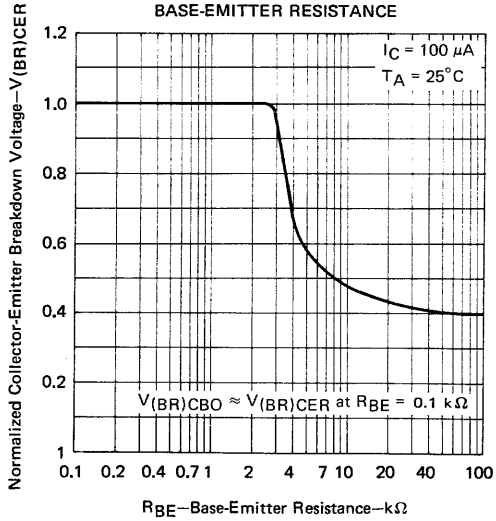


FIGURE 5

NOTE 4: These parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle ⩽ 2%.

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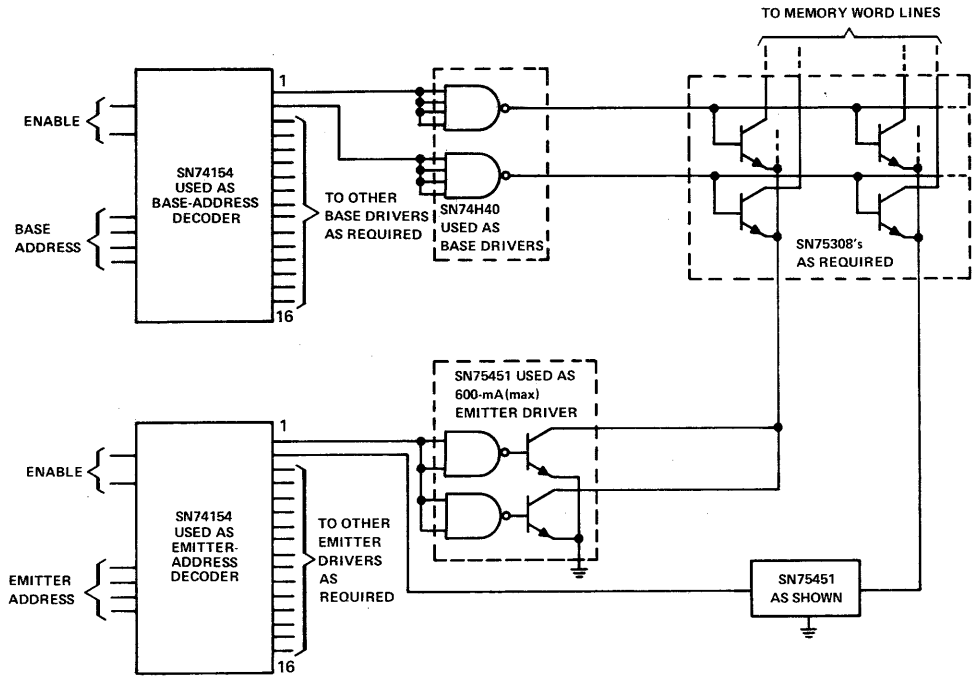
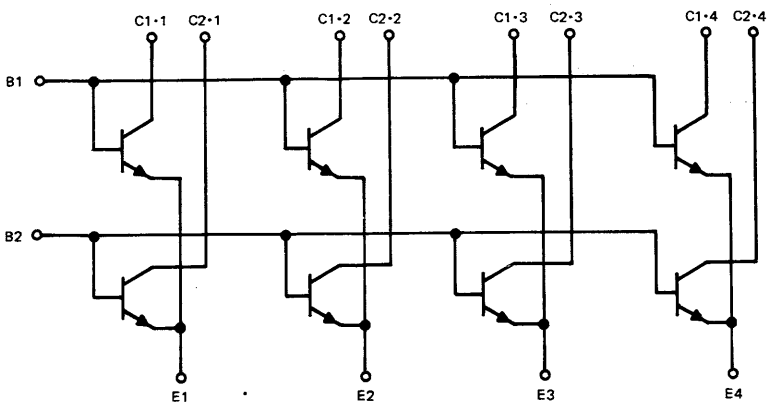
TYPICAL APPLICATION DATA

The SN75308 two-by-four transistor array is designed to perform the word-line drive or select function for medium current, high-speed, read-only memories organized in the word-oriented (2D) or linear-select configuration. Such memories use magnetic memory elements such as plated wires, planar thin-films, transformers (as in a braided-wire memory), or ferrite switch cores. They also may utilize passive elements such as resistors, capacitors, or diodes. The typical organization of a word-oriented ROM is shown on the SN75303 data sheet; a base and emitter selection technique is shown below. A similar selection circuit can be used with the SN75303 although with it the SN75451's need not be paralleled.



3

schematic



CIRCUIT TYPE SN75324
MEMORY DRIVER WITH DECODE INPUTS

SERIES 75 MEMORY DRIVER

PERFORMANCE

- fast switching times
- 400-mA output capability
- internal decoding and timing circuitry
- dual sink/source outputs
- output short-circuit protection

EASE OF DESIGN

- TTL or DTL compatibility
- eliminates transformer coupling
- reduces drive-line lengths
- increases reliability
- minimizes external components
- choice of flat or dual-in-line packages

description

The SN75324 is a monolithic memory driver with decode inputs designed for use with magnetic memories. The device contains two 400-milliampere (source/sink) switch pairs, with decoding capability from four address lines. Two address inputs (B and C) are used for mode selection, i.e., source or sink. The other two address inputs (A and D) are used for switch-pair selection, i.e., output switch-pair Y/Z or W/X respectively.

The sink circuit is composed of an inverting switch with a transistor-transistor-logic (TTL) input. The source circuit is an emitter-follower driven from a TTL input stage.

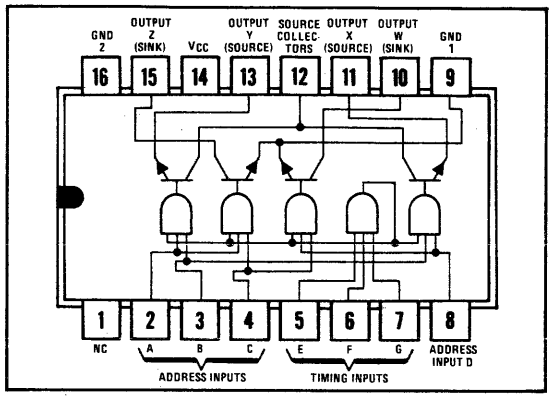
The SN75324 is characterized for operation from 0°C to 70°C.

TRUTH TABLE

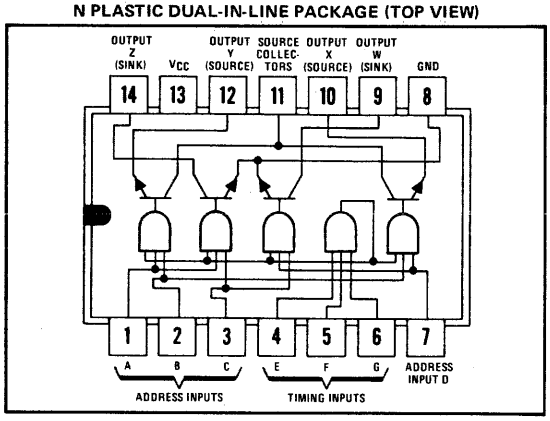
INPUTS							OUTPUTS			
ADDRESS				TIMING			SINK	SOURCES		SINK
A	B	C	D	E	F	G	W	X	Y	Z
0	0	1	1	1	1	1	ON	OFF	OFF	OFF
0	1	0	1	1	1	1	OFF	ON	OFF	OFF
1	1	0	0	1	1	1	OFF	OFF	ON	OFF
1	0	1	0	1	1	1	OFF	OFF	OFF	ON
X	X	X	X	0	X	X	OFF	OFF	OFF	OFF
X	X	X	X	X	0	X	OFF	OFF	OFF	OFF
X	X	X	X	X	X	0	OFF	OFF	OFF	OFF

NOTES: 1. X = Logical 1 or logical 0.
2. Not more than one output is to be allowed to be ON at one time: When all timing inputs are at a logical 1, two of the address inputs must be at a logical 0.

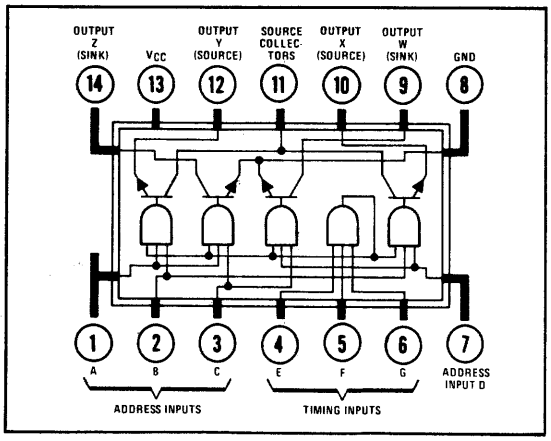
J CERAMIC DUAL-IN-LINE PACKAGE (TOP VIEW)



N PLASTIC DUAL-IN-LINE PACKAGE (TOP VIEW)



S FLAT PACKAGE (TOP VIEW)



NC—No internal connection
GND 1 and GND 2 are to be used in parallel

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logic definition

Standard positive logic applies with the following definitions used for specifying digital-level signals:

LOW VOLTAGE = LOGICAL 0
HIGH VOLTAGE = LOGICAL 1

absolute maximum ratings over operating case temperature range (unless otherwise noted)

Supply voltage V_{CC} (See Note 1) . . . . . 17 V
Input voltage (See Note 2) . . . . . 5.5 V
Operating case temperature range . . . . . 0°C to 70°C
Continuous total power dissipation at (or below) 70°C case temperature . . . . . 800 mW
Storage temperature range . . . . . -65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

3

electrical characteristics (unless otherwise noted, V_{CC} = 14 V, T_C = 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input	1		3.5			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input	1				0.8	V
$I_{in(1)}$	Logical 1 level address input current	1	V_{in} = 5 V			200	μA
$I_{in(1)}$	Logical 1 level timing input current	1	V_{in} = 5 V			100	μA
$I_{in(0)}$	Logical 0 level address input current	1	V_{in} = 0 V			-6	mA
$I_{in(0)}$	Logical 0 level timing input current	1	V_{in} = 0 V			-12	mA
$V_{(sat)}$	Sink saturation voltage	2	$I_{sink} \simeq$ 420 mA, R_L = 53 Ω		0.75	0.85	V
$V_{(sat)}$	Source saturation voltage	2	$I_{source} \simeq$ -420 mA, R_L = 47.5 Ω		0.75	0.85	V
I_{off}	Output reverse current (off state)	1	V_{in} = 0 V		125	200	μA
I_{CC}	Supply current, all sources and sinks off	3	V_{in} = 0 V		12.5	15	mA
I_{CC}	Supply current, either sink selected	4			30	40	mA
I_{CC}	Supply current, either source selected	4			25	35	mA

†These typical values are at T_C = 25°C.

switching characteristics, V_{CC} = 14 V, T_C = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd(1)}$	Propagation delay time to logical 1 level, source output	5	R_{L1} = 53 Ω, R_{L2} = 500 Ω, C_L = 20 pF			90	ns
$t_{pd(0)}$	Propagation delay time to logical 0 level, source output	5				50	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level, sink output	6	R_L = 53 Ω, C_L = 20 pF			110	ns
$t_{pd(0)}$	Propagation delay time to logical 0 level, sink output	6				40	ns
t_s	Sink storage time	6				70	ns

3

thermal information

The SN75324 is designed to be used at a case temperature not to exceed 70°C. Under this condition, infrared microradiometer and X-ray studies indicate that a safe junction temperature is maintained under specified worst-case conditions.

SN75324 circuits should be mounted so that minimum thermal resistance is achieved. A thermal compound should be used between the bottom of the flat S package and a heat sink. This, in conjunction with unrestricted forced-air flow across the heat sink and package, has been found to adequately satisfy thermal requirements. No thermal compound is required with the dual-in-line package. Air flow should be across the short dimension of either package.

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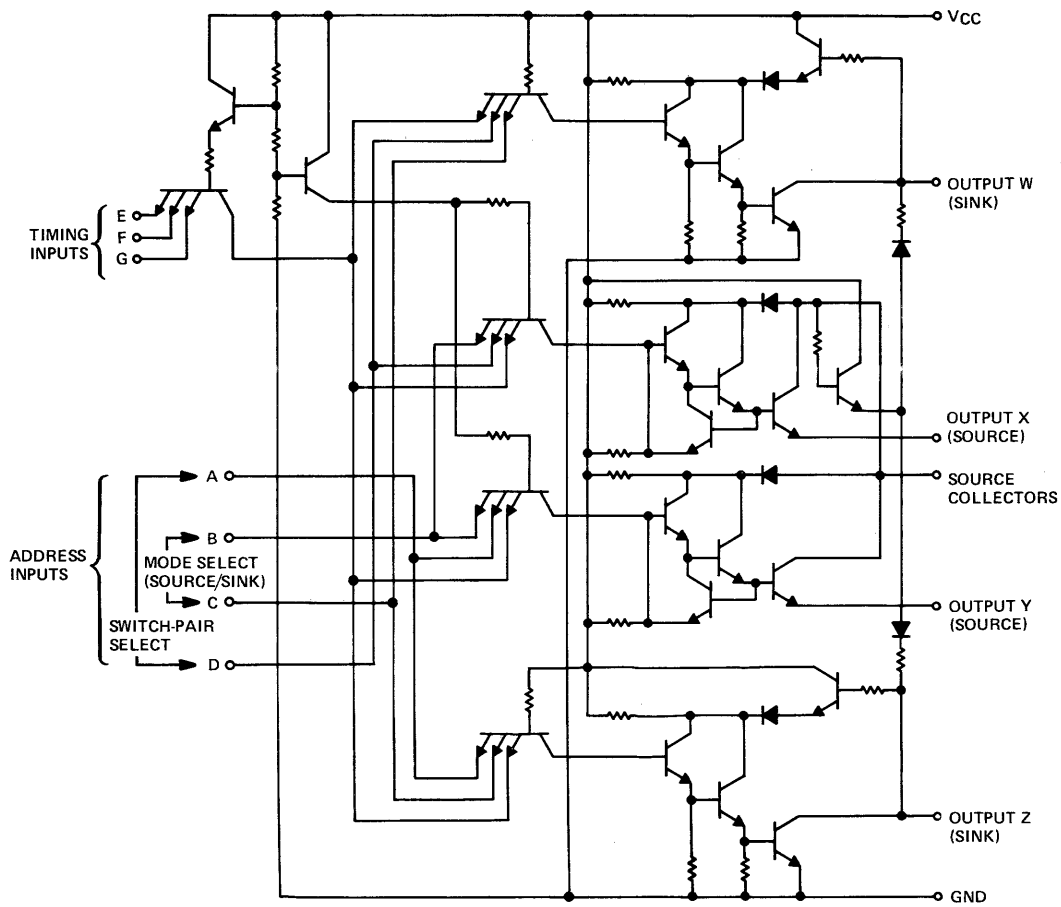
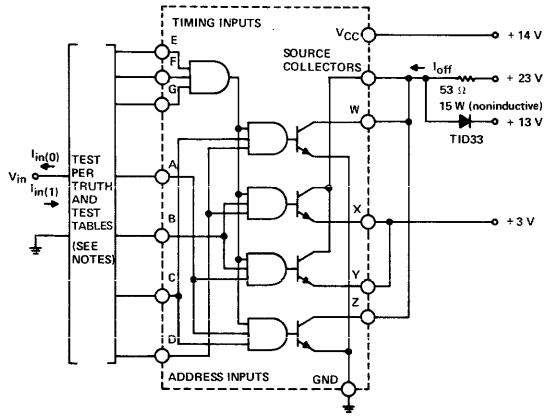
schematic


VCC
OUTPUT W
(SINK)
TIMING
INPUTS
E
F
G
OUTPUT X
(SOURCE)
SOURCE
COLLECTORS
A
B
C
D
ADDRESS
INPUTS
MODE SELECT
(SOURCE/SINK)
SWITCH-PAIR
SELECT
OUTPUT Y
(SOURCE)
OUTPUT Z
(SINK)
GND

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

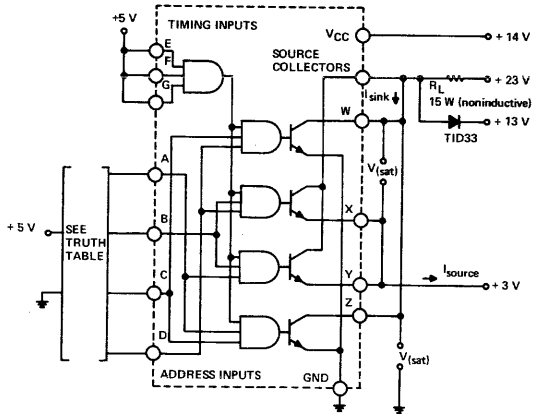


TEST TABLE FOR $I_{in(0)}$

APPLY 3.5 V	GROUND	TEST $I_{in(0)}$
B, C, E, F, and G	A and D	A
B, C, E, F, and G	A and D	D
A, D, E, F, and G	B and C	B
A, D, E, F, and G	B and C	C
A, B, C, D, F, and G	E	E
A, B, C, D, E, and G	F	F
A, B, C, D, E, and F	G	G

NOTES: 1. Check $V_{in(1)}$ and $V_{in(0)}$ per Truth Table.
2. Measure $I_{in(0)}$ per Test Table.
3. When measuring $I_{in(1)}$, all other inputs are at ground. Each input is tested separately.

FIGURE 1 – $V_{in(0)}$, $V_{in(1)}$, $I_{in(0)}$, $I_{in(1)}$, and I_{off}



NOTE: This parameter must be measured using pulse techniques. t_p = 500 ns, duty cycle ⩽ 1%.

FIGURE 2 – $V_{(sat)}$

† Arrows indicate actual direction of current flow.

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PARAMETER MEASUREMENT INFORMATION

d-c test circuits † (continued)

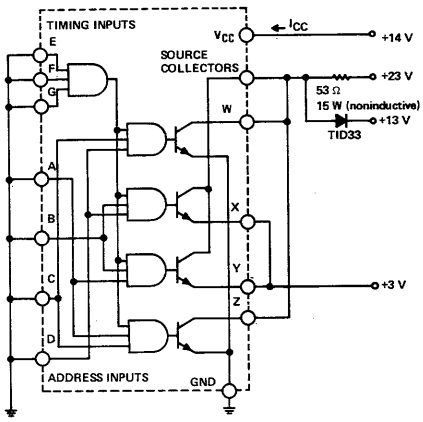
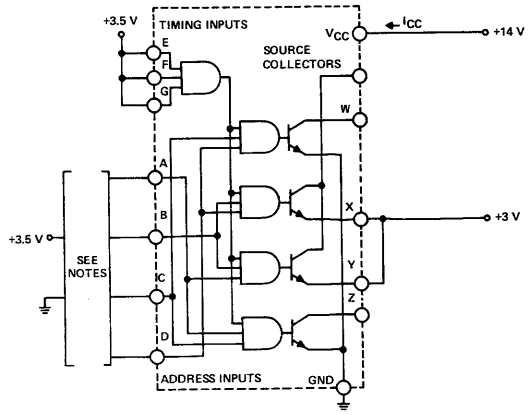


FIGURE 3 – I_{CC} (ALL OUTPUTS OFF)



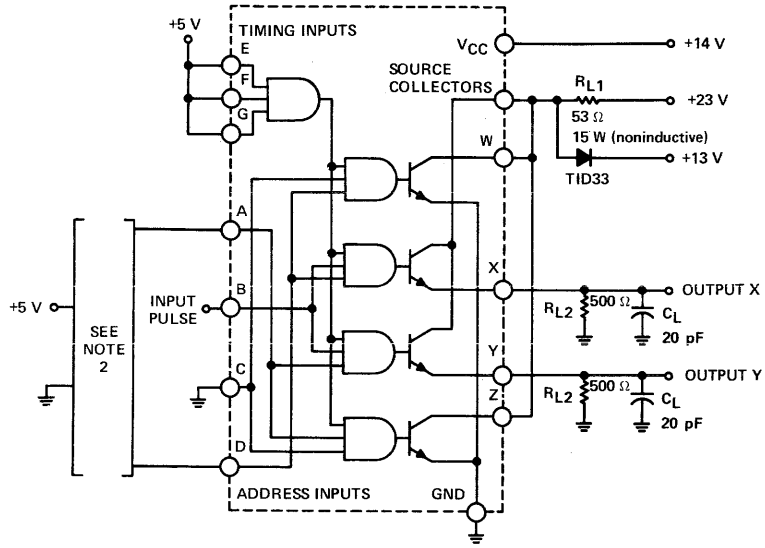
NOTES: 1. Ground A and B, apply 3.5 V to C and D, and measure I_{CC} (output W is on).
2. Ground B and D, apply 3.5 V to A and C, and measure I_{CC} (output Z is on).
3. Ground A and C, apply 3.5 V to B and D, and measure I_{CC} (output X is on).
4. Ground C and D, apply 3.5 V to A and B, and measure I_{CC} (output Y is on).

FIGURE 4 – I_{CC} (ONE OUTPUT ON)

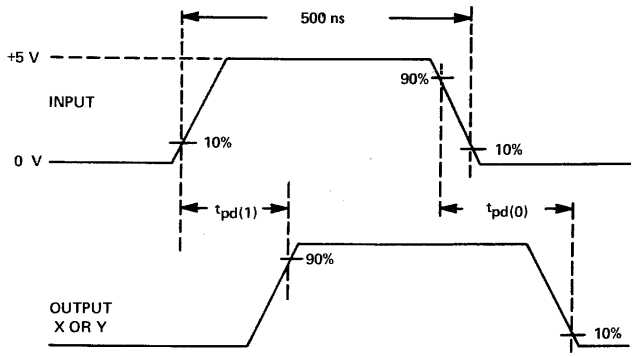
† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST TABLE



VOLTAGE WAVEFORMS

NOTES: 1. The input waveform is supplied by a generator with the following characteristics: $t_r = t_f = 10$ ns, duty cycle $\leqslant 1\%$, and $Z_{out} \approx 50\ \Omega$.
2. When measuring delay times at output X, apply +5 V to input D, and ground A. When measuring delay times at output Y, apply +5 V to input A, and ground D.
3. C_L includes probe and jig capacitance.
4. Unless otherwise noted all resistors are 0.5 W.

FIGURE 5 — SOURCE-OUTPUT SWITCHING TIMES

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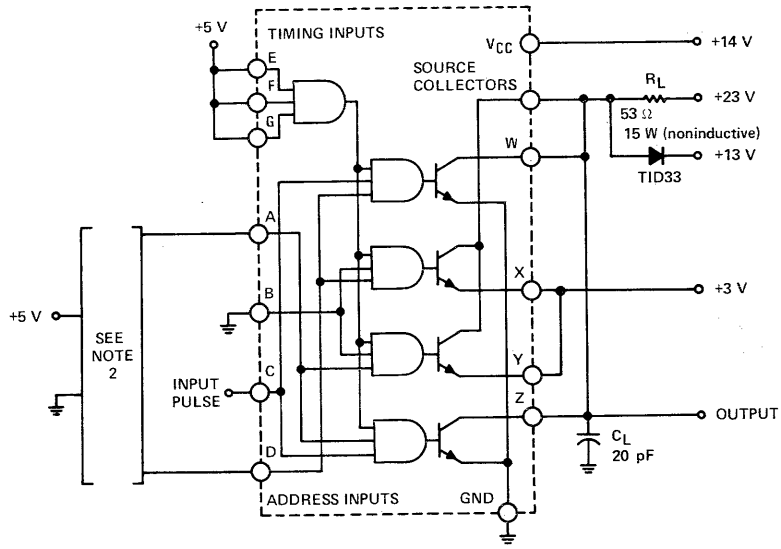
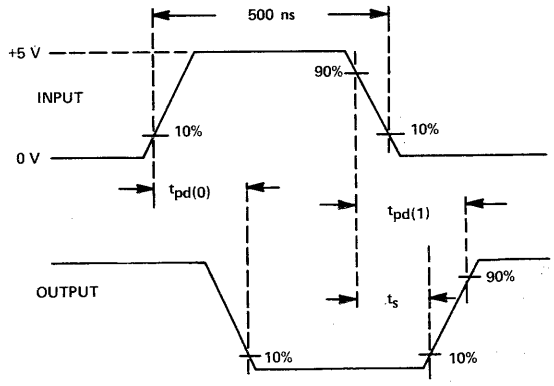
PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The input waveform is supplied by a generator with the following characteristics: $t_r = t_f = 10$ ns, duty cycle $\leq 1\%$, $Z_{out} \approx 50\ \Omega$.
2. When measuring delay times at output W, apply +5 V to input D, and ground A. When measuring delay times at output Z, apply +5 V to input A, and ground D.
3. C_L includes probe and jig capacitance.

FIGURE 6 – SINK-OUTPUT SWITCHING TIMES

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CIRCUIT TYPES SN55325, SN75325
MEMORY DRIVERS

SERIES 55/75 MEMORY DRIVER
featuring

PERFORMANCE

- 600-mA Output Capability
- Fast Switching Times
- Output Short-Circuit Protection
- Dual Sink and Dual Source Outputs
- Minimum Time Skew between Address and Output Current Rise
- 24-Volt Output Capability

EASE OF DESIGN

- Source Base Drive Externally Adjustable
- TTL or DTL Compatibility
- Input Clamping Diodes
- Transformer Coupling Eliminated
- Reliability Increased
- Drive-Line Lengths Reduced
- Use of External Components Minimized

3

description

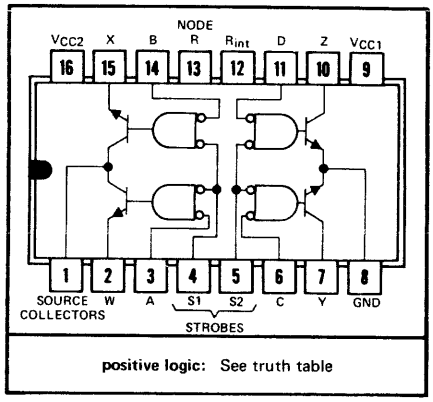
The SN55325 and SN75325 are monolithic integrated circuit memory drivers with logic inputs and are designed for use with magnetic memories.

The devices contain two 600-milliampere source-switch pairs and two 600-milliampere sink-switch pairs. Source selection is determined by one of two logic inputs, and source turn-on is determined by the source strobe. Likewise, sink selection is determined by one of two logic inputs, and sink turn-on is determined by the sink strobe. This arrangement allows selection of one of the four switches and its subsequent turn-on with minimum time skew of the output current rise.

When R_{int} and node R are connected together, the amount of base drive available for the source-1 or source-2 output transistor is set internally by a 575-ohm resistor. This method provides adequate base drive for source currents up to 375 mA with a V_{CC2} voltage of 15 volts or 600 mA with a V_{CC2} voltage of 24 volts.

When source currents greater than 375 mA are required, it is recommended that a resistor of the appropriate value be connected between V_{CC2} and node R and R_{int} must remain open. By using this method the source base current may usually be regulated within ±5%. An advantage of this method of setting the base drive is that the power dissipated by this resistor is external to the package and allows the integrated circuit to operate at higher source currents for a given junction temperature.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



TRUTH TABLE

ADDRESS INPUTS				STROBE INPUTS		OUTPUTS			
SOURCE		SINK		SOURCE	SINK	SOURCE		SINK	
A	B	C	D	S1	S2	W	X	Y	Z
L	H	X	X	L	H	ON	OFF	OFF	OFF
H	L	X	X	L	H	OFF	ON	OFF	OFF
X	X	L	H	H	L	OFF	OFF	ON	OFF
X	X	H	L	H	L	OFF	OFF	OFF	ON
X	X	X	X	H	H	OFF	OFF	OFF	OFF
H	H	H	H	X	X	OFF	OFF	OFF	OFF

H = high level, L = low level, X = irrelevant
NOTE: Not more than one output is to be on at any one time.

Each sink-output collector has an internal pull-up resistor in parallel with a clamping diode connected to V_{CC2}. This arrangement provides protection from voltage surges associated with switching inductive loads.

The SN55325 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN75325 is characterized for operation from 0°C to 70°C.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN55325	SN75325	UNIT
Supply voltage V_{CC1} (see Note 1)		7	7	V
Supply voltage V_{CC2} (see Note 1)		25	25	V
Input voltage (any address or strobe input)		5.5	5.5	V
Continuous total dissipation at (or below) 70°C free-air temperature (see Note 2)		800	800	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N Package	260	260	°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation of SN55325 above 70°C free-air temperature, refer to Dissipation Derating Curve, Figure 20.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

3

PARAMETER			TEST FIGURE	TEST CONDITIONS		SN55325 MIN	SN55325 TYP†	SN55325 MAX	SN75325 MIN	SN75325 TYP†	SN75325 MAX	UNIT
V_{IH}	High-level input voltage		1 & 2			2			2			V
V_{IL}	Low-level input voltage		3 & 4					0.8			0.8	V
V_I	Input clamp voltage		5	V_{CC1} = 4.5 V, I_I = −10 mA,	V_{CC2} = 24 V, T_A = 25°C		−1.3	−1.7		−1.3	−1.7	V
$I_{(off)}$	Source-collectors terminal off-state current		1	V_{CC1} = 4.5 V, V_{CC2} = 24 V	Full range			500			200	μA
					T_A = 25°C		3	150		3	200	
V_{OH}	High-level sink output voltage		2	V_{CC1} = 4.5 V, I_O = 0	V_{CC2} = 24 V,	19	23		19	23		V
$V_{(sat)}$	Saturation voltage‡	Source outputs	3	V_{CC1} = 4.5 V, V_{CC2} = 15 V, R_L = 24 Ω, $I_{(source)}$ ≈ −600 mA, See Note 3	Full range			0.9			0.9	V
					T_A = 25°C		0.43	0.7		0.43	0.75	
		Sink outputs	4	V_{CC1} = 4.5 V, V_{CC2} = 15 V, R_L = 24 Ω, $I_{(sink)}$ ≈ 600 mA, See Note 3	Full range			0.9			0.9	
					T_A = 25°C		0.43	0.7		0.43	0.75	
I_I	Input current at maximum input voltage	address inputs	5	V_{CC1} = 5.5 V, V_I = 5.5 V	V_{CC2} = 24 V,			1			1	mA
		strobe inputs						2			2	
I_{IH}	High-level input current	address inputs	5	V_{CC1} = 5.5 V, V_I = 2.4 V	V_{CC2} = 24 V,		3	40		3	40	μA
		strobe inputs					6	80		6	80	
I_{IL}	Low-level input current	address inputs	5	V_{CC1} = 5.5 V, V_I = 0.4 V	V_{CC2} = 24 V,		−1	−1.6		−1	−1.6	mA
		strobe inputs					−2	−3.2		−2	−3.2	
$I_{CC(off)}$	Supply current, all sources and sinks off	from V_{CC1}	6	V_{CC1} = 5.5 V, T_A = 25°C	V_{CC2} = 24 V,		14	22		14	22	mA
		from V_{CC2}					7.5	20		7.5	20	
I_{CC1}	Supply current from V_{CC1}, either sink on		7	V_{CC1} = 5.5 V, $I_{(sink)}$ = 50 mA,	V_{CC2} = 24 V, T_A = 25°C		55	70		55	70	mA
I_{CC2}	Supply current from V_{CC2}, either source on		8	V_{CC1} = 5.5 V, $I_{(source)}$ = −50 mA,	V_{CC2} = 24 V, T_A = 25°C		32	50		32	50	mA

†All typical values are at T_A = 25°C.
‡Not more than one output is to be on at any one time.
NOTE 3: These parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle ≤ 2%.

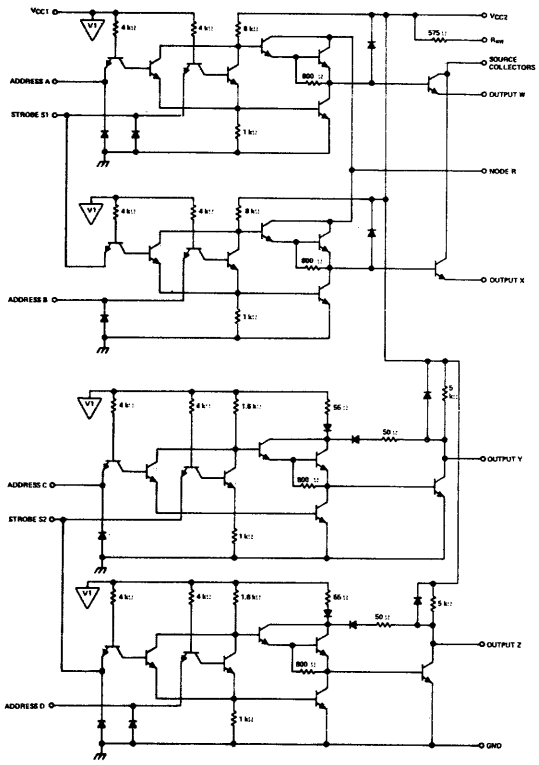
switching characteristics, V_{CC1} = 5 V, T_A = 25°C

PARAMETER¶	TO (OUTPUT)	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Source collectors	9	V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF		25	50	ns
t_{PHL}					25	50	
t_{TLH}	Source outputs	10	V_{CC2} = 20 V, R_L = 1 kΩ, C_L = 25 pF		55		ns
t_{THL}					7		
t_{PLH}	Sink outputs	9	V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF		20	45	ns
t_{PHL}					20	45	
t_{TLH}	Sink outputs	9	V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF		7	15	ns
t_{THL}					9	20	
t_s	Sink outputs	9	V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF		15	30	ns

3

¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{TLH} = transition time, low-to-high-level output
t_{THL} = transition time, high-to-low-level output
t_s = storage time

schematic



Component values shown are nominal.
V1 . . . V_{CC} bus

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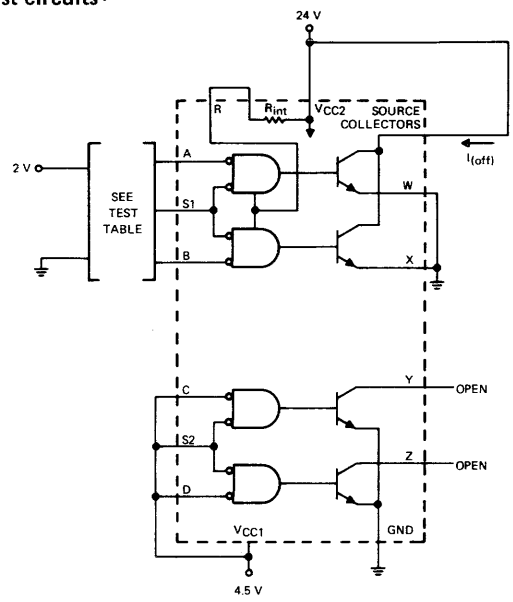
PARAMETER MEASUREMENT INFORMATION

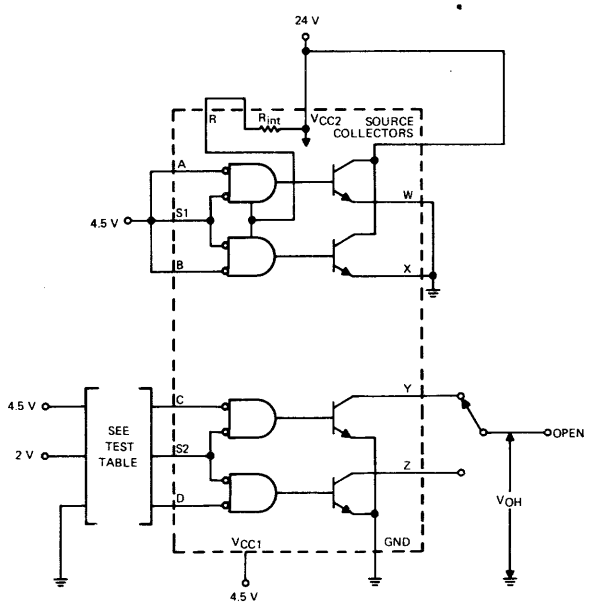
d-c test circuits†



TEST TABLE

A	B	S1
GND	GND	2 V
2 V	2 V	GND

FIGURE 1–$I_{(off)}$



TEST TABLE

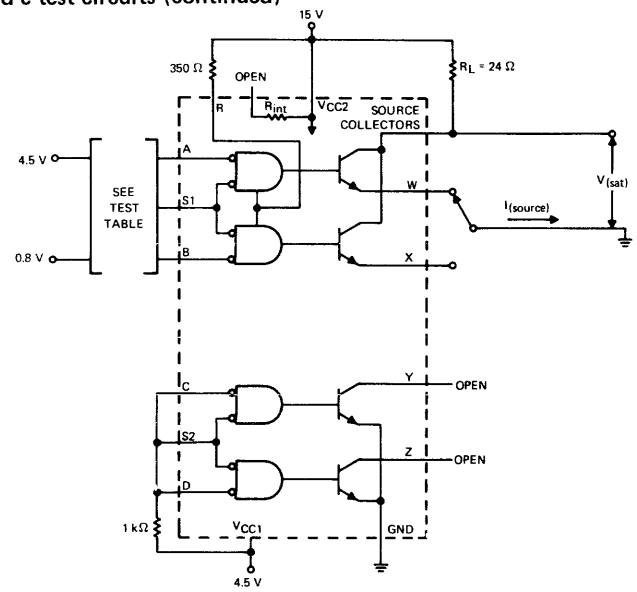
C	D	S2	Y	Z
2 V	4.5 V	GND	V_{OH}	OPEN
GND	4.5 V	2 V	V_{OH}	OPEN
4.5 V	2 V	GND	OPEN	V_{OH}
4.5 V	GND	2 V	OPEN	V_{OH}

FIGURE 2–V_{IH} AND V_{OH}

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits (continued)†

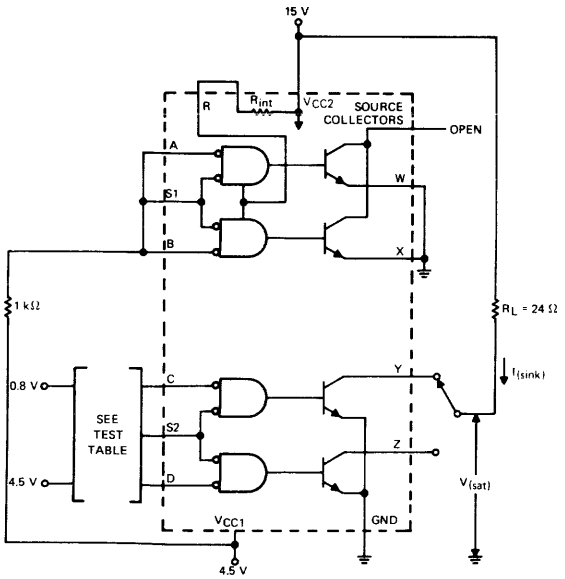


TEST TABLE

A	B	S1	W	X
0.8 V	4.5 V	0.8 V	GND	OPEN
4.5 V	0.8 V	0.8 V	OPEN	GND

NOTE A: These parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle ⩽ 2%.

FIGURE 3–V_{IL} AND SOURCE $V_{(sat)}$



TEST TABLE

C	D	S2	Y	Z
0.8 V	4.5 V	0.8 V	R_L	OPEN
4.5 V	0.8 V	0.8 V	OPEN	R_L

NOTE A: These parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle ⩽ 2%.

FIGURE 4–V_{IL} AND SINK $V_{(sat)}$

† Arrows indicate actual direction of current flow.

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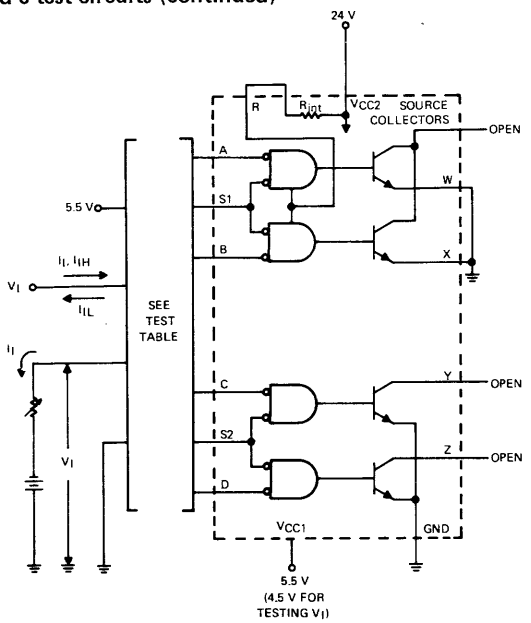
PARAMETER MEASUREMENT INFORMATION

d-c test circuits (continued)†



TEST TABLES

I_I, I_{IH}

APPLY V_I = 5.5 V, MEASURE I_I APPLY V_I = 2.4 V, MEASURE I_{IH}	GROUND	APPLY 5.5 V
A	S1	B, C, S2, D
S1	A, B	C, S2, D
B	S1	A, C, S2, D
C	S2	A, S1, B, D
S2	C, D	A, S1, B
D	S2	A, S1, B, C

V_I, I_{IL}

APPLY V_I = 0.4 V, MEASURE I_{IL} APPLY I_I = −10 mA MEASURE V_I	APPLY 5.5 V
A	S1, B, C, S2, D
S1	A, B, C, S2, D
B	A, S1, C, S2, D
C	A, S1, B, S2, D
S2	A, S1, B, C, D
D	A, S1, B, C, S2

FIGURE 5–V_I, I_I, I_{IH}, AND I_{IL}

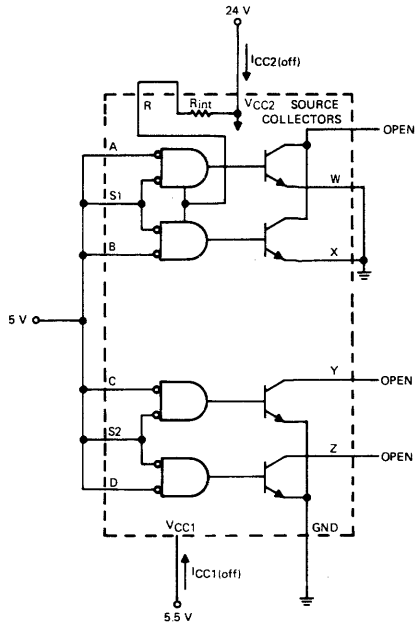
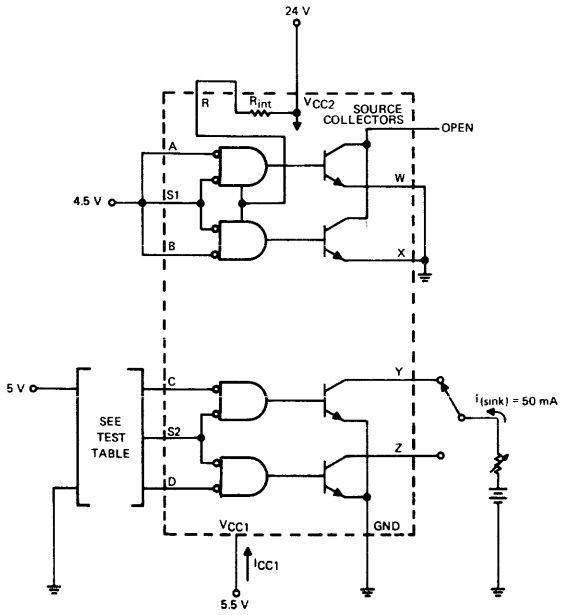


FIGURE 6–$I_{CC1(off)}$ AND $I_{CC2(off)}$

† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

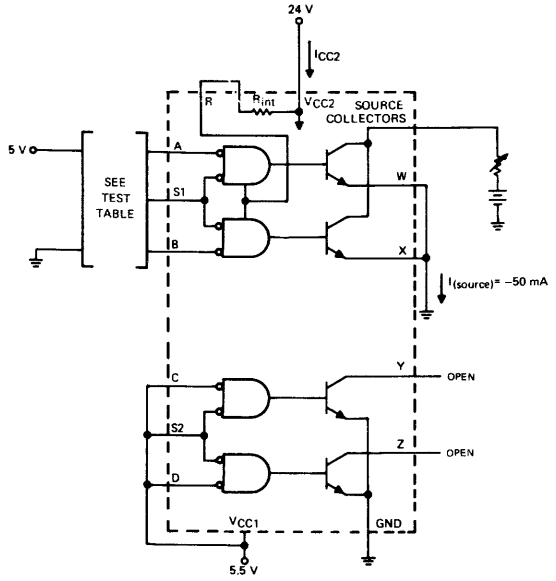
d-c test circuits (continued)†



TEST TABLE

C	D	S2	Y	Z
GND	5 V	GND	$I_{(sink)}$	OPEN
5 V	GND	GND	OPEN	$I_{(sink)}$

FIGURE 7–I_{CC1}, EITHER SINK ON



TEST TABLE

A	B	S1
GND	5 V	GND
5 V	GND	GND

FIGURE 8–I_{CC2}, EITHER SOURCE ON

† Arrows indicate actual direction of current flow.

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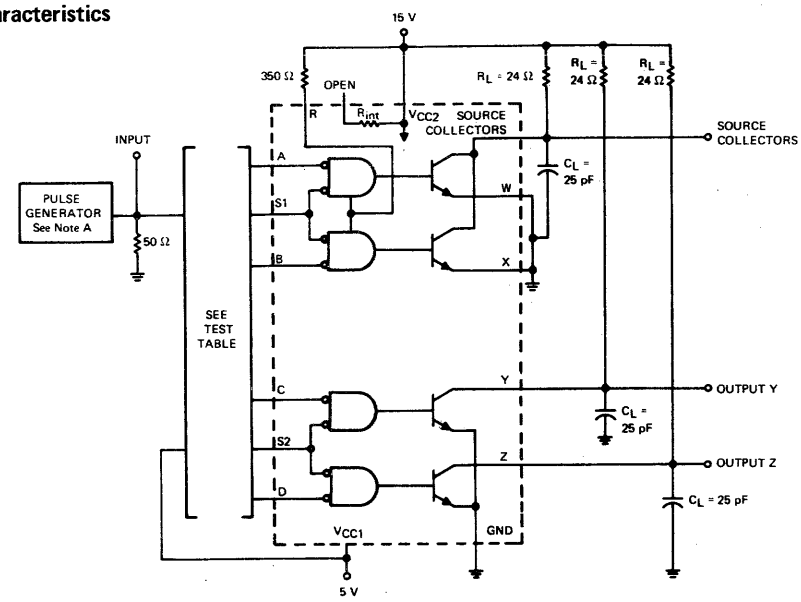
PARAMETER MEASUREMENT INFORMATION

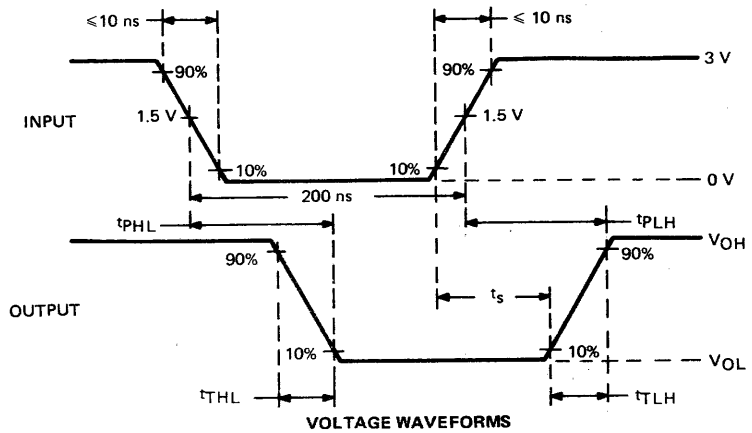
switching characteristics



TEST CIRCUIT

TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5 V
t_{PLH} and t_{PHL}	Source collectors	A and S1	B, C, D and S2
		B and S1	A, C, D and S2
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, and t_s	Sink output Y	C and S2	A, B, D and S1
	Sink output Z	D and S2	A, B, C and S1



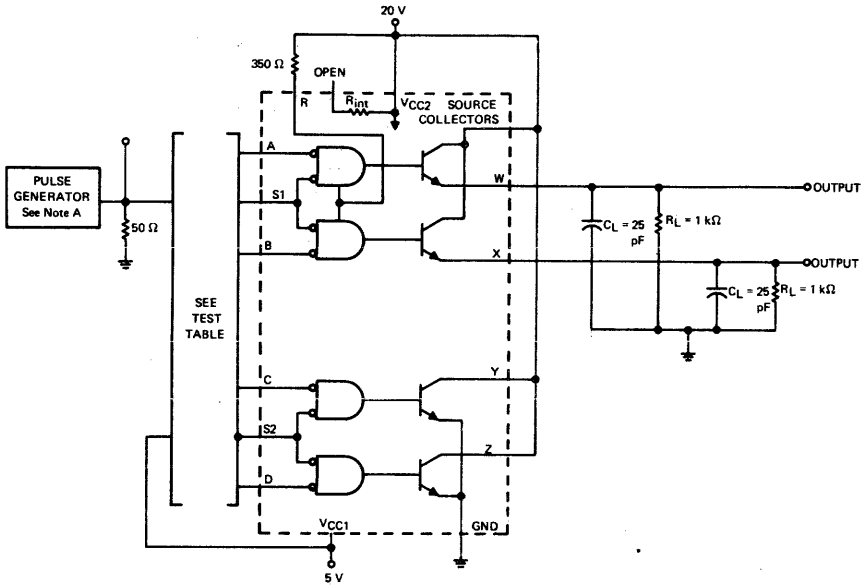
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, duty cycle ≤ 1%.
B. C_L includes probe and jig capacitance.

FIGURE 9–SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

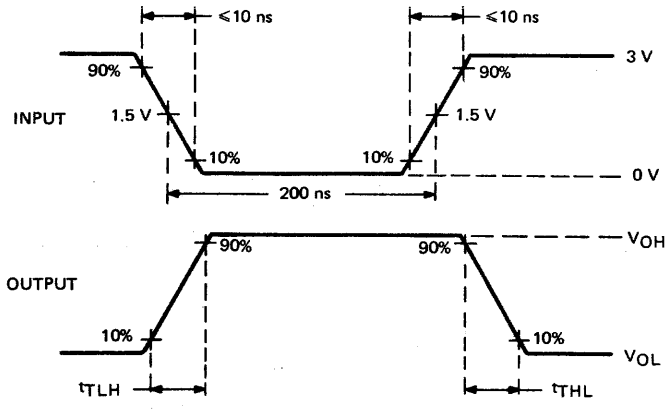
switching characteristics



TEST CIRCUIT

TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5 V
t_{TLH} and t_{THL}	Source output W	A and S1	B, C, D, and S2
	Source output X	B and S1	A, C, D, and S2



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, duty cycle ≤ 1%.
B. C_L includes probe and jig capacitance.

FIGURE 10–TRANSITION TIMES OF SOURCE OUTPUTS

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TYPICAL CHARACTERISTICS

OFF-STATE CURRENT INTO SOURCE COLLECTORS
vs
FREE-AIR TEMPERATURE

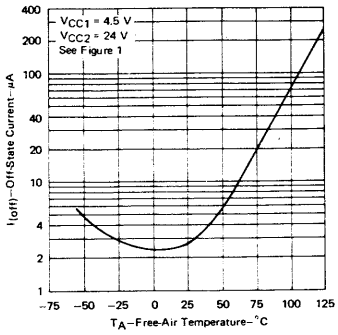


FIGURE 11

HIGH-LEVEL SINK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

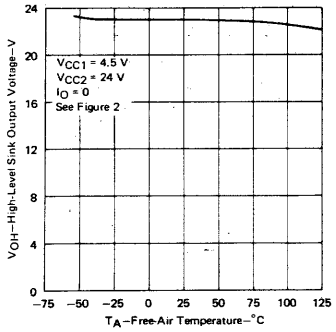


FIGURE 12

SOURCE OR SINK SATURATION VOLTAGE
vs
SOURCE CURRENT OR SINK CURRENT

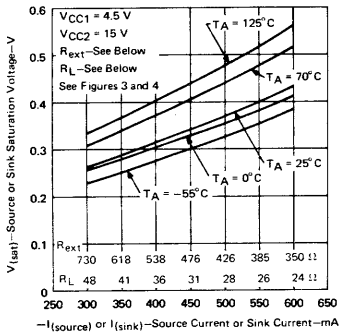


FIGURE 13

SOURCE OR SINK SATURATION VOLTAGE
vs
FREE-AIR TEMPERATURE

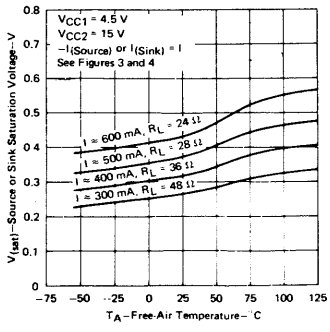


FIGURE 14

SUPPLY CURRENT, ALL SOURCES AND SINKS OFF
vs
FREE-AIR TEMPERATURE

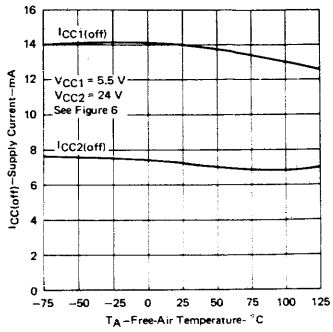
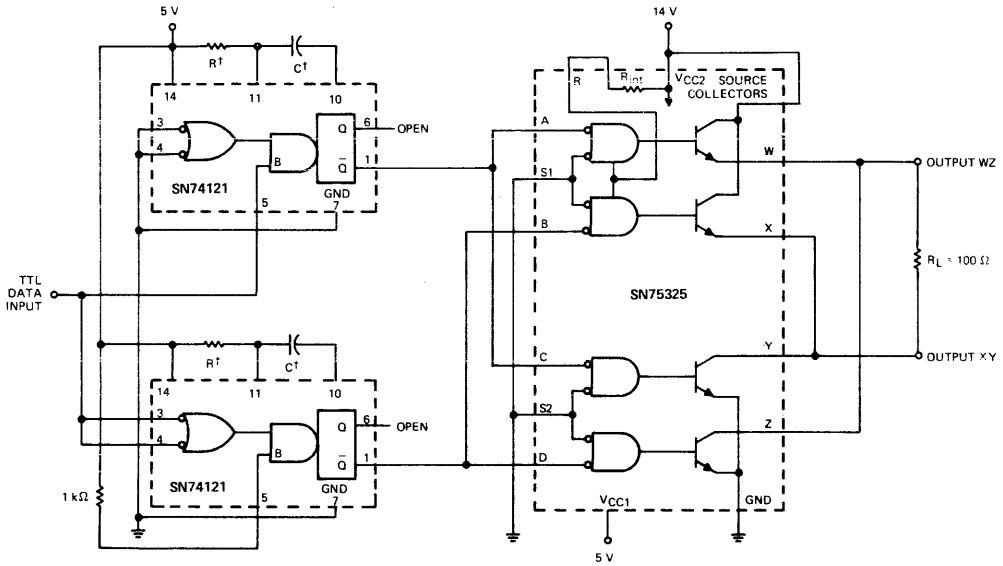


FIGURE 15

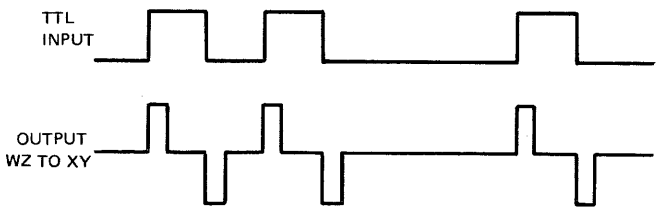
TYPICAL APPLICATION DATA

balanced bipolar logic-line driver

The circuit shown in Figure 16 converts standard TTL logic to bipolar logic. Bipolar logic is primarily used in transmitting data or clock pulses over long lines. This line-driver may be operated from a single 5-volt supply; however, the output drive may be increased by raising the supply voltage to the source collectors. The circuit features a tri-state output which is off during the absence of data, thus not dissipating high power. It provides a balanced drive circuit giving maximum noise immunity when used with the proper line receiver. Large drive levels can be used to further increase noise immunity. The circuit is capable of driving twisted-pair lines of several miles in length or low-impedance coaxial lines.



TEST CIRCUIT



VOLTAGE WAVEFORMS

†R and C are adjusted to give the desired bipolar output pulse width.

FIGURE 16–BALANCED BIPOLAR LOGIC–LINE DRIVER

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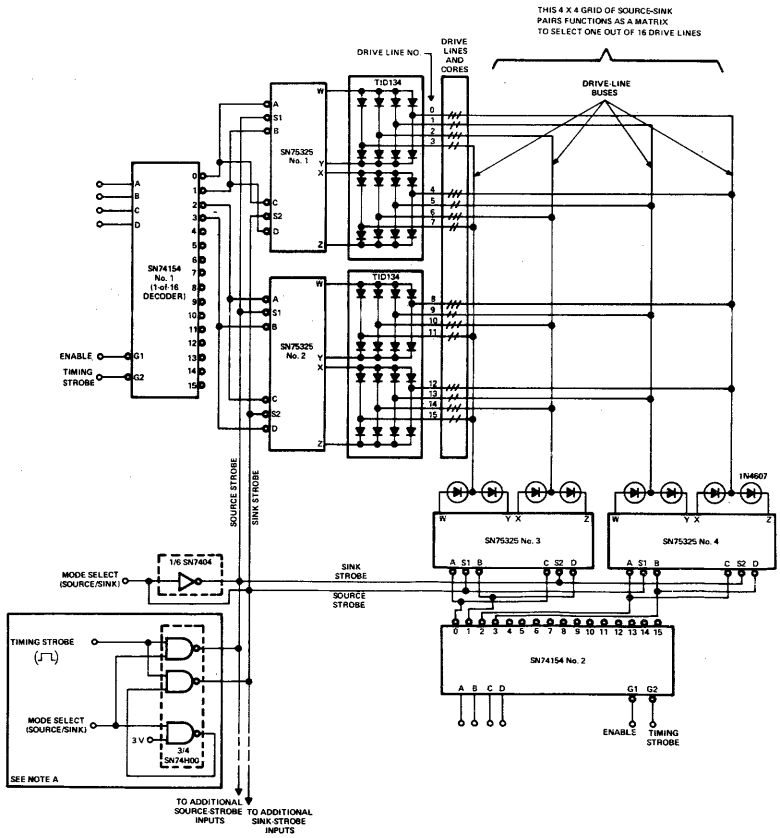
TYPICAL APPLICATION DATA

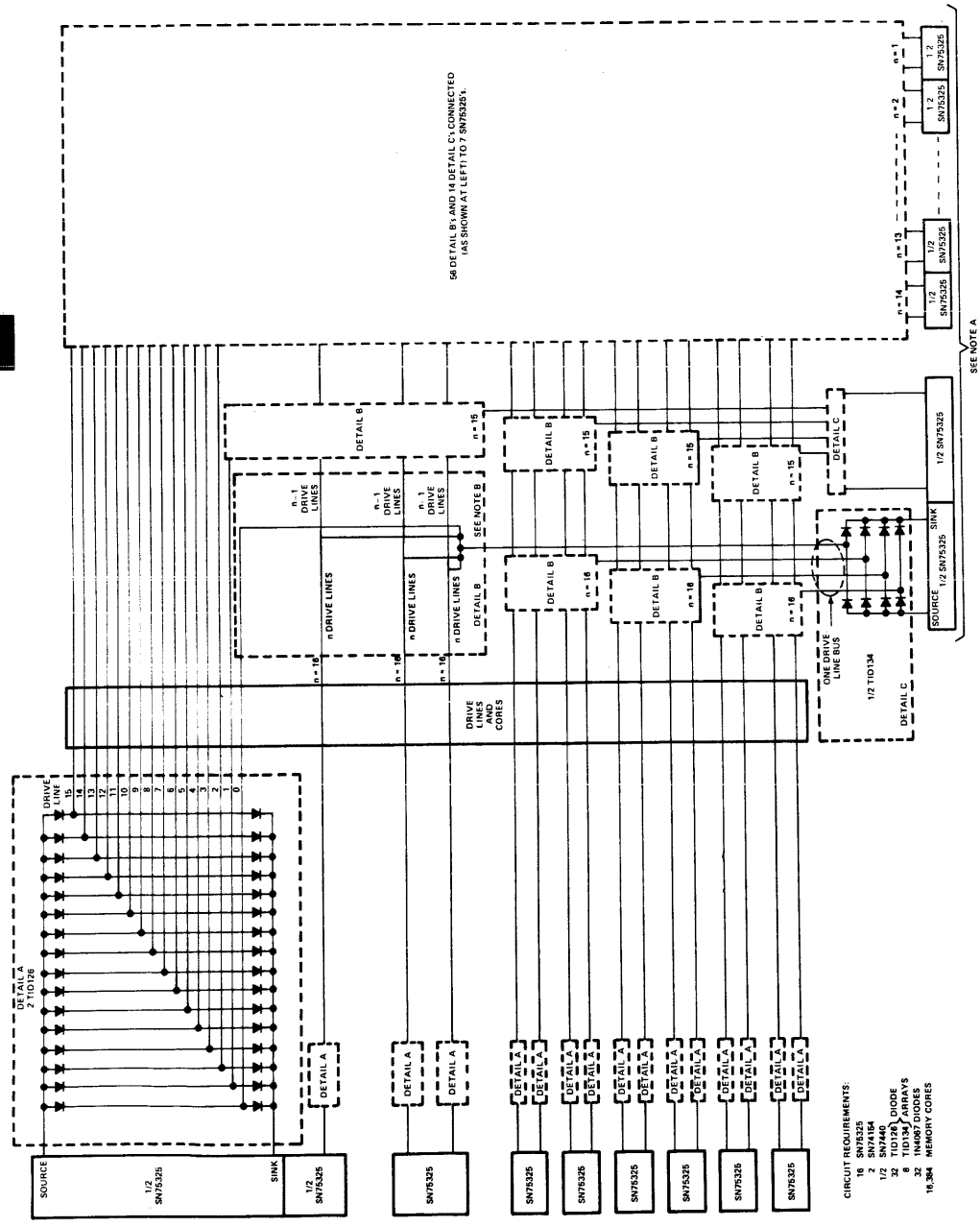
In memory-drive applications the SN75325 (or for full-temperature operation, the SN55325) can be connected in any of several ways. Typically, however, sources and sinks are arranged in pairs from which many drive-lines branch off as shown in Figure 17. Here each drive-line is served by a unique combination of two source/sink pairs so that a selection matrix is formed. To select drive-line 13, SN74154 No. 1 must be set to 3 (with mode select high), enabling source X of SN75325 No. 2 to drive lines 12 through 15, and SN74154 No. 2 must be set to 2, providing a sink at Y of SN75325 No. 4 for drive-line 13 only. Alternatively, to drive current in drive-line 13 in the opposite direction, only the mode-select voltage would be changed from high to low. The size of such a matrix is limited only by the number of drive-lines that a source/sink pair can serve. This number in turn depends on the capacitive and inductive load that each drive-line of the particular system imposes on the driver. A 256-drive-line selection matrix is shown in Figure 18. These 256 drive-lines are sufficient to serve $(256/2)^2 = 16{,}384$ individual cores.



NOTE A: This optional mode-select and timing-strobe technique can be used in place of the SN7440 mode-select and SN74154 timing-strobe when minimum time skew is desired.

FIGURE 17–SN75325 USED AS A MEMORY DRIVER TO SELECT ONE OF SIXTEEN DRIVE LINES

TYPICAL APPLICATION DATA



NOTES: A. Outputs from one SN74154 decoder are connected to each SN75325 as shown in Figure 17. Source strobe and sink strobe from an SN7440 are connected to each SN75325 as shown in Figure 17.

B. The division of the drive-line bus into four segments reduces the capacitive load on the SN75325 driver.

FIGURE 18–SN75325 SERVING 256 DRIVE LINES IN A MAGNETIC MEMORY

TYPICAL APPLICATION DATA

external resistor calculation

A typical magnetic-memory word-drive requirement is shown in Figure 19. A source-output transistor of one SN75325 delivers load current (I_L). The sink-output transistor of another SN75325 sinks this current.

The value of the external pull-up resistor (R_{ext}) for a particular memory application may be determined using the following equation:

$$R_{ext} = \frac{16\,[V_{CC2(min)} - V_S - 2.2]}{I_L - 1.6\,[V_{CC2(min)} - V_S - 2.9]} \qquad \text{(Equation 1)}$$

where: R_{ext} is in kΩ,
$V_{CC2(min)}$ is the lowest expected value of V_{CC2} in volts,
V_S is the source output voltage in volts with respect to ground,
I_L is in mA.

3

The power dissipated in resistor R_{ext} during the load current pulse duration is calculated using Equation 2,

$$P_{Rext} \approx \frac{I_L}{16}\,[V_{CC2(min)} - V_S - 2] \qquad \text{(Equation 2)}$$

where: P_{Rext} is in mW.

After solving for R_{ext}, the magnitude of the source collector current (I_{CS}) is determined from Equation 3,

$$I_{CS} \approx 0.94\, I_L \qquad \text{(Equation 3)}$$

where: I_{CS} is in mA.

As an example, let $V_{CC2(min)}$ = 20 V and V_L = 3 V while I_L of 500 mA flows.

Using Equation 1,

$$R_{ext} = \frac{16\ (20 - 3 - 2.2)}{500 - 1.6\ (20 - 3 - 2.9)} = 0.5\ k\Omega$$

and from Equation 2,

$$P_{Rext} \approx \frac{500}{16}\,[20 - 3 - 2] \approx 470\ mW$$

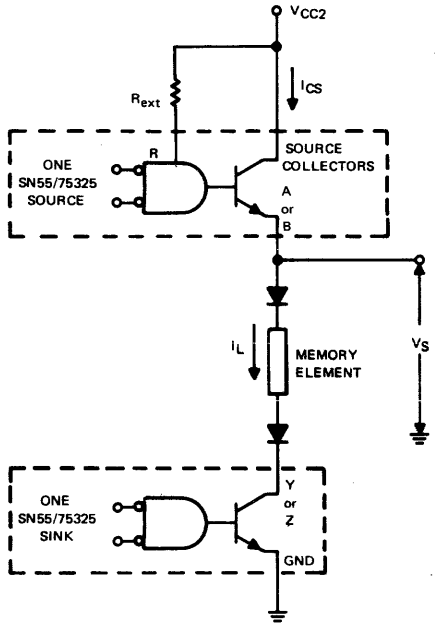
The amount of the memory system current source (I_{CS}) from Equation 3 is:

$$I_{CS} \approx 0.94\ (500) \approx 470\ mA$$

In this example the regulated source-output transistor base current through the external pull-up resistor (R_{ext}) and the source gate is approximately 30 mA. This current and I_{CS} comprise I_L.

TYPICAL APPLICATION DATA

external resistor calculation (continued)



NOTES: A. For clarity, partial logic diagrams of two SN75325's are shown.
B. Source and sink shown are in different packages.

FIGURE 19

THERMAL INFORMATION

SN55325
DISSIPATION DERATING CURVE

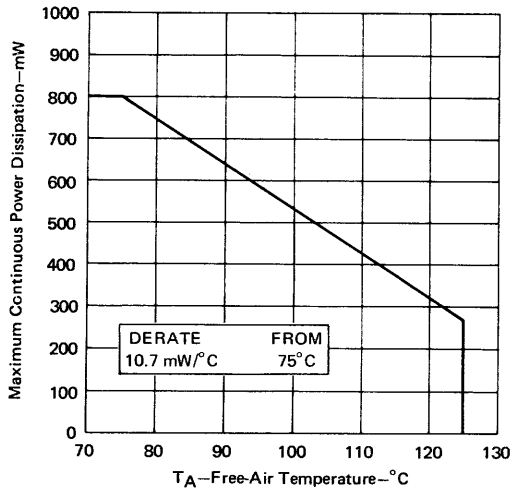


FIGURE 20

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SERIES 75450
DUAL PERIPHERAL DRIVERS

PERIPHERAL DRIVERS FOR HIGH-CURRENT SWITCHING AT HIGH SPEEDS

performance

- 300-mA Output Current Capability
- High-Voltage Outputs
- High-Speed Switching

ease-of-design

- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL or DTL Compatible Diode-Clamped Inputs
- Standard Supply Voltages

SUMMARY OF DUAL DRIVERS

DEVICE	LOGIC OF COMPLETE CIRCUIT	PACKAGE
SN75450A	AND†	N
SN75451A	AND	P
SN75452	NAND	P
SN75453	OR	P
SN75454	NOR	P

†With transistor base connected directly to output of gate.

3

description

Series 75450 dual peripheral drivers are a family of versatile devices designed for use in systems that employ TTL or DTL logic. Typical applications include high-speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, and memory drivers. Additionally, the SN75450A may be used as a line driver. The SN75450A and SN75451A are functionally interchangeable with and are recommended for replacement of SN75450 and SN75451, respectively, in most applications which do not require the very high speed of the prototypes. The A-versions offer improved freedom from latch-up and diode-clamped inputs to simplify system design. They can drive lamps, relays, and memories to rated levels of voltage and current without external loading capacitors. Series 75450 drivers are monolithic circuits designed for operation over the temperature range of 0°C to 70°C.

The SN75450A is a unique general-purpose device featuring two standard Series 74 TTL gates and two uncommitted, high-current, high-voltage n-p-n transistors. The SN75450A offers the system designer the flexibility of tailoring the circuit to the application.

The SN75451A, SN75452, SN75453, and SN75454 are dual peripheral AND, NAND, OR, and NOR drivers respectively, (assuming positive logic) with the output of the logic gates internally connected to the bases of the n-p-n output transistors.

CONTENTS

	PAGE
MAXIMUM RATINGS AND RECOMMENDED OPERATING CONDITIONS	3-246
DEFINITIVE SPECIFICATIONS:	
CIRCUIT TYPE SN75450A	3-247
CIRCUIT TYPE SN75451A	3-249
CIRCUIT TYPE SN75452	3-250
CIRCUIT TYPE SN75453	3-251
CIRCUIT TYPE SN75454	3-252
D-C TEST CIRCUITS	3-253
SWITCHING TIME TEST CIRCUITS AND VOLTAGE WAVEFORMS	3-255
TYPICAL CHARACTERISTICS	3-258
TYPICAL APPLICATIONS	3-259

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN75450A	SN75451A SN75452 SN75453 SN75454	UNIT
Supply voltage, V_{CC}	7	7	V
Input voltage (see Note 1)	5.5	5.5	V
Interemitter voltage (see Note 2)	5.5	5.5	V
V_{CC}-to-substrate voltage	35		V
Collector-to-substrate voltage	35		V
Collector-base voltage	35		V
Collector-emitter voltage (see Note 3)	30		V
Emitter-base voltage	5		V
Output voltage (see Notes 1 and 4)		30	V
Continuous collector current (see Note 5)	300		mA
Continuous output current (see Note 5)		300	mA
Continuous total power dissipation	800	800	mW
Operating free-air temperature range	0 to 70	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 10 seconds	260	260	°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.
4. This is the maximum voltage which should be applied to any output when it is in the off state.
5. Both halves of these dual circuits may conduct rated current simultaneously.

recommended operating conditions (see note 6)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Operating free-air temperature range, T_A	0	25	70	°C

NOTE 6: For the SN75450A only, the substrate (pin 8), must always be at the most-negative device voltage for proper operation.

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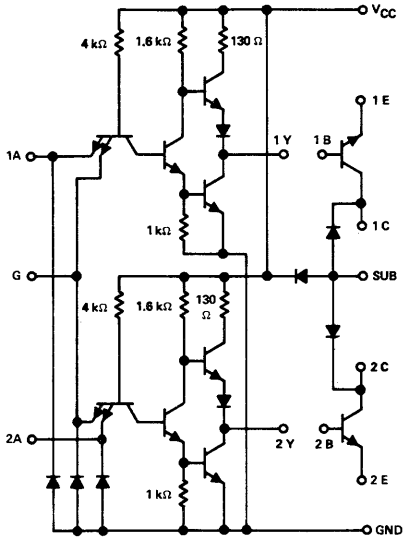
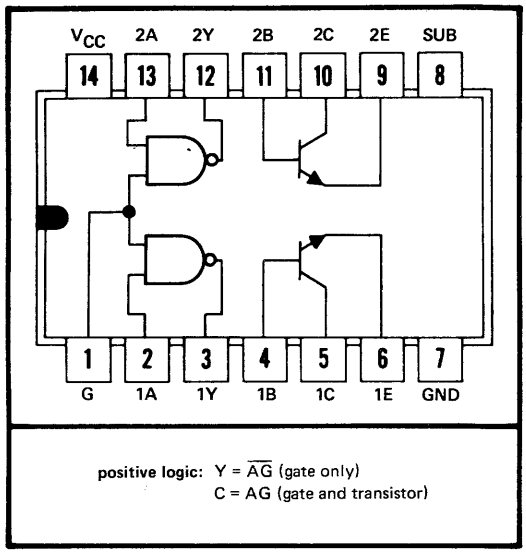
schematic



Component values shown are nominal

N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AG}$ (gate only)
$C = AG$ (gate and transistor)

3

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

TTL gates

PARAMETER			TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage		1		2			V
V_{IL}	Low-level input voltage		2				0.8	V
V_I	Input clamp voltage		3	V_{CC} = 4.75 V, I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		2	V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OH} = −400 μA	2.4	3.3		V
V_{OL}	Low-level output voltage		1	V_{CC} = 4.75 V, V_{IH} = 2 V, I_{OL} = 16 mA		0.22	0.4	V
I_I	Input current at maximum input voltage	input A	4	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
		input G					2	
I_{IH}	High-level input current	input A	4	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
		input G					80	
I_{IL}	Low-level input current	input A	3	V_{CC} = 5.25 V, V_I = 0.4 V			−1.6	mA
		input G					−3.2	
I_{OS}	Short-circuit output current‡		5	V_{CC} = 5.25 V	−18		−55	mA
I_{CCH}	Supply current, high-level output		6	V_{CC} = 5.25 V, V_I = 0		2	4	mA
I_{CCL}	Supply current, low-level output			V_{CC} = 5.25 V, V_I = 5 V		6	11	mA

†All typical values at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

output transistors

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 100 μA,	I_E = 0		35			V
$V_{(BR)CER}$	Collector-Emitter Breakdown Voltage	I_C = 100 μA,	R_{BE} = 500 Ω		30			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 100 μA,	I_C = 0		5			V
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 3 V, T_A = 25°C	I_C = 100 mA,	See Note 7	25			
		V_{CE} = 3 V, T_A = 25°C	I_C = 300 mA,		30			
		V_{CE} = 3 V, T_A = 0°C	I_C = 100 mA,		20			
		V_{CE} = 3 V, T_A = 0°C	I_C = 300 mA,		25			
V_{BE}	Base-Emitter Voltage	I_B = 10 mA,	I_C = 100 mA	See Note 7		0.85	1	V
		I_B = 30 mA,	I_C = 300 mA			1.05	1.2	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_B = 10 mA,	I_C = 100 mA	See Note 7		0.25	0.4	V
		I_B = 30 mA,	I_C = 300 mA			0.5	0.7	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 7: These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

TTL gates

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	12	C_L = 15 pF,	R_L = 400 Ω		20		ns
t_{PHL}	Propagation delay time, high-to-low-level output					8		ns

output transistors

PARAMETER		TEST FIGURE	TEST CONDITIONS‡		MIN	TYP	MAX	UNIT
t_d	Delay time	13	I_C = 200 mA,	$I_{B(1)}$ = 20 mA,		8		ns
t_r	Rise time		$I_{B(2)}$ = −40 mA,	$V_{BE(off)}$ = −1 V,		12		ns
t_s	Storage time		C_L = 15 pF,	R_L = 50 Ω		7		ns
t_f	Fall time					6		ns

gates and transistors combined

PARAMETER		TEST FIGURE	TEST CONDITIONS‡		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	14	I_C = 200 mA,	C_L = 15 pF,		40		ns
t_{PHL}	Propagation delay time, high-to-low-level output		R_L = 50 Ω			25		ns
t_{TLH}	Transition time, low-to-high-level output					10		ns
t_{THL}	Transition time, high-to-low-level output					12		ns

‡Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

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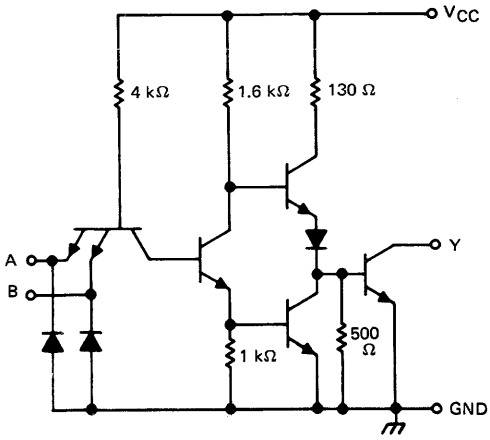
schematic (each driver)



Component values shown are nominal

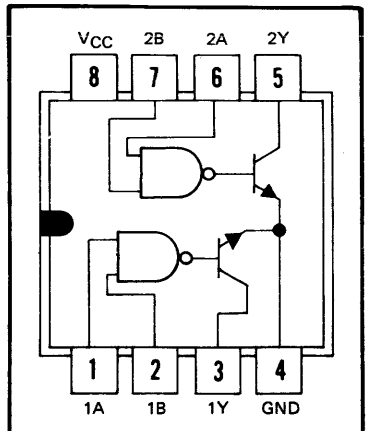
logic

TRUTH TABLE

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

H = high level, L = low level

P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Y = AB

3

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage	7		2			V
V_{IL}	Low-level input voltage	7				0.8	V
V_I	Input clamp voltage	8	V_{CC} = 4.75 V, I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	7	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{OH} = 30 V			100	μA
V_{OL}	Low-level output voltage	7	V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.4	V
			V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	9	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	9	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	8	V_{CC} = 5.25 V, V_I = 0.4 V		−1	−1.6	mA
I_{CCH}	Supply current, high-level output	10	V_{CC} = 5.25 V, V_I = 5 V		7	11	mA
I_{CCL}	Supply current, low-level output		V_{CC} = 5.25 V, V_I = 0		52	65	mA

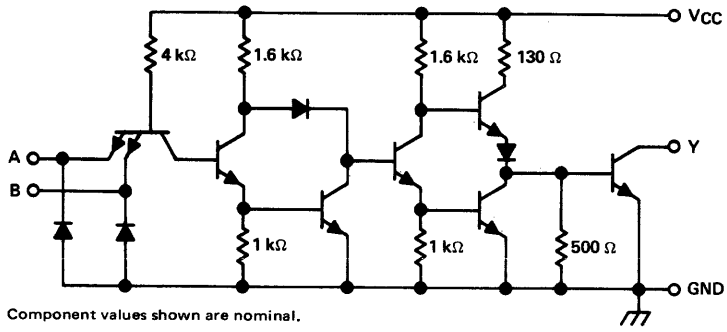
†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		45		ns
t_{PHL}	Propagation delay time, high-to-low-level output				25		ns
t_{TLH}	Transition time, low-to-high-level output				10		ns
t_{THL}	Transition time, high-to-low-level output				12		ns

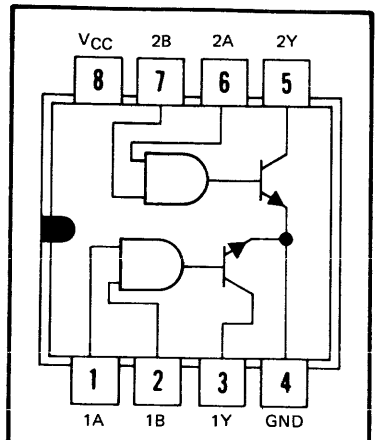
CIRCUIT TYPE SN75452
DUAL PERIPHERAL POSITIVE-NAND DRIVER

schematic (each driver)



Component values shown are nominal.

P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AB}$

logic

3

TRUTH TABLE

A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

H = high level L = low level

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage	7		2			V
V_{IL}	Low-level input voltage	7				0.8	V
V_I	Input clamp voltage	8	V_{CC} = 4.75 V, I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	7	V_{CC} = 4.75 V, V_{IL} = 0.8 V, V_{OH} = 30 V			100	μA
V_{OL}	Low-level output voltage	7	V_{CC} = 4.75 V, V_{IH} = 2 V, I_{OL} = 100 mA		0.25	0.4	V
			V_{CC} = 4.75 V, V_{IH} = 2 V, I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	9	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	9	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	8	V_{CC} = 5.25 V, V_I = 0.4 V			−1.6	mA
I_{CCH}	Supply current, high-level output	10	V_{CC} = 5.25 V, V_I = 0 V		11	14	mA
I_{CCL}	Supply current, low-level output		V_{CC} = 5.25 V, V_I = 5 V		56	71	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		50		ns
t_{PHL}	Propagation delay time, high-to-low-level output				35		ns
t_{TLH}	Transition time, low-to-high-level output				10		ns
t_{THL}	Transition time, high-to-low-level output				12		ns

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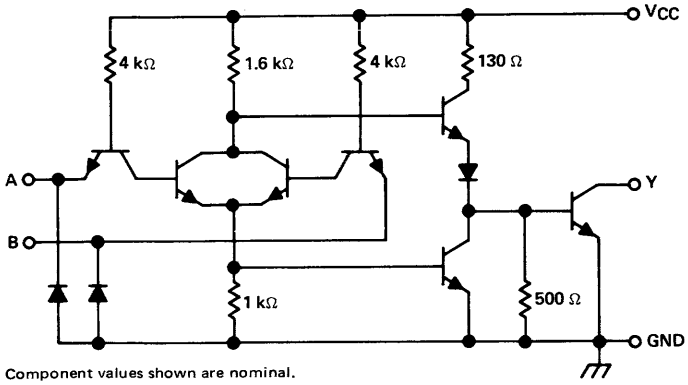
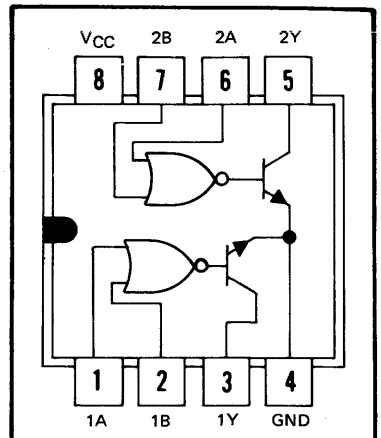
schematic (each driver)



Component values shown are nominal.

P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Y = A + B

logic

TRUTH TABLE

A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

H = high level, L = low level

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage	7		2			V
V_{IL}	Low-level input voltage	7				0.8	V
V_I	Input clamp voltage	8	V_{CC} = 4.75 V, I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	7	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{OH} = 30 V			100	μA
V_{OL}	Low-level output voltage	7	V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.4	V
			V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	9	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	9	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	8	V_{CC} = 5.25 V, V_I = 0.4 V		−1	−1.6	mA
I_{CCH}	Supply current, high-level output	11	V_{CC} = 5.25 V, V_I = 5 V		8	11	mA
I_{CCL}	Supply current, low-level output		V_{CC} = 5.25 V, V_I = 0		54	68	mA

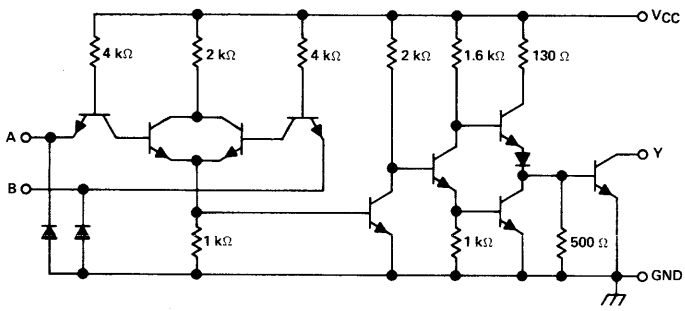
†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		35		ns
t_{PHL}	Propagation delay time, high-to-low-level output				25		ns
t_{TLH}	Transition time, low-to-high-level output				10		ns
t_{THL}	Transition time, high-to-low-level output				12		ns

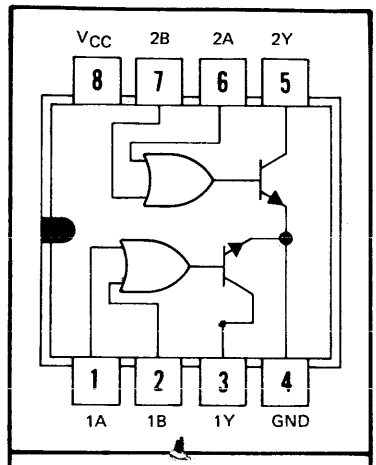
CIRCUIT TYPE SN75454
DUAL PERIPHERAL POSITIVE-NOR DRIVER

schematic (each driver)



P

DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A + B}$

3

logic

TRUTH TABLE

A	B	Y
L	L	H (off state)
L	H	L (on state)
H	L	L (on state)
H	H	L (on state)

H = high level, L = low level

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage	7		2			V
V_{IL}	Low-level input voltage	7				0.8	V
V_I	Input clamp voltage	8	V_{CC} = 4.75 V, I_I = −12 mA			−1.5	V
I_{OH}	High-level output voltage	7	V_{CC} = 4.75 V, V_{IL} = 0.8 V, V_{OH} = 30 V			100	μA
V_{OL}	Low-level output voltage	7	V_{CC} = 4.75 V, V_{IH} = 2 V, I_{OL} = 100 mA		0.25	0.4	V
			V_{CC} = 4.75 V, V_{IH} = 2 V, I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	9	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	9	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	8	V_{CC} = 5.25 V, V_I = 0.4 V		−1	−1.6	mA
I_{CCH}	Supply current, high-level output	11	V_{CC} = 5.25 V, V_I = 0 V		13	17	mA
I_{CCL}	Supply current, low-level output		V_{CC} = 5.25 V, V_I = 5 V		61	79	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		50		ns
t_{PHL}	Propagation delay time, high-to-low-level output				25		ns
t_{TLH}	Transition time, low-to-high-level output				10		ns
t_{THL}	Transition time, high-to-low-level output				12		ns

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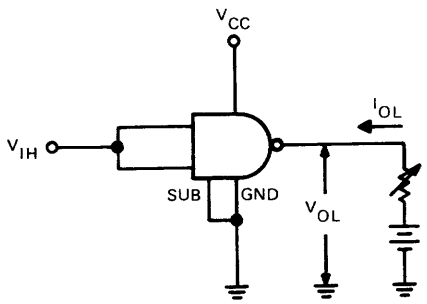
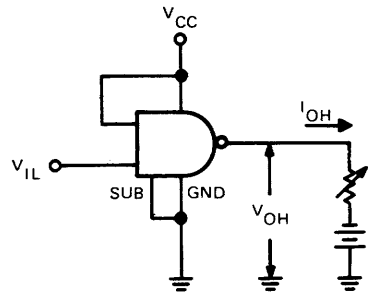
PARAMETER MEASUREMENT INFORMATION

d-c test circuits †



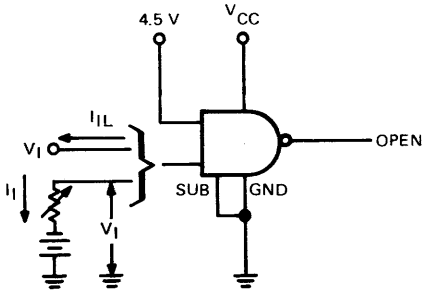
Both inputs are tested simultaneously.

FIGURE 1–V_{IH}, V_{OL}



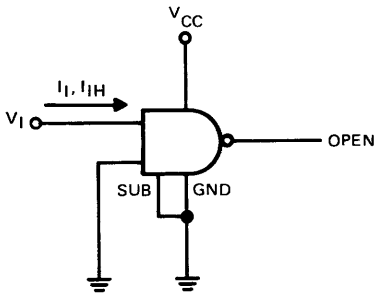
Each input is tested separately.

FIGURE 2–V_{IL}, V_{OH}



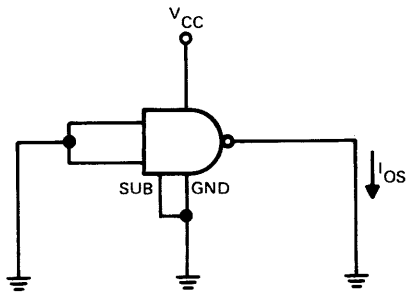
Each input is tested separately.

FIGURE 3–V_I, I_{IL}



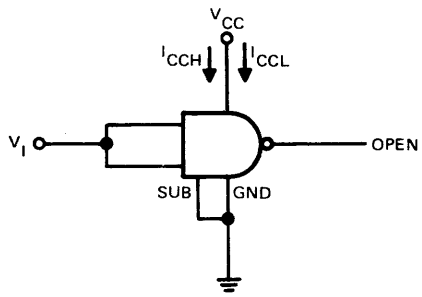
Each input is tested separately.

FIGURE 4–I_I, I_{IH}



Each gate is tested separately.

FIGURE 5–I_{OS}



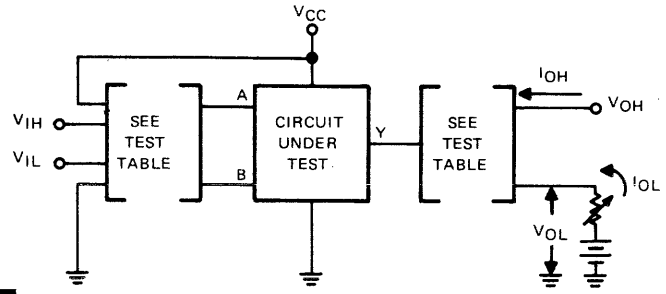
Both gates are tested simultaneously.

FIGURE 6–I_{CCH}, I_{CCL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

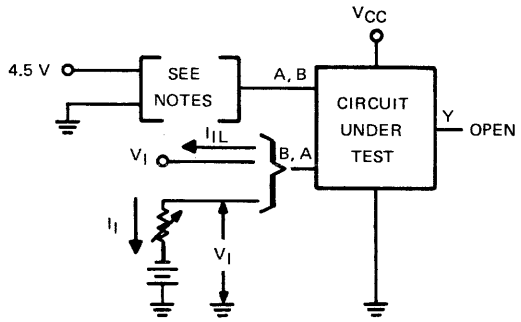


TEST TABLE

CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
SN75451A	V_{IH} V_{IL}	V_{IH} V_{CC}	V_{OH} I_{OL}	I_{OH} V_{OL}
SN75452	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OL} V_{OH}	V_{OL} I_{OH}
SN75453	V_{IH} V_{IL}	GND V_{IL}	V_{OH} I_{OL}	I_{OH} V_{OL}
SN75454	V_{IH} V_{IL}	GND V_{IL}	I_{OL} V_{OH}	V_{OL} I_{OH}

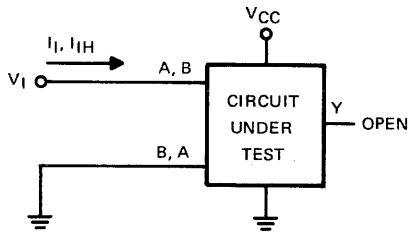
NOTE: Each input is tested separately.

FIGURE 7–V_{IH}, V_{IL}, I_{OH}, V_{OL}



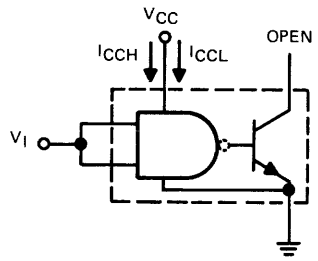
NOTES: A. Each input is tested separately.
B. When testing SN75453 and SN75454, input not under test is grounded. For all other circuits it is at 4.5 V.

FIGURE 8–V_I, I_{IL}



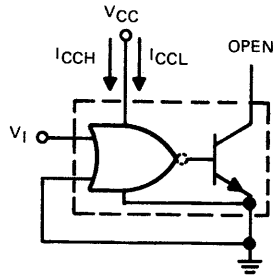
Each input is tested separately.

FIGURE 9–I_I, I_{IH}



Both gates are tested simultaneously.

FIGURE 10–I_{CCH}, I_{CCL} FOR AND, NAND CIRCUITS



Both gates are tested simultaneously.

FIGURE 11–I_{CCH}, I_{CCL} FOR OR, NOR CIRCUITS

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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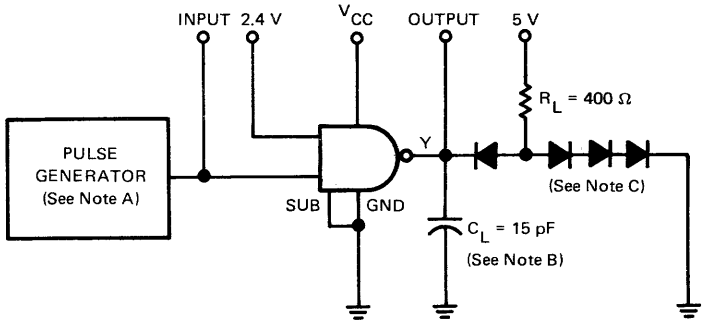
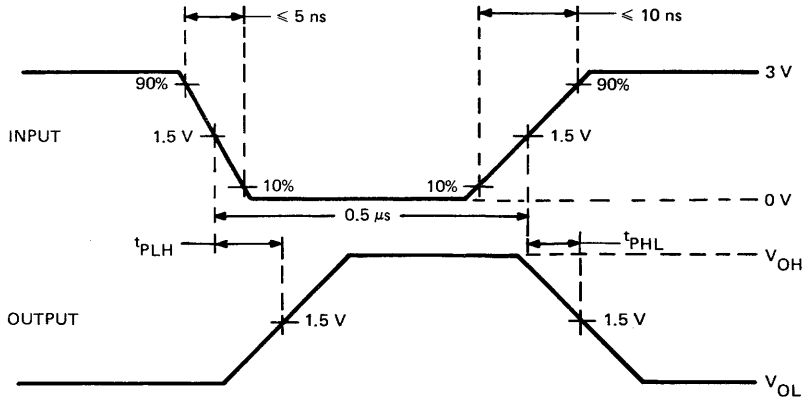
PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



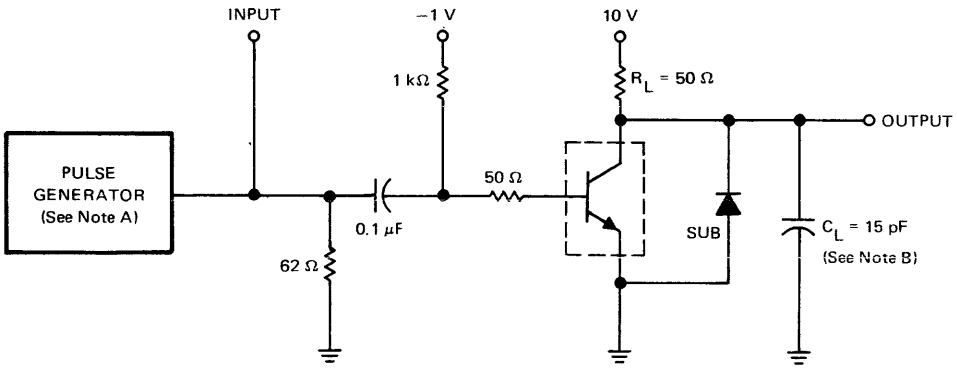
VOLTAGE WAVEFORMS

NOTES. A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L include probe and jig capacitance.
C. All diodes are 1N3064.

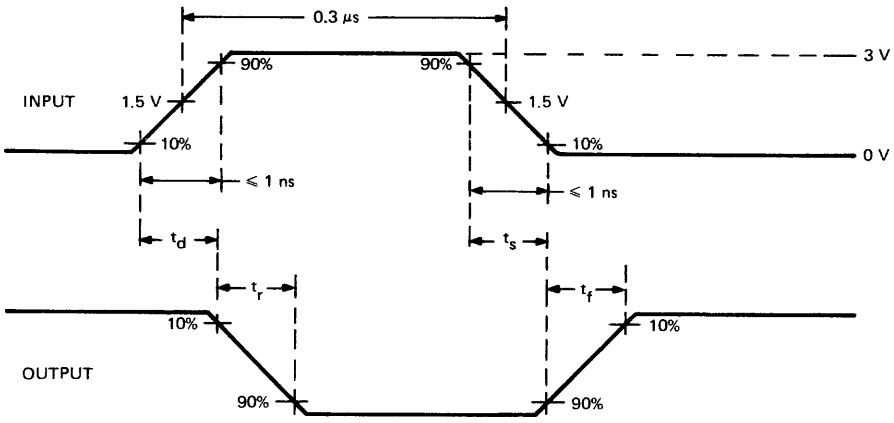
FIGURE 12–PROPAGATION DELAY TIMES, EACH GATE (SN75450A ONLY)

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 1%, Z_{out} ≈ 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 13–SWITCHING TIMES, EACH TRANSISTOR (SN75450A ONLY)

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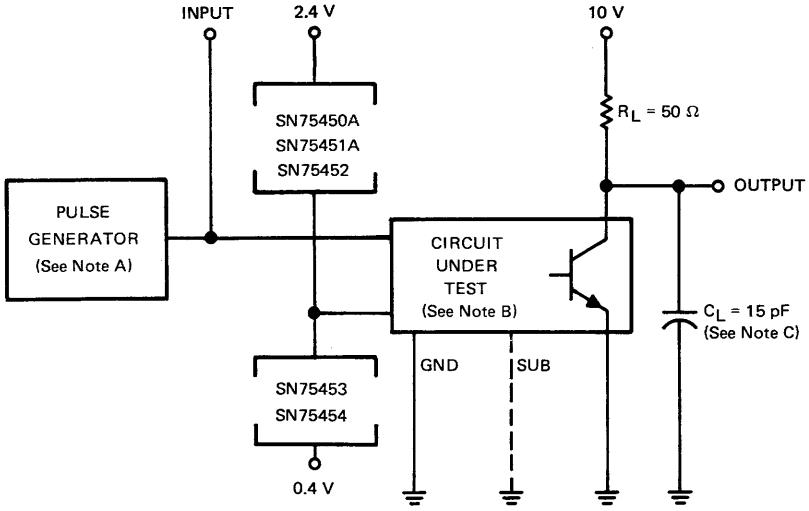
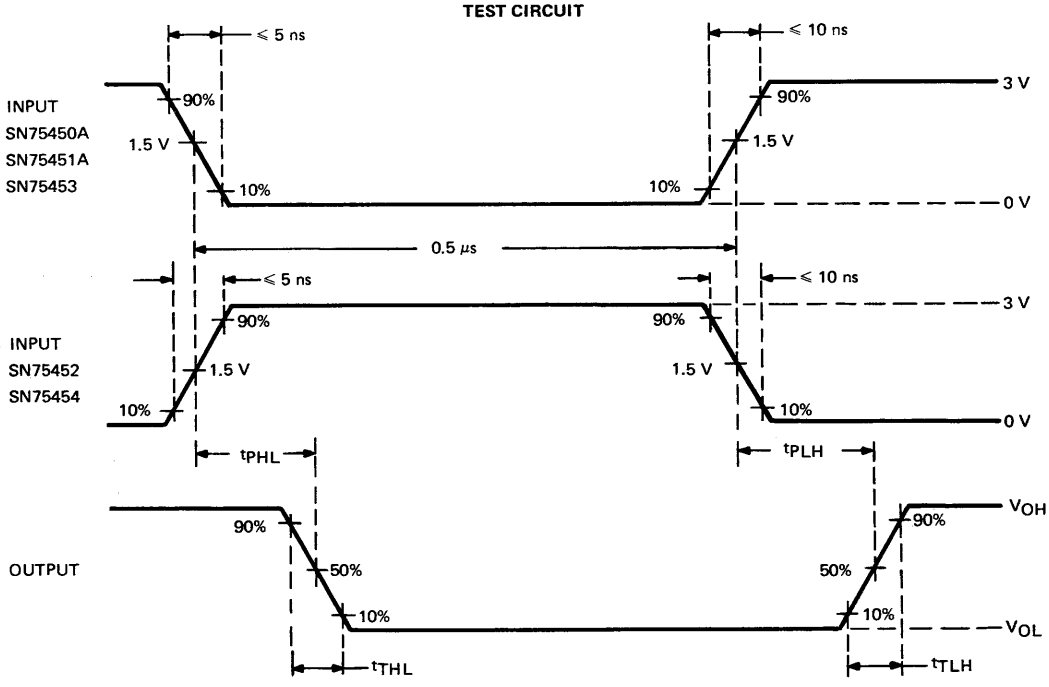
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. When testing SN75450A, connect output Y to transistor base and ground the substrate terminal.
C. C_L includes probe and jig capacitance.

FIGURE 14–SWITCHING TIMES OF COMPLETE DRIVERS

TYPICAL CHARACTERISTICS

SN75450A
TTL GATE
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

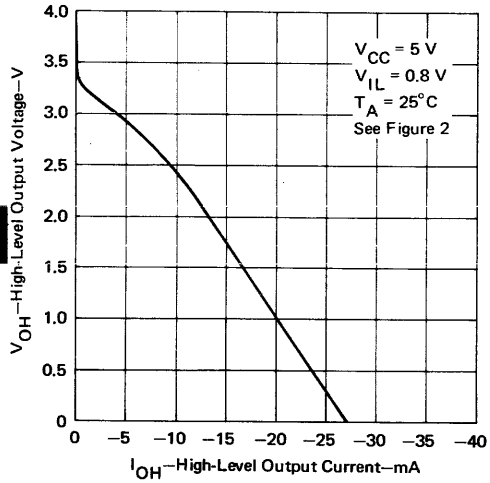


FIGURE 15

SN75450A
TRANSISTOR
STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

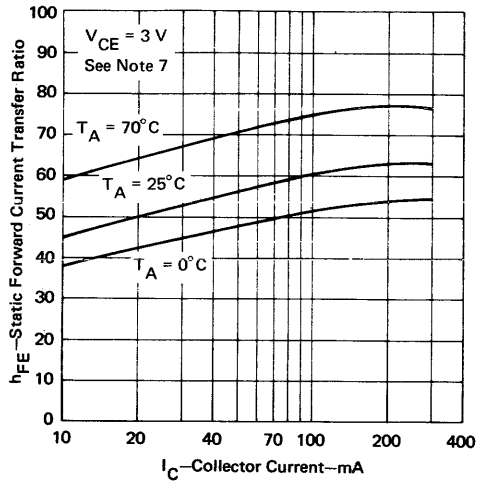


FIGURE 16

SN75450A
TRANSISTOR
BASE-EMITTER VOLTAGE
vs
COLLECTOR CURRENT

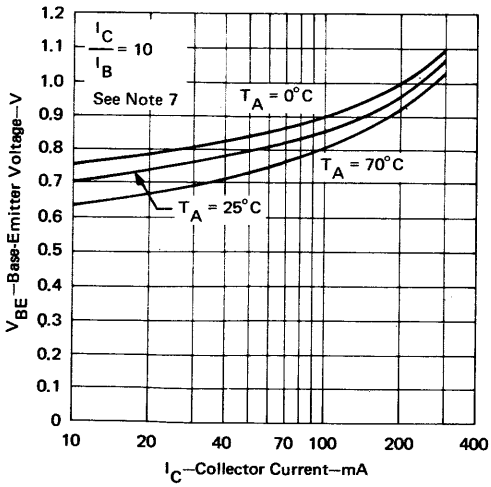


FIGURE 17

TRANSISTOR
COLLECTOR-EMITTER SATURATION VOLTAGE
vs
COLLECTOR CURRENT

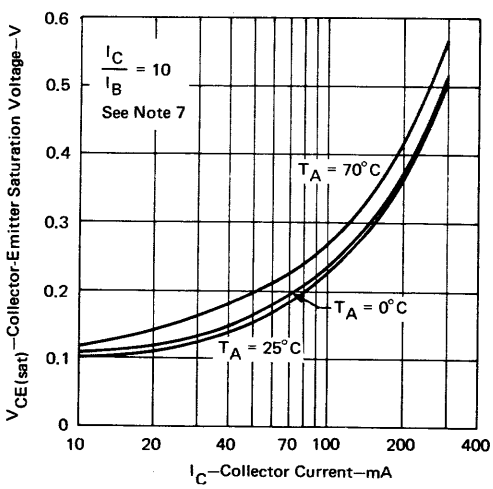
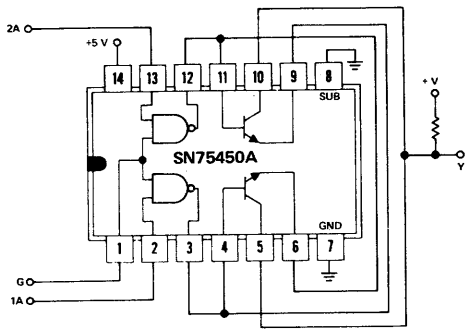


FIGURE 18

NOTE 7: These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

TYPICAL APPLICATION DATA



$Y = \overline{G} + 1A \cdot 2A + 1\overline{A} \cdot 2\overline{A}$

FIGURE 19–GATED COMPARATOR

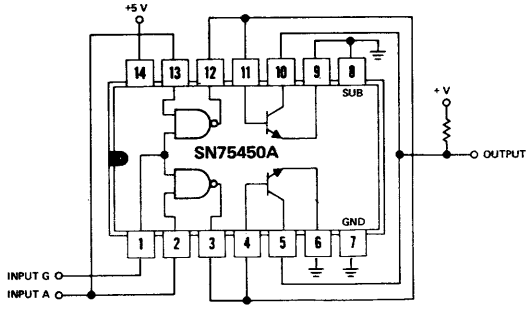


FIGURE 20–500-mA SINK

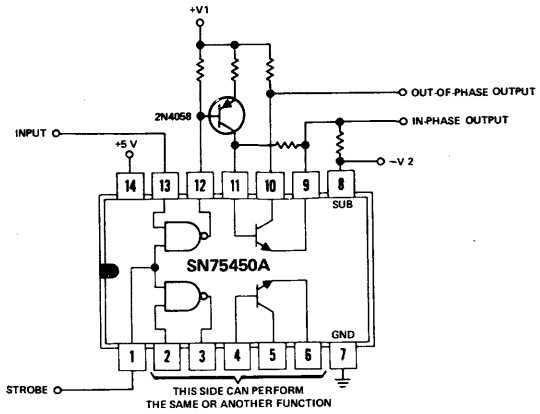


FIGURE 21–FLOATING SWITCH

TYPICAL APPLICATION DATA

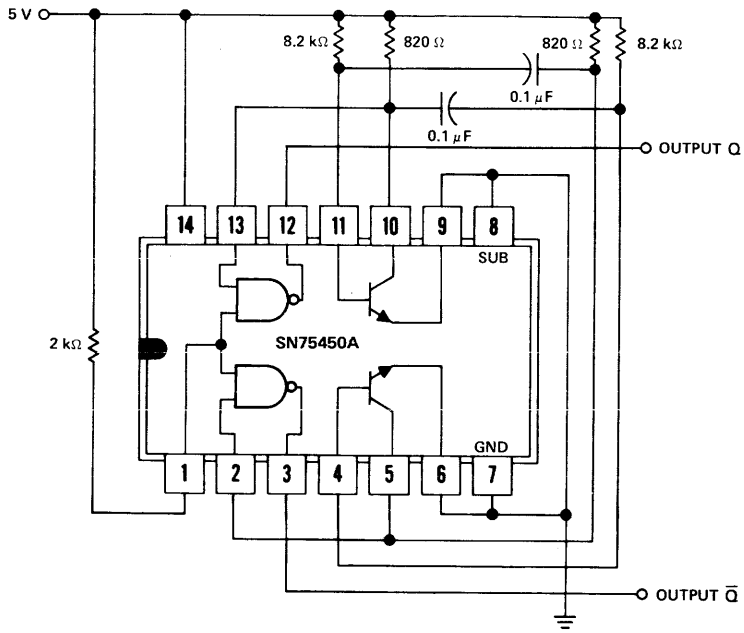
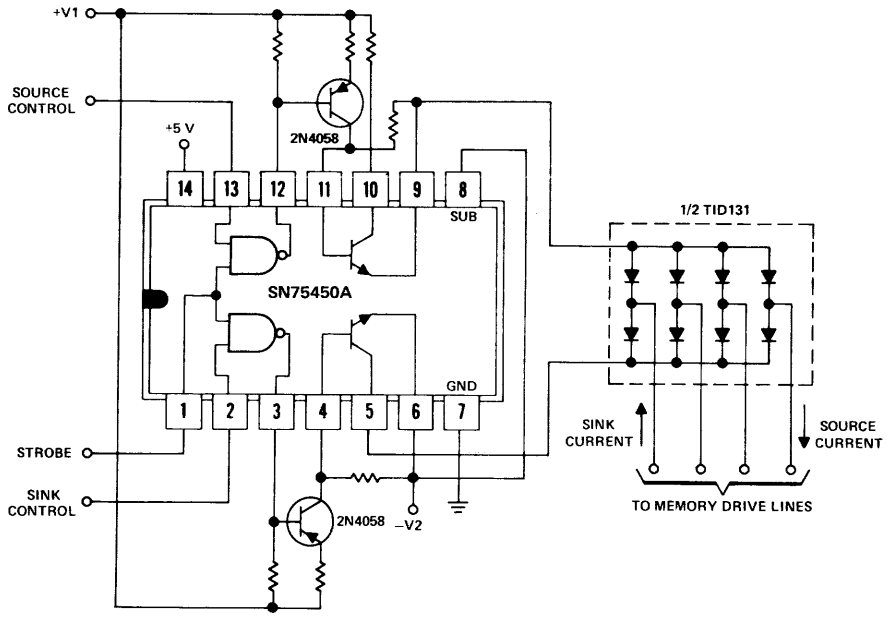


FIGURE 22–SQUARE-WAVE GENERATOR



Source and sink controls are activated by high-level input voltages ($V_{IH} \geq 2V$).

FIGURE 23–CORE MEMORY DRIVER

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TYPICAL APPLICATION DATA

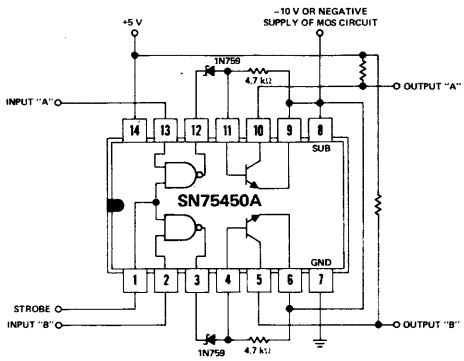


FIGURE 24—DUAL TTL-TO-MOS DRIVER

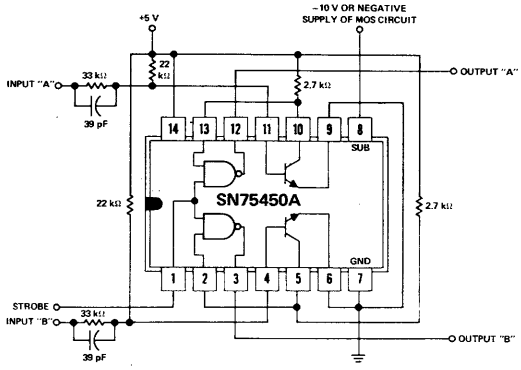
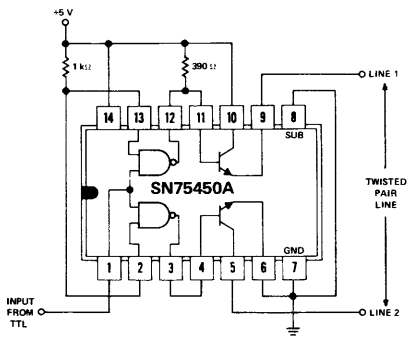
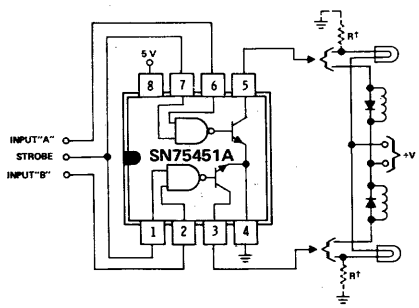


FIGURE 25—DUAL MOS-TO-TTL DRIVER



Termination is made at the receiving end as follows:
Line 1 is terminated to ground through $Z_O/2$;
Line 2 is terminated to +5 volts through $Z_O/2$;
where Z_O is the line impedence.

FIGURE 26—BALANCED LINE DRIVER



† Optional keep-alive resistors maintain off-state lamp current at ≈ 10% to reduce surge current.

FIGURE 27—DUAL LAMP OR RELAY DRIVER

TYPICAL APPLICATION DATA

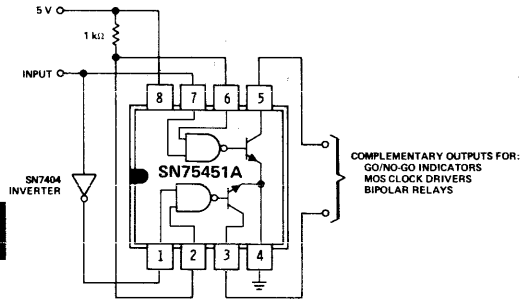


FIGURE 28–COMPLEMENTARY DRIVER

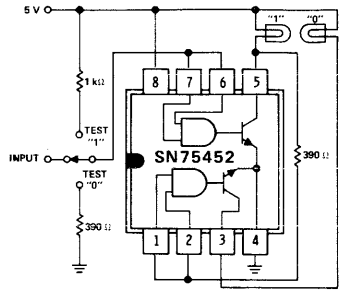
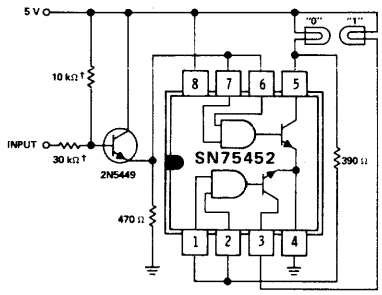


FIGURE 29–TTL OR DTL POSITIVE LOGIC-LEVEL DETECTOR



†The two input resistors must be adjusted for the level of MOS input.

FIGURE 30–MOS NEGATIVE-LOGIC-LEVEL DETECTOR

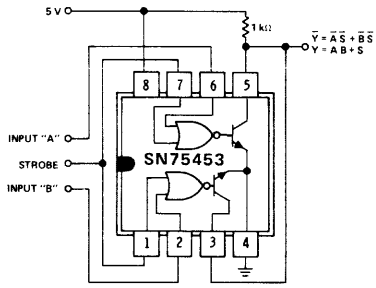


FIGURE 31–LOGIC SIGNAL COMPARATOR

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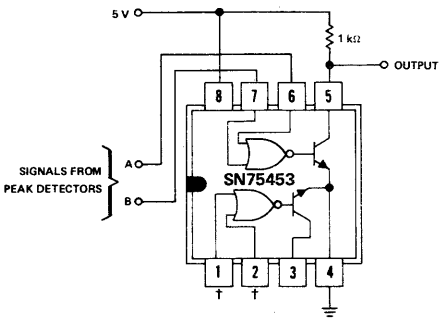
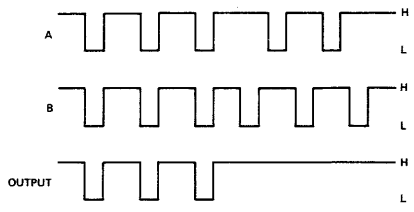
TYPICAL APPLICATION DATA





Low output occurs only when inputs are low simultaneously.

†If inputs are unused, they should be connected to +5 V through a 1 kΩ resistor.

FIGURE 32–IN-PHASE DETECTOR

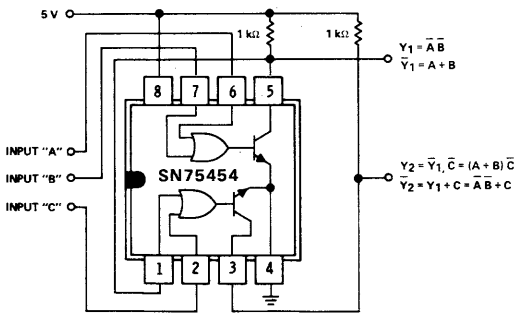


FIGURE 33–MULTIFUNCTION LOGIC-SIGNAL COMPARATOR

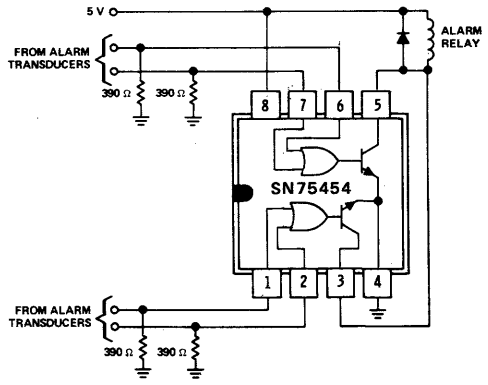


FIGURE 34–ALARM DETECTOR

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TYPES TID21A THRU TID26A, TID29A, TID30A, TID121 THRU TID126, TID129 THRU TID134 EPITAXIAL PLANAR SILICON DIODE ARRAYS

CORE-DRIVER DIODE ARRAYS

For Application With

- Magnetic Cores
- Plated-Wire Memories
- Thin-Film Memories
- Decoding or Encoding Applications

For Use In

- Airborne Computers
- Military Computers
- Industrial Computers
- Peripheral Equipment

description

3

These diode arrays are multiple diode junctions fabricated by a planar process and mounted in integrated circuit packages for use in high-current, fast-switching core-driver applications. These arrays offer many of the advantages of integrated circuits such as high-density packaging and improved reliability. These advantages result from such factors as fewer connections, more uniform device parameters, smaller size, less weight, fewer glass-to-metal seals, and the elimination of pressure contacts and whiskers.

The arrays are available in hermetically sealed, welded flat packages or in dual-in-line plastic packages.

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

	FLAT PACKAGE			DUAL-IN-LINE PACKAGE			UNIT
	EACH DIODE		TOTAL DEVICE	EACH DIODE		TOTAL DEVICE	
8-DIODE ARRAYS (COMMON CATHODE) 8-DIODE ARRAYS (COMMON ANODE) 16-DIODE ARRAYS DUAL 10-DIODE ARRAYS DUAL 8-DIODE ARRAYS	TID21A TID23A TID25A TID29A TID131	TID22A TID24A TID26A TID30A TID132	ALL TYPES	TID121 TID123 TID125 TID129 TID133	TID122 TID124 TID126 TID130 TID134	ALL TYPES	
Peak Reverse Voltage (See Note 1)	60	40		60	40		V
Steady-State Reverse Voltage, V_R	40	25		40	25		V
Peak Forward Current at (or below) 25°C Free-Air Temperature (See Notes 1 and 2)	500†			500‡			mA
Continuous Forward Current at (or below) 25°C Free-Air Temperature (See Note 2)	300§			400¶			mA
Continuous Power Dissipation at (or below) 25°C Free-Air Temperature			500◇			600□	mW
Operating Free-Air Temperature Range	−65 to 150			−65 to 125			°C
Storage Temperature Range	−65 to 200			−65 to 150			°C
Lead Temperature 1/16 Inch from Case for 10 Seconds	300			260			°C

NOTES: 1. These values apply for 100-μs pulses, duty cycle ⩽ 20%.
2. The values shown for total device apply for any combination provided the ratings of individual diodes are not exceeded.

†Derate linearly to 150°C free-air temperature at the rate of 4 mA/°C.
‡Derate linearly to 125°C free-air temperature at the rate of 5 mA/°C.
§Derate linearly to 150°C free-air temperature at the rate of 2.4 mA/°C.
¶Derate linearly to 125°C free-air temperature at the rate of 4 mA/°C.
◇Derate linearly to 150°C free-air temperature at the rate of 4 mW/°C.
□Derate linearly to 125°C free-air temperature at the rate of 6 mW/°C.

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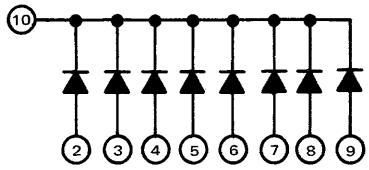
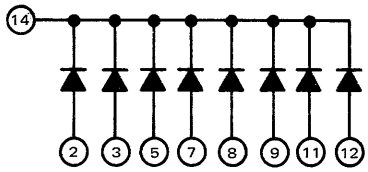
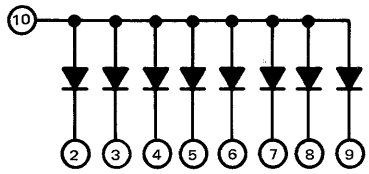
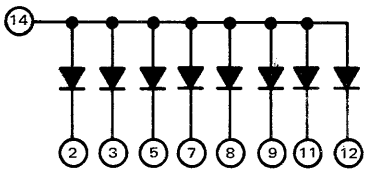
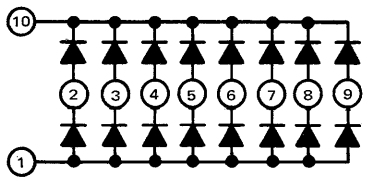
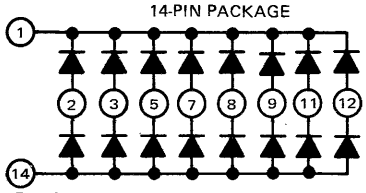
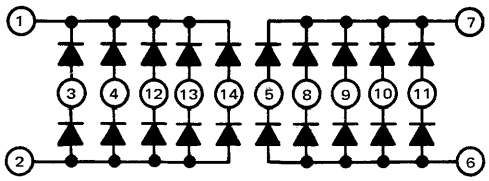
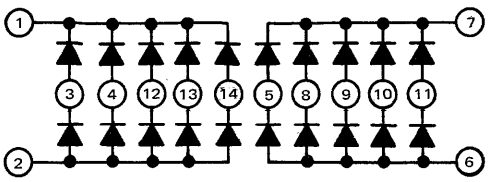
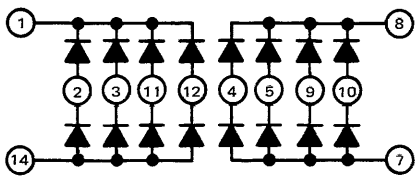
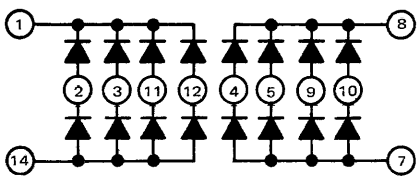
TYPES TID21A THRU TID26A, TID29A, TID30A, TID121 THRU TID126, TID129 THRU TID134 EPITAXIAL PLANAR SILICON DIODE ARRAYS

FLAT PACKAGES	14-PIN PLASTIC DUAL-IN-LINE PACKAGES
TID21A, TID22A 8-DIODE ARRAY (COMMON CATHODE) 10-PIN PACKAGE  (1) No internal connection	**TID121, TID122** 8-DIODE ARRAY (COMMON CATHODE) 14-PIN PACKAGE  (1) (4) (6) (10) (13) No internal connection
TID23A, TID24A 8-DIODE ARRAY (COMMON ANODE) 10-PIN PACKAGE  (1) No internal connection	**TID123, TID124** 8-DIODE ARRAY (COMMON ANODE) 14-PIN PACKAGE  (1) (4) (6) (10) (13) No internal connection
TID25A, TID26A 16-DIODE ARRAY 10-PIN PACKAGE 	**TID125, TID126** 16-DIODE ARRAY 14-PIN PACKAGE  (4) (6) (10) (13) No internal connection
TID29A, TID30A DUAL 10-DIODE ARRAY 14-PIN PACKAGE 	**TID129, TID130** DUAL 10-DIODE ARRAY 14-PIN PACKAGE 
TID131, TID132 DUAL 8-DIODE ARRAY 14-PIN PACKAGE  (6) (13) No internal connection	**TID133, TID134** DUAL 8-DIODE ARRAY 14-PIN PACKAGE  (6) (13) No internal connection

3

electrical characteristics at 25°C free-air temperature

single-diode operation (see note 3)

PARAMETER		TEST CONDITIONS	TID21A TID121	TID22A TID122	TID23A TID25A TID29A TID123 TID125 TID129 TID131 TID133	TID24A TID26A TID30A TID124 TID126 TID130 TID132 TID134	UNIT
			MIN MAX	MIN MAX	MIN MAX	MIN MAX	
$V_{(BR)}$	Reverse Breakdown Voltage	I_R = 10 μA	60	40	60	40	V
I_R	Static Reverse Current	V_R = 40 V, See Note 4	0.1		0.1		μA
		V_R = 25 V, See Note 4		0.1		0.1	μA
V_F	Static Forward Voltage	I_F = 100 mA	1	1.1	1	1.1	V
v_F	Instantaneous Forward Voltage	I_F = 500 mA, See Note 5	1.3	1.5	1.3	1.5	V
V_{FM}	Peak Forward Voltage	I_F = 500 mA, See Note 6	5	5	5	5	V
C_T	Total Capacitance†	V_R = 0, f = 1 MHz	4	4	8	8	pF

multiple-diode operation (see note 7)

PARAMETER		TEST CONDITIONS	ALL TYPES	UNIT
			MIN MAX	
I_{R1}	Static Reverse Current	V_{R1} = rated V_R, I_{FN} = 25 mA	10	μA
V_{F1}	Static Forward Voltage	I_{F1} = I_{FN} = 25 mA	1	V

switching characteristics at 25°C free-air temperature

single-diode operation (see note 3)

PARAMETER		TEST CONDITIONS	ALL TYPES	UNIT
			MIN MAX	
t_{fr}	Forward Recovery Time	I_F = 500 mA, See Figure 3	40	ns
t_{rr}	Reverse Recovery Time	I_F = 200 mA, I_{RM} = 200 mA, R_L = 100 Ω, i_{rr} = 20 mA, See Figure 4	20	ns

NOTES: 3. Test conditions and limits apply separately to each of the diodes. The diodes not under test are open-circuited during the measurement of these characteristics except for the measurement of I_R on arrays having both common-cathode and common-anode diodes (see Figures 1 and 2).

4. For arrays having both common-anode and common-cathode diodes see Figures 1 and 2, Parameter Measurement Information section.

5. This parameter is measured using pulse techniques. t_w = 300 μs, duty cycle = 2 %. Read time is 90 μs from the leading edge of the pulse.

6. The initial instantaneous value is measured using pulse techniques. t_w = 150 ns, duty cycle ⩽ 2%, pulse rise time ⩽ 10 ns. The total diode shunt capacitance is 19 pF maximum and the equipment bandwidth is 80 MHz.

7. Subscript numeral 1 refers to the diode under test; subscript N refers simultaneously to each of the other diodes in the section. Each diode is individually tested after the device reaches operating thermal equilibrium. Test conditions apply separately to common-anode and common-cathode sections.

†C_T is the total pin-to-pin capacitance measured across any of the diodes. For arrays having both common-anode and common-cathode sections, the interaction of the other diodes cannot easily be separated out unless three-terminal guarded measurement techniques are used. The actual capacitance of a single isolated diode will typically be 30% of the measured pin-to-pin value for the common-cathode diodes, and 75% of the measured value for the common-anode diodes.

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PARAMETER MEASUREMENT INFORMATION

When measuring the reverse current of an individual diode of a device having both common-anode and common-cathode sections, the current meter must be placed so that the shunt current through the other diodes is bypassed around the meter to obtain accurate readings, the voltage drop across the current meter must be less than 10 mV.

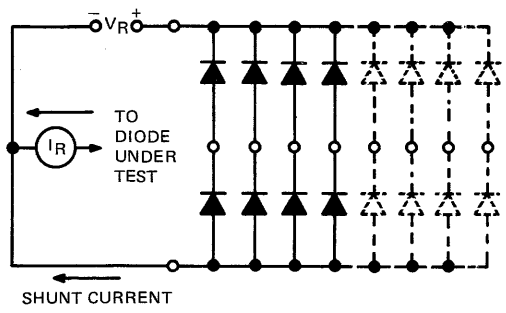


FIGURE 1–TEST CIRCUIT FOR COMMON-CATHODE DIODES

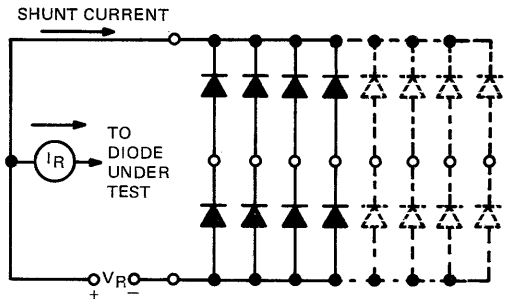
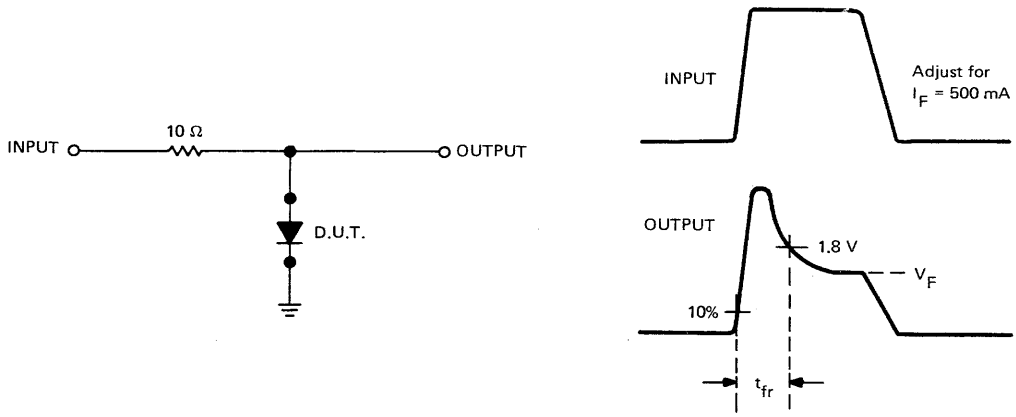


FIGURE 2–TEST CIRCUIT FOR COMMON-ANODE DIODES



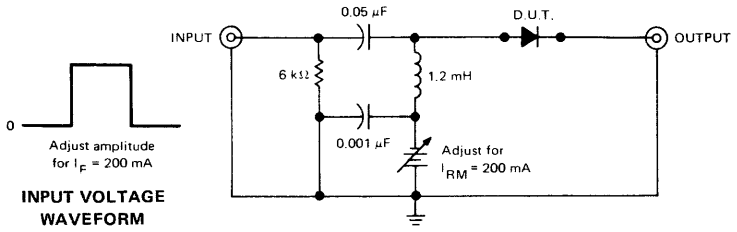
TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 3–FORWARD RECOVERY TIME

NOTES: a. The input pulse is supplied by a generator with the following characteristics: $t_r \leq 15$ ns, $Z_{out} = 50\ \Omega$, $t_w = 150$ ns, duty cycle $\leq 2\%$.

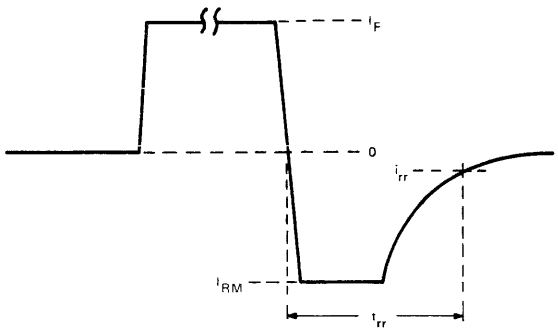
b. The output waveform is monitored on an oscilloscope with the following characteristics: $t_r \leq 4.5$ ns, $R_{in} \geq 1\ M\Omega$, $C_{in} \leq 5$ pF.

PARAMETER MEASUREMENT INFORMATION



INPUT VOLTAGE WAVEFORM

TEST CIRCUIT



OUTPUT CURRENT WAVEFORM

FIGURE 4–REVERSE RECOVERY TIME

NOTES: c. The input pulse is supplied by a generator with the following characteristics: $t_f \leq 1$ ns, $Z_{out} = 50\ \Omega$, $t_w = 200$ ns, duty cycle $\leq 1\%$.

d. The output waveform is monitored on an oscilloscope with the following characteristics: $t_r \leq 0.4$ ns, $R_{in} = 50\ \Omega$.

TYPICAL CHARACTERISTICS

FORWARD CONDUCTION CHARACTERISTICS

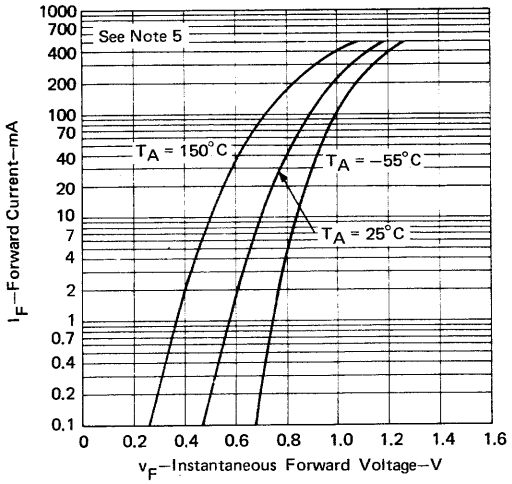


FIGURE 5

NOTE 5: This parameter is measured using pulse techniques. $t_w = 300\ \mu s$, duty cycle = 2%. Read time is 90 μs from the leading edge of the pulse.

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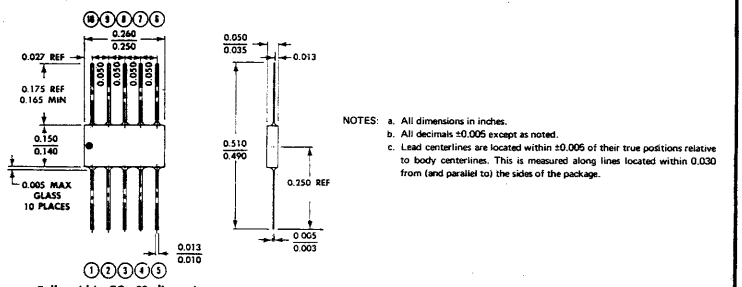
MECHANICAL DATA

flat packages

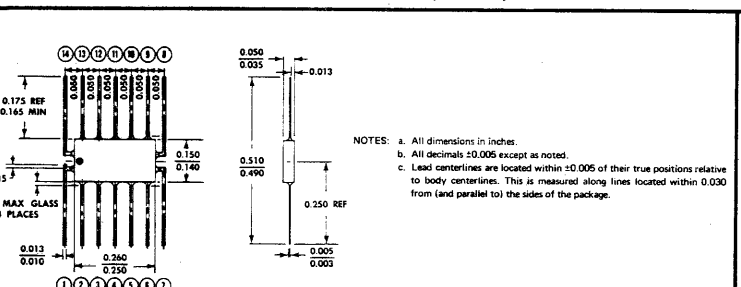
These hermetic packages feature glass-to-metal seals and welded construction in 10-pin and 14-pin configurations. Package body and leads are gold-plated F-15‡ glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic.

TID21A, TID22A, TID23A, TID24A, TID25A, TID26A



NOTES: a. All dimensions in inches.
b. All decimals ±0.005 except as noted.
c. Lead centerlines are located within ±0.005 of their true positions relative to body centerlines. This is measured along lines located within 0.030 from (and parallel to) the sides of the package.

TID29A, TID30A, TID131, TID132

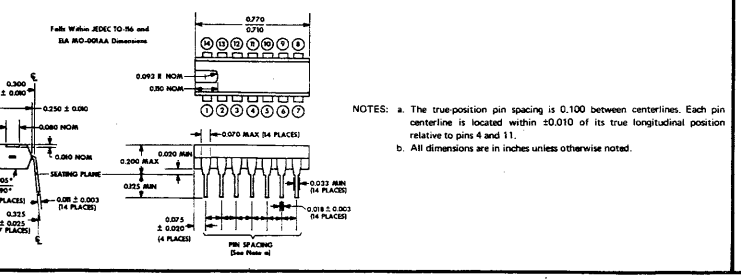


NOTES: a. All dimensions in inches.
b. All decimals ±0.005 except as noted.
c. Lead centerlines are located within ±0.005 of their true positions relative to body centerlines. This is measured along lines located within 0.030 from (and parallel to) the sides of the package.

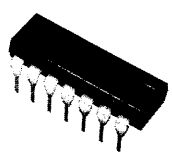
plastic dual-in-line package

The compound used to mold the dual-in-line package will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. These packages are intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. The silver-plated leads require no additional cleaning or processing when used in soldered assembly.

TID121, TID122, TID123, TID124, TID125, TID126, TID129, TID130, TID133, TID134



NOTES: a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins 4 and 11.
b. All dimensions are in inches unless otherwise noted.

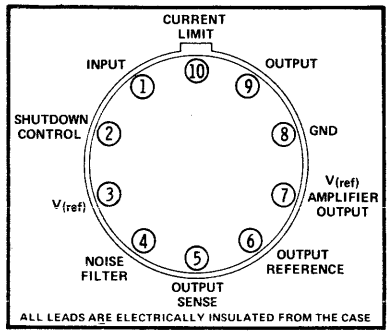


‡F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

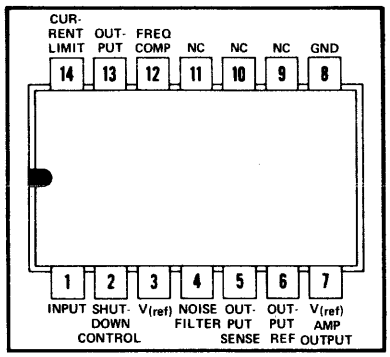
CIRCUIT TYPE SN72400
VOLTAGE REGULATOR

- 200-mA Load Current without External Power Transistor
- Remote Shutdown Control
- Adjustable Short-Circuit Current Limiter
- Input Voltages to 40 Volts
- Output Adjustable from 2 to 37 Volts

L
PLUG-IN PACKAGE (TOP VIEW)



N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection

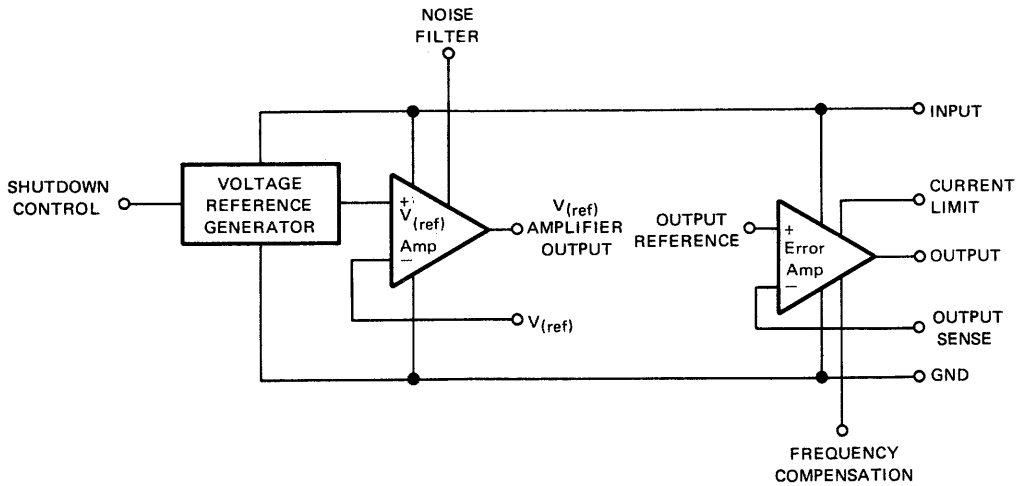
description

The SN72400 voltage regulator is a monolithic integrated circuit featuring a versatile circuit configuration and excellent performance specifications. A temperature-compensated power supply may be constructed by the addition of only two resistors to set the desired output voltage and two capacitors.

The circuit consists of a temperature-compensated reference voltage generator, a reference voltage amplifier, an error amplifier, a 200-milliampere output transistor, a remote shutdown circuit, and an adjustable output current limiter. The device features high ripple rejection, excellent input and load regulation, low temperature sensitivity, and low standby current. The SN72400 is designed for use in positive or negative power supplies as a series, shunt, switching, or floating regulator.

3

functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Input voltage (see Note 1)	40 V
Input-output voltage differential	40 V
Load current	200 mA
$V_{(ref)}$ amplifier output current	5 mA
Shutdown control voltage (see Notes 1 and 2)	V_I or 10 V
Power dissipation at (or below) 50°C free-air temperature (see Note 3)	800 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds, L package	300°C
Lead temperature 1/16 inch from case for 10 seconds, N package	260°C

NOTES: 1. Voltage values, except input-output voltage differential, are with respect to the network ground terminal.
2. The shutdown control voltage must never exceed the amount of the input voltage or 10 volts, whichever is less.
3. Power dissipation = $(I_I - I_O)\,V_I + (V_I - V_O)\,I_O$. For devices in the L package operating above 50°C free-air temperature, derate linearly at the rate of 8 mW/°C. No derating is required for devices in the N package.

3

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I	8.5	40	V
Output voltage, V_O	2	37	V
Input-to-output voltage differential, $V_I - V_O$	3		V
Output current, I_O	1	200	mA
Operating free-air temperature, T_A	0	70	°C

electrical characteristics (unless otherwise noted, T_A = 25°C, see Note 4)

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input regulation	1	$V_O \approx 5$ V, I_O = 1 mA, V_I = 12 V to 15 V		0.03%	0.1%	
Ripple rejection	3	Ripple frequency = 50 Hz to 10 kHz		60		dB
Load regulation	4	V_I = 15 V, $V_O \approx 10$ V, I_O = 1 mA to 50 mA, T_A = 0°C to 70°C, See Note 5		−0.03%	−0.1%	
Reference voltage, $V_{(ref)}$	1 or 2		2.1	2.3	2.5	V
Standby current	1	V_I = 40 V, I_O = 0		3	8	mA
Temperature coefficient of output voltage	1	T_A = 0°C to 70°C		±0.002		%/°C
Short-circuit output current	1 or 2	R_L = 0, R_{SC} = 7 Ω		91		mA
Output impedance	5	V_I = 14 V, f = 10 kHz		0.02		Ω
Output noise voltage	1	R1 = 0 Ω ($V_O \approx V_{(ref)}$), BW = 10 Hz to 5 MHz		0.1		mV
Minimum shutdown control voltage	6	V_I = 40 V, $I_O \leq 150\ \mu A$			2.4	V
Shutdown control current	6	V_I = 40 V, Shutdown control at 2.4 V		0.8	1.5	mA

NOTES: 4. Unless otherwise specified, V_I = 12 V, V_O = 8 V, I_O = 10 mA, C_N = 0.1 μF.
5. Load regulation is measured using pulsed techniques (t_w = 150 μs, duty cycle = 5%) to limit changes in internal power dissipation. Output voltage drift due to large changes in internal power dissipation must be taken into account separately.

CIRCUIT TYPE SN72400
VOLTAGE REGULATOR

DEFINITION OF TERMS

Input Regulation The percentage change in the output voltage for a specified change in the input voltage.

$$\text{Input Regulation} = \left[\frac{\Delta V_O}{V_O \text{ at } V_I = 12\text{ V}}\right] 100\%$$

Ripple Rejection The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Load Regulation The percentage change in the output voltage for a specified change in output current.

$$\text{Load Regulation} = \left(\frac{V_O \text{ at } I_{O(2)} - V_O \text{ at } I_{O(1)}}{V_O \text{ at } I_{O(1)}}\right) 100\%$$

where $I_{O(1)}$ and $I_{O(2)}$ are the specified low and high current extremes, respectively.

Standby Current The input current to the regulator with no load current.

3

Temperature Coefficient of Output Voltage (α_{VO}) The ratio of the difference between the highest and lowest values of output voltage for the full temperature range to the output voltage at 25°C, expressed as a percentage and averaged over the full temperature range.

$$\alpha_{VO} = \pm\left[\frac{V_O \text{ max} - V_O \text{ min}}{V_O \text{ at } 25^\circ\text{C}}\right] \frac{100\%}{70^\circ\text{C}}$$

Short-Circuit Output Current The output current of the regulator with the output shorted to ground.

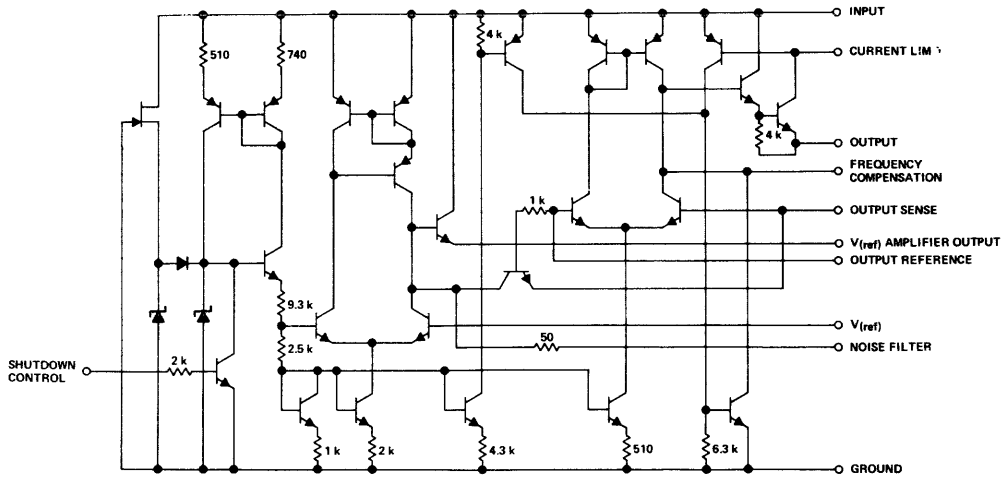
Output Impedance The ratio of a-c rms output voltage to the a-c rms output current.

Output Noise Voltage The rms output noise voltage with a constant load and no input ripple.

Minimum Shutdown Control Voltage The lowest voltage at the shutdown control terminal which will cause the regulator output current to decrease to below a specified value.

Shutdown Control Current The current into the shutdown control terminal.

schematic



All resistor values are nominal in ohms.

NOTE: The frequency compensation terminal is not available on devices in the 10-pin plug-in package (outline L).

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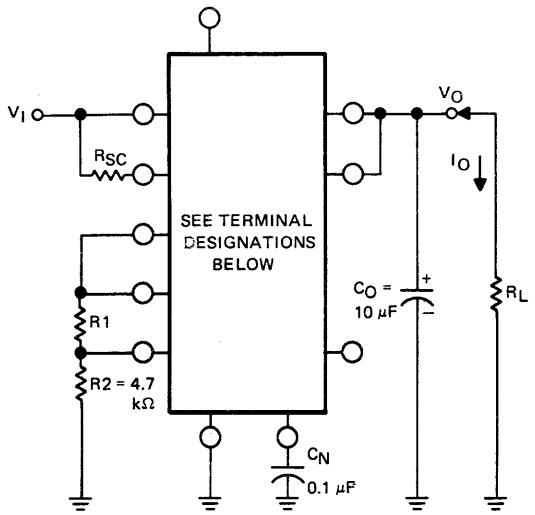
PARAMETER MEASUREMENT INFORMATION

BASIC REGULATOR CONFIGURATION
FOR $V_{(ref)} \leq V_O \leq 37$ V



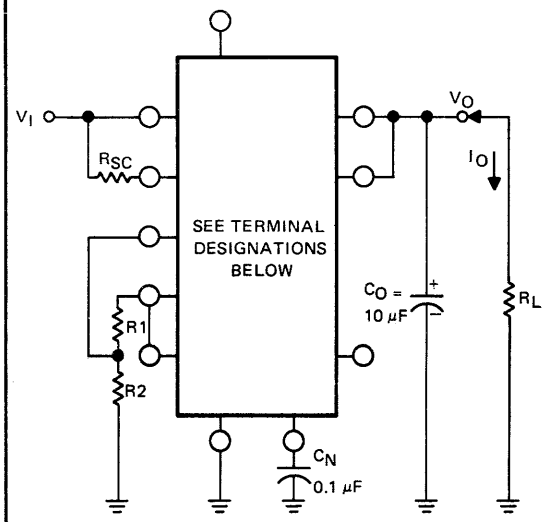
$$V_O = \frac{R1 + R2}{R2} V_{(ref)}$$

For $V_{(ref)} = 2.35$ V and R2 = 4.7 kΩ:

$$R1 = \left(2 \frac{k\Omega}{V}\right) V_O - 4.7\ k\Omega$$

FIGURE 1

BASIC REGULATOR CONFIGURATION
FOR $2\ V \leq V_O \leq V_{(ref)}$



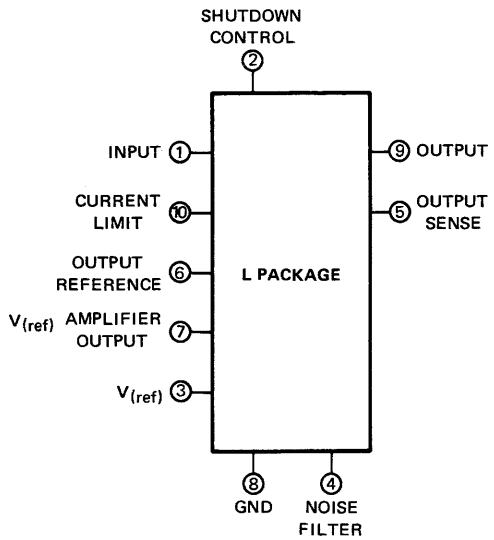
$$V_O = \frac{R2}{R1 + R2} V_{(ref)}$$

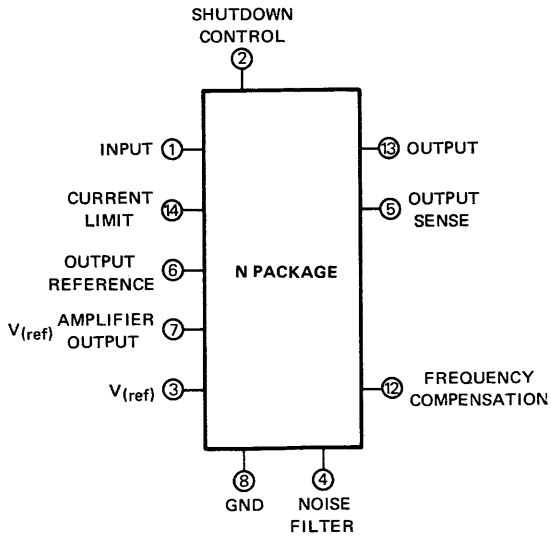
For $V_{(ref)} = 2.35$ V:

$R2 \approx (2\ V_O)\ k\Omega$; $R1 \approx 4.7\ k\Omega - R2$

FIGURE 2

TERMINAL DESIGNATIONS





For basic regulator configurations, test circuits, and applications circuits appearing in this data sheet, terminal functions are defined by their relative positions as shown in the drawings above.

PARAMETER MEASUREMENT INFORMATION

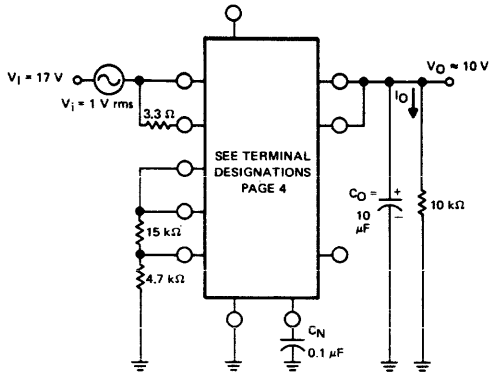


FIGURE 3–RIPPLE REJECTION

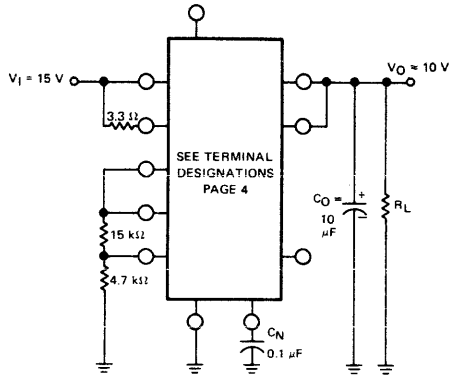


FIGURE 4–LOAD REGULATION

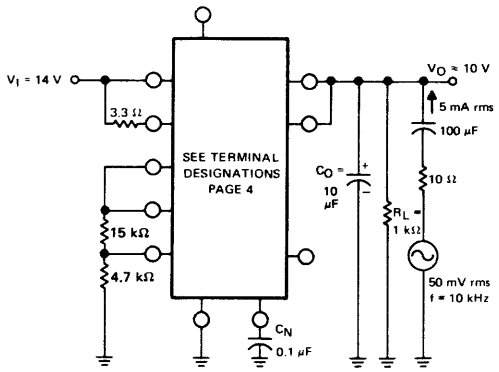


FIGURE 5–OUTPUT IMPEDANCE

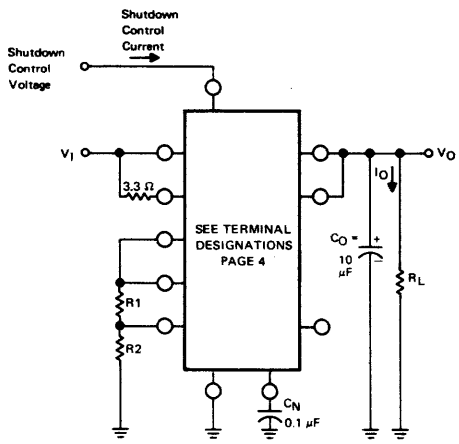


FIGURE 6–SHUTDOWN CONTROL VOLTAGE AND CURRENT

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TYPICAL CHARACTERISTICS

INPUT REGULATION
vs
INPUT-TO-OUTPUT
VOLTAGE DIFFERENTIAL

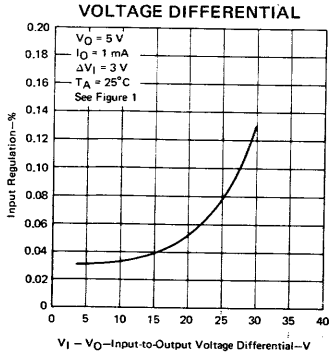

FIGURE 7

LOAD REGULATION
vs
INPUT-TO-OUTPUT
VOLTAGE DIFFERENTIAL

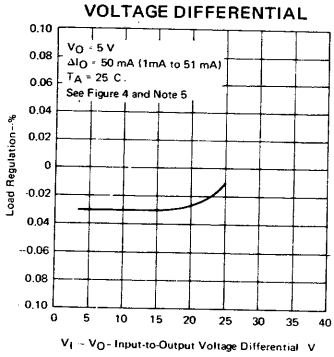

FIGURE 8

STANDBY CURRENT
vs
INPUT VOLTAGE

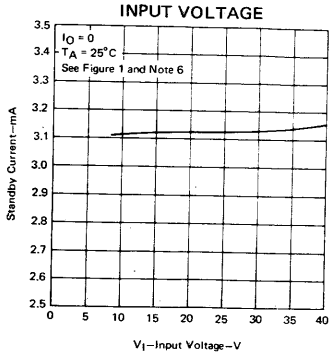

FIGURE 9

3

CURRENT LIMITING
CHARACTERISTICS

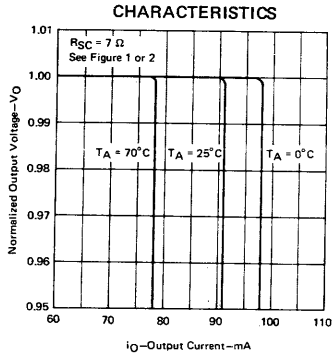

FIGURE 10

OUTPUT IMPEDANCE
vs
FREQUENCY

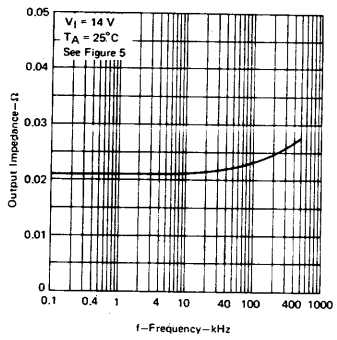

FIGURE 11

TRANSIENT RESPONSE
for
CHANGE IN INPUT VOLTAGE

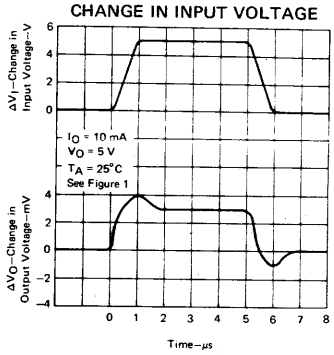

FIGURE 12

TRANSIENT RESPONSE
for
CHANGE IN OUTPUT CURRENT

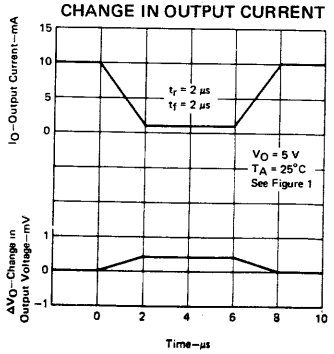

FIGURE 13

TRANSIENT RESPONSE
for
CHANGE IN OUTPUT CURRENT

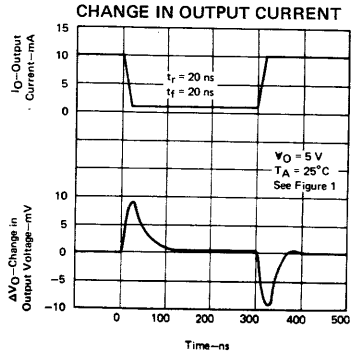

FIGURE 14

THERMAL CHARACTERISTICS

MAXIMUM OUTPUT CURRENT
vs
INPUT-TO-OUTPUT
VOLTAGE DIFFERENTIAL

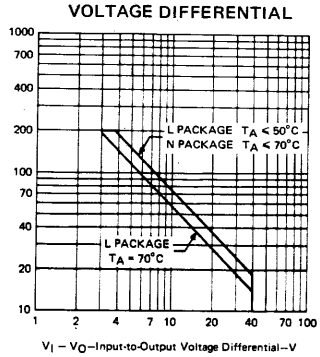

FIGURE 15

NOTES:

5. Load regulation is measured using pulsed techniques (t_w = 150 μs, duty cycle = 5%) to limit changes in internal power dissipation. Output voltage drift due to large changes in internal power dissipation must be taken into account separately.
6. $V_{(ref)}$ amplifier output current is 0.5 mA.

TYPICAL APPLICATION DATA

output voltage

Figures 1 and 2 show basic positive voltage regulator configurations for output voltages from 2 volts to 37 volts. For an adjustable output voltage, make R1 in Figure 1 a potentiometer with a maximum resistance of:

$$R1\ (max) \geq \left(2\frac{k\Omega}{V}\right)(V_O\ max) - 4.7\ k\Omega$$

See Figure 16 for the basic negative voltage regulator connections.

short-circuit output current limiting

The maximum output current, I_{OS}, is determined by the magnitude of resistor R_{SC} which is connected between the input and current limit terminals. Select $R_{SC} \approx 0.63$ volts/I_{OS} in amperes.

noise filter capacitor, C_N

3

A 0.1-μF capacitor from the noise filter terminal to ground will reduce the output noise voltage to typically below 100 μV (rms). The capacitance value can be increased or decreased depending on the application requirements, but a minimum value of 0.001 μF is recommended.

frequency compensation

The compensation technique shown in Figures 1 through 6 (10-μF capacitor, C_O, from the output terminal to ground) is used for optimum transient response. The 14-pin N plastic package provides a separate frequency compensation terminal and, for most applications, a 0.001-μF capacitor from the frequency compensation terminal to the output sense terminal (C_C) is adequate compensation. Larger values of C_C will degrade pulse response and output impedance characteristics and smaller values will reduce stability.

shutdown control

A d-c voltage (2.4 V minimum) applied to the shutdown control terminal will effectively turn off the regulated output voltage, thereby eliminating power consumption by output loading circuitry and greatly reducing the regulator standby current. Standard TTL or DTL IC logic circuits driving the shutdown control terminal can be used to turn the regulator on and off.

CONNECTION FOR A NEGATIVE OUTPUT VOLTAGE

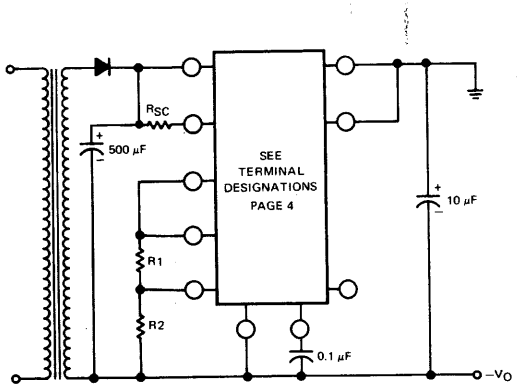

FIGURE 16

POSITIVE VOLTAGE REGULATOR WITH EXTERNAL N-P-N OUTPUT TRANSISTOR

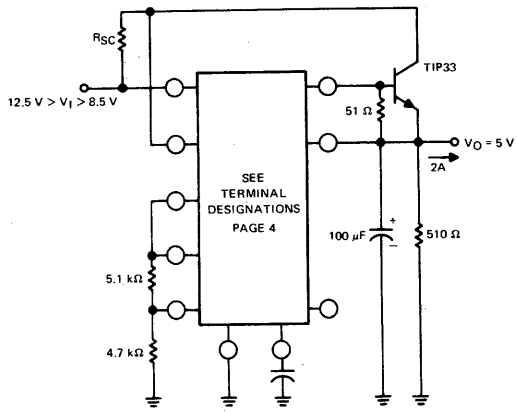

FIGURE 17

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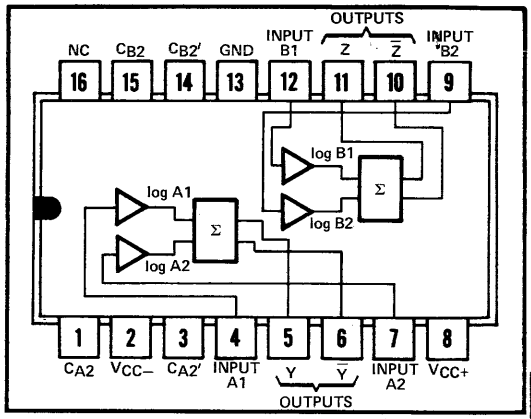
CIRCUIT TYPES SN56502, SN76502 LOGARITHMIC AMPLIFIERS

- Excellent Dynamic Range
- Wide Bandwidth
- Built-In Temperature Compensation
- Log Linearity (30 dBV Sections) . . . 1 dBV
- Wide Input Voltage Range

J OR N
DUAL-IN-LINE PACKAGES (TOP VIEW)



3

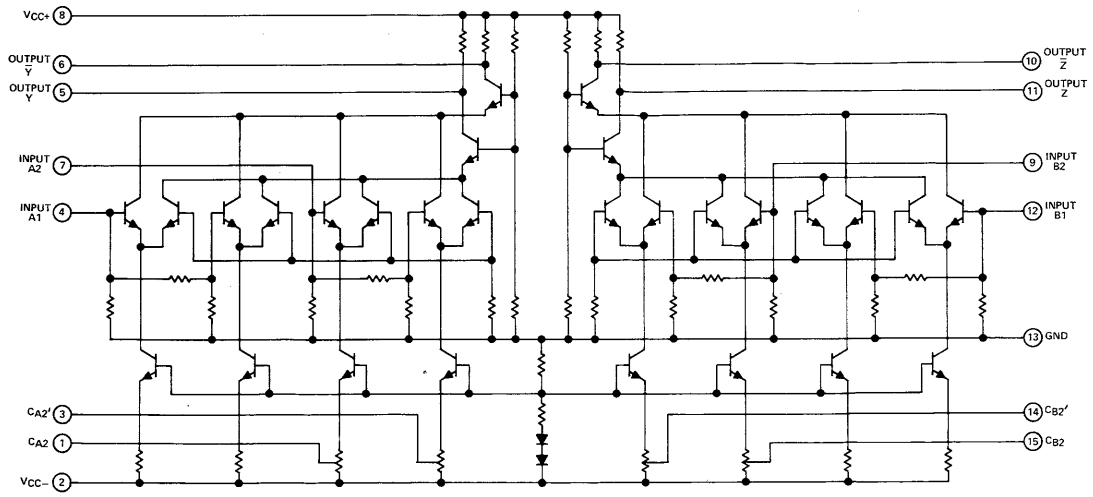
Y∝ log A1 + log A2; Z∝ log B1 + B2
where: A1, A2, B1, and B2 are in dBV, 0 dBV = 1 V.
C_{A2}, $C_{A2'}$, C_{B2}, and $C_{B2'}$, are detector compensation inputs.
NC—No internal connection

description

This monolithic logarithmic amplifier circuit contains four 30-dBV log stages. Gain in each stage is such that the output of each stage is proportional to the logarithm of the input voltage over the 30-dBV input voltage range. Each half of the circuit contains two of these 30-dBV stages summed together in one differential output which is proportional to the sum of the logs of the input voltages of the two stages. The four stages may be interconnected to obtain a theoretical input voltage range of 120 dBV. In practice, this permits the input voltage range to be typically greater than 80 dBV with log linearity of ±0.5 dBV (see application data). Bandwidth is from dc to 40 megahertz.

These circuits are useful in military weapons systems, broadband radar, and infrared reconnaissance systems. They serve for data compression and analog compensation. The logarithmic amplifiers are used in log IF circuitry as well as video and log amplifiers. The SN56502 is characterized for operation over the full military temperature range of –55°C to 125°C; the SN76502 is characterized for operation from 0°C to 70°C.

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltages (see Note 1):
- V_{CC+} 8V
- V_{CC-} . . . . . −8V

Input voltage (see Note 1) 6V
Output sink current (any one output) . . . . . 30 mA
Continuous total power dissipation . . . . . 500 mW
Operating free-air temperature range: SN56502 Circuits . . . . . −55°C to 125°C
SN76502 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

Note 1: All voltage values, except differential output voltages, are with respect to network ground terminal.

recommended operating conditions

	SN56502			SN76502			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Input voltage for each 30-dBV stage	0.01		1	0.01		1	V_{p-p}
Operating free-air temperature, T_A	−55	25	125	0	25	70	°C

3

electrical characteristics, V_{CC+} = 6 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST FIGURE	SN56502			SN76502			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Differential output offset voltage	1		±25	±60		±40		mV
Quiescent output voltage	2	5.45	5.6	5.85	5.45	5.6	5.85	V
D-c scale factor (differential output), each 30-dBV stage, −35 dBV to −5 dBV	3	7	8	10	6	8	12	mV/dBV
A-c scale factor (differential output)			8			8		mV/dBV
D-c error at −20 dBV (midpoint of −35 dBV to −5 dBV range)	3		1	2		1		dBV
Input impedance			500			500		Ω
Output impedance			200			200		Ω
Rise time, 10% to 90% points, C_L = 24 pF	4		20	25		20	25	ns
Supply current from V_{CC+}	2	14.5	18.5	23	14.5	18.5	23	mA
Supply current from V_{CC-}	2	−6	−8.5	−10.5	−6	−8.5	−10.5	mA
Power dissipation	2	123	162	201	123	162	201	mW

PARAMETER MEASUREMENT INFORMATION

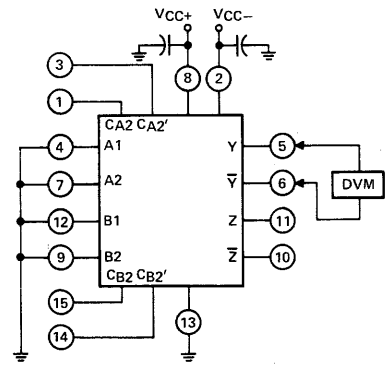


FIGURE 1

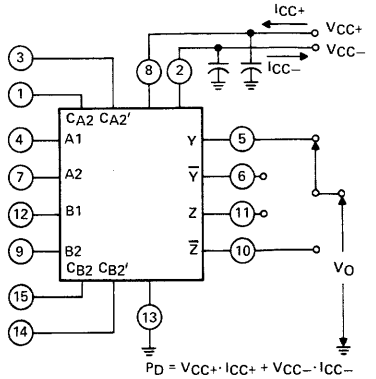


FIGURE 2

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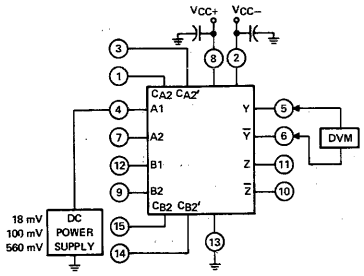
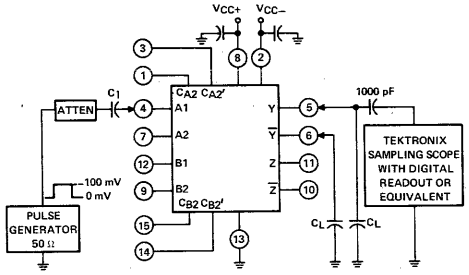
PARAMETER MEASUREMENT INFORMATION



$$\text{Scale Factor} = \frac{[V_{out(560\ mV)} - V_{out(18\ mV)}]\ mV}{30\ dBV}$$

$$\text{Error} = \frac{|V_{out(100\ mV)} - 0.5\,V_{out(560\ mV)} - 0.5\,V_{out(18\ mV)}|}{\text{Scale Factor}}$$

FIGURE 3



NOTES: A. The input pulse has the following characteristics: t_W = 50 ns, $t_r \leqslant 2$ ns, $t_f \leqslant 2$ ns, PRR = 10 MHz.

B. Capacitor C_I consists of three capacitors in parallel: 1 μF, 0.1 μF, and 0.01 μF.

C. C_L includes probe and jig capacitance.

FIGURE 4

3

TYPICAL CHARACTERISTICS

SN56502

DIFFERENTIAL OUTPUT OFFSET VOLTAGE vs FREE-AIR TEMPERATURE

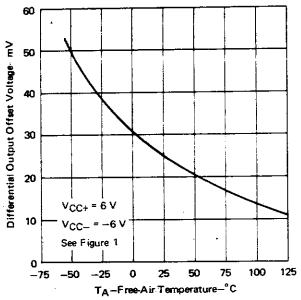


FIGURE 5

QUIESCENT OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

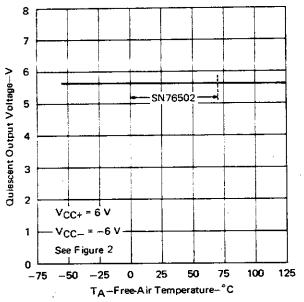


FIGURE 6

SN56502

D-C SCALE FACTOR vs FREE-AIR TEMPERATURE

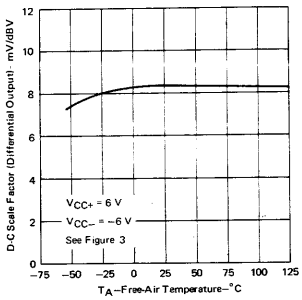


FIGURE 7

SN56502

D-C ERROR vs FREE-AIR TEMPERATURE

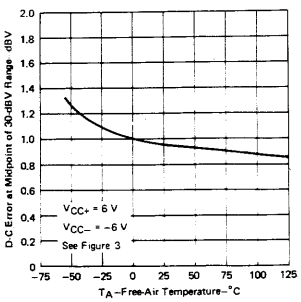


FIGURE 8

OUTPUT RISE TIME vs LOAD CAPACITANCE

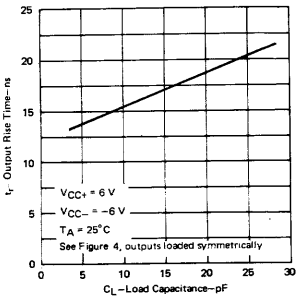


FIGURE 9

POWER DISSIPATION vs FREE-AIR TEMPERATURE

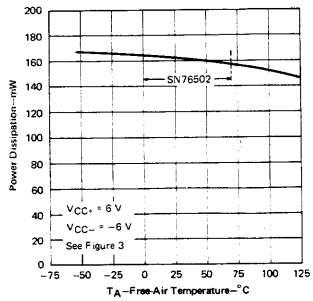


FIGURE 10

TYPICAL APPLICATION DATA

Although designed for high-performance applications such as broadband radar infrared detection, and weapons systems, this device has a wide range of applications in data compression and analog computation.

basic log function

The basic log response is derived from the exponential current-voltage relationship of collector current and base-emitter voltage. This relationship is given in the equation:

$$m \cdot V_{BE} = \ln [(I_C + I_{CES})/I_{CES}]$$

where: I_C = collector current
I_{CES} = collector current at $V_{BE} = 0$
$m = q/kT$ (in V^{-1})
V_{BE} = base-emitter voltage

The differential input amplifier allows dual-polarity inputs, is self-compensating for temperature variations, and is relatively insensitive to noise.

functional block diagram

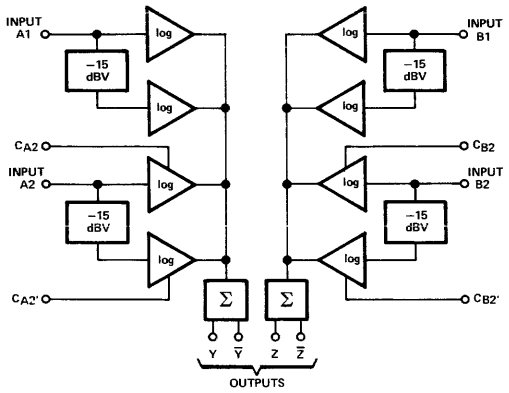


FIGURE 11

log sections

As can be seen from the schematic, there are eight differential pairs. Each pair is a 15-dBV log subsection, and each input feeds two pairs for a range of 30 dBV per stage.

Four compensation points are made available to allow slight variations in the gain (slope) of the two individual 15-dBV stages of input A2 and B2. By slightly changing the voltage on any of the compensation pins from its quiescent value, the gain of that particular 15-dBV stage can be adjusted to match the other 15-dBV stage in the pair. The compensation pins may also be used to match the transfer characteristics of input A2 to A1 or B2 to B1.

The log stages in each half of the circuit are summed by directly connecting their collectors together and summing through a common-base output stage. The two sets of output collectors are used to give two log outputs, Y and $\overline{Y}$ (or Z and $\overline{Z}$) which are equal in amplitude but opposite in polarity. This increases the versatility of the device.

By proper choice of external connections, linear amplification, linear attentuation, and many different applications requiring logarithmic signal processing are possible.

input levels

The recommended input voltage range of any one stage is given as 0.01 volt to one volt. Input levels in excess of one volt may result in a distorted output. When several log sections are summed together, the distorted area of one section overlaps with the next section and the resulting distortion is insignificant. However, there is a limit to the amount of overdrive that may be applied. As the input drive reaches ±3.5 volts, saturation occurs, clamping the collector-summing line and severely distorting the output. Therefore, the signal to any input must be limited to approximately ±3 volts to ensure a clean output.

output levels

Differential-output-voltage levels are low, generally less than 0.6 volt. As demonstrated in Figure 12, the output swing and the slope of the output response can be adjusted by varying the gain by means of the slope control. The coordinate origin may also be adjusted by positioning the offset of the output buffer.

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TYPICAL APPLICATION DATA

circuits

Figures 12 through 19 show typical circuits using these logarithmic amplifiers. Operational amplifiers not otherwise designated are SN52741 or SN72741. For operation at higher frequency, use of SN52733/SN72733 is recommended instead of SN52741/SN72741, with the differential outputs connected as in Figure 14. The SN5510/SN7510 or SN5511/SN7511 wideband amplifiers may also be used.

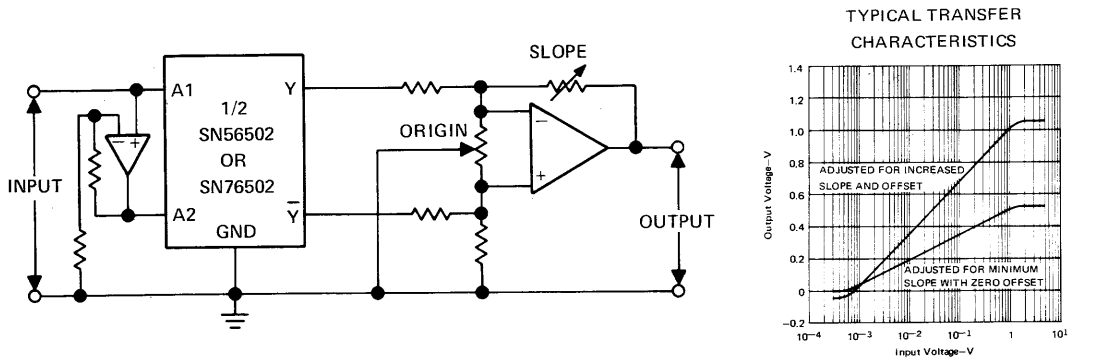


FIGURE 12–OUTPUT SLOPE AND ORIGIN ADJUSTMENT

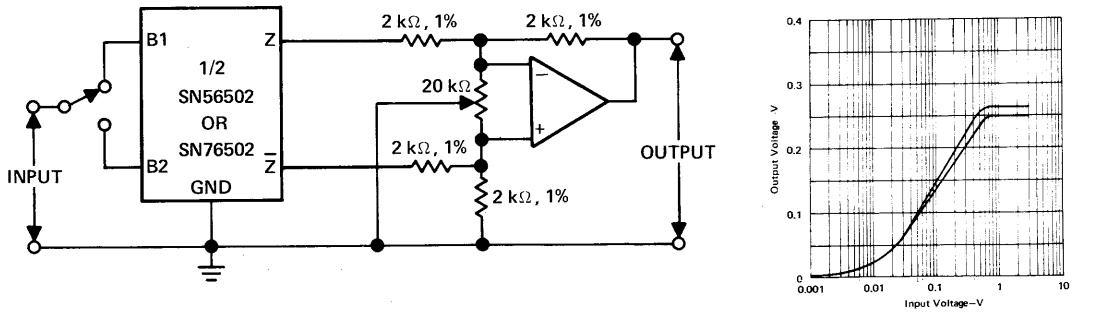


FIGURE 13–UTILIZATION OF SEPARATE STAGES

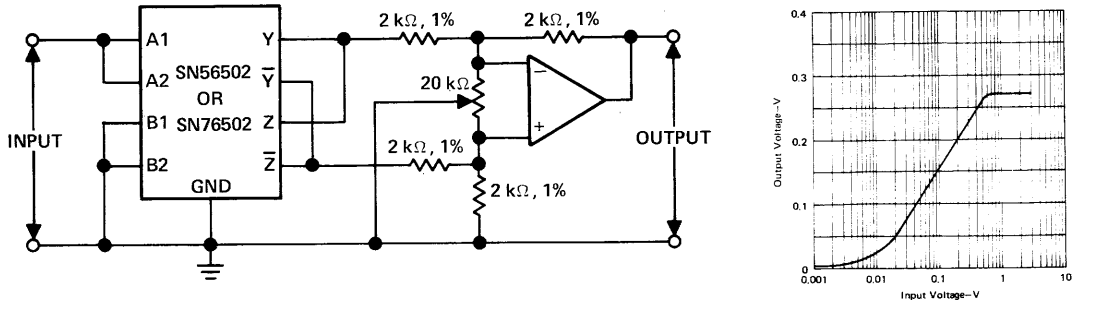
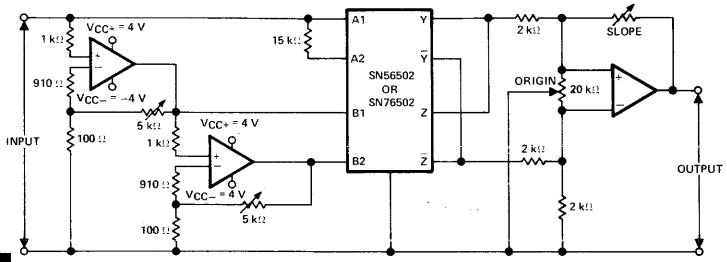
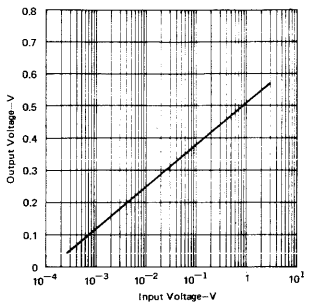


FIGURE 14–UTILIZATION OF PARALLELED INPUTS

TYPICAL APPLICATION DATA

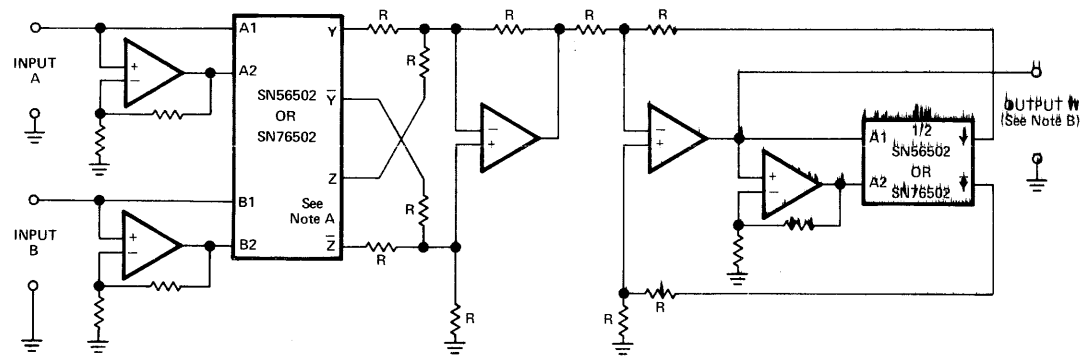


TRANSFER CHARACTERISTICS



NOTES: A. Inputs are limited by reducing the supply voltages for the input amplifiers to ±4 V.
B. The gains of the input amplifiers are adjusted to achieve smooth transitions.

FIGURE 15–LOGARITHMIC AMPLIFIER WITH INPUT VOLTAGE RANGE GREATER THAN 80 dB



NOTES: A. Connections shown are for multiplication. For division, Z and $\overline{Z}$ connections are reversed.
B. Output W may need to be amplified to give actual product or quotient of A and B.
C. R designates resistors of equal value, typically 2 kΩ to 10 kΩ.

Multiplication: $W = A \cdot B \Rightarrow \log W = \log A + \log B$, or $W = a^{(\log_a A + \log_a B)}$

Division: $W = A/B \Rightarrow \log W = \log A - \log B$, or $W = a^{(\log_a A - \log_a B)}$

FIGURE 16–MULTIPLICATION OR DIVISION

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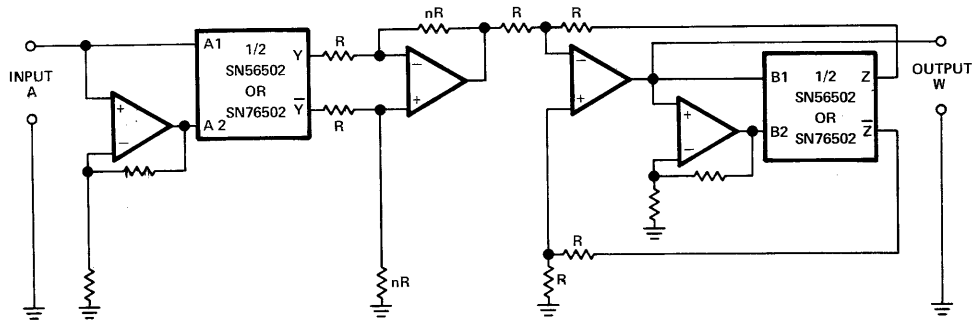
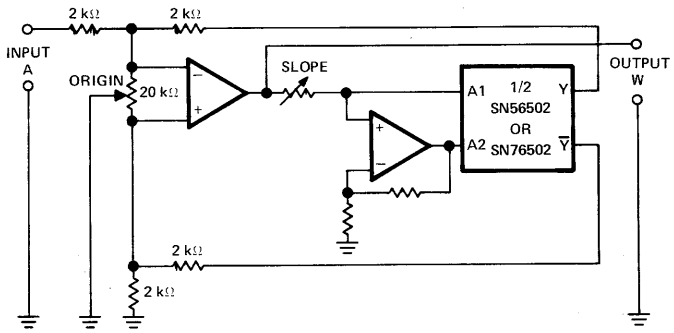
TYPICAL APPLICATION DATA



NOTE: R designates resistors of equal value, typically 2 kΩ to 10 kΩ. The power to which the input variable is raised is fixed by setting nR. Output W may need to be amplified to give the correct value.

Exponential: $W = A^n \Rightarrow \log W = n \log A$, or $W = a^{(n \log_a A)}$

FIGURE 17—RAISING A VARIABLE TO A FIXED POWER



NOTE: Adjust the slope to correspond to the base "a".

Exponential to any base: W = a

FIGURE 18—RAISING A FIXED NUMBER TO A VARIABLE POWER

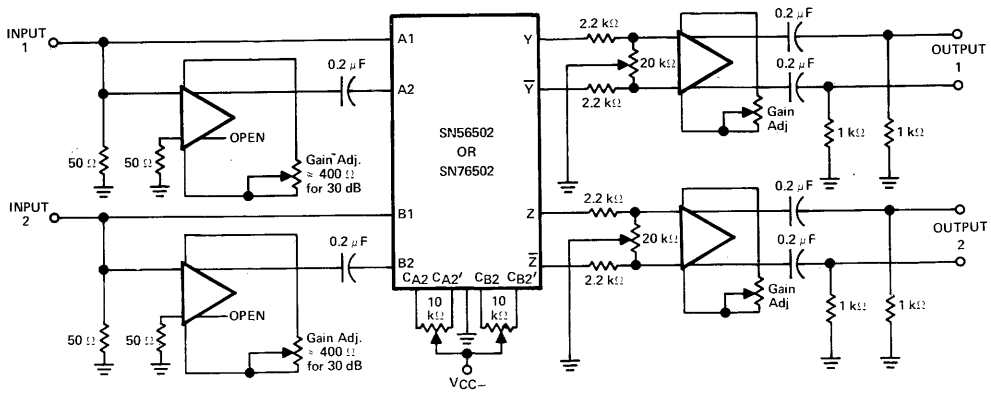


FIGURE 19—DUAL-CHANNEL RF LOGARITHMIC AMPLIFIER WITH 50-dB INPUT RANGE PER CHANNEL AT 10 MHz

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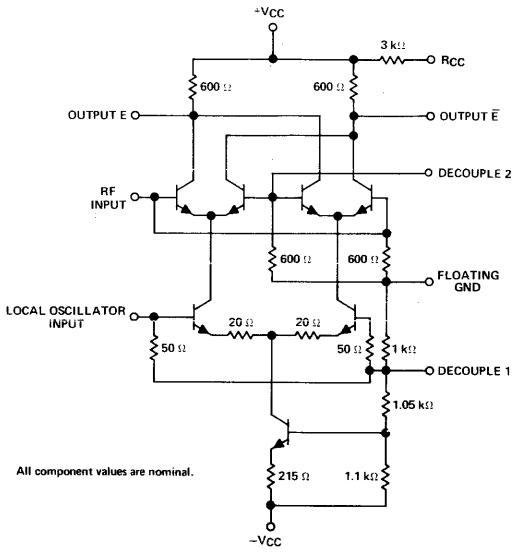
CIRCUIT TYPES SN56514, SN76514
BALANCED MIXERS

- Flat Response to 100 MHz
- Local Oscillator IF Isolation . . . 30 dB Typ
- Local Oscillator RF Isolation . . . 60 dB Typ
- RF-IF Isolation . . . 30 dB Typ
- Conversion Gain . . . 14 dB Typ
- Use with 12-V or ±6-V Power Supplies

schematic



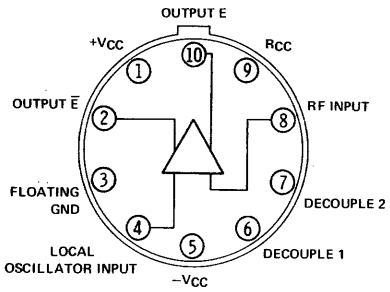
description

3

The SN56514 and SN76514 are doubly balanced mixers which utilize two cross-coupled, differential transistor pairs driven by a third balanced pair. The circuit features a flat response over a wide band of frequencies. The SN56514 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN76514 is characterized for operation from 0°C to 70°C.

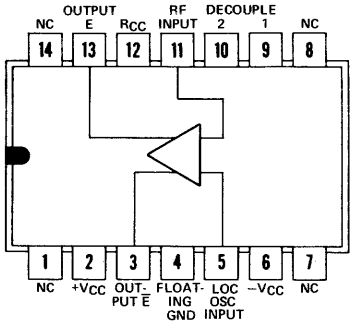
terminal assignments

L PLUG-IN PACKAGE
(TOP VIEW)



PIN 5 IS IN ELECTRICAL CONTACT WITH THE CASE

J AND N DUAL-IN-LINE PACKAGES
(TOP VIEW)



For operation from a single 12-V supply, connect the positive terminal of the supply to $+V_{CC}$, the negative terminal to $-V_{CC}$, and the floating-ground terminal to R_{CC}. For operation from two 6-V supplies, leave R_{CC} open and connect the positive terminal of one supply to $+V_{CC}$, the negative terminal of the other supply to $-V_{CC}$, and the remaining terminals of the two supplies to the floating-ground terminal. See Figure 19.

NC—No internal connection

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	18 V
Input voltage (see Notes 1 and 2)	7 V
Continuous output current (see Note 3)	10 mA
Continuous total power dissipation at (or below) 70°C free-air temperature (see Note 4)	500 mW
Operating free-air temperature range: SN56514 Circuits	−55°C to 125°C
SN76514 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		12		V
Local oscillator input voltage (see Note 5)		250	300	mV p-p
RF input voltage (see Note 5)		10	30	mV p-p
Operating free-air temperature range: SN56514 Circuits	−55	25	125	°C
SN76514 Circuits	0	25	70	°C

electrical characteristics at 25°C free-air temperature, V_{CC} = 12 V

PARAMETER		TEST FIGURE	TEST CONDITIONS	SN56514			SN76514			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Quiescent output voltage	1		9.6	10.5	11.3	9.6	10.5	11.3	V
I_{CC}	Supply current	1		5.5	7.4	10.9	5.5	7.4	10.9	mA
G_C	Conversion gain (single-ended output)	2	f_{RF} and f_{LO} = 100 kHz thru 40 MHz	11	14	17	11	14	17	dB
LOIFI	Local oscillator to IF isolation	3	f_{LO} = 100 kHz thru 40 MHz	15	29†			29†		dB
LORFI	Local oscillator to RF isolation	3	f_{LO} = 100 kHz thru 40 MHz	40	52†			52†		dB
RFIFI	RF to IF isolation	4	f_{RF} = 100 kHz thru 40 MHz	15	28†			28†		dB

†The typical values are at 40 MHz.

NOTES: 1. All d-c voltage values are with respect to $-V_{CC}$ terminal.
2. This rating applies to the local-oscillator input, RF input, and Decouple 2.
3. This value applies for both outputs simultaneously.
4. For operation of SN56514 above 70°C free-air temperature, refer to Dissipation Derating Curve, Figure 18.
5. All signal voltages are with respect to the floating-ground terminal. Alternatively, the RF input may be applied differentially between the RF input terminal and Decouple 2.

PARAMETER MEASUREMENT INFORMATION

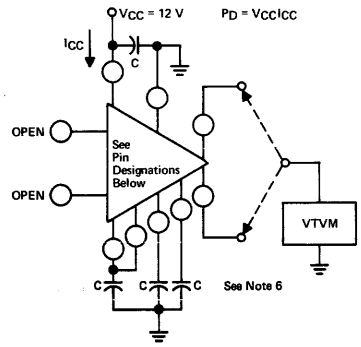


FIGURE 1–V_O, I_{CC}, and P_D

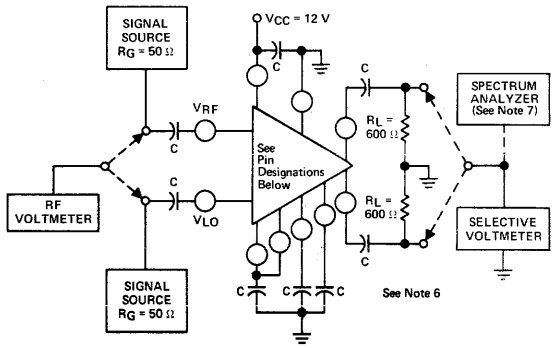


FIGURE 2–G_C

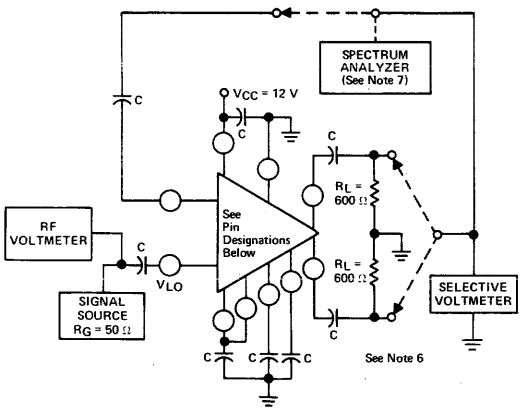


FIGURE 3–LOIFI and LORFI

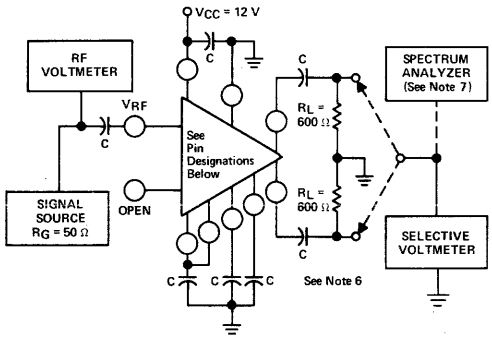
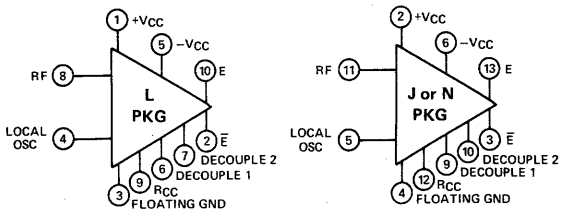


FIGURE 4–RFIFI

Pin Designations: For all test circuits appearing in this data sheet, terminal functions are defined by their relative positions as shown in the drawings in this block.



NOTES: 6. Capacitor C comprises the following capacitors in parallel: 1 μF, 0.1 μF, and 0.0015 μF.
7. The spectrum analyzer is used for frequencies above the normal range of the selective voltmeter.

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TYPICAL CHARACTERISTICS

QUIESCENT OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

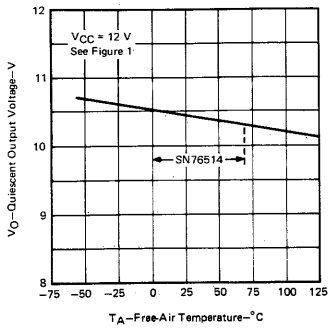

FIGURE 5

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

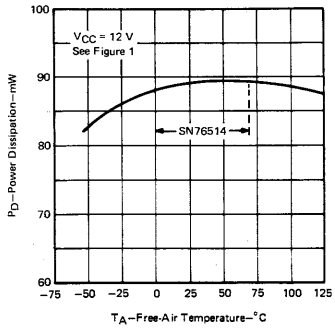

FIGURE 6

CONVERSION GAIN
vs
SUPPLY VOLTAGES

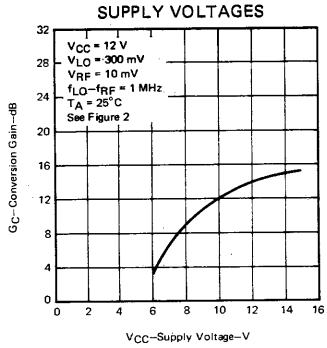

FIGURE 7

CONVERSION GAIN
vs
LOCAL OSCILLATOR VOLTAGE

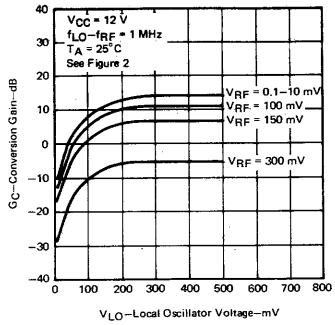

FIGURE 8

CONVERSION GAIN
vs
FREQUENCY

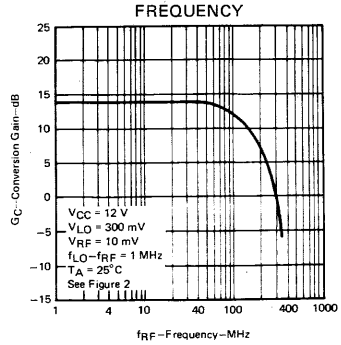

FIGURE 9

CONVERSION GAIN
vs
FREE-AIR TEMPERATURE

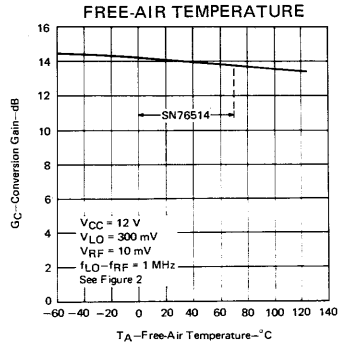

FIGURE 10

TYPICAL CHARACTERISTICS

LOCAL OSCILLATOR TO IF ISOLATION
vs
FREQUENCY

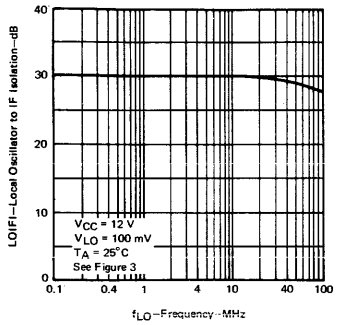

FIGURE 11

LOCAL OSCILLATOR TO IF ISOLATION
vs
FREE-AIR TEMPERATURE

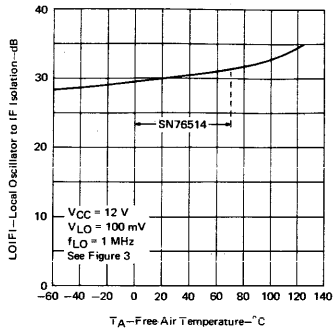

FIGURE 12

LOCAL OSCILLATOR TO RF ISOLATION
vs
FREQUENCY

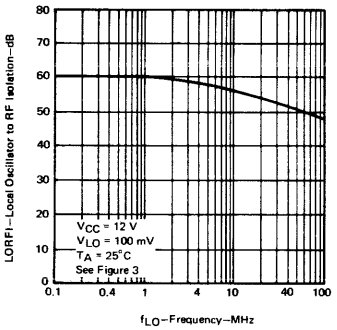

FIGURE 13

LOCAL OSCILLATOR TO RF ISOLATION
vs
FREE-AIR TEMPERATURE

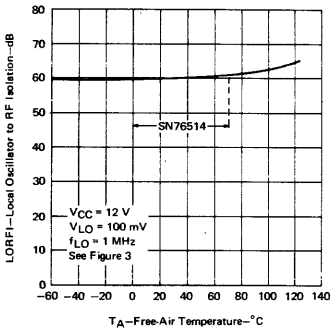

FIGURE 14

RF TO IF ISOLATION
vs
FREQUENCY

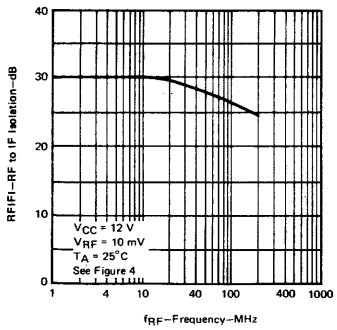

FIGURE 15

RF TO IF ISOLATION
vs
FREE-AIR TEMPERATURE

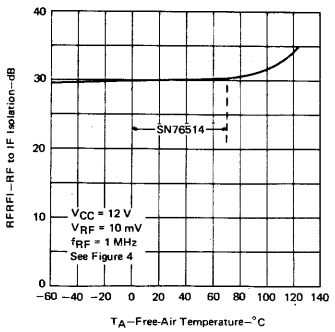

FIGURE 16

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TYPICAL CHARACTERISTICS

SIDEBAND HARMONIC SUPPRESSION
vs
LOCAL OSCILLATOR FREQUENCY

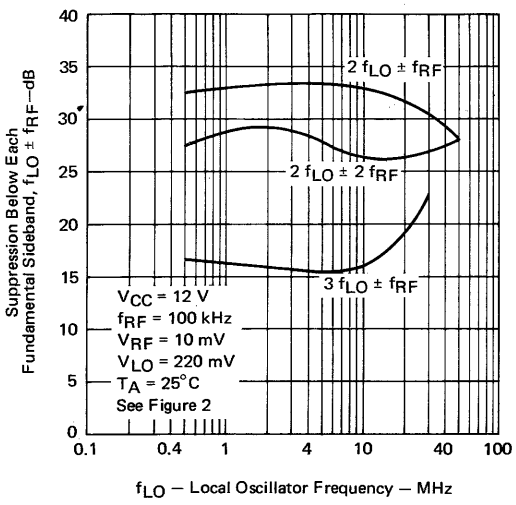


FIGURE 17

THERMAL INFORMATION

DISSIPATION DERATING CURVE

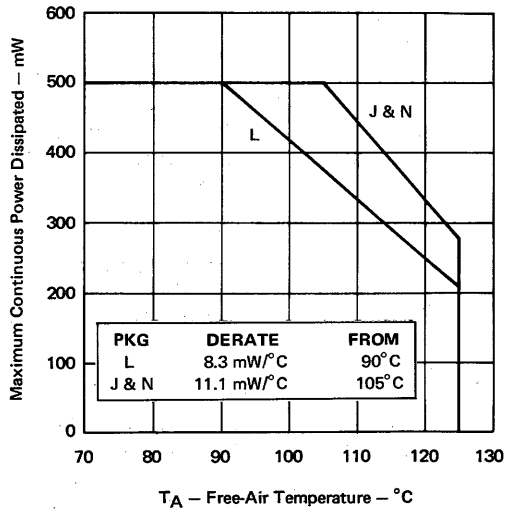


FIGURE 18

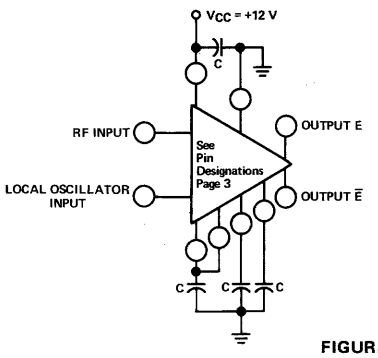
3

TYPICAL APPLICATION DATA

The SN55514 and SN75514 balanced mixers are designed to have considerable circuit flexibility which results in a wide range of applications. Typical applications include use as balanced modulators for sideband-suppressed-carrier generation, product detectors for demodulation, frequency converters, and frequency or phase modulators. In addition, the SN55514 and SN75514 may be used in control systems and analog computers as low-level multipliers or squaring circuits.

The circuits are designed to operate from either a single 12-V supply or two 6-V supplies. Electrical characteristics will be unchanged with the use of either power supply option. External bypass capacitors, as shown in Figure 19, should be used for optimum performance.

The mixer's electrical performance and the inherent IC advantages of size, reliability, and component matching make it very desirable for use in communication and control systems.



NOTE: Capacitor C comprises the following capacitors in parallel: 1 μF, 0.1 μF, and 0.0015 μF.

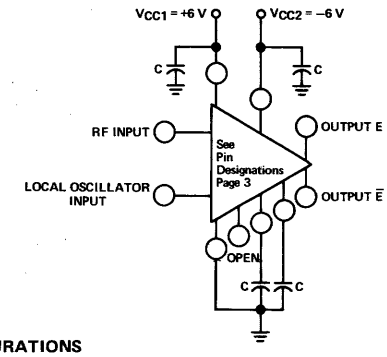


FIGURE 19—EXTERNAL CAPACITOR CONFIGURATIONS

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CONSUMER CIRCUITS SUMMARY

Following is a listing of Consumer Circuits presently available from Texas Instruments. Should you desire additional information, application engineering advice, or sales assistance, please contact your nearest TI Sales office.

AUDIO AMPLIFIERS

SN76001	1 W Audio at 9 V and 8 Ω
SN76003	3 W Audio at 30 V and 16 Ω
SN76010	Same as SN76001 except for different pin arrangement
SN76013	3 W Audio at 24 V and 8 Ω
SN76005	5 W Audio at 34 V and 16 Ω
SN76050	5 W Audio at 14 V and 4 Ω

DUAL CHANNEL AND STEREO

SN76104	Stereo Multiplex Decoder
SN76105	Stereo Multiplex Decoder
SN76110	Stereo Multiplex Decoder
SN76131	Stereo Preamplifier

CHROMA CIRCUITS

SN76242	Chroma Sub-carrier Regenerator
SN76243	Chroma Amplifier
SN76246	Chroma Demodulator
SN76630	PAL Chroma Demodulator

COMPLEX TV FUNCTIONS

SN76530	Video Detector
SN76532	TV Jungle (suitable for horizontal deflection with tubes)
SN76533	TV Jungle (suitable for horizontal deflection with semiconductors)
SN76540	TV Jungle for N-P-N Tuners and Ge Diode Detection
SN76541	TV Jungle for N-P-N Tuners and Low Level Detection
SN76542	TV Jungle for P-N-P Tuners and Ge Diode Detection
SN76564	Automatic Fine Tuning

REGULATORS FOR VARACTOR TUNERS

SN76550	33 V at 5 mA
SN76552	22 V at 5 mA
SN76553	12 V at 5 mA

IF CIRCUITS FOR RADIO AND TV

SN76600	1st and 2nd Video IF Stages
SN76603	RF/IF Amplifier
SN76619	RF Amplifier/FM Detector
SN76640	Sound IF/Limiter, Slope Detector, Audio Driver, Voltage Regulator
SN76641	IF Limiting Amplifier
SN76642	Sound IF/Detector
SN76643	Sound IF/Detector
SN76650	1st and 2nd Video IF with Keyed AGC
SN76660	Sound IF/Amplifier Limiter, Balanced Coincidence Detector, D-c Volume Control
SN76665	Sound IF/Amplifier Limiter, Detector, Attenuator, Audio Driver, Voltage Regulator
SN76670	SN76660 with Open-Collector Output
SN76680	SN76660 with Audio Driver and Voltage Regulator

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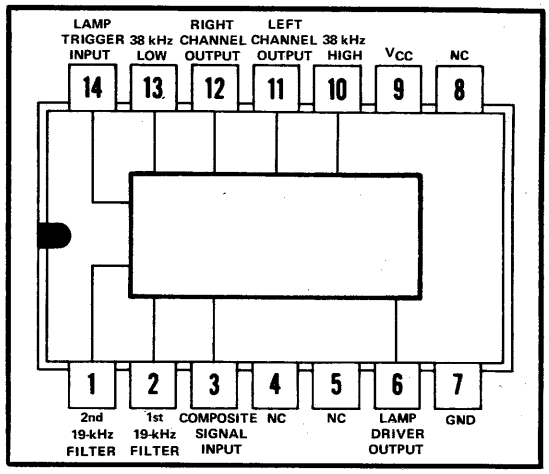
CIRCUIT TYPE SN76110 STEREO DEMODULATOR

FOR USE IN FM MULTIPLEX SYSTEMS

- Designed to be Interchangeable with Motorola MC1307P
- Power Supply Range . . . 8 to 14 V
- Low Harmonic Distortion
- Stereo-Indicator Lamp Driver
- Monaural Squelch Capability

N
DUAL-IN-LINE PACKAGE (TOP VIEW)



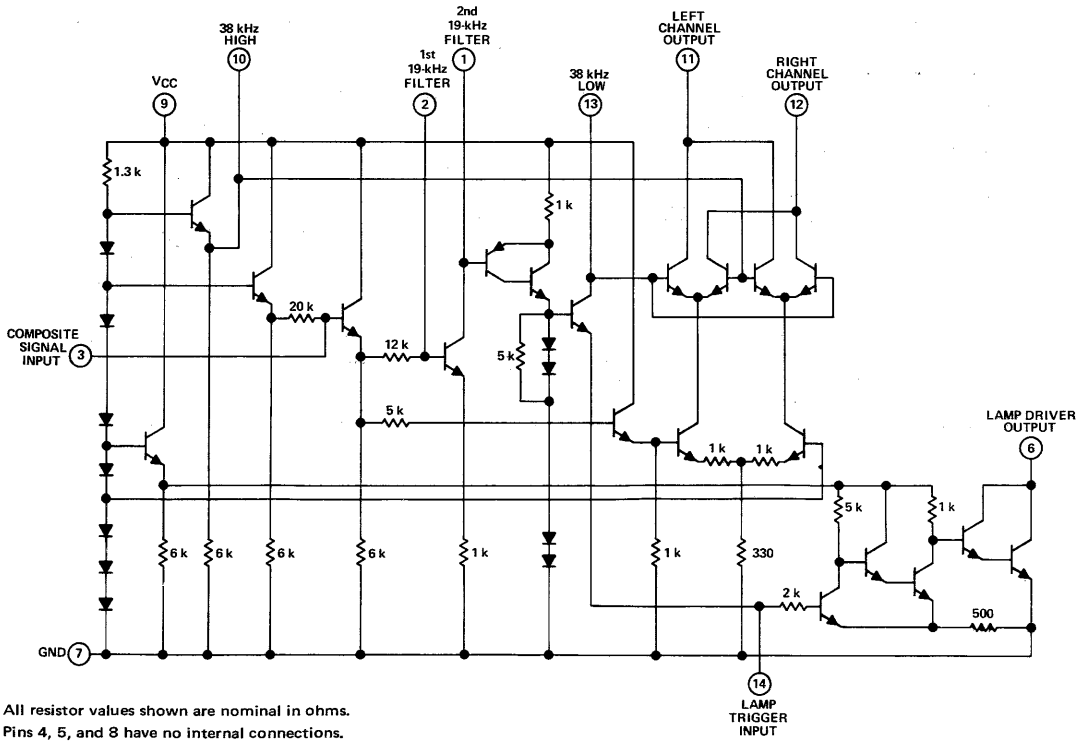
NC—No internal connection

description

The SN76110 is a monolithic integrated circuit designed to process the detected composite multiplex signal. The circuit provides left-channel and right-channel separation and balance, and also has a driver output for a stereo-indicator lamp.

3

schematic



All resistor values shown are nominal in ohms.
Pins 4, 5, and 8 have no internal connections.

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CIRCUIT TYPE SN76110
STEREO DEMODULATOR

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 22 V
Lamp driver current . . . . . 40 mA
Power dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 625 mW
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Derate linearly to 375 mW at 75°C free-air temperature at the rate of 5 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	8	12	14	V
Operating free-air temperature, T_A	0	25	75	°C

3

electrical characteristics (unless otherwise noted V_{CC} = 8 V to 14 V, T_A = 25°C, see figure 1)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Input impedance	f = 1 kHz			20		kΩ
Stereo channel separation	See Note 3	f_{mod} = 100 Hz		40		dB
		f_{mod} = 1 kHz	30	45		
		f_{mod} = 10 kHz		35		
Total harmonic distortion	f_{mod} = 1 kHz, See Notes 3 and 4			0.3%		
Channel balance	Monaural input = 200 mV rms			0.5	1	dB
Ultrasonic frequency rejection	See Note 5	f = 19 kHz		25		dB
		f = 38 kHz		20		
Inherent SCA rejection (without filter)	f_{mod} = 60 kHz to 74 kHz, See Notes 4 and 5 and Figure 2			55‡		dB
Minimum trigger input for on state at lamp-driver output	Trigger frequency = 19 kHz, R1 = 180 Ω			10	20	mV rms
Maximum trigger input for off state at lamp-driver output			2	6		
Power dissipation	V_{CC} = 12 V	lamp off		140		mW
		lamp on		170		

NOTES: 3. These characteristics are measured with a 564-mV p-p standard multiplex composite signal. This is defined as a signal containing left and/or right audio modulation with a 10-percent, 19-kHz pilot signal in accordance with FCC regulations. For stereo testing, both left-channel-only and right-channel-only modulation are used.
4. The total harmonic distortion and SCA rejection values apply for both stereo and monaural operation.
5. Rejection is referenced to a 1-kHz output signal produced by a 364-mV p-p standard multiplex composite signal as defined in Note 3.

†All typical values are at V_{CC} = 12 V.

‡This is the lowest value for the specified frequency range.

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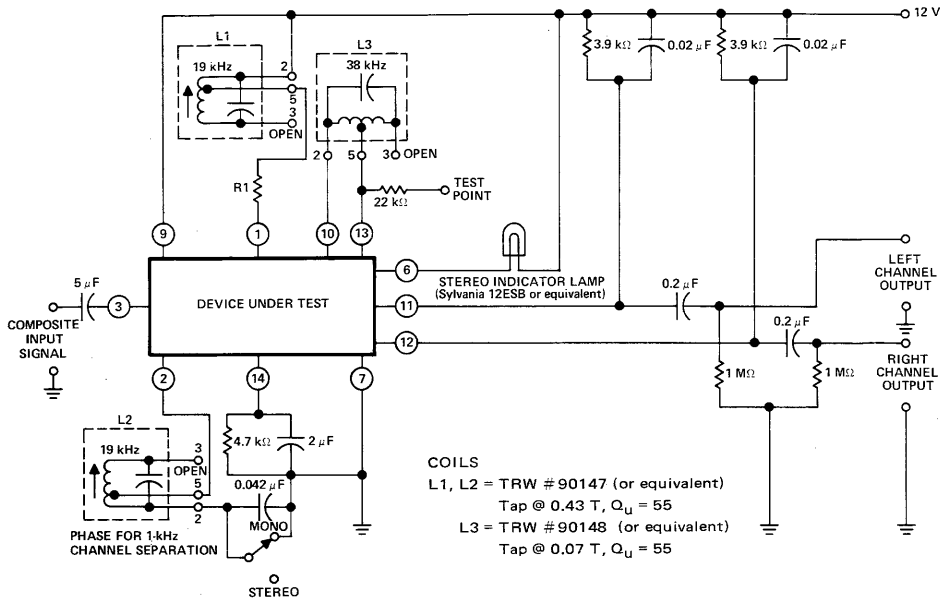
PARAMETER MEASUREMENT INFORMATION



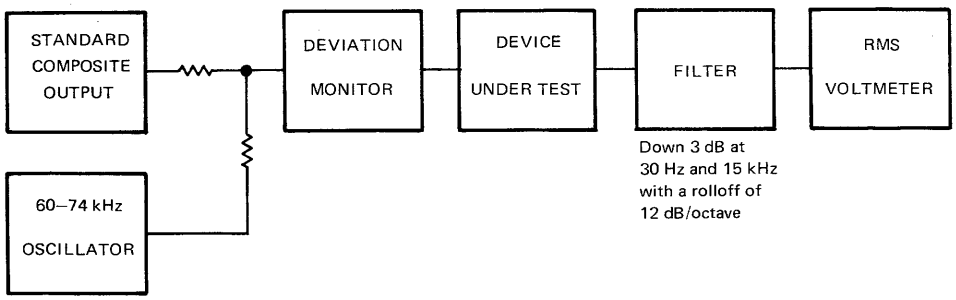
TEST CIRCUIT

typical voltages with respect to pin 7, V_{CC} = 12 V, R1 = 180 Ω, lamp on, measured using a VTVM

Pin Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Volts	11.8	3.2	3.9	NC	NC	0.9	0	NC	12	4.8	8.8	8.8	4.8	1.7

NC—No internal connection

FIGURE 1



test procedure for SCA rejection

1. Modulate the stereo generator with a 1-kHz reference signal.
2. Adjust output for 67.5 kHz deviation.
3. Remove the 1-kHz reference signal.
4. Alternately adjust a 19-kHz pilot signal and a 60-kHz to 74-kHz external signal to deviate 6.7-kHz.
5. Rejection is defined as the difference in dB between the magnitude of the 1-kHz reference signal and the audio components present due to the interaction of the 19-kHz and 38-kHz components with the 60-kHz to 74-kHz signal.

FIGURE 2

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION AND BEAT FREQUENCY COMPONENTS IN AUDIO SIGNAL vs FREQUENCY

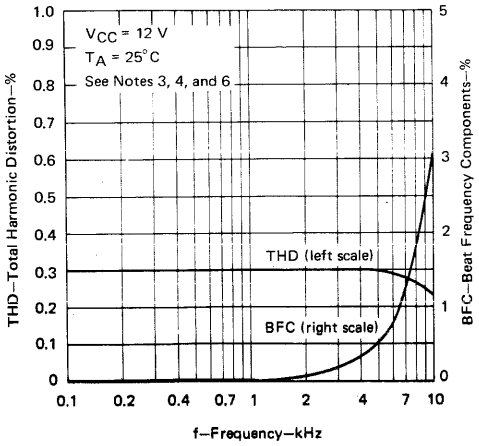


FIGURE 3

TOTAL HARMONIC DISTORTION vs COMPOSITE INPUT LEVEL

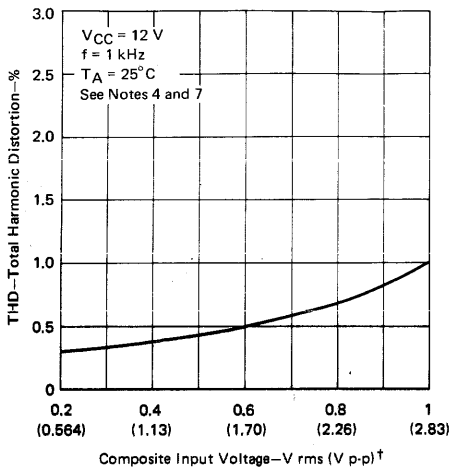


FIGURE 4

CHANNEL SEPARATION vs COMPOSITE INPUT LEVEL

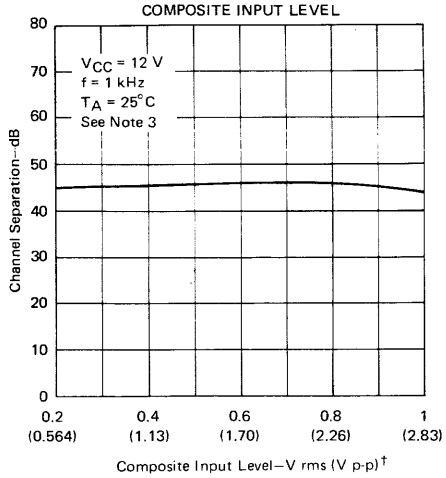


FIGURE 5

CHANNEL SEPARATION vs FREQUENCY

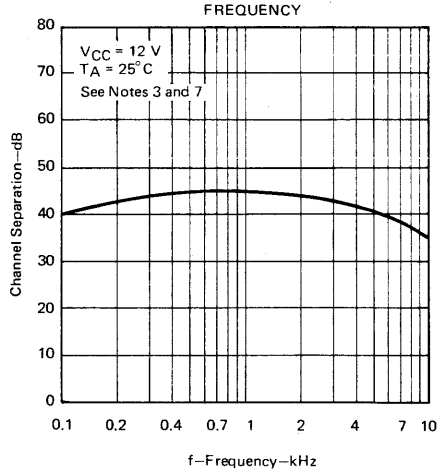


FIGURE 6

NOTES: 3. These characteristics are measured with a 564-mV p-p standard multiplex composite signal. This is defined as a signal containing left and/or right audio modulation with a 10-percent, 19-kHz pilot signal in accordance with FCC regulations. For stereo testing, both left-channel-only and right-channel-only modulation are used.
4. The total harmonic distortion and SCA rejection values apply for both stereo and monaural operation.
6. Beat frequency components (BFC) result from the presence of the 19-kHz pilot signal in stereo broadcasts.
7. Input signal is a 1-kHz composite signal, 846 mV p-p.

†The rms scale is valid for monaural modulation (L=R) only. The peak-to-peak scale is valid for monaural or stereo modulation.

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TYPICAL CHARACTERISTICS

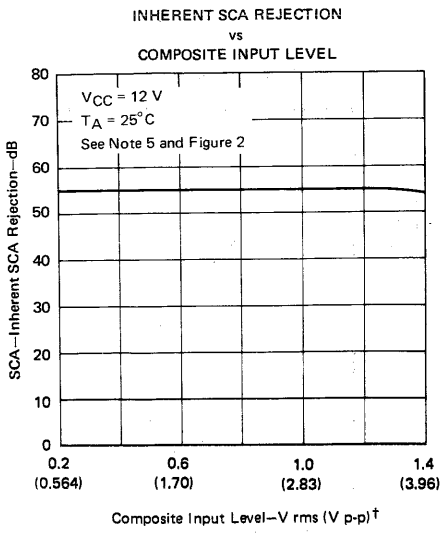


FIGURE 7

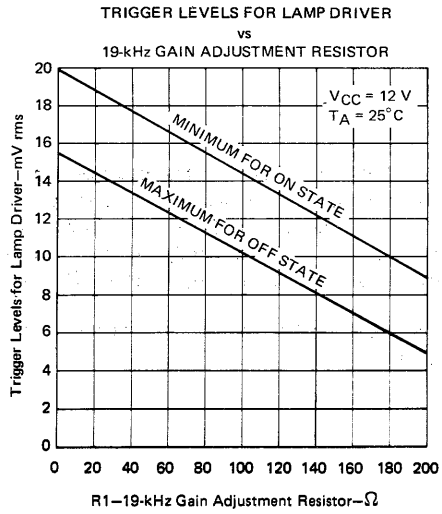


FIGURE 8

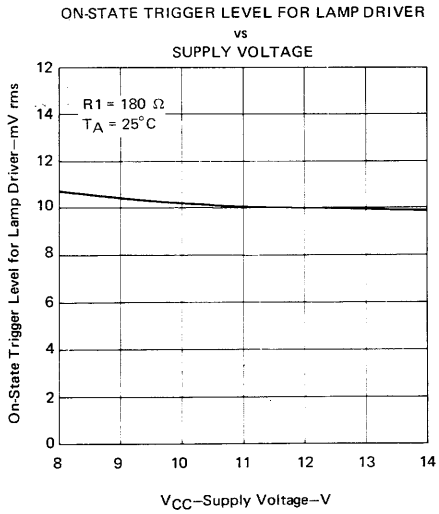


FIGURE 9

NOTE 5: Rejection is referenced to a 1-kHz output signal produced by a 364-mV p-p standard multiplex composite signal as defined in Note 3.

† The rms scale is valid for monaural modulation (L=R) only. The peak-to-peak scale is valid for monaural or stereo modulation.

CIRCUIT TYPE SN76110
STEREO DEMODULATOR

ORDERING INSTRUCTIONS AND MECHANICAL DATA

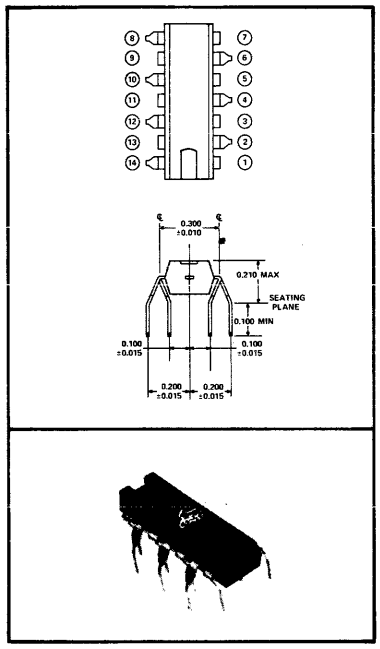
general

The SN76110 is available in the plastic dual-in-line package (outline N). Orders for these devices should include the package outline letter at the end of the type number. The device may also be ordered with the leads formed in the quad-in-line configuration by adding the dash number –07 after the package outline letter, i.e., SN76110N, SN76110N–07.

Refer to Section 1 for physical dimensions for the dual-in-line N-package outline.

3

quad-in-line lead configuration



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