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Systems Interface Business Group
Spectra Logic Products

SPECTRA 126-PLUS

Product Reference Manual

NOTICE

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*RETURN INFORMATION REFERENCE SHEET

Chapter One

Introduction

1.1 GENERAL INFORMATION

The SPECTRA 126-PLUS is a single board multifunction disk and tape controller for use with Texas Instruments' (TI) 990, BS600, and BS800 series of computers. It is constructed on a single full width board, is TILINE compatible, and interfaces with any combination of two Storage Module Drive (SMD) disk drives and two formatted 1/2" tape drives. Configuration changes, including drive mixing and mapping, can be made by setting the appropriate switches outlined in the Drive Configuration Table.

The SPECTRA 126-PLUS provides high reliability, easy maintainability, and quality performance. Advantages not only include cost savings in the purchase price of the controller, but also the option of buying disk and tape drives from independent manufacturers. Extensive use is made of low-power Schottky and standard Schottky Integrated Circuits on an 8 layer PCB with power and ground planes internal. On board, self-test microdiagnostics execute upon power up, and system level diagnostics allow verification of proper operation on the subsystem. A Light Emitting Diode (LED) indication is provided to aid in fault isolation of the system. Most of the standard TI diagnostics run without modification.

The SPECTRA 126-PLUS architecture employs a 2901B processor and a 2911A sequencer using bit slice technology. This design approach provides high performance and flexability to support most SMD interface compatible disk drives, and Pertec compatible 1/2" interface tape drives. The dual bipolar microprocessor implementation provides simultaneous control of the TILINE interface, disk interface, and tape interface.

1.2 FEATURES

The SPECTRA 126-PLUS controller provides many important features. These features include:

* Single full width TI compatible PCB.
* EMI/RFI Chassis Compatible.
* Dual bipolar microprocessor implementation and architecture.
* Full emulation of the DS80/DS300, and WD900 disk subsystems.
* Full emulation of the TI 979 tape subsystem.
* Full Emulation of the MT3200 streamer tape subsystem including extended tape command set when using Cipher Cache Tape.
* One model supports any two SMD disk drives.
* Supports two streaming or formatted start/stop tape drives.
* Provides an Error Correction Code (ECC) with up to 7-bit burst error correction.
* Contains 28 sector disk buffering.
* Supports interleaved and contiguous multiple sector transfers.
* Supports concurrent 2.5MB/sec disk and 1MB/sec tape data transfers.
* Automatic Position Verification.
* Automatic Alternate Track Seeking.
* Removable or fixed media compatible.
* Power consumption comparable to disk-only controllers.
* Supports extended tape and disk commands.
* Compliant with TI's FCC approved "hardened" chassis.
* Any physical to logical mapping.
* Compatible with DX10 or DNOS.
* Overlapped seek support.
* Self-test microdiagnostic.

1.2.1 UNIQUE FEATURES OF THE SPECTRA 126-PLUS vs SPECTRA 26

* TI FCC COMPATIBLE - The SPECTRA 126-PLUS is designed to be compatible with the TI approach to meet current FCC regulations on the 990 minicomputers. It allows the shields of round cables to be attached to the chassis ground.

* NUMBER OF PERIPHERALS SUPPORTED - Due to the restrictions placed on the controller by the connector requirement, the SPECTRA 126-PLUS supports only 2 physical disk and 2 physical tape drives, instead of 4 and 4 as on the SPECTRA-26. The SPECTRA 126-PLUS will still, however, support up to 4 logical drives in cases where a physical drive is divided into multiple logical drives.

* DRIVE CONFIGURABILITY - The SPECTRA 26 has 4 switches, allowing for one model of the controller to support 16 different total drive configurations. The SPECTRA 126-PLUS has 7 switches for each physical drive. The drive configuration PROM describes the physical, rather than the logical drive, allowing the SPECTRA 126-PLUS to support any mix of 2 out of 128 different drive configurations. This scheme should eliminate the need for different models of the controller to support different drive types.

* INCREASED SECTOR BUFFERING - The SPECTRA 126-PLUS has 28 sectors of disk sector buffer rather than 4, as on the SPECTRA 26. This should be sufficient for even the largest ADU size, and virtually eliminate the possibility of missing disk revolutions under operational conditions.

* FORMAT - The SPECTRA 126-PLUS supports 2 different disk drive formats. Along with the format currently supported on the current SPECTRA 26 with 256 bytes per sector, a second format with a smaller leading gap is supported. This allows the controller to take advantage of the fact that fixed media drives eliminate the need for extra format bytes to allow for head skew, and more sectors may be placed on each track increasing the formatted capacity.

* "BAD SYNC" DETECT - The SPECTRA 126-PLUS allows up to a 3 bit error in the 16 bit sync word prior to the data field and will still manage to read the data.

* SURFACE ANALYSIS ASSIST - The SPECTRA 126-PLUS supports an extended 'Surface Analysis Assist' command. The command allows the controller to perform the majority of the functions required to do a surface analysis, and will improve the time necessary, especially when using interleaved sectors.

* TAG 4 AND 5 SUPPORT - The SPECTRA 126-PLUS supports TAG 4 and 5 on the SMD interface, allowing software access to more status information when using Fujitsu or certain CDC disk drives.

* CIPHER CACHE TAPE SUPPORT - The SPECTRA 126-PLUS supports virtually all of the extended features of the Cipher Cache Tape. These are mainly diagnostic aids, but also include features such as 'Write Sync' to flush the Cache, and remote density selection to allow the software to switch tape densities.

* DOCS DIAGNOSTIC SUPPORT - When using a Cipher Cache Tape and CDC FSD disk drive, the new versions of diagnostics under DOCS should run with no expected errors on the SPECTRA 126-PLUS.

1.3 SPECIFICATIONS

FUNCTIONAL CHARACTERISTICS	DISK	TAPE
Drive Attachment	2 physical, 4 logical	2
Interface	All SMD drives	Formatted 1/2"
Base Address	F800-F8F0 (hexadecimal)	F800-F8F0 (hex)
Sector Addressing	Contiguous or Interleaved	N/A
DMA Addressing Range	20 bit	20 bit
DMA Burst Control	1 to 128 words	-----
DMA Block Mode Transfer	Yes	No
Interrupt Priority level	Slot Dependent	Slot Dependent
Buffering	7168 bytes	64 byte FIFO
Capacity/Configuration	Selectable	Selectable
Error Correction Code	32-bit ECC Polynomial	N/A
Seek Operation Control	Overlapped	N/A
Transfer Rate	Up to 2.5MB/sec	Up to 1MB/sec

SPECIFICATIONS [continued]

PHYSICAL CHARACTERISTICS	SPECIFICATION
PCB Size	Single full width 10.8"x 14.2"; 8 layers.
Cable Connections	Disk: One 60 pin Ampmodu connector and one 26 pin Ampmodu cable connector mounted at edge of the PCB. Tape: Two 40 pin Ampmodu connectors.
Environmental	Exceeds TI 990 temperature and humidity specifications.
Power	+5 volts DC @ 7 amps. -12 volts DC @ .7 amps.

NOTE-Cable sets are available for the SPECTRA 126-PLUS which will assist in meeting FCC requirements.

DISK CABLES:Shielded "A" cable with Ampmodu connector to standard flat cable socket. Special dual shielded "B" cable with one Ampmodu connector branching to 2 (Drive 0, Drive 1) standard flat cable sockets.

TAPE CABLES:Special shielded tape cable set, 1 and 2. Each has 40 pin Ampmodu connector transitioning to standard 50 pin edge card connector.

1.4 WARRANTY

Spectra Logic Corporation provides a 12 month limited warranty for the SPECTRA 126-PLUS controller. Repair of PCBs returned in warranty to Spectra Logic will be effected within ten (10) working days after receipt of the failing unit. Repair of PCBs out of warranty will be performed at a nominal charge.

Chapter Two

Installation

2.1 INSTALLATION PROCEDURE

This chapter contains the information needed to install the SPECTRA 126-PLUS controller in any I/O slot of the TI 990, BS600, or BS800 computer. Installation/maintenance personnel should be familiar with both the TI hardware and the specific disk and tape drives being installed.

2.2 INSPECTION

Perform a thorough visual inspection of the SPECTRA 126-PLUS PCB and cables after removal from their shipping container. Note all damage and notify the freight carrier immediately, as Spectra Logic's warranty does not cover shipping damage. Any damage claim is to be filed through the carrier with its insurance company.

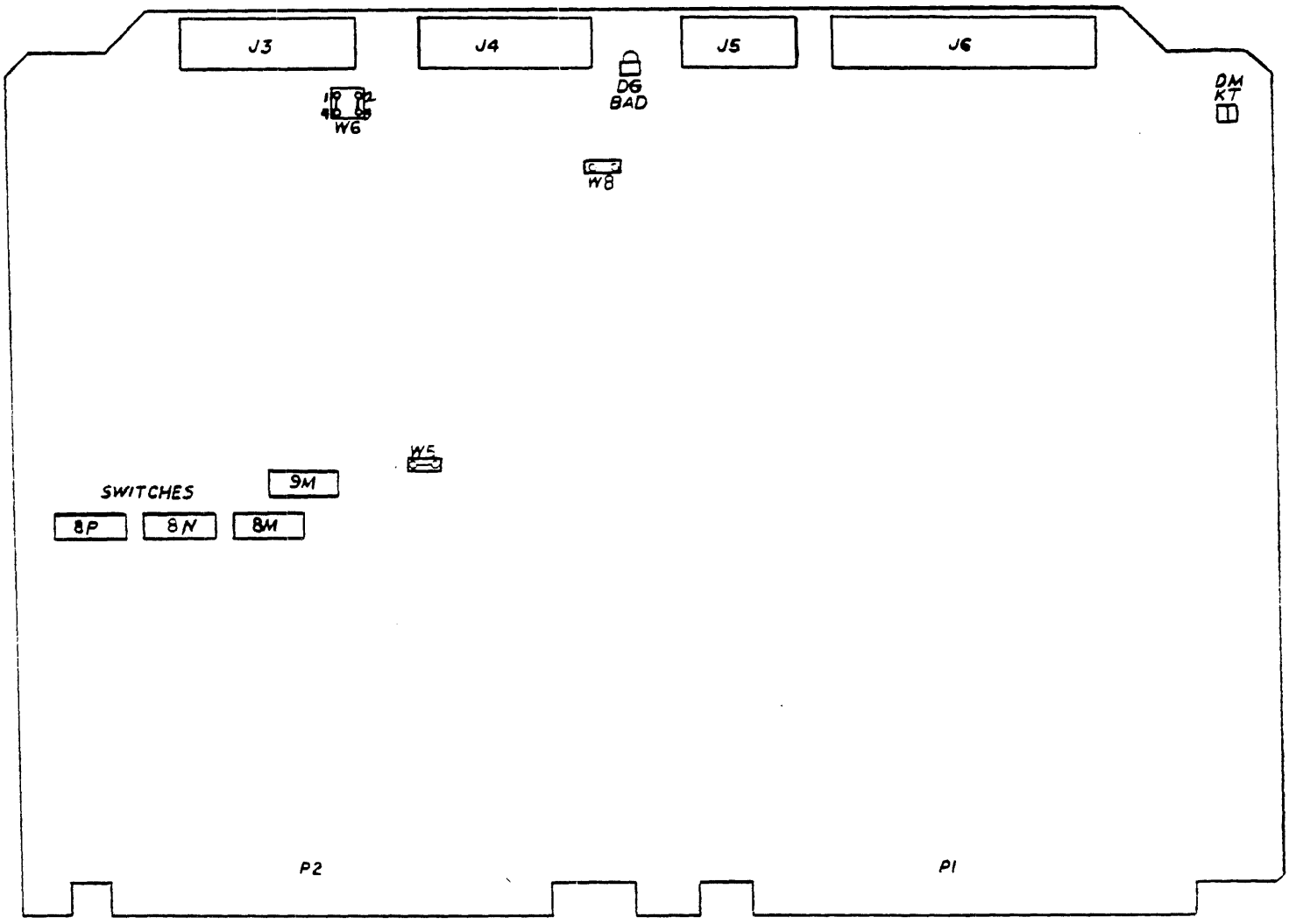
Check for any broken components or bent pins, and ensure that any socketed ICs are securely in place. Inspect the interface cables for cut or broken wires, ensure that the cable is cleanly terminated with the connector.

2.3 CONTROLLER SETUP

The SPECTRA 126-PLUS disk and tape controller is configured using switches and jumpers. The jumper and switch settings must be set up to the configuration desired before installation into the CPU or expansion chassis. Figure 2-1 shows the location of the switches and jumper pins on the board.

2.3.1 JUMPER SETTINGS

There are three jumpers on the SPECTRA 126-PLUS controller. In most cases the "standard" setting is with the jumper installed. To select an alternate option, a trace must be cut, or a jumper must be removed or moved to a different location.


J3
J4
J5
J6
DG
BAD
DM
KT
W6
W8
W5
SWITCHES
9M
8P
8N
8M
P2
P1

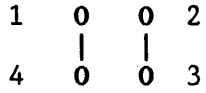
Tape Microdiagnostic Enable Jumper (W5)

Jumper W5 enables magnetic tape microdiagnostic routines when installed. If the controller is failing the tape microdiagnostic tests, the trace installing this jumper may be cut. This causes the controller to skip these tests and allow the SPECTRA 126-PLUS to function as a disk controller only.

W5	
IN	Tape microdiagnostics enabled.
OUT	Tape microdiagnostics disabled.

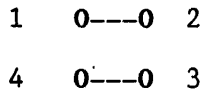
Mag Tape Address Select Jumpers (W6 Pins 1-4)

The SPECTRA 126-PLUS has a four pin jumper (W6) used to control mag tape address selection. The controller is shipped from the factory with pin 1 connected to pin 4, and pin 2 connected to pin 3; the pins are connected by trace. This setting allows the connection of two tape transports, each configured as one logical unit (units 0 and 1). This setting is shown below.



STD

The option of remote density and speed selection is offered by mapping each transport as two logical units. This enables a user to select up to 4 logical units per controller,(for example MT01,2,3,4), mapped to 2 physical units. Each physical unit may be run at low speed and low density, or high speed and high density. This option is installed by cutting the etched trace between pin 1 and 4, and pin 2 and 3. Jumpers are then installed between pin 1 and 2, and pin 3 and 4, as shown below. Switch 8 at location 8M must be closed for this option.



LOGICAL UNIT #	PHYSICAL UNIT #	SPEED	DENSITY
0	1	LOW	LOW
1	1	HIGH	HIGH
2	2	LOW	LOW
3	2	HIGH	HIGH

If the traces are cut and a jumper is installed between pins 1-2 (pins 3-4 left open), all four logical transports operate at high speed and high density.

Tape Density Status Jumper (W8)

If a tape drive is used that has the capability of providing density status and the user would like the controller to read density status from the drive, then the jumper at W8 should be installed. When this jumper is not installed (standard), it assumes that the tape drive is at an operating density of 1600 bpi (PE). This is used for setting or clearing bit 6 in control word 7.

W8	
IN	Controller reads density status from the drive.
(STD) OUT	Controller assumes an operating density status of 1600 bpi (PE).

2.3.2 SWITCH SETTINGS

TILINE Address Switch (Location 8P, SW1-SW8)

The DIP switch in location 8P establishes the controller's disk and tape address. The disk and tape portions must be assigned to different addresses. The TILINE addresses shown are in hexadecimal.

DISK: 1 / TAPE: 5	2 / 6	3 / 7	4 / 8	TILINE ADDRESS
OFF	OFF	OFF	OFF	F800
ON	OFF	OFF	OFF	F810
OFF	ON	OFF	OFF	F820
ON	ON	OFF	OFF	F830
OFF	OFF	ON	OFF	F840
ON	OFF	ON	OFF	F850
OFF	ON	ON	OFF	F860
ON	ON	ON	OFF	F870
OFF	OFF	OFF	ON	F880
ON	OFF	OFF	ON	F890
OFF	ON	OFF	ON	F8A0
ON	ON	OFF	ON	F8B0
OFF	OFF	ON	ON	F8C0
ON	OFF	ON	ON	F8D0
OFF	ON	ON	ON	F8E0
ON	ON	ON	ON	F8F0

CPU Option Switch (Location 9M, SW1-SW8)

The DIP switch at location 9M provides a burst rate option, a format option, and a sector interleave option. These options are described below.

Burst Rate Option (Location 9M, SW1, SW2, SW3)

The burst rate is the number of words the controller will transfer on the TILINE interface each time it obtains access to the TILINE during data transfers.

SW1	SW2	SW3	BURST RATE	
OFF	OFF	OFF	1 WORD	
ON	OFF	OFF	2 WORDS	
OFF	ON	OFF	4 WORDS	(STD)
ON	ON	OFF	8 WORDS	
OFF	OFF	ON	16 WORDS	
ON	OFF	ON	32 WORDS	
OFF	ON	ON	64 WORDS	
ON	ON	ON	128 WORDS	

TRANSFER RATE	INTERLEAVING	RECOMMENDED BURST RATE
1.2 MB/sec	3:1	1 WORD
1.2 MB/sec	2:1	2 WORDS
1.2 MB/sec	1:1	4 WORDS
1.8 MB/sec	3:1	4 WORDS
1.8 MB/sec	2:1	8 WORDS
1.8 MB/sec	1:1	16 WORDS
2.5 MB/sec	3:1	8 WORDS
2.5 MB/sec	2:1	16 WORDS
2.5 MB/sec	1:1	32 WORDS

Extended Tape Status and Write Sync Option (Location 9M, SW4)

The Extended Tape Option allows full MT3200 emulation when used with Cipher 890 and 891 tape drives. This emulation provides additional control and status information as shown in section 3.5.2. The MT3200 emulation offers significant advantages in maximizing system tape transfers when used. The Write Sync Command ensures that all pending write operations are completed. Reference section 3.5.1 for complete information.

SW4

OFF — Disables Automatic Extended Status and Write Sync. Use this setting for **ALL NON-CACHE TAPE DRIVES.** (STD).

ON — Enables Extended Status and Write Sync. (MT 3200).

Format Option (Location 9M, SW5)

The format option is generally used when mapping a physical drive as two or more logical drives. To prevent the disk system from selecting the incorrect head on a mapped drive, the SPECTRA 126-PLUS formats the disk with the physical head number rather than the logical. This ensures that the head addresses are different for the two logical drives. When testing the fixed portion of a CDC CMD, or Ampex DFR, the diagnostics will report several more errors with this option set to physical head format.

SW5	
OFF	Physical head format.
ON	Logical head format.

Sector Interleave Option (Location 9M, SW6, SW7, SW8)

Sectors may be interleaved 1:1, 2:1, or 3:1 on the SPECTRA 126-PLUS controller. However, 3:1 interleaving is not supported on a drive where the number of sectors per track is exactly divisible by 3. Select 2:1 if the drive has an odd number of sectors. The default value for sector interleaving is set for each drive in the Drive Configuration PROM; for standard configurations the default is 1:1. To change this value, it is necessary to set switches 6, 7, and 8 as given below. 1:1 interleaving is recommended for maximum performance due to the increased sector buffering (28) used on the SPECTRA 126-PLUS.

SW6	SW7	SW8	
---	---	OFF	Sector interleave default value is used. (STD)
OFF	OFF	ON	3:1 interleave.
ON	OFF	ON	2:1 interleave.
---	ON	ON	1:1 interleave.

2.3.3 DISK DRIVE CONFIGURATION (Location 8M or 8N)

Drive configuration for the SPECTRA 126-PLUS controller is done through the use of a Drive Configuration PROM. The Drive Configuration PROM contains 128 blocks of 16 bytes. Each block defines one physical drive as one to four logical drives. Switches 1-7 of the configuration switch at location 8M define physical drive 0. Switches 1-7 of the configuration switch in location 8N define physical drive 1. The SPECTRA 126-PLUS supports up to four logical drives; therefore, if physical drive 0 is mapped as four logical units, the configuration switch at location 8N for physical drive 1 becomes meaningless. All of the 128 blocks in the Drive Configuration PROM use the following format for each block.

BLOCK BYTE DEFINITIONS

BYTE 0	The number of logical drives.
BYTE 1	The drive type: Bit 7 = Mapped drive. Bit 6 = CMD type. Bit 5 = CDC Lark type. Bit 4 = Interleaved sectors 3:1. Bit 3 = Interleaved sectors 2:1. Bit 2 = 20 byte GAP1. Bit 1 = Reserved for physical drive number. Bit 0 = Reserved for physical drive number.
BYTE 2	Number of sectors for all drives.
BYTE 3	Number of heads for the first logical drive.
BYTE 4	Number of heads for 2nd, 3rd, and 4th logical drives.
BYTE 5	Head offset for the first logical drive.
BYTE 6	Head offset for the second logical drive.
BYTE 7	Head offset for the third logical drive.
BYTE 8	Head offset for the fourth logical drive.
BYTE 9	Number of cylinders for the first logical drive (MSB).
BYTE A	Number of cylinders for the first logical drive (LSB).
BYTE B	Number of cylinders for the 2nd, 3rd, 4th logical drives (MSB)
BYTE C	Number of cylinders for the 2nd, 3rd, 4th logical drives (LSB)
BYTE D	Mapped cylinders/cylinder offset: Bit 7 = Mapped cylinder. Bits 6-3 = Unused. Bits 2-0 = Cylinder offset for second drive.
BYTE E	Cylinder offset for 2nd drive; if mapped cylinders: (1st = 0, 3rd = 2X, 4th = 3X).
BYTE F	Unused.

DRIVE SELECTION

The following Disk Drive Selection Guides and Configuration Tables define specifications for each major disk drive manufacturer. This section can be used as a reference for insuring SPECTRA 16/26/46 media compatibility, or to maximize disk storage capacity.

The major distinction between DS80/300 and WD900 drive types is the number of alternate cylinders specific to each. DS80/300 drive types use 10 alternate cylinders. The WD900 drive types use 16 alternate cylinders. The SPECTRA 126-PLUS supports some drives with 16 alternate cylinders, some with 10 alternate cylinders, and some with either. Selection of number of alternate cylinders is based on drive size and anticipated spare track requirements. Drives with 16 alternate cylinders are indicated in the disk drive selection guide by an asterisk (*) or pound sign (#), and must be formatted as a WD900 drive type. All other drive types will require formatting as a DS80/300 drive.

The WD900 is supported by DOCS Revision 207/84 or later, DX10 Revision 3.6.1 or later, and DNOS Revision 1.2.1 or later. Drives indicated by the pound sign (#) in the selection guides (switch settings 0 through 3) will be recognized as a WD900 disk type when running diagnostics and the IDS (Initialize Disk Surface) utility which accomplishes surface analysis and bad track mapping. Drives not recognized as a WD900 disk type will be flagged as an unknown disk drive and require formatting by the disk surface analysis test (DSKSA), which is a verb module under the Diagnostic Operational Controls System (DOCS).

When running any disk diagnostic on a disk whose parameters are not recognized by the software, the store register values must be patched to allow the diagnostic to run the disk as a known disk drive supporting diagnostic cylinders and alternate tracking features. Drives over 500MB are supported only as 2 logical units because of allocatable disk units (ADU) size limitations under most operating systems.

Disabling DS80/300 Alternate Cylinders (Location 8N, SW8)

Alternate cylinders are normally used and are recommended. In cases where existing drives have been formatted without alternate cylinders, (an option on the S16,26 controller) and data cannot be removed, it may be desireable to disable the ten alternate cylinders on the S126-PLUS. This option disables the alternate cylinders by adding a count of ten to the store register word 3 (Head, Cylinders) values.

SW 8	
OFF	Disables Ten Alternate Cylinders (STD).
ON	Enables Ten Alternate Cylinders.

MANUFACTURER-AMPEX

DISK DRIVE SELECTION GUIDE

MODEL #	UNFORMATTED CAPACITY	PHYSICAL CYL/HD/SEC	SWITCH VALUE DECIMAL	LOG. UNIT	FORMATTED CAPACITY	COMMENTS
DM940	40MB	411/5/64	17	1	32 MB	
DM980	80MB	823/5/61	12	1	63 MB	
DM980	80MB	823/5/64	13	1	66 MB	
DM9160	160MB	1645/5/64	18	1	133.7 MB	
DM9300	300MB	815/19/61	19	1	238 MB	
DM9300A	300MB	823/19/61	20	1	240 MB	
DM9300A	300MB	823/19/64	21	1	252MB	
DFR 932	16MB/16MB	823/1-1/64	22	2	13MB/13MB	1st LOG REMOVEABLE
DFR 932	16MB/16MB	823/1-1/64	23	2	13MB/13MB	1st LOG FIXED
DFR 964	16MB/48MB	823/1-3/64	24	2	13MB/ 39.8MB	
DFR 964	16MB/48MB	823/1-3/64	25	2	13MB/ 39.8MB	
DFR 964	16MB/48MB	823/1-3/64	26	4	4 x 13MB	1st LOG REMOVEABLE
DFR 964	16MB/48MB	823/1-3/64	27	4	4 x 13MB	2nd LOG REMOVEABLE
DFR 996	16MB/80MB	823/1-5/64	28	2	13MB/66MB	1st LOG REMOVEABLE
DFR 996	16MB/80MB	823/1-5/64	29	2	66MB/13MB	1st LOG FIXED
C 165	160MB	823/10/64	10	2	2 x 66MB	
C 165	160MB	823/10/64	8	1	132MB	
C 165	160MB	823/10/67	0	1	138MB	16 ALTCYL* 20 BT GAP1
C 165	160MB	823/10/67	2	2	2 X 69MB	16 ALTCYL* 20 BT GAP1
C 330	330MB	1024/16/64	14	1	265MB	
330	330MB	1024/8/128	73	1	265MB	
660	660MB	1024/16/128	74	2	2 x 263.7MB	16 ALT CYL *
825	825MB	1024/20/128	75	2	2 x 263.7MB	16 ALT CYL *

*Must be formatted as WD900

MANUFACTURER-AMPEX

DISK DRIVE CONFIGURATION TABLE

SWITCH 8M, 8N								MODEL	LOGICAL	LOG.	STORE REGISTER VALUES		
DECIMAL VALUE	7	6	5	4	3	2	1	#	CYL/HD/SEC	UNIT	WORD 1	WORD 2	WORD 3
17	0	0	1	0	0	1	0	DM 940	399/5/64	1	2000	4000	298F
12	0	0	0	1	1	0	0	DM 980	811/5/61	1	1E80	3D00	2B2B
13	0	0	0	1	1	0	1	DM 980	811/5/64	1	2000	4000	2B2B
18	0	0	1	0	0	1	0	DM9160	1633/5/64	1	2000	4000	9B23
19	0	0	1	0	0	1	1	DM9300	803/19/61	1	1E80	3D00	9B23
20	0	0	1	0	1	0	0	DM9300A	811/19/61	1	1E80	3D00	9B2B
21	0	0	1	0	1	0	1	DM9300A	811/19/64	1	2000	4000	9B2B
22	0	0	1	0	1	1	0	DFR 932	811/1/64	2	2000	4000	0B2B
23	0	0	1	0	1	1	1	DFR 932	811/1/64	2	2000	4000	0B2B
24	0	0	1	1	0	0	0	DFR 964	811/1/64 811/3/64	2	2000	4000	0B2B 1B23
25	0	0	1	1	0	0	1	DFR 964	811/3/64 811/1/64	2	2000	4000	1B23 0B2B
26	0	0	1	1	0	1	0	DFR 964	811/1/64	4	2000	4000	0B2B
27	0	0	1	1	0	1	1	DFR 964	811/1/64	4	2000	4000	0B2B
28	0	0	1	1	1	0	0	DFR 996	811/1/64 811/5/64	2	2000	4000	0B2B 2B2B
29	0	0	1	1	1	0	1	DFR 996	811/5/64 811/1/64	2	2000	4000	2B2B 0B2B
10	0	0	0	1	0	1	0	C 165	811/5/64	2	2000	5800	2B2B
8	0	0	0	1	0	0	0	C 165	811/10/64	1	2000	4000	532B
0	0	0	0	0	0	0	0	C 165	805/10/67	1	2180	4300	5325*#
2	0	0	0	0	0	1	0	C 165	805/5/67	2	2180	4300	2325*#
14	0	0	0	1	1	1	0	C 330	1012/16/64	1	2000	4000	83F4
73	1	0	0	1	0	0	1	330	1012/8/128	1	4000	8000	43F4
74	1	0	0	1	0	1	0	660	1006/8/128	2	4000	8000	43EE*
75	1	0	0	1	0	1	1	825	1006/10/128	2	4000	8000	53EE*

*Must be formatted as WD900
#WD900 Disk Parameters-No Patching Required.
1 = ON
0 = OFF

MANUFACTURER-CENTURY DATA SYSTEMS

DISK DRIVE SELECTION GUIDE

MODEL #	UNFORMATTED CAPACITY	PHYSICAL CYL/HD/SEC	SWITCH VALUE DECIMAL	LOG. UNIT	FORMATTED CAPACITY	COMMENTS
T82	80MB	815/5/61	43	1	62MB	
T82	80MB	815/5/64	40	1	65MB	
T302	300MB	815/19/64	45	1	249MB	
T302	300MB	815/19/61	19	1	238MB	
M80	80MB	569/6/76	46	1	65MB	
M160	162MB	845/6/101	47	1	129MB	
AMS190	191MB	569/14/76	48	1	151MB	
AMS380	378MB	845/14/101	49	1	301MB	
AMS513	513MB	845/19/101	50	1	409MB	
AMS571	571MB	941/19/119	51	2	2 x 235MB	
AMS315	315MB	823/19/61	20	1	240MB	
AMS315	315MB	823/19/64	21	1	252MB	
AMS615	615MB	981/19/110	69	2	2 x 245MB	
C2075	26MB(R) 53MB(F)	644/2/66 644/4/66	78	2	21MB 42MB	
C2476	474MB	842/20/93	5	1	392MB	16 ALT.CYL.*
C2476	474MB	842/10/93	7	2	2 x 196MB	16 ALT.CYL.*
C2476	474MB	842/20/88	9	1	373.9MB	
C2476	474MB	842/10/88	11	2	2 x 187MB	

*Must be formatted as WD900

MANUFACTURER-CENTURY DATA SYSTEMS

DISK DRIVE CONFIGURATION TABLE

SWITCH 8M, 8N								MODEL	LOGICAL	LOG.	STORE REGISTER VALUES		
DECIMAL	SWITCH SETTINGS							#	CYL/HD/SEC	UNIT	WORD 1	WORD 2	WORD 3
VALUE	7	6	5	4	3	2	1						
43	0	1	0	1	0	1	1	T82	803/5/61	1	IE80	3D00	2B23
40	0	1	0	1	1	0	0	T82	803/19/64	1	2000	4000	2B23
45	0	1	0	1	1	0	0	T302	803/19/64	1	2000	4000	9B23
19	0	0	1	0	0	1	1	T302	803/19/61	1	1E80	3D00	9B23
46	0	1	0	1	1	1	0	M80	557/6/76	1	2600	4C00	322D
47	0	1	0	1	1	1	1	M160	833/6/101	1	3280	6500	3341
48	0	1	1	0	0	0	0	AMS190	557/14/76	1	2600	4C00	722D
49	0	1	1	0	0	0	1	AMS380	833/14/101	1	3280	6500	7341
50	0	1	1	0	0	1	0	AMS513	833/19/101	1	3280	6500	9B41
51	0	1	1	0	0	1	1	AMS571	929/9/110	2	3700	6E00	53A1
20	0	0	1	0	1	0	0	AMS315	811/19/61	1	1E80	3D00	9B2B
21	0	0	1	0	1	0	1	AMS315	811/19/64	1	2000	4000	9B2B
69	1	0	0	0	1	0	1	AMS615	969/9/110	2	3700	6E00	53C9
78	1	0	0	1	1	1	0	C2075	632/2/66 632/4/66	2	2100 2100	4200 4200	1278 2278
5	0	0	0	0	1	0	1	C2476	824/20/93	1	2E80	5D00	A338 *
7	0	0	0	0	1	1	1	C2476	824/10/93	2	2E80	5D00	5338 *
9	0	0	0	1	0	0	1	C2476	830/20/88	1	2C00	5800	A33E
11	0	0	0	1	0	1	1	C2476	830/10/88	2	2C00	5800	5338

*Must be formatted as WD900
1 = ON
0 = OFF

MANUFACTURER-CONTROL DATA CORPORATION

DISK DRIVE SELECTION GUIDE

MODEL #	UNFORMATTED CAPACITY	PHYSICAL CYL/HD/SEC	SWITCH VALUE DECIMAL	LOG. UNIT	FORMATTED CAPACITY	COMMENTS
9760	40MB	411/5/64	17	1	32MB	
9730-80 9762 9710	80MB	823/5/61	12	1	63MB	
9730-80 9762 9710	80MB	823/5/64	13	1	66MB	
9766	300MB	11/19/61	20	1	240MB	
9766	300MB	11/19/64	21	1	252MB	
9448-32	16MB 16MB	823/1/64	22	2	13/13MB	1st LOG. REMOVEABLE
9448-64	16MB 16MB	823/1/64	23	2	13/13MB	1st LOG. FIXED
9448-64	16MB 48MB	823/1/64 823/3/64	24	2	13/39.8MB	1st LOG. REMOVEABLE
9448-64	48MB 16MB	823/3/64 823/1/64	25	2	39.8/13MB	1st LOG. FIXED
9448-64	16MB X 4	823/1/64 823 X 4	26	4	13MB X 4	
9448-64	16MB X 4	823/1/64 823 X 4	27	4	13MB X 4	
9448-96	16MB 80MB	823/1/64 823/5/64	28	2	13MB/66MB	1st LOG. REMOVEABLE
9448-96	16MB 80MB	823/5/64	29	2	66MB/13MB	1st LOG. FIXED
9730-160 9715-160	160MB	823/10/61	31	2	2 X 63MB	
9730-160 9715-160	160MB	823/10/64	10	2	2 X 66MB	
9730-160 9715-160	160MB	823/10/64	8	1	132MB	
9730-160 9715-160	160MB	823/10/67	0	1	138MB	16 ALT.CYL* 20 BYTEGAP1
9730-160 9715-160	160MB	823/10/67	2	2	2 X 69MB	16 ALT.CYL* 20 BYTEGAP1
9715-340	340MB	711/24/64	38	1	274MB	
9715-500	500MB	711/24/95	39	1	407MB	
9715-500	500MB	711/24/100	1	1	425MB	16 ALT.CYL*
9715-500	500MB	711/24/100	3	2	2 X 212MB	16 ALT.CYL*
9715-500	500MB	711/24/95	40	2	2 X 203MB	
9771	825MB	1024/16/160	41	2	2 X 331	
9771	825MB	1024/16/160	85	2	2 X 329MB	16 ALT.CYL*
9775	675MB	843/40/61	32	2	2 X 259MB	
9775	675MB	843/40/64	68	2	2 X 276MB	
9412	80MB	784/5/64	35	1	63MB	
9455-16	8/8MB	206/2/64	33	2	2 X 6.3MB	
9457-50	25/25MB	624/2/64	34	2	2 X 20MB	
9720	368MB	1217/10/100	53	1	308MB	10 ALT.CYL
9720	368MB	1217/10/95	88	1	293MB	10 ALT.CYL

*Must be formatted as WD900

MANUFACTURER-CONTROL DATA CORPORATION

DISK DRIVE SELECTION GUIDE

MODEL #	UNFORMATTED CAPACITY	PHYSICAL CYL/HD/SEC	SWITCH VALUE DECIMAL	LOG. UNIT	FORMATTED CAPACITY	COMMENTS
9720	368MB	1217/10/100	103	1	307MB	16 ALT.CYL*
9720	369MB	1217/10/95	104	2	147MB	
9720	500MB	1217/10/126	96	1	389MB	
9720	500MB	1217/10/128	97	1	392MB	16 ALT CYL*
9720	500MB	1217/10/126	98	2	194MB	
9720	736MB	1635/15/95	99	1	592MB	
9720	736MB	1635/15/100	100	1	620MB	16 ALT CYL*
9720	736MB	1635/15/95	101	2	293MB	
9720	736MB	1635/15/95	102	2	306MB	16 ALT CYL*

*Must Be Formatted As WD900.

MANUFACTURER-CONTROL DATA CORPORATION

DISK DRIVE CONFIGURATION TABLE

SWITCH 8M, 8N								MODEL	LOGICAL	LOG.	STORE REGISTER VALUES		
DECIMAL	SWITCH SETTINGS							#	CYL/HD/SEC	UNIT			
VALUE	7	6	5	4	3	2	1				WORD 1	WORD 2	WORD 3
17	0	0	1	0	0	0	1	9760	399/5/64	1	2000	4000	298F
12	0	0	0	1	1	0	0	9730-80 9762 9710	811/5/61	1	1E80	3D00	2B2B
13	0	0	0	1	1	0	1	9730-80 9762 9710	811/5/64	1	2000	4000	2B2B
20	0	0	1	0	1	0	0	9766	811/19/61	1	1E80	3D00	9B2B
21	0	0	1	0	1	0	1	9766	811/19/64	1	2000	4000	9B2B
22	0	0	1	0	1	1	0	9448-32	811/1/64	2	2000	4000	0B2B
23	0	0	1	0	1	1	1	9448-32	811/1/64	2	2000	4000	0B2B
24	0	0	1	1	0	0	0	9448-64	811/1/64 811/3/64	2	2000	4000	0B2B 1B2B
25	0	0	1	1	0	0	1	9448-64	811/3/64 811/1/64	2	2000	4000	1B2B 0B2B
26	0	0	1	1	0	1	0	9448-64	811/1/64	4	2000	4000	0B2B
27	0	0	1	1	0	1	1	9448-64	811/1/64	4	2000	4000	0B2B
28	0	0	1	1	1	0	0	9448-96	811/1/64 811/5/64	2	2000	4000	0B2B 2B2B
29	0	0	1	1	1	0	1	9448-96	811/5/64 811/1/64	2	2000	4000	2B2B 0B2B
31	0	0	1	1	1	1	1	9730-160 9715-160	811/5/61	2	1E80	3D00	2B2B
10	0	0	0	1	0	1	0	9730-160 9715-160	811/5/61	2	1E80	3D00	2B2B
8	0	0	0	1	0	0	0	9730-160 9715-160	811/10/64	1	2000	4000	532B
0	0	0	0	0	0	0	0	9730-160 9715-160	805/10/67	1	2180	4300	5325*#
2	0	0	0	0	0	1	0	9730-160 9715-160	805/5/67	2	2180	4300	2B25*#
38	0	1	0	0	1	1	0	9715-340	699/24/64	1	2000	4000	C2BB
39	0	1	0	0	1	1	1	9715-500	699/24/95	1	2F80	5F00	C2BB
1	0	0	0	0	0	0	1	9715-500	693/24/100	1	3200	6400	C2B5*#
3	0	0	0	0	0	1	1	9715-500	693/12/100	2	3200	6400	62B5*#
40	0	1	0	1	0	0	0	9715-500	699/12/95	2	2F80	5F00	62BB
41	0	1	0	1	0	0	1	9771	1012/8/160	2	5000	A000	83F4
85	1	0	1	0	1	0	1	9771	1006/8/160	2	5000	A000	43EE*
32	0	1	0	0	0	0	0	9775	831/20/61	2	1E80	3D00	A33F
68	1	0	0	0	1	0	0	9775	831/20/64	2	2000	4000	A33F
35	0	1	0	0	0	1	1	9412	772/5/64	1	2000	4000	2B04
33	0	1	0	0	0	0	1	9455-16	194/2/64	2	2000	4000	10C2
34	0	1	0	0	0	1	0	9455-50	612-1 64	2	2000	4000	0A64
53	0	1	1	0	1	0	1	9720	1205/10/100	1	3200	6400	54B5
88	1	0	1	1	0	0	0	9720	1205/10/95	1	2F80	5F00	54B5

*Must be formatted as WD900

#WD900 Disk Parameter-No Patching Required.

1=ON

0=OFF

MANUFACTURER-CONTROL DATA CORPORATION

DISK DRIVE CONFIGURATION TABLE

SWITCH 8M, 8N								MODEL	LOGICAL	LOG.	STORE REGISTER VALUES		
DECIMAL	SWITCH SETTINGS							#	CYL/HD/SEC	UNIT			
VALUE	7	6	5	4	3	2	1				WORD 1	WORD 2	WORD 3
103	1	1	0	0	1	1	1	9720-368	1199/10/100	1	3200	6400	54AF*
104	1	1	0	1	0	0	0	9720-368	1205/5/95	2	2F80	5F00	2CB5
96	1	1	0	0	0	0	0	9720-500	1205/10/126	1	3F00	7E00	54B5
97	1	1	0	0	0	0	1	9720-500	1199/10/128	1	4000	8000	54AF*
98	1	1	0	0	0	1	0	9720-500	1205/5/126	2	3F00	7E00	2CB5
99	1	1	0	0	0	1	1	9720-500	1623/15/95	1	2F80	5F00	7E57
100	1	1	0	0	1	0	0	9720-736	1617/15/100	1	3200	6400	7E51*
101	1	1	0	0	1	0	1	9720-736	805/15/95	2	2F80	5F00	7B25
102	1	1	0	0	1	1	0	9720-736	799/15/100	2	3200	6400	7B1F*

*Must Be Formatted As WD900.

MANUFACTURER-DISK TECH ONE

DISK DRIVE SELECTION GUIDE

MODEL #	UNFORMATTED CAPACITY	PHYSICAL CYL/HD/SEC	SWITCH VALUE DECIMAL	LOG. UNIT	FORMATTED CAPACITY	COMMENTS
4300	301MB	832/14/82	42	1	240MB	
4160	165MB	823/10/64	10	2	2 X 66MB	
4160	165MB	823/10/64	8	1	132MB	
4160	160MB	823/10/67	0	1	138MB	16 ALT.CYL.* 20 BYTEGAP 1
4160	160MB	823/10/67	2	2	2 X 69MB	20 BYTEGAP 1 *

MANUFACTURER-DISK TECH ONE

DISK DRIVE CONFIGURATION TABLE

SWITCH DECIMAL VALUE	8M, 8N SWITCH SETTINGS 7	6	5	4	3	2	1	MODEL #	LOGICAL CYL/HD/SEC	LOG. UNIT	STORE REGISTER VALUES WORD 1	WORD 2	WORD 3
42	0	1	0	1	0	1	0	4300	820/14/82	1	2900	5200	7334
10	0	0	0	1	0	1	0	4160	811/5/64	2	2000	4000	2B2B
8	0	0	0	1	0	0	0	4160	811/10/64	1	2000	4000	532B
0	0	0	0	0	0	0	0	4160	805/10/67	1	2180	4300	5325 *#
2	0	0	0	0	0	1	0	4160	805/10/67	2	2180	4300	2325 *#

#WD900 Disk Parameter-No Patching Required.
*Must be formatted as WD900

1=ON
0=OFF

MANUFACTURER-FUJITSU

DISK DRIVE SELECTION GUIDE

MODEL #	UNFORMATTED CAPACITY	PHYSICAL CYL/HD/SEC	SWITCH VALUE DECIMAL	LOG. UNIT	FORMATTED CAPACITY	COMMENTS
2211	80MB	823/5/61	12	1	63MB	
2211	80MB	823/5/64	13	1	66MB	
2312	84MB	589/7/64	127	1	66MB	
2284 2322	165MB	823/10/64	8	1	132MB	
2284 2322	165MB	823/10/64	10	2	2 X 66MB	
2284 2322	165MB	823/10/61	31	2	2 X 63MB	
2284 2322	165MB	823/10/68	4	1	140 MB	16 ALT. CYLINDERS *
2284 2322	165MB	823/10/68	6	2	2 X 70MB	16 ALT. CYLINDERS *
2284 2322	160MB	823/10/67	0	1	138MB	16 ALT. CYL. 20 BYTE GAP 1*
2284 2322	160MB	823/10/67	2	2	2 X 69MB	16 ALT. CYL. 20 BYTE GAP 1*
2294	330MB	1024/16/64	14	1	265MB	
2298	671MB	1024/16/128	15	2	2 X 265MB	
2331	165MB	823/5/128	60	1	132MB	
2333	337MB	823/10/128	62	1	265MB	
2333	337MB	823/10/128	63	2	2 X 132MB	
2333	337MB	823/10/128	82	1	263.7MB	16 ALT. CYL. *
2333	337MB	823/10/128	83	2	2 X 131.8MB	16 ALT. CYL. *
2351	474MB	842/20/88	9	1	373MB	
2351	474MB	842/20/88	11	2	2 X 186MB	
2351	474MB	842/20/93	5	1	392MB	16 ALT. CYL. *
2351	474MB	842/20/93	7	2	2 X 196MB	16 ALT. CYL. *
2361	686MB	842/20/128	61	2	2 X 271.9MB	
2361	689MB	842/20/128	81	2	2 X 270MB	16 ALT. CYL. *
2361	698MB	842/20/128	89	1	544MB	10 ALT. CYL.
2361	698MB	842/20/128	90	1	540MB	16 ALT. CYL. *
2344	690MB	624/27/128	91	1	541MB	10 ALT. CYL.
2344	690MB	624/27/128	92	1	536MB	16 ALT. CYL. *
2344	690MB	624/27/128	93	2	265MB	10 ALT. CYL.
2344	690MB	624/27/128	94	2	260MB	16 ALT. CYL. *

*Must Be Formatted As WD900.

MANUFACTURER-FUJITSU

DISK DRIVE CONFIGURATION TABLE

SWITCH DECIMAL VALUE	8M, 8N SWITCH SETTINGS 7	6	5	4	3	2	1	MODEL #	LOGICAL CYL/HD/SEC	LOG. UNIT	STORE REGISTER VALUES WORD 1	WORD 2	WORD 3
12	0	0	0	1	1	0	0	2211	811/5/61	1	1E80	3D00	2B2B
13	0	0	0	1	1	0	1	2211	811/5/64	1	2000	4000	2B2B
127	1	1	1	1	1	1	1	2212	577/7/64	1	2000	4000	3A41
8	0	0	0	1	0	0	0	2284 2322	811/10/64	1	2000	4000	532B
10	0	0	0	1	0	1	0	2284 2322	811/5/64	2	2000	4000	2B2B
31	0	0	1	1	1	1	1	2284 2322	811/5/61	2	1E80	3D00	2B2B
4	0	0	0	0	1	0	0	2284 2322	805/10/68	1	2200	4400	5325*
6	0	0	0	0	1	1	0	2284 2322	805/5/68	2	2200	4400	2B25*
0	0	0	0	0	0	0	0	2322 2284	805/10/67	1	2180	4300	5325*#
2	0	0	0	0	0	1	0	2322 2284	805/5/67	2	2180	4300	2325*#
14	0	0	0	1	1	1	0	2294	1012/16/64	1	2000	4000	83F4
15	0	0	0	1	1	1	1	2298	1012/8/128	2	4000	8000	43F4
60	0	1	1	1	1	0	0	2331	811/5/128	1	4000	8000	2B2B
62	0	1	1	1	1	1	0	2333	811/10/128	1	4000	8000	532B
63	0	1	1	1	1	1	1	2333	811/5/128	2	4000	8000	2B2B
82	1	0	1	0	0	1	0	2333	805/10/128	1	4000	8000	5325*
83	1	0	1	0	0	1	1	2333	805/5/128	2	4000	8000	2B25*
9	0	0	0	1	0	0	1	2351	830/20/88	1	2C00	5800	A33E
11	0	0	0	1	0	1	1	2351	830/10/88	2	2C00	5800	533E
5	0	0	0	0	1	0	1	2351	824/20/93	1	2E80	5D00	A338*
7	0	0	0	0	1	1	1	2351	824/10/93	2	2E80	5D00	5338*
61	0	1	1	1	1	0	1	2361	830/10/128	2	4000	8000	533E
81	1	0	1	0	0	0	1	2361	824/10/128	2	4000	8000	5338*
89	1	0	1	1	0	0	1	2361	830/20/128	1	4000	8000	A33E
90	1	0	1	1	0	1	0	2361	824/20/128	1	4000	8000	A338 *
91	1	0	1	1	0	1	1	2344	612/27/128	1	4000	8000	DA64
92	1	0	1	1	1	0	0	2344	606/27/128	1	4000	8000	DA5E *
93	1	0	1	1	1	0	1	2344	300/27/128	2	4000	8000	D92C
94	1	0	1	1	1	1	0	2344	294/27/128	2	4000	8000	D926 *

*Must be formatted as WD900
#WD900 Disk Parameter-No Patching Required.

1=ON
0=OFF

MANUFACTURER-KENNEDY

DISK DRIVE SELECTION GUIDE

MODEL #	UNFORMATTED CAPACITY	PHYSICAL CYL/HD/SEC	SWITCH VALUE DECIMAL	LOG. UNIT	FORMATTED CAPACITY	COMMENTS
5380 7380	80MB	823/5/61	12	1	63MB	
5380 7380	80MB	823/5/64	13	1	66MB	
53160	160MB	823/10/64	8	1	132MB	
53160	160MB	823/10/64	10	2	2 X 66MB	
53160	160MB	823/10/67	0	1	138MB	16 ALT. CYL.*
53160	160MB	823/10/67	2	2	2 X 69MB	16 ALT. CYL.*
7340	40MB	411/5/64	17	1		

MANUFACTURER-KENNEDY

DISK DRIVE CONFIGURATION TABLE

SWITCH DECIMAL VALUE	8M, 8N SWITCH SETTINGS 7	6	5	4	3	2	1	MODEL #	LOGICAL CYL/HD/SEC	LOG. UNIT	STORE REGISTER VALUES WORD 1	WORD 2	WORD 3
12	0	0	0	1	1	0	0	5380 7380	811/5/61	1	IE80	3D00	2B2B
13	0	0	0	1	1	0	1	5380 7380	811/5/64	1	2000	4000	2B2B
8	0	0	0	1	0	0	0	53160	811/10/64	1	2000	4000	532B
10	0	0	0	1	0	1	0	53160	811/5/64	2	2000	4000	2B2B
0	0	0	0	0	0	0	0	53160	805/10/67	1	2180	4300	5325*#
2	0	0	0	0	0	1	0	53160	805/5/67	2	2180	4300	2325*#
17	0	0	1	0	0	0	1	7340	399/5/64	1	2000	4000	298F
31	0	0	1	1	1	1	1	53160	811/5/61	2	IE80	3D00	2B2B

* Must be formatted as WD900
# WD900 Disk Parameter-No Patching Required.

1=ON
0=OFF

MANUFACTURER-NEC

DISK DRIVE SELECTION GUIDE

MODEL #	UNFORMATTED CAPACITY	PHYSICAL CYL/HD/SEC	SWITCH VALUE DECIMAL	LOG. UNIT	FORMATTED CAPACITY	COMMENTS
D2257	167.7MB	1024/8/68	64	1	140MB	
D2368	330MB	823/10/128	62	1	265MB	
D2368	330MB	823/10/128	63	2	2 X 132MB	
D2352	520MB	760/19/118	71	1	425MB	16 ALT. CYL.*
D2352	520MB	760/19/118	70	2	2 X 211MB	CYLINDER MAPPED
D2352	520MB	760/19/113	72	1	411MB	
2362	800MB	850/23/128	105	1	632MB	
2362	800MB	850/23/128	106	1	627MB	16 ALT. CYL*
2362	800MB	850/23/128	107	2	311MB	

MANUFACTURER-NEC

DISK DRIVE CONFIGURATION TABLE

SWITCH 8M, 8N								MODEL	LOGICAL	LOG.	STORE REGISTER VALUES		
DECIMAL	SWITCH SETTINGS							#	CYL/HD/SEC	UNIT			
VALUE	7	6	5	4	3	2	1				WORD 1	WORD 2	WORD 3
64	1	0	0	0	0	0	0	D2257	1012/8/68	1	2200	4400	43F4
62	0	1	1	1	1	1	0	D2368	811/10/128	1	4000	8000	532B
63	0	1	1	1	1	1	1	D2368	811/5/128	2	4000	8000	532B
71	1	0	0	0	1	1	1	D2352	742/19/118	1	3B00	7600	9AE6 *
70	1	0	0	0	1	1	0	D2352	368/19/118 368/19/118	2	3B00	7600	9170
72	1	0	0	1	0	0	0	D2352	748/19/113	1	3880	7100	9AEC
105	1	1	0	1	0	0	1	2362	838/23/128	1	4000	8000	BB46
106	1	1	0	1	0	1	0	2362	832/23/128	1	4000	8000	BB40 *
107	1	1	0	1	0	1	1	2362	413/23/128	2	4000	8000	B99D

*Must be formatted as WD900

1=ON
0=OFF

MANUFACTURER-NORTHERN TELECOM

DISK DRIVE SELECTION GUIDE

MODEL #	UNFORMATTED CAPACITY	PHYSICAL CYL/HD/SEC	SWITCH VALUE DECIMAL	LOG. UNIT	FORMATTED CAPACITY	COMMENTS
8210	222MB	1029/10/66	54	1	171MB	

MANUFACTURER-NORTHERN TELECOM

DISK DRIVE CONFIGURATION TABLE

SWITCH DECIMAL VALUE	8M, 8N SWITCH SETTINGS 7	6	5	4	3	2	1	MODEL #	LOGICAL CYL/HD/SEC	LOG. UNIT	STORE REGISTER VALUES WORD 1	WORD 2	WORD 3
54	0	1	1	0	1	1	0	8210	1017/10/66	1	2100	4200	53F9

1=ON
0=OFF

MANUFACTURER-PERTEC

DISK DRIVE SELECTION GUIDE

MODEL #	UNFORMATTED CAPACITY	PHYSICAL CYL/HD/SEC	SWITCH VALUE DECIMAL	LOG. UNIT	FORMATTED CAPACITY	COMMENTS
DX199	199MB	1649/6/67	57	1	168MB	
DX265	265MB	1649/8/67	58	1	224MB	
DX332	332MB	1649/10/67	59	1	280MB	
DX332	332MB	1649/10/67	56	2	2 X 140MB	
DX300	300MB	1505/10/64	55	1	244MB	
DX332	332MB	1649/10/67	84	1	279MB	16 ALT.CYL.*

MANUFACTURER-PERTEC

DISK DRIVE CONFIGURATION TABLE

SWITCH DECIMAL VALUE	8M, 8N SWITCH SETTINGS 7	6	5	4	3	2	1	MODEL #	LOGICAL CYL/HD/SEC	LOG. UNIT	STORE REGISTER VALUES WORD 1	WORD 2	WORD 3
57	0	1	1	1	0	0	1	DX199	1637/6/67	1	2180	4300	3665
58	0	1	1	1	0	1	0	DX265	1637/8/67	1	2180	4300	4665
59	0	1	1	1	0	1	1	DX332	1637/10/67	1	2180	4300	5665
56	0	1	1	1	0	0	0	DX332	1637/5/67	2	2180	4300	2E65
55	0	1	1	0	1	1	1	DX300	1493/10/64	1	2000	4000	55C7
84	1	0	1	0	1	0	0	DX332	1631/10/67	1	2180	4300	565F*

*Must be formatted as WD900

1=ON
0=OFF

MANUFACTURER-PRIAM

DISK DRIVE SELECTION GUIDE

MODEL #	UNFORMATTED CAPACITY	PHYSICAL CYL/HD/SEC	SWITCH VALUE DECIMAL	LOG. UNIT	FORMATTED CAPACITY	COMMENTS
3350	34MB	561/3/64	53	1	26.9MB	
6650	67MB	1121/3/64	30	1	54.5MB	
15450	155MB	1121/7/64	36	1	127MB	
3450	35MB	525/5/43	37	1	28MB	
7050	70MB	1049/5/43	52	1	57MB	
803	85MB	850/5/64	65	1	68MB	
804	100MB	1050/5/64	66	1	85MB	
806	188MB	850/11/64	67	1	151MB	
807	344MB	1550/11/64	76	1	277MB	
807	344MB	1552/11/64	86	1	276MB	16 ALT.CYL*
808	480	1552/11/96	87	1	414MB	16 ALT.CYL*
808	480MB	1550/11/96	77	1	415MB	
806-23	230MB	1023/11/64	95	1	182MB	

MANUFACTURER-PRIAM

DISK DRIVE CONFIGURATION TABLE

SWITCH DECIMAL VALUE	8M, 8N SWITCH SETTINGS 7	6	5	4	3	2	1	MODEL #	LOGICAL CYL/HD/SEC	LOG. UNIT	STORE REGISTER VALUES WORD 1	WORD 2	WORD 3
53	0	1	1	0	1	0	1	3350	549/3/64	1	2000	4000	1A25
30	0	0	1	1	1	1	0	6650	1109/3/64	1	2000	4000	1C55
36	0	1	0	0	1	0	0	15450	1109/7/64	1	2000	4000	3C55
37	0	1	0	0	1	0	1	3450	513/5/43	1	1580	2B00	2A01
52	0	1	1	0	1	0	0	7050	1037/5/43	1	1580	2B00	2C0D
65	1	0	0	0	0	0	1	803	838/5/64	1	2000	4000	2B46
66	1	0	0	0	0	1	0	804	1038/5/64	1	2000	4000	2C0E
67	1	0	0	0	0	1	1	806	838/11/64	1	2000	4000	5B46
76	1	0	0	1	1	0	0	807	1540/11/64	1	2000	4000	5E02
86	1	0	1	0	1	1	0	807	1534/11/64	1	2000	4000	5DFE*
77	1	0	0	1	1	0	1	808	1540/11/96	1	3000	6000	5E02
87	1	0	1	0	1	1	1	808	1534/11/96	1	3000	6000	5DFE*
95	1	0	1	1	1	1	1	806-23	1011/11/64	1	2000	4000	5BF3

*Must be formatted as WD900

1=ON
0=OFF

MANUFACTURER-TECSTOR

DISK DRIVE SELECTION GUIDE

MODEL #	UNFORMATTED CAPACITY	PHYSICAL CYL/HD/SEC	SWITCH VALUE DECIMAL	LOG. UNIT	FORMATTED CAPACITY	COMMENTS
160	160MB	704/12/64	16	1	136MB	
166	166MB	823/10/61	31	2	2 X 63MB	
166	166MB	823/10/64	10	2	2 X 66MB	
166	166MB	823/10/64	8	1	132MB	
166	166MB	823/10/67	0	1	138MB	16 ALT.CYL*
166	166MB	823/10/67	2	2	2 X 69MB	16 ALT.CYL*
315	315MB	823/19/61	20	1	238MB	
315	315MB	823/19/64	21	1	252MB	
3-83	82MB	823/5/61	12	1	63MB	
3-83	82MB	823/5/64	13	1	66MB	
3-200	199MB	823/12/67	79	1	166.9MB	
3-300	331MB	823/20/67	80	1	278MB	

MANUFACTURER-TECSTOR

DISK DRIVE CONFIGURATION TABLE

SWITCH DECIMAL VALUE	8M, 8N SWITCH SETTINGS 7	6	5	4	3	2	1	MODEL #	LOGICAL CYL/HD/SEC	LOG. UNIT	STORE REGISTER VALUES WORD 1	WORD 2	WORD 3
16	0	0	1	0	0	0	0	160	692/12/64	1	2000	4000	62B0
31	0	0	1	1	1	1	1	166	811/5/61	2	IE80	3D00	2B2B
10	0	0	0	1	0	1	0	166	811/5/64	2	2000	4000	2B2B
8	0	0	0	1	0	0	0	166	811/10/64	1	2000	4000	532B
0	0	0	0	0	0	0	0	166	805/10/67	1	2180	4300	5325*#
2	0	0	0	0	0	1	0	166	805/5/67	2	2180	4300	2325*#
20	0	0	1	0	1	0	0	315	811/19/61	1	IE80	3D00	9B2B
21	0	0	1	0	1	0	1	315	811/19/64	1	2000	4000	9B2B
12	0	0	0	1	1	0	0	3-83	811/5/61	1	IE80	3D00	2B2B
13	0	0	0	1	1	0	1	3-83	811/5/64	1	2000	4000	2B2B
79	1	0	0	1	1	1	1	3-200	811/12/67	1	2180	4300	632B
80	1	0	1	0	0	0	0	3-300	811/20/67	1	2180	4300	A32B

*Must be formatted as WD900
#WD900 Disk Parameter-No Patching Required.

1=ON
0=OFF

2.4 INSTALLATION INTO CPU

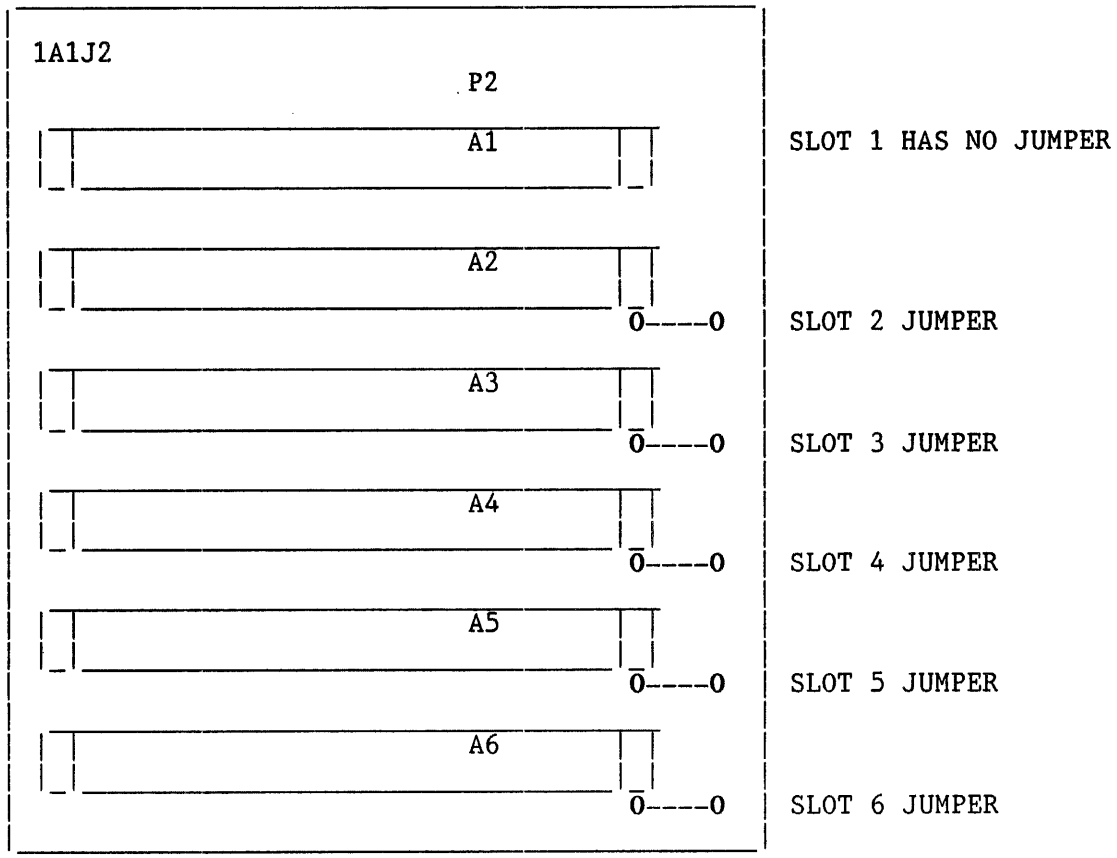
The SPECTRA 126-PLUS may be installed in any PERIPHERAL SLOT in the CPU or expansion chassis. ENSURE THAT POWER IS OFF BEFORE INSERTING OR REMOVING THE BOARD TO AVOID ANY POSSIBLE DAMAGE. DC voltage should be measured on the PCB and adjusted, if necessary, to 5 volts ±5%.

2.4.1 PREPARING a CHASSIS SLOT

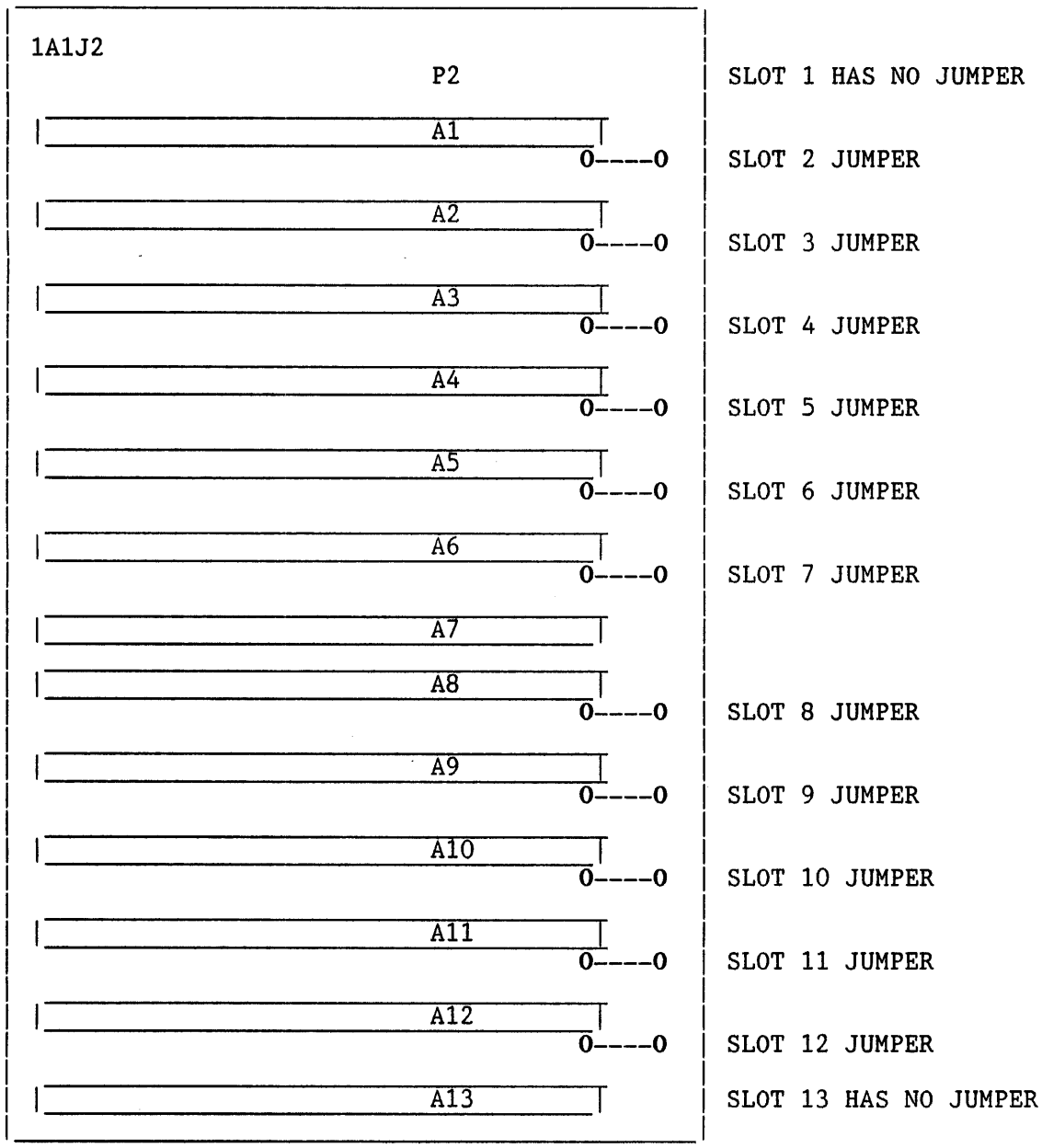
Before the SPECTRA 126-PLUS can be installed, the TILINE Access Granted (TLAG) jumper must be removed. The modifications to the various chassis versions follow. For further information, see the Model 990/10, /10A, /12, BS600, or BS800 Computer System Hardware Reference Manual. DO NOT ATTEMPT ANY MODIFICATIONS WITH AC POWER CONNECTED.

Current Production (6-slot)

1. Remove any circuit boards necessary for access to TLAG plug.
2. Remove TLAG plug for selected location.
3. Replace circuit boards.



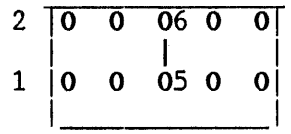
Current Production (13-slot)



Early Production (6 and 13-slot)

1. Remove left access cover.
2. Remove power supply and RF shield.
3. Cut trace or wire between P2-5 and P2-6 (TLAG).
4. Reinstall power supply, RF shield, and access cover.

The following diagram is the rear view of the 990 Motherboard (power supply side).



Current Production (17-Slot)

1. Remove the rear chassis cover.
2. The TLAG switches are located below the power supply.
3. If a switch is on, it indicates the TLAG is jumpered across slot (P2-6 to P2-5). If a switch is off, it indicates that the TLAG signal is not jumpered.

SWITCH	SLOT	SWITCH	SLOT
2-1	2	1-1	10
2-2	3	1-2	11
2-3	4	1-3	12
2-4	5	1-4	13
2-5	6	1-5	14
2-6	7	1-6	15
2-7	8	1-7	16
2-8	9	1-8	N/C

Interrupt Connections

The SPECTRA 126-PLUS has the disk interrupt available at P2-66 and the tape interrupt available at P1-66. When changing the interrupts, ensure that P1-66 and P2-66 are not connected together for the slot containing the SPECTRA 126-PLUS. For further information concerning interrupt changes, consult the System Hardware Reference Manual.

2.5 DRIVE INSTALLATION

Disk Drive

Prior to connecting the interface cables, ensure that the drive unit number and sectors per track settings are correct. Also, the drive must be set for hard sectoring (a fixed number of sectors/track). The SPECTRA 126-PLUS does not detect soft sectoring (using address marks).

To connect the interface cables to the controller board, attach the 60 conductor 'A' cable connector to the J6 header on the controller PCB. Ensure that pin 1 of the cable connector mates with pin 1 of the PCB header.

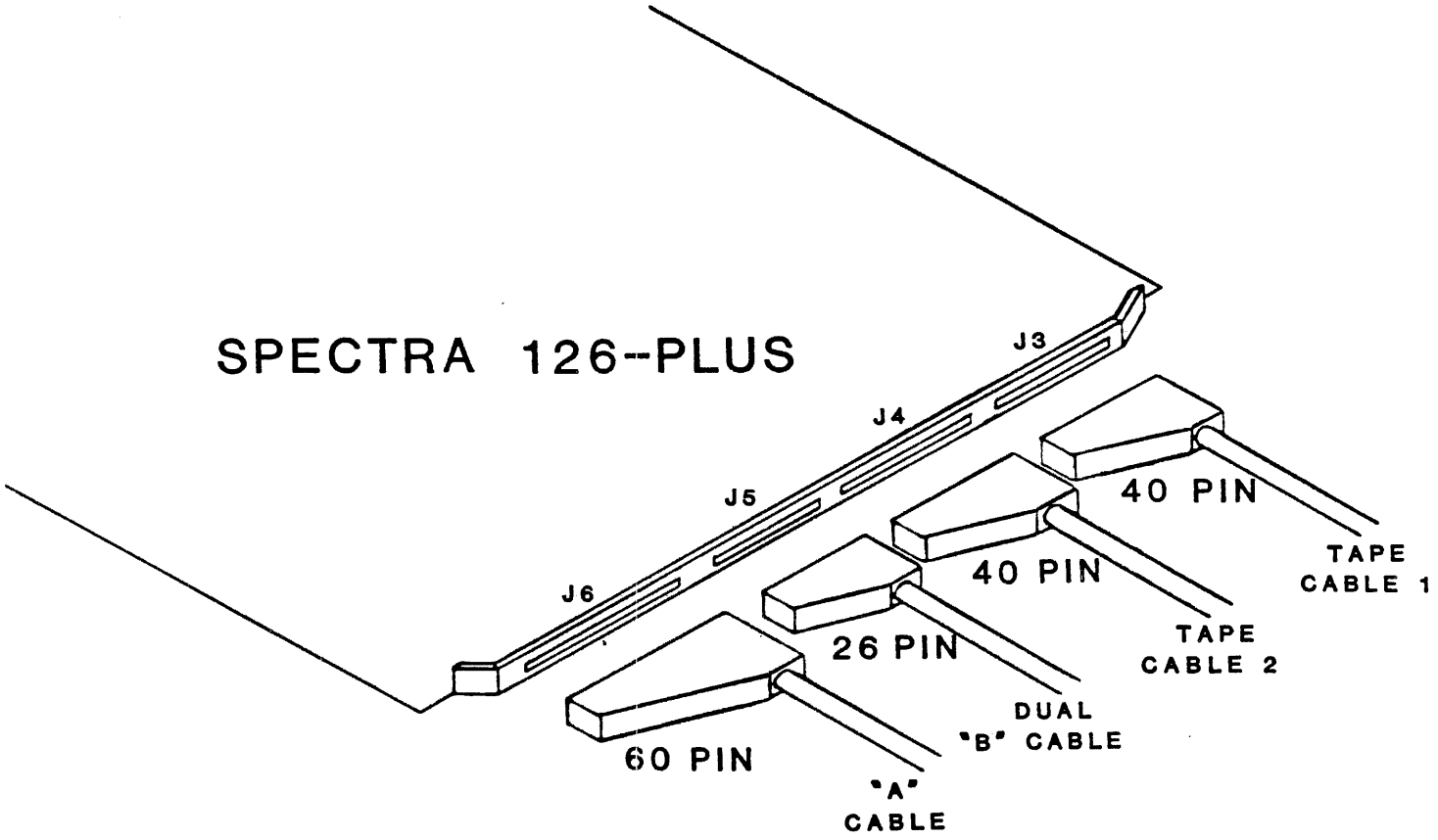
The SPECTRA 126-PLUS uses one modified 'B' connector and a Dual 'B' cable to support two disk drives. Connect the 26 conductor 'B' cable connector to the J5 header on the controller. Again, ensure that pin 1 of the cable connector mates with pin 1 of the PCB header.

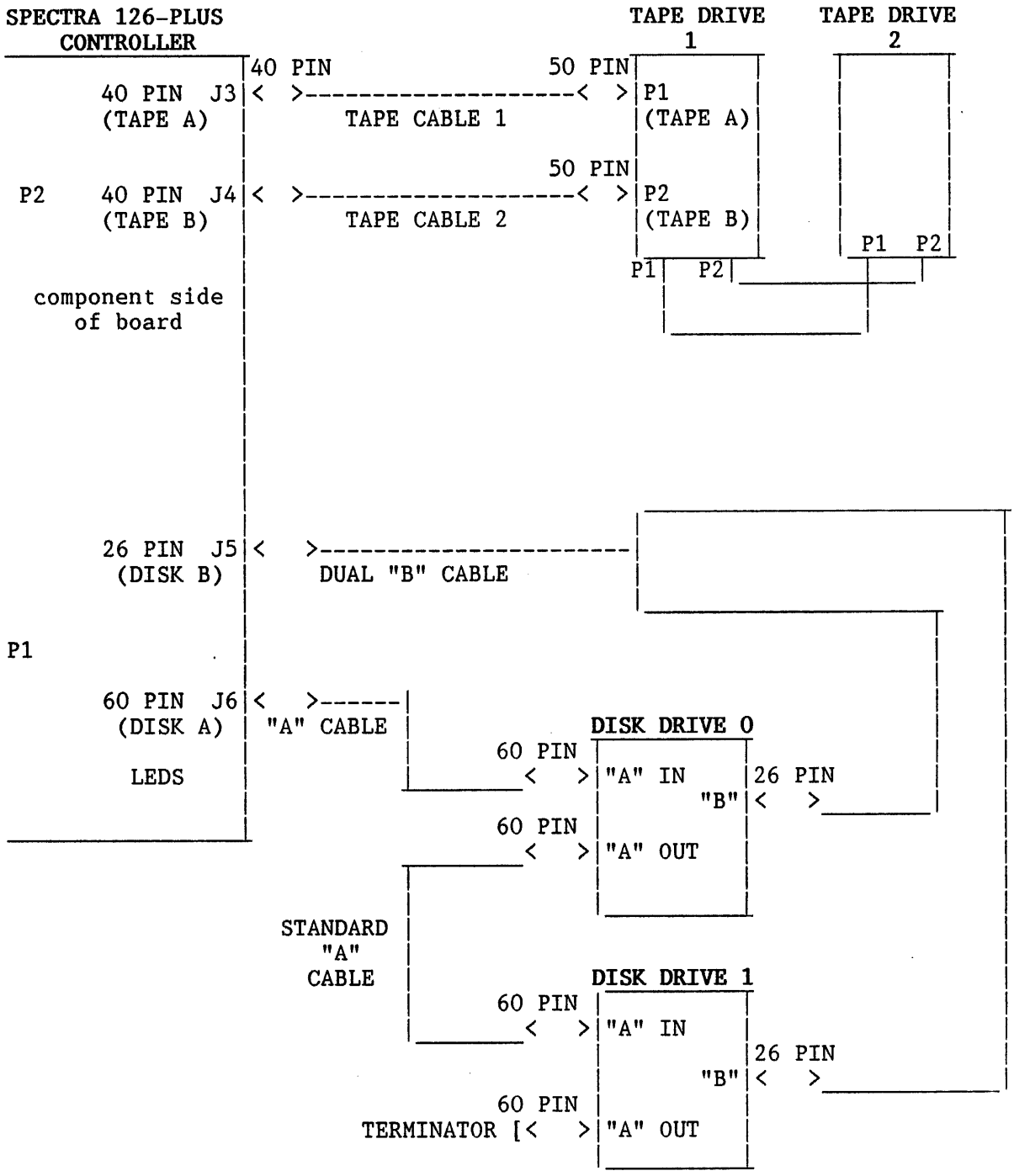
To connect the interface cables to the disk drive, route all cables neatly out of the CPU chassis. Connect the 60 conductor 'A' cable to the first disk drive, and if more than one drive is attached, daisy chain the 'A' cable between units. Install a terminator on the last drive in the chain. Then connect one 25 conductor 'B' cable to each drive. It is recommended that the ground braid on each cable be attached to each disk drive chassis.

Tape Drive

The SPECTRA 126-PLUS uses non-standard 40 conductor cables for tape. Consult the tape drive manual for the list of interface signals for each connector. Pin 2 of one connector has a signal called "FBY" or "IFBY". Normally, the cable labelled "Tape Cable 1" is only connected to J3 on the controller and to P1 of the tape drive. The cable labelled "Tape Cable 2" is only connected to J4 and to P2 on the tape drive. Ensure that Pin 1 on the tape side is mated with Pin 1 on drive.

It is recommended that the ground braid on each cable be attached to the tape drive chassis. Additional cable grounding may be required for certain peripheral types. Please contact SLC for further information.


SPECTRA 126--PLUS
J3
J4
J5
J6
40 PIN
TAPE
CABLE 1
40 PIN
TAPE
CABLE 2
26 PIN
DUAL
"B" CABLE
60 PIN
"A"
CABLE



CABLE CONFIGURATION
MAXIMUM SYSTEM PER CONTROLLER

Chapter Three

Theory of Operation

3.1 THEORY OF OPERATION

The SPECTRA 126-PLUS multifunction disk and tape controller is a dual microprocessor design employing bit slice microprogrammable technology. The two microprocessors perform independent functions to simultaneously control the TILINE interface. The microprocessor controlling the TILINE interface is referred to as the CPU Microprocessor (CM), and the microprocessor controlling SMD interface is referred to as the Disk Microprocessor (DM).

The CPU Microprocessor is responsible for command decoding, command initiation, command termination, data transfer operations, final status, and interrupt request generation. The CPU microprocessor also allocates time to the disk and tape units during concurrent data transfer operations.

The Disk Microprocessor controls the SMD interface, selects the disk drive, and generates tag and bus information to the drive. It controls read/write operations, serialization/deserialization, sector format, CRC, and ECC. Additionally, the Disk Microprocessor accesses the sector data buffer during read and write operations to transfer bytes of data between the buffer and serializer/deserializer. It also reads drive status from the SMD interface and stores it into the appropriate status register.

The two microprocessors communicate with each other through the first 304 bytes of the 4K word RAM buffer. The CM loads the disk registers as addressed during I/O write operations into the space designated in the RAM buffer. Once a command is given with the GO flip-flop set, the CM sets a flag in the buffer to inform the DM that there is a command to perform. When the DM accepts the command, it resets the flag. The DM sets the ATTENTION flip-flop when it has completed a command and updated the status. The CM waits for ATTENTION before completing the termination and setting DONE. Whenever the SPECTRA 126-PLUS does not have a command active, both microprocessors go into an idle loop. The CM waits for a new command while the DM polls the two disk drive ports to update and maintain drive status.

The upper 7616 words of the RAM data buffer are shared between the two microprocessors to provide up to 28 sectors of data buffering during read/write operations. During write operations, a sector buffer full flag is set to inform the DM once a sector of data has been transferred to the buffer from the TILINE via the CM. Additionally, a 64 byte FIFO is used to buffer data between the formatted tape drive and the CPU.

3.1.1 THE CPU MICROPROCESSOR

The CPU Microprocessor (CM) is a bit slice design using four 2901 processors and two major busses, CSRC and CDEST. The CSRC BUS is a 16-bit wide data path providing the four 2901 bit slice processors a source for their "D" inputs. Data on the CSRC BUS may be selected from TILINE data, DIP switches, tape input data, the RAM data buffer, and constants from the control store literal field. The CDEST BUS is a 16-bit wide data path used for 2901 "Y" output destination. A variety of destinations may be selected for the CDEST such as TILINE data, TILINE address, tape data, RAM data buffer address, and RAM data buffer data.

The CPU microprocessor also consists of three 2911 sequencers. The sequencers address the control store from its program counter, perform jumps, conditional jumps, subroutine jumps, and subroutine returns. Up to four levels of subroutines may be nested in the sequencer's stack. When Interrupt Enable (IE) is set, interrupts occur on memory error or TILINE address comparison.

The instruction width of the CPU microprocessor is 48 bits. Six 2Kx8 PROMs are used to form a 2Kx48 control store containing the firmware for the CM. The instruction word is defined below.

CPU MICROPROCESSOR
INSTRUCTION WORD BIT DEFINITIONS

BIT	NAME	FUNCTION
47-45	NA NEXT ADDRESS	These bits provide the next address control inputs (decoded by a 74S288 PROM) that define the type of jump to be performed.
44	TINT TILINE INTERR	This bit enables TILINE address comparison interrupt.
43	MEM ERR MEMORY ERROR	This bit enables Memory Error interrupts.
42-40	CSRC ADD 0-2 CPU SOURCE ADDRESS	These bits define one of eight sources of input to the 2901 processors on the CSRC BUS.
39-37	CDEST ADD 0-2 CPU DESTINATION ADDRESS	These bits define one of eight destinations to route output information from the 2901 processors on the CDEST BUS.
36	CCN CPU CARRY-IN	This bit enables carry-in control.

CPU MICROPROCESSOR
INSTRUCTION WORD BIT DEFINITIONS

BIT	NAME	FUNCTION
35-27	CI CPU INSTRUCTION	These bits provide the instruction input to the 2901 processors.
26-23	CRA CPU REGISTER ADDRESS	These bits supply the 2901 processors' A input address to select one of 16 registers in the 2901 processors.
22	FLGINS FLAG INSTRUCTION	For instructions using the flag field, the 2901's B input address will be the same as the A input address. For instructions not using the flag field, flag address bits 5-2 will supply the B input address.
21-16	FLGADD FLAG ADDRESS	For instructions using the flag field, these bits are decoded to select one of several flags. Depending on the address, flags may either be latched or pulsed.
15-0	CPD CPU PROM DATA	These bits supply a 16-bit constant on the CSRC BUS for instructions using a constant. For jump Instructions, bits 15-5 supply the processors with a next address. For conditional jump instructions, bits 4-0 are decoded to select a branch condition to be tested.

3.1.2 THE DISK MICROPROCESSOR

The Disk Microprocessor (DM) is a bit slice design using two 2901 processors. The two processors form an 8-bit data path to perform arithmetic, logical, and shift operations. The two major busses used by the DM are DSRC and DDEST. The DSRC bus provides an 8-bit wide data path used for the 2901 processor's input source on their "D" inputs. The firmware may select several input sources such as serializer/deserializer data, the drive configuration PROM, drive status, the data buffer, and error status. The DDEST bus provides an 8-bit wide data path used for 2901 "Y" output destination. Selectable destinations include the data buffer address, data buffer data, branch condition input, serializer/deserializer data, the serializer/deserializer control register, and the SMD interface control registers.

The DM also uses three 2911 sequencers, as used in the CM. The sequencers address the control store from its program counter, perform jumps, conditional jumps, subroutine jumps, and subroutine returns. Interrupt capability is not provided by the DM's sequencers.

The instruction width of the Disk Microprocessor is 32 bits. Four 2Kx8 PROMs are used to form a 2Kx32 control store which contains the firmware. The DM instruction word is described below.

DISK MICROPROCESSOR
INSTRUCTION WORD BIT DEFINITIONS

BIT	NAME	FUNCTION
31-30	DISK PROM DATA	These bits define the type of jump to be performed.
29-27	DSRC DISK SOURCE	These bits are decoded to determine one of 8 sources of information to be placed on the DSRC bus.
26-23	DDEST DISK DESTINATION	These bits are decoded to determine which register or control function is strobed with information on the DDEST bus.
22	DISK CARRY-IN	This bit enables carry-in control.
21-13	DISK INSTRUCTION	These bits provide the instruction input to the 2901 processors.
12	DISK FLAG ENABLE	This bit enables pulsed or latched flags to be generated from data on DPIPE 31-24.
11-0	DISK PIPELINE	These bits are stored in two LS273 registers to provide address input to the 2911 sequencers, jump target address, flag selection for instructions using the flag enable, A and B input addresses for the 2901 processors, and a constant value for instructions using a constant.

3.1.3 DISK INTERFACE

The SMD disk interface is controlled by the Disk Microprocessor. The firmware transmits information on the SMD bus and tag lines by loading the 74LS273 registers. MC3453 quad line drivers drive the SMD interface lines, and MC3450 quad line receivers are used to receive signals on the SMD interface. The DM controls selection of the logical disk drive, interrupt status from the drive, cylinder/head addressing, and READ/WRITE operations.

The serializer/deserializer uses two 74F299 registers to form a 16-bit shift register to convert data from parallel to serial during Write operations, and from serial to parallel during Read operations. During Write operations, parallel data is transferred from the data buffer and loaded 8 bits at a time into the 74F299 shift registers. During Read operations, data is transferred from the S/D shift register into two 29823 registers and then into the data buffer. The data buffer is comprised of four 1420 RAMs and two 74S374 registers.

The DM firmware is synchronized to the SMD interface by a bit counter which sets a word available flip-flop (WRDAV) each time the counter overflows. A control register is also clocked by the counter overflow to synchronize firmware control information previously stored in a 74LS273 register. This register synchronizes switching of ECC logic enable, ECC reset, and ECC clock enable. These controls are pre-loaded by the firmware into a holding register in the previous word time and are enabled at the next word available time.

The Error Correction Code (ECC) polynomial is implemented with four 74S299 registers hooked up as a barrel shifter with a parity tree providing the feedback for each term of the polynomial. The polynomial used in this design is:

$$X^{32} + X^{30} + X^{29} + X^{27} + X^{17} + X^{15} + X^{5} + X^{3} + 1$$

The ECC feedback is enabled by the CWE signal under firmware control. The clock driving the ECC logic is also enabled by firmware and may be taken from read clock, servo clock, the half frequency controller clock, or a firmware generated ECC CLK. These same four sources generate the bit clock to drive the serializer/deserializer.

3.1.4 TAPE INTERFACE

The Pertec compatible formatted tape interface is controlled by the CPU microprocessor via the CDEST bus. This 16-bit bus is clocked into two 74LS273 octal latches which drive tape control lines and initiate the micro sequencer, which consists of an octal latch and a 16L8 PAL. The micro sequencer issues clocks and other internal control signals to the magnetic tape control circuitry.

The input and output data flows through two 67402 FIFOs which create a 64 byte buffer. A 74S280 generates the Write Parity (WP) bit during Write operations. Write data is clocked off of the CDEST bus through 74LS374 latches into the FIFO buffers. Read data is clocked out of the FIFO buffers, through latches, onto the CSRC bus, and back to the CPU microprocessor.

3.2 DISK REGISTER DEFINITIONS

The control and status words on the SPECTRA 126-PLUS are used for both operating the controller and reporting disk system status. The CPU can write Control Words into controller registers to initiate operation, and can read Status Words in these registers to determine disk status upon completion of an operation. Some bits in these registers are used for disk operation control, some for status reporting, and some for both control and status. A summary of the Control and Status words is shown below.

CONTROL WORD	CPU BYTE ADDRESS	TILINE WORD ADDRESS
0	F800	FFC00
1	F802	FFC01
2	F804	FFC02
3	F806	FFC03
4	F808	FFC04
5	F80A	FFC05
6	F80C	FFC06
7	F80E	FFC07

CONTROL WORD 0

DISK STATUS

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OFL	NR	WP	UNS	EC	SKI	OSA	PC	ATA	ATA	ATA	ATA	AIM	AIM	AIM	AIM

CONTROL WORD 1

FORMAT AND COMMAND

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
EXA	EXB	SE	SL	TIH	COM	COM	COM	OS	OSF	HA	HA	HA	HA	HA	HA

CONTROL WORD 2

SECTOR

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
SPR	SPR	SPR	SPR	SPR	SPR	SPR	SPR	SSA	SSA	SSA	SSA	SSA	SSA	SSA	SSA

CONTROL WORD 3

CYLINDER ADDRESS

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA

CONTROL WORD 4

WORD COUNT

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC

CONTROL WORD 5

MEMORY ADDRESS

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MA	MA	MA	MA	MA	MA	MA	MA	MA	MA	MA	MA	MA	MA	MA	MA

CONTROL WORD 6

SELECT AND MEMORY ADDRESS

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	DS	DS	DS	DS	0	0	0	MA	MA	MA	MA	MA

CONTROL WORD 7

CONTROLLER STATUS

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
IDL	CP	ERR	INT	LO	RT	ECC	AC	ME	DE	TO	IE	RE	CT	SE	UE

CONTROL WORD 0 DISK STATUS

This word contains disk status codes for the selected drive. It also contains attention bits and attention mask bits for generating interrupts.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OFL	NR	WP	UNS	EC	SKI	OSA	PC	ATA	ATA	ATA	ATA	AIM	AIM	AIM	AIM

BIT	NAME	FUNCTION
0	OFL Offline	Set if the drive is not powered on, not up to speed, does not have a cartridge or pack loaded, or is in an unsafe condition.
1	NR Not Ready	When set, indicates that the drive is off line or executing a RESTORE command.
2	WP Write Protect	When set, indicates that the drive is write protected.
3	UNS Unsafe	When set, this bit indicates that the drive is in an unsafe condition preventing normal disk operation. Cleared by issuing a RESTORE or a STORE REGISTERS command (if the unsafe condition no longer exists).
4	EC End of Cylinder	This bit is always zero.
5	SKI Seek Incomplete	Set when the drive fails to complete a seek operation and reports seek incomplete status. A restore operation is required to recover.
6	OSA Offset Active	Not used. Always zero.
7	PC Pack Change	This bit is set if the drive has lost power, if the drive is spinning up, or if regaining cabling to CPU
8-11	ATA Attention	Attention bits for drives 0-3.
12-15	AIM Attention Interrupt Mask	If an Attention Mask bit and its corresponding attention bit are both set, an interrupt to the 990 is generated. These bits are used with overlap seek operation on multiple non-mapped disk drives.

CONTROL WORD 1 FORMAT AND COMMAND

This word contains command codes, head address, and several control bits used during certain data recovery operations.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
EXA	EXB	SE	SL	TIH	COM	COM	COM	OS	OSF	HA	HA	HA	HA	HA	HA

BIT	NAME	FUNCTION
0-1	EXT A&B Extended Commands A&B	These bits work in conjunction with the command bits 7-5 so that they are interpreted as ten additional commands.
2	SE Strobe Early	When set, this bit enables a strobe early condition.
3	SL Strobe Late	When set, this bit enables a strobe late condition.
4	TIH Transfer Inhibit	When set, this bit inhibits the transfer of data to the TILINE interface during read operations. Data is checked for ECC errors with no transfer to main memory
5-7	COM Command	These bits represent normal commands. The commands are shown in table 3-1.
8	OS Head Offset	This bit is used in conjunction with bit 9 to offset the heads forward or reverse from nominal during reads
9	OSF Head Offset	This bit is set to 1 for offset forward, and to 0 for offset reverse.
10-15	HA Head Address	These bits select the Read/Write heads as follows: 15 = H_1 14 = H_2 13 = H_4 12 = H_8 11 = H_{16} 10 = H_{32}

TABLE 3-1 COMMAND CODES

BIT 0	BIT 1	BIT 5	BIT 6	BIT 7	COMMAND
0	0	0	0	0	STORE REGISTERS
0	0	0	0	1	WRITE FORMAT
0	0	0	1	0	READ DATA
0	0	0	1	1	WRITE DATA
0	0	1	0	0	READ UNFORMATTED (3)
0	0	1	0	1	WRITE UNFORMATTED
0	0	1	1	0	SEEK (1)
0	0	1	1	1	RESTORE
1	0	1	0	0	READ UNFORMATTED
1	0	1	1	1	SELF-TEST (2)
1	1	0	0	1	ABSOLUTE WRITE
0	1	0	0	1	RELOCATE
0	1	1	0	0	SURFACE ANALYSIS ASSIST

NOTES: 1) Seek commands are ignored for mapped drives.

2) SPECTRA 126-PLUS microdiagnostics are not the same as the LDECC self-tests. See section 4.3.

3) Does not actually read from disk. See section 3.2.2.

CONTROL WORD 2 SECTOR

This word contains bits which select the starting sector address and determines the number of sectors per record on the disk.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
SPR	SPR	SPR	SPR	SPR	SPR	SPR	SPR	SSA	SSA	SSA	SSA	SSA	SSA	SSA	SSA

BIT	NAME	FUNCTION
0-7	SPR Sectors Per Record	These bits are ignored by the controller.
8-15	SSA Starting Sector Address	These bits select the starting sector address for all Read and Write operations (except WRITE FORMAT which does not require a starting sector address).

CONTROL WORD 3 CYLINDER

This word contains the cylinder address.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA

BIT	NAME	FUNCTION
0-15	CA Cylinder Address	These bits select the cylinder address. Bit 15 is the least significant cylinder weight, ascending from right to left.

CONTROL WORD 4 WORD COUNT

This word specifies the number of bytes to be transferred between the disk and CPU memory.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC

BIT	NAME	FUNCTION
0-15	TBC Transfer Byte Count	These bits specify the number of bytes to be transferred. The byte count must be an even number. Up to 64K bytes may be transferred.

CONTROL WORD 5 LSB MEMORY ADDRESS

This word contains the 15 least significant bits of the 20-bit TILINE memory address.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MA	MA	MA	MA	MA	MA	MA	MA	MA	MA	MA	MA	MA	MA	MA	MA

BIT	NAME	FUNCTION
0-15	MA Memory Address	Bits 14-0 contain the 15 least significant bits of the 20-bit TILINE starting memory address. Bit 15 is always zero. The 5 most significant bits are in word 6

CONTROL WORD 6 SELECT AND MSB MEMORY ADDRESS

This word contains drive select codes and the 5 most significant bits of the 20-bit TILINE memory address.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	DS0	DS1	DS2	DS3	0	0	0	MA	MA	MA	MA	MA

BIT	NAME	FUNCTION
0-3	-----	Not used. Always zero.
4-7	DS 0-3 Drive Select	These bits contain drive select codes. They should be set one at a time.
8-10	SPARE	Not used. Always zero.
11-15	MA Memory Address	Bits 15-11 contain the 5 most significant bits of the 20-bit TILINE starting memory address.

CONTROL WORD 7 CONTROLLER STATUS

This word contains controller status codes, the Interrupt Enable (IE) bit, and the idle/busy bit.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
IDL	CP	ERR	INT	LO	RT	ECC	AC	ME	DE	TO	IDE	RE	CTO	SE	UE

BIT	NAME	FUNCTION
0	IDL Idle	When set, this bit indicates that the controller is not busy and ready to accept a new command.
1	CP Complete	Set when the controller completes a command without error.
2	ERR Error	Set if an error is detected. Bits 15-7 provide the detailed error indicators.
3	IE Interrupt	This bit must be set to enable the controller to generate an interrupt on completion of a command. If IE is set while the controller is idle and the Complete or Error bit is set, an interrupt is generated immediately. Attention interrupts in word 0 are independent of the Interrupt Enable bit.
4	LO Lock Out	This bit is set when control word 7 is read.
5	RE Retry	Set when the controller encounters a data error causing a re-read operation to be performed.
6	ECC Corrected	Set when the controller corrects data within its buffer during a Read operation.
7	AC Abnormal Condition	Set if a disk operation is terminated due to an I/O reset, TILINE power fail warning, TILINE power reset, or if a WRITE FORMAT or WRITE UNFORMATTED command is issued with the Format Enable switch disabled.
8	ME Memory Error	Set if a TILINE memory error is detected during a disk Write operation. Any data transfer operation is terminated upon detecting a Memory Error.

CONTROL WORD 7 CONTROLLER STATUS [continued]

BIT	NAME	FUNCTION
9	DE Data Error	Set if an uncorrectable ECC error is detected during a Read operation.
10	TO Time-Out	Set if the controller's 10 microsecond timer expires before any TILINE cycle has completed. May be caused by attempting to access non-existent memory.
11	IDE ID Error	Set if an ID word non-comparison occurs during ID verification of ID words 1, 2, or 3 executing a READ DATA or WRITE DATA command.
12	RE Rate Error	Set if the TILINE is unable to keep up with the disk. This error cannot occur due to 28 sector buffering.
13	CTO Command Time Out	Set if the controller fails to complete an operation before the command timer expires.
14	SE Search Error	Set if the controller fails to detect a sync character within a physical sector during a Read operation.
15	UE Unit Error	Set if an operation is terminated due to a disk drive error.

The following table shows how a combination of bits 15 to 13 (word 7) is used to flag errors more specifically after a format command.

BIT 13	BIT 14	BIT 15	
0	1	0	SECTOR/INDEX SEARCH TIMEOUT
0	1	1	SECTOR COUNT ERROR
1	0	1	LOSS OF SERVO CLOCK

3.2.1 PROGRAMMING THE CONTROLLER

The SPECTRA 126-PLUS controller may be programmed using the eight control and status words previously described. Each control word must have the appropriate bits set or reset, depending on the desired operation. The control words must then be transmitted to the controller so that the operation may be executed. An operation is immediately executed when the controller receives Control Word 7 with bit 0 reset; therefore, Control Word 7 must be transmitted last.

Transmitting a new set of Control Words to the controller destroys the status words from the previous operation, except for the disk status bits (0-11) of Word 0. The disk status bits are set by the disk drive and cannot be modified by overwriting with a new Control Word. If overwriting is attempted, the controller does not acknowledge the new settings of the disk status bits.

Before issuing a command to the controller, bit 0 in Word 7 should be checked to verify that the controller is idle and ready to accept the command. The controller becomes busy only when it has been given a command. If bit 0 in Word 7 is zero (busy) when attempting to read status, bits 1 through 15 of this word become meaningless. If a command is issued to the controller after an operation has already been initiated, the attempt seems to complete normally, but the controller ignores the command.

3.2.2 NORMAL COMMAND DESCRIPTIONS

STORE REGISTERS COMMAND

The STORE REGISTERS command allows the operating system software to determine critical disk parameters, such as words per track and cylinders available per drive unit. This command causes the controller to send one, two, or three words to the 990 memory from the disk system, starting at the memory address specified in Control Words 5 and 6, and specified by the word count in Control Word 4. The three words contain the following information:

WORD 0: Word 0 is the total number of unformatted words that can be recorded on a disk track. For the SPECTRA 126-PLUS controller, there is a fixed format as indicated by the zero value in the bytes of overhead per sector parameter. The word zero value defaults to formatted words per track.
(Unformatted words = 128 words per sector x sectors per track).

WORD 1: Bits 0-7 of word 1 specify the number of sectors per track, and bits 8-15 specify the number of bytes of overhead per sector.
(Always zero for the Spectra 126-PLUS controller).

WORD 2: Bits 0-4 of word 2 specify the number of track/heads per cylinder, and bits 5-15 specify the number of cylinders per drive.

WRITE FORMAT COMMAND

The WRITE FORMAT command formats a new disk or reformats a disk already in service. One complete track is formatted per command. After receiving all command words, the controller verifies that there are no disk status errors (such as offline, not ready, unsafe, write protect, offset active, or seek incomplete), seeks to the specified cylinder, and sets the specified head address. A verify ID and ECC is done after the seek. Relocation from a bad track to a spare track is allowed with the spare track being formatted. If the verify ID fails due to a data or search error, the track is formatted; however, the verify ID or search error is retried up to three times before formatting. The WRITE FORMAT command also returns ID error status if the ID is invalid and no ECC errors exist. If these errors are encountered during the verify ID, retries are returned. The controller assembles the ID words from its internal registers and counters and records the word(s) on the disk at the specified disk track address. The controller then records the data field following the ID words with the data word in the specified TILINE address. This is repeated for all data word positions and ECC. The controller formats each sector on the track with ID words, data, ECC, and the required gaps. Each sector has a physical data field of 128 words (256 bytes). All sectors contain ID words and the ECC field.

READ DATA COMMAND

The READ DATA command identifies a record location, specifies the number of bytes to be transferred from this location, and gives the starting address for the TILINE memory address buffer area to receive data from the disk.

After firmware initialization, the controller performs the following operations:

1. Checks for unit errors by examining the disk status bits (Offline, Offset Active, Not Ready, Unsafe, and Seek Incomplete).
2. Seeks to the specified cylinder.
3. Sets the specified head address.
4. Locates the desired sector by reading sectors into the sector buffer and checking the ID Words. If the Words contain the defective track bit (no ECC error existing), another SEEK is issued to the head and cylinder address specified in the data field, and the operation continues on the alternate track.
5. Transfers the Data Words to the specified TILINE address.

A failure to verify an ID Word results in an ID Error Status (bit 11) and termination of the Read Data operation. If the ECC is incorrect for the sector where data is being read, Data Error Status (bit 9) is also set. When the controller encounters the end of a sector, but the remaining Transfer Word is nonzero, the controller automatically continues reading data on the next sequential logical sector (if it exists). The controller automatically switches heads and/or cylinders, if necessary, to access the next logical sector.

When the remaining transfer word count is zero but the controller has not encountered the end of a sector, the controller discontinues transmitting Data Words across the TILINE. However, it does continue to read data from the disk until the end of the sector is encountered so that the ECC character can be checked before loading status.

When the controller encounters the end of a track and the remaining word count is nonzero, the controller automatically increments the head address to the next track. The controller then repeats steps 4 and 5 in the list above.

When the controller encounters the end of a cylinder and the remaining transfer count is nonzero (and head offset is not specified), the controller automatically seeks to the next cylinder and selects head address zero for the new track. The controller then repeats steps 4 and 5 in the list above.

WRITE DATA COMMAND

The WRITE DATA command causes the controller to record data on a previously formatted track, or to write over a previously recorded sector. After firmware initialization, the disk controller performs the following operations:

1. Checks for unit errors by examining disk status (Offline, Not Ready, Unsafe, Write Protect, Offset Active, or Seek Incomplete).

2. Seeks to the specified cylinder.

3. Selects the specified head address.

4. Locates the desired starting sector by reading the ID Words of each sector and comparing its contents to the desired sector address. If the Words contain the defective track bit and no ECC errors exist, another SEEK is issued to the head and cylinder address specified in the data field and the operation continues on the alternate track. When the controller detects the sector immediately before the desired sector, it arms the interface so that the Write operation is started when the next sector mark occurs.

5. Writes a leading gap, a synchronization character, header, 256 bytes of data from the specified TILINE memory location, and an ECC character. It also leaves a trailing gap at the end of the sector.

If the ID Words in step 4 do not compare, the Write operation is terminated with an ID status error.

Data is written on the disk, sector by sector, until the specified number of words have been transferred (unless a terminate condition is encountered). When the transfer word count is less than the sector word count, the controller fills the remainder of the sector with zeroes until the sector word count has been decremented to zero. When the number of words is greater than the words per sector, the controller continues to the next sequential sector.

When the controller encounters the end of a track and the remaining transfer word count is nonzero, the controller automatically increments the head address to the next track and selects sector 0 as the next sector to be written. The controller then repeats steps 4 and 5 of the list above.

When the controller encounters the end of a cylinder and the remaining transfer word count is nonzero, the controller automatically seeks to the next cylinder, selects head address zero for the new cylinder, and selects sector 0 as the next sector to be written. The controller then repeats steps 4 and 5 in the list above.

UNFORMATTED READ COMMAND

The UNFORMATTED READ command is included to insure compatibility with Texas Instruments' device service routines that acquire disk parameters by reading header information. This non-extended command does not actually read any data from the disk. Instead, three Words are returned to the CPU after this command is executed. The first Word returned contains the head and cylinder addressed, the second Word contains the number of sectors per record (01), and the third Word contains the record word count (80). If a genuine Unformatted Read operation is desired, the extended UNFORMATTED READ command may be used.

UNFORMATTED WRITE COMMAND

An UNFORMATTED WRITE command transfers up to 510 bytes of data from a specified TILINE address to a specified disk address. After firmware initialization, the controller seeks to the specified cylinder, selects the specified head address, detects the beginning of a sector, generates the correct lead gap, writes a sychronization character, and writes data on the disk. All data is written consecutively without regard to existing sector boundaries until the specified number of words has been transferred, or until a termination condition is encountered. The controller adds an ECC character and a trailing gap at the end of the data. The maximum transfer count is 510 bytes.

SEEK COMMAND

The SEEK command causes the drive to orient the heads at the cylinder specified in the Command Words. An interrupt may be generated, if desired, to alert the CPU that this operation has been completed.

If the heads are located on a common carriage assembly (as in the CMD disk drive), independent Seek operations cause the assembly to move all heads to the next specified recording or reading location and then return to the original track to finish the operation. This head thrashing is eliminated by ignoring (NOP) any pre-SEEK command from the software to the CMD disk drive.

On other types of drives not using a common carriage for two drive units, Seek operations are performed normally. If two or more of these drives are daisy chained, independent OVERLAPPED SEEK commands may be used.

RESTORE COMMAND

The RESTORE command re-initializes the cylinder counter and repositions the heads of the disk drive over cylinder zero. The RESTORE command is generally used to clear an Unsafe condition at the disk drive, but is required if Seek Incomplete or Unsafe status is detected. Before executing the Restore operation, the controller examines the Offline bit for a disk status error. If a disk status error is detected before the RESTORE command is initiated, the controller sets the Unit Error bit in Control Word 7. Completion of the Restore operation may be determined by enabling a disk drive completion interrupt (Attention bit interrupt), or by monitoring the Attention bit for the selected drive unit.

3.2.3 EXTENDED COMMAND DESCRIPTIONS

The extended commands set the Extended Mode bits (Control Word 1, bits 0 and 1). The extended mode bits allow the command code field (Control Word 1, bits 5-7) to select from an additional set of commands. These commands are less commonly used during the course of data storage and retrieval operations.

READ UNFORMATTED COMMAND

The extended READ UNFORMATTED command allows the programmer to read a sector and to examine a specified number of words starting immediately after the sync character without regard to ECC errors or standard sector formatting. This is primarily a diagnostic feature.

After firmware initialization, the controller selects the proper head and seeks to the specified cylinder. When the sector is located, the controller transfers the specified number of words to TILINE memory, starting with the first word after the sync character.

The ID words, data fields, ECC words, and trailing gap are read and transferred to memory as data words. There are normally glitches in the trailing gap due to write head turn-on and turn-off transients and differing write clock phases recorded during Formatting and Write operations. These glitches may cause shifting of word boundaries when the word count is large enough to require data to be written beyond the normal position of the ECC characters.

An ECC check is performed at the end of the operation, and data error status is reported if the ECC check shows an error. However, no ECC correction is attempted. A data error will occur unless the byte count is the correct value to allow a comparison between the calculated ECC checkbits and the read checkbits.

The word transfer count is limited to 510 bytes, and a command TIME-OUT occurs if too many bytes are requested. The extended READ UNFORMATTED command may also be used to read the information.

SELF-TEST COMMAND

This command causes the controller to execute Self-Test routines. The Self-Test routines are not individually selectable, but in order to maintain compatibility, the upper byte of Control Word 3 is copied into the lower byte of Control Word 2 upon successful completion of the SELF-TEST command. The controller self-test may be called from the extended command field by entering 8700 (hexadecimal) in Control Word 1, and 0000 (hexadecimal) in Control Word 3. A loop on all self-tests occurs when 8000 (hexadecimal) is entered in Control Word 3; an I/O RESET must be issued to exit this loop. Word 7 should be the last word entered. If the SELF-TEST command fails, it causes all ones to be reported in the right byte of Control Word 7, and two 16-bit failure codes to be written to Control Word 2 and 4. Control Words 2 and 4 may give more information concerning any failure.

Additional status information may be obtained by setting the appropriate bits in register 3. Placing 7C (hexadecimal) in the upper byte of this register causes the controller to report the revision of the disk firmware PROMs in the lower byte of the register. There are four additional commands available to obtain extended status from disk drives that support TAG4 and TAG5. The desired drive status is returned in the lower byte of register 3 by setting the appropriate bits (see the table below) in the upper byte of register 3. Consult the appropriate drive manual for the proper setting of TAG4 and TAG5, bits 3 and 4.

REGISTER 3 - EXTENDED SELF TEST COMMANDS

COMMAND	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
EXECUTE SELF TEST	0	0	0	0	0	0	0	0
LOOP ON SELF TEST	1	0	0	0	0	0	0	0
READ PROM REVISION	0	1	1	1	1	1	0	0
EXTENDED STATUS	0	0	1	TAG4	TAG5	1	0	0

Drive status is obtained by using TAGS 4 and 5 and returned in the lower byte of register 3 as follows:

BIT 8	BIT 9	BIT 10	BIT 11	BIT 12	BIT 13	BIT 14	BIT 15
STATUS 7	STATUS 6	STATUS 5	STATUS 4	STATUS 3	STATUS 2	STATUS 1	STATUS 0

ABSOLUTE WRITE FORMAT COMMAND

The ABSOLUTE WRITE FORMAT command is non-relocatable. The controller checks for unit errors by examining disk status (Offline, Not Ready, Unsafe, Write Protect, Offset Active, or Seek Incomplete). It also seeks to the specified cylinder, sets the specified head address, waits for the correct starting sector, and formats the track with the fill word specified by the TILINE address. The format of this command is as follows:

WORD 0: Always zero.
WORD 1: Most significant byte = $C1_{16}$, least significant byte = head address of the track.
WORD 2: 0100.
WORD 3: Cylinder address of the track.
WORD 4: TILINE byte count = 0002_{16}.
WORD 5: TILINE address.
WORD 6: TILINE address and unit address.
WORD 7: Always zero.

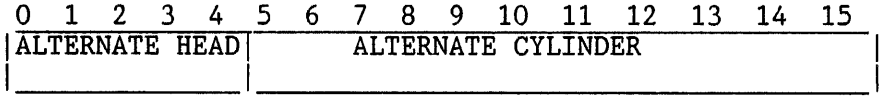
RELOCATE COMMAND

The RELOCATE command is issued by the Surface Analysis program. The Surface Analysis program acknowledges the alternate cylinders by performing a surface check on all physical cylinders and keeping a record of the defective tracks. At the end of the program, the defective tracks on any logical cylinders are assigned to good alternate tracks within the reserved cylinders by using the RELOCATE command. The format of this command is as follows:

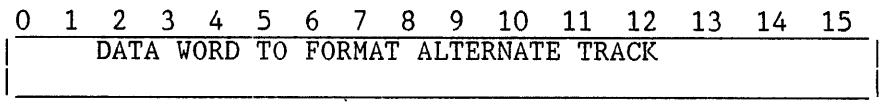
WORD 0: Always zero.
WORD 1: Most significant byte = 41_{16}, least significant byte = head address of the bad track.
WORD 2: Always 0.
WORD 3: Cylinder address of the bad track.
WORD 4: TILINE byte count = 0004_{16}.
WORD 5: TILINE address.
WORD 6: TILINE address and unit address.
WORD 7: Always zero.

After verifying the ID of the bad track, the RELOCATE command reads two words from memory. These words are shown below.

WORD 0



WORD 1



The RELOCATE command then formats sectors on the defective track with the following format.

WORD 0

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CYLINDER ADDRESS															

WORD 1

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
HEAD ADDRESS								SECTOR ADDRESS							

WORD 2

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

WORD 3-258

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ALTERNATE HEAD								ALTERNATE CYLINDER							

WORDS 259-260

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ECC FIELD GENERATED BY THE CONTROLLER															

Having formatted the defective track, the controller seeks to the alternate track and formats it before terminating the command. The format of the alternate track is as follows.

WORD 0

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DEFECTIVE CYLINDER ADDRESS															

WORD 1

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
BAD HEAD ADDRESS								SECTOR ADDRESS							

WORD 2

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

WORD 3-258

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DATA WORD FROM MEMORY															

WORDS 259-260

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ECC FIELD GENERATED BY THE CONTROLLER															

RELOCATE COMMAND [continued]

If a normal READ or WRITE command is now issued to a track marked as defective, the controller reads the alternate information, seeks to the alternate track, and executes the command. On termination of a normal READ or WRITE command, the TILINE control space is the same as if no defective track existed.

If a normal READ or WRITE command is issued directly to the alternate track, the command fails and ID ERROR is set. The alternate track can be read indirectly via the defective track or with a READ UNFORMATTED EXTENDED command to the alternate track. The defective track must be read with a READ UNFORMATTED EXTENDED command.

The Drive Configuration PROM contains the number of cylinders in the drive minus those reserved for alternate tracks. Any even number from 0-30 may be reserved by having an appropriate value in the Configuration PROM. The STORE REGISTERS command reports the number of logical cylinders minus those assigned as alternates.

SURFACE ANALYSIS ASSIST COMMAND

The SURFACE ANALYSIS ASSIST command assists in locating and defining bad tracks. It performs a bit by bit comparison of data recorded on the disk in order to identify possible errors on the disk surface. This command tests portions of GAP1, GAP2, SYNC, HEADER, data, and ECC fields. Using the Surface Analysis Assist command options, a READ/WRITE or READ only command using a single data pattern may be issued to either multiple heads or to a single head. The format for the SURFACE ANALYSIS ASSIST command is as follows:

WORD 0: Always zero.
WORD 1: Most significant byte = 44_{16}, least significant byte = head address.
WORD 2: Always 0.
WORD 3: Cylinder address.
WORD 4: Buffer length (2 + input length + output length).
WORD 5: TILINE address.
WORD 6: TILINE address and unit address.
WORD 7: Always zero.

The TILINE buffer is defined as follows:

ADDRESS 0: Spare (may be used for buffer count).
ADDRESS 1: Read types, write and cylinder flags with the format:

OF	OR	SE	SL	NOM	EF	ER	LF	LR	0	0	0	0	0	WR	CYL

SURFACE ANALYSIS ASSIST COMMAND [continued]

If CYL is set, SURFACE ANALYSIS ASSIST runs from the specified starting head to the maximum head address; if CYL is reset, SURFACE ANALYSIS ASSIST runs for the specified head only. If WR is set, SURFACE ANALYSIS ASSIST writes to specified locations; if WR is reset, SURFACE ANALYSIS ASSIST runs in the read only mode.

ADDRESS 2: Format pattern.
ADDRESS 3: Failing read types for the starting head with the format:

OF	OR	SE	SL	NOM	EF	ER	LF	LR	0	0	0	0	0	0	0

ADDRESS 4: Last sector and defect length (1st byte is the failing physical sector, 2nd byte is the defect length) for 1st head.
ADDRESS 5: Failing read type for 2nd head.
ADDRESS 6: Last sector and defect length (1st byte is the failing physical sector, 2nd byte is the defect length) for 2nd head.
ADDRESS n: Failing read types (maximum head address).
ADDRESSn+1: Last sector and defect length (1st byte is the failing physical sector, 2nd byte is the defect length).

During SURFACE ANALYSIS ASSIST command execution, the SPECTRA 126 performs the following operations:

1. Gets the read types, flags and clears the specified buffers.

2. Seeks to the specified track.

3. Issues track format (if the write flag is set) for all heads.

4. Issues track read for all specified read types.

5. If any errors occur, the SPECTRA 126-PLUS fills in the appropriate buffers with the failing read type and defect length from the first to the last defect. The sector reported will be a failing physical sector address. Controller status of search error and data error can occur together indicating that both of these conditions exist in the track read. Controller status is the sum of status for all tracks; therefore, it is necessary to examine the output buffer to determine which heads failed with which read types. A defect length of zero will be reported for search errors unless a defect length other than zero can be determined by previous or subsequent reads. A defect length count of 255 hexadecimal will be reported for defects that are either 255 bits in length (or greater), or for defects that span multiple sectors.

3.2.4 COMMAND COMPLETION

Upon completion of an operation, the controller will generate an interrupt to the CPU if the Interrupt Enable (IE) bit in Control Word 7 is set. The SPECTRA 126 controller may be used with either an interrupt driven or a polled device service routine.

Command Completion Without Interrupts

To check command completion or controller availability in a polled system, it is necessary to read Control Word 7 periodically to check bit 0 for idle status. If the bit is set, it indicates that the controller is idle and available to accept commands; if the bit is reset, it indicates that the controller is busy.

When controller operation begins, the software initiates a timing loop and checks the Idle bit at timer expiration. If the idle bit is still zero, the timer may be restarted and the sequence may be repeated a preselected number of times. This method requires more software overhead than the interrupt driven approach.

If a RESTORE or INDEPENDENT SEEK command is initiated, the disk may not be ready even after the controller has reported completion. To determine if the disk has completed a RESTORE or INDEPENDENT SEEK command, the software should check the drive status bits of Control Word 0. If the disk drive has finished the operation, the attention line for the selected drive will be set, and either the Not Ready bit will be inactive or the Seek Incomplete bit will be set. The Independent Seek operation is intended for use with SMD type drives, not with CMD type drives.

Command Completion With Interrupts

The controller may issue two types of interrupts to the computer. One type of interrupt is issued when the controller completes a command, and the other type is issued when the disk drive completes an operation. Most disk drive operations are completed when the controller has completed a command. For independent Seek and Restore operations, however, the controller completes the command before the drive completes the operation. The drive completion interrupt may then be used to determine when the system is again ready.

In order to have the controller issue an interrupt to the processor upon command completion, the Interrupt Enable (IE) bit in Control Word 7 must be set when the operation is initiated. When the controller returns to idle, the interrupt is issued to the CPU. This interrupt is cleared by resetting the IE bit or the appropriate completion bit in Control Word 7.

Drive completion interrupts are issued when the attention bit and mask bit for any disk drive unit are both set, setting the interrupt line to the computer. Control Word 0 contains four attention lines (one for each of the four disk drive unit addresses) and four attention mask lines. Each drive's attention line is set when either the disk drive is ready or a seek error has occurred.

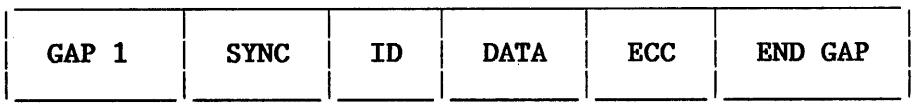
Command Completion With Interrupts [continued]

The mask bits may be set or reset using any of the computer memory instructions. However, the attention bits and disk status bits are set only by the controller, to indicate current disk operation status.

To use the drive completion interrupts during a Restore operation, first issue the RESTORE command to the controller. After the controller reports command completion (by a controller Idle or command completion interrupt), set the mask bit corresponding to the desired drive. When the drive finishes the Restore operation and the controller is idle, an interrupt is issued to the CPU. The interrupt may be cleared by resetting the mask bit corresponding to the interrupting drive. The controller resets all controller interrupts when it switches from an idle to a busy condition.

3.3 DISK FORMAT

Sector Format:



FIELD	CONTENTS
*GAP 1	35 bytes of zeroes.
SYNC	2 bytes, hexadecimal A7CC.
ID	6 bytes containing head, cylinder, and sector addresses, plus a flagged track indicator.
DATA	256 bytes of system data.
ECC	4 bytes of Error Correction Code.
END GAP	A variable number of bytes per sector (usually 12).

* GAP 1 is 20 bytes if bit 2 of byte 1 in the Drive Configuration PROM is set.

DS80/DS300/WD900 ID FIELD

The ID field used to perform position verification and flag tracks has the following format:

ID WORD 0

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	CYL	CYL	CYL	CYL	CYL	CYL	CYL	CYL	CYL	CYL

BIT	NAME	FUNCTION
0-4	-----	Not used. Always zero.
5	CYL Cylinder Address MSB	This bit is to be used with Ampex 160 MB drives or the equivalent as the 1024 weight cylinder bit.
6-15	CYL Cylinder Address	These bits contain the cylinder address which ranges from 0-1023. Bit 15 is the Least Significant Bit. The maximum address range with bit 5 is 2047.

ID WORD 1

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
HA	HA	HA	HA	HA	HA	HA	HA	SA	SA	SA	SA	SA	SA	SA	SA

BIT	NAME	FUNCTION
0-7	HA Head Address	These bits contain the head address.
8-15	SA Sector Address	These bits contain the sector address.

ID WORD 2

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
BTF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	NAME	FUNCTION
0	BTF Bad Track Flag	When set, this bit indicates that a defective track has been reallocated to an alternate track. The alternate head and cylinder address is recorded in the following data field.
1-15	-----	Not used. Always zero.

3.4 INTERLEAVING

The SPECTRA 126-PLUS interleaves sectors 3 to 1 in a standard configuration. For increased performance, the controller is also capable of interleaving 1 to 1 for contiguous sectors, or 2 to 1 provided that the total number of sectors per track is odd.

The following algorithms are used to calculate the format to be written on the disk.

3:1 Interleaving

Divide the total number of sectors per track (S) by 3.
If the remainder = 2, set i = S/3 + 1.
If the remainder = 1, set i = 2S/3 + 1.
If the remainder = 0, set i = 1.

The logical sector addresses after index are calculated as shown below, where h = logical head number and S = the number of sectors per track.

The first logical sector address = FSEC = (i-1) - h(i+1) modulo S.
The second logical sector address = FSEC + i modulo S.
The third logical sector address = FSEC + 2i modulo S.
The fourth logical sector address = FSEC + 3i modulo S.

If the number of sectors per track is exactly divisible by three and the remainder is zero, setting i = 1 causes the sectors to be contiguous instead of interleaved 3 to 1.

EXAMPLE

3 : 1 interleaving with 64 sectors per track:

64/3 = 21 remainder 1
i = 42 + 1 = 43
For head 0, FSEC = (43-1) -0(43+1) modulo 64 = 42
For head 1, FSEC = (43-1) -1(43+1) modulo 64 = 62

The logical sector addresses after index are:
For head 0: 42, 21, 0, 43, 22, 1, 45, 23, 2, etc.
For head 1: 62, 41, 20, 63, 42, 21, 0, 43, 22, 1, etc.

2 : 1 INTERLEAVING

Divide the total number of sectors per track (S) by 2.
If the remainder = 1, set i = S/2 + 1.
If the remainder = 0, set i = 1.

The logical sector addresses after index are calculated as shown below, where h = logical head number and S = the number of sectors per track.

The first logical sector address = FSEC = (i-1) - h(i+1) modulo S.
The second logical sector address = FSEC + i modulo S.
The third logical sector address = FSEC + 2i modulo S.

If the number of sectors per track is exactly divisible by two and the remainder is zero, setting i = 1 causes the sectors to be contiguous instead of interleaved 2 to 1.

EXAMPLE

2 : 1 interleaving with 61 sectors per track:

61/2 = 30 remainder 1
i = 30 + 1 = 31
For head 0, FSEC = (31-1) -0(31+1) modulo 61 = 30
For head 1, FSEC = (31-1) -1(31+1) modulo 61 = 59

The logical sector addresses after index are:
For head 0: 30, 0, 31, 1, 32, 2, 33, 3, 34, etc.
For head 1: 59, 29, 60, 30, 0, 31, 1, 32, 2, 33, etc.

1 : 1 INTERLEAVING

For 1 : 1 interleaving, set i = 1 and the same formulas apply.

EXAMPLE

1 : 1 interleaving with 64 sectors per track:

For head 0, FSEC = (1-1) - 0(1+1) modulo 64 = 0.
For head 1, FSEC = (1-1) - 1(1+1) modulo 64 = 62.

The logical sector addresses after index are:
For head 0: 0, 1, 2, 3, 4, 5, etc.
For head 1: 62, 63, 0, 1, 2, 3, etc.

The head skew seen here is necessary to allow the controller time to select a new head when a multiple sector transfer crosses a track boundary.

3.5 TAPE REGISTER DEFINITIONS

The control and status words described in this section are used to control tape operations and to report tape status. A summary of these words is shown below.

CONTROL WORD 0 TAPE TRANSPORT STATUS

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OFL	BOT	EOR	EOF	EOT	WRP	TR	CTO	TRW	TRW	TRW	TRW	RWM	RWM	RWM	RWM

CONTROL WORD 1 READ OVERFLOW STATUS COUNT

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC

CONTROL WORD 2 READ OVERFLOW STATUS COUNT

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	HES	HES	HES	HES	HES	HES	HES	HES

CONTROL WORD 3 READ OFFSET

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS

CONTROL WORD 4 CHARACTER COUNT

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CC	CC	CC	CC	CC	CC	CC	CC	CC	CC	CC	CC	CC	CC	CC	CC

CONTROL WORD 5 BUFFER ADDRESS

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA

CONTROL WORD 6 COMMAND AND TRANSPORT SELECT

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
US	US	US	US	CMC	CMC	CMC	CMC	WD	0	0	MBA	MBA	MBA	MBA	MBA

CONTROL WORD 7 TMTC STATUS AND CONTROL

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
IDL	OC	ERR	IE	LO	RSV	PE	AC	VRC	ECC	HE	MER	TE	TOE	FE	TER

CONTROL WORD 0 TAPE TRANSPORT STATUS

This word contains tape transport status.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OFL	BOT	EOR	EOF	EOT	WRP	TR	CTO	TRW	TRW	TRW	TRW	RWM	RWM	RWM	RWM

BIT	NAME	FUNCTION
0	OFL Offline	When set, this bit indicates that the selected drive is not ready and unavailable for any tape commands.
1	BOT Beginning Of Tape	When set, it indicates that the tape is positioned at the load point.
2	EOR End Of Record	This bit is set when an inter-record gap is encountered.
3	EOF End Of File	This bit is set when a file mark is read. Error and Tape Error are also set.
4	EOT End Of Tape	Set when the tape is positioned at or beyond the end of the tape reflective strip. Reset when the tape passes over the strip in reverse under program control
5	WP Write Protected	Set if the drive is write protected and status is read. Error and Tape Error are also set.
6	TR Tape Rewind	Set when the tape drive reaches End Of Tape and the drive proceeds to rewind.
7	CTO Command Time Out	Set if the controller fails to complete an operation before the command timer expires.
8-11	TRW Transport Rewinding	When the appropriate bit is set, it indicates that the corresponding tape drive is rewinding.
12-15	RWM Rewind Mask	When the appropriate bit is set, it enables a rewind complete interrupt for the corresponding tape drive.

CONTROL WORD 1 READ OVERFLOW STATUS COUNT

This word contains the read overflow count.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC

BIT	NAME	FUNCTION
0-15	ROC Read Overflow Count	These bits contain the lower 16 bits of the 24-bit read overflow count. Bit 0 is the most significant bit.

CONTROL WORD 2 READ OVERFLOW STATUS COUNT

This word contains the read overflow count.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	HES	HES	HES	HES	HES	HES	HES	HES

BIT	NAME	FUNCTION
0-7	ROC Read Overflow Count	These bits contain the upper 8 bits of the 24-bit read overflow count. Bit 7 is the least significant bit.
8-15	HES Hard Error Status	If the Extended Tape Status is enabled (9M-SW4 is ON), these bits contain the drive status when a hard error is detected.

CONTROL WORD 3 READ OFFSET

This word is used by the processor to specify the read offset.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS

BIT	NAME	FUNCTION
0-15	ROS Read Offset	These bits specify the number of characters to read before starting a data transfer to memory. They also contain control/status codes when in the Extended Command mode.

CONTROL WORD 4 CHARACTER COUNT

This word is used for read character count, write character count, skip record count, or erase length.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CC	CC	CC	CC	CC	CC	CC	CC	CC	CC	CC	CC	CC	CC	CC	CC

BIT	NAME	FUNCTION
0-15	CC Character Count	The function of these bits is determined by the command code in word 6, bits 7-4. The contents are decremented as each character is read. If an error occurs, these bits contain the remaining number of bytes not read. During a Write operation, these bits determine the number of bytes not written. A SKIP RECORD COUNT command decrements the count for each record skipped, and an ERASE LENGTH command specifies the length of tape that is to be erased.

CONTROL WORD 5 BUFFER ADDRESS

This word contains the 15 least significant bits of the 20-bit TILINE memory buffer starting address.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA

BIT	NAME	FUNCTION
0-15	MBA Memory Buffer Address	Bits 14-0 are the 15 least significant bits of the 20-bit TILINE starting memory address. The 5 most significant bits are contained in word 6. Bit 15 is always zero.

CONTROL WORD 6 COMMAND AND TRANSPORT SELECT

This word contains command codes and selects one of four possible tape transport units.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
US	US	US	US	CMC	CMC	CMC	CMC	WD	0	0	MBA	MBA	MBA	MBA	MBA

BIT	NAME	FUNCTION
0-3	US Unit Select	These bits select one of the four possible logical tape units. If a command is issued without a unit select bit set, the tape interface will be reset and the command will terminate with "Command Timeout".
4-7	CMC Command Codes	These bits select the operation to be performed. The command codes are defined in table 3-2.
8	WD Write Diagnostic	When set, this bit forces a parity error on a Write. This causes the drive to pulse the Hard Error signal on the tape interface.
9-10	-----	These bits are reserved for diagnostics. Always zero.
11-15	MBA Memory Buffer Address	Bits 15-11 are the 5 most significant bits of the 20-bit TILINE starting memory address.

TABLE 3-2 COMMAND CODES

BIT 4	BIT 5	BIT 6	BIT 7	COMMAND
0	0	0	0	NOP
0	0	0	1	WRITE SYNC
0	0	1	0	WRITE EOF
0	0	1	1	RECORD SKIP REVERSE
0	1	0	0	READ BINARY
0	1	0	1	RECORD SKIP FORWARD
0	1	1	0	WRITE BINARY
0	1	1	1	ERASE
1	0	0	0	READ STATUS
1	0	0	1	READ STATUS
1	0	1	0	REWIND
1	0	1	1	REWIND AND UNLOAD
1	1	0	0	NOP
1	1	0	1	NOP
1	1	1	0	NOP
1	1	1	1	EXTENDED CONTROL/STATUS

CONTROL WORD 7 TMTC STATUS AND CONTROL

This word contains control bits from the processor and status information from the tape controller.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
IDL	OC	ERR	IE	LO	RSV	PE	AC	VRC	ECC	HE	MER	TE	TOE	FE	TER

BIT	NAME	FUNCTION
0	IDL Idle	When set, the controller is not busy. If a command is used when Idle is 0, the controller ignores the command.
1	OC Operation Complete	Set at the error-free completion of an operation.
2	ERR Error	Set when an operation is terminated due to error.
3	IE Interrupt Enable	When set, this bit enables the controller to generate an interrupt when Operation Complete or Error is set.
4	LO Lock Out	This bit is set when control word 7 is read.
5	-----	Reserved for diagnostics. Always zero.
6	PE PE Format	Set if the transport is in PE format (1600 bpi).
7	AC Abnormal Completion	This bit is set if a tape operation is terminated due to an I/O reset or power fail warning.

CONTROL WORD 7 TMTC STATUS AND CONTROL [continued]

BIT	NAME	FUNCTION
8	VRC Vertical Redundancy Check	This bit is set if the controller detected a Read Data Parity error.
9	ECC Error Correction Enabled	The setting of this bit is determined by the type of transport selected. For an NRZI transport, this bit is a longitudinal Redundancy Check (LRC) error indicator. For a PE format, this bit indicates that ECC is enabled and a single bit correction has been performed.
10	HE Hard Error	This bit is a CRC error indicator for an NRZI drive. For a PE drive, this bit is set if one of the following errors is detected during a Read Binary Forward operation: No PE mark, Multitrack dropout error, False postamble error, or a Skew error. See the table below.
11	MER Memory Error	Set if a memory Read error is detected during a data transfer operation. ERR is also set.
12	TE TILINE Timing Error	When set indicates that a timing error has occurred because the TILINE could not keep up with the controller during a data transfer operation.
13	TOE TILINE Time-out Error	Set if a transfer cycle is not completed in 10 microseconds after the controller gains TILINE access. May occur when attempting to access non-existent memory.
14	FE Format Error	Not used. Always zero. (NRZI format).
15	TER Tape Error	This bit is set if a transport error has occurred.

HARD ERROR INFORMATION

The controller will report two types of Hard Error Status. One error may be retried, and the other is unrecoverable. The unrecoverable error results when the tape drive has exhausted its retry capability and has failed to correct an error. The transport indicates this condition by latching the Hard Error signal (IHER) on the interface. The controller will check IHER in the On-Line status check prior to command start up. If the signal is active, the controller will set TILINE Hard Error (Word 7, bit 10) and Off-Line status (Word 0, bit 0). The controller will also check for this signal after command completion. If the Hard Error status is true, an Off-line status will also be issued.

HARD ERROR INFORMATION [continued]

The retryable Hard Error is returned to the controller as a pulsed condition prior to command completion; however, the Off-line bit is not set as with the unrecoverable error. If a Hard Error of either type is detectedand the Extended Tape Status is enabled (9M, SW4 is ON), then the controller returns three bytes of transport status to the TILINE interface via Control Word 3 and the lower half of Control Word 2 each time a hard error occurs. The status reported from the transport consists of ERROR CLASSIFICATION, OPERATING DENSITY, TRACK IN ERROR, and READ/WRITE RETRY COUNT information. Status is returned to the TPCS interface as shown below.

NOTE: The extended status functions only with Cipher Cache Tapes.

TPCS REGISTER 2

BIT	NAME	FUNCTION
8-10	DENSITY	These bits determine the density as follows: 000 = 800 001 = 1600 010 = 3200 011 = 6250
11	WRITE OVERRUN	When set, this bit indicates that there was an over-run when writing from tape to cache.
12	READ OVERRUN	When set, this bit indicates that there was an over-run when reading from tape to cache.
13-15	CACHE BLOCK SIZE	These bits determine the auto-expanded cache size as follows: 000 = 9K 010 = 24K 100 = 64K 001 = 16K 011 = 32K

TPCS REGISTER 3

BIT	NAME	FUNCTION
0	TRACK ERROR 0	When set, this bit indicates that track 0 is in error.
1	TRACK ERROR 1	When set, this bit indicates that track 1 is in error.
2	TRACK ERROR 2	When set, this bit indicates that track 2 is in error.
3	TRACK ERROR 3	When set, this bit indicates that track 3 is in error.
4	TRACK ERROR 4	When set, this bit indicates that track 4 is in error.
5	TRACK ERROR 5	When set, this bit indicates that track 5 is in error.
6	TRACK ERROR 6	When set, this bit indicates that track 6 is in error.
7	TRACK ERROR 7	When set, this bit indicates that track 7 is in error.
8-14	RETRY COUNT	These bits comprise a count of the number of retries that have occurred on the current host record. Bit 8 is the most significant bit; bit 14 is the least significant bit.
15	TRACK PARITY	When set, this bit indicates that there is a track parity in error.

3.5.1 COMMAND DESCRIPTIONS

The command code which selects the operation to be performed by the controller is formed by bits 4-7 of Control Word 6. The command code assignments are shown in the description of Word 6, and the tape commands are described below.

NO OPERATION COMMAND

When a NO OPERATION (NOP) command is issued, the controller responds by setting Idle and Operation Complete status (Control Word 7, bits 0 and 1).

WRITE SYNC

The WRITE SYNC command ensures that all pending Write operations are completed. After this command is issued, the controller remains busy (IDLE set to 0) until the entire contents of the buffers (controller and drive) are written on tape. (Applicable only to cache tapes).

WRITE END-OF-FILE

The WRITE END-OF-FILE command causes a file mark to be written on the tape. The controller checks the EOF mark after writing it on the tape. An error will be reported as a VRC error (Control Word 7, bit 8) by an NRZI tape drive, or as a PE hard error (Control Word 7, bit 10) by a PE tape drive.

RECORD SKIP REVERSE

The RECORD SKIP REVERSE command causes the tape to pass over the heads in the reverse direction without transferring data to memory. The number of records to be skipped is specified in Control Word 4, and the contents of that Word are decremented each time a record is skipped.

READ BINARY FORWARD

The READ BINARY FORWARD command reads data from tape and transfers it to main memory. The controller acquires control of the TILINE, assembles the tape characters into 16-bit words, and transmits the words into successive memory locations.

SKIP RECORD FORWARD

The SKIP RECORD FORWARD command causes the tape to skip over records without transferring any data to memory. The number of records to be skipped is loaded into Control Word 4, which is decremented each time a record is skipped. If the initial record number is zero, the controller attempts to skip 65,536 records and stops on EOT or EOF.

WRITE BINARY FORWARD

The WRITE BINARY FORWARD command reads data from main memory via the TILINE and records it on tape. The 20-bit starting address of the memory buffer is specified in Control Word 6 (bits 11-15) and Control Word 5 (bits 0-14). The number of 8-bit characters to be recorded is specified in Control Word 4.

ERASE

The ERASE command erases a measured length of tape. Control Word 4 is loaded with the value "K" from which the length (L) is determined as follows:

NRZI transport: L (inches)=0.666 + K(0.00125). Maximum length = 81.92 inches.

PE transport: L (inches)=0.666 + K(0.000625). Maximum length = 42.6 inches.

READ STATUS

The READ STATUS command selects a transport and returns transport status information without performing any transport functions. The controller responds to the command by returning a transport status word (Control Word 0) and a controller status word (Control Word 7).

REWIND

The REWIND command checks the selected transport to see if it is already rewinding. If it is not rewinding, the controller commands the transport to rewind, and reports Idle and Operation Complete in Control Word 7. If the selected transport is already rewinding, the controller reports Idle, Error and Tape Error (Control Word 7, bits 0, 2, and 15), and the tape rewinding status (Control Word 0, bit 6).

REWIND AND UNLOAD

The REWIND AND UNLOAD command causes the tape to rewind and unload from the transport. It also causes the Offline bit to be set.

3.5.2 EXTENDED COMMANDS

The Extended Commands initiate self-test routines, read the controller PROM revision, obtain status from the drive, and issue commands to the drive. To operate in the Extended Command mode for either control or status, enter an F (hexadecimal) in the command block of Control Word 6. Then enter the appropriate command code in Control Word 3, bits 0-7. The following table shows the codes that must be placed in Control Word 3 for Extended Control .

EXTENDED COMMANDS (CONTROL)

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7	COMMAND
0	1	1	1	1	1	0	0	REPORT PROM REVISION LEVEL
0	0	0	0	0	0	0	0	EXECUTE SELF-TEST
1	0	0	0	0	0	0	0	LOOP ON SELF-TEST
0	0	1	0	0	0	0	0	READ FORWARD
0	0	1	1	0	0	0	0	READ REVERSE
0	0	1	1	0	0	1	0	READ REVERSE EDIT
0	0	1	0	1	0	0	0	WRITE *
0	0	1	0	1	0	1	0	WRITE EDIT *
0	0	1	0	1	1	0	0	WRITE FILE MARK
0	0	1	0	1	0	0	1	ERASE VARIABLE LENGTH
0	0	1	0	1	1	0	1	ERASE FIXED LENGTH
0	0	1	0	1	1	1	1	SECURITY ERASE
0	0	1	0	0	0	0	1	SPACE FORWARD
0	0	1	1	0	0	0	1	SPACE REVERSE
0	0	1	0	0	1	0	0	FILE SEARCH FORWARD
0	0	1	0	0	1	0	1	FILE SEARCH FORWARD **
0	0	1	1	0	1	0	0	FILE SEARCH REVERSE
0	0	1	1	0	1	0	1	FILE SEARCH REVERSE **
0	0	1	0	0	0	1	1	WRITE SYNC
0	0	1	1	0	1	1	1	3200 BPI
0	0	1	0	0	1	1	1	1600 BPI (PE)

* This command results in a TILINE Timing Error because data transfer to the drive is not supported in this mode.

** Ignore data with this command.

Extended Control

The controller self-test may be called from the extended command field by entering 0000 (hexadecimal) in Control Word 3. A loop bit (bit 0) is provided to allow for scope loops on self-test by entering 8000 (hexadecimal) in Control Word 3. An I/O RESET must be issued to exit this loop. Control Word 7 must always be the last Word issued to the controller.

The controller PROM revision level is reported in the least significant byte of Control Word 3 when 7C (hexadecimal) is entered in the most significant byte.

After the controller issues a command code from Control Word 3 to the drive, the controller enters the read transfer mode and transfers the number of bytes specified to the TILINE memory. If a WRITE command is issued, a TILINE Timing Error status will occur. The controller terminates with normal completion status for those commands which do not result in a read (IRSTR) or write (IWSTR) strobe.

Extended Status

Certain tape drives (such as the Cipher CacheTape) will present detailed status information when commanded. Obtaining status from the drive requires two commands for each block of status to be transferred. First, the READ EXTENDED STATUS command must be issued to Control Word 3 followed by the desired status command. The desired status command must also include a Read Character Count (up to 16 bytes) in Control Word 4, and a TILINE Memory Address in Control Word 5. The following table shows the extended status codes that must be placed in Control Word 3. This table is followed by a bit by bit description of the resulting status blocks as they would appear in memory.

EXTENDED COMMANDS (STATUS)

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7	COMMAND
0	0	1	0	0	0	1	0	READ EXTENDED STATUS
0	0	1	0	0	0	0	0	CURRENT STATUS
0	0	1	1	0	0	0	0	CONFIGURATION STATUS
0	0	1	0	0	0	1	0	ERROR HISTORY STATUS
0	0	1	1	0	0	1	0	MACHINE STATUS
0	0	1	1	0	0	1	1	ERROR HISTORY RESET

CURRENT STATUS BLOCK (BYTE 0)

BIT	NAME	FUNCTION
0	IDENT	This is the least significant bit. When set, this bit indicates that IDENT is active.
1	IHER	When set, this bit indicates that IHER is active.
2	ICER	When set, this bit indicates that ICER is active.
3	IFMK	When set, this bit indicates that IFMK is active.
4	IRDY	When set, this bit indicates that IDRY is active.
5	IONL	When set, this bit indicates that IONL is active.
6	IRWD	When set, this bit indicates that IRWD is active.
7	IFPT	When set, this bit indicates that IFPT is active.

CURRENT STATUS BLOCK (BYTE 1)

BIT	NAME	FUNCTION
0	ILDP	When set, this bit indicates that ILDP is active.(LSB)
1	IEOT	When set, this bit indicates that IEOT is active.
2	RETRIES	When set, this bit indicates that the Read retries were exceeded.
3	PARITY ERROR	When set, this bit indicates that a Write Parity Error was encountered at the interface.
4	WRITE HARD ERROR	When set, this bit indicates a Hard Error.
5	ILLEGAL COMMAND	When set, this bit indicates that an illegal command was issued.
6-7	-----	Not used.

CURRENT STATUS BLOCK (BYTE 2)

BIT	NAME	FUNCTION
0-2	CACHE BLOCK SIZE	These bits determine the auto-expanded cache size as follows: 000 = 9K 010 = 24K 001 = 16K 011 = 32K 100 = 64K Bit 0 is the least significant bit.
3	READ OVERRUN	When set, this bit indicates that there was an overrun when reading from tape to cache.
4	WRITE OVERRUN	When set, this bit indicates that there was an overrun when writing from host to cache.
5-7	-----	Not used.

CURRENT STATUS BLOCK (BYTE 3)

BIT	NAME	FUNCTION
0	TRACK ERROR 7	This is the least significant bit. When set, this bit indicates that track 7 is in error.
1	TRACK ERROR 6	When set, this bit indicates that track 6 is in error.
2	TRACK ERROR 5	When set, this bit indicates that track 5 is in error.
3	TRACK ERROR 4	When set, this bit indicates that track 4 is in error.
4	TRACK ERROR 3	When set, this bit indicates that track 3 is in error.
5	TRACK ERROR 2	When set, this bit indicates that track 2 is in error.
6	TRACK ERROR 1	When set, this bit indicates that track 1 is in error.
7	TRACK ERROR 0	When set, this bit indicates that track 0 is in error.

CURRENT STATUS BLOCK (BYTE 4)

BIT	NAME	FUNCTION
0	PARITY ERROR	When set, this bit indicates that the parity track is in error. This is the least significant bit.
1-7	RETRY COUNT	When set, these bits specify the Read/Write retry count on the current host record. Bit 1 is the least significant bit; bit 7 is the most significant bit.

CURRENT STATUS BLOCK (BYTE 5)

BIT	NAME	FUNCTION
0-4	PANEL ERROR	When set, these bits specify the front panel error code. Bit 0 is the least significant bit; bit 4 is the most significant bit.

CURRENT STATUS BLOCK (BYTE 6)

BIT	NAME	FUNCTION
0-2	DENSITY	Bit 0 is the least significant bit. These bits determine the operating density as follows: 000 = 800 001 = 1600 010 = 3200 011 = 6250
3-5	DENSITY	These bits determine the requested density as follows: 000 = 800 010 = 3200 001 = 1600 011 = 6250
6	READ DENSITY CONFLICT	When set, this bit indicates that there was a Read density conflict.
7	WRITE DENSITY CONFLICT	When set, this bit indicates that there was a Write density conflict.

CURRENT STATUS BLOCK (BYTE 7)

BIT	NAME	FUNCTION
0-7	UNFIXED BLOCK COUNT	When set, these bits indicate that there are block detachable structures remaining in cache (includes file marks). Bit 0 is the least significant bit.

CURRENT STATUS BLOCK (BYTE 8)

BIT	NAME	FUNCTION
0-7	LOW ORDER BYTE	These bits indicate the low order byte of the fixed block count from BOT (includes file marks). Bit 0 is the least significant bit.

CURRENT STATUS BLOCK (BYTE 9)

BIT	NAME	FUNCTION
0-7	MID ORDER BYTE	These bits indicate the mid order byte of the fixed block count from BOT (includes file marks). Bit 0 is the least significant bit.

CURRENT STATUS BLOCK (BYTE 10)

BIT	NAME	FUNCTION
0-7	HIGH ORDER BYTE	These bits indicate the high order byte of the fixed block count from BOT (includes file marks). Bit 0 is the least significant bit.

CURRENT STATUS BLOCK (BYTE 11)

BIT	NAME	FUNCTION
0-7	LOW ORDER BYTE	These bits indicate the low order byte of the sequence number of the record in hard error. Bit 0 = LSB

CURRENT STATUS BLOCK (BYTE 12)

BIT	NAME	FUNCTION
0-7	MID ORDER BYTE	These bits indicate the mid order byte of the sequence number of the record in hard error. Bit 0 = LSB

CURRENT STATUS BLOCK (BYTE 13)

BIT	NAME	FUNCTION
0-7	HIGH ORDER BYTE	These bits indicate the high order byte of the sequence number of the record in hard error. Bit 0=LSB

CONFIGURATION STATUS BLOCK (BYTE 0)

BIT	NAME	FUNCTION
0	800 BPI	When set, this bit indicates that the tape drive has 800 bpi capability. This is the least significant bit.
1	1600 BPI	When set, this bit indicates that the tape drive has 1600 bpi capability.
2	3200 BPI	When set, this bit indicates that the tape drive has 3200 bpi capability.
3	6250 BPI	When set, this bit indicates that the tape drive has 6250 bpi capability.
4	OTHER BPI	When set, this bit indicates that the tape drive has some other bpi capability.

CONFIGURATION STATUS BLOCK (BYTE 1)

BIT	NAME	FUNCTION
0-7	VENDOR CODE	This byte indicates the manufacturer of the drive. Bit 0 = LSB.

CONFIGURATION STATUS BLOCK (BYTE 2)

BIT	NAME	FUNCTION
0-2	MODEL CODE	These bits determine the model code as follows: 000 = other 011 = M891-I 110 = M990-II 001 = M890-I 100 = M891-II 111 = M991-HPGGR 010 = M890-II 101 = M990-I
3-7	-----	Not used. Always zero.

CONFIGURATION STATUS BLOCK (BYTE 3)

BIT	NAME	FUNCTION
0	EOT LOCATION	This bit determines the EOT location as follows: 1 = EOT search 0 = STD Bit 0 = LSB
1	PARITY	This bit determines the parity as follows: 1 = external 0 = internal
2-3	MAXIMUM BLOCK SIZE	These bits determine the maximum block size: 00 = 9K 10 = 24K 01 = 16K 11 = 32K
4	RAMPS	This bit determines the ramps as follows: 1 = disabled 0 = enabled
5-7	SPEED SETTING	These bits indicate the value of the simulated speed setting. Bit 5 is the least significant bit; bit 7 is the most significant bit.

CONFIGURATION STATUS BLOCK (BYTE 4)

BIT	NAME	FUNCTION
0-2	-----	Not used. Always zero. Bit 0 = LSB.
3	POST EOT	When set, this bit indicates Post-EOT streaming is enabled.
4	IDENT	When set, this bit indicates that IDENT will be asserted at BOT when at 3200 bpi.
5-7	-----	Not used. Always zero.

ERROR HISTORY BLOCK (BYTE 0)

BIT	NAME	FUNCTION
0-7	READ RETRY COUNT	These bits contain the Read Retry Count subsequent to unloading the tape (255 maximum). Bit 0 = LSB.

ERROR HISTORY BLOCK (BYTE 1)

BIT	NAME	FUNCTION
0-7	WRITE RETRY COUNT	These bits contain the Write Retry Count subsequent to unloading the tape (255 maximum). Bit 0 = LSB.

ERROR HISTORY BLOCK (BYTE 2)

BIT	NAME	FUNCTION
0-7	TRACK 0	These bits contain the error counts for track 0 (255 maximum). Bit 0 = LSB.

ERROR HISTORY BLOCK (BYTE 3)

BIT	NAME	FUNCTION
0-7	TRACK 1	These bits contain the error counts for track 1 (255 maximum). Bit 0 = LSB.

ERROR HISTORY BLOCK (BYTE 4)

BIT	NAME	FUNCTION
0-7	TRACK 2	These bits contain the error counts for track 2 (255 maximum). Bit 0 = LSB.

ERROR HISTORY BLOCK (BYTE 5)

BIT	NAME	FUNCTION
0-7	TRACK 3	These bits contain the error counts for track 3 (255 maximum). Bit 0 = LSB.

ERROR HISTORY BLOCK (BYTE 6)

BIT	NAME	FUNCTION
0-7	TRACK 4	These bits contain the error counts for track 4 (255 maximum). Bit 0 = LSB.

ERROR HISTORY BLOCK (BYTE 7)

BIT	NAME	FUNCTION
0-7	TRACK 5	These bits contain the error counts for track 5 (255 maximum). Bit 0 = LSB.

ERROR HISTORY BLOCK (BYTE 8)

BIT	NAME	FUNCTION
0-7	TRACK 6	These bits contain the error counts for track 6 (255 maximum). Bit 0 = LSB.

ERROR HISTORY BLOCK (BYTE 9)

BIT	NAME	FUNCTION
0-7	TRACK 7	These bits contain the error counts for track 7 (255 maximum). Bit 0 = LSB.

ERROR HISTORY BLOCK (BYTE 10)

BIT	NAME	FUNCTION
0-7	TRACK P	These bits contain the error counts for track P (255 maximum). Bit 0 = LSB.

MACHINE STATUS BLOCK (BYTE 0)

BIT	NAME	FUNCTION
0-7	LOW ORDER	These bits contain the low order byte of the tach count for the head position (in multiples of 1.28").

MACHINE STATUS BLOCK (BYTE 1)

BIT	NAME	FUNCTION
0-7	HIGH ORDER	These bits contain the high order byte of the tach count for the head position (in multiples of 1.28").

MACHINE STATUS BLOCK (BYTE 2)

BIT	NAME	FUNCTION
0-7	PREVIOUS HOST COMMAND	These bits contain the previous host command.

MACHINE STATUS BLOCK (BYTE 3)

BIT	NAME	FUNCTION
0-7	2nd PREVIOUS HOST COMMAND	These bits contain the second previous host command.

MACHINE STATUS BLOCK (BYTE 4)

BIT	NAME	FUNCTION
0-7	3rd PREVIOUS HOST COMMAND	These bits contain the third previous host command.

MACHINE STATUS BLOCK (BYTE 5)

BIT	NAME	FUNCTION
0-7	4th PREVIOUS HOST COMMAND	These bits contain the fourth previous host command.

MACHINE STATUS BLOCK (BYTE 6)

BIT	NAME	FUNCTION
0-7	5th PREVIOUS HOST COMMAND	These bits contain the fifth previous host command.

MACHINE STATUS BLOCK (BYTE 7)

BIT	NAME	FUNCTION
0-1	REEL SIZE	These bits determine the reel size as follows: 00 = Unknown 01 = 7 inch 10 = 8 1/2 11 = 10 1/2"
2	DOOR LOCK STATUS	This bit determines the door lock status as follows: 0 = Unlocked 1 = locked

Chapter Four

Diagnostics

4.1 DISK DIAGNOSTIC PROGRAMS

This chapter explains the diagnostic programs that may be used to check out the disk subsystem when connecting the SPECTRA 126-PLUS controller to a particular drive. The three disk diagnostics supplied by TI are:

DSKSA	SURFACE ANALYSIS TEST
DSKCD1	CDD CONTROLLER/DISK DIAG PART 1
DSKCD2	CDD CONTROLLER/DISK DIAG PART 2
DSKCOM	COMMON CONTROLLER/DISK

NOTE: The above diagnostics must include WD900 disk types for WD900 emulation.

The first program that should be run is DSKSA to format the whole disk. Use the verb FD to format the system part of the disk, and the verb FC to format the diagnostic cylinders. The two other diagnostics may be run in any order. Depending upon the disk type chosen and the drive attached, the diagnostics may need to be patched. If the **DS80** disk type is chosen, **10** alternate tracks are used. If the **WD900** disk type is chosen, **16** alternate tracks are used.

If the selected drive is not compatible with the selected disk type, three locations must be patched using the following procedure:

After loading the diagnostic and answering the "IT" questions, run the subsequent list of verbs.

-Reference appropriate notes on following pages.

(The drive used in the following example is a Fujitsu 2351).

```
VERB?   SR  <CR>
STORE REGISTERS
*** ERROR 001B  DSKSA XR
STORE REGISTER VALUES DIDN'T AGREE WITH THE DISK TYPE ENTERED DURING "IT".
EXPECTED VALUES FOR A DS80
WORD 1=1E80     WORD 2=3D00      WORD 3=2B35
RECEIVED VALUES FOR AN UNDEFINED DISK TYPE
WORD 1=2C00     WORD 2=5800      WORD 3=533E
```

(Note 1)

```
VERB?  .MS   <CR>
COND (EQ NE GT LT DEF=EQ)  EQ  <CR>
ADDRESS (000000)  6000  <CR>                                  (Note 2)
# OF WORDS (DEF-0000)  9000   <CR>  DATA (DEF=0000)  1E80 <CR>
0072BC= 1E80 (Note 3)
```

```
VERB?  .MM  <CR>
ADDRESS (000000)  0072B6  <CR>
0072E6 - 1E80 -  2C00  <CR>
0072E8 - 3D00 -  5800  <CR>
0072EA - 2B35 -  533E  <CR>
0072EC - 3200 - <CMD>
VERB?_____  (Patching is complete)
```

Note 1: Verify that the "received values for undefined disk type" are the values required for selected disk drive. (See Disk Drive Configuration Store Register Tables, section 2.3.3).

Note 2: If word 1 is a 2000 value, use word 3 to do the memory search. Be sure to subtract two word counts when running .MM.

Note 3: Address values will be different with each rev level and each diagnostic used.

4.2 DIAGNOSTIC TESTING ERRORS

Certain errors may be encountered; these errors are shown as follows.

DSKCD1 TEST 33 - Quick Disk Test	Fails due to format differences when testing the fixed portion of a CMD or DFR with switch 5 of 9M off.
DSKCD1 TEST 41 - Command Verification	Fails due to format differences when testing the fixed portion of a CMD or DFR with switch 5 of 9M off or fails on higher transfer rate drives due to Data Field Verify Error.
DSKCD1 TEST 56 - Rate Error Test	Fails because the buffer presents this error from occurring.
DSKCD1 TEST 57 - Command Time Out Test	Fails on higher transfer rate drives due to timing differences.
DSKCD1 TEST 58 - Search Error Test	Fails due to format differences if sectors are not interleaved 3 to 1.
DSKCD2 TEST 21 - Interlace Timing Test	May fail if the motor RPM is not 3600, if a burst count other than 1 has been selected, or if contiguous sectors are being used, or a higher transfer rate drive is used.
DSKCD2 TEST 22 - Motor RPM Test	May fail if the motor RPM is not 3600.
DSKCD2 TEST 31 - Interactive Test	Fails when switching the drive on-line when the program expects to see the unsafe bit set.
DSKCOM TEST 23 - Jitter Address Test	Fails due to format differences when testing the fixed portion of a CMD or DFR with switch 5 of 9M off.
DSKCOM TEST 24 - Random Read Test	Fails due to format differences when testing the fixed portion of a CMD or DFR with switch 5 of 9M off.
DSKCOM TEST 62 - Drive Exerciser	Fails due to format differences when testing the fixed portion of a CMD or DFR with switch 5 of 9M off.

4.2.1 MAG TAPE ERRORS

The TI diagnostic "TAPTST" may be run on the SPECTRA 126-PLUS. The current version supporting the 979/080A, MT1600 and MT3200 tape test is revision 333/84H or later. This would fully support the MT3200 tape drives (Cipher Cache Tape) when the extended status switch 9M SW4 is enabled.When not running a cache tape drive or if MR3200 diagnostic support is not available, the extended status switch must be disabled and the drive tested as a 979 type drive. When running this type drive, some diagnostic failures must be expected due to the different characteristics of the tape drive being used and the TI 979 tape drive. The following table gives a list of some expected failures when running "TAPTST".

TEST	FAILURE
A,B	Fails because the diagnostic expects a VRC error after a diagnostic write. The controller will force a bad parity on a diagnostic write, but will only report Hard Error.
C	Fails on some NRZ tranports due to different ramp times.
7 & 8	Fails because of a 2 bit overflow when running 800 BPT tape density. (Extra 2 read pulses).
10	Fails forward creep test on some transports due to different transport characteristics.
15	Fails the rewind and unload test on transports which do not go off line until after they have rewound to BOT.

4.3 MICRODIAGNOSTICS

Microdiagnostics are run each time the controller powers up. There are three LEDs on the SPECTRA 126-PLUS that show the status of the controller. The red LED indicates that the microdiagnostics have failed on power up. The two green LEDs indicate that both the disk and tape portions of the controller are idle.

The following table gives a list of possible combinations of these lights after power up.

GREEN LED (MT)	GREEN LED (DK)	RED LED (DG BAD)	MEANING
ON	ON	OFF	Microdiagnostics Successful.
OFF	ON	OFF	Disk portion of microdiagnostics successful. Ensure that W5 is installed.
OFF	OFF	OFF	LED failure.
OFF	OFF	ON	Microdiagnostics failure.
OFF	ON	ON	Microdiagnostics failure.
ON	ON	ON	LED failure.
ON	OFF	ON	LED failure.
ON	OFF	OFF	LED failure.

For further information concerning microdiagnostic failure, examine the contents of Disk Control Words 2 and 4. Words 2 and 4 have the following meanings.

WORD 2	WORD 4	MEANING
0000	0000	Diagnostics successful.
00XX	0000	Self-test command successful.
XX1X	XXXX	CSRC or CDEST bus failed.
F121	XXXX	CPU processor ALU failed logical test.
F222	XXXX	CPU processor ALU failed arithmetic test.
F323	XXXX	CPU processor ALU failed shift test.
F333	XXXX	CPU processor failed register address test.
F434	XXXX	CPU processor count failed.
F242	XXXX	CPU processor failed sector buffer pattern test.
F141	XXXX	CPU processor failed JSR/RTS test.
F343	XXXX	CPU processor INH CLK signal failed.
F444	XXXX	CPU processor MDAC signal failed.
F151	XXXX	CPU processor TIGO signal failed.
F353	XXXX	CPU processor WRN signal failed.
F454	XXXX	CPU processor NMTO signal failed.
F555	XXXX	CPU processor NMPE signal failed.
F181	XXXX	CPU processor/MT sequencer handshake failed.
F282	XXXX	MT FIFO full/empty not properly detected.
F383	XXXX	MT FIFO data failed.
F484	XXXX	MT data late or parity error detection failed.
F585	XXXX	MT timer test failed.
FF14	XXXX	CPU processor/Disk processor handshake failed.
FF15	XXXX	CPU processor INH CLK signal failed.
0000	1XXX	DSRC or DDEST bus failed.
0000	XX1X	DSRC or DDEST bus failed.
0000	2121	Disk processor ALU failed logical test.
0000	2222	Disk processor ALU failed arithmetic test.
0000	2323	Disk processor ALU failed shift test.
0000	3333	Disk processor ALU failed register address test.
0000	4141	Disk processor failed JSR/RTS test.
0000	4242	Disk processor failed serializer/deserializer data test.
0000	4343	Disk processor detected word available signal early.
0000	4444	Disk processor did not detect a word available signal.
0000	4545	Disk processor failed sync word detection test.
0000	5151	Disk processor ECC test failed.
0000	5252	Disk processor ECC error not detected.
0000	5353	Disk processor ECC error could not be reset.
0000	5454	Disk processor did not detect a word available signal.
0000	6161	Disk processor failed sector buffer upper byte test.
0000	6262	Disk processor failed sector buffer lower byte test.
0000	AAAA	Disk processor did not set ATTN at the end of its microdiagnostics.

RETURN INFORMATION REFERENCE SHEET

cipher data products, inc.

Systems Interface Business Group

Spectra Logic Products

297 NORTH BERNARDO AVE.
P.O. BOX 7260
MOUNTAIN VIEW, CA.
94039-7260
(415)964-2211

IMPORTANT: This form should be completed ONLY AFTER RETURN SHIPMENT HAS BEEN PRE-AUTHORIZED BY SPECTRA LOGIC. Contact Customer Support Department for further information.

MODEL# _____
SERIAL# _____

COMPANY NAME: _____
CONTACT NAME: _____
PHONE#( ) _____
DATE _____ CRO# _____

REASON FOR RETURN:
CREDIT
MARKETING DEMO _____
UPDATED ONLY _____
REPAIR _____

IN WARRANTY _____
OUT OF WARRANTY _____

THE REMAINDER OF THIS FORM SHOULD BE COMPLETED ONLY IF REPAIR IS NEEDED.

Did the Controller Work Previously? _____ Or was it DOA? _____

CPU TYPE _____
OPERATING SYSTEM & REV. _____
DISK DRIVE MODEL(S) _____
TAPE DRIVE MODEL(S) _____

Other comments on System Configuration (i.e.-mapping?) _____

Did the board fail during diagnostics? _____
microdiagnostics? _____
or operating system? _____

If diagnostic was run, give diagnostic name and detailed error message, and/or attach hard copy. _____

Other Comments _____

P/N 8600023