DEPOT MAINTENANCE MANUAL

Model 990/4 Computer System

Part No. 945403-9701
15 May 1977

TEXAS INSTRUMENTS

LIST OF EFFECTIVE PAGES

INSERT LATEST CHANGED PAGES DESTROY SUPERSEDED PAGES

Note: The portion of the text affected by the changes is indicated by a vertical bar in the outer margins of the page.

Model 990/4 Computer System Depot Maintenance Manual (945403-9701)

Original Issue . . . . . 1 July 1976
Change 1 . . . . . 15 May 1977 (ECN 419781)

Total number of pages in this publication is 226 consisting of the following:

PAGE NO.	CHANGE NO.	PAGE NO.	CHANGE NO.	PAGE NO.	CHANGE NO.
Cover	1	8-15	1		
Effective Pages	1	8-16	0		
iii - x	0	8-17 - 8-18	1		
1-1 - 1-3	0	8-19 - 8-22	0		
1-4	1	9-1 - 9-5	0		
1-5 - 1-18	0	9-6 - 9-8	1		
2-1 - 2-8	0	10-1 - 10-10	0		
3-1 - 3-6	0	11-1 - 11-8	0		
4-1 - 4-12	0	12-1 - 12-8	0		
5-1 - 5-12	0	13-1 - 13-30	0		
6-1 - 6-12	0	Appendix A Div	0		
7-1 - 7-9	0	A-1 - A-6	0		
7-10	1	Appendix B Div	0		
7-11 - 7-14	0	B-1 - B-8	0		
7-15	1	Alphabetical Index Div	0		
7-16 - 7-19	0	Index-1 - Index-4	0		
7-20	1	User's Response	1		
7-21 - 7-28	0	Business Reply	0		
7-29 - 7-32	1	Cover Blank	0		
7-33 - 7-36	0	Cover	0		
8-1 - 8-14	0				

PREFACE

This manual contains depot-level maintenance information required to troubleshoot and repair all assemblies and subassemblies of the 990/4 Microcomputer System with exception of the peripheral channels which are documented in their respective depot level manuals. This manual should be used in conjunction with the 990/4 Hardware Reference Manual (detailed theory of operation), 990/4 Field Maintenance Manual (system-level troubleshooting information), and the 990/4 Maintenance Drawing Manual (contains logic diagrams, IC data sheets, assembly drawings and list of materials for all assemblies and subassemblies of the 990/4 system).

MANUAL ORGANIZATION

This manual is organized into 13 sections and two appendixes including:

I – General Description
Provides a general description of the 990/4 Microcomputer System and briefly describes the various options available for the system.

II – Test Bench Setup
Describes the troubleshooting and repair workstations and the recommended tools, test equipment and materials required to perform depot-level maintenance.

III – Assembly and Disassembly
Provides assembly and disassembly procedures for all major subassemblies of a 990/4 system.

IV – Hot Mockup and Special Test Equipment
Describes the hot mockup system and the special test units (990 Power Supply Test Set, 733 ASR Data Terminal) required for depot maintenance of the 990/4 system.

V – Corrective Maintenance
Provides procedures for component removal and replacement and cable repair.

VI – Chassis Troubleshooting Data
Provides a brief description of the chassis wiring and provides wiring diagrams, parts location diagrams and fault isolation procedures for tracing malfunctions down to the replaceable component level.

VII – 990/4 Microcomputer Board Troubleshooting Data
Provides brief theory of operation, timing diagrams and fault isolation procedures for the 990/4 microcomputer board.

VIII – 990/4 Memory Extension Board Troubleshooting Data
Provides brief theory of operation, timing diagrams, checkout procedures and fault isolation procedures for the 990/4 memory extension board.

IX – 990 EPROM Memory Extension Board
Provides theory of operation, timing diagrams, checkout procedures and fault isolation procedures for the 990 EPROM board.

X – 990 Programmers Panel Troubleshooting Data
Provides brief theory of operation, timing diagrams, checkout procedures and fault isolation procedures for the programmer panel.

XI – CRU Expander Board Troubleshooting Data
Provides functional circuit analysis, checkout procedures and fault isolation procedures for the 990 CRU expander board.

XII – CRU Buffer Board Troubleshooting Data
Provides functional circuit analysis and fault isolation procedures for the 990 CRU buffer board used in the 990 expansion chassis.

XIII – Power Supply Troubleshooting Data
Describes the 990 Power Supply Test Setup and provides fault isolation procedures for the ac power converter board, the 20 and 40 ampere power supplies and the optional standby power supply board.

APPENDIX A – Programming Reference Data
Provides a listing of TMS 9900 instructions, op codes, instruction formats, etc., required for maintenance of the 990/4 microcomputer system.

APPENDIX B – Backpanel Connector Listing
Provides a listing of all signals and their associated backpanel pin assignments.

RELATED PUBLICATIONS
The following publications contain information related to installation, operation, and maintenance of the 990/4 Microcomputer System:

Title	Part Number
Model 990 Computer Diagnostics Manual	945400-9701
Model 990/4 Computer System Hardware Reference Manual	945251-9701
Model 990/4 Computer System Field Maintenance Manual	945401-9701
Model 990 Family Maintenance Drawings	945421-9701
Model 990 Computer Family Peripheral Device Field Maintenance Manual	945419-9701
Model 990 Computer PROM Programming Module Depot Maintenance Manual	945405-9701
Model 990 Computer Model 913 CRT Display Terminal Depot Maintenance Manual	945406-9701
Model 990 Computer 16 I/O Data Module Depot Manual	945407-9701
Model 990 Computer Full Duplex EIA Module Depot Maintenance Manual	945408-9701
Model 990 Computer Asynchronous Modem System Depot Maintenance Manual	945409-9701
Model 990 Computer Synchronous Modem System Depot Maintenance Manual	945410-9701
Model 990 Computer 16 I/O EIA Data Module Depot Maintenance Manual	945415-9701
Model 990 Floppy Disc Depot Maintenance Manual	945418-9701
475 Oscilloscope and DM43/DM40 Digital Multimeters – Operators Instruction Manual (Tektronix)	070-1739-01

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

APPENDIXES

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF TABLES

LIST OF TABLES (Continued)

SECTION I

GENERAL DESCRIPTION

1.1 GENERAL

This section provides a brief physical and functional description of the 990/4 Microcomputer System and describes the various system options. Additional theory of operation (at the board level) is provided in Sections VII through XIII.

1.2 SYSTEM FUNCTIONAL DESCRIPTION

The 990/4 Microcomputer System is a modular data processing system consisting of the following major units:

- 990/4 microcomputer
- Optional peripherals including card readers, CRT display terminals, floppy disc units, and line printers
- Optional 733 ASR data terminal(s)
- Optional 990 I/O expansion chassis (up to seven chassis)
- Optional communication networks

A simplified block diagram of a typical 990/4 system is shown in figure 1-1. A brief functional description of each of the major units in the system is provided in the following paragraphs.

1.2.1 990/4 MICROCOMPUTER. The 990/4 microcomputer is available in a variety of configurations including:

- 3 slot OEM chassis with 990/4 microcomputer board in slot one and any combination of optional full or half-slot boards in the remaining two slots. This configuration is not equipped with power supply or cooling fans.
- 6 slot chassis with 20 amp power supply, internal cooling, either a programmer or operator panel, a 990/4 microcomputer board and any combination of optional full or half-slot boards in the remaining 5 slots. This configuration may also be equipped with optional standby power supply.
- 13 slot chassis with 40 ampere power supply, internal cooling, either a programmer or operator panel, a 990/4 microcomputer board and any combination of full and half-size boards in the remaining 12 slots. This configuration may also be equipped with a standby power supply.

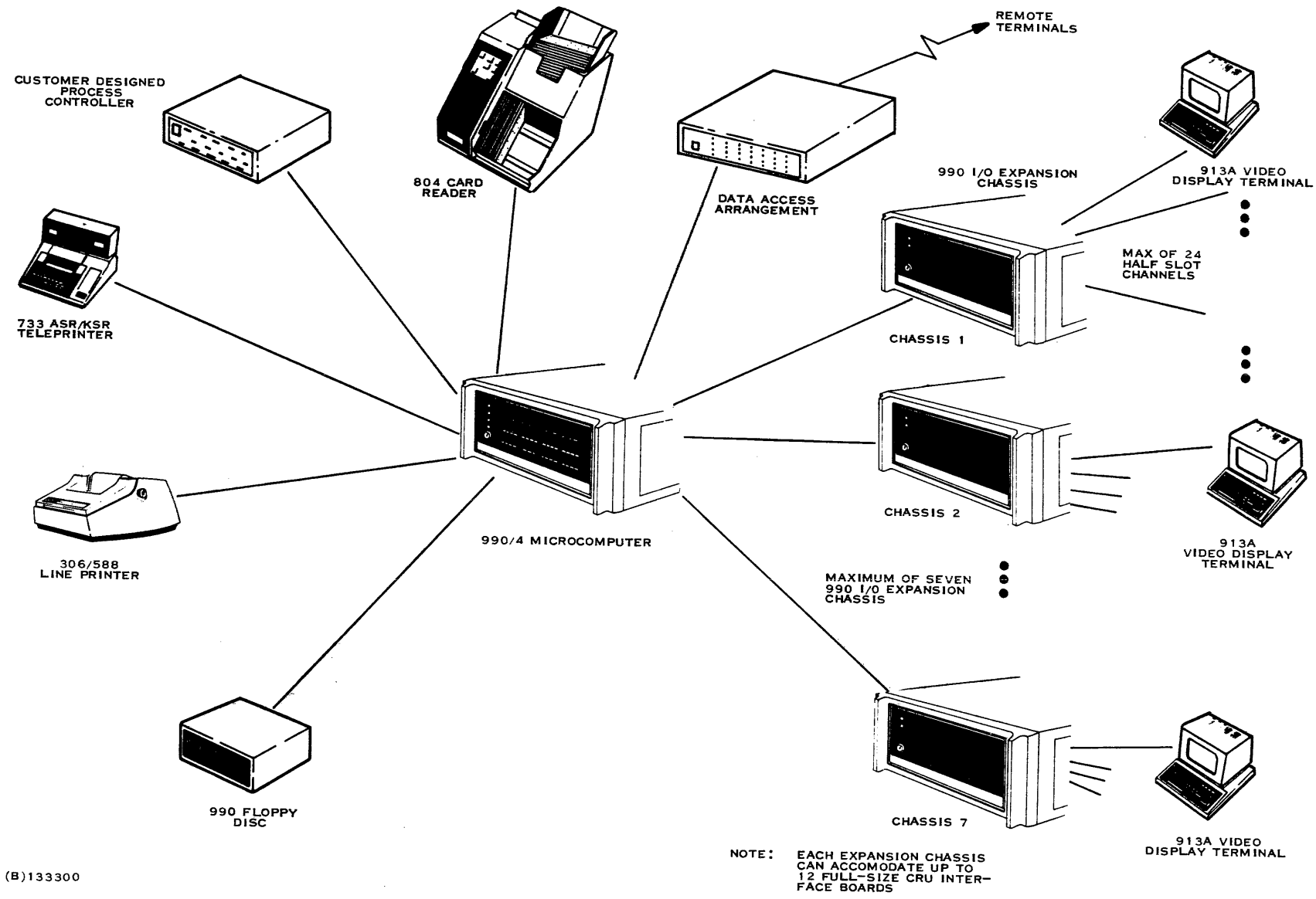


Figure 1-1. 990/4 Microcomputer System

A simplified block diagram showing the board-level organization of a typical 990/4 Microcomputer System is shown in figure 1-2. As indicated in this figure, the 990/4 chassis consists of the following board types:

- 990/4 microcomputer board with a TMS 9900 microprocessor chip, an optional 4K RAM memory, a 1K ROM memory and a programmable CRU (communications register unit) serial I/O interface.
- Optional 990/4 memory expansion board with up to 20K RAM memory (expandable in 4K increments from 4K to 20K) and optional write protect and parity check features.
- Optional EPROM memory expansion board – provides up to 8K of EPROM memory storage.
- Optional CRU expansion board which permits up to seven external 990 I/O expansion chassis to interconnect with the 990/4 main chassis.
- One or more optional CRU interface boards which match the CRU serial interface requirements of the 990/4 microcomputer board with the interface requirements of an external peripheral device, data terminal or external process control equipment.
- Optional programmer panel/programmer panel interface board – permits manual entry of data and commands into the microcomputer and permits data from selected registers and memory locations to be displayed on the panel LEDs in response to commands entered from the panel.
- Two power supply boards including the ac power converter board and the main power supply board (either 20 or 40 ampere main board).
- Optional standby power supply – provides battery power for memory circuits during a power fail condition to preserve data in the semiconductor memories.

A functional block diagram of the 990/4 microcomputer is shown in figure 1-3. The overall operation of each board is briefly described in the following paragraphs.

1.2.1.1 990/4 Microcomputer Board. The 990/4 microcomputer board is a low cost but powerful computer-on-a-board constructed around the TMS 9900 16-bit processor on a chip. The board includes a 4-phase clock circuit which drives the TMS 9900 and synchronizes all onboard and offboard memory transfers between the TMS 9900 and the memory circuits. The board also contains a vectored interrupt structure which encodes the ID of the highest priority interrupt present onto four interrupt lines to the TMS 9900. When an interrupt is present, the microprocessor chip traps to a dedicated memory location (after completion of any present instruction) to obtain the parameters required to enter the appropriate interrupt servicing routine.

Other features incorporated on the 990/4 board include a decode for five external TMS 9900 instructions (which result in no-ops in the chip), a programmable real time clock interrupt network which is driven by a 120 Hz signal from the main power supply board (must be externally supplied in the 3-slot OEM configuration), a two-way bus structure which permits an external DMA memory user to access either the onboard memories or any of the memory space on the expansion boards without interfering with the TMS 9900.

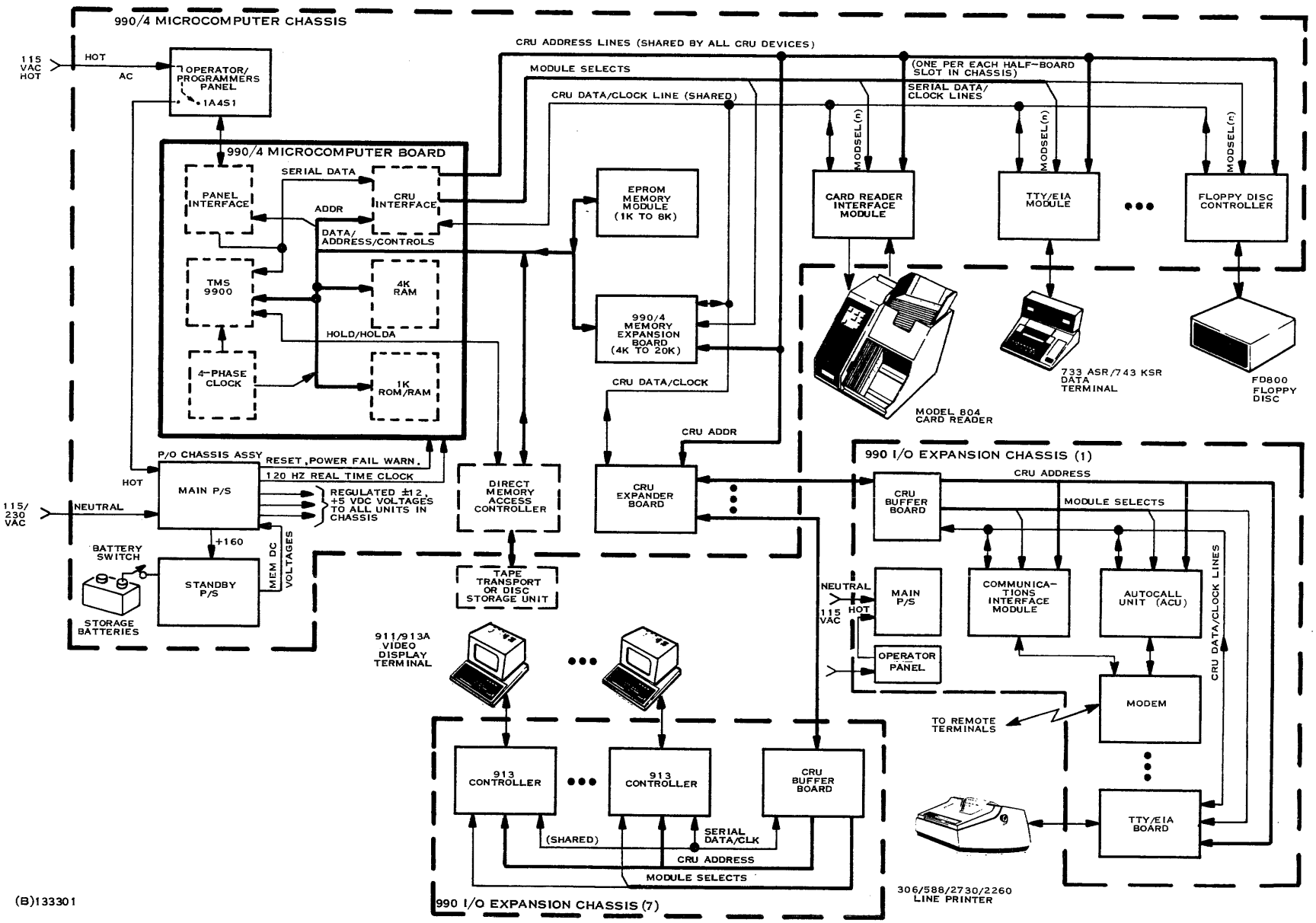


Figure 1-2. 990/4 Board Level Organization

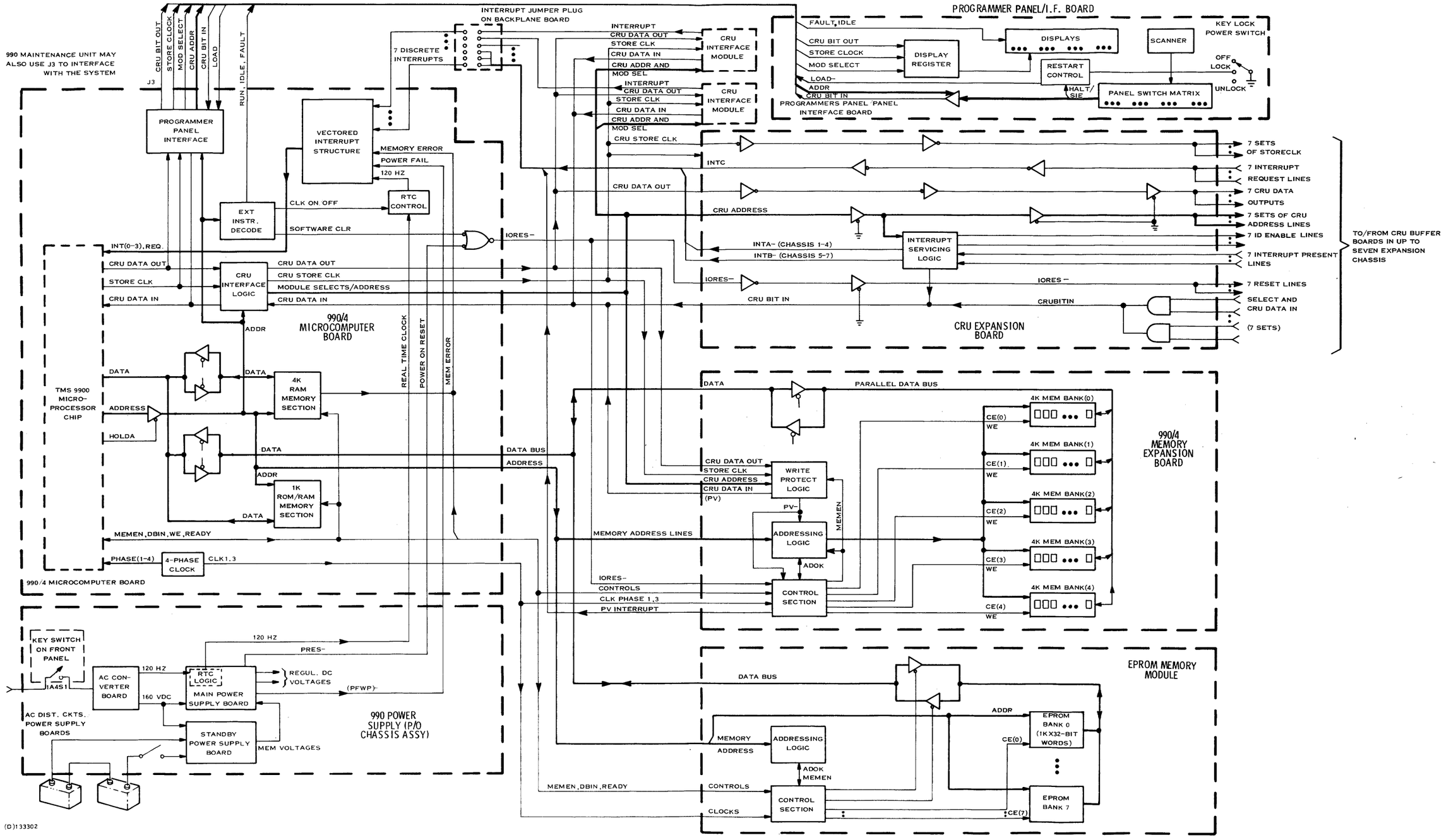


Figure 1-3. 990/4 System, Simplified Functional Diagram

The board also contains the CRU module select decode for the main chassis and special interfacing circuits for the programmer panel (provides a CRU type interface for the panel).

1.2.1.2 **990/4 Memory Expansion Board.** The 990/4 memory expansion board provides an additional 4K to 20K of RAM memory storage (expandable in 4K increments) which is accessible by either the TMS 9900 on the 990/4 board or by an external DMA controller such as a tape or disc controller.

The board also contains a programmable write protect circuit which interfaces with 990/4 software through a conventional CRU serial interface. The upper and lower address protect bounds are serially transferred from the TMS 9900 to the write protect logic on the memory expander board over the CRUBITOUT line. Then prior to any write operation, the address bounds are compared against the memory address supplied by the TMS 9900 or external controller to determine if an attempt is made to write into a protected memory location. If so (and the write protect mode bit is set), the write protect logic inhibits the memory cycle and sets a protect violate latch on the board which can be monitored under software control via the CRUBITIN line. The protect violate latch output also provides the stimulus for a general interrupt which the user can incorporate if desired. The protect violate interrupt is then cleared by issuing an SBZ instruction to the address reserved for the memory expansion board.

The RAM memory on the expansion board is organized in 4K banks with each bank made up of sixteen 4K RAM chips (or 17 if parity option is installed). A read or write cycle is initiated when a memory enable (MEMEN) and a read/write indication (DBIN) are generated by the memory user and the address on the memory address lines falls within the address space recognized by the memory expander board's address decode circuitry. If all of these events occur, the control section on the board generates a chip enable, and write enable (for write cycles) required to initiate a memory cycle and sets up the tri-state data bus to transfer data to or from the specified memory location. If the parity option is installed, the memory board waits until valid read data is available and then checks the read data word for correct parity. If invalid parity is detected, a memory error signal is sent to the 990/4 microcomputer board where it is used to develop a memory error interrupt. The memory expansion board also contains provisions for displaying parity error indications on an LED mounted on the board and for manually clearing the parity error flip-flop.

The memory expansion board is also equipped with jumper wire and switch-selectable options which control the starting memory address recognized by the board and indicates the amount of memory (in 4K increments) implemented on the board. These options are described in greater depth in Section VIII.

1.2.1.3 **EPROM Memory Module.** The 990 EPROM memory module is an optional memory board which may contain from 1K to 8K words (in 1K increments) of memory storage. The memory is implemented with 1024 by 8-bit eraseable programmable read only memory (EPROM) chips which may be removed from the board, erased, reprogrammed and reinstalled on the board.

The starting address for the EPROM module may be set up on any 1K boundary within the 32K address space of the 990/4 microcomputer system. A memory size bias DIP switch is programmed with the amount of memory available on the board.

Another wiring option permits the EPROM board to be used in either a 990/4 or 990/10 system.

1.2.1.4 **Operators Panel.** The operators panel, shown in figure 1-4, provides for key-control of ac power to the system and for manually initiating a bootstrap load operation. The panel also contains two LED displays (POWER and FAULT) which indicate the status of the dc power supplies and the operating status of the 990/4 system based on a built-in diagnostic ROM test. The POWER indicator lights when the power supplies are functioning properly and the FAULT LED lights when a bootstrap load is attempted and the ROM diagnostic on the 990/4 microcomputer board indicates that an error condition exists. When the FAULT LED lights, the load operation is interrupted and the system locks up until the fault is corrected.

The operators panel is normally used on 990/4 microcomputers and I/O expansion chassis where manual control of the system is not required.

1.2.1.5 **Programmers Panel.** The 990 programmers panel (figure 1-5) includes a key-switch for control of ac power to the system. This key switch also permits the panel to be locked out to prevent unauthorized program intervention. Additionally, the panel contains a large array of LED indicators and switches used to enter data into the TMS 9900 registers or memory locations on either the 990/4 board or 990/4 memory expansion boards and to display the contents of selected memory or TMS 9900 locations. The programmer's panel is used on both the 990 microcomputer chassis and on the 990 Maintenance Unit.

NOTE

A detailed description of the programmer panel controls and indicators is provided in Section IV of this manual.

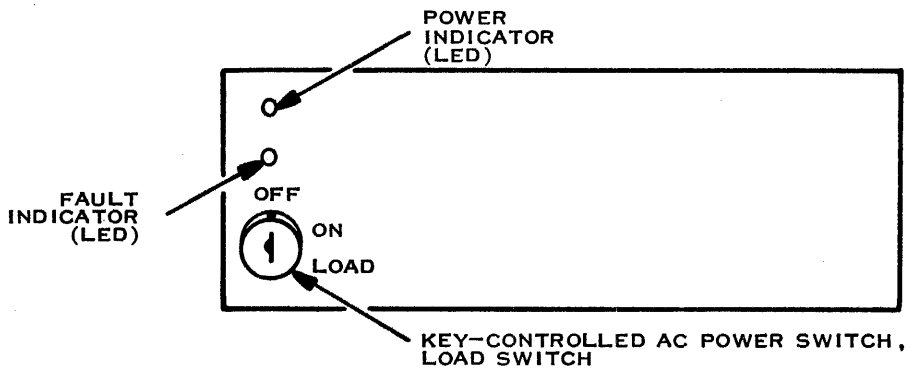


Figure 1-4. 990 Operator Panel

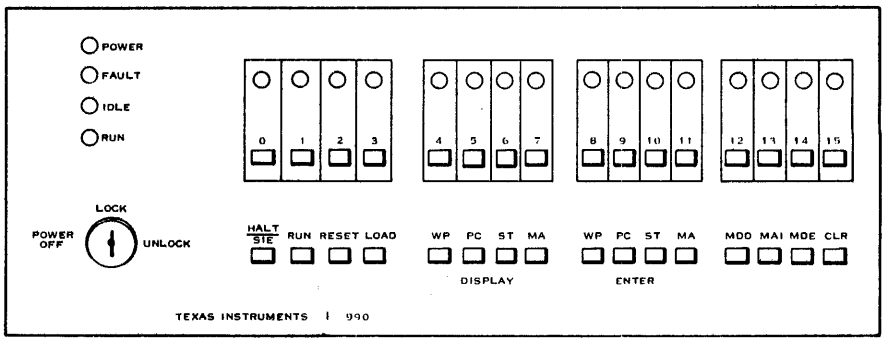


Figure 1-5. 990 Programmer Panel

1.2.1.6 **990 Power Supplies.** Two types of main power supplies are used in 990/4 microcomputer chassis and 990 I/O expansion chassis including a 20 ampere main supply and 40 ampere main supply. The 20 ampere supply is used in 6 slot chassis and 13 slot chassis having relatively low power consumption requirements. The 40 ampere supply is used in the 13-slot chassis.

The main power supply also contains a real time clock circuit which develops the 120 Hz clock output used in the 990/4's programmable interrupt structure. In addition, the power supply develops a power on master clear signal and a power warning signal when ac power failure is imminent. This power warning signal is tied into the 990/4's interrupt structure to permit the 990/4 software up to 7 milliseconds to react to an impending power failure.

An optional standby power supply is also available for use with either the 20 or 40 ampere main supply. During normal ac power conditions, the standby supply is driven by an unregulated output of the ac converter board in the main supply. The standby board then develops the regulated dc voltages used in the memory sections of the computer. The standby supply also maintains a trickle charge on the batteries. In the event of a power failure, the standby supply automatically switches to battery power to preserve memory data in the semiconductor memories. The standby batteries contain enough storage capacity to operate the RAM memories for approximately 30 minutes.

1.2.1.7 **CRU Interface Boards.** All interfaces between the 990/4 microcomputer board and the external peripherals, terminals, communications networks, etc., are accomplished via CRU interface boards which may be located in either the main chassis or in one of the expansion chassis. Basically, the interface boards provide the buffering, packing and unpacking of data required to interface the CRU serial data lines with the serial or parallel interface requirements of various peripherals. Each CRU interface board decodes the address on the CRU address lines when a module select signal is received from the decode logic on the 990/4 microcomputer board (or CRU buffer board for boards located in an expansion chassis). A unique module select line is provided for each half-board slot in the chassis. All other address lines, data lines and CRU clock lines are shared by all CRU interface cards in the chassis. The CRU interface boards gain processor attention via interrupt lines which are optionally wired into the 990's vectored interrupt structure.

Some of the commonly-used CRU interface boards available for use in the 990/4 microcomputer system include:

- 990 TTY/EIA Terminal Interface Module, Part Number 945075-0001
- 16 I/O EIA Data Module, Part Number 945140-0001
- 16 I/O TTL Data Module with Interrupt Option, Part Number 945145-0001
- 990 Communications Interface Module, Part Number 946104-1
- CRU Controller Module, Part Number 945082-1
- Buffered Card Reader Interface Controller, Part Number 945083-2
- PROM Programmer Control Board (part of 944924-1)

990 TTY/EIA Terminal Interface Module. The 990 TTY/EIA terminal interface module provides an interface between any terminal device using an EIA standard RS232 interface or 20 milliampere TTY current loop. This interface board is typically used with the following types of terminals in the 990/4 Microcomputer System:

- 733 ASR/KSR Teleprinter
- 913A video display terminal
- Model 306 line printer
- Model 588 line printer

The following hardwired options are available with the TTY/EIA module:

- Interrupts enabled – if selected, the module will generate an interrupt for each character sent, each character received or when status of the peripheral or terminal device changes
- Selection of data transfer rate of the device (110 to 9600 baud)
- Selection of interface (TTY compatible or EIA compatible)

16 I/O EIA Data Module. The 16 I/O EIA data module provides a general purpose 16-bit input and output interface between the 990/4 microcomputer and any external device containing an EIA interface. An EIA interface is defined as follows:

INPUTS	Logic 1: +3 to +25V Logic 0: -3 to -25V
OUTPUTS	Logic 1: +5 to +8V Logic 0: -5 to -8V

The 16 I/O EIA module is a half-size board containing 16 input lines and 16 output lines. Each line may be addressed as a single binary value or as a member of a group of 2 to 16 lines.

16 I/O TTL Data Module. The 16 I/O TTL data module provides an interface between the CRU portion of the 990/4 microcomputer and any external device which operates on TTL voltage levels. The module provides for 16 input lines and 16 output lines each of which may be addressed as a single binary value via the CRU address lines or as a member of a group of 2 to 16 lines. An alternate version provides for 15 normal inputs, 14 normal outputs, an interrupt output line, and an interrupt mask output.

1.2.1.8 990 CRU Expansion Board. The 990 CRU expansion board basically expands a single CRU port to seven CRU ports which interconnect with up to seven CRU buffer boards in external expansion chassis (see figures 1-6 and 1-7).

The CRU expansion board contains provisions for monitoring interrupts from the expansion chassis and generating an interrupt to the 990/4 microcomputer board which indicates whether the interrupt occurred in chassis 1-4 or 5-7. The board also enables the ID lines from the CRU buffer board in the interrupting chassis to permit 990 software to determine which CRU interface board issued the interrupt. Software interrogates the ID lines via a CRU instruction addressed to the expansion board and reads a 16-bit word vector (by changing the CRU address lines 12-15) which includes the chassis ID, board ID, and interrupt lines.

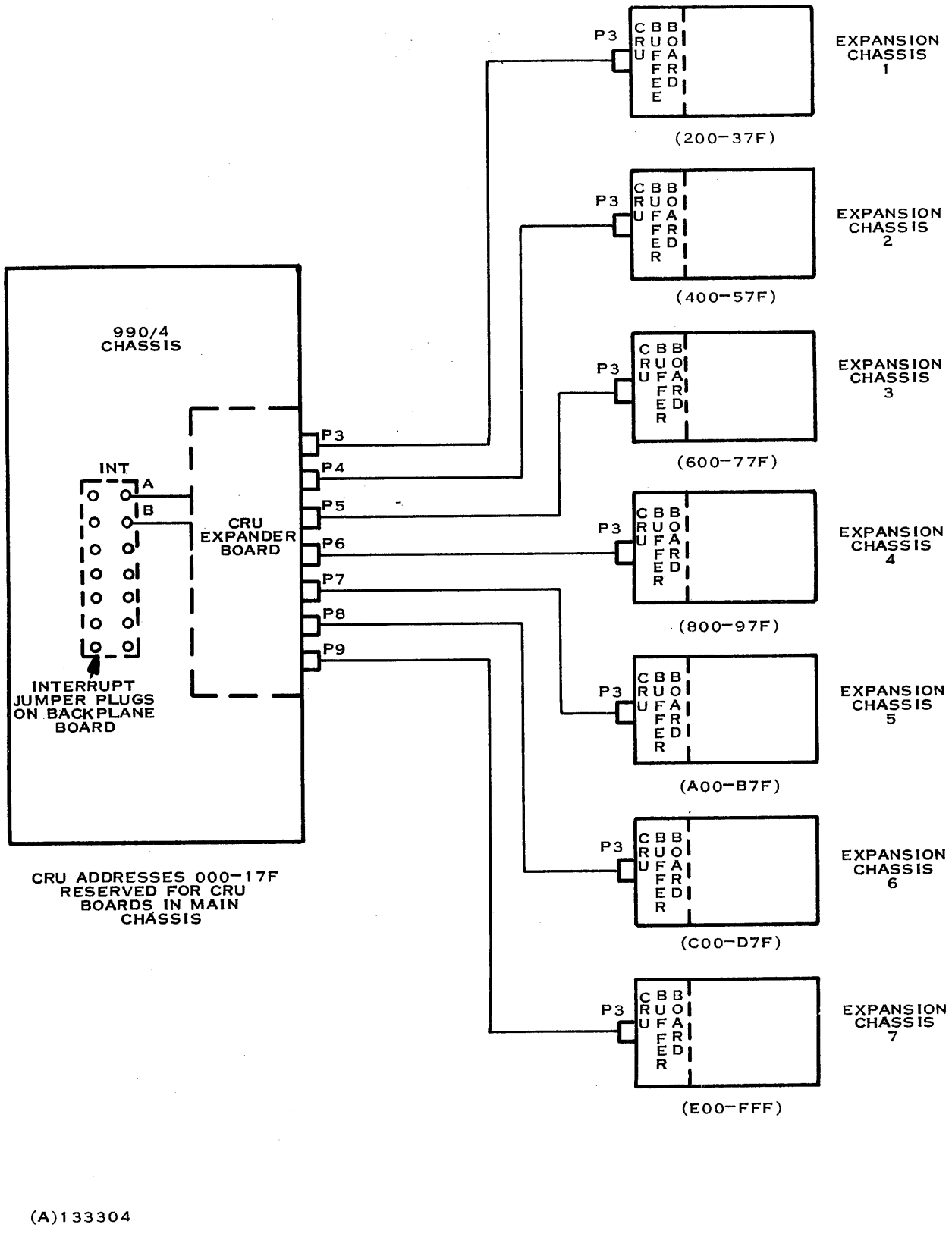


Figure 1-6. CRU Expansion, Simplified Block Diagram

A CRU address map showing the CRU addresses associated with each expansion chassis is provided in figure 1-8. The addresses shown on this map represent absolute CRU addresses (one-half the CRU base address contained in workspace register 12, e.g., $1E0_{16}$ base address corresponds to $0F0_{16}$ absolute address).

1.2.2 **990 EXPANSION CHASSIS.** A 990 expansion chassis is added to a system when the main chassis does not contain enough CRU interface slots for a given configuration. As shown in figure 1-2, the expansion chassis must contain a 990 CRU buffer board in slot 1 which connects to the appropriate connector on the CRU expansion board in the main chassis (see figure 1-6).

1.2.2.1 **990 CRU Buffer Board.** The CRU buffer board provides the module select function for the expansion chassis similar to that performed by the 990/4 microcomputer board in the main chassis. Additionally, the CRU buffer board contains an interrupt scanner which constantly monitors the interrupt lines from the boards installed in that particular chassis and issues an "Interrupt Present" to the main chassis if an interrupt is detected. When the CRU expansion board in the main chassis acknowledges the interrupt by returning an ID enable signal, the CRU buffer board sends over the encoded ID of the board which initiated the interrupt. This information is then examined by 990 software to determine which board issued the interrupt.

1.3 TYPICAL SYSTEM OPERATION

The standard system configuration includes a 990/4 microcomputer (either 6 or 13 slot) with programmer panel, a 733 ASR data terminal and various peripherals and display terminals as indicated in figure 1-1. The following discussion of system operation is based on the standard configuration which includes the following constraints on the 990/4 microcomputer board:

- Starting RAM address on 990/4 microcomputer board wired to 0000.
- Starting ROM address prewired to F800.
- Power up load wired to 0000.
- Restart wired to FFFC.
- 733 ASR/card reader loader ROM with self-test installed on 990/4 board.

1.3.1 **SYSTEM INITIALIZATION.** When the key switch on the programmer panel is set to the LOCK position, ac power is applied to the main chassis. Similarly ac power is applied to each expansion chassis by setting its key switch to the ON position. When the power is first applied to the main chassis, the power supply generates a "system reset" which is routed through the 990/4 microcomputer board to all subsystems in the 990/4 microcomputer system. This signal forces the TMS 9900 microprocessor to trap to location 0000 and begin processing (see figure 1-9).

When the key switch on the programmer panel is set to the UNLOCK position, the HALT/SIE switch on the panel is activated. When the HALT/SIE switch is pressed, a "restart" signal is generated which causes the restart circuit on the 990/4 microcomputer board to generate a LOAD– signal for the microprocessor. This signal causes the microprocessor to trap to location FFFC which is in ROM memory (after saving the workspace pointer, current PC and status register values of the main program).

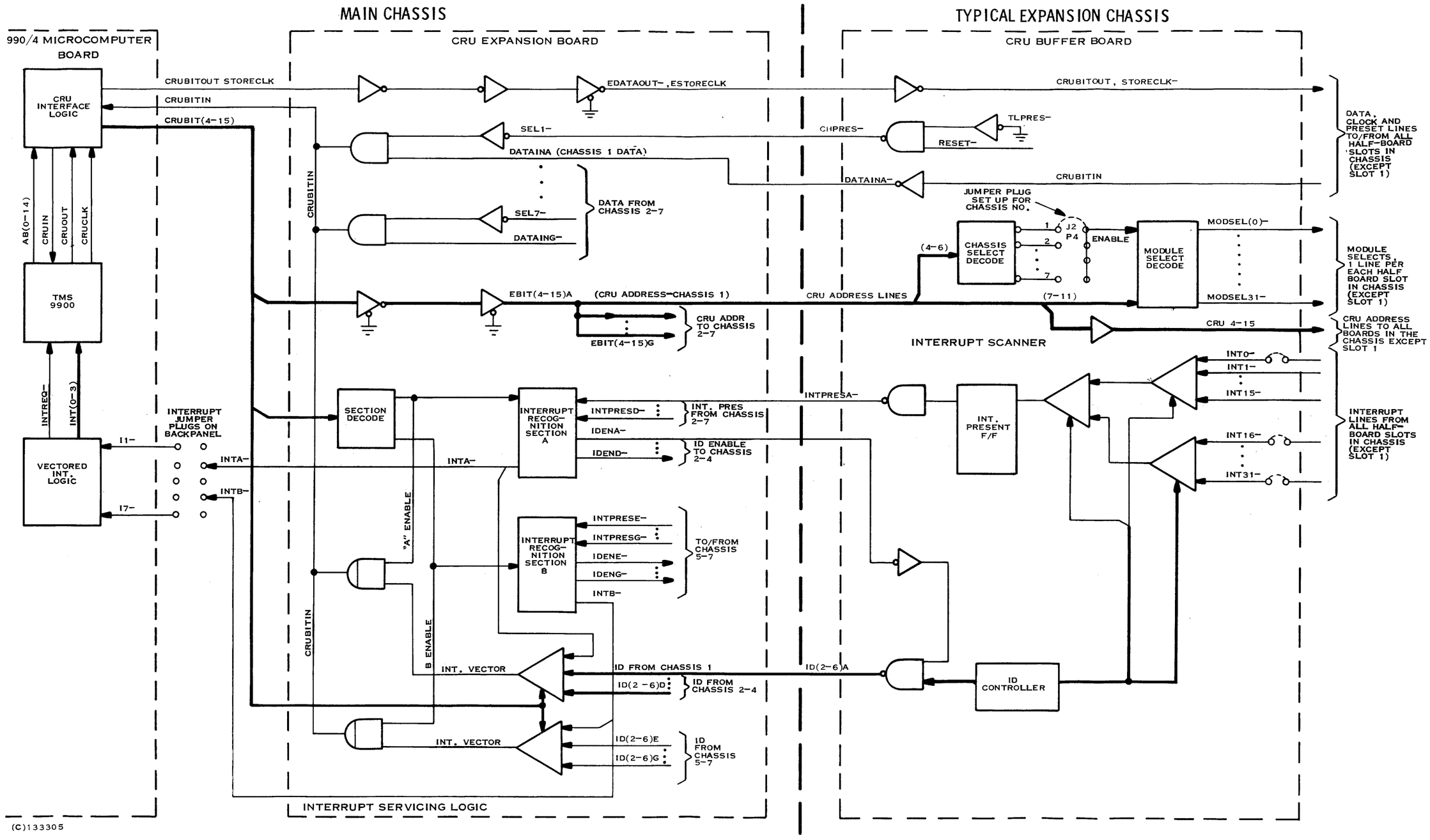


Figure 1-7. CRU Expansion System, Functional Diagram

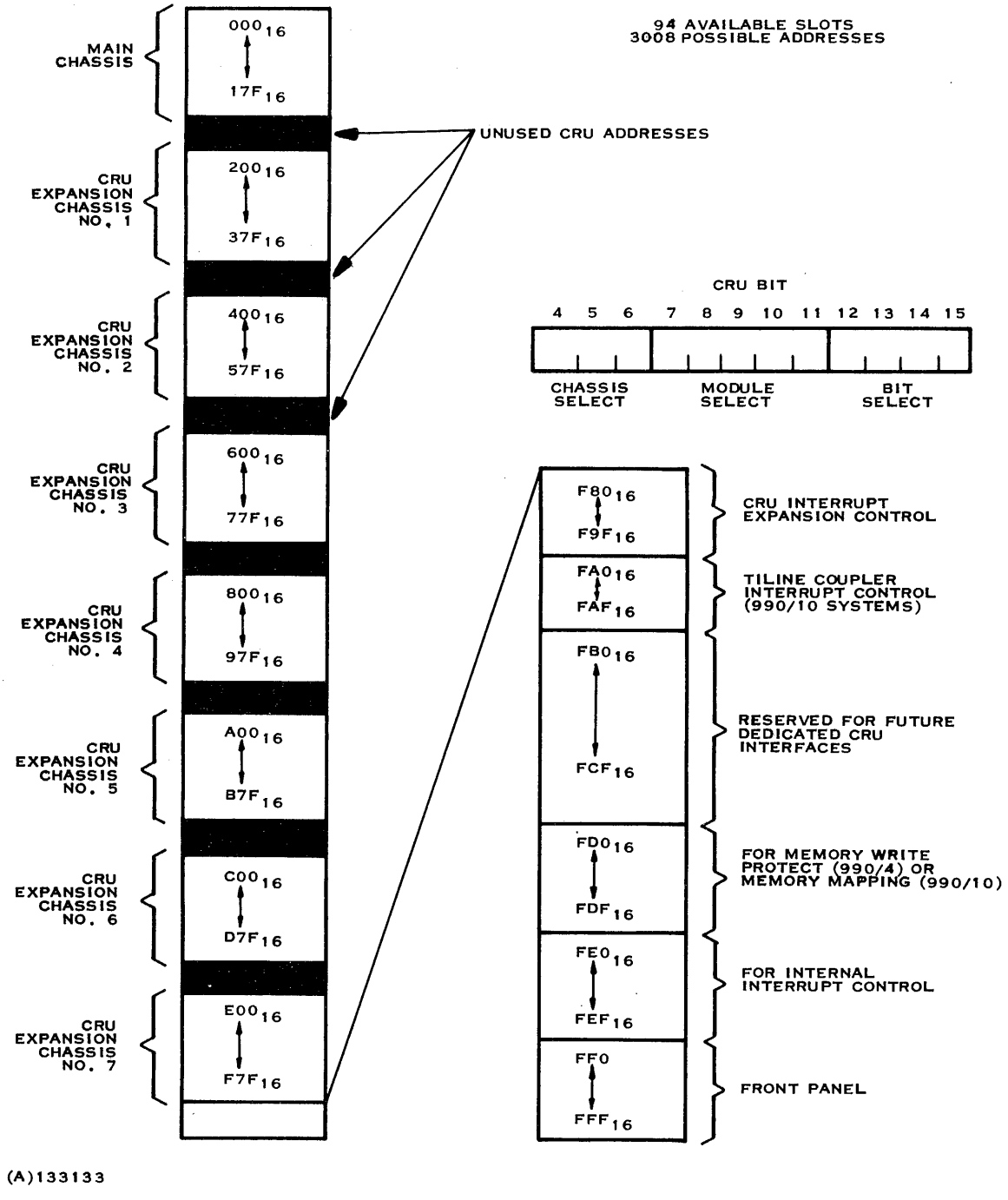


Figure 1-8. CRU Address Map for Standard Expansion (13-slot Chassis)

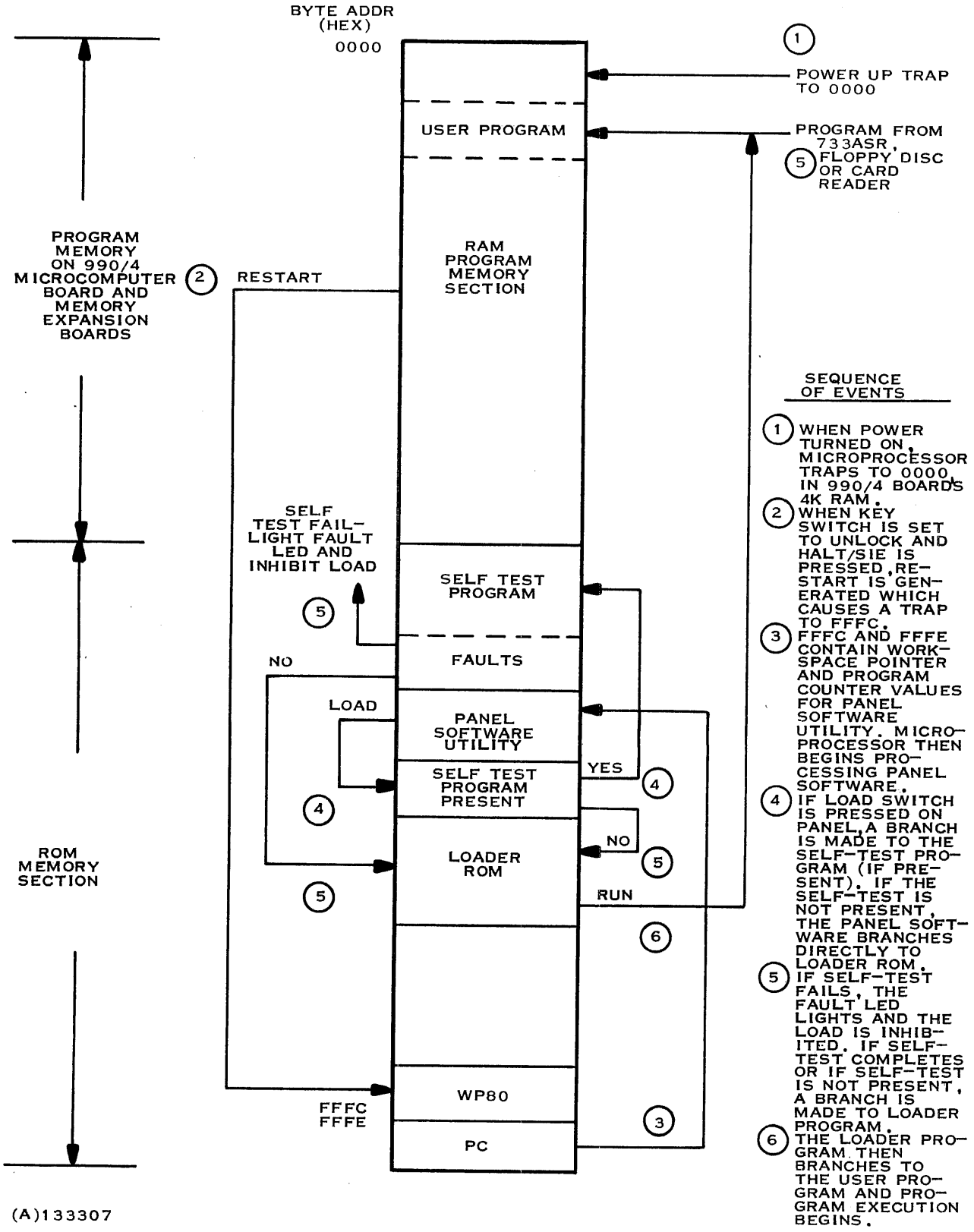


Figure 1-9. Initialization of Standard 990/4 Systems

Location FFFC contains a value of 80_{16} which is the starting memory address for the programmer panel software workspace (workspace pointer). The microprocessor transfers this value to its workspace register and fetches the program counter value (starting memory address for the panel software) from the next consecutive memory address (FFFE).

The TMS 9900 then branches to the starting address of the panel software which is in the ROM address space. As the panel software begins executing, the controls and indicators on the programmer panel become active and the RUN light extinguishes on the panel.

At this point, a program load from a tape cassette on the 733 ASR data terminal (or other peripheral device such as card reader or floppy disc if so equipped) is initiated by pressing the LOAD switch on the programmer panel. Before initiating the load operation, the panel software first branches to the self-test ROM program. If the program fails to run to completion without any errors, the FAULT LED on the programmer panel lights and the LOAD operation is inhibited. However, if the self-test program runs to completion, the program branches to the 733 ROM loader and the user program is loaded into program memory under software control. Upon completion of the load operation, the processor begins program execution (program execution usually is initiated by a transfer vector in the object code of the loaded program).

In order to prevent program intervention from the programmer panel, the key switch is generally set to the LOCK position and the key is removed after completion of the load operation. In this condition, the switches on the panel are completely locked out and manual intervention cannot occur until the key is reinserted and the switch rotated to the UNLOCK position.

1.3.2 **TMS 9900 MEMORY CYCLE.** The TMS 9900 performs a memory cycle to either the onboard 4K RAM or 1K ROM or to the memory on the optional memory expansion boards (RAM or EPROM boards) as follows:

1. Microprocessor sets up the DBIN line to correspond to either a read (High DBIN) or write transfer, places a valid memory address on the address lines and issues a memory enable. In the case of a write transfer, the microprocessor also places valid data on the data bus and issues a write enable (write enable used for RAM accesses in 1K ROM/ RAM memory only).

2. The TMS9900 bus logic on the board looks for a 4KOK or a 1KOK from the onboard address decode circuits. If the address is not within the onboard memory address space, the bus control logic sets up the tri-state data and address drivers for an offboard memory transfer. If the address is within the onboard address space, the offboard address and data lines are disabled.

1.3.3 **MEMORY CYCLE BY DMA CONTROLLER.** A memory cycle by a DMA controller is similar to a memory cycle by the processor except that the sequence is preceded by a memory request from the controller (HOLD) and a corresponding acknowledge by the processor (HOLDA) when the processor is ready to relinquish memory. The 990/4 board's bus control logic places the onboard tri-state drivers in the high impedance state and the external user provides the DBIN, MEMEN, address (and data and write enable in case of write cycles). When the controller is ready to relinquish memory, it deactivates the HOLD– line which permits the microprocessor to regain control of memory.

1.3.4 **INTERRUPT SERVICING.** The 990/4 microcomputer uses eight priority levels as shown in table 1-1. A priority ranking system assigns numbers from 0 (highest priority) to 7 (lowest priority) so that interrupt conflicts can be resolved. The highest priority level is used for the power-up trap and seven inputs (INT1– through INT7–) are assigned to various

Table 1-1. Interrupt Level Data

Interrupt Level	Vector Location (Trap Address)	Device Assignment	Enabling Mask Values
0	00	Reset	0 through F
1	04	Power failure	1 through F
2	08	Memory error	2 through F
3	0C	External device	3 through F
4	10	External device	4 through F
5	14	Real time clock*	5 through F
6	18	External device	6 through F
7	1C	External device*	7 through F

*Real time clock interrupt may be implemented at interrupt level 5 or 7 or may be disconnected. The normal configuration is for implementation at level 5.

onboard and offboard interrupts including memory error, real time clock, and power fail interrupts plus any external interrupts which are jumper wired on the interrupt plugs on the backpanel board. The interrupt lines are synchronized with the microprocessor clock on the 990/4 circuit board, encoded, and presented to the TMS 9900 Microprocessor along with an interrupt request, INTREQ–. The interrupt levels are vectored for rapid reaction to recognized interrupts. That is, corresponding to each interrupt level is a 2-word vector located in low-order memory (addresses 0 through 1F, hexadecimal). When the TMS 9900 Microprocessor recognizes an interrupt, it loads the vector for that level into WP (first vector word) and PC (second vector word) to define the new workspace and program starting point for the interrupt servicing routine. The old values of the WP, PC, and ST are saved at the bottom of the new workspace. When the interrupt routine is complete, the microprocessor returns to the program that was executing when the interrupt occurred by restoring the original values to the PC, WP, and ST registers. Should a higher priority interrupt occur while an interrupt service subroutine is executing, the microprocessor will honor the interrupt. The microprocessor enters the higher priority interrupt subroutine and preserves the linkage to the earlier interrupt in the same manner described for the first interrupt. Thus, many interrupts can occur simultaneously with the microprocessor maintaining an orderly linkage between the interrupt programs. Table 1-1 lists the interrupt levels, assignments, vector location, and mask information. Three interrupt conditions are generated on the 990/4 circuit board and are wired directly to external interrupts INT1–, INT2–, and INT5– (or INT7–). Any of these three interrupts may be disconnected by cutting a jumper wire.

1.3.4.1 **Interrupt Masking.** The microprocessor uses a 4-bit field in the status register to determine the lowest priority interrupt that will be recognized during a program operation and also to ensure that an interrupt service routine will not be halted due to another interrupt of equal or lower priority. At the start of a program the mask field in the status register is loaded with the mask value. The microprocessor compares this value continuously with any interrupts that occur. If the level of the interrupt is equal to or less than the mask value (equal or greater priority), then the microprocessor recognizes the interrupt and calls the service routine for that interrupt level. When the microprocessor sets up the service routine, it loads a value into the mask field that is one less than the interrupt level being serviced, thereby disabling interrupts from devices of equal or less priority. The enabling mask values for the different interrupt levels are also shown in table 1-1.

SECTION II

BENCH TEST SETUP

2.1 GENERAL

This section describes the bench test setup and the special tools and test equipment required to perform depot-level maintenance on the various subassemblies of the 990/4 Microcomputer System.

2.2 WORK STATION REQUIREMENTS

The work station requirements for performing depot-level maintenance varies somewhat depending on the size of the facility and the volume of work. For a smaller facility, a single workstation serves a dual function of test and troubleshooting and corrective maintenance. However, for the larger depot facilities having a high volume of work, several test and troubleshooting workstations may be supported by one (or more) corrective maintenance workstation. In general, both types of workstations should be well lighted, protected against static electricity buildup (damaging to MOS IC), and provide adequate space for the required tools and test equipment.

2.2.1 TEST AND TROUBLESHOOTING STATION. The test and troubleshooting station should provide sufficient work space to house a 990/4 hot mockup system and supporting test equipment including the 990 power supply test set and dual trace oscilloscope (see Section IV for detailed description of hot mockup system). This station should also be provided with a source of compressed air (regulated at 40 psi), and both 115 and 230 vac, 50 to 60 Hz input ac power fused at 30 amperes. A typical test and troubleshooting station is shown in figure 2-1. The test equipment required to support depot-level maintenance is listed and described in table 2-1.

2.2.2 CORRECTIVE MAINTENANCE WORKSTATION. The corrective maintenance workstation should be well lighted and provide adequate space for parts storage bins and the special tools and materials required to perform depot-level maintenance. A typical corrective maintenance workstation is shown in figure 2-2. The associated tools and materials are listed and described in tables 2-2 and 2-3. The bench top, stool and floor space immediately in front of the workstation should be covered with an electrically conductive material, such as the Velostat plastic product line (manufactured by 3M Company), to provide static electricity protection for working with the 990 memory boards.

The repair workstation should also be equipped with a lighted magnifier unit to permit close inspection of printed circuit etch and component repairs. The station should be provided with a source of shop air (70 to 90 psi) and a multioutlet 115 vac, 50-60 Hz power line fused at 30 amperes.

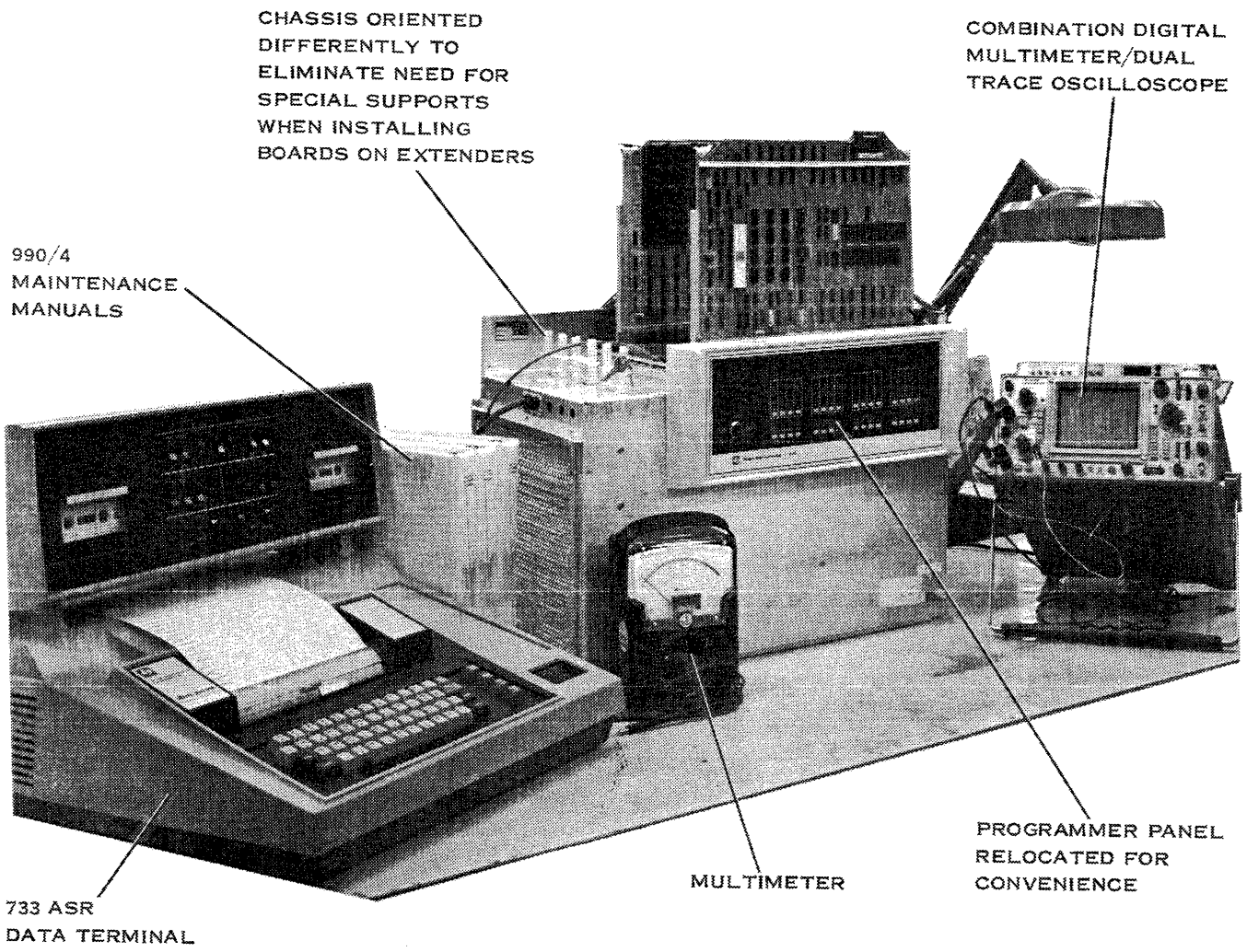


Figure 2-1. Typical Depot Maintenance Workstation

Table 2-1. Test Equipment Required for Depot Maintenance

Test Equipment Type	Function	Manufacturer	Model or Part No.
Dual trace oscilloscope with built-in digital voltmeter	Troubleshooting circuit boards to component level; performing power supply tests and adjustments	Tektronix	475 with DM40
990/4 microcomputer system hot mockup (see Section IV for details)	Used to troubleshoot faulty subassemblies	Texas Instruments	–
990 power supply test set	Used in troubleshooting 990/4 power supplies	Texas Instruments	946158-1
990 full size extender board	Permits full size logic boards to be operated outside the 990/4 or 990 I/O expansion chassis	Texas Instruments	975170-1
990 half-size extender board	Permits half-size logic boards to be operated outside the 990/4 or 990 I/O expansion chassis	Texas Instruments	945071-1
990 ac power converter test set	Used to troubleshoot ac power converter board in 990 power supply	Texas Instruments	947871-1

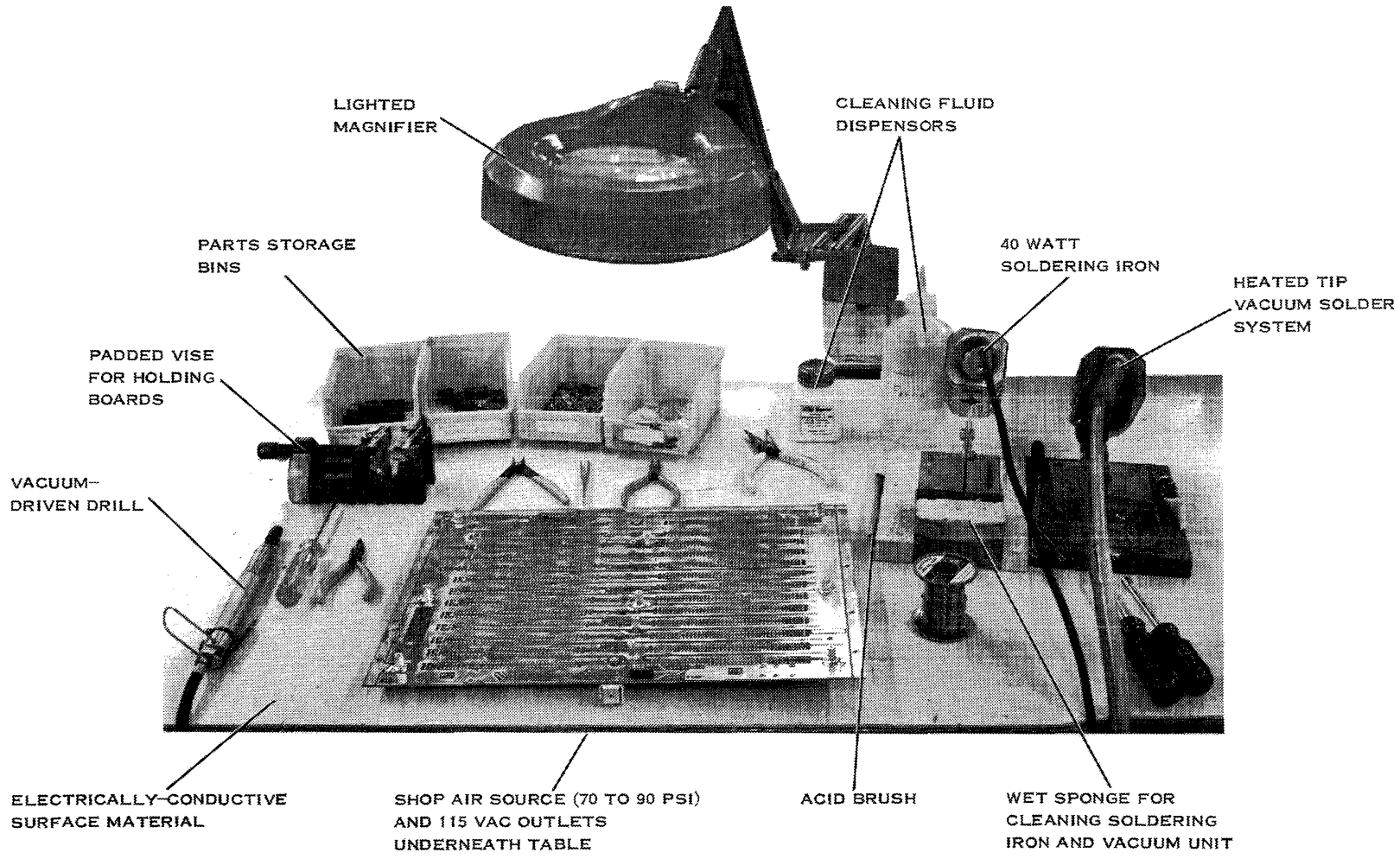


Figure 2-2. Typical Depot Level Corrective Maintenance Workstation

Table 2-2. Tools Required for Depot Maintenance

Tool Description	Purpose	Manufacturer*	Model or Part No.
IC extraction and insertion tool	Remove and replace ICs	GC Electronics	9481
Flat cable assembly press	Installing connectors on flat cables	3M Company	3440
Locator plate (for 26 conductor ribbon cable)	Used with assembly press to install connectors on flat cables	3M Company	3443-7
Cable shear	Used with assembly press to cut flat cable	3M Company	3437
Cable extractor tool	Used to remove socket connectors from mating posts	3M Company	3438
Heated tip solder vacuum system	Used in removing and replacing components on logic boards	Air-Vac Eng. Co.	–
Variable power supply module	Part of solder vacuum system	Air-Vac Eng. Co.	VPM-1A
70 watt solder gobbler	Part of solder vacuum system	Air-Vac Eng. Co.	SG-200-Z70
Stand and maintenance kit	Part of solder vacuum system	Air-Vac Eng. Co.	SDK-3
Alcohol dispensor	Used to dispense alcohol or other cleaning solvents	Menda	613
Polyethylene syringe, 50cc	Used to dispense liquid flux for board repairs	Techon	TS50T
Tiewrap gun	Installing plastic tiedown straps	–	MS3367, 68
Heat gun	Installing heat shrinking tubing in power supply unit	–	–
Diagonal cutter pliers	Clipping and removing components cutting leads to proper size	Microshear	170
Needlenose pliers, no serrations	Installing and removing components	–	–
X-acto knife	Repairing circuit board etch	–	–
Disposable wipers	General cleaning purposes	–	–
30 watt soldering iron and station	Installation and removal of board components	–	–
Table top vise	Holding boards during component removal and replacement	–	–
Soldering aid kit	Board repairs	–	348

*or equivalent

Table 2-2. Tools Required for Depot Maintenance (Continued)

Tool Description	Purpose	Manufacturer*	Model or Part No.
Acid brushes	Cleaning of boards, applying flux to large areas, etc.	–	–
Set of heatsinks	Heat protection for removing and replacing LEDs	–	–
Wire strippers modified with Polystrip universal wire stripper replacement blades	Stripping flat cables	Stripmaster	–
Industrial tweezers	Board repair use	–	–
Standard technicians screwdriver set	Equipment assembly and dis-	–	–
Nut driver set	Equipment Assembly and disassembly	–	–
Sponges	Cleaning of soldering iron and heated tip vacuum system	–	–

*or equivalent

Table 2-3. Materials Required for Depot Maintenance

Material Description	Function
Denatured alcohol	Board and component cleaning
Rosin core solder, 63/37, .030 core diameter	Installing and removing components
Rosin base solder cream (alpha 711)	Improve solder joints for tarnished components or etch, dispensed through hypodermic syringe

SECTION III

ASSEMBLY AND DISASSEMBLY PROCEDURES

3.1 GENERAL

This section provides instructions required to remove and replace subassemblies of a 990 computer or I/O expansion chassis.

3.2 CIRCUIT BOARD REMOVAL

Logic boards are removed from a 990 chassis using the following procedure.

CAUTION

Always turn ac power OFF to the chassis before attempting to remove circuit boards. Failure to observe this precaution may result in damage to circuit board components since the connector pins are temporarily misaligned during the removal procedure.

1. Set the keyed switch on the operator/programmer panel of the chassis to the OFF position.
2. Remove the front edge interface connectors from the board.
3. Simultaneously lift the inside edge of both ejector tabs on the board to free the board from the backplane connector.
4. Remove board from the chassis.

3.3 LOGIC BOARD REPLACEMENT

Logic boards (or extender boards) are installed in a 990 chassis using the following procedure:

1. Set the keyed switch on the operator/programmer panel on the chassis to the OFF position.
2. Insert the board into the desired slot with the component side of the board facing upward.
3. Ensure that the slots in the circuit board mate properly with the alignment comb on the backplane connector.
4. Press the board firmly into place and ensure that the board is properly seated.

3.4 FILTER REMOVAL AND REPLACEMENT

The washable filter used in the 990 chassis snaps into place. The unit is removed by applying finger pressure along the top and bottom edges.

3.5 REMOVAL AND REPLACEMENT OF CHASSIS COMPONENTS

Most of the ac power distribution conponents, the ac power converter board (1A2) and the two chassis cooling fans are accessed by removing the access plate directly behind the filter unit (see figure 6-2). Six screws must be removed from the perimeter of the air filter in order to remove the access cover.

3.5.1 AC POWER CONVERTER BOARD. The ac power converter board is removed as follows:

1. Remove cable plugs 1A2P1, 1A2P2 and 1A2P3 from board.

2. Remove single screw in center of board.

The board is installed by inserting the holding screw and reinstalling the three cable plugs.

3.5.2 CAPACITOR 1C1. The large electrolytic capacitor (1C1) is removed from the chassis by removing the two screw-type terminals from the top of the capacitor and clipping the two plastic tie-down straps which hold the capacitor in place.

WARNING

Prior to removing capacitor 1C1, ensure that capacitor is fully discharged by placing screwdriver blade across positive and negative terminals.

To install a new capacitor, use two new plastic tie-down straps (with rough side against the capacitor) and pull tight using a tiewrap gun or needlenose pliers. If pliers are used, the excess length of strap beyond the joint should be clipped using diagonal cutters.

CAUTION

Correct polarity must be observed when installing electrolytic capacitors. The orange/white wire must connect to the positive terminal and the blue/white wire must connect to the negative terminal.

3.5.3 COOLING FANS. The cooling fans are removed by unplugging the two snap-on terminal wires and removing two hold-down screws. Installation is accomplished by reversing this procedure.

3.6 FRONT PANEL REMOVAL AND INSTALLATION

The front panel (operator or programmer type) is removed from the chassis using the following procedure:

1. Remove side access panel (directly opposite open side of computer) by removing six holding screws around the panel perimeter.

2. Remove two screws from the rear of the panel on each side of the panel (4 screws total).

3. Remove the two terminal clamps from the ac microswitch (1A4S1) on the rear of the key switch.

4. Remove connector plug 1A4P3 from top of 990/4 microcomputer board and push plug through slot in chassis.

The panel may be reinstalled by reversing the above procedure.

3.6.1 REMOVAL/REPLACEMENT OF KEY SWITCH. The key switch may be removed from the panel using the following procedure (see figure 3-1):

1. Remove key from switch.
2. With panel out of the chassis and rear of panel facing upwards, remove outer nut and disassemble switch. Then loosen and remove two nuts which secure switch to panel.
3. Remove key from new switch to ensure proper alignment of tumblers.
4. Install holding nuts to secure switch to panel. Tighten first nut against panel. Then tighten second nut without turning first nut.
5. Install springs in spring holders.
6. Ensure that cam is installed in accordance with figure 3-1 and install outer nut.

3.6.2 SWITCH REPLACEMENT. Faulty keyboard switches are removed and replaced in groups of four. The removal procedure is as follows:

1. Using heated tip solder vacuum system, remove solder from the nine leads which connect the switch block to the programmer panel board.
2. Remove four screws from switch block and remove block from chassis.

To install a new switch block, reverse the above procedure.

3.6.3 PROGRAMMER PANEL INTERFACE BOARD REMOVAL AND REPLACEMENT. To remove the programmer panel interface board, use the following procedure:

1. Remove the six holding screws (two on each end and two in the middle).
2. Using heated tip solder vacuum system, detach all interconnecting leads between the switch blocks and the board.

Board installation is the reverse of the above procedure.

3.7 POWER SUPPLY REMOVAL AND INSTALLATION

The 990 power supply consists of an ac converter board (removed and installed as described in paragraph 3.5.1), a main power supply board (1A3) and an optional standby power supply board. Access to the main and standby power supply boards is gained by removing the side access panel (opposite the open side of the computer) which is held in place by six holding screws around the perimeter of the panel.

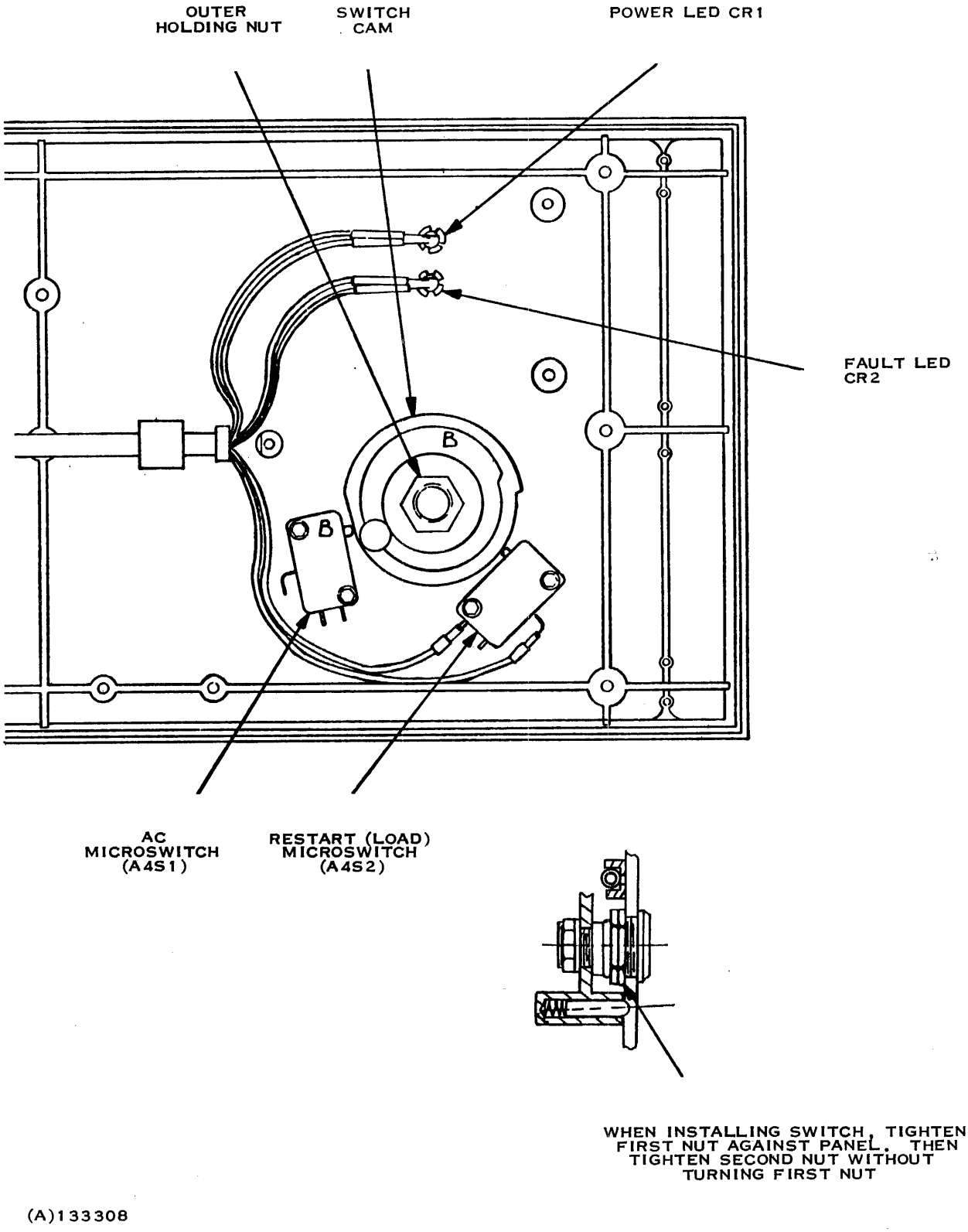


Figure 3-1. Key Switch Removal and Installation Diagram

3.7.1 **MAIN POWER SUPPLY BOARD REMOVAL AND REPLACEMENT.** The main power supply board is removed from the chassis using the following procedure:

1. If standby board is installed, remove in accordance with procedure in paragraph 3.7.2.
2. Remove 4 holding screws (2 on each end of board) and three standoffs from center of board.
3. Remove connectors 1A3P1A (or 1A3P1B for 40 amp power supply) and 1A3P2 from board.

The main power supply board may be installed by reversing the above procedure.

NOTE

Two board guide pins are provided on the backplane to permit proper alignment of board on the backplane.

3.7.2 **STANDBY POWER SUPPLY BOARD REMOVAL AND REPLACEMENT.** The standby power supply board is removed from the chassis using the following procedure:

1. Remove 1A6P1 and 1A6P2 from standby board. Remove 1A3P3 from main power supply board.
2. Remove five holding screws from board.

Installation of a standby board is the reverse of the above procedure.

3.8 BACKPLANE REMOVAL AND INSTALLATION

The backplane assembly may be removed from the 990 chassis using the following procedure:

1. Remove all logic cards from the backplane.
2. Remove side access panel by removing six screws around perimeter of panel.
3. Remove two screws (one from top and one from bottom plate) which hold backplane to top and bottom panels.
4. Remove the 16 screws (8 on each side) which hold the backplane to the card guides.
5. Remove backplane through side opposite the normally open side of the computer.

Installation of a backpanel is essentially the reverse of the above procedure.

SECTION IV

HOT MOCKUP AND SPECIAL TEST EQUIPMENT

4.1 GENERAL

This section describes the depot maintenance philosophy for the 990/4 system, describes the hot mockup, and provides operating procedures for the special test equipment required to perform depot-level troubleshooting.

4.2 MAINTENANCE PHILOSOPHY

Depot maintenance for the assemblies and subassemblies is based on the use of a 990/4 hot mockup, a 990 power supply test set and a combination dual-trace scope/digital multimeter as shown in figure 4-1. Suspect boards from the Field Maintenance Repair Facilities are serviced, one at a time, by placing the defective board on an extender board in the 990/4 chassis (or 990 I/O expansion chassis when testing CRU buffer boards). Initially, the board is tested under control of a diagnostic tape read into 990/4 memory from a cassette transport located in the 733 ASR data terminal. Any resulting error messages are then printed out on the 733 teleprinter.

Fault isolation down to the replaceable component level is performed using scoping loops (type determined by previous error message printout) entered from the programmers panel on the hot mockup chassis in conjunction with a dual trace scope/digital multimeter, the troubleshooting procedures provided in Sections VI through XIII, and the logic and assembly diagrams located in the 990 Family Maintenance Drawing Manual.

Troubleshooting 990 power supply assemblies is performed on the 990 power supply test set rather than in the hot mockup to permit access to the internal components of the power supply assemblies.

Once the faulty component(s) has been identified, the board should be properly tagged (describing the corrective maintenance to be performed) and sent to the corrective maintenance workstation for repair. The repaired board is then returned to the troubleshooting workstation and tested for further problems. If the diagnostic test runs to completion five consecutive times, without an error message printout, the board is returned to normal use.

4.3 SPECIAL TEST EQUIPMENT

The special test equipment required to perform depot maintenance includes:

- 990/4 hot mockup system
- 990 Power supply test set
- Ac Power converter test set

The operating controls and indicators and normal operating procedures for these units are provided in the following paragraphs.

NOTE

Refer to the manufacturer-supplied user manuals for oscilloscope/ digital multimeter operating procedures.

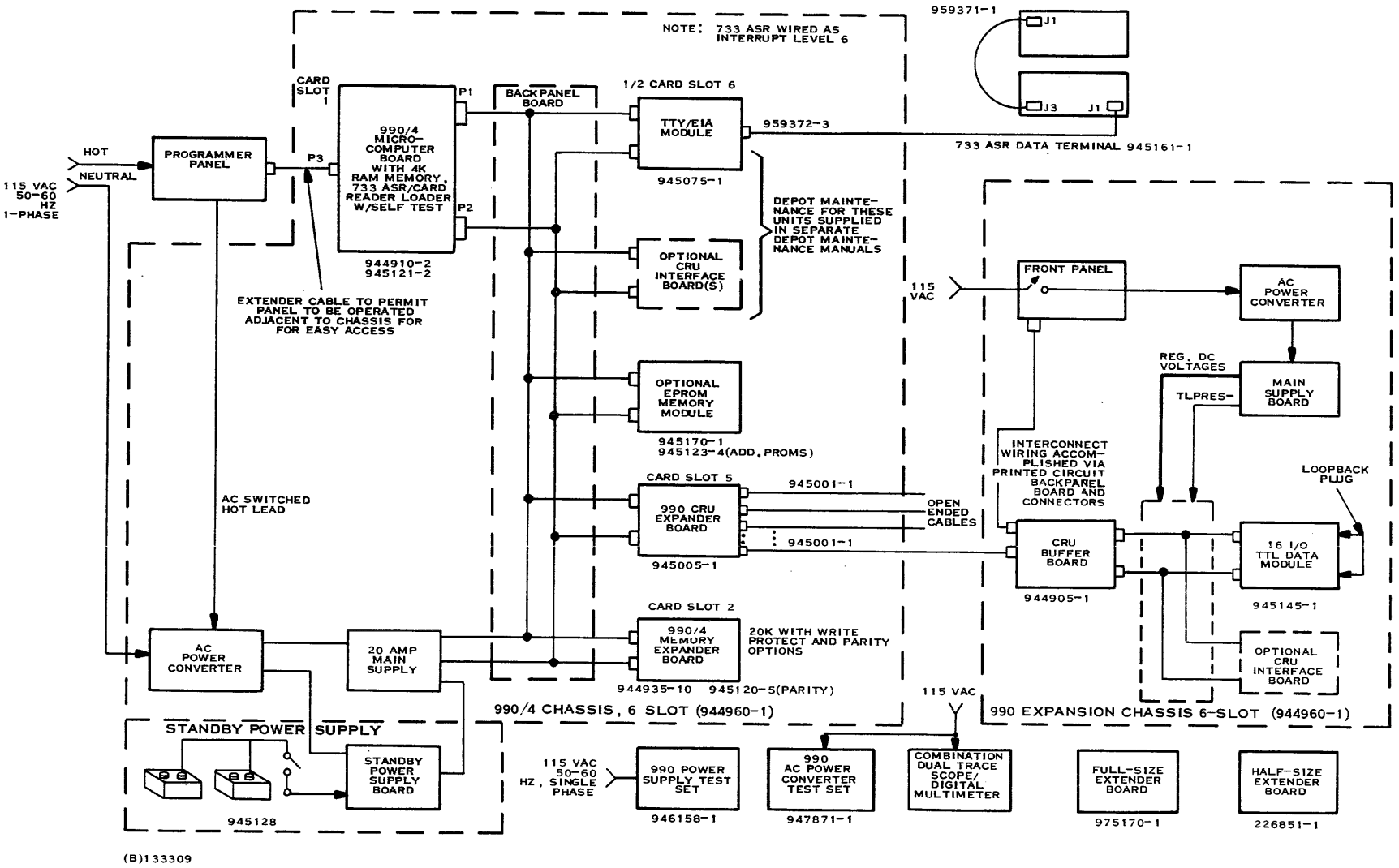


Figure 4-1. 990/4 Hot Mockup System, Block Diagram

4.3.1 **990/4 HOT MOCKUP SYSTEM.** The 990/4 hot mockup system consists of the following hardware units:

- 990/4 6-slot chassis with programmer panel and standby power supply options (Part Numbers 944960-1 and 945128-1)
- 990/4 microcomputer board with 4K RAM memory (Part Number 944910-2) and 733 ASR/card reader loader ROM with self-test (Part Number 945121-2)
- 990/4 memory expansion board with 20K memory and write protect option (Part Number 944935-10) and parity option (Part Number 945120-5)
- 733 ASR kit including TTY/EIA module, interface cable and 733 ASR data terminal (Part Number 945161-1)
- 990 CRU expansion kit including 990 CRU expansion board, interface cable and CRU buffer board (Part Number 944985-1)
- 6-slot 990 I/O expansion chassis with optional peripheral interface boards or associated peripherals, depending on subsystems serviced by the depot maintenance facility (chassis Part Number 944960-2)
- 16 I/O TTL data module (Part Number 945145-1)

A block diagram of the hot mockup system is shown in figure 4-1.

4.3.1.1 **990/4 Diagnostics.** A list of diagnostic tests available to support 990/4 system maintenance is provided in table 4-1. For detailed diagnostic user information, refer to the 990 Computer Diagnostics Handbook.

4.3.1.2 **733 ASR Data Terminal.** The 733 ASR data terminal is used to load diagnostics from tape cassettes into the computer memory and to provide hardcopy printout of test results. The keyboard permits the operator to communicate with the diagnostic software when system parameters are required to execute the diagnostic or when calling up one of the loop programs available with some diagnostic systems (see Model 990 Computer Diagnostics Handbook for details).

A photo showing the 733 ASR is provided in figure 4-2. As indicated in this figure, the 733 is equipped with two cassette transports. When one transport is in the read or playback mode, the other transport is in the record mode (this features permits duplicating diagnostic tapes on the 733).

The 733 ASR controls and indicators are shown in figure 4-3 and listed and described in table 4-2. However, only the controls and indicators associated with loading diagnostics into the computer are described in table 4-2.

For additional information on the 733 ASR, refer to the *Model 990 Computer, Model 733 ASR/KSR Data Terminal Installation and Operation.*

Table 4-1. 990/4 Diagnostics

Diagnostic Title	Part Number	Function
HDT04	945460	Hardware demonstration test – 990/4
RAM04	945440	Random access memory test – 990/4
AU04	945434	990/4 arithmetic unit test
ROMVER	945443	ROM verifier test – 990/10 and 990/4
MEMPRO04	945442	Memory protect logic test – 990/4
EROMBT	945459	EROM memory board test – 990/10 and 990/4
CRUTST04	945446	CRU interface logic test – 990/4
CRUEXP	945457	CRU expansion chassis interface test – 990/10 and 990/4
TST733	945447	733 ASR/KSR data terminal test – 990/10 and 990/4
IO16	945452	16 I/O TTL module test – 990/10 and 990/4
PROMPG	945454	PROM programmer test – 990/10 and 990/4
TTYEIA	945453	Full duplex TTY/EIA interface module test – 990/10 and 990/4
CARDRD	945449	Model 804 card reader test – 990/10 and 990/4
CRT913	945450	913 CRT diagnostic – 990/10 and 990/4
LPTEST	945448	990 line printer diagnostic – 990/10 and 990/4
TILCOM	945458	TILINE coupler logic test synchronous and asynchronous communication interface test – CRU 990/10 and 990/4
DAADC	945438	D to A + A to D converter test – 990/10 and 990/4
TINET	945444	TINET test – 990/10 and 990/4

Loading a Diagnostic Into the 990. The procedure for loading a diagnostic into the computer is as follows:

1. Open the transport door on either transport and install the cassette. Then shut the transport door.

2. If the cassette PLAYBACK light for the selected transport is not lit (figure 4-3, reference 5), press the PLAYBACK switch (figure 4-3, reference 6).

3. Set the POWER and ONLINE switches to ON and ONLINE positions respectively (figure 4-3, references 9 and 7).

4. Set the KEYBOARD, PLAYBACK and PRINTER switches (figure 4-3, references 10, 11, and 12) to the LINE position. Set RECORD switch to OFF.

5. Press the REWIND switch for the selected transport (figure 4-3, reference 1). Wait for the END LED (reference 4) to light.

6. Press the LOAD/FF switch (reference 2). Wait for the READY LED (reference 3) to light.

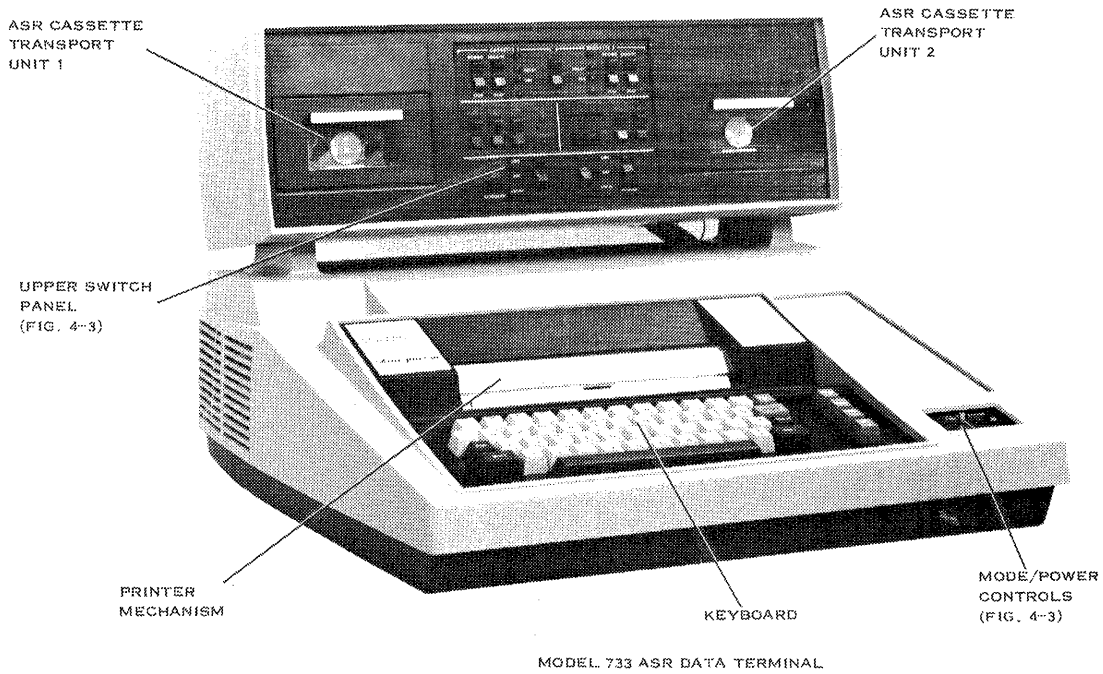


Figure 4-2. 733 ASR Data Terminal Controls and Indicators

7. Set the key switch on the programmer panel on the hot mockup to the UNLOCK position. If the RUN LED is lit, press the HALT/SIE switch. Ensure that the RUN LED extinguishes.

8. Press the LOAD switch on the programmer panel. The cassette tape should begin moving in short jerky motions.

   Also, the PLAYBACK CONTROL ON indicator should light (figure 4-3, reference 14).

Generally, the diagnostic program will begin execution immediately after completion of the load operation which takes anywhere from a minute to several minutes depending on the diagnostic. The diagnostic then prints out the diagnostic heading and prints the test results of each subtest. During this time, the printout can be manually inhibited by setting the PRINTER switch on the 733 to the LINE position.

4.3.1.3 Programmer Panel. The programmer panel controls and indicators are shown in figure 4-4 and listed and described in table 4-3. Basically, the panel functions in one of two modes:

- Run mode
- Halt mode

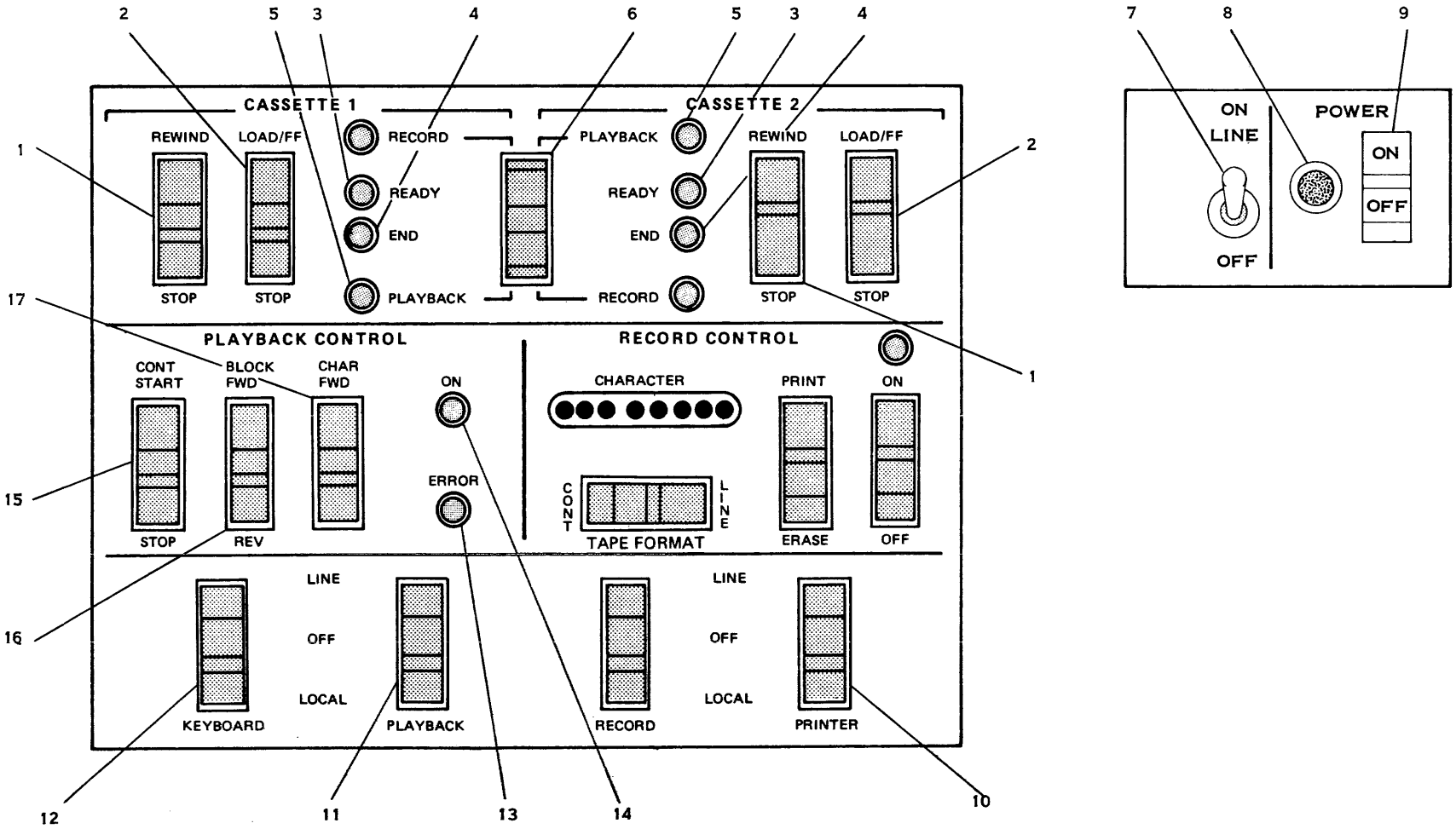


Figure 4-3. 733 Operating Panel Controls and Indicators

Table 4-2. 733 ASR Controls and Indicators

Reference Number	Control or Indicator	Function
	CASSETTE TRANSPORT CONTROLS AND INDICATORS	
1	REWIND/STOP switch	When pressed to the forward (REWIND) position, causes the tape to wind toward beginning of tape until clear leader is sensed or the REWIND/STOP switch is pressed to the STOP position.
2	LOAD FF/STOP switch	After rewinding to tape beginning, the program is read into the computer by pressing the LOAD FF switch. The tape then moves forward to the beginning of the tape marker and stops. Pressing the switch again causes the tape transport to go into the fast forward mode to the end of the tape or until the same switch is pressed to the STOP position.
3	READY indicator	Lights when the cassette has been positioned to the beginning of tape and is ready for playback.
4	END indicator	Lights when the clear leader is sensed at either the beginning or end of the tape.
5	PLAYBACK indicator	Lights to indicate which cassette is in the playback mode. The other cassette is placed in the record mode.
6	RECORD/PLAYBACK switch	Selects which cassette is in the playback mode. The other cassette is switched to the record mode.
	TERMINAL POWER AND ONLINE/OFFLINE CONTROL	
7	ONLINE/OFF switch	When set to the ONLINE position, the data terminal is permitted to communicate with the computer. In the OFF position, the terminal is electrically disconnected from the computer.
8	POWER indicator	Lights when the POWER switch is set to the ON position and ac power is present.
9	POWER ON/OFF switch	Controls ac power to the terminal.
	KEYBOARD/PRINTER LOCAL/LINE CONTROLS	
10	PRINTER LINE/OFF/LOCAL switch	Permits the printer portion of the terminal to be disabled (OFF), set up for LOCAL operation or tied to the computer. Normally this switch is set to the LINE position.
11	PLAYBACK/LINE/OFF/LOCAL switch	Used to control the playback portion of the terminal. In the OFF position, cassette playback is disabled In the LOCAL position, a cassette may be copied but the output is disabled from the computer interface. In the LINE position, the cassette playback is linked to the computer.
12	KEYBOARD LINE/OFF/LOCAL switch	Permits keyboard to be operated in the local mode, disabled or placed under computer control (LINE position).

Table 4-2. 733 ASR Controls and Indicators (Continued)

Reference Number	Control or Indicator	Function
	PLAYBACK CONTROL	
13	ERROR indicator	Lights when a missing flux reversal is detected on the tape during a playback operation.
14	ON indicator	Lights when playback control is operational (tape is being read under control of the 990 or started manually through use of CONT START/STOP switch).
15	CONT START/STOP switch	Momentarily pressing this switch causes the tape cassette designated by the PLAYBACK light in the top row of switches/indicators to begin a continuous playback operation. The tape halts when the clear leader is sensed or when the same switch is momentarily set to STOP position.
16	BLOCK FWD/REV switch	Momentarily pressing the BLOCK FWD switch causes the next block of data on tape to be read (or the remainder of the block if the read was previously halted in the middle of a read operation). Momentarily pressing the switch in the REV position causes the tape to back up one block and halt.
17	CHAR FWD switch	Momentarily pressing CHAR FWD switch permits one character at a time to be read from tape.

NOTE

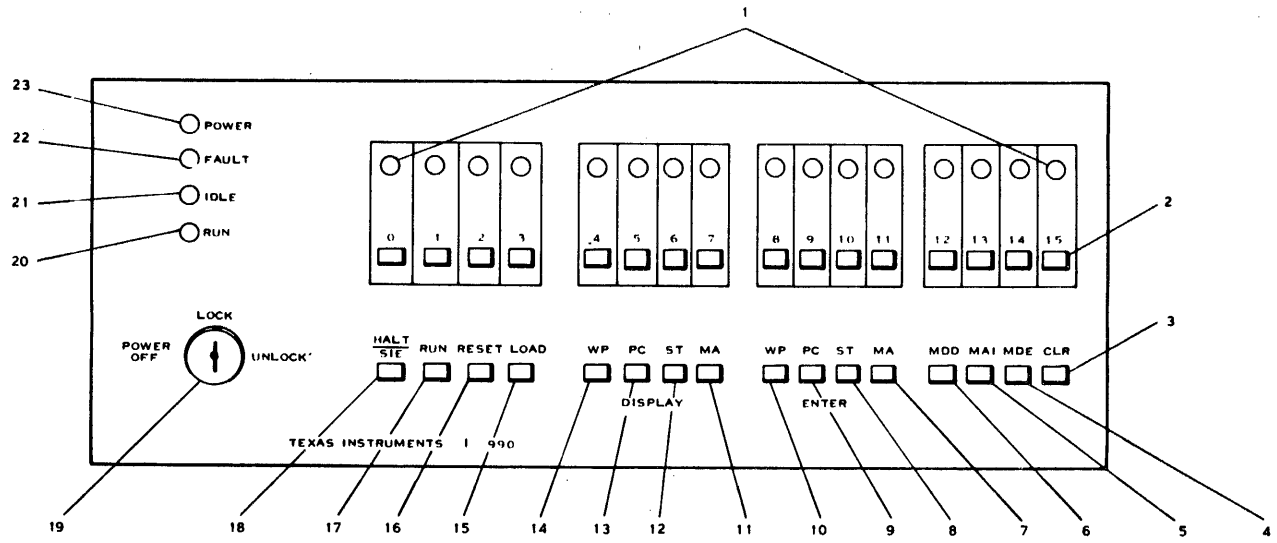
All remaining controls and indicators on the 733 ASR data terminal are not normally used in reading diagnostic tapes into the computer during maintenance operations. If the terminal is being used to duplicate or build new diagnostic tapes, refer to the *Silent 700 Model 733 ASR/KSR Operating Instructions Manual.*

Run Mode. When power is initially applied to the computer, the system comes up in the Run mode which locks out the programmer controls.

In this mode of operation, the RUN LED and all DATA DISPLAY LEDs on the panel light and remain lit.

Halt Mode. In order to set the programmer panel to the Halt mode, the key must be inserted in the key switch and the switch rotated to the UNLOCK position. At this time, pressing the HALT/SIE switch halts the computer and activates the controls on the programmer panel. The panel may be returned to the RUN mode by pressing the RUN switch.

4.3.2 990 POWER SUPPLY TEST SET. The 990 power supply test set operating controls and indicators are shown in figure 4-5.



(B)133312

Figure 4-4. 990 Programmer Panel Controls and Indicators

Table 4-3. Programmer Panel Controls and Indicators

Reference Number	Control or Indicator	Function
1	DATA LEDs	In the RUN mode of operation, all DATA LEDs light except when the computer halts. At this point, the contents of the CPU's program counter is displayed. A lit LED denotes a logic 1, an extinguished indicator denotes logic 0. The LSB is displayed on the far right of the LEDs. In the HALT mode, the LEDs display a computer register contents, memory contents or a value entered into computer memory via the data entry switches depending on which switches are pressed (see reference 5, 7, 9, 11, 13, 15).
2	DATA entry switches	Used in conjunction with the ENTRY switches on the panel to enter data and addresses into selected computer registers and memory locations (active only when the panel is in the HALT mode of operation). In the HALT mode, the data LED located immediately above each data entry switch lights as each switch is pressed. The value indicated by the DATA LEDs is then stored in the register or memory address selected by the entry switches.
3	CLR switch	When pressed, this switch clears the DATA LED displays.
4	MDE switch	This switch is pressed to transfer a value displayed on the DATA LEDs to the memory location defined by the contents of the memory address (MA) register in the computer.
5	MAI switch	The memory address increment (MAI) switch is pressed to increment the value stored in the CPU's memory address register by a value of 2.
6	MDD switch	When pressed, this switch causes the contents of the memory location defined by the contents of the memory address register to be displayed on the DATA DISPLAY LEDs.
7	ENTER MA switch	When pressed, this switch causes the value displayed by the DATA LEDs to be entered into the computer's memory address register.
8	ENTER ST switch	When pressed, the value displayed on the DATA LEDs is entered into the computer's status register.
9	ENTER PC	When pressed, the value displayed on the DATA LEDs is loaded into the computer's program counter.
10	ENTER WP	When pressed, the value displayed on the DATA LEDs is loaded into the computer's workspace pointer register.
11	DISPLAY MA	When pressed, the value stored in the computer's memory address register is displayed on the DATA LEDs.
12	DISPLAY ST	When pressed, the contents of the computer's status register is displayed on the DATA LEDs.
13	DISPLAY PC	When pressed, the contents of the computer's program counter is displayed on the DATA LEDs.
14	DISPLAY WP	When pressed, the contents of the computer's workspace pointer register is displayed on the DATA LEDs.

Table 4-3. Programmer Panel Controls and Indicators (Continued)

Reference Number	Control or Indicator	Function
15	LOAD switch	When the panel is in the HALT mode, pressing this switch causes the computer to trap to the ROM loader starting address.
16	RESET switch	Pressing the RST switch results in an IORESET– pulse being generated which resets all units in the system.
17	RUN switch	When the computer is halted (programmer panel is active), pressing the RUN switch returns the computer to the RUN mode of operation and deactivates the panel.
18	HALT/SIE switch	When the computer is in the RUN mode (RUN LED is lit), pressing the HALT/SIE switch causes the computer to halt and begin processing the front panel software if the key switch is set to the UNLOCK position. Pressing the switch when the computer is not in the RUN mode causes the computer to execute a single instruction at the present PC (program counter) address. The contents of the program counter are incremented by two and displayed on the DATA LEDs.
19	Key switch	The key switch (OFF/LOCK/UNLOCK) switch prevents unauthorized computer turnon or program intervention. In order to apply ac power to the chassis, the key must be inserted into the switch and the switch set to the LOCK position. At this point, power is applied to the computer, but the programmer panel is locked out. In the UNLOCK position, the computer may be halted by pressing the HALT/SIE switch. The key may be removed from the switch in either the OFF or LOCK position.
20	RUN LED	The RUN LED lights when a low-active RUN– signal is generated by the computer indicating the computer is in the RUN mode. When this LED is lit, all switches on the panel except the HALT/SIE switch are disabled and the DATA LEDs are driven under program control. When the RUN LED is extinguished, the panel controls are active.
21	IDLE LED	Lights when the computer is executing an idle instruction (indication of computer inactivity for most interrupt driven software).
22	FAULT LED	The FAULT LED lights when the computer has detected a diagnostic test failure.
23	POWER LED	Lights when power is applied to the unit (key switch on the panel set to the LOCK or UNLOCK position.

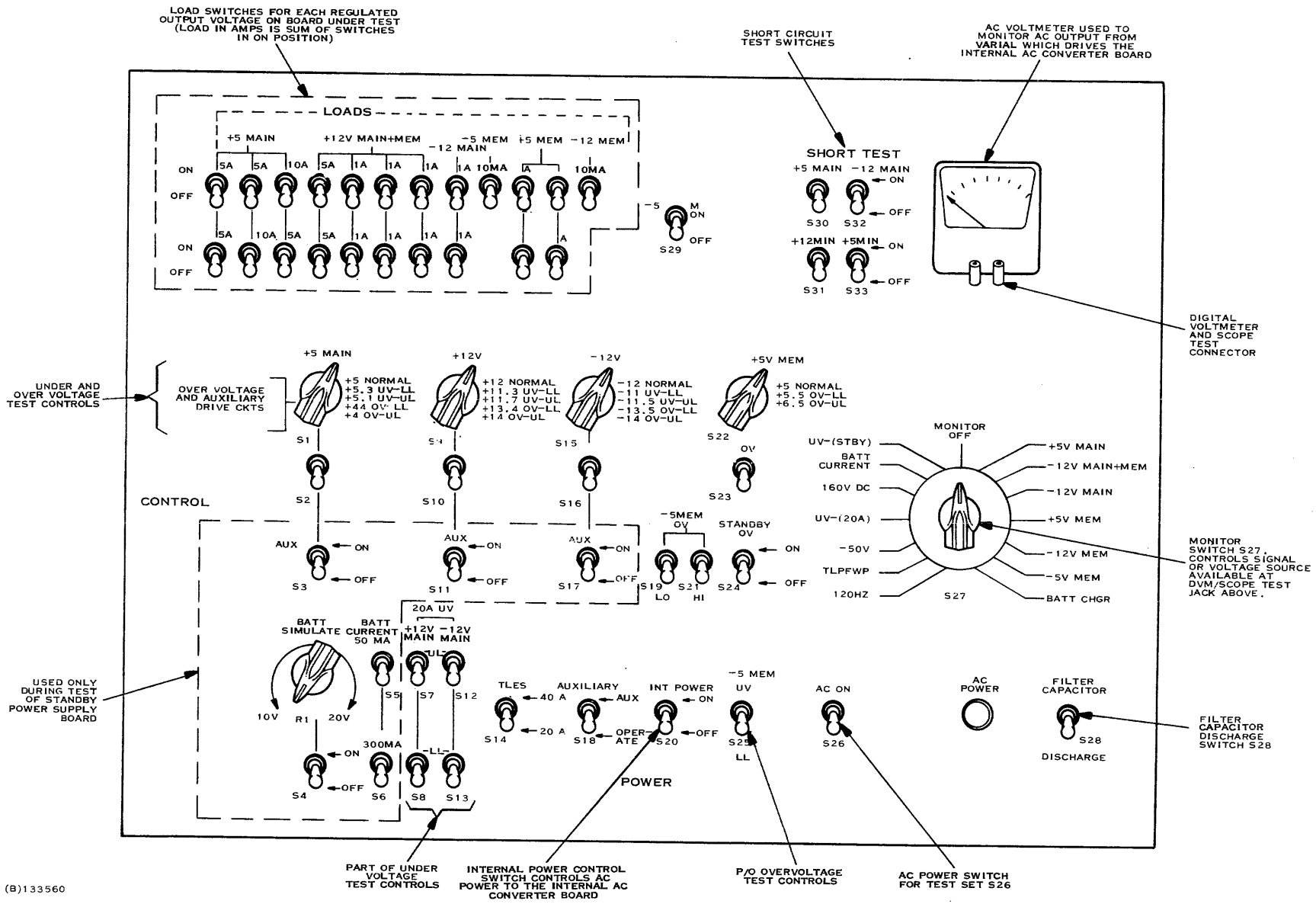


Figure 4-5. 990 Power Supply Test Set Controls and Indicators

SECTION V

CORRECTIVE MAINTENANCE

5.1 GENERAL

This section provides board, cable and other subassembly repair procedures required to correct circuit malfunctions on 990 assemblies and subassemblies. The workstation and the associated tools and materials required to perform depot-level corrective maintenance are described in Section II of this manual.

5.2 BOARD REPAIR PROCEDURES

The board repair procedures include repair of etch conductors and removal and replacement of defective components. These procedures are described in the following paragraphs.

5.2.1 SOLDERED-IN COMPONENT REMOVAL AND REPLACEMENT. Soldered-in component removal and replacement requires the use of a heated tip vacuum solder system, a padded bench top vise used for holding boards while removing and replacing components and a 30 watt soldering iron used primarily for installing new components.

5.2.1.1 Preparation of Heated Tip Solder Vacuum System. All soldered in multilead components such as ICs and connectors are removed from the printed circuit boards through the use of the heated tip solder vacuum system. Basically, this system consists of a hollow tip soldering iron which melts the solder from around the leads of the defective component, and a foot actuated vacuum system which pulls the molten solder through the hollow tip into a solder reservoir. Once the solder is removed, the component is easily detached from the board. Prior to use of the heated tip vacuum system, the following initial preparation steps should be performed:

1. Clean the solder trap using the instructions supplied by the system manufacturer. Also, ensure that the vacuum section is clear of solder or other residue (the unit should be thoroughly cleaned at the end of each workday according to the manufacturer's instructions).

2. Install a clean heat tip on the system. Then apply 115 vac to the system and allow 10 minutes for the tip temperature to stabilize.

3. Tin the heated tip with 63/37 rosin core solder.

NOTE

The heated tip must be kept clean and well tinned at all times to permit rapid solder flow during component removal procedures.

4. Check the operation of the vacuum section by flowing a bead of molten solder over the hole in the tip and actuating the vacuum switch. If the system is functioning properly, the molten solder will be pulled through the tip into the solder reservoir. If not, refer to the operator maintenance procedures supplied by the equipment manufacturer.

5. Once the system is satisfactorily pulling molten solder from the tip into the reservoir, the unit is ready for normal operation.

5.2.1.2 **Component Removal Procedure.** The following procedure should be followed in removing soldered components from printed circuit boards:

1. Wipe the heated tip of the solder vacuum system using a wet sponge and ensure that the tip is well tinned.

CAUTION

Do not permit the heated tip of the vacuum solder system to touch any portion of the board except the immediate area of the component being removed. Failure to observe this precaution may result in damage to board etch through accidental overheating. Always return the unit to cradle when the unit is not being used for component removal.

2. Identify the leads of the component to be removed. Then carefully position the hollow tip over the first lead (if the lead is not bent) as shown in figure 5-1. In the event the lead is bent, place the heated tip immediately adjacent to the lead. When the solder around the lead is molten, move the lead (using tweezers from the component side of the board) in a slight circular motion and actuate the solder vacuum system. Momentarily touch the etch pad (straight leads) or the board surface (adjacent to the lead for bent pins) approximately 2 seconds after the vacuum system has been actuated to form a vacuum seal to pull the solder out of the immediate area of the leads. In the case of a bent lead, straighten the lead after removing the solder adjacent to the lead. Then place the hollow tip over the lead and repeat step 2.

NOTE

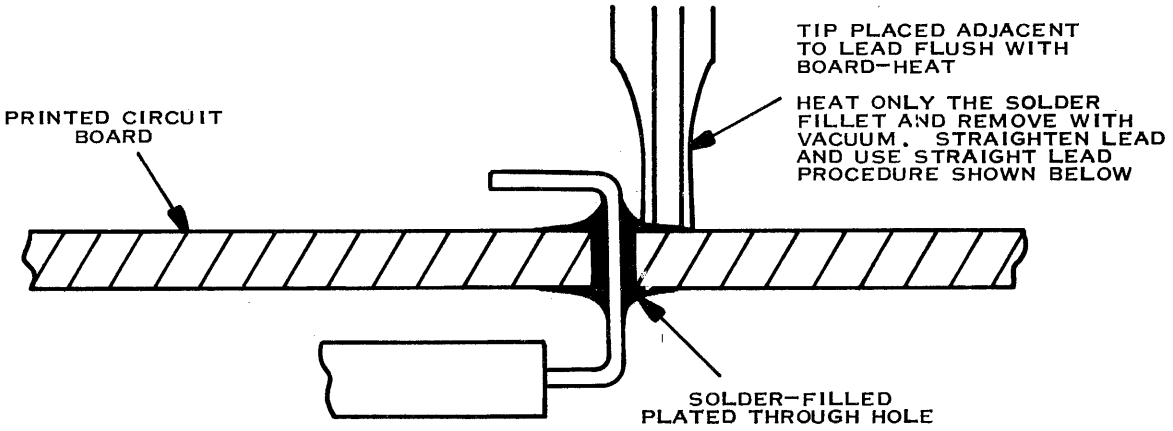
If a component lead does not contain a good solder bead, sufficient solder required to form a vacuum seal and to transfer heat to the other side of the board may not be present. In this case, apply additional solder (63/37, .30 diameter rosin core) to the lead(s) with a 30 watt soldering iron prior to using the solder vacuum system.

3. Repeat the solder removal procedure described in step 2 for each of the leads on the defective component.

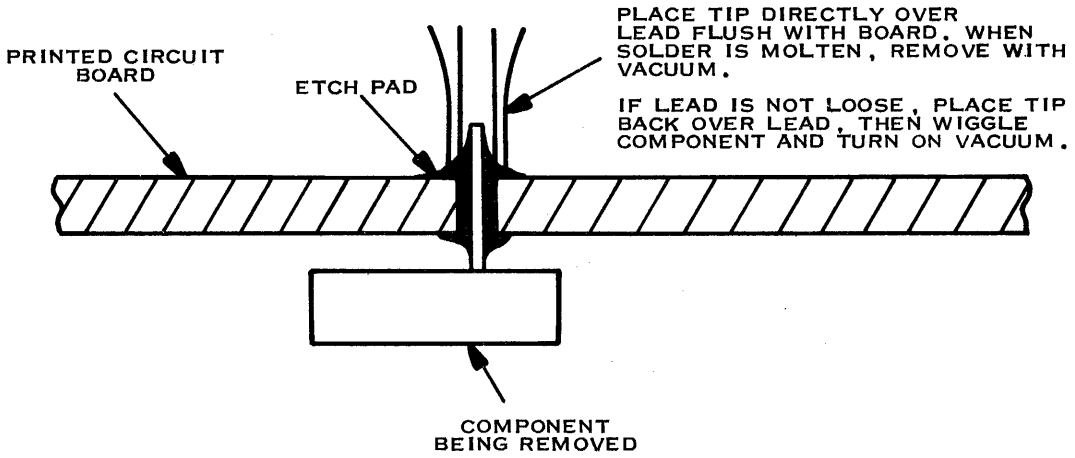
4. Using tweezers, carefully lift the defective component from the printed circuit board.

CAUTION

If any of the component leads are still soldered to the board, do not use force to break the leads loose as this practice may result in pulling the etch conductor away from the board. Typically, any pin still connected at this time is tied to the board's ground plane and will require additional work prior to removal.



REMOVAL OF BENT–LEAD COMPONENTS



(A)133314

REMOVAL OF STRAIGHT LEAD COMPONENTS

Figure 5-1. Component Removal, Simplified Diagram

5. If any lead of the component is still attached, place the board in a padded bench top vise to permit working on both sides of the board at the same time. Heat the component side of the component with a 30 watt iron and simultaneously heat the circuit side of the board with the heated tip solder vacuum system. When the solder melts, actuate the vacuum system and then momentarily press the hollow tip flush against the pad to create a vacuum seal and draw out the solder. The component may then be removed from the board.

6. Immediately after removing the defective component, clean the repair area using an acid brush dipped in isopropyl alcohol or other approved solvent such as denatured ethyl alcohol or Alpha 563 cleaning solvent.

5.2.1.3 Component Installation Procedure. After removing the defective component, a new component is installed on the printed circuit board using the following procedure.

1. Carefully inspect the plated through holes and pads in the area where the new component is being installed. Clean the areas thoroughly using an acid brush and isopropyl alcohol. Then clamp the board in the padded vise exercising care to avoid damage to the components on the board.

2. Preheat a 30 watt soldering iron. Then clean the tip using a wet sponge and retin the tip using 63/37 rosin core solder (.30 diameter).

3. Insert the new component into the existing plated through holes and sparingly apply liquid rosin base flux (using a hypodermic syringe applicator) to the component leads and the plated through holes and pads.

CAUTION

Delicate components such as LEDs and transistors should be protected against heat damage by temporarily installing a heat sink on the leads next to the body of the component prior to soldering the component in place.

4. Solder the component in place using 63/37 rosin core solder (.030 diameter) and a 30 watt soldering iron. Maintain a smooth fillet of solder around each lead. Then permit the solder to cool undisturbed to pervent cold solder joints.

5. Immediately remove any residual flux from the repaired area using an acid brush dipped in isopropyl alcohol.

6. Clip the component leads protruding from the circuit side of the board and inspect the repair using the lighted magnifying lens unit.

5.2.2 REMOVAL AND REPLACEMENT OF PLUG IN ICs. Many of the ICs on the 990/4 microcomputer board and memory extension board are plug in types which are installed in soldered-in IC sockets. These components may be removed and replaced at either the trouble-shooting station or the corrective maintenance station using a combination IC extractor/installer tool. Since the IC leads are slightly flared (see figure 5-2), a special tool must be used to compress these leads during removal and installation. Failure to use the proper tool can result in bent pins and improperly seated ICs which may not be apparent once the IC is down in the socket. Also, correct IC orientation must be observed when installing an IC (see figure 5-2).

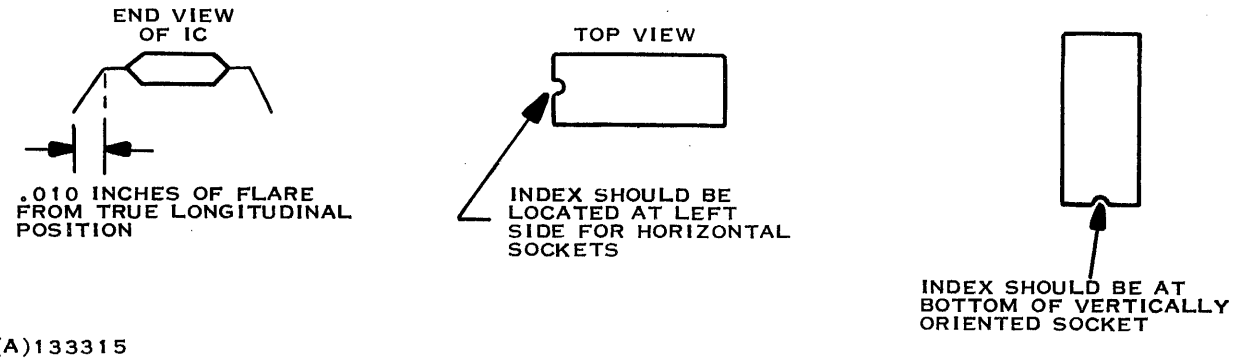


Figure 5-2. Removing and Installing Plug-In ICs

5.2.3 **REPAIRING DAMAGED ETCH CIRCUITS.** Broken, raised, or partially deteriorated etch circuits may be repaired using one of two repair procedures, depending on the length of the damaged etch. These two procedures are described in the following paragraphs.

5.2.3.1 **Repairing Small Breaks in Copper Etch.** If the length of the damaged etch on a printed circuit board is less than twice the width of the conductor, the following procedure may be used to repair the etch conductor.

1. Using an X-acto knife, trim back the jagged edges of the broken conductor or remove the raised portion of a damaged conductor.

2. Sand the conductor edges (approximately 1/4-inch on each side of the break) with 400A Durite paper (or equivalent).

3. Blow off any residue using compressed air and wipe area clean with a clean cloth dipped in isopropyl alcohol.

4. Cut a length of bus wire to overlap the break approximately 1/4-inch on each end. The wire gage for the bus wire is determined by the width of the conductor as follows:

Width	Gage
1/32	26
1/16	22
3/32	20
1/8	18

5. Sparingly apply rosin base flux to the sanded edges of the conductor and to the bus wire which is laid directly over the previous conductor path (see figure 5-3).

6. Solder the bus wire to the etch conductor using 63/37 rosin core solder and a 30 watt soldering iron. Maintain an unbroken fillet of solder along the junction of the bus wire and the etch conductor. Permit the solder to cool undisturbed.

7. Immediately after the solder has cooled, remove any residual flux using an acid brush dipped in alcohol. This completes the etch repair procedure.

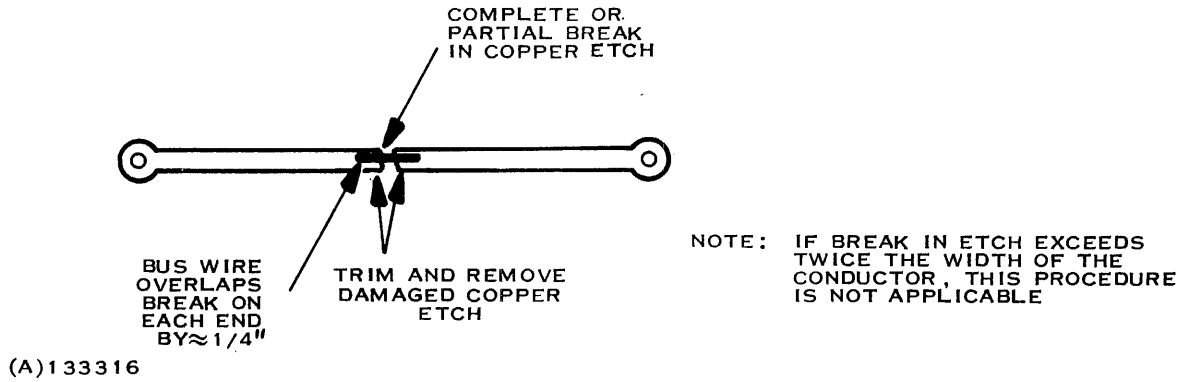


Figure 5-3. Repairing Small Breaks in Etch Conductors

5.2.3.2 **Repairing Large Breaks in Etch Circuitry.** If the length of damaged etch circuitry exceeds twice the width of the etch conductor, the following repair procedure should be used.

NOTE

The following procedure should be used only with two-sided boards which do not contain conflicting etch on the opposite side.

1. Cut back the copper conductor on either side of a broken or raised etch circuit using an X-acto knife. Carefully peel the damaged portion of the conductor from the printed circuit board.

2. Drill a #59 hole approximately 1/32-inch from each edge of the conductor as shown in figure 5-4(a).

3. Clean the copper conductor at least 3/8-inch on each side of the gap area using 400A Durite sand paper. Clean the area using compressed air and carefully wipe the etch conductors with a cotton swab or cloth saturated with isopropyl alcohol.

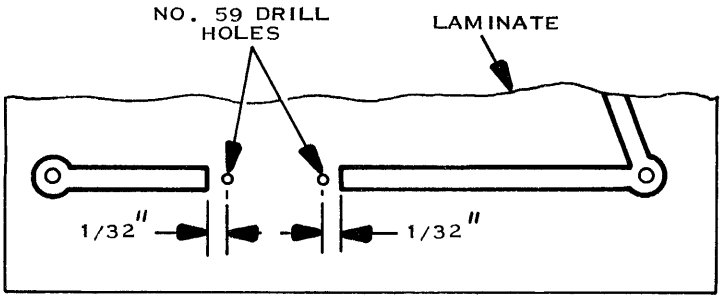
4. Tin the etch conductor ends using 63/37 rosin core solder and a 30 watt soldering iron.

CAUTION

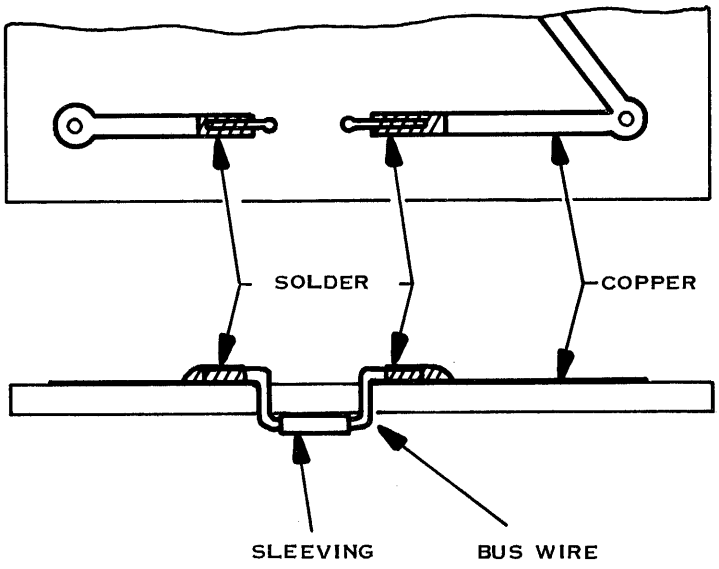
Avoid overheating the etch conductor as additional damage to the etch may result.

5. Select the proper gage of sleeved bus wire according to the width of the etch conductor and strip the sleeving such that the sleeving extends from hole to hole as shown in figure 5-4(b). The gage of bus wire is selected as follows:

Etch Conductor Width (inches)	Bus Wire Gage
1/32	26
1/16	22
3/32	20
1/8	18



(A) HOLE LOCATION DIAGRAM



(B)REPAIR PROCEDURE

(A)133317

Figure 5-4. Repairs to Printed Circuit Etch Where Break Exceeds Twice Width of Etch Conductor

6. Bend the stripped ends of the bus wire to protrude through the holes in the board on the circuit side and to overlay the ends of the damaged etch conductors (see figure 5-4).

7. Sparingly apply rosin flux to the bus wire ends and solder the bus wire to the etch using 63/37 rosin core solder and a 30 watt soldering iron. Ensure a smooth fillet of solder flows along the joint. Then permit the solder to cool undisturbed for a few seconds.

8. After the solder has cooled, clean the excess flux from the repaired area using an acid brush dipped in alcohol. This completes the etch repair procedure.

5.3 FLAT CABLE REPAIR PROCEDURES

The flat cables which are used to interconnect various components of the 990 system may be repaired using the following procedures. Generally speaking, the cable problems involve a loose or improperly mated connecter on one end of the cable. Carefully inspect the entire cable for physical signs of damage such as burned or cut surfaces or loose or damaged connectors. In the case of a loose connector, the cable is repaired by cutting the cable just behind the connector and installing a new connector using the following procedure.

1. Using the cable shear, carefully trim the cable as close to the defective connector as possible. The cut must be absolutely square (90 degrees ± 1 degree). Note the relationship of the old connector to the black strip along the cable and mount the new connector in the same relative position.

2. Using an X-acto knife, carefully trim the sides of the cable for a length of 1.75 inches to permit the cable to fit through the associated connector. (See figure 5-5.) Then strip the end of the cable for a distance of .75 inches using wire strippers modified with Polystrip universal wire strip blades.

3. Insert the prepared cable end between the cover and the strain relief of the new connector in accordance with either figure 5-6 or 5-7 depending on the orientation of the connector previously removed.

4. Remove the paper liner from the pressure sensitive adhesive of the cover. Fold the cable back 180 degrees aligning the ribs of the cable with the groves in the cover. With the cable end flush to the cover, press the cable firmly in the groves.

5. Place the subassembly in the locator plate (plate will vary depending on size of cable and connector being used – see manufacturer's specifications) with the retaining pins upward. Locate the connector body over the subassembly with the contacts pointing downward. The triangle marking pin number 1 should always be oriented with the black stripe of the cable (see figures 5-6 and 5-7).

6. Ensure that the cable end is flush with the cover and that the cable humps are within the cover grooves. Complete the assembly by lowering the arm of the assembly press.

7. Raise the handle to remove the assembly force allowing the weight of the handle to rest the platen on the assembly.

8. Pull the cable back to seat it in the cover. Raise the handle fully and remove the completed assembly which should resemble the assembly shown in figure 5-8.

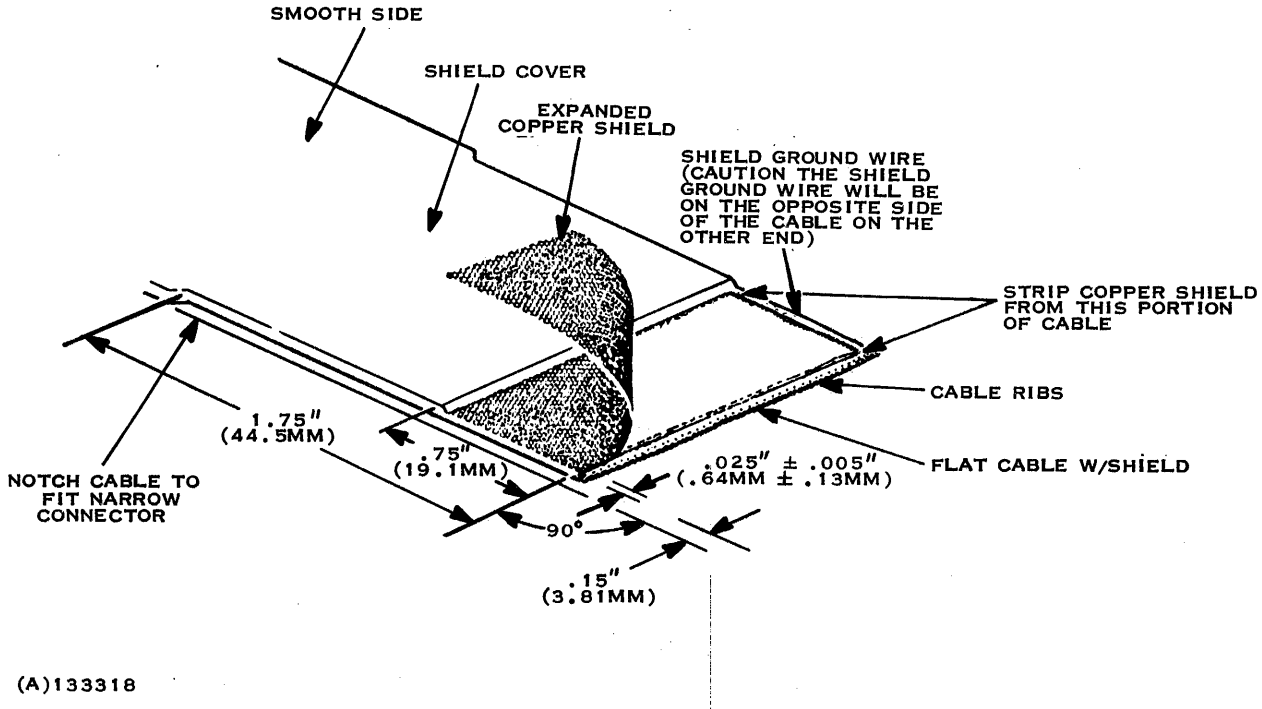
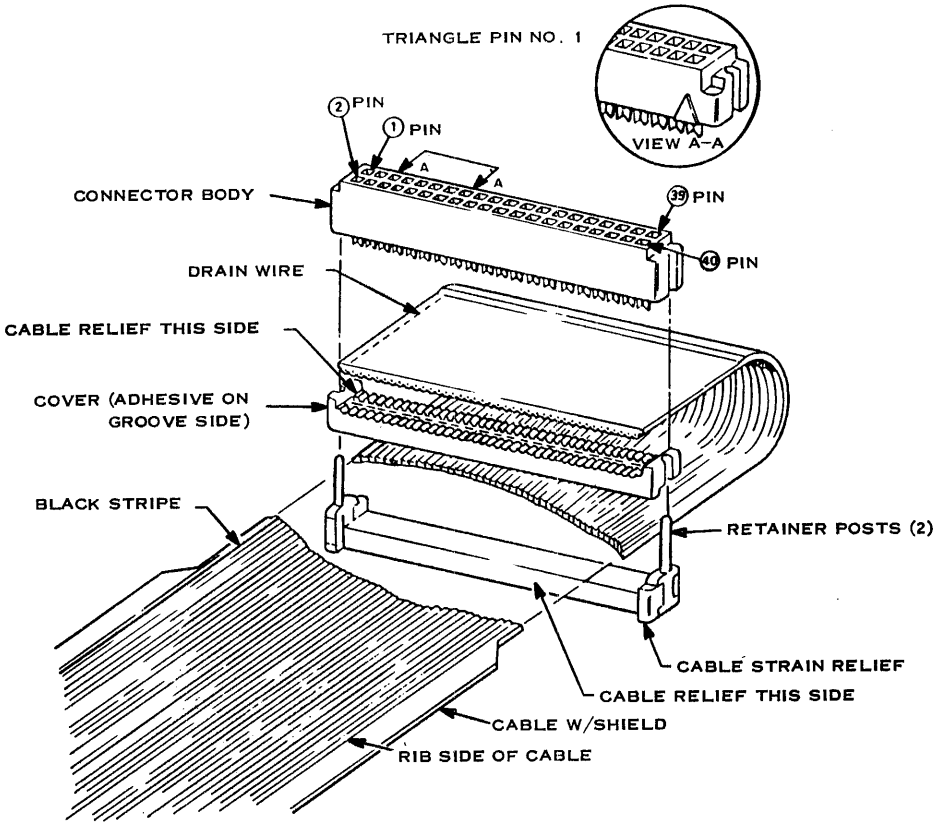
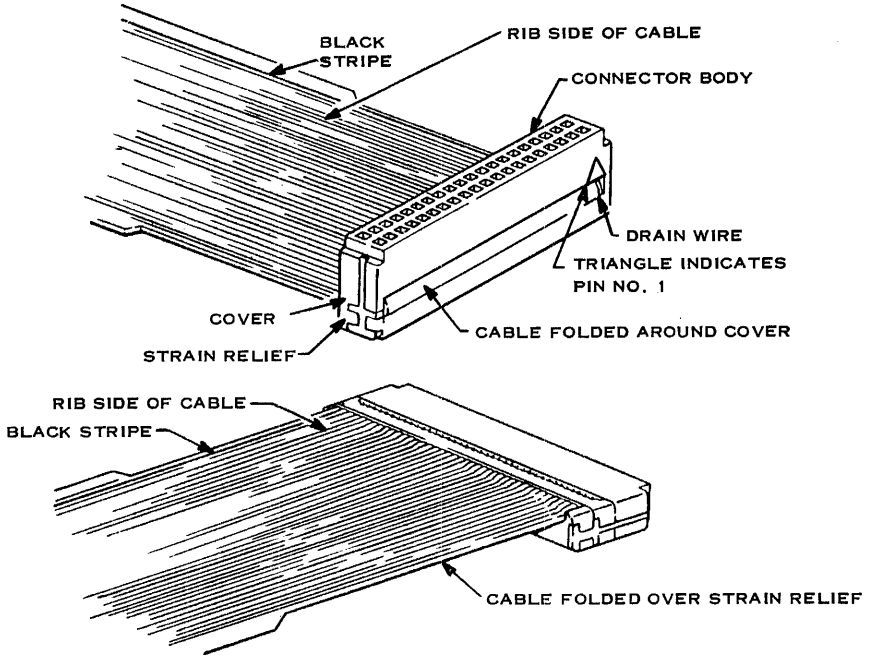


Figure 5-5. Flatcable Notching and Stripping Specifications



CABLE TO CONNECTOR INSTALLATION



(B)133320

FINISHED ASSEMBLY

Figure 5-6. Flatcable to Connector Installation Procedures

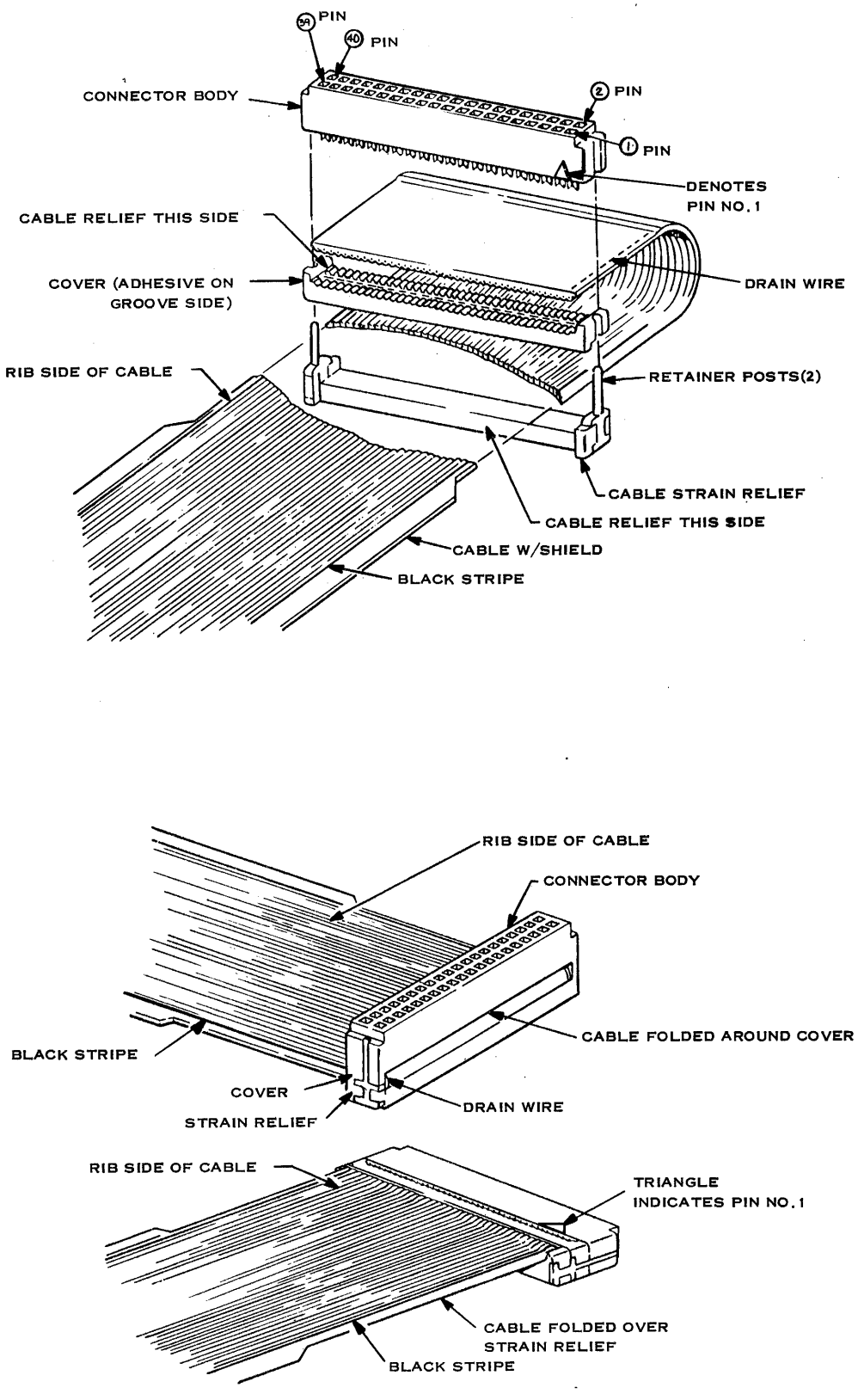


Figure 5-7. Opposite End of Cable Orientation, Simplified Diagram

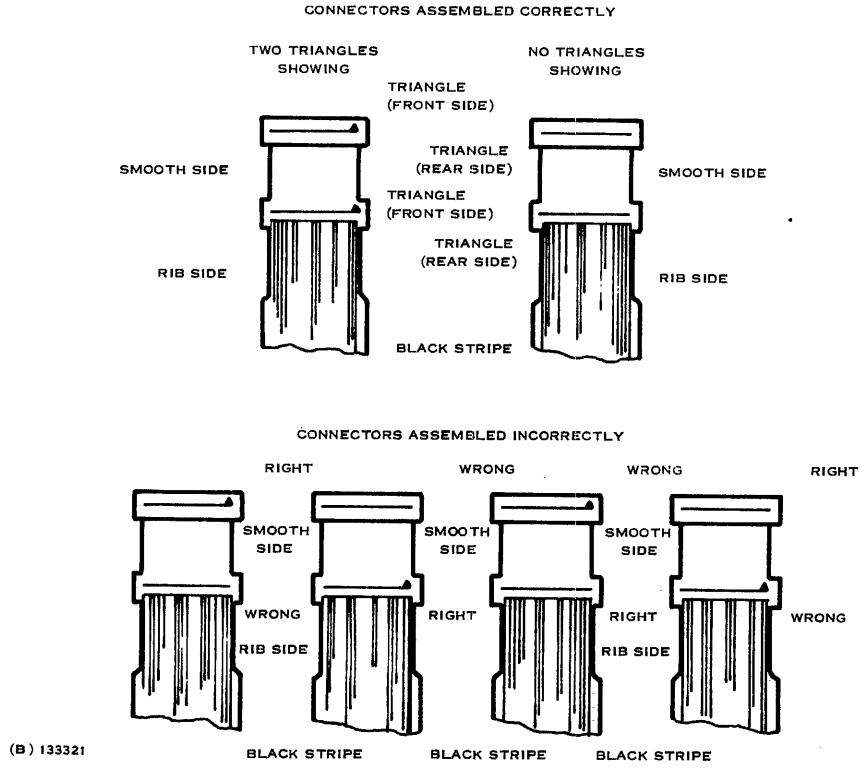


Figure 5-8. Examples of Correctly and Incorrectly Assembled Flatcable Connections

SECTION VI

CHASSIS TROUBLESHOOTING DATA

6.1 GENERAL

This section provides a general description of the 990 chassis components and contains wiring diagrams and other troubleshooting data required to perform depot-level maintenance on the chassis.

6.2 CHASSIS ORGANIZATION

Functionally, the chassis comprises the following:

- Ac power distribution circuits
- Dual cooling fans
- Backpanel connector board
- Interconnecting cable assemblies

A wiring diagram for the 6 slot chassis is shown in figure 6-1 and the wiring diagram for the 13 slot chassis is shown in figure 6-2. A parts location diagram is provided in figure 6-3.

6.2.1 AC POWER DISTRIBUTION CIRCUITS. As shown in figure 6-1, ac power to the chassis is routed through a 10 ampere, slo-blo fuse 1F1 and up to a microswitch 1A4S1 on the operator/programmer panel which is controlled by a cam on the rear of the key switch. The hot ac line is then routed through a line filter (1FL1) and over to terminal 1 of terminal strip 1TB1. For chassis which are used with 100 vac or 230 vac, an optional transformer 1T1 is installed between the line filter and the terminal strip.

NOTE

For installation instructions for the optional transformer, refer to the 990/4 Field Maintenance Manual.

The neutral ac line is routed through the line filter (and optional transformer if used) over to terminal 2 on the terminal strip. The two cooling fans and the input cable to the ac power converter board are wired across terminals 1 and 2 of the terminal strip. Also an over-voltage protector (1C2) which is rated at 230 V, ± 15 percent is tied across the same two terminals to protect the system against lightning or other surge voltages on the ac lines.

The optional standby circuit connects two batteries in series. The positive terminal of battery number 2 is connected to terminal 5 on the terminal strip through a protective fuse (1F2) and the battery ON/OFF switch 1S1. Terminal number 4 on the terminal strip accomplishes the series connection of batteries 1 and 2 and the negative terminal of battery 1 is connected to terminal 3. The battery voltage available across terminals 5 and 3 is wired to the P2 inputs on the standby power supply board 1A6.

6.2.2 **990 CHASSIS BACKPANEL BOARD.** A majority of the electrical interconnections between the circuit boards in the 990 chassis are accomplished through the etch wiring on the backpanel board (figure 6-4). This board also contains pull-up resistors for the various 990/4 microcomputer board interface lines and contains provisions for wiring the interrupts from each half-board slot in the chassis to interrupt levels 1 through 7. Interrupt levels 8 through 15 are not used in the 990/4 system but are included on the jumper plugs since the same chassis is used in the 990/10 system.

In an expansion chassis, the interrupts from the half-board slots are connected to interrupt levels 0 through 15 which are scanned by the interrupt scanner logic on the expansion chassis's CRU buffer board located in board slot 1. For both the main chassis and the expansion chassis, the interrupt wiring is accomplished through interrupt plugs which plug into J2 and J3 on the associated backpanel board.

NOTE

For a detailed explanation of interrupt wiring, refer to the installation section in the 990/4 Hardware Reference Manual.

6.2.3 **CHASSIS WIRING HARNESS.** Most of the interconnections between the ac power converter board (1A2), main power supply board (1A3), optional standby power supply board (1A6), front panel switch 1A4S1 and the backpanel board (1A1) is accomplished via the chassis wiring harness. In addition, the ground, chassis ground, and +5 MAIN connections between the main power supply board and the backpanel board are implemented by the mounting hardware on the backpanel (pads on the power supply board are bolted to pads on the backpanel).

6.2.3.1 **Standby Jumper Plug.** If the optional standby power supply board is not installed in the chassis, a jumper plug (Part Number 946739) must be installed on 1A3P3 which substitutes the main power supply voltages for the memory voltages normally developed on the standby power supply board. The standby jumper plug is wired as shown in figure 6-5.

6.3 CHASSIS TROUBLESHOOTING PROCEDURES

As standard procedure, all chassis which are returned for depot maintenance should be equipped with new backpanel boards due to the probability of connector problems. All logic and power supply boards should also be removed from the chassis and individually tested in accordance with the information provided in the subsequent sections of this manual (and other depot-level manuals for board types not covered in this manual).

The chassis is then checked out using the procedures in table 6-1. Fault isolation procedures for the chassis are provided in both tables 6-1 and 6-2.

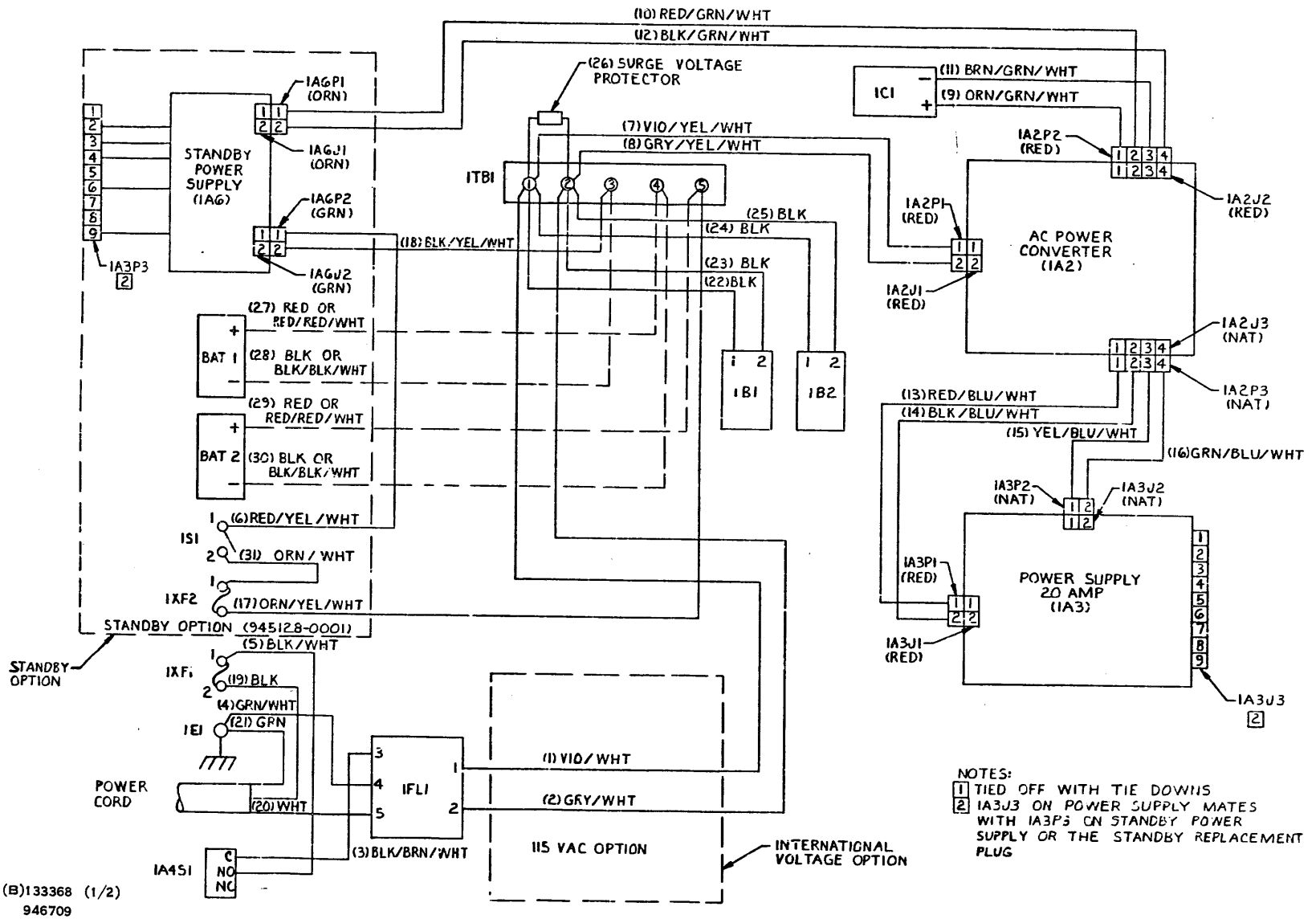
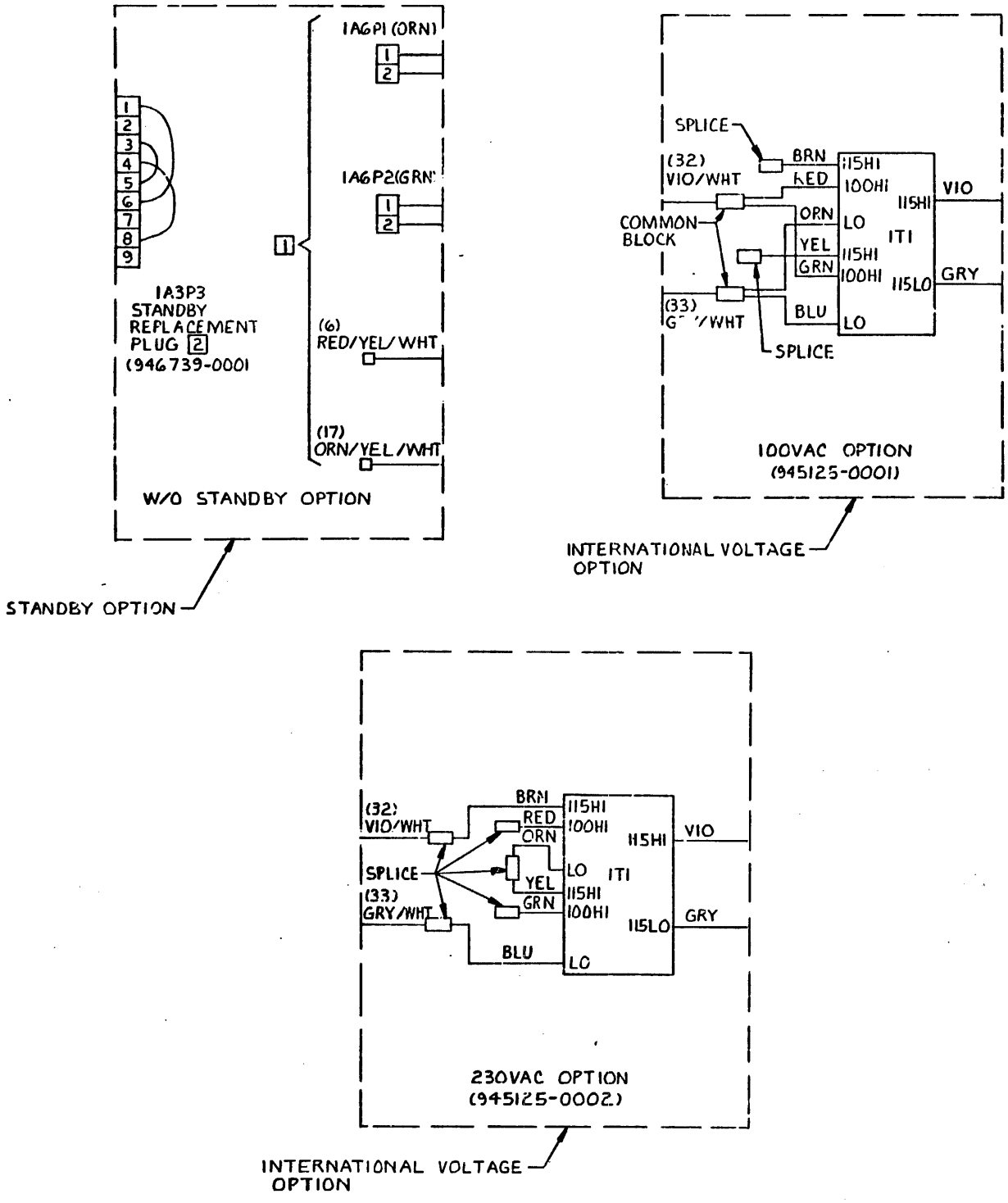


Figure 6-1. 990 Chassis Wiring Diagram (6 slot Chassis)(Sheet 1 of 2)



(B)133368 (2/2)
946709

Figure 6-1. 990 Chassis Wiring Diagram (6 slot Chassis) (Sheet 2 of 2)

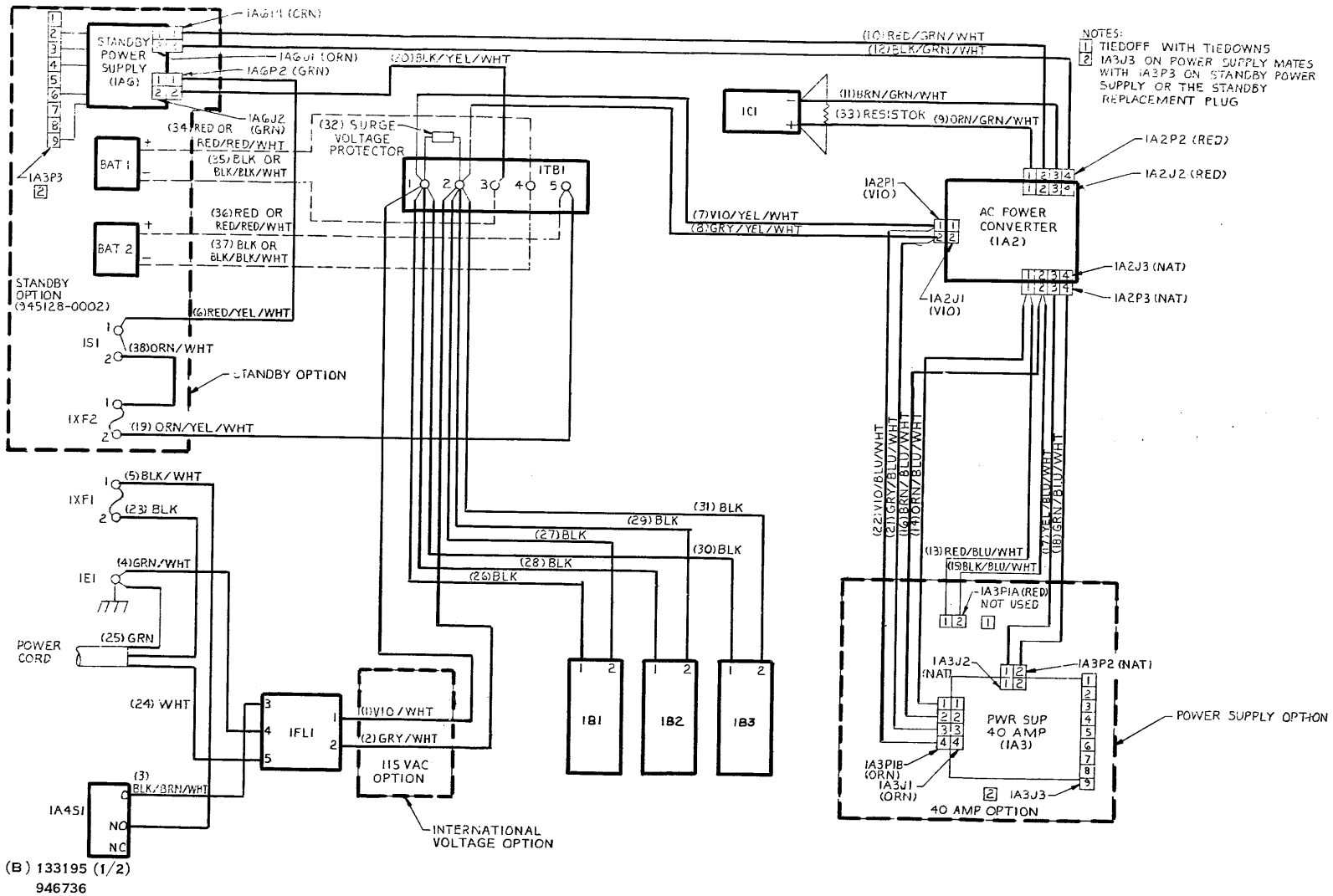
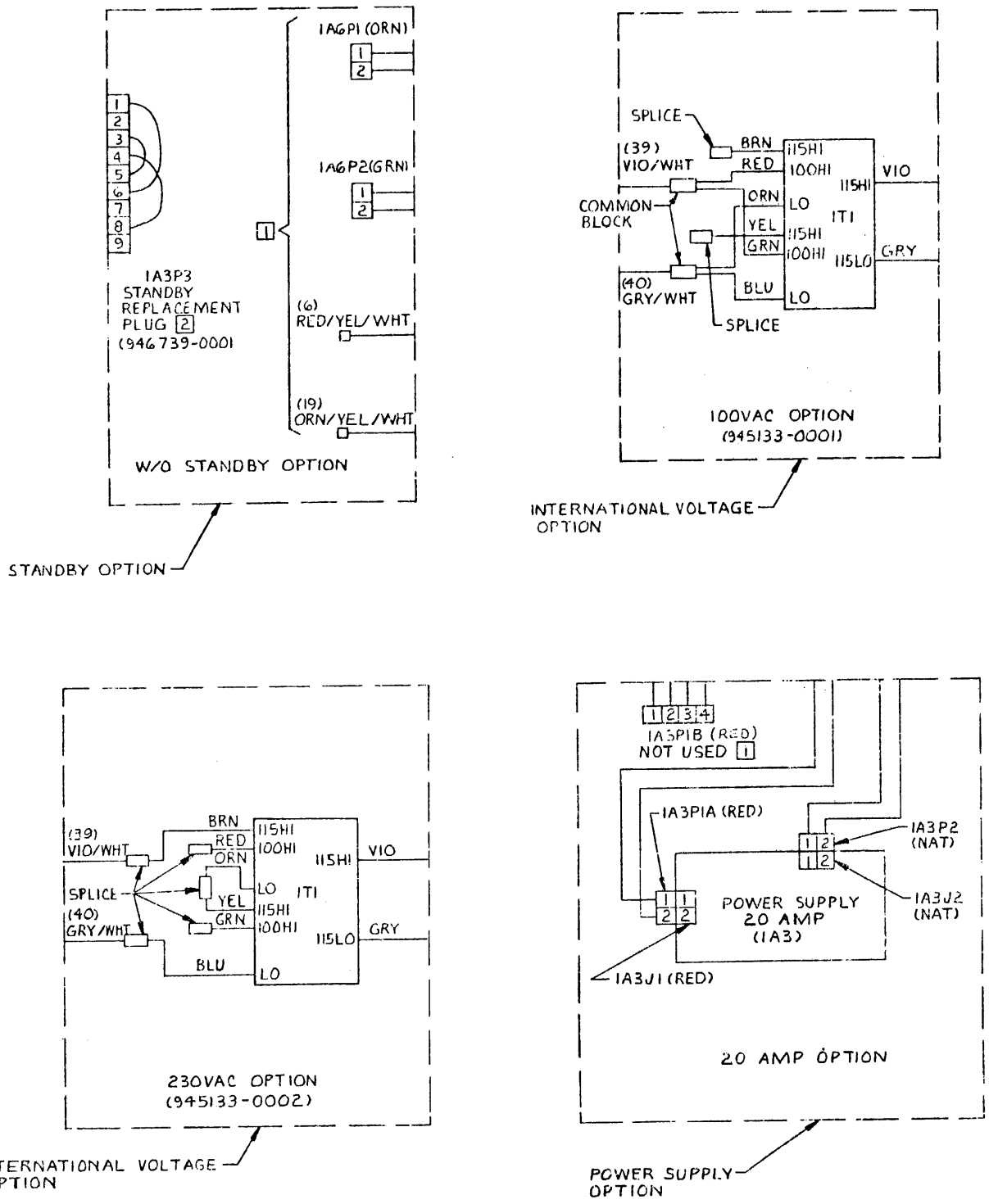
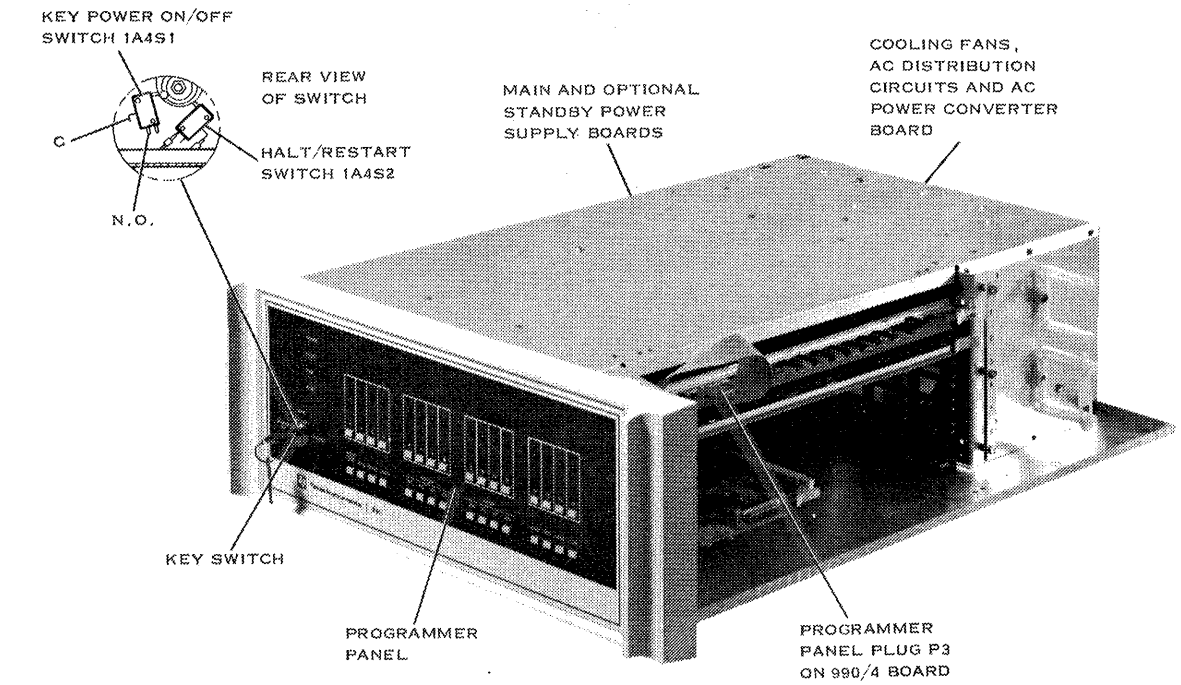


Figure 6-2. 990 Chassis Wiring Diagram (13 slot Chassis)(Sheet 1 of 2)



(B) 133195 (2/2)
946736

Figure 6-2. 990 Chassis Wiring Diagram (13 slot Chassis) (Sheet 2 of 2)



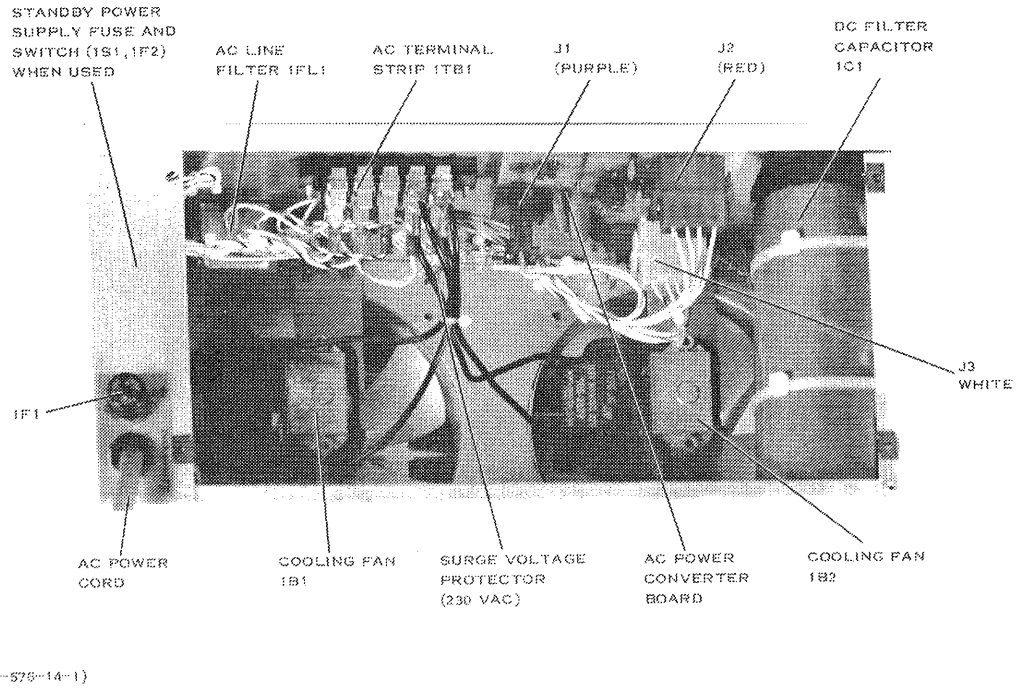


Figure 6-3. 990 Chassis Parts Location Diagram

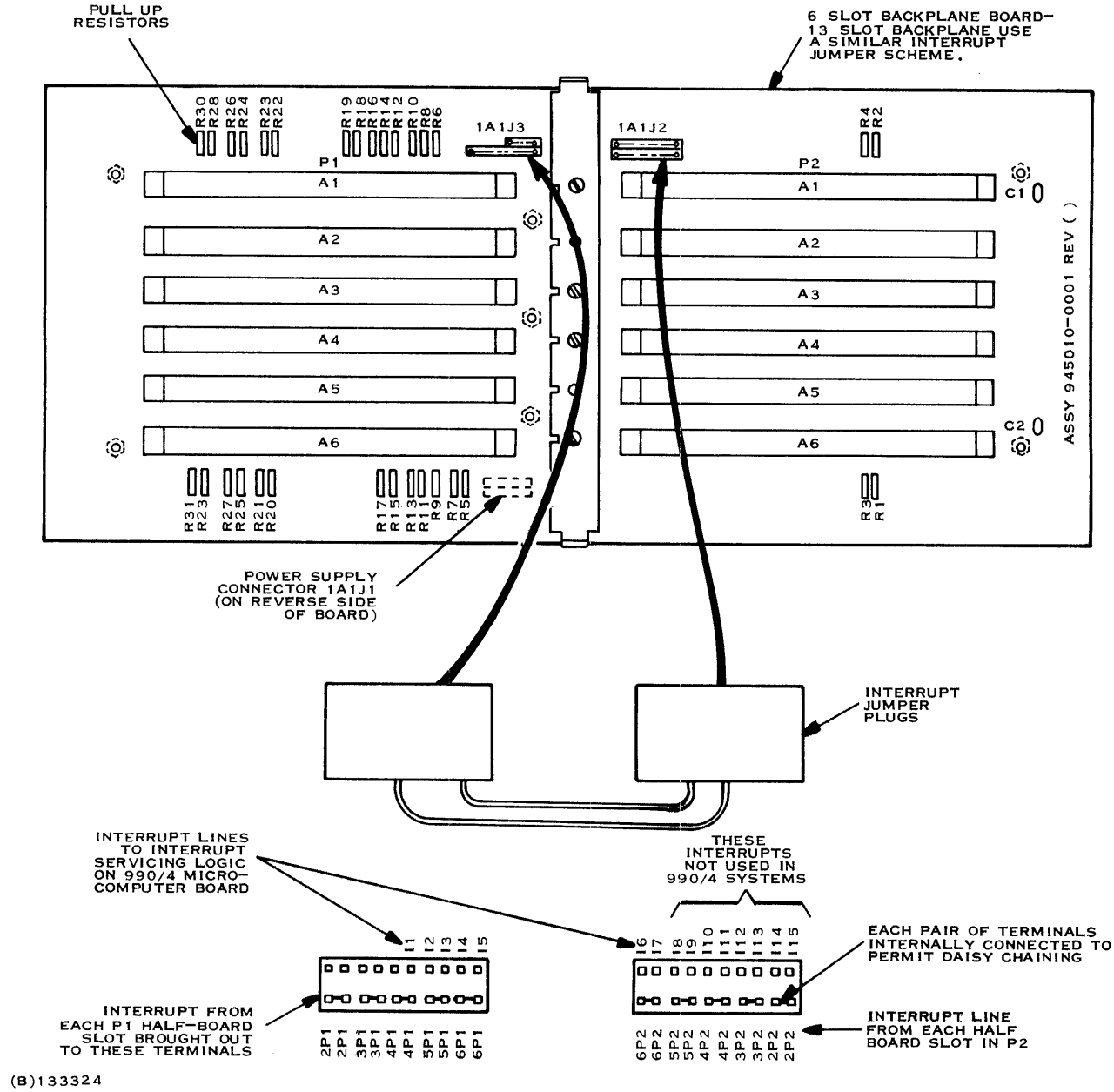


Figure 6-4. Typical Interrupt Jumper Scheme

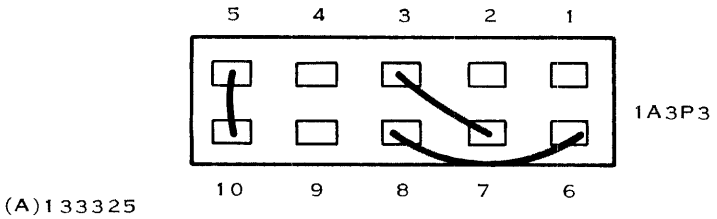


Figure 6-5. Standby Jumper Plug (Required When not Using Standard Supply)

Table 6-1. Chassis Checkout Procedure (Continued)

Step	Procedure	Normal Indication	If Abnormal
15	Using digital voltmeter, measure the dc voltage between pin 1 of backplane connector 1A1A1P2 and the following pins on the same connector (slot 1):		Replace power supply boards.
	P1 Pins / *P2 Pins* / *Signal*		
	3, 4, 77, 78 / 3, 4, 77, 78 / +5 MAIN	+5 vdc, ±3%	
	39, 40 / 39, 40 / +12 MAIN	+12 vdc, ±3%	
	41, 42 / 41, 42 / -12 MAIN	-12 vdc, ±6%	
	9, 10 / 71, 72 / -5 MEM	-5 vdc, ±6%	
	7, 8 / 73, 74 / +5 MEM	+5 vdc, ±3%	
	5, 6 / 75, 76 / +12 MEM	+12 vdc, ±3%	
16	Set KEY SWITCH to OFF position (remove ac power from power supply).	–	–
17	Install full complement of known good logic boards and substitute the chassis for the hot mockup chassis (figure 4-1).	–	–
18	Set KEY SWITCH to ON or LOCK position.	Fan motors operate quietly, POWER and RUN LEDs light.	–
19	Load and execute 990/4 diagnostics in accordance with table 7-1.	–	–

Table 6-2. Chassis Fault Isolation Procedures

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
1	Fuse continues to blow when replaced. All power supply and logic boards removed from chassis.	Shorted windings in blower motor	SHUT OFF POWER TO THE CHASSIS. Disconnect blower motor leads from terminal strip pin 1 and measure dc resistance across each motor winding. **NOTE** A defective motor may contain shorted windings which may or may not show up with a dc resistance check.	Dc resistance greater than 20 ohms. Motor not abnormally hot to the touch.	Replace defective blower motor.
		Shorted surge voltage protector 1C1	WITH AC POWER OFF, disconnect 1C1 lead from terminal 1 on terminal strip and measure resistance across 1C1.	High resistance	Replace 1C1
		Internal short in line filter	WITH AC POWER OFF, measure resistance between pins 3 and 5 of line filter 1FL1.	If optional transformer not installed, infinite resistance should be measured.	Replace 1FL1
		Short winding in optional transformer (if installed)	WITH AC POWER OFF, disconnect transformer leads from circuit and measure resistance across primary and and secondary windings.	Greater than 5 ohms.	Replace transformer if chassis will be returned to original site. Otherwise, remove transformer and wire in accordance with figure 6-1.
2	Loss of ac power, fans inoperative	Defective switch 1A4S1.	WITH AC POWER PLUG REMOVED FROM THE AC POWER SOURCE, and key switch on panel set to LOCK or ON position, measure resistance between terminals C and NO (see figure 6-2).	0 ohms	Replace 1A4S1
		Open winding in line filter	WITH POWER PLUG REMOVED FROM AC SOURCE, measure resistance between terminals 1 and 3 of 1FL1.	Approximately 0 ohms	Replace 1FL1
			Repeat above procedure for terminals 2 and 5 of line filter.	Same as above	Replace 1FL1
		Faulty power cord	WITH POWER PLUG REMOVED FROM AC POWER SOURCE, measure resistance between hot prong on plug and either side of power fuse 1F1.	0 ohms	Check resistance across fuse socket terminals 1 and 2. If normal, replace power cord.
			Repeat above step and measure resistance between neutral prong and pin 5 on line filter 1FL1.	0 ohms	Replace power cord.

Table 6-1. Chassis Checkout Procedure

Step	Procedure	Normal Indication	If Abnormal
1	Disconnect chassis power plug from ac power source.	–	–
2	Remove rear and side access panels from chassis to permit access to ac distribution circuits (see figure 6-3).	–	–
3	Visually inspect the ac line filter (1FL1), optional power transformer (1T1) and filter capacitor 1C1 for signs of overheating or leakage.	No visible signs of leakage or discoloring	Replace damaged components
4	Inspect all terminals on the terminal board 1TB1 and on the blower motors (where used) for secure fit.	Tight electrical connections, no looseness or slack	Repair defective terminals
5	Measure resistance across terminals 1 and 2 on main fuseholder, 1XF1.	0 ohms	Replace fuse with 10A, slo-blo fuse
6	With key switch on operator/programmer panel set to OFF position, measure resistance between common and normally open terminals of 1A4S1 (see figure 6-2 for location).	Infinite ohms	Replace 1A4S1
7	Set key switch to UNLOCK position and repeat resistance measurement between common and normally open contacts of 1A4S1.	0 ohms	Check cam on key switch. If normal, replace 1A4S1.
8	Repeat resistance measurement with key switch in UNLOCK position.	0 ohms	Same as above
9	Measure resistance across terminals 1 and 2 of terminal strip 1TB1.	Greater than 5	See table 6-2
10	Measure resistance between ground prong on ac power plug and the chassis.	0 ohms	Check ground connection on power cord. Replace power cord if necessary.
11	Temporarily short access + and – terminals of capacitor 1C1 and then measure resistance between the two terminals using the RX1K scale.	Temporarily goes toward 0 ohms and gradually increases toward infinity	Replace 1C1.
12	Remove all logic boards from chassis. Remove power supply boards 1A2, 1A3, and 1A6 (if standby option installed) and test these boards in accordance with Section XIII. Remove and replace backpanel board.	–	–
13	Install known good power supply boards and ensure that all cables are correctly installed in accordance with figure 6-1. If standby supply is not used, a jumper plug must be installed in 1A3J3 on main supply board.	–	–
14	Connect chassis to ac source and set key switch on operator/programmer panel to ON/LOCK position.	Fan motors operate quietly.	–

SECTION VII

990/4 MICROCOMPUTER BOARD TROUBLESHOOTING DATA

7.1 GENERAL

This section provides detailed circuit analysis and other troubleshooting data required to perform depot-level maintenance on the 990/4 microcomputer circuit board.

7.2 CIRCUIT BOARD ANALYSIS

Functionally, the 990/4 microcomputer board consists of seven major sections including:

- Processor section
- Memory section
- CRU interface section
- Vectored interrupt structure
- Programmer panel interface
- Clock and clear section
- DMA/extension memory interface

A detailed block diagram of the 990/4 microcomputer board is shown in figure 7-1. Functional circuit analysis for each section is provided in the following paragraphs. For the following discussion, reference should also be made to the 990/4 microcomputer board logic diagram, Part Number 944911 in the *990 Family Maintenance Drawings Manual.*

7.2.1 PROCESSOR SECTION. The processor function for the 990/4 microcomputer system is provided by the TMS 9900 microprocessor chip. Basically, the chip is a 16-bit computer with a flexible set of 69 instructions as summarized in Appendix A of this manual. The chip contains no internal program memory or clock source and makes use of the memory and clock functions on the 990/4 microcomputer board (and the memory on the 990/4 memory expansion board). The TMS 9900 chip pin assignments are shown in figure 7-1 and the TMS 9900 interface timing is shown in figure 7-2.

7.2.1.1 Restart Initiate Logic. The restart initiate logic (figure 7-3 and 7-4) provides for the generation of a LOAD– signal under the following conditions:

- When power is initially applied to the system if a jumper is installed between terminals E21 and E22 (processor traps to FFFC).
- When the panel is in the RUN mode, the key switch in in the UNLOCK position and the HALT/SIE switch is pressed (provides a trap to location FFFC which leads to the programmer panel software). Also generated if operator panel key switch is set to LOAD position.

- When the panel is in the HALT mode and the HALT/SIE switch is pressed, the microprocessor executes a single user instruction and then issues an SBO instruction which is decoded on the 990/4 board and used to generate an SIECLK–. This signal results in the generation of another LOAD– which leads back to the panel software.

The operation of the restart initiate logic for the above cases is briefly described in the following subparagraphs.

Power Up Restart. If a jumper wire is installed between E21 and E22, a LOAD– signal is generated when the power up clear signal TLPRES– occurs (see figure 7-4(a)). This option is not used in the standard configuration. The sequencing of the flip-flops for this condition is as follows:

1. U98-5 and U99-9 forced to 1 by TLPRES– at preset inputs.

2. U99-5 goes to 1 on trailing edge of next IAQA–. U99-6 goes low at same time clearing U98-5 to a 0.

3. On trailing edge of second IAQA–, U99-9 goes to 0 which clears U99-5.

4. LOAD– goes low for the period of time that SIELOAD (U99-5) is a logic 1.

If the jumper is installed between E22 and E27, a LOAD– will be generated but goes away before being recognized by the microprocessor (TMS 9900 looks for the signal during the second IAQ). This sequence is shown in figure 7-4(b).

Restart From Programmer Panel. If the programmer panel is in the RUN mode, the key switch is in the UNLOCK position and the HALT/SIE switch is pressed on the panel, a logic low RESTART– signal is generated which results in a LOAD– signal to the processor.

For the following discussion of panel restart operation, refer to figure 7-3 and figure 7-4(c). The sequencing of flip-flops to generate the restart LOAD– is as follows:

1. RESTART– from the programmer panel is debounced and used to clock the RUNQ flip-flop (U115-9 goes low).

2. If the Idle flip-flop is not set (CPU in RUN mode), the panel load enable flip-flop (U115-5) clears on the following IAQA–. This results in a logic-low input to U98-12.

3. LOAD– goes low.

4. On the trailing edge of the next IAQA–, U98-8 returns high which disables the LOAD– signal.

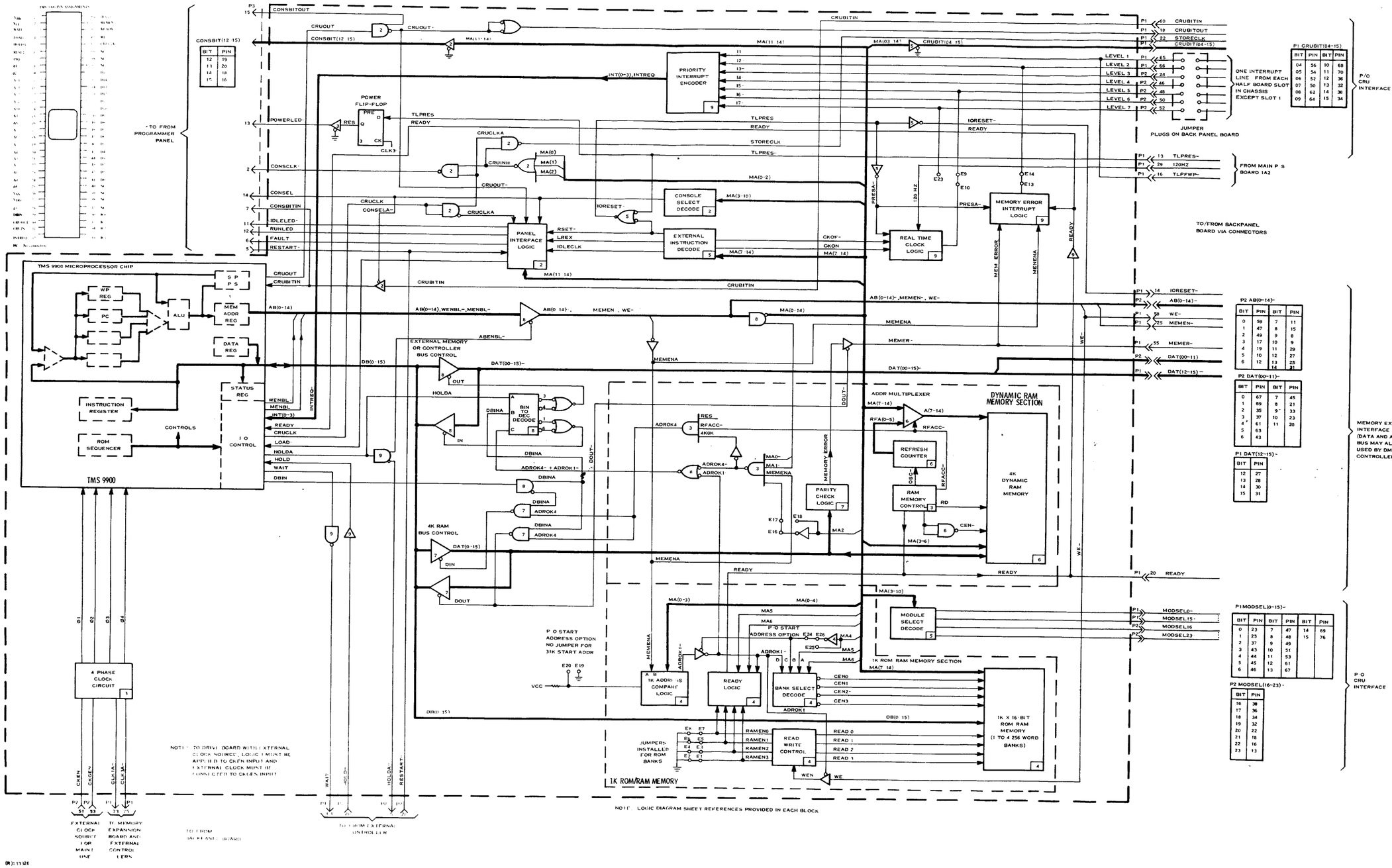


Figure 7-1. 990/4 Microcomputer Board, Detailed Block Diagram

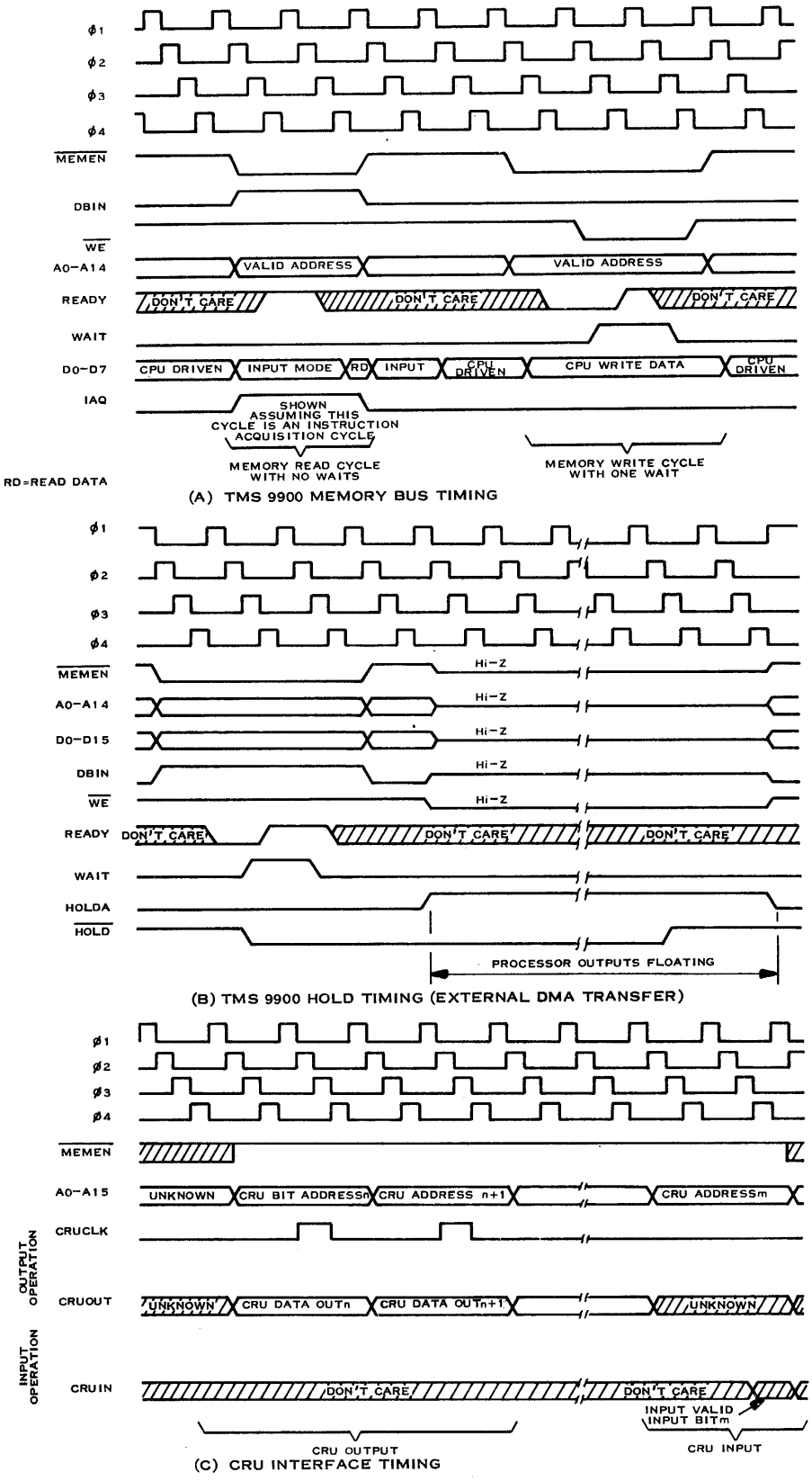


Figure 7-2. TMS 9900 Interface Timing Diagram

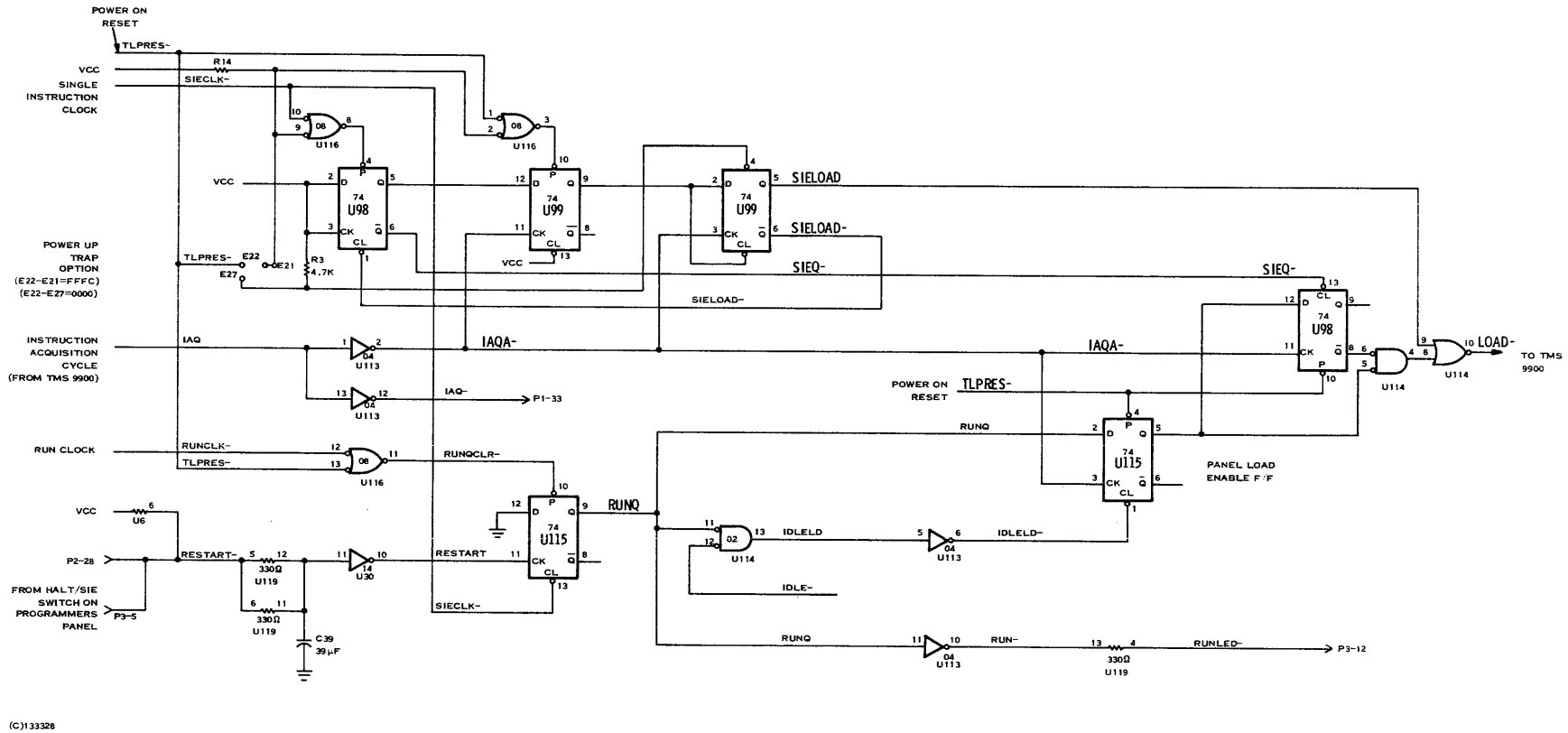
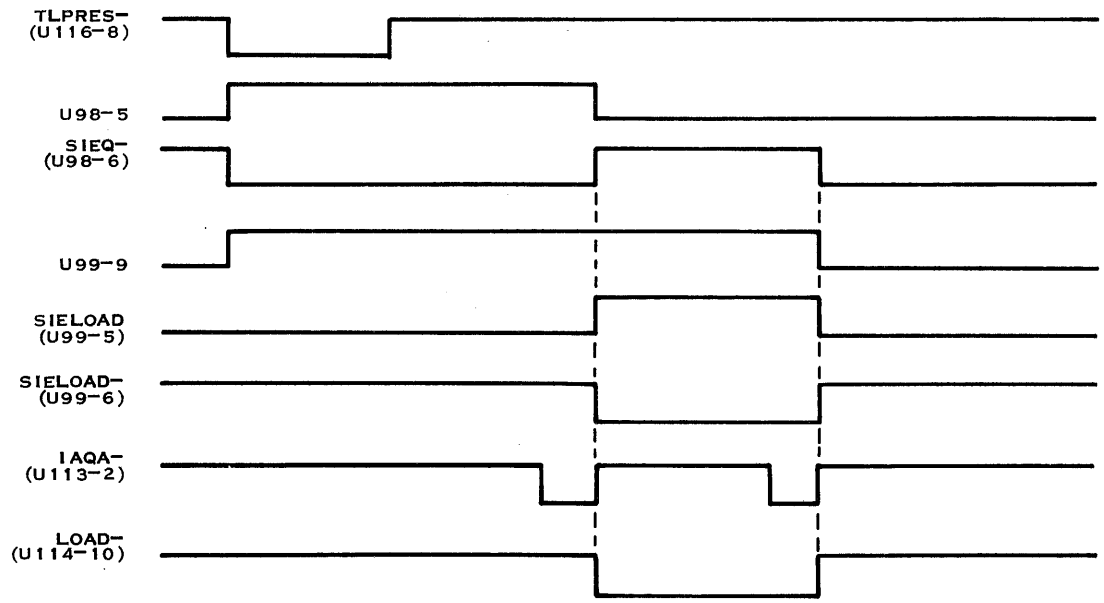
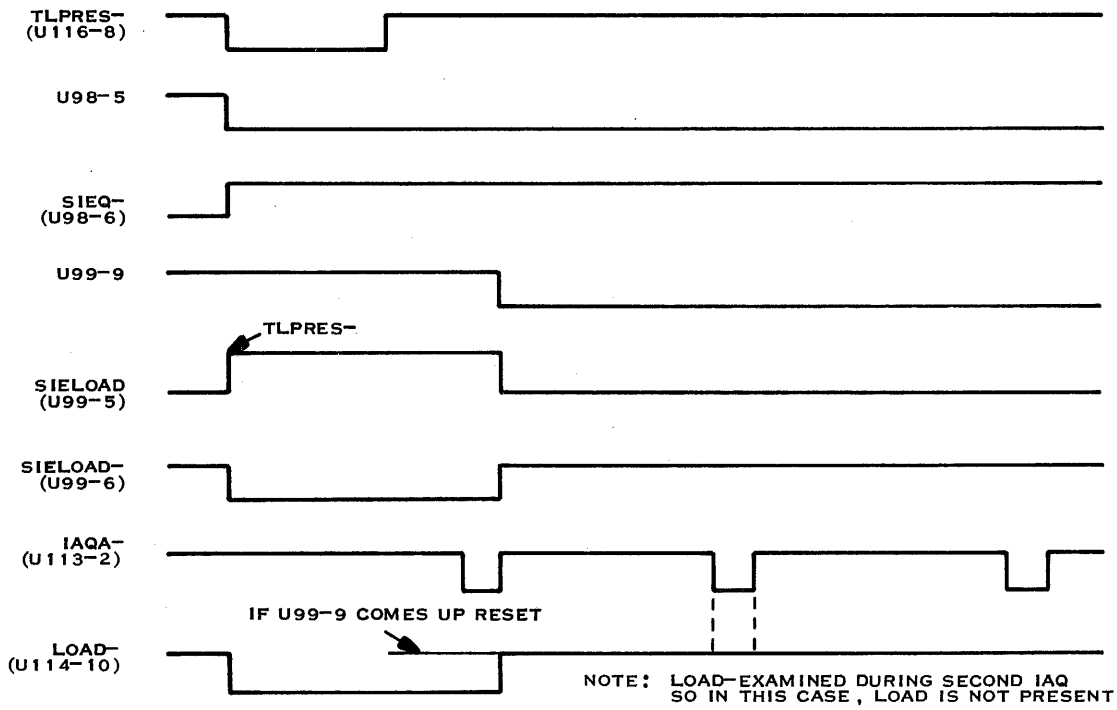


Figure 7-3. TMS 9900 Load Control, Simplified Logic Diagram



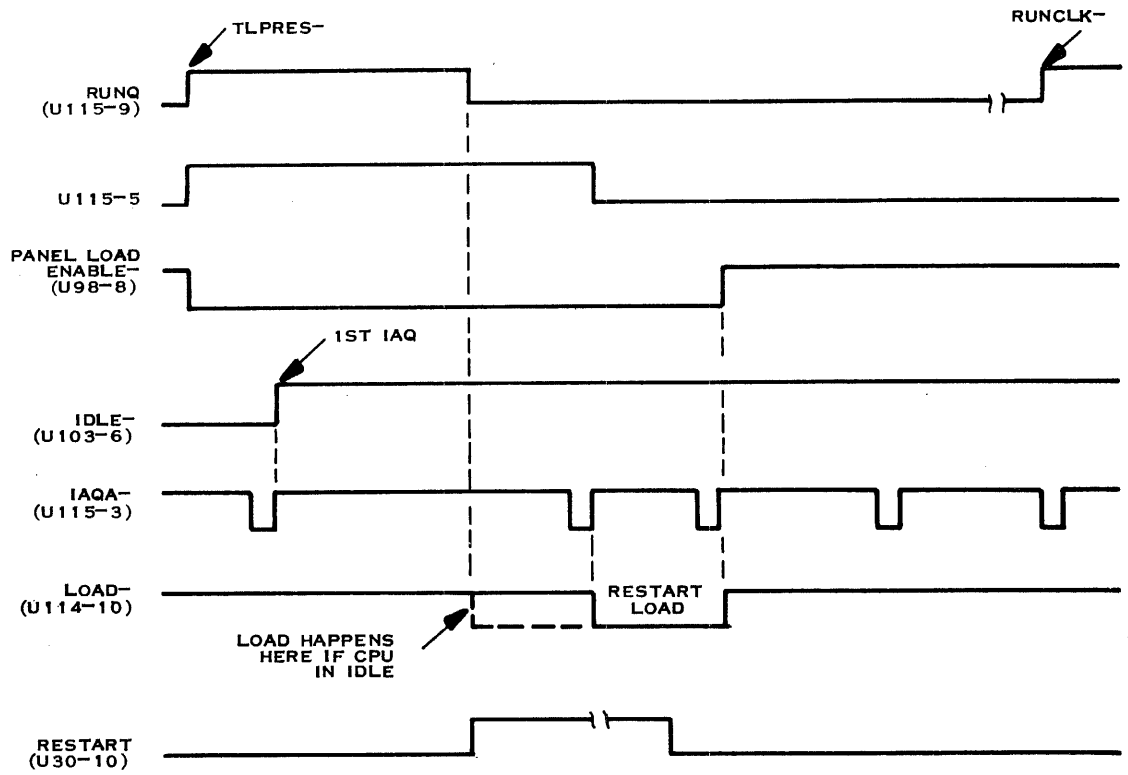
(A) INITIAL POWER UP LOAD TO FFFC (JUMPER E22 TO E21 INSTALLED

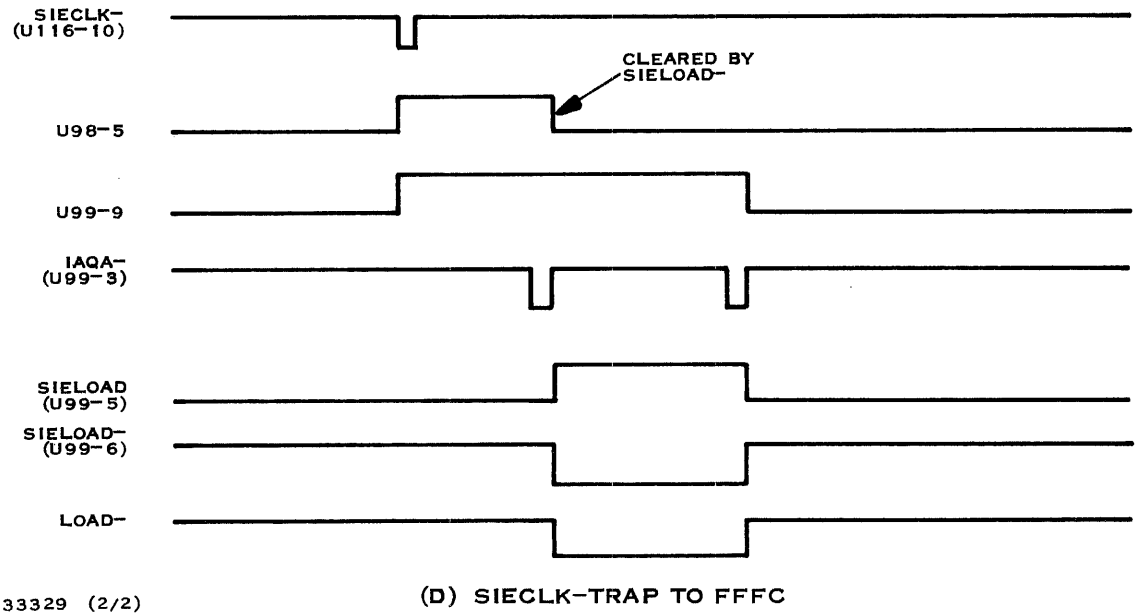


(B) 0000 INITIAL POWER UP LOAD (JUMPER E22 TO E27)

(A)133329 (1/2)

Figure 7-4. Load Timing Diagram (Sheet 1 of 2)





(A)133329 (2/2)

Figure 7-4. Load Timing Diagram (Sheet 2 of 2)

SIE Restart. An SIE restart is shown in figure 7-4(d) and briefly described below:

1. U98-5 and U99-9 both preset to a 1 by SIECLK–.

2. On trailing edge of IAQA–, SIELOAD (U99-5) goes high. At the same time, SIELOAD– goes low which clears U98-5.

3. On the trailing edge of the next IAQA–, SIELOAD clears which causes the LOAD– signal to return high.

4. The sequence is repeated each time an SIE is initiated by the software (generally in response to the HALT/SIE switch being pressed with the panel in the HALT mode of operation.

The low-active LOAD– signal causes the microprocessor to trap to memory location FFFC which points back to the panel software.

7.2.2 MEMORY SECTION. The 990/4 microcomputer board may be equipped with two functionally independent memories including the 1K ROM/RAM memory and the 4K dynamic RAM memory. Basically, the 1K memory is implemented with ROMs which contain 733 ASR loader program, the programmer panel software, and the self-test diagnostic programs.

The 4K dynamic RAM is used for program storage. In the standard configuration, the 4K dynamic memory occupies the address space from 0000_{16} to 1FFE (byte addresses) and the 1K ROM/RAM memory occupies the upper end of memory (F800 to FFFE). A simplified diagram showing the 990/4 microcomputer memory map is presented in figure 7-5. The operation of the two onboard memory sections are briefly described in the following paragraphs.

7.2.2.1 4K Dynamic RAM Memory. A simplified block diagram of the 4K dynamic RAM memory is shown in figure 7-6. As indicated in this figure, the 4K RAM is implemented with 16 TMS 4051 4K by 1-bit RAM ICs plus an optional TMS 4051 for parity storage. Due to the MOS structure of the TMS 4051s, a refresh cycle must be performed on every memory chip every 2-milliseconds to prevent loss of data.

The circuitry required to perform the refresh function includes:

- Refresh oscillator
- Refresh address counter (counts to 64)
- Address multiplexer
- Refresh controller

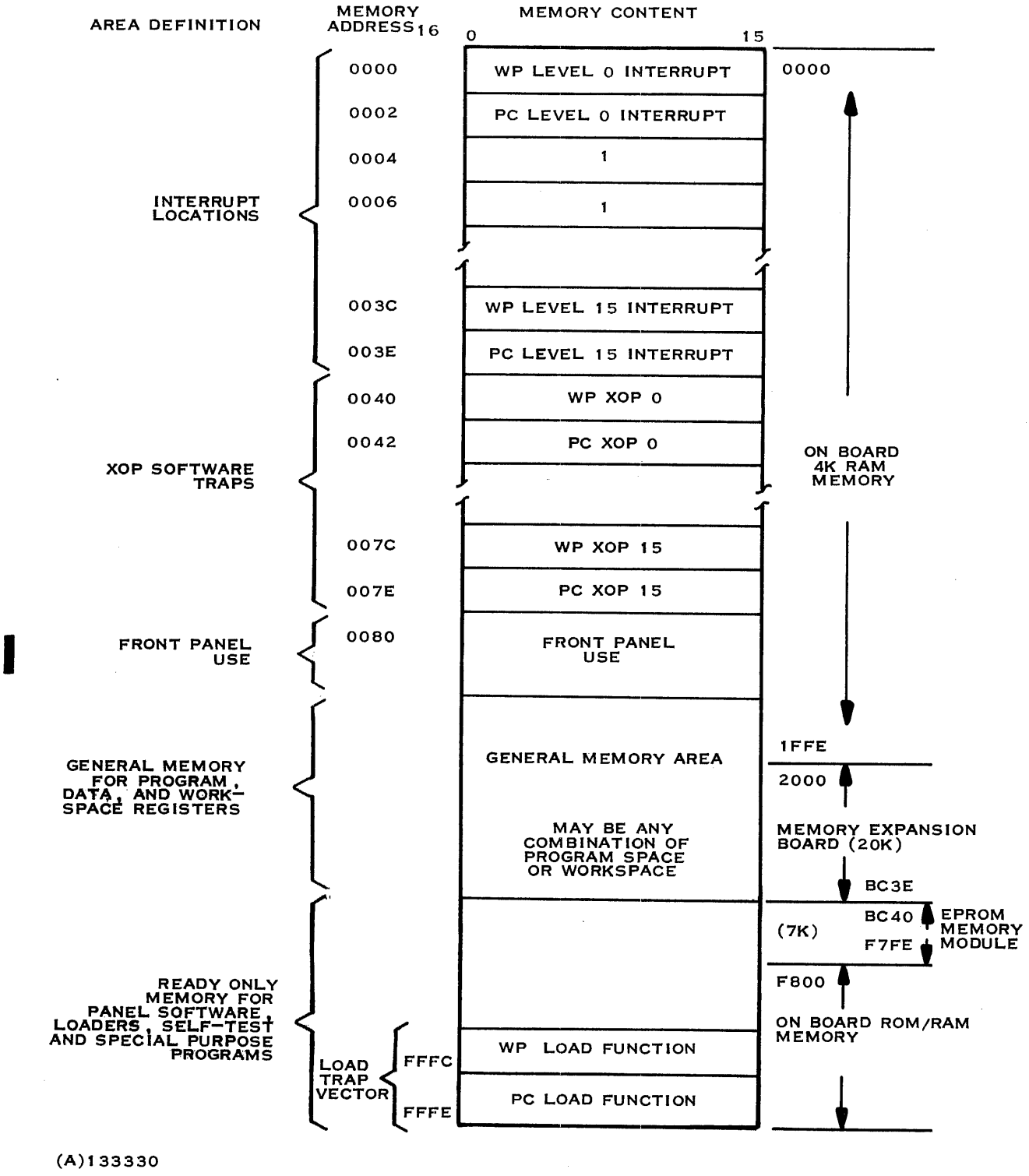
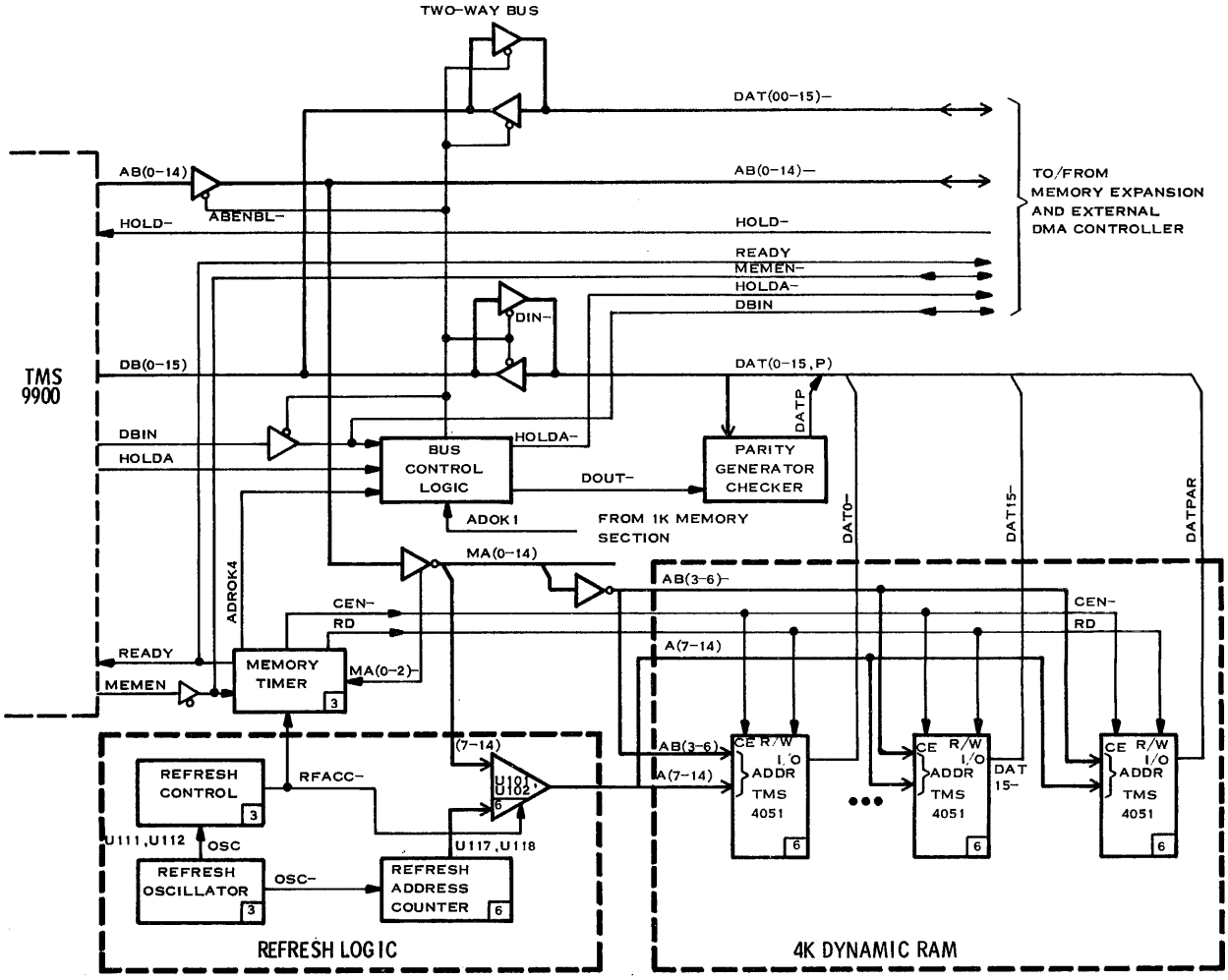


Figure 7-5. 990/4 Microcomputer Memory Map (Standard Configuration)



NOTE: LOGIC DIAGRAM SHEET REFERENCES PROVIDED IN EACH BLOCK

DAT	4051	PU	TWO-WAY BUS CHIP
0	U44	U65 – 10	U41,U42
1	U45	– 11	
2	U46	– 12	
3	U47	– 13	U41,U42
4	U48	– 14	U63,U64
5	U49	– 15	
6	U50	– 2	
7	U51	U65 – 1	U65,U64

DAT	4051	PU	TWO-WAY BUS CHIP
8	U66	U65 – 4	U63,U64
9	U67	– 7	U63,U64
10	U68	– 3	U80,U121
11	U69	– 5	
12	U70	– 6	
13	U71	– 9	
14	U72	U65 – 8	
15	U73	R – 19	U80,U121
P	U74	R – 20	—

(C)133331

Figure 7-6. 4K Dynamic RAM Memory

Refresh Timing. For the following discussion of refresh operation, refer to the simplified logic diagram in figure 7-7 and the associated timing diagram in figure 7-8.

Basic timing for a memory refresh cycle is provided by the refresh oscillator stage U108. As indicated in figure 7-7, the output of the oscillator is a pulse train with a positive pulse width of approximately 20-microseconds and a negative pulse width of 11-microseconds. The cycle time is approximately 31-microseconds.

The inverted output of the refresh oscillator (OSC–) is used to drive the refresh address counter (64 pulses every 2-milliseconds). The true output of the refresh oscillator (OSC) is applied to the clock input of the first stage (U111) of the refresh controller. On the leading edge (low-to-high transition) of OSC, RFEQD (U111-9) goes high. On the trailing edge of the next phase 3 clock (CLK3–), the next stage of the controller sets (RFRQ goes high). On the next phase 2 clock (after completion of any memory cycle currently in progress), Refresh Access (RFACC–) is generated which resets the first two stages of the refresh controller (RFEQD and RFRQ), sets up the address multiplexer to route the outputs of the refresh address counter to the highorder six address lines of all 4K RAM chips and activates the chip enable timing circuit. At the same time, RFACC (Q output of U112-9) is inverted and gated to the TMS 9900 and to the memory interrupt circuits.

The logic-low RFACC– signal causes the chip enable flip-flop (U95-9) to set. The output of this flip-flop (CE) is inverted and applied to the chip enable inputs on all 4K RAM memory chips. On the following phase 3 clock (CLK3–), the CED flip-flop (U95) sets and then both flip-flops are reset on the leading edge of the next phase 1 clock (CK1A) by memory cycle end (CYEND–).

Memory Read/Write Timing. For the following discussion of memory timing for a read or write operation, refer to the simplified logic diagram in figure 7-7 and the timing diagram in figure 7-9. A memory read or write cycle is initiated when MEMENA (inverted version of MEMEN–) from the TMS 9900 goes high and the address on the data bus falls within the address space of the 4K RAM (0000 to 1FFE). When these conditions are met, a 4K address OK (4KOK–) is generated. This signal is gated with refresh access (RFACC–) to inhibit the memory cycle during memory refresh. If a refresh is not being performed and a reset is not present, ADROK4– is generated which causes the chip enable flip-flop U95 to set on the trailing edge of the next CLK3–.

Chip enable delayed (CED) is then generated on the trailing edge of the next CLK3– pulse and cycle end (CYEND–) is generated on the leading edge of the next phase 1 clock (CK1A) for a read operation or immediately after CYEND– goes low for a write cycle.

The address OK signal (ADROK–), which activated the chip enable generation logic, is also sent to the 9900 bus control logic to lock out the external memory data lines. The two-way bus lines between the 4K RAM and the TMS 9900 are gated in the proper direction by DBIN from the microprocessor chip.

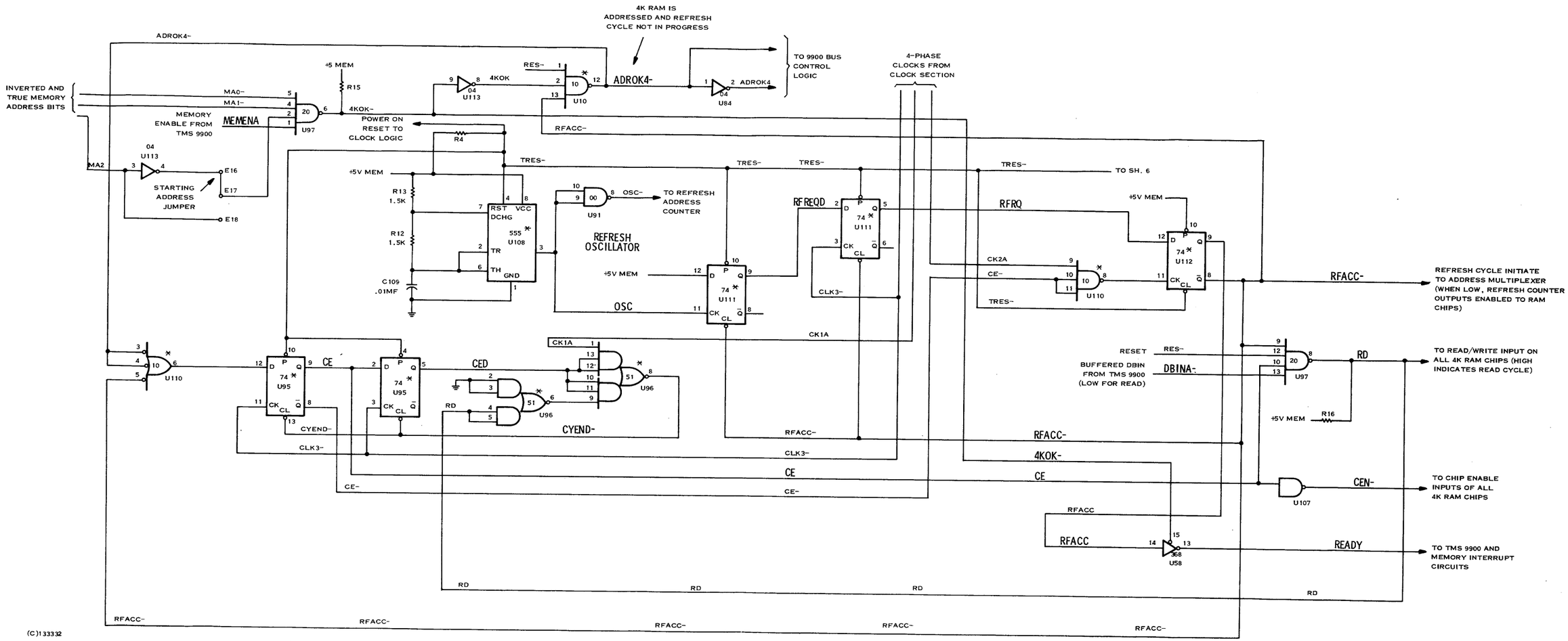


Figure 7-7. 4K RAM Timing Control, Simplified Logic Diagram

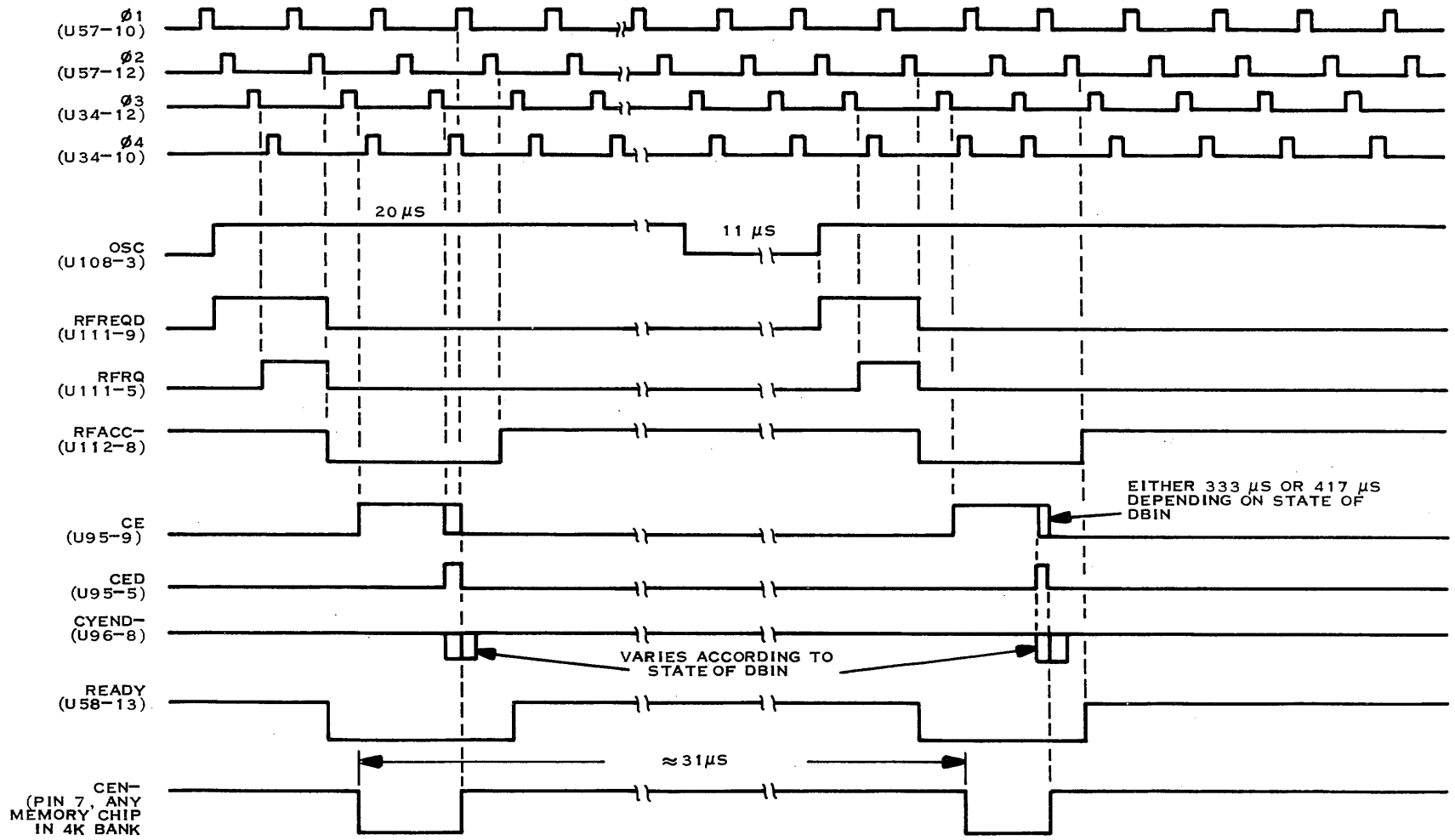


Figure 7-8. Memory Refresh Timing Diagram

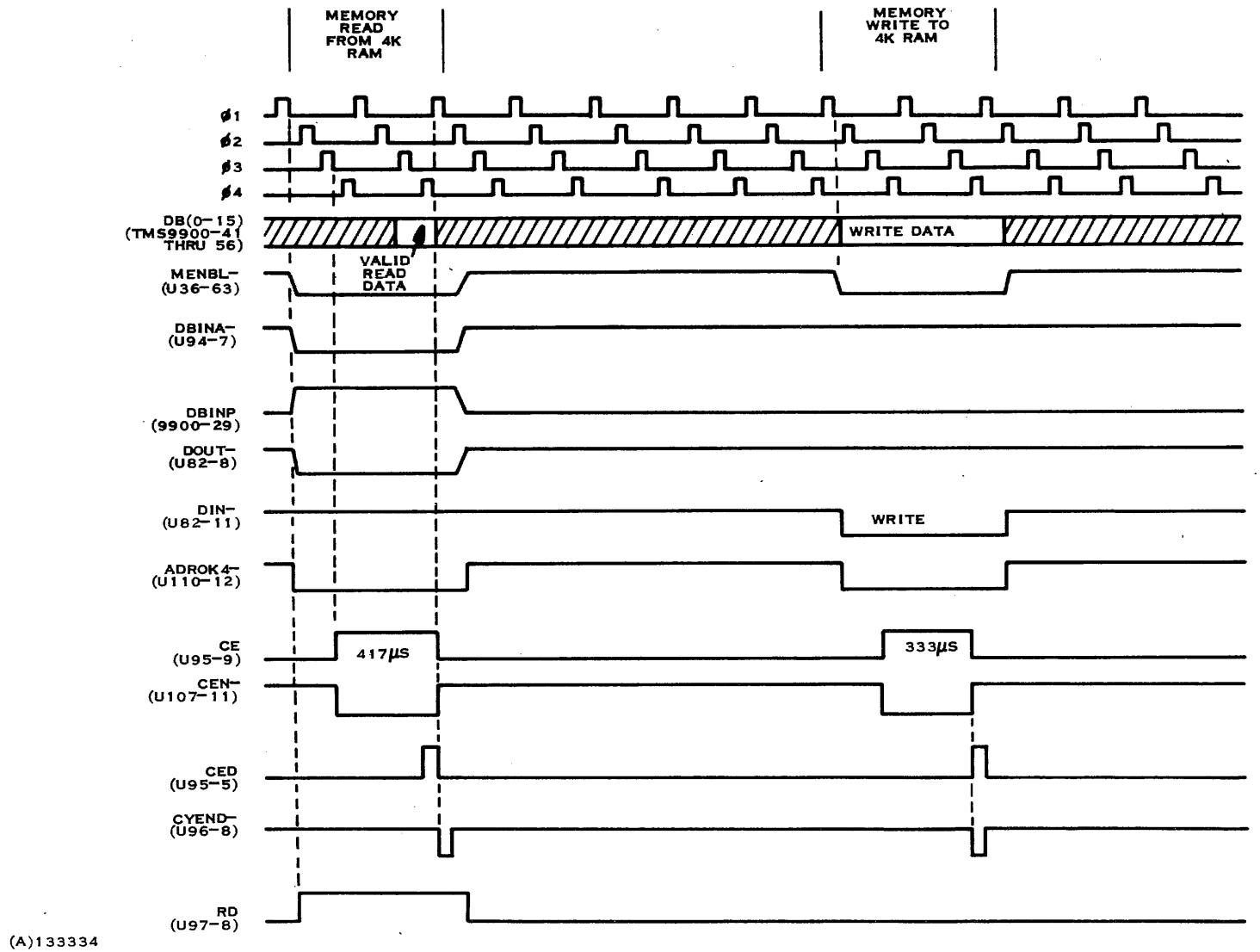


Figure 7-9. Dynamic RAM Memory, Read/Write Timing Diagram

7.2.2.2 **1K ROM/RAM Memory.** The 990/4 microcomputer board also contains provisions for a 1K memory at the upper end of the address space (F800 to FFFE byte addresses). This memory is functionally divided into four 256 by 16-bit word banks and may be implemented on a bank level with either SN74S287 ROM ICs or TMS 4043 static RAM ICs (a given 256-word bank must contain all ROM or all RAM chips). A group of four jumper wires are used to differentiate between ROM and RAM memory. In the case of a ROM bank, the jumper is installed as shown in figure 7-10. The jumper holds the associated READ(n) output at a constant logic low level which permits a read to be initiated whenever a bank enable (CEN(n)–) is generated by the address decode. The jumper wires also perform another important function in the generation of the READY signal. With the jumper installed, READY is returned to the microprocessor on the trailing edge of the next CLK3– pulse following ADROK1– (see timing diagram in figure 7-11 and logic diagram sheet 4 (drawing number 944911). If the jumper is not installed (RAM bank), ready is delayed by two phase 3 clocks to meet the 1 microsecond cycle time requirements of the static MOS RAM. Ready indicates to the processor that a new memory cycle can be initiated on the next phase 1 clock.

7.2.3 **CRU INTERFACE SECTION.** The CRU interface logic permits the TMS 9900 to set, reset or test any of 16-bits in any half-board slot in up to seven expansion chassis under software control. Basically, the CRU interface section buffers the processor address bus, bits 3-14, and sends these bits out as CRU address bits 4-15 (CRUBIT 4-15) as shown in the simplified diagram in figure 7-12. The CRU interface also includes a CRUBITIN (serial input data) line which is fanned in from all CRU interface boards; a CRUBITOUT output data line used to transfer serial data from the TMS 9900 to the CRU interface boards and an IORESET– signal which resets all CRU interface boards when power is initially turned on or when a RSET instruction is executed by the microprocessor. Interrupts from the various CRU interface boards in the chassis are jumper-wired to the vectored interrupt logic on the 990/4 board through a jumper plug on the backpanel board (see figure 6-3).

7.2.3.1 **CRU Addressing Scheme.** As shown in figure 7-12, the 990/4 board monitors MA(3-10), which is equivalent to CRUBIT(4-11). If bits 3-5 specify chassis 0, the chassis 0 module decode select circuit generates a logic-low line to one of the 24 half-board slots in the chassis (for 13-slot chassis) corresponding to the value of MA(6-10). For 6-slot chassis, only 10 module select lines are used.

If chassis 1 through 7 is addressed, the module select decode function is accomplished on the CRU buffer board in the addressed chassis. (See Sections XI and XII for description of CRU expansion and CRU buffer boards.)

In order to read a bit from a selected board in a selected chassis, the microprocessor places the appropriate CRU address on the memory address lines and reads the data on the CRUBITIN line after a delay to permit the addressed device to respond (see figure 7-2).

In order to store data in a specified bit location in one of the boards in either the main chassis or up to seven expansion chassis, the microprocessor places a valid CRU address on the memory address lines and issues a store clock pulse. The addressed module then accepts the data bit from the CRUBITOUT line. However, if the main chassis is addressed, the store clock pulse to all external boards is inhibited.

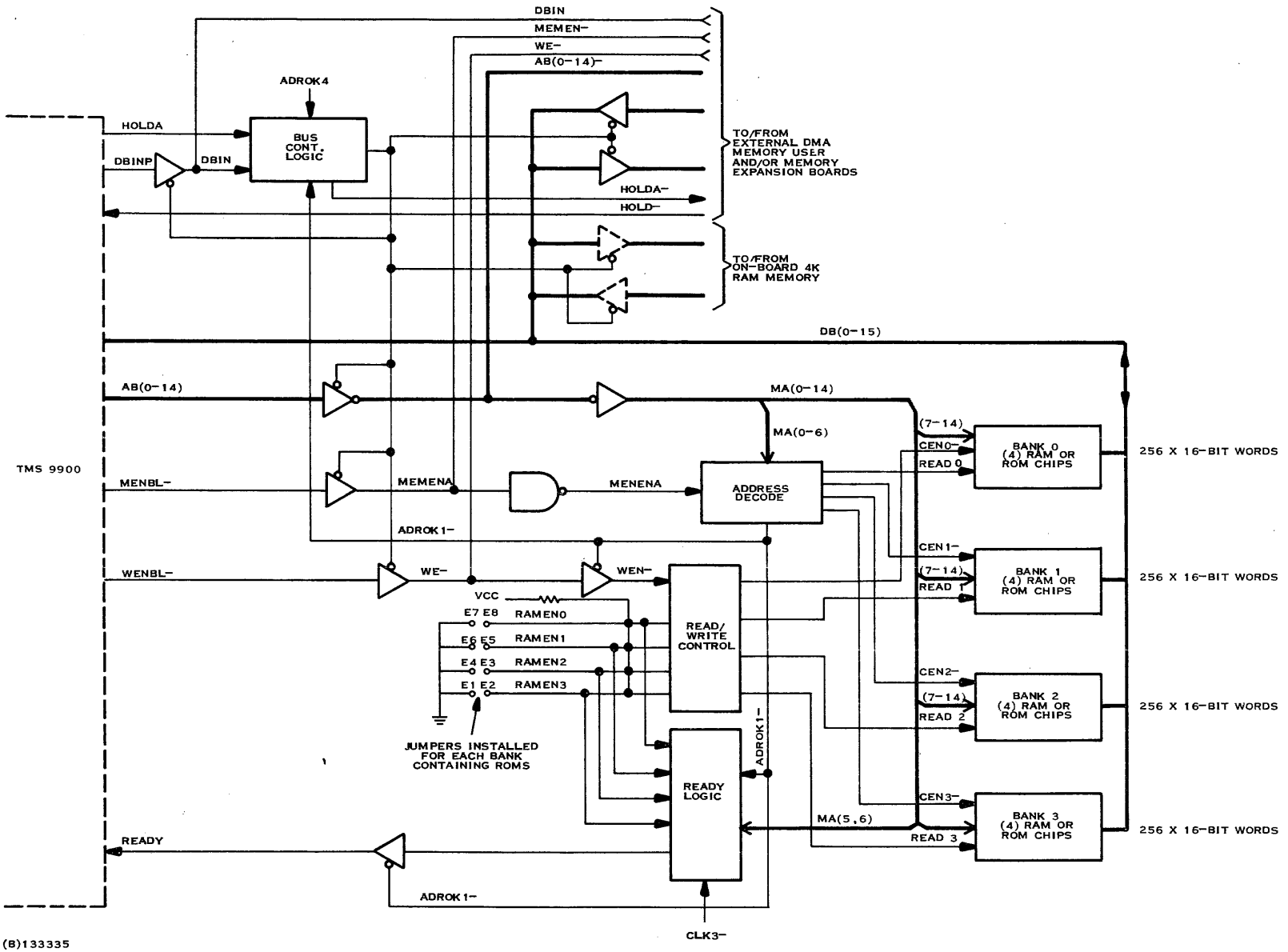


Figure 7-10. 1K ROM/RAM Memory Section, Block Diagram

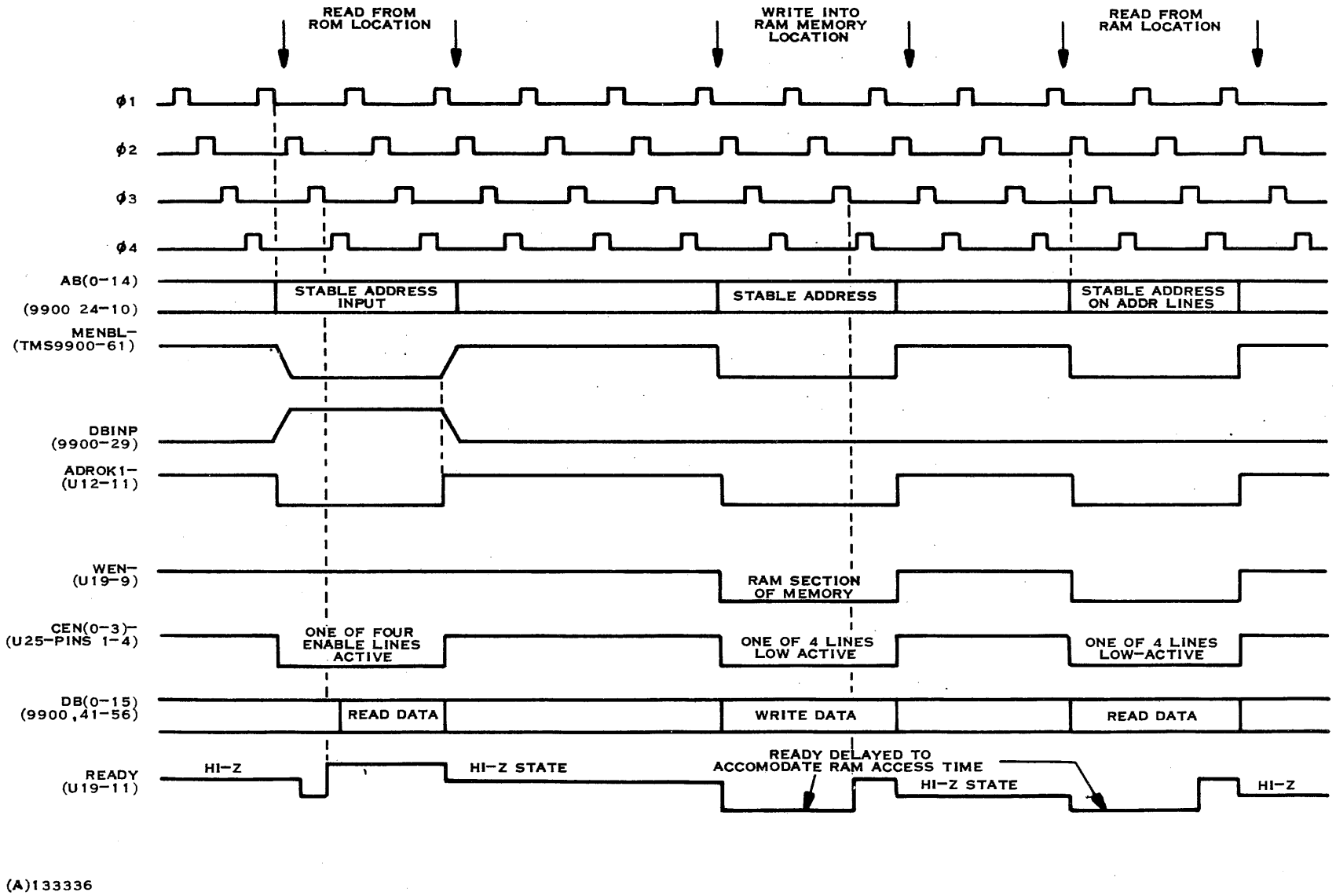


Figure 7-11. ROM/RAM Memory Section, Timing Diagram

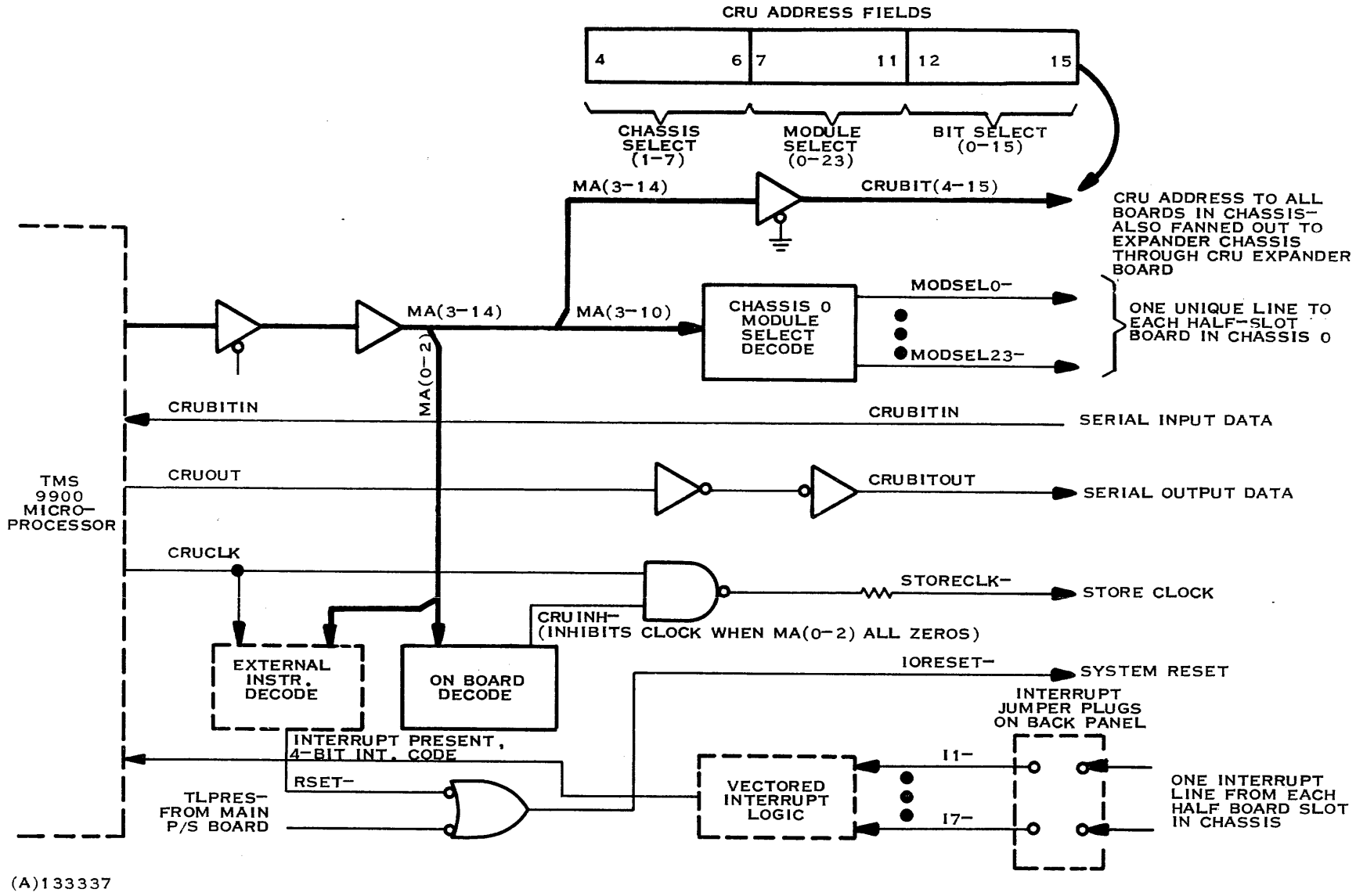


Figure 7-12. CRU Interface Logic, Simplified Diagram

7.2.4 **CLOCK SECTION.** The 990/4 microcomputer board develops true and complement outputs of a 4-phase clock for use in synchronizing operations between the TMS 9900 and all external circuits throughout the system. For the following discussion of the 4-phase clock logic, refer to the simplified logic diagram in figure 7-13.

Generation of the 4-phase clocks originate in a 12 MHz free running, crystal-controlled oscillator. Provisions are included in the circuit to permit substitution of an external clock source for the 12 MHz oscillator output. The basic pulse train output from the oscillator is frequency-divided by means of two flip-flop stages (U92). The Q and $\overline{Q}$ outputs from these two flip-flops are gated in various combinations to generate the 4-phase clocks as shown in the timing diagram in figure 7-14.

The true outputs of the clock gating stage are routed to four clock driver circuits which provide the clocks for the TMS 9900. The waveform specifications for the 4-phase clocks are provided in figure 7-15. As indicated in this figure, the clocks at the output of the clock driver stages typically have rise and fall times of 10 ns, pulse widths of 65 ns and cycle times of 33 ns.

7.2.5 **INTERRUPT SECTION.** The 990/4 microcomputer board monitors interrupts from the external CRU interface boards and from the power fail, memory error and real time clock circuits on the 990/4 board. When an interrupt is detected, the interrupt logic issues an interrupt request (INTREQ) to the TMS 9900 and encodes the highest interrupt present onto the INT(0-3) lines. For the following discussion of the interrupt section, refer to the simplified logic diagram in figure 7-16.

As shown in figure 7-16, the interrupt lines from the external devices are routed directly to the inputs of the interrupt latch (U4) via the jumper plug on the chassis backplane board. Each side (P1 and P2) of each chassis slot contains an interrupt line which is routed up to the jumper plugs. The assignment of interrupt levels 1 through 7 are then determined by the jumper wires installed in the jumper plugs (see installation section of the 990/4 Hardware Reference Manual). When a CRU interface board in the main chassis (or one of the expansion chassis) issues an interrupt, its interrupt line goes low and remains low until the microprocessor resets the interrupt via a CRU instruction addressed to the device (or by issuing an IORESET–).

The seven interrupt lines are assigned priority with I1– having highest priority and I7– having lowest priority. Incoming interrupts are synchronized with the phase 3 clock (CLK3–) and the highest priority interrupt present is encoded onto the INT(0-3) lines to the microprocessor. At the same time, an interrupt request (INTREQ) is sent to the 9900. When the 9900 completes processing any present instruction, it traps to a dedicated memory location corresponding to the interrupt level. The memory location includes a workspace pointer and program counter value which defines the workspace and starting address for the interrupt servicing routine. When the processor completes the routine, it returns to the previous program counter and workspace pointer values and continues processing the original program.

7.2.5.1 **Onboard Interrupts.** The interrupt structure monitors three types of onboard interrupts including:

- Power fail interrupt (TLPFWP–) – Output from the power supply board is routed through a jumper wire (E11 to E12) to I1– (highest priority available outside of the TMS 9900).

- Memory error interrupt (MEINT) – Connects to interrupt level 2 via a jumper wire between E13 and E14.

- Real time clock interrupts (120 HZINT) – Connects to interrupt level 5 via a jumper between E9 and E10.

Real Time Clock Logic. The real time clock logic is a software-controlled source of interrupts which occur at a nominal 120 Hz rate. The basic clock pulse (120HZ) is generated by the main power supply boards, inverted and routed to the input of the real time clock flip-flop (U29-3). If the interrupt mask stage (U29-8) is set (CKON instruction executed by microprocessor), an interrupt is generated when the first pulse is received from the power supply. The interrupt is reset by a CKOF instruction. In order to enable the next interrupt, another CKON instruction must be executed. This same sequence of CKON, CKOF and CKON instructions is repeated for each real time clock interrupt. In the standard configuration, the RTC interrupt is wired to level 5 via a jumper from E9 to E10. Optionally, the interrupt can be wired to interrupt level 7 by jumpering E10 to E23 with E9 left open.

Memory Error Interrupts. The memory error interrupt logic is activated each time a memory cycle is initiated (MEMENA goes high) and READY is returned by the active memory section. An enable is generated at U28-5 on the trailing edge of the CLK3– pulse after READY goes high. The enable is gated with the inverted MEMER– (memory error) signal from the parity error checker in the RAM memory sections (either the 4K RAM on the 990/4 microcomputer board or the 990/4 memory expansion board). If an error was present, the memory error flip-flop (U28-8) latches in the clear state and an interrupt is stored in level 2 of interrupt register, U4.

The memory error interrupt flip-flop then remains latched until cleared by a CRU instruction executed by the TMS 9900 software (MERCIR– goes low). The memory error interrupt enable flip-flop (U28-5) clears on the trailing edge of the next phase 1 clock after either READY or MEMENA goes low.

7.3 990/4 MICROCOMPUTER TROUBLESHOOTING PROCEDURES

Troubleshooting procedures for the 990/4 microcomputer board are based on the use of the checkout procedures in table 7-1 to locate board functional failures and the use of scoping loops (paragraph 7.3.2) and the fault isolation procedures in table 7-2 to isolate malfunctions down to a defective component.

After the faulty component has been replaced, the board must be retested in accordance with the procedures in table 7-1 to ensure that all malfunctions have been corrected.

7.3.1 PRELIMINARY VISUAL INSPECTION. Prior to inserting the 990/4 board into the hot mockup chassis, the following inspection should be performed:

1. Inspect all components for signs of overheating, looseness in the socket (memory chips), broken etch or other signs of visible damage. Remove and replace any faulty components before proceeding with the checkout procedure.

2. Ensure that the ROMs and jumper options are properly installed in accordance with figure 7-17. This restores the board to the standard configuration.

3. Using an ohmmeter, measure the resistance between each of the power supply connector pins to the board and the ground connector pin. If a short circuit (0 ohms) is detected on any supply connector, locate and replace shorted component before continuing the checkout procedure.

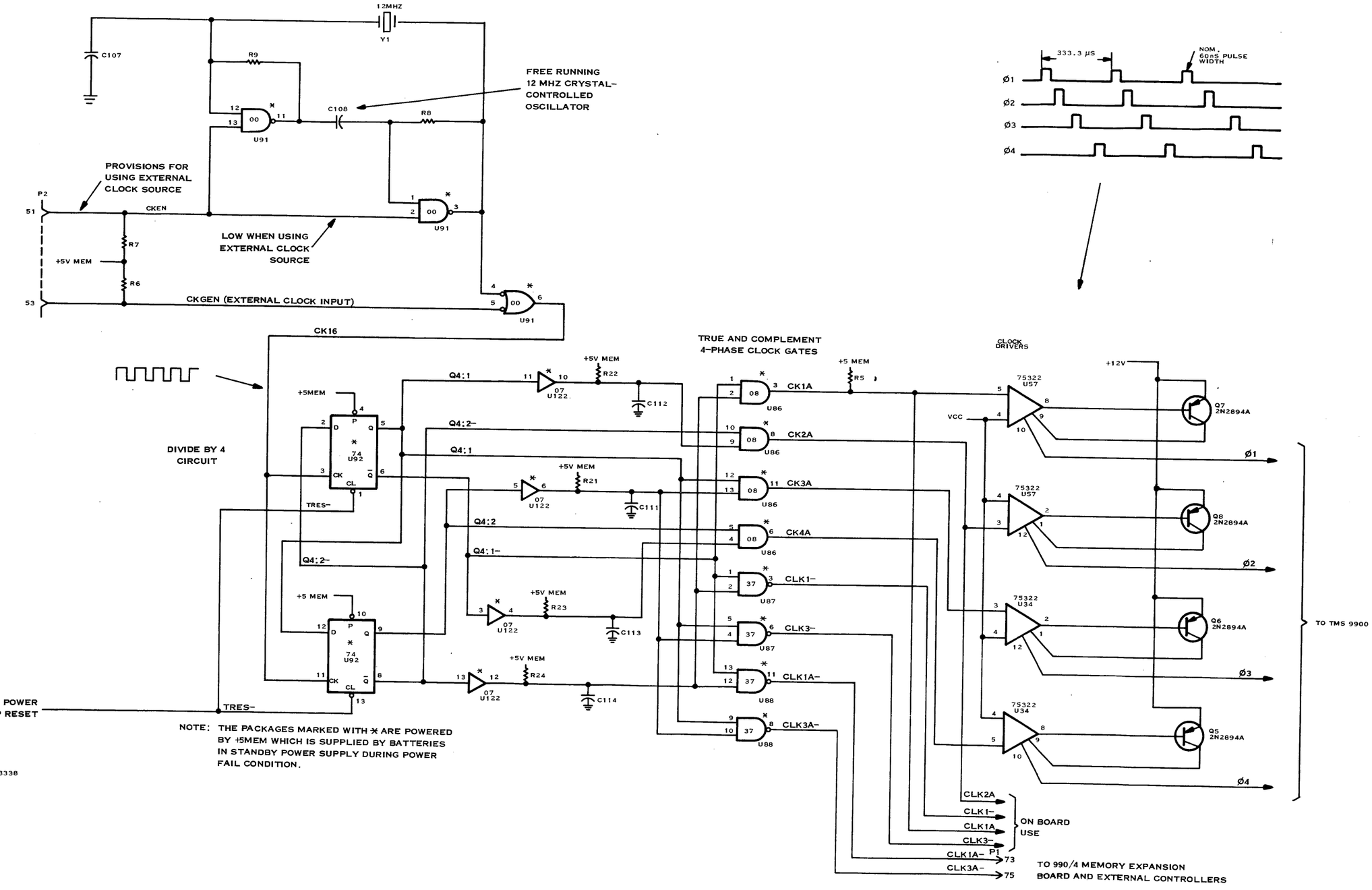


Figure 7-13. 4-phase Clock Logic, Simplified Logic Diagram

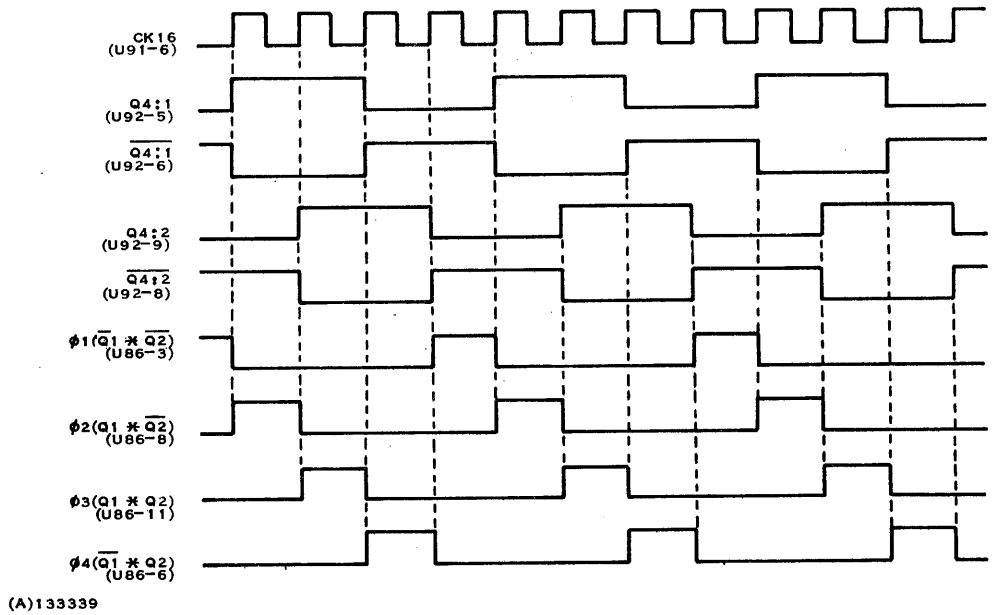
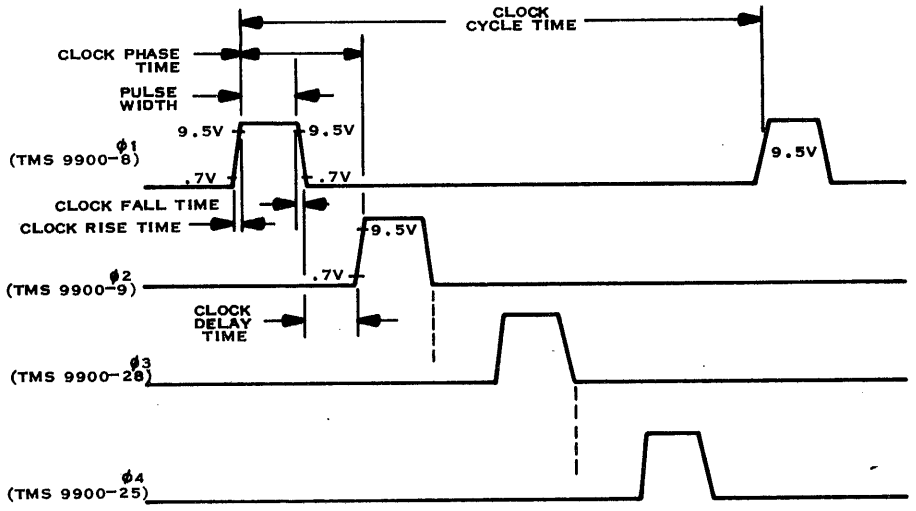


Figure 7-14. 4-Phase Clock Timing Diagram



	MINIMUM	NOMINAL	MAXIMUM
CLOCK RISE TIME	7ns	10ns	50
CLOCK FALL TIME	7ns	10ns	50
PULSE WIDTH	50ns	65ns	*
CLOCK DELAY TIME	5	18ns	*
CLOCK PHASE TIME	80	83ns	*
CLOCK CYCLE TIME	333	333.3ns	333.35

* MAX TIME IS A FUNCTION OF SEVERAL PARAMETERS AND CANNOT BE SPECIFIED INDIVIDUALLY. IN GENERAL, PULSE WIDTH AND CLOCK DELAY CANNOT BE SUCH THAT CLOCK EDGES OVERLAP.

(A)133340

Figure 7-15. 4-Phase Clock Specifications

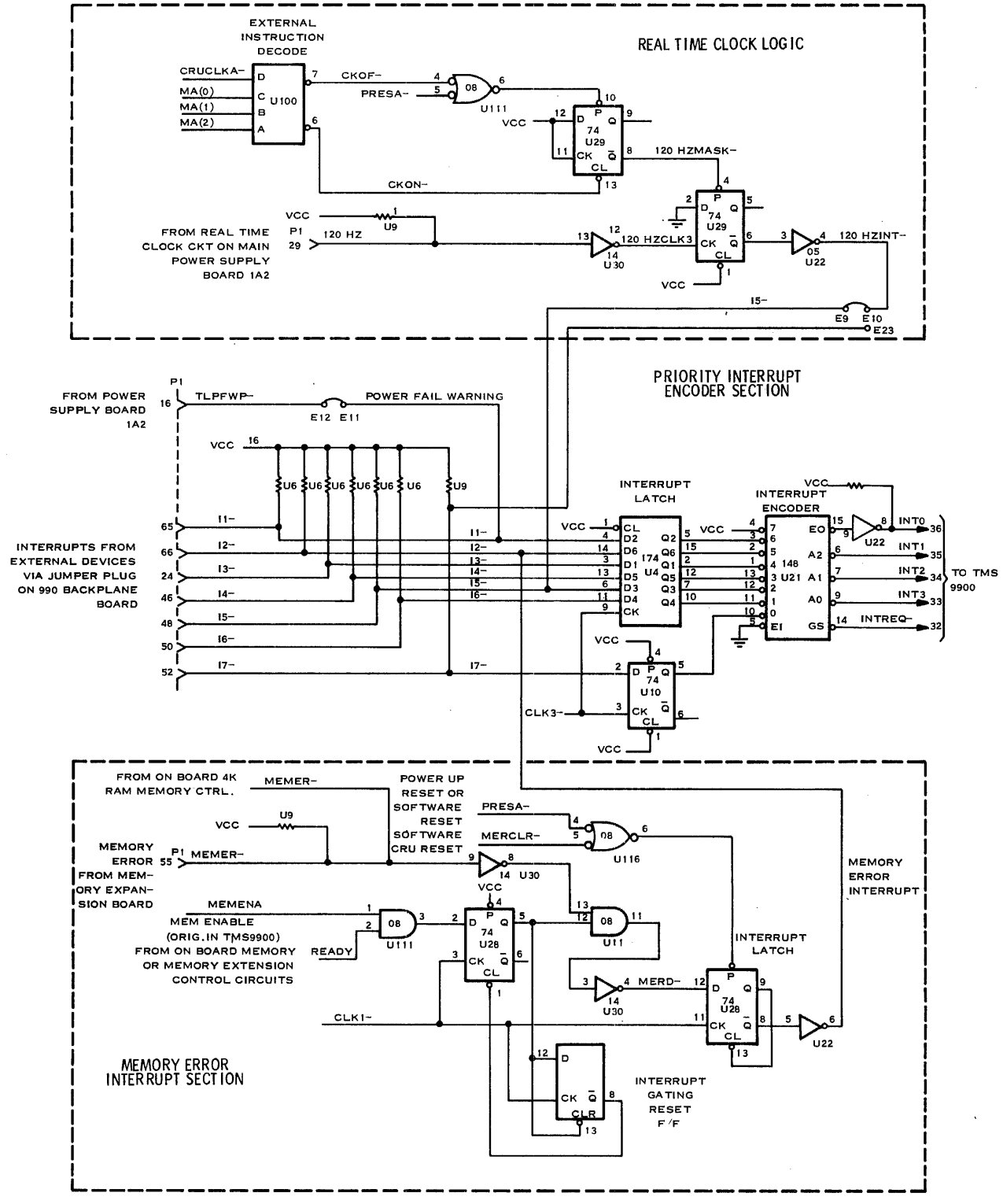


Figure 7-16. Real Time Clock/Interrupt Section, Simplified Logic Diagram

Table 7-1. 990/4 Microcomputer Board Checkout Procedures

Step	Procedure	Normal Indication	If Abnormal
1	Set key switch on programmer panel to LOCK position. Set battery switch to ON position. Set key switch to OFF position thereby operating board on standby power supply batteries.	–	–
2	Connect channel 1 scope probe to pin 7 of any memory chip in the 4K RAM memory. Connect channel 2 probe to RFACC– (U112-8).	CEN– (Pin 7, any memory chip) RFACC– (U112-8)	See memory troubleshooting section in table 7-2.
3	One at a time, connect channel 2 probe to address lines A7-A14 on any memory chip.	AD(7-14) address lines toggle	Same as above.
4	Connect channel 1 to phase 1 clock (TMS 9900-8). Connect channel 2 to phase 2 clock (TMS 9900-9).	See figure 7-15.	See 4-phase clock troubleshooting section in table 7-2.
5	Connect channel 1 to phase 3 clock (TMS 9900-28).	See figure 7-15.	Same as above.
6	Connect channel 1 probe to phase 4 clock (TMS 9900-25).	See figure 7-15.	Same as above.
7	Insert the cassette containing RAM04 diagnostic (Part Number 945440) into 733 ASR cassette transport (see Section IV).	–	–
8	Set KEYBOARD, PLAYBACK and PRINTER switches on 733 to LINE position (see figure 4-3).	–	–
9	Set 733 ASR POWER switch to ON position. Set ON LINE switch to ON LINE position. Press REWIND for associated transport and wait for END indicator to light.	733 END indicator lights	–
10	Press LOAD/FF and wait for READY indicator to light.	When tape is positioned at the starting point, READY indicator lights.	–
11	Set key switch on programmer panel to UNLOCK position. Press HALT/SIE switch.	RUN light extinguishes.	–
12	Press LOAD switch on programmer panel.	Cassette begins moving under software control. When load is complete, ID message prints out and cassette halts. Program execution then begins.	
13	Examine 733 printout for test results.	Printout indicates additional parameters which must be input through the 733 keyboard and indicates the test results.	

Table 7-1. 990/4 Microcomputer Board Checkout Procedures (Continued)

Step	Procedure	Normal Indication	If Abnormal
14	Permit the diagnostic to run until five normal completions are obtained.	5 normal completions, no error message printouts.	See table 7-3.
15	Press REWIND on 733 to rewind diagnostic tape.	Tape rewinds and halts	–
16	Open door and remove cassette from 733 ASR.	–	–
17	Repeat steps 7-16 for AU04 diagnostic (Part Number 945434).	Same as 7-16.	Same as 14.
18	Repeat steps 7-16 for ROMVER diagnostic (Part Number 945443).	Same as 7-15.	Same as above.
19	Repeat steps 7-16 for CRUTST04 diagnostic (Part Number 945446).	Same as 7-15.	Same as above.

7.3.2 **TROUBLESHOOTING SCOPING LOOPS.** Once a malfunction has been identified through the use of the diagnostic tests in the checkout chart, a scoping loop program is then entered into the computer memory via the programmer panel which permits a single (or group) of instructions to be continuously executed. This procedure then permits various circuit conditions to be tested to isolate the malfunction down to a replaceable component level. Several commonly used scoping loops are described in the following paragraphs.

7.3.2.1 **Read Followed by Write at Single Address.** The following program may be used to loop on a single address within the RAM memory space:

MEM Location	Machine Code	Comments
0900	02E0	LWPI, 100
0902	0100	
0904	0208	LI R8, LOC
0906	LOC	Desired loop address (0000 to $1FFE_{16}$)
0908	0209	LI R9, DATA
090A	DATA	Selected data pattern
090C	C609	MOV R9, *R8
090E	10FE	JMP $-1

Table 7-2. 990/4 Microcomputer Board Fault Isolation Procedures

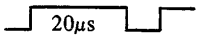
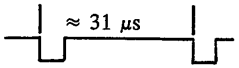
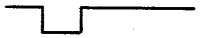
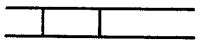
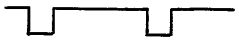
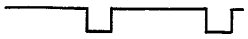
Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
1	Memory refresh inoperative in 4K RAM section	Faulty refresh oscillator stage	Connect channel 1 scope probe to OSC (U108-3).	OSC (U108-3) 	Replace U108.
		Faulty refresh timing stage	Connect channel 1 probe to RFACC– at U112-8.	RFACC– (U112-8) 	See figures 7-7 and 7-8 and check inputs and outputs of following stages: U110, 111, 112.
		Loss of 4-phase clocks	See steps 3 and 4		
		Faulty memory timer (chip enable generator)	Connect channel 1 probe to RFACC– (U112-8). Connect channel 2 probe to CEN– (pin 7 of any memory chip).	RFACC– (U112-8)  CEN– (pin 7, 4K RAM) 	See figures 7-7 and 7-8. Check inputs and outputs to following stages: U95, U96, and U107.
		Faulty refresh address counter or address multiplexer	Connect channel 1 probe to CEN– (pin 7 of any RAM chip). Connect channel 2 probe to each of the following address lines on any 4K RAM chip: A7-A14 (pins 3-5, 8, 9, 11-13).	CEN– (pin 7)  AD(7-14)  All address lines should toggle just outside the chip enable window.	Check A inputs to MPX stages U102, U101. If inputs are not toggling, replace U117 and/or U118. If normal, replace U101 and/or U102. If address lines toggling within CE window, check timing circuits in accordance with figure 7-8.
2	Unable to access 4K RAM – Ext memory and 1K mem normal (Multiple address failures in 0000 to 1FFE range).	Address decode failure (refer to figures 7-7 and 7-9).	Set up a scoping loop to read and write into suspect address (see paragraph 7.3.2.1). Connect channel 1 to ADROK4– (U110-12).	ADROK4– (U110-12) 	Refer to figures 7-7, 7-8 and check inputs and outputs of following stages: U110, U113, and U97.
		Faulty address mpx	Check each input and output address line to ensure that MPX is switching from refresh address to user address. Also, ensure that the address lines are not changing during CE time.	When RFACC– is high (U112-8), MPX switches to user address lines for AD(7-14).	Replace U101 and/or U102.
		Two way bus control logic inoperative	Connect channel 1 probe to DOUT– (U82-8). Connect channel 2 to DIN– (U82-11).	DOUT– U82-8  DIN– U82-11 	Check inputs to the same two gates (ARDOK4, DBINA– and DBINA) (figure 7-9). If normal, replace U82. If abnormal, check source of input signals (U19, U94, U84).
		Tri-state bus stage inoperative.	Check the data on the processor side of the bus when DOUT– is active. Similarly check data on memory side of bus when DIN– is active.	Data should be same as data entered in scoping loop – paragraph 7.3.2.1.	Replace faulty tri-state driver stage U42, 41, 63 or 80.

Table 7-2. 990/4 Microcomputer Board Fault Isolation Procedures (Continued)

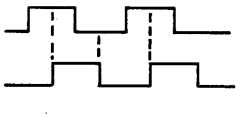
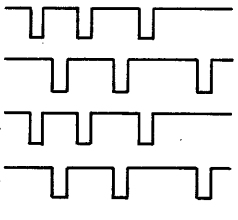
Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
3	4-phase clock inoperative (both true and complement outputs)	Faulty oscillator stage	Connect scope to output of crystal-controlled oscillator (U92-3). Reference figures 7-13 and 7-14.	16 MHz pulse train	Check clock enable to U91-2. If enable is high, replace U91 and/or Y1.
		Clock divider stage inoperative	Connect channel 1 probe to U92-5. Connect channel 2 to U92-9.	Q4:1 (U92-5) Q4:2 (U92-9) 	If pulse train is not observed, check logic-level on clear inputs to both flip-flops (92-1, 13). If high, replace U92.
		Clock buffer inoperative	Check outputs of buffer stage U122 (pins 4, 6, 10, 12)	Pulse train outputs	Replace U122.
4	Loss of 4-phase clocks to 9900; bar clocks normal	Faulty clock gating circuit (U86)	Check outputs at U86, pins 3, 6, 8, and 11.	See figure 7-14.	Replace U86.
		Faulty clock driver stage	Check to see if more than one output driver is inoperative (loss of +12 vdc would disable all drivers).	See figure 7-15.	Replace faulty transistor and/or differential driver stage.
5	Loss of bar clocks, other clocks normal	Defective gate in U87 or U88 package	Check inputs and outputs to gates in U87 and U88.	CLK1– U87-3 CLK3– U87-6 CLK1A– U88-11 CLK3A– U88-8 	Replace U87 and/or U88.
6	Single Bit errors in one or more 4K RAM memory locations.	Faulty memory chip	Replace 4K chip corresponding to failing bit position: Bit 0 - U44 Bit 8 - U66 Bit 1 - U45 Bit 9 - U67 Bit 2 - U46 Bit 10 - U68 Bit 3 - U47 Bit 11 - U69 Bit 4 - U48 Bit 12 - U70 Bit 5 - U49 Bit 13 - U71 Bit 6 - U50 Bit 14 - U72 Bit 7 - U51 Bit 15 - U73	Bit errors disappear when chip is replaced	See next substep
		Faulty two-way bus chip	If problem persists when memory chip is replaced, replace two-way bus chips corresponding to failing bit position: Bits (0-3) - U41 and U42 Bits (4-9) - U63 and U64 Bits (10-15) - U80 and U121	Bit errors disappear when chip is replaced	See next substep

Table 7-2. 990/4 Microcomputer Board Fault Isolation Procedure (Continued)

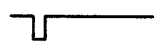
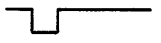
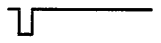
Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
6	(Continued)	Faulty pull-up stage associated with bit position.	If problem persists, replace pullup associated with bit position: Bits 0-14 - U65 Bit 15 - R19 Parity - R20		
7	Failure of 1 or more internal 9900 instructions.	4-phase clock out of tolerance or faulty TMS 9900.	Check 4-phase clocks to the TMS 9900 in accordance with figure 7-13. If clocks are within tolerance, replace TMS 9900 (U36).		
8	Unable to get programmer panel out of RUN mode.	Faulty restart initiate circuit	Connect scope to LOAD– (U114-10), set key switch on panel to OFF, then to UNLOCK position and press HALT/SIE switch.	U114-10 (LOAD–) 	See figure 7-4, sheet 4 and figure 7-3. Check inputs and outputs to following stages: U98, U115, and U30. Remove and replace faulty component.
		Faulty 1K ROM/RAM memory section	Set key switch to OFF and back to LOCK position. Observe 1K RAM address and control signals.	TMS 9900 addresses FFFC. ADROK1– and CEN3– are generated each time power is turned on.	See figure 7-10, 7-11 and logic drawing 944911, sheet 4 and replace faulty chip (U93, U12, U22, U24, U25).
		Faulty TMS 9900	Replace TMS 9900 if above steps are good.		
9	Panel fails to return to HALT mode when SIE is executed.	Faulty restart initiate circuit	Connect channel 1 to LOAD– (U114-10). Connect channel 2 to SIECLK–. Set key switch to OFF and back to UNLOCK position. Press HALT/SIE switch. Then while observing scope, press HALT/SIE switch a second time.	LOAD– (U114-10)  SIECLK– 	See figures 7-3 and 7-4(d). Check inputs and outputs to following stages: U98, U99, U114, U116, U113. If SIECLK– absent, replace U104.
10	Unable to send or receive data from panel. RUN light will extinguish.	Loss of CONSEL– or faulty panel software ROM.	Connect scope to CONSELA– (U109-9).	Periodically goes low.	Replace U109.
		Loss of STORECLK–	Check output of U107-6. Press a data switch on the panel.	STORECLK– goes low.	Replace U107 and/or U33.
11	RUN LED fails to light when RUN switch is pressed on programmer panel.	Faulty CRU decoder stage	Connect scope to U104-13. Press RUN switch on panel (key switch in UNLOCK position).	RUNCLK– temporarily goes low.	Replace U104.
12	FAULT LED lights on programmer panel, unable to load diagnostic.	Faulty loader ROM, TMS 9900 or memory.	Set programmer panel key switch to UNLOCK position and press HALT/SIE switch.	RUN LED extinguishes.	See step 8. If RUN LED extinguishes, go to next substep.

Table 7-2. 990/4 Microcomputer Board Fault Isolation Procedure (Continued)

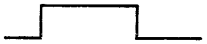
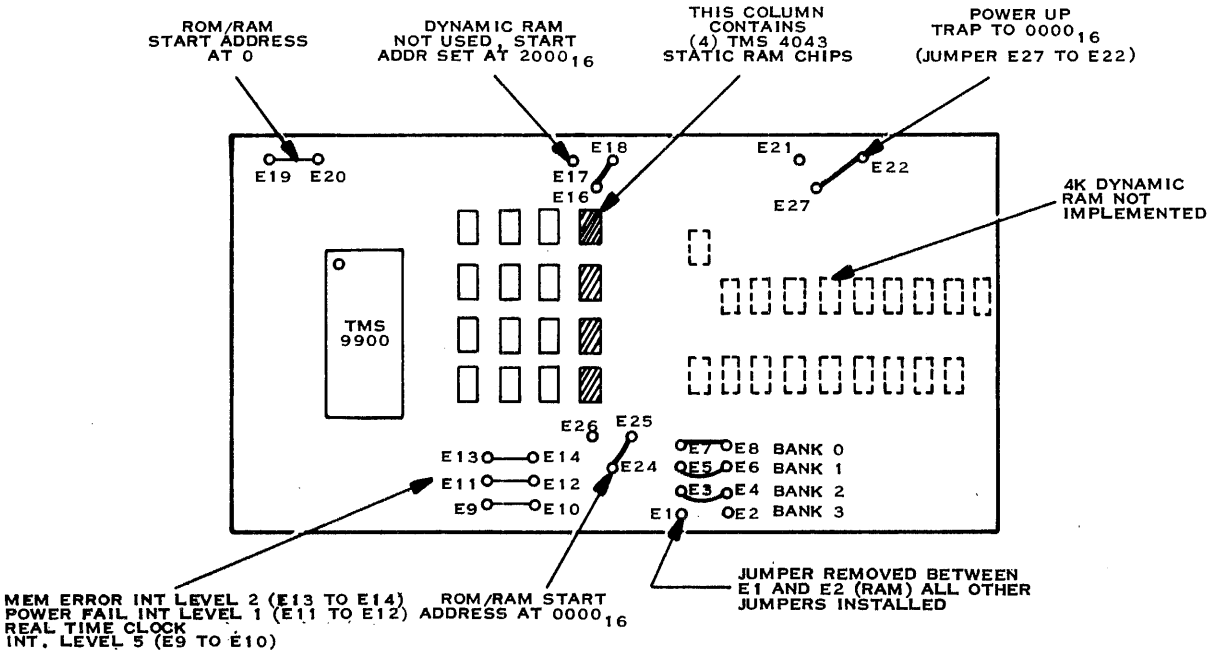
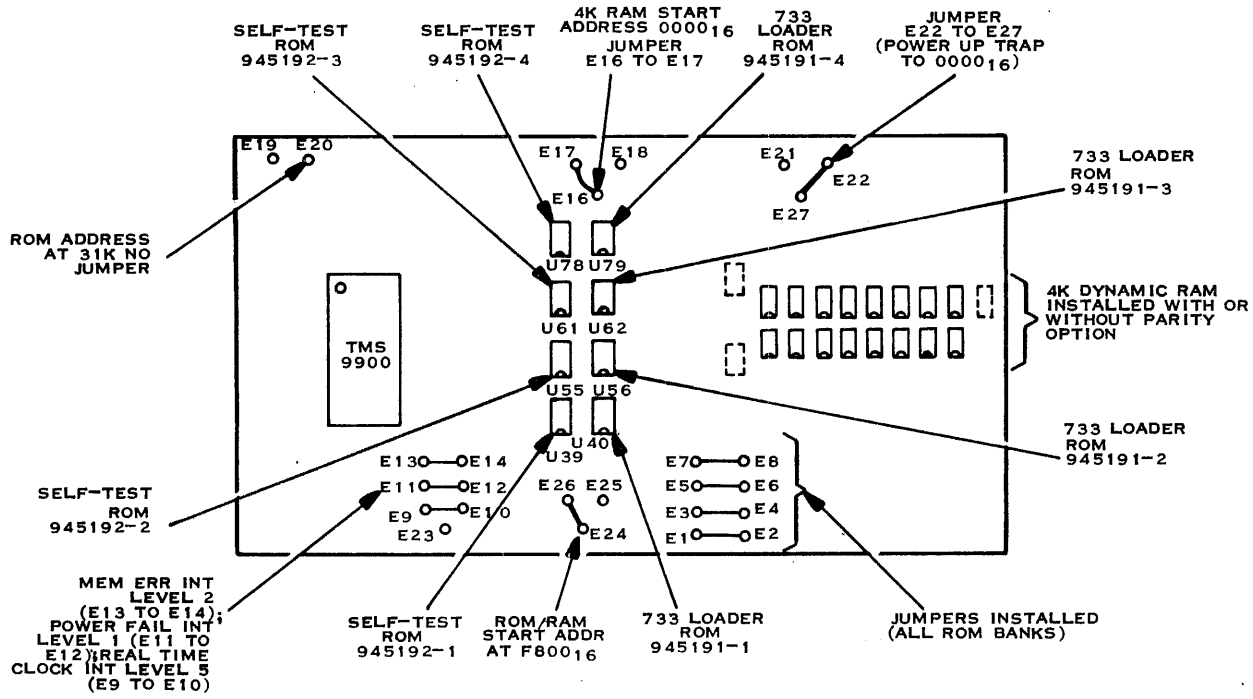
Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
12	(Continued)		Manually enter a value into any selected onboard RAM memory location and then display the contents of the same memory location.	Data can be entered and retrieved from onboard RAM memory.	Go to step 2. If onboard cycle can be performed, go to next substep.
			Display the value stored in memory location $FFFC_{16}$.	0080_{16}	Proceed to step 13. If normal, proceed to next substep.
			Replace self-test loader ROM and attempt another diagnostic load operation.	Diagnostic loads into program memory and program execution begins. RUN LED lights and test results printout on 733.	Replace TMS 9900 stage U36.
13	1K PROM/static RAM memory inoperative; 4K RAM normal.	Faulty address decode or chip enable decode stage.	Set up read scoping loop at memory address $FFFC_{16}$ in accordance with paragraph 7.3.2.2. Connect channel 1 probe to ADROK1– at U93-6. Connect channel 2 probe to MEMENA (U93-3). Sync on channel 1.	ADROK1– (U93-6)  MEMENA (U93-3) 	Check jumper wire connections in accordance with figure 7-17. If jumpers normal, check inputs/outputs to U93, U22, and U12. Remove/replace faulty stage. If normal, replace U25.
14	Loss of all interrupts.	Faulty interrupt register, interrupt encoder, or microprocessor.	Connect ground jumper to E11. Check level 1 output of interrupt register stage U4-5.	Logic 0	Replace U4.
			Check outputs of interrupt encoder stage U21.	(U21-15) – Logic 1 (U21-6) – Logic 0 (U21-7) – Logic 0 (U21-9) – Logic 1 (U21-14) – Logic 0	Replace U21. If normal, check U22-8 for logic 0 value. If normal, replace TMS 9900 stage U36.
15	Loss of real time clock interrupts, all other interrupts normal.	Faulty external instruction decode or clock interrupt mask stage.	Manually execute a CKON instruction from programmer panel by storing $03A0_{16}$ in memory location 0100_{16}, loading program counter with 0100_{16} and pressing HALT/SIE. Connect channel 1 scope probe to U29-4.	120HZMASK (U29-4) – Logic 1	Replace U100 and/or U29. If normal, proceed to next substep.
			Manually execute a CKOF external instruction (op code $03C0_{16}$).	120HZMASK (U29-4) – Logic 0	Replace U100, U11, or U29. If normal, proceed to next substep.
		Faulty real time clock interrupt flip-flop or input inverter stage.	Connect channel 1 probe to 120HZCLK (U30-12).	→|≅8 ms|← 120HZCLK (U30-12) 	Replace U30. If normal, proceed to next substep.

Table 7-2. 990/4 Microcomputer Board Fault Isolation Procedure (Continued)

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
15	(Continued)		Temporarily ground U29-13. Connect scope to U4-6.	I5– (U4-6) – Logic 0	Check for jumper between E9 and E10. If present, check output of U29-6. If logic 0, replace U22. If logic 1, replace U29.



(A) MACHINE CONTROLLER CONFIGURATION (944910-1)



(B) GENERAL PURPOSE COMPUTER CONFIGURATION (944910-2)

(B)133342

Figure 7-17. 990/4 Microcomputer Board, Standard Configuration

This program will continuously read and write the data specified by memory location 0908 into the address specified by 0906. The scoping loop program may be entered into computer memory using the following procedure:

1. Set the key switch on the programmer panel to the UNLOCK position.
2. If the RUN LED is lit, press the HALT/SIE switch to halt the processor and begin execution of the programmer panel code. When the panel is active, the RUN LED is extinquished.
3. Press the CLR switch to clear the panel's display register.
4. Press the ENTER ST (enter status) switch to clear the status register in the TMS 9900.
5. Set up 0900_{16} on the data display LEDs using the data entry switches. This is the address in memory where the first instruction of the scoping loop is to be stored.

NOTE

When a data display LED is lit, it indicates a "1".

6. Press ENTER MA switch to load the memory address value 0900 into the memory address register of the TMS 9900.
7. Press CLR to clear the displays for the next entry.
8. Set up the instruction code ($02E0_{16}$) on the data LED displays using the data entry switches.
9. Press MDE switch which causes 02E0 to be loaded into memory location 0900.
10. Press MAI which increments the memory address value stored in the memory address register and repeat steps 8-11 to enter the following program values into successive memory locations:
    - 0100
    - 0208
    - Address on which the test will loop (0000 to 1FFFE inclusive)
    - 0209
    - Data to be written into the looped memory location (e.g., $1F1F_{16}$)
    - C609
    - 10FE

11. Press CLR to clear the displays.

12. Enter 0900 into the displays (address of first instruction in the scoping loop).

13. Press ENTER PC to load the value into the program counter.

14. Press RUN to begin execution of the program. The RUN LED should light to indicate proper operation.

NOTE

If the RUN LED fails to light, return to step 1 and repeat the program setup procedure.

7.3.2.2 **Continuous Read From Selected Memory Location.** The basic scoping loop program described in 7.3.2.1 may be modified to perform a continuous read at a selected memory extension address by changing the instruction at memory location 090C in the previous program from C609 to C258 which is a MOV *R8,R9 instruction. This change to the basic program causes data to be read from a selected address and stored in memory location 0112 (workspace register 9). For maintenance purposes, the scoping loop may be interrupted at any time and the value stored in the workspace register may be examined using the following procedure:

1. Halt the processor by pressing HALT/SIE. The RUN LED should extinguish.

2. Press CLR to clear the displays.

3. Enter 0112 into the displays using the data entry switches.

4. Press ENTER MA to load 0112 into the memory address register.

5. Press MDD. The resulting value displayed on the panel LEDs should be the same value stored in memory location 990A of the scoping loop program.

7.3.2.3 **Scoping Loop for a Band of Memory Addresses.** The basic scoping loop program may also be modified as follows to permit looping over a band of memory addresses in which the beginning and ending addresses are specified in the program:

Scoping Loop for Reading Band of Memory Addresses

MEM Location	Machine Code	Comments
0900	02E0	LWPI >80
0902	0100	
0904	020A	LI R10, ENDLOC
0906	ENDLOC	Ending address +2
0908	0209	LI R9, DATA
090A	DATA	
090C	0208	LI R8, LOC
090E	LOC	
0910	CE09	MOV R9, *R8+
0912	820A	C R10, R8
0914	14FB	JHE
0916	10FC	JMP

The procedures for entering this program into computer memory are essentially the same as described in paragraph 7.3.2.1.

SECTION VIII

990/4 MEMORY EXPANSION BOARD TROUBLESHOOTING DATA

8.1 GENERAL

This section provides troubleshooting data required to troubleshoot malfunctions on the 990/4 memory expansion board (Part Number 944935) down to the replaceable component level.

8.2 CIRCUIT BOARD ANALYSIS

The 990/4 memory expansion board contains seven major sections including:

- Memory address section
- Control section
- Two way data bus
- Chip select drivers
- Memory storage section (up to five 4K memory banks)
- Parity function (optional)
- Write protect section

A simplified functional block diagram of the memory expansion board showing all interface signals and pin numbers is provided in figure 8-1. A brief functional description of each major section is presented in the following paragraphs.

8.2.1 MEMORY ADDRESS SECTION. The memory address section provides the following functions:

- Modifies the three most significant bits of the incoming address (ADR 0-2) according to the bias set up on switches S2-S4 to permit the board's starting address to be set at any 4K boundary between 0 and 28K (see figure 8-2).
- Compares the "biased" user address against the maximum amount of memory implemented on the board (indicated by jumper wires) to determine if the user address falls within the address space of the memory expansion board.
- If a valid user address is detected and a protect violate is not indicated by the write protect section (write cycles only), the address section generates an address OK (ADOK) which is used by the control section to initiate memory cycles.
- Contains a multiplexer stage which permits a refresh address to be substituted for the user address during memory refresh cycles.

A simplified block diagram of the memory address section is provided in figure 8-2.

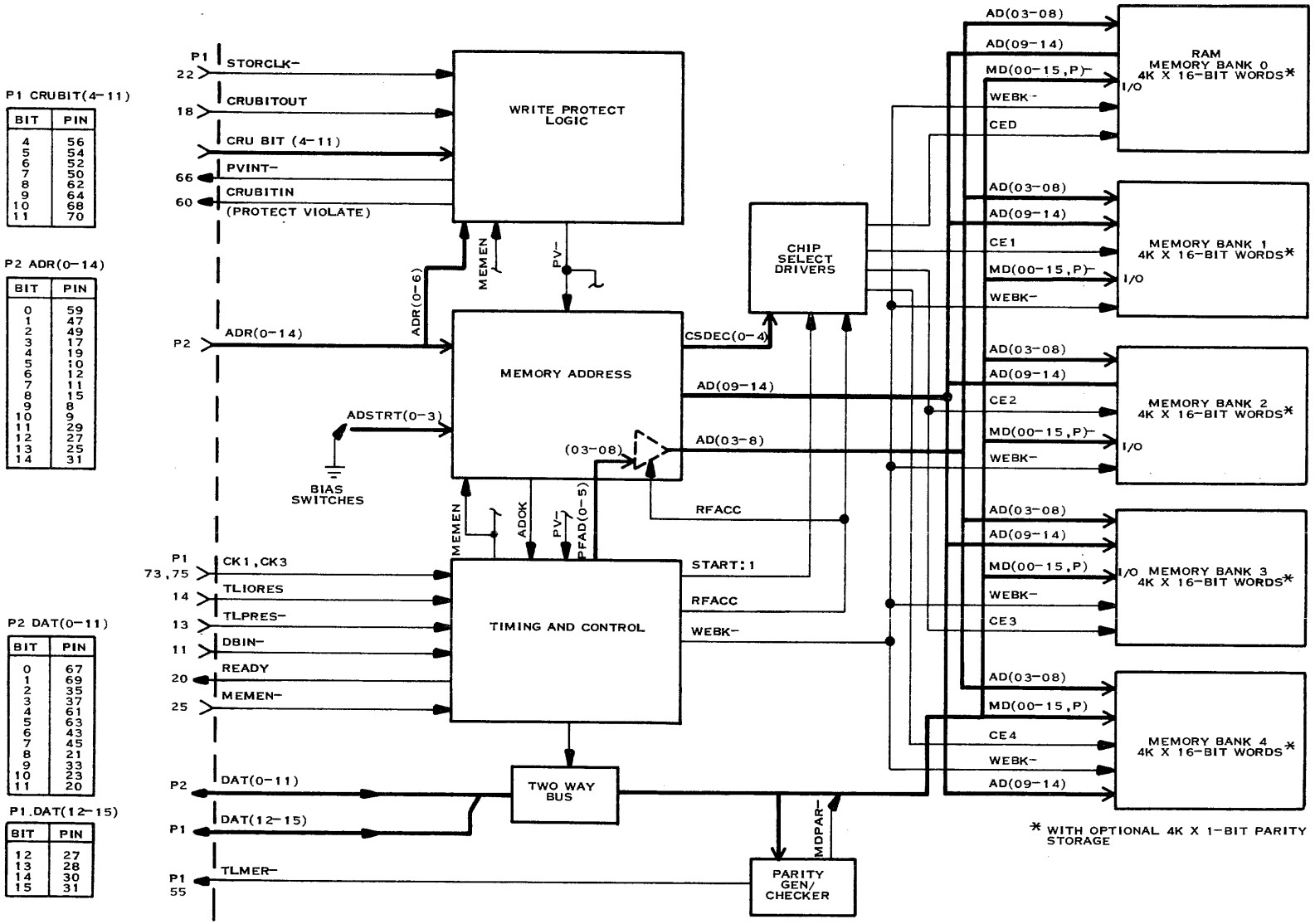


Figure 8-1. 990/4 Memory Expansion Board, Block Diagram

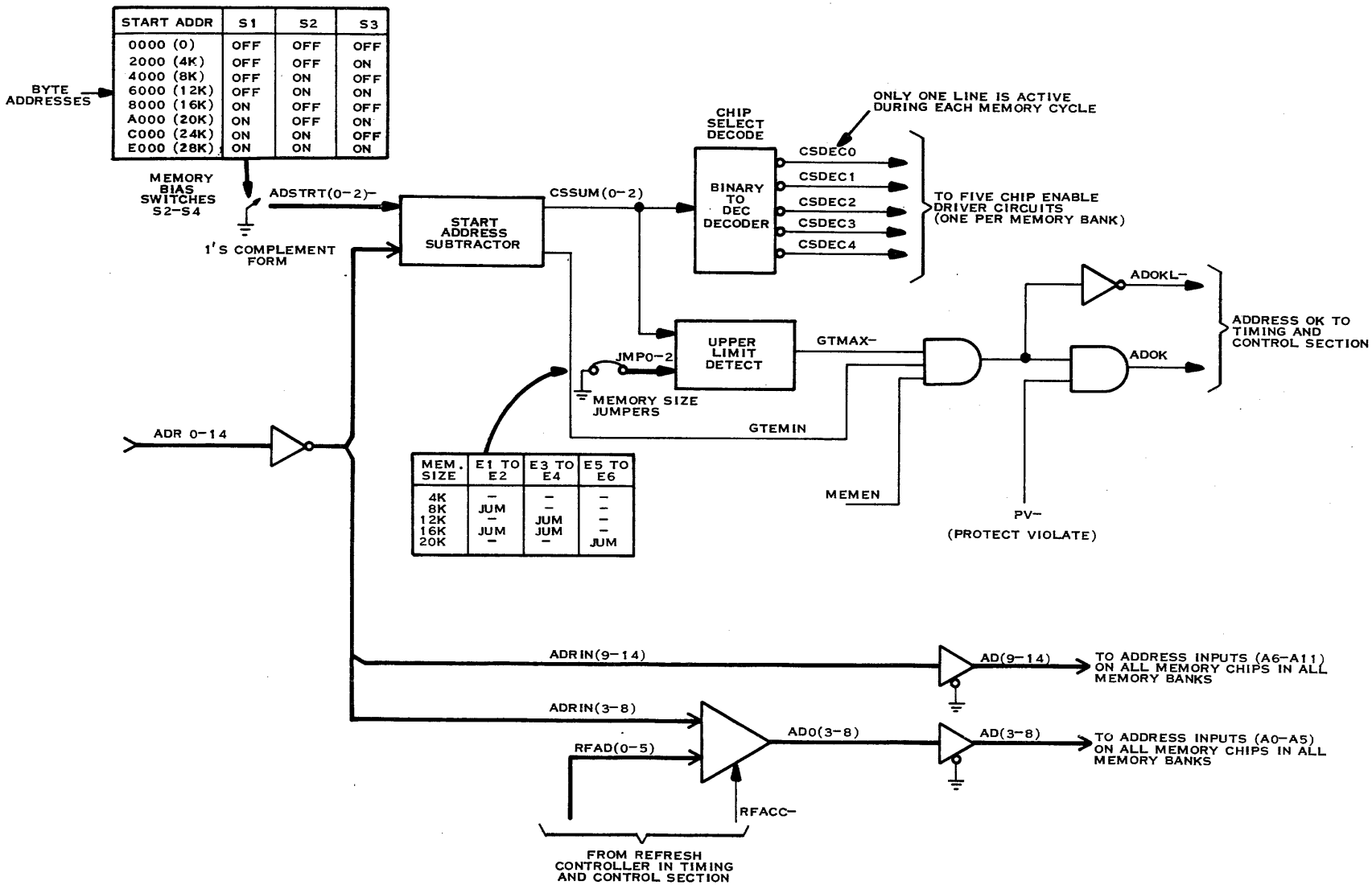


Figure 8-2. Memory Address Section, Block Diagram

8.2.2 **WRITE PROTECT SECTION.** The write protect section performs the following functions on the 990/4 memory expansion board:

- Provides storage for the upper and lower bounds of the memory space locked out to a write operation (protected bounds has 256-word granularity).
- Provides storage for a write protect bit which permits software to easily switch from protected to unprotected mode of operation.
- Monitors Address bits 0-6 during each memory write cycle (write indicated by logic high DBIN– signal) and generates a protect violate signal (PV–) if the user address falls within the protected address space when the protect bit is set in the bounds register.
- Sets a flip-flop when protect violate occurs. Provisions are also included to permit software to interrogate the flip-flop via the CRUBITOUT line. The PV flip-flop may be reset by either the TLIORESET from the 990/4 or by an LDCRU instruction from 990/4 software which toggles the high order protect bit (Bit 00).
- The output of the PV flip-flop also generates an interrupt (PVINT–) when protect violate is detected. Use of this interrupt is optional.

A simplified logic block diagram of the write protect section is provided in figure 8-3. The operation of this section is briefly described in the following paragraphs.

8.2.2.1 **Bounds Register.** The bounds register is a 16-bit register used to store the write protect bit and the upper and lower bounds vector word from the 990/4. The register is initially cleared by the I/O Reset signal from the 990/4 board (TLIORST–). The TMS 9900 software must then initialize the protect bounds register prior to the first memory write cycle by executing a "Load CRU" instruction addressed to the memory expansion board. The CRU address is decoded to generate MODSEL– which is gated with the inverted store clock (STORCLK–) from the 990/4 board to serially clock the protect information from the CRUBITOUT line into the bounds register.

MODSEL– also enables the output of the protect violate flag onto the CRUBITIN line to permit software to interrogate the flip-flop.

The output of the bounds register is compared with user address bits 0-6 from the memory address bus during each memory write request to determine if the protected space is being addressed. If so (and the write protect bit is set), a protect violate signal is generated (PV–) which sets the protect violate latch, generates a protect violate interrupt (PVINT–) to the 990/4 board and inhibits the generation of address OK (ADOK) required to initiate a memory cycle.

The protect violate latch may then be read under software control by addressing the memory expansion board with a read CRU instruction. The protect violate latch is cleared under software control by toggling bit 0 of the bounds register via a CRU instruction.

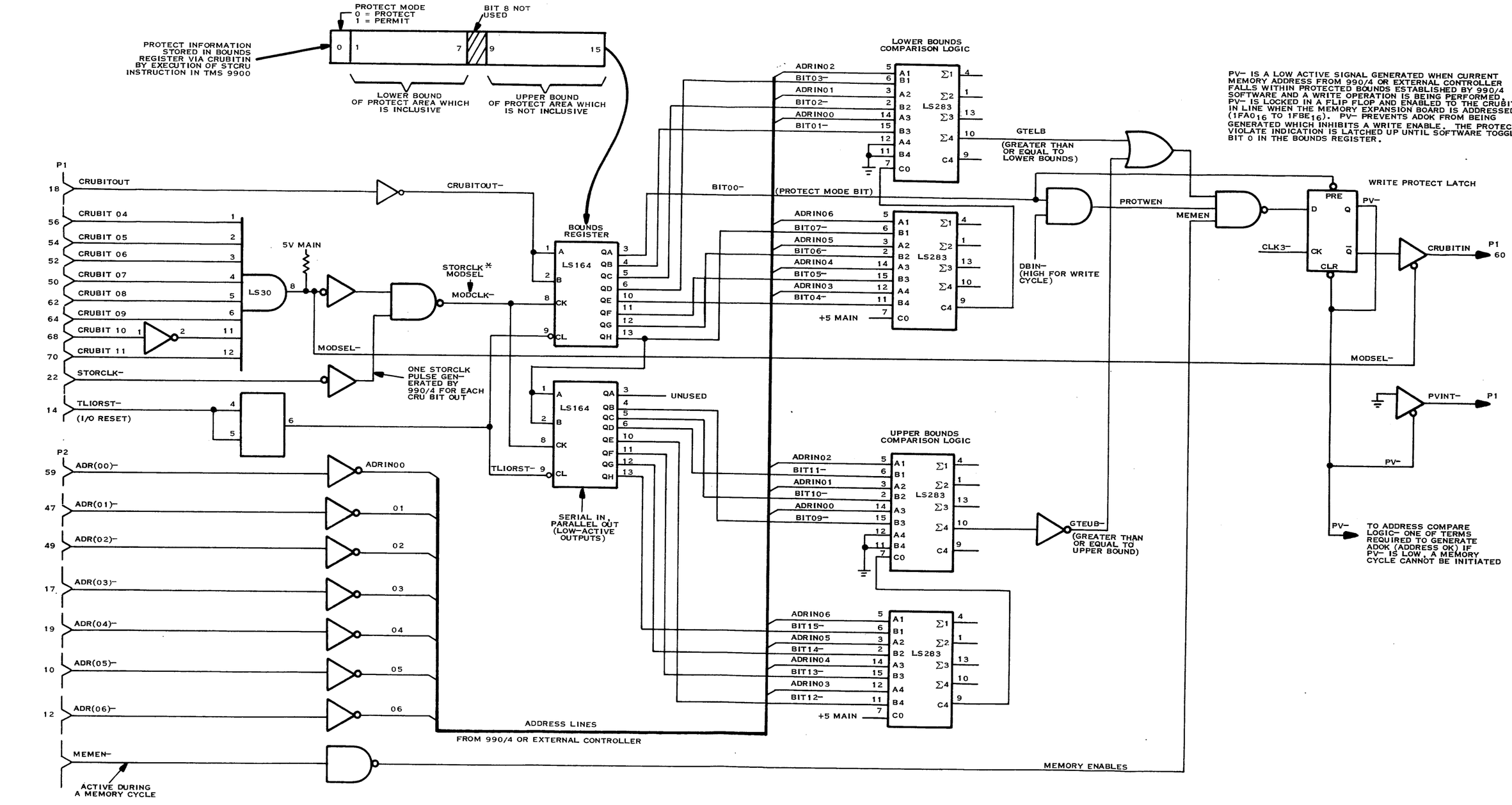


Figure 8-3. Write Protect Logic, Simplified Logic Diagram

8.2.3 **MEMORY TIMING AND CONTROL SECTION.** The memory timing and control section monitors signals from the address and write protect sections plus the control signals from the memory user (TMS 9900 or external DMA controller) and, in turn, generates the timing pulses required to initiate memory cycles. This section also periodically initiates memory refresh cycles to prevent loss of data due to the inherent data decay characteristics of the MOS memory chips. For the following discussion of the timing and control section, refer to logic diagram 944937, sheet 7, in the *990 Family Maintenance Drawings Manual* and the associated timing diagram in figure 8-4.

8.2.3.1 **Memory Read Cycle.** A memory read cycle is initiated by a logic low START– pulse at the $\overline{Q}$ output of U43-6. This signal goes low on the trailing edge of a phase 3 clock pulse (CLK3–) after an address OK (ADOK–) is generated by the memory address section. ADOK– indicates that a reset is not being performed, a memory enable has been supplied by the memory user, and that the address on the memory address lines falls within the address space of the memory expansion board. The START– signal is inverted to form START:1 which is a high-active signal used to clock the chip enable flip-flops. One of the five chip select flip-flops (one per 4K memory bank) will be supplied with a low-active chip select decode which indicates that the address space has fallen within that particular 4K memory bank. As a result, a +12 volt positive-going chip enable pulse is sent to all memory chips in the selected memory bank (see paragraph 8.2.4 for a detailed description of the chip enable drivers).

During the period of time that the chip enable is applied to the memory chips, the address lines to the memory chip must be stable. Valid read data is available on the two-way data bus at the trailing edge of the next phase 3 clock. DBINA which is the double inverted form of DBIN from the memory user, is used to set up the 2-way bus for a read operation.

As shown in figure 8-4, the START output is also applied to the data input of the "start delayed" flip-flop (U43-12). Therefore on the trailing edge of the second phase 3 clock (start flip-flop was set on the trailing edge of the first clock pulse), STRTDLY is generated. When START is cleared, STRTDLY clears thereby generating (MCYEND–) at the output of U45-6. This signal presets the chip enable flip-flop to terminate the chip enable signal to the memory chips and also resets the start flip-flop. Additionally, memory cycle end is used to gate the output of the parity checker to the parity error flip-flop stage, U12.

If a parity error is detected at the end of a memory read cycle, memory error (TLMER–) goes low which is sent to the 990/4 microcomputer board where it is wire-ORed with the memory error signal from the 990/4 board's 4K RAM and any additional memory expansion boards used in the system. The memory error signal results in a level 2 interrupt being sent to the TMS 9900.

8.2.3.2 **Memory Write Cycle.** A memory write cycle is initiated in a manner similar to the read cycle previously described except that ADOK– also indicates that the write cycle is not taking place in a protected address (provided the write protect option is installed on the board and the write protect bit (bit 0) indicates write protect mode). If an attempt is made to write in a protected location, ADOK– will not be generated and a memory cycle cannot be initiated. The START signal is also gated with refresh access, DBIN– and PRES– to generate a low active write enable (WEBK–) which is routed to all memory chips.

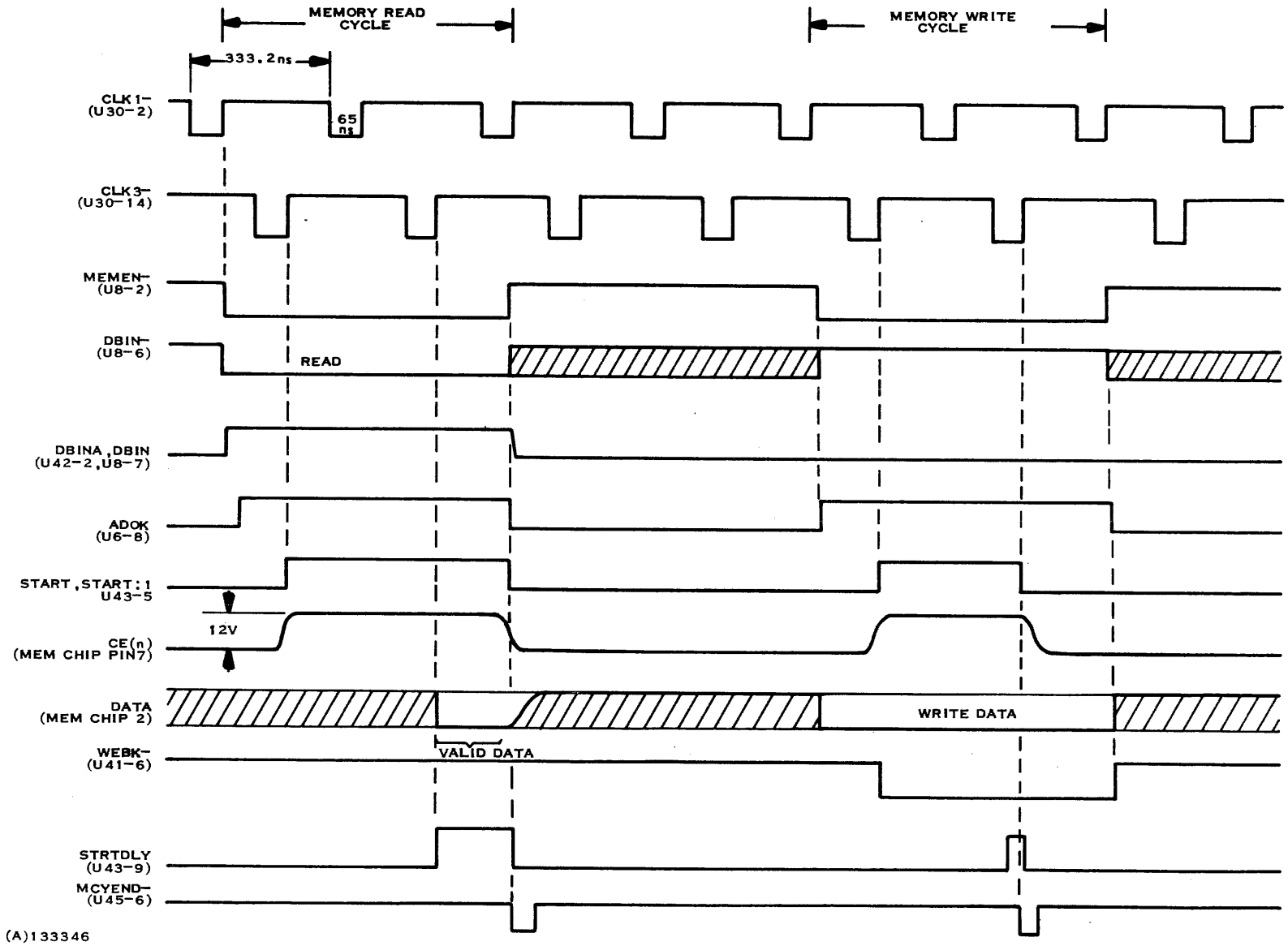


Figure 8-4. Memory Read Followed by Memory Write Cycle, Timing Diagram

During a write cycle, Memory Cycle End occurs sooner as the delay for the next phase 1 clock is omitted in the U45 dual AND-OR-Invert stage. Also, a write enable WDEN– is generated at the output of U7-8 by gating the ADOK with DBIN– (high for a write cycle). In addition to setting up the two-way data bus for a memory write transfer, the write enable gates the output of the parity generator onto the data bus lines to store the parity bit associated with the input data.

NOTE

The difference in "Memory Cycle End" caused by the state of DBIN results in a "ghost" signal on all major timing control signals.

8.2.3.3 **Memory Refresh.** On a 2-millisecond interval, all memory chips must be refreshed to prevent loss of data. On the memory expansion board, this function is accomplished through the use of an oscillator, binary counter and an address multiplexer which permits the output of the counter to be substituted for the user memory address lines 3-8 on a periodic basis.

For the following discussion, refer to logic diagram 944937, sheets 2, 4 and 7 and the timing diagram in figure 8-5. A refresh cycle is initiated as follows. The Refresh Required flip-flop (U26-9) sets on the low-to-high transition of the oscillator output (OSC, OSCA). As a result, RFREQD goes high and is synchronized with the phase 3 clock in the Refresh Synchronizer stage (U22-5). If a memory cycle is not currently in progress (START– is HIGH), the Refresh Access flip-flop sets on the trailing edge of the next phase 1 clock (CLK1). The $\overline{Q}$ output of the Refresh flip-flop (RFACC–) is used to reset the Refresh Required and the Refresh Synchronizer stages, set up the address multiplexer to route the output of the counter to the memory chip address lines, set the START flip-flop on the following clock 3 trailing edge. If ADOKL– is present when RFACC is generated, the READY line to the CPU board is lowered which causes the CPU to wait before initiating a memory cycle. The Q-output of the same stage (RFACC) is gated with START to simultaneously clear all chip-enable flip-flops thereby generating a chip enable for all chips in all memory banks.

Notice that the memory cycle end pulse may occur either immediately after the Start Delay flip-flop sets or on the leading edge of the next clock 1 pulse depending on the state of DBIN– at the time the refresh cycle is initiated.

The refresh address counter (U33 and U19) is advanced by the oscillator output at approximately a 31-millisecond rate which permits the counter to reach a count of 64 every 2-milliseconds.

8.2.4 **CHIP ENABLE DRIVERS.** The memory expansion board is equipped with five identical chip enable drivers, one per 4K memory bank, as shown in the simplified logic diagram in figure 8-6. A chip enable is generated each time the Chip Select flip-flop for the given bank is reset (cleared). During a normal read or write operation, the flip-flop is cleared by the logic-low chip select decode at the data input of the flip-flop which indicates that the user address has fallen within that particular 4K memory bank. The logic-low chip-select decode is clocked into the flip-flop on the leading edge of the START:1 pulse from the memory timing circuit. The chip enable flip-flop is then preset to disable the chip enable signal by memory cycle end (MCYEND–) which is also generated by the memory timing circuits.

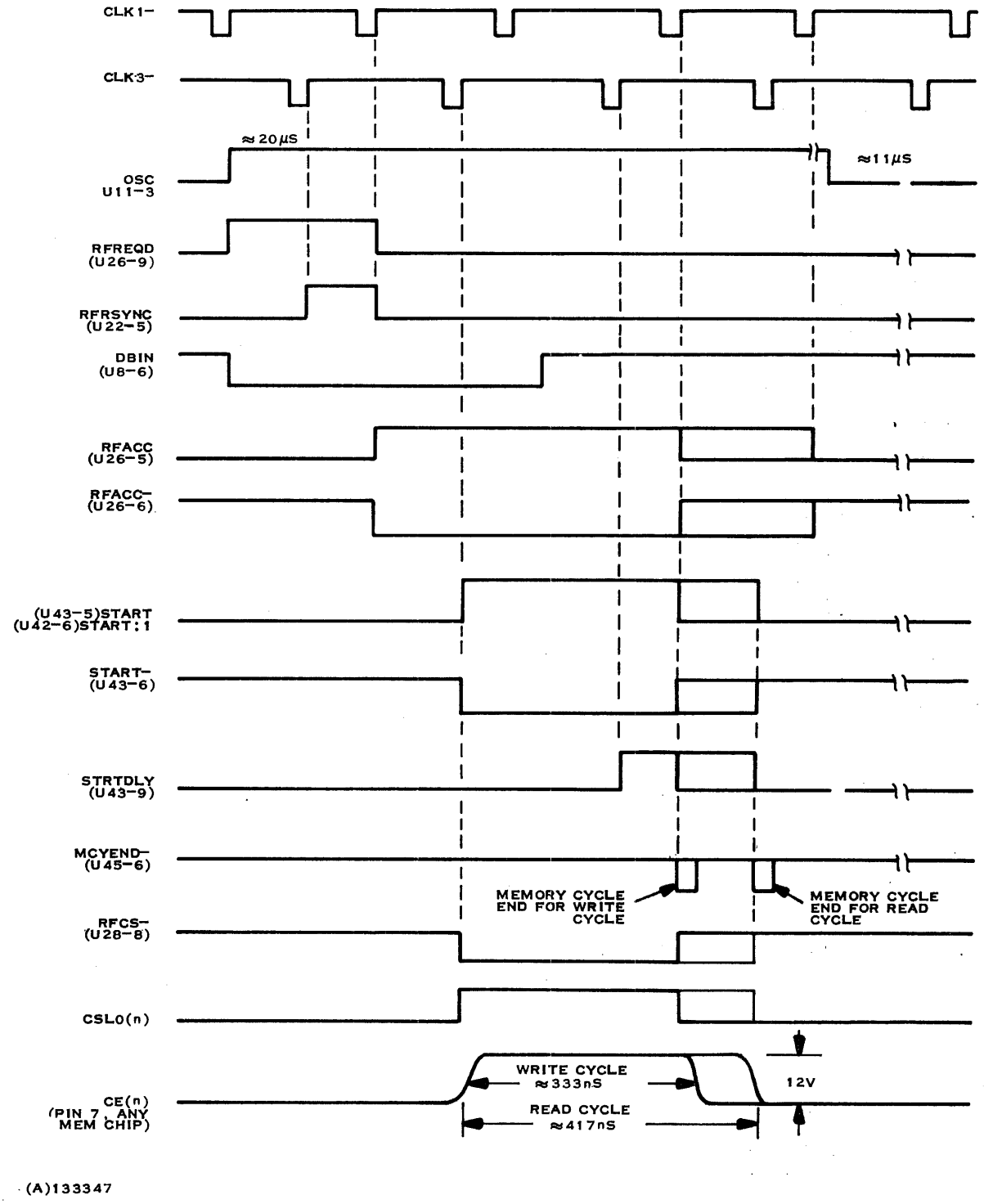


Figure 8-5. Memory Refresh Timing Diagram

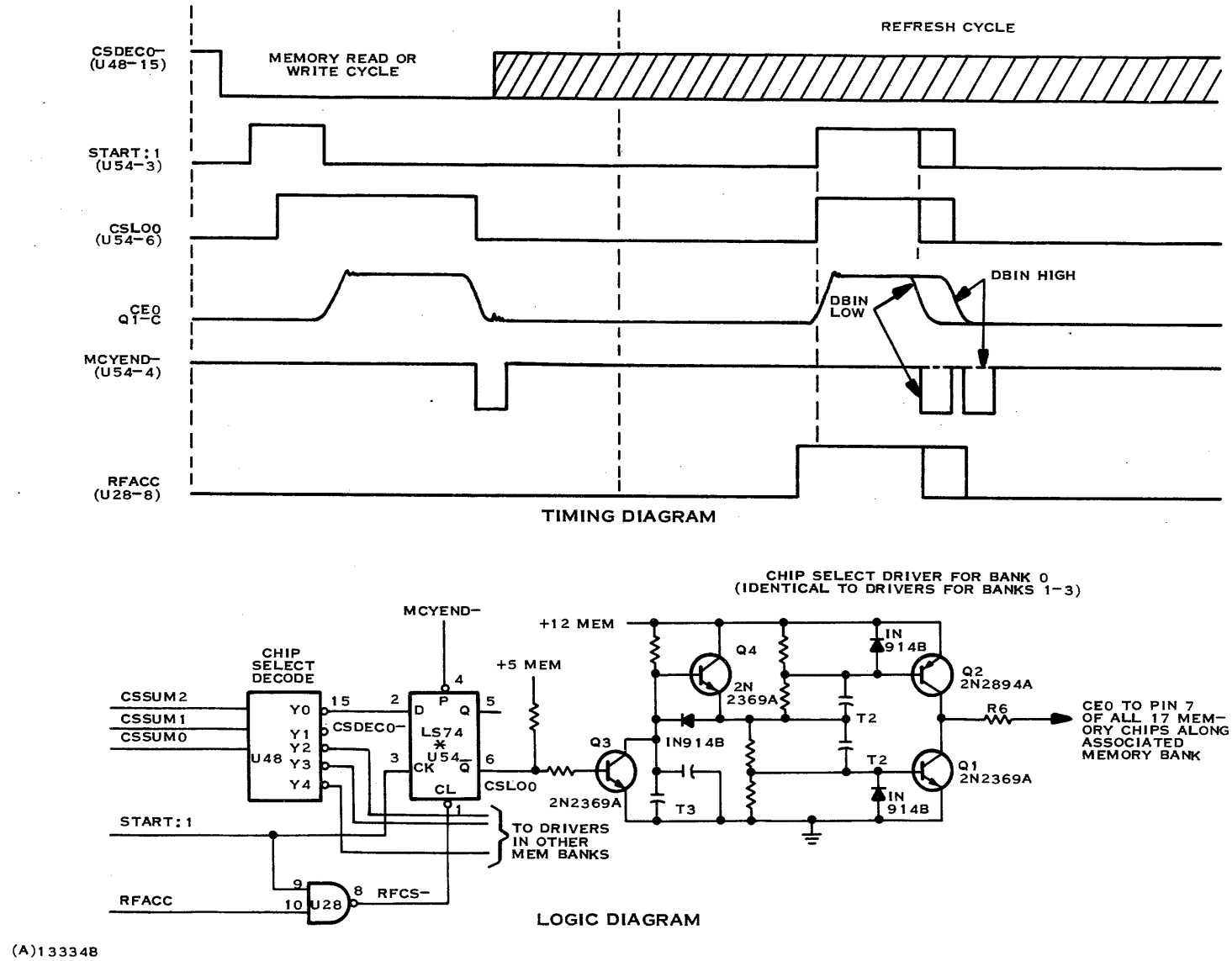


Figure 8-6. Chip Enable Devices, Simplified Logic and Timing Diagram

During a refresh operation, all five chip enable flip-flops are reset at the same time by the refresh chip select (RFCS–) signal generated by gating refresh access (RFACC) with the START:1 pulse from the memory timing circuits. Similarly, a refresh cycle is terminated by MCYEND– which is applied to the preset inputs of all the chip enable flip-flops. Note that the chip enable pulse width varies according to the state of the DBIN line from the TMS 9900. As long as the microprocessor is executing code, a ghost signal appears on the CE outputs at the end of each refresh cycle.

When the chip enable flip-flop for a given bank resets, the resulting logic 1 level at the $\overline{Q}$ output of the chip enable flip-flop causes Q3 to begin conducting. As a result, the voltage at the base of Q4 drops causing the Q4 stage to cease conducting. Therefore, transistor stage Q2 is driven to saturation and Q1 is biased at cutoff. As a result, the output of the driver approaches the +12 volt level and stabilizes at this point.

When the chip enable flip-flop sets (preset by MCYEND–), a reverse sequence of events occur. Q3 is once more biased at cutoff, Q4 begins conducting causing Q1 to saturate and Q2 to cease conduction. As a result, the output of the chip enable driver approaches ground potential.

8.3 990/4 MEMORY EXPANSION BOARD TROUBLESHOOTING PROCEDURES

The remainder of this section provides fault isolation procedures for the memory expansion board. When a faulty component (or suspect component) has been identified, the component is removed and replaced in accordance with the procedures described in Section V. A parts location diagram for the memory expansion board is provided in figure 8-7.

8.3.1 PRELIMINARY INSPECTION. Prior to installing the suspect board in the hot mockup chassis, the following visual inspection should be performed:

1. Inspect all components for signs of overheating, bent pins or socket looseness. Repair before proceeding.

2. Inspect the etched circuit side of the board for cracks in the etch. Repair if required.

3. Inspect the connector pins on the board for signs of excessive wear. If the gold coating is gone, the board should be sent back to the factory for repair.

4. Set up the memory bias switches for a starting memory address of 2000_{16} (S2 off, S3 off, S4 on).

5. Ensure that the memory size jumpers are installed to match the amount of memory installed on the board

	Jumper E1 to E2	Jumper E3 to E4	Jumper E5 to E6
4K	–	–	–
8K	Jumper	–	–
12K	–	Jumper	–
16K	Jumper	Jumper	–
20K	–	–	Jumper

6. If the write protect option is not installed, ensure that a jumper wire is connected between terminals E7 and E8.

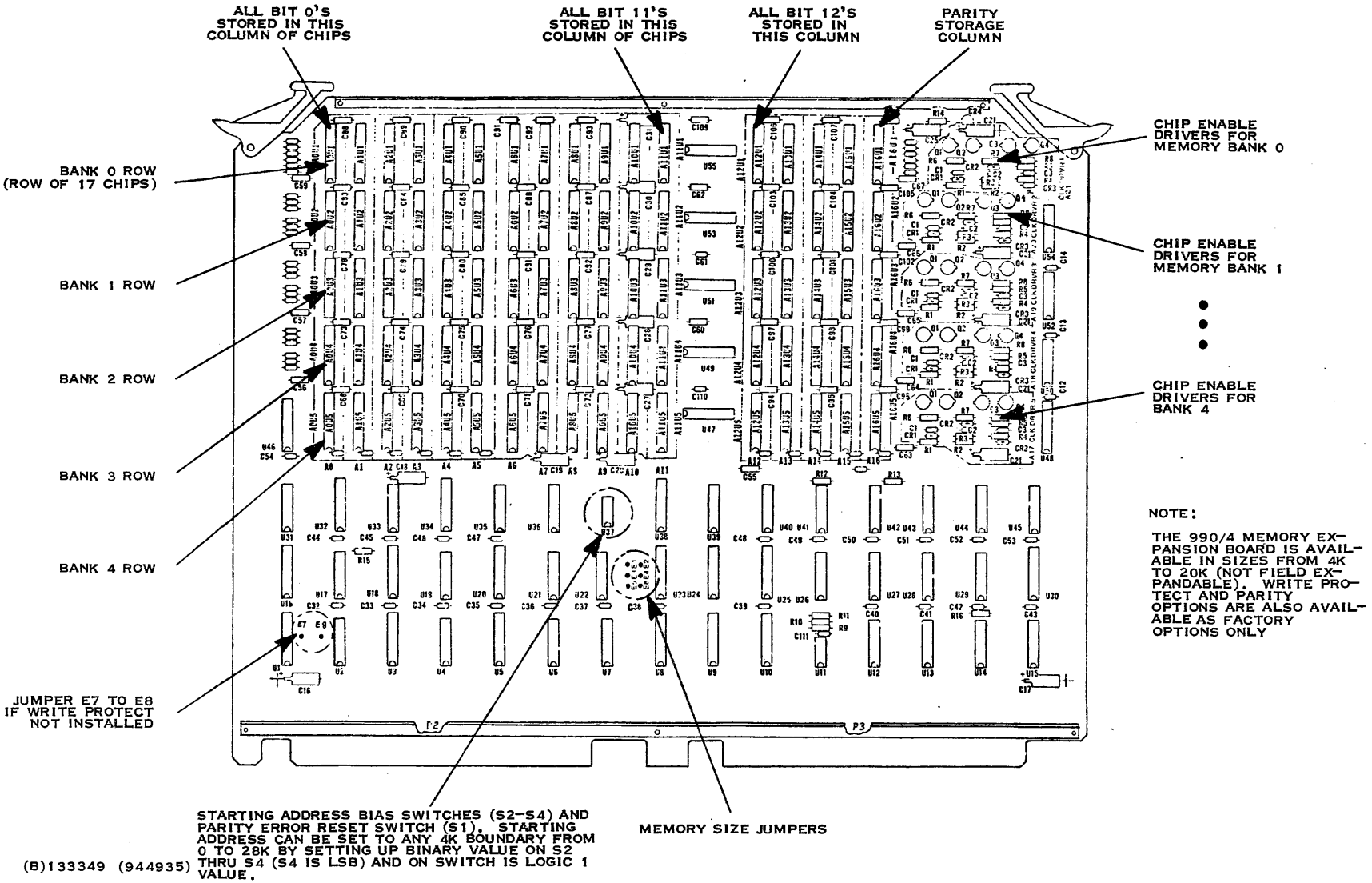


Figure 8-7. 990/4 Memory Expansion Board Layout

8.3.2 **MEMORY EXPANSION CHECKOUT PROCEDURE.** Set the key switch and battery switch to the OFF position. Then mount the suspect memory expansion board on a 990 extender board and install the extender in slot 5 of a 990/4 hot mockup chassis (see Section IV). Then perform the checkout procedures described in table 8-1. If a normal indication is not obtained during any phase of the checkout procedure, refer to the fault isolation procedures in table 8-2.

8.3.3 **SCOPING LOOP.** Once a malfunction has been discovered through the use of the checkout procedure in table 8-1, a scoping loop is then entered into the computer via the programmer panel (see Section IV for description of programmer panel controls and indicators). The scoping loop permits data to be continuously written into or read from a desired memory location or block of memory locations where a malfunction was identified by the memory diagnostics. Dynamic troubleshooting may then be performed on the memory extension board in accordance with the fault isolation procedures in table 8-2, using dual channel scope and DIP clip to facilitate probe connections to the IC pins. The various types of scoping loops used in performing fault isolation are described in the following paragraphs.

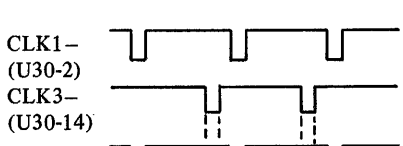
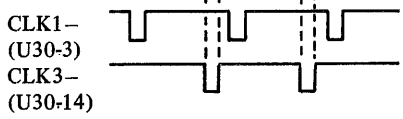
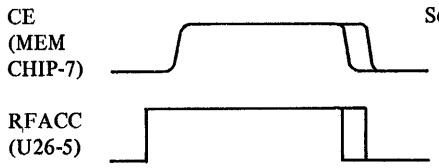
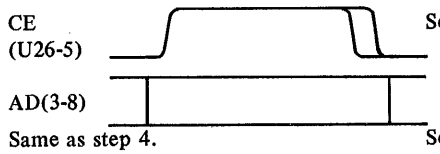
8.3.3.1 **Read Followed by Write at Same Memory Location.** The following program may be used to loop on a single specified address on the memory expansion board:

MEM Location	Machine Code	Comments
0900	02E0	LWPI, >100
0902	0100	
0904	0208	LI R8, (location)
0906	2000	Desired memory extension address
0908	0209	LI R9, (data)
090A	0F0F	(or any desired data pattern)
090C	C609	Mov R9, *R8
090E	10FE	JMP $-1

The scoping loop is entered into the computer from the programmer panel using the following procedure:

1. Set the key switch on the programmer panel to the UNLOCK position.
2. If the RUN LED is lit, press the HALT/SIE switch to halt the processor and begin execution of the programmer panel code. When the panel is active, the RUN LED is extinguished.
3. Press the CLR switch to clear the panel's display register.

Table 8-1. 990/4 Memory Expansion Board Checkout Procedure

Step	Procedure	Normal Indication	If Abnormal
1	Turn on both the ac and battery power switches on 990/4 chassis.	–	–
2	Connect channel 1 probe to the phase 1 clock (U30-2) and the channel 2 probe to the phase 3 clock (U30-14).		Replace U30
3	Move channel 1 probe to U30-3.		Replace U30
4	Connect channel 1 of dual trace scope to the Chip Enable input (pin 7) on any memory chip in bank, channel 2 scope input to refresh access (U26-5). Sync on channel 2.		See table 8-2
5	Repeat step 2 for each memory bank by moving channel 1 scope probe to pin 7 of memory chip in each row.	Same as step 2.	See table 8-2
6	Connect channel 1 probe to pin 7 of any memory chip in bank 0 and scope each high order address line (AD 3-8) with the channel 2 probe. Sync on channel 1.		See table 8-2
7	Repeat step 4 for each memory bank.	Same as step 4.	See table 8-2
8	Insert the cassette containing RAM04 diagnostic (Part Number 945440) into 733 ASR cassette transport number 1. Close the cassette drive door.	–	–
9	Set 733 POWER switch to ON position. Set 733 ON LINE switch to ON LINE position.	733 POWER indicator lights, PLAYBACK CONTROL indicator extinguishes.	–
10	Set KEYBOARD, PLAYBACK and PRINTER switches on 733 to LINE position (see figure 4-3).	–	–
11	Press REWIND switch for applicable cassette transport and wait for END indicator to light.	END indicator on 733 lights.	–
12	Press LOAD/FF and wait for READY indicator to light.	Both READY and END lights extinguish. When tape is properly positioned, READY indicator lights.	–
13	Set key switch on programmer panel to UNLOCK position. Then press HALT/SIE switch, then press LOAD switch.	PLAYBACK ON indicator on 733 ASR lights. Cassette begins moving under software control. When load is complete, ID message is printed out and program begins execution.	–
14	Examine 733 printout for test results.	Printout indicates successful test completion	Evaluate any error message printout and see paragraph 8.3.3.
15	Run diagnostic until five normal completions are obtained. Then press REWIND on 733 to rewind the cassette.	Tape rewinds and halts.	–
16	Remove cassette from transport	–	–
17	Repeat steps 8-16 for MEMPRO04 diagnostic cassette (Part Number 945442).	Same as steps 8-16	Same as steps 8-15

4. Press the ENTER ST (enter status) switch to clear the status register in the TMS 9900.

5. Set up 0900_{16} on the data display LEDs using the data entry switches. This is the address in memory where the first instruction of the scoping loop is to be stored.

NOTE

When a data display LED is lit, it indicates a "1".

6. Press ENTER MA switch to load the memory address value 0900 into the memory address register of the TMS 9900.

7. Press CLR to clear the displays for the next entry.

8. Set up the instruction code ($02E0_{16}$) on the data LED displays using the data entry switches.

9. Press MDE switch which causes 02E0 to be loaded into memory location 0900.

10. Press MAI which increments the memory address value stored in the memory address register and repeat steps 7 through 10 to enter the following program values into successive memory locations:

    - 0100
    - 0208
    - Address which the test will loop on (greater than 2000_{16} for memory ext)
    - 0209
    - Data to be written into the looped memory location
    - C609
    - 10FE

11. Press CLR to clear the displays.

12. Enter 0900 into the displays (address of first instruction in the scoping loop).

13. Press ENTER PC to load the value into the program counter.

14. Press RUN to begin execution of the program. The RUN LED should light to indicate proper operation.

NOTE

If the RUN LED fails to light, return to step 1 and repeat the program setup procedure.

Table 8-2. 990/4 Memory Expansion Board, Fault Isolation Procedures

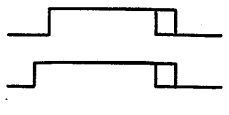
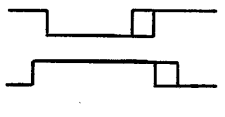
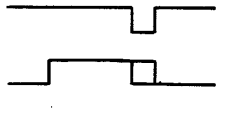
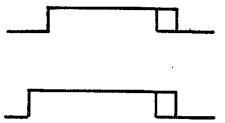
Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
			MEMORY REFRESH PROBLEMS		
1	RFACC present, chip enable missing from all 4K banks	Short circuit between +12 MEM and ground	Monitor +12 MEM at junction of Q2 emitter and CR2 anode in suspect driver circuit.	+12 vdc, ±3%	If near ground potential, locate and replace shorted component • C21 in any driver circuit • C(18, 20, 27-31, 68-108)
		Faulty memory start timing circuit	Connect channel 1 scope probe to START:1 (U42-6). Connect channel 2 probe to RFACC (U26-5).	START:1 (U42-6) RFACC (U26-5) 	See figure 8-5 and individually scope control signals until faulty component is located.
		Loss of RFCS– which clears all four chip select flip-flops during refresh	Connect channel 1 probe to RFCS– (U28-8). Connect channel 2 probe to RFACC (U26-5)	RFCS– (U28-8) RFACC (U26-5) 	Same as above.
		Memory cycle end (MCYEND–) remains low.	Connect channel 1 probe to MCYEND– (U45-6); channel 2 probe to RFACC (U26-5).	MCYEND– (U45-6) RFACC (U26-5) 	Same as above.
2	Chip enable not present for only 1 4K memory bank, RFACC normal.	Faulty chip select F/F (U54 for memory banks 0 and 1, U52 for banks 2 and 3, U50 for bank 4).	Connect channel 1 scope probe to $\overline{Q}$ output of chip select flip-flop for faulty memory bank (see logic diagram); connect channel 2 scope probe to RFACC (U26-5).	$CSLO^{(n)}$ ($\overline{Q}$ of CS F/F) RFACC (U26-5) 	Replace chip select flip-flop U54, U52, or U50.
		Faulty component in 12 volt chip-enable driver circuit.	Refer to paragraph 8.2.4 and figure 8-6 and board logic diagram (944937, sheet 3). Using digital voltmeter, isolate problem to replaceable component using conventional solid state troubleshooting procedures.	Compare voltage potentials in one of the operative CE driver stages against potentials in faulty circuit.	Remove and replace defective component(s).
3	All memory banks down, CE and RFACC both missing	Faulty component in refresh timing circuit	Refer to figure 8-5 and observe the control signals used to generate RFACC.	Timing relationships shown in figure 8-5.	Identify and replace faulty component suspect components include: • U11 • U28 • U44 • U26 • U26 • U43 • U22 • U45

Table 8-2. 990/4 Memory Expansion Board, Fault Isolation Procedures (Continued)

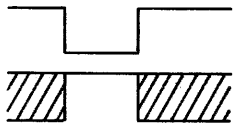
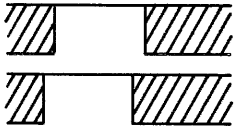
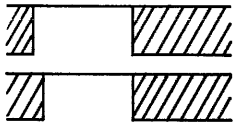
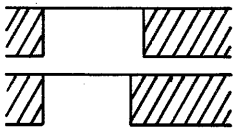
Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
			MEMORY REFRESH PROBLEMS (Continued)		
4	All memory banks down, RFACC present, address lines AD(03-08) not toggling	Faulty address counter	Temporarily connect channel 1 probe to following points: U33-9, U33-5, U33-4, U33-8, U19-5 and U19-4	All outputs should toggle continuously	Replace U33 and/or U19.
		Faulty address multiplexer or address buffer chip.	Temporarily connect channel 1 probe to following points: U32, pins 4, 7, 9, 12 and U34, pins 4 and 7.	All outputs should toggle	If not, replace U32 and/or U34. If all outputs are toggling, replace U47.
			READ/WRITE FAILURES		
5	Refresh appears normal, but unable to read/write into any memory location	Address decode failure or memory enable failure	Set up a write followed by read scoping loop (see paragraph 8.3.3.1). Connect channel 1 scope probe to ADOK– (U28-4). Connect channel 2 probe to ADRIN02 (U4-6). Sync on channel 2.	ADOK– (U28-4) ADRIN02 (U4-6) 	If MEMEN not present, replace U8. If ADOK– not present, check bias switches and memory size jumpers against values provided in figure 8-2. If jumpers are correct, proceed to next step.
			Move channel 1 probe to GTEMIN (U38-10).	GTEMIN (U38-10) ADRIN02 (U4-6) 	Remove and replace U38.
			Move channel 1 probe to GTMAX– (U23-10).	GTMAX– (U23-10) ADRIN02 (U4-6) 	Remove and replace U23.
			Move channel 1 probe to PV– (U7-6).	PV– (U7-6) ADRIN02 (U4-6) 	If PV– is low during first MEMEN, check U6, pins 1, 2. If normal, replace U6. If U6-2 is high, replace U8.
6	Refresh normal, unable to read/write into any memory bank	Chip select decode inoperative	If ADOK– is normal, faulty chip select decode is indicated.	–	Remove and replace U48.

Table 8-2. 990/4 Memory Expansion Board, Fault Isolation Procedures (Continued)

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
			READ/WRITE FAILURES (Continued)		
7	Refresh normal, unable to read/write into one of the 4K banks	Faulty bit in chip select decode	Set up read scoping loop for entire memory bank (see paragraph 8.3.3.2 and 8.3.3.3). Monitor each output of the chip select decode (U48).	All outputs should toggle	Replace U48.
		Faulty chip enable flip-flop associated with defective memory bank.	Monitor all inputs to chip enable flip-flop	–	Remove and replace faulty IC (U54 for banks 0 or 1, U52 for banks 2 or 3, U50 for bank 4).
8	Single bit data error in one or more addresses	Faulty memory chip	Remove and replace memory chip corresponding to bit position (see figure 8-7).	Bit error disappears when diagnostic is rerun in accordance with table 8-1.	Replace memory chips (one at a time in the same bit position in the remaining memory banks (outputs ORed together). If problem persists, replace 2-way bus chip corres. to bit position (U20, U24 or U25).
9	Intermittant data errors at varying memory addresses.	Memory refresh or memory timing problem	Carefully examine timing relationships of control signals and address lines. Ensure that AD(3-8) are changing just outside the CE window (step 4 of table 8-1).	See figure 8-5.	Check inputs and outputs to stage which does not corres. to timing shown in figure 8-5. If inputs are good, replace chip.
			If refresh timing is normal, set up read/write scoping loop (paragraph 8.3.3.1). Check timing relationships of control signals according to figure 8-4.	See figure 8-4.	Locate chip with faulty output. If inputs abnormal replace IC.
			If control signals appear to be normal, carefully examine address section.	Address entered in scoping loop should be good TTL levels at mem chip inputs.	Remove and replace faulty address stage.
10	Protect Violate is not generated when attempt is made to write into protected address.	Faulty output driver	Set up scoping loop described in paragraph 8.3.3.4 and monitor PV– at U13-4.	Should periodically go low.	If PV– is present, replace U13.
		Faulty write protect circuit	Connect scope to MODCLK– (U29-8)	Should pulse low (string of 16 clocks followed by single clock).	Check inputs and outputs to following stages: U29, U14 and U15. Remove and replace faulty stage.

Table 8-2. 990/4 Memory Expansion Board, Fault Isolation Procedures (Continued)

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
			READ/WRITE FAILURES (Continued)		
10		←(Continued)→	Connect channel 1 to MODCLK– (U29-8). Connect channel 2 to CRUBITOUT– (U14-12).	Value entered in 020A (1011_{16}) should be serially shifted to the input of the bounds register.	Replace U14.
			Monitor value stored in the bounds register.	Same as above.	Replace U02 and/or U17.
			Connect scope to PROTWEN (U06-3).	Should periodically go high.	Check DBIN–. If periodically goes high, replace U06. If DBIN– stays low, replace U42 and/or U08.
			Connect scope to OUTBOUD (U06-6).	Should periodically go high.	Replace U01 and/or U03 if GTELB does not periodically go high. Replace U16, U18 or U21 if GTEUB– does not periodically go high.

8.3.3.2 Continuous Read From Selected Memory Location. The basic scoping loop program described in 8.3.3.1 may be modified to perform a continuous read at a selected memory extension address by changing the instruction at memory location 090C in the previous program from C609 to C258 which is a MOV *R8,R9 instruction. This change to the basic program causes data to be read from a selected address and stored in memory location 0112 (workspace register 9). For maintenance purposes, the scoping loop may be interrupted at any time and the value stored in the workspace register may be examined using the following procedure:

1. Halt the processor by pressing HALT/SIE. The RUN LED should extinguish.
2. Press CLR to clear the displays.
3. Enter 0112 into the displays using the data entry switches.
4. Press ENTER MA to load 0112 into the memory address register.
5. Press MDD. The resulting value displayed on the panel LEDs should be the same value stored in the address indicated by memory location 090A of the scoping loop program.

8.3.3.3 Scoping Loop for a Band of Memory Addresses. The basic scoping loop program may also be modified as follows to permit looping over a band of memory addresses in which the beginning and ending addresses are specified in the program:

Scoping Loop for Reading Band of Memory Addresses

MEM Location	Machine Code	Comments
0900	02E0	LWPI >80
0902	0100	
0904	020A	LI R10, ENDLOC
0906	ENDLOC	Ending address +2
0908	0209	LI R9, DATA
090A	DATA	
090C	0208 ←	LI R8, LOC
090E	LOC	
0910	→ CE09	MOV R9, *R8+
0912	820A	C R10, R8
0914	14FB →	JHE
0916	10FC	JMP

The procedures for entering this program into computer memory are essentially the same as described in paragraph 8.3.3.1.

8.3.3.4 Scoping Loop for Write Protect. The following scoping loop will permit the write protect register on the memory expansion board to be loaded with a protect value and will then attempt to write into the protected memory space resulting in a protect violate condition. The program then loops back and repeats these functions to permit a dynamic test of the write protect section.

MEM Location	Machine Code	Comments
0200	0300	LIMI >0
0202	0000	
0204	02E0	LWPI >100
0206	0100	
0208	020C	LI R12, >1FA0
020A	1FA0	
020C	0209	LI R9, >1011 (Adr. 2000 to 21FE)
020E	1011	
0210	3009	LDCR R9, 0
0212	C809	MOV R9, >2000 (Attempt write into LOC 2000)
0214	2000	
0216	1F00	TB 0
0218	1D00	SBO 0
021A	10FA	JMP $-6

Setting a Write Protect Region. To set a write protect region, the lower and upper bounds must be output to CRU base address $1FA0_{16}$. The most significant bit (bit 0) is the Protect/Permit bit. Bit 0, when set to 1, indicates write permit, and, when set to 0, indicates write protect. To specify the protect region, memory is divided into 256-word blocks. The lower and upper bounds are each seven bits long and serve as an index into the memory addresses to specify which contiguous 256-word block of memory is to be protected. For example, the lower bound of the protect region equal to 2000_{16} would be represented in the Protect register as 10_{16}. The memory block beginning at location 2000_{16} is the sixteenth 256-word (512-byte) memory block. A bound is calculated by dividing the starting address of the memory block by 200_{16} (512_{10}). In this example, 2000_{16} divided by 200_{16} is equal to 10_{16}. The upper bound is not included in the protect region. When outputting to the CRU Protect register to specify the protect bounds, a Load CRU (LDCR) instruction with a count of 16 must be used to set all 16 bits because the Protect register works like a shift register. To protect the memory range 2000_{16} to 4000_{16}, the lower bound is set equal to 10_{16}, the upper bound is set equal to 20_{16}, and the Protect bit is set to 0. Therefore, the Protect register is set to 1020_{16} by outputting these fields to the CRU in the format specified in figure 8-3.

SECTION IX

990 EPROM MEMORY MODULE TROUBLESHOOTING DATA

9.1 GENERAL

This section provides a functional description of the 990 EPROM memory module (Part Number 945170-1) and describes the jumper and switch selectable options which must be installed on the board prior to normal use. This section also provides checkout procedures required to locate board failures and fault isolation procedures to isolate malfunctions down to a replaceable component(s) level.

The board is checked out using the hot mockup described in Section IV. Corrective maintenance procedures required to replace components on the memory module are supplied in Section V. The logic diagram and assembly drawing/list of materials for the memory module are available in the *990 Family Maintenance Drawings Manual.*

9.2 JUMPER AND SWITCH OPTIONS

Prior to installing a 990 EPROM memory module in a system, the following options must be installed:

- Computer ID jumper – To use the EPROM board in a 990/4 microcomputer, a jumper must be installed between E11 and E12 (E11 to E10 for use in 990/10 computer).

- Starting Memory Address Bias – The starting memory address for the board may be set at any 1K boundary between 0 and 31K using the five microswitches on SW2 (SW1 is used only with 990/10). See figure 9-1 for details. For use in the hot mockup, the switches should be set up for a starting address at 25K (just above memory expansion).

- Maximum Memory Size Jumpers – Jumpers must be installed on terminals E1 through E9 to indicate the amount of memory installed on the board. The table in figure 9-1 describes the jumper configurations for various memory sizes from 1K to 8K.

For jumper and switch locations, see figure 9-2.

9.3 FUNCTIONAL CIRCUIT ANALYSIS

The incoming address lines ADR(0-14) from the 990/4 microcomputer board (or from an external DMA type controller) map onto the EPROM board address inputs TLADR(05-19), respectively. TLAD(00-04) are not used with the 990/4 computer system.

The user address is then biased with the starting address inputs from bias switch SW2, and tested in adder stages U28, 38, and 30 plus gates U20 and U31 to see if the address is greater than or equal to the lowest address on the board and less than the maximum amount of memory implemented on the board (as indicated by the jumpers on E2, E5 and E8).

If the address is within the address space of the EPROM memory board, memory bus address OK data (MBADOKD) is generated which is then synchronized with the phase three clock (CLK3–) to generate MBADOK (U33-9), provided that memory enable is present. MBADOK is routed through the "computer type" selector stage (U23) to generate ADOK. Note that the select line to U23 must be tied to VCC through a jumper from E11 to E12 to permit selection of the 990/4 memory bus address OK.

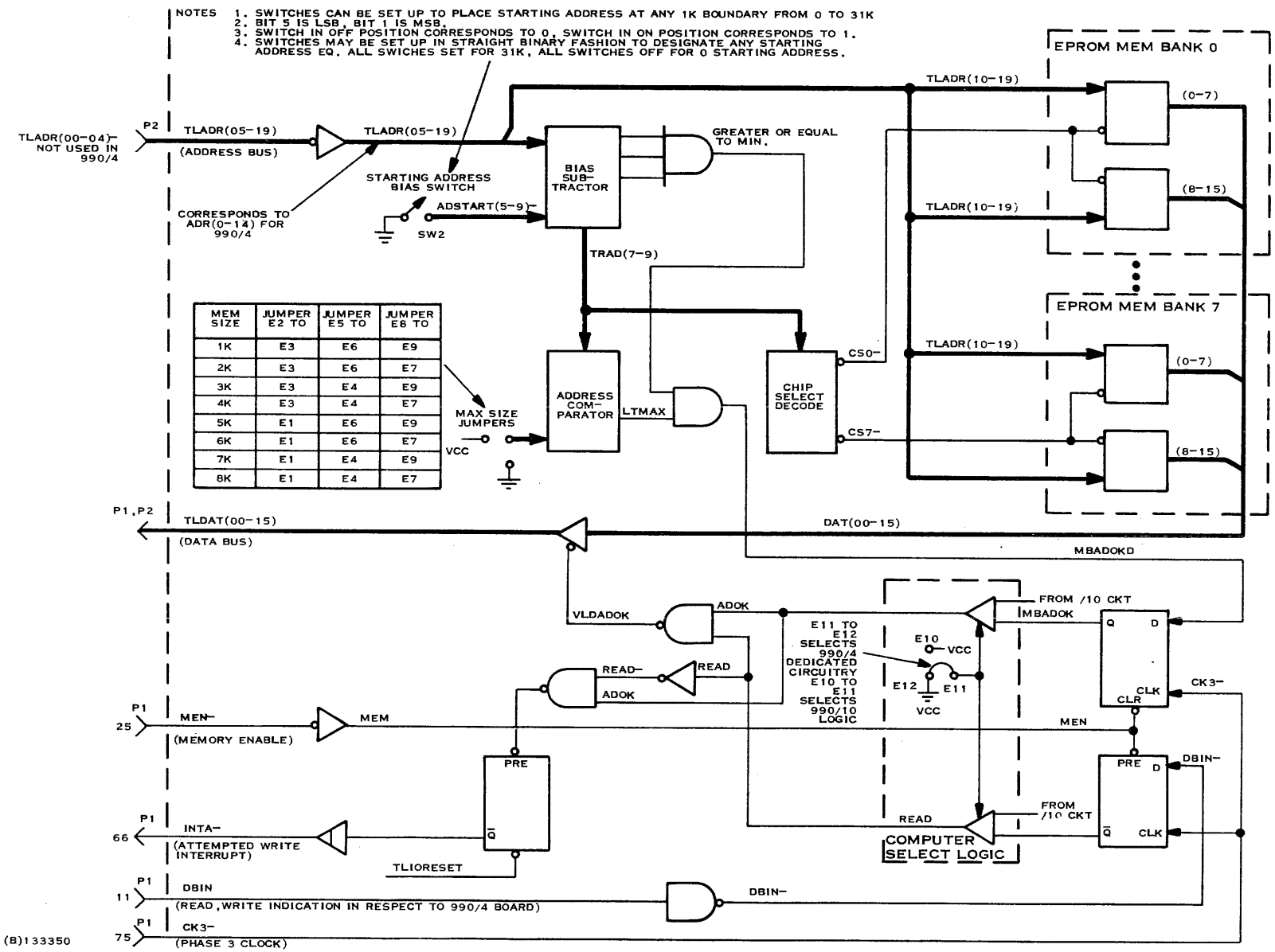


Figure 9-1. EPROM Memory Module, Block Diagram

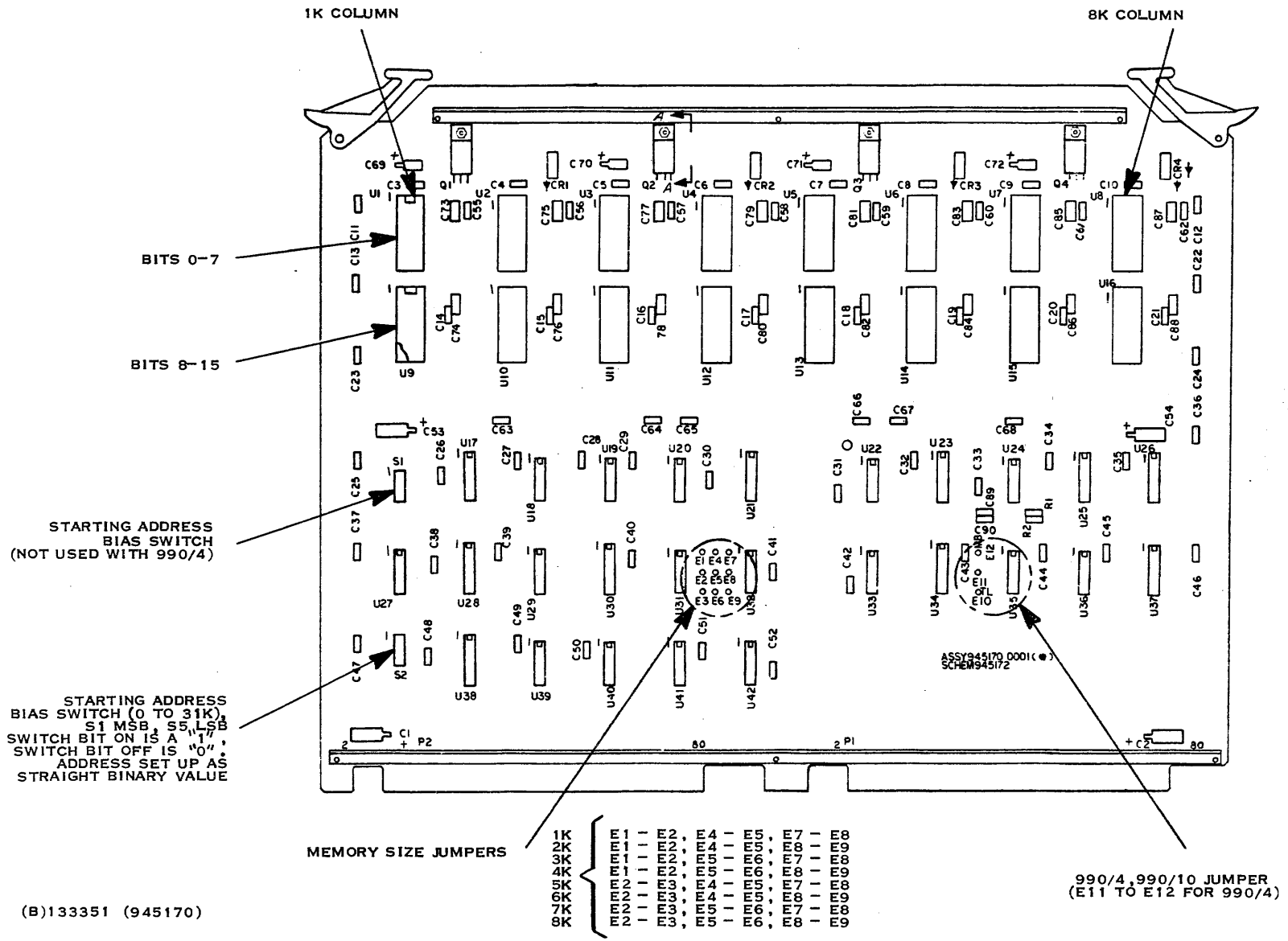


Figure 9-2. EPROM Memory Module Board Layout

The address OK signal (ADOK) at the output of the selector enables the chip select decoder stage U21 which decodes the biased user address lines (TRAD 7-9) to enable one of the 8 possible 1K EPROM memory banks on the board. At approximately the same time, the DBIN input from the user processor is synchronized with the phase 3 clock and enabled through the "computer type" selector as READ. READ is then gated with ADOK to enable the data output of the EPROM memory chips through the tri-state drivers on the output data lines.

The READ signal, which is developed from DBIN, is also inverted and gated with ADOK to issue an interrupt (INTA–) in the event that a write is attempted into the EPROM memory address space. The interrupt flip-flop (U32) can then be cleared (preset) with an IORESET from the 990/4 microcomputer board.

9.4 TROUBLESHOOTING PROCEDURES

The troubleshooting procedures for the 990 EPROM memory module are based on the use of the checkout procedures in table 9-1 to locate malfunctions and the use of the procedures in table 9-2 to isolate the malfunction down to the replaceable component(s) level. After the board has been repaired, the checkout procedure should be repeated to ensure that all malfunctions have been corrected. The board is then ready to be returned for normal use.

9.4.1 TEST SETUP. The 990 EPROM memory module is tested in the hot mockup chassis as described in Section IV of this manual. Prior to installing the suspect board in the chassis, perform the following checks:

- Ensure that a jumper is installed between E11 and E12 (see figure 9-2).
- Set the bias switch SW2 for a 25K starting address (S1, S2 and S5 ON, S3 and S4 OFF).
- Ensure that the maximum size jumpers (see figure 9-1) are installed to correspond to the amount of memory implemented on the board. Note that 2 chips correspond to 1K of memory with banks 0-7 installed from left to right on the board (see figure 9-2).
- With an ohmmeter, check each dc power input to ensure that no shorts exist on the input power lines.

At this point, proceed to table 9-1 for the board checkout procedures.

Table 9-1. EPROM Memory Module, Checkout Procedure

Step	Procedure	Normal Indication	If Abnormal
1	Perform initial tests as described in paragraph 9.4.1. Ensure that all jumper wires are properly installed.	–	–
2	Set key switch on 990/4 programmer panel to OFF position.	POWER LED on panel extinguishes	–
3	Mount 990 EPROM memory module on full size extender board and install in any available slot in 990/4 hot mockup chassis.	–	–
4	Set key switch on programmer panel to UNLOCK position.	RUN, POWER LEDs light	–
5	Measure the dc voltage at pin 21 of each memory chip.	-5 vdc, ±3%	Replace regulator stage for associated bank (Q1-Q4).
6	Insert cassette containing the 990 EPROM diagnostic (ROMBT), Part Number 945459, into one of the two transports on the 733 ASR. Shut the door after inserting cassette.	–	–
7	Set controls on 733 ASR to following: • POWER switch to ON • 733 ONLINE switch to ONLINE position • KEYBOARD and PLAYBACK switches to LINE position • RECORD switch to OFF position • RECORD/PLAYBACK switch (for transport containing diagnostic) to PLAYBACK.	PLAYBACK LED for selected xport lights.	
8	Press REWIND switch for selected transport and wait for END indicator to light.	END LED lights.	–
9	Press LOAD/FF and wait for READY indicator to light.	Both READY and END LEDs extinguish. When tape is properly positioned, READY lights.	–
10	Press HALT/SIE switch on programmer panel.	RUN LED extinguishes.	Ensure that key switch is in UNLOCK position.
11	Press LOAD switch.	PLAYBACK ON LED lights, cassette begins moving under software control. When load is complete, (1 to several minutes) ID message is printed out and program execution begins. RUN LED on programmer panel lights.	–
12	Examine 733 printout for test results.	Printout indicates successful test completion.	See table 9-2.
13	Permit diagnostic to run for five normal completions. Then press REWIND on 733 ASR. When tape stops, open transport door and remove cassette.	–	–

Table 9-2. EPROM Memory Module, Fault Isolation Procedures

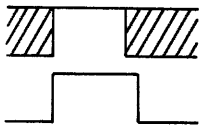
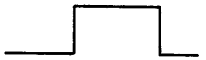
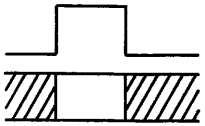
Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
1	Unable to read valid data from any location.	Loss of address OK	Set up scoping loop to read from address $BC40_{16}$. (See paragraph 8.3.3.2.) Connect channel 1 of scope to TLADR05 (U28-6) and sync on channel 1. Connect channel 2 to ADOK (U21-6).	TLADR05 (U28-6) ADOK (U21-6) 	Check all jumper options in accordance with paragraph 9.4.1. If correct, proceed with next substep.
			Move channel 2 probe to MBADOK (U23-6).	MBADOK (U23-6) 	Proceed to next substep. If normal, check for jumper between E12 (vcc) and E11. If normal, replace U23.
			Move channel 2 probe to MBADOKD (U33-12).	MBADOKD (U33-12) 	Proceed to next substep. If normal, check preset input (replace U34 if constant logic 0 is detected). If preset input periodically goes low, check CLK3– at U22-11. If missing, replace U36. If preset and clock inputs normal, replace U22.
			Move channel 2 probe to monitor each input to gate U31.	Both inputs should go high when TLADR05 goes high.	If U31-1 abnormal, replace U30 and/or U38. If U31-2 abnormal, remove and replace U28 and/or U20.
		Faulty chip select decode stage U21.	Remove and replace U21 if ADOK normal.		If problem persists, remove and replace U38.
		Faulty tri-state driver stage.	Analyze printout to determine which bit(s) is in error.		Replace driver stage U37, U25 or U26.
2	No interrupt generated when write is attempted. Read functions normal.	Faulty interrupt circuit.	Set up scoping loop to execute a read followed by write at address $BC40_{16}$ (see paragraph 8.3.3.1). Connect channel 1 probe to preset input of interrupt flip-flop.	Preset input should periodically go low.	Trace read - signal paths and remove and replace faulty component (U42, U40, U23, U22 or U34). If normal, check clear input (U32-1). If high, check U32-6. If low, replace U24. If high, replace U32.

Table 9-2. EPROM Memory Module, Fault Isolation Procedures (Continued)

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
3	1 memory bank inoperative, all others normal.	Faulty chip select decode stage.	Set up scoping loop to continuously read from faulty bank. Connect scope to chip select output for appropriate bank (U21 stage outputs).	Output should periodically go low.	Proceed to next substep.
			Connect channel 1 scope probe to ADOK (U21-6). Sync on channel 1. Connect channel 2 scope input to address lines TRAD (7-9).	ADOK (U21-6) TRAD (7-9)  Address lines should correspond to binary value of addressed bank (TRAD9 is the LSB).	Check SW2 for proper setting (see figure 9-1). If normal, replace U38 and/or U39, U40. If address lines are normal, replace U21.
4	READY remains low, all other functions normal.	Faulty multiplexer or driver stage.	Check TM/RDY– output of computer type selector stage U23-4.	Constant low value.	Remove and replace U23. If normal, replace U34.

SECTION X

PROGRAMMER PANEL TROUBLESHOOTING DATA

10.1 GENERAL

This section provides functional circuit analysis and troubleshooting procedures for the 990 programmer panel/panel interface board assembly.

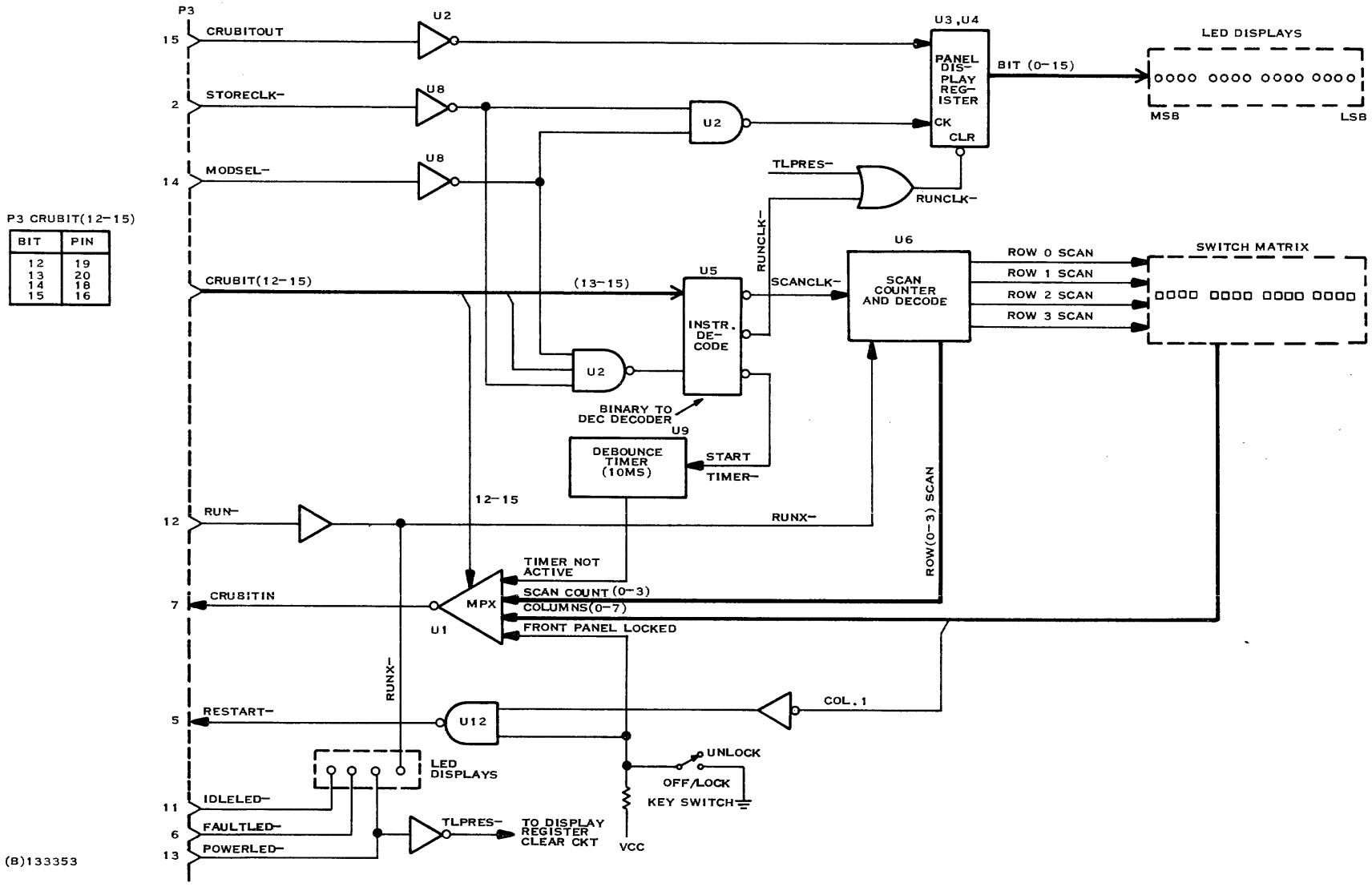
10.2 FUNCTIONAL CIRCUIT ANALYSIS

The 990 programmer panel provides for manual control of the computer when the key switch on the panel is in the UNLOCK position. In the LOCK position, the panel switches are all disabled and data may be displayed on the panel's LED displays under software control.

When power is first applied to the system, the 990/4 comes up in the run mode of operation which results in a low-active RUN– signal at P3-12 to the programmer panel interface board. This signal is buffered on the board and used to halt the scan counter (stage U6) at a count which constantly enables the row 2 input to the panel's switch matrix. Therefore, only the SIE/HALT switch, which is located at the intersection of Row 2 and Column 1, is enabled provided the key switch on the panel is set to the UNLOCK position (see figure 10-1). The RUN– signal also clears the data display register and forces all data display LEDs to display 1s (all LEDs light).

In order to make the switches operational on the programmer panel, the key switch must be set to the UNLOCK position and the SIE/HALT switch must be pressed on the panel. The resulting column 1 (low active) signal is inverted and gated with the output of the key switch (VCC when switch is in UNLOCK position). As a result, a low active RESTART– signal is sent to the 990/4 microcomputer board which results in a trap to memory location FFFC. This location contains the workspace pointer and workspace register values required to initialize the panel software which is stored in approximately 70 words of ROM on the 990/4 microcomputer board. At this point, the RUN– signal from the computer goes high thereby removing the clear and preset signals from the scan timer (see figure 10-2). Software then periodically advances the scan timer by issuing scan clocks (SCANCLK–) via SBO or SBZ instructions with CRUBIT(12-15) encoded with a hex value of 8. As the scan counter is advanced, panel software issues STCR instructions to individually read the various inputs to multiplexer stage U1.

If an indication is received that one of the panel switches has been pressed, the software utility activates a 10-millisecond debounce timer on the programmer panel board via an SBO or SBZ instruction addressed to bit 8 (CRUBIT12-15 encoded with 8_{16}). The resulting START TIMER– signal activates the debounce timer. Since the output of the timer is also routed to the CRUBITIN line via the multiplexer, software can determine when 10 milliseconds have elapsed. At this time, the software monitors the column containing the pressed key to ensure that the key is still pressed. If so, the software determines whether the key is a data key or function key. In the case of a function key, panel software branches to the appropriate instruction in the program which executes the specified function. In the case of a data key, the data bit is complemented (if previously a 1, changed to a zero and vise versa). The complemented bit is also stored in the data display register on the programmer panel board and applied to the corresponding DATA LED. A logic 1 is indicated by a lighted LED and a logic 0 is indicated by an extinguished LED.



P3 CRUBIT(12-15)

BIT	PIN
12	19
13	20
14	18
15	16

(B)133353

Figure 10-1. Programmer Panel Functional Block Diagram

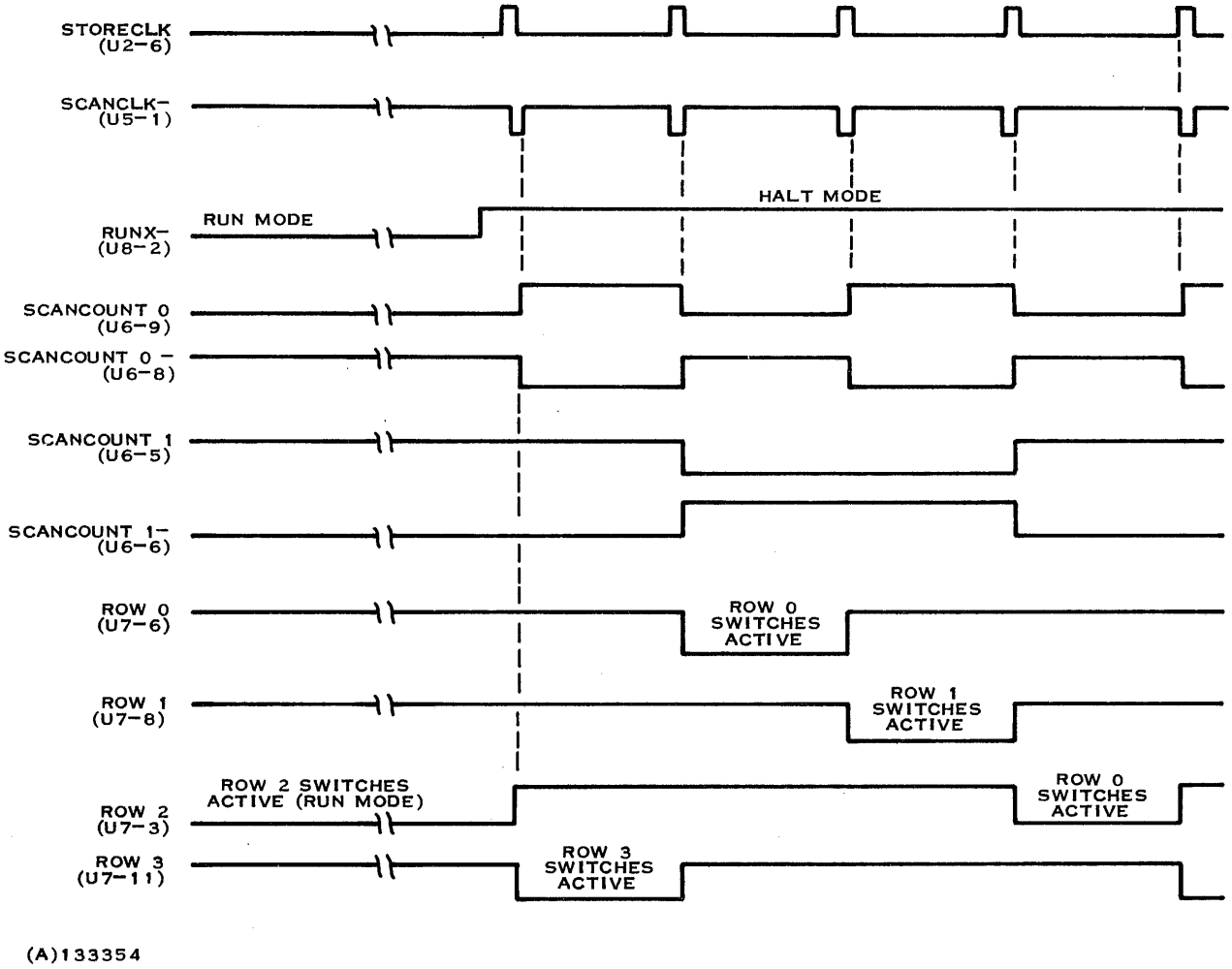


Figure 10-2. Scan Counter Timing Diagram

10.3 TROUBLESHOOTING PROCEDURES

Troubleshooting procedures for the 990 programmer panel are based on the use of the 990/4 hot mockup system (see Section IV) to drive the panel. Initially, the panel is cabled to the system in accordance with paragraph 10.3.1 and tested using the procedures provided in table 10-1. When a malfunction is discovered, the trouble is isolated down to a faulty component level using the procedures provided in table 10-2.

Table 10-1. Programmer Panel Checkout Procedure

Step	Procedure	Normal Indication	If Abnormal
1	Set key switch to OFF position. Measure resistance between the C and NO terminals on 1A4S1 (microswitch located to left of key switch when viewed from rear of panel).	Infinite resistance.	Replace 1A4S1.
2	Measure resistance across C and NO terminals of 1A4S1 with key switch in LOCK position.	0 ohms	Same as above.
3	Repeat resistance measurement with key switch in UNLOCK position.	0 ohms	–
4	Connect the hot mockup chassis ac power plug to ac power. Set key switch on hot mockup panel to LOCK position.	POWER, FAULT and RUN LEDs on panel under test should light, all data LEDs should light.	See table 7-2.
5	Set key switch on panel under test to LOCK position.	--	–
6	Press SIE/HALT switch.	RUN LED remains lit.	See table 7-2.
7	Set key switch on panel under test to UNLOCK position. Press SIE/HALT switch.	RUN LED extinguishes.	See table 7-2.
8	Press RST switch.	FAULT LED extinguishes.	See table 7-2.
9	Press odd numbered data entry switches (1, 3, 5, etc.).	Corresponding data LEDs should light.	See table 7-2.
10	Press CLR switch.	All LEDs extinguish.	–
11	Press even numbered DATA ENTRY switches.	Even numbered LEDs light.	–
12	Press CLR switch.	All LEDs extinguish.	–
13	Press HALT/SIE switch eight times.	DATA LEDs between 9 and 15 display different value each time switch is pressed.	–
14	Press the following switches in the order listed: • CLR • DATA ENTRY SWITCH number 4 • ENTER MA (stores 0800_{16} in memory address register).	DATA LED number 4 lights	
15	Press the following switches in the order listed: • CLR • DATA ENTRY switch number 8 • MDE switch (stores 0080_{16} in address location 0800)	DATA LED number 8 lights	
16	Press the following switches in the order listed: • CLR • MAI • DATA ENTRY switch number 9 • MDE (Increments memory address and stores 0040 in memory location 0802).	DATA LED number 9 lights	

Table 10-1. Programmer Panel Checkout Procedure (Continued)

Step	Procedure	Normal Indication	If Abnormal
17	Press following switches in order listed: • CLR • DISPLAY MA (Value currently stored in memory address register is displayed on DATA LEDs).	DATA LEDs 4 and 14 should light (0802).	
18	Press following switches in order listed: • CLR • DATA ENTRY switch number 4 • ENTER MA • MDD (address 0800 entered into memory address register and value stored in memory address 0800 is displayed on DATA LEDs - should be same as value entered in step 15).	Only DATA LED number 8 lights.	
19	Press MAI switch and then press MDD switch. (Display value stored in address 0802 - same value entered in step 16.)	Only DATA LED number 9 lights.	
20	Press following switches in order listed: • CLR • DATA ENTRY switch number 4 • ENTER WP • DATA ENTRY switch number 5 • ENTER PC • DATA ENTRY switch number 6 • ENTER ST	DATA LED number 4 lights. DATA LEDs 4, 5, and 6 light.	
21	Press following switches in order listed: • CLR • DISPLAY WP	Only DATA LED number 4 lights.	
22	Press DISPLAY PC switch.	DATA LED 4 remains lit and DATA LED number 5 lights.	
23	Press DISPLAY ST switch.	DATA LEDs 4 and 5 remain lit, DATA LED number 6 lights.	
24	Press LOAD switch.	All DATA LEDs light, RUN LED lights.	
25	Press HALT/SIE switch; press CLR switch.	All DATA LEDs extinguish, RUN LED extinguishes.	
26	Press following switches in order listed: • DATA ENTRY switch number 4 • ENTER MA • DATA ENTRY switches 3, 5, 7, 12, 14, and 15 • MDE • MAI • CLR • DATA ENTRY switches 6, 7, and 9		

Table 10-1. Programmer Panel Checkout Procedure (Continued)

Step	Procedure	Normal Indication	If Abnormal
26 (cont)	• MDE • MAI • CLR • DATA ENTRY switches 5, 9, 10 • MDE • MAI • CLR • DATA ENTRY switch number 4 • MDE • RUN	RUN, IDLE, and FAULT LEDs light.	
27	Press CLR and then press each DATA ENTRY switch.	All LEDs light.	
28	Again, press each DATA ENTRY switch.	As each switch is pressed a second time, note that the corresponding LED extinguishes.	

This concludes the programmer panel checkout procedure.

Table 10-2. Programmer Panel Fault Isolation Procedures

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
1	RUN and/or POWER LEDs fail to light when power is turned on.	Faulty microswitch 1A4S1 on key switch or faulty U8 stage.	With ac power disconnected from chassis, measure resistance across C and NO terminals of switch, when key switch is set to LOCK and UNLOCK positions.	0 ohms	Replace 1A4S1. If normal, replace U8 and/or LEDs.
2	RUN LED extinguishes when HALT/SIE switch is pressed and key switch is in LOCK position.	Faulty cam or microswitch on key switch assembly.	Examine cam on rear of key switch. If normal, replace 1A4S2.		
3	Panel locked in RUN mode, key switch in UNLOCK position.	Faulty 1A4S2 microswitch or faulty gating stage associated with RESTART–.	Set key switch to UNLOCK position. Connect scope probe to U12-9 (RESTART–) and press and hold HALT/SIE switch.	Logic low RESTART– pulse is generated at U12-9.	Remove and replace U12 and/or R1. If problem persists, replace rightmost switch block when view from rear.
4	In RUN mode, all LEDs light; in HALT mode, unable to light any LED using data entry switches.	Faulty row decode stage.	Using scope, monitor ROW decodes at output of U7.	All ROW enable signals periodically go low (see figure 10-2).	Monitor outputs of scan counter. If all scan counter outputs are toggling, replace U7.
		Faulty scan counter.	If scan counter outputs (U6- pins 5, 6, 8 and 9) are not toggling, check inputs to the counter.	See figure 10-2.	Locate and replace faulty stage (U5, U2, or U8). If inputs normal, replace U6.
		Faulty display register.	Monitor inputs to stages U3 and U4.	Clear input (U3 and U4, pin 9) should be high; CK input (pin 8) should periodically go low. CRUBITOUT– (U3-1) should periodically go low.	Faulty clear may be caused by U12, U8, or U5. Loss of clock may be faulty U2 or U8 stage. If CRUBITOUT– remains high, replace U12. If all inputs normal, replace U3.
		Faulty output multiplexer stage.	Monitor inputs to U1 stage.	MODSELX– periodically goes low, address lines (CRUBIT 12X, 13-15) changing.	Replace U8. If inputs normal, replace U1.
5	DATA SWITCHES 0-7 inoperative; all other switches normal.	Loss of ROW 0 enable.	Check ROW 0 at U7-6.	Periodically goes low (see figure 10-2).	Replace U7 if scan counter is functioning properly.
6	DATA SWITCHES 8-15 inoperative; all others normal.	Loss of ROW 1 enable.	Check ROW1 at U7-8.	Periodically goes low.	Replace U7.
7	ENTER function switches, MDD, MAI, MDE and CLR functions inoperative, all others normal.	Loss of ROW3 enable.	Check ROW 3 at U7-11.	Periodically goes low.	Replace U7.

Table 10-2. Programmer Panel Fault Isolation Procedures (Continued)

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
8	DISPLAY function switches inoperative.	Loss of ROW 2 enable or faulty switch block.	Check ROW 2 at U7-3.	Periodically goes low.	Replace U7. If problem persists, replace switch block.
9	Failure of two DATA switches and two function switches.	Faulty bit on multiplexer stage U1.	Press and hold suspect key and monitor column input to multiplexer stage U1: Column 0 (U1-1) – Data bits 0, 8, HALT/SIE, WPE Column 1 (U1-2) – Data bits 1, 9, RUN, PCE Column 2 (U1-3) – Data bits 2, 10, RST, STE Column 3 (U1-4) – Data bits 3, 11, LOAD, MAE Column 4 (U1-5) – Data bits 4, 12, WPD, MDD Column 5 (U1-6) – Data bits 5, 13, PCD, MAI Column 6 (U1-7) – Data bits 6, 14, STD, MDE Column 7 (U1-8) – Data bits 7, 15, MAD, CLR	When the switch is pressed, the associated input to the multiplexer should go low.	If normal, replace U1.

10.3.1 HOT MOCKUP CABLING. The 990 programmer panel connects to the hot mockup assembly (described in Section IV) as follows:

1. Disconnect chassis ac power plug from the ac supply.

2. Connect a 26-pin ribbon extender cable (Part Number 945023) between P3 on the 990/4 microcomputer board in the hot mockup chassis and the 26-pin ribbon cable connector on the programmer panel.

NOTE

When installing the extender cable, ensure that the arrows on the two connectors align with each other.

3. In the test configuration, the key switch on the hot mockup programmer panel controls the application of ac power to the chassis. However, all other functions are controlled by and displayed on the panel under test.

10.3.2 PRELIMINARY INSPECTION. Prior to applying ac power to the system, inspect the panel for the following:

1. Inspect the keys on the panel for signs of looseness when pressed.

2. Inspect the operation of the key switch. If too loose, disassemble switch and stretch tension springs. Reassemble switch and recheck operation.

3. Check ribbon cable and associated connector for signs of a loose connector or frayed wires. Repair if required (see Section V).

4. Inspect the cam on the rear of the key switch for signs of visible damage. If cam is damaged, replace switch.

SECTION XI

CRU EXPANDER BOARD TROUBLESHOOTING DATA

11.1 GENERAL

This section provides circuit analysis, checkout procedures and fault isolation procedures required to perform depot-level maintenance on the 990 CRU expander board, Part Number 945005-1.

11.2 FUNCTIONAL CIRCUIT ANALYSIS

The CRU expander board basically provides a 1 X 7 fanout of the CRU interface presented by the 990/4 microcomputer board and provides interrupt processing logic to permit the 990 software to determine which board in the seven possible expansion chassis issued an interrupt.

A functional block diagram of the 990 CRU expansion board is shown in figure 11-1 and the board layout is shown in figure 11-2.

11.2.1 CRU FANOUT LOGIC. The CRU expansion board provides a 1 X 7 fanout of the following CRU interface signals:

- TLIORES– (or TLPRES– using jumper option)
- CRUBITOUT
- CRUBIT (4-15)
- STORECLK–

Each of these signals, with exception of STORECLK–, is buffered and series terminated. STORECLK– is driven by a power gate which requires parallel termination in the CRU buffer board in the receiving chassis.

11.2.2 INTERRUPT RECOGNITION LOGIC. The interrupt recognition logic on the CRU expansion board is functionally divided into two sections, A and B. The "A" section monitors the interrupt lines from chassis 1-4 and reports interrupts to the computer over the INTA– line. Section B monitors the interrupts from expansion chassis 5-7 and reports interrupts via the INTB– line.

The interrupt request lines (INTREQ–) from all chassis are wire-ORed together, buffered, and sent to the computer as INTC–. The direct interrupt feature is used when faster interrupt processing response time is required by a peripheral in an external chassis.

When an interrupt present (INTPRES–) is detected by one of the two interrupt recognition sections, it develops a 2-bit binary word (ID(0,1)) which corresponds to the highest priority interrupt present. This binary word is decoded to send a logic-low ID enable signal (IDEN–) to the selected requesting chassis. The ID enable is a request for the external chassis's CRU buffer board to send back the ID word (ID(2-6)) which identifies the board in the external chassis that initiated the interrupt.

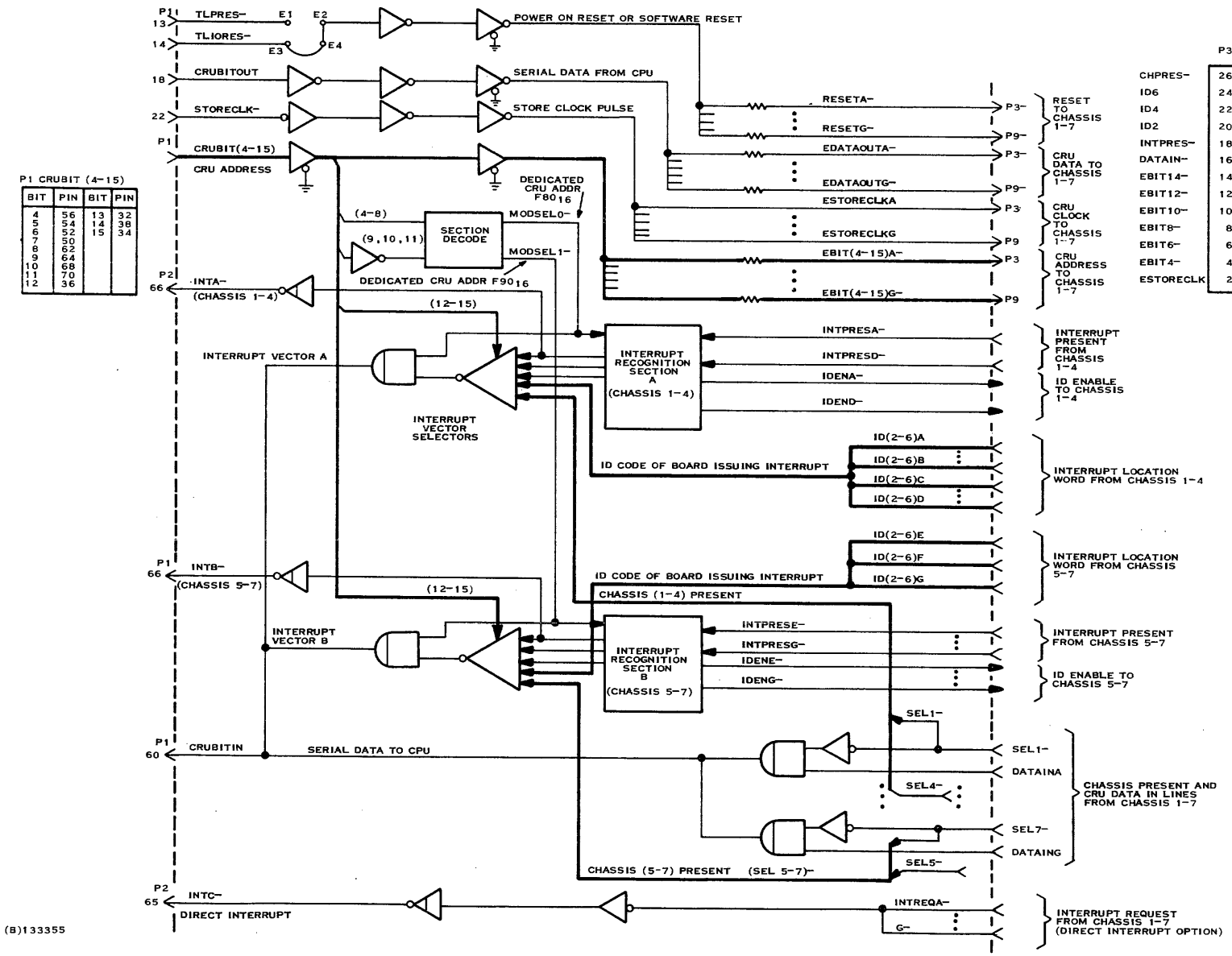


Figure 11-1. CRU Expansion Board, Block Diagram

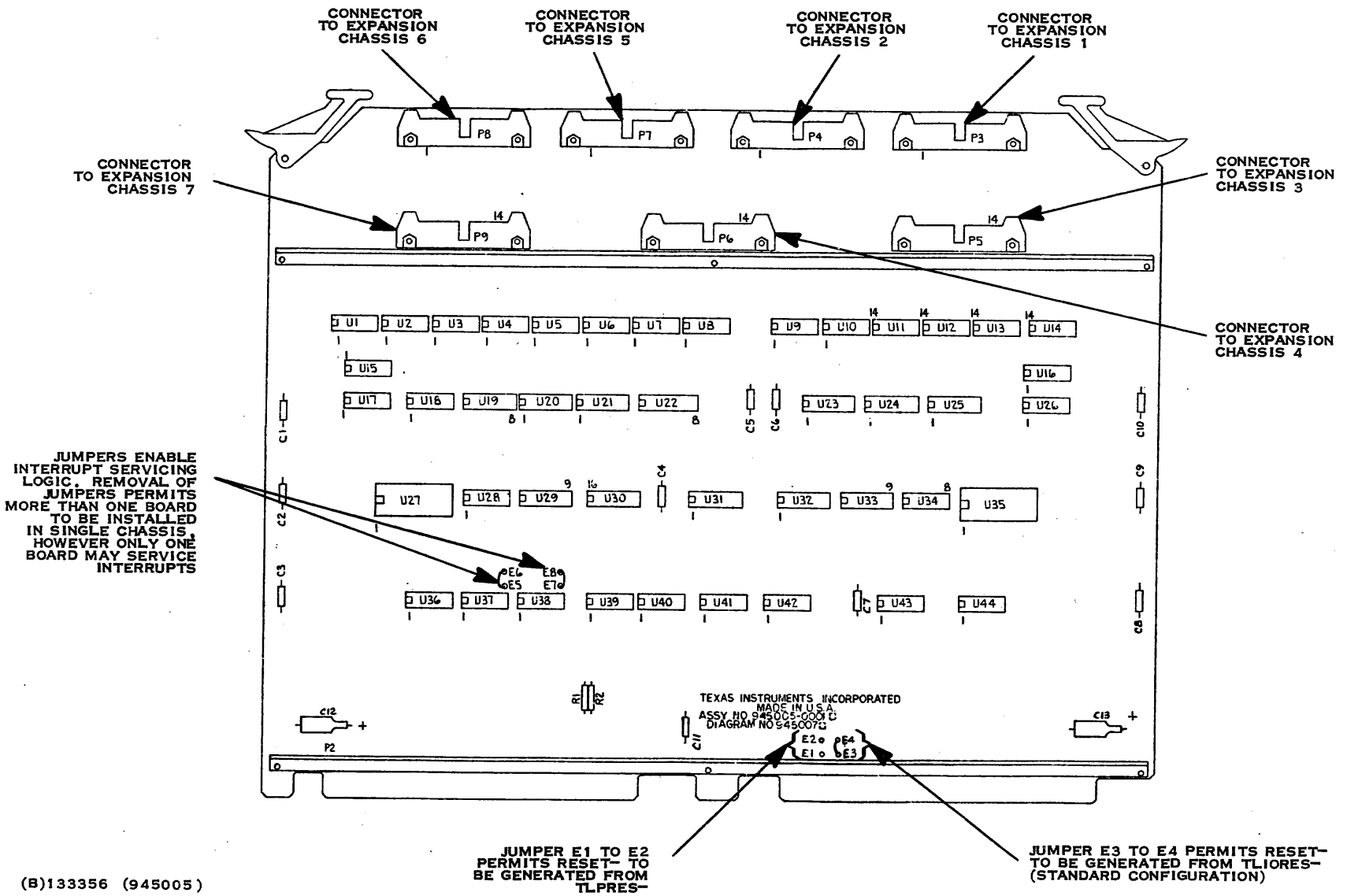


Figure 11-2. CRU Expansion Board Layout

In a similar fashion, section B of the interrupt recognition logic monitors and processes the interrupts from chassis 5 through 7. Provisions are incorporated on the board to permit software to address either the A or B interrupt section via an STCR addressed to either $F80_{16}$ (section A) or $F90_{16}$ (section B). Then by manipulating the CRU address lines 12-15, software is able to serially transfer a full 16-bit interrupt vector from either interrupt section to computer memory via the CRUBITIN data line. The interrupt vector format is shown in figure 11-3.

Note that the vector includes the encoded binary word (ID(0,1)) developed by the interrupt sections, the ID word returned from the external chassis and the chassis present (SEL–) lines from each expansion chassis (If a chassis is connected, its associated SEL– line will be a logic 0 level).

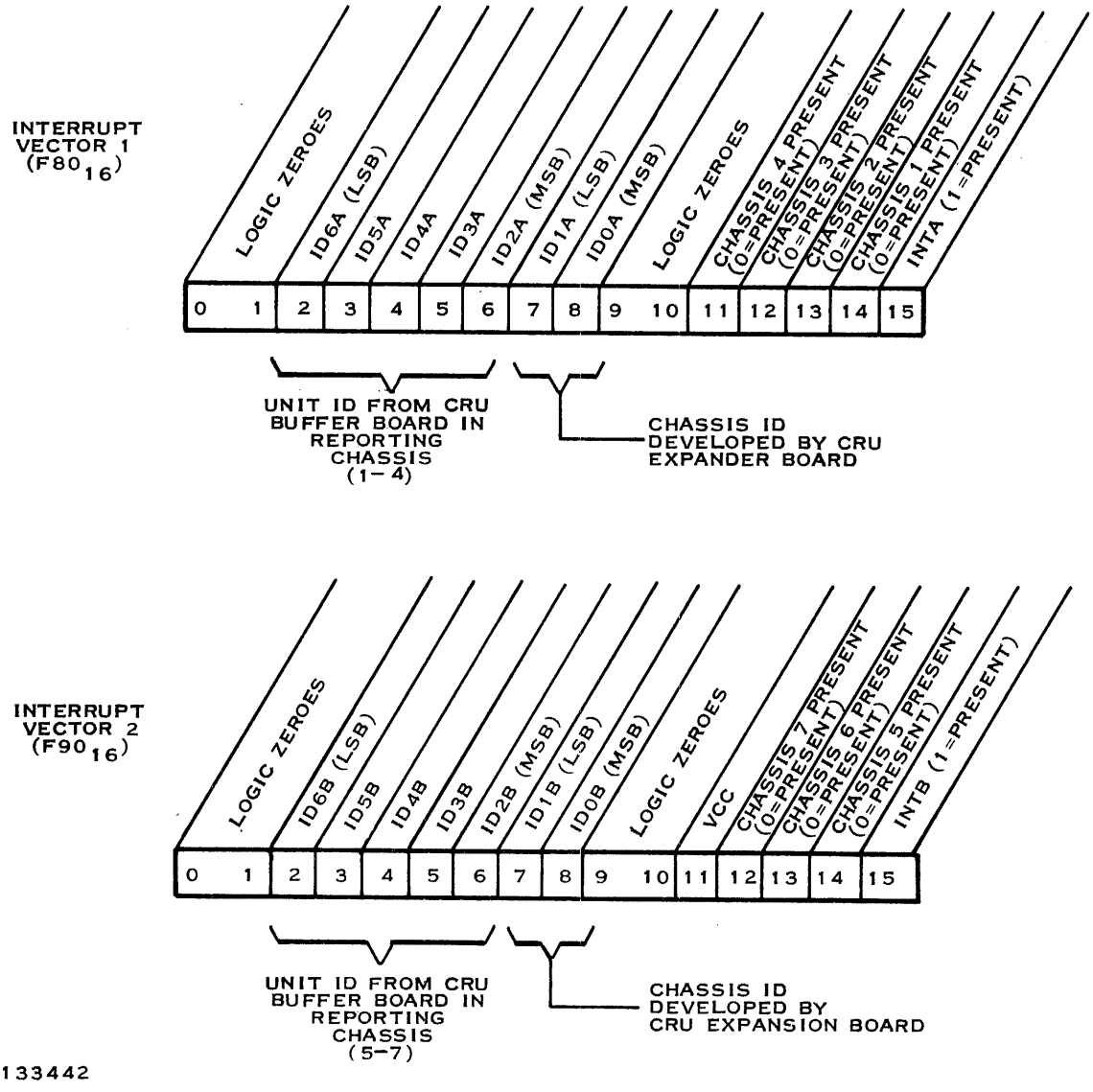


Figure 11-3. CRU Expansion Interrupt Vector Format

11.3 TROUBLESHOOTING PROCEDURES

Troubleshooting procedures for the CRU expansion board are based on the use of the checkout procedures in table 11-1 to isolate malfunctions down to a general area and the use of the logic diagrams and assembly drawings (in the *990 Family Maintenance Drawings Manual*) in conjunction with the fault isolation procedures in table 11-2 to isolate malfunctions down to the replaceable component level. Corrective maintenance procedures are then performed in accordance with the instructions in Section V of this manual. After the suspect defective component(s) has been replaced, the board is retested in accordance with the procedures in table 11-1.

Table 11-1. CRU Expansion Board Checkout Procedure

Step	Procedure	Normal Indication	If Abnormal
1	Install suspect board on extender board in hot mockup chassis in accordance with the directions provided in paragraph 11.3.1.	–	–
2	Insert the cassette containing the CRUEXP diagnostic (Part Number 945957) into the cassette transport in the 733 ASR data terminal.	–	–
3	Set POWER switch on 733 to ON position; set ON LINE switch to ON LINE position; press REWIND and wait for END indicator to light on 733 control panel.	END indicator should light within a few seconds.	See 733 ASR operators Manual.
4	Press LOAD and wait for READY indicator to light.	READY indicator on 733 lights.	–
5	Set 733 KEYBOARD, PLAYBACK and PRINTER switches to ON LINE position which places all further operations under 990/4 software control.	–	–
6	Set key switch on programmer panel to UNLOCK position. Press SIE/HALT switch.	RUN light extinguishes on programmer panel.	–
7	Press LOAD switch on programmer panel.	Cassette reels on 733 begins moving. PLAYBACK ON LED lights. Diagnostic execution begins when load is complete.	–
8	Permit diagnostic to execute to normal completion five times before pressing SIE/HALT switch on programmer panel.	Printout on 733 indicates successful test completion (see 990 diagnostic manual for error message printout interpretations).	See table 10-2.
9	Shut down power to the system and move the CRU buffer interface cable to P4 of the CRU expansion board. Move the open-ended cable previously connected to P4 to P3 on the expansion board.	–	–
10	Turn on power to the system and repeat steps 3-8.	Same as step 8.	See table 10-2.
11	Repeat steps 9 and 10 for each port on the CRU expansion board.	Same as above.	Same as above.
12	After last port (P9) has been tested, REWIND cassette. This concludes the CRU expansion board checkout procedure.	–	–

Table 11-2. CRU Expander Board, Fault Isolation Procedures

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
1	No interrupts reported for chassis 1-4; interrupt service normal on chassis 5-7.	Faulty priority encoder stage for A section.	Temporarily connect jumper between ground and U33-4 (interrupt input line from chassis 1). Check A0, A1 and E0 outputs of U33 stage.	E0 (U33-15) Logic 1 A0 (U33-9) Logic 0 A1 (U33-7) Logic 0	Replace U33
		Faulty driver stage for A section.	With jumper installed between ground and U33-4, check INTA– (U39-6).	INTA– (U39-6) Logic 0	Replace U39
2	No interrupts reported for chassis 5-7; chassis 1-4 normal.	Faulty priority encoder stage for B section.	Temporarily connect jumper between ground and U29-4. Check outputs of B section priority encoder stage U29.	E0 (U29-15) Logic 1 A0 (U29-9) Logic 0 A1 (U29-7) Logic 0	Replace U29
		Faulty driver stage for B section.	With jumper installed between ground and U29-4, check INTB– at U39-8.	INTB– (U39-8) Logic 0	Replace U39
3	Errors in ID field of interrupt vector for section A; interrupt vector for section B normal.	Faulty module 0 select decode.	Set up scoping loop to continuously read vector A (CRU address $F80_{16}$). Connect scope to MODSEL0– (U37-8).	MODSEL0– (U37-8) should periodically go low.	Replace U37. If problem persists, replace U19 and/or U20.
		Faulty ID enable circuit.	Set up a scoping loop to continuously read the interrupt vector from section A. Temporarily connect a jumper between ground and U33-4. Connect channel 1 scope probe to ID1A (U31-9). Connect channel 2 scope probe to ID0A (U31-10).	ID1A Logic 0 (U31-9) ID0A Logic 0 (U31-10)	Replace U31
			Move channel 1 probe to IDENA– (U32-1).	IDENA– should be logic 0.	Replace U32
			Check U32- pins 2, 3, and 4.	Should all be high.	Replace U32
			Move ground jumper to U33-4. Check Q outputs of U31.	U31-9 and U31-10 should both be high.	Replace U31
4	Unable to read interrupt vector for section A; section B normal.	Faulty output gating stage.	Set up scoping loop to read interrupt vector for section A. Check U41-10.	Should go high.	Replace U41 and/or U42.
5	Single bit error in interrupt vector for section A; section B normal.	Faulty multiplexer stage.			Remove and replace U35.

Table 11-2. CRU Expansion Board, Fault Isolation Procedures (Continued)

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
6	Unable to write data into one of seven expansion chassis.	Loss of store clock to chassis.	Set up a scoping loop to execute an SBO instruction to the inoperative chassis. Check ESTORECLK output to chassis.	Clock output periodically goes low.	Replace associated output driver (U15, U16, U17 or U26).
7	Unable to send or receive data from chassis 1-4; chassis 5-7 normal.	Faulty output data driver.			Replace U25
8	Unable to communicate with chassis 5-7; chassis 1-4 normal.	Faulty output data driver.			Replace U22
9	Unable to communicate with groups of card slots in chassis 1-7.	Faulty CRU address driver stage.	Evaluate CRU addresses which are failing and replace associated driver stage.		Remove and replace U19 and/ or U20.
10	Unable to communicate with groups of boards in chassis 1-4; chassis 5-7 normal.	Faulty address CRU driver.	Same as above.		Remove and replace U21, U22 or U23.

11.3.1 **CRU EXPANSION HOT MOCKUP.** The hot mockup required to perform depot-level maintenance on the CRU expander board and/or CRU buffer board is shown in figure 4-1 (Section IV). As indicated in this figure, the CRU expander board is mounted on an extender board and inserted into any available full-size board slot in the 990/4 chassis.

In the expansion chassis, a CRU buffer board (also mounted on an extender board) is installed in slot 1. Place the Jumper J2 in jumper location 1 (CRU address 200_{16}, base address 0400). A 16 I/O data module with loop-back plug is installed in the lowest CRU slot in the chassis (slot 6 or slot 13). A cable is then installed between P3 of the CRU expander board and P3 of the CRU buffer board to provide the electrical interconnections between the two chassis. The chassis front panel cable is connected to P5 on the buffer board. A full complement of cables (Part Number 945001) should also be installed on the remaining connectors (P4-P9) on the CRU expansion board to provide proper loading of the board's output drivers (the loading effect occurs even though the other end of the cable is not connected to an associated CRU buffer board).

SECTION XII

CRU BUFFER BOARD TROUBLESHOOTING DATA

12.1 GENERAL

This section provides functional circuit analysis and troubleshooting procedures for performing depot-level maintenance on the 990 CRU buffer board, Part Number 944905-1.

12.2 FUNCTIONAL CIRCUIT ANALYSIS

The CRU buffer board performs a module select decode and CRU fanout/fanin function similar to that performed by the CRU interface logic on the 990/4 microcomputer board. The buffer board decodes CRU address lines from the 990/4 chassis (via the 990 CRU expansion board) to generate the low-active Module Select signals for the CRU interface boards within the expansion chassis.

The board also buffers the CRUDATAOUT, CRUSTORECLK, TLIORES– and CRUBITOUT lines between the main chassis and all CRU slots in the expansion chassis.

An interrupt scanner circuit on the buffer board (figure 12-1) continuously monitors for the presence of interrupts from any of the CRU buffer boards in the chassis and issues an Interrupt Present (INTPRES–) if an interrupt is detected on any line. The buffer board then enables the ID word (ID(2-6)) which identifies which board in the expansion chassis issued the interrupt when ID Enable signal (IDENA) is received from the CRU expansion board.

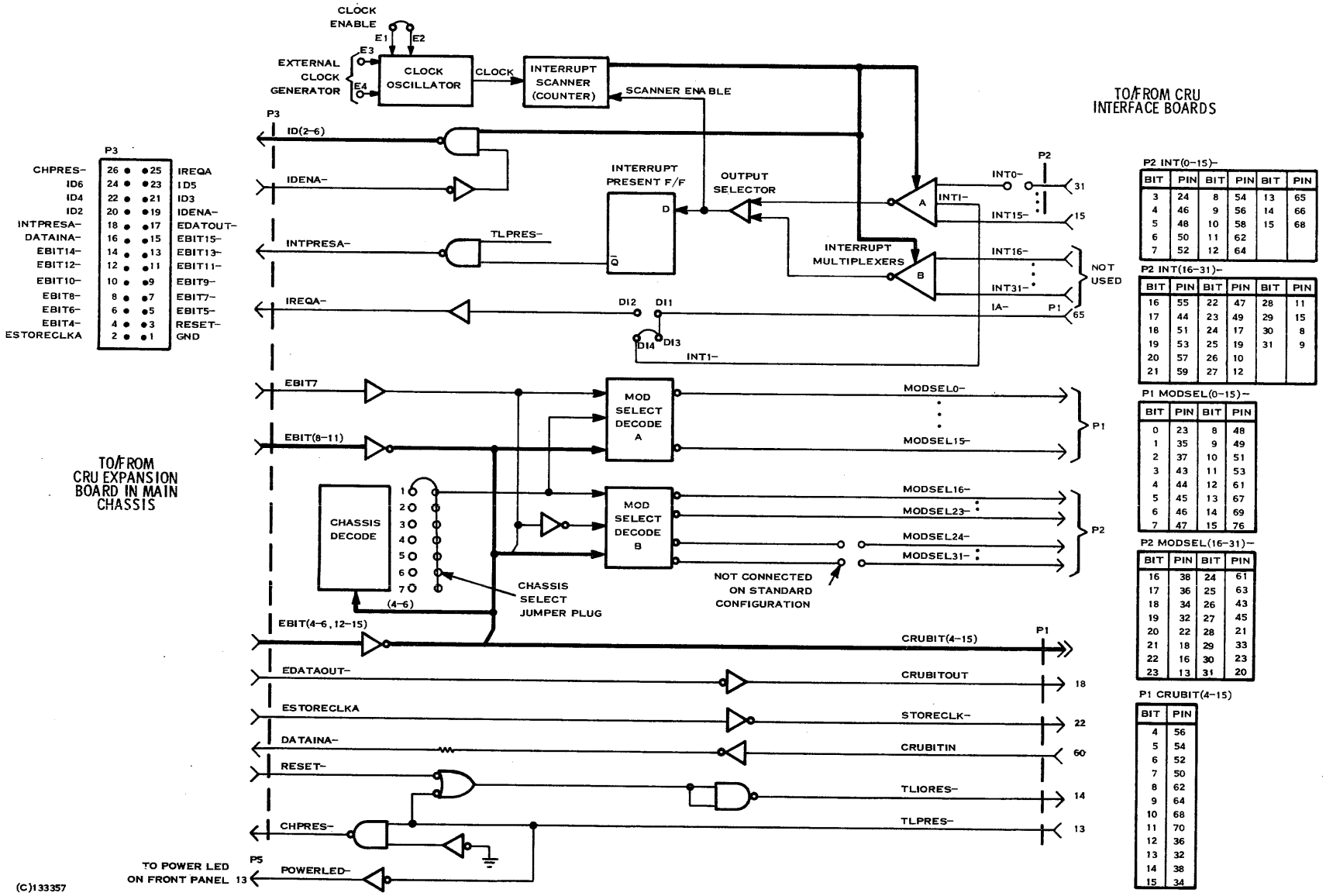
12.2.1 INTERRUPT SCANNER LOGIC. The CRU buffer board contains provisions for encoding up to 32 interrupts onto a single interrupt line to the CRU expander board and supplying the expander board, on request, the ID of the board which originated the interrupt. However, in the present 13-slot chassis, only the first 15 interrupt lines (INT(1-15)–) are actually connected into the scanner circuitry (see paragraph 12.2.2 for wiring options).

The interrupt scanner consists of a clock oscillator stage (U21, U10 plus R1 and C1), a 5-bit counter (U11 and U12), two 16-bit multiplexer stages U1 and U2, a multiplexer selector U17, interrupt present flip-flop stage U22, and output driver stage U15.

The scanner oscillator, which is enabled when jumper E1 is connected to E2, develops a 250 nanosecond pulse train used to advance the 5-stage scan counter. The 4 least significant counter outputs (U11, pins 14, 13, 12 and 11) are used to address the two interrupt multiplexer stages U1 and U2. The most significant counter output bit (and its complement) is used to control the multiplexer selector stage U17. The output of the selector is also routed back to the counter inputs which permit the counter to be inhibited when an interrupt is detected by either of the multiplexers.

The output of the multiplexer selector stage U17 (INTPRES–) is clocked into the interrupt present flip-flop stage U22 and routed to the CRU expansion board in the main chassis.

When the ID enable is received from the expansion board, the outputs from all five stages of the scan counter are sent to the CRU expansion board for use by software in constructing the interrupt vector which identifies which chassis and which board slot issued the interrupt.



P2 INT(0-15)-

BIT	PIN	BIT	PIN	BIT	PIN
3	24	8	54	13	65
4	46	9	56	14	66
5	48	10	58	15	68
6	50	11	62		
7	52	12	64		

P2 INT(16-31)-

BIT	PIN	BIT	PIN	BIT	PIN
16	55	22	47	28	11
17	44	23	49	29	15
18	51	24	17	30	8
19	53	25	19	31	9
20	57	26	10		
21	59	27	12		

P1 MODSEL(0-15)-

BIT	PIN	BIT	PIN
0	23	8	48
1	35	9	49
2	37	10	51
3	43	11	53
4	44	12	61
5	45	13	67
6	46	14	69
7	47	15	76

P2 MODSEL(16-31)-

BIT	PIN	BIT	PIN
16	38	24	61
17	36	25	63
18	34	26	43
19	32	27	45
20	22	28	21
21	18	29	33
22	16	30	23
23	13	31	20

P1 CRUBIT(4-15)

BIT	PIN
4	56
5	54
6	52
7	50
8	62
9	64
10	68
11	70
12	36
13	32
14	38
15	34

Figure 12-1. CRU Buffer Board, Block Diagram

The interrupt logic on the CRU buffer board also includes an option to bypass the scanner for interrupt 1 (IA–). In this case, the interrupt is wired to the interrupt request gate U15 and used to generate a low-active IREQA– signal. This signal is wire-ORed on the CRU expansion board with the IREQ– signals from all seven CRU buffer boards. The direct interrupt option is used when a peripheral requiring more rapid interrupt processing time is implemented in an expansion chassis.

The interrupt scanner section also contains provisions for disabling the internal interrupt scanner clock and using an external pulse generator to advance the counter. Provisions are also included for clearing the counter manually. The jumper connections associated with the maintenance options are described in paragraph 12.2.3.

12.2.2 **MODULE SELECT DECODING.** The module select decode function performed by the CRU buffer board is similar to the function provided in the main chassis by the 990/4 microcomputer board. To set up the chassis address to correspond to the CRU expansion board connector (may be connected to any connector from P3 to P9), a single jumper wire is installed on the 14-pin socket P4 (as described in paragraph 12.2.3). Then if the incoming CRU address lines (EBIT4-11) indicate an address within the chassis address space, one of the 24 module select lines (MODSEL(0-23)–) goes low. This signal is routed to the appropriate CRU board slot via the chassis backpanel board.

The CRU buffer board has provisions for decoding up to 32 module selects but the option is not wired up on the conventional system.

12.2.3 **CRU BUFFER OPTIONS.** The following jumper options are available on the CRU buffer board:

- Option to wire interrupt 1 either directly to the CRU expansion board in the main chassis or wiring the interrupt through the interrupt scanner. If J1, pins 1 and 2 are connected, the interrupt is sent directly; if J1, pins 3 and 4 are connected, the interrupt uses the scanner circuitry (normal configuration).

- Module select decodes 24 through 31 – Jumpers installed between appropriate P2 pins (see logic diagram 944907, sheet 2) and M 24-31 (see figure 12-2).

- Chassis select – A single jumper is installed on 14 pin socket P4 as follows:

Expander Connector	Jumper Pins on P4	Chassis Number
P3	1, 14	1
P4	2, 13	2
P5	3, 12	3
P6	4, 11	4
P7	5, 10	5
P8	6, 9	6
P9	7, 8	7

12.3 CRU BUFFER BOARD TROUBLESHOOTING PROCEDURES

The CRU buffer board is installed in the hot mockup system as described in paragraph 11.3 (CRU expansion board hot mockup description). Checkout procedures for the buffer board are provided in table 12-1 and the fault isolation procedures are contained in table 12-2. The associated corrective maintenance procedures are provided in Section V.

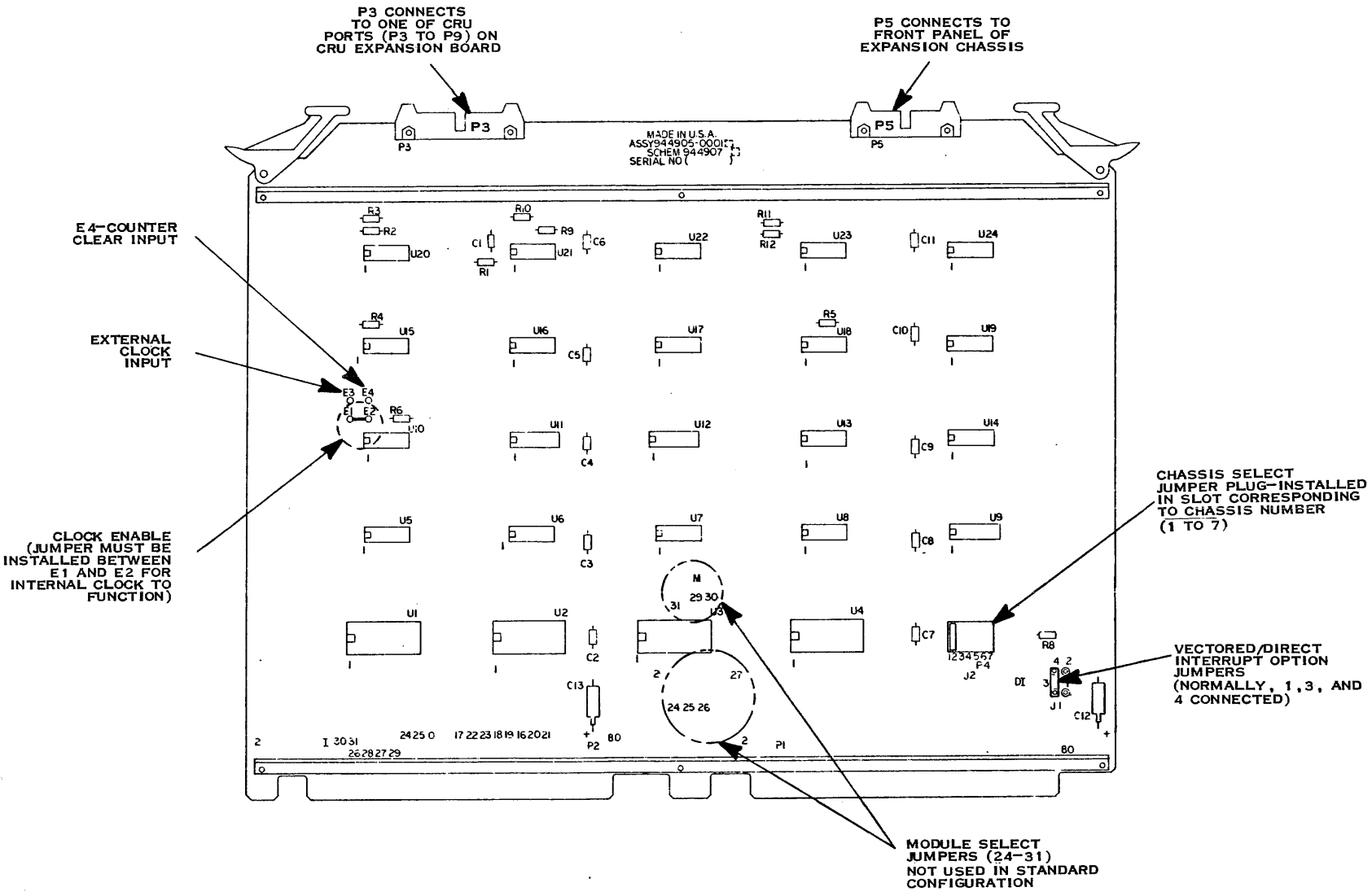


Figure 12-2. CRU Buffer Board Layout

Table 12-1. CRU Buffer Board, Checkout Procedures

Step	Procedure	Normal Indication	If Abnormal
1	Turn off power to the external chassis and install the suspect buffer board in slot 1 of the expansion chassis of the hot mockup system.	–	–
2	Connect scope to CHPRES– (U15-6).	Logic-zero	Replace U15 and/or U21.
3	Ensure that jumper is installed between E1 and E2 (clock enable).	–	–
4	Apply ac power to the expansion chassis (key switch to ON position).	–	–
5	Connect scope to interrupt scanner outputs (U11 - pins 11-15).	All outputs are toggling.	See table 11-2.
6	Connect scope to U15-8 (INTPRESA–). Temporarily short P1-66 to ground.	INTPRESA– goes low and remains low.	See table 11-2.
7	Shut down power to the external expansion chassis and the 990/4 chassis. Install a 26-pin ribbon cable between P3 of the buffer board and P3 of the expander board in the 990/4 chassis (see figure 4-1).	–	–
8	Install jumper between pin 1 and pin 14 of IC jumper plug P4 (corresponds to chassis 1).	–	–
9	Cable up remainder of system in accordance with the instructions in paragraph 11.3.1.	–	–
10	Insert the cassette containing the CRUEXP diagnostic (Part Number 945957) into the cassette transport in the 733 ASR data terminal.	–	–
11	Set POWER switch on 733 to ON position; set ON LINE switch to ON LINE position; set CONT/START/STOP switch to STOP position; press REWIND and wait for END indicator to light on 733 control panel.	END indicator should light within a few seconds.	See 733 ASR operators Manual.
12	Press LOAD and wait for READY indicator to light.	READY indicator on 733 lights.	–
13	Set 733 KEYBOARD, PLAYBACK and PRINTER switches to ON LINE position which places all further operations under 990/4 software control.	–	–
14	Set key switch on programmer panel to UNLOCK position. Press SIE/HALT switch.	RUN light extinguishes.	–
15	Press LOAD switch on programmer panel.	Cassette reels on 733 begin moving. Diagnostic execution begins upon completion of load operation.	
16	Permit diagnostic to execute to normal completion five times before pressing SIE/HALT switch on programmer panel.	Printout on 733 indicates successful test completion (see 990 diagnostic manual for error message printout interpretations).	See table 11-2.
17	Press REWIND on 733 ASR. When rewind operation is complete, remove cassette from transport.		

Table 12-2. CRU Buffer Board, Fault Isolation Procedures

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
1	Unable to communicate with one CRU board slot – all others normal.	Loss of module select.	Set up scoping loop which addresses inoperative board slot.	MODSEL(n)– goes low periodically.	Replace U3 or U4.
2	Interrupts not reported at any level.	Loss of scanner clocks.	Connect channel 1 probe to clock output (U10-3).	U10-3	Ensure that clock enable jumper E1 to E3 is installed. If so, replace U10 and/or U21. If problem persists, replace C1 and/or U16.
		Faulty interrupt scanner stage.	Monitor outputs of scan counter (U11, pins 11 to 15).	All outputs are toggling.	Check for CLK3– at U11-2. If absent, replace U10. If clock is normal, check enable at U11-10. If high, replace U11.
		Faulty interrupt multiplexer stage.	Connect ground jumper to pin 18 of U1. Connect scope to the output of mpx stage U1-10.	U1-10 goes low and remains low as long as ground jumper is installed (scan counter also halts with U11-13 high and U11-pins 11, 12, 14, and 15 all with logic 0 levels).	Replace U1. If U1-10 periodically goes low, replace U17.
3	Data errors on all chassis addresses.	Faulty data or clock driver stage.	Set up scoping loop to continuously execute an SBO instruction at any board slot in the chassis. Connect channel 1 scope probe to CRUBITOUT (U23-6). Connect channel 2 probe to STORECLK– (U23-8).	CRUBITOUT (U23-6) STORECLK– (U23-8)	Replace U23
		Faulty CRU address drivers.	Set up scoping loop to continuously execute an SBO instruction for bit 0 at one of the CRU addresses in the expansion chassis; monitor the address outputs at U19-6, U24-6, U19-8, U24-8.	All outputs should be low.	Replace associated IC (U19, U23 or U24).
		Faulty data in driver.	If the above steps result in normal indications, the CRU data in line is probably at fault.		Replace U21
4	Data errors in same bits on all CRU board addresses.	Faulty CRU address driver stage.	Evaluate error message printout and determine which bit positions are failing.		Remove and replace U19, U23 and/or U24.

Table 12-2. CRU Buffer Board, Fault Isolation Procedures (Continued)

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
5	Unable to communicate with any board slot in the chassis.	Channel present signal is high.	Check output at U16-6.	Logic low level.	Replace U15 and/or U21.
		Chassis jumper not properly installed in J2/P4.	Check jumper wiring at J2/P4 both visually and with an ohmmeter.	Jumper connections installed in accordance with figure 11-2.	Install appropriate jumper and repeat test.
6	Unable to communicate with groups of CRU boards in the chassis – other CRU board groups normal.	Faulty CRU address driver stage.	Set up scoping loop to continuously address one of the faulty board addresses. Check outputs of U13-8, U14-8 and U14-6.	Outputs should be same as CRU address bits 4-6 (memory address bits 3-5) issued by scoping loop program.	Remove and replace U13 and/or U14.

SECTION XIII

POWER SUPPLY TROUBLESHOOTING DATA

13.1 GENERAL

This section contains theory of operation and troubleshooting information required to perform depot-level maintenance on the power supply boards used in the 990/4 microcomputer and expansion chassis.

The board types covered in this section include:

- Ac power converter board
- 20 ampere main power supply board
- 40 ampere main power supply board
- Standby power supply board

13.2 FUNCTIONAL DESCRIPTION

Functionally, the power supply section develops the regulated dc voltages required to power the logic boards, generates the power up master clear signal (TLPRES–) which remains low until power supply voltages are stable, develops a power fail warning (TLPFWP–) when a power failure is imminent, and generates a 120 Hz real time clock output used by the 990/4 microcomputer board to develop real time clock interrupts.

Each of the 990 power supply boards is described in greater detail in the following paragraphs.

13.2.1 AC POWER CONVERTER BOARD. The ac power converter board performs the function of converting the input ac power (normally 115 vac) into an unregulated +160 vdc (±20%) used to drive the main and standby power supply boards. The power converter board also develops a 120 Hz sinewave output which is converted into real time clock pulses on the main power supply board. A schematic diagram of the ac power converter board is shown in figure 13-1.

The 115 vac input power from the chassis power distribution circuits is applied across a full-wave bridge rectifier (CR1) through two 5 ohm thermal resistors which limit surge current during initial power turn-on. The output of the bridge rectifier is capacitively filtered by 1C1 which is connected to the J2 outputs of the ac converter board. Additional high-frequency filtering is provided by the onboard capacitor C2. Three 160 vdc outputs (and associated ground returns) are provided. These provide for the electrical connection to 1C1 and provide +160 vdc for the main and optional standby power supply boards. The 120 Hz sinewave output used to develop the real time clocks is produced as follows. The 115 vac input power is routed to a second bridge rectifier unit (CR2) via series limiting resistors. The rectified output (120 Hz) is optically coupled to output pins J3-3 and J3-4 via the optical converter stage U1.

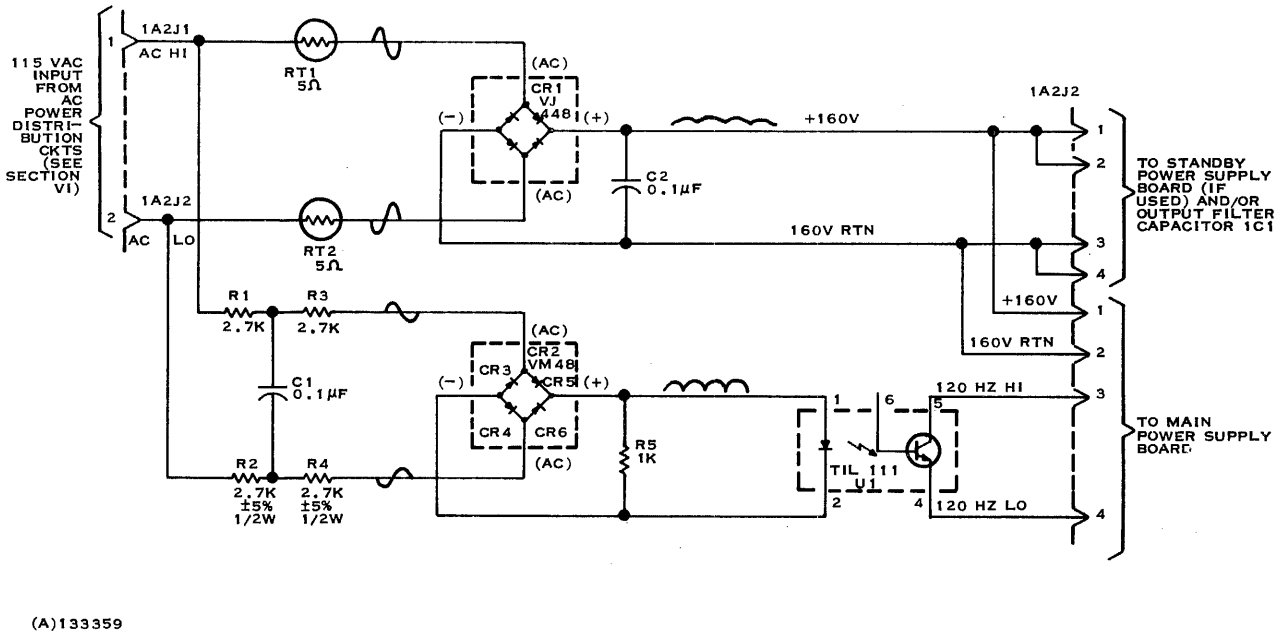


Figure 13-1. Ac Power Converter Board Schematic Diagram

13.2.2 20 AMPERE MAIN POWER SUPPLY BOARD. The main power supply is a ringing choke (flyback) dc to dc converter type power supply. The incoming +160 vdc from the ac power converter board is converted to a pulsating dc voltage and fed to the primary winding of a step-down transformer with several secondary windings. The resulting ac voltages appearing across the secondary windings are rectified, filtered and highly regulated to produce the following regulated output voltages:

- +5 MAIN (+5 vdc, ±3%, 20A)
- +12 MAIN (+12 vdc, ±3%, 2A)
- -5 MEM (-5 vdc, ±6%, 1A)
- -12 MAIN (-12 vdc, ±6%, .05A)

For the following discussion of the 20 ampere main power supply board, refer to the simplified schematic diagram in figure 13-2 and the 20 ampere main power supply schematic diagram (944972).

As shown in figure 13-2, the 160 vdc (unregulated output of the ac power converter board) is applied to the primary winding of T1 which is in series with the switching transistor stage Q2. At this time, capacitor C8 begins charging toward the +160 vdc input through R85. When the voltage across capacitor C8 exceeds the base-emitter threshold of Q2 (approximately 0.6 volts), Q2 turns on to produce an initial current through the primary of T1. The primary current produces a positive-going voltage at secondary number 4 that is applied through C8 to the base

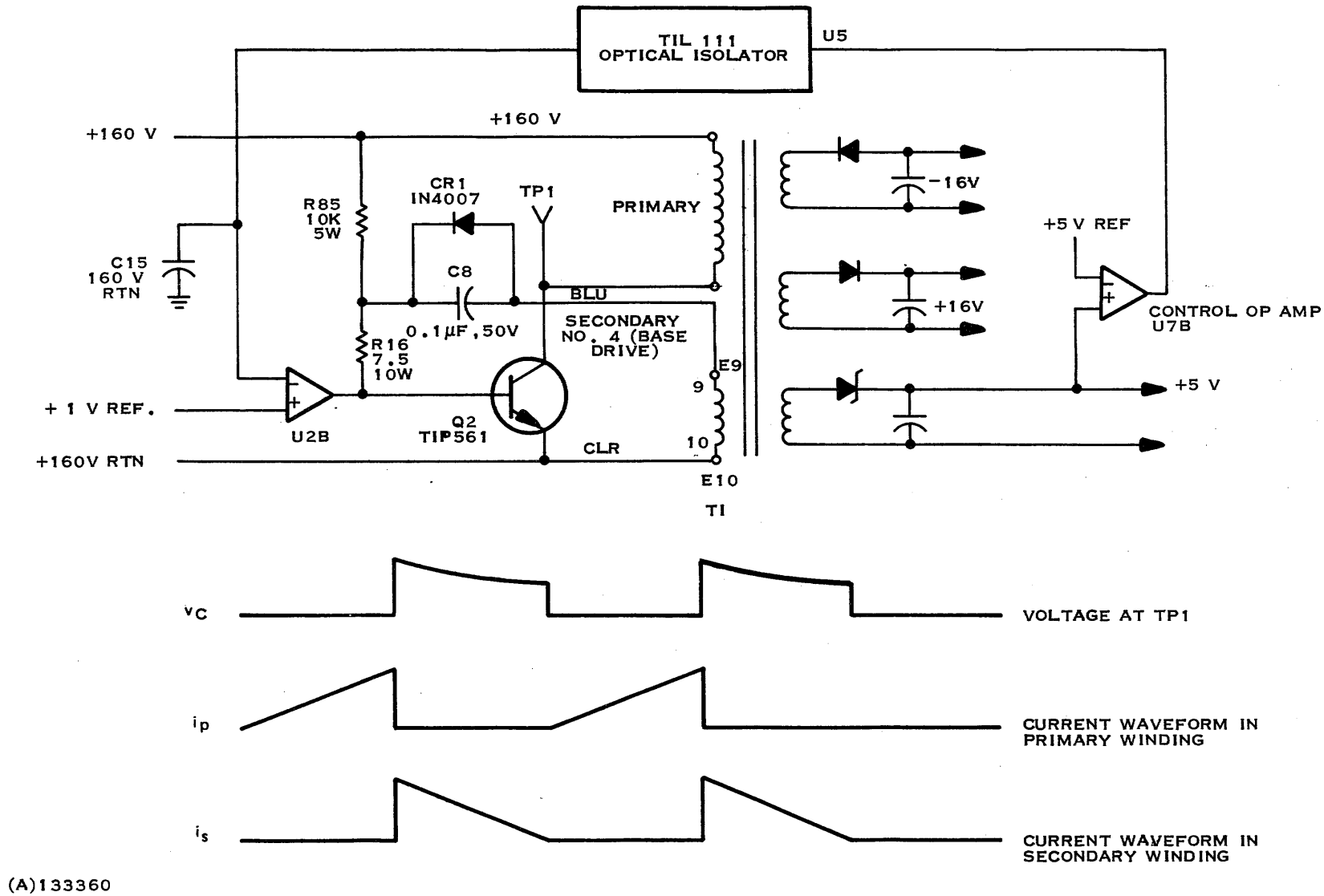


Figure 13-2. 20 Ampere Main Power Supply Board, Simplified Schematic Diagram

of Q2. Q2 then conducts more current and the regenerative process is repeated to quickly turn Q2 completely on to initiate the charging cycle. Since the conduction drop across Q2 is relatively small, the application of +160 volts across the primary winding produces a sawtooth of current through the winding as shown in the i_p waveform in figure 13-2. During the charging cycle, the voltages induced in the secondary windings are of the wrong polarity to produce outputs from the half-wave rectifier circuits so the primary of T1 acts like a simple inductor. For given output circuit conditions, the output transistor of optical isolator U5 acts as a constant current source that charges capacitor C15. The linearly increasing voltage across C15 is applied to the inverting input of U2B; a 1 volt reference voltage is applied to the noninverting input.

When the voltage across C15 exceeds 1 volt, the output of U2B goes low which biases the switching transistor stage Q2 at cutoff. The collapsing magnetic field (flyback) in transformer T1 results in an induced voltage in each of the three secondary windings. The ac induced in the first two secondary windings is half-wave rectified and filtered to produce the ± 16 vdc used to drive the ±16 volt regulators. The output of the third winding is rectified and filtered to develop the +5 MAIN output dc voltage.

The reversal of voltage in secondary number 4 of transformer T1 (see figure 13-2) discharges capacitor C15 (through a diode-resistor branch not shown on the simplified schematic diagram) which initiates another charge cycle.

The +5 volt output of the 20 ampere power supply is controlled by feedback action. Assume that the output is too high and produces a relatively high input to optical isolator U5. The resulting high output current from U5 then charges C15 at a greater rate. As a result, the voltage across C15 reaches the 1 volt threshold voltage of U2B and terminates the charge cycle earlier. The reduced peak primary current of T1 reduces the average primary and secondary currents, thus reducing the output voltage. Since shorter charge and flyback times are involved, the frequency of operation is increased. A lower +5 volt output (e.g., due to a greater load current) reduces the constant current output of U5, thereby lengthening the charging cycle. The resulting increased peak primary current produces increased average currents in T1, thereby increasing the output voltage. Longer charge and flyback times produce a lower frequency of operation. The frequency of operation under various input voltage and output load conditions generally varies between 17 kHz and 50 kHz. Transformer T1 has a step gap construction that sets a lower limit on the inductance of the windings. That results in limiting the operating frequency of the power supply to approximately 50 kHz.

13.2.2.1 Main Power Supply Board, Detailed Circuit Analysis. The remainder of the main power supply theory of operation is based on the detailed block diagram shown in figure 13-3 and the schematic diagram (944972).

As previously discussed, the +160 vdc is applied across the inputs of the main power supply. The primary voltage reference for voltage comparitor and latch stage U1 is adjusted for 130 volts dc. When the input power exceeds that value, the latch sets. The output of the latch is coupled to the TLPRES and TLPWPF stages U9 and U11 through the optical coupler stage U3.

If the output of the ac converter board drops to approximately 120 volts, the voltage comparator stage U1 switches off which results in a TLPFWP– being generated. This power fail warning signal allows the 990/4 microcomputer board approximately 7 milliseconds to transfer all data out of the TMS 9900 into program memory. If the system is equipped with a standby power supply, memory power is then automatically supplied by the dc storage batteries.

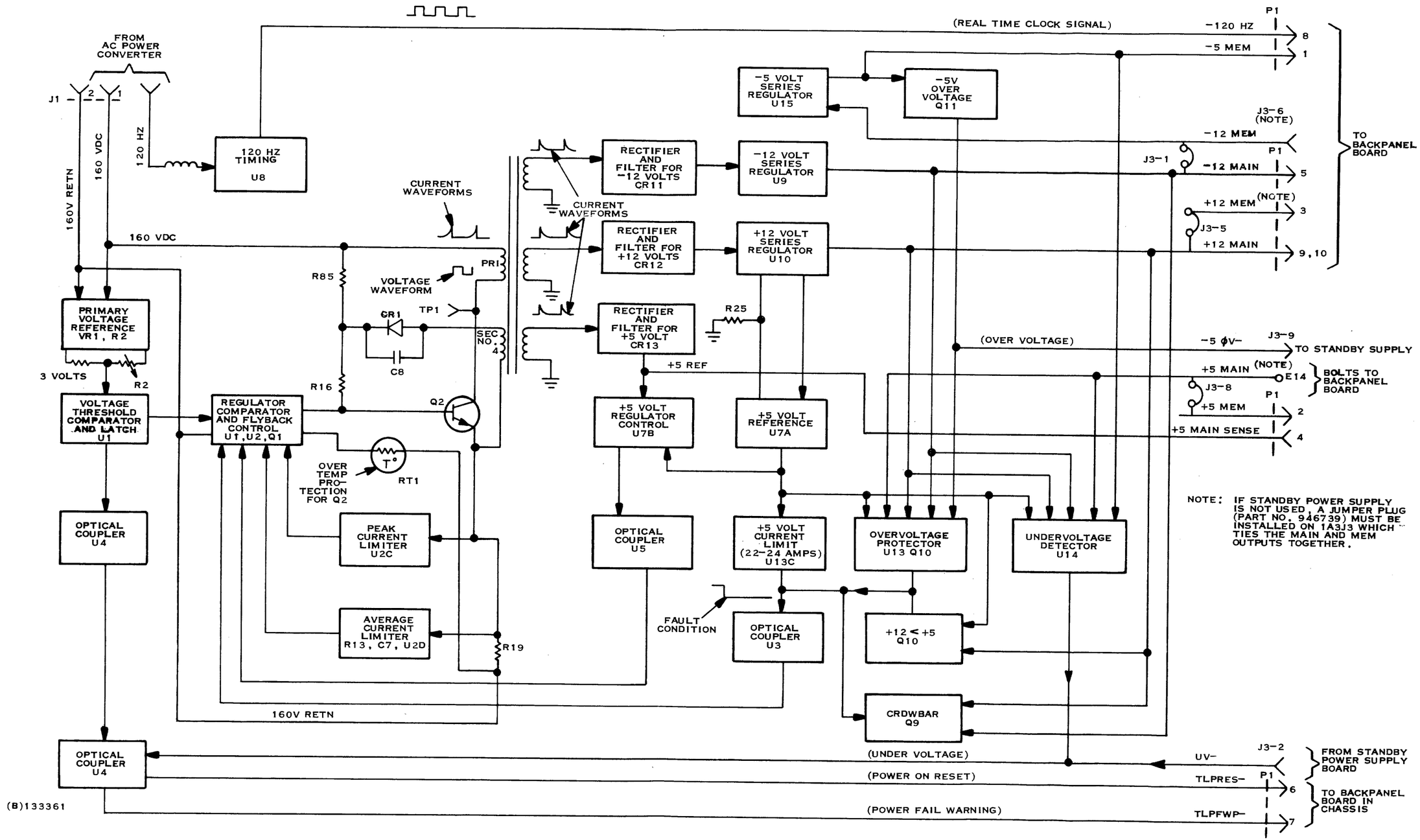


Figure 13-3. 20 Ampere Main Power Supply Board, Detailed Block Diagram

The flyback control circuit (U1 and U2) causes the switching transistor stage Q2 to switch on and off at a relatively high frequency rate as described in paragraph 13.2.2.

The induced current in the secondary windings is rectified and filtered by stages CR11-CR13. The ±16 vdc outputs of CR11 and CR12 are tied to the inputs of the series regulator stages U6 and U10. The +5 volt MAIN output of CR13 is sensed and compared to a +5 volt reference level applied to the +5 volt regulator control circuit U7B. A signal from the +5 volt control circuit is optically coupled back to flyback control circuit to control the frequency of the switching transistor circuit as previously explained.

The series regulator stage U15 provides the -5 MEM output from either the -12 MEM input from the standby power supply (if used) or from the -12 MAIN output. Similarly, the +5 MAIN output is patched to the +5 MEM if the standby supply is not used.

Over-voltage Protection. As indicated in figures 13-3 and 13-4, an over-voltage condition at any of the power supply outputs, over-current condition on the +5 MAIN output or primary winding of transformer T1 or an over-temperature condition at the heatsink for switching transistor stage Q2 shuts down the entire power supply (crowbars the power supply) and the ac power must be turned off and then turned back on to restart the power supply.

An over-voltage on any output voltage or an over-current in the +5 MAIN output produces an output from U13 or Q10 that is optically coupled back to the flyback control circuit (via U3) to trigger an SCR stage Q9 that shuts down the power supply. A nondestructive shutdown also occurs if the peak current in the primary winding of T1 exceeds 10 amperes of if the average current through the winding exceeds 2.5 amperes (as sensed by the voltage drop across R19). Thermistor RT1 also develops a shutdown signal if the temperature of the Q2 heatsink exceeds 105 degrees C.

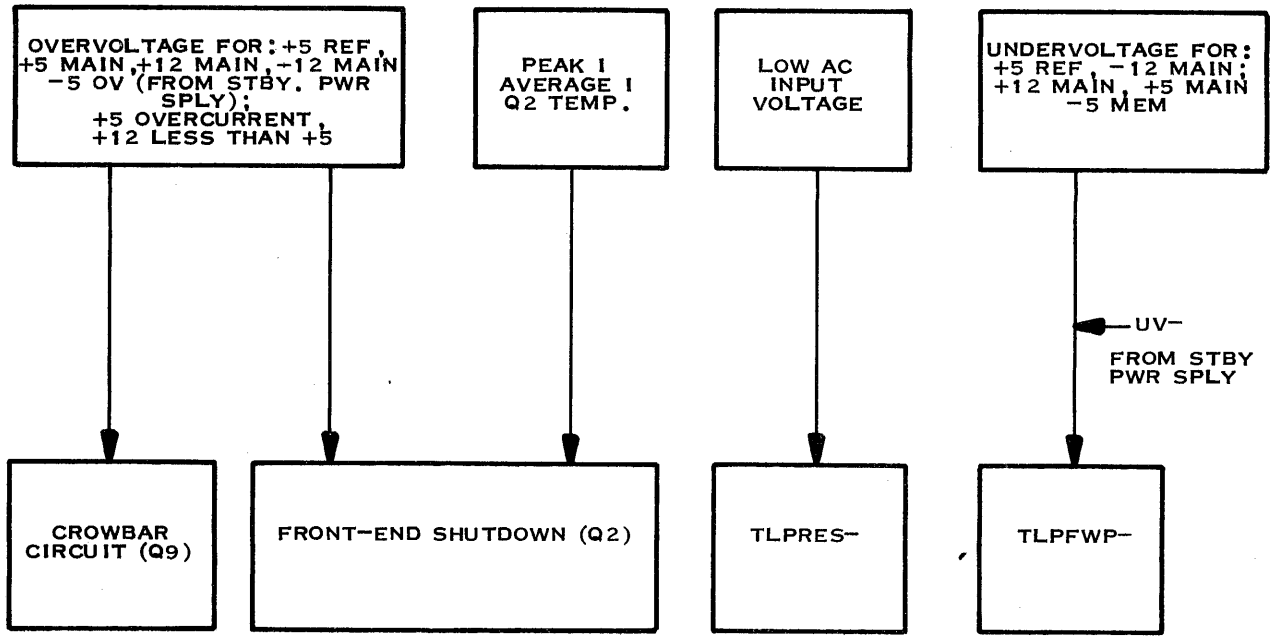


Figure 13-4. Interrelationship of 20A Power Supply Shutdown Controls

Real Time Clock Outputs. The main power supply board also receives a 120 Hz sinewave input from the ac converter board and provides pulse shaping and driver functions on the signal before sending the 120 Hz pulse train to the 990/4 microcomputer board for use by the real time clock interrupt circuits.

13.2.3 **STANDBY POWER SUPPLY.** The standby power supply is an optional power supply system consisting of a standby power supply board and a set of storage batteries which provide the regulated voltages used in the 990 memory section. The standby supply automatically switches to battery power to prevent loss of data in the dynamic memory of the computer when ac power fails (output of ac power converter board drops to approximately +120 vdc).

During normal ac power conditions, the standby power supply derives its input power from the +160 volt dc output from the power converter assembly in the main power supply. The standby supply then converts the unregulated dc input into the regulated ±12 and +5 volts dc voltages required by the RAM memories used in the computer. The standby supply also contains a battery charger circuit used to provide charging current for the storage batteries.

In the event that the output of the power converter assembly drops below a predetermined voltage level (approximately 120 volts), the standby power supply generates UV– to notify the main power supply board of impending power failure and automatically switches to battery operation. The under voltage signal (UV–) is used by the main power supply to generate the power fail warning (TLPFWP–) signal sent to the computer circuit board. When the batteries discharge to the minimum functional voltage level, the standby power supply shuts down (approximately 30 minutes of standby operation).

When normal ac power is restored, the standby supply develops an equalizing voltage which charges the standby batteries until the charge current drops to the trickle charge level. The supply then switches to a float voltage to maintain the batteries at full charge. The standby power supply also prevents battery operation unless ac power is first applied to the system (+160 volts dc output of the ac power converter is within tolerance).

Another feature of the standby power supply is an over-voltage protection circuit that disables the standby supply and blows the battery fuse in the event that any of the memory voltages exceed predetermined values.

Functionally, the standby power supply consists of the following major circuits:

- 160 volt to 20 volt converter
- 12 volt converter
- Regulator control
- 5 volt regulator
- 12 volt over-voltage protection circuit
- 5 volt over-voltage protection circuit
- Battery charger circuit
- Battery circuit

A simplified block diagram of the standby power supply is shown in figure 13-5. For the following discussion, reference should also be made to the schematic diagram for the standby power supply board (944992).

13.2.3.1 **160 Volt to 20 Volt Converter.** The 160 volt to 20 volt converter is a flyback type dc-dc converter similar to the converters used in the main power supply. The converter circuit includes transformer T1, transistors Q1 through Q5 and CR8. The converter steps down the unregulated +160 volt (nominal) output of the power converter in the main supply to an unregulated +20 volts dc used by the battery charger stage Q6 and by the 12 volt and 5 volt regulators during normal operation. The converter is automatically shut down if an overvoltage condition is detected on any of the memory supply voltage lines (±12 or 5 volts dc).

13.2.3.2 **12 Volt Converter.** The 12 volt converter is also of the flyback converter type. It operates from the unregulated +20 volts dc output of either the 160 volt to 20 volt converter (normal operation) or from the standby batteries (power fail condition). The circuit includes Q7 through Q9, T2 and U5. The 12 volt converter is also shut down for an over-voltage condition at the converter output.

13.2.3.3 **5 Volt Regulator.** The 5 volt regulator (U7) is a series regulator used to develop the reference voltage for the regulator control circuit and the 12 volt converter and to develop the regulated +5 volts dc memory voltage. The over-voltage associated with the 5 volt regulator shuts down the 160 volt and 20 volt converter and causes the battery fuse to open in the event that the output of the +5 volt regulator rises above a predetermined value.

13.2.3.4 **Battery Charger Circuit.** The battery charger circuit is an SN72723 voltage regulator that develops either a float voltage (batteries at full charge) or an equalizing voltage (batteries discharged).

13.2.3.5 **Regulator Control.** The regulator control circuit (U8) monitors the output of the 160 volt to 20 volt converter and generates a logic low UV– when the output of the converter drops below a predetermined value (usually during ac power fail condition). The regulator control circuit also disables the 12 volt converter and the 5 volt regulator if the battery switch is turned on before the ac switch is turned on. After the system is initialized, the regulators will function properly from battery power if ac power is lost.

13.3 AC POWER CONVERTER BOARD TROUBLESHOOTING PROCEDURES

Troubleshooting procedures for the ac power converter board are based on the use of the checkout chart in table 13-1 to locate circuit malfunctions and the fault isolation procedures in table 13-2 to trace malfunctions down to the replaceable part level.

13.3.1 **CONVERTER BOARD TEST SETUP.** The ac power converter board is checked using the 990 ac converter board test set and the combination scope/digital multimeter as shown in the cabling diagram in figure 13-6.

13.4 20 AMPERE MAIN POWER SUPPLY TROUBLESHOOTING PROCEDURES

Maintenance of the 20 ampere main power supply board is performed in conjunction with the 990 power supply test set and the combination scope/digital multimeter described in Section IV. The maintenance philosophy for this board includes a preliminary visual inspection to locate and replace components showing signs of overheating. The board is then resistance checked in accordance with the values provided in table 13-3 to locate and correct short circuit conditions on the board.

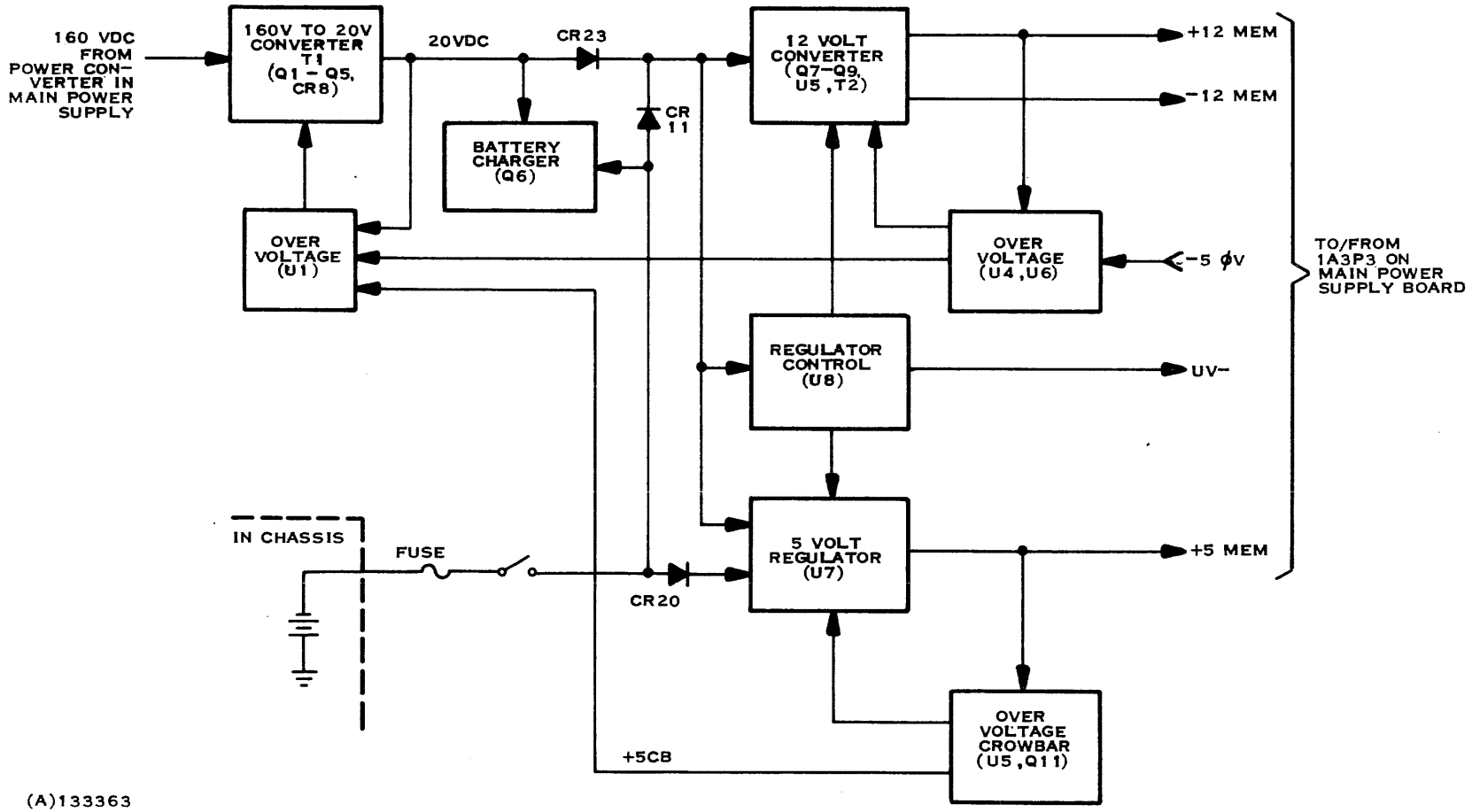


Figure 13-5. Standby Power Supply, Block Diagram

Table 13-1. Ac Power Converter Board, Checkout Procedure

(To Be Supplied)

Table 13-2. Ac Power Converter Board, Fault Isolation Procedures

(To Be Supplied)

(TO BE SUPPLIED)

Figure 13-6. Ac Converter Board Test Setup

Table 13-3. 20 Ampere Main Power Supply Resistance Checks

Meter Scale	Reference Designator	+Lead	-Lead	Reading
X100K	Q1	Case	Logic Common (LC)	Inifnity
X100K	Q2	Case	LC	Infinity
X100K	Q1	LC	Case	Infinity
X100K	Q2	LC	Case	Infinity
X1	C18	Neg. Side	LC	>3 ohms
X1	C19	Pos. Side	LC	>40 ohms
X1	C20	5 Main Etch Plane	LC	>5 ohms
X1	C18	LC	Neg. Side	>40 ohms
X1	C20	LC	+5 Main Etch Plane	>1 ohms
X10	Q2	160 RTN	TP1	>100 ohms
X100K	Q4	Case	160 RTN	>15K ohms
X100K	Q4	160 RTN	Case	Infinity
X100K	U4	160 RTN	Case	Infinity
X100K		160 RTN	LC	Infinity
X100K		LC	160 RTN	Infinity

At this point, the board is installed in the power supply test set in accordance with the instructions provided in paragraph 13.4.1. The board is then thoroughly tested using the checkout procedures supplied in table 13-4. In the event of a malfunction, additional fault isolation procedures are provided in table 13-5. Once a faulty component is located, the component is removed and replaced in accordance with the procedures provided in Section V.

13.4.1 **POWER SUPPLY TEST SETUP.** After completion of the resistance tests described in table 13-3, the 20 ampere main power supply board is installed in the power supply test set in accordance with the cabling information provided in figure 13-7.

WARNING

Dangerous voltages are present in the power supply circuitry. Undischarged filter capacitors in the power supply under test are also electrical shock hazards. Before handling the power supply (after each live test), discharge the capacitors by operating the toggle switch FILTER CAPACITOR in the lower right-hand corner of the test set to the DISCHARGE position or by manual means if the test set is not being used.

13.4.2 **20 AMPERE POWER SUPPLY CHECKOUT PROCEDURES.** After the board has been installed in the power supply test set in accordance with the information provided in figure 13-6, the power supply board is ready to undergo the checkout procedures provided in table 13-4. In the event that any step of the procedure results in a abnormal indication, refer to the fault isolation procedures in table 13-5 and the theory of operation presented at the beginning of this section to isolate the malfunction down to the replaceable part level.

Table 13-4. Main Power Supply Board Checkout Procedure

Step	Procedure	Normal Indication	If Abnormal
	INITIAL SETUP		
1	Set AC ON switch S26 to OFF or down position.	–	–
2	Mount main power supply board on lower portion of upper panel as shown in figure 13-7. Torque the holddowns at E14, E15 and E16. Holddown on E11 should be finger-tight.	–	–
3	Connect 1A3P1A (red), 1A3P1B (used with 40 amp supply only), 1A3P2 (nat) and 1A3P3 to respective connectors on the board under test. Connect the logic clip to U13.	–	–
4	Ensure that a solid 30 AWG wire is connected between the fuse posts (upper right-hand corner of upper panel).	–	–
5	Set the POWER switch on the oscilloscope and digital voltmeter to the ON position.	–	–
6	Set the control switches on the test set (figure 4-5) to the following initial positions:	–	–
	Switch / **Position**		
	Loads (all) / OFF		
	S1, S9, S15 and S22 / Normal		
	S3, S11, S17 and S24 / OFF		
	R1 / Minimum (10V)		
	S4 / OFF		
	S5, S6, S7, S8, S12 and S13 / Down		
	S14 / 20A		
	S18 and S20 / OFF		
	S26 / Down		
	S27 / +5V Main		
	S29, S30, S31, S32 and S33 / OFF		
	VARIAC / Zero (CCW)		
7	Connect the digital voltmeter to the monitor test jacks located just underneath the ac voltmeter on the control panel. Set up the DVM to read dc voltage on the AUTO RANGE.	–	–
8	Connect channel 1 10X scope probe to test point TP1 (next to Q2 heat sink) on board under test. Connect common lead to case of Q1 (160 VRTN).	–	–

Table 13-4. Main Power Supply Board Checkout Procedure (Continued)

Step	Procedure	Normal Indication	If Abnormal
9	Set the oscilloscope controls to the following settings: Function — Setting Vertical Mode — CH1 Vertical — 50 volts/div (using 10X probe) Horizontal — 10 μsec/div Input — DC Trigger Mode — Auto Trigger Coupling — AC Trigger Source — CH1 Trigger Slope — +	–	–
	INITIAL TURNON PROCEDURE		
10	Adjust R2 on power supply board fully CCW and R25 fully CW.	–	–
11	Set ac MAIN circuit breakers to ON position and set the AC ON switch S26 on the power supply test set to the up or AC ON position.	Fans activated.	–
12	Ensure that the VARIAC is set to the fully CCW position. Then set S20 to the ON position.	–	–
13	While observing the oscilloscope, turn the VARIAC clockwise until the ac voltmeter on the test set indicates 50 vac.	Approximately 3 flyback pulses with amplitude greater than 100 V_{p-p}, but less than 200 V_{p-p} should appear on scope.	Set S20 to OFF position and see table 13-5.
	REGULATOR ADJUSTMENT AND TEST		
14	Observe the voltage reading on the DVM.	5.6 ± .3 vdc	See table 13-5.
15	Adjust R25 (on the main power supply board) in the CCW direction to obtain an output voltage of +5.00, ±.01 vdc.	+5.00 vdc, ±.01 vdc	See table 13-5.
	NOTE If power supply shuts down (flyback pulses disappear and +5 main voltage reading on DVM drops to 0 volts), momentarily press S28 to the FILTER CAPACITOR DISCHARGE position (down).	Power supply should restart.	See table 13-5.
	OUTPUT VOLTAGE TEST		
16	Rotate monitor switch S27 through the following positions and observe the DVM reading at each position:		
	• +5 MAIN	+5.00 ± .01 vdc	See table 13-5.
	• +12 MAIN	+12.00 ± .12 vdc	See table 13-5.
	• -5 MEM	-5.00 ± .15 vdc	See table 13-5.
	• -12 MAIN	-12.00 ± .3 vdc	See table 13-5.
	PEAK CURRENT TEST		
17	Set monitor switch S27 to +5 MAIN position. Adjust VARIAC for reading of 110 vac.	Ac voltmeter indicates 110 vac. Flyback pulses on scope do not exceed .275 v_{p-p}. DVM reading remains at +5.00 ± .01 vdc.	See table 13-5.

Table 13-4. Main Power Supply Board Checkout Procedure (Continued)

Step	Procedure	Normal Indication	If Abnormal
18	Set up a 20 AMP load for the +5 MAIN output (total value of all +5 MAIN load switches set to UP position equals 20 AMPS). Set up a 2 AMP load for the +12 MAIN output. Ensure that the MONITOR switch S27 is still set to the +5 MAIN position.	Flyback pulse observed on scope do not exceed 400 V_{p-p}; DVM indicates less than 4.9 vdc.	See table 13-5.
	+160 VOLT THRESHOLD ADJUSTMENT		
19	Return all LOAD switches to the down position. Set the INT POWER switch S20 to the OFF position. Remove the scope probe from the power supply board and connect a BNC cable between the TLPRES– BNC connector on the test set and the channel 2 input to the scope.	–	–
20	Set up the oscilloscope as follows: **Function** / **Setting** Vertical Mode: CH2 Vertical: 1 VOLT/DIV Horizontal: 10 μSEC/DIV Input: DC Trigger Mode: AUTO Trigger Coupling: AC Trigger Source: CH2 Trigger Slope: +	–	–
21	Set INT POWER switch S20 to the ON position. Rotate the MONITOR switch S27 to the 160VDC position. Adjust the VARIAC for a reading of 118 vdc on the DVM.	DVM indicates +118 vdc; dc level on scope (TLPRES–) is +4.0 ± .5 vdc.	See table 13-5.
22	Adjust R2 clockwise until TLPRES– just switches low (as indicated on scope, channel 2). Set the VERTICAL SETTING of the scope to .1 VOLTS/DIV.	Dc level less than or equal to .4 vdc (ignoring spikes).	See table 13-5.
23	Return the VERTICAL setting to 1 VOLT/DIV. Adjust the VARIAC in the clockwise direction and observe channel 2 of the scope. When the monitored output (TLPRES–) switches high, observe the reading on the DVM.	DVM indicates +130 ± 2 vdc.	See table 13-5.
	LOAD AND RIPPLE TEST		
24	Adjust the VARIAC in a clockwise direction for a DVM reading of 170 vdc.	DVM indicates +170 ± 5 vdc.	–
25	Rotate the MONITOR switch S27 through the following positions and observe the voltage readings on the DVM:		
	• +5 MAIN	+5.0 ± .01 vdc	See table 13-5.
	• +12 MAIN	+12.00 ± .12 vdc	See table 13-5.
	• -5 MEM	-5.00 ± .15 vdc	See table 13-5.
	• -12 MAIN	-12.0 ± .3 vdc	See table 13-5.

Table 13-4. Main Power Supply Board Checkout Procedure (Continued)

Step	Procedure	Normal Indication	If Abnormal
26	Set MONITOR switch S27 to +5 MAIN position. Set up a load on each of the outputs (using the load switches in the upper left of the control panel) as follows: **Output** — **Load** +5 MAIN — 20A +12 MAIN — 2A -5 MEM — 100 mA -12 MAIN — 1A **NOTE** If the power supply board shuts down, momentarily press the FILTER CAPACITOR switch S28 to the DISCHARGE position.	–	–
27	Rotate MONITOR switch S27 to the following positions and observe the voltage readings on the DVM:		
	• +5 MAIN	+5.00 ± .05 vdc	See table 13-5.
	• +12 MAIN	+12.00 ± .24 vdc	See table 13-5.
	• -5 MEM	-5.00 ± .2 vdc	See table 13-5.
	• -12 MAIN	-12.00 ± .4 vdc	See table 13-5.
28	Temporarily disconnect the DVM leads from the MONITOR test jacks and connect the BNC lead from channel 2 of the oscilloscope to the MONITOR BNC.	–	–
29	Set up the scope controls as follows: **Function** — **Setting** Vertical Mode — CH2 Vertical — 50 mV/DIV Horizontal — 20 μS/DIV Input — AC Trigger Mode — NORM Trigger Coupling — HF REJ Trigger Source — CH2 Trigger Slope — +	–	–
30	Rotate MONITOR switch S27 to the following positions and observe the channel 2 scope display to ensure that each output is not oscillating and that the ripple is within tolerance:	–	–
	• +5 MAIN	50 mv_{p-p}	See table 13-5.
	• +12 MAIN	50 mv_{p-p}	See table 13-5.
	• -12 MAIN	50 mv_{p-p}	See table 13-5.
	• -5 MEM	50 mv_{p-p}	See table 13-5.
31	Reconnect the DVM leads to the MONITOR test jacks and reconnect the channel 2 scope lead to the TLPRES– BNC connector.	–	–

Table 13-4. Main Power Supply Board Checkout Procedure (Continued)

Step	Procedure	Normal Indication	If Abnormal
32	Change the oscilloscope controls as follows: Function / Setting Vert Mode: CH2 Vertical: 1V/DIV Horizontal: 10 μS/DIV Input (CH2): DC Trigger Mode: AUTO Trigger Coupling: AC Trigger Source: CH2 Trigger Slope: +	–	–
33	Set the MONITOR switch S27 to the 160 VDC position. Observe the TLPRES– output on channel 2 of the scope while rotating the VARIAC in a counter-clockwise direction. When TLPRES– switches low, rotate the MONITOR switch S27 to the following positions and observe the reading on the DVM:		
	• +5 MAIN	+5.00 ± .1 vdc	See table 13-5.
	• +12 MAIN	+12.00 ± .24 vdc	See table 13-5.
	• -5 MEM	-5.00 ± .2 vdc	See table 13-5.
	• -12 MAIN	-12.00 ± .4 vdc	See table 13-5.
	THERMAL PROTECTION TEST		
34	Using the DVM, monitor the voltage drop across RT1 which is attached to the Q2 heat-sink. **NOTE** Probing RT1 may result in a power supply shutdown. If this occurs, momentarily press S28 to restart the power supply.	≤2.7 vdc	See table 13-5.
35	Return the DVM leads to the MONITOR jacks. Adjust the VARIAC in a clockwise direction until a reading of +180 vdc is obtained.	+180 ± 5 vdc	–
	CURRENT LIMIT TEST		
36	Rotate the MONITOR switch S27 to the +5 MAIN position. Momentarily switch in an additional 10 AMP load on the +5 MAIN output.	Power supply immediately shuts down.	See table 13-5.
37	Remove the additional NO amp load from the +5 MAIN output and restart the power supply by momentarily setting S28 to the DISCHARGE position.	–	–
38	Set MONITOR switch S27 to the +12 MAIN position and apply an additional 1 AMP load on the +12 MAIN output. Observe the DVM reading.	≤11 vdc	See table 13-5.
39	Set MONITOR switch S27 to the -12 MAIN position and apply an additional 1 AMP load on the -12 MAIN output. Observe the DVM reading.	≤[-11 vdc]	See table 13-5.

Table 13-4. Main Power Supply Board Checkout Procedure (Continued)

Step	Procedure	Normal Indication	If Abnormal
	SHORT CIRCUIT TEST		
40	Set MONITOR switch S27 to +5 MAIN position. Momentarily set S30 to the ON or UP position and observe the DVM reading.	+5 MAIN shuts down, 30 AWG fuse wire does not burn open.	See table 13-5.
41	Return S30 to the DOWN position and restart the +5 MAIN supply by momentarily pressing S28 to the DISCHARGE position.	+5 MAIN supply restarts (see DVM).	See table 13-5.
42	Set MONITOR switch S27 to +12 MAIN position. Momentarily press S31 to the UP or ON position and observe the DVM reading.	Power supply shuts down.	See table 13-5.
43	Restart the power supply by momentarily pressing S28 to the DISCHARGE position and set MONITOR switch S27 to the -12 MAIN position.	-12 vdc.	See table 13-5.
44	Momentarily press S32 and then release switch.	DVM reading returns to -12.00 ± .4 vdc when S32 is released.	See table 13-5.
45	Rotate MONITOR switch S27 to -5 MEM position. Momentarily press S29 to the ON position and observe the DVM reading.	DVM reading indicates 0 volts; then returns to -5.00 ± .2 vdc when S29 is released.	See table 13-5.
46	Set all LOAD switches to OFF or down positions. Momentarily press S28 to DISCHARGE position.	–	–
	UNDERVOLTAGE TESTS		
47	Set MONITOR switch S27 to UV-(20A) position. Move the channel 2 scope lead to the MONITOR BNC connector. Observe channel 2 display on scope.	Dc level +4.5 ± 1 vdc.	See table 13-5.
48	Rotate +5 MAIN OVER/UNDER VOLTAGE switch S1 to the 5.3 UV-LL position. While observing channel 2 scope display, press and hold S2 until UV- goes low. Then release S2.	UV- goes low after a few seconds.	See table 13-5.
49	Rotate S1 to 5.1 UV-UL position and press S2.	UV- displayed on channel 2 remains high.	See table 13-5.
50	Return S1 to the +5 NORMAL position. Set the +12V MAIN switch S7 to the up or UL position. Release S7.	UV- stays high.	See table 13-5.
51	Momentarily press S8 to the LL (up) position and observe the scope. Then release S8.	UV- goes low.	See table 13-5.
52	Momentarily press S12 to the UL (up) position and observe the channel 2 display. Release S12.	UV- stays high.	See table 13-5.
53	Momentarily press S13 to the LL position and observe the scope display. Then release S13.	UV- goes low.	See table 13-5.
54	Momentarily press S25 to the UL position. Observe the channel 2 display. Then release S25.	UV- stays high.	See table 13-5.
55	Momentarily press S25 to the LL position and observe the scope display. Then release S25.	UV- goes low. When S25 is released UV- goes high.	See table 13-5.

Table 13-4. Main Power Supply Board Checkout Procedure (Continued)

Step	Procedure	Normal Indication	If Abnormal
	OVERVOLTAGE TEST		
56	Rotate +5V MAIN OVERVOLTAGE switch S1 to +4.4 OV-LL position. Rotate MONITOR switch S27 to the +5 MAIN position. Momentarily press S2 and observe DVM reading.	+5.6 ± .1 vdc while S2 is pressed.	See table 13-5.
57	Rotate S1 to the +4 OV-UL position and momentarily press S2.	DVM reading increases to 5.8 ± .4 vdc and then drops to 0 volts.	See table 13-5.
58	Return S1 to the +5 NORMAL position. Momentarily press S28 to the DISCHARGE position to restart the power supply.	–	See table 13-5.
59	Rotate the MONITOR switch S27 to the +12 MAIN position. Rotate S9 to the 13.4 OV-LL position. Press S10 and note the DVM reading; then release S10.	+13.4 ± .2 vdc.	See table 13-5.
60	Rotate S9 to the +14 OV-UL position, press S10 and note the DVM reading.	+1.7 ± .5 vdc.	See table 13-5.
61	Release S10 and momentarily press S28 to the DISCHARGE position. Return S9 to the +12 NORMAL position.	–	See table 13-5.
62	Rotate MONITOR switch S27 to -12 MAIN position. Rotate S15 to the -13.4 OV-LL position. Press S16 and note DVM reading. Then, release S16.	-13.5 ± .2 vdc.	See table 13-5.
63	Rotate S15 to -14 OV-UL position and press S16. Release S16 and momentarily press S28 to DISCHARGE position. Return S15 to -12 NORMAL position.	-2.5 ± .5 vdc.	See table 13.5
64	Rotate MONITOR switch S27 to -50V position. Observe the DVM reading. Press S19 to the ON (up) position.	5 ± 1 vdc; reading does not change when S19 is pressed.	See table 13-5.
65	Set MONITOR switch S27 to +5 MAIN position and momentarily press S21 and observe DVM reading.	DVM reading goes to zero.	See table 13-5.
66	Set MONITOR switch S27 to -5 MEM position. Press S21 to the ON (up) position and observe the DVM.	-6.0 ± .4 vdc when S21 is ON; -5.0 ± .4 vdc when S21 is OFF.	See table 13-5.
67	Set MONITOR switch S27 to -50V position and observe DVM.	+5 ± 1 vdc.	See table 13-5.
68	Press S21 and observe DVM reading. Release S21 and momentarily press S28 to DISCHARGE position.	0 ± .5 vdc.	See table 13-5.
69	Set S27 to +5 MAIN position and press S21.	–	–
	TIMING TEST		
70	Rotate MONITOR switch S27 to TLPFWP– position. Connect channel 1 scope lead to the MONITOR BNC connector.	–	–

Table 13-4. Main Power Supply Board Checkout Procedure (Continued)

Step	Procedure	Normal Indication	If Abnormal
71	Change the oscilloscope controls as follows: Function / Setting Vertical Mode: CHOP Vertical (CH1 & CH2): 2 V/DIV Horizontal: 2 MS/DIV Trigger Mode: NORMAL Trigger Coupling: AC Trigger Source: CH1 Trigger Slope: – Then observe the channel 1 display. NOTE Set the scope to trigger on the negative transition of the TLPFWP– pulse by rotating the VARIAC in a CCW direction and then in a CW direction several times.	TLPFWP– switches low for ≅ 8.5 ms and switches high as the 160 vdc input decreases below ≅ 118 vdc. The high level of the pulse should be 3.5 ± 1 vdc and the low level should be 0.2 ± .2 vdc. The low time should be 8.5 ± 1.5 milliseconds.	See table 13-5.
72	Adjust the VARIAC in a clockwise direction for a reading of 130 vac on the built-in ac voltmeter.	130 vac on ac voltmeter.	–
73	Set up the following loads: Output / Load +5 MAIN: 20 AMPS +12 MAIN: 2 AMPS -5 MEM: 100 MA -12 MAIN: 1 AMP Observe the timing between TLPFWP– and TLPRES– on the scope as the VARIAC output voltage ranges between 90 and 110 vac.	Leading edge of TLPFWP– goes high a minimum of 1 μsec before TLPRES– goes high and goes low 7.0 msec before TLPRES– goes low.	See table 13-5.
74	Set all load switches to the OFF or down position.	–	–
	120 HZ CLOCK TEST		
75	Rotate MONITOR switch S27 to 120 HZ position. Adjust VARIAC for a reading of 50 ± 5 vac. Change the following scope settings: Function / New Setting Vert Mode: CH1 Vert Range (CH1): 1V/DIV Trigger Mode: AUTO	50 ± 5 vac reading on ac voltmeter on panel.	–
76	Observe waveform on scope.	High level of 3.5 ± 1 vdc and low level of 0.2 ± .2 vdc, high level time is 4 ± 1 msec and period for 1 cycle is 8.3 ± 3 msec.	See table 13-5.
77	Set INT POWER switch S20 to OFF or down position.	0 vac reading on ac voltmeter.	–
78	Disconnect all cables from the power supply board and remove the board from the test set. This step concludes the main converter board checkout procedure.	–	–

Table 13-5. 20 Ampere Power Supply Fault Isolation Procedure

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
			ONE OR MORE OUTPUTS OF MAIN POWER SUPPLY ABNORMAL		
1	Missing or defective 120 Hz.	Defective U8 or U16.	Check waveforms at input and output of indicated sections of U8 and U16.	Clean 120 Hz signal switching between logic levels.	Replace indicated defective U8 or U16.
2	All outputs absent.	Automatic shutdown due to overvoltage or overcurrent (+5 MAIN) in output.	Disable crowbar temporarily shorting resistor R62.	Does not produce an output voltage.	Check Q10, U13, U7B and VR2. Replace defective part.
		Automatic shutdown due to average current excessive.	Disable U2D by temporarily shorting pins 10-12.	Does not produce an output voltage.	Check Q2, T1 and associated parts. Replace defective part.
		Automatic shutdown due to overheating of Q2.	Spray coolant on Q2.	Does not momentarily produce an output.	Check Q2, T1 and associated parts. Replace defective part.
		Failure of oscillator to start.	Check saveform at TP1.	160V squarewave.	Check bias on Q2 (approximately 2.5V). Check R85, R16, CR1, CR2, C8 and Q2. Replace defective part.
3	+5 MAIN voltage abnormal.	Defective rectifier or filter.	Check secondary number 3 voltage and dc output of rectifier filter.	Approximately 6V peak ac, 5 vdc.	Check T1, CR13, C20, C21 and R27. Replace defective part.
		Defect in oscillator control loop.	Check +5V REF at pin 1 of U7A.	+5V.	Check U10, R25, C25, C22 and U7A. Replace defective part.
			Check for charging waveform across C15.	Charge waveform approximately 20V peak.	Check U5, U7B, C15, R22 and CR1. Replace defective part.
4	+12 MAIN voltage abnormal.	Defective rectifier or filter.	Check secondary number 1 voltage and dc output of rectifier filter.	Approximately 20V peak, +16 vdc.	Replace defective transformer T1, rectifier CR12 or filter capacitor C19.
		Defective regulator or output circuit.	Check +12 MAIN output voltage across C34.	+12V.	Check Q3, U10, Q4, C34 and associated parts. Replace defective part.
5	-12 MAIN voltage abnormal.	Defective rectifier or filter.	Check secondary number 2 voltage and dc output of rectifier filter.	Approximately 20V peak, -16 vdc.	Replace defective transformer T1, rectifier CR11, or C18.
		Defective regulator or output circuit.	Check -12 MAIN output voltage across C27.	-12V.	Check R26, U6 and C27. Replace defective part.
6	-5 MEM voltage abnormal.	Defective -12 MEM input from Standby power supply.	Check -12 MEM voltage at cathode of CR23.	-12V.	Check -12 MEM output of Standby PS per below.
		Defective regulator or output circuit.	Check -5 MEM output voltage across C43.	-5V.	Check U15 and C43. Replace defective part.

Table 13-5. 20 Ampere Power Supply Fault Isolation Procedure (Continued)

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
			ONE OR MORE OUTPUTS OF MAIN POWER SUPPLY ABNORMAL (Continued)		
7	Missing or defective TLPRES–.	Defective sensor U1 or optical coupler U4.	Check voltage at pin 5 of U4 with input adjusted lower than 122V.	+5V.	Check U1 and U4. Replace defective part.
		Defective output circuit.	Check for high output at pin 5 of U9.	+5V.	Replace U9.
8	Missing or defective TLPFWP–.	Failure of UV– signal from Standby PS.	Check for logic low at pin 13 of U11.	0V	Check UV– source in Standby PS.
		Failure of output circuit.	Check for setting of U11 (pin 8), clock input from pin 4 of U9.	Zero volts, short SS pulse output.	Replace defective U9 or U11.
			ONE OR MORE OUTPUTS OF STANDBY POWER SUPPLY ABNORMAL		
9	Missing or defective UV–.	U8.	Check inputs to U8B and U8C. Check output.	+5 REF, +12 MEM, +5 MEM; output high for good inputs.	Replace U8 if indicated defective; otherwise troubleshoot output voltages as indicated below.
10	All putputs absent.	Automatic shutdown due to overvoltage.	Disable overvoltage shutdown by shorting terminals 1 and 2 of optical isolator U1.	Output voltages appear normal (after recycling input).	Check CR9, U1, U5, U8. Replace defective part.
		Rectifier filter defect.	Check peak ac output of 7-8 of T1.	Approximately 24V.	Replace T1 if it indicates defective.
			Check rectifier filter output.	Approximately 22V.	Check CR8, C10. Replace defective part.
		Oscillator failure.	Check for squarewave at collector of Q5.	Approximately 160V.	Check Q5, CR7, C8, and related parts. Replace defective part.
11	+5V MEM abnormal.	Defective regulator Q10.	Check regulator output scross C15.	+5V.	Check Q10, C15 and associated parts. Replace defective part.
12	+12V MEM and -12V MEM both absent.	Automatic shutdown of 12V converter.	Check voltage at base of Q7.	Approximately 0V.	Check circuits of U5A, U6A, U6D. Replace faulty part.
		Failure of oscillator in 12V converter.	Check voltage waveform at collector of Q9.	20V squarewave.	Check Q9 and associated circuit. Replace defective part.
13	+12V MEM absent.	Fault in rectifier or filter.	Check secondary voltage and dc output of filter.	Approximately 14V peak; +12 vdc.	Replace component indicated as defective.
14	-12V MEM absent.	Fault in rectifier or filter.	Check secondary voltage and dc output of filter.	Approximately 14V peak; -12 vdc.	Replace component indicated as defective.
			MALFUNCTION OF OVERVOLTAGE SHUTDOWNS		
15	Overvoltage test does not shut down the power supply.	U13.	Check for appropriate input to U13, and corresponding output.	Overvoltage per individual input, low output.	Replace U13.

Table 13-5. 20 Ampere Power Supply Fault Isolation Procedure (Continued)

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
			FAILURES OF SHORT CIRCUIT TESTS		
16	Shorting of +5 MAIN does not shutdown power supply.	U13C.	Check that input voltage of pin 8 of U13C tracks overcurrent. Check for low output of U13C.	Voltage increases with overcurrent. Low output.	Check C36, C37. Check output voltage. Replace defective part.
17	Shorting +12 MAIN does not shut down power supply.	Q10. U3 and input shutdown circuit.	Check Q10 and associated components. Check U3.	Normal bias voltages produce expected outputs.	Replace component indicated as defective.
18	Shorting -12 MAIN shuts down PS.	U6, CR11.	Check that input voltage at pin 3 of U6 does not drop when short is applied.	Approximately -15 vdc.	Check rectifier, filter and regulator. Replace defective part.
19	Shorting -5 MEM shuts down PS.	CR23, U15.	Check voltage drop across diode and voltage regulator.	Normal diode drop, normal regulator drop (7V operating, 10V shorted).	Replace part indicated as defective.

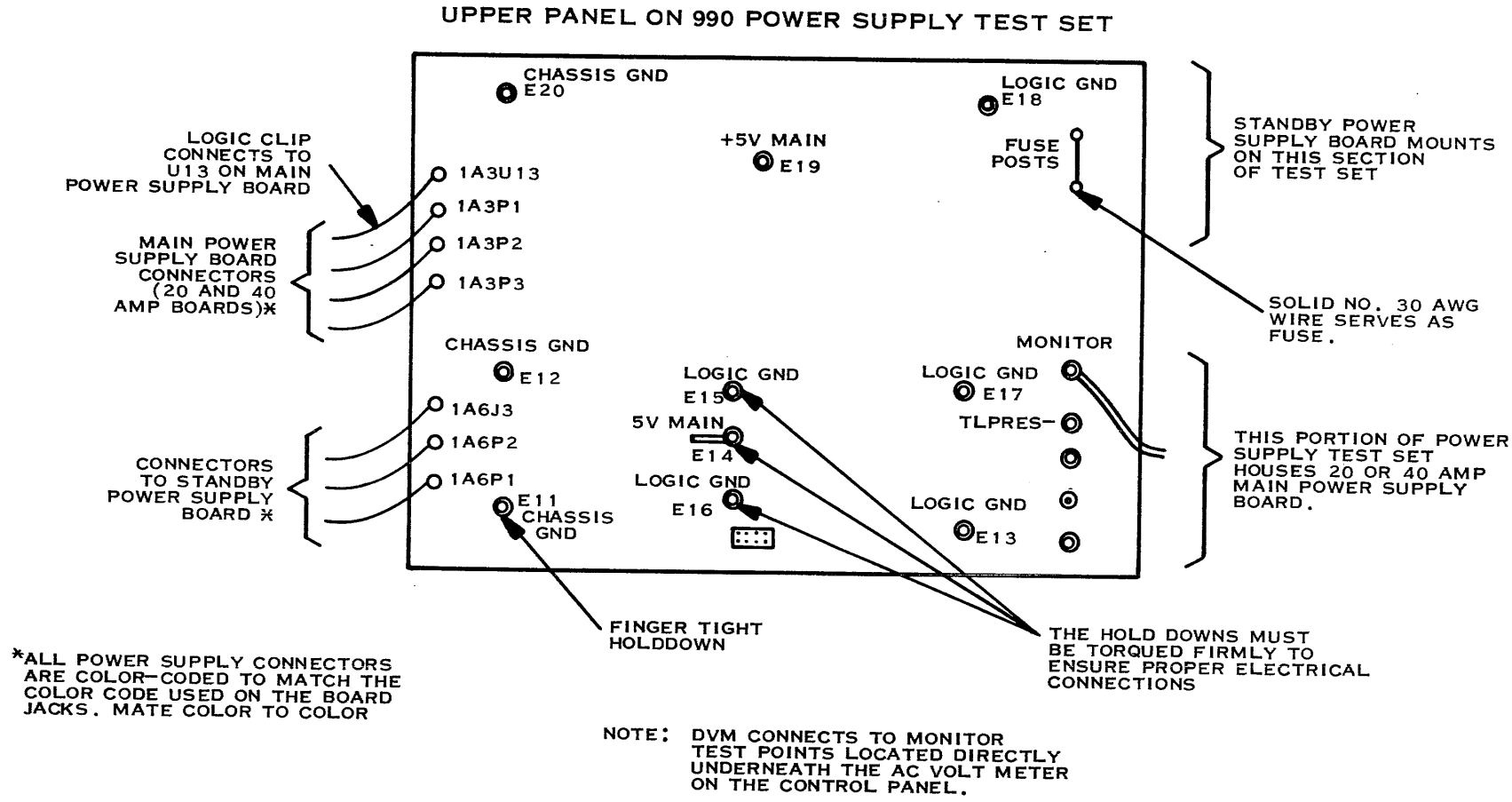


Figure 13-7. 20 Ampere Main Power Supply Board, Test Setup

13.4.3 **MAIN POWER SUPPLY FAULT ISOLATION PROCEDURES.** The fault isolation procedures for the 20 ampere main power supply is provided in table 13-5. In addition to the fault isolation data provided in this table, some general troubleshooting data is provided in the following paragraphs.

13.4.3.1 **General Troubleshooting Data.** Because of the interaction of the shutdown controls on the power supply, troubleshooting of front-end shutdown symptoms may be expedited by disabling the crowbar circuit (connecting a jumper between the junction of R75 and R76 to ground) and disabling the optical coupler by shorting R62 to ground.

In addition, the use of coolants and/or heating units may be used to isolate intermittant failures.

CAUTION

Do not spray coolant directly on RT1 (mounted on one fin of the heatsink for switching transistor stage Q2) as this may result in destructive overheating of Q2.

Once the front end shutdown circuits have been removed, the various output conditions which may result in shutdown should be examined (see figure 13-4).

13.5 STANDBY POWER SUPPLY TROUBLESHOOTING PROCEDURES

Troubleshooting procedures for the standby power supply board are based on the use of the checkout procedures in table 13-6 to locate circuit malfunctions and the use of the fault isolation procedures in table 13-7 to isolate circuit malfunctions down to the replaceable component level.

13.5.1 **STANDBY POWER SUPPLY TEST SETUP.** Depot maintenance on the standby power supply board is accomplished by using the 990 power supply test set as shown in the cabling diagram in figure 13-6.

Table 13-6. Standby Power Supply Board, Checkout Procedure

(To Be Supplied)

Table 13-7. Standby Power Supply Board Fault Isolation Procedures

(To Be Supplied)

APPENDIX A

PROGRAMMING REFERENCE DATA

990/4 INSTRUCTION SET (ALPHABETICAL ORDER)

Mnemonic Operation Code	Hexadecimal Operation Code	Name	Format
A	A000	Add Words	I
AB	B000	Add Bytes	I
ABS	0740	Absolute Value	VI
AI	0220	Add Immediate	VIII
ANDI	0240	AND Immediate	VIII
B	0440	Branch	VI
BL	0680	Branch and Link	VI
BLWP	0400	Branch and Load Workspace Pointer	VI
C	8000	Compare Words	I
CB	9000	Compare Bytes	I
CI	0280	Compare Immediate	VIII
CKOF	03C0	Clock Off	VII
CKON	03A0	Clock On	VII
CLR	04C0	Clear Operand	VI
COC	2000	Compare Ones Corresponding	III
CZC	2400	Compare Zeros Corresponding	III
DEC	0600	Decrement By One	VI
DECT	0640	Decrement By Two	VI
DIV	3C00	Divide	IX
IDLE	0340	Computer Idle	VII
INC	0580	Increment By One	VI
INCT	05C0	Increment By Two	VI
INV	0540	Invert	VI
JEQ	1300	Jump Equal	II
JGT	1500	Jump Greater Than	II
JH	1B00	Jump High	II
JHE	1400	Jump High Or Equal	II
JL	1A00	Jump Low	II
JLE	1200	Jump Low Or Equal	II
JLT	1100	Jump Less Than	II
JMP	1000	Jump Unconditional	II

990/4 INSTRUCTION SET (ALPHABETICAL ORDER) (Continued)

Mnemonic Operation Code	Hexadecimal Operation Code	Name	Format
JNC	1700	Jump No Carry	II
JNE	1600	Jump Not Equal	II
JNO	1900	Jump No Overflow	II
JOC	1800	Jump On Carry	II
JOP	1C00	Jump Odd Parity	II
LDCR	3000	Load Communication Register	IV
LI	0200	Load Immediate	VIII
LIMI	0300	Load Interrupt Mask Immediate	VIII
LREX	03E0	Load or Restart Execution	VII
LWPI	02E0	Load Workspace Pointer Immediate	VIII
MOV	C000	Move Word	I
MOVB	D000	Move Byte	I
MPY	3800	Multiply	IX
NEG	0500	Negate	VI
ORI	0260	OR Immediate	VIII
RSET	0360	Computer Reset	VII
RTWP	0380	Return From Interrupt Subroutine	VII
S	6000	Subtract Word	I
SB	7000	Subtract Byte	I
SBO	1D00	Set Bit To One	II
SBZ	1E00	Set Bit To Zero	II
SETO	0700	Set Ones	VI
SLA	0A00	Shift Left Arithmetic	V
SOC	E000	Set Ones Corresponding, Word	I
SOCB	F000	Set Ones Corresponding, Byte	I

990/4 INSTRUCTION SET (ALPHABETICAL ORDER) (Continued)

Mnemonic Operation Code	Hexadecimal Operation Code	Name	Format
SRA	0800	Shift Right Arithmetic	V
SRC	0B00	Shift Right Circular	V
SRL	0900	Shift Right Logical	V
STCR	3400	Store Communication Register	IV
STST	02C0	Store Status	VIII
STWP	02A0	Store Workspace Pointer	VIII
SWPB	06C0	Swap Bytes	VI
SZC	4000	Set Zeros Corresponding, Word	I
SZCB	5000	Set Zeros Corresponding, Byte	I
TB	1F00	Test Bit	II
X	0480	Execute	VI
XOP	2C00	Extended Operation	IX
XOR	2800	Exclusive OR	III

990/4 INSTRUCTION SET (HEXADECIMAL OP CODE ORDER)

Hexadecimal Operation Code	Mnemonic Operation Code	Name	Format
0200	LI	Load Immediate	VIII
0220	AI	Add Immediate	VIII
0240	ANDI	AND Immediate	VIII
0260	ORI	OR Immediate	VIII
0280	CI	Compare Immediate	VIII
02A0	STWP	Store Workspace Pointer	VIII
02C0	STST	Store Status	VIII
02E0	LWPI	Load Workspace Pointer Immediate	VIII
0300	LIMI	Load Interrupt Mask Immediate	VIII
0340	IDLE	Computer Idle	VII
0360	RSET	Computer Reset	VII
0380	RTWP	Return From Interrupt Subroutine	VII
03A0	CKON	Clock On	VII
03C0	CKOF	Clock Off	VII
03E0	LREX	Load ROM and Execute	VII
0400	BLWP	Branch And Load Workspace Pointer	VI
0440	B	Branch	VI
0480	X	Execute	VI
04C0	CLR	Clear Operand	VI
0500	NEG	Negate	VI
0540	INV	Invert	VI
0580	INC	Increment By One	VI
05C0	INCT	Increment By Two	VI
0600	DEC	Decrement By One	VI
0640	DECT	Decrement By Two	VI
0680	BL	Branch and Link	VI
06C0	SWPB	Swap Bytes	VI
0700	SETO	Set Ones	VI

990/4 INSTRUCTION SET
(HEXADECIMAL OP CODE ORDER) (Continued)

Hexadecimal Operation Code	Mnemonic Operation Code	Name	Format
0740	ABS	Absolute Value	VI
0800	SRA	Shift Right Arithmetic	V
0900	SRL	Shift Right Logical	V
0A00	SLA	Shift Left Arithmetic	V
0B00	SRC	Shift Right Circular	V
1000	JMP	Jump Unconditional	II
1100	JLT	Jump Less Than	II
1200	JLE	Jump Low Or Equal	II
1300	JEQ	Jump Equal	II
1400	JHE	Jump High Or Equal	II
1500	JGT	Jump Greater Than	II
1600	JNE	Jump Not Equal	II
1700	JNC	Jump No Carry	II
1800	JOC	Jump On Carry	II
1900	JNO	Jump No Overflow	II
1A00	JL	Jump Low	II
1B00	JH	Jump High	II
1C00	JOP	Jump Odd Parity	II
1D00	SBO	Set Bit To One	II
1E00	SBZ	Set Bit To Zero	II
1F00	TB	Test Bit	II
2000	COC	Compare Ones Corresponding	III
2400	CZC	Compare Zeros Corresponding	III
2800	XOR	Exclusive OR	III
2C00	XOP	Extended Operation	IX
3000	LDCR	Load Communication Register	IV
3400	STCR	Store Communication Register	IV
3800	MPY	Multiply	IX
3C00	DIV	Divide	IX

990/4 INSTRUCTION SET (HEXADECIMAL OP CODE ORDER) (Continued)

Hexadecimal Operation Code	Mnemonic Operation Code	Name	Format
4000	SZC	Set Zeros Corresponding, Word	I
5000	SZCB	Set Zeros Corresponding, Byte	I
6000	S	Subtract Word	I
7000	SB	Subtract Byte	I
8000	C	Compare Words	I
9000	CB	Compare Bytes	I
A000	A	Add Words	I
B000	AB	Add Bytes	I
C000	MOV	Move Word	I
D000	MOVB	Move Byte	I
E000	SOC	Set Ones Corresponding, Word	I
F000	SOCB	Set Ones Corresponding, Byte	I

APPENDIX B

BACKPANEL CONNECTOR LISTING

MODSEL CONNECTIONS

SIGNAL NAME	SOURCE SLOT,CONNECTOR,PIN	LOAD SLOT, CONNECTOR, PIN (SLOT = 7"/12" CHASSIS)
MODSEL0-	1,P1,PIN 23	6/13,P2,PIN 48
MODSEL1-	1,P1,PIN 35	6/13,P1,PIN 48 and 6/13,P2,PIN 46
MODSEL2-	1,P1,PIN 37	5/12,P2,PIN 48
MODSEL3-	1,P1,PIN 43	5/12,P1,PIN 48 and 5/12,P2,PIN 46
MODSEL4-	1,P1,PIN 44	4/11,P2,PIN 48
MODSEL5-	1,P1,PIN 45	4/11,P1,PIN 48 and 4/11,P2,PIN 46
MODSEL6-	1,P1,PIN 46	3/10,P2,PIN 48
MODSEL7-	1,P1,PIN 47	3/10,P1,PIN 48 and 3/10,P2,PIN 46
MODSEL8-	1,P1,PIN 48	2/9,P2,PIN 48
MODSEL9-	1,P1,PIN 49	2/9,P1,PIN 48 and 2/9,P2,PIN 46
MODSEL10-	1,P1,PIN 51	8,P2,PIN 48
MODSEL11-	1,P1,PIN 53	8,P1,PIN 48 and 8,P2,PIN 46
MODSEL12-	1,P1,PIN 61	7,P2,PIN 48
MODSEL13-	1,P1,PIN 67	7,P1,PIN 48 7,P2,PIN 46
MODSEL14-	1,P1,PIN 69	6,P2,PIN 48
MODSEL15-	1,P1,PIN 76	6,P1,PIN 48 and 6,P2,PIN 46
MODSEL16-	1,P2,PIN 38	5,P2,PIN 48
MODSEL17-	1,P2,PIN 36	5,P1,PIN 48 and 5,P2,PIN 46
MODSEL18-	1,P2,PIN 34	4,P2,PIN 48
MODSEL19-	1,P2,PIN 32	4,P1,PIN 48 and 4,P2,PIN 46
MODSEL20-	1,P2,PIN 22	3,P2,PIN 48
MODSEL21-	1,P2,PIN 18	3,P1,PIN 48 and 3,P2,PIN 46
MODSEL22-	1,P2,PIN 16	2,P2,PIN 48
MODSEL23-	1,P2,PIN 13	2,P1,PIN 48 and 2,P2,PIN 46

TEXAS INSTRUMENTS INCORPORATED
DIGITAL SYSTEMS DIVISION
HOUSTON, TEXAS

A | 945014 | SHEET | REV

TI-4259-E

CHASSIS BACKPLANE PINOUTS

990 FAMILY

PIN P1-	FUNCTION BACKPLANE	990-4	990-10	TILINE/CRU	TERMINATION	P1 BUSSED TO P2	COMMENTS
1,2	GND	GND	GND	GND		GND PLANE	ROUTED TO P.S.CONN
3,4	+5 MAIN	+5 MAIN	+5 MAIN	+5 MAIN		X	ROUTED TO P.S. CONN.
5,6	+12 MEM	+12 MEM	+12 MEM	+12 MEM		X	ROUTED TO P.S. CONN.
7,8	+5 MEM	+5 MEM	+5 MEM	+5 MEM		X	ROUTED TO P.S. CONN.
9,10	-5 MEM	-5 MEM	-5 MEM	-5 MEM		X	ROUTED TO P.S. CONN.
11	BUS	DBIN	TLREAD	TLREAD	DP		
12	GND	GND	GND	GND		GND PLANE	ROUTED TO P.S. CONN.
13	BUS	TLPRES-	TLPRES-	TLPRES-		X	SUPPLIED FROM P.S.
							ROUTED TO P.S. CONN.
14	BUS	TLIORES-	TLIORES-	TLIORES-	PU	X	
15	GND	GND	GND	GND		GND PLANE	
16	BUS	TLPFWP-	TLPFWP-	TLPFWP-		X	SUPPLIED FORM P.S.
							ROUTED TO P.S. CONN.
17	GND	GND	GND	GND		GND PLANE	ROUTED TO P.S. CONN.
18	BUS	CRUBITOUT	CRUBITOUT	CRUBITOUT		X	
19	GND	GND	GND	GND		GND PLANE	ROUTED TO P.S. CONN.
20	BUS	READY	TLTM-	TLTM-	DP		
21	GND	GND	GND	GND		GND PLANE	ROUTED TO P.S. CONN.
22	BUS	STORECLK-	STORECLK-	STORECLK-		X	
23	OPEN	MODSELO-	MODSELO-	SPARE			
24	GND	GND	GND	GND		GND PLANE	ROUTED TO P.S. CONN.
25	BUS	MEMEN-	TLGO-	TLGO-	DP		
26	GND	GND	GND	GND		GND PLANE	ROUTED TO P.S. CONN.
27	BUS	DAT12-	TLDAT12-	TLDAT12-			
28	BUS	DAT13-	TLDAT13-	TLDAT13-			

DP = DOUBLE PARALLEL TERMINATION - USE 75138 RECEIVER

TEXAS INSTRUMENTS INCORPORATED DIGITAL SYSTEMS DIVISION HOUSTON, TEXAS

A | SHEET 945014 | REV

TI-4859-E

CHASSIS BACKPLANE PINOUTS
990 FAMILY

PIN P1-	FUNCTION BACKPLANE	990-4	990-10	TILINE/CRU	TERMINATION	P1 BUSSED TO P2	COMMENTS
29	BUS	120 HZ	120 HZ	120 HZ			SUPPLIED FROM P.S. TO PROCESSOR
30	BUS	DAT14-	TLDAT14-	TLDAT14-			
31	BUS	DAT15-	TLDAT15-	TLDAT15-			
32	BUS	CRUBIT13	CRUBIT13	CRUBIT13		X	
33	OPEN	IAQ-	IAQ-	SPARE			
34	BUS	CRUBIT15	CRUBIT15	CRUBIT15		X	
35	OPEN	MODSEL1-	MODSEL1-	SPARE			
36	BUS	CRUBIT12	CRUBIT12	CRUBIT12		X	
37	OPEN	MODSEL2-	MODSEL2-	SPARE			
38	BUS	CRUBIT14	CRUBIT14	CRUBIT14		X	
39,40	+12 MAIN	+12 MAIN	+12 MAIN	+12 MAIN		X	ROUTED TO P.S. CONN.
41,42	-12 MAIN	-12 MAIN	-12 MAIN	-12 MAIN			
43	OPEN	MODSEL3-	MODSEL3-	SPARE		x	ROUTED TO P.S. CONN.
44	OPEN	MODSEL4-	MODSEL4-	SPARE			
45	OPEN	MODSEL5-	MODSEL5-	SPARE			
46	OPEN	MODSEL6-	MODSEL6-	SPARE			
47	OPEN	MODSEL7-	MODSEL7-	SPARE			
48	OPEN	MODSEL8-	MODSEL8-	MODSELB-			
49	OPEN	MODSEL9-	MODSEL9-	SPARE			
50	BUS	CRUBIT7	CRUBIT7	CRUBIT7			
51	OPEN	MODSEL10-	MODSEL10-	SPARE			
52	BUS	CRUBIT6	CRUBIT6	CRUBIT6			
53	OPEN	MODSEL11-	MODSEL11-	SPARE			
54	BUS	CRUBIT5	CRUTIT5	CRUBIT5			
55	BUS	TLMER-	TLMER-	TLMER-	PU		

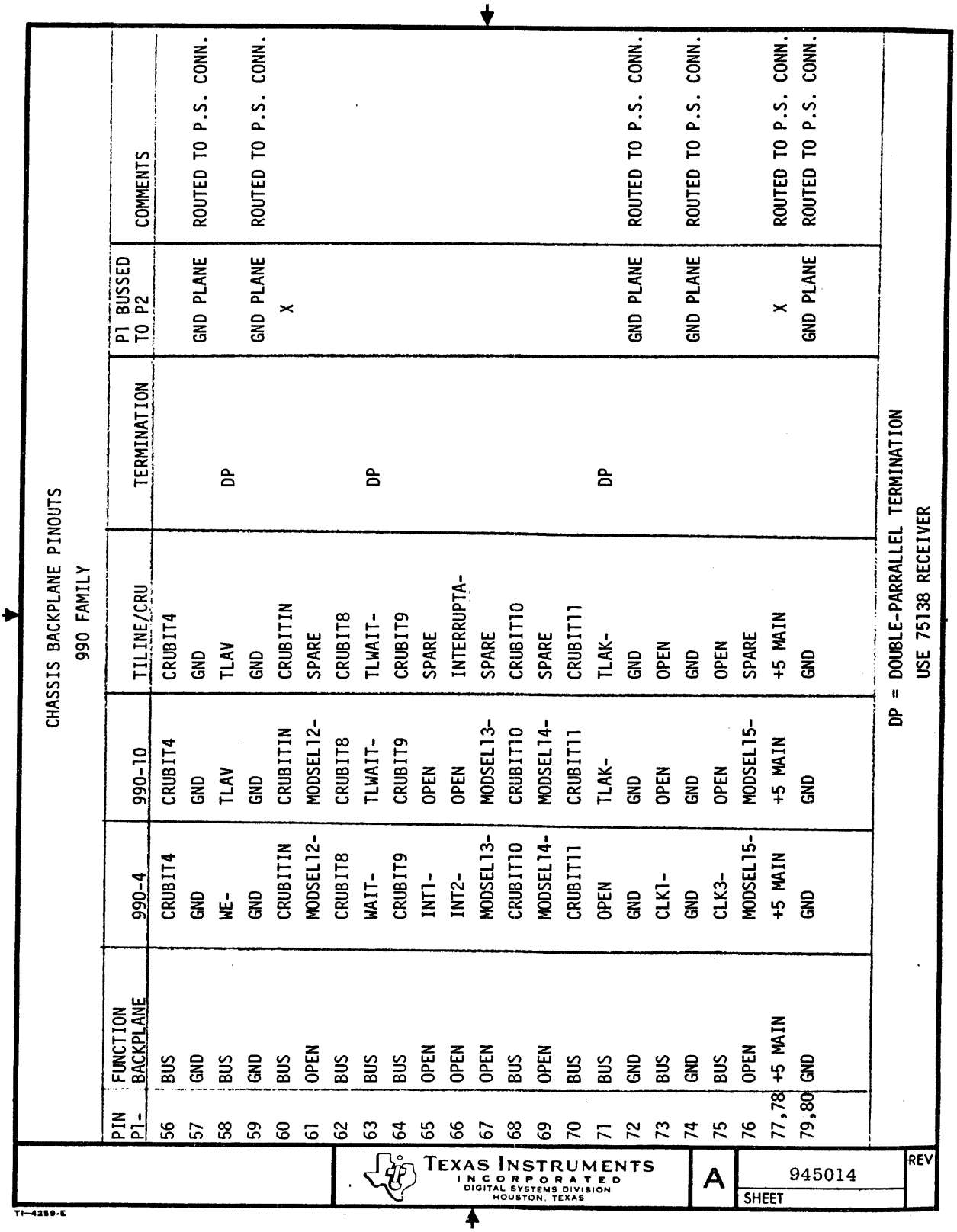
PU = PULL-UP RESISTOR TO +5 MAIN

TEXAS INSTRUMENTS INCORPORATED
DIGITAL SYSTEMS DIVISION
HOUSTON, TEXAS

A

SHEET 945014

REV



CHASSIS BACKPLANE PINOUTS
990 FAMILY

PIN P1-	FUNCTION BACKPLANE	990-4	990-10	TILINE/CRU	TERMINATION	P1 BUSSED TO P2	COMMENTS
56	BUS	CRUBIT4	CRUBIT4	CRUBIT4			
57	GND	GND	GND	GND		GND PLANE	ROUTED TO P.S. CONN.
58	BUS	WE-	TLAV	TLAV	DP		
59	GND	GND	GND	GND		GND PLANE	ROUTED TO P.S. CONN.
60	BUS	CRUBITIN	CRUBITIN	CRUBITIN		X	
61	OPEN	MODSEL12-	MODSEL12-	SPARE			
62	BUS	CRUBIT8	CRUBIT8	CRUBIT8			
63	BUS	WAIT-	TLWAIT-	TLWAIT-	DP		
64	BUS	CRUBIT9	CRUBIT9	CRUBIT9			
65	OPEN	INT1-	OPEN	SPARE			
66	OPEN	INT2-	OPEN	INTERRUPTA-			
67	OPEN	MODSEL13-	MODSEL13-	SPARE			
68	BUS	CRUBIT10	CRUBIT10	CRUBIT10			
69	OPEN	MODSEL14-	MODSEL14-	SPARE			
70	BUS	CRUBIT11	CRUBIT11	CRUBIT11			
71	BUS	OPEN	TLAK-	TLAK-	DP		
72	GND	GND	GND	GND		GND PLANE	ROUTED TO P.S. CONN.
73	BUS	CLK1-	OPEN	OPEN			
74	GND	GND	GND	GND		GND PLANE	ROUTED TO P.S. CONN.
75	BUS	CLK3-	OPEN	OPEN			
76	OPEN	MODSEL15-	MODSEL15-	SPARE		X	ROUTED TO P.S. CONN.
77,78	+5 MAIN	+5 MAIN	+5 MAIN	+5 MAIN			
79,80	GND	GND	GND	GND		GND PLANE	ROUTED TO P.S. CONN.

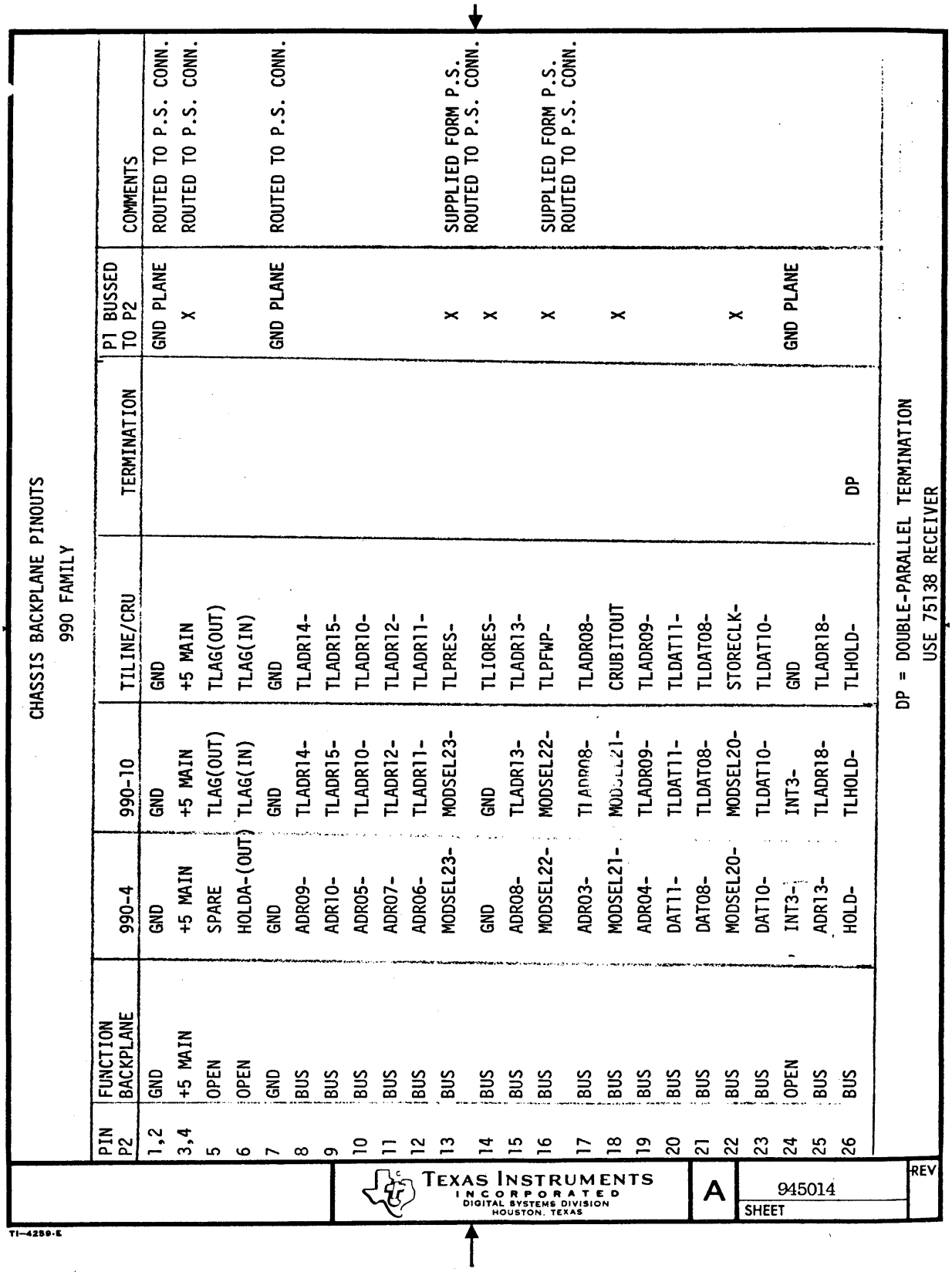
DP = DOUBLE-PARRALLEL TERMINATION
USE 75138 RECEIVER

TEXAS INSTRUMENTS
INCORPORATED
DIGITAL SYSTEMS DIVISION
HOUSTON, TEXAS

A | 945014 | REV

SHEET

TI-4259-E



CHASSIS BACKPLANE PINOUTS
990 FAMILY

PIN P2	FUNCTION BACKPLANE	990-4	990-10	TILINE/CRU	TERMINATION	P1 BUSSED TO P2	COMMENTS
1,2	GND	GND	GND	GND		GND PLANE	ROUTED TO P.S. CONN.
3,4	+5 MAIN	+5 MAIN	+5 MAIN	+5 MAIN		X	ROUTED TO P.S. CONN.
5	OPEN	SPARE	TLAG(OUT)	TLAG(OUT)			
6	OPEN	HOLDA-(OUT)	TLAG(IN)	TLAG(IN)			
7	GND	GND	GND	GND		GND PLANE	ROUTED TO P.S. CONN.
8	BUS	ADR09-	TLADR14-	TLADR14-			
9	BUS	ADR10-	TLADR15-	TLADR15-			
10	BUS	ADR05-	TLADR10-	TLADR10-			
11	BUS	ADR07-	TLADR12-	TLADR12-			
12	BUS	ADR06-	TLADR11-	TLADR11-			
13	BUS	MODSEL23-	MODSEL23-	TLPRES-		X	SUPPLIED FORM P.S. ROUTED TO P.S. CONN.
14	BUS	GND	GND	TLIORES-		X	
15	BUS	ADR08-	TLADR13-	TLADR13-			
16	BUS	MODSEL22-	MODSEL22-	TLPFWP-		X	SUPPLIED FORM P.S. ROUTED TO P.S. CONN.
17	BUS	ADR03-	TLADR08-	TLADR08-			
18	BUS	MODSEL21-	MODSEL21-	CRUBITOUT		X	
19	BUS	ADR04-	TLADR09-	TLADR09-			
20	BUS	DAT11-	TLDAT11-	TLDAT11-			
21	BUS	DAT08-	TLDAT08-	TLDAT08-			
22	BUS	MODSEL20-	MODSEL20-	STORECLK-		X	
23	BUS	DAT10-	TLDAT10-	TLDAT10-			
24	OPEN	INT3-	INT3-	GND		GND PLANE	
25	BUS	ADR13-	TLADR18-	TLADR18-			
26	BUS	HOLD-	TLHOLD-	TLHOLD-	DP		

DP = DOUBLE-PARALLEL TERMINATION
USE 75138 RECEIVER

TEXAS INSTRUMENTS
INCORPORATED
DIGITAL SYSTEMS DIVISION
HOUSTON, TEXAS

A | 945014 | SHEET | REV

TI-4259-E

CHASSIS BACKPLANE PINOUTS
990 FAMILY

PIN P2	FUNCTION BACKPLANE	990-4	990-10	TILINE/CRU	TERMINATION	P1 BUSSED TO P2	COMMENTS
27	BUS	ADR12-	TLADR17-	TLADR17-			
28	OPEN	RESTART-	RESTART-	SPARE			
29	BUS	ADR11-	TLADR16-	TLADR16-			
30	OPEN	GND	GND	GND		GND PLANE	ROUTED TO P.X. CONN
31	BUS	ADR14-	TLADR19-	TLADR19-			
32	BUS	MODSEL19-	MODSEL19-	CRUBIT13		X	
33	BUS	DAT09-	TLDAT09-	TLDAT09-			
34	BUS	MODSEL18-	MODSEL18-	CRUBIT15		X	
35	BUS	DAT02-	TLDAT02-	TLDAT02-			
36	BUS	MODSEL17-	MODSEL17-	CRUBIT12		X	
37	BUS	DAT03-	TLDAT03-	TLDAT03-			
38	BUS	MODSEL16-	MODSEL16-	CRUBIT14		X	
39,40	+12 MAIN	+12 MAIN	+12 MAIN	+12 MAIN		X	ROUTED TO P.S. CONN
41,42	-12 MAIN	-12 MAIN	-12 MAIN	-12 MAIN		X	ROUTED TO P.S. CONN
43	BUS	DAT06-	TLDAT06-	TLDAT06-			
44	BUS	OPEN	TLADR01-	TLADR01-			
45	BUS	DAT07-	TLDAT07-	TLDAT07-			
46	OPEN	INT4-	INT4-	MODSELB-			
47	BUS	ADR01-	TLADR06-	TLADR06-			
48	OPEN	INT5-	INT5-	MODSELA-			
49	BUS	ADR02-	TLADR07-	TLADR07-			
50	OPEN	INT6-	INT6-	SPARE			
51	BUS	OPEN	TLADR02-	TLADR02-			
52	OPEN	INT7-	INT7-	SPARE			

TI-4459-E

TEXAS INSTRUMENTS INCORPORATED DIGITAL SYSTEMS DIVISION HOUSTON, TEXAS

A | SHEET 945014 | REV

CHASSIS BACKPLANE PINOUTS
990 FAMILY

PIN P2	FUNCTION BACKPLANE	990-4	990-10	TILINE/CRU	TERMINATION	P1 BUSSED TO P2	COMMENTS
53	BUS	OPEN	TLADR03-	TLADR03-			
54	OPEN	INT8-	INT8-	SPARE			
55	BUS	OPEN	TLADR00-	TALDR00-			
56	OPEN	INT9-	INT9-	SPARE			
57	BUS	OPEN	TLADR04-	TLADR04-			
58	OPEN	INT10-	INT10-	GND		GND PLANE	
59	BUS	ADR00-	TLADR05-	TLASR05-			
60	BUS	GND	GND	CRUBITIN		X	
61	BUS	DATA04-	TLDAT04-	TLADAT04-			
62	OPEN	INT11-	INT11-	SPARE			
63	BUS	DAT05-	TLDAT05-	TLADT05-			
64	OPEN	INT12-	INT12-	SPARE			
65	OPEN	INT13-	INT13-	SPARE			
66	OPEN	INT14-	INT14-	INTERRUPTA-			
67	BUS	DAT00-	TLDAT00-	TLDAT00-			
68	OPEN	INT15-	INT15-	SPARE			
69	BUS	DAT01-	TLDAT01-	TLDAT01-			
70	OPEN	SPARE	SPARE	SPARE			
71,72	-5MEM	-5 MEM	-5 MEM	-5 MEM		X	ROUTED TO P.S. CONN
73,74	+5 MEM	+5 MEM	+5 MEM	+5 MEM		X	ROUTED TO P.S. CONN
75,76	+12 MEM	+12 MEM	+12 MEM	+12 MEM		X	ROUTED TO P.S. CONN
77,78	+5 MAIN	+5 MAIN	+5 MAIN	+5 MAIN		X	ROUTED TO P.S. CONN
79,80	GND	GND	GND	GND		GND PLANE	ROUTED TO P.S. CONN

TEXAS INSTRUMENTS INCORPORATED
DIGITAL SYSTEMS DIVISION
HOUSTON, TEXAS

A | SHEET 945014 | REV

TI-4239-E

ALPHABETICAL INDEX

ALPHABETICAL INDEX

INTRODUCTION

The following index lists key words and concepts from the subject material of the manual together with the area(s) in the manual that supply major coverage of the listed concept. The numbers along the right side of the listing reference the following manual areas:

- Sections - References to Sections of the manual appear as "Section x" with the symbol x representing any numeric quantity.
- Appendixes - References to Appendixes of the manual appear as "Appendix y" with the symbol y representing any capital letter.
- Paragraphs - References to paragraphs of the manual appear as a series of alphanumeric or numeric characters punctuated with decimal points. Only the first character of the string may be a letter; all subsequent characters are numbers. The first character refers to the section or appendix of the manual in which the paragraph is found.
- Tables - References to tables in the manual are represented by the capital letter T followed immediately by another alphanumeric character (representing the section or appendix of the manual containing the table). The second character is followed by a dash (-) and a number:

  Tx-yy

- Figures - References to figures in the manual are represented by the capital letter F followed immediately by another alphanumeric character (representing the section or appendix of the manual containing the figure). The second character is followed by a dash (-) and a number:

  Fx-yy

- Other entries in the Index - References to other entries in the index are preceded by the word "See" followed by the referenced entry.

USER'S RESPONSE SHEET

Manual Title: Model 990/4 Computer System Depot Maintenance Manual (945403-9701)

Manual Date: 15 May 1977 **Date of This Letter:** _____

User's Name: _____ **Telephone:** _____

Company: _____ **Office/Department:** _____

Street Address: _____

City/State/Zip Code: _____

Please list any discrepancy found in this manual by page, paragraph, figure, or table number in the following space. If there are any other suggestions that you wish to make, feel free to include them. Thank you.

Location in Manual	Comment/Suggestion

CUT ALONG LINE

NO POSTAGE NECESSARY IF MAILED IN U.S.A.
FOLD ON TWO LINES (LOCATED ON REVERSE SIDE), TAPE AND MAIL

FOLD

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL

FIRST CLASS PERMIT NO. 7284 DALLAS, TX

POSTAGE WILL BE PAID BY ADDRESSEE

TEXAS INSTRUMENTS INCORPORATED
DIGITAL SYSTEMS GROUP

ATTN: TECHNICAL PUBLICATIONS
P.O. Box 2909 M/S 2146
Austin, Texas 78769

FOLD