TeleVideo® TS 803 and 803H Technical Reference Manual

TELEVIDEO SYSTEMS, INC.

TS 803 AND TS 803H TECHNICAL REFERENCE MANUAL

TeleVideo Part Number 122910-00 Rev. B

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This document contains reference information to be used in specifying, operating, and maintaining the TS 803 and TS 803H computer systems.

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

INTRODUCTION

The TeleVideo TS 803 and TS 803H microcomputer systems are based on the Zilog Z80 microprocessor, using the same basic circuit board in different configurations.

The TS 803 contains two vertically-mounted slim-line floppy disk drives. This system features two RS-232C serial I/O ports: one configured to transmit data to a serial printer and receive data from a graphics mouse, and the other configured for a modem or similar device.

The TS 803H contains one vertically-mounted slim-line floppy disk drive and one 5 1/4-inch slim-line Winchester hard disk drive. The I/O port configuration is identical to the TS 803.

A TS 803 option board adds a single RS-422 serial I/O port to the system board. This option is field-installable.

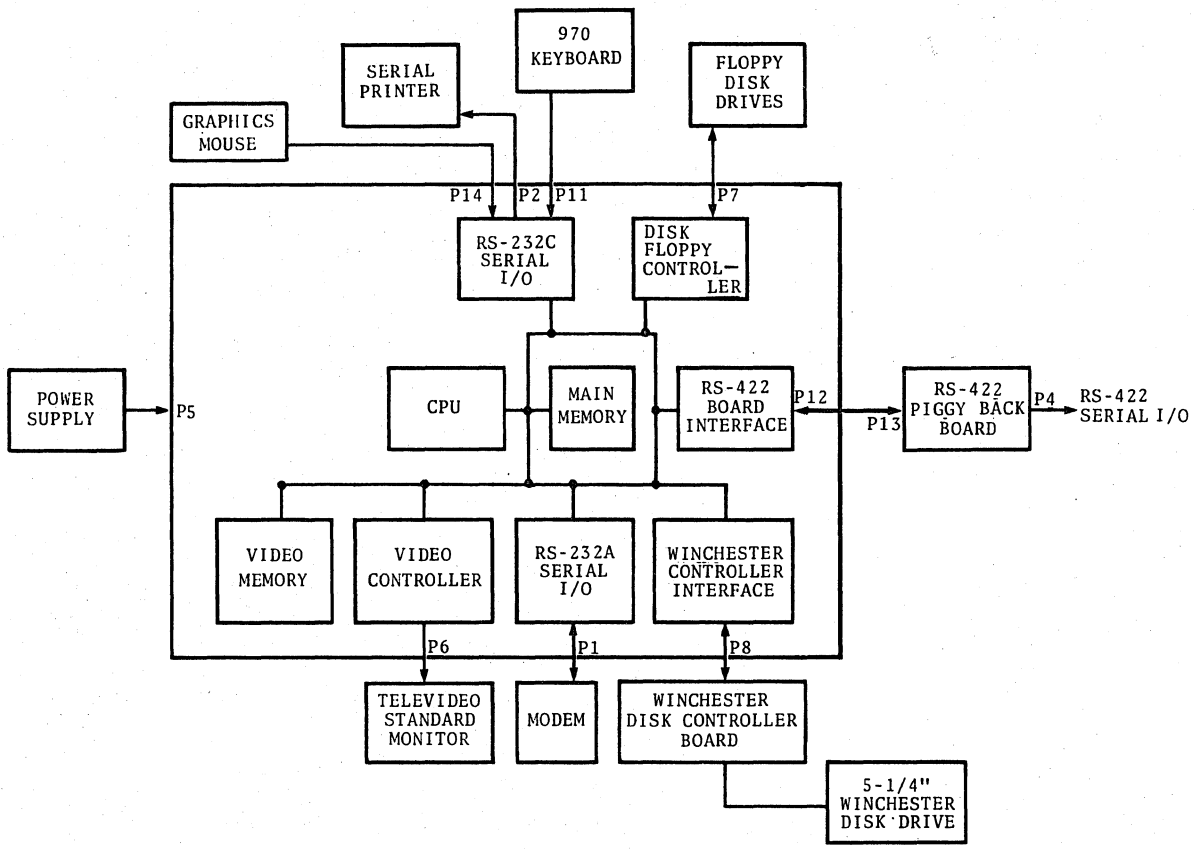
Main memory for both systems is 64 kilobytes of dynamic RAM. A separate memory, dedicated to graphics and video display, is composed of 32 kilobytes of dynamic RAM. Graphics display capability is 640 pixels horizontal by 240 pixels vertical, with 24 lines by 80 characters for alphanumeric display. Read-only memory is 8 kilobytes, used for system boot and power-up diagnostics.

Both systems use the same switching-type power supply, TeleVideo 970-type keyboard, and video driver circuits.

2. FUNCTIONAL DESCRIPTION

The TS 803 system is contained on a single circuit board. The RS-422 option board and the Winchester disk controller board are mounted piggyback fashion on the system board. A block diagram of the TS 803H, showing all system features, is in Figure 2-1.

Figure 2-1
TS 803H Block Diagram



TS 803 SYSTEM BOARD

The central processing unit functions are carried out by a Zilog Z80 CPU microprocessor device. The CPU carries out logical and computational functions of the running software, handles graphics processing, and updates video memory.

The CPU communicates with the system on a 16-bit address bus, an 8-bit data bus, and control lines. Interrupts from the system are passed to the CPU on an interrupt line. The system has six interrupting devices, including a software time-of-day clock. The order of interrup priorities as as follows:

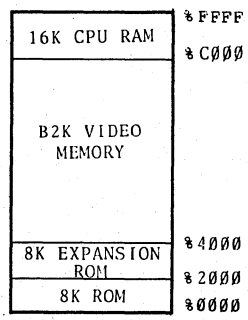
(highest)	0	RS-422 option board
	1	Z80A DART (RS-232C serial I/O)
	2	Z80 STI (RS 232C modem port)
	3	FD 1793 floppy disk controller
	4	Winchester disk controller board
(lowest)	5	Time-of-day clock

Interrupts 0 through 2 are prioritized in a daisy-chain arrangement. Interrupts 3 through 5 are wired to the Z80 STI interrupt input pins.

Main memory is configured in 64K x 1 dynamic RAM devices. Standard main memory is 64 kilobytes. Read-only memory is configured in a single 16K x 8 EPROM device.

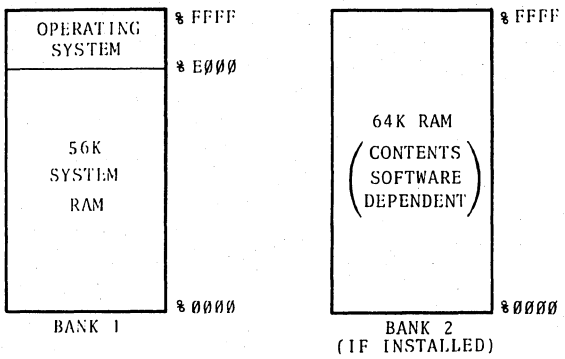
Two mappings of main memory are used in the system. At boot, the system selects the map of Figure 2-2. The lower eight kilobytes of the CPU memory address space are occupied by the system ROM. The next eight kilobytes are reserved for expansion of the ROM. The area from %4000 through %BFFF is occupied by the video memory, physically separate from main memory. The upper 16 kilobytes of the CPU address space are located in main memory, and are loaded with the operating system, such as CP/M.

Figure 2-2
Boot Memory Map



After boot, the system switches to the memory map shown in Figure 2-3. Main memory is now fully addressed, with 56 kilobytes of user space. The upper eight kilobytes of main memory are now dedicated to the operating system. The lower end of memory contains vectors to operating system BIOS routines in CP/M that in turn call video memory.

Figure 2-3
Post-Boot Memory Map



An I/O port decoder is contained in a decoder device on the system board. The decoder is addressed on address bus lines A4 through A7 as shown in Table 2-1. The decoder produces enables, which, along with the system control lines, configure the system I/O ports and pass data to peripheral devices.

Table 2-1
I/O Port Addresses

Device	Address
System Status Switch 1	%00
Diagnostic Indicators 1 and 2	%10
Diagnostic Indicators 3 and 4	%11
RS-422 Control and Auto Wait	%12
Memory Bank Select	%13
STI Device	%20-%2F
DART Device	%30-%33
RS-422 SIO Device	%40-%43
Floppy Disk Controller	%80-%83
Floppy Disk Drive Decoder	%90
Winchester Disk Controller Reset	%A0
Winchester Disk Controller	%B0-%BF
Graphics Controller	%C0-%CF

I/O port enables at addresses %00 through %13 are applied to a system control port decoder to produce the functions listed in Table 2-2. This decoder is addressed as an I/O port on the addresses shown, and data is written on lines D0 and D1 to perform the listed function.

Table 2-2
Control Port Decoder Signals

Address	D1	D0	Function
%10	1	0	Indicator 1 on
%10	0	1	Indicator 2 on
%10	1	1	Indicators 1 and 2 off
%11	1	0	Indicator 3 on
%11	0	1	Indicator 4 on
%11	1	1	Indicators 3 and 4 off
%12	0	0	RS-422 on; auto wait on
%12	0	1	RS-422 off; auto wait on
%12	1	0	RS-422 on; auto wait off
%12	1	1	RS-422 off; auto wait off
%13	0	0	Select memory bank 0
%13	0	1	Select memory bank 1
%13	1	0	Select memory bank 2

The RS-232C serial I/O channels are configured in separate devices. The Z80 STI contains a single RS-232C channel configured for interface to a modem. Two other communications channels are contained in a Z80A DART device. One channel is configured to transmit data to a serial printer at standard baud rates and to receive data from a graphics mouse. The other channel handles keyboard I/O at 9600 baud.

Timeout for the RS-232C baud rate, interrupts, and a time-of-day clock are handled through the Z80 STI. Timer settings for standard baud rates are shown in Table 2-3. To change the baud rate, load the hexidecimal value given in the table into the appropriate STI time data register.

Table 2-3
Interval Timer Settings for Baud Rates

Baud Rate	Hex	Decimal
75	80	128
110	60	96
150	40	64
300	20	32
600	10	16
1200	08	08
2400	04	04
4800	02	02
9600	01	01

The floppy disk controller on the system board supports two drives in double-sided, double-density format. This circuit is composed of a Western Digital FD1793 floppy disk controller, an SMC 9216 data separator, and a drive control latch at I/O port address %90.

The Winchester disk control board interface is installed in both the TS 803 and TS 803H. The control board is installed in the TS 803H only.

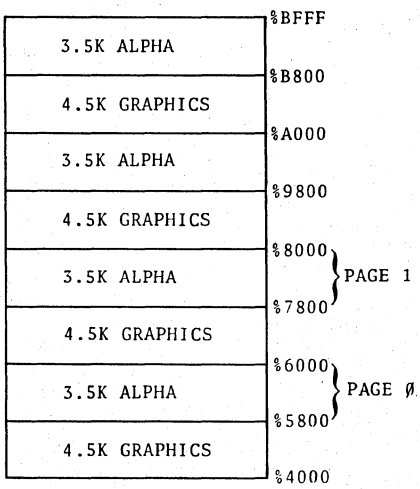
Space is allocated on the system board for a parallel interface. This area is uninstalled in any of the standard systems, and is not supported by TeleVideo.

Screen updates are provided through a Synertek SY6545 CRT controller device. This device is programmed during power-up through the system ROM for display characteristics and operating modes.

Video memory is composed of two banks of 16K x 1 dynamic RAM devices. The memory is accessible by either the CPU or the CRT controller during alternate clock cycles. All writes of data to video memory are done by the CPU. The CRT controller retrieves the data from video memory and controls the screen updates. Dynamic RAM refresh is handled by the CRT controller and is transparent to normal operation.

Video memory is mapped as shown in Figure 2-4. The memory is divided into 4.5 kilobyte portions of graphics storage, with 3.5 kilobyte portions of alpha storage. Each alpha area holds the full two kilobytes of data for a single page. Only pages 0 and 1 of the alpha area can be accessed.

Figure 2-4
Video Memory Map



A TeleVideo 925-type gate array character generator creates the dot patterns for the alphanumeric characters as they are called up from video memory. The character generator output is sent to a shift register, which generates a serial alpha bitstream. Graphics video goes directly from video memory to the shift register, bypassing the alpha circuits. The shift register output is passed through a video driver board and sent to the system monitor.

Diagnostic indications for the system are given by four LED indicators on the system board. The diagnostic code for these indicators is given in Chapter 4.

Also included on the system board is a bank of ten DIP switches, of which nine are designated to be read by software. These switches function for default baud rate selection, system mode, and general system configuration.

RS-422 OPTION BOARD

The optional RS-422 board adds a single RS-422 channel to the system. This board receives parallel data lines and control lines from the system and generates the RS-422 signal used to communicate with a TeleVideo network processor. The RS-422 channel operates according to the TeleVideo Systems Service Processor Protocol. Data is transferred between the system and service processor at a nominal 800 kilobaud rate.

WINCHESTER DISK CONTROLLER BOARD

The Winchester disk controller board receives commands and data from the system using address lines A0 through A2 to address internal registers, and data lines D0 through D7 to pass data.

The board uses a WD1010-00 controller processor. Individual registers in the controller processor are accessed through a task file register. This register is addressed on A0 through A2, and data is written or read as in Table 2-4.

Table 2-4
Task File Register

Address	Read	Write
%B0	WE 1010-00 tri-stated	WD 1010-00 tri-stated
%B1	Error flags	Write precomp cyl.
%B2	Sector count	Sector Count
%B3	Sector number	Sector Number
%B4	Cylinder low	Cylinder low
%B5	Cylinder high	Cylinder high
%B6	Sector/Drive/Head	Sector/Drive/Head
%B7	Status Register	Command register
%B8 thru %BF	Not used	Not used

A summary of the task file register functions is give in Table 2-5.

Table 2-5
Task File Register Functions

Register	Function
Error Register	Contains error flags for bad block detect, CRC data field, ID not found, aborted command, TK0000 error, and data address mark (DAM) error.
Write Precomp Cylinder	Defines the starting cylinder number at which the RWC (reduced write current) line is asserted. This value is internally multiplied by four to obtain the actual cylinder.
Sector Count	Contains the number of sectors that are to be transferred to buffer RAM.
Sector Number	Contains the starting sector of a command.
Cylinder Number Low	Least significant eight bits of the starting cylinder number.
Cylinder Number High	Carries the most significant bits of the starting cylinder number. The other bits of this register are unused.
Sector/Drive/Head	Contains the sector size, drive number, and head number parameters for the operation.
Status Register	Contains status bits for device busy, device ready, write fault (same as WF line), seek complete (same as SC line), data request (same as BDRQ line), command in progress, and error register flags set.
Command Register	This register contains the current command: a. RESTORE - restore heads b. SEEK - for seek operations between multiple drives c. READ SECTOR - transfers one or more sectors to disk d. WRITE SECTOR - writes one or more sectors to disk e. SCAN ID - updates the head, sector size, sector number, and cylinder registers f. WRITE FORMAT - used to format a single track

For a typical operation, the task file registers are written to or read for status, and a command is given to the command register. The WD1010-00 then tri-states the address bus and executes the command. At the end of the operation, the task file is again opened to the system.

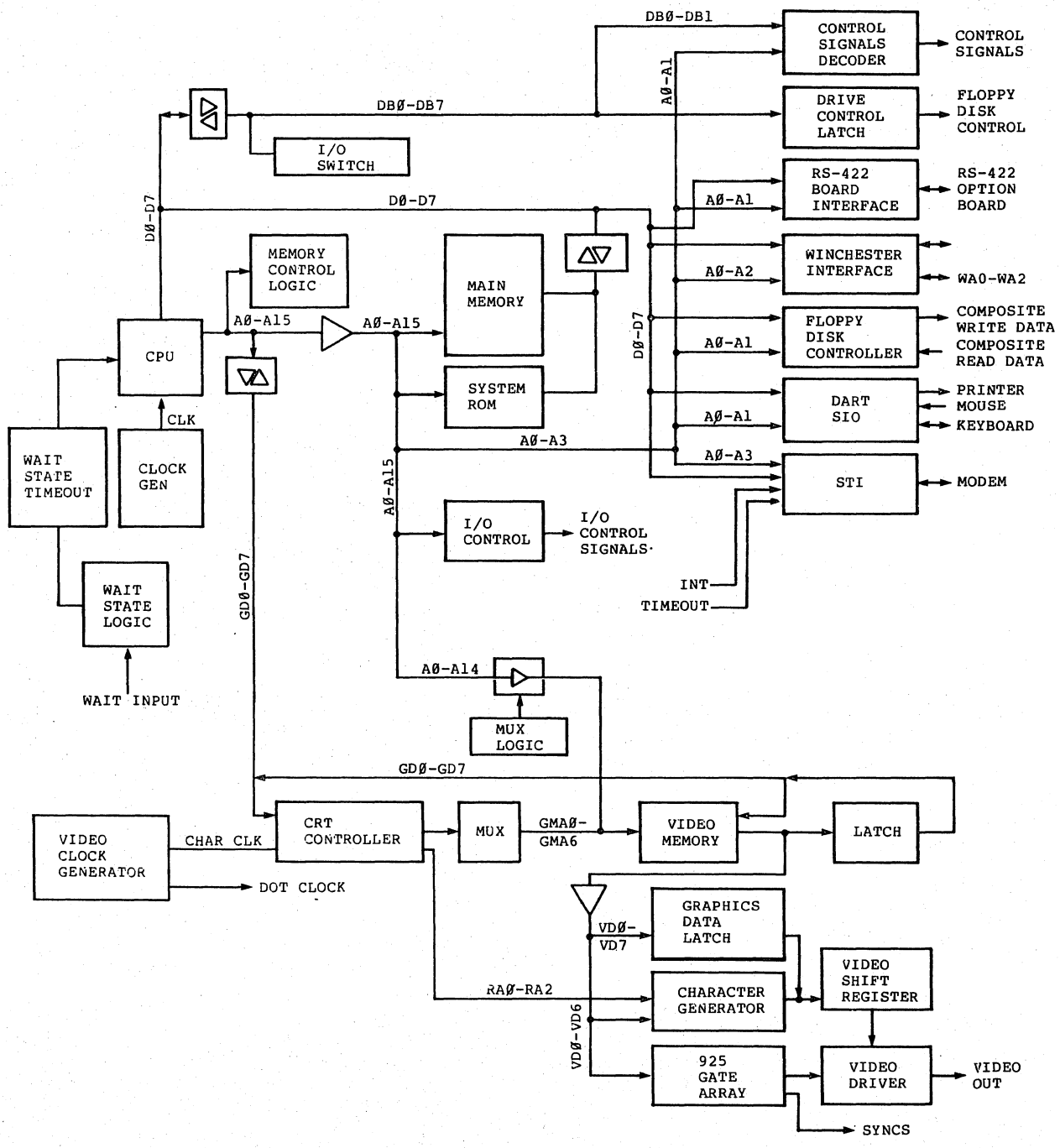
A detailed description of the WD 1010-00 device is given in the referenced Western Digital documentation.

3. CIRCUIT DESCRIPTION

This section contains circuit descriptions of the major functional blocks on the system board.

The system board contains the CPU, main memory, I/O ports, controllers, and video display circuits for the system. A block diagram of the system board is shown in Figure 3-1.

Figure 3-1
Block Diagram of the Main Board



CENTRAL PROCESSOR UNIT

The major components of the central processing unit are:

A43	Zilog Z80A CPU System Microprocessor
A51, A42	Address Drivers
A52	Control Buffers
A18	Z80 STI
A57	2764-2 System ROM

The active lines for the CPU are diagrammed in Figure 3-2 and are listed with a description in Table 3-1.

Figure 3-2
CPU Active Lines

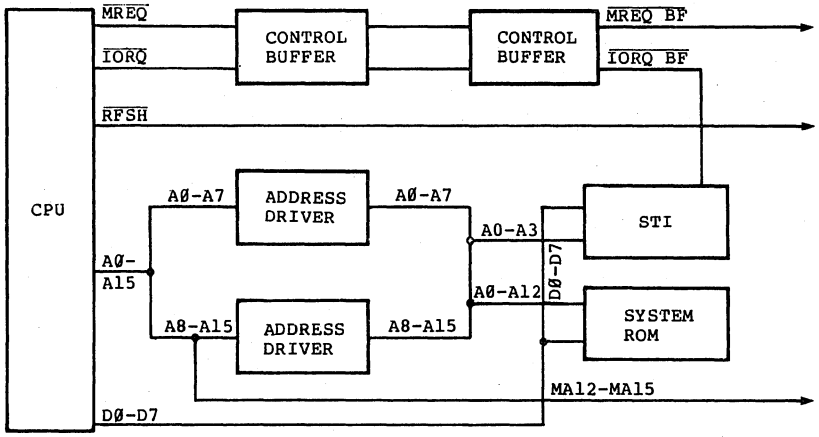


Table 3-1
CPU Devices

Device/Active Line	Source/Description
Z80A CPU	Handles central processing functions, graphics display-related processing, and all writes to video memory. CPU timing conforms to the standards shown in the Zilog Data Book.
-MREQ	CPU Memory Request. Indicates that address bus holds valid address for memory read or write operation.
-IORQ	CPU Input/Output Request. Indicates that lower half of address bus holds a valid address for an I/O read or write operation.
-RFSH	CPU Memory Refresh. -RFSH together with -MREQ indicates that lower seven bits of address bus contain a refresh address to RAM.
A0-A15	CPU address lines to system, driven through address drivers.

MA12-MA15	CPU memory access lines, driven directly from CPU to drive memory decoder ROM.
D0-D7	CPU/System data bus lines.
Address Drivers	Drives address lines A0 through A15.
Control Buffers	One set of buffers control lines from CPU and passes them through combinational logic to derive associated control signals.
Z80 STI	Serial Timer Interrupt Controller. Sets lower order interrupt priorities.

Interrupt priorities are set using the interrupt controller facilities of the Z80 STI for the lower order interrupts, and daisy chaining the interrupts for the RS-232C and RS-422 ports in standard Z80A fashion. Interrupt priorities are listed in Chapter 2.

System clock is generated from a 16 MHz clock module output. The signal is passed to two four-bit counters. One counter produces the 4 MHz system clock signal, an 8 MHz clock for the TTL logic in the memory control circuit, and a 2 MHz clock for the wait state timeout circuit. The system clock signal is passed through a driver transistor before being applied to the system devices. The other counter produces a divide-by-thirteen clock signal of 1.23 MHz, used to derive all the RS-232C baud rates through the Z80 STI.

Resets from the keyboard are de-glitched before application to the system.

READ-ONLY MEMORY

The major components of the read-only memory are:

A57	2764-2 System ROM
A59	Memory Decoder
A58	Data Buffer

The active lines for the read-only memory are diagrammed in Figure 3-3 and are listed with a description in Table 3-2.

Figure 3-3
Read-Only Memory Active Lines

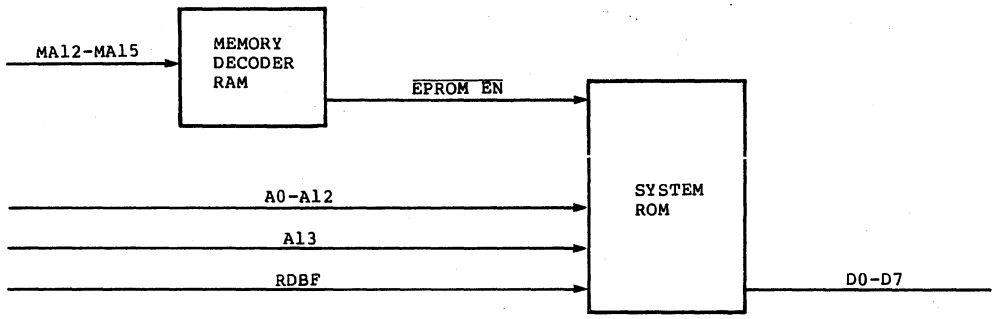


Table 3-2
Main Memory Components

Device/Active Line	Source/Description
System ROM	Read-only memory.
A0-A12	CPU. Address lines to ROM.
A13	CPU. Allows higher-capacity compatible devices to be installed.
-EPROM EN	CPU. Memory decoder line to enable ROM.
-RD BF	CPU. Control line that enables a read of ROM. Also controls data buffer that puts ROM data on data bus lines D0 through D7.

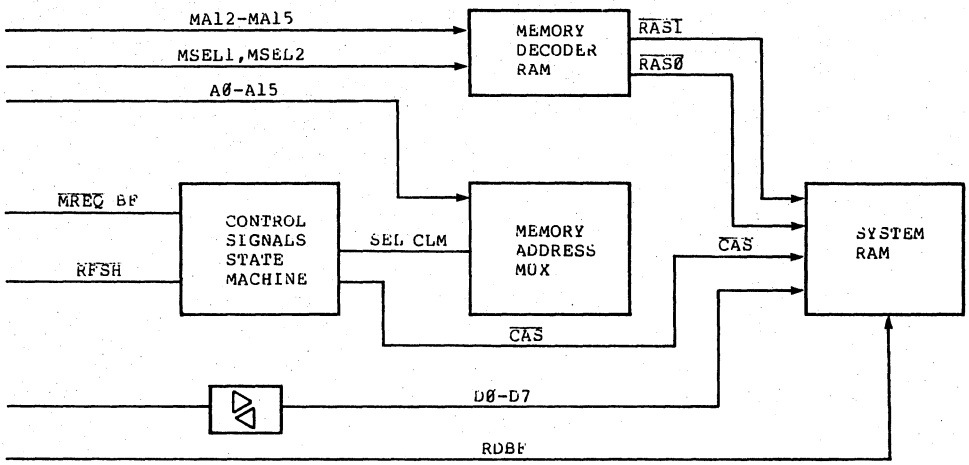
MAIN MEMORY

The major components of main memory are:

A1,A2, A6,A7,A16, A17,A24,A25, A29,A30,A32, A33,A39,A40, A48,A49	64K x 1 Dynamic RAM
A41,A50	Address Multiplexers
A71,A79	Control Signals State Machine
A59	Memory Decoder ROM

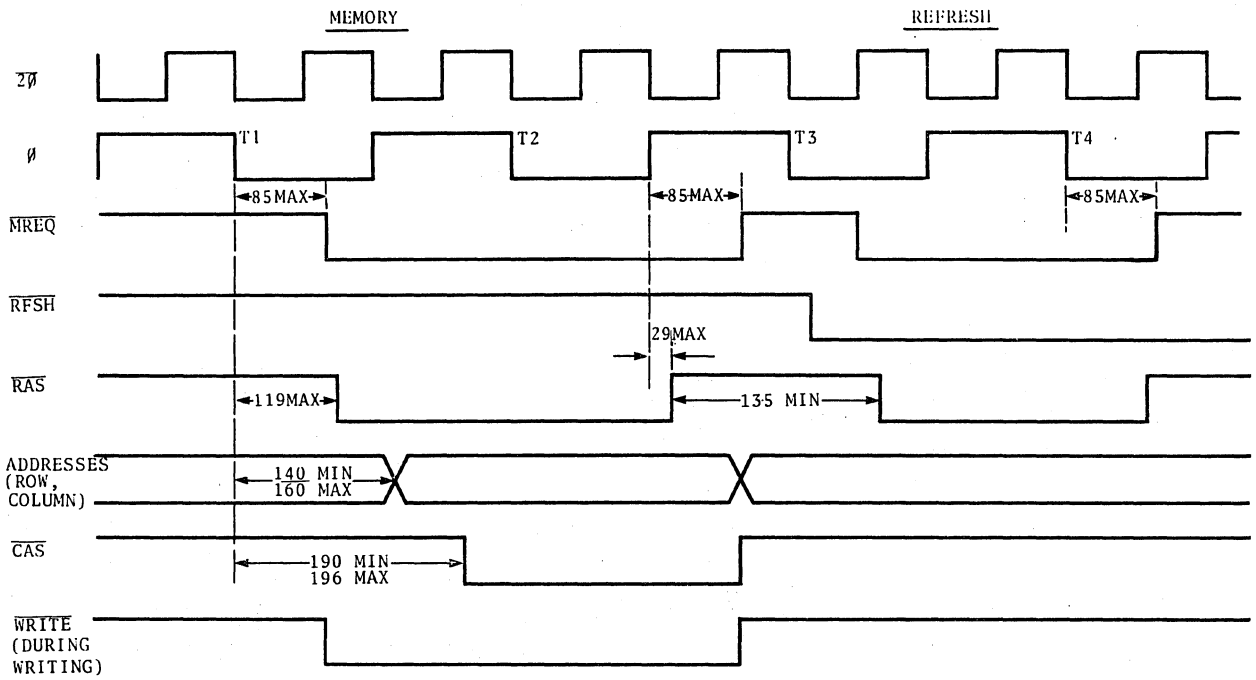
The active lines for the main memory are diagrammed in Figure 3-4 and are listed with a description in Table 3-3.

Figure 3-4
Main Memory Active Lines



A timing diagram for memory operations is shown in Figure 3-5. Other signals not shown in Figure 3-4 are as shown in the Zilog Data Book.

Figure 3-5
Timing For Memory Operations



Memory Control Logic

The sequence of operations in Table 3-3 takes place during a memory access.

Table 3-3
Memory Access Sequence of Operations

Device/Active Line	Source/Description
-MREQ BF,-RFSH	CPU. Inactive high to hold state machine in a preset state.
MA12-MA15	CPU. Along with MEM SEL1 and MEM SEL2, from I/O port decoder, form command address to memory decoder ROM.
-MREQ BF	CPU. Activated to begin memory access.
-RAS	State Machine. Active when -MREQBF goes goes active as an AND function of -MREQ BF and the third F/F of the state machine. -RAS is ANDed with memory decoder ROM signals to produce bank select signals -RAS0 or -RAS1.
SEL CLM	State Machine. Produced on next clock after -RAS to change memory address multiplexers from a row to a column address.
-CAS	State Machine. Produced on next clock after SEL CLM to complete the memory address.

For a memory refresh, the preset -RAS signal from the state machine is ANDed with the -RFSH signal from the CPU to hold the state machine in the preset state. The memory request signal, -MREQ BF gates the -RAS signal to the RAS gates, where it is ANDed with the buffered refresh signal -RFSH BF to produce simultaneous refresh of both memory banks. Memory refresh is carried out every instruction fetch cycle.

DECODERS

The major components of the decoders are:

A60,A61	I/O Signals Decoder
A20	System Control Signals Decoder
A11	ID Switch Buffer
A68,A21,A77	Wait State Logic

The active lines for the decoders are diagrammed in Figure 3-6 and are listed with a description in Table 3-4.

Figure 3-6
Decoder Active Lines

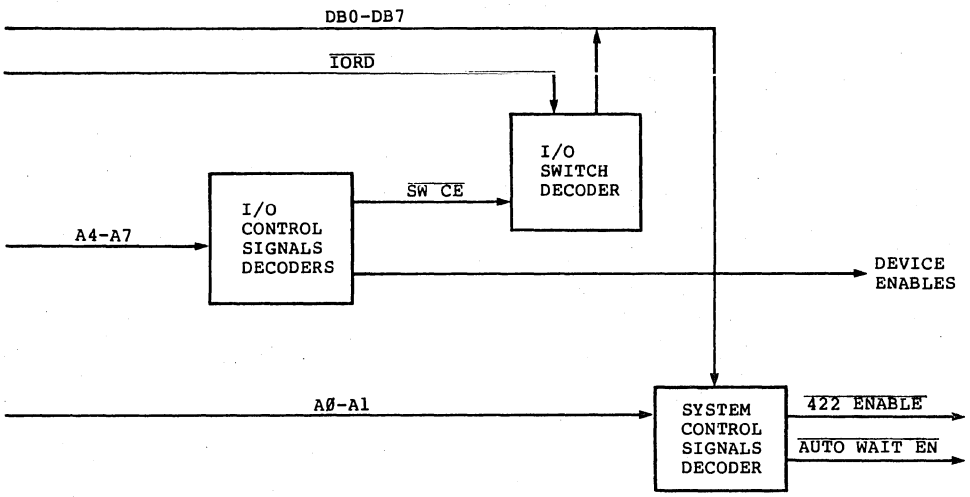


Table 3-4
Decoder Devices

Device/Active Line	Source/Description
I/O Control Signals Decoder	Contained in two demultiplexer devices, addressed by lines A4 through A7. Line A7 changes decoder from low order address selection to high order address selection. A listing of port addresses is given in section 2.
System Control Signals Decoder	Contained in dual 4-bit addressable latch. Latch is addressed with lines A0 and A1. Data is supplied to latch on lines DB0 and DB1.
ID Switch Buffer	Settings of 10-section DIP switch are enabled to data bus lines DB0 through DB7 with decoded signal -SW CE and CPU signal -IORD. Nine sections of the DIP switch are used, with each switch position being software defined as listed in the system User's Manual.

Wait State Logic

Wait states are inserted by peripheral devices to allow response time to a CPU request. Waits for the graphics section, Winchester disk controller, and RS-422 interface are passed through combinational logic to produce the signal -WAIT. When video memory is accessed, a single automatic wait state is produced by a flip-flop before being combined into the -WAIT signal. Wait signals from the RS-422 board are given a single wait state in a similar flip-flop. The signal -WAIT is passed through a timeout counter, clocked by the 2 MHz clock, to limit the maximum wait time to 32 microseconds. The timeout is applied to the -WAIT input of the CPU.

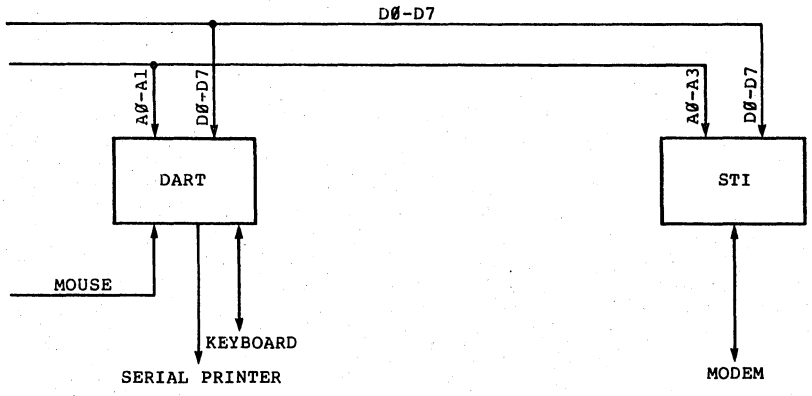
SERIAL I/O

Both systems contain RS-232C ports for modem, printer, keyboard, and graphics mouse. The major serial I/O components are:

A18	Z80 STI
A26	Z80A DART

The active lines for the serial I/O are diagrammed in Figure 3-7 and are listed with a description in Table 3-5.

Figure 3-7
Serial I/O Active Lines



Default baud rates for the RS-232C serial I/O channels are set by a DIP switch on the system board as defined in the system User's Manual.

The system board also contains an interface to the RS-422 option board. This board is optional in the TS 803 and TS 803H.

Table 3-5
Serial I/O Devices

Device/Active Line	Source/Description
Z80A DART	Handles keyboard I/O, printer output, and mouse input. Baud rate for keyboard channel is derived by dividing 153.8 KHz clock signal at the DART down to 9600 baud. Asynchronous baud rate for the printer output is generated by a timeout signal from Z80 STI on channel TB0. Jumper option on board connects incoming clock for synchronous operation.
Z80 STI	Z80 STI serial I/O channel is configured as modem interface or for general purpose. Baud rate is derived from STI timer channel TA0. STI outputs are buffered before application to connector P1.

The system uses a standard TeleVideo 970-type keyboard with certain keycaps changed. The keyboard contains an Intel 8048 microprocessor to scan the keyboard matrix for a closure. When a closure is detected, the keyboard sends a code for the key position to the system through the DART. The system must perform a hardware reset when a CTRL/RESET is sent from the keyboard.

Keyboard codes are listed in the system User's Manual.

FLOPPY DISK CONTROLLER

The major components of the floppy disk controller are:

A28	FD1793 Floppy Disk Controller Device
A37	9216B Data Separator Device
A45,A46,A54	Write Precompensation Circuit
A53	Clock Divider
A14	Drive Control Latch

The active lines for the floppy disk controller are diagrammed in Figure 3-8 and are listed with a description in Table 3-6.

Figure 3-8
Floppy Disk Controller Active Lines

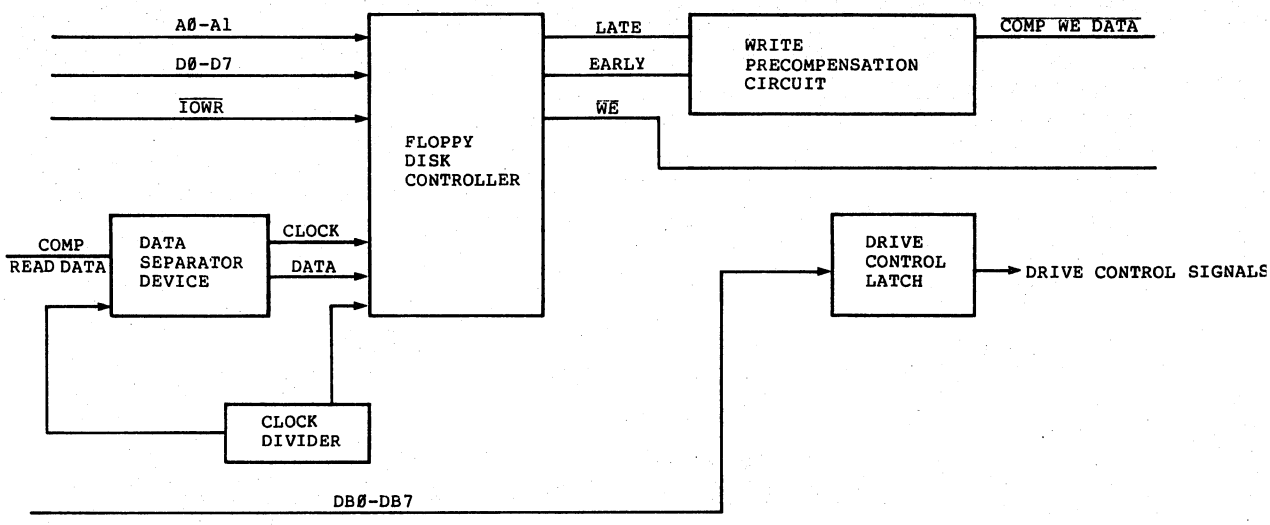


Table 3-6
Floppy Disk Controller Devices

Device/Active Line	Source/Description
Floppy Disk Controller	Provides serial/parallel conversion of data passing between floppy disk and system, as well as all drive control functions, such as head step, head direction, write protect, track 0 detection, and write precompensation. Controller can be programmed to handle seek track, read sector, write sector, read address, read track, write track, and force interrupt operations.
D0-D7	Carries data and programming signals between the FDC and CPU.
EARLY,LATE	FDC. Signals to precompensation logic. These signals are outputs of the FDC.
Precompensation Logic	This circuit is based on a shift register. The LATE signal is applied to the F pin, the EARLY signal is applied to the H pin and the normal signal is applied to the G pin. When the WD signal of the FDC goes high, the appropriate bit position is shifted out of the register, along with zeros in all the other bit positions.

	Write precompensation appears in the form of the position of the bit in the data stream output of the shift register. Precompensation is applied in 250-nanosecond increments. A normal bit occupies the second position in the shifted data stream and occurs 500 nanoseconds after the stream starts. An early bit appears 250 nanoseconds sooner, and a late bit 250 nanoseconds later. The duration of the entire string of pulses from the precompensation logic, including the data bit and all the zeros in the other bit positions, is much less than the minimum duration between two adjacent bits in the disk data stream.
Clock Divider	A counter that clocks the precompensation logic at 4 MHz. A 1 MHz signal from the divider is applied to the WD input of the FDC to gate the data bits into a definite early, late, or normal category.
-IOWR	CPU. Two flip-flops are used to make the -WE signal shorter to satisfy the data hold time
tor.	
Data Separator	Separates the raw read data and clock signals for the FDC.
Drive Control Latch	Selected as an I/O port on address %90, Latch receives control signals on DB0 through DB7.
tor.	
Data Separator	Separates the raw read data and clock signals for the FDC.
Drive Control Latch	Selected as an I/O port on address %90, Latch receives control signals on DB0 through DB7. Other drive control signals are generated by the FDC according to programmed instructions from the system.

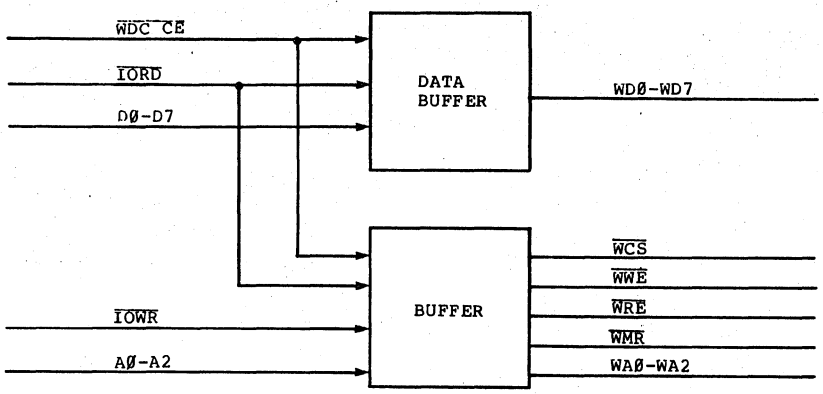
WINCHESTER CONTROLLER INTERFACE

The major components of the Winchester controller interface are:

A4	Data Buffer
A15	Buffer

The active lines for the Winchester controller interface are diagrammed in Figure 3-9.

Figure 3-9
Winchester Controller Interface Active Lines



The components of the Winchester controller interface act to pass data between the Winchester disk controller board and the system. The interface is written to as an I/O port by the system.

VIDEO MEMORY

The CPU performs all writes to video memory, and reads data from video memory to perform graphics formatting. All graphics control is contained in firmware in system ROM and is acted on by the CPU. On alternate clock cycles, the CRT controller reads data from video memory to perform screen updates. The major components of video memory are:

A83,A84, A91,A92,A98, A99, A106,A107, A113,A114,A121, A122, A126,A127, A131,A132	Type 4116 Dynamic RAM devices
A73	CPU Address Buffer
A72,A88	CPU Address Multiplexer
A97,A105	Data Out Latch
A90,A112	Data In Latch

The active lines for video memory are diagrammed in Figure 3-10 and are listed with a description in Table 3-7.

Figure 3-10
Video Memory Active Lines

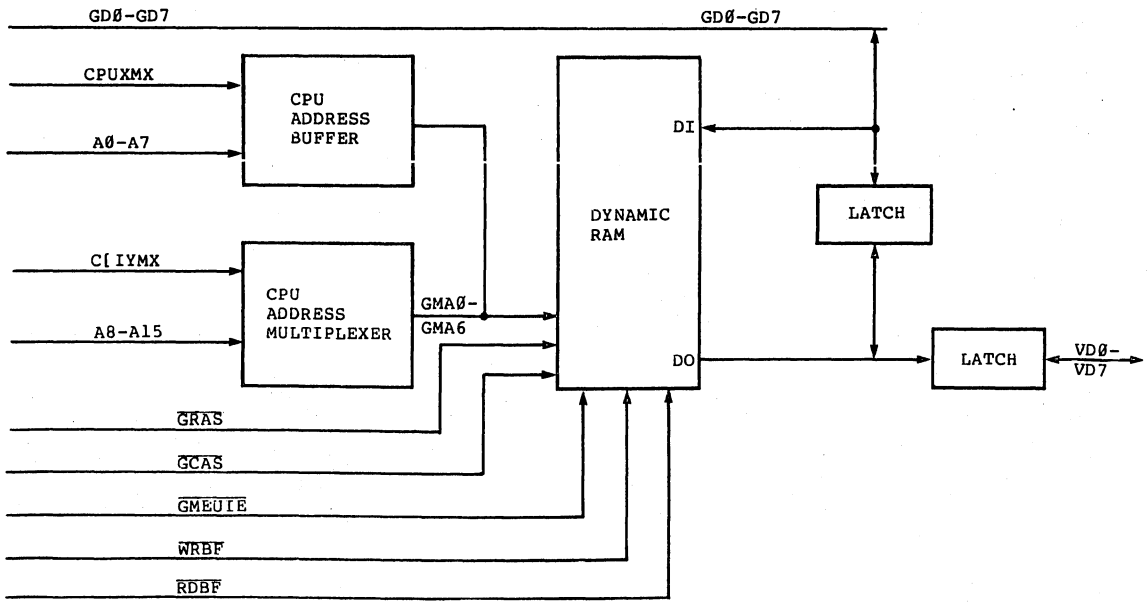


Table 3-7
Video Memory Devices

Device/Active Line	Source/Description
-GRAS,-GCAS	Video memory control logic. These signals are continuously generated every eight dot clock times. Used by both the CPU and CRT controller accesses to video memory.
A1-A15	CPU. Address to video memory.
CPUXMX,CPUYMX	Video memory control logic. Multiplex control lines for the CPU address to video memory.
-GWAIT	Video memory control logic. Holds off CPU access to video memory until the display cycle is completed. With -GWAIT, the CPU can request video memory at any time, but can only access it at CPU access times (alternate to display cycles).
GD0-GD7	CPU. Buffered data lines D0-D7, carries write data to video memory. Buffer is controlled by memory decoder line -GMEMSEL.
-GMEMWE	Video memory control logic. Write enable for video memory.

-RDBF	CPU. With -GMEMSEL, enables buffers for CPU read of video memory on GD0-GD7.
GMA0-GMA6	CRT controller. Address to video memory for display cycle read. Both banks of memory are addressed at the same time.
VD0-VD7	Video memory. Carries read data from video memory. Data is multiplexed using -MSB and -LSB. In this way, two words of video data are read in each display cycle access. The first word is placed on the screen immediately after access, the second word is displayed during CPU access times.

CRT CONTROLLER AND CHARACTER GENERATOR

The CRT controller retrieves data from video memory for screen updates, and performs refresh of the dynamic RAM in video memory. Alphanumeric data from the video memory is passed through a character generator and shifted into a serial bit stream for the video display circuits. Graphics data is sent directly to the shift register. The major components of the CRT controller and character generator are:

A89	Synertek SY6545 CRT Controller
A80,A81	CRT Controller Address Multiplexer
A96	Multiplexer
A123,A124	Video Clock Generator
A119	Type 2532 Character Generator ROM
A104	TeleVideo 925 Gate Array Attribute Generator
A120	Graphics Data Latch
A125	Shift Register
Q2,Q3	Video Drivers

A block diagram of the CRT controller is shown in Figure 3-11.

Figure 3-11
CRT Controller Block Diagram

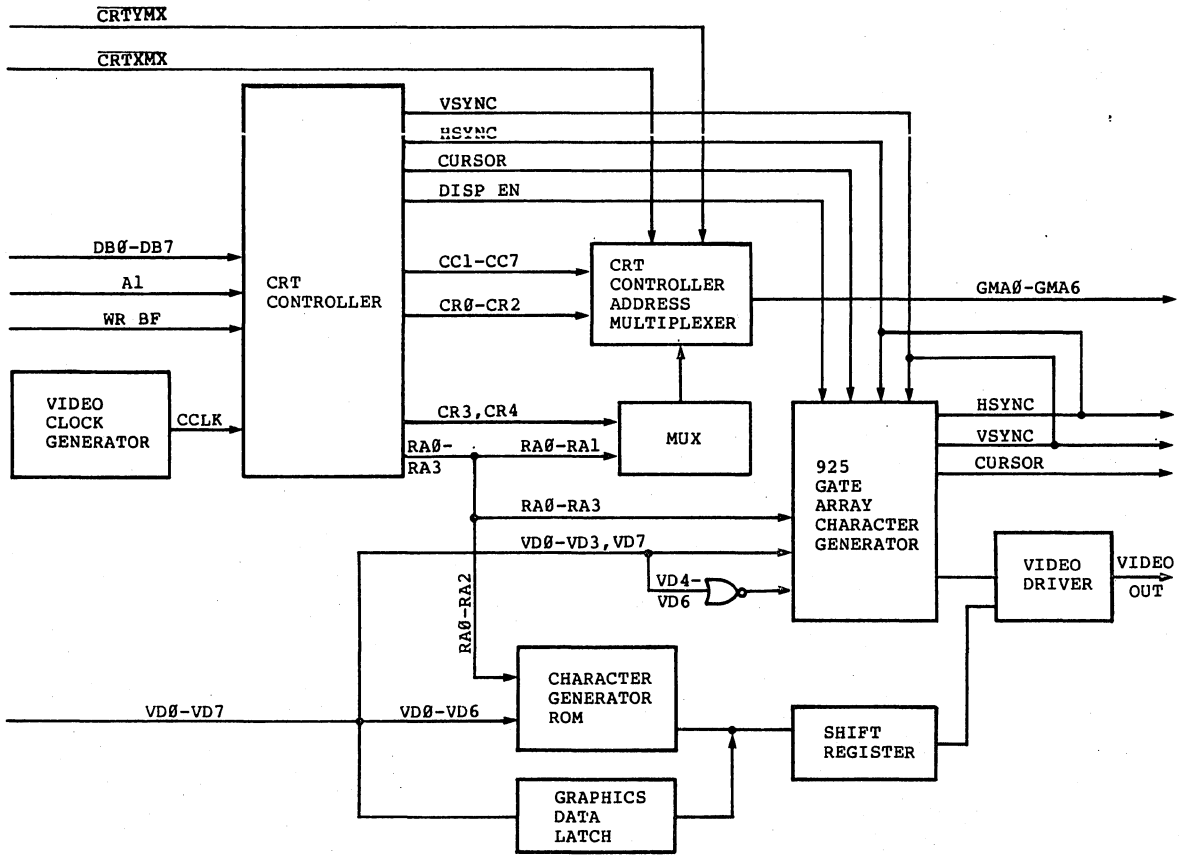


Table 3-8 lists the CRT controller and character generator components and their description.

Table 3-8
CRT Controller and Character Generator Components

Device/Active Line	Source/Description
CRT Controller	Performs screen updates and generates control signals for video display. The controller is operated in the shared memory mode and the input address mode.
VSYNC,HSYNC	CRT controller. Vertical and horizontal synchronization signals for video monitor.
CURSOR	CRT controller. Active for cursor position.
DISP EN	CRT controller. Active when CRT controller is generating display information.
GD0-GD7	CPU. Carries programming data to CRT controller.
A1	CPU. Selects CRT controller internal register for programming or status read.
-WR BF	CPU. Selects the direction of data transfer, write or status read, with the CRT controller. Timing for the operations between the CPU and the CRT controller is derived from the system clock through a dual flip-flop divider. The clock, Ø2, is produced when the controller is selected for the operation through the -6545CS line.
Video Clock Generator	Using a 13.6 MHz crystal and divider, produces the character clock and dot clock. The character clock is used as a time base for internal CRT controller functions. The dot clock is used by the fast logic of the display circuits, and to shift out the video bit stream.
CRT Controller Address Mux	Gates the row and column address lines from the CRT controller to video memory address lines GMA0 though GMA7.
CR0-CR4,RA0,RA1	CRT controller. Row address lines. A multiplexer selects lines CR3, CR4, RA0, and RA1 for alpha mode, and de-selects these lines for graphics mode.

CC1-CC7	CRT controller. Column address lines to video memory.
-CRTXMX,-CRTYMX	Video memory control logic. Controls the gating of row and column addresses to video memory address lines GMA0 through GMA7.
Character Generator	A read-only memory containing the fonts for display characters. Four character sets are included in the ROM. These sets are selected at jumper options E8 and E9 as described in the system User's Manual.
VD0-VD6, RA0-RA2	Video memory/CRT controller. These lines form the address to the character generator.
Graphics Data Latch	In graphics mode, as controlled by the ALPHA/-GRAPHICS line from the CRT controller, bypasses the VD bus lines around the character generator. The ALPHA/-GRAPHICS line is switched as an I/O port from the CPU, and the mode is programmed on line GD0 through CPU data line D0.
Shift Register	Takes in alpha or graphics data and creates a serial bit stream for the video drivers.
Attribute Gate Array	Lines VD0 through VD6, RA0 through RA3 are applied to the attribute gate array to generate screen attributes and other signals for the video monitor.
Video Drivers	Boost the video signal for application to the TeleVideo monitor video board.

TS 803 OPTION BOARD

The TS 803 option board plugs into P12 of the sytem board and supplies an RS-422 interface to the system. The board contains the following major components:

A5	Z80A SIO
A2	Differential Line Receiver
A1	Differential Line Driver
A4	Clock Divider

Baud rate for the SIO device is derived from the system clock. The MODEM BAUD RATE line to the SIO device is non-functional. When the board is installed in the system, it occupies the highest priority in the CPU interrupt structure by having its IEI pin tied to +5 Vdc.

WINCHESTER DISK CONTROLLER BOARD

The WD1000-05 Winchester Disk Controller board provides all control and data handling functions needed to interface the system with a 5 1/4-inch Winchester disk drive. Figure 3-12 shows a block diagram of the WD1000-05.

The major components of the WD1000-05 disk controller board are:

U24	WD1100-11 Host Interface, Head and Drive Select, and Buffer Ram Controller
U23	WD1010-00 Winchester Disk Controller
U16	WD1100-10 Write Precompensation and Data Separator
U25	Type 6116 Buffer RAM
U26	Board Busy Tristate Buffer
U5	Error Amplifier
U11,U18	Pump Logic
U13	Voltage Controlled Oscillator (VCO)
U27	Host Interface Bus Transceiver
U3	Differential Line Receiver
U17	Precompensation Logic
U4	Differential Line Transmitter

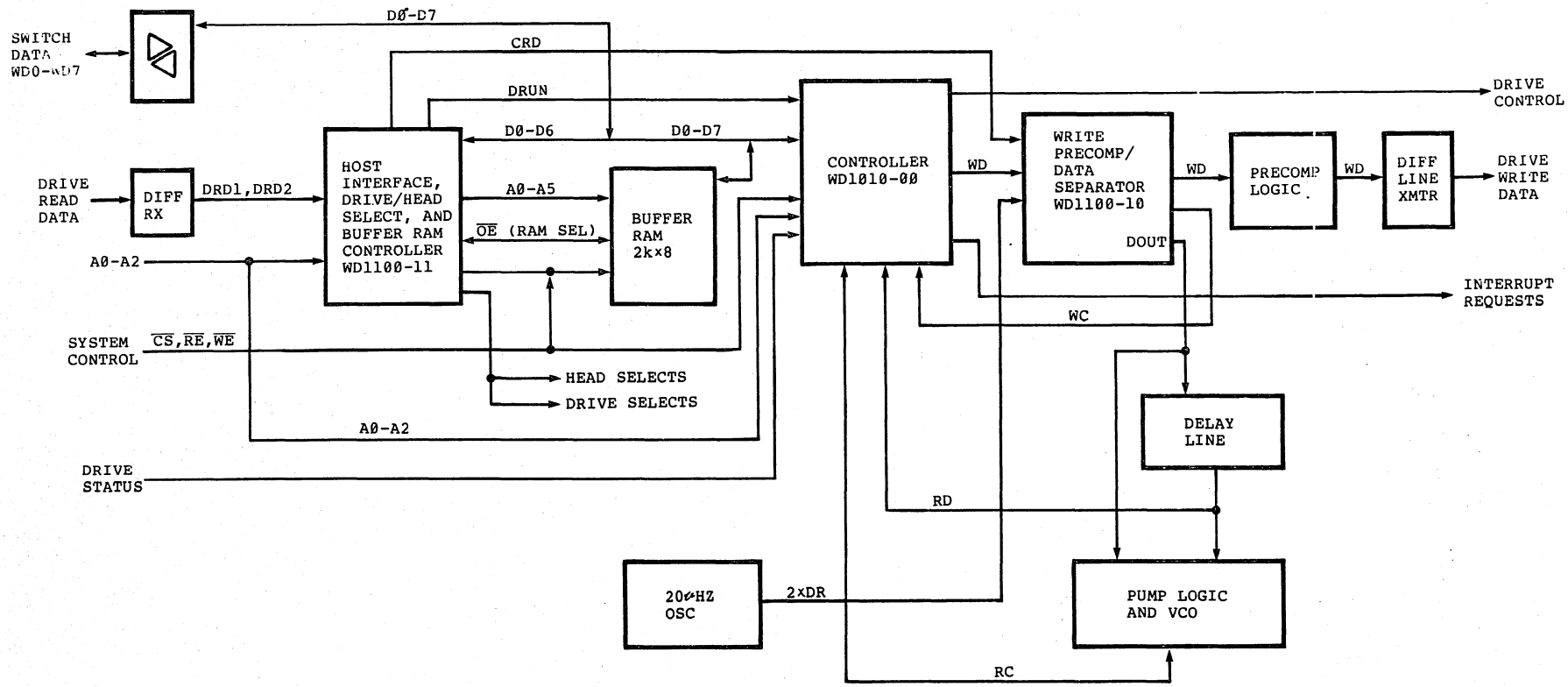


Figure 3-12
Winchester Disk Controller Board Block Diagram

System/Controller Interface

The system programs the Winchester controller board by accessing the WD1010-00 controller device Task File registers.

The active lines for the system/controller interface are diagrammed in Figure 3-13 and are listed with a description in Table 3-9.

Figure 3-13
System/Controller Interface Active Lines

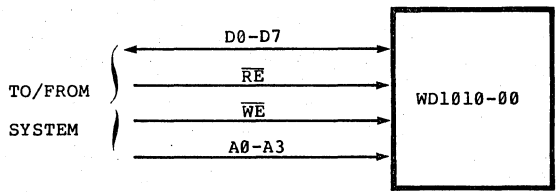


Table 3-9
System/Controller Interface Components

Active Line	Source/Description
A0-A3	System. Task file register address.
-WE or -RE	System. -WE to activate task file write, or -RE to activate task file read.
D0-D7	System. Data or command.

Register addresses and contents are summarized in Chapter 2.

Operations with Buffer RAM

The Winchester controller board uses a 2 kilobyte-by-8-bit buffer RAM to interact with the system during disk read or write operations. When writing to disk, the system writes the data to the buffer RAM on a sector basis. After a sector of data is loaded into buffer RAM, the WD1010-00 reads the data from the buffer RAM to the disk.

The active lines for the buffer RAM are diagrammed in Figure 3-14 and are listed with a description in Table 3-10.

Figure 3-14
Buffer RAM Active Lines

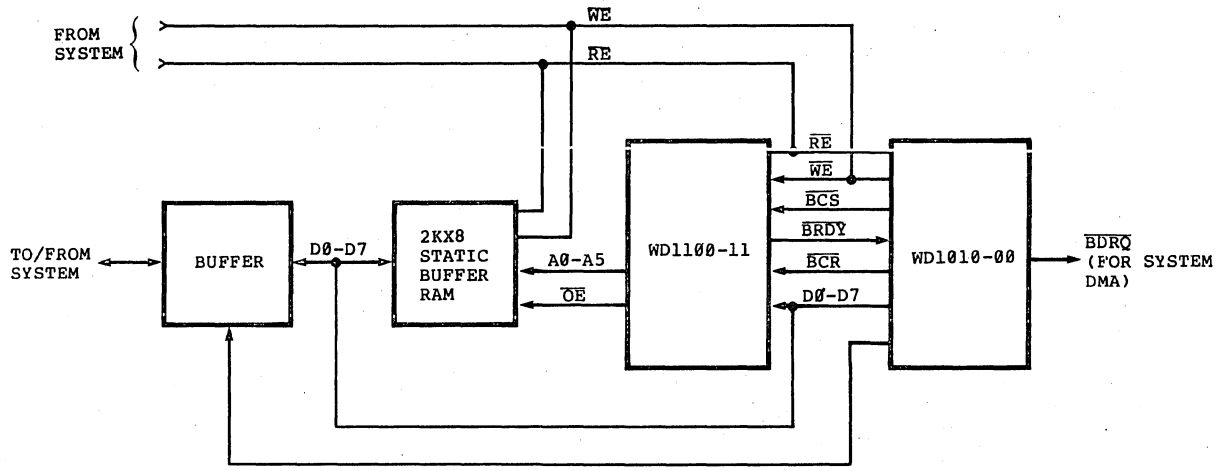


Table 3-10
Buffer RAM Components

Active Line	Source/Description
D0-D7	System. Sets up Write Sector command in WD1010-00 task file and writes data to buffer RAM.
-BCR	WD1010-00. Strobed to zero counter in WD1100-11.
BDRQ	WD1010-00. Active to indicate that the controller has set the drive up to receive data.
-BCS	WD1010-00. Set high to enable host control of buffer RAM. Transceiver direction is ready for write.
-WE	System. Loads buffer and increments counter with -CS.
-BRDY	WD1100-11. Active to indicate buffer full.
INTRQ	WD1010-00. Signals end of command to system.
-BCS	WD1010-00. Active to disconnect host control of buffer RAM. Board busy tristate buffer on line WD7 is activated by -BCS to prevent system access during next operation.
-RE	WD1010-00. Reads buffer RAM to transfer data to disk (described below).

-BCS	WD1010-00. Set high to allow next operation by system. Board busy tristate buffer inactive.

Reads of buffer RAM occur after a sector of data has been loaded to the RAM from the disk. For a read from buffer RAM, see Table 3-11.

Table 3-11
Read from Buffer RAM

Active Line	Source/Description
D0-D7	System. Sets up data and Read Sector command in WD1010-00 task file.
-BCS	WD1010-00. Active to disconnect host control of buffer RAM. Board busy tristate buffer on line WD7 is activated by -BCS to prevent system access during next operation.
-BCR	WD1010-00. Strobed to zero counter in WD1100-11.
-WE	WD1010-00. Loads buffer from disk (described below), and increments counter with -CS.
BRDY	WD1100-11. Active to indicate buffer full.
-BCR	WD1010-00. Strobed to zero counter in WD1100-11.
-BCS	WD1010-00. Set high to enable system control of buffer RAM. Board busy tristate buffer inactive.
-BDRQ	WD1010-00. Active to initiate transfer to system.
-RE	System. Reads buffer RAM and increments counter with -CS.
-BRDY	WD1100-11. Active to indicate buffer empty.
-INTRQ	WD1010-00. Set high to stop operation.

Multiple sector writes and reads are handled through a sector count register and multiple sector flag. When this flag is set, the controller re-loads the buffer RAM after each transfer and decrements the register. When the sector count register is zeroed, the controller ends the loop as for a single sector transfer.

Writing Disk Data

The write sector command requires that the Winchester controller locate the place on the disk that is to receive the data, control the write operation to buffer RAM by the system, then read the data from buffer RAM, condition the data into MFM format, and write the data to disk.

Under MFM, clock bits are recorded only when two successive data bits are missing in the serial data stream. Using MFM reduces the total number of bits required to record a given amount of information on the disk. Because this effectively doubles the amount of disk capacity, it is termed "double density".

Encoding MFM follows three rules: (a)if the current data cell contains a data bit, then no clock is generated; (b)if the previous data cell contained a data bit, then no clock is generated; (c)if the previous data cell and the present data cell are vacant, then a clock is generated in the current clock cell. Data and clock cells are defined by the state of the write clock line, WC. If WC is low, it is a data cell; if WC is high, it is a clock cell. Both clock and data cells are 100 nanoseconds long in ST506-compatible drives.

The active lines for writing disk data are diagrammed in Figure 3-15 and are listed with a description in Table 3-12.

Figure 3-15
Writing Disk Data

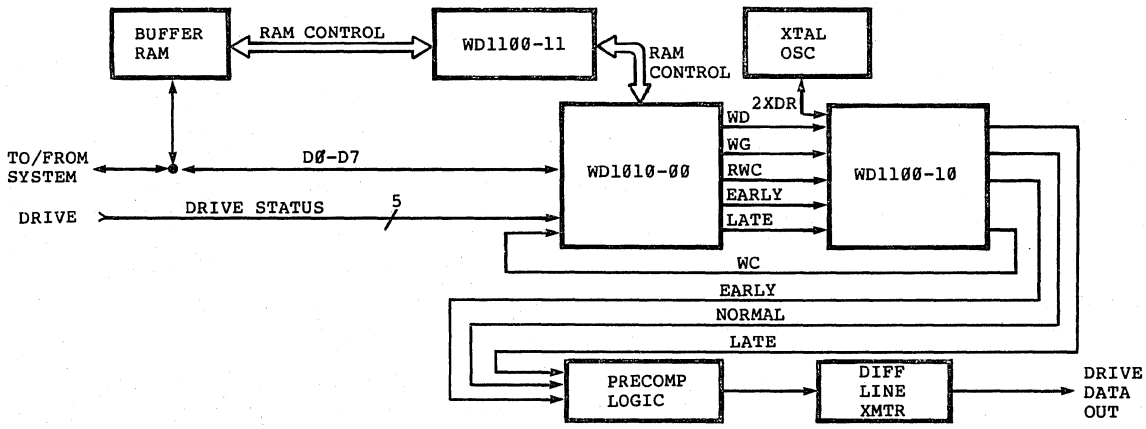


Table 3-12
Writing Disk Data

Active Line	Source/Description
D0-D7	System. Write sector command. The WD1010-00 checks its cylinder registers against the current cylinder position.

-BCR	WD1010-00. Strobed to begin write to buffer RAM by system.
BRDY	WD1100-11. Buffer RAM full.
-BCS	WD1010-00. Active to disconnect host control of buffer RAM. Board busy tristate buffer on line WD7 is activated by -BCS to prevent system access during next operation.
-STEP,-DIRET	WD1010-00. Moves head to locate cylinder.
-SEEK COMPLETE	Drive. Informs WD1010-00 that the head settling time for the current step is expired. If current step is not the required cylinder position, the head is moved again. After seek to desired cylinder, controller checks for desired sector address by reading data from drive.
WG	WD1010-00. Write gate signal to WD1100-10.
-WC	WD1100-10. Carries 5 MHz write clock, derived from 2XDR clock signal, to WD1100-00.
-RWC	WD1010-00. Reduced write current signal; turns on precompensation circuits for write to disk.
-WD	WD1010-00. Write data as read from buffer RAM and serialized by WD1010-00.
-EARLY,-LATE	WD1010-00. Precompensation signals to WD1100-10. Precompensation is used to counteract the effects of dynamic bit shift when writing the inside recorded tracks of the disk. Dynamic bit shift results when a bit on the disk influences the position of an adjacent bit. The leading edges of the bits are moved closer together, or further apart, depending upon the polarity of each bit. Because the positions of the bits shift as they are written to the disk, the data is harder to recover without error. Write precompensation is applied to counteract the effects of dynamic bit shift. Precompensation predicts the direction a bit will be shifted, then writes the bit out of position in the opposite direction to the shift. The prediction is done in the WD1010-00 by checking the next two data bits, the last bit written, and the present bit.

EARLY,NORMAL, LATE	WD1100-10. Precompensation signals to precompensation logic. Data is shifted +/-12 nanoseconds from normal position.
Data	Differential Line Driver. Carries MFM formatted, precompensated, RS-422 write data to drive head.
-BCS	Set high to allow next operation by system. Board busy tristate buffer inactive.

Reading Disk Data

For disk reads, the Winchester disk controller board locates the sector to be read, identifies the start of the data field, reads the data in from the disk, separates the data and clock signals, writes the data to buffer RAM, and controls the system read of the data out of buffer RAM.

The active lines for reading disk data are diagrammed in Figure 3-16 and are listed with a description in Table 3-11.

Figure 3-16
Reading Disk Data

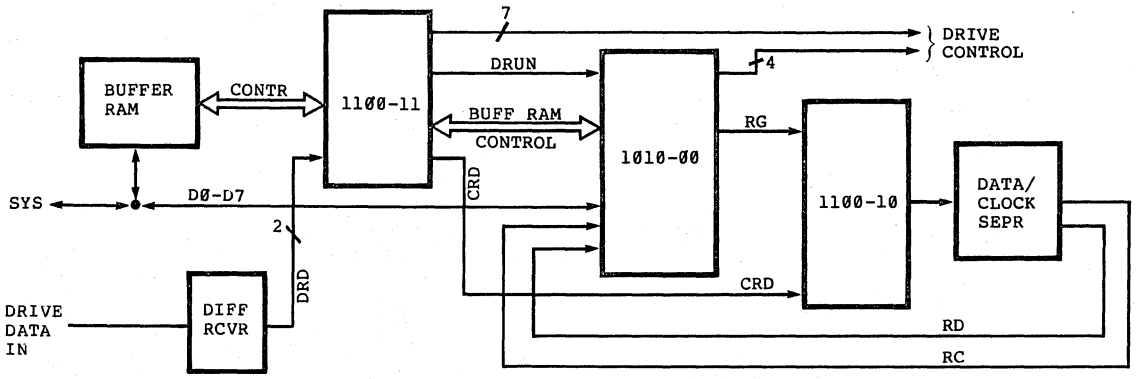


Table 3-13
Disk Data

Active Line	Source/Description
D0-D7	System. Read sector command. The WD1010-00 checks its cylinder registers against the current cylinder position.
-BCS	WD1010-00. Active to disconnect host control of buffer RAM. Board busy tristate buffer on line WD7 is activated by -BCS to prevent system access during next operation.

-STEP,-DIRET	WD1010-00. Moves head to locate cylinder.
-SEEK COMPLETE	Drive. Informs WD1010-00 that head settling time for the current step has expired. If current step is not the required cylinder position, the head is moved again. After seek to desired cylinder, controller checks for desired sector address by reading data from drive.
-DRD1,-DRD2	Differential Data Receiver. Carries differential data from drive.
CRD	WD1100-10. Composite read data.
DRUN	WD1100-11. Output of internal one-shot that retriggers on data field. When DRUN is counted high for 2 consecutive bytes, the ID field must be found within the next 8 disk revolutions, or an error is signalled. When the ID field is found, an address mark (AM) must be found within 15 bytes of the end of the data field. If the AM is not found in eight retries, an error is signalled.
-RG	WD1010-00. Set low to begin read of data from disk. This line may also be lowered for two byte times during the search for the AM to allow WD1010-00 to re-lock to the reference clock. An address mark (AM) identifies the start of a field of information within each sector of data. The WD1010-00 looks for the AM pattern, consisting of the data pattern %A1, with a missing clock pattern %0A. According to the rules of MFM encoding, the data byte %A1 requires a missing clock pattern of %0E, so the address mark can only be on disk by design.
Dout	WD1100-10. Carries data to phase detector and VCO to separate read data and clock signals.
RD	WD1100-10. Read data signal.
RC	VCO. Read clock signal.
-BCR	WD1010-00. Strobed to begin write of data to buffer RAM by WD1010-00.
-BCS	Set high to allow next operation by system. Board busy tristate buffer inactive.

INTRQ	WD1010-00. Set high to indicate that buffer RAM is full and system may initiate read.

Pump Logic and VCO

Using MFM, the board circuits must remain in synchronization with the data without clock bits on every data bit. The pump logic and VCO circuits synthesize clock bit timing when the clocks are present, and synchronize to clock bits when they are present. The synthesized clock, RC, is used as the read clock for the WD1010-00.

The VCO is held locked to the Dout signal of the WD1100-10 through the pump logic. This circuit is essentially a three-state machine that operates in a continuous loop around pump-up, reset, and pump-down. A block diagram of the pump logic and VCO is shown in Figure 3-17.

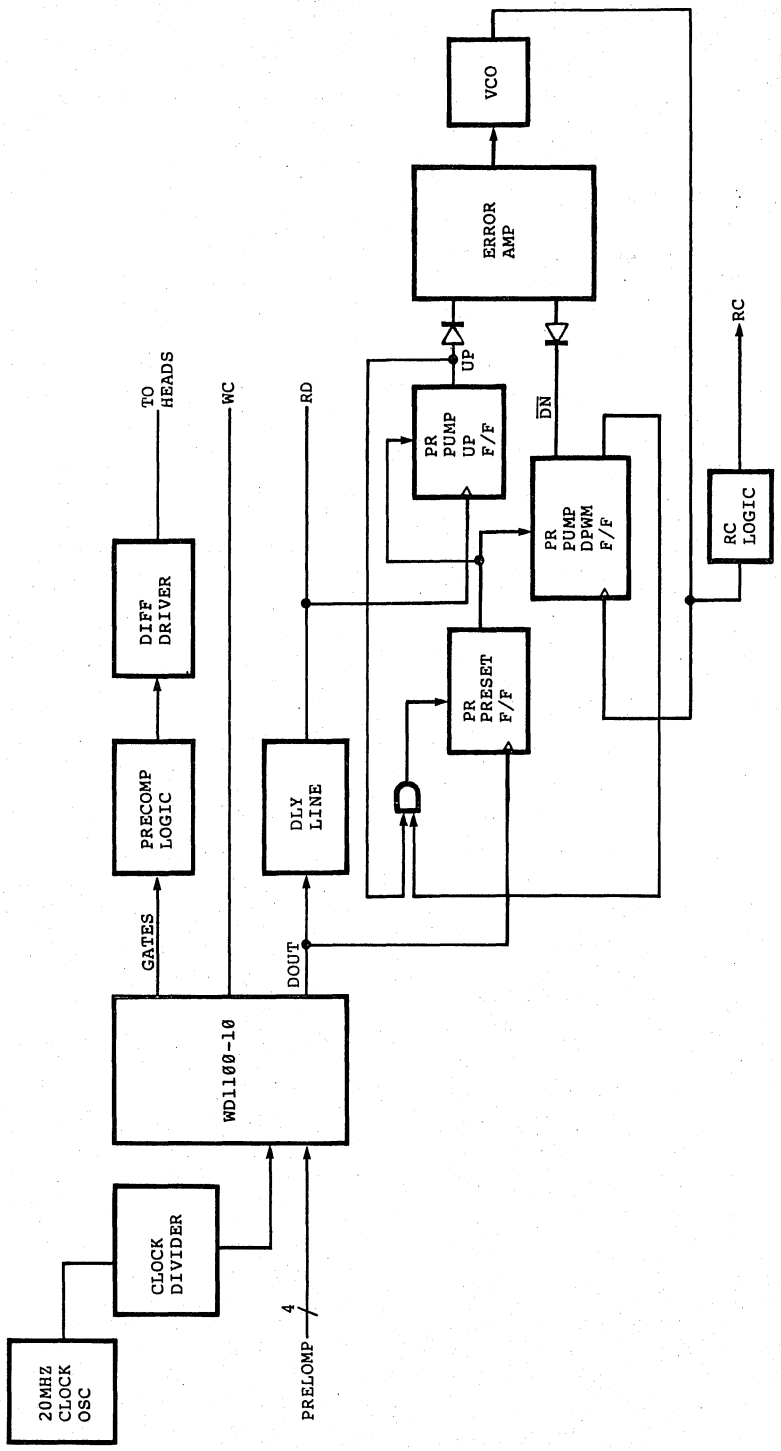
Assuming an initial state of preset, all -Q outputs of the circuit are set low. This produces a low state at the UP line, and a high state at the -DOWN line. When a data bit at the Dout pin of the WD1100-10 clocks the preset flip-flop, it sets the pump flip-flop preset signals high. If a delayed data bit clocks the pump-up flip-flop first, the UP line gets toggled low, causing a pump up error voltage. If a VCO bit clocks the pump-down flip-flop first, the -DOWN line gets toggled low, causing a pump down error voltage. If both signals arrive simultaneously, both flip-flips are toggled and the net error voltage is zero. Coincident signals give a toggle to the preset flip-flop to place the circuit into its initial state.

During write data operations, and when the board is idle, the data rate of the WD1100-10 is the write data rate, derived from the crystal-controlled oscillator 2XDR signal. Because this presents a stable signal at the Dout pin of the WD1100-10, the circuit tends to idle in a loop around the three states. The net average frequency of the VCO at this time is slightly below the write data rate.

During read data operations, the data rate at the Dout pin varies according to disk speed, media inconsistencies, and other variables. Now the VCO signal makes wider variations in the same loop as it tracks the data rate.

The pump signals are presented to an error amplifier, which generates voltage variations of between 1.7 and 3.3V for extreme pump-down and pump-up conditions. This produces a net VCO frequency of 10.0000 MHz +/-.0005 MHz. The VCO output signal is divided to produce a read clock for the WD1010-00.

Figure 3-17
Pump Logic and VCO Block Diagram



4. SYSTEM MAINTENANCE

The TS 803 and TS 803H contain self test diagnostics that are automatically run during system initialization at power-up. These diagnostics light LED indicators on the system board and send messages to the video monitor. When the tests are completed successfully, the system reads the status switches to determine the bootstrapping device. Successful conclusion of the tests and bootstrapping procedure is indicated when the system prompt is shown on the video monitor. The diagnostic LED indicators are not visible with the system case closed.

A special set of diagnostics for the system is available from TeleVideo. These diagnostics provide a more detailed check of the system, with error messages that closely isolate a malfunction.

INITIALIZATION AND SELF-TEST DIAGNOSTICS

At power-on, the system executes a hardware reset of all major components, including the CPU, CRT controller, STI, DART, RS-422 option board, floppy disk controller, and Winchester controller board. The CPU jumps to location %0000 to obtain a vector to the initialization and self-test diagnostic routine.

The first test is a memory test. The upper 1 kilobyte of main memory is tested by writing in an incrementing pattern and then reading the pattern back. If the pattern is read back correctly, a memory test is loaded into this area from system ROM. The memory test checks the rest of main memory with the same test: writing in an incrementing pattern, then reading the pattern back. During this test diagnostic LED 1 is lit. Failure of the memory test is indicated by the message:

Hardware Error: (Memory); Contact Distributor

The CPU stops executing the diagnostics and diagnostic LED 1 remains lit. Successful completion is signalled when LED 1 goes out and the system moves to the next routine.

The system shifts back to ROM for the remainder of the procedure. The CRT controller is now initialized into alpha mode, the rear panel switch is read for line frequency, and the controller is set for an 80 x 24-line display.

Next, the STI device is tested by writing a pattern into some of its data registers, and reading the pattern back. During this test diagnostic LED 2 is lit. Failure of the STI test is indicated with the message:

Hardware Error: (STI); Contact Distributor

The CPU stops executing the diagnostics and LED 2 remains lit. Successful completion is signalled when LED 2 goes out and the system moves to the next procedure.

The STI is then initialized. The UART is set for asynchronous mode, the rear panel baud rate switches are read and the timer set accordingly, and interrupts are disabled. The interrupts are disabled to allow the tests to run fully. They must be re-enabled by system software at the conclusion of the procedure.

Next, the DART is initialized. Channel B is set asynchronous, with its baud rate coming from the STI timer, and channel A is set asynchronous with its baud rate derived from system clock.

The serial I/O device on the RS-422 option board, if installed, is now initialized. Channel A is set asynchronous for the board test, and must be switched to SDLC by software at the conclusion of the procedure. Channel B of this device is not used.

The DART is now tested by sending a message to its transmit buffer and immediately checking the transmit buffer full bit for a full indication. The test then waits an interval for the device to transmit its message, and the transmit buffer full bit is again checked to verify that the transmit buffer is empty. During this test diagnostic LED 3 is lit. Failure of the DART test is indicated with the message:

Hardware Error: (DART); Contact Distributor

The CPU stops executing the diagnostics and LED 3 remains lit. Successful completion of the test is indicated when LED 3 goes out and the system moves to the next procedure.

The next test is for the serial I/O device on the RS-422 option board. This test is similar to the DART test. A message is sent to its transmit buffer and the transmit buffer full bit is immediately checked for a full indication. The test then waits an interval for the device to transmit its message, and the transmit buffer full bit is again checked to verify that the transmit buffer is empty. During this test diagnostic LED 4 is lit. Failure of the SIO test is indicated with the message:

Hardware Error: (SIO); Contact Distributor

The CPU stops executing the diagnostics and LED 4 remains lit. Successful completion of the test is indicated when LED 4 goes out and the system moves to the next procedure.

The floppy disk controller is now tested. First, the track register of the controller is checked for zero. Then the drive head is stepped in 10 tracks, and stepped out 10 tracks. The track register is again checked for zero. During this test diagnostic LEDs 1 and 2 are lit. Failure of the FDC test is indicated with the message:

Hardware Error: (FDC); Contact Distributor

The CPU stops executing the diagnostics and LEDs 1 and 2 remain lit. Successful completion of the test is indicated when LEDs 1 and 2 go out and the system moves to the next test.

The Winchester disk controller board, if installed, is then tested. A pattern is written to the board and read back for correctness. During this test diagnostic LEDs 3 and 4 are lit. Failure of this test is indicated with the message:

Hardware Error: (WDC); Contact Distributor

The system stops executing the diagnostics and LEDs 3 and 4 remain lit. Successful completion of the test is indicated when LEDs 3 and 4 go out.

The system now initiates its bootstrapping procedure, with the message:

System "boot" (Rev. x) from (boot device) in progress

The boot device may be a floppy disk, hard disk, or service processor, depending on system configuration. At the conclusion of the bootstrapping procedure, the operating system is loaded and the system displays a prompt on the monitor.

WINCHESTER DISK CONTROLLER BOARD MAINTENANCE

The DRUN and RD pulse widths are set by fixed resistors on the board to the following values:

DRUN	270 nanoseconds minimum, 300 nanoseconds nominal
RD	100 nanoseconds nominal

These values are given for reference only, no adjustment is provided on the board.

Check and adjust the VCO frequency according to the following procedure:

a. Connect a frequency counter to pin 7 of U13.

b. Verify that the VCO frequency is 10 +/-0.005 MHz. If the frequency cannot be brought to tolerance with the following steps, the VCO circuit is defective.

c. Using a non-conductive tuning tool, adjust C20 clockwise until the VCO loses lock, evidenced by a sudden change in frequency. Note the position of the adjusting screw slot.

d. Adjust C20 counterclockwise until the VCO again loses lock. Note the position of the adjusting screw slot.

e. Set the adjustment of C20 to the center of the range found in steps b and c.

APPENDIX A
REFERENCES

The publications listed here contain information on the TS 803 and TS 803H microcomputer systems:

* TS 803 User's Manual, TeleVideo
* TS 803H User's Manual, TeleVideo
* Zilog Data Book, Zilog
* Synertek SY6545 CRT Controller Data Sheet

APPENDIX B
CONNECTOR PIN ASSIGNMENTS

Table B-1
Connectors P1 and P2 (RS-232C Serial I/O)

Pin Number	RS-232C Designator	RS-232C Description	P1	P2
1	AA	Protective Ground	GND	GND
2	BA	Transmitted Data	TXD	TXD
3	BB	Received Data	RXD	RXD
4	CA	Request to Send	RTS	RTS
5	CB	Clear to Send	CTS	CTS
6	CC	Data Set Ready		DSR
7	BA	Signal Ground	GND	GND
8	CF	Data Carrier Detect	DCD	DCD
15	DB	Transmit Clock	TxC	
17	DD	Receive Clock	RxC	
20	CD	Data Terminal Ready	DTR	DTR
24	DA	Transmit Clock	TxC	

Table B-2
Connector P4 (Rear Panel RS-422 Serial I/O)

Pin Number	RS-422 Designator	RS-422 Description
1	GND	Chassis Ground
2	TxD	Transmit Data +
3	RxD	Receive Data +
4	RTS	Request to Send+
5	CTS	Clear to Send +
6	-TxC	Transmit Clock -
7	-RxC	Receive Clock -
8	GND	Signal Ground
9	-TxD	Transmit Data -
10	-RxD	Receive Data -
11	-RTS	Request to Send -
12	-CTS	Clear to Send -
13	TxD	Transmit Clock +
14	RxC	Receive Clock +
15	TEST	Test

Table B-3
Connector P5 (Power Supply)

Pin Number	Signal Designator	Signal Description
1	-12V	-12 Volts
2	-----	Not used
3	GND	Ground
4	+5V	+5 Volts
5	+12V	+12 Volts

Table B-4
Connector P6 (Video Monitor)

Pin Number	Signal Designator	Signal Description
1	HSYNC	Horizontal Sync.
3	GROUND	Video Ground
4	VIDEO	Video Signal
5	VSYNC	Vertical Sync.
6	COMP V	Composite Video

Table B-5
Connector P7 (Floppy Disk Drive)

Pin Number*	Signal Designator	Signal Description
6	-DR SEL 3	Select Drive 3
8	-INDEX	Index/Sector
10	-DR SEL 0	Select Drive 0
12	-DR SEL 1	Select Drive 1
14	-DR SEL 2	Select Drive 2
16	-MOTOR ON	Motor On
18	-DIR SEL	Direction Select
20	-STEP	Step
22	-COMP WE DATA	Composite Write Data
24	-WR EN	Write Enable
26	-TRACK 0	Track 0 Detect
28	-WR PROTECTED	Write Protected Detect
30	COMP READ DATA	Composite Read Data
32	-SIDE SEL	Side Select

*Odd numbered pins tied to ground.

Table B-6
Connector P8 (Winchester Controller Interface)

Pin Number	Signal Designator	Signal Description
1	WD0	Data Line 0
3	WD1	Data Line 1
5	WD2	Data Line 2
7	WD3	Data Line 3
9	WD4	Data Line 4
11	WD5	Data Line 5
13	WD6	Data Line 6
15	WD7	Data Line 7
17	WA0	Address Line 0
19	WA1	Address Line 1
21	WA2	Address Line 2
23	-WCS	Controller Chip Select
25	-WWE	Controller Write Enable
27	-WRE	Controller Read Enable
29	-WWAIT	Wait
35	WINTRQ	Controller Interrupt Req.
39	-WMR	Controller Reset

* Even numbered pins tied to ground.

Table B-7
Connector P9 (Composite Video)

Pin Number	Signal Designator	Signal Description
1	GND	Ground
2	COMPV	Composite Video

Table B-8
Connector P11 (Keyboard)

Pin Number	Signal Designator	Signal Description
1	SHIELD GND	Shield Ground
2	+12V	+12 Volts
3	GND	Signal Ground
4	KBD TxD	Data from Kybd.
5	KBD RxD	Data to Kybd.
6	RESET	Reset

APPENDIX C
DIP SWITCH SETTINGS

Table C-1
DIP Switch Settings

Section	Setting	Function
1	closed (right)	Baud rate (see Table C-2)
2	closed (right)	Baud rate (see Table C-2)
3	closed (right)	Baud rate (see Table C-2)
4	closed (right)	TS 803
	open (left)	TS 803H
5	closed (right)	Required setting (TS 803 only) Local (TS 803H only)
	open (left)	Remote (TS 803H only)
6	closed (right)	Required setting (TS 803 only) 2-head drive (TS 803H only)
	open (left)	4-head drive (TS 803H only)
7	closed (right)	60 Hertz (default)
	open (left)	50 Hertz
8	closed (right)	Not used (TS 803 only)
	open (left)	Required setting (TS 803H only)
9	closed (right)	Black on green screen
	open (left)	Green on black screen (default)
10	closed (right)	Not used

Table C-2
Printer Baud Rates

DIP Switch Sections			Baud Rate
1	2	3	
C	C	C	9,600 (default)
O	C	C	4,800
C	O	C	2,400
O	O	C	1,200
C	C	O	600
O	C	O	300
C	O	O	150
O	O	O	75

C = Switch closed (right)
O = Switch open (left)

APPENDIX D
ASCII CHARACTER CODE CHART

Figure D-1
ASCII Character Code Chart

Bits 7 6 5	0_0	0_1	0_2	0_3	1_0	1_1	1_2	1_3
4 3 2 1 (Column → / Row ↓)	0	1	2	3	4	5	6	7
0 0 0 0	0	NUL	DLE	SP	0	@	P	`	p
0 0 0 1	1	SOH	DC1	!	1	A	Q	a	q
0 0 1 0	2	STX	DC2	"	2	B	R	b	r
0 0 1 1	3	ETX	DC3	#	3	C	S	c	s
0 1 0 0	4	EOT	DC4	$	4	D	T	d	t
0 1 0 1	5	ENQ	NAK	%	5	E	U	e	u
0 1 1 0	6	ACK	SYN	&	6	F	V	f	v
0 1 1 1	7	BEL	ETB	'	7	G	W	g	w
1 0 0 0	8	BS	CAN	(	8	H	X	h	x
1 0 0 1	9	SKIP HT	EM	)	9	I	Y	i	y
1 0 1 0	10(a)	LF	SUB	*	:	J	Z	j	z
1 0 1 1	11(b)	VT	ESC	+	;	K	[	k	{
1 1 0 0	12(c)	FF	FS	,	<	L	\	l	|
1 1 0 1	13(d)	CR	GS	-	=	M	]	m	}
1 1 1 0	14(e)	SO	HOME RS	.	>	N	^	n	~
1 1 1 1	15(f)	SI	NEW LINE US	/	?	O	_	o	DEL RUB

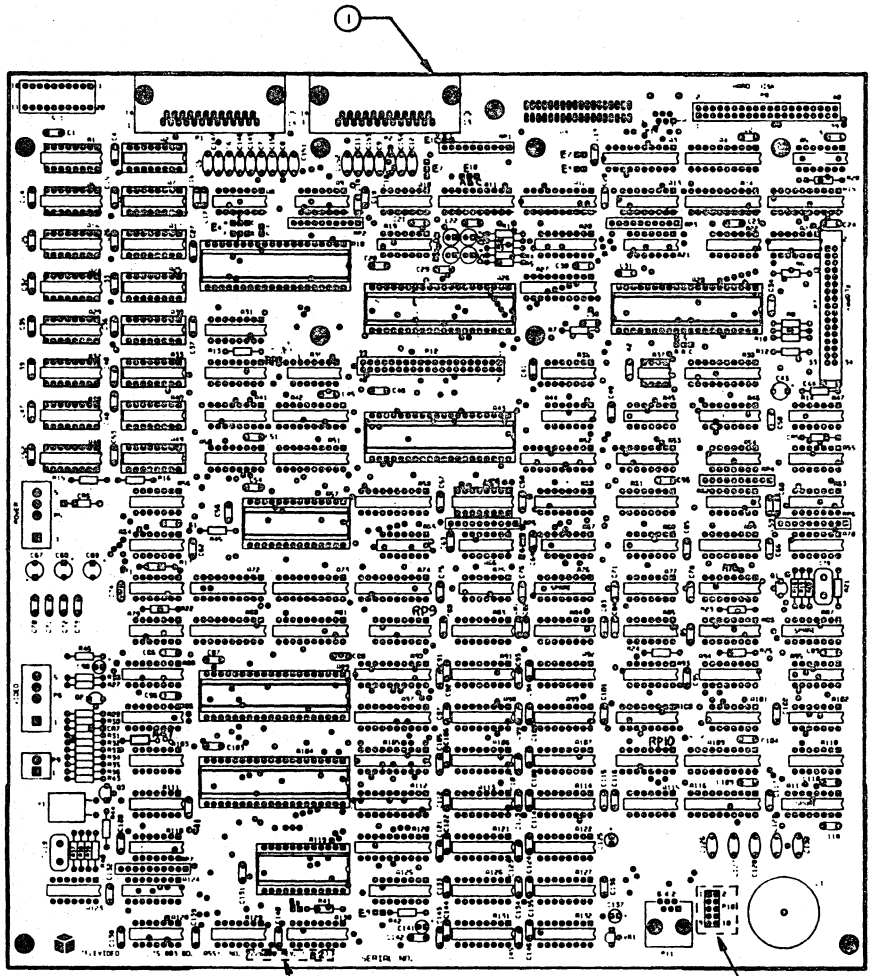
ASCII Code Table
Abbreviations For Control Characters

NUL	null	FF	form feed	CAN	cancel
SOH	start of heading	CR	carriage return	EM	end of medium
STX	start of text	SO	shift out	SUB	substitute
ETX	end of text	SI	shift in	ESC	escape
EOT	end of transmission	DLE	data link escape	FS	file separator
ENQ	enquiry	DC1	device control 1	GS	group separator
ACK	acknowledge	DC2	device control 2	RS	record separator
BEL	bell	DC3	device control 3	US	unit separator
BS	backspace	DC4	device control 4	SP	space
HT	horizontal tabulation	NAK	negative acknowledge	DEL	delete
LF	linefeed	SYN	synchronous idle		
VT	vertical tabulation	ETB	end of transmission block		

APPENDIX E
SCHEMATICS

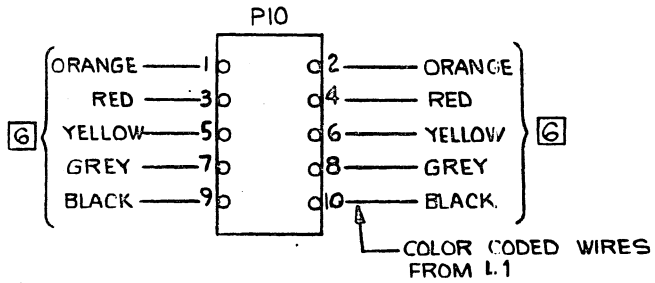
This section contains board assembly schematics and logic diagrams. Parts for TeleVideo systems are available from TeleVideo distributors.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B	INCORP. PER ECO 0676	2/9/89	
	B1	RECORD CHG PER ECO 0684	2/14/89	
	B2	" " " " 0692	3/31/89	
	B3	" " " " 0819	11/5/89	
	B4	" " " " 0837	4/5/90	
	B5	" " " " 0842	4/19/90	
	C	INCORP. PER ECO 0872	4/5/91	



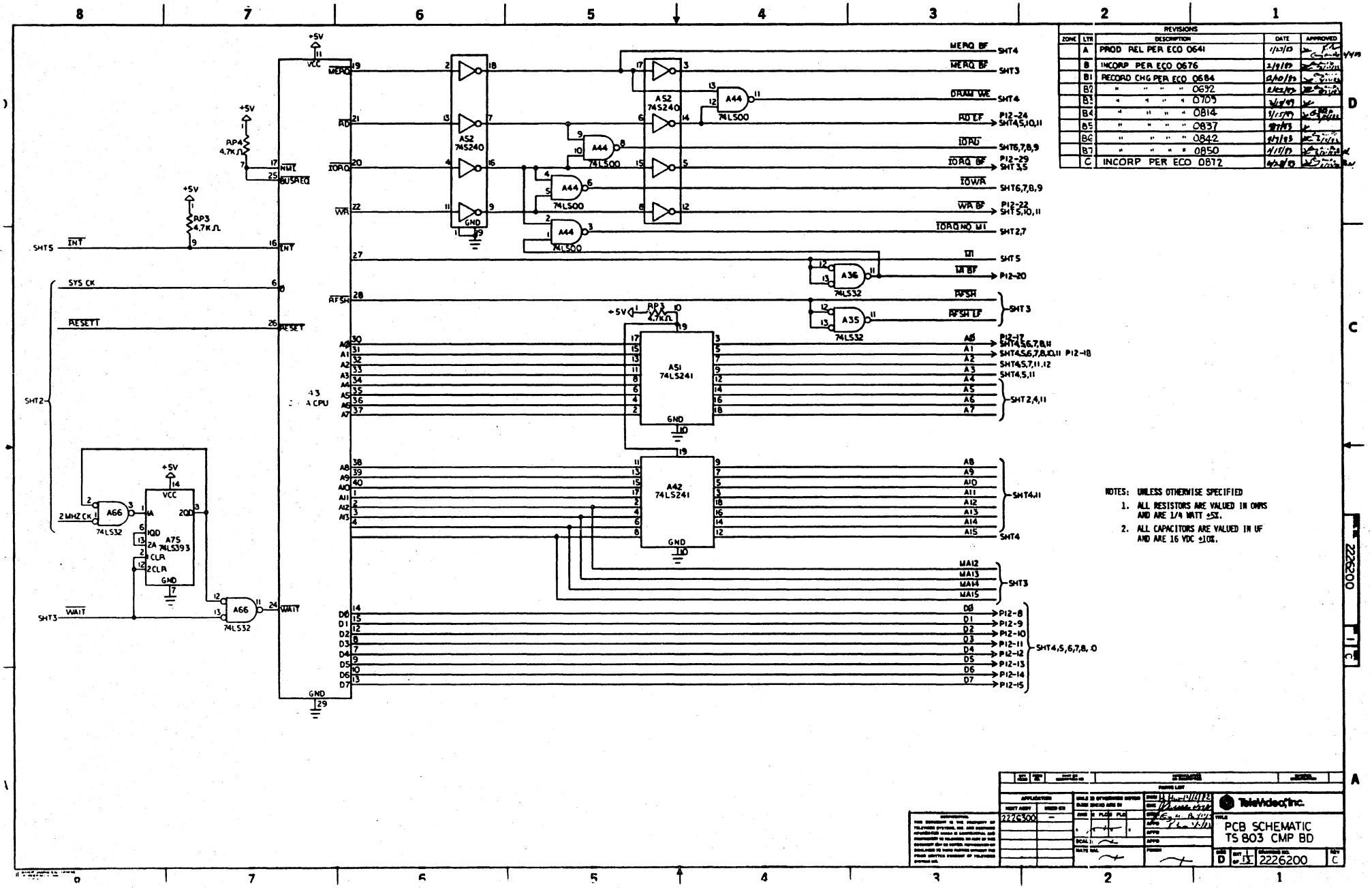
NOTES: UNLESS OTHERWISE SPECIFIED

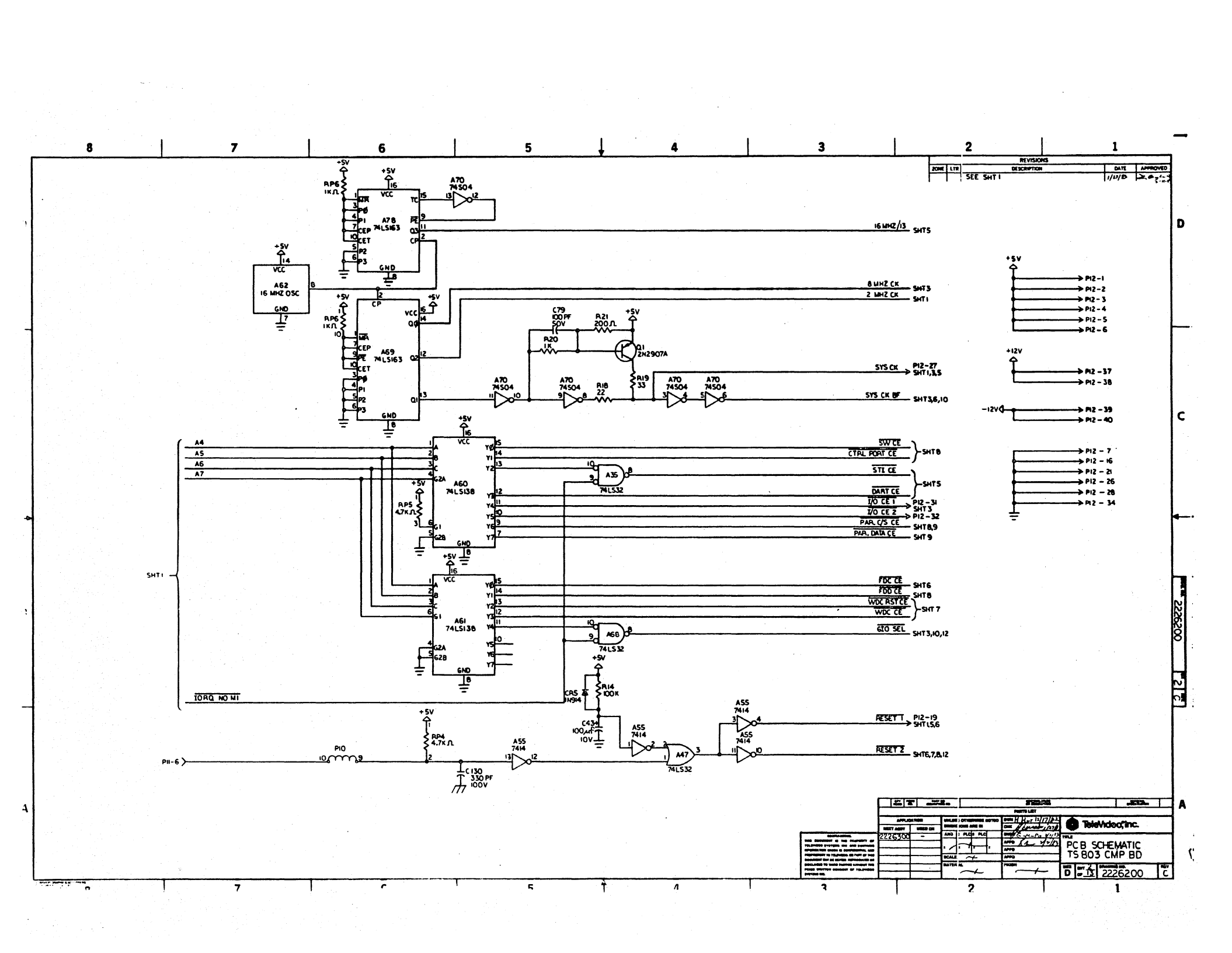
1. COMPLETE HEIGHT NOT TO EXCEED .50 ABOVE MOUNTING SURFACE OF BOARD.
2. SILKSCREEN DASH NUMBER & REV LEVEL WITH NON-CONDUCTIVE WHITE INK 50-100R APPROXIMATELY WHERE SHOWN.
3. MADE FROM 2226100 FAB REV B.
4. ALL COMPONENT HOLES NOT TO BE PLUGGED BY SOLDER AFTER FLOW SOLDERING. (FEED THRU'S ARE PLUGGED UNLESS SPECIFIED)
5. 2 PIN JUMPERS ON E10 B TO C.
6. COLOR CAN BE IN ANY ORDER BUT MUST BE IN PAIRS.



DETAIL A
(SCALE NONE)

APPLICATION		TeleVideo Inc.
NEXT ASSY 2246700	USED ON —	TITLE PCB ASSY DWG TS 803 CMP BD
		SIZE D DWG NO 2226300 REV C
		SHEET 1 OF 1


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A PROD REL PER ECO 0641 1/23/80
B INCORP PER ECO 0676 2/19/80
B1 RECORD CHG PER ECO 0684 3/10/80
B2 " " " 0692 3/27/80
B3 " " " 0705 4/28/80
B4 " " " 0814 7/15/80
B5 " " " 0837 8/7/80
B6 " " " 0842 8/7/80
B7 " " " 0850 9/15/80
C INCORP PER ECO 0872 9/28/80
+5V
RP4 4.7K
RP3 4.7K
INT
SYS CK
RESETT
SHT2
SHT5
SHT3
2 MHZ CK
WAIT
A66
74LS32
A75
74LS393
VCC
GND
MERQ
RD
IORQ
WR
BUSAEO
WAIT
A CPU
AFSH
A52 74S240
A44 74LS00
A36 74LS32
A35 74LS32
A51 74LS241
A42 74LS241
MERQ BF
DRAM WE
RD EF
IORQ
IORQ BF
IOWR
WR BF
IOAQ MQ WT
M1
M1 BF
RFSH
RFSH EF
A0 A1 A2 A3 A4 A5 A6 A7
A8 A9 A10 A11 A12 A13 A14 A15
MA12 MA13 MA14 MA15
D0 D1 D2 D3 D4 D5 D6 D7
PI2-8 PI2-9 PI2-10 PI2-11 PI2-12 PI2-13 PI2-14 PI2-15
PI2-24 PI2-29 PI2-22 PI2-20 PI2-17 PI2-18
SHT4 SHT3 SHT6,7,8,9 SHT3,5 SHT4,5,10,11 SHT2,7 SHT5 SHT4,5,6,7,8,11 SHT4,5,7,11,12 SHT2,4,11 SHT4,11 SHT4,5,6,7,8,10
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE VALUED IN OHMS AND ARE 1/4 WATT ±5%.
2. ALL CAPACITORS ARE VALUED IN UF AND ARE 16 VDC ±10%.
2226200
TeleVideo, Inc.
PCB SCHEMATIC
TS 803 CMP BD
2226200
D
C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SEE SHT 1 | 11/27/85
A78 74LS163
A69 74LS163
A62 16 MHZ OSC
A70 74S04
A60 74LS138
A61 74LS138
A35 74LS32
A68 74LS32
A47 74LS32
A55 7414
16 MHZ/13 SHT5
8 MHZ CK SHT3
2 MHZ CK SHT1
SYS CK P12-27 SHT1,3,5
SYS CK BF SHT3,6,10
SW CE
CTAL PORT CE
STI CE
DART CE
I/O CE 1 P12-31 SHT3
I/O CE 2 P12-32
PAR. C/S CE SHT8,9
PAR. DATA CE SHT 9
FDC CE SHT6
FDD CE SHT8
WDC RST CE
WDC CE SHT 7
GIO SEL SHT3,10,12
IORQ NO MI
RESET 1 P12-19 SHT1,5,6
RESET 2 SHT6,7,8,12
P12-1
P12-2
P12-3
P12-4
P12-5
P12-6
P12-37
P12-38
P12-39
P12-40
P12-7
P12-16
P12-21
P12-26
P12-28
P12-34
TeleVideo, Inc.
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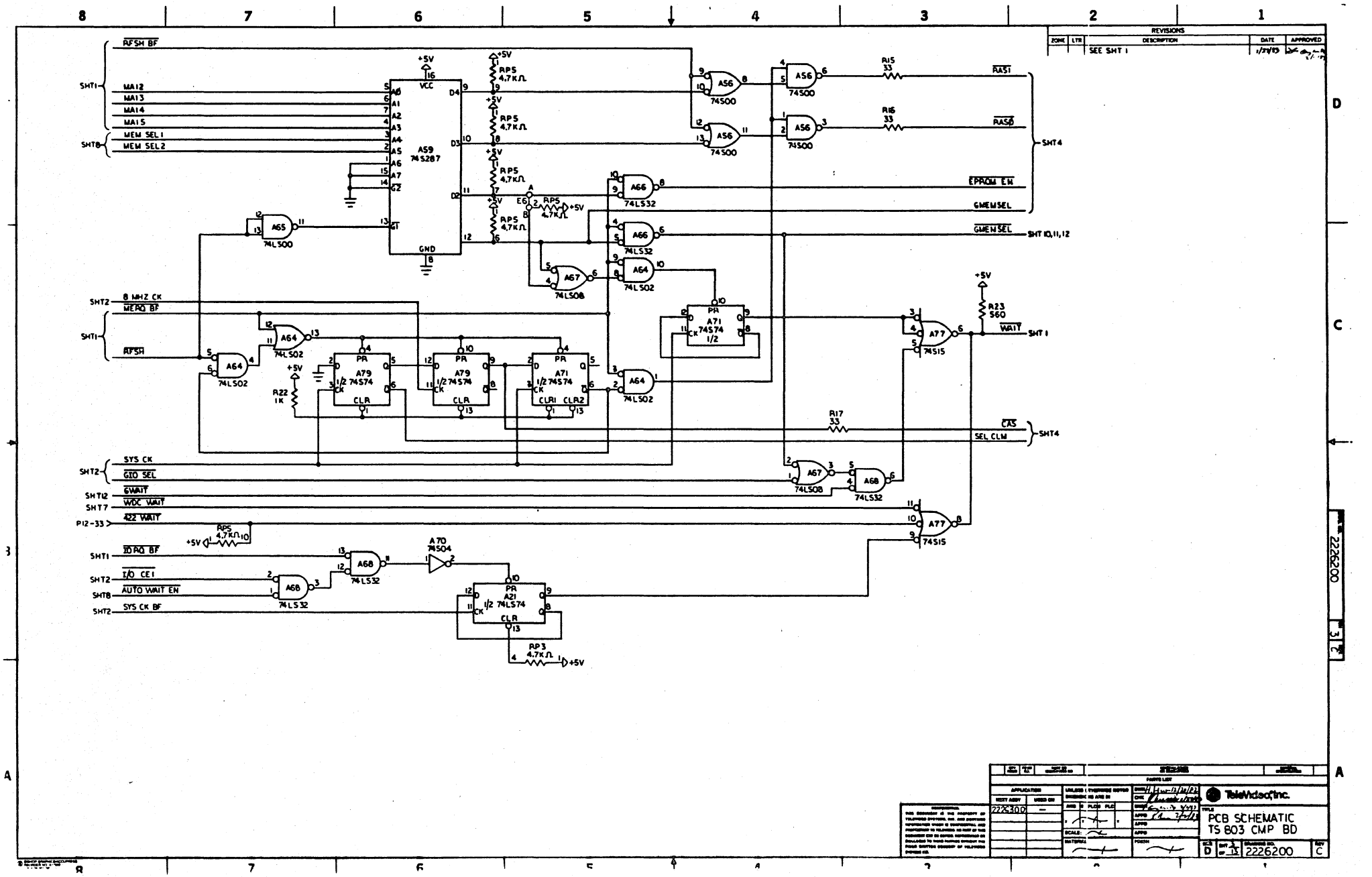
TS 803 CMP BD
2226200
D
C
A



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		SEE SHT 1	1/29/85	

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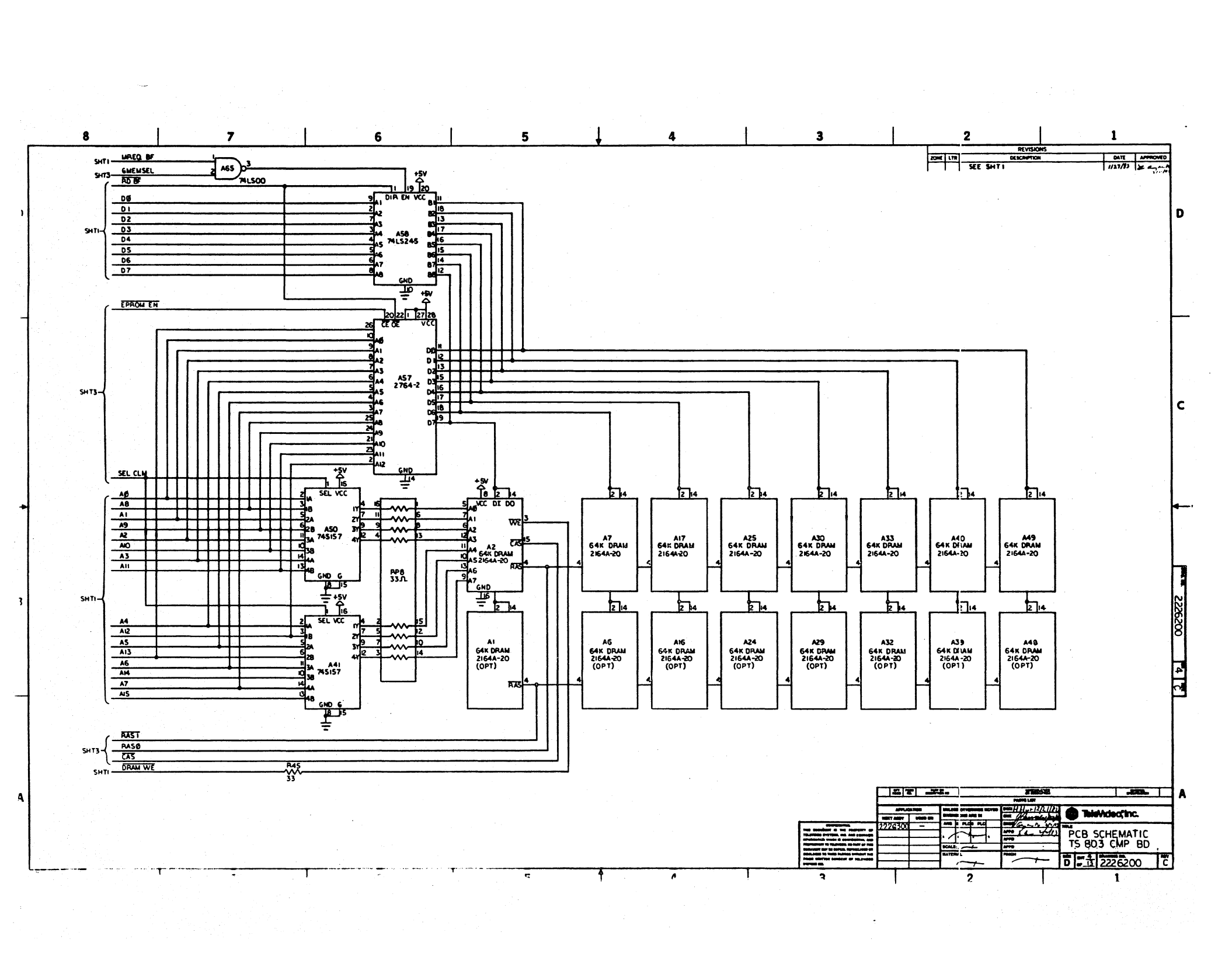
TS 803 CMP BD

2226200 REV C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MREQ BF
GMEMSEL
AD BF
A65
74LS00
+5V
A58
74LS245
DIR EN VCC
GND
DB
D1
D2
D3
D4
D5
D6
D7
EPROM EN
A57
2764-2
CE OE VCC
SEL CLM
A50
74S157
SEL VCC
GND G
A41
74S157
RP8
33Ω
A2
64K DRAM
2164A-20
VCC DI DO
WE
CAS
RAS
GND
A1
64K DRAM
2164A-20
(OPT)
A7
64K DRAM
2164A-20
A17
64K DRAM
2164A-20
A25
64K DRAM
2164A-20
A30
64K DRAM
2164A-20
A33
64K DRAM
2164A-20
A40
64K DRAM
2164A-20
A49
64K DRAM
2164A-20
A6
64K DRAM
2164A-20
(OPT)
A16
64K DRAM
2164A-20
(OPT)
A24
64K DRAM
2164A-20
(OPT)
A29
64K DRAM
2164A-20
(OPT)
A32
64K DRAM
2164A-20
(OPT)
A39
64K DRAM
2164A-20
(OPT)
A48
64K DRAM
2164A-20
(OPT)
RAST
RAS0
CAS
DRAM WE
R45
33
SHT1
SHT3
TeleVideo Inc.
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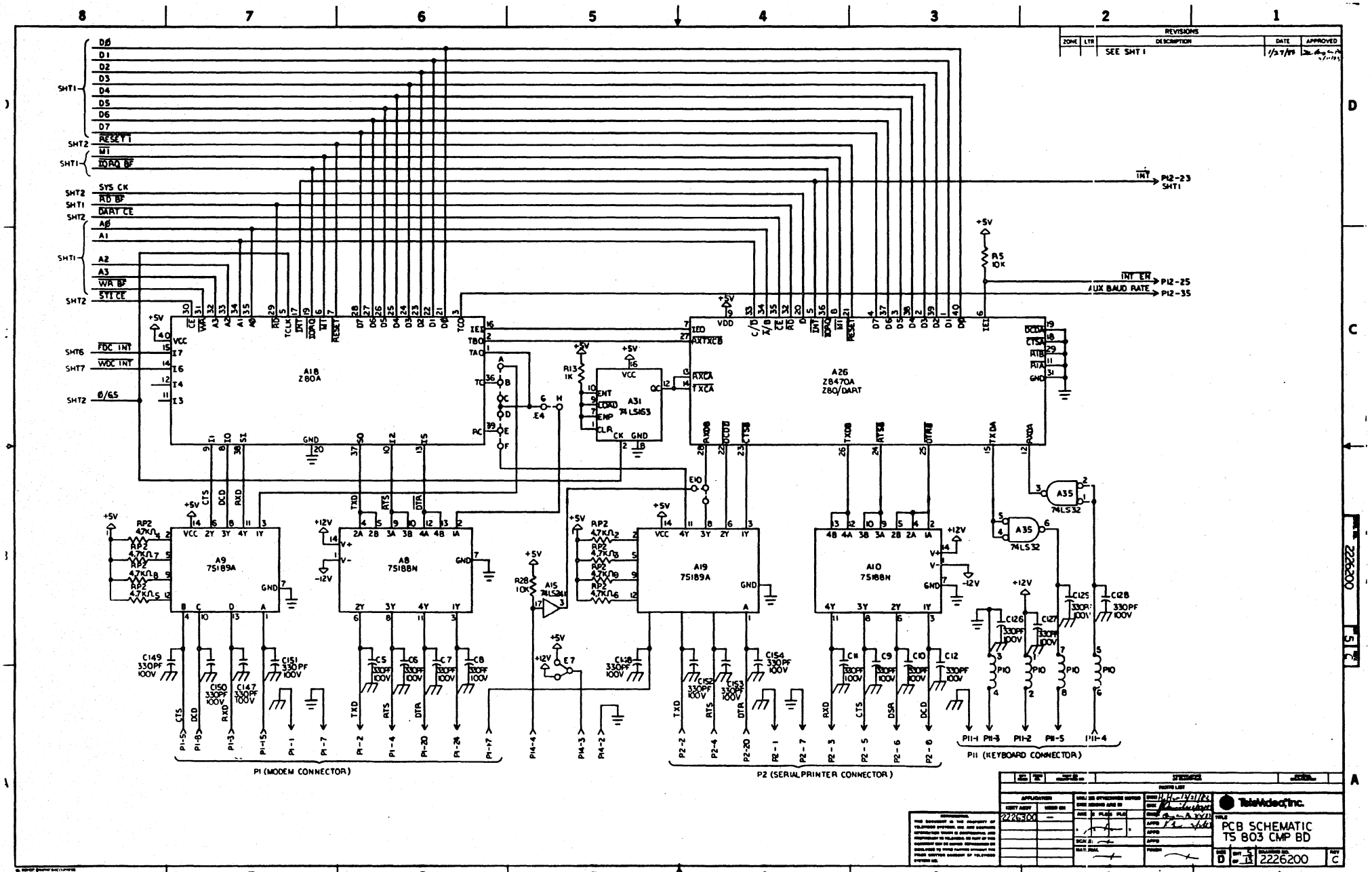
TS 803 CMP BD
2226200
D
C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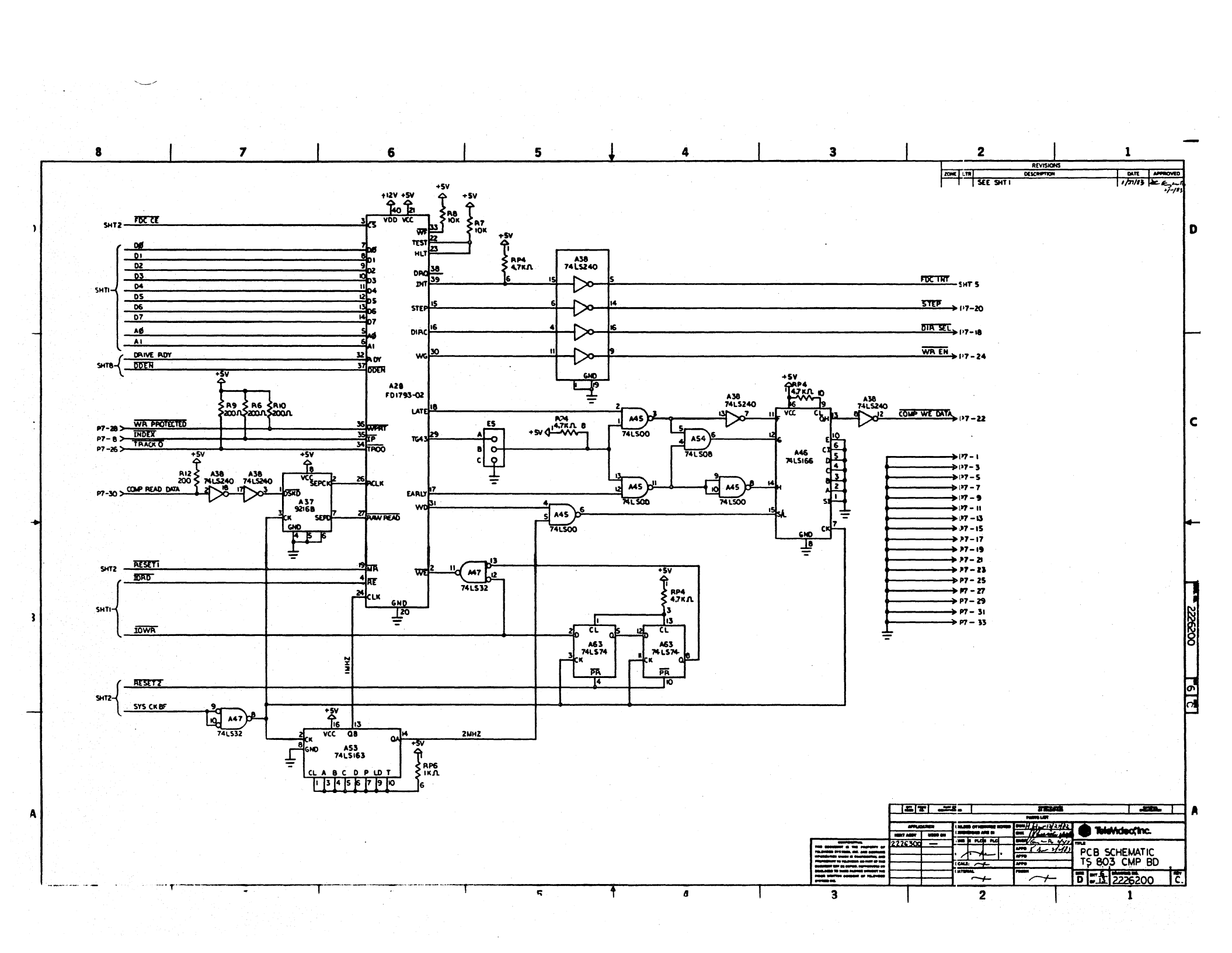
A18 Z80A
A26 Z8470A Z80/DART
A31 74LS163
A9 75189A
A8 75188N
A19 75189A
A10 75188N
A15 74LS241
A35 74LS32
P1 (MODEM CONNECTOR)
P2 (SERIAL/PRINTER CONNECTOR)
P11 (KEYBOARD CONNECTOR)
INT → P12-23 SHT1
INT EN → P12-25
AUX BAUD RATE → P12-35
TeleVideo, Inc.
PCB SCHEMATIC
TS 803 CMP BD
2226300
C


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
SEE SHT 1 1/21/83
FDC CE
DRIVE RDY
ODEN
WR PROTECTED
INDEX
TRACK 0
COMP READ DATA
RESET1
IORD
IOWR
RESET2
SYS CKBF
2MHZ
FDC INT
STEP
DIR SEL
WR EN
COMP WE DATA
A28 FD1793-02
A38 74LS240
A45 74LS00
A54 74LS08
A46 74LS166
A37 92168
A47 74LS32
A63 74LS74
A53 74LS163
RP4 4.7KΩ
RP6 1KΩ
R8 10K
R7 10K
R9 200Ω
R6 200Ω
R10 200Ω
R12 200
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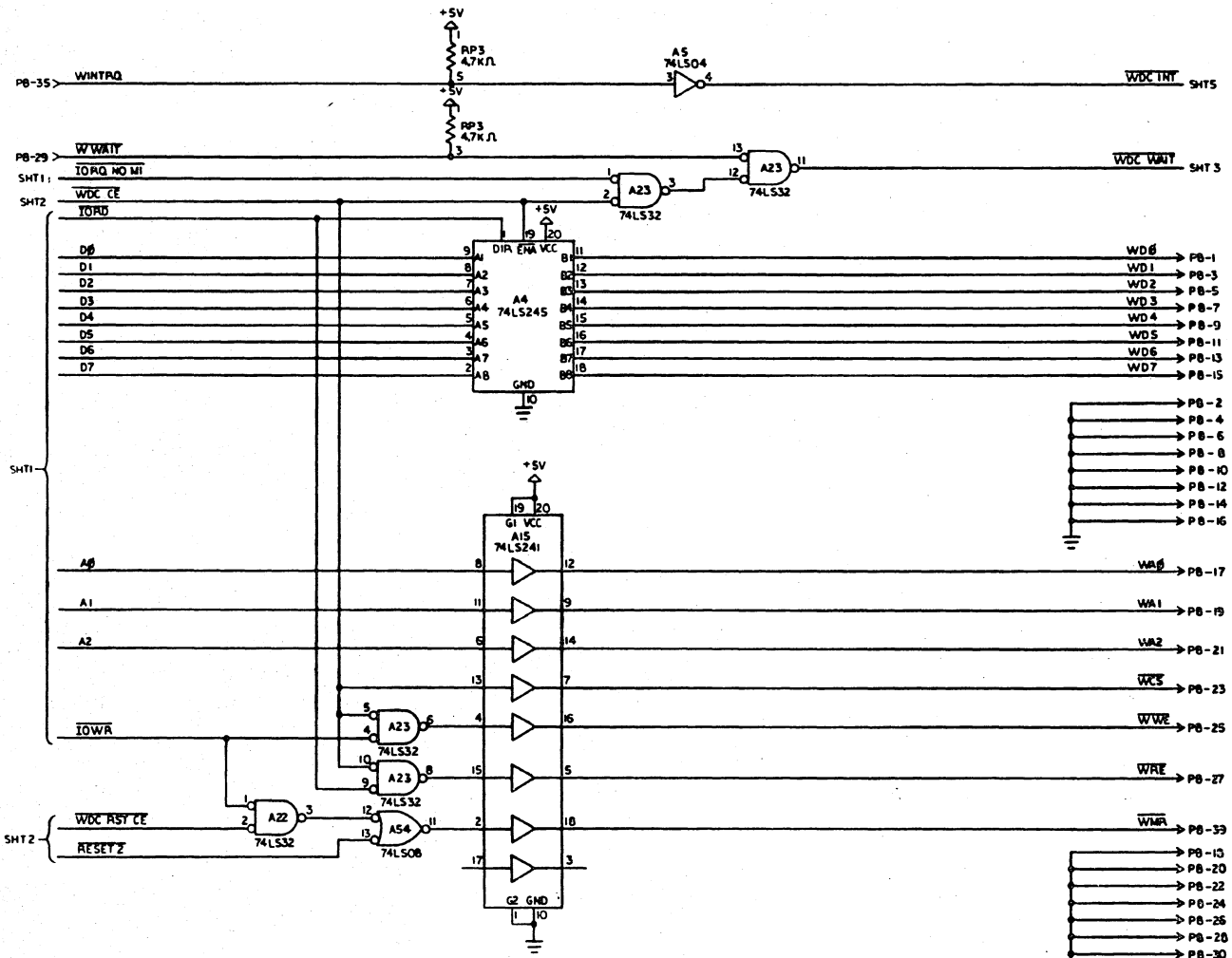
2226200



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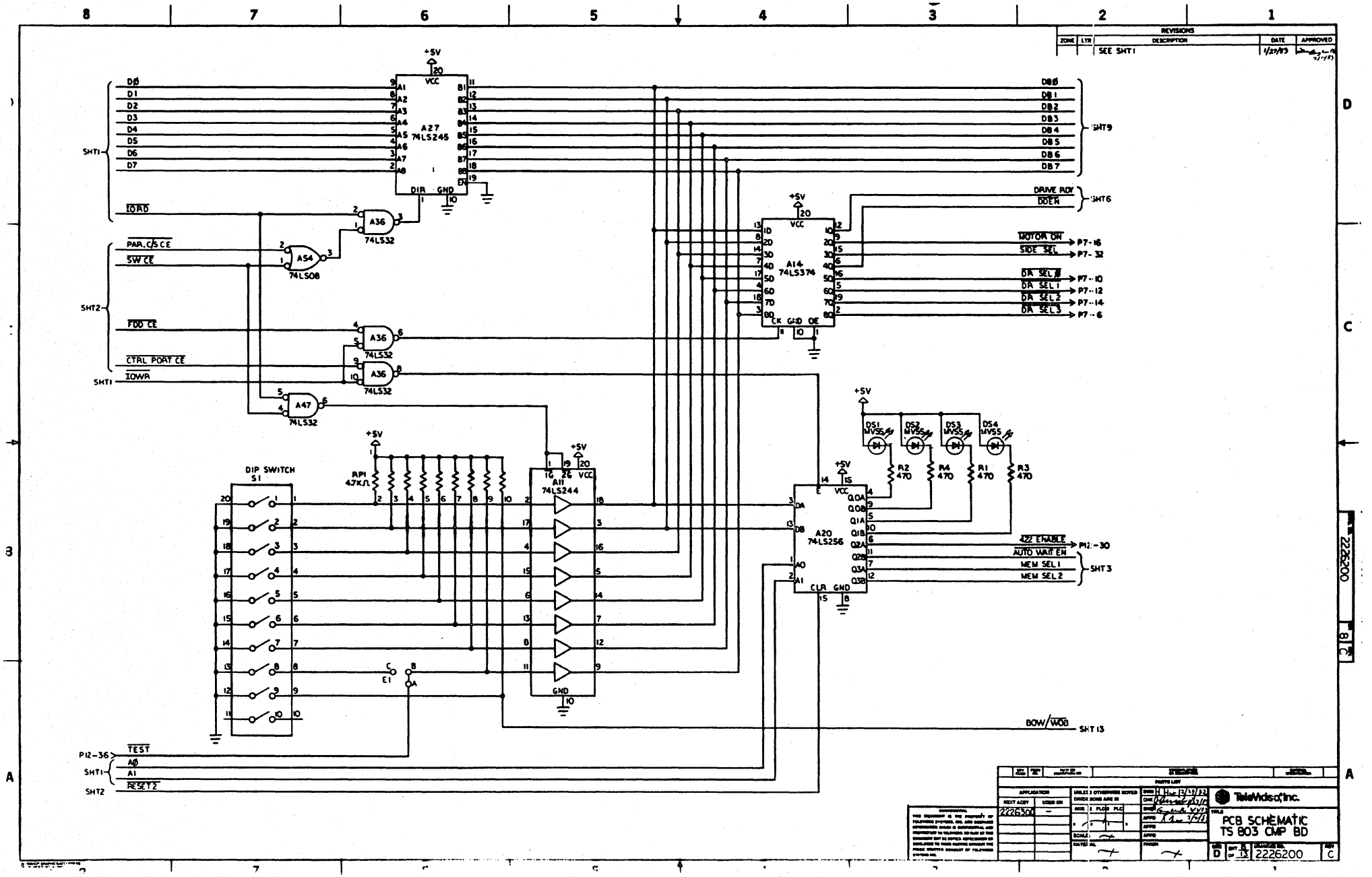
TeleVideo, Inc.

TITLE: PCB SCHEMATIC TS 803 CMP BD

SIZE D | SHT 1 OF 13 | DRAWING NO. 2226200 | REV C

2226200 1 OF 2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ZONE | LTR | DESCRIPTION | DATE | APPROVED
SEE SHT1 | 1/27/83
+5V
A27 74LS245
DIR GND
D0 D1 D2 D3 D4 D5 D6 D7
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
SHT9
IORD
PAR.C/S CE
SW CE
FDD CE
CTRL PORT CE
IOWR
SHT1
SHT2
A36 74LS32
A54 74LS08
A47 74LS32
A14 74LS374
CK GND OE
DRIVE RDY
DDEN
SHT6
MOTOR ON
SIDE SEL
DA SEL 0
DA SEL 1
DA SEL 2
DA SEL 3
P7-16
P7-32
P7-10
P7-12
P7-14
P7-6
DIP SWITCH S1
RP1 4.7K Ω
A11 74LS244
GND
E1
DS1 MVS5
DS2 MVS5
DS3 MVS5
DS4 MVS5
R1 470
R2 470
R3 470
R4 470
A20 74LS256
CLR GND
422 ENABLE
AUTO WAIT EN
MEM SEL 1
MEM SEL 2
P12-30
SHT3
BOW/WOB
SHT13
P12-36
TEST
A0
A1
RESET2
SHT1
SHT2
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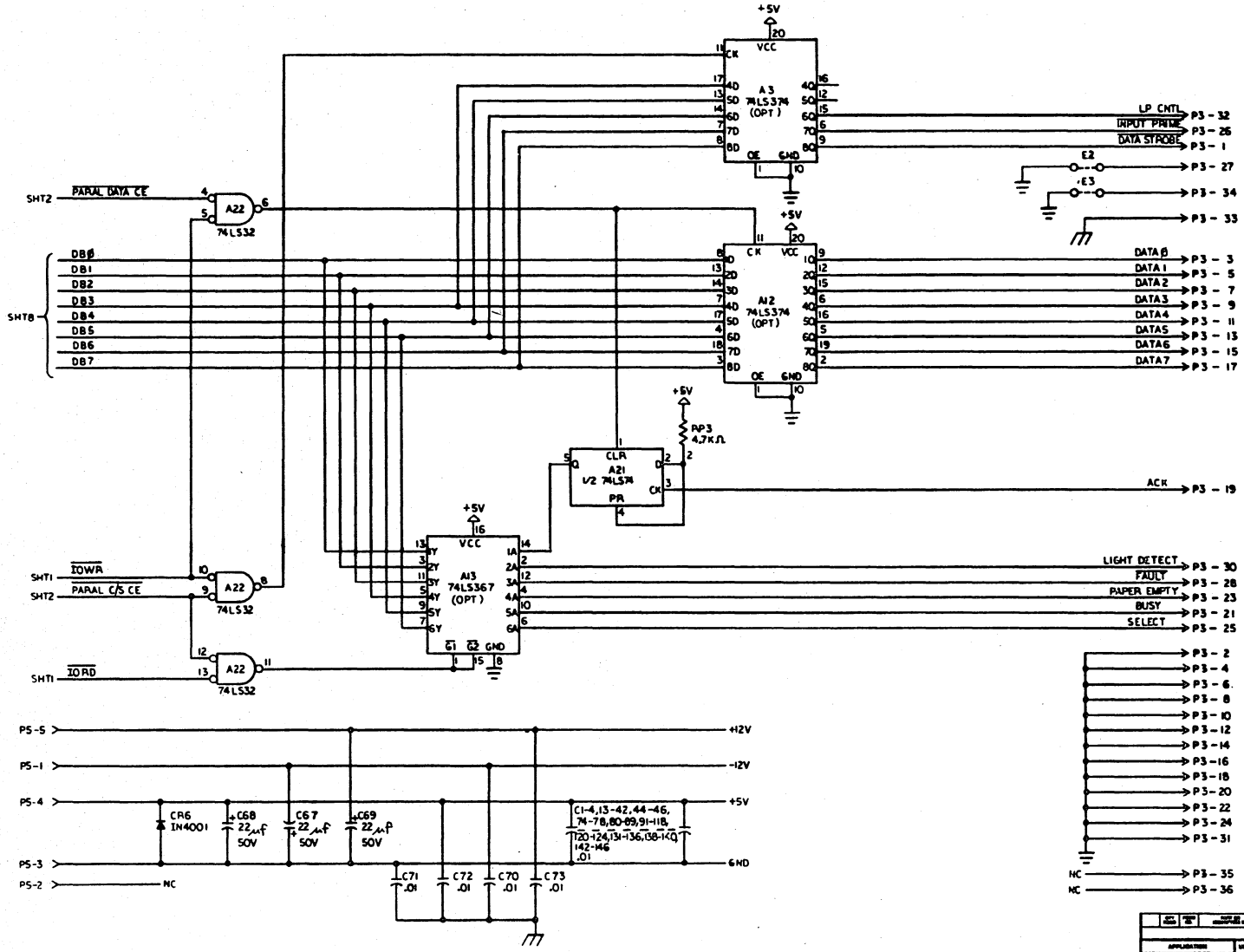
PCB SCHEMATIC
TS 803 CMP BD
2226200
C



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHT1	1/27/83	

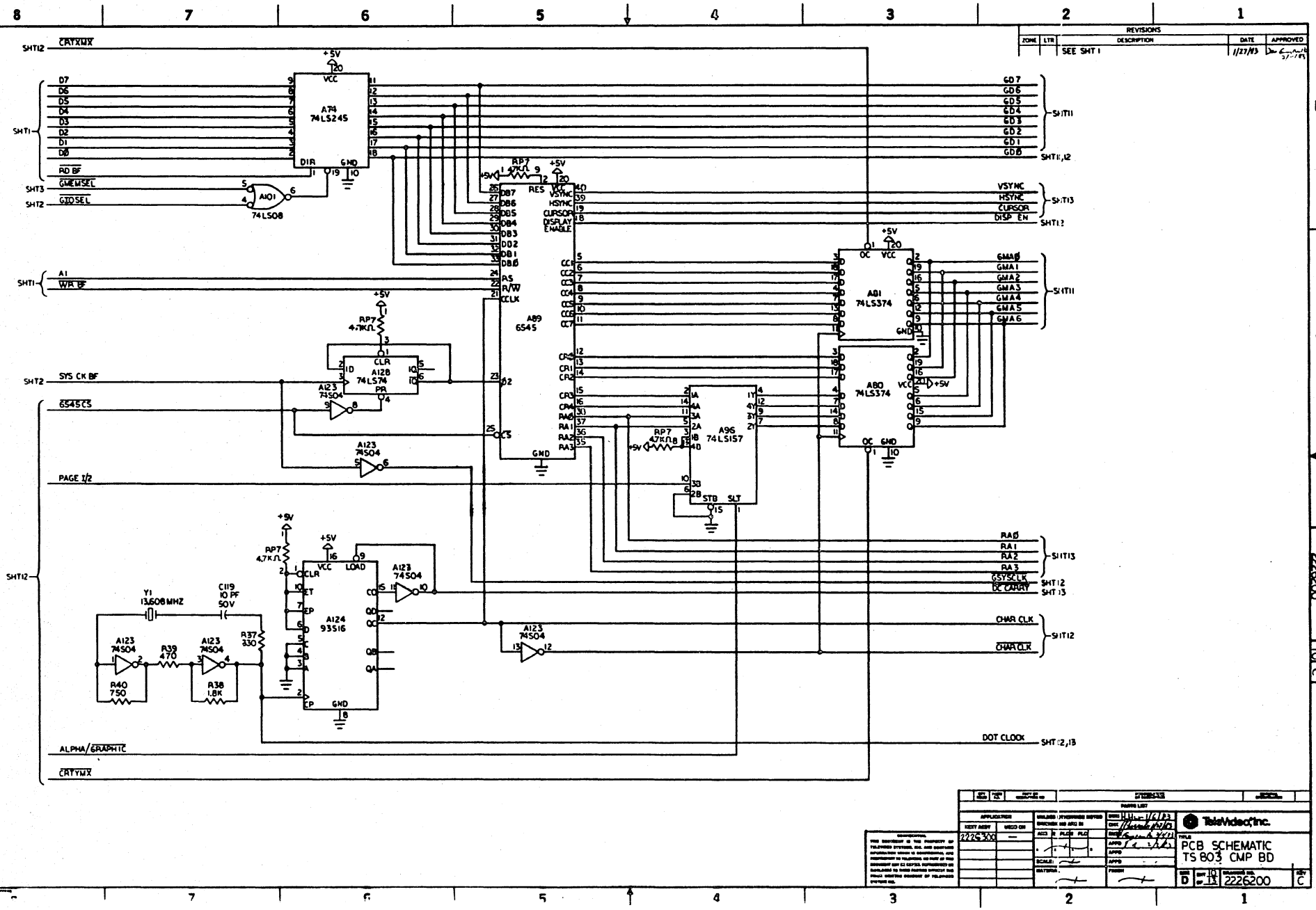
TeleVideo Inc.

PCB SCHEMATIC
TS 803 CMP BD

SIZE D | DWG NO 2226200 | REV C

SHT 9 OF 13

2226200


CRTXMX
A74 74LS245
AI01 74LS08
A89 6545
A128 74LS74
A123 74S04
A124 93S16
AB1 74LS374
AB0 74LS374
A95 74LS157
RP7 4.7KΩ
Y1 13.608 MHZ
C119 10 PF 50V
R37 330
R39 470
R40 750
R38 1.8K
PAGE 1/2
SYS CK BF
6545CS
ALPHA/GRAPHIC
CRTYMX
DOT CLOCK
CHAR CLK
CHAR CLR
GSYSCLK
DC CARRY
VSYNC
HSYNC
CURSOR
DISP EN
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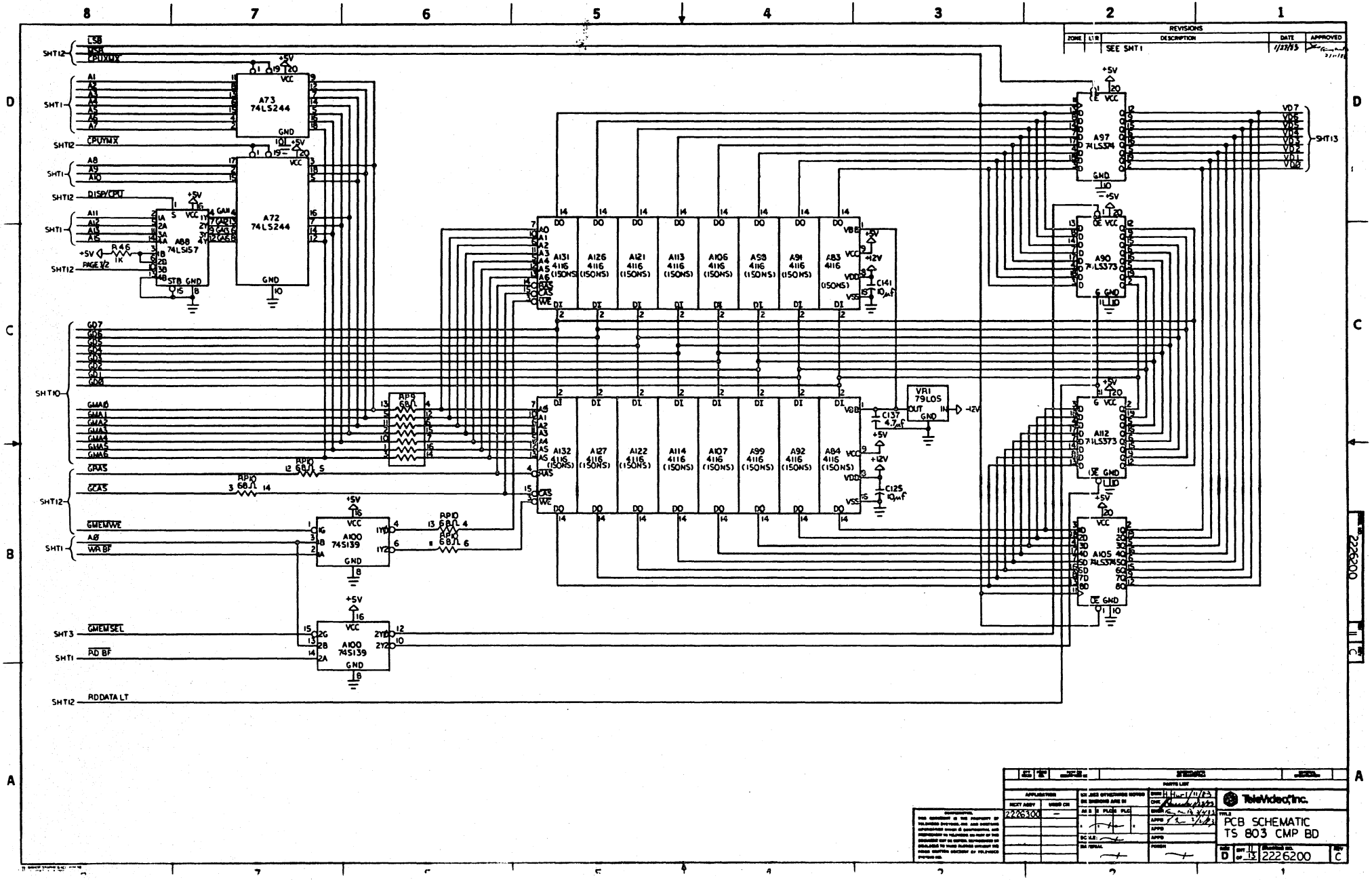
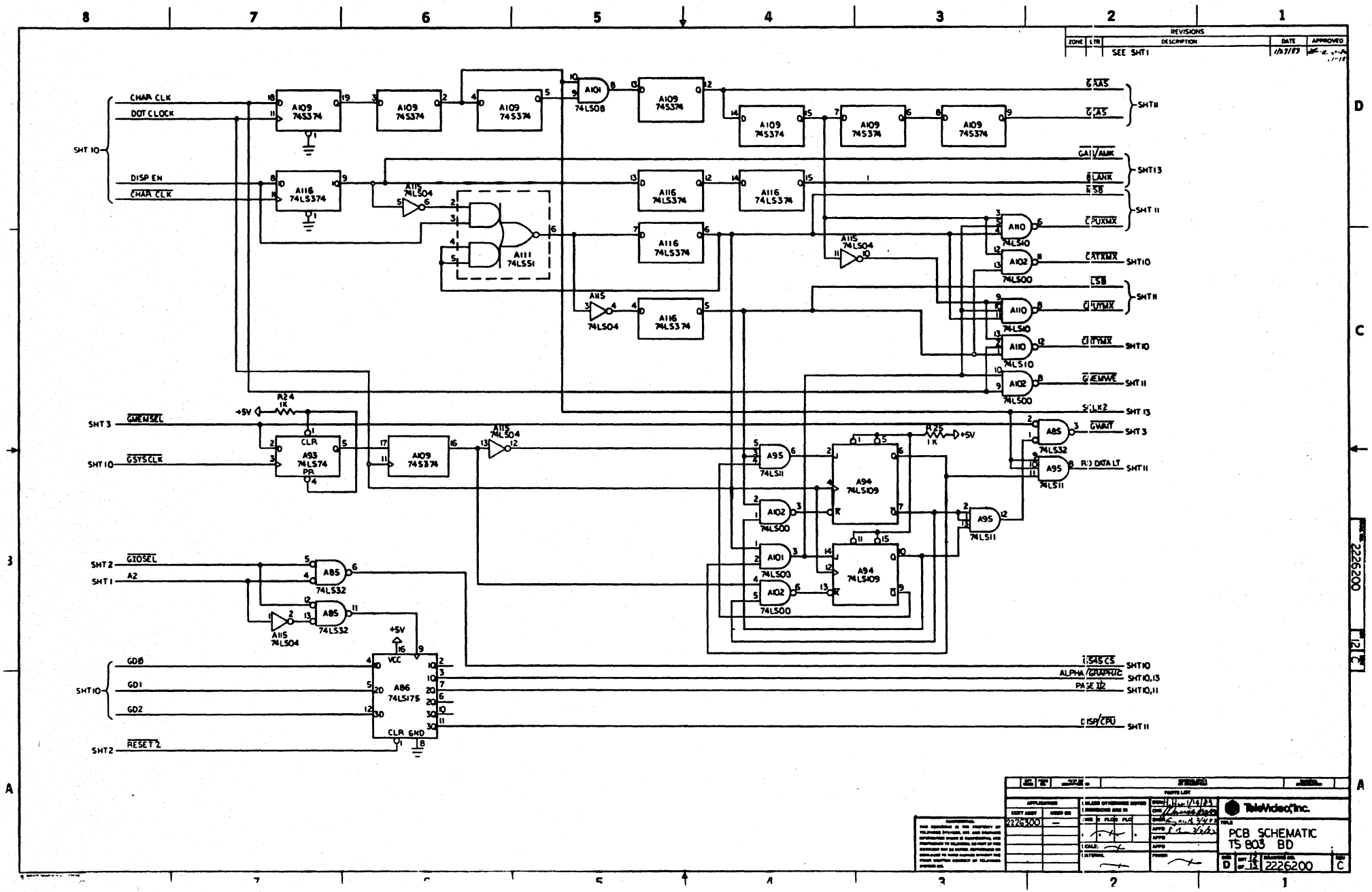
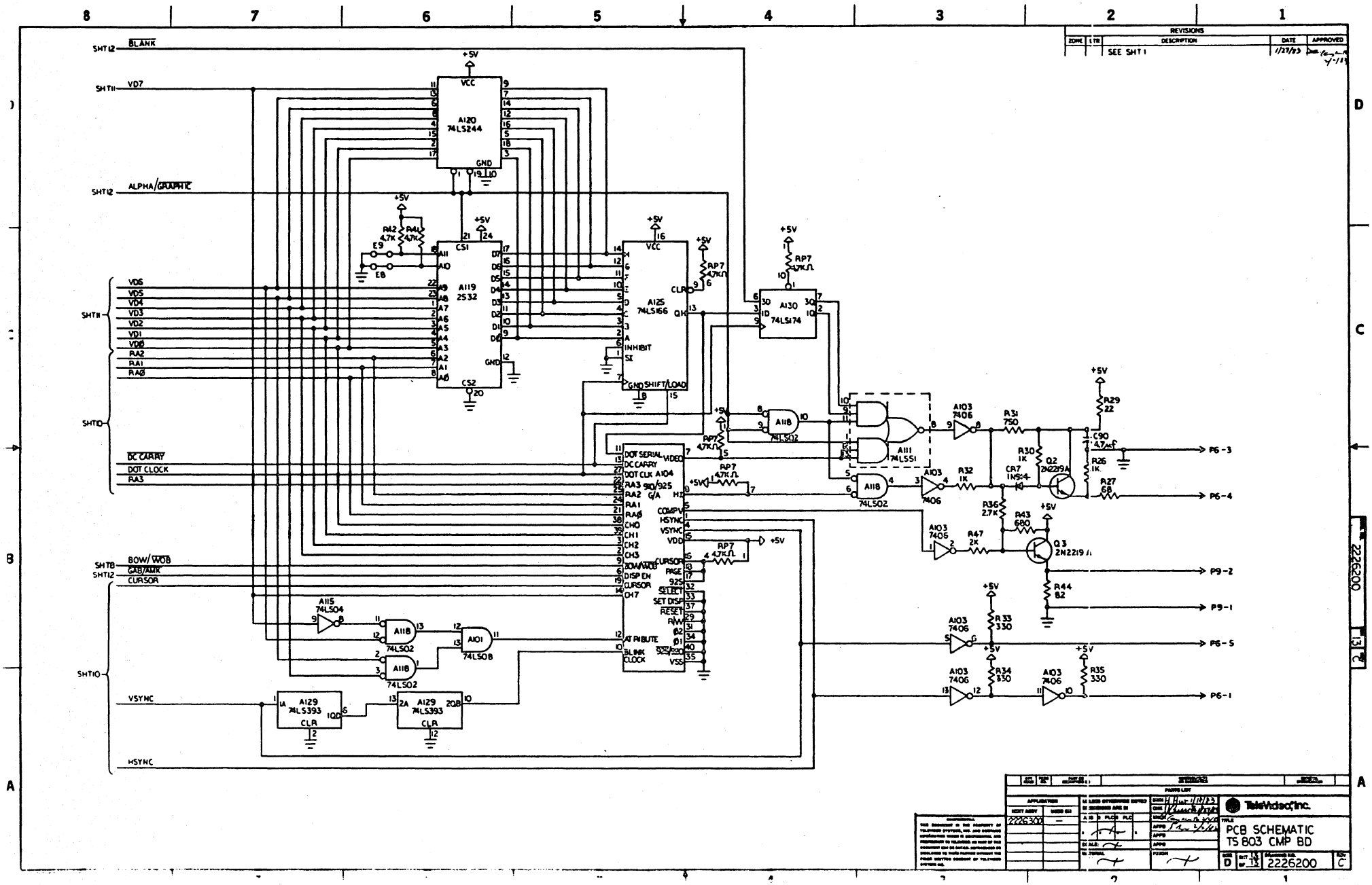
TS 803 CMP BD
2226200
REVISIONS
SEE SHT 1


REVISIONS
SEE SHT 1
A73 74LS244
A72 74LS244
A88 74LS157
A97 74LS374
A90 74LS373
A112 74LS373
A105 74LS374
A100 74S139
A131 4116 (150NS)
A126 4116 (150NS)
A121 4116 (150NS)
A113 4116 (150NS)
A106 4116 (150NS)
A98 4116 (150NS)
A91 4116 (150NS)
A83 4116 (150NS)
A132 4116 (150NS)
A127 4116 (150NS)
A122 4116 (150NS)
A114 4116 (150NS)
A107 4116 (150NS)
A99 4116 (150NS)
A92 4116 (150NS)
A84 4116 (150NS)
VR1 79L05
C137 4.7µF
C141 10µF
C125 10µF
R46 1K
RP8 68Ω
RP10 68Ω
RP9 68Ω
CPUYMX
DISP/CPU
PAGE 1/2
GMA0
GMA1
GMA2
GMA3
GMA4
GMA5
GMA6
GCAS
GRAS
GMEMWE
WR BF
GMEMSEL
RD BF
RDDATA LT
VD7
VD6
VD5
VD4
VD3
VD2
VD1
VD0
TeleVideo, Inc.
PCB SCHEMATIC
TS 803 CMP BD
2226200
2226100

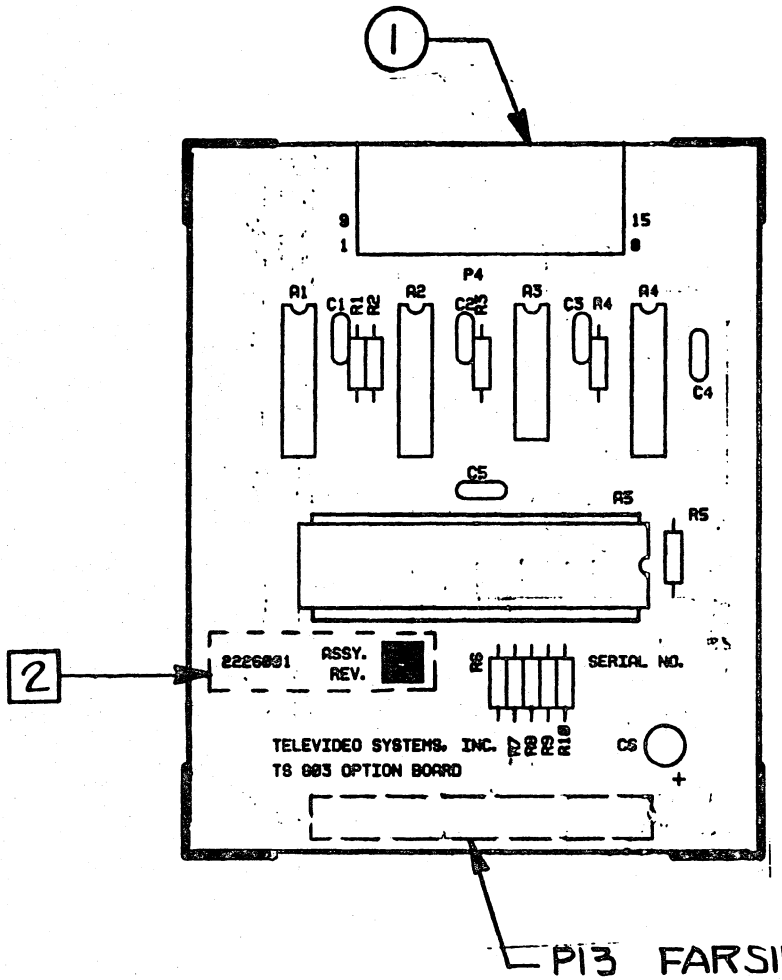


APPLICATIONS					TeleVideo, Inc.
NEXT ASSY	USED ON				
2276300	—				TITLE: PCB SCHEMATIC TS 803 BD
					SIZE: D — DOCUMENT NO.: 2226200 — REV: C
					SCALE: — SHT 12 OF 13

2226200
12
C


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
SEE SHT 1 | 1/27/83
SHT12 BLANK
SHT11 VD7
SHT12 ALPHA/GRAPHIC
SHT11 VD6 VD5 VD4 VD3 VD2 VD1 VD0 RA2 RA1 RA0
SHT10 DC CARRY DOT CLOCK RA3
SHT8 BOW/WOB
SHT12 GAB/AMR CURSOR
SHT10 VSYNC HSYNC
+5V
A120 74LS244
A119 2532
A125 74LS166
A130 74LS174
A111 74LS51
A118 74LS02
A103 7406
A115 74LS04
A101 74LS08
A129 74LS393
A104 8Y/925 G/A
P6-3
P6-4
P9-2
P9-1
P6-5
P6-1
TeleVideo Inc.
PCB SCHEMATIC
TS 803 CMP BD
2226200
D
C

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
ASSY	FIRST USED ON					
2252600	—	A	PROD REL	0684	2/9/84	



NOTE: UNLESS OTHERWISE SPECIFIED

1. COMPLETE HEIGHT NOT TO EXCEED .50 ABOVE MOUNTING SURFACE OF BOARD.
2. SILKSCREEN DASH NUMBER & REV LEVEL WITH NON-CONDUCTIVE WHITE INK 50-100R APPROXIMATELY WHERE SHOWN.
3. MADE FROM 2226101 FAB REV A.

MATERIAL

FINISH

REMOVE ALL BURRS AND SHARP EDGES

TOLERANCES UNLESS NOTED

DIMENSION | INCH | MM

X = ±

XX = ±

XXX = ±

ANGLES ±

CONTRACT NUMBER

DES.	H.H	1/27/84 DATE
DR.		DATE
CHK.		DATE 2/4/84
ENGR.		DATE 2/7/84

DESIGN ACTIVITY APPROVAL

CUSTOMER APPROVAL

SUPERSEDES

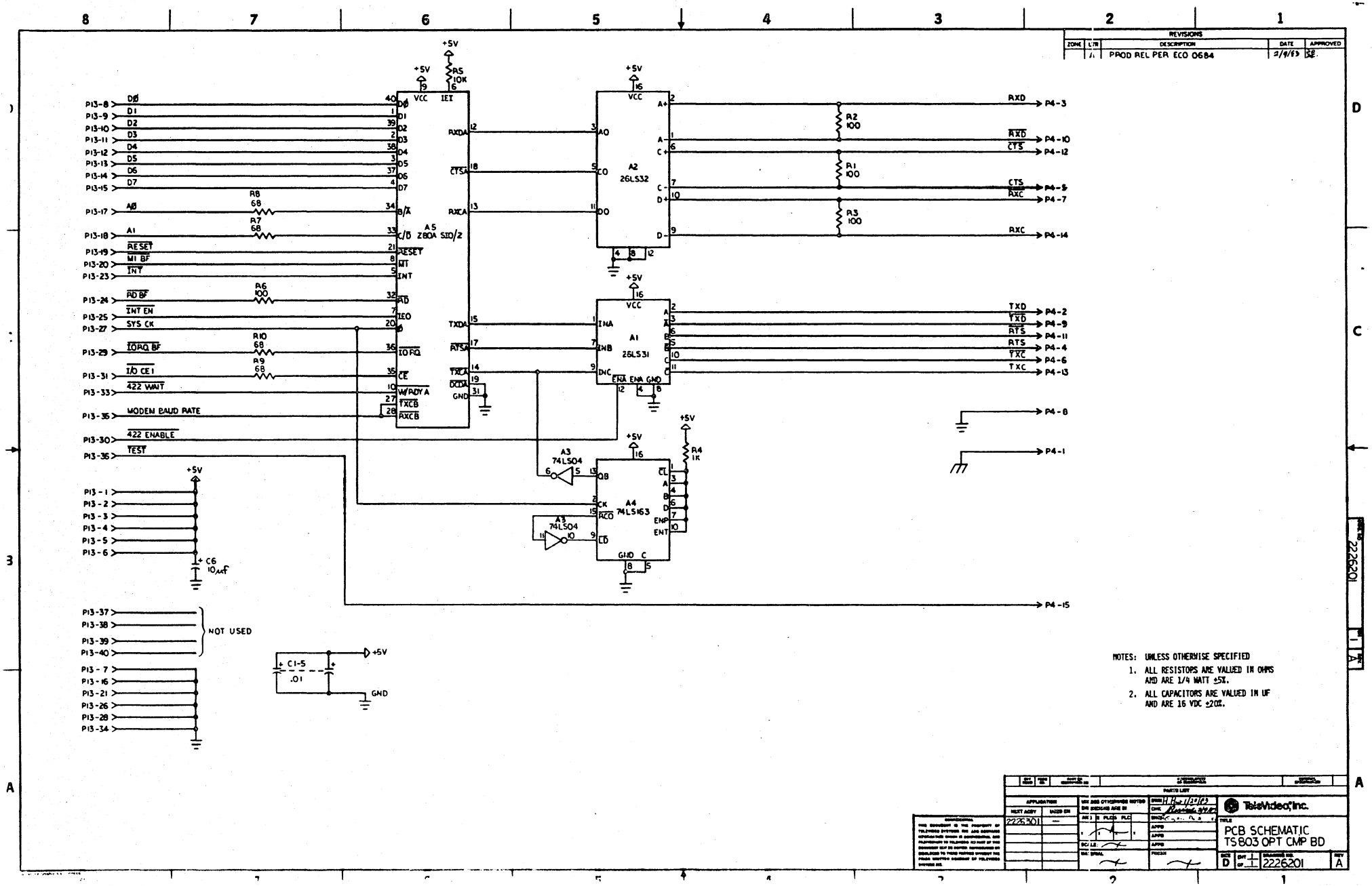
TeleVideo Systems, Inc.

PCB ASSY DWG
TS 803 OPT CMP BD

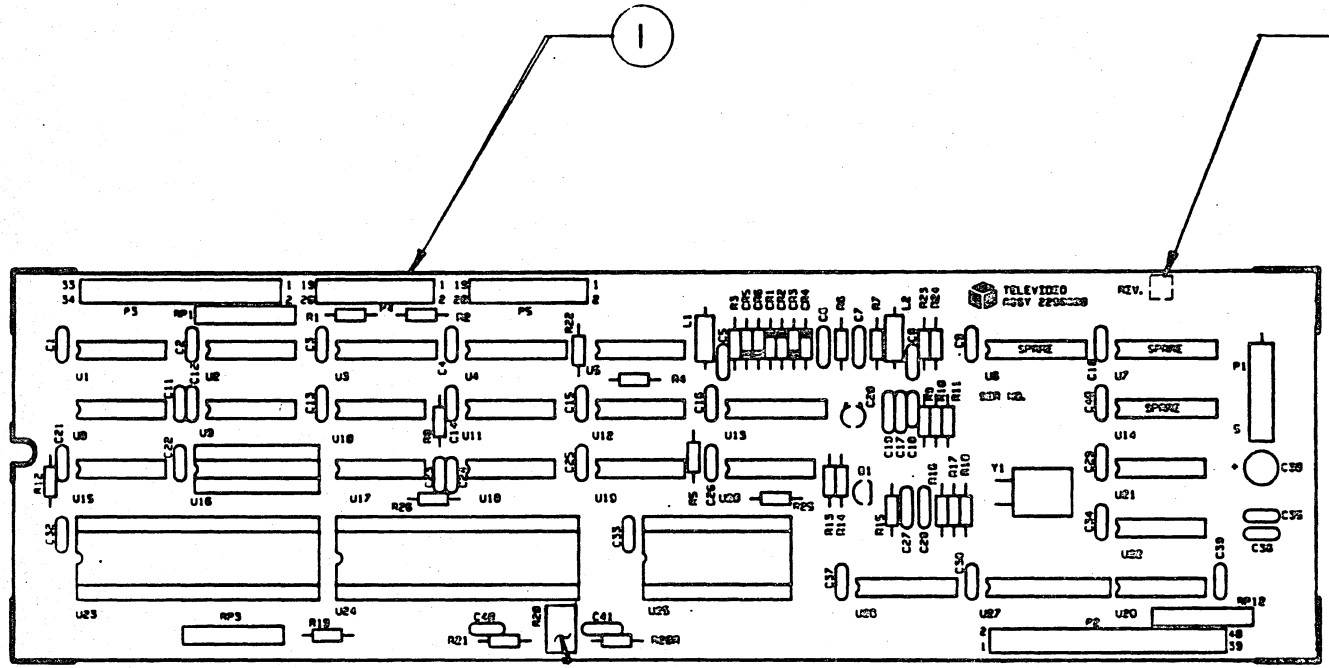
SIZE	CODE IDENT		REV
C		2226301	A

SCALE 1/1 SHEET 1 OF 1

2226301


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
PROD REL PER ECO 0684
P13-8 D0
P13-9 D1
P13-10 D2
P13-11 D3
P13-12 D4
P13-13 D5
P13-14 D6
P13-15 D7
P13-17 A0
P13-18 A1
P13-19 RESET
P13-20 WT BF
P13-23 INT
P13-24 RD BF
P13-25 INT EN
P13-27 SYS CK
P13-29 IORQ BF
P13-31 I/O CE1
P13-33 422 WAIT
P13-35 MODEM BAUD RATE
P13-30 422 ENABLE
P13-36 TEST
A5 Z80A SIO/2
A2 26LS32
A1 26LS31
A3 74LS04
A4 74LS163
R1 100
R2 100
R3 100
R4 1K
R5 10K
R6 100
R7 68
R8 68
R9 68
R10 68
C6 10uf
C1-5 .01
+5V
GND
NOT USED
RXD P4-3
RXD P4-10
CTS P4-12
CTS P4-5
RXC P4-7
RXC P4-14
TXD P4-2
TXD P4-9
RTS P4-11
RTS P4-4
TXC P4-6
TXC P4-13
P4-8
P4-1
P4-15
P13-1
P13-2
P13-3
P13-4
P13-5
P13-6
P13-37
P13-38
P13-39
P13-40
P13-7
P13-16
P13-21
P13-26
P13-28
P13-34
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE VALUED IN OHMS AND ARE 1/4 WATT ±5%.
2. ALL CAPACITORS ARE VALUED IN UF AND ARE 16 VDC ±20%.
TeleVideo, Inc.
PCB SCHEMATIC
TS803 OPT CMP BD
2226201
A

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	PROD REL PER ECO 0900	6/24/93	



NOTE: UNLESS OTHERWISE SPECIFIED

1. COMPLETE HEIGHT NOT TO EXCEED .50 ABOVE MOUNTING SURFACE OF BOARD.

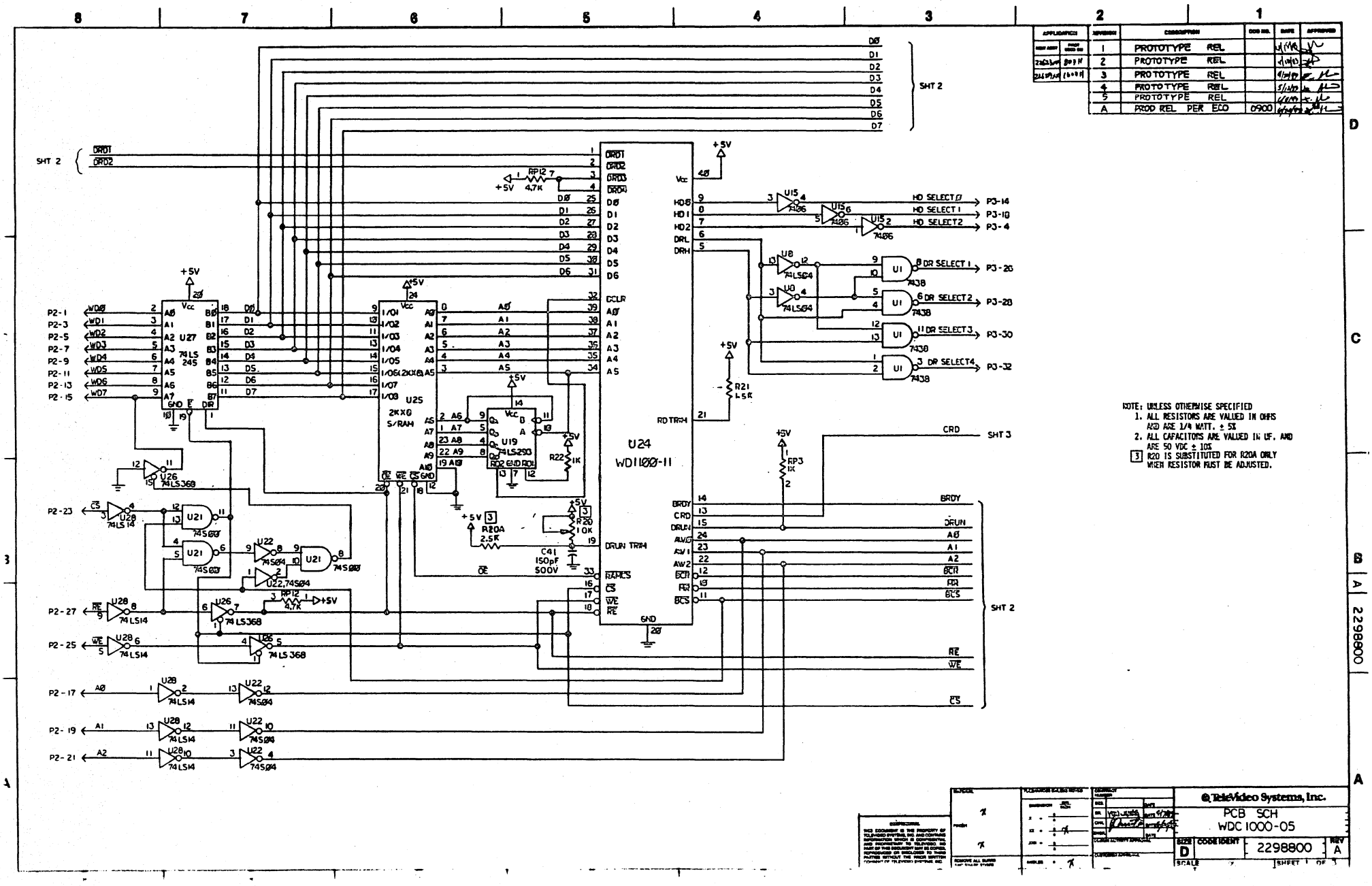
2. SILKSCREEN DASH NUMBER & REV LEVEL WITH NON-CONDUCTIVE WHITE INK (50-100R), APPROXIMATELY WHERE SHOWN.

3. MADE FROM 2298700 FAB REV A

4. DO NOT INSTALL R20. SEE SCH 2298800 NO 3.

		TeleVideo, Inc.	
		PCB ASY DWG WDC 1000-05	
		SIZE D	DRAWING NO. 2298900 REV A

2298900 F1A



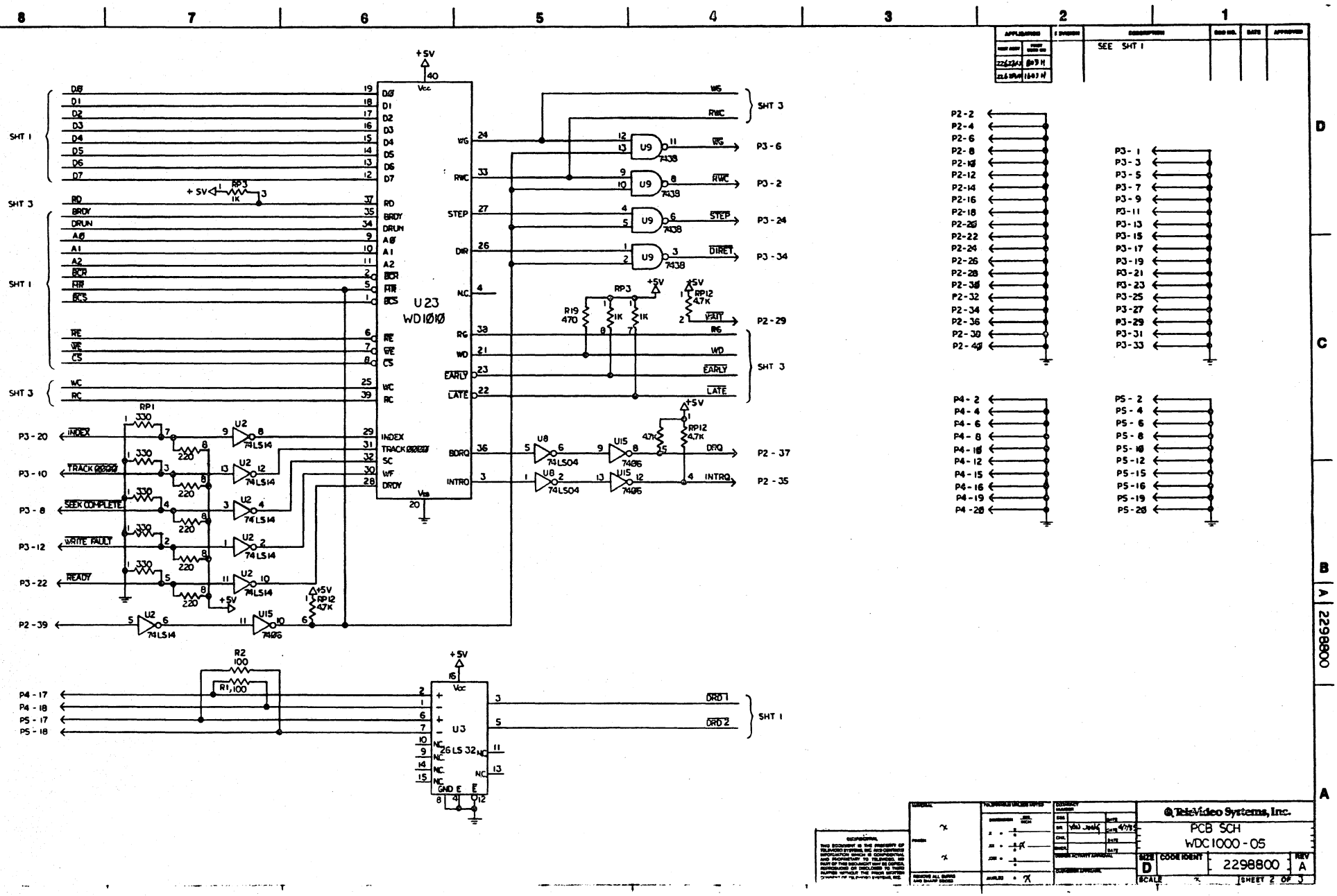
NOTE: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE VALUED IN OHMS AND ARE 1/4 WATT, ± 5%
2. ALL CAPACITORS ARE VALUED IN UF, AND ARE 50 VDC ± 10%
[3] R20 IS SUBSTITUTED FOR R20A ONLY WHEN RESISTOR MUST BE ADJUSTED.

APPLICATION	REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
	1	PROTOTYPE REL			
	2	PROTOTYPE REL			
	3	PROTOTYPE REL			
	4	PROTOTYPE REL			
	5	PROTOTYPE REL			
	A	PROD REL PER ECO	0900		

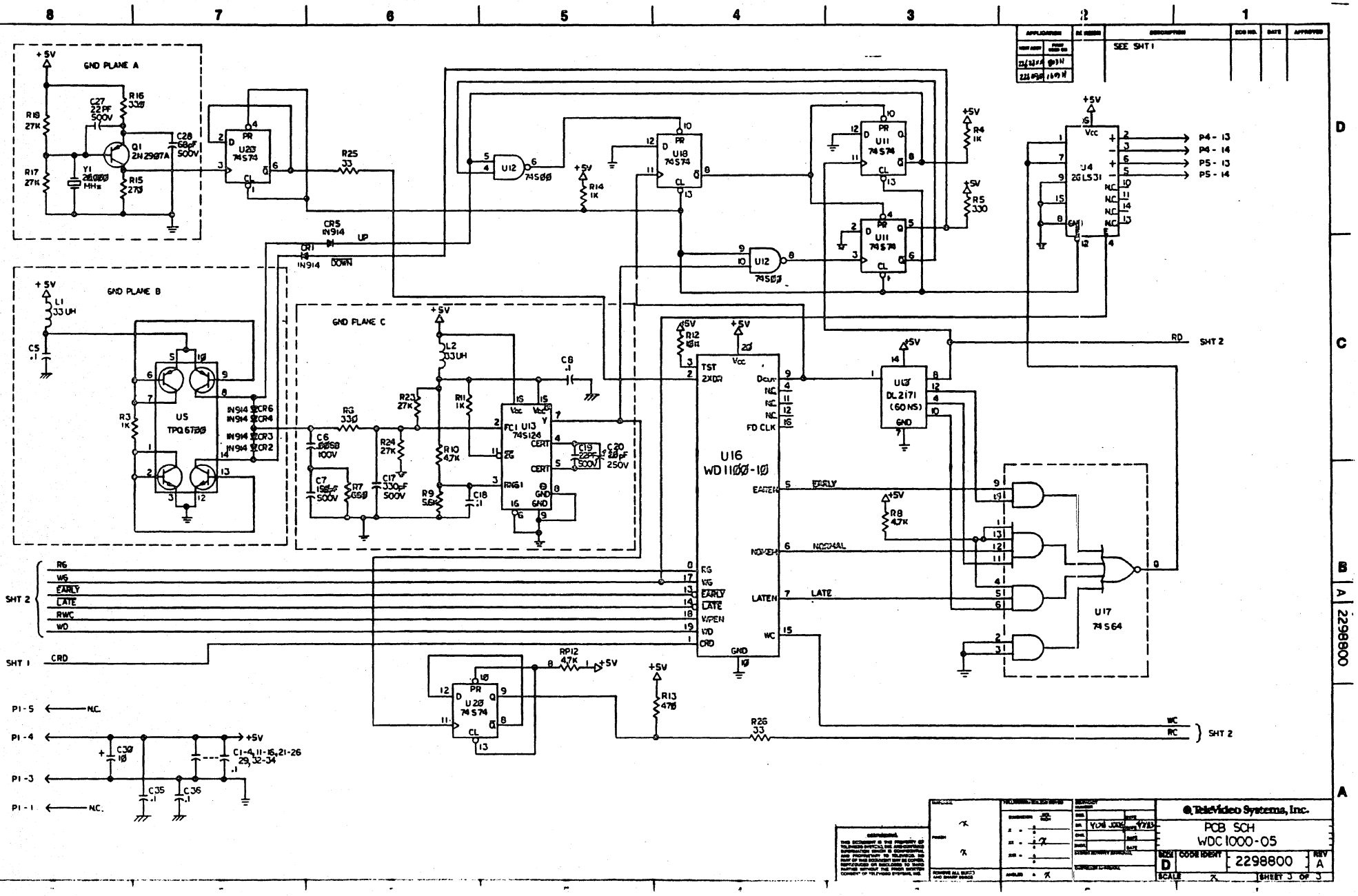
© TeleVideo Systems, Inc.

PCB SCH
WDC 1000-05

SIZE D | CODE IDENT | 2298800 | REV A
SCALE | SHEET 1 OF 3



© RisVideo Systems, Inc.
PCB SCH
WDC1000-05
SIZE D | CODE IDENT | 2298800 | REV A
SCALE | SHEET 2 OF 3



		SEE SHT 1			

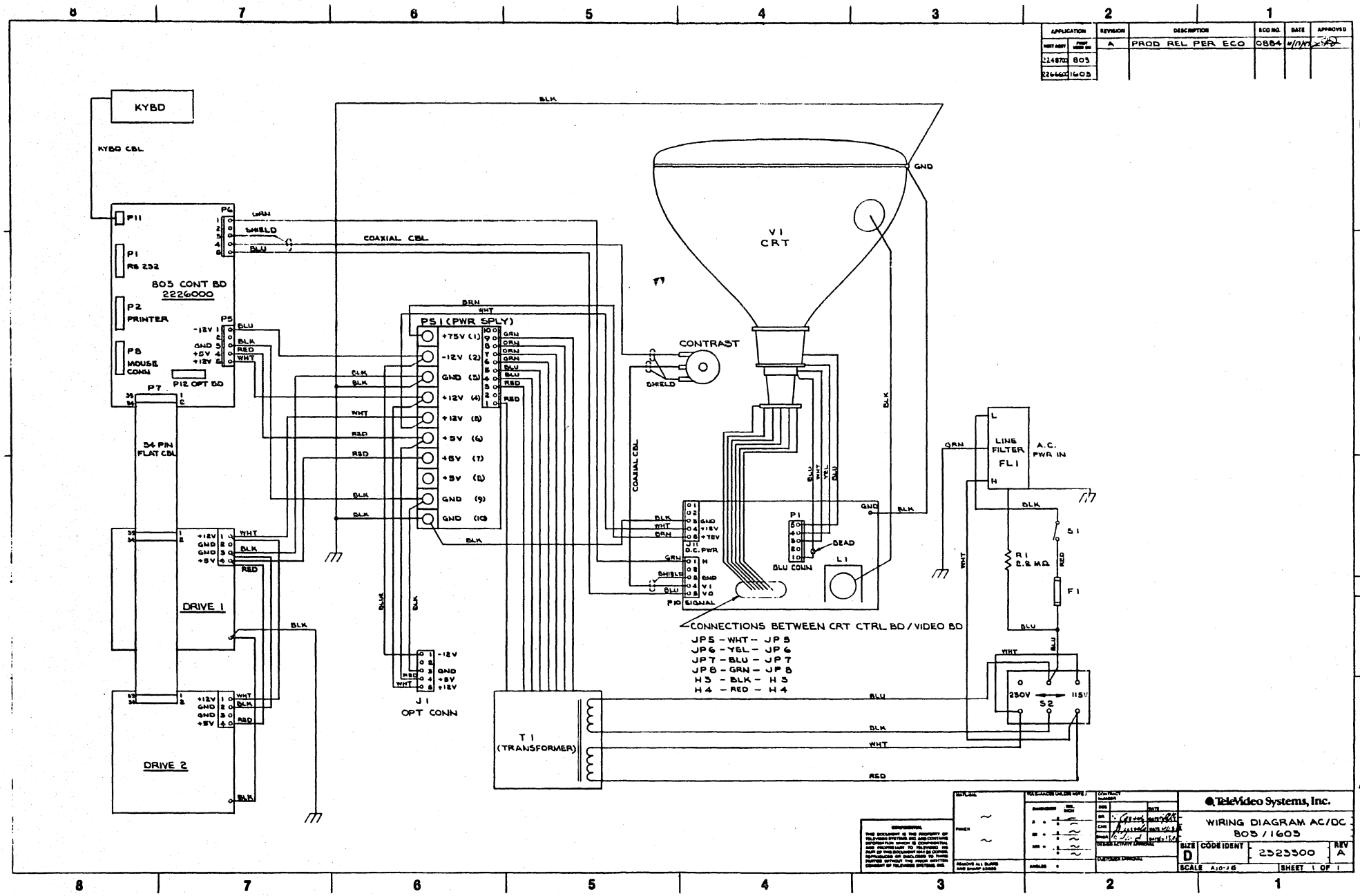
TeleVideo Systems, Inc.

PCB SCH
WDC 1000-05

SIZE D | CODE IDENT 2298800 | REV A

SCALE | SHEET 3 OF 3

2298800



APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	PRINT USED ON					
2248700	805	A	PROD REL PER ECO	0884	6/11/87	
2264600	1605					

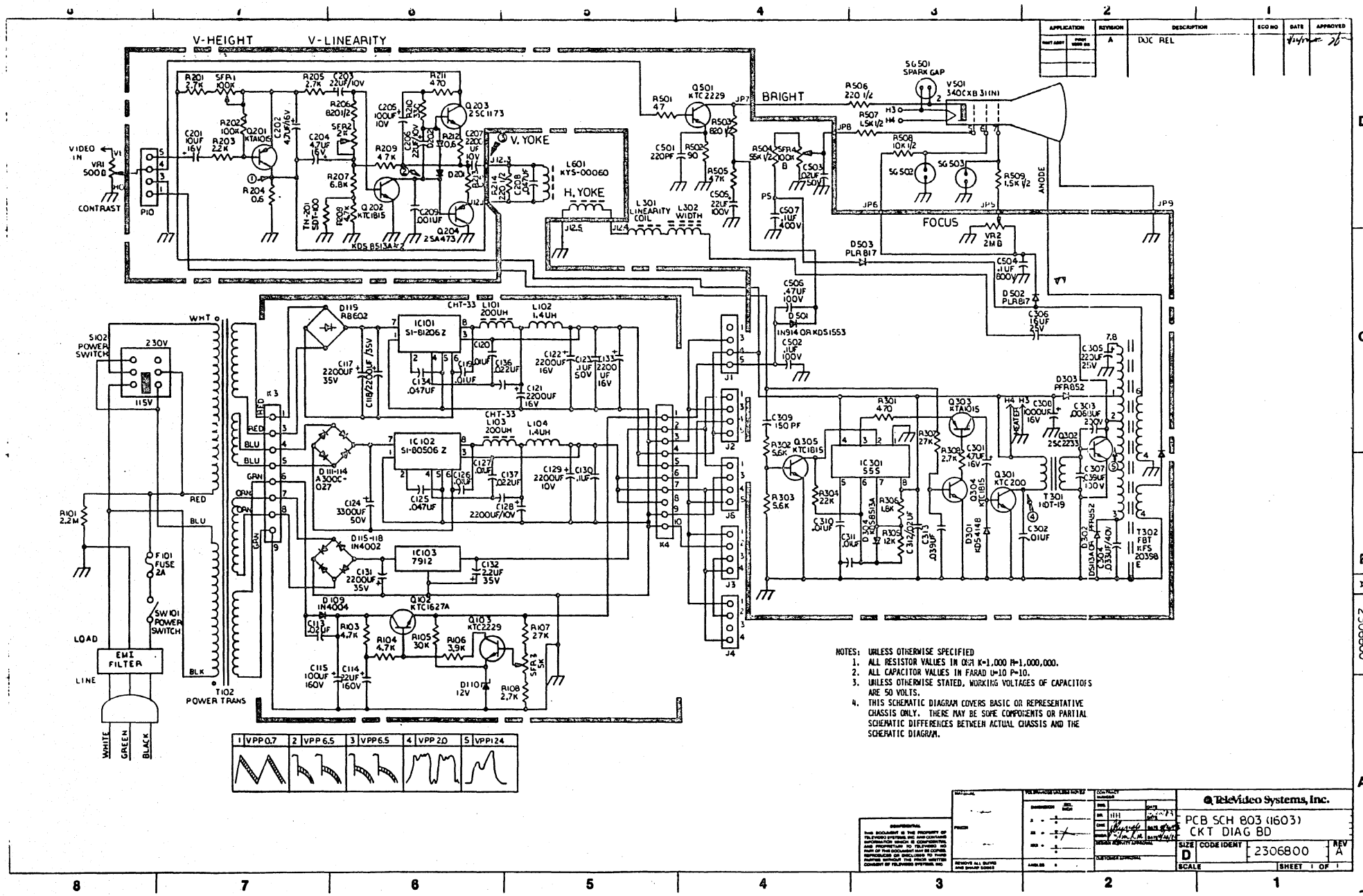
TeleVideo Systems, Inc.

WIRING DIAGRAM AC/DC
805 / 1605

SIZE	CODE IDENT		REV
D		2323300	A

SCALE 1/2 | SHEET 1 OF 1

2323300 A



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES IN OHM K=1,000 M=1,000,000.
2. ALL CAPACITOR VALUES IN FARAD U=10 P=10.
3. UNLESS OTHERWISE STATED, WORKING VOLTAGES OF CAPACITORS ARE 50 VOLTS.
4. THIS SCHEMATIC DIAGRAM COVERS BASIC OR REPRESENTATIVE CHASSIS ONLY. THERE MAY BE SOME COMPONENTS OR PARTIAL SCHEMATIC DIFFERENCES BETWEEN ACTUAL CHASSIS AND THE SCHEMATIC DIAGRAM.

APPLICATION	REVISION	DESCRIPTION	ECO NO	DATE	APPROVED
	A	DOC REL			

TeleVideo Systems, Inc.

PCB SCH 803 (1603)
CKT DIAG BD

SIZE	CODE IDENT		REV
D		2306800	A
SCALE		SHEET 1 OF 1	

2306800

TeleVideo Systems, Inc.

122910-00 Rev. B