Model 925 Maintenance Manual

TeleVideo Systems, Inc.

TELEVIDEO®
925 VIDEO DISPLAY TERMINAL
MAINTENANCE MANUAL

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TeleVideo Systems, Inc. makes no representations or warranties with respect to this manual. Further, TeleVideo Systems, Inc. reserves the right to make changes in the specifications of the product described within this manual at any time without notice and without obligation of TeleVideo Systems, Inc. to notify any person of such revision or changes.

TeleVideo Systems, Inc., 550 East Brokaw Road, P.O. Box 6602, San Jose, CA 95150-6602 408/971-0255

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SERVICE AND WARRANTY INFORMATION

If your terminal has technical problems, TeleVideo's Technical Support Department will assist you. The toll-free numbers are 800/821-3774 (inside California) or 800/521-4897 (outside California). International customers can telex 4745041. Or you can call your regional sales office, listed in this section.

A repairs price list is in the last section of this manual.

SERVICE UNDER WARRANTY

TeleVideo products are covered by a limited warranty, found in this section. For service under warranty you must return products to TeleVideo's factory repair facility.

Return Procedures

1. To return a terminal or part for service, call Customer Service for a Return Material Authorization (RMA) number.

2. Have the following information ready:

   Your name and your company's name, address and telephone number. Give a street address, since freight delivery services do not deliver to a post office box.

   Your terminal's model number and serial number.

   A brief but accurate description of the problem. If you have more than one problem, list each problem separately. A separate RMA will be issued for each item. TeleVideo can repair only the problems described on an RMA.

3. Tag each item to be returned with the RMA number and your description of the problem. This is especially important if you plan to ship more than one part in the same container. See the Operator's Manual for information about packing the terminal for shipment.

4. Write the RMA number on the shipping label. TeleVideo will refuse any item delivered without an RMA number on the outside of the shipping carton and return it to the sender.

5. Use the RMA number if you call to ask about your terminal while it is being repaired.

6. If the item is under warranty, it will be returned to you via best way. All express shipments will be at the customer's expense and must be requested when receiving the RMA.

REGIONAL SALES OFFICES

East
6900 Jericho Turnpike
Suite 100 LL
Syosset, NY 11791
(516) 496-4777

Northeast
1601 Trapelo Road
Reservoir Place
Waltham, MA 02154
(617) 890-3282

West
18662 MacArthur Blvd.
Suite #107
Irvine, CA 92715
(714) 476-0244

Northwest
550 East Brokaw Road
P.O. Box 6602
San Jose, CA 95150-6602
(408) 971-0255

Southcentral
5525 High Point Drive
Suite #101
Irving, TX 75062
(214) 258-6776

Midwest
1002 E. Algonquin Road
Suite #112
Schaumburg, IL 60195
(312) 397-5400

Southeast
6075 The Corners Parkway
Suite #208
Norcross, GA 30092
(404) 447-1231

Central Europe
Saturnusstraat 25
2132 HB Hoofdorp
The Netherlands
Phone: 011-31-2503-35444
Telex: 74615 TLVDO NL

Northern Europe
Dorna House,
Guildford Rd., West End
Surrey GU249PW
England
Phone: 011-44-9905-6464
Telex: 858922

Southern Europe
3 bis rue leCorbusier
bat. Berne Silic 244
94568 Rungis Cedex,
France
Phone: 011-33-1-687-34-40
Telex: 205191F
(TVIVID 205191F)

STATEMENT OF LIMITED WARRANTY

TeleVideo Systems, Inc. ("TeleVideo") warrants to its distributors, systems houses, end users, and OEMs ("Buyer"), that products manufactured by TeleVideo are free from defects in materials and workmanship. TeleVideo's obligations under this warranty are limited to repairing or replacing, at TeleVideo's option, the part or parts of the products which prove defective in material or workmanship within 15 months after shipment by TeleVideo. Buyer must pass along to its initial customer or user ("Customer") a minimum of 12 months' coverage within this 15-month warranty period, provided that Buyer gives TeleVideo prompt notice of any defect and satisfactory proof thereof.

Products may be returned to Buyer only after a Return Material Authorization number ("RMA") has been obtained from TeleVideo by telephone or in writing. Buyer will prepay all freight charges to return any products to the repair facility designated by TeleVideo and include the RMA number on the shipping container. TeleVideo will, at its option, either repair the defective products or parts or deliver replacements for defective products or parts on an exchange basis to Buyer, freight prepaid to the Buyer. Products returned to TeleVideo under this warranty will become the property of TeleVideo. With respect to any product or part thereof not manufactured by TeleVideo, only the warranty, if any, given by the manufacturer thereof, applies.

Exclusions

This limited warranty does not cover losses or damage which occur in shipment to or from Buyer, or are due to, (1) improper installation or maintenance, misuse, neglect, or any cause other than ordinary commercial or industrial application, or (2) adjustment, repair, or modifications by other than TeleVideo-authorized personnel, or (3) improper environment, excessive or inadequate heating or air conditioning and electrical power failures, surges, or other irregularities, or (4) any statements made about TeleVideo's products by salesmen, dealers, distributors or agents, unless confirmed in writing by a TeleVideo officer.

If the firmware or hardware is altered or modified by the Buyer, this firmware and hardware is not covered within this limited warranty and the Buyer bears sole responsibility and liability for that firmware and hardware.

THE FOREGOING TELEVIDEO LIMITED WARRANTY IS IN LIEU OF ALL OTHER WARRANTIES, WHETHER ORAL, WRITTEN, EXPRESSED, IMPLIED, OR STATUTORY. IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE DO NOT APPLY. TELEVIDEO'S WARRANTY OBLIGATIONS AND DISTRIBUTOR'S REMEDIES HEREUNDER ARE SOLELY AND EXCLUSIVELY AS STATED HEREIN.

TELEVIDEO'S LIABILITY, WHETHER BASED ON CONTRACT, TORT, WARRANTY, STRICT LIABILITY, OR ANY OTHER THEORY, SHALL NOT EXCEED THE PRICE OF THE INDIVIDUAL UNIT WHOSE DEFECT OR DAMAGE IS THE BASIS OF THE CLAIM. IN NO EVENT SHALL TELEVIDEO BE LIABLE FOR ANY LOSS OF PROFITS, LOSS OF USE OF FACILITIES OR EQUIPMENT, OR OTHER INDIRECT, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

SERVICE OUT OF WARRANTY

If your terminal is out of waranty when it needs service, follow the same procedure to receive an RMA. You will be responsible for all shipping costs.

If your company requires a purchase order for out-of-warranty repairs, let us know the purchase order number when you call in. One purchase order may cover several repairs, but we will give each unit its own individual RMA number. This allows us to return each unit quickly without holding up the entire purchase order for one unit.

EXTENDED WARRANTY

TeleVideo offers an Extended Warranty Agreement, which extends the terms of the above-stated Limited Warranty for an additional year. To take advantage of this Extended Warranty, you must sign the Extended Warranty Agreement and return it, together with full payment, to TeleVideo before the Limited Warranty expires. Shippng charges are not included in the Extended Warranty. This is normally the only expense you incur. Please contact the Customer Service department or your sales representative for details. To renew the Extended Warranty for another year, follow the same procedure.

ORDERING SPARE PARTS

Parts may be ordered by telephone, written purchase order or telex, or through Regional Sales Office electronic bulletin board systems. You may direct orders to the TeleVideo Regional Sales Office in your area or to the TeleVideo Corporate Spare Parts Order Entry Department at the following address:

TeleVideo Systems, Inc.
550 E. Brokaw Road
P.O. Box 6602
San Jose, CA 95150-6602

or call

San Jose:	408-971-0255
CA Watts:	800-821-3774
U.S. Watts:	800-521-4897
Telex:	474-5041
Fax:	408-734-1927 or
	408-998-2092
TWX	910-338-7633

All orders are shipped F.O.B. our designated site.

PCB ASSEMBLY CONTROL BOARD

Part Number	Description	Location
120302-00	IC NE555 TIMER	A46
120358-00	IC 2114ICB RAM 150ns.	A41, 42
180000-16	IC ROM CHAR GEN 910	A31
120492-00	IC 6116 RAM 2Kx8 150ns.	A47
120496-00	IC 6502A MICROPROCESSOR	A60
123443-00	IC CRT CNTRL 6845R	A59
120530-00	IC SY6551A/1 2-MHz SYN/AMI	A32, 33
120242-00	IC 74LS00	A3, 28, 55
120416-00	IC 74LS02	A4
120246-00	IC 74S04	A16
120248-00	IC 74LS04	A27, 35
120348-00	IC 7406	A5
120252-00	IC 74LS08	A10, 13, 18, 54
120254-00	IC 74LS10	A2
120258-00	IC 74LS32	A11, 12, 14, 23, 26, 36, 38
120266-00	IC 74LS74	A1, 6
120268-00	IC 74LS86	A15
120410-00	IC 74LS138	A29
120272-00	IC 74LS139	A37
120274-00	IC 74LS157	A56-58
120276-00	IC 74LS163	A24
120278-00	IC 74LS166	A30
120280-00	IC 74LS173	A19-21
120282-00	IC 74LS174	A22
120442-00	IC 74LS244	A43, 51-53
120362-00	IC 74LS245,N8T245N	A40
120376-00	IC 74LS273	A44, 45
120290-00	IC 74LS374	A39
120292-00	IC 75188 4X LINE DRVR	A25, 34
120294-00	IC 75189A 4X LINE RCVR	A9, 17
120315-00	RES CF 1M OHM 1/4W 5%	R19
120335-00	RES CF 22 OHM 1/4W 5%	R2
120511-00	RES CF 68 OHM 1/4W 5%	R3
120513-00	RES CF 270 OHM 1/4W 5%	R8
120515-00	RES CF 330 OHM 1/4W 5%	R15, 24-26
120517-00	RES CF 470 OHM 1/4W 5%	R13
120317-00	RES CF 750 OHM 1/4W 5%	R7, 12
120521-00	RES CF 1000 OHM 1/4W 5%	R4, 5, 9
120523-00	RES CF 1800 OHM 1/4W 5%	R14
120531-00	RES CF 4700 OHM 1/4W 5%	R1, 10, 11, 17, 23, 27
120337-00	RES CF 47K OHM 1/4W 5%	R21
120323-00	RES CF 51K OHM 1/4W 5%	R16
120413-00	RES PK 4.7K OHM 10P SIP	RP1-5
120287-00	CAP CER .01uF 16V 20%	C2, 5, 7, 14-17, 19, 23B, 24-26, 28-30, 33-40, 43-46, 48, 49, 52-55, 60
120289-00	CAP MONO .01uF 50V 10%	C6, 27, 47, 50, 51

PCB ASSEMBLY CONTROL BOARD

Part Number	Description	Location
120279-00	CAP ELEC 1uF 16V 10%	C4
120275-00	CAP TANT 4.7uF 16V 10%	C1, 3
120273-00	CAP ELEC 10uF 16V 20%	C41, 61
120257-00	CAP ELEC 22uF 15V 20%	C56-58
120241-00	CAP MICA 10pF 50V 5%	C18
120291-00	CAP CER 330pF 50V 20%	C8-13, 20-23, 62-70
120271-00	CAP TANT 10uF 25V 10%	C42
120475-00	DIODE 1N914	CR1, 2
120527-00	RES CF 3300 OHM 1/4W 5%	R20
120455-00	TRAN 2N4401 NPN/SILICON	Q1, 2
120986-02	CRY 1.8432-MHz	Y1 OPT, Y5 OPT
120986-05	CRY 13.6080-MHz	Y2
120968-00	SWITCH 10P DIP/20P SIDE ADJ	S1-3
120984-01	SOCKET 24P IC DIP	A31-47-50
120984-02	SOCKET 40P IC DIP	A59, 60
120984-04	SOCKET 28P IC DIP	A32, 33
120984-00	SOCKET 18P IC DIP	A41, 42
120979-00	CONN 4P MOD JK RJ11	P1
120988-02	CONN 4P HDR WT (5P W/#2P OUT)	P2, 5
180000-31	IC EPROM SYS PROG 925	A50
180000-33	IC EPROM SYS PROG 925	A49

PCB ASSEMBLY CONTROL BOARD GATE ARRAY

Part Number	Description	Location
120496-00	IC 6502A MICROPROCESSOR	A11
123443-00	IC SRT CRT CNTRL 6845R	A28
120530-00	IC SY6551A/1 2-MHz SYN/AMI	A4, 5
130181-00	IC GATE ARRAY TELEPRT C	A39
180000-31	IC EPROM SYS PROG 925	A14
180000-33	IC EPROM SYS PROG 925	A15
120492-00	IC 6116 STAT RAM 150ns.	A32
180000-16	IC ROM CHAR GEN 910	A17
120358-00	IC 2114-ICB RAM 150ns.	A9, 10
120242-00	IC 74LS00	A35
120246-00	IC 74S04	A40
120248-00	IC 74LS04	A36
120252-00	IC 74LS08	A8, 37
120258-00	IC 74LS32	A24, 30, 42, 43
120266-00	IC 74LS74	A7
120272-00	IC 74LS139	A38
120274-00	IC 74LS157	A20-22
120278-00	IC 74LS166	A12
120290-00	IC 74LS374	A18
120292-00	IC 75188N 4X LINE DRIVER	A16, 23
120294-00	IC 75189A 4X LINE RECEIVER	A1, 2
120302-00	IC NE555 TIMER	A6
120348-00	IC 7406	A31
120362-00	IC 74LS245, N8T245N	A19
120376-00	IC 74LS273	A26, 27
120410-00	IC 74LS138	A13
120442-00	IC 74LS244 8X BFR/L DRVR/L RCV	A3, 29, 34, 41
120276-00	IC 74LS163 4-BIT CNTR	A25
120345-00	RES CF 33 OHM 1/4W 5%	R9
120513-00	RES CF 270 OHM 1/4W 5%	R5
120515-00	RES CF 330 OHM 1/4W 5%	R22-24, 27
120517-00	RES CF 470 OHM 1/4W 5%	R28
120521-00	RES CF 1000 OHM 1/4W 5%	R7, 11, 16
120523-00	RES CF 1800 OHM 1/4W 5%	R26
120527-00	RES CF 3300 OHM 1/4W 5%	R18
120531-00	RES CF 4700 OHM 1/4W 5%	R3, 4, 10, 12-15, 21
120315-00	RES CF 1M OHM 1/4W 5%	R20
120317-00	RES CF 750 OHM 1/4W 5%	R6, 25
120323-00	RES CF 51K OHM 1/4W 5%	R2
120335-00	RES CF 22 OHM 1/4W 5%	R1
120337-00	RES CF 47K OHM 1/4W 5%	R19
120341-00	RES CF 10K OHM 1/4W 5%	R8
120413-00	RES PK 4.7K OHM 10P SIP	RP1-4
120241-00	CAP MICA 10pF 50V 5%	C31
120271-00	CAP TANT 10uF 25V 10%	C32
121969-00	CAP MYLAR .001uF 50V (OPC)	C34

PCB ASSEMBLY CONTROL BOARD GATE ARRAY

Part Number	Description	Location
120251-00	CAP MICA 150pF 500V 1%	C35
120257-00	CAP ELEC 22uF 16V +20%	C24-26
120273-00	CAP ELEC 10uF 16V 20%	C28, 30
120275-00	CAP TANT 4.7uF 16V 10%	C18
120279-00	CAP ELEC 1uF 16V 10%	C18A, 33
120287-00	CAP CER .01uF 16V 20%	UNMARKED C20
120289-00	CAP MONO .01uF 50V 10%	C27
120293-00	CAP MONO 330pF 100V 20%	C1-17, 19 UNMARKED
120301-00	CAP CER .1uF 50V 10%	C29
120475-00	DIODE 1N914	CR1, 2
120455-00	TRAN 2N4401 NPN/SI	Q1, 2
120986-02	CRY 1.8432-MHz	Y1 (OPT.), Y3
120986-05	CRY 13.6080-MHz	Y2
121754-00	TAPE FOAM DBL/S 1/16 x 1/4" WD	Y1 (OPT.), Y2, Y3
120968-00	SWITCH 10P DIP/20P SIDE ADJ	SW-1-3
120984-00	SOCKET 18P IC DIP	XA9, 10
120984-01	SOCKET 24P IC DIP	XA14, 15, 17, 32, 33
120984-02	SOCKET 40P IC DIP	XA11, 28, 29
120984-04	SOCKET 28P IC DIP	XA4, 5
121746-01	SOCKET 16P IC DIP LO PROF	XP6
121653-00	CONN 25P D-SUB MTL	P3, 4
120979-00	CONN 4P MOD JK RJ11	P1
120988-02	CONN 4P HDR WT (5PW/#2P OUT)	P2, 5

PCB ASSEMBLY VIDEO MONITOR

Part Number	Description	Location
120257-00	CAP ELEC 22uF 16V +20%	C203
120273-00	CAP ELEC 10uF 16V 20%	C201
120275-00	CAP TANT 4.7uF 16V 10%	C202, 204
120289-00	CAP MONO .01uF 50V 10%	C503
120305-00	CAP MONO .039uF 50V 5%	C307
120309-00	CAP CER 1.0pF 1KV SG	SG501
120321-00	RES CF 100K OHM 1/4W 5%	R202
120531-00	RES CF 4.7K OHM 1/4W 5%	R208
120337-00	RES CF 47K OHM 1/4W 5%	R209, 505
120339-00	RES CF 150 OHM 1/4W 5%	R211
120377-00	RES CF 47 OHM 1/4W +/-5%	R501
120383-00	RES CF 2.7K OHM 1/4W +/-5%	R201, R205
120387-00	RES CF 2.2K OHM 1/4W 5%	R203
120391-00	RES CF 6.8K OHM 1/4W 5%	R207
120395-00	RES CF 56K OHM 1/4W 5%	R504
120513-00	RES CF 270 OHM 1/4W 5%	R214
120515-00	RES CF 330 OHM 1/4W 5%	R210
120517-00	RES CF 470 OHM 1/4W 5%	R301
120531-00	RES CF 4700 OHM 1/4W 5%	R208
121771-00	RES WW 0.6 OHM 2W	R204, 212, 213
121776-00	RES CF 90 OHM 1/4W	R502
121777-00	POT TRIM 100K SIDE ADJ PCMT	SFR1, 4
121778-00	POT TRIM VERTICAL LINEARITY	SFR2
121779-00	POT TRIM 5K OHM SIDE ADJ PCMT A	SFR3
121801-00	POT FOCUS 2M OHM	VR2
121802-00	POT OCNTRAST	VR1
121803-00	THERMISTOR OPC 1K OHM	TH201
121860-00	RES CF 220 OHM 1/2W 5%	R506
121862-00	RES CF 820 OHM 1/2W 5%	R206, 503
121863-00	RES CF 1.5K OHM 1/2W 5%	R507, 509
121864-00	RES CF 10K OHM 1/2W 5%	R508
121959-00	CAP CER 220pF 50V	C501
121960-00	CAP ELEC 100uF 10V +/-20%	C205
120261-00	CAP 22uF 25V	C206
121961-00	CAP ELEC 22uF 100V	C505
121962-00	CAP ELEC 220uF 10V (OPC)	C207
121967-00	CAP ELEC 4.7uF 16V (OPC)	C301
121968-00	CAP MYLAR .0068uF 200V (OPC)	C303
121970-00	CAP MYLAR .01uF 50V (OPC)	C302
121971-00	CAP MYLAR .47uF 50V (OPC)	C208
121970-00	CAP MYLAR .01uF 50V	C502
121973-00	CAP MYLAR .1uF 600V (OPC)	C504

PCB ASSEMBLY VIDEO MONITOR

Part Number	Description	Location
121972-00	CAP MYLAR .47uF 50V (OPC)	C506
121975-00	CAP MYLAR .47uF 400V (OPC)	C304
121993-00	CAP ELEC 220uF 16V	C305
122008-00	YOKE DEFLECT W/CONN KYS-00060	L202
122009-00	COIL LINEARITY NON ADJ LC-36	L201
122010-00	COIL INDCTR 27uF .3PIE	L302
122012-00	TNFR HORIZ DR HDT-19	T301
130745-00	TNFR FLYBACK KYS-20708	T302
122018-00	DIODE 1N920/KD8513A	D201, 202 301
122017-00	DIODE DS113A/MR1-1000 (DAMPER)	D302
120475-00	DIODE 1N914	D501
122022-00	DIODE 1N4004 MOT	D502
122136-00	COIL LINEARITY ADJ IC-014631	L201
122800-00	CAP ELEC 16V (NON-P)	C306
130745-00	TNFR FLYBACK KYS-20708	T302
130116-00	TRAN KTC 2229Y	Q103
120455-00	TRAN 2N4401/2SC1166	Q201
120465-00	TRAN 2N3904/KTC1815	Q202
121997-00	TRAN 2N6121/2SC1173	Q203
122021-00	TRAN 2N6124/2SA473	Q204
120455-00	TRAN 2N4401/2SC1166	Q301
120473-00	TRAN 2SC2373	Q302

PCB ASSEMBLY POWER SUPPLY

Part Number	Description	Location
121982-00	CAP 470uF 35V (OPC)	C116
121981-00	CAP TANT .33uF 35V (OPC)	C114, 115
121966-00	CAP ELEC 4700uF 16V (OPC)	C117
121965-00	CAP ELEC 3300uF 35V (OPC)	C113
121964-00	CAP ELEC 22uF 160V	C120
121963-00	CAP ELEC 100uF 160V	C119
120287-00	CAP CER .01uF 16V 20%	C101-109
122006-00	DIODE 1N5391/DS135D	D101, 102, 109, 113, 114
130098-00	DIODE BY251 3A 200V	D103-108
122016-00	DIODE 1N759A/RD12EB ZENER	D111, 112
121931-00	FUSE 3A 125V 3AG	F102, 103
121268-00	VOLT REG LAS 1605 2A/5V	IC2
121269-00	VOLT REG LAS 16CB 2A/13.8V GEN	IC1
121766-00	RES CF 390 OHM 1/2W 5%	R102
121774-00	RES CF 3.9K OHM 1/4W	R107
121373-00	RES CF 27K OHM 1/4W +/-5%	R108
120531-00	RES CF 4700 OHM 1/4W 5%	R105, 106
120393-00	RES CF 30K OHM 1/4W 5%	R110
120383-00	RES CF 2.7K OHM 1/4W +/-5%	R109
121779-00	POT TRIM 5K OHM SIDE ADJ PCMT	SFR3
120471-00	TRAN 2N5551 NPN/HIGH VOLTAGE	Q103
120467-00	TRAN KTC1627/MPSA06 NPN/SIL	Q102

DETACHABLE KEYCAPS

Description	Sculptured Printed	Sculptured Blank	Degree
1X1 LG BLANK		121616-00	0
1X1 LG NO SCROLL/SETUP	120887-00		0
1X1 LG F1	120850-00		0
1X1 LG F2	120851-00		0
1X1 LG F3	120852-00		0
1X1 LG F4	120853-00		0
1X1 LG F5	120854-00		0
1X1 LG F6	120855-00		0
1X1 LG F7	120856-00		0
1X1 LG F8	120857-00		0
1X1 LG F9	120858-00		0
1X1 LG F10	120859-00		0
1X1 LG F11	120860-00		0
1X1 LG CHAR INSERT	120861-00		0
1X1 LG CHAR DELETE	120862-00		0
1X1 LG LINE INSERT	120863-00		0
1X1 LG LINE DELETE	120864-00		0
1X1 DG BLANK		121617-00	+14
DG ESC/LOC ESC	120842-00		+14
1X1 DG 1/!	120778-00		+14
1X1 DG 2/@	120779-00		+14
1X1 DG 3/#	120780-00		+14
1X1 DG 4/$	120781-00		+14
1X1 DG 5/%	120782-00		+14
1X1 DG 6/^	120783-00		+14
1X1 DG 7/&	120784-00		+14
1X1 DG 8/*	120785-00		+14
1X1 DG 9/(	120786-00		+14
1X1 DG 0/)	120787-00		+14
1X1 DG -/_	120788-00		+14
1X1 DG =/+	120789-00		+14
1X1 DG `/~	120790-00		
1X1 DG BACK SPACE	120792-00		+14
1X1.5 DG TAB	120845-00		+7
1X1.5 DG BLANK		121618-01	+7
1X1 DG BLANK		121618-00	+7
1X1 DG Q	120806-00		+7
1X1 DG W	120807-00		+7
1X1 DG E	120808-00		+7
1X1 DG R	120809-00		+7
1X1 DG T	120810-00		+7
1X1 DG Y	120811-00		+7
1X1 DG U	120812-00		+7
1X1 DG I	120813-00		+7
1X1 DG O	120814-00		+7
1X1 DG P	120815-00		+7
1X1 DG [/]	120816-00		+7
1X1.5 DG LINE FEED	120844-00		+7
1X1.25 LG CLEAR SPACE	120896-00		+7
1X1 LG CTRL	120869-00		0

DETACHABLE KEYCAPS

Description	Sculptured Printed	Sculptured Blank	Degree
1X1 DG ALPHA LOCK	120818-00		0
1X1 DG A	120819-00		0
1X1 DG S	120820-00		0
1X1 DG D	120821-00		0
1X1 DG BLANK		121616-01	0
1X1 DG F	120822-00		0
1X1 DG G	120823-00		0
1X1 DG H	120824-00		0
1X1 DG J	120825-00		0
1X1 DG K	120826-00		0
1X1 DG L	120827-00		0
1X1 DG ;/:	120828-00		0
1X1 DG '/"	120829-00		0
LG "L" RETURN	120894-00		
1X1 LG BREAK	120870-00		0
1X1 DG BACK TAB	120817-00		-7
1X1.5 LG SHIFT	120847-00		-7
1X1 DG Z	120830-00		-7
1X1 DG X	120831-00		-7
1X1 DG C	120832-00		-7
1X1 DG V	120833-00		-7
1X1 DG B	120834-00		-7
1X1 DG N	120835-00		-7
1X1 DG M	120836-00		-7
1X1 DG BLANK		121619-00	-7
1X1 DG ,/<	120837-00		-7
1X1 DG ./>	120838-00		-7
1X1 DG //?	120839-00		-7
1X1 DG {/}	120840-00		
1X1 LG DELETE	120871-00		-7
1X1 LG PRINT (LP)	120893-00		0
1X1 LG FUNCT (LP)	120890-00		0
1X8 DG SPACE BAR	120897-00		
1X1 LG HOME (LP)	120891-00		0
1X1 LG CURSOR ARROW (LP)	120892-00		0
1X1 LG LINE ERASE	120865-00		0
1X1 LG PAGE ERASE	120866-00		0
1X1 LG SEND	120885-00		0
1X1 DG 7	120799-00		0
1X1 DG 8	120800-00		0
1X1 DG 9	120801-00		0
1X1 DG 4	120796-00		0
1X1 DG 5	120797-00		0
1X1 DG 6	120798-00		0
1X1 DG 1	120793-00		0
1X1 DG 2	120794-00		0
1X1 DG 3	120795-00		0
1X1 DG ,	120804-00		0
1X1 DG 0	120802-00		0
1X1 DG .	120805-00		0

DETACHABLE KEYCAPS

Description	Sculptured Printed	Blank	Degree
1X1.5 LG ENTER	120848-00		0
1X1 DG -	120803-00		0

925 THEORY OF OPERATION

SECTION

MAIN LOGIC BOARD

4.1

OVERVIEW

The TeleVideo Model 925 terminal is the third member of a family of terminals based on the 6502A microprocessor. Circuitwise, it is very similar to the Model 910; the main differences being increased program ROM space, serial keyboard interface, and more complex attribute and communications sections. Functionally, the 925 is designed to be halfway between the more sophisticated Model 950 and the conversational 910.

As in the 950 and 910, the microprocessor is totally interrupt driven. This operation provides the most efficient and error free means for asynchronous reception and transmission of data.

4.2

OPERATING CLOCKS

There are three clocks of the 925 control board. Two of these are synchronized; shift clock and character clock, while the third, the receive and transmit clock, is totally independent of the other two. The basic clock on the board is the Video or Dot clock. It's frequency range is 13.608 megaHertz and is produced by a crystal controlled oscillator which is made up of the crystal, Y2, part of chip A16, and several passive feedback components (see Sheet 7 of schematic). This clock is used to shift video data out of a shift register for display on the CRT. It is also used to clock a counter, A24, to create the system clock. The system clock is designated 'Character Clock' on the 925 schematic. It is used for two purposes; character clock input to the CRT control chip (A59, Sheet 2) and as the system clock (00) input to the 6502A microprocessor (A60 Sheet 1).

A 74LS163 presettable 4 bit binary counter A24, Sheet 7) is used to divide the shift clock by eight; providing a frequency of 1.701 megaHertz. The 74LS163, which is normally a divide by 16 counter, is forced to divide by eight by loading a count of eight into the counter when it reaches it's highest count (15).

In this mode, the QC output of the counter is low for 4 clocks and high for 4, making it suitable for use as a symmetrical clock.

The two Asynchronous Communications Interface Adapters (ACIA #1 and ACIA #2, Sheet 5) have internal clock oscillators and require only that the external crystal be added. The circuitry of the 925 allows the two ACIA's to share one crystal, Y1.

Internal to each ACIA, the basic frequency of 1.8432 megaHertz is divieded down by a factor determined by a firmware controlled register. ACIA # 2, which is used for receiving keyboard data, is always set for 1200 baud (bits per second). ACIA # 1 is

shared by the Host Communications port (P3), and the printer port (P4). The baud rate for ACIA # 1 depends on the baud rate switch settings for the two ports.

4.3

ADDRESS DECODING

The 65,536 byte address field of the 6502A microprocessor (MPU) is divided as follows. The two highest address lines (A14 & A15) are decoded by a 1 of 4 decoder (half of A37, Sheet 1) to divide it into four 16,384 (16K) byte sections. The highest 16K bytes ($C000_{16}$ - $FFFF_{16}$)are used for program Read Only Memory (ROM).

The program ROM contains a program which controls the microprocessor, causing it to process data fed to it by the Keyboard or the host computer. The 16K block is divided further into two 8,192 (8K) byte sections. When the MPU is addressing the higher 8K bytes, the chip located at A50 is selected. When the MPU is addressing the lower 8K bytes, the chip located at A49 is selected.

The next lower 16K bytes, 8000-BFFF is used to access I/O devices. This output of A37 is connected to a 1 of 8 decoder (A29, Sheet 1) and the other section of A37 where, using lower order address lines, 12 individual locations are decoded. Each I/O device is treated as if it were an individual byte within the memory map.

The output labeled $\overline{4000\text{-}7FFF}$ from A37 defines the second lowest 16K clock within the address range. This signal is 'OR'ed with 02 low (A54, Sheet 1) to select two 6116, 2K by 8 bit RAM chips. (A47 and A48, Sheet 2).

These chips are used to store data to be displayed on the CRT (Display RAM). A48 contains data for one screen (page 1) and A47 the other (page 2).

The output labeled $\overline{0000\text{-}3FFF}$ is true (low) when the MPU is addressing any location within that range. It is used to select two 2114, 1K X 4 bit RAM chips. These RAMS are used to store variable data that is processed by the MPU during program execution. (System RAM).

4.4

TERMINAL MEMORY

Memory in the 925 terminal consists of ROM and RAM. As stated in Section 4.3, Program (or System) ROM is located within the range C000-FFFF. It is further broken down into two 8K byte

sections, C000-DFFF and E000-FFFF. Each of these sections is represented by a socket capable of accepting a 2K (2048) byte ROM, a 4K (4096) byte ROM or an 8K (8192) byte ROM. This allows expansion of program ROM from 2K bytes to 16K bytes in 2K byte increments. Each socket is selected using the C000-FFFF output of A37 'AND'ed with the high (E000-FFFF) or low (C000-DFFF) condition of address line A13.

The standard configuration of the 925 is 4K bytes located from D000-DFFF and another 4K bytes located from F000-FFFF.

System RAM consists of 1K (1024) bytes of static random access (read/write) memory. (A41 & 42, Sheet 1). The 0000-3FFF output of A37 is used to select these two chips. Since there are no other devices located in this section, further decoding is not required. System RAM is used as a buffer for characters received from and transmitted to the host computer and printer; 'Flags' used by the program for decision making, and for storing the states of various software 'timers'.

4.5

DISPLAY FUNDAMENTALS

The circuitry required to display data on the CRT other than the video circuitry, which is covered in Section 4.7 is made up of three parts; display memory, character generation memory and the CRT controller chip (A59, Sheet 2).

The display memory consists of 4K bytes of high speed static RAM (A47 & A48, Sheet 2). The screen contains 25 rows of 80 characters each for a total of 2000 characters. Therefore, each 6116 RAM (2048 bytes each) is capable of storing an entire screen of characters.

The address lines of the two 6116's are controlled by the outputs of three 2 to 1 multiplexers (A56, A57 & A58, Sheet 2). The sources for the inputs of the multiplexers are the address lines of the MPU (A0-A11) and the memory address outputs of the CRT controller (MA0-MA10). The multiplexers' inputs are switched by the 01 output to the MPU. This operation allows the CRT controller memory address lines to drive the display RAM address lines when 01 is high, while the MPU address lines are enabled during 01 low. The MPU accesses the display RAM to update a location due to keyboard input or transmission from the host (Write), or to READ a location for transmission to the host during a block mode transmit.

Display memory accesses from the MPU occur while 01 is low. Data from the display RAM is gated to and from the main Data Bus (D0-D7 lines of the MPU) by a byte wide bi-direction of 01. This buffer is selected if the MPU is addressing a location in Display RAM. The direction of the data is controlled by the R/W signal from the MPU during 02 high.

During the high portion of 01 (02 low), the CRT controller accesses the location specified by its memory address lines. The display RAM is always selected during 02 low and the R/W line of the display RAM is always high at this time. Because of this, any access of display RAM during 02 low will cause a read of the location being addressed. This data is latched by DC Carry (A39, Sheet 3) and used as address lines A3-A9 of the character generator ROM (A31, Sheet 3). A0, A1, and A2 address lines of the character generator ROM are controlled by the RA0, RA1, and RA2 lines from the CRT controller. These define which line of the 10 line character cell is in effect. The data to be displayed for the character and line being addressed is loaded into a parallel in/serial out shift register (A30, Sheet 2). During the next eight cycles of the shift clock this data is shifted out one bit at a time and combined with other signals to create the video output to the video amplifier in the monitor.

The MPU is capable, using address line A11, of writing to or reading from any of the 4096 bytes of display RAM. The CRT controller can only access a maximum of 2048 bytes (using MA0-MA10). To allow the second page to be displayed (providing that a chip is installed in A47), the program, in response to an ESC K, sets a bit in one of the control latches labeled 'Display Page Two'. This connects to the highest order line on the CRT controller side of the multiplexers. Thus, when 01 is high, this bit will be high and A47 will be accessed by the CRT controller.

4.6

INTERRUPT SIGNALS

As mentioned in Section 4.1, the MPU is interrupt driven in the 925. An interrupt is an input to the MPU which causes it to complete its present instruction, save the contents of its internal registers and go to a predetermined location in the program. The MPU will respond to an interrupt within a maximum of 8 system clock cycles of 4.7 microseconds.

The 6502A MPU has two interrupt inputs, IRQ and NMI. IRQ is a maskable interrupt which can, under program control, be ignored. NMI is non-maskable interrupt that cannot be ignored by the MPU.

The Model 925 uses the NMI for interrupts generted by the Keyboard ACIA (A33, Sheet 5). IRQ has two possible sources; the communications ACIA (A32, Sheet 4) and the vertical sync interrupt. The interrupts generated by the ACIA's indicate that data has been received or that the transmitter section is ready to accept a new character. The vertical sync interrupt is used by the program to increment timing registers used to keep track of the time of day, blink the cursor, time the bell, etc. When an interrupt occurs, the firmware (program ROM) must determine which source caused the interrupt and act accordingly.

4.7

VIDEO GENERATION

Control signals for the CRT monitor are generated by the CRT controller, the attribute logic and the shift register mentioned in Sectin 4.5.

The CRT controller produces vertical sync, horizontal sync, display enable and cursor signals. Horizontal and vertical sync are buffered and sent directly to the monitor. Display enable and cursor are used along with the attributes and serial data from the shift register to produce the video signal for the monitor.

Because of the character address latch (A39, Sheet 2), the character generator ROM, and the shift register, it takes two character clock times for a character addressed by the CRT controller to be displayed on the screen. The display enable and cursor signals simultaneously with the memory address coinciding with the position on the screen. Because of this the cursor and display enable signals must be delayed by two character clock times. This is accomplished by a hex D flip-flop (A22, Sheet 4).

The remaining two stages are used to provide a 1 character time delay for the attribute signal and half intensity signal (an additional delay is provided by the character address latch).

The 925 visual attributes are achieved in the following manner:

The high order bit coming out of the character address latch (Chad 7) is used to indicate a protected (half intensity) character. This is the only attribute which is done on a character by character basis. The remaining four attributes, blinking, blank (hidden characters), reverse video and underline, are produced by special characters written into the display RAM by the firmware in response to a special 3 character sequence. (See operators manual). These special characters are decoded to provide a signal labeled 'Attribute' (see pin 4 of A22, Sheet 3). This signal is used to gate DC Carry to the data input of a 'D' flip-flop (pin 2 of A1, Sheet 3) which is clocked on the rising edge of shift clock while DC Carry is low. As long as the character in the character address latch is an attribute character, the data input will be low when the flip-flop is clocked. This keeps the 'Q' output low, enabling the outputs of one of three quad tri-state latches (A19, Sheet 3). This latch is used to carry the existing attributes through a new attribute character, and its outputs are used only during the time that an attribute character is being displayed. (An attribute character is displayed as a half intensity blank). As soon As a non-attribute character is decoded, the 'Q' output of the D flip-flop (pin 5 of A1) is clocked high, disabling the outputs of A19. At the same time, Q output (pin 6) goes low. This is connected to one of the

output enable inputs of another quad tri-state latch (A20). The other output enable input of A20 is controlled by the Q output of another D flip-flop (pin 8 of A1) that goes low approximately 35 nanoseconds after pin 6 of A1. This operation ensures that the outputs of only one of the latches are active at any given time.

The purpose of the second latch is to contain the most recent attributes on the present scan line. The third quad tri-state latch (A21) is used to remember the last attribute character encountered. Unlike the first two latches, which are reset by horizontal sync (once each scan line) the third latch is reset only once each frame by vertical sync. In this manner, the attributes are allowed to continue from one character row to another. The outputs of this third latch are enabled when both D flip-flops mentioned earlier are reset (Q outputs low). The time during which these outputs are enabled is defined as; from the beginning of a new character row that was preceded by a character row containing an attribute character; until a new attribute character is found, i.e., if the only attribute character is character number 62 on character row 10, the outputs of A21 will be enabled at the start of character row 11 and remain enabled until the end of the frame (vertical sync).

The attribute signals, underline, reverse video, blink and blank, are combined with other signals pertinent to the video output (see upper left side of sheet 4), to create a stream of pulses used by the video amplifier to control the electron beam within the CRT.

4.8

COMMUNICATIONS

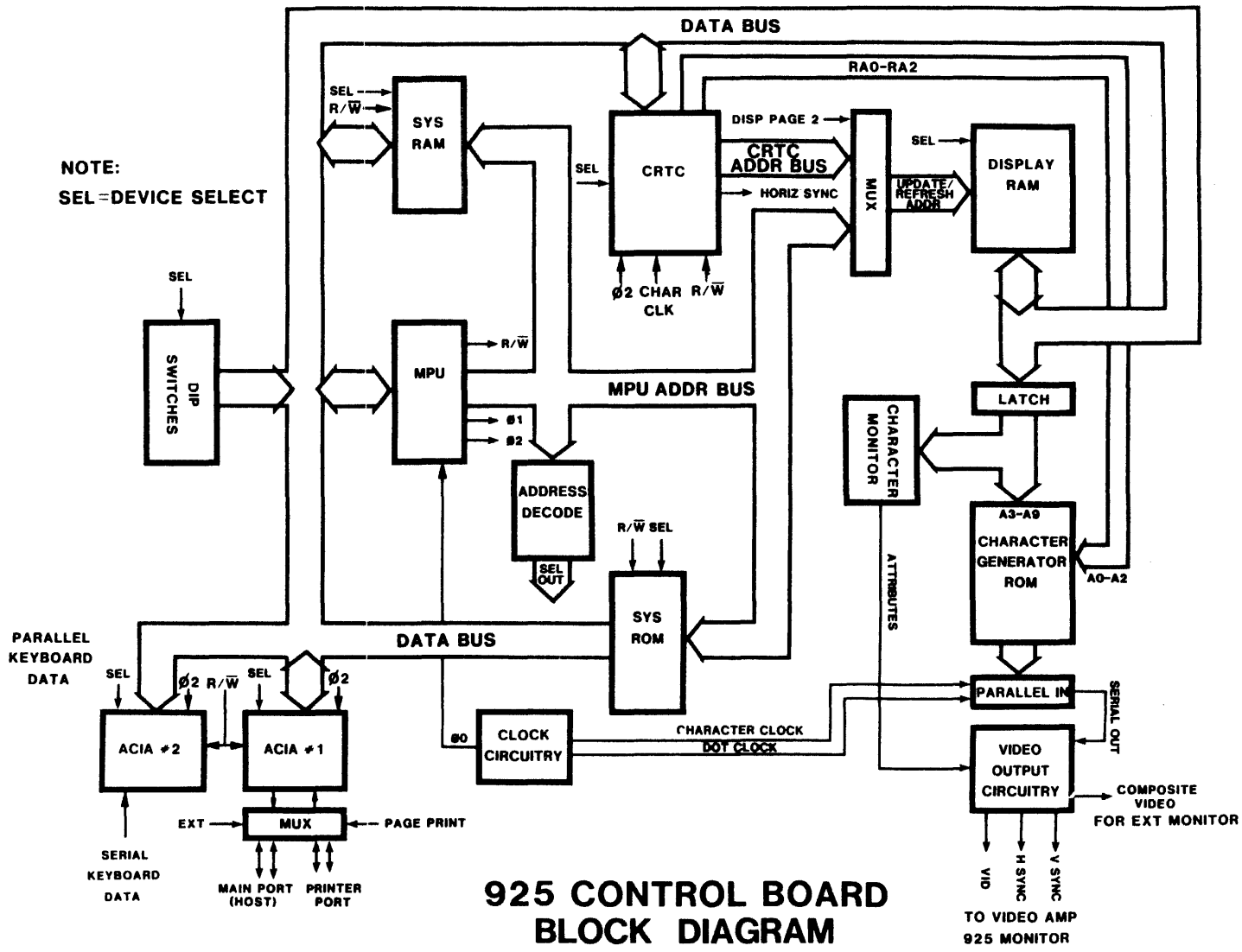
Data from the Keyboard is received via a standard RJ11 connector located on the rear of the board. ACIA # 2 (A33, Sheet 5) is used to convert the serial data into parallel form. When the ACIA receives a character, it interrupts the MPU via the NMI input. The MPU, during the NMI routine, reads the contents of the receive buffer of the ACIA. The keyclick is produced automatically by the hardware, requiring no firmware overhead. The IRQ output of the ACIA also connects to the trigger input of a simple one-shot circuit used to produce a pulse which drives the speaker located in the Keyborad (see lower left section of sheet 5).

The terminal connects to the host computer through P3 (sheet 5) which is a standard 25 pin D type connector located on the rear of the board. In half or full duplex, (conversational) mode, data is sent to the host one character at a time as it is typed on the keyboard. In block mode, data is not sent to the host unless a send command of some sort is entered on the keyboard. These modes of data transmission are completely under control of the firmware.

The 925 also has a separate connector which can be connected to a printer with a serial communications port. The connector for the printer port is P4. Data sent to the printer can come from two selectable sources; the host computer or the terminal screen (display RAM). To enable data from the Host to the printer, the control latch output labeled 'EXTENSION' is used. This gates data received on P3 pin 3 to P4 pin 3 via or gate A26 (pins 4,5,6). It also allows two possible control lines, DTR (P4-20) and Handshake (P4-11) to go to the host.

Another control latch output labeled '$\overline{\text{BI-DIR}}$' allows data from the printer (P4-2) to be sent to the host (P3-2). Data from the printer is not received by the 925 terminal.

During transmission from the host to the printer, the screen may (normal) or may not (transparent) be updated. Another mode of printer operation is page print. In this mode, text is entered on the screen (either page or display RAM) and, when the desired text is entered and properly edited, the data can be sent to the printer by depressing the 'PRINT' key. The data on the screen will be sent to the printer from the 'HOME' position to the cursor position. During page print, the data is not sent to the host. This is done by disabling the data to the host through another gate (A26 pin 8,9,10).



925 CONTROL BOARD BLOCK DIAGRAM

Figure 4-1

Table 4-1

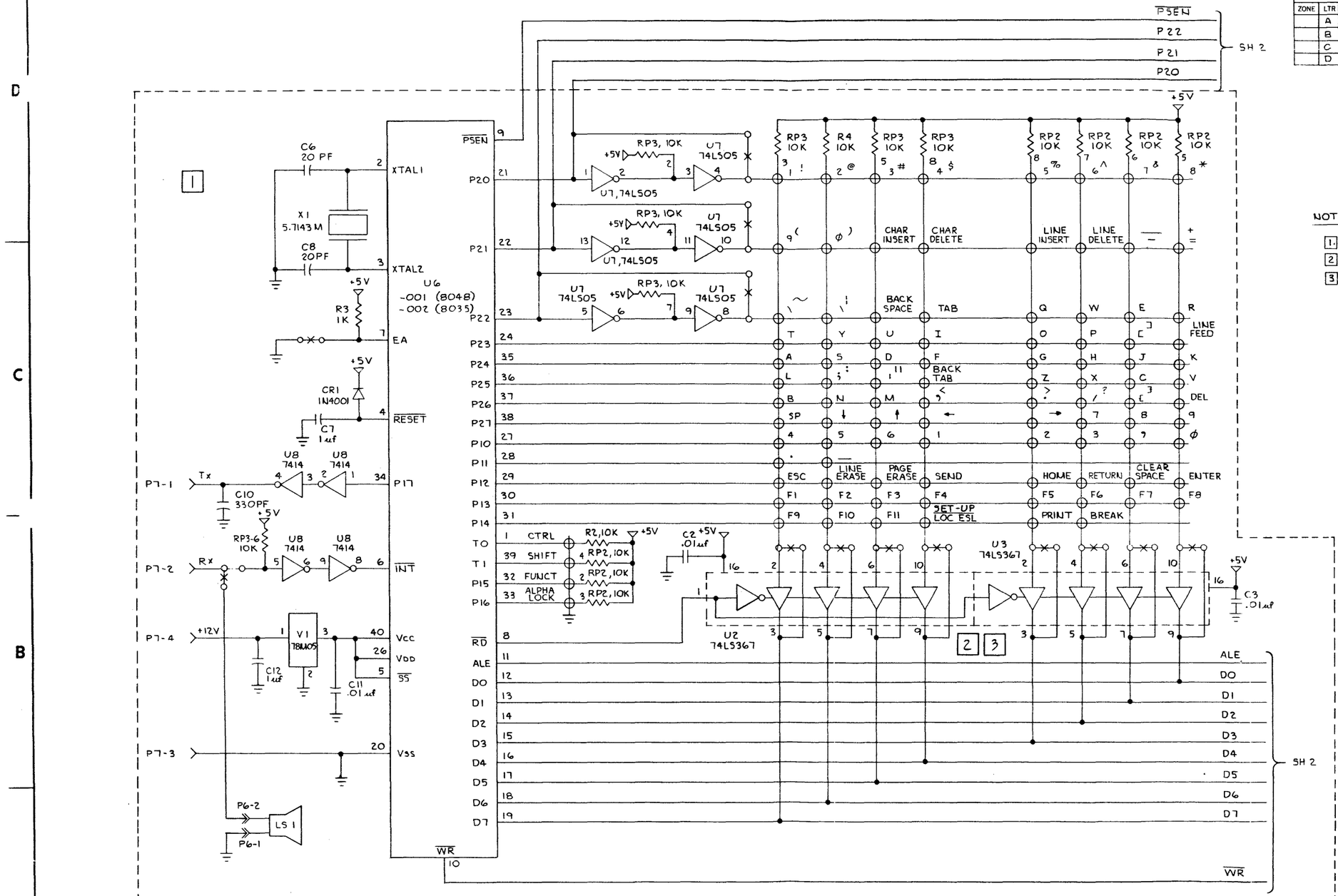
			D7	D6	D5	D4	D3	D2	D1	DØ	
Read Only	ROM # 1	FFFF E000	PROGRAM DATA								SYS ROM
	Unused ROM # 1	EFFF E000									
	ROM # 2	DFFF D000	PROGRAM DATA								
	Unused ROM # 2	CFFF C000									
	Unused I/O	BFFF 9004									
Write	Control Latch # 2	9003	Display Mode	BOW/ WOB	Bell	Timeout Blank	Keyclick On/Off	DTR	Monitor Mode	Spare	Printer
Read	Dipswitch Port # 2	9002	SP/MK	O/E	Par.	BOW/ WOB	Baud Rate 3	Baud Rate 2	Baud Rate 1	Baud Rate 0	
Read	Dipswitch Port # 1	9001	Stop Bits	Edit	Word Length	925/ 920	Baud Rate 3	Baud Rate 2	Baud Rate 1	Baud Rate 0	Main
Write	Control Latch # 1	9000	CPU Reset	Exten.	Bi-Direc.	925/ 920ATT	60/ 50Hz	Cursor Under	Blink Clock	Page Print	
——	Spare	8070									
Read/Wr	Control Register	8063	Stop Bits	Word Lnth 1	Word Lnth 0	Rcvr Clk Source	Baud Rate 3	Baud Rate 2	Baud Rate 1	Baud Rate 0	ACIA #2 (Keybd) I/O
Read/Wr	Command Register	8062	Par.2	Par.1	Par.0	Norm/ Echo	Xmit 1	Xmit 0	RCV IRQ	DTR	
Read/Wr	Status Register	8061	Read: Status Register				Write: Program Reset(No Data)				
Read/Wr	Transmit or Receive Data	8060	Read: Receive Register				Write: Transmitter Register				
Read	Dipswitch Port # 5	8050	Not Used		Cursor 1	Cursor 0	DTR	SRTS	Not Used		
Write	Reset IRQ	8040	NO DATA								
Read/Wr	Control Register	8033	Stop Bits	Word Lnth 1	Word Lnth 0	Rcvr Clk Source	Baud Rate 3	Baud Rate 2	Baud Rate 1	Baud Rate 0	ACIA #1 (Host)
Read/Wr	Command Register	8032	Par.2	Par.1	Par.0	Norm/ Echo	Xmit 1	Xmit 0	Rcv IRQ	DTR	
Read/Wr	Status Register	8031	Read: Status Register				Write: Program Reset(No Data)				
Read/Wr	Transmit or Receive Reg.	8030	Read: Receive Register				Write: Transmit Register				
Read/Wr	Read or Write Regs 0-31	8021			DISPLAY PARAMETERS						CTRC
Write	Address Register (Contains Reg. Number)	8020			REGISTER NUMBER						
Read	Dipswitch Port # 4	8010	Char Set 1	Char Set 0	Not Used		Keyclick On/Off	Test	Not Used		
Read	Dipswitch Port # 3	8000	Not Used		Line/Pg Att.	Timeout Blank	60/ 50Hz	CR/ CR-LF	Comm Mode 1	Comm Mode 0	
	Unused Display RAM	7FFF 4C00									Disp RAM
	Page 2	4BFF 4800									
	Page 1	47FF 4000									
	Unused Sys. RAM	3FFF 0400									Sys. RAM
		03FF 0000			VARIABLE PROGRAM DATA						

925 MEMORY MAP

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	PROD REL PER ECO 42		
	B	" " ECO 43		
	C	" " ECO 44		
	D	" " ECO 46		

NOTES:-UNLESS OTHERWISE SPECIFIED

1. VERSION -001 AND -002
2. VERSION -002 ONLY
3. CIRCUITRY OPTIONAL



APPLICATION		UNLESS OTHERWISE NOTED	DWN O. Cavallero 10-1-80
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK O. Cavallero 10-2-80
		ANG 2 PLC 3 PLC	ENGR [illegible] 10-2-80
			APPD
		SCALE NONE	APPD
		MATERIAL	FINISH

B600003-001

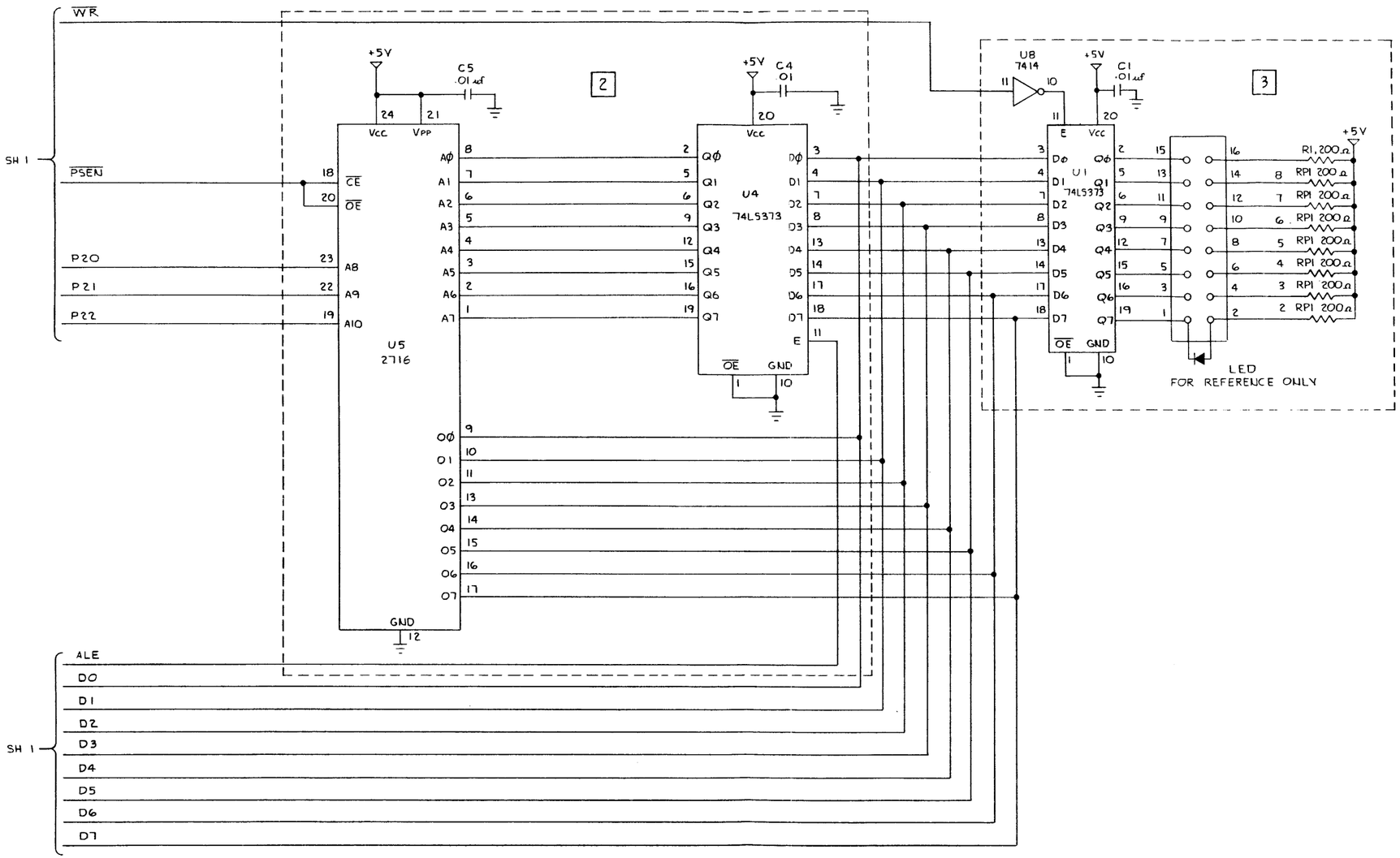
TeleVideo, Inc.

TITLE PCB SCHEMATICS 950 KEYBOARD

SIZE D | SHT 1 OF 2 | DRAWING NO 2010300 | REV D

D | 20103-00

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	D	SEE SHT 1		



APPLICATION		UNLESS OTHERWISE NOTED	DWN Cavallaro 10-2-80	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK Cavallaro 10-2-80	TITLE PCB SCHEMATIC 950 KEYBOARD
		ANG ± 2 PLC ± .3 PLC ±	ENGR	
			APPD	
		SCALE NONE	APPD	
		MATERIAL	FINISH	SIZE D SHT 2 OF 2 DRAWING NO 2010300 REV D

20103-00

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED
	A	PROD REL PER ECO 42		
	B	" " ECO 43		
	C	" " ECO 44		
	D	" " ECO 46		
	D1	ADD 7406 TO U7 ECO 30004	3/22/84	

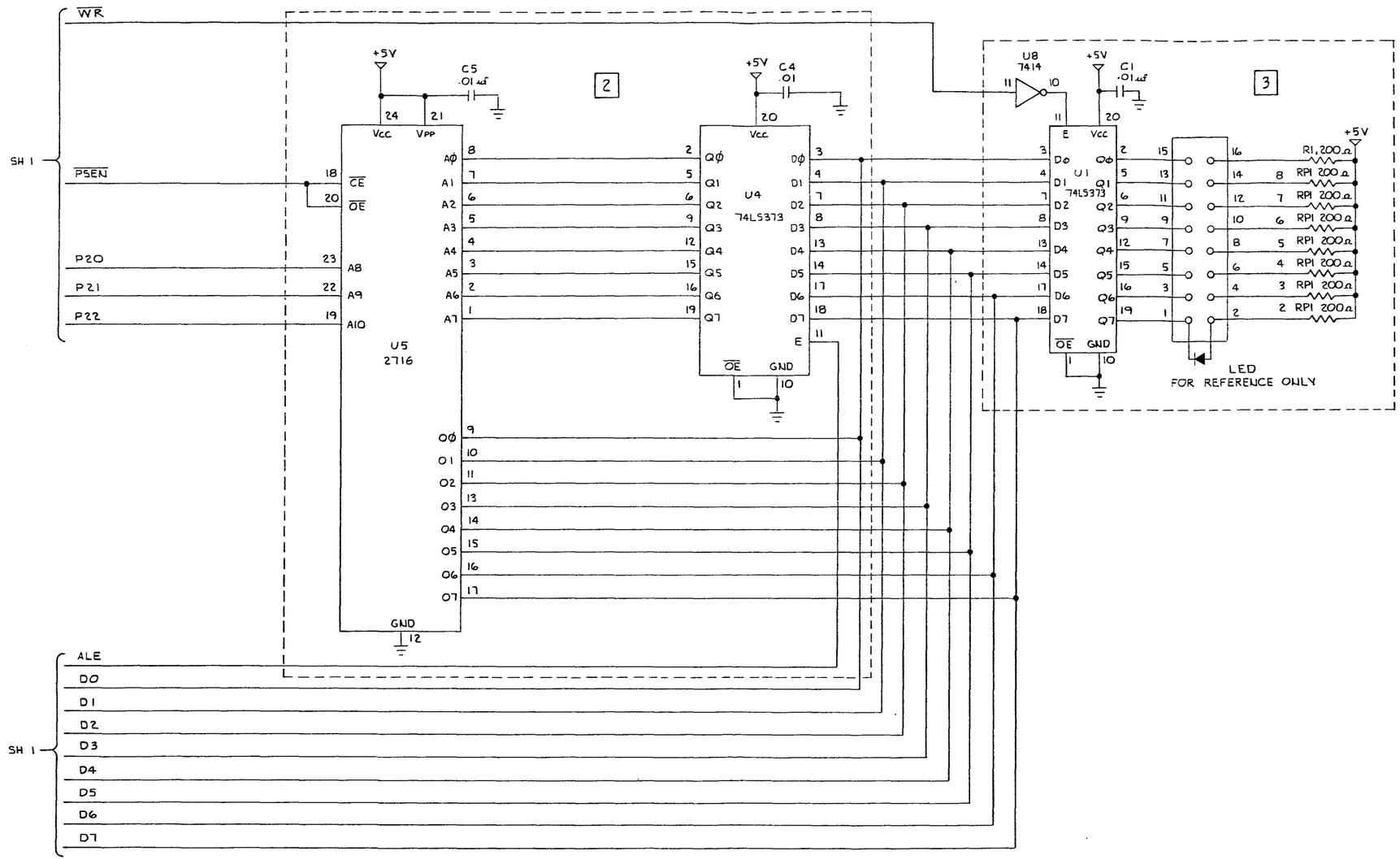
NOTES:-UNLESS OTHERWISE SPECIFIED

1. VERSION -00 AND -01
2. VERSION -01 ONLY
3. CIRCUITRY OPTIONAL

B600003-001

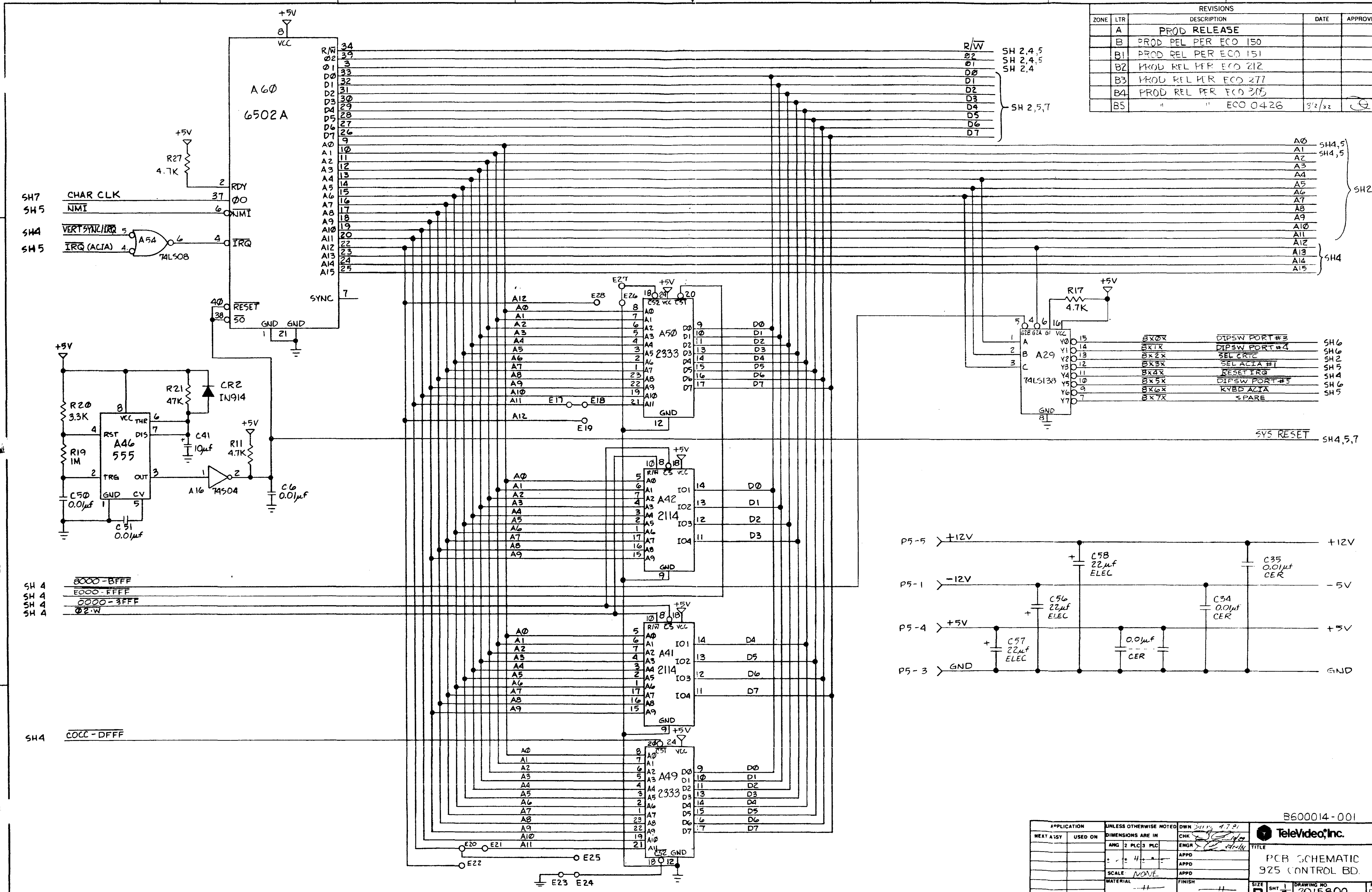
APPLICATION		UNLESS OTHERWISE NOTED	DWN G. Gonzales 10-1-80	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK A. Gomez 10-2-80	
		ANG ± PLC.3 PLC	ENGR	TITLE PCB SCHEMATICS 950 KEYBOARD
			APPD	
		SCALE 1/1 SIZE	APPD	
		MATERIAL	FINISH	SIZE D SHT OF DRAWING NO 120103-00 REV 21

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	D	SEE SHT 1		



APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN		DWN Casallano 10-2-80	TeleVideo, Inc.
NEXT ASSY	USED ON	ANG ± 2 PLC ± 3 PLC		CHK Casallano 10-2-80	TITLE PCB SCHEMATIC 950 KEYBOARD
				ENGR [illegible] 10-2-80	
				APPD	
		SCALE NONE		APPD	
		MATERIAL		FINISH	SIZE D SHT 1 OF 2 DRAWING NO 120103-CC REV -1

D 20103-00



REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	PROD RELEASE		
	B	PROD REL PER ECO 150		
	B1	PROD REL PER ECO 151		
	B2	PROD REL PER ECO 212		
	B3	PROD REL PER ECO 277		
	B4	PROD REL PER ECO 305		
	B5	" " ECO 0426	3/2/82	

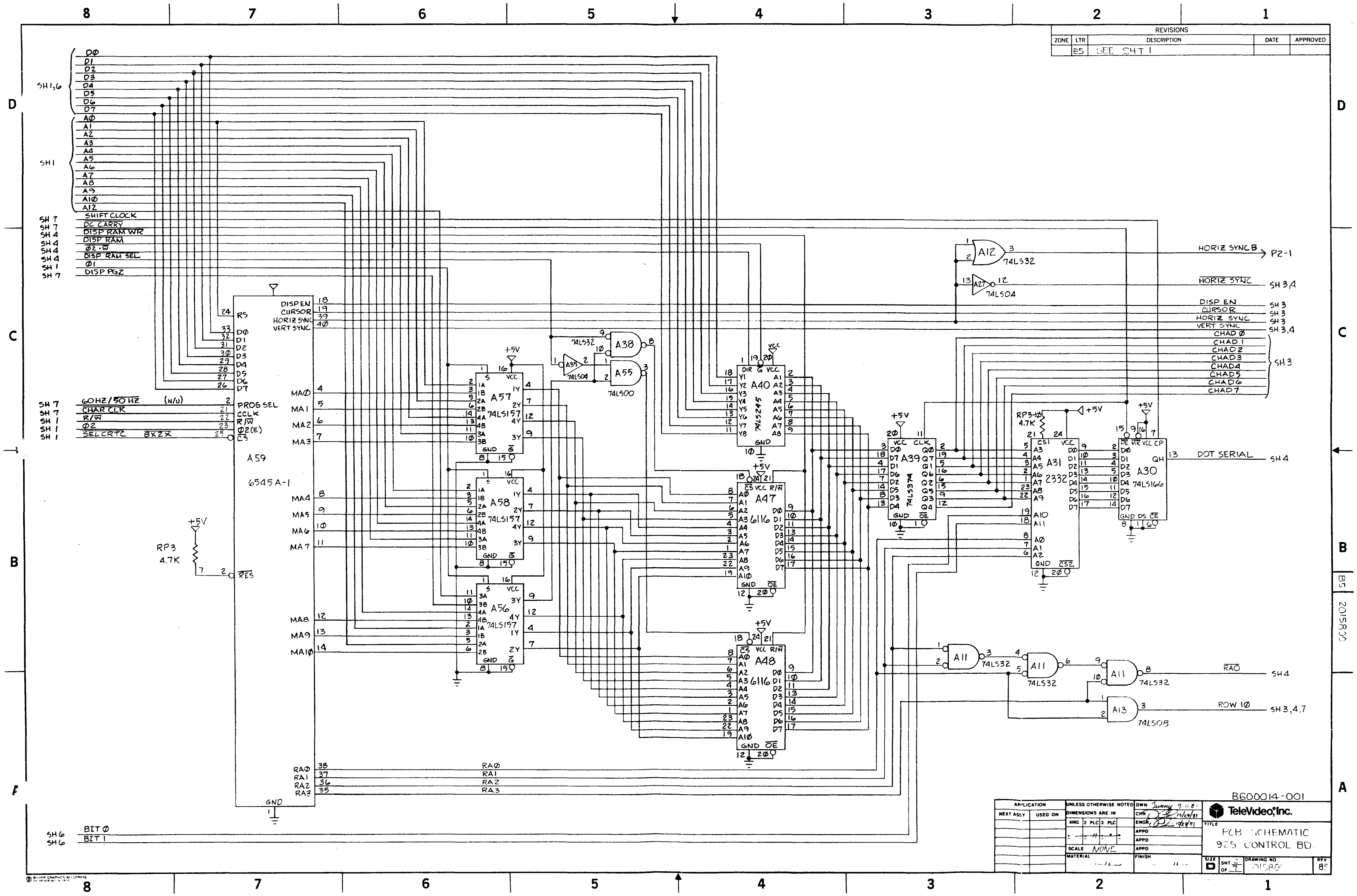
B600014-001

TeleVideo® Inc.

TITLE: PCB SCHEMATIC 925 CONTROL BD.

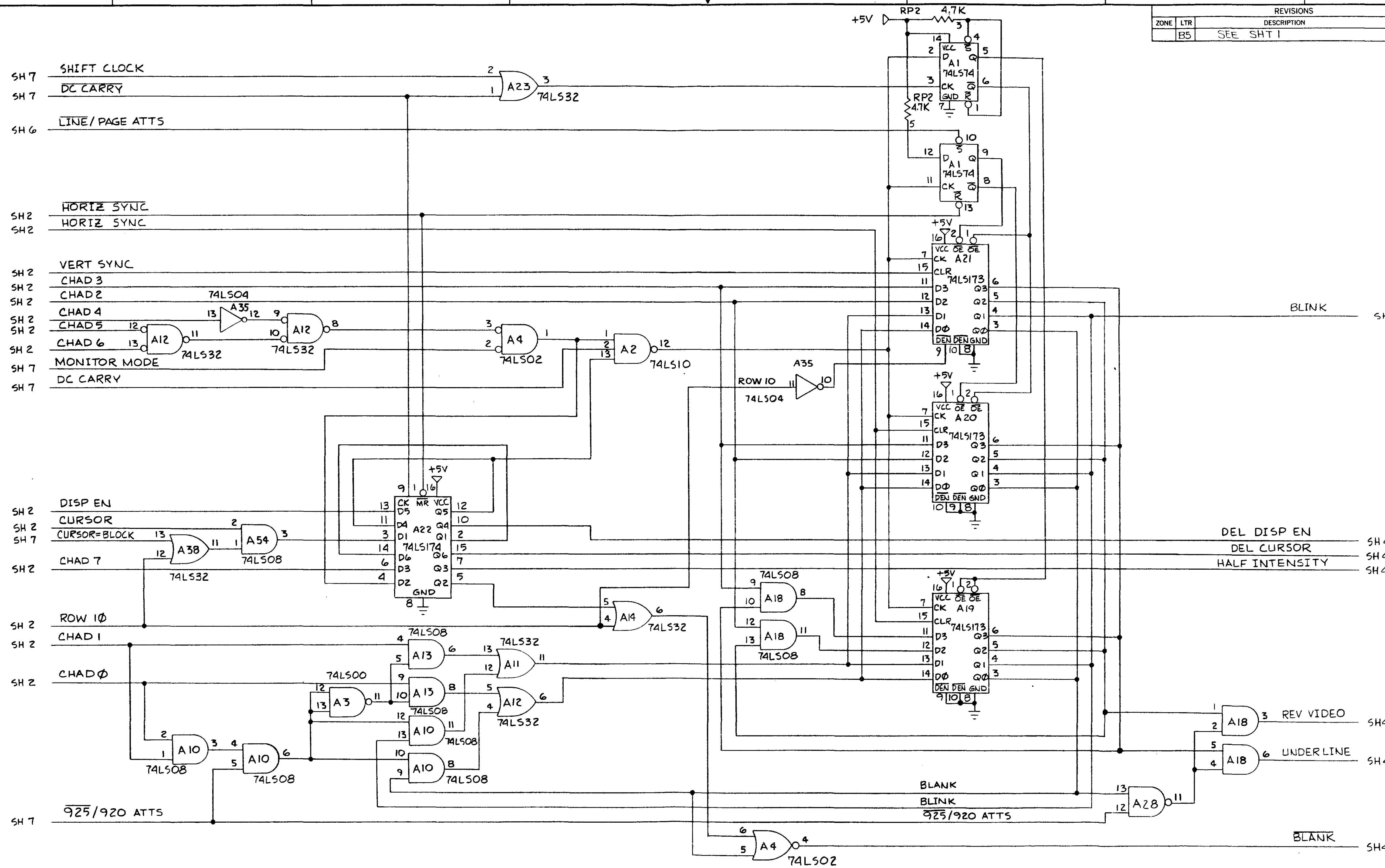
SIZE D | SHT 1 OF 7 | DRAWING NO 2015800 | REV B5

SCALE NONE



REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
B5 SEE SHT 1
SH 1,6
D0 D1 D2 D3 D4 D5 D6 D7
SH 1
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A12
SH 7 SHIFT CLOCK
SH 7 DC CARRY
SH 4 DISP RAM WR
SH 4 DISP RAM
SH 4 Ø2·W
SH 4 DISP RAM SEL
SH 1 Ø1
SH 7 DISP PGZ
SH 7 60HZ/50HZ (N/U)
SH 7 CHAR CLK
SH 1 R/W
SH 1 Ø2
SH 1 SELCRTC 8X2X
A59
6545A-1
RP3 4.7K
+5V
A57 74LS157
A58 74LS157
A56 74LS157
A38 74LS32
A55 74LS00
A35 74LS04
A40 74LS245
A47 6116
A48 6116
A39 74LS374
A31 2332
A30 74LS166
RP3-10 4.7K
A12 74LS32
A27 74LS04
A11 74LS32
A13 74LS08
HORIZ SYNC B P2-1
HORIZ SYNC SH 3,4
DISP EN SH 3
CURSOR SH 3
HORIZ SYNC SH 3
VERT SYNC SH 3,4
CHAD 0 CHAD 1 CHAD 2 CHAD 3 CHAD 4 CHAD 5 CHAD 6 CHAD 7 SH 3
DOT SERIAL SH 4
RA0 SH 4
ROW 10 SH 3,4,7
RA0 RA1 RA2 RA3
SH 6 BIT 0
SH 6 BIT 1
B600014-001
TeleVideo, Inc.
TITLE PCB SCHEMATIC 925 CONTROL BD.
SCALE NONE
SIZE D SHT 2 OF 7 DRAWING NO 2015800 REV B5

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B5	SEE SHT 1		



B600014-001

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN Sunny 10-22-81	TeleVideo, Inc.
NEXT ASSY	USED ON	ANG / 2 PLC / 3 PLC	CHK 10-29-81	TITLE PCB SCHEMATIC 925 CONTROL BD
		SCALE: NONE	ENGR	
			APPD	
		MATERIAL	FINISH	SIZE D · SHT 3 OF 7 · DRAWING NO. 2015800 · REV B5

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B5	SEE SHT 1		

SH 3 BLINK
SH 7 BLINK CLK
SH 2 SH 3 RAO / BLANK
SH 2 DOT SERIAL
SH 2 ROW 10
SH 3 UNDERLINE
SH 7 TIMEOUT BLANK
SH 3 DEL CURSOR
SH 3 REV VIDEO
SH 7 BOW / WOB
SH 3 DEL DISP EN
SH 3 HALF INTENSITY
SH 2 HORIZ SYNC
SH 2 VERT SYNC
SH 1 SH 1 RESET IRQ (8x4x) / A13
SH 1 A14
SH 1 A15
SH 1 A0
SH 1 A1
SH 1 A12
SH 1 Ø2
SH 1 R/W
SH 1 Ø1
SH 7 SET DISP RAM
SH 1 SYS RESET
SH 7 CHAR CLK

74LS00 A3, A2 · 74LS10 · A16 74S04 · A55 74LS00 · A3 74LS00 · A15 74LS86 · A15 74LS86 · A5 7406 · A5 7406 · A27 74LS04 · A5 7406 · A5 7406 · A16 74S04 · A15 74LS86 · A5 7406 · A35 74LS04 · A28 74LS00 · A14 74LS32 · A37 74LS139 · A55 74LS00 · A35 74LS04 · A54 74LS08 · A55 74LS00 · A35 74LS04 · A4 74LS02 · A36 74LS32 · A6 74LS74 · A36 74LS32 · A36 74LS32 · A36 74LS32 · A23 74LS32

RP3 4.7K · A6 74LS74 · RP3 4.7K

E3 E4 · R7 750 · R5 1K · R2 22 · +5V · C3 4.7µf · VIDEO SHIELD GND → P2-3 · R4 1K · R8 270 · CR1 IN914 · Q1 2N2219 · R3 68 · VIDEO → P2-4 · E1 · R9 1K · E2 · COMP V+TTL VIDEO → P2-6 · VERT SYNC → P2-5

VERT SYNC / IRQ → SH 1
E000-FFFF → SH 1
C000-DFFF → SH 1
9xx0
9xx1 DIPSWITCH PORT #1 → SH 6
9xx2 DIPSWITCH PORT #2 → SH 6
9xx3
8000-BFFF → SH 1
0000-3FFF → SH 1
DISP RAM SEL → SH 2
CONTROL LATCH #1 → SH 7
CONTROL LATCH #2 → SH 7
Ø2 · W → SH 1,2
DISP RAM WR → SH 2
DISP RAM → SH 2

APPLICATION		UNLESS OTHERWISE NOTED	DWN Sunny 10-22-81
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK
		ANG 2 PLC 3 PLC	ENGR
		± ± ±	APPD
		SCALE NONE	APPD
		MATERIAL	APPD
			FINISH

B600014-001

TeleVideo, Inc.

TITLE PCB SCHEMATIC 925 CONTROL BD

SIZE D · SHT 4 OF 7 · DRAWING NO 2015800 · REV B5

B5 2015800

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B5	SEE SHT 1		

P4-4 RTS E5
P4-11 HSHAKE E6 E7
P3-18 TEST E8 E9
P3-6 DSR 12 S3 9
P4-20 DTR E10 E11

+5V
R P2 4.7K
A17 75189
C20 C22 C23 C21 330pf (4)

SH7 EXTENSION

+5V
RP2 4.7K
A9 75189
P3-8 DCD 13 S3 8
P3-5 CTS
P3-3 RxD
P6-3 RxD
P4-2 SERIAL DATA FROM PRINTER
C11 C13 C12 C10 330pf

SH7 DTR
SH7 BI-DIRECTIONAL
SH7 PAGE PRINT

SH1 SEL ACIA (8x3x)
SH1 R/W
SH1 Ø2
SH1 AØ
SH1 A1
1,2,6 DØ D1 D2 D3 D4 D5 D6 D7

A32 ACIA #1 6551A-1
DSR CSØ VCC
DCD CTS RxD CS1 R/W Ø2 RSØ RS1 DØ D1 D2 D3 D4 D5 D6 D7 CS1 RST GND
TxD RTS IRQ RxC XTAL1 XTAL2

A33 ACIA #2 6551A-1
CSØ VCC
R/W Ø2 RSØ RS1 DØ D1 D2 D3 D4 D5 D6 D7 CS1 RST GND
XTAL1 XTAL2 IRQ RxC TxD CTS DCD DSR RxD

+5V R28 10K
+5V RP3 4.7K
Y1 OPTIONAL
Y3 OPTIONAL
C31 10pf
R18 3.3K
C32 10pf
Y1 1.8432 MHZ
+5V RP3 4.7K

IRQ (ACIA) SH1
RxC P6-12
NMI SH1,7

SH1 KYBD ACIA (8x6x)
P0-3
P1-3
C8 330 pf
A13 74LS08
SH1 SYS RESET

A28 A26 A27 A14 74LS32 74LS04 74LS08

HSHAKE SH6
TEST SH6
DTR SH6

A25 75188
HSHAKE P3-11
DSR P4-6
DCD P4-8
CTS P4-5
C62 C66 C63 C65 330 pf

A34 75188
E15 E16 E14
DTR EN S3 P3-20
TxD P3-2
TxD MODEM P6-2
SERIAL DATA TO PRINTER P4-3
RTS P3-4
C67 C69 C64 C68 330 pf

B600014-001

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN Sunny 10-18-81	TeleVideo, Inc.
NEXT ASSY	USED ON	ANG 2 PLC 3 PLC	CHK 10/19/81	TITLE PCB SCHEMATIC 925 CONTROL BD
			ENGR 10/19/81	
		SCALE 1/2 VP	APPD	
		MATERIAL	FINISH	SIZE D SHT 5 OF 7 DRAWING NO 205800 REV B5

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B5	SEE SHT 1		

SH1 DIPSWITCH PORT #5
SH1 DIPSWITCH PORT #4
SH1 DIPSWITCH PORT #3
SH4 DIPSWITCH PORT #2
SH4 DIPSWITCH PORT #1

RP5 4.7K
+5V
R23 4.7K

S1
BD RT 3
BD RT 2
BD RT 1
BD RTØ
WD LENGTH
STOP BITS

EDIT
920/925
BD RT3
BD RT2
BD RT1
BD RTØ
PAR 2
PAR 1
PAR Ø
BOW/WOB
COMM MODE Ø
COMM MODE 1
50/60 HZ
CR/CR-LF

S2

R1 4.7K +5V

RP1 4.7K +5V

RP4 4.7K +5V

S3
TIMEOUT BLANK ENABLE
LINE/PAGE ATTRIBUTES
KEY CLICK
CHAR SET 1
CHAR SET Ø
CURSOR 1
CURSOR Ø

SH5 DTR
SH5 TEST
SH5 HSHAKE

A53 74LS244: A0→DØ, A1→D1, A2→D2, A3→D3, A7→D5, A6→D7, A5→D6, A4→D4
A52 74LS244: A0→D3, A1→D2, A2→D1, A3→DØ, A7→D7, A6→D6, A5→D5, A4→D4
A51 74LS244: A0→DØ, A1→D1, A2→D3, A3→D2, A7→D4, A6→D5
A43 74LS244: A0→D3, A1→D7, A2→D6, A3→D5, A7→D4, A6→D3, A5→D2, A4→D2

DØ D1 D2 D3 D4 D5 D6 D7 → SH 2,5,7

LINE/PAGE ATTRIBUTES SH3
BIT 1 SH2
BIT Ø SH2

8600014-001

APPLICATION		UNLESS OTHERWISE NOTED	DWN Sunny 10.20.81	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK 10/20/81	
		ANG 2 PLC 3 PLC	ENGR 10/20/81	TITLE PCB SCHEMATIC 925 CONTROL BD
		SCALE NONE	APPD	
		MATERIAL	FINISH	SIZE D SHT 6 OF 7 DRAWING NO 2015800 REV B5

B5 2015800

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B5	SEE SHT1		

Y2 XTAL 13.608 MHZ
C18 10pF
R15 330
R12 750
R19 1.8K
R13 470
A16 74S04
E13
E12
+5V
RP3 4.7K
A24 74LS163
A27 74LS04
A2 74LS10
A4 74LS02
A16 74S04

SHIFT CLOCK — SH 2,3
DC CARRY — SH 2,3
DC CARRY — SH 3
SET DISP RAM — SH 4
CHAR CLK — SH 2,4
CHAR CLK — SH 1

SH1 SYS RESET
SH 4 CONTROL LATCH #1
SH 4 CONTROL LATCH #2
SH1,2,6 D0 D1 D2 D3 D4 D5 D6 D7
A95 74LS273

PAGE PRINT — SH5
BLINK CLOCK — SH4
CURSOR=BLOCK — SH3
60/50 HZ — SH2
925/920 ATTS — SH3
BI-DIRECTIONAL — SH5
EXTENSION — SH5
CPU RESET — (NOT USED)

A94 74LS273

MONITOR MODE — SH3
DTR — SH5
TIMEOUT BLANK — SH4
BOW/WOB — SH4
DISPLAY PAGE 2 — SH2

BELL
KEYCLICK ON/OFF
R16 51K
C4 1μf
R10 4.7K
R25 330
R24 330
C61 10 Uf
Q2
R26 330
74LS32
A38
A28 74LS00
A5 7406
A54 74LS08

SH5 NMI
SH2 ROW 10
P6-13 SPEAKER (FROM INTERNAL MODEM)

P7-1
P7-2
P0-4
P1-4

P0-1
P1-1
P0-2
P1-2
+12V
C27 0.01
C47 0.01
C9 330pf

NOTE:
P6 IS A 14- OR 16-PIN DIP SOCKET FOR OPTIONAL BOARD CONNECTION.
* PINS 0 & 15 ARE PINS 1 & 16 IF A 16-PIN SOCKET IS INSTALLED FOR P6.

+12V — P6-1, P6-14
-12V — P6-5, P6-10
+5V — P6-6, P6-9, P6-7, P6-8

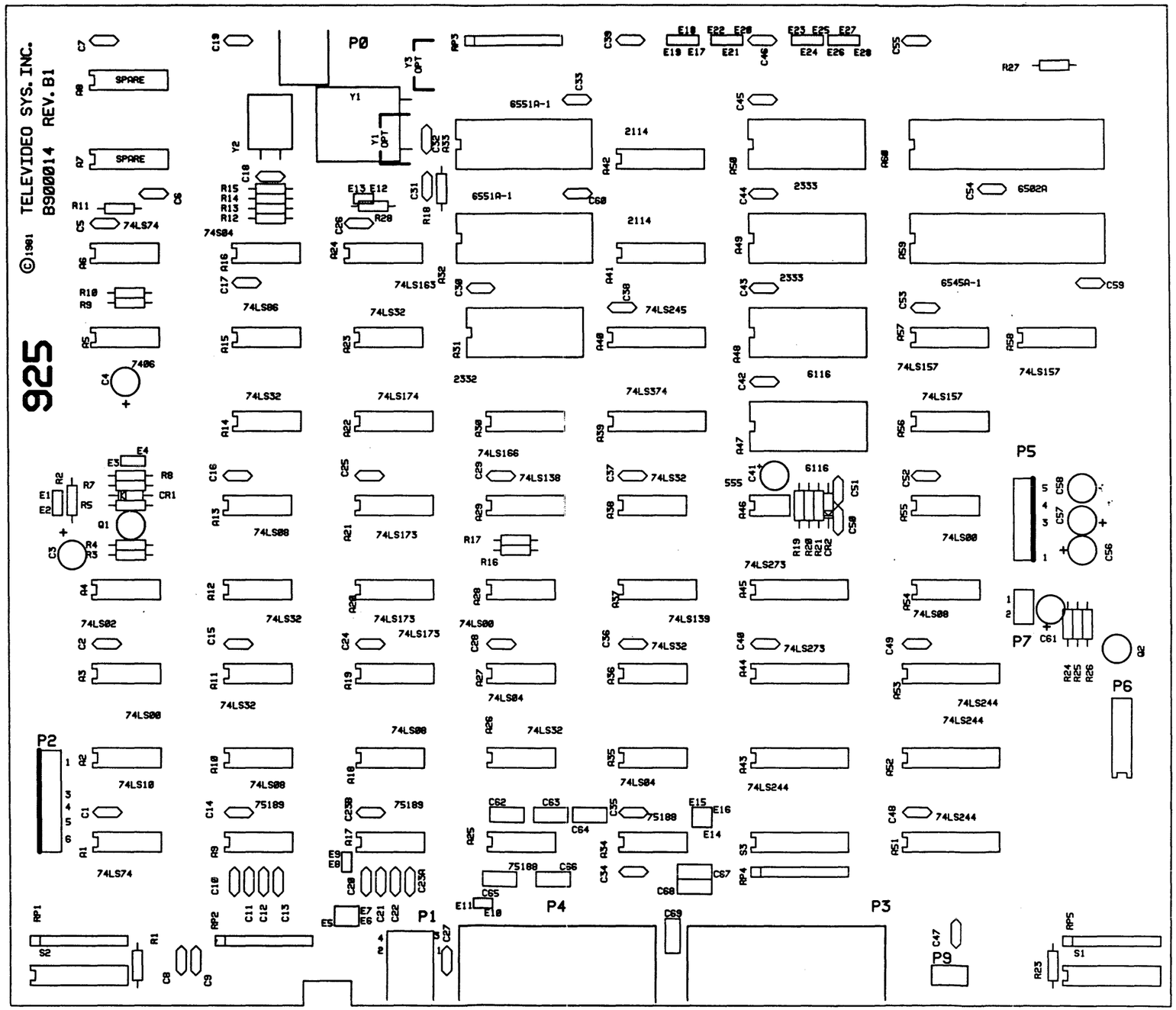
P3-12 RxD+ — P6-15*
P3-24 RxD- — P6-0*
P6-11 TxD+ — P3-25
P6-4 TxD- — P3-13
CURRENT LOOP COMM (OPTIONAL)

P9-1, P9-2, P3-1, P4-1 — CHASSIS GND
P3-7, P4-7 — LOGIC GND

B600014-001

APPLICATION		UNLESS OTHERWISE NOTED	DWN Swagg 10-21-81	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK 10/22/81	
		ANG 2 PLC 3 PLC	ENGR 10/22/81	TITLE PCB SCHEMATIC 925 CONTROL BD
			APPD	
		SCALE NONE	APPD	
		MATERIAL	FINISH	SIZE D SHT 7 OF 7 DRAWING NO 7000280 REV B5

B5 2015800


©1981 TELEVIDEO SYS. INC.
B900014 REV.B1
925
P0
P1
P2
P3
P4
P5
P6
P7
P9
SPARE
SPARE
74LS74
7406
74S84
74LS86
74LS32
74LS163
6551A-1
2114
2333
6116
6502A
6545A-1
74LS245
74LS157
74LS374
74LS166
74LS138
74LS174
74LS173
74LS88
74LS139
74LS273
74LS244
74LS10
74LS02
75189
Y1
Y2
Y3
Y1 OPT
Y3 OPT
925
CONTROL
BOARD
REV B

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	PROD REL PER ECO 235	3/3/82	
	A1	" " ECO 0370,0410,0426		
	A2	" " ECO 437		
	A3	" " ECO 0530		

A11 6502A

A8 74LS08

A13 74LS138

A14 2333

A15 2333

A9 2114

A10 2114

A6 555

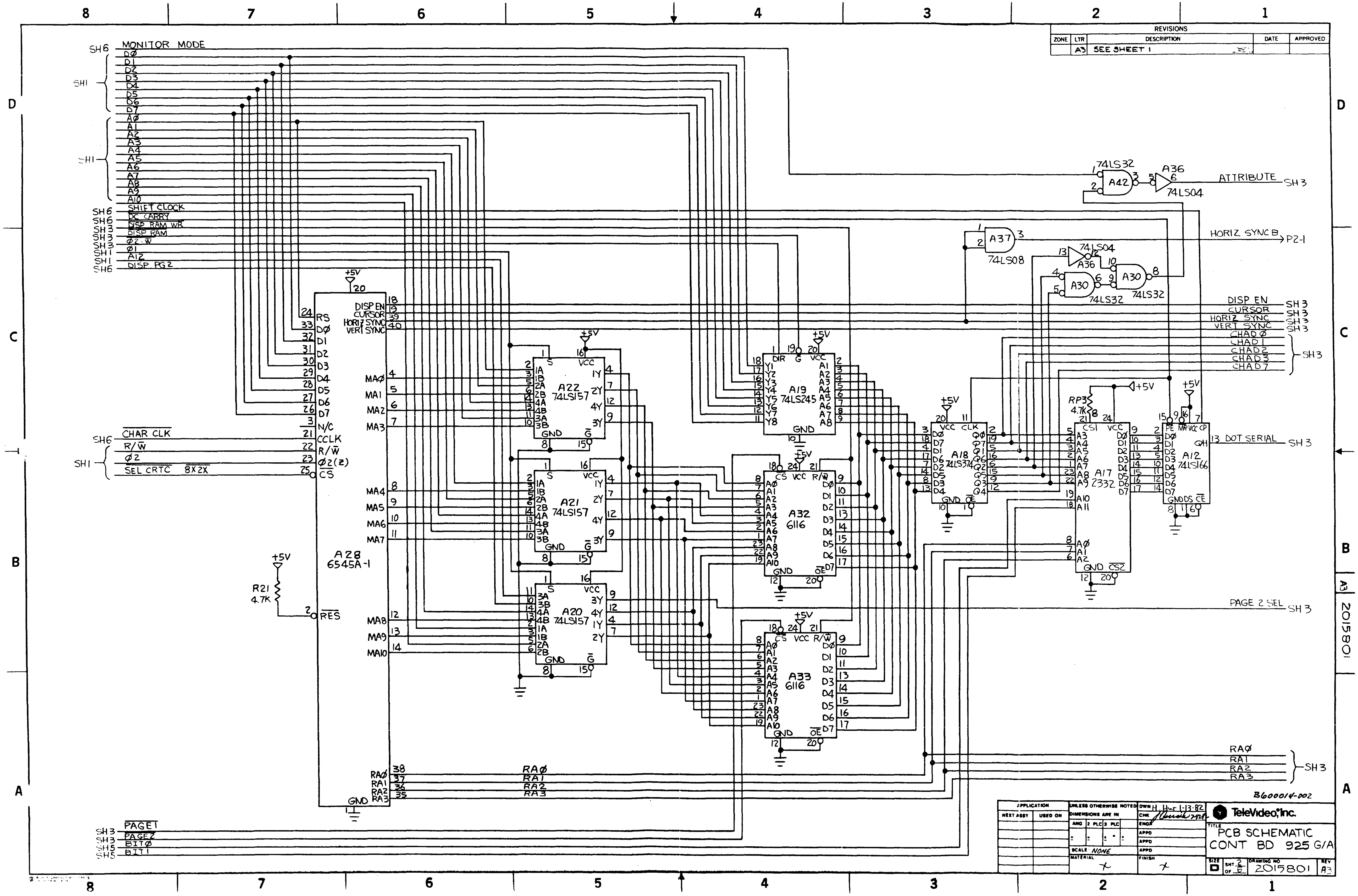
A31 7406

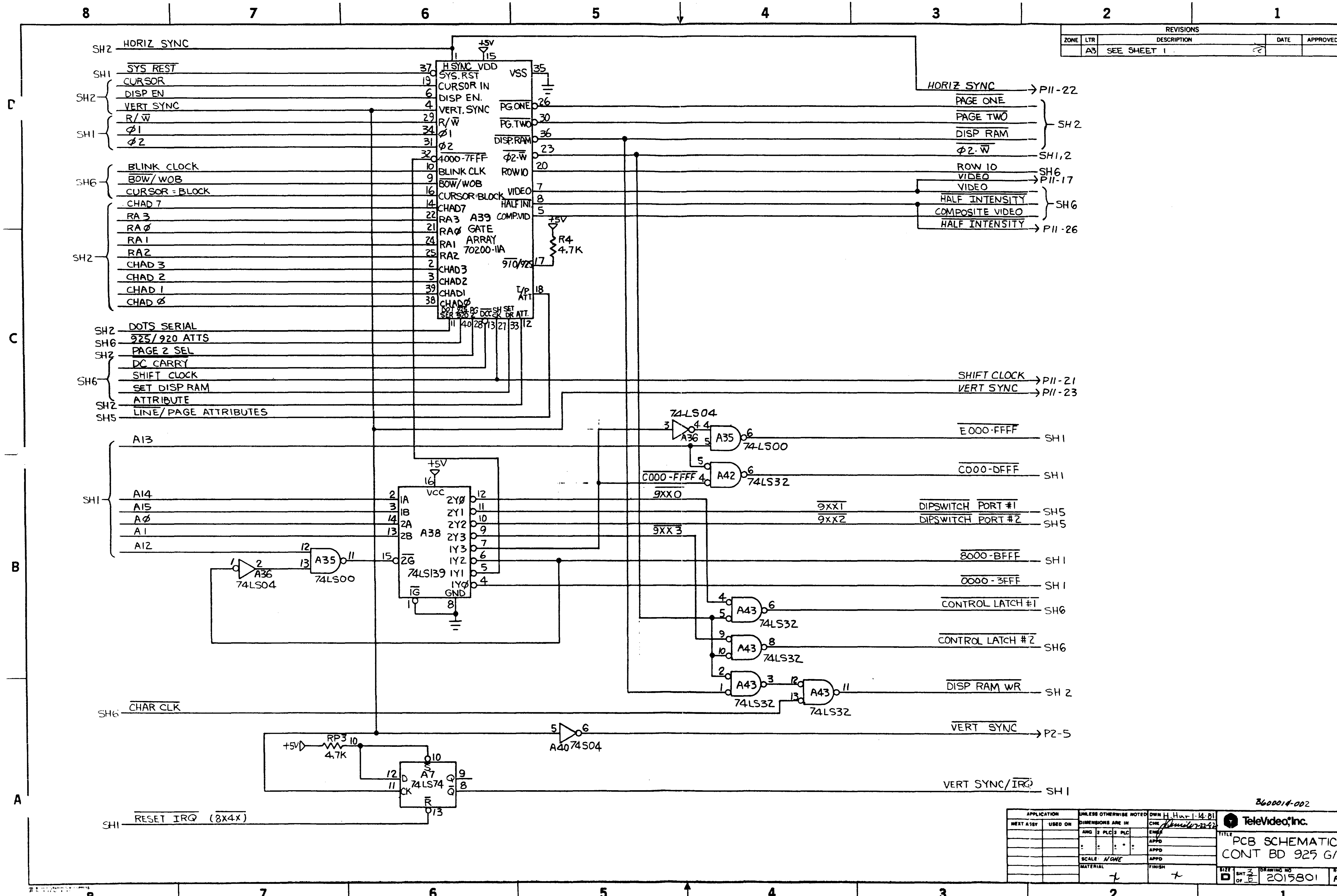
NOTES UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE VALUED IN OHMS ±5 % AND ARE 1/4 WATT.
2. ALL CAPACTOR ARE VALUED IN MICOFARADS ±10% AND ARE 50 VDC.
3. DRAWINGS COMFORMS WITH TELEVIDEO SPEC. NO S000000-001.
4. P6 IS A 14-OR 16-PIN DIP SOCKET FOR OPTIONAL BOARD CONNECTION
5. PINS Ø&15 ARE PINS 1&16 IF A 16-PIN SOCKET IS INSTALLED FOR P6.

B6000/4-002

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN						TeleVideo, Inc.
NEXT ASSY	USED ON	ANG	2 PLC	3 PLC		DWN H. Hyer 1-12-82		
		:	:	:	:	CHK	3/3/82	TITLE
		SCALE NONE				ENGR	3/4/82	PCB SCHEMATIC CONT BD 925 G/A
		MATERIAL				APPD	3/4/82	
						APPD		
						APPD		
						FINISH		SIZE D SHT 1 OF 6 DRAWING NO 2015801 REV A


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A3 SEE SHEET 1
MONITOR MODE
SH6
SH1
D0 D1 D2 D3 D4 D5 D6 D7
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10
SHIFT CLOCK
DC CARRY
DISP RAM WR
DISP RAM
Ø2·W
Ø1
A12
DISP PG2
CHAR CLK
R/W
Ø2
SEL CRTC
8X2X
A28
6545A-1
RS
CCLK
CS
RES
DISP EN
CURSOR
HORIZ SYNC
VERT SYNC
MA0 MA1 MA2 MA3 MA4 MA5 MA6 MA7 MA8 MA9 MA10
RA0 RA1 RA2 RA3
R21
4.7K
+5V
A22 74LS157
A21 74LS157
A20 74LS157
A19 74LS245
A32 6116
A33 6116
A18 74LS374
A17 2332
A12 74LS166
RP3 4.7K
74LS32 A42
A36 74LS04
ATTRIBUTE
A37 74LS08
HORIZ SYNC B
P2-1
A30 74LS32
DISP EN
CURSOR
HORIZ SYNC
VERT SYNC
CHAD 0
CHAD 1
CHAD 2
CHAD 3
CHAD 7
SH3
DOT SERIAL
PAGE 2 SEL
PAGE 1
PAGE 2
BIT 0
BIT 1
SH5
B600014-002
APPLICATION
NEXT ASSY
USED ON
UNLESS OTHERWISE NOTED DIMENSIONS ARE IN
SCALE NONE
MATERIAL
FINISH
DWN 1-13-82
TeleVideo, Inc.
TITLE
PCB SCHEMATIC
CONT BD 925 G/A
SIZE D
SHT 2 OF 6
DRAWING NO 2015801
REV A3
2015801



TeleVideo, Inc.

PCB SCHEMATIC CONT BD 925 G/A

SIZE D SHT 3 OF 6 DRAWING NO 2015801 REV A3

SCALE NONE

DWN H. Har 1-14-81

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A3	SEE SHEET 1		

P4-4 RTS E5
P4-11 HSHAKE E6 E7
P3-18 TEST E8 E9
P3-6 DSR 12 S3 9
P4-20 DTR E10 E11

+5V
RP3 4.7K
A1 75189
C9 330PF 100V
C7 330PF 100V
C6 330PF 100V
C8 330PF 100V

SH6 EXTENSION

P3-8 DCD S3
P3-5 CTS
P3-3 RXD
P6-3 RXD
P4-2 SERIAL DATA FROM PRINTER

+5V
RP3 4.7K
A2 75189
C2 330PF 100V
C3 330PF 100V
C5 330PF 100V
C4 330PF 100V

SH6 DTR
SH6 BI-DIRECTIONAL
SH6 PAGE PRINT
P10-11
P10-9

SEL ACIA (8X3X)
SH1 R/W Ø2 AØ A1 DØ D1 D2 D3 D4 D5 D6 D7

E29
E30
A4 ACIA#1 6551A-1
DSR CSØ VCC
DCD TXD
CTS RTS
RXD
CST
R/W
Ø2
RSØ
RS1
DØ D1 D2 D3 D4 D5 D6 D7
RST GND
IRQ RXC XTALI XTAL2

+5V
RP4 4.7K
A31 7406
A35 74S04
A40 74S04
74LS32
A24 74LS32
A30 74LS32
A36 74LS04
A24 74LS32
A24 74LS32
E31 E32

75188
A16
A23
75188
E15 E16 E14
DTREN
S3
C10 330PF 100V
C17 330PF 100V
C15 330PF 100V
C16 330PF 100V

HSHAKE SH5
TEST SH5
DTR SH5
HSHAKE P3-11
DSR P4-6
DCD P4-8
CTS P4-5
C14 330PF 100V
C13 330PF 100V
C11 330PF 100V
C12 330PF 100V
TXD P3-2
TXD MODEM P6-2
SERIAL DATA TO PRINTER P4-3
RTS P3-4
P10-5
P10-7/10
IRQ (ACIA) SH1
RXC P6-12
P10-13

R13 4.7K +5V
Y1 OPTIONAL
C23 10pf
R16 1K
C22 10pf
Y1 1.8432 MHZ
R17 10K +5V
Y3 OPTIONAL
+5V
R15 4.7K
NMI SH1,6

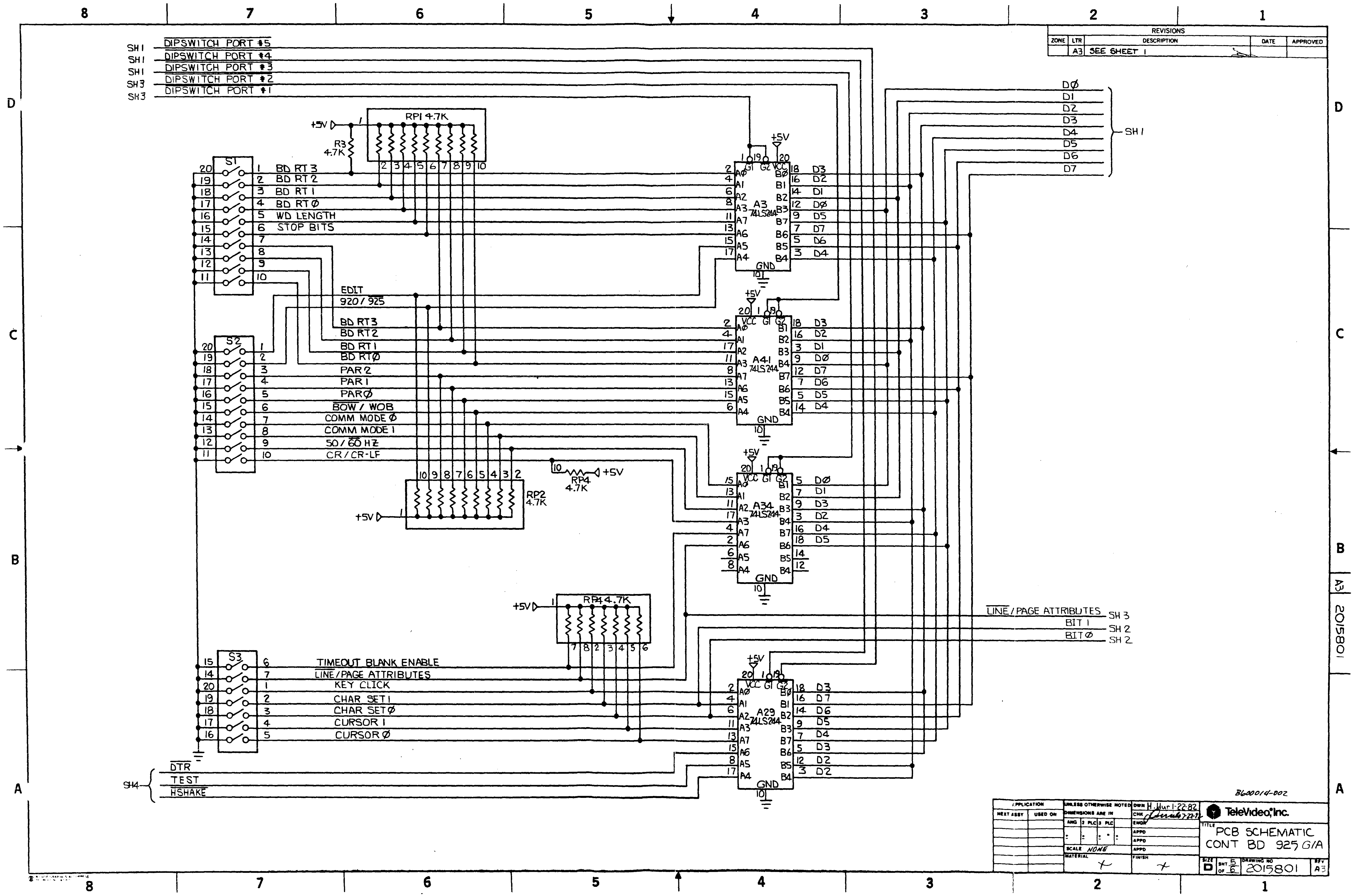
A5 ACIA#2 6551A-1
CSØ VCC
R/W XTALI
Ø2
RSØ
RS1 XTAL2
DØ D1 D2 D3 D4 D5 D6 D7
CS1
IRQ RXC TXD CTS DCD DSR
RXD RST GND

SH1 KYBD ACIA (8X6X)
PØ-3
P1-3
C1 330pf 100V
A8 74LS08
SH1 SYS RESET

86000114-002

APPLICATION		UNLESS OTHERWISE NOTED	DWN H. Li 1-21-82	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK	
		ANG ± PLC ± PLC ±	ENGR	TITLE PCB SCHEMATIC CONT BD 925 G/A
		SCALE: NONE	APPD	
		MATERIAL —	FINISH —	SIZE D SHT 4 OF 6 DRAWING NO 2015801 REV A3

A3 2015801



REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A3 SEE SHEET 1
SH1 DIPSWITCH PORT #5
SH1 DIPSWITCH PORT #4
SH1 DIPSWITCH PORT #3
SH3 DIPSWITCH PORT #2
SH3 DIPSWITCH PORT #1
RP1 4.7K
R3 4.7K
+5V
S1
BD RT3
BD RT2
BD RT1
BD RTØ
WD LENGTH
STOP BITS
EDIT
920/925
S2
BD RT3
BD RT2
BD RT1
BD RTØ
PAR2
PAR1
PARØ
BOW / WOB
COMM MODE Ø
COMM MODE 1
50/60 HZ
CR/CR-LF
RP2 4.7K
RP4 4.7K
S3
TIMEOUT BLANK ENABLE
LINE/PAGE ATTRIBUTES
KEY CLICK
CHAR SET 1
CHAR SET Ø
CURSOR 1
CURSOR Ø
SH4
DTR
TEST
HSHAKE
A3 74LS244
A41 74LS244
A34 74LS244
A29 74LS244
DØ D1 D2 D3 D4 D5 D6 D7 — SH1
LINE/PAGE ATTRIBUTES SH3
BIT 1 SH2
BIT Ø SH2
B600014-002
APPLICATION
NEXT ASSY USED ON
UNLESS OTHERWISE NOTED DIMENSIONS ARE IN
SCALE NONE
MATERIAL
FINISH
DWN H. Hur 1-22-82
TeleVideo, Inc.
PCB SCHEMATIC CONT BD 925 G/A
SIZE D SHT 5 OF 6
DRAWING NO 2015801
REV A3

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A3	SEE SHEET 1		

SH1 DIPSWITCH PORT #5
SH1 DIPSWITCH PORT #4
SH1 DIPSWITCH PORT #3
SH1 DIPSWITCH PORT #2
SH3 DIPSWITCH PORT #1

+5V — R3 4.7K — RP1 4.7K

S1
1 BD RT 3
2 BD RT 2
3 BD RT 1
4 BD RT Ø
5 WD LENGTH
6 STOP BITS
7
8
9
10

EDIT 920/925

S2
1 BD RT3
2 BD RT2
3 BD RT1
4 BD RTØ
5 PAR 2
6 PAR 1
7 PARØ
8 BOW / WOB
9 COMM MODE Ø
10 COMM MODE 1
11 50/60 HZ
12 CR/CR-LF

RP2 4.7K
RP4 4.7K +5V

S3
1 KEY CLICK
2 CHAR SET 1
3 CHAR SET Ø
4 CURSOR 1
5 CURSOR Ø
6 TIMEOUT BLANK ENABLE
7 LINE/PAGE ATTRIBUTES

RP3 4.7K

A3 74LS244 — A4-1 74LS244 — A34 74LS244 — A29 74LS244
GND

DØ D1 D2 D3 D4 D5 D6 D7 — SH1

LINE/PAGE ATTRIBUTES SH3
BIT 1 SH2
BIT Ø SH2

SH4 DTR, TEST, HSHAKE

86000/4-002

APPLICATION		UNLESS OTHERWISE NOTED	DWN H. Hur 1-22-82	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK	
		ANG ± 2 PLC ± 3 PLC ±	ENGR	TITLE PCB SCHEMATIC CONT BD 925 G/A
		SCALE NONE	APPD	
		MATERIAL —	FINISH —	SIZE D SHT 5 OF 6 DRAWING NO 2015801 REV A3

A3 2015801

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A3	SEE SHEET 1		

Y2 XTAL 13.608MHZ
C31 10 pf 50V
R27 330
R25 750
R26 1.8K
R28 470
74S04 A40
E13
E12
+5V
R11 1K
A25 74LS163
A36 74LS04
A40 74S04
A37 74LS08
SHIFT CLOCK — SH2,3
DC CARRY — SH 2,3
SET DISP RAM — SH 3
CHAR CLK — SH2,3
CHAR CLK — SH 1

SH1 SYS RESET
SH3 CONTROL LATCH #1
SH3 CONTROL LATCH #2
SH1 D0 D1 D2 D3 D4 D5 D6 D7
A27 74LS273
A26 74LS273
PAGE PRINT — SH4
BLINK CLOCK — SH3
CURSOR*BLOCK — SH3
SPARE
525/920 ATTS — SH3
BI-DIRECTIONAL — SH4
EXTENSION — SH4
CPU RESET — (NOT USED)
MONITOR MODE — SH2
DTR — SH4
BOW/WOB — SH3
DISPLY PAGE 2 — SH2

C33 1uf 16V
TIMEOUT BLANK
R2 51K
C18A 1uf 16V
R10 4.7K
R24 330
R22 330
Q2 2N4401
C30 10uf 16V
R23 330
A35 74LS00
A31 7406
A42 74LS32
A37 74LS08
P7-1
P7-2
P0-4
P1-4

SH4 NMI
SH3 ROW 10
P6-13 SPEAKER (FROM INTERNAL MODEM)
P0-1
P1-1
P0-2
P1-2
+12V
.01uf 16V
C19 330pf 100V

SH3 VIDEO
E3 E4
R6 750
R7 1K
R1 22
C18 4.7uf 16V
R8 10K
R9 33
CR1 IN914
Q1 2N4401
VIDEO SHIELD GND — P2-3
VIDEO — P2-4
R5 270
E1
E2
SH3 HALF INTENSITY
SH3 COMPOSITE VIDEO
R16 1K
COMP V+TTL VIDEO — P2-6

+12V — P6-1, P6-14
-12V — P6-5, P6-10
+5V — P6-6, P6-9, P6-7, P6-8

P3-12 RXD+ — P6-15 (SEE NOTE 5)
P3-24 RXD- — P6-0 (SEE NOTE 5)
P6-11 TXD+ — P3-25
P6-4 TXD- — P3-13
CURRENT LOOP COMM (OPTIONAL)

P9-1, P9-2, P3-1, P4-1 — CHASSIS GND
P3-7, P4-7 — LOGIC GND

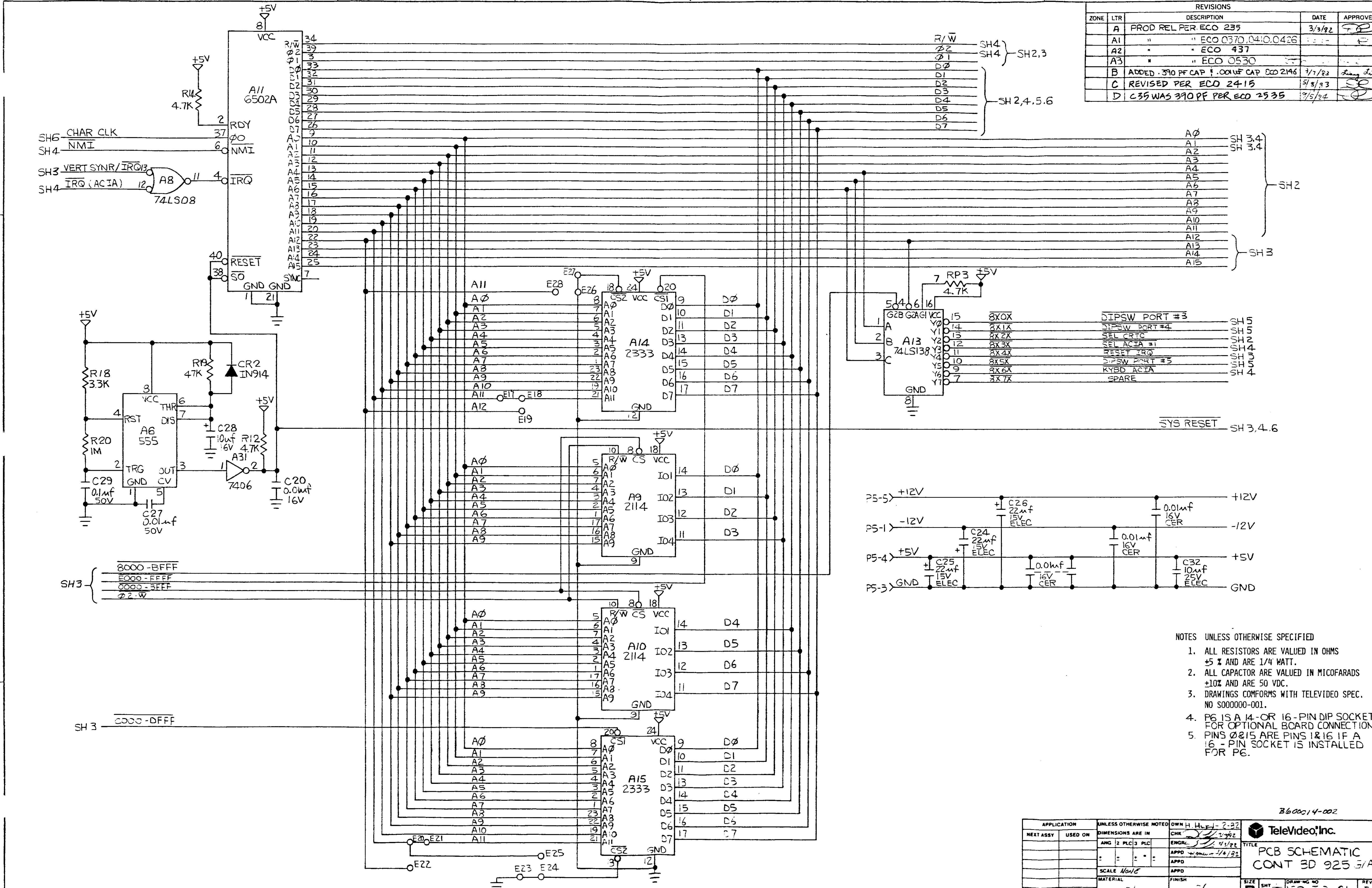
B600014-002

APPLICATION		UNLESS OTHERWISE NOTED	DWN H.Hwr 1-25-82	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK	
		ANG ± 2 PLC ± 3 PLC ±	ENGR	TITLE PCB SCHEMATIC CONT BD 925 G/A
		SCALE NONE	APPD	
		MATERIAL	APPD	
			APPD	
			FINISH	SIZE D SHT 1 OF 2 DRAWING NO 2015801 REV A3

A3 2015801

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	PROD REL PER ECO 235	3/3/82	
	A1	" " ECO 0370,0410,0426		
	A2	" " ECO 437		
	A3	" " ECO 0530		
	B	ADDED .390 PF CAP & .001uF CAP ECO 2146	7/7/83	Liang Lin
	C	REVISED PER ECO 2415	5/3/83	
	D	C35 WAS 390 PF PER ECO 2535	9/5/84	



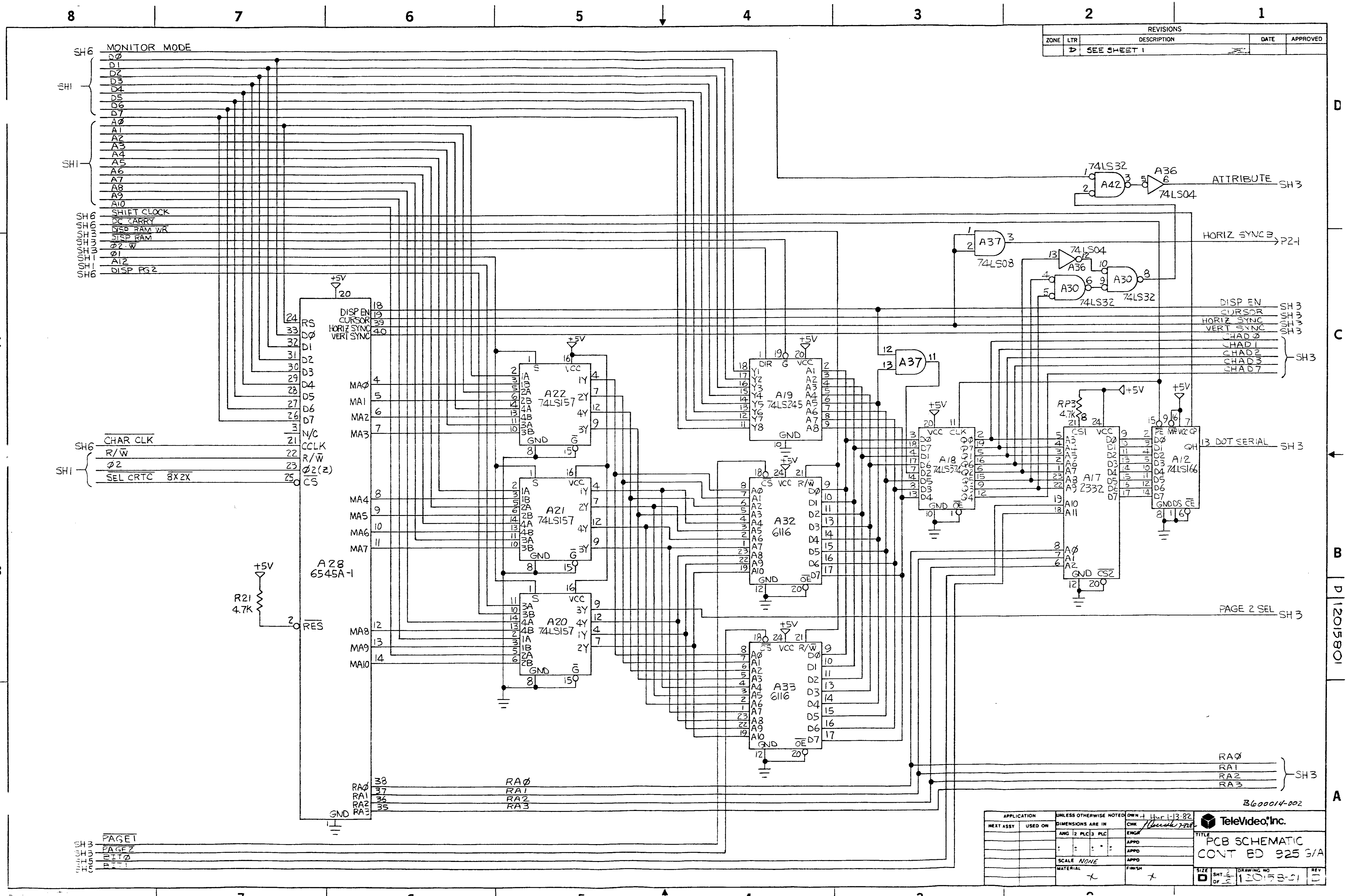
NOTES UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE VALUED IN OHMS ±5 % AND ARE 1/4 WATT.
2. ALL CAPACITOR ARE VALUED IN MICOFARADS ±10% AND ARE 50 VDC.
3. DRAWINGS CONFORMS WITH TELEVIDEO SPEC. NO S000000-001.
4. P6 IS A 14-OR 16-PIN DIP SOCKET FOR OPTIONAL BOARD CONNECTION.
5. PINS Ø&15 ARE PINS 1&16 IF A 16-PIN SOCKET IS INSTALLED FOR P6.

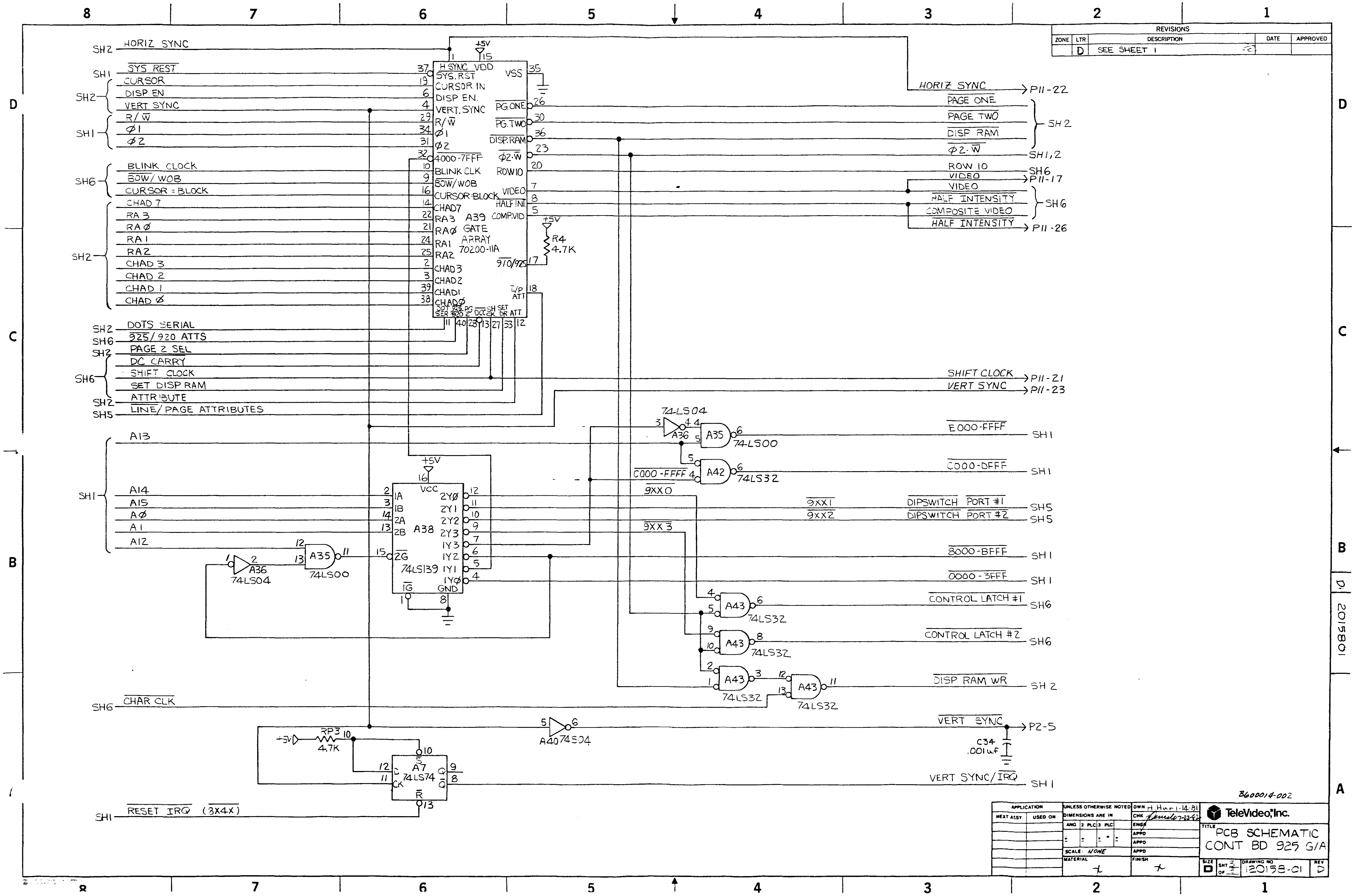
B600014-002

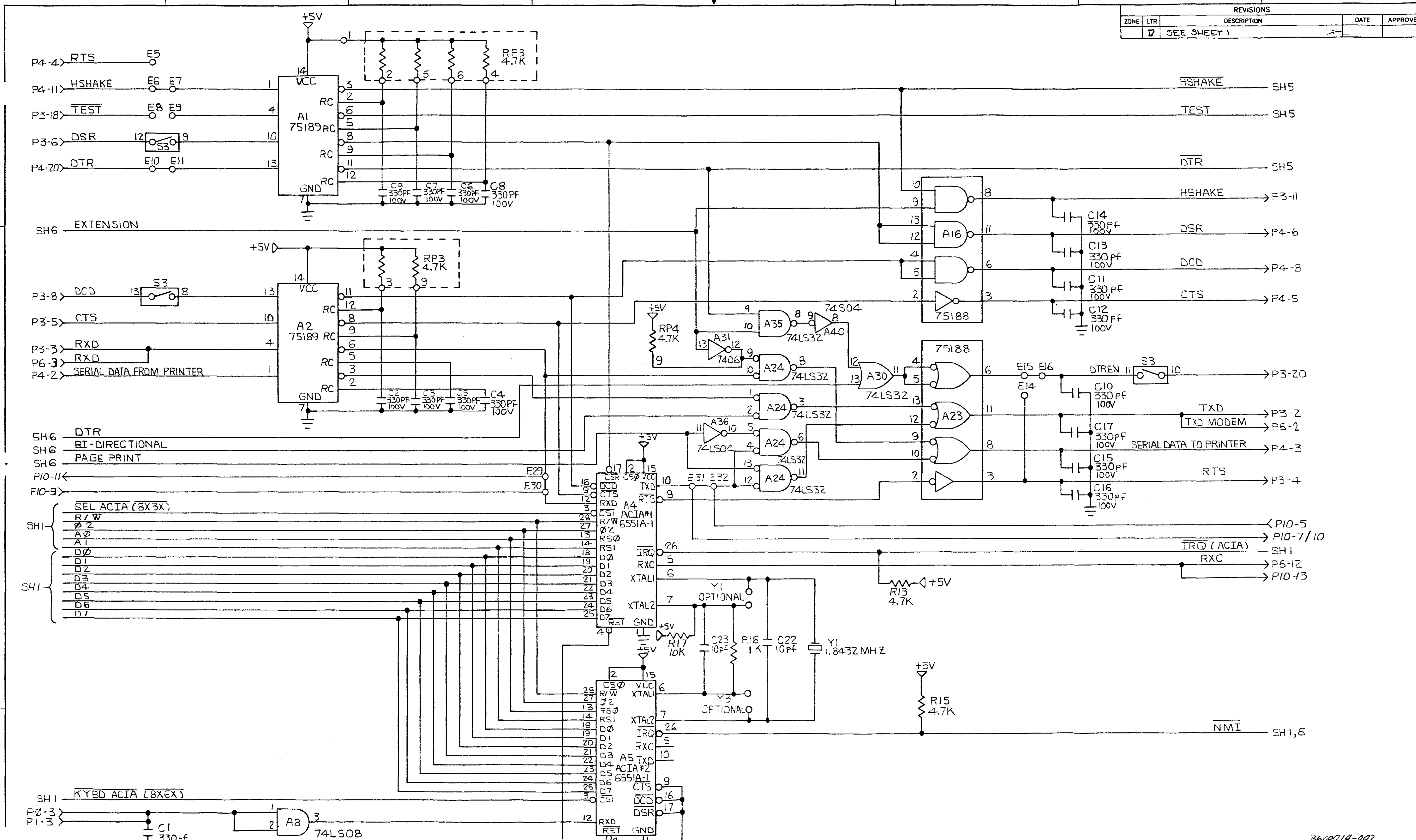
APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN H. Hurd 2-82	TeleVideo, Inc.
NEXT ASSY	USED ON	ANG / 2 PLC / 3 PLC	CHK 3/4/82	TITLE PCB SCHEMATIC CONT BD 925 G/A
		SCALE NONE	ENGR 3/3/82	
		MATERIAL	APPD 3/4/82	
			FINISH	SIZE D · SHT OF · DRAWING NO · REV

D 201980 I



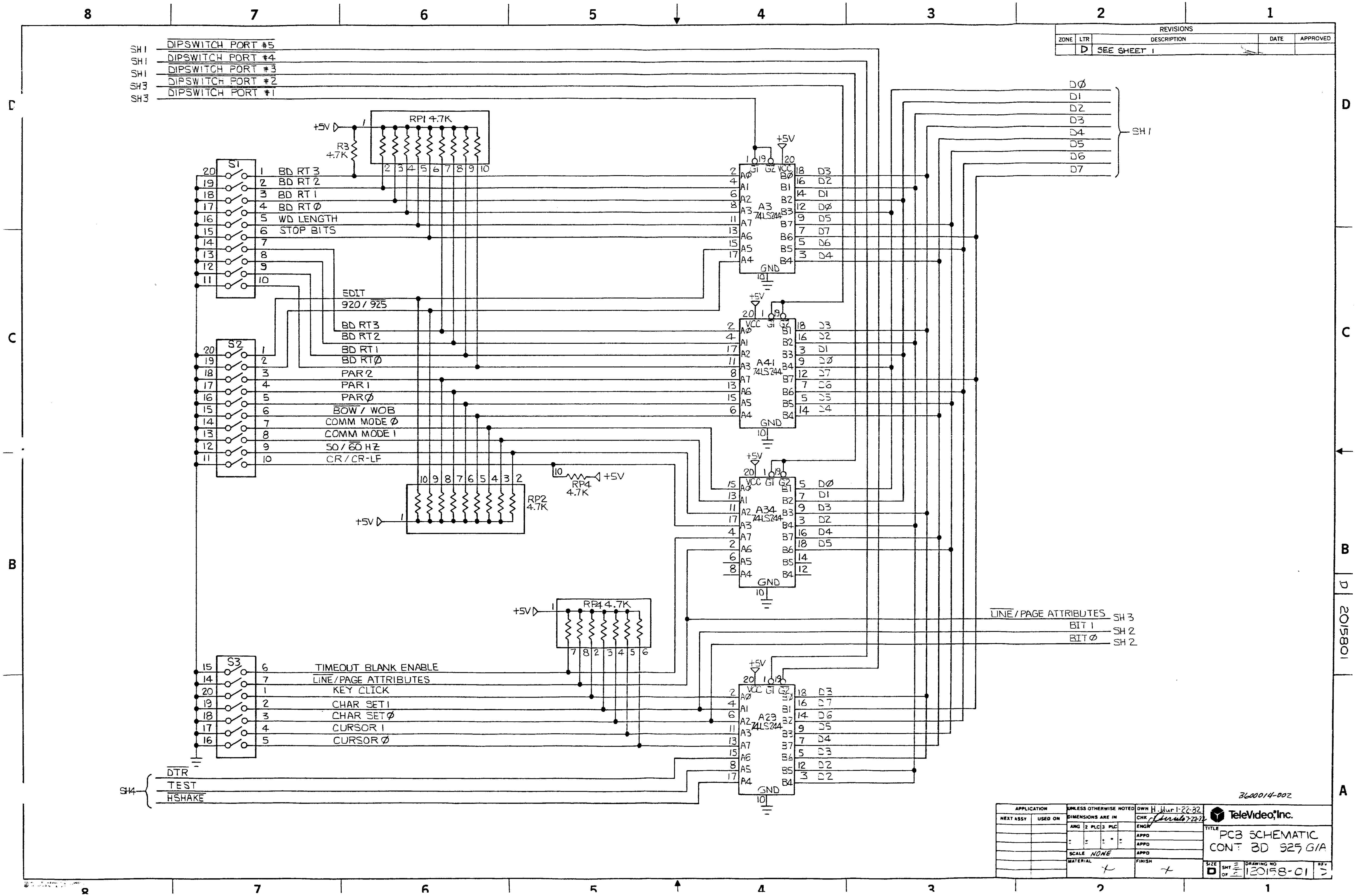
REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
D | SEE SHEET 1
MONITOR MODE
D0 D1 D2 D3 D4 D5 D6 D7
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10
SHIFT CLOCK
DC CARRY
DISP RAM WR
DISP RAM
Ø2 · W
Ø1
A12
DISP PG2
CHAR CLK
R/W
Ø2
SEL CRTC 8X2X
A28 6545A-1
R21 4.7K
+5V
A22 74LS157
A21 74LS157
A20 74LS157
A19 74LS245
A32 6116
A33 6116
A18 74LS374
A17 2332
A12 74LS166
RP3 4.7K
A42 74LS32
A36 74LS04
A37 74LS08
A30 74LS32
ATTRIBUTE SH3
HORIZ SYNC B P2-1
DISP EN SH3
CURSOR SH3
HORIZ SYNC SH3
VERT SYNC SH3
CHAD Ø
CHAD 1
CHAD 2
CHAD 3
CHAD 7
SH3
DOT SERIAL SH3
PAGE 2 SEL SH3
RAØ RA1 RA2 RA3 SH3
PAGE1
PAGE2
BIT0
BIT1
B600014-002
APPLICATION
NEXT ASSY | USED ON
UNLESS OTHERWISE NOTED DIMENSIONS ARE IN
SCALE NONE
MATERIAL
FINISH
TeleVideo, Inc.
TITLE PCB SCHEMATIC CONT BD 925 G/A
SIZE D
SHT 2 OF 2
DRAWING NO 120158-01
D 120158-01


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
D SEE SHEET 1
SH2 HORIZ SYNC
SH1 SYS REST
SH2 CURSOR
DISP EN
VERT SYNC
SH1 R/W
Ø1
Ø2
SH6 BLINK CLOCK
80W/WOB
CURSOR=BLOCK
SH2 CHAD 7
RA 3
RA Ø
RA 1
RA 2
CHAD 3
CHAD 2
CHAD 1
CHAD Ø
SH2 DOTS SERIAL
SH6 925/920 ATTS
SH2 PAGE 2 SEL
SH6 DC CARRY
SHIFT CLOCK
SET DISP RAM
SH2 ATTRIBUTE
SH5 LINE/PAGE ATTRIBUTES
H SYNC VDD
SYS.RST
CURSOR IN
DISP EN.
VERT. SYNC
R/W
Ø1
Ø2
4000-7FFF
BLINK CLK
80W/WOB
CURSOR:BLOCK
CHAD7
RA3
RAØ
RA1
RA2
CHAD3
CHAD2
CHAD1
CHADØ
VSS
PG.ONE
PG.TWO
DISP.RAM
Ø2·W
ROW10
VIDEO
HALF INT.
COMP.VID
970/925
C/P ATT
A39 GATE ARRAY 70200-11A
+5V
R4 4.7K
HORIZ SYNC → P11-22
PAGE ONE
PAGE TWO
DISP RAM
Ø2·W
SH 2
SH1,2
ROW 10 SH6
VIDEO → P11-17
VIDEO
HALF INTENSITY
COMPOSITE VIDEO
SH6
HALF INTENSITY → P11-26
SHIFT CLOCK → P11-21
VERT SYNC → P11-23
74LS04
A36
A35 74LS00
A42 74LS32
C000-FFFF
E000-FFFF SH1
C000-DFFF SH1
9XX0
9XX1
9XX2
9XX3
DIPSWITCH PORT #1 SH5
DIPSWITCH PORT #2 SH5
SH1 A13
A14
A15
AØ
A1
A12
VCC
1A
1B
2A
2B
2G
1G
GND
2YØ
2Y1
2Y2
2Y3
1Y3
1Y2
1Y1
1YØ
A38
74LS139
A36 74LS04
A35 74LS00
8000-BFFF SH1
0000-3FFF SH1
CONTROL LATCH #1 SH6
CONTROL LATCH #2 SH6
A43 74LS32
DISP RAM WR SH 2
SH6 CHAR CLK
+5V RP3 4.7K
A7 74LS74
A40 74S04
VERT SYNC → P2-5
C34 .001uf
VERT SYNC/IRQ SH1
SH1 RESET IRQ (8X4X)
B600014-002
APPLICATION
NEXT ASSY USED ON
UNLESS OTHERWISE NOTED DIMENSIONS ARE IN
SCALE: NONE
MATERIAL
FINISH
DWN H. Hur 1-14-81
CHK
TeleVideo, Inc.
TITLE PCB SCHEMATIC CONT BD 925 G/A
SIZE D
SHT 2 OF 2
DRAWING NO 120158-01
REV D
D 2015801


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
D SEE SHEET 1
P4-4 RTS E5
P4-11 HSHAKE E6 E7
P3-18 TEST E8 E9
P3-6 DSR S3
P4-20 DTR E10 E11
A1 75189
RP3 4.7K
C9 C7 C6 C8 330PF 100V
SH6 EXTENSION
P3-8 DCD S3
P3-5 CTS
P3-3 RXD
P6-3 RXD
P4-2 SERIAL DATA FROM PRINTER
A2 75189
C2 C3 C5 C4 330PF 100V
SH6 DTR
SH6 BI-DIRECTIONAL
SH6 PAGE PRINT
P10-11 E29
P10-9 E30
SH1 SEL ACIA (8X3X)
R/W
Ø2
AØ
A1
DØ D1 D2 D3 D4 D5 D6 D7
A4 ACIA#1 6551A-1
A5 ACIA#2 6551A-1
R17 10K
C23 10pF
R16 1K
C22 10pF
Y1 1.8432 MHZ
Y1 OPTIONAL
Y2 OPTIONAL
SH1 KYBD ACIA (8X6X)
PØ-3
P1-3
C1 330pf 100V
A8 74LS08
SH1 SYS RESET
RP4 4.7K
A31 7406
A35 74LS32
A40 74S04
A30 74LS32
A24 74LS32
A36 74LS04
E31 E32
A16 75188
75188
A23
E15 E16 E14
DTREN S3
C14 C13 C11 C12 330pF 100V
C10 C17 C15 C16 330pF 100V
HSHAKE SH5
TEST SH5
DTR SH5
HSHAKE P3-11
DSR P4-6
DCD P4-3
CTS P4-5
P3-20
TXD P3-2
TXD MODEM P6-2
SERIAL DATA TO PRINTER P4-3
RTS P3-4
P10-5
P10-7/10
IRQ (ACIA) SH1
RXC P6-12
P10-13
R13 4.7K +5V
R15 4.7K
NMI SH1,6
D 2015801

B600014-002

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN H. H. 1-21-82	TeleVideo, Inc.
NEXT ASSY	USED ON	SCALE NONE	CHK	TITLE PCB SCHEMATIC CONT BD 925 G/A
		MATERIAL	FINISH	SIZE D SHT 4 OF 6 DRAWING NO 120158-01 REV D



REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
D SEE SHEET 1
SH1 DIPSWITCH PORT #5
SH1 DIPSWITCH PORT #4
SH1 DIPSWITCH PORT #3
SH3 DIPSWITCH PORT #2
SH3 DIPSWITCH PORT #1
RP1 4.7K
+5V
R3 4.7K
S1
BD RT 3
BD RT 2
BD RT 1
BD RT Ø
WD LENGTH
STOP BITS
EDIT
920/925
BD RT3
BD RT2
BD RT1
BD RTØ
S2
PAR 2
PAR 1
PARØ
BOW/WOB
COMM MODE Ø
COMM MODE 1
50/60 HZ
CR/CR-LF
RP2 4.7K
RP4 4.7K
A3 74LS244
A41 74LS244
A34 74LS244
A23 74LS244
GND
VCC
DØ D1 D2 D3 D4 D5 D6 D7
SH1
LINE/PAGE ATTRIBUTES SH3
BIT 1 SH2
BIT Ø SH2
S3
TIMEOUT BLANK ENABLE
LINE/PAGE ATTRIBUTES
KEY CLICK
CHAR SET1
CHAR SETØ
CURSOR 1
CURSOR Ø
SH4
DTR
TEST
HSHAKE
D 2015801
3600014-002
TeleVideo, Inc.
PCB SCHEMATIC CONT BD 925 G/A
SCALE NONE
D 120158-01

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	D	SEE SHEET 1		

Y2 XTAL 13.608 MHZ
C31 10 pf 50V
R27 330
R25 750
R26 1.8K
R28 470
E13
E12
A40 74S04
74S04 A40
C35 150 PF
+5V
R11 1K
A25 74LS163
SHIFT CLOCK SH2,3
A36 74LS04
A40 74S04
A37 74LS08
DC CARRY SH 2,3
SET DISP RAM SH 3
CHAR CLK SH2,3
A40 74S04
CHAR CLK SH 1

SH1 SYS RESET
SH3 CONTROL LATCH #1
SH3 CONTROL LATCH #2
SH1 D0 D1 D2 D3 D4 D5 D6 D7
A27 74LS273
PAGE PRINT SH4
BLINK CLOCK SH 3
CURSOR=BLOCK SH 3
SPARE
525/920 ATTS SH 3
BI-DIRECTIONAL SH4
EXTENSION SH4
CPU RESET (NOT USED)

A26 74LS273
MONITOR MODE SH 2
DTR SH4
BOW/WOB SH 3
DISPLY PAGE 2 SH 2

C33 1uf 16V
TIMEOUT BLANK
R2 51K
C18A 1uf 16V
R10 4.7K
R24 330
R22 330
Q2 2N4401
C30 10uf 16V
A42 74LS32
A35 74LS00
A31 7406
A37 74LS08
A42 74LS32
R23 330
P7-1
P7-2
P0-4
P1-4

SH4 NMI
SH3 ROW 10
P6-13 SPEAKER (FROM INTERNAL MODEM)
P0-1
P1-1
P0-2
P1-2
+12V
.01uf 16V
.01uf 16V
C19 330pf 100V

SH3 VIDEO
E3 E4
R6 750
R7 1K
CR1 IN914
R5 270
E1
R1 22
C18 4.7uf 16V
R8 10K
R9 33
Q1 2N4401
VIDEO SHIELD GND P2-3
VIDEO P2-4

SH3 HALF INTENSITY
SH3 COMPOSITE VIDEO
A31 7406
R16 1K
E2
COMP V+TTL VIDEO P2-6

+12V P6-1 P6-14
-12V P6-5 P6-10
+5V P6-6 P6-9 P6-7 P6-8

P3-12 RXD+ P6-15 (SEE NOTE 5)
P3-24 RXD- P6-0 (SEE NOTE 5)
P6-11 TXD+ P3-25
P6-4 TXD- P3-13
CURRENT LOOP COMM (OPTIONAL)

P9-1 P9-2 P3-1 P4-1
CHASSIS GND

P3-7 P4-7
LOGIC GND

B600014-002

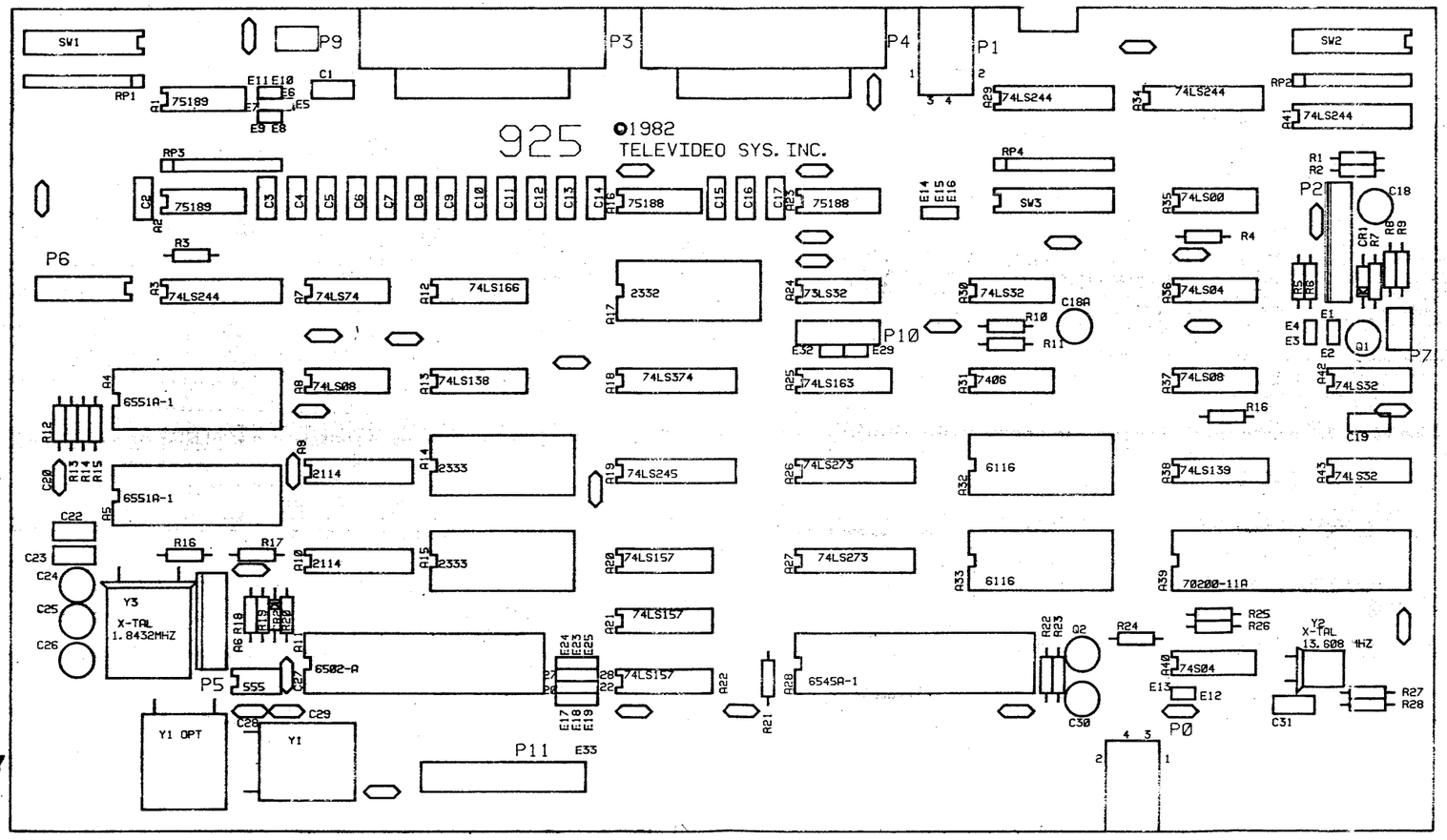
APPLICATION		UNLESS OTHERWISE NOTED	DWN	CHK	ENGR	APPD	APPD	APPD
NEXT ASSY	USED ON	DIMENSIONS ARE IN						
		ANG ± PLC ± PLC						
		SCALE NONE						
		MATERIAL			FINISH			

TeleVideo, Inc.

TITLE PCB SCHEMATIC CONT 3D 925 SYA

SIZE D | SHT 5 OF 5 | DRAWING NO 20 538-01 | REV D

D 20538-01



925 GATE ARRAY
CONTROL BOARD
REV A

VIDEO MONITOR

The video monitor contains two sections: the vertical amplifier and the horizontal amplifier. These amplifiers provide the voltages necessary to drive the CRT yoke, which deflects the electron beam across the CRT.

The electron beam, which is generated by the CRT electron gun, sweeps across and down the screen to create scan lines (see section on character generation). The beam's movement is driven by vertical and horizontal sweep rates, which are determined by the display circuitry on the logic board. The horizontal sweep is approximately 16 KHz, the vertical sweep 60 Hz for domestic and 50 Hz for European applications.

The horizontal synch pulses coming into the video monitor are inverted and amplified by transistor Q301. This signal is then coupled across the drive transformer T301 and applied to the base of the ouptut transistor Q302. Q302's output drives both horizontal yoke windings, as well as the step-up transformer that produces the anode voltage and the grid voltage for the CRT grid in the neck of the CRT. Since high-frequency magnetic fields are produced and then broken, the flyback transformer is necessary to provide high voltages for the horizontal scans.

These horizontal scans start in the upper left corner and scan across to the upper right corner. Once the scan reaches the end of the line, a blank appears where the video beam is turned off and retraced to the beginning of the next scan line.

The vertical synch pulses coming into the video monitor are converted to a sawtooth waveform. Initially, this pulse goes from a negative leading edge to a positive falling edge and passes through transistor Q202, which inverts it to its usable form.

At that point, the pulse goes from a +2-volt leading edge to a -2.5-volt falling edge. Timing is critical since 250 horizontal scan lines (which comprise the total number of horizontal scan lines on the CRT) occur within one sawtooth pulse. Therefore, the sawtooth pulse has to be proportional to all previous pulses or the timing will be off for the vertical as well as the horizontal sweep.

When the vertical sweep is negative, Q201 conducts and C202 discharges. During the positive portion, Q201 cuts off and allows C202 to charge. While C202 is charging, the electron beam scans.

The vertical sweep scans from top to bottom. Once it reaches the bottom of the page, a blank occurs when the video beam is turned off and is retraced to the top of the screen. At that point, C202 discharges. After the retrace, the beam turns off again and begins its scan routine.

Adjusting SFR1 (vertical height) and SFR2 (vertical linearity) changes the rate of C202's charge, and therefore the slope of the sawtooth pulse.

TUBE SPECIFICATION

12 INCH 90 DEGREE, HIGH RESOLUTION

DISPLAY TUBE

310KGB 31

The 310KGB31 is a 12 inch 90 degree high resolution, rectangular display tube primarily intended for use as a alpha-numerical and graphic display tube for computer peripheral devices. The tube is provided with banded type integral implosion protection (with mounting lugs). The tube features a low reflectance high contrast screen.

ELECTRICAL DATA

Heating
Indirect by AC or DC:
Heater voltage. . . . . .12.0 volts
Heater current. . . . . 75 nA

Focusing Method. . . . . Electrostatic

Deflection Method. . . . . Magnetic

Deflection Angles (Approx.)
Diagonal. . . . . 90 degrees
Horizontal. . . . . 78 degrees
Vertical. . . . . 61 degrees

Anode voltage . . . . . 15,000 max. volts
8,000 min. volts

Using high voltage with this tube internal flash-overs may occur, which may cause damage to the cathode of the tube and to various circuit components on the video monitor board. Therefore it is necessary to provide protective circuits using spark-gaps etc. These should be connected as illustrated in figure #1 below.

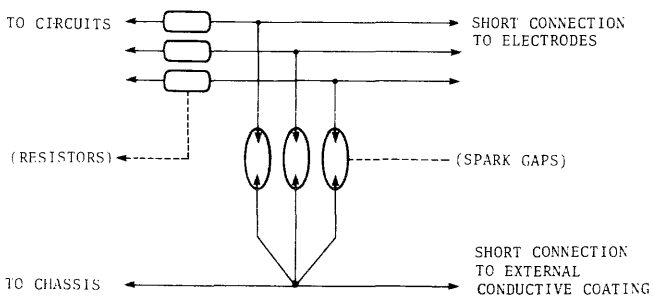


Figure 1.

No other connections between external conductive coating and chassis are permissible.

OPTICAL DATA

Faceplate	Filterglass
Anti-reflection treatment	No
Screen	Aluminized
Appearance	Low Reflective

A:
The dark-colored screen, in combination with the filterglass, produces the low reflectivity (equivalent to a 20% light transmission filterglass) for easy-to-see display.

MECHANICAL DATA

Tube Dimensions:

Overall length	278.8 max. mm
Greatest dimensions of tube (excluding lugs)	
Diagonal	318.5 +/- 2.7 mm
Width	279.6 +/- 2.7 mm
Heigth	218.7 +/- 2.7 mm
Useful screen dimensions (projected)	
Diagonal	295.0 min. mm
Width	257.0 min. mm
Heigth	195.0 min. mm

Pin Position Alignment	Pin No 5 aligns approx. with anode contact.
Operating Position	Any
Weight (approx.)	3.2 kg
Implosion Protection	Tension band (with mounting lugs)

GENERAL CONSIDERATIONS:

1. Tube handling. Care should be taken not to scratch the tube.

2. Impact. The tubes should never be exposed to impacts of more than 30G during handling or transportation.

3. Grounding. The external conductive coating of the tube should be grounded with multiple contacts (e.g. a contact plate having many fingers.) Poor contact might cause local heating resulting in tube leakage.

WARNING

SHOCK HAZARD:

The high voltage at which the tube is operated may be very dangerous. Design of the equipment should include safeguards to prevent the user from coming in contact with the high voltage. Extreme care should be taken in the servicing or adjustment of any high voltage circuit.

Caution must be exercised during the replacement or servicing of the tube since a residual electrical charge is stored within the tube. Before handling the tube remove any undersible residual high voltage charge from the tube, by shorting the anode contact button to the frame of the terminal as illustrated in figure #2. Discharging the high voltage to isolated metal parts sucha as cabinets and control brackets may produce a shock hazard.

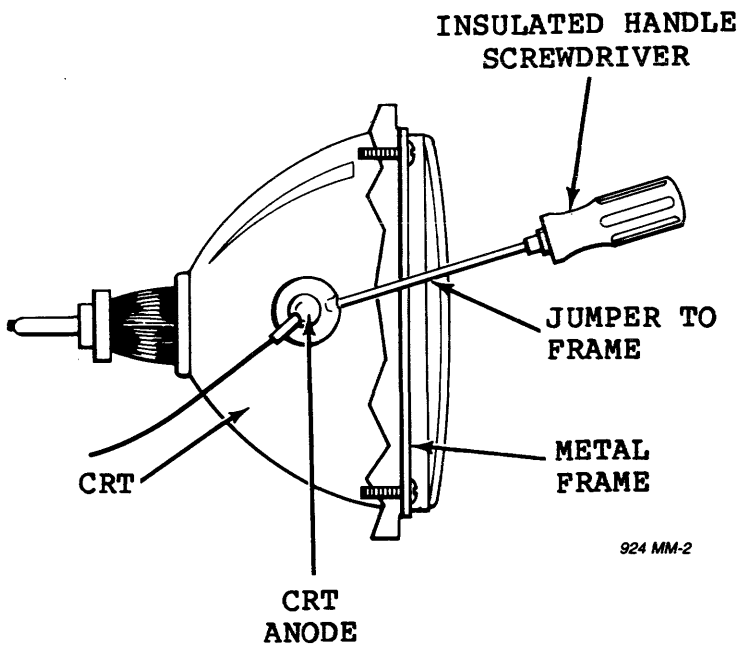


Figure 2

POWER SUPPLY

Voltages are created and regulated as follows: A 9.8 AC voltage is rectified by diodes D105 and D108, resulting in a 9-volt output. These 9 volts are then filtered through C117 and applied at the 5-volt regulator IC2.

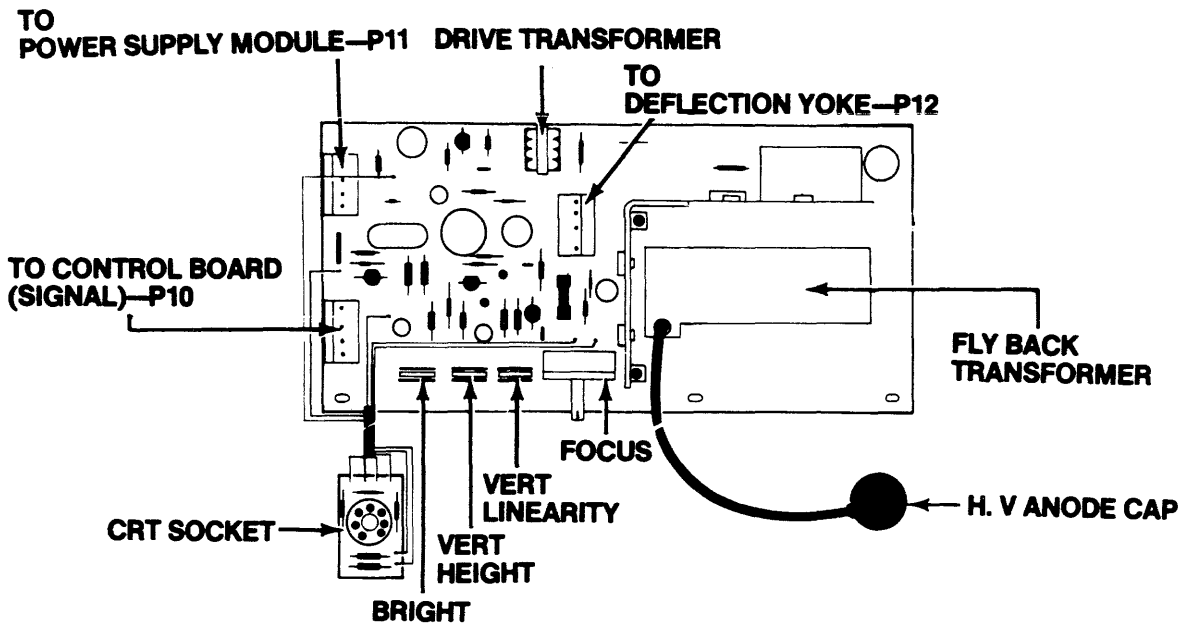
The raw AC voltages for the positive and negative 12 DC voltage are derived from the center top of the secondary winding of D101. The diodes D101 and D102 form a full-wave rectifier that converts the 37-volt AC waveform to a 20-volt DC level. This DC voltage is then filtered by C116 and stabilized to -12 volts by a zener-regulated circuit that consists of a resistor (R102) and the zener diode (D112).

Diodes D103 and D104 also form a full-wave rectifier that converts the 37-volt AC waveform to a +20-volt DC level.

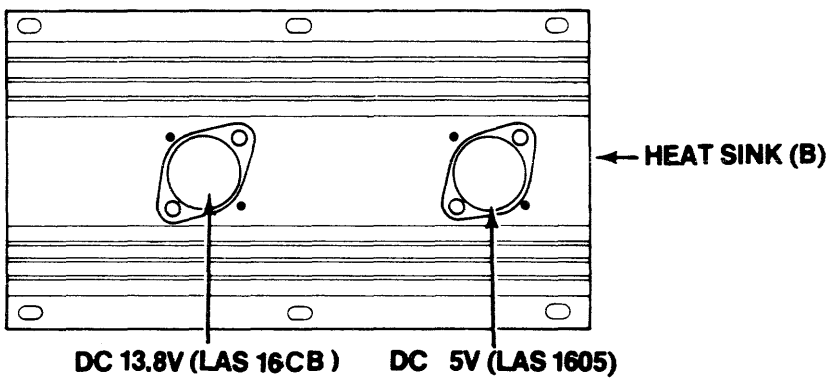
This DC voltage is filtered by C113 and applied to the 13.8-volt regulator IC1. The 13.8 output, in turn, is dropped 1.6 volts across diodes D113 and D114 to achieve the desired +12 volts DC.

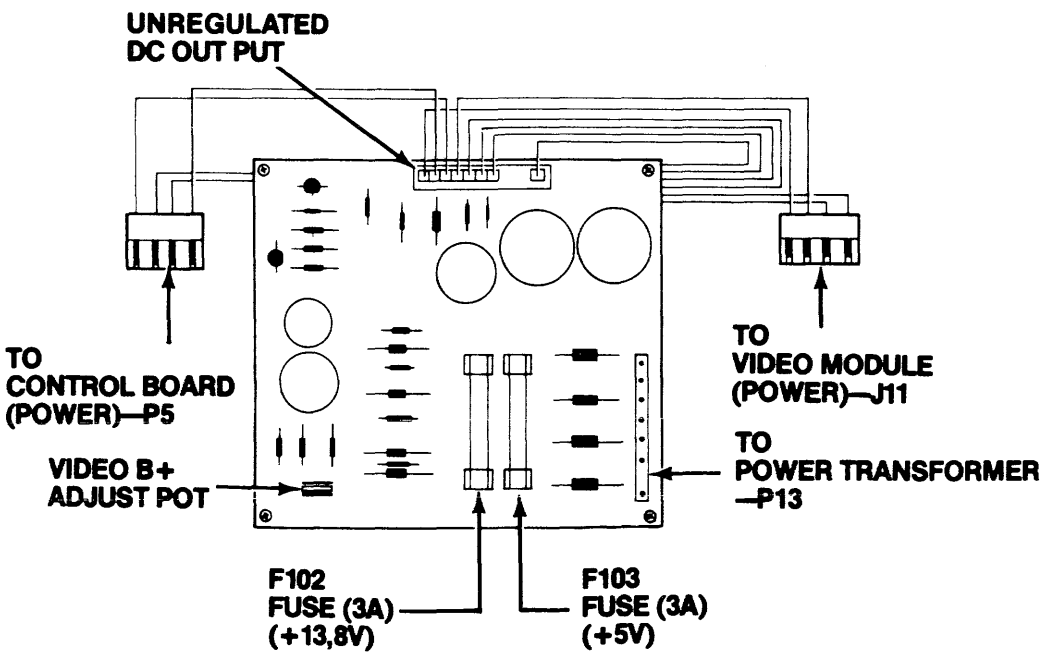
A 79-volt AC waveform is applied to the half-wave rectifier D109, which is filtered by C119. The resulting 95-volt DC level is then regulated by a series voltage regulator. The reference element is the positive 12-volt zener diode D111. The sensing and control elements are transistors Q103 and Q102.

The high voltages needed to drive the CRT tube V501 are derived from the flyback transformer T302 on the video module.



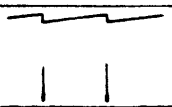
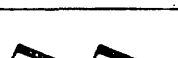
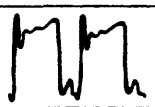
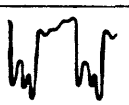
VIDEO MONITOR MODULE





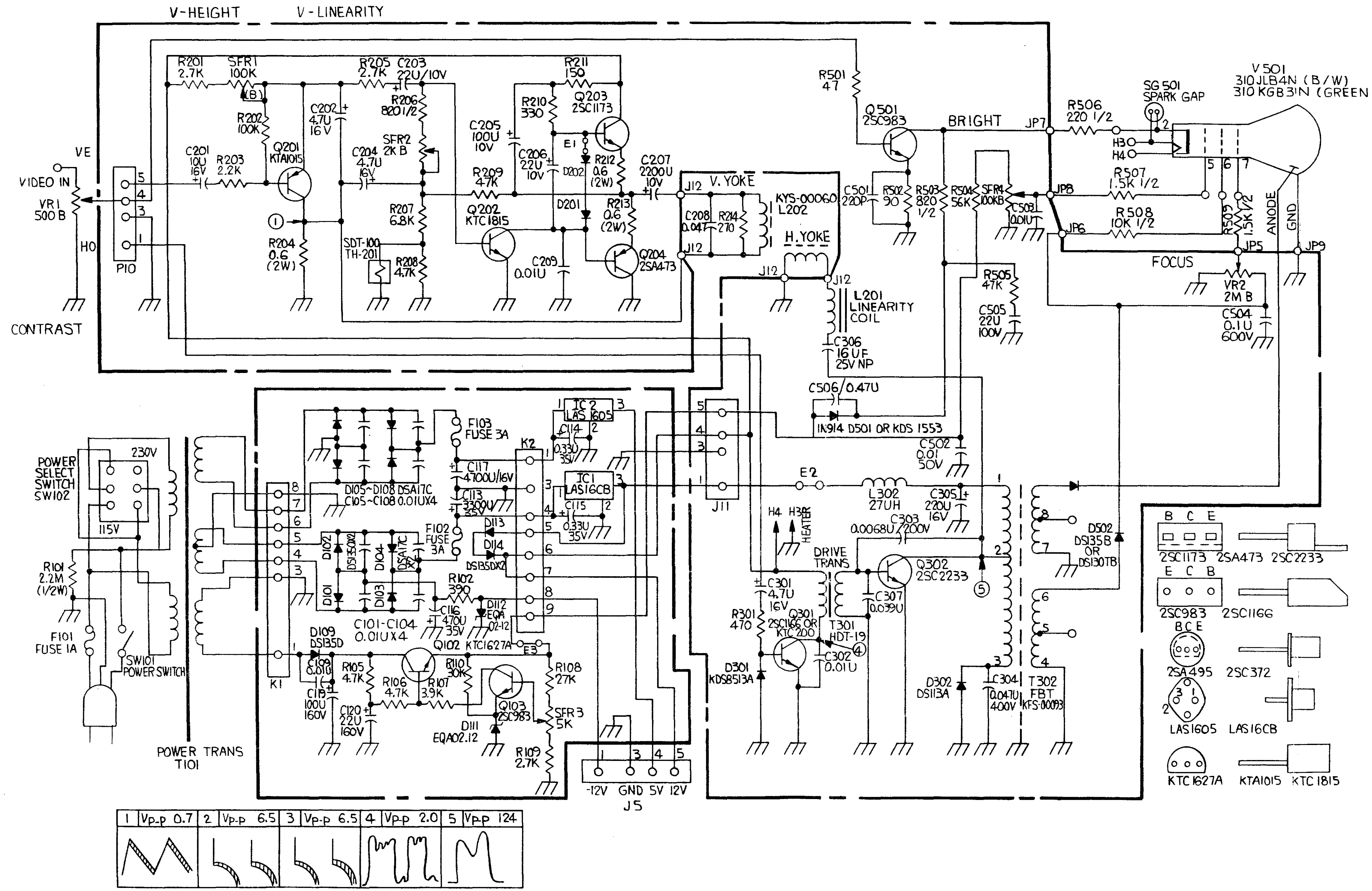
POWER SUPPLY MODULE

TR WAVEFORM and VOLTAGE

Transistor			Base(In)			Collector(Out)			Emitter(GND)		
Location	Parts	Function	Vtg DC V	Vtg AC Vp-p	Wave Form	Vtg DC V	Vtg AC Vp-p	Wave Form	Vtg DC V	Vtg AC Vp-p	Wave Form
IC	LAS1512	Regulation	12	2.5		12	0.0	—	0.0	0.0	—
IC	LAS1605	〃		1.6		5	0.0	—	0.0	0.0	—
IC	LAS1812	〃		0.1		-12	0.0	—	0.0	0.0	—
IC	LAS16CB	〃		1.4		13.8	0.0	—	0.0	0.0	—
Q102	2SC509	〃	78.7	0.0	—	86.4	1.5		98.0	0.0	—
Q103	2SC983	〃	12.0	0.0	—	75.7	0.0	—	11.9	0.0	—
Q201	2SA495	Vert Pree Drive	2.0	3.0		0.6	0.57		1.0	1.7	
Q202	2SC372	Vert Drive	0.68	0.5		8.0	6.5		0.0	0.0	—
Q203	2SC1173	Vert Out	9.36	6.5		12	0.0	—	8.76	6.5	
Q204	2SA473	Vert Out	8.0	6.5		0.0	0.0	—	8.6	6.5	
Q301	2SC735	Horiz Drive	-0.25	0.64		12	20		0.0	0.0	—
Q302	2SC2233	Horiz Out	-0.08	6		12.8	124		0.0	0.0	—
Q501	2SC983	Video Amp	0.4	3		76.8	25		-0.8	2.8	
D302	DS-113A	Damping	12.8	132							

DC Voltage reading taken with VTVM from point indicated to chassis ground.

AC Voltage reading taken with Oscilloscope from point indicated to chassis ground



V-HEIGHT
V-LINEARITY
VIDEO IN
VE
VR1
500 B
HO
CONTRAST
P10
R201
2.7K
SFR1
100K
R202
100K
C201
10U
16V
R203
2.2K
Q201
KTA1015
R204
0.6
(2W)
C202
4.7U
16V
R205
2.7K
C203
22U/10V
R206
820 1/2
SFR2
2K B
C204
4.7U
16V
R207
6.8K
SDT-100
TH-201
R208
4.7K
C205
100U
10V
R209
4.7K
Q202
KTC1815
R210
330
R211
150
Q203
2SC1173
C206
22U
10V
D202
D201
R212
0.6
(2W)
R213
0.6
(2W)
C209
0.01U
Q204
2SA473
C207
2200U
10V
V. YOKE
J12
C208
0.047
R214
270
KYS-00060
L202
H. YOKE
L201
LINEARITY
COIL
C306
16 UF
25V NP
R501
47
Q501
2SC983
BRIGHT
C501
220P
R502
90
R503
820
1/2
R504
56K
SFR4
100KB
C503
0.01U
R505
47K
C505
22U
100V
JP7
JP8
JP6
JP5
JP9
R506
220 1/2
SG501
SPARK GAP
V501
310JLB4N (B/W)
310KGB31N (GREEN)
H3
H4
R507
1.5K 1/2
R508
10K 1/2
R509
1.5K 1/2
ANODE
GND
FOCUS
VR2
2M B
C504
0.1U
600V
C506/0.47U
1N914 D501 OR KDS 1553
C502
0.01
50V
POWER SELECT SWITCH SW102
230V
115V
R101
2.2M
(1/2W)
F101
FUSE 1A
SW101
POWER SWITCH
POWER TRANS
T101
K1
D105~D108 DSA17C
C105~C108 0.01UX4
D101
D102
D103
D104
C101-C104
0.01UX4
F103
FUSE 3A
F102
FUSE
3A
C117
4700U/16V
C113
3300U
35V
IC2
LAS1605
C114
0.33U
35V
IC1
LAS16CB
C115
0.33U
35V
K2
D113
D114
DS135DX2
R102
390
C116
470U
35V
D112
EQA02-12
D109
DS135D
C109
0.01U
C118
100U
160V
R105
4.7K
C120
22U
160V
R106
4.7K
R107
3.9K
Q102
KTC1627A
R110
30K
Q103
2SC983
D111
EQA02.12
E3
R108
27K
SFR3
5K
R109
2.7K
J5
-12V
GND
5V
12V
J11
E2
L302
27UH
C305
220U
16V
C303
0.0068U/200V
H4
H3
HEATER
DRIVE
TRANS
C301
4.7U
16V
R301
470
Q301
2SC1166 OR
KTC200
T301
HDT-19
C302
0.01U
D301
KDS8513A
Q302
2SC2233
C307
0.039U
D302
DS113A
C304
0.047U
400V
T302
FBT
KFS-00093
D502
DS135B
OR
DS130TB
1 Vp-p 0.7
2 Vp-p 6.5
3 Vp-p 6.5
4 Vp-p 2.0
5 Vp-p 124
B C E
2SC1173
2SA473
2SC2233
E C B
2SC983
2SC1166
B C E
2SA495
2SC372
LAS1605
LAS16CB
KTC1627A
KTA1015
KTC1815

1. ALL RESISTANCE VALUES IN OHM K=1,000 M=1,000,000.
2. ALL CAPACITOR VALUES IN FARAD $U=10^{-6}$ $P=10^{-12}$
3. UNLESS OTHERWISE STATED, WORKING VOLTAGES OF CAPACITORS ARE 50 VOLTS.
4. THIS SCHEMATIC DIAGRAM COVERS BASIC OR REPRESENTATIVE CHASSIS ONLY. THERE MAY BE SOME COMPONENT OR PARTIAL SCHEMATIC DIFFERENCE BETWEEN ACTUAL CHASSIS AND THE SCHEMATIC DIAGRAM.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

QTY REQD	FSCM NO.	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN H.Hur 2/8/83
NEXT ASSY	USED ON	ANG / 2 PLC / 3 PLC	CHK
		±	ENGR S.M.Kim 2/8/83
		SCALE: —	APPD
		MATERIAL —	FINISH —

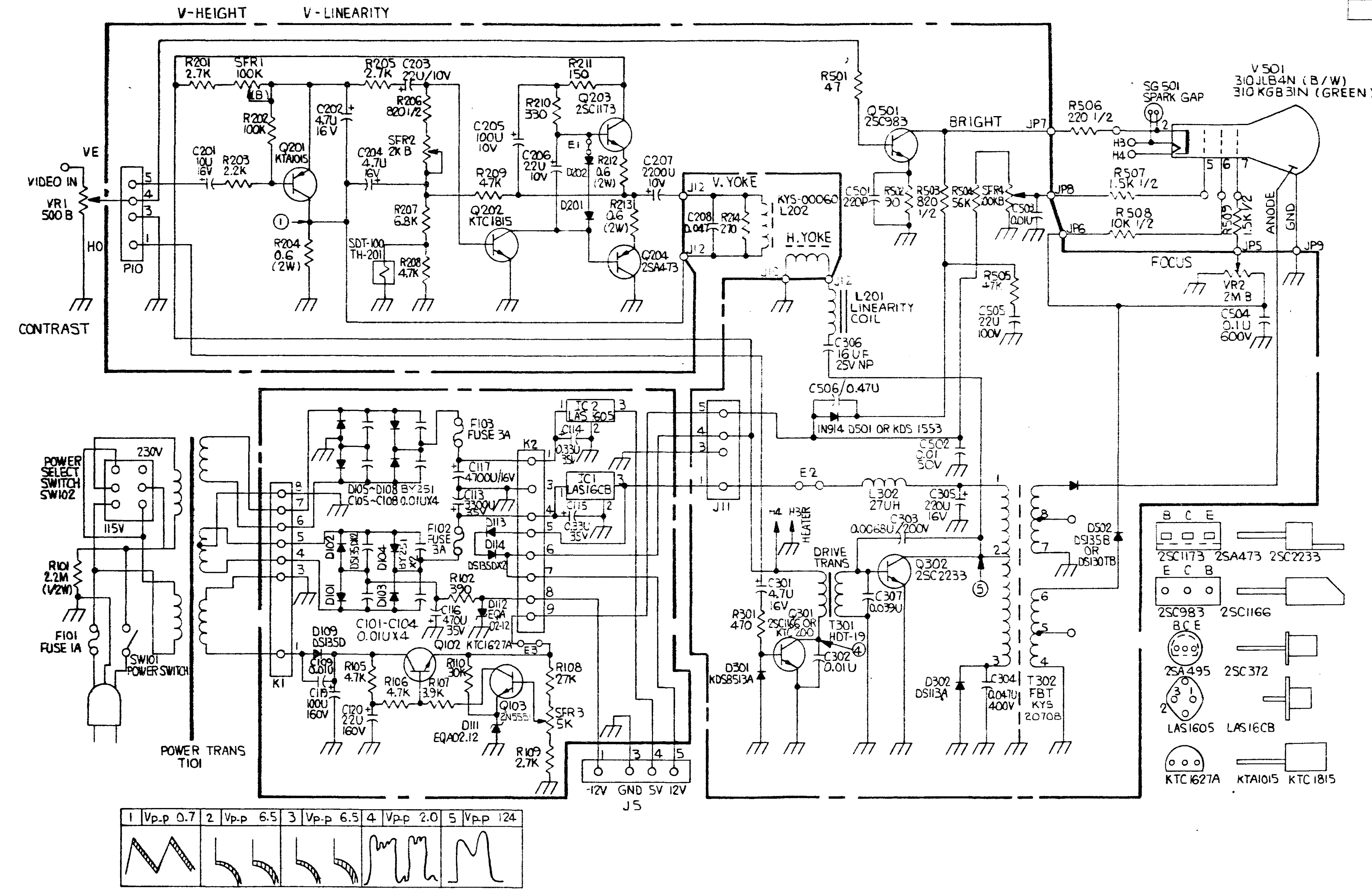
TeleVideo, Inc.

TITLE PCB SCHEMATIC DIARAM POWER SUPPLY VIDEO MONITOR

SIZE D | SHT 1 OF 1 | DRAWING NO. 2281900 | REV

DWG NO 2281900 SH 1 REV

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	REMOVED C209 PER ECC 2243		
	A1	T302 WAS KSF00093 ECO 2557		
	B	CHG D103-D108 FROM DSA17C TO BY251 ECO # 23097		



V-HEIGHT
V-LINEARITY
VIDEO IN
VR1 500 B
CONTRAST
P10
R201 2.7K
SFR1 100K
R202 100K
C201 10U 16V
R203 2.2K
Q201 KTA1015
R204 0.6 (2W)
C202 4.7U 16V
R205 2.7K
C203 22U/10V
R206 820 1/2
SFR2 2K B
C204 4.7U 16V
R207 6.8K
SDT-100 TH-201
R208 4.7K
R209 4.7K
Q202 KTC1815
C205 100U 10V
R210 330
C206 22U 10V
R211 150
Q203 2SC1173
R212 0.6 (2W)
R213 0.6 (2W)
Q204 2SA473
C207 2200U 10V
V. YOKE
KYS-00060 L202
H. YOKE
L201 LINEARITY COIL
C306 16UF 25V NP
R501 47
Q501 2SC983
BRIGHT
R506 220 1/2
SG501 SPARK GAP
V501 310JLB4N (B/W) 310KGB31N (GREEN)
R507 1.5K 1/2
R508 10K 1/2
FOCUS
VR2 2M B
C504 0.1U 600V
ANODE
GND
R505 47K
C505 22U 100V
C506/0.47U
1N914 D501 OR KDS 1553
C502 0.01 50V
POWER SELECT SWITCH SW102
230V
115V
R101 2.2M (1/2W)
F101 FUSE 1A
SW101 POWER SWITCH
POWER TRANS T101
F103 FUSE 3A
F102 FUSE 3A
IC2 LAS 605
IC1 LAS16CB
C117 4700U/16V
C113 3300U 35V
D105~D108 BY251
C105~C108 0.01UX4
C101-C104 0.01UX4
Q102 KTC1627A
Q103 2N5551
R108 27K
SFR3 5K
R109 2.7K
-12V GND 5V 12V
J5
J11
L302 27UH
C305 220U 16V
DRIVE TRANS
Q302 2SC2233
C301 4.7U 16V
R301 470
D301 KDS8513A
T301 HDT-19
T302 FBT KYS 20708
D502 DS135B OR DS130TB
D302 DS113A
C304 0.047U 400V
2SC1173 2SA473 2SC2233
2SC983 2SC1166
2SA495 2SC372
LAS1605 LAS16CB
KTC1627A KTA1015 KTC1815
1 Vp-p 0.7
2 Vp-p 6.5
3 Vp-p 6.5
4 Vp-p 2.0
5 Vp-p 124

1. ALL RESISTANCE VALUES IN OHM K=1,000 M=1,000,000.
2. ALL CAPACITOR VALUES IN FARAD U=10^{-6} P=10^{-12}
3. UNLESS OTHERWISE STATED, WORKING VOLTAGES OF CAPACITORS ARE 50 VOLTS.
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TeleVideo Inc.

PCB SCHEMATIC DIAGRAM POWER SUPPLY VIDEO MONITOR 910-950/...

SIZE D REV B

DOCUMENT NO. 29000 D47
REVISION 1, OCT. 1978

PART NUMBER
R6522

Rockwell

R6500 Microcomputer System
DATA SHEET

VERSATILE INTERFACE ADAPTER (VIA)

SYSTEM ABSTRACT

The 8-bit R6500 microcomputer system is produced with N-channel, silicon-gate, depletion-load technology. Its performance speeds are enhanced by advanced system architecture. Its innovative architecture results in smaller chips – the semiconductor threshold to cost-effectivity. System cost-effectivity is further enhanced by providing a family of 10 software-compatible microprocessor (CPU) devices, memory and I/O devices . . . as well as low-cost design aids and documentation.

DESCRIPTION

The R6522 VIA adds two powerful, flexible Interval Timers, a serial-to-parallel/parallel-to-serial shift register and input latching on the peripheral ports to the capabilities of the R6520 Peripheral Interface Adapter (PIA) device. Handshaking capability is expanded to allow control of bidirectional data transfers between VIAs in multiple processor systems and between peripherals.

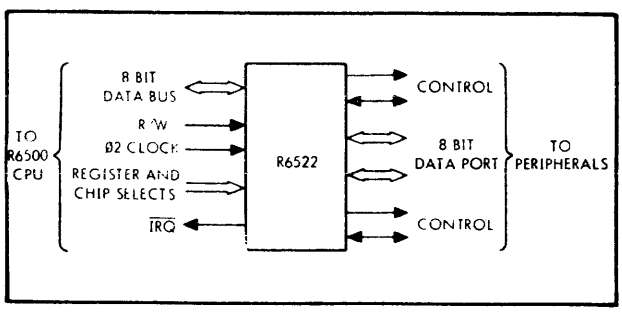
Control of peripherals is primarily through two 8-bit bidirectional ports. Each of these ports can be programmed to act as an input or an output. Peripheral I/O lines can be selectively controlled by the Interval Timers to generate programmable-frequency square waves and/or to count externally generated pulses. Positive control of VIA functions is gained through its internal register organization: Interrupt Flag Register, Interrupt Enable Register, and two Function Control Registers.

FEATURES

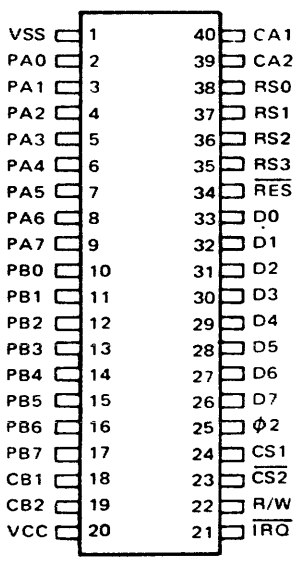
- Organized for simplified software control of many functions
- Compatible with the R650X and R651X family of microprocessors (CPUs)
- Bi-directional, 8-bit data bus for communication with microprocessor
- Two Bi-directional, 8-bit input/output ports for interface with peripheral devices
- CMOS and TTL compatible input/output peripheral ports
- Data Direction Registers allow each peripheral pin to act as either an input or an output
- Interrupt Flag Register allows the microprocessor to readily determine the source of an interrupt and provides convenient control of the interrupts within the chip
- Handshake control logic for input/output peripheral data transfer operations
- Data latching on peripheral input/output ports
- Two fully-programmable interval timers/counters
- Eight-bit Shift Register for serial interface
- Forty-pin plastic or ceramic DIP package.

Ordering Information

Order Number	Package Type	Frequency	Temperature Range
R6522P	Plastic	1 MHz	0°C to +70°C
R6522AP	Plastic	2 MHz	0°C to +70°C
R6522C	Ceramic	1 MHz	0°C to +70°C
R6522AC	Ceramic	2 MHz	0°C to +70°C
R6522PE	Plastic	1 MHz	-40°C to +85°C
R6522APE	Plastic	2 MHz	-40°C to +85°C
R6522CE	Ceramic	1 MHz	-40°C to +85°C
R6522ACE	Ceramic	2 MHz	-40°C to +85°C
R6522CMT	Ceramic	1 MHz	-55°C to +125°C



Basic R6522 Interface Diagram



Pin Configuration

Specifications subject to change without notice

OPERATION SUMMARY

Register Select Lines (RS0, RS1, RS2, RS3)

The four Register select lines are normally connected to the processor address bus lines to allow the processor to select the internal R6522 register which is to be accessed. The sixteen possible combinations access the registers as follows:

RS3	RS2	RS1	RS0	Register	Remarks	RS3	RS2	RS1	RS0	Register	Remarks
L	L	L	L	ORB		H	L	L	L	T2L-L T2C-L	Write Latch Read Counter
L	L	L	H	ORA	Controls Handshake						
L	L	H	L	DDRB		H	L	L	H	T2C-H	Triggers T2L-L/T2C-L Transfer
L	L	H	H	DDRA							
						H	L	H		SR	
L	H	L	L	T1L-L T1C-L	Write Latch Read Counter	H	L	H	H	ACR	
						H	H	L	L	PCR	
L	H	L	H	T1C-H	Trigger T1L-L/T1C-L Transfer	H	H	L	H	IFR	
						H	H	H	L	IER	
L	H	H	L	T1L-L							
L	H	H	H	T1L-H		H	H	H	H	ORA	No Effect on Handshake

Note: L = 0.4V DC, H = 2.4V DC.

Timer 2 Control

RS3	RS2	RS1	RS0	R/W = L	R/W = H
H	L	L	L	Write T2L-L	Read T2C-L Clear Interrupt flag
H	L	L	H	Write T2C-H Transfer T2L-L to T2C-L Clear Interrupt flag	Read T2C-H

Writing the Timer 1 Register

The operations which take place when writing to each of the four T1 addresses are as follows:

RS3	RS2	RS1	RS0	Operation (R/W = L)
L	H	L	L	Write into low order latch Write into high order latch
L	H	L	H	Write into high order counter Transfer low order latch into low order counter Reset T1 interrupt flag
L	H	H	L	Write low order latch
X	H	H	H	Write high order latch Reset T1 interrupt flag

Reading the Timer 1 Registers

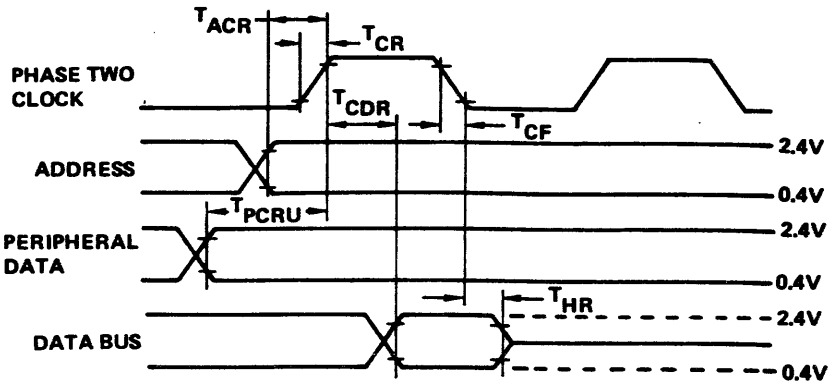
For reading the Timer 1 registers, the four addresses relate directly to the four registers as follows:

RS3	RS2	RS1	RS0	Operation (R/W = H)
L	H	L	L	Read T1 low order counter Reset T1 interrupt flag
L	H	L	H	Read T1 high order counter
L	H	H	L	Read T1 low order latch
L	H	H	H	Read T1 high order latch

TIMING CHARACTERISTICS

Read Timing Characteristics (loading 130 pF and one TTL load)

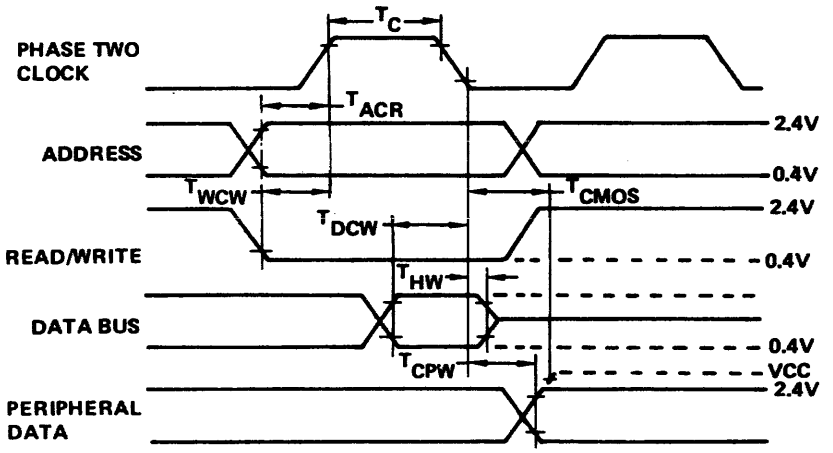
Parameter	Symbol	Min	Typ	Max	Unit
Delay time, address valid to clock positive transition	T_{ACR}	180	–	–	nS
Delay time, clock positive transition to data valid on bus	T_{CDR}	–	–	395	nS
Peripheral data setup time	T_{PCR}	300	–	–	nS
Data bus hold time	T_{HR}	10	–	–	nS
Rise and fall time for clock input	T_{RC} T_{RF}	–	–	25	nS



Read Timing Characteristics

Write Timing Characteristics

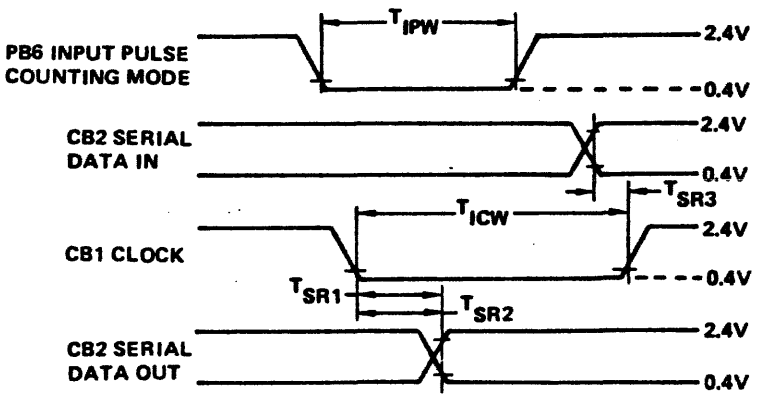
Parameter	Symbol	Min	Typ	Max	Unit
Enable pulse width	T_C	0.47	–	25	μS
Delay time, address valid to clock positive transition	T_{ACW}	180	–	–	nS
Delay time, data valid to clock negative transition	T_{DCW}	300	–	–	nS
Delay time, read/write negative transition to clock positive transition	T_{WCW}	180	–	–	nS
Data bus hold time	T_{HW}	10	–	–	nS
Delay time, Enable negative transition to peripheral data valid	T_{CPW}	–	–	1.0	μS
Delay time, clock negative transition to peripheral data valid CMOS (VCC - 30%)	T_{CMOS}	–	–	2.0	μS



Write Timing Characteristics

I/O Timing Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Rise and fall time for CA1, CB1, CA2 and CB2 input signals	T_{RF}	–	–	1.0	μs
Delay time, clock negative transition to CA2 negative transition (read handshake or pulse mode)	T_{CA2}	–	–	1.0	μs
Delay time, clock negative transition to CA2 positive transition (pulse mode)	T_{RS1}	–	–	1.0	μs
Delay time, CA1 active transition to CA2 positive transition (handshake mode)	T_{RS2}	–	–	2.0	μs
Delay time, clock positive transition to CA2 or CB2 negative transition (write handshake)	T_{WHS}	–	–	1.0	μs
Delay time, peripheral data valid to CB2 negative transition	T_{DC}	0	–	1.5	μs
Delay time, clock positive transition to CA2 or CB2 positive transition (pulse mode)	T_{RS3}	–	–	1.0	μs
Delay time, CB1 active transition to CA2 or CB2 positive transition (handshake mode)	T_{RS4}	–	–	2.0	μs
Delay time, peripheral data valid to CA1 or CB1 active transition (input latching)	T_{IL}	300	–	–	ns
Delay time CB1 negative transition to CB2 data valid (internal SR clock, shift out)	T_{SR1}	–	–	300	ns
Delay time, negative transition of CB1 input clock to CB2 data valid (external clock, shift out)	T_{SR2}	–	–	300	ns
Delay time, CB2 data valid to positive transition of CB1 clock (shift in, internal or external clock)	T_{SR3}	–	–	300	ns
Pulse Width – PB6 Input Pulse	T_{IPW}	2	–	–	μs
Pulse Width – CB1 Input Clock	T_{ICW}	2	–	–	μs
Pulse Spacing – PB6 Input Pulse	I_{IPS}	2	–	–	μs
Pulse Spacing – CB1 Input Pulse	I_{ICS}	2	–	–	μs



I/O Timing Characteristics

Timer 1 Operating Modes

Two bits are provided in the Auxiliary Control Register to allow selection of the T1 operating modes. These bits and the four possible modes are as follows:

ACR7 Output Enable	ACR6 "Free-Run" Enable	Mode
0	0	Generate a single time-out interrupt each time T1 is loaded
0	1	Generate continuous interrupts
1	0	Generate a single interrupt and an output pulse on PB7 for each T1 load operation
1	1	Generate continuous interrupts and a square wave output on PB7

FUNCTION CONTROL

Control of the various functions and operating modes within the R6522 is accomplished primarily through two registers, the Peripheral Control Register (PCR), and the Auxiliary Control Register (ACR). The PCR is used primarily to select the operating mode for the four peripheral control pins. The Auxiliary Control Register selects the operating mode for the Interval Timers (T1, T2), and the Serial Port (SR).

Peripheral Control Register

The Peripheral Control Register is organized as follows:

Bit #	7	6	5	4	3	2	1	0
Function	CB2 Control			CB1 Control	CA2 Control			CA1 Control

Typical functions are shown below:

PCR3	PCR2	PCR1	Mode
0	0	0	Input mode – Set CA2 interrupt flag (IFR0) on a negative transition of the input signal. Clear IFR0 on a read or write of the Peripheral A Output Register.
0	0	1	Independent interrupt input mode – Set IFR0 on a negative transition of the CA2 input signal. Reading or writing ORA does not clear the CA2 interrupt flag.
0	1	0	Input mode – Set CA2 interrupt flag on a positive transition of the CA2 input signal. Clear IFR0 with a read or write of the Peripheral A Output Register.
0	1	1	Independent interrupt input mode – Set IFR0 on a positive transition of the CA2 input signal. Reading or writing ORA does not clear the CA2 interrupt flag.
1	0	0	Handshake output mode – Set CA2 output low on a read or write of the Peripheral A Output Register. Reset CA2 high with an active transition on CA1.
1	0	1	Pulse output mode – CA2 goes low for one cycle following a read or write of the Peripheral A Output Register.
1	1	0	Manual output mode – The CA2 output is held low in this mode.
1	1	1	Manual output mode – The CA2 output is held high in this mode.

Auxiliary Control Register

Many of the functions in the Auxiliary Control Register have been discussed previously. However, a summary of this register is presented here as a convenient reference for the R6522 user. The Auxiliary Control Register is organized as follows:

Bit #	7	6	5	4	3	2	1	0
Function	T1 Control		T2 Control	Shift Register Control			PB Latch Enable	PA Latch Enable

Shift Register Control

The Shift Register operating mode is selected as follows:

ACR4	ACR3	ACR2	Mode
0	0	0	Shift Register Disabled.
0	0	1	Shift in under control of Timer 2.
0	1	0	Shift in under control of system clock.
0	1	1	Shift in under control of external clock pulses.
1	0	0	Free-running output at rate determined by Timer 2.
1	0	1	Shift out under control of Timer 2.
1	1	0	Shift out under control of the system clock.
1	1	1	Shift out under control of external clock pulses.

T2 Control

Timer 2 operates in two modes. If ACR5 = 0, T2 acts as an interval timer in the one-shot mode. If ACR5 = 1, Timer 2 acts to count a predetermined number of pulses on pin PB6.

Rockwell

R6500 Microcomputer System
DATA SHEET

CRT CONTROLLER (CRTC)

DESCRIPTION

The R6545-1 CRT Controller (CRTC) is designed to interface an 8-bit microprocessor to CRT raster scan video displays, and adds an advanced CRT controller to the established and expanding line of R6500 products.

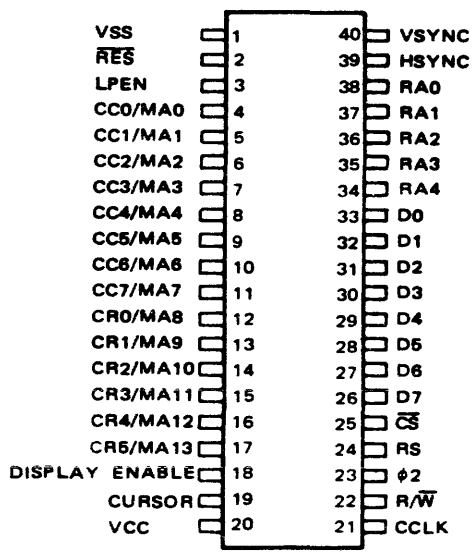
The R6545-1 provides refresh memory addresses and character generator row addresses which allow up to 16K characters with 32 scan lines per character to be addressed. A major advantage of the R6545-1 is that the refresh memory may be addressed in either straight binary or by row/column.

Other functions in the R6545-1 include an internal cursor register which generates a cursor output when its contents are equal to the current refresh address. Programmable cursor start and end registers allow a cursor of up to the full character scan in height to be placed on any scan lines of the character. Variable cursor display blink rates are provided. A light pen strobe input allows capture of the current refresh address in an internal light pen register. The refresh address lines are configured to provide direct dynamic memory refresh.

All timing for the video refresh memory signals is derived from the character clock input. Shift register, latch, and multiplex control signals (when needed) are provided by external high-speed timing. The mode control register allows non-interlaced video display modes at 50 or 60 Hz refresh rate. The internal status register may be used to monitor the R6545-1 operation. The $\overline{RES}$ input allows the CRTC-generated field rate to be dynamically-synchronized with line frequency jitter.

FEATURES

- Compatible with 8-bit microprocessors
- Up to 2.5 MHz character clock operation
- Refresh RAM may be configured in row/column or straight binary addressing
- Alphanumeric and limited graphics capability
- Up and down scrolling by page, line, or character
- Programmable Vertical Sync Width
- Fully programmable display (rows, columns, character matrix)
- Non-interlaced scan
- 50/60 Hz operation
- Fully programmable cursor
- Light pen register
- Addresses refresh RAM to 16K characters
- No external DMA required
- Internal status register
- 40-Pin ceramic or plastic DIP
- Pin-compatible with MC6845
- Single +5 ±5% Volt Power Supply



R6545-1 Pin Configuration

ORDERING INFORMATION

Part Number	Package Type	Frequency	Temperature Range
R6545-1P	Plastic	1 MHz	0°C to +70°C
R6545-1AP	Plastic	2 MHz	0°C to +70°C
R6545-1C	Ceramic	1 MHz	0°C to +70°C
R6545-1AC	Ceramic	2 MHz	0°C to +70°C

CRT CONTROLLER (CRTC)

Specifications subject to change without notice
Document No. 29000 D67
December 1980

INTERFACE SIGNAL DESCRIPTION

CPU INTERFACE

ϕ2 (Phase 2 Clock)

The input clock is the system Phase 2 (ϕ2) clock and is used to trigger all data transfers between the system processor (CPU) and the R6545-1. Since there is no maximum limit to the allowable ϕ2 clock time, it is not necessary for it to be a continuous clock. This capability permits the R6545-1 to be easily interfaced to non-6500 compatible microprocessors.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ input signal generated by the processor is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the R6545-1, a low on the R/$\overline{W}$ pin allows data on data lines D0-D7 to be written into the R6545-1.

$\overline{CS}$ (Chip Select)

The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The R6545-1 is selected when $\overline{CS}$ is low.

RS (Register Select)

The Register Select input is used to access internal registers. A low on this pin permits writes (R/$\overline{W}$ = low) into the Address Register and reads (R/$\overline{W}$ = high) from the Status Register. The contents of the Address Register is the identity of the register accessed when RS is high.

D0-D7 (Data Bus)

D0-D7 are the eight data lines used to transfer data between the processor and the R6545-1. These lines are bidirectional and are normally high-impedance except during read cycles when the chip is selected ($\overline{CS}$ = low).

VIDEO INTERFACE

HSYNC (Horizontal Sync)

The HSYNC signal is an active-high output used to determine the horizontal position of displayed text. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC (Vertical Sync)

The VSYNC signal is an active high output used to determine the vertical position of displayed text. Like HSYNC, VSYNC may be used to drive a CRT monitor or composite video generation circuits. VSYNC time position and width are both programmable.

DISPLAY ENABLE (Display Enable)

The DISPLAY ENABLE signal is an active-high output used to indicate when the R6545-1 is generating active display information. The number of horizontal display characters per row and the number of vertical display rows are both fully programmable and together are used to generate the DISPLAY ENABLE signal. DISPLAY ENABLE can be delayed one character time by setting bit 4 of R8 equal to 1.

CURSOR (Cursor Coincidence)

The CURSOR signal is an active-high output used to indicate when the scan coincides with the programmed cursor position. The cursor position may be programmed to be any character in the address field. Furthermore, within the character, the cursor may be programmed to be any block of scan lines, since the start scan line and the end scan line are both programmable. The cursor position may be delayed by one character time by setting Bit 5 of R8 to A "1".

LPEN (Light Pen Strobe)

The LPEN signal is an edge-sensitive input used to load the internal Light Pen Register with the contents of the Refresh Scan Counter at the time the active edge occurs. The active edge of LPEN is the low-to-high transition.

CCLK (Clock)

The CCLK signal is the character timing clock input and is used as the time base for all internal count/control functions.

$\overline{RES}$

The $\overline{RES}$ signal is an active-low input used to initialize all internal scan counter circuits. When $\overline{RES}$ is low, all internal counters are stopped and cleared, all scan and video outputs are low, and control registers are unaffected. $\overline{RES}$ must stay low for at least one CCLK period. All scan timing is initiated when $\overline{RES}$ goes high. In this way, $\overline{RES}$ can be used to synchronize display frame timing with line frequency. $\overline{RES}$ may also be used to synchronize multiple CRTC's in horizontal and/or vertical split screen operation.

REFRESH RAM AND CHARACTER ROM INTERFACE

MA0-MA13 (Refresh RAM Address Lines)

These 14 signals are active-high outputs used to address the Refresh RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters/line and lines/frame.

There are two selectable address modes for MA0-MA13:

In the straight binary mode (R8, Mode Control, bit 2 = "0"), characters are stored in successive memory locations. Thus, the software must be designed such that row and column character coordinates are translated into sequentially-numbered addresses. In the row/column mode (R8, Mode Control, bit 2 = "1"), MA0-MA7 become column addresses CC0-CC7 and MA8-MA13 become row addresses CR0-CR5. In this case, the software can manipulate characters in terms of row and column locations, but additional address compression circuits are needed to convert the CC0-CC7 and CR0-CR5 addresses into a memory-efficient binary address scheme.

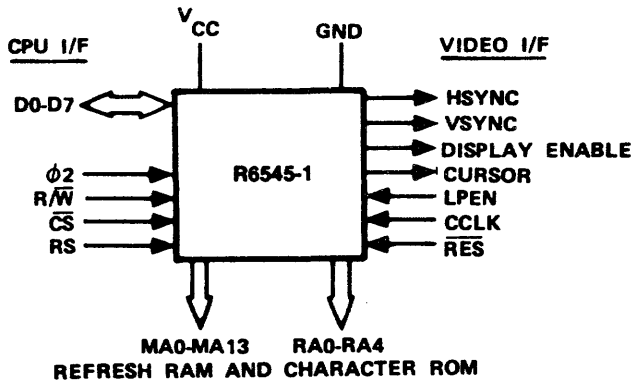
RA0-RA4 (Raster Address Lines)

These 5 signals are active-high outputs used to select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

INTERNAL REGISTER ORGANIZATION

$\overline{CS}$	RS	Address Register 4	3	2	1	0	Reg. No.	Register Name	Register Units	Read ($R/\overline{W}$ = High)	Write ($R/\overline{W}$ = Low)	Register Bit 7	6	5	4	3	2	1	0
1	X	X	X	X	X	X	X												
0	0	X	X	X	X	X	X	Address Register	Register No.		✓				4	3	2	1	0
0	0	X	X	X	X	X	X	Status Register	-	✓			6	5					
0	1	0	0	0	0	0	R0	Horizontal Total Char	No. of Characters/Row		✓	7	6	5	4	3	2	1	0
0	1	0	0	0	0	1	R1	Horizontal Displayed Char	No. of Characters/Row		✓	7	6	5	4	3	2	1	0
0	1	0	0	0	1	0	R2	Horizontal Sync Position	Character Position		✓	7	6	5	4	3	2	1	0
0	1	0	0	0	1	1	R3	YSYNC, HSYNC Widths	No. of Scan Lines, Characters		✓	7	6	5	4	3	2	1	0
0	1	0	0	1	0	0	R4	Vertical Total Rows	No. of Character Rows		✓		6	5	4	3	2	1	0
0	1	0	0	1	0	1	R5	Vertical Total Adjust Lines	No. of Scan Lines		✓				4	3	2	1	0
0	1	0	0	1	1	0	R6	Vertical Displayed Rows	No. of Character Rows		✓		6	5	4	3	2	1	0
0	1	0	0	1	1	1	R7	Vertical Sync Position	No. of Character Rows		✓		6	5	4	3	2	1	0
0	1	0	1	0	0	0	R8	Mode Control	-		✓	7	6	5	4	3	2	1	0
0	1	0	1	0	0	1	R9	Scan Line	No. of Scan Lines		✓				4	3	2	1	0
0	1	0	1	0	1	0	R10	Cursor Start Line	Scan Line No.		✓		6	5	4	3	2	1	0
0	1	0	1	0	1	1	R11	Cursor End Line	Scan Line No.		✓				4	3	2	1	0
0	1	0	1	1	0	0	R12	Display Start Address (H)	-		✓			5	4	3	2	1	0
0	1	0	1	1	0	1	R13	Display Start Address (L)	-		✓	7	6	5	4	3	2	1	0
0	1	0	1	1	1	0	R14	Cursor Position Address (H)	-	✓	✓			5	4	3	2	1	0
0	1	0	1	1	1	1	R15	Cursor Position Address (L)	-	✓	✓	7	6	5	4	3	2	1	0
0	1	1	0	0	0	0	R16	Light Pen Register (H)	-	✓				5	4	3	2	1	0
0	1	1	0	0	0	1	R17	Light Pen Register (L)	-	✓		7	6	5	4	3	2	1	0

Table 1. Overall Register Structure and Addressing



R6545-1 Interface Diagram

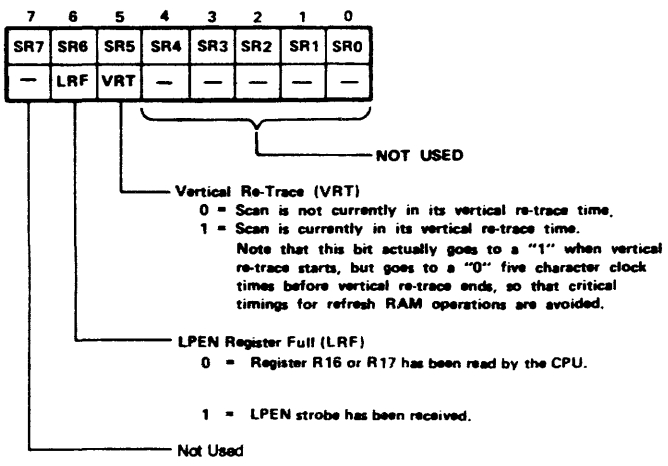
INTERNAL REGISTER DESCRIPTION

ADDRESS REGISTER

This 5-bit write-only register is used as a "pointer" to direct CRTC/CPU data transfers within the CRTC. Its contents is the number of the desired register (0-17). When $\overline{CS}$ and RS are low, then this register may be loaded; when $\overline{CS}$ is low and RS is high, then the register selected is the one whose identity is stored in this address register.

STATUS REGISTER (SR)

This 8-bit register contains the status of the CRTC. Only two bits are assigned, as follows:



NOTE: The Status Register takes the State, | – | 0 | 1 | – | – | – | – | – | immediately after power (V_{CC}) turn-on.

R0—HORIZONTAL TOTAL CHARACTERS

This 8-bit write-only register contains the total of displayed and non-displayed characters, minus one, per horizontal line. The frequency of HSYNC is thus determined by this register.

R1—HORIZONTAL DISPLAYED CHARACTERS

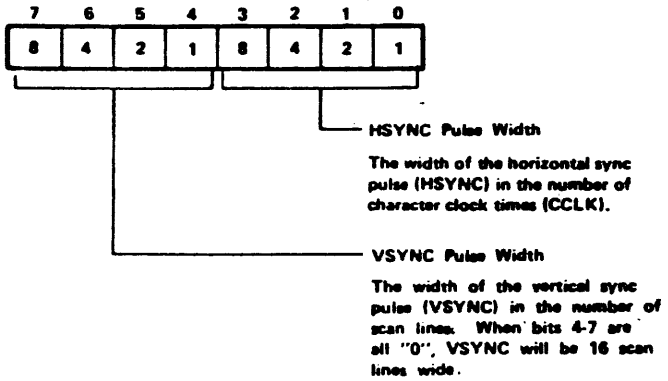
This 8-bit write-only register contains the number of displayed characters per horizontal line.

R2—HORIZONTAL SYNC POSITION

This 8-bit write-only register contains the position of the horizontal SYNC on the horizontal line, in terms of the character location number on the line. The position of the HSYNC determines the left to right location of the displayed text on the video screen. In this way, the side margins are adjusted.

R3—HORIZONTAL AND VERTICAL SYNC WIDTHS

This 8-bit write-only register contains the widths of both HSYNC and VSYNC, as follows:



Control of these parameters allows the R6545-1 to be interfaced to a variety of CRT monitors, since the HSYNC and VSYNC timing signals may be accommodated without the use of external one shot timing.

R4—VERTICAL TOTAL ROWS

The Vertical Total Register is a 7-bit register containing the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to be longer than the period of the line frequency, then $\overline{RES}$ may be used to provide absolute synchronism.

R5—VERTICAL TOTAL LINE ADJUST

The Vertical Total Line Adjust Register (R5) is a 5-bit write-only register containing the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

R6—VERTICAL DISPLAYED ROWS

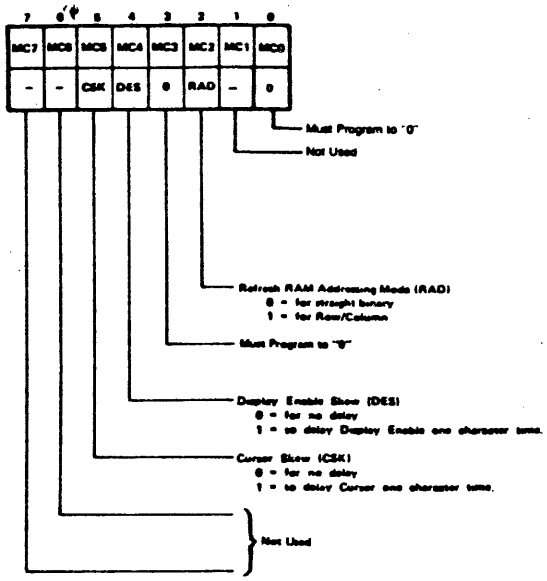
This 7-bit write-only register contains the number of displayed character rows in each frame.

R7—VERTICAL SYNC POSITION

This 7-bit write-only register is used to select the character row time at which the vertical SYNC pulse is desired to occur and, thus, is used to position the displayed text in the vertical direction.

R8—MODE CONTROL (MC)

This 8-bit write-only register selects the operating modes of the R6545-1, as follows:



R9—ROW SCAN LINES

This 5-bit write-only register contains the number of scan lines, minus one, per character row, including spacing.

R10—CURSOR START LINE
R11—CURSOR END LINE

These 5-bit write-only registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R10 are used to select the cursor blink mode, as follows:

Bit 6	Bit 5	Cursor Blink Mode
0	0	Display Cursor Continuously
0	1	Blank Cursor Continuously
1	0	Blink Cursor at 1/16 Field Rate
1	1	Blink Cursor at 1/32 Field Rate

R12—DISPLAY START ADDRESS HIGH
R13—DISPLAY START ADDRESS LOW

These registers form a 14-bit register whose contents is the memory address of the first character of the displayed scan (the character on the top left of the video display, as in Figure 1). Subsequent memory addresses are generated by the R6545-1 as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address associated with the first character of the desired line of text to be displayed first. Entire pages of text may be scrolled or changed as well via R12 and R13.

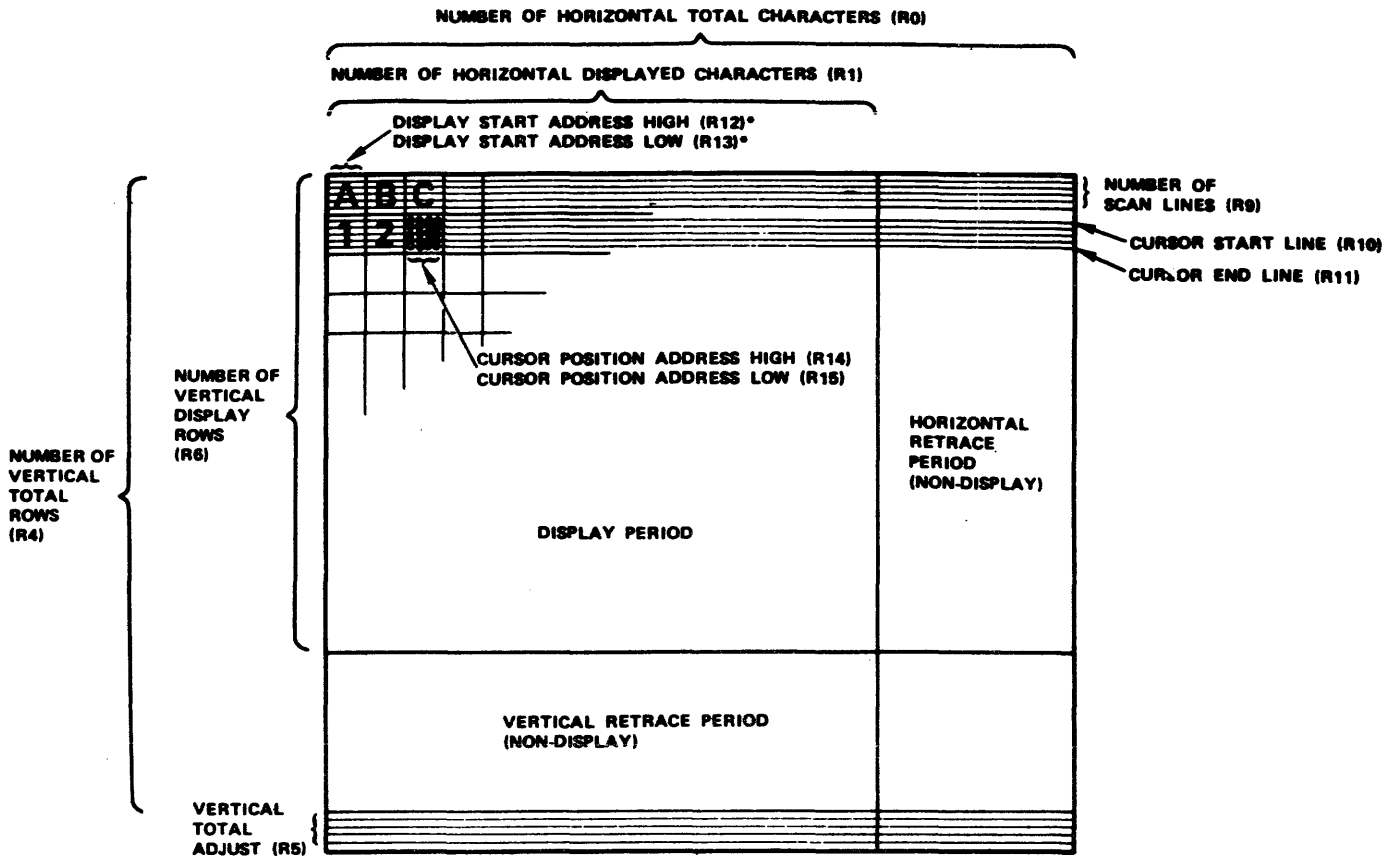


Figure 1. Video Display Format

R14—CURSOR POSITION HIGH
R15—CURSOR POSITION LOW

These registers form a 14-bit register whose contents is the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, then the CURSOR output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the CURSOR output by a full CCLK time to accommodate slow access memories.

R16—LIGHT PEN HIGH
R17—LIGHT PEN LOW

These registers form a 14-bit register whose contents is the light pen strobe position, in terms of the video display address at which the strobe occurred. When the LPEN input changes from low to high, then, on the next negative-going edge of CCLK, the contents of the internal scan counter is stored in registers R16 and R17.

REGISTER FORMATS

Register pairs R12/R13, R14/R15, and R16/R17 are formatted in one of two ways:

(1) Straight binary, if register R8, bit 2 = "0".

(2) Row/Column, if register R8, bit 2 = "1". In this case the low byte is the Character Column and the high byte is the Character Row.

DESCRIPTION OF OPERATION

VIDEO DISPLAY

Figure 1 indicates the relationship of the various program registers in the R6545-1 and the resultant video display.

Non-displayed areas of the Video Display are used for horizontal and vertical retrace functions of the CRT monitor. The horizontal and vertical sync signals, HSYNC and VSYNC, are programmed to occur during these intervals and are used to trigger the retrace in the CRT monitor. The pulse widths are constrained by the monitor requirements. The time position of the pulses may be adjusted to vary the display margins (left, right, top, and bottom).

REFRESH RAM ADDRESSING

Shared Memory Mode (R8, bit 3 = "0")

In this mode, the Refresh RAM address lines (MA0-MA13) directly reflect the contents of the internal refresh scan character counter. Multiplex control, to permit addressing and selection of the RAM by both the CPU and the CRTC, must be provided external to the CRTC. In the Row/Column address mode, lines MA0-MA7 become character column addresses (CC0-CC7) and MA8-MA13 become character row addresses (CR0-CR5).

ADDRESSING MODES

Row/Column

In this mode, the CRTC address lines (MA0-MA13) are generated as 8 column (MA0-MA7) and 6 row (MA8-MA13) addresses. Extra hardware is needed to compress this addressing into a straight binary sequence in order to conserve memory in the refresh RAM.

Binary

In this mode, the CRTC address lines are straight binary and no compression circuits are needed. However, software complexity is increased since the CRT characters cannot be stored in terms of their row and column locations, but must be sequential.

USE OF DYNAMIC RAM FOR REFRESH MEMORY

The R6545-1 permits the use of dynamic RAMS as storage devices for the Refresh RAM by continuing to increment memory addresses in the non-display intervals of the scan. This is a viable technique, since the Display Enable signal controls the actual video display blanking. Figure 2 illustrates Refresh RAM addressing for the case of binary addressing for 80 columns and 24 rows with 10 non-displayed columns and 10 non-displayed rows.

TOTAL = 90

DISPLAY = 80

TOTAL = 34

DISPLAY = 24

0	1	2	3		76	77	78	79	80	81	89
80	81	82	83		156	157	158	159	160	161	169
160	161	162				237	238	239	240		249
240	241	242				317	318	319	320		329
1680	1681	1682				1757	1758	1759	1760		1769
1760	1761	1762				1837	1838	1839	1840		1849
1840	1841	1842				1917	1918	1919	1920		1929
1920	1921	1922				1997	1998	1999	2000		2009
2000	2001	2002				2077	2078	2079	2080		2089
2640	2641	2642				2717	2718	2720			2729

Figure 2. Memory Addressing Example (80 x 24)

CURSOR OPERATION

A one character wide cursor can be controlled by storing values into the Cursor Start Line (R10) and Cursor End Line (R11) registers and into the Cursor Position Address High (R14) and Cursor Position Low (R15) registers.

Bits 5 and 6 in the Cursor Start Line High Register (R10) control the cursor display and blink rate as follows:

Bit 6	Bit 5	Cursor Operating Mode
0	0	Display Cursor Continuously
0	1	Blank Cursor Continuously
1	0	Blink Cursor at 1/16 Field Rate
1	1	Blink Cursor at 1/32 Field Rate

The cursor of up to 32 characters in height can be displayed on and between the scan lines as loaded into the Cursor Start Line (R10) and Cursor End Line (R11) Registers.

The cursor is positioned on the screen by loading the Cursor Position Address High (R14) and Cursor Position Address Low (R15) registers with the desired refresh RAM address. The cursor can be positioned in any of the 16K character positions. Hardware paging and data scrolling is thus allowed without loss of cursor position. Figure 3 is an example of the display cursor scan line.

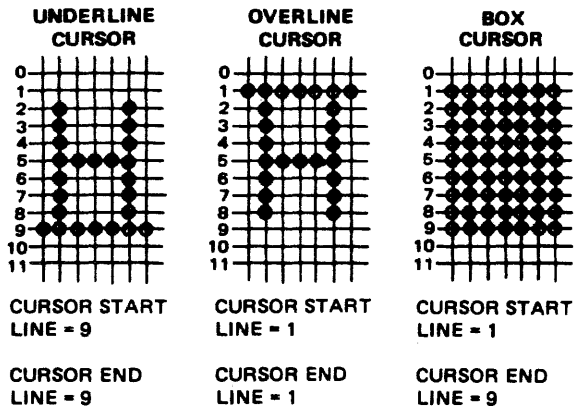


Figure 3. Cursor Display Scan Line Control Examples

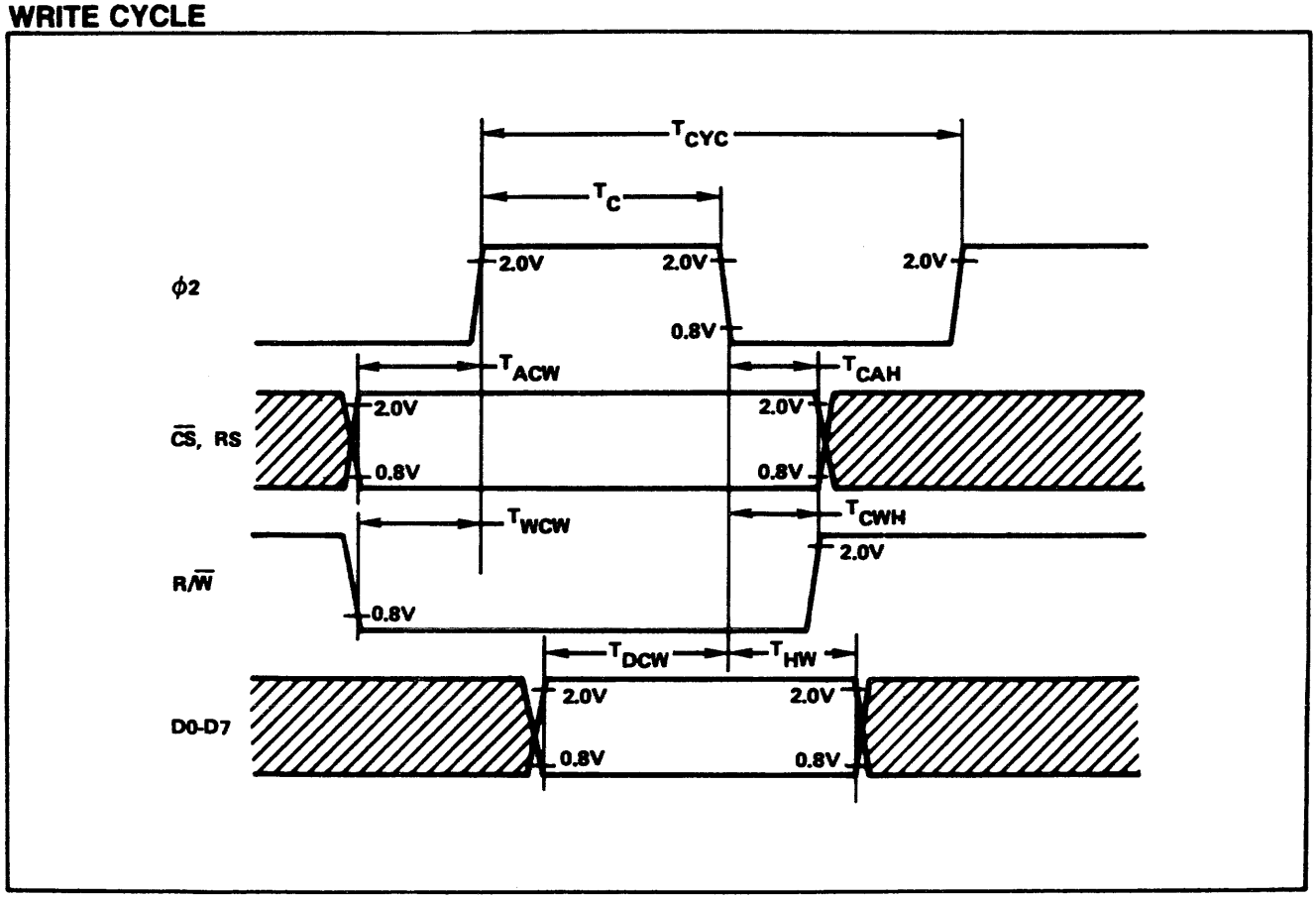
MPU WRITE TIMING CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Cycle Time	T_{CYC}	1.0	–	0.5	–	μs
Ø2 Pulse Width	T_C	440	–	200	–	ns
Address Set-Up Time	T_{ACW}	180	–	90	–	ns
Address Hold Time	T_{CAH}	0	–	0	–	ns
R/$\overline{W}$ Set-Up Time	T_{WCW}	180	–	90	–	ns
R/$\overline{W}$ Hold Time	T_{CWH}	0	–	0	–	ns
Data Bus Set-Up Time	T_{DCW}	265	–	100	–	ns
Data Bus Hold Time	T_{HW}	10	–	10	–	ns

(t_r and t_f = 10 to 30 ns)

WRITE CYCLE



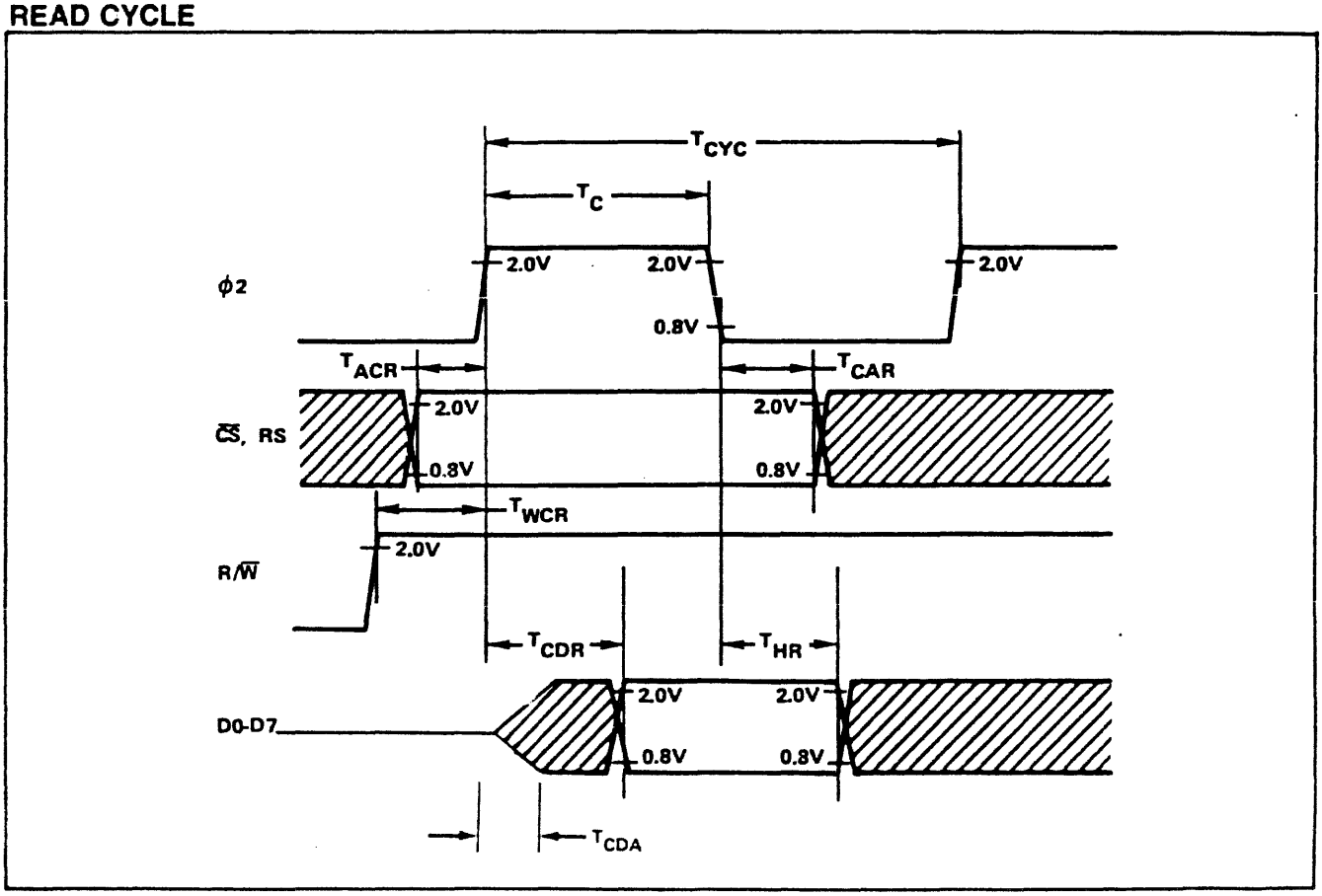
MPU READ TIMING CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Cycle Time	T_{CYC}	1.0	–	0.5	–	μs
Ø2 Pulse Width	T_C	440	–	200	–	ns
Address Set-Up Time	T_{ACR}	180	–	90	–	ns
Address Hold Time	T_{CAR}	0	–	0	–	ns
R/$\overline{W}$ Set-Up Time	T_{WCR}	180	–	90	–	ns
Read Access Time	T_{CDR}	–	340	–	150	ns
Read Hold Time	T_{HR}	10	–	10	–	ns
Data Bus Active Time (Invalid Data)	T_{CDA}	40	–	40	–	ns

(t_r and t_f = 10 to 30 ns)

READ CYCLE



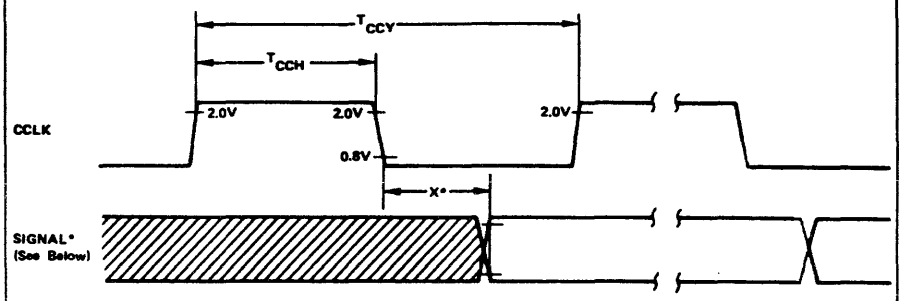
MEMORY AND VIDEO INTERFACE CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristics	Symbol	1 MHz		2 MHz		Units
		Min	Max	Min	Max	
Char. Clock Cycle Time	T_{CCY}	0.4	40	0.4	40	µs
Char. Clock Pulse Width	T_{CCH}	200	–	200	–	ns
MA0-MA13 Propagation Delay	T_{MAD}	–	300	–	300	ns
RA0-RA4 Propagation Delay	T_{RAD}	–	300	–	300	ns
DISPLAY ENABLE Prop. Delay	T_{DTD}	–	450	–	450	ns
HYSNC Propagation Delay	T_{HSD}	–	450	–	450	ns
VSYNC Propagation	T_{VSD}	–	450	–	450	ns
Cursor Propagation Delay	T_{CDD}	–	450	–	450	ns
LPEN Strobe Width	T_{LPH}	150	–	150	–	ns
LPEN to CCLK Delay	T_{LP1}	20	–	20	–	ns
CCLK to LPEN Delay	T_{LP2}	0	–	0	–	ns

t_r, t_f = 20 ns (max)

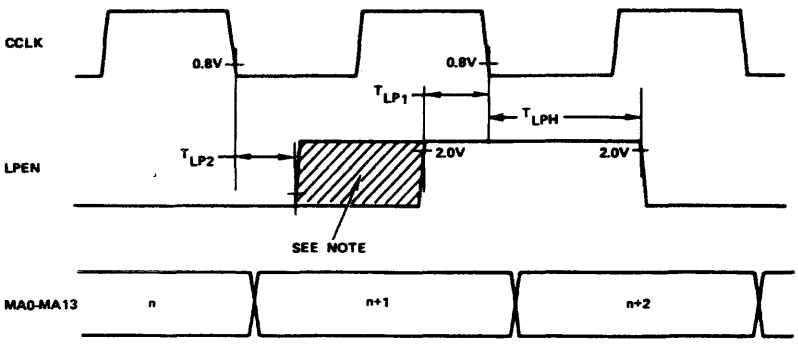
SYSTEM TIMING DEFINITIONS



*

SIGNAL	SIGNAL SYMBOL (X)
MA0-MA13	T_{MAD}
RA0-RA4	T_{RAD}
DISPLAY ENABLE	T_{DTD}
HSYNC	T_{HSD}
VSYNC	T_{VSD}
CURSOR	T_{CDD}

LIGHT PEN STROBE TIMING DEFINITIONS



NOTE:

SLASH AREA DEFINES THE "WINDOW" IN WHICH AN LPEN POSITIVE EDGE WILL CAUSE ADDRESS N+2 TO LOAD INTO LIGHT PEN REGISTER. TRANSITIONS ON EITHER SIDE OF THIS "WINDOW" WILL RESULT IN UNPREDICTABLE VALUES BEING LOADED INTO THE LIGHT PEN REGISTER.

SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{IN}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_{OP}	0 to +70	°C
Storage Temperature	T_{STG}	-55 to 150	°C

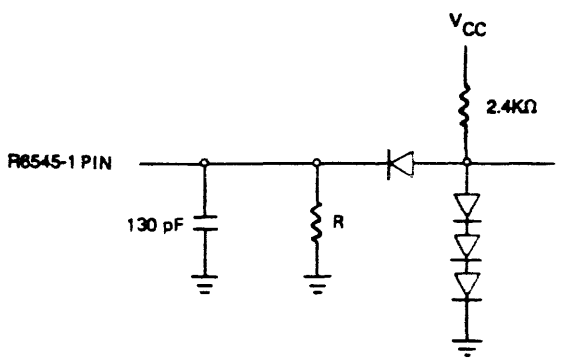
All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be taken to prevent unnecessary application of voltages in excess of the allowable limits.

Electrical Characteristics

(V_{CC} = 5.0V ±5%, T_A = 0-70°C, unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2.0	V_{CC}	Vdc
Input Low Voltage	V_{IL}	0.3	0.8	Vdc
Input Leakage (Ø2, R/$\overline{W}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK)	I_{IN}	–	2.5	μAdc
Three-State Input Leakage (D0-D7) (V_{IN} = 0.4 to 2.4V)	I_{TSI}	–	10.0	μAdc
Output High Voltage I_{LOAD} = 205 μAdc (D0-D7) I_{LOAD} = 100 μAdc (all others)	V_{OH}	2.4	–	Vdc
Output Low Voltage I_{LOAD} = 1.6 mAdc	V_{OL}	–	0.4	Vdc
Power Dissipation	P_D	–	1000	mW
Input Capacitance				
Ø2, R/$\overline{W}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK	C_{IN}	–	10.0	pF
D0-D7		–	12.5	pF
Output Capacitance	C_{OUT}	–	10.0	pF

TEST LOAD



R=11KΩ FOR D0-D7
=24KΩ FOR ALL OTHER OUTPUTS

PART NUMBER
R6551

Rockwell

R6500 Microcomputer System
DATA SHEET

Asynchronous Communication Interface Adapter (ACIA)

The R6551 Asynchronous Communication Interface Adapter (ACIA) provides a program-controlled interface between 8-bit microprocessor-based systems and serial communication data sets and modems.

With its on-chip baud rate generator, the R6551 is capable of transmitting at 15 different program-selectable rates between 50 baud and 19,200 baud, and receiving at either the transmit rate or at 16 times an external clock rate. The R6551 has programmable word lengths of 5, 6, 7, or 8 bits; even, odd or no parity; 1, 1-1/2 or 2 stop bits.

With the R6551, a crystal is the only required external support component – eliminating the multiple-component support that is typically needed.

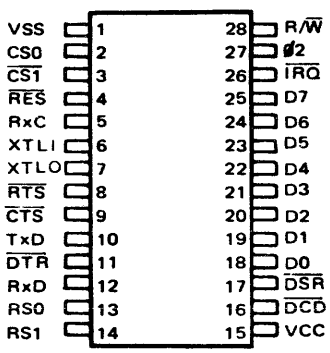
In addition, the R6551 is designed for maximum programmed control from the CPU, to simplify hardware implementation. A control register and a separate command register permit the CPU to easily select the R6551's operating modes and check data, parameters and status.

FEATURES

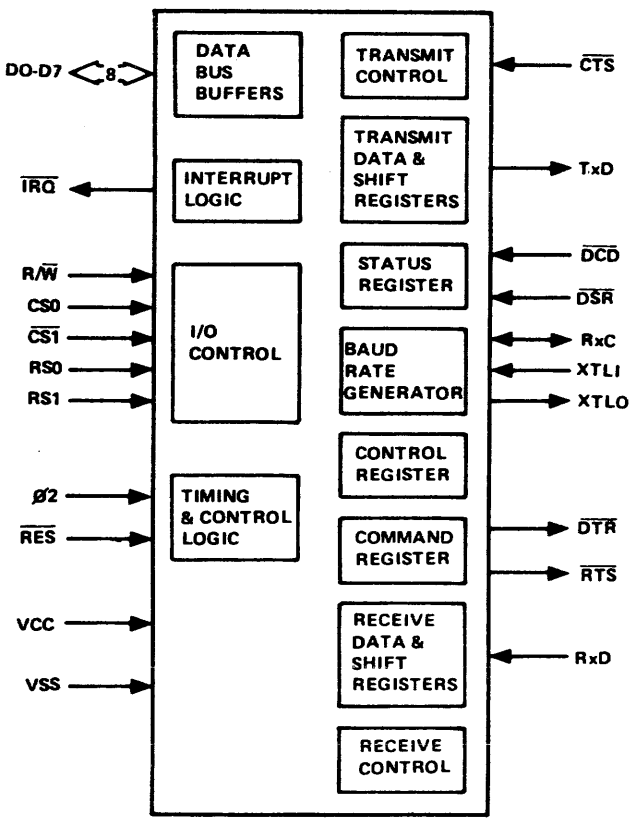
- Compatible with 8-bit microprocessors
- Full duplex or half duplex operation with buffered receiver and transmitter
- 15 programmable Baud Rates (50 to 19,200)
- Receiver data rate may be identical to baud rate or may be 16 times the external clock input
- Data set/modem control functions
- Programmable word lengths, number of stop bits, and parity bit generation and detection
- Programmable interrupt control
- Software reset
- Program-selectable serial echo mode
- Two chip selects
- 2 MHz or 1 MHz clock rate
- Single +5V ±5% power supply
- 28-pin plastic or ceramic DIP
- Full TTL compatibility

Ordering Information

Order Number	Package Type	Frequency	Temperature Range
R6551P	Plastic	1 MHz	0°C to +70°C
R6551AP	Plastic	2 MHz	0°C to +70°C
R6551C	Ceramic	1 MHz	0°C to +70°C
R6551AC	Ceramic	2 MHz	0°C to +70°C



R6551 Pin Configuration

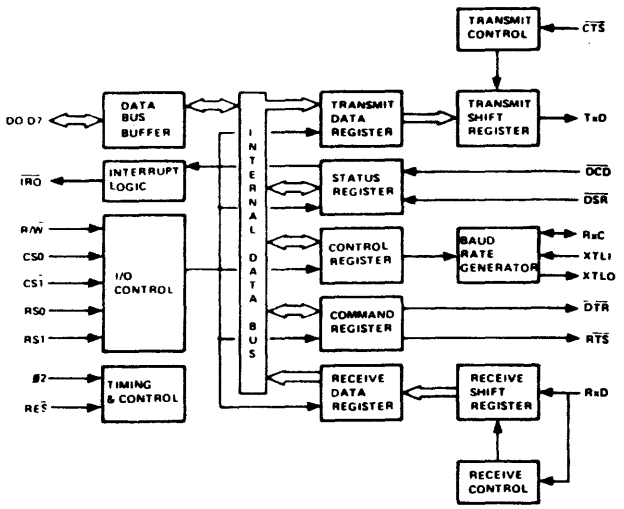


R6551 Interface Diagram

Asynchronous Communication Interface Adapter (ACIA)

Specifications subject to change without notice
Document No. 29000 D53
Rev. 1, January 1981

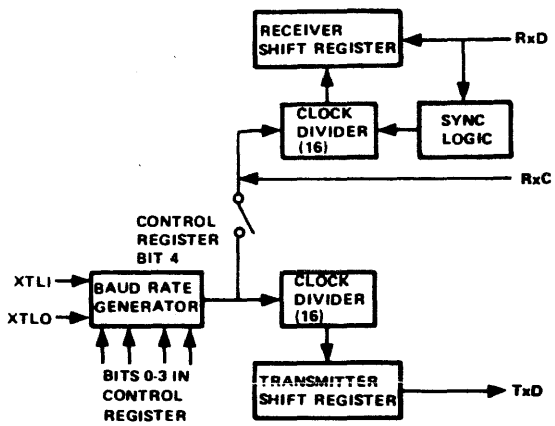
INTERNAL ORGANIZATION



R6551 Block Diagram

Transmitter/Receiver

Bits 0-3 of the Control Register select the divisor used to generate the baud rate for the Transmitter. If the Receiver clock is to use the same baud rate as the Transmitter, then RxC becomes an output pin and can be used to slave other circuits to the R6551.



Transmitter/Receiver Clock Circuits

Transmit and Receive Data Registers

These registers are used as temporary data storage for the 6551 Transmit and Receive circuits. The Transmit Data Register is characterized as follows:

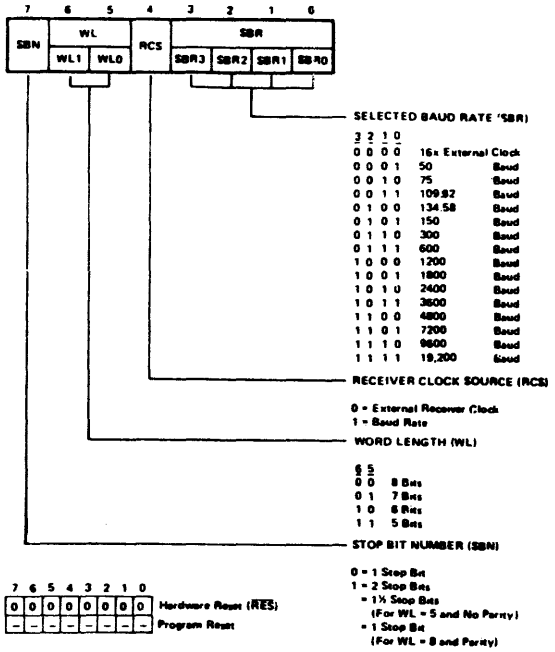
- Bit 0 is the leading bit to be transmitted.
- Unused data bits are the high-order bits and are "don't care" for transmission.

The Receive Data Register is characterized in a similar fashion:

- Bit 0 is the leading bit received.
- Unused data bits are the high-order bits and are "0" for the receiver.
- Parity bits are not contained in the Receive Data Register, but are stripped-off after being used for external parity checking. Parity and all unused high-order bits are "0".

Control Register

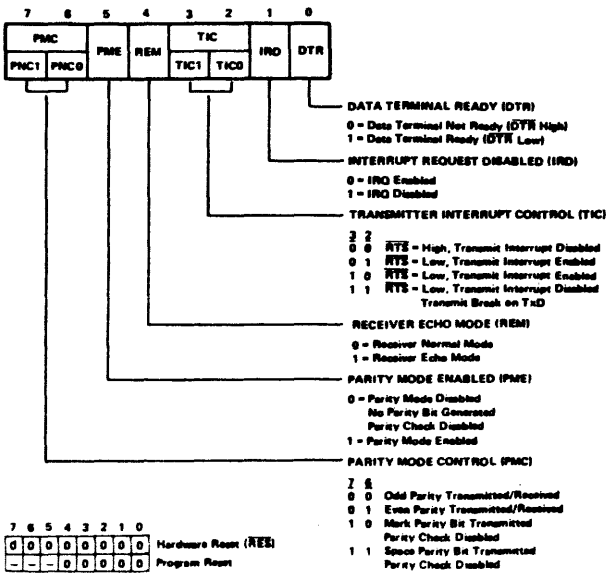
The Control Register selects the desired baud rate, frequency source, word length, and the number of stop bits.



R6551 Control Register

Command Register

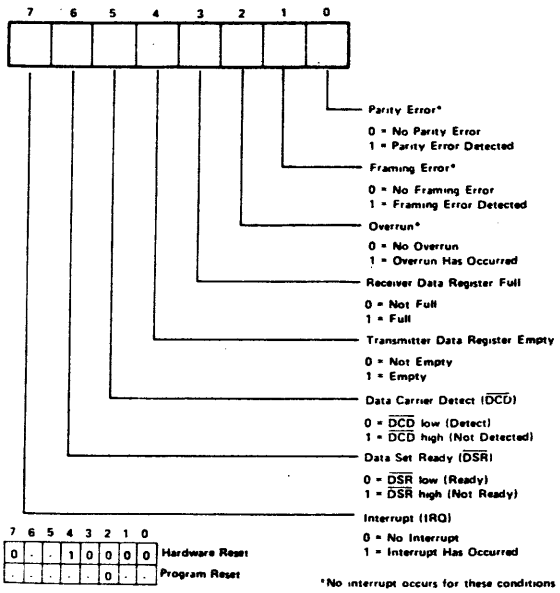
The Command Register controls specific modes and functions.



R6551 Command Register

Status Register

The Status Register reports the status of various R6551 functions



R6551 Status Register

INTERFACE SIGNAL DESCRIPTION

$\overline{RES}$ (Reset)

During system initialization a low on the $\overline{RES}$ input will cause internal registers to be cleared.

Ø2 (Input Clock)

The input clock is the system Ø2 clock and is used to synchronize all data transfers between the system microprocessor and the R6551.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the R6551. A low on the R/$\overline{W}$ pin allows a write to the R6551.

$\overline{IRQ}$ (Interrupt Request)

The $\overline{IRQ}$ pin is an interrupt output from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common $\overline{IRQ}$ microprocessor input. Normally a high level, $\overline{IRQ}$ goes low when an interrupt occurs.

D0-D7 (Data Bus)

The D0-D7 pins are the eight data lines used to transfer data between the processor and the R6551. These lines are bi-directional and are normally high-impedance, except during Read cycles when the R6551 is selected.

CS0, $\overline{CS1}$ (Chip Selects)

The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The R6551 is selected when CS0 is high and $\overline{CS1}$ is low.

RS0, RS1 (Register Selects)

The two register select lines are normally connected to the processor address lines to allow the processor to select the various R6551 internal registers. The following table indicates the internal register select coding:

RS1	RS0	Write	Read
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

Note that only the Command and Control registers are read/write. The Programmed Reset operation does not cause any data transfer, but is used to clear Bits 0 through 4 in the Command Register and Bit 2 in the Status Register. The Programmed Reset is slightly different from the Hardware Reset ($\overline{RES}$); these differences are described in the individual register definitions.

ACIA/Modem Interface Signal Description

XTLI, XTLO (Crystal Pins)

These pins are normally directly connected to the external crystal (1.8432 MHz) used to derive the various baud rates. Alternatively, an externally generated clock may be used to drive the XTLI pin, in which case the XTLO pin must float. XTLI is the input pin for the transmit clock.

TxD (Transmit Data)

The TxD output line is used to transfer serial NRZ (non-return-to-zero) data to the modem. The LSB (least significant bit) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected, or under control of an external clock (as selected by the Control Register).

RxD (Receive Data)

The RxD input line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or the rate of an externally generated receiver clock (as selected by the Control Register).

RxC (Receive Clock)

The RxC is a bi-directional pin which serves as either the receiver 16x clock input or the receiver 16x clock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

$\overline{RTS}$ (Request to Send)

The $\overline{RTS}$ output pin is used to control the modem from the processor. The state of the $\overline{RTS}$ pin is determined by the contents of the Command Register.

$\overline{CTS}$ (Clear to Send)

The $\overline{CTS}$ input pin is used to control the transmitter operation. The enable state is with $\overline{CTS}$ low. The transmitter is automatically disabled if $\overline{CTS}$ is high.

$\overline{DTR}$ (Data Terminal Ready)

This output pin is used to indicate the status of the R6551 to the modem. A low on $\overline{DTR}$ indicates the R6551 is enabled and a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

$\overline{DSR}$ (Data Set Ready)

The $\overline{DSR}$ input pin is used to indicate to the R6551 the status of the modem. A low indicates the "ready" state and a high, "not-ready". $\overline{DSR}$ is a high-impedance input, and must be connected. If unused, it should be driven high or low, but not switched.

$\overline{DCD}$ (Data Carrier Detect)

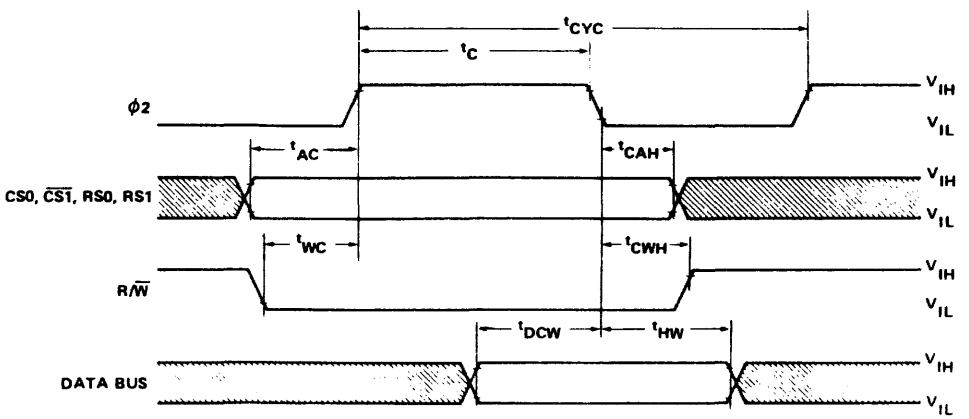
The $\overline{DCD}$ input pin is used to indicate to the R6551 the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not. Like $\overline{DSR}$, $\overline{DCD}$ is a high-impedance input, and must be connected.

READ/WRITE CYCLE CHARACTERISTICS

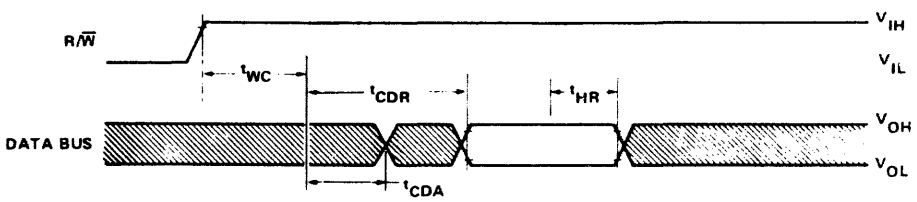
(V_{CC} = 5.0V ±5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Cycle Time	t_{CYC}	1.0	40	0.5	40	μs
Ø2 Pulse Width	t_C	400	–	200	–	ns
Address Set-Up Time	t_{AC}	120	–	70	–	ns
Address Hold Time	t_{CAH}	0	–	0	–	ns
R/$\overline{W}$ Set-Up Time	t_{WC}	120	–	70	–	ns
R/$\overline{W}$ Hold Time	t_{CWH}	0	–	0	–	ns
Data Bus Set-Up Time	t_{DCW}	150	–	60	–	ns
Data Bus Hold Time	t_{HW}	20	–	20	–	ns
Read Access Time (Valid Data)	t_{CDR}	–	200	–	150	ns
Read Hold Time	t_{HR}	20	–	20	–	ns
Bus Active Time (Invalid Data)	t_{CDA}	40	–	40	–	ns

(t_r and t_f = 10 to 30 ns)



Write Timing Characteristics



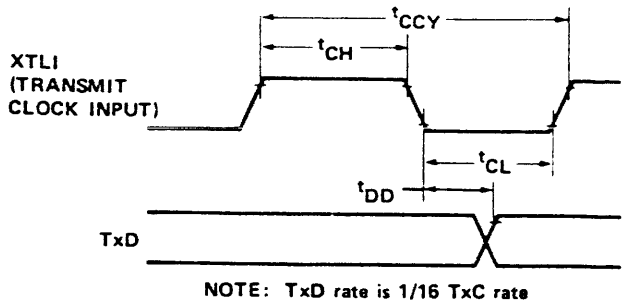
Read Timing Characteristics

TRANSMIT/RECEIVE CHARACTERISTICS

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Transmit/Receive Clock Rate	t_{CCY}	400*	–	400*	–	ns
Transmit/Receive Clock High Time	t_{CH}	175	–	175	–	ns
Transmit/Receive Clock Low Time	t_{CL}	175	–	175	–	ns
XTLI to TxD Propagation Delay	t_{DD}	–	500	–	500	ns
$\overline{RTS}$ Propagation Delay	t_{DLY}	–	500	–	500	ns
$\overline{IRQ}$ Propagation Delay (Clear)	t_{IRQ}	–	500	–	500	ns

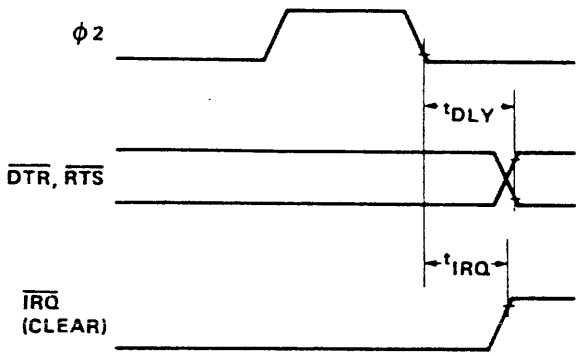
(t_r, t_f = 10 to 30 ns)

*The baud rate with external clocking is: Baud Rate = $\frac{1}{16 \times T_{CCY}}$

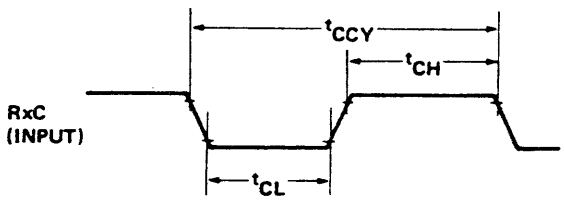


NOTE: TxD rate is 1/16 TxC rate

Transmit Timing with External Clock



Interrupt and Output Timing

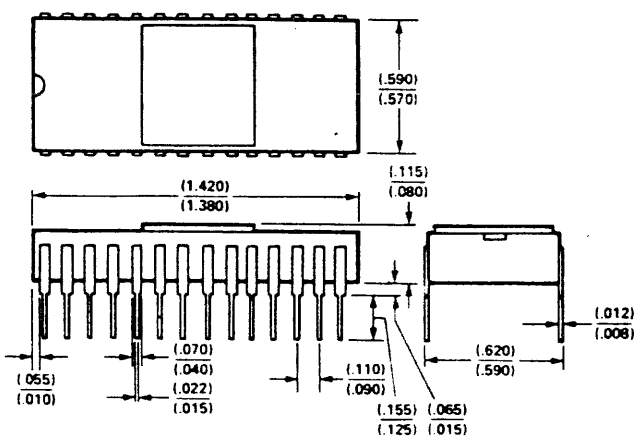


NOTE: RxD rate is 1/16 RxC rate

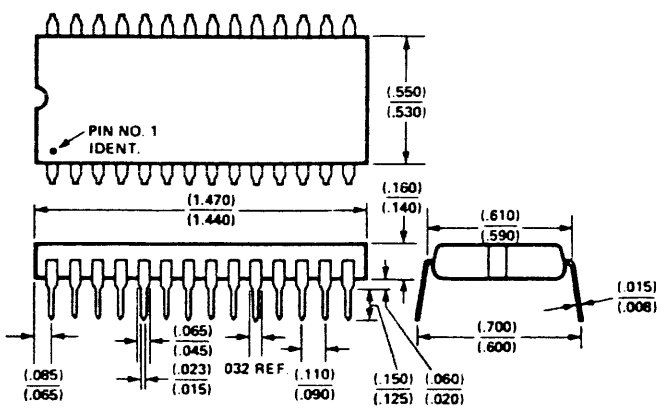
Receive External Clock Timing

PACKAGE OUTLINES

28 LEAD CERAMIC



28 LEAD PLASTIC



PRELIMINARY

8048H/8048H-1/8035HL/8035HL-1
HMOS SINGLE COMPONENT 8-BIT MICROCOMPUTER

- **8048H/8048H-1 Mask Programmable ROM**
- **8035HL/8035HL-1 CPU Only with Power Down Mode**

- **8-BIT CPU, ROM, RAM, I/O in Single Package**
- **High Performance HMOS**
- **Reduced Power Consumption**
- **1.4 usec and 1.9 usec Cycle Versions All Instructions 1 or 2 Cycles.**
- **Over 90 Instructions: 70% Single Byte**
- **1K x 8 ROM**
  64 x 8 RAM
  27 I/O Lines
- **Interval Timer/Event Counter**
- **Easily Expandable Memory and I/O**
- **Compatible with 8080/8085 Series Peripherals**
- **Two Single Level Interrupts**

The Intel® 8048H/8048H-1/8035HL/8035HL-1 are totally self-sufficient, 8-bit parallel computers fabricated on single silicon chips using Intel's advanced N-channel silicon gate HMOS process.

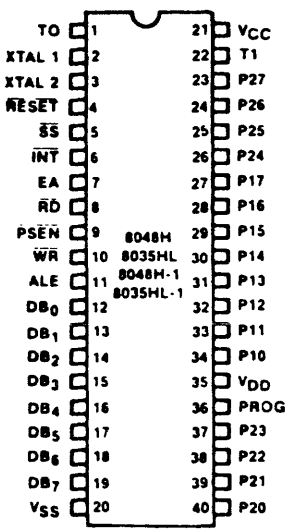
The 8048H contains a 1K X 8 program memory, a 64 X 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on-board oscillator and clock circuits. For systems that require extra capability the 8048H can be expanded using standard memories and MCS-80™/MCS-85™ peripherals. The 8035HL is the equivalent of the 8048H without program memory and can be used with external ROM AND RAM.

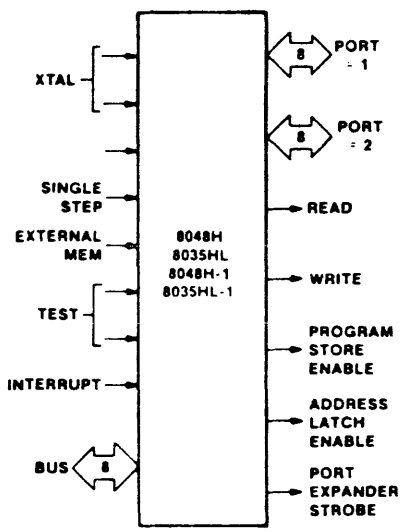
To reduce development problems to a minimum and provide maximum flexibility, a logically and functionally pin compatible version of the 8048H with UV-erasable user-programmable EPROM program memory is available. The 8748 will emulate the 8048H up to 6 MHz clock frequency with minor differences.

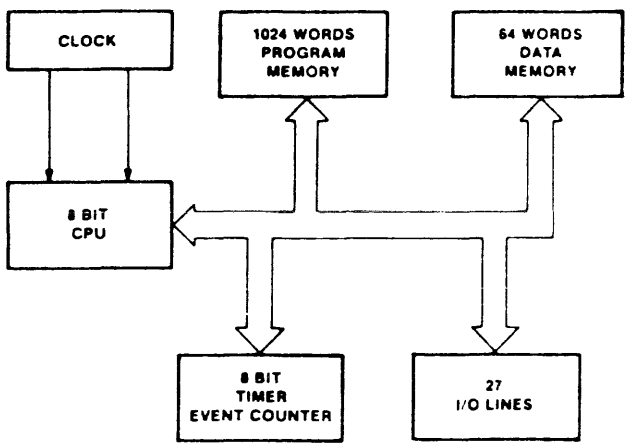
The 8048H is fully compatible with the 8048 when operated at 6 MHz.

These microcomputers are designed to be efficient controllers as well as arithmetic processors. They have extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single bit instructions and no instructions over 2 bytes in length.

PIN CONFIGURATION **LOGIC SYMBOL** **BLOCK DIAGRAM**







PIN DESCRIPTION

Designation	Pin #	Function
V_{SS}	20	Circuit GND potential
V_{DD}	26	Low power standby pin
V_{CC}	40	Main power supply; +5V during operation.
PROG	25	Output strobe for 8243 I/O expander.
P10-P17 Port 1	27-34	8-bit quasi-bidirectional port.
P20-27 Port 2	21-24	8-bit quasi-bidirectional port.
	35-38	P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243.
DB0-DB7 BUS	12-19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched.
		Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.
TO	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction.
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low)
$\overline{RD}$	8	Output strobe activated during a BUS read. Can be used to enable data onto the bus from an external device.
		Used as a read strobe to external data memory. (Active low)
$\overline{RESET}$	4	Input which is used to initialize the processor. (Active low) (Non TTL V_{IH})
$\overline{WR}$	10	Output strobe during a bus write. (Active low)
		Used as write strobe to external data memory.
ALE	11	Address latch enable. This signal occurs once during each cycle and is useful as a clock output.
		The negative edge of ALE strobes address into external data and program memory.
$\overline{PSEN}$	9	Program store enable. This output occurs only during a fetch to external program memory. (Active low)
$\overline{SS}$	5	Single step input can be used in conjuhction with ALE to "single step" the processor through each instruction. (Active low)
EA	7	External access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification. (Active high)
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Non TTL V_{IH})
XTAL2	3	Other side of crystal input.

INSTRUCTION SET

Accumulator

Mnemonic	Description	Bytes	Cycles
ADD A, R	Add register to A	1	1
ADD A, @R	Add data memory to A	1	1
ADD A, # data	Add immediate to A	2	2
ADDC A, R	Add register with carry	1	1
ADDC A, @R	Add data memory with carry	1	1
ADDC A, # data	Add immediate with carry	2	2
ANL A, R	And register to A	1	1
ANL A, @R	And data memory to A	1	1
ANL A, # data	And immediate to A	2	2
ORL A, R	Or register to A	1	1
ORL A @R	Or data memory to A	1	1
ORL A, # data	Or immediate to A	2	2
XRL A, R	Exclusive or register to A	1	1
XRL A, @R	Exclusive or data memory to A	1	1
XRL A, # data	Exclusive or immediate to A	2	2
INC A	Increment A	1	1
DEC A	Decrement A	1	1
CLR A	Clear A	1	1
CPL A	Complement A	1	1
DA A	Decimal adjust A	1	1
SWAP A	Swap nibbles of A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1

Input/Output

Mnemonic	Description	Bytes	Cycles
IN A, P	Input port to A	1	2
OUTL P, A	Output A to port	1	2
ANL P, # data	And immediate to port	2	2
ORL P, # data	Or immediate to port	2	2
INS A, BUS	Input BUS to A	1	2
OUTL BUS, A	Output A to BUS	1	2
ANL BUS, # data	And immediate to BUS	2	2
ORL BUS, # data	Or immediate to BUS	2	2
MOVD A,P	Input expander port to A	1	2
MOVD P, A	Output A to expander port	1	2
ANLD P, A	And A to expander port	1	2
ORLD P, A	Or A to expander port	1	2

Registers

Mnemonic	Description	Bytes	Cycles
INC R	Increment register	1	1
INC @R	Increment data memory	1	1
DEC R	Decrement register	1	1

Branch

Mnemonic	Description	Bytes	Cycles
JMP addr	Jump unconditional	2	2
JMPP @A	Jump indirect	1	2
DJNZ R, addr	Decrement register and skip	2	2
JC addr	Jump on carry = 1	2	2
JNC addr	Jump on carry = 0	2	2
JZ addr	Jump on A zero	2	2
JNZ addr	Jump on A not zero	2	2
JTO addr	Jump on TO = 1	2	2
JNTO addr	Jump on TO = 0	2	2
JT1 addr	Jump on T1 = 1	2	2
JNT1 addr	Jump on T1 = 0	2	2
JF0 addr	Jump on F0 = 1	2	2
JF1 addr	Jump on F1 = 1	2	2
JTF addr	Jump on timer flag	2	2
JN1 addr	Jump on INT = 0	2	2
JBb addr	Jump on accumulator bit	2	2

Subroutine

Mnemonic	Description	Bytes	Cycles
CALL addr	Jump to subroutine	2	2
RETR	Return	1	2
RETR	Return and restore status	1	2

Flags

Mnemonic	Description	Bytes	Cycles
CLR C	Clear carry	1	1
CPL C	Complement carry	1	1
CLR F0	CLear flag 0	1	1
CPL F0	Complement flag 0	1	1
CLR F1	Clear flag 1	1	1
CPL F1	Complement flag 1	1	1

Data Moves

Mnemonic	Description	Bytes	Cycles
MOV A, R	Move register to A	1	1
MOV A, @R	Move data memory to A	1	1
MOV A, # data	Move immediate to A	2	2
MOV R, A	Move A to register	1	1
MOV @R, A	Move A to data memory	1	1
MOV R, # data	Move immediate to register	2	2
MOV @R, #data	Move immediate to data memory	2	2
MOV A, PSW	Move PSW to A	1	1
MOV PSW, A	Move A to PSW	1	1
XCH A, R	Exchange A and register	1	1
XCH A, @R	Exchange A and data memory	1	1
XCHD A, @R	Exchange nibble of A and register	1	
MOVX A, @R	Move external data memory to A	1	2
MOVX @R, A	Move A to external data memory	1	2
MOVP A, @A	Move to A from current page	1	2
MOVP3 A, @	Move to A from page 3	1	2

Timer/Counter

Mnemonic	Description	Bytes	Cycles
MOV A, T	Read timer/counter	1	1
MOV T, A	Load timer/counter	1	1
STRT T	Start timer	1	1
STRT CNT	Start counter	1	1
STOP TCNT	Stop timer/counter	1	1
EN TCNTI	Enable timer/counter interrupt	1	1
DIS TCNTI	Disable timer/counter interrupt	1	1

Control

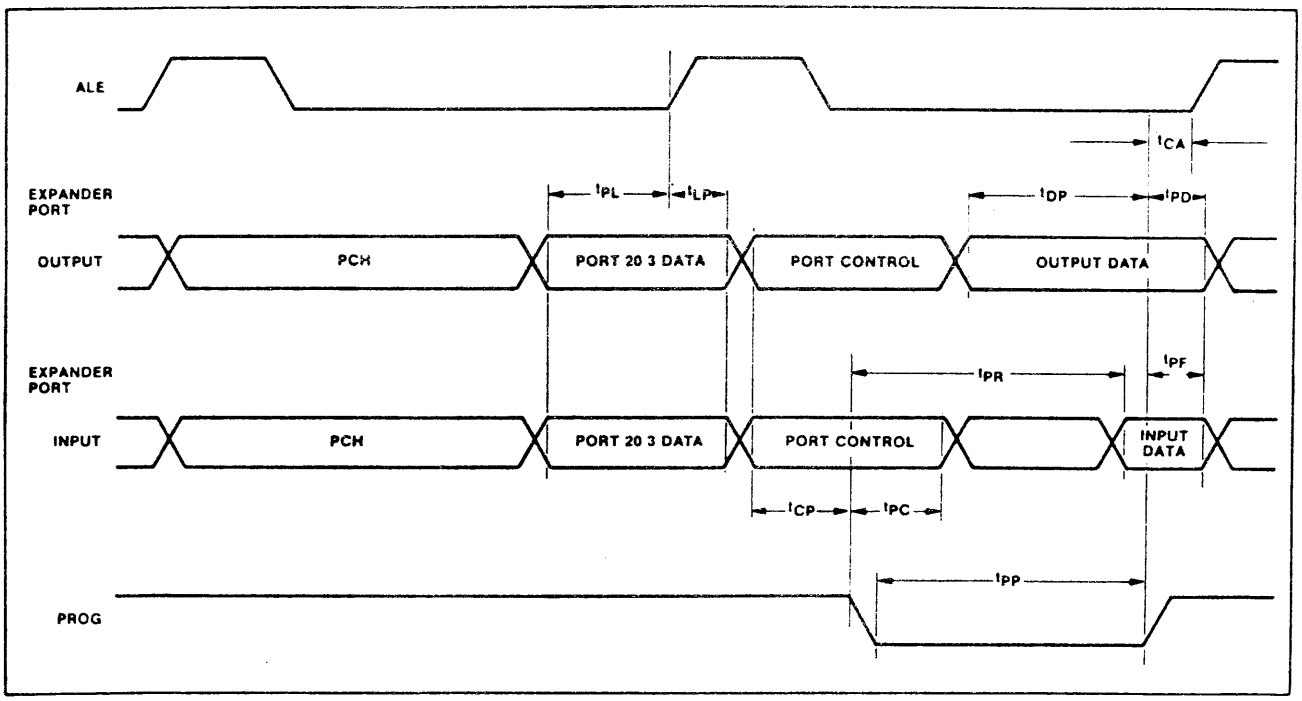
Mnemonic	Description	Bytes	Cycles
EN I	Enable external interrupt	1	1
DIS I	Disable external interrupt	1	1
SEL RB0	Select register bank 0	1	1
SEL RB1	Select register bank 1	1	1
SEL MB0	Select memory bank 0	1	1
SEL MB1	Select memory bank 1	1	1
ENT 0 CLK	Enable clock output on T0	1	1

Mnemonic	Description	Bytes	Cycles
NOP	No operation	1	1

A.C. CHARACTERISTICS (PORT 2 TIMING) TA = 0°C to 70°C, VCC = 5V ± 10%, VSS = 0V

Symbol	Parameter	8048H 8035HL				8048H-1 8035HL-1		Unit
		6 MHz		8 MHz		11 MHz		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CP}	Port control Setup Before Falling Edge of PROG.	110		105				ns
t_{PC}	Port Control Hold After Falling Edge of PROG.	100		90				ns
t_{PR}	PROG to Time P2 Input Must Be Valid		810		700		650	ns
t_{PF}	Input Data Hold Time	0	150	0	150	0	150	ns
t_{DP}	Output Data Setup Time	250		210		200		ns
t_{PD}	Output Data Hold Time	65		35		20		ns
t_{PP}	PROG Pulse Width	1200		970		700		ns
t_{PL}	Port 2 I/O Data Setup	350		300		250		ns
t_{LP}	Port 2 I/O Data Hold	150		65		20		ns

PORT 2 TIMING



BUS TIMING AS A FUNCTION OF TCY *

SYMBOL	FUNCTION OF TCY		
T_{LL}	7/30	T_{CY}	MIN
T_{AL}	1/10	T_{CY}	MIN
T_{LA}	1/15	T_{CY}	MIN
T_{CC} (1)	1/2	T_{CY}	MIN
T_{CC} (2)	2/5	T_{CY}	MIN
T_{DW}	2/15	T_{CY}	MIN
T_{WD}	1/15	T_{CY}	MIN
T_{DR}	0		MIN

T_{CC} (1) : $\overline{RD}/\overline{WR}$
T_{CC} (2) : $\overline{PSEN}$

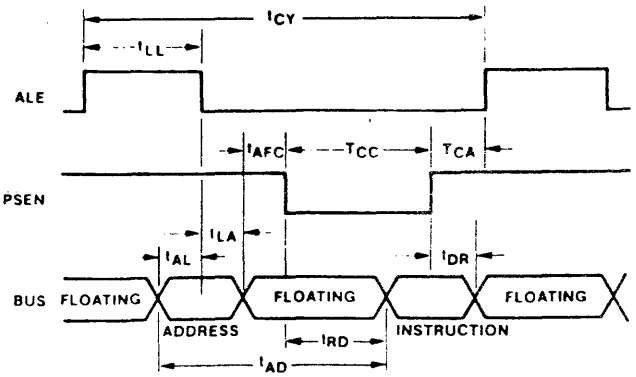
SYMBOL	FUNCTION OF TCY		
T_{RD} (1)	11/30	T_{CY}	MAX
T_{RD} (2)	3/10	T_{CY}	MAX
T_{AW}	3/10	T_{CY}	MIN
T_{AD} (1)	1/2	T_{CY}	MAX
T_{AD} (2)	1/3	T_{CY}	MAX
T_{AFC}	1/30	T_{CY}	MIN
T_{CA}	1/15	T_{CY}	MIN

T_{RD} (1) : $\overline{RD}$
T_{RD} (2) : $\overline{PSEN}$

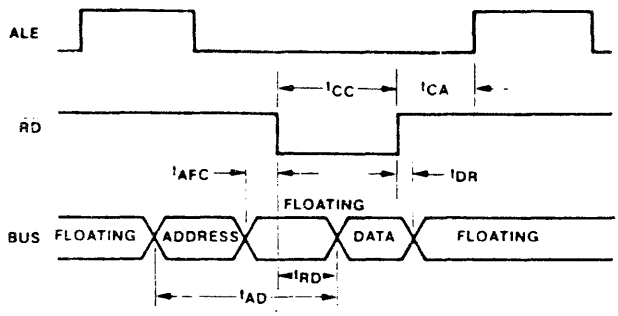
T_{AD} (1) : $\overline{RD}$
T_{AD} (2) : $\overline{PSEN}$

* APPROXIMATE VALUES NOT INCLUDING GATE DELAYS.

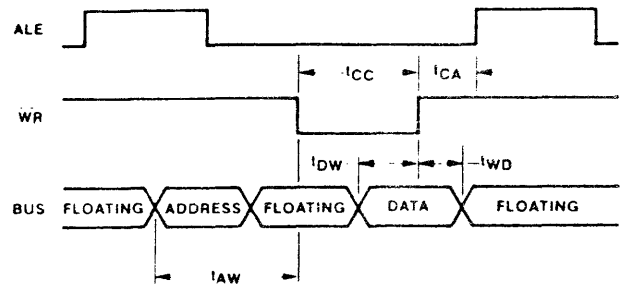
WAVEFORMS



Instruction Fetch From External Program Memory



Read From External Data Memory



Write to External Data Memory

Input and Output for A.C.Tests

A.C. CHARACTERISTICS TA = 0°C to 70°C VCC = VDD = 5V ± 10%, VSS = 0V

Symbol	Parameter	8048H 8035HL				8048H-1 8035HL-1		Unit	Conditions
		6 MHz		8 MHz		11 MHz			
		Min.	Max.	Min.	Max.	Min.	Max.		(Note 1)
t_{LL}	ALE Pulse Width	400		270		150		ns	
t_{AL}	Address Setup to ALE	75		75		70		ns	
t_{LA}	Address Hold from ALE	65		65		50		ns	
t_{CC}	Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)	700		490		300		ns	
t_{DW}	Data Setup before $\overline{WR}$	370		370		280		ns	
t_{WD}	Data Hold after $\overline{WR}$	80		80		40		ns	CL = 20pF (NOTE 2)
t_{CY}	Cycle Time	2.5		1.875		1.36		μs	
t_{DR}	Data Hold	0	200	0	150	0	100	ns	
t_{RD}	$\overline{PSEN}$, $\overline{RD}$ to Data In		500		340		200	ns	
t_{AW}	Address Setup to $\overline{WR}$	230		210		200		ns	
t_{AD}	Address Setup to Data In		950		650		400	ns	
t_{AFC}	Address Float to $\overline{RD}$, $\overline{PSEN}$	0		0		-1		ns	
t_{CA}	Control Pulse to ALE	10		10		0		ns	

NOTE 1: Control outputs CL = 80 pF
BUS outputs CL = 150 pF

NOTE 2: BUS High Impedance Load: 20 pF