Section 1

INTRODUCTION AND INSTALLATION

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INTRODUCTION

This document describes the TEK6100 Series family of computing systems. This first section provides an introduction along with installation procedures (to be provided). Each following section discusses individual major subassemblies, for example Section 2 discusses the computer board and Section 3 discusses the expansion memory board.

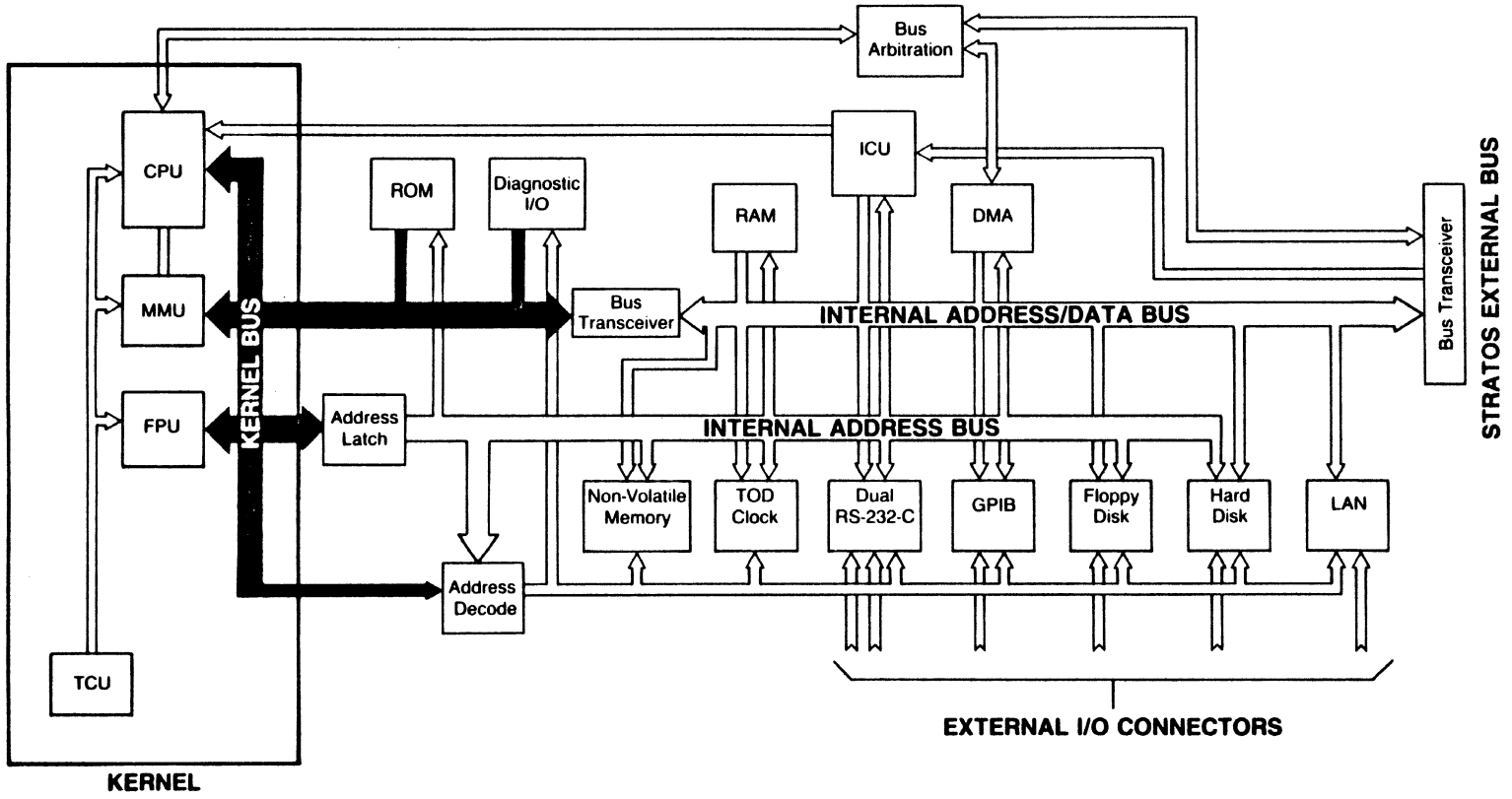
INSTALLATION

This information will be provided at a later date.

Section 2

COMPUTER BOARD

TABLES



Computer Board Block Diagram.

Section 2

COMPUTER BOARD

INTRODUCTION

This section describes the use and operation of the TEK6100 Series computer board. This document does not discuss software interface topics relevent to the computer board. Refer to the TEK6100 Series OEM Manual for this information.The contents of this section are organized as follows:

- Computer Board Overview
- Board Configuration
- Functional Block Description

COMPUTER BOARD OVERVIEW

The TEK6100 Series computer board, is a 16032-based processor that provides the computer resources and base I/O interfaces for the TEK6100 Series family of workstations. The board is a large circuit board located at the top of the system cabinet and contains up to 1 megabyte of main memory, with an additional 2 megabytes (maximum) available on an expansion board.

BOARD CONFIGURATION

The board has a number of jumpers and links that must be configured at the factory if the board is to be installed properly. Jumpers are zero ohm resistors that are machine insertable. Links are small shorting connectors that are installed on .025-inch diameter pins.

ON-BOARD RAM CONFIGURATION JUMPERS

There are six jumpers that select the density of the RAM memory chip used on the board. These jumpers are configured for the applicable memory chip as indicated in the following table:

Table 2-1

RAM CONFIGURATION JUMPERS

	W2141	W2143	W2130	W2131	W2140	W2142
64-kbit chip	remove	install	remove	install	remove	install
256-kbit chip	install	remove	install	remove	install	remove

EXPANSION RAM JUMPERS

A jumper pair is used to select whether or not an expansion memory board is used in the system. If expansion memory is used, jumper W0151 is installed and jumper is removed. If expansion is not used, jumper W0151 is removed and jumper W0152 is installed.

ROM CONFIGURATION LINKS

There are two links that establish the density of the ROM chips used, either 64k/128k bit or 256-kbit. If the system uses 64 or 128-kbit ROM parts, install links between pins 2 and 3 only of jumpers J5290 and J5291. If the system uses 256-kparts, install links between pins 1 and 2 only of jumpers J5290 and J5291.

KERNEL CONFIGURATION.

There are four links that are used to establish whether the MMU is used in the system and one link that establishes if the FPU is in the system. If the MMU is resident, no links are installed in jumpers J2040-J2042, and J0243. If the MMU is not resident, install a link between pins 1 and 2 of jumpers J2040-J2042, and J0243.

If the FPU is resident in the system, no link is installed in jumper J0250. If the FPU is resident, install a link between pins 1 and 2 of jumper J0250.

LAN INTERFACE JUMPERS

Three jumpers select which serial interface chip is used for the LAN interface. If the Intel 82501 Serial Interface chip is used, jumpers W8050 and W8051 are installed, and jumper W8052 is removed. If the SEEQ 8002 Serial Interface chip is used, jumpers W8350 and W8351 are removed and jumper W8352 is installed.

SPECIAL REGISTERS

Refer to the OEM Manual for topics such as software interface, memory maps, system and I/O control and status registers, etc.

FUNCTIONAL BLOCK DESCRIPTION

The computer board is divided into several major functional circuit areas or blocks, with each block performing a general function. This section identifies and discusses the operation of each functional block. The bus structures that tie the major functional blocks together are discussed first. The number immediately following the various section titles identifies the schematic page on which that fucntional block of circuitry can be found.

Figure 1-1 is a block diagram showing each of the blocks discussed.

SYSTEM BUS STRUCTURES

There are four major buffered bus structures that support data transfer between each functional block and throughout the computer board:

Kernel Bus

This bus supports data transfer within the kernel and is buffered from the remainder of the system. The kernel is further defined later in this section.

Internal Address Bus

The Internal Address Bus (IA Bus) is the latched address portion of the multiplexed Kernel Bus (see page 9 of te schematic diagrams). This bus provides 24-bit addressing for Kernel ROM and main memory as well as the system I/O control decoders. Latching is performed by three 74F373 octal latches.

Internal Address/Data Bus

The Internal Address/Data Bus (IA/D Bus) provides the address and data interface between the kernel and the various system I/O devices on the compute engine. Interface between the External Bus and the kernel is also provided by the IA/D Bus. The structure of the I/AD Bus is basically the same as the Kernel Bus: a 24-bit multiplexed address/data bus with the 16-bit data bus sharing the lower 16 lines of the 24-bit address bus (see page 9 of the schematic diagrams). The IA/D Bus is buffered from the Kernel Bus by three 74ALS245 octal bus transceivers.

External Bus

The External Bus provides the interface between the compute engine and system options. Bus connectors located on the options backplane provide electrical interface. The External Bus primarily an extension of the IA/D Bus. Bidirectional interface for the address/data bus itself is provided by six 74AS373 octal D-type latches and associated bus interface control logic. Interface for the bus-control and protocol signals is provided by two 74F244 octal buffer/line drivers (see page 11 of the schematic diagrams.

KERNEL (1)

The kernel controls, either directly or indirectly, the major functions for the entire compute engine. As stated above, the kernel is comprised of five major components: the Central Processing Unit (CPU), the Memory Management Unit (MMU), the Floating Point Unit (FPU), and the Timing Control Unit (TCU), and kernel ROM. The FPU is an optional device. Within the kernel, these devices are supported by additional logic. System addressing and memory management/protection is a task that is shared between the CPU and the MMU, while floating point operations are supported by the FPU.

Data transfer within the kernel and with the remainder of the system is via the Kernel Bus, which consists of the multiplexed address and data bus. Another bus apart from the Kernel Bus is the Kernel Timing and Control Bus, which provides the necessary timing, status, and control signals between the primary components.

Kernel Bus

The Kernel Bus provides the means of data transfer within the kernel and between the kernel and the rest of the compute engine. All signals on the Kernel Bus are high-active. The Kernel Bus may be sampled at the CPU pinout. Refer to "Central Processing Unit" for CPU pin assignments or page 1 of the schematic diagrams.

Address Bits 16-23. These lines are high-active outputs and are the most significant eight bits of the Kernel Bus address bus. During clock period T1, the bus contains the virtual address output by the CPU. During clock period TMMU, this bus contains the translated, physical address output by the MMU.

Address/Data Bits 00-15. These are the multiplexed, bi-directional address and data lines for the Kernel Bus. All lines are high-active. Bit 00 is the least-significant bit. During clock period TMMU, this bus contains the virtual address output by the CPU. During TMMU this bus contains the physical address output by the MMU. During clock periods T2 through T4, this bus contains data output by the CPU, MMU, memory, etc.

Kernel Timing and Control Bus

This bus is local to the kernel and is used to provide control, timing, and coordination of kernel-level operations, including memory management, and the execution of floating point operations. These signals may be sampled at the CPU pinout, which is provided in the following section. Bus signals are defined below:

Phase 1, Phase 2. These pins provide two non-overlapping phases of a single frequency, 10-megahertz clock, although this clock may be slowed to 5 megahertz for big build. These inputs are taken from the Timing Control Unit. The execution of microinstructions within the CPU or steps in a data transfer over the Kernel Bus is synchronized and controlled with respect to the number of Timing states or T states required to complete the execution. A T state is defined as the wavelength of the Phase 1 clock input. T states are numbered progressively from the beginning of a bus cycle to it's completion.

Ready-1. This is a high-active signal that is asserted by the Timing Control Unit at the end of the bus cycle to signal the CPU that the operation is complete. The CPU then terminates the cycle. An external device that requires additional time to finish the bus cycle can request an extension to the TCU. The TCU will then insert a given number of wait states, allowing the device to finish the cycle before asserting Ready-1.

Hold Request-0. This low-active input is asserted by another device (MMU) that is requesting the use of the Kernel Bus. If the CPU complies, the CPU asserts Hold Acknowledge-0 to the MMU, thereby granting the bus to the MMU. Hold Request-0 is asserted for the entire time the MMU has the bus and Hold Acknowledge-0 remains asserted by the CPU until the bus is regained by the CPU. This handshake sequence allows the MMU to acquire the bus and place the translated address on the bus. See the following definition.

Hold Request Acknowledge. This low-active output is asserted by the CPU to grant the bus to another device on the Kernel Bus (MMU). This signal is asserted after the MMU has asserted Hold Request-0. Both signals remain asserted for the duration of the bus cycle, after which the MMU deasserts Hold Request-0 and the CPU regains control of the bus by deasserting Hold Request Acknowledge-0. See the previous definition.

High Byte Enable-0. This low-active output is asserted by the by the CPU to enable the high byte of the addressed location to be placed on the bus. Memory is organized as two eight-bit banks, with each bank receiving the 24-bit address in parallel. The low bank (bits D00-D07) responds to even byte addresses, that is when the least-significant address bit (A00) is low. The high memory bank (bits D08-D15) is enabled when High Byte Enable-0 is asserted. This feature permits the addressing of individual bytes even though the data bus is 16-bits wide.

Data Strobe-0/Float-0. This is a dual-function pin, the function of which is determined by whether or not the MMU is performing address translation or the CPU is addressing the Kernel Bus directly. For bus cycles that are not address-translated, this pin functions as a Data Strobe-0 output from the CPU. Data Strobe-0 is asserted after the multiplexed address/data bus has switched from address presentation to accepting or presenting data. The assertion of Data Strobe-0 validates the data on bus lines AD00-AD15. Since address translation is always performed for every bus cycle initiated by the CPU, Data Strobe-0 is never asserted.

For bus cycles that are address-translated, this pin functions as the Float-0 input to the CPU. The assertion of Float-0 by the MMU causes the CPU to wait longer than the normally allotted TMMU T state for the MMU to perform address translation. This function is employed by the MMU in order for it to update its internal translation cache from page tables in memory, or to update status bits contained within the tables. Timing states are not numbered during a float condition, and the entire bus cycle is placed on a temporary hold. After Float-0 is deasserted, the bus cycle continues from where it was suspended. The Kernel has been implemented such that address translation is always performed by the MMU, although the translated physical address may be the same as the virtual address.

Reset-0/Abort-0. This is a low-active, dual-function input. If this signal is asserted during TMMU or TFloat (an address-translated cycle) and held low for one clock cycle, this pin causes an Abort of the bus cycle and the instruction that executed it. The rest of the system remains unaware of the aborted cycle, since the MMU Physical Address Valid-0 address strobe, which triggers the physical cycle, was not yet asserted.

If this pin is held low for at least 64 clock cycles a Reset is initiated.

Address Translation-0/Slave Processor Control-0. AT-0/SPC-0 is a bidirectional, dual function signal. The AT-0 portion of this signal enables address translation by the MMU. The SPC-0 function enables slave processor communications (ie, with the FPU).

The CPU is able to operate with or without address translation. The mode of operation is determined by the presence of the MMU. The MMU asserts Address Translation-0 during reset and at power up. The CPU samples AT-0 on the rising edge of the reset pulse. If the AT-0 is high (no MMU present), bus cycles are performed without address translation. If during reset AT-0 is low, the bus cycle includes an extra clock cycle (TMMU). At this point, the DS-0/FLT-0 signal becomes a Float-0 command input to the CPU (see previous definition of DS-0/FLT-0).

AT-0/SPC-0 is also used as the data strobe in slave processor data transfers. During slave processor data transfers, data is transferred on bus lines AD00- AD15, but no bus control lines other than DDIN-0 (controlled by the CPU) are asserted. For example, ADS-0, HBE-0, ect, are not used. During a slave processor bus cycle, the slave processor samples the CPU status lines ST0 and ST1 on the leading edge of SPC-0. During a data read, SPC-0 remains asserted until data has been read from the slave processor. During a data write, the slave processor latches the status bits on the leading edge of SPC-0 and latches data on the trailing edge of SPC-0. In all slave processor bus cycles, SPC-0 is asserted by the CPU. Refer to Slave Processor Bus Cycles.

User-1/Supervisor-0. This output is taken from the U bit in the Processor Status Register, which is an internal status register. Asserted high, this signal indicates that the CPU is running in the user mode. Asserted low indicates the supervisor. This signal is sampled by the MMU for mapping and protection purposes.

Address Strobe-0. Address Strobe-0 (ADS-0) is asserted by the CPU when it places an address on the Kernel address bus. Without the MMU, this signal would be used to validate and latch the address. However, with address translation by the MMU, this signal is sent to the MMU only, where it latches the virtual address. The MMU outputs the Physical Address Valid-0 strobe to validate the translated, physical address.

Physical Address Valid-0. This MMU output is generated during TMMU and is used as the address strobe to latch the physical address into external memory devices. This signal is also used during a float condition to access the external page tables.

Data Direction In-0. Data Direction In-0 (DDIN-0) is output by the CPU or the MMU to specify a read operation (low) or a write operation (high). During normal bus cycle with address translation, this signal is output by the CPU to indicate data direction. During a float condition, the CPU tristates DDIN-0, allowing the MMU to assert DDIN-0 low, thus allowing the MMU to update its page tables from memory. The MMU also controls DDIN-0 when it has control of the Kernel Bus.

Program Flow Status-0. This low-active pulse is asserted by the CPU to indicate the beginning of an instruction cycle.

Status ST0-ST3. This is a four-bit bus cycle status code that provides status information. The pins are interpreted as a four-bit value, with ST0 as the least-significant bit. Only two bits, ST0 and ST1, are sampled by the FPU during slave processor bus cycles. Refer to the CPU data manual for a definition of each of the codes.

Interlocked Operation-0. This is a low-active output that is asserted during a Set Bit, Interlocked or Clear Bit, Interlocked instruction. This signal is used to reserve the bus in a multiprocessor system that shares resources, in this case, common RAM that the compute engine shares with the display engine.

Non-Maskable Interrupt-0. The Non-Maskable Interrupt-0 (NMI-0) is a low-active input to the CPU.

Central Processing Unit

The NS16032 CPU (U1280) is the heart of the kernel. This device is configured in a 48-pin, dual-in-line package. The CPU provides a 16-megabyte uniform address space. The CPU's internal architecture features 32-bit data paths, although the data path at the pin-out is 16-bits wide. Refer to page 1 of the schematic diagrams.

The CPU provides 16 registers, eight of which are dedicated control/status registers, and eight general purpose registers. The general-purpose registers are 32-bits in length and are used for general storage requirements, such as storing temporary variables and addresses. The CPU clock frequency is 10 megahertz. As stated previously, data transfer within the computer board is afforded by the Kernel Bus and other bus structures. Within the Kernel however, dedicated data transfer that is transparent to the rest of the system is accomplished via the slave processor bus cycle.

Slave Processor Bus Cycles. The slave processor bus cycle permits communication between the CPU and the slave processors (the MMU and the FPU) without executing the Kernel Bus protocol. This type of transfer utilizes the data bus portion (AD00-AD15) but none of the bus control/signals (excluding DDIN-0).

Slave processor bus cycles require only 2 clock cycles or T states (labeled T1 and T4) to finish. At the start of a data read cycle (T1), the CPU places the appropriate status code on lines ST3-ST0 and the appropriate processor identification byte on data line AD00-AD07 of the Kernel Bus. The CPU then asserts SPC-0. Both the FPU and the MMU decode the ID byte and latch the status from the CPU on the leading edge of SPC-0. The appropriate slave processor responds by placing data on lines AD00-AD15 at T4. The CPU reads the data and terminates the cycle by deasserting SPC-0.

During a data write (at T1), the CPU places the appropriate status code and processor ID on data lines AD00-AD07, as before. The CPU then asserts SPC-0 and the appropriate processor responds by latching the status and ID byte. The CPU then removes the ID byte from the Kernel Bus and places data on the bus. The data is latched by the slave processor on the trailing edge of SPC-0 as it is deasserted (T4). At the end of a data write, the slave processor signals a successful transfer by pulsing SPC-0 low.

Since ADS-0 is not asserted by the CPU, none of the other associated bus protocol signals are asserted. The CPU, however asserts DDIN-0 as appropriate. In both of the above cases, the status code is set up by the CPU during the previous clock cycle.

Memory Management Unit

The NS16082 Memory Management Unit (MMU) (U1300) provides support for demand-paged virtual-memory management. The chip, in concert with the CPU, permits rapid address translation and protection on individual 512-byte memory pages. The chip uses a associative cache that stores the 32 most frequently used memory page table entries. The MMU is packaged in a 48-pin, dual-in-line configuration. Refer to page 1 of the schematic diagrams.

Memory Management. For addressing purposes, memory is divided into several 512-byte pages. Associated with each page of memory are page tables that the MMU and the operating system maintain in physical memory. The page tables contain information pertinent to each memory page, such as the page access permission codes, whether the page has been accessed, and if it has been written to. Also contained in the page tables are values that are used to arrive at the physical address. The MMU executes a translation algorithm that determines the validity of the access and provides the physical address. Of the virtual address provided by the CPU, the least-significant 9-bits are not modified. These 9 bits provide discrimination to the byte level within the 512-byte page.

By modifying the page tables as required, the operating system controls the mapping of virtual addresses to physical memory. Additionally, the operating system can control the degree of access (read or read and write) permitted to specific pages in the supervisor and user modes by generating translation error aborts if access permission codes are violated.

The most frequently referenced or accessed page tables are stored by the MMU in an internal cache memory, thus saving the MMU from having to retrieve the page table from memory for the majority of accesses. The cache contains 32 page table entries. If during a bus cycle, the given access is not a "hit", the MMU asserts the Float-0 signal to the CPU, which temporarily suspends the bus cycle while the MMU retrieves the page table from physical memory via the Kernel Bus. Once the page table entry has been retrieved, the least-used entry is removed from the cache and the newest entry is placed in the cache. The Float condition is terminated and the bus cycle continues from where it was suspended.

All bus cycles initiated by the CPU are address-translated, however in some cases the translated, physical address may equal the virtual address placed on the Kernel Bus by the CPU.

Floating Point Unit

The NS16081 Floating Point Unit (FPU) (U1260) operates as a slave processor and performs both single precision (32-bit) and double precision (64-bit) arithmetic. This device is packaged in a 24-pin configuration. Data transfer between the CPU and the FPU is not accomplished using the normal Kernel Bus protocol, but the slave communications protocol described previously. The FPU contains 9 32-bit registers, eight of which are general-purpose. The ninth register is a status register. Refer to the FPU data sheet for additional information and page 1 of the schematic diagrams.

Timing Control Unit

The NS16201 Timing Control Unit (TCU) (U0320) is a 24-pin DIP that provides the two-phase 10 megahertz clock output based on the 20 megahertz crystal frequency, as well as several signals that support Kernel Bus logic, timing and control functions. The TCU also provides for a variety of bus cycle extensions to compensate for slower devices (compute engine or peripheral devices). Refer to the TCU data sheet for additional information and page 1 of the schematic diagrams.

Kernel ROM (2)

Up to 128 kbytes of Kernel ROM are provided by four 256-kbit (32k x 8) EPROM chips (U3280, 3300, 4280, and 4300). Kernel ROM is organized as two, 64-kword banks. Lesser total capacities are 64 kbytes and 32 kbytes, depending on chip density. Addressing is provided via the Internal Address Bus, which is the latched address portion (AD00-AD15) of the Kernel Bus, while ROM data is placed directly on the Kernel Bus data bus. Refer to page 2 of the schematic diagrams. Kernel ROM is discussed further in Section Five of the TEK6100 Series OEM Manual.

NON-VOLATILE MEMORY (8)

This block consists of two 256-bit, non-volatile, sequential-access EEPROMs (U143, U144) and a Non-volatile-Memory Control Register (U108). Each memory chip is organized as 16 registers containing 16 bits each. Each register is read from serially.

MAIN MEMORY (14)

Main memory provided on the computer board consists of up to 1 megabyte of dynamic RAM using 256-kbit parts, or 256 kbytes using 64-kbit parts. The board contains a maximum of 36 RAM chips, each of which is organized in a 256 k by 1-bit or 64 k by 1-bit format. On the board, memory is organized as two rows, each containing a maximum of 18 chips. Each memory row is two-bytes wide plus one parity bit per byte. Jumpers that select the chip density and board capacity, as well as whether or not the sytem is equipped with an expansion memory board, are discussed in the a previous section of this document, titled Board Configuration.

The computer board contains logic that provides support functions for the RAM. These functions are: memory access and refresh timing, memory addressing, and parity generation and error detection.

Memory Access and Refresh Timing (13)

This logic coordinates the memory refresh cycle, which is performed every 12.5 microseconds, and normal memory accesses. The Refresh Clock operates a 80 KHz and initiates a memory refresh cycle on the rising edge of the clock pulse, at which time various status lines that indicate an impending data transfer are sampled. If the status lines are asserted, the refresh is postponed until the data transfer is completed. When refresh is in process, memory access are locked out until the refresh is completed.

This logic employs a 200-nanosecond delay line to establish memory-access and refresh-cycle timing. The data read cycle from memory requires approximately 400 nanoseconds, whereas a data write cycle from memory can be extended beyond 400 nanoseconds.

This logic supports a distributed refresh method whereby only one memory row is refreshed per refresh cycle. The next refresh cycle increments the refresh address counter by one in preparation for that cycle. The counter is incremented on the trailing edge of the Refresh Clock. After the new row address has been placed on the Memory Address Bus (MA Bus), the Row Address Strobe (RAS-0) is pulsed, refreshing the 512 memory-bit locations in that row. With 256 k-byte parts, 512 refresh cycles are required for a full memory refresh.

Memory Addressing (14)

This block samples the IA/D lines 18-23 to determine if the bus cycle is a memory access, in which case the impending refresh cycle is may be postponed until the end of the data transfer. This block also provides the multiplexing required to place the 16-bit address word (IA/D01 - IA/D16) on the 9-bit Memory Address Bus (MA0 - MA8), as well as the Row Address Strobe-0 (RAS-0) and Column Address Strobe-0 (CAS-0) synchronization required to latch the address into memory.

Parity Generation and Checking (14)

This block utilizes two parity generators/checkers and associated logic to generate and store an odd parity bit for each byte during a memory write operation, and to check the stored parity bit during a memory read. If an error is detected during a read, a Parity Error signal is generated, as well as a bit defining whether the error applies to the high or low byte. A Parity Error Register, which is continually loaded with the current memory address, is used to provide the address of the faulty memory location. A brief description of the operation of the parity generation and checking logic for the high byte is given below:

During a memory write, the high data byte from the IA/D Bus is input to the U25 parity generator/checker. At this time, the octal D-type latch U140 is disabled by status signals that are set as a function of the type of data transfer, read or write. Nand gate U139 outputs a high at pin six, and the parity generator U25 generates even parity for the data byte plus the additional high bit input at pin 4. This parity bit is equivalent to odd parity for the data byte, and the parity bit is stored with the byte in memory.

During a memory read, the octal latch U140 is enabled and the stored parity bit is inverted by nand gate U139 and input at pin four of parity generator U25. U25 generates parity for the data byte plus the inverted parity bit. If the stored bit or the data byte is in error by one bit, the parity checker generates an even-low parity bit, thus signaling a parity error.

SYSTEM CONTROL BLOCK (9)

The system control block provides the system I/O enables and control signals required to enable DMA transfers via the various I/O devices, as well as the enables for the System Control Register and the System Status Register. These enables are arranged as memory-mapped I/O locations in the kernel's external memory space. This logic consists primarily of two 74F138 3-to-8-bit decoders.

This block also contains the System Control Register (octal D-type flipflop U18) and the System Status Register (octal D-type flipflop U19), along with the enables required to drive these registers (as given above).

The system control block also provides a mechanism for low-level debugging of the board. This consists of a diagnostics switch register and a diagnostics display register. The switch register is a 8-switch DIP that corresponds to lines AD00-AD07. The setting of the switch is read by enabling 74F244 octal buffer U16 (address FFF008). Diagnostic information is displayed by a write to the same address. An 74LS273 octal D-type flipflop performs as the display register. The D outputs (AD00-AD06) correspond to segments A-G of a seven-segment display. Bit AD07 drives the decimal point.

FLOPPY DISK INTERFACE (4, 10)

The floppy disk interface is composed of two major LSI components: the WD1770 Floppy Disk Controller (U7020) and the AM9516 DMA Controller (U8290), along with supporting logic. The WD1770 is a floppy disk controller and formatter and also contains digital data separation logic and write precompensation circuitry. The WD1770 is a 28-pin DIP. There are six registers within the floppy disk controller that allow the Am9516 DMA controller to execute data transfer between the disk controller and the DMA controller. These registers contain command and status information, various head positioning information, and 8-bit data. Interface between the two controllers is via an 8-bit bidirectional data bus and various control signals.

The DMA controller (page 10 of the schematic diagrams) is equipped to handle two separate channels although only one DMA channel (channel B) is used. DMA operations are initiated by the kernel by loading DMA control parameters into a control block known as the Channel Control Table. The Channel Control Table is maintained by the kernel in main memory. The kernel then places the starting address of the Channel Control Table in the Chain Address Register (internal to the DMA controller) and issues a "Start Chain" command to the controller. The DMA controller responds by updating its various internal control registers with the control parameters located in the Channel Control Table. The Channel Control Table contains such information as what specific registers are to be updated or reloaded, the source data address, the destination data address, ect.

"Chaining", allows the several DMA transfers to be performed asynchronously. This method places the address of the next Channel Control Table in the within the previous table, so that when a given DMA operation is completed, the DMA controller reads the new address of the control table, updates internal control registers with the table, and executes the new command.

The DMA controller also performs byte/word alignment between the 8-bit disk data bus and the 16-bit IA/D Bus. As mentioned before, the System Control Block provides the address decoding required to access the floppy disk interface.

Erroneous ALE Detection Logic

Logic associated with the AM9516 DMA Controller includes erroneous ALE detection logic. This consists of the D-type flipflops U6041, U6130 and associated logic. This logic was implimented in order to detect and void or cancel the erroneous assertion of Address Latch Enable-1 by the controller. This logic differentiates between chain operations and single data transfers. Note that this interface allows only single data transfers per bus-request/bus-release cycle. This logic operates as follows:

The Normal/System-0 output from the DMA Controller is programmed to be asserted high when data is being transferred between the controller and the host. During a data transfer, ALE is asserted by the controller to the Kernal Bus as Kernal Physical Addrss Valid-0 (KPAV-0). When data is placed on the bus, Normal is asserted by the DMA Controller, which is clocked through U6041 as NOALE-0. NOALE-0 disables AND gate U3140 and Quit ALE-1 (QALE-) deasserts KPAV-0 to the Kernel Bus.

During chaining operations, System-0 is asserted by the DMA Controller, which is clocked though U60410 and U6130 as Hold Bus-0 (HLDBUS-0). In this case, Bus Request has been released and there is no data strobe. Disk Data Strobe-0 is asserted as Memory Data Strobe-1 (MDS-1) in order to complete the bus cycle. Since the DMA Controller is executing reads from memory during chaining operations, memory data is not affected.

HARD DISK INTERFACE (3)

The hard disk interface is composed primarily of the WD1010 Winchester Disk Controller (U7100), an external 4-kbyte cache, a DP8460 data separator and a Hard Disk Control Register.

The controller performs the normal functions of a hard disk drive controller/formatter, although it does not feature write precompensation and this logic (consisting of quad D-type flipflop U47, delay line U51, and data multiplexer U52) is implimented externally.

On the drive side of the controller, the data separator receives MFM encoded data from the disk drive and separates this data into synchronized data (SDATA) and a Read Clock (RCLK) signal. The disk controller decodes this serial data from RCLK into 8-bit parallel data. During a write to the disk, data is MFM-encoded by the controller.

Disk Data Cache

On the host side of the controller, the 4-kbyte cache is a serial, disk-data transfer buffer that is accessible by the disk controller or the kernel. The buffer appears to the kernel as a 2-kword (16-bits) sequential-access buffer. The buffer itself consists of two 2048 x 8-bit static RAM chips, U156 and U157. This buffer and octal bus transceiver U159 also serve as a data assembler/disassembler in that data is transferred between the kernel and the buffer in 16-bit words, whereas data transfer between the buffer and the disk controller occurs in 8-bit bytes.

Buffer addressing is performed by two dual, four-bit binary counters, U155 and U99. Only half of U99 is used. During a data write to the disk, the kernel clears the buffer by setting the Manual Clear bit in the Hard Disk Control Register (octal D-type flipflop U158). This generates the Counter Clear (CCLR) output of the Buffer Control Programmable Array Logic (PAL) chip U44, which clears the counter. As each 16-bit word is loaded into the buffer, the counter is incremented by the Counter Clock (CCLK) output of PAL U44, which develops the clock from the Data Strobe-0 input. When the kernel has loaded the buffer, the kernel writes a Manual Ready-1 signal to the controller via the PAL (input to the controller as Hard Disk Buffer Ready-0 (HDBRDY-0)). The controller then clears the buffer counter and transfers the

contents of the buffer to disk, incrementing the buffer address counter as each 16-bit word is read. Since the buffer is organized as two 2k x 8-bit chips, each byte can be read individually by the controller. This is permitted by the bus transceiver U159, which multiplexes both the high and the low bytes of the buffer onto Hard Disk Data lines 0-7 (HDD0-HDD7).

During a data read from the disk, the controller clears the buffer address counter and begins loading the buffer. This time the bus transceiver operates in reverse fashion, demultiplexing the 8-bit data from the controller into the high and low bytes prior to loading into the buffer. CCLK is generated by Buffer Chip Select-0 output from the controller, via the PAL. When the controller-to-buffer transfer to completed, the controller signal the kernel by asserting Hard Disk Interrupt-1. The kernel proceeds to read the contents of the buffer, by first resetting the buffer address counter and then incrementing the counter with each word read.

Two 74LS245 bus transceivers (U45 and U46) serve to buffer or isolate the IA/D bus from disk/cache data. As given previously, the System Control Block provides the address decoding required to enable data transfer via the hard disk interface.

Buffer Control PAL

The Buffer Control PAL (U8050) controls the operation the disk data buffer and the data buffer address counter. Inputs to the PAL are from the disk controller and the system control logic (address decode). Outputs drive the buffer chip enables, address counter, and Controller Ready-0 line.

DUAL RS-232-C INTERFACE (5)

The RS-232-C interface is a dual-channel, serial asynchronous DCE port that utilizes the AM8530 Serial Communications Controller (U6340). The output driver for each port is a DS1488 transmission line driver. The receiver for each port is DS1489 transmission line receiver. All configuration, control, status, and data registers are internal to the controller. Serial port enables are address-decoded by the System Control block. A 4 MHz clock developed by the clock generator is supplies to the controller.

GPIB INTERFACE (6)

The GPIB interface utilizes the TMS 9914 GPIB Controller and the SN75160 and SN75162 bus transceivers. This interface supports talker, listener, and controller functions. This design does not incorporate DMA support and the transfer rate is limited by the speed of the programmed data transfer. System control of the bus is provided via a GPIB Control Register (U36), which is a 74LS174 hex D-type flipflop. The System Control Block provides the address decoding required to enable GPIB I/O operations.

Communication between the controller and the kernel is performed via 13 memory-mapped registers that contain status and control information, data. These registers are contained within the controller. Three Register Select lines (RS0-RS2) address one of eight possible locations, each of which contain one read and/or one write register. Register selection within the addressed location is a function of the operation: read or write.

On the host side of the controller, data interface is 8-bits wide over lines IA/D0-IA/D7. As stated previously, there is no DMA support for this port.

The 75162 octal bus transceiver U35 drives and receives the GPIB control bus lines, while a 751600 octal bus transceiver U34 drives and receives the 8-bit port data.

The GPIB Control Register contains a GPIB Enable bit (bit IA/D0) that disables the GPIB bus transceivers and also enables the bus buffer gate U98. U98 permits the kernel to test the GPIB protocol sequence of the TMS9914 controller by writing test bits to the control register.

LOCAL AREA NETWORK INTERFACE (12)

The Local Area Network (LAN) interface consists primarily of the 82586 LAN Controller (8310) and the 82501 Serial Interface Chip (U9370). The primary function of this port is to provide an interface between system memory and the LAN link. The host initiates a transfer over the LAN by the writing the transfer parameters to a control block residing in system memory. Once the control block is configured, the host toggles the Channel Attention line to the LAN controller by writing the appropriate address to the system control decoders. This causes the LAN controller to copy the contents of the control block into internal memory and execute the command. The controller signals the completion of the transfer by asserting an interrupt to the host. The LAN controller is a bus master of the IA/D Bus and most of the DMA transfers are executed with the LAN directly accessing system memory. For this purpose, 256 kbytes of system memory are reserved for the LAN. The LAN interface is tested via the System Control Register. Refer to page 12 of the schematic diagrams.

The 82501 Serial Interface chip provides the 10 MHz transmit clock for the 82586 controller, performs the encoding/decoding of the transmitted/received frames, and provides the electrical interface for the Ethernet transceiver cable.

INTERRUPT CONTROL

The Interrupt Control Unit (ICU) and associated logic provide interrupt management for the CPU. This logic handles up to 15 prioritized interrupt sources from the various intelligent I/O devices within the system. Six interrupt lines handle computer board I/O devices, two lines handle the MMU and FPU, and seven interrupt lines are reserved for optional devices operating on the External Bus. The ICU resolves interrupt priorities and issues a byte-wide interrupt vector to the CPU. This device is configured in a 40-pin DIP configuration. Refer to page 12 of the schematic diagrams.

EXTERNAL BUS INTERFACE

This block provides the interface between the Interal Address/Data Bus and the External Bus. The block consists of primarily of a Bus Interface Control PAL (U6290), six octal D-type latches used as bus buffers, Bus Timeout Logic, and associated logic. The Bus Interface Control PAL monitors various system status and control signals and controls the direction and enable signals required to control the bus buffers.

Bus Timeout

This block also handles bus timeout control. The bus timeout counter is started by the assertion of System Address Strobe-1 (SAS-1) and is clocked by a 400 KHz clock. The counter is cleared by the normal execution of the bus protocol within the time required. The counter is also cleared by a reset. The bus-timeout period is approximately 10 microseconds. The complete bus-timeout cycle takes about 20 microseconds; 10 microseconds are alloted for the faulty DMA device to release the bus after the associated Bus Grant signal has been deasserted by the host.

DMA ARBITRATION (2)

This block performs DMA arbitration for the six available External Bus options slots, and the computer-board based LAN port and floppy disk drive interface. Each bus-request line is weighted at a particular priority level. Simultaneous External Bus bus requests are arbitrated according to the priority level assigned to each request line and a bus-grant signal is issued to the arbitrated requester. This block also generates a 4-bit code (via the 74LS140 8-to-3 line encoder U70) that is loaded into the System Status Register and indicates the most recently used DMA channel. This code is used after a bus timeout to identify the faulty DMA device.

DMA Arbitration PAL

DMA arbitration is performed by a 24-pin DMA Arbitration PAL (U1230) and associated logic. The PAL monitors the various prioritized bus-request signals from the External Bus option boards, the floppy disk DMA controller, and the LAN interface, and issues a bus grant to the highest-priority requester.

CLOCK GENERATION (7)

The clock generation logic develops most of the clock pulses required by the system. The primary clock source is a 20 MHz clock taken from a crystal oscillator. Three 74LS390 4-bit counters divide this pulse into a 10 MHz clock, a 1 MHz clock, an 80 KHz refresh clock, and a 200 Hz ICU clock. A secondary crystal oscillator operating at 16 MHz is used to develop an 8 MHz clock and a 4 MHz clock.

Reset Pulse Stretcher

Resets are generated by any device on the External Bus, the power supply, and the Interrupt Control Unit. All resets pulses are expanded by 2 milliseconds by the pulse-stretching logic shown on page 7. This logic consists binary counter U6301, quad nand gate U6270 (shown in four locations), and inverter U6320. U6301 is employed as a flipflop that is set when Received Reset-0 (RRSET-0) is first asserted. Two milliseconds later the counter U6301 resets the flip-flop, which desasserts External Reset-0. Reset signals from the ICU (Insane-0) and power supply (PSINIT-0) are placed on the External Reset-0 path. This allows them to be input to the clock generator block as Received Reset-0, and the Reset Pulse Stretcher operates in the same fasion as described above.

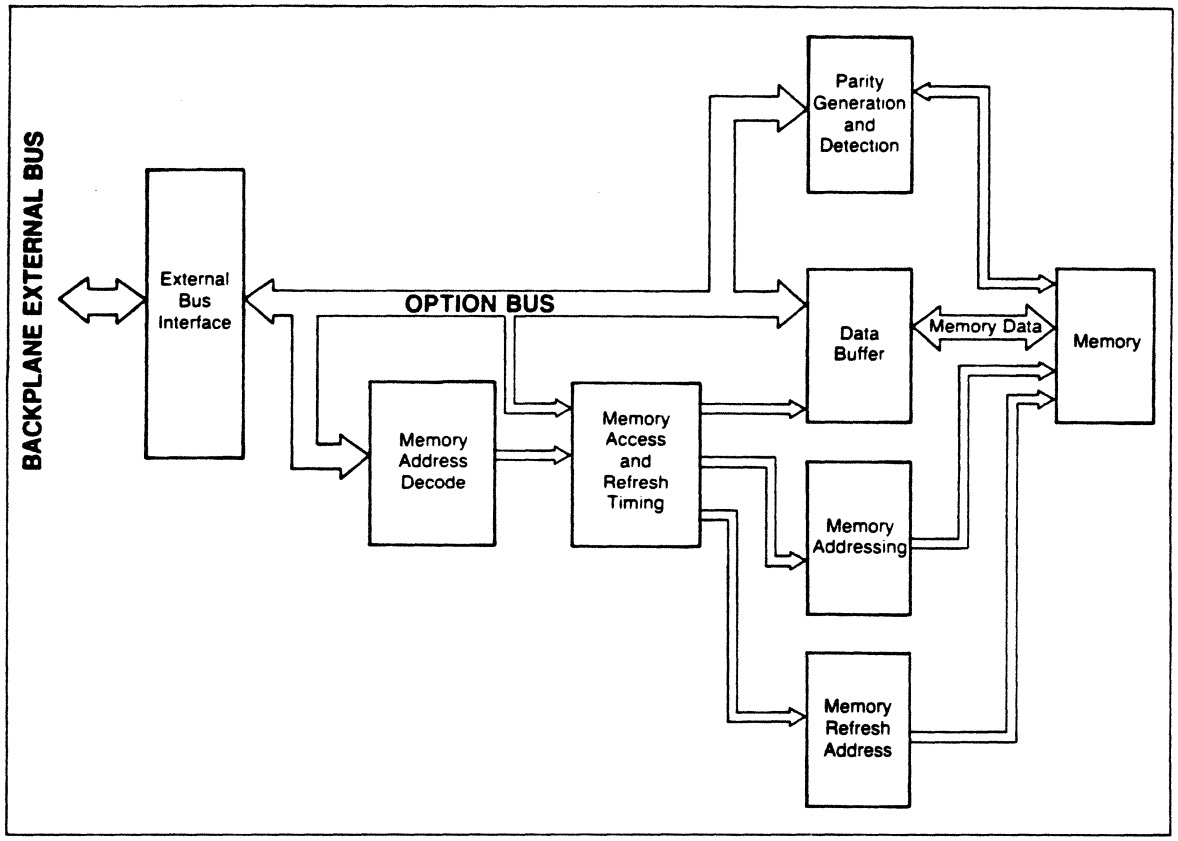
TIME-OF-DAY CLOCK (9)

This block consists of a MM58167 microprocessor-compatible real-time clock and a 32.768 KHz reference crystal oscillator. The clock contains a real-time counter, 56-bits of RAM, two interrupts, and a comparator. The RAM is used during power-down storage and as the alarm latch for comparison to the counter. Address interface with the CPU is via the five low-order bits (IA0-IA5) of the latched Internal Address Bus. Data interface with the CPU is via the low byte of the Internal Address/Data Bus. Battery back-up is provided for the clock by a 3 volt, 1200 milliampere/hour lithium battery and associated power-fail logic.

Section 3

EXPANSION MEMORY BOARD

ILLUSTRATIONS



Expansion Memory Board Block Diagram

Section 3

EXPANSION MEMORY BOARD

INTRODUCTION

This section discusses the use and operation of te Expansion Memory Board for Big Build. This discussion does not necessarily apply to the final production product. This contents of this section are organized as follows:

- Expansion Memory Board Overview"
- Board Configuration
- Functional Block Description

EXPANSION MEMORY BOARD OVERVIEW

The Expansion Memory board is a double-width option board that provides additional main memory for the TEK6100 workstation. The amount of memory provided by the board is dependent on the density of the memory chip used. Using 64K X 1-bit memory chips provides 256K bytes of memory in a fully populated board. Using 256K x 1-bit chips provides 2 megabytes on a fully populated board. (The Big Build version of this board uses 64-kbit chips only)

BOARD CONFIGURATION

The Big Build version of this board will use 64-kbit chips only. If necessary, refer to the schematic diagrams for jumper information. Additional configuration information will be provided at a later date.

FUNCTIONAL BLOCK DESCRIPTION

The Expansion Memory board is comprised of eight major functional blocks that are listed below and discussed in the following paragraphs:

- External Bus Interface Logic
- Memory Address Decode Logic
- Memory Access and Refresh Timing
- Refresh Logic
- Parity Generation and Check Logic
- Memory Address Logic
- Memory Data Buffer
- Memory

EXTERNAL BUS INTERFACE LOGIC

This block provides the electrical interface between the External Bus and the Option Bus located on the Expansion Memory board. This function is performed by a 74F373 octal D-type flipflop (U102) and two 74ALS245 octal bus transceivers (U9103 and U9104) along with associated logic. U102 latches bits 16-23 of the address word, while U9103 and U9104 provide bidirectional interface for bits AD00 - AD15 of the External Bus.

MEMORY ADDRESS DECODE LOGIC

Address decoding for the memory board is provided by a 25LS251 equal-to comparator (U9105, which decodes the memory board CSR address) and the U9113 programmable array logic (PAL) chip.

The comparator decodes the CSR address by comparing the predetermined Status Select Lines SS0-SS4 with bits 11-15 of the Option Bus. A match selects the memory board CSR. Data is latched into the CSR on the trailing edge of Data Enable (DEN-1). DEN-1 is the inverted equivalent of External Data Enable (EDEN-0).

The PAL U9113 decodes bits 17-23 of the address word and outputs the appropriate bank select signal to memory, as well as an additional memory-access control signal. The P0-P2 signals input to the PAL define a 3-bit program code that is loaded into the CSR by the host. This code is used to map the memory into the desired address space. The U9113 PAL is also used during memory refresh in the generation of the row address strobes.

Control and Status Register

The passing of status and control information between the host and the memory board is permitted by the Control and Status Register (CSR). The CSR is a 16-bit read/write register that consists of a 74LS273 octal D-type flipflop U9120, and two 74ALS244 octal bus transceivers (U9121 and U9122).

The contents of the CSR is dependant whether the host is writing to the CSR or reading from it. During a CSR write, the host loads the CSR with memory mapping program bits (P0-P2) and parity logic control bits. During a read from the CSR, bus transceivers U9121 and U9122 permit the host to read the mapping program bits, parity status information, and a code that defines the option type.

The contents of the CSR during a CSR write is defined below:

D15	D14-D12	D11	D10	D09	D08	D07-D00
N.U.	P2-P0	N.U.	N.U.	PBAD-1	PARE-1	N.U.

Figure 3-1. The Control and Status Register During CSR Write.

Program Bits P2-P0. This is a 3-bit code that is used by the host to map the memory board into the desired location within address range of the host. There are eight possible mapping locations.

PBAD-1. PBAD-1 (Parity Bad-1) is a parity logic test bit that is set by the host to force the generation of bad parity during a memory write. The host then reads from the same location and generates valid parity, and then compares the stored parity value against the valid bit.

PARE-1. PARE-1 (Parity Enable-1) is set by the host to enable the parity logic. Writing a zero to this location disables parity.

The CSR contains the following information during a CSR read operation.

D15	D14-D12	D11	D10	D09	D08	D07-D00
N.U.	P2-P0	IRQ-0	N.U.	PERHI-1	PERLO-1	DEV TYPE

Figure 3-2. The Control and Status Register During CSR Read .

P2-P0. This is the mapping code that is defined above. This feature allows host to read back this value.

IRQ-0. IRQ-0 (Interrupt Request-0) is asserted by the memory board after a parity error is detected.

PERHI-1. PERHI-1 (Parity Error High-1) is set by the memory board when a parity error is detected on the high byte (bits 08-15).

PERLO-1. PERLO-1 (Parity Error Low-1) is set by the memory board when a parity error is detected on the low byte (bits 00-07).

DEV TYPE. DEV TYPE (Device Type) bits 00-07 of the CSR register contain an 8-bit code that is used to identify the option device type that is located at a given option slot. The hexadecimal value that is assigned to the double-width expansion memory board is 18 through 1F. Bit 01 of the code defines whether the board is equipped with 64K (0) or 256K chips (1). Bit 00 defined whether the board is half-populated (1) or fully-populated (0).

MEMORY ACCESS AND REFRESH TIMING

This block coordinates the memory refresh cycle, which is performed approximately every 14.5 microseconds, and normal memory accesses. The refresh clock (REFCLK-1) operates at approximately 69.5 KHz and initiates a refresh cycle on the rising edge of the clock pulse. This block then samples RAM Select (RAMSEL-1) to insure that a memory access is not imminent. IF RAMSEL-1 is asserted, the refresh cycle is aborted until the memory access is completed (this function is performed by U9304 at pin 4). After a refresh is in process, memory accesses are locked out until the refresh is completed (this function is performed by U9302 at pin 10). Refer to page 3 of the schematic diagrams.

This block employs a 200 nanosecond delay line to establish memory access and refresh cycle timing. The data-read cycle from memory requires approximately 400 nanoseconds, whereas the data-write cycle can be extended beyond 400 nanoseconds.

REFRESH LOGIC

Once a refresh cycle has been initiated by the memory access and refresh timing block, the memory refresh logic executes the memory refresh. This block supports a distributed refresh method whereby only one memory row is refreshed per refresh cycle. The next refresh cycle increments a refresh row address counter by one in preparation for that cycle. The counter is incremented on the trailing edge of the REFCLK-1. After the new row address has been placed on the Memory Address Bus, all four row address strobes RAS1-0 through RAS4-0) are pulsed to refresh the memory bit locations in that row.

PARITY GENERATION AND CHECK LOGIC

This block generates odd parity for both the high and the low byte during memory writes and checks parity for both bytes during memory reads. The block uses a 74F280 parity generator/checker for both the high and low bytes. If, during a memory read a parity error is detected, the parity error signal is generated that also indicates whether the error applies to the high byte or the low byte.

MEMORY ADDRESS

Memory addressing is performed by two 74F373 octal D-type flipflops (see page 2 of the schematic diagrams), which are used to demultiplex the 16-bit Option Bus address onto 8-bit Memory Address Bus, along with associated Row Address Strobe (RAS) and Column Address Strobe (CAS) logic. RAS and CAS signals are used to latch the memory address into memory. See page 3 of the schematic diagrams.

MEMORY DATA BUFFER

Two 74F373 octal D-type flipflops (U9202 and U9203) act as buffers between the 16-bit Memory Data Bus and the multiplexed Option Bus. See page 2 of the schematic diagrams.

MEMORY

The memory board is organized electronically as four banks of 18 chips each. Each bank is organized as two 8-bit bytes with parity. The board can be configured either fully populated or half populated. The use of 64K x 1-bit memory chips provides 256k bytes of memory on a fully populated board, whereas a fully populated board using 256K x 1-bit chips provides 2 megabytes of memory. Board population and chip density are selected by jumper configuration.

Section 4

HARD COPY INTERFACE BOARD

ILLUSTRATIONS

TABLES

Section 4

HARD COPY INTERFACE BOARD

INTRODUCTION

This section describes the installation, use, and operation of the Hard Copy Interface Board. The contents of this section are organized as follows:

- Option Overview
- Option Board Configuration
- Special Registers
- Block Level Hardware Description

OPTION OVERVIEW

The Hard Copy Interface board is a single-width option board that provides two independent Centronix-type parallel interface ports for the TEK 6100 family of workstations. Each port provides communication with, and control of, peripheral devices via a parallel data bus and associated control signals.

OPTION BOARD CONFIGURATION

This section describes the jumpers that are used to configure the option board and also describes the peripheral interface connectors.

DEVICE ID JUMPERS

The device ID jumpers are configured at the factory during manufacturing and are not configurable by the user.

SIGNAL TERMINATION JUMPERS

There are four 8-bit DIP switches that, when installed (or closed), connect all inputs from the peripherals to 100 ohm pull-up resistors and removes the 33 ohm series termination resistors on all outputs. These DIP switches are removed (or opened) when driving a standard Centronix peripheral, and installed when driving modified instruments that have input terminations, such as the Tektronix 4691 and 4692 copiers.

OPTION BASE ADDRESS CONFIGURATION

The base address for the option board is determined by which slot the board occupies. Refer to the Installation section at the front of this document for more information.

HARD COPY PORT HARDWARE INTERFACE

Electrical interface for each hard copy port is provided by an AMP connector, part number 102893-3. The connectors are attached to the rear of the board and are accessable at the rear of the box when the board is installed.

SPECIAL REGISTERS

The Hard Copy Option Board contains eight registers, two of which are DMA Control registers and six of which are option configuration, status, and data registers. Each register is defined below. All register addresses are given relative to the base address of the board. The base address of the board is dependent on the option slot in which it is installed. Refer to the Installation section at front of this document for option board installation information.

DEVICE ID REGISTER

This is 8-bit (D0-D7) read-only register is located at relative address 0. This register defines one of three possible option configurations, as indicated below:

Table 4-1

HARD COPY INTERFACE DEVICE ID CODES

ID Code (Hex)	Board Configuration
D	Single Port board, no DMA support
E	Single Port board, with DMA support
F	Dual Port board, with DMA support

DMA CONTROLLER POINTER REGISTER

This 6-bit read/write register (D0-D5) is located at relative address 02. This register contains the address of the internal register to be accessed by the host. Valid addresses for this register are provided in the AMD 9516 DMA Controller data manual

DMA CONTROLLER ACCESS REGISTER

This 16-bit read/write register (D0-D15) is located at relative address 04. The register provides access to all of the DMA controller registers. The contents written to this register by the host are transferred to the DMA control register specified by the address located in the pointer register. The format of the data placed in this register is dependent on the register that is being accessed. Refer to the DMA controller data manual for more information. When this register is read, the cycle is delayed by approximately 2 microseconds to allow for slow registers.

PORT 1 DATA REGISTER

This 8-bit read/write register (D0-D7) is located at relative address 06. It is the interface between the option address/data bus and the port 1 data path. All data transferred from the option bus to the peripheral bus are aligned on the low byte (D0-D7) of the option bus. The host can read the last byte sent to the peripheral by reading the contents of this register.

PORT 1 CONFIGURATION REGISTER

This 6-bit (D0-D5) read/write register is located at relative address 08. This register is used to establish the configuration of the port 1 interface.

The contents of the Port 1 Configuration register are defined below:

05	04	03	02	01	00
RST1-1	SM1-1	AIE1-1	BTEI-1	BLEI-1	ME1-1

Figure 4-1. Port 1 Configuration Register.

RST1-1, Bit 05

RST1-1 (Reset 1-1), when set, issues a hardware rest to the peripheral. Reset remains asserted until it is cleared by the host.

SM1-1, Bit 04

SM1-1 (Stream Mode 1-1), when set, places port 1 in the streaming mode of operation. This mode can be used by some peripherals to increase data transmission rates. In the streaming mode, if DMA is being performed, the next transfer is initiated immediately after the current byte is transferred, without waiting for the peripheral to assert Acknowledge-1. The streaming mode has no affect on non-DMA transfers. When this bit is cleared, the port returns to the normal mode of operation.

AIE1-1, Bit 03

AIE1-1 (Acknowledge Interrupt Enable 1-1) is set by the host to enable the generation of an interrupt on the assertion of Acknowledge-1 by the port 1 peripheral. Clearing AIE1-1 causes the interrupt control logic to ignore the Acknowledge signal.

BTEI-1, Bit 02

Setting this bit (Busy Trailing Edge Interrupt-1) enables an interrupt to be generated to the host whenever the port 1 Busy-1 line is deasserted by the peripheral. This interrupt is generated by the trailing edge of Busy-1. Clearing this bit causes the interrupt logic to ignore the trailing edge of Busy, and no interrupt is generated.

BLEI-1, Bit 01

Setting this bit (Busy Leading Edge Interrupt-1) enables an interrupt to be generated to the host whenever the port 1 Busy-1 line is asserted by the peripheral. This interrupt is generated by the leading edge of Busy-1. Clearing this bit causes the interrupt logic to ignore the leading edge of Busy, and no interrupt is generated.

ME1-1, Bit 00

ME1-1 (Master Enable 1-1) is set by the host to enable interrupts to be generated by the port. Clearing this bit still allows the Interface Status register to store status information, but keeps the port status lines from generating an interrupt to the host.

PORT 2 DATA REGISTER

This 8-bit (D7-D0) read/write register is located at relative address 0A. It is the interface between the option address/data bus and the port 2 data path. All data transferred from the option bus to the peripheral bus are aligned on the low byte (D0-D7) of the option bus. The host can read the last byte sent to the peripheral by reading the contents of this register.

PORT 2 CONFIGURATION REGISTER

This 6-bit (D0-D5) read/write is register located at relative address 0C (Hex). This register is used to establish the configuration of the port 2 interface. Each bit is defined below:

05	04	03	02	01	00
RST2-1	SM2-1	AIE2-1	BTEI-1	BLEI-1	ME2-1

Figure 4-2. Port 2 Configuration Register.

RST2-1, Bit 05

RST2-1 (Reset 2-1), when set, issues a hardware reset to the peripheral. Reset remains asserted until cleared.

SM2-1, Bit 04

SM2-1 (Stream Mode 2-1) when set, places port 2 in the streaming mode of operation. This mode can be used by some peripherals to increase data transmissions rates. In the streaming mode, if DMA is being performed, the next transfer is initiated immediately after the current byte is transferred, without waiting for the peripheral to assert Acknowledge-1. The streaming mode has no effect on non-DMA transfers. When this bit is cleared, the port returns to the normal mode of operation.

AIE2-1, Bit 03

AIE2-1 (Acknowledge Interrupt Enable 2-1) is set by the host to enable the generation of an interrupt on the assertion of Acknowledge-1 by the port 2 peripheral. Clearing AIE2-1 causes the interrupt control logic to ignore the Acknowledge signal.

BTEI-1, Bit 02

Setting this bit (Busy Trailing Edge Interrupt-1) enables an interrupt to be generated to the host whenever the port 2 Busy-1 line is deasserted by the peripheral. This interrupt is generated by the trailing edge of Busy-1. Clearing this bit causes the interrupt logic to ignore the trailing edge of Busy, and no interrupt is generated.

BLEI-1, Bit 01

Setting this bit (Busy Leading Edge Interrupt-1) enables an interrupt to be generated to the host whenever the port 2 Busy-1 line is asserted by the peripheral. This interrupt is generated by the leading edge of Busy-1. Clearing this bit causes the interrupt logic to ignore the leading edge of Busy, and no interrupt is generated.

ME1-1, Bit 00

ME1-1 (Master Enable 1-1) is set by the host to enable interrupts to be generated by the port. Clearing this bit still allows the Interface Status register to store status information, but keeps the port status lines from generating an interrupt to the host.

INTERFACE STATUS REGISTER

This 16-bit read-only register is located at relative address 0E and contains all of the status information for both ports. This register is usually read by the host after an interrupt has been generated to determine the cause of the interrupt. When this register is read, all bits capable of generating an interrupt are cleared, except bit 0. Bit 15 (Master Interrupt Pending) is also cleared. The contents of this register are defined below:

15	14	13	12	11	10	09	08
MIP-1	BIP2-1	ACKIP2-1	ACK2-1	FLT2-1	BSY2-1	PE2-1	SEL2-1

Interface Status Register High Byte

07	06	05	04	03	02	01	00
BIP1-1	ACKIP1-1	ACK1-1	FLT1-1	BSY1-1	PE1-1	SEL1-1	DIP1-1

Interface Status Register Low Byte

Figure 4-3. Hard Copy Interface Status Register.

MIP-1, Bit 15

This bit (Master Interrupt Pending-1), when set, indicates that the DMA Controller has an interrupt pending. This occurs when any of bits 0, 6, 7, 13, or 14 of the Interface Status Register are set.

Bits 14-8 of the Interface Status register apply to port 2.

BIP2-1, Bit 14

This bit (Busy Interrupt Pending 2-1), when set, indicates that a Busy Interrupt from the port 2 peripheral is pending. The conditions that will enable the generation of this interrupt are selected by bits 1 and 2 of the Port 2 Configuration Register.

ACKIP2-1, Bit 13

This bit (Acknowledge Interrupt Pending 2-1), when set, indicates that an Acknowledge Interrupt is pending from the port 1 peripheral.

ACK2-1, Bit 12

This bit (Acknowledge 2-1), when set, indicates that Acknowledge been asserted by the port 2 peripheral since that the last reading of this register.

FLT2-1, Bit 11

This bit (Fault 2-1), when set, indicates that the port peripheral is off-line (deselected) and/or is out of paper.

BSY2-1, Bit 10

This bit (Busy 2-1), when set, indicates that the peripheral on port 2 has been deselected, is out of paper, or the data buffer is full.

PE2-1, Bit 09

This bit (Paper Empty 2-1), when set, indicates that the peripheral on port 2 is out of paper.

SEL2-1, Bit 08

This bit (Select 2-1), when set, indicates that the peripheral on port 2 is in the selected state.

BIP1-1, Bit 07

This bit (Busy Interrupt Pending 1-1), when set, indicates that a Busy Interrupt from the port 1 peripheral is pending. The conditions that will enable the generation of this interrupt are selected by bits 1 and 2 of the Port 1 Configuration Register.

ACKIP1-1, Bit 06

This bit (Acknowledge Interrupt Pending 1-1), when set, indicates that an Acknowledge Interrupt from the port 1 peripheral is pending.

ACK1-1, Bit 05

This bit (Acknowledge 1-1), when set, indicates that the Acknowledge signal has been asserted by the port 1 peripheral since the last time the register was read.

FLT1-1, Bit 04

This bit (Fault 1-1), when set, indicates that the port peripheral is off line (deselected) and/or is out of paper.

BSY1-1, Bit 03

This bit (Busy 1-1), when set, indicates that the peripheral on port 1 has been deselected, is out of paper, or the data buffer is full.

PE1-1, Bit 02

This bit (Paper Empty 1-1), when set, indicates that the peripheral on port 1 is out of paper.

SEL1-1, Bit 01

This bit (Select 1-1), when set, indicates that the port 1 peripheral is in the selected state.

DIP1-1, Bit 00

This bit (DMA Interrupt Pending 1-1), when set, indicates that the DMA Controller has an interrupt pending.

FUNCTIONAL BLOCK DESCRIPTION

The Hard Copy Interface board comprises of six major functional blocks that are listed below.

- External Bus Interface and Address Decode Logic
- DMA Control Block
- Interface Status and Configuration Registers
- Port 1 Data/Protocol Interface
- Port 2 Data/Protocol Interface
- Interrupt Control Block

Each of the functional blocks are discussed in the following paragraphs. Refer to the block diagram of the board shown in figure 1-1 and the schematic diagram.

EXTERNAL BUS INTERFACE AND ADDRESS DECODE LOGIC

This block provides the electrical interface between the External Bus and the multiplexed address/data bus on the option board, as well as address recognition for the hard copy interface option board. External Bus electrical interface is provided by three 74LS245 octal bus transceivers.

Address recognition is performed by a 25LS2521 Equal-to comparator that compares address lines AD11-AD18 of the on-board address bus against the predefined slot select lines SS0-SS4. A match indicates that the board has been addressed and lets the host access the option board status, control, and data registers.

Associated with the address recognition logic is the Device Register. This 8-bit, read-only register contains the jumper-selected, 8-bit ID word assigned to the Hard Copy Interface Board. The register consists of a 74LS244 bus transceiver (U1020) that is output-enabled by the address recognition logic. The contents of this register are read by the host at power-up and system reset.

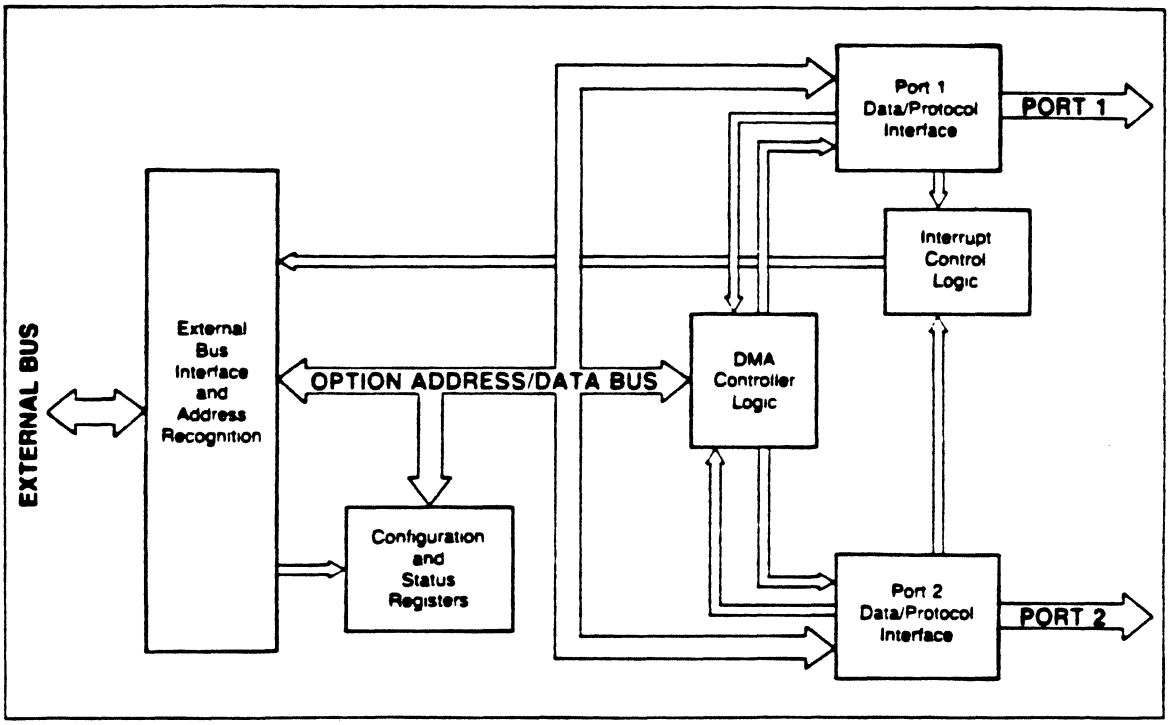


Figure 4-4. Hard Copy Option Board Block Diagram.

Register Address Decode

This option board contains 6 registers that are mapped into the address space of the host. These registers are accessed for read or write operations by two 74LS138 3-to-8 decoders and enabled by the address recognition logic described above. All board-level registers other than DMA Control Registers are discussed in a previous section of this document titled "Special Registers".

DMA CONTROL BLOCK

The DMA Control Block comprises a AMD 9516 DMA Controller and associated support logic. This block executes the protocols necessary for data transfer from the the External Bus (host side) to the peripherals. Each port is completely independent of the other. DMA transfers are initiated by the host by loading DMA control parameters into a control block known as the Chain Control Table. The Chain Control Table is maintained in main memory by the host. The host also programs two registers internal to the controller known as the Master Mode Register, which controls chip-level interface parameters, and the Chain Address Register, which

contains the address of the Chain Control Table. The host then issues a Start command to the controller, which proceeds to copy the contents of the Chain Control Table into its own internal registers and execute the transfer. Only fly-by transfers are supported by this interface.

The DMA Control Block includes the logic necessary to support the External Bus bus protocol, such as the Bus Request/Bus Grant flip-flop U3070, the bus protocol signal driver U4030, the Wait State Generator (flip-flop U5070, pin 8), and associated logic. During a DMA cycle, the Wait State Generator asserts a WAIT to the DMA controller on the assertion of Address Latch Enable by the controller. The DMA controller samples WAIT at T2 and maintains data on the bus until BTACK-0 (Bus Transfer Acknowledge) is asserted by the host. At that time, WAIT is cleared and the bus cycle finishes. The DMA Control Block will be discussed more thoroughly in later documenation.

INTERFACE STATUS AND CONFIGURATION REGISTERS

This functional block consists of six board-level registers that are accessed by the Register Address Decode logic discussed previously in this section. The use of each register differs to the extent that each register is discussed in the appropriate functional-block description rather than being grouped together in this subsection.

PORT 1 DATA/PROTOCOL INTERFACE

The port 1 data interface consists primarily of a 29825 octal bus buffer, U5110, which places data and protocol signals on the bus, and a counter which allows the voltage levels on the port 1 data path to stabilize before issuing Strobe 1-0 and validating the data. The data buffer is loaded by a write operation to the buffer by the DMA Controller or the host. Clock 1-1 is issued on the trailing edge of either Write 6-0 (WT6) (in the non-DMA mode) or DACK1 (in the DMA mode). Clock 1-1 latches the data into the bus buffer U5110 and also clocks a timer-control flip-flop (U4100). This in turn allows a dual 4-bit binary counter (U3100) to begin incrementing on a 16 Mhz clock pulse. After approximately 1 microsecond, a 1 microsecond high-active strobe is issued by the counter and inverted by U2100. This strobe is issued to the port 1 interface as STB1-0. On the trailing edge of the strobe, a clear signal is issued by the counter to the timer control flip-flop U4100, which resets the counter.

Hardware on the board allows the host to read back the most recent byte written to the port 1 peripheral. This feature is used primarily for diagnostic purposes and takes advantage of the fact that the port 1 bus driver latches each byte of data that it places on the port data path. The port 1 read back logic consists of a 74LS244 octal bus transceiver (U1100) that is enabled by executing a read from the Port 1 Data Register, relative address 06.

PORT 2 DATA/PROTOCOL INTERFACE

The Port 2 data/protocol interface uses logic identical to the port 1 interface and operates in the same fashion. The Port 2 Data Register is 29825 octal bus buffer (U2110). The counter is U4105. The timer-control flipflop is U4090. The read-back logic for the Port 2 Data Register consists of the octal buffer U1101. Refer to the above description.

INTERRUPT CONTROL BLOCK

The interrupt control logic samples for specified status conditions that are generated by the port 1 and port 2 peripherals and generates an interrupt request to the host. Information pertaining to the cause of the interrupt is placed in the Interface Status Register. When an interrupt is sent to the host, the host can then read the Interface Status Register to determine the cause of the interrupt. The specific status conditions that will generate an interrupt request for a given port are selected by the contents of configuration register associated with that port.

The Port 1 Configuration Register (register 8) consists of a 74LS374 octal D-type flip-flop (U1080), which is write-enabled by the address decode logic, and a 74LS244 octal buffer (U1090), which is the register-read mechanism for the host. The Port 2 Configuration register consists of identical components (U2080 and U2090) and operates in the same fashion.

Configuration information for each port is passed to the Status Select PAL (2070) which samples the selected status lines for each port. When a selected status line is asserted, it is latched by the Status Select PAL and passed to the Interrupt Request and Status Latch PAL U2060. U2060 then generates an interrupt request to the host. The host can then read the contents of the Interface Status Register to determine the cause of the interrupt.

The Interface Status Register is broken into two components. PAL U2060 latches status information selected by the port configuation registers and the 74LS244 octal driver U1060 also forwards port status information. A read of the Interface Status Register by the host output-enables both devices.

Section 5

HIGH SPEED GENERAL PURPOSE INTERFACE BUS

ILLUSTRATIONS

TABLES

Section 5

HIGH SPEED GENERAL PURPOSE INTERFACE BUS

INTRODUCTION

This section discusses the High Speed GPIB option for the 6100 Series workstations. The text includes a general explanation of the option, plus a register description, a block diagram, and a functional block description. The text is divided into the following headings:

- Hardware Overview
- Option Board Configuration
- Special registers
- Functional Block Description

NOTE

The material in this section refers only to the "bigbuild" version of the I/O Processor circuit board. Although the production version is expected to be similiar to this circuit board, there will be some variation.

HARDWARE OVERVIEW

The General Purpose Interface Bus (GPIB) is a standardized parallel interface for programmable instrumentation. It is defined by the IEEE Standard 488-1980.

The High Speed GPIB option for the 6100 Series comes on a single half-width option board, which can be installed in the Options Backplane. There is one GPIB port per board. This option can be configured as a talker, listener, or controller. It is also designed to work in a multicontroller environment, and to terminate direct memory transfers by end-of-message byte detection. The transfer rates for this option are 500 kbytes/sec in the listener mode and at least 300 kbytes/sec in the talker mode. The GPIB is able to attain these high speeds because of a cache RAM designed into its architecture.

BUS SIGNALS

The following paragraphs list and define the bus signal names used in this section. There are two groups of signals in the list: the 6100 data bus signals used during a data transfer, and the signals for the GPIB interface.

6100 Data Bus Signals

The following handshake signals are used during data transfers between the 61PE10 and the GPIB option.

EAV-0 EAV-0 (External Address Valid-0) is pulsed by the 61PE10 to indicate that an address on the address bus is now valid.

EDEN-0 EDEN-0 (External Data Enable-0) goes true in two possible circumstances:

- During a 61PE10 data-read, EDEN-0 precedes the loading of data onto the data bus.
- During a 61PE10 data-write, EDEN-0 follows the loading of data onto the data bus.

ETAK-0 ETAK-0 (External Transfer Acknowledge-0) is asserted from the GPIB board to the 61PE10 to indicate that data has been captured or placed on the bus.

GPIB Signals

GPIB control signals are divided into two groups: Management Bus signals and Transfer Bus signals. Management Bus signals are general control signals. Transfer Bus signals are used specifically for handshaking during a data transfer. Some Transfer Bus signals are similar (but not identical) in title and operation to the 6100 data bus signals described above, and therefore must be distinguished to avoid confusion.

Management Bus.

ATN-0 ATN-0 (Attention-0) is asserted by the controller to assign other devices as talkers or listeners, or when the controller is giving universal commands to all devices on the GPIB.

SRQ-0 SRQ-0 (Service Request-0) is asserted by any device on the bus when that device wants the controller's attention.

IFC-0 IFC-0 (Interface Clear-0) is asserted by the controller to put all devices on the bus into a known quiescent state.

REN-0 REN-0 (Remote Enable-0) is asserted by the controller to transfer devices from manual operation to remote control in some GPIB applications.

EOI-0 EOI-0 (End Or Identify-0) may be asserted by a talker during the last byte of a data transfer. In this application EOI-0 marks the end of the data transfer. EOI-0 may also be asserted in conjunction with ATN-0 by a controller to perform a parallel poll.

Transfer Bus.

NRFD-0 NRFD-0 (Not Ready For Data-0), when true, indicates that one or more listeners on the bus are not ready to receive the next data byte. This prevents the talker from placing a new data byte on the bus.

DAV-0 DAV-0 (Data Valid-0) is asserted by the talker shortly after a data byte is placed on the bus. DAV-0 tells each listener to capture the data presented on the bus.

NDAC-0 NDAC-0 (Not Data Accepted-0) is held true (low) until all listeners have captured the present data byte. Then it is released and allowed to float high, which signals the talker that it may remove the data byte from the bus.

OPTION BOARD CONFIGURATION

The High Speed GPIB option contains no straps or jumpers to be set prior to installation. Refer to the Section 1 of this document for guidelines about proper installation.

The base address for the option board is determined by the slot into which the board is installed. Refer to the *OEM Manual*, Section 5, for base address designations of the option slots.

SPECIAL REGISTERS

The High Speed GPIB contains eight special registers in addition to those registers internal to the TMS9914A GPIB controller chip. These external registers are described in the following paragraphs. For detailed information about the TMS9914A registers, refer to the data sheet for that chip.

The eight special registers are:

- Type register
- Cache RAM Mapping register
- Status buffer
- Board register
- Diagnostic register
- Byte Counters
- Address Counters
- End-of-Message Byte Select register

Table 5-1 shows the address offsets for the various registers on the High Speed GPIB board.

Table 5-1

HIGH SPEED GPIB REGISTER ADDRESS OFFSETS

ADDRESS OFFSET	REGISTER	
	READ	WRITE
00	Type	--------
02	--------	Cache RAM Mapping
04	Status	Board/Diagnostic
06	Byte Counters	Byte Counters
08	--------	Address Counters
0A	--------	End-of-Message
10-1F	TMS9914A (see data sheet for details)	TMS9914A (see data sheet for details)

TYPE REGISTER (ADDRESS 00)

The Type register identifies the High Speed GPIB board. Each option board that installs into the options backplane of the workstation has a unique hex code that identifies that particular option. The 61PE10 reads base address 00 at all option slots during system initialization and identifies which options are present according to the hex codes found. The hex code for the High Speed GPIB is 01. The Type register presents this number on data bits BD0-BD7.

CACHE RAM MAPPING REGISTER (ADDRESS 02)

The Cache RAM Mapping register performs two functions for the GPIB board:

- Mapping the Cache RAM within system address space.
- Enabling or disabling the Cache RAM.

Refer to the Functional Block Description for the Cache RAM Logic block for more information.

The Mapping register generates one signal which is listed below:

M RAM SEL-1

M RAM SEL-1 (Mapping RAM Select-1) indicates that the 61PE10 wants to access the Cache RAM. The signal is sent to the Control PAL, which then enables the Cache.

STATUS BUFFER (ADDRESS 04)

The Status buffer stores the current states of several control lines. This read-only buffer uses data bits BD0-BD10. The 61PE10 uses this buffer to check the status of these control lines. Fig. %-1 illustrates the bit designations for this buffer.

10	9	8	7	6	5	4	3	2	1	0
EGPIBD-1	SC-1	NRFDS-1	DBM-1	DMADIR-0	DMASER-1	EDMAI-1	EEOM-1	CO-0	EOMI-0	ITMS-0

Figure 1-1. Status Register Bit Designation.

Most of the control signals stored by the Status register are generated by the Board register. Those signals that originate from sources other than the Board register are listed and explained below:

DBM-1 — DBM-1 (Diagnostic Byte Match-1) comes from the End-of-Message Byte Select. It is used for diagnostic purposes. See the functional description of End-of-Message Byte Select for more explanation.

CO-0 — CO-0 (Carry Out-0) comes from the Byte Counters. It indicates that the counters have reached maximum count (that is, the last byte in a data transfer has been transferred).

EOMI-0 — EOMI-0 (End-of-Message Interrupt-0) indicates that the End-of-Message Byte Select has detected an end-of-message character. This is the *interrupt pending* bit for the end-of-message function. It is cleared by the Board register (CNRFD-0).

ITMS-0 — ITMS-0 (Interrupt from TMS9914A-0) is an interrupt request generated by the TMS9914A.

BOARD REGISTER (ADDRESS 04)

The Board register is a write-only register that drives a number of control lines used on the GPIB board. The register latches input data from bus data lines BD0-BD7. Fig. %-2 illustrates the bit designations for the Board register.

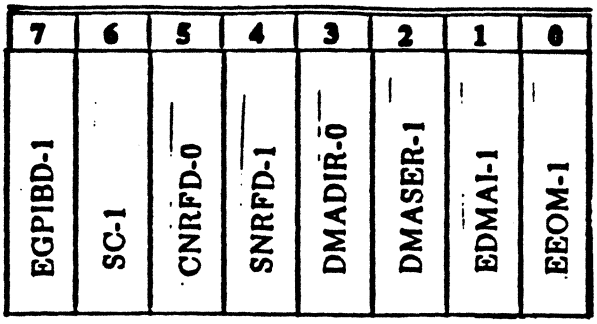


Figure 1-2. Board Register Bit Designation.

The Board register output signals are listed and explained below.

EGPIBD-1 EGPIBD-1 (Enable GPIB Driver-1) causes the GPIB driver chips (in the GPIB Controller Interface circuit) to power up. The driver chips do not power up when the circuit board is first initialized so that stray signals are not transmitted on the GPIB bus.

SC-1 SC-1 (System Controller-1) enables the GPIB board to function as a system controller for the GPIB bus.

CNRFD-0 CNRFD-0 (Clear Not Ready For Data-0) clears the NRFD signal from the End-of-Message Byte Select circuit.

SNRFD-1 SNRFD-1 (Set Not Ready For Data-1) forces the assertion of NRFD on the GPIB bus.

DMADIR-0 DMADIR-0 (DMA Direction-0) sets the direction of DMA transfers (that is, whether data flows from the TMS9914A to the Cache RAM or from the Cache RAM to the TMS9914A). DMADIR-0 is a *read* operation, which is a transfer from the TMS9914A to the Cache RAM.

DMASER-1 DMASER-1 (DMA Service-1) turns on the DMA State Machine.

EDMAI-1 EDMAI-1 (Enable DMA Interrupt-1) enables the Counter/Interrupt PAL to send interrupts for End-of-Message (EOM) detect and Terminal Count (CO-0).

EEOM-1 EEOM-1 (Enable End Of Message-1) enables the End-of-Message Byte Select.

DIAGNOSTIC REGISTER (ADDRESS 04)

The Diagnostic register manipulates the NRFD-0 and NDAC-0 control lines. (Refer to Bus Signals in the Hardware Overview for definition of NRFD-0 and NDAC-0.) It is a write-only register and uses data bits BD9 and BD10. The register allows software to set up test conditions with the GPIB controller chip (TMS9914A) such that the TMS9914A outputs data on its GPIB interface lines. This supports diagnostics without requiring external test equipment.

The Diagnostic register becomes disabled when the GPIB output drivers are enabled (the EGPIBD-1 signal from the Board register enables the GPIB output drivers). This prevents

interference with the NRFD-0 and NDAC-0 signal outputs from the TMS9914A GPIB controller chip during normal operation of the GPIB.

The Diagnostic register resides at the same address offset as the Board register, but uses the upper byte of the 16-bit data bus (the Board register uses the lower byte).

BYTE COUNTERS (ADDRESS 06)

The Byte Counters count the number of data transfers that occur during a DMA transfer. The 61PE10 writes to these counters to load the initial count. (The initial count must be the ones complement of the number of bytes to be transferred.) The 61PE10 reads these counters to check the current status of the count. Refer to Memory Transfer Counters in the Functional Block Description for more information.

ADDRESS COUNTERS (ADDRESS 08)

The Address Counters generate the addresses for the Cache during a DMA transfer. The 61PE10 writes to these counters to load the initial address. The 61PE10 cannot read these counters. Refer to Memory Transfer Counters in the Functional Block Description for more information.

END-OF-MESSAGE BYTE SELECT REGISTER (ADDRESS 0A)

The End-of-Message Byte Select register monitors the GPIB bus and asserts a signal when a data transfer is complete. The register latches an 8-bit data byte (the one's complement of the designated end-of-message byte) from the 61PE10. When the option is in listener mode, The register monitors all eight lines of the GPIB waiting for a match to occur between the GPIB and the end-of-message byte previously latched. When a match occurs, the register sends an End-of-Message signal to indicate that the data transfer is complete. Refer to GPIB Interface, subsection End-of-Message Byte Select, in the Functional Block Description for more information.

FUNCTIONAL BLOCK DESCRIPTION

The High Speed GPIB consists of nine functional blocks, as follows:

- Bus Interface Logic
- Timing Generator
- Memory Transfer Counters
- Status and Control registers
- DMA State Machine
- Counter/Interrupt PAL

- Control PAL
- Cache RAM Logic
- GPIB Interface

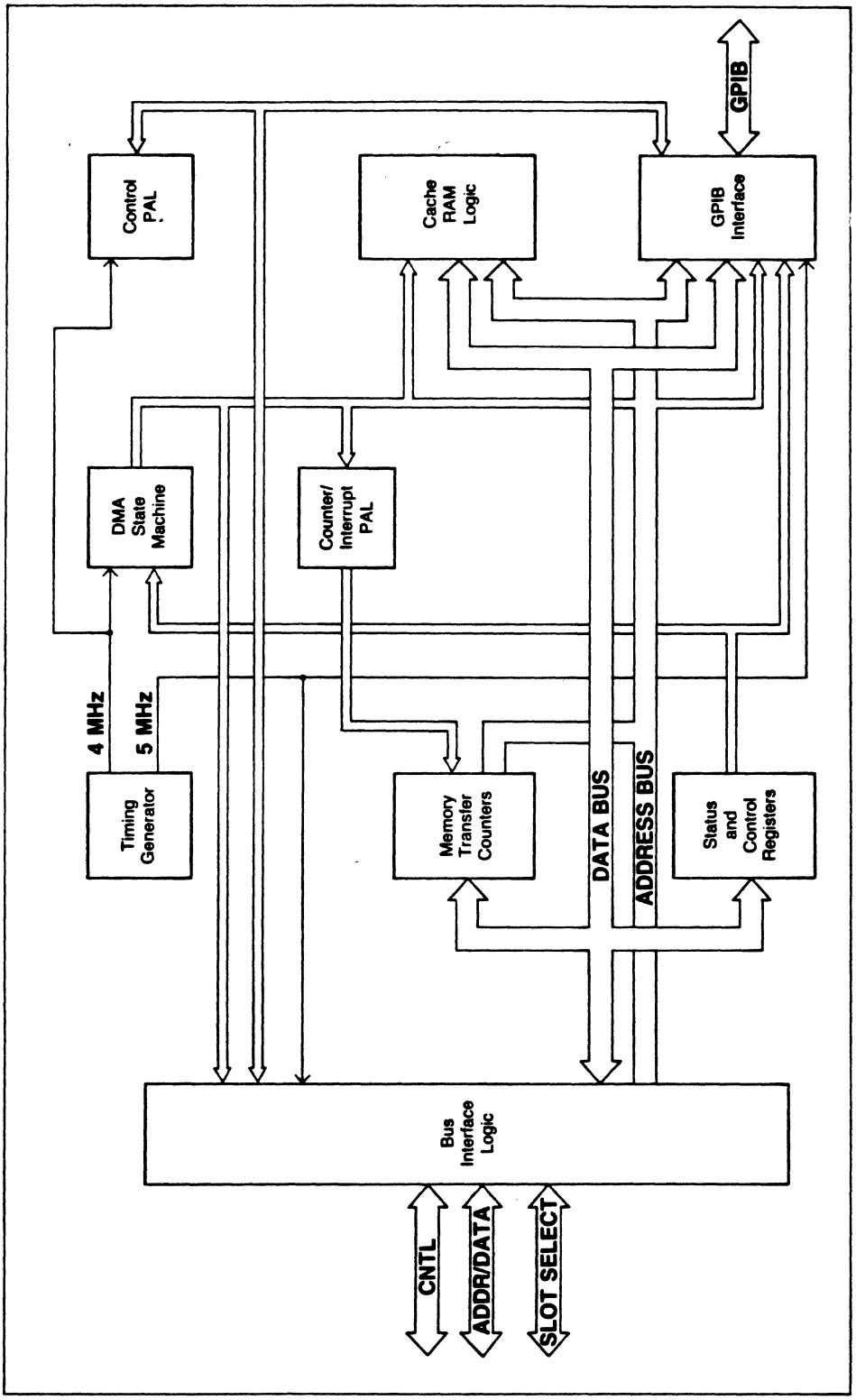


Figure 1-3. Block Diagram for the High Speed GPIB.

The following paragraphs describe the general function for each block of the block diagram.

BUS INTERFACE LOGIC

The Bus Interface Logic performs all of the interface functions between the GPIB board and the External Bus. The functions performed by this block can be broken down into the following circuits:

- Address/Data Bus Interface Logic
- Latched Address Line Decode Logic
- ETAK-0 Signal Circuit

Address/Data Bus Interface Logic

The Address/Data Bus Interface Logic (on page 1 of the schematics) consists of latches and drivers for address and control lines, and bidirectional buffers for data lines. These connect directly to the External Bus.

The incoming address/data lines are not in numerical order. This was done because AD1-AD3 and AD11-AD15 have special functions and are latched together with a single chip. These lines become the Latched Address Lines. The address and data lines are restored to numerical order after passing through the Address/Data Bus Interface portion of the circuitry.

Latched Address Line Decode Logic

Address/data lines AD1-AD3 and AD11-AD15 are clustered together and latched by a single chip (U2010) in the Address/Data Bus Interface Logic. These lines become the Latched Address Lines (LA1-LA3 and LA11-LA15). The Latched Address Lines are decoded by the Latched Address Line Decode Logic (on page 1 of the schematics) and are used to perform various control functions on the circuit board.

The following description divides the Latched Address Lines into two groups: LA1-LA3 and LA11-LA15. The decode circuitry for each group is then briefly discussed.

LA1-LA3. LA1-LA3 are decoded by the following circuits:

Load Selector. The Load Selector (U1080) decodes the Latched Address Lines LA1-LA3 into four LOAD signals. These signals are used as follows:

LEB-0 — LEB-0 (Load End-of-Message Byte Select-0) causes the comparator chip in the End-of-Message Byte Select circuit to latch the data byte currently presented on the data bus lines BD0-BD7.

LMR-0 — LMR-0 (Load Mapping register-0) causes the comparator chip in the Cache RAM Mapping register to latch the data byte currently presented on the data bus lines BD0-BD7.

LAC-0 LAC-0 (Load Address Counters-0) goes to the Counter/Interrupt PAL and initiates control signals to load the Address Counters for a DMA transfer.

LBC-0 LBC-0 (Load Byte Counters-0) goes to the Counter/Interrupt PAL and initiates control signals to load the Byte Counters for a DMA transfer.

There is a fifth LOAD signal generated by the Load Selector that is not designated by a signal name. This signal is gated with BA0 and loads the Board register.

Dump Selector. The Dump Selector (U1090) decodes the Latched Address Lines LA1-LA3 into three DUMP signals. These signals are used as follows:

DAC-0 DAC-0 (Dump Address Counters-0) goes to the Counter/Interrupt PAL and initiates the control signals that cause the Address Counters to output addresses during a DMA transfer.

DBC-0 DBC-0 (Dump Byte Counters-0) causes the Byte Counters to present the current count on the data bus.

DSR-0 DSR-0 (Dump Status register-0) causes the Status register to present its data on the data bus.

There is a fourth DUMP signal generated by the Dump Selector that is not designated by a signal name. This signal dumps the Type register onto the data bus (lines BD0-BD7).

LA1-LA3 also manipulate the Register Select inputs for the TMS9914A GPIB controller chip. Refer to the TMS9914A data sheet for more information about the Register Select function.

LA11-LA15. LA11-LA15 select the circuit board. These lines are compared to the five Slot Select (SS) lines by a comparator chip (U1040). When these two sets of lines match, the signal LATCH BD SELECT-0 is sent to the Control PAL and the circuit board is selected.

ETAK-0 Signal Circuit

The Bus Ack Handshake (on page 2 of the schematics) generates the ETAK-0 signal, which is a handshake signal sent back to the 61PE10 to indicate that a data transfer is complete. Bus Ack Handshake is a timing circuit that sends ETAK-0 only after enough time has elapsed for the slowest device on the circuit board to complete its data transfer operation.

TIMING GENERATOR

The Timing Generator (on page 2 of the schematics) produces two clocks (5 MHz and 4 MHz) for use on the GPIB board.

MEMORY TRANSFER COUNTERS

The Memory Transfer Counters block consists of two sets of counters that work together during DMA transfers. These two counters are the Byte Counters and the Address Counters, and the function of each is described in the following paragraphs.

Byte Counters

The Byte Counters (U1060 and U2060 on page 3 of the schematics) count the number of bytes moved during a data transfer. The 61PE10 can both read from and write to the Byte Counters. These counters operate in the following circumstances:

- During a DMA transfer between the 61PE10 and the Cache
- During a DMA transfer between the GPIB and the Cache

For a DMA transfer between the 61PE10 and the Cache, these counters must be loaded initially with the one's complement of the number of bytes to be transferred (since the counters can only count up). When the counters reach maximum count, a Carry Out (CO-0) signal is generated, informing the DMA State Machine that the data transfer is complete. CO-0 is also sent to the Counter/Interrupt PAL, which generates an interrupt if the interrupt function is enabled.

For a DMA transfer between the GPIB and the Cache, the board must be in listener mode and the Byte Counters must be initially set to zero. As the DMA transfer progresses, the Byte Counters increment, keeping track of the number of transfers taking place. When the transfer is complete (as detected by the End-of-Message Byte Select), the 61PE10 can read the Byte Counters to determine how many transfers have taken place. If the counters reach maximum count, CO-0 is generated. This asserts NRFD-0 (stopping GPIB data transfers) and signals the Counter/Interrupt PAL to generate an interrupt if the interrupt function is enabled.

The 61PE10 clears the Byte Counters (and CO-0) by writing zeros into the counters. The data bus outputs for the counter chips are normally in tristate unless a read of the byte count is requested by the 61PE10. This prevents interference with the data bus.

Address Counters

The Address Counters (U1070 and U2070 on page 3 of the schematics) generate addresses for the Cache RAM during a data transfer. The 61PE10 can write to, but not read from, the Address Counters. A starting address is loaded into the counters and then is continually incremented as long as a data transfer is taking place. The generation of addresses terminates under the following conditions:

- When the Byte Counters indicate the end of a DMA transfer from the 61PE10
- When the end-of-message circuit detects the completion of a data transfer from the GPIB

STATUS AND CONTROL REGISTERS

The Status and Control registers consist of four Special registers: Board register, Type register, Diagnostic register, and Status buffer. The other Special registers (Cache RAM Mapping register, Byte Counters, Address Counters, and End-of-Message Byte Select) have their functions associated with other blocks in the block diagram and are discussed separately in other Functional Block explanations.

Details about the output signals for the registers discussed below can be found in the section Special registers.

Board register

The Board register (on page 1 of the schematics) is a write-only register that consists of a 74LS273 octal D-type flip-flop (U2100). This register accepts input from bus data lines BD0-BD7 and is loaded by a signal from the Load Selector. The outputs from the register are control lines that govern functions of the GPIB interface and DMA operations.

Type register

The Type register (on page 1 of the schematics) is a read-only register that consists of a 74LS244 line driver (U1100). This register contains a unique ID byte that identifies the High Speed GPIB option. The inputs to the driver chip are preconfigured to the number 01H. The register presents this number on bus data lines BD0-BD7 in response to a signal from the Dump Selector. When the GPIB is accessed by the 61PE10 during system initialization, the 61PE10 reads 01H, which identifies the High Speed GPIB board.

Diagnostic register

The Diagnostic register (on page 1 of the schematics) is a write-only register that consists of a 74LS373 transparent latch (U4050). The register accepts bus data lines BD9 and BD10 as inputs and is loaded by a signal from the Load Selector.

Status buffer

The Status buffer (on page 3 of the schematics) consists of a 74LS244 line driver (U1110) and a 74LS126 tristate buffer (U5070). The buffer accepts 11 status signals from other circuits as inputs and gates them onto data lines BD0-BD10. These inputs are presented to the 61PE10 on bus data lines BD0-BD10 by a signal from the Dump Selector.

DMA STATE MACHINE

The DMA State Machine (on page 2 of the schematics) generates timing and control signals for the following functions:

- Timing for on-board devices during a DMA transfer.
- Control for operations involving Cache RAM, TMS9914A, Byte Counters, and Address Counters.
- Access Arbitration

The DMA State Machine generates the following timing signals:

GA-0 — GA-0 controls the direction of the bidirectional buffer (U3060) in the Cache RAM circuit.

GC-0 — GC-0 controls the ACCGR-0 (Access Granted-0) input to the TMS9914A in the GPIB Controller Interface circuit.

GE-0 — GE-0 enables the bidirectional buffer (U3060) in the Cache RAM circuit.

GF-0 — GF-0 enables the address latches and data buffers that interface with the External Bus in the Bus Interface Logic.

The Access Arbitration feature of the DMA State Machine differentiates between the 61PE10 and the TMS9914A when both want the attention of the GPIB board at the same time. Normally, when either the 61PE10 or the TMS9914A want access to the GPIB board, the controller that makes the first request gains access. In the event that both request access at the same time, the Access Arbiter is programmed to give priority to the TMS9914A.

COUNTER/INTERRUPT PAL

The Counter/Interrupt PAL (U5040 on page 2 of the schematics) generates two sets of signals:

- An interrupt request signal to the 61PE10
- A set of clock and control signals that manage the Byte and Address Counters.

These signals are defined as follows:

IRQ-0 — IRQ-0 (Interrupt Request-0) is sent to the Bus Interface Logic. It is transmitted to the External Bus as BIRQ-0 (Bus Interrupt Request-0).

BI-1, BI-0 — BI-1 and BI-0 (Byte Counter Function Selects) manipulate the Function Select inputs (labled I0 and I1) on the counter chips in the Byte Counter circuit. This distinguishes which mode of operation the counter chips use during a transfer. Refer to the data sheet for the counter chips for further information.

AI-1, AI-0 — AI-1 and AI-0 (Address Counter Function Selects) manipulate the Function Select inputs (labled I0 and I1) on the counter chips in the Address Counter circuit. This distinguishes which mode of operation the counter chips use during a transfer. Refer to the data sheet for the counter chips for further information.

CPBC-1 — CPBC-1 (Clock Pulse Byte Counter-1) provides the clock pulse for the Byte Counters.

CPAC-1 — CPAC-1 (Clock Pulse Address Counter-1) provides the clock pulse for the Address Counters.

ACOE-0 — ACOE-0 (Address Counter Output Enable-0) enables the Address Counters.

CONTROL PAL

The Control PAL (U4070 on page 2 of the schematics) governs a variety of timing and control operations. These operations include:

- Decoding LA1-LA3 (control of Load and Dump Selectors)
- Controlling the direction of the data buffers on the Bus Interface Logic circuit
- Providing input (timing and control signals) to the GPIB and Cache RAM MUX circuit
- Generating a clock signal to the EOM detect circuit

CACHE RAM LOGIC

The Cache RAM Logic block performs those functions directly relating to the Cache RAM. These functions include the Cache RAM itself, plus the generation of control signals for the Cache RAM, and the mapping function for the Cache RAM. These functions are described in the following paragraphs.

Cache RAM

The Cache RAM (on page 3 of the schematics) functions as a local buffer during data transfers between the GPIB and 61PE10. It remains disabled during and after power-up and becomes enabled by writing into the Cache RAM Mapping register. The major components are two 8-bit static CMOS RAMs (U1050, U2050). Since the 61PE10 operates with a 16-bit data bus and the GPIB uses an 8-bit data bus, a method of data transfer was needed that was compatible with both. The Cache RAM accomplishes this in the following way:

- The two 8-bit static RAMs are connected in tandem for the 61PE10 data bus. This provides a destination for all 16 data lines (BD0-BD15) and appears to the 61PE10 as a memory space that is 16 bits wide and 8 kwords deep.
- The higher-order byte of the 16-bit data bus (BD8-BD15) is connected to an 8-bit bidirectional buffer (U3060). One side of the bidirectional buffer is connected to BD8-BD15 (the high order byte); the other side of the buffer is connected to BD0-BD7 (the low order byte). This arrangement allows for information on BD8-BD15 to be transferred to BD0-BD7 and vice versa. When a data transfer occurs with the GPIB, control circuits on the board enable the RAMs one at a time, each one appearing on data bits BD0-BD7. Thus, the Cache RAM appears to the GPIB as a memory space that is 8 bits wide and 16 kbytes deep.

With this arrangement, the 61PE10 reads from and writes to the Cache RAM perceiving it as 16-bit data words. The TMS9914A, on the other hand, reads from and writes to the Cache RAM perceiving it as 8-bit data bytes.

GPIB and Cache RAM MUX

The GPIB and Cache RAM MUX (on page 2 on the schematics) generates timing and control signals for both the GPIB Interface and the Cache RAM. (Most of the signals involved pertain to the Cache RAM, so this circuit was placed in the Cache RAM block and not in the GPIB block.) The signals for the Cache RAM and GPIB are described in the following text.

CS1 EVEN-0, CS2 ODD-1, CS1 ODD-0, CS2 EVEN-1
: These Chip Selects manipulate the static RAMs in the Cache RAM block.

OE RAM-0
: OE RAM-0 (Output Enable, RAM-0) enables the outputs for the static RAMs in the Cache RAM block.

DBIN-1
: DBIN-1 (Data Bus Input-1) enables the TMS9941A GPIB Controller chip to receive data.

CS TMS-0
: CS TMS-0 (Chip Select, TMS9914A-0) is a chip select for the TMS9914A GPIB Controller chip.

WE TMS-0
: WE TMS-0 (Write Enable, TMS9914A-0) indicates to the TMS9914A GPIB Controller chip that data is being written to one of its registers.

WE RAM-0 WE RAM-0 (Write Enable, RAM-0) enables the Cache RAM memory chips to accept data when written to.

Cache RAM Mapping register

The Cache RAM Mapping register (U1010 on page 4 on the schematics) performs two functions for the GPIB board:

- Locating the Cache RAM within the 61PE10 address space.
- Enabling and disabling of the Cache RAM.

The Mapping register has a set of inputs connected to data bus lines BD0-BD7. From these data lines, the comparator chip loads an 8-bit data byte, which is compared to address lines A16-A23. This comparison is called the *mapping function.* The mapping function is selected by writing a 1 into data bit BD15. Once selected, the comparator chip monitors A16-23. When A16-23 matches the latched data byte, the M RAM SEL-1 signal is generated by the register and sent to the Control PAL, which enables the Cache RAM.

Fig. 5-4 illustrates how the Cache is mapped into the 61PE10 address space. The NS16032 microprocessor has a 24-bit address bus. This allows for a 16 Mbyte address space. The upper 8 bits (A16-A23) divide this 16 Mbytes into 64 kbyte blocks. The Cache Mapping register monitors these 8 address lines and can place the Cache in any one of these 64 kbyte blocks.

A 16 kbyte Cache RAM can have four possible locations within a 64 kbyte block of address space. Once a 64 kbyte block is selected, the Cache RAM is then mapped inside this block in the following way:

- Address line 15 (LA15) is an enable line for the Mapping register and must be 0 for the mapping function to operate. This places the 16 kbyte Cache RAM in the lower half of the 64 kbyte block.
- The addresses for the 16 kbyte Cache RAM range from 0000 to 3FFF. Starting at 0000 places the Cache RAM at the bottom of the 64 kbyte block. The remaining portion of the 64 kbyte block is unused.

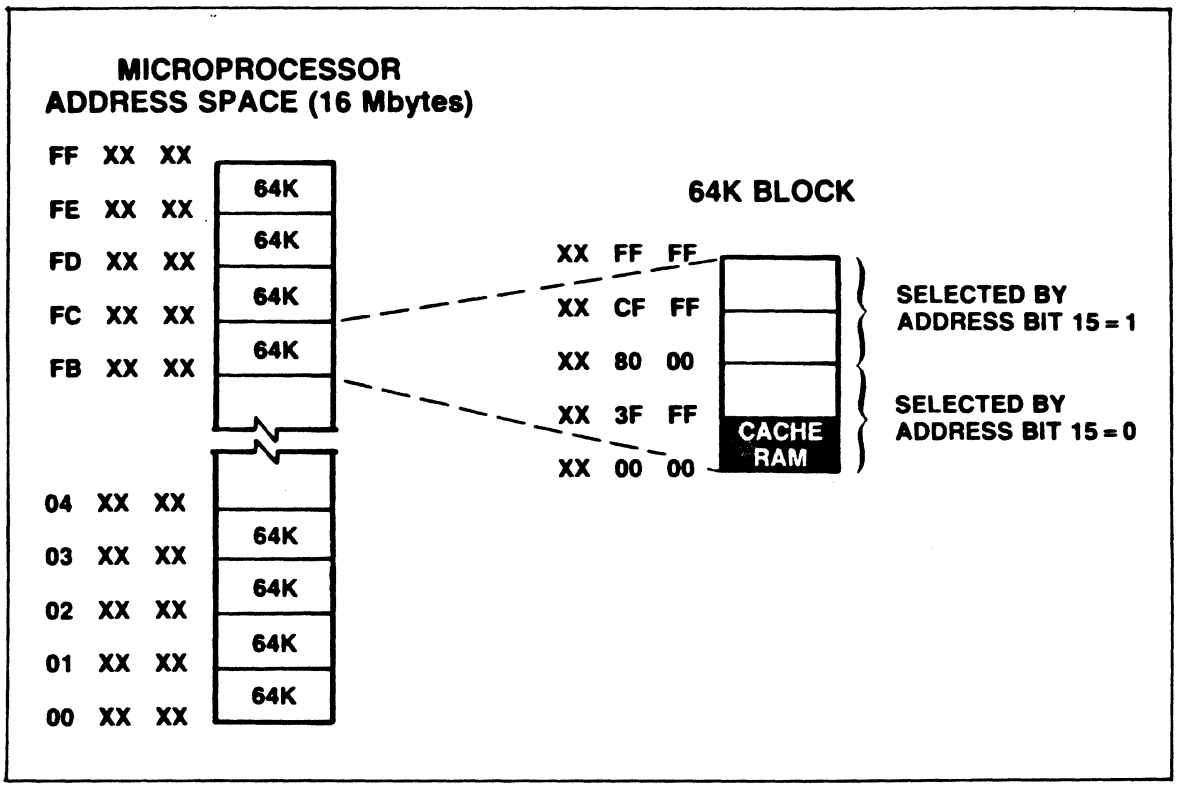


Figure 5-4. Cache RAM Address Map.

GPIB INTERFACE

The GPIB Interface block manages the actual GPIB operations. This includes control of the GPIB itself (which primarily means the operation of the TMS9914A GPIB controller chip), and the End-of-Message detection. These functions are described in the following paragraphs.

GPIB Controller Interface

The GPIB Controller Interface (on page 4 of the schematics) governs the operation of the GPIB bus, including all control and handshake signals associated with the GPIB.

The major component of the circuit is the TMS9914A GPIB controller chip. This special purpose programmable component provides all data and control lines needed to carry out GPIB operations. The chip accepts data on lines BD0-BD7. It also uses Latched Address lines LA1-LA3 for its register Select function. The chip handles all data and control functions associated with GPIB operations. Refer to the data sheet for the TMS9914A for more information.

End-of-Message Byte Select

End-of-Message Byte Select (on page 4 of the schematics) generates an interrupt and shuts down GPIB data transfers when an end-of-message character is detected on the GPIB bus. This action occurs only when the board is in listener mode.

Normally, GPIB has a control line designated for use in end-of-message detection (the EOI, or End Or Identify line). The EOI line is asserted along with the last data byte in the transfer and the receiving circuitry detects this and recognizes that the data transmission is complete. Another method for end-of-message detection is End-of-Message Byte Select. With this method, an 8-bit code (usually an ASCII code, but not necessarily) is latched into a register and compared to the incoming data. When an incoming byte matches the previously latched code, an end-of-message signal is generated and NRFD-0 is asserted. The High Speed GPIB is able to use either of these methods. However, this circuit is designed to implement the End-of-Message Byte Select system.

The comparator chip in the End-of-Message Byte Select (U2080) has one set of inputs connected to data bus lines BD0-BD7. The chip latches the 8-bit character that designates the end-of-message. Since all eight bits are used, the state of the parity bit (bit 7) of an ASCII character used for end-of-message detection must be known so that the correct state is written into the End-of-Message register. Also, since data on the GPIB bus is low true data, and data on the rest of the board is high true data, the 8-bit character latched into the register must be the one's complement of the actual end-of-message character.

The comparator chip has another set of inputs connected to the GPIB data lines. When the GPIB is functioning in listener mode, the register chip monitors the GPIB data bus, watching for the predetermined end-of-message byte (the End-of-Message Byte Select is disabled when the GPIB is functioning as a talker or a controller). When the byte is recognized, the comparator chip sends an interrupt request signal to the Counter/Interrupt PAL and asserts the NRFD-0 signal to the GPIB bus. The NRFD-0 signal stops data transfer operations on the GPIB bus. NRFD-0 is cleared by the CNRFD-0 bit from the Board register.

The GPIB board has diagnostic support for the End-of-Message Byte Select. First, an end-of-message character is written into the comparator chip from the bus data lines. Then, by using the Diagnostic register, the TMS9914A can be forced to output the same end-of-message character. If End-of-Message Byte Select is functioning properly, the comparator chip

matches the two data bytes and generates the DBM-1 signal, which then can be read by the 61PE10 through the Status register.

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6100 Series

COMPUTER BOARD

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Theory of Operation 6

INTRODUCTION

This section discusses the theory of operation of the 6100 Series Computer Board. The contents of this section are organized as follows:

- Introduction
- System Memory Map and Software Interface
- Functional Block Description

COMPUTER BOARD OVERVIEW

The 6100 Series computer board is a NS32016-based processor board that provides the primary computer resource for the 6100 Series of workstations. The computer board consists of the system processor, main memory, base I/O interfaces (such as dual RS-232-C and GPIB), Winchester and flexible diskette interfaces and internal bus structures.

SYSTEM MEMORY MAP AND SOFTWARE INTERFACE

This section describes the allocation and use of the system address space. Included are system memory maps, system status and control registers, and I/O device status and control registers. Also discussed are general system functions and I/O considerations.

GENERAL SYSTEM ADDRESS SPACE

The system memory map includes areas reserved to support kernel functions, system memory, computer-board resident I/O, and expansion I/O.

Table 6-1 shows the general system memory map.

Table 6-1
GENERAL SYSTEM MEMORY MAP

Address Range	Allocation	Purpose
FF FFFF to FF 0000	64 kbytes	Computer board-based I/O
FE FFFF to FE 0000	64 kbytes	Expansion-based I/O
FD FFFF to 82 0000		External bus
81 FFFF to 80 0000	128 kbytes	Computer board ROM (a)
7F FFFF to 30 0000	5 Mbytes	External bus
2F FFFF to 0C 0000	2.25 Mbytes	Main memory (b)
0B FFFF to 00 0000	768 kbytes	Main memory (c)

(a) Computer board ROM appears at 00 0000 at system reset and power-up.
(b) Systems using 256-kbit chips use 3 megabytes total main memory space.
(c) Systems using 64k-bit chips use 768 kbyte total main memory space.

Addresses for the computer board-based I/O, system ROM, and system RAM do not access the External bus. Additionally, the display processor and expansion I/O devices cannot be mapped to these locations.

System ROM

System ROM consists of a minimum of 32 kbytes of EPROM, provided by two 16k × 8-bit chips. System ROM can be increased to 64 kbytes using four 16-kbytes parts, or 128 kbytes using four 32-kbyte parts. ROM is arranged in two equal banks. The starting address for each bank is fixed. Bank 0 begins at 80 0000 (hex) and bank 1 begins at 81 0000 (hex).

During power-up and also during a system reset, the CPU begins executing at address location 00 0000. Since system RAM starts at address 00 0000, a method was devised to allow the CPU to execute initialization ROM out of address location 00 0000. During a system reset, the initialization ROM is mapped to address 00 0000 and the system RAM is disabled. After the initialization ROM has been executed, the RAM Enable bit in the System Control register is set, which effectively removes the initialization ROM from lowest memory and enables the system RAM. ROM is always present from 80 0000 to 81 FFFF.

The upper 256 bytes of ROM bank 0 (address 80 FF00 - 80 FFFF) are also addressed at the top of memory (FF FF00 - FF FFFF) to initialize the LAN interface during boot. Although all 256 bytes of ROM are mapped to the top of memory, only the highest 10 bytes (address 80 FFF6 - 80 FFFF) are actually used. The remaining 246 bytes are not reserved and are available for normal boot code.

System RAM

Using 64-kbit parts allows 256 kbytes of RAM on the computer board, while 256-kbit parts provides a full megabyte of RAM. Additional main memory is available on the 61MP01, 61MP02, and 61MP03 Expansion Memory boards. The system can have as

much as 3 megabytes of main memory.

Parity Generation and Checking

The memory support logic provides parity generation and checking. Parity generation and checking is controlled by various bits in the System Status register (SSR), the System Control register (SCR), and the Parity Error register (PER).

Parity logic is enabled by setting the Parity Enable (PARE) in the SCR. Parity is generated and checked for the high and low bytes individually. Parity is generated during a memory-write and checked again during a read. If bad parity is detected during a read, the address of the bad location is stored in a Parity Error register, including a bit indicating the high or low byte. If enabled, a nonmaskable interrupt (NMI) is generated to the CPU as a result of the parity error. If the NMI is not enabled, the parity error (PERR) signal is still generated but the NMI does not occur. PERR is cleared by clearing the PARE bit in the SCR.

The parity generation and checking logic is tested by setting the Parity Bad (PARB) bit in the SCR. This feature forces the generation of bad (even) parity during a memory write. When the same location is read, the bad parity bit is detected and PERR is generated.

SYSTEM I/O

This section discusses the system I/O interfaces, including the system control and status registers, devices registers, and interfaces.

Computer Board I/O Memory Map

The memory map in Table 6-2 provides the address locations for the hardware registers and I/O space for the standard I/O devices. The computer board I/O memory map extends from FF 0000 to FF FFFF.

Table 6-2
COMPUTER BOARD I/O MEMORY MAP

Address Range	Amount	Purpose
FF FFFF to FF FF00	256 bytes	Ethernet Boot/ID ROM
FF FEFF to FF FE00	256 bytes	Interrupt Control Unit
FF FDFF to FF FD00	256 bytes	Disk DMA Controller
FF FCFF to FF FC00	256 bytes	Flexible Disk Interface
FF FBFF to FF FB00	256 bytes	ST-506 Interface
FF FAFF to FF FA00	256 bytes	RS-232-C Controller
FF F9FF to FF F900	256 bytes	GPIB Controller
FF F8FF to FF F800	256 bytes	Time-of-Day Clock
FF F7FF to FF F010		Register ghosts
FF F01F to FF F00E		System Status register (SSR)
FF F00D to FF F00C		System Control register (SCR)
FF F00B to FF F00A		Parity Status register
FF F009 to FF F008		Configuration switch register and display
FF F007 to FF F006		Power-down register
FF F005 to FF F004		LAN Channel Attention (CA) register
FF F003 to FF F002		GPIB Control register
FF F001 to FF F000		Flexible Control register
FF EFFF to FF 8000		Nonvolatile memory ghosts
FF 7FFF to FF 0000	4 kbytes	Hard disk data cache (a)

(a) An access to any location within this block reads the current 16-bit word.

Interrupt Control

The interrupt circuitry uses the NS32202 Interrupt Control Unit (ICU). The ICU provides 16 interrupt channels that are prioritized individually. Six of the interrupt channels are assigned to the backplane and one is assigned to the display processor. The remaining channels are assigned to the I/O devices on the computer board. The interrupt channels are assigned as shown in Table 6-3.

Table 6-3
INTERRUPT PRIORITY ASSIGNMENTS

Interrupt Channel	Active State	Device
0		MMU configuration link
1	Low	RS-232-C interface
2	Low	Hard disk interface
3	Low	Display system
4	Low	Backplane slot 1
5	Low	Backplane slot 2
6	Low	Backplane slot 3
7	Low	Backplane slot 4
8	Low	Backplane slot 5
9	Low	Backplane slot 6
10	Low	GPIB
11	High	Loca Area Network
12	High	Power switch interrupt
13	High	Flexible disk interface
14		FPU configuration link
15		Software interrupt 0

Bus Arbitration

Bus arbitration is performed between expansion boards capable of DMA, the flexible disk DMA controller, the LAN, and the CPU. Arbitration is performed according to the DMA priority given in Table 6-4.

Table 6-4
DMA PRIORITY ASSIGNMENTS

Channel	Device
7	CPU
8	Slot 6
9	Slot 5
A	Slot 4
B	Slot 3
C	Slot 2
D	Slot 1
E	LAN
F	Flexible disk

System Registers

The System Control register (SCR) and the System Status register (SSR) each contain various control and status bits that are used to regulate the External bus (which is the medium for backplane expansion) as well as various other system and I/O functions. The External bus is discussed in this section under System Bus

Structures and in further detail in the *System Enclosure Service Manual.*

System Control Register

The SCR is a read/write register located at address FF F00C. This register is cleared after system reset and power-up, and contains many device and logic-enable bits that must be set after power-up. A diagram of the register is provided in Figure 6-1.

07	06	05	04	03	02	01	00
PARE	PARB	DMAE	BERRE	LLOP	NMIE	Not Used	RAME

Figure 6-1. System Control Register.

PARE — When set, the Parity Enable bit enables parity checking and the generation of a Nonmaskable Interrupt (NMI) by the parity-checking logic. A NMI is generated if the NMI Enable bit is set and a parity error occurs. The parity error signal can be generated without an NMI if PARE is set and NMIE is clear. Parity generation and checking is discussed earlier in this section.

PARB — The Parity Bad bit is set to force the generation of bad parity. This feature allows the checking of the parity-checking logic.

DMAE — The DMA Enable bit is set to allow devices other than the CPU (such as the LAN controller, disk controller, and external DMA devices) to gain mastership of the External bus.

BERRE — The Bus Error Enable bit is set to allow the generation of the Bus Error signal and NMI, as the result of a bus time-out.

LLOP — The LAN Loopback bit is set to take the LAN interface out of loop-back mode. The LAN starts in loop-back mode to minimize network disturbances and allow diagnostics to run.

NMIE — The Nonmaskable Interrupt Enable bit is set to allow NMIs to be sent to the CPU. When this bit is clear, NMI-0 is forced high.

RAME — When set, the RAM Enable bit enables system RAM. This bit is clear during power-up and system reset, which temporarily places the system ROM restart code at the bottom of the address range, allowing the restart to be run from address 0. After restart, the restart code is returned to address 80 0000 (hex) and the RAME bit is set, thus enabling system RAM.

System Status Register

The System Status register (SSR) is a read-only register located at address FF F00E. A diagram of the register is in Figure 6-2.

07	06	05	04	03-00
PERR	PFAIL	PWRSW	BERR	DMACH

Figure 6-2. System Status Register.

PERR — The Parity Error bit is set when the parity checking logic detects a parity error. The parity checking logic is enabled when the Parity Enable (PARE) bit is set in the SCR. The occurrence of PERR also results in the generation of an NMI to the CPU. PERR and NMI are both reset when PARE is cleared. PARE must be set again to enable the parity checking logic.

PFAIL — The Power Fail bit is set by the power supply during a power failure. This bit generates a NMI to the CPU. System power is stable for approximately 20 milliseconds after the NMI is asserted.

PWRSW — The Power Switch bit is asserted low when the start/stop switch on the front panel of the chassis is closed, which turns on the power supply. This bit is deasserted at the front panel to power down the system. This generates an interrupt to the ICU but does not turn the power supply off until the PON-1 bit in the Nonvolatile Memory register is deasserted (low). When PON-1 is cleared (low) by software, the system is powered down.

BERR — The Bus Error bit is set in response to a bus transfer time-out. The time-out also results in the generation of a NMI to the CPU. BERR is cleared by clearing the BERRE bit in the SCR.

DMACH — The DMA Channel bits 03-00 contain a 4-bit binary code that defines the most recently used DMA channel. The code is used after a bus time-out to identify which channel was active when the time-out occurred. The correspondence between the 4-bit code and the associated bus devices is given in Table 6-5. Code values 1-6 are not used.

Table 6-5
DMA CHANNEL CODE

DMACH Code	Hex Value	Bus Device
0000	0	None (reset)
0111	7	CPU
1000	8	Slot 6
1001	9	Slot 5
1010	A	Slot 4
1011	B	Slot 3
1100	C	Slot 2
1101	D	Slot 1
1110	E	LAN
1111	F	Flexible disk

Parity Error Register

The Parity Error register is a 16-bit read-only register that stores parity error information. This register is located at address FF F00A and is cleared when PARE is set in the SCR. The register is represented by Figure 6-3.

15	14	13-00
HIERR	LOERR	PARADR

Figure 6-3. Parity Error Register.

HIERR — The High Error bit is set by the parity-checking logic to indicate that the current parity error occurred on the high byte (bits 08-15) of the 16-bit word.

LOERR — The Low Error bit is used in the same manner as HIERR, but on the low byte. LOERR is set by the parity checking logic to indicate that the current parity error occurred on the low byte (bits 00-07) of the 16-bit word.

PARADR — The Parity Address bits are bits 13-00 of the register, which correspond to address bits A22-A9 of the Internal Address bus (the IA bus is defined in this section under Functional Block Description. After a parity error has been detected, the PARADR bits contain the address of the memory location associated with the parity error. This information is used with HIERR and LOERR to determine the location of the faulty memory address. Parity errors occurring on expansion memory boards are always reported as high-byte parity errors to the computer board.

Configuration Input/Display

The Configuration switch is an 8-switch DIP located on the computer board. The Diagnostic LED is a seven-segment LED display. The Configuration switch and display are accessed at the back of the system cabinet, as shown in Figure 6-4. Switches numbered 1-8 correspond to Address/Data lines AD07-AD00 respectively. The contents (setting) of the switches are read from address FF F008. Diagnostics information is displayed by a write to the same address. The LED register drives a seven-segment display located on the computer board. Bits AD00-AD06 of the bus drive segments A-G respectively. Bit AD07 drives the decimal point.

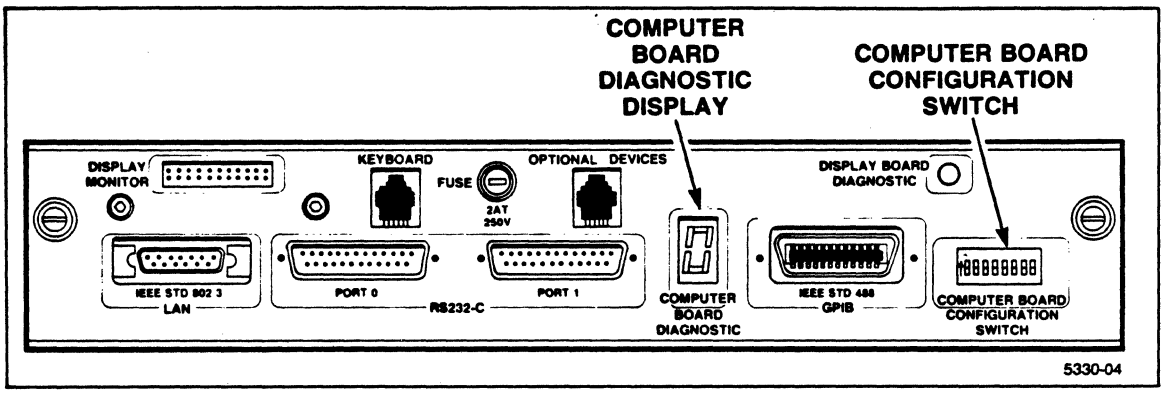


Figure 6-4. Computer Board Configuration Switch and Diagnostic Display.

CAUTION

Never change the settings of the configuration switches while the workstation is on. Always turn it off and unplug the power cord first.

Switch 1

The power-up firmware stored in ROM has two major modes of operation: service mode and power-up mode. The mode of operation is selected by configuration switch 1. Placing the switch in the up position selects normal mode. Placing the switch in the down position selects service mode. If switch 1 is set to normal mode, switches 2-8 select certain parameters that pertain to normal system operation. If switch 1 is set to service mode, switches 2-8 select diagnostic tests used to locate system hardware faults.

The remaining switch functions are defined for normal mode. These switches are defined for service mode in the *6100 Series Diagnostics* manual.

Switches 2 and 3

These switches select the console and baud rate. The console is the device that displays system messages. Table 6-6 shows the four switch combinations for selecting the appropriate console and baud rate.

Table 6-6
SELECTING THE CONSOLE DEVICE

Console Device	Switch 2	Switch 3
Display (Option 27/28)	up	up
9600 baud RS-232-C terminal (port 0)	up	down
1200 baud RS-232-C modem/terminal (port 1)	down	up
300 baud modem/terminal (port 1)	down	down

Switch 4

Determines whether the workstation boots from UTek (up), or from a file that you specify (down). Switch 4 should be set to boot from UTek (up).

Switches 5, 6

Select the device called the *boot device*, the device that the workstation loads the operating system from. Possible boot devices are:

- Diskette
- Internal hard disk
- Local Area Network (LAN)

Table 6-7 shows how to set Switches 5 and 6 to select the boot device.

Table 6-7
SELECTING THE BOOT DEVICE

Boot Device	Switch 5	Switch 6
Autoboot	up	up
Hard disk	up	down
Diskette drive	down	up
LAN port	down	down

If you select *autoboot*, the workstation searches for a device from which to boot UTek. The workstation tries to boot from (in order): the diskette drive, the hard disk, and the Local Area Network (LAN).

Switches 7, 8

Reserved for use with the Diagnostics operating system. See the *6100 Series Diagnostics* manual. These two switches should always be up during normal

system operation.

Power Control

The supply of power to the system is controlled by software. System power is first applied to the system by pressing the start/stop switch at the front panel. Power is then maintained as long as the PON bit in the Nonvolatile Memory register is set or the start/stop switch is closed. A sanity timer gives complete control of system power to the start/stop switch in the event of a system crash.

Nonvolatile Memory Register

This 8-bit register controls the characteristics of nonvolatile memory. Bits 07-04 are not used. The register, located at address FF 0000, is shown in Figure 6-5.

D07, D06	D05	D04	D03	D02	D01	D00
Not Used	PON	LED	CS 1	CS 0	SK	NDAT

Figure 6-5. Nonvolatile Memory Register.

PON — This write-only bit is set by software to maintain system power. During a power-down, system power is maintained until this bit is cleared by software.

LED — This bit is set by software to light the power-on indicator on the start/stop switch. This bit is cleared by software.

CS 1 — Nonvolatile memory consists of two 256-bit serial access EEPROMs. The Chip Select 1 bit, when set, enables the memory chip designated as number 1.

CS 0 — Nonvolatile memory consists of two 256-bit serial access EEPROMs. The Chip Select 0 bit, when set, enables the memory chip designated as number 0.

SK — The Serial Clock is a positive-edge clock that is used to clock serial data into or out of the chip. The nonvolatile memory register must be loaded and clocked for each bit being read into or out of memory.

NDAT — Nonvolatile memory data is the serial data bit that is read or written during a nonvolatile memory access.

Flexible Disk Interface

The flexible disk interface is based on the WD 1770 disk controller and supports up to two flexible disk drives. The interface is an open-collector interface that is compatible with most 5 1/4-inch disk drives. DMA control is provided by the AMD

9516 disk DMA controller. Channel 2 of the DMA controller is assigned to the flexible disk interface. The DMA channel associated with the flexible disk drive must be set for flyby, byte-mode operation. Refer to the AMD 9516 data manual for specific DMA programming information.

The flexible disk control register is a 8-bit write-only register located at address FF F000. This register controls the selection of the drive, media side, and density. The register is represented by Figure 6-6.

D07-D04	D03	D02	D01	D00
Not Used	FDEN	DDEN	SIDE	DRIVE

Figure 6-6. Flexible Disk Control Register.

FDEN — The Flexible Disk Enable is set (high) to enable the drive and cleared (low) to disable the drive.

DDEN — The Double Density bit is cleared (low) to indicate double density storage. If this bit is set (high), single density format is used.

SIDE — This bit is used to select the side of the disk for the data transfer.

DRIVE — This bit selects which drive the impending transfer applies to. Clearing this bit selects the drive on the left side (drive 00). Setting this bit selects the drive on the right side (drive 01).

Bits 04-07 of this register are not used.

The registers used by the WD1770 controller are located at the addresses given in Table 6-8.

Table 6-8
FLEXIBLE DISK CONTROLLER REGISTER ADDRESSES

Controller Register	Address
Command/Status	FF FC00
Track	FF FC02
Sector	FF FC04
Data	FF FC06

Hard Disk Interface

The hard disk interface is based around the WD2010 Hard Disk Controller. The interface includes a dedicated data buffer and Hard Disk Control register. The disk data buffer is 4 kbytes in size and appears to the CPU as a 2 kword (16-bits) sequential-access buffer. This is an open-collector TTL interface that is ST-506-compatible and supports one hard (Winchester) disk drive (drive 0). Electrical

interface information is discussed in the Functional Block Description in this section.

The disk data buffer is a single-port buffer that can only be accessed by the CPU or the controller at any given time. There is no DMA associated with hard disk data transfer, meaning that data transfers to or from hard disk via the data buffer are executed by the CPU. The Am9516 DMA Controller is not used by this interface.

The disk data buffer serves as a serial transfer buffer between the CPU and the hard disk controller. The buffer and associated logic also serve as a data assembler/disassembler in that data is transferred between the CPU and the data buffer in 16-bit words, whereas data is transferred between the controller and the data buffer in 8-bit bytes.

A data write to the disk requires that the CPU set the address counter to zero (0) prior to loading the buffer. This is accomplished by clearing the Manual Clear (MNCLR) bit in the Hard Disk Control register. Additionally, the controller must be alerted when the data buffer is full and can be read. Currently, the CPU informs the controller by setting the MNRDY (Manual Ready) bit in the Hard Disk Control register. The controller then proceeds to read the contents of the buffer. Additional information concerning the operation of the controller can be found in the WD1010 controller data manual.

The Hard Disk Control register is an 8-bit register located at address FF FB10 and is shown in Figure 6-7.

D07	D06	D05	D04	D03	D02	D01	D00
BCCLR	BFRDY	MULT	DRSEL	HDSEL4	HDSEL2	HDSEL1	HDSEL0

Figure 6-7. Hard Disk Control Register.

BCCLR — Buffer Counter Clear is cleared by the host to reset the data buffer address counter. The host then sets this bit again after a clear for the counter to advance during a data transfer. This bit is cleared during power-up and is set by the CPU before the data buffer is used (and a hard disk data transfer executed).

BFRDY — Buffer Ready is set by the CPU to inform the disk controller that the data buffer is full or empty and may be accessed by the controller.

MULT — Multiple is set by the CPU to allow multiple-sector operations to be performed. Single-sector operations are performed when this bit is clear (0).

DRSEL — This bit is set to select the drive. Although only one hard disk drive is supported, this bit must be set prior to a hard disk access.

HDSELn — The Head Select bits (HDSEL4, 2, 1, 0) constitute a 4-bit binary code that identifies the disk drive read/write head or disk surface that the disk access applies to. HDSEL0 is the least significant bit.

When accessing the data buffer, address lines A00-A14 are not sampled to allow for string-move operations. Disk controller registers are mapped on word boundries from FF FB00 to FFFF FB0E, as shown in Table 6-9. Refer to the WD1010 disk controller manual for bit assignments.

Table 6-9
HARD DISK CONTROLLER REGISTER ADDRESSES

Register	Address
Disk Data Buffer	FF 0000- FF 7FFF
Unused	FF FB00
Error Flags/Write Precomp Cylinder	FF FB02
Sector Count	FF FB04
Sector Number	FF FB06
Cylinder Low	FF FB08
Cylinder High	FF FB0A
SDH Register	FF FB0C
Status/Command Register	FF FB0D
Hard Disk Control Register	FF FB10

Dual RS-232-C Interface

The two serial interface ports are based on the AMD 8530 Serial Communications Controller. A data clock is provided to allow baud rates of up to 19.2 kbaud with less than 0.3% error. The interface is configured as an asynchronous DCE. Software control is provided for pins 8 (CD) and 6 (CTS). Sensing is provided for pins 4 (RTS) and 20 (DTR). Connector pin assignments and logic levels are provided in Section 2 Specifications of this document. Associated with each channel is a serial data and channel clock register and a channel Status and Control register. The address for each register is given in Table 6-10.

Table 6-10
DUAL RS-232-C INTERFACE REGISTER ADDRESSES

Register	Address
Channel A Data	FF FA06
Channel A Status/Control	FF FA04
Channel B Data	FF FA02
Channel B Status/Control	FF FA00

The AMD 8530 Serial Communications Controller cannot be accessed by successive

read or write operations. Idle time must be provided by software between successive accesses to the controller. Table 6-11 shows the time required after the given access has been completed before the next read or write access can be performed. Idle time is specified in timing states (T states) or memory cycles.

Table 6-11
SUCCESSIVE-ACCESS IDLE-TIME REQUIREMENTS

Operation	Idle Time Required
Read	
With MMU	11 T states (2 memory cycles)
Without MMU	12 T states (3 memory cycles)
Write	
With MMU	9 T states (2 memory cycles)
Without MMU	10 T states (2 memory cycles)

Refer to the controller data manual for additional information.

LAN Interface

The LAN interface is based around the 82586 LAN Controller. The Channel Attention line is used to initiate transfer operations over the LAN. To execute data transfer over the LAN, the host places command information and data into a command block. The block is placed in main memory and pointed to by command information previously loaded into the controller. Once the command block has been placed in memory, the LAN Channel Attention (CA) control signal is toggled by writing to the appropriate system control decoder. The LAN controller then copies the contents of the command block and executes the command. Most operations with the LAN are performed with the LAN directly accessing system memory.

The LAN Loopback (LLOP) bit in the System Control register is used to enable loopback testing. Clearing the bit asserts the loopback pin on the 82501 data separator, thereby enabling loopback testing. Since the LAN interacts with the system as a DMA device, the DMA Enable (DMAE) in the System Control register must be set before the LAN interface can operate.

The LAN interface can only address the lowest three megabytes of physical memory. Memory addresses generated by the interface in the 3 to 4 megabyte range of physical memory access the top 1 megabyte of the physical address range. Table 6-12 shows the mapping of addresses generated by the LAN.

Table 6-12
LAN ADDRESS MAPPING

LAN Memory Adress	Physical Address
00 0000	00 0000
2F FFFF	2F FFFF
30 0000	F0 0000
3F FFFF	FF FFFF

GPIB Interface

The GPIB interface is based on the TMS 9914 GPIB Controller. The interface supports talker, listener, and controller functions. Address information is set and read by software from within the system and saved in nonvolatile memory. Because there is no DMA support of the GPIB, the transfer rate is limited by the speed of the programmed data transfer. There is no End-of-Message (EOM) character detection associated with this interface. System control of the GPIB interface is provided by the GPIB Control register. This 8-bit write-only register is located at address FFF002. The GPIB line drivers are disabled by a system reset (power-up) and must be enabled by setting the GPIB Enable bit in the GPIB Control register. The control register is represented by Figure 6-8.

D07-D02	D01	D00
Not Used	SYSCTL	Not Used

Figure 6-8. GPIB Control Register.

SYSCTL The System Control bit, if cleared, relinquishes control of the GPIB to other devices. If the SYSCTL bit is set, the TMS 9914 interface controller becomes bus controller, allowing the TMS 9914 to drive the REN and IFC signals on the bus.

Communication between the controller and the host is performed via 13 memory-mapped registers. Three select lines address one of eight possible locations, each of which contains one read and/or one write register. Register selection within the addressed location is provided as a function of the operation, read or write. The 13 controller registers are memory-mapped as indicated below. Note that there are eight addressable locations and that the specific register is determined by the operation. A read operation does not select the same register as a write operation, even if the registers share the same address. The registers are numbered below in Table 6-13 for convenience. Refer to the TMS 9914 data manual for register definition and layout.

Table 6-13
GPIB CONTROLLER STATUS AND CONTROL REGISTERS

Address	Read Register	Reg No.
FF FC00	Interrupt Status reg.	0
FF FC02	Interrupt Status reg.	1
FF FC04	Address Status reg.	3
FF FC06	Bus Status reg.	4
FF FC08	Not Used	
FF FC0A	Not Used	
FF FC0C	Cmnd. Pass Through reg.	5
FF FC0E	Data In reg.	6

GPIB Function Subsets

The hardware design supports complete compatibility with all GPIB functions. Portions of various functions are implemented in software. However, the software release present in your system may not support all functions. The hardware design supports the subsets given in Table 6-14.

Table 6-14
GPIB FUNCTION SUBSETS

Function	Subset	Description
SH	SH1	Complete capability
AH	AH1	Complete capability
T	T5, TE5	Complete capability
L	L5, LE5	Complete capability
SR	SR1	Complete capability
RL	RL1	Complete capability
PP	PP1	Remote configuration
DC	DC1	Complete capability
DT	DT1	Complete capability
C	C1	System controller
	C2	Send IFC and take charge
	C3	Send REN
	C4	Respond to SRQ
	C5	Send IF Message, receive control, pass control, pass control to self, parallel poll, take control synchronously

Backplane Memory Allocation

Each backplane slot has a 2-kbyte memory space reserved for the device hardware registers. The starting address for each slot is a function of the slot number, as indicated in Table 6-15. A total of six slots are available for expansion.

Table 6-15
BACKPLANE SLOT MEMORY MAP

Address Range	Allocation	Purpose
FE 3FFF to FE 3800	2 kbytes	Reserved for display system
FE 37FF to FE 3000	2 kbytes	Slot 6
FE 2FFF to FE 2800	2 kbytes	Slot 5
FE 27FF to FE 2000	2 kbytes	Slot 4
FE 1FFF to FE 1800	2 kbytes	Slot 3
FE 17FF to FE 1000	2 kbytes	Slot 2
FE 0FFF to FE 0800	2 kbytes	Slot 1
FE 07FF to FE 0000	2 kbytes	Not available

Of the 2 kbytes of memory reserved for each expansion board, the first byte of each 2-kbyte block contains a board identifier (ID) byte that is unique to each board type. This serves to identify the circuit board type. The remaining address locations within the 2-kbyte block are used to access various addresses relative to the given expansion board.

FUNCTIONAL BLOCK DESCRIPTION

The computer board is divided into several major functional circuit areas or blocks, with each block performing a general function. This section identifies and discusses the operation of each functional block. The bus structures that tie the major functional blocks together are discussed first.

Figure 6-9 shows each of the functional blocks discussed in this section.

SYSTEM BUS STRUCTURES

There are four major buffered bus structures that support data transfer between each functional block and throughout the computer board.

Kernel Bus

This bus supports data transfer within the kernel and is buffered from the remainder

of the system. The Kernel bus is further defined later in this section.

Internal Address Bus

The Internal Address bus (IA bus) is the latched address portion of the multiplexed Kernel bus. This bus provides 24-bit addressing for Kernel ROM and main memory as well as the system I/O control decoders. Latching is performed by three 74F373 octal latches (see page 9 of the schematic diagrams).

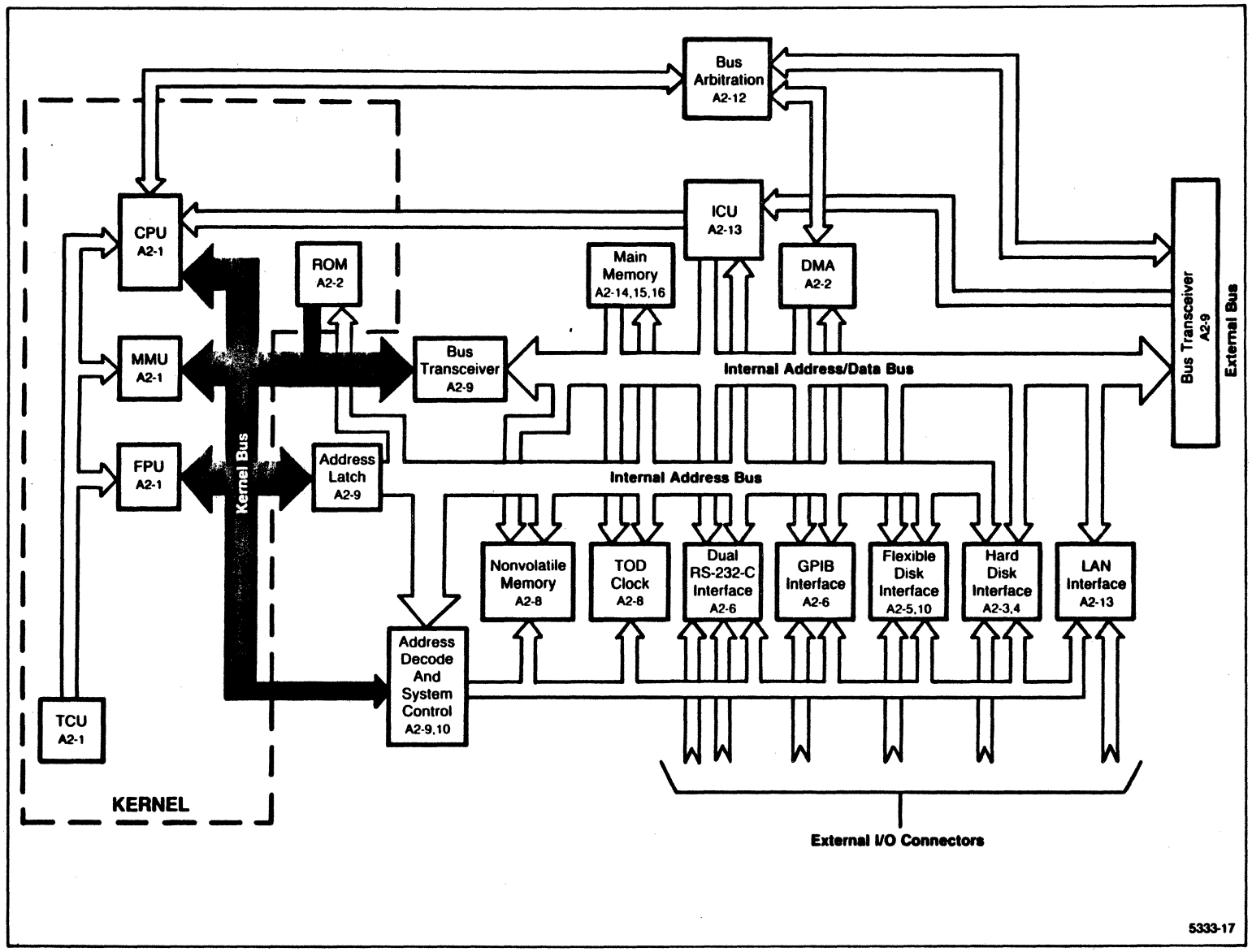


Figure 6-9. Computer Board Block Diagram.

Internal Address/Data Bus

The Internal Address/Data bus (IA/D bus) provides the address and data interface between the kernel and the various system I/O devices on the compute board. Interface between the External bus and the kernel is also provided by the IA/D bus. The structure of the I/AD bus is basically the same as the Kernel bus: a 24-bit multiplexed address/data bus with the 16-bit data bus sharing the lower 16 lines of the 24-bit address bus (see page 9 of the schematic diagrams). The IA/D bus is buffered from the Kernel bus by three 74ALS245 octal bus transceivers.

External Bus

The External bus provides the interface between the computer board and system options. Bus connectors located on the options backplane provide electrical interface. The External is bus primarily an extension of the IA/D bus. Bidirectional interface for the address/data bus itself is provided by six 74AS373 octal D-type latches and associated bus interface control logic. Interface for the bus-control and protocol signals is provided by two 74F244 octal buffer/line drivers (see page 11 of the schematic diagrams).

KERNEL

Refer to page A2-1 of the schematic diagrams. The kernel controls, either directly or indirectly, the major functions for the entire computer board. The kernel is comprised of five major components: the Central Processing Unit (CPU), the Memory Management Unit (MMU), the Floating Point Unit (FPU), the Timing Control Unit (TCU), and kernel ROM. The FPU is an optional device. Within the kernel, these devices are supported by additional logic. System addressing and memory management/protection is a task that is shared between the CPU and the MMU, while floating point operations are supported by the FPU.

Data transfer within the kernel and with the remainder of the system is via the Kernel bus, which consists of the multiplexed address and data bus. Another bus apart from the Kernel bus is the Kernel Timing and Control bus, which provides the necessary timing, status, and control signals between the primary kernel components.

Kernel Bus

The Kernel bus provides the means of data transfer within the kernel and between the kernel and the rest of the compute board. All signals on the Kernel bus are high-active. The Kernel bus may be sampled at the CPU pinout.

A16-23 Address bits 16-23 are high-active outputs and are the most-significant eight address bits of the Kernel bus. During clock period T1, the bus contains the virtual address output by the CPU. During clock

period TMMU, this bus contains the translated, physical address output by the MMU.

A/D15-00 These are the multiplexed, bidirectional address and data lines for the Kernel bus. All lines are high-active. Bit 00 is the least significant bit. During clock period T1, this bus contains the virtual address output by the CPU. During TMMU, this bus contains the physical address output by the MMU. During clock periods T2 through T4, this bus contains data output by the CPU, MMU, memory, etc.

Kernel Timing and Control Bus

This bus is local to the kernel and is used to provide control, timing, and coordination of kernel-level operations, including memory management, and the execution of floating point operations. These signals may be sampled at the CPU pinout. Bus signals are defined next.

PH1, PH2 These signals (Phase 1, Phase 2) provide two non-overlapping phases of a single frequency, 10 megahertz clock. These inputs are taken from the Timing Control Unit. The execution of microinstructions within the CPU or steps in a data transfer over the Kernel bus is synchronized and controlled with respect to the number of timing states or T-states required to complete the execution. A T-state is defined as the time between the leading edges of the Phase 1 clock. T-states are numbered progressively from the beginning of a bus cycle to its completion.

KRDY-1 This high-active signal (Kernel Ready-1) is asserted by the Timing Control Unit at the end of the bus cycle to signal the CPU that the operation is complete. The CPU then terminates the cycle. An external device that requires additional time to finish the bus cycle can request an extension to the TCU. The TCU then inserts a given number of wait states, allowing the device to finish the cycle before asserting KRDY-1.

KHOLD-0 This low-active input (Kernel Hold-0) is asserted by another device that is requesting the use of the Kernel Bus. If the CPU complies, the CPU asserts Kernel Hold Acknowledge-0 (KHLDA-0) to the MMU. The MMU then outputs Kernel Hold Acknowledge Output (HLDAO-0) to the DMA device requesting the bus. KHOLD-0 is asserted for the entire time the DMA device has the bus, and KHLDA-0 remains asserted by the CPU (and HLDAO-0 by the MMU) until the bus is regained by the CPU.

KHLDA-0 Kernel Hold Request Acknowledge-0. See previous KHOLD-0 description.

KHLDAO-0 Kernel Hold Request Acknowledge Out-0. See previous KHOLD-0 description.

HBE-0 This low-active output (Kernel High Byte Enable-0) is asserted by the CPU to enable the high byte of the addressed location to be

placed on the bus. Memory is organized as two 8-bit banks, with each bank receiving the 24-bit address in parallel. The low bank (bits D00-D07) responds to even byte addresses, that is, when the least significant address bit (A00) is low. The high memory bank (bits D08-D15) responds to odd addresses. To address an even-odd byte pair, the even address is placed on the bus and KHBE-0 is asserted. This feature permits word-wide addressing or single-byte addressing.

DS/KFLT-0 — Data Strobe/Kernel Float-0 is a dual-function signal, whose function is determined by whether or not the MMU is performing address translation or the CPU is addressing the Kernel bus directly. If the MMU is present in a system, the DS portion is not used. For bus cycles that are not address-translated (no MMU), this pin functions as a Data Strobe-0 output from the CPU. Data Strobe-0 is asserted after the multiplexed address/data bus has switched from address presentation to accepting or presenting data. The assertion of Data Strobe-0 validates the data on bus lines AD00-AD15. Since address translation is always performed for every bus cycle initiated by the CPU, Data Strobe-0 is never asserted.

For bus cycles that are address-translated, this pin functions as the Kernel Float-0 input to the CPU. The assertion of KFLT-0 by the MMU causes the CPU to wait longer than the normally allotted TMMU Timing state for the MMU to perform address translation. This function is employed by the MMU in order for it to update its internal translation cache from page tables in memory, or to update status bits contained within the tables. Timing states are not numbered during a float condition, and the entire bus cycle is placed on a temporary hold. After KFLT-0 is deasserted, the bus cycle continues from where it was suspended. The Kernel has been implemented such that address translation is always performed by the MMU, although the translated physical address may be the same as the virtual address.

KABT-0 — This is a low-active, dual-function signal. This signal is asserted during TMMU or TFloat (an address-translated cycle) by the MMU and held low for one clock cycle to cause an Abort of the bus cycle and the instruction that executed it. The rest of the system remains unaware of the aborted cycle, since the MMU Physical Address Valid-0 address strobe, which triggers the physical cycle, was not yet asserted.

If this pin is held low for at least 64 clock cycles, the CPU and MMU interprets it as a reset. If a reset is received by the MMU, the MMU activates the KABT-0 signal to the CPU.

KRST-0 — Kernel Reset-0 is an input to the CPU and MMU from the Timing Control Unit (U1330A) and is used to reset the system. Upon receiving KRST-0, the MMU asserts KABT-0 to reset the CPU.

KAT-0/KSPC-0 The Kernel Address Translation-0/Slave Processor Control-0 is a bidirectional, dual function signal. The AT-0 portion of this signal enables address translation by the MMU. The SPC-0 function enables slave processor communications (for example, with the FPU).

The CPU is able to operate with or without address translation. The mode of operation is determined by the presence of the MMU. The MMU asserts Address Translation-0 during reset and at power-up. The CPU samples AT-0 on the rising edge of the reset pulse. If the AT-0 is high (no MMU present), bus cycles are performed without address translation. If during reset AT-0 is low, the bus cycle includes an extra clock cycle (TMMU). At this point, the DS-0/FLT-0 signal becomes a Float-0 command input to the CPU (see previous definition of DS-0/FLT-0). Since the MMU is always present and address translation is always performed, this signal is always low at power-up and reset.

AT-0/SPC-0 is also used as the data strobe in slave processor data transfers. During slave processor data transfers, data is transferred on bus lines AD00- AD15, but no bus control lines other than DDIN-0 (controlled by the CPU) are asserted. For example, ADS-0 and HBE-0 are not used. During a slave processor bus cycle, the slave processor samples the CPU status lines ST0 and ST1 on the leading edge of SPC-0. During a data read, SPC-0 remains asserted until data has been read from the slave processor. During a data write, the slave processor latches the status bits on the leading edge of SPC-0 and latches data on the trailing edge of SPC-0. In all slave processor bus cycles, SPC-0 is asserted by the CPU. Refer to Slave Processor Bus Cycles, later in this section.

KUS-1 Kernel User-1 is an output taken from the U bit in the Processor Status register, which is an internal status register. This signal is asserted low to indicate the supervisor mode. This signal is sampled by the MMU for mapping and protection purposes.

KADS-0 Kernel Address Strobe-0 is asserted by the CPU when it places an address on the Kernel address bus. Without the MMU, this signal would be used to validate and latch the address. However, with address translation by the MMU, this signal is sent to the MMU only, where it latches the virtual address. The MMU outputs the Physical Address Valid-0 strobe to validate the translated, physical address.

KPAV-0 This MMU output is generated during TMMU and is used as the address strobe to latch the physical address into external memory devices. This signal is also used during a float condition to access the external page tables.

KDDIN-0 Kernel Data Direction In-0 (KDDIN-0) is output by the CPU or the MMU to specify a read operation (low) or a write operation (high). During normal bus cycle with address translation, this signal is output by the CPU to indicate data direction. During a float condition, the CPU tristates KDDIN-0, allowing the MMU to assert KDDIN-0 low, and thus allowing the MMU to update its page tables from memory. The MMU also controls KDDIN-0 when it has control of the Kernel Bus.

KPFS-0 Kernel Processor Flow Status-0 is a low-active pulse that is asserted by the CPU to indicate the beginning of an instruction cycle.

KST0-KST3 This is a 4-bit bus cycle status code (Kernel Status 0-3) that provides status information. The pins are interpreted as a 4-bit value, with ST0 as the least-significant bit. Only two bits, ST0 and ST1, are sampled by the FPU during slave processor bus cycles, while all four bits are sampled by the MMU. Refer to the CPU data manual for a definition of each of the codes.

KILO-0 Kernel Interlocked Operation-0 is a low-active output that is asserted during a Set Bit Interlocked or Clear Bit Interlocked instruction. This signal is used to reserve the bus in a multiprocessor system that shares resources, in this case, common RAM that the computer board shares with the display processor.

NMI-0 This signal generates a nonmaskable interrupt-0 (NMI-0) to the CPU.

Central Processing Unit

The NS32016 CPU (U1280) is the heart of the kernel. This device is configured in a 48-pin DIP. The CPU provides a 16-megabyte uniform address space. The CPU's internal architecture features 32-bit data paths, although the data path at the pin-out is 16-bits wide. Refer to page 1 of the schematic diagrams.

The CPU provides 16 registers, eight of which are dedicated control/status registers, and eight general purpose registers. The general-purpose registers are 32-bits in length and are used for general storage requirements, such as storing temporary variables and addresses. The CPU clock frequency is 10 megahertz. As stated previously, data transfer within the computer board is afforded by the Kernel bus and other bus structures. Within the kernel however, dedicated data transfer that is transparent to the rest of the system is accomplished with the slave processor bus cycle.

Slave Processor Bus Cycles

The slave processor bus cycle permits communication between the CPU and the slave processors (the MMU and the FPU) without executing the Kernel bus protocol. This type of transfer utilizes the data bus portion (AD00-AD15) but none of the bus control/signals (excluding DDIN-0).

Slave processor bus cycles require only 2 clock cycles or T states (labeled T1 and T4) to finish. At the start of a data read cycle (T1), the CPU places the appropriate status code on lines ST3-ST0 and the appropriate processor identification byte on data line AD00-AD07 of the Kernel bus. The CPU then asserts SPC-0. Both the FPU and the MMU decode the identification byte and latch the status from the CPU on the leading edge of SPC-0. The appropriate slave processor responds by placing data on lines AD00-AD15 at T4. The CPU reads the data and terminates the cycle by deasserting SPC-0.

During a data write (at T1), the CPU asserts the appropriate status code processor identification byte as before. The CPU then asserts SPC-0 and the appropriate

processor responds by latching the status code and identification byte. The CPU then removes the identification byte from the Kernel bus and places data on the bus. The data is latched by the slave processor on the trailing edge of SPC-0 as it is deasserted (T4). At the end of a data write, the slave processor signals a successful transfer by pulsing SPC-0 low.

Since ADS-0 is not asserted by the CPU, none of the associated bus protocol signals are asserted. The CPU, however, asserts DDIN-0 as appropriate. In both of the above cases, the status code is set up by the CPU during the previous clock cycle.

Memory Management Unit

The NS32082 Memory Management Unit (U1300) provides support for demand-paged, virtual-memory management. The device, in concert with the CPU, permits rapid address translation and protection on individual 512-byte memory pages. The chip uses an associative cache that stores the 32 most frequently used memory-page table entries. The MMU is packaged in a 48-pin DIP. Refer to page 1 of the schematic diagrams.

Memory Management

For addressing purposes, memory is divided into several 512-byte pages. Associated with each page of memory are page tables that the MMU and the operating system maintain in physical memory. The page tables contain information pertinent to each memory page, such as the page access permission codes, whether the page has been accessed, and if it has been written to. Also contained in the page tables are values that are used to determine the physical address. The MMU executes a translation algorithm that determines the validity of the access and provides the physical address. Of the virtual address provided by the CPU, the least-significant 9 bits are not modified. These 9 bits provide discrimination to the byte level within the 512-byte page.

By modifying the page tables as required, the operating system controls the mapping of virtual addresses to physical memory. Additionally, the operating system can control the degree of access (read or read and write) permitted to specific pages in the supervisor and user modes by generating translation error aborts if access permission codes are violated.

The most frequently referenced or accessed page tables are stored by the MMU in an internal cache memory, thus saving the MMU from having to retrieve the page table from memory for the majority of accesses. The cache contains 32 page-table entries. If during a bus cycle, the given access is not a "hit," the MMU asserts the Float-0 signal to the CPU, which temporarily suspends the bus cycle while the MMU retrieves the page table from physical memory via the Kernel bus. Once the page table entry has been retrieved, the least-used entry is removed from the cache and the newest entry is placed in the cache. The Float condition is terminated and the bus cycle continues from where it was suspended.

All bus cycles initiated by the CPU are address-translated; however, in some cases the translated, physical address may equal the virtual address placed on the Kernel

bus by the CPU.

Floating Point Unit

The NS32081 Floating Point Unit (U1260) operates as a slave processor and performs both single precision (32-bit) and double precision (64-bit) arithmetic. This device is packaged in a 24-pin configuration. Data transfer between the CPU and the FPU is not accomplished using the normal Kernel bus protocol, but the slave communications protocol described previously. The FPU contains nine 32-bit registers, eight of which are general-purpose. The ninth register is a status register. Refer to to page A2-1 of the schematic diagrams and the FPU data sheet for additional information.

Timing Control Unit

The NS32201 Timing Control Unit (U0320) is a 24-pin DIP that provides the two-phase 10 megahertz clock outputs based on the 20 megahertz crystal frequency, as well as several signals that support Kernel bus logic, timing and control functions (refer to the Kernel bus signal definitions section). The TCU also provides for a variety of bus cycle extensions to compensate for slower devices (compute board or peripheral devices). Refer to the TCU data sheet for additional information and to page 1 of the schematic diagrams.

Kernel ROM

Refer to page A2-2 of the schematic diagrams. Up to 128 kbytes of Kernel ROM are provided by four 256-kbit (32k × 8-bit) EPROM chips (U3280, 3300, 4280, and 4300). Kernel ROM is organized as two 64-kword banks. Lesser total capacities are 64 kbytes and 32 kbytes, depending on chip density and whether two or four ROMS are installed.

ROM addressing is provided by the Internal Address bus, which is the latched address portion (AD00-AD15) of the Kernel bus, while ROM data is placed directly on the data path of the Kernel bus. Internal Address lines IA16-IA23 access the specific ROM bank while lines IA1-IA14 address the ROM location. ROM is accessed in words.

NONVOLATILE MEMORY

Refer to page A2-8 of the schematic diagrams. This functional block consists of one or two 256-bit, nonvolatile, sequential-access EEPROMs (U9241 and 9240) and a Nonvolatile Memory Control register (U8240). Each memory chip is organized as 16 registers containing 16 bits each. Each register is written to or read from serially. Nonvolatile memory is read from by loading an instruction into the chip. This intruction, which includes an address, is decoded by the chip and data is placed into an internal serial shift register. The contents of the shift register are read out by

the SK clock (pin 2 of each chip), which synchronizes the data transfer.

MAIN MEMORY

Refer to pages A2-14 through A2-16 of the schematic diagrams. Main memory provided on the computer board consists of up to 1 megabyte of dynamic RAM using 256-kbit parts, or 256 kbytes using 64-kbit parts. The board contains a maximum of 36 RAM devices, each of which is organized in a 256 k × 1-bit or 64 k × 1-bit format. On the board, memory is organized as two rows, each containing a maximum of 18 chips. Each memory row is two bytes wide plus one parity bit per byte.

The computer board contains logic that provides support functions for the RAM. These functions are:

- Memory access and refresh control
- Memory addressing
- Parity generation and error detection

Memory Access and Refresh Control

This logic employs a 200-nanosecond delay line to establish memory-access and refresh-cycle timing. This block coordinates the memory refresh cycle, which is performed every 12.5 microseconds, and normal memory accesses. The Refresh clock (REFCLK-1) initiates a memory refresh cycle on the falling edge of the clock pulse, at which time various status lines are sampled to determine whether a system memory access is in progress. If a system memory access is in progress, the refresh cycle is postponed until the data transfer is completed. When refresh is in progress, memory accesses are locked out until the refresh is completed.

Memory refresh is initiated by REFCLK-1 (inverted by U3150), which clocks flip-flop U3160B at pin 3. U3160 outputs Refresh Request-1 (REFREQ-1) to flip-flop U0150A. U0150B is clocked on the trailing edge of System Address Strobe-0 (SAS-0) and outputs a low, which is inverted by U3150 at pin 5.

Contention between a normal memory access and refresh is handled at this point by AND gate U3140, which is enabled to pass the refresh request signal only if a memory access is not in progress. A high output at pin 11 of U3140D clocks flip-flop U2170B, outputting Refresh-1 and Refresh-0 (REF-1 and REF-0). REF-1 is used to set the Program bit (pin 12) of the decoder U0140 high, while REF-1 sets pin 15 of U0140 high, thus causing all Bank Select bits BNK0-1 through BNK5-1 to be asserted. This is in preparation for refresh.

REF-0 is also inverted by U3150F and ANDed with Memory Busy-0 (MBUSY-0). If MBUSY-0 is high, the refresh cycle continues. MBUSY-0 is a memory access control signal and that, when asserted, indicates that memory is busy performing either a refresh or normal access. If a refresh is being performed, MBUSY-0 locks out normal accesses. If a normal access is being performed, MBUSY-0 locks out refresh cycles. With MBUSY-0 high, NAND gate U0170 is enabled and Row Address Strobe Gate-1

(RASGATE-1) output to the memory banks. RASGATE-1 is ANDed with each of the asserted memory bank select signals, causing RAS-0 to be asserted to each chip. This logic supports a distributed refresh method whereby only one memory row is refreshed per refresh cycle. The refresh address is developed by a Refresh Counter (U3120), which is incremented for the next refresh cycle by one on the trailing edge of REF-1. Output from the counter is placed on the Memory Address bus by the octal transceiver U3110, which is enabled by REF-0. After the new row address has been placed on the Memory Address bus (MA bus), the Row Address Strobe (RAS-0) is pulsed, refreshing the 512 memory-bit locations in that row. With 256 k-byte parts, 256 refresh cycles are required for a full memory refresh.

The above method for performing a refresh cycle requires that SAS-0 be asserted in order to clock the refresh flip-flop U3160. Under certain circumstances, SAS-0 may not be asserted often enough (at least every 12.5 microseconds) to perform the refresh cycle. For this reason, REFREQ-1 also is used via AND gate 4150D and NAND gate 2150D to set flip-flop U0150A and thereby force a refresh cycle.

During a normal memory access, the address is determined to be a valid memory address at pin 3 of AND U3140A, which outputs Memory Address-1 (MMADR-1). MMADR-1 is clocked out of flip-flop U2170A as Access Request-1. The Q-bar output of U2170A, which is low at this time, disables NAND gate U3140, thereby disabling refreshes until the memory access is completed. ACCREQ-1 is ANDed with MBUSY-0 as before. RASGATE-1 is output to memory and RAS-0 is output to the memory bank selected by the decoder U0140.

The 200-nanoseccond delay line DL4160 provides timing for the block. During a normal access, row addresses are set up prior to Memory Time 0-0 (MTIM0) and RAS-0 is asserted at MTIM0-0. At MTIM40-0, row addresses are removed from the Memory Address (MA0-8) and column addresses are placed on the Memory Address. The multiplexing of the row and column addresses onto the Memory Address bus is performed by octal transceivers U1110, U2110, and 2120. At MTIM80-0, CAS-0 is asserted, and for a read option, data is available at MTIM200-0. At that time the pulse becomes high, reseting the logic in preparation for the next cycle. RAS-0 and CAS-0 are not cleared until MTIM280. The data read cycle from memory requires approximately 400 nanoseconds, whereas a data write cycle from memory can be extended beyond 400 nanoseconds.

Memory Addressing

This functional block samples the IA/D lines 18-23 to determine if the bus cycle is a memory access, in which case the impending refresh cycle may be postponed until the end of the data transfer. This block also provides the multiplexing required to place the 16-bit address word (IA/D01 - IA/D16) on the 9-bit Memory Address bus (MA0 - MA8), as well as the Row Address Strobe-0 (RAS-0) and Column Address

Strobe-0 (CAS-0) synchronization required to latch the address into memory.

Parity Generation and Checking

This block utilizes two parity generators/checkers and associated logic to generate and store an even parity bit for each byte during a memory write operation, and to check the stored parity bit during a memory read. If an error is detected during a read, a Parity Error signal is generated, as well as a bit defining whether the error applies to the high or low byte. A Parity Error register, which is continually loaded with the current memory address, is used to provide the address of the faulty memory location. A brief description of the operation of the parity generation and checking logic for the high byte is given below.

During a memory write, the high data byte from the IA/D bus is input to the U5100 parity generator/checker. At this time, the octal D-type latch U5110 is disabled because DDIN-1 is low and the output of NAND gate U4120 is high. NAND gate U4120 outputs a high at pin 8, and the parity generator U5100 generates even parity (HPARI) for the high data byte plus the additional high bit input at pin 4. The parity bit is stored with the byte in memory.

During a memory read DDIN-1 is high and the octal latch U5110 is enabled. The stored parity bit is inverted by NAND gate U4120 (which is enabled by DDIN-1) and input at pin 4 of parity generator U5100. U5100 generates odd parity for the data byte plus the inverted parity bit. If the stored bit or the data byte is in error by one bit, the parity checker generates a a parity error signal on the odd parity output, Parity Error High (PEHI-0). PEHI-0 is clocked through flip-flop U6130A and inverted to become Parity Error-1 (PERR-1), which is read by the CPU when it reads the System Status register, U6150. The occurrence of a parity error clocks the octal D-type flip-flops U6190 and U6200, which latch bits 10-23 of the Internal Address bus, thus saving the address of the faulty memory location (although discrimination is not provided to the byte level). The content of flip-flops U6190 and U6200 are read by the CPU. Both are output-enabled by the system I/O control decoders, described below.

SYSTEM CONTROL BLOCK

Refer to pages A2-9 and A2-10 of the schematic diagrams. The system control block provides the system I/O enables and control signals required to enable DMA transfers via the various I/O devices, as well as the enables for the System Control register and the System Status register. These enables are arranged as memory-mapped I/O locations in the kernel's external memory space. The System Control block is addressed by the Internal Address bus, which is the latched address portion of the Kernel bus. Two 74F138 3-to-8-bit decoders (U4250 and U4270) and associated logic decode the internal address value, enabling the selected I/O

device.

System Control and Status Registers

This functional block also contains the System Control register and the System Status register. The System Control register consists of two flip-flops, U5140 and U5150. U5140 is selected and clocked during a register-write operation, whereas U5150 is selected and clocked during a register-read operation. The System Status register U6150 is also an octal D-type flip-flop and is also selected by the system I/O decoders described in the previous paragraph.

Configuration Switch and Diagnostic Display Registers

The system control block also provides a mechanism for low-level debugging of the board. This consists of a Configuration Switch register and a Diagnostics Display register. The switch register is a 8-switch DIP that corresponds to lines AD00-AD07. The setting of the switch is read by enabling 74F244 octal buffer U0350 (address FFF008). Diagnostic information is displayed by a write to the same address. An 74LS273 octal D-type flip-flop U4340 performs as the display register. The D outputs (AD00-AD06) correspond to segments A-F of a seven-segment display. Bit AD07 drives the decimal point. Both registers are selected by the system I/O decoders.

FLEXIBLE DISK INTERFACE

The flexible disk interface is composed of three major components: the WD1770 Flexible Disk Controller (U7020), the AM9516 DMA Controller (U8290), and the Flexible Disk Control register (U8010) which is a hex D-type flip-flop, along with supporting logic. The WD1770 is a flexible disk controller and formatter and also contains digital data separation logic and write-precompensation circuitry. All accesses of the flexible disk are through the DMA controller. Interface between the two controllers is by an 8-bit bidirectional data bus and various control signals.

DMA Controller

Refer to page A2-10 of the schematic diagrams. The host accesses the DMA controller via the system I/O control block. The DMA controller (page 10 of the schematic diagrams) is equipped to handle two separate channels although only one DMA channel (channel B) is used. DMA operations are initiated by the kernel by loading DMA control parameters into a control block known as the Channel Control Table. The Channel Control Table is maintained by the kernel in main memory. The kernel then places the starting address of the Channel Control Table in the Chain Address register (internal to the DMA controller) and issues a "Start Chain" command to the controller. The DMA controller responds by updating its various internal control registers with the control parameters located in the Channel Control Table. The Channel Control Table contains such information as what specific registers are to be updated or reloaded, the source data address, the destination data address, and so forth.

Chaining allows the several DMA transfers to be performed asynchronously. This method places the address of the next Channel Control Table within the previous table. So that when a given DMA operation is completed, the DMA controller reads the new address of the control table, updates internal control registers with the table, and executes the new command.

As mentioned before, the System Control Block provides the address decoding required to access the flexible disk interface.

Signals that input or output the DMA controller are discussed next.

DSKDMA-0 This input (Disk DMA-0) is developed by the system I/O decoders and is the chip-select input used by the host to activate the DMA controller. This signal is asserted to select the controller and perform reading or writing of the controller's internal registers.

DREQ2-0 This input (DMA Request-0) is developed by the flexible disk controller and indicates to the DMA controller that the flexible disk controller internal data register is full and can be read from (during a read operation) or is empty and can be written to (during a write).

BREQ-1 This output (Bus Request-1) is used by the controller to gain control of the IA/D bus. This is a request signal that is arbitrated by the DMA Arbitration Programmable Array Logic (PAL) U1230.

DSKG-0 This input is from the DMA Arbitration PAL U1230 and indicates to the controller that it has been granted the bus.

IA1 This bit is an input that is used only when the DMA controller is bus slave. When high, this line indicates that the information on data lines D0-D16 of system bus is an address of an internal register to be accessed. When this line is low, it indicates that a transfer is taking place between the host and the DMA controller register previously selected.

BUSWAIT-0 This input (Bus Wait-0) is asserted for every bus cylce initiated by the host. This input is developed from System Address Strobe-1 and intiates a Wait state to the DMA controller. This causes the controller to extend the Data Strobe-0 (DS-0) and allows slower devices time to latch the data before it is removed from the bus.

BYTE-1 This output indicates that data is being transferred on the bus. A high indicates a byte-wide transfer (IAD0-IAD7), and a low indicates a word-wide transfer (IA/D0-IA/D15).

NORM-1 This output (Normal-1) is active only when the controller is bus master. A high indicates normal bus cycle and a low indicates system bus cycle. This output is high during a normal data transfer between the controller and memory and low when the controller is accessing I/O space and is performing a chaining operation.

FDACK-0 This output (Flexible DMA Acknowledge-0) is asserted to indicate that the controller is executing a DMA operation. This output is used to select the flexible disk controller U7120 and enable the disk data

interface transceiver U7010.

READ-1 — This bidirectional line is asserted to indicate the direction of the data transfer. This signal is asserted by the host when data is being transferred from the DMA controller to the host. The DMA controller asserts READ-1 when it is bus master and is executing a transfer from another source to the controller.

DS-0 — Data Strobe-0 is a bidirectional signal that is asserted when valid data is present on the data bus IAD0-IAD15. Data is removed from the bus after this signal is deasserted.

ALE-1 — This signal is asserted by the DMA controller and is used to develop SAS-1, which is used by main memory to latch the address.

Erroneous ALE Detection Logic

Logic associated with the DMA controller includes erroneous ALE detection logic. This consists of the D-type flip-flops U6041A and U6130B, and associated logic. This logic was implemented in order to detect and void or cancel the erroneous assertion of Address Latch Enable-1 by the controller. This logic differentiates between chain operations and single data transfers. Note that this interface allows only one data transfer per bus-request/bus-release cycle. This logic operates as follows.

The NORM-1 output from the DMA controller is programmed to be asserted high when data is being transferred between the flexible disk controller and memory. During a data transfer, ALE-1 is asserted by the controller to the Kernal bus as Kernal Physical Addrss Valid-0 (KPAV-0). When data is placed on the bus, NORM-1 is asserted by the DMA controller, which is clocked through U6041 as NOALE-0. NOALE-0 disables AND gate U3140B and Quit ALE-1 (QALE-1) deasserts KPAV-0 to the Kernel bus.

During chaining operations, NORM-1 is output low by the DMA controller and is clocked though U6041A as CHAIN-0. The assertion of ALE-1 clocks flip-flop U6130B, which outputs Hold Bus-0 (HLDBUS-0). In this case, BREQ-1 has been released (low) by the DMA controller and the DMA controller does not assert DS-0. NAND gate U4170C outputs Hold Data Strobe-0 (HLDDS-0), which becomes Disk Data Strobe-0 (DSKDS-0). DSKDS-0 is used to develop Memory Data Strobe-1 (MDS-1) in order to complete the bus cycle. Since the DMA controller is executing reads from memory during chaining operations, memory data is not affected.

Flexible Disk Controller

Refer to page A2-5 of the schematic diagrams. The flexible disk interface uses the WD1770 flexible disk controller U7020, which operates as a controller and formatter and also contains digital data separation logic and write-precompensation circuitry. There are six registers within the flexible disk controller that let the DMA controller execute data transfer between the disk controller and the DMA controller. These registers contain command and status information, various head positioning

information, and 8-bit data.

The signals that input or output the flexible disk controller are discussed next.

CS-0 — This input (Chip Select-0) is developed from the FDACK-0 output from the DMA controller, when disk data is being transferred, or from the FLEX-0 and Data Strobe-0 signals when the host is programming the flexible disk controller is preparation for the disk data transfer.

READ-1 — This input specifies whether the transfer is a read or a write operation. A high specifies a read operation, where data is being transferred from a selected internal register to the 8-bit IA/D bus. A low specifies a write operation , where data from the IA bus is being placed in an internal register.

A1, A0 — These inputs are developed from either IA2 and IA1 of the IA bus, respectively, when the host is accessing the flexible disk controller, or from DSKG-1, when the DMA controller is performing a disk DMA operation. A1 and A2 are used to select one of four registers internal to the flexible disk controller that are used in the transfer of program information or data between the controller and the 8-bit data bus IAD0-IAD7.

MR-0 — This input resets the flexible disk controller.

DDEN-0 — This input is from the Flexible Disk Control register (U8010) and is written to by the host to select double or single-density formatting. DDEN-0 low double-density formatting. DDEN-0 high selects single-density formatting.

INTRQ-1 — This output (Interrupt Request-1) becomes Flexible Interrupt-1 and inputs the Interrupt Control Unit (U5240). This bit is set at the completion of any command and is reset when the host reads the flexible disk controller's status register.

DRQ-0 — This output (Data Request-0) is sent to the DMA controller to indicate that the disk controller's internal data register is full and can be read from (during a read operation) or is empty and can be written to (during a write operation).

HARD DISK INTERFACE

Refer to pages A2-3 and A2-4 of the schematic diagrams. This interface is composed primarily of the WD2010 Winchester Disk Controller (U7100), an external 4-kbyte cache (U7060 and U7080), a DP8460 data separator (U9170), and a Hard Disk Control register (U6060).

The controller performs the normal functions of a hard disk drive controller/formatter, although it does not feature write precompensation and this logic (consisting of quad D-type flip-flop U47, delay line U51, and data multiplexer U52) is implemented externally.

On the drive side of the controller, during a disk data read, the data separator receives Modified Frequency Modulation (MFM) encoded data from the disk drive via the differential line receiver U9140. The data separator U9170 receives and separates this data into synchronized data (SDATA) and a Read Clock (RCLK) signal. SDATA is synchronized with the VCO Clock output of the disk data separator by flip-flop U8150B, which outputs serial Read Data to the hard disk controller U7100, pin 37. Read Data is decoded by the controller using RLCK into 8-bit parallel data and output on the Hard Disk Data bus (HDD0-HDD7).

During a disk data write operation, the flexible disk controller outputs Write Data, which is a serial output that contains the MFM clock and data pulses to be written to the disk. EARLY and LATE are precompensation outputs from the controller that are used by the delay line DL7130 and the data selector (U7120) to delay the data pulses to the disk.

Write Precompensation

When data is written to magnetic disk media, the flux transitions recorded on the disk have an undesirable characteristic of spreading apart from each other at time the data is written to the disk. Write precompensation circuitry retards or advances (relatively) the encoding of flux transitions to the disk to compensate for this effect. The write-precompensation logic consists of D-type flip-flop (U6120), delay line (DL7130), and data selector (U7120). Serial data from the disk controller (WD) is synchronized by the 10 MHz clock and input into delay line DL7130. For the non-precompensated pulse, the normal delay is 24 nanoseconds, and the data selector (U7120) outputs the pulse to the differential line driver U8120 with a 24-nanosecond delay. To advance the pulse relative to the standard 24-nanosecond delay, EARLY-1 is output by the disk controller, causing the selector U7120 to select D5 input, which is only delayed 12 nanoseconds. To retard the pulse relative to the standard 24-nanosecond delay, LATE-1 is output by the disk controller, causing the data selector to select the D6 input from DL7120, which is delayed by 36-nanoseconds.

Disk Data Cache

On the host side of the controller, the 4-kbyte cache is a FIFO, disk-data transfer buffer that is accessible by the disk controller or the kernel. The buffer appears to the kernel as a 2-kword (16-bits) sequential-access buffer. The buffer itself consists of two 2048 × 8-bit static RAM chips, U7060 and U7080. This buffer and the octal bus transceiver (U7090) also serve as a data assembler/disassembler in that data is transferred between the kernel and the buffer in 16-bit words, whereas data transfer between the buffer and the disk controller occurs in 8-bit bytes.

Buffer addressing is performed by two dual, four-bit binary counters, U7050 and U6050. Only half of U6050 is used. During a data write to the disk, the host clears the buffer by setting the Manual Clear bit (MNCLR-0) in the Hard Disk Control register (octal D-type flip-flop U6060). This generates the Counter Clear-1 (CCLR-1) output of the Buffer Control PAL U8050, which clears the counter. As each 16-bit word is loaded into the buffer, the counter is incremented by the Counter Clock-0 (CCLK-0) output of PAL U8050, which develops the clock from the Data Strobe-0

(DSTB-0) input. When the host has loaded the buffer, the host writes a Manual Ready-1 (MNRDY-1) signal to the controller via the PAL (input to the controller as Hard Disk Buffer Ready-0 (HDBRDY-0)). The controller then clears the buffer counter and transfers the contents of the buffer to disk, incrementing the buffer address counter as each 16-bit word is read. Since the buffer is organized as two 2k × 8-bit chips, each byte can be read individually (although sequentially) by the controller. This is permitted by the bus transceiver U7090, which multiplexes both the high and the low bytes of the buffer onto Hard Disk Data lines 0-7 (HDD0-HDD7).

During a data read from the disk, the controller clears the buffer address counter and begins loading the buffer. This time the bus transceiver operates in reverse fashion, demultiplexing the 8-bit data from the controller into the high and low bytes prior to loading into the buffer. CCLK-0 is generated by the PAL U8050, which monitors the Hard Disk Buffer Chip Select-0 (HDBCS-0) output from the disk controller U7100. When the controller-to-buffer transfer is completed, the controller signals the host by asserting Hard Disk Interrupt-1 (HDINT-1). The host proceeds to read the contents of the buffer, by first resetting the buffer address counter and then incrementing the counter with each word read.

Two 74LS245 bus transceivers (U6080 and U6090) serve to buffer or isolate the IA/D bus from disk/cache data. As given previously, the System Control block provides the address decoding required to enable data transfer via the hard disk interface.

Buffer Control PAL

The Buffer Control PAL (U8050) controls the operation the disk data buffer and the data buffer address counter. Inputs to the PAL are from the disk controller and the system control logic (address decode). Outputs drive the buffer chip enables, address counter, and Hard Disk Buffer Controller Ready-0 (HDBCR-0) line. Figure 6-10 defines the pin and signal correspondence for PAL U8050, followed by a description of each of the signals and their functions.

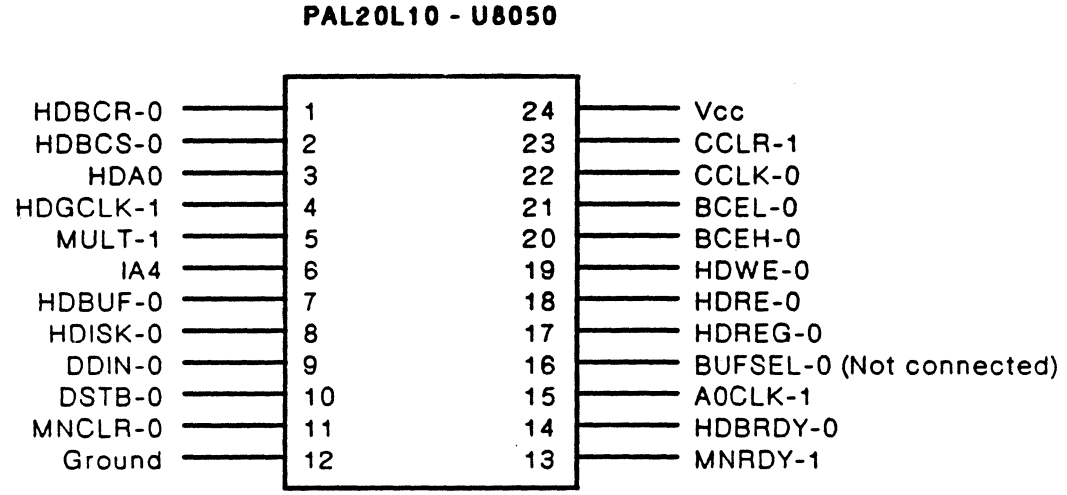


Figure 6-10. PAL Signal Identification for U8050.

All signals that input or output PAL U8050 are discussed next.

HDBCR-0 Hard Disk Buffer Counter Clear-0 is output by the disk controller to clear the counter in preparation for a cache data transfer between the cache and the disk controller.

HDBCS-0 Hard Disk Buffer Chip Select-0 is asserted by the disk controller to enable the reading or writing of the cache by the disk controller. This signal is used to differentiate what device is accessing the cache, the host or the disk controller.

HDA0 This input is used when the disk controller is accessing the cache and is generated by the A0 Clock output from the PAL. HDA0 is used to develop Buffer Chip Enable High-0 (BCEH-0) and Buffer Chip Enable Low-0 (BCEL-0), which are the chip select signals for the high and low bytes of the cache RAM. HDA0 is toggled high and low to read or write the high and low bytes of the cache.

HDGCLK-1 Hard Disk Go Clock-1 is a 400-kHz clock that is ANDed with MULT-1 by the PAL. In the multiple-sector mode, this clock informs the controller that the buffer is always ready (HDBRDY-1).

MULT-1 Multiple Sector-1 is input to the PAL from the Hard Disk Control register. This signal is asserted by the host in order to perform a multiple sector data transfer. This transfer is possible since the disk data cache can store up to 8 sectors. The assertion of MULT-1 stops the counter from being cleared (by disabling the Counter Clear-1 output from the PAL).

IA4 Internal Address, bit 4 is asserted to the PAL, along with other signals when the host is ready to write to the Hard Disk Control register.

HDBUF-0 Hard Disk Buffer-0 is asserted by the system I/O decoder (U4270) of the system control block. This signal is asserted during all cache data transfers initiated by the host and also enables the hard disk interface octal bus transceivers U6080 and U6090.

HDISK-0 Hard Disk-0 is asserted by the system I/O decoder U4270 when the host is accessing the disk controller. This signal also enables the single octal bus transceiver U6080.

DDIN-0 Data Direction In-0 is input from the host and is low when data is transferred from the hard disk interface to the host. This signal also enables the direction inputs to the octal bus transceivers U6080 and U6090.

DSTB-0 Data Strobe-0 is developed from the Read-0 and Write-0 signals output by the Timing Control Unit.

MNCLR-0 Manual Clear-0 is a counter-clear bit from the Hard Disk Control register. This bit is written by the host.

MNRDY-1 Manual Ready-1 is from the Hard Disk Control register and is written by the host. For single-sector transfers, this bit causes the PAL to output Hard Buffer Ready-0 to the disk controller, informing the controller that the cache is ready to be read from or written to.

HDBRDY-0 Hard Disk Buffer Ready-0 is output by the PAL to inform the controller that the cache may be written to or read from.

A0CLK-1 Address 0 Clock-1 is toggled by the PAL during a disk-controller access of the cache, in order increment bit 0 of the Hard Disk Address 0. This action allows the PAL to alternately enable the high and low-byte RAMs of the cache (BCEH-0 and BCEL-0).

BUFSEL-0 Buffer Select is output low when the host is accessing the cache. This signal is not externally connected but is used inside the PAL to develop CCLK-0.

HDREG-0 Hard Disk register-0 is output by the PAL and clocks the Hard Disk Control register on the trailing edge of the signal. This action occurs when the host is writing to the register.

HDRE-0 Hard Disk Read-0 is asserted by the PAL whenever the host is performing a read of the disk controller's internal registers, or of the cache. This signal is also asserted by the hard disk controller when the controller is reading from the cache.

HDWE-0 Hard Disk Write-0 is asserted by the PAL whenever the host is performing a write to the disk controller's internal registers, or to the cache. This signal is also asserted by the hard disk controller when the controller is writing to the cache.

BCEH-0 Buffer Chip Enable High-0 is output by the PAL to enable the high byte RAM. This signal is asserted when the host or disk controller is performing a read or write of the cache. During a host access of the

cache, this signal is asserted coincidentally with Buffer Chip Enable Low-0, since the host data bus structure is 16-bits wide. Conversely, during a disk controller access of the cache, the high and low bytes must be multiplexed or demultiplexed with the contoller's 8-bit data bus, and BCEH-0 and BCEL-0 are asserted alternately.

BCEL-0 Buffer Chip Enable Low-0 is output by the PAL to enable the low byte RAM. This signal is asserted when the host or disk controller is performing a read or write of the cache. See the previous description of BCEH-0.

CCLK-0 Counter Clock-0 is output by the PAL and asserted to increment the cache address counter, either during a disk controller access or a host access of the cache.

CCLR-1 Counter Clear-1 is output by the PAL to clear the cache-address counter. This is performed in advance of a single-sector access of the cache. During multisector transfers, CCLR-1 is disabled in order to keep from overwriting data.

Table 6-16 defines the Boolean expressions that govern the operation of PAL U8050. In Table 6-16, the bar or lack of a bar does not indicate logic convention. Rather, the bar over the signal name is for troubleshooting purposes only and indicates that the signal is at a low voltage level (0 volts). A signal name without the bar indicates only that the signal is at a high voltage level (+5 volts).

Table 6-16
PAL EQUATIONS FOR U8050

PAL Ouput	PAL Input States That Enable Output
$\overline{HDRE}$	$=\overline{DSTB}*DDIN*\overline{HDISK}$ $+\overline{DSTB}*\overline{DDIN}*\overline{HDBUF}$ (equation is true only if HDBCS is high, otherwise HDRE is tristated)
$\overline{HDWE}$	$=\overline{DSTB}*DDIN*\overline{HDISK}$ $+\overline{DSTB}*\overline{DDIN}*\overline{HDBUF}$ (equation is true only if HDBCS is high, otherwise HDWE is tristated)
$\overline{BCEH}$	$=\overline{HDBUF}*HDBCS$ $+HDA0*\overline{HDBCS}$
$\overline{BCEL}$	$=\overline{HDBUF}*HDBCS$ $+\overline{HDA0}*\overline{HDBCS}$
$\overline{CCLK}$	$=BUFSEL*\overline{HDBCS}$ $+BUFSEL*\overline{HDA0}$ $+HDBCS*DSTB$
$\overline{CCLR}$	$=HDBCR*MNCLR$ $+MULT*MNCLR$
$\overline{A0CLK}$	$=\overline{HDRE}*\overline{HDBCS}$ $+\overline{HDWE}*\overline{HDBCS}$
$\overline{HDREG}$	$=IA4*\overline{HDISK}*DDIN*\overline{DSTB}$
$\overline{HDBRDY}$	$=MNRDY+HDGCLK*MULT$
$\overline{BUFSEL}$	$=\overline{HDBUF}*\overline{DSTB}$

the system control decoders. This causes the LAN controller to copy the contents of the control block into internal memory and execute the command. The controller signals the completion of the transfer by asserting an interrupt to the host. The LAN controller is a bus master of the IA/D bus and most of the DMA transfers are executed with the LAN directly accessing system RAM. The LAN interface is tested via the System Control register. Clearing the LAN Loopback bit in the System Control register asserts the Loopback-0 signal (LBBK-0) to the serial interface chip (U9370) for testing.

The 82586 controller performs the encoding/decoding of the transmitted/received frames, and provides the electrical interface for the Ethernet transceiver cable. More information about this interface is available in the Memory Map section of this document.

INTERRUPT CONTROL

Refer to page A2-13 of the schematic diagrams. The Interrupt Control Unit (ICU) and associated logic provide interrupt management for the CPU. This logic handles 16 prioritized interrupt sources from the various intelligent I/O devices within the system. Six interrupt lines are reserved for devices installed in the backplane and one line is assigned to the display. The remaining channels are assigned to I/O devices on the computer board. The ICU resolves interrupt priorities and issues a byte-wide interrupt vector to the CPU.

EXTERNAL BUS INTERFACE

Refer to page A2-12 of the schematic diagrams. This block provides the interface between the Interal Address/Data bus and the External bus. The block consists of primarily of a Bus Interface Control PAL (U6290), six octal D-type latches used as bus buffers, Bus Time-out logic, and associated logic.

Bus Interface Control PAL

The Bus Interface Control PAL monitors various system status and control signals and controls the direction and enable signals required to control the bus buffers. Figure 6-11 shows the signal name and pin correspondence for the Bus Interface Control PAL (U6290), followed by a description of each of the signals and their functions.

TIMOUT-1	This is an input from the bus time-out counter U6301A and signals an External bus time-out.
ROMSEL-0	ROM Select-0 is asserted by the computer board ROM address decode logic and indicates that kernel ROM has been addressed.
KBEN-0	Kernel Bus Enable-0 is output by the PAL to enable octal bus transceivers U5160, U5190, and U6160, which provide buffering between the Kernel Address Data bus and the Internal Address bus.
KBDIR-1	Kernel Bus Direction-1 is output by the PAL to enable the bus transceivers decribed previously to place the contents of the Kernel Address/Data bus onto the Internal Address/Data bus.
EBOUT-1	External bus Out-1 is output by the PAL to output-enable the 3 octal D-type latches U0180, U2180, and U3180, thereby placing the contents of the Internal Address/Data bus onto the External bus.
LANDN-0	LAN Done-0 is asserted by the LAN interface when the interface has nearly completed performing a DMA operation.
LANBOOT-0	LANBOOT-0 is asserted by the System Control block decoders. This signal enables the LAN to access the ROM at the top of the memory space (FF FFF6-FF FFFF) for initialization purposes.
TSO-0	The leading edge of Timing State Output-0 signals the start of the second T-state for the TCU and the trailing edge signals the start of the last T-state. Used for timing purposes.
DREG-0	Diagnostic register is asserted by the System Control block I/O decoders. This signal selects the register for a read or write cycle.
ENDIOW-0	End I/O Wait-0 is asserted by the PAL to end the wait state that is entered automatically when the bus time-out counter (U6301A) begans incrementing.

Table 6-17 provides the Boolean expressions that govern the operation of PAL U6290. In Table 6-17, a bar or lack of a bar over a signal name does not indicate logic convention. Rather, a bar over a signal is for troubleshooting purposes only and indicates a low voltage level (0 volts). A signal name without the bar indicates a high voltage level (+5 volts).

which is the Q output of the Bus Time-out flip-flop (U6300A). BUSTO-0 is the Q bar output of flip-flop U6300A and disables the DMA Arbitration PAL U1230. A bus time-out is cleared by a system reset or automatically after an additional 10-microsecond wait.

The complete bus time-out cycle takes about 20 microseconds. Ten microseconds are allotted for the faulty DMA device to release the bus after the associated bus grant signal has been deasserted by the host.

DMA ARBITRATION

Refer to page A2-2 of the schematic diagrams. This functional block performs DMA arbitration for the six available External bus backplane slots, and the computer board-based LAN port and flexible disk drive interface. Each bus-request line is weighted at a particular priority level. Simultaneous bus requests are arbitrated according to the priority level assigned to each request line and a bus-grant signal is issued to the arbitrated requester. This block also generates a 4-bit code (via the 74LS140 8-to-3 line encoder U70) that is loaded into the System Status register and indicates the most recently used DMA channel. This code is used after a bus time-out to identify the faulty DMA device.

DMA Arbitration PAL

DMA arbitration is performed by a 24-pin DMA Arbitration PAL (U1230) and associated logic. The PAL monitors the various prioritized bus-request signals from the External bus expansion boards, the flexible disk DMA controller, and the LAN interface, and issues a bus grant to the highest-priority requester.

Figure 6-12 shows the signal name and signal correspondence for the DMA Arbitration PAL U1230, followed by a description of each of the signals and their functions.

DMAE-1 DMA Enable-1 is a bit set in the System Control register to allow devices other than the CPU to gain mastership of the External bus.

KHOLD-0 Kernel Hold-0 is asserted by the DMA Arbitration block when a non-kernel device is requesting mastership of the bus, including the External bus, the Internal Address/Data bus, and the Kernel bus. The method that KHOLD-0 is asserted depends on the revision level of the CPU. The H3 and K revisions of the NS32016 CPU requires KHOLD-0 be controlled by the flip-flop consisting of NAND gates U0260A and U0260D. Other revisions let the PAL U1230 control the KHOLD-0 signal.

DSKG-0 Disk Grant-0 is asserted by the PAL to grant the bus to the hard disk DMA controller.

LANG-0 LAN Grant-0 is asserted by the PAL to grant the bus to the LAN interface.

EBG1-0 External Bus Grant 1-0 is asserted by the PAL to grant the bus to the device present in slot 1 of the External bus backplane.

EBG2-0 External Bus Grant 2-0 is asserted by the PAL to grant the bus to the device present in slot 2 of the External bus backplane.

EBG3-0 External Bus Grant 3-0 is asserted by the PAL to grant the bus to the device present in slot 3 of the External bus backplane.

EBG4-0 External Bus Grant 4-0 is asserted by the PAL to grant the bus to the device present in slot 4 of the External bus backplane.

EBG5-0 External Bus Grant 5-0 is asserted by the PAL to grant the bus to the device present in slot 5 of the External bus backplane.

EBG6-0 External Bus Grant 6-0 is asserted by the PAL to grant the bus to the device present in slot 6 of the External bus backplane.

EDMA-1 Expansion DMA-1 is asserted to indicate that the device granted the bus is a backplane-resident device using the External bus. This signal is used to enable the line drivers that pass the bus protocol control signals between the system bus structures and the External bus.

OC Output Control is tied low to output-enable the PAL itself, as well as the bus-request flip-flop U2230.

Table 6-18 provides the Boolean expressions that govern the operation of PAL U1230. A bar or lack of a bar over the signal name below does not indicate logic convention. Rather, a bar over the signal name is for troubleshooting purposes only and indicates a low voltage level (0 volts). A signal name without the bar indicates a high voltage level (+5 volts).

Table 6-18 (cont.)
PAL EQUATIONS FOR U1230

PAL Output	Pal Input States That Enable Output
$\overline{EBG5}$	$:=\overline{KHLDAO}*\overline{EBR5}*DMAE*DKSDRQ*\overline{LANRQ}*EBR1$ $*EBR2*EBR3*EBR4*EBG6*EBG4*EBG3$ $*\overline{EBG2}*\overline{EBG1}*\overline{LANG}*DSKG$ $+\overline{KHLDAO}*\overline{EBR5}*\overline{EBG5}*DMAE$
$\overline{EBG6}$	$:=\overline{KHLDAO}*\overline{EBR6}*DMAE*DKSDRQ*\overline{LANRQ}*EBR1$ $*EBR2*EBR3*EBR4*\overline{EBR5}*EBG5*EBG4$ $*EBG3*EBG2*EBG1*\overline{LANG}*DSKG$ $+\overline{KHLDAO}*\overline{EBR6}*\overline{EBG6}*DMAE$
$\overline{EDMA}$	$=EBG1*EBG2*EBG3*EBG4*EBG5*EBG6$

CLOCK GENERATION

Refer to page A2-7 of the schematic diagrams. The clock generation logic develops most of the clock pulses required by the system. The primary clock source is a 20 MHz clock taken from a crystal oscillator. Three 74LS390 4-bit counters divide this pulse into a 10 MHz clock, a 1 MHz clock, an 80 kHz refresh clock, and a 200 Hz ICU clock. A secondary crystal oscillator operating at 16 MHz is used to develop an 8 MHz clock and a 4 MHz clock.

Reset Pulse Stretcher

Resets are generated by any device on the External bus, the power supply, and the Interrupt Control Unit. All resets pulses are expanded by 2 milliseconds by the pulse-stretching logic shown on page A2-7 of the schematic diagrams. This logic consists of binary counter U6301, quad NAND gate U6270 (shown in four locations), and inverter U6320. U6301 is employed as a flip-flop that is set when Received Reset-0 (RRSET-0) is first asserted. Two milliseconds later the counter U6301 resets the flip-flop, which deasserts External Reset-0. Reset signals from the ICU (INSANE-0) and power supply (PSINIT-0) are placed on the External Reset-0 path. This allows them to be input to the clock generator block as Received Reset-0, and the Reset Pulse Stretcher operates in the same fashion as described above.

TIME-OF-DAY CLOCK

Refer to page A2-8 of the schematic diagrams. This block consists of a MM58167 microprocessor-compatible real-time clock and a 32.768 kHz reference crystal oscillator. The clock contains a real-time counter, 56-bits of RAM, two interrupts, and a comparator. The RAM is used during power-down storage. Address interface

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
00779	AMP INC	P O BOX 3608	HARRISBURG PA 17105
00815	NORTHERN ENGINEERING LABORATORIES INC	357 BELOIT	BURLINGTON WI 53105
00853	SANGAMO WESTON INC SANGAMO CAPACITOR DIV	SANGAMO RD P O BOX 128	PICKENS SC 29671
01121	ALLEN-BRADLEY CO	1201 SOUTH 2ND ST	MILWAUKEE WI 53204
01295	TEXAS INSTRUMENTS INC SEMICONDUCTOR GROUP	13500 N CENTRAL EXPRESSWAY P O BOX 225012 M/S 49	DALLAS TX 75265
01807	PETERSEN RADIO CO INC	2800 WEST BROADWAY	COUNCIL BLUFFS IA 51501
01961	VARIAN ASSOCIATES INC PULSE ENGINEERING DIV	7250 CONVOY CT P O BOX 12235	SAN DIEGO CA 92112
03508	GENERAL ELECTRIC CO SEMI-CONDUCTOR PRODUCTS DEPT	W GENESEE ST	AUBURN NY 13021
04222	AVX CERAMICS DIV OF AVX CORP	19TH AVE SOUTH P O BOX 867	MYRTLE BEACH SC 29577
04713	MOTOROLA INC SEMICONDUCTOR GROUP	5005 E MCDOWELL RD	PHOENIX AZ 85008
05397	UNION CARBIDE CORP MATERIALS SYSTEMS DIV	11901 MADISON AVE	CLEVELAND OH 44101
05828	GENERAL INSTRUMENT CORP GOVERNMENT SYSTEMS DIV	600 W JOHN ST	HICKSVILLE NY 11802
07263	FAIRCHILD CAMERA AND INSTRUMENT CORP SEMICONDUCTOR DIV	464 ELLIS ST	MOUNTAIL VIEW CA 94042
07716	TRW INC TRW ELECTRONICS COMPONENTS TRW IRC FIXED RESISTORS/BURLINGTON	2850 MT PLEASANT AVE	BURLINGTON IA 52601
09353	C AND K COMPONENTS INC	15 RIVERDALE AVE	NEWTON MA 02158
09922	BURNDY CORP	RICHARDS AVE	NORWALK CT 06852
09969	DALE ELECTRONICS INC	EAST HIGHWAY 50 P O BOX 180	YANKTON SD 57078
11236	CTS OF BERNE INC	406 PARR ROAD	BERNE IN 46711
14752	ELECTRO CUBE INC	1710 S DEL MAR AVE	SAN GABRIEL CA 91776
18324	SIGNETICS CORP	811 E ARQUES	SUNNYVALE CA 94086
19701	MEPCO/ELECTRA INC A NORTH AMERICAN PHILIPS CO	P O BOX 760	MINERAL WELLS TX 76067
20932	EMCON INC	11620 SORRENTO VALLEY RD P O BOX 81542	SAN DIEGO CA 92138
20999	MINNESOTA MINING AND MFG CO INDUSTRIAL ELECTRICAL PRODUCTS DIV	3M CENTER	ST PAUL MN 55101
22526	DU PONT E I DE NEMOURS AND CO INC DU PONT CONNECTOR SYSTEMS	30 HUNTER LANE	CAMP HILL PA 17011
22929	DALE ELECTRONICS CORP FREQUENCY CONTROL GROUP	1155 W 23RD ST PO BOX 3164	TEMPE AZ 85282
24546	CORNING GLASS WORKS	550 HIGH ST	BRADFORD PA 16701
27014	NATIONAL SEMICONDUCTOR CORP	2900 SEMICONDUCTOR DR	SANTA CLARA CA 95051
27264	MOLEX INC CORPORATE HQ	2222 WELLINGTON COURT	LISLE IL 60532
29587	BUNKER RAMO CORP AMPHENOL INDUSTRIAL DIV	1830 S 54TH AVE	CHICAGO IL 60650
34335	ADVANCED MICRO DEVICES	901 THOMPSON PL	SUNNYVALE CA 94086
34649	INTEL CORP	3065 BOWERS AVE	SANTA CLARA CA 95051
52840	WESTERN DIGITAL CORP	3128 RED HILL AVE	COSTA MESA CA 92626
55680	NICHICON /AMERICA/ CORP	927 E STATE PKY	SCHAUMBURG IL 60195
56708	ZILOG INC	10460 BUBB RD	CUPERTINO CA 95014
58361	GENERAL INSTRUMENT CORP OPTOELECTRONICS DIV	3400 HILLVIEW AVE	PALO ALTO CA 94304
61892	NEC ELECTRONICS USA INC MICROCOMPUTER DIVISION ADVANCED CIRCUITS ENGINEERING	1 NATICK EXECUTIVE PARK	NATICK MA 01760
80009	TEKTRONIX INC	4900 S W GRIFFITH DR P O BOX 500	BEAVERTON OR 97077
TK1360	DALE ELECTRONICS INC	BOX 26950	EL PASO TX 79926

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A2C2120	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C2150	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C2160	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C2170	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C2180	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C2190	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C2230	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C2240	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C2260	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C2270	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C2290	283-0359-00			CAP,FXD,CER DI:1000PF,10%,200V	05397	C330C102K2G5CA
A2C2291	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C2310	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C2320	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C2330	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C2360	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C3020	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C3030	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C3040	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C3050	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C3060	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C3070	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C3080	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C3090	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C3100	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C3120	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C3140	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C3141	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C3150	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C3151	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C3160	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C3161	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C3170	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C3171	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C3260	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C3270	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C3320	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C3330	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C4140	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C4150	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C4160	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C4180	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C4190	290-1076-00			CAP,FXD,ELCTLT:47UF,20%,10V	55680	TLB10470M
A2C4191	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C4200	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C4220	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C4240	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C4250	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C4270	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C4290	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C4310	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C4320	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C4330	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C4340	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C4360	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C4375	283-0111-00			CAP,FXD,CER DI:0.1UF,20%,50V	05397	C330C104M5U1CA
A2C5010	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C5011	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C5020	290-1076-00			CAP,FXD,ELCTLT:47UF,20%,10V	55680	TLB10470M
A2C5040	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA

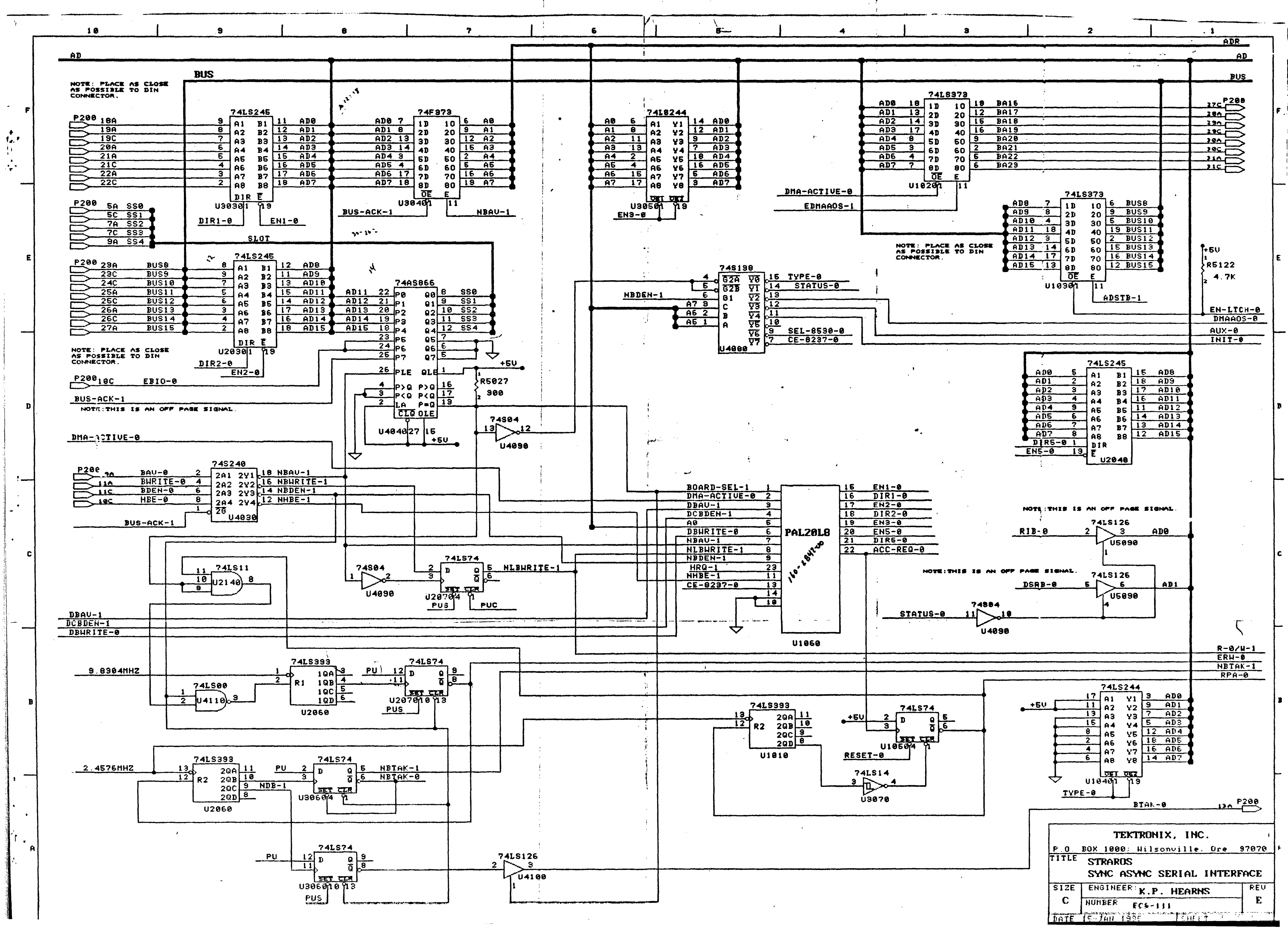
Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A2C8180	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C8181	283-0167-00			CAP,FXD,CER DI:0.1UF,10%,100V	04222	3430-100C-104K
A2C8190	283-0479-00			CAP,FXD,CER DI:0.47UF,+80-20%,25V	20932	501ES25DP474Z
A2C8240	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C8241	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C8260	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C8270	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C8330	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C8340	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C8360	281-0767-00			CAP,FXD,CER DI:330PF,20%,100V	04222	MA106C331MAA
A2C8361	281-0767-00			CAP,FXD,CER DI:330PF,20%,100V	04222	MA106C331MAA
A2C8362	281-0767-00			CAP,FXD,CER DI:330PF,20%,100V	04222	MA106C331MAA
A2C8364	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C9150	283-0479-00			CAP,FXD,CER DI:0.47UF,+80-20%,25V	20932	501ES25DP474Z
A2C9160	283-0479-00			CAP,FXD,CER DI:0.47UF,+80-20%,25V	20932	501ES25DP474Z
A2C9161	283-0631-00			CAP,FXD,MICA DI:95PF,1%,500V	00853	D155F950FD
A2C9180	285-1306-00			CAP,FXD,PLASTIC:1.0UF,1%,50V	14752	MC12B105F
A2C9230	281-0819-00			CAP,FXD,CER DI:33 PF,5%,50V	04222	GC105A330J
A2C9240	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C9241	281-0819-00			CAP,FXD,CER DI:33 PF,5%,50V	04222	GC105A330J
A2C9300	290-1076-00			CAP,FXD,ELCTLT:47UF,20%,10V	55680	TLB1A470M
A2C9350	283-0479-00			CAP,FXD,CER DI:0.47UF,+80-20%,25V	20932	501ES25DP474Z
A2CR6220	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A2CR6221	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A2CR7220	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A2CR7340	152-0066-00			SEMICOND DVC,DI:RECT,SI,400V,1A,DO-41	05828	GP10G-020
A2CR7341	152-0066-00			SEMICOND DVC,DI:RECT,SI,400V,1A,DO-41	05828	GP10G-020
A2CR8190	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A2CR9230	152-0066-00			SEMICOND DVC,DI:RECT,SI,400V,1A,DO-41	05828	GP10G-020
A2DL4160	119-1448-00			DELAY LINE,ELEC:200NS,TAPPED,14 DIP	01961	PE-21213-005
A2DL7130	119-1825-00			DELAY LINE,ELEC:60NS,TAPPED,14 DIP	00222	14TD60
A2DS3370	150-1037-00			LAMP,LED RDOUT:ORANGE,7 SEG,LH DECIMAL	58361	Q3409/MAN3620A
A2J150	131-3196-00			CONN,RCPT,ELEC:CKT BD,18PIN,LOCKING	27264	09-80-1183
A2J151	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 3)	22526	48283-036
A2J152	131-0812-00			CONN,RCPT,ELEC:CKT BD MT,25 CONT,FEMALE	00779	205858-1
A2J153	131-0812-00			CONN,RCPT,ELEC:CKT BD MT,25 CONT,FEMALE	00779	205858-1
A2J154	131-3168-00			CONN,RCPT,ELEC:CKT BD,RTANG,2 X 12,0.085 SP ACING	29587	57-92245-12
A2J155	131-2248-00			CONN,RCPT,ELEC:CIRCUIT BOARD,15 FEMALE	00779	205868-1
A2J160	131-3186-00			CONN,PLUG,ELEC:MALE,3 X 32,0.1 SPACING	09922	RPI9683P4T02Z1
A2J180	131-2963-00			CONN,RCPT,ELEC:MALE,3 X 32,0.1 CTR	00779	532523-1
A2J240	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 2)	22526	48283-036
A2J241	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 2)	22526	48283-036
A2J242	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 2)	22526	48283-036
A2J243	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 2)	22526	48283-036
A2J250	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 2)	22526	48283-036
A2J1170	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 2)	22526	48283-036
A2J5290	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 3)	22526	48283-036
A2J5291	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 3)	22526	48283-036
A2P190	131-3187-00			CONN,RCPT,ELEC:CKT BD,HEADER,2 X 10	20999	3428-6002
A2P191	131-3188-00			CONN,RCPT,ELEC:CKT BD,HEADER,2 X 17	20999	3431-6002
A2P192	131-3188-00			CONN,RCPT,ELEC:CKT BD,HEADER,2 X 17	20999	3431-6002

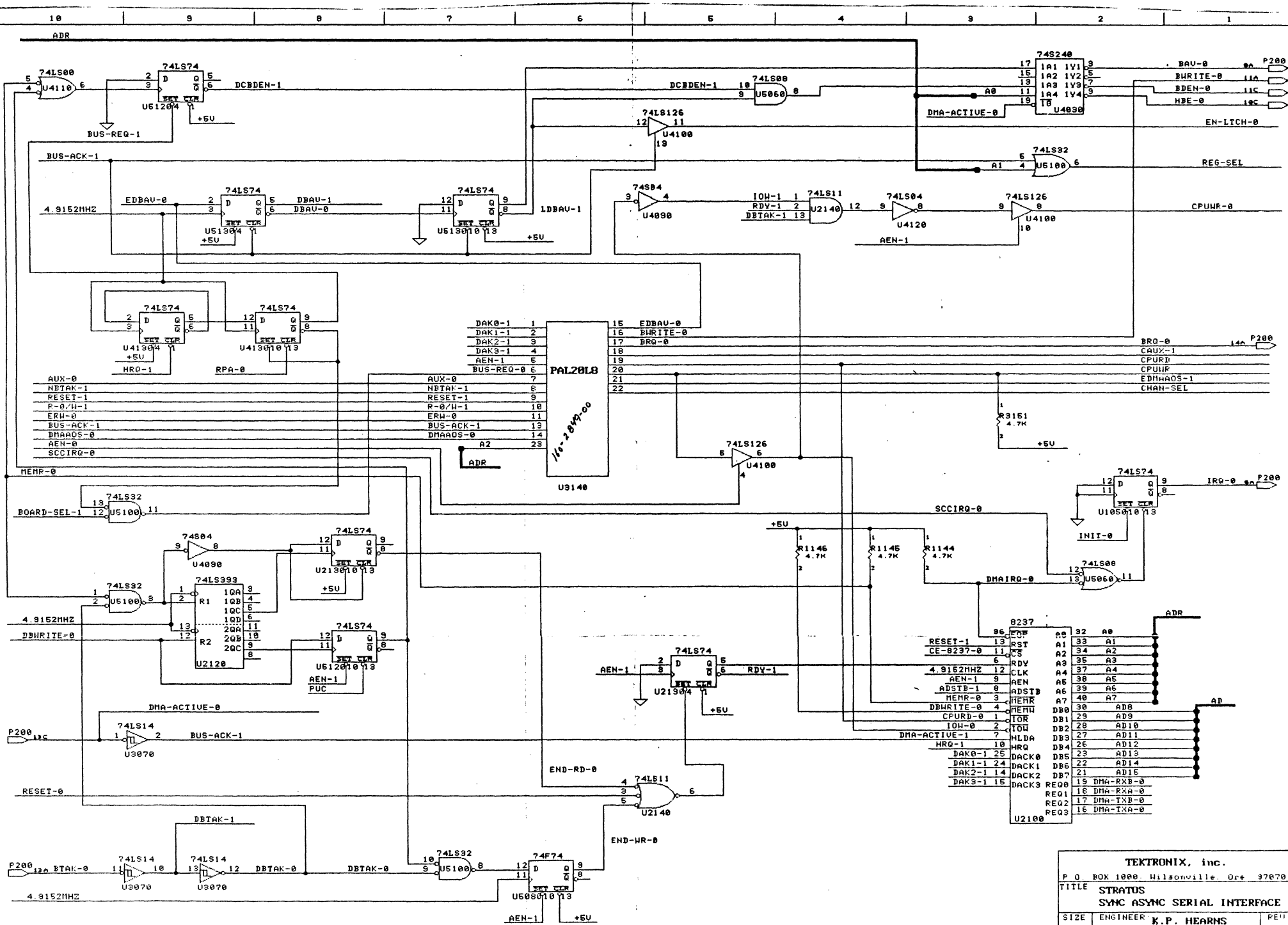
Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A2R8010	315-0102-00			RES,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A2R8060	315-0103-00			RES,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A2R8120	315-0102-00			RES,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A2R8160	321-0258-01			RES,FXD,FILM:4.75K OHM,0.5%,0.125W,TC=T0	01121	ADVISE
A2R8161	321-0210-00			RES,FXD,FILM:1.50K OHM,1%,0.125W,TC=T0	19701	5033ED1K50F
A2R8165	315-0472-00			RES,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A2R8170	321-0126-01			RES,FXD,FILM:200 OHM,0.5%,0125W	07716	CEA0200R0D
A2R8190	315-0471-00			RES,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A2R8250	315-0103-00			RES,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A2R8251	315-0471-00			RES,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A2R9050	315-0151-00			RES,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A2R9051	315-0151-00			RES,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A2R9052	315-0151-00			RES,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A2R9053	315-0151-00			RES,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A2R9140	315-0101-00			RES,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A2R9150	321-0193-00			RES,FXD,FILM:1K OHM,1%,0.125W,TC=T0	19701	5033ED1K00F
A2R9160	321-0210-00			RES,FXD,FILM:1.50K OHM,1%,0.125W,TC=T0	19701	5033ED1K50F
A2R9180	321-0114-01			RES,FXD,FILM:150 OHM,0.5%,0.125W,TC=T0	07716	CEA0150R0D
A2R9190	315-0181-00			RES,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
A2R9191	315-0103-00			RES,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A2R9230	315-0473-00			RES,FXD,CMPSN:47K OHM,5%,0.25W	01121	CB4735
A2R9231	315-0103-00			RES,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A2R9232	315-0103-00			RES,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A2R9233	315-0103-00			RES,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A2R9280	315-0102-00			RES,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A2R9330	315-0102-00			RES,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A2R9331	315-0103-00			RES,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A2R9340	321-0105-00			RES,FXD,FILM:121 OHM 1%,0.125W,TC=\0	07716	CEA0121R0F
A2R9341	315-0103-00			RES,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A2R9342	321-0105-00			RES,FXD,FILM:121 OHM 1%,0.125W,TC=\0	07716	CEA0121R0F
A2R9343	315-0103-00			RES,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A2R9344	315-0103-00			RES,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A2R9351	315-0102-00			RES,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A2R9352	315-0132-00			RES,FXD,CMPSN:1.3K OHM,5%,0.25W	01121	CB1325
A2R9353	315-0132-00			RES,FXD,CMPSN:1.3K OHM,5%,0.25W	01121	CB1325
A2R9354	315-0302-00			RES,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
A2R9355	315-0302-00			RES,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
A2R9356	315-0390-00			RES,FXD,CMPSN:39 OHM,5%,0.25W	01121	CB3905
A2R9357	315-0390-00			RES,FXD,CMPSN:39 OHM,5%,0.25W	01121	CB3905
A2R9358	315-0390-00			RES,FXD,CMPSN:39 OHM,5%,0.25W	01121	CB3905
A2R9359	315-0390-00			RES,FXD,CMPSN:39 OHM,5%,0.25W	01121	CB3905
A2RP190	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9)RES	11236	750101R4.7KOHM
A2RP360	307-0446-00			RES NTWK,FXD,FI:10K OHM,20%,(9)RES	11236	750101R10K
A2RP1250	307-0675-00			RES NTWK,FXD,FI:9,1K OHM,2%1.25W	11236	750101R1KOHM
A2RP2100	307-1104-00			RES NTWK,FXD,FI:27 OHM,5%,16 PIN ISOLATED	TK1360	MDP1603-270J
A2RP3250	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9)RES	11236	750101R4.7KOHM
A2RP4190	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9)RES	11236	750101R4.7KOHM
A2RP4191	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9)RES	11236	750101R4.7KOHM
A2RP4220	307-0541-00			RES NTWK,FXD,FI:(7)1K OHM,10%,1W	01121	108A102
A2RP4370	307-0992-00			RES NTWK,FXD,FI:8,330 OHM,5%	09969	CSC08A03-331J
A2RP4371	307-0992-00			RES NTWK,FXD,FI:8,330 OHM,5%	09969	CSC08A03-331J
A2RP8080	307-0594-00			RES NTWK,FXD,FI:7,220 OHM,2%,1.0W	11236	75081R220
A2RP8090	307-0598-00			RES NTWK,FXD,FI:7,330 OHM,2%,1.0W	11236	75081R330
A2S380	260-2237-00			SWITCH,SLIDE:SPST,100MA,50VAC	09353	BD08-AV
A2TP220	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A2TP225	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A2TP270	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A2TP280	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A2TP300	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A2TP305	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A2U1280	156-2033-01			MICROCKT,DGTL:MICROPROCESSOR,16 BIT CPU	27014	NS32016-8NA+
A2U1300	156-2035-01			MICROCKT,DGTL:MEMORY MANAGEMENT UNIT	27014	NS32082-8NA+
A2U1320	156-1722-00			MICROCKT,DGTL:HEX INVERTER,SCRN	04713	MC74F04(NDORJD)
A2U1330	156-1724-00			MICROCKT,DGTL:QUAD 2 INPUT OR GATE,SCRN	04713	74F32(ND OR JD)
A2U1360	156-1414-02			MICROCKT,DGTL:OCTAL GPIB BUS XCVR,SCRN	27014	DS75160A(NORJ)A+
A2U2010	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM (6110 ONLY)	04713	MCM6665-AP-15
A2U2010	156-2139-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (6120,6130 ONLY)	61892	UPD41256C-15
A2U2020	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM (6110 ONLY)	04713	MCM6665-AP-15
A2U2020	156-2139-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (6120,6130 ONLY)	61892	UPD41256C-15
A2U2030	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM (6110 ONLY)	04713	MCM6665-AP-15
A2U2030	156-2139-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (6120,6130 ONLY)	61892	UPD41256C-15
A2U2040	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM (6110 ONLY)	04713	MCM6665-AP-15
A2U2040	156-2139-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (6120,6130 ONLY)	61892	UPD41256C-15
A2U2050	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM (6110 ONLY)	04713	MCM6665-AP-15
A2U2050	156-2139-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (6120,6130 ONLY)	61892	UPD41256C-15
A2U2060	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM (6110 ONLY)	04713	MCM6665-AP-15
A2U2060	156-2139-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (6120,6130 ONLY)	61892	UPD41256C-15
A2U2070	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM (6110 ONLY)	04713	MCM6665-AP-15
A2U2070	156-2139-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (6120,6130 ONLY)	61892	UPD41256C-15
A2U2080	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM (6110 ONLY)	04713	MCM6665-AP-15
A2U2080	156-2139-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (6120,6130 ONLY)	61892	UPD41256C-15
A2U2090	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM (6110 ONLY)	04713	MCM6665-AP-15
A2U2090	156-2139-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (6120,6130 ONLY)	61892	UPD41256C-15
A2U2110	156-1962-00			MICROCKT,DGTL:OCTAL BUFFER/LINE DRIVER,SCRN	07263	74F244P
A2U2120	156-1962-00			MICROCKT,DGTL:OCTAL BUFFER/LINE DRIVER,SCRN	07263	74F244P
A2U2150	156-0382-02			MICROCKT,DGTL:QUAD 2 INP NAND GATE BURN	18324	N74LS00(N80RFB)
A2U2160	156-0388-03			MICROCKT,DGTL:DUAL D FLIP-FLOP,SCRN	01295	N74LS74ANP3ORJP4
A2U2170	156-1611-00			MICROCKT,DGTL:DUAL D TYPE EDGE-TRIGGERED FF	07263	74F74(PC OR DC)
A2U2180	156-1721-00			MICROCKT,DGTL:OCTAL TRANSPARENT LATCH W/3 S TATE OUT,ASTTL,SCRN	18324	74F373(NB OR FB)
A2U2190	156-2065-00			MICROCKT,DGTL:OCTAL D TYPE TRANS LATCHES W/ 3 STATE OUT,SCRN	01295	SN74AS373P3
A2U2230	156-1704-00			MICROCKT,DGTL:OCTAL D-TYPE FF W/3-STATE OUT	07263	74F374PCQR
A2U2240	156-0391-02			MICROCKT,DGTL:HEX LATCH W/CLEAR,SCRN	18324	N74LS174(N80RFB)
A2U2320	156-0966-01			MICROCKT,DGTL:DUAL 5 INP NOR GATES,SCRN	01295	SN74S260NP3
A2U2330	156-1723-00			MICROCKT,DGTL:QUAD 2 INPUT & GATE,SCRN	04713	MC74F08 ND OR JD
A2U2340	156-1444-01			MICROCKT,DGTL:NMOS,GPIB INTFC CONTROLLER	01295	TMS9914A(NLORJL)
A2U2360	156-1459-00			MICROCKT,DGTL:GPIB BUS MGT CKT	01295	SN75162A(N OR J)
A2U3010	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM (6110 ONLY)	04713	MCM6665-AP-15
A2U3010	156-2139-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (6120,6130 ONLY)	61892	UPD41256C-15
A2U3020	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM (6110 ONLY)	04713	MCM6665-AP-15
A2U3020	156-2139-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	61892	UPD41256C-15

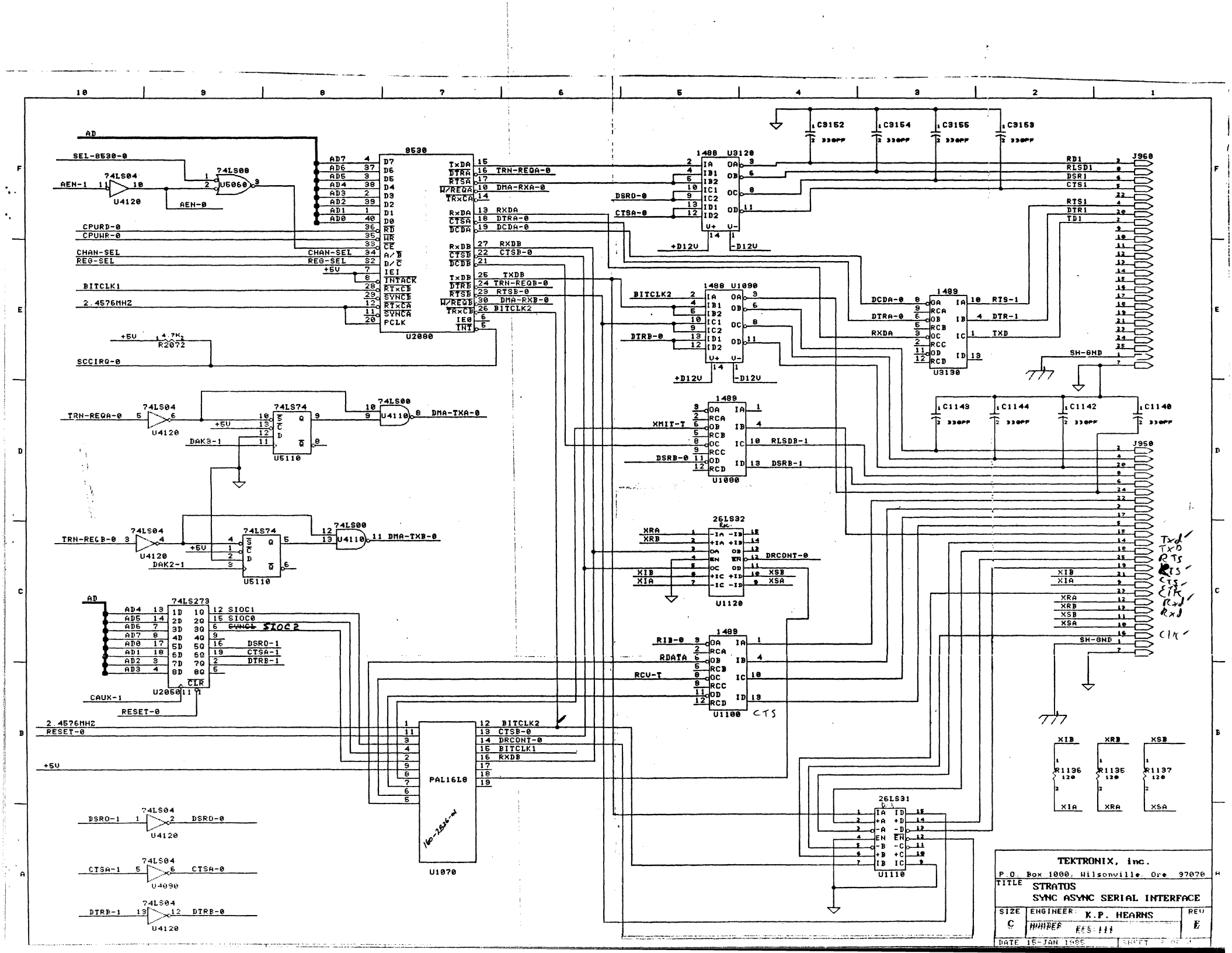
Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A2U4040	156-2139-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (6120,6130 ONLY)	61892	UPD41256C-15
A2U4050	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM (6110 ONLY)	04713	MCM6665-AP-15
A2U4050	156-2139-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (6120,6130 ONLY)	61892	UPD41256C-15
A2U4060	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM (6110 ONLY)	04713	MCM6665-AP-15
A2U4060	156-2139-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (6120,6130 ONLY)	61892	UPD41256C-15
A2U4070	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM (6110 ONLY)	04713	MCM6665-AP-15
A2U4070	156-2139-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (6120,6130 ONLY)	61892	UPD41256C-15
A2U4080	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM (6110 ONLY)	04713	MCM6665-AP-15
A2U4080	156-2139-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (6120,6130 ONLY)	61892	UPD41256C-15
A2U4090	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM (6110 ONLY)	04713	MCM6665-AP-15
A2U4090	156-2139-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (6120,6130 ONLY)	61892	UPD41256C-15
A2U4100	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM (6110 ONLY)	04713	MCM6665-AP-15
A2U4100	156-2139-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (6120,6130 ONLY)	61892	UPD41256C-15
A2U4110	156-1216-01			MICROCKT,DGTL:QUAD 2 INP NAND BFR,SCRN	01295	SN74S37JP4
A2U4120	156-1707-00			MICROCKT,DGTL:QUAD 2-INPUT NAND GATE,SCRN	04713	74F00 (ND OR JD)
A2U4140	156-0479-02			MICROCKT,DGTL:QUAD 2-INP OR GATE,SCRN,	18324	N74LS32(NBORFB)
A2U4150	156-0480-02			MICROCKT,DGTL:QUAD 2-INP & GATE,SCRN,	18324	N74LS08(NBORFB)
A2U4170	156-0479-02			MICROCKT,DGTL:QUAD 2-INP OR GATE,SCRN,	18324	N74LS32(NBORFB)
A2U4220	156-1663-00			MICROCKT,DGTL:ASTTL,TPL 3-INP & GATE	04713	MC74F11ND/JD
A2U4250	156-0469-02			MICROCKT,DGTL:3/8 LINE DCDR,SCRN,74LS138,MI	18324	N74LS138(NBORFB)
A2U4270	156-1727-00			MICROCKT,DGTL:1 OF 8 DCDR/DMUX,SCRN	04713	MC74F138 ND/JD
A2U4280	160-2650-00			MICROCKT,DGTL:16384 X 8 EPROM,PROGRAMMED	80009	160-2650-00
A2U4300	160-2922-01			MICROCKT,DGTL:16384 X 8 EPROM,PRGM (6110 ONLY)	80009	160-2922-01
A2U4300	160-2922-02			MICROCKT,DGTL:16384 X 8,EPROM PRGM (6120/6130 ONLY)	80009	160-2922-02
A2U4320	156-1752-00			MICROCKT,DGTL:TRIPLE 3-INPUT NAND GATE,SCRN	18324	74F10 (NB OR FB)
A2U4330	156-1611-00			MICROCKT,DGTL:DUAL D TYPE EDGE-TRIGGERED FF	07263	74F74(PC OR DC)
A2U4340	156-0865-02			MICROCKT,DGTL:OCTAL D FF W/CLEAR,SCRN	18324	N74LS273(NBORFB)
A2U4360	156-0878-01			MICROCKT,DGTL:QUAD LINE RCVR,SCREENED	04713	MC1489LDS
A2U5020	156-1721-00			MICROCKT,DGTL:OCTAL TRANSPARENT LATCH W/3 STATE OUT,ASTTL,SCRN	18324	74F373(NB OR FB)
A2U5021	156-1065-01			MICROCKT,DGTL:OCTAL D TYPE TRANS LATCHES	04713	SN74LS373 ND/JD
A2U5050	156-2039-00			MICROCKT,DGTL:9-BIT PARITY GENERATOR/CHECKER,SCRN	07263	74F280PCQR
A2U5051	156-0479-02			MICROCKT,DGTL:QUAD 2-INP OR GATE,SCRN,	18324	N74LS32(NBORFB)
A2U5080	156-1721-00			MICROCKT,DGTL:OCTAL TRANSPARENT LATCH W/3 STATE OUT,ASTTL,SCRN	18324	74F373(NB OR FB)
A2U5081	156-1065-01			MICROCKT,DGTL:OCTAL D TYPE TRANS LATCHES	04713	SN74LS373 ND/JD
A2U5100	156-2039-00			MICROCKT,DGTL:9-BIT PARITY GENERATOR/CHECKER,SCRN	07263	74F280PCQR
A2U5110	156-1721-00			MICROCKT,DGTL:OCTAL TRANSPARENT LATCH W/3 STATE OUT,ASTTL,SCRN	18324	74F373(NB OR FB)
A2U5140	156-0865-02			MICROCKT,DGTL:OCTAL D FF W/CLEAR,SCRN	18324	N74LS273(NBORFB)
A2U5150	156-1065-01			MICROCKT,DGTL:OCTAL D TYPE TRANS LATCHES	04713	SN74LS373 ND/JD
A2U5160	156-1748-02			MICROCKT,DGTL:OCTAL BUS XCVR W/3-STATE OUT, SCRN	01295	SN74ALS245AN3/J4
A2U5180	156-1721-00			MICROCKT,DGTL:OCTAL TRANSPARENT LATCH W/3 STATE OUT,ASTTL,SCRN	18324	74F373(NB OR FB,

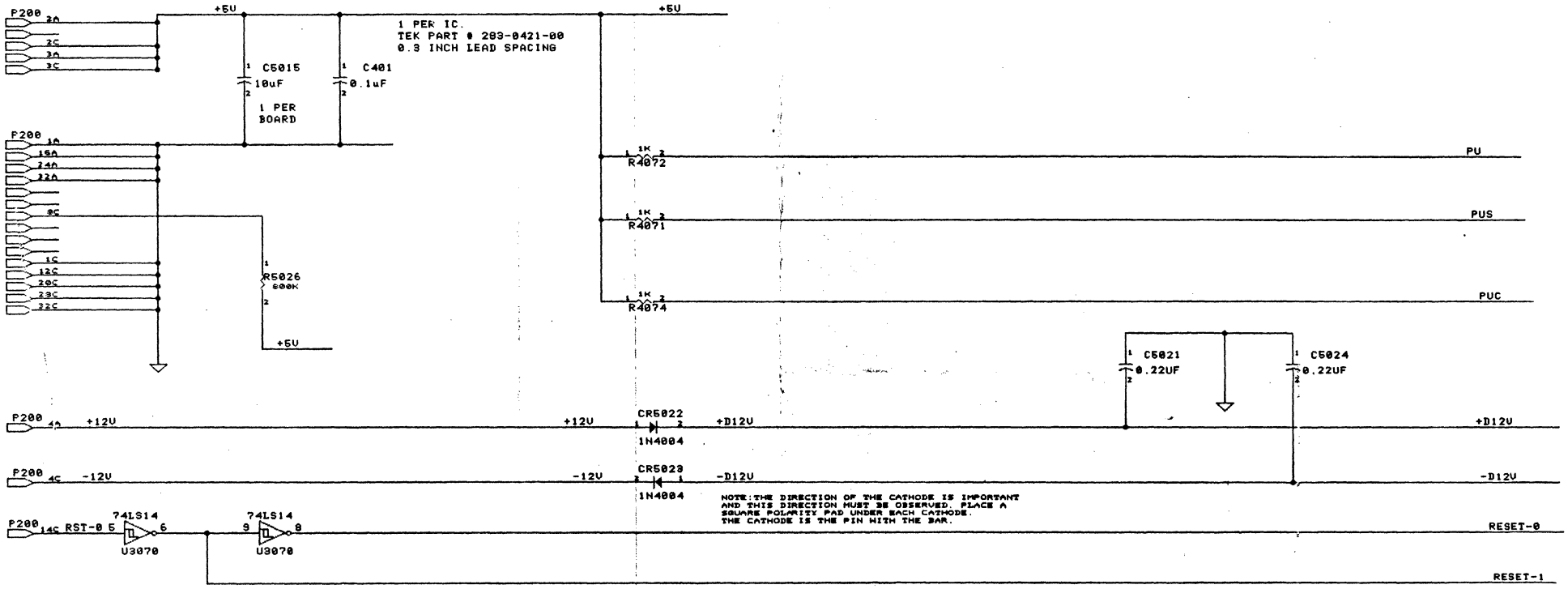
Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A2U8120	156-1681-00			MICROCKT,DGTL:QUAD DIFF LINE DRIVER,SCRN	34335	AM26LS31DCB
A2U8150	156-1611-00			MICROCKT,DGTL:DUAL D TYPE EDGE-TRIGGERED FF	07263	74F74(PC OR DC)
A2U8230	156-1601-00			MICROCKT,DGTL:CMOS,RT CLOCK CALENDAR W/3 ST ATE OUT	27014	MM58167A(N OR D)
A2U8240	156-0391-02			MICROCKT,DGTL:HEX LATCH W/CLEAR,SCRN	18324	N74LS174(N80RFB)
A2U8260	156-0385-02			MICROCKT,DGTL:HEX INVERTER,SCRN,74LS04,MI	18324	N74LS04(N80RFB)
A2U8270	156-1373-01			MICROCKT,DGTL:QUAD BUS BFR GATES W/3 STATE OUT,SCREENED	01295	SN74LS125N3ORJ4
A2U8290	156-2080-00			MICROCKT,DGTL:DMA CONTROLLER,SCREENED	34335	AM9516NB/JB
A2U8310	156-2043-00			MICROCKT,DGTL:LAN,SCRN	34649	QC82586
A2U8330	156-2027-00			MICROCKT,DGTL:CMOS,HEX INVERTER	27014	MM74HC04(NORJ)
A2U9140	156-1315-00			MICROCKT,INTFC:QUAD DIFF RCVR,SCRN	27014	DS26LS32NA+JA+
A2U9170	156-2030-01			MICROCKT,DGTL:DATA SEPATATOR,SCRN	27014	DP8460-4N
A2U9240	156-2029-00			MICROCKT,DGTL:NONVOLATILE STSTIC RAM,SCRN	80009	156-2029-00
A2U9260	156-1707-00			MICROCKT,DGTL:QUAD 2-INPUT NAND GATE,SCRN	04713	74F00 (ND OR JD)
A2U9270	156-1753-00			MICROCKT,DGTL:OCTAL BUFFER & LINE DRIVER W/ 3-STATE OUT,SCRN	01295	74LS240NP3ORJP4
A2U9330	156-1707-00			MICROCKT,DGTL:QUAD 2-INPUT NAND GATE,SCRN	04713	74F00 (ND OR JD)
A2U9370	156-2246-00			MICROCKT,DGTL:MANCHESTER CODE CVTR,SCRN	61394	8023
A2W150	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A2W1130	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L (6120/6130 ONLY)	24546	OMA 07
A2W1131	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L (6110 ONLY)	24546	OMA 07
A2W1140	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L (6120/6130 ONLY)	24546	OMA 07
A2W1141	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L (6110 ONLY)	24546	OMA 07
A2W2130	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L (6120/6130 ONLY)	24546	OMA 07
A2W2131	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L (6110 ONLY)	24546	OMA 07
A2W2140	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L (6120/6130 ONLY)	24546	OMA 07
A2W2141	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L (6120/6130 ONLY)	24546	OMA 07
A2W2142	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L (6110 ONLY)	24546	OMA 07
A2W2143	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L (6110 ONLY)	24546	OMA 07
A2W8352	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A2Y6230	119-1413-00			OSC,XTAL CLOCK:20MHZ,0.05%	09969	XO-33-C-20
A2Y6240	119-1408-00			OSC,XTAL CLOCK:16MHZ,0.01%	22929	XO-33B16
A2Y6320	158-0124-00			XTAL UNIT,QTZ:2.4576 MHZ,0.05%,PARALLEL	01807	Z9N
A2Y9230	158-0253-00			XTAL UNIT,QTZ:32.768KHZ,0.01%,ANTIRESONANT	00815	NE-3355XY


TEKTRONIX, INC.
P.O. BOX 1000; Wilsonville, Ore 97070
TITLE STRAROS
SYNC ASYNC SERIAL INTERFACE
SIZE C
ENGINEER: K.P. HEARNS
NUMBER ECS-111
REV E
DATE 15-JAN 1986
NOTE: PLACE AS CLOSE AS POSSIBLE TO DIN CONNECTOR.
NOTE: THIS IS AN OFF PAGE SIGNAL.
PAL20L8



TEKTRONIX, inc.		
P O BOX 1000, Wilsonville, Ore 97070		
TITLE	STRATOS SYNC ASYNC SERIAL INTERFACE	
SIZE C	ENGINEER K.P. HEARNS	REV E
	NUMBER 685-111	

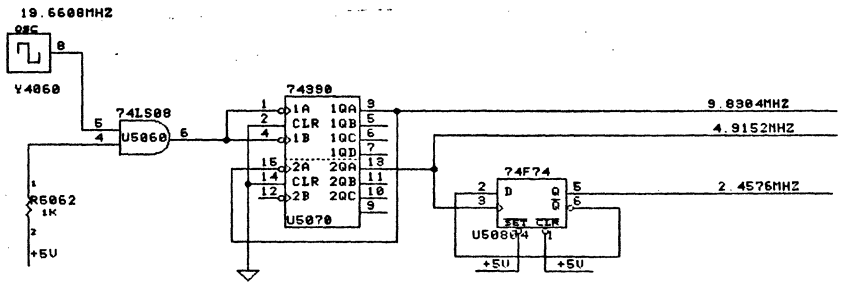

AD
SEL-8530-0
AEN-1
74LS04
U4120
74LS08
U5060
AEN-0
8530
U2080
CPURD-0
CPUWR-0
CHAN-SEL
REG-SEL
BITCLK1
2.4576MHZ
+5V
4.7K
R2072
SCCIRQ-0
TRN-REQA-0
DMA-RXA-0
RXDA
DTRA-0
DCDA-0
TXDB
TRN-REQB-0
RTSB-0
DMA-RXB-0
BITCLK2
CTSB-0
RXDB
DSRO-0
CTSA-0
DTRB-0
+D12V
-D12V
1488 U3120
1488 U1090
1489
U3130
U1000
U1120
U1100
U1110
C3152
C3154
C3155
C3153
C1149
C1144
C1142
C1140
330PF
RD1
RLSD1
DSR1
CTS1
RTS1
DTR1
TD1
J960
SH-GND
RTS-1
DTR-1
TXD
XMIT-T
RLSDB-1
DSRB-1
DMA-TXA-0
DMA-TXB-0
DAK3-1
DAK2-1
74LS74
U5110
74LS00
U4110
26LS32
DRCONT-0
XSB
XSA
XIB
XIA
XRA
XRB
74LS273
SIOC1
SIOC0
SYNC1
SIOC2
DSRO-1
CTSA-1
DTRB-1
CAUX-1
RESET-0
CLR
PAL16L8
160-2866-01
U1070
RIB-0
RDATA
RCV-T
26LS31
U1110
CTS
R1136
R1135
R1137
120
TEKTRONIX, inc.
P.O. Box 1000, Wilsonville, Ore 97070
TITLE
STRATOS
SYNC ASYNC SERIAL INTERFACE
SIZE
C
ENGINEER: K.P. HEARNS
NUMBER
REV
E
DATE 15-JAN 1985
SHEET



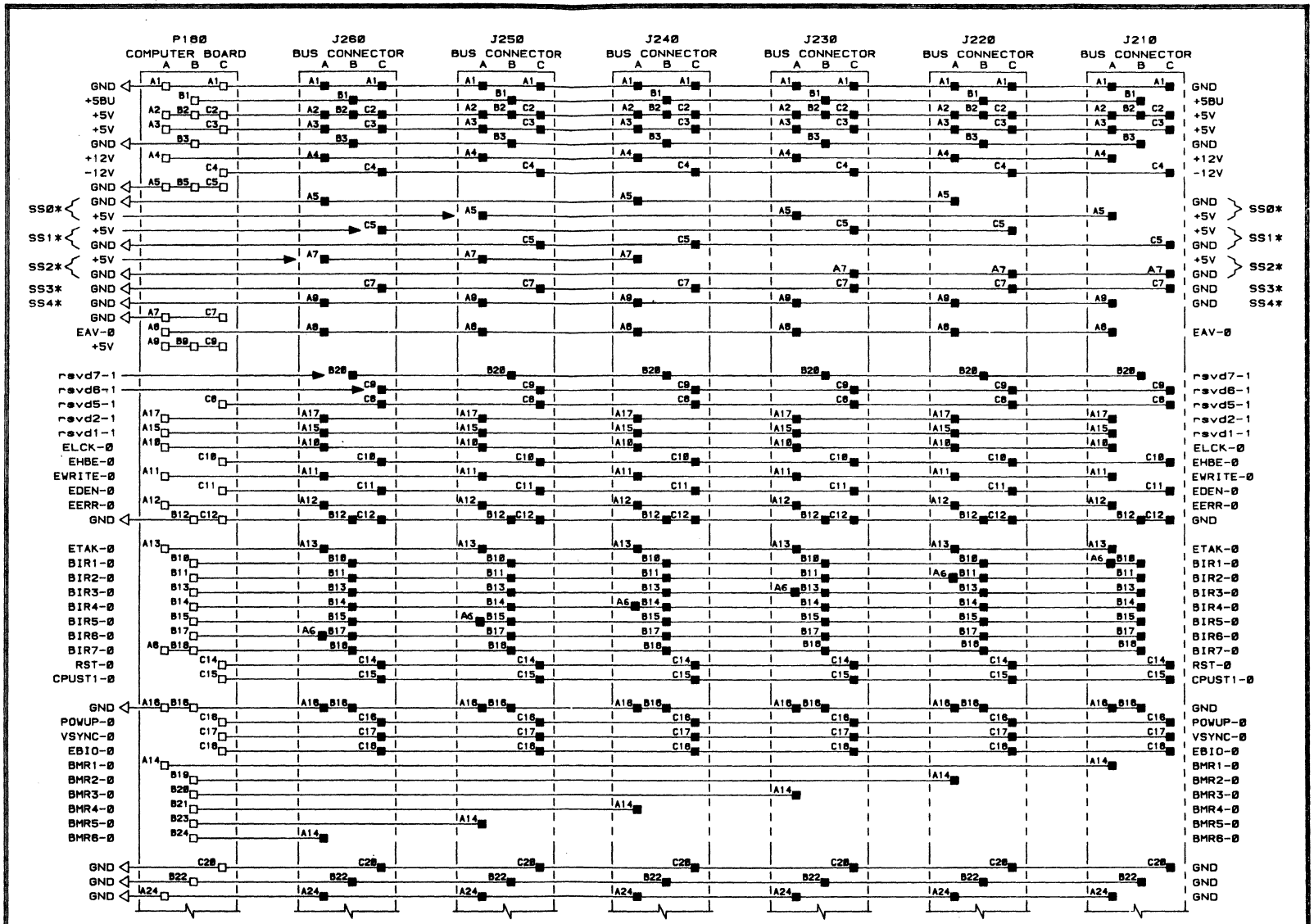
NOTE: THE DIRECTION OF THE CATHODE IS IMPORTANT AND THIS DIRECTION MUST BE OBSERVED. PLACE A SQUARE POLARITY PAD UNDER EACH CATHODE. THE CATHODE IS THE PIN WITH THE BAR.

NOTES:

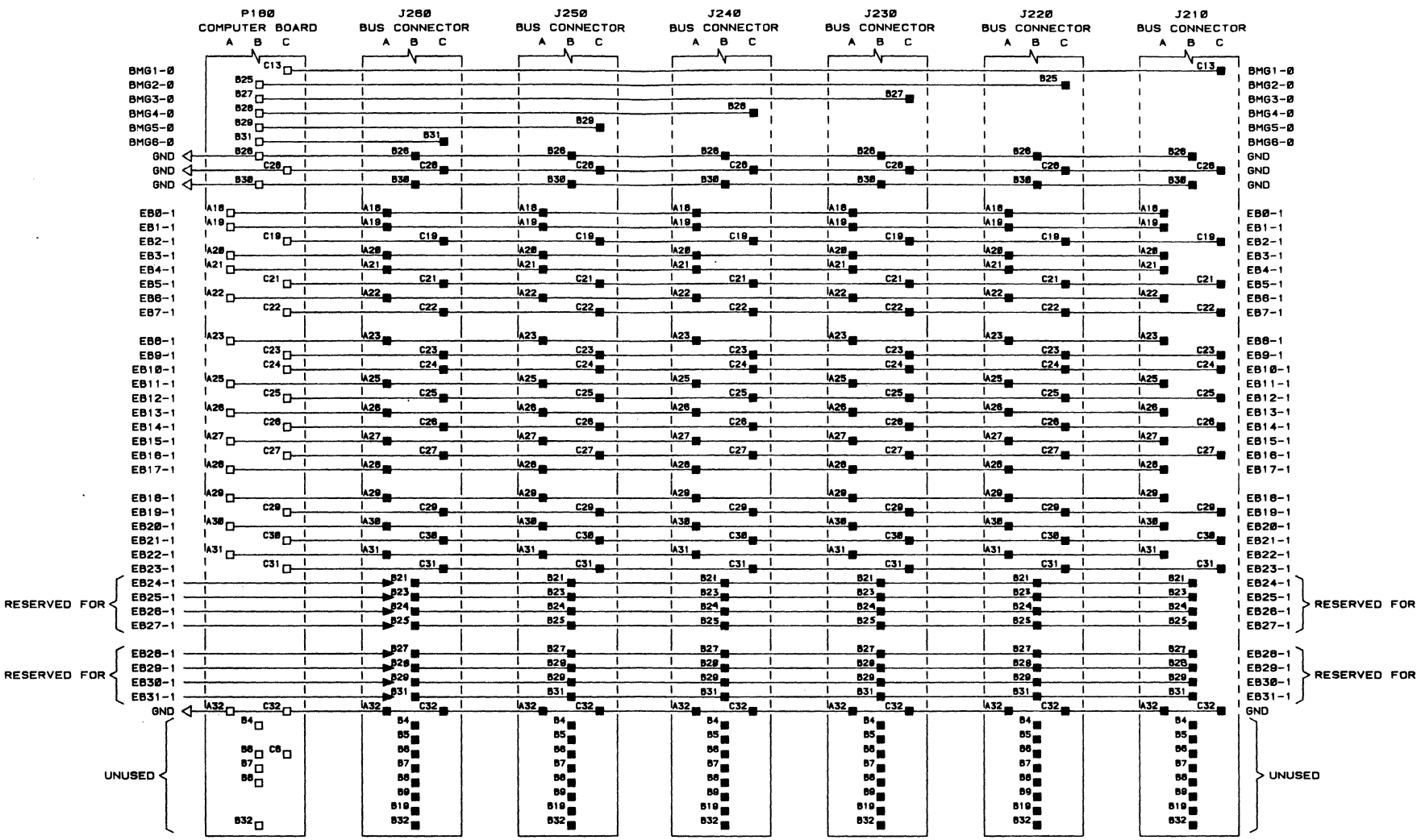
1. CAPACITORS C300 THRU C306 ARE TEK PART NUMBER 281-0767-00
2. THE BOARD DECOUPLE CAPACITOR IS A TEK PART # 290-0167-00 THIS CAPACITOR MUST BE PLACED CLOSE TO THE DIN CONNECTOR.
3. CHASSIS GND MUST BE CONNECTED TO CONNECTORS J950 AND J960 PIN 1. CHASSIS GND CAN BE LOCATED PER THE MECHANICAL DRAWING.
4. PLACE R1130 THRU R1132 AS CLOSE TO CONNECTOR J950 AS POSSIABLE.
5. U1030-9, AND U3130-9 ARE TO BE PROVIDED WITH ROOM FOR A CAPACITOR TO GND. SHOULD IT BECOME NECASSARY TO USE THIS CAPACITOR IT WILL BE ADDED. THIS CAP. HELPS WITH FILTERING. THIS CAP. IS NOT TO BE ADDED TO DOLLY.



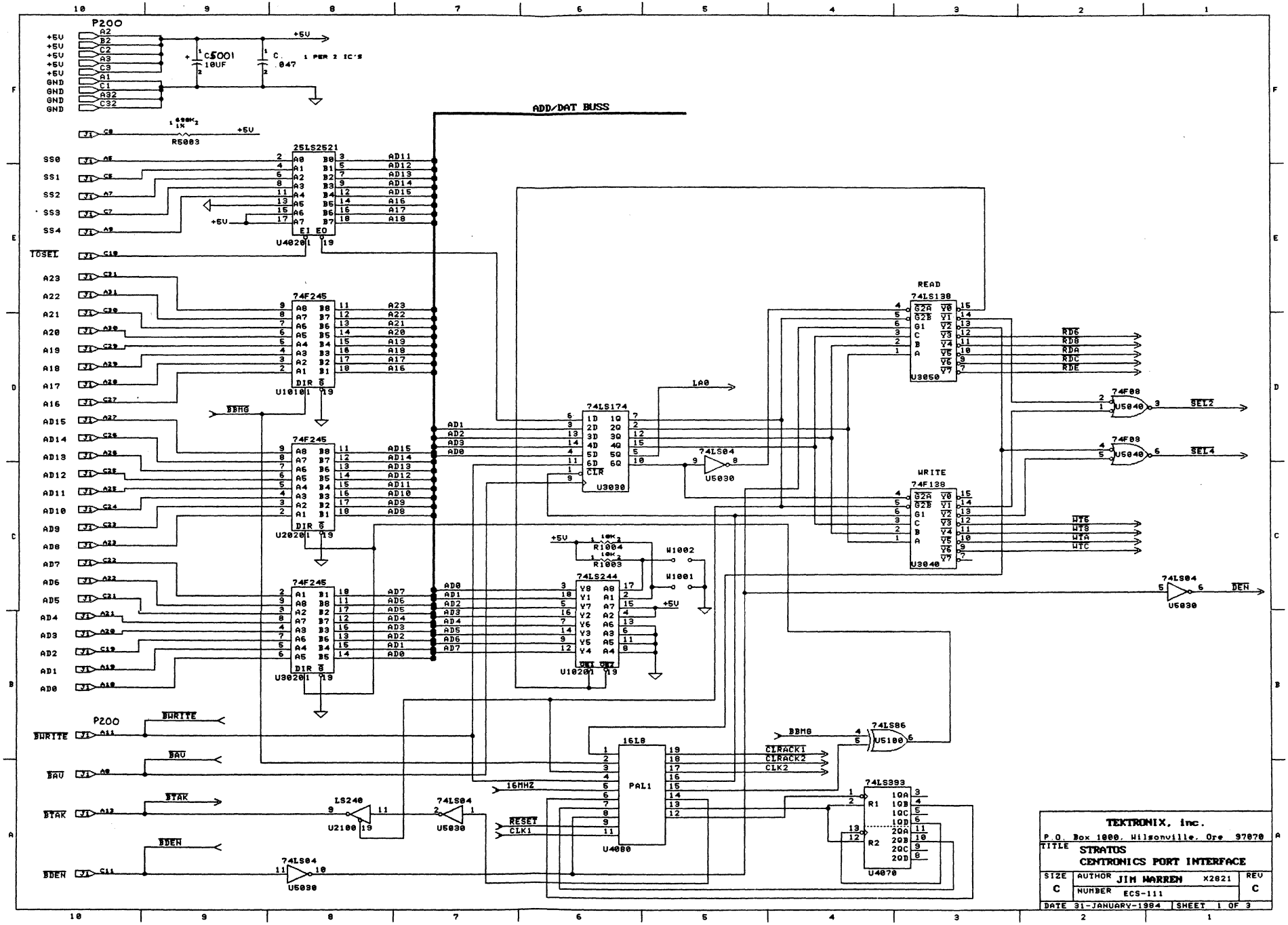
TEKTRONIX, inc.		
P.O. BOX 1000; Wilsonville, Ore 97070		
TITLE: STRATOS SYNC ASYNC SERIAL INTERFACE		
SIZE: C	ENGINEER: K.P. HEARNS	REV: E
	NUMBER: ECS-111	
DATE: 15-JAN 1985	SHEET 4 OF 4	

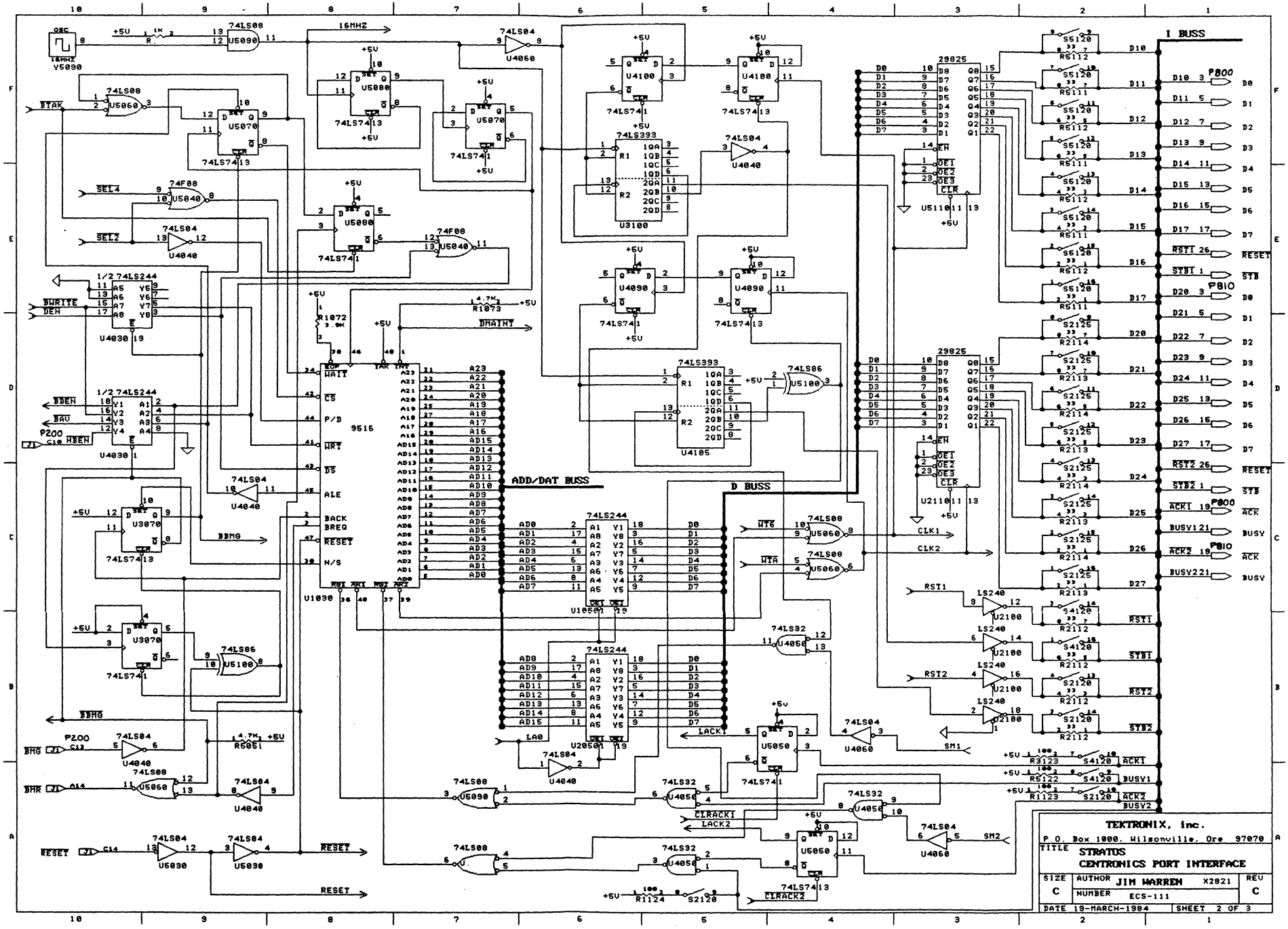


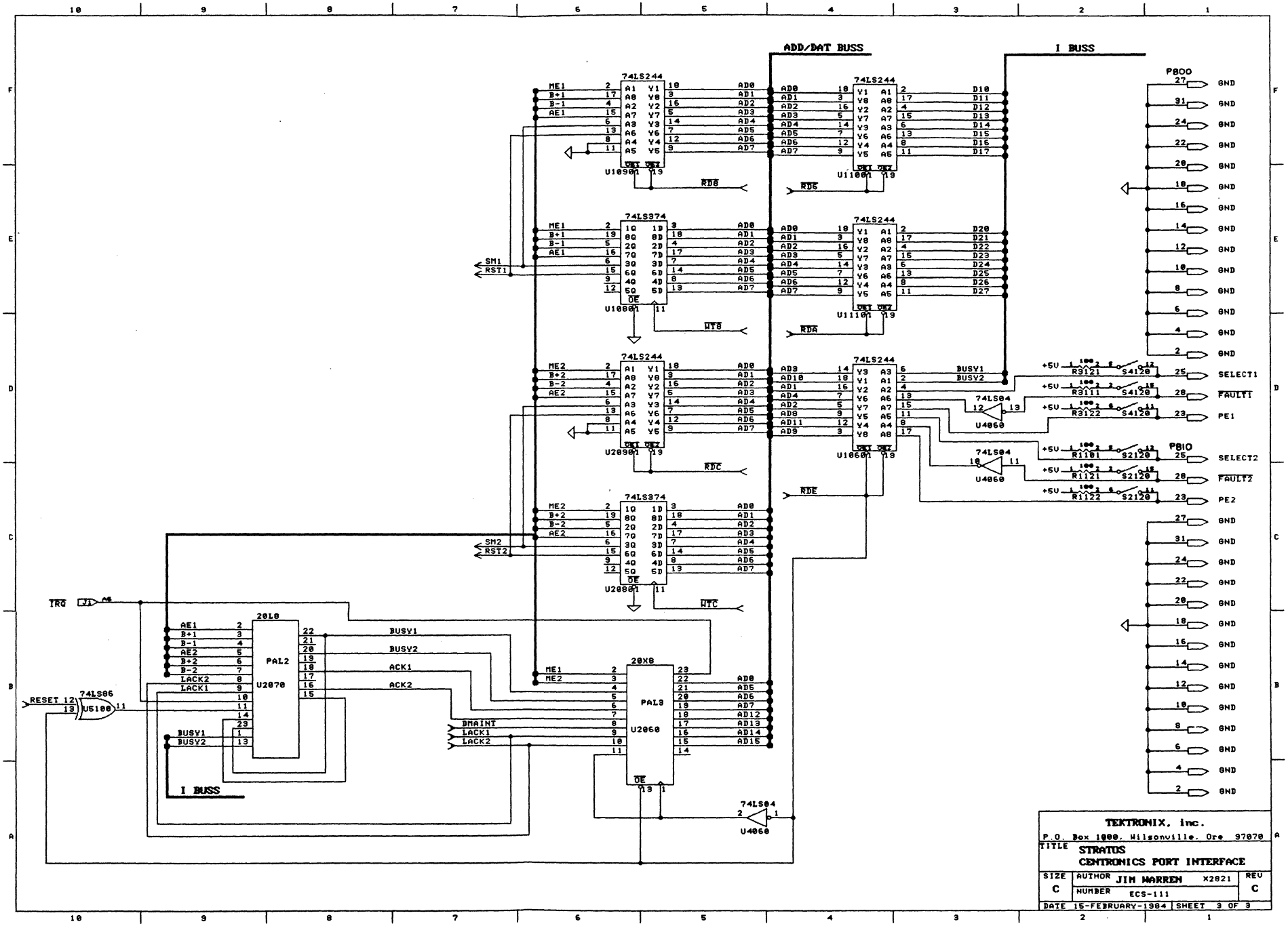
FIRST USE: 02/21/84	OTHER USES:	NOTES: * SIGNAL LEVEL VARIES WITH SLOT	TITLE: EXPANSION BACKPLANE	Tektronix	ASSEMBLY:
DRAWN BY: LFW					
CONTROL NO.: S0006A		TEKTRONIX, INC. © 1983			SHEET: 1 OF 2

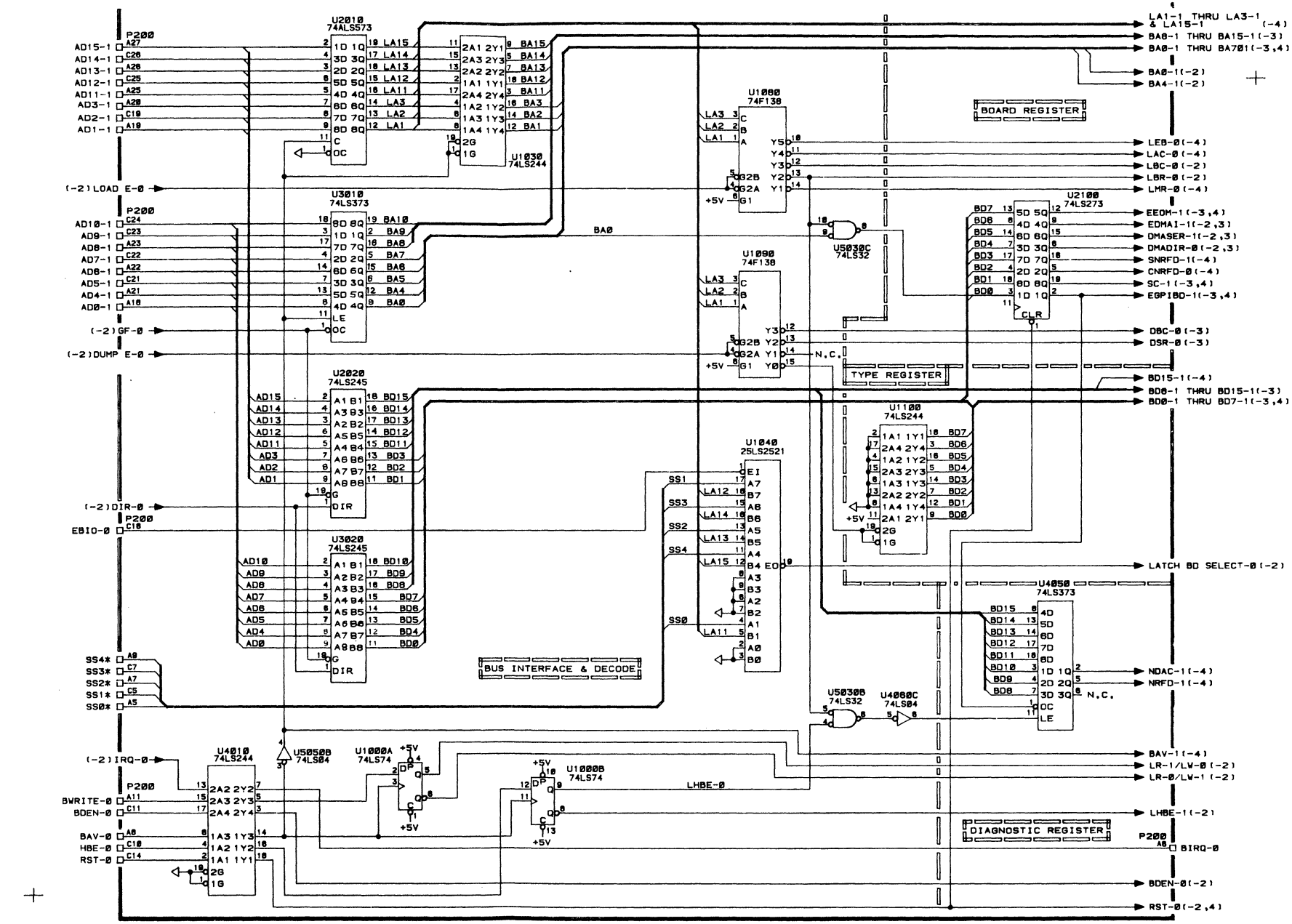


FIRST USE: 02/23/84	OTHER USES:	NOTES:	TITLE:		ASSEMBLY:
DRAWN BY: LFW			EXPANSION BACKPLANE	Tektronix	
CONTROL NO.: S00078		TEKTRONIX, INC. © 1983			SHEET: 2 OF 2

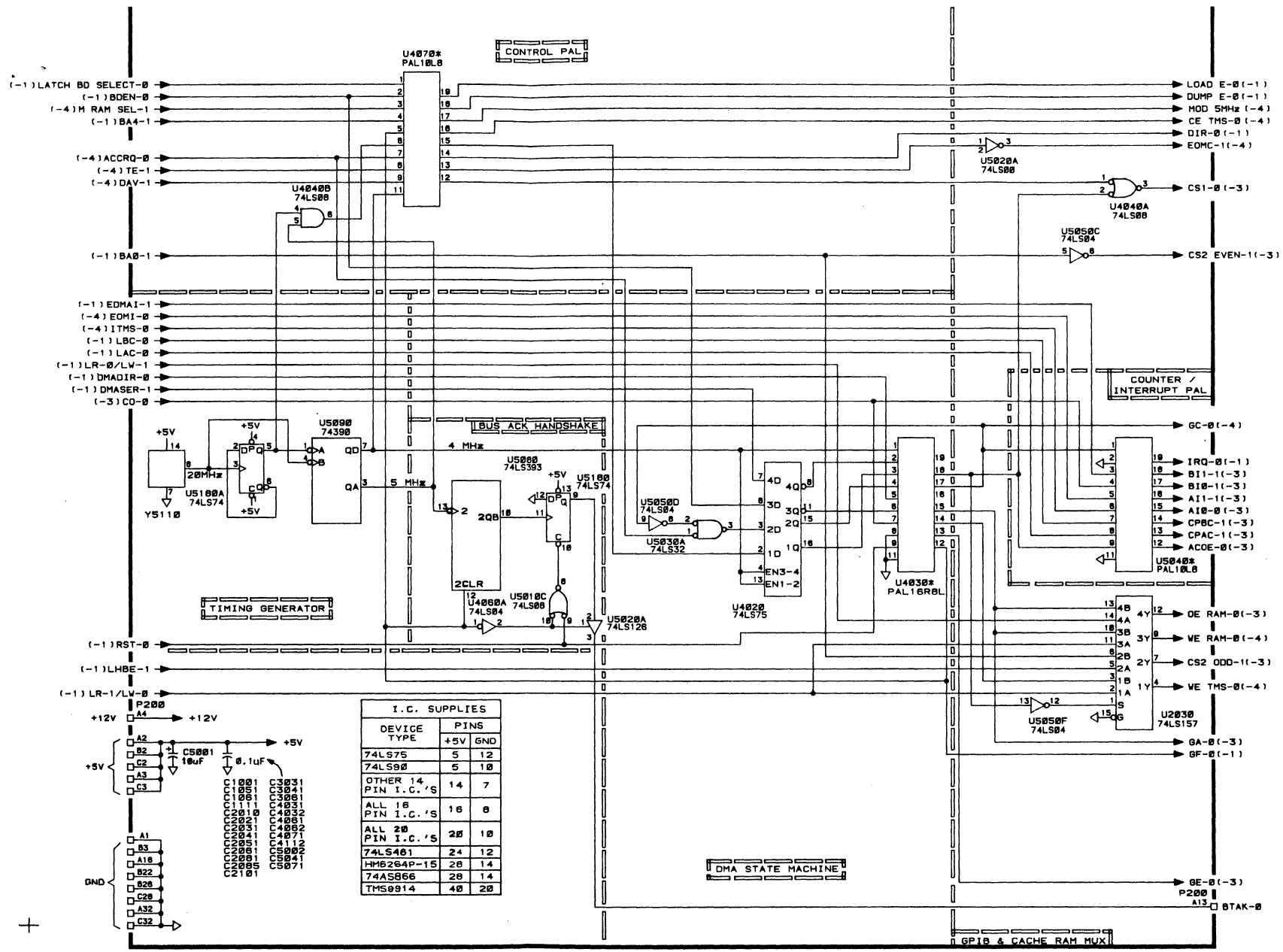

P200
ADD/DAT BUSS
25LS2521
74F245
74LS174
74LS244
74LS138
READ
WRITE
74F138
74F08
74LS04
74LS86
74LS393
LS240
PAL1
16L8
R5003
R1004
R1003
W1002
W1001
U4020
U1010
U2020
U3020
U5030
U3030
U5040
U3050
U3040
U5100
U2100
U4080
U4070
SS0
SS1
SS2
SS3
SS4
TOSEL
BBHG
BWRITE
BAU
BTAK
BDEN
RESET
CLK1
16MHZ
CLRACK1
CLRACK2
CLK2
LA0
SEL2
SEL4
DEN
RD5
RD8
RDA
RDC
RDE
WT5
WT8
WTA
WTC
TEKTRONIX, inc.
P O Box 1000, Wilsonville, Ore 97070
TITLE
STRATUS
CENTRONICS PORT INTERFACE
SIZE
C
AUTHOR JIM WARREN x2821
NUMBER ECS-111
REV
C
DATE 31-JANUARY-1984
SHEET 1 OF 3


I BUSS
ADD/DAT BUSS
D BUSS
9516
29825
74LS244
74LS393
74LS74
74LS04
74LS08
74LS32
74LS86
74F08
LS240
S5120
S2125
S4120
S2120
TEKTRONIX, inc.
P.O. Box 1000, Wilsonville, Ore 97070
TITLE STRATUS
CENTRONICS PORT INTERFACE
SIZE C
AUTHOR JIM WARREN X2821
NUMBER ECS-111
REV C
DATE 19-MARCH-1984
SHEET 2 OF 3

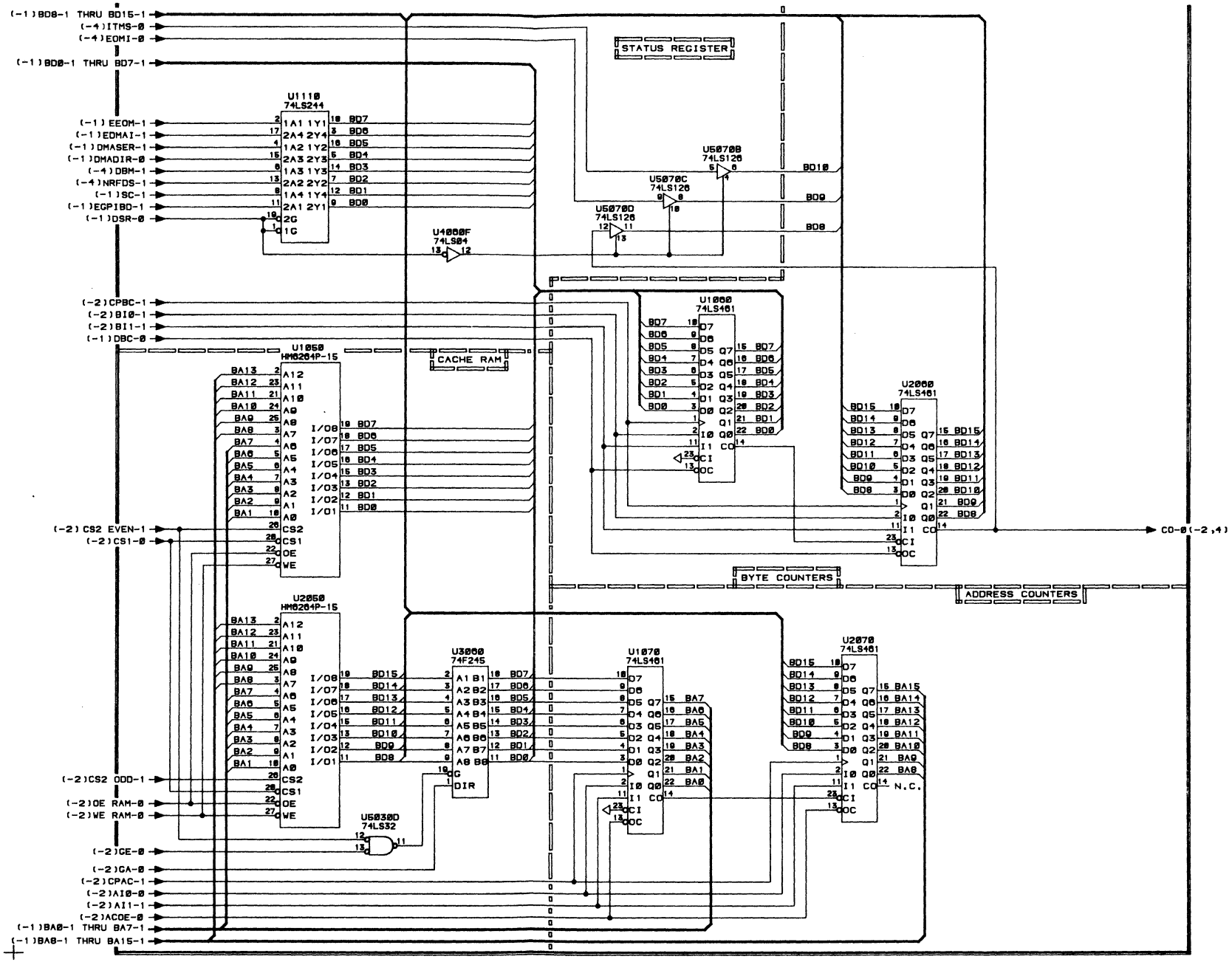

ADD/DAT BUSS
I BUSS
74LS244
74LS374
74LS86
74LS04
20L8
20X8
PAL2
PAL3
U2070
U2060
U4060
U5100
P800
P810
GND
SELECT1
FAULT1
PE1
SELECT2
FAULT2
PE2
RDB
RDA
RDC
RDE
WTB
WTC
SM1
RST1
SM2
RST2
BUSY1
BUSY2
ACK1
ACK2
DMAINT
LACK1
LACK2
RESET
IRQ
TEKTRONIX, inc.
P.O. Box 1000, Wilsonville, Ore 97070
TITLE
STRATUS
CENTRONICS PORT INTERFACE
SIZE
C
AUTHOR JIM WARREN X2021
NUMBER ECS-111
REV
C
DATE 15-FEBRUARY-1984
SHEET 3 OF 3



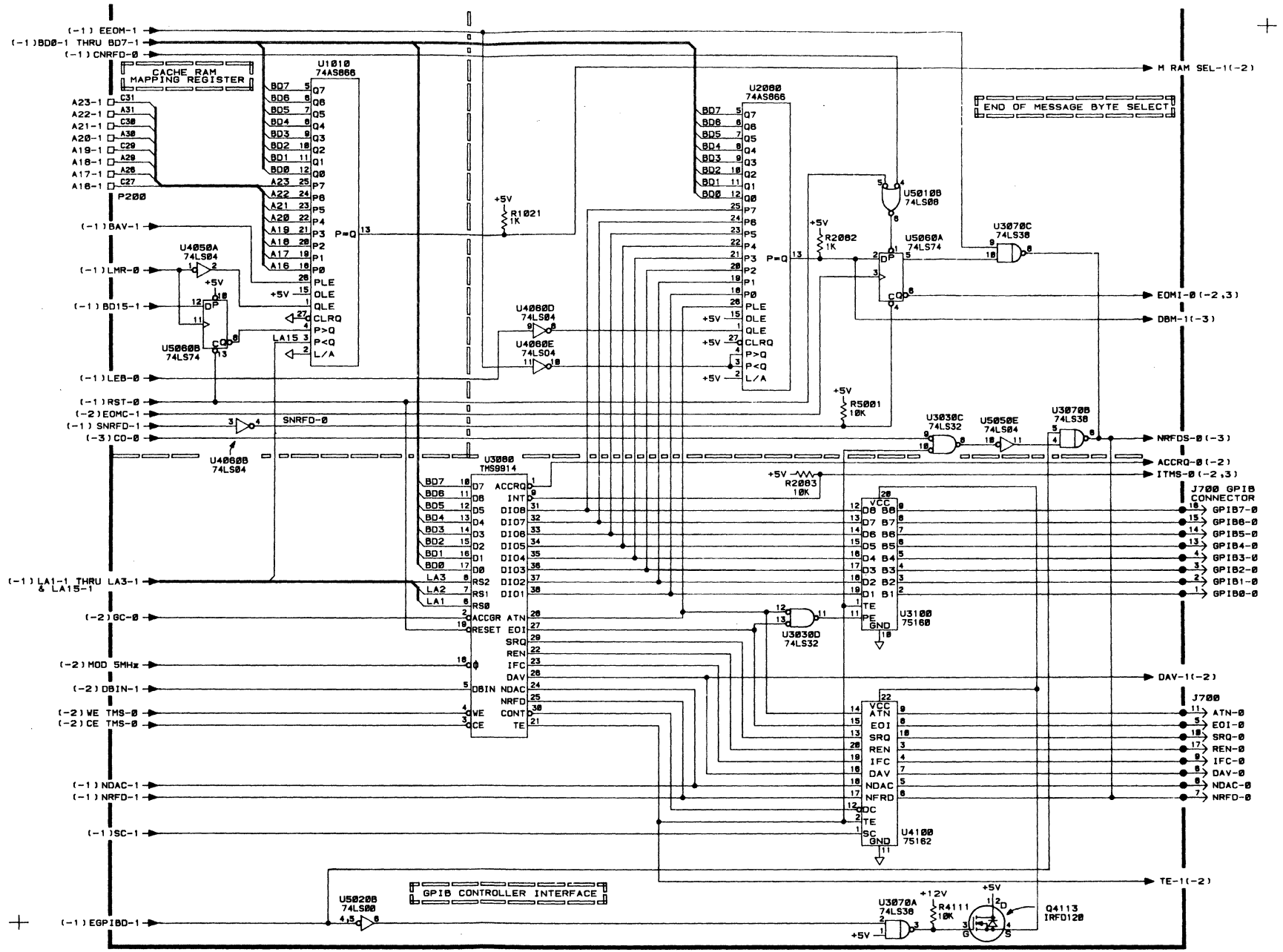
FIRST USE: 02/17/84 DRAWN BY: LFW CONTROL NO.: S0002A REV	OTHER USES:	NOTES: * ACTIVE STATE CHANGES WITH SLOT SELECTION TEKTRONIX, INC. © 1983	TITLE: HIGH SPEED GPIB INTERFACE	ASSEMBLY: SHEET: 1 OF 4



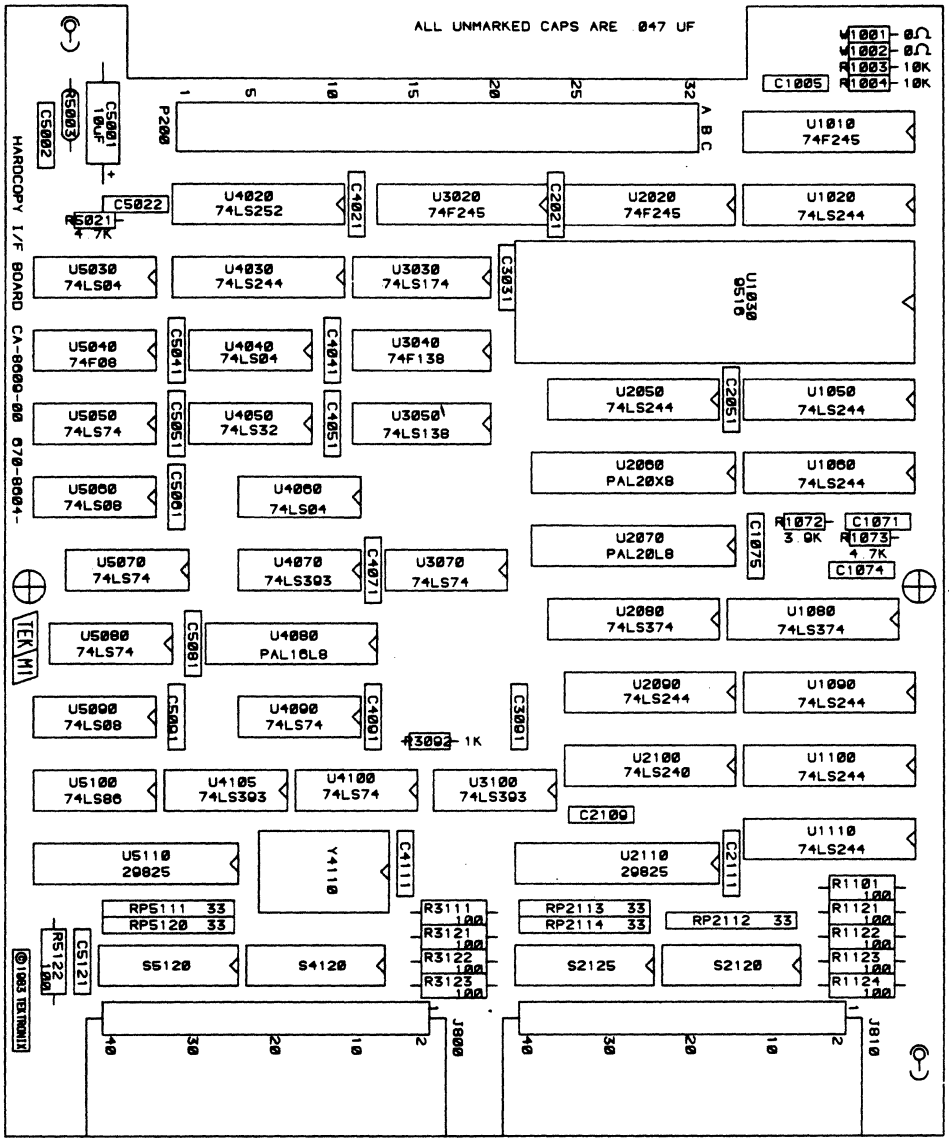
FIRST USE: 02/17/84	OTHER USES:	NOTES: *SEE SECTION 4 OF THIS MANUAL FOR CIRCUIT DESCRIPTION	TITLE: HIGH SPEED GPIB INTERFACE	ASSEMBLY:
DRAWN BY: LFW				
CONTROL NO.: S00025 REV		40% BLACK	Tektronix	SHEET: 2 OF 4
		TEKTRONIX, INC. © 1983		



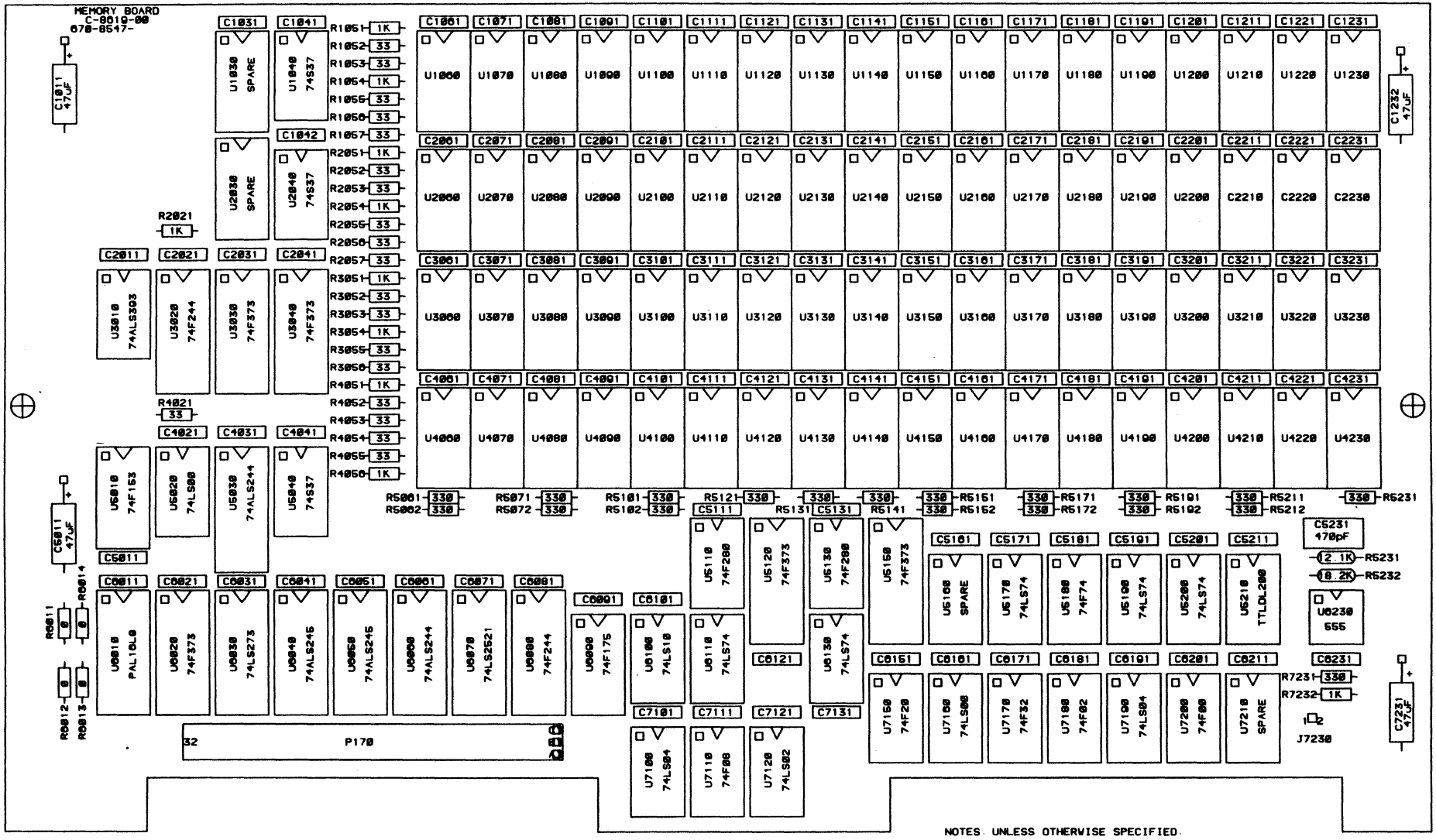
FIRST USE: 02/17/84	OTHER USES:	NOTES:	TITLE:	ASSEMBLY:
DRAWN BY: LFW		40% BLACK	HIGH SPEED GPIB INTERFACE	
CONTROL NO.: S0002C REV		TEKTRONIX, INC. © 1983	Tektronix	SHEET: 3 OF 4



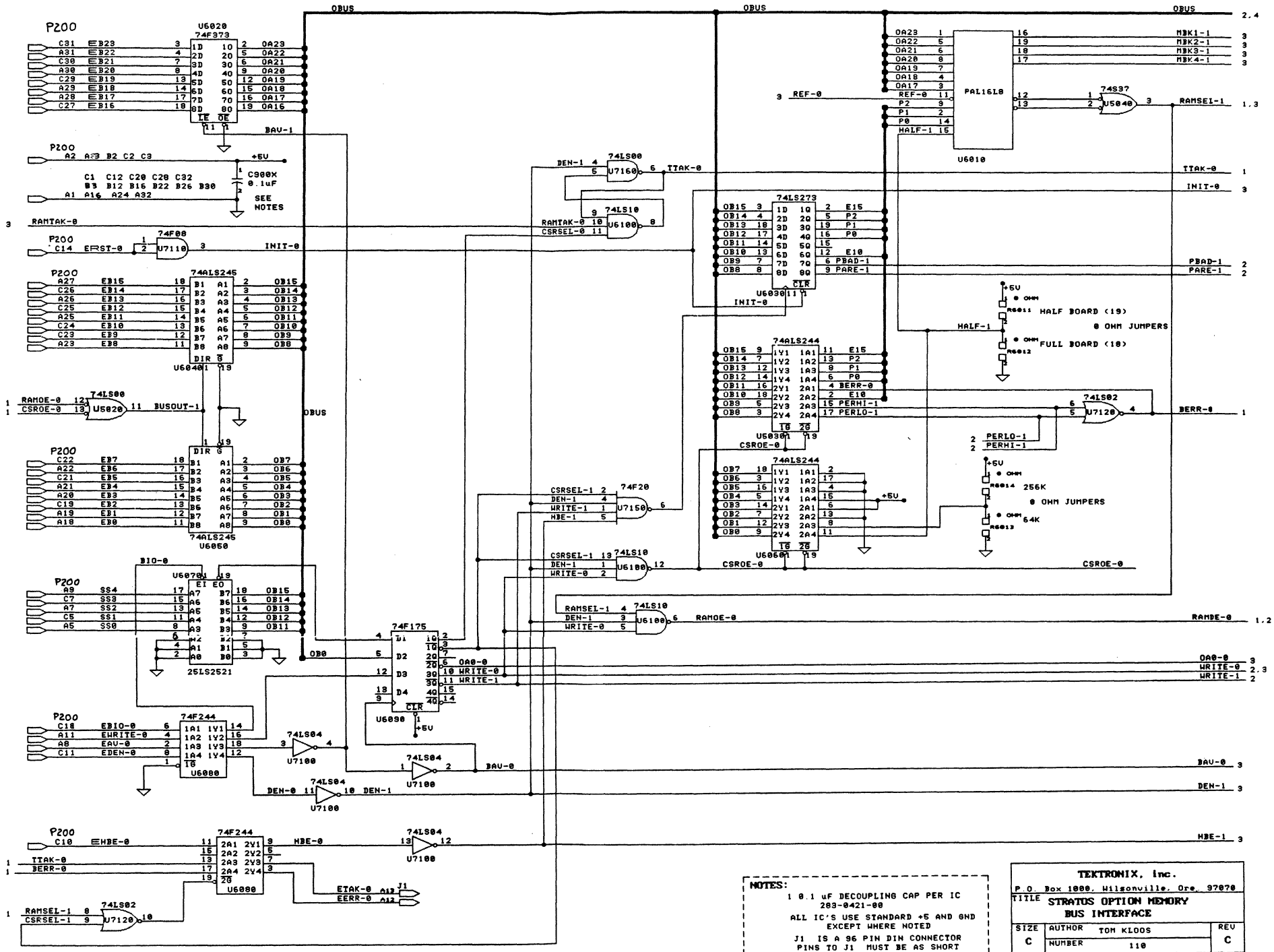
FIRST USE: 01/23/84	OTHER USES:	NOTES:	TITLE: HIGH SPEED GPIB INTERFACE	ASSEMBLY:
DRAWN BY: LFW		TEKTRONIX, INC. © 1983	Tektronix	SHEET: 4 OF 4
CONTROL NO.: S0002D REV				



Hardcopy Interface Component Locations



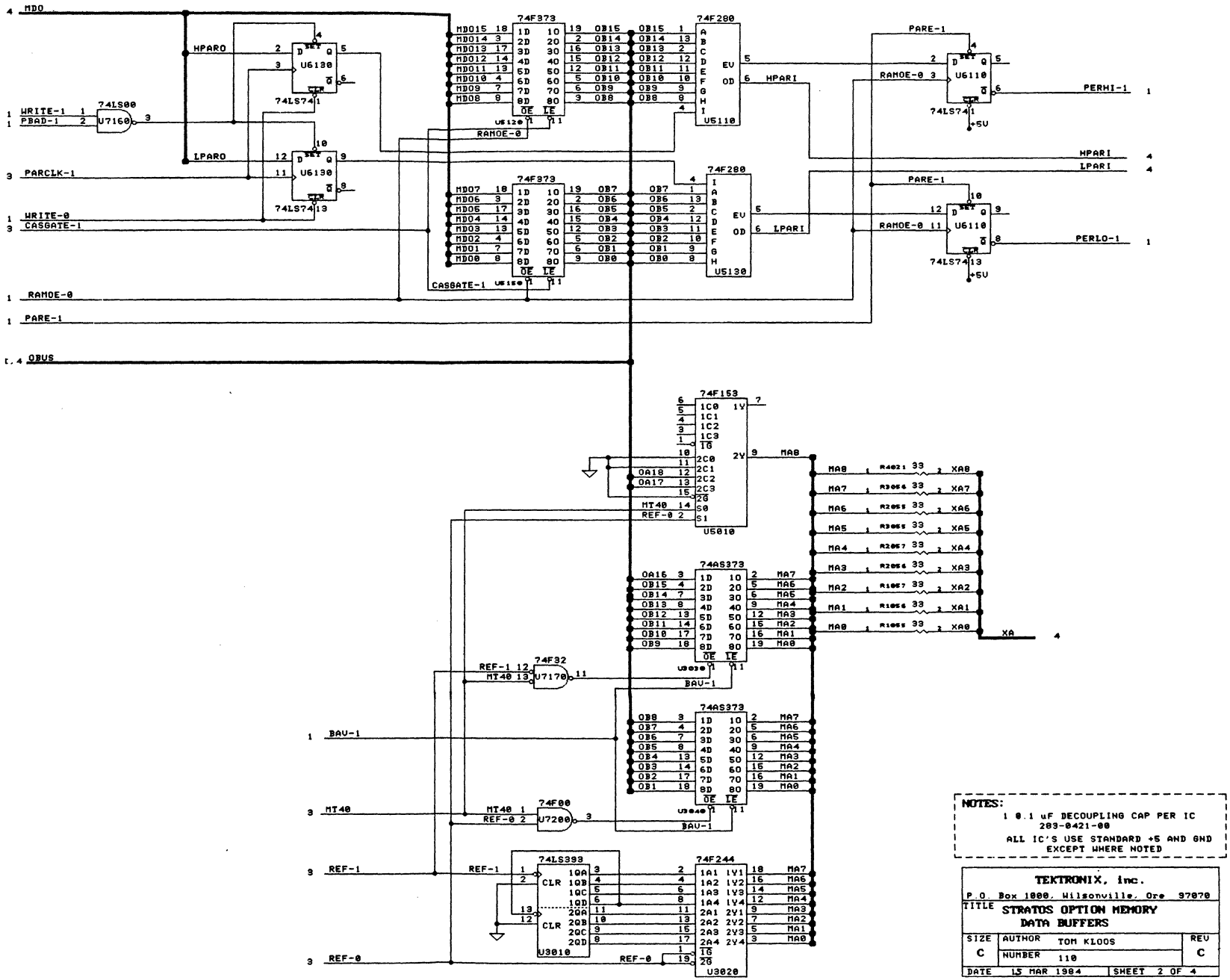
Memory Board Component Locations



NOTES:

1. 0.1 uF DECOUPLING CAP PER IC 283-0421-00
2. ALL IC'S USE STANDARD +5 AND GND EXCEPT WHERE NOTED
3. J1 IS A 96 PIN DIN CONNECTOR PINS TO J1 MUST BE AS SHORT AS POSSIBLE

TEKTRONIX, Inc.	
P.O. Box 1000, Wilsonville, Ore. 97070	
TITLE	STRATUS OPTION MEMORY BUS INTERFACE
SIZE: C	AUTHOR: TOM KLOOS
	NUMBER: 110
REV: C	
DATE: 2 MAR 1984	SHEET 1 OF 4



NOTES:

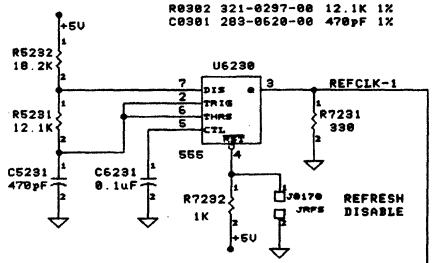
1. 0.1 uF DECOUPLING CAP PER IC 283-0421-00
2. ALL IC'S USE STANDARD +5 AND GND EXCEPT WHERE NOTED

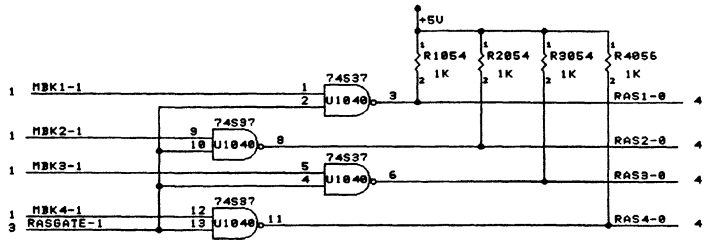
TEKTRONIX, inc.		
P.O. Box 1000, Wilsonville, Ore 97070		
TITLE: STRATOS OPTION MEMORY DATA BUFFERS		
SIZE: C	AUTHOR: TOM KLOOS	REV: C
	NUMBER: 110	
DATE: 15 MAR 1984	SHEET 2 OF 4	

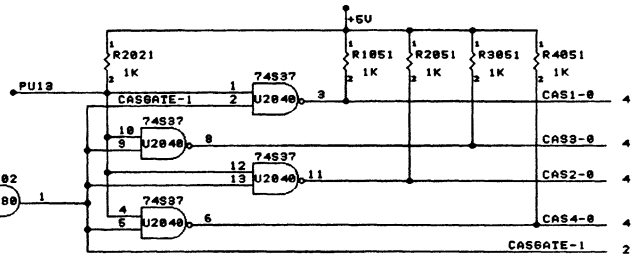
NOTES:

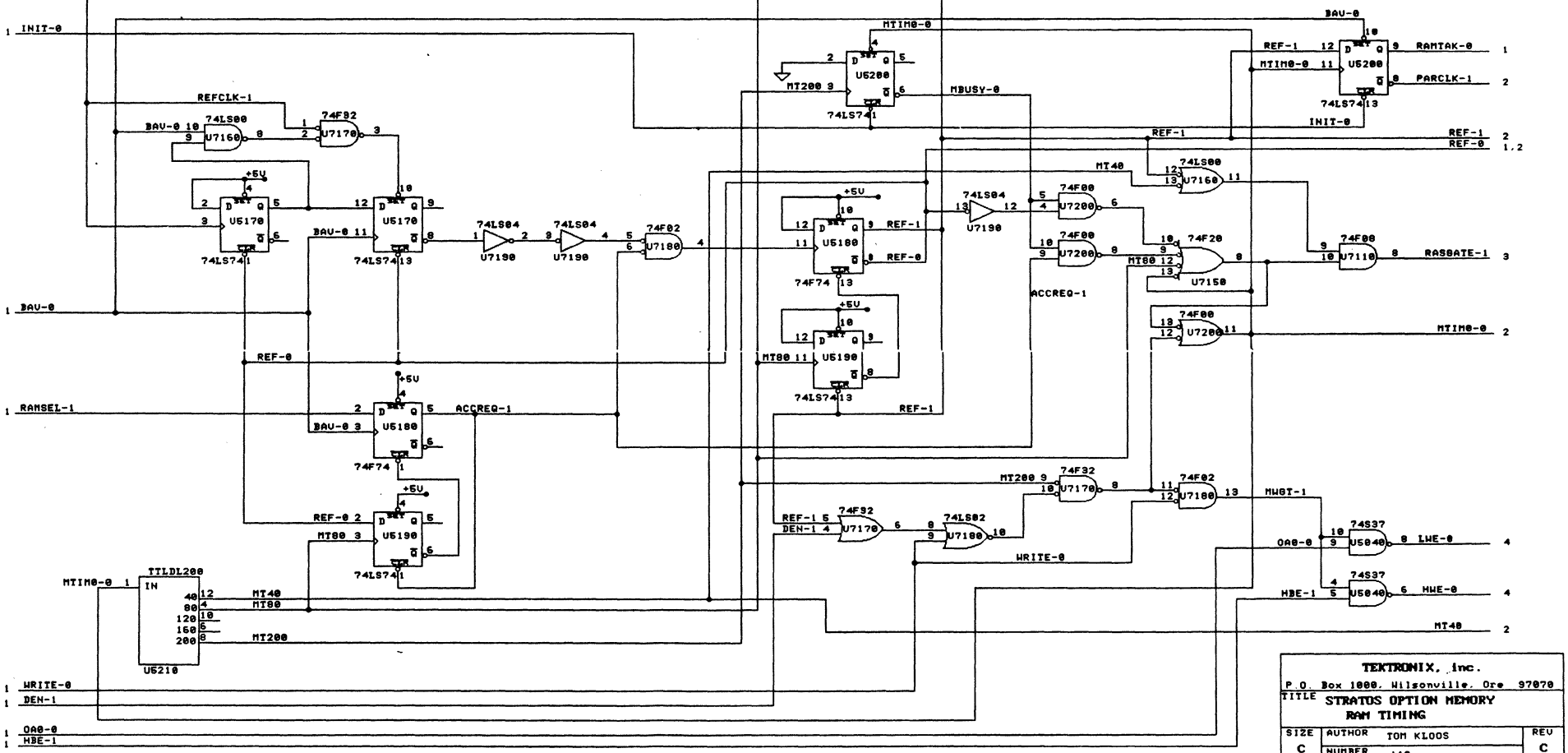
1 0.1 uF DECOUPLING CAP PER IC
283-0421-00
ALL IC'S USE STANDARD +5 AND GND
UNLESS NOTED OTHERWISE
TTLDL USES +5 PIN 14 - GND PIN 7

R0301 321-0314-00 18.2K 1%
R0302 321-0297-00 12.1K 1%
C0301 283-0620-00 470pF 1%

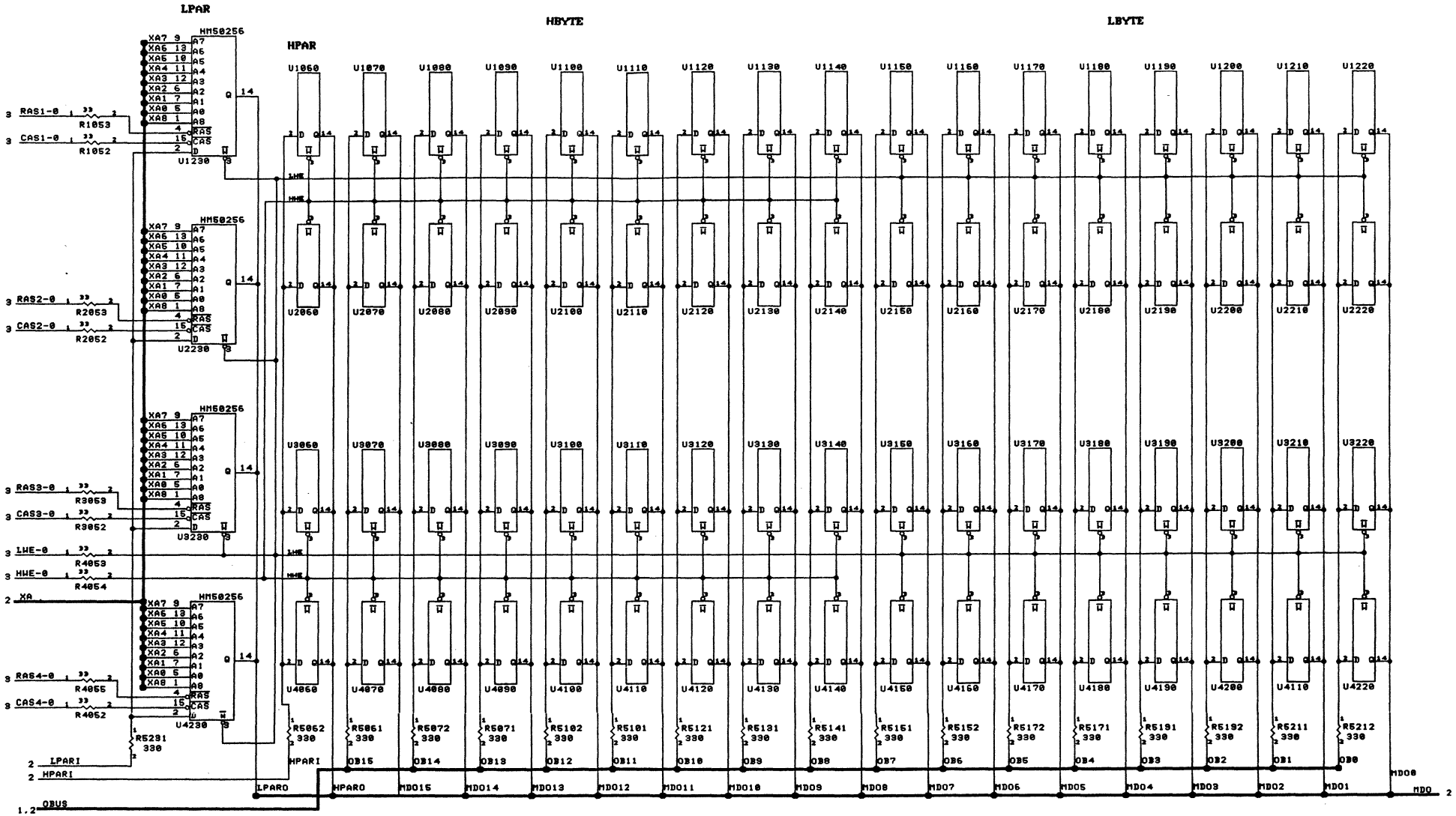






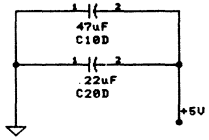


TEKTRONIX, inc.		
P.O. Box 1000, Wilsonville, Ore 97070		
TITLE: STRATOS OPTION MEMORY RAM TIMING		
SIZE: C	AUTHOR: TOM KLOOS	REV: C
	NUMBER: 110	
DATE: 1 MAR 1984	SHEET 3 OF 4	



NOTES:

= HM50256 (RAM PARTS) POWER:
+5 PIN 8
GND PIN 16

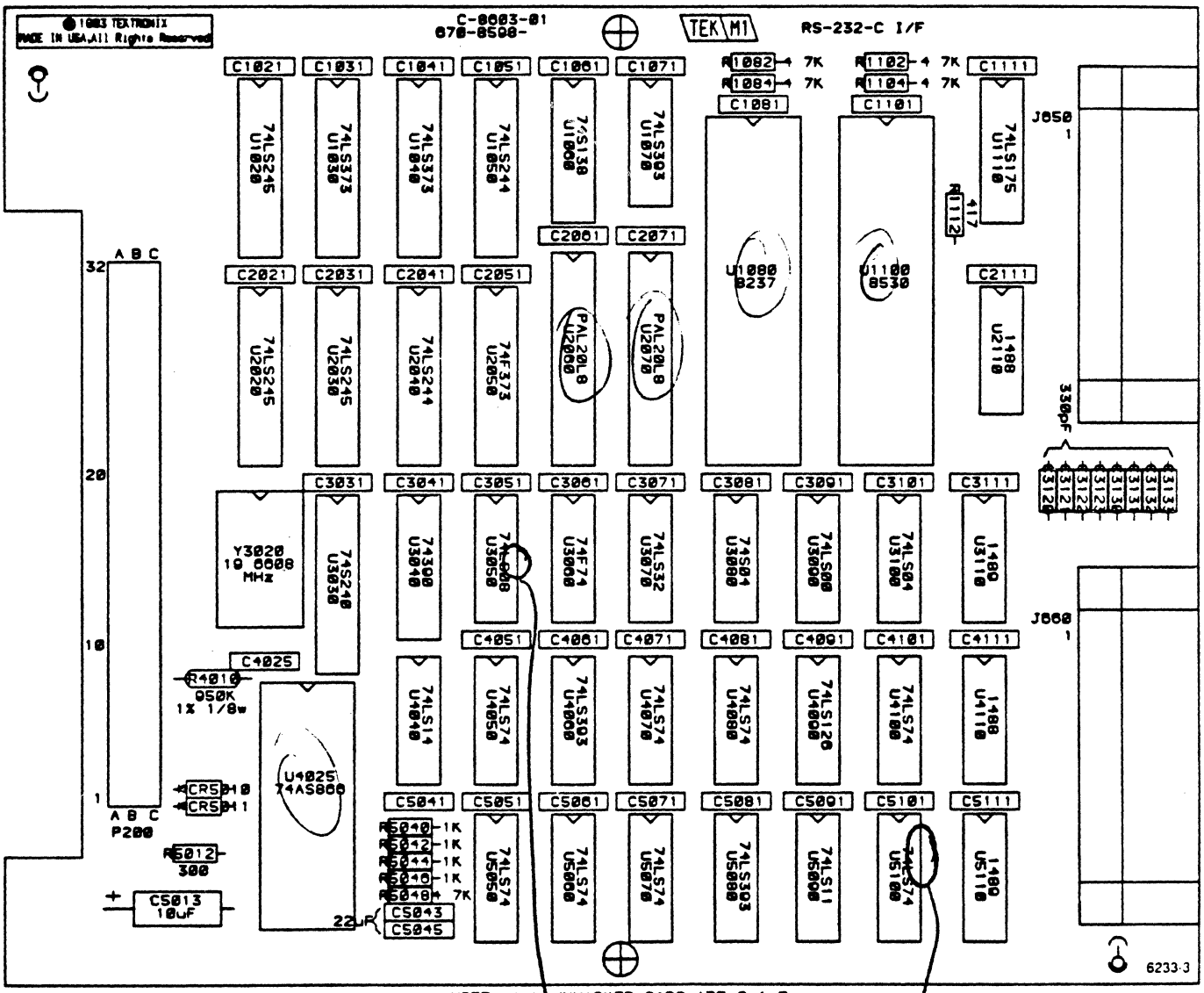


4 47uF DECOUPLING CAPS C1011,C5011,C1231,C7231
290-0847-00

72 0.22 uF DECOUPLING CAPS
283-0423-00
(1 PER RAM CHIP)

RAM PARTS SHOULD BE ARRANGED IN
BIT NUMBER ORDER

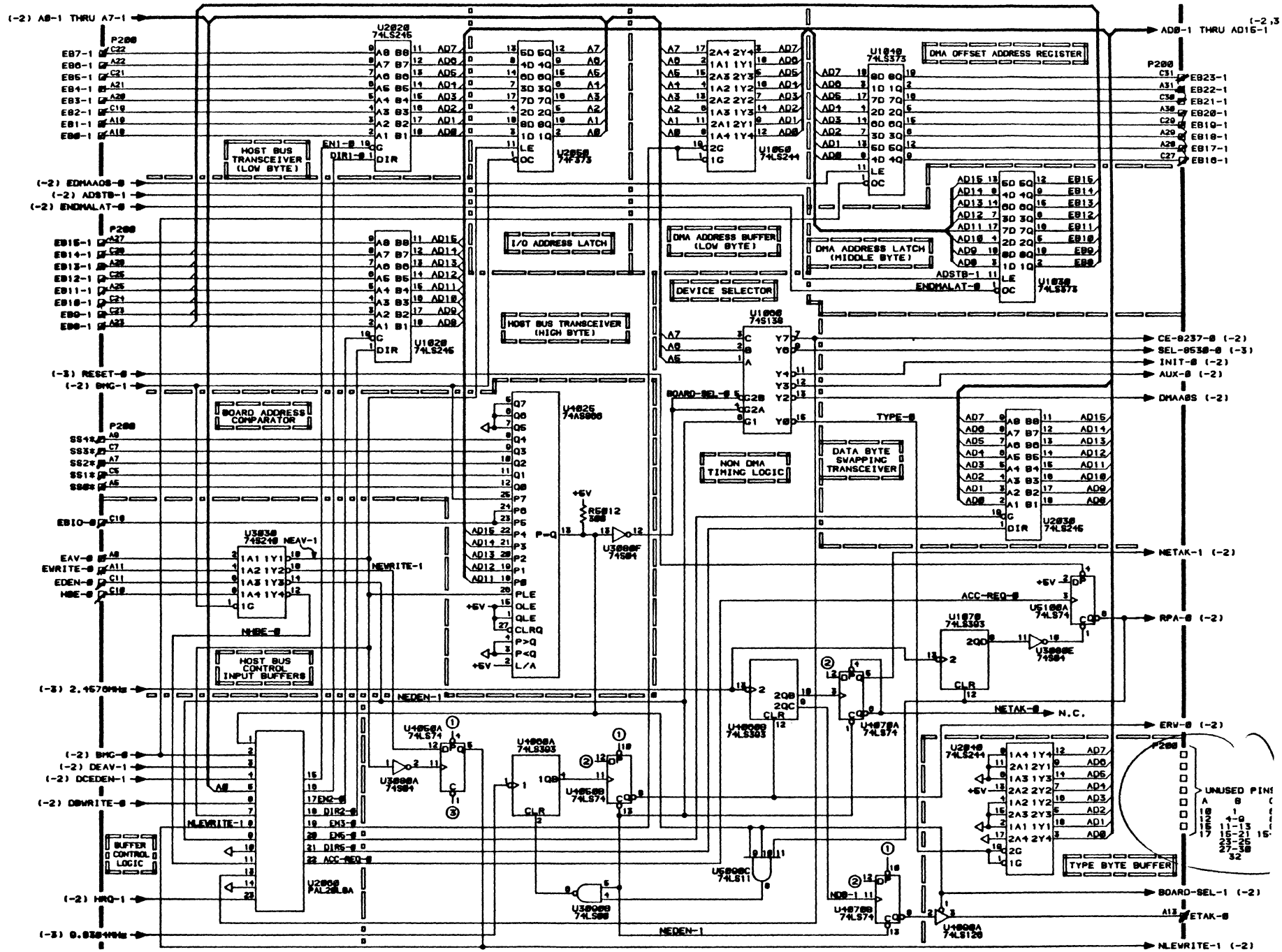
TEKTRONIX, inc.		
P.O. Box 1000, Wilsonville, Ore 97070		
TITLE: STRATUS OPTION MEMORY MEMORY ARRAY		
SIZE: C	AUTHOR: TOM KLOOS	REV: C
	NUMBER: 110	
DATE: 6 FEB 1984	SHEET: 4 OF 4	



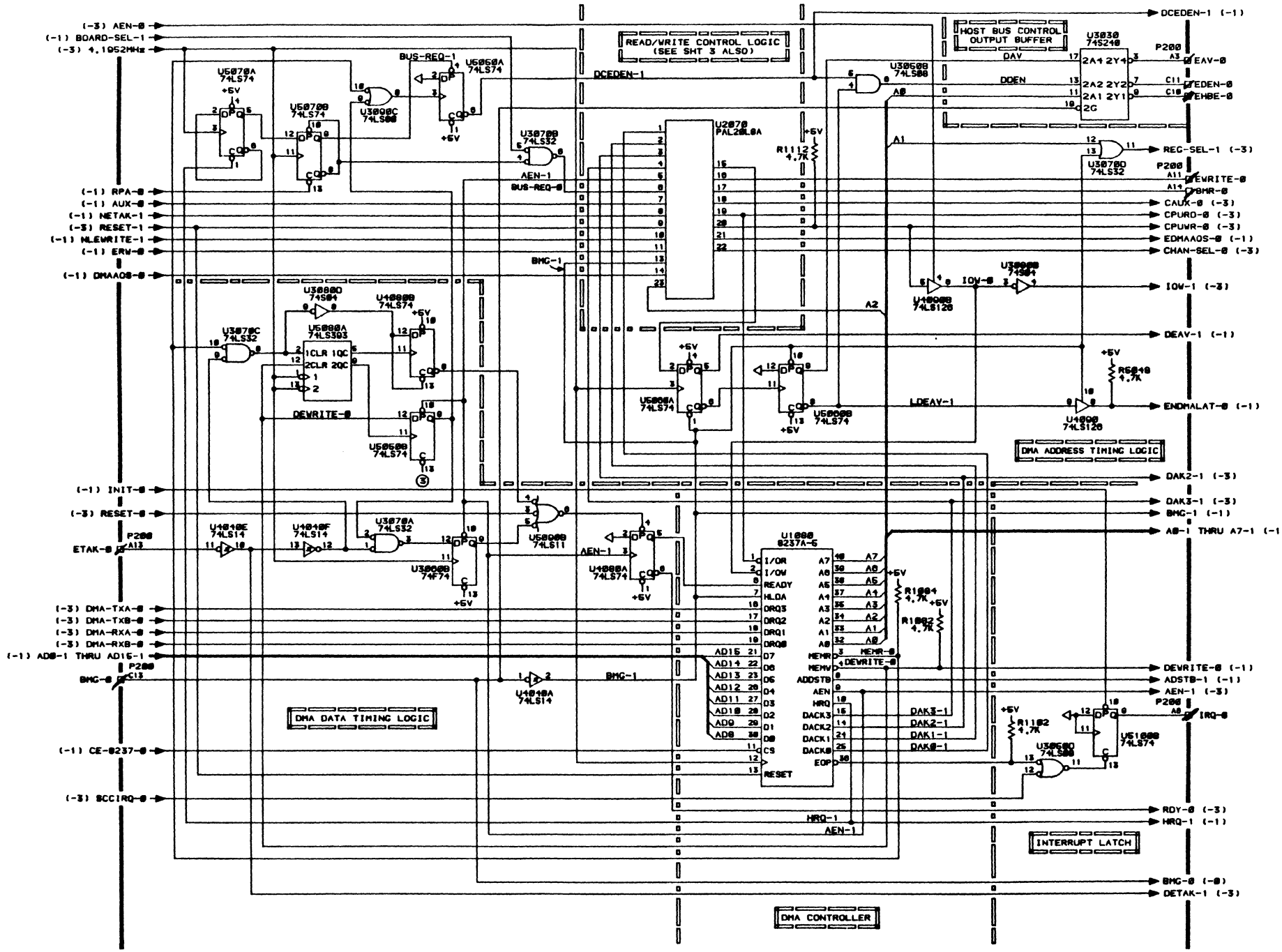
NOTE ALL UNMARKED CAPS ARE @ 1uF

RS-232-C Interface (670-8598-00, 01) Component Locations.

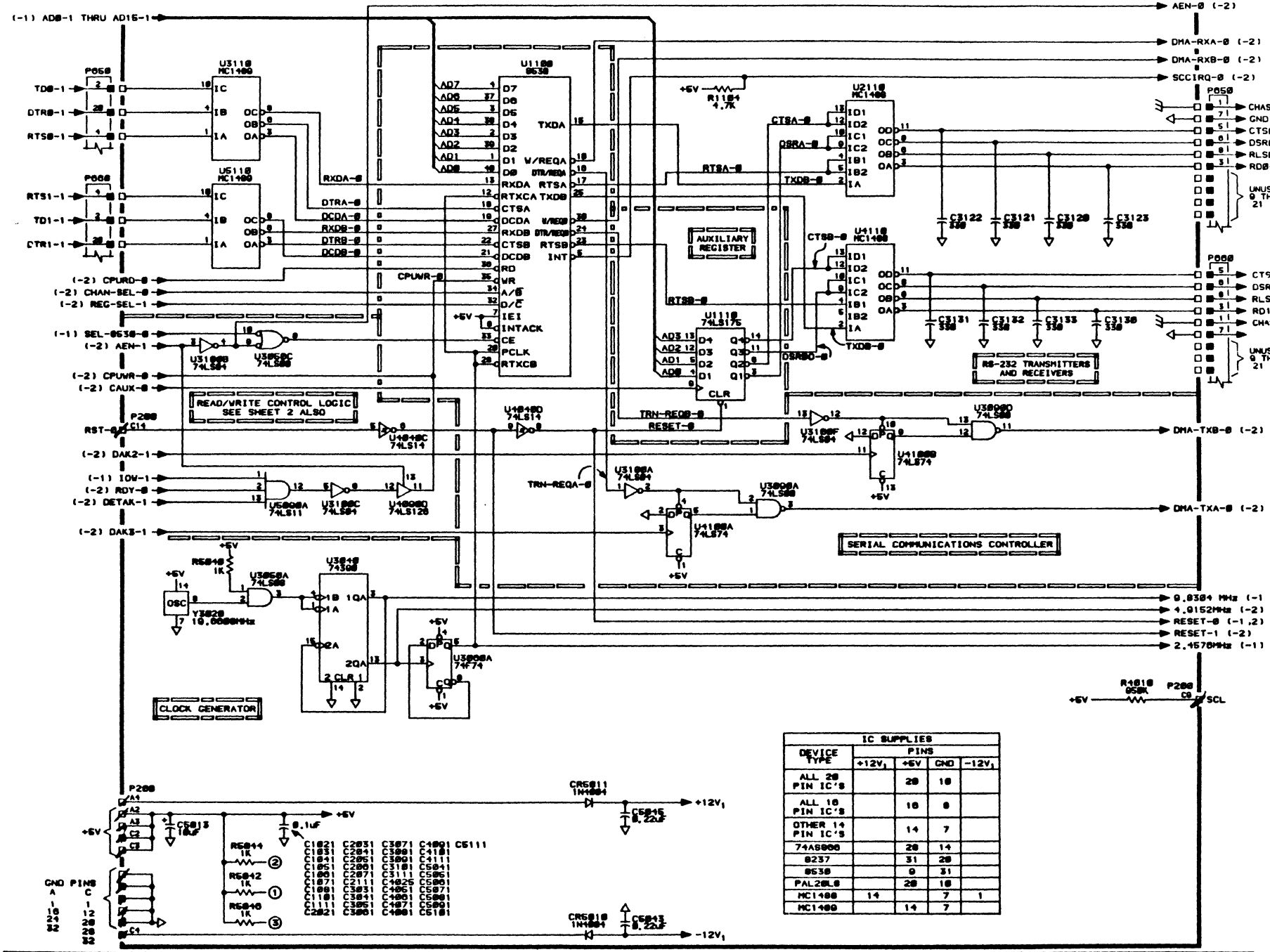
WIRE MODS HERE



FIRST USE: 8139	OTHER USES: 4132	NOTES: * ACTIVE STATE CHANGES WITH SLOT SELECTION	TITLE: 070-0509-00,01 OPTION 3A RS-232-C INTERFACE BOARD	ASSEMBLY: A8
DATE: REV, 28 AUG 86		TEKTRONIX, INC. © 1986	Tektronix	SHEET: 1 OF
CONTROL NO.: S0000A				



FIRST USE: 0138 DATE: REV, 20 AUG 80 CONTROL NO.: 000000	OTHER USES: 4132	NOTES:	TITLE: 070-0500-00,01 OPTION 3A RS-232-C INTERFACE BOARD	Tektronix	ASSEMBLY: A8 SHEET: 2 0



IC SUPPLIES				
DEVICE TYPE	PINS			
	+12V1	+5V	GND	-12V1
ALL 20 PIN IC'S		20	10	
ALL 16 PIN IC'S		16	8	
OTHER 14 PIN IC'S		14	7	
74AS888		20	14	
8237		31	20	
8530		9	31	
PAL20L8		20	10	
MC1488	14		7	1
MC1489		14	7	

FIRST USE: 6130	OTHER USES: 4132	NOTES:	TITLE: 670-8508-00,01	ASSEMBL' A
DATE: REV, 20 AUG 86			OPTION 3A RS-232-C INTERFACE BOARD	
CONTROL NO.: 880086		TEKTRONIX, INC. © 1986	Tektronix	SHEET:

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PAL20L8                                                PAL DESIGN SPECIFICATION
160-2842-00(156-1803-00)                               Keith Hearns 03/26/84
Driver/Transceiver Direction and Enable Control
Stratos, ECS, DAID, Tektronix, Wilsonville, OR
BS DM DV DB AO DW NV NW NB NC1 NH GND CE NC2
EN1 DR1 EN2 DR2 EN3 EN5 DR5 AR HRQ VCC
; BS = Board-Sel
; DM = DMA-Active
; CE = CE8237
; DV = DBAV
; DB = DBDEN
; DW = DBWRITE
; NH = NHBE
; NV = NBAV
; NW = NBWRITE
; NB = NBDEN
; AR = ACC_REQ
; HRQ = BUS HOLD REQUEST
;
IF(VCC) /EN1 = DM
             + /DM * DV
             + /DM * /AO * /DV
IF(VCC) /DR1 = DM * /NW * NB * BS
             + /DM * DV
             + /DM * /DW * /DV * /AO
;
IF(VCC) /EN2 = DM * NV
             + DM * BS * /CE * NB * NH * AO
             + /DM * AO * /DV
;            + /DM * DV
IF(VCC) /DR2 = DM * BS * /CE * NB * /NW
             + /DM * DV
             + /DM * /DV * AO * /DW
;
;
IF(VCC) /EN3 = /DM * DV
;
;
IF(VCC) /EN5 = DM * BS * /CE * NB * /AO * /NH
             + /DM * AO * /DV
IF(VCC) /DR5 = DM * NB * /CE * BS * /NW
             + /DM * DW * AO
;
IF(VCC) /AR = BS * NB
            + HRQ * /BS
;
;
FUNCTION TABLE
; Inputs ------------------------------------------! Outputs ---------------
NC1 NC2 HRQ NH CE BS  DM DV DB AO DW NV NW NB EN1 DR1 EN2 DR2 EN3 EN5 DR5 AR
;
;N N H N C B D D D A D N N N    E D E D E E D A C
;C C R H E S M B B O B B B B    N I N I N N I R O
;1 2 Q B * * A A D * W A W D    1 R 2 R 3 5 R * M
;* * * E * * * V E * R V R E    * 1 * 2 * * 5 * M
;* * * * * * * * N * I * I N    * * * * * * * * E
```

```
;* * * * * * * * * * * T * T *     * * * * * * * * N
;* * * * * * * * * * * E * E *     * * * * * * * * T
;* * * * * * * * * * * * * * *     * * * * * * * * S
-------------------------------------------------------------------------------
 L L L L H L H L L L L H L L     L H L H H H H H Enable Address Drivers (1)
 L L L L H H H L L L L L L H     L L H H H H H L Direct Address Drivers
 L L L L L H H H H L L L L H     L L H L H L L L Low Data enable Read DMAC
 L L L L L H H H H L L L H H     L H H H H L H L Low Data enable Write DMAC
 L L L L H L L L L L L H H L     L L H H H H H H DMA GRANT (5)
 L L L L H H L H L L L H H H     L L H L L H H L Output DMA Address
 L L L L H H L L H L L L L L     L L H H H H H H Output DMA Low Data
 L L L L H H L L H H H L L L     H H L H H L L H Input DMA HIGH Data
 L L L L H H L L H H L L L L     H H L L H L H H Output DMA HIGH Data
 L L L L H H L L H L H L L L     L H H H H H H H Input DMA LOW DATA (10)
 L L L L H H L L H L L L L L     L L H H H H H H Output DMA LOW DATA
 L L L L H H L L L L H L L L     L H H H H H H H Wait for DBDEN to become active
 L L L L L H H L L L H H H L     L H L H H H H H
 L L L L L H H L L L H H H L     L H L H H H H H
 L L L L L L L L L L H H H H     L H H H H H H H (15)
 L L L L L L L L L L H H H H     L H H H H H H H
 L L L L H H H L L L L L L L     L H H H H H H H Low Byte READ
 L L L H L H H H H H L L L H     L L L L H H L L High Data enable Read DMAC
 L L L H L H H H H H L L H H     L H L H H H H L High Data enable Write DMAC
 X X H X X L X X X X X X X L     X X X X X X X L
 X X H X X L X X X X X X X X     X X X X X X X L
 X X L X X L X X X X X X X X     X X X X X X X H
-------------------------------------------------------------------------------
```

DESCRIPTION

This PAL is used to control the transceivers, and drivers on the serial option board. The PAL will allow the CPU to write an address to the latchs on board, and allow the DMC to write out its addresses when it is in control of the bus. Other functions include turning on the DMA Offset Register, turning around the direction of the data transceivers, and doing the necessary byte swap.

```
PAL20L8                                                PAL DESIGN SPECIFICATION
160-2842-00(156-1803-00)                               Keith Hearns 05/16/84
Write/Read Control, Latch Clocks, and Bus Request
Stratos, ECS, DAID, Tektronix, Wilsonville, OR
DO D1 D2 D3 AN BQ AX NB RS RW ERW GND BA DA
ED BW BR CA CR CW EDM CS A2 VCC
; DO = DAK0
; D1 = DAK1
; D2 = DAK2
; D3 = DAK3
; AN = AEN
; BQ = BUS-REQ
; AX = AUX
; NB = NBTAK
; RS = RESET
; RW = R-0/W-1
; BA = BUS-ACK
; DA = DMAADS
; ED = EDBAV
; BW = BWRITE
; BR = BRQ
; CA = CAUX
; CR = CPURD
; CW = CPUWR
; EDM = EDMAADS
; CS = CHAN-SEL
;
;
IF(VCC) /ED = DO * AN
            + D1 * AN
            + D2 * AN
            + D3 * AN
;
IF(BA) /BW = DO
           + D1
;
IF(VCC) /BR = /BQ
            + AN
;
IF(VCC) /CA = /NB * /AX
;
IF(/BA) /CR = /RW * /ERW
            + RS
;
IF(/BA) /CW = RW * /ERW * /NB
            + RS
;
IF(VCC) /EDM = DA
;
IF(VCC) /CS = /BA * /A2
              + BA * DO
              + BA * D2
;
FUNCTION TABLE
; Inputs ------------------------------------! Outputs ----------------------
DO D1 D2 D3 AN BQ AX NB RS RW ERW BA DA A2 ED BW BR CA CR CW EDM CS
```

```
;
;D D D D A B A N R R E B D A  E B B C C C E C  C
;A A A A E U U B E O R U M 2  D W R A P P D H  O
;K K K K N S X T S / W S A *  B R Q U U U M A  M
;0 1 2 3 * - * A E W * - A *  A I * X R W A N  M
;* * * * * R * K T 1 * A O *  V T * * D R A -  E
;* * * * * E * * * * * C S *  * E * * * * O S  N
;* * * * * Q * * * * * * K *  * * * * * * * S  E  T
;* * * * * * * * * * * * * *  * * * * * * * *  L  S
-------------------------------------------------------------------------
 H H H H H X X X X X X X X X  L X X X X X X X   EDBAV (1)
 H H H H L X X X X X X X X X  H X X X X X X X
 L L L H H X X X X X X X X X  L X X X X X X X
 L L H L H X H H X X X X X X  L X X H X X X X  EDBAV, CAUX
 L H L L H X L H X X X X X X  L X X H X X X X  (5)
 H L L L H X L L X X X X X X  L X X L X X X X
 L L L L H X H X X X X X X X  H X X H X X X X
 X X X X L H X X X X X X X X  X X H X X X X X  BUS-REQ
 X X X X H H X X X X X X X X  X X L X X X X X
 X X X X L L X X X X X X X X  X X L X X X X X  (10)
 X X X X H L X X X X X X X X  X X L X X X X X
 L L X X X X X H H H H X X  X H X X Z X X X  CPURD, BWRITE
 L H X X X X X X L L L H X X  X L X X Z X X X
 X X X X X X X X L H H L X X  X X X X H X X X
 X X X X X X X X L H L L X X  X X X X H X X X  (15)
 X X X X X X X X L L L L X X  X X X X L X X X
 X X X X X X X X L L H L X X  X X X X H X X X
 X X X X X X X X H L H L X X  X X X X L X X X
 X X X X X X X X H H L L X X  X X X X L X X X
 L L X X X X X L H L H H X X  X H X X X Z X X  CPUWR, BWRITE (20)
 H L X X X X X L L H L H X X  X L X X X Z X X
 H L X X X X X L L L L L X X  X Z X X X H X X
 L H X X X X X L L L H L X X  X Z X X X H X X
 X X X X X X X L L H L L X X  X X X X X L X X
 X X X X X X X L L H H L X X  X X X X X H X X  (25)
 X X X X X X X H L L L L X X  X X X X X H X X
 X X X X X X X H L L H L X X  X X X X X H X X
 X X X X X X X H L H L L X X  X X X X X H X X
 X X X X X X X H L H H L X X  X X X X X H X X
 X X X X X X X X X X X X L X  X X X X X X H X  EDMAAOS (30)
 X X X X X X X X X X X X H X  X X X X X X L X
 X X X X X X X X X X X X L X L  X X X X X X X L  CHAN-SEL
 X X X X X X X X X X X X L X H  X X X X X X X H
 L X X X X X X X X X X H X X  X X X X X X X H
 H X X X X X X X X X X H X X  X X X X X X X L  (35)
 L X L X X X X X X X X H X X  X X X X X X X H
 X X H X X X X X X X X H X X  X X X X X X X L
 X X X X X X X H H L H L X X  X X X X X L X X
-------------------------------------------------------------------------
```

DESCRIPTION

This PAL is used to control read write control lines, generate clock signals, channel select for the serial controller, and bus request. Several of its output pins will be in tri-state during DMA.

SERIAL INTERFACE

LIFT U3050 PIN 11

LIFT U5100 PINS 9, 11, 13

WIRE U3050 PIN 11 TO U5100 PIN 13

WIRE U3050 PAD 11 TO U5100 PIN 9

WIRE U3050 PIN 13 TO U1080 PIN 36

WIRE U5100 PIN 11 TO U5100 PIN 7

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Serial/Assembly No. Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A8	670-8598-01			CIRCUIT BD ASSY:RS232C INTFC	80009	670-8598-01
A8C1021	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C1031	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C1041	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C1051	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C1061	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C1071	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C1081	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C1101	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C1111	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C2021	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C2031	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C2041	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C2051	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C2061	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C2071	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C2111	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C3031	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C3041	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C3051	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C3061	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C3071	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C3081	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C3091	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C3101	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C3111	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C3120	281-0767-00			CAP,FXD,CER DI:330PF,20%,100V	04222	MA106C331MAA
A8C3121	281-0767-00			CAP,FXD,CER DI:330PF,20%,100V	04222	MA106C331MAA
A8C3122	281-0767-00			CAP,FXD,CER DI:330PF,20%,100V	04222	MA106C331MAA
A8C3123	281-0767-00			CAP,FXD,CER DI:330PF,20%,100V	04222	MA106C331MAA
A8C3130	281-0767-00			CAP,FXD,CER DI:330PF,20%,100V	04222	MA106C331MAA
A8C3131	281-0767-00			CAP,FXD,CER DI:330PF,20%,100V	04222	MA106C331MAA
A8C3132	281-0767-00			CAP,FXD,CER DI:330PF,20%,100V	04222	MA106C331MAA
A8C3133	281-0767-00			CAP,FXD,CER DI:330PF,20%,100V	04222	MA106C331MAA
A8C4025	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C4051	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C4061	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C4071	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C4081	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C4091	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C4101	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C4111	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C5013	290-0167-00			CAP,FXD,ELCTLT:10UF,20%,15V	05397	T110B106M015AS
A8C5041	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C5043	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A8C5045	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A8C5051	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C5061	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C5071	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C5081	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C5091	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C5101	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C5111	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8CR5010	152-0066-01			SEMICOND DVC,DI:SELECTED	80009	152-0066-01
A8CR5011	~~152-0066-01~~			SEMICOND DVC,DI:SELECTED	80009	152-0066-01
A8P200	131-3268-00 OR 131-2964-00			CONN,RCPT,ELEC:EUROCARD,RTANG,2 X 32,0.1 SP	00779	531796-2
A8P650	~~131-0812-00~~			CONN,RCPT,ELEC:CKT BD MT,25 CONT,FEMALE	00779	205858-1
A8P660	131-0812-00			CONN,RCPT,ELEC:CKT BD MT,25 CONT,FEMALE	00779	205858-1
A8R1082	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A8R1084	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A8R1102	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A8R1104	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A8R1112	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A8R4010	321-0936-00			RES,FXD,FILM:950K OHM,1%,0.125W,TC=TO	19701	5033ED950K0F
A8R5012	315-0301-00			RES,FXD,FILM:300 OHM,5%,0.25W	57668	NTR25J-E300E
A8R5040	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A8R5042	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A8R5044	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A8R5046	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A8R5048	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A8U1020	156-1111-02			MICROCKT,DGTL:OCTAL BUS XCVRS W/3 ST OUT	01295	SN74LS245N3
A8U1030	156-1065-01			MICROCKT,DGTL:OCTAL D TYPE TRANS LATCHES	04713	SN74LS373 ND/JD
A8U1040	156-1065-01			MICROCKT,DGTL:OCTAL D TYPE TRANS LATCHES	04713	SN74LS373 ND/JD
A8U1050	156-0956-02			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A8U1060	156-0694-02			MICROCKT,DGTL:DECODER/3 LINE TO 8 LINE,SCRN	01295	SN74S138N3/J4
A8U1070	156-1172-03			MICROCKT,DGTL:DUAL 4 BIT BINARY COUNTER	01295	SN74LS393N3/J4
A8U1080	156-1606-00			MICROCKT,DGTL:DMA CONTROLLER	34335	AM9517A-5 DC
A8U1100	156-2076-01			MICROCKT,DGTL:SCC SERIAL COMM CONT,SCRN	56708	Z8530PS
A8U1110	156-0392-03			MICROCKT,DGTL:QUAD LATCH W/CLEAR	07263	74LS175PCQR
A8U2020	156-1111-02			MICROCKT,DGTL:OCTAL BUS XCVRS W/3 ST OUT	01295	SN74LS245N3
A8U2030	156-1111-02			MICROCKT,DGTL:OCTAL BUS XCVRS W/3 ST OUT	01295	SN74LS245N3
A8U2040	156-0956-02			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A8U2050	156-1721-00			MICROCKT,DGTL:OCTAL TRANPARENT LATCH	04713	MC74F373ND
A8U2060	160-2842-00			MICROCKT,DGTL:ARRAY LOGIC,PRGM	80009	160-2842-00
A8U2070	160-2849-00			MICROCKT,DGTL:ARRAY LOGIC,PRGM	80009	160-2849-00
A8U2110	156-0879-01			MICROCKT,DGTL:QUAD LINE DRIVER	04713	MC1488LD
A8U3030	156-1058-01			MICROCKT,DGTL:OCTAL ST BUFFER W/3 STATE OUT	01295	SN74S240JP4
A8U3040	156-0626-02			MICROCKT,DGTL:SCREENED	01295	SN74390NP3
A8U3050	156-0480-02			MICROCKT,DGTL:QUAD 2-INP & GATE	01295	SN74LS08NP3
A8U3060	156-1611-00			MICROCKT,DGTL:DUAL D TYPE EDGE-TRIGGERED FF	~~80009~~	~~156-1611-00~~
A8U3070	156-0479-02			MICROCKT,DGTL:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A8U3080	156-0323-02			MICROCKT,DGTL:HEX INVERTER,BURN-IN	18324	N74S04(NB OR FB)
A8U3090	156-0382-02			MICROCKT,DGTL:QUAD 2 INP NAND GATE BURN	18324	N74LS00NB
A8U3100	156-0385-02			MICROCKT,DGTL:HEX INVERTER	07263	74LS04PCQR
A8U3110	156-0878-01			MICROCKT,DGTL:QUAD LINE RCVR	04713	MC1489LDS
A8U4025	156-2028-00			MICROCKT,DGTL:8-BIT MAGNITUDE COMPARATOR	01295	74AS866
A8U4040	156-0645-02			MICROCKT,DGTL:HEX INV ST NAND GATES	04713	SN74LS14NDS
A8U4050	156-0388-03			MICROCKT,DGTL:DUAL D FLIP-FLOP	01295	SN74LS74ANP3
A8U4060	156-1172-03			MICROCKT,DGTL:DUAL 4 BIT BINARY COUNTER	01295	SN74LS393N3/J4
A8U4070	156-0388-03			MICROCKT,DGTL:DUAL D FLIP-FLOP	01295	SN74LS74ANP3
A8U4080	156-0388-03			MICROCKT,DGTL:DUAL D FLIP-FLOP	01295	SN74LS74ANP3
A8U4090	156-1619-00			MICROCKT,DGTL:LSTTL,QUAD BUS BUFFER,SCRN	04713	SN74LS126AND
A8U4100	156-0388-03			MICROCKT,DGTL:DUAL D FLIP-FLOP	01295	SN74LS74ANP3
A8U4110	156-0879-01			MICROCKT,DGTL:QUAD LINE DRIVER	04713	MC1488LD
A8U5050	156-0388-03			MICROCKT,DGTL:DUAL D FLIP-FLOP	01295	SN74LS74ANP3
A8U5060	156-0388-03			MICROCKT,DGTL:DUAL D FLIP-FLOP	01295	SN74LS74ANP3
A8U5070	156-0388-03			MICROCKT,DGTL:DUAL D FLIP-FLOP	01295	SN74LS74ANP3
A8U5080	156-1172-03			MICROCKT,DGTL:DUAL 4 BIT BINARY COUNTER	01295	SN74LS393N3/J4
A8U5090	156-0481-02			MICROCKT,DGTL:TRIPLE 3-INP & GATE	01295	SN74LS11NP3
A8U5100	156-0388-03			MICROCKT,DGTL:DUAL D FLIP-FLOP	01295	SN74LS74ANP3
A8U5110	156-0878-01			MICROCKT,DGTL:QUAD LINE RCVR	04713	MC1489LDS
A8Y3020	119-1799-00			OSC,XTAL CLOCK:19.660MHZ,0.01%	09969	XO-43B-19.6608

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