

# SPHERE 300

CORPORATION

OPERATOR AND REFERENCE MANUAL  
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SPHERE 1 COMPUTER SYSTEM OPERATOR AND REFERENCE MANUAL SET

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**ABSTRACT:**

This document gives a brief overview of computing in general and gives detailed examples and guidelines to the assembly and use of the SPHERE 300 series computers and those components manufactured by SPHERE CORPORATION.

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INTRODUCTION

The purpose of this manual set is to provide the user with information that will aid him in solving problems. Because of its great cost reduction the SPHERE computer system has introduced computing to many new applications. These new applications are often thought up by first time computer users, therefore, a new approach to the manual organization has been taken. There are sections which should be of interest to the hobbyist, other sections will satisfy the needs of the advanced user, and others will be of interest to both advanced and novice users. It would be suggested that you glance through the information that is found in this manual so that you may effectively use it for future reference.

## 1.1

SYSTEM DESCRIPTION

The SPHERE system contains a central processor, memory, input and output devices just as other digital computers on the market today. The system is a fully capable general purpose computer. Because of its size one might be deceived into believing that it has limited capability. The SPHERE system is far more capable than the UNIVAC 1 which cost \$1,000,000 to insurance and other firms in early commercial computing. Yet one UNIVAC 1 was used to handle the maintenance, billing, and claims of a million different insurance policies. A million dollars for a UNIVAC 1 was an honest cost justified expense which saved many millions of dollars. The advent of the microprocessor has reduced the size and price of the computer. Computing ability and computing speed continue to increase. These capability increases mean substantial changes in the way we think about computers. When the computer cost \$1,000,000, a million dollars to program the computer to run "efficiently" was justifiable. Today, a million dollar programming effort on a \$1,000 or less computer is ridiculous. People and their time are valuable. COMPUTING EFFICIENCY AT THE EXPENSE OF A VALUABLE PERSON'S TIME is a waste of a valuable resource. The SPHERE system is the first designed around people and their needs.

## 1.1.1

SOFTWARE

The Program Development System (PDS) includes an EDITOR, MINI-ASSEMBLER, and a debugging package. It also may include a CRT, floppy disk and audio cassette software drivers. Although most computer processing occurs at the character (8 BIT) level, it is sometimes desirable to use 16 bit arithmetic so we have provided an extended 16 bit instruction set in the PDS system. This package rounds out the "SYSTEM" concept for our smallest systems. There are proponents of various computer languages everywhere. Each language is suited more or less to a specific group of applications. Although the advent of the microprocessor really

## 1 INTRODUCTION

### 1.1 SYSTEM DESCRIPTION

#### 1.1.1 SOFTWARE cont'd

dictates some new philosophies in computing language, the BASIC language seems to come closest to this philosophy. Because of its widespread use we have selected it to be our first computer language. A SPHERE operating system is supplied to all users of SPHERE equipment. The software is set up to the configuration required for that system's hardware. This system includes a comprehensive 300 page operator's manual. The software supplied to make the SPHERE system a useful "SYSTEM" is attractive; however, the real contribution that SPHERE offers is one of commitment. The SPHERE "SYSTEM" concept demonstrates only the surface of the real technological advances that are possible when true design innovation is combined with foresight and state-of-the-art technology. The SPHERE "SYSTEM" concept is the commitment. The fundamentals of software are discussed in section 2.3. Details on SPHERE software are contained in section 9.

#### 1.1.2 HARDWARE

The SPHERE computer system was designed to provide an uncompromising computer system at minimal cost. The keyword to the design is the word "SYSTEM". Every phase of the design has been influenced by the "SYSTEM" philosophy. To justify the system title, a "COMPUTER" must perform an application acceptably. Recently, the cost of peripherals and software have substantially exceeded the cost of the computer, but without them, a computer cannot perform much of anything acceptably. With the onset of the microprocessor, real design innovations have been possible, but without the system philosophy, a microprocessor can only reduce the processor cost. Peripherals, memory, and software continue to be expensive. The SPHERE computer is uniquely cost effective because it utilizes real design innovations to reduce the amount of circuitry required throughout the system. The SPHERE add-on memory board will support 4, 8, 12, or 16K of dynamic random access memory. Our power supply has been placed in a separate chassis to eliminate a common source of heat. This allows the system to run cooler and eliminates the need for an expensive fan. The system uses a standard TV monitor for a 512 character display. The use of the TV and other common components has reduced the cost and allowed more machine versatility. Further cost reductions have been achieved by replacing the front console (lights and switches) with the TV terminal, keyboard, and a program in Read Only Memory (ROM) that performs the same function, only better. The CPU card is packaged to provide all of the basic functions required by a useful system, thereby eliminating

1 INTRODUCTION  
1.1 SYSTEM DESCRIPTION  
1.1.2 HARDWARE cont'd

unnecessary extra PC BOARDS. Peripherals that are available with our system include a low cost line printer, audio cassette, teletype, modem, and a floppy disk. Also available is a programmable digital Input/Output port. The SPHERE system also supports its own set of terminals, the lowest cost terminals available today.

1.2 DIGITAL COMPUTER HISTORY

The digital computer is an outgrowth of thought and effort spanning three centuries, directed at reducing the time and tedium of human calculation. Blaise Pascal, the French mathematician and philosopher, developed in 1642 the first mechanical calculating machine. Proposals for new, and more powerful, computing devices appear in nineteenth century literature. In 1812 the Englishman, Charles Babbage, constructed in mechanical form the recognized prototype of the computer. His "analytical engine" had a "store" (the equivalent of internal memory) and a "mill" (the equivalent of an arithmetic unit), and it was designed to accept input data in the form of cards with holes in them, an idea that Babbage borrowed from Jacquard's loom. In 1889, Herman Hollerith, a statistician employed by the United States government, developed and patented the first line of primitive punched-card equipment consisting of a punch, a sorter, and a tabulator, to aid in the compilation of the 1890 census data. The era of the modern computer dates from the late 1930's. The years 1939 to 1944 mark the successful development, at Harvard University, of the first automatic, general-purpose digital computer (electro-mechanical). The Automatic Sequence Controlled Calculator, as the machine was called, was developed by Professor Howard Aiken with financial and technical assistance from the IBM Corporation. At about the same time, pioneering work in this area was also being done by George Stibitz of Bell Laboratories, who developed an electro-mechanical automatic digital computer. Concepts of modern digital computers were defined in detail between 1943 and 1946 by John von Neumann, a Hungarian mathematician working at Princeton University, and by the team of J. P. Eckert and J. W. Mauchly of the University of Pennsylvania, who perfected and built ENIAC (Electronic Numerical Integrator and Computer), the first electronic digital computer, in 1946.

# 1 INTRODUCTION

## 1.1 SYSTEM DESCRIPTION

## 1.2 DIGITAL COMPUTER HISTORY cont'd

Since then, the development of computer technology has accelerated in an explosive fashion. Never before has a technological product been developed and improved to such an extent over such a brief period. The modern computer is a far cry from its calculating precursors indeed. It must be pointed out that the connotation of the term "computer" is now, unfortunately, somewhat misleading as it evokes the image of "computing", i.e., some arithmetic operation with its manipulation of numerical data. The notion that the computer is a strictly numerical device is quite incorrect. A computer is basically a symbol-manipulating device and numerical symbols are merely one of the symbol classes that the computer can manipulate. The computer is a machine that duplicates and amplifies certain powers of the human mind. It provides an extension to man's intellect. It has been called the universal machine and man's ultimate machine. In the latter sense, it is seen as the supreme technological achievement, because the computer deals not in raw power but in the sublime, abstract processes of mental work. In this connection, we should realize that before the advent of computers, practically every other tool or machine ever invented and built served as an extension of man's legs (locomotion), back muscles (materials displacement), or arms and hands (manufacturing). Today's most advanced machines such as the bulldozer, the combine, the automatic machine tool, the jet plane, and the rocket-powered space vehicle all belong to this category. The computer, on the other hand, is in a category all by itself. It does not, alone, achieve any physical feats whatever. It can plan and control physical action by other machines (and men), but its own output is always symbolic and therefore abstract. The symbols that a computer has the ability to manipulate are numerical digits, letters of the alphabet, special characters, and sub-characters or bits which represent information in the form of data. A computer processes information by means of receiving, storing (remembering), operating on, and producing (output) data. These information-handling operations are directed by a program of instructions which itself is stored in the computer's memory. This principle of utilizing, internally stored, alterable instructions to control the action of the machine is what provides the computer with a versatility, a logical flexibility, and an open-endedness that are not matched by anything short of a living organism. In addition to duplicating certain intellectual processes, a computer is also capable of performing clerical tasks that can be viewed as routines performed by rote, such as the retrieval of records, posting and filing, i.e., record keeping, as well as transmitting, regenerating, and display of information over distance. Although the computer is relatively limited, as compared to the human mind in its range of capability and although it uses rather crude methods of internal processing, it has the advantages of speed, total recall, and complete





2 STARTING AT THE BOTTOM  
 2.1 COMPUTER LOGIC FUNDAMENTALS cont'd

In addition to the graphic representation of a gate, a functional representation of a gate would be listed in a logic table or logic diagram. Here inputs and their states (one or zero) are listed in a tabular form so that matching a desired row and column will indicate the correct output state. An "and" gate logic diagram appears in figure 2.2.

FIGURE 2.2

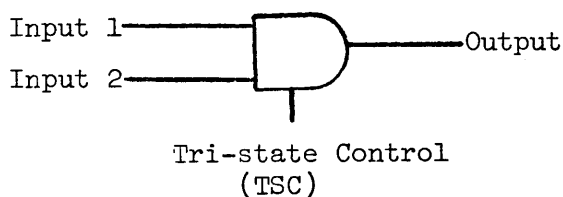
AND Gate Truth Table

Inputs		Output
0	0	0
0	1	0
1	0	0
1	1	1

The output of a standard TTL gate can usually supply enough current to wire to the inputs of 10 other standard TTL gates (10 standard loads). Only one standard TTL output can be on any wire at any one time, two gates cannot usually output onto the same wire. Other forms of non-standard TTL logic exist but some design consideration must be made when using these devices. Some types are low power, high speed, schottky, low power schottky, CMOS, and other "compatible" MOS. Each non-standard TTL or compatible device should be checked for power compatibility with respect to the number of loads each will drive with respect to another. Two types of TTL logic not mentioned here-to-fore are Tri-state and Open Collector. Tri-state (sometimes called high impedance state) does not mean a third set of voltages which indicate a third state. It simply means that the output gate has been disconnected from the line. This is useful when many different output gates would like to use the same wire to communicate at mutually independent times (party line). Computer systems use this philosophy extensively. An "and" gate that has Tri-state capability is illustrated in figure 2.3. It's logic diagram is shown in figure 2.4.

FIGURE 2.3

Tri-state AND Gate



2 STARTING AT THE BOTTOM  
 2.1 COMPUTER LOGIC FUNDAMENTALS cont'd

FIGURE 2.4

Tri-state AND Gate Truth Table

Inputs			Output
1	2	TSC	
∅	∅	1	∅
∅	1	1	∅
1	∅	1	∅
1	1	1	1
*	*	∅	*

\*high impedance output state

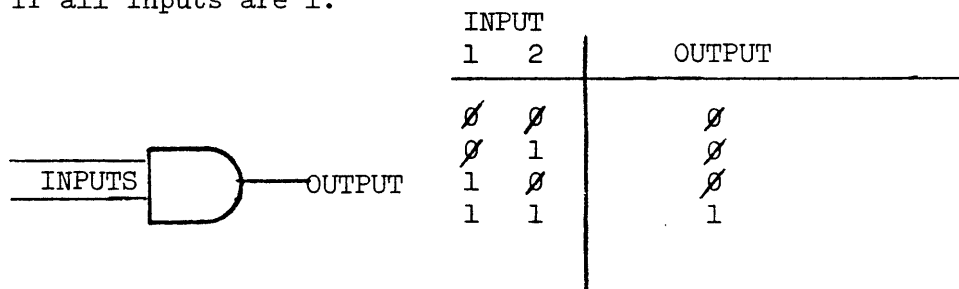
If an "\*" appears in the input side of a logic diagram it indicates a "don't care" state. In other words, that input is not used to calculate the output if other conditions of the logic diagram are met.

Normally, only one output is used to connect to inputs of other gates as needed (within load limits). When this rule is violated, circuit damage will result. This is not true of party line (tri-state or open collector) circuits. Tri-state places only one output on the line at a time. Open collector, on the other hand, simply has protective circuitry to eliminate possible damage due to multiple outputs on the same line. If any output is off, the combined output will be off, otherwise it will be on. Figures 2.5 through 2.12 illustrate some common gates.

FIGURE 2.5

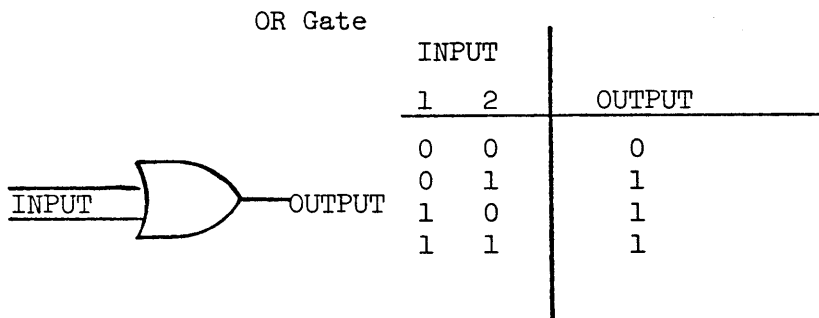
AND Gate

The AND gate takes several inputs and produces a 1 output if all inputs are 1.



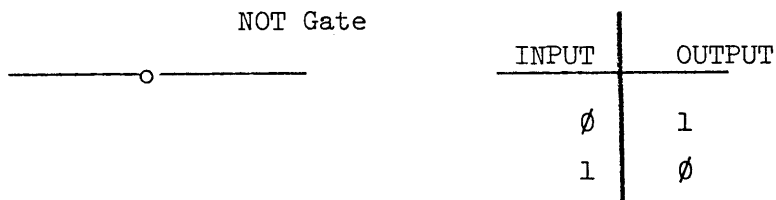
2 STARTING AT THE BOTTOM  
 2.1 COMPUTER LOGIC FUNDAMENTALS cont'd

FIGURE 2.6



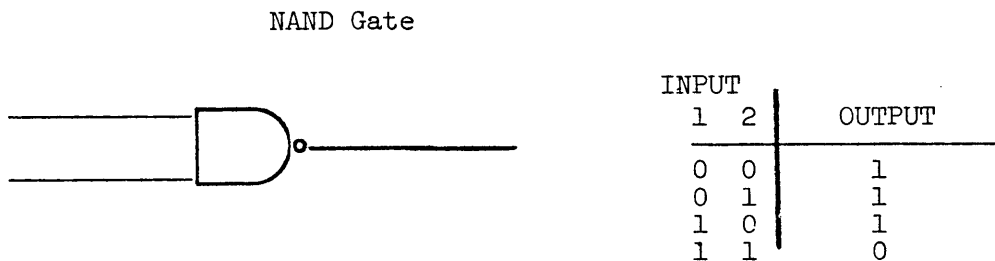
An OR gate takes several inputs and produces a 1 output if any input is a 1.

FIGURE 2.7



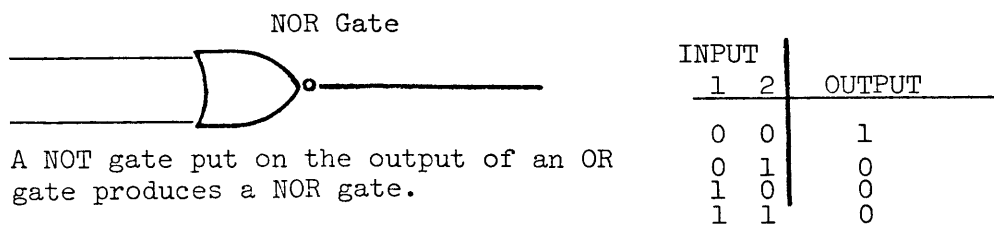
A NOT gate inverts the signal to produce the opposite output.

FIGURE 2.8



A NOT gate put on the output of an AND gate produces a NAND gate.

FIGURE 2.9

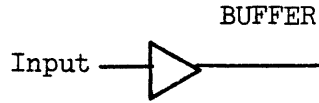


A NOT gate put on the output of an OR gate produces a NOR gate.

2 STARTING AT THE BOTTOM  
 2.1 COMPUTER LOGIC FUNDAMENTALS cont'd

FIGURE 2.10

BUFFER GATE



INPUT	OUTPUT
0	0
1	1

A Buffer gate allows a single load line to drive 10 output lead lines.

FIGURE 2.11

INVERTING GATE

INVERTER



INPUT	OUTPUT
0	1
1	0

When a NOT gate is added to a Buffer it becomes an inverter.

FIGURE 2.12

EXCLUSIVE OR GATE



INPUT		OUTPUT
1	2	
0	0	0
0	1	1
1	0	1
1	1	0

Often, a complex set of gates will simply be expressed as a box with inputs and outputs identified. A description and logic diagram will accompany such descriptions. If the circuit is repetitive in function such as an adder or shift register, a sample circuit and/or logic diagram will be documented. Through the use of new technology, logic gates have successively grown smaller. Now thousands of these gate circuits can fit in a package the size of a postage stamp. These circuits are called integrated circuits (IC's). They are combined in various fashions to create simple memories, complex memories, complete computer processors (CPU's) and a whole array of other circuits. In commercial applications, they are usually packaged in dual in-line packages (DIP). These are some times referred to as "Bugs" as they appear to have a body and many legs. The legs are spaced at .10 inches and are designed to be inserted into printed circuit boards for subsequent soldering. Appendix D includes descriptions of circuits

## 2 STARTING AT THE BOTTOM

### 2.1 COMPUTER LOGIC FUNDAMENTALS cont'd

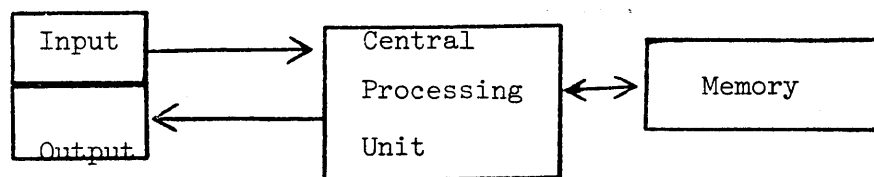
used in the SPHERE Computing systems. It includes reference information for maintenance and theory. Consult IC manufacturers' literature for more detailed information.

### 2.2 COMPUTER ARCHITECTURE

Computers and buildings are designed by architects to perform various functions. In many ways their design is similar, they each have basic components that are required, then materials are selected and arranged in a suitable form. Computer architecture refers to what units are to be in a computer system and their characteristics and interconnections. Some units, such as the arithmetic unit, are composed solely of logic circuits designed to perform a particular function. Other units may be mostly mechanical in nature such as card readers or teleprinters. A computer is basically a data manipulation machine. It transforms one set of data into another set according to a fixed list of instructions called a program. To accomplish this, a computer contains several units to move and change data. The basic unit is a Central Processing Unit (CPU), which interprets the program commands and does the requested data manipulation. Another basic unit is the memory, which stores the data used by the system. Also needed are units to perform input and output on the stored data. A general configuration would be similar to the one shown in Figure 2.13.

FIGURE 2.13

GENERAL COMPUTER CONFIGURATION

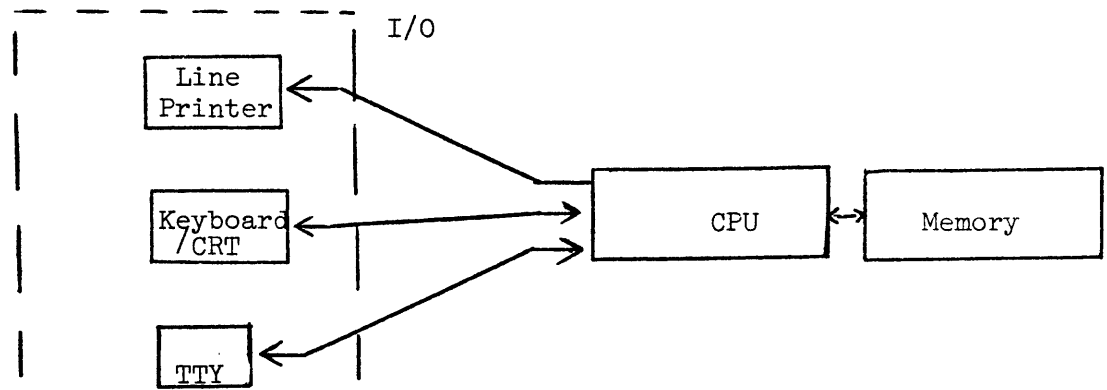


Computers are fast accurate and inflexible while the humans that use them are slow, clumsy, and flexible. The interface between the two has always been a problem. In the early days of computing, the most widely used devices for input and output were the 80 column card and a printer running at 150 to 600 lines a minute. The machine would stop computing during I/O and would usually spend the majority of its time waiting for the I/O to be completed. The man would spend two or three days waiting to get his program keypunched, run on the computer and the results back. This was very wasteful for both man and machine. To improve ease of use, time-sharing and multiprogramming systems were developed in the early 60's. Multiprogramming allowed several programs

2 STARTING AT THE BOTTOM  
2.2 COMPUTER ARCHITECTURE cont'd

to be in the machine at a time with one running while the others performed I/O, thus greatly improving machine usage. Time-sharing allowed several users multiple access to a computer at the same time. The user would use a teleprinter or a CRT (cathode ray tube) display to enter information directly into the machine. These developments allowed better use of very expensive machines. With the progress in electronics the price of computer systems fell during the 70's to the point where a small computer was less than the cost of an earlier terminal. A typical system of this type is the SPHERE which allows I/O to be performed with the keyboard/CRT, printer, teletype, or digital I/O lines. A typical computer would then look as in Figure 2.14.

FIGURE 2.14

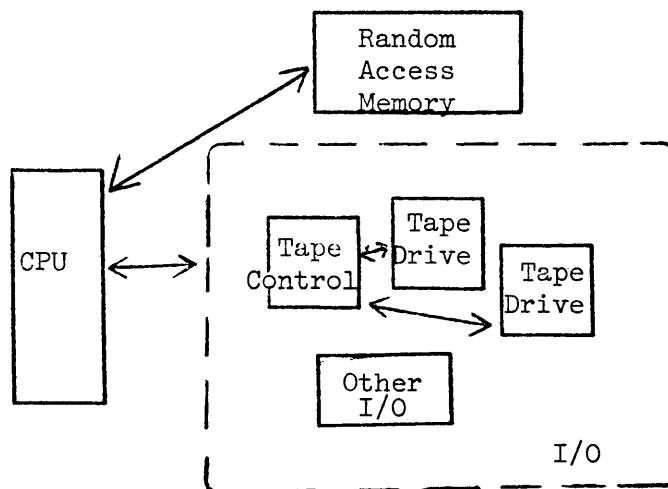


Once the data is entered into the computer, it must be stored for access by the CPU as needed. There are several types of memory available with different costs and speed. Memory devices fall into two main categories, sequential devices and random access devices. Sequential memories are those where each unit of memory is ordered one after the other so that the data is accessed in a specific order. Typical are magnetic tape units or cassette tapes. Sequential units offer the lowest cost per unit of information but have the longest access time to a specific information unit. It is useful in applications where there is a lot of information to be processed in a specific unvarying order. Random Access Memories (RAM) are those where the time to retrieve any random unit is the same as for any other data unit. This type of memory offers the fastest unit access but has the smallest storage capacity. This is the memory accessed directly by the CPU when it is executing a program. High speed memory has traditionally been made out of ferrite "cores", so called because each resembles a doughnut in shape with read, write and sense wires run throughout the hole or "core" of the doughnut. Random access memories can also be made up of flip-flops, which is an electrical circuit capable of storing one binary digit. The flip-flop was originally used in designing circuits for the purpose of storing the

2 STARTING AT THE BOTTOM  
2.2 COMPUTER ARCHITECTURE cont'd

output of other circuits so that circuits would have access to previous results. With the advent of metallic oxide semiconductor large scale integration (MOS LSI) circuits, it has become possible to put several thousand flip-flop circuits on a single chip. The SPHERE uses such chips with 4096 (4K) bits (binary digits) of memory on each chip. Even though the memory is now semiconductor, it is often still referred to as "core" memory to denote that it is the memory used by the CPU for storage of executing programs and data. Disk and drum memories are devices that are both sequential and random access in nature, offering moderate size at moderate cost. They consist of a disk or drum that is coated with a magnetic material rotating continuously past a set of read or write heads. There is one 'track' of data under each read or write head. The devices are random access in that any given data is accessible within an average period of time. This is called the 'access time' and averages one half the time it takes the disk to rotate once. On most disk units, there is only one read or write head which is movable between tracks. There is then a track latency or access time to move the head to the proper track. The disk used on the SPHERE is a "floppy" disk with 64 tracks having 4096 bytes of data per track. The type of memory used is thus determined by tradeoffs of access time, capacity and cost with access time increasing with storage capacity (floppy) and decreasing with cost (semi-conductor RAM). Devices which require physical movement to access data are usually referenced through a control unit designed to interface that device to the CPU. A typical system would appear as in Figure 2.15.

FIGURE 2.15





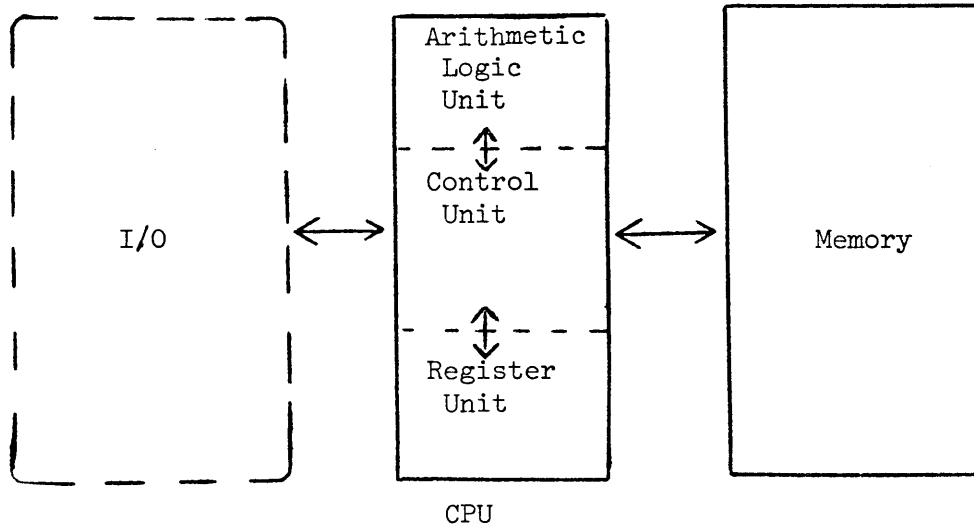
## 2 STARTING AT THE BOTTOM

### 2.2 COMPUTER ARCHITECTURE cont'd

The CPU carries out the instructions of the program for manipulating the data. It is composed of three main subunits, the arithmetic/logic unit (ALU), the register unit, and the control unit. The arithmetic/logic unit does the actual data manipulation performing such arithmetic functions as addition and subtraction, and such logical functions as comparing two units of data, shifting them and performing "AND", "OR", "XOR" and other functions on the individual bits of data. The registers act as storage for specific units of data. The registers are accumulators, index registers, the program counter and the stack pointer. An accumulator is a storage location used by the ALU. An instruction such as ADD A would take the contents of the accumulator and the contents of a memory location and add them together and put the result in the accumulator. The index register is used as a pointer into main memory. Its contents can be added to a fixed starting address for accessing arrays of data. The stack pointer is used for referencing the stack. A stack is an area of main memory reserved for sequential accessing. Information in the stack is referenced on a last-in-is-first-out (LIFO) basis. It is used to store temporary data and subroutine linkage return addresses during program jumps. While most data has fixed locations (addresses) in main memory during execution of a program, the stack data varies dynamically during execution of a program. All references to data on the stack are from the top-of-stack (TOS) which is implicit in any stack operation. The stack pointer is sometimes referred to as the TOS pointer register. The index register can be used to reference data a given distance from the TOS. This allows programs to be dynamically assigned blocks of data as needed. The program counter is pointer into main memory, pointing to the location of the next program instruction to be executed. It is changed either automatically with each instruction execution or modified by the program to change the instruction flow. The control unit of the CPU takes the program instructions, determines what is to be done, then activates the various gates, registers, adders, etc. to perform the requested operations. It also tests the results of instructions to determine what location the next instruction is to be taken from. In a computer, while all data consists of binary digits, these bits are grouped into bigger units of data for manipulation by the computer. The basic unit is the byte, which consists of 8 bits. A byte can thus contain a value between 0 and 255 decimal. It is used most frequently for representing a written character such as 'A', 'B', or '+'. Because it can't contain a very big number, bytes are put into larger groupings called words, which usually contain 4 bytes (32 bits) on large computers and 2 bytes (16 bits) on small computers. The basic unit used on the SPHERE is the byte, thus making it ideal for character and text manipulation.

2 STARTING AT THE BOTTOM  
2.2 COMPUTER ARCHITECTURE cont'd

FIGURE 2.16  
COMPONENTS OF THE CPU



2.3 SOFTWARE

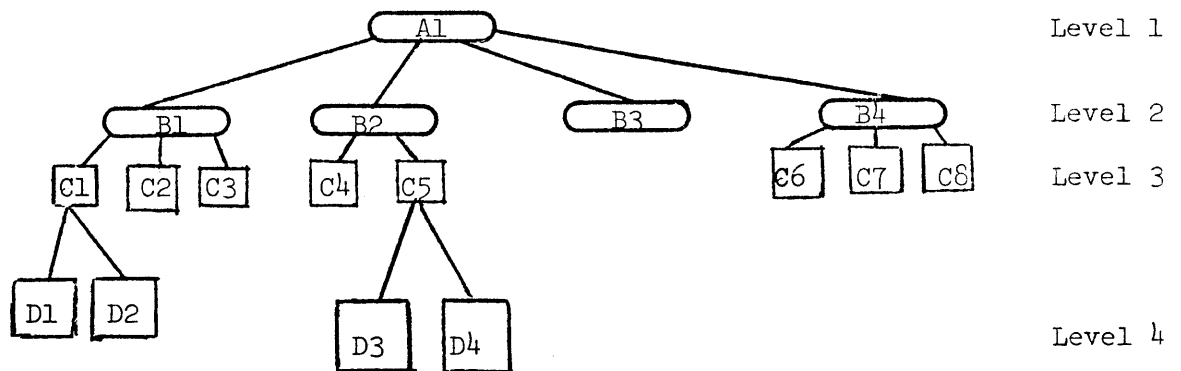
While a computer is a very sophisticated piece of circuitry, it is absolutely useless without being told what to do. It must be given instructions on how to handle the data. A computer program is basically a set of such instructions for handling data. Software consists of all the programs and data needed by a computer system to produce useful results. An analogy of a computer program could be made with a country post office that could only hire a moron as postmaster. Unfortunately, while being a conscientious worker, he can't remember how to do his job. So someone must continually tell him what to do. Because no one else is around for that job, the post office management decided to leave instructions for him to follow on what to do to get the job of sorting the mail done. In order to help the moron keep track of the large number of instructions he had to follow, they were put in unused slots in the sorting bin, one instruction per slot. The instructions had to be very simple for the moron to follow. Typical instructions would be like "Pick up a letter from the mail pile", or "if the letter lacks a stamp, take your next instruction from slot #57. On coming to work in the morning, the moron would take the first instruction from slot #1, then another from box #2 and so forth unless the instruction specifically said to go to another box for the next instruction. By following each instruction, the moron could then perform any task the Post Office could think of. A computer is very similar. The computer's central processing unit (CPU) is the moron, slavishly following the instructions that it takes from memory. Memory consists of a set of numbered locations, with each location or memory cell con-

2 STARTING AT THE BOTTOM  
2.3 SOFTWARE

taining an instruction or an item of data. Having a computer "moron" do useful work for you thus becomes a task of producing an explicit set of instructions for it to follow. The set of instructions is called a "program" and the task of producing them is called programming. The task of programming can be broken down into several steps. The first step is to analyze the problem. What does the problem consist of? What information is used and what is the desired output. Defining the boundaries to the problem area is one of the most critical in producing a workable solution. Once the problem has been defined, it can be broken up into modules for ease of handling since most problems are too large to tackle in one piece. These are then further subdivided into smaller modules. This subdividing continues until the modules are small enough to work with. A diagram of such a top-down modularized structure would appear as in Figure 2.17.

FIGURE 2.17

TOP DOWN STRUCTURING

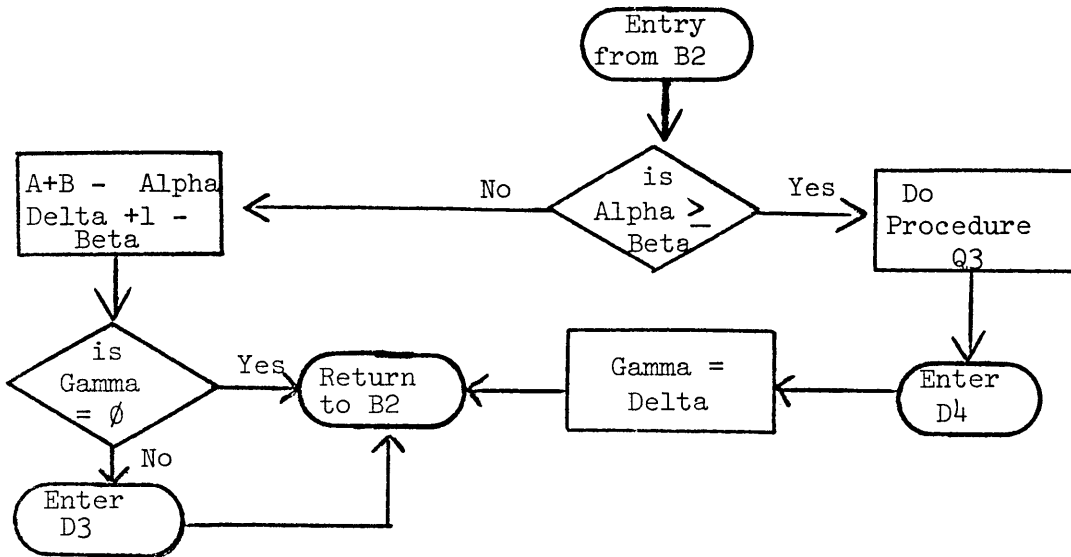


Each module on any given level is independent of any other module on that level, but are connected by modules on higher levels. This enables one part of the program to be changed with minimal effects on other parts of the program. After the overall problem has been modularized, a detailed diagram description called a flowchart can be produced describing each step in a given module. Module C5 might appear as the example in Figure 2.18.

2 STARTING AT THE BOTTOM  
 2.3 SOFTWARE

FIGURE 2.18

FLOWCHART OF MODULE C5



For clarity, a complex function such as procedure Q3 can be described on a separate flow chart. By using this process of zooming in for more detailed descriptions, flow charts can be kept simple and understandable. After a detailed description of the problem and the procedures used in producing the result have been written, the flow charts can be used to translate or 'code' the processes into a computer language most suitable for that application, such as BASIC, RPG or FORTRAN. When the program has been coded, it is run on the computer and the process of debugging begins. Debugging is the process of getting a program to work correctly. Bugs are errors in the program. There are two types of bugs: syntactic and semantic. Syntax errors are those that do something not allowed by the programming language, such as jumping to a nonexistent statement or something like  $A \leftarrow B)0$ . These bugs should be recognized by the language and an error message given. Semantic bugs are where the programmer says one thing but means another, such as subtracting a number where it should have been added. These errors in meaning must be found by testing each module with preselected input data for which the result is known. After the bugs are found, the program must be corrected and debugged again, as correcting one bug may result in another bug. Remember Murphey's third law: "If anything can go wrong, it will, but only after it appears to be correct". After the program is debugged and running, the question must be asked "is the information the computer is producing what I really needed in the first place?". Errors can be made in the original problem analysis and not show up until you tell the prospective user what he can do with

## 2 STARTING AT THE BOTTOM

### 2.3 SOFTWARE cont'd

your program. In order to help the user develop his programs, computers come supplied with a set of programs called system software, which is designed to make the computer easier to use. The basic system software program is the executive or operating system. The executive schedules and runs all of the users programs and schedules the input/output operations. It does all of the file handling; including device assignment and logical name/physical device translation. In a multiprogramming or time sharing system, it determines which program is to run at any given time. The executive can be thought of as the chief decision maker of the computer system. Most useful of all systems as far as the programmer is concerned, are the computer languages available to write programs with. A computer language is nothing more than a restricted set of instructions understandable by both computer and human. The most basic computer language is machine language, which consists of the actual binary numbers executed by the CPU. Because strings of binary numbers are hard for humans to use, a form of it called an Assembly Language has been developed. Assembly Language allows symbolic names to be used instead of binary numbers. For instance, the mnemonic ABA (add accumulator B to accumulator A) would stand for the binary number 00011011. Because this is still a very constrained format, high level languages such as BASIC, RPG 11, TRAC or COBOL have been developed. A high level language would allow a statement such as  $A=B+C - (D/5)$  instead of the equivalent 10 or 15 assembly instructions. Each high level language is aimed at a specific users such as COBOL (Common Business Oriented Language) for business use, ALGOL (ALGOrithmic Language) for scientific uses, BASIC (Beginners All purpose Symbolic Interpretive Computer) for novice users, and TRAC (Text Reconing and Compiling) for text and character manipulation. High level languages fall into two major divisions, compilers and interpreters. A compiler translates from the high level language directly into machine language, which is then the program that the computer executes. The high level language program is called the source code or source language and the machine language translation is known as object code or object program. An interpreter doesn't translate the program into machine language but interprets each statement as the program is executed. For short programs, an interpreter will run fast as it doesn't have any 'compile time' overhead, that is, it doesn't spend any time in translating to machine language. However, a compiled program will execute seven to ten times faster than an interpreted version. Another segment of system software is the utility programs. These programs consist of such goodies as text editors, used for creating and changing source language programs; file utilities, used for changing or manipulating files; linkers to hook different programs together and other useful programs. No matter what high level language is used, it will contain certain features for the implementation of programs.

2 STARTING AT THE BOTTOM  
2.3 SOFTWARE cont'd

These features may vary widely from language to language in how they are implemented, but their functions are similar as to what they do. The most basic construct is the arithmetic statement. This statement allows a number to be calculated from an arithmetic expression of variables and constants, and to be assigned to another variable. A variable is a number that has a name and that can change in value during execution of the program. Typical arithmetic statements appear in Figure 2.19.

FIGURE 2.19

SAMPLE ARITHMETIC STATEMENTS

```
ALPHA ← A x B + 5.1 - (3.2÷C);  
LET ALPHA = A * B + 5.1 - (3.2/C)  
ALPHA EQUALS A TIMES B PLUS 5.1 MINUS 3.2 DIVIDED BY C.  
#(DS, ALPHA #(SB, #(AD, #(ML, A B), 5.1), #(DV, 3.2, C)))
```

An arithmetic statement also makes use of built in functions such as sine, cosine and square root as well as operators like add and subtract. There must, of course, be input/output statements, or else what the computer does is not very useful. These statements move data to and from the executing program and another data source, such as a file, a teleprinter, paper tape, or another program. These statements can also be used to format the data so it appears in a desired manner. A logical instruction is a statement that compares two values and returns a value of 1 or 0 depending on whether the comparison was true or false. The logical expression is used with the control statement to provide run time control of which statements are executed. The simplest control command, the branch, is of the form GO TO X which causes the computer to branch and start executing at the statement labeled X. A conditional branch would use a logical expression for a statement like 'IF ALPHA  $\geq$  1 THEN GO TO X'. Individual statements can be executed in statements such as 'IF GAMMA=0 THEN ALPHA ← A+B ELSE ALPHA ← 0'. Another form of control statement is the loop. The loop causes repeated execution of a block of code until a specific logical condition is met. A typical format would be 'WHILE A  $\geq$  1 DO XXX is a series of statements. Usually, each time the block of code is executed a value can change by a specific amount such as

## 2 STARTING AT THE BOTTOM

### 2.3 SOFTWARE cont'd

'WHILE A > 1 STEP A BY 2 DO XXX'; which would increase the value of A by 2 each time through the loop. As programmers, like most other people, are somewhat lazy and don't like to do more work than they have to they invented the subroutine. A subroutine is a segment of code that can be used several times in different places in the program. This makes programs much easier to write, as certain functions are made use of repeatedly. A subroutine is defined once and then explicitly called later in the program for greater flexibility, each time a subroutine is called, different numbers or data can be passed to the subroutine from the main program. This allows it to act similar to a built in function such as SINE. By the use of software, the computer can become a very useful tool. Without it, it is nothing more than a pile of unused electronic parts.

### 2.4 APPLICATIONS

A computer is a general purpose tool for problem solving. A piece of hardware called a "general purpose computer" can perform absolutely nothing by itself because there is no such thing as a general purpose problem. A piece of software designed specifically to "apply" some general purpose computing power to solve a specific problem is called an "application" program. Not all software (programs) are written to solve a specific problem. Some are written specifically to aid application programs performance. These "SYSTEM" programs make the computer more useful to a greater number of application programs. All programs are not application programs. Almost any problem that takes mental effort can be solved by a computer with an appropriate application program. A computer then is a problem solving tool which, if used properly, can provide the user the ability to solve his problems. There are as many applications as there are imaginations. There are, however, general application subjects that we would like to illustrate so that you can understand how a typical non-computer activity is transformed into an application on a computer. We will illustrate an accounting problem.

Late in December the last month of the taxable year, Arthur Morton and his wife Lois, engage you to prepare their income tax return and advise them concerning other matters that may affect the amount of their tax liability. They are entitled to a total of five exemptions for themselves and their dependent children. They have been using the cash method of determining taxable income and expect to file a joint return.

Mr. Morton is employed at a salary of \$24,000 for the current year and has been notified that he will receive an increase of \$300.00 per month, effective

## 2 STARTING AT THE BOTTOM

### 2.4 APPLICATIONS cont'd

in January. He has no deductible expenses connected with his employment. Income from dividends for the current year will amount to \$900.00 for Mr. Morton and \$400.00 for Mrs. Morton.

During the current year, Mr. Morton sold "A" company stock at a loss of \$1,000.00. He proposes to sell his holdings with "B" company stock before the end of the year. These were acquired three years ago at a cost of \$2,000, and the market price which has been relatively stable is currently \$3,000.00. He plans to use the funds to pay amounts pledged to his church, \$500.00 for operating budget and \$2,500.00 for building fund both due by the following March 31st. He also suggest that it might be advantageous to use the \$1,000.00 loss on the sale of "A" company stock as an effort to gain on "B" company stock.

Miscellaneous payments for the current year to date that would qualify as deductions from gross income total \$400.00. In addition, real estate taxes of \$350.00 for the first half of the year have been paid. Unpaid real estate taxes of \$350.00 for the second half of the year are due on December 31st, but may be paid as late as January 10 without penalty.

This illustration is a painful but real life situation. By attempting to do this income tax problem, you would have a lot of headaches in researching the tax exemptions. In addition, computing the appropriate amount of exemption to determine the amount of tax you need to pay would be difficult. At some point in time many other individuals have had to encounter each of the problems Mr. Morton of our example had to research. A Tax Consultant might write a computer program which considers these possibilities in detail. He would include all information necessary to advise of wise future tax decisions and current tax liabilities. All you would need to do with this computer program is input the information listed in the above problem and the computer determine your legal tax exemptions. Then it would determine the amount which you could deduct so as to save as much of your income from taxes as possible. The computer could also inform you of the status of your total asset holding, liabilities and cash balances through the use of its many intelligence. Applications such as this



2 STARTING AT THE BOTTOM  
2.4 APPLICATIONS cont'd

are virtually unlimited and each can be efficiently handled by a computer. Following is a list of common applications:

BUSINESS

- cash receipts
- cash disbursement
- notes receivable and interest income
- retail method of inventory costing
- perpetual inventory control
- depreciation based on averages
- intangible asset amortization
- journal recording and posting
- depletion schedules
- mortgage amortization schedules
- payroll deduction computation
- checking account balance
- taxes payable
- and many, many more

EDUCATION

- test checking and Scoring
- student records
- teacher evaluation
- book index
- class scheduling
- periodical referencing
- audio-visual cataloging
- current subject reference
- rare document storage
- great talks and speeches
- teacher planning
- thesis research
- and many, many more

REAL ESTATE

- prospective customer index
- property categorizing
- multiple listings index
- residential development program
- mortgage and interest compiler
- proposed commercial development format
- monthly payment breakdown
- and more

2 STARTING AT THE BOTTOM  
2.4 APPLICATIONS cont'd

SCIENCE

physics experiment  
chemical analysis  
motion study  
sound and wave investigation  
zoological reference and documentation  
biological reference and documentation  
testing and experimentation  
cross reference index  
geological survey studies  
geothermal research  
solar energy analysis  
and the list goes on

BANKING

accounts receivable  
savings deposits  
certificates of deposit  
checking account balance  
notes receivable  
customer credit information  
federal reserve deposits  
trust fund accounts  
interest rate computations  
auto installment loans  
mortgage handling  
statistical computations  
and lots more

PERSONAL COMPUTER USE

checking account balance  
savings, stocks and bonds, etc.  
household budgets  
dates to remember file  
Christmas card list  
menus and shopping list  
security system and crime preventor  
vital document record  
as many uses as you can think of

2 STARTING AT THE BOTTOM  
2.4 APPLICATIONS cont'd

GAMES

Button, Button, Whose got the Button  
Create a Random Maze  
3D Tic Tac Toe  
14 Civil War Battles for 2  
Star Trader  
Try to Beat the Taxman  
Baseball  
Basketball  
Black Jack  
Life  
Pro Football  
Monopoly  
Checkers  
Chess  
and hundreds more

A computer is more than a practical tool for compiling data and solving problems. A tool or machine that can teach you and help you to broaden your scope of thought is indeed helpful to personal development. Through the implementation of computer games, mental stimulation can occur. Games Encourage Imaginative and Constructive Responses. The result of games are unimportant---we take risks, tolerate uncertainty, and proceed with less-than complete understandings the ability to react creatively to new and unexpected situations are constantly changing. We develop our decision making capabilities and problem solving skills, games are fun. The computer waits patiently while you experiment with different lines of thought. It's available to play any game you want, and as many times as you'd like. A simulation is a model of a real life situation. With your computer, you can reconstruct and analyze real life situations, if you want to be creative. Your computer can do complicated bookkeeping---You can create the initial conditions, establish the limits, and then analyze the results. With your own computer, a simulated situation can be repeated as many times as you want. Many people ask, "Why play games at all?" A game involves competition as a relationship among players. On a computer we can transform a competitive 2 player game into a teamwork relationship with many more players. Instead of always playing one side, through the use of your computer, you can alternate positions throughout the game. Computer games can introduce new ideas into your built in computer. Games are open ended, multi-purposed, and can be suited to your particular whims. Games can be the tool which could re-open your mind to a vast new frontier of ideas.

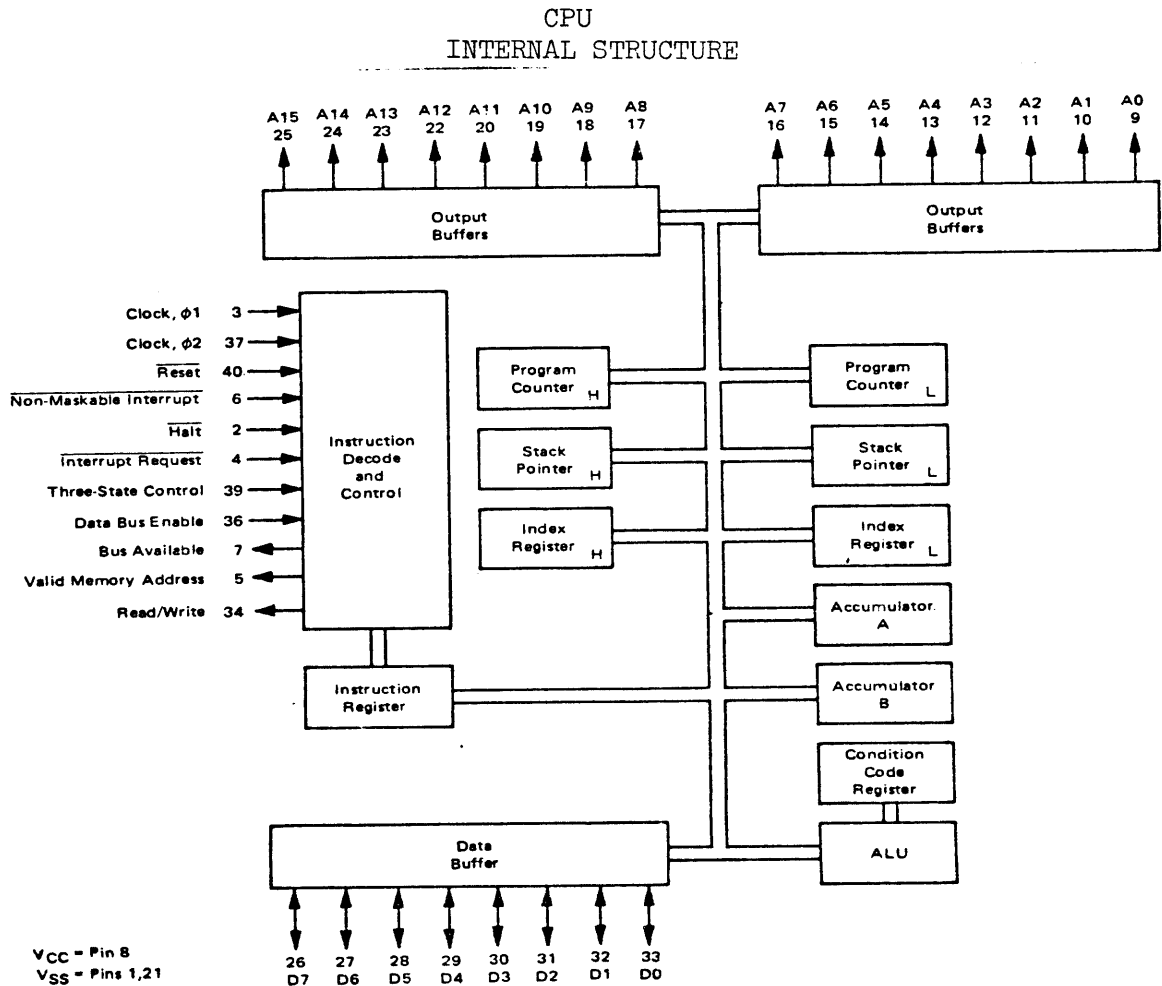
### 3 SYSTEM ORGANIZATION

In Section 1, a general description of the System was given. In this chapter, a more detailed description of the device making up the system will be given. The Motorola MC 6800 is an 8-bit micro-processor forming the central control function for the System. As in all computer systems, its main function is to:

1. Control the sequence and execute the instructions received from a program stored in memory to accomplish a given task (prepare a payroll, etc.)
2. Perform data transfers from one point in the system to another.
3. Perform logical and arithmetic operations on data during transfers as needed.
4. Monitor and respond to external influences that alter program sequences.

Figure 3.1 shows in block form the internal structure of SPHERE CPU.

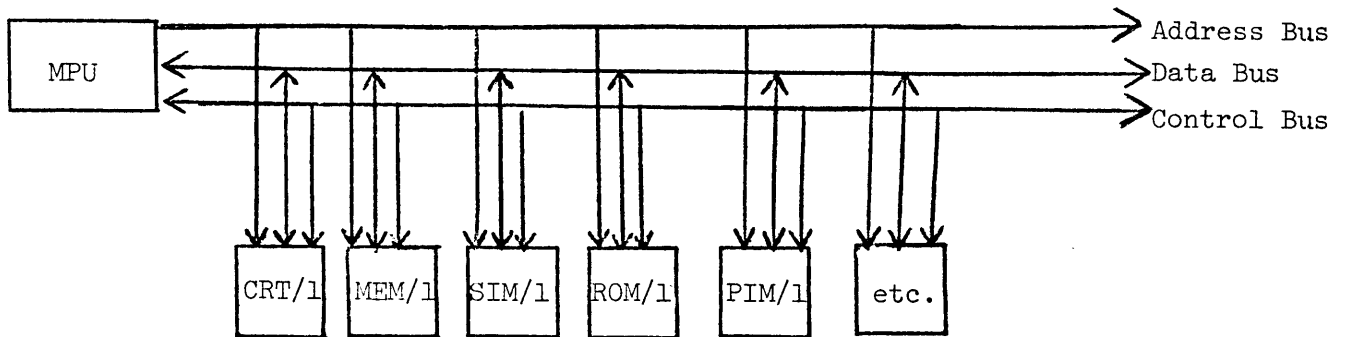
FIGURE 3.1



3 SYSTEM ORGANIZATION cont'd

Figure 3.2 shows the relationship of the MPU to the other devices on the external BUS, which make up the system. Note that all devices are paralleled on the bus; i.e., the address, data and control lines are 'common' to all devices. Each device has a unique address and responds only when its address and required control signals are presented on the bus. All address decoding is done by the devices themselves. This bus structure eliminates the need for separate I/O channels for each device and simplifies the interface requirements. In addition, because each device contains its own status and data registers, they look just like memory locations to the MPU. Each device is therefore addressed, like memory, no special I/O instructions are needed. In fact, any instruction that can access memory or operate on data in memory can also manipulate the I/O device registers. This provides much greater programming flexibility than would be possible with a system requiring special I/O instructions. This structure also simplifies and standardizes the interface requirements for peripherals.

FIGURE 3.2  
SPHERE BUS STRUCTURE

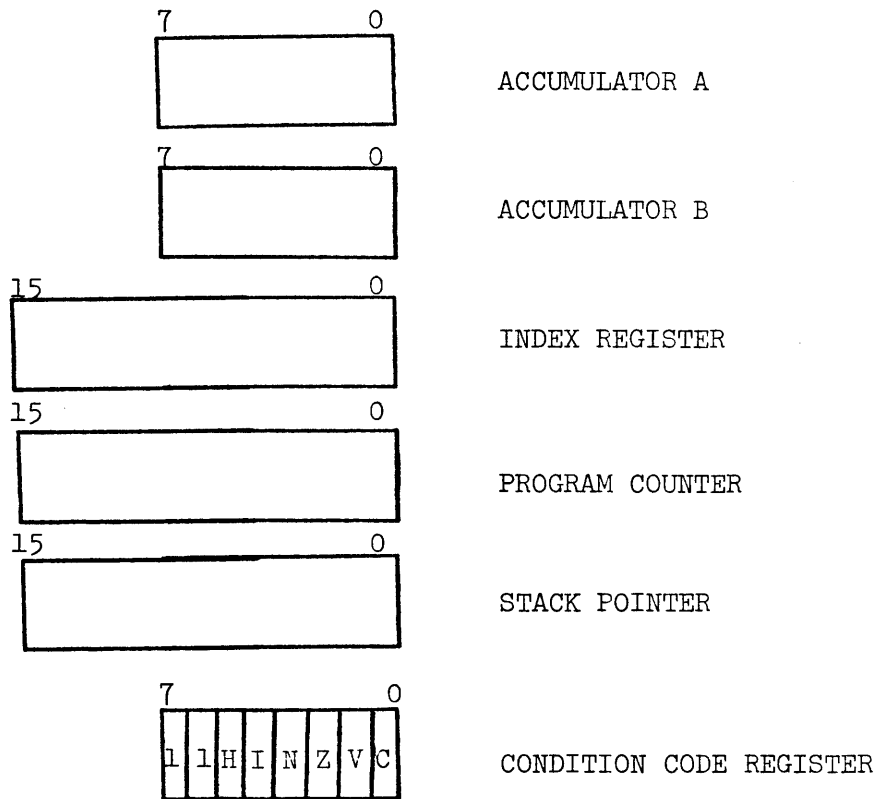


3 SYSTEM ORGANIZATION cont'd

Figure 3.3 shows a programming model of the MPU. This shows the registers that can be directly accessed by the programmer. The bit size of each register is also shown. The following is a general description of each module, which combined make up the basic SPHERE system.

FIGURE 3.3

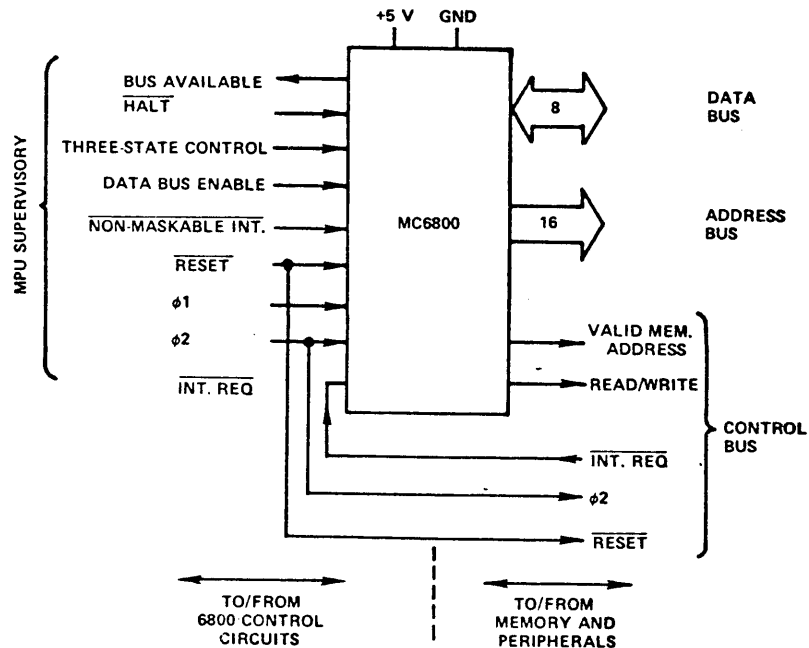
PROGRAMMING MODEL OF MC6800



3 SYSTEM ORGANIZATION cont'd

Several of the components of the processor are not directly accessible to the user and are explained here for information purposes only. The processor contains a control unit which provides the necessary timing to control the instruction decoding and execution sequences. The arithmetic and logic (ALU) performs the actual arithmetic operations, such as addition, subtraction, etc., and all boolean type operations, such as AND, OR, etc. Each accumulator receives and transmits data to and from the bus and temporarily stores results from the ALU. The input and output buffers provide the access to the address and bi-directional data lines for the MPU. The instruction register holds the instruction read from memory while it is decoded by the control unit. Also shown are the main MPU and peripheral control lines. The remainder of the registers are accessible to the programmer. The working environment for programming consists of 72 instructions, seven addressing modes, six registers and memory (including the stack). Figure 3.4 gives a summary of the six registers that are program accessible.

FIGURE 3.4



### 3 SYSTEM ORGANIZATION cont'd

A stack consists of a number of contiguous memory locations for temporary storage. The information stored on the stack may consist of status during interrupts, subroutine linkage return addresses, and data. The stack pointer is a 16 bit register containing the address of the next position in which to store information. As information is stored, the stack pointer is decremented to the next free position. As data is recalled from the stack, the stack pointer is incremented to the previous position, and then the data is retrieved. It is the programmer's responsibility to initialize the stack pointer register.

#### 3.1 THE ONE CARD COMPUTER

The logical approach to the solution of any problem is to determine the minimum requirement for a satisfactory result. In the case of a small computer, an absolute minimum would include a reasonable amount of memory, a capable CPU, Input/Output capability, a real-time clock, read only memory program which if used in conjunction with a terminal can replace the computer's switch panel and display lights, and finally it ought to have a convenient Bus structure to easily attach other modules. The SPHERE ONE CARD COMPUTER includes all of the above features plus a few that also deserve attention. The one card computer is the heart of the 300 series computers.

##### 3.1.1 THE CPU

The MOTOROLA 6800 microprocessor is the most advanced microprocessor available today. It reduces the necessity for support components and includes features not found on computers of many times the size. The IBM 370, for example, will not store all of its registers automatically upon receipt of an interrupt as the 6800 system does. The 6800 resembles the architecture of the Digital PDP-11 in many ways including instructions that "PUSH" data onto a STACK. As that storage is no longer required the data may be "POPped" off of the stack. The 6800 doesn't have as many registers as other CPU's, however, the 6800 has several addressing modes which in most cases completely outweigh its lack of registers. These modes are particularly advantageous when tables are processed.

##### 3.1.2 MEMORY

This system uses the 2107A type 4K by 1 dynamic random access memory. This memory was used because it is the least expensive memory available and would lower the cost of the system. All refresh circuitry for the system is included on the CPU board.



### 3 SYSTEM ORGANIZATION

#### 3.1 THE ONE CARD COMPUTER

##### 3.1.3 I/O

If this board is used as a stand alone CPU it must communicate to the outside world. Therefore, the system is supplied with 16 programmable I/O lines. Four additional lines which may be used as programmed interrupts are also supplied on the board. The board also has the ability to drive a 20 ma current loop, RS232 serial device.

##### 3.1.4 REAL-TIME CLOCK

A stand alone process control system and many other systems require the capability of monitoring the progress of an activity. The SPHERE system has a real-time clock which will interrupt the system at a set interval. This interval is a function of the refresh clock which is set at 2 ms. The interrupt may occur at 1x, 2x, 4x, 8x or 16x the refresh rate. The interval may also be set externally. The rate is determined by a wire strap.

##### 3.1.5 EPROM

The Erasable Programmable Read Only Memory used by the system is the 1702 A. Programmers for this EPROM are commonly available so that users may find programming the system for a stand alone application a reasonable task. When delivered with a SPHERE system the EPROM contains a Program Development Systems (PDS) which is described in Section 9 compatible to the hardware structure obtained with the order.

##### 3.1.6 BUS STRUCTURE

The BUS is driven by tri-state TTL buffers which are capable of driving 35 standard TTL devices. The BUS is connected to this board via three 14 pin dual-in-line connectors which will transmit and receive information over three 14 conductor flat ribbon cables. Eight data, 16 address, BUS and control lines are transmitted bidirectionally to and from the CPU, memory, and peripherals. I/O devices, buffer, and status registers are addressed as memory locations at the top (HIGH ORDER LOCATIONS) of memory in much the same as the Digital PDP-11. This means that about 35,000 devices could be attached to the system (theoretically). It also means that any machine instructions may operate on device buffer and status registers as they would to memory. This limits the maximum memory on SPHERE systems to 56K instead of the theoretical 64K because the high order 8K is reserved for device status and buffer registers.

### 3 SYSTEM ORGANIZATION

#### 3.1 THE ONE CARD COMPUTER

##### 3.1.7 POWER-ON RESET

When power is applied to this board, circuitry forces a reset to the processor until the system power has had time to stabilize. The system will immediately thereafter jump to a specific location in the read only memory (EPROM) to begin meaningful processing.

##### 3.2 SYSTEM 310

This computer system is capable of satisfying the needs of the user who wishes to program, develop, and debug programs for light process control, experimenting, and some educational purposes. As with all SPHERE "SYSTEMS", the computer was designed to perform a useful function. It was not intended to be a useless computer with a lot of money spent on front console. All SPHERE systems are shipped with software and a commitment that software developed in the future by SPHERE or one of its users will be available at minimal cost. The PDS SYSTEM is included in the read only memory of this system. It and other software which is available is described in Section 9. Expandability has been considered from the onset. Some of these considerations include additional memory to 56K inter-computer communications, a full line of peripherals, home and industry utility, and lowering cost while increasing performance in the future. Below are listed the modules contained in this system:

##### 3.2.1 CPU2

This module contains all of the features listed under "THE ONE CARD COMPUTER".

##### 3.2.2 KBD2

This module includes a standard typewriter style alpha-numeric keyboard layout.

##### 3.2.3 CRT 1

This module contains the necessary electronics to display 512 characters on a video monitor. The 64 character ASCII character set is displayed in a matrix of 32 characters by 16 lines. Each character is displayed in a matrix of dots, 5 dots wide and 7 dots high. To display a character a computer program simply moves the desired character into a memory position which is also the display refresh buffer. The refresh buffer is located in the high-order 8K of memory. It

### 3 SYSTEM ORGANIZATION

#### 3.2 SYSTEM 310

##### 3.2.3 CRT 1 cont'd

consists of 512 bytes of static RAM that is organized to be accessed by the CPU and CRT simultaneously without degrading the access time to the CPU. Output from this module to the video monitor appears as a composite video signal. Etches for RF modulator (adjustable from channels 1-3) have been left on the PC board, and schematics have been provided; however, components have not been supplied because this type of circuit requires FCC testing and approval. Instructions for TV modifications are generally available.

##### 3.2.4 PWR/2

The power supply has been designed expressly for the SPHERE system. It produces 5 volts at 3.5 amps, 12 volts at .7 amps, -5 volts at .2 amps, and -12 volts at .5 amps.

##### 3.2.5 BCB 1

Each of the system modules is connected via a system bus. The bus consists of three flat ribbon cables containing 14 conductors each. Each cable is connected to each board via a 14 pin dual-in-line (DIP) connector. Each board has three standard 14 pin IC sockets where each of the three bus cables attach.

##### 3.2.6 PCB 1

Power is bussed to each of the boards of the system via a separate 14 conductor ribbon cable. This cable is attached to each board via a 14 pin dual-in-line connector.

##### 3.2.7 OPR 1

The operator/reference manual set is designed to introduce the SPHERE system to the new computer user. It describes in detail how each instruction works. It also describes in detail interrupts, stack operations, Input/Output, peripheral device characteristics, memory organization, projected device reserved locations and limited characteristics, and execution timing. Programming examples are included to illustrate various hardware features and a section is included to introduce programming concepts to the first time computer user. Appendices are included to aid program development. Although this manual set is comprehensive, some users may require further information so references are amply provided. The manual set is loose bound to receive updates and includes sections where Global Newsletters, kit assembly instructions, manuals, and maintenance manuals may be kept. Kit assembly

### 3 SYSTEM ORGANIZATION

#### 3.2.7 OPR 1 cont'd

instructions manuals are a part of the package; however, each module in kit form contains an associated kit assembly manual which may be kept in this binder. SPHERE encourages user groups to promote interchange of ideas, useful circuits, comments, gripes, and software (from games to statistical packages). A Global Newsletter subscription is included with any "SYSTEM" purchase or with the purchase of the OPR1 manual set.

#### 3.3 SYSTEM 320

This system was specifically designed to solve the needs of two different users.

1. The user who wishes to communicate to other devices over serial lines such as a telephone.
2. The user who wishes to utilize this device as a stand alone computer, and use the communications facility to save and restore programs and data using a standard audio cassette.

The communications facility is implemented as a single module (one board) which contains a standard asynchronous communications interface and a modem. Serial communications to other devices such as a teletype or other computer may take place without the use of a modem. This system includes all of the features found in System 310 plus the following:

##### 3.3.1 SIM 1

This module provides the facility to communicate data in several serial forms. The module has two independent serial I/O ports. One can be connected only to a Kansas City standard cassette interface. The other can either be connected to a second cassette interface or any one of the following: EIA RS-232-C interface, 20 mA current loop, direct TTL interface, or industry standard low-speed modem enabling communications over standard telephone lines. The ACIA's can accept data in an 8 bit parallel format from the CPU and transmit it serially with a start bit and 1-2 stop bits. Seven or eight data bits may be transmitted with optional even or odd parity. At the same time data in same format may be received serially, presented to the CPU in 8 bit parallel format. The data will be checked for proper parity (if desired) and false start bits will be rejected. Communications may occur at several standard strap-selectable rates; 110, 150, 300, 600, 1200, 2400, 4800, and 9600 Baud. X-on and X-off functions are provided by an on board relay. This module optionally contains a complete ORIGINATE/ANSWER modem. The modem will operate at a maximum speed of 600 Baud. The SH, RING, +V, DH, DA, DR, and GND signals are provided for the CBT type of DAA (Direct Access Arrangement). A speaker and a microphone are all that are required to complete the acoustic coupler. No cabling is provided with this unit.

### 3 SYSTEM ORGANIZATION

#### 3.4 SYSTEM 330

This system was designed for the user who wishes to have total stand alone program development. The features found in the earlier mentioned systems along with the additional 16K of memory included with System 330 supplies the user enough memory for major program design.

##### 3.4.1 MEM 1

This module contains 16K of memory which provides ample space for the Basic interpreter and user programs. The memory board is designed with four rows of memory chips. Each row has eight chips with 4096, 8-bit bytes per row. Total number of bytes per board is 16,384. Memory addresses are selectable by a wire jumper on the PC Board. With this you can select the address area you want for memory storage (within 4K boundaries) without having to rewrite your program.

##### 3.4.2 BASIC SOFTWARE

The Basic Software package included is a fully extended language which includes matrix operators, string operators and file functions, plus the capability of calling the assembler subroutines.

#### 3.5 SYSTEM 340

Total computer capabilities are included in this system. System 340 has been designed for the user who needs large amounts of memory and peripheral capabilities. Included is a 65 line per min., 80-column printer; also included are two IBM compatible floppy disk modules complete with SDOS disk operating system and Basic. The disk operating system handles file maintenance, and provides an editor, assembler, and debugging facility with file handling extensions for thorough disk utilization. This system includes everything previously listed except the SIM board plus the following:

##### 3.5.1 LPT 1

The SPHERE Line Printer produces 80 columns of 5x7 dot matrix characters at 110 characters per second, or 65 lines per minute. The impact head prints bidirectionally on 8 1/2 inch continuous paper using a conventional teletype ribbon. This line printer has been designed with high reliability and extremely low cost required by small scale data handling systems. This system features the ability to print double wide characters for heading and other applications. The printer is available with either tractor feed or pressure rollers. Up to four highly legible copies may be produced.

### 3 SYSTEM ORGANIZATION

#### 3.5 SYSTEM 340 cont'd

##### 3.5.3 DSK 1

The disk interfaces to the SPHERE system via the peripheral interface module and disk cable assembly and is fully supported by the SPHERE Disk Operating System (SDOS) package. The flexible disk used is media and format compatible to the IBM 3540 and 3740 with a maximum data storage capacity of 256,256 bytes per diskette. A single controller handles up to four drive units which may be individually write-protected. Hardware track seek and seek verification as well as CRC generation and verification insure data validity.

##### 3.6 PIM 1

Both the Disk and the Line Printer are interfaced through this module which provides up to 64 digital I/O lines and 16 control lines (4 PIA's). The module also includes some circuitry dedicated to the Line Printer interface. The LPT 1 interface requires one PIA and Disk interface requires 1 1/2 PIA's. Strapping is provided to address up to 8 PIM boards on a system.

## 4 ADDRESSING MODES

In computers, both the instruction and the data it manipulates must be specified. The instruction consists of an operator portion, which specifies the instruction code, and a data part called the operand. Sometimes, the operand portion may not be the actual data but a number or address used in finding the data. Operands are associated with each operator except when the instruction operates on the state of the machine, such as HALT or WAIT, or when there is only one operand and the operator specifies implied or accumulator addressing. The addressing modes available are a function of both the type of instruction and the mode bits in that instruction.

### 4.1 INHERENT ADDRESSING

In the inherent addressing mode, the operand (stack pointer, accumulator, index register, condition codes, etc.) is implicit in the instruction, which is one byte long. An instruction such as DEX - Decrement Index Register, would be of this type.

### 4.2 DIRECT ADDRESSING

In direct addressing instructions the locations of the operand is specified by the second byte. The address specified is one of the first 256 locations of main memory, i.e. bytes 0 through 255. The length of the operand is either one or two bytes, depending on the operator (load accumulator is a one byte operand while load index is a two bytes long operand). This mode takes two bytes.

### 4.3 EXTENDED ADDRESSING

Extended addressing is a 3 byte instruction where the second and third bytes are used to form a 16 bit address. This allows any location in main memory to be accessed, compared with only the first 256 addressable locations accessible with the Direct Addressing mode. The main difference of Direct Addressing and Extended Addressing is that Direct Addressing can only reference part of memory but takes one less byte to do it, thus reducing program size.

### 4.4 IMMEDIATE ADDRESSING

The immediate addressing mode contains the actual operand in the bytes following the operator byte. This is useful where the data is a constant value as opposed to a variable with an address as used in the direct addressing mode. These instructions are two bytes long, one byte for the operator code and one byte for data for instructions using the accumulators. For the instructions which use the 16 bit stack and index registers, the operand data is two bytes long producing a three byte instruction.

#### 4 ADDRESSING MODES

FIGURE 4.1

ADDRESS MODE	BYTE 1	BYTE 2	BYTE 3	REMARKS
Inherent SWI	Operator 3F			Seven bytes of the computer's status are pushed onto the stack and a branch to the location pointed to by memory locations FFFA and FFFB is executed.
Direct	Operator	Address of Operand		
LDAA	96	10		Load the A accumulator with the contents of memory location 10. Load the index register with the contents of memory locations 73 & 74.
LDX	DE	73		
Extended	Operator	Address of Operand		
LDAA	B6	OF	ED	Load the A accumulator with the contents of memory location OFED. Load the index register with the contents of memory 2BAD & 2BAE.
LDX	FE	2B	AD	
Immediate	Operator	Operand		
LDAA	86	20		Load the A accumulator with 20. Load the index register with E1FF.
LDX	CE	E1	FF	
Index	Operator	Displacement of Operand		
LDAA	A6	30		(Assume index register=1000) Load the A accumulator with the contents of memory location 1030 (1000 + 30). Load the index register with the contents of memory location 1000 (1000+0).
LDX	EE	00		
Relative	Operator	Operand		
BRA	20	05		(Assume instruction begins at 100) Branch always; execute the next instruction from location 107. Branch only if the condition code bit Z=0 to location FA; if Z=1, execute the next instruction from location 102.
BNE	26	F8		



## 4 ADDRESSING MODES

### 4.5 INDEX ADDRESSING

Index addressing uses the index register to help form the address of the data in memory. The instruction format is the same as in direct addressing made but the second byte is added to the contents of the index register to form a 16 bit address in main memory. This allows addresses to be formed under program control. The address byte is in effect an offset from the address specified by the index register. The index register is usually used to form pointers into data tables.

### 4.6 RELATIVE ADDRESSING

In relative address mode the 8 bit number contained in the second byte of the instruction is added to the contents of the program counter (which is pointing to the next instruction). The 8 bit number is taken as a signed number, thus giving an offset of - 128 to +127 from the current instruction. The new address is relative to the current address. Relative addressing is used for branches, where the new address is used as the address of the next instruction.

## 5 STACK AND STACK POINTER

The stack consists of any number of consecutive locations in main memory. The stack provides for temporary storage and retrieval of successive bytes of information, which may include any of the following items:

- \*Current values of the CPU registers
- \*Subroutine return addresses
- \*Data

The stack can be used for the following purposes:

- \*Temporary storage of data (under control of the program)
- \*Interrupt control
- \*Subroutine linkage
- \*Re-entrant code
- \*Recursive subroutine data

### 5.1 STACK CHARACTERISTICS

The CPU includes a 16-bit stack pointer. The stack pointer points to the top of the stack-1, thus enabling the CPU to find the current location of the top of the stack and where the next byte is to be stored on the stack. Stack memory is usually referenced sequentially with respect to the top of the stack on a last-in-first-out (LIFO) basis. Because stack memory is dynamically allocated while a program is running, it can be used to store the same temporary variable or return address any number of times, thus allowing a routine to recursively call itself several times.

When a byte of information is pushed onto the stack, it is stored at the address which is contained in the stack pointer and the stack pointer is then immediately decremented. Conversely, when pulling a byte from the stack, the stack pointer is incremented and the byte is then obtained from the address contained in the revised stack pointer.

### 5.2 START UP

When a program starts up, it must reserve a block of main memory for use by the stack. Care must be taken that when data is pushed or put onto the stack, the stack size does not exceed the size of the memory block reserved for it, called stack overflow. Since the stack grows toward the bottom of memory, it is advisable to start the stack at the top of useable memory. Care must be taken not to take more data off the stack than was put on, or to leave data on the stack that was pushed there after a subroutine jump.

## 5 STACK AND STACK POINTERS

### 5.3 MULTIPLE STACKS

Normally, the stack will consist of a single block of successive memory locations. However, some instructions such as Transfer Index to Stack (TXS) will change the address contained in the stack pointer without storing or retrieving information into or from the stack. The use of these instructions can result in the stack being other than one continuous block of memory locations. In such a case it may alternatively be considered that there exist two or more stacks, each of which consists of a block of successive locations in the memory. This would be useful when multiple tasks are performed at the same time.

### 5.4 SAVING THE MPU REGISTER VALUES

It is sometimes desirable to temporarily save the register values on the stack so they can be used for other calculations. The values of the CPU registers are automatically saved on the stack when honoring an interrupt. The status is stored in the stack in accordance with the scheme shown in Figure 5.1. Before storing the status, the stack pointer contains the address of a memory location represented in Figure 5.1 by "m". The stack extends from location m+1 to higher locations. The status is then stored in seven bytes of memory, beginning with the byte at location "m", and ending with the byte at location "m-6". The stack pointer is decremented after each byte of information is pushed onto the stack. The information saved on the stack consists of the numerical content of all of the registers contained in the CPU except the stack pointer. The value stored for the program counter (PCH and PCL) is in accordance with the following rules:

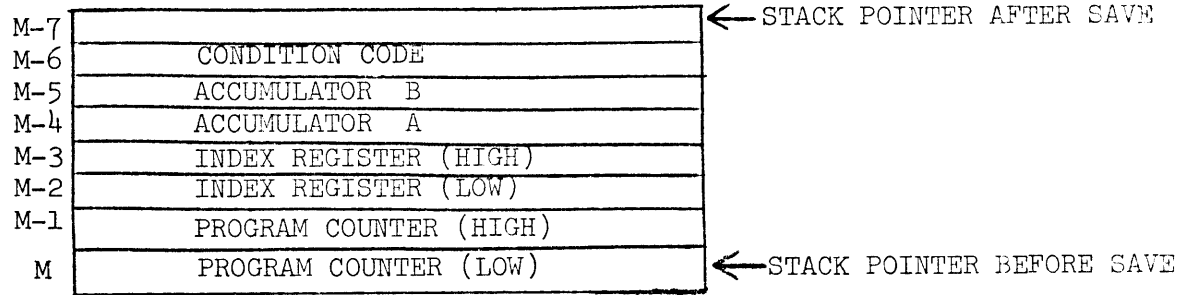
1. If the values are stored in response to a non-maskable interrupt, or to an interrupt from a peripheral device, the value saved for the program counter is the address of the instruction which would be the next executed, if the interrupt had not occurred.
2. If during execution of a SWI or WAI instruction, the value saved for the program counter is the address of that SWI or WAI instruction, plus one.

The values stored for the other registers (CC, ACCB, ACCA, IXH and IXL) are in accordance with the following rules:

1. If in response to a non-maskable interrupt, or an interrupt from a peripheral device, the values saved are those which resulted from the last instruction executed before the interrupt was serviced.
2. If during execution of a SWI or WAI instruction, the values saved are those which resulted from the last instruction executed before the SWI or WAI instruction.
3. The condition codes, H,I,N,Z,V, and C, in bit positions 5 thru 0 of the processor condition code register, are stored respectively in bit positions 5 thru 0 of the applicable memory location in the stack. Bit positions 7 and 6 of that memory location are set (i.e., go to the 1 state).

5 STACK AND STACK POINTERS  
 5.4 SAVING THE MPU REGISTER VALUES cont'd

FIGURE 5.1



5.5 BLOCKS OF DATA ON THE STACK

By using the Transfer Stack to Index (TSX) instruction to set the index register to point to the top of stack, programs can make references into the stack instead of just referencing the top of stack. This is useful where a block of data has been put on the stack for temporary use by a routine or for use in software interrupts. By allowing a routine to store its temporary variables on the stack, it can be made re-entrant, i.e. it can be working on several independent sets of data at the same time without one set affecting another.

## 6 INSTRUCTION SET

This section describes the SPHERE Instruction Set in the following order:

ACCUMULATOR & MEMORY INSTRUCTIONS  
INDEX REGISTER AND STACK POINTER MANIPULATION INSTRUCTIONS  
BRANCH INSTRUCTIONS  
CONDITION CODE MANIPULATION INSTRUCTIONS

Instruction related to Interrupt processing are covered in Section 7.

The condition codes are a set of 6 bits in the condition code register which indicate the status of the CPU and are used by the branch instructions. Whenever an instruction is executed the condition code bits are either set, cleared or left unchanged, depending on the results of the operation.

### The condition codes are as follows:

H half-carry from bit 3  
I interrupt mask bit (set=enhibit, cleared=enabled)  
N negative (sign bit)  
Z zero (byte)  
V overflow, 2's complement  
C carry from bit 7

### The condition code bits are set as follows:

R reset always  
S set always  
T test and set if true, cleared otherwise  
blank unchanged

### Condition code register notes

(set if test true, cleared otherwise)  
1 (bit V) test: result=10000000  
2 (bit C) test: result=00000000  
3 (bit C) test: Decimal value of most significant ECD character greater than 9? (not cleared if previously set)  
4 (bit V) test: operand=to 10000000 prior to execution?  
5 (bit V) test: operand=to 01111111 prior to execution?  
6 (bit V) test: set equal to result of  $N \oplus C$  after shifting.  
7 (bit N) test: sign bit of most significant byte of result=1?  
8 (bit V) test: 2's comp. overflow from subtraction of least significant byte  
9 (bit N) test: result less than zero? (bit 15=1)  
10 (all) Load CCR from stack  
11 (bit I) Set when interrupt occurs. If previously set, a Non Maskable interrupt is required to exit the wait state.  
12 (all) Set according to the contents of Accumulator A

6 INSTRUCTION SET cont'd

LEGEND

+	Arithmetic Plus
-	Arithmetic Minus
•	Boolean AND
$M_{SP}$	Contents of memory location pointed to by stack pointer
$\underline{+}$	Boolean Inclusive OR
$\oplus$	Boolean Exclusive OR
$\bar{M}$	Complement of M
$\rightarrow$	Transfer into
$\emptyset$	Bit zero
$\emptyset\emptyset$	Byte zero
CCR	Condition Code Register

6 INSTRUCTION SET  
 6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

6.1.1 ADD

ADDA

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
IMMEDIATE	8B	2	2
DIRECT	9B	2	3
INDEXED	AB	2	5
EXTENDED	BB	3	4

BOOLEAN/ARITHMETIC OPERATION

$A + M \rightarrow A$

DESCRIPTION

The contents of the A accumulator are added to the contents of a byte of memory, and the results are placed back into the accumulator.

T		T	T	T	T
5	4	3	2	1	0
H	I	N	Z	V	C

ADDB

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
IMMEDIATE	CB	2	2
DIRECT	DB	2	3
INDEXED	EB	2	5
EXTENDED	FB	3	4

BOOLEAN/ARITHMETIC OPERATION

$B + M \rightarrow B$

DESCRIPTION

The contents of the B accumulator are added to the contents of a byte of memory, and the results are placed back into the accumulator.

T		T	T	T	T
5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

6.1.2 ADD ACCUMULATORS

ABA

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	1B	1	2

BOOLEAN/ARITHMETIC OPERATION

$A + B \rightarrow A$

DESCRIPTION

The contents of both accumulators are added and the results are placed in accumulator A.

T		T	T	T	T
5	4	3	2	1	0
H	I	N	Z	V	C

6.1.3 ADD WITH CARRY

ADCA

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
IMMEDIATE	89	2	2
DIRECT	99	2	3
INDEXED	A9	2	5
EXTENDED	B9	3	4

BOOLEAN/ARITHMETIC OPERATION

$A + M + C \rightarrow A$

DESCRIPTION

The contents of accumulator A is added to a byte of memory; the carry bit of the condition code register is interrogated and if set, the results is incremented by one. The results are then placed back into accumulator A.

T		T	T	T	T
5	4	3	2	1	0
H	I	N	Z	V	C



6 INSTRUCTION SET

6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

6.1.3 ADD WITH CARRY cont'd

ADCB

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
IMMEDIATE	C9	2	2
DIRECT	D9	2	3
INDEXED	E9	2	5
EXTENDED	F9	3	4

BOOLEAN/ARITHMETIC OPERATION

$$B + M + C \rightarrow B$$

DESCRIPTION

T		T	T	T	T
5	4	3	2	1	0
H	I	N	Z	V	C

The contents of accumulator B is added to a byte of memory; the carry bit of the condition code register is interrogated and if set the result is incremented by one. The results are then placed back into accumulator B.

6.1.4 AND

ANDA

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
IMMEDIATE	84	2	2
DIRECT	94	2	3
INDEXED	A4	2	5
EXTENDED	B4	3	4

BOOLEAN/ARITHMETIC OPERATION

$$A \cdot M \rightarrow A$$

DESCRIPTION

		T	T	R	
5	4	3	2	1	0
H	I	N	Z	V	C

Accumulator A and a byte of memory are logically ANDed together and the results stored in accumulator A.

6 INSTRUCTION SET

6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

6.1.4 AND cont'd

ANDB

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
IMMEDIATE	C4	2	2
DIRECT	D4	2	3
INDEXED	E4	2	5
EXTENDED	F4	3	4

BOOLEAN/ARITHMETIC OPERATION

$B \cdot M \rightarrow B$

DESCRIPTION

Accumulator B and a byte of memory are logically ANDed together and the results stored in the accumulator.

		T	T	R	
5	4	3	2	1	0
H	I	N	Z	V	C

6.1.5 BIT TEST

BITA

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
IMMEDIATE	85	2	2
DIRECT	95	2	3
INDEXED	A5	2	5
EXTENDED	B5	3	4

BOOLEAN/ARITHMETIC OPERATION

$A \cdot M$

DESCRIPTION

Accumulator A and a byte of memory are logically ANDed.

		T	T	R	
5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

6.1.5 BIT TEST cont'd

BITB

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
IMMEDIATE	C5	2	2
DIRECT	D5	2	3
INDEXED	E5	2	5
EXTENDED	F5	3	4

BOOLEAN/ARITHMETIC OPERATION

B • M

DESCRIPTION

Accumulator B and a byte of memory are logically ANDed.

		T	T	R	
5	4	3	2	1	0
H	I	N	Z	V	C

6.1.6 CLEAR

CLR

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INDEXED	6F	2	7
EXTENDED	7F	3	6

BOOLEAN/ARITHMETIC OPERATION

00 → M

DESCRIPTION

The addressed byte of memory is set to zero.

		R	S	R	R
5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET  
 6.1 ACCUMULATOR & MEMORY INSTRUCTIONS  
 6.1.6 CLEAR cont'd

CLRA

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	4F	1	2

BOOLEAN/ARITHMETIC OPERATION

00  $\Rightarrow$  A

DESCRIPTION

The A accumulator is set to zero.

		R	S	R	R
5	4	3	2	1	0
H	I	N	Z	V	C

CLRB

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	5F	1	2

BOOLEAN/ARITHMETIC OPERATION

00  $\Rightarrow$  B

DESCRIPTION

The B accumulator is set to zero.

		R	S	R	R
5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.1 ACCUMULATOR & MEMORY INSTRUCTIONS cont'd

6.1.7 COMPARE

CMPA

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
IMMEDIATE	81	2	2
DIRECT	91	2	3
INDEXED	A1	2	5
EXTENDED	B1	3	4

BOOLEAN/ARITHMETIC OPERATION

A - M

DESCRIPTION

A byte of memory is subtracted from accumulator A.

		T	T	T	T
5	4	3	2	1	0
H	I	N	Z	V	C

CMPB

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
IMMEDIATE	C1	2	2
DIRECT	D1	2	3
INDEXED	E1	2	5
EXTENDED	F1	3	4

BOOLEAN/ARITHMETIC OPERATION

B - M

DESCRIPTION

A byte of memory is subtracted from accumulator B.

		T	T	T	T
5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

6.1.8 COMPARE ACCUMULATORS

CBA

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	11	1	2

BOOLEAN/ARITHMETIC OPERATION

A - B

DESCRIPTION

Accumulator B is subtracted from accumulator A.

		T	T	T	T
5	4	3	2	1	0
H	I	N	Z	V	C

6.1.9 COMPLEMENT, 1's

COM

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INDEXED	63	2	7
EXTENDED	73	3	6

BOOLEAN/ARITHMETIC OPERATION

$\bar{M} \rightarrow M$

DESCRIPTION

Each bit of a byte is reversed, that is, the ones are set to zeros, the zeros are set to ones.

		T	T	R	S
5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

6.1.9 COMPLEMENT, 1's cont'd

COMA

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	43	1	2

BOOLEAN/ARITHMETIC OPERATION

$$\overline{A} \rightarrow A$$

DESCRIPTION

Each bit of a byte is reversed, that is, the ones are set to zeros the zeros are set to ones.

		T	T	R	S
5	4	3	2	1	0
H	I	N	Z	V	C

COMB

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	53	1	2

BOOLEAN/ARITHMETIC OPERATION

$$\overline{B} \rightarrow B$$

DESCRIPTION

Each bit of a byte is reversed, that is, the ones are set to zeros the zeros are set to ones.

		T	T	R	S
5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

6.1.10 COMPLEMENT, 2's (Negate)

NEG

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INDEXED	60	2	7
EXTENDED	70	3	6

BOOLEAN/ARITHMETIC OPERATION

00 -  $M \rightarrow M$

DESCRIPTION

Memory contents are subtracted from 0 and the results placed back in memory.

		T	T	1	2
5	4	3	2	1	0
H	I	N	Z	V	C

NEGA

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	40	1	2

BOOLEAN/ARITHMETIC OPERATION

00 -  $A \rightarrow A$

DESCRIPTION

Accumulator A's contents are subtracted from 0 and the results placed back in the accumulator.

		T	T	1	2
5	4	3	2	1	0
H	I	N	Z	V	C



6 INSTRUCTION SET

6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

6.1.10 COMPLEMENT, 2's (Negate) cont'd

NEGB

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	50	1	2

BOOLEAN/ARITHMETIC OPERATION

00-B>B

DESCRIPTION

Accumulator B's contents are subtracted from 0 and the results placed back in the accumulator.

		T	T	1	2
5	4	3	2	1	0
H	I	N	Z	V	C

6.1.11 DECIMAL ADJUST, A

DAA

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	19	1	2

BOOLEAN/ARITHMETIC OPERATION

Converts Binary Add. of BCD Characters into BCD Format

DESCRIPTION

Used after ABA, ADC, and ADD in BCD arithmetic operation; each 8-bit byte regarded as containing two 4-bit BCD numbers. DAA adds 0110 to lower half-byte if least significant number > 1001 or if preceding instruction caused a Half-carry. Adds 0110 to upper half-byte if most significant number > 1001 or if preceding instruction caused a Carry. Also adds 0110 to upper half-byte if least significant number > 1001 and most significant number = 9.

		T	T	T	3
5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

6.1.12 DECREMENT

DEC

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INDEX	6A	2	7
EXTENDED	7A	3	6

BOOLEAN/ARITHMETIC OPERATION

$M-1 \rightarrow M$

DESCRIPTION

A one is subtracted from the contents of a memory location.

		T	T	4	
5	4	3	2	1	0
H	I	N	Z	V	C

DECA

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	4A	1	2

BOOLEAN/ARITHMETIC OPERATION

$A - 1 \rightarrow A$

DESCRIPTION

A one is subtracted from the contents of Accumulator A.

		T	T	4	
5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

6.1.12 DECREMENT cont'd

DECB

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	5A	1	2

BOOLEAN/ARITHMETIC OPERATION

$B - 1 \rightarrow B$

DESCRIPTION

A one is subtracted from the contents of a memory location.

		T	T	4	
5	4	3	2	1	0
H	I	N	Z	V	C

6.1.13 EXCLUSIVE OR

ECRA

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
IMMEDIATE	88	2	2
DIRECT	98	2	3
INDEXED	A8	2	5
EXTENDED	B8	3	4

BOOLEAN/ARITHMETIC OPERATION

$A \oplus M \rightarrow A$

DESCRIPTION

The contents of accumulator A is exclusive ORed with the contents of a memory location. The results are returned to the indicated accumulator.

		T	T	R	
5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

6.1.13 EXCLUSIVE OR cont'd

EORB

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
IMMEDIATE	C8	2	2
DIRECT	D8	2	3
INDEXED	E8	2	5
EXTENDED	F8	3	4

BOOLEAN/ARITHMETIC OPERATION

$B \oplus M \rightarrow B$

DESCRIPTION

The contents of accumulator B is exclusive ORed with the contents of a memory location. The results are returned to the indicated accumulator.

		T	T	R	
5	4	3	2	1	0
H	I	N	Z	V	C

6.1.14 INCREMENT

INC

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INDEXED	6C	2	7
EXTENDED	7C	3	6

BOOLEAN/ARITHMETIC OPERATION

$M + 1 \rightarrow M$

DESCRIPTION

A one is added to the contents of a memory location.

		T	T	5	
5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

6.1.14 INCREMENT cont'd

**INCA**

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	4C	1	2

**BOOLEAN/ARITHMETIC OPERATION**

$A + 1 \rightarrow A$

**DESCRIPTION**

A one is added to the contents of accumulator A.

		T	T	5	
5	4	3	2	1	0
H	I	N	Z	V	C

**INCB**

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	5C	1	2

**BOOLEAN/ARITHMETIC OPERATION**

$B + 1 \rightarrow B$

**DESCRIPTION**

A one is added to the contents of accumulator B.

		T	T	5	
5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

6.1.15 LOAD ACCUMULATOR

**LDAA**

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
IMMEDIATE	86	2	2
DIRECT	96	2	3
INDEXED	A6	2	5
EXTENDED	B6	3	4

**BOOLEAN/ARITHMETIC OPERATION**

**M → A**

**DESCRIPTION**

The contents of a memory location are transferred to accumulator A.

		T	T	R	
5	4	3	2	1	0
H	I	N	Z	V	C

**LDAB**

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
IMMEDIATE	C6	2	2
DIRECT	D6	2	3
INDEXED	E6	2	5
EXTENDED	F6	3	4

**BOOLEAN/ARITHMETIC OPERATION**

**M → B**

**DESCRIPTION**

The contents of a memory location are transferred to accumulator B.

		T	T	R	
5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

6.1.16 OR, INCLUSIVE

ORRA

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
IMMEDIATE	8A	2	2
DIRECT	9A	2	3
INDEXED	AA	2	5
EXTENDED	BA	3	4

BOOLEAN/ARITHMETIC OPERATION

$$A \pm M \rightarrow A$$

DESCRIPTION

Accumulator A is inclusively ORed with the contents of a byte of memory and the results placed back in the accumulator.

		T	T	R	
5	4	3	2	1	0
H	I	N	Z	V	C

ORAB

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
IMMEDIATE	CA	2	2
DIRECT	DA	2	3
INDEXED	EA	2	5
EXTENDED	FA	3	4

BOOLEAN/ARITHMETIC OPERATION

$$B \pm M \rightarrow B$$

DESCRIPTION

Accumulator B is inclusively ORed with the contents of a byte of memory and the results placed back in the accumulator.

		T	T	R	
5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

6.1.17 PUSH DATA

PSHA

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	36	1	4

BOOLEAN/ARITHMETIC OPERATION

$A \rightarrow M_{SP}, SP - 1 \rightarrow SP$

DESCRIPTION

The contents of accumulator A are transferred to the memory stack position and the stack pointer is decremented.

5	4	3	2	1	0
H	I	N	Z	V	C

PSHB

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	37	1	4

BOOLEAN/ARITHMETIC OPERATION

$B \rightarrow M_{SP}, SP - 1 \rightarrow SP$

DESCRIPTION

The contents of accumulator B are transferred to the memory stack position and the stack pointer is decremented.

5	4	3	2	1	0
H	I	N	Z	V	C



6 INSTRUCTION SET

6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

6.1.18 PULL DATA

PULA

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	32	1	4

BOOLEAN/ARITHMETIC OPERATION

$SP + 1 \rightarrow SP, M_{SP} \rightarrow A$

DESCRIPTION

The stack pointer is incremented and the contents of memory pointed to by the stack pointer is transferred to accumulator A.

5	4	3	2	1	0
H	I	N	Z	V	C

PULB

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	33	1	4

BOOLEAN/ARITHMETIC OPERATION

$SP + 1 \rightarrow SP, M_{SP} \rightarrow B$

DESCRIPTION

The stack pointer is incremented and the contents of memory pointed to by the stack pointer is transferred to accumulator B.

5	4	3	2	1	0
H	I	N	Z	V	C

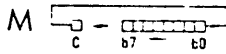
6 INSTRUCTION SET  
 6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

6.1.19 ROTATE LEFT

ROL

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INDEXED	69	2	7
EXTENDED	79	3	6

BOOLEAN/ARITHMETIC OPERATION



DESCRIPTION

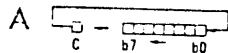
The contents of a memory location are shifted one bit to the left with the condition code bit C shifted to bit 0 and bit 7 being shifted to the condition code bit C.

		T	T	6	T
5	4	3	2	1	0
H	I	N	Z	V	C

ROLA

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	49	1	2

BOOLEAN/ARITHMETIC OPERATION



DESCRIPTION

The contents of accumulator A are shifted one bit to the left with the condition code bit C shifted to bit 0 and bit 7 being shifted to the condition code bit C.

		T	T	6	T
5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

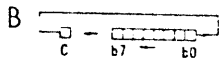
6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

6.1.19 ROTATE LEFT cont'd

ROLB

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	59	1	2

BOOLEAN/ARITHMETIC OPERATION



DESCRIPTION

The contents of accumulator B are shifted one bit to the left with the condition code bit C shifted to bit 0 and bit 7 being shifted to the condition code bit C.

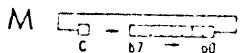
		T	T	6	T
5	4	3	2	1	0
H	I	N	Z	V	C

6.1.20 ROTATE RIGHT

ROR

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INDEXED	66	2	7
EXTENDED	76	3	6

BOOLEAN/ARITHMETIC OPERATION



DESCRIPTION

A memory location contents are shifted one bit to the right with bit zero of the memory shifted to the condition code C bit, the condition Code C bit being shifted to bit 7.

		T	T	6	T
5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

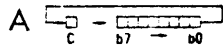
6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

6.1.20 ROTATE RIGHT cont'd

RORA

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	46	1	2

BOOLEAN/ARITHMETIC OPERATION



DESCRIPTION

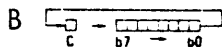
Accumulator A's contents are shifted one bit to the right with bit zero of the accumulator shifted to the condition Code C bit, the condition Code C bit being shifted to bit 7.

		T	T	6	T
5	4	3	2	1	0
H	I	N	Z	V	C

RORB

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	56	1	2

BOOLEAN/ARITHMETIC OPERATION



DESCRIPTION

Accumulator B's contents are shifted one bit to the right with bit zero of the accumulator shifted to the condition Code C bit, the condition Code C bit being shifted to bit 7.

		T	T	6	T
5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

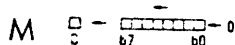
6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

6.1.21 SHIFT, LEFT, ARITHMETIC

ASL

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INDEXED	68	2	7
EXTENDED	78	3	6

BOOLEAN/ARITHMETIC OPERATION



DESCRIPTION

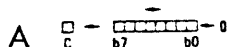
The contents of a memory shifted left one bit with bit 7 being shifted to the condition code register bit C. A zero is shifted into the memory bit 0.

		T	T	6	T
5	4	3	2	1	0
H	I	N	Z	V	C

ASLA

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	48	1	2

BOOLEAN/ARITHMETIC OPERATION



DESCRIPTION

The contents of accumulator A shifted left one bit with bit 7 being shifted to the condition code register bit C. A zero is shifted into the accumulator bit 0.

		T	T	6	T
5	4	3	2	1	0
M	I	N	Z	V	C

A zero is shifted into the

6 INSTRUCTION SET

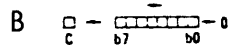
6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

6.1.21 SHIFT LEFT, ARITHMETIC cont'd

ASLB

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	58	1	2

BOOLEAN/ARITHMETIC OPERATION



DESCRIPTION

The contents of accumulator B shifted left one bit with bit 7 being shifted to the condition code register bit C. A zero is shifted into the accumulator bit 0.

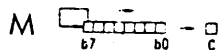
		I	I	6	T
5	4	3	2	1	0
H	I	N	Z	V	C

6.1.22 SHIFT RIGHT, ARITHMETIC

ASR

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INDEXED	67	2	7
EXTENDED	77	3	6

BOOLEAN/ARITHMETIC OPERATION



DESCRIPTION

A memory byte is shifted right one bit with bit 7 being shifted back into bit 7 and bit 0 being shifted into the condition code register bit C.

		I	I	6	T
5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

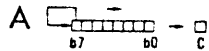
6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

6.1.22 SHIFT RIGHT, ARITHMETIC cont'd

ASRA

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	47	1	2

BOOLEAN/ARITHMETIC OPERATION



DESCRIPTION

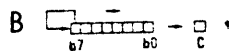
Accumulator A is shifted right one bit with bit 7 being shifted back into bit 7 and bit 0 being shifted into the condition code register bit C.

		T	T	6	T
5	4	3	2	1	0
H	I	N	Z	V	C

ASRB

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	57	1	2

BOOLEAN/ARITHMETIC OPERATION



DESCRIPTION

Accumulator B is shifted right one bit with bit 7 being shifted back into bit 7 and bit 0 being shifted into the condition code register bit C.

		T	T	6	T
5	4	3	2	1	0
H	I	N	Z	V	C

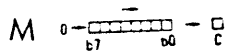
6 INSTRUCTION SET  
 6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

61.123 SHIFT RIGHT, LOGICAL

LSR

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INDEXED	64	2	7
EXTENDED	74	3	6

BOOLEAN/ARITHMETIC OPERATION



DESCRIPTION

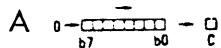
A memory byte is shifted right one bit with a zero being shifted into bit 7 and bit 0 being shifted into the condition code register.

		R	T	6	T
5	4	3	2	1	0
H	I	N	Z	V	C

LSRA

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	44	1	2

BOOLEAN/ARITHMETIC OPERATION



DESCRIPTION

Accumulator A is shifted right one bit with a zero being shifted into bit 7 and bit 0 being shifted into the condition code register.

		R	T	6	T
5	4	3	2	1	0
H	I	N	Z	V	C



6 INSTRUCTION SET

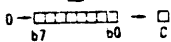
6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

6.1.23 SHIFT RIGHT, LOGICAL cont'd

LSRB

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	54	1	2

BOOLEAN/ARITHMETIC OPERATION

B 0- - 0

DESCRIPTION

Accumulator B is shifted right one bit with a zero being shifted into bit 7 and bit 0 being shifted into the condition code register.

		R	T	6	T
5	4	3	2	1	0
H	I	N	Z	V	C

6.1.24 STORE ACCUMULATOR

STAA

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
DIRECT	97	2	4
INDEXED	A7	2	6
EXTENDED	B7	3	5

BOOLEAN/ARITHMETIC OPERATION

A  $\rightarrow$  M

DESCRIPTION

Accumulator A's contents are transferred to memory.

		T	T	R	
5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

6.1.24 STORE ACCUMULATOR cont'd

STAB

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
DIRECT	D7	2	4
INDEXED	E7	2	6
EXTENDED	F7	3	5

BOOLEAN/ARITHMETIC OPERATION

B → M

DESCRIPTION

Accumulator B's contents are transferred to memory.

		T	T	R	
5	4	3	2	1	0
H	I	N	Z	V	C

6.1.25 SUBTRACT

SUBA

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
IMMEDIATE	80	2	2
DIRECT	90	2	3
INDEXED	A0	2	5
EXTENDED	B0	3	4

BOOLEAN/ARITHMETIC OPERATION

A - M → A

DESCRIPTION

The contents of a byte of memory are subtracted from accumulator A and the results placed in that accumulator.

		T	T	T	T
5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

6.1.25 SUBTRACT cont'd

**SUBB**

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
IMMEDIATE	C0	2	2
DIRECT	D0	2	3
INDEXED	E0	2	5
EXTENDED	F0	3	4

**BOOLEAN/ARITHMETIC OPERATION**

$B - M \rightarrow B$

**DESCRIPTION**

The contents of a byte of memory are subtracted from accumulator B and the results placed in that accumulator.

		T	T	T	T
5	4	3	2	1	0
H	I	N	Z	V	C

6.1.26 SUBTRACT ACCUMULATORS

**SBA**

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	10	1	2

**BOOLEAN/ARITHMETIC OPERATION**

$A - B \rightarrow A$

**DESCRIPTION**

Accumulator B is subtracted from accumulator A and the results are stored in accumulator A.

		T	T	T	T
5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

6.1.27 SUBTRACT WITH CARRY

SBCA

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
IMMEDIATE	82	2	2
DIRECT	92	2	3
INDEXED	A2	2	5
EXTENDED	B2	3	4

BOOLEAN/ARITHMETIC OPERATION

A - M - C → A

DESCRIPTION

A byte of memory is subtracted from accumulator A, the condition code bit C is interrogated and if set, the results are decremented by one. The results are placed in accumulator A.

		I	I	I	I
5	4	3	2	1	0
H	I	N	Z	V	C

SBCB

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
IMMEDIATE	C2	2	2
DIRECT	D2	2	3
INDEXED	E2	2	5
EXTENDED	F2	3	4

BOOLEAN/ARITHMETIC OPERATION

B - M - C → B

DESCRIPTION

A byte of memory is subtracted from accumulator B, the condition code carry bit is interrogated and if set, the results are decremented by one. The results are placed in accumulator B.

		I	I	I	I
5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

6.1.28 TRANSFER ACCUMULATORS

TAB

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	16	1	2

BOOLEAN/ARITHMETIC OPERATION

A → B

DESCRIPTION

The contents of accumulator A are transferred to accumulator B.

		T	T	R	
5	4	3	2	1	0
H	I	N	Z	V	C

TBA

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	17	1	2

BOOLEAN/ARITHMETIC OPERATION

B → A

DESCRIPTION

The contents of accumulator B are transferred to accumulator A.

		T	T	R	
5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

6.1.29 TEST, ZERO or MINUS

TST

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INDEXED	6D	2	7
EXTENDED	7D	3	6

BOOLEAN/ARITHMETIC OPERATION

M - 00

DESCRIPTION

Binary zeros are subtracted from the indicated memory position.

		T	T	R	R
5	4	3	2	1	0
H	I	N	Z	V	C

TSTA

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	4D	1	2

BOOLEAN/ARITHMETIC OPERATION

A - 00

DESCRIPTION

Binary zeros are subtracted from accumulator A.

		T	T	R	R
5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.1 ACCUMULATOR & MEMORY INSTRUCTIONS

6.1.29 TEST, ZERO or MINUS cont'd

6.1.29 TEST, ZERO or MINUS cont'd

TSTB

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	5D	1	2

BOOLEAN/ARITHMETIC OPERATION

B - 00

DESCRIPTION

Binary zeros are subtracted from accumulator B.

		I	T	R	R
5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.2 INDEX REGISTER AND STACK POINTER MANIPULATION INSTRUCTIONS

6.2.1 COMPARE INDEX REGISTER

**CPX**

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
IMMEDIATE	8C	3	3
DIRECT	9C	2	4
INDEXED	AC	2	6
EXTENDED	BC	3	5

**BOOLEAN/ARITHMETIC OPERATION**  
 $(X_H/X_L) - (M/M_{+1})$

**DESCRIPTION**  
 The 16 bit Index Register is compared to the contents of two consecutive memory locations.

		7	T	8	
5	4	3	2	1	0
H	I	N	Z	V	C

6.2.2 DECREMENT INDEX REGISTER

**DEX**

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	09	1	4

**BOOLEAN/ARITHMETIC OPERATION**  
 $X - 1 \rightarrow X$

**DESCRIPTION**  
 The Index Register is decremented by one

			I		
5	4	3	2	1	0
H	I	N	Z	V	C



6 INSTRUCTION SET

6.2 INDEX REGISTER AND STACK POINTER MANIPULATION INSTRUCTIONS

6.2.3 DECREMENT STACK POINTER

DES

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	34	1	4

BOOLEAN/ARITHMETIC OPERATION

$$SP - 1 - SP$$

DESCRIPTION

The stack pointer register is decremented by one. . . .

5	4	3	2	1	0
H	I	N	Z	V	C

6.2.4 INCREMENT INDEX REGISTER

INX

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	08	1	4

BOOLEAN/ARITHMETIC OPERATION

$$X + 1 \rightarrow X$$

DESCRIPTION

The Index Register is incremented by one.

				I	
5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.2 INDEX REGISTER AND STACK POINTER MANIPULATION INSTRUCTIONS

6.2.5 INCREMENT STACK POINTER

INS

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	31	1	4

BOOLEAN/ARITHMETIC OPERATION

$$SP + 1 - SP$$

DESCRIPTION

The stack pointer register is incremented by one

5	4	3	2	1	0
H	I	N	Z	V	C

6.2.6 LOAD INDEX REGISTER

LDX

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
IMMEDIATE	CE	3	3
DIRECT	DE	2	4
INDEXED	EE	2	6
EXTENDED	FE	3	5

BOOLEAN/ARITHMETIC OPERATION

$$M \rightarrow X_H, (M_{+1}) \rightarrow X_L$$

DESCRIPTION

Two bytes are transferred from memory to the Index Register.

		9	I	R	
5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.2 INDEX REGISTER AND STACK POINTER MANIPULATION INSTRUCTIONS

6.2.7 LOAD STACK POINTER

LDS

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
IMMEDIATE	8E	3	3
DIRECT	9E	2	4
INDEXED	AE	2	6
EXTENDED	BE	3	5

BOOLEAN/ARITHMETIC OPERATION

$$M \rightarrow SP_H, (M_{+1}) \rightarrow SP_L$$

DESCRIPTION

A two byte address is transferred from memory to the stack pointer register.

		9	T	R	
5	4	3	2	1	0
H	I	N	Z	V	C

6.2.8 STORE INDEX REGISTER

STX

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
DIRECT	DF	2	5
INDEXED	EF	2	7
EXTENDED	FF	3	6

BOOLEAN/ARITHMETIC OPERATION

$$X_H \rightarrow M, X_L \rightarrow (M_{+1})$$

DESCRIPTION

The two byte Index Register contents are transferred to memory.

		9	T	R	
5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.2 INDEX REGISTER AND STACK POINTER MANIPULATION INSTRUCTIONS

6.2.9 STORE STACK POINTER

STS

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
DIRECT	9F	2	5
INDEXED	AF	2	7
EXTENDED	BF	3	6

BOOLEAN/ARITHMETIC OPERATION

$SP_H \rightarrow M, SP_L \rightarrow (M_{+1})$

DESCRIPTION

The two byte stack pointer address is transferred to memory

		9	T	R	
5	4	3	2	1	0
H	I	N	Z	V	C

6.2.10 Transfer Index Register to Stack Pointer

TXS

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	35	1	4

BOOLEAN/ARITHMETIC OPERATION

$X - 1 \rightarrow SP$

DESCRIPTION

The contents of the Index Register contents are transferred to the Stack Pointer register and decremented by one.

5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.2 INDEX REGISTER AND STACK POINTER MANIPULATION INSTRUCTIONS

6.2.11 TRANSFER STACK POINTER TO INDEX REGISTER

TSX

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	30	1	4

BOOLEAN/ARITHMETIC OPERATION

$SP + 1 \rightarrow X$

DESCRIPTION

The contents of the Stack Pointer are transferred to the index register and incremented by one.

The index register now points to the current data item on the stack.

5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET  
 6.3 BRANCH INSTRUCTIONS

6.3.1 BRANCH ALWAYS

**BRA**

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
RELATIVE	20	2	4

BRANCH TEST  
 NONE

DESCRIPTION  
 Unconditional branch to the specified relative address.

5	4	3	2	1	0
H	I	N	Z	V	C

6.3.2 BRANCH IF CARRY CLEAR

**BCC**

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
RELATIVE	24	2	4

BRANCH TEST  
 $C = 0$

DESCRIPTION  
 Branch if the condition code C bit is 0. The BCC instruction is used to test the results of an unsigned binary operation.

5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.3 BRANCH INSTRUCTIONS

6.3.3 BRANCH IF CARRY SET

BCS

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
RELATIVE	25	2	4

BRANCH TEST

$$C = 1$$

DESCRIPTION

Branch if the condition code C bit is 1. The BCS instruction is used to test the results of an unsigned binary operation.

5	4	3	2	1	0
H	I	N	Z	V	C

6.3.4 BRANCH IF EQUAL TO ZERO

BEQ

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
RELATIVE	27	2	4

BRANCH TEST

$$Z = 1$$

DESCRIPTION

Branch if the condition code bit Z is set to a 1.

5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.3 BRANCH INSTRUCTIONS

6.3.5 BRANCH IF EQUAL TO A GREATER THAN ZERO

BGE

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
RELATIVE	2C	2	4

BRANCH TEST

$$N \oplus V = 0$$

DESCRIPTION

Branch if the condition code N and V bits are both set or branch if the condition codes N bit and V bit are both reset. The BGE instruction is used to test the results of a signed binary operation.

5	4	3	2	1	0
H	I	N	Z	V	C

6.3.6 BRANCH IF GREATER THAN ZERO

BGT

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
RELATIVE	2E	2	4

BRANCH TEST

$$Z + (N \oplus V) = 0$$

DESCRIPTION

Branch if the condition code Z bit is reset and either the N and V bits are both set or reset. The BGT instruction is used to test the results of a signed binary operation.

5	4	3	2	1	0
H	I	N	Z	V	C



6 INSTRUCTION SET  
 6.3 BRANCH INSTRUCTIONS

6.3.7 BRANCH IF HIGHER

BHI

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
RELATIVE	22	2	4

BRANCH TEST

$$C + Z = 0$$

DESCRIPTION

Branch if the condition code bits C and Z are both reset. The BHI instruction is used to test the results of an unsigned binary operation.

5	4	3	2	1	0
H	I	N	Z	V	C

6.3.8 BRANCH IF LESS THAN OR EQUAL TO ZERO

BLE

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
RELATIVE	2F	2	4

BRANCH TEST

$$Z + (N \oplus V) = 1$$

DESCRIPTION

Branch if the condition code Z bit is set, or the condition code N bit is set and the condition code V bit is reset, or if the condition code N bit is reset and the condition code V bit is set. The BLE instruction is used to test the results of a signed binary operation.

5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.3 BRANCH INSTRUCTIONS

6.3.9 BRANCH IF LOWER OR SAME

BLS

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
RELATIVE	23	2	4

BRANCH TEST

$$C + Z = 1$$

DESCRIPTION

Branch if either the C bit or the Z bit is set. The BLS instruction is used to test the results of an unsigned binary operation.

5	4	3	2	1	0
H	I	N	Z	V	C

6.3.10 BRANCH IF LESS THAN ZERO

BLT

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
RELATIVE	2D	2	4

BRANCH TEST

$$N \oplus V = 1$$

DESCRIPTION

Branch if the condition code N bit is set and the condition V bit is reset, or if the condition code N is reset and the condition code V bit is set. The BLT instruction is used to test the results of a signed binary operation

5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.3 BRANCH INSTRUCTIONS

6.3.11 BRANCH IF MINUS

BMI

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
RELATIVE	2B	2	4

BRANCH TEST

N = 1

DESCRIPTION

Branch if the condition code N bit is set.

5	4	3	2	1	0
H	I	N	Z	V	C

6.3.12 BRANCH IF NOT EQUAL TO ZERO

BNE

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
RELATIVE	26	2	4

BRANCH TEST

Z = 0

DESCRIPTION

Branch if the condition code Z bit is reset.

5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.3 BRANCH INSTRUCTIONS

6.3.13 BRANCH IF OVERFLOW CLEAR

BVC

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
RELATIVE	28	2	4

BRANCH TEST

V = 0

DESCRIPTION

Branch if the condition code V bit is reset.

5	4	3	2	1	0
H	I	N	Z	V	C

6.3.14 BRANCH IF OVERFLOW SET

BVS

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
RELATIVE	29	2	4

BRANCH TEST

V = 1

DESCRIPTION

Branch if the condition code V bit is set.

5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.3 BRANCH INSTRUCTIONS

6.3.15 BRANCH IF PLUS

BPL

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
RELATIVE	2A	2	4

BRANCH TEST

N = 0

DESCRIPTION

Branch when the condition code N bit is reset.

5	4	3	2	1	0
H	I	N	Z	V	C

6.3.16 BRANCH TO SUBROUTINE

BSR

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
RELATIVE	8D	2	8

DESCRIPTION

The two byte address of the byte following the Branch to Subroutine instruction is pushed on the stack. The next instruction will be fetched as if this instruction were a branch always.

5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.3 BRANCH INSTRUCTIONS

6.3.17 JUMP

JMP

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INDEX	6E	2	4
EXTENDED	7E	3	3

DESCRIPTION

Unconditional jump to the specified address, similar to BRA, but may branch farther than 127 bytes.

5	4	3	2	1	0
H	I	N	Z	V	C

6.3.18 JUMP TO SUBROUTINE

JSR

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INDEXED	AD	2	8
EXTENDED	BD	3	9

DESCRIPTION

The two byte address of the instruction following the Jump to Subroutine instruction is pushed on the stack similar to BSR except may branch farther than 127 bytes.

5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.3 BRANCH INSTRUCTIONS

6.3.19 NO OPERATION

NØP

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	01	1	2

BRANCH TEST

Advances Program Counter Only

5	4	3	2	1	0
H	I	N	Z	V	C

DESCRIPTION

The NØP instruction advances the program counter by one.

6.3.20 RETURN FROM SUBROUTINE

RTS

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	39	1	5

DESCRIPTION

The top two bytes of the stack are "pulled" into the Program Counter register. This instruction is used to return from BSR or JSR called routines.

5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.4 CONDITION CODE MANIPULATION INSTRUCTIONS

6.4.1 CLEAR CARRY

CLC

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	0C	1	2

BOOLEAN/ARITHMETIC OPERATION

0 → C

DESCRIPTION

The condition code register C bit is reset to 0.

					R
5	4	3	2	1	0
H	I	N	Z	V	C

6.4.2 CLEAR INTERRUPT MASK

CLI

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	0E	1	2

BOOLEAN/ARITHMETIC OPERATION

0 → I

DESCRIPTION

The condition code register interrupt mask bit is reset to 0.

	R				
5	4	3	2	1	0
H	I	N	Z	V	C



6 INSTRUCTION SET

6.4 CONDITION CODE MANIPULATION INSTRUCTIONS

6.4.3 CLEAR OVERFLOW

CLV

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	0A	1	2

BOOLEAN/ARITHMETIC OPERATION

0 → V

DESCRIPTION

The condition code register overflow bit is reset to 0.

				R	
5	4	3	2	1	0
H	I	N	Z	V	C

6.4.4 SET CARRY

SEC

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	0D	1	2

BOOLEAN/ARITHMETIC OPERATION

1 → C

DESCRIPTION

The condition code register C bit is set to

					S
5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.4 CONDITION CODE MANIPULATION INSTRUCTIONS

6.4.5 SET INTERRUPT MASK

SEI

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	OF	1	2

BOOLEAN/ARITHMETIC OPERATION

1 → I

DESCRIPTION

The condition code register interrupt mask bit is set to 1. Peripheral device interrupts are not serviced until the interrupt mask is cleared.

	S				
5	4	3	2	1	0
H	I	N	Z	V	C

6.4.6 SET OVERFLOW

SEV

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	OB	1	2

BOOLEAN/ARITHMETIC OPERATION

1 → V

DESCRIPTION

The condition code register overflow bit is set to 1.

				S	
5	4	3	2	1	0
H	I	N	Z	V	C

6 INSTRUCTION SET

6.4 CONDITION CODE MANIPULATION INSTRUCTIONS

6.4.7 TRANSFER ACCUMULATOR A TO CONDITION CODE REGISTER

TAP

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	06	1	2

BOOLEAN/ARITHMETIC OPERATION  
A → CCR

DESCRIPTION

The contents of accumulator A are transferred to the condition code register.

12	12	12	12	12	12
5	4	3	2	1	0
H	I	N	Z	V	C

6.4.8 TRANSFER CONDITION CODE REGISTER TO ACCUMULATOR A

TPA

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	07	1	2

BOOLEAN/ARITHMETIC OPERATION  
CCR → A

DESCRIPTION

The contents of the condition code register are transferred to accumulator A

5	4	3	2	1	0
H	I	N	Z	V	C

## 7 INTERRUPT INSTRUCTIONS AND OPERATION

INTERRUPTS are a means of signaling the occurrence of an external event to the SPHERE computer system. These events typically include indications of a device operation complete, change in status of an external device, or indication of a certain time elapsed. When an interrupt occurs, it generally indicates that the need to perform some action such as read some data that is now ready, ring an alarm indicating an abnormal status, or monitor a patient's heartbeat. If the computer were only doing one thing at a time, a computer could constantly monitor what is happening. If, however, a computer were also performing some other task then that task must be "interrupted" to perform the new task. All interrupts except the Reset interrupt save the registers in the format, shown in Figure 7.1.

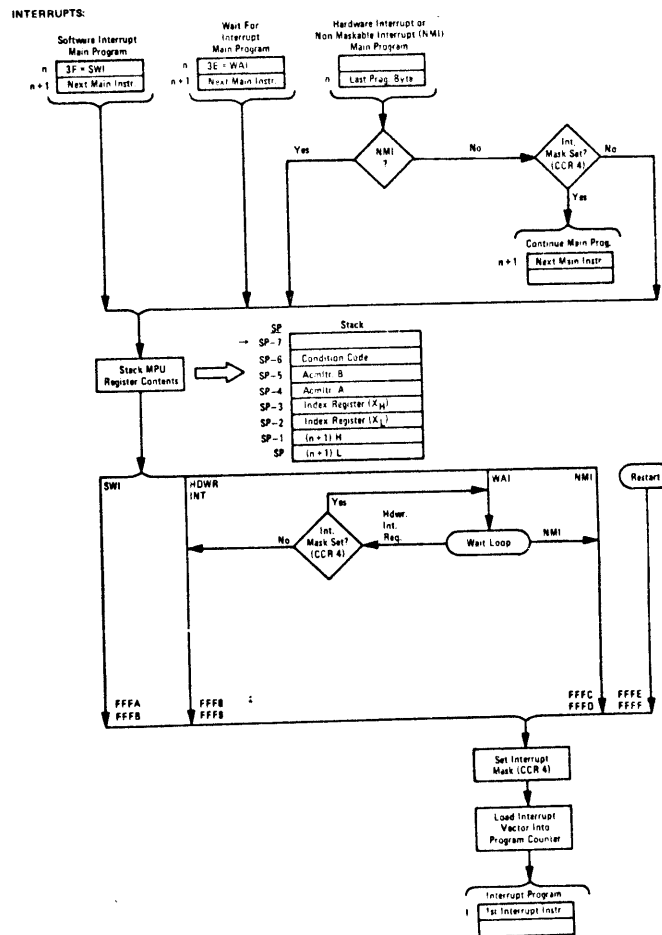


FIGURE 7.1  
INTERRUPTS

## 7 INTERRUPT INSTRUCTIONS AND OPERATION

### 7.1 INTERRUPT THEORY OF OPERATION

There are four types of Interrupts that may occur on the SPHERE system. They are as follows:

- 1 - RESET INTERRUPT
- 2 - NON-MASKABLE INTERRUPT
- 3 - SOFTWARE INTERRUPT
- 4 - DEVICE INTERRUPT

Each interrupt has its use and general characteristics.

#### 7.1.1 RESET INTERRUPT

This interrupt is normally used following power on to reach an initializing program that sets up system starting conditions such as the initial values of the stack pointer, peripheral interface startup states, and initial program counter. The reset interrupt is also used to restart the system in the event that there is a lock-up or runaway. Since this interrupt is used to start or restart the system, no registers are saved. The process will retrieve an address from locations FFFE and FFFF and jump to those addresses. These locations are located in the Read Only Memory of the system. Standard procedure dictates that this address is an address of the startup routine in Read Only Memory (ROM).

#### 7.1.2 NON-MASKABLE INTERRUPT

The Non-Maskable Interrupt is similar to the standard device interrupt except, as its name implies, the central processor must service this interrupt. This interrupt is principally used as a power failure interrupt. This interrupt may also be used to service a "Hot" device which cannot wait for anything. This interrupt is not used by the SPHERE SYSTEM. The processor will retrieve an address from locations FFFC and FFFD and jump to the indicated location. Since this feature is not implemented in the SPHERE SYSTEM, all SPHERE ROM's will indicate location 0104 as the NMI Interrupt Vector Location.

#### 7.1.3 SOFTWARE INTERRUPT

The Software interrupt is provided so that the user can easily Save and Restore his registers. One convenient use of this feature is its peculiar ability to be useful as an Executive call. It is most often used to implement breakpoint or single stepped operation. Further information on the Operation of the SWI Interrupt Vector locations are FFFA and FFFB the SPHERE system default address is location 0100.

## 7 INTERRUPT INSTRUCTIONS AND OPERATION

### 7.1 INTERRUPT THEORY OF OPERATION

#### 7.1.4 DEVICE INTERRUPT

This interrupt is the mainstay of interrupt processing. It provides a convenient facility for rapid processing of device I/O and status. Locations FFF8 and FFF9 contain the address of the routine that processes device interrupts. Typically the routine that processes these interrupts first checks the interrupts of highest priority. Below is a typical list in priority order:

1. Process control devices requiring high speed response
2. Character oriented devices (High speed)
3. Character oriented devices (Low speed)
4. Lowest speed DMA device (operation done)
5. Highest speed DMA device (operation done)
6. Lowest requirement process sense
7. Requiring no immediate response

Interrupt is vectored to location 0108.

### 7.2 INTERRUPT PROCESSING INSTRUCTIONS

#### 7.2.1 RETURN FROM INTERRUPT

RTI

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	3B	1	10

BOOLEAN/ARITHMETIC OPERATION

DESCRIPTION

The status of the computer at the time of the last interrupt is restored from the stack. The registers including the PC are restored and execution continues from interrupted task.

10	10	10	10	10	10
5	4	3	2	1	0
H	I	N	Z	V	C

7 INTERRUPT INSTRUCTIONS AND OPERATION

7.2 INTERRUPT PROCESSING INSTRUCTIONS

7.2.2 SOFTWARE INTERRUPT

SWI

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	3F	1	12

BOOLEAN/ARITHMETIC OPERATION

DESCRIPTION

The seven bytes of computer status are saved on the stack, including the address following the SWI instruction, which is saved for the return from interrupt.

	S				
5	4	3	2	1	0
H	I	N	Z	V	C

7.2.3 WAIT FOR INTERRUPT

WAI

ADDRESSING MODE	OPERATION CODE	NUMBER OF BYTES	NUMBER OF CYCLES
INHERENT	3E	1	9

BOOLEAN/ARITHMETIC OPERATION

DESCRIPTION

The seven bytes of computer status are saved on the stack, including the address following the wait instruction, which is saved for the return from interrupt.

		11			
5	4	3	2	1	0
H	I	N	Z	V	C

## 8 ELEMENTARY PROGRAMMING TECHNIQUES

A digital computer is capable of storing information, performing calculations, then making decisions based on the results of the calculations and arriving at a final solution to the given problems. However, the computer cannot perform even a simple task without direction. Each step of the task must be worked out in advance by the programmer.

The programmer must write a program for the computer to follow. The program consists of a list of instructions which the computer must follow step by step to arrive at the desired solution. This list of instructions, called a program, is based on a computational method which is sometimes referred to as an algorithm, to solve the problem. The program or list of instructions is placed in the computer memory to activate the control circuitry of the computer in a specific response pattern specified by the programmer to perform the computation algorithm.

To solve a problem with a computer the programmer proceeds through five programming phases as listed below:

1. Define the problem
2. Determine a solution
3. Analyze and design the program (flowcharting)
4. Code the program in the programming language
5. Program check out (debug)

The following sections describe the procedures to be followed when writing a program.

### 8.1 DEFINE THE PROBLEM

Defining the problem is probably the most important step in the design of a program for much time and energy can be wasted in trying to get the computer to solve a problem with unknowns. Remember, the computer must know each step. The programmer cannot tell the computer to "do what I mean". The computer must be given an exact set of instructions, it knows only "do what I say".

The major stumbling block in getting a computer to perform is generally found in the definition of the problem what is to be solved. If there is sufficient data available that can be given values which the computer can interpret it can solve very simple or very complex problems. The problems which the computer can be directed to solve need to be defined in small enough segments that they can be easily understood by the programmer for he must instruct the computer in each step of the process.



## 8 ELEMENTARY PROGRAMMING TECHNIQUES

### 8.1 DEFINE THE PROBLEM cont'd

A simple arithmetic sequence to add two numbers may be accomplished more rapidly with pencil and paper than writing the program to perform the same steps with the computer. The advantage of the computer is that if this same set of arithmetic operations must be performed many, many times with variable data now the computer can perform the additions much more rapidly. It is a trade off of using the tool, the computer, to perform the function for which it was designed.

The programmer must realize that the definition must be accurate if the computer is to provide an accurate result. Defining the problem for the average of ten numbers is obvious. However, when the problem is to monitor equipment performance such as airconditioners or heating systems in a high rise building, or to optimize the electrical system loading, a precise definition of the problem is required. The question is what exactly must the program do?

### 8.2 FINDING A SOLUTION

Finding a solution is the second phase in solving a problem with the computer. There are as many different ways to solve a problem as there are programmers. The selection of one method over another is often determined by the particular hardware or computer system to be used. Finding the best solution to a problem varies in difficulty and in number of solutions with the complexity of the problem. Each individual programmer will evaluate a problem in the light of his own experience and will make judgments determined by his evaluation. Each individual programmer may select a different method for arriving at the solution and yet all may be correct in giving the same answer the same problem.

Mastery of the computer instruction set is a requirement for design as well as programming to solve a problem. Efficient use of instructions are important in considering execution speed and memory space requirements. It is interesting to note that over the years two specific goals have always been at odds with each other. As a general rule the faster a program runs, the bigger it is while the small programs tend to run a little bit longer.

### 8.3 ANALYZE AND DESIGN (FLOWCHARTING)

When a particular method is selected, based on the definition of the problem then the programmer must develop that method into a solution that will work. The programmer may now analyze and design the solution into a program. This is to be accomplished by identifying the steps that are necessary to solve the problem and arranging them into a logical order. A graphic technique called flowcharting has been developed as

8 ELEMENTARY PROGRAMMING TECHNIQUES  
8.3 ANALYZE AND DESIGN (FLOWCHARTING) cont'd

an effective method for representing the logical steps in a program. The flowcharting technique is an effective method for quickly graphing out a visual representation for the programmer to evaluate alternative approaches to individual or combination of steps of the program. The objective is to implement the method for solving the problem into logical steps which can be coded as instructions for the computer. Various flowcharting symbols have become standardized to indicate the processes which are to be accomplished by the computer. Normal process blocks, decisions and directional flow arrows between the symbols provide a quick reference for the programmer to scan through simple or complex portions of a program. See Figure 8-1

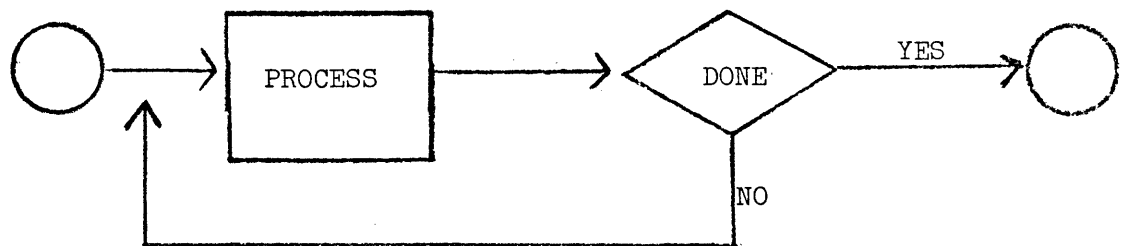


FIGURE 8-1

The flowchart organizes the processing steps which must be performed by the computer and provides a tremendous advantage to the programmer when he is determining which method will be used in the solving of a problem in addition the flowchart can be a valuable aid to the programmer when he is determining the coding required for program instructions and also for the checking of the program during the debug phase. The flowchart will be developed for use by the programmer. The amount of detail in the flowchart will be determined by the complexity of the problem and the experience of the programmer. Each programmer should remember that someone will come along after him and want to, need to, or have to understand the program, at this point a well done flowchart with sufficient detail and explanation will be valuable assets. The examples shown in Figure 8-2, 8-3, and 8-4 illustrate a summation program and two sort programs.

8 ELEMENTARY PROGRAMMING TECHNIQUES  
8.3 ANALYZE AND DESIGN (FLOWCHARTING) cont'd

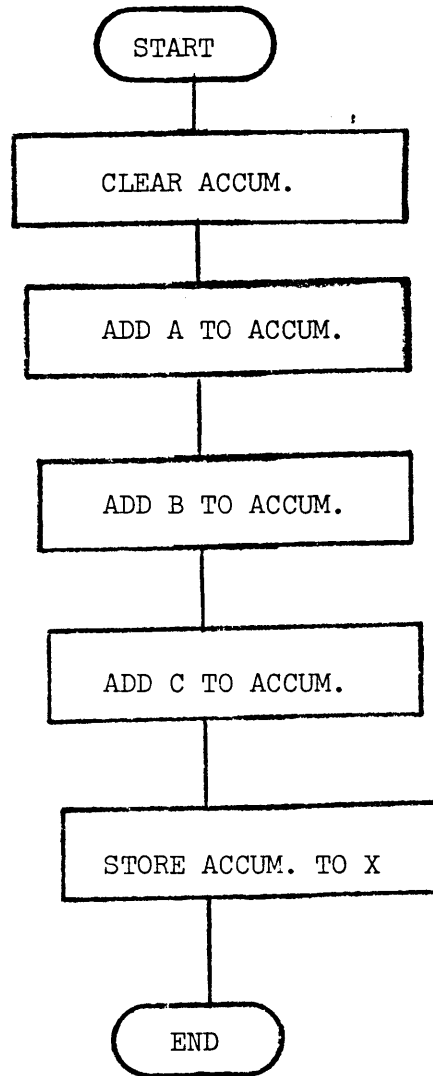
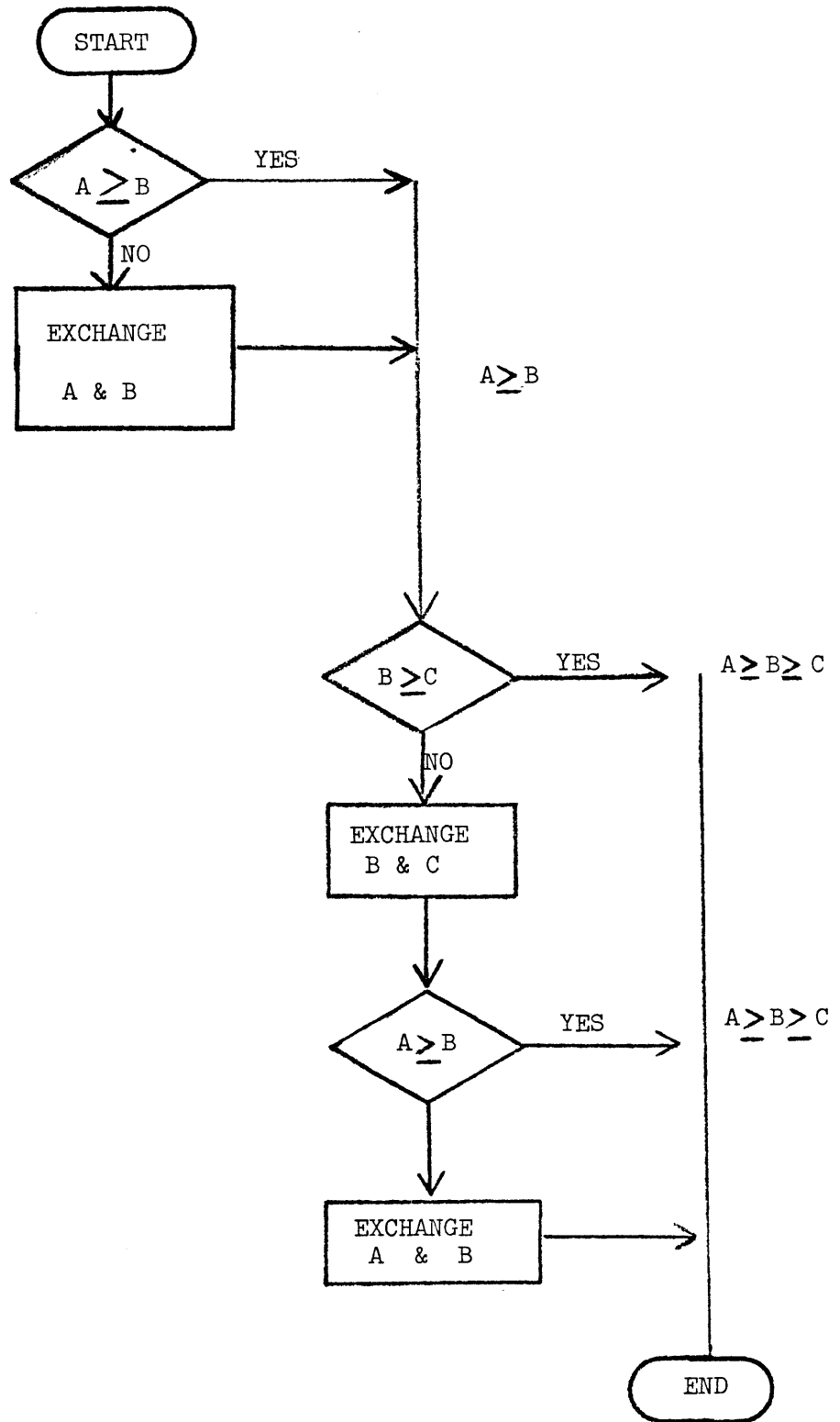


FIGURE 8-2

Let  $X = A + B + C$

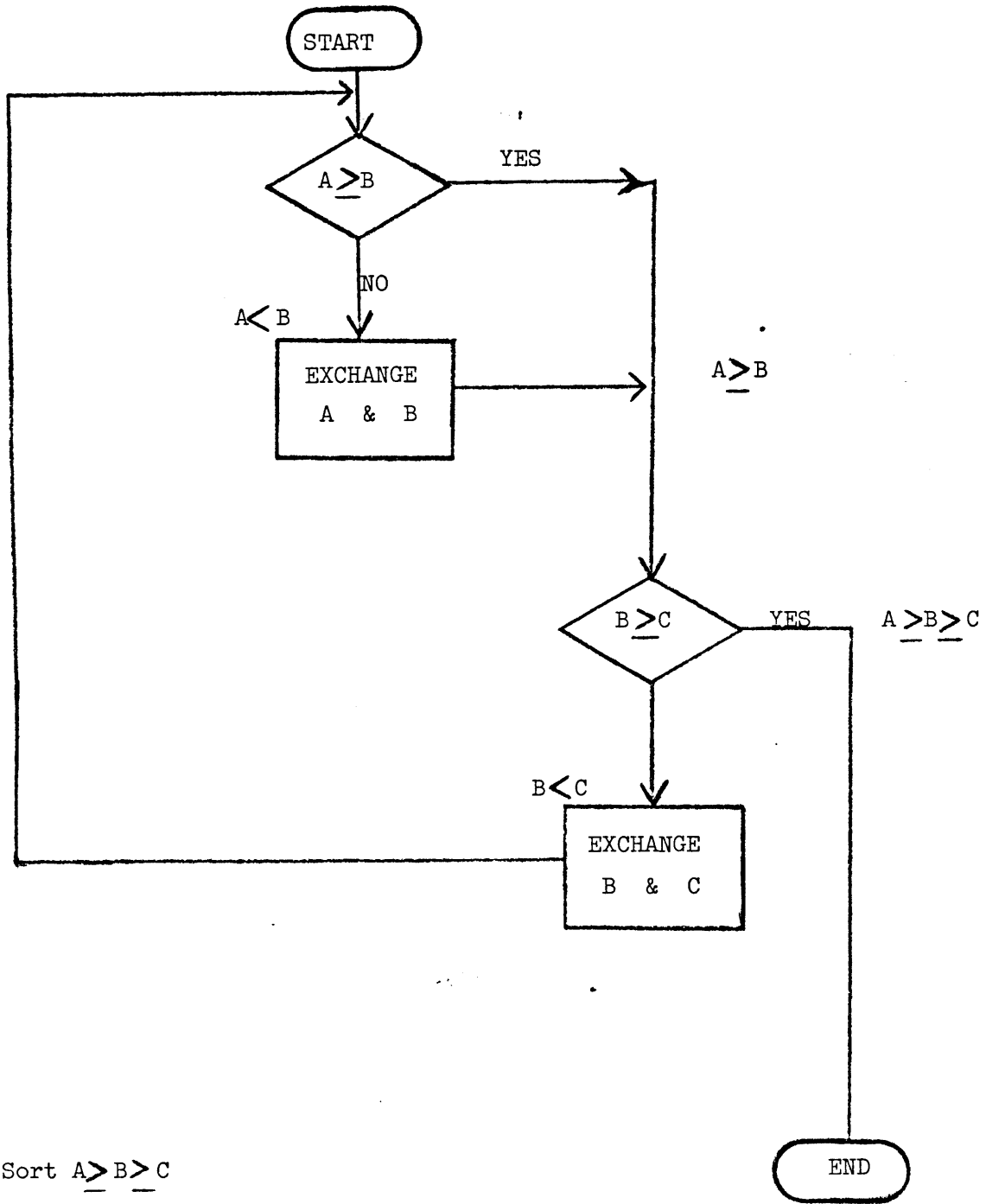
8 ELEMENTARY PROGRAMMING TECHNIQUES  
 8.3 ANALYZE AND DESIGN (FLOWCHARTING) cont'd



Sort A > B > C

FIGURE 8-3

8 ELEMENTARY PROGRAMMING TECHNIQUES  
8.3 ANALYZE AND DESIGN (FLOWCHARTING) cont'd



Sort A > B > C

FIGURE 8-4

## 8 ELEMENTARY PROGRAMMING TECHNIQUES

### 8.4 CODING THE PROGRAM

On reaching this point the programmer is ready to begin coding the program. This step is often called 'Programming'; however, it is really the coding phase of programming a problem. All of the preceding steps and the following step must necessarily be accomplished as part of programming the computer for a problem. This step is properly called the Coding Phase. Coding the solution into the programming language or the language that can be understood by the computer.

Early computers required that each machine instruction be converted into a binary number by a programmer. As machine usage and experience progressed assembler programs were developed to perform the conversion process. Now the programmer could use symbolic references and the computer would assemble instructions for itself. However, each instruction was still required to be written by a programmer. Macro Assemblers and Compilers (FORTRAN, COBOL, RPG, ALGOL, BASIC, PL/1) were developed to ease the burden of the programmer. A compiler instruction may generate one or many instructions. The program instructions can be stored in the computer memory and the problem can be solved by the computer. At this point the program is rarely complete. There are very few programs which function exactly as expected on the first try and thus the fifth programming phase must be performed.

### 8.5 PROGRAM CHECKOUT (DEBUG)

The program check out phase is referred to as the 'Debug Phase'. The reference to Debug refers to little flaws that may be in the program. These flaws may be instructions left out, instructions improperly sequenced, or tests operations which are performed incorrectly. These flaws, or bugs as they are called, must be found and corrected. The approach to debugging a program must be methodical, exacting, and requires testing of each step of a program. Don't just check out your program with ideal test data that your program was written to use, quite often programs fail when they are asked to use bad data to compute with. Make sure that your program can handle bad data and report error conditions instead of run off and output an answer that is not correct for the input.

## 9 SYSTEM SOFTWARE

The One Card Computer software is supplied to all users of the System 300 CPU card that do not have a larger system. The Program Development System is standard on systems 310, 320 and 330 while SDOS is for the 340 user. All of these represent a unique approach to the software of a low cost computer system since no bootstrapping is required to begin execution; each system has enough Read Only Memory to contain the basic operating system while other computers require lights and switches. The operation of a SPHERE is through the ROM and standard I/O devices.

### 9.1 ONE CARD COMPUTER SOFTWARE

Contained in the two ROM's on the 300 CPU are teletypewriter I/O drivers and a simple debug program. With this software and a 110 baud terminal or TTY one can develop programs and applications for many different things.

#### 9.1.1 ONE CARD COMPUTER DEBUGGER V2.0

The one card computer debugger has the ability to examine and change memory, set and clear breakpoints, branch to a program and examine and change the registers while stopped at a breakpoint. The characters used for these functions are as follows:

- C/B Breakpoint at opened location
- C/C Clear breakpointed location
- C/E Exit back to where breakpoint was encountered
- G Branch to opened location
- O Open a location
- R Open location pointed to by (SP + 1)
- S Set stack pointer
- + Open next location
- Open previous location
- SP Change contents of the opened location
- CR End of numericfield, execute command

The debugger is executed automatically by system reset: The prompt character "#" should be displayed.

The most common procedure would probably be to open a memory location. This process causes the contents of the specified location to be displayed. To change the contents of that location, enter a space, new contents, and carriage return. To set a breakpoint on an opened location, press control and B at the same time. The breakpoint is set by saving the contents of the specified byte in a reserved location and replacing it with a SWI instruction. When the instruction with the breakpoint

## 9 SYSTEM SOFTWARE

### 9.1 ONE CARD COMPUTER SOFTWARE

#### 9.1.1 ONE CARD COMPUTER DEBUGGER V2.0 cont'd

as its operation code is encountered, a software interrupt is generated which returns control to Debug. To remove the breakpoint, enter control C, which will restore the op code to the instruction which was breakpointed. To return from the interrupt, enter control E. The saved program counter will be decremented by one so that the interrupted instruction will be executed and control will be returned to the location which contained the breakpointing SWI instruction. To execute a program the G command will cause a jump indexed (6E00) with the index register containing the address of the last opened location. While at an interrupt the stack can be examined with the R command. The S command can be used to initialize the stack pointer but must not be used while at an interrupt because the stack then contains valuable data. See Figure 9-1

#### 9.1.2 ONE CARD COMPUTER SUBROUTINES

Available in the One Card Computer ROM's are utility routines used by the debugger. When the function of these routines are well defined they can be used by user written programs. Available are routines for input and output and a command dispatcher.

CASC	Low 4 bits of accumulator A converted to ASCII and output. High bits lost, condition code modified.
CNTRLO	Outputs an up-arrow as indication of a control character then outputs character in accumulator A, condition code register modified.
CO	Outputs character in accumulator A. Condition code register modified.
CRLF	Outputs carriage return and linefeed. Accumulator A and condition code registers modified.
DSPA	Outputs accumulator A in Hexadecimal. Accumulator A and condition code registers modified.
DSPX	Outputs index register in Hex. Accumulator A and condition code registers modified.
GDICIT	Inputs, echoes and converts the input to base 16. Accumulator A contains returned value, condition code register modified; carry set if not hexadecimal input



9 SYSTEM SOFTWARE  
 9.1 ONE CARD COMPUTER SOFTWARE

<u>#0 400CB</u>	open location 400
<u>0400 xx # 01CB</u>	contents of location don't matter enter a NOP
<u>#+</u>	open next location
<u>0401 xx # 20CB</u>	enter op code of BRANCH ALWAYS
<u>#+</u>	
<u>0402 xx # FD CB</u>	enter relative address of branch
<u>#0 400CB</u>	open location 400 again
<u>0400 01 #+</u>	check to see if program is right
<u>0401 20 #+</u>	
<u>0402 FD #-</u>	open previous location
<u>0401 20 #C/B#-</u>	set breakpoint at 401, open previous location
<u>0400 01 #+</u>	
<u>0401 3F #-</u>	look where branch was, now SWI instruction
<u>0400 01 #G</u>	begin execution at opened location, 400
<u>SWI @ 0401</u>	SWI was forend at 401
<u>#R</u>	look at registers in stack
<u>0FEA xx #+</u>	condition code, doesn't matter
<u>0FEB xx #+</u>	accumulator B, doesn't matter
<u>0FEC xx #+</u>	accumulator A, doesn't matter
<u>0FED 04 #+</u>	high byte of index register
<u>0FEE 00 #+</u>	low byte of index register
<u>0FEF 04 #+</u>	high byte of interrupted program counter
<u>0FF0 02 #C/C</u>	low byte of PC, clear breakpoint
<u>0401 20 #-</u>	displays restored contents automatically
<u>0400 01 #C/B#C/E</u>	set breakpoint at 400, exit current interrupt
<u>SWI @ 0400</u>	trap found at 400
<u>#R</u>	look at registers again
<u>0FEA xx #+</u>	
<u>0FEB xx #+</u>	
<u>0FEC xx #+</u>	
<u>0FED 04 #+</u>	index still points to location we did G from
<u>0FEE 00 #+</u>	
<u>0FEF 04 #+</u>	
<u>0FF0 01 #C/C</u>	note PC, still address of next instruction
<u>0400 01 #C/E</u>	but now 401, not 402 as above
	with breakpoint cleared, return from interrupt
	program goes infinite

FIGURE 9-1

OPERATION OF ONE CARD COMPUTER DEBUGGER

## 9 SYSTEM SOFTWARE

### 9.1 ONE CARD COMPUTER SOFTWARE

#### 9.1.2 ONE CARD COMPUTER SUBROUTINES cont'd

INPCHR	Inputs and echoes character. Accumulator A contains character, condition code register modified.
INPNUM	Last 4 hexdigits placed in X. Accumulators and condition code register modified.
MSGOUT	Outputs a message terminated by a byte of zero, X contains message address. Index accumulator A and condition code registers modified.
PCOM	Dispatcher. Index register contains address of table of three byte entries, accumulator A contains key character. Outputs "?" if contents of A not in table else JSR's to specified routine. All registers used. Table format: one byte character, two byte address, etc. ended with character byte = 0.
SPACE	Outputs ASCII space. Condition code modified.

## 9.2 PROGRAM DEVELOPMENT SYSTEM

The software, consisting of a debugger, assembler, editor, 16 bit arithmetic, and ASCII conversion routines, allows for development of user software in much the same way as large disk based systems. The SPHERE Debugging Aid (SDA) is designed to allow the user to easily view and alter the contents of memory or CPU registers from the keyboard-CRT display. The Mini-Assembler allows the user the ability to input source assembly language programs (via the editor) and output absolute binary object code. It can handle up to 62 symbolic addresses, different operand sizes and octal, decimal hexadecimal, and symbolic operands. The operation codes are entered in hexadecimal (i.e. ADDA immediate is "8B"). Included is a set of routines for 16 bit arithmetic manipulation. The routines include 16 bit multiply and divide as well as ASCII-to-BINARY and BINARY-to-ASCII conversion routines operating on 16 bit binary numbers. On the SIM board included with systems 320 and 330 are subroutines to perform input-output on audio cassettes, modems or serial devices thru Asynchronous Communications Interface Adapters. The system includes a built in CRT based editor allowing scrolling and text insertion and deletion based on a cursor, allowing easy text manipulation.

When power is turned on, or when a manual reset is performed the system initializes its parameters and goes into executive mode. Entry into executive mode causes the display to blank and enables input from the keyboard. All valid commands are a single character.

9 SYSTEM SOFTWARE

9.2 PROGRAM DEVELOPMENT SYSTEM cont'd

If a Non-command character is entered it will be echoed, and followed by a Carriage Return. The acceptable Command Characters are listed below with their associated function:

"Ctrl A"	ASSEMBLE
"Ctrl D"	DEBUG
"Ctrl E"	EDIT
"Ctrl R"	RE-EDIT

9.2.1 MINI-ASSEMBLER

The Mini-Assembler is entered via the Ctrl A Command from the keyboard to assemble source code from a fixed position in memory. The low memory pointer SRCASM is set up by the editor to point to the start of the source code. This assembler requires that only one statement reside on a line at a time. Each line to be assembled must appear in fixed format. Each line must end in a carriage return, however, the CR is not recognized until after column 8 of the input line. Below is a description of the assembler statement format.

<u>Example</u>	<u>B</u>	<u>_</u>	<u>_</u>	<u>7</u>	<u>F</u>	<u>_</u>	<u>E</u>	<u>*</u>	<u>2</u>	<u>3</u>	<u>4</u>
Input position	1	2	3	4	5	6	7	8	9	10	11

LOCATION TAG: Position 1  
This position contains any one of the Sixty three ASCII characters or a blank. Placing a non-blank character in this position allows the user to access the location in other places by a label rather than an address.

EQUATE: Position 2  
This position may contain an "=" or a blank. If it is equal to "=", then the location label (position) will reference the location specified by the operand.  
(position 8 +)

OP-CODE: Position 4 and 5  
These positions may contain spaces or a two digit, hexadecimal equivalent of an instruction code. If the field is blank no allocation of memory will be made for the instruction code. Otherwise the supplied two hexadecimal digits will be converted to a single byte and be deposited in the current assembly output location.

## 9 SYSTEM SOFTWARE

### 9.2 PROGRAM DEVELOPMENT SYSTEM

#### 9.2.1 MINI-ASSEMBLER cont'd

##### OPERAND TYPE: Position 7

This field may contain one of the three letters R, D, E, or a blank. If the operand type is blank no operand will be evaluated and no allocation of memory will take place. An "R" specifies that the operand in positions 8 + will create one byte of data relative to the current label assignment plus 2, this operand type is used for branches. A "D" specifies that the operand in position 8 + will create one byte of data. An "E" specifies that the operand in positions 8 + will create two bytes of data.

##### OPERAND VALUE: Positions 8 +

These positions must be terminated by a space or a carriage return. The four forms of operand values are described below:

- (1) @ - The at sign "@" followed by a single character indicates that data shall be referenced at the location specified by the letter following the "@". The reference is to the last definition encountered before it is used. The definition can be made on either the first or second pass (backward or forward references respectively)
- (2) One or more hexadecimal characters. If a number overflows the 16 bit BA register, only the low order 16 bits are saved, high order bits are best.
- (3) One or more decimal digits preceded by a period.
- (4) One or more octal digits preceded by an asterisk.

An origin may be defined by using a blank tag equate. To end a program, type 'END' on the last line. The start of executable code will be at the end of the source text or at the location specified by an origin statement. The assembler returns to command mode on completion. No errors are flagged in the mini-assembler, so be sure to check your object output.

## 9 SYSTEM SOFTWARE

### 9.2 PROGRAM DEVELOPMENT SYSTEM

#### 9.2.2 SPHERE DEBUGGING AID (V3N, V3D)

The SPHERE Debugging aid is designed to aid the user in debugging his programs. It allows the user to perform functions usually done through the front console, such as modify the contents of a location or start program execution, as well as debug programs. It is entered from command mode by typing a C/D. Initially the ">" will appear indicating that a debug command will be accepted. The following are the acceptable debug commands:

- Space            CHANGE After the contents of a location have been displayed and the user wishes to change the contents of the location, he may type a space followed by an octal, decimal or hexadecimal number. Octal numbers are prefixed by an asterisk, decimal numbers are preceded by a period.
- +                OPNNXT When the plus ("+") is typed the location following the last displayed location will be displayed and available to other commands.
- OPNPRE When the minus ("-") is typed the location prior to the last displayed location will be displayed and available to other commands.
- C/B            BRKSET This feature causes program operation to cease at the current location whenever it is encountered. This breakpoint instruction is accomplished by placing a SWI instruction in the last examined location and saving its prior value in a location in low memory. This feature is requested by typing a C/B. Breakpoints are used in place of a front console single step switch.
- C/C            CLRSET The breakpoint is cleared when a C/C is typed. The location that was replaced by a SWI instruction by breakset is returned to its original value. The location is automatically displayed.
- C/E            EXIT A C/E is typed when the user desires to resume operation after a breakpoint has been encountered. The breakpoint causing the interruption must be cleared before an Exit is performed to allow the program to continue execution.
- C/G            GO When a C/G is typed control is transferred to the program at the location last examined.

9 SYSTEM SOFTWARE

9.2 PROGRAM DEVELOPMENT SYSTEM

9.2.2 SPHERE DEBUGGING AID (V3N, V3D) cont'd

(C/J)

JUMP Jumps to a user subroutine. This instruction uses a JSR to exit from the Debugger while the (C/G) (go) command uses a JMP.

(C/O)

OPNLOC Opens the location whose address is typed in and displays the byte contents in hexadecimal format. The address is typed in immediately after the O and can be an octal, decimal or hexadecimal number. The address is then printed out on the next line as a hexadecimal number followed by a space and the contents of that memory location.

(C/R)

OPNREG or OPNTOS This instruction opens the Top-Of-Stack. This is used for stepping through the contents of the stack. When DEBUG is entered by a breakpoint, this instruction is used for examining and modifying the CPU registers. When a breakpoint is encountered, the register contents are put on the stack in the following order:

SP	
SP + 1	Condition Code
SP + 2	Accumulator B
SP + 3	Accumulator A
SP + 4	Index Register HIGH
SP + 5	Index Register LOW
SP + 6	Return Address HIGH
SP + 7	Return Address LOW

By stepping through the stack with + command, the registers can be examined and changed.

(C/S)

SETSTK Set stack command. This instruction sets the stack pointer to point to the currently opened location. This is used for changing the stack location from its initial reset position of 01FF<sub>x</sub>.

(C/T)

OPNTBL Opens the symbol table. The location opened is the address of the first character symbol following the T command. The symbol is any one of the symbols used by the Assembler, including the space symbol (program counter).

(C/X)

EXEC This command exits from the Debugger and returns to the executive command interpreter.

(ESC)

The escape character is used to terminate numeric input in the debugger.

## 9 SYSTEM SOFTWARE

### 9.2 PROGRAM DEVELOPMENT SYSTEM

#### 9.2.2 EDITOR

The editor is a routine that does input to a buffer from the keyboard/CRT. It allows for modification of text by cursor manipulation. It is entered by the character C/E typed in the command mode. The editor allows for scrolling in order to allow editing of a text segment larger than can be displayed on the screen. If the cursor is moved off either end of the screen, it causes text to be scrolled up or down. The editor commands are as follows:

KBD/2	KBD/1	
<u>C/L</u> or <u>LF</u>	<u>HOME</u>	sets cursor to home position.
<u>C/X</u> or <u>CLEAR</u>	<u>CLEAR</u>	clears the screen from the cursor position to the bottom of the screen.
<u>C/Q</u>	↑	moves cursor up one line.
<u>C/R</u>	→	moves the cursor one position to the right.
<u>C/S</u>	↓	moves cursor down one line.
<u>C/T</u>	←	moves the cursor one position to the left.
<u>C/DEL</u>	<u>C/KBD</u> ←	moves cursor to left of screen.
<u>CR</u>	<u>CR</u>	carriage return - puts cursor to left of screen on the next line.
<u>C/D</u>	<u>C/D</u>	deletes the top line on the CRT.
<u>C/I</u>	<u>C/I</u>	insert new line at the top of the CRT
<u>ESC</u>	<u>ESC</u>	exit from the editor back to executive.

NOTE: Each line must have a carriage return <sup>at</sup> from proper scrolling.

#### 9.2.4 RE-EDIT

The re-edit command is called from the executive and allows source text to be revised. When entered, the previously edited text is in the low part of the edit buffer. This text can now be scrolled back down onto the screen from the edit buffer by moving the cursor off the top of the screen. Note that if the cursor is moved up past the top line, the editor will move the cursor to the bottom line and insert a blank line (a line with a carriage return only) at the beginning of text.

9 SYSTEM SOFTWARE  
9.2 PROGRAM DEVELOPMENT SYSTEM

9.2.5 UTILITIES

The utility routines are a set of subroutines residing in PROM and used by other PDS routines. They are called by:

JSR                   E, SUBNAME OR

BDaaaa               where aaaa is the address of the utility routine.

and make use of reserved locations in low memory as described in Appendix J. All parameters are passed through low memory locations or registers. Low memory psuedo registers are also listed in the memory map.

ADD32               moves cursor down one line, CSRPTR is passed to ADD32 in X, returned in CSRPTR, scrolls if necessary. Uses accumulator B.

ASCBIN            This routine converts from an ASCII number string pointed to by the index register to an unsigned binary number in accumulators BA. Conversion is from Octal, Decimal, or Hexadecimal. The base is specified by the first digit of the string, decimal has a '.' (2E<sub>x</sub>) for the first digit, octal has an ASCII character less than 2E<sub>x</sub> for the first digit (\*,!,\$,%,#, to name a few). If the first digit is numeric or alphabetic it will be considered part of a hexadecimal number.

BINASC            The BINASC routine converts a 16 bit number in accumulators EA into a string of ASCII digits starting at the address in the index register. Conversion can be any base from base 2 to base 41. For bases greater than 10, the ASCII alphabet A-Z and the following characters are used for representing digits, as is the case with hexadecimal. The base is specified in ARB. Upon return, the index register points to the last character output plus one.

CLEAR             The CLEAR subroutine stores internal carriage returns (60<sub>x</sub>'s) from the cursor position to the end of the CRT display. Both the index register and accumulator B are used by this routine.

CRLF             prints carriage return - line feed. CSRPTR is passed to CRLF in S, returned in CSRPTR but not in X.

DEBUG            This is the entry address to the debugger mentioned above. The DEBUG routine is a main-line program, not a subprogram; JMP to it, don't JSR.



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9.2 PROGRAM DEVELOPMENT SYSTEM  
9.2.5 UTILITIES cont'd

DIVIDE This subroutine divides the 16 bit number in accumulators BA by the 16 bit number in ARA. This routine modifies the index register.

$$\frac{BA}{ARA} \rightarrow \begin{array}{l} \text{BA-quotient} \\ \text{ARA-remainder} \end{array}$$

EDITIN The EDITIN routine provides an input routine that can read a screen of text using cursor controls and carriage returns and returns to the caller when an ESC is pushed. Low memory location SCNPTR points to the start of the text.

EDITOR The Editor routine allows a string of characters to be read in from the keyboard, echoed on the CRT and stored in buffer memory. Editor contains the editor described above. It starts inserting characters at the location specified in BUFADR and continues until BUFEND is hit or the character in ENDCHR is typed. At restart time, BUFADR is set to 200<sub>x</sub>, BUFADR to FFF<sub>x</sub>. ENDCHR is permanently set to the ESC character. On input accumulator A should be non-zero.

EDITRD This entry point to the REEDIT subroutine skips the blanking of the CRT. Like the EDITOR and REEDIT subroutines, accumulator A should be non-zero.

GETCHR The GETCHR subroutine inputs one single character from the keyboard while blinking the cursor at the screen position pointed to by CSRPTR. The character value is returned in accumulator A, the cursor pointer is in the index register as well as CSRPTR.

HOME homes cursor. Both CSRPTR and the index register are reset to the first location of CRT display.

INPCHR does GETCHR and PUTCHR.

INPNUM Inputs a string of characters terminated by an ESC character then calls ASCBIN to convert the string to a binary value in accumulators B,A.

LFTJST moves cursor to the left of the screen. Uses accumulator B.

MULT The MULT routine multiplies 2 unsigned 16 bit numbers to give a 16 bit result. Accumulators BA X ARA → BA. The index register is used in this routine.

9 SYSTEM SOFTWARE  
 9.2 PROGRAM DEVELOPMENT SYSTEM

```

  (C/E)
  = 400 (CR)
  S BD EFEE4 (CR)
    D7 IC (CR)
    97 DC1 (CR)
    BD EFD14 (CR)
    BD EFEE4 (CR)
    97 D05 (CR)
    4F (CR)
    97 D01 (CR)
    BD EFD14 (CR)
    D6 DC (CR)
    96 DC1 (CR)
    DE D10 (CR)
    BD EFF64 (CR)
    BD EFD14 (CR)
    20 RFS (CR)
  ENL (CR)
  seventeen (CR) 's
  (ESC)
  (C/D)
  (C/D)
  (C/O) 407 (ESC)
  0407 (C/D)
  (C/O) 400 (ESC)
  0400 (C/D) 12 (ESC)
  (C/R)
  01F9 xx+
  01FA 00+
  01FB 12+
  01FC xx+
  01FD xx+
  01FE 04+
  01FF 07 (C/O)
  0407 (C/D)
  12 (ESC)
  10010
  1.8 (ESC)
  11 (ESC)
  50
  1*527 (ESC)
  1.4 (ESC)
  8N
  
```

```

  as system starts up in EXECUTIVE mode, enter Editor
  origin this assembly to 400x
  define label S to this instruction, S JSR INPNUM
  STAB TMPB save input number
  STAA TMPA to be converted
  JSR CRLF output carriage return - line feed
  JSR INPNUM input number for base
  STAA AR2 set up number for base
  CLRA of conversion
  STAA AR3
  JSR CRLF
  LDAB TMPB restore number to convert
  LDAA TMPA
  LDY CSRPTB pick up address to output to
  JSR BINASC convert and output the number
  JSR CRLF output a carriage return - line feed
  BRA S do it again
  EMD last statement of assembly is EMD
  scroll all text off screen with (CR)'s
  exit the Editor
  Assemble the Editor's output
  execute Debug
  open a location and set a breakpoint to show
  how it works, not necessary for proper execution.
  open first location of program and begin
  execution. Enter number to convert
  breakpoint encountered, Debug entered automatically
  open top of stack, see condition code register,
  accumulator B,
  accumulator A,
  index register HIGH,
  index register LOW,
  program counter HIGH,
  program counter LOW, clear breakpoint
  automatically displays restored value. Exit breakpoint
  enter base
  12x converted to base 2=10010
  enter number to convert, 80A
  enter base, 10x=16A
  output converted number, 50x
  enter number, 5278
  enter base, 40A
  output converted number, 8E10
  
```

PDS OPERATION

FIGURE 9.2

9 SYSTEM SOFTWARE  
9.2 PROGRAM DEVELOPMENT SYSTEM  
9.2.5 UTILITIES cont'd

OUTSTR        The OUTSTR routine displays the character string from OUTBUF to OUTEND on the CRT starting at the current cursor location.

PNTBYT        This subroutine displays the A accumulator at the current cursor position.

PUTCHR        The PUTCHR subroutine takes the character in accumulator A and displays it on the CRT at the position pointed to by CSRPTR. The cursor is then advanced by one. If the character printed to is a carriage return, then the cursor is put to the first position on the next line. Also scrolls. Both accumulator B and the index register are modified.

REEDIT        This subroutine entry is similar to the EDITOR subroutine mentioned in this section except the BUFADR and BUFEND are not initialized by this entry point. The screen is still blanked by this entry point.

SUB32        moves cursor up one line, scrolls, uses index and accumulator B registers.

9.3        SPHERE DISK OPERATING SYSTEM

SPHERE SYSTEM 340 computers with floppy disks and lineprinter are supplied with SDOS. The SDOS is contained in ROM and on each initialized disk. In the 1K ROM are the disk handler and Debugger routines while on the disk reside the Editor, Assembler and resident SDOS programs. Using the disk handler the resident portion of SDOS is loaded and then application or system programs can be loaded and run.

9.3.1     SDOS DEBUGGER

The Debugger in SDOS resides in ROM and provides the ability to examine memory, change memory and execute programs. The basic commands also include the loading of the SDOS resident. When a system reset is performed this mode is entered. Valid commands include:

Examine memory  
Change memory  
Execute memory  
Invoke SDOS

Invalid commands are echoed and followed by a question mark (?).

## 9 SYSTEM SOFTWARE

### 9.3 SPHERE DISK OPERATING SYSTEM

#### 9.3.1 SDOS DEBUGGER

##### 9.3.1.1 EXAMINE MEMORY

To Examine memory the address of the location of interest is typed and followed by a slash (/). The contents will be displayed immediately after the slash. Consecutive locations can be displayed by entering a slash for each location desired.

##### 9.3.1.2 CHANGE MEMROY

After a location has been examined, it may be changed by entering a space, new contents and a carriage return. The sequence might be as follows:

1234/55 AACR

##### 9.3.1.3 EXECUTE MEMORY

A program may be executed by typing the execution address and a C/G. No characters should intervene between the number and the Control-G.

##### 9.3.1.4 INVOKE SDOS

The full powers of the Disk Operating System are brought to force by reading in the resident portion of SDOS from disk. When C/F is entered that portion required to access the disk's files is read in and control is passed to it. If the resident is present but has lost control to an application program, control can be returned by manually resetting the system and Executing Memory at location 100. This does not read in the resident again, just begins its execution.

#### 9.3.2 SDOS RESIDENT EXECUTIVE

The disk operating system executive handles the commands that may be considered the utilities of the disk system. The following sections give the specifics of the commands in SDOS.

## 9 SYSTEM SOFTWARE

### 9.3 SPHERE DISK OPERATING SYSTEM

#### 9.3.2 SDOS RESIDENT EXECUTIVE

##### 9.3.2.1 ASSEMBLE

An,m,p<sup>CR</sup>

This command specifies execution of a Motorola type assembler with file number 'n' as source input, file 'm' as object output and assembled by parameter 'p' as follows: 2=object only, 3=pass II list only, 4 both object and pass II listing.

##### 9.3.2.2 COPY DISK

C

Copy the contents of disk drive unit 0 to unit 1. Prior to this command a Home command should be issued. This process takes approximately seven minutes as the whole disk will be copied.

##### 9.3.2.3 EDITOR

En,m<sup>CR</sup>

This command passes control to the Editor and specifies file 'n' as input and file 'm' as output.

##### 9.3.2.4 HOME

Hu<sup>CR</sup>

The Home head command causes the head on the disk drive 'u' to return to its reset or home position.

##### 9.3.2.5 INITIALIZE

Iu<sup>CR</sup>

The initialize command is used to cause the user file directory on drive 'u' to be cleared of all files.

##### 9.3.2.6 LIST

Lu<sup>CR</sup>

The list directory command causes the seven directory entries to be listed. The entries show file number, file name, and used space.

## 9 SYSTEM SOFTWARE

### 9.3 SPHERE DISK OPERATING SYSTEM

#### 9.3.2 SDOS RESIDENT EXECUTIVE

##### 9.3.2.7 RETURN TO MONITOR

M

The 'M' command is used to return control to the Debug supervisor. Note that a CR is not necessary.

##### 9.3.2.8 NAME

Nm,xxxxxxxxxCR

The file name command allows the user to name a new file or change the name on an old file. The file name can be any alphanumeric character calling space, 1 to 10 characters.

##### 9.3.2.9 PRINT

PnCR

The Print command will allow file 'n' to be dumped to the CRT screen.

##### 9.3.2.10 RUN

RnCR

The run command causes file 'n' to be loaded but not executed. To begin execution the user exits the resident and executes the loaded program with Debug's **Execute Memory**.

##### 9.3.2.11 TRANSFER

Tn,mCR

To transfer or append the contents of file 'n' to file 'm' this command is used.

#### 9.3.3 ASSEMBLER

The assembler is invoked with the SDOS command An,m,p as explained in section 9.3.2.1. Source programs are usually written with the EDITOR and then are assembled. Source programs may contain any of the 72 executable instructions explained in sections 6 and 7 of this manula and any of the assembly directives which are covered in Figure 9.3. Characters recognized by the assembler are the alphabetic characters A-Z numeric characters 0-9, and arithmetic operators

9 SYSTEM SOFTWARE  
 9.3 SPHERE DISK OPERATING SYSTEM  
 9.3.3 ASSEMBLER

END	<u>End</u> of Program
EQU	<u>Equate</u> a value to a symbol
FCB	Form a <u>Constant Byte</u> of Data. One or more operands separated by commas, each operand produces one byte of data.
FCC	Form <u>Constant Character Bytes</u> produces 7-bit ASCII codes 20 <sub>x</sub> through 5F <sub>x</sub> . May be in the format of <u>Count</u> , <u>Comma</u> , <u>Text</u> ; 9,TEXT <del>0000</del> ; or <u>delimiter</u> , <u>text</u> , <u>delimiter</u> ; <del>TEXT</del> or 'TEXT'.
FDB	Form <u>Double Constant Byte</u> One or more operands separated by commas, each operand produces two byte of data.
NAM	<u>Name</u> defines a name for the program listing.
OPT	<u>Option</u> Allows the user to control the type of output generated. Options include <u>List*</u> , <u>Short List</u> , <u>Nolist</u> , <u>Symbol table*</u> , <u>No Symbol</u> , <u>Generate full code of FCC's*</u> , <u>No Generate</u> , <u>Error list*</u> , <u>Short Error list</u> , <u>No Error</u> , <u>Page*</u> , <u>No Page</u> separations, <u>Tab*</u> , <u>No Tab</u> suppresses horizontal formatting, <u>Display Base 8</u> , <u>Display Base 10</u> , <u>Display Base 16*</u> , <u>Mem</u> saves object, <u>No Mem*</u> . *=default for most systems, may be altered.
ORG	<u>Origin</u> defines origin of a program segment.
PAGE	<u>Page</u> advance to top of next page.
RMB	<u>Reserve Memory Bytes</u> advances program counter by value of the operand field.
SPC	<u>Space lines</u> advances listing by the number of lines specified in the operand field.

ASSEMBLER DIRECTIVES

FIGURE 9.3

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9.3 SPHERE DISK OPERATING SYSTEM  
9.3.3 ASSEMBLER

# (Pound Sign) specifies the immediate mode of addressing.  
\$ (Dollar Sign) specifies a hexadecimal number  
@ (at symbol) specifies an octal number  
% (percent) specifies a binary number  
' (apostrophe) specifies an ASCII literal character  
, (comma) separator within a field parameter  
CR (carriage return) end of line character.

FIGURE 9.4  
Special Characters used by the Assembler



## 9 SYSTEM SOFTWARE

### 9.3 SPHERE DISK OPERATING SYSTEM

#### 9.3.3 ASSEMBLER cont'd

+, -, /, \*. Also recognized for special purposes are the characters in Figures 9.4. Label fields must begin in column 1 and all fields must be separated by at least one space. Labels must not be the single characters A, B, or X as they are reserved for the register designations. Operand field expressions are evaluated from left to right without parenthetical grouping and with no hierarchy of precedence of operators. All arithmetic will be integer. Comments can follow the operand field when separated by one or more spaces. The whole line can be used as a comment if the first position of the line is an asterisk.

#### 9.3.4 EDITOR

The SDOS Editor is a cursor based editor which allows the user to enter and modify text and source for later assembly or other processing. The Editor is called and executed by the SDOS Command En, m CR. Any number of commands can be entered and they will be executed in order, left to right. Input is ended with double ESC character.

##### 9.3.4.1 APPEND

A

Append inputs about 50 lines of text from the input device to the edit buffer.

##### 9.3.4.2 BEGINNING

B

Moves the cursor to the beginning of the edit buffer.

##### 9.3.4.3 CHANGE

Cstring1 ESC string2

Replaces the first occurrence of "string1" with "string2"  
Cursor is left at the end of the second string. Terminate  
string2 with a single ESC if more commands follow.

##### 9.3.4.4 DELETE

nD

Deletes 'n' characters either forward (+) or backward (-) from cursor. Cursor is always considered between characters.

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9.3 SPHERE DISK OPERATING SYSTEM

9.3.4 SDOS RESIDENT EXECUTIVE

9.3.4.5 END

E

Terminates the edit operation by writing the contents of the edit buffer to the output device and copying the rest of the file to the output device.

9.3.4.6 INSERT

Istring

Inserts characters or lines into the edit buffer after the cursor. Terminate string with an ESC if other commands follow. String **may** contain any valid characters except ESC.

9.3.4.7 KILL LINES

nK

Deletes 'n' lines from the edit buffer from the beginning of the line the cursor is in.

9.3.4.8 LINE

nL

Moves the cursor backward (-) or forward (+) 'n' lines from the beginning of the present line.  $\emptyset$ L moves the cursor to the beginning of the current line.

9.3.4.9 MOVE

nM

Moves the cursor backward (-) or forward (+) 'n' characters.

9.3.4.10 PUT

nP

Puts 'n' lines of text to the output device.

9.3.4.11 SEARCH

Sstring

Searches the **buffer** from the cursor for the first occurrence of "string". Places the cursor after the string if it is found or leaves it undisturbed if not found.

9 SYSTEM SOFTWARE

9.3 SPHERE DISK OPERATING SYSTEM

9.3.2 SDOS RESIDENT EXECUTIVE

9.3.4.12 DISPLAY

nT

Displays 'n' lines from cursor forward (+) or from '-n' lines back forward to the cursor.

9.3.4.13 END

Z

Moves cursor to end of edit buffer.

9.4 SPHERE BASIC

This section will be provided when the final version of Basic is ready in the Fall of 1976.

The SPHERE basic computer system consists of:

1. MOTOROLA MC6800 MICROPROCESSING UNIT with control logic.
2. 1,024 8 bit words of Reprogrammable Read only Memory Preprogrammed with the Micro Editor, Assembler, debugger, load & dump routines and the Mini-Executive
3. 4,096 8 bit words of Dynamic Random Access Memory
4. ASCII Keyboard for inputting data
5. TV (or CRT) Driver logic for output display of data (TV not supplied with kits)
6. Peripheral Interface Adapter to allow user to interface his own I/O device (s).
7. Power supply, which supplies power to all components of system.

### 10.1

#### BUS STRUCTURE

The System Bus provides the address, control, and bi-directional data lines between the CPU and the peripherals via three separate flat ribbon cables and 14 pin dual-in-line connectors. These cables are carried from one device to another in a common bus fashion. All peripheral devices are tied onto the bus in parallel and constantly monitor the address lines. If a device detects its own unique address, it responds as required, depending upon whether the data transfer is a read or write function. Each signal is driven from the CPU through Tri-State buffers. This technique of a common bus I/O structure makes it possible to connect many devices to the bus and makes interfacing requirements simpler. The signals that make up the System Bus are described under the CPU description.

### 10.2

#### THEORY OF OPERATION

The only thing any computer can do, from the largest to the smallest, is transfer data from one place to another. During transfer, however, the data can be altered or manipulated in various ways by the CPU, such as adding two peices of data together and transferring the results to a device such as memory.

10 SPHERE BASIC SYSTEM  
10.2 THEORY OF OPERATION cont'd

This function of transferring of data is done under program control to accomplish a given task. In addition, the CPU is capable of making logical decisions based on results of tests performed on data and altering the program sequence or flow accordingly. The computer cannot think for itself - it performs sequences of "instructions" that it understands and can act upon which have been stored in memory in the form of a functional program. The program counter is the register the CPU uses to determine which instructions to perform - it "points" (or provides the address) to the next instruction to be executed in memory.

A typical sequence to perform an Addition of two number is as follows:

LDA A  
ADD A  
STA A

1. The CPU sends an address out on the address bus along with a read on the control bus. The memory responds by sending an 8 bit operation code to the CPU which saves this data in the Instruction Register. At this time the Program Counter is incremented by one. It is in the Instruction Register that the 8 bits of data are decoded into commands the CPU can understand. In our example a  $96_x$  was placed into the Instruction Register and decodes to a "Load Accumulator A Direct" from low memory. Since "low memory" describes 256 different locations, something needs to indicate which location. The  $96_x$  tells the CPU to read the memory location which follows the operation code for an absolute address. The memory responds with  $C1_x$  which the CPU saves in the lower byte of Data Address Register. The Program Counter would be incremented again since one more byte of the program had been fetched. Now that the CPU has the actual data address, that address and another read command can be put onto the buses. The memory will respond with the contents of location  $00C1_x$  which might be a  $23_x$ . This data is put by the CPU into the A Accumulator. To execute a LDA A direct from  $C1_x$  the CPU took 3 cycles.

2. Now that the LDA A is complete the CPU goes back to the Instruction Fetch mode. The Program Counter is placed on the address lines and a read is performed. The data read,  $8B_x$ , is placed into the Instruction Register to be decoded. The CPU recognize the op code as a ADD A immediate instruction. Immediate means that the operand follows the op code and is not elsewhere like the LDA A above. The CPU

## 10 SPHERE BASIC SYSTEM

### 10.2 THEORY OF OPERATION cont'd

puts the updated Program Counter back on the address bus and again request a read from the device recognizing the address as being itself. The memory responds with the data,  $C4_x$  which the CPU adds to the A accumulator. The Program Counter is again incremented and the instruction is completed, taking 2 CPU cycles.

3. Now in accumulator A is the sum of the contents of memory location  $C1_x$ , which was  $23_x$ , and  $C4_x$  or  $E7_x$ . The Program Counter now points to the next instruction's op code, which is fetched by the CPU. The instruction decode logic recognizes  $B7_x$  as a STA A extended op code and now must get the extended address of where to store accumulator A. The CPU again places the PC onto the address bus, asks for a read and gates, or directs the incoming data bus to the high order byte of the Data Address Register. The Program Counter is advanced and another fetch is performed to the low order byte of the Data Address Register. The Program Counter is advanced again after the second address fetch so that at the end of this instruction it will point to the next instructions' Operation Code. The Data Address Register would now be connected to the system address bus, the A accumulator connected to the data bus and a write command given on the control bus. The data in Accumulator A is thus copied to the location whose address followed the Operation Code.

Note that the CPU only did three instructions and that while it takes a human seconds to read the written instructions which left out many details, the CPU took only 15/1,000,000 second to do it. All the CPU did was to transfer two operands from memory, add them together and then store the result back in memory. If the result of the addition was zero, or a negative number, or the result of the addition was a number too large to fit in the 8 bit accumulator (overflow), then the program could have tested the condition code register for these and altered the program sequence accordingly. The computer can only do what it is told, in a sequential fashion, but does it at such high speeds compared to a human, that it becomes a tremendously valuable tool.

#### 10.2.1 CRT/1

The CRT control module stores data received from the CPU in a 512 word static RAM, arranged as a 16 line by 32 word buffer. The CRT buffer memory can be accessed from the CPU or by the address generators  $E6$ , 10, 11, 22 on the CRT board when the screen is being updated.  $E3$ , 4, 5 determine whether the CPU address lines or the CRT generated addresses will be supplied to the buffer. This is done via the CPU address

## 10 SPHERE BASIC SYSTEM

### 10.2 THEORY OF OPERATION

#### 10.2.1 CRT/1 cont'd

decode logic and the resultant "CPU SELECTED" signal. (i.e., the buffer is a psuedo dual-part memory; either the CPU is accessing it or the CRT update circuitry.) Since the buffer looks like memory to the CPU, it can be written into or read out of. The data transfer direction is determined by the R/W control line.

The Video display format is comprised of 16 lines containing 32 characters each. Each character is made up of 35 dots in a 5 x 7 arrangement with 5 horizontal and 7 vertical dots. A character generator (2513) decodes the ASCII data provided into the correct dot pattern for the character being displayed. Horizontal spacing of characters is accomplished by displaying a blank dot column between each character. Vertical spacing is accomplished by sweeping three blank video lines between each character. The first line A B C D  $\emptyset$  is generated by having the row select of the character generator then as the row counter counts off Rows 1 thru 7, Rows 1 thru 7 of the character are decoded and processed but when E22-11 sees the 8 and 9 counts of the row counter through E27-3 its output goes low thus enabling the video blanking circuitry which places all zeros on the row select of the character generator creating the other two blank lines.

Along with video information a vertical and horizontal Sync must be supplied.

Oscillator E29 initiates the horizontal Sync pulse which is fed thru inverter E16 to E24 pins 5 and 10 where a 4- $\mu$ s horizontal Sync pulse is generated. The pulse goes to E12-5 where it is wire or'ed with the vertical Sync pulse.

The falling edge of the Sync pulse on E24-8 triggers E31 a one shot, which puts out a positive pulse on pin 13 that is adjustable by R19 from 4 to 20 $\mu$ s. A delay pulse causes a lag between the beginning of a video sweep and the generation of characters, giving an adjustable left hand margin.  $\bar{Q}$  of E31-4 inhibits dot oscillator E31-12 through AND - OR - INVERT gate E28. E31-13 resets E6 and E11, the 16 - bit counters that keep track of the selected horizontal character. Since we are starting a new line, we must clear the counter to prepare it for incoming data. At the end of a negative going pulse on E31-4 the row counter, E22, is incremented and in the case of a ripple carry, E10, the line counter is incremented as well.

Keeping track of the 10 rows of horizontal lines forming each character is the job of E22, a decade counter which has a unique BCD output for each seven rows of dots and three blank rows used for painting a character and supplying vertical spacing.

A 4 bit counter, E10, keeps track of the 16 sets of ten row lines. Together E22 and E10 provide a distinct BCD code for each of the 10 x 16 video scan lines. A complete video frame contains around 262 lines.

10 SPHERE BASIC SYSTEM  
10.2 THEORY OF OPERATION  
10.2.1 CRT/1 cont'd

Since the scan line counter E22 and E10 can only count to 160 it is allowed to run for another cycle. E23 has been in the high state during the last 160 scan lines and is now toggled via and gate E27-8 and NAND gates E24-11 and E18-8. The video blanking circuit for the character generator is activated when E23-9 (Q) is toggled low and forces the generation of blanks from the character generator.

This continues until the line counter gets to 40. Lines 40 through 50 are then used to generate the vertical Sync. NAND gate E18 along with inverters E16 pins 8, 10 and 12 perform the actual line number decoding. The out put of the horizontal oscillator is NAND'ed as well in E18-6 with the line counter data, this chops the vertical Sync signal required by the video monitor. The output at E18-6 is fed to E12-4 where it is joined with the horizontal Sync to form the composit Sync signal at the output of ANDgate E12-6. At line 50 the vertical Sync generation is stopped and the line and row counters continue their count to 104 which is decoded by E18-3. The  $\bar{Q}$  output of E23 is NAND'ed by the decoder E18, since the 102 count is not significant when in the "display dot video" mode.

The output of E18-8 in turn generates a positive clock pulse to E27 via ANDgate E23 making the Q output of E27 high again as it was in the beginning. The same signal from the output of E18-8 resets row counter E22 and line counter E10 to 0 thus completing 262 lines required for the raster. Again briefly the 264 lines required for a full video frame are generated as follows. 160 lines of video, 40 lines of blanking, 10 lines of vertical Sync and 54 more lines of blanking.

Resistor R20 dictates the cycle time for oscillator E31-12 between 150 and 300us which in turn determine the width of the characters. The "Dot Clock" is not the output of E31-12, but rather the output of AND - OR - INVERT gate E28. Its output is normally high but goes low for about 30 $\mu$ s each time E31 pin 12 resets. The 30 $\mu$ s pulse time is determined by the propagation time of E28 and E31. The "Dot Clock" is used to toggle shift registers E9 and E21.

The horizontal data for each character is made up of five dots and one blank for horizontal spacing on each video line. The video data for the horizontal portion of each character is parallel loaded from the character generator into 4-bit shift registers E9 and E21 with zero, bit 1, bit 2 and bit 3 going into E9. Bit 4, bit 5, zero and a one going into E21.

The serial input of E21 is tied high to load one's into the shift register to replace the character data as it is shifted out of the register bit by bit. E15 monitors the parallel output of the dot register and goes low when six bits have been clocked out, it detects the ones that have been shifted into the register. A low transition



10 SPHERE BASIC SYSTEM  
10.2 THEORY OF OPERATION  
10.2.1 CRT/1 cont'd

on the output of E15 is inverted by E17-4 and changes the dot register from a shift up to a parallel load data mode. This same pulse also increments the character counters E6 and E11. Each time pin 6 goes high and the dot register is set up to parallel load new data, E11 is incremented thus keeping track of which of the 32 horizontal character positions we are working with.. As dot data is shifted out bit by bit, on pin 10 of E9 at a rate set by the dot clock, it then goes to E12 pins 12 and 13 where it is mixed with the horizontal and vertical Sync pulses to form the composite video signal which is buffered by Emitter follower Q1 and fed to the video monitor.

10.2.2 KBD/2

The keyboard converts keyswitch depressions to ASCII character codes to be used as an 8-bit input device. The keys are wired in a matrix array of 8 columns by 16 rows. The array is scanned until a key is depressed closing the circuit between the 8 columns and the 16 rows.

The scanning clock is generated by E6b and the associated R/C network and is halted as long as a key is depressed or the debounce circuit E6a is running. 1.6ms after the key has been depressed, long enough for any key bounce to end, and if the key is still depressed E12 will signal character present on x20-12. The clock is fed to the input of E1, a 4-bit binary counter, which will generate as its output the row address. The high order bit of the row address, E1-11 is also used as the input of E5, another 4-bit counter, of which the low 3-bits make up the column address. The column address is decoded by E4 into 8 separate columns which are then driven by 7407 open collector drivers. Only the column selected is pulled to ground by the 7407 on that column, all others are left high. The pull-up resistors are on each row and provide a high to the 16 inputs of the row selector E3. The selected input to E3, as addressed by E1, is provided on the output, E3-10, to the debounce and clock circuits. When a key is depressed, chances are it is not at the location of the matrix currently selected, so the clock continues to run. The rows will be checked, the column incremented, and the rows checked again until the correct column and row addresses locate a closed switch, a connection which causes the pull-up resistor R1-R16 associated with the row of the switch to be pulled down through the 7407 of the selected column. E3-10 will go high, stopping the clock and beginning the debounce time.

When the device reading the keyboard sees a high going pulse it reads the data lines which are the addresses of the column and row decoders, D0-D3 from the row address, D4-D6 the column address.

10 SPHERE BASIC SYSTEM  
10.2 THEORY OF OPERATION  
10.2.2 KBD/2 cont'd

D4 is modified by a combination of Shift, Row 2, Row 3, Column 0 and the A column address line such that the numeric characters 1-9 and the special characters ; : = ? will produce other special characters when shifted. D5 is modified such that when shift is pushed or column address C is high and the control key is pressed, D5 is low, D6 is modified so that D6 is low when either column address C is low or the control key is pressed. If the modification for FULL ASCII to MODIFIED ASCII is made all alphabetic characters are shifted to upper case automatically and shift lower when the shift is pushed (when column address C is high, column address B to the above mentioned D5 logic is inverted).

The reset keys are wired in series and when pressed together cause the RESET line to be pulled low. The repeat key simply causes the D7 output line to be raised and can be used as a repeat function under software control.

The outputs provided at X20 are plugged to X4 of the CPU board and power is obtained from the CPU's X4.

10.2.3 CPU/2

There are four classes of control signals which control the execution of the MC 6800 CPU. The first pair of control signals are the two phase clocks,  $\phi 1$  and  $\phi 2$  which provide the basic timing to the system. The second pair of signals, HALT and BUS AVAILABLE (BA) are used to stop program execution and free up the address and data bus for other uses. The interrupt signals make the CPU responsive to outside control and are listed in decreasing order of interrupt priority: RESET, NON-MASKABLE INTERRUPT (NMI), and MASKABLE INTERRUPT (IRQ). An interrupt can be generated by a Software interrupt instruction internally. The three state control (TSC) and DATA BUS ENABLE (DBE) control lines provide a way to momentarily remove the CPU from busses. The TSC line is not used in the basic SPHERE system. The SPHERE system uses INTEL 2107 A-8 or equivalent dynamic RAM's (Random Access Memory) for main memory. These are 4069 X 1 bit N-channel MOS chips. 8 of these chips are arranged into a 4K X 8 bit main memory. Extended memory is done by implementing additional 4K blocks of RAM chips. The 1702A Programmable Read Only Memorys are 256 X 8 bit chips with 4 chips making up the total 1024 X 8 bit memory. These chips contain the standard system software programmed into them but can be erased and reprogrammed. Two 9602 retriggerable one-shots (E45) and the MPQ6842 (E51) clock buffer generate

10 SPHERE BASIC SYSTEM  
10.2 THEORY OF OPERATION  
10.2.3 CPU/2 cont'd

the basic clocks,  $\phi 1$  and  $\phi 2$  to the system. The clocks are free running and the RC time constants (R11, R12, C22, C23) were chosen to provide a basic cycle time of 1.50 usec. The two clocks are non-overlapping, meaning that  $\phi 1$  is low before  $\phi 2$  goes high and conversely,  $\phi 2$  goes low before  $\phi 1$  goes high again. This insures that adequate time is provided during  $\phi 2$  for memories to sense the written data. Due to the capacitive storage design of the dynamic RAM's, they must be refreshed every 2 msec or data will be lost. E8 is a free running clock providing the timing for the refresh cycle (2msec). When #9 sets, this generates REFRESH which enables the address counters E22, 27 and address line drivers E21 and halts the CPU. Bus Available goes high after completing the current instruction, disabling the CPU address buffers, E44, 47, 48 and enables  $\phi 1$  clock to refresh address counters (generator). On the next  $\phi 1$  after the CPU has halted,  $\phi 1$  begins clocking the refresh address generator, which is a simple up-counter.

As it counts, the addresses are supplied on the bus, which are the RAM memory 'Row' addresses necessary for refreshing. On count 64, the counter resets REFRESH, HALT and Address counters. The CPU then proceeds to perform the next instruction in sequence after it halted. The circuitry comprising E37, E38, and E23 insure that the RAM's get refreshed even if the CPU should be halted or should hang up on a bad instruction, etc. E42, E43 are Bi-directional data line buffers and the direction is determined by the Read/Write line. If the CPU is doing a LOAD instruction for example, this is a READ from some peripheral to the CPU, so the R/W line is a high. This configures the buffers for a data transfer to the CPU. A WRITE, such as a STORE instruction does the opposite. Any instruction that addresses the dynamic RAM ( $\phi 000$  thru  $\phi FFF$ ) is detected by address decode gate E24 and generates CHIP SELECT (CS) and CHIP ENABLE (CE), via E28 and transistor Q1. CE is also generated by REFRESH. E37 insures during a Write cycle to memory that there is at least a 200 nsec delay between CHIP ENABLE and WRITE ENABLE (WE). Chips E2, 5, 11, 17, 19, 26, 34, and 36 constitute the 4,096 X 8 bits per word RAM. E1, 33 are tri-state buffers and are active when reading data from memory. They are enabled by CS. When writing to memory, these buffers are disabled (put in high-impedance or disconnect mode) and data is transferred directly to memory. Gates E4, 10, 16, 32 and E13 select one of the four-256 x 8 ROM chips. The addresses begin at FC00 and extend to FFFF. The address bits A0 to A7 then select 1 of the 256 words to be read. These are read-only device's and contain the system software (Assembler, Editor, etc.) The ROM's can be reprogrammed but only with special equipment. E18 also supplies chip selects to the Peripheral Interface Adapter E3. The total decoding is F040 to F043. E3 is used for I/O to the teletype-writer interface on the SPHERE 300 series one card computer and for keyboard input on the 310-340 systems. Also the real time clock uses E3.

## 10 SPHERE BASIC SYSTEM

### 10.2 THEORY OF OPERATION

#### 10.2.3 CPU/2 cont'd

When the CPU/2 board is used as the One Card Computer, the three signals on the right side of the board provide a 20 am current loop to connect directly to a teletype common, Transmit, and Receive wires. Also available are RS232c interfaces. In this mode the 512 Bytes of ROM perform the teletype I/O routine as well as a Debug mode. The jumper on PB0 and PB7 may be omitted and 19 digital I/O lines will be available for dedicated use by the customer's own ROM's (up to 1K Bytes.) When using the teletype I/O routines the CPU clock must be set up at 1.50 usec  $\pm$  2% in order to interface with the required 110 BAUD rate of the standard teletypes.

The real time clock is also on the CPU/2 board. E7 counts refresh pulses to establish a series of real time interrupts. The P.C. board has dotted lines showing the various frequencies that may be selected. The real time clock counter can be reset by putting F044 (HEX) on the address lines. Also a system reset will reset the clock. The clock interrupts enter the E3 PIA (F041) on CA-1 (pin 40) and can be used through that PIA device as a CPU real time interrupt. The PIA may be programmed to interrupt or ignore the clock.

#### 10.2.4 ROM/1

The Read Only Memory Board consists of two sections of logic, the first provides those elements common to the second, address buffering, data gating and power control. The second set of logic is repeated four times and contains the necessary address select logic for the four 1702's in its bank.

Address lines A0-A7 are buffered and isolated from the address bus by E3 and E4, while A8 and A9 are buffered by two of the four bus driver gates of E7 that are not used for data gating. A10 through A15 are inverted and buffered by two 7404 gates each in E1 and E2 to provide the necessary signals for address selection. The bank selects from the four banks are OR'd together in E5a and AND'd together with R/W, VMA, and 02 to produce the board select line which enables the 8097 tri-state bus drivers E6 and 2/6 E7. Diodes D1-D4 drop the -12v from X6-5,12 to -9v.

The address select for the bank is provided by the jumpers at J1-J4. The combined A10-A15 true and inverted signals are AND'd by E13, E19, E25, E31 and provide the BANK SELECT A through D signals. The BANK SELECT also feeds the C and D inputs of E8, E14, E20, E26 which along with A8 and A9 (A and B inputs) the binary to

10 SPHERE BASIC SYSTEM  
10.2 THEORY OF OPERATION  
10.2.4 ROM/1 cont'd

BCD 7442 provides outputs to select one 1702 in E9, E10, E11, or E12 (or E15-18, E21-24 or E27-30). Address lines A0-A7 are bused to all 1702's from E3 and E4. And D0-D7 is bused from all 1702's to E6 and E7.

Resistors R1 through R24 provide pullup and logic conversion between TTL and CMOS. Once a bank of 1702's is selected the selection of which 1702 is from right to left (away from the address select logic to near the address select logic). The address select logic for each bank of 1702's consists of 3 row of holes; the one nearest E1 is 7 holes and is Address true. The next row, Address inverted, is 12 holes, three extra on the left and two on the right (DO NOT USE THESE HOLES) the address bits for the bank select logic is the third row, 6 holes. Bit A15 is the left most hole, bit A10 is the right most hole of the address select row. In some banks an extra feed-through may have been required, DO not mistake this for an address hole.

10.2.5 SIM/1

The serial Interface module is built around two ACIA (Asynchronous communications Interface Adaptor) chips. The board is segregated into 9 main areas: Board decoding, cassette interface number 1, cassette interface number2, ROM, Baud rate generators, Teletype interface, RS232 interface, TTL direct interface, and modem. The basic board just decodes the address lines to allow selection of the PROM, ACIA number1, or ACIA number2.

BOARD DECODING

Three strapable addresses are provided on the board. As initially set ACIA port number 1 is located at F050 & F051. The second port is located at F060/1 (hex). If a second SIM/1 board is added to the system, A1 on the second board would be cut and a jumper placed along the dotted lines by the A1 etch. The addresses on this board will then be F052/3 and F062/3. The PROM will always be located at FB00 to FBFF on all boards. Hence do not put a PROM in the socket on any added boards after the first one. A third board can be added by changing the jumper at A2 instead of A1. This will give another set of unique ACIA ports for control. Table 10.1 shows the configuration of the 8 boards that could be independantly addressed. The A0 address line determines which of the two registers in the ACIA is being selected. When A0 is high the transmit/receive data register is selected.

10 SPHERE BASIC SYSTEM  
 10.2 THEORY OF OPERATION  
 10.2.5 SIM/1 cont'd

A1	A2	A3	ACIA No.1 Address		ACIA No.2 Address	
			Logical	Physical	Logical	Physical
-	-	-	0	F050/1	1	F060/1
X	-	-	2	F052/3	3	F062/3
-	X	-	4	F054/5	5	F064/5
X	X	-	6	F056/7	7	F066/7
-	-	X	8	F058/9	9	F068/9
X	-	X	A	F05A/B	B	F06A/B
-	X	X	C	F05C/D	D	F06C/D
X	X	X	E	F05E/F	F	F06E/F

X= Jumper added and etch cut.

TABLE 10.1

CASSETTE INTERFACES

There are two identical cassette interface circuits in the center section of the SIM/1 board. One is controlled through ACIA 1 and the other through ACIA No.2 (F060). The theory of operation has been fully explained in such publications as BYTE (see the Bit Buffer P.30 March, 76). In summary: the audio cassette input sine wave is squared by the 311 comparators. If it is a long pulse, a one shot has time to fire providing an extra 2 clock pulses and indicating a long pulse received. A short pulse (1/2 of a long pulse) one shot reset and each edge provides a clock pulse. Hence a simulated clock frequency is generated and the 1's and 0's are recaptured. The trimpot allows setting the trigger level to the 4001 IC to compare the long to short ratio actually present, thus audio cassette player speed variations can be tuned out. The output data is fed to the 4018 (counter) through two clocked gates. The resulting outputs are summed through different resistors to provide a symmetrical step function looking like a sine wave. Further RC networks smooth out the signal and an output transistor provides ample drive to the cassette recorder. The long and short digital pulses now look like two frequencies of about 1200 Hz and 2400 Hz. F38 is a free running multivibrator that provides the 300 baud rate for both cassette clocks. This frequency is fed into the ACIA clock input when used as a cassette port. The ACIA should be set for 16X rate. Each cassette has a relay (K1 and K2) provided to allow the cassette drive to be turned on or off when the CPU calls the ACIA port 0 for example, K1 will be energized by  $\overline{RTS}$  going low and the 7407 buffer pulling current through the coil of K1. The normally open contact now closes. If the relay contacts have been plugged into the remote terminal on a cassette recorder, the cassette drive is turned on. The software in the PROM will not send valid data until after a long enough delay for the cassette drive to get up to speed. In the event the cassette recorder does NOT have a remote on/off plug, a 12 volt coil relay may be used to switch the 110VAC line. A separate output through R13 for cassette 1 and R14 for cassette 2, (optional current limiting resistors) will be tied to the top of the coil in the new relay and the bottom of the coil will be tied to the normally open line of K1 (K2). The common will be jumpered to ground (or -12 if a 24 volt coil is used). Hence the SIM/1 board provides the coil power to drive a larger relay for direct switching of 110VAC lines. Since these relays always respond when the respective ACIA is called, they can be used to turn on/off teletypes or any other relay or device desired.

10 SPHERE BASIC SYSTEM  
10.2 THEORY OF OPERATION  
10.2.5 SIM/1 cont'd

PROM

Whenever the 16 address lines from the CPU board contain FF:xx in Hex, the ROM will be addressed. This read only memory chip contains logic to enable reading and writing to the cassette tapes. See listing of the contents of the ROM for details of the software operations.

BAUD RATE GENERATORS

The SIM/1 Board has a series of straps for selection of desired baud rates. It is prewired to 300 baud but this strap maybe cut and standard frequency from 150 to 9600 may be used. A trimming resistor (R74) may be added to compensate for the 90% tree running one shot being off frequency. If the 110 baud rate is desired for a teletype, the 150 line must be selected AND C47 (a 33 pf cap.) must be strapped in the place labeled TTY. This will slow the main clock down to within a range that R74 can be selected to yield a precise 110 baud rate. Usually R74 is about 120K  $\Omega$ . External frequencies may be added through X1 pins 8 & 9 when the 625 KHz (150 baud rate multiplies) and the 455KHz (110 baud rate) jumpers on the lower left sector of the board are added.

TELETYPE INTERFACE

With the input clock to the No. 1 ACIA set at 110 baud rate (see baud rate generator), the output data will be correctly formatted by the ACIA if the 64x mode is selected by software. Two 4N33 photo couplers are used to isolate the teletype + 12 volt, 20 ma current loops from the + 5 volt TTL logic. When using the teletype interface, the RS232 and TTL jumpers must be put in and the 20 ma jumper left out. Also set up the baud rate generator and ACIA jumpers per the assembly instructions.

RS232 INTERFACE

Any desired input baud rate can be selected. The TTL and 20 ma jumpers must be put in place. E5 and E13 are standard RS232 driver/receivers. Except for the baud rate selection the operation is like the teletype. An RS232 line has more drive capability than either TTL or 20 ma current loops. The voltage swings are + 12 volts.

TTL DIRECT

This interface allows high speed data transfers over short direct wire connections. The ACIA can be initialized to 1x, 16x, or 64x. The baud rate can be any selected value. The 20 ma and RS232 jumpers must be put in. The voltage swings will be +5 volts compatible with any other TTL/DTL input. The driver is a 7494 with 10 TTL loads maximum.

MODEM

The modem section is built around the 6860 modem chip and the 6850 ACIA. See the M6800 microprocessor applications manual for details. In addition two filter sections are included making full single wire communications possible. Jumpers are provided on the board to select single wire full duplex. See assembly instructions.

A CONVERSION TABLES

A.1 HEXADECIMAL AND DECIMAL CONVERSION

HOW TO USE THE TABLES

CONVERSION TO DECIMAL: Find the decimal value for corresponding hexadecimal value for each hexadecimal character. The sum of the decimal values is the decimal value of the hexadecimal number.

CONVERSION TO HEXADECIMAL: Find the highest decimal value in the table which is lower than or equal to the decimal number to be converted. Add the corresponding hexadecimal value to the previous hexadecimal sum. Subtract the decimal value found from the decimal number to be converted. With the difference repeat the process to find subsequent hexadecimal values.

HEXADECIMAL AND DECIMAL CONVERSION

BYTE		BYTE					
HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC
0000	0	000	0	00	0	0	0
1000	4096	100	256	10	16	1	1
2000	8192	200	512	20	32	2	2
3000	12288	300	768	30	48	3	3
4000	16384	400	1024	40	64	4	4
5000	20480	500	1280	50	80	5	5
6000	24576	600	1536	60	96	6	6
7000	28672	700	1792	70	112	7	7
8000	32768	800	2048	80	128	8	8
9000	36864	900	2304	90	144	9	9
A000	40960	A00	2560	A0	160	A	10
B000	45056	B00	2816	B0	176	B	11
C000	49152	C00	3072	C0	192	C	12
D000	53248	D00	3328	D0	208	D	13
E000	57344	E00	3584	E0	224	E	14
F000	61440	F00	3840	F0	240	F	15



A CONVERSION TABLES

A.2 POWERS

	<u>2</u>	<u>8</u>	<u>10</u>	<u>16</u>
0	1	1	1	16
1	2	8	10	256
2	4	64	100	4096
3	8	512	1000	65,536
4	16	4096	10,000	1,046,576
5	32	32,768	100,000	
6	64	262,144	1,000,000	
7	128			
8	256			
9	512			
10	1024			
11	2048			
12	4096			
13	8192			
14	16,384			
15	32,768			
16	65,536			
17	131,072			
18	262,144			
19	524,288			
20	1,048,576			

B ASCII CHARACTER SET

HEX	DEC	OCT	BINARY	CHARACTER	DESCRIPTION
00	0	000	00000000	NUL	Null
01	1	001	00000001	SOH	Start of Heading
02	2	002	00000010	STX	Start of Text
03	3	003	00000011	ETX	End of Text
04	4	004	00000100	EOT	End of Transmission
05	5	005	00000101	ENQ	Enquiry
06	6	006	00000110	ACK	Acknowledge
07	7	007	00000111	BEL	Bell
08	8	010	00001000	BS	Back Space
09	9	011	00001001	HT	Horizontal Tab
0A	10	012	00001010	LF	Line Feed
0B	11	013	00001011	VT	Vertical Tab
0C	12	014	00001100	FF	Form Feed
0D	13	015	00001101	CR	Carriage Return
0E	14	016	00001110	SO	Shift Out
0F	15	017	00001111	SI	Shift In
10	16	020	00010000	DLE	Data Link Escape
11	17	021	00010001	DC1	Device Control 1
12	18	022	00010010	DC2	Device Control 2
13	19	023	00010011	DC3	Device Control 3
14	20	024	00010100	DC4	Device Control 4
15	21	025	00010101	NAK	Negative Acknowledge
16	22	026	00010110	SYN	Synchronize
17	23	027	00010111	ETB	End of Transmission Block
18	24	030	00011000	CAN	Cancel
19	25	031	00011001	EM	End of Media
1A	26	032	00011010	SUB	Substitute
1B	27	033	00011011	ESC	Escape
1C	28	034	00011100	FS	File Separator
1D	29	035	00011101	GS	Group Separator
1E	30	036	00011110	RS	Record Separator
1F	31	037	00011111	VS	
20	32	040	00100000	SP	Space
21	33	041	00100001	!	Exclamation
22	34	042	00100010	"	Double Quote
23	35	043	00100011	#	Number or Pound
24	36	044	00100100	\$	Dollar Sign
25	37	045	00100101	%	Percentage
26	38	046	00100110	&	Ampersand
27	39	047	00100111	'	Apostrophe or Single Quote
28	40	050	00101000	(	Parentheses
29	41	051	00101001	)	Parentheses
2A	42	052	00101010	*	Astrick
2B	43	053	00101011	+	Plus
2C	44	054	00101100	,	Comma
2D	45	055	00101101	-	Minus
2E	46	056	00101110	.	Period
2F	47	057	00101111	/	Slash

B ASCII CHARACTER SET cont'd

HEX	DEC	OCT	BINARY	CHARACTER	DESCRIPTION
30	48	060	00110000	0	Zero
31	49	061	00110001	1	One
32	50	062	00110010	2	Two
33	51	063	00110011	3	Three
34	52	064	00110100	4	Four
35	53	065	00110101	5	Five
36	54	066	00110110	6	Six
37	55	067	00110111	7	Seven
38	56	070	00111000	8	Eight
39	57	071	00111001	9	Nine
3A	58	072	00111010	:	Colon
3B	59	073	00111011	;	Semi-colon
3C	60	074	00111100	<	Less Than
3D	61	075	00111101	=	Equal
3E	62	076	00111110	>	Greater Than
3F	63	077	00111111	?	Question
40	64	100	01000000	@	At sign
41	65	101	01000001	A	Letter A
42	66	102	01000010	B	Letter B
43	67	103	01000011	C	Letter C
44	68	104	01000100	D	Letter D
45	69	105	01000101	E	Letter E
46	70	106	01000110	F	Letter F
47	71	107	01000111	G	Letter G
48	72	110	01001000	H	Letter H
49	73	111	01001001	I	Letter I
4A	74	112	01001010	J	Letter J
4B	75	113	01001011	K	Letter K
4C	76	114	01001100	L	Letter L
4D	77	115	01001101	M	Letter M
4E	78	116	01001110	N	Letter N
4F	79	117	01001111	O	Letter O
50	80	120	01010000	P	Letter P
51	81	121	01010001	Q	Letter Q
52	82	122	01010010	R	Letter R
53	83	123	01010011	S	Letter S
54	84	124	01010100	T	Letter T
55	85	125	01010101	U	Letter U
56	86	126	01010110	V	Letter V
57	87	127	01010111	W	Letter W
58	88	130	01011000	X	Letter X
59	89	131	01011001	Y	Letter Y
5A	90	132	01011010	Z	Letter Z
5B	91	133	01011011	[	Left Bracket
5C	92	134	01011100	]	Right Bracket
5D	93	135	01011101	/	Back Slash
5E	94	136	01011110	↑	Up Arrow
5F	95	137	01011111	←	Back Arrow

B ASCII CHARACTER SET cont'd

HEX	DEC	OCT	BINARY	CHARACTER	DESCRIPTION
60	96	140	01100000	`	Back Quote or Accent Mark
61	97	141	01100001	a	Small Letter a
62	98	142	01100010	b	Small Letter b
63	99	143	01100011	c	Small Letter c
64	100	144	01100100	d	Small Letter d
65	101	145	01100101	e	Small Letter e
66	102	146	01100110	f	Small Letter f
67	103	147	01100111	g	Small Letter g
68	104	150	01101000	h	Small Letter h
69	105	151	01101001	i	Small Letter i
6A	106	152	01101010	j	Small Letter j
6B	107	153	01101011	k	Small Letter k
6C	108	154	01101100	l	Small Letter l
6D	109	155	01101101	m	Small Letter m
6E	110	156	01101110	n	Small Letter n
6F	111	157	01101111	o	Small Letter o
70	112	160	01110000	p	Small Letter p
71	113	161	01110001	q	Small Letter q
72	114	162	01110010	r	Small Letter r
73	115	163	01110011	s	Small Letter s
74	116	164	01110100	t	Small Letter t
75	117	165	01110101	u	Small Letter u
76	118	166	01110110	v	Small Letter v
77	119	167	01110111	w	Small Letter w
78	120	170	01111000	x	Small Letter x
79	121	171	01111001	y	Small Letter y
7A	122	172	01111010	z	Small Letter z
7B	123	173	01111011	{	Left Brace
7C	124	174	01111100		Vertical Bar
7D	125	175	01111101	}	Right Brace
7E	126	176	01111110	~	Approximate or Tilde
7F	127	177	01111111	DEL	Delete

## C INTERFACING SPECIFICATIONS

### C.1 INTERFACING SIGNALS

The Sphere system interface is chiefly TTL compatible. It consists of 4 main bus cables and provisions for peripheral adaptors. See Table C-1.

THE DATA BUS is a 14 conductor ribbon cable connecting to socket X3 on all boards. This Bus contains the 8 data lines (D0-D7), the Bus Available (BA), and the REFRESH signals. Eight pins are used for the data bus. It is bi-directional, transferring data to and from the memory and peripheral devices; it's three-state output buffers are capable of driving 35 standard TTL loads. A high on BA indicates the CPU is NOT using the 8 data lines and they are in a TRI-STATE (high impedance) mode. In this mode the Data Bus is available for other functions. BA can drive up to 35 TTL loads. The REFRESH signal will go low each time a dynamic memory bank is to be refreshed or updated. During these times the address lines will be determining the set of memories that are to be refreshed and the CPU will be in a halted mode. REFRESH can drive up to 8 TTL loads.

THE ADDRESS BUS consists of two 14 conductor flat ribbon cables which join X1 and X2 on all boards. Table C-1 gives the pin numbers. The signals with their definitions are as follows:

CLOCK PHASE TWO ( $\phi 2$ ) - 670 KHZ signal, High 950 ns and Low 540 ns, capable of driving 35 TTL loads.

ADDRESS BUS (A0-A15) - Sixteen pins are used for the address bus. The outputs are three-state bus drivers capable of driving 35 standard TTL loads. When the output is turned off, it is essentially an open circuit. This permits the system to be used in DMA applications. BA also indicates the state of the Address Bus.

HALT - When this input is in the low state, all activity in the machine will be halted. This input is level sensitive. In the halt mode, the machine will stop at the end of an instruction, Bus Available will be at a high level and Valid Memory Address will be at a low level. This line is open-collector with the pull-up on the CPU board.

Transition of the HALT line must not occur during the last 250 ns of  $\phi 1$ . To insure single instruction operation, the Halt line must go high for one  $\phi 1$  Clock cycle. If HALT is chopped during  $\phi 2$ , the next machine cycle will take place.

THREE-STATE CONTROL (TSC) - In order to use this line a jumper must be added on the CPU board. This input causes all of the address lines and the Read/Write line to go into the off or high impedance state

## C INTERFACING SPECIFICATIONS

### C.1 INTERFACING SIGNALS cont'd

500 ns after TSC rises above 2.4V The Valid Memory Address and Bus Available signals will be forced low. The data bus is not affected by TSC and has its own enable (Data Bus Enable). In DMA applications, the Three-State Control line should be brought high on the leading edge of the Phase One Clock. The  $\phi 1$  clock must be held in the high state and ~~the~~  $\phi 2$  in the low state for this function to operate properly. Since the MPU is a dynamic device, it can be held in this state for only 5.0 us or destruction of data will occur in the MPU.

READ/WRITE (R/W) - This TTL compatible output signals the peripherals and memory devices whether the MPU is in a Read (high) or Write (low) state. The normal standby state of this signal is Read (high). Three-State Control going high will turn Read/Write to the high state. Also, when the processor is halted, it will be in the high state. This output is capable of driving 35 standard TTL loads.

VALID MEMORY ADDRESS (VMA) - This output indicates to peripheral devices that there is a valid address on the address bus. In normal operation, this signal should be utilized for enabling peripheral interfaces such as the PIA and ACIA. This signal is not Tri-State. 35 standard TTL loads may be directly driven by this active high signal.

INTERRUPT REQUEST ( $\overline{\text{IRQ}}$ ) - This level sensitive input requests that an interrupt sequence be generated within the machine. The processor will wait until it completes the current instruction that is being executed before it recognizes the request. At that time, if the interrupt mask bit in the Condition Code Register is not set, the machine will begin an interrupt sequence. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored on the stack. Next the MPU will respond to the interrupt request by setting the interrupt mask bit high so that no further interrupts will be recognized. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFF8 and FFF9. An address loaded at these locations causes the MPU to branch to an interrupt routine in memory.

The  $\overline{\text{Halt}}$  line must be in the high state for interrupts to be recognized.

The  $\overline{\text{IRQ}}$  has a high impedance pull-up device internal to the chip; however a 3.3K ohm external resistor to  $V_{CC}$  has been used for wire-OR and optimum control of interrupts.

## C INTERFACING SPECIFICATIONS

### C.1 INTERFACING SIGNALS cont'd

RESET - This input is used to reset and start the MPU from a power down condition, resulting from a power failure or an initial start up of the processor. This is an Open-Collector line with the pull up resistor on the CPU board. Lower this signal will cause the MPU to begin the restart sequence. This will start execution of a routine to initialize the processor from its reset condition. All the higher order address lines will be forced high. For the restart, the last two (FFFE, FFFF) locations in memory will be used to load the program that is addressed by the program counter. During the restart routine, the interrupt mask bit is set and must be reset before the MPU can be interrupted by IRQ.

Figure C-1 shows the initialization of the microprocessor after restart. Reset must be held low for at least eight clock periods after  $V_{CC}$  reaches 4.75 volts. If Reset goes high prior to the leading edge of  $\phi_2$ , on the next  $\phi_1$  the first restart memory vector address (FFFE) will appear on the address lines. This location should contain the higher order eight bits to be stored into the program counter. Following, the next address FFFF should contain the lower order eight bits to be stored into the program counter.

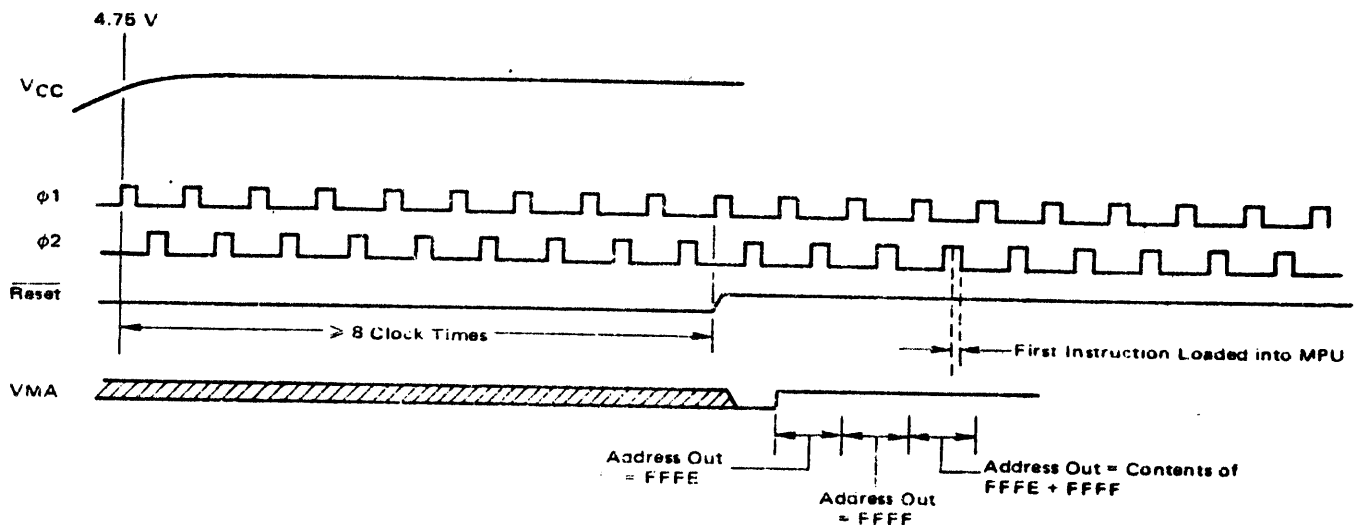


FIGURE C.1  
INITIALIZATION OF MPU AFTER RESTART

TABLE C-1

CONNECTOR STANDARD PIN ASSIGNMENTS

Pin No.	Address Bus		Data Bus	PIA (A)	PIA (B)	KBD/2
	X1	X2	X3	X4, X7, X9, X11	X5, X8, X10, X12	X20
1	R/W	A2	D4	RESET	RESET	RESET
2	A9	A4	D7	PA 0	PB 0	D 0
3	VMA	A3	BA	PA 1	PB 1	D 1
4	A14	A5	OPEN	PA 3	PB 3	D 3
5	A15	A6	D3	PA 5	PB 5	D 5
6	HLT	A7	D2	PA 6	PB 6	D 6
7	NMI	A8	D0	OPEN **	OPEN **	OPEN
8	OPEN	A0	D1	GROUND	GROUND	GROUND
9	OPEN	A1	REFRESH	PA 7	PB 7	Repeat/D 7
10	A13	IRQ(intcpt)	OPEN	PA 4	PB 4	D 4
11	A12	OPEN	OPEN	PA 2	PB 2	D 2
12	A11	RESET	OPEN	CA 2	CB 2	Character Strobe
13	A10	TSC	D5	CA 1*	CB 1	unused
14	Ø2	OPEN	D6	+5V DC	+5V DC	+5V DC

C INTERFACING SPECIFICATIONS

\* On CPU/2 X4 CA1 is hard wired to the Real Time Clock  
 \*\* On CPU/1 & CPU/2 X4 & X5 pin is wired to +5VDC



TABLE C-1 cont'd

CONNECTOR STANDARD PIN ASSIGNMENTS

<u>Pin No.</u>	<u>Power Bus</u>	<u>CRT/1</u>	<u>Line Printer</u>	<u>SIM/1</u>			
	X6	X5	X13	X14	X15	X24	X25
1	GND		D5	RUN	SWI	C1 EAR	MODEM OUT
2	GND		D4	STROBE	HOME	C2 REM	RI
3	+12 VDC		D3	LAMP 1	EMPTY	C2 REM	RS232 R <sub>x</sub>
4	-5 VDC		D2	FEED	SW 2	C1 REM	OH
5	-12 VDC		D1	CLEAR	JAM	C1 REM <sub>A</sub>	RS232 T <sub>x</sub>
6	+5 VDC		D0	LAMP 2	PO	20maT <sub>x</sub>	TV
7	+5 VDC		+5 VDC	OPEN	OPEN	GND	GND
8	GND		GND	GND	GND	20maR <sub>x</sub>	MODEM IN
9	GND		GND	GND	GND	20maCOM	-12
10	+12 VDC		GND	GND	GND	C1 +12	TTL R <sub>x</sub>
11	-5 VDC		GND	GND	GND	C2 EAR	SH
12	-12 VDC		GND	D6	GND	C2 MIC	DA
13	+5 VDC		GND	GND	GND	C1 MIC	TTL T <sub>x</sub>
14	+5 VDC		D7	GND	GND	C2 +12	GND

For use with light pen

## C INTERFACING SPECIFICATIONS

### C.1 INTERFACING SIGNALS cont'd

NON-MASKABLE INTERRUPT (NMI) - A low going edge on this input requests that a non-maskable-interrupt sequence be generated within the processor. As with the Interrupt Request signal, the processor will complete the current instruction that is being executed before it recognizes the NMI signal. The interrupt mask bit in the Condition Code Register has no effect on NMI.

The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFFC and FFFD. An address loaded at these locations causes the MPU to branch to a non-maskable interrupt routine in memory.

NMI has a high impedance pullup resistor internal to the chip; however a 3.3K ohm external resistor to V<sub>CC</sub> has been used for wire-OR and optimum control of interrupts.

Inputs IRQ and NMI are hardware interrupt lines that are sampled during  $\phi 2$  and will start the interrupt routine on the  $\phi 1$  following the completion of an instruction.

Figure C-2 is a flow chart describing the major decision paths and interrupt vectors of the microprocessor. Table C-2 gives the memory map for interrupt vectors.

Vector		Description
MS	LS	
FFFE	FFFF	Restart
FFFC	FFFD	Non-maskable Interrupt
FFFA	FFFB	Software Interrupt
FFF8	FFF9	Interrupt Request

TABLE C-2  
MEMORY MAP FOR INTERRUPT VECTORS

C INTERFACING SPECIFICATIONS

C.1 INTERFACING SIGNALS cont'd

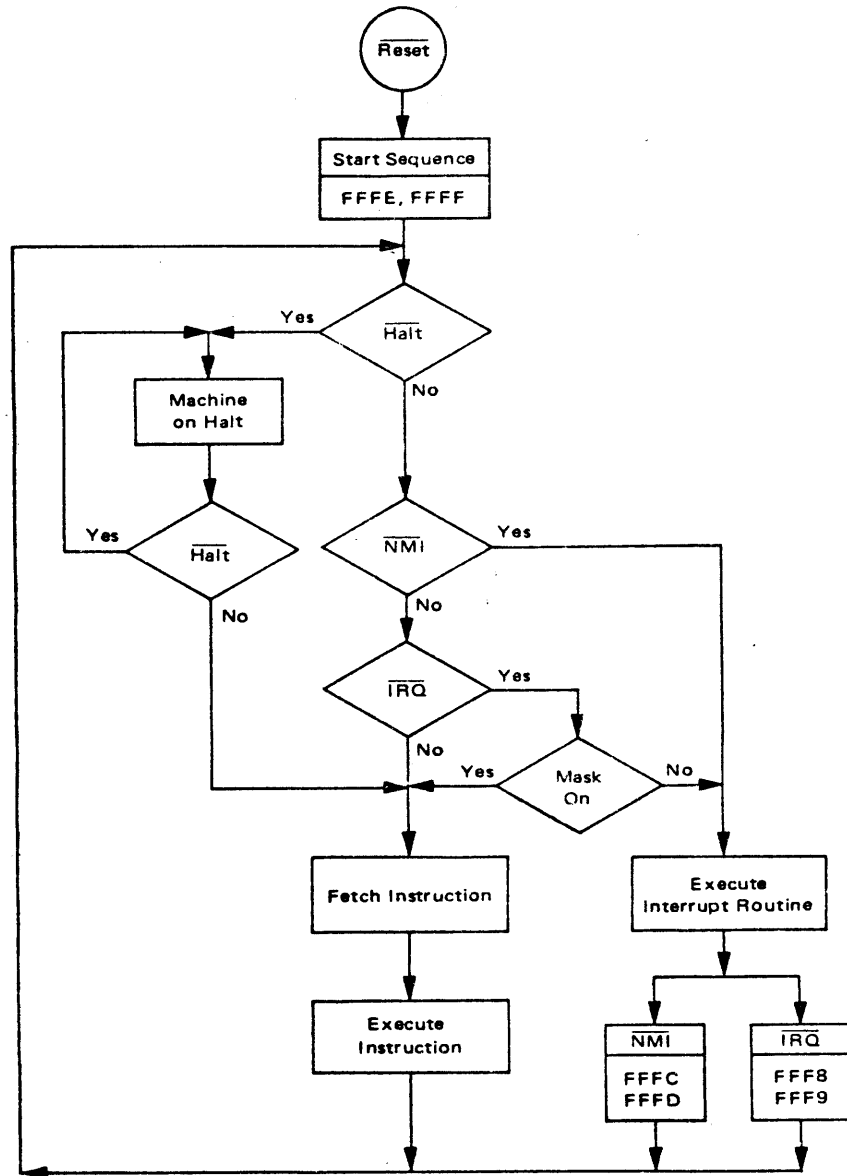


FIGURE C-2

MPU FLOW DIAGRAM

THE PIA BUS

The Peripheral Interface Adaptor on the CPU/2 Board is connected to sockets X4 and X5. On the Peripheral Interface Module (PIM/1) board there are 4 PIA chips with 8 sockets numbered X4-X5 and X7-X12. All interconnections remain common for ease of use and standardization. See Table C-1 for pin numbers.

## C INTERFACING SPECIFICATIONS

### C.2 PIA INTERNAL ORGANIZATION

An expanded Block Diagram of the PIA is shown in Figure C-3. Internally, the PIA is divided into two symmetrical independent register configurations. Each half has three main features: an Output Register, a Control Register, and a Data Direction Register. It is these registers that the CPU treats as memory locations, i.e., they can be either read from or written into. The Output and Data Direction Registers on each side represent a single memory location to the CPU. Selection between them is internal to the PIA and is determined by a bit in their Control Register.

The Data Direction Registers (DDR) are used to establish each individual peripheral bus line as either an input or an output. This is accomplished by having the CPU write "ones" or "zeros" into the eight bit positions of the DDR. Zeros or ones cause the corresponding peripheral data lines to function as inputs or outputs, respectively.

The Output Registers, ORA and ORB, when addressed, store the data present on the CPU Data Bus during a CPU write operation. As used here, an "CPU Write" operation refers to the execution of the "Store" instruction, i.e., writing into Output Register A is equivalent to execution of STAA PIA by the CPU. Similarly, a "CPU Read" operation is equivalent to execution of the 'Load' instruction: LDAA PIA. This data will also appear on those peripheral lines that have been programmed as outputs. If a peripheral line has been programmed as an input, the corresponding bit position of the Output Register can still be written into by the CPU, however, the data will be influenced by the external signal applied on that peripheral data line.

During a CPU read operation, the data present on peripheral lines programmed as inputs is transferred directly to the system Data Bus. Due to differing circuitry, the results of reading positions programmed as outputs differ slightly between sides A and B of the PIA. On the B side, there is three-state buffering between Output Register B and the peripheral lines such that the CPU will read the current contents of ORB for those bit positions programmed as outputs. During an CPU Read of the A side, the data present on the Peripheral lines will effect the CPU Data Bus regardless of whether the lines are programmed as outputs or inputs. The bit positions in ORA designated as outputs will be read correctly only if the external loading on the Peripheral lines is within the specification for one TTL load. That is, a logic one level could be read as a logic zero if excessive loading reduced the voltage below 2.0 volts.

C INTERFACING SPECIFICATIONS

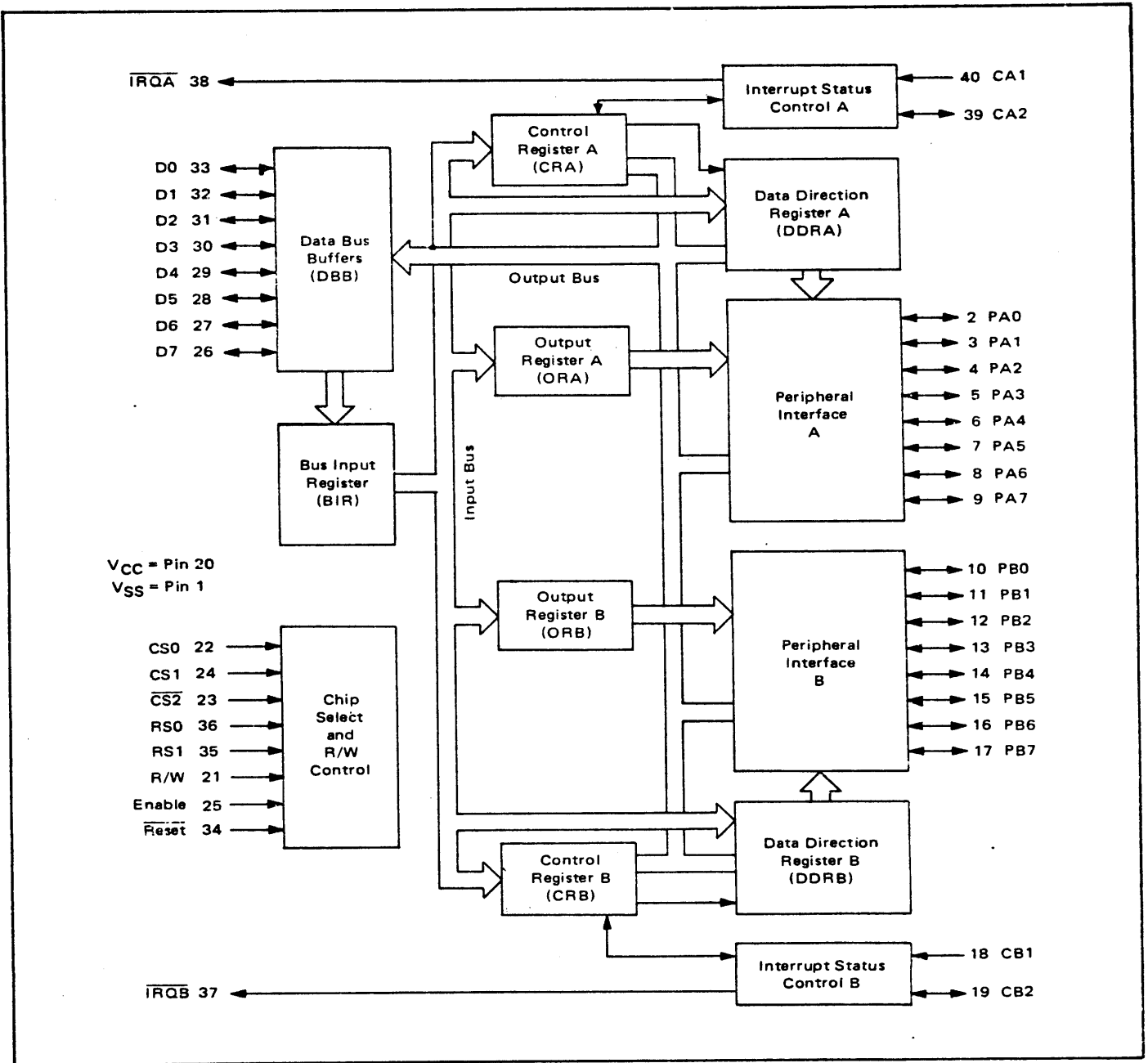


FIGURE C-3  
PIA BLOCK DIAGRAM  
C-9

## C INTERFACE SPECIFICATIONS

### C.2 PIA INTERNAL ORGANIZATION cont'd

The two Control Registers, CRA and CRB, allow the CPU to establish and control the operating modes of the peripheral control lines, CA1, CA2, CB1, and CB2. It is by means of these four lines that control information is passed back and forth between the CPU and peripheral devices. The control word format and a summary of its features is shown in Figure C-4.

The Data Direction Register access bit ( $b_2 = \text{DDR Access}$ ) is used in conjunction with the register select lines to select between internal registers. For a given register select combination, the status of the DDR bit determines whether the Data Direction Register ( $b_2$  of DDR = 0) or the Output Register ( $b_2$  of DDR = 1) is addressed by the CPU.

Each Control Register has two interrupt request flags,  $b_7 = \text{IRQA(B)1}$  and  $b_6 = \text{IRQA(B)2}$ ; they are set by transitions of the CA1 (CB1) and CA2 (CB2) control lines and can be read by an CPU Read Control Register operation. The status of the interrupt flags cannot be altered by an CPU write instruction, that is,  $\text{IRQA(B)1}$  and  $\text{IRQA(B)2}$  are Read Only with respect to the CPU. They are indirectly reset to zero each time the CPU reads the corresponding Output Register or can be cleared with the hardware Reset.

Bits  $b_0$  and  $b_1$  of the Control Registers determine the CA1 (CB1) operating mode. A "one" written into  $b_1$  by the CPU will cause subsequent positive going transitions of the CA1 (CB1) input to set  $\text{IRQA(B)1}$ ; if  $b_1 = 0$ , negative going transitions on CA1 (CB1) cause  $\text{IRQA(B)1}$  to set. If  $b_0 = 1$  when the  $\text{IRQA(B)1}$  flag goes high, the PIA's external interrupt request line,  $\text{IRQA(B)}$ , immediately goes low, providing a hardware interrupt signal to the CPU. The external interrupt is disabled if  $b_0 = 0$  when the internal interrupt is set by CA1 (CB1). If  $b_0$  is later set by an CPU write Control Register operation, the disable is immediately released and a pending external interrupt request will occur.

When  $b_5 = 0$ ,  $b_3$  and  $b_4$  of the Control Register perform similarly to  $b_0$  and  $b_1$ , controlling the  $\text{IRQA(B)2}$  interrupt via the CA2 (CB2) input. The  $\text{IRQ}$  interrupt request, when enabled, responds to either  $\text{IRQA(B)1}$  or  $\text{IRQA(B)2}$ .

If  $b_5 = 1$ , CA2 (CB2) acts as an output and will function in one of three modes. If  $b_4$  is also equal to one, CA2 (CB2) serves as a program controlled set/reset output to the peripheral and follows  $b_3$  as it is changed by CPU Write Control Register operations. If  $b_4 = 0$  when  $b_5 = 1$ , CA2 (CB2) can be used in either a pulse strobed or handshake mode. Operation of the two sections differ slightly for these two operating modes. In the handshake mode ( $b_3 = 0$ ) CA2 is taken low by the negative transition of the CPU Enable Pulse following an CPU read Output Register operation and returns high when  $\text{IRQA1}$  is next set by CA1.

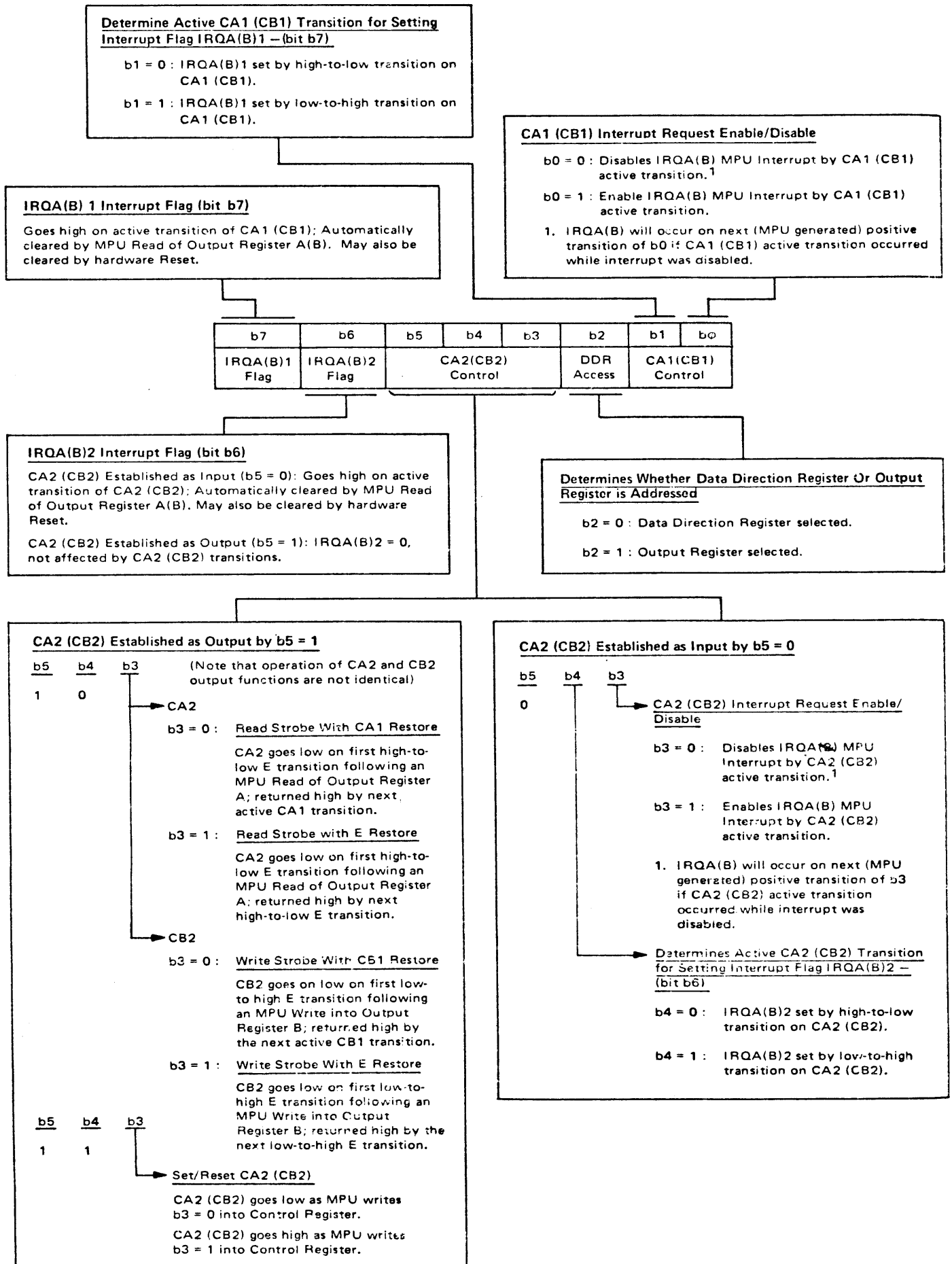


FIGURE C-4  
 PIA CONTROL REGISTER FORMAT  
 C-11

## C INTERFACING SPECIFICATIONS

### C.2 PIA INTERNAL ORGANIZATION cont'd

This, in effect, tells the peripheral it has been read and allows it to acknowledge via CA1. The "B" Side operation is similar except that CB2 is taken low following an MPU Write Output Register operation and returned high by the next CBI transition; this tells the peripheral it has been written into and allows it to respond via CBI.

In the pulse strobed mode ( $b_3 = 1$ ), CA2 is again set low by a Read Output Register command, but is now returned high by the negative transition of the next MPU originated Enable Pulse. CB2 operation is similar except that an MPU Write Operation initiates the pulse. The use of A side for Read and B side for Write in those figures is not meant to imply that A and B sides must be used only for peripheral data in and out, respectively. However, the strobe modes are implemented only as shown, i.e., a strobe is not generated by an A side Write or a B side Read. Strokes can be generated for these cases by including "dummy" instructions in the program. For example, an A side Write instruction can be followed immediately by an A side dummy Read to generate the strobe. Similarly, a B side Read can be followed by a dummy Write.

### C.3 LINE PRINTER

For interfacing signals to the Line Printer see the PIM/1 schematic and Table C-1 for pin numbers. Socket X15 receives signals from the Line Printer. They include HOME, EMPTY, SW1, SW2, JAM, and PO. When HOME is low, it indicates the print head is at either side of the printer and ready for data. When EMPTY is low, it indicates no data has been entered into the storage buffer. SW1 will go low when the RED switch (left) is depressed. This signal will generate a CLEAR signal for the printer. SW2 will go high when the YELLOW switch (right) is depressed. This signal places the printer on-line when first pressed (Light comes on) and Off-Line when pressed again (Light goes out).

JAM will go high if the paper is jammed or some other printer malfunction occurs. The RED Lamp (left) will come on. Once the jam condition is corrected, the clear switch (RED) can be depressed to reinitialize the printer (RED light will go out). PO is the out of paper signal and acts the same as JAM. Holding the RED clear switch down will allow automatic paper feeding.

Sockets X13 and X14 provide signals to the printer. D0 to D5 contain the Data codes. D6 provides for lowercase letters and D7 provides for double width printing. They are true when high. RUN going low will cause the data on D0-D7 to be loaded into the buffer register. After the first strobe pulse, the EMPTY signal will go high. CLEAR going low resets the printer from a JAM or PO condition.



## C INTERFACING SPECIFICATIONS

### C.3 LINE PRINTER cont'd

A system reset also causes a CLEAR signal. LAMP 1 going low causes the RED (left) lamp to light. LAMP 2 going low causes the YELLOW (right) lamp to light.

### C.4 P.C. BOARD CONNECTIONS

#### C.4.1 CRT/1

On the CRT/1 board there are two types of signals. The "COMP VIDEO" and "GND" are used to connect via 2 wires directly to the composite video input of a video monitor. The two long paths are used for RF TV antenna "proximity" connection. See the assembly instructions for the CRT Board.. These wires may be soldered directly into the P.C. board hole as labeled. If the Video monitor is over 10 feet distant from the CRT board, coaxial cable should be used.

#### C.4.2 SIM/1

On the Serial Interface Module board SIM/1 there are a large number of solder holes or "posts" for direct wiring to various interface I/O peripherals. As explained in the assembly instructions, these include cassettes, modems, teletypes, RS232 lines, 20 ma current loop, and TTL compatible devices. Wires may be taken from the board edge nearest the back panel to jacks along the chassis or directly out to the devices. An ON/OFF relay with one normally open 10 watt contact (DC only) is also provided on this board for each communications interface. This relay can be used for computer control of the cassette, TTY, or any other device with in the 10 watt limit.

#### C.4.3 PIM/1

On the PIM board the top two PIA chips with their sockets may be used to control a floppy disc (IBM Compatible types). The third PIA is prewired out to a large "breadboard" area for the customer to interface any devices he can dream up. The IC sockets have power provided to pins 14 and Ground on pins 8. A place is present for resistors and capacitors. The 4th PIA is used for the printer interface circuitry. The 20 I/O lines may be used by removing the printer interface circuitry. Then X11 and X12 will provide the connections via 14 conductor flat ribbon cables. Similiarly the first 3 PIA's can be used via their 14 pin sockets with flat ribbon cables out through the bottom or back of

## C INTERFACING SPECIFICATIONS

### C.4 P.C. BOARD CONNECTIONS

#### C.4.3 PIM/1 cont'd

the chassis. This makes 80 I/O lines with +5V DC, RESET, and Ground available as Digital TTL compatible (1 load each) interface signals. Pin 7 is uncommitted and other necessary signals can be jumpered to this location.

#### C.4.4 CPU/2

On the CPU/2 board at the right hand side are 3 solder points for interface to a teletype or other 20 ma current loop device. In this mode add the two jumpers PB0 and PB7 and use the appropriate software. Note that PB0 and PB7 on the X5 connector socket should not be used as I/O lines. Also available on the top edge of the board are connections for an RS232c serial device.

## D COMPONENT DESCRIPTIONS

This section is designed to help the user by providing a summary of the specifications of the components used in the Sphere system. Not listed are resistors, capacitors and hardware generally available.

### DIODES

MBD501	D-3
SCBA05 (or VK048)	D-5
1N914	D-6
1N4001	D-6
1N4743	D-8
1N5225-B	D-13
1N5338-B	D-19
1N5339-B	D-19
1N5348-B	D-19
1N5349	D-19
3SM2 (or V352)	D-22

### TRANSISTORS

MPS6521	D-23
MPS6523	D-23
TIP36A	D-24
2N2369-A	D-28
2N5129	D-30
2N4400	D-31

### OPTO-ISOLATORS

4N33	D-36
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### VOLTAGE REGULATORS

LM309K	D-40
LM340K-12	D-43

### VOLTAGE COMPARATORS

LM311	D-50
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### INTEGRATED CIRCUITS

555	D-55
741	D-59
1488 (or 75188)	D-63
1489 (or 75189)	D-67
4001	D-71
4013	D-73
4018	D-76
4070	D-81
6800	D-84
6810	D-95
6820	D-99
6842	D-107
6850	D-117
6860	D-126

D COMPONENT DESCRIPTIONS

INTEGRATED CIRCUITS cont'd

7400	D-141
7402	D-142
7404	D-143
7405	D-145
7407	D-146
7408	D-147
7409	D-148
7410	D-149
7411	D-150
7417	D-146
7420	D-151
7427	D-152
7430	D-153
7442	D-154
7451	D-155
7474	D-157
7483	D-159
7486	D-161
7490	D-162
7493	D-163
7495	D-165
74123	D-166
74150	D-168
74155	D-170
74156	D-170
74157	D-173
74163	D-175
74166	D-180
74174	D-181
8096	D-183
8097	D-183
8098	D-183
8123	D-185
8833	D-187
9601	D-188
9602	D-190

CHARACTER GENERATORS

2513	D-193
SCM 3088L 7435A 604-V10H-01	D-200


MEMORIES

1702A	D-201
2102	D-206
2107A (or equiv.)	D-209

# D COMPONENT DESCRIPTIONS

## D.1 DIODES

MBD501

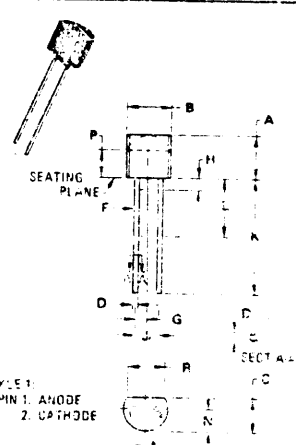


**SILICON HOT-CARRIER DIODE  
(SCHOTTKY BARRIER DIODE)**

... designed primarily for high-efficiency UHF and VHF detector applications. Readily adaptable to many other fast switching RF and digital applications. Supplied in an inexpensive plastic package for low-cost, high volume consumer and industrial/commercial requirements.

- The Schottky Barrier Construction Provides Ultra Stable Characteristics By Eliminating the "Cut-Whisker" or "S-Bend" Contact
- Extremely Low Minority Carrier Lifetime — 100 ps (Max)
- Very Low Capacitance — 1.0 pF
- High Reverse Voltage — to 70 Volts
- Low Reverse Leakage — 200 nA (Max)

**HIGH-VOLTAGE  
SILICON HOT-CARRIER  
DETECTOR AND SWITCHING  
DIODES  
50-70 VOLTS**



STYLE 1:  
PIN 1 ANODE  
PIN 2 CATHODE

CASE 102-1

Rating	Symbol	Value	Unit
Reverse Voltage	V <sub>R</sub>	50 70	Volts
Forward Power Dissipation @ T <sub>A</sub> = 25°C Derate Above 25°C	P <sub>F</sub>	100 5.0	mW mW/°C
Operating Junction Temperature Range	T <sub>J</sub>	-55 to +125	°C
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C

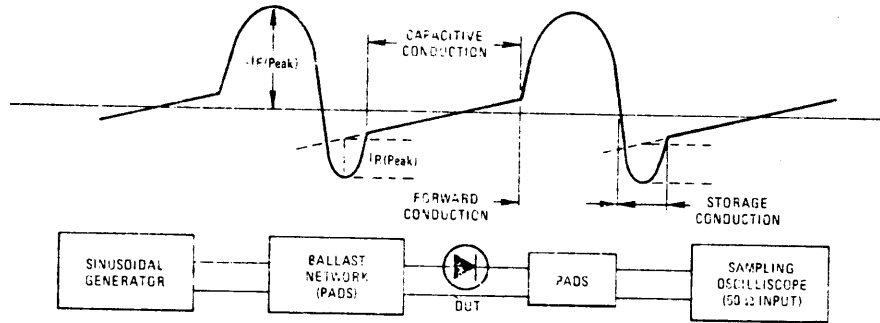
### ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I <sub>R</sub> = 10 μA dc)	V <sub>(BR-R)</sub>	50 70	-	-	Volts
Total Capacitance, Figure 1 (V <sub>R</sub> = 20 Volts, f = 1.0 MHz)	C <sub>T</sub>	-	0.5	1.0	pF
Minority Carrier Lifetime, Figure 2 (I <sub>F</sub> = 0 mA, Kraussner Method)	τ	-	15	100	ps
Reverse Leakage, Figure 3 (V <sub>R</sub> = 15 V) (V <sub>R</sub> = 35 V)	I <sub>R</sub>	-	7.0 3.0	200 200	nA dc
Forward Voltage, Figure 4 (I <sub>F</sub> = 10 mA dc)	V <sub>F</sub>	-	1.0	1.2	V dc
Series Inductance (f = 250 MHz, Lead Length ≈ 1.16")	L <sub>S</sub>	-	9.0	-	nH
Parasitic Capacitance (f = 1.0 MHz, Lead Length ≈ 1.15")	C <sub>C</sub>	-	0.18	-	pF

D COMPONENT DESCRIPTIONS  
 D.1 DIODES

MBD501 cont'd

KRAKAUER METHOD OF MEASURING LIFE TIME



TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 - TOTAL CAPACITANCE

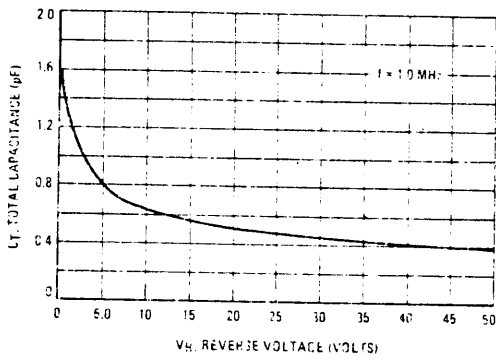


FIGURE 2 - MINORITY CARRIER LIFETIME

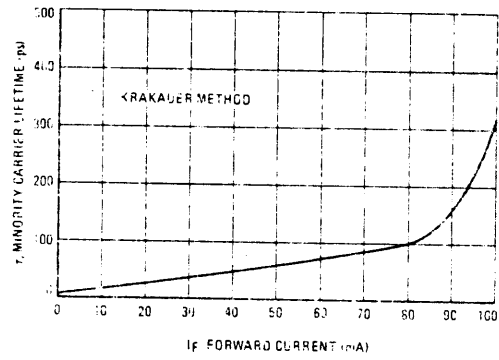


FIGURE 3 - REVERSE LEAKAGE

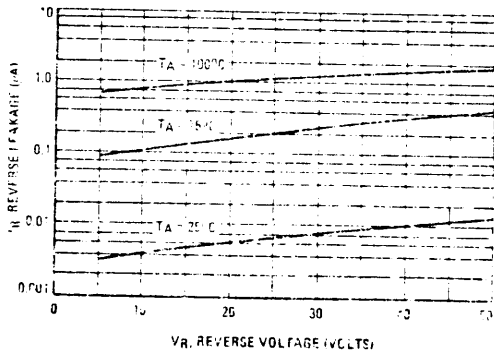
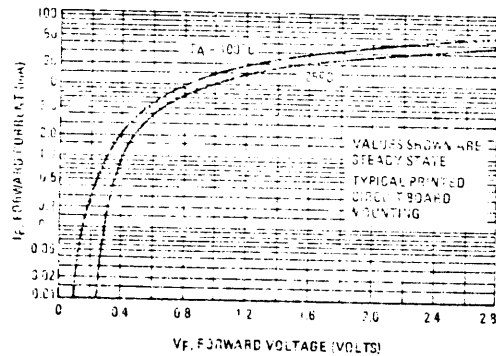


FIGURE 4 - FORWARD VOLTAGE



## D COMPONENT DESCRIPTIONS

### D.1 DIODES

SCBA05 (or VK048)

### "ALPAC" SILICON BRIDGE RECTIFIERS

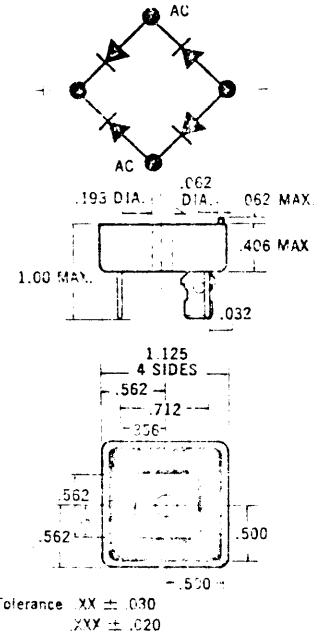
Semtech Corporation introduces "ALPAC" a complete line of Single Phase Silicon Bridge Rectifier circuits. Designed in Aluminum Cases to provide maximum thermal conductivity and simple installation. "ALPAC" universal terminals, insulated from case, provide a 3 way electrical connection: fast disconnect, wire wrap around and hole wire insert for soldering. Internally the device utilizes the Semtech high performance solid double heat sink junctions designed for mechanical strength and eliminating the use of solders for improved reliability. The bridges are designed for utilization in power supplies, AC to DC converters and motor control circuits.

Type No.	Riv Per Leg	Sine Wave Input Voltage (Vrms)	Average AC Output (Vrms)			Average DC Output (Vdc)			Peak 1 Cycle Fwd. Surge	Peak Recurrent Fwd.	VF Max. For Leg (V) 50 Hz AC	Reverse Current (I <sub>R</sub> Max. @ 100°C)		Data Sheet No.
			50	100	175	25	50	100				25	100	
		Volts	Amps	Amps	Amps	Amps	Amps	Amps	Amps	Volts	µA	µA		

SCBA05	50	35	25	19.5	12.5	6.0	5.0	3.0	150	75	1.0	5	100	MB3
SCBA1	100	70	25	18.5	12.5	6.0	5.0	3.0	150	75	1.0	5	100	MB3
SCBA2	200	140	25	18.5	12.5	6.0	5.0	3.0	150	75	1.0	5	100	MB3
SCBA3	300	210	25	18.5	12.5	6.0	5.0	3.0	150	75	1.0	5	100	MB3
SCBA4	400	280	25	18.5	12.5	6.0	5.0	3.0	150	75	1.0	5	100	MB3
SCBA6	600	420	25	18.5	12.5	6.0	5.0	3.0	150	75	1.0	5	100	MS3

Maximum thermal impedance junction to mounting surface 1.5° C/Watt.  
Maximum operating and storage temperature —55° C to +150° C.

ALSO AVAILABLE IN FAST RECOVERY  
TECH BULLETIN MB15



# D COMPONENT DESCRIPTIONS

## D.1 DIODES

### 1N914

absolute maximum ratings at 25°C ambient temperature (unless otherwise noted)

$V_R$	Reverse Voltage at -65 to +120°C	1N914	1N914A	1N914B	1N915	1N916	1N916A	1N916B	1N917	Unit
$I_O$	Average Rectified Fwd. Current	75	75	75	50	75	75	75	30	v
$I_O$	Average Rectified Fwd. Current at +150°C	75	75	75	75	75	75	75	50	ma
$I_F$	Recurrent Peak Fwd. Current	10	10	10	10	10	10	10	10	ma
$I_{F(surge)}$	Surge Current, 1 sec	225	225	225	225	225	225	225	150	ma
$P$	Power Dissipation	500	500	500	500	500	500	500	300	mW
$T_A$	Operating Temperature Range	-65 to +175								°C
$T_{stg}$	Storage Temperature Range	200								°C

maximum electrical characteristics at 25°C ambient temperature (unless otherwise noted)

$BVR$	Min Breakdown Voltage at 100 $\mu$ A	160	100	100	65	100	100	100	40	v
$I_R$	Reverse Current at $V_R$	5	5	5	5	5	5	5	5	$\mu$ A
$I_R$	Reverse Current at -20 v	0.025	0.025	0.025		0.025	0.025	0.025		$\mu$ A
$I_R$	Reverse Current at -20 v at 100°C	3	3	3	5	3	3	3	25	$\mu$ A
$I_R$	Reverse Current at -20 v at +150°C	50	50	50		50	50	50		$\mu$ A
$I_R$	Reverse Current at -10 v				0.025				0.05	$\mu$ A
$I_R$	Reverse Current at -10 v at 125°C									$\mu$ A
$I_F$	Min Fwd Current at $V_F = 1$ v	10	20	100	50	10	20	30	10	ma
$V_F$	at 250 $\mu$ A								0.64	v
$V_F$	at 1.5 ma								0.74	v
$V_F$	at 3.3 ma								0.83	v
$V_F$	at 5 ma				0.72	0.73		0.73		v
$V_F$	Min at 5 ma				0.60					v
$C$	Capacitance at $V_R = 0$	4	4	4	4	2	2	2	2.5	pf

operating characteristics at 25°C ambient temperature (unless otherwise noted)

$t_{rr}$	Max Reverse Recovery Time	**4 °8	**4 °8	**4 °8	°10	**4 °8	**4 °8	**4 °8	°3	nsec
$V_F$	Fwd Recovery Voltage (50 ma Peak Sq. wave, 0.1 $\mu$ sec pulse width, 10 nsec rise time, 5 kc to 100 kc rep. rate)	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	v

- \* Trademark of Texas Instruments
- Lumatron (10 ma  $I_F$ , 10 ma  $I_R$ , recover to 1 ma)
- \*\* EG&G (10 ma  $I_F$ , 6v  $V_F$ , recover to 1 ma)

### 1N4001

\*absolute maximum ratings at specified ambient† temperature

		1N4001	1N4002	1N4003	1N4004	1N4005	1N4006	1N4007	UNIT
$V_{RM}$	Peak Reverse Voltage from -65°C to +175°C (See Note 1)	50	100	200	400	600	800	1000	v
$V_R$	Steady State Reverse Voltage from 25°C to 75°C	50	100	200	400	600	800	1000	v
$I_O$	Average Rectified Forward Current from 25°C to 75°C (See Notes 1 and 2)	1							a
$I_{FM(rep)}$	Repetitive Peak Forward Current, 10 cycles, at (or below) 75°C (See Note 3)	10							a
$I_{FM(surge)}$	Peak Surge Current, One Cycle, at (or below) 75°C (See Note 3)	30							a
$T_{A(oper)}$	Operating Ambient Temperature Range	-65 to +175							°C
$T_{stg}$	Storage Temperature Range	-65 to +200							°C
	Lead Temperature $\frac{1}{8}$ inch from Case for 10 Seconds	350							°C

NOTES: 1. These values may be applied continuously under single-phase, 60-cps, half-sine-wave operation with resistive load. Above 75°C derate  $I_O$  according to Figure 1

2. This rectifier is a lead-conduction-cooled device. At (or above) ambient temperatures of 75°C, the lead temperature  $\frac{1}{8}$  inch from case must be no higher than 5°C above the ambient temperature for these ratings to apply.

3. These values apply for 60-cps half sine waves when the device is operating at (or below) rated values of peak reverse voltage and average rectified forward current. Surge may be repeated after the device has returned to original thermal equilibrium.

\* Indicates JEDEC registered data.

† The ambient temperature is measured at a point 2 inches below the device. Natural air cooling shall be used.



D COMPONENT DESCRIPTIONS

D.1 DIODES

1N4001 cont'd

\*electrical characteristics at specified ambient temperature

PARAMETER	TEST CONDITIONS	MAX	UNIT
$I_R$ Static Reverse Current	$V_R = \text{Rated } V_{RR}, T_A = 25^\circ\text{C}$	10	$\mu\text{a}$
	$V_R = \text{Rated } V_{RR}, T_A = 100^\circ\text{C}$	50	$\mu\text{a}$
$I_{R(\text{avg})}$ Average Reverse Current	$V_{RM} = \text{Rated } V_{RM}, I_O = 1 \text{ a}, f = 60 \text{ cps}, T_A = 25^\circ\text{C}$	30	$\mu\text{a}$
$V_F$ Static Forward Voltage	$I_O = 1 \text{ a}, T_A = 25^\circ\text{C to } 75^\circ\text{C}$	1.1	v
$V_{F(\text{avg})}$ Average Forward Voltage	$V_{RM} = \text{Rated } V_{RM}, I_O = 1 \text{ a}, f = 60 \text{ cps}, T_A = 25^\circ\text{C to } 75^\circ\text{C}$	0.8	v
$V_{FM}$ Peak Forward Voltage	$V_{RM} = \text{Rated } V_{RM}, I_O = 1 \text{ a}, f = 60 \text{ cps}, T_A = 25^\circ\text{C to } 75^\circ\text{C}$	1.6	v

\*Indicates JEDEC registered data.

THERMAL INFORMATION

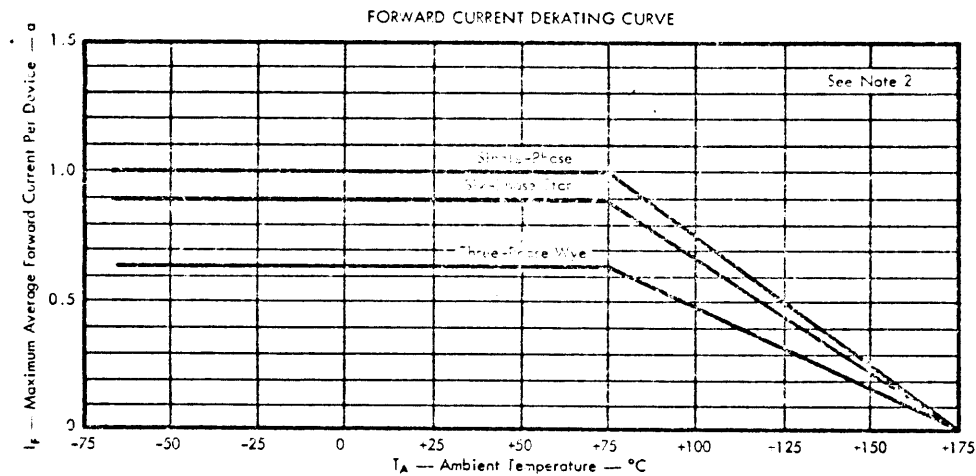


FIGURE 1

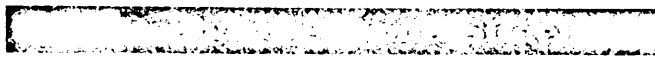
† The ambient temperature is measured at a point 2 inches below the device. Natural air cooling shall be used.

NOTE 2: This rectifier is a lead-temperature-sensitive device. At (or above) ambient temperatures of 75°C, the lead temperature 3/8 inch from case must be no higher than 5°C above the ambient temperature for these ratings to apply.

# D COMPONENT DESCRIPTIONS

## D.1 DIODES

1N4743



### 1.0 WATT SURMETIC 30 SILICON ZENER DIODES

A complete series of 1.0 Watt Zener Diodes with limits and operating characteristics that reflect the superior capabilities of silicon oxide-passivated junctions. All this in an axial lead, transfer-molded plastic package offering protection in all common environmental conditions.

- To 80 Watts Surge Rating @ 1.0 ms
- Maximum Limits Guaranteed on Six Electrical Parameters
- Package No Larger Than the Conventional 400 mW Package

#### Designer's Data for "Worst Case" Conditions

The Designer's Data sheets permit the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

#### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*DC Power Dissipation @ $T_L = 50^\circ\text{C}$ Derate above $50^\circ\text{C}$	$P_D$	1.0	Watt
		6.67	mW/ $^\circ\text{C}$
†DC Power Dissipation @ $T_L = 75^\circ\text{C}$ Lead Length = 3/8" Derate above $75^\circ\text{C}$	$P_D$	3.0	Watts
		24	mW/ $^\circ\text{C}$
*Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +200	$^\circ\text{C}$

#### MECHANICAL CHARACTERISTICS

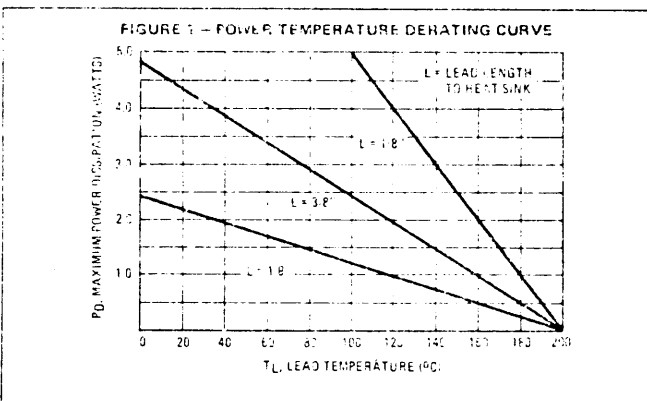
CASE: Mold free, transfer-molded, thermosetting plastic

FINISH: All external surfaces are corrosion resistant and leads are readily solderable and weldable.

POLARITY: Cathode indicated by polarity band. When operated in zener mode, cathode will be positive with respect to anode.

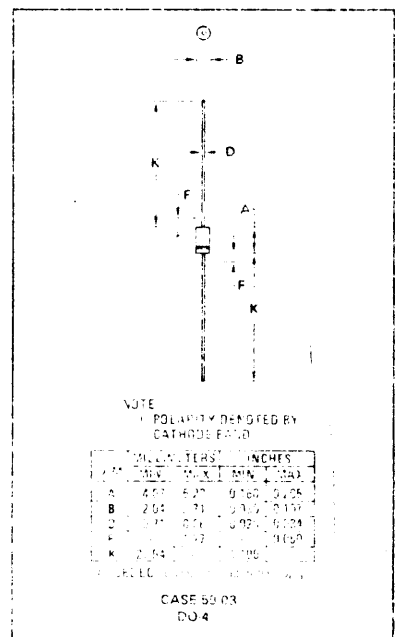
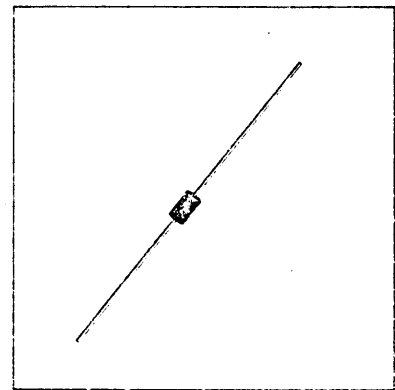
MOUNTING POSITION: Any

WEIGHT: 0.4 gram (approx)



\*Indicates JEDEC Registered Data

### 1.0 WATT ZENER REGULATOR DIODES 3.3-200 VOLTS



D COMPONENT DESCRIPTIONS  
D.1 DIODES

1N4743 cont'd

ELECTRICAL CHARACTERISTICS (TA = 25°C unless otherwise noted) \*V<sub>F</sub> = 1.5 V max, I<sub>F</sub> = 200 mA for all types

JEDEC Type No. (Note 1)	Motorola Type No. (Note 2)	*Nominal Zener Voltage V <sub>Z</sub> @ I <sub>ZT</sub> Volts (Note 2 & 3)	*Test Current I <sub>ZT</sub> mA	*Max Zener impedance (Note 4)			*Leakage Current		*Surge Current @ T <sub>A</sub> = 25°C I <sub>S</sub> - mA (Note 5)
				Z <sub>ZT</sub> @ I <sub>ZT</sub> Ohms	Z <sub>ZK</sub> @ I <sub>ZK</sub> Ohms	I <sub>ZK</sub> mA	I <sub>R</sub> μA Max @ V <sub>R</sub> Volts		
1N4728	1M3.3ZS10	3.3	76	10	400	1.0	100	1.0	1350
1N4729	1M3.6ZS10	3.6	64	10	400	1.0	100	1.0	1260
1N4730	1M3.9ZS10	3.9	54	9.0	400	1.0	50	1.0	1190
1N4731	1M4.1ZS10	4.3	58	9.0	400	1.0	10	1.0	1070
1N4732	1M4.7ZS10	4.7	53	8.0	500	1.0	10	1.0	970
1N4733	1M5.1ZS10	5.1	49	7.0	550	1.0	10	1.0	950
1N4734	1M5.6ZS10	5.6	45	5.0	500	1.0	10	2.0	910
1N4735	1M5.2ZS10	6.2	41	2.0	700	1.0	10	3.0	730
1N4736	1M6.8ZS10	6.8	37	3.5	700	1.0	10	4.0	660
1N4737	1M7.5ZS10	7.5	34	4.0	700	0.5	10	5.0	605
1N4738	1M8.2ZS10	8.2	31	4.5	700	0.5	10	6.0	550
1N4739	1M9.1ZS10	9.1	28	5.0	700	0.5	10	7.0	500
1N4740	1M10ZS10	10	25	7.0	700	0.25	10	7.6	454
1N4741	1M11ZS10	11	23	8.0	700	0.25	5.0	8.4	414
1N4742	1M12ZS10	12	21	9.0	700	0.25	5.0	9.1	390
1N4743	1M13ZS10	13	19	10	700	0.25	5.0	9.9	344
1N4744	1M15ZS10	15	17	14	700	0.25	5.0	11.4	304
1N4745	1M16ZS10	16	15.5	16	700	0.25	5.0	12.2	285
1N4746	1M18ZS10	18	14	20	750	0.25	5.0	13.7	250
1N4747	1M20ZS10	20	12.5	22	750	0.25	5.0	15.2	215
1N4748	1M22ZS10	22	11.5	23	750	0.25	5.0	16.7	205
1N4749	1M24ZS10	24	10.5	25	750	0.25	5.0	18.2	190
1N4750	1M27ZS10	27	9.5	35	750	0.25	5.0	20.6	170
1N4751	1M30ZS10	30	8.5	40	1000	0.25	5.0	22.8	150
1N4752	1M33ZS10	33	7.5	45	1000	0.25	5.0	25.1	135
1N4753	1M33ZS10	36	7.0	50	1000	0.25	5.0	27.4	125
1N4754	1M33ZS10	39	6.5	60	1000	0.25	5.0	29.7	115
1N4755	1M43ZS10	43	6.0	70	1500	0.25	5.0	32.7	110
1N4756	1M47ZS10	47	5.5	80	1500	0.25	5.0	35.8	95
1N4757	1M51ZS10	51	5.0	95	1500	0.25	5.0	38.3	90
1N4758	1M66ZS10	56	4.5	110	2000	0.25	5.0	42.5	80
1N4759	1M62ZS10	62	4.0	125	2000	0.25	5.0	47.1	70
1N4760	1M68ZS10	68	3.7	150	2000	0.25	5.0	51.7	65
1N4761	1M75ZS10	75	3.3	175	2000	0.25	5.0	56.0	60
1N4762	1M82ZS10	82	3.0	200	3000	0.25	5.0	62.2	55
1N4763	1M91ZS10	91	2.8	250	3000	0.25	5.0	69.2	50
1N4764	1M100ZS10	100	2.5	350	3000	0.25	5.0	76.0	45
-	1M110ZS10	110	2.3	450	4000	0.25	5.0	83.6	-
-	1M120ZS10	120	2.0	550	4500	0.25	5.0	91.2	-
-	1M130ZS10	130	1.9	700	5000	0.25	5.0	98.8	-
-	1M150ZS10	150	1.7	1000	6000	0.25	5.0	114.0	-
-	1M160ZS10	160	1.6	1100	6500	0.25	5.0	121.6	-
-	1M180ZS10	180	1.4	1200	7000	0.25	5.0	136.8	-
-	1M200ZS10	200	1.2	1500	8000	0.25	5.0	152.0	-

NOTE 1 - TOLERANCE AND TYPE NUMBER DESIGNATION

The JEDEC type numbers listed have a standard tolerance on the nominal zener voltage of ±10%. A standard tolerance of ±5% on individual units is also available and is indicated by suffixing "A" to the standard type number.

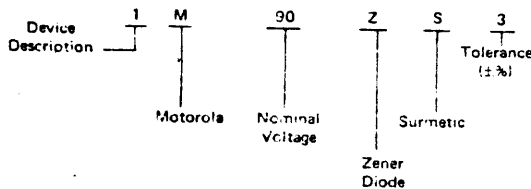
NOTE 2 - SPECIALS AVAILABLE INCLUDE:

(A) NOMINAL ZENER VOLTAGES BETWEEN THE VOLTAGES SHOWN AND TIGHTER VOLTAGE TOLERANCES: To designate units with zener voltages other than those assigned JEDEC numbers and/or tight voltage tolerances (±5%, ±3%, ±2%, ±1%), the Motorola type number should be used.

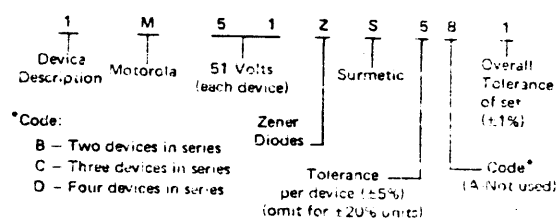
(B) MATCHED SETS: (Standard Tolerances are ±5.0%, ±3.0%, ±2.0%, ±1.0%).

Zener diodes can be obtained in sets consisting of two or more matched devices. The method for specifying such matched sets is similar to the one described in (A), except that two extra suffixes are added to the code number described.

These units are marked with code letters to identify the matched sets and, in addition, each unit in a set is marked with the same serial number, which is different for each set being ordered.



Example: 1M90ZS3



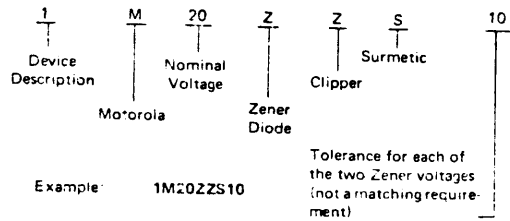
Example: 1M51ZS5B1

D COMPONENT DESCRIPTIONS  
 D.1 DIODES

1N4743 cont'd

(C) ZENER CLIPPERS. (Standard Tolerance  $\pm 10\%$  and  $\pm 5\%$ ).

Special clipper diodes with opposing Zener junctions built into the device are available by using the following nomenclature:



NOTE 3 - ZENER VOLTAGE ( $V_Z$ ) MEASUREMENT

Motorola guarantees the zener voltage when measured at 90 seconds while maintaining the lead temperature ( $T_L$ ) at  $30^\circ\text{C} \pm 1^\circ\text{C}$ ,  $\pm 8\%$  from the diode body.

NOTE 4 - ZENER IMPEDANCE ( $Z_Z$ ) DERIVATION

The zener impedance is derived from the 60 cycle ac voltage, which results when an ac current having an rms value equal to  $10\%$  of the dc zener current ( $I_{ZT}$  or  $I_{ZK}$ ) is superimposed on  $I_{ZT}$  or  $I_{ZK}$ .

NOTE 5 - SURGE CURRENT ( $I_r$ ) NON-REPETITIVE

The rating listed in the electrical characteristics table is maximum peak non-repetitive reverse surge current of 1/20 square wave or equivalent sine wave pulse of 1/120 second duration superimposed on the test current,  $I_{ZT}$ , per JEDEC registration, however, actual device capability is as described in Figures 4 and 5.

APPLICATION NOTE

Since the actual voltage available from a given zener diode is temperature dependent, it is necessary to determine junction temperature under any set of operating conditions in order to calculate its value. The following procedure is recommended:

Lead Temperature,  $T_L$ , should be determined from:

$$T_L = \theta_{LA} P_D + T_A$$

$\theta_{LA}$  is the lead-to ambient thermal resistance ( $^\circ\text{C}/\text{W}$ ) and  $P_D$  is the power dissipation. The value for  $\theta_{LA}$  will vary and depends on the device mounting method.  $\theta_{LA}$  is generally  $30-40^\circ\text{C}/\text{W}$  for the various clips and tie points in common use and for printed circuit board wiring.

The temperature of the lead can also be measured using a thermocouple placed on the lead as close as possible to the tie point. The thermal mass connected to the tie point is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady-state conditions are achieved. Using the measured value of  $T_L$ , the junction temperature may be determined by

$$T_J = T_L + \Delta T_{JL}$$

$\Delta T_{JL}$  is the increase in junction temperature above the lead temperature and may be found from Figure 2 for a train of power pulses ( $L = 3/8$  inch) or from Figure 3 for dc power.

$$\Delta T_{JL} = \theta_{JL} P_D$$

For worst-case design, using expected limits of  $I_Z$ , limits of  $P_D$  and the extremes of  $T_J$  ( $\Delta T_J$ ) may be estimated. Changes in voltage,  $V_Z$ , can then be found from

$$\Delta V = \theta_{VZ} \Delta T_J$$

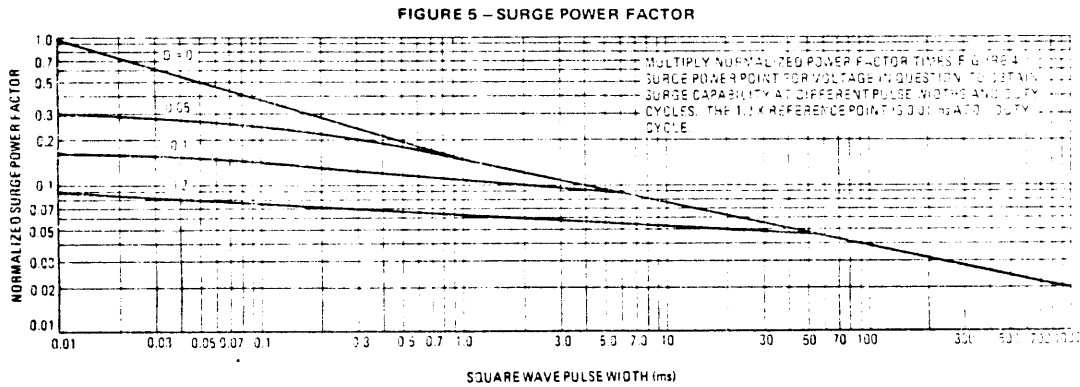
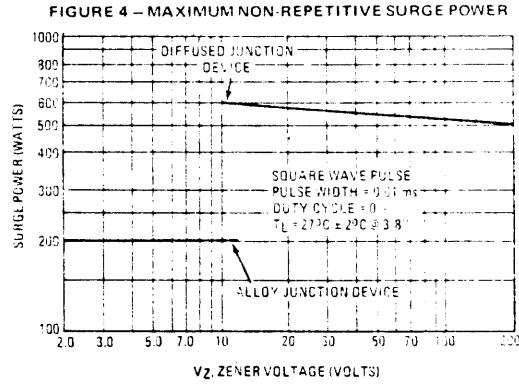
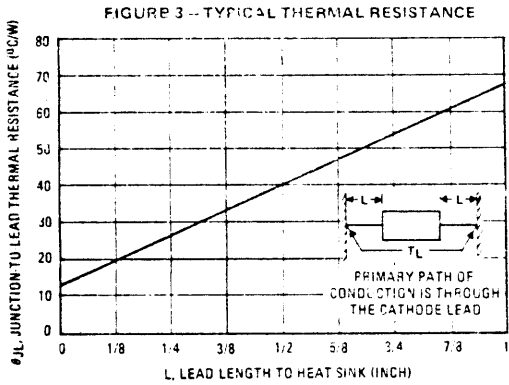
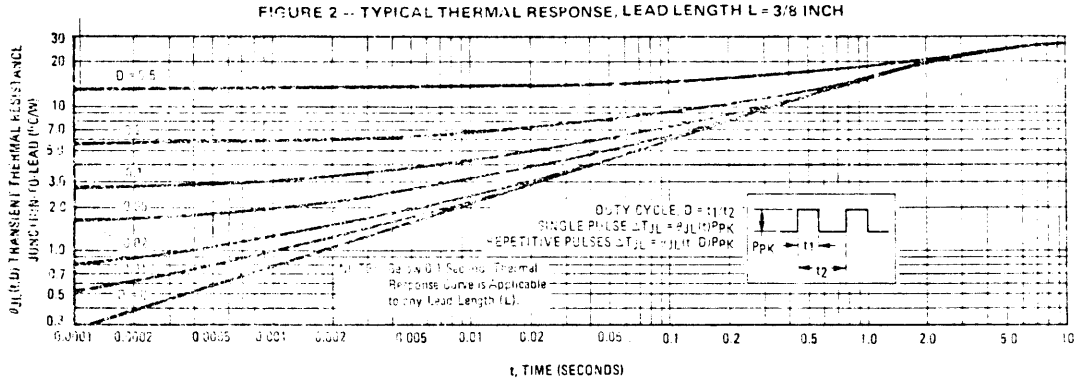
$\theta_{VZ}$ , the zener voltage temperature coefficient, is found from Figures 6 and 7.

Under high power pulse operation, the zener voltage will vary with time and may also be affected significantly by the zener resistance. For best regulation, keep current excursions as low as possible.

Data of Figure 2 should not be used to compute surge capability. Surge limitations are given in Figure 4. They are lower than would be expected by considering only junction temperature, as current crowding effects cause temperatures to be extremely high in small spots resulting in device degradation should the limits of Figure 4 be exceeded.

D COMPONENT DESCRIPTION  
 D.1 DIODES

1N4743 cont'd



D COMPONENT DESCRIPTIONS  
 D.1 DIODES

1N4743 cont'd

TEMPERATURE COEFFICIENTS AND VOLTAGE REGULATION  
 (90% OF THE UNITS ARE IN THE RANGES INDICATED)

FIGURE 6 - TEMPERATURE COEFFICIENT-RANGE FOR UNITS TO 12 VOLTS

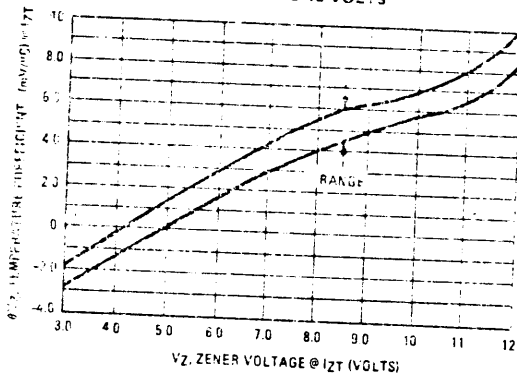


FIGURE 7 - TEMPERATURE COEFFICIENT-RANGE FOR UNITS 10 TO 200 VOLTS

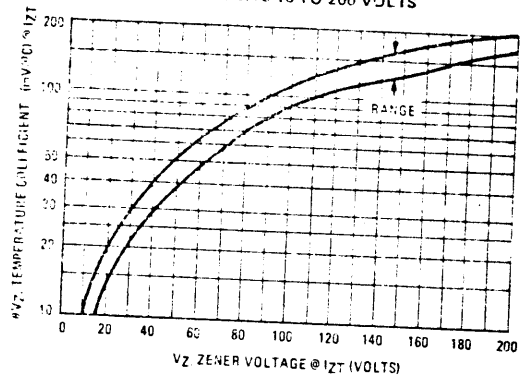


FIGURE 8 - VOLTAGE REGULATION

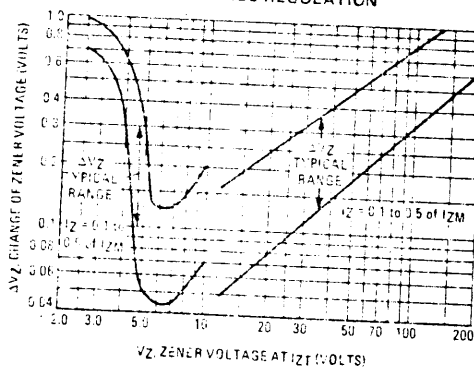
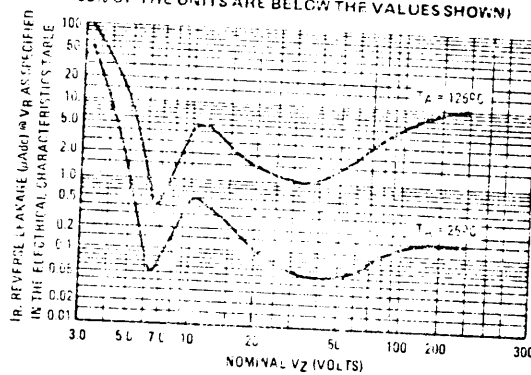


FIGURE 9 - MAXIMUM REVERSE LEAKAGE  
 (95% OF THE UNITS ARE BELOW THE VALUES SHOWN)



# D COMPONENT DESCRIPTIONS

## D.1 DIODES

1N 5225-B

**500 MILLIWATT SURMETIC 20 SILICON ZENER DIODES  
(SILICON OXIDE PASSIVATED)**

In answer to the Circuit Design and Component Engineers' many requests - A complete new series of Zener Diodes in the popular DO-204AA case with higher ratings, tighter limits, better operating characteristics and a full set of designers' curves that reflect the superior capabilities of silicon-oxide-passivated junctions. All this in an axial-lead, transfer-molded plastic package offering protection in all common environmental conditions.

- Proven Capability to MIL-S-19500 Specifications
- 10 Watt Surge Rating
- Weldable Leads
- Maximum Limits Guaranteed on Six Electrical Parameters

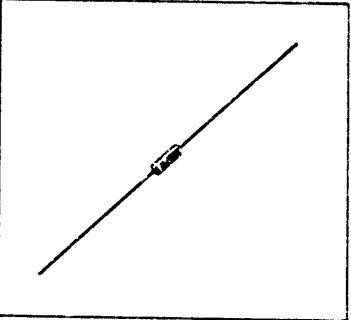
{ .5M2.4ZS10 thru .5M200ZS10 }  
 { 1N5221A thru 1N5281A }  
 { .5M2.4ZS5 thru .5M200ZS5 }  
 { 1N5221B thru 1N5281B }

**500 MILLIWATT  
ZENER REGULATOR  
DIODES**

**2.4 - 200 VOLTS**

**MAXIMUM RATINGS**

Junction and Storage Temperature: -65 to +200°C  
 Lead Temperature not less than 1/16" from the case for 10 seconds: 230°C  
 DC Power Dissipation: 500 mW @ T<sub>L</sub> = 75°C, Lead Length = 3/8"  
 (Derate 4.0mW/°C above 75°C)  
 Surge Power: 10 Watts (Non-recurrent square wave @ PW = 8.3 ms, T<sub>r</sub> = 55°C, Figure 16)

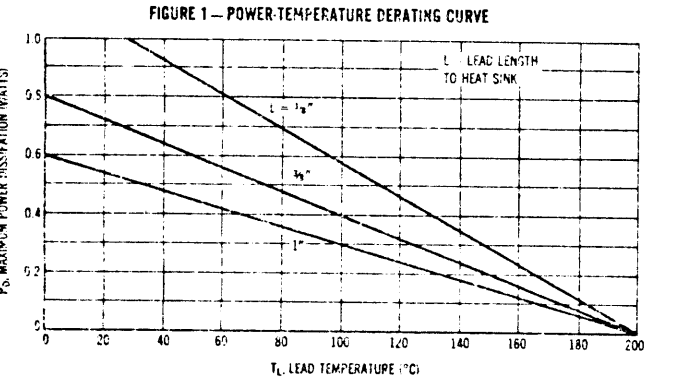


**MECHANICAL CHARACTERISTICS**

CASE: Void free, transfer molded, thermosetting plastic.  
 FINISH: All external surfaces are corrosion resistant. Leads are readily solderable and weldable.  
 POLARITY: Cathode indicated by color band. When operated in zener mode, cathode will be positive with respect to anode.  
 MOUNTING POSITION: Any.  
 WEIGHT: 0.12 gram (approximately).

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	5.84	2.52	0.230	0.100
B	2.15	0.12	0.085	0.107
C	2.44	0.54	0.018	0.022
F	1.27	0.12	0.050	0.048
K	1.20	0.12	0.048	0.048

All JEDEC dimensions and notes apply  
**CASE 51-02**  
**DO-7**



# D COMPONENT DESCRIPTIONS

## D.1 DIODES

1N 5225-B cont'd

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted). Based on dc measurements at thermal equilibrium. Lead length =  $\frac{3}{8}$ " thermal resistance of heat sink =  $30^\circ\text{C/W}$ .  $V_Z \approx 1.1 \text{ Max @ } I_Z = 200 \text{ mA}$  for all types.

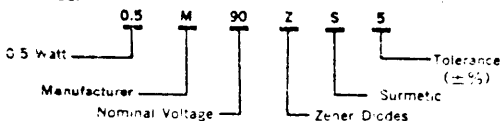
JEDEC Type No. (Note 1)	Nominal Zener Voltage $V_Z @ I_{ZT}$ (Volts) (Note 2)	Test Current $I_{ZT}$ mA	Max Zener Impedance A & B Suffix Only		Max Reverse Leakage Current			Max Zener Voltage Temp. Coeff. (A & B Suffix Only) $\%_{V_Z} / ^\circ\text{C}$ (Note 3)	
			$Z_{ZT} @ I_{ZT}$ Ohms	$Z_{ZK} @ I_{ZK} = 0.25 \text{ mA}$ Ohms	A & B Suffix Only		Non Suffix $I_R @ V_R$ Used For Suffix A $\mu\text{A}$		
					$I_R @ V_R$ $\mu\text{A}$	$V_R$ Volts			
1N5221	2.4	20	30	1200	100	0.35	1.0	200	-0.045
1N5222	2.5	20	30	1200	100	0.35	1.0	200	-0.045
1N5223	2.7	20	30	1300	75	0.35	1.0	150	-0.060
1N5224	2.8	20	30	1400	75	0.35	1.0	150	-0.080
1N5225	2.9	20	29	1500	50	0.35	1.0	100	-0.075
1N5226	3.0	20	28	1600	25	0.35	1.0	100	-0.070
1N5227	3.1	20	24	1700	15	0.35	1.0	100	-0.065
1N5228	3.3	20	23	1800	10	0.45	1.0	75	-0.060
1N5229	3.6	20	22	2000	5.0	0.35	1.0	50	-0.055
1N5230	4.7	20	19	1900	5.0	1.9	2.0	50	-0.030
1N5231	5.1	20	17	1600	5.0	1.9	2.0	50	-0.030
1N5232	5.6	20	11	1600	5.0	2.9	3.0	50	-0.018
1N5233	6.0	20	7.0	1600	5.0	3.1	3.5	50	-0.038
1N5234	6.2	20	7.0	1300	5.0	3.8	4.0	50	-0.045
1N5235	6.4	20	5.0	750	3.0	4.8	5.0	30	-0.050
1N5236	7.5	20	5.0	500	3.0	5.7	6.0	30	-0.058
1N5237	8.2	20	8.0	600	3.0	6.2	6.5	30	-0.062
1N5238	8.7	20	8.0	600	3.0	6.2	6.5	30	-0.065
1N5239	9.1	20	10	600	3.0	6.7	7.0	30	-0.068
1N5240	10	20	17	600	3.0	7.6	8.0	30	-0.075
1N5241	11	20	20	600	2.0	8.0	8.4	30	-0.076
1N5242	12	20	30	600	1.0	9.7	9.1	10	-0.077
1N5243	13	9.5	13	600	0.5	9.4	9.9	10	-0.079
1N5244	14	3.0	15	600	0.1	9.5	10	10	-0.082
1N5245	15	6.5	16	600	0.1	10.5	11	10	-0.082
1N5246	16	7.8	17	600	0.1	11.4	12	10	-0.083
1N5247	17	7.4	19	600	0.1	12.4	13	10	-0.084
1N5248	18	7.0	21	600	0.1	13.3	14	10	-0.085
1N5249	19	6.6	23	600	0.1	13.3	14	10	-0.086
1N5250	20	6.2	25	600	0.1	14.3	15	10	-0.085
1N5251	22	5.6	29	600	0.1	16.2	17	10	-0.087
1N5252	24	5.2	33	600	0.1	17.1	18	10	-0.088
1N5253	25	5.0	35	600	0.1	18.1	19	10	-0.089
1N5254	27	4.8	41	600	0.1	20	21	10	-0.090
1N5255	28	4.5	44	600	0.1	20	21	10	-0.091
1N5256	30	4.2	49	600	0.1	22	23	10	-0.091
1N5257	33	3.0	38	700	0.1	24	25	10	-0.092
1N5258	36	3.4	39	700	0.1	26	27	10	-0.093
1N5259	38	3.2	43	800	0.1	29	30	10	-0.094
1N5260	42	3.0	93	900	0.1	31	33	10	-0.095
1N5261	47	2.7	105	1200	0.1	34	36	10	-0.095
1N5262	51	2.5	125	1100	0.1	37	39	10	-0.096
1N5263	56	2.2	150	1300	0.1	41	42	10	-0.096
1N5264	60	2.1	170	1400	0.1	44	46	10	-0.097
1N5265	62	2.0	185	1400	0.1	45	47	10	-0.097
1N5266	68	1.8	230	1600	0.1	49	52	10	-0.097
1N5267	75	1.7	270	1700	0.1	53	56	10	-0.098
1N5268	82	1.5	330	2000	0.1	59	62	10	-0.098
1N5269	87	1.4	370	2400	0.1	65	68	10	-0.099
1N5270	91	1.4	400	2500	0.1	66	69	10	-0.099
1N5271	100	1.3	500	2900	0.1	72	76	10	-0.100
1N5272	110	1.1	750	3800	0.1	80	84	10	-0.100
1N5273	120	1.0	900	4200	0.1	80	82	10	-0.100
1N5274	130	0.95	1100	4700	0.1	94	99	10	-0.100
1N5275	14	0.90	1300	4700	0.1	101	106	10	-0.100
1N5276	150	0.85	1500	5000	0.1	108	114	10	-0.100
1N5277	160	0.80	1700	5300	0.1	116	122	10	-0.100
1N5278	170	0.74	1900	5500	0.1	123	129	10	-0.100
1N5279	180	0.68	2200	6000	0.1	130	137	10	-0.100
1N5280	190	0.63	2400	6200	0.1	137	144	10	-0.100
1N5281	200	0.65	2500	7000	0.1	144	152	10	-0.100

### NOTE 1 — TOLERANCE AND VOLTAGE DESIGNATION

**Tolerance designation** — The JEDEC type numbers shown indicate a tolerance of  $\pm 10\%$  with guaranteed limits on only  $V_Z$ ,  $I_R$  and  $V_R$  as shown in the above table. Units with guaranteed limits on all six parameters are indicated by suffix "A" for  $\pm 10\%$  tolerance and suffix "B" for  $\pm 5\%$  units.

**Non-Standard voltage designation** — To designate units with zener voltages other than those assigned JEDEC numbers, the type number should be used.

**EXAMPLE:**



### NOTE 2 — SPECIAL SELECTIONS AVAILABLE INCLUDE:

1 — Nominal zener voltages between those shown.

2 — Matched sets (Standard Tolerances are  $\pm 5.0\%$ ,  $\pm 3.0\%$ ,  $\pm 2.0\%$ ,  $\pm 1.0\%$ ) depending on voltage per device.

a. Two or more units for series connection with specified tolerance on total voltage. Such matched sets make zener voltages in excess of 250 volts possible as well as providing lower temperature coefficients, lower dynamic impedance and greater power handling ability.

b. Two or more units matched to one another with any specified tolerance.

3 — Tight voltage tolerances: 1.0%, 2.0%, 3.0%.

### NOTE 3 — TEMPERATURE COEFFICIENT ( $\theta_{VZ}$ )

Test conditions for temperature coefficient are as follows:

a.  $I_{ZT} = 7.5 \text{ mA}$ ,  $T_1 = 25^\circ\text{C}$ .

$T_2 = 125^\circ\text{C}$  (1N5221A, B thru 1N5242A, B)

b.  $I_{ZT} = \text{Rated } I_{ZT}$ ,  $T_1 = 25^\circ\text{C}$ .

$T_2 = 125^\circ\text{C}$  (1N5243A, B thru 1N5281A, B)

Device to be temperature stabilized with current applied prior to reading breakdown voltage at the specified ambient temperature.



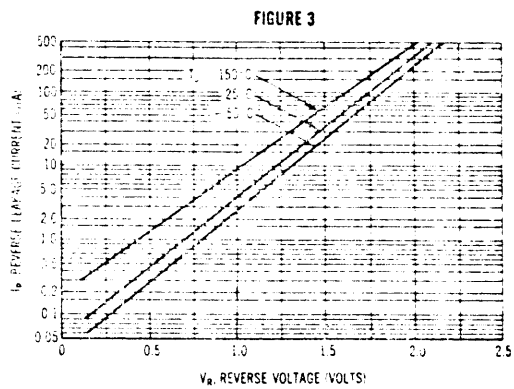
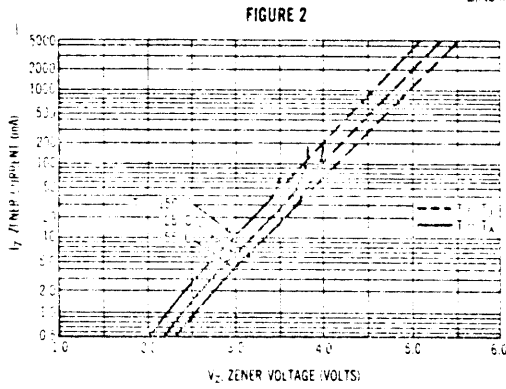
D COMPONENT DESCRIPTIONS  
 D.1 DIODES

1N 5225-B cont'd

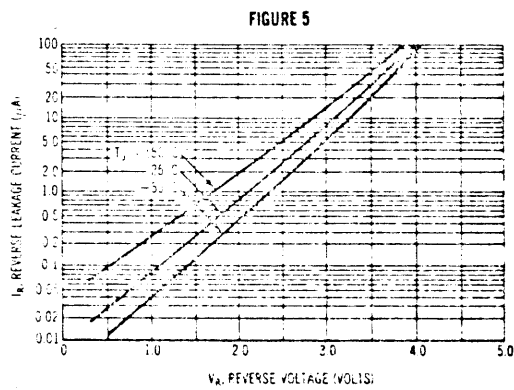
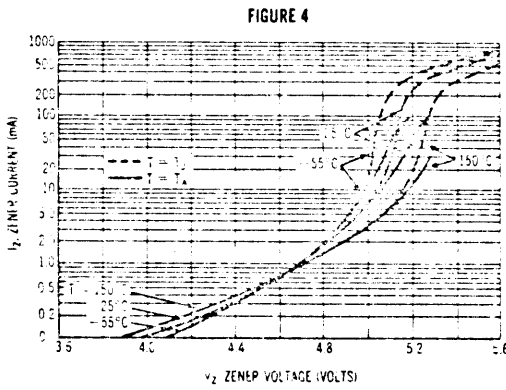
TYPICAL REVERSE CHARACTERISTICS FOR SELECTED ZENER DIODES

Curves marked  $T_1$  were obtained from pulse tests; measurements at thermal equilibrium (lead length = 1/4"); thermal resistance of heat sink = 30°C/W. Curves marked  $T_2$  were obtained from pulse tests; mounting conditions are not a factor.

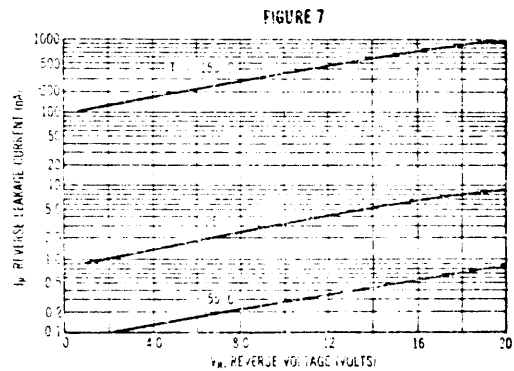
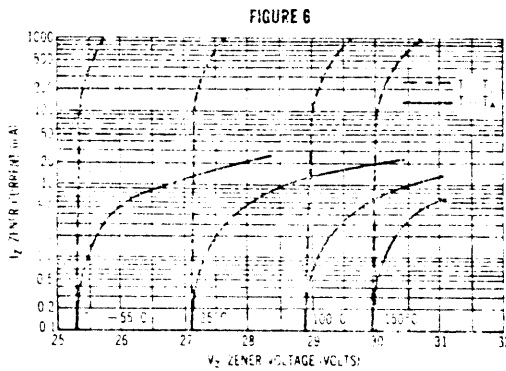
$V_{Z(Nominal)} = 3.3$  Volts



$V_{Z(Nominal)} = 5.1$  Volts



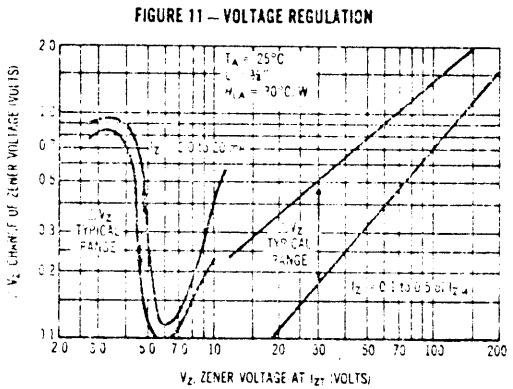
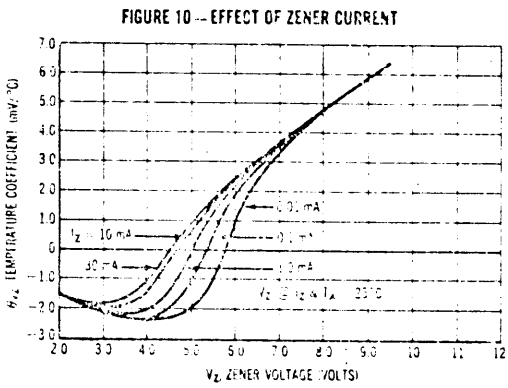
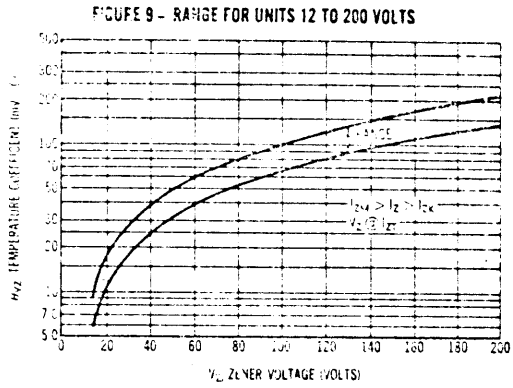
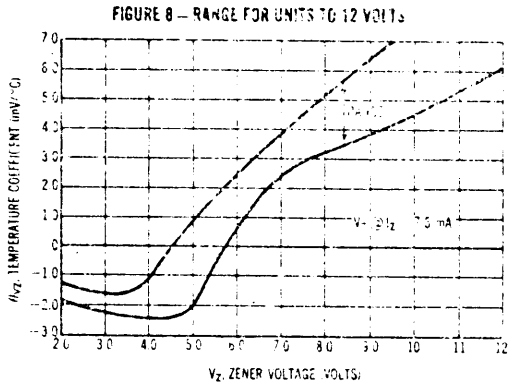
$V_{Z(Nominal)} = 27$  Volts



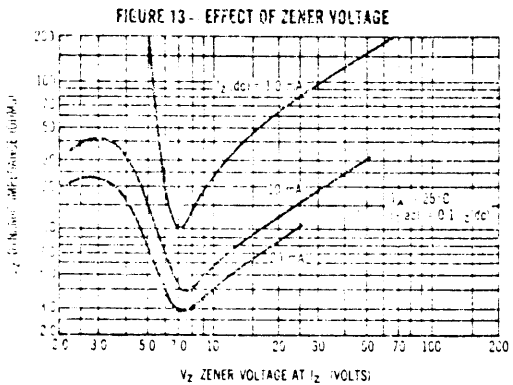
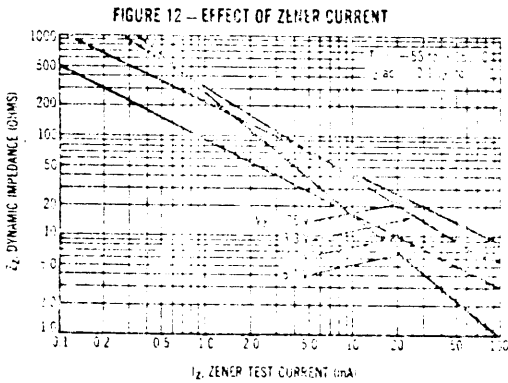
D COMPONENT DESCRIPTIONS  
 D.1 DIODES

1N 5225-B cont'd

TEMPERATURE COEFFICIENTS AND VOLTAGE REGULATION  
(30% of the units are in the range indicated)



TYPICAL ZENER IMPEDANCE



D COMPONENT DESCRIPTIONS  
 D.1 DIODES

1N 5225-B cont'd

FIGURE 14 — TYPICAL THERMAL RESPONSE

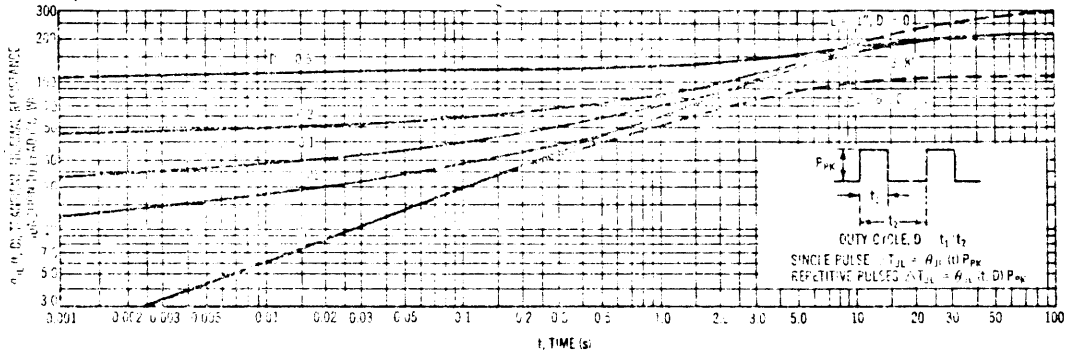
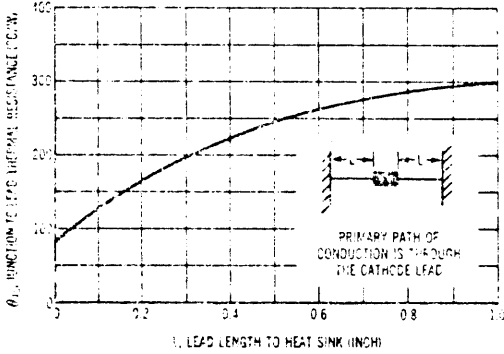


FIGURE 15 — TYPICAL THERMAL RESISTANCE



APPLICATION NOTE

Since the actual voltage available from a given zener diode is temperature dependent, it is necessary to determine junction temperature under any set of operating conditions in order to calculate its value. The following procedure is recommended:

Lead Temperature,  $T_L$ , should be determined from:  
 $T_L = \theta_{JA} P_D + T_A$

$\theta_{JA}$  is the lead to ambient thermal resistance and  $P_D$  is the power dissipation.  $\theta_{JA}$  is generally 30-40°C/W for the various clips and the points in common use and for printed circuit board wiring.

Junction Temperature,  $T_J$ , may be found from:

$$T_J = T_L + \Delta T_{JL}$$

$\Delta T_{JL}$  is the increase in junction temperature above the lead temperature and may be found from Figure 14 for a train of power pulses or from Figure 15 for dc power.

For worst case design, using expected limits of  $t_p$ , limits of  $P_D$  and the extremes of  $T_L$ , ( $\Delta T_{JL}$ ) may be estimated. Changes in voltage,  $\Delta V_Z$ , can then be found from:

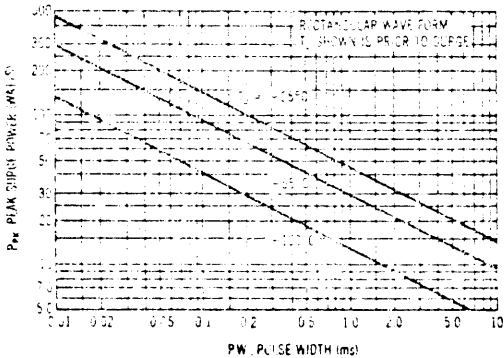
$$\Delta V = \theta_{VZ} \Delta T_J$$

$\theta_{VZ}$ , the zener voltage temperature coefficient, is found from Figures 8, 9, and 10.

Under high power pulse operation, the zener voltage will vary with time and may also be affected significantly by the zener resistance. For best regulation, use short leads, especially to the cathode, and keep current excursions as low as possible.

Data of Figure 14 should not be used to compute surge capability. Surge limitations are given in Figure 16. They are lower than would be expected by using only junction temperature, as current crowding effects cause temperatures to be extremely high in small spots resulting in device degradation should the limits of Figure 16 be exceeded.

FIGURE 16 — MAXIMUM NON-REPETITIVE SURGE POWER — Note 4



Note 4.

This curve is directly readable when applied to devices with nominal voltages in the 11 to 200 Volt range. For devices with nominal voltages in the 2.4 to 10 Volt range, multiply the appropriate peak surge power reading by 0.4.

D COMPONENT DESCRIPTIONS  
 D.1 DIODES

1N 5225-B cont'd

FIGURE 17 - TYPICAL CAPACITANCE

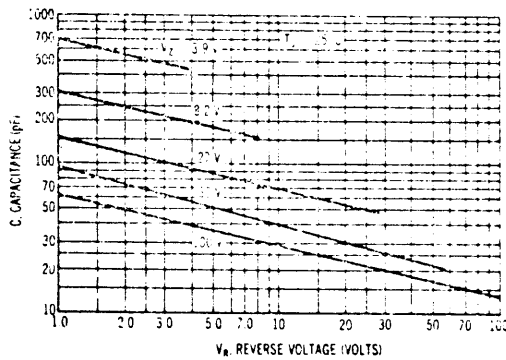


FIGURE 18 - TYPICAL FORWARD CHARACTERISTICS

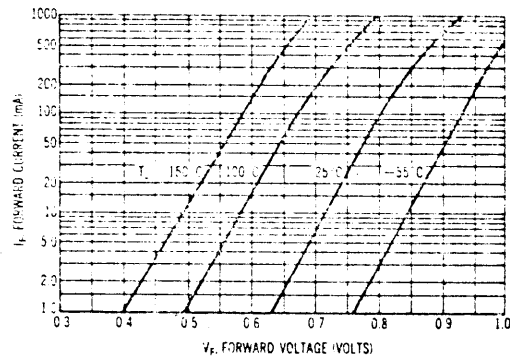


FIGURE 19 - TYPICAL NOISE DENSITY

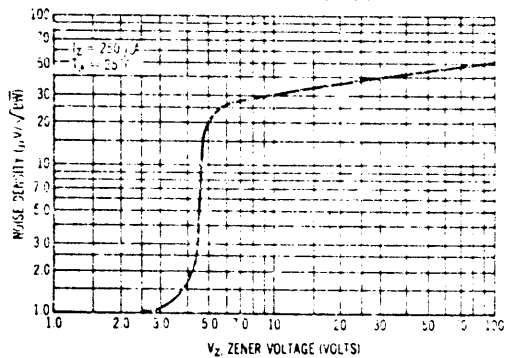
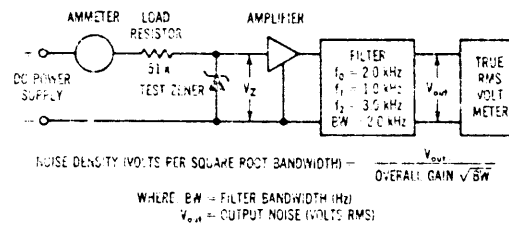


FIGURE 20 - NOISE DENSITY MEASUREMENT METHOD



The input voltage and load resistance are high so that the zener diode is driven from a constant current source. The amplifier is low noise so that the amplifier noise is negligible compared to that of the test zener. The filter bandwidth is known so that the noise density can be calculated from the formula shown. The data of Figure 19 and the formula can also be used to find noise for any system bandwidth.

**D COMPONENT DESCRIPTIONS**  
**D.1 DIODES**

1N5338-B, 1N5339-B, 1N5348-B, 1N5349

**5.0 WATT SURMETIC 40 SILICON ZENER DIODES  
 (SILICON OXIDE PASSIVATED)**

... a complete new series of 5.0 Watt Zener Diodes with tight limits and better operating characteristics that reflect the superior capabilities of silicon-oxide-passivated junctions. All this in an axial-lead, transfer-molded plastic package offering protection in all common environmental conditions.

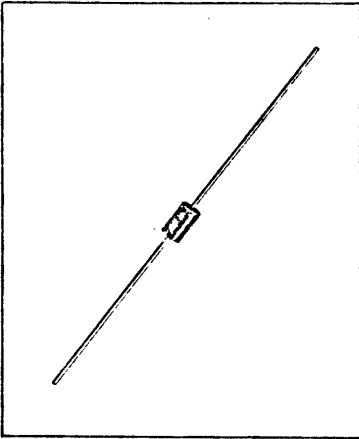
- Up to 180 Watt Surge Rating @ 8.3 ms
- Maximum Limits Guaranteed on Seven Electrical Parameters

(5M3.3ZS10 thru 5M200ZS10)  
 1N5333A thru 1N5388A  
 (5M3.3ZS5 thru 5M200ZS5)  
 1N5333B thru 1N5388B

**5.0 WATT  
 ZENER REGULATOR DIODES**  
**3.3 - 200 VOLTS**

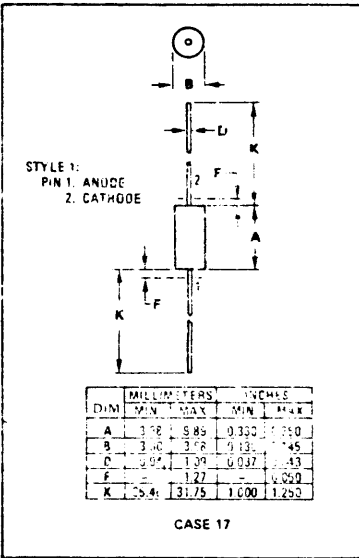
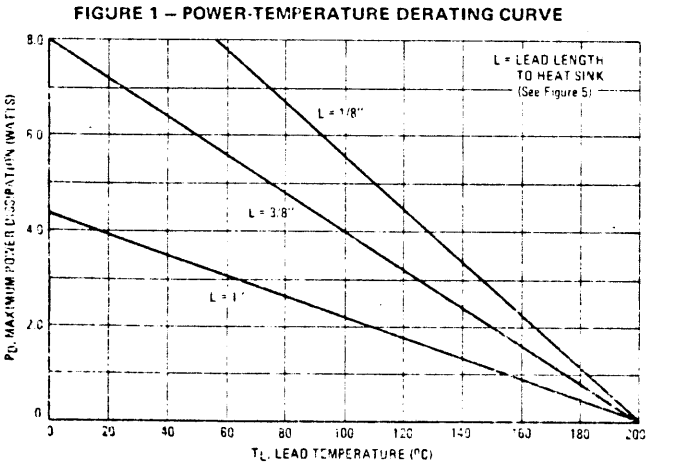
**MAXIMUM RATINGS**

Junction and Storage Temperature: -65 to +200°C  
 Lead Temperature not less than 1/16" from the case for 10 seconds: 230°C  
 D.C. Power Dissipation: 5.0 W @ T<sub>L</sub> = 75°C, Lead Length = 3/8"  
 (Derate 40 mW/°C above 75°C)



**MECHANICAL CHARACTERISTICS**

CASE: Void-free, transfer-molded, thermosetting plastic  
 FINISH: All external surfaces are corrosion resistant. Leads are readily solderable  
 POLARITY: Cathode indicated by color band. When operated in zener mode, cathode will be positive with respect to anode.  
 MOUNTING POSITION: Any  
 WEIGHT: 0.7 gram (approx)



D COMPONENT DESCRIPTIONS  
D.1 DIODES

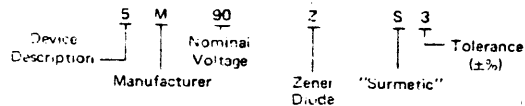
1N5338-B, 1N5339-B, 1N5348-B, 1N5349-B cont'd

ELECTRICAL CHARACTERISTICS (For 25°C unless otherwise noted;  $V_F = 1.2$  Max;  $I_F = 1.0$  A for all types)

JEDEC Type No. (Note 1 & 2)	Nominal Zener Voltage $V_Z$ Volts (Note 3)	Test Current $I_{ZT}$ mA	Max Zener Impedance A & B Suffix Only		Max Reverse Leakage Current			Applies to all Suffix	A & B Suffix Only	Maximum Regulator Current $I_{ZM}$ mA		
			$Z_{ZT}$ @ $I_{ZT}$ Ohms (Note 3)	$Z_{ZK}$ @ $I_{ZK} = 1.0$ mA (Note 3)	$I_R$ @ $V_R$ Volts	Non & A Suffix	B-Suffix				Max Surge Current i, Amps (Note 4)	Max Voltage Regulation $V_Z$ Volts (Note 5)
1N5335	3.0	380	3.0	40	300	1.0	1.0	20.0	0.85	1440		
1N5334	3.5	350	2.5	50	150	1.0	1.0	18.7	0.80	1320		
1N5335	3.9	320	2.0	500	50	1.0	1.0	17.6	0.54	1220		
1N5336	4.3	250	2.0	500	10	1.0	1.0	16.4	0.49	1100		
1N5337	4.7	260	2.0	450	5.0	1.0	1.0	15.3	0.44	1010		
1N5338	5.1	240	1.5	400	1.0	1.0	1.0	14.4	0.39	930		
1N5339	5.6	230	1.0	400	1.0	2.0	2.0	13.4	0.25	665		
1N5340	6.0	250	1.0	300	1.0	3.0	3.0	12.7	0.19	790		
1N5341	6.2	200	1.0	250	1.0	3.0	3.0	12.4	0.10	765		
1N5342	6.3	175	1.0	200	10	4.9	5.2	11.5	0.15	700		
1N5343	7.0	175	1.5	200	10	5.4	5.7	10.7	0.15	630		
1N5344	8.2	150	1.5	200	10	5.9	6.2	10.0	0.20	350		
1N5345	8.7	150	2.0	2.1	10	6.3	6.5	9.5	0.20	5-5		
1N5346	9.1	150	2.0	150	7.5	6.6	6.9	9.2	0.12	690		
1N5347	10	125	2.0	125	5.0	7.2	7.6	8.6	0.22	475		
1N5348	11	125	2.5	125	5.0	8.0	8.4	8.0	0.15	430		
1N5349	12	100	2.5	120	2.0	9.6	9.1	7.5	0.25	295		
1N5350	13	100	2.5	100	1.0	9.4	9.9	7.0	0.25	365		
1N5351	14	100	2.5	75	1.0	10.1	10.6	6.7	0.25	340		
1N5352	15	75	2.5	75	1.0	10.6	11.5	6.3	0.25	315		
1N5353	16	75	2.5	75	1.0	11.5	12.2	6.0	0.30	295		
1N5354	17	70	2.5	75	0.5	12.2	12.3	5.5	0.35	280		
1N5355	18	65	2.5	75	0.5	13.0	13.7	5.5	0.40	264		
1N5356	19	65	3.0	75	0.5	13.7	14.4	5.3	0.40	250		
1N5357	20	63	3.0	75	0.5	14.4	15.2	5.1	0.40	227		
1N5358	22	50	3.5	75	0.5	16.3	16.7	4.7	0.45	215		
1N5359	24	50	3.5	100	0.5	17.3	18.0	4.4	0.55	192		
1N5360	25	30	4.0	110	0.5	18.0	19.7	4.2	0.55	180		
1N5361	27	50	5.0	150	0.5	19.4	20.5	4.1	0.60	176		
1N5362	28	50	6.0	125	0.5	20.1	21.2	3.9	0.60	170		
1N5363	30	40	6.0	140	0.5	21.6	22.8	3.7	0.60	158		
1N5364	33	40	11	150	0.5	23.6	25.1	3.5	0.50	144		
1N5365	36	30	11	160	0.5	25.0	27.4	3.3	0.55	132		
1N5366	39	20	14	170	0.5	25.1	29.7	3.1	0.65	122		
1N5367	43	30	20	190	0.5	31.0	32.7	2.8	0.70	116		
1N5368	47	25	25	200	0.5	33.0	37.8	2.7	0.50	100		
1N5369	51	25	27	250	0.5	35.7	41.8	2.5	0.50	92.0		
1N5370	55	20	25	240	0.5	40.7	42.6	2.3	1.00	86.0		
1N5371	60	20	10	250	0.5	43.0	45.5	2.2	1.21	79.0		
1N5372	63	20	12	400	0.5	44.8	47.1	2.1	1.35	70.0		
1N5373	68	20	44	290	0.5	49.0	51.7	2.0	1.51	70.0		
1N5374	75	20	45	320	0.5	54.0	56.0	1.9	1.80	63.0		
1N5375	82	15	65	320	0.5	59.0	62.2	1.8	1.80	59.0		
1N5376	87	15	75	360	0.5	62.0	65.3	1.7	2.00	54.5		
1N5377	91	15	75	360	0.5	65.0	69.2	1.6	2.20	52.5		
1N5378	100	12	90	390	0.5	72.0	76.0	1.5	2.50	47.5		
1N5379	110	12	125	1900	0.5	79.2	82.8	1.4	2.50	43.0		
1N5380	120	10	170	1150	0.5	86.4	89.2	1.3	2.50	39.5		
1N5381	130	10	190	1250	0.5	92.6	95.4	1.2	2.50	36.5		
1N5382	140	6.0	230	1500	0.5	101	106	1.2	2.50	34.0		
1N5383	150	6.0	330	1700	0.5	108	114	1.1	3.00	31.5		
1N5384	160	6.0	340	1850	0.5	115	122	1.1	3.00	29.4		
1N5385	170	4.0	380	1750	0.5	123	129	1.0	3.00	28.0		
1N5386	180	5.0	430	1750	0.5	130	137	1.0	4.00	25.4		
1N5387	190	5.0	450	1550	0.5	137	144	0.9	5.00	25.0		
1N5388	200	5.0	4.0	160	0.5	144	152	0.9	5.00	23.5		

NOTE 1 - TOLERANCE AND VOLTAGE DESIGNATION

TOLERANCE DESIGNATION - The JEDEC type numbers shown indicate a tolerance of  $\pm 20\%$  with guaranteed limits on only  $V_Z$ ,  $I_R$ , and  $V_F$  as shown in the electrical characteristics table. Units with guaranteed limits on all zener parameters are indicated by suffix "A" for  $\pm 10\%$  tolerance and suffix "B" for  $\pm 5.0\%$  units.



Example 5M90ZS3

NOTE 2 - SPECIALS AVAILABLE INCLUDE:

(A) NOMINAL ZENER VOLTAGES BETWEEN THE VOLTAGES SHOWN AND TIGHTER VOLTAGE TOLERANCES. To designate units with zener voltages other than those assigned JEDEC numbers and/or tight voltage tolerances ( $\pm 1.3\%$ ,  $\pm 2\%$ ,  $\pm 1\%$ ), the Mfg. type number should be used.

(B) MATCHED SETS (Standard Tolerances are  $\pm 5.0\%$ ,  $\pm 2.0\%$ ,  $\pm 1.0\%$ ).

Zener diodes can be obtained in sets consisting of two or more matched devices. The method for specifying such matched sets is similar to the one described in (A) for specifying units.

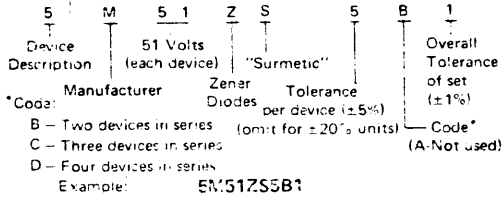
# D COMPONENT DESCRIPTIONS

## D. 1 DIODES

### 1N5338-B, 1N5339-B, 1N5348-B, 1N5349-B cont'd

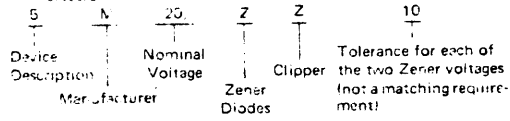
with a special voltage and/or tolerance except that two extra suffixes are added to the code number described.

These units are marked with code letters to identify the matched sets and in addition, each unit in a set is marked with the same serial number, which is different for each set being ordered.



(C) ZENER CLIPPER (Standard Tolerance  $\pm 10\%$  and  $\pm 5\%$ ).

Special clipper diodes with opposing Zener junctions built into the device are available by using the following nomenclature:



### NOTE 3 - ZENER VOLTAGE ( $V_Z$ ) AND IMPEDANCE ( $Z_{ZT}$ & $Z_{ZK}$ )

Test conditions for Zener voltage and impedance are as follows:  $I_Z$  is applied  $40 \pm 10$   $\mu$ s prior to reading. Mounting contacts are

located  $3/8"$  to  $1/2"$  from the inside edge of mounting clips to the body of the diode ( $T_A = 25^\circ\text{C} \pm 8^\circ\text{C}$ ).

### NOTE 4 - SURGE CURRENT ( $I_P$ )

Surge current is specified as the maximum allowable peak, non-recurrent square-wave current with a pulse width, PW, of 8.3 ms. The data given in Figure 6 may be used to find the maximum surge current for a square wave of any pulse width between 1.0 ms and 1000 ms by plotting the applicable points on logarithmic paper. Examples of this, using the 3.3 V and 200 V zeners, are shown in Figure 7. Mounting contact located as specified in Note 3. ( $T_A = 25^\circ\text{C} \pm 8^\circ\text{C}$ ).

### NOTE 5 - VOLTAGE REGULATION ( $\Delta V_Z$ )

Test conditions for voltage regulation are as follows:  $V_Z$  measurements are made at  $10\%$  and then at  $50\%$  of the  $I_Z$  max value listed in the electrical characteristics table. The test currents are the same for the  $5\%$  and  $10\%$  tolerance devices. The test current time duration for each  $V_Z$  measurement is  $40 \pm 10$  ms. ( $T_A = 25^\circ\text{C} \pm 8^\circ\text{C}$ ). Mounting contact located as specified in Note 3.

### NOTE 6 - MAXIMUM REGULATOR CURRENT ( $I_{ZM}$ )

The maximum current shown is based on the maximum voltage of a  $5\%$  type unit, therefore, it applies only to the B suffix device. The actual  $I_{ZM}$  for any device may not exceed the value of 5.0 watts divided by the actual  $V_Z$  of the device.  $T_L = 75^\circ\text{C}$  at  $3/8"$  maximum from the device body.

## TEMPERATURE COEFFICIENTS

FIGURE 2 - TEMPERATURE COEFFICIENT-RANGE FOR UNITS 3.0 TO 10 VOLTS

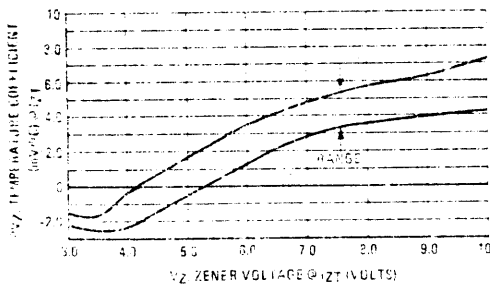


FIGURE 3 - TEMPERATURE COEFFICIENT-RANGE FOR UNITS 10 TO 220 VOLTS

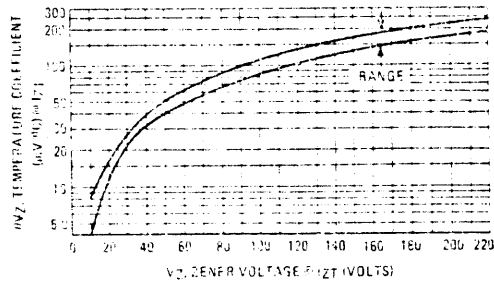
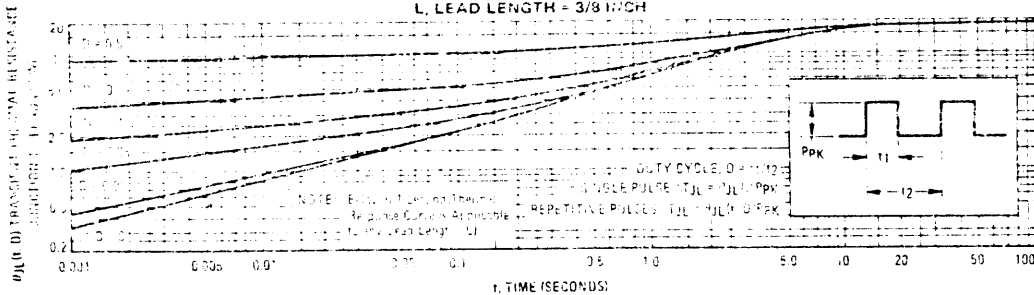


FIGURE 4 - TYPICAL THERMAL RESPONSE  
L, LEAD LENGTH = 3/8 INCH



D COMPONENT DESCRIPTIONS  
D.1 DIODES

1N5338-B, 1N5339-B, 1N5348-B, 1N5349-B cont'd

FIGURE 5 - TYPICAL THERMAL RESISTANCE

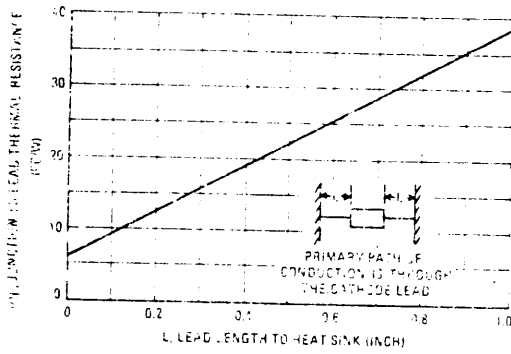


FIGURE 6 - MAXIMUM NON-REPETITIVE SURGE CURRENT versus NOMINAL ZENER VOLTAGE (See Note 4)

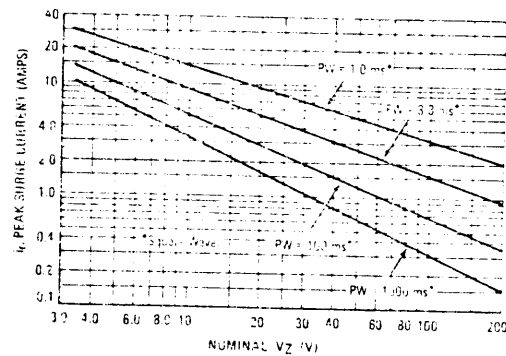
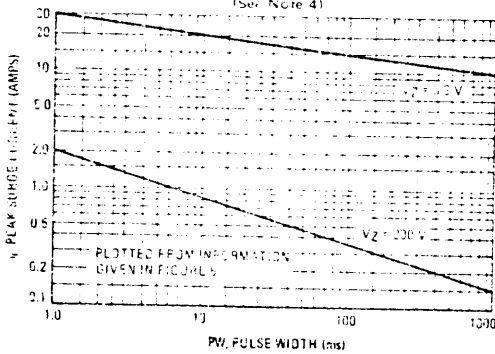


FIGURE 7 - PEAK SURGE CURRENT versus PULSE WIDTH (See Note 4)



APPLICATION NOTE

Since the actual voltage available from a given zener diode is temperature dependent, it is necessary to determine junction temperature under any set of operating conditions, in order to calculate its value. The following procedure is recommended:

Lead Temperature,  $T_L$ , should be determined from:

$$T_L = \theta_{LA} P_D + T_A$$

$\theta_{LA}$  is the lead-to-ambient thermal resistance and  $P_D$  is the power dissipation.

Junction Temperature,  $T_J$ , may be found from:

$$T_J = T_L + \Delta T_{JL}$$

$\Delta T_{JL}$  is the increase in junction temperature above the lead temperature and may be found from Figure 4 for a train of power pulses or from Figure 5 for dc power.

$$\Delta T_{JL} = \theta_{JL} P_D$$

For worst-case design, using expected limits of  $I_Z$ , limits of  $P_D$  and the extremes of  $T_J$  ( $\Delta T_J$ ) may be estimated. Changes in voltage,  $V_Z$ , can then be found from

$$\Delta V = \theta_{VZ} \Delta T_J$$

$\theta_{VZ}$ , the zener voltage temperature coefficient, is found from Figures 2 and 3.

Under high power-pulse operation, the zener voltage will vary with time and may also be affected significantly by the zener resistance. For best regulation, keep current excursions as low as possible.

Data of Figure 4 should not be used to compute surge capability. Surge limitations are given in Figure 6. They are lower than would be expected by considering only junction temperature, as current crowding effects cause temperatures to be extremely high in small spots resulting in device degradation should the limits of Figure 5 be exceeded.

3SM2 (or V352)

Type	Peak Voltage (V)	DC Voltage (V)	DC Current (mA)	Series Resistance (ohms)	Par. Capacitance (pF)	Max. Storage Temp. (°C)	Max. Power Dissipation (mW)	Frequency (kHz)	Ques. (ohms)	Secondary Temp. (°C)		
3SM2	200	140	500	3	2	1.0	1	20	25	150	2	1
3SM4	400	280	400	3	2	1.0	1	20	25	150	2	1
3SM6	600	420	600	3	2	1.0	1	20	25	150	2	1
3SM8	800	570	800	3	2	1.1	1	20	25	150	2	1
3SM6	1000	750	1000	3	2	1.1	1	20	25	150	2	1

MEDIUM RECOVERY (t) 2 MICROSECONDS

3SM2	200	140	500	3	2	1.0	1	20	25	150	2	1
3SM4	400	280	400	3	2	1.0	1	20	25	150	2	1
3SM6	600	420	600	3	2	1.0	1	20	25	150	2	1
3SM8	800	570	800	3	2	1.1	1	20	25	150	2	1
3SM6	1000	750	1000	3	2	1.1	1	20	25	150	2	1



D COMPONENT DESCRIPTIONS

D.2 TRANSISTORS

		MPS6521		MPS6523	
$V_{CBO}$	min	40V		25V	
$V_{CEO}$	min	25V		25V	
$V_{EBO}$	min	4V		4V	
$I_{CBO}$	max	50nA		50nA	
@ $V_{CB}$		30V		20V	
$h_{FE}$	min	150	300	150	300
	max		600		600
@ $I_C$		0.1mA	2mA	0.1mA	2mA
& $V_{CE}$		10V	10V	10V	10V
$V_{CE(sat)}$	max	0.5V		0.5V	
& $V_{BE}$	min				
	max				
@ $I_C$		50mA		50mA	
$C_{ob}$		3.5pF		4pF	
NF	max	3dB		3dB	

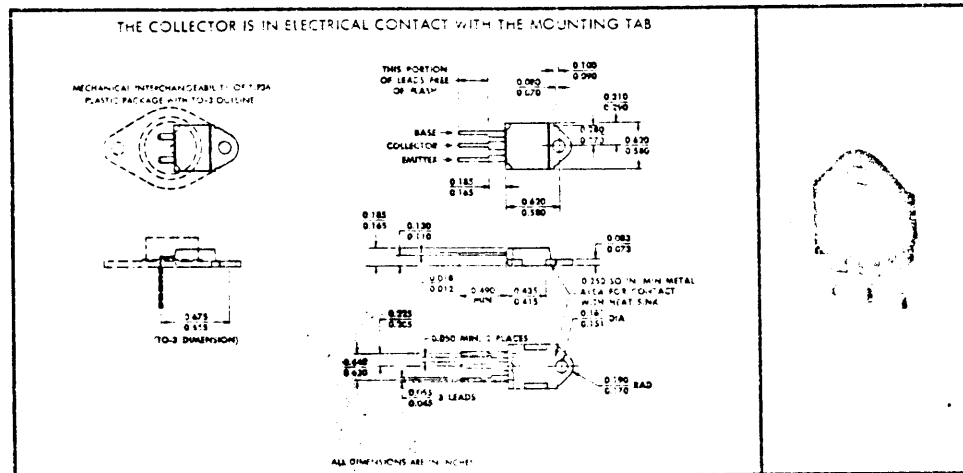
D COMPONENT DESCRIPTIONS  
 D.2 TRANSISTORS

TIP36A

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS  
 DESIGNED FOR COMPLEMENTARY USE WITH TIP35, TIP35A

- 90 Watts at 25°C Case Temperature
- 25 A Rated Collector Current
- Min  $f_T$  of 3 MHz at 10 V, 1 A

mechanical data



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP36	TIP36A
Collector-Base Voltage	-40 V	-60 V
Collector-Emitter Voltage (See Note 1)	-40 V	-60 V
Emitter-Base Voltage	← -5 V →	← -5 V →
Continuous Collector Current	← -25 A →	← -25 A →
Continuous Base Current	← -5 A →	← -5 A →
Safe Operating Region at (or below) 25°C Case Temperature	See Figure 2	
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 2)	← 90 W →	← 90 W →
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 3)	← 3.5 W →	← 3.5 W →
Operating Collector Junction Temperature Range	-65°C to 150°C	
Storage Temperature Range	-65°C to 150°C	
Lead Temperature 1/8 Inch from Case for 10 Seconds	← 260°C →	← 260°C →

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.  
 2. Derate linearly to 150°C case temperature at the rate of 0.72 W/deg.  
 3. Derate linearly to 150°C free-air temperature at the rate of 28 mW/deg.

D COMPONENT DESCRIPTIONS  
D.2 TRANSISTORS

TIP36A cont'd

electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	TIP36		TIP36A		UNIT
		MIN	MAX	MIN	MAX	
$V_{BR}(CEO)$ Collector-Emitter Breakdown Voltage	$I_C = -200 \text{ mA}, I_B = 0$ , See Note 4	-40		-60		V
$I_{CEO}$ Collector Cutoff Current	$V_{CE} = -30 \text{ V}, I_B = 0$	-1		-1		mA
$I_{CES}$ Collector Cutoff Current	$V_{CE} = -40 \text{ V}, V_{BE} = 0$	-0.7				mA
	$V_{CE} = -60 \text{ V}, V_{BE} = 0$			-0.7		
$I_{EBO}$ Emitter Cutoff Current	$V_{EB} = -5 \text{ V}, I_C = 0$	-1		-1		mA
$h_{FE}$ Static Forward Current Transfer Ratio	$V_{CE} = -4 \text{ V}, I_C = -5 \text{ A}$ , See Notes 4 and 5	20	100	20	100	
	$V_{CE} = -4 \text{ V}, I_C = -15 \text{ A}$ , See Notes 4 and 5	10		10		
	$V_{CE} = -4 \text{ V}, I_C = -25 \text{ A}$ , See Notes 4 and 5	5		5		
$V_{BE}$ Base-Emitter Voltage	$V_{CE} = -4 \text{ V}, I_C = -15 \text{ A}$ , See Notes 4 and 5	-2		-2		V
	$V_{CE} = -4 \text{ V}, I_C = -25 \text{ A}$ , See Notes 4 and 5	-4		-4		
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -1.5 \text{ A}, I_C = -15 \text{ A}$ , See Notes 4 and 5	-1.8		-1.8		V
	$I_B = -5 \text{ A}, I_C = -25 \text{ A}$ , See Notes 4 and 5	-4		-4		
$h_{fw}$ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}, I_C = -1 \text{ A}, f = 1 \text{ kHz}$	25		25		
$h_{fe}$ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}, I_C = -1 \text{ A}, f = 1 \text{ MHz}$	3		3		

NOTES: 4. These parameters must be measured using pulse techniques:  $t_p \leq 300 \mu\text{s}$ , duty cycle  $\leq 2\%$ .  
Pulse width must be such that halving or doubling does not cause a change greater than the required accuracy of the measurement.  
5. These parameters are measured with voltage sensing contacts separate from the current-carrying contacts.

thermal characteristics

PARAMETER	MAX	UNIT
$\theta_{J-C}$ Junction-to-Case Thermal Resistance	1.39	°Cg/W
$\theta_{J-A}$ Junction-to-Free-Air Thermal Resistance	35.7	

switching characteristics at 25°C case temperature

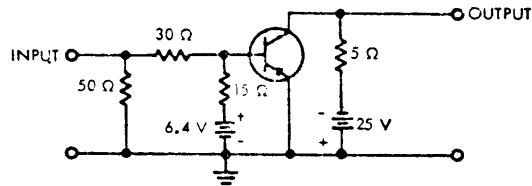
PARAMETER	TEST CONDITIONS†	TYP	UNIT
$t_{on}$ Turn-On Time	$I_C = -5 \text{ A}, I_{B(1)} = -300 \text{ mA}, I_{B(2)} = 300 \text{ mA}$	0.65	$\mu\text{s}$
$t_{off}$ Turn-Off Time	$V_{BE(2)} = 5 \text{ V}, R_L = 5 \Omega$ , See Figure 1	0.35	

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

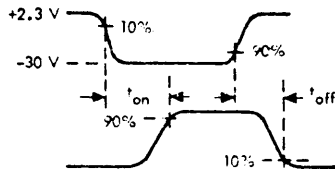
D COMPONENT DESCRIPTIONS  
 D.2 TRANSISTORS

TIP36A cont'd

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 1

- NOTES:
- a. The input waveform is supplied by a generator with the following characteristics:  $t_r \leq 15$  ns,  $t_f \leq 15$  ns,  $Z_{out} = 50 \Omega$ ,  $I_p = 10 \mu$ s, duty cycle  $\leq 2\%$ .
  - b. Waveforms are monitored on an oscilloscope with the following characteristics:  $t_r \leq 15$  ns,  $R_{in} \geq 10$  k $\Omega$ ,  $C_{in} \leq 11.5$  pF.
  - c. Resistors must be noninductive types.
  - d. The d.c. power supplies may require additional bypassing in order to minimize ringing.

MAXIMUM SAFE OPERATING REGION

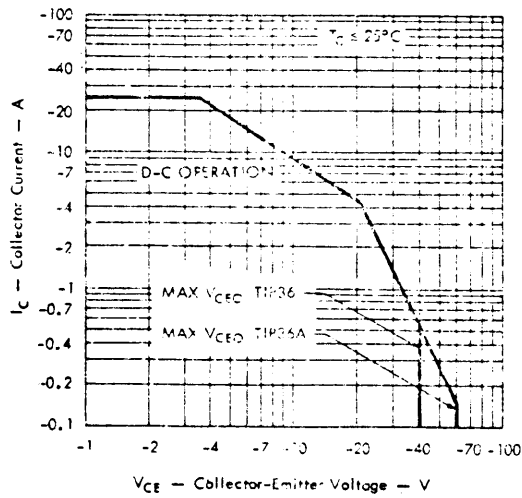


FIGURE 2

D COMPONENT DESCRIPTIONS  
 D.2 TRANSISTORS

TIP36A cont'd

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO  
 vs  
 COLLECTOR CURRENT

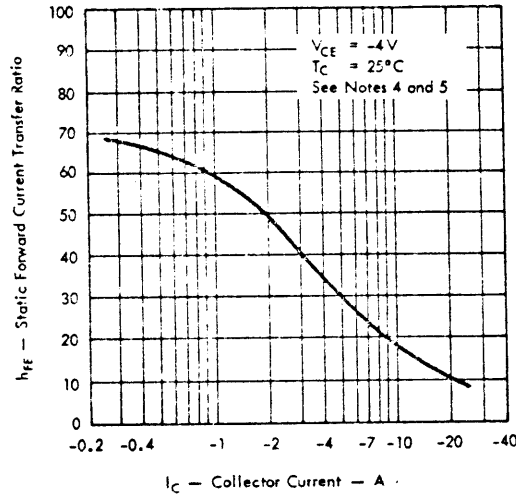


FIGURE 3

BASE-EMITTER VOLTAGE  
 vs  
 COLLECTOR CURRENT

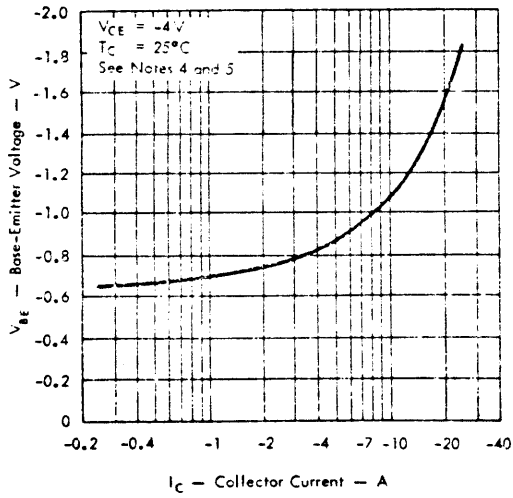


FIGURE 4

COLLECTOR-EMITTER SATURATION VOLTAGE  
 vs  
 COLLECTOR CURRENT

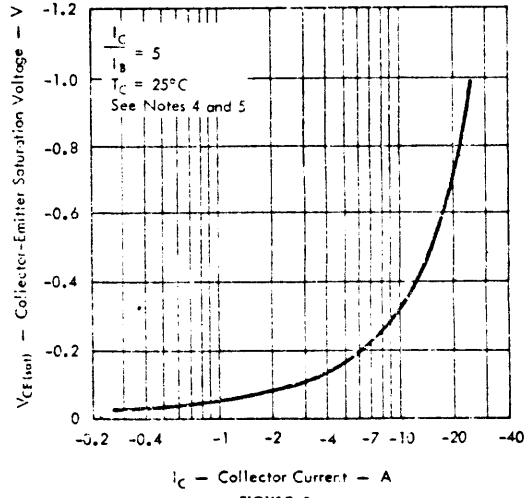


FIGURE 5

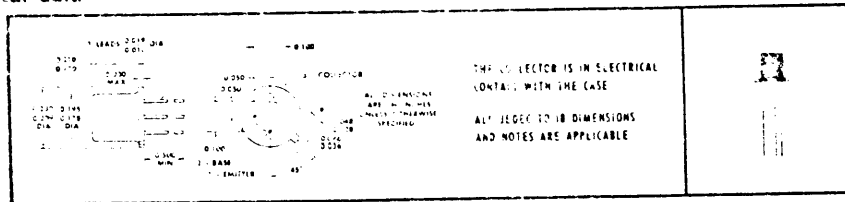
- NOTES: 4. These parameters must be measured using pulse techniques.  $t_p \leq 300$  ns, duty cycle  $\leq 2\%$ . Pulse width must be such that heating or doubling does not cause a change greater than the required accuracy of the measurement.  
 5. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

D COMPONENT DESCRIPTIONS  
D.2 TRANSISTORS

2N2369A

DESIGNED FOR VERY-HIGH-SPEED SWITCHING APPLICATIONS

\*mechanical data



\*absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Collector-Base Voltage	40 v
Collector-Emitter Voltage (See Note 1)	40 v
Collector-Emitter Voltage (See Note 2)	15 v
Emitter-Base Voltage	4.5 v
Continuous Collector Current	200 ma
Peak Collector Current (See Note 3)	500 ma
Continuous Device Dissipation at (or below) 25°C Free Air Temperature (See Note 4)	0.36 w
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 5)	1.2 w
Continuous Device Dissipation at 100°C Case Temperature	0.68 w
Operating Collector Junction Temperature	200°C
Storage Temperature Range	-65°C to 200°C
Lead Temperature 1/8 Inch from Case for 60 Seconds	300°C

\*electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	MAX	UNIT
$V_{BR}(CO)$ Collector-Base Breakdown Voltage	$I_B = 10 \mu A, I_C = 0$		40	v
$V_{BR}(CE)$ Collector-Emitter Breakdown Voltage	$I_B = 10 \mu A, I_E = 0$ See Note 6		15	v
$V_{BR}(CB)$ Collector-Base Breakdown Voltage	$I_C = 10 \mu A, I_E = 0$		40	v
$V_{BR}(EB)$ Emitter-Base Breakdown Voltage	$I_C = 10 \mu A, I_B = 0$		4.5	v
$I_{CBO}$ Collector Cutoff Current	$V_{CE} = 20 v, I_B = 0, T_A = 150^\circ C$		30	$\mu A$
$I_{ECS}$ Collector Cutoff Current	$V_{CE} = 20 v, V_{BE} = 0$		0.4	$\mu A$
$I_B$ Base Current	$V_{CE} = 20 v, I_C = 0$		-0.4	$\mu A$
$h_{FE}$ Static Forward Current Transfer Ratio	$V_{CE} = 0.75 v, I_C = 10 ma$ See Note 6		40	
	$V_{CE} = 1 v, I_C = 10 ma$ See Note 6		120	
	$V_{CE} = 0.4 v, I_C = 30 ma$ See Note 6		30	
	$V_{CE} = 1 v, I_C = 100 ma$ See Note 6		20	
	$V_{CE} = 0.35 v, I_C = 10 ma, T_A = -55^\circ C$ See Note 6		20	
$V_{BE}$ Base-Emitter Voltage	$I_B = 1 ma, I_C = 10 ma$	0.7	0.85	v
	$I_B = 3 ma, I_C = 30 ma$		1.15	v
	$I_B = 10 ma, I_C = 100 ma$		1.6	v
	$I_B = 1 ma, I_C = 10 ma, T_A = 125^\circ C$	0.59		v
	$I_B = 1 ma, I_C = 10 ma, T_A = -55^\circ C$	1.02		v
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 1 ma, I_C = 10 ma$	0.2		v
	$I_B = 3 ma, I_C = 30 ma$	0.25		v
	$I_B = 10 ma, I_C = 100 ma$	0.5		v
	$I_B = 1 ma, I_C = 10 ma, T_A = 125^\circ C$	0.3		v
$[h_{FE}]$ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 v, I_C = 20 ma, f = 100 Mc$	5		
$C_{ob}$ Common-Base Open-Circuit Output Capacitance	$V_{CB} = 5 v, I_E = 0, f = 140 kc$	4		pf

- NOTES: 1. This value applies when the base-emitter diode is short-circuited.  
 2. This value applies between 10  $\mu A$  and 10 mA collector current when the base-emitter diode is open-circuited.  
 3. This value applies for  $PW \leq 10 \mu sec$ .  
 4. Dissipate linearly to 200°C free air temperature at the rate of 2.06 mW/°C.  
 5. Dissipate linearly to 200°C case temperature at the rate of 85 mW/°C.  
 6. These parameters must be measured using pulse techniques:  $PW = 300 \mu sec$ , Duty Cycle  $\leq 2\%$ .  
 \*Indicates JEDEC registered data.

D COMPONENT DESCRIPTIONS  
 D.2 TRANSISTORS

2N2369A cont'd

\*switching characteristics at 25°C free-air temperature

PARAMETER	TEST CONDITIONS†	MAX	UNIT
$t_{on}$ Turn-On Time	$I_C = 10 \text{ ma}$ , $I_{B1} = 3 \text{ ma}$ , $I_{B2} = -1.5 \text{ ma}$	12	nsec
$t_{off}$ Turn-Off Time	$V_{BE(on)} = -1.5 \text{ v}$ , $R_L = 250 \Omega$	18	nsec
$t_s$ Storage Time	$I_C = I_{B1} = 10 \text{ ma}$ , $I_{B2} = -10 \text{ ma}$	13	nsec

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

\*PARAMETER MEASUREMENT INFORMATION

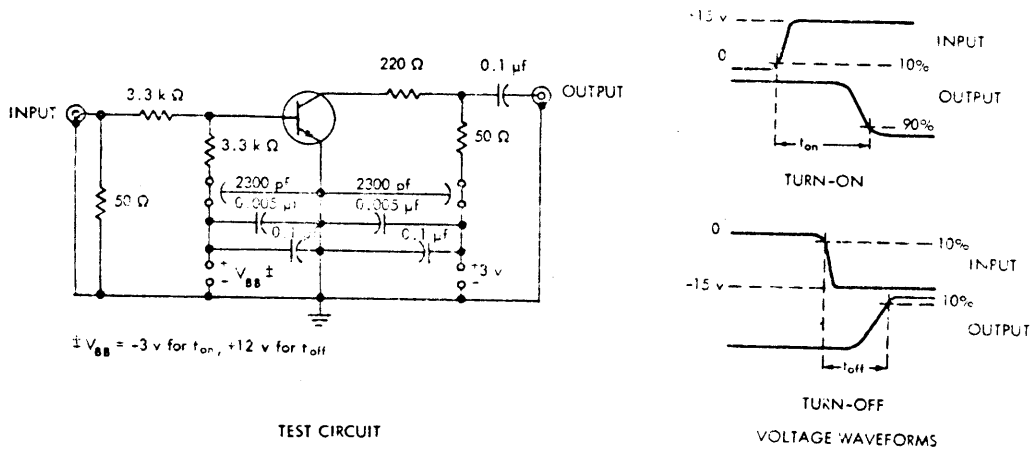


FIGURE 1—TURN-ON AND TURN-OFF TIMES

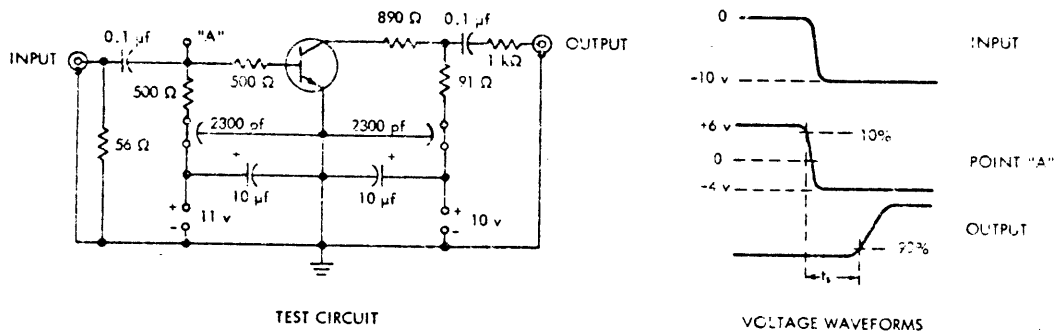


FIGURE 2—STORAGE TIME

NOTES a. The input waveforms are supplied by a pulse generator with the following characteristics:  $Z_{out} = 50 \Omega$ ,  $t_r \leq 1 \text{ nsec}$ ,  $PW > 300 \text{ nsec}$ , Duty Cycle  $\leq 2\%$ .  
 b. Output waveforms are monitored on an oscilloscope with the following characteristics:  $t_r \leq 1 \text{ nsec}$ ,  $Z_{in} = 50 \Omega$ .

\*Indicates JEDEC registered data.

D COMPONENT DESCRIPTIONS

D.2 TRANSISTORS

2N5121

CASE TO-106

$V_{CBO}$  min 15V

$V_{CEO}$  min 12V

$V_{EBO}$  min 3V

$I_{CBO}$  max 50nA  
@  $V_{CB}$  10V

$h_{FE}$  min 20 35  
max 350  
@  $I_C$  10mA 50mA  
&  $V_{CE}$  10V 10V

$V_{CE(sat)min}$  0.25V  
&  $V_{BE(sat)min}$   
max 1.1V  
@  $I_C$  150mA

$C_{ob}$  max 10pF

$f_T$  min 200MHz  
max 800MHz  
@  $I_C$  50mA



D COMPONENT DESCRIPTIONS  
D.2 TRANSISTORS

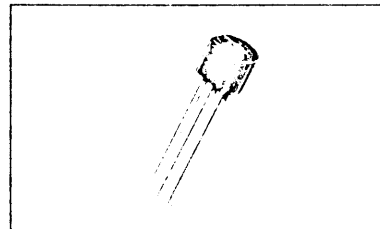
2N4400

**NPN SILICON ANNULAR TRANSISTORS**

... designed for general-purpose switching and amplifier applications and for complementary circuitry with types 2N4402 and 2N4403.

- Collector-Emitter Breakdown Voltage --  
 $V_{CE0} = 40 \text{ Vdc (Min) @ } I_C = 1.0 \text{ mAdc}$
- Current Gain Specified from 0.1 mAdc to 500 mAdc
- Complete Switching and Amplifier Specifications
- Collector-Base Capacitance --  
 $C_{cb} = 6.5 \text{ pF (Max) @ } V_{CB} = 5.0 \text{ Vdc}$

**NPN SILICON  
SWITCHING AND AMPLIFIER  
TRANSISTORS**



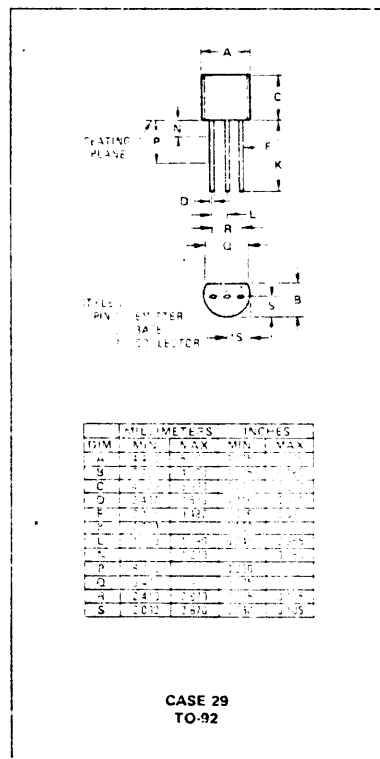
**\*MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CE0}$	40	Vdc
Collector-Base Voltage	$V_{CB}$	60	Vdc
Emitter-Base Voltage	$V_{EB}$	6.0	Vdc
Collector Current - Continuous	$I_C$	600	mAdc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	350 28	mW mW/°C
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.0 3.0	Watt mW/°C
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-55 to +150	°C

**THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	357	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	125	°C/W

\*Indicates JEDEC Registered Data



D COMPONENT DESCRIPTIONS  
D.2 TRANSISTORS

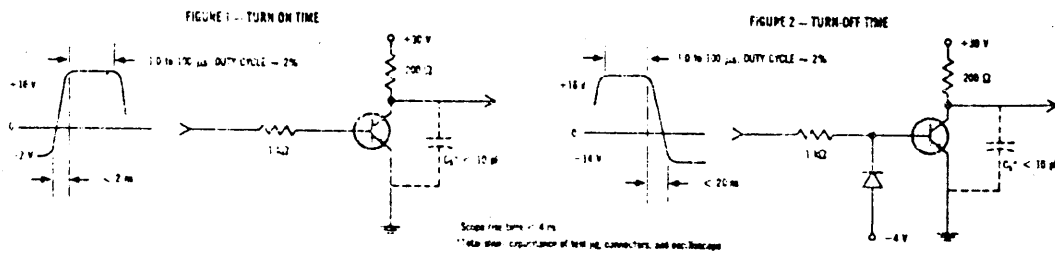
2N4400 cont'd

ELECTRICAL CHARACTERISTICS (TA = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector-Emitter Breakdown Voltage (1) ( $I_C = 1 \text{ mAdc}, I_B = 0$ )	$BV_{CEO}$	40	—	Vdc
Collector-Base Breakdown Voltage ( $I_C = 0.1 \text{ mAdc}, I_E = 0$ )	$BV_{CBO}$	60	—	Vdc
Emitter-Base Breakdown Voltage ( $I_E = 0.1 \text{ mAdc}, I_C = 0$ )	$BV_{EBO}$	6.0	—	Vdc
Collector Cutoff Current ( $V_{CE} = 35 \text{ Vdc}, V_{BE(off)} = 0.4 \text{ Vdc}$ )	$I_{CBO}$	—	0.1	$\mu\text{Adc}$
Base Cutoff Current ( $V_{CE} = 35 \text{ Vdc}, V_{BE(off)} = 0.4 \text{ Vdc}$ )	$I_{EBO}$	—	0.1	$\mu\text{Adc}$
<b>ON CHARACTERISTICS (1)</b>				
DC Current Gain ( $I_C = 0.1 \text{ mAdc}, V_{CE} = 1 \text{ Vdc}$ ) ( $I_C = 1 \text{ mAdc}, V_{CE} = 1 \text{ Vdc}$ ) ( $I_C = 10 \text{ mAdc}, V_{CE} = 1 \text{ Vdc}$ ) ( $I_C = 150 \text{ mAdc}, V_{CE} = 1 \text{ Vdc}$ ) ( $I_C = 500 \text{ mAdc}, V_{CE} = 2 \text{ Vdc}$ )	$\beta_{FE}$	20 20 40 40 20	— — — 150 —	—
Collector-Emitter Saturation Voltage ( $I_C = 150 \text{ mAdc}, I_B = 15 \text{ mAdc}$ ) ( $I_C = 500 \text{ mAdc}, I_B = 50 \text{ mAdc}$ )	$V_{CE(sat)}$	—	0.4 0.75	Vdc
Base-Emitter Saturation Voltage ( $I_C = 150 \text{ mAdc}, I_B = 15 \text{ mAdc}$ ) ( $I_C = 500 \text{ mAdc}, I_B = 50 \text{ mAdc}$ )	$V_{BE(sat)}$	0.75	0.95 1.2	Vdc
<b>SMALL SIGNAL CHARACTERISTICS</b>				
Current Gain - Bandwidth Product ( $I_C = 20 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}, f = 100 \text{ MHz}$ )	$f_T$	200 250	—	MHz
Collector-Base Capacitance ( $V_{CE} = 5 \text{ Vdc}, I_C = 0, f = 100 \text{ kHz}$ )	$C_{cb}$	—	5.5	pF
Emitter-Base Capacitance ( $V_{BE} = 0.7 \text{ Vdc}, I_C = 0, f = 100 \text{ kHz}$ )	$C_{eb}$	—	30	pF
Input Impedance ( $I_C = 1 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}, f = 1 \text{ kHz}$ )	$h_{ie}$	0.5 1.0	7.5 15	k ohms
Voltage Feedback Ratio ( $I_C = 1 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}, f = 1 \text{ kHz}$ )	$F_{re}$	0.1	8.0	$\times 10^{-4}$
Small-signal Current Gain ( $I_C = 1 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}, f = 1 \text{ kHz}$ )	$h_{fe}$	20 40	250 500	—
Output Admittance ( $I_C = 1 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}, f = 1 \text{ kHz}$ )	$h_{oe}$	1.0	30	$\mu\text{mhos}$
<b>SWITCHING CHARACTERISTICS</b>				
Delay Time ( $V_{CC} = 30 \text{ Vdc}, V_{BE(off)} = 2 \text{ Vdc}$ )	$t_d$	—	15	ns
Rise Time ( $I_C = 150 \text{ mAdc}, I_B = 15 \text{ mAdc}$ )	$t_r$	—	20	ns
Storage Time ( $V_{CC} = 30 \text{ Vdc}, I_C = 150 \text{ mAdc}$ )	$t_s$	—	275	ns
Fall Time ( $I_{B1} = I_{B2} = 15 \text{ mAdc}$ )	$t_f$	—	35	ns

(1) Pulse Test: Pulse Width = 350  $\mu\text{s}$ , Duty Cycle = 2.0%.  
\*Indicates JEDEC Registered Data

SWITCHING TIME EQUIVALENT TEST CIRCUITS



D COMPONENT DESCRIPTIONS

D.2 TRANSISTORS

2N4400 cont'd

TRANSIENT CHARACTERISTICS

— 25°C    - - - 100°C

FIGURE 3 — CAPACITANCES

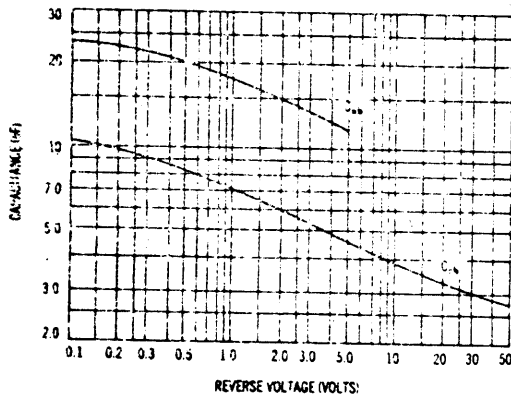


FIGURE 4 — CHARGE DATA

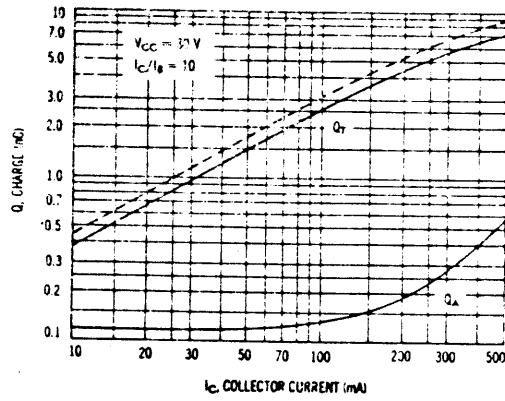


FIGURE 5 — TURN-ON TIME

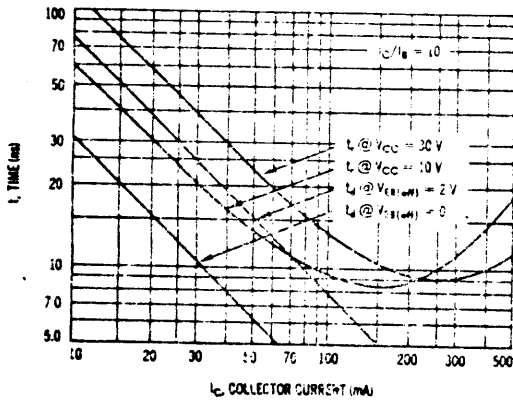


FIGURE 6 — RISE AND FALL TIMES

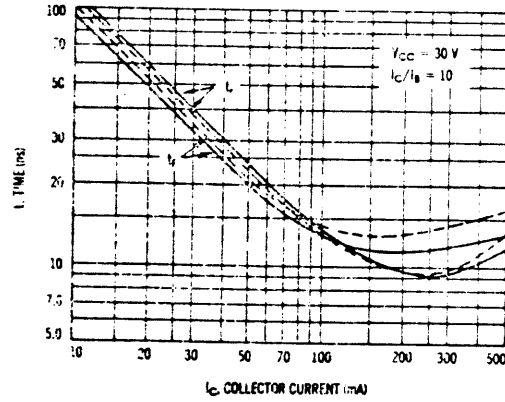


FIGURE 7 — STORAGE TIME

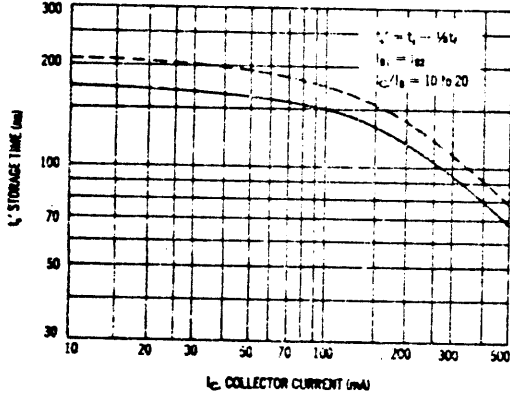
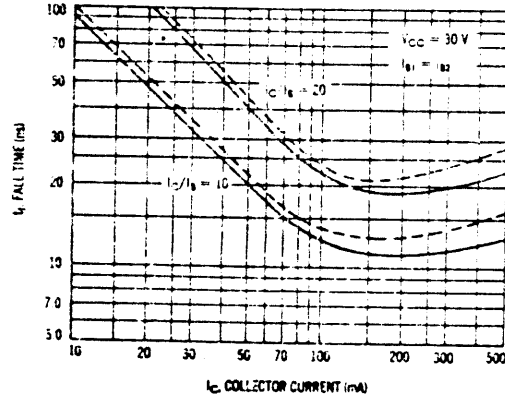


FIGURE 8 — FALL TIME



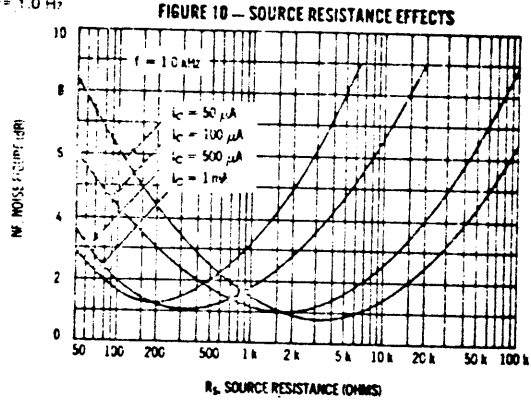
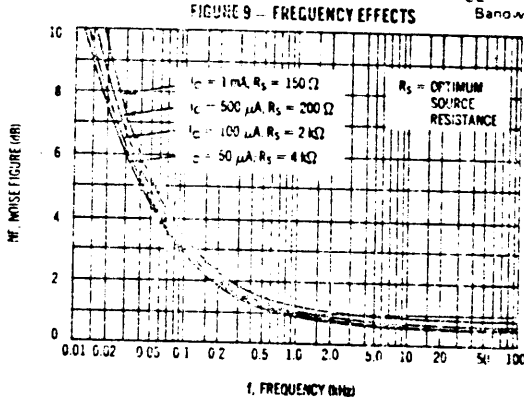
D COMPONENT DESCRIPTIONS  
 D.2 TRANSISTORS

2N4400 cont'd

SMALL-SIGNAL CHARACTERISTICS

NOISE FIGURE

$V_{CE} = 10 \text{ Vdc}$ ,  $T_A = 25^\circ\text{C}$   
 Bandwidth = 1.0 Hz

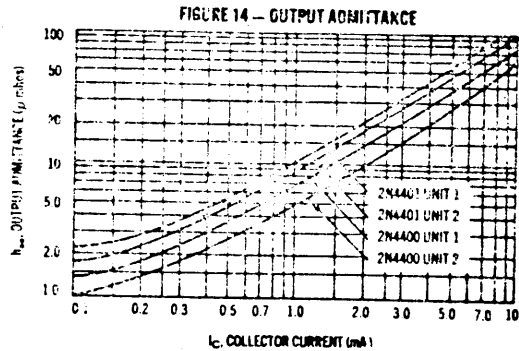
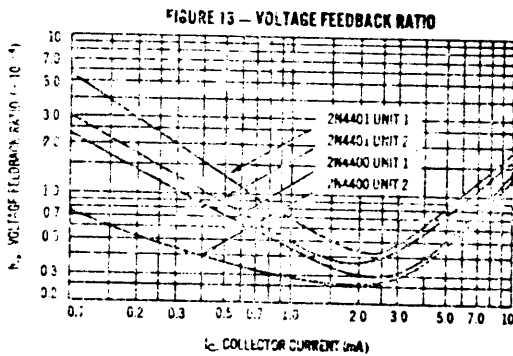
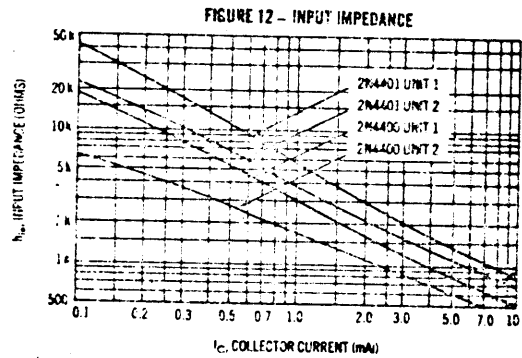
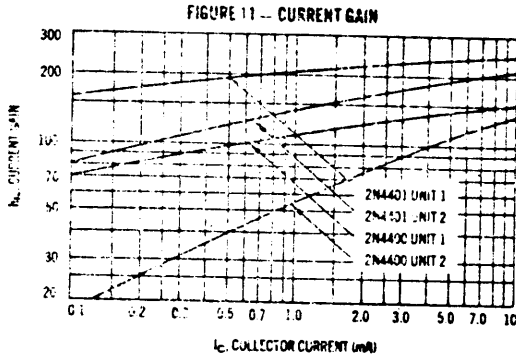


h PARAMETERS

$V_{CE} = 10 \text{ Vdc}$ ,  $f = 1 \text{ kHz}$ ,  $T_A = 25^\circ\text{C}$

This group of graphs illustrates the relationship between  $h_{ie}$  and other "h" parameters for this series of transistors. To obtain these curves, a high gain and a low gain unit were selected from both the

2N4400 and 2N4401 lines, and the same units were used to develop the correspondingly numbered curves on each graph.



D COMPONENT DESCRIPTIONS  
 D.2 TRANSISTORS

2N4400 cont'd

STATIC CHARACTERISTICS

FIGURE 15 — DC CURRENT GAIN

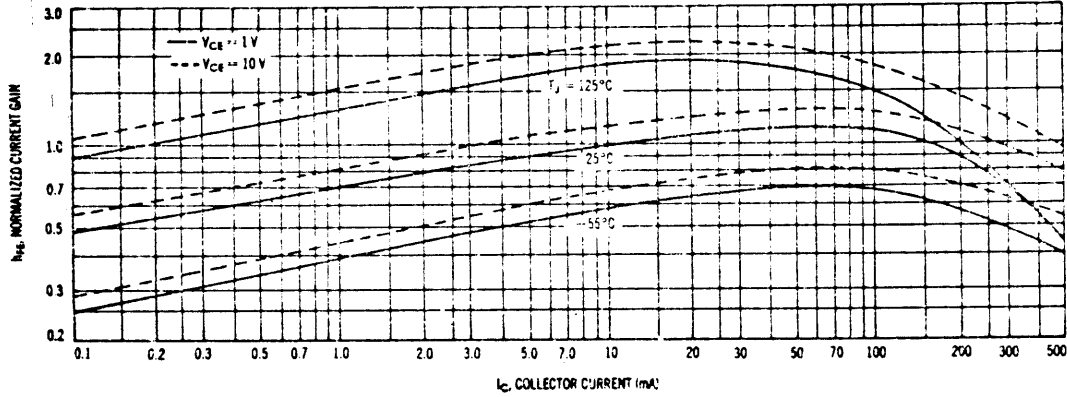


FIGURE 16 — COLLECTOR SATURATION REGION

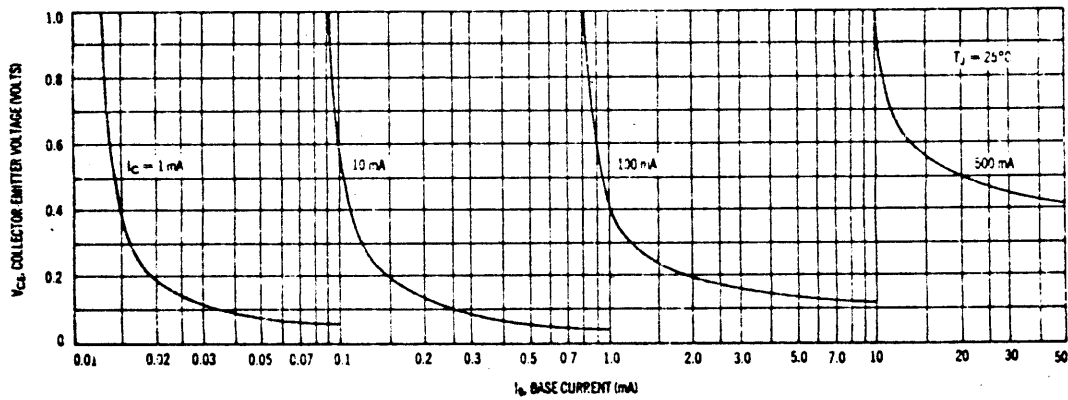


FIGURE 17 — "ON" VOLTAGES

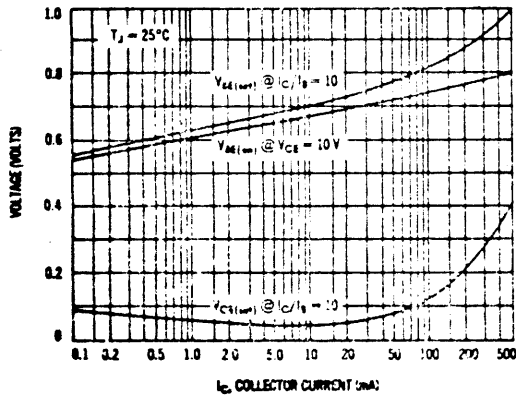
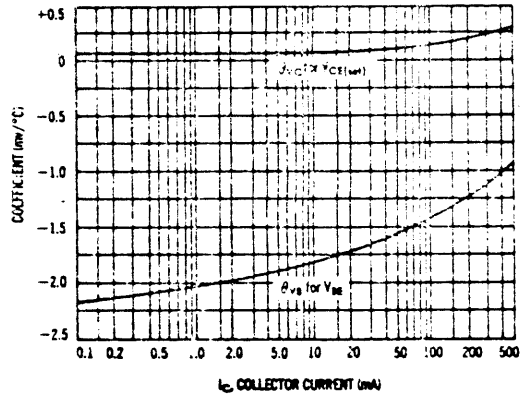


FIGURE 18 — TEMPERATURE COEFFICIENTS



D COMPONENT DESCRIPTIONS  
 D.3 OPTO-ISOLATORS

4N33

**NPN PHOTOTRANSISTOR AND PN INFRARED EMITTING DIODE**

Gallium Arsenide LED optically coupled to a Silicon Photo Darlington Transistor designed for applications requiring electrical isolation, high-current transfer ratios, small package size and low cost; such as interfacing and coupling systems, phase and feedback controls, solid-state relays and general purpose switching circuits.

- High Isolation Voltage –  $V_{ISO} = 2500\text{ V (Min)} - 4N29,32$   
 $1500\text{ V (Min)} - 4N30,31,33$
- High Collector Output Current @  $I_C = 10\text{ mA}$  –  $I_C = 50\text{ mA (Min)} - 4N32,33$   
 $10\text{ mA (Min)} - 4N29,30$   
 $5.0\text{ mA (Min)} - 4N31$
- Excellent Frequency Response –  $30\text{ kHz (Typ)}$
- Fast Switching Times @  $I_C = 50\text{ mA}$   
 $t_{on} = 0.6\text{ }\mu\text{s (Typ)}$   
 $t_{off} = 17\text{ }\mu\text{s (Typ)} - 4N29,30,31$   
 $45\text{ }\mu\text{s (Typ)} - 4N32,33$
- Economical, Compact, Dual-In-Line Package

**MAXIMUM RATINGS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

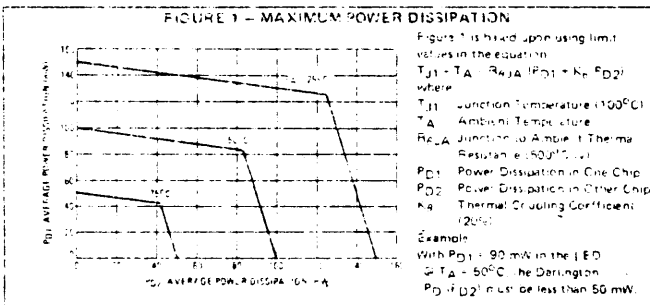
Rating	Symbol	Value	Unit
<b>INFRARED EMITTING DIODE MAXIMUM RATINGS</b>			
Reverse Voltage	$V_R$	30	Volts
Forward Current – Continuous	$I_F$	50	mA
Forward Current – Peak (Pulse Width = 30% or 20% Duty Cycle)	$I_{FP}$	50	Amps
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Negligible Power in Transistor Derate above $25^\circ\text{C}$	$P_D$	150	mW
		2.0	mW/°C

**PHOTOTRANSISTOR MAXIMUM RATINGS**

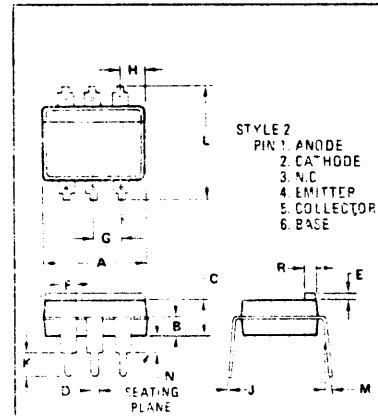
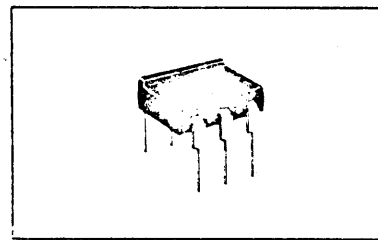
Collector-Emitter Voltage	$V_{CE0}$	30	Volts
Emitter-Collector Voltage	$V_{EC0}$	50	Volts
Collector-Base Voltage	$V_{CB0}$	30	Volts
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Negligible Power in Diode Derate above $25^\circ\text{C}$	$P_D$	150	mW
		2.0	mW/°C

**TOTAL DEVICE RATINGS**

Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Equal Power Dissipation in Each Element Derate above $25^\circ\text{C}$	$P_D$	250	mW
		3.3	mW/°C
Operating Junction Temperature Range	$T_J$	-55 to +100	°C
Storage Temperature Range	$T_{stg}$	-55 to +150	°C
Soldering Temperature (10 sec)		260	°C



**INFRARED LIGHT EMITTING DIODE PHOTO DARLINGTON TRANSISTOR COUPLED PAIR**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.75	8.87	0.330	0.350
B	1.40	1.75	0.055	0.065
C	2.12	3.18	0.115	0.125
D	0.41	0.51	0.016	0.020
E	0.62	0.82	0.025	0.035
F	1.27	1.40	0.045	0.055
G	2.54	2.54	0.100	0.100
H	1.52	1.52	0.062	0.072
I	0.25	0.25	0.010	0.011
K	2.54	2.54	0.100	0.100
L	7.37	7.37	0.250	0.310
M	—	50	—	50
N	—	1.27	—	0.050
R	1.52	1.73	0.060	0.070

CASE 673-03

## D COMPONENT DESCRIPTIONS

### D.3 OPTO-ISOLATORS

4N33 cont'd

#### LED CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Reverse Leakage Current (V <sub>R</sub> = 3.0 V, R <sub>L</sub> = 1.0 M ohms)	I <sub>R</sub>	—	0.05	100	μA
*Forward Voltage (I <sub>F</sub> = 50 mA)	V <sub>F</sub>	—	1.2	1.5	Volts
Capacitance (V <sub>R</sub> = 0 V, f = 1.0 MHz)	C	—	150	—	pF

#### PHOTOTRANSISTOR CHARACTERISTICS (T<sub>A</sub> = 25°C and I<sub>F</sub> = 0 unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Collector-Emitter Dark Current (V <sub>CE</sub> = 10 V, Base Open)	I <sub>CEO</sub>	—	—	100	nA
*Collector-Base Breakdown Voltage (I <sub>C</sub> = 100 μA, I <sub>E</sub> = 0)	BV <sub>CBO</sub>	30	—	—	Volts
*Collector-Emitter Breakdown Voltage (I <sub>C</sub> = 100 μA, I <sub>B</sub> = 0)	BV <sub>CEO</sub>	30	—	—	Volts
*Emitter-Collector Breakdown Voltage (I <sub>E</sub> = 100 μA, I <sub>B</sub> = 0)	BV <sub>ECO</sub>	5.0	—	—	Volts
DC Current Gain (V <sub>CE</sub> = 5.0 V, I <sub>C</sub> = 500 μA)	h <sub>FE</sub>	—	5000	—	—

#### COUPLED CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Collector Output Current (1) (V <sub>CE</sub> = 10 V, I <sub>F</sub> = 10 mA, I <sub>B</sub> = 0)	I <sub>C</sub>	50 10 5.0	— — —	— — —	mA
*Isolation Voltage (2)	V <sub>ISO</sub>	2500 1500	— —	— —	Volts
Isolation Resistance (2) (V = 500 V)	—	—	10 <sup>11</sup>	—	Ohms
*Collector-Emitter Saturation Voltage (1) (I <sub>C</sub> = 2.0 mA, I <sub>F</sub> = 8.0 mA)	V <sub>CE(sat)</sub>	— —	— —	1.2 1.0	Volts
Isolation Capacitance (2) (V = 0, f = 1.0 MHz)	—	—	0.8	—	pF
Bandwidth (3) (I <sub>C</sub> = 2.0 mA, R <sub>L</sub> = 100 ohms, Figures 6 and 8)	—	—	30	—	kHz

#### SWITCHING CHARACTERISTICS (Figures 7 and 9), (4)

Turn-On Time (I <sub>C</sub> = 50 mA, I <sub>F</sub> = 200 mA, V <sub>CC</sub> = 10 V)	t <sub>on</sub>	—	0.6	5.0	μs
Turn-Off Time (I <sub>C</sub> = 50 mA, I <sub>F</sub> = 200 mA, V <sub>CC</sub> = 10 V)	t <sub>off</sub>	—	17	40	μs
		—	45	100	μs

\*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%

(2) For this test LED pins 1 and 2 are common and Photo Transistor pins 4,5 and 6 are common.

(3) I<sub>F</sub> adjusted to yield I<sub>C</sub> = 2.0 mA and t<sub>c</sub> = 2.0 mA P-P at 10 kHz.

(4) t<sub>d</sub> and t<sub>r</sub> are inversely proportional to the amplitude of I<sub>F</sub>; t<sub>s</sub> and t<sub>f</sub> are not significantly affected by I<sub>F</sub>.

#### DC CURRENT TRANSFER CHARACTERISTICS

FIGURE 2 — 4N29, 4N30, 4N31

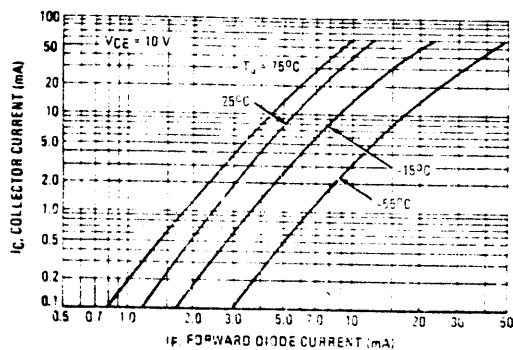
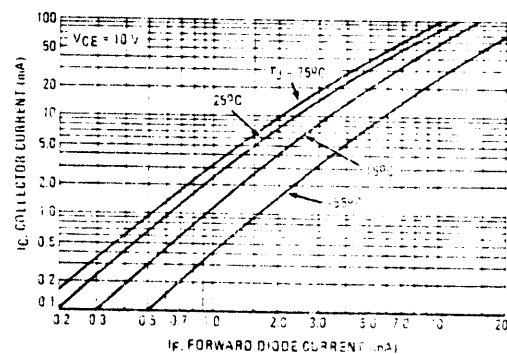


FIGURE 3 — 4N32, 4N33



D COMPONENT DESCRIPTIONS  
 D.3 OPTO-ISOLATORS

4N33 cont'd

TYPICAL ELECTRICAL CHARACTERISTICS  
 (Printed Circuit Board Mounting)

FIGURE 4 - DIODE FORWARD CHARACTERISTIC

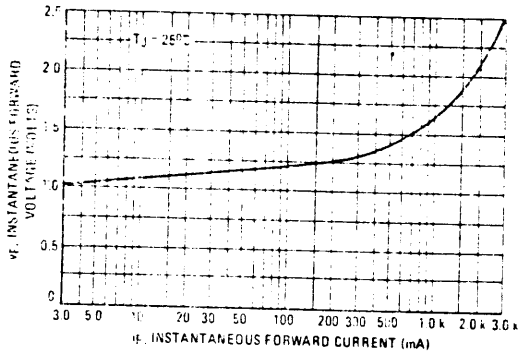


FIGURE 5 - COLLECTOR-EMITTER CUTOFF CURRENT

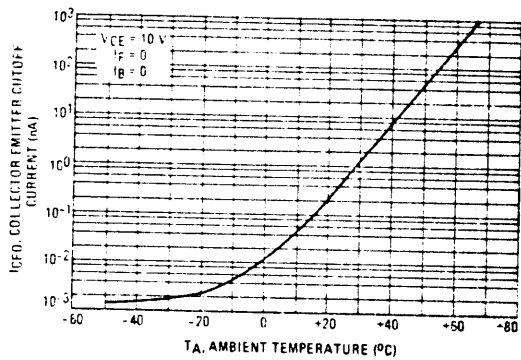


FIGURE 6 - FREQUENCY RESPONSE

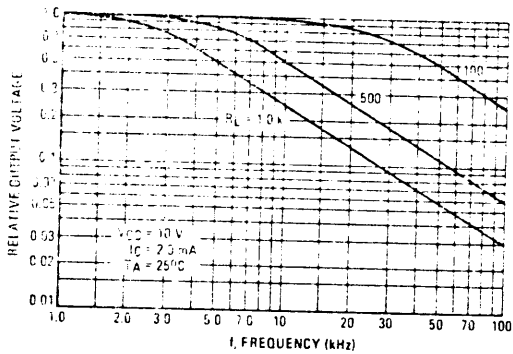


FIGURE 7 - SWITCHING TIMES

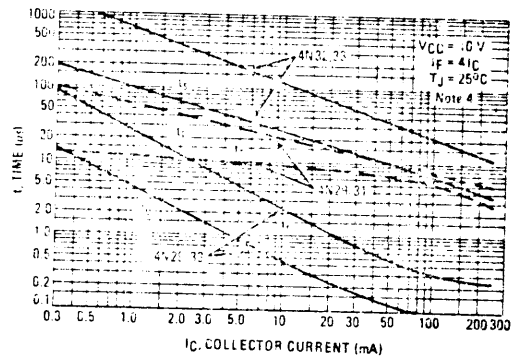


FIGURE 8 - FREQUENCY RESPONSE TEST CIRCUIT

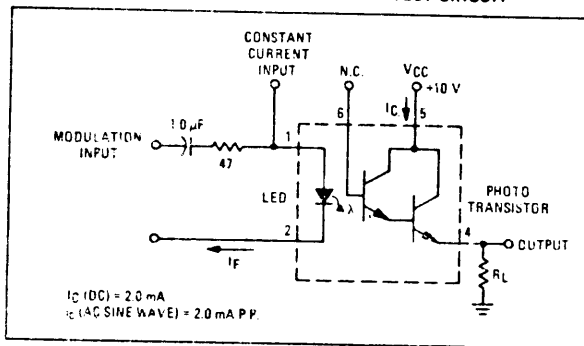
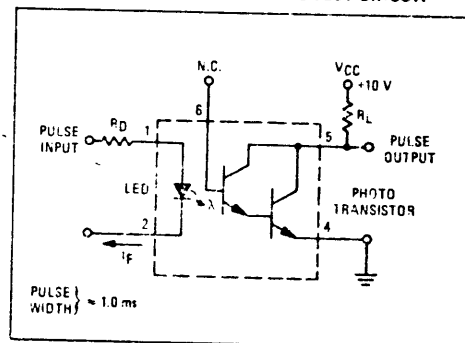


FIGURE 9 - SWITCHING TIME TEST CIRCUIT





D COMPONENT DESCRIPTIONS  
 D.3 OPTO-ISOLATORS

4N33 cont'd

TYPICAL APPLICATIONS  
 FIGURE 10 - VOLTAGE CONTROLLED TRIAC

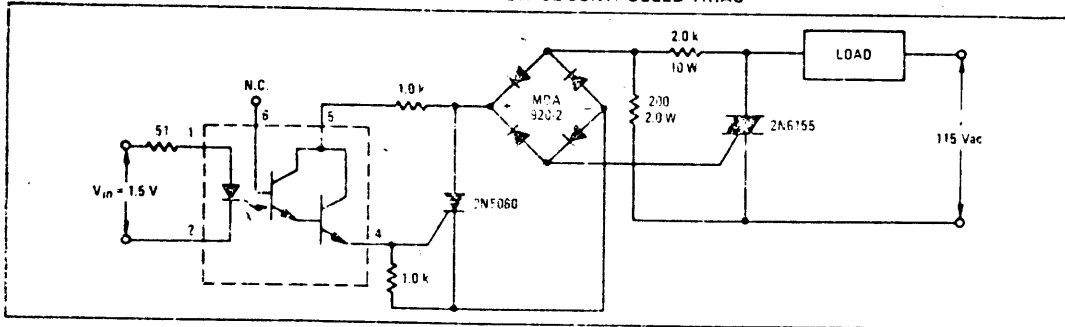


FIGURE 11 - AC SOLID STATE RELAY

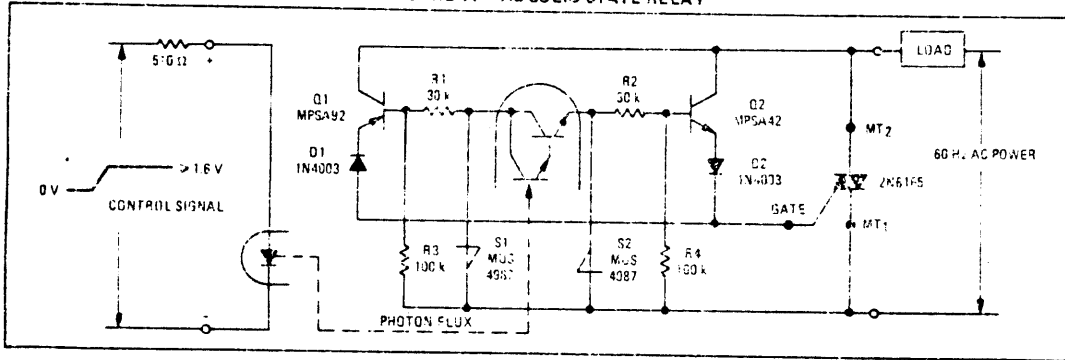


FIGURE 12 - OPTICALLY COUPLED ONE SHOT

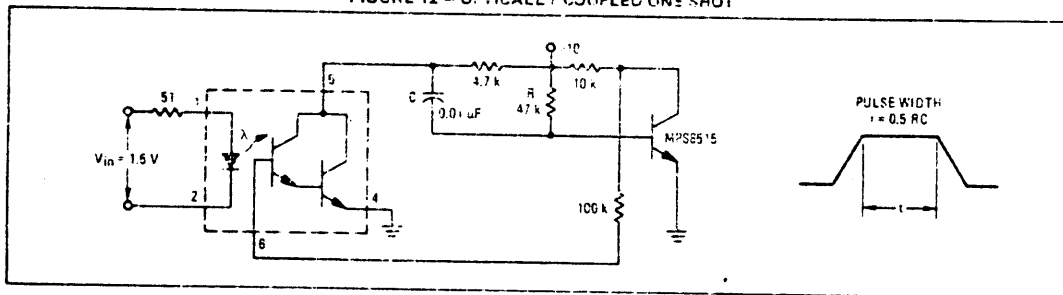
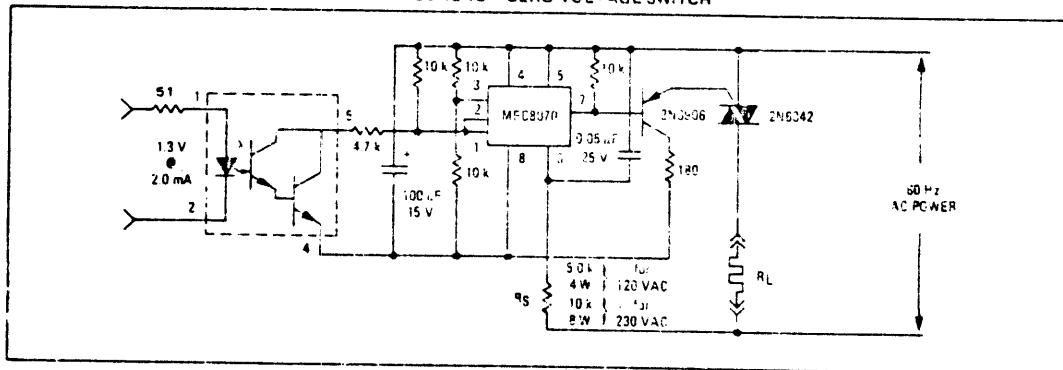


FIGURE 13 - ZERO VOLTAGE SWITCH



D COMPONENT DESCRIPTIONS  
 D.4 VOLTAGE REGULATORS

LM309K

The LM309 is a complete 5V regulator fabricated on a single silicon chip. It is designed for local regulation on digital logic cards, eliminating the distribution problems associated with single-point regulation. The device is available in two common transistor packages. In the solid-kovar TO-5 header, it can deliver output currents in excess of 200 mA, if adequate heat sinking is provided. With the TO-3 power package, the available output current is greater than 1A.

The regulator is essentially blow-out proof. Current limiting is included to limit the peak output current to a safe value. In addition, thermal shutdown is provided to keep the IC from overheating. If internal dissipation becomes too great, the regulator will shut down to prevent excessive heating.

Considerable effort was expended to make the LM309 easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient

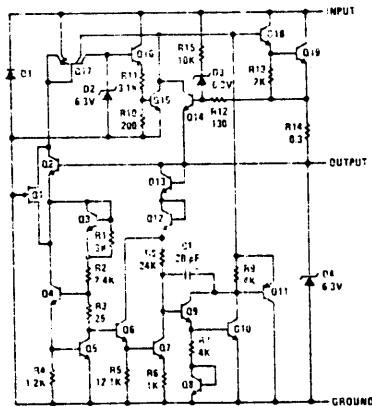
response somewhat. Input bypassing is needed, however, if the regulator is located very far from the filter capacitor of the power supply. Stability is also achieved by methods that provide very good rejection of load or line transients as are usually seen with TTL logic.

Although designed primarily as a fixed-voltage regulator, the output of the LM309 can be set to voltages above 5V, as shown below. It is also possible to use the circuit as the control element in precision regulators, taking advantage of the good current-handling capability and the thermal overload protection.

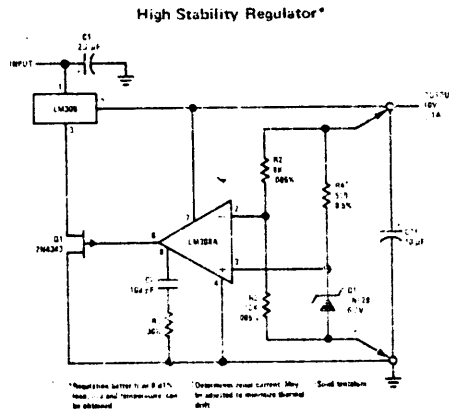
To summarize, outstanding features of the regulator are:

- Specified to be compatible, worst case, with TTL and DTL
- Output current in excess of 1A
- Internal thermal overload protection
- No external components required

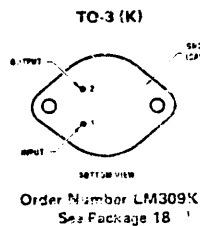
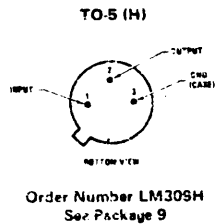
schematic diagram



typical application



connection diagrams



D COMPONENT DESCRIPTIONS  
 D.4 VOLTAGE REGULATORS

LM309K cont'd

absolute maximum ratings

Input Voltage	35V
Power Dissipation	Internally Limited
Operating Junction Temperature Range	0°C to 125°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

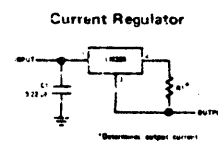
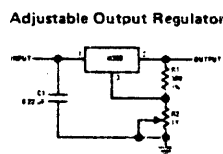
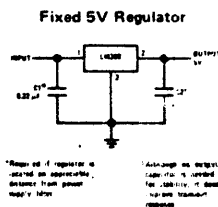
design characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	$T_J = 25^\circ\text{C}$	4.8	5.05	5.2	V
Line Regulation	$T_J = 25^\circ\text{C}$ $7\text{V} \leq V_{IN} \leq 25\text{V}$		4.0	50	mV
Load Regulation	$T_J = 25^\circ\text{C}$				
LM309H	$5\text{mA} \leq I_{OUT} \leq 0.5\text{A}$		20	50	mV
LM309K	$5\text{mA} \leq I_{OUT} \leq 1.5\text{A}$		50	100	mV
Output Voltage	$7\text{V} \leq V_{IN} \leq 25\text{V}$ $5\text{mA} \leq I_{OUT} \leq I_{max}$ $P < P_{max}$	4.75		5.25	V
Quiescent Current	$7\text{V} \leq V_{IN} \leq 25\text{V}$		5.2	10	mA
Quiescent Current Change	$7\text{V} \leq V_{IN} \leq 25\text{V}$ $5\text{mA} \leq I_{OUT} \leq I_{max}$			0.5	mA
Output Noise Voltage	$T_A = 25^\circ\text{C}$ $10\text{Hz} \leq f \leq 100\text{kHz}$		40		$\mu\text{V}$
Long Term Stability				20	mV
Thermal Resistance					
Junction to Case (Note 2)					$^\circ\text{C/W}$
LM309H			15		$^\circ\text{C/W}$
LM309K			3.0		$^\circ\text{C/W}$

Note 1: Unless otherwise specified, these specifications apply for  $0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ ,  $V_{IN} = 10\text{V}$  and  $I_{OUT} = 0.1\text{A}$  for the LM309H or  $I_{OUT} = 0.5\text{A}$  for the LM309K. For the LM309H,  $I_{max} = 0.2\text{A}$  and  $P_{max} = 2.0\text{W}$ . For the LM309K,  $I_{max} = 1.0\text{A}$  and  $P_{max} = 20\text{W}$ .

Note 2: Without a heat sink, the thermal resistance of the TO-5 package is about  $150^\circ\text{C/W}$ , while that of the TO-3 package is approximately  $35^\circ\text{C/W}$ . With a heat sink, the effective thermal resistance can only approach the values specified, depending on the efficiency of the sink.

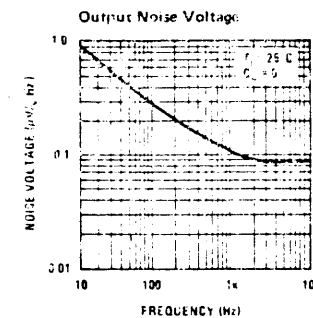
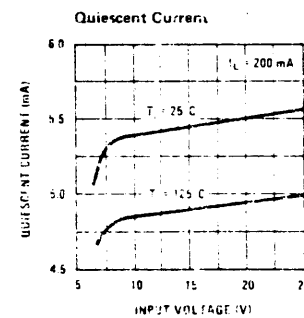
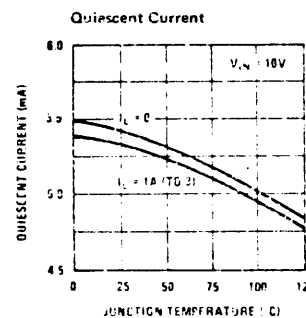
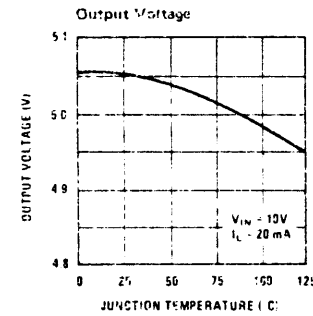
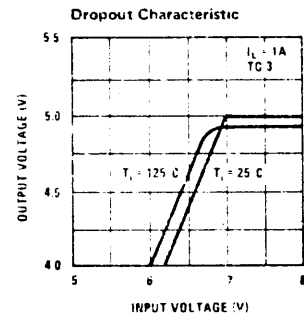
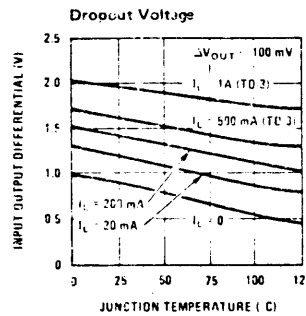
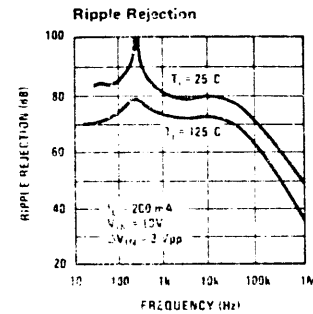
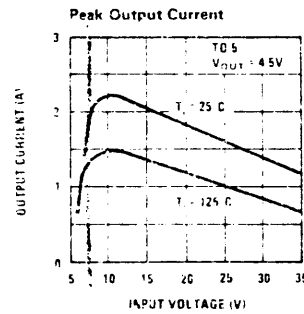
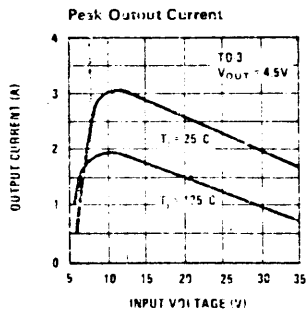
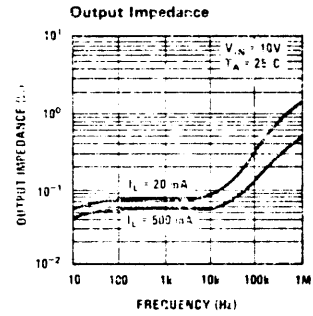
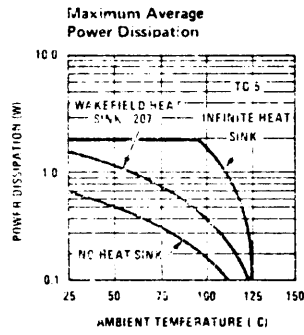
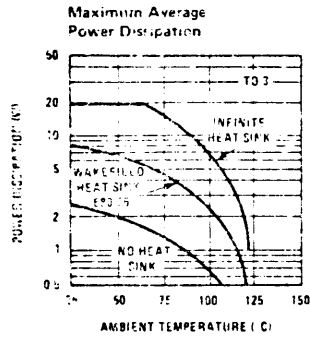
typical applications(con't)



D COMPONENT DESCRIPTIONS  
 D.4 VOLTAGE REGULATORS

LM309K cont'd

typical performance characteristics



D COMPONENT DESCRIPTIONS

D.4 VOLTAGE REGULATORS

LM340K

general description

The LM340-XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on board regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM340-XX series is available in two power packages. Both the plastic TO-220 and metal TO-3 packages allow these regulators to deliver over 1.0A if adequate heat sinking is provided. Even with over 1.0A of output current available the regulators are essentially blow-out proof. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Considerable effort was expended to make the LM340-XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

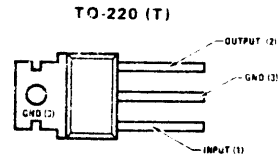
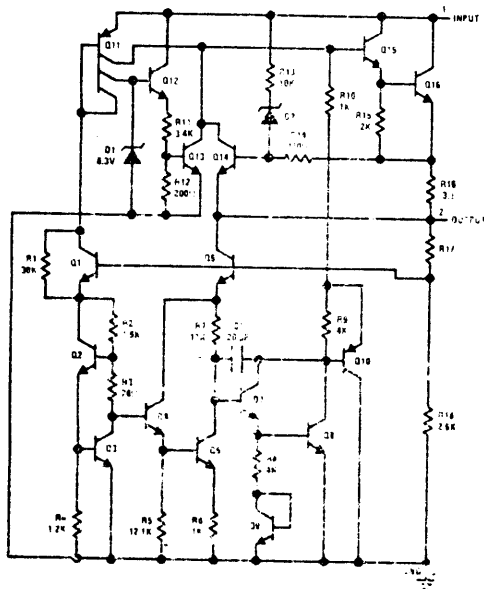
features

- Output current in excess of 1A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in plastic TO-220 and metal TO-3 packages

voltage range

LM340-5	5V	LM340-15	15V
LM340-6	6V	LM340-18	18V
LM340-8	8V	LM340-24	24V
LM340-12	12V		

schematic and connection diagrams

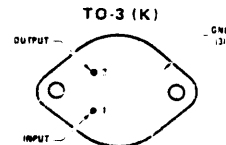


TOP VIEW

Order Numbers:

LM340T-5	LM340T-15
LM340T-6	LM340T-18
LM340T-8	LM340T-24
LM340T-12	

See Package 26



BOTTOM VIEW

Order Numbers:

LM340K-5	LM340K-15
LM340K-6	LM340K-18
LM340K-8	LM340K-24
LM340K-12	

See Package 13

## D COMPONENT DESCRIPTIONS

### D.4 VOLTAGE REGULATORS

#### LM340K cont'd

#### absolute maximum ratings

Input Voltage ( $V_O = 5V$ through $18V$ )	35V
( $V_O = 24V$ )	40V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range	0°C to 70°C
Maximum Junction Temperature	
TO-3 Package	150°C
TO-220 Package	150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature	
TO-3 Package (Soldering, 10 sec)	300°C
TO-220 Package (Soldering, 10 sec)	230°C

#### electrical characteristics

LM340-5 ( $V_{IN} = 10V$ ,  $I_{OUT} = 500$  mA,  $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ , unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	$T_j = 25^\circ\text{C}$	4.8	5	5.2	V
Line Regulation	$T_j = 25^\circ\text{C}$ , $7V \leq V_{IN} \leq 25V$ $I_{OUT} = 100$ mA $I_{OUT} = 500$ mA			50	mV
				100	mV
Load Regulation	$T_j = 25^\circ\text{C}$ , $5$ mA $\leq I_{OUT} \leq 1.5$ A			100	mV
Output Voltage	$7V \leq V_{IN} \leq 20V$ , $5$ mA $\leq I_{OUT} \leq 1.0$ A $P_D \leq 15W$	4.75		5.25	V
Quiescent Current	$T_j = 25^\circ\text{C}$		7	10	mA
Quiescent Current Change	$7V \leq V_{IN} \leq 25V$ $5$ mA $\leq I_{OUT} \leq 1.5$ A			1.3	mA
				.5	mA
Output Noise Voltage	$T_A = 25^\circ\text{C}$ , $10$ Hz $\leq f \leq 100$ kHz		40		$\mu\text{V}$
Long Term Stability				20	mV/1000 hr
Ripple Rejection	$I_{OUT} = 20$ mA, $f = 120$ Hz		60		dB
Dropout Voltage	$T_j = 25^\circ\text{C}$ , $I_{OUT} = 1.0$ A		2		V

LM340-6 ( $V_{IN} = 11V$ ,  $I_{OUT} = 500$  mA,  $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ , unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	$T_j = 25^\circ\text{C}$	5.75	6	6.25	V
Line Regulation	$T_j = 25^\circ\text{C}$ , $8V \leq V_{IN} \leq 25V$ $I_{OUT} = 100$ mA $I_{OUT} = 500$ mA			60	mV
				120	mV
Load Regulation	$T_j = 25^\circ\text{C}$ , $5$ mA $\leq I_{OUT} \leq 1.5$ A			120	mV
Output Voltage	$8V \leq V_{IN} \leq 21V$ , $5$ mA $\leq I_{OUT} \leq 1.0$ A $P_D \leq 15W$	5.7		6.3	V
Quiescent Current	$T_j = 25^\circ\text{C}$		7	10	mA
Quiescent Current Change	$8V \leq V_{IN} \leq 25V$ $5$ mA $\leq I_{OUT} \leq 1.5$ A			1.3	mA
				.5	mA
Output Noise Voltage	$T_A = 25^\circ\text{C}$ , $10$ Hz $\leq f \leq 100$ kHz		45		$\mu\text{V}$
Long Term Stability				24	mV/1000 hr
Ripple Rejection	$I_{OUT} = 20$ mA, $f = 120$ Hz		57		dB
Dropout Voltage	$T_j = 25^\circ\text{C}$ , $I_{OUT} = 1.0$ A		2		V

Note 1: Thermal resistance without a heat sink for junction to case temperature is  $4^\circ\text{C/W}$  for the TO-3 package and  $6^\circ\text{C/W}$  for the TO-220 package. Thermal resistance for case to ambient temperature is  $35^\circ\text{C/W}$  for the TO-3 package and  $50^\circ\text{C/W}$  for the TO-220 package.

D COMPONENT DESCRIPTIONS

D.4 VOLTAGE REGULATORS

LM340x cont'd

electrical characteristics (cont)

LM340-9 ( $V_{IN} = 14V$ ,  $I_{OUT} = 500\text{ mA}$ ,  $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ , unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	$T_J = 25^\circ\text{C}$	7.7	8	8.3	V
Line Regulation	$T_J = 25^\circ\text{C}$ , $10.5V \leq V_{IN} \leq 25V$ $I_{OUT} = 100\text{ mA}$ $I_{OUT} = 500\text{ mA}$			80 160	mV mV
Load Regulation	$T_J = 25^\circ\text{C}$ , $5\text{ mA} \leq I_{OUT} \leq 1.5A$			160	mV
Output Voltage	$10.5V \leq V_{IN} \leq 23V$ , $5\text{ mA} \leq I_{OUT} \leq 1.0A$ $P_D \leq 15W$	7.6		8.1	V
Quiescent Current	$T_J = 25^\circ\text{C}$		7	10	mA
Quiescent Current Change	$10.5V \leq V_{IN} \leq 25V$ $5\text{ mA} \leq I_{OUT} \leq 1.5A$			1 5	mA mA
Output Noise Voltage	$T_A = 25^\circ\text{C}$ , $10\text{ Hz} \leq f \leq 100\text{ kHz}$		52		$\mu\text{V}$
Long Term Stability				32	mV/1000 hr
Ripple Rejection	$I_{OUT} = 20\text{ mA}$ , $f = 120\text{ Hz}$		55		dB
Dropout Voltage	$T_J = 25^\circ\text{C}$ , $I_{OUT} = 1.0A$		2		V

LM340-12 ( $V_{IN} = 19V$ ,  $I_{OUT} = 500\text{ mA}$ ,  $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ , unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	$T_J = 25^\circ\text{C}$	11.5	12	12.5	V
Line Regulation	$T_J = 25^\circ\text{C}$ , $14.5V \leq V_{IN} \leq 30V$ $I_{OUT} = 100\text{ mA}$ $I_{OUT} = 500\text{ mA}$			120 240	mV mV
Load Regulation	$T_J = 25^\circ\text{C}$ , $5\text{ mA} \leq I_{OUT} \leq 1.5A$			240	mV
Output Voltage	$14.5V \leq V_{IN} \leq 27V$ , $5\text{ mA} \leq I_{OUT} \leq 1.0A$ $P_D \leq 15W$	11.4		12.6	V
Quiescent Current	$T_J = 25^\circ\text{C}$		7	10	mA
Quiescent Current Change	$14.5V \leq V_{IN} \leq 30V$ $5\text{ mA} \leq I_{OUT} \leq 1.5A$			1 5	mA mA
Output Noise Voltage	$T_A = 25^\circ\text{C}$ , $10\text{ Hz} \leq f \leq 100\text{ kHz}$		75		$\mu\text{V}$
Long Term Stability				48	mV/1000 hr
Ripple Rejection	$I_{OUT} = 20\text{ mA}$ , $f = 120\text{ Hz}$		52		dB
Dropout Voltage	$T_J = 25^\circ\text{C}$ , $I_{OUT} = 1.0A$		2		V

LM340-15 ( $V_{IN} = 23V$ ,  $I_{OUT} = 500\text{ mA}$ ,  $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ , unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	$T_J = 25^\circ\text{C}$	14.4	15	15.6	V
Line Regulation	$T_J = 25^\circ\text{C}$ , $17.5V \leq V_{IN} \leq 30V$ $I_{OUT} = 100\text{ mA}$ $I_{OUT} = 500\text{ mA}$			150 300	mV mV
Load Regulation	$T_J = 25^\circ\text{C}$ , $5\text{ mA} \leq I_{OUT} \leq 1.5A$			300	mV
Output Voltage	$17.5V \leq V_{IN} \leq 30V$ , $5\text{ mA} \leq I_{OUT} \leq 1.0A$ $P_D \leq 15W$	14.25		15.75	V
Quiescent Current	$T_J = 25^\circ\text{C}$		7	10	mA
Quiescent Current Change	$17.5V \leq V_{IN} \leq 30V$ $5\text{ mA} \leq I_{OUT} \leq 1.5A$			1 5	mA mA
Output Noise Voltage	$T_A = 25^\circ\text{C}$ , $10\text{ Hz} \leq f \leq 100\text{ kHz}$		60		$\mu\text{V}$
Long Term Stability				60	mV/1000 hr
Ripple Rejection	$I_{OUT} = 20\text{ mA}$ , $f = 120\text{ Hz}$		50		dB
Dropout Voltage	$T_J = 25^\circ\text{C}$ , $I_{OUT} = 1.0A$		2		V

D COMPONENT DESCRIPTIONS  
 D.4 VOLTAGE REGULATORS

LM340K cont'd

electrical characteristics (con't)

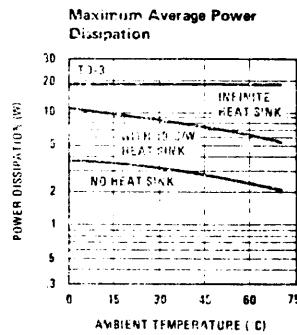
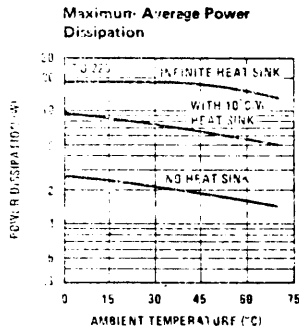
LM340-18 ( $V_{IN} = 27V$ ,  $I_{OUT} = 500\text{ mA}$ ,  $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ , unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	$T_J = 25^\circ\text{C}$	17.2	18	18.7	V
Line Regulation	$T_J = 25^\circ\text{C}$ , $21V \leq V_{IN} \leq 33V$ $I_{OUT} = 100\text{ mA}$			150	mV
	$I_{OUT} = 500\text{ mA}$			360	mV
Load Regulation	$T_J = 25^\circ\text{C}$ , $5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$			360	mV
Output Voltage	$21V \leq V_{IN} \leq 33V$ , $5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$ $P_D \leq 15W$	17.1		18.9	V
Quiescent Current	$T_J = 25^\circ\text{C}$		7	10	mA
Quiescent Current Change	$21V \leq V_{IN} \leq 33V$ $5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$			1	mA
				5	mA
Output Noise Voltage	$T_A = 25^\circ\text{C}$ , $10\text{ Hz} < f < 100\text{ kHz}$		110		$\mu\text{V}$
Long Term Stability				72	mV/1000 hr
Ripple Rejection	$I_{OUT} = 20\text{ mA}$ , $f = 120\text{ Hz}$		48		dB
Dropout Voltage	$T_J = 25^\circ\text{C}$ , $I_{OUT} = 1.0\text{ A}$		2		V

LM340-24 ( $V_{IN} = 30V$ ,  $I_{OUT} = 500\text{ mA}$ ,  $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ , unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	$T_J = 25^\circ\text{C}$	23	24	25	V
Line Regulation	$T_J = 25^\circ\text{C}$ , $27V \leq V_{IN} \leq 38V$ $I_{OUT} = 100\text{ mA}$			240	mV
	$I_{OUT} = 500\text{ mA}$			480	mV
Load Regulation	$T_J = 25^\circ\text{C}$ , $5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$			480	mV
Output Voltage	$27V \leq V_{IN} \leq 38V$ , $5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$ $P_D \leq 15W$	22.8		25.2	V
Quiescent Current	$T_J = 25^\circ\text{C}$		7	10	mA
Quiescent Current Change	$27V \leq V_{IN} \leq 38V$ $5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$			1	mA
				5	mA
Output Noise Voltage	$T_A = 25^\circ\text{C}$ , $10\text{ Hz} < f < 100\text{ kHz}$		170		$\mu\text{V}$
Long Term Stability				96	mV/1000 hr
Ripple Rejection	$I_{OUT} = 20\text{ mA}$ , $f = 120\text{ Hz}$		44		dB
Dropout Voltage	$T_J = 25^\circ\text{C}$ , $I_{OUT} = 1.0\text{ A}$		2		V

typical performance characteristics

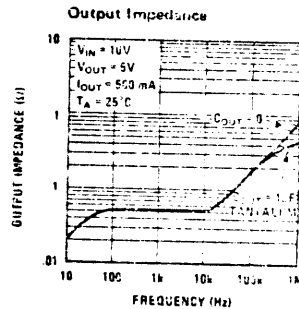
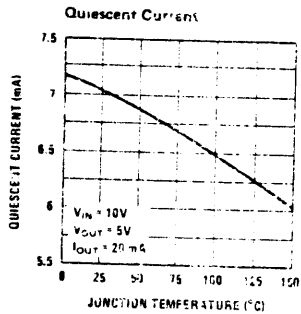
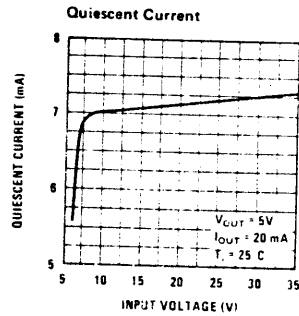
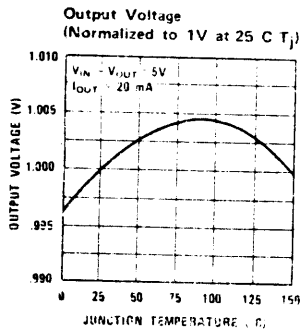
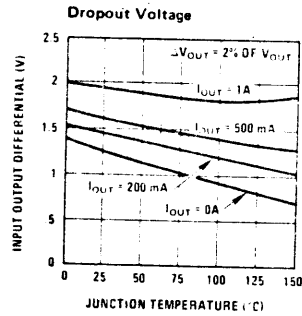
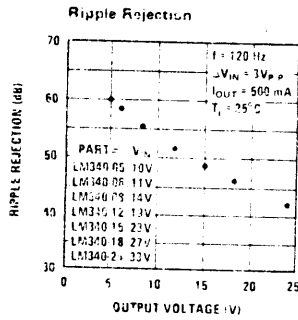
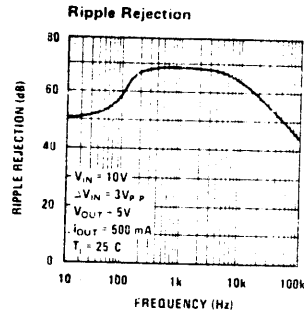
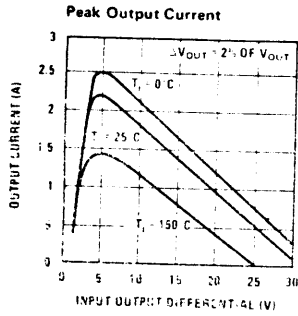




D COMPONENT DESCRIPTIONS  
 D.4 VOLTAGE REGULATORS

LM340K cont'd

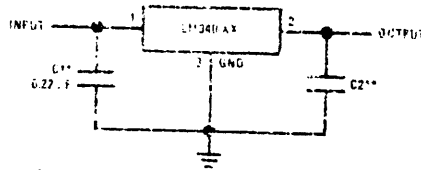
typical performance characteristics (con't)



D COMPONENT DESCRIPTIONS  
 D.4 VOLTAGE REGULATORS

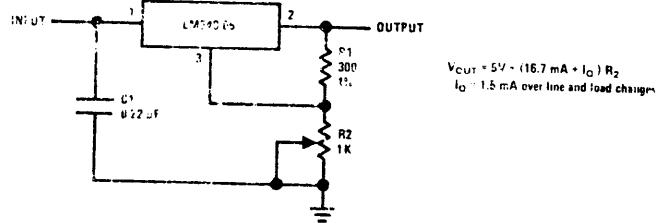
LM340K cont'd  
 typical applications

Fixed Output Regulator

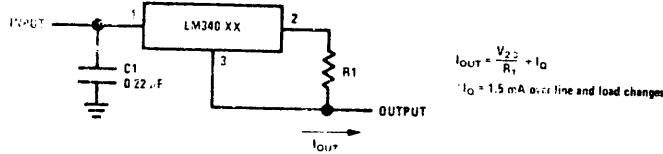


\*REQUIRED IF THE REGULATOR IS LOCATED FAR FROM THE POWER SUPPLY FILTER.  
 \*\*ALTHOUGH NO OUTPUT CAPACITOR IS REQUIRED FOR STABILITY, IT DOES HELP TRANSIENT RESPONSE. (IF NEEDED USE 2.1 F. ELECTRIC DISC)

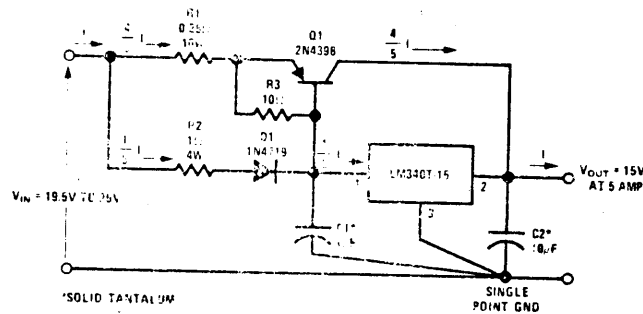
Adjustable Output Regulator



Current Regulator



15V 5 Amp Regulator With Short Circuit Current Limit

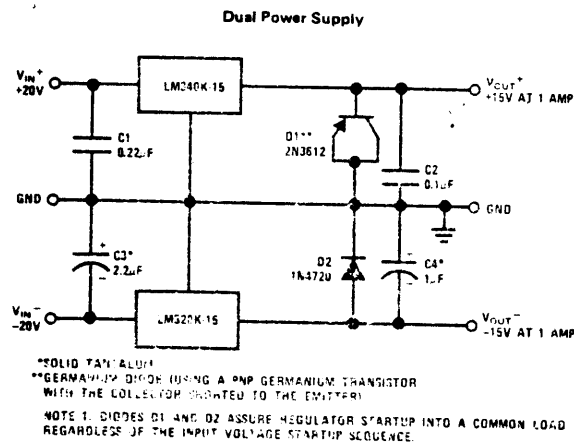
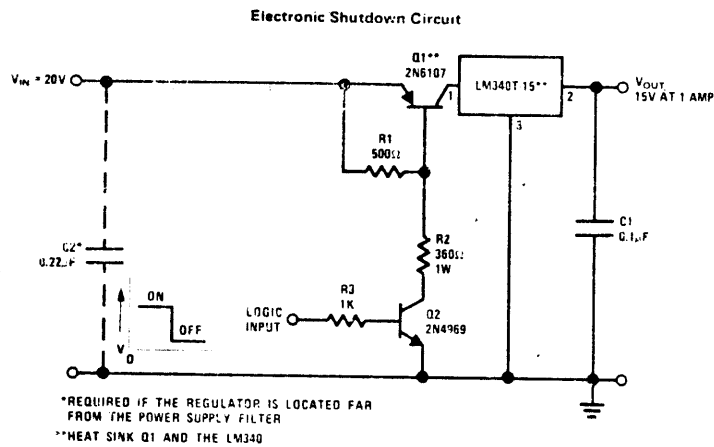
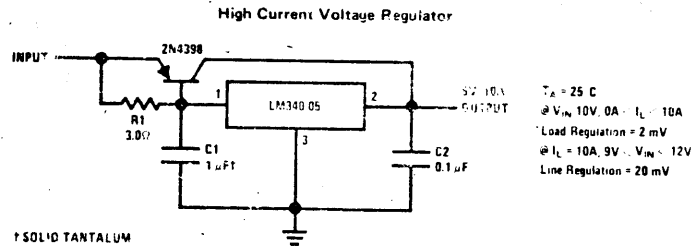


\*SOLID TANTALUM  
 NOTE 1: CURRENT DIVIDING BETWEEN THE LM340 AND Q1 ALLOWS THE EXTENSION OF SHORT CIRCUIT CURRENT LIMIT, SAFE OPERATING AREA PROTECTION, AND (ASSUMING Q1) R. 6.5 WATT AND 100 μS TIME THE CAPACITY OF THE LM340 HEAT SINK) THERMAL SHUTDOWN PROTECTION.  
 NOTE 2: SHORT CIRCUIT I IS APPROXIMATELY 5.5 AMP.  
 NOTE 3: Iout max. AT Vout = 15V IS APPROXIMATELY 9.5 AMP

D COMPONENT DESCRIPTIONS  
 D.4 VOLTAGE REGULATORS

LM340K cont'd

typical applications (con't)



**D COMPONENT DESCRIPTIONS**  
**D.5 VOLTAGE COMPARATOR**

**LM311**

**general description**

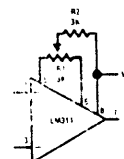
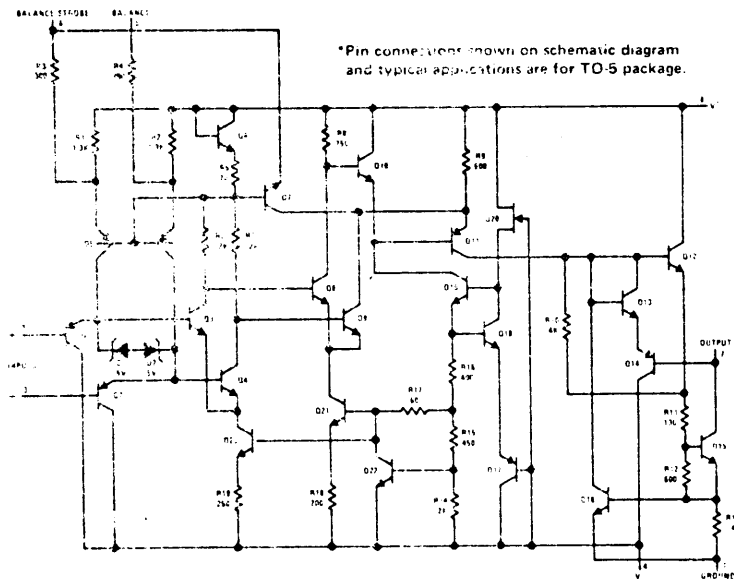
The LM311 is a voltage comparator that has more current than a hundred times faster than devices like the LM308 or LM710C. It is also designed to operate over a wider range of supply voltages: from standard  $\pm 15V$  op amp supplies down to the single 5V supply used for IC logic. Its output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, it can drive lamps or relays, switching voltages up to 40V at currents as high as 50 mA.

**features**

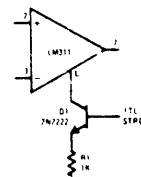
- Operates from single 5V supply
- Maximum input current: 250 nA
- Maximum offset current: 50 nA
- Differential input voltage range:  $\pm 130V$
- Power consumption: 135 mW at  $\pm 15V$

Both the input and the output of the LM311 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be in either OE or  $\bar{O}$ . Although slower than the LM308 and LM710C (200 ns response time vs 40 ns), the device is also much less prone to spurious oscillations. The LM311 has the same pin configuration as the LM308 and LM710C.

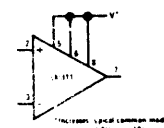
**schematic diagram and auxiliary circuits**



Offset Balancing

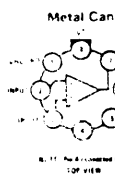


Strob ing

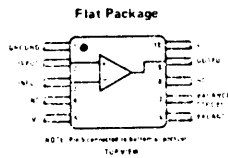


Increasing Input Stage Current\*

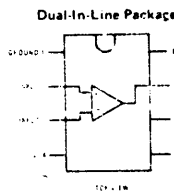
**connection diagrams \***



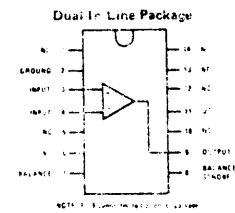
Order Number LM311H  
See Package 11



Order Number LM311F  
See Package 12



Order Number LM311N  
See Package 20



Order Number LM311D  
See Package 1 or  
Order Number LM311N-14  
See Package 22

**D COMPONENT DESCRIPTIONS**  
**D.5 VOLTAGE COMPARATOR**

LM311 cont'd

**absolute maximum ratings**

Total Supply Voltage ( $V_{PS}$ )	36V
Output to Negative Supply Voltage ( $V_{OL}$ )	40V
Ground to Negative Supply Voltage ( $V_{GL}$ )	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (soldering, 10 sec)	300°C

**electrical characteristics (Note 3)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25^\circ\text{C}$ , $R_S \leq 50\text{K}$		2.0	7.5	mV
Input Offset Current (Note 4)	$T_A = 25^\circ\text{C}$		5.0	30	nA
Input Bias Current	$T_A = 25^\circ\text{C}$		100	250	nA
Voltage Gain	$T_A = 25^\circ\text{C}$		200		V/mV
Response Time (Note 5)	$T_A = 25^\circ\text{C}$		300		ns
Saturation Voltage	$V_{IN} \leq -10\text{ mV}$ , $I_{OUT} = 50\text{ mA}$ $T_A = 25^\circ\text{C}$		0.75	1.5	V
Strobe On Current	$T_A = 25^\circ\text{C}$		3.0		mA
Output Leakage Current	$V_{IN} \geq 10\text{ mV}$ , $V_{OUT} = 35\text{V}$ $T_A = 25^\circ\text{C}$		0.2	50	nA
Input Offset Voltage (Note 4)	$R_S \leq 50\text{K}$			10	mV
Input Offset Current (Note 4)				70	nA
Input Bias Current				300	nA
Input Voltage Range			±14		V
Saturation Voltage	$V_{IN}^+ \geq 4.5\text{V}$ , $V_{IN}^- = 0$ $V_{IN} \leq -10\text{ mV}$ , $I_{SINK} \leq 8\text{ mA}$		0.23	0.4	V
Positive Supply Current	$T_A = 25^\circ\text{C}$		5.1	7.5	mA
Negative Supply Current	$T_A = 25^\circ\text{C}$		4.1	5.0	mA

Note 1: The rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LM311 is 150°C. For operating at elevated temperatures, devices in the TO-8 package must be derated based on a thermal resistance of 151°C/W (junction to ambient) or 45°C/W (junction to case). For the flat package, the derating is based on a thermal resistance of 165°C/W when mounted on a 1.16-inch thick, 0.005-inch gap board with ten 0.003-inch-wide, 2-ounce copper conductors. The thermal resistance of the quad-line package is 100°C/W (junction to ambient).

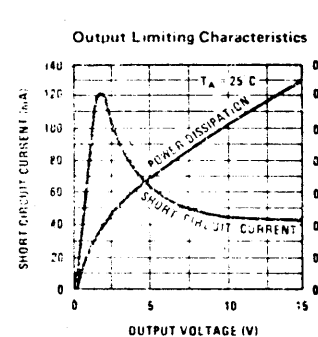
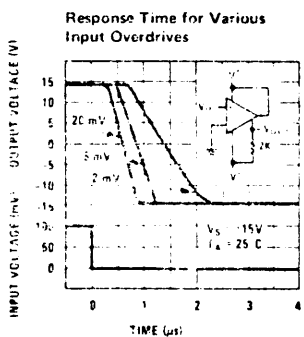
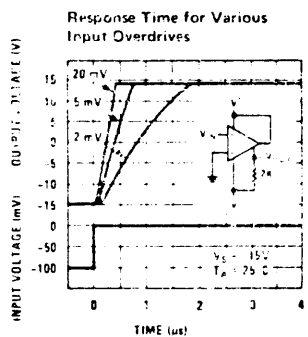
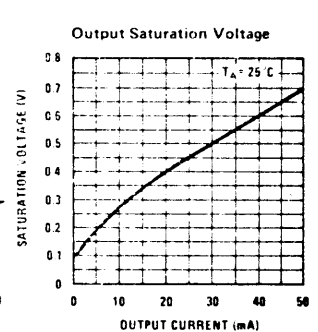
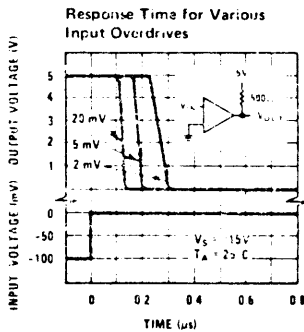
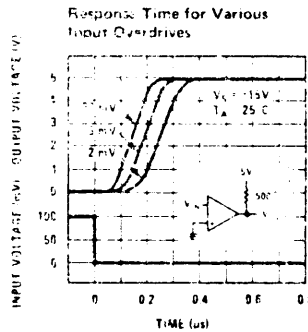
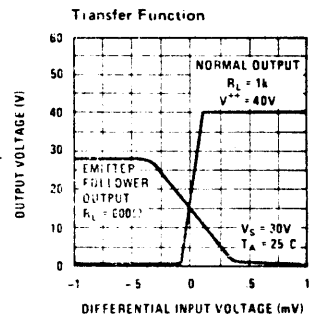
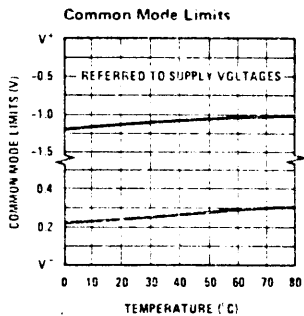
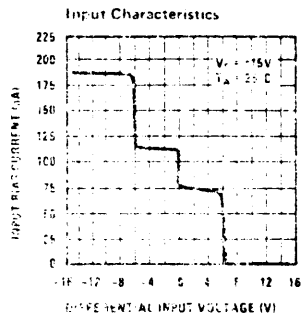
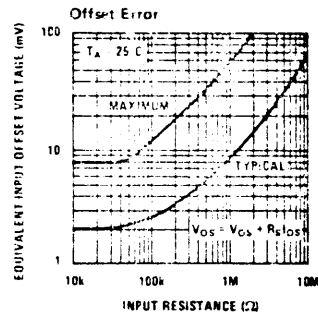
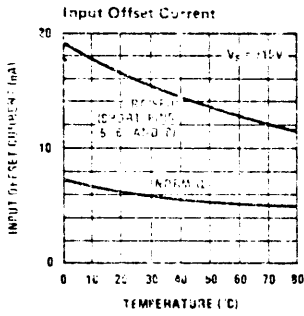
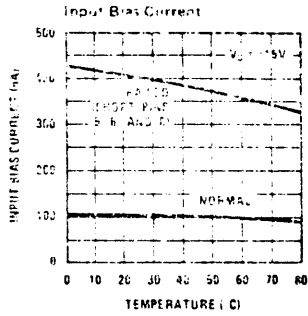
Note 3: These specifications apply for  $V_{PS} = \pm 15\text{V}$  and  $0^\circ\text{C} < T_A < 70^\circ\text{C}$ , unless otherwise specified. The offset voltage,  $I_{SINK}$  current, and bias current specifications apply for any supply voltage from a single 5V supply up to dual supplies.

Note 4: The offset voltages and offset currents given are the maximum values measured to drive the output within a voltage of 1 mV of unity with 1 mA load. These values are given for an error signal and take into account the offset error effect on voltage gain and output impedance.

Note 5: The response time specified (see definition) is for a 100 mV input step with 5 mV overdrive.

D COMPONENT DESCRIPTIONS  
 D.5 VOLTAGE COMPARATOR

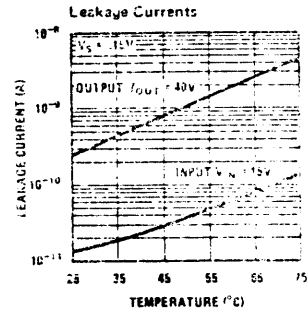
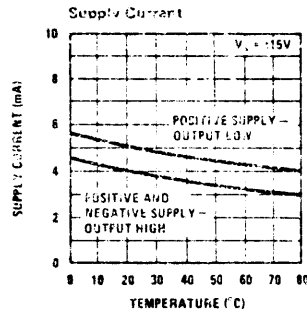
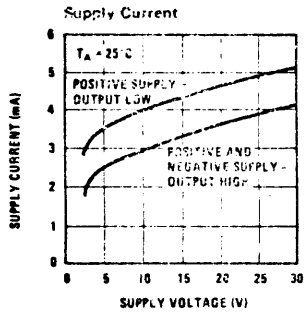
LM311 cont'd  
 typical performance characteristics



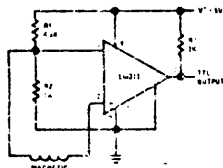
D COMPONENT DESCRIPTIONS  
 D.5 VOLTAGE COMPARATOR

LM311 cont'd

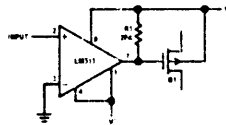
typical performance characteristics (cont')



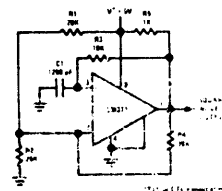
typical applications



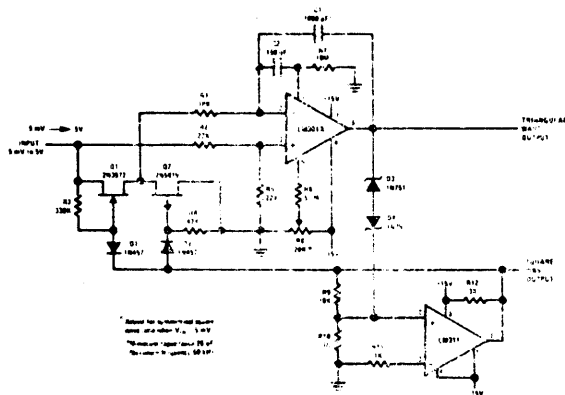
Detector for Magnetic Transducer



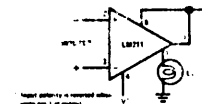
Zero Crossing Detector Driving MOS Switch



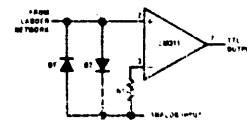
100 kHz Free Running Multivibrator



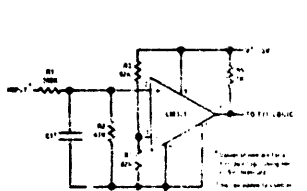
10 Hz to 10 kHz Voltage Controlled Oscillator



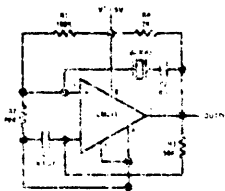
Driving Ground-Referred Load



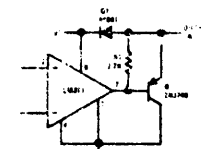
Using Clamp Diodes to Improve Response



TTL Interface with High Level Logic



Crystal Oscillator

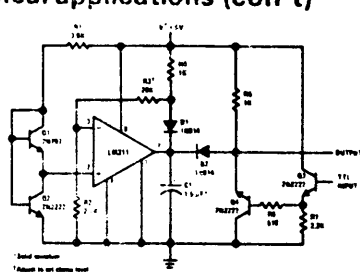


Comparator and Solenoid Driver

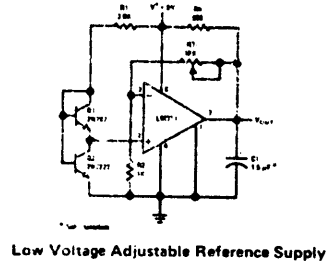
D COMPONENT DESCRIPTION  
 D.5 VOLTAGE COMPARATOR

LM311 cont'd

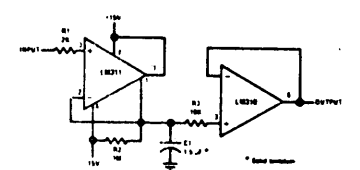
typical applications (con't)



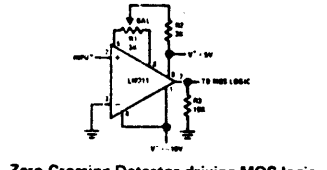
Precision Squarer



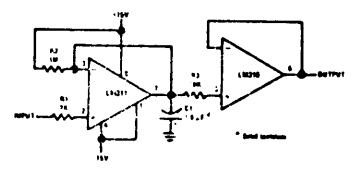
Low Voltage Adjustable Reference Supply



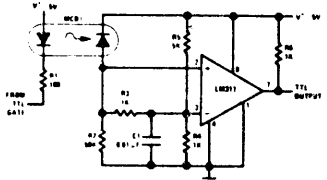
Positive Peak Detector



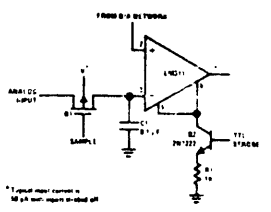
Zero Crossing Detector driving MOS logic



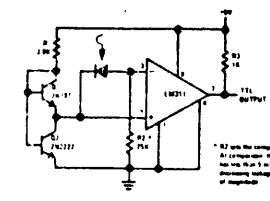
Negative Peak Detector



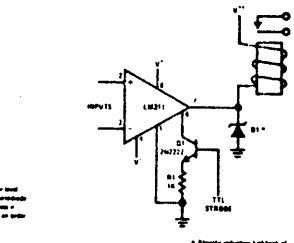
Digital Transmission Isolator



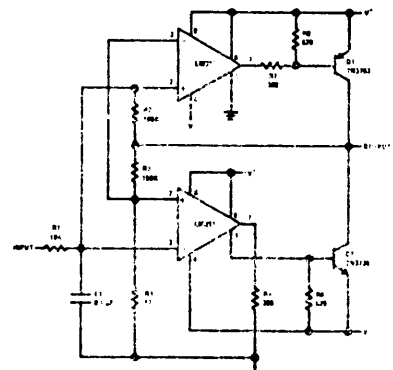
Strobing off Both Input\* and Output Stages



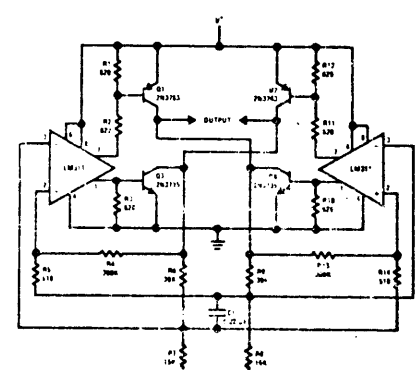
Precision Photodiode Comparator



Relay Driver with Strobe



Switching Power Amplifier



Switching Power Amplifier



D COMPONENT DESCRIPTIONS

D.6 INTEGRATED CIRCUITS

555

DESCRIPTION

The NE/SE 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA or drive TTL circuits.

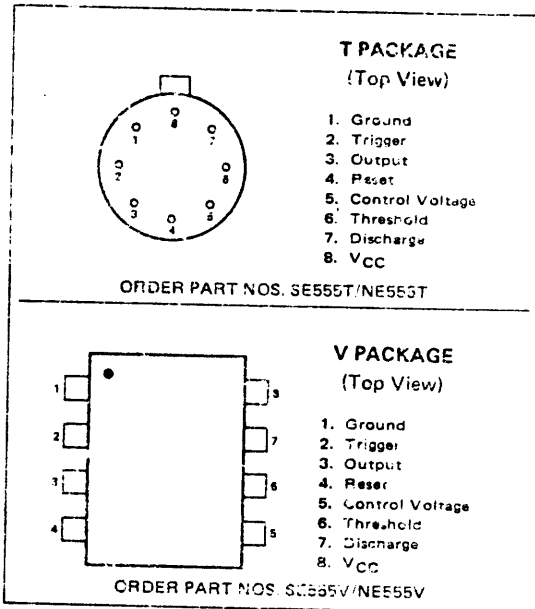
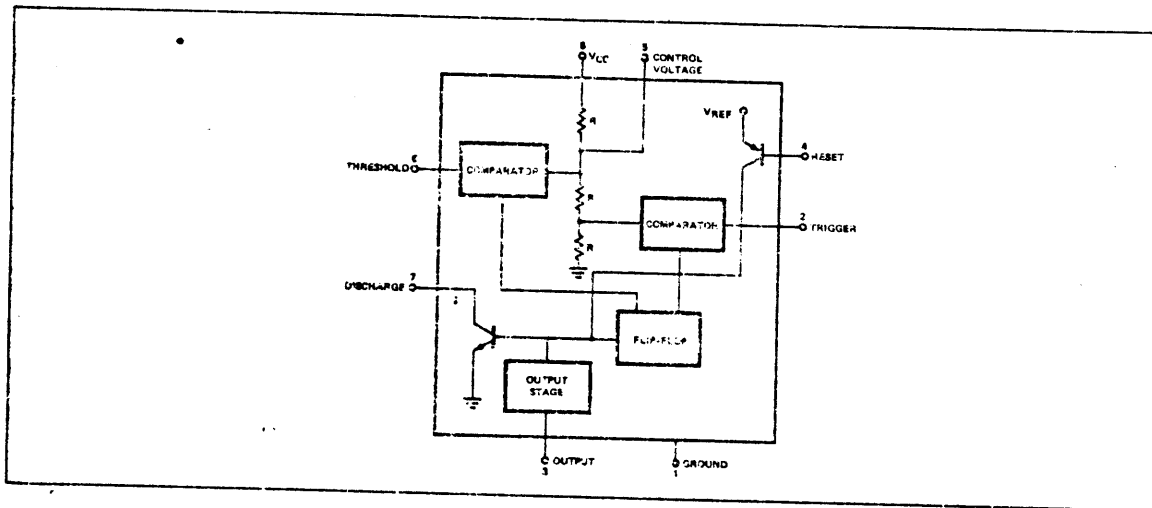
FEATURES

- TIMING FROM MICROSECONDS THROUGH HOURS
- OPERATES IN BOTH ASTABLE AND MONOSTABLE MODES
- ADJUSTABLE DUTY CYCLE
- HIGH CURRENT OUTPUT CAN SOURCE OR SINK 200mA
- OUTPUT CAN DRIVE TTL
- TEMPERATURE STABILITY OF 0.005% PER °C
- NORMALLY ON AND NORMALLY OFF OUTPUT

APPLICATIONS

- PRECISION TIMING
- PULSE GENERATION
- SEQUENTIAL TIMING
- TIME DELAY GENERATION
- PULSE WIDTH MODULATION
- PULSE POSITION MODULATION
- MISSING PULSE DETECTOR

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+18V
Power Dissipation	600 mW
Operating Temperature Range	
NE555	0°C to +70°C
SE555	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	+300°C

D COMPONENT DESCRIPTIONS  
D.6 INTEGRATED CIRCUITS

555 cont'd

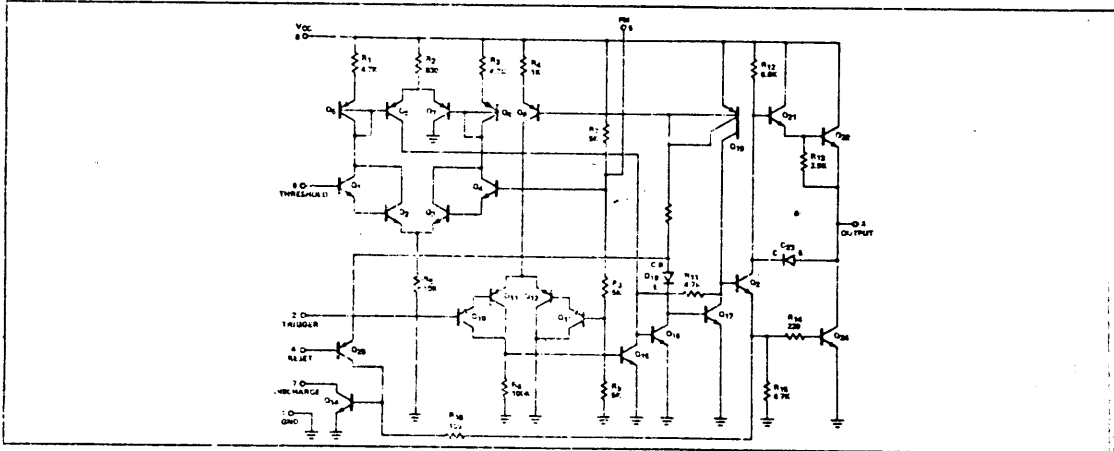
ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ ,  $V_{CC} = +5\text{V}$  to  $+15\text{V}$  unless otherwise specified)

PARAMETER	TEST CONDITIONS	SE 555			NE 555			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	$V_{CC} = 5\text{V}$ $R_L = \infty$		3	5		3	6	mA
	$V_{CC} = 15\text{V}$ $R_L = \infty$		10	12		10	15	mA
	Low State, Note 1							
Timing Error	$R_A, R_B = 1\text{K}\Omega$ to $100\text{K}\Omega$							
Initial Accuracy	$C = 0.1\mu\text{F}$ Note 2		0.5	2		1		%
Drift with Temperature			30	100		50		ppm/ $^\circ\text{C}$
Drift with Supply Voltage			0.005	0.02		0.01		%/Volt
Threshold Voltage			2/3			2/3		$\times V_{CC}$
Trigger Voltage	$V_{CC} = 15\text{V}$	4.8	5	5.2		5		V
	$V_{CC} = 5\text{V}$	1.45	1.67	1.9		1.67		V
Trigger Current			0.5			0.5		$\mu\text{A}$
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current			0.1			0.1		mA
Threshold Current	Note 3		0.1	.25		0.1	.25	$\mu\text{A}$
Control Voltage Level	$V_{CC} = 15\text{V}$	9.6	10	10.4	9.0	10	11	V
	$V_{CC} = 5\text{V}$	2.9	3.33	3.8	2.6	3.33	4	V
Output Voltage $\leq$ $V_{OH}$ (low)	$V_{CC} = 15\text{V}$							
	$I_{SINK} = 10\text{mA}$		0.1	0.15		0.1	.25	V
	$I_{SINK} = 50\text{mA}$		0.4	0.5		0.4	.75	V
	$I_{SINK} = 100\text{mA}$		2.0	2.2		2.0	2.5	V
	$I_{SINK} = 200\text{mA}$		2.5			2.5		V
	$V_{CC} = 5\text{V}$							
	$I_{SINK} = 8\text{mA}$		0.1	0.25				V
	$I_{SINK} = 5\text{mA}$					.25	.35	V
Output Voltage Drop (high)	$I_{SOURCE} = 200\text{mA}$		12.5			12.5		V
	$V_{CC} = 15\text{V}$							
	$I_{SOURCE} = 100\text{mA}$							
	$V_{CC} = 15\text{V}$	13.0	13.3		12.75	13.3		V
	$V_{CC} = 5\text{V}$	3.0	3.3		2.75	3.3		V
Rise Time of Output			100			100		nsec
Fall Time of Output			100			100		nsec

NOTES:

- Supply Current when output high typically 1mA less.
- Tested at  $V_{CC} = 5\text{V}$  and  $V_{CC} = 15\text{V}$
- This will determine the maximum value of  $R_A + R_B$ . For 15V operation, the max total  $R = 20$  megohm.

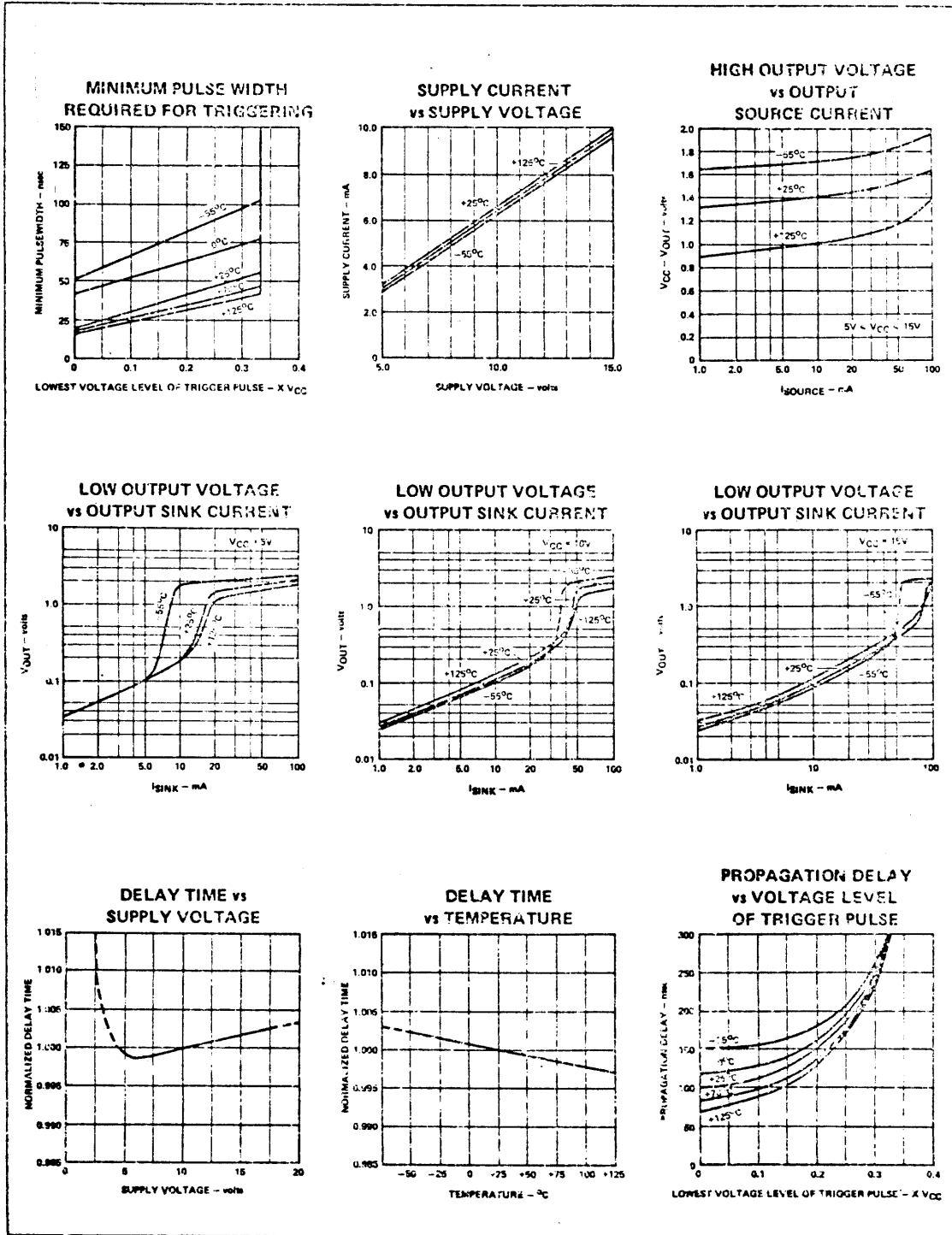
EQUIVALENT CIRCUIT



D COMPONENT DESCRIPTIONS  
 D.6 INTEGRATED CIRCUITS

555 cont'd

TYPICAL CHARACTERISTICS



D COMPONENT DESCRIPTIONS  
 D.6 INTEGRATED CIRCUITS

555 cont'd

APPLICATIONS INFORMATION  
 MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot. Referring to Figure 1a the external capacitor is initially held discharged by a transistor inside the timer.

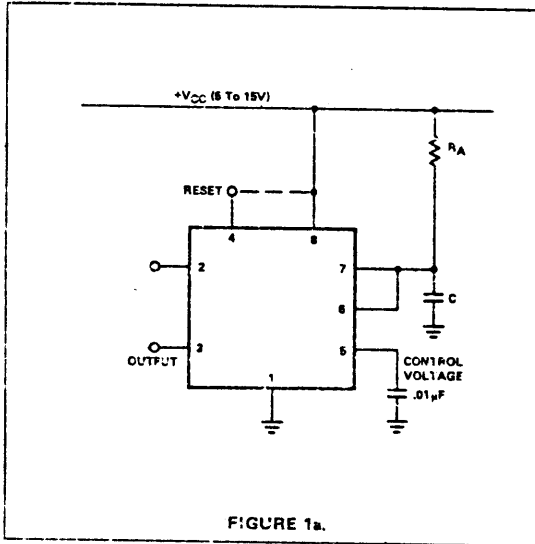
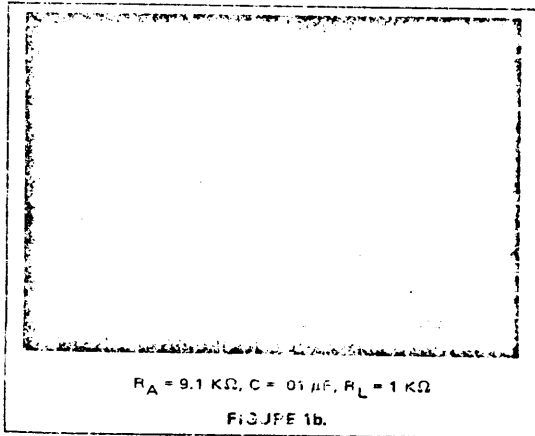


FIGURE 1a.

Upon application of a negative trigger pulse to pin 2, the flip-flop is set which releases the short circuit across the external capacitor and drives the output high. The voltage across the capacitor, now, increases exponentially with the time constant  $\tau = R_A C$ . When the voltage across the capacitor equals  $2/3 V_{CC}$ , the comparator resets the flip-flop which in turn discharges the capacitor rapidly and drives the output to its low state. Figure 1b shows the actual waveforms generated in this mode of operation.

The circuit triggers on a negative going input signal when the level reaches  $1/3 V_{CC}$ . Once triggered, the circuit will remain in this state until the set time is elapsed, even if it is triggered again during this interval. The time that the



$R_A = 9.1 \text{ K}\Omega$ ,  $C = .01 \mu\text{F}$ ,  $R_L = 1 \text{ K}\Omega$

FIGURE 1b.

output is in the high state is given by  $t = 1.1 R_A C$  and can easily be determined by Figure 1c. Notice that since the charge rate, and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the reset terminal (pin 4) and the trigger terminal (pin 2) during the timing cycle discharges the external capacitor and causes the cycle to start over again. The timing cycle will now commence on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its low state.

When the reset function is not in use, it is recommended that it be connected to  $V_{CC}$  to avoid any possibility of false triggering.

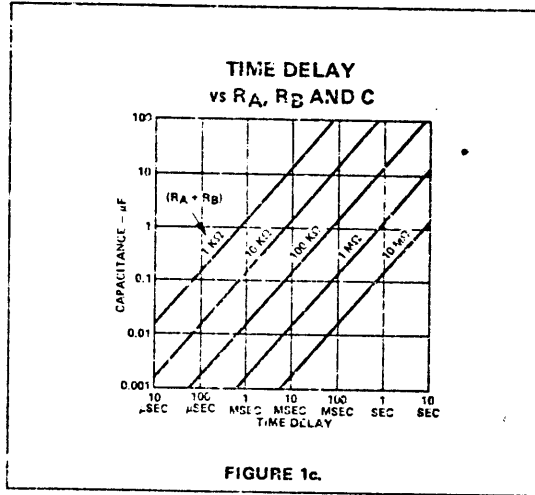


FIGURE 1c.

ASTABLE OPERATION

If the circuit is connected as shown in Figure 2a (pins 2 and 6 connected) it will trigger itself and free run as a multi-vibrator. The external capacitor charges through  $R_A$  and  $R_B$  and discharges through  $R_B$  only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

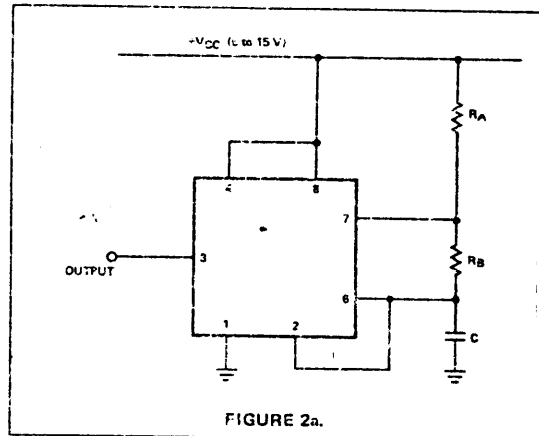


FIGURE 2a.

D COMPONENT DESCRIPTIONS  
 D.6 INTEGRATED CIRCUITS

741

DESCRIPTION

The  $\mu A741$  is a high performance operational amplifier with high open loop gain, internal compensation, high common mode range and exceptional temperature stability. The  $\mu A741$  is short-circuit protected and allows for nulling of offset voltage.

FEATURES

- INTERNAL FREQUENCY COMPENSATION
- SHORT CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- EXCELLENT TEMPERATURE STABILITY
- HIGH INPUT VOLTAGE RANGE
- NO LATCH-UP

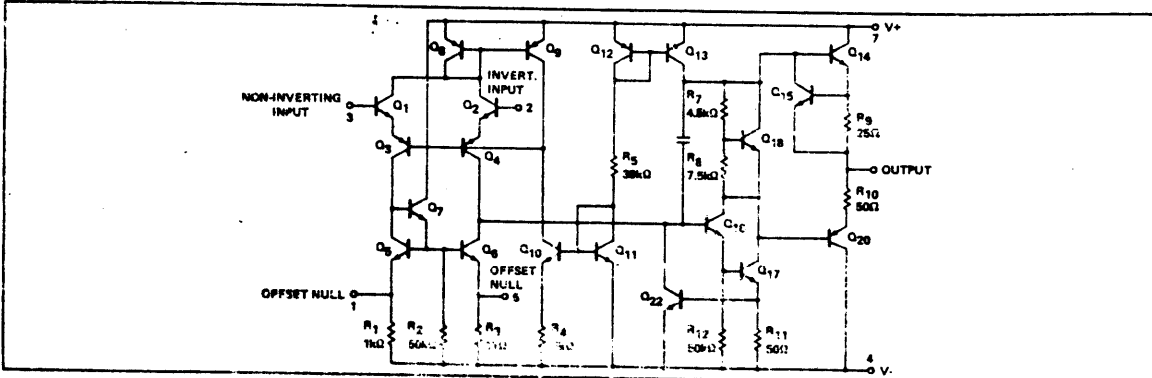
ABSOLUTE MAXIMUM RATINGS

	$\mu A741C$	$\mu A741$
Supply Voltage	$\pm 18V$	$\pm 22V$
Internal Power		
Dissipation (Note 1)	500mW	500mW
Differential Input Voltage	$\pm 30V$	$\pm 30V$
Input Voltage (Note 2)	$\pm 15V$	$\pm 15V$
Voltage between Offset Null and $V^-$	$\pm 0.5V$	$\pm 0.5V$
Operating Temperature		
Range	$0^\circ C$ to $+70^\circ C$	$-55^\circ C$ to $+125^\circ C$
Storage Temperature		
Range	$-65^\circ C$ to $+150^\circ C$	$-65^\circ C$ to $+150^\circ C$
Lead Temperature		
(Solder, 60 sec)	$300^\circ C$	$300^\circ C$
Output Short Circuit Duration (Note 3)	Indefinite	Indefinite

Notes

1. Rating applies for case temperatures to  $125^\circ C$ ; derate linearly at  $8.5mW/^\circ C$  for ambient temperatures above  $+75^\circ C$ .
2. For supply voltages less than  $\pm 15V$ , the absolute maximum input voltage is equal to the supply voltages.
3. Short circuit may be to ground or either supply. Rating applies to  $+125^\circ C$  case temperature or  $+75^\circ C$  ambient temperature.

EQUIVALENT CIRCUIT



PIN CONFIGURATIONS

**A PACKAGE**  
(Top View)

1. NC
2. NC
3. Offset Null
4. Inv. Input
5. Non-Inv. Input
6. $V^-$
7. NC
8. NC
9. Offset Null
10. Output
11. $V^+$
12. NC
13. NC
14. NC

ORDER PART NO.  $\mu A741CA$

---

**T PACKAGE**

1. Offset Null
2. Inverting Input
3. Non-Inverting Input
4. $V^-$
5. Offset Null
6. Output
7. $V^+$
8. NC

ORDER PART NOS.  $\mu A741T/\mu A741CT$

---

**V PACKAGE**

1. Offset Null
2. Inv. Input
3. Non-Inv. Input
4. $V^-$
5. Offset Null
6. Output
7. $V^+$
8. NC

ORDER PART NO.  $\mu A741CV$

D COMPONENT DESCRIPTIONS  
D.6 INTEGRATED CIRCUITS

741 cont'd

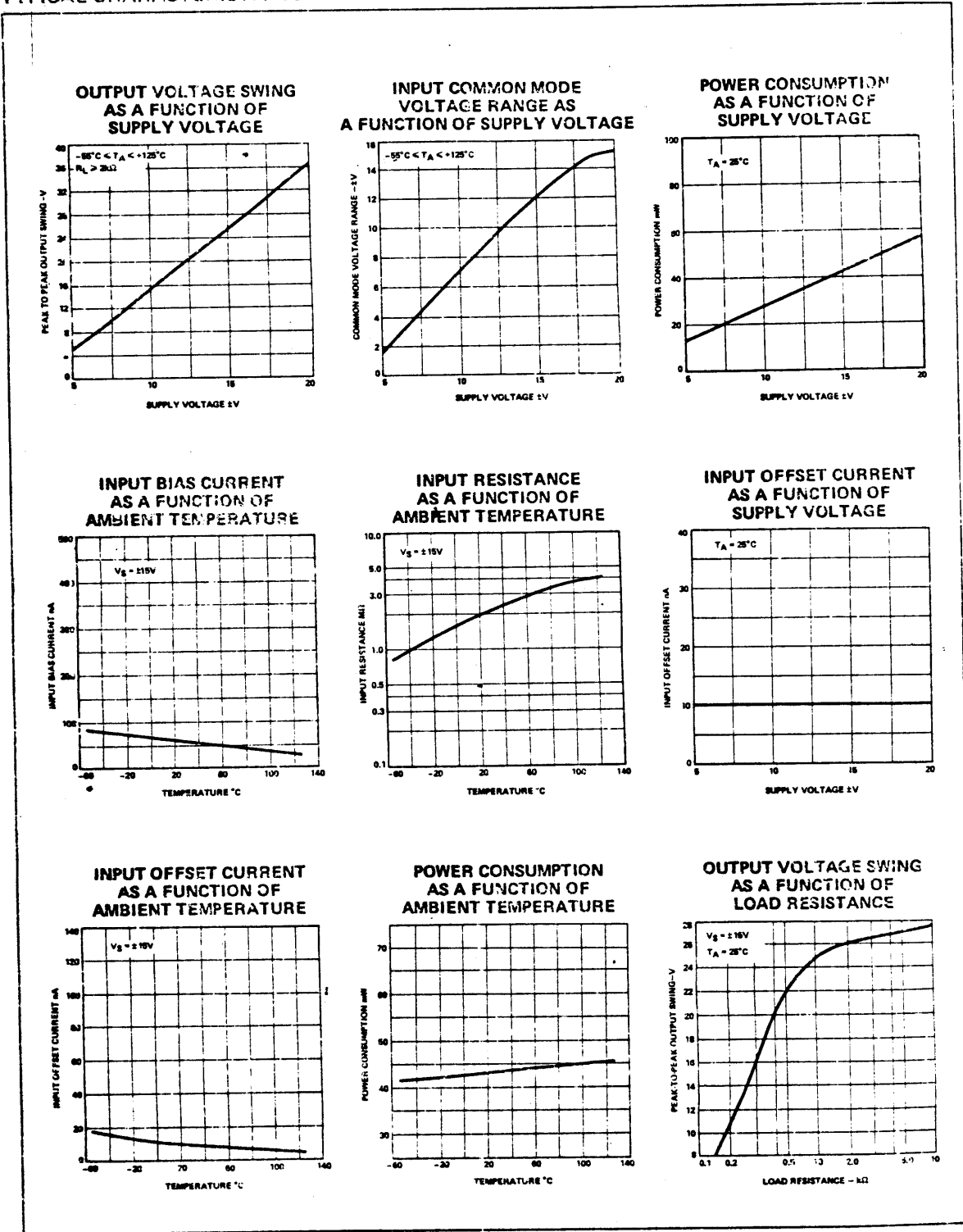
ELECTRICAL CHARACTERISTICS  $V_S = \pm 15V$ ,  $T_A = 25^\circ C$  unless otherwise specified)

PARAMETER	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
<b><math>\mu A741C</math></b>					
Input Offset Voltage		2.0	6.0	mV	$R_S < 10k\Omega$
Input Offset Current		20	200	nA	
Input Bias Current		80	500	nA	
Input Resistance	0.3	2.0		M $\Omega$	
Input Capacitance		1.4		pF	
Offset Voltage Adjustment Range		$\pm 15$		mV	
Input Voltage Range	$\pm 12$	$\pm 13$		V	
Common Mode Rejection Ratio	70	90		dB	$R_S < 10k\Omega$
Supply Voltage Rejection Ratio		10	150	$\mu V/V$	$R_S < 10k\Omega$
Large-Signal Voltage Gain	20,000	200,000			$R_L > 2k\Omega$ , $V_{out} = \pm 10V$
Output Voltage Swing	$\pm 12$ $\pm 10$	$\pm 14$ $\pm 13$		V	$R_L > 10k\Omega$ $R_L > 2k\Omega$
Output Resistance		75		$\Omega$	
Output Short-Circuit Current		25		mA	
Supply Current		1.4	2.8	mA	
Power Consumption		50	85	mW	
Transient Response (unity gain)					$V_{in} = 20mV$ , $R_L = 2k\Omega$ , $C_L < 100pF$
Risetime		0.3		$\mu s$	
Overshoot		5.0		%	
Slew Rate		0.5		V/ $\mu s$	$R_L > 2k\Omega$
The following specifications apply for $0^\circ C < T_A < +70^\circ C$					
Input Offset Voltage			7.5	mV	
Input Offset Current			300	nA	
Input Bias Current			800	nA	
Large-Signal Voltage Gain	15,000				$R_L > 2k\Omega$ , $V_{out} = \pm 10V$
Output Voltage Swing	$\pm 10$	$\pm 13$		V	$R_L > 2k\Omega$
<b><math>\mu A741</math></b>					
Input Offset Voltage		1.0	5.0	mV	$R_S < 10k\Omega$
Input Offset Current		10	200	nA	
Input Bias Current		80	500	nA	
Input Resistance	0.3	2.0		M $\Omega$	
Input Capacitance		1.4		pF	
Offset Voltage Adjustment Range		$\pm 15$		mV	
Large-Signal Voltage Gain	50,000	200,000			$R_L > 2k\Omega$ , $V_{out} = \pm 10V$
Output Resistance		75		$\Omega$	
Output Short Circuit Current		25		mA	
Supply Current		1.4	2.8	mA	
Power Consumption		50	85	mW	
Transient Response (unity gain)					$V_{in} = 20mV$ , $R_L = 2k\Omega$ , $C_L < 100pF$
Risetime		0.3		$\mu s$	
Overshoot		5.0		%	
Slew Rate		0.5		V/ $\mu s$	$R_L > 2k\Omega$
The following specifications apply for $-55^\circ C < T_A < +125^\circ C$					
Input Offset Voltage		1.0	6.0	mV	$R_S < 10k\Omega$
Input Offset Current		7.0	200	nA	$T_A = +125^\circ C$
		20	500	nA	$T_A = -55^\circ C$
Input Bias Current		0.03	0.5	$\mu A$	$T_A = +125^\circ C$
		0.3	1.5	$\mu A$	$T_A = -55^\circ C$
Input Voltage Range	$\pm 12$	$\pm 13$		V	
Common Mode Rejection Ratio	70	90		dB	$R_S < 10k\Omega$
Supply Voltage Rejection Ratio		10	150	$\mu V/V$	$R_S < 10k\Omega$
Large-Signal Voltage Gain	25,000				$R_L > 2k\Omega$ , $V_{out} = \pm 10V$
Output Voltage Swing	$\pm 12$ $\pm 10$	$\pm 14$ $\pm 13$		V	$R_L > 10k\Omega$ $R_L > 2k\Omega$
Supply Current		1.5	2.5	mA	$T_A = +125^\circ C$
		2.0	3.3	mA	$T_A = -55^\circ C$
Power Consumption		45	75	mW	$T_A = +125^\circ C$
		45	100	mW	$T_A = -55^\circ C$

D COMPONENT DESCRIPTIONS  
 D.6 INTEGRATED CIRCUITS

741 cont'd

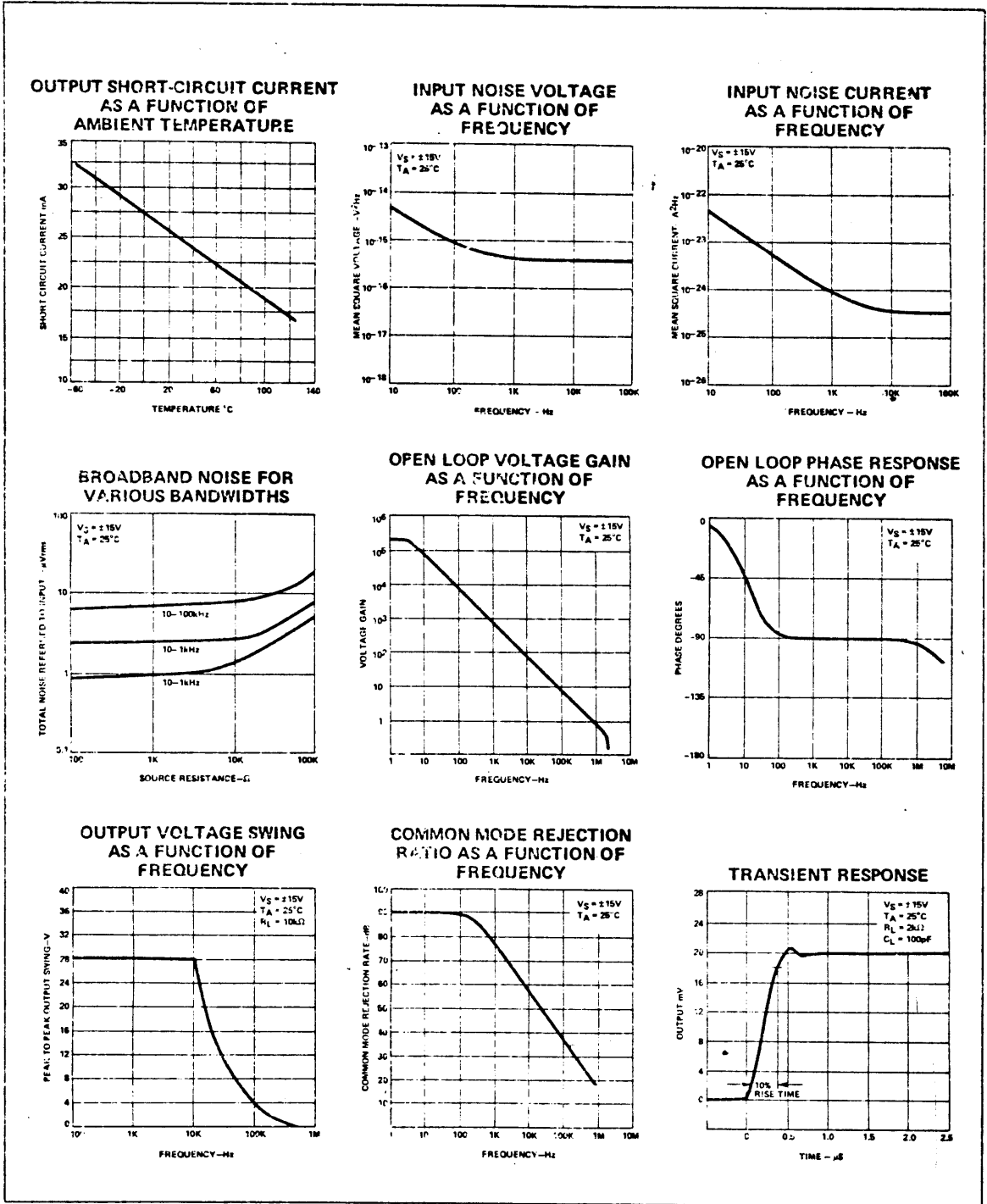
TYPICAL CHARACTERISTIC CURVES



D COMPONENT DESCRIPTIONS  
 D.6 INTEGRATED CIRCUITS

741 cont'd

TYPICAL CHARACTERISTIC CURVES (Cont'd.)





D. COMPONENT DESCRIPTIONS  
 D.6 INTEGRATED CIRCUITS

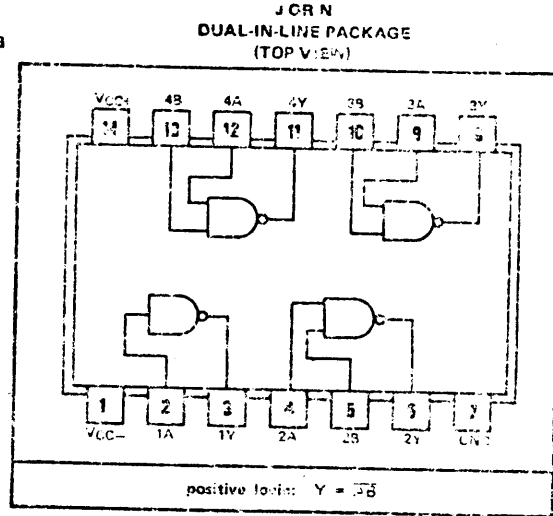
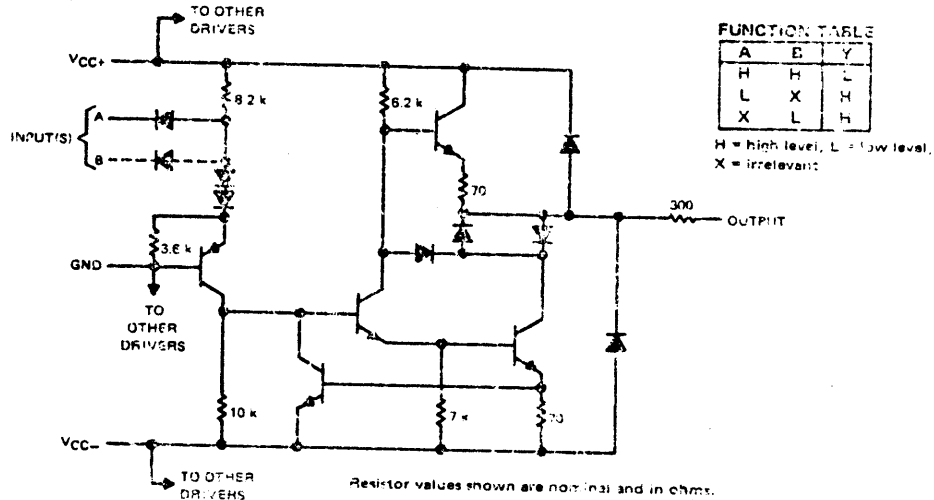
1488 (or 75188)

- Meets Specifications of EIA RS-232C
- Designed to be Interchangeable with Motorola MC1488L
- Current-Limited Output . . . 10 mA Typical
- Power-Off Output Impedance . . . 300  $\Omega$  Min
- Slew Rate Control by Load Capacitor
- Flexible Supply Voltage Range
- Input Compatible with Most TTL and DTL Circuits

**description**

The SN75183 is a monolithic quadruple line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard RS-232C. The device is characterized for operation from 0°C to 75°C.

**schematic (each driver)**



**absolute maximum ratings over operating free-air temperature (unless otherwise noted)**

Supply voltage VCC+ at (or below) 25°C free-air temperature (see Notes 1 and 2)	15 V
Supply voltage VCC- at (or below) 25°C free-air temperature (see Notes 1 and 2)	-15 V
Input voltage range	-15 V to 7 V
Output voltage range	-15 V to 15 V
Continuous total dissipation at (or below) 54°C free-air temperature (see Note 3)	1 W
Operating free-air temperature range	0°C to 75°C
Storage temperature range	-65°C to 175°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: D package	250°C

- NOTES: 1. All voltage values are with respect to the network ground terminal.  
 2. For operation above 25°C free-air temperature, refer to the Maximum Supply Voltage Curve, Figure 6.  
 3. Derate linearly to 730 mW at 75°C free-air temperature at the rate of 10.4 mW/°C.

D COMPONENT DESCRIPTIONS  
 D.6 INTEGRATED CIRCUITS

1488 cont'd

electrical characteristics over operating free-air temperature range,  $V_{CC+} = 9\text{ V}$ ,  $V_{CC-} = -9\text{ V}$   
 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>†</sup>	MAX	UNIT
$V_{IH}$	High-level input voltage			1.9			V
$V_{IL}$	Low-level input voltage					0.8	V
$V_{OH}$	High-level output voltage	$V_{IL} = 0.8\text{ V}$ , $R_L = 3\text{ k}\Omega$	$V_{CC+} = 9\text{ V}$ , $V_{CC-} = -9\text{ V}$	6	7		V
			$V_{CC+} = 13.2\text{ V}$ , $V_{CC-} = -13.2\text{ V}$	9	10.5		
$V_{OL}$	Low-level output voltage	$V_{IH} = 1.9\text{ V}$ , $R_L = 3\text{ k}\Omega$	$V_{CC+} = 9\text{ V}$ , $V_{CC-} = -9\text{ V}$		-7	-6	V
			$V_{CC+} = 13.2\text{ V}$ , $V_{CC-} = -13.2\text{ V}$		-10.5	-9	
$I_{IH}$	High-level input current	$V_I = 5\text{ V}$				10	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_I = 0$				-1 -1.6	mA
$I_{OS(H)}$	Short-circuit output current at high level	$V_I = 0.8\text{ V}$ , $V_O = 0$		-6	-10	-12	mA
$I_{OS(L)}$	Short-circuit output current at low level	$V_I = 1.9\text{ V}$ , $V_O = 0$		6	10	12	mA
$r_o$	Output resistance, power off	$V_{CC+} = 0$ , $V_{CC-} = 0$ , $V_O = -2\text{ V to } 2\text{ V}$		300			$\Omega$
$I_{CC+}$	Supply current from $V_{CC+}$	No load	$V_{CC+} = 9\text{ V}$ , All inputs at 1.9 V		15	20	mA
			$V_{CC+} = 12\text{ V}$ , All inputs at 0.8 V		4.5	6	
		No load	$V_{CC+} = 9\text{ V}$ , All inputs at 1.9 V		19	25	
			$V_{CC+} = 12\text{ V}$ , All inputs at 0.8 V		5.5	7	
$I_{CC-}$	Supply current from $V_{CC-}$	No load	$V_{CC-} = -9\text{ V}$ , All inputs at 1.9 V		-13	-17	mA
			$V_{CC-} = -12\text{ V}$ , All inputs at 0.8 V		-0.015		
		No load	$V_{CC-} = -9\text{ V}$ , All inputs at 1.9 V		-16	-23	
			$V_{CC-} = -12\text{ V}$ , All inputs at 0.8 V		-0.015		
$P_D$	Total power dissipation	No load	$V_{CC+} = 9\text{ V}$ , $V_{CC-} = -9\text{ V}$			333	mW
			$V_{CC+} = 12\text{ V}$ , $V_{CC-} = -12\text{ V}$			576	

<sup>†</sup>All typical values are at  $T_A = 25^\circ\text{C}$ .

NOTE 4: The algebraic convention where the most positive (least negative) limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if -6 V is a maximum, the typical value is a more-negative voltage.

switching characteristics,  $V_{CC+} = 9\text{ V}$ ,  $V_{CC-} = -9\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PH}$	Propagation delay time, low-to-high-level output		220	375	ns
$t_{PL}$	Propagation delay time, high-to-low-level output		100	175	ns
$t_{TLH}$	Transition time, low-to-high-level output <sup>‡</sup>	See Figure 1	55	100	ns
$t_{THL}$	Transition time, high-to-low-level output <sup>‡</sup>		45	75	ns
$t_{PLH}$	Transition time, low-to-high-level output <sup>§</sup>	See Figure 1	2.5		$\mu\text{s}$
$t_{PHL}$	Transition time, high-to-low-level output <sup>§</sup>		3.0		$\mu\text{s}$

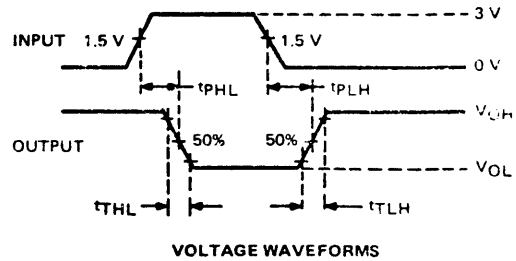
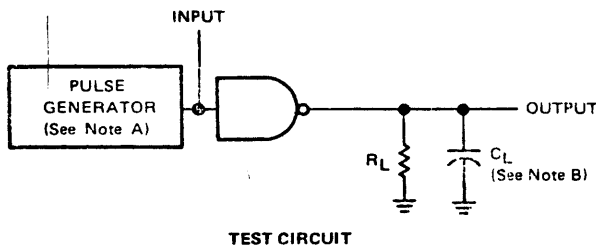
<sup>‡</sup>Measured between 10% and 90% points of output waveform.

<sup>§</sup>Measured between +3 V and -3 V points of output waveform (EIA RS-232C conditions)

D COMPONENT DESCRIPTIONS  
 D.6 INTEGRATED CIRCUITS

1488 cont'd

PARAMETER MEASUREMENT INFORMATION



NOTE: A. The pulse generator has the following characteristics:  $t_w = 0.5 \mu s$ , PRR = 1 MHz,  $Z_0 = 50 \Omega$ .  
 B.  $C_L$  includes probe and jig capacitance.

FIGURE 1—PROPAGATION AND TRANSITION TIMES

TYPICAL CHARACTERISTICS

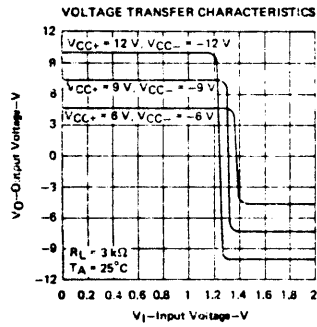


FIGURE 2

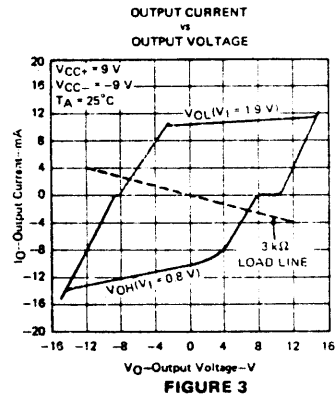


FIGURE 3

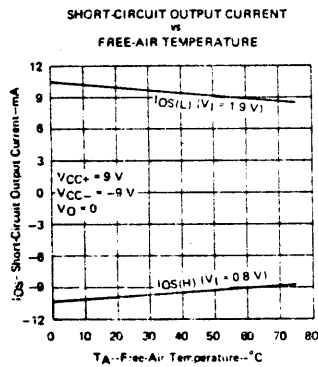


FIGURE 4

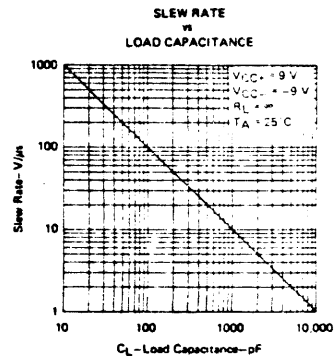
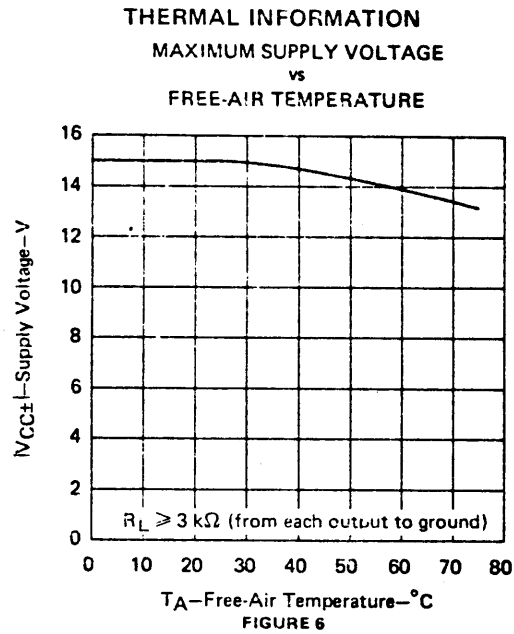


FIGURE 5

D COMPONENT DESCRIPTIONS  
 D.6 INTEGRATED CIRCUITS

1488 cont'd



**TYPICAL APPLICATION DATA**

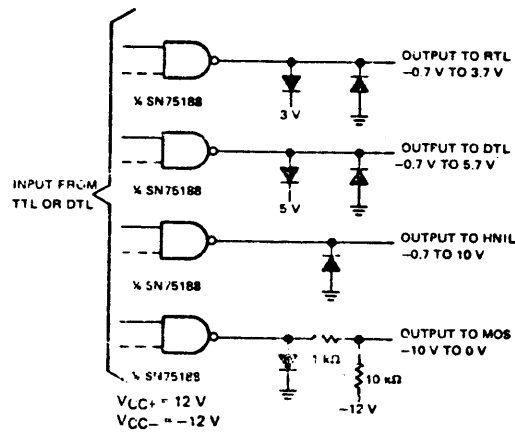


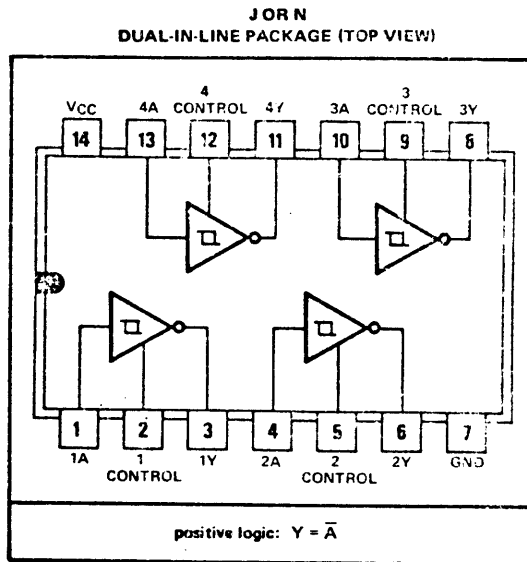
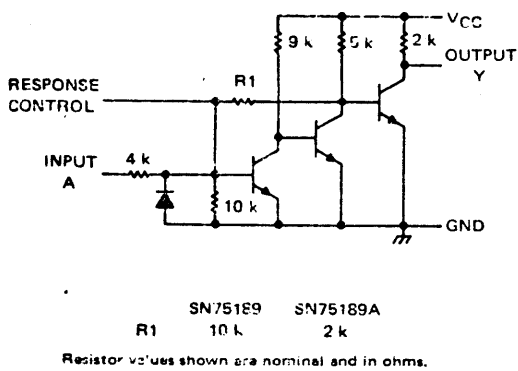
FIGURE 7—LOGIC TRANSLATOR APPLICATIONS

D COMPONENT DESCRIPTION  
 D.6 INTEGRATED CIRCUITS

1489 (or 75189)

- Input Resistance . . . 3 kΩ to 7 kΩ
- Input Signal Range . . . ±30 V
- Fully Interchangeable with Motorola MC1489, MC1489A
- Operates From Single 5-V Supply
- Built-in Input Hysteresis (Double Thresholds)
- Response Control Provides:  
 Input Threshold Shifting  
 Input Noise Filtering
- Satisfies Requirements of EIA RS-232-C

schematic (each receiver)



description

The SN75189 and SN75189A are monolithic quadruple line receivers designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232C. A separate response control terminal is provided for each receiver. A resistor or a resistor and bias voltage can be connected between this terminal and ground to shift the input threshold voltage levels. An external capacitor can be connected from this terminal to ground to provide input noise filtering.

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Supply voltage, VCC (see Note 1)	10 V
Input voltage	±30 V
Output current	20 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1 W
Operating free-air temperature range	0°C to 75°C
Storage temperature range	-65°C to 175°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

- NOTES: 1. Voltage values are with respect to the network ground terminal.  
 2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curve, Figure 12.

D COMPONENT DESCRIPTIONS  
D.6 INTEGRATED CIRCUITS

1489 cont'd

electrical characteristics over operating free-air temperature range,  $V_{CC} = 5V \pm 1\%$ , (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SN75189			SN75189A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{T+}$ Positive-going threshold voltage	1		1		1.5	1.75	1.9	2.25	V
$V_{T-}$ Negative-going threshold voltage	1		0.75		1.25	0.75	0.97	1.25	V
$V_{OH}$ High-level output voltage	1	$V_I = 0.75V$ , $I_{OH} = -0.5mA$	2.6	4	5	2.6	4	5	V
		Input open, $I_{OH} = -0.5mA$	2.6	4	5	2.6	4	5	
$V_{OL}$ Low-level output voltage	1	$V_I = 3V$ , $I_{OL} = 10mA$		0.2	0.45		0.2	0.45	V
$I_{IH}$ High-level input current	2	$V_I = 25V$		3.6	8.3		3.6	8.3	mA
		$V_I = 3V$		0.43			0.43		
$I_{IL}$ Low-level input current	2	$V_I = -25V$		-3.6	-8.3		-3.6	-8.3	mA
		$V_I = -3V$		-0.43			-0.43		
$I_{OS}$ Short-circuit output current	3			-3		-3		mA	
$I_{CC}$ Supply current	2	$V_I = 5V$ , Outputs open		20	26		20	26	mA

† All characteristics are measured with the response control terminal open.

‡ All typical values are at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ .

switching characteristics,  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$t_{PLH}$ Propagation delay time, low-to-high-level output	4	$C_L = 15pF$ , $R_L = 3.9k\Omega$		25	85	ns
$t_{PHL}$ Propagation delay time, high-to-low-level output		$C_L = 15pF$ , $R_L = 390\Omega$		25	50	
$t_{TLH}$ Transition time, low-to-high-level output		$C_L = 15pF$ , $R_L = 3.9k\Omega$		120	175	ns
$t_{THL}$ Transition time, high-to-low-level output		$C_L = 15pF$ , $R_L = 390\Omega$		10	20	

PARAMETER MEASUREMENT INFORMATION§

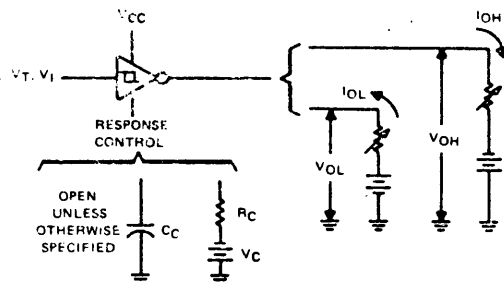


FIGURE 1— $V_{T+}$ ,  $V_{T-}$ ,  $V_{OH}$ ,  $V_{OL}$

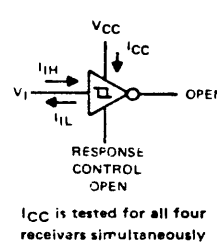


FIGURE 2— $I_{IH}$ ,  $I_{IL}$ ,  $I_{CC}$

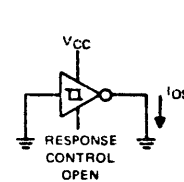
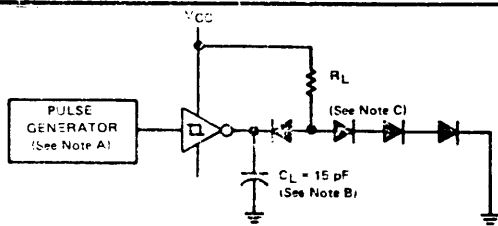
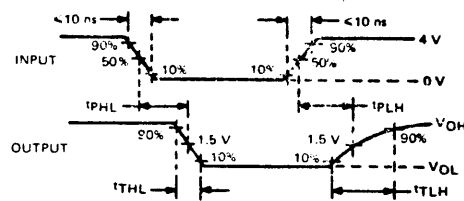


FIGURE 3— $I_{OS}$



TEST CIRCUIT

- NOTES: A. The pulse generator has the following characteristics:  $Z_{OUT} \approx 50\Omega$ ,  $t_w = 500ns$ .  
B.  $C_L$  includes probe and jig capacitance.  
C. All diodes are 1N305A or equivalent.



VOLTAGE WAVEFORMS

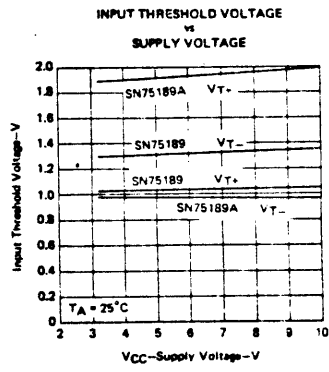
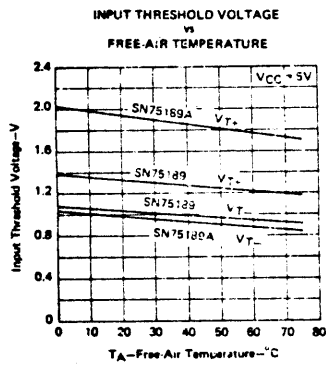
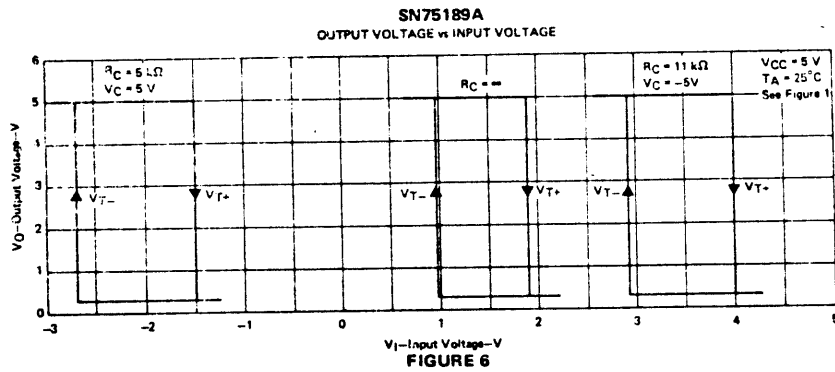
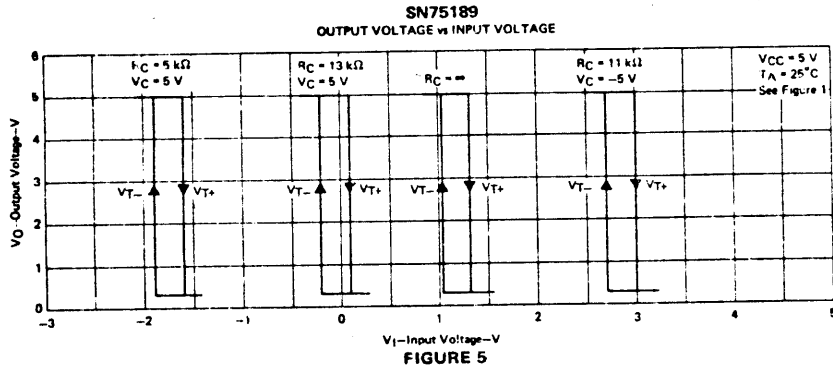
FIGURE 4—SWITCHING TIMES

§ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

D COMPONENT DESCRIPTIONS  
 D.6 INTEGRATED CIRCUITS

1489 cont'd

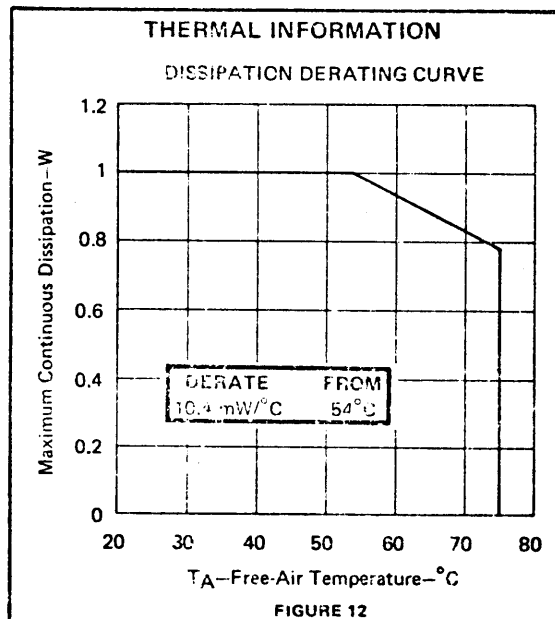
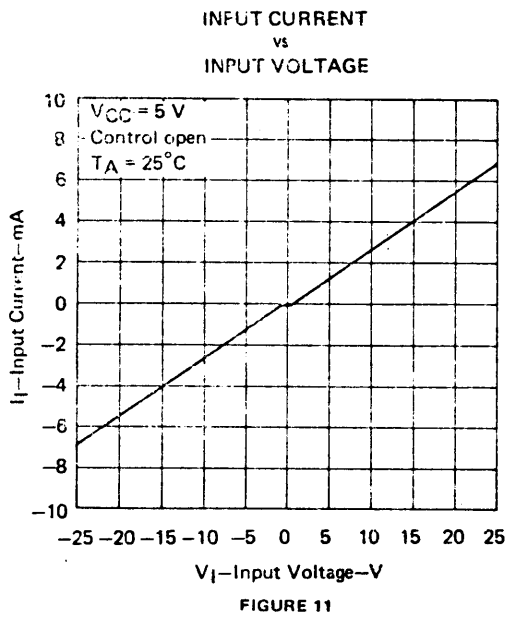
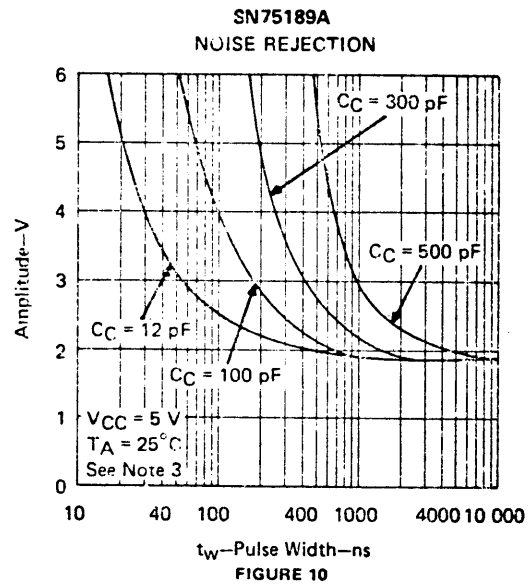
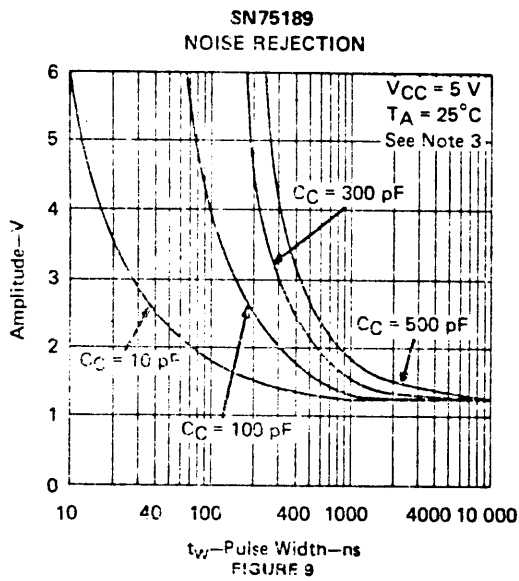
TYPICAL CHARACTERISTICS



D COMPONENT DESCRIPTIONS  
 D.6 INTEGRATED CIRCUITS

1489 cont'd

TYPICAL CHARACTERISTICS



NOTE 3: This figure shows the maximum amplitude of a positive-going pulse that, starting from zero volts, will not cause a change of the output level.



4001

**general description**

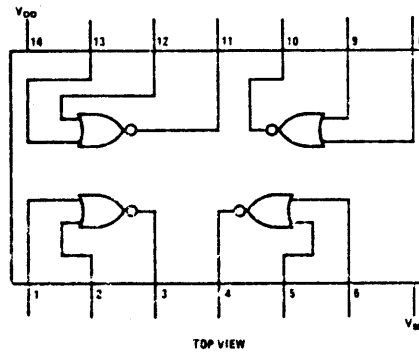
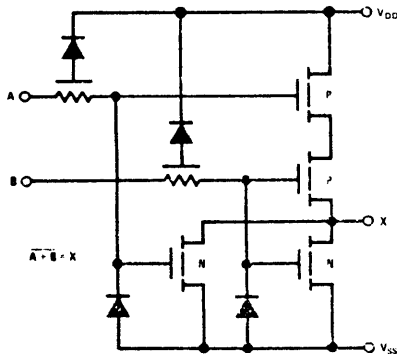
The CD4001M/CD4001C is a monolithic complementary MOS (CMOS) quadruple two-input NOR gate integrated circuit. N and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No dc power other than that caused by leakage current is consumed during static conditions.

All inputs are protected against static discharge and latching conditions.

**features**

- Wide supply voltage range 3V to 15V
- Low power 10 nW (typ)
- High noise immunity 0.45 V<sub>DD</sub> (typ)

**schematic and connection diagrams**



**absolute maximum ratings**

Voltage at Any Pin (Note 1)	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Operating Temperature Range	
CD4001M	-55°C to +125°C
CD4001C	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Package Dissipation	500 mW
Operating V <sub>DD</sub> Range	$V_{SS} + 3.0V$ to $V_{SS} + 15V$
Lead Temperature (Soldering, 10 seconds)	300°C

**dc electrical characteristics CD4001M**

PARAMETER	CONDITIONS	LIMITS									UNITS
		-55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I <sub>Q</sub> )	V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V			0.05 0.1		0.001 0.001	0.05 0.1			3 6	μA
Quiescent Device Dissipation (Package) (P <sub>Q</sub> )	V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V			0.25 1		0.005 0.01	0.25 1			15 60	μW
Output Voltage Low Level (V <sub>OL</sub> )	V <sub>DD</sub> = 5V, V <sub>I</sub> = V <sub>DD</sub> , I <sub>O</sub> = 0A V <sub>DD</sub> = 10V, V <sub>I</sub> = V <sub>DD</sub> , I <sub>O</sub> = 0A			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V
Output Voltage High Level (V <sub>OH</sub> )	V <sub>DD</sub> = 5V, V <sub>I</sub> = V <sub>SS</sub> , I <sub>O</sub> = 0A V <sub>DD</sub> = 10V, V <sub>I</sub> = V <sub>SS</sub> , I <sub>O</sub> = 0A	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V
Noise Immunity (V <sub>NI</sub> ) (All Inputs)	V <sub>DD</sub> = 5V, V <sub>O</sub> = 3.5V, I <sub>O</sub> = 0A V <sub>DD</sub> = 10V, V <sub>O</sub> = 7.2V, I <sub>O</sub> = 0A	1.5 3			1.5 3	2.25 4.5		1.4 2.9			V
Noise Immunity (V <sub>NI</sub> ) (All Inputs)	V <sub>DD</sub> = 5V, V <sub>O</sub> = 0.95V, I <sub>O</sub> = 0A V <sub>DD</sub> = 10V, V <sub>O</sub> = 2.9V, I <sub>O</sub> = 0A	1.4 2.9			1.5 3	2.25 4.5		1.5 3			V
Output Drive Current N-Channel (I <sub>ON</sub> )	V <sub>DD</sub> = 5V, V <sub>O</sub> = 0.4V, V <sub>I</sub> = V <sub>DD</sub> V <sub>DD</sub> = 10V, V <sub>O</sub> = 0.5V, V <sub>I</sub> = V <sub>DD</sub>	0.5 1.1			0.40 0.9	1 2.5		0.28 0.65			mA
Output Drive Current P-Channel (I <sub>OP</sub> )	V <sub>DD</sub> = 5V, V <sub>O</sub> = 2.5V, V <sub>I</sub> = V <sub>SS</sub> V <sub>DD</sub> = 10V, V <sub>O</sub> = 9.5V, V <sub>I</sub> = V <sub>SS</sub>	-0.62 -0.62			-0.5 -0.5	-2 -1		-0.35 -0.35			mA
Input Current (I <sub>I</sub> )						10					pA

D COMPONENT DESCRIPTIONS  
D.6 INTEGRATED CIRCUITS

4001 cont'd

dc electrical characteristics CD4001C

PARAMETER	CONDITIONS	LIMITS									UNITS
		-40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current ( $I_Q$ )	$V_{DD} = 5V$ $V_{DD} = 10V$			0.5 5		0.005 0.005	0.5 5			15 30	$\mu A$ $\mu A$
Quiescent Device Dissipation/Package ( $P_D$ )	$V_{DD} = 5V$ $V_{DD} = 10V$			2.5 50		0.025 0.05	2.5 50			75 300	$\mu W$ $\mu W$
Output Voltage Low Level ( $V_{OL}$ )	$V_{DD} = 5V, V_i = V_{DD}, I_O = 0A$ $V_{DD} = 10V, V_i = V_{DD}, I_O = 0A$			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V
Output Voltage High Level ( $V_{OH}$ )	$V_{DD} = 5V, V_i = V_{SS}, I_O = 0A$ $V_{DD} = 10V, V_i = V_{SS}, I_O = 0A$	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V
Noise Immunity ( $V_{NI}$ ) (All Inputs)	$V_{DD} = 5V, V_O = 3.6V, I_O = 0A$ $V_{DD} = 10V, V_O = 7.2V, I_O = 0A$	1.5 3			1.5 3	2.25 4.5		1.4 2.9			V V
Noise Immunity ( $V_{NI}$ ) (All Inputs)	$V_{DD} = 5V, V_O = 0.95V, I_O = 0A$ $V_{DD} = 10V, V_O = 2.9V, I_O = 0A$	1.4 2.9			1.5 3	2.25 4.5		1.5 3			V V
Output Drive Current N-Channel ( $I_{ON}$ )	$V_{DD} = 5V, V_O = 0.4V, V_i = V_{DD}$ $V_{DD} = 10V, V_O = 0.5V, V_i = V_{DD}$	0.35 0.72			0.3 0.6	1 2.5		0.24 0.48			mA mA
Output Drive Current P-Channel ( $I_{OP}$ )	$V_{DD} = 5V, V_O = 2.5V, V_i = V_{SS}$ $V_{DD} = 10V, V_O = 9.5V, V_i = V_{SS}$	-0.35 -0.3			-0.3 -0.25	-2 -1		-0.24 -0.2			mA mA
Input Current ( $I_i$ )						10					pA

Note 1: This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

ac electrical characteristics CD4001M

$T_A = 25^\circ C$  and  $C_L = 15$  pF and input rise and fall times = 20 ns. Typical temperature coefficient for all values of  $V_{DD} = 0.3\%/^\circ C$ .

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time High to Low Level ( $t_{PHL}$ )	$V_{DD} = 5V$		35	65	ns
	$V_{DD} = 10V$		25	40	ns
Propagation Delay Time Low to High Level ( $t_{PLH}$ )	$V_{DD} = 5V$		35	65	ns
	$V_{DD} = 10V$		25	40	ns
Transition Time High to Low Level ( $t_{THL}$ )	$V_{DD} = 5V$		65	125	ns
	$V_{DD} = 10V$		35	70	ns
Transition Time Low to High Level ( $t_{TLH}$ )	$V_{DD} = 5V$		65	175	ns
	$V_{DD} = 10V$		35	75	ns
Input Capacitance ( $C_i$ )	Any Input		5		pF

ac electrical characteristics CD4001C

$T_A = 25^\circ C$  and  $C_L = 15$  pF and input rise and fall times = 20 ns. Typical temperature coefficient for all values of  $V_{DD} = 0.3\%/^\circ C$ .

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time High to Low Level ( $t_{PHL}$ )	$V_{DD} = 5V$		35	80	ns
	$V_{DD} = 10V$		25	55	ns
Propagation Delay Time Low to High Level ( $t_{PLH}$ )	$V_{DD} = 5V$		35	120	ns
	$V_{DD} = 10V$		25	65	ns
Transition Time High to Low Level ( $t_{THL}$ )	$V_{DD} = 5V$		65	200	ns
	$V_{DD} = 10V$		35	115	ns
Transition Time Low to High Level ( $t_{TLH}$ )	$V_{DD} = 5V$		65	300	ns
	$V_{DD} = 10V$		35	125	ns
Input Capacitance ( $C_i$ )	Any Input		5		pF

4013

**general description**

The CD4013M/CD4013C dual D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P channel enhancement transistors. Each flip flop has independent data, set, reset, and clock inputs and "Q" and "Q̄" outputs. These devices can be used for shift register applications, and, by connecting "Q" output to the data input, for counter and toggle applications. The logic level present at the "D" input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line respectively.

**features**

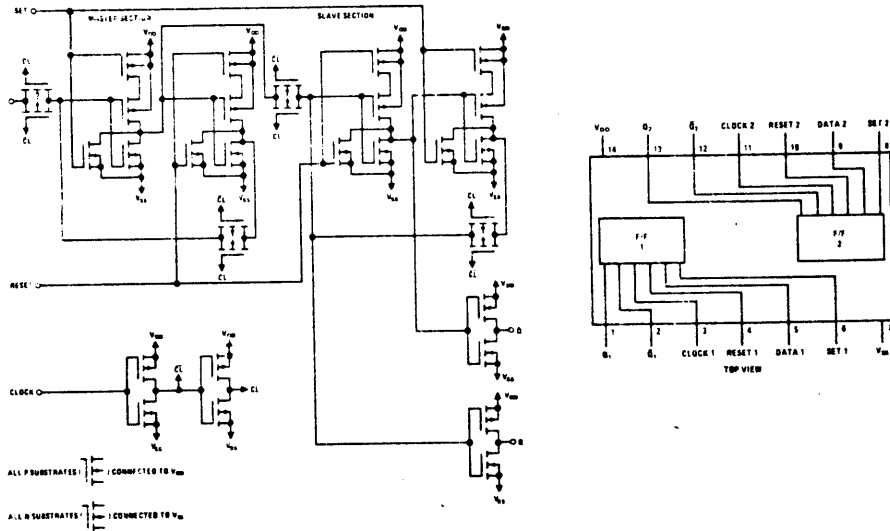
- Supply voltage range                    3V to 15V

- Noise immunity                            0.45 V<sub>DD</sub> (typ)
- Low power                                    50 nW (typ)
- Medium speed operation                10 MHz (typ) with  
    10 volt supply

**applications**

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial electronics
- Remote metering
- Computers

**schematic and connection diagrams**



**absolute maximum ratings**

Voltage at Any Pin (Note 1)	V <sub>SS</sub> - 0.3V to V <sub>SS</sub> + 15.5V
Operating Temperature Range	
CD4013M	-55°C to +125°C
CD4013C	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 sec)	300°C
Operating V <sub>DD</sub> Range	V <sub>SS</sub> + 3V to V <sub>SS</sub> + 15V

D COMPONENT DESCRIPTIONS  
 D.6 INTEGRATED CIRCUITS

4013 cont'd

dc electrical characteristics

CHARACTERISTIC	TEST CONDITIONS		LIMITS															UNITS		
			CD4013M						CD4013C						85 C					
			55 C			25 C			25 C			40 C			25 C					
			V <sub>CC</sub> VOLTS	V <sub>DD</sub> VOLTS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	A-V		TYP	MAX
Quiescent Device Current (I <sub>CC</sub> )		5				0.005	1	30									140	μA		
Quiescent Device Dissipation (Package) (P <sub>D</sub> )		5				0.005	2	120									280	mW		
Output Voltage	V <sub>OH</sub> = 5	5				0.05	20	1700									0.05	V		
Low Level (V <sub>OL</sub> )	V <sub>OH</sub> = 10	10				0.01	0	0.05									0.05	V		
High Level (V <sub>OH</sub> )	V <sub>OH</sub> = 0	5	4.99			4.99	5	4.95				4.99					4.95	V		
High Level (V <sub>OH</sub> )	V <sub>OH</sub> = 0	10	9.99			9.99	10	9.95				9.99					9.95	V		
Noise Immunity (All Inputs) (V <sub>NI</sub> )	V <sub>OH</sub> > 3.5	5	1.5			1.4	2.25	1.4				1.5					2.25	V		
(V <sub>NI</sub> )	V <sub>OH</sub> > 10	10	3			3	4.5	2.9				3					4.5	V		
(V <sub>NI</sub> )	V <sub>OH</sub> = 15	5	1.4			1.5	2.25	1.5				1.4					2.25	V		
(V <sub>NI</sub> )	V <sub>OH</sub> = 3.0	10	2.9			3	4.5	3				2.9					4.5	V		
Output Drive Current	V <sub>OH</sub> = 0.5	5	0.65			0.5	1	0.35				0.65					0.3	1	mA	
N-Channel (I <sub>ON</sub> )	V <sub>OH</sub> = 0.5	10	1.25			1.0	2.5	0.75				1.25					0.6	2.5	mA	
P-Channel (I <sub>OP</sub> )	V <sub>OH</sub> = 4.5	5	-0.31			-0.25	0.5	-0.175				-0.31					-0.14	-0.5	-0.095	mA
Input Current (I <sub>I</sub> )	V <sub>CC</sub> = 9.5	10	-0.8			-0.65	-1.3	-0.45				-0.8					-0.33	-1.3	0.27	μA

Note 1: Devices should not be connected with power on.  
 \*Test performed with the following sequence of 1's and 0's.

C <sub>L</sub>	D	S	R
0	1	0	1
0	0	1	1
0	0	1	0
1	0	1	0

ac electrical characteristics at T<sub>A</sub> = 25°C and C<sub>L</sub> = 15 pF  
 Typical Temperature Coefficient for all values of V<sub>DD</sub> = 0.3%/°C

CHARACTERISTICS	TEST CONDITIONS		LIMITS						UNITS
			CD4013M			CD4013C			
			V <sub>DD</sub> (VOLTS)	MIN	TYP	MAX	MIN	TYP	
<b>CLOCKED OPERATION</b>									
Propagation Delay Time (t <sub>PLH</sub> + t <sub>PLL</sub> )		5	-	150	250	-	150	250	ns
Transition Time (t <sub>PLH</sub> + t <sub>PLL</sub> )		10	-	75	110	-	75	125	ns
Minimum Clock Pulse Width (t <sub>CLK</sub> )		5	-	75	125	-	75	150	ns
Maximum Clock Rise & Fall Time (t <sub>CLR</sub> + t <sub>CLF</sub> )		10	-	50	70	-	50	200	ns
Set-Up Time		5	15	-	-	-	15	-	μs
Maximum Clock Frequency (f <sub>CLK</sub> )		10	5	-	-	-	5	-	MHz
Input Capacitance (C <sub>I</sub> )		5	-	20	40	-	20	50	25
		10	-	10	20	-	10	25	
		5	3	4	-	2.5	4	-	
		10	7	10	-	5	10	-	
		10	-	5	-	-	5	-	μF
<b>SET &amp; RESET OPERATION</b>									
Propagation Delay Time (t <sub>PLH</sub> + t <sub>PLL</sub> )		5	-	125	225	-	125	250	ns
Minimum Set and Reset Pulse Width (t <sub>SET</sub> )		10	-	75	110	-	75	125	ns
		5	-	125	175	-	125	200	
		10	-	50	80	-	50	100	

D COMPONENT DESCRIPTIONS  
 D.6 INTEGRATED CIRCUITS

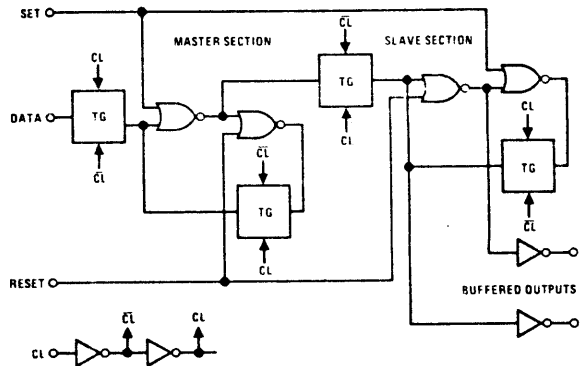
4013 cont'd

truth table

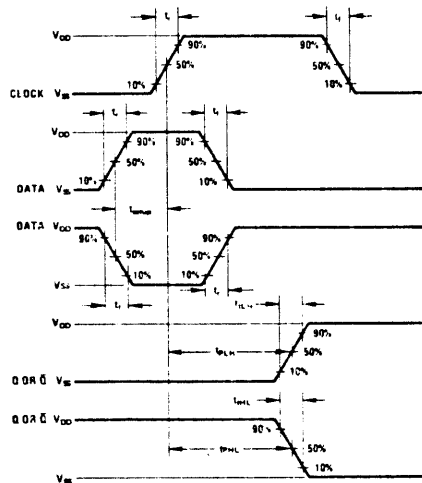
CL†	D	R	S	Q	$\bar{Q}$
	0	0	0	0	1
	1	0	0	1	0
	x	0	0	Q	$\bar{Q}$
x	x	1	0	0	1
x	x	0	1	1	0
x	x	1	1	.	.

No change  
 \* = Invalid condition  
 \*\* = FF1/FF2 terminal assignments  
 † = Level change  
 x = Don't care case

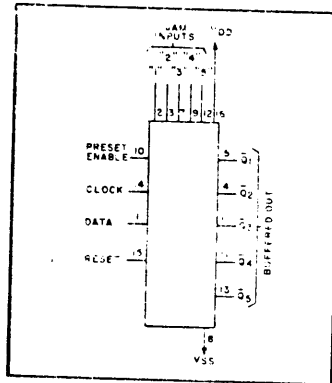
logic diagram



switching time waveforms



4018



## COS/MOS Presettable Divide-By-'N' Counter

### Special Features

- Medium speed operation . . . . . 5 MHz (typ.) at  $V_{DD} - V_{SS} = 10\text{ V}$
- Fully static operation
- MSI complexity on a single chip

### Applications

- Fixed and programmable divide-by-10, 9, 8, 7, 6, 5, 4, 3, 2 counters
- Fixed and programmable counters greater than 10
- Programmable decade counters
- Divide-by-"N" counters/frequency synthesizers
- Frequency division
- Counter control/timers

CD4018A types consist of 5 Johnson-Counter stages, buffered  $\bar{Q}$  outputs from each stage, and counter preset control gating. "Clock", "Reset", "Data", "Preset Enable", and 5 individual "Jam" inputs are provided. Divide by 10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the  $\bar{Q}_5$ ,  $\bar{Q}_4$ ,  $\bar{Q}_3$ ,  $\bar{Q}_2$ ,  $\bar{Q}_1$  signals, respectively, back to the Data input. Divide-by-9, 7, 5, or 3 counter configurations can be implemented by the use of a CD4011A gate package

to properly gate the feedback connection to the Data input. Divide-by functions greater than 10 can be achieved by use of multiple CD4018A units. The counter is advanced one count at the positive clock-signal transition. A "high" Reset signal clears the counter to an "all-zero" condition. A "high" Preset Enable signal allows information on the Jam inputs to preset the counter. Anti-lock gating is provided to assure the proper counting sequence.

For maximum ratings, see page 22.

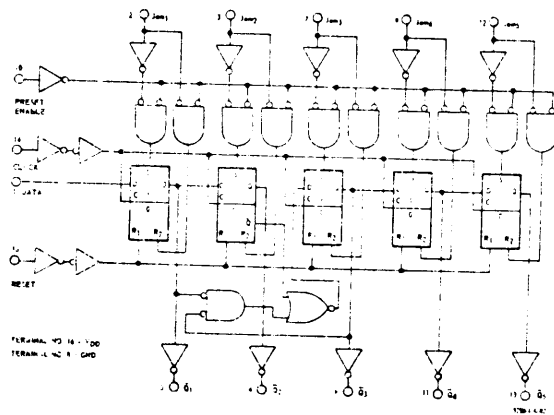


Fig.13.1—Logic diagram.

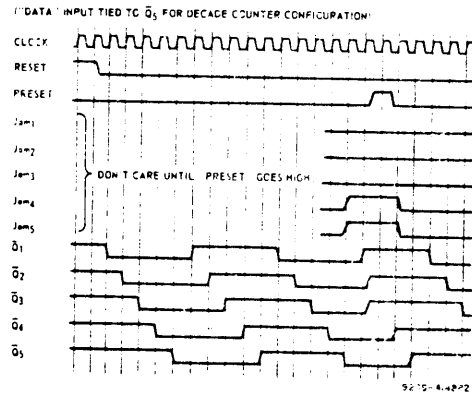


Fig.13.2—Timing diagram.

D COMPONENT DESCRIPTIONS  
D.6 INTEGRATED CIRCUITS

4018 cont'd

STATIC ELECTRICAL CHARACTERISTICS (All inputs  $V_{SS} < V_I \leq V_{DD}$ )  
(Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS										UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig No.		
			CD4018AD, CD4018AK, CD4018AF													
			$V_O$ Volts	$V_{DD}$ Volts	-55°C			25°C			125°C					
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max						
Quiescent Device Current	$I_L$		5	5	-	-	5	-	0.2	5	-	-	300	$\mu A$	13.9	
			10	10	-	-	10	-	0.5	10	-	-	500			
Quiescent Device Dissipation/Package	PD		5	-	-	-	25	-	1.5	25	-	-	1500	$\mu W$	-	
			10	-	-	-	100	-	5	100	-	-	6000			
Output Voltage Low Level	$V_{OL}$		5	-	-	-	0.01	-	0	0.01	-	-	0.05	V	-	
			10	-	-	-	0.01	-	0	0.01	-	-	0.05			
High Level	$V_{OH}$		5	4.99	-	-	4.99	5	-	4.95	-	-	-	V	-	
			10	9.99	-	-	9.99	10	-	9.95	-	-	-			
Noise Immunity (Any Input) For Definition See Appendix	$V_{NI}$		0.8	5	1.5	-	-	1.5	2.25	-	1.4	-	-	V	13.10	
			1.0	10	3	-	-	3	4.5	-	2.9	-	-			
	$V_{NH}$		4.2	5	1.4	-	-	1.5	2.25	-	1.5	-	-	V	-	
			9.0	10	2.9	-	-	3	4.5	-	3	-	-			
Output Drive Current N Channel	$I_{DN}$	$\bar{Q}_5$	0.5	5	0.18	-	-	0.15	0.4	-	0.105	-	-	mA	♦	
			0.5	10	0.45	-	-	0.35	1	-	0.25	-	-			
			$\bar{Q}_1, \bar{Q}_2$	0.5	5	0.06	-	-	0.05	0.1	-	0.035	-			-
			$\bar{Q}_3, \bar{Q}_4$	0.5	10	0.25	-	-	0.2	0.4	-	0.14	-			-
Output Drive Current P Channel	$I_{DP}$	$\bar{Q}_5$	4.5	5	-0.185	-	-	-0.15	-0.4	-	-0.105	-	-	mA	♦	
			4.5	10	-0.45	-	-	-0.35	-1	-	-0.25	-	-			
			$\bar{Q}_1, \bar{Q}_2$	4.5	5	-0.075	-	-	-0.06	-0.15	-	-0.04	-			-
			$\bar{Q}_3, \bar{Q}_4$	4.5	10	-0.25	-	-	-0.2	-0.4	-	-0.14	-			-
Input Current	$I_I$												$\mu A$	-		

♦ See Appendix.

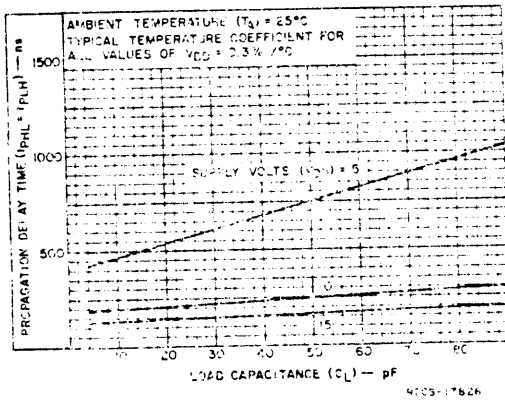


Fig. 13.3—Typ. propagation delay time vs  $C_L$  for decoded outputs.

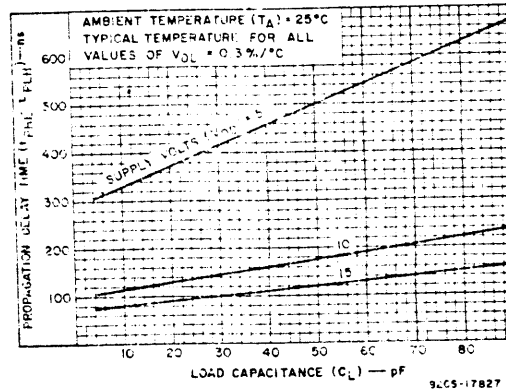


Fig. 13.4—Typ. propagation delay time vs  $C_L$  for  $\bar{Q}_5$  output.

D COMPONENT DESCRIPTIONS  
D.6 INTEGRATED CIRCUITS

4018 cont'd

STATIC ELECTRICAL CHARACTERISTICS (All inputs  $V_{SS} \leq V_i \leq V_{DD}$ )  
(Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS									UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	
			CD4018AE											
			$V_i$ Volts	$V_{DD}$ Volts	-40°C			25°C			85°C			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max				
Quiescent Device Current	$I_Q$		5	-	-	50	-	0.5	50	-	-	700	$\mu A$	13.9
			10	-	-	100	-	1	100	-	-	1400		
Quiescent Device Dissipation/Package	$P_D$		5	-	-	250	-	2.5	250	-	-	3500	$\mu W$	-
			10	-	-	1000	-	10	1000	-	-	14000		
Output Voltage Low Level	$V_{OL}$		5	-	-	0.01	-	0	0.01	-	-	0.05	V	-
			10	-	-	0.01	-	0	0.01	-	-	0.05		
Output Voltage High Level	$V_{OH}$		5	4.99	-	-	4.95	5	-	4.95	-	-	V	-
			10	9.99	-	-	9.95	10	-	9.95	-	-		
Noise Immunity (Any Input) For Definition, See Appendix	$V_{NI}$		0.3	5	1.5	-	-	1.5	2.25	-	1.4	-	V	13.10
			1.0	10	3	-	-	3	4.5	-	2.9	-		
	$V_{NH}$		4.2	5	1.4	-	-	1.5	2.25	-	1.5	-	V	-
			9.0	10	2.0	-	-	3	4.5	-	3	-		
Output Drive Current N Channel	$I_{ON}$	$\bar{Q}_5$	0.5	5	0.095	-	-	0.08	0.4	-	0.065	-	mA	♦
			0.5	10	0.3	-	-	0.25	1	-	0.2	-		
		$\bar{Q}_1, \bar{Q}_2, \bar{Q}_3, \bar{Q}_4$	0.5	5	0.03	-	-	0.025	0.1	-	0.02	-		
			0.5	10	0.18	-	-	0.15	0.4	-	0.12	-		
Output Drive Current P Channel	$I_{OP}$	$\bar{Q}_5$	4.5	5	-0.095	-	-	-0.08	-0.4	-	-0.065	-	mA	♦
			4.5	10	-0.3	-	-	-0.25	-1	-	-0.2	-		
		$\bar{Q}_1, \bar{Q}_2, \bar{Q}_3, \bar{Q}_4$	4.5	5	-0.035	-	-	-0.03	-0.15	-	-0.024	-		
			4.5	10	-0.18	-	-	-0.15	-0.4	-	-0.12	-		
Input Current	$I_i$			-	-	-	-	10	-	-	-	pA	-	

♦ See Appendix

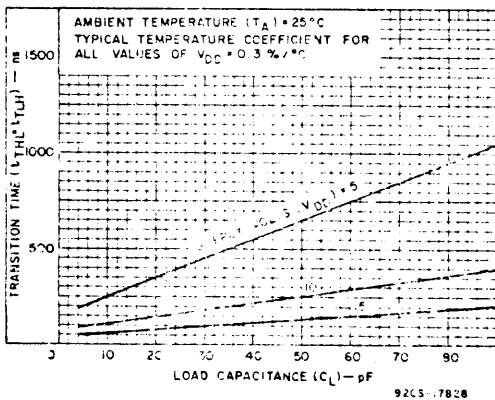


Fig. 13.5—Typ. transition time vs.  $C_L$  for decoded outputs

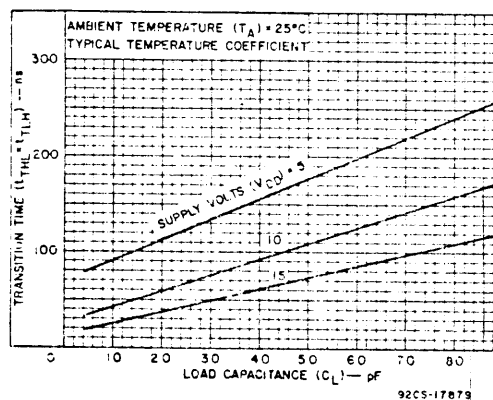


Fig. 13.6—Typ. transition time vs.  $C_L$  for  $\bar{Q}_5$  output



D COMPONENT DESCRIPTIONS  
 D.6 INTEGRATED CIRCUITS

4018 cont'd.

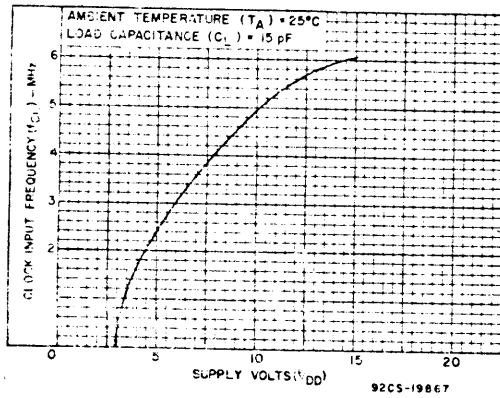


Fig. 13.7—Typical clock frequency vs.  $V_{DD}$ .

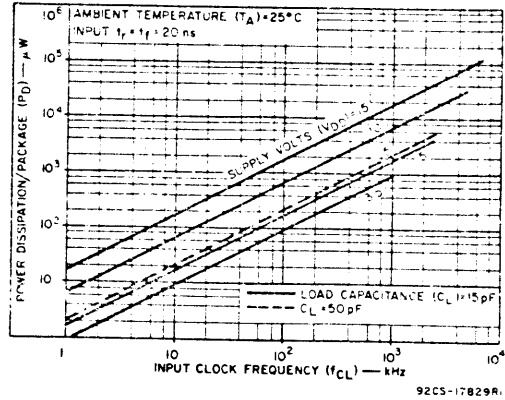


Fig. 13.8—Typ. dissipation characteristics

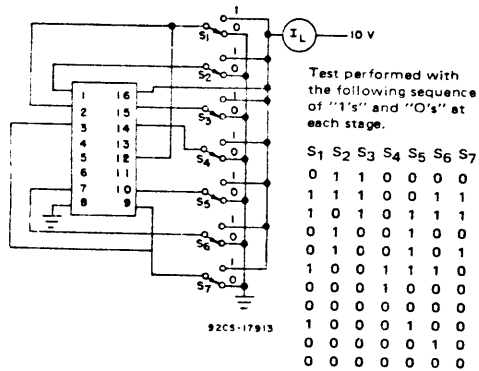


Fig. 13.9—Quiescent device current test circuit.

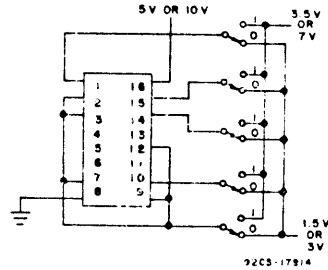


Fig. 13.10—Noise immunity test circuit.

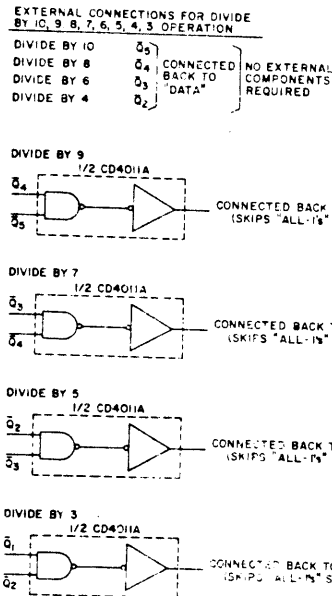


Fig. 13.11—External connections for divide by 10, 9, 8, 7, 6, 5, 4, 3 operation.

D COMPONENT DESCRIPTIONS  
D.6 INTEGRATED CIRCUITS

4018 cont'd

**DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $C_L = 15\text{ pF}$ ,  
and input rise and fall times = 20 ns except  $t_{rCL}$ ,  $t_{fCL}$   
Typical Temperature Coefficient for all values of  $V_{DD} = 0.3\%/^\circ\text{C}$  (See Appendix for Waveforms)**

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS						UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.
			CD4018AD CD4018AK CD4018AF			CD4018AE				
			$V_{DD}$ (Volts)	Min.	Typ.	Max.	Min.	Typ.		
<b>CLOCKED OPERATION</b>										
Propagation Delay Time To $\bar{Q}_5$ Output	$t_{PHL}$	5	-	350	1000	-	350	1300	ns	13.4
		10	-	125	250	-	125	300		
To Other Outputs	$t_{PLH}$	5	-	500	1200	-	500	1600	ns	13.3
		10	-	200	400	-	200	500		
Transition Time To $\bar{Q}_5$ Output	$t_{THL}$	5	-	100	300	-	100	350	ns	13.6
		10	-	50	150	-	50	200		
To Other Outputs	$t_{TLH}$	5	-	300	900	-	300	1200	ns	13.5
		10	-	125	350	-	125	450		
Minimum Clock Pulse Width	$t_{WL}$ $t_{WH}$	5	-	200	500	-	200	830	ns	-
		10	-	100	170	-	100	250		
Clock Rise & Fall Time	$t_{rCL}$ $t_{fCL}$	5	-	-	15	-	-	15	$\mu\text{s}$	-
		10	-	-	15	-	-	15		
Data Input Set Up Time		5	-	175	500	-	175	700	ns	-
		10	-	75	200	-	75	300		
Maximum Clock Frequency	$f_{CL}$	5	1	25	-	0.6	25	MHz	-	
		10	3	5	-	2	5			
Input Capacitance	$C_i$	Any Input	-	5	-	-	5	$\text{pF}$	-	
<b>PRESET* OR RESET OPERATION</b>										
Propagation Delay Time To $\bar{Q}_5$ Output	$t_{PLH(PR)}$ $t_{PLH(PR)}$	5	-	350	1000	-	350	1300	ns	-
		10	-	125	250	-	125	300		
To Other Outputs	$t_{PLH(PR)}$ $t_{PLH(PR)}$	5	-	500	1200	-	500	1600	ns	-
		10	-	200	400	-	200	500		
Preset or Reset Pulse Width	$t_{WH(PR)}$ $t_{WH(PR)}$	5	-	200	500	-	200	830	ns	-
		10	-	100	165	-	100	250		
Preset or Reset Removal Time		5	-	300	750	-	300	1000	ns	-
		10	-	100	225	-	100	275		

\*At Preset Enable or Jam Inputs

D COMPONENT DESCRIPTIONS  
 D.6 INTEGRATED CIRCUITS

4070 (MM74C86 is similar, not an exact replacement)

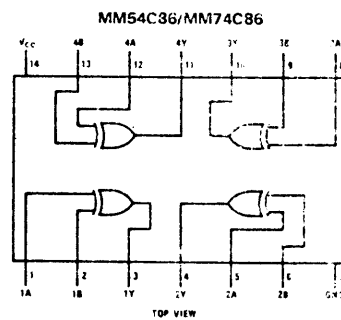
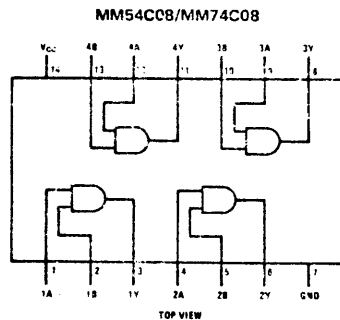
**general description**

Employing complementary MOS (CMOS) transistors to achieve wide power supply operating range, low power consumption and high noise margin these gates provide basic functions used in the implementation of digital integrated circuit systems. The N and P-channel enhancement mode transistors provide a symmetrical circuit with output swing essentially equal to the supply voltage. No dc power other than that caused by leakage current is consumed during static condition. All inputs are protected from damage due to static discharge by diode clamps to  $V_{CC}$  and GND.

**features**

- Wide supply voltage range      3.0V to 15V
- Guaranteed noise margin          1.0V
- High noise immunity              0.45  $V_{CC}$  typ
- Low power consumption            fan out of 2  
TTL compatibility                  driving 74L
- Low power consumption            10 nW/package typ

**connection diagrams**



**truth tables**

MM54C08/MM74C08

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

MM54C86/MM74C86

INPUTS		OUTPUTS
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High Level    L = Low Level

D COMPONENT DESCRIPTIONS  
D.6 INTEGRATED CIRCUITS

4070 cont'd

**absolute maximum ratings** (Note 1)

Voltage at Any Pin	-0.3V to $V_{CC} + 0.3V$
Operating Temperature Range	
MM54C08, MM54C86	-55°C to +125°C
MM74C08, MM74C86	-40°C to +95°C
Storage Temperature Range	-65°C to +150°C
Package Dissipation	500 mW
Operating $V_{CC}$ Range	3.0V to 15V
Absolute Maximum $V_{CC}$	16V
Lead Temperature (Soldering, 10 seconds)	300°C

**dc electrical characteristics**

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>CMOS TO CMOS</b>					
Logical "1" Input Voltage ( $V_{IN(1)}$ )	$V_{CC} = 5.0V$ $V_{CC} = 10V$	3.5 8.0			V V
Logical "0" Input Voltage ( $V_{IN(0)}$ )	$V_{CC} = 5.0V$ $V_{CC} = 10V$			1.5 2.0	V V
Logical "1" Output Voltage ( $V_{OUT(1)}$ )	$V_{CC} = 5.0V, I_O = -10\mu A$ $V_{CC} = 10V, I_O = -10\mu A$	4.5 9.0			V V
Logical "0" Output Voltage ( $V_{OUT(0)}$ )	$V_{CC} = 5.0V, I_O = +10\mu A$ $V_{CC} = 10V, I_O = +10\mu A$			0.5 1.0	V V
Logical "1" Input Current ( $I_{IN(1)}$ )	$V_{CC} = 15V, V_{IN} = 15V$		0.005	1.0	$\mu A$
Logical "0" Input Current ( $I_{IN(0)}$ )	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		$\mu A$
Supply Current ( $I_{CC}$ )	$V_{CC} = 15V$		0.01	15	$\mu A$
<b>CMOS/LPTTL INTERFACE</b>					
Logical "1" Input Voltage ( $V_{IN(1)}$ )	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
Logical "0" Input Voltage ( $V_{IN(0)}$ )	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$			0.8 0.8	V V
Logical "1" Output Voltage ( $V_{OUT(1)}$ )	54C, $V_{CC} = 4.5V, I_O = -360\mu A$ 74C, $V_{CC} = 4.75V, I_O = -360\mu A$	2.4 2.4			V V
Logical "0" Output Voltage ( $V_{OUT(0)}$ )	54C, $V_{CC} = 4.5V, I_O = +360\mu A$ 74C, $V_{CC} = 4.75V, I_O = +360\mu A$			0.4 0.4	V V
<b>OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)</b>					
Output Source Current ( $I_{SOURCE}$ ) (P-Channel)	$V_{CC} = 5.0V, V_{OUT} = 0V$ $T_A = 25^\circ C$	-1.75	-3.3		mA
Output Source Current ( $I_{SOURCE}$ ) (P-Channel)	$V_{CC} = 10V, V_{OUT} = 0V$ $T_A = 25^\circ C$	-8.0	-15		mA
Output Sink Current ( $I_{SINK}$ ) (N-Channel)	$V_{CC} = 5.0V, V_{OUT} = V_{CC}$ $T_A = 25^\circ C$	1.75	3.6		mA
Output Sink Current ( $I_{SINK}$ ) (N-Channel)	$V_{CC} = 10V, V_{OUT} = V_{CC}$ $T_A = 25^\circ C$	8.0	16		mA

D COMPONENT DESCRIPTIONS  
D.6 INTEGRATED CIRCUITS

4070 cont'd

**ac electrical characteristics**

(MM54C08/MM74C08)  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$ , unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time to Logical "1" or "0" ( $t_{pd}$ )	$V_{CC} = 5.0\text{V}$		80	140	ns
	$V_{CC} = 10\text{V}$		40	70	ns
Input Capacitance ( $C_{IN}$ )	Note 2		5.0		pF
Power Dissipation Capacitance ( $C_{PD}$ )	Note 3 Per Gate		14		pF

**ac electrical characteristics**

(MM54C86/MM74C86)  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$ , unless otherwise specified

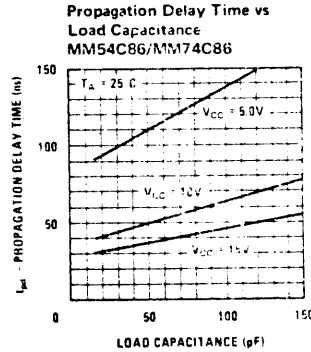
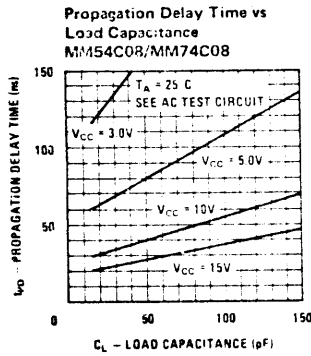
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time to Logical "1" or "0" ( $t_{pd}$ )	$V_{CC} = 5.0\text{V}$		110	185	ns
	$V_{CC} = 10\text{V}$		50	90	ns
Input Capacitance ( $C_{IN}$ )	Note 2		5.0		pF
Power Dissipation Capacitance ( $C_{PD}$ )	Note 3 Per Gate		20		pF

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

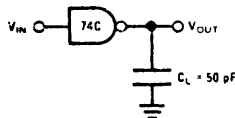
**Note 2:** Capacitance is guaranteed by periodic testing.

**Note 3:**  $C_{PD}$  determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

**typical performance characteristics**

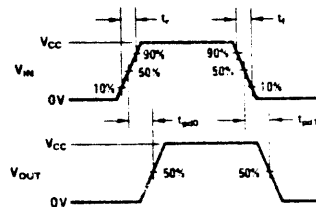


**ac test circuit**



NOTE: DELAYS MEASURED WITH INPUT  $t_r, t_f = 20\text{ ns}$

**switching time waveforms**



D COMPONENT DESCRIPTIONS  
D.6 INTEGRATED CIRCUITS

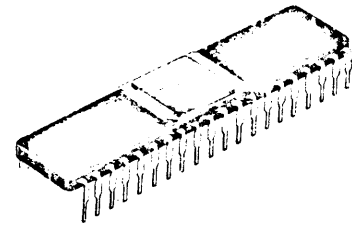
6800

**MICROPROCESSING UNIT (MPU)**

The MC6800 is a monolithic 8-bit microprocessor forming the central control function for Motorola's M6800 family. Compatible with TTL, the MC6800, as with all M6800 system parts, requires only one +5.0-volt power supply, and no external TTL devices for bus interface.

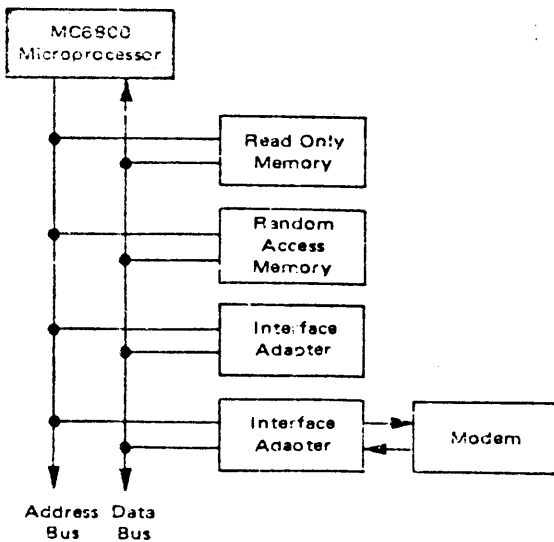
The MC6800 is capable of addressing 65 k bytes of memory with its 16-bit address lines. The 8-bit data bus is bidirectional as well as 3-state, making direct memory addressing and multiprocessing applications realizable.

- Eight-Bit Parallel Processing
- Bi-Directional Data Bus
- Sixteen-Bit Address Bus – 65 k Bytes of Addressing
- 72 Instructions – Variable Length
- Seven Addressing Modes – Direct, Relative, Immediate, Indexed, Extended, Implied and Accumulator
- Variable Length Stack
- Vectored Restart
- Maskable Interrupt Vector
- Separate Non-Maskable Interrupt – Internal Registers Saved In Stack
- Six Internal Registers – Two Accumulators, Index Register, Program Counter, Stack Pointer and Condition Code Register
- Direct Memory Addressing (DMA) and Multiple Processor Capability
- Clock Rates as High as 1 MHz
- Simple Bus Interface Without TTL
- Halt and Single Instruction Execution Capability

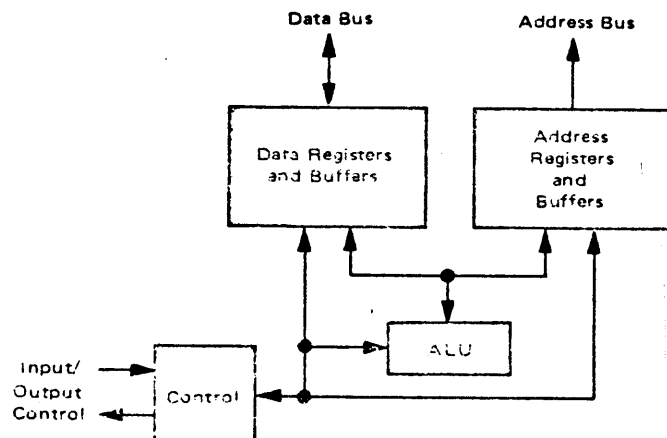


CERAMIC PACKAGE  
CASE 699

**M6800 MICROCOMPUTER FAMILY  
BLOCK DIAGRAM**



**MC6800 MICROPROCESSOR  
BLOCK DIAGRAM**



D COMPONENT DESCRIPTIONS  
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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V <sub>CC</sub>	-0.3 to +7.0	Vdc
Input Voltage	V <sub>in</sub>	-0.3 to +7.0	Vdc
Operating Temperature Range	T <sub>A</sub>	0 to +70	°C
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 5.0 V ± 5%, V<sub>SS</sub> = 0, T<sub>A</sub> = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage (Normal Operating Levels) Logic φ1, φ2	V <sub>IH</sub>	V <sub>SS</sub> + 2.4 V <sub>CC</sub> - 0.20	— —	V <sub>CC</sub> V <sub>CC</sub> + 0.25	Vdc
Input Low Voltage (Normal Operating Levels) Logic φ1, φ2	V <sub>IL</sub>	V <sub>SS</sub> - 0.3 V <sub>SS</sub> - 0.3	— —	V <sub>SS</sub> + 0.4 V <sub>SS</sub> + 0.2	Vdc
Input High Threshold Voltage Reset, NMI, Halt, IRQ, Data	V <sub>IHT</sub>	V <sub>SS</sub> + 2.0	—	—	Vdc
Input Low Threshold Voltage Reset, NMI, Halt, IRQ, Data	V <sub>ILT</sub>	—	—	V <sub>SS</sub> + 0.8	Vdc
Input Leakage Current (V <sub>in</sub> = 0 to 5.25 V, V <sub>CC</sub> = 0) Logic* φ1, φ2	I <sub>in</sub>	— —	— —	2.5 100	μAdc
Three-State (Off State) input Current (V <sub>in</sub> = 0.4 to 2.4 V, V <sub>CC</sub> = max) Data A0-A15, R/W	I <sub>TSI</sub>	— —	— —	10 100	μAdc
Output High Voltage (I <sub>Load</sub> = -100 μAdc, V <sub>CC</sub> = min)	V <sub>OH</sub>	V <sub>SS</sub> + 2.4	—	—	Vdc
Output Low Voltage (I <sub>Load</sub> = 1.6 mAdc, V <sub>CC</sub> = min)	V <sub>OL</sub>	—	—	V <sub>SS</sub> + 0.4	Vdc
Power Dissipation	P <sub>D</sub>	—	0.600	1.2	W
Capacitance (V <sub>in</sub> = 0, T <sub>A</sub> = 25°C, f = 1.0 MHz) Logic Data, TSC φ1, φ2 A0-A15, R/W	C <sub>in</sub>	— — —	— — —	10 15 200	pF
Frequency of Operation	C <sub>out</sub>	—	—	12	pF
Clock Timing For 1-MHz Operation (Figure 1) (C <sub>clock</sub> = 200 pF)	f	0.1	—	1.0	MHz
Cycle Time	t <sub>cyc</sub>	1.0	—	—	μs
Clock Pulse Width (Measured at V <sub>CC</sub> - 0.2 V) φ1 φ2	PW <sub>φH</sub>	430 470	— —	— —	ns
Rise and Fall Times (Measured between 0.2 V and V <sub>CC</sub> - 0.2 V) φ1, φ2	t <sub>r</sub> , t <sub>f</sub>	—	—	25	ns
Delay Time or Clock Overlap (Measured at 0.2 V)	t <sub>d</sub>	0	—	—	ns

\*Except IRQ and NMI, which require 3 kΩ pullup load resistors for wire-OR capability at optimum operation.

READ/WRITE TIMING Figures 2 and 3, f = 1.0 MHz, Loading = 130 pF and one TTL Load except VMA and BA Loading = 30 pF and one TTL Load.

Characteristic	Symbol	Min	Typ	Max	Unit
Read/Write Setup Time from MPU	T <sub>ASR</sub>	—	100	300	ns
Address Setup Time from MPU	T <sub>ASC</sub>	—	200	300	ns
Memory Read Access Time t <sub>cyc</sub> - (T <sub>ASC</sub> + T <sub>DSU</sub> + t <sub>r</sub> )	T <sub>ACC</sub>	—	—	575	ns
Data Setup Time	T <sub>DSU</sub>	100	—	—	ns
Address Setup Time from MPU for VMA	T <sub>VSC</sub>	—	150	300	ns
Data Hold Time	T <sub>H</sub>	10	30	—	ns
Enable High Time for DBE Input	T <sub>EH</sub>	470	—	—	ns
Data Setup Time from MPU	T <sub>ASD</sub>	—	150	200	ns

D COMPONENT DESCRIPTIONS  
 D.6 INTEGRATED CIRCUITS

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FIGURE 1 -- CLOCK TIMING WAVEFORM:

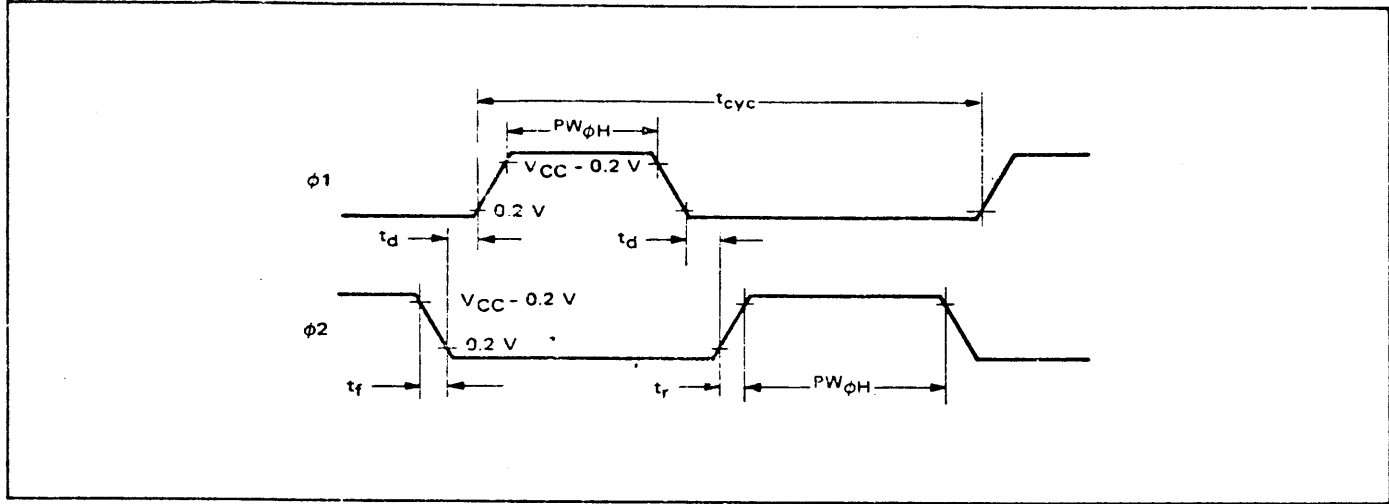
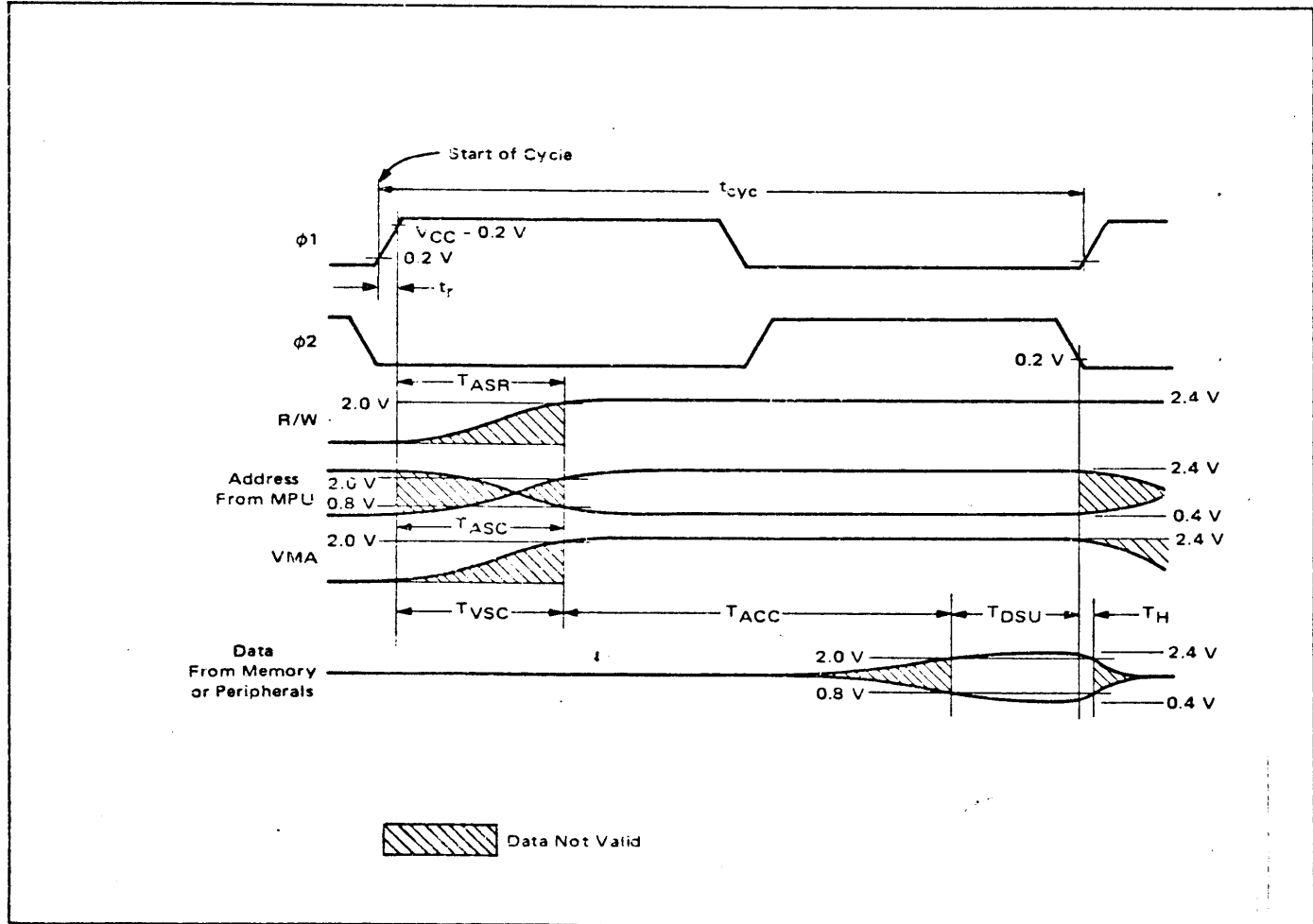


FIGURE 2 -- READ DATA FROM MEMORY OR PERIPHERALS

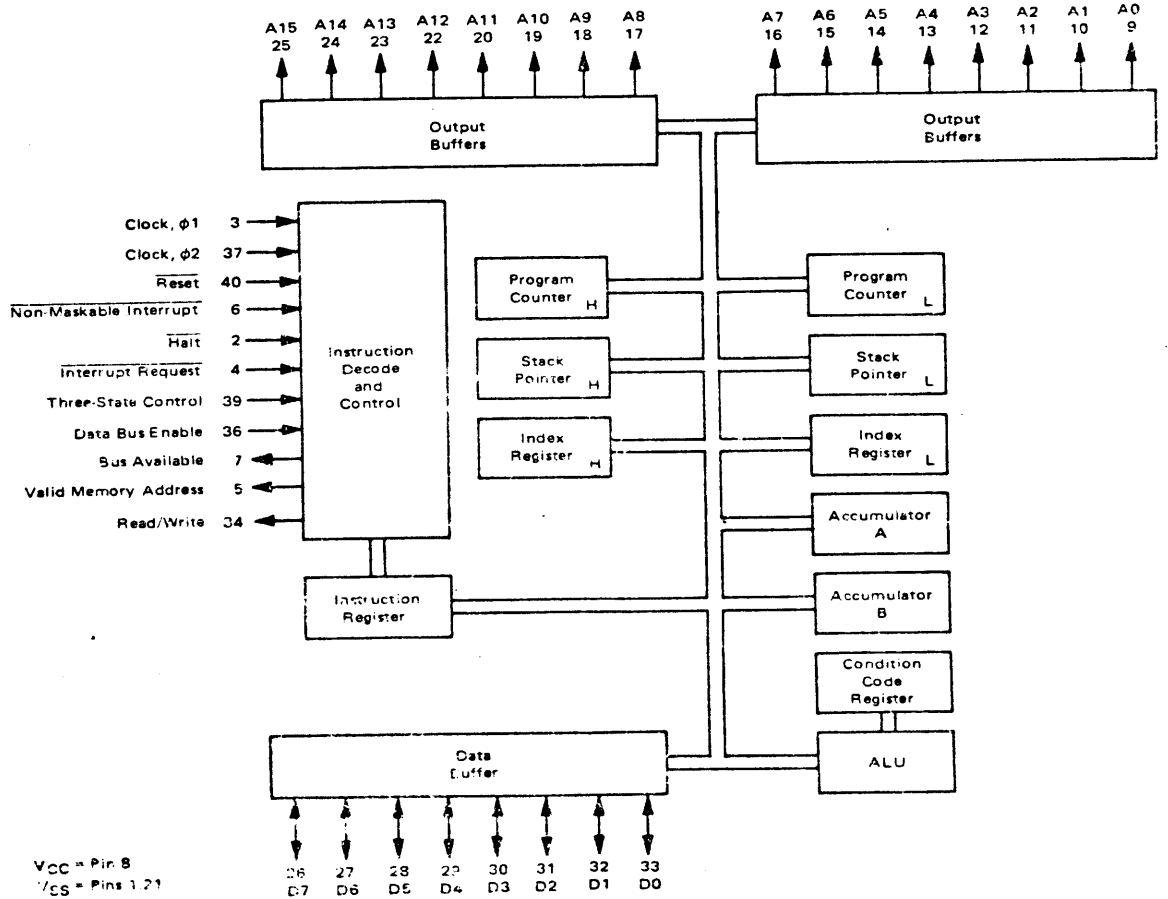
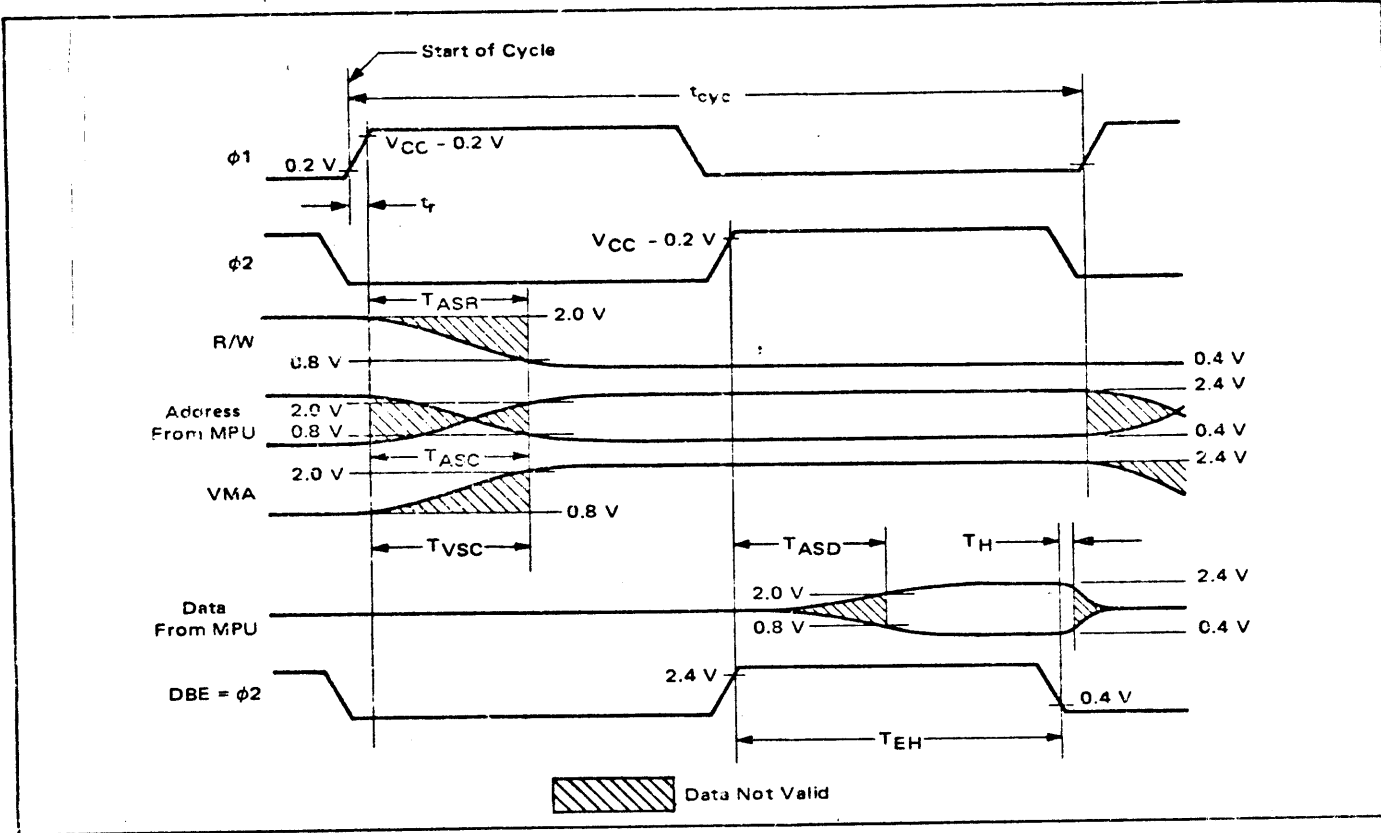




D COMPONENT DESCRIPTIONS  
 D.6 INTEGRATED CIRCUITS

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FIGURE 3 - WRITE DATA IN MEMORY OR PERIPHERALS



6800 cont'd

### MPU SIGNAL DESCRIPTION

Proper operation of the MPU requires that certain control and timing signals be provided to accomplish specific functions and that other signal lines be monitored to determine the state of the processor.

**Clocks Phase One and Phase Two ( $\phi 1, \phi 2$ )** — Two pins are used for a two-phase non-overlapping clock that runs at the  $V_{CC}$  voltage level.

**Address Bus (A0-A15)** — Sixteen pins are used for the address bus. The outputs are three-state bus drivers capable of driving one standard TTL load and 130 pF. When the output is turned off, it is essentially an open circuit. This permits the MPU to be used in DMA applications.

**Data Bus (D0-D7)** — Eight pins are used for the data bus. It is bi-directional, transferring data to and from the memory and peripheral devices. It also has three-state output buffers capable of driving one standard TTL load and 130 pF.

**Halt** — When this input is in the low state, all activity in the machine will be halted. This input is level sensitive. In the halt mode, the machine will stop at the end of an instruction, Bus Available will be at a one level, Valid Memory Address will be at a zero, and all other three-state lines will be in the three-state mode.

Transition of the  $\overline{\text{Halt}}$  line must not occur during the last 250 ns of phase one. To insure single instruction operation, the  $\overline{\text{Halt}}$  line must go high for one Phase One Clock cycle.

**Three-State Control (TSC)** — This input causes all of the address lines and the Read/Write line to go into the off or high impedance state. This state will occur 500 ns after  $TSC = 2.4 V$ . The Valid Memory Address and Bus Available signals will be forced low. The data bus is not affected by TSC and has its own enable (Data Bus Enable). In DMA applications, the Three-State Control line should be brought high on the leading edge of the Phase One Clock. The  $\phi 1$  clock must be held in the high state and the  $\phi 2$  in the low state for this function to operate properly. The address bus will then be available for other devices to directly address memory. Since the MPU is a dynamic device, it can be held in this state for only 5.0  $\mu s$  or destruction of data will occur in the MPU.

**Read/Write (R/W)** — This TTL compatible output signals the peripherals and memory devices whether the MPU is in a Read (high) or Write (low) state. The normal standby state of this signal is Read (high). Three-State Control going high will turn Read/Write to the off (high impedance) state. Also, when the processor is halted, it will be in the off state. This output is capable of driving one standard TTL load and 130 pF.

**Valid Memory Address (VMA)** — This output indicates to peripheral devices that there is a valid address on the address bus. In normal operation, this signal should be utilized for enabling peripheral interfaces such as the PIA and ACIA. This signal is not three-state. One standard TTL load and 30 pF may be directly driven by this active high signal.

**Data Bus Enable (DBE)** — This input is the three-state control signal for the MPU data bus and will enable the bus drivers when in the high state. This input is TTL compatible; however in normal operation, it would be driven by the phase two clock. During an MPU read cycle, the data bus drivers will be disabled internally. When it is desired that another device control the data bus such as in Direct Memory Access (DMA) applications, DBE should be held low.

**Bus Available (BA)** — The Bus Available signal will normally be in the low state; when activated, it will go to the high state indicating that the microprocessor has stopped and that the address bus is available. This will occur if the  $\overline{\text{Halt}}$  line is in the low state or the processor is in the WAIT state as a result of the execution of a WAIT instruction. At such time, all three-state output drivers will go to their off state and other outputs to their normally inactive level. The processor is removed from the WAIT state by the occurrence of a maskable (mask bit 1 = 0) or nonmaskable interrupt. This output is capable of driving one standard TTL load and 30 pF.

**Interrupt Request ( $\overline{\text{IRQ}}$ )** — This level sensitive input requests that an interrupt sequence be generated within the machine. The processor will wait until it completes the current instruction that is being executed before it recognizes the request. At that time, if the interrupt mask bit in the Condition Code Register is not set, the machine will begin an interrupt sequence. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. Next the MPU will respond to the interrupt request by setting the interrupt mask bit high so that no further interrupts may occur. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFF8 and FFF9. An address loaded at these locations causes the MPU to branch to an interrupt routine in memory.

The  $\overline{\text{Halt}}$  line must be in the high state for interrupts to be recognized.

The  $\overline{\text{IRQ}}$  has a high impedance pullup device internal to the chip; however a 3 k $\Omega$  external resistor to  $V_{CC}$  should be used for wire-OR and optimum control of interrupts.

**Reset** — This input is used to reset and start the MPU from a power down condition, resulting from a power failure or an initial start-up of the processor. If a positive edge is detected on the input, this will signal the MPU to begin the restart sequence. This will start execution of a routine to initialize the processor from its reset condition. All the higher order address lines will be forced high. For the restart, the last two (FFFF, FFFF) locations in memory will be used to load the program that is addressed by the program counter. During the restart routine, the interrupt mask bit is set and must be reset before the MPU can be interrupted by  $\overline{\text{IRQ}}$ .

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 D.6 INTEGRATED CIRCUITS

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Figure 4 shows the initialization of the microprocessor after restart.  $\overline{\text{Reset}}$  must be held low for at least eight clock periods after  $V_{CC}$  reaches 4.75 volts. If  $\overline{\text{Reset}}$  goes high prior to the leading edge of  $\phi 2$ , on the next  $\phi 1$  the first restart memory vector address (FFFE) will appear on the address lines. This location should contain the higher order eight bits to be stored into the program counter. Following, the next address FFFF should contain the lower order eight bits to be stored into the program counter.

**Non-Maskable Interrupt (NMI)** – A low-going edge on this input requests that a non-mask-interrupt sequence be generated within the processor. As with the **Interrupt Request** signal, the processor will complete the current instruction that is being executed before it recognizes the **NMI** signal. The interrupt mask bit in the Condition Code Register has no effect on **NMI**.

The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFFC and FFFD. An address loaded at these locations causes the MPU to branch to a non-maskable interrupt routine in memory.

**NMI** has a high impedance pullup resistor internal to the chip; however a  $3\text{ k}\Omega$  external resistor to  $V_{CC}$  should be used for wire-OR and optimum control of interrupts.

Inputs  $\overline{\text{IRQ}}$  and  $\overline{\text{NMI}}$  are hardware interrupt lines that are sampled during  $\phi 2$  and will start the interrupt routine on the  $\phi 1$  following the completion of an instruction.

Figure 5 is a flow chart describing the major decision paths and interrupt vectors of the microprocessor. Table 1 gives the memory map for interrupt vectors.

FIGURE 4 – INITIALIZATION OF MPU AFTER RESTART

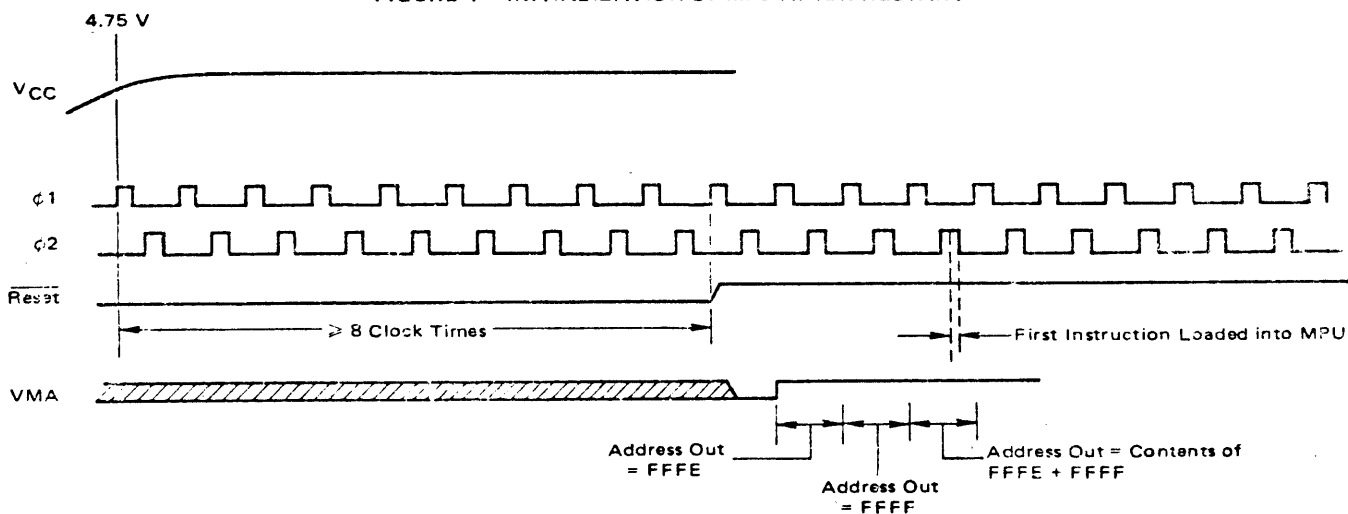
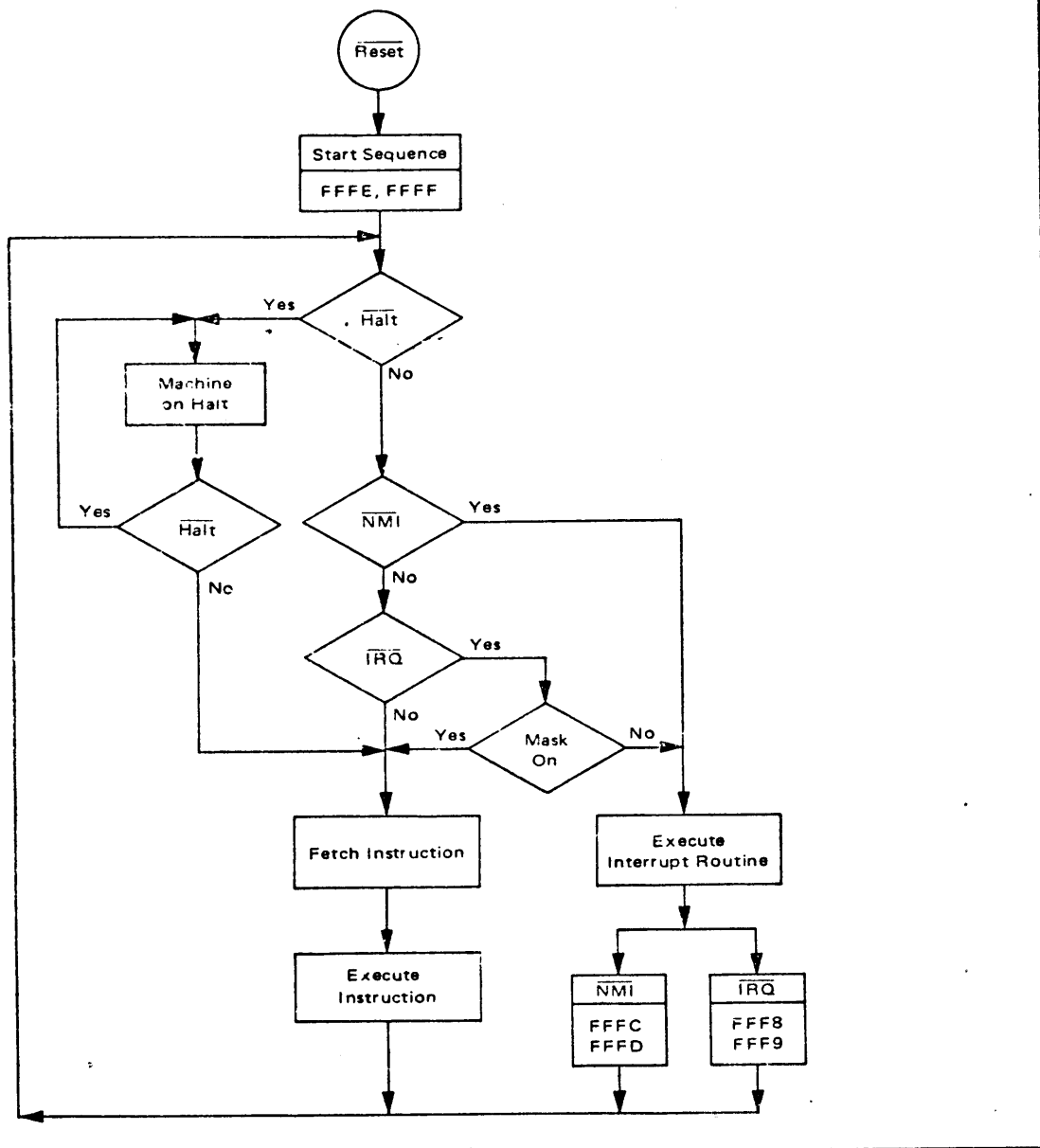


TABLE 1 – MEMORY MAP FOR INTERRUPT VECTORS

Vector		Description
MS	LS	
FFFE	FFFF	Restart
FFFC	FFFD	Non-maskable Interrupt
FFFA	FFFB	Software Interrupt
FFF8	FFF9	Interrupt Request

6800 cont'd

FIGURE 5 - MPU FLOW CHART



### MPU REGISTERS

The MPU has three 16-bit registers and three 3-bit registers available for use by the programmer (Figure 6).

**Program Counter** — The program counter is a two byte (16-bits) register that points to the current program address.

**Stack Pointer** — The stack pointer is a two byte register that contains the address of the next available location in an external push-down/pop-up stack. This stack is normally a random access Read/Write memory that may

have any location (address) that is convenient. In those applications that require storage of information in the stack when power is lost, the stack must be non-volatile.

**Index Register** — The index register is a two byte register that is used to store data or a sixteen bit memory address for the Indexed mode of memory addressing.

**Accumulators** — The MPU contains two 8-bit accumulators that are used to hold operands and results from an arithmetic logic unit (ALU).

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FIGURE 6 - PROGRAMMING MODEL OF THE MICROPROCESSING UNIT

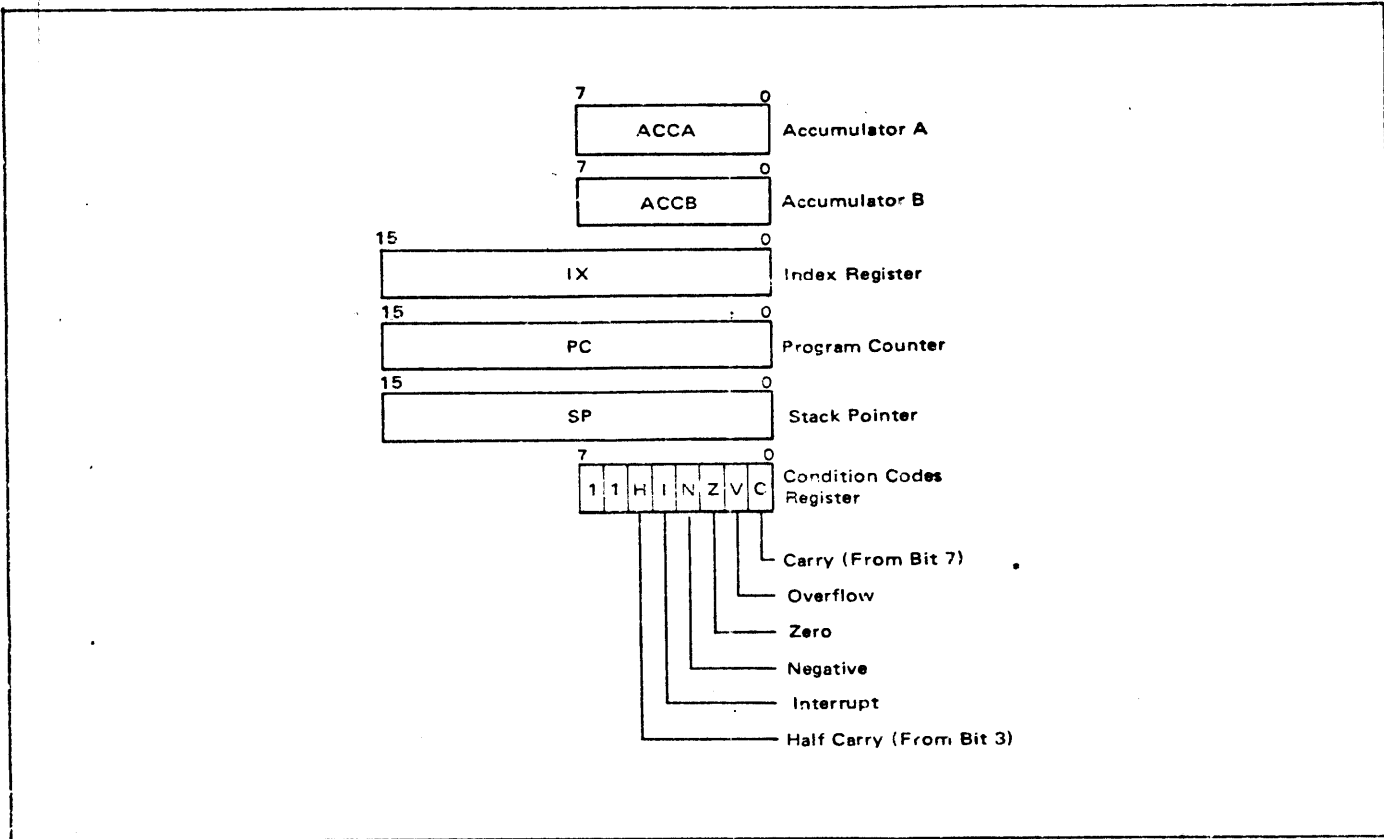
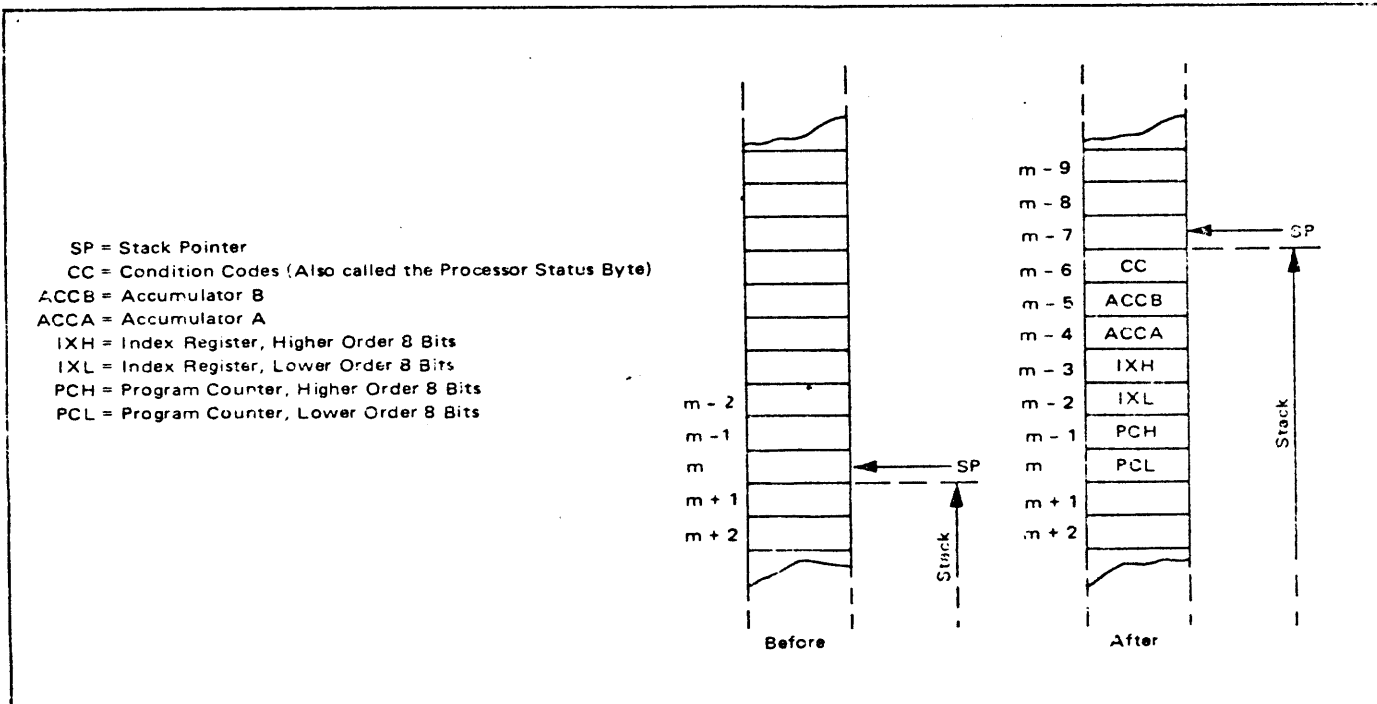


FIGURE 7 - SAVING THE STATUS OF THE MICROPROCESSOR IN THE STACK



6800 cont'd

**Condition Code Register** — The condition code register indicates the results of an Arithmetic Logic Unit operation: Negative (N), Zero (Z), Overflow (V), Carry from bit 7 (C), and half carry from bit 3 (H). These bits of the Condition Code Register are used as testable conditions for the conditional branch instructions. Bit 4 is the interrupt mask bit (I). The unused bits of the Condition Code Register (b6 and b7) are ones.

Figure 8 shows the order of saving the microprocessor status within the stack.

### MPU INSTRUCTION SET

The MC6800 has a set of 72 different instructions. Included are binary and decimal arithmetic, logical, shift, rotate, load, store, conditional or unconditional branch, interrupt and stack manipulation instructions (Tables 2 thru 6).

### MPU ADDRESSING MODES

The MC6800 eight-bit microprocessing unit has seven address modes that can be used by a programmer, with the addressing mode a function of both the type of instruction and the coding within the instruction. A summary of the addressing modes for a particular instruction can be found in Table 7 along with the associated instruction execution time that is given in machine cycles. With a clock frequency of 1 MHz, these times would be microseconds.

**Accumulator (ACCX) Addressing** — In accumulator only addressing, either accumulator A or accumulator B is specified. These are one-byte instructions.

**Immediate Addressing** — In immediate addressing, the operand is contained in the second byte of the instruction except LDS and LDX which have the operand in the second and third bytes of the instruction. The MPU addresses

this location when it fetches the immediate instruction for execution. These are two or three-byte instructions.

**Direct Addressing** — In direct addressing, the address of the operand is contained in the second byte of the instruction. Direct addressing allows the user to directly address the lowest 256 bytes in the machine (i.e., locations zero through 255). Enhanced execution times are achieved by storing data in these locations. In most configurations, it should be a random access memory. These are two-byte instructions.

**Extended Addressing** — In extended addressing, the address contained in the second byte of the instruction is used as the higher eight-bits of the address of the operand. The third byte of the instruction is used as the lower eight-bits of the address for the operand. This is an absolute address in memory. These are three-byte instructions.

**Indexed Addressing** — In indexed addressing, the address contained in the second byte of the instruction is added to the index register's lowest eight bits in the MPU. The carry is then added to the higher order eight bits of the index register. This result is then used to address memory. The modified address is held in a temporary address register so there is no change to the index register. These are two-byte instructions.

**Implied Addressing** — In the implied addressing mode the instruction gives the address (i.e., stack pointer, index register, etc.). These are one-byte instructions.

**Relative Addressing** — In relative addressing, the address contained in the second byte of the instruction is added to the program counter's lowest eight bits plus two. The carry or borrow is then added to the high eight bits. This allows the user to address data within a range of -125 to +129 bytes of the present instruction. These are two-byte instructions.

TABLE 2 — MICROPROCESSOR INSTRUCTION SET — ALPHABETIC SEQUENCE

ASA	Add Accumulators	CLR	Clear	PUL	Pull Data
ADC	Add with Carry	CLV	Clear Overflow	ROL	Rotate Left
ADD	Add	CLW	Clear Overflow	ROR	Rotate Right
AND	Logical And	CMP	Compare	RTI	Return from Interrupt
ASL	Arithmetic Shift Left	COM	Complement	RTS	Return from Subroutine
ASR	Arithmetic Shift Right	CPX	Compare Index Register	SBA	Subtract Accumulators
ECC	Branch if Carry Clear	DAA	Decimal Adjust	SBC	Subtract with Carry
BCS	Branch if Carry Set	DEC	Decrement	SEC	Set Carry
BEQ	Branch if Equal to Zero	DES	Decrement Stack Pointer	SEI	Set Interrupt Mask
BGE	Branch if Greater or Equal Zero	DEX	Decrement Index Register	SEV	Set Overflow
BGT	Branch if Greater than Zero	EOR	Exclusive OR	STA	Store Accumulator
BHI	Branch if Higher	INC	Increment	STS	Store Stack Register
BIT	Bit Test	INS	Increment Stack Pointer	STX	Store Index Register
BLE	Branch if Less or Equal	INX	Increment Index Register	SUB	Subtract
BLS	Branch if Lower or Same	JMP	Jump	SWI	Software Interrupt
BLT	Branch if Less than Zero	JSR	Jump to Subroutine	TAB	Transfer Accumulators
BMI	Branch if Minus	LDA	Load Accumulator	TAP	Transfer Accumulators to Condition Code Reg.
BNE	Branch if Not Equal to Zero	LDS	Load Stack Pointer	TBA	Transfer Accumulators
BPL	Branch if Plus	LDX	Load Index Register	TPA	Transfer Condition Code Reg. to Accumulator
BRN	Branch Always	LSR	Logical Shift Right	TST	Test
BSR	Branch to Subroutine	NEG	Negate	TSX	Transfer Stack Pointer to Index Register
BVC	Branch if Overflow Clear	NOP	No Operation	TXS	Transfer Index Register to Stack Pointer
BVS	Branch if Overflow Set	ORA	Inclusive OR Accumulator	WAI	Wait for Interrupt
CBA	Compare Accumulators	PSH	Push Data		
CLC	Clear Carry				
CLI	Clear Interrupt Mask				

D COMPONENT DESCRIPTIONS  
D.6 INTEGRATED CIRCUITS

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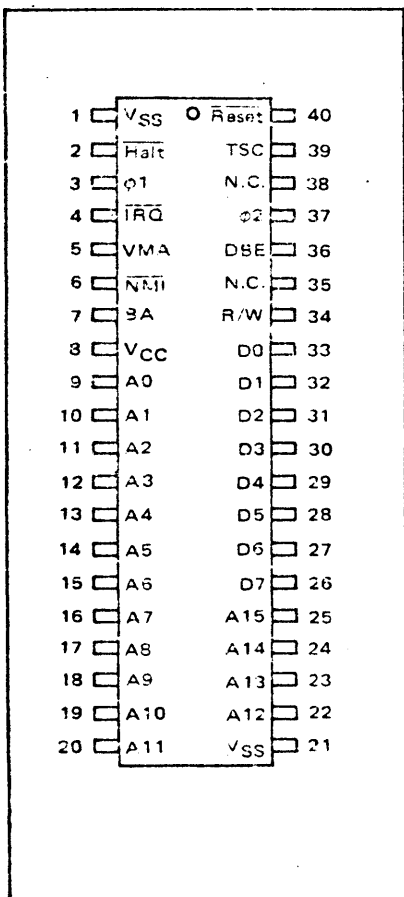
TABLE 6 - CONDITION CODE REGISTER MANIPULATION INSTRUCTIONS

OPERATIONS	MNEMNIC	IMPLIED			BOOLEAN OPERATION	COND. CODE REG.					
		OP	~	=		5	4	3	2	1	0
						H	I	N	Z	V	C
Clear Carry	CLC	0C	2	1	0 → C	•	•	•	•	•	R
Clear Interrupt Mask	CLI	0E	2	1	0 → I	•	R	•	•	•	•
Clear Overflow	CLV	0A	2	1	0 → V	•	•	•	•	R	•
Set Carry	SEC	0D	2	1	1 → C	•	•	•	•	•	S
Set Interrupt Mask	SEI	0F	2	1	1 → I	•	S	•	•	•	•
Set Overflow	SEV	0B	2	1	1 → V	•	•	•	•	S	•
Accmltr A → CCR	TAP	06	2	1	A → CCR	⑫					
CCR → Accmltr A	TPA	07	2	1	CCR → A	•	•	•	•	•	•

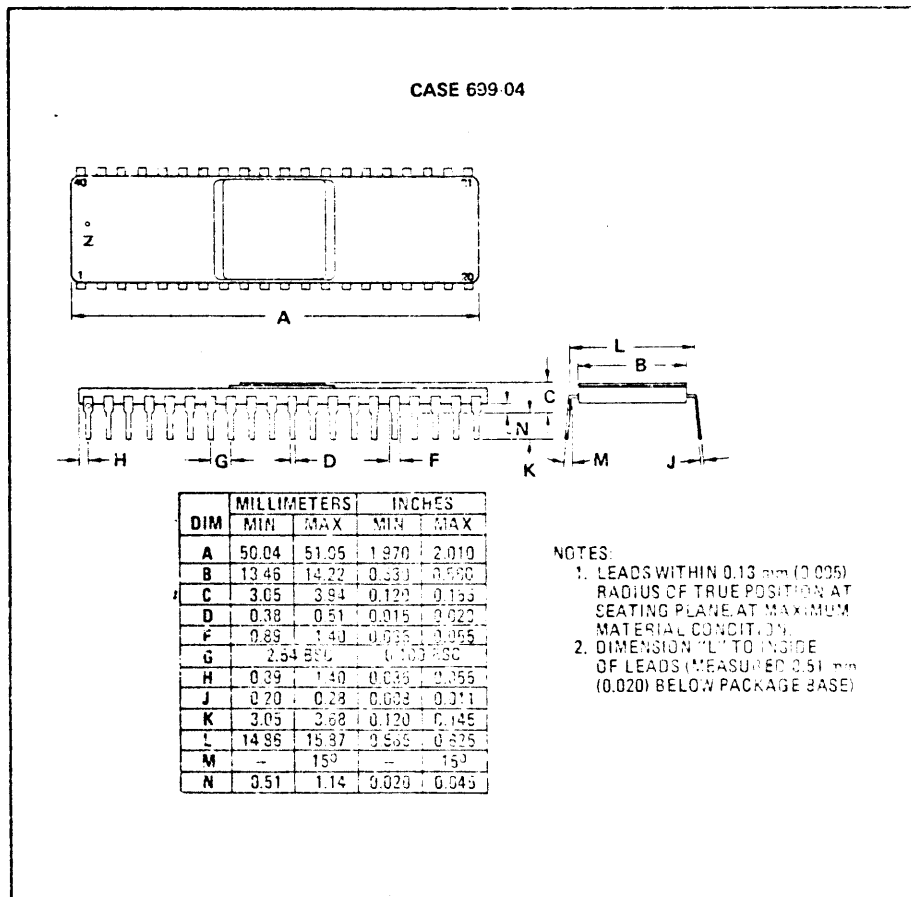
CONDITION CODE REGISTER NOTES:

- (Bit set if test is true and cleared otherwise)
- (Bit V) Test: Result = 10000000?
  - (Bit C) Test: Result = 00000000?
  - (Bit C) Test: Decimal value of most significant BCD Character greater than nine? (Not cleared if previously set.)
  - (Bit V) Test: Operand = 10000000 prior to execution?
  - (Bit V) Test: Operand = 01111111 prior to execution?
  - (Bit V) Test: Set equal to result of NDC after shift has occurred.
  - (Bit N) Test: Sign bit of most significant (MS) byte = 1?
  - (Bit V) Test: 2's complement overflow from subtraction of MS bytes?
  - (Bit N) Test: Result less than zero? (Bit 15 = 1)
  - (A) Load Condition Code Register from Stack. (See Special Operations)
  - (Bit I) Set when interrupt occurs. If previously set, a Non Maskable Interrupt is required to exit the wait state.
  - (A) Set according to the contents of Accumulator A.

PIN ASSIGNMENT



PACKAGE DIMENSIONS



D COMPONENT DESCRIPTIONS  
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TABLE 7 - INSTRUCTION ADDRESSING MODES AND ASSOCIATED EXECUTION TIMES  
 (Times in Machine Cycles)

	(Dual Operand)								(Dual Operand)						
	ACCX	Immediate	Direct	Extended	Indexed	Implied	Relative		ACCX	Immediate	Direct	Extended	Indexed	Implied	
ABA								INC	2			6	7		
ADC	x		2	3	4	5		INS						4	
ADD	x		2	3	4	5		INX						4	
AND	x		2	3	4	5		JMP				3	4		
ASL		2						JSR							
ASR		2			6	7		LDA	x		2	3	4	5	
BCC								LDS			3	4	5	6	
BCS								LDX			3	4	5	6	
BEA								LSR		2			6	7	
BGE								NEG		2			6	7	
BGT								NOP							
BHi								ORA	x		2	3	4	5	
BIT	x		2	3	4	5		PSH						4	
BLE								PUL						4	
BLS								ROL		2			6	7	
BLT								ROR		2			6	7	
BMI								RTI						10	
BNE								RTS						5	
BPL								SBA						2	
BRA								SBC	x		2	3	4	5	
BSR								SEC						2	
BVC								SEI						2	
BVS								SEV						2	
CBA						2		STA	x			4	5	6	
CLC						2		STS				5	6	7	
CLI						2		STX				5	6	7	
CLR		2			6	7		SUB	x		2	3	4	5	
CLV							2	SWI						12	
CMP	x		2	3	4	5		TAB						2	
COM		2			6	7		TAP						2	
CPX			3	4	5	6		TBA						2	
DAA							2	TPA						2	
DEC		2			6	7		TST		2			6	7	
DES							4	TSX						4	
DEX							4	TSX						4	
EOR	x		2	3	4	5		WAI						9	

NOTE: Interrupt time is 12 cycles from the end of the instruction being executed, except following a WAI instruction. Then it is 4 cycles.



D COMPONENT DESCRIPTIONS  
 D.6 INTEGRATED CIRCUITS

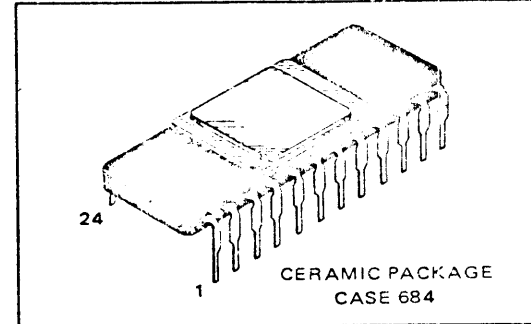
6810

**128 X 8-BIT STATIC RANDOM ACCESS MEMORY**

The MCM6810 is a byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

The memory is compatible with the M6800 Microcomputer Family, providing random storage in byte increments. Memory expansion is provided through multiple Chip Select inputs.

- Organized as 128 Bytes of 8 Bits
- Static Operation
- Bi-Directional Three-State Data Input/Output
- Six Chip Select Inputs (Four Active Low, Two Active High)
- Single 5-Volt Power Supply
- TTL-Compatible
- Maximum Access Time = 1.0  $\mu$ s for MCM6810L  
 575 ns for MCM5810L-1



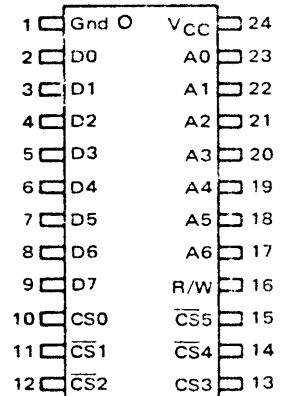
CERAMIC PACKAGE  
 CASE 684

**ABSOLUTE MAXIMUM RATINGS** (See Note 1)

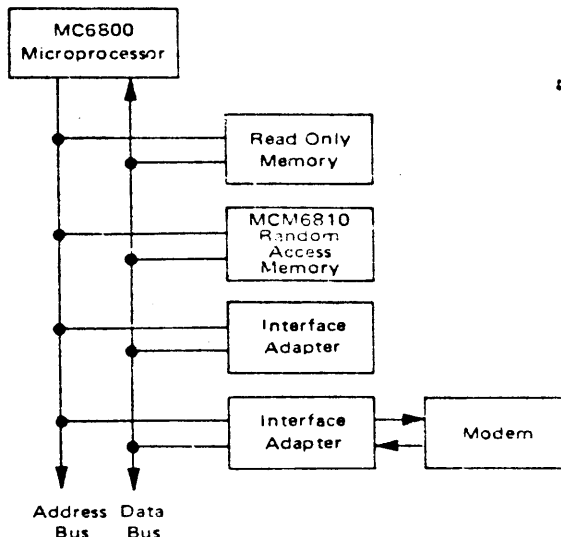
Rating	Symbol	Value	Unit
Supply Voltage	$V_{CC}$	-0.3 to +7.0	Vdc
Input Voltage	$V_{in}$	-0.3 to +7.0	Vdc
Operating Temperature Range	$T_A$	0 to +70	$^{\circ}$ C
Storage Temperature Range	$T_{stg}$	-55 to +150	$^{\circ}$ C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

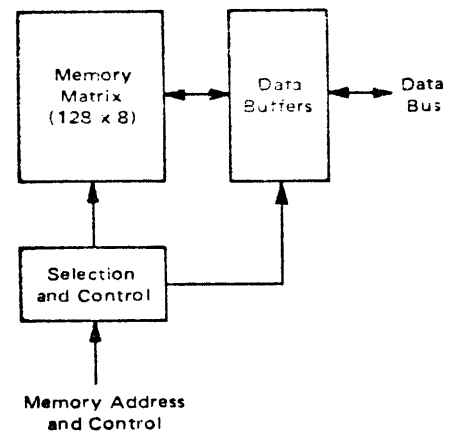
**PIN ASSIGNMENT**



**M6800 MICROCOMPUTER FAMILY  
 BLOCK DIAGRAM**



**MCM6810 RANDOM ACCESS MEMORY  
 BLOCK DIAGRAM**



D COMPONENT DESCRIPTIONS  
D.6 INTEGRATED CIRCUITS

6810 cont'd

DC OPERATING CONDITIONS AND CHARACTERISTICS  
(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	$V_{CC}$	4.75	5.0	5.25	Vdc
Input High Voltage	$V_{IH}$	2.4	—	5.25	Vdc
Input Low Voltage	$V_{IL}$	-0.3	—	0.4	Vdc

DC CHARACTERISTICS

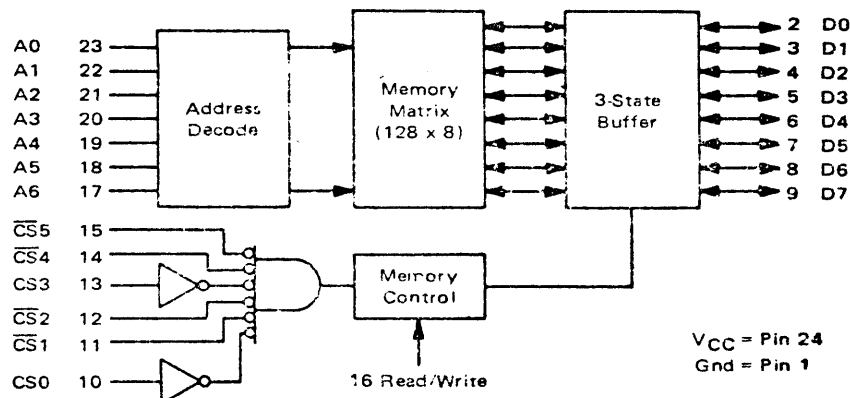
Characteristic	Symbol	Min	Typ	Max	Unit
Input Current ( $A_n, R/W, CS_n, \overline{CS}_n$ ) ( $V_{in} = 0$ to 5.25 V)	$I_{in}$	—	—	2.5	$\mu$ Adc
Input High Threshold Voltage	$V_{IHT}$	2.0	—	—	Vdc
Input Low Threshold Voltage	$V_{ILT}$	—	—	0.8	Vdc
Output High Voltage ( $I_{OH} = -100 \mu$ A)	$V_{OH}$	2.4	—	—	Vdc
Output Low Voltage ( $I_{OL} = 1.6$ mA)	$V_{OL}$	—	—	0.4	Vdc
Output Leakage Current (D0 – D7) ( $V_O = 2.4$ V, $CS = 0.4$ V, $\overline{CS} = 2.4$ V)	$I_{LOH}$	—	—	10	$\mu$ Adc
Output Leakage Current (D0 – D7) ( $V_O = 0.4$ V, $CS = 0.4$ V, $\overline{CS} = 2.4$ V)	$I_{LOL}$	—	—	10	$\mu$ Adc
Supply Current ( $V_{CC} = 5.25$ V, $T_A = 0^\circ$ C)	$I_{CC}$	—	—	130	mAdc

CAPACITANCE ( $f = 1.0$  MHz,  $T_A = 25^\circ$ C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance	$C_{in}$	7.5	pF
Output Capacitance	$C_{out}$	15	pF

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

BLOCK DIAGRAM



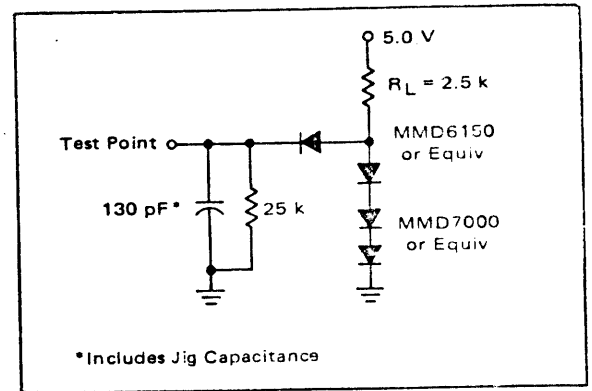
6810 cont'd

**AC OPERATING CONDITIONS AND CHARACTERISTICS**  
(Full operating voltage and temperature unless otherwise noted.)

**RECOMMENDED AC OPERATING CONDITIONS**

Parameter	Symbol	Min	Unit
Address Setup Time	$t_{AS}$	30	ns
Address Hold Time	$t_{AH}$	0	ns
Chip Select Pulse Width	$t_{CS}$		ns
MCM6810L		800	
MCM6810L-1		400	

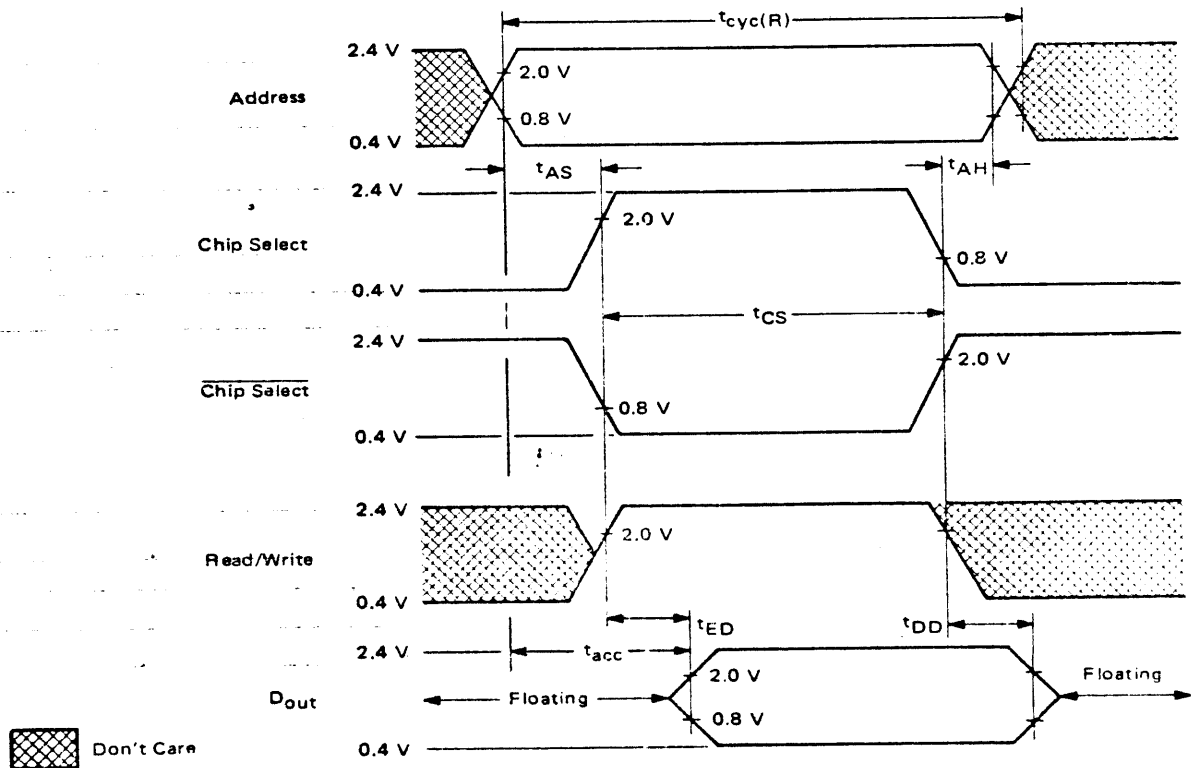
**FIGURE 1 – AC TEST LOAD**



**READ CYCLE** (All timing with  $t_r = t_f = 20$  ns, Load of Figure 1)

Characteristic		Symbol	Min	Max	Unit
Read Cycle Time	MCM6810L	$t_{cyc}(R)$	1000	—	ns
	MCM6810L-1		575	—	ns
Output Enable Delay Time	MCM6810L	$t_{ED}$	—	400	ns
	MCM6810L-1		—	300	ns
Output Disable Delay Time	MCM6810L	$t_{DD}$	10	200	ns
	MCM6810L-1		10	150	ns
Read Access Time	MCM6810L	$t_{acc}$	—	1000	ns
	MCM6810L-1		—	575	ns

**READ CYCLE TIMING**



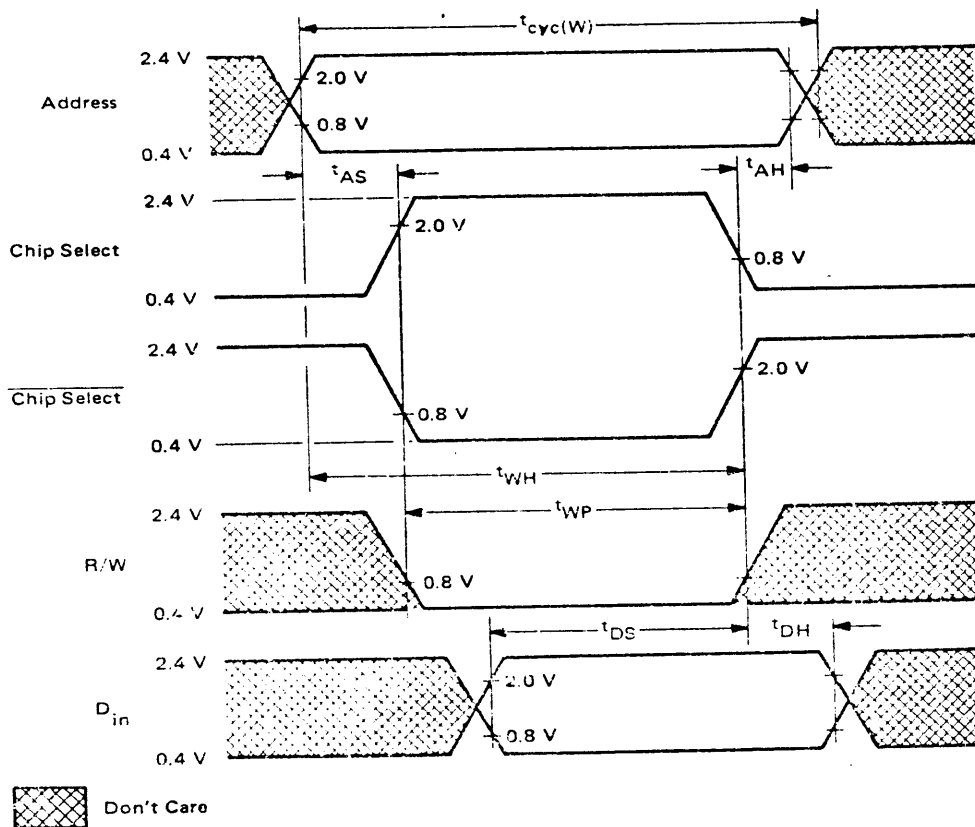
D COMPONENT DESCRIPTIONS  
D.6 INTEGRATED CIRCUITS

6810 cont'd

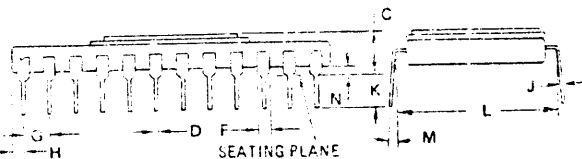
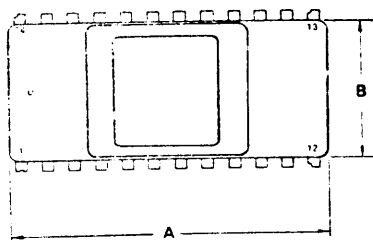
WRITE CYCLE (All timing with  $t_r = t_f = 20$  ns, Load of Figure 1)

Characteristic	Symbol	Min	Max	Unit
Write Cycle Time	MCM6810L	1000	—	ns
	MCM6810L-1	500	—	ns
Write Pulse Width	MCM6810L	800	—	ns
	MCM6810L-1	400	—	ns
Write Pulse Hold Time	MCM6810L	1000	—	ns
	MCM6810L-1	500	—	ns
Data Setup Time	MCM6810L	500	—	ns
	MCM6810L-1	300	—	ns
Data Hold Time	$t_{DH}$	0	—	ns

WRITE CYCLE TIMING



PACKAGE DIMENSIONS



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	29.04	30.26	1.143	1.215
B	12.70	14.22	0.500	0.560
C	8.89	9.54	0.350	0.375
D	6.35	6.75	0.250	0.265
E	7.62	8.25	0.300	0.325
F	2.54	2.54	0.100	0.100
G	0.76	1.27	0.030	0.050
H	0.76	1.27	0.030	0.050
I	0.76	1.27	0.030	0.050
J	2.54	2.54	0.100	0.100
K	2.54	2.54	0.100	0.100
L	2.54	2.54	0.100	0.100
M	2.54	2.54	0.100	0.100
N	0.76	1.27	0.030	0.050

NOTES

- LEADS WITHIN 0.13 mm (0.005 INCH) RADIUS OF TRUE POSITION AT SEATING PLANE WITH MAXIMUM MATERIAL CONDITION.
- LEAD NOT CUT FOR IDENTIFICATION, OR BUMP ON TOP.
- DIM L TO INSIDE OF LEADS (MEASURED 0.51 mm (0.020 INCH) BELOW PKG BASE)

CASE 024.04

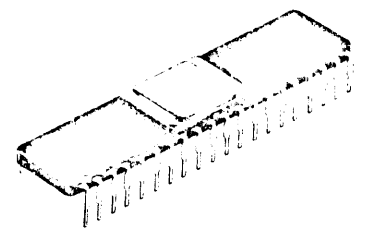
6820

### PERIPHERAL INTERFACE ADAPTER (PIA)

The MC6820 Peripheral Interface Adapter provides the universal means of interfacing peripheral equipment to the MC6800 Micro-processing Unit (MPU). This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

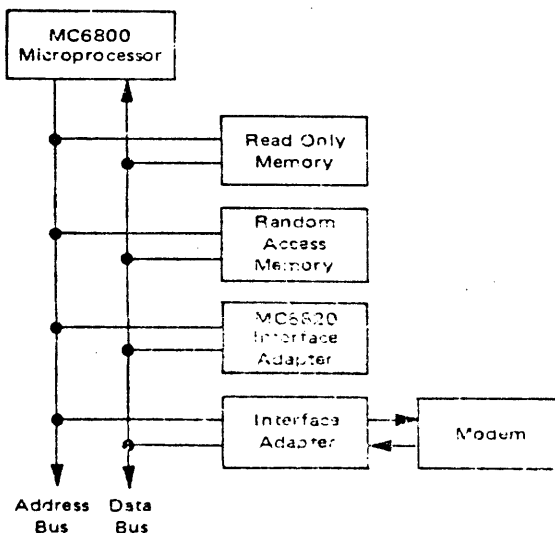
The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the over-all operation of the interface.

- 8-Bit Bidirectional Data Bus for Communication with the MPU
- Two Bidirectional 8-Bit Buses for Interface to Peripherals
- Two Programmable Control Registers
- Two Programmable Data Direction Registers
- Four Individually-Controlled Interrupt Input Lines; Two Usable as Peripheral Control Outputs
- Handshake Control Logic for Input and Output Peripheral Operation
- High-Impedance 3-State and Direct Transistor Drive Peripheral Lines
- Program Controlled Interrupt and Interrupt Disable Capability
- CMOS Compatible Peripheral Lines

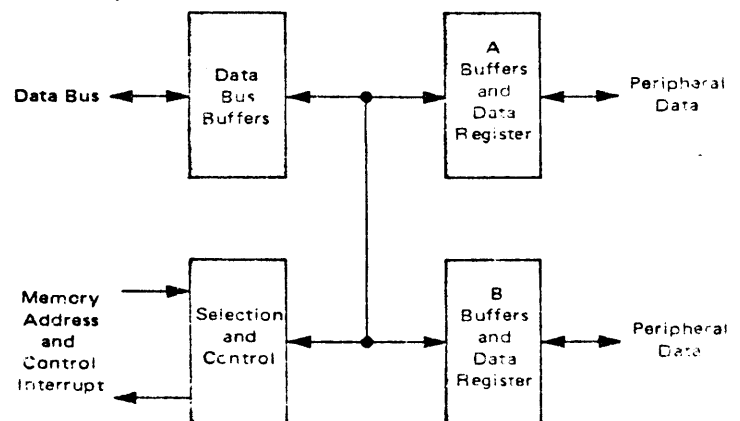


CERAMIC PACKAGE  
 CASE 699

M6800 MICROCOMPUTER FAMILY  
 BLOCK DIAGRAM



MC6820 PERIPHERAL INTERFACE ADAPTER  
 BLOCK DIAGRAM



D COMPONENTS DESCRIPTIONS  
D.6 INTEGRATED CIRCUITS

6820 cont'd

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V <sub>CC</sub>	-0.3 to +7.0	V <sub>dcc</sub>
Input Voltage	V <sub>in</sub>	-0.3 to +7.0	V <sub>dcc</sub>
Operating Temperature Range	T <sub>A</sub>	0 to +70	°C
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 5.0 V ± 5%, V<sub>SS</sub> = 0, T<sub>A</sub> = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage (Normal Operating Levels)	V <sub>IH</sub>	V <sub>SS</sub> + 2.4	—	V <sub>CC</sub>	V <sub>dcc</sub>
Input Low Voltage (Normal Operating Levels)	V <sub>IL</sub>	V <sub>SS</sub> - 0.3	—	V <sub>SS</sub> + 0.4	V <sub>dcc</sub>
Input High Threshold Voltage	V <sub>IHT</sub>	V <sub>SS</sub> + 2.0	—	—	V <sub>dcc</sub>
Input Low Threshold Voltage	V <sub>I LT</sub>	—	—	V <sub>SS</sub> + 0.8	V <sub>dcc</sub>
Input Leakage Current (V <sub>in</sub> = 0 to 5.0 V <sub>dcc</sub> ) R/W, Reset, RS0, RS1, CS0, CS1, CS2, CA1, CB1, Enable	I <sub>in</sub>	—	1.0	2.5	μA <sub>dcc</sub>
Tri-state (Off State) Input Current (V <sub>in</sub> = 0.4 to 2.4 V <sub>dcc</sub> , V <sub>CC</sub> = max)	I <sub>TSI</sub>	—	2.0	10	μA <sub>dcc</sub>
Input High Current (V <sub>IH</sub> = 2.4 V <sub>dcc</sub> )	I <sub>IH</sub>	-100	-250	—	μA <sub>dcc</sub>
Input Low Current (V <sub>IL</sub> = 0.4 V <sub>dcc</sub> )	I <sub>IL</sub>	—	-1.0	-1.6	mA <sub>dcc</sub>
Output High Voltage (V <sub>CC</sub> = min, I <sub>Load</sub> = -100 μA <sub>dcc</sub> , Enable Pulse Width < 25 μs)	V <sub>OH</sub>	V <sub>SS</sub> + 2.4	—	—	V <sub>dcc</sub>
Output Low Voltage (V <sub>CC</sub> = min, I <sub>Load</sub> = 1.6 mA <sub>dcc</sub> )	V <sub>OL</sub>	—	—	V <sub>SS</sub> + 0.4	V <sub>dcc</sub>
Output High Current (Sourcing) (V <sub>OH</sub> = 2.4 V <sub>dcc</sub> ) (V <sub>O</sub> = 1.5 V <sub>dcc</sub> , the current for driving other than TTL, e.g., Darlington Base)	I <sub>OH</sub>	-100	-1000	—	μA <sub>dcc</sub>
Output Low Current (Sinking) (V <sub>OL</sub> = 0.4 V <sub>dcc</sub> )	I <sub>OL</sub>	1.5	—	—	mA <sub>dcc</sub>
Output Leakage Current (Off State) IRQA, IROB	I <sub>off</sub>	—	1.0	10	μA <sub>dcc</sub>
Power Dissipation	P <sub>D</sub>	—	300	600	mW
Input Capacitance (V <sub>in</sub> = 0, T <sub>A</sub> = 25°C, f = 1.0 MHz) D0-D7, PA0-PA7, PB0-PB7, CA2, CB2 R/W, Reset, RS0, RS1, CS0, CS1, CS2, CA1, CB1 Enable	C <sub>in</sub>	—	—	10 7.0 20	pF
Output Capacitance (V <sub>in</sub> = 0, T <sub>A</sub> = 25°C, f = 1.0 MHz)	C <sub>out</sub>	—	—	10	pF

READ TIMING CHARACTERISTICS (Figure 1, Loading = 30 pF and one TTL load for PA0-PA7, PB0-PB7, CA2, CB2 = 130 pF and one TTL load for D0-D7, IRQA, IROB)

Characteristic	Symbol	Min	Typ	Max	Unit
Delay Time, Address valid to Enable positive transition	T <sub>AEW</sub>	180	—	—	ns
Delay Time, Enable positive transition to Data valid on bus	T <sub>EDH</sub>	—	—	205	ns
Combinational Data Set-up Time	T <sub>PSU</sub>	300	—	—	ns
Enable Hold Time	T <sub>EH</sub>	10	—	—	ns
Delay Time, Enable negative transition to CA2 negative transition	T <sub>CA2</sub>	—	—	1.0	μs
Delay Time, Enable negative transition to CA2 positive transition	T <sub>PS1</sub>	—	—	1.0	μs
Rise and Fall Time for CA1 and CA2 input signals	t <sub>r, f</sub>	—	—	1.0	μs
Delay Time from CA1 active transition to CA2 positive transition	T <sub>RS2</sub>	—	—	2.0	μs
Rise and Fall Time for Enable input	t <sub>r, f</sub>	—	—	25	ns

WRITE TIMING CHARACTERISTICS (Figure 2)

Characteristic	Symbol	Min	Typ	Max	Unit
Enable Pulse Width	T <sub>E</sub>	0.470	—	25	μs
Delay Time, Address valid to Enable positive transition	T <sub>AEW</sub>	180	—	—	ns
Delay Time, Data valid to Enable negative transition	T <sub>DSU</sub>	300	—	—	ns
Delay Time, Read/Write negative transition to Enable positive transition	T <sub>WE</sub>	130	—	—	ns
Enable Hold Time	T <sub>EH</sub>	10	—	—	ns
Delay Time, Enable negative transition to Peripheral Data valid	T <sub>PDV</sub>	—	—	1.0	μs
Delay Time, Enable negative transition to Peripheral Data Valid, CMOS (V <sub>CC</sub> = 30%) PA0-PA7, CA2	T <sub>CMOS</sub>	—	—	2.0	μs
Delay Time, Enable positive transition to CB2 negative transition	T <sub>CB2</sub>	—	—	1.0	μs
Delay Time, Peripheral Data valid to CB2 negative transition	T <sub>DC</sub>	0	—	1.5	μs
Delay Time, Enable positive transition to CB2 positive transition	T <sub>PS1</sub>	—	—	1.0	μs
Rise and Fall Time for CB1 and CB2 input signals	t <sub>r, f</sub>	—	—	1.0	μs
Delay Time, CB1 active transition to CB2 positive transition	T <sub>RS2</sub>	—	—	2.0	μs

Note: Negative sign indicates outward current flow, positive sign indicates inward flow.

D COMPONENTS DESCRIPTIONS  
 D.6 INTEGRATED CIRCUITS

6820 cont'd

FIGURE 1 - READ TIMING CHARACTERISTICS

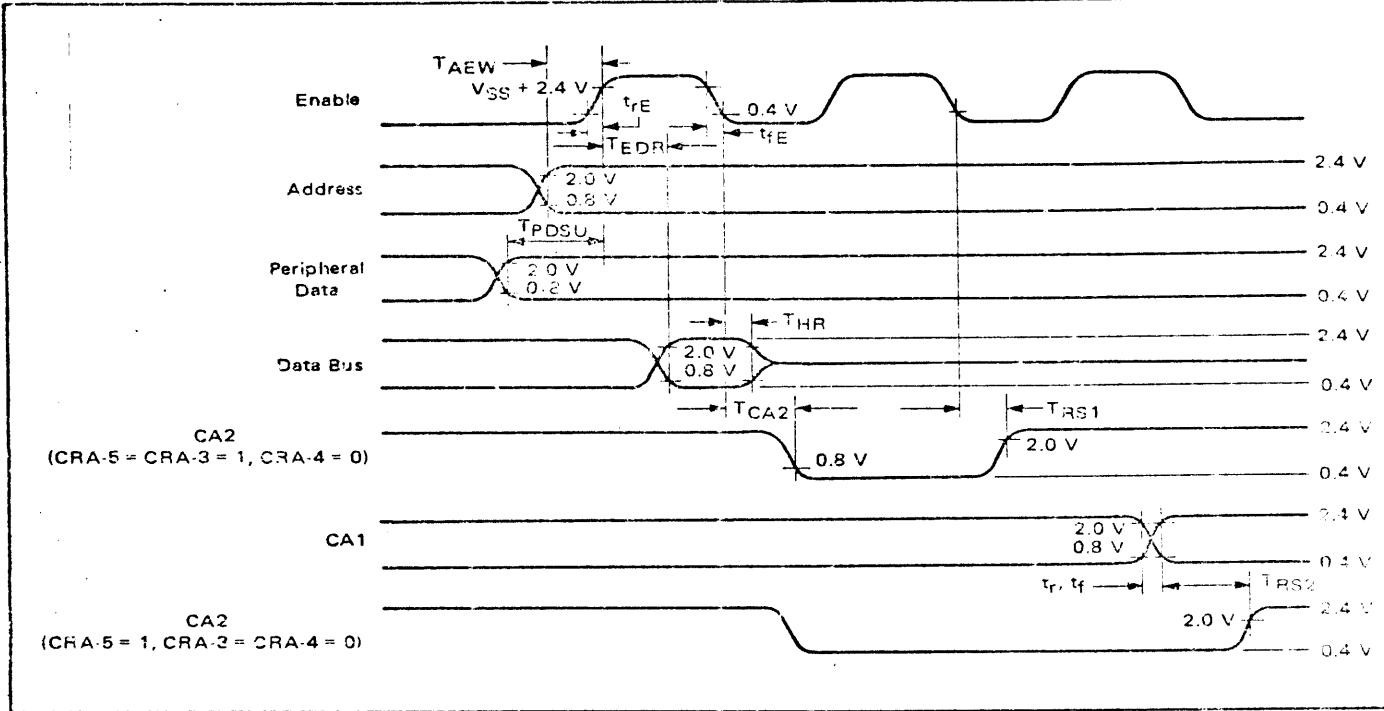
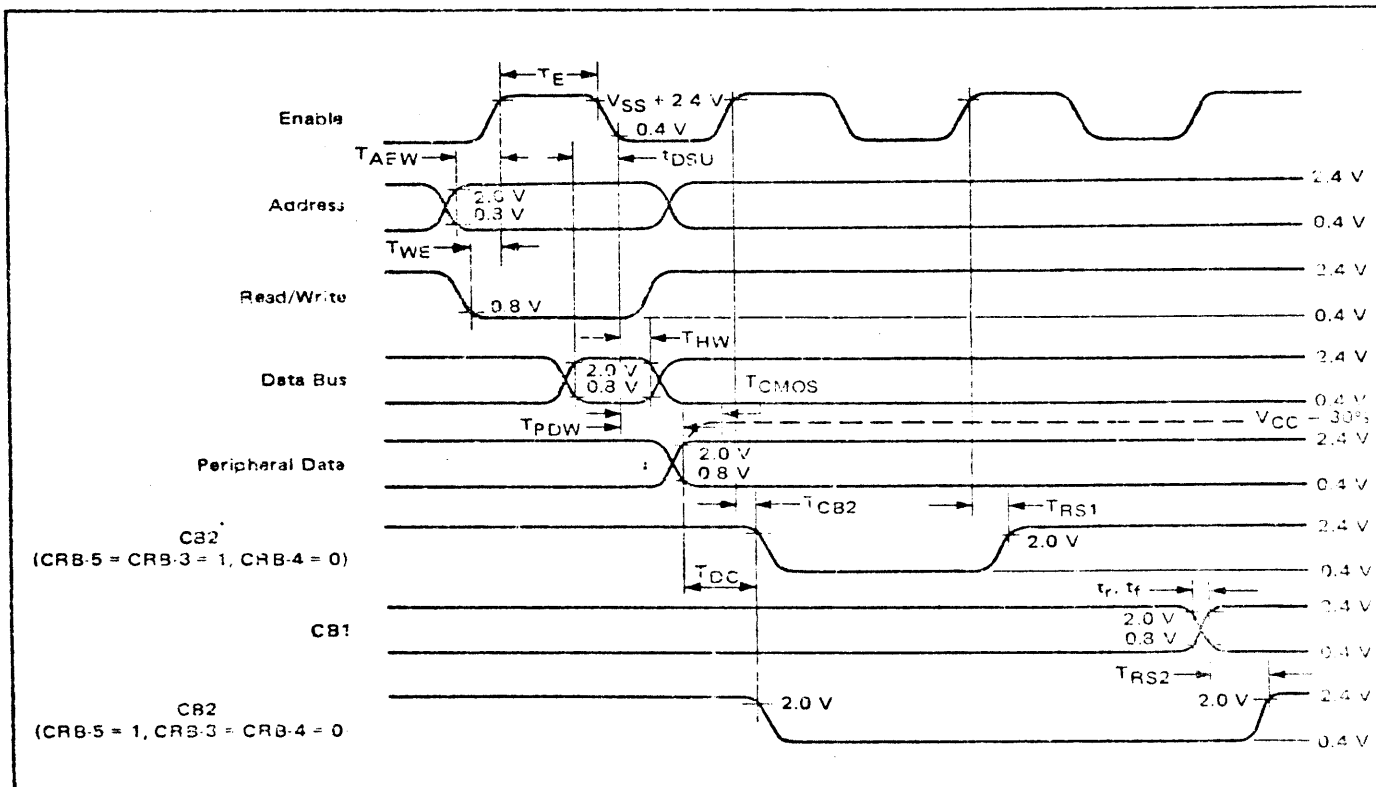
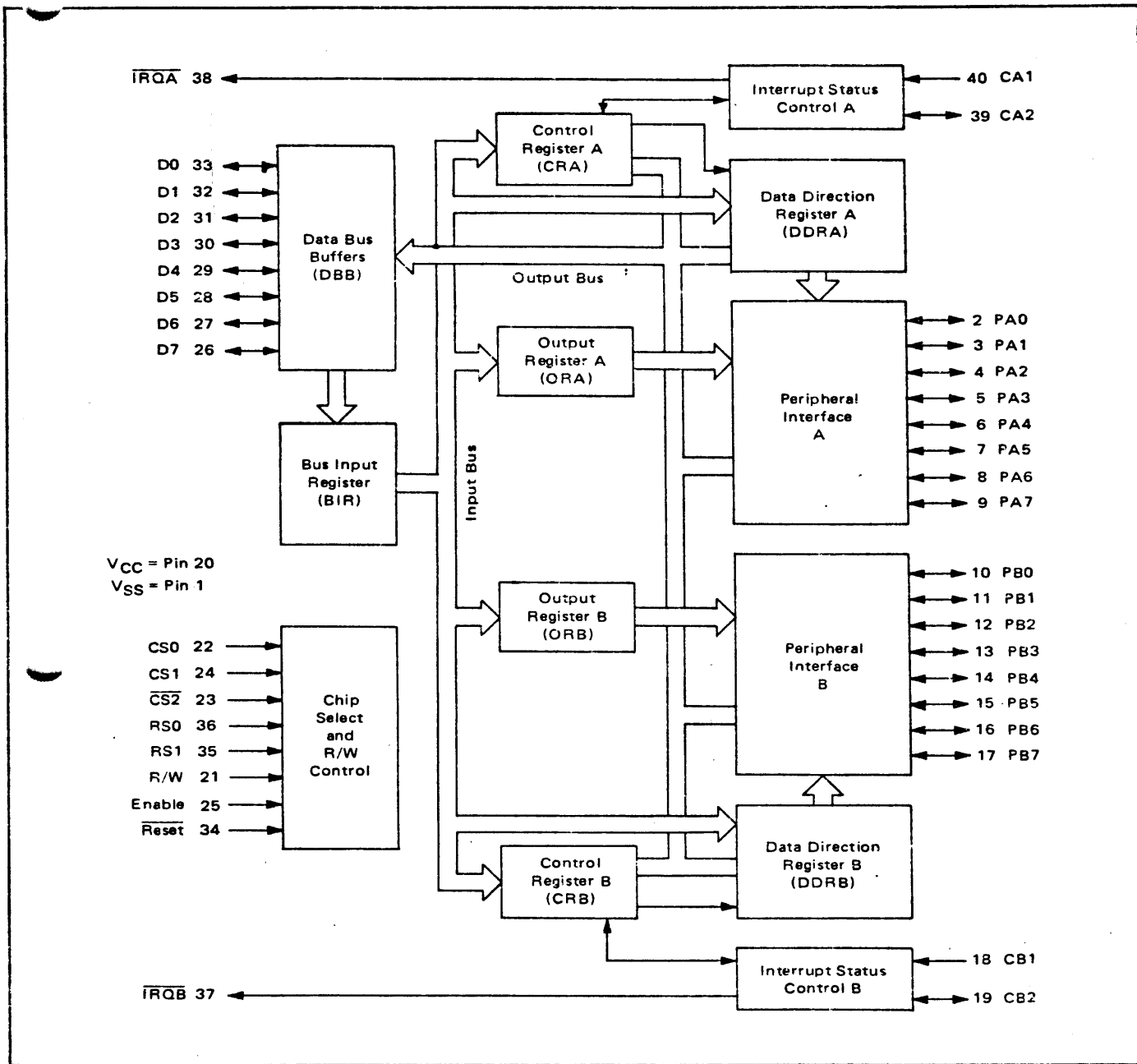


FIGURE 2 - WRITE TIMING CHARACTERISTICS



6820 cont'd.

EXPANDED BLOCK DIAGRAM



PIA INTERFACE SIGNALS FOR MPU

The PIA interfaces to the MC6800 MPU with an eight-bit bi-directional data bus, three chip select lines, two register select lines, two interrupt request lines, read/write line, enable line and reset line. These signals, in conjunction with the MC6800 VMA output, permit the MPU to have complete control over the PIA. VMA may be utilized to gate the input signals to the PIA.

**Bi-Directional Data (D0-D7)** — The bi-directional data lines (D0-D7) allow the transfer of data between the MPU and the PIA. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs a PIA read operation. The

Read/Write line is in the Read (high) state when the PIA is selected for a Read operation.

**PIA Enable (E)** — The enable pulse, E, is the only timing signal that is supplied to the PIA. Timing of all other signals is referenced to the leading and trailing edges of the E pulse. This signal will normally be a derivative of the MC6800  $\phi 2$  Clock.

The E pulse is used to condition the interrupt/control lines CA1, CA2, CB1, and CB2. At least one E pulse must occur from the inactive edge to the active edge of the input signal to set the interrupt flag, when the lines are used as inputs.



D COMPONENTS DESCRIPTIONS  
D.6 INTEGRATED CIRCUITS

6820 cont'd

**PIA Read/Write (RAW)** — This signal is generated by the MPU to control the direction of data transfers on the Data Bus. A low state on the PIA Read/Write line enables the input buffers and data is transferred from the MPU to the PIA on the E signal if the device has been selected. A high on the Read/Write line sets up the PIA for a transfer of data to the bus. The PIA output buffers are enabled when the proper address and the enable pulse E are present.

**Reset** — The active low  $\overline{\text{Reset}}$  line is used to reset all register bits in the PIA to a logical zero (low). This line can be used as a power-on reset and as a master reset during system operation.

**PIA Chip Select (CS0, CS1 and CS2)** — These three input signals are used to select the PIA. CS0 and CS1 must be high and  $\overline{\text{CS2}}$  must be low for selection of the device. Data transfers are then performed under the control of the Enable and Read/Write signals. The chip select lines must be stable for the duration of the E pulse.

**PIA Register Select (RS0 and RS1)** — The two register select lines are used to select the various registers inside the PIA. These two lines are used in conjunction with internal Control Registers to select a particular register

that is to be written or read.

The Register select lines should be stable for the duration of the E pulse while in the read or write cycle.

**Interrupt Request (IROA and IRCB)** — The active low Interrupt Request lines ( $\overline{\text{IROA}}$  and  $\overline{\text{IRCB}}$ ) act to interrupt the MPU either directly or through interrupt priority circuitry. These lines are "open source" (no load device on the chip) and are capable of sinking a current of 1.6 mA from an external source. This permits all interrupt request lines to be tied together in a wire-OR configuration.

Each Interrupt Request line has two internal interrupt flag bits that will cause the Interrupt Request line to go low. Each flag bit is associated with a particular peripheral interrupt line. Also four interrupt enable bits are provided in the PIA which may be used to inhibit a particular interrupt from a peripheral device.

Servicing an interrupt by the MPU may be accomplished by a software routine that, on a prioritized basis, sequentially reads and tests the two control registers in each PIA for interrupt flag bits that are set.

The Interrupt Flag is cleared (zeroed) as a result of an MPU Read Peripheral Data Operation.

## PIA PERIPHERAL INTERFACE LINES

The PIA provides two 8-bit bi-directional data buses and four interrupt/control lines for interfacing to peripheral devices.

**Section A Peripheral Data (PA0-PA7)** — Each of the peripheral data lines can be programmed to act as an input or output. This is accomplished by setting a "1" in the corresponding Data Direction Register bit for those lines which are to be outputs. A "0" in a bit of the Data Direction Register causes the corresponding peripheral data line to act as an input. During an MPU Read Peripheral Data Operation, the data on peripheral lines programmed to act as inputs appears directly on the corresponding MPU Data Bus lines. In the input mode the internal pullup resistor on these lines represents a maximum of one standard TTL load.

The data in Output Register A will appear on the data lines that are programmed to be outputs. A logical "1" written into the register will cause a "high" on the corresponding data line while a "0" results in a "low". Data in Output Register A may be read by an MPU "Read Peripheral Data A" operation when the corresponding lines are programmed as outputs. This data will be read properly if the voltage on the peripheral data lines is greater than 2.0 volts for a logic "1" output and less than 0.8 volt for a logic "0" output. Loading the output lines such that the voltage on these lines does not reach full voltage causes the data transferred into the MPU on a Read operation to differ from that contained in the respective bit of Output Register A.

**Section B Peripheral Data (PB0-PB7)** — The peripheral data lines in the B Section of the PIA can be programmed

to act as either inputs or outputs in a similar manner to PA0-PA7. However, the output buffers driving these lines differ from those driving lines PA0-PA7. They have three-state capability, allowing them to enter a high impedance state when the peripheral data line is used as an input. In addition, data on the peripheral data lines PB0-PB7 will be read properly from those lines programmed as outputs even if the voltages are below 2.0 volts for a "high". As outputs, these lines are compatible with standard TTL and may also be used as a source of up to 1 milliampere at 1.5 volts to directly drive the base of a transistor switch.

**Interrupt Input (CA1 and CB1)** — Peripheral Input lines CA1 and CB1 are input only lines that set the interrupt flags of the control registers. The active transition for these signals is also programmed by the two control registers.

**Peripheral Control (CA2)** — The peripheral control line CA2 can be programmed to act as an interrupt input or as a peripheral control output. As an output, this line is compatible with standard TTL; as an input the internal pullup resistor on this line represents one standard TTL load. The function of this signal line is programmed with Control Register A.

**Peripheral Control (CB2)** — Peripheral Control line CB2 may also be programmed to act as an interrupt input or peripheral control output. As an input, this line has high input impedance and is compatible with standard TTL. As an output it is compatible with standard TTL and may also be used as a source of up to 1 milliampere at 1.5 volts to directly drive the base of a transistor switch. This line is programmed by Control Register B.

6820 cont'd

## INTERNAL CONTROLS

There are six locations within the PIA accessible to the MPU data bus: two Peripheral Registers, two Data Direction Registers, and two Control Registers. Selection of these locations is controlled by the RS0 and RS1 inputs together with bit 2 in the Control Register, as shown in Table 1.

TABLE 1 — INTERNAL ADDRESSING

RS1	RS0	Control Register Bit		Location Selected
		CRA-2	CRB-2	
0	0	1	X	Peripheral Register A
0	0	0	X	Data Direction Register A
0	1	X	X	Control Register A
1	0	X	1	Peripheral Register B
1	0	X	0	Data Direction Register B
1	1	X	X	Control Register B

X = Don't Care

### INITIALIZATION

A low reset line has the effect of zeroing all PIA registers. This will set PA0-PA7, PB0-PB7, CA2 and CB2 as inputs and all interrupts disabled. The PIA must be configured during the restart program which follows the reset.

Details of possible configurations of the Data Direction and Control Register are as follows.

### DATA DIRECTION REGISTERS (DDRA and DDRB)

The two Data Direction Registers allow the MPU to control the direction of data through each corresponding peripheral data line. A Data Direction Register bit set at "0" configures the corresponding peripheral data line as an input; a "1" results in an output.

### CONTROL REGISTERS (CRA and CRB)

The two Control Registers (CRA and CRB) allow the MPU to control the operation of the four peripheral control lines CA1, CA2, CB1 and CB2. In addition they allow the MPU to enable the interrupt lines and monitor the status of the interrupt flags. Bits 0 through 5 of the two registers may be written or read by the MPU when the proper chip select and register select signals are applied. Bits 6 and 7 of the two registers are read only and are modified by external interrupts occurring on control lines CA1, CA2, CB1 or CB2. The format of the control words is shown in Table 2.

TABLE 2 — CONTROL WORD FORMAT

	7	6	5	4	3	2	1	0
CRA	IRQA1	IRQA2	CA2 Control			DDRA Access	CA1 Control	
CRB	IRQB1	IRQB2	CB2 Control			DDRB Access	CB1 Control	

**Data Direction Access Control Bit (CRA-2 and CRB-2) —**  
Bit 2 in each Control register (CRA and CRB) allows selection of either a Peripheral Interface Register or the Data Direction Register when the proper register select signals are applied to RS0 and RS1.

**Interrupt Flags (CRA-6, CRA-7, CRB-6, and CRB-7) —**  
The four interrupt flag bits are set by active transitions of signals on the four Interrupt and Peripheral Status lines when those lines are programmed to be inputs. These bits cannot be set directly from the MPU Data Bus and are reset indirectly by a Read Peripheral Data Operation on the appropriate section.

TABLE 3 — CONTROL OF INTERRUPT INPUTS CA1 AND CB1

CRA-1 (CRB-1)	CRA-0 (CRB-0)	Interrupt Input CA1 (CB1)	Interrupt Flag CRA-7 (CRB-7)	MPU Interrupt Request IRQA (IRQB)
0	0	↓ Active	Set high on ↓ of CA1 (CB1)	Disabled — IRQ remains high
0	1	↓ Active	Set high on ↓ of CA1 (CB1)	Goes low when the interrupt flag bit CRA-7 (CRB-7) goes high
1	0	↑ Active	Set high on ↑ of CA1 (CB1)	Disabled — IRQ remains high
1	1	↑ Active	Set high on ↑ of CA1 (CB1)	Goes low when the interrupt flag bit CRA-7 (CRB-7) goes high

- Notes:
- ↑ indicates positive transition (low to high)
  - ↓ indicates negative transition (high to low)
  - The Interrupt flag bit CRA-7 is cleared by an MPU Read of the A Data Register, and CRB-7 is cleared by an MPU Read of the B Data Register.
  - If CRA-0 (CRB-0) is low when an interrupt occurs (Interrupt disabled) and is later brought high, IRQA (IRQB) occurs on the positive transition of CRA-0 (CRB-0).

D COMPONENTS DESCRIPTIONS  
D.6 INTEGRATED CIRCUITS

6820 cont'd

Control of CA1 and CB1 Interrupt Input Lines (CRA-0, CRB-0, CRA-1, and CRB-1) — The two lowest order bits of the control registers are used to control the interrupt input lines CA1 and CB1. Bits CRA-0 and CRB-0 are

used to enable the MPU interrupt signals IRQA and IRQB, respectively. Bits CRA-1 and CRB-1 determine the active transition of the interrupt input signals CA1 and CB1 (Table 3).

TABLE 4 — CONTROL OF CA2 AND CB2 AS INTERRUPT INPUTS  
CRA5 (CRB5) is low

CRA-5 (CRB-5)	CRA-4 (CRB-4)	CRA-3 (CRB-3)	Interrupt Input CA2 (CB2)	Interrupt Flag CRA-6 (CRB-6)	MPU Interrupt Request IRQA (IRQB)
0	0	0	↓ Active	Set high on ↓ of CA2 (CB2)	Disabled — IRQ remains high
0	0	1	↓ Active	Set high on ↓ of CA2 (CB2)	Goes low when the interrupt flag bit CRA-6 (CRB-6) goes high
0	1	0	↑ Active	Set high on ↑ of CA2 (CB2)	Disabled — IRQ remains high
0	1	1	↑ Active	Set high on ↑ of CA2 (CB2)	Goes low when the interrupt flag bit CRA-6 (CRB-6) goes high

- Notes: 1. ↑ indicates positive transition (low to high)  
2. ↓ indicates negative transition (high to low)  
3. The Interrupt flag bit CRA-6 is cleared by an MPU Read of the A Data Register and CRB-6 is cleared by an MPU Read of the B Data Register.  
4. If CRA-3 (CRB-3) is low when an interrupt occurs (Interrupt disabled) and is later brought high, IRQA (IRQB) occurs on the positive transition of CRA-3 (CRB-3).

TABLE 5 — CONTROL OF CB2 AS AN OUTPUT  
CRB-5 is high

CRB-5	CRB-4	CRB-3	CB2	
			Cleared	Set
1	0	0	Low on the positive transition of the first E pulse following an MPU Write "B" Data Register operation.	High when the interrupt flag bit CRB-7 is set by an active transition of the CB1 signal.
1	0	1	Low on the positive transition of the first E pulse following an MPU Write "B" Data Register operation.	High on the positive transition of the next "E" pulse.
1	1	0	Low when CRB-3 goes low as a result of an MPU Write in Control Register "B".	Always low as long as CRB-3 is low. Will go high on an MPU Write in Control Register "B" that changes CRB-3 to "one".
1	1	1	Always high as long as CRB-3 is high. Will be cleared when an MPU Write Control Register "B" results in clearing CRB-3 to "zero".	High when CRB-3 goes high as a result of an MPU write into control register "B".

D COMPONENTS DESCRIPTIONS  
D.6 INTEGRATED CIRCUITS

6820 cont'd

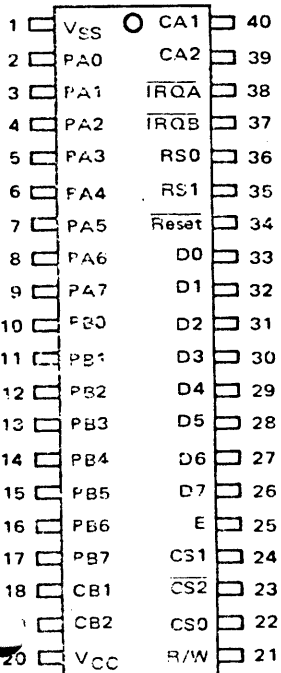
Control of CA2 and CB2 Peripheral Control Lines (CRA-3, CRA-4, CRA-5, CRB-3, CRB-4, and CRB-5) — Bits 3, 4, and 5 of the two control registers are used to control the CA2 and CB2 Peripheral Control lines. These bits determine if the control lines will be an interrupt input or an output control signal. If bit CRA-5 (CRB-5)

is low, CA2 (CB2) is an interrupt input line similar to CA1 (CB1) (Table 4). When CRA-5 (CRB-5) is high, CA2 (CB2) becomes an output signal that may be used to control peripheral data transfers. When in the output mode, CA2 and CB2 have slightly different characteristics (Tables 5 and 6).

TABLE 6 — CONTROL OF CA2 AS AN OUTPUT  
CRA-5 is high:

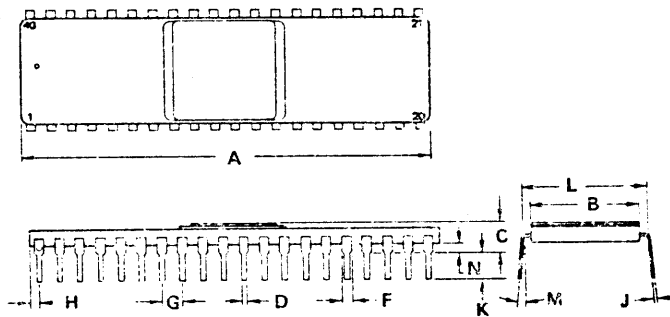
CRA-5	CRA-4	CRA-3	CA2	
			Cleared	Set
1	0	0	Low on negative transition of E after an MPU Read "A" Data operation.	High on an active transition of the CA1 signal.
1	0	1	Low immediately after an MPU Read "A" Data operation.	High on the negative edge of the next "E" pulse.
1	1	0	Low when CRA-3 goes low as a result of an MPU Write in Control Register "A".	Always low as long as CRA-3 is low.
1	1	1	Always high as long as CRA-3 is high.	High when CRA-3 goes high as a result of a Write in Control Register "A".

PIN ASSIGNMENT



PACKAGE DIMENSIONS

CASE 693-04



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	50.04	51.05	1.970	2.010
B	13.78	14.22	0.540	0.560
C	3.05	3.94	0.120	0.155
D	3.05	3.51	0.120	0.138
E	0.28	0.40	0.011	0.016
F	2.54	2.54	0.100	0.100
G	0.25	0.25	0.010	0.010
H	0.25	0.25	0.010	0.010
I	0.25	0.25	0.010	0.010
J	0.25	0.25	0.010	0.010
K	0.25	0.25	0.010	0.010
L	14.86	15.51	0.585	0.610
M	0.25	0.25	0.010	0.010
N	0.51	1.14	0.020	0.045

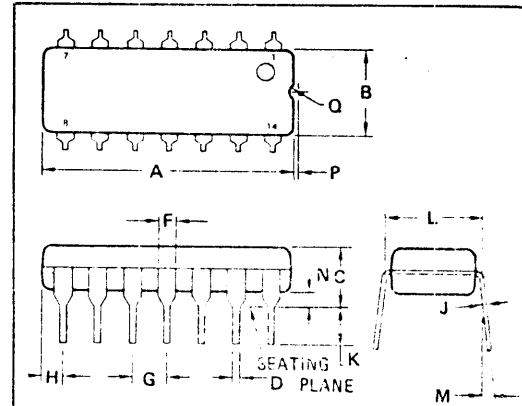
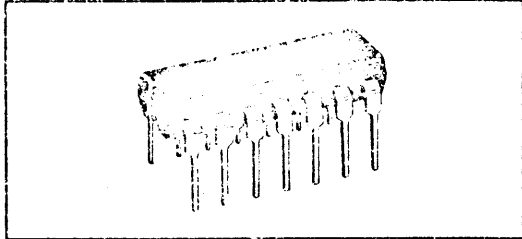
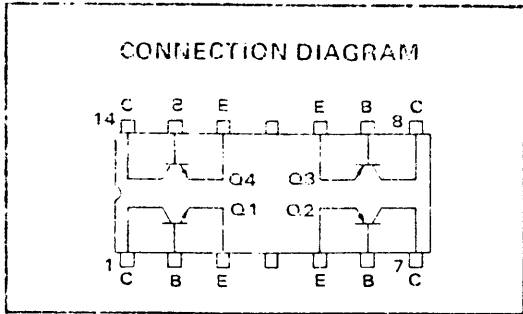
- NOTES:
- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SPATIAL PLANE AT MAXIMUM MATERIAL CONDITION.
  - DIMENSION "L" TO INSIDE OF LEADS (MEASURED 0.51 mm (0.020) BELOW PACKAGE CASE)

D COMPONENT DESCRIPTIONS  
 D.6 INTEGRATED CIRCUITS

6842

**MPU CLOCK BUFFER**

The MPQ6842 is designed to provide the switching speed and saturation voltages necessary in the clock circuit for the  $\phi 1$  and  $\phi 2$  inputs of the MC6800 Microprocessor.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.33	0.51	0.015	0.020
E	1.02	1.52	0.040	0.060
F	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.29	0.30	0.010	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	— 109		— 4.30	
N	0.51	1.02	0.020	0.040
P	0.15	0.2	0.005	0.015
Q	0.51	—	0.020	0.030

**MAXIMUM RATINGS**

Rating	Symbol	Value		Unit
Collector-Emitter Voltage	$V_{CEO}$	30		Vdc
Collector-Base Voltage	$V_{CB}$	30		Vdc
Emitter-Base Voltage	$V_{EB}$	4.0		Vdc
Collector Current - Continuous	$I_C$	200		mA dc
		Each Transistor	Four Transistors Equal Power	
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (1) Derate above $25^\circ\text{C}$	$P_D$	500 4.0	900 7.2	mW mW/°C
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	825 6.7	2400 19.2	mW mW/°C
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-55 to +150		°C

(1) Second Breakdown occurs at power levels greater than 3 times the power dissipation rating.

**THERMAL CHARACTERISTICS**

Characteristic		Junction to Case	Junction to Ambient	Unit
Thermal Resistance	Each Die	151	250	$^\circ\text{C}/\text{W}$
	Effective, 4 Die	37	139	$^\circ\text{C}/\text{W}$
Coupling Factors	Q1-Q4 or Q2-Q3	34	70	%
	Q1-Q2 or Q3-Q4	2.0	26	%

NOTES:  
 1. LEAD WIDTH: 0.13 mm (0.005 IN) PLUS OF TRUE POSITION AT SEATING SURFACE AT MAXIMUM MATERIAL CONDITION.  
 2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

CASE 646  
 PLASTIC PACKAGE

D COMPONENT DESCRIPTIONS  
D.6 INTEGRATED CIRCUITS

6812 cont'd

**THERMAL COUPLING AND EFFECTIVE THERMAL RESISTANCE**

In multiple chip devices, coupling of heat between die occurs. The junction temperature can be calculated as follows:

$$(1) \Delta T_{J1} = R_{\theta 1} P_{D1} + R_{\theta 2} K_{\theta 2} P_{D2} + R_{\theta 3} K_{\theta 3} P_{D3} + R_{\theta 4} K_{\theta 4} P_{D4}$$

Where  $\Delta T_{J1}$  is the change in junction temperature of die 1  
 $R_{\theta 1}$  thru 4 is the thermal resistance of die 1 through 4  
 $P_{D1}$  thru 4 is the power dissipation in die 1 through 4  
 $K_{\theta 2}$  thru 4 is the thermal coupling between die 1 and die 2 through 4.

Assuming equal thermal resistance for each die, equation (1) simplifies to

$$(3) \Delta T_{J1} = R_{\theta 1} (P_{D1} + K_{\theta 2} P_{D2} + K_{\theta 3} P_{D3} + K_{\theta 4} P_{D4})$$

For the conditions where  $P_{D1} = P_{D2} = P_{D3} = P_{D4}$ ,  $P_{DT} = 4P_D$ , equation (3) can be further simplified and by substituting into equation (2) results in

$$(4) R_{\theta}(EFF) = R_{\theta 1} (1 + K_{\theta 2} + K_{\theta 3} + K_{\theta 4}) / 4$$

An effective package thermal resistance can be defined as follows:

$$(2) R_{\theta}(EFF) = \Delta T_{J1} / P_{DT}$$

Where:  $P_{DT}$  is the total package power dissipation.

Values for the coupling factors when either the case or the ambient is used as a reference are given in the table on page 1. If significant power is to be dissipated in two die, die at the opposite ends of the package should be used so that lowest possible junction temperatures will result.

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector-Emitter Breakdown Voltage (1) ( $I_C = 10 \text{ mAdc}$ , $I_B = 0$ )	$BV_{CEO}$	30	—	—	Vdc
Collector-Base Breakdown Voltage ( $I_C = 10 \text{ mAdc}$ , $I_E = 0$ )	$BV_{CBO}$	30	—	—	Vdc
Emitter-Base Breakdown Voltage ( $I_E = 10 \text{ mAdc}$ , $I_C = 0$ )	$BV_{EBO}$	4.0	—	—	Vdc
Collector Cutoff Current ( $V_{CE} = 20 \text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	—	—	50	nAac
Emitter Cutoff Current ( $V_{EB} = 3.0 \text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	—	50	nAac
<b>ON CHARACTERISTICS (1)</b>					
DC Current Gain ( $I_C = 0.5 \text{ mAac}$ , $V_{CE} = 1.0 \text{ Vdc}$ ) ( $I_C = 1.0 \text{ mAac}$ , $V_{CE} = 1.0 \text{ Vdc}$ ) ( $I_C = 10 \text{ mAac}$ , $V_{CE} = 1.0 \text{ Vdc}$ )	$h_{FE}$	30 50 70	— — —	— — —	—
Collector-Emitter Saturation Voltage ( $I_C = 0.5 \text{ mAac}$ , $I_B = 0.05 \text{ mAac}$ , $0^\circ\text{C} \leq T \leq 70^\circ\text{C}$ )	$V_{CE(sat)}$	—	0.05	0.15	Vdc
Base-Emitter Saturation Voltage ( $I_C = 0.5 \text{ mAac}$ , $I_B = 0.05 \text{ mAac}$ )	$V_{BE(sat)}$	—	0.65	0.9	Vdc
<b>DYNAMIC CHARACTERISTICS</b>					
Current Gain — Bandwidth Product (1) ( $I_C = 10 \text{ mAac}$ , $V_{CE} = 20 \text{ Vdc}$ , $f = 100 \text{ MHz}$ )	$f_T$	200	350	—	MHz
Output Capacitance ( $V_{CB} = 5.0 \text{ Vdc}$ , $I_E = 0$ , $f = 100 \text{ kHz}$ )	$C_{ob}$	—	3.0	4.5	pF
Input Capacitance ( $V_{EB} = 0.5 \text{ Vdc}$ , $I_C = 0$ , $f = 100 \text{ kHz}$ )	$C_{ib}$	—	5.0	10	pF
					PNP NPN
			4.0	8.0	
<b>SWITCHING CHARACTERISTICS</b> ( $T_A = 25^\circ\text{C}$ , $V_{CC} = 5.0 \text{ Vdc}$ )					
Propagation Delay Time (50% Points TP1 to TP3) (50% Points TP2 to TP4)	$t_{PLH}$ $t_{PHL}$	— —	15 6.0	25 15	ns
Rise Time (0.3 V to 1.7 V, TP3 or TP4)	$t_r$	5.0	25	35	ns
Fall Time (1.7 V to 0.3 V, TP3 or TP4)	$t_f$	5.0	10	20	ns

(1) Pulse Test. Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

D COMPONENTS DESCRIPTIONS  
 D.6 INTEGRATED CIRCUITS

6842 cont'd

NPN

PNP

FIGURE 1 - DC CURRENT GAIN

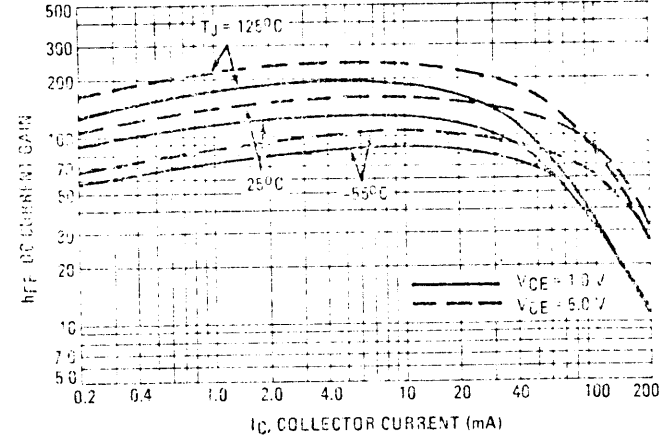
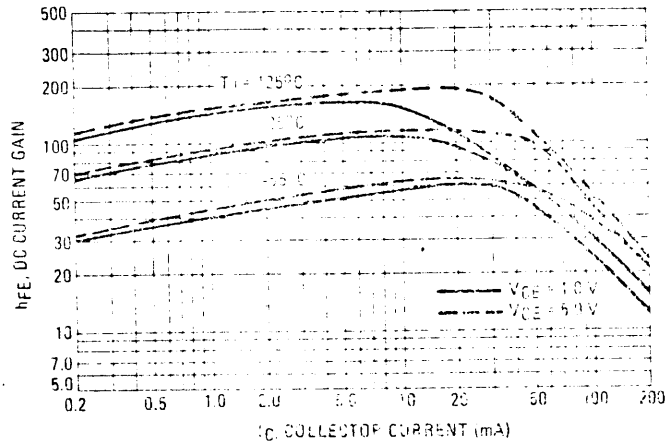


FIGURE 2 - "ON" VOLTAGE

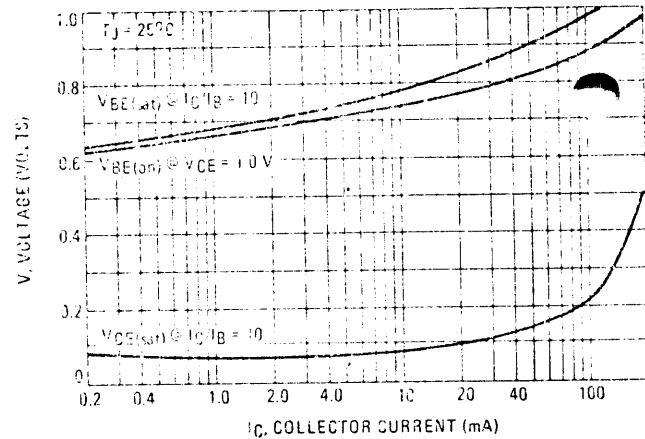
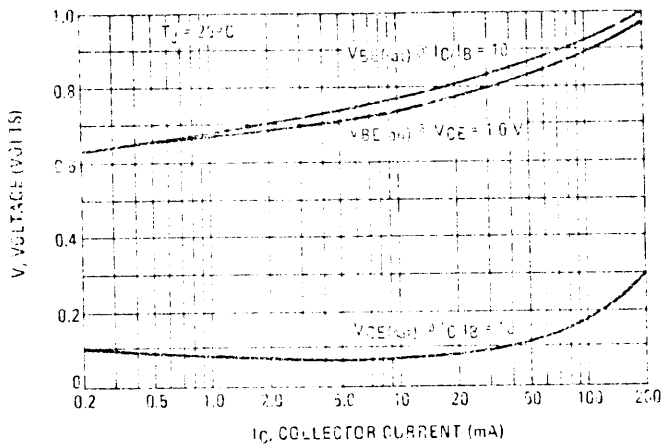
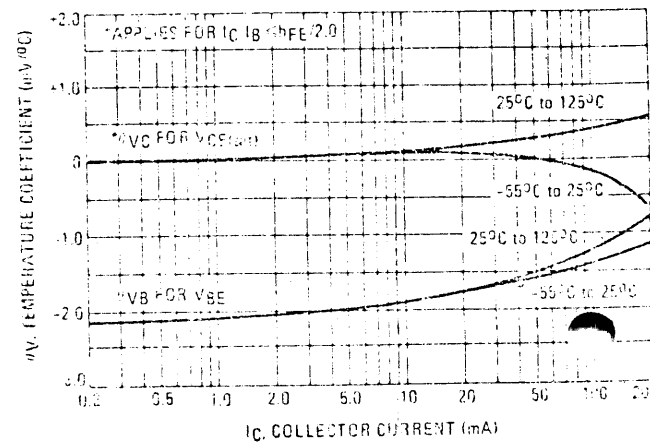
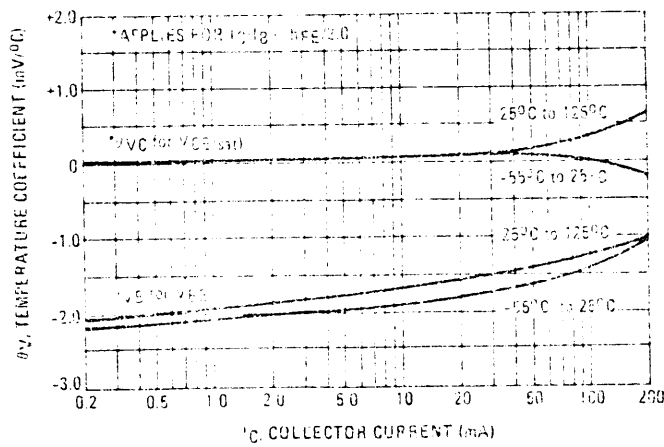


FIGURE 3 - TEMPERATURE COEFFICIENTS



D COMPONENT DESCRIPTIONS  
D.6 INTEGRATED CIRCUITS

6842 cont'd

NPN

PNP

FIGURE 4 - COLLECTOR SATURATION REGION

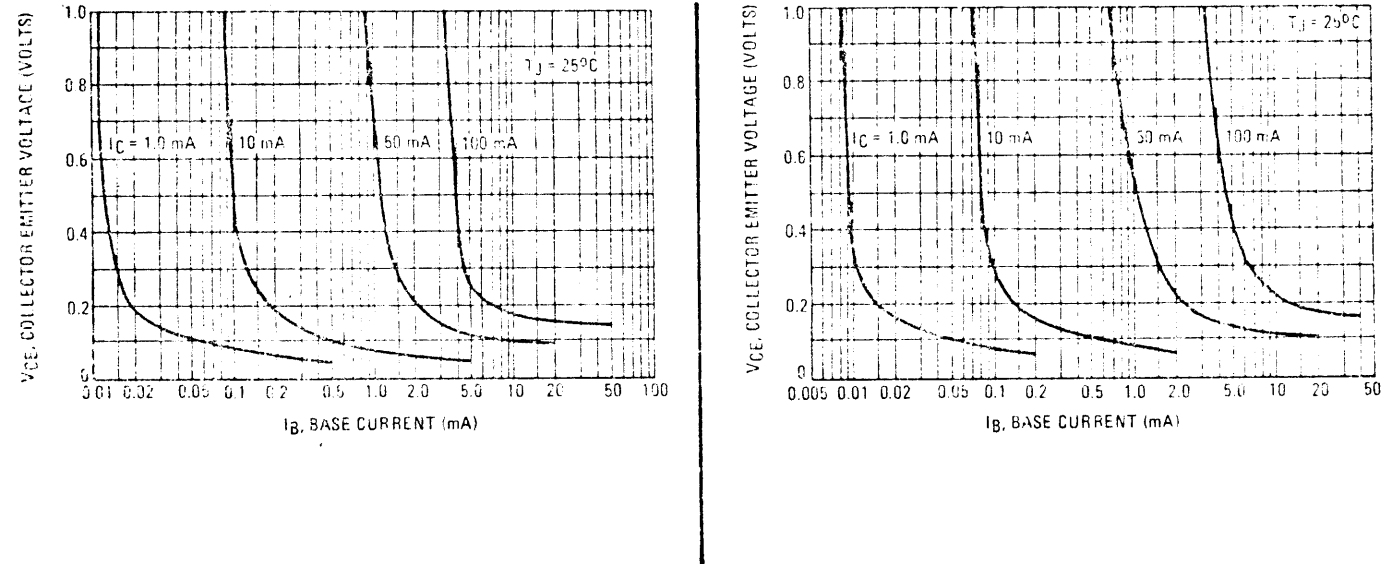
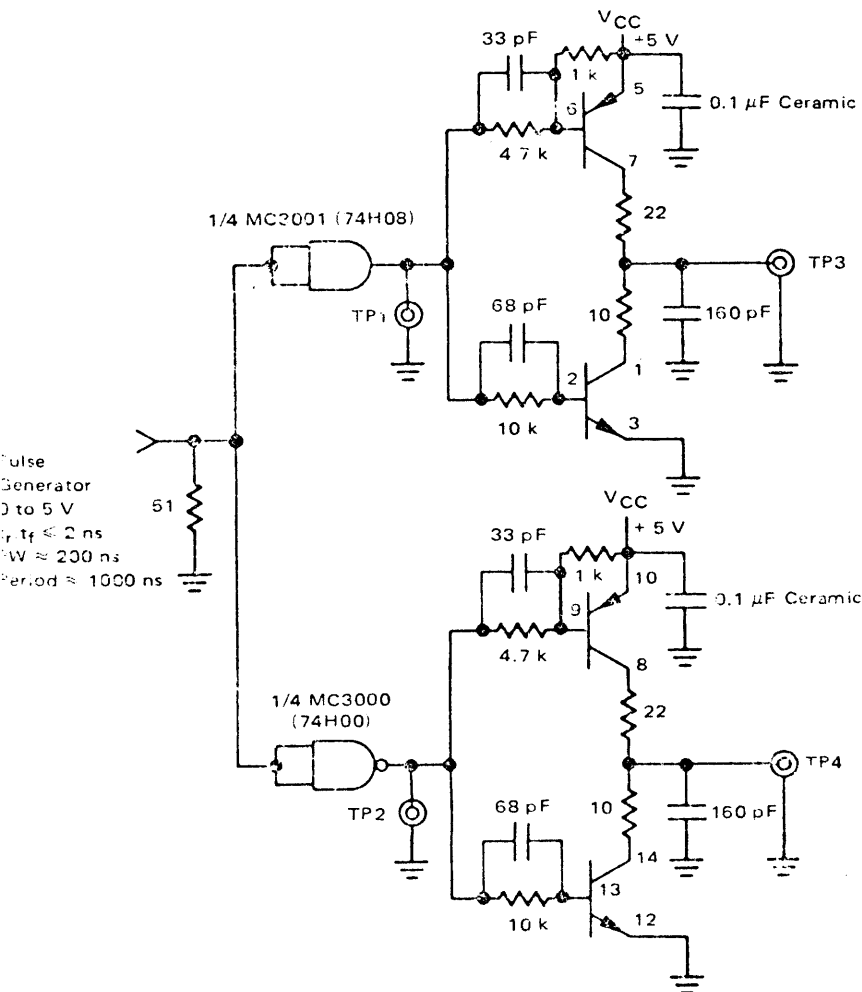
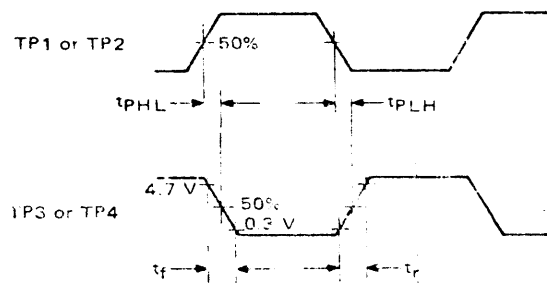


FIGURE 5 - SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



NOTES:

1. Unless otherwise noted, all resistors carbon composition ¼ W ±5%, all capacitors dipped mica ±2%.
2. Use short interconnect wiring with good power and ground buses.
3. TP1 thru TP4 are coaxial connectors to accept scope probe tip and provide a good ground.
4. Device under test is MPO6842.
5. 160 pF load does not include stray or scope probe capacitance.
6. Scope probe resistance > 5 kΩ  
Scope probe capacitance < 10 pF.





6842 cont'd

APPLICATIONS INFORMATION #

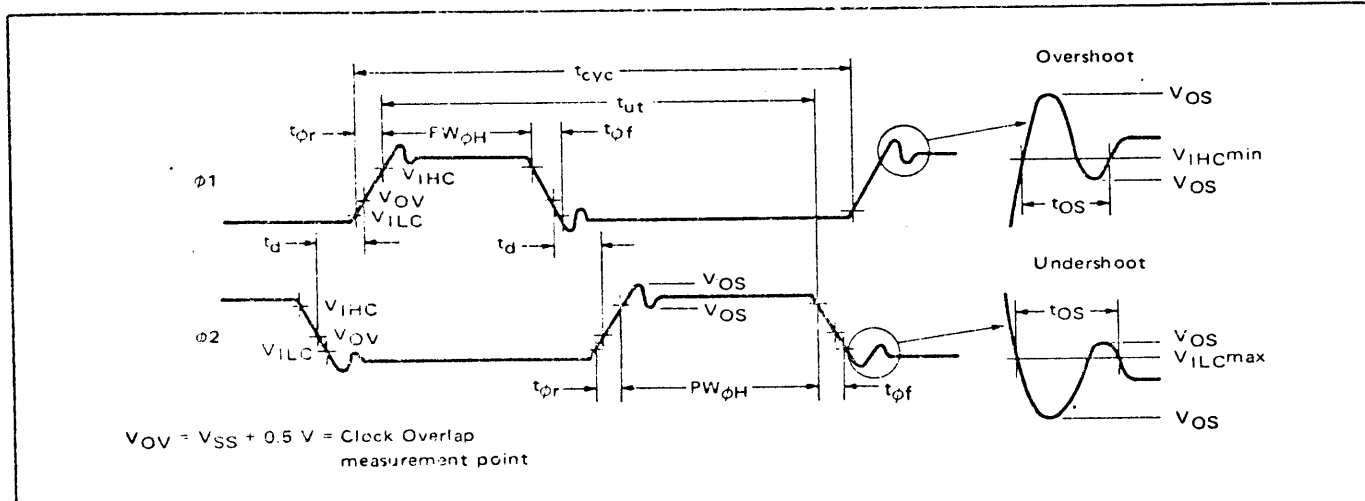
Figure 6 is a summary of the MC6800 Microprocessor clock waveform requirements. The  $\phi 1$  and  $\phi 2$  clock inputs require complementary 1 MHz, 5 volt non-overlapping clocks. The clock inputs of the MPU appear primarily capacitive, being 120 pF typical and 160 pF maximum with 100  $\mu$ Adc leakage. Provision is made in the specification for the undershoot and overshoot that will result from the generation of a high speed transition into a capacitive load.

The clock specifications which constrain the clock driver are the rise and fall times required to meet the pulse widths at the maximum operating frequency of 1 MHz, the non-overlapping requirement, the logic level requirements of  $V_{SS} + 0.3$  volt and  $V_{CC} - 0.3$  volt, the

overshoot specification, and the MPU input capacitance. The clock buffer circuit that drives the MPU clock inputs must be designed to meet the rise and fall time requirements as well as provide the proper logic levels into the load capacitance, within the overshoot constraints. The non-overlapping requirements of the clock signal can be met by the design of the control logic which drives the buffers. The MPQ6842 clock buffer can guarantee the clock designer the speed and saturation voltages necessary to design the clock circuit to meet the MPU clock requirements.

Figure 7 is a circuit designed with TTL logic devices and the MPQ6842 buffer to meet the MPU clock requirements while operating from a single +5 volt supply. The oscillator

FIGURE 6 - MPU CLOCK SPECIFICATION



ELECTRICAL CHARACTERISTICS ( $V_{CC} = 5.0 V \pm 5\%$ ,  $V_{SS} = 0$ ,  $T_A = 0$  to  $70^\circ C$  unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage $\phi 1, \phi 2$	$V_{IHC}$	$V_{CC} - 0.3$	—	$V_{CC} + 0.1$	Vdc
Input Low Voltage $\phi 1, \phi 2$	$V_{ILC}$	$V_{SS} - 0.1$	—	$V_{SS} + 0.3$	Vdc
Clock Overshoot/Undershoot — Input High Level — Input Low Level	$V_{OS}$	$V_{CC} - 0.5$ $V_{SS} - 0.5$	—	$V_{CC} + 0.5$ $V_{SS} + 0.5$	Vdc
Input Leakage Current $\phi 1, \phi 2$ ( $V_{in} = 0$ to $5.25 V$ , $V_{CC} = 0 V$ )	$I_{in}$	—	—	100	$\mu$ Adc
Capacitance* ( $V_{in} = 0$ , $T_A = 25^\circ C$ , $f = 1.0 MHz$ )	$C_{in}$	80	120	160	pF
Frequency of Operation	$f$	0.1	—	1.0	MHz
<b>Clock Timing</b>					
Cycle Time	$t_{cyc}$	1.0	—	10	$\mu$ s
Clock Pulse Width (Measured at $V_{CC} - 0.3 V$ )	$PW_{\phi H}$	430 450	—	4500 4500	ns
Total $\phi 1$ and $\phi 2$ Setup Time	$t_{ut}$	940	—	—	ns
Rise and Fall Times (Measured between $V_{SS} + 0.3 V$ and $V_{CC} - 0.3 V$ )	$t_{\phi r}, t_{\phi f}$	5.0	—	50	ns
Delay Time or Clock Separation (Measured at $V_{OV} = V_{SS} + 0.5 V$ )	$t_d$	0	—	9100	ns
Overshoot Duration	$t_{OS}$	0	—	40	ns

\*Capacitances are periodically sampled rather than 100% tested.

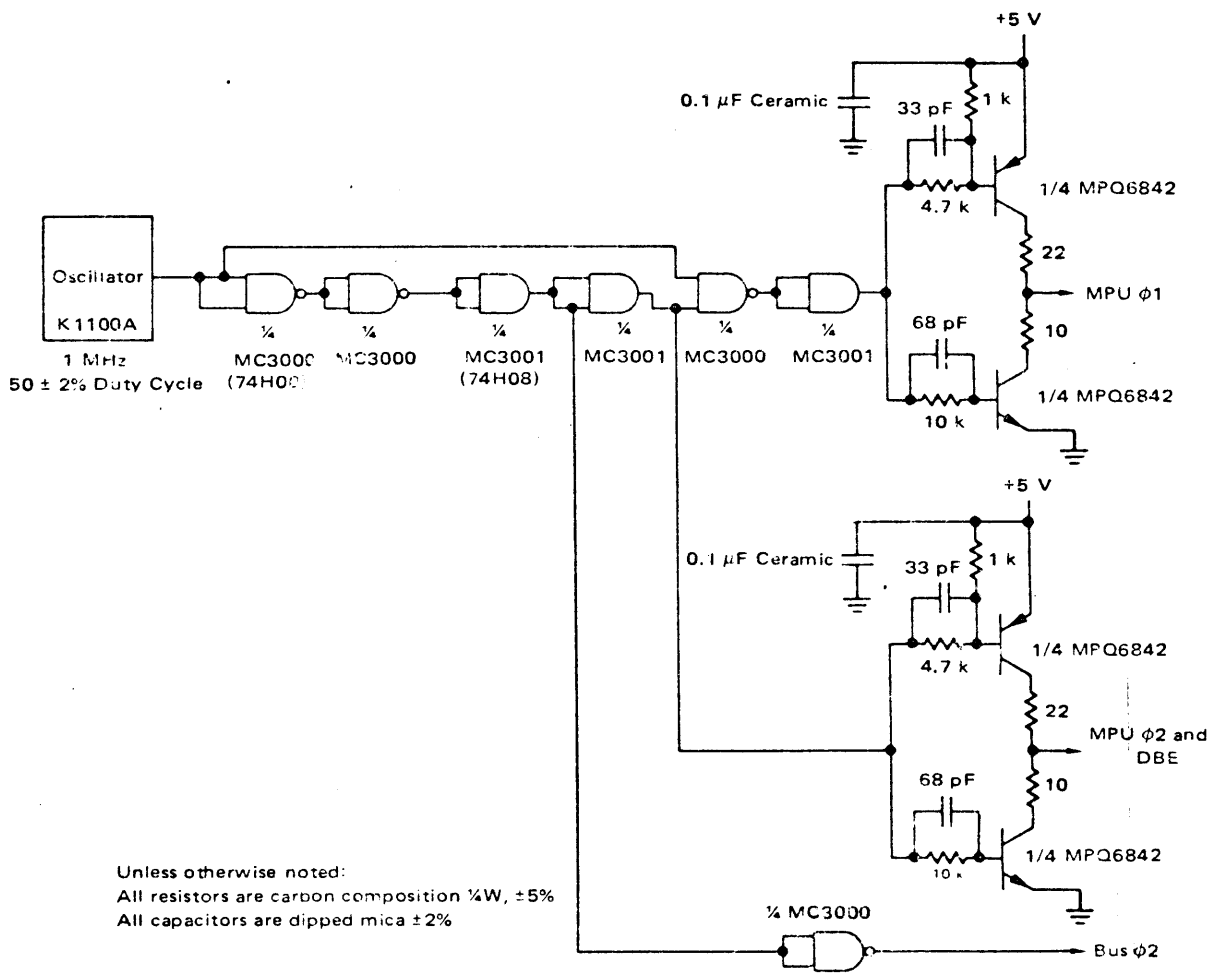
#For further information on MC6800 system usage, refer to the MG800 Applications Manual.

6842 cont'd

can be any source with a maximum frequency of 1 MHz, TTL logic levels and a 50% duty cycle. This oscillator signal source could vary from a commercial oscillator, such as a K1100A available from Motorola's Component Products Department,<sup>1</sup> to a signal derived from a higher frequency signal already available in the system. The TTL gates shown are standard MC3000 and MC3001 (74H00 and 74H08) gates which were chosen for their speed and drive characteristics. The discrete buffers require good "1" level pullup and drive capability which is provided by the MC3001. The circuit was constructed on a wirewrap board and tested on an EXORciser.<sup>2</sup> Good power and ground distribution practice was followed but no special care was taken in parts layout.

Waveforms typical of the circuit in Figure 7 are shown in Figures 8a and 8b, with  $T_A = 20^\circ\text{C}$  and  $V_{CC} = 5.0$  volts. These figures depict the logic levels and pulse widths achieved by this circuitry with  $V_{CC}$  and Ground as reference levels. Figure 8c superimposes the two clock waveforms so that their phase relationship can be seen. Figure 8d shows the phase relationship of Bus  $\phi 2$  and MPU  $\phi 2$ . Figures 8e and 8f examine the non-overlap regions as well as rise and fall times typical of this clock driver circuit. Table 1 presents test data taken over a voltage range of 4.75 volts to 5.25 volts and over a temperature range of  $0^\circ\text{C}$  to  $70^\circ\text{C}$ . Note the stability of these measured parameters, and that the logic levels achieved will provide noise margin on the system clocks.

FIGURE 7 - MPU CLOCK CIRCUIT



1. 2553 N. Edgington, Franklin Park, Illinois 60131, (312) 451-1000.  
2. A prototyping system for the M6800 family.

D COMPONENTS DESCRIPTIONS

D.6 INTEGRATED CIRCUITS

6842 cont'd

Both  $\phi 1$  and  $\phi 2$  clock high times were designed to be 15-30 ns wider than the minimum required by the MPU ( $\phi 1 = 430$  ns,  $\phi 2 = 450$  ns) to provide system margin. Rise and fall times were minimized to provide maximum clock high times consistent with non-critical circuit layout considerations. The overlap margin shown easily meets the MPU requirement of 0 ns at 0.5 volt but will decrease as the capacitive loading increases, as shown in Table 1. The MPU tested for this data had a typical clock input capacitance of 120 pF.

In many systems, especially in the breadboard and evaluation stage, it may be desirable to have the flexibility to vary the system clock to test the effects on data throughput, real time operation with interrupts, or to help diagnose a system timing problem. In those applications, or in those not requiring crystal oscillator stability, an even simpler clock circuit can be used. A pair of cross coupled monostable multivibrators with individual pulse width adjustments can be used as the clock oscillator with the previously described clock buffer circuit. This approach is shown in Figure 9. The non-overlapping clock is generated by the propagation delays through the monostable multivibrators. Figures 10a - 10d show waveforms resulting from this circuit. Table 2 shows test data taken of this

circuit over the voltage and temperature range. Note the small variations in the pulse widths.

The fast rise and fall times produced by this circuitry and the highly capacitive loads require some care in layout to avoid excessive ringing and/or pulse distortion. While no particular care was taken in the construction of the wire-wrap test boards other than placing all of the discrete devices into one header board, the following construction guidelines are recommended. Wide power and ground lines (50-100 mils) should be used to provide low impedance voltage and ground sources. The clock driver should be physically located as near the MPU as possible to avoid ringing down long lines. Close proximity of the clock circuitry to the MPU allows common power and ground connections so that any noise appears common mode rather than differential to the MPU and clock driver. Finally, it is recommended that the MPU  $\phi 2$  clock signal not be used to clock any device other than the MPU so that it is not distributed all over the system with the possibility of picking up noise and causing reflections. The circuits shown provide an additional buffer for the other  $\phi 2$  loads in the system to isolate MPU  $\phi 2$  from all the other  $\phi 2$  loads.

TABLE 1 - PERFORMANCE OF CIRCUIT OF FIGURE 7  
( $C_L = 120$  pF unless otherwise noted.)

Test Conditions	MPU $\phi 1$					MPU $\phi 2$					Non-Overlap Region	
	PW	$t_r$	$t_f$	"1" LL*	"0" LL*	PW	$t_r$	$t_f$	"1" LL*	"0" LL*	$\phi 1 \downarrow$ to $\phi 2 \uparrow$	$\phi 2 \downarrow$ to $\phi 1 \uparrow$
<b>T = 25°C</b>												
$V_{CC} = 4.75$ V	460 ns	15 ns	10 ns	4.75 V	0.1 V	455 ns	15 ns	10.5 ns	4.75 V	0 V	10.5 ns	12 ns
$V_{CC} = 5.00$ V	460	16	11	5.00	0.1	465	16	10	5.00	0	10	11
$V_{CC} = 5.25$ V	460	16	11	5.25	0.1	465	16	11	5.25	0	9.5	10.5
$V_{CC} = 5.00$ V, ( $C_L = 210$ pF)	450	21	15.5	5.00	0.1	460	22	15	5.00	0	2	5.5
<b>T = 70°C</b>												
$V_{CC} = 4.75$ V	460	15	12	4.75	0.1	465	16	12	4.75	0	9	10.5
$V_{CC} = 5.00$ V	450	16	12	5.00	0.1	465	17	12	4.75	0	8.5	10
$V_{CC} = 5.25$ V	455	17	12.5	5.25	0.1	465	17	13	5.25	0	8	9
<b>T = 0°C</b>												
$V_{CC} = 4.75$ V	460	14	10	4.75	0.1	465	15	10.5	4.75	0	11	12
$V_{CC} = 5.00$ V	460	15	10	5.00	0.1	465	15	10	5.00	0	10.5	11.5
$V_{CC} = 5.25$ V	460	15	10.5	5.25	0.1	465	15	10	5.25	0	10	10.5

\*Resolution of this measurement  $\approx \pm 50$  mV

LEGEND:

PW: Pulse width measured at  $V_{CC} - 0.3$  V  
 $t_r$ : Rise time measured from 0.3 V to  $V_{CC} - 0.3$  V  
 $t_f$ : Fall time measured from  $V_{CC} - 0.3$  V to 0.3 V

"0" LL: Zero logic level  
 "1" LL: One logic level  
 Non-Overlap: Measured from 0.5 volt levels

D COMPONENT DESCRIPTIONS  
 D.6 INTEGRATED CIRCUITS

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FIGURE 9 — MONOSTABLE CLOCK GENERATOR

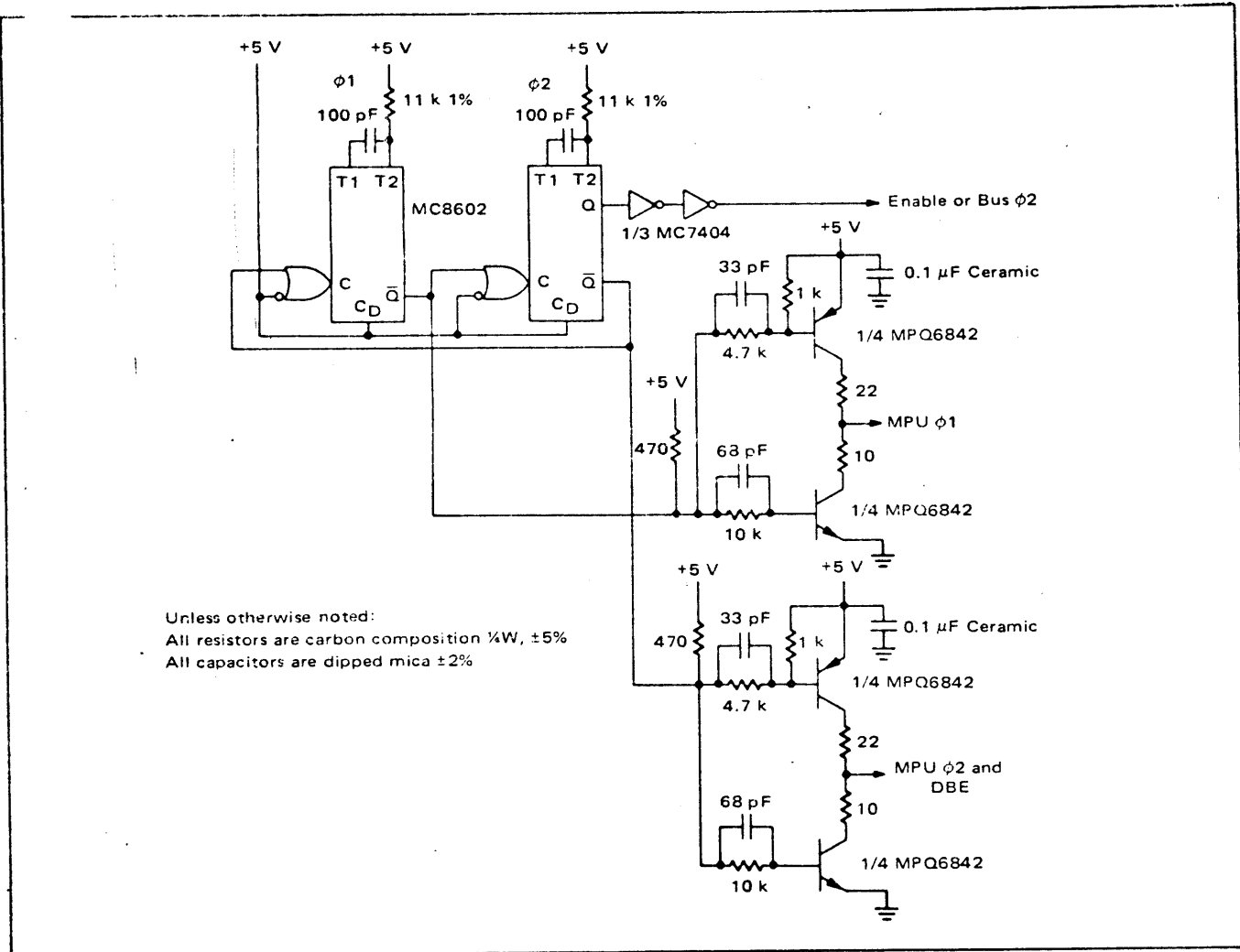


TABLE 2 — PERFORMANCE OF CIRCUIT OF FIGURE 9

Test Conditions	MPU φ1					MPU φ2					Non-Overlap Region	
	PW	t <sub>r</sub>	t <sub>f</sub>	"1" LL*	"0" LL*	PW	t <sub>r</sub>	t <sub>f</sub>	"1" LL*	"0" LL*	φ1↓ to φ2↑	φ2↓ to φ1↑
<b>T = 20°C</b>												
V <sub>CC</sub> = 4.75 V	470 ns	11 ns	11.5 ns	4.75 V	0.1 V	450 ns	12 ns	12 ns	4.75 V	0 V	12 ns	11 ns
V <sub>CC</sub> = 5.00 V	470	12.5	13	5.00	0.1	460	13	12.5	5.00	0	11	9.5
V <sub>CC</sub> = 5.25 V	470	13	12	5.25	0.1	460	13.5	12.5	5.25	0	10	9
<b>T = 70°C</b>												
V <sub>CC</sub> = 4.75 V	455	12.5	13.5	4.75	0.1	450	13	13	4.75	0	11	10
V <sub>CC</sub> = 5.00 V	455	13	14	5.00	0.1	450	14	14	5.00	0	10	9
V <sub>CC</sub> = 5.25 V	455	13	14.5	5.25	0.1	450	14	14	5.25	0	8.5	7
<b>T = 0°C</b>												
V <sub>CC</sub> = 4.75 V	473	12	12	4.75	0.1	470	12	12	4.75	0	11	11
V <sub>CC</sub> = 5.00 V	475	12	12	5.00	0.1	470	12.5	12	5.00	0	9	11
V <sub>CC</sub> = 5.25 V	475	12.5	12.5	5.25	0.05	473	12.5	12	5.25	0	9	8

\*Resolution of this measurement ≈ ±50 mV

LEGEND: PW: Pulse width measured at V<sub>CC</sub> - 0.3 V  
 t<sub>r</sub>: Rise time measured from 0.3 V to V<sub>CC</sub> - 0.3 V  
 t<sub>f</sub>: Fall time measured from V<sub>CC</sub> - 0.3 V to 0.3 V

"0" LL: Zero logic level  
 "1" LL: One logic level  
 Non-Overlap: Measured from 0.5 volt points

D COMPONENT DESCRIPTION  
 D.6 INTEGRATED CIRCUITS

6812 cont'd

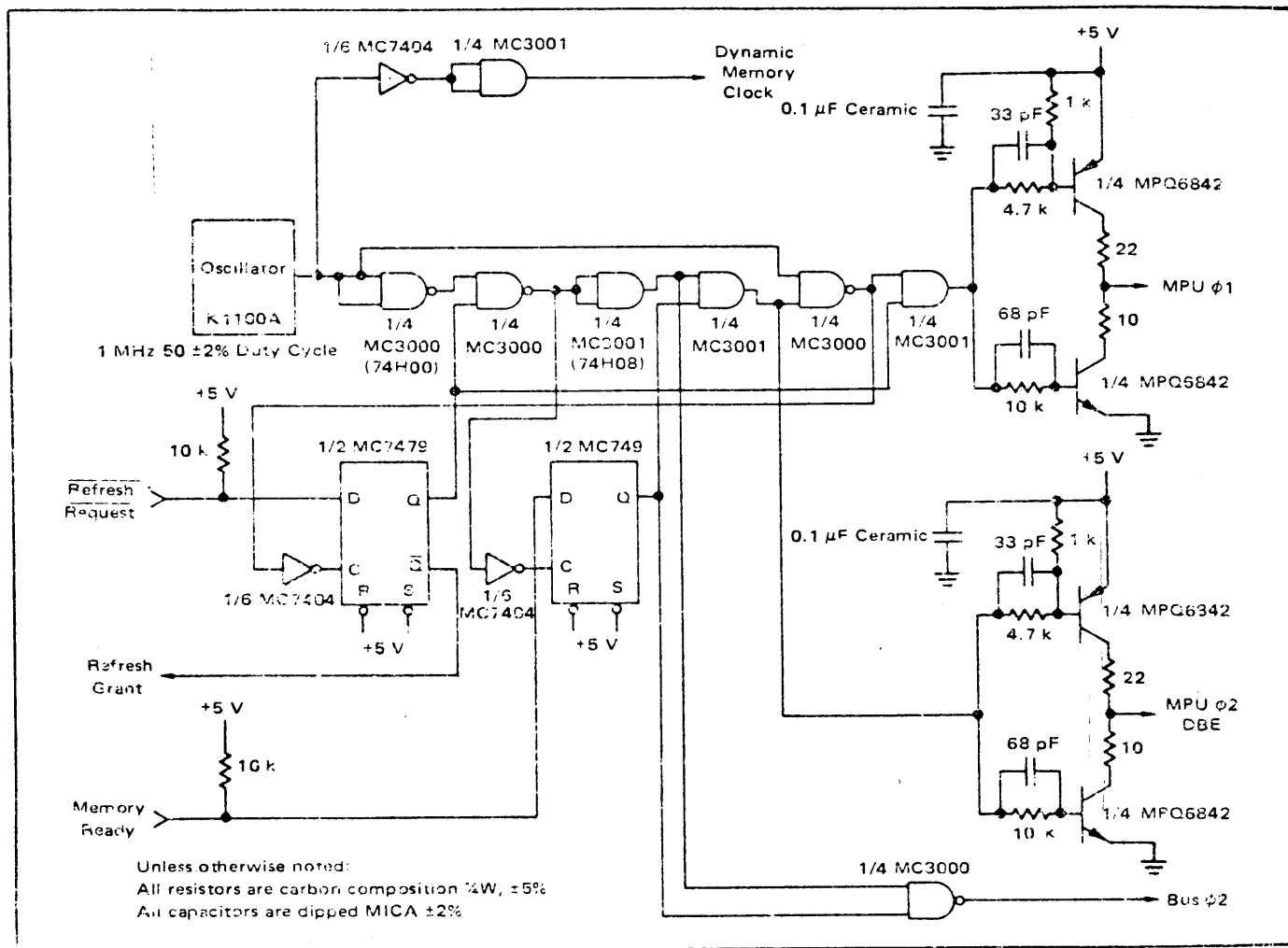
CLOCK CIRCUITRY FOR SLOW AND DYNAMIC MEMORIES

The circuitry to modify the clock signals to interface the MC6800 with dynamic (e.g., MCM6605) and slow memories can be evolved from the clock circuitry described previously. Figure 11 expands the clock circuit of Figure 7 (which has a crystal stabilized source) to include interface signals for dynamic (Refresh Request and Refresh Grant) and slow memories (Memory Ready). Note that the only extra parts required are an MC7479 dual latch, an MC7404 hex inverter, and a pair of 10 k ohm pullup resistors. The state of Refresh Request is sampled during the leading edge of  $\phi_1$  and, if it is low, the  $\phi_1$  and  $\phi_2$  clocks to the MPU are held in the high and low states respectively for at least one full clock cycle. A high Refresh Grant signal is issued to indicate to the dynamic memory system that this cycle is a refresh cycle. Upon receipt of the Refresh Grant signal, the memory system controller sets Refresh Request back high; this is clocked through on the next leading edge of  $\phi_1$ , thereby restoring the system to normal operation. The Memory Ready line is sampled on the leading edge of  $\phi_2$  and, if low, the MPU  $\phi_1$  and  $\phi_2$  clocks are held in the low and high states,

respectively. The clocks will be held in these states until the Memory Ready line is brought high by the slow memory controller, allowing the slow memory controller to determine the amount by which  $\phi_2$  is stretched. Figures 12a and 12b show the effect of Refresh Request and Memory Ready signals on the MPU clocks. Note that the Refresh Request signal is asynchronous with the MPU clocks as it is generated by the refresh oscillator in the dynamic memory controller. Figures 13a and 13b show the phase relationship between MPU  $\phi_2$ , Bus  $\phi_2$  and Dynamic Memory Clock. Note that Bus  $\phi_2$  and MPU  $\phi_2$  are in phase and that the Dynamic Memory Clock leads MPU  $\phi_2$  to help offset delays added by the memory system controller in decoding and level shifting this signal on to the memory array.

The circuit in Figure 14 shows how the Memory Ready capability can be added to the cross-coupled monostable clock generator of Figure 9. The Memory Ready feature is incorporated into this circuit by switching in or out of the  $\phi_2$  pulse width generator an additional timing resistor. By selection of the timing resistors for  $\phi_1$  and  $\phi_2$ , all combinations of  $\phi_1$ ,  $\phi_2$ , and stretched  $\phi_2$  pulse width can be generated.

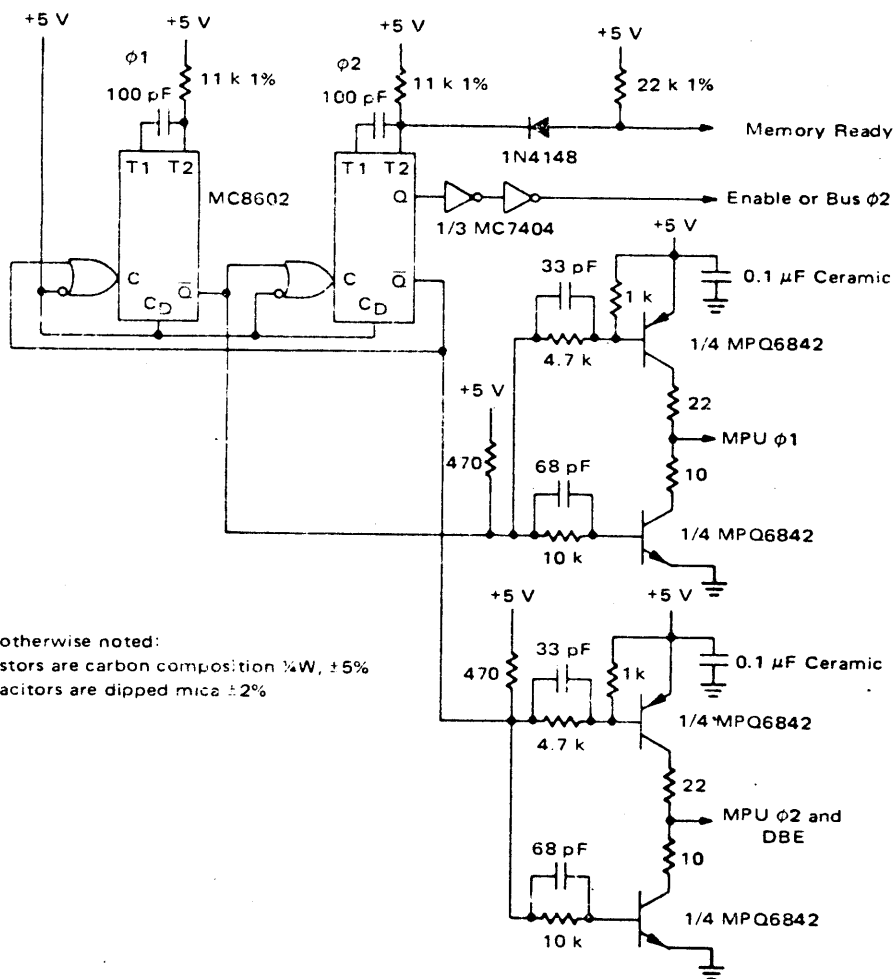
FIGURE 11 — MPU CLOCK CIRCUITRY WITH INTERFACE FOR SLOW AND DYNAMIC MEMORY



D COMPONENT DESCRIPTIONS  
 D.6 INTEGRATED CIRCUITS

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FIGURE 14 - MONOSTABLE CLOCK GENERATOR WITH MEMORY READY



Unless otherwise noted:  
 All resistors are carbon composition  $\frac{1}{4}$ W,  $\pm 5\%$   
 All capacitors are dipped mica  $\pm 2\%$

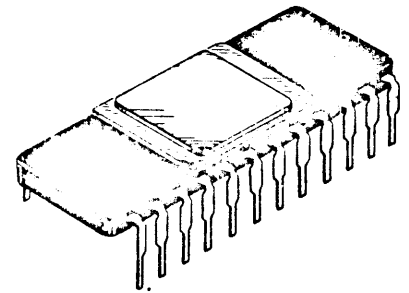
6850

### ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER (ACIA)

The MC6850 Asynchronous Communications Interface Adapter provides the data formatting and control to interface serial asynchronous data communications information to bus organized systems such as the MC6800 Microprocessing Unit.

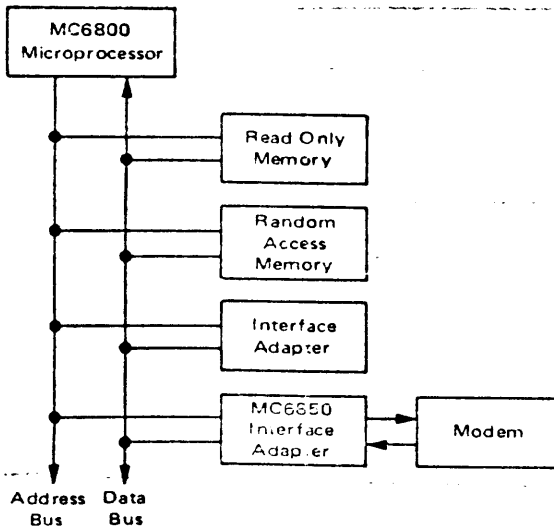
The bus interface of the MC6850 includes select, enable, read/write, interrupt and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. A programmable Control Register provides variable word lengths, clock division ratios, transmit control, receive control, and interrupt control. For peripheral or modem operation three control lines are provided. These lines allow the ACIA to interface directly with the MC6860L 0-600 bps digital modem.

- Eight and Nine-Bit Transmission
- Optional Even and Odd Parity
- Parity, Overrun and Framing Error Checking
- Programmable Control Register
- Optional  $\div 1$ ,  $\div 16$ , and  $\div 64$  Clock Modes
- Up to 500 kbps Transmission
- False Start Bit Deletion
- Peripheral/Modem Control Functions
- Double Buffered
- One or Two Stop Bit Operation

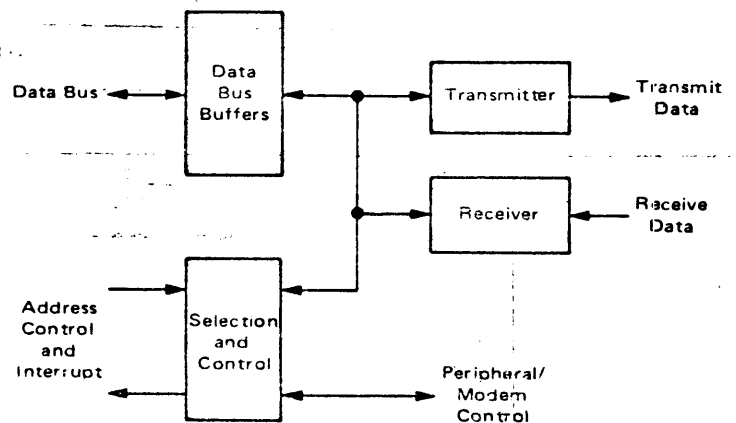


CERAMIC PACKAGE  
CASE 684

M6800 MICROCOMPUTER FAMILY  
BLOCK DIAGRAM



MC6850 ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER  
BLOCK DIAGRAM



D COMPONENT DESCRIPTIONS  
D.6 INTEGRATED CIRCUITS

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V <sub>CC</sub>	-0.3 to +7.0	V <sub>dc</sub>
Input Voltage	V <sub>in</sub>	-0.3 to +7.0	V <sub>dc</sub>
Operating Temperature Range	T <sub>A</sub>	0 to +70	°C
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 5.0 V ± 5%, all voltages referenced to V<sub>SS</sub> = 0, T<sub>A</sub> = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage (Normal Operating Levels)	V <sub>IH</sub>	2.4	—	V <sub>CC</sub>	V <sub>dc</sub>
Input Low Voltage (Normal Operating Levels)	V <sub>IL</sub>	-0.3	—	0.4	V <sub>dc</sub>
Input High Threshold Voltage All Inputs Except Enable	V <sub>IHT</sub>	2.0	—	—	V <sub>dc</sub>
Input Low Threshold Voltage All Inputs Except Enable	V <sub>ILT</sub>	—	—	0.8	V <sub>dc</sub>
Input Leakage Current (V <sub>in</sub> = 0 to 5.25 V <sub>dc</sub> ) R/W, CS0, CS1, $\overline{CS2}$ , Enable	I <sub>in</sub>	—	1.0	2.5	μA <sub>dc</sub>
Three-State (Off State) Input Current (V <sub>in</sub> = 0.4 to 2.4 V <sub>dc</sub> , V <sub>CC</sub> = 5.25 V <sub>dc</sub> ) D0-D7	I <sub>TSI</sub>	—	2.0	10	μA <sub>dc</sub>
Output High Voltage (Load A, I <sub>Load</sub> = -100 μA <sub>dc</sub> , Enable Pulse Width < 25 μs) All Outputs Except $\overline{IRQ}$	V <sub>OH</sub>	2.4	—	—	V <sub>dc</sub>
Output Low Voltage (Load A, I <sub>Load</sub> = 1.6 mA <sub>dc</sub> , except $\overline{IRQ}$ = Load B, Enable Pulse Width < 25 μs)	V <sub>OL</sub>	—	—	0.4	V <sub>dc</sub>
Output Leakage Current (Off State) $\overline{IRQ}$	I <sub>LOH</sub>	—	1.0	10	μA <sub>dc</sub>
Power Dissipation	P <sub>D</sub>	—	300	525	mW
Input Capacitance (V <sub>in</sub> = 0, T <sub>A</sub> = 25°C, f = 1.0 MHz) D0-D7 Tx Clk, Rx Clk, R/W, RS, Rx Data, CS0, CS1, $\overline{CS2}$ , $\overline{CTS}$ , $\overline{DCD}$ Enable	C <sub>in</sub>	—	—	10 7.0 10	pF
Output Capacitance (V <sub>in</sub> = 0, T <sub>A</sub> = 25°C, f = 1.0 MHz)	C <sub>out</sub>	—	—	10	pF
Minimum Clock Pulse Width, Low (Figure 1)	PW <sub>CL</sub>	600	—	—	ns
Minimum Clock Pulse Width, High (Figure 2)	PW <sub>CH</sub>	600	—	—	ns
Clock Frequency ÷ 1 Mode ÷ 16, ÷ 64 Modes	f <sub>C</sub>	—	—	500 800	kHz
Clock-to-Data Delay for Transmitter (Figure 3)	T <sub>TDD</sub>	—	—	1.0	μs
Receive Data Setup Time (Figure 4) ÷ 1 Mode	T <sub>RDSU</sub>	500	—	—	ns
Receive Data Hold Time (Figure 5) ÷ 1 Mode	T <sub>RDH</sub>	500	—	—	ns
Interrupt Request Release Time (Figure 6)	T <sub>IROR</sub>	—	—	1.2	μs
Request-to-Send Delay Time (Figure 6)	T <sub>RTS</sub>	—	—	1.0	μs

BUS TIMING CHARACTERISTICS

READ (Figures 7 and 8)

Characteristic	Symbol	Min	Typ	Max	Unit
Enable Pulse Width	T <sub>E</sub>	0.470	—	25	μs
Setup Time, Address valid to Enable positive transition	T <sub>AEW</sub>	180	—	—	ns
Setup Time, Enable positive transition to Data valid on bus	T <sub>EDR</sub>	—	—	395	ns
Data Bus Hold Time	T <sub>HR</sub>	10	—	—	ns
Rise and Fall Time for Enable input	t <sub>RE</sub> , t <sub>FE</sub>	—	—	25	ns

WRITE (Figures 7 and 9)

Characteristic	Symbol	Min	Typ	Max	Unit
Enable Pulse Width	T <sub>E</sub>	0.470	—	25	μs
Setup Time, Address valid to Enable positive transition	T <sub>AEW</sub>	180	—	—	ns
Setup Time, Data valid to Enable negative transition	T <sub>DSU</sub>	300	—	—	ns
Setup Time, Read/Write negative transition to Enable positive transition	T <sub>WE</sub>	130	—	—	ns
Data Bus Hold Time	T <sub>HW</sub>	10	—	—	ns
Rise and Fall Time for Enable input	t <sub>RE</sub> , t <sub>FE</sub>	—	—	25	ns



D COMPONENT DESCRIPTIONS  
 D.6 INTEGRATED CIRCUITS

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FIGURE 1 – CLOCK PULSE WIDTH, LOW-STATE

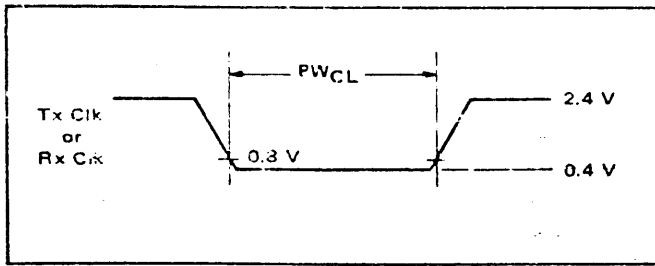


FIGURE 2 – CLOCK PULSE WIDTH, HIGH-STATE

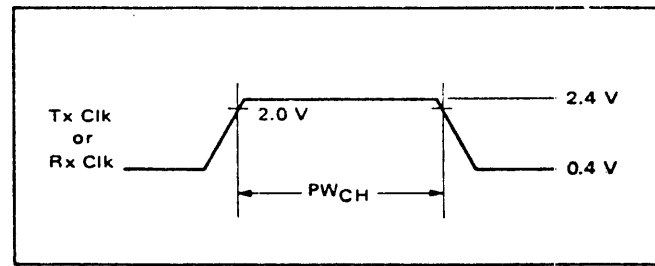


FIGURE 3 – TRANSMIT DATA OUTPUT DELAY

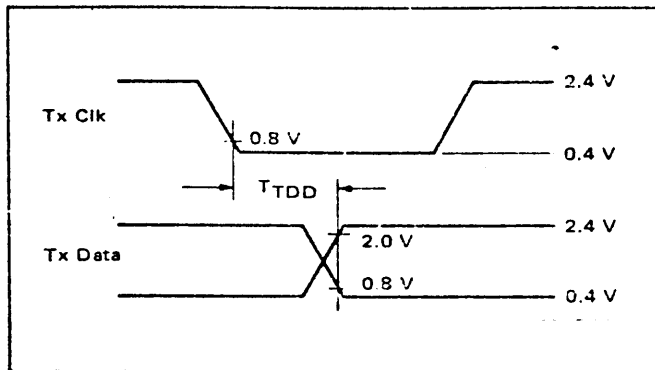


FIGURE 4 – RECEIVE DATA SETUP TIME  
 (±1 Mode)

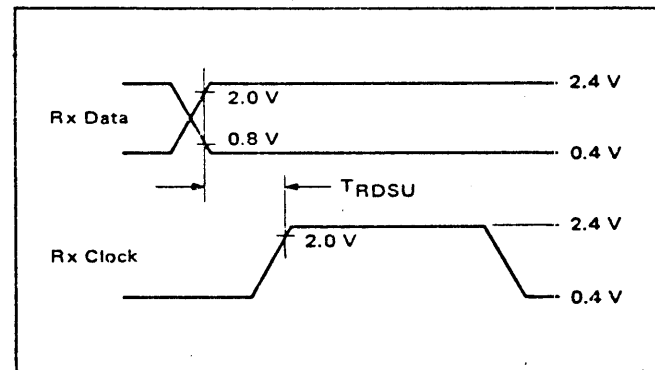


FIGURE 5 – RECEIVE DATA HOLD TIME  
 (±1 Mode)

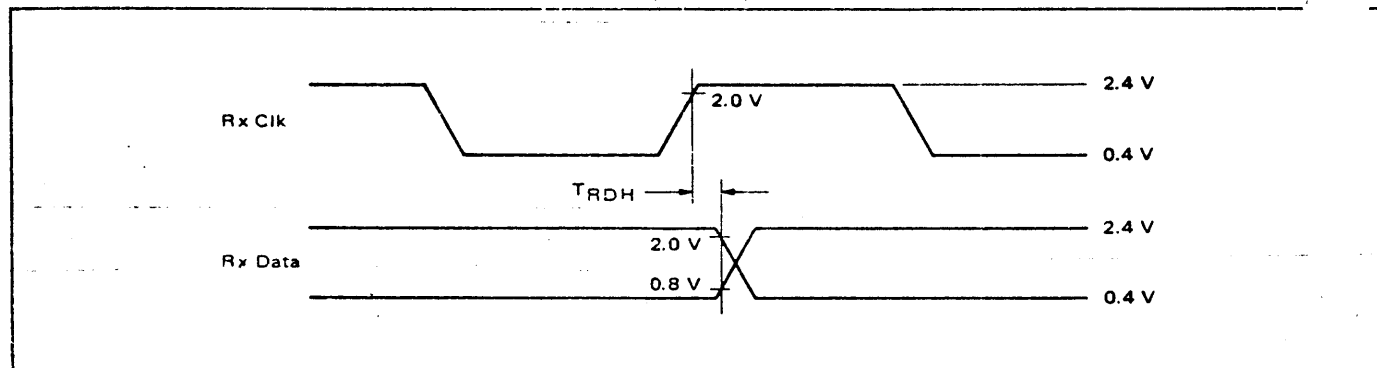
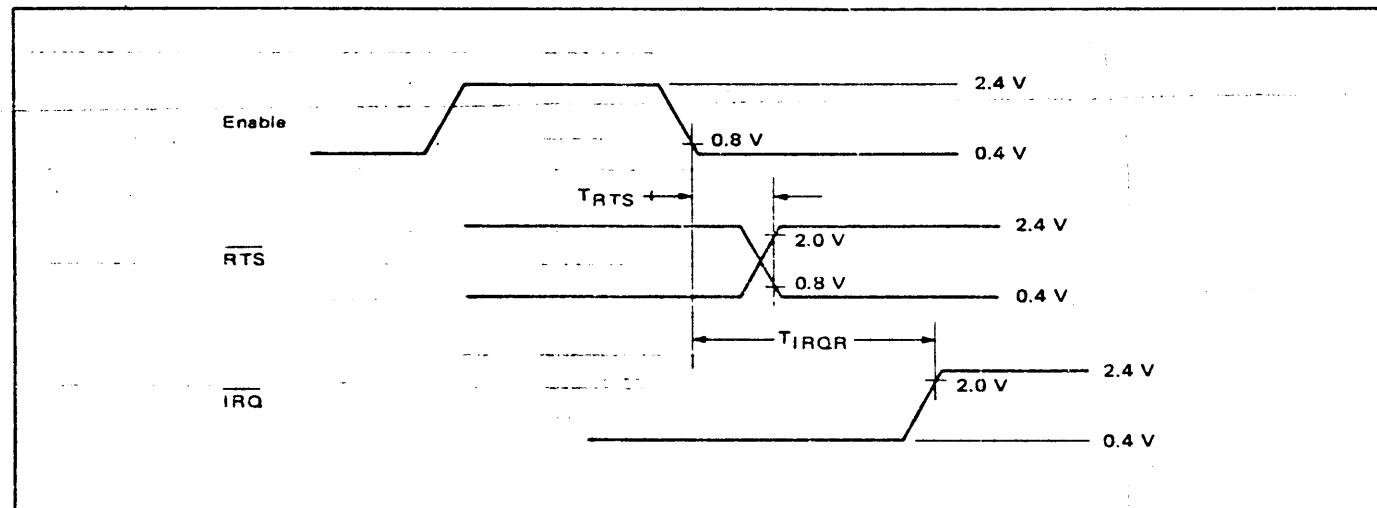


FIGURE 6 – REQUEST-TO-SEND DELAY AND INTERRUPT-REQUEST RELEASE TIMES



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FIGURE 7 - BUS TIMING TEST LOADS

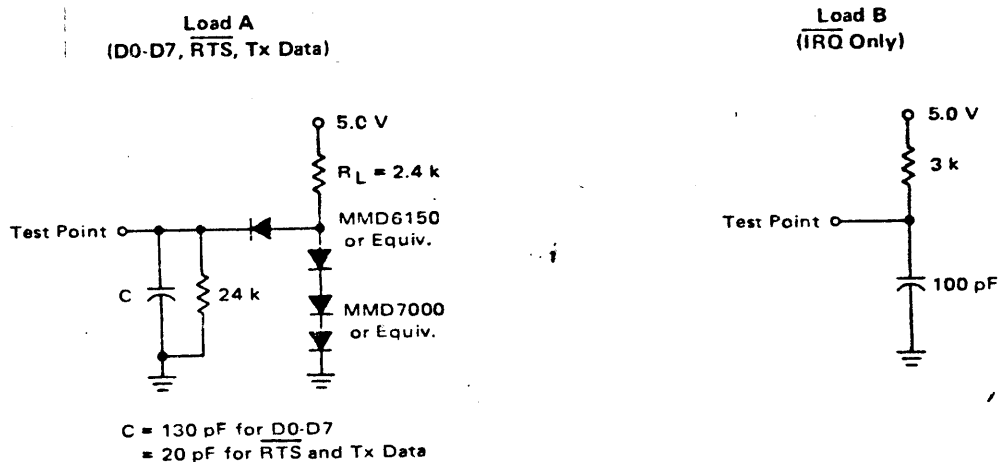


FIGURE 8 - BUS READ TIMING CHARACTERISTICS  
 (Read information from ACIA)

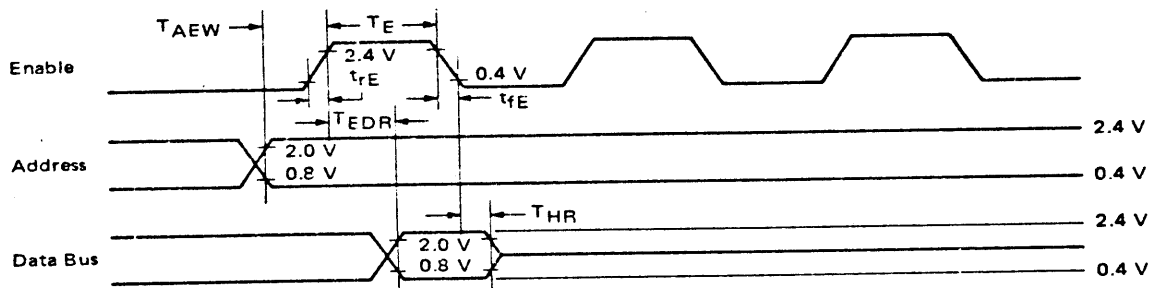
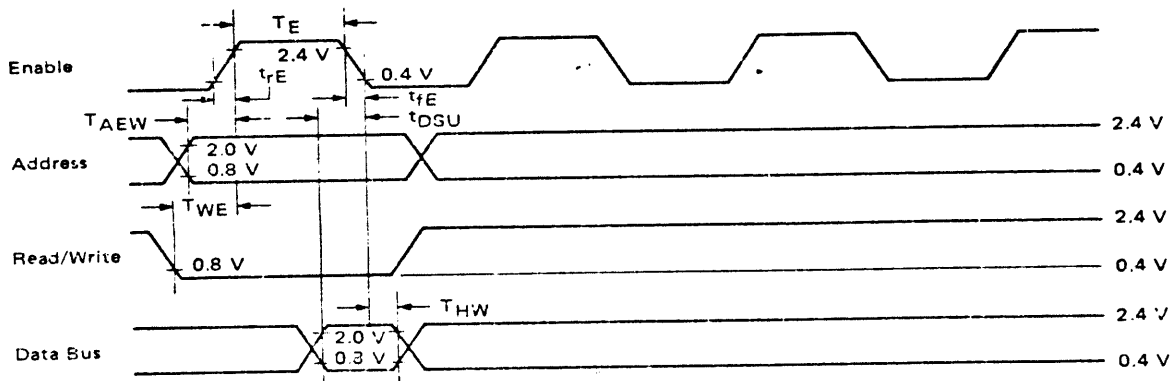
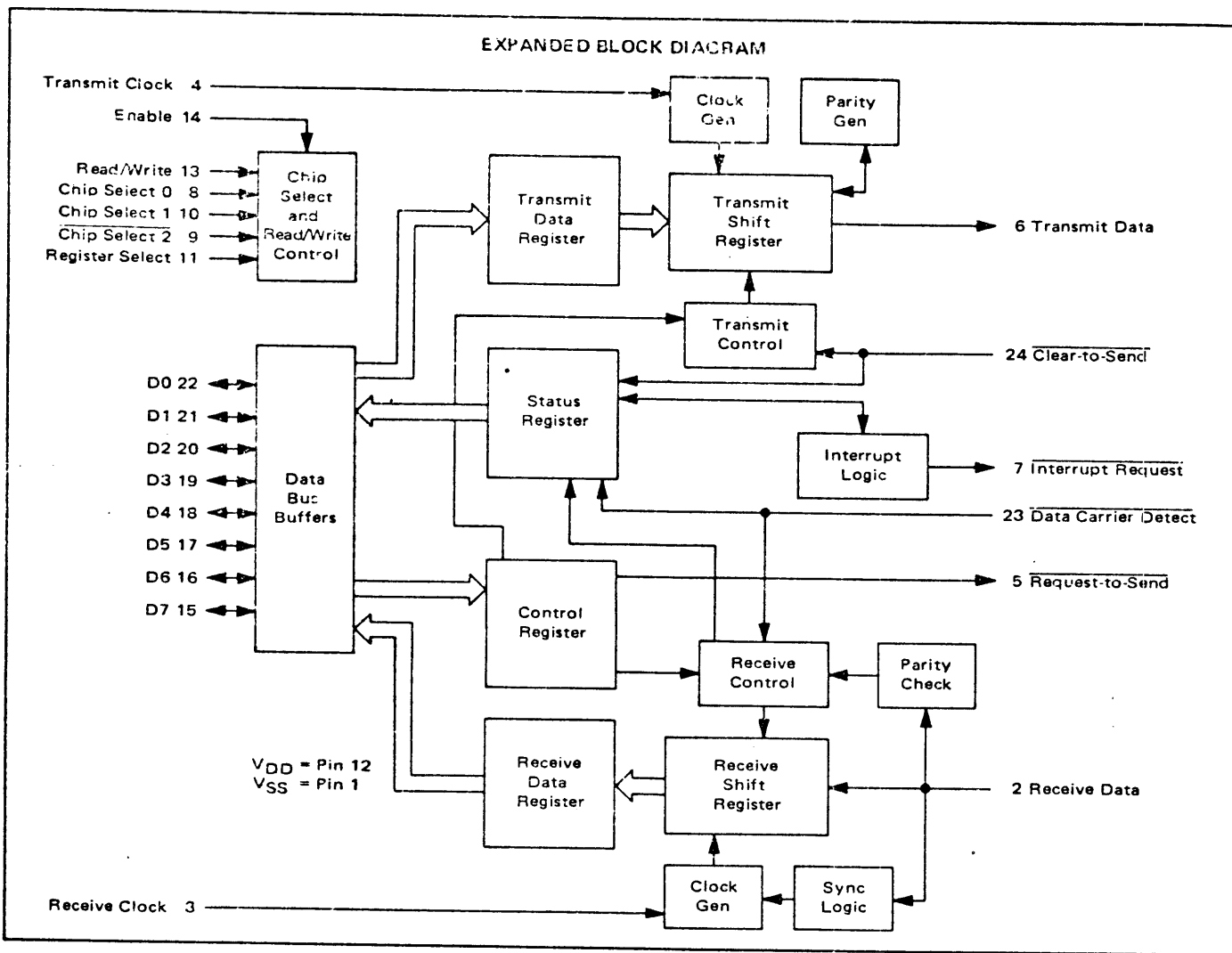


FIGURE 9 - BUS WRITE TIMING CHARACTERISTICS  
 (Write information into ACIA)



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### DEVICE OPERATION

At the bus interface, the ACIA appears as two addressable memory locations. Internally, there are four registers: two read-only and two write-only registers. The read-only registers are Status and Receive Data; the write-only registers are Control and Transmit Data. The serial interface consists of serial input and output lines with independent clocks, and three peripheral/modem control lines.

#### POWER ON/MASTER RESET

The master reset (CR0, CR1) should be set during system initialization to insure the reset condition and prepare for programming the ACIA functional configuration when the communications channel is required. Control bits CR5 and CR6 should also be programmed to define the state of  $\overline{RTS}$  whenever master reset is utilized. The ACIA also contains internal power-on reset logic to detect the power line turn-on transition and hold the chip in a reset state to prevent erroneous output transitions prior to initialization. This circuitry depends on clean power turn-on transitions. The power-on reset is released

by means of the bus-programmed master reset which must be applied prior to operating the ACIA. After master resetting the ACIA, the programmable Control Register can be set for a number of options such as variable clock divider ratios, variable word length, one or two stop bits, parity (even, odd, or none), etc.

#### TRANSMIT

A typical transmitting sequence consists of reading the ACIA Status Register either as a result of an interrupt or in the ACIA's turn in a polling sequence. A character may be written into the Transmit Data Register if the status read operation has indicated that the Transmit Data Register is empty. This character is transferred to a Shift Register where it is serialized and transmitted from the Transmit Data output preceded by a start bit and followed by one or two stop bits. Internal parity (odd or even) can be optionally added to the character and will occur between the last data bit and the first stop bit. After the first character is written in the Data Register,

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the Status Register can be read again to check for a Transmit Data Register Empty condition and current peripheral status. If the register is empty, another character can be loaded for transmission even though the first character is in the process of being transmitted (because of double buffering). The second character will be automatically transferred into the Shift Register when the first character transmission is completed. This sequence continues until all the characters have been transmitted.

## RECEIVE

Data is received from a peripheral by means of the Receive Data input. A divide-by-one clock ratio is provided for an externally synchronized clock (to its data) while the divide-by-16 and 64 ratios are provided for internal synchronization. Bit synchronization in the divide-by-16 and 64 modes is initiated by the detection of the leading mark-to-space transition of the start bit. False start bit deletion capability insures that a full half bit of a start bit has been received before the internal clock is synchronized to the bit time. As a character is being received, parity (odd or even) will be checked and the error indication will be available in the Status Register along with framing error, overrun error, and Receive Data Register full. In a typical-receiving sequence, the Status Register is read to determine if a character has been received from a peripheral. If the Receiver Data Register is full, the character is placed on the 8-bit ACIA bus when a Read Data command is received from the MPU. When parity has been selected for an 8-bit word (7 bits plus parity), the receiver strips the parity bit (D7 = 0) so that data alone is transferred to the MPU. This feature reduces MPU programming. The Status Register can continue to be read again to determine when another character is available in the Receive Data Register. The receiver is also double buffered so that a character can be read from the data register as another character is being received in the shift register. The above sequence continues until all characters have been received.

## INPUT/OUTPUT FUNCTIONS

### ACIA INTERFACE SIGNALS FOR MPU

The ACIA interfaces to the MC6800 MPU with an 8-bit bi-directional data bus, three chip select lines, a register select line, an interrupt request line, read/write line, and enable line. These signals, in conjunction with the MC6800 VMA output, permit the MPU to have complete control over the ACIA.

**ACIA Bi-Directional Data (D0-D7)** — The bi-directional data lines (D0-D7) allow for data transfer between the ACIA and the MPU. The data bus output drivers are three-state devices that remain in the high-impedance (of state except when the MPU performs an ACIA read operation.

**ACIA Enable (E)** — The Enable signal, E, is a high impedance TTL compatible input that enables the bus

input/output data buffers and clocks data to and from the ACIA. This signal will normally be a derivative of the MC6800  $\phi$ 2 Clock.

**Read/Write (R/W)** — The Read/Write line is a high impedance input that is TTL compatible and is used to control the direction of data flow through the ACIA's input/output data bus interface. When Read/Write is high (MPU Read cycle), ACIA output drivers are turned on and a selected register is read. When it is low, the ACIA output drivers are turned off and the MPU writes into a selected register. Therefore, the Read/Write signal is used to select read-only or write-only registers within the ACIA.

**Chip Select (CS0, CS1,  $\overline{CS2}$ )** — These three high impedance TTL compatible input lines are used to address the ACIA. The ACIA is selected when CS0 and CS1 are high and  $\overline{CS2}$  is low. Transfers of data to and from the ACIA are then performed under the control of the Enable signal, Read/Write, and Register Select.

**Register Select (RS)** — The Register Select line is a high impedance input that is TTL compatible. A high level is used to select the Transmit/Receive Data Registers and a low level the Control/Status Registers. The Read/Write signal line is used in conjunction with Register Select to select the read-only or write-only register in each register pair.

**Interrupt Request ( $\overline{IRQ}$ )** — Interrupt Request is a TTL compatible, open-drain (no internal pullup), active low output that is used to interrupt the MPU. The Interrupt Request remains low as long as the cause of the interrupt is present and the appropriate interrupt enable within the ACIA is set.

## CLOCK INPUTS

Separate high impedance TTL compatible inputs are provided for clocking of transmitted and received data. Clock frequencies of 1, 16 or 64 times the data rate may be selected.

**Transmit Clock (Tx Clk)** — The Transmit Clock input is used for the clocking of transmitted data. The transmitter initiates data on the negative transition of the clock.

**Receive Clock (Rx Clk)** — The Receive Clock input is used for synchronization of received data. (In the  $\div 1$  mode, the clock and data must be synchronized externally.) The receiver samples the data on the positive transition of the clock.

## SERIAL INPUT/OUTPUT LINES

**Receive Data (Rx Data)** — The Receive Data line is a high impedance TTL compatible input through which data is received in a serial format. Synchronization with a clock for detection of data is accomplished internally when clock rates of 16 or 64 times the bit rate are used. Data rates are in the range of 0 to 500 kbps when external synchronization is utilized.

**Transmit Data (Tx Data)** — The Transmit Data output line transfers serial data to a modem or other peripheral.

D COMPONENT DESCRIPTIONS  
 D.6 INTEGRATED CIRCUITS

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Data rates are in the range of 0 to 500 kb/s when external synchronization is utilized.

PERIPHERAL/MODEM CONTROL

The ACIA includes several functions that permit limited control of a peripheral or modem. The functions included are Clear-to-Send, Request-to-Send and Data Carrier Detect.

Clear-to-Send (CTS) - This high impedance TTL compatible input provides automatic control of the transmitting end of a communications link via the modem Clear-to-Send active low output by inhibiting the Transmit Data Register Empty (TDRE) status bit.

Request-to-Send (RTS) - The Request-to-Send output enables the MPU to control a peripheral or modem via the data bus. The RTS output corresponds to the state of the Control Register bits CR5 and CR6. When CR6 = 0 or both CR5 and CR6 = 1, the RTS output is low (the active state). This output can also be used for Data Terminal Ready (DTR).

Data Carrier Detect (DCD) - This high impedance TTL compatible input provides automatic control, such as in the receiving end of a communications link by means of a modem Data Carrier Detect output. The DCD input inhibits and initializes the receiver section of the ACIA when high. A low to high transition of the Data Carrier Detect initiates an interrupt to the MPU to indicate the occurrence of a loss of carrier when the Receive Interrupt Enable bit is set.

ACIA REGISTERS

The expanded block diagram for the ACIA indicates the internal registers on the chip that are used for the

status, control, receiving, and transmitting of data. The content of each of the registers is summarized in Table 1.

TRANSMIT DATA REGISTER (TDR)

Data is written in the Transmit Data Register during the negative transition of the enable (E) when the ACIA has been addressed and RS • R/W is selected. Writing data into the register causes the Transmit Data Register Empty bit in the Status Register to go low. Data can then be transmitted. If the transmitter is idling and no character is being transmitted, then the transfer will take place within one bit time of the trailing edge of the Write command. If a character is being transmitted, the new data character will commence as soon as the previous character is complete. The transfer of data causes the Transmit Data Register Empty (TDRE) bit to indicate empty.

RECEIVE DATA REGISTER (RDR)

Data is automatically transferred to the empty Receive Data Register (RDR) from the receiver deserializer (a shift register) upon receiving a complete character. This event causes the Receive Data Register Full (RDRF) in the status buffer to go high (full). Data may then be read through the bus by addressing the ACIA and selecting the Receive Data Register with RS and R/W high when the ACIA is enabled. The non-destructive read cycle causes the RDRF bit to be cleared to empty although the data is retained in the RDR. The status is maintained by RDRF as to whether or not the data is current. When the Receive Data Register is full, the automatic transfer of data from the Receiver Shift Register to the Data

TABLE 1 - DEFINITION OF ACIA REGISTER CONTENTS

Data Bus Line Number	Buffer: Address			
	RS • R/W Transmit Data Register	RS • R/W Receive Data Register	RS • R/W Control Register	RS • R/W Status Register
	(Write Only)	(Read Only)	(Write Only)	(Read Only)
0	Data Bit 0*	Data Bit 0	Counter Divide Select 1 (CR0)	Receive Data Register Full (RDRF)
1	Data Bit 1	Data Bit 1	Counter Divide Select 2 (CR1)	Transmit Data Register Empty (TDRE)
2	Data Bit 2	Data Bit 2	Word Select 1 (CR2)	Data Carrier Detect (DCD)
3	Data Bit 3	Data Bit 3	Word Select 2 (CR3)	Clear to Send (CTS)
4	Data Bit 4	Data Bit 4	Word Select 3 (CR4)	Framing Error (FE)
5	Data Bit 5	Data Bit 5	Transmit Control 1 (CR5)	Receiver Overrun (OVRN)
6	Data Bit 6	Data Bit 6	Transmit Control 2 (CR6)	Parity Error (PE)
7	Data Bit 7***	Data Bit 7**	Receive Interrupt Enable (CR7)	Interrupt Request (IRQ)

\* Leading bit = LSB = Bit 0  
 \*\* Data bit will be zero in 7-bit plus parity modes.  
 \*\*\* Data bit is "don't care" in 7-bit plus parity modes.

D COMPONENT DESCRIPTIONS  
D.6 INTEGRATED CIRCUITS

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Register is inhibited and the RDR contents remain valid with its current status stored in the Status Register.

**CONTROL REGISTER**

The ACIA Control Register consists of eight bits of write-only buffer that are selected when RS and R/W are low. This register controls the function of the receiver, transmitter, interrupt enables, and the Request-to-Send peripheral/modem control output.

**Counter Divide Select Bits (CR0 and CR1)** – The Counter Divide Select Bits (CR0 and CR1) determine the divide ratios utilized in both the transmitter and receiver sections of the ACIA. Additionally, these bits are used to provide a master reset for the ACIA which clears the Status Register (except for external conditions on  $\overline{CTS}$  and  $\overline{DCD}$ ) and initializes both the receiver and transmitter. Master reset does not affect other Control Register bits. Note that after power-on or a power fail/restart, these bits must be set high to reset the ACIA. After resetting, the clock divide ratio may be selected. These counter select bits provide for the following clock divide ratios:

CR1	CR0	Function
0	0	÷ 1
0	1	÷ 16
1	0	÷ 64
1	1	Master Reset

**Word Select Bits (CR2, CR3, and CR4)** – The Word Select bits are used to select word length, parity, and the number of stop bits. The encoding format is as follows:

CR4	CR3	CR2	Function
0	0	0	7 Bits + Even Parity + 2 Stop Bits
0	0	1	7 Bits + Odd Parity + 2 Stop Bits
0	1	0	7 Bits + Even Parity + 1 Stop Bit
0	1	1	7 Bits + Odd Parity + 1 Stop Bit
1	0	0	8 Bits + 2 Stop Bits
1	0	1	8 Bits + 1 Stop Bit
1	1	0	8 Bits + Even Parity + 1 Stop Bit
1	1	1	8 Bits + Odd Parity + 1 Stop Bit

Word length, Parity Select, and Stop Bit changes are not buffered and therefore become effective immediately.

**Transmitter Control Bits (CR5 and CR6)** – Two Transmitter Control bits provide for the control of the interrupt from the Transmit Data Register Empty condition, the Request-to-Send output, and the transmission of a Break level (space). The following encoding format is used:

CR6	CR5	Function
0	0	$\overline{RTS}$ = low, Transmitting Interrupt Disabled.
0	1	$\overline{RTS}$ = low, Transmitting Interrupt Enabled.
1	0	$\overline{RTS}$ = high, Transmitting Interrupt Disabled.
1	1	$\overline{RTS}$ = low, Transmits a Break level on the Transmit Data Output. Transmitting Interrupt Disabled.

**Receive Interrupt Enable Bit (CR7)** – Interrupts will be enabled by a high level in bit position 7 of the Control Register (CR7). Interrupts from the receiver section, Receive Data Register Full being high or by a low to high transition on the Data Carrier Detect signal line, are enabled or disabled by the Receive Interrupt Enable Bit.

**STATUS REGISTER**

Information on the status of the ACIA is available to the MPU by reading the ACIA Status Register. This read-only register is selected when RS is low and R/W is high. Information stored in this register indicates the status of the Transmit Data Register, the Receive Data Register and error logic, and the peripheral/modem status inputs of the ACIA.

**Receive Data Register Full (RDRF), Bit 0** – Receive Data Register Full indicates that received data has been transferred to the Receive Data Register. RDRF is cleared after an MPU read of the Receive Data Register or by a master reset. The cleared or empty state indicates that the contents of the Receive Data Register are not current. Data Carrier Detect being high also causes RDRF to indicate empty.

**Transmit Data Register Empty (TDRE), Bit 1** – The Transmit Data Register Empty bit being set high indicates that the Transmit Data Register contents have been transferred and that new data may be entered. The low state indicates that the register is full and that transmission of a new character has not begun since the last write data command.

**Data Carrier Detect (DCD), Bit 2** – The Data Carrier Detect bit will be high when the  $\overline{DCD}$  input from a modem has gone high to indicate that a carrier is not present. This bit going high causes an Interrupt Request to be generated when the Receive Interrupt Enable is set. It remains high after the  $\overline{DCD}$  input is returned low until cleared by first reading the Status Register and then the Data Register or until a master reset occurs. If the  $\overline{DCD}$  input remains high after read status and read data or master reset have occurred, the  $\overline{DCD}$  status bit remains high and will follow the  $\overline{DCD}$  input.

**Clear-to-Send (CTS), Bit 3** – The Clear-to-Send bit indicates the state of the  $\overline{Clear-to-Send}$  input from a modem. A low  $\overline{CTS}$  indicates that there is a Clear-to-Send from the modem. In the high state, the Transmit Data Register Empty bit is inhibited and the Clear-to-Send status bit will be high. Master reset does not affect the  $\overline{Clear-to-Send}$  Status bit.

**Framing Error (FE), Bit 4** – Framing error indicates that the received character is improperly framed by a start and a stop bit and is detected by the absence of the 1st stop bit. This error indicates a synchronization error, faulty transmission, or a break condition. The framing error flag is set or reset during the receive data transfer time. Therefore, this error indicator is present throughout the time that the associated character is available.

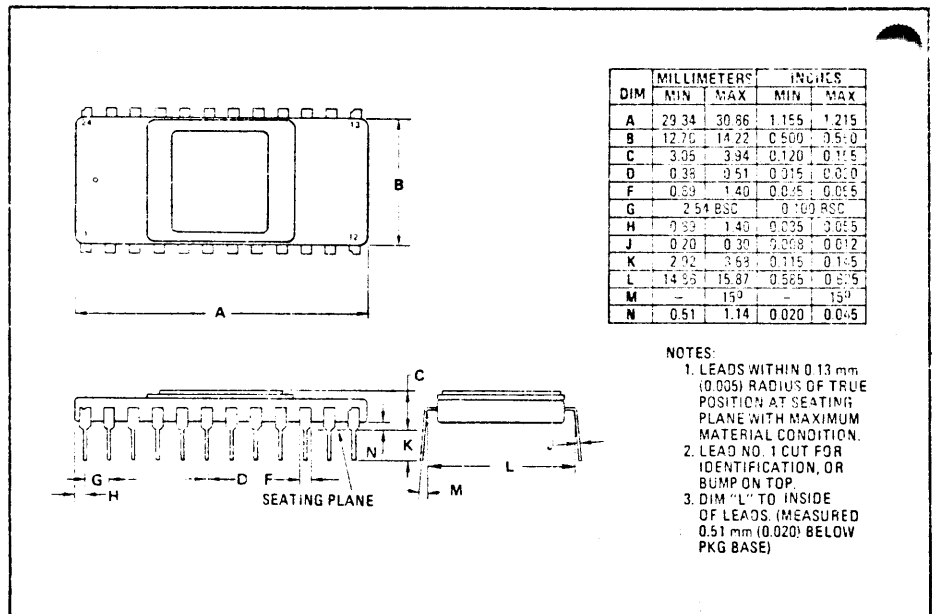
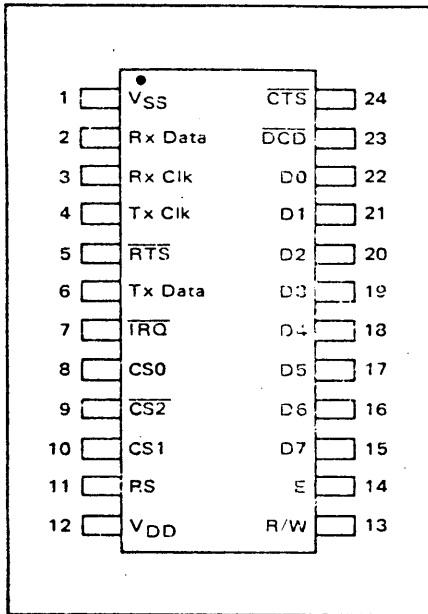
D COMPONENT DESCRIPTIONS  
 D.6 INTEGRATED CIRCUITS

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**Receiver Overrun (OVRN), Bit 5** — Overrun is an error flag that indicates that one or more characters in the data stream were lost. That is, a character or a number of characters were received but not read from the Receive Data Register (RDR) prior to subsequent characters being received. The overrun condition begins at the midpoint of the last bit of the second character received in succession without a read of the RDR having occurred. The Overrun does not occur in the Status Register until the valid character prior to Overrun has been read. The RDRF bit remains set until the Overrun is reset. Character synchronization is maintained during the Overrun condition. The Overrun indication is reset after the reading of data from the Receive Data Register. Overrun is also reset by the Master Reset.

**Parity Error (PE), Bit 6** — The parity error flag indicates that the number of highs (ones) in the character does not agree with the preselected odd or even parity. Odd parity is defined to be when the total number of ones is odd. The parity error indication will be present as long as the data character is in the RDR. If no parity is selected, then both the transmitter parity generator output and the receiver parity check results are inhibited.

**Interrupt Request (IRQ), Bit 7** — The IRQ bit indicates the state of the  $\overline{IRQ}$  output. Any interrupt condition with its applicable enable will be indicated in this status bit. Anytime the  $\overline{IRQ}$  output is low the IRQ bit will be high to indicate the interrupt or service request status.



6060

### 0-600 bps DIGITAL MODEM

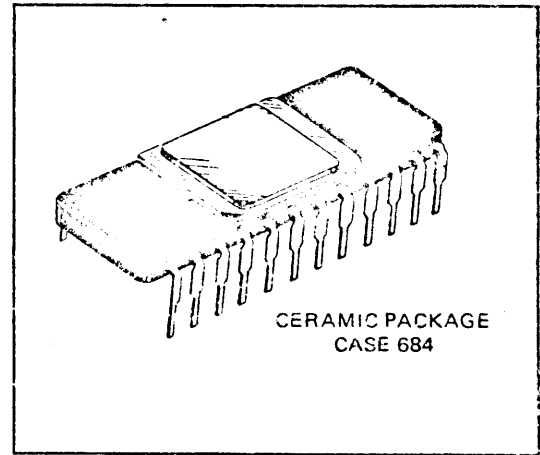
The MC6860 is a MOS subsystem designed to be integrated into a wide range of equipment utilizing serial data communications.

The modem provides the necessary modulation, demodulation and supervisory control functions to implement a serial data communications link, over a voice grade channel, utilizing frequency shift keying (FSK) at bit rates up to 600 bps. The MC6860 can be implemented into a wide range of data handling systems, including stand alone modems, data storage devices, remote data communication terminals and I/O interfaces for minicomputers.

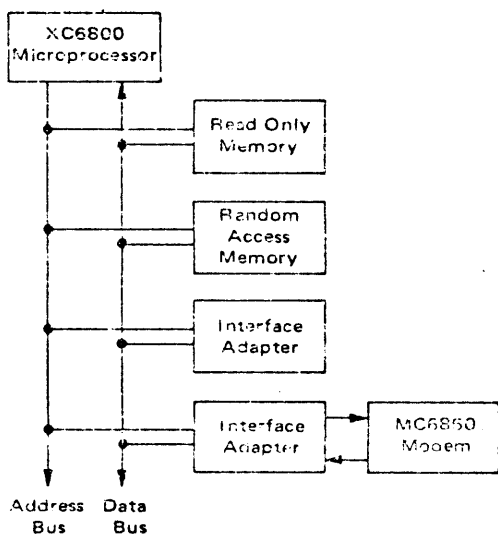
N-channel silicon gate technology permits the MC6860 to operate using a single voltage supply and be fully TTL compatible.

The modem is compatible with the M6800 microcomputer family, interfacing directly with the Asynchronous Communications Interface Adapter to provide low-speed data communications capability.

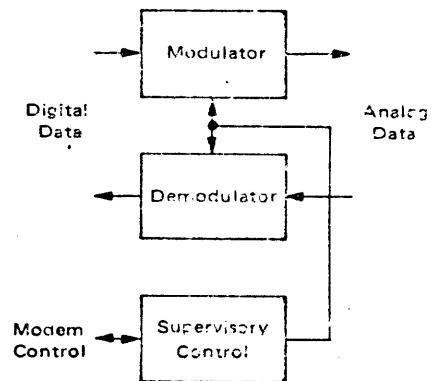
- Originate and Answer Mode
- Crystal or External Reference Control
- Modem Self Test
- Terminal Interfaces TTL-Compatible
- Full-Duplex or Half-Duplex Operation
- Automatic Answer and Disconnect
- Compatible Functions for 100 Series Data Sets
- Compatible Functions for 1001A/B Data Couplers



M6800 MICROCOMPUTER FAMILY  
 BLOCK DIAGRAM



MC6860 DIGITAL MODEM  
 BLOCK DIAGRAM





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MAXIMUM RATINGS (Voltages referenced to  $V_{SS}$ , Pin 1)

Rating	Symbol	Value	Unit
Supply Voltage	$V_{DD}$	-0.3 to +7.0	Vdc
Data Input Voltage	$V_{in}$	-0.5 to +7.0	Vdc
Operating Temperature Range	$T_A$	0 to +70	$^{\circ}C$
Storage Temperature Range	$T_{stg}$	-55 to +150	$^{\circ}C$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

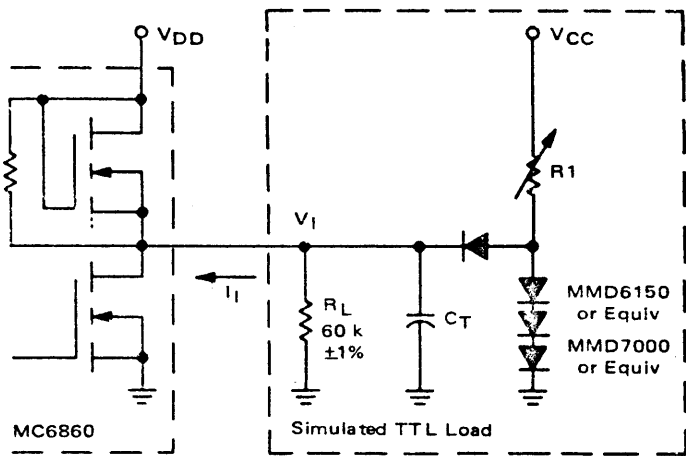
ELECTRICAL CHARACTERISTICS ( $V_{DD} = 5.0 \pm 0.25$  Vdc, all voltages referenced to  $V_{SS} = 0$ ,  $T_A = 0$  to  $70^{\circ}C$ , all outputs loaded as shown in Figure 1 unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage, All Inputs Except Crystal	$V_{IH}$	2.0	—	$V_{DD}$	Vdc
Input Low Voltage, All Inputs Except Crystal	$V_{IL}$	$V_{SS}$	—	0.80	Vdc
Crystal Input Voltage (Crystal Input Driven from an External Reference, Input Coupling Capacitor = 200 pF, Duty Cycle = $50 \pm 5\%$ )	$V_{in}$	1.5	—	2.0	$V_{0-p}$
Input Current ( $V_{in} = V_{SS}$ ) All Inputs Except Rx Car, Tx Data, $\overline{TD}$ , TST, $\overline{RI}$ , $\overline{SH}$ $\overline{RI}$ , $\overline{SH}$ Inputs	$I_{in}$	—	—	-0.2 -1.6	mAdc
Input Leakage Current ( $V_{in} = 7.0$ Vdc, $V_{DD} = V_{SS}$ , $T_A = 25^{\circ}C$ )	$I_{IL}$	—	—	1.0	$\mu$ Adc
Output High Voltage, All Outputs Except An Ph and Tx Car ( $I_{OH1} = -0.04$ mAdc, Load A)	$V_{OH1}$	2.4	—	$V_{DD}$	Vdc
Output Low Voltage, All Outputs Except An Ph and Tx Car ( $I_{OL1} = 1.6$ mAdc, Load A)	$V_{OL1}$	$V_{SS}$	—	0.40	Vdc
Output High Current, An Ph ( $V_{OH2} = 0.8$ Vdc, Load B)	$I_{OH2}$	0.30	—	—	mAdc
Output Low Voltage, An Ph ( $I_{OL2} = 0$ , Load B)	$V_{OL2}$	$V_{SS}$	—	0.30	Vdc
Input Capacitance ( $f = 0.1$ MHz, $T_A = 25^{\circ}C$ )	$C_{in}$	—	5.0	—	pF
Output Capacitance ( $f = 0.1$ MHz, $T_A = 25^{\circ}C$ )	$C_{out}$	—	10	—	pF
Transmit Carrier Output Voltage (Load C)	$V_{CO}$	0.20	0.35	0.50	V(RMS)
Transmit Carrier Output 2nd Harmonic (Load C)	$V_{2H}$	-25	-32	—	dB
Input Transition Times, All Inputs Except Crystal (Operating in the Crystal Input Mode; from 10% to 90% Points)	$t_r$ $t_f$	—	—	1.0*	$\mu$ s
Input Transition Times, Crystal Input (Operating in External Input Reference Mode)	$t_r$ $t_f$	—	—	30	ns
Output Transition Times, All Outputs Except Tx Car (From 10% to 90% Points)	$t_r$ $t_f$	—	—	5.0	$\mu$ s
$V_{DD}$ Supply Current (All Inputs at $V_{SS}$ and All Outputs Open)	$I_{DD}$	—	30	65	mAdc

\*Maximum Input Transition Times are  $\leq 0.1 \times$  Pulse Width or the specified maximum of 1.0  $\mu$ s, whichever is smaller.

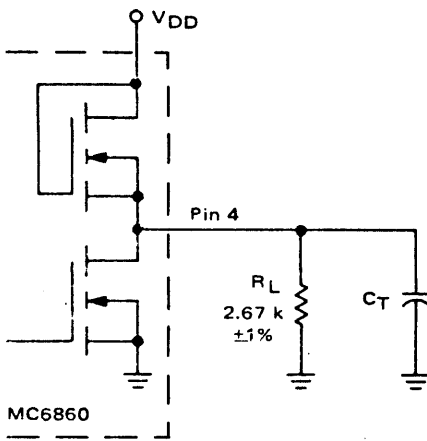
FIGURE 1 - OUTPUT TEST LOADS

**Load A - TTL Output Load for Receive Break, Digital Carrier, Mode, Clear-to-Send, and Receive Data Outputs**

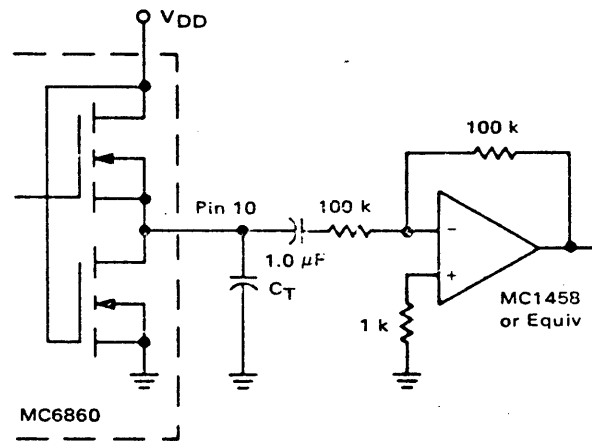


$C_T = 20 \text{ pF}$  = total parasitic capacitance, which includes probe, wiring, and load capacitances  
 $R_1$  is adjusted for  $I_1 = 1.6 \text{ mA}$  at  $V_1 = 0.4 \text{ V}$  when output node is disconnected.

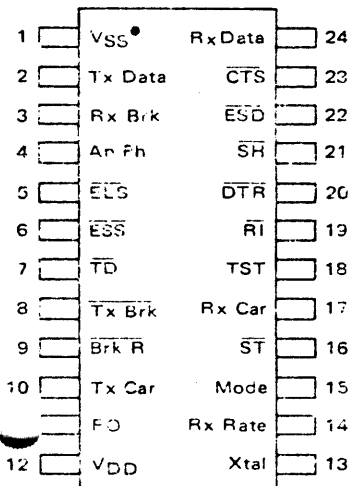
**Load B - Answer Phone Load**



**Load C - Transmit Carrier Load**

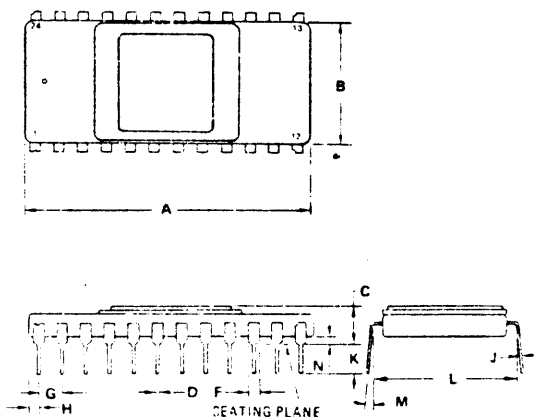


**PIN ASSIGNMENT**



**PACKAGE DIMENSIONS**

**CASE 684-04**

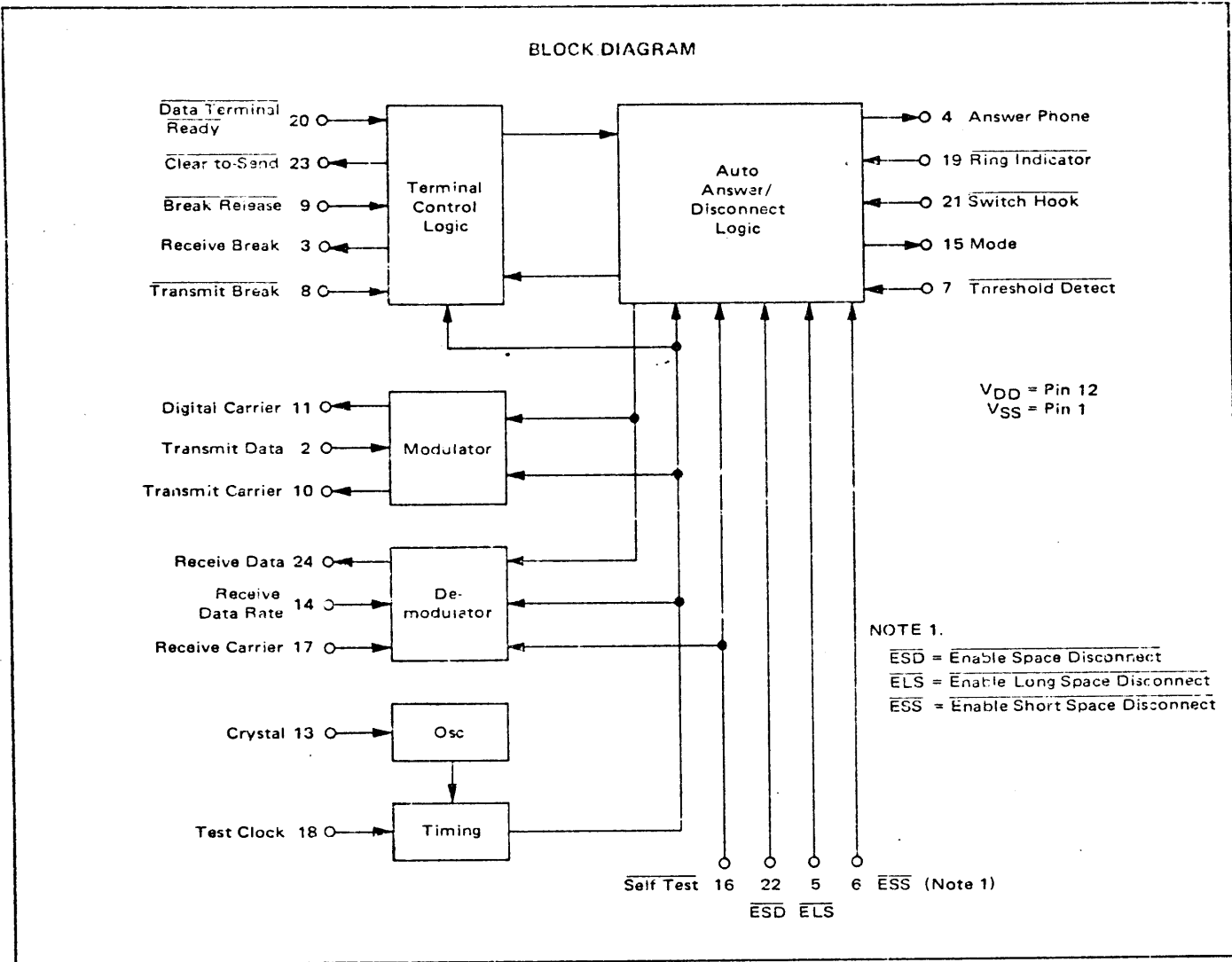


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.35	30.68	1.155	1.215
B	12.70	14.22	0.500	0.560
C	3.25	3.94	0.128	0.155
D	0.38	0.51	0.015	0.020
E	0.95	1.40	0.038	0.055
G	2.94 BSC 0.100 BSC			
H	0.69	1.42	0.035	0.055
J	0.20	0.30	0.008	0.012
K	2.91	3.68	0.115	0.145
L	14.86	15.67	0.585	0.625
M	15°			
N	0.51	1.14	0.020	0.045

**NOTES**

- LEADS WITHIN 0.13 mm (0.005" RADIUS OF TRUE POSITION AT SEATING PLANE WITH MAXIMUM MATERIAL CONDITION
- LEAD NO. 1 CUT FOR IDENTIFICATION OR BUMP ON TOP
- DIM. C TO INSIDE OF LEADS (MEASURED 0.51 mm (0.020") BELOW PKG BASE)

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**DEVICE OPERATION\***

**GENERAL**

Figure 2 shows the modem and its interconnections. The data to be transmitted is presented in serial format to the modulator for conversion to FSK signals for transmission on the telephone line. The modulator output is buffered before driving the line.

The FSK signal from the remote modem is received via the telephone line and filtered to remove extraneous signals such as the local Transmit Carrier. This filtering can be either a bandpass which passes only the desired band of frequencies or a notch which rejects the known interfering signal. The desired signal is then limited to preserve the axis crossings and fed to the demodulator where the data is recovered from the received FSK carrier.

The Supervisory Control provides the necessary commands and responses for handshaking with the remote modem, along with the interface signals to the data coupler and communication terminal. If the modem is a built-in unit, all input-output (I/O) logic need not be RS-232

\*See Tables 1 and 2 for delay time tolerances.

compatible. However, if the modem is a stand-alone unit the computer-modem I/O interface must conform to the EIA specification. The use of MC1428 and MC1489A line drivers and receivers will provide the required interface.

**Answer Mode**

Automatic answering is first initiated by a receipt of a Ring Indicator (RI) signal. This can be either a low level for at least 51 ms as would come from a CBS data coupler, or at least 20 cycles of a 20-47 Hz ringing signal (low level  $\geq$  50% of the duty cycle) as would come from a CBT data coupler. The presence of the Ring Indicator signal places the modem in the Answer Mode; if the Data Terminal Ready line is low, indicating the communication terminal is ready to send or receive data, the Answer output goes high. This output is designed to drive a transistor switch which will activate the Off Hook (OH) and

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Data transmission (DA) relays in the data coupler. Upon answering the phone the 2225-Hz Transmit Carrier is turned on.

The originate modem at the other end detects this 2225-Hz signal and after a 450 ms delay (used to disable any echo suppressors in the telephone network) transmits a 1270-Hz signal which the local answering modem detects, provided the amplitude and frequency requirements are met. The amplitude threshold is set external to the modem chip. If the signal level is sufficient the  $\overline{TD}$  input should be low for 20  $\mu$ s at least once every 32 ms. The absence of a threshold indication for a period greater than 51 ms denotes the loss of Receive Carrier and the modem begins hang-up procedures. Hang-up will occur 17 s after  $\overline{RI}$  has been released provided the handshaking routine is not re-established. The frequency tolerance during handshaking is  $\pm 100$  Hz from the Mark frequency.

After the 1270-Hz signal has been received for 150 ms, the Receive Data is unclamped from a Mark condition and data can be received. The Clear-to-Send output goes low 450 ms after the receipt of carrier and data presented to the answer modem is transmitted.

Enable Short Space Disconnect at the most negative voltage (low), the modem automatically hangs up. If Enable Long Space Disconnect is low, the modem requires 1.5 s of continuous space to hang up.

#### Originate Mode

Upon receipt of a Switch Hook ( $\overline{SH}$ ) command the modem function is placed in the Originate Mode. If the Data Terminal Ready input is enabled (low) the modem will provide a logic high output at Answer Phone. The modem is now ready to receive the 2225-Hz signal from the remote answering modem. It will continue to look for this signal until 17 s after  $\overline{SH}$  has been released. Disconnect occurs if the handshaking routine is not established.

Upon receiving 2225  $\pm 100$  Hz for 150 ms at an acceptable amplitude, the Receive Data output is unclamped from a Mark condition and data reception can be accomplished. 450 ms after receiving a 2225-Hz signal, a 1270-Hz signal is transmitted to the remote modem. 750 ms after receiving the 2225-Hz signal, the Clear-to-Send output is taken low and data can now be transmitted as well as received.

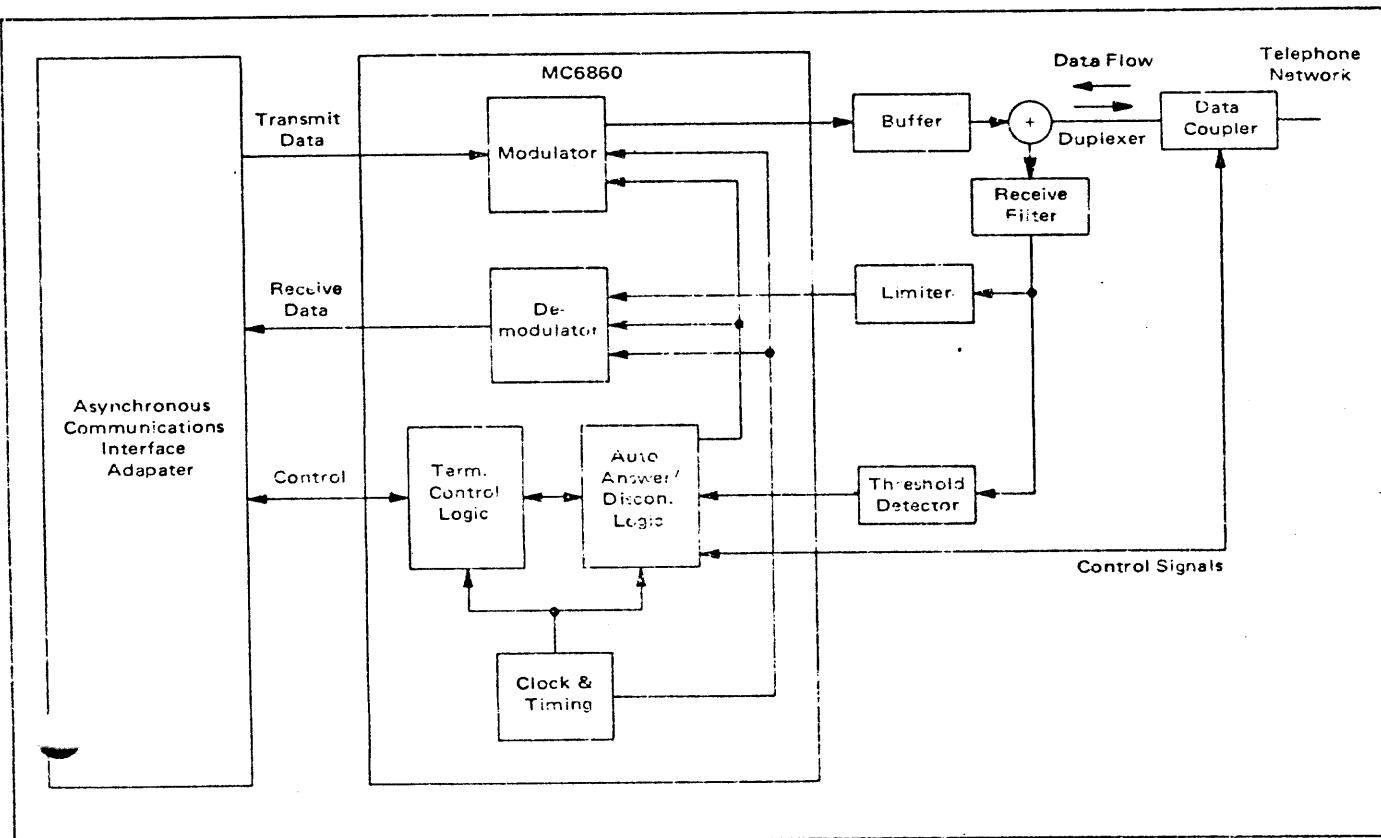
#### Automatic Disconnect

Upon receipt of a space of 150 ms or greater duration, the modem clamps the Receive Break high. This condition exists until a Break Release command is issued at the receiving station. Upon receipt of a 0.3 s space, with

#### Initiate Disconnect

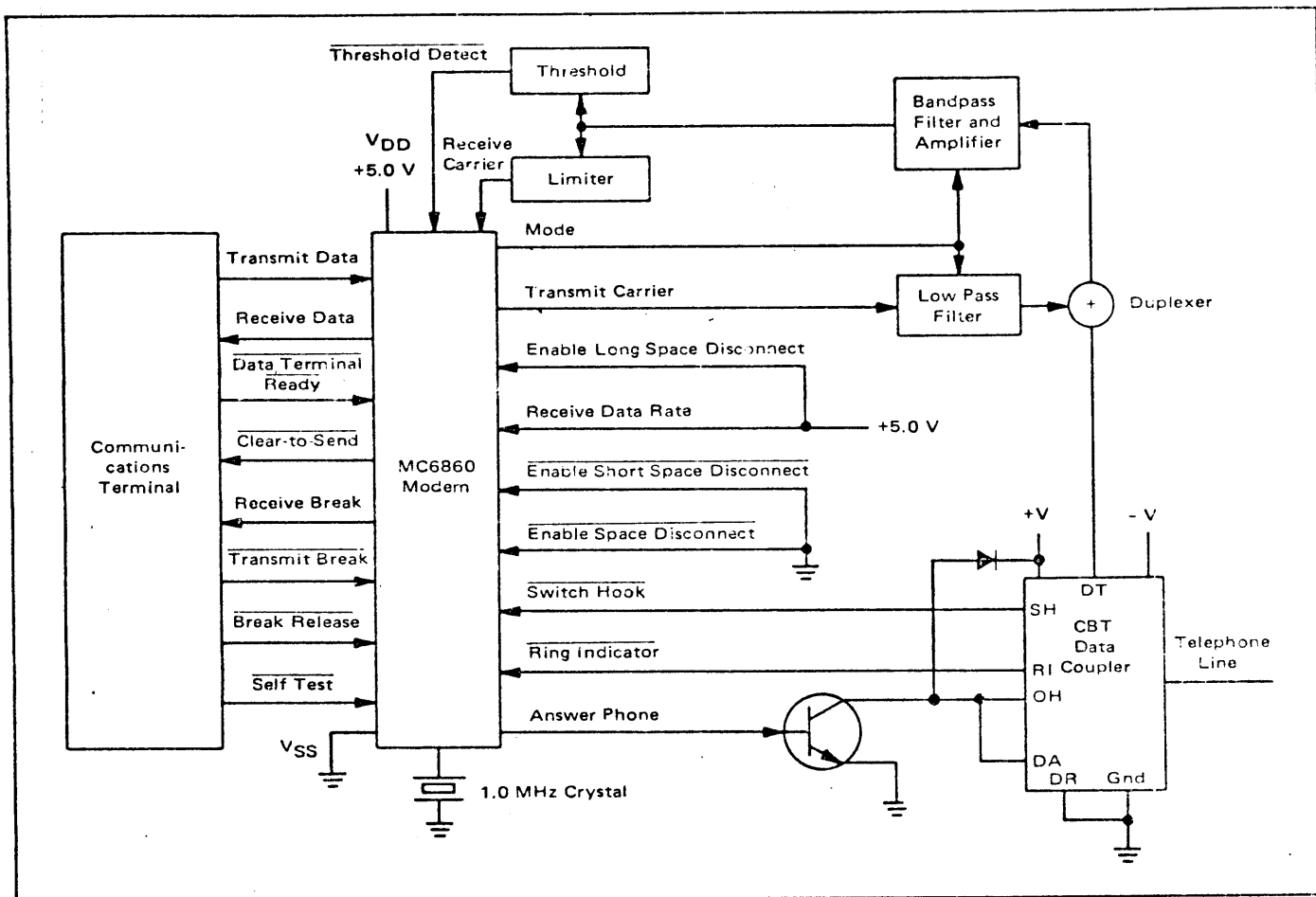
In order to command the remote modem to automatically hang up, a disconnect signal is sent by the local modem. This is accomplished by pulsing the normally low Data Terminal Ready into a high state for greater than

FIGURE 2 - TYPICAL MC6860 SYSTEM CONFIGURATION



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FIGURE 3 - I/O INTERFACE CONNECTIONS FOR MC6860  
 (ORIGINATE/ANSWER MODEM)



34 ms. The local modem then sends a 3 s continuous space and hangs up provided the Enable Space Disconnect is low. If the remote modem hangs up before 3 s, loss of Threshold Detect will cause loss of Clear-to-Send, which marks the line in Answer Mode and turns the carrier off in the Originate Mode.

If  $\overline{ESD}$  is high the modem will transmit data until hang-up occurs 3 s later.  $\overline{Transmit Break}$  is clamped 150 ms following the Data Terminal Ready interrupt.

### INPUT/OUTPUT FUNCTIONS

Figure 3 shows the I/O interface for the low speed modem. The following is a description of each individual signal:

#### Receive Carrier (Rx Car)

The Receive Carrier is the FSK input to the demodulator. The local Transmit Carrier must be balanced or filtered out prior to this input, leaving only the Receive Carrier in the signal. The Receive Carrier must also be hard limited. Any half-cycle period greater than or equal to  $429 \pm 1.0 \mu s$  for the low band or  $235 \pm 1.0 \mu s$  for the high band is detected as a space.

#### Ring Indicator ( $\overline{RI}$ )

The modem function will recognize the receipt of a call from the CBT if at least 20 cycles of the 20-47 Hz ringing signal (low level  $\geq 50\%$  of the duty cycle) are present. The CBS  $\overline{RI}$  signal must be level-converted to TTL according to the EIA RS-232 specification before interfacing it with the modem function. The receipt of a call from the CBS is recognized if the  $\overline{RI}$  signal is present for at least 51 ms. This input is held high except during ringing. A  $\overline{RI}$  signal automatically places the modem function in the Answer Mode.

#### Switch Hook ( $\overline{SH}$ )

$\overline{SH}$  interfaces directly with the CBT and via the EIA RS-232 level conversion for the CBS. An  $\overline{SH}$  signal automatically places the modem function in the Originate Mode.

$\overline{SH}$  is low during origination of a call. The modem will automatically hang up 17 s after releasing  $\overline{SH}$  if the handshaking routine has not been accomplished.

#### Threshold Detect ( $\overline{TD}$ )

This input is derived from an external threshold detector. If the signal level is sufficient, the  $\overline{TD}$  input must

D COMPONENT DESCRIPTION  
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be low for 20  $\mu$ s at least once every 32 ms to maintain normal operation. An insufficient signal level indicates the absence of the Receive Carrier; an absence for less than 32 ms will not cause channel establishment to be lost; however, data during this interval will be invalid.

If the signal is present and the level is acceptable at all times, then the threshold input can be low permanently.

Loss of threshold for 51 ms or longer results in a loss of Clear-to-Send. The Transmit Carrier of the originate modem is clamped off and a constant Mark is transmitted from the answer modem.

**Receive Data Rate (Rx Rate)**

The demodulator has been optimized for signal-to-noise performance at 300 bps and 600 bps. The Receive Data Rate input must be low for 0-600 bps and should be high for 0-300 bps.

**Transmit Data (Tx Data)**

Transmit Data is the binary information presented to the modem function for modulation with FSK techniques. A high level represents a Mark.

**Data Terminal Ready (DTR)**

The Data Terminal Ready signal must be low before the modem function will be enabled. To initiate a disconnect, DTR is held high for 34 ms minimum. A disconnect will occur 3 s later.

**Break Release (Brk R)**

After receiving a 150 ms space signal, the clamped high condition of the Receive Break output can be removed by holding Break Release low for at least 20  $\mu$ s.

**Transmit Break (Tx Brk)**

The Break command is used to signal the remote modem to stop sending data.

A Transmit Break (low) greater than 34 ms forces the modem to send a continuous space signal for 233 ms. Transmit Break must be initiated only after CTS has been established. This is a negative edge sense input. Prior to initiating Tx Brk, this input must be held high for a minimum of 34 ms.

**Enabled Space Disconnect (ESD)**

When ESD is strapped low and DTR is pulsed to initiate a disconnect, the modem transmits a space for either 3 s or until a loss of threshold is detected, whichever occurs first. If ESD is strapped high, data instead of a space is transmitted. A disconnect occurs at the end of 3 s.

**Enable Short Space Disconnect (ESS)**

ESS is a strapping option which, when low, will automatically hang up the phone upon receipt of a continuous space for 0.3 s. ESS and ELS must not be simultaneously strapped low.

**Enable Long Space Disconnect (ELS)**

ELS is a strapping option which, when low, will automatically hang up the phone upon receipt of a continuous space for 1.5 s.

**Crystal (Xtal)**

A 1.0-MHz crystal with the following parameters is required to utilize the on-chip oscillator. A 1.0-MHz square wave can also be fed into this input to satisfy the clock requirement.

Mode:	Parallel
Frequency:	1.0 MHz $\pm$ 0.1%
Series Resistance:	750 ohms max
Shunt Capacitance:	7.0 pF max
Temperature:	0-70°C
Test Level:	1.0 mW
Load Capacitance:	13 pF

When utilizing the 1.0-MHz crystal, external parasitic capacitance, including crystal shunt capacitance, must be  $\leq$  9 pF at the crystal input.

**Test Clock (TST)**

A test signal input is provided to decrease the test time of the chip. In normal operation this input *must be strapped low*.

**Self Test (ST)**

When a low voltage level is placed on this input, the demodulator is switched to the modulator frequency and demodulates the transmitted FSK signal. Channel establishment, which occurred during the initial handshake, is not lost during self test. The Mode Control output changes state during Self Test, permitting the receive filters to pass the local Transmit Carrier.

ST	SH	RI	Mode
H	L	H	H
H	H	L	L
L	L	H	L
L	H	L	H

**Answer Phone (An Ph)**

Upon receipt of Ring Indicator or Switch Hook signal and Data Terminal Ready, the Answer Phone output goes high  $\{(\overline{SH} + \overline{RI}) \bullet \overline{DTR}\}$ . This signal drives the base of a transistor which activates the Off Hook and Data Transmission control lines in the data coupler. Upon call completion, the Answer Phone signal returns to a low level.

**Mode**

The Mode output indicates the Answer (low) or Originate (high) status of the modem. This output changes state when a Self Test command is applied.

D COMPONENT DESCRIPTION  
 D.6 INTEGRATED CIRCUITS

6860 cont'd

**Clear-To-Send (CTS)**

A low on the  $\overline{\text{CTS}}$  output indicates the Transmit Data input has been unclamped from a steady Mark, thus allowing data transmission.

**Receive Data (Rx Data)**

The Receive Data output is the data resulting from demodulating the Receive Carrier. A Mark is a high level.

**Receive Break (Rx Brk)**

Upon receipt of a continuous 150 ms space, the modem automatically clamps the Receive Break output high. This output is also clamped high until Clear-to-Send is established.

**Digital Carrier (FO)**

A test signal output is provided to decrease the chip test time. The signal is a square wave at the transmit frequency.

**Transmit Carrier (Tx Car)**

The Transmit Carrier is a digitally-synthesized sine wave (Figure 4) derived from the 1.0-MHz crystal reference. The frequency characteristics are as follows:

Mode	Data	Transmit Frequency	Tolerance*
Originate	Mark	1270 Hz	-0.16 Hz
Originate	Space	1070 Hz	0.07 Hz
Answer	Mark	2225 Hz	-0.31 Hz
Answer	Space	2025 Hz	-0.71 Hz

\*The reference frequency tolerance is not included.

The proper output frequency is transmitted within 3.0  $\mu\text{s}$  following a data bit change with no more than 2.0  $\mu\text{s}$  phase discontinuity. The typical output level is 0.35 V (RMS) into a 100 k-ohm load impedance.

The second harmonic is typically 32 dB below the fundamental (Figure 5).

**POWER-ON RESET**

Power-on reset is provided on-chip to insure that when power is first applied the Answer Phone output is in the low (inactive) state. This holds the modem in the inactive or idle mode until a  $\overline{\text{SH}}$  or  $\overline{\text{RI}}$  signal has been applied. Once power has been applied, a momentary loss of power at a later time may not be of sufficient time to guarantee a chip reset through the power-on reset circuit.

To insure initial power-on reset action, the external parasitic capacitance on  $\overline{\text{RI}}$  and  $\overline{\text{SH}}$  should be  $< 30$  pF. Capacitance values  $> 30$  pF may require the use of an external pullup resistor to  $V_{\text{DD}}$  on these inputs in addition to the pullup devices already provided on chip.

FIGURE 4 – TRANSMIT CARRIER SINE WAVE

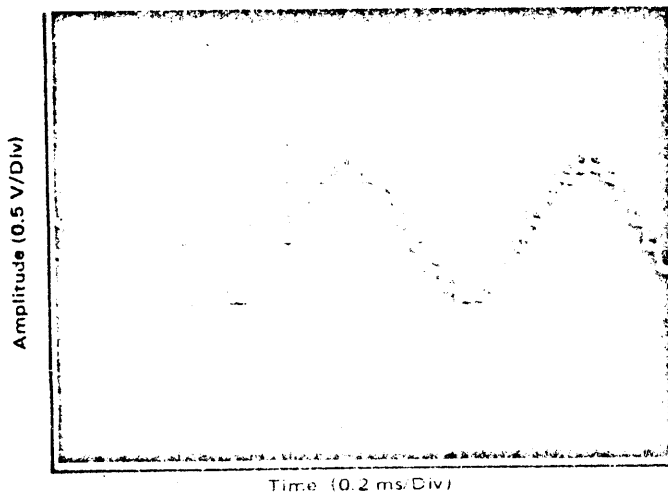
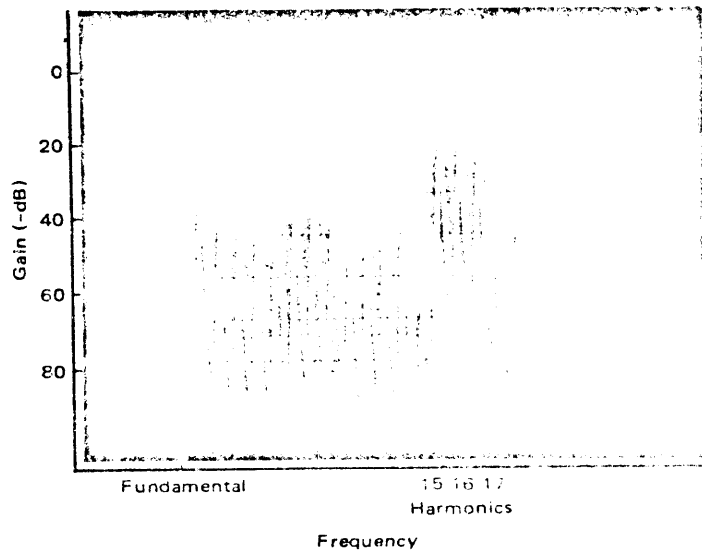


FIGURE 5 – TRANSMIT CARRIER FREQUENCY SPECTRUM



6860 cont'd

TIMING DIAGRAMS  
 FIGURE 6 - ANSWER MODE

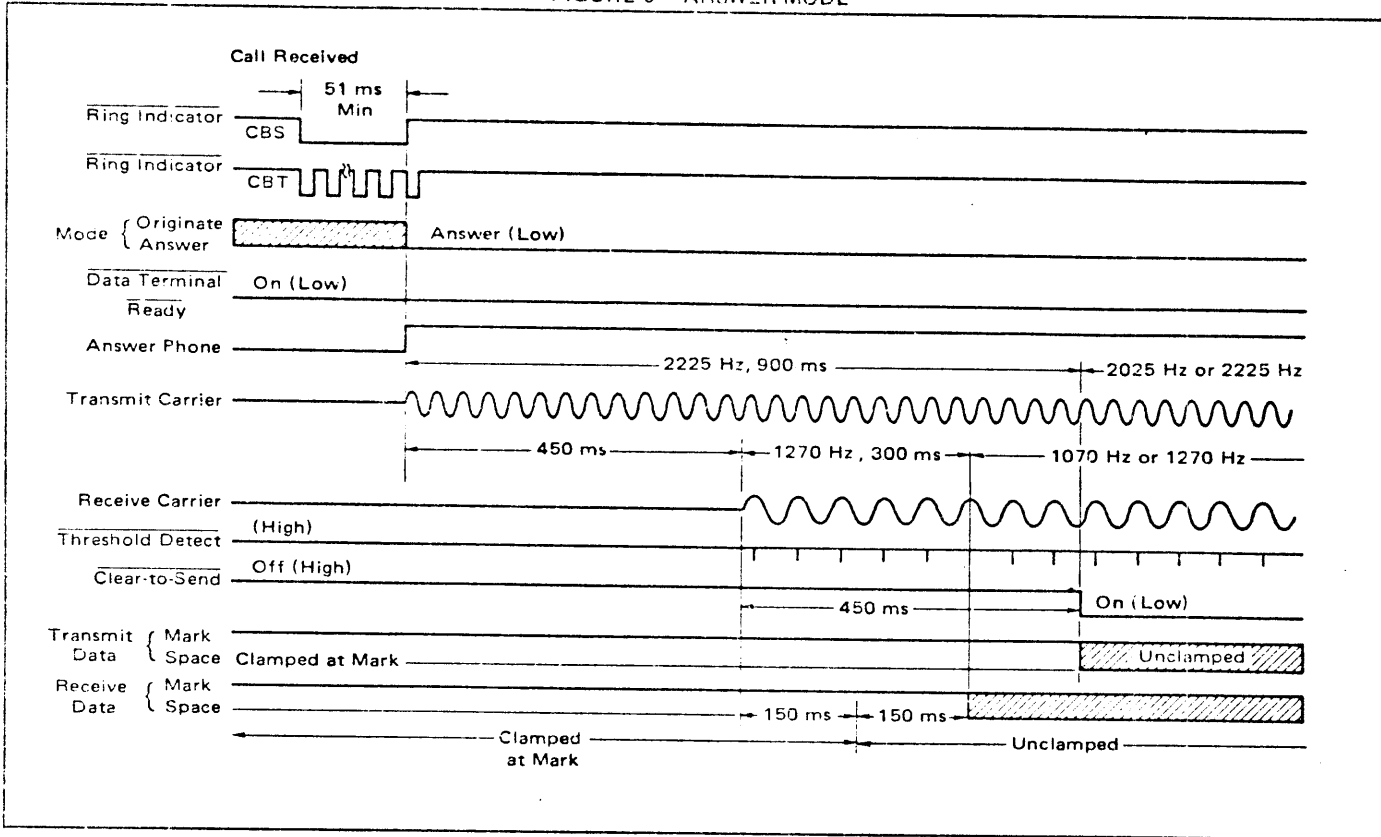
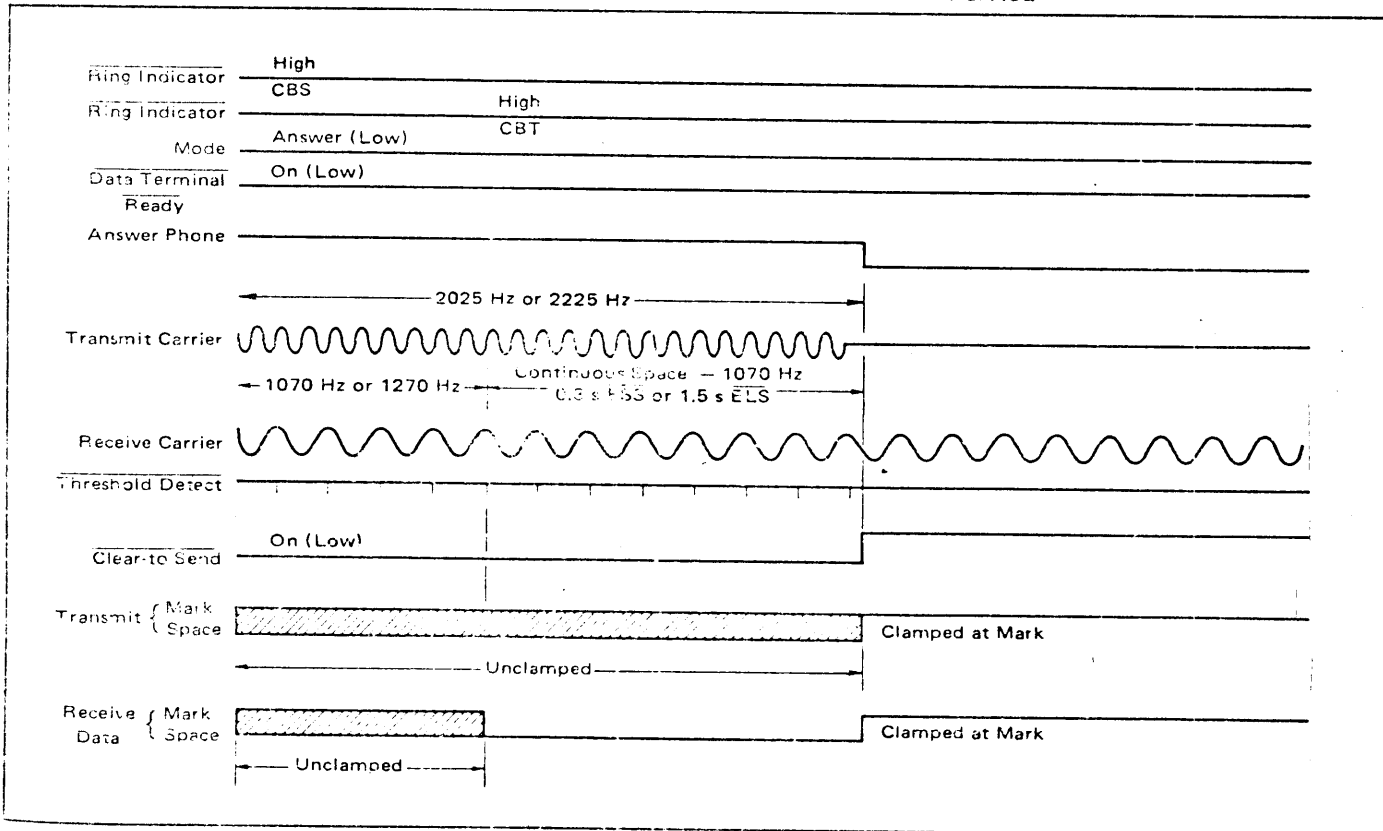


FIGURE 7 - AUTOMATIC DISCONNECT - LONG OR SHORT SPACE





6860 cont'd

FIGURE 8 - ORIGINATE MODE

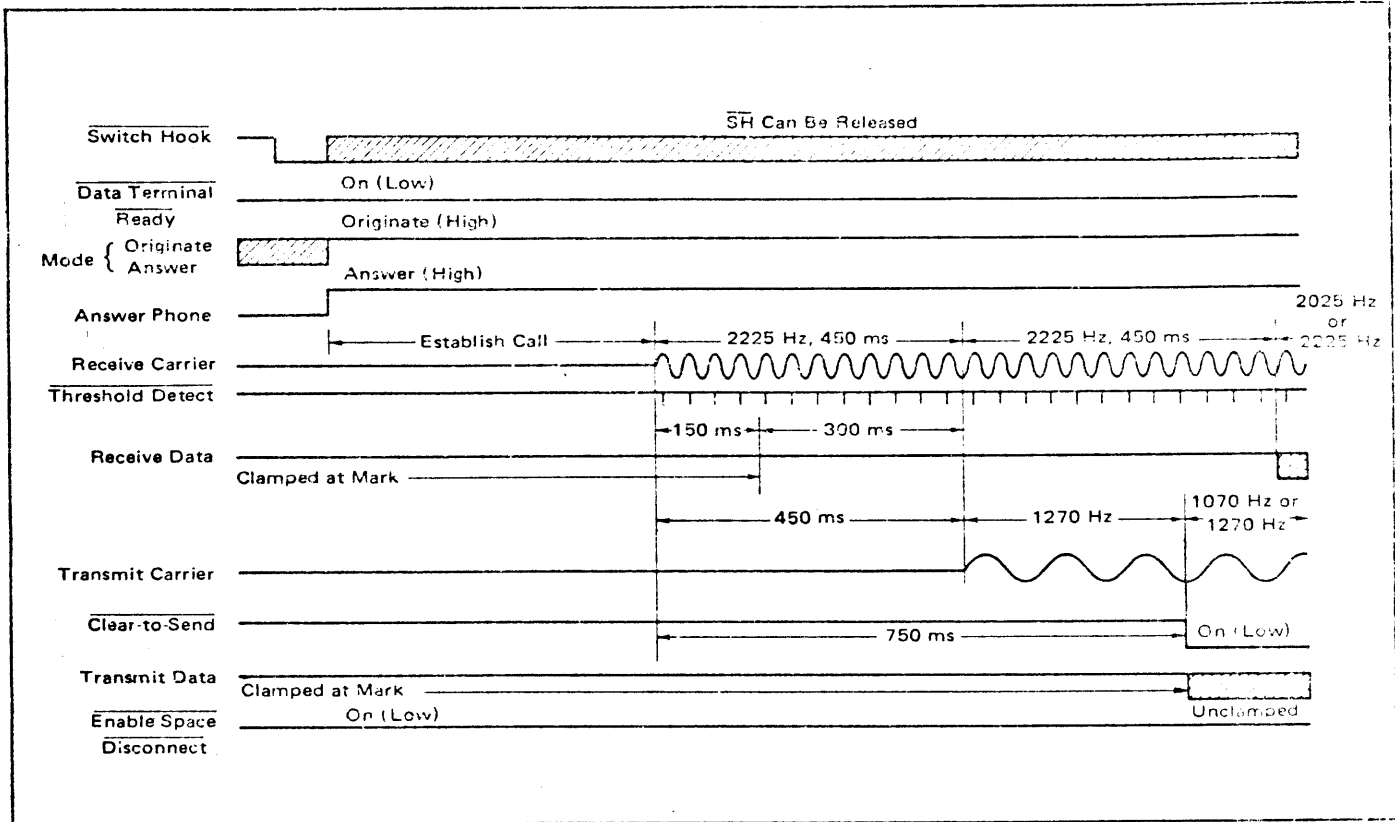
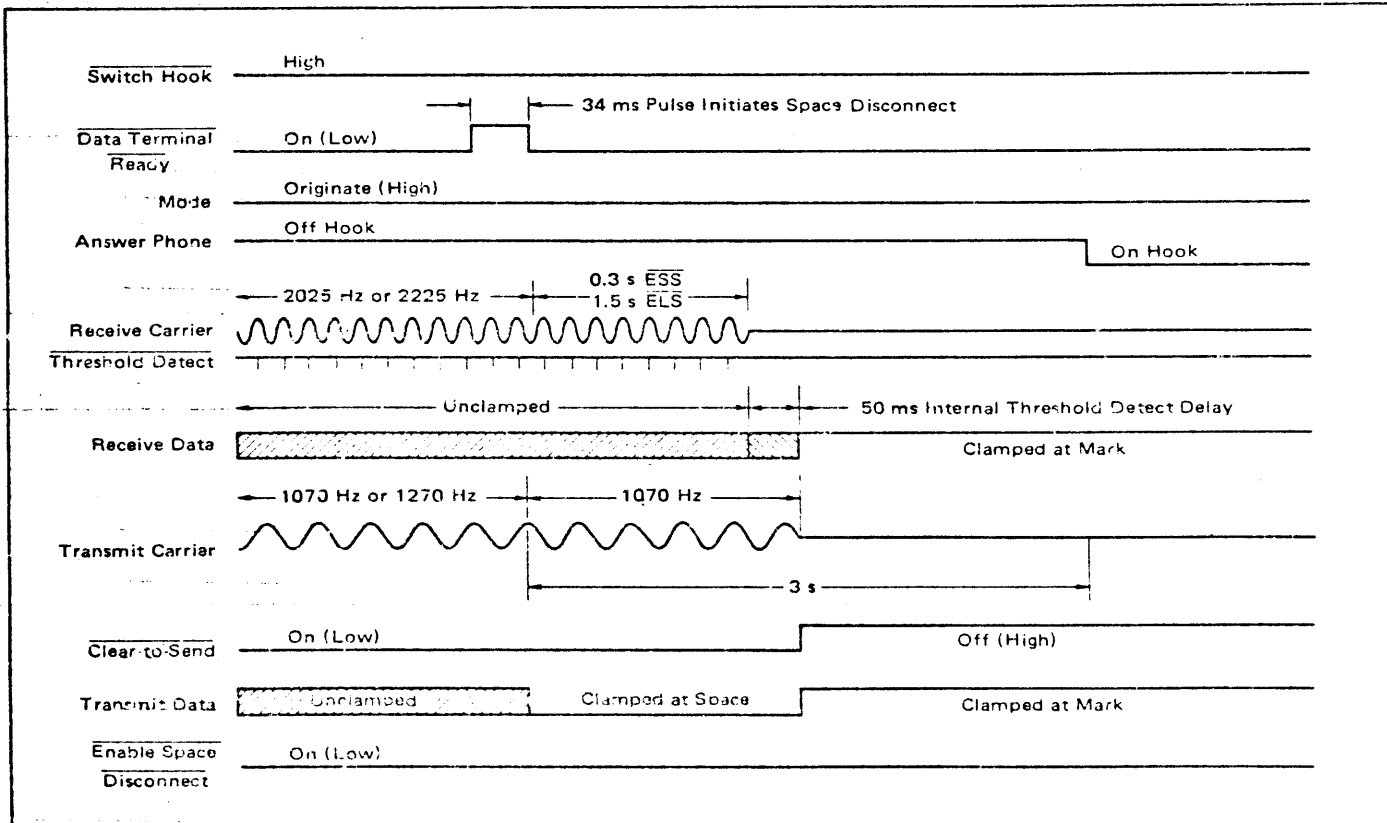


FIGURE 9 - INITIATE DISCONNECT



D COMPONENT DESCRIPTION  
 D.6 INTEGRATED CIRCUITS

6860 cont'd

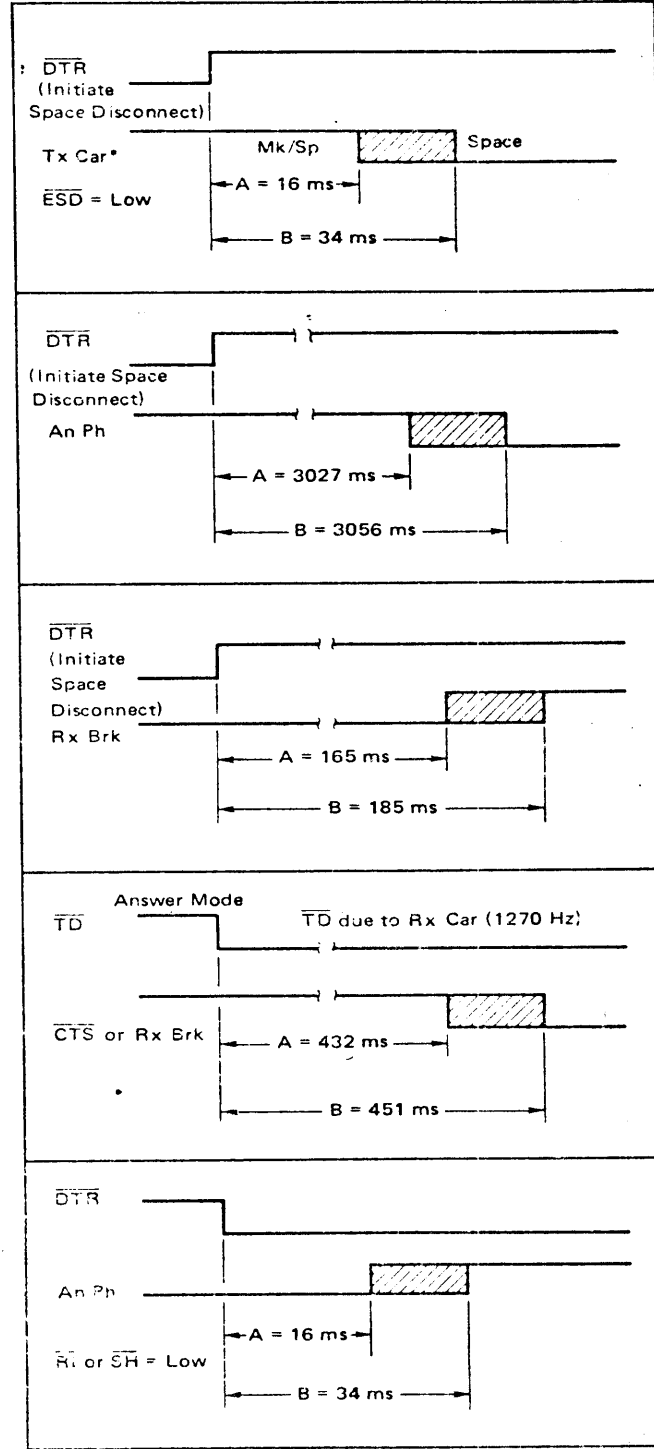
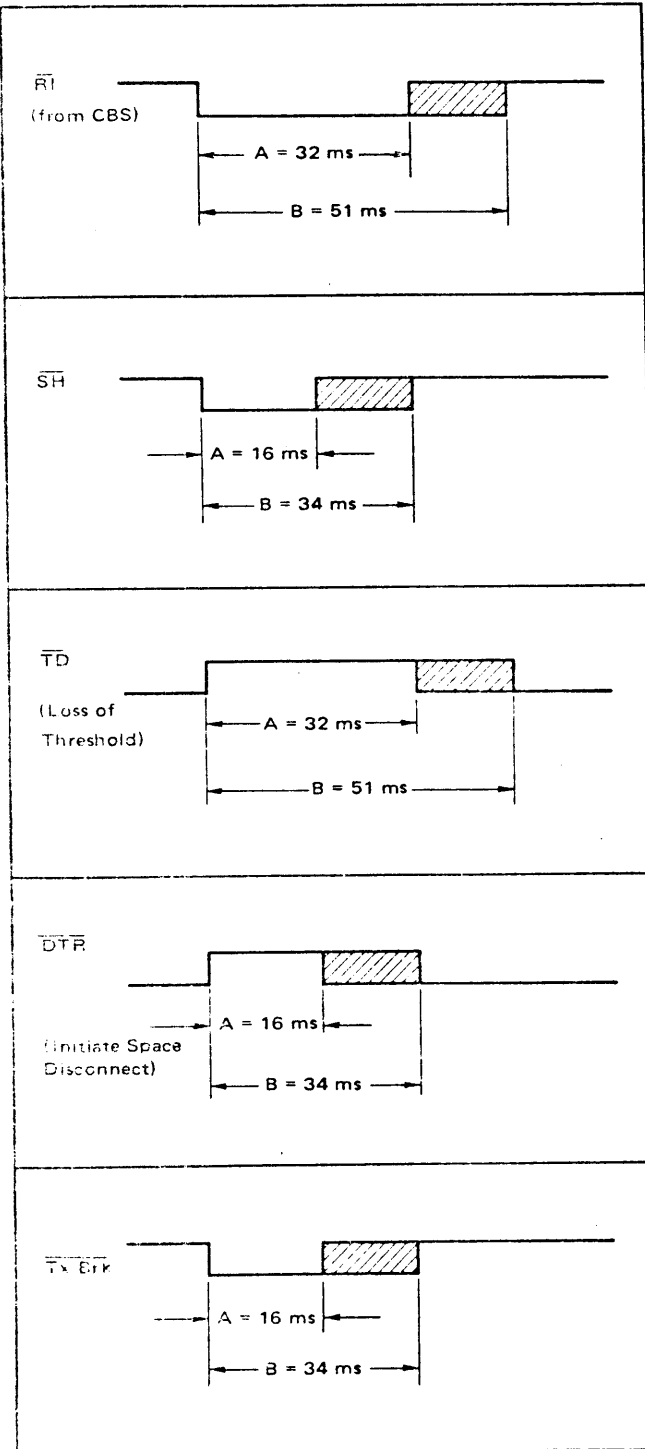
TABLE 1 — ASYNCHRONOUS INPUT PULSE WIDTH AND OUTPUT DELAY VARIATIONS  
 (Time delays specified do not include the 1-MHz reference tolerance.)

Due to the asynchronous nature of the input signals with respect to the circuit internal clock, a delay variation or input pulse width requirement will exist. Time delay A is the maximum time for which no response will occur. Time delay B is the minimum time required to guarantee an input response. Input signal widths in the cross-hatched region (i.e., greater than A but less than B) may or may not be recognized as valid.

For output delays, time A is the minimum delay before an output will respond. Time B is the maximum delay for an output to respond. Output signal response may or may not occur in the cross-hatched region (i.e., greater than A but less than B).

INPUT PULSES

OUTPUT DELAYS

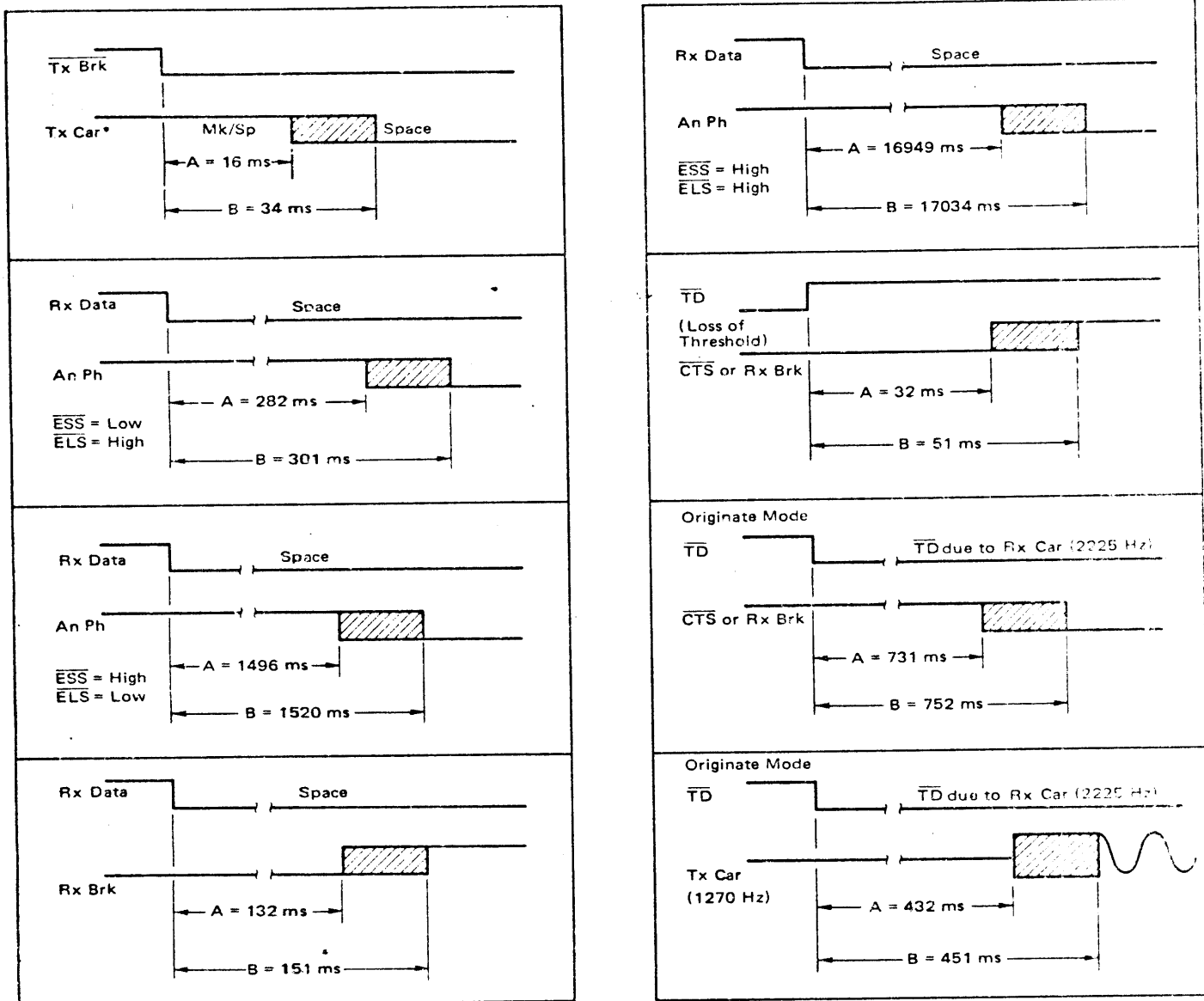


\* Digital Representation.

(continued)

6860 cont'd

TABLE 1 – OUTPUT DELAY VARIATIONS (continued)



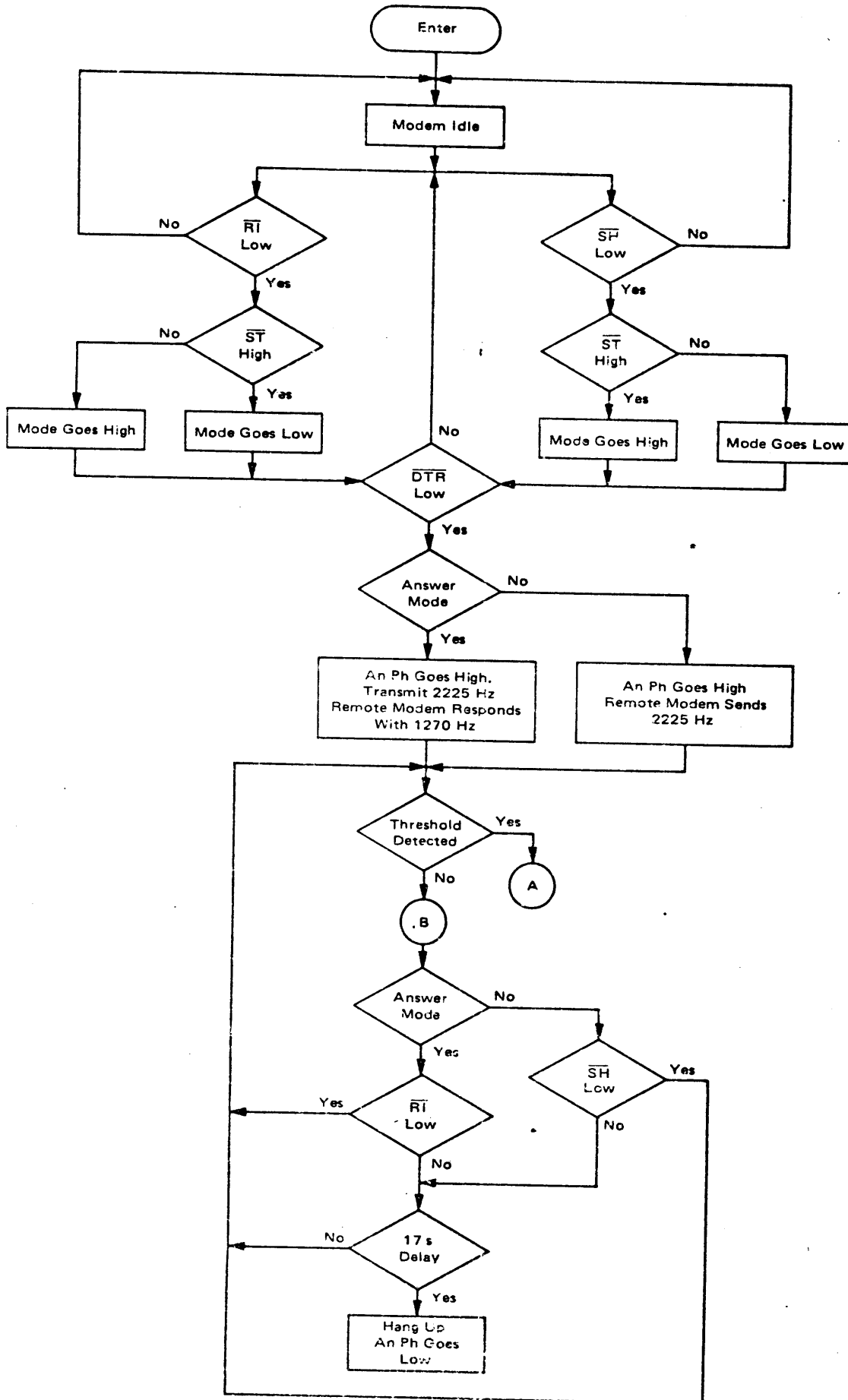
\*Digital Representation

TABLE 2 – TRANSMIT BREAK AND DISCONNECT DELAYS

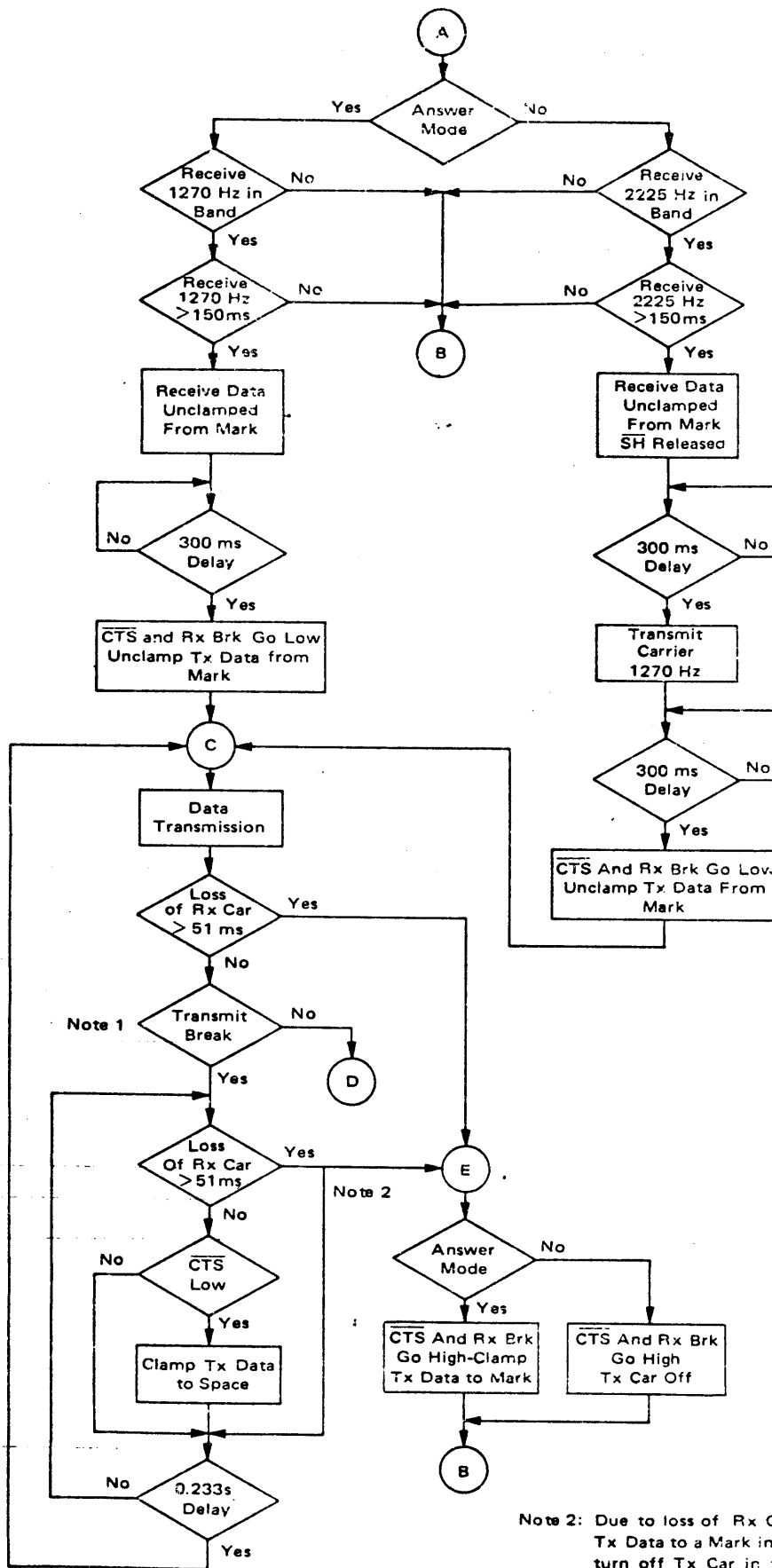
Function Description	Min	Max	Unit
Tx Brk (Space Duration)	232	235	ms
Space Disconnect (Space Duration) ( $\overline{DTR} = \text{High}$ , $\overline{ESD}$ and $\overline{TD} = \text{Low}$ )	3010	3023	ms
Loss of Carrier Disconnect (Measured from positive edge of $\overline{CTS}$ to negative edge of An Ph, with $\overline{RI}$ , $\overline{SH}$ , and $\overline{TD} = \text{High}$ )	16965	17034	ms
Override Disconnect (Measured from positive edge of $\overline{RI}$ or $\overline{SH}$ to negative edge of An Ph, with $\overline{TD} = \text{High}$ )	16916	17101	ms

6860 cont'd

FIGURE 10 - FLOW DIAGRAM



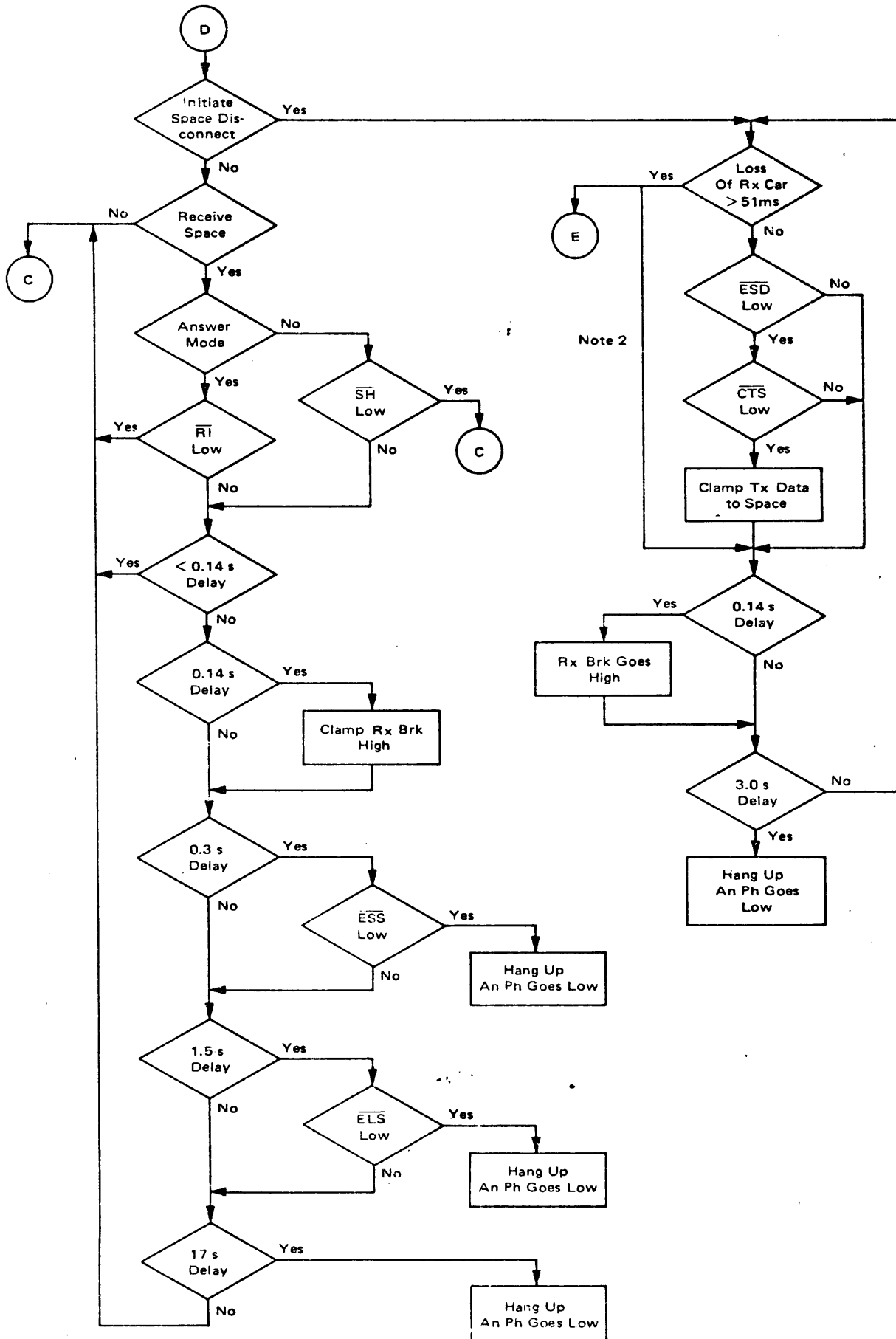
6860 cont'd



Note 1: Transmit Break, Initiate Space Disconnect, and Receive Space are mutually exclusive events.

Note 2: Due to loss of Rx Car, the modem will clamp Tx Data to a Mark in the Answer Mode and will turn off Tx Car in the Originate Mode. If Rx Car is detected before completion of Tx Brk or Initiate Space Disconnect, normal operation of Tx Brk or Initiate Space Disconnect will continue until completion of their respective time delays.

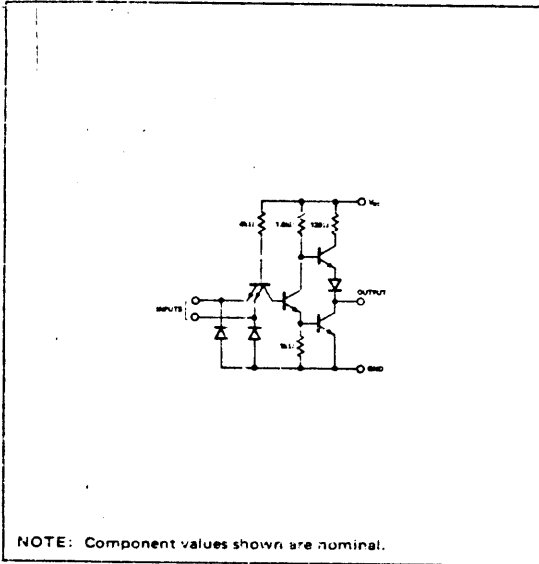
6860 cont'd



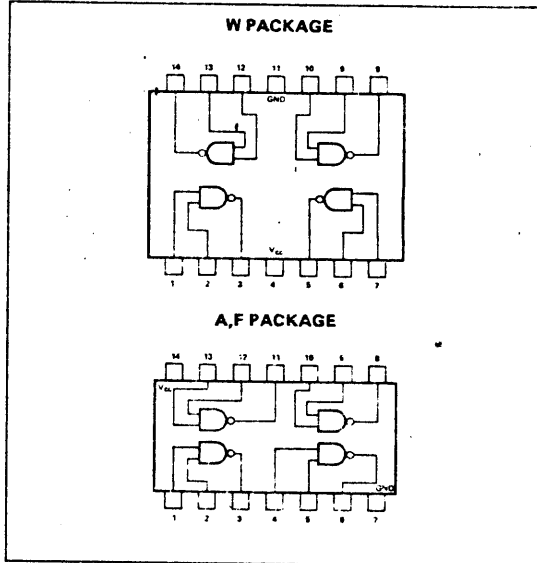
D COMPONENT DESCRIPTION  
D.6 INTEGRATED CIRCUITS

7400

Schematic (each gate)



PIN CONFIGURATIONS



RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage $V_{CC}$ : S5400 Circuits	4.5	5	5.5	V
N7400 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10	
Operating Free-Air Temperature Range, $T_A$ : S5400 Circuits	-55	25	125	$^{\circ}C$
N7400 Circuits	0	25	70	$^{\circ}C$

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 level at output	$V_{CC} = \text{MIN}$	2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 level at output	$V_{CC} = \text{MIN}$			0.8	V
$V_{out(1)}$	Logical 1 output voltage	$V_{CC} = \text{MIN}$ , $I_{load} = -400\mu A$	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	$V_{CC} = \text{MIN}$ , $I_{sink} = 16\text{mA}$		0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	$V_{CC} = \text{MAX}$ , $V_{in} = 0.4\text{V}$			-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	$V_{CC} = \text{MAX}$ , $V_{CC} = \text{MAX}$ , $V_{in} = 2.4\text{V}$ , $V_{in} = 5.5\text{V}$			40 1	$\mu A$ mA
$I_{OS}$	Short circuit output current†	$V_{CC} = \text{MAX}$	S5400 N7400	-20 -18	-55 -55	mA

D COMPONENT DESCRIPTION  
D.6 INTEGRATED CIRCUITS

7400 cont'd

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$I_{CC(0)}$	Logical 0 level supply current	$V_{CC} = \text{MAX.}$	$V_{in} = 5V$		12	22	mA
$I_{CC(1)}$	Logical 1 level supply current	$V_{CC} = \text{MAX.}$	$V_{in} = 0$		4	8	mA

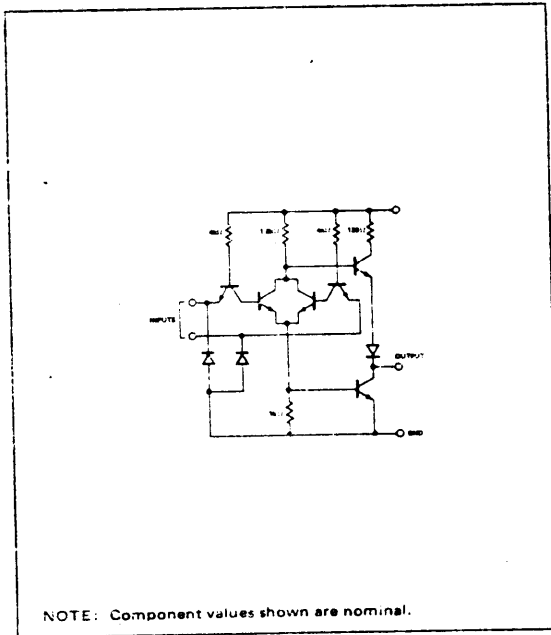
SWITCHING CHARACTERISTICS,  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $N = 10$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	$C_L = 15pF$	$R_L = 400\Omega$		7	15	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level	$C_L = 15pF$	$R_L = 400\Omega$		11	22	ns

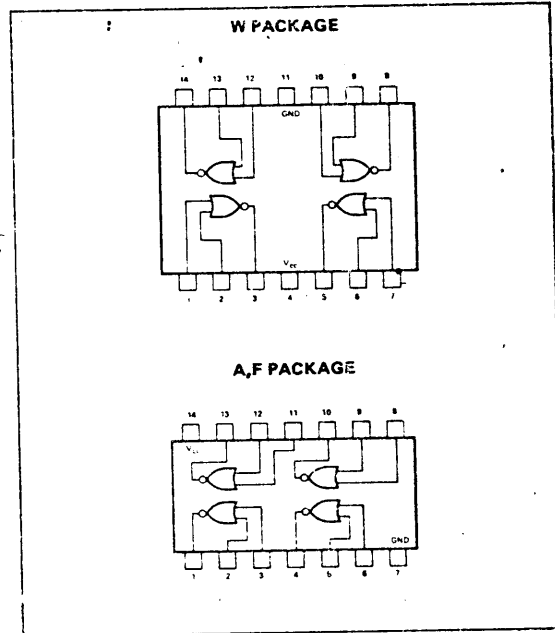
- \* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- \*\* All typical values are at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$
- † Not more than one output should be shorted at a time.

7402

SCHEMATIC (each gate)



PIN CONFIGURATIONS



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage $V_{CC}$ :	S5402 Circuits	4.5	5	5.5	V
	N7402 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, $T_A$ :	S5402 Circuits	-55	25	125	$^\circ C$
	N7402 Circuits	0	25	70	$^\circ C$



D COMPONENT DESCRIPTION  
 D.6 INTEGRATED CIRCUITS

7402 cont'd

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at either input terminal to ensure logical 0 level at output	$V_{CC} = \text{MIN}$		2			V
$V_{in(0)}$	Logical 0 input voltage required at both input terminals to ensure logical 1 level at output	$V_{CC} = \text{MIN}$				0.8	V
$V_{out(1)}$	Logical 1 output voltage	$V_{CC} = \text{MIN}$ , $I_{load} = -400\mu\text{A}$	$V_{in} = 0.8\text{V}$	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	$V_{CC} = \text{MIN}$ , $I_{sink} = 16\text{mA}$	$V_{in} = 2\text{V}$		0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	$V_{CC} = \text{MAX}$ ,	$V_{in} = 0.4\text{V}$			-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	$V_{CC} = \text{MAX}$ , $V_{CC} = \text{MAX}$ ,	$V_{in} = 2.4\text{V}$ , $V_{in} = 5.5\text{V}$			40 1	$\mu\text{A}$ mA
$I_{OS}$	Short circuit output current†	$V_{CC} = \text{MAX}$	S5402 N7402	-20 -18		-55 -55	mA
$I_{CC(0)}$	Logical 0 level supply current	$V_{CC} = \text{MAX}$ ,	$V_{in} = 5\text{V}$		14	27	mA
$I_{CC(1)}$	Logical 1 level supply current	$V_{CC} = \text{MAX}$ ,	$V_{in} = 0$		8	16	mA

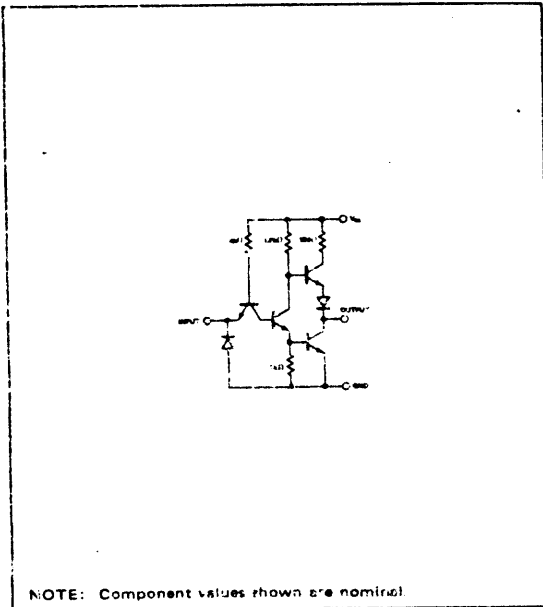
SWITCHING CHARACTERISTICS,  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ ,  $N = 10$

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{pd0}$	Propagation delay time to logical 0 level	$C_L = 15\text{pF}$ , $R_L = 400\Omega$		8	15	ns
$t_{pd1}$	Propagation delay time to logical 1 level	$C_L = 15\text{pF}$ , $R_L = 400\Omega$		12	22	ns

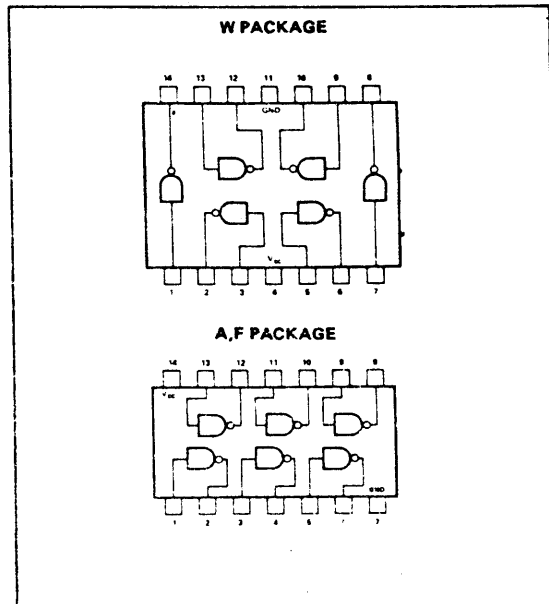
- \* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- \*\* All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$
- † Not more than one output should be shorted at a time.

7404

SCHEMATIC (each inverter)



PIN CONFIGURATIONS



D COMPONENT DESCRIPTION  
D.6 INTEGRATED CIRCUITS

7404 cont'd

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage $V_{CC}$ : S5404 Circuits	4.5	5	5.5	V
N7404 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output, N			10	
Operating Free-Air Temperature Range, $T_A$ : S5404 Circuits	-55	25	125	°C
N7404 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 level at output	$V_{CC} = \text{MIN}$		2	V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	$V_{CC} = \text{MIN}$		0.8	V
$V_{out(1)}$	Logical 1 output voltage	$V_{CC} = \text{MIN}$ , $I_{load} = -400\mu\text{A}$	$V_{in} = 0.8\text{V}$ , 3.3	2.4	V
$V_{out(0)}$	Logical 0 output voltage	$V_{CC} = \text{MIN}$ , $I_{sink} = 16\text{mA}$	$V_{in} = 2\text{V}$ , 0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	$V_{CC} = \text{MAX}$ , $V_{in} = 0.4\text{V}$		-1.6	mA
$I_{in(1)}$	Logical 1 level input current	$V_{CC} = \text{MAX}$ , $V_{CC} = \text{MAX}$ , $V_{in} = 2.4\text{V}$ , $V_{in} = 5.5\text{V}$		40 1	$\mu\text{A}$ mA
$I_{OS}$	Short circuit output current†	$V_{CC} = \text{MAX}$	S5404 N7404	-20 -18	-55 -65 mA
$I_{CC(0)}$	Logical 0 level supply current	$V_{CC} = \text{MAX}$ , $V_{in} = 5\text{V}$		18	33 mA
$I_{CC(1)}$	Logical 1 level supply current	$V_{CC} = \text{MAX}$ , $V_{in} = 0$		6	12 mA

SWITCHING CHARACTERISTICS,  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ ,  $N = 10$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd0}$	Propagation delay time to logical 0 level	$C_L = 15\text{pF}$ , $R_L = 400\Omega$	8	15	ns
$t_{pd1}$	Propagation delay time to logical 1 level	$C_L = 15\text{pF}$ , $R_L = 400\Omega$	12	22	ns

\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

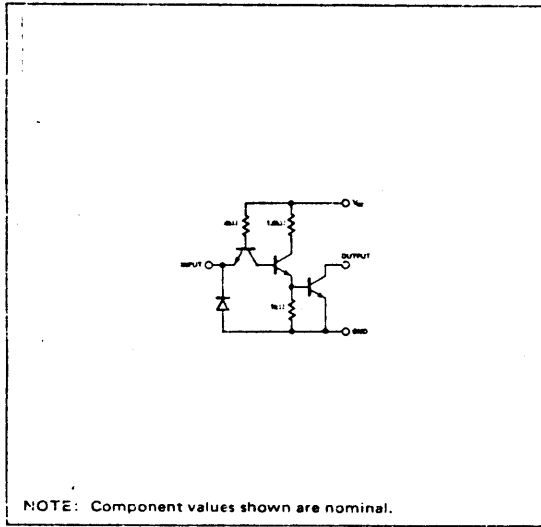
\*\* All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ .

† Not more than one output should be shorted at a time.

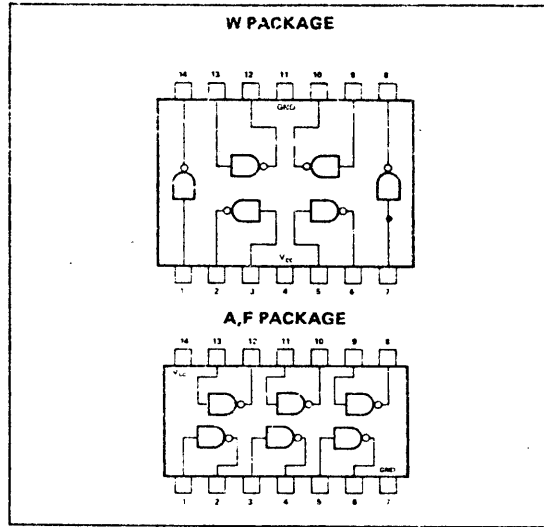
D COMPONENT DESCRIPTION  
D.6 INTEGRATED CIRCUITS

7405

SCHEMATIC (each inverter)



PIN CONFIGURATIONS



RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage $V_{CC}$ : S5405 Circuits	4.5	5	5.5	V
N7405 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output, N			10	
Operating Free-Air Temperature Range, $T_A$ : S5405 Circuits	-55	25	125	$^{\circ}C$
N7405 Circuits	0	25	70	$^{\circ}C$

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 (on) level at output $V_{CC} = \text{MIN}$	2			V
$V_{in(0)}$	Logical 0 input voltage required at input terminal to ensure logical 1 (off) level at output $V_{CC} = \text{MIN}$			0.3	V
$I_{out(1)}$	Output reverse current $V_{CC} = \text{MIN}$ , $V_{out(1)} = 5.5V$ , $V_{in} = 0.8V$			250	$\mu A$
$V_{out(0)}$	Logical 0 output voltage (on level) $V_{CC} = \text{MIN}$ , $I_{sink} = 16mA$ , $V_{in} = 2V$			0.4	V
$I_{in(0)}$	Logical 0 level input current $V_{CC} = \text{MAX}$ , $V_{in} = 0.4V$			-1.6	mA
$I_{in(1)}$	Logical 1 level input current $V_{CC} = \text{MAX}$ , $V_{CC} = \text{MAX}$ , $V_{in} = 2.4V$ , $V_{in} = 5.5V$			40 1	$\mu A$ mA
$I_{CC(0)}$	Logical 0 level supply current $V_{CC} = 5V$ , $T_A = 25^{\circ}C$ , $V_{in} = 5V$		18	33	mA
$I_{CC(1)}$	Logical 1 level supply current $V_{CC} = 5V$ , $T_A = 25^{\circ}C$ , $V_{in} = 0$		6	12	mA

SWITCHING CHARACTERISTICS,  $V_{CC} = 5V$ ,  $T_A = 25^{\circ}C$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd0}$	Propagation delay time to logical 0 level $C_L = 15pF$ , $R_L = 400\Omega$		8	15	ns
$t_{pd1}$	Propagation delay time to logical 1 level $C_L = 15pF$ , $R_L = 4k\Omega$		40	55	ns

- \* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- \*\* All typical values are at  $V_{CC} = 5V$ ,  $T_A = 25^{\circ}C$

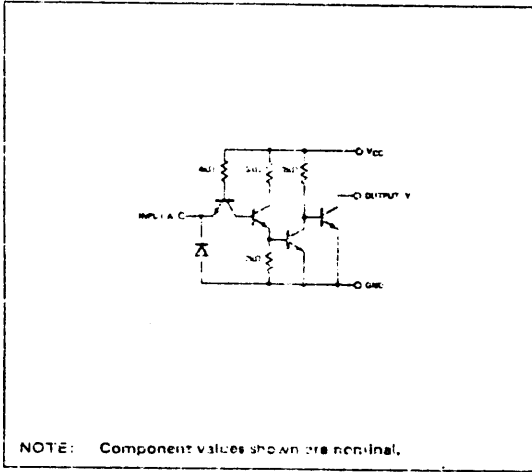
D COMPONENT DESCRIPTION  
D.6 INTEGRATED CIRCUITS

7407, 7417

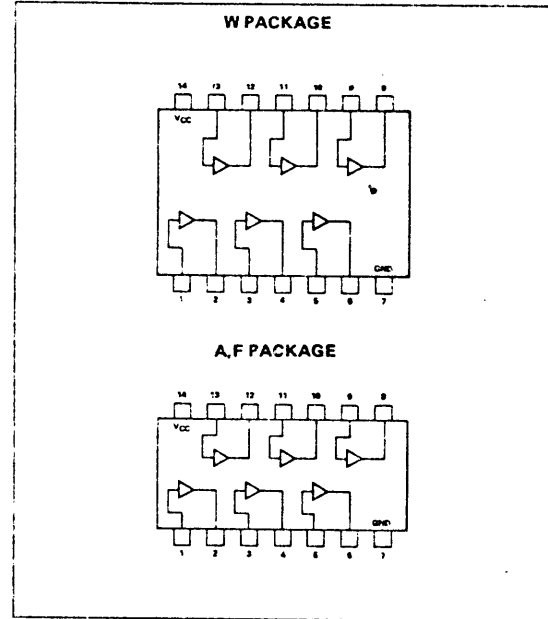
DESCRIPTION

The 54/7407 and 54/7417 Hex Buffer/Driver features standard TTL inputs with non-inverted high voltage, high current open collector outputs for interface with MOS, lamps or relays. The 54/7407 minimum output is 30 volts and the 54/7417 minimum output is 15 volts.

SCHEMATIC (each buffer/driver)



PIN CONFIGURATIONS



RECOMMENDED OPERATING CONDITIONS

	S5407, S5417			N7407, N7417			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
Output Voltage, $V_{OH}$ : S5407, N7407			30			30	V
S5417, N7417			15			15	V
Low-Level Output Current, $I_{OL}$			30			40	mA
Operating Free-Air Temperature Range, $T_A$	-55	25	125	0	25	70	$^{\circ}C$

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS *	MIN	TYP**	MAX	UNIT
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{OH}$	High-level output current	$V_{CC} = \text{MIN}, V_1 = 2V, V_{OH} = \text{MAX}$		250	$\mu A$
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}, V_1 = 0.8V, I_{OL} = \text{MAX}$		0.7	V
		$V_{CC} = \text{MIN}, V_1 = 0.8V, I_{OL} = 16\text{mA}$		0.4	V
$I_{IH}$	High-level input current (each input)	$V_{CC} = \text{MAX}, V_1 = 2.4V$		40	$\mu A$
		$V_{CC} = \text{MAX}, V_1 = 5.5V$		1	mA
$I_{IL}$	Low-level input current (each input)	$V_{CC} = \text{MAX}, V_1 = 0.4V$		-1.6	mA
$I_{CCH}$	Supply current, high-level output	$V_{CC} = \text{MAX}, V_1 = 5V$	29	41	mA
$I_{CCL}$	Supply current, low-level output	$V_{CC} = \text{MAX}, V_1 = 0$	21	30	mA

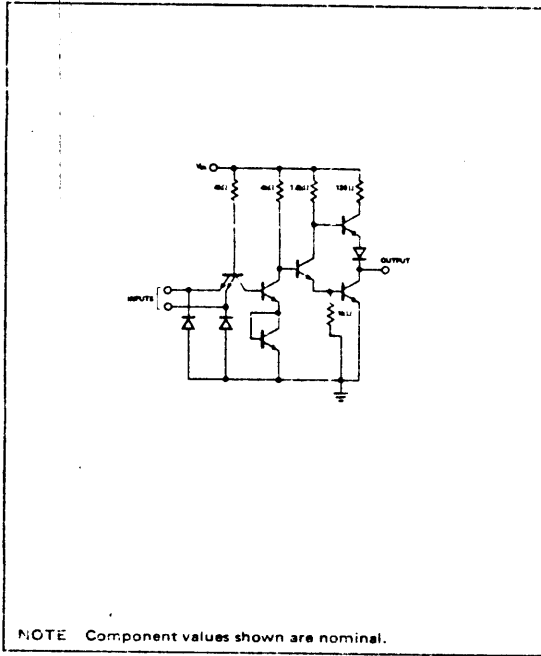
SWITCHING CHARACTERISTICS,  $V_{CC} = 5V, T_A = 25^{\circ}C$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time, low-to-high-level output	$C_L = 15\text{pF}, R_L = 110\Omega$	6	10	ns
$t_{PHL}$	Propagation delay time, high-to-low-level output	$C_L = 15\text{pF}, R_L = 110\Omega$	20	30	ns

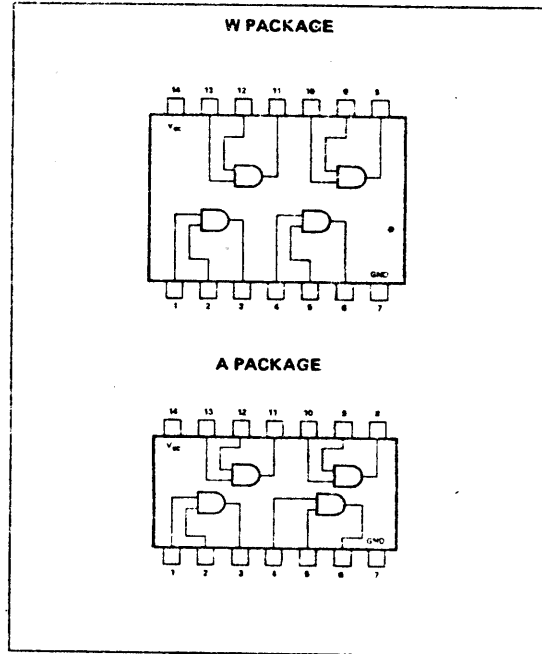
\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.  
\*\* All typical values are at  $V_{CC} = 5V, T_A = 25^{\circ}C$ .

7408

SCHEMATIC (each gate)



PIN CONFIGURATIONS



RECOMMENDED OPERATING CONDITIONS

Supply Voltage $V_{CC}$ : S5408 Circuits N7408 Circuits	MIN	NCM	MAX	UNIT
	4.5	5	5.5	V
Normalized Fan-Out from Output, N	4.75	5	5.25	V
			10	
Operating Free-Air Temperature Range, $T_A$ : S5408 Circuits N7408 Circuits	-55	25	125	$^{\circ}\text{C}$
	0	25	70	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 1 level at output	$V_{CC} = \text{MIN}$		2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 0 level at output	$V_{CC} = \text{MIN}$				0.8	V
$V_{out(1)}$	Logical 1 output voltage	$V_{CC} = \text{MIN}$ , $I_{load} = 800\mu\text{A}$	$V_{in} = 2.0\text{V}$	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	$V_{CC} = \text{MIN}$ , $I_{sink} = 16\text{mA}$	$V_{in} = 0.8\text{V}$		0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	$V_{CC} = \text{MAX}$	$V_{in} = 0.4\text{V}$			-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	$V_{CC} = \text{MAX}$ , $V_{CC} = \text{MAX}$	$V_{in} = 2.4\text{V}$ , $V_{in} = 5.5\text{V}$			40 1	$\mu\text{A}$ mA
$I_{OS}$	Short circuit output current†	$V_{CC} = \text{MAX}$		S5408 -20 N7408 -18		-55 -55	mA
$I_{CC(1)}$	Logical 1 level supply current	$V_{CC} = \text{MAX}$	$V_{in} = 5\text{V}$		10	15	mA
$I_{CC(0)}$	Logical 0 level supply current	$V_{CC} = \text{MAX}$	$V_{in} = 0$		18	26	mA

SWITCHING CHARACTERISTICS,  $V_{CC} = 5\text{V}$ ,  $T_A = 25^{\circ}\text{C}$ , N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{pd0}$	Propagation delay time to logical 0 level	$C_L = 15\text{pF}$	$R_L = 400\Omega$		12	19	ns
$t_{pd1}$	Propagation delay time to logical 1 level	$C_L = 15\text{pF}$	$R_L = 400\Omega$		17.5	27	ns

\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.  
\*\* All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^{\circ}\text{C}$   
† Not more than one output should be shorted at a time.

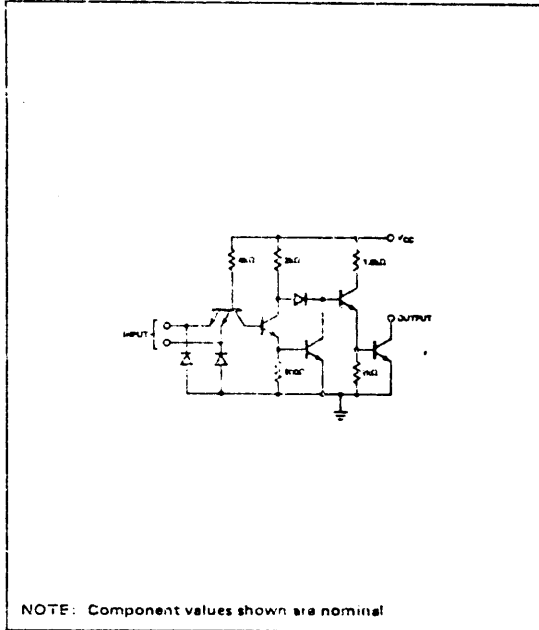
D COMPONENT DESCRIPTION  
 D.6 INTEGRATED CIRCUITS

7409

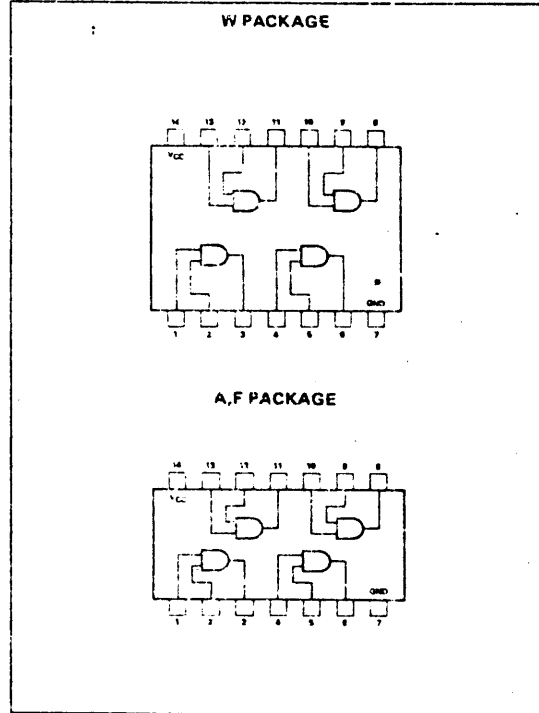
DESCRIPTION

The 54/7409 Quad 2-Input AND Gate with open collector outputs provides the capability of expanding AND logic functions.

SCHEMATIC (each gate)



PIN CONFIGURATIONS



RECOMMENDED OPERATING CONDITIONS

	5409			7409			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10			10	
Operating Free-Air Temperature Range, $T_A$	-55	25	125	0	25	70	$^{\circ}$ C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS *	MIN	TYP **	MAX	UNIT
$V_{IH}$	High-level input voltage		2		V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{OH}$	High-level output current	$V_{CC} = \text{MIN}, V_{IH} = 2V, V_{OH} = 5.5V$		250	$\mu$ A
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = 0.8V, I_{OL} = 16\text{mA}$		0.4	V
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX}, V_1 = 2.4V$		40	$\mu$ A
$I_{IH}$	(each input)	$V_{CC} = \text{MAX}, V_1 = 5.5V$		1	mA
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX}, V_1 = 0.4V$		-1.6	mA
$I_{CCH}$	Supply current, high-level output	$V_{CC} = \text{MAX}, V_1 = 5V$	10	15	mA
$I_{CCL}$	Supply current, low-level output	$V_{CC} = \text{MAX}, V_1 = 0$	18	26	mA

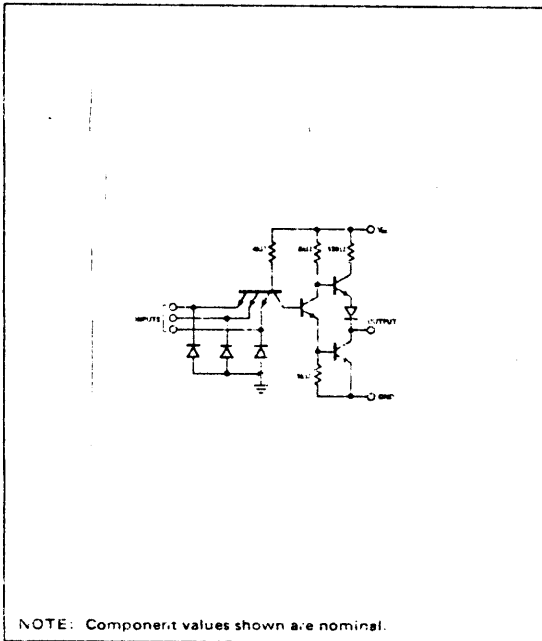
SWITCHING CHARACTERISTICS,  $V_{CC} = 5V, T_A = 25^{\circ}\text{C}, N = 10$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time, low-to-high-level output		21	32	ns
$t_{PHL}$	Propagation delay time, high-to-low-level output		16	24	ns

\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.  
 \*\* All typical values at  $V_{CC} = 5V, T_A = 25^{\circ}\text{C}$ .

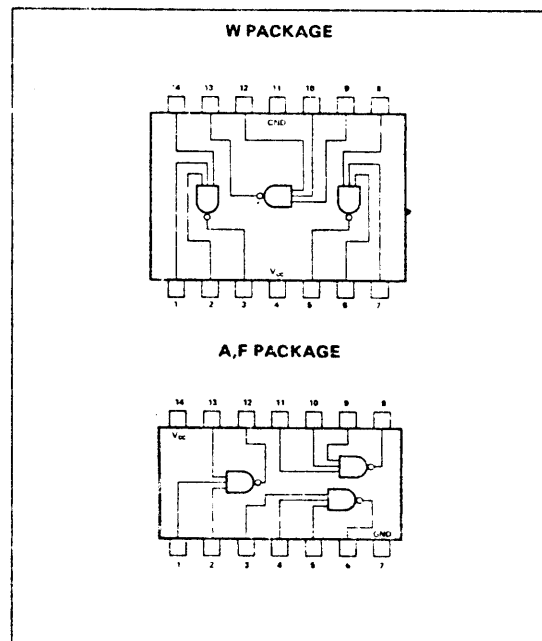
7410

SCHEMATIC (each gate)



NOTE: Component values shown are nominal.

PIN CONFIGURATIONS



RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage $V_{CC}$ : S5410 Circuits	4.5	5	5.5	V
N7410 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output, N			10	
Operating Free-Air Temperature Range, $T_A$ : S5410 Circuits	-55	25	125	$^{\circ}C$
N7410 Circuits	0	25	70	$^{\circ}C$

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	$V_{CC} = \text{MIN}$		2	V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	$V_{CC} = \text{MIN}$		0.8	V
$V_{out(1)}$	Logical 1 output voltage	$V_{CC} = \text{MIN}$ , $I_{load} = -400\mu A$	$V_{in} = 0.8V$	2.4 3.3	V
$V_{out(0)}$	Logical 0 output voltage	$V_{CC} = \text{MIN}$ , $I_{sink} = 16mA$	$V_{in} = 2V$	0.22 0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	$V_{CC} = \text{MAX}$	$V_{in} = 0.4V$	-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	$V_{CC} = \text{MAX}$ , $V_{CC} = \text{MAX}$	$V_{in} = 2.4V$ , $V_{in} = 5.5V$	40 1	$\mu A$ mA
$I_{OS}$	Short circuit output current†	$V_{CC} = 5.5V$	S5410 N7410	-20 -18	mA
$I_{CC(0)}$	Logical 0 level supply current	$V_{CC} = \text{MAX}$	$V_{in} = 5V$	9 16.5	mA
$I_{CC(1)}$	Logical 1 level supply current	$V_{CC} = \text{MAX}$	$V_{in} = 0$	3 6	mA

SWITCHING CHARACTERISTICS,  $V_{CC} = 5V$ ,  $T_A = 25^{\circ}C$ , N = 10

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd0}$	Propagation delay time to logical 0 level	$C_L = 15pF$ , $R_L = 400\Omega$	7	15	ns
$t_{pd1}$	Propagation delay time to logical 1 level	$C_L = 15pF$ , $R_L = 400\Omega$	11	22	ns

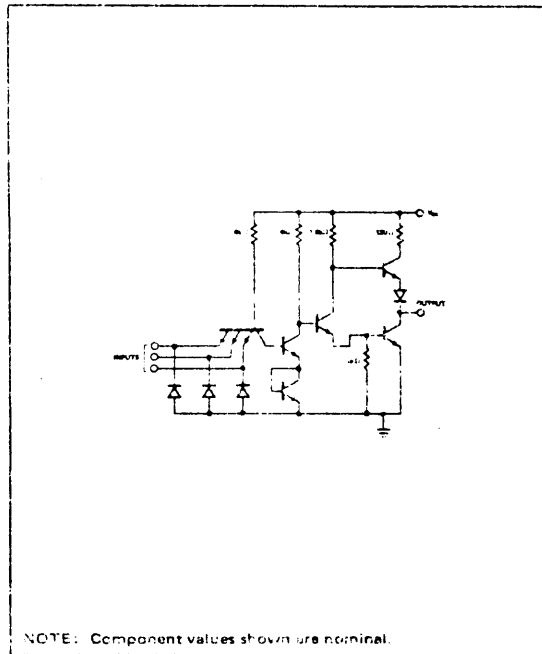
\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

\*\* All typical values are at  $V_{CC} = 5V$ ,  $T_A = 25^{\circ}C$ .

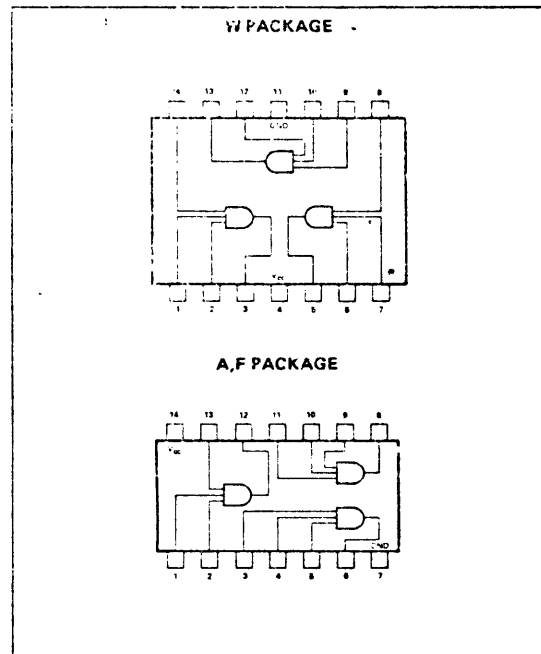
† Not more than one output should be shorted at a time.

7411

SCHEMATIC DIAGRAM



PIN CONFIGURATIONS



RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage $V_{CC}$ : S5411 Circuits	4.5	5	5.5	V
N7411 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output, N			10	
Operating Free-Air Temperature Range, $T_A$ : S5411 Circuits	-55	25	125	$^{\circ}C$
N7411 Circuits	0	25	70	$^{\circ}C$

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT	
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 1 level at output	$V_{CC} = \text{MIN}$			V	
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 0 level at output	$V_{CC} = \text{MIN}$		0.8	V	
$V_{out(1)}$	Logical 1 output voltage	$V_{CC} = \text{MIN}$ $I_{load} = -200\mu A$	$V_{in} = 2.0V$ , 2.4	3.3	V	
$V_{out(0)}$	Logical 0 output voltage	$V_{CC} = \text{MIN}$ $I_{sink} = 10mA$	$V_{in} = 0.8V$ , 0.22	0.4	V	
$I_{in(0)}$	Logical 0 level input current (each input)	$V_{CC} = \text{MAX}$	$V_{in} = 0.4V$	-1.6	mA	
$I_{in(1)}$	Logical 1 level input current (each input)	$V_{CC} = \text{MAX}$ $V_{CC} = \text{MAX}$	$V_{in} = 2.4V$ $V_{in} = 5.5V$	40 1	$\mu A$ mA	
$I_{OS}$	Short circuit output current†	$V_{CC} = \text{MAX}$	S5411 N7411	-20 -18	-55 -55	mA
$I_{CC(1)}$	Logical 1 level supply current	$V_{CC} = \text{MAX}$ , current	$V_{in} = 5V$	7.5	12	mA
$I_{CC(0)}$	Logical 0 level supply current	$V_{CC} = \text{MAX}$ , current	$V_{in} = 0$	13.5	20	mA

SWITCHING CHARACTERISTICS,  $V_{CC} = 5V$ ,  $T_A = 25^{\circ}C$ ,  $N = 10$

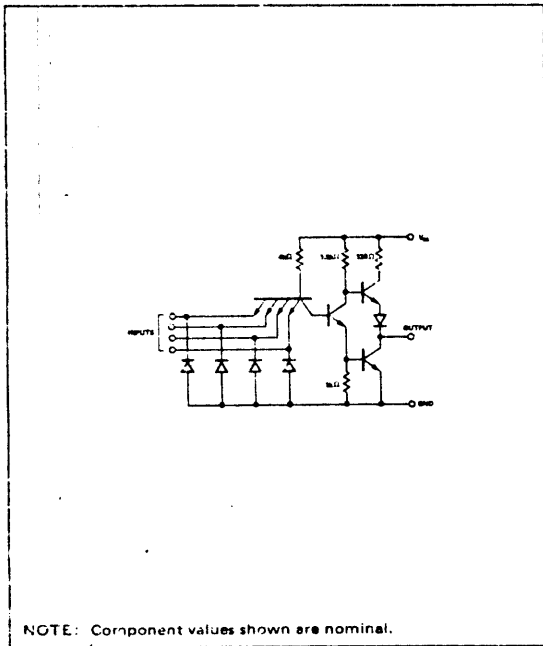
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd0}$	Propagation delay time to logical 0 level	$C_L = 15pF$ , $R_L = 400\Omega$	12	19	ns
$t_{pd1}$	Propagation delay time to logical 1 level	$C_L = 15pF$ , $R_L = 400\Omega$	17.5	27	ns

\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.  
\*\* All typical values are at  $V_{CC} = 5V$ ,  $T_A = 25^{\circ}C$   
† Not more than one output should be shorted at a time.

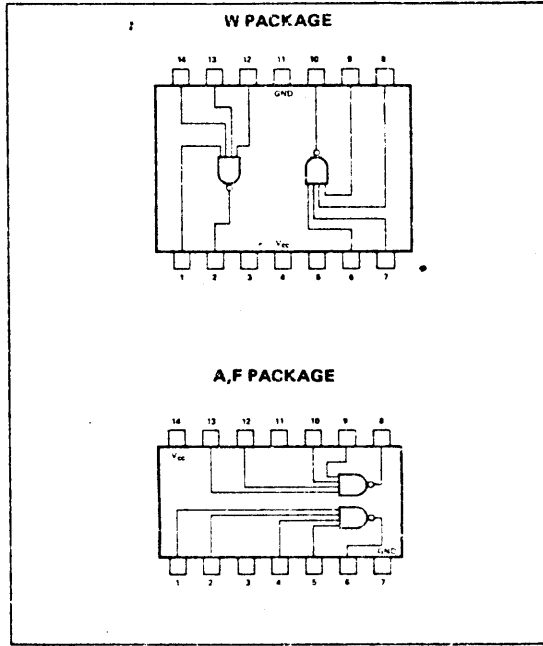


7420

SCHEMATIC (each gate)



PIN CONFIGURATIONS



RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage $V_{CC}$ : S5420 Circuits	4.5	5	5.5	V
N7420 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output, $N$			10	
Operating Free-Air Temperature Range, $T_A$ : S5420 Circuits	-55	25	125	$^{\circ}$ C
N7420 Circuits	0	25	70	$^{\circ}$ C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT	
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	$V_{CC} = \text{MIN}$	2		V	
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	$V_{CC} = \text{MIN}$		0.8	V	
$V_{out(1)}$	Logical 1 output voltage	$V_{CC} = \text{MIN}$ , $I_{load} = -400\mu\text{A}$	$V_{in} = 0.8\text{V}$ , 2.4	3.3	V	
$V_{out(0)}$	Logical 0 output voltage	$V_{CC} = \text{MIN}$ , $I_{sink} = 16\text{mA}$	$V_{in} = 2\text{V}$ , 0.22	0.4	V	
$I_{i(0)}$	Logical 0 level input current (each input)	$V_{CC} = \text{MAX}$ , $V_{in} = 0.4\text{V}$		-1.6	mA	
$I_{i(1)}$	Logical 1 level input current (each input)	$V_{CC} = \text{MAX}$ , $V_{CC} = \text{MAX}$ , $V_{in} = 2.4\text{V}$ , $V_{in} = 5.5\text{V}$		40 1	$\mu\text{A}$ mA	
$I_{OS}$	Short circuit output current†	$V_{CC} = \text{MAX}$ , $V_{in} = 5\text{V}$	S5420 N7420	-20 -18	-55 -55	mA
$I_{CC(0)}$	Logical 0 level supply current	$V_{CC} = \text{MAX}$ , $V_{in} = 5\text{V}$		6	11	mA
$I_{CC(1)}$	Logical 1 level supply current	$V_{CC} = \text{MAX}$ , $V_{in} = 0$		2	4	mA

SWITCHING CHARACTERISTICS,  $V_{CC} = 5\text{V}$ ,  $T_A = 25^{\circ}\text{C}$ ,  $N = 10$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd0}$	Propagation delay time to logical 0 level	$C_L = 15\text{pF}$ , $R_L = 400\Omega$	8	15	ns
$t_{pd1}$	Propagation delay time to logical 1 level	$C_L = 15\text{pF}$ , $R_L = 400\Omega$	12	22	ns

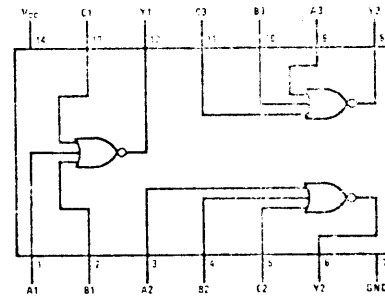
\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

\*\* All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^{\circ}\text{C}$ .

† Not more than one output should be shorted at a time.

D COMPONENT DESCRIPTION  
D.6 INTEGRATED CIRCUITS

7427



5427/7427(J), (N) (W); 54LS27/74LS27(J), (N) (W)

Supply Currents

DEVICE	I <sub>CCH</sub> (mA) Total With Outputs High		I <sub>CCL</sub> (mA) Total With Outputs Low	
	TYP	MAX	TYP	MAX
02	8	16	14	27
25	8	16	10	19
27	10	16	16	26
L02	0.3	1.6	1.4	2.6
LS02	1.6	3.2	2.8	5.4
LS27	2.0	4	3.4	6.8
S02	17	29	26	45
S260	17	29	26	45

Switching Characteristics at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C

DEVICE	CONDITIONS	t <sub>PLH</sub> (ns) Propagation Delay Time, Low-To-High Level Output			t <sub>PHL</sub> (ns) Propagation Delay Time, High-To-Low Level Output		
		MIN	TYP	MAX	MIN	TYP	MAX
02	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 400Ω	12	22	8	15		
25		13	22	8	15		
27		7	11	10	15		
L02	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 4 kΩ	31	60	35	60		
LS02, LS27	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ	10	15	10	15		
S02	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 280Ω	3.5	5.5	3.5	5.5		
	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 280Ω	5	7.5	5	7.5		
S260	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 280Ω	4	5.5	4	6		

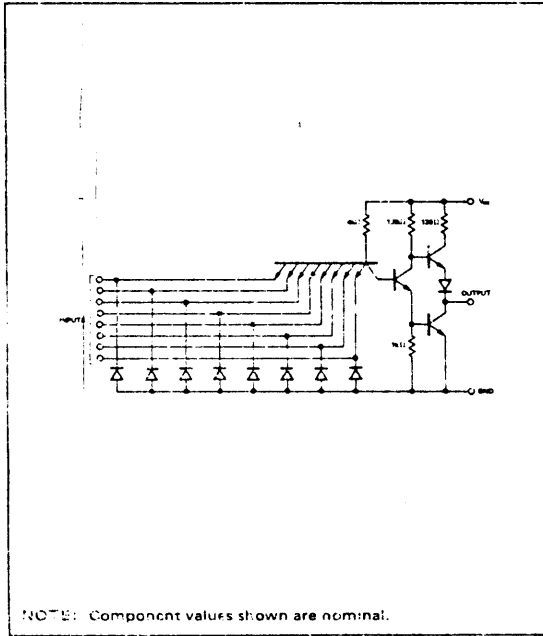
Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER	CONDITIONS	DM54/74		DM54L/74L		DM54LS/74LS			DM74S			UNITS	
		02, 25, 27		L02		LS02, LS27			S02, S260				
		MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN		TYP(1)
V <sub>IH</sub>	High Level Input Voltage	2		2		2			2			V	
V <sub>IL</sub>	Low Level Input Voltage	0.8		0.7		0.7			N/A			V	
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min	I <sub>I</sub> = 10 mA	1.5		N/A			N/A			V	
			I <sub>I</sub> = 15 mA	N/A		1.5			1.2				
I <sub>OH</sub>	High Level Output Current	25, 27		800		200			-400			μA	
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min V <sub>IL</sub> = Max I <sub>OH</sub> = Max	LS27		2.4		2.4			N/A			V
			Others		DM54	2.4	3.4	DM74	2.4	3.2	LS02, LS27	2.5	3.4
I <sub>OL</sub>	Low Level Output Current	DM54		16		2			4			N/A	
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min V <sub>IH</sub> = 2V	I <sub>OL</sub> = Max	DM54	0.2	0.4	DM74	0.15	0.3	LS02, LS27	0.25	0.4	N/A
			I <sub>OL</sub> = 1 mA	DM74	0.2	0.4	DM74	0.2	0.4	LS02, LS27	0.35	0.5	0.5
I <sub>I</sub>	Input Current at Maximum Input Voltage	V <sub>CC</sub> = Max	V <sub>I</sub> = 5.5V V <sub>I</sub> = 7V	1		0.1			0.1			mA	
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = Max	Fast Edge Strobe of 25	40		10			N/A			μA	
			All Inputs	V <sub>I</sub> = 2.7V	160		N/A			20			50
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = Max	All Inputs	V <sub>I</sub> = 0.4V		0.18			N/A			mA	
			Fast Edge Strobe of 25	V <sub>I</sub> = 0.4V	1.6		0.36			N/A			
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (2)	DM54	20	55	-3	-15	-30	-130	N/A	mA		
			DM74	18	55	3	-15	-30	-130	40	-100		
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = Max	See Table										

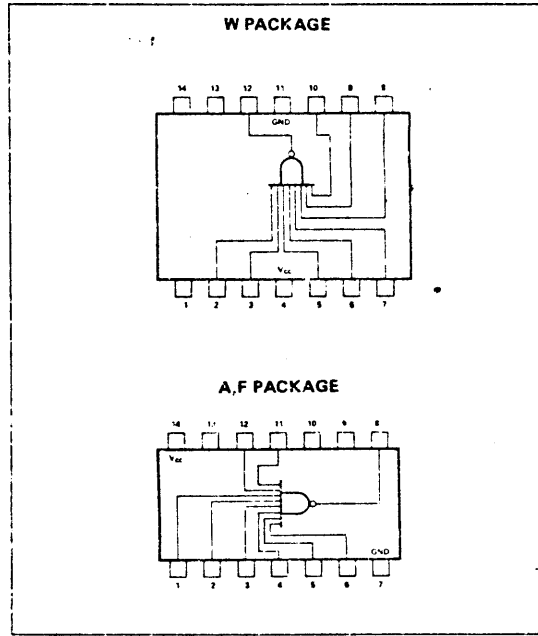
Note:  
(1) All typical values are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.  
(2) For the minimum see output should be shorted at a time, per for DM54LS, DM74LS and DM74S, duration of short circuit should not exceed one second.  
(3) Commercial Semiconductors temporarily reserve the right to specify DM54/DM74LS02, LS27 and DM74S to have a maximum I<sub>OS</sub> = 5.0 mA.

7430

**SCHEMATIC DIAGRAM**



**PIN CONFIGURATIONS**



**RECOMMENDED OPERATING CONDITIONS**

	MIN	NOM	MAX	UNIT
Supply Voltage $V_{CC}$ : S5430 Circuits	4.5	5	5.5	V
N7430 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output, N			10	
Operating Free-Air Temperature Range, $T_A$ : S5430 Circuits	-55	25	125	$^{\circ}C$
N7430 Circuits	0	25	70	$^{\circ}C$

**ELECTRICAL CHARACTERISTICS** (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS *	MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	$V_{CC} = \text{MIN}$	2		V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	$V_{CC} = \text{MIN}$		0.8	V
$V_{out(1)}$	Logical 1 output voltage	$V_{CC} = \text{MIN}$ , $I_{load} = -400\mu A$	2.4	3.3	V
$V_{out(0)}$	Logical 0 output voltage	$V_{CC} = \text{MIN}$ , $I_{sink} = 16\text{mA}$	0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	$V_{CC} = \text{MAX}$ , $V_{in} = 0.4\text{V}$		-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	$V_{CC} = \text{MAX}$ , $V_{CC} = \text{MAX}$ , $V_{in} = 2.4\text{V}$ , $V_{in} = 5.5\text{V}$		40 1	$\mu A$ mA
$I_{OS}$	Short circuit output current †	$V_{CC} = \text{MAX}$ , S5430 N7430	-20 -18	-55 -55	mA
$I_{CC(0)}$	Logical 0 level supply current	$V_{CC} = \text{MAX}$ , $V_{in} = 5\text{V}$		3	6 mA
$I_{CC(1)}$	Logical 1 level supply current	$V_{CC} = \text{MAX}$ , $V_{in} = 0$		1	2 mA

**SWITCHING CHARACTERISTICS**,  $V_{CC} = 5\text{V}$ ,  $T_A = 25^{\circ}C$ , N = 10

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd0}$	Propagation delay time to logical 0 level $C_L = 15\text{pF}$ , $R_L = 400\Omega$		8	15	ns
$t_{pd1}$	Propagation delay time to logical 1 level $C_L = 15\text{pF}$ , $R_L = 400\Omega$		13	22	ns

\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

\*\* All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^{\circ}C$ .

† Not more than one output should be shorted at a time.

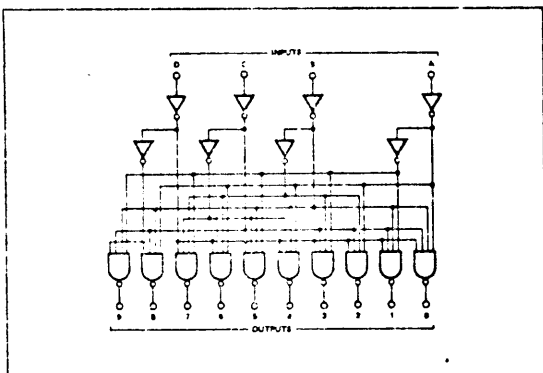
D COMPONENT DESCRIPTION  
D.6 INTEGRATED CIRCUITS

7442

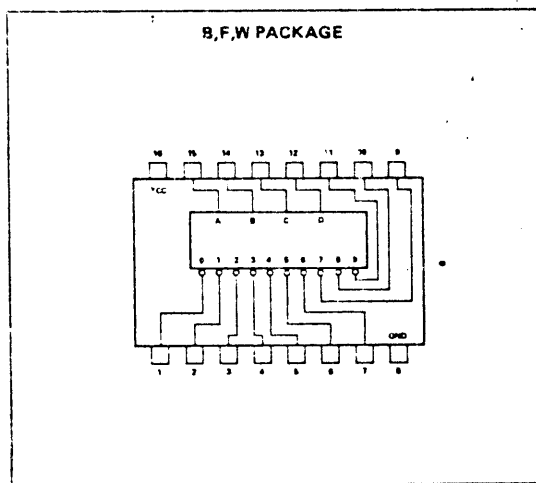
DESCRIPTION

The 54/7442 BCD-to-Decimal Decoder is a TTL MSI array utilized in decoding and logic conversion applications. The 54/7442 decodes a four bit BCD number to one of ten outputs.

LOGIC DIAGRAM



PIN CONFIGURATIONS



TRUTH TABLE

S5442/N7442 BCD INPUT				ALL TYPES DECIMAL OUTPUT									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	1	1	1	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	1	1	1
0	0	1	0	1	1	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1	1	1
0	1	0	0	1	1	1	1	1	1	1	1	1	1
0	1	0	1	1	1	1	1	1	1	1	1	1	1
0	1	1	0	1	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	1	1	1	1	1	1
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
$V_{in(1)}$ Input voltage required to ensure logical 1 at any input terminal	$V_{CC} = \text{MIN}$	2			V
$V_{in(0)}$ Input voltage required to ensure logical 0 at any input terminal	$V_{CC} = \text{MIN}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	$V_{CC} = \text{MIN}, V_{in(1)} = 2V, V_{in(0)} = 0.8V, I_{load} = -400\mu A$	2.4			V
$V_{out(0)}$ Logical 0 output voltage	$V_{CC} = \text{MIN}, V_{in(1)} = 2V, V_{in(0)} = 0.8V, I_{sink} = 16mA$			0.4	V
$I_{in(1)}$ Logical 1 level input current (each input)	$V_{CC} = \text{MAX}, V_{in} = 2.4V$			40	$\mu A$
	$V_{CC} = \text{MAX}, V_{in} = 5.5V$			1	mA
$I_{in(0)}$ Logical 0 level input current (each input)	$V_{CC} = \text{MAX}, V_{in} = 0.4V$			-1.6	mA
$I_{OS}$ Short-circuit output current†	$V_{CC} = \text{MAX},$ S5442	-20		-55	mA
	N7442	-18		-55	mA
	S5442		28	41	mA
$I_{CC}$ Supply current	$V_{CC} = \text{MAX},$ N7442		28	56	mA

D COMPONENT DESCRIPTION  
 D.6 INTEGRATED CIRCUITS

7442 cont'd

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage $V_{CC}$ : S5442 Circuits	4.5	5	5.5	V
N7442 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10	

SWITCHING CHARACTERISTICS,  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $N = 10$

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{pd0}$	Propagation delay time to logical 0 level through two logic levels	$C_L = 15pF$ ,	$R_L = 400\Omega$	10	22	30	ns
$t_{pd0}$	Propagation delay time to logical 0 level through three logic levels	$C_L = 15pF$ ,	$R_L = 400\Omega$		23	35	ns
$t_{pd1}$	Propagation delay time to logical 1 level through two logic levels	$C_L = 15pF$ ,	$R_L = 400\Omega$	10	17	25	ns
$t_{pd1}$	Propagation delay time to logical 1 level through three logic levels	$C_L = 15pF$ ,	$R_L = 400\Omega$		26	35	ns

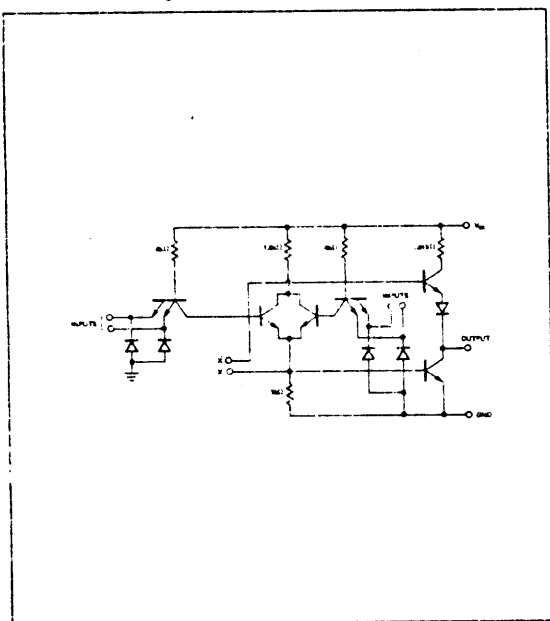
\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

\*\* All typical values are at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ .

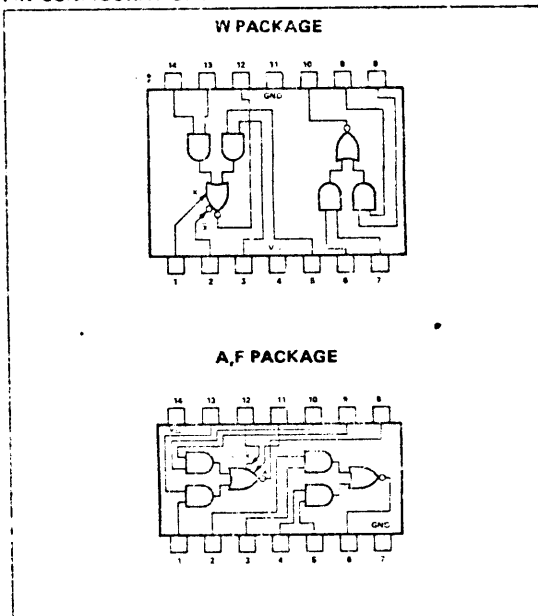
† Not more than one output should be shorted at a time.

7451

SCHEMATIC (each gate)



PIN CONFIGURATIONS



NOTES:

- Component values shown are nominal.
- Both expander inputs are used simultaneously for expanding.
- If expander is not used, leave X and  $\bar{X}$  pins open.

- Make no external connection to X and  $\bar{X}$  pins of the S5451 and N7451.
- A total of four expander gates can be connected to the expander inputs.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage $V_{CC}$ : S5450, S5451 Circuits	4.5	5	5.5	V
N7450, N7451 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output, N			10	
Operating Free-Air Temperature Range, $T_A$ : S5450, S5451 Circuits	-55	25	125	$^\circ C$
N7450, N7451 Circuits	0	25	70	$^\circ C$

7451 cont'd

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 at output	$V_{CC} = \text{MIN}$		2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	$V_{CC} = \text{MIN}$				0.8	V
$V_{out(1)}$	Logical 1 output voltage	$V_{CC} = \text{MIN}$ , $I_{load} = -400\mu\text{A}$	$V_{in} = 0.8\text{V}$	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	$V_{CC} = \text{MIN}$ , $I_{sink} = 16\text{mA}$	$V_{in} = 2\text{V}$		0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	$V_{CC} = \text{MAX}$ ,	$V_{in} = 0.4\text{V}$			-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	$V_{CC} = \text{MAX}$ ,	$V_{in} = 2.4\text{V}$			40	$\mu\text{A}$
		$V_{CC} = \text{MAX}$ ,	$V_{in} = 5.5\text{V}$			1	mA
$I_{OS}$	Short circuit output current†	$V_{CC} = \text{MAX}$	S5450, S5451 N7450, N7451	-20		-55	mA
				-18		-55	mA
$I_{CC(0)}$	Logical 0 level supply current	$V_{CC} = \text{MAX}$ ,	$V_{in} = 5\text{V}$		7.4	14	mA
$I_{CC(1)}$	Logical 1 level supply current	$V_{CC} = \text{MAX}$ ,	$V_{in} = 0$		4	8	mA

ELECTRICAL CHARACTERISTICS (S5450 circuits) using expander inputs,  $V_{CC} = 4.5\text{V}$ ,  $T_A = -55^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP**	MAX	UNIT
$I_X$	Expander current	$V_1 = 0.4\text{V}$ ,	$I_{sink} = 16\text{mA}$			2.9	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	$I_{sink} = 16\text{mA}$ , $R_1 = 0$	$I_1 = 0.41\text{mA}$			1	V
$V_{out(1)}$	Logical 1 output voltage	$I_{load} = -400\mu\text{A}$ , $I_2 = -0.15\text{mA}$	$I_1 = 0.15\text{mA}$	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	$I_{sink} = 16\text{mA}$ , $R_1 = 138\Omega$	$I_1 = 0.3\text{mA}$		0.22	0.4	V

ELECTRICAL CHARACTERISTICS (N7450 circuits) using expander inputs,  $V_{CC} = 4.75\text{V}$ ,  $T_A = 0^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP**	MAX	UNIT
$I_X$	Expander current	$V_1 = 0.4\text{V}$ ,	$I_{sink} = 16\text{mA}$			3.1	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	$I_{sink} = 16\text{mA}$ , $R_1 = 0$	$I_1 = 0.52\text{mA}$			1	V
$V_{out(1)}$	Logical 1 output voltage	$I_{load} = -400\mu\text{A}$ , $I_2 = -270\mu\text{A}$	$I_1 = 270\mu\text{A}$	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	$I_{sink} = 16\text{mA}$ , $R_1 = 139\Omega$	$I_1 = 0.43\text{mA}$		0.22	0.4	V

SWITCHING CHARACTERISTICS,  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ ,  $H = 10$

PARAMETER		TEST CONDITIONS*		MIN	TYP	MAX	UNIT
$t_{pd0}$	Propagation delay time to logical 0 level	$C_L = 15\text{pF}$ ,	$R_L = 400\Omega$		8	15	ns
$t_{pd1}$	Propagation delay time to logical 1 level	$C_L = 15\text{pF}$ ,	$P_L = 400\Omega$		13	22	ns

\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander inputs X and X are open.

\*\* All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ .

† Not more than one output should be shorted at a time.

D COMPONENT DESCRIPTION  
 D.6 INTEGRATED CIRCUITS

7474

DESCRIPTION

The 55474/N7474 is a monolithic, dual, D-type, edge-triggered flip-flop featuring direct clear and preset inputs and complementary Q and  $\bar{Q}$  outputs. Input information is transferred to the Q output on the positive edge of the clock pulse.

Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the clock input threshold voltage has been passed, the data input (D) is locked out.

TRUTH TABLE

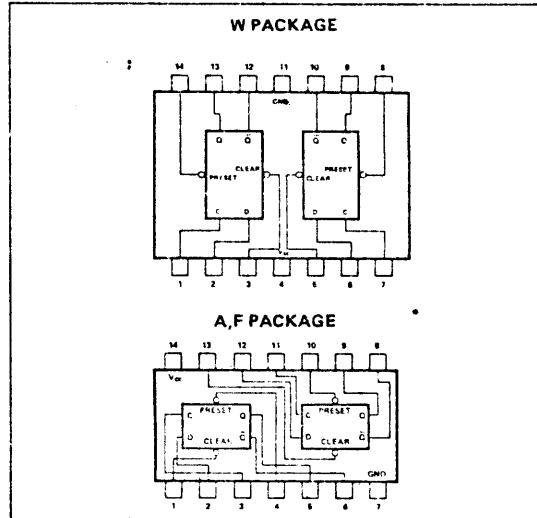
$D_n$	$Q_{n+1}$	$\bar{Q}_{n+1}$
1	1	0
0	0	1

Preset	Clear	Q
1	1	Q
1	0	0
0	1	1
0	0	†

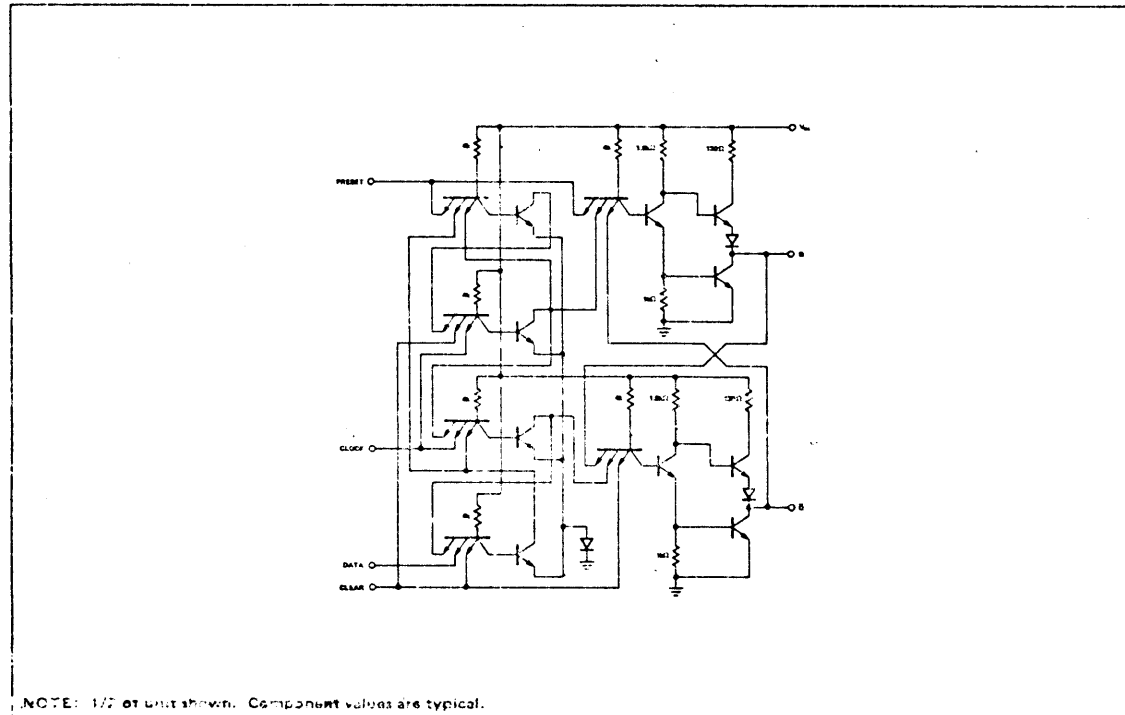
† Both outputs in 1 state  
 n is time prior to clock  
 n+1 is time following clock

PIN CONFIGURATIONS



POSITIVE LOGIC — Low input to preset sets Q to logical 1  
 Low input to clear sets Q to logical 0; Preset and clear are independent of clock

SCHEMATIC DIAGRAM



NOTE: 1/2 of unit shown. Component values are typical.

D COMPONENT DESCRIPTION  
D.6 INTEGRATED CIRCUITS

7474 cont'd

RECOMMENDED OPERATING CONDITIONS

	MIN	NGM	MAX	UNIT
Supply Voltage $V_{CC}$ : S5474 Circuits	4.5	5	5.5	V
N7474 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, $T_A$ : S5474 Circuits	-55	25	125	$^{\circ}$ C
N7474 Circuits	0	25	70	$^{\circ}$ C
Normalized Fan-Out from each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$	30			ns
*Width of Preset Pulse, $t_{p(preset)}$	30			ns
Width of Clear Pulse, $t_{p(clear)}$	30			ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal $V_{CC} = \text{MIN}$	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal $V_{CC} = \text{MIN}$			0.8	V
$V_{out(1)}$	Logical 1 output voltage $V_{CC} = \text{MIN}$ , $I_{load} = -400\mu\text{A}$	2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage $V_{CC} = \text{MIN}$ , $I_{sink} = 16\text{mA}$		0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at preset or D $V_{CC} = \text{MAX}$ , $V_{in} = 0.4\text{V}$			-1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock $V_{CC} = \text{MAX}$ , $V_{in} = 0.4\text{V}$			-3.2	mA
$I_{in(1)}$	Logical 1 level input current at D $V_{CC} = \text{MAX}$ , $V_{in} = 2.4\text{V}$ $V_{CC} = \text{MAX}$ , $V_{in} = 5.5\text{V}$			40 1	$\mu\text{A}$ mA
$I_{in(1)}$	Logical 1 level input current at preset or clock $V_{CC} = \text{MAX}$ , $V_{in} = 2.4\text{V}$ $V_{CC} = \text{MAX}$ , $V_{in} = 5.5\text{V}$			80 1	$\mu\text{A}$ mA
$I_{in(1)}$	Logical 1 level input current at clear $V_{CC} = \text{MAX}$ , $V_{in} = 2.4\text{V}$ $V_{CC} = \text{MAX}$ , $V_{in} = 5.5\text{V}$			120 1	$\mu\text{A}$ mA
$I_{OS}$	Short circuit output current† $V_{CC} = \text{MAX}$ , $V_{in} = 0$	S5474 N7474		-20 -57	mA
$I_{CC}$	Supply current $V_{CC} = \text{MAX}$ , $V_{in} = 5\text{V}$			-18 17	mA

SWITCHING CHARACTERISTICS:  $V_{CC} = 5\text{V}$ ,  $T_A = 25^{\circ}\text{C}$ , N = 10

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{clock}$	Maximum clock frequency $C_L = 15\text{pF}$ , $R_L = 400\Omega$	15	25		MHz
$t_{setup}$	Minimum input setup time $C_L = 15\text{pF}$ , $R_L = 400\Omega$		15	20	ns
$t_{hold}$	Minimum input hold time $C_L = 15\text{pF}$ , $R_L = 400\Omega$		2	5	ns
$t_{pd1}$	Propagation delay time to logical 1 level from clear or preset to output $C_L = 15\text{pF}$ , $R_L = 400\Omega$			25	ns
$t_{pd0}$	Propagation delay time to logical 0 level from clear or preset to output $C_L = 15\text{pF}$ , $R_L = 400\Omega$			40	ns
$t_{pd1}$	Propagation delay time to logical 1 level from clock to output $C_L = 15\text{pF}$ , $R_L = 400\Omega$	10	14	25	ns
$t_{pd0}$	Propagation delay time to logical 0 level from clock to output $C_L = 15\text{pF}$ , $R_L = 400\Omega$	10	20	40	ns

\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

\*\* All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^{\circ}\text{C}$ .

† Not more than one output should be shorted at a time.



D COMPONENT DESCRIPTION  
 D.6 INTEGRATED CIRCUITS

7483

DESCRIPTION

The 547483 is a 4-Bit Binary Full Adder for adding two four bit binary numbers. A Carry Look Ahead circuit is included to provide minimum carry propagation delays.

Propagation delays of carry-in to carry-out is typically 12 nsec.

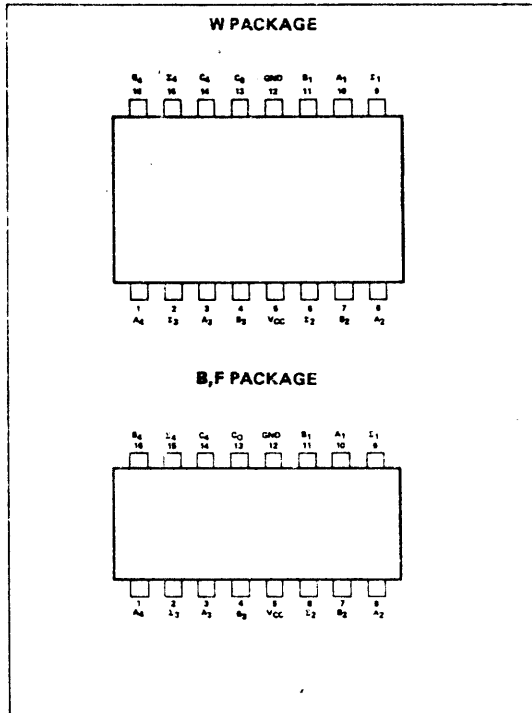
TRUTH TABLE

INPUT				OUTPUT							
				WHEN $C_0 = 0$				WHEN $C_0 = 1$			
				WHEN $C_2 = 0$				WHEN $C_2 = 1$			
$A_1$	$B_1$	$A_2$	$B_2$	$\Sigma_1$	$\Sigma_2$	$C_2$	$\Sigma_1$	$\Sigma_2$	$C_2$		
$A_3$	$B_3$	$A_4$	$B_4$	$\Sigma_3$	$\Sigma_4$	$C_4$	$\Sigma_3$	$\Sigma_4$	$C_4$		
0	0	0	0	0	0	0	1	0	0		
1	0	0	0	1	0	0	0	1	0		
0	1	0	0	1	0	0	0	1	0		
1	1	0	0	0	1	0	1	1	0		
0	0	1	0	0	1	0	1	1	0		
1	0	1	0	1	1	0	0	0	1		
0	1	1	0	1	1	0	0	0	1		
1	1	1	0	0	0	1	1	0	1		
0	0	0	1	0	1	0	1	1	0		
1	0	0	1	1	1	0	0	0	1		
0	1	0	1	1	1	0	0	0	1		
1	1	0	1	0	0	1	1	0	1		
0	0	1	1	0	0	1	1	0	1		
1	0	1	1	1	1	0	0	1	1		
0	1	1	1	1	1	0	1	1	1		
1	1	1	1	0	1	1	1	1	1		

NOTES:

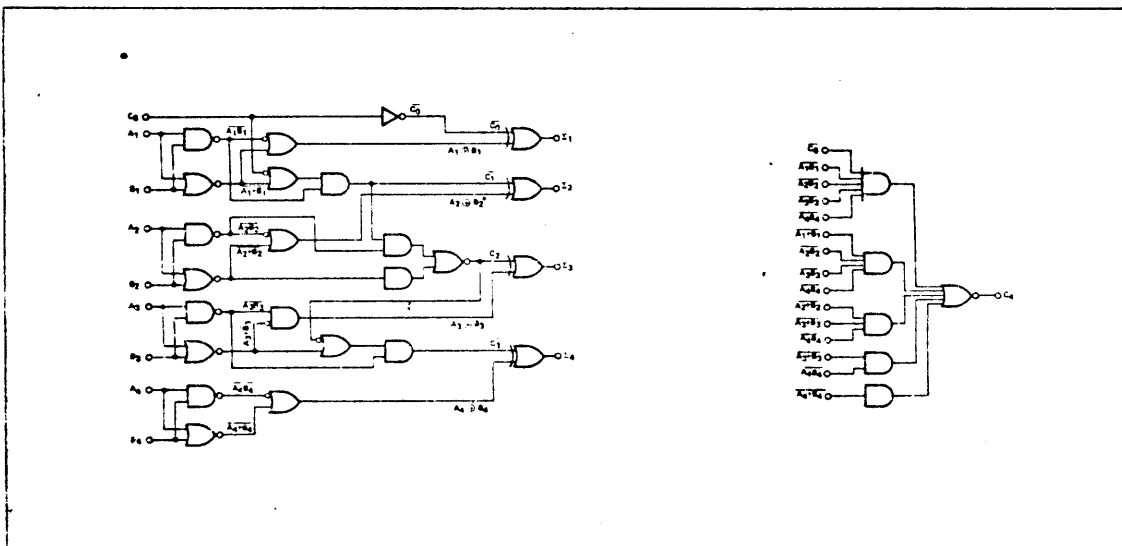
Input conditions at  $A_1, A_2, B_1, B_2$ , and  $C_0$  are used to determine outputs  $\Sigma_1$  and  $\Sigma_2$ , and the value of the internal carry  $C_2$ . The

PIN CONFIGURATIONS



values at  $C_2, A_3, B_3, A_4$ , and  $B_4$ , are then used to determine outputs  $\Sigma_3, \Sigma_4$ , and  $C_4$ .

LOGIC DIAGRAM



D COMPONENT DESCRIPTION  
D.6 INTEGRATED CIRCUITS

7483 cont'd

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage $V_{CC}$ : (See Note 1) S5483 Circuits	4.5	5	5.5	V
N7483 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Outputs: $C_4$			5	
$\Sigma_1, \Sigma_2, \Sigma_3$ or $\Sigma_4$			10	

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
$V_{in(1)}$ Input voltage required to ensure logical 1 at any input terminal	$V_{CC} = \text{MIN}$	2			V
$V_{in(0)}$ Input voltage required to ensure logical 0 at any input terminal	$V_{CC} = \text{MIN}$			0.8 <sup>†</sup>	V
$V_{out(1)}$ Logical 1 output voltage	$V_{CC} = \text{MIN}$	2.4			V
$V_{out(0)}$ Logical 0 output voltage	$V_{CC} = \text{MIN}$			0.4	V
$I_{in(0)}$ Logical 0 level input current at $A_1, A_3, B_1, B_3$ , or $C_0$	$V_{CC} = \text{MAX}, V_{in} = 0.4\text{V}$			-3.2	mA
$I_{in(0)}$ Logical 0 level input current at $A_2, A_4, B_2$ , or $B_4$	$V_{CC} = \text{MAX}, V_{in} = 0.4\text{V}$			-1.6	mA
$I_{in(1)}$ Logical 1 level input current at $A_1, A_3, B_1, B_3$ , or $C_0$	$V_{CC} = \text{MAX}, V_{in} = 2.4\text{V}$			80	$\mu\text{A}$
$I_{in(1)}$ Logical 1 level input current at $A_2, A_4, B_2$ , or $B_4$	$V_{CC} = \text{MAX}, V_{in} = 5.5\text{V}$			1	mA
$I_{in(1)}$ Logical 1 level input current at $A_1, A_3, B_1, B_3$ , or $C_0$	$V_{CC} = \text{MAX}, V_{in} = 2.4\text{V}$			40	$\mu\text{A}$
$I_{in(1)}$ Logical 1 level input current at $A_2, A_4, B_2$ , or $B_4$	$V_{CC} @ \text{MAX}, V_{in} = 5.5\text{V}$			1	mA
$I_{OS}$ Short-circuit output current at $\Sigma_1, \Sigma_2, \Sigma_3$ , or $\Sigma_4$ †	$V_{CC} = \text{MAX}$ S5483	-20		-55	mA
	N7483	-18		-55	mA
$I_{OS}$ Short-circuit output current at $C_4$ †	$V_{CC} = \text{MAX}$ S5483	-20		-70	mA
	N7483	-18		-70	mA
$I_{CC}$ Supply current	$V_{CC} = \text{MAX}$ ,		58	79	mA

SWITCHING CHARACTERISTICS,  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted N = 10

PARAMETER ‡	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd1}$ From $C_0$ to 1	$C_L = 50\text{pF}, R_L = 400\Omega$		23	34	ns
$t_{pd0}$ From $C_0$ to 1	$C_L = 50\text{pF}, R_L = 400\Omega$		20	34	ns
$t_{pd1}$ From $C_0$ to 2	$C_L = 50\text{pF}, R_L = 400\Omega$		24	35	ns
$t_{pd0}$ From $C_0$ to 2	$C_L = 50\text{pF}, R_L = 400\Omega$		22	35	ns
$t_{pd1}$ From $C_0$ to 3	$C_L = 50\text{pF}, R_L = 400\Omega$		30	50	ns
$t_{pd0}$ From $C_0$ to 3	$C_L = 50\text{pF}, R_L = 400\Omega$		24	40	ns
$t_{pd1}$ From $C_0$ to 4	$C_L = 50\text{pF}, R_L = 400\Omega$		30	50	ns
$t_{pd0}$ From $C_0$ to 4	$C_L = 50\text{pF}, R_L = 400\Omega$		28	50	ns
$t_{pd1}$ From $C_0$ to $C_4$	$C_L = 50\text{pF}, R_L = 780\Omega$		12	20	ns
$t_{pd0}$ From $C_0$ to $C_4$	$C_L = 50\text{pF}, R_L = 780\Omega$		12	20	ns
$t_{pd1}$ From $A_2$ or $B_2$ to 2	$C_L = 50\text{pF}, R_L = 400\Omega$			40	ns
$t_{pd0}$ From $A_2$ or $B_2$ to 2	$C_L = 50\text{pF}, R_L = 400\Omega$			35	ns
$t_{pd1}$ From $A_4$ or $B_4$ to 4	$C_L = 50\text{pF}, R_L = 400\Omega$			40	ns
$t_{pd0}$ From $A_4$ or $B_4$ to 4	$C_L = 50\text{pF}, R_L = 400\Omega$			35	ns

†  $t_{pd1}$  is propagation delay time to logical 1 level;  $t_{pd0}$  is propagation delay time to logical 0 level.

\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

\*\* All trigger values are at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ .

† Not more than one output should be shorted at a time.

NOTE 1: These voltage values are with respect to network ground terminal.

7486

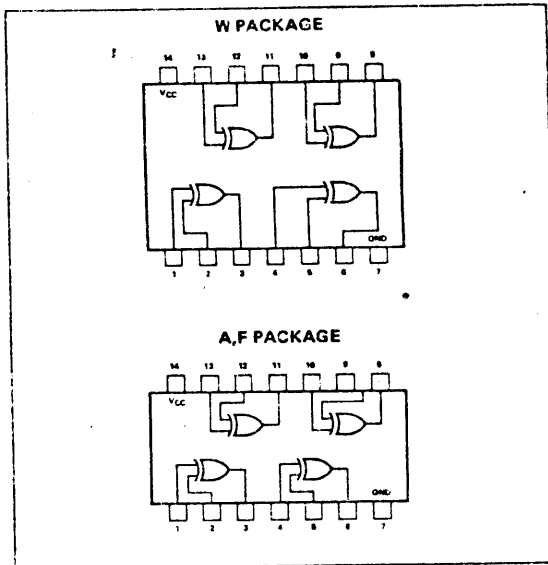
DESCRIPTION

The 54/7486 Quad 2-Input Exclusive OR Gate is a TTL element providing the function  $\overline{A}B + A\overline{B}$  at the output.

TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

PIN CONFIGURATIONS



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage $V_{CC}$	5426 Circuits 7486 Circuits	4.5 4.75	5 5	5.5 5.25	V
Normalized Fan-Out from each output, N:	Logical 0 Logical 1			10 20	

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal $V_{CC} = \text{MIN}$	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal $V_{CC} = \text{MIN}$			0.8	V
$V_{out(1)}$	Logical 1 output voltage $V_{CC} = \text{MIN}, V_{in(1)} = 2V,$ $V_{in(0)} = 0.8V, I_{load} = -800 \mu A$	2.4			V
$V_{out(0)}$	Logical 0 output voltage $V_{CC} = \text{MIN}, V_{in(1)} = 2V,$ $V_{in(0)} = 0.8V, I_{sink} = 16mA$			0.4	V
$I_{in(1)}$	Logical 1 level input current (each input) $V_{CC} = \text{MAX}, V_{in} = 2.4V$			40	$\mu A$
$I_{in(0)}$	Logical 0 level input current (each input) $V_{CC} = \text{MAX}, V_{in} = 5.5V$			1	mA
$I_{in(0)}$	Logical 0 level input current (each input) $V_{CC} = \text{MAX}, V_{in} = 0.4V$			-1.6	mA
$I_{OS}$	Short circuit output current† $V_{CC} = \text{MAX}, V_{in(1)} = 4.5V,$ $V_{in(0)} = 0$	-20		-55	mA
$I_{OS}$	Short circuit output current† $V_{CC} = \text{MAX}, V_{in(1)} = 4.5V,$ $V_{in(0)} = 0$	-18		-55	mA
$I_{CC}$	Supply current $V_{CC} = \text{MAX}, V_{in} = 4.5V$		30	43	mA
$I_{CC}$	Supply current $V_{CC} = \text{MAX}, V_{in} = 4.5V$		30	50	mA

SWITCHING CHARACTERISTICS,  $V_{CC} = 5V, T_A = 25^\circ C, N = 10$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd0}$	Propagation delay time to logical 0 level (other input low) $C_L = 15pF, R_L = 400$		11	17	ns
$t_{pd1}$	Propagation delay time to logical 1 level (other input low) $C_L = 15pF, R_L = 400$		15	23	ns
$t_{pd0}$	Propagation delay time to logical 0 level (other input high) $C_L = 15pF, R_L = 400$		13	22	ns
$t_{pd1}$	Propagation delay time to logical 1 level (other input high) $C_L = 15pF, R_L = 400$		18	30	ns

\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

\*\* All typical values are at  $V_{CC} = 5V, T_A = 25^\circ C$ .

† Not more than one output should be shorted at a time.

7490

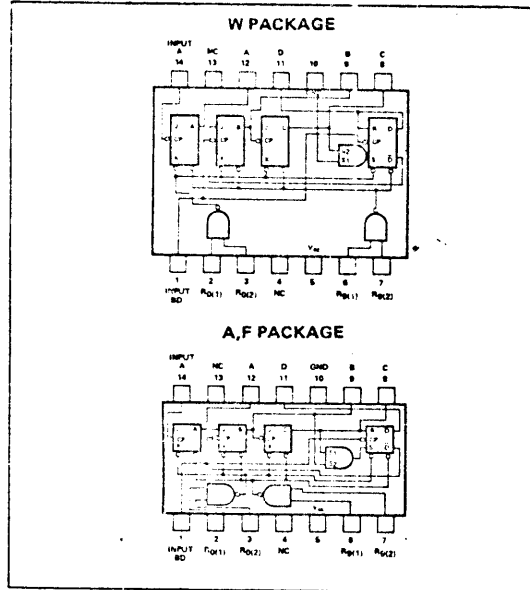
**DESCRIPTION**

The 5490/7490 is a high-speed, monolithic decade counter consisting of four dual-rank, master-slave flip-flops internally interconnected to provide a divide-by-two counter and a divide-by-five counter. Gated direct reset lines are provided to inhibit count inputs and return all outputs to a logical "0" or to a binary coded decimal (BCD) count of 9. As the output from flip-flop A is not internally connected to the succeeding stages, the count may be separated in three independent count modes:

1. When used as a binary coded decimal decade counter, the BD input must be externally connected to the A output. The A input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table shown above. In addition to a conventional "0" reset, inputs are provided to reset a BCD 9 count for nine's complement decimal applications.
2. If a symmetrical divide-by-ten count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of ten, the D output must be externally connected to the A input. The input count is then applied at the BD input and a divide-by-ten square wave is obtained at output A.
3. For operation as a divide-by-two counter and divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The BD input is used to obtain binary divide-by-five operation at the B, C, and D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

The 5490/7490 is completely compatible with Series 54 and Series 74 logic families. Average power dissipation is 160mW.

**PIN CONFIGURATIONS**

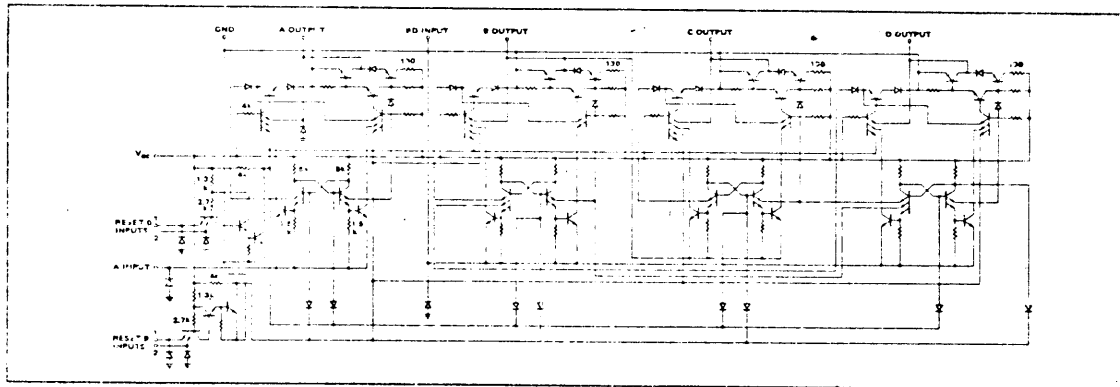


**LOGIC TRUTH TABLES**

BCD COUNT SEQUENCE (See Note 1)					RESET/COUNT (See Note 2)							
COUNT	OUTPUT				RESET INPUTS				OUTPUT			
	D	C	B	A	R <sub>0</sub> (1)	R <sub>0</sub> (2)	R <sub>9</sub> (1)	R <sub>9</sub> (2)	D	C	B	A
0	0	0	0	0	1	1	0	X	0	0	0	0
1	0	0	0	1	1	1	X	0	0	0	0	0
2	0	0	1	0	X	X	1	1	1	0	0	1
3	0	0	1	1	X	0	X	0	COUNT			
4	0	1	0	0	0	X	0	X	COUNT			
5	0	1	0	1	0	X	0	X	COUNT			
6	0	1	1	0	0	X	X	0	COUNT			
7	0	1	1	1	0	X	X	0	COUNT			
8	1	0	0	0	X	0	0	X	COUNT			
9	1	0	0	1								

- NOTES:**
1. Output A connected to input BD for BCD count.
  2. X indicates that either a logical 1 or a logical 0 may be present.
  3. Fanout from output A to input BD and to 10 additional Series 54/74 loads is permitted.

**SCHEMATIC DIAGRAM**



**RECOMMENDED OPERATING CONDITIONS**

	MIN	NOM	MAX	UNIT
Supply Voltage V <sub>CC</sub> : 5490 Circuits	4.5	5	5.5	V
7490 Circuits	4.75	5	5.25	V
Normal, rated Fan-Out from each Output, N			10	
Width of Input Count Pulse, t <sub>pin</sub>	50			ns
Width of Reset Pulse, t <sub>reset</sub>	50			ns
Operating Free-Air Temperature Range, T <sub>A</sub> : 5490 Circuits	-55	25	125	°C
7490 Circuits	0	25	70	°C

7490 CONT'D

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	$V_{CC} = \text{MIN}$		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	$V_{CC} = \text{MIN}$				0.8	V
$V_{out(1)}$	Logical 1 output voltage	$V_{CC} = \text{MIN}$ ,	$I_{load} = -400\mu\text{A}$	2.4			V
$V_{out(0)}$	Logical 0 output voltage	$V_{CC} = \text{MIN}$ ,	$I_{sink} = 16\text{mA}$			0.4	V
$I_{in(1)}$	Logical 1 level input current at $R_0(1)$ , $R_0(2)$ , $R_9(1)$ , or $R_9(2)$	$V_{CC} = \text{MAX}$ , $V_{CC} = \text{MAX}$ ,	$V_{in} = 2.4\text{V}$ $V_{in} = 5.5\text{V}$			40 1	$\mu\text{A}$ mA
$I_{in(1)}$	Logical 1 level input current at input A	$V_{CC} = \text{MAX}$ , $V_{CC} = \text{MAX}$ ,	$V_{in} = 2.4\text{V}$ $V_{in} = 5.5\text{V}$			80 1	$\mu\text{A}$ mA
$I_{in(i)}$	Logical 1 level input current at input BD	$V_{CC} = \text{MAX}$ , $V_{CC} = \text{MAX}$ ,	$V_{in} = 2.4\text{V}$ $V_{in} = 5.5\text{V}$			190 1	$\mu\text{A}$ mA
$I_{in(0)}$	Logical 0 level input current at $R_0(1)$ , $R_0(2)$ , $R_9(1)$ , or $R_9(2)$	$V_{CC} = \text{MAX}$ ,	$V_{in} = 0.4\text{V}$			-1.6	mA
$I_{in(0)}$	Logical 0 level input current at input A	$V_{CC} = \text{MAX}$ ,	$V_{in} = 0.4\text{V}$			-3.2	mA
$I_{in(0)}$	Logical 0 level input current at input BD	$V_{CC} = \text{MAX}$ ,	$V_{in} = 0.4\text{V}$			-6.4	mA
$I_{OS}$	Short circuit output current †	$V_{CC} = \text{MAX}$ ,	$V_{out} = 0\text{V}$	S5490 N7490 -20 -18		-57 -57	mA mA
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}$ ,	$V_{in} = 4.5\text{V}$		S5490 N7490 32 32	46 53	mA mA

SWITCHING CHARACTERISTICS,  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ ,  $N = 10$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{max}$	Maximum frequency of input count pulses	$C_L = 15\text{pF}$ ,	$R_L = 400\Omega$	10	18		MHz
$t_{pd1}$	Propagation delay time to logical 1 level from input count pulse to output C	$C_L = 15\text{pF}$ ,	$R_L = 400\Omega$		60	100	ns
$t_{pd0}$	Propagation delay time to logical 0 level from input count pulse to output C	$C_L = 15\text{pF}$ ,	$R_L = 400\Omega$		60	100	ns

- \* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.
- \*\* All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ .
- † Not more than one output should be shorted at a time.

7493

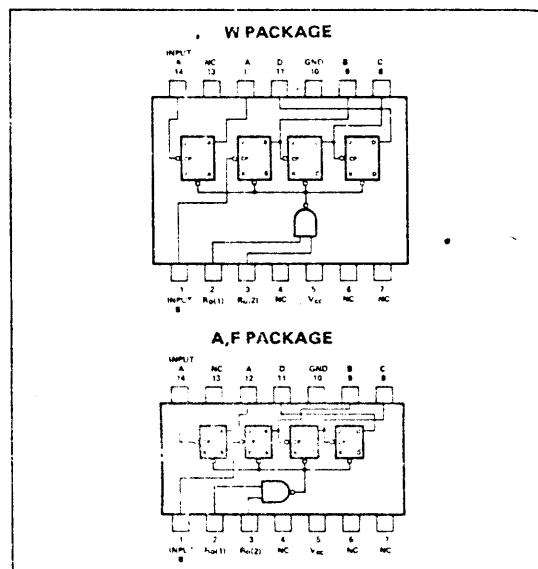
DESCRIPTION

The S5493/N7493 is a high-speed, monolithic 4-bit binary counter consisting of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

1. When used as a 4-bit ripple-through counter output A must be externally connected to input B. The input count pulses are applied to input A. Simultaneous divisions of 2, 4, 8, and 16 are performed at the A, B, C, and D outputs as shown in the truth table.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to input B. Simultaneous frequency divisions of 2, 4, and 8 are available at the B, C, and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the 3-bit ripple-through counter.

The S5493/N7493 is completely compatible with Series 54 and Series 74 logic families. Average power dissipation is 32mW per flip-flop (128mW total).

PIN CONFIGURATIONS



D COMPONENT DESCRIPTION  
D.6 INTEGRATED CIRCUITS

7493 cont'd

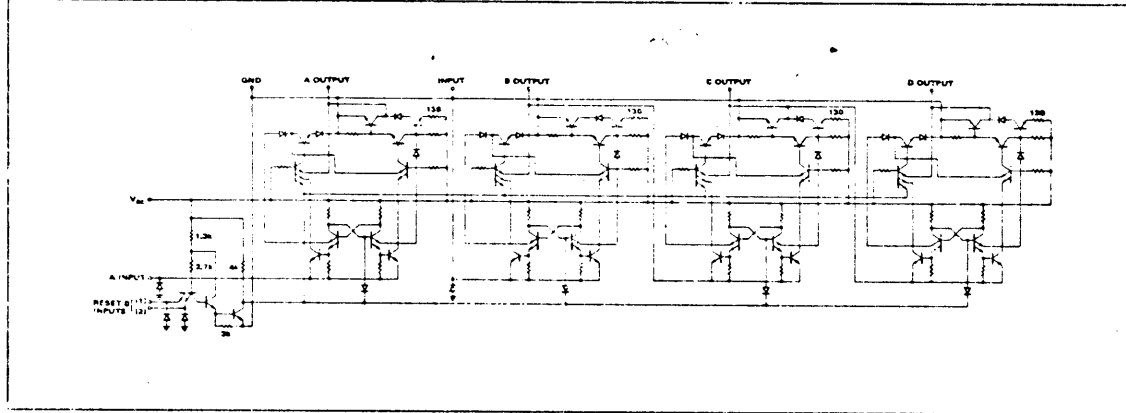
TRUTH TABLE (See Notes 1 and 2)

LOGIC				
COUNT	OUTPUT			
	D	C	E	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0

COUNT	OUTPUT			
	D	C	E	A
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

NOTES:  
1. Output A connected to input B.  
2. To reset all outputs to logical 0, both R<sub>0</sub>(1) and R<sub>0</sub>(2) inputs must be at logical 1.

SCHEMATIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V <sub>CC</sub> : S5493 Circuits	4.5	5	5.5	V
N7493 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T <sub>A</sub> : S5493 Circuits	-65	25	125	°C
N7493 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N			10	
Width of Input Count Pulse, t <sub>p(in)</sub>	50			ns
Width of Reset Pulse, t <sub>p(reset)</sub>	50			ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
V <sub>in(1)</sub>	V <sub>CC</sub> = MIN	2			V
V <sub>in(0)</sub>	V <sub>CC</sub> = MIN			0.8	V
V <sub>out(1)</sub>	V <sub>CC</sub> = MIN, I <sub>load</sub> = -400μA	2.4			V
V <sub>out(0)</sub>	V <sub>CC</sub> = MIN, I <sub>sink</sub> = 16mA			0.4	V
I <sub>in(1)</sub>	V <sub>CC</sub> = MAX, V <sub>in</sub> = 2.4V			40	μA
	V <sub>CC</sub> = MAX, V <sub>in</sub> = 5.5V			1	mA
I <sub>in(1)</sub>	V <sub>CC</sub> = MAX, V <sub>in</sub> = 2.4V			30	μA
	V <sub>CC</sub> = MAX, V <sub>in</sub> = 5.5V			1	mA
I <sub>in(0)</sub>	V <sub>CC</sub> = MAX, V <sub>in</sub> = 0.4V			-1.6	mA
I <sub>in(0)</sub>	V <sub>CC</sub> = MAX, V <sub>in</sub> = 0.4V			-3.2	mA
I <sub>OS</sub>	V <sub>CC</sub> = MAX, V <sub>out</sub> = 0	S5493 N7493	-20 -18	-57 -57	mA
I <sub>CC</sub>	V <sub>CC</sub> = MAX, V <sub>in</sub> = 4.5V	S5493 N7493	32 32	46 53	mA

7493 cont'd

SWITCHING CHARACTERISTICS,  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $N = 10$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{max}$	Maximum frequency of input count pulses	$C_L = 15pF$ ,	$R_L = 400\Omega$	10	18		MHz
$t_{pd1}$	Propagation delay time to logical 1 level from input count pulse to output D	$C_L = 15pF$ ,	$R_L = 400\Omega$		75	135	ns
$t_{pd0}$	Propagation delay time to logical 0 level from input count pulse to output D	$C_L = 15pF$ ,	$R_L = 400\Omega$		75	135	ns

\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

\*\* All typical values are at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ .

† Not more than one output should be shorted at a time.

7495

DESCRIPTION

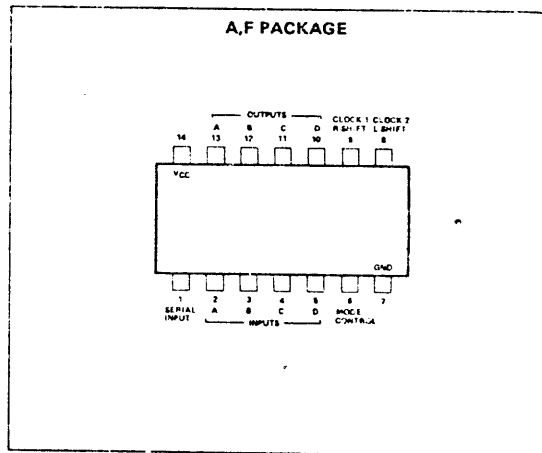
The 54/7495 is a monolithic universal 4-Bit Shift Register designed with standard TTL techniques. The circuit layout consists of 4 R-S master-slave flip-flops, 4 AND-OR-INVERT gates, and 6 inverters configured to form a versatile register which will perform right-shift, left-shift, or parallel-in, parallel-out operations depending on the logical input level to the mode control.

Right-shift operations are performed when a logical 0 level is applied to the mode control. Serial data is entered at the serial input  $D_0$  and shifted one position right on each clock 1 pulse. In this mode, clock 2 and parallel inputs  $D_A$  thru  $D_D$  are inhibited.

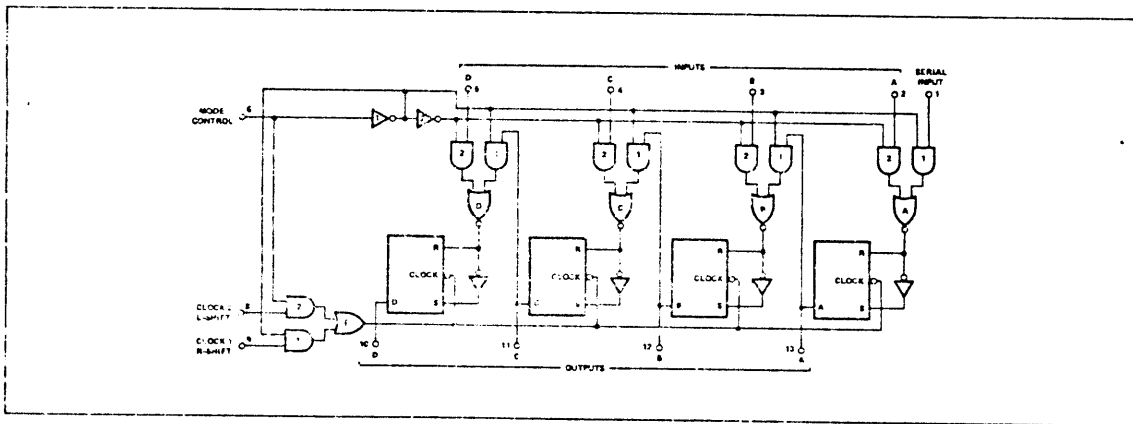
Parallel-in, parallel-out operations are performed when a logical 1 level is applied to the mode control. Parallel data is entered at parallel inputs  $D_A$  thru  $D_D$  and is transferred to the data outputs  $A_0$  thru  $D_0$  on each clock 2 pulse. In this mode, shift-left operations may be implemented by externally tying the output of each flip-flop to the parallel input of the previous flip-flop ( $D_0$  to  $D_C$  and etc.), with serial data entry at input  $D_D$ .

Information must be present at the R-S inputs prior to clocking and transfer of data occurs on the falling edge of the clock pulse

PIN CONFIGURATIONS



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage $V_{CC}$	5495 Circuits N7495 Circuits	4.5 4.75	5 5	5.5 5.25	V V
Normalized Fan-Out From Each Output				10	
Width of Clock Pulse $t_{p(clock)}$	5495 Circuits N7495 Circuits	20 15	10 10		ns ns
Setup Time Required at Serial, A, B, C, or D Inputs $t_{setup}$		10	10		ns
Hold Time Required at Serial, A, B, C, or D Inputs $t_{hold}$		0	10		ns
Logical 0 Level Setup Time Required at Mode Control (With Respect to Clock 1 inputs)		15			ns
Logical 1 Level Setup Time Required at Mode Control (With Respect to Clock 2 input)		15			ns
Logical 0 Level Setup Time Required at Mode Control (With Respect to Clock 2 input)		5			ns
Logical 1 Level Setup Time Required at Mode Control (With Respect to Clock 1 input)		5			ns

D COMPONENT DESCRIPTION  
D.6 INTEGRATED CIRCUITS

7495 cont'd

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT	
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	$V_{CC} = \text{MIN}$	2		V	
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	$V_{CC} = \text{MIN}$		0.8	V	
$V_{out(1)}$	Logical 1 output voltage	$V_{CC} = \text{MIN}$ , $I_{load} = -800\mu\text{A}$	2.4		V	
$V_{out(0)}$	Logical 0 output voltage	$V_{CC} = \text{MIN}$ , $I_{sink} = 16\text{mA}$		0.4	V	
$I_{in(0)}$	Logical 0 level input current at any input except mode control	$V_{CC} = \text{MAX}$ , $V_{in} = 0.4\text{V}$		-1.6	mA	
$I_{in(0)}$	Logical 0 level input current at mode control	$V_{CC} = \text{MAX}$ , $V_{in} = 0.4\text{V}$		-3.2	mA	
$I_{in(1)}$	Logical 1 level input current at any input except mode control	$V_{CC} = \text{MAX}$ , $V_{in} = 2.4\text{V}$ $V_{CC} = \text{MAX}$ , $V_{in} = 5.5\text{V}$		40 1	$\mu\text{A}$ mA	
$I_{in(1)}$	Logical 1 level input current at mode control	$V_{CC} = \text{MAX}$ , $V_{in} = 2.4\text{V}$ $V_{CC} = \text{MAX}$ , $V_{in} = 5.5\text{V}$		80 1	$\mu\text{A}$ mA	
$I_{OS}$	Short-circuit output current†	$V_{CC} = \text{MAX}$	-18	-57	mA	
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}$	39	50	63	mA

N7495

SWITCHING CHARACTERISTICS,  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ ,  $N = 10$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{max}$	Maximum shift frequency	$C_L = 15\text{pF}$ , $R_L = 400\Omega$	25	36	MHz
$t_{pd1}$	Propagation delay time to logical 1 level from clock 1 or clock 2 to outputs	$C_L = 15\text{pF}$ , $R_L = 400\Omega$	18	27	ns
$t_{pd0}$	Propagation delay time to logical 0 level from clock 1 or clock 2 to outputs	$C_L = 15\text{pF}$ , $R_L = 400\Omega$	21	32	ns

\*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

\*\*All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ .

†Not more than one output should be shorted at a time.

74123

DESCRIPTION

These monostables are designed to provide the system designer with complete flexibility in controlling the pulse width, either to lengthen the pulse by retriggering, or to shorten by clearing. N74122 has an internal timing resistor which allows the circuit to be operated with only an external capacitor, if so desired. Applications requiring more precise pulse widths and not requiring the clear feature can best be satisfied with N74121.

The output pulse is primarily a function of the external capacitor and resistor. For  $C_{ext} > 1000\text{pF}$ , the output pulse width ( $t_w$ ) is defined as:

$$t_w = 0.32 R_T C_{ext} \left( 1 + \frac{0.7}{R_T} \right)$$

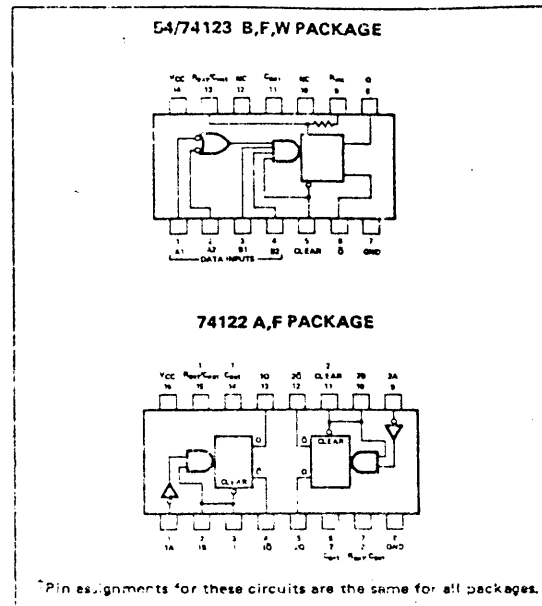
where

$R_T$  is in  $k\Omega$  (either internal or external timing resistor)  
 $C_{ext}$  is in pF  
 $t_w$  is in ns

For pulse widths when  $C_{ext} \leq 1000\text{pF}$ , see Figure B.

These circuits are fully compatible with most TTL or DTL families. Inputs are diode-clamped to minimize reflections due to transmission-line effects, which simplifies design. Typical power dissipation per chip is 115 mW (max); typical average propagation delay time to the Q output is 21 nanoseconds. The N74122 and N74123 are characterized for operation from  $0^\circ\text{C}$  to  $70^\circ\text{C}$ .

PIN CONFIGURATIONS



\*Pin assignments for these circuits are the same for all packages.



74123 cont'd

TRUTH TABLE (See Note A)

N74122						S54123, N74123			
INPUTS				OUTPUTS		INPUTS		OUTPUTS	
A <sub>1</sub>	A <sub>2</sub>	B <sub>1</sub>	B <sub>2</sub>	Q	Q	A	B	Q	Q
H	H	X	X	L	H	H	X	L	H
X	X	L	X	L	H	X	L	L	H
X	X	X	L	L	H	L	↑	⌋	⌋
L	X	H	H	L	H	L	↑	⌋	⌋
L	X	↑	H	⌋	⌋	X	L	L	H
L	X	H	↑	⌋	⌋	L	↑	⌋	⌋
X	L	H	H	L	H	↓	H	⌋	⌋
X	L	↑	H	⌋	⌋				
X	L	H	↑	⌋	⌋				
H	↓	H	H	⌋	⌋				
↓	↓	H	H	⌋	⌋				
	H	H	H	⌋	⌋				

**NOTES:**

A. H = high level (steady-state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⌋ = one high-level pulse, ⌋ = one low-level pulse, X = irrelevant (any input, including transitions).

B. NC = No internal connection.

C. To use the internal timing resistor of N74122 (10kΩ nominal), connect R<sub>int</sub> to V<sub>CC</sub>.

D. An external timing capacitor may be connected between C<sub>ext</sub> and R<sub>ext</sub>/C<sub>ext</sub> (positive).

**RECOMMENDED OPERATING CONDITIONS**

	S54123, N74122, N74123			UNIT
	MIN	NOM	MAX	
Supply Voltage V <sub>CC</sub>	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			20	
			10	
Input data setup time, t <sub>setup</sub> (See Note 3)	40†			ns
Input data hold time, t <sub>hold</sub> (See Note 4)	40†			ns
Width of Clear Pulse, t <sub>w(clear)</sub>	40†			ns
External Timing Resistance	5		50	kΩ
External Capacitance	No Restriction			
Wiring Capacitance at R <sub>ext</sub> /C <sub>ext</sub> Terminal			50	pF
Operating Free-Air Temperature, T <sub>A</sub>	0	25	70	°C

† These conditions are recommended for use at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

**NOTES:**

1. Voltage values, except intermitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For the N74122 circuit, this rating applies to each A input with respect to the other and to each B input with respect to the other.
3. Setup time for a dynamic input is the interval immediately preceding the transition which constitutes the dynamic input, during which interval a steady-state logic level must be maintained at the input to ensure recognition of the transition.
4. Hold time for a dynamic input is the interval immediately following the transition which constitutes the dynamic input, during which interval a steady-state logic level must be maintained at the input to ensure continued recognition of the transition.
5. Ground C<sub>ext</sub> to measure V<sub>OH</sub> at Q, V<sub>OL</sub> at Q̄, or I<sub>OS</sub> at Q. C<sub>ext</sub> is open to measure V<sub>OH</sub> at Q, V<sub>OL</sub> at Q, or I<sub>CS</sub> at Q̄.
6. Quiescent I<sub>CC</sub> is measured (after clearing) with 2.4V applied to all clear and A inputs, B inputs grounded, all outputs open. C<sub>ext</sub> = 0.02μF, and R<sub>ext</sub> = 25kΩ. R<sub>int</sub> of S54122/N74122 is open.
7. I<sub>CC</sub> is measured in the triggered state with 2.4V applied to all clear and B inputs, A inputs grounded, all outputs open. C<sub>ext</sub> = 0.02μF, and R<sub>ext</sub> = 25kΩ. R<sub>int</sub> of S54122/N74122 is open.

**ELECTRICAL CHARACTERISTICS (over operating free-air temperature range unless otherwise noted)**

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
V <sub>IH</sub>	High-level input voltage	2			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
V <sub>I</sub>	Input clamp voltage			-1.5	V
V <sub>OH</sub>	High-level output voltage	2.4			V
V <sub>OL</sub>	Low-level output voltage		0.22	0.4	V
I <sub>I</sub>	Input current at maximum input voltage			1	mA
I <sub>IH</sub>	High-level input current			40	μA
	data inputs			80	
	clear input			-1.6	
I <sub>IL</sub>	Low-level input current			-3.2	mA
	data inputs			-40	
	clear input†			28	
I <sub>OS</sub>	Short-circuit output current†	-10		28	mA
I <sub>CC</sub>	Supply current (quiescent or triggered)		23	66	mA
			46		

D COMPONENT DESCRIPTION  
 D.6 INTEGRATED CIRCUITS

74123 cont'd

SWITCHING CHARACTERISTICS,  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $N = 10$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time, low-to-high-level Q output, from either A input		22	33	ns
$t_{PLH}$	Propagation delay time, low-to-high-level Q output, from either B input		19	28	ns
$t_{PHL}$	Propagation delay time, high-to-low-level $\bar{Q}$ output, from either A input	$C_{ext} = 0$ , $C_L = 15pF$	30	40	ns
$t_{PHL}$	Propagation delay time, high-to-low-level $\bar{Q}$ output, from either B input	$R_{ext} = 5k\Omega$ , $R_L = 400\Omega$	27	36	ns
$t_{PHL}$	Propagation delay time, high-to-low-level Q output, from clear input		18	27	ns
$t_{PLH}$	Propagation delay time, low-to-high-level $\bar{Q}$ output, from clear input		30	40	ns
$t_w(\min)$	Minimum width of Q output pulse		45	65	ns
$t_w$	Width of Q output pulse	$C_{ext} = 1000pF$ , $C_L = 15pF$	3.08	3.42	$\mu s$
		$R_{ext} = 10k\Omega$ , $R_L = 400\Omega$		3.76	

74150

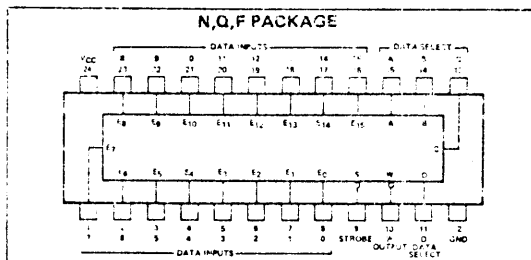
DESCRIPTION

The 54/74150 is a one-of-sixteen data selector which performs parallel-to-serial data conversion. The unit incorporates an enable circuit for chip select. This allows multiplexing from N-lines to one-line.

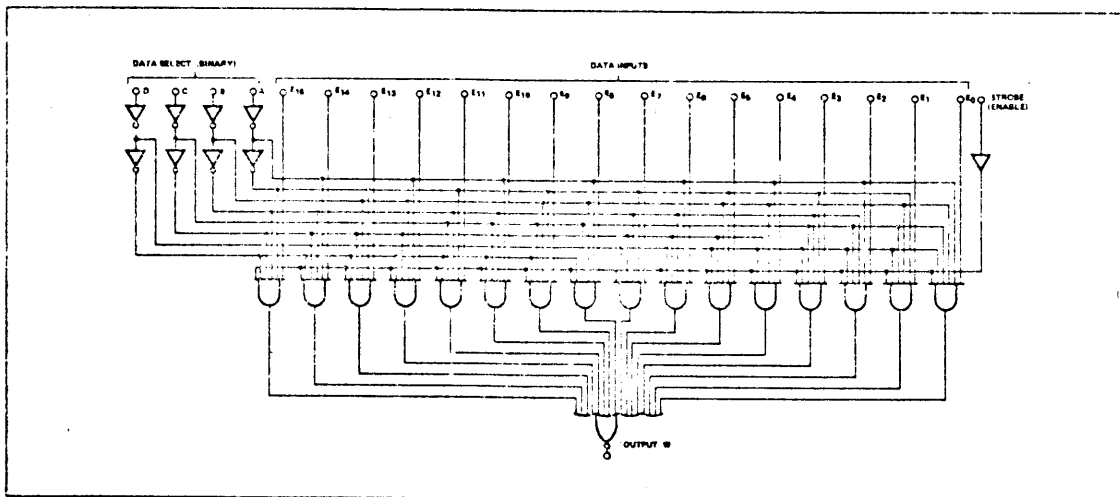
The 54150/N74150 is provided with a strobe-input which, when taken to a logical 0, enables the function of these multiplexers.

This data selector/multiplexer is fully compatible for use with other TTL or DTL circuit. Each input represents only one normalized Series 54/74 load, and full fan-out to 10 normalized Series 54/74 loads is available from each of the outputs in the logical 0 state. A fan-out to 20 normalized Series 54/74 loads is provided in the logical 1 state to facilitate connection of unused inputs to used inputs. Typical power dissipations are:  
 54150/N74150 - 200 milliwatts.

PIN CONFIGURATIONS



LOGIC DIAGRAM



74150 cont'd

TRUTH TABLE

INPUTS																OUTPUT						
D	C	B	A	STROBE	E <sub>0</sub>	E <sub>1</sub>	E <sub>2</sub>	E <sub>3</sub>	E <sub>4</sub>	E <sub>5</sub>	E <sub>6</sub>	E <sub>7</sub>	E <sub>8</sub>	E <sub>9</sub>	E <sub>10</sub>	E <sub>11</sub>	E <sub>12</sub>	E <sub>13</sub>	E <sub>14</sub>	E <sub>15</sub>	W	
0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	1	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	1	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
1	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
1	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
1	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
1	0	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
1	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
1	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
1	1	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
1	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
1	1	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
1	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
1	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V <sub>CC</sub> : S54150 Circuits	4.5	5	5.5	V
N74150 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: Logical 0			10	
Logical 1			20	

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS *	MIN	TYP **	MAX	UNIT
V <sub>in(1)</sub> Input voltage required to ensure logical 1 at any input terminal	V <sub>CC</sub> = MIN	2			V
V <sub>in(0)</sub> Input voltage required to ensure logical 0 at any input terminal	V <sub>CC</sub> = MIN			0.8	V
V <sub>out(1)</sub> Logical 1 output voltage	V <sub>CC</sub> = MIN, V <sub>in(1)</sub> = 2V, V <sub>in(0)</sub> = 0.8V, I <sub>load</sub> = -800 μA	2.4			V
V <sub>out(0)</sub> Logical 0 output voltage	V <sub>CC</sub> = MIN, V <sub>in(1)</sub> = 2V, V <sub>in(0)</sub> = 0.8V, I <sub>sink</sub> = 16mA			0.4	V
I <sub>in(1)</sub> Logical 1 level input current (each input)	V <sub>CC</sub> = MAX, V <sub>in</sub> = 2.4V			40	μA
	V <sub>CC</sub> = MAX, V <sub>in</sub> = 5.5V			1	mA
I <sub>in(0)</sub> Logical 0 level input current (each input)	V <sub>CC</sub> = MAX, V <sub>in</sub> = 0.4V			-1.6	mA
I <sub>OS</sub> Short circuit output current†	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 0	-20		-55	mA
I <sub>CC</sub> Supply current	V <sub>CC</sub> = MAX, V <sub>in</sub> = 4.5V		40	68	mA

SWITCHING CHARACTERISTICS, V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C, N = 10

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>pd0</sub>	A, B, or C (4 levels)	Y	C <sub>L</sub> = 15pF, R <sub>L</sub> = 400Ω		20	30	ns
t <sub>pd1</sub>	A, B, or C (4 levels)	Y			35	52	ns
t <sub>pd0</sub>	A, B, C, or D (3 levels)	W			22	33	ns
t <sub>pd1</sub>	A, B, C, or D (3 levels)	W			23	35	ns
t <sub>pd0</sub>	STROBE	Y			19	30	ns
t <sub>pd1</sub>	STROBE	Y			35	52	ns
t <sub>pd0</sub>	STROBE	W			21	30	ns
t <sub>pd1</sub>	STROBE	W			15.5	24	ns
t <sub>pd0</sub>	D <sub>0</sub> thru D <sub>7</sub>	Y			16	24	ns
t <sub>pd1</sub>	D <sub>0</sub> thru D <sub>7</sub>	Y			19	29	ns
t <sub>pd0</sub>	E <sub>0</sub> thru E <sub>15</sub>	W		8.5	14	ns	
t <sub>pd1</sub>	E <sub>0</sub> thru E <sub>15</sub>	W		13	20	ns	

\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

\*\* All typical values are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

† Not more than one output should be shorted at a time.

D COMPONENT DESCRIPTION  
 D.6 INTEGRATED CIRCUITS

74155, 74156

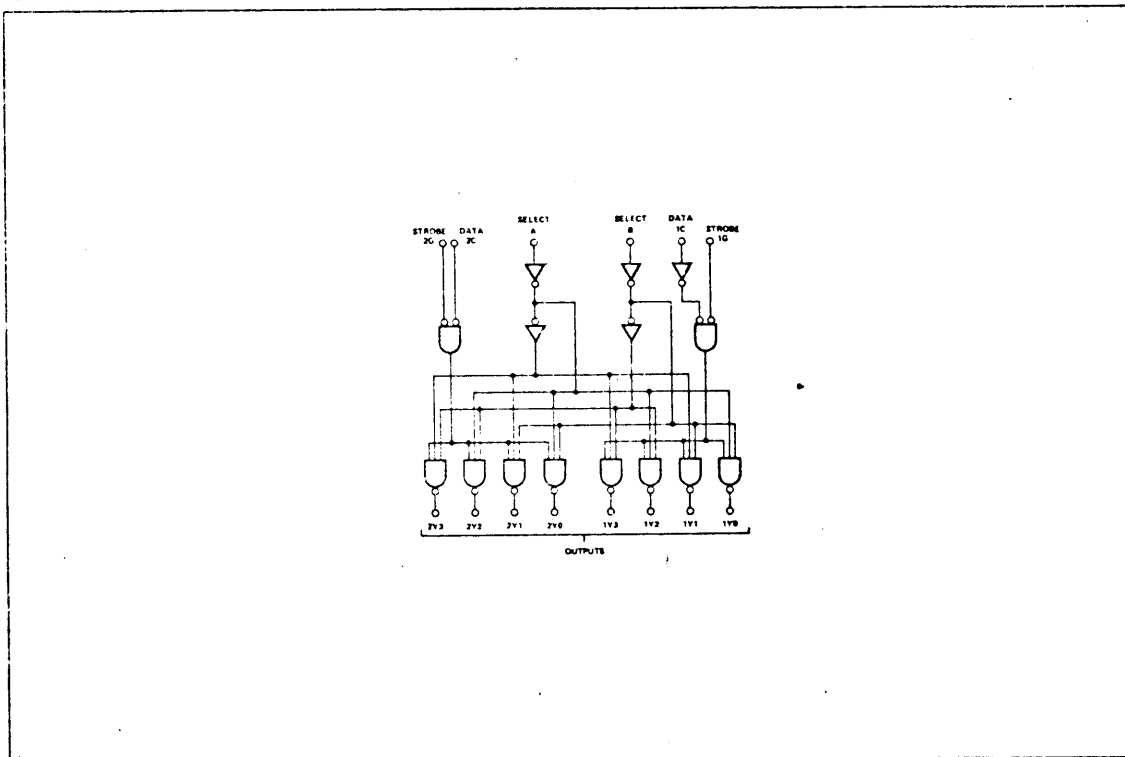
DESCRIPTION

These monolithic transistor-transistor-logic (TTL) circuits feature dual 1-line to 4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired.

Data applied to input 1C is inverted at its outputs and data applied at 2C is not inverted through its outputs. The inverter following the 1C data input permits use as a 2- to 8-line decoder or 1- to 8-line demultiplexer without external gating. See typical applications data and the truth tables for more details.

The S54155/N74155 circuits, with totem pole outputs, are rated to fan-out to 10 normalized Series 54/74 loads in the low-level output state, and to 20 loads in the high-level output state. The S54156/N74156 circuits, with open-collector outputs, are rated to sink 16 milliamperes at a low-level output voltage of less than 0.4 volt. Input-clamping diodes are provided on all of these circuits to minimize transmission-line effects and simplify system design.

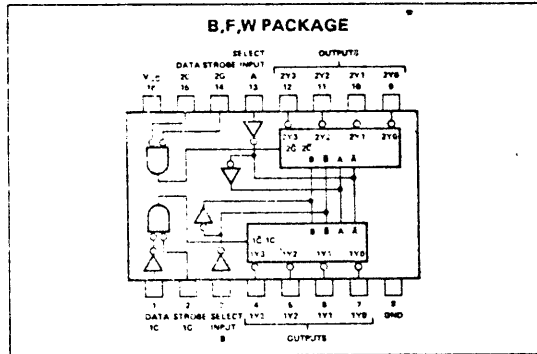
LOGIC DIAGRAM



Typical power dissipation is 125 milliwatts. Typical average propagation delay times are 16 nanoseconds through 2 levels of logic and 21 nanoseconds through 3 levels of logic for the S54155/N74155.

The S54155 and S54156 are characterized for operation over the full military temperature range of -55°C to 125°C the N74155 and N74156 are characterized for operation from 0°C to 70°C.

PIN CONFIGURATION



D COMPONENT DESCRIPTION  
D.6 INTEGRATED CIRCUITS

74155, 74156 cont'd

TRUTH TABLES

TRUTH TABLES (H = High Level, L = Low Level, X = Irrelevant)

**2-LINE TO 4-LINE DECODER OR 1-LINE TO 4-LINE DEMULTIPLEXER**

INPUTS				OUTPUTS				INPUTS				OUTPUTS			
SELECT		STROBE	DATA	1Y0	1Y1	1Y2	1Y3	SELECT		STROBE	DATA	2Y0	2Y1	2Y2	2Y3
B	A	1G	1C					B	A	2G	2C				
X	X	H	X	H	H	H	H	X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H	L	L	L	L	L	H	H	H
L	H	L	H	H	L	H	H	L	H	L	L	H	L	H	H
H	L	L	H	H	H	L	H	L	L	L	L	H	H	L	H
H	H	L	H	H	H	H	L	L	L	L	L	H	H	H	L
X	X	X	L	H	H	H	H	X	X	X	H	H	H	H	H

**3-LINE TO 8-LINE DECODER TO 1-LINE TO 8-LINE DEMULTIPLEXER**

INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

†C = inputs 1C and 2C connected together  
‡G = inputs 1G and 2G connected together

RECOMMENDED OPERATING CONDITIONS

	SS4155			N74155			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N:			20			20	
High logic level							
Low logic level			10			10	
Operating Free-Air Temperature Range, $T_A$	-55	25	125	0	25	70	°C

	SS4156			N74156			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
Low-level Output Current, $I_{OL}$			16			16	mA
Operating Free-Air Temperature Range, $T_A$	-55	25	125	0	25	70	°C

D COMPONENT DESCRIPTION  
D.6 INTEGRATED CIRCUITS

74155, 74156 cont'd

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	S54155, N74155			UNIT
		MIN	TYP**	MAX	
V <sub>IH</sub>	High-level input voltage	2			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, I <sub>OH</sub> = -800μA	V <sub>IH</sub> = 2V,	2.4	V
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, I <sub>OL</sub> = 16mA	V <sub>IL</sub> = 0.8V,		V
I <sub>IH</sub>	High-level input current (each input)	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 2.4V	40	μA
I <sub>IL</sub>	Low-level input current (each input)	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 5.5V	1	mA
I <sub>OS</sub>	Short-circuit output current †	V <sub>CC</sub> = MAX			mA
I <sub>CC</sub>	Supply current		S54155	-20	-55
			N74155	-18	-57
I <sub>CC</sub>	Supply current		S54155	25	35
			N74155	25	40

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	S54156, N74156			UNIT
		MIN	TYP**	MAX	
V <sub>IH</sub>	High-level input voltage	2			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = MIN, V <sub>OH</sub> = 5.5V	V <sub>I</sub> = 2V,	250	μA
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, I <sub>OL</sub> = 16mA	V <sub>IL</sub> = 0.8V,	0.4	V
I <sub>IH</sub>	High-level input current (each input)	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 2.4V	40	μA
I <sub>IL</sub>	Low-level input current (each input)	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 5.5V	1	mA
I <sub>IL</sub>	Low-level input current (each input)	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 0.4V	-1.6	mA
I <sub>CC</sub>	Supply current		S54156	25	35
			N74156	25	40

SWITCHING CHARACTERISTICS, V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C, N = 10

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	S54155 N74155			S54156 N74156			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>FLH</sub>	A, B, 2C, 1G, or 2G	Y	2			13	20		15	23	ns
t <sub>FHL</sub>	A, B, 2C, 1G, or 2G	Y	2	C <sub>L</sub> = 15pF,		18	27		20	30	ns
t <sub>PLH</sub>	A or B	Y	3	R <sub>L</sub> = 400Ω		21	32		23	34	ns
t <sub>PHL</sub>	A or B	Y	3			21	32		23	34	ns
t <sub>PLH</sub>	1C	Y	3			16	24		18	27	ns
t <sub>PHL</sub>	1C	Y	3			20	30		22	33	ns

\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

\*\* All typical values are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

† Not more than one output should be shorted at a time.

‡ t<sub>PLH</sub> = propagation delay time, low-to-high-level output

§ t<sub>PHL</sub> = propagation delay time, high-to-low-level output

74155, 74156 cont'd

TYPICAL APPLICATION DATA

The S54155, N74155, S54156, or N74156 may be used as a dual 2-line to 4-line decoder or a 1-line to 4-line demultiplexer. These applications are identical except as follows:

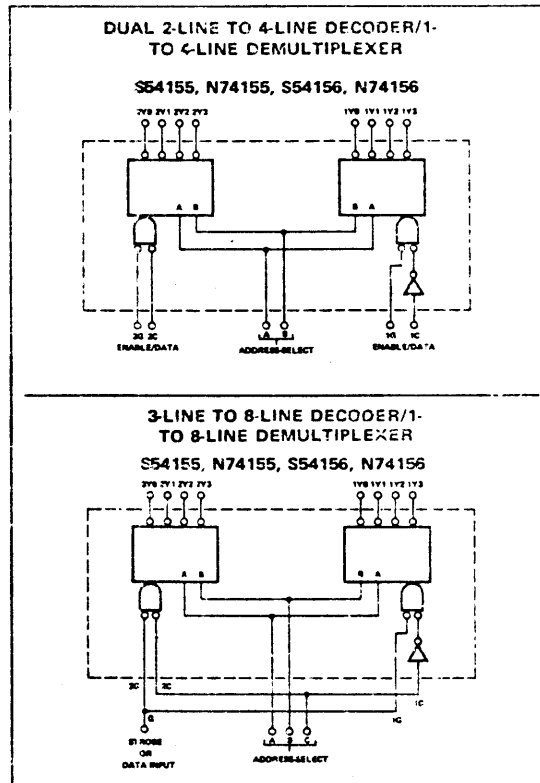
When decoding, the 2-line code is applied to select inputs A and B. The 4-line output section (1Y0, 1Y1, 1Y2, 1Y3) is enabled by taking strobe 1G low and input 1C high. The other 4-line output section (2Y0, 2Y1, 2Y2, 2Y3) is enabled by taking both strobe 2G and input 2C low. Note that the separate enable lines permit the user complete flexibility in decoding at either or both of the output sections. The strobe also permits cascading and allows disabling of the circuits until the addressing transients have passed.

When demultiplexing, the serial data is applied to the data inputs 1C and 2C and distribution to the outputs is controlled by the A and B select inputs. Again, the separate strobe inputs, 1G and 2G, permit demultiplexing to occur at either or both output sections, and cascading.

Any of these circuits may also be used as a 3-line to 8-line decoder or a 1-line to 8-line demultiplexer.

When used as a decoder, data inputs 1C and 2C are connected together and serve as the third (C) select line. The strobes are also connected together and are used for enabling and/or cascading.

When used as a demultiplexer, the common strobe line serves as the data input.

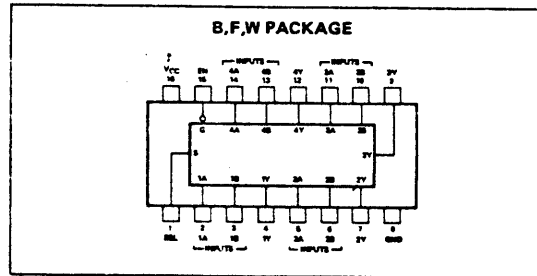


74157

DESCRIPTION

The S54157/N74157 and S54158/N74158 are identical with the exception of the S54158/N74158 being inverted. These devices are logical implementations of a four-pole two-position switch, with the position of the switch being set by the logic levels supplied to the one select input. Both assertion and negation outputs are provided. The enable input (E) is active low. When it is not activated the negation output is high and the assertion output is low regardless of all other inputs. The devices provide the ability, in one package, to select four bits of either data or control from two sources. By proper manipulation of the inputs, it can generate four functions of two variables with one variable common. Thus any number of random logic elements used to generate unusual truth tables can be replaced. All outputs are low when disabled (enable high). Both inputs and outputs are buffered.

PIN CONFIGURATION



S54/N74157

TRUTH TABLE

INPUTS			OUTPUT Y
STROBE	SELECT	A B	
H	X	X X	L
L	L	L X	L
L	L	H X	H
L	H	X L	L
L	H	X H	H

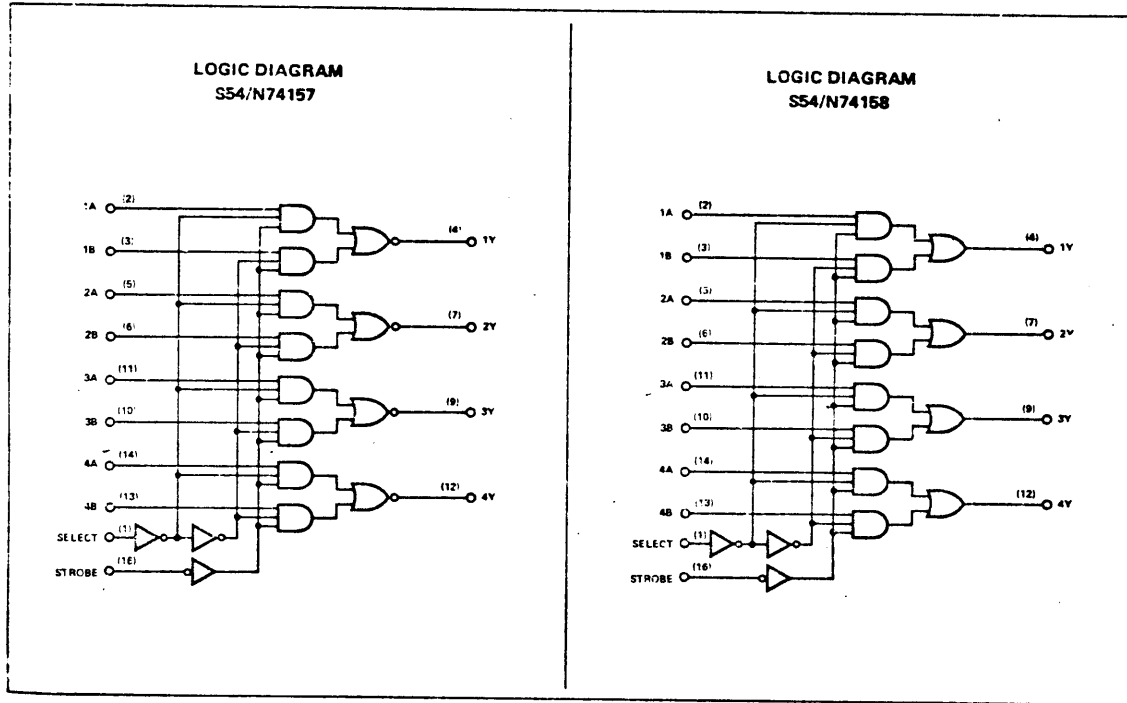
S54/N74158

TRUTH TABLE

INPUTS			OUTPUT Y
STROBE	SELECT	A B	
H	X	X X	H
L	L	L X	H
L	L	H X	L
L	H	X L	H
L	H	X H	L

D COMPONENT DESCRIPTION  
D.6 INTEGRATED CIRCUITS

74157 cont'd



RECOMMENDED OPERATING CONDITIONS

	S54157/58			N74157/58			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N							
High Logic Level			20			20	
Low Logic Level			10			10	
Operating Free-Air Temperature, $T_A$	-55	25	125	0	25	70	$^{\circ}C$

ELECTRICAL CHARACTERISTICS (over operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	S54157/58			N74157/58			UNIT
		MIN	TYP**	MAX	MIN	TYP**	MAX	
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$V_I$	Input clamp voltage			-1.5			-1.5	V
$V_{OH}$	High-level output voltage	2.4			2.4			V
$V_{OL}$	Low-level output voltage			0.4			0.4	V
$I_I$	Input current at maximum input voltage			1			1	mA
$I_{IH}$	High-level input current			40			40	$\mu A$
$I_{IL}$	Low-level input current			-1.6			-1.6	mA
$I_{OS}$	Short-circuit output current†			-20			-20	mA
$I_{CC}$	Supply current		30	43		30	43	mA

SWITCHING CHARACTERISTICS,  $V_{CC} = 5V$ ,  $T_A = 25^{\circ}C$ ,  $N = 10$

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PHL}$	Data	Output	$C_L = 15pF$ $R_L = 400$		9	14	ns
$t_{PLH}$	Data	Output			9	14	ns
$t_{PHL}$	Enable	Any Output			14	21	ns
$t_{PLH}$	Enable	Any Output			13	20	ns
$t_{PHL}$	Select	Any Output			18	27	ns
$t_{PLH}$	Select	Any Output			15	23	ns

\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

\*\* All typical values are at  $V_{CC} = 5V$ ,  $T_A = 25^{\circ}C$ .

† Not more than one output should be shorted at a time.



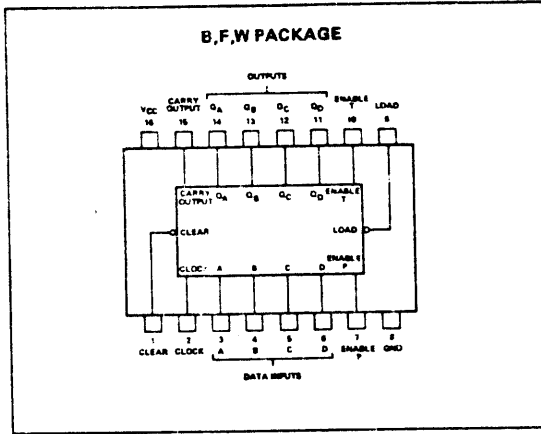
74163

**DESCRIPTION**

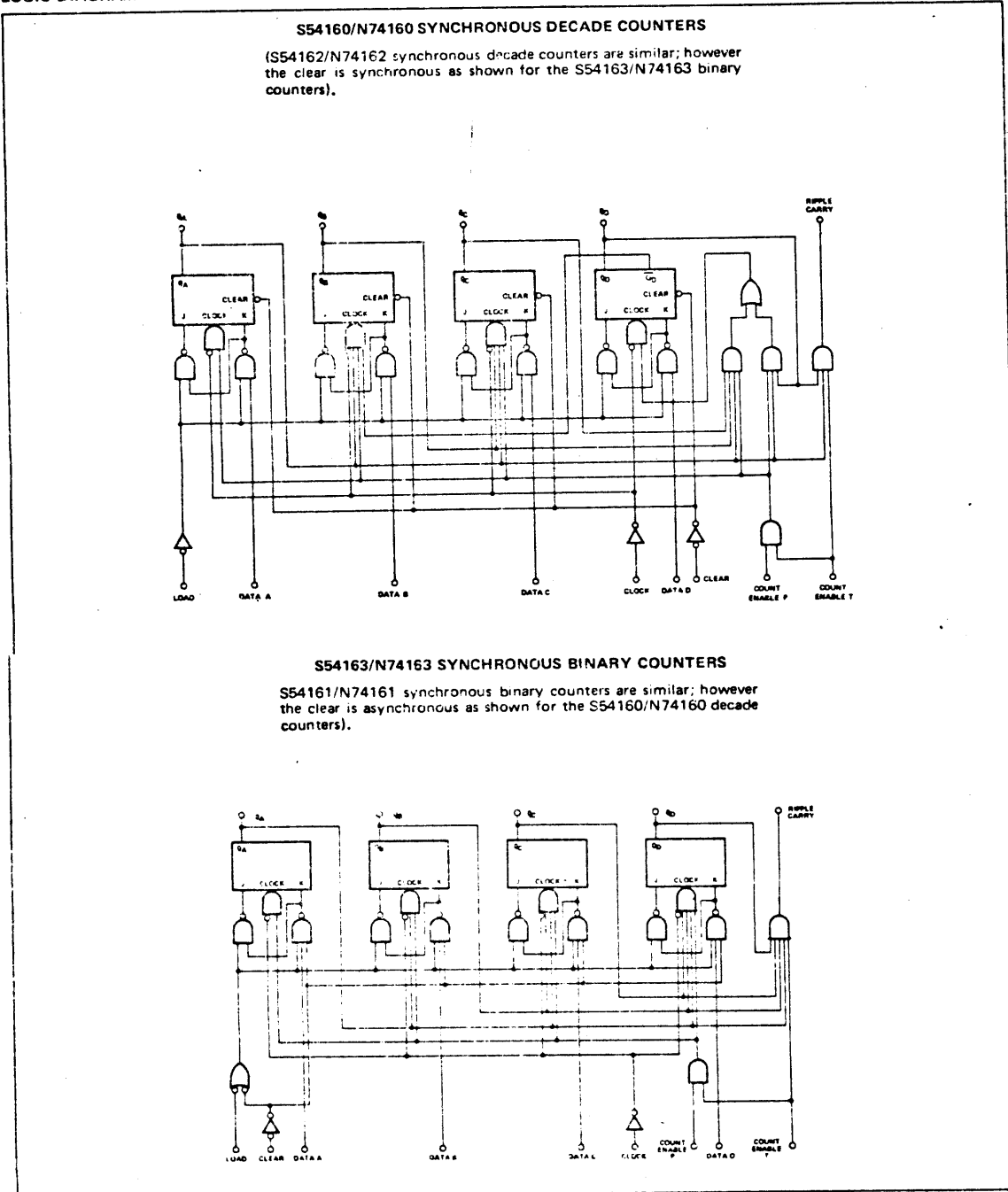
These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting schemes. The S54160, S54162, N74160, and N74162 are decade counters and the S54161, S54163, N74161, and N74163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four J-K master-slave flip-flops on the rising (positive-going) edge of the clock input waveform.

All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. A full fan-out to ten normalized Series 54/74 loads is available from each of the outputs in the low-level state. A fan-out to 20 normalized Series 54/74 loads is provided in the high-level state to facilitate connection of unused inputs and power dissipation is typically 325 milliwatts.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



74163 cont'd

RECOMMENDED OPERATING CONDITIONS

	S54160, S54161 S54162, S54163			N74160, N74161 N74162, N74163			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N:	High logic level			20			
	Low logic level			10			
Input Clock Frequency, $f_{clock}$	0		25	0		25	MHz
Width of Clock Pulse, $t_w(\text{clock})$	25			25			ns
Width of Clear Pulse, $t_w(\text{clear})$	20			20			ns
Setup Time, $t_{setup}$ :	Data Inputs, A,B,C,D			15			
	Enable P			20			
	Load			15			
	Clear			20			
Hold Time at any Input, $t_{hold}$	0			0			ns
Operating Free-Air Temperature, $T_A$	-55	25	125	0	25	70	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise specified)

PARAMETER	TEST CONDITIONS*	S54160, S54161 S54162, S54163			N74160, N74161 N74162, N74163			UNIT
		MIN	TYP**	MAX	MIN	TYP**	MAX	
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$V_I$	Input clamp voltage			-1.5			-1.5	V
$V_{OH}$	High-level output voltage	2.4			2.4			V
$V_{OL}$	Low-level output voltage			0.4			0.4	V
$I_I$	Input current at maximum input voltage			1			1	mA
$I_{IH}$	High-level Clock or enable T input current - Other inputs			80			80	$\mu\text{A}$
	Low-level Clock or enable T input current - Other inputs			40			40	$\mu\text{A}$
$I_{IL}$	High-level Clock or enable T input current - Other inputs			-3.2			-3.2	mA
	Low-level Clock or enable T input current - Other inputs			-1.6			-1.6	mA
$I_{OS}$	Short-circuit output current†	-20		-57	-18		-57	mA
$I_{CCL}$	Supply current, all outputs high		59	85		59	94	mA
	Supply current, all outputs low		63	91		63	101	mA

SWITCHING CHARACTERISTICS,  $V_{CC} = 5\text{V}$ ,  $T_A = 25^{\circ}\text{C}$ ,  $N = 10$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{max}$	Maximum input clock frequency	25	32		MHz
$t_{PLH}$	Propagation delay time, low-to-high-level carry output from clock		23	35	ns
$t_{PHL}$	Propagation delay time, high-to-low-level carry output from clock		23	35	ns
$t_{PLH}$	Propagation delay time, low-to-high-level Q output from clock		13	20	ns
$t_{PHL}$	Propagation delay time, high-to-low-level Q output from clock		15	23	ns
$t_{PLH}$	Propagation delay time, low-to-high-level carry output from enable T		8	13	ns
$t_{PHL}$	Propagation delay time, high-to-low-level carry output from enable T		10	15	ns
$t_{PHL}$	Propagation delay time, high-to-low-level Q output from clear		20	30	ns

\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

\*\* All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^{\circ}\text{C}$ .

† Not more than one output should be shorted at a time.

NOTES:

3.  $I_{CCH}$  is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.

4.  $I_{CCL}$  is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

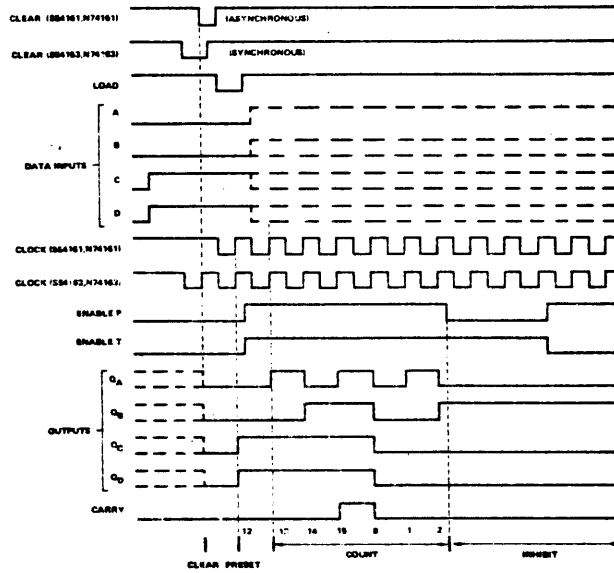
D COMPONENT DESCRIPTION  
 D.6 INTEGRATED CIRCUITS

74163 cont'd.

TYPICAL CLEAR, PRESET, COUNT, AND INHIBIT SEQUENCES FOR 54161, 74161, 54163, 74163 SYNCHRONOUS BINARY COUNTERS

Illustrated below is the following sequence:

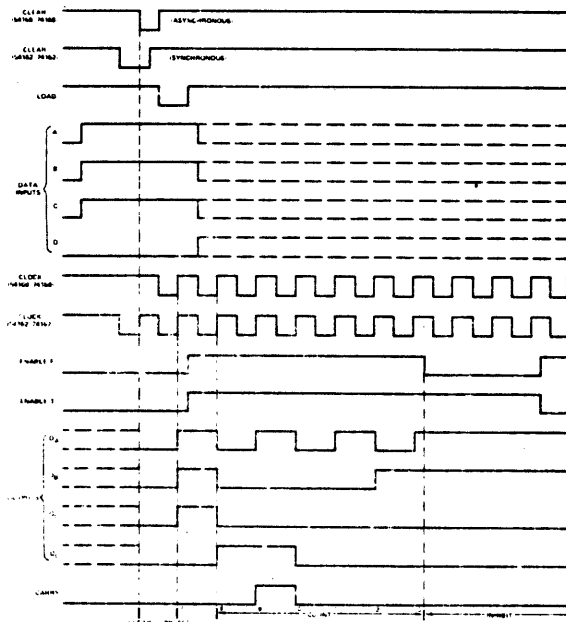
1. Clear outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.



TYPICAL CLEAR, PRESET, COUNT, AND INHIBIT SEQUENCES FOR 54160, 54162, 74160, 74162 SYNCHRONOUS BINARY COUNTERS

Illustrated below is the following sequence:

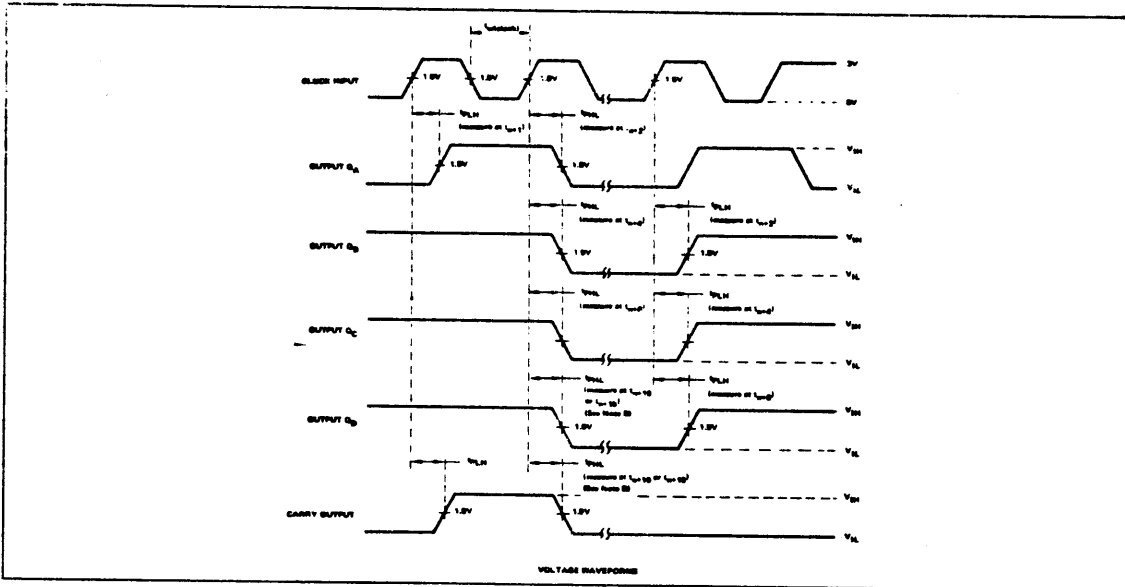
1. Clear outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two, and three.
4. Inhibit.



D COMPONENT DESCRIPTION  
 D.6 INTEGRATED CIRCUITS

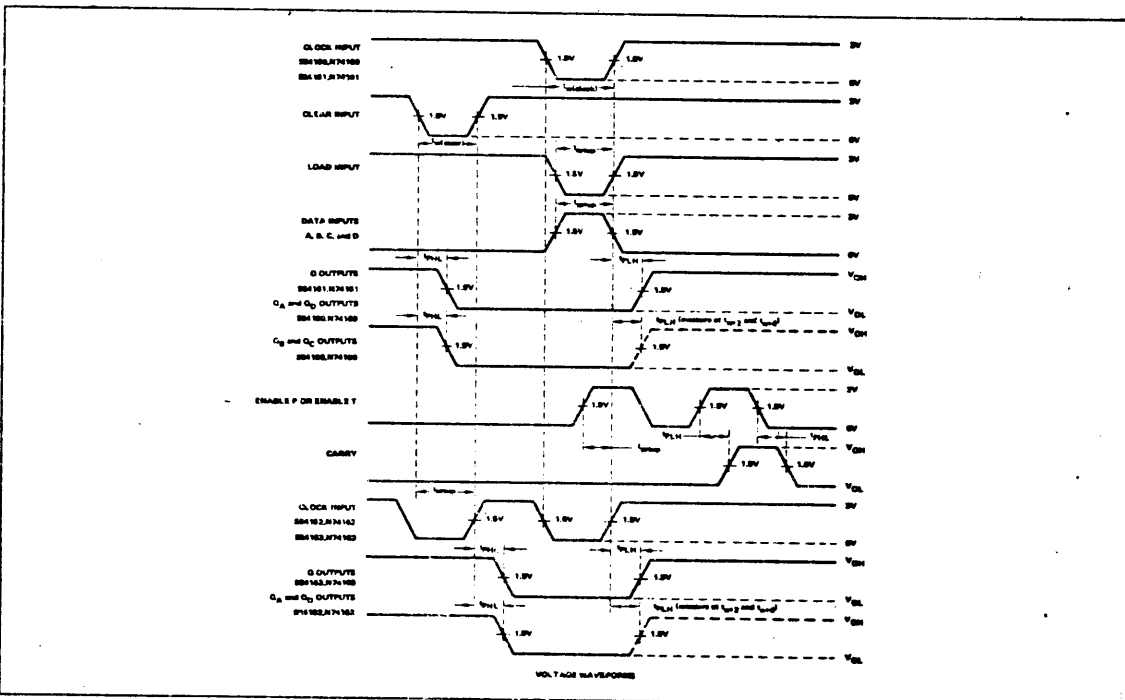
74163 cont'd

PARAMETER MEASUREMENT INFORMATION



NOTES:

- The input pulses are supplied by a generator having the following characteristics:  $t_r < 10ns$ ;  $t_f < 10ns$ ; PRR  $< 1$  MHz, duty cycle  $< 50\%$ ,  $Z_{out} \approx 50\Omega$ . Vary PRR to measure  $t_{max}$ .
- Outputs  $Q_D$  and carry are tested at  $t_{n+10}$  for the S54160, S54162, N74160, and N74162, and at  $t_{n+16}$  for the S54161, S54163, N74161, and N74163, where  $t_n$  is the bit time when all outputs are low.

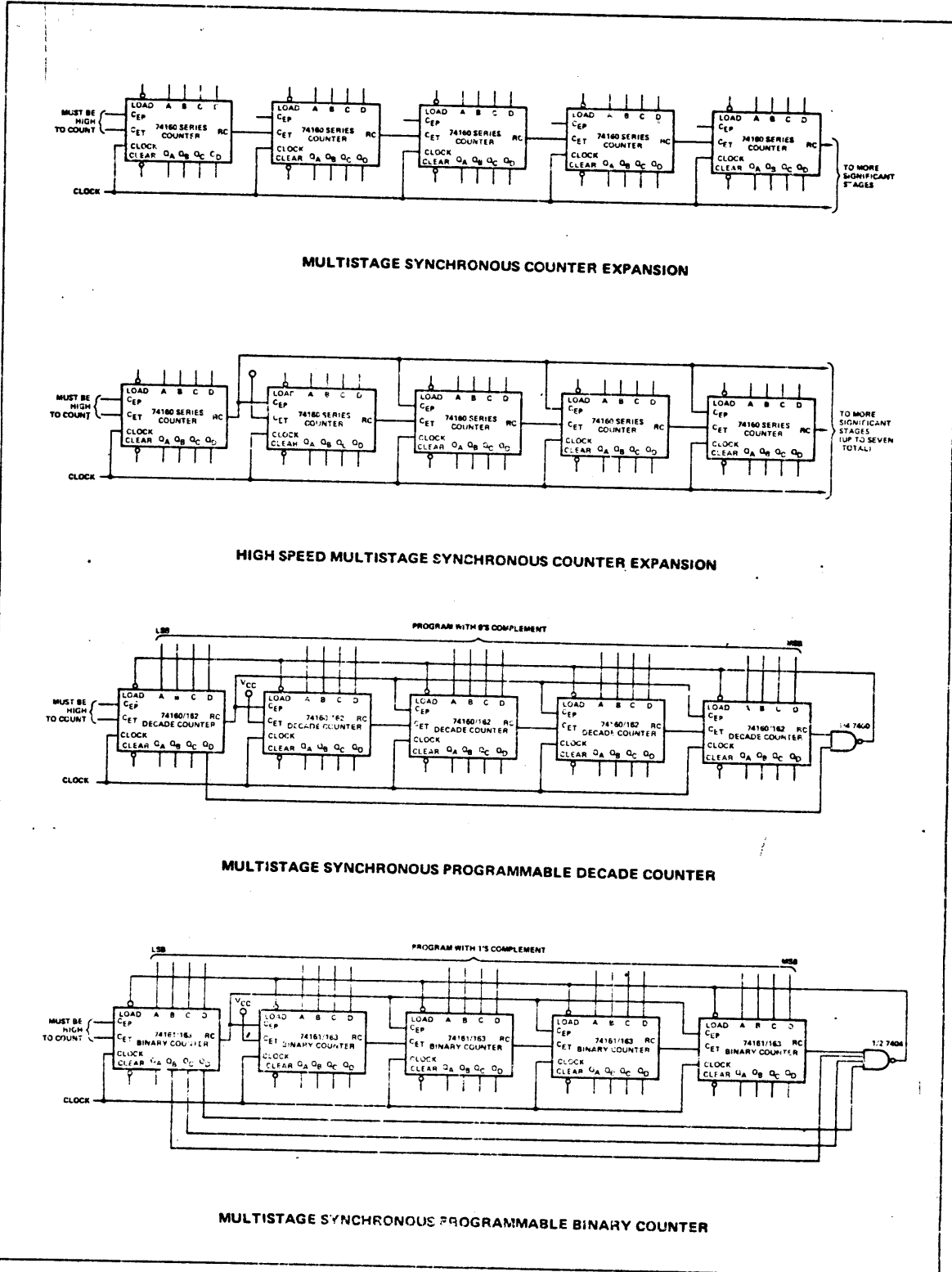


NOTES:

- The input pulses are supplied by a generator having the following characteristics:  $t_r < 10ns$ ;  $t_f < 10ns$ ; PRR  $< 1$  MHz, duty cycle  $< 50\%$ ,  $Z_{out} \approx 50\Omega$ .
- Enable P and enable T setup times are measured at  $t_n = 0$ .

D COMPONENT DESCRIPTION  
 D.6 INTEGRATED CIRCUITS

74163 cont'd  
 TYPICAL APPLICATIONS



74166

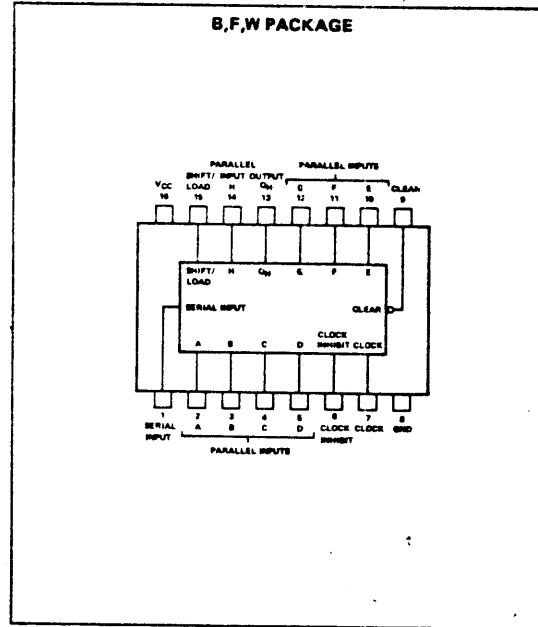
**DESCRIPTION**

These 8-bit shift registers are compatible with most other TTL, DTL, and MSI logic families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input clamping diodes minimize switching transients to simplify system design. Maximum input clock frequency is typically 35 megahertz and power dissipation is typically 360 mW.

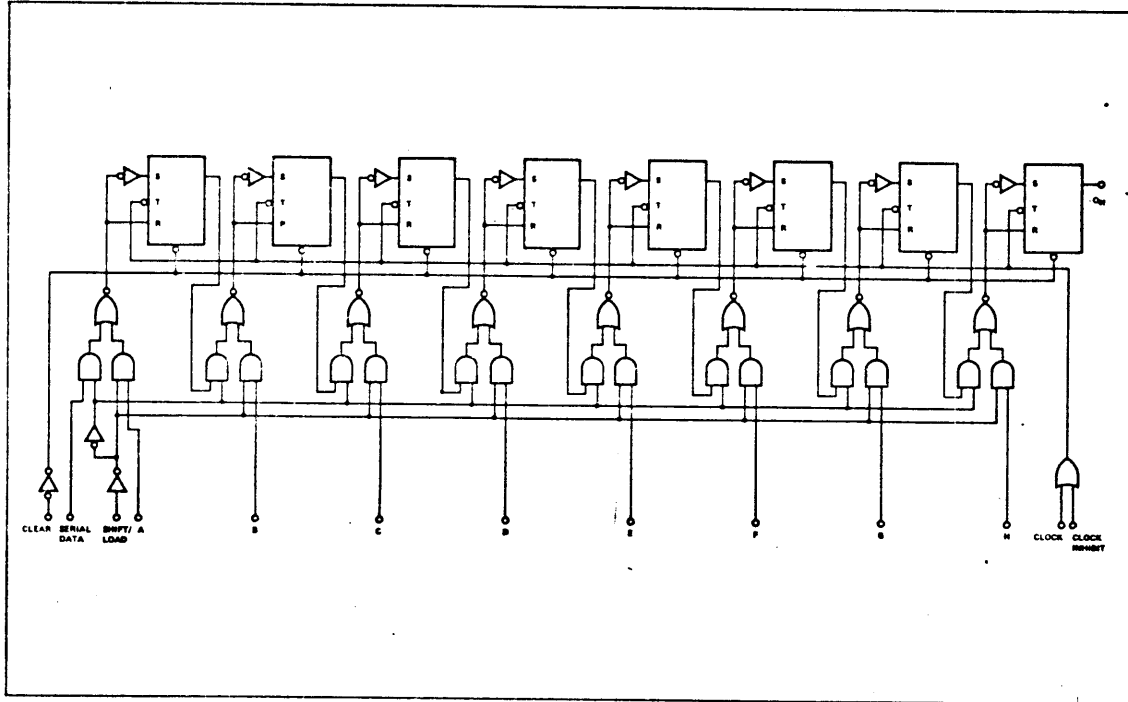
All Series 54 devices are characterized for operation over the full military temperature range of -55°C to 125°C. Series 74 devices are characterized for operation from 0°C to 70°C.

These parallel-in or serial-in, serial-out shift registers have a complexity of 77 equivalent gates on a monolithic chip. They feature gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This, of course, allows the system clock to be free-running and the register can be stopped on command with the gate input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock and sets all flip-flops to zero. Average power dissipation per gate is typically 4.7 mW.

**PIN CONFIGURATIONS**



**LOGIC DIAGRAM**



**RECOMMENDED OPERATING CONDITIONS**

	S54166			N74166			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level Low logic level			20 10			20 10	
Input Circuit Frequency, $f_{count}$	0		25	0		25	MHz
Width of Clock or Clear Pulse, $t_w$	20			20			ns
Mode-Control Setup Time, $t_{setup}$	30			30			ns
Data Setup Time, $t_{setup}$	20			20			ns
Hold Time at any Input, $t_{hold}$	0			0			ns
Operating Free-Air Temperature, $T_A$	-55	25	125	0	25	70	°C

74166 cont'd

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	S54166			N74166			UNIT
		MIN	TYP <sup>†</sup>	MAX	MIN	TYP <sup>†</sup>	MAX	
V <sub>IH</sub> High-level input voltage		2			2			V
V <sub>IL</sub> Low-level input voltage				0.8			0.8	V
V <sub>I</sub> Input clamp voltage	V <sub>CC</sub> = MAX, I <sub>I</sub> = -12mA			-1.5			-1.5	V
V <sub>OH</sub> High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2V, V <sub>IL</sub> = 0.8V, I <sub>OH</sub> = -800μA	2.4			2.4			V
V <sub>OL</sub> Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2V, V <sub>IL</sub> = 0.8V, I <sub>OL</sub> = 12mA			0.4			0.4	V
I <sub>I</sub> Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5V			1			1	mA
I <sub>IH</sub> High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4V			40			40	μA
I <sub>IL</sub> Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4V			-1.6			-1.6	mA
I <sub>OS</sub> Short-circuit output current†	V <sub>CC</sub> = MAX	-20		-57	-18		-57	mA
I <sub>CC</sub> Supply current	V <sub>CC</sub> = MAX, Table Below		72	104		72	116	mA

SWITCHING CHARACTERISTICS, V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C, N = 10

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>max</sub> Maximum input count frequency		25	35		MHz
t <sub>PHL</sub> Propagation delay time, high-to-low-level output from clear	C <sub>L</sub> = 15pF, R <sub>L</sub> = 400Ω		23	35	ns
t <sub>PHL</sub> Propagation delay time, high-to-low-level output from clock		8	20	30	ns
t <sub>PLH</sub> Propagation delay time, low-to-high-level output from clock		8	17	26	ns

- \* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- \*\* All typical values are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.
- † Not more than one output should be shorted at a time.

TEST CONDITIONS FOR I<sub>CC</sub> (all outputs are open)

TYPE	APPLY 4.5V	FIRST GROUND, THEN APPLY 4.5V	GROUND
S54166, N74166	Serial Input	Clock	All other inputs

74174

DESCRIPTION

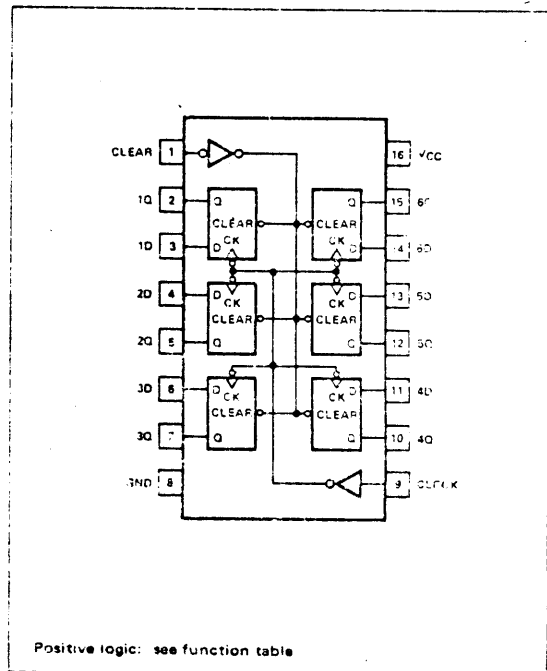
These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. The 54/74174 has a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These circuits are fully compatible for use with most TTL or DTL circuits. A full fanout to 10 normalized Series 54/74 loads is available from each output at low logic levels, and to 20 loads at high logic levels to facilitate connection of unused inputs to used inputs. Maximum clock frequency is typically 35 MHz with a typical power dissipation of 38 milliwatts per flip-flop.

The S54174 characterized for operation over the full military temperature range of -55°C to 125°C. The N74174 is characterized for operation from 0°C to 70°C.

PIN CONFIGURATION (Top View)



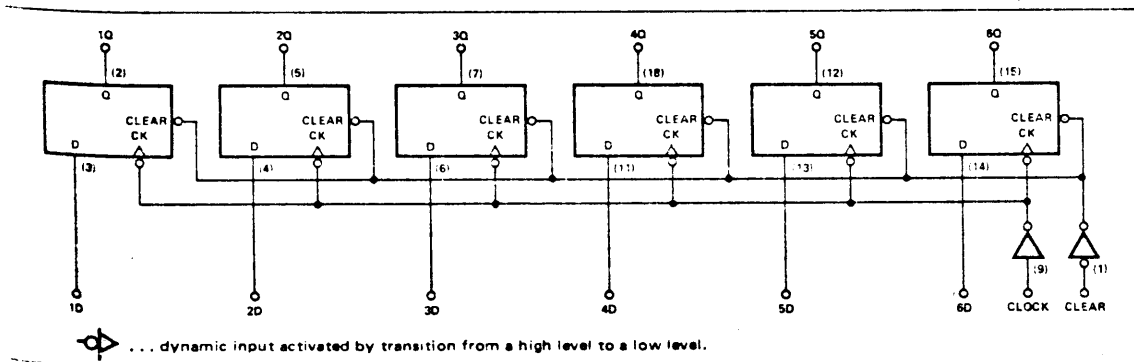
Positive logic: see function table

74174 cont'd

FUNCTION TABLE (Each Flip-Flop)

Clock	INPUTS		OUTPUTS	H high level (steady state) L low level (steady state) X irrelevant ↑ transition from low to high level Q <sub>0</sub> the level of Q before the indicated steady state input conditions were established.
	D	Q	Q	
L	X	X	H	
H	↑	H	H	
H	↑	L	L	
H	L	X	Q <sub>0</sub>	

FUNCTIONAL BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	S54174			N74174			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V <sub>CC</sub>	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	high logic level			20			
	low logic level			10			
Input clock frequency, f <sub>clock</sub>	0		25	0		25	MHz
Width of clock or clear pulse, t <sub>w</sub> (see Figure 1)	20			20			ns
Setup time, t <sub>setup</sub> (see Figure 1)	data input			20			ns
	clear inactive-state			25			
Data hold time, t <sub>hold</sub> (see Figure 1)	0			0			ns
Operating free-air temperature, T <sub>A</sub>	-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>†</sup>	MIN	TYP <sup>‡</sup>	MAX	UNIT
V <sub>IH</sub>	High-level input voltage		2		V
V <sub>IL</sub>	Low-level input voltage			0.8	V
V <sub>I</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA		-1.5	V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2V, V <sub>IL</sub> = 0.8V, I <sub>OH</sub> = -800 μA		2.4	V
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2V, V <sub>IL</sub> = 0.8V, I <sub>OL</sub> = 16 mA		0.4	V
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5V		1	mA
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4V		40	μA
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4V		-1.6	mA
I <sub>OS</sub>	Short-circuit output current <sup>§</sup>	V <sub>CC</sub> = MAX		-20	mA
		SN54174, SN74174		-57	
I <sub>CC</sub>	Supply current	V <sub>CC</sub> = MAX, See Note 1		45	65
		SN54174, SN74174		30	
		SN54175, SN74175		45	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 1: With all outputs open and 4.5V applied to all data and clear inputs, I<sub>CC</sub> is measured after a momentary ground, then 4.5V is applied to clock.

SWITCHING CHARACTERISTICS, V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C, N = 10

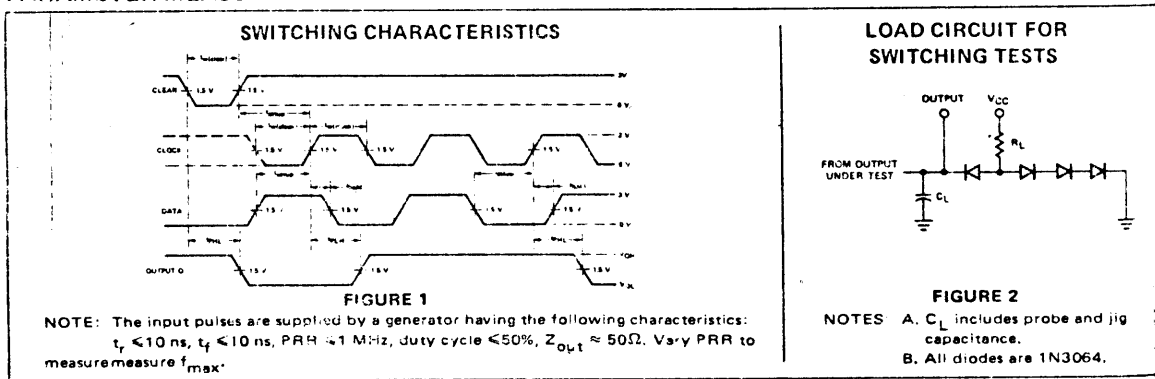
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>max</sub>	Maximum input clock frequency	25	35		MHz
t <sub>PHL</sub>	Propagation delay time, high-to-low-level output from clear		23	35	ns
t <sub>PLH</sub>	Propagation delay time, low-to-high-level output from clock		20	30	ns
t <sub>PHL</sub>	Propagation delay time, high-to-low-level output from clock		21	30	ns

C<sub>L</sub> = 15 pF, R<sub>L</sub> = 400 Ω  
See Figures 1 and 2



74174 cont'd

PARAMETER MEASUREMENT INFORMATION



8096, 8097, 8098

general description

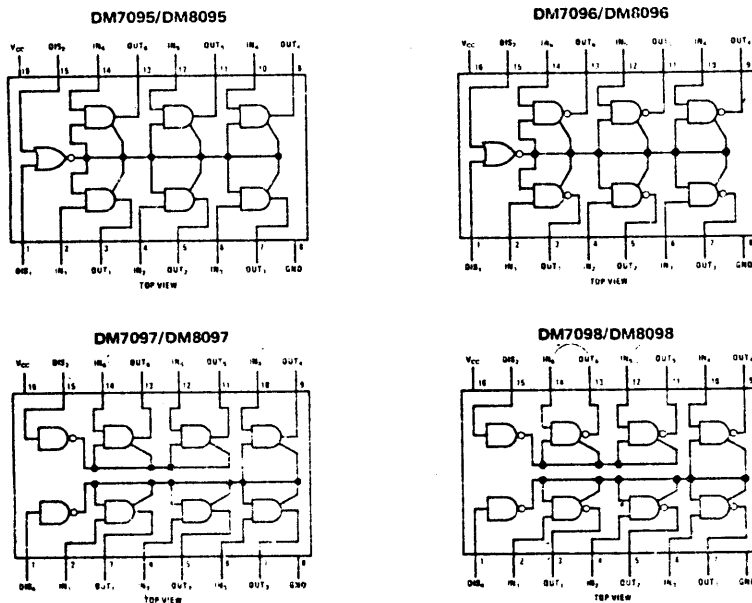
Each of the devices described herein are used to convert standard TTL or DTL outputs to TRI-STATE outputs. The DM7095/DM8095 and the DM7097/DM8097 do so with no logic inversion; the DM7096/DM8096 and DM7098/DM8098 provide the logical opposite of the input signal. The DM7095/DM8095 and DM7096/DM8096 control all six devices from common inputs; the DM7097/DM8097 and DM7098/DM8098 control

four devices from one input and two from another input.

features

- Maximum package utilization
- Typical power dissipation  
DM7095/DM8095, DM7097/DM8097 325 mW  
DM7096/DM8096, DM7098/DM8098 295 mW
- Typical propagation delay 15 ns

connection diagrams (Dual-In-Line and Flat Packages)



truth tables

DM7095/DM8095

DISABLE DIS <sub>1</sub>	INPUT DIS <sub>2</sub>	INPUT	OUTPUT
0	0	0	0
0	0	1	1
0	1	X	H <sub>Z</sub>
1	0	X	H <sub>Z</sub>
1	1	X	H <sub>Z</sub>

DM7096/DM8096

DISABLE DIS <sub>1</sub>	INPUT DIS <sub>2</sub>	INPUT	OUTPUT
0	0	0	1
0	0	1	0
0	1	X	H <sub>Z</sub>
1	0	X	H <sub>Z</sub>
1	1	X	H <sub>Z</sub>

DM7097/DM8097

DISABLE DIS <sub>4</sub>	INPUT DIS <sub>2</sub>	INPUT	OUTPUT
0	0	0	0
0	0	1	1
X	1	X	H <sub>Z</sub> *
1	X	X	H <sub>Z</sub> **

DM7098/DM8098

DISABLE DIS <sub>4</sub>	INPUT DIS <sub>2</sub>	INPUT	OUTPUT
0	0	0	1
0	0	1	0
X	1	X	H <sub>Z</sub> *
1	X	X	H <sub>Z</sub> **

\*Output 5,6 only  
\*\*Output 1,4 only  
X = Irrelevant

D COMPONENT DESCRIPTION  
D.6 INTEGRATED CIRCUITS

8096, 8097, 8098 cont'd

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Time that 2 bus-connected devices may be in opposite low-impedance states simultaneously . . .	Indefinite

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V <sub>CC</sub> )	4.5	5.5	V
DM7095/6/7/8	4.75	5.25	V
DM8095/6/7/8			
Temperature (T <sub>A</sub> )	-55	+125	°C
DM7095/6/7/8	0	70	°C
DM8095/6/7/8			

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V <sub>CC</sub> = Min T <sub>A</sub> = 25°C	2.0			V
Logical "0" Input Voltage	V <sub>CC</sub> = Min			0.8	V
Logical "1" Output Voltage	DM7095/6/7/8 DM8095/6/7/8 V <sub>CC</sub> = Min I <sub>O</sub> = -2.0 mA I <sub>O</sub> = -5.2 mA	2.4			V
Logical "0" Output Voltage	V <sub>CC</sub> = Min I <sub>O</sub> = 32 mA			0.4	V
Third State Input Current	V <sub>CC</sub> = Max V <sub>IN</sub> = 0.5V DIS = 2.0V			-40	μA
Third State Output Current	V <sub>CC</sub> = Max V <sub>O</sub> = 2.4V V <sub>O</sub> = 0.4V			40 -40	μA μA
Logical "1" Input Current	V <sub>CC</sub> = Max V <sub>IN</sub> = 2.4V V <sub>IN</sub> = 5.5V			40 1	μA mA
Logical "0" Input Current	V <sub>CC</sub> = Max V <sub>IN</sub> = 0.4V DIS = 0.4V			-1.6	mA
Output Short Circuit Current (Note 3)	V <sub>CC</sub> = Max V <sub>O</sub> = 0V	-40	-80	-115	mA
Supply Current (each device)	DM7095/7 DM8095/7 DM7096/8 DM8096/8 V <sub>CC</sub> = Max		65 59	85 77	mA
Input Clamp Voltage	V <sub>CC</sub> = Min I <sub>IN</sub> = -12 mA			-1.5	V
Propagation Delay to a Logical "0" from Data Input to Output, t <sub>pd0</sub>	DM7095/7 DM8095/7 DM7096/8 DM8096/8 V <sub>CC</sub> = 5.0V T <sub>A</sub> = 25°C		14	22	ns
Propagation Delay to a Logical "1" from Data Input to Output, t <sub>pd1</sub>	DM7095/7 DM8095/7 DM7096/8 DM8096/8 V <sub>CC</sub> = 5.0V T <sub>A</sub> = 25°C		10	16	ns
Propagation Delay to a Logical "1" from Data Input to Output, t <sub>pd1</sub>	DM7095/7 DM8095/7 DM7096/8 DM8096/8 V <sub>CC</sub> = 5.0V T <sub>A</sub> = 25°C		10	16	ns
Delay from Disable Input to High Impedance State (from Logical "1" Level), t <sub>1H</sub>	V <sub>CC</sub> = 5.0V T <sub>A</sub> = 25°C		6	11	ns
Delay from Disable Input to High Impedance State (from Logical "0" Level), t <sub>0H</sub>	V <sub>CC</sub> = 5.0V T <sub>A</sub> = 25°C		16	27	ns
Delay from Disable Input to Logical "1" Level (from High Impedance State), t <sub>H1</sub>	V <sub>CC</sub> = 5.0V T <sub>A</sub> = 25°C		21	35	ns
Delay from Disable Input to Logical "0" Level (from High Impedance State), t <sub>H0</sub>	V <sub>CC</sub> = 5.0V T <sub>A</sub> = 25°C		24	37	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the -55°C to +125°C temperature range for the DM7095/6/7/8 and across the 0°C to 70°C range for the DM8095/6/7/8. All typicals are given for V<sub>CC</sub> = 5.0V and T<sub>A</sub> = 25°C.

Note 3: Only one output at a time should be shorted.

D COMPONENT DESCRIPTION  
 D.6 INTEGRATED CIRCUITS

8123

**general description**

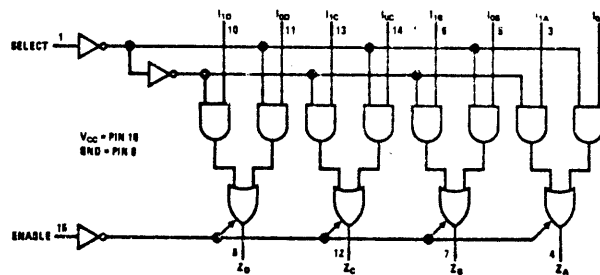
The DM7123/DM8123 consists of four 2-input multiplexers with common input select logic and common output disable circuitry. It allows two groups of four bits each to be multiplexed to four parallel outputs. When the Enable input is at the logical "0" level the outputs are conventional TTL. However, when a logical "1" is applied, the outputs assume a high-impedance state. Both upper and lower output transistors are turned off and the resulting condition allows many devices to be connected to a common bus line without loading down or being loaded down by other devices on the line.

The DM7123/DM8123 is pin compatible and functionally compatible with the FSC 9322 and the SN54157/SN74157 except for the TRI-STATE capability.

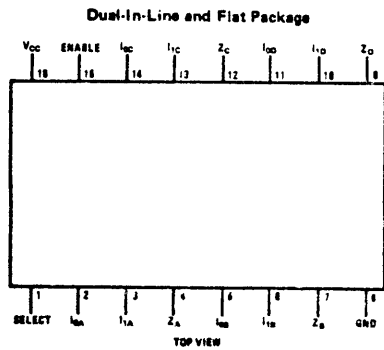
**features**

- Typically 10 ns from data to output
- Power dissipation 200 mW typ
- TRI-STATE outputs
- Pin compatible with FSC 9322 and SN54157/SN74157
- Diode clamped inputs

**logic diagram**



**connection diagram**



**truth table**

ENABLE	SELECT	INPUT I <sub>0</sub> I <sub>1</sub>	OUTPUT
1	X	X X	Hi-Z State
0	1	X 0	0
0	1	X 1	1
0	0	0 X	0
0	0	1 X	1

D COMPONENT DESCRIPTION  
 D.6 INTEGRATED CIRCUITS

8123 cont'd

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Operating Temperature Range	
DM7123	-55°C to 125°C
DM8123	0°C to 70°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7123 $V_{CC} = 4.5V$ DM8123 $V_{CC} = 4.75V$	2.0			V
Logical "0" Input Voltage	DM7123 $V_{CC} = 4.5V$ DM8123 $V_{CC} = 4.75V$			.8	V
Logical "1" Output Voltage	DM7123 $V_{CC} = 4.5V$ $I_{OUT} = -2.0 mA, V_{IN} = 2V$ DM8123 $V_{CC} = 4.75V$ $I_{OUT} = -5.2 mA, V_{IN} = 2V$	2.4			V
Logical "0" Output Voltage	DM7123 $V_{CC} = 4.5V$ $I_{OUT} = 16 mA, V_{IN} = .8V$ DM8123 $V_{CC} = 4.75V$			.4	V
Third State Output Current	DM7123 $V_{CC} = 5.5V$ $0.40 \leq V_{OLH} \leq 2.4V$ DM8123 $V_{CC} = 5.25V$ $V_{IN} (Enable) = 2V$	-40		40	$\mu A$
Logical "1" Input Current	DM7123 $V_{CC} = 5.5V$ DM8123 $V_{CC} = 5.25V$ $V_{IN} = 2.4V$			40	$\mu A$
	DM7123 $V_{CC} = 5.5V$ $V_{IN} = 5.5V$ DM8123 $V_{CC} = 5.25V$			1	mA
Logical "0" Input Current	DM7123 $V_{CC} = 5.5V$ $V_{IN} = 0.4V$ DM8123 $V_{CC} = 5.25V$		-1.0	-1.6	mA
Output Short Circuit Current (Note 3)	DM7123 $V_{CC} = 5.5V$ $V_{IN} = 4.5V$ DM8123 $V_{CC} = 5.25V$	-30	-50	-70	mA
Supply Current	DM7123 $V_{CC} = 5.5V$ $V_{IN} (Enable) = 4.5V$ DM8123 $V_{CC} = 5.25V$ Other Inputs 0V		40	51	mA
Input Clamp Voltage	DM7123 $V_{CC} = 5.0V$ DM8123 $T_A = 25^\circ C$ $I_{IN} = -12 mA$		-1.0	-1.5	V
Propagation Delay to a Logical "0" from Data to Output, $t_{p00}$	$V_{CC} = 5.0V$ $T_A = 25^\circ C$	5	11	18	ns
Propagation Delay to a Logical "0" from Select to $Z_A$ , $t_{p00}$	$V_{CC} = 5.0V$ $T_A = 25^\circ C$	8	17	24	ns
Propagation Delay to a Logical "1" from Data to Output, $t_{p01}$	$V_{CC} = 5.0V$ $T_A = 25^\circ C$	4	8	15	ns
Propagation Delay to a Logical "1" from Select to $Z_A$ , $t_{p01}$	$V_{CC} = 5.0V$ $T_A = 25^\circ C$	5	15	23	ns
Delay from Disable to High Impedance State (from Logical "1" Level), $t_{1H}$	$V_{CC} = 5.0V$ $T_A = 25^\circ C$	4	7	11	ns
Delay from Disable to High Impedance State (from Logical "0" Level), $t_{0H}$	$V_{CC} = 5.0V$ $T_A = 25^\circ C$	9	19	27	ns
Delay from Disable to Logical "1" Level (from High Impedance State), $t_{H1}$	$V_{CC} = 5.0V$ $T_A = 25^\circ C$	9	18	25	ns
Delay from Disable to Logical "0" Level (from High Impedance State), $t_{H0}$	$V_{CC} = 5.0V$ $T_A = 25^\circ C$	10	23	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the -55°C to +125°C temperature range for the DM7123 and across the 0°C to 70°C range for the DM8123. All typicals are given for  $V_{CC} = 5.0V$  and  $T_A = 25^\circ C$ .

Note 3: Only one output at a time should be shorted.

D COMPONENT DESCRIPTION  
 D.6 INTEGRATED CIRCUITS

8833

general description

This family of TRI-STATE® party line transceivers offer extreme versatility in bus organized data transmission systems. The data bus may be unterminated, or terminated DC or AC at one or both ends. Drivers in the third (high impedance) state load the data bus with a negligible leakage current. The receiver input current is low allowing at least 100 driver/receiver pairs to utilize a single bus. The bus loading is unchanged when  $V_{CC} = 0V$ . The receiver incorporates hysteresis to provide greater noise immunity. All devices utilize a high current TRI-STATE output driver. The DM7833/DM8833 and DM7835/DM8835 employ TRI-STATE outputs on the receiver also, while on the DM7834/DM8834 and DM7839/DM8839 the receiver outputs are standard active pull up T<sup>2</sup>L.

The DM7833/DM8833 are non-inverting quad transceivers with a common driver disable control and a common receiver disable control.

The DM7839/DM8839 are non-inverting quad transceivers with a common two-input driver disable control.

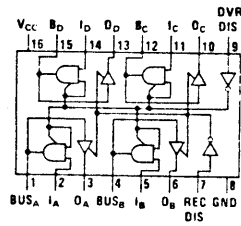
The DM7834/DM8834 are inverting quad transceivers with a common two input driver disable control.

The DM7835/DM8835 are inverting quad transceivers with a common driver disable control and a common receiver disable control.

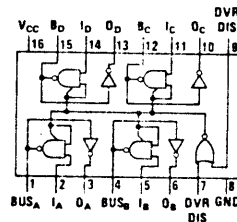
features

- Receiver hysteresis 450 mV (typ)
- Receiver noise immunity 1.4V (typ)
- Receiver input current 50  $\mu A$  (max) for normal  $V_{CC}$  or  $V_{CC} = 0V$
- Receivers
  - Sink 16 mA at 0.4V (max)
  - Source 2.0 mA (mil) at 2.4V (min)  
5.2 mA (com)
- Drivers
  - Sink 50 mA at 0.5V (max) or 32 mA at 0.4V (max)
  - Source 10.4 mA at 2.4V (min)
- Drivers have TRI-STATE outputs
- DM7833/DM8833 and DM7835/DM8835 receivers have TRI-STATE outputs
- Capable of driving 100 $\Omega$  DC terminated buses
- 74 series TTL compatible

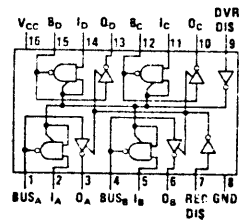
connection diagrams



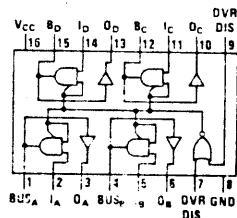
TOP VIEW  
 DM7833/DM8833



TOP VIEW  
 DM7834/DM8834



TOP VIEW  
 DM7835/DM8835



TOP VIEW  
 DM7839/DM8839

D COMPONENT DESCRIPTION  
 D.6 INTEGRATED CIRCUITS

9601

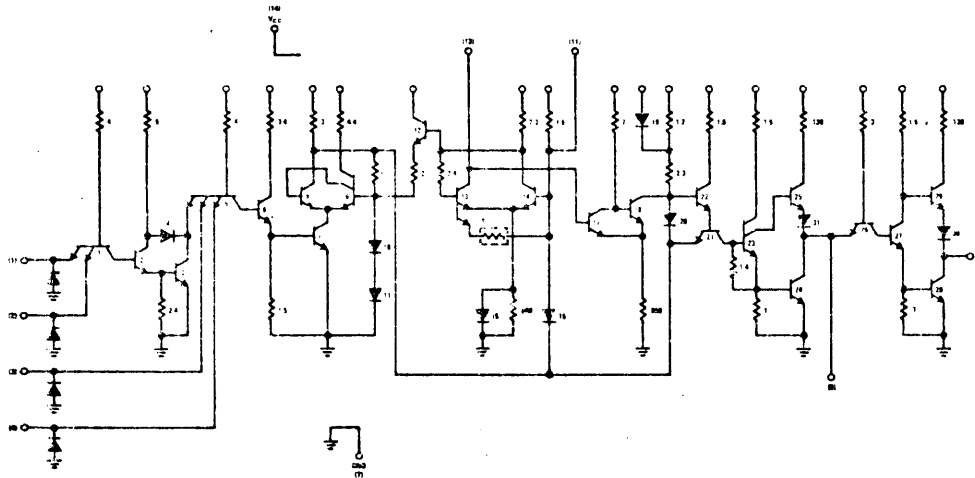
**general description**

The DM9601/DM8601 is both pin-for-pin and spec-for-spec interchangeable with the 9601 one-shot. Pulse widths range from 50 ns upward depending upon the values of the external R&C used. The retriggerable feature allows for output pulse widths to be extended beyond the normal range attainable with just a resistor and capacitor.

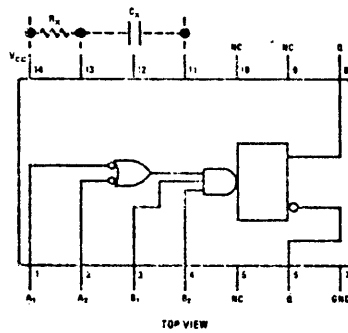
**features**

- Input Clamping Diodes
- Complementary DC Level Sensitive Inputs
- Flexibility of Operation—Optional Retriggering/Lockout Capability
- DTL/TTL Compatible Logic Levels
- High Speed Operation—Input Repetition Rate > 10 MHz
- Output Pulse Width Range 50 ns to  $\infty$
- Leading or Trailing Edge Triggering
- Complementary Outputs

**schematic and connection diagrams**



Dual-In-Line and Flat Package



D COMPONENT DESCRIPTION  
D.6 INTEGRATED CIRCUITS

9601 cont'd

**DM9601**

**absolute maximum ratings**

Supply Voltage to Ground	-0.5V to +8.0V
Input Voltage	-0.5V to +5.5V
Voltage Applied to Outputs	-0.5V to +V <sub>CC</sub>
Storage Temperature	-65°C to +150°C
Operating Temperature	-55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

**electrical characteristics**

TABLE 1

Symbol	Parameter	Limits						Units	Conditions (Note 1)	
		-55°C		-25°C			+125°C			
		Min.	Max.	Min.	Typ.	Max.	Min.			Max.
V <sub>OH</sub>	Output High Voltage	2.4		2.4	3.3		2.4		V	V <sub>CC</sub> = 4.5V I <sub>OH</sub> = -0.72 mA (Note 2)
V <sub>OL</sub>	Output Low Voltage		0.4		0.2	0.4		0.4	V	V <sub>CC</sub> = 4.5V I <sub>OL</sub> = 10 mA (Note 2)
V <sub>IH</sub>	Input High Voltage	2.0		1.7				1.4	V	V <sub>CC</sub> = 4.5V
V <sub>IL</sub>	Input Low Voltage		0.85			0.90		0.85	V	V <sub>CC</sub> = 5.5V (Note 3)
I <sub>I</sub>	Input Load Current		-1.6		-1.1	-1.6		-1.6	mA	V <sub>CC</sub> = 5.5V V <sub>I</sub> = 0.4V
I <sub>R</sub>	Input Leakage Current				15	60		60	μA	V <sub>CC</sub> = 5.5V V <sub>I</sub> = 4.5V
I <sub>SC</sub>	Short Circuit Current			-10		-40				V <sub>CC</sub> = 5.0V V <sub>OUT</sub> = 0V (Note 2)
I <sub>PD</sub>	Quiescent Power Supply Drain		25			25		25	mA	V <sub>CC</sub> = 5.5V
t <sub>pd-</sub>	Negative Trigger Input to True Output				25	40			ns	V <sub>CC</sub> = 5.0V R <sub>X</sub> = 5.0 KΩ
t <sub>pd-</sub>	Negative Trigger input to Complement Output				25	40			ns	C <sub>X</sub> = 0 C <sub>L</sub> = 15 pF
t <sub>pw(min)</sub>	Minimum True Output Pulse Width				45	65			ns	R <sub>X</sub> = 5.0 KΩ
t <sub>pw</sub>	Pulse Width			3.03	3.42	3.76			μs	V <sub>CC</sub> = 5.0V R <sub>X</sub> = 10 KΩ, C <sub>X</sub> = 1,000 pF
C <sub>stray</sub>	Maximum Allowable Wiring Capacitance (Pin 13)		50			50		50	pF	Pin 13 to GND
R <sub>X</sub>	External Timing Resistor	5.0	25	5.0		25	5.0	25	kΩ	

**Note 1:** Unless otherwise specified, R<sub>X</sub> = 10 KΩ between Pin 13 and V<sub>CC</sub> on all tests.

**Note 2:** Ground Pin 11 for V<sub>OL</sub> test on Pin 6, V<sub>OH</sub> test on Pin 3 and I<sub>SC</sub> test on Pin 8. Open Pin 11 for V<sub>CL</sub> test on Pin 8, V<sub>OH</sub> test on Pin 6 and I<sub>SC</sub> test on Pin 6.

**Note 3:** Pulse test to determine V<sub>IH</sub> and V<sub>IL</sub> (Min PW = 40 ns).

9601 cont'd  
 operating rules

1. An external resistor  $R_X$  and an external capacitor  $C_X$  are required for operation. The value of  $R_X$  can vary between the limits shown on tables I and II. The value of  $C_X$  is optional and may be adjusted to achieve the required output pulse width.
2. Output pulse width  $t_{pw}$  may be calculated as follows:  

$$t_{pw} = 0.32 R_X C_X \left[ 1 + \frac{0.7}{R_X} \right] \text{ (for } C_X \geq 10^3 \text{ pF)}$$
 $R_X$  in  $K\Omega$ ,  $C_X$  in pF and  $t_{pw}$  in ns  
 For  $C_X < 10^3$  pF, see curve.
3.  $R_X$  and  $C_X$  must be kept as close as possible to the circuit in order to minimize stray capaci-

tance and noise pickup. If remote trimming is required,  $R_X$  may be split up such that at least  $R_{X(MIN)}$  must be as close as possible to the circuit and the remote portion of the trimming resistor  $R < R_{X(MAX)} - R_X$ .

4. Set-up time ( $t_1$ ) for input trigger pulse  $> 40$  ns. (See Figure 1)  
 Release time ( $t_2$ ) for input trigger pulse  $> 40$  ns. (See Figure 2)
5. Retrigger pulse width (see Figure 3) is calculated as follows:

$$t_w = t_{pw} + t_{pd} = 0.32 R_X C_X \left[ 1 + \frac{0.7}{R_X} \right] + t_{pd}$$

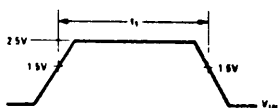


Figure 1

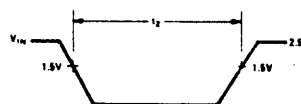


Figure 2

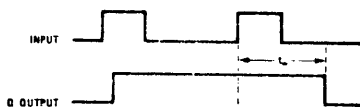


Figure 3

9602

general description

The TTL/Monostable DM9602/DM8602 dual retriggerable, resettable monostable multivibrator provides an output pulse whose duration and accuracy is a function of external timing components. The DM9602/DM8602 has excellent immunity to noise on the  $V_{CC}$  and ground lines. The DM9602/DM8602 uses TTL inputs and outputs for high speed and high fanout capability and is compatible with all members of the TTL family.

features

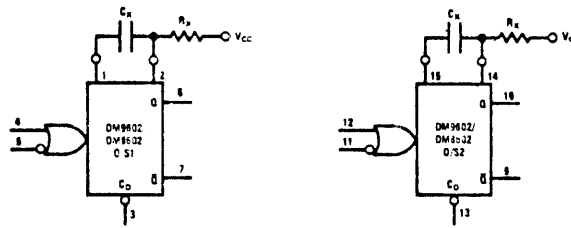
- 70 ns to  $\infty$  output width range
- Resettable and retriggerable 0% to 100% duty cycle
- TTL input gating—leading or trailing edge triggering
- Complementary TTL outputs
- Optional retrigger lock-out capability
- Pulse width compensated for  $V_{CC}$  and temperature variations



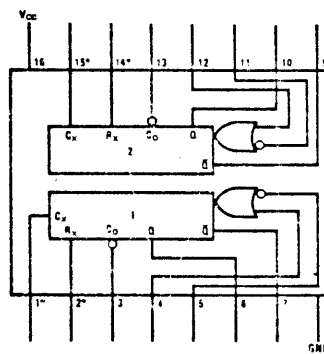
D COMPONENT DESCRIPTION  
 D.6 INTEGRATED CIRCUITS

9602 cont'd

logic and connection diagrams



Dual-In-Line and Flat Package



\*PINS FOR EXTERNAL TIMING.

absolute maximum ratings

Supply Voltage	7.0V
Input Voltage (Note 2)	5.5V
Output Voltage	5.5V
Storage Temperature Range	-65°C to +153°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V <sub>CC</sub> )			
DM9602	4.5	5.5	V
DM8602	4.75	5.25	V
Temperature (T <sub>A</sub> )			
DM9602	-55	+125	°C
DM8602	0	+70	°C

D COMPONENT DESCRIPTION  
D.6 INTEGRATED CIRCUITS

9602 cont'd

electrical characteristics (DM960?) ( $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$ )

PARAMETER	CONDITIONS (Note 3)	LIMITS									UNITS
		55 C			-25 C			+125 C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Output High Voltage ( $V_{OH}$ )	$V_{CC} = 4.5\text{V}$ , $I_{OH} = -0.80\text{mA}$ (Note 2)	2.4			2.4	3.3		2.4			V
Output Low Voltage ( $V_{OL}$ )	$V_{CC} = 4.5\text{V}$ , $I_{OL} = 16\text{mA}$ (Note 2)			0.4		0.2	0.4			0.4	V
Input High Voltage ( $V_{IH}$ )	Guaranteed Input High Threshold Voltage	2.0			1.7			1.5			V
Input Low Voltage ( $V_{IL}$ )	Guaranteed Input Low Threshold Voltage			0.85			0.90			0.95	V
Input Low Current ( $I_{IL}$ )	$V_{CC} = 5.5\text{V}$ , $V_{IN} = 0.4\text{V}$			-1.6		-1.1	-1.6			-1.6	mA
	$V_{CC} = 4.5\text{V}$ , $V_{IN} = 0.4\text{V}$			-1.24		-0.97	-1.24			-1.24	mA
Input High Current ( $I_{IH}$ )	$V_{CC} = 5.5\text{V}$ , $V_{IN} = 4.5\text{V}$					10	60			60	$\mu\text{A}$
Input Clamp Voltage ( $V_{CLAMP}$ )	$V_{CC} = 4.5\text{V}$ , $I_L = -12\text{mA}$						-1.5				V
Short Circuit Current ( $I_{SC}$ )	$V_{CC} = 5.5\text{V}$ , $V_{OUT} = 1.0\text{V}$ (Note 2)						-25				mA
Quiescent Power Supply Drain ( $I_{PD}$ )	$V_{CC} = 5.0\text{V}$			45		39	45			45	mA
Negative Trigger Input to True Output ( $t_{PLH}$ )	$V_{CC} = 5.0\text{V}$ , $R_X = 5.0\text{k}\Omega$ , $C_X = 0$ , $C_L = 15\text{pF}$					25	35				ns
Negative Trigger Input to Complement Output ( $t_{PHL}$ )	$V_{CC} = 5.0\text{V}$ , $R_X = 5.0\text{k}\Omega$ , $C_X = 0$ , $C_L = 15\text{pF}$					29	43				ns
Minimum True Output Pulse Width ( $t_{MIN}$ )	$V_{CC} = 5.0\text{V}$ , $R_X = 5.0\text{k}\Omega$ , $C_X = 0$ , $C_L = 15\text{pF}$					72	90				ns
Minimum Complement Output Pulse Width ( $t_{MIN}$ )	$V_{CC} = 5.0\text{V}$ , $R_X = 5.0\text{k}\Omega$ , $C_X = 0$ , $C_L = 15\text{pF}$					78	100				ns
Pulse Width (t)	$V_{CC} = 5.0\text{V}$ , $R_X = 10\text{k}\Omega$ , $C_X = 1000\text{pF}$				3.08	3.42	3.76				$\mu\text{s}$
Maximum Allowable Wiring Cap. (Pins 2 and 14) ( $C_{STRAY}$ )	Pins 2 and 14 to Ground			50			50			50	pF
Timing Resistor ( $R_X$ )		50		25	50		25	50		25	k $\Omega$

**Note 1:** The maximum  $V_{CC}$  value of 8.0V is not the primary factor in determining the maximum  $V_{CC}$  which may be applied to a number of interconnected devices. The voltage at a High output is approximately 1.0  $V_{BE}$  below the  $V_{CC}$  voltage, so the primary limit on the  $V_{CC}$  is that the voltage at any input may not go above 5.5V unless the current is limited. This effectively limits the system  $V_{CC}$  to approximately 7.0V.

**Note 2:** Because of the input clamp diodes, excess current can be drawn out of the inputs if the dc input voltage is more negative than -0.5V. The diode is designed to clamp off large negative ac swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.

**Note 3:** Unless otherwise noted, 10 k $\Omega$  resistor placed between Pin 2 (14) and  $V_{CC}$  for all tests. ( $R_X$ )

**Note 4:** Ground Pin 1 (15) for  $V_{OL}$  on Pin 7 (9), or for  $V_{OH}$  on Pin 6 (10), or for  $I_{SC}$  on Pins 6 (10); also, apply momentary ground to Pin 4 (12). Open Pin 1 (15) for  $V_{OL}$  on Pin 6 (10), or for  $V_{OH}$  on Pin 7 (9), or for  $I_{SC}$  on Pin 7 (9).

truth tables

TTL Input Load and Drive Factors

INPUTS	LOAD	
	HIGH	LOW
3, 4, 5, 11, 12, 13	1 U.L.	1 U.L.

OUTPUTS	DRIVE FACTOR	
	HIGH	LOW
6, 7, 9, 10	16 U.L.	8 U.L.

1 Unit Load (U.L.) = 60 $\mu\text{A}$  HIGH; 1.6 mA LOW

Triggering Truth Table

PIN NO.'S	OPERATION		
	5(11)	4(12)	3(13)
H-L	L	H	Trigger
H	L-H	H	Trigger
X	X	L	Reset

H = High Voltage Level  $\geq V_{IH}$   
L = Low Voltage Level  $\leq V_{IL}$   
X = Don't Care  
H-L = High to Low Voltage Level Transition  
L-H = Low to High Voltage Level Transition

2513

**DESCRIPTION**

The Signetics 2513 is a high speed 2560-bit Static ROM available in 64x7x5, and 64x8x5 versions. The product uses +5V, -5V and -12V power supplies, 5V TTL level input signals and Tri-State-Outputs for direct, low cost interfacing with TTL, DTL and 2500 Series MOS.

**FEATURES**

- 450 ns TYPICAL ACCESS TIME
- STATIC OPERATION
- TTL/DTL COMPATIBLE INPUTS
- +5, -5, -12V POWER SUPPLIES
- TRI-STATE OUTPUT CONTROLLED BY CHIP ENABLE FOR POWERFUL BUSSING CAPABILITY
- 2513/CM2140 ASCII FONT STANDARD (7 X 5)
- 24-PIN DIP
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

**APPLICATIONS**

RASTER SCAN CRT DISPLAYS (ROW OUTPUT)  
 PRINTER CHARACTER GENERATOR  
 PANEL DISPLAYS AND BILLBOARDS  
 MICRO PROGRAMMING  
 CODE CONVERSION

**PROCESS TECHNOLOGY**

The use of Signetics' unique Silicon Gate Low Threshold Process allows the design and production of higher functional density and operating speed than other techniques.

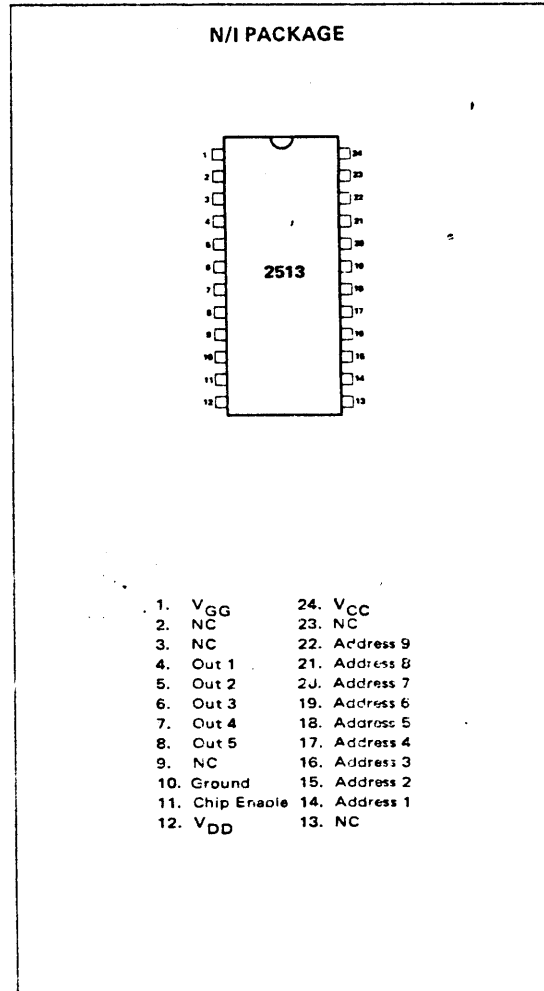
**SILICONE PACKAGING**

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process the silicon material over the gate oxide passivates the MOS transistors. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability, superior moisture resistance, and ionic contamination barriers. For further information reference Signetics - "Silicone Package Qualification Report".

**BIPOLAR COMPATIBILITY**

All inputs of the 2513 can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc). The data output buffers are capable of sinking a minimum of 1.6 mA, sufficient to drive one standard TTL load.

**PIN CONFIGURATION (Top View)**



- |                     |                     |
|---------------------|---------------------|
| 1. V <sub>GG</sub>  | 24. V <sub>CC</sub> |
| 2. NC               | 23. NC              |
| 3. NC               | 22. Address 9       |
| 4. Out 1            | 21. Address 8       |
| 5. Out 2            | 20. Address 7       |
| 6. Out 3            | 19. Address 6       |
| 7. Out 4            | 18. Address 5       |
| 8. Out 5            | 17. Address 4       |
| 9. NC               | 16. Address 3       |
| 10. Ground          | 15. Address 2       |
| 11. Chip Enable     | 14. Address 1       |
| 12. V <sub>DD</sub> | 13. NC              |

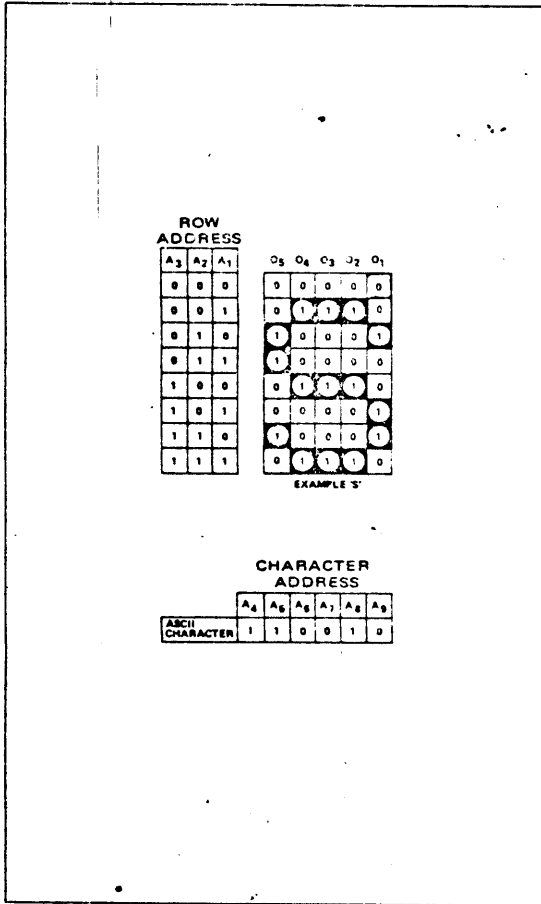
**PART IDENTIFICATION TABLE**

PART	ORGANIZATION	PROGRAMMING
2513N/I CM2140	64X8X5	ASCII Font
2513N/I CMXXXX	64X7X5 64X8X5	Custom*

\* Ask for "Signetics 2513/2514 Read Only Memory Software Package"

D COMPONENT DESCRIPTION  
D.7 CHARACTER GENERAL

2513 cont'd  
**CHARACTER FORMAT**



**MAXIMUM GUARANTEED RATINGS(1)**

Operating Ambient Temperature	0°C to 70°C
Storage Temperature	-65°C to +150°C
Package Power Dissipation(2) @T <sub>A</sub> 70°C	730mW
Input(3) and Supply Voltages with respect to V <sub>CC</sub>	+0.3 to -20V

**NOTES:**

- Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
- For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 110°C/W junction to ambient.
- All inputs are protected against static charge.
- Parameters are valid over operating temperature range unless specified.
- All voltage measurements are referenced to ground.
- Manufacturer reserves the right to make design and process changes and improvements.
- Typical values are at +25°C and nominal supply voltages.
- V<sub>CC</sub> tolerance is ±5%. Any variation in actual V<sub>CC</sub> will be tracked directly by V<sub>IL</sub>, V<sub>IH</sub> and V<sub>OH</sub> which are stated for a V<sub>CC</sub> of exactly 5 volts.

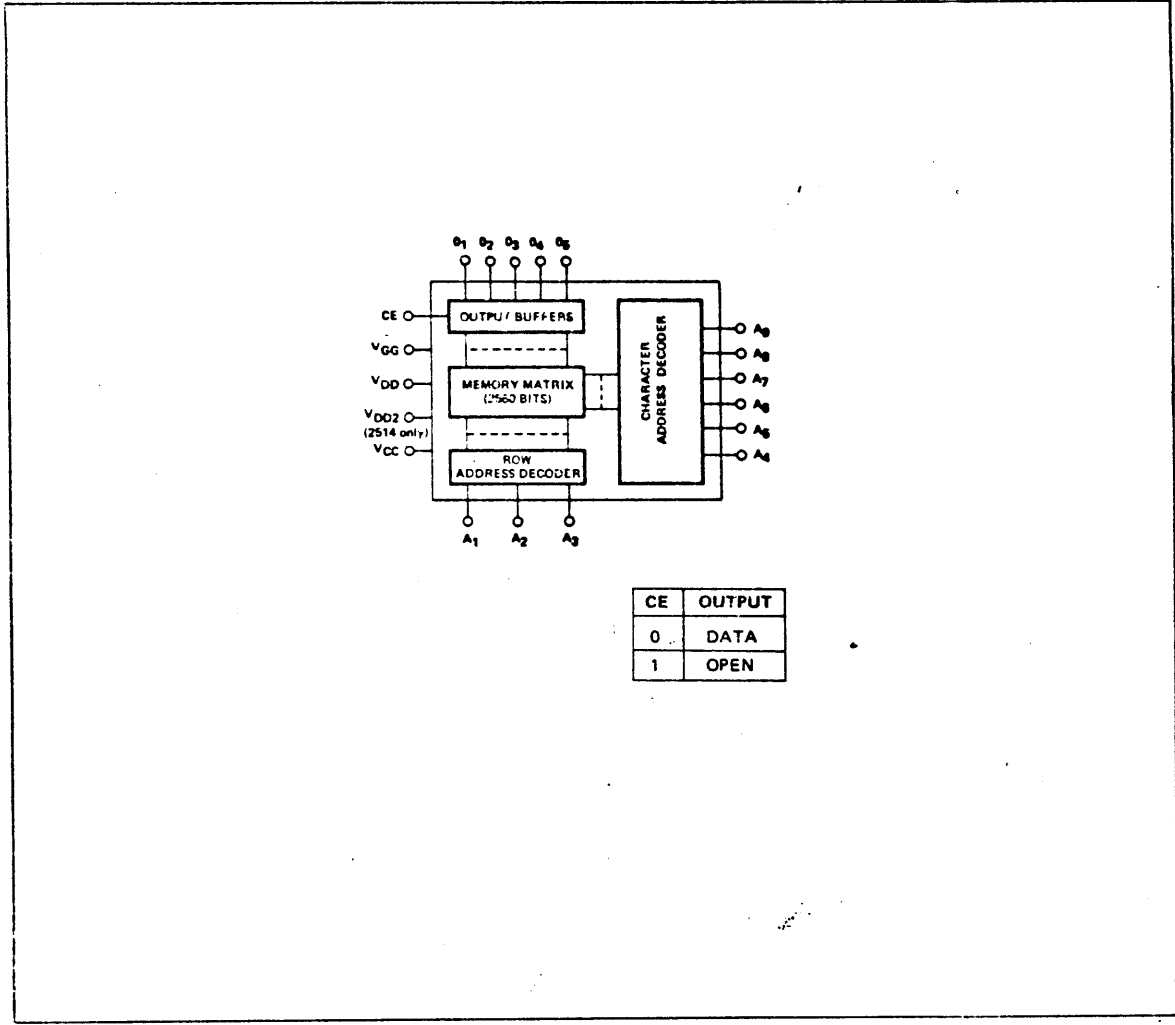
**DC CHARACTERISTICS**

T<sub>A</sub> = 0°C to +70°C; V<sub>CC</sub> = +5V (8); V<sub>DD</sub> = -5V; V<sub>GG</sub> = -12V ±5% unless otherwise noted. (Notes 4, 5, 6, 7)

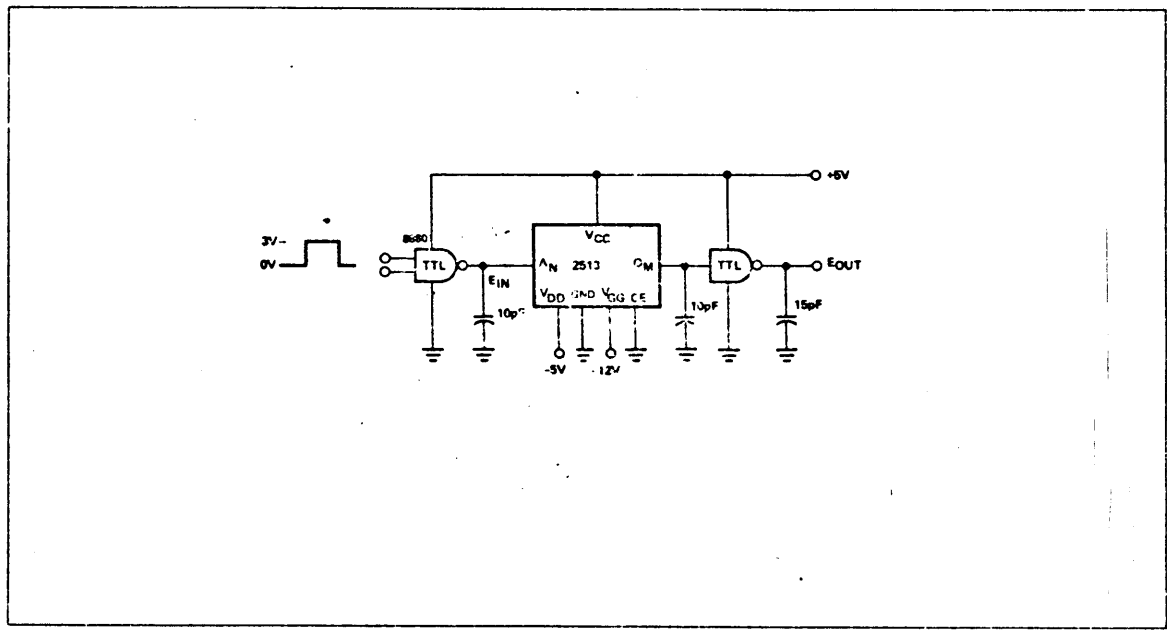
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I <sub>LI</sub>	Input Load Current		10	500	nA	V <sub>IN</sub> = -5.5V T <sub>A</sub> = 25°C
I <sub>LO</sub>	Output Leakage Current		10	1000	nA	V <sub>OUT</sub> = -5.5V T <sub>A</sub> = 25°C V <sub>CE</sub> = V <sub>CC</sub>
I <sub>DD</sub>	V <sub>DD</sub> Power Supply Current		12	15	mA	Outputs Open
I <sub>GG</sub>	V <sub>GG</sub> Power Supply Current		10	15	mA	Outputs Open V <sub>CE</sub> = V <sub>CC</sub>
V <sub>IL</sub>	Input Logic "0"			1.05	V	
V <sub>IH</sub>	Input Logic "1"	3.2		5.3	V	

D COMPONENT DESCRIPTION  
 D.7 CHARACTER GENERAL

2513 cont'd  
 BLOCK DIAGRAM



AC TEST SETUP

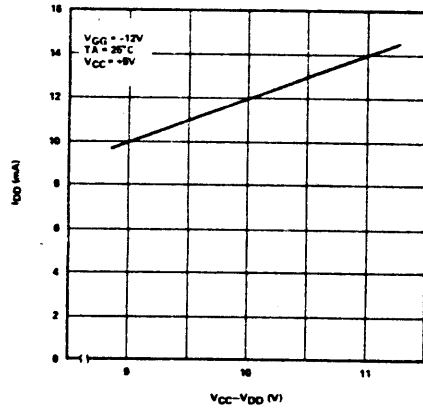


D COMPONENT DESCRIPTION  
 D.7 CHARACTER GENERAL

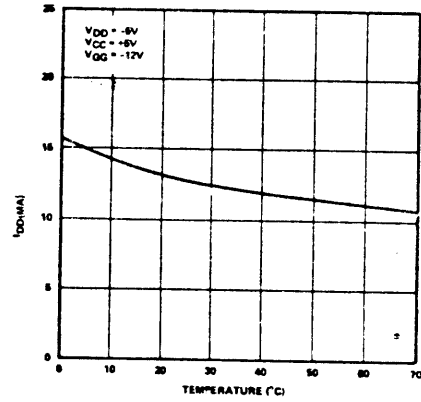
2513 cont'd

CHARACTERISTIC CURVES

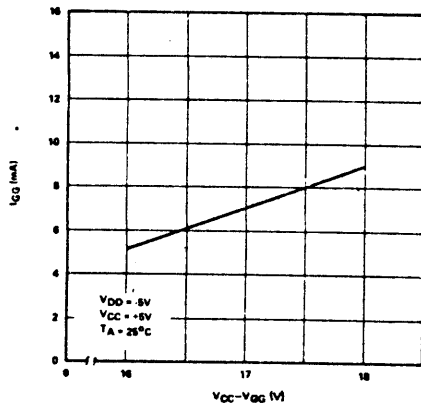
$V_{DD}$  POWER SUPPLY CURRENT  
 VERSUS VOLTAGE



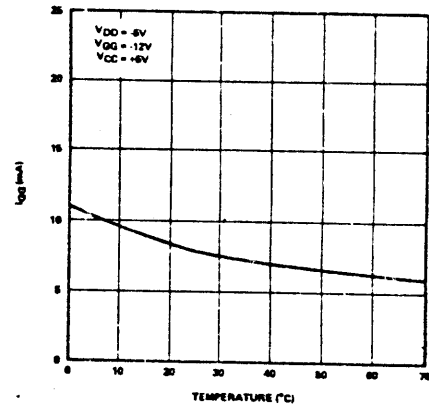
$V_{DD}$  POWER SUPPLY CURRENT  
 VERSUS TEMPERATURE



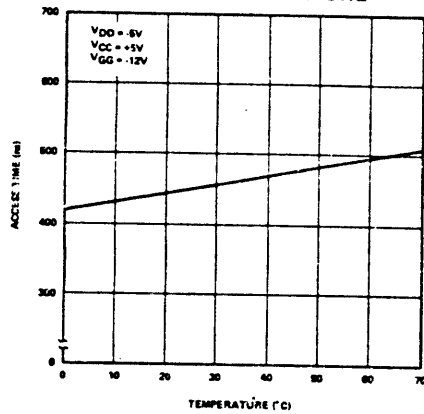
$V_{GG}$  POWER SUPPLY CURRENT  
 VERSUS VOLTAGE



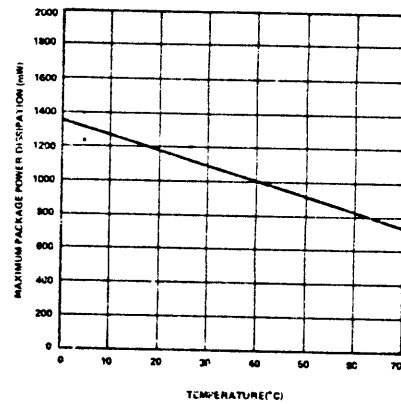
$V_{GG}$  POWER SUPPLY CURRENT  
 VERSUS TEMPERATURE



TYPICAL ACCESS TIME  
 VERSUS TEMPERATURE



MAXIMUM PACKAGE  
 POWER DISSIPATION



D COMPONENT DESCRIPTION  
 D.7 CHARACTER GENERAL

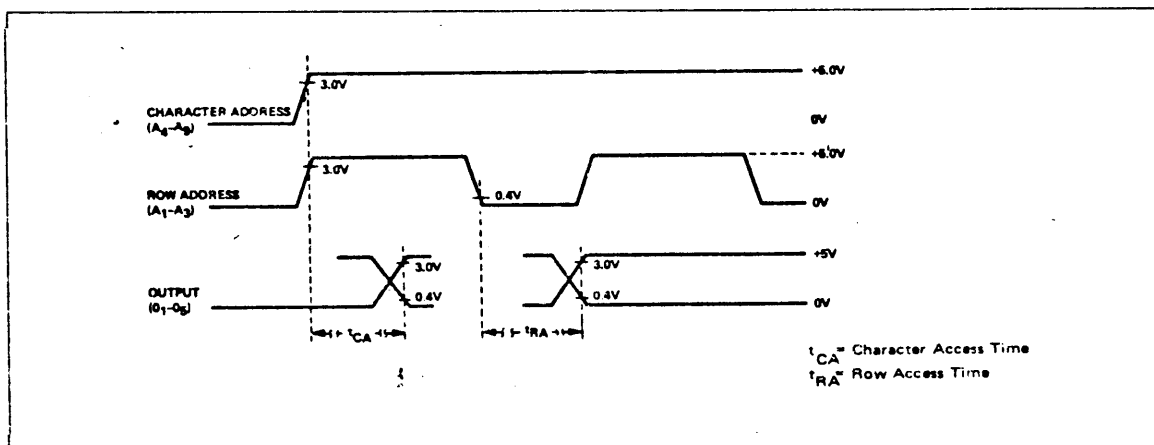
2513 cont'd

AC CHARACTERISTICS

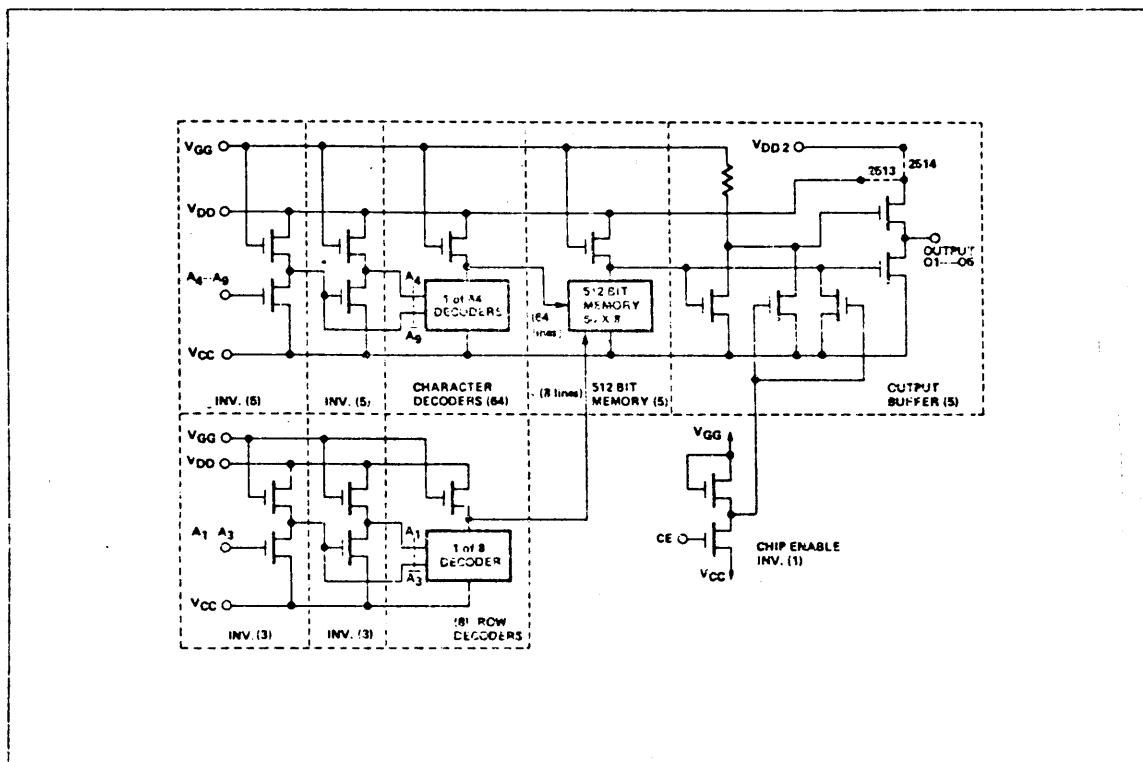
$T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ;  $V_{CC} = 5\text{V}$  (8);  $V_{DD} = -5\text{V} \pm 5\%$ ;  $V_{GG} = -12\text{V} \pm 5\%$ ; unless otherwise noted.

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
$V_{OL}$	Output Logic "Zero"	-5		0.4	V	One TTL Load
$V_{OH}$	Output Logic "One"	3.0			V	One TTL Load
$t_{CA}$ (CM2140)	Character Access Time		500	600	ns	See AC Test Setup
$t_{RA}$	Row Access Time ( $A_1 - A_3$ )		450	500	ns	See AC Test Setup
$t_{CE}$	Chip Enable to Output		150		ns	
$C_{IN}$	Address Input Capacitance			10	pF	$f = 1\text{ MHz}$ , $V_{IH} = V_{CC}$ , 25mV p-p

TIMING DIAGRAM (ADDRESS TIME)



CIRCUIT SCHEMATIC

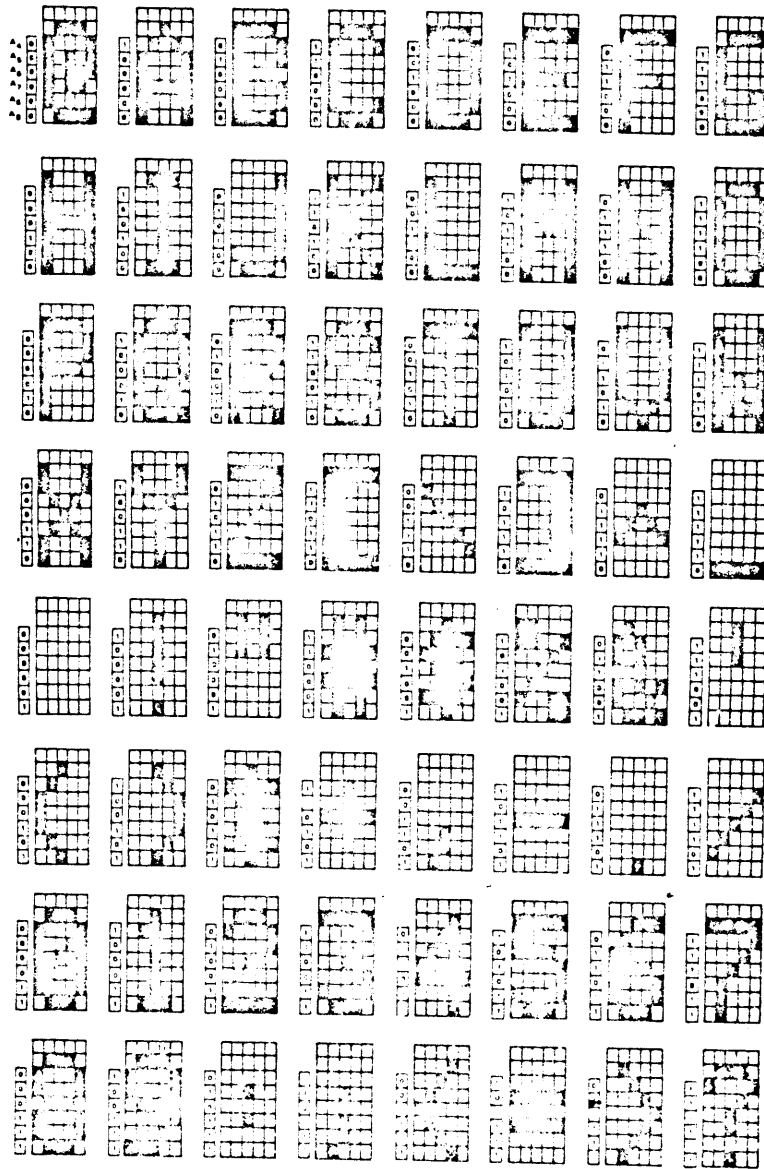


D COMPONENT DESCRIPTION  
D.7 CHARACTER GENERAL

2513 cont'd

ASCII CHARACTER FONT

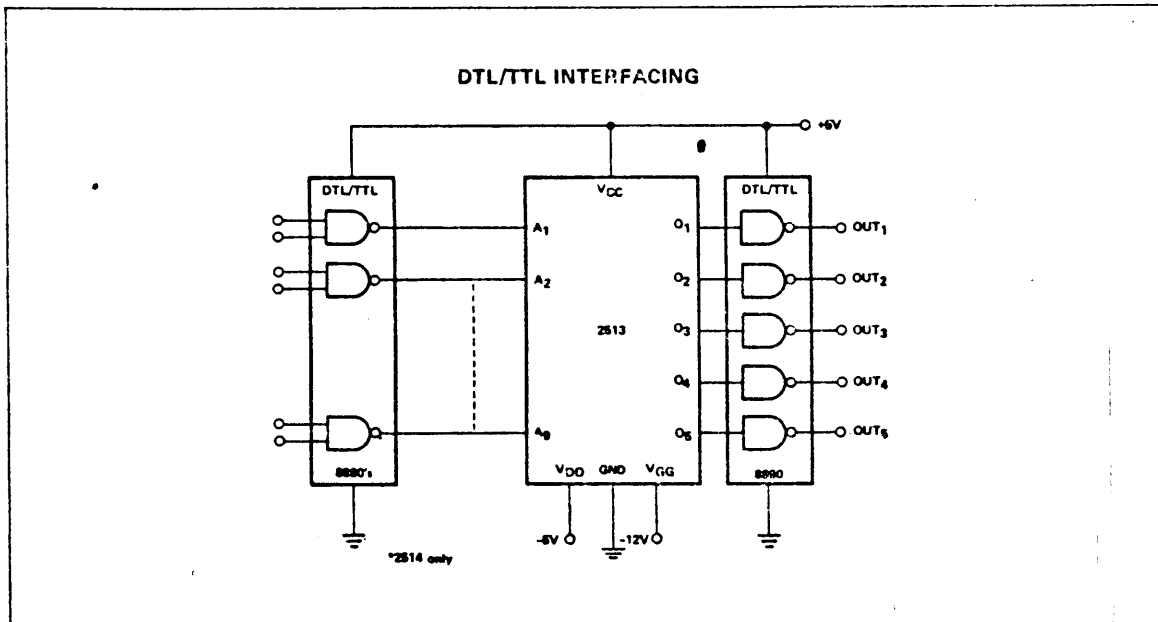
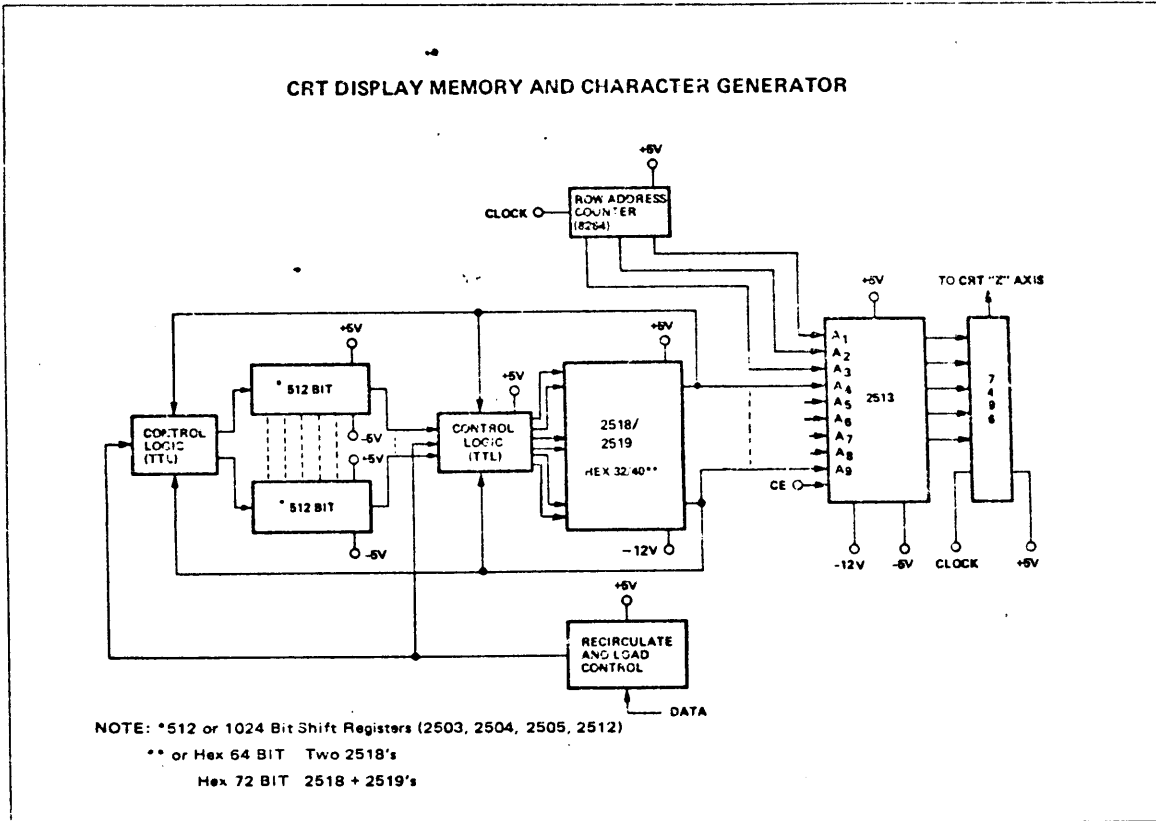
2513NX/CM2140





2513 cont'd

APPLICATIONS INFORMATION



D COMPONENT DESCRIPTIONS

D.7 CHARACTER GENERATOR

SCM 3088L 7435A 604-V10H-01

This Character Generator is a proprietary part, information and replacements are available only through Sphere Corp.

D COMPONENT DESCRIPTIONS  
D.8 MEMORIES

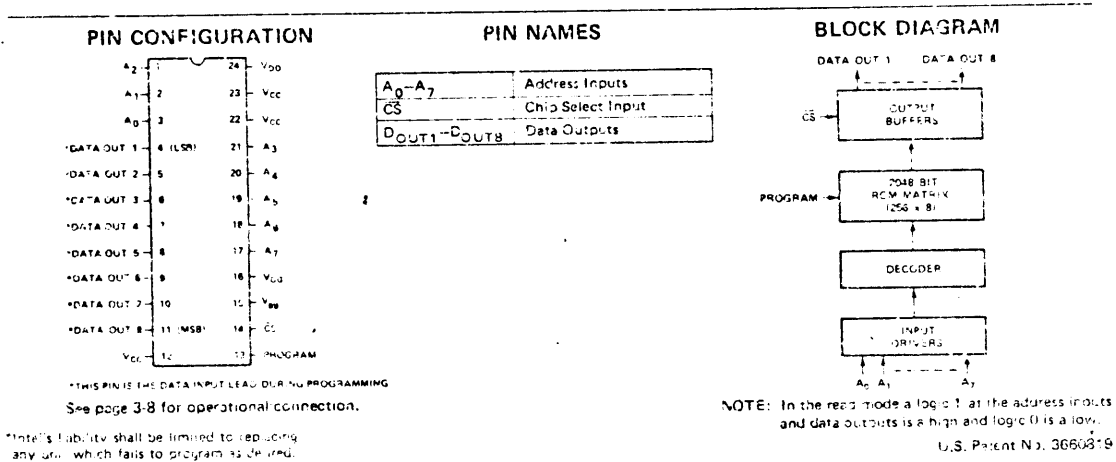
1702

The 1602A and 1702A are 256 word by 8-bit electrically programmable ROMs ideally suited for uses where fast turn-around and pattern experimentation are important. The 1602A and 1702A undergo complete programming and functional testing on each bit position prior to shipment, thus insuring 100% programmability. The 1602A and 1702A use identical chips. The 1702A is packaged in a 24 pin dual in-line package with a transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device. The 1602A is packaged in a 24 pin dual in-line package with a metal lid and is not erasable.

The circuitry of the 1602A/1702A is entirely static; no clocks are required.

A pin-for-pin metal mask programmed ROM, the Intel 1302, is ideal for large volume production runs of systems initially using the 1602A or 1702A.

The 1602A/1702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.



**PIN CONNECTIONS**

The external lead connections to the 1602A/1702A differ, depending on whether the device is being programmed or used in read mode. (See following table.) In the programming mode, the data inputs 1-8 are pins 4-11 respectively.

MODE	PIN	12 (V <sub>CC</sub> )	13 (Program)	14 (CS)	15 (V <sub>BB</sub> )	16 (V <sub>GG</sub> )	22 (V <sub>CC</sub> )	23 (V <sub>CC</sub> )
Read		V <sub>CC</sub>	V <sub>CC</sub>	GND	V <sub>CC</sub>	V <sub>GG</sub>	V <sub>CC</sub>	V <sub>CC</sub>
Programming		GND	Program Pulse	GND	V <sub>BB</sub>	Pulsed V <sub>GG</sub> (V <sub>IL4P</sub> )	GND	GND

**Absolute Maximum Ratings\***

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	-65°C to +125°C
Soldering Temperature of Leads (10 sec)	+300°C
Power Dissipation	2 Watts
Read Operation: Input Voltages and Supply	
Voltages with respect to V <sub>CC</sub>	-0.5V to +20V
Program Operation: Input Voltages and Supply	
Voltages with respect to V <sub>CC</sub>	-48V

**\*COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

D COMPONENT DESCRIPTIONS  
D.8 MEMORIES

1702 cont'd

READ OPERATION

D.C. and Operating Characteristics  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = +5V \pm 5\%$ ,  $V_{DD} = -9V \pm 5\%$ ,  $V_{GG}^{(1)} = -9V \pm 5\%$ , unless otherwise noted. Typical values are at nominal voltages and  $T_A = 25^\circ\text{C}$ .

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
$I_{LI}$	Address and Chip Select Input Load Current			1	$\mu\text{A}$	$V_{IN} = 0.0\text{V}$
$I_{LO}$	Output Leakage Current			1	$\mu\text{A}$	$V_{OUT} = 0.0\text{V}$ , $\overline{CS} = V_{CC} - 2$
$I_{DD0}$	Power Supply Current		5	10	mA	$V_{GG} = V_{CC}$ , $\overline{CS} = V_{CC} - 2$ , $I_{OL} = 0.0\text{mA}$ , $T_A = 25^\circ\text{C}$ } Note 1
$I_{DD1}$	Power Supply Current		35	50	mA	$\overline{CS} = V_{CC} - 2$ , $I_{OL} = 0.0\text{mA}$ , $T_A = 25^\circ\text{C}$
$I_{DD2}$	Power Supply Current		32	46	mA	$\overline{CS} = 0.0$ , $I_{OL} = 0.0\text{mA}$ , $T_A = 25^\circ\text{C}$
$I_{DD3}$	Power Supply Current		38.5	60	mA	$\overline{CS} = V_{CC} - 2$ , $I_{OL} = 0.0\text{mA}$ , $T_A = 0^\circ\text{C}$
$I_{CF1}$	Output Clamp Current		8	14	mA	$V_{OUT} = -1.0\text{V}$ , $T_A = 0^\circ\text{C}$
$I_{CF2}$	Output Clamp Current			13	mA	$V_{OUT} = -1.0\text{V}$ , $T_A = 25^\circ\text{C}$
$I_{GG}$	Gate Supply Current			1	$\mu\text{A}$	
$V_{IL1}$	Input Low Voltage for TTL Interface	-1.0		0.65	V	
$V_{IL2}$	Input Low Voltage for MOS Interface	$V_{DD}$		$V_{CC} - 6$	V	
$V_{IH}$	Address and Chip Select Input High Voltage	$V_{CC} - 2$		$V_{CC} + 0.5$	V	
$I_{OL}$	Output Sink Current	1.6	4		mA	$V_{OUT} = 0.45\text{V}$
$I_{OH}$	Output Source Current	-2.0			mA	$V_{OUT} = 0.0\text{V}$
$V_{OL}$	Output Low Voltage		0.7	0.45	V	$I_{OL} = 1.6\text{mA}$
$V_{OH}$	Output High Voltage	3.5	4.5		V	$I_{OH} = -100\mu\text{A}$

NOTE 1: POWER-DOWN OPTION:  $V_{GG}$  may be clocked to reduce power dissipation. The average  $I_{DD}$  will vary between  $I_{DD0}$  and  $I_{DD1}$  depending on the  $V_{GG}$  duty cycle (see typical characteristics). For this option please specify 1702AL or 1602AL.

A.C. Characteristics

$T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = +5V \pm 5\%$ ,  $V_{DD} = -9V \pm 5\%$ ,  $V_{GG} = -9V \pm 5\%$  unless otherwise noted

SYMBOL	TEST	MINIMUM	TYPICAL	MAXIMUM	UNIT
Freq.	Repetition Rate			1	MHz
$t_{OH}$	Previous read data valid			100	ns
$t_{ACC}$	Address to output delay		0.7	1	ns
$t_{DVGG}$	Clocked $V_{GG}$ set up (Note 1)	1			ns
$t_{CS}$	Chip select delay			100	ns
$t_{CO}$	Output delay from $\overline{CS}$			900	ns
$t_{OH}$	Output deselect			300	ns
$t_{OHG}$	Data out hold in clocked $V_{GG}$ mode (Note 1)			5	ns

Capacitance\*  $T_A = 25^\circ\text{C}$

SYMBOL	TEST	MINIMUM	TYPICAL	MAXIMUM	UNIT	CONDITIONS
$C_{IN}$	Input Capacitance		8	15	pF	$V_N = V_{CC}$ , All pins
$C_{OUT}$	Output Capacitance		10	15	pF	$\overline{CS} = V_{CC}$ , Input at A.C. ground
$C_{VGG}$	$V_{GG}$ Capacitance (Note 1)			30	pF	$V_{OUT} = V_{CC}$ , $V_{GG} = V_{CC}$ , Input at A.C. ground

\*This parameter is periodically sampled and is not 100% tested.

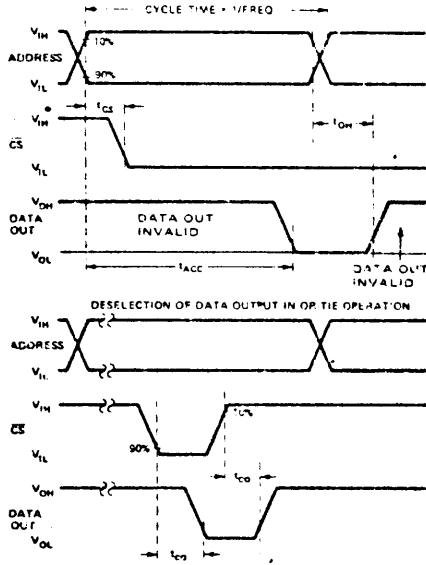
1702 cont'd

Switching Characteristics

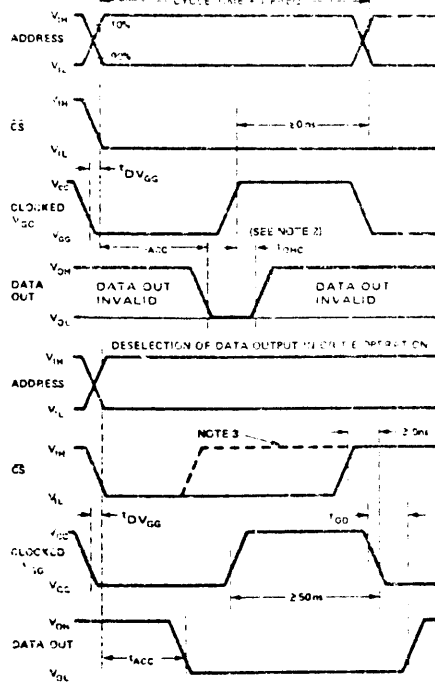
Conditions of Test:

Input pulse amplitudes: 0 to 4V,  $t_p, t_c \leq 50$  ns  
 Output load is 1 TTL gate; measurements made at output of TTL gate ( $t_{PD} \leq 15$  ns),  $C_L = 15$  pF

A) Constant  $V_{GG}$  Operation



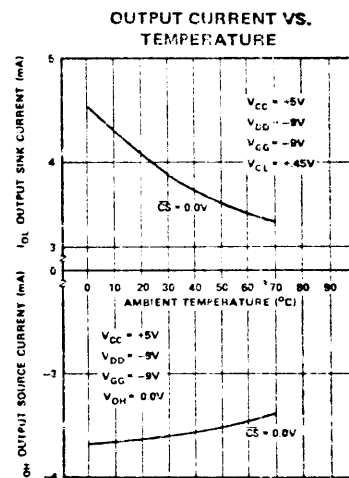
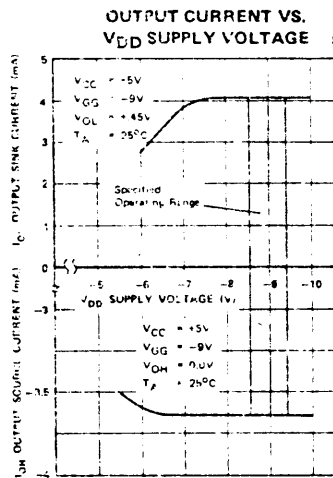
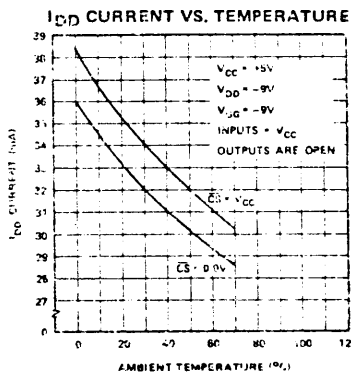
B) Power-Down Option (See Note 1)



NOTE 2: The output will remain valid for  $t_{OH}$  as long as clocked  $V_{GG}$  is at  $V_{CC}$ . An address change may occur as soon as the output is sensed (clocked  $V_{GG}$  may still be at  $V_{CC}$ ). Data becomes invalid on the old address when clocked  $V_{GG}$  is returned to  $V_{GG}$ .

NOTE 3: If  $\overline{CS}$  makes a transition from  $V_{IL}$  to  $V_{IH}$  while clocked  $V_{GG}$  is at  $V_{GG}$ , then deselection of output occurs at  $t_{CO}$  as shown in that operation with constant  $V_{GG}$ .

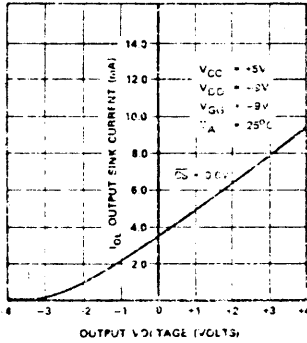
Typical Characteristics



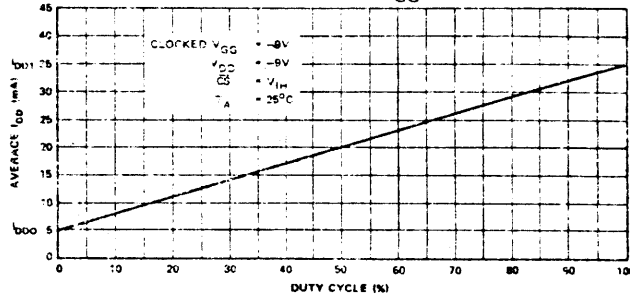
D COMPONENT DESCRIPTIONS  
 D.8 MEMORIES

1702 cont'd

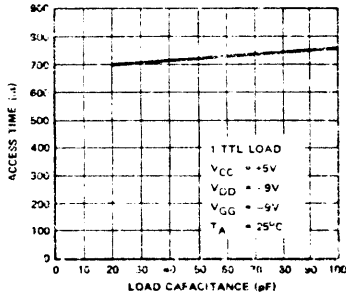
OUTPUT SINK CURRENT  
 VS. OUTPUT VOLTAGE



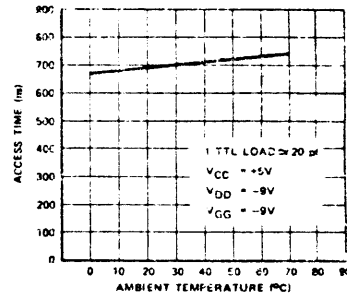
AVERAGE CURRENT VS. DUTY  
 CYCLE FOR CLOCKED V<sub>GG</sub> (Note 1)



ACCESS TIME VS.  
 LOAD CAPACITANCE



ACCESS TIME VS.  
 TEMPERATURE



PROGRAMMING OPERATION

D.C. and Operating Characteristics for Programming Operation

T<sub>A</sub> = 25°C, V<sub>CC</sub> = 0V, V<sub>BB</sub> = +12V ± 10%, C<sub>S</sub> = 0V unless otherwise noted

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I <sub>L1P</sub>	Address and Data Input Load Current			10	mA	V <sub>IN</sub> = -48V
I <sub>L2P</sub>	Program and V <sub>DD</sub> Load Current			10	mA	V <sub>IN</sub> = -48V
I <sub>9B</sub>	V <sub>9B</sub> Supply Load Current		10		mA	(Note 5)
I <sub>DDP</sub>	Peak I <sub>DD</sub> Supply Load Current		200		mA	V <sub>DD</sub> = V <sub>prog</sub> = -48V V <sub>GG</sub> = -35V (Note 4)
V <sub>IHP</sub>	Input High Voltage			0.3	V	
V <sub>L1P</sub>	Pulsed Data Input Low Voltage	-46		-48	V	
V <sub>L2P</sub>	Address Input Low Voltage	-40		-48	V	
V <sub>L3P</sub>	Pulsed Input Low V <sub>DD</sub> and Program Voltage	-46		-48	V	
V <sub>L4P</sub>	Pulsed Input Low V <sub>GG</sub> Voltage	-35		-40	V	

Note 4: I<sub>DDP</sub> flows only during V<sub>DD</sub>, V<sub>GG</sub> on time. I<sub>DDP</sub> should not be allowed to exceed 200mA for greater than 100µsec. Average power supply current I<sub>DDP</sub> is typically 40mA at 20% duty cycle.

Note 5: The V<sub>9B</sub> supply must be limited to 100mA max current to prevent damage to the device.

D COMPONENT DESCRIPTIONS  
 D.8 MEMORIES

1702 cont'd

**A.C. Characteristics for Programming Operation**

$T_{AMBIENT} = 25^{\circ}C$ ,  $V_{CC} = 0V$ ,  $V_{BB} = +12V \pm 10\%$ ,  $\overline{CS} = 0V$  unless otherwise noted

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
	Duty Cycle ( $V_{DD}$ , $V_{GG}$ )			20	%	
$t_{pW}$	Program Pulse Width			3	ms	$V_{GG} = -35V$ , $V_{DD} = V_{prog} = -48V$
$t_{DW}$	Data Set Up Time	25			$\mu s$	
$t_{DH}$	Data Hold Time	10			$\mu s$	
$t_{VW}$	$V_{DD}$ , $V_{GG}$ Set Up	100			$\mu s$	
$t_{VD}$	$V_{DD}$ , $V_{GG}$ Hold	10		100	$\mu s$	
$t_{ACW}^{(6)}$	Address Complement Set Up	25			$\mu s$	
$t_{ACH}^{(6)}$	Address Complement Hold	25			$\mu s$	
$t_{ATW}$	Address True Set Up	10			$\mu s$	
$t_{ATH}$	Address True Hold	10			$\mu s$	

Note 6: All 8 address bits must be in the complement state when pulsed  $V_{DD}$  and  $V_{GG}$  move to their negative levels. The addresses 10 through 255 must be programmed as shown in the timing diagram for a minimum of 32 times.

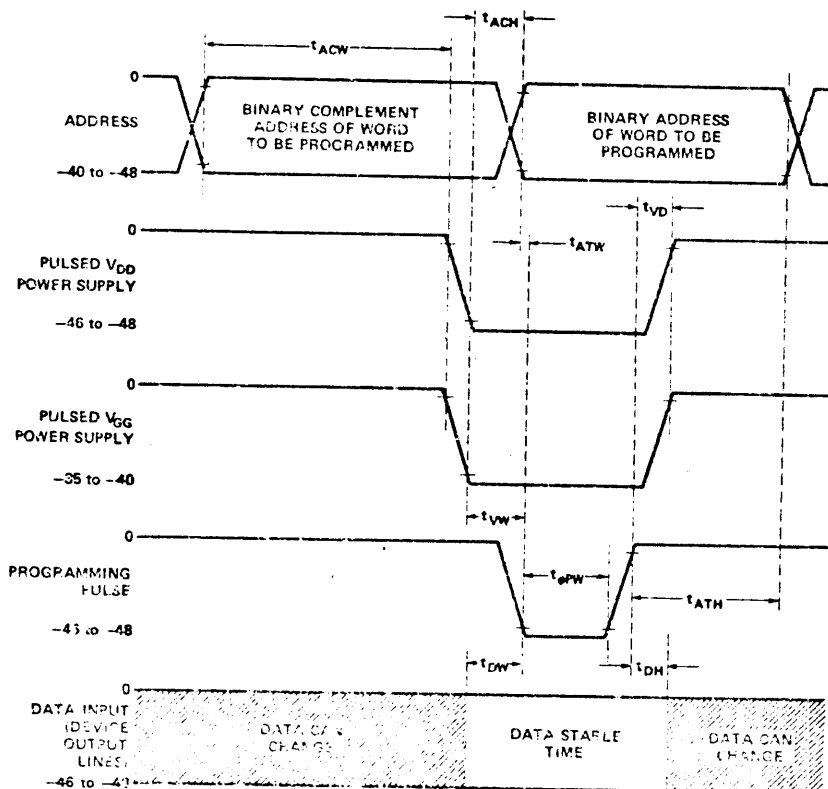
**Switching Characteristics for Programming Operation**

Conditions of Test:

input pulse rise and fall times  $\leq 1\mu sec$

$\overline{CS} = 0V$

**PROGRAM WAVEFORMS**



1702 cont'd

**OPERATION OF THE 1602A/1702A IN PROGRAM MODE**

Initially, all 2048 bits of the ROM are in the "0" state (output low). Information is introduced by selectively programming "1"s (output high) in the proper bit locations.

Word address selection is done by the same decoding circuitry used in the READ mode (see table on page 3-11 for logic levels). All 8 address bits must be in the binary complement state when pulled  $V_{DD}$  and  $V_{GG}$  move to their negative levels. The addresses must be held in their binary complement state for a minimum of 25 $\mu$ sec after  $V_{DD}$  and  $V_{GG}$  have moved to their negative levels. The addresses must then make the transition to their true state a minimum of 10 $\mu$ sec before the program pulse is applied. The addresses should be programmed in the sequence 0 through 255 for a minimum of 32 times. The eight output terminals are used as data inputs to determine the information pattern in the eight bits of each word. A low data input level (-4.8V) will program a "1" and a high data input level (ground) will leave a "0" (see table on page 3-11). All eight bits of one word are programmed simultaneously by setting the desired bit information patterns on the data input terminals.

During the programming,  $V_{GG}$ ,  $V_{DD}$  and the Program Pulse are pulsed signals.

**1702A ERASING PROCEDURE**

The 1702A may be erased by exposure to high intensity short-wave ultraviolet light at a wavelength of 2537 $\text{\AA}$ . The recommended integrated dose (i.e., UV intensity x exposure time) is 2W-sec/cm<sup>2</sup>. Examples of ultraviolet sources which can erase the 1702A in 10 to 20 minutes are the Model UVS 54 and Model S-52 short wave ultraviolet lamps manufactured by Ultra-Violet Products, Inc. (5114 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without short-wave filters, and the 1702A to be erased should be placed about one inch away from the lamp tubes.

2102

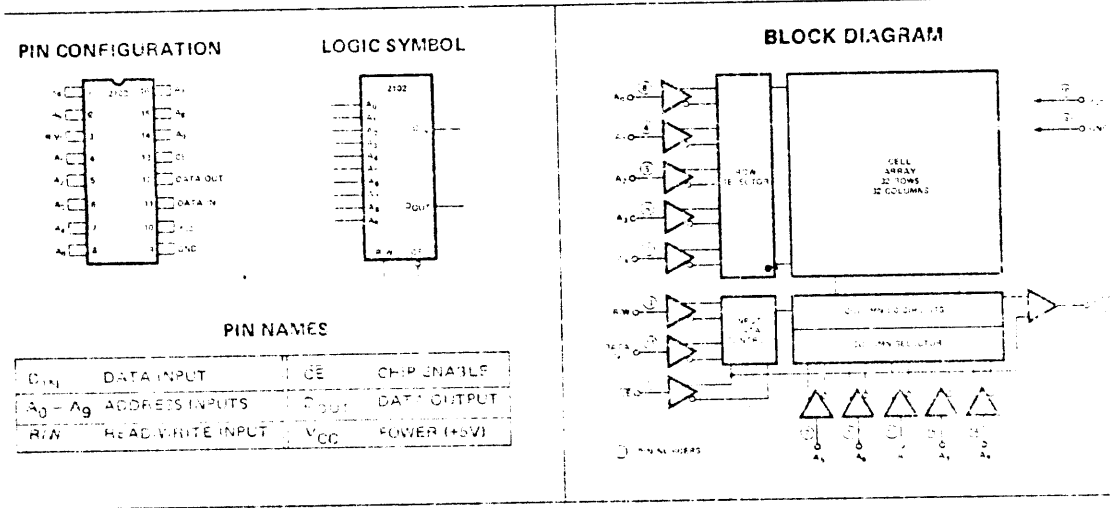
The Intel 2102 is a 1024 word by one bit static random access memory element using normally of N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

The 2102 is designed for memory applications where high performance, low cost, large bit storage and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, output, and a single +5 volt supply. A separate chip enable (CE) lead allows easy selection of an individual package when outputs are OR-tied.

The Intel 2102 is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance easy to use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost silicone packaging.





D COMPONENT DESCRIPTIONS  
D.8 MEMORIES

2102 cont'd

**Absolute Maximum Ratings\***

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
Voltage On Any Pin With Respect To Ground	-0.5V to +7V
Power Dissipation	1 Watt

**\*COMMENT:**

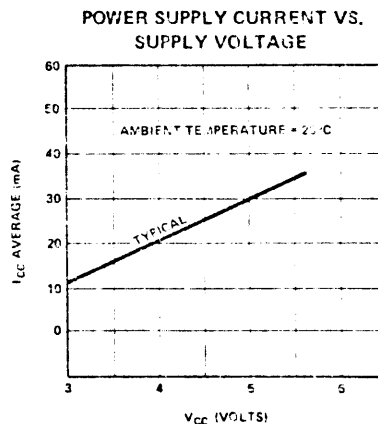
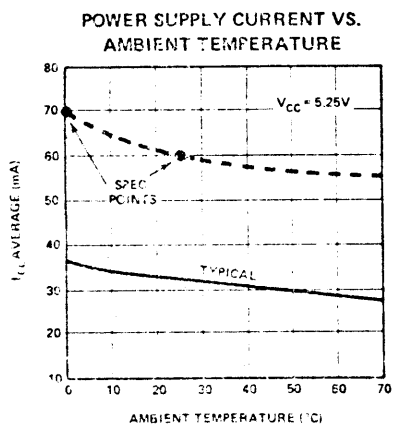
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**D. C. and Operating Characteristics**

T<sub>A</sub> = 0°C to +70°C, V<sub>CC</sub> = 5V ±5% unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP. <sup>(1)</sup>	MAX.		
I <sub>LI</sub>	INPUT LOAD CURRENT (ALL INPUT PINS)			10	μA	V <sub>IN</sub> = 0 to 5.25V
I <sub>LOH</sub>	OUTPUT LEAKAGE CURRENT			10	μA	C <sub>E</sub> = 2.2V, V <sub>OUT</sub> = 4.0V
I <sub>LOL</sub>	OUTPUT LEAKAGE CURRENT			-100	μA	C <sub>E</sub> = 2.2V, V <sub>OUT</sub> = 0.45V
I <sub>CC1</sub>	POWER SUPPLY CURRENT		30	60	mA	ALL INPUTS = 5.25V DATA OUT OPEN T <sub>A</sub> = 25°C
I <sub>CC2</sub>	POWER SUPPLY CURRENT			70	mA	ALL INPUTS = 5.25V DATA OUT OPEN T <sub>A</sub> = 0°C
V <sub>IL</sub>	INPUT "LOW" VOLTAGE	-0.5		+0.65	V	
V <sub>IH</sub>	INPUT "HIGH" VOLTAGE	2.2		V <sub>CC</sub>	V	
V <sub>OL</sub>	OUTPUT "LOW" VOLTAGE			+0.45	V	I <sub>OL</sub> = 1.9mA
V <sub>OH</sub>	OUTPUT "HIGH" VOLTAGE	2.2			V	I <sub>OH</sub> = -100μA

**Typical D.C. Characteristics**



NOTE: 1. Typical values are for T<sub>A</sub> = 25°C and nominal supply voltage.

**A. C. CONDITIONS OF TEST**

Input Pulse Levels:	-0.65 Volt to 2.2 Volt
Input Pulse Rise and Fall Times:	20nsec
Timing Measurement Reference Level:	1.5 Volt
Output Load:	1 TTL Gate and C <sub>L</sub> = 100 pF

**Capacitance<sup>(2)</sup> T<sub>A</sub> = 25°C, f = 1MHz**

SYMBOL	TEST	LIMITS (pF)	
		TYP. <sup>(1)</sup>	MAX.
C <sub>IN</sub>	INPUT CAPACITANCE (ALL INPUT PINS) V <sub>IN</sub> = 0V	3	5
C <sub>OUT</sub>	OUTPUT CAPACITANCE V <sub>OUT</sub> = 0V	7	10

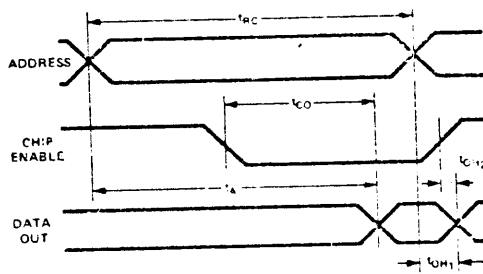
2102 cont'd

**A. C. Characteristics**  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5V \pm 5\%$  unless otherwise specified

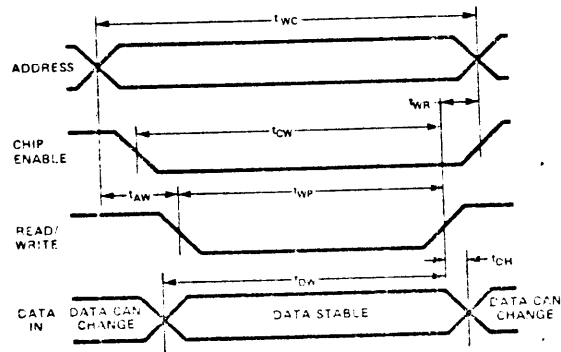
SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP. (1)	MAX.	
<b>READ CYCLE</b>					
$t_{RC}$	READ CYCLE	1000			ns
$t_A$	ACCESS TIME		500	1000	ns
$t_{CO}$	CHIP ENABLE TO OUTPUT TIME			500	ns
$t_{OH1}$	PREVIOUS READ DATA VALID WITH RESPECT TO ADDRESS	50			ns
$t_{OH2}$	PREVIOUS READ DATA VALID WITH RESPECT TO CHIP ENABLE	0			ns
<b>WRITE CYCLE</b>					
$t_{WC}$	WRITE CYCLE	1000			ns
$t_{AW}$	ADDRESS TO WRITE SETUP TIME	200			ns
$t_{WP}$	WRITE PULSE WIDTH	750			ns
$t_{WR}$	WRITE RECOVERY TIME	50			ns
$t_{DW}$	DATA SETUP TIME	800			ns
$t_{DH}$	DATA HOLD TIME	100			ns
$t_{CW}$	CHIP ENABLE TO WRITE SETUP TIME	900			ns

**Waveforms**

**READ CYCLE**

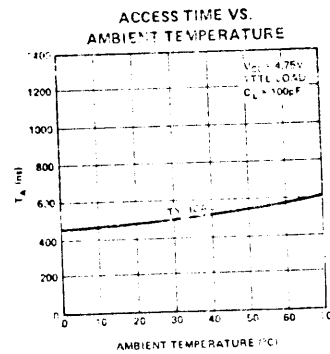
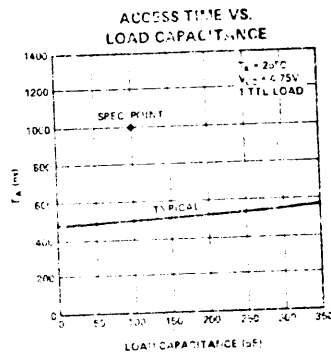


**WRITE CYCLE**



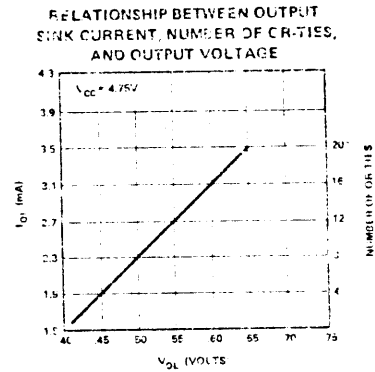
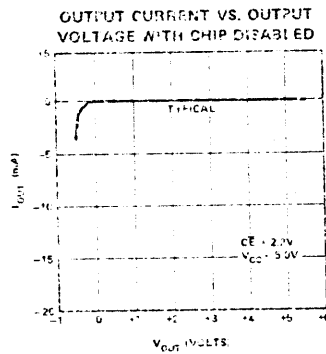
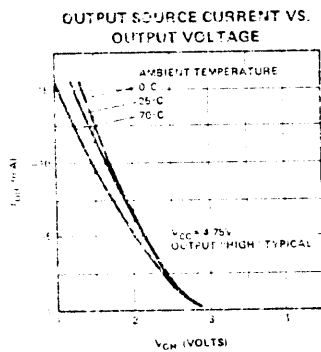
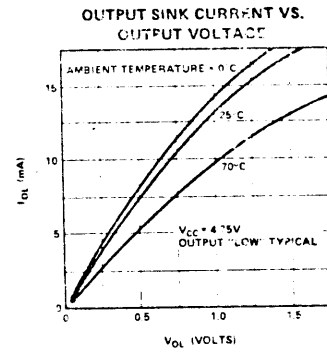
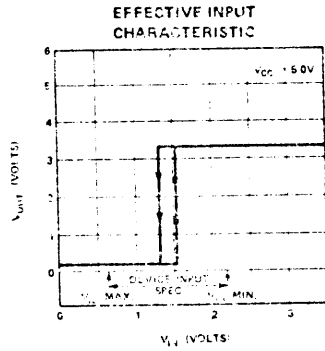
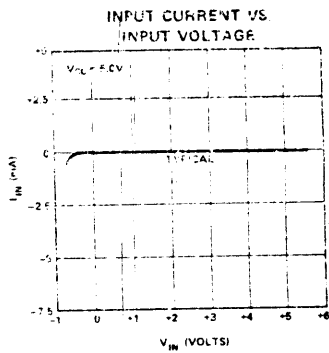
- NOTES: 1. Typical values are for  $T_A = 25^\circ\text{C}$  and nominal supply voltage.  
 2. This parameter is periodically sampled and is not 100% tested.

**Typical A. C. Characteristics**



2102 cont'd

Typical D. C. Characteristics



2107 A Type Dynamic RAM

4030  $V_{BB} = -3v$

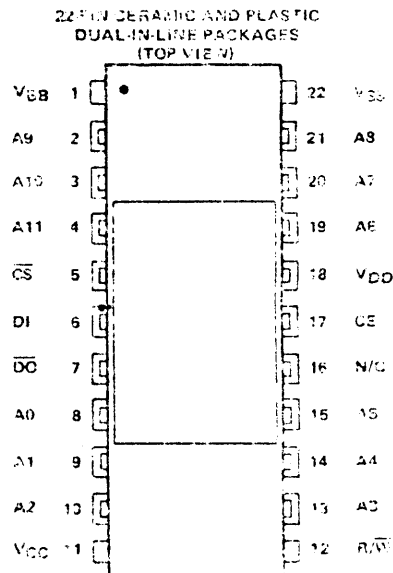
4060  $V_{BB} = -5v$

Do not mix different voltage chips on a single board. Boards containing different types of chips may be mixed in a system.

- 4096 x 1 Organization
- 3 Performance Ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY WRITE CYCLE (MIN)
TMS 4060	300 ns	470 ns	710 ns
TMS 4060-1	250 ns	430 ns	640 ns
TMS 4060-2	300 ns	430 ns	580 ns

- Full TTL Compatibility on All Inputs (No Pull-up Resistors Needed)
- Low Power Dissipation
  - 400 mW Operating (Typical)
  - 0.2 mW Standby (Typical)
- Single Low-Capacitance Clock
- N-Channel Silicon-Gate Technology
- 22-Pin 400-Mil Dual-In-Line Package



2107A cont'd

Description

The TMS 4060 series is composed of integrated dynamic 4096-bit CMOS random-access memories, organized as 4096 one-bit words. Advanced subcircuit technology is employed to optimize the speed/power density trade-off. Three performance options are offered: 300 ns access for the TMS 4060, 250 ns access for the TMS 4060-1, and 200 ns for TMS 4060-2. These options allow the system designer to more closely match the memory performance to the capability of the arithmetic processor.

All inputs except the chip enable are fully TTL compatible and require no pull-up resistors. The low capacitance of the address and control inputs precludes the need for specialized drivers. When driven by a Series 74 device, the guaranteed dc input noise immunity is 200 mV. The TTL-compatible buffer is guaranteed to drive two Series 74 TTL gates. The TMS 4060 series uses only one clock (chip enable) to simplify system design. The low-capacitance chip enable input requires a positive voltage swing (12 volts), which can be driven by a variety of widely available drivers.

The typical power dissipation of these RAMs is 400 mW active and 0.3 mW standby. To retain data only 6 mW average power is required, which includes the power consumed to refresh the contents of the memory.

The TMS 4060 series is offered in both 22-pin ceramic (JL suffix) and plastic (NL suffix) dual-in-line packages. The series is guaranteed for operation from 0°C to 70°C. These packages are designed for insertion in mounting hole rows on 0.400-mil centers.

Operation

chip select ( $\overline{CS}$ )

The chip-select terminal, which can be driven from standard TTL circuits without an external pull-up resistor, affects the data-in, data-out and read/write inputs. The data input and data output terminals are enabled when chip select is low. Therefore, the read, write, and read, modify write operations are performed only when chip select is low. If the chip is to be selected for a given cycle, the chip-select input must be low on or before the rising edge of the chip enable. If the chip is not to be selected for a given cycle, chip select must be held high as long as chip enable is high. A register for the chip-select input is provided on the chip to reduce overhead and simplify system design.

chip enable (CE)

A single external clock input is required. All read, write, and read, modify write operations take place when the chip enable input is high. When the chip enable is low, the memory is in the low-power standby mode. No read/write operations can take place because the chip is automatically precharging.

mode select ( $\overline{R/\overline{W}}$ )

The read or write mode is selected through the read/write ( $\overline{R/\overline{W}}$ ) input. A logic high on the  $\overline{R/\overline{W}}$  input selects the read mode and a logic low selects the write mode. The read/write terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected.

address (A0-A11)

All addresses must be stable on or before the rising edge of the chip-enable pulse. All address inputs can be driven from standard TTL circuits without pull-up resistors. Address registers are provided on chip to reduce overhead and simplify system design.

data-in (DI)

Data is written during a write or read, modify write cycle while the chip enable is high. The data-in terminal can be driven from standard TTL circuits without a pull-up resistor. There is no register on the data-in terminal.

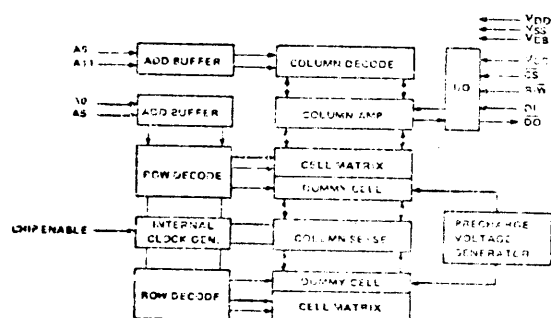
data-out ( $\overline{DO}$ )

The three-state output buffer provides direct TTL compatibility with a fan-out of two Series 74 TTL gates. The output is in the high-impedance (floating) state when the chip enable is low. It remains in the high-impedance state if the chip-select input is high when chip enable goes high and provided that chip select remains high as long as chip enable is high. If the chip select is set up low prior to the rise of chip enable and held low an interval after that rise, the output will be enabled as long as chip enable stays high regardless of subsequent changes in the level of chip select. A data valid mode is always preceded by a low output state. Data-out is inverted from data-in.

refresh

Refresh must be performed every two milliseconds by cycling through the 64 addresses of the lower-order-address inputs A0 through A5 (pins 8, 9, 10, 13, 14, 15), or by addressing every row within any 2-millisecond period. Addressing any row refreshes all 64 bits in that row. The chip does not need to be selected during the refresh. If the chip is refreshed during a write mode, then chip select must be high. The column addresses (A6 through A11) can be indeterminate during refresh.

functional block diagram



D COMPONENT DESCRIPTIONS  
D.8 MEMORIES

2107A cont'd

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note)	-0.3 to 20 V
Supply voltage, $V_{DD}$ (see Note)	-0.3 to 20 V
Supply voltage, $V_{SS}$ (see Note)	-0.3 to 20 V
All input voltages (see Note)	-0.3 to 20 V
Chip-enable voltage (see Note)	-0.3 to 20 V
Output voltage (operating with respect to $V_{SS}$ )	-2 to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-55°C to 150°C

NOTE: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage,  $V_{BB}$  (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to  $V_{SS}$ .

recommended operating conditions (see Note)

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$	4.75	5	5.25	V
Supply voltage, $V_{DD}$	11.4	12	12.6	V
Supply voltage, $V_{SS}$		0		V
Supply voltage, $V_{BB}$	-4.5	-5	-5.5	V
High-level input voltage, $V_{IH}$ (all inputs except chip enable)	2.2		5.25	V
High-level chip enable input voltage, $V_{IH}(CE)$	$V_{DD} - 0.6$		$V_{DD} + 1.0$	V
Low-level input voltage, $V_{IL}$ (all inputs except chip enable) (see Note)	-0.6		0.5	V
Low-level chip enable input voltage, $V_{IL}(CE)$ (see Note)	-1		0.5	V
Refresh time, $t_{refresh}$			2	ns
Operating free-air temperature, $T_A$	0		70	°C

NOTE: The algebraic convention where the most-negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYPI	MAX	UNIT
$V_{OH}$	High-level output voltage $I_O = -2\text{ mA}$	2.4		$V_{DD}$	V
$V_{OL}$	Low-level output voltage $I_O = 5.2\text{ mA}$	$V_{SS}$		0.4	V
$I_I$	Input current (all inputs except chip enable) $V_I = 0$ to 5.25 V			10	$\mu\text{A}$
$I_{I(CE)}$	Chip-enable input current $V_I = 0$ to 13.2 V			2	$\mu\text{A}$
$I_{OZ}$	High-impedance-state (off state) output current $V_O = 0$ to 5.25 V			10	$\mu\text{A}$
$I_{CC}$	Supply current from $V_{CC}$ 2 Series 74 TTL loads			1	mA
$I_{DD}$	Supply current from $V_{DD}$ $V_{I(CE)} = 12.6\text{ V}$		30	60	mA
$I_{SD}$	Supply current from $V_{DD}$ , standby $I_{I(CE)} = 0.6\text{ V}$		20	200	$\mu\text{A}$
$I_{DD(av)}$	Average supply current from $V_{DD}$ during read or write cycle	Minimum cycle time	TMS 4060	32	mA
			TMS 4060-1	35	
			TMS 4060-2	33	
			TMS 4060	32	
			TMS 4060-1	35	
$I_{DD(av)}$	Average supply current from $V_{DD}$ during read, modify write cycle		TMS 4060-2	38	mA
$I_{BB}$	Supply current from $V_{BB}$ $V_{BB} = -0.5\text{ V}$ , $V_{DD} = 12.6\text{ V}$ , $V_{CC} = 5.25\text{ V}$ , $V_{SS} = 0\text{ V}$		-5	-100	$\mu\text{A}$

\* All typical values are at  $T_A = 25^\circ\text{C}$ .

capacitance at  $V_{DD} = 12\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $V_{BB} = -5\text{ V}$ ,  $V_{CC} = 5\text{ V}$ ,  $V_{I(CE)} = 0\text{ V}$ ,  $V_I = 0\text{ V}$ ,  $f = 1\text{ MHz}$ ,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYPI	MAX	UNIT
$C_{in(ad)}$	Input capacitance address inputs		5	7	pF
$C_{I(CE)}$	Input capacitance clock input $V_{I(CE)} = 10.3\text{ V}$		18	22	pF
$C_{I(ES)}$	Input capacitance chip-select input $V_I(ES) = -1.0\text{ V}$		23	27	pF
$C_{in(data)}$	Input capacitance data input		4	6	pF
$C_{in(W)}$	Input capacitance write enable input		5	7	pF
$C_{in}$	Input capacitance		5	7	pF

\* All typical values are at  $T_A = 25^\circ\text{C}$ .

\* 4030  $V_{BB} = 2.7, -3, -3.3$

D COMPONENT DESCRIPTIONS

D.8 MEMORIES

2107 A cont'd

read cycle timing requirements over recommended supply voltage range,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$

PARAMETER	TMS 4060		TMS 4060-1		TMS 4060-2		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{rd}$ Read cycle time	470		430		400		ns
$t_w(\text{CEH})$ Pulse width, chip enable high	300	4000	260	4000	230	4000	ns
$t_w(\text{CEL})$ Pulse width, chip enable low	130		130		130		ns
$t_r(\text{CE})$ Chip-enable rise time		40		40		40	ns
$t_f(\text{CE})$ Chip-enable fall time		40		40		40	ns
$t_{su}(\text{A})$ Address setup time	0 $\uparrow$		0 $\uparrow$		0 $\uparrow$		ns
$t_{su}(\text{CS})$ Chip select setup time	0 $\uparrow$		0 $\uparrow$		0 $\uparrow$		ns
$t_{su}(\text{D})$ Data setup time	0 $\uparrow$		0 $\uparrow$		0 $\uparrow$		ns
$t_h(\text{A})$ Address hold time	150 $\downarrow$		150 $\downarrow$		150 $\downarrow$		ns
$t_h(\text{CS})$ Chip select hold time	150 $\downarrow$		150 $\downarrow$		150 $\downarrow$		ns
$t_h(\text{D})$ Data hold time	40 $\downarrow$		40 $\downarrow$		40 $\downarrow$		ns

$\uparrow$  The arrow indicates the edge of the chip enable pulse used for reference:  $\uparrow$  for the rising edge,  $\downarrow$  for the falling edge.

read cycle switching characteristics over recommended supply voltage range,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$

PARAMETER	TMS 4060		TMS 4060-1		TMS 4060-2		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a}(\text{CE})$ Access time from chip enable $\uparrow$		280		270		190	ns
$t_{a}(\text{A})$ Access time from address $\uparrow$		300		250		200	ns
$t_{PDZ}$ or $t_{PZL}$ Output disable time from high or low level $\uparrow$	30		30		30		ns
$t_{PZL}$ Output enable time to low level $\downarrow$		250		200		150	ns

$\uparrow$  Test conditions:  $C_L = 50$  pF,  $t_r(\text{CE}) = 20$  ns, Load = 1 Series 74 TTL gate.

$\downarrow$  Test conditions:  $C_L = 50$  pF, Load = 1 Series 74 TTL gate.

write cycle timing requirements over recommended supply voltage range,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$

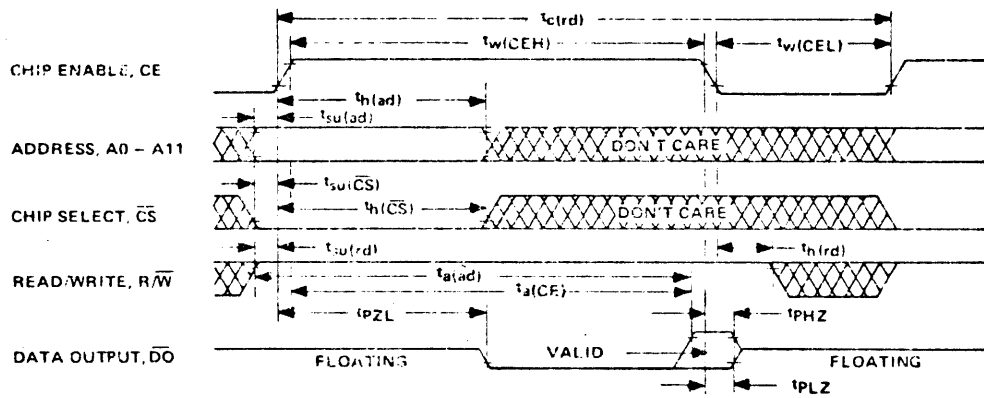
PARAMETER	TMS 4060		TMS 4060-1		TMS 4060-2		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{o}(\text{wr})$ Write cycle time	470		430		400		ns
$t_w(\text{CEH})$ Pulse width, chip enable high	300	4000	260	4000	230	4000	ns
$t_w(\text{CEL})$ Pulse width, chip enable low	130		130		130		ns
$t_w(\text{D})$ Write pulse width	200		190		180		ns
$t_r(\text{CE})$ Chip-enable rise time		40		40		40	ns
$t_f(\text{CE})$ Chip-enable fall time		40		40		40	ns
$t_{su}(\text{A})$ Address setup time	0 $\uparrow$		0 $\uparrow$		0 $\uparrow$		ns
$t_{su}(\text{CS})$ Chip select setup time	0 $\uparrow$		0 $\uparrow$		0 $\uparrow$		ns
$t_{su}(\text{D} \rightarrow \text{wr})$ Data-to-write setup time*	0		0		0		ns
$t_{su}(\text{wr})$ Write-pulse setup time	240 $\downarrow$		220 $\downarrow$		210 $\downarrow$		ns
$t_h(\text{A})$ Address hold time	150 $\downarrow$		150 $\downarrow$		150 $\downarrow$		ns
$t_h(\text{CS})$ Chip select hold time	150 $\downarrow$		150 $\downarrow$		150 $\downarrow$		ns
$t_h(\text{D})$ Data hold time	40 $\downarrow$		40 $\downarrow$		40 $\downarrow$		ns

$\uparrow$  The arrow indicates the edge of the chip enable pulse used for reference:  $\uparrow$  for the rising edge,  $\downarrow$  for the falling edge.

\* If  $\overline{\text{R}}/\overline{\text{W}}$  is low before CE goes high then DI must be valid when CE goes high.

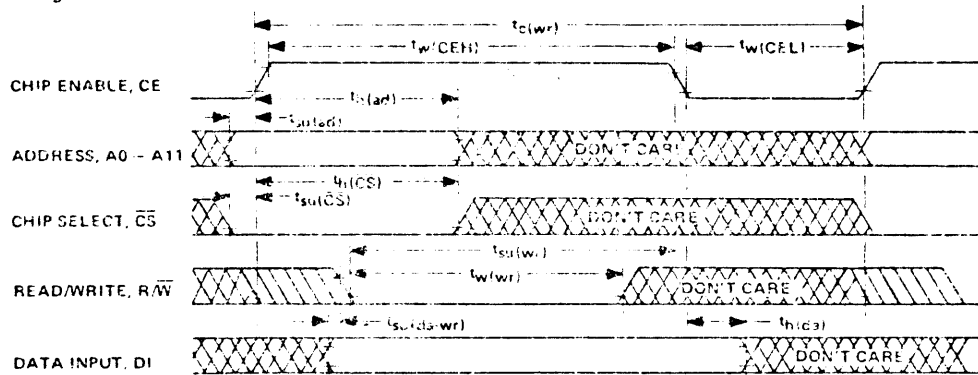
2107 A cont'd

read cycle timing



NOTE: For the chip enable input, high and low timing points are 90% and 10% of  $V_{IH}(CE)$ . Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).

write cycle timing



NOTE: For the chip-enable input, high and low timing points are 90% and 10% of  $V_{IH}(CE)$ . Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high). During the time from the rise of CE to the fall of R/W, R/W is permitted to change from high to low only.

read, modify write cycle timing requirements over recommended supply voltage range,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$

PARAMETER	TMS 4060		TMS 4060-1		TMS 4060-2		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(RW)}$ Read, modify write cycle time*	710		640		580		ns
$t_w(CEH)$ Pulse width, chip enable high*	540	4000	470	4000	410	4000	ns
$t_w(CEL)$ Pulse width, chip enable low	130		130		130		ns
$t_w(wr)$ Write pulse width	200		190		180		ns
$t_r(CE)$ Chip-enable rise time		40		40		40	ns
$t_f(CE)$ Chip-enable fall time		40		40		40	ns
$t_{su(ad)}$ Address setup time	0†		0†		0†		ns
$t_{su(CS)}$ Chip-select setup time	0†		0†		0†		ns
$t_{su(wr)}$ Data-to-write setup time	0		0		0		ns
$t_{su(rd)}$ Read pulse setup time	0†		0†		0†		ns
$t_{su(dw)}$ Write pulse setup time	240†		220†		210†		ns
$t_h(ad)$ Address hold time	150†		150†		150†		ns
$t_h(CS)$ Chip-select hold time	150†		150†		150†		ns
$t_h(di)$ Read hold time	230†		230†		190†		ns
$t_h(dw)$ Data hold time	180†		40†		40†		ns

† The arrow indicates the edge of the chip enable pulse used for reference: † for the rising edge, ‡ for the falling edge.

\* Test conditions:  $V_{DD} = 2.0\text{V}$ .

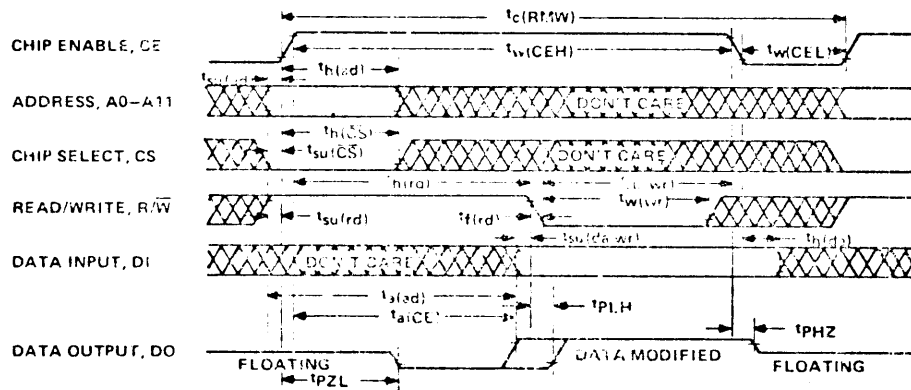
2107 A cont'd

read, modify write cycle switching characteristics over recommended supply voltage range,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$

PARAMETER	TMS 4960		TMS 4960-1		TMS 4960-2		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{CE}$ Access time from chip enable $\bar{t}$		250		220		150	ns
$t_{ACT}$ Access time from address $\bar{t}$		300		250		200	ns
$t_{PLH}$ Propagation delay time, low-to-high level output from write pulse $\bar{t}$	30		30		30		ns
$t_{PHZ}$ Output disable time from high level $\bar{t}$	30		30		30		ns
$t_{PZL}$ Output enable time to low level $\bar{t}$		250		200		150	ns

$\bar{t}$  Test conditions:  $C_L = 50$  pF,  $t_{(CE)} = 20$  ns, Load = 1 Series 74 TTL gate.  
 $\bar{t}$  Test conditions:  $C_L = 50$  pF, Load = 1 Series 74 TTL gate.

read, modify write cycle timing



NOTE: For the chip enable input, high and low timing points are 90% and 10% of  $V_{IH}(CE)$ . Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).

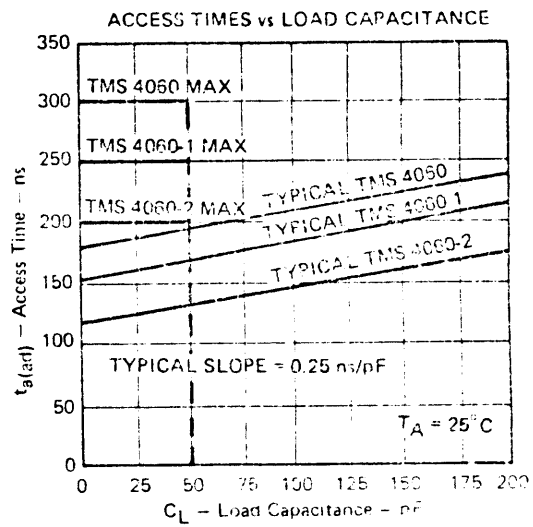
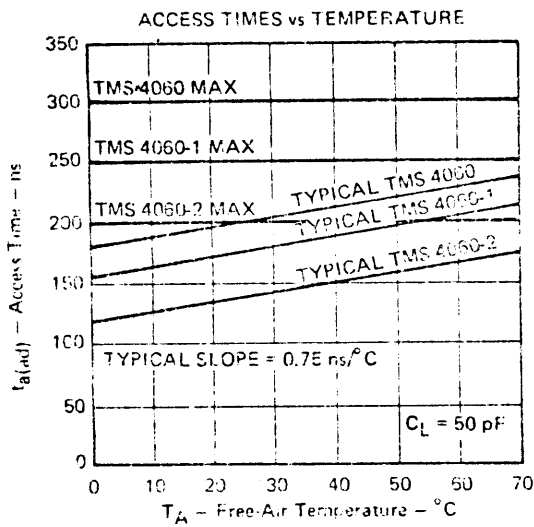
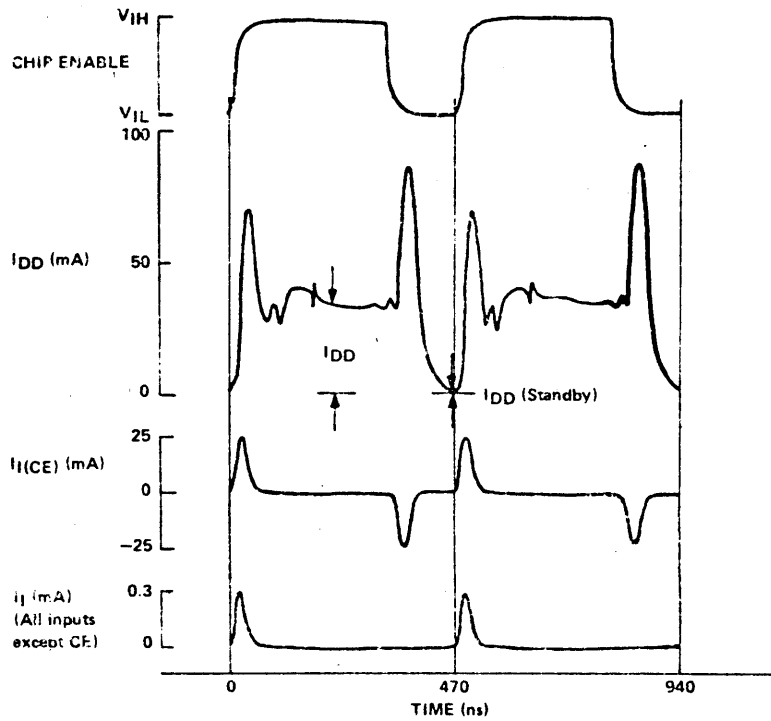
timing diagram conventions

TIMING DIAGRAM SYMBOL	INPUT FORCING FUNCTIONS	MEANING	OUTPUT RESPONSE FUNCTIONS
	Must be steady high or low		Will be steady high or low
	High-to-low changes permitted		Will be changing from high to low sometime during designated interval
	Low-to-high changes permitted		Will be changing from low to high sometime during designated interval
	Don't care		State unknown or charging
	(Does not apply)		Center line is high-impedance off-state



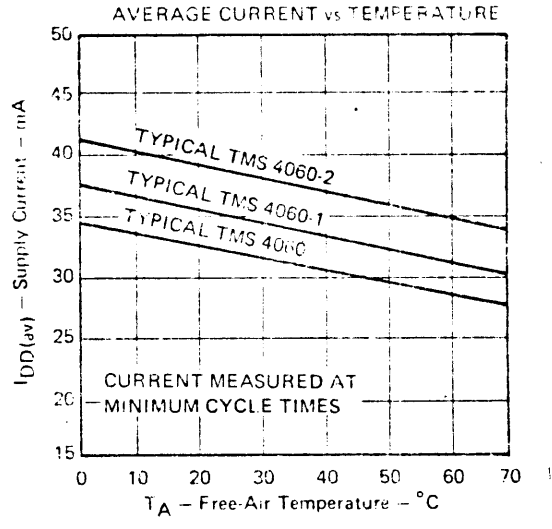
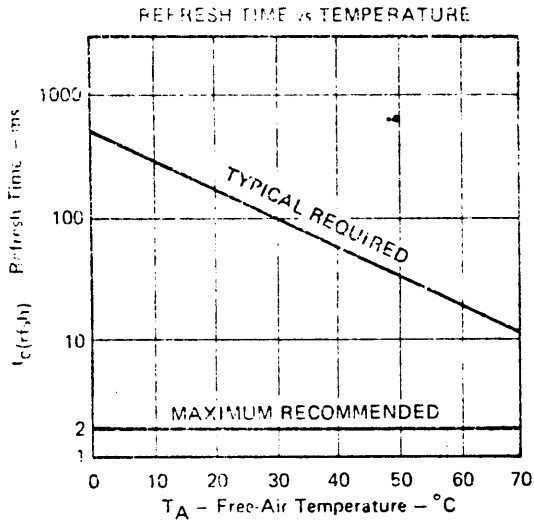
21C7 A cont'd

TYPICAL WAVEFORMS



D COMPONENT DESCRIPTIONS  
 D.8 MEMORIES

2107 A cont'd



Books

Basic	Robert L. Albrecht, LeRoy Finkel, and Jerald R. Brown	John Wiley & Sons, Inc.
Microprogramming Handbook		Microdata
My Computer Likes Me		Dymax
101 Basic Computer Games		Digital Equipment Corp.
What To Do After You Hit Return		Peoples Computer Company
Structured Programming	O.J. Dahl; E.W. Dijkstra; C.A.R. Hoare	1972 Academic Press, New York
The Logical Design of Operating Systems	Alan C. Shaw	1974 Prentice-Hall, INC, Englewood Cliffs, NJ
Fundamental Algorithms-The Art of Computer Programming	Donald E. Knuth	Addison-Wesley Pub. Co. INC. Menlo Park, Calif.
Switching & Finite Automat Theory	Zvi Kohavi	McGraw-Hill Book Co. New York
Introduction to Computing	T.E. Hull	1966 Prentice-Hall
Computer Architecture	Carton C. Foster	1970 Van Nostrand Reinhold Co. 450 W. 33rd St., NY, NY
Introduction to Artificial Intelligence	Philip C. Jackson	Petrocelli Books, New York
Introduction to Computer Organization & Data Structure	Harold S. Stone	McGraw-Hill 1972
Introduction to Micro Computer	Adam Osborne	Osborne And Associates Inc. 2950 Seventh St. Berkeley, Calif. 94710
Micro-Computer Dictionary and Guide	Charles Sippi	
Computer Chess	Monroe Newborn	
The Elements of Programming Style	Brain W. Kernighan/P.J. Plauger	McGraw-Hill, New York, N.Y. 1974
Designing Logic Systems Using State Machines	Christopher R. Clare	McGraw-Hill New York, New York 1973
T T L Cookbook	Don Lancaster, Howard W. Sams & Co.	Indianapolis, Indiana 1974
Computer Lib/Dream Machines	Theodore H. Nelson	Hugo's Book Service, Box 2622, Chicago,

## Periodicals

Byte Magazine  
Petersboro, New Hampshire  
03458

Computer Decisions  
Hayten Publishing Co., Inc.  
50 Essex St.  
Rochelle Park, NJ  
07662

Computer Design  
221 Baker Ave.  
Concord, MA  
01742

Computer Magazine  
McGraw-Hill Publications Inc.  
1221 Avenue of the Americas  
New York, N.Y.  
10020

Data Communications  
McGraw-Hill Publications, Inc.  
1221 Avenue of the Americas  
New York, N.Y.  
10020

Datamation  
1801 S. La Cienega Blvd.  
Los Angeles, CA  
90035

Digital Design  
Benwill Publishing Corp.  
167 Corey Rd.  
Brookline, MA  
02146

E.D.N.  
221 Columbus Ave.  
Boston, Mass.  
02116

Electronic Design  
Hayden Publishing, INC.  
50 Essex St.  
Rochelle Park, NJ  
07662

Electronics Magazine  
McGraw-Hill Publications, INC.  
1221 Avenue of the Americas  
New York, N.Y.  
10020

Electronic Products  
645 Stewart Ave.  
Garden City, N.Y.  
11530

Elementry Electronics  
Davis Publications, INC.  
229 Park Ave. So.  
New York, N.Y.  
10003

Infosystems  
Hitchcock Building  
Wheaton, Ill.  
60187

Mini/Micro Systems  
5 Kane Industrial Dr.  
Hudson, Mass.  
01749

Popular Electronics  
Ziff-Davis Publishing Co.  
Editorial & Executive Office  
One Park Ave.  
New York, N.Y.  
10016

Popular Mechanics  
Hearst Corp.  
224 West 57th St.  
New York, N.Y.  
00019

Popular Science  
380 Madison Ave.  
New York, N.Y.  
10017

Radio Electronics  
Gernback Publications, INC.  
200 Park Ave So.  
New York, N.Y.  
10003

Creative Computing  
Ideametrics  
P.O. Box 789-M  
Morristown, NJ  
07960

IEEE Spectrum  
The Institute of Electrical and  
Electronics Engineers, INC.  
345 East 47 St.  
New York, N.Y.  
10017

Computer & People  
815 Washington St.  
Newtonville, MA  
02160

Periodicals cont'd

Data Processing  
134 N. 13th St.  
Philadelphia, PA  
19107

Peoples Computer Company  
P.O. Box 310  
Menlo Park, Calif.  
94025

Sphere Users Groups

Warren Weimer  
23025 Kinard  
Carson, Calif. 90745

Trenton State Col. Digital Cp.  
Dept. of Engineering Tech.  
Trenton State College  
Trenton, New Jersey 08625

Long Island Computer Assoc.  
P.O. Box 864  
Jamaica, New York 11431

Southern Calif. Comp. Society  
Ward Spaniol  
Box 987  
South Pasadena, Calif. 91030

CACHE  
c/o Robert Swartz  
195 Ivy Lane  
Highland Park, Ill. 60035

Amateur Compt. Group of N.J.  
S. Libes  
V.C.T.I.  
1776 Raritan Rd.  
Scotch Plains, NJ 07076

Midwestern Affiliation of Comp.  
P.O. Box 83  
Brecksville, Ohio 44141

Homebrew Computer Club  
Box 626 (193 Thompson Sq. )  
Mountain View, Calif. 94042

Atlanta Ham Festival  
53 Old Stone Mill Rd.  
Marietta, Georgia 30062

Personal Systems  
10137 Caminite Jovial  
San Diego, Calif. 92126

LLLRA Hobbieist Computer Club  
c/o Gordon Jones  
4257 Findlay  
Livermore, Calif. 94550

John Blackhall  
3608 Larchmont Sq. Lane  
Sacramento, Calif. 95821

Chesapeak Micro Compt. Club  
% Dr. Jerald Zegar Esq. Suite 201  
7338 Baltimore Ave.  
College Park, Maryland 20740

Denver Amateur Compt. Club  
Jerry Fife  
Box 6338  
Denver, Colo. 80206

Villa West Compt. Society  
% Michael McGinnis  
13613 So. 86th Ave.  
Orland Park, Ill. 60462

Oklahoma City Club  
Bill Cowden  
2412 S. W. 45th  
Oklahoma City, Oklahoma 73119

NECS  
% Carl Helmers  
Byte Magazine  
Petersborough, NH 03458

People Compt. Comp.  
% Dymax  
P.O. Box 310  
Menlo Park, Calif. 94025

Canadian Computer Club  
c/o Harold Dye Jr.  
1860 Windmere Dr. N.E.  
Atlanta, Georgia 30324

Micro 8 Compt. User Group  
Hal Singer  
Cabrillo Computer Center  
4350 Constellation Rd.  
Lompoc, Calif. 93436

Crescent City Comput. Club  
Atn: Bob Latham  
Univer. of New Orleans  
Box 1097 Lakefront  
New Orleans, Louisiana 70122

Cleveland Digital Group  
1200 Seneca Blvd.  
Apt. 407  
Broadview Heights, Ohio 44147

Texas Amateur Compy. Club  
% Bill Fuller  
2377 Dalworth, Apt. 157  
Grand Prarie, Texas 75050

Computers For Hobbyists  
Mike Hayes  
Box 367  
Jamul, Calif. 92035

G ASSEMBLY INSTRUCTIONS

G.1 KIT ASSEMBLY INSTRUCTIONS

WARNING 1

SOLDER EACH PIN CAREFULLY AND COMPLETELY FROM THE BACK OF THE BOARD WITH A SOLDERING IRON (NOT A SOLDERING GUN) AND DO NOT LEAVE A HOT TIP ON THE IC PIN OVER 5 SECONDS.

WARNING 2

WHENEVER A CPU, ACIA, PIA (40 PIN IC), 1702 PROM (24 PIN IC), 4K DYNAMIC MEMORY (22 PIN CHIPS) OR ANY OTHER CHIP IN BLACK FOAM OR A SPECIAL PACKAGE IS REMOVED OR HANDLED USE CAUTION TO PREVENT STATIC CHARGE. USE SPECIAL PLASTIC SHIPPING PACKAGE TO HOLD THE IDLE IC CHIP SINCE IT IS CONDUCTIVE AND PREVENTS STATIC CHARGE BUILDUP. IT IS ADVISABLE TO "GROUND" YOURSELF PRIOR TO HANDLING THIS IC, ESPECIALLY IF YOU ARE ON A CARPET.

CHECK PARTS procedure: When Kit arrives check all items against the Parts List. If any part appears to be missing, check against any extra parts. Some equivalent substitutes may have been sent to avoid delays in shipping. If a shortage exists, SPHERE will mail any actual shortages you request within two weeks. Check the entire shipment as only one "missing parts" request will be handled. All other requests for parts will be considered purchases. All parts that are in parenthesis on the parts list are optional and are not provided by SPHERE.

NOTE I

The printed circuit board is marked with labels to identify location of parts. Each label includes a letter prefix followed by a number. Each letter identifies a particular type of component. A list of component types and identifiers is included below:

C CAPACITORS  
D DIODES  
E INTEGRATED CIRCUITS  
L INDUCTOR  
Q TRANSISTOR  
R RESISTOR  
X CONNECTOR SOCKET

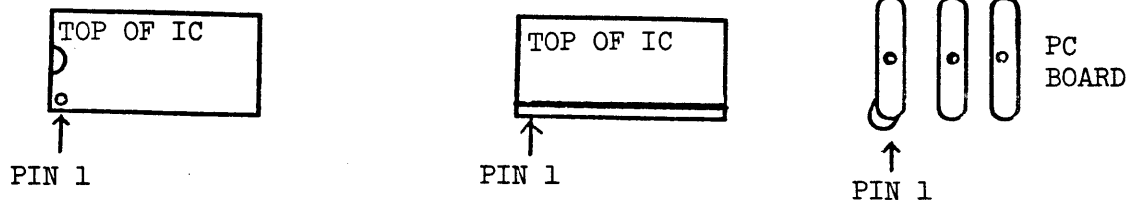
To aid location of parts, a parts layout is provided for each board.

## G ASSEMBLY INSTRUCTIONS

### G.1 KIT ASSEMBLY INSTRUCTIONS cont'd

#### NOTE II

Most sockets and IC's are to be mounted with PIN 1 located in the lower left corner (with printed circuit board writing in normal position). On a chip or socket PIN 1 is designated by the notched end or the dot to the left or a bar. PIN 1 on PC board is marked with extra dot of etch.



If any problems develop in the function of a board the theory of operation should be used in conjunction with the schematic to debug the module.

#### IMPORTANT

Read all instructions before handling the parts as damage may result if the parts are improperly handled.

#### G.1.1 ASSEMBLY INSTRUCTIONS FOR KBD/2

- \_\_\_\_\_ CHECK PARTS - When Kit arrives check all items against the Parts List. If any part appears to be missing, check against any extra parts. Some equivalent substitutes may have been sent to avoid delays in shipping.
- \_\_\_\_\_ SOCKET INSERTION - Place 14 pin dual-in-line socket on front side of board in position X20. Carefully solder socket in place. Check with ohm meter.
- \_\_\_\_\_ RESISTORS & CAPACITORS - Carefully bend leads of resistors and capacitors to required length and insert on front side of board in positions shown on layout sheet. Solder carefully and cut off extra lead lengths. Insert and solder resistor networks with PIN 1 to the right.
- \_\_\_\_\_ INTEGRATED CIRCUITS - Most Integrated Circuits (IC's) come with the leads spaced a little wider than the printed circuit board layout holes. Remove each of the IC's one at a time and press carefully one side of the pins on a hard surface. Repeat on the other side and fit into P.C. board position holes. If IC is still too wide, repeat this process carefully until the parts fit into their proper location. BE SURE PIN 1 IS IN THE PROPER PLACE.



## G ASSEMBLY INSTRUCTIONS

### G.1 KIT ASSEMBLY INSTRUCTIONS

#### G.1.1 ASSEMBLY INSTRUCTIONS FOR KBD/2 cont'd

\_\_\_\_\_ KEYBOARD - Place the keyboard assembly on the PC board being very careful not to bend the many pins. Solder the keyboard in place being sure that enough solder is used to make good electrical contact. Do not overheat the terminals.

\_\_\_\_\_ INSPECTION:

#### NOTE

CAREFUL INSPECTION WILL SAVE MANY HOURS OF DEBUGGING LATER.

Procedure: Using a magnifying glass examine each solder joint and printed circuit trace for problem "splashes" or "cold" joints.

#### NOTE

The KBD/2 is capable of producing both upper and lower case characters if desired. However most software is not able to recognize that A=a. To inhibit lower case characters:

1. Cut etch between ASCII and FULL
2. Cut etch between E7-4 and E7-13 (near Pin 13 there is a loop for that purpose).
3. Add a jumper from ASCII to MOD along the dotted line
4. Add a jumper from FULL to E7-4 (soldering to leg of the IC is o.k.).

This will cause the normal, unshifted characters to be UPPER case, the shifted position to be lower case. Involved are the alphabetic characters and @, \, ^.

\_\_\_\_\_ KEYBOARD PHYSICAL ATTACHMENT - Using spacers and screws provided mount the keyboard to the metal cover. Mount the metal cover to the metal base by first inserting the side screws (one on each side) then the three screws under the front of the base.

\_\_\_\_\_ KEYBOARD ELECTRICAL ATTACHMENT - Using the one 14 conductor cable provided with a connector at each end connect Keyboard X20 to CPU/2 X4 being sure Pin 1 is connected to Pin 1.

## G ASSEMBLY INSTRUCTION

## G.1 KIT ASSEMBLY INSTRUCTIONS

## KEYBOARD PARTS LIST

## G.1.1 ASSEMBLY INSTRUCTIONS FOR KBD/2 cont'd

REF	SCHEMATIC	C000027		
1	PC BOARD	E000028		
1	ALPHANUMERIC KEYBOARD	873-10184		
1	CAPACITOR 100 $\mu$ F 10V	DDM-103	C9	
1	CAPACITOR .01 $\mu$ F		C7	
1	CAPACITOR 100PF		C6	
1	CAPACITOR .2 $\mu$ F		C5	
1	CAPACITOR .001 $\mu$ F		C4	
4	CAPACITOR .1 $\mu$ F 50V	CK104	C1,C2,C3,C8	
1	RESISTOR 47K 1/4W	RC07GF473	R18	
1	RESISTOR 10K 1/4W	RC07GF103	R17	
2	RESISTOR NETWORK	750-81-R33K	R2-8,R10-16	
8	RESISTOR 3.3K 1/4W	RC076F332	R1,9,19-24	
1	SOCKET, 14 PIN IC	314-A639D	X20	
1	DUAL D FLIP FLOP	SN7474N	E12	
1	QUAD 2 INPUT NAND	SN7400N	E11	
1	QUAD 2 INPUT AND	SN7408N	E10	
1	HEX INVERTER	SN7404N	E9	
1	QUAD EXCLUSIVE - OR	SN7486N	E7	
1	DUAL ONE SHOTS	SN74123N	E6	
1	BCD TO DECIMAL DECODER	SN7442N	E4	
1	16 TO 1 MULTIPLEXER	SN74150N	E3	
2	HEX BUFFER/DRIVER	SN7407N	E2,E8	
2	4 BIT BINARY COUNTER	SN7493N	E1,E5	

## G ASSEMBLY INSTRUCTIONS

### G.1 KIT ASSEMBLY INSTRUCTIONS

#### G.1.2 ASSEMBLY INSTRUCTION FOR MEM/1

14 PIN SOCKET INSERTION - Place IC 14 pin sockets in positions X1, X2, X3 and X6 on front (writing) side of board. Solder sockets carefully in place. Verify good solder joints with an ohm-meter.

INTEGRATED CIRCUITS - Most Integrated Circuits (IC's) come with the leads spaced a little wider than the printed circuit board layout holes. Remove each of the IC's except the memory chips one at a time and press carefully one side of the pins on a hard surface. Repeat on the other side and fit into P.C. board position holes. If IC is still too side repeat this process carefully until the parts fit into their proper locations. BE SURE PIN 1 IS IN THE PROPER PLACE. See layout sheet and Parts List for positions.

DIODES AND RESISTORS - Carefully bend leads of diodes and resistors to required length and insert on front side of board in positions shown on layout sheet. Solder carefully and cut off extra lead lengths. Leave the 2 Ohm Resistors slightly off the board as they get warm.

TRANSISTORS - Insert transistors on the front side of the board in positions shown on layout sheet. Be aware of the correct positioning of the transistor before inserting it into the circuit board.

CAPACITORS - Insert capacitors on front side of board in positions shown on layout sheet. Solder carefully and cut off extra lead lengths. Note the polarity of the larger capacitors, (100uf 10v, 47uf 16v.)

4K DYNAMIC MEMORY (22 PIN CHIPS) - Your memories have been pretested at the factory. Carefully remove Memory Chips from packing tube and insert into the first column of 8 designated positions. Be sure to take precautions to ground yourself before inserting them into the circuit board. Test board with first bank in place. If a failure should be noted, your grounding precautions may not be adequate. A single ship accounts for one bit in an 8 bit word and can usually be detected easily by writing in all zeros and reading back. Note that all banks are common and a failure would affect the other 3 columns also. For this reason it is best to insert and test 1 bank of 8 at a time. You may order replacement Memory chips from Sphere. Use a grounded soldering iron. As alternative to this procedure is to use 22 pin IC sockets. Insert and solder the sockets in place. Then carefully insert the memory chips. (Sockets are also available from Sphere).

ITEM	QTY	PART NO.	DESCRIPTION	DESIGN.	✓
1	1	MEM/1	P.C. BOARD -	MEM/1	
2	1	SN74123	ONE SHOT	E7	
3	1	SN7400	NAND GATES	E6	
4	1	SN7402	NOR GATES	E3	
5	1	SN7404	INVERTER	E1	
6	1	SN7408	AND GATE	E5	
7			SPARE	E2	
8	1	SN7483	FULL ADDER	E8	
9	2	DM8098	BUFFER	E10,E11	
10	1	SN74156	2 Line to 4 Line DEMUX	E9	
11	32	ZA-0428	4K X 1 DYNAMIC RAM	E12-E14	
12			SPARE	E4	
13	4	2N2369A	TRANSISTOR	Q1-Q4	
14	3	1N4001	DIODE	D3-D5	
15	1	1N914	DIODE	D1	
16	1	1N5225B	3.0V ZENER	D2 *	
17	4		RESISTOR, 100ohm 2w	R6-R9	
18	4		RESISTOR, 3.3K 1/4w	R2-R5	
19	1		RESISTOR, 33K 1/4w	R1	
20	1		RESISTOR, 100ohm 1/4w	R10 *	
21	1		CAPACITOR, 33pf	C4	
22	46		CAPACITOR, .1 uf	C1-3,C5-7,C14-53	
23	1		CAPACITOR, 100 uf 10v	C12	
24	5		CAPACITOR, 47 uf 16v	C8-C11,C13	
25	4	314-A639D	14 PIN SOCKET	X1-X3,X6	
26	5		RESISTOR 510 ohm 1/4w	R11-R15	

\*Parts not used but jumper -3 to -5 when -5v RAMS used

## G ASSEMBLY INSTRUCTIONS

### G.1 KIT ASSEMBLY INSTRUCTIONS

#### G.1.3 ASSEMBLY INSTRUCTIONS FOR CRT/1A

\_\_\_\_\_ SOCKET INSERTION - Place 14 pin sockets in positions X1, X2, X3, X6 on front side of board. (X5 is optional on this board). Place 24 pin sockets in E8, E14, E20, E25 and E30. Solder sockets carefully in place. Verify good solder joints with ohm-meter.

\_\_\_\_\_ DIODES AND RESISTORS - Carefully bend leads of resistors and diodes to required length and insert on front side of board in positions shown on layout sheet. Solder carefully and cut off extra lead lengths.

\_\_\_\_\_ TRANSISTORS - Insert transistors on front side of board in positions shown on layout sheet. Be aware of the correct positioning of the transistor before inserting it into the circuit board.

\_\_\_\_\_ CAPACITORS - Insert on front side of board in positions shown on layout sheet. Solder carefully and cut off extra lead lengths. Note the polarity of the larger capacitors, (100 $\mu$ F 10v, 47 $\mu$ F 16v) There will be a "+" on the capacitor and a "+" on the PC Board which must be aligned.

\_\_\_\_\_ INTEGRATED CIRCUITS - Most Integrated Circuits (IC's) come with the leads spaced a little wider than the Printed circuit board layout holes. Remove each of the IC's one at a time and Press carefully one side of the pins on a hard surface. Repeat on the other side and fit into P.C. Board position holes. If IC is still too wide, repeat this process carefully until the parts fit into their proper locations. BE SURE PIN 1 IS IN THE PROPER PLACE. Solder each pin carefully and completely from the back of the board. See the layout sheet and Parts List for positions.

DO NOT REMOVE 24 PIN LARGE IC's FROM PACKAGE UNTIL 24 PIN SOCKETS HAS BEEN SOLDERED IN PLACE ON THE P.C. BOARD. USE SPECIAL PLASTIC SHIPPING PACKAGE TO HOLD THE IDLE IC CHIP SINCE IT IS CONDUCTIVE AND PREVENTS STATIC CHAGE BUILDUP. MOS devices may be damaged by static charge.

\_\_\_\_\_ 24 PIN CHIPS - Carefully remove the 6810's memories and 2513 character generator 24 pin ships form packages and insert with pin 1 in the proper locations.

\_\_\_\_\_ INSPECTION - Following assembly, inspect carefully all Solder joints and lines for problem splashes or "cold" joints.

## G ASSEMBLY INSTRUCTIONS

### G.1 KIT ASSEMBLY INSTRUCTIONS

#### G.1.3 ASSEMBLY INSTRUCTIONS FOR CRT/1A cont'd

\_\_\_\_\_  
VIDEO MONITOR - If a Video Monitor is used, connect composite VIDEO wires to the pads labeled "COMP VIDEO OUT and GND". Add a jumper from +5v to D4 along the dotted line shown.

\_\_\_\_\_  
TELEVISION TRANSMITTER - If you want to connect up to a commercial TV, the TV XMIT circuit area must be built. Parts for it are shown in ( ) in the parts list and the Schematic shows the circuit. By placing a shield can over the completed TV circuit after laying a section of TV antenna Twin Lead along the shown path, you will eliminate most radiation. Components will not be supplied by SPHERE Corp. The circuit was not implemented because FCC regulations make this form of implementation impractical. If implemented you do so at your risk. Solder the twin lead antenna to the feed throughs at the bottom of the "Ground" and "Antenna" etch paths, not directly to the long etches.

#### ADDRESS INTERFACING

Your CRT interface board comes pre-addressed for E000 to E1FF (hex notation). If your programs want to use another address or if you use this board as a Satellite you can change its address as shown in the following table. Note that A9, A10, and A11 straps along the left side and that the Solid etch must be cut before the dashed line is jumpered in.

TABLE 1

<u>Address</u>	<u>Change Lines</u>
<u>E000 - E1FF</u>	none
<u>E200 - E3FF</u>	A9
<u>E400 - E5FF</u>	A10
<u>E600 - E7FF</u>	A9 and A10
<u>E800 - E9FF</u>	A11
<u>EA00 - EBFF</u>	A11 and A9
<u>EC00 - EDFF</u>	A11 and A10
<u>EE00 - EFFF</u>	A11, A10, and A9

## G ASSEMBLY INSTRUCTIONS

## G.1 KIT ASSEMBLY INSTRUCTIONS

## CRT PARTS LIST

## G.1.3 ASSEMBLY INSTRUCTIONS FOR CRT/1A cont'd

ITEM	QNTY	PART#	DESCRIPTION	DESIGNATION
1	1	CRT/1	P.C. Board	
2	4	314-AG39D	14 Pin Socket	X1-X3,X6
3	2	SN7400	Quad NAND Gate	E24,E19
4	2	SN7404	HEX Inverter	E13,E17
5	1	SN7405	HEX Inverter	E16
6	2	SN7408	Quad AND Gate	E26,E27
7	1	SN7409	Quad AND Gate OC	E12
8	1	SN7420	Dual NAND Gate	E18
9	2	SN7430	NAND Gate	E7,E15
10	1	SN7451	Dual AND/OR Gate	E28
11	1	SN7474	Dual D F/F	E23
12	1	SN7490	4 bit Dec. Cntr.	E22
13	3	SN7493	4 bit Bin. Cntr.	E6,E10,E11
14	2	SN7495	4 bit Shift Reg.	E9,E21
15	1	SN74123	Dual Monostable	E31
16	3	SN74157	Quad MUX	E3,E4,E5
17	1	NE555	Timer	E29
18	1	2513N (CM2140)	ASCII Char. Gen.	E8
19	2	DM8833	Quad T/R	E1,E2
20	4	MCM6810	128 x 8 Static RAM	E14,E20,E25,E30
21	1	2N2222Aor2N5129	Transistor	Q1
22	(1)	2N918	Transistor	(Q2)
23	(1)	L1	Inductive Coil	(L1)
24	4(1)	1N914	Diode	D1-D3,(D4),D5
25	1	47 uf	Cap. 16 vdc	C35
26	1(1)	100 uf	Cap. 10 vdc	C1,(C31)
27	24	.1 uf	Capacitor	C2-C14,C17-C19,C21-C22 C26-C28,C30,C33,C36
28	1	.01 uf	Capacitor	C29
29	3	.001 (1K)	Capacitor	C20,C34,C38
30	(1)	27 pf	Capacitor	(C23)
31	1(1)	47 pf	Capacitor	(C16),C37
32	1(2)	470 pf	Capacitor	C15,(C24),(C32)
33	(1)	8-25 pf	Capacitor, var	(C25)
34	1	20K	Resistor, var	R19
35	1	5K	Resistor, var	R20
36	1	50K	Resistor, var	R22
37	(1)	22	Resistor	(R13)
38	2	20K	Resistor	R17,R16
39	(1)	470	Resistor	(R4)
40	8(2)	1K	Resistor	R2,R3,R6-R9,(R12) (R15),R18,R23
41	1	47,1/2w	Resistor	R10
42	1	100,1/2w	Resistor	R11
43				
44	2	10K	Resistor	R1,R5
45	(1)	2.2K	Resistor	(R14)
46	1	3.3K	Resistor	R21

## G ASSEMBLY INSTRUCTIONS

### G.1 KIT ASSEMBLY INSTRUCTIONS

#### G.1.4 ASSEMBLY INSTRUCTIONS FOR CPU/2

\_\_\_\_\_ SOCKET INSERTION - Place IC 14 pin sockets in positions X1, X2, X3, X4, X5 and X6 on front side of board. Place the 22 pin sockets in E2, E5, E11, E17, E19, E26, E34 and E36. Place the 24 pin sockets in E6, E12, E20 and E35 and place the 40 pin sockets in E3 and E50. Solder sockets carefully into place. Verify good soldering techniques with ohm-meter.

\_\_\_\_\_ INTEGRATED CIRCUITS - Most Integrated Circuits (IC's) come with the leads spaced a little wider than the Printed circuit board layout holes. Remove each of the small IC's one at a time and Press carefully one side of the pins on a hard surface. Repeat on the other side and fit into P.C. board position holes. If IC is still too wide, repeat this process carefully until the parts fit into their proper locations. BE SURE PIN 1 IS IN THE PROPER PLACE. (The notched end to the Left or the Dot by the lower left corner). Solder each pin carefully and completely from the back of the board with a soldering iron (Not a Soldering Gun) and do not leave a hot tip on the IC pin over 5 seconds. See the Layout sheet and Parts List for positions.

\_\_\_\_\_ DIODES AND RESISTORS - Carefully bend leads of resistors and diodes to required length and insert on front side of board in positions shown on layout sheet. Solder carefully and cut off extra lead lengths.

\_\_\_\_\_ TRANSISTOR - Insert transistors in board observing polarity and solder into place.

\_\_\_\_\_ CAPACITORS - Insert on front side of circuit board in positions shown on layout sheet. Note the polarity of larger capacitors, (100 F 10v, 47 F 16v). Solder carefully and cut off extra lead lengths.

\_\_\_\_\_ 4K DYNAMIC MEMORIES - Remove 22 Pin Chips carefully from the Shipping Container and insert into positions E2, E5, E11, E17, E19, E26, E32, and E34. Be sure to take precaution to ground yourself before inserting these into sockets on the circuit board. If memories are soldered directly, be sure to ground the soldering iron tip.

\_\_\_\_\_ 1702 PROM - Carefully remove 1702 PROM 24 pin chip from package and insert with Pin 1 mark (normally writing will also be in proper position when Pin 1 Mark is) at lower left corner.



G ASSEMBLY INSTRUCTIONS

G.1 KIT ASSEMBLY INSTRUCTIONS

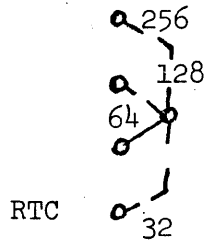
G.1.4 ASSEMBLY INSTRUCTIONS FOR CPU/2 cont'd

CPU AND PIA 40 PIN CHIPS - Carefully remove CPU (6800) 40 Pin chip from package and insert with raised dot OR single alphabetic character as Pin 1. Repeat with 6820 PIA Chip.

INSPECTION - Following assembly inspect carefully all solder joints and lines for problem splashes or "cold" joints.

REAL - TIME CLOCK

The real-time clock is located on the CPU board. It is located immediately left of E8 and is denoted by the symbols "RTC". Below is the layout of the clock on the PC Board.



MODIFICATION - The clock is pre-strapped to 64 interrupts per second.\* If 32, 128, or 256 interrupts per second are desired, the etch to 64 must be carefully cut. An insulated wire (20 to 30 Gage) should be soldered into place between the common point and the selected interrupt rate. To disable the clock entirely, jumper the common point to the location labeled GND above and to the right of E13. To use the CAL line of PIA E3 for other than RTC purposes, all connections to the RTC must be disconnected.

\*The number of interrupts per second is derived from the refresh clock (2 ms) and is approximate.

Teletype driving circuit

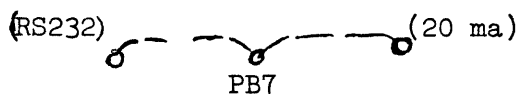
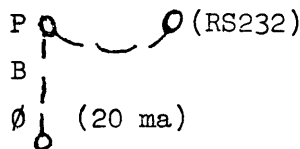
To use either the 20 ma or RS232 interface the parts listed in the assembly 2 parts list must be used.

RS232 Serial interface add strap from PB $\emptyset$  to the right and PB7 to left. Connect terminal to T<sub>x</sub>, GND and R<sub>x</sub>.

20 ma Serial interface Add strap from PB $\emptyset$  down and PB7 to the right. Connect terminal to COM, R<sub>x</sub> and T<sub>x</sub>.

NOTE

When using the CPU/2 as a one card computer the CPU clock must be regulated to 1.5  $\mu$ s  $\pm$  2% to synchronize the CPU with the 110 baud I/O device attached. R14 is used to slow down the clock if necessary.



REF	REF	61	SCHEMATIC	D000019	
1	1	60	PRINTED CIRCUIT BOARD	E000020	
1	1	59	TRANSISTOR	2N2369A	Q1
2	2	58	CAPACITOR CERAMIC 68pf 1kv	DD-680	C24,30
3	3	57	CAPACITOR CERAMIC 33pf 1kv	DD-101	C21,27,31
3	3	56	CAPACITOR CERAMIC 100pf 1kv	DDM-103	C17,22,23
2	2	55	CAPACITOR CERAMIC .01uf 150v	DDM-103	C16,26
1	1	54	CAPACITOR TANTULUM 100uf 10VDC		C5
9	9	53	CAPACITOR 47uf 16VDC	EK47116	C2,3,10,11,13,18,28, 29,32
12	11	52	CAPACITOR CERAMIC .1uf 50V	CK-104	C1,4,6-9,12,14,15,19,20,25
2	2	51	RESISTOR 4.7k ohm 1/4w	RC07GF472	R24,27
2	2	50	RESISTOR 10 ohm 1/4w	RC07GF100	R23,26
2	2	49	RESISTOR 22 ohm 1/4 w	RC07GF220	R22,25
3	3	48	RESISTOR 10k ohm 1/4w	RC07GF103	R21,28,30
4	3	47	RESISTOR 1k ohm 1/4w	RC07GF102	R17,19,31,32
1	-	46	RESISTOR 510 ohm 1/4w	RC07GF511	R16
2	2	45	RESISTOR 470 ohm 1/4w	RC07GF471	R15,33
1	1	44	RESISTOR	RC07GFSEL	R14
1	1	43	RESISTOR 33k ohm 1/4w	RC07GF333	R13
1	1	42	RESISTOR 11k ohm 1/4w 1%	RNC65H2712F	R12
1	1	41	RESISTOR 27.1k ohm 1/4 1%	RNC65H2712F	R11
1	1	40	RESISTOR 15k ohm 1/4w	RC07GF153	R10
1	-	39	RESISTOR 2k ohm 1/4w	RC07GF202	R9
5	5	38	RESISTOR 3.3k ohm 1/4w	RC07GF332	R7,8,18,20,29
1	1	37	RESISTOR 130 ohm 2w	RC42GF131	R6
1	-	36	RESISTOR 820 ohm 1w	RC32GF821	R5
1	-	35	RESISTOR 1.1k ohm 1w	RC32GF112	R4
2	2	34	RESISTOR 36k ohm 1/4w	RC07GF363	R2,3
1	1	33	RESISTOR 100 ohm 1/4w	RC07GF101	R1*
6	4	32	DIODE	1N4001	D5,6,7,8,10,11
5	5	31	DIODE	1N914	D2,3,4,9,12
1	1	30	ZENER DIODE 3V	1N5225B	D1*
8	8	29	22 PIN IC SOCKETS	CA 22-CSITSD	
2	2	28	40 PIN IC SOCKETS	340-A639D	XE3,50
2	4	27	24 PIN IC SOCKETS	324-A639D	XE6,12,20,35
6	4	26	14 PIN IC SOCKETS	314-A639D	X1-X6
1	-	25	QUAD RECEIVER - RS232	MC1489	E52
1	1	24	QUAD TRANSISTOR	MPG6842N	E51
1	1	23	MICROPROCESSOR	MC6800	E50
1	1	22	QUAD EXCLUSIVE OR	SN 7486N	E49
1	-	21	QUAD TRANSMITTER-RS232	MC1488N	E46
2	2	20	QUAD TRI-STATE TRANSCEIVER	DM8833N	E42,43
2	2	19	HEX INVERTER W/OC	SN7405N	E40,41
1	1	18	DUAL ONE SHOTS	SN74123N	E38
2	2	17	QUAD 2-INPUT NAND GATE	SN7400N	E32,E39
2	-	16	PHOTO COUPLER	4N33N	E30,E31
1	1	15	HEX INVERTER	SN7404N	E29
1	1	14	QUAD 2 INPUT AND GATE	SN7408N	E28
-	-	13	(SPARE)		E25
5	5	12	TRI-STATE HEX BUFFER	DM8097N	E15,21,44,47,48,
2	2	11	TRIPLE 3-INPUT AND GATE	SN7411N	E14,18
1	1	10	4-LINE TO 10 LINE DECODER	SN7442N	E13
3	3	9	QUAD 2-INPUT NOR GATE	SN7402N	E10,16,23
2	2	8	DUAL D FLIP FLOP	SN7474N	E9,37
2	2	7	DUAL ONE SHOT	9602(DM8602N)	E8,45
3	3	6	4 BIT BINARY COUNTER	SN7493N	E7,22,27
2	4	5	EPROM 256 X 8 BIT	MM1702A	E6,12,20,35
2	2	4	8-INPUT NAND GATE	SN7420N	E4,24
1	1	3	PERIPHERAL INTERFACE ADAPTER	MC6820	E3
8	8	2	4K DYNAMIC RAM MEMORY	7A0248	E2,5,11,17,19,26,34,36
2	2	1	TRI-STATE HEX INVERTER	DM8098M	E1,33
-02	-01		ASSEMBLY	G-12	*SEE MEM/1 PARTS LIST

## G ASSEMBLY INSTRUCTIONS

### G.1 KIT ASSEMBLY INSTRUCTIONS

#### G.1.5 ASSEMBLY INSTRUCTIONS FOR SIM/1 BOARD

---

14 PIN SOCKET INSERTION - Place 14 pin sockets in positions X1, X2, X3, X24, X25, and X6 on board. Place 24 pin sockets in the following positions depending on options purchased.

Modem option - E34

Cassette 1 - E19

Cassette 11 - E32

Extra EPROM - E3

Solder carefully in place verify good solder connections.

---

DIODES AND RESISTORS - Carefully bend leads of the diodes and resistors to required lengths one by one and mount as shown by Parts List and/or Layout Diagram. Solder carefully into place. Verify resistor values and placement carefully. Due to the many options on this board and the number of discrete components, great care must be used in determining which sections to build up. R74 is used as a trimmer value to establish accurate frequency rates. See Description of Options.

---

TRANSISTOR MOUNTING - Q1, Q2, Q4, and Q5 are plastic packages associated with the two cassette interface sections, these 4 transistors mount with the flat side (top view) facing to the right of the board (X1-X6 at the top). Q3 has a triangular lead configuration and mounts in the normal manner. Solder all transistors in place carefully. You may leave the cases above the board as much as 1/4 inch.

---

CAPACITOR MOUNTING - Most capacitors on a digital logic board are associated with noise bypassing on the power supply lines. This board has several capacitors for this purpose; however, many others are associated with timing functions and active filter sections, and the values and types used are more critical. Follow the Layout sheet and/or Parts List carefully. For better modem operation at 600 Baud, use good temperature compensated capacitors for C28, C29, C30, and C31. At the standard preselected 300 Baud rate, these values are not so critical. C47 and C48 are critical to establish the basic frequency of the Baud rates. These two capacitors should have reasonable temperature and tolerance specifications for teletype operation.

---

CRYSTAL MOUNTING - Place the 1mHz crystal in the two holes by "XTAL". Leave the case about 1/4" to 1/16" above the board.

NOTE: Ignore the dash line jumper option directly under the crystal. A future design will feature crystal controlled CPU clocks and a 1mHz signal will be brought across the address bus line X2-11. At that time, this crystal will be omitted and the jumper added at the factory. Also at that time, R74, R75, C47, C48, and E43 will be eliminated. The dashed lines in the lower left corner will be used to select either 625kHz (divides down for 300 Baud rate) or 455kHz (divides down to 110 Baud rate for teletypes). These two frequencies will be on the address bus lines X1-8 and 9 respectively.

## G ASSEMBLY INSTRUCTIONS

### G.1 KIT ASSEMBLY INSTRUCTIONS

#### G.1.5 ASSEMBLY INSTRUCTIONS FOR SIM/1 BOARD cont'd

---

TRIMPOT MOUNTING - Place the trim pots in R20 and R63 in the 3-hole pattern provided. These are the key adjustment elements to get the cassette interface to operate satisfactorily.

---

INTEGRATED CIRCUITS - The integrated circuits may now be soldered into place. See Layout Sheet and/or Parts List for placement. The 24 pin chips need not be removed from their packages until the assembly is complete and the initial power on tests are run. The only other chips requiring careful handling are the 4000 series CMOS. See General Solder Instructions at the beginning of Appendix G.

---

RELAY MOUNTING - Mount and solder the three relays into positions K1, K2, and K3. Be sure the SPDT type goes into K3 on the lower right side of the board. K1 and K2 are identical SPST contacts.

#### OPTION SELECTION AND SET UP

---

BOARD ADDRESSING - In the center of the upper left quadrant are three address lines that provide for 8 unique binary board addresses. A1, A2, and A3 are prestrapped to address the top ACIA (asynchronous communications interface adaptor), E19, as address F050 in HEX notation. This automatically places the bottom ACIA, E32, at address F060. If a second SIM/1 board is used, the etch by A1 should be cut and a jumper placed across the dotted lines. This moves the ACIA addresses up to F052 and F062. In a like manner, A2 could be changed (cut etch and add jumper) instead of A1 with the resulting change in addresses to F054 and F064. The ultimate selection would be with all three addresses changed (etches by A1, A2, and A3 cut and jumpers soldered in place). This would place the ACIA's respectively at F05E and F06E.

NOTE: The PROM socket at E3 is not selectable and will respond to F800 through FBFF only. If a second board is added, E3 must be left open or else you will have two PROM's residing at the same address and your system will falter. However, you may select any of the addresses for your cassettes or modems and/or use the PROM on any one of the boards. It will still reside at the addresses just below the 4 PROMs on the CPU/2 board.

## G ASSEMBLY INSTRUCTIONS

### G.1 KIT ASSEMBLY INSTRUCTIONS

#### G.1.5 ASSEMBLY INSTRUCTIONS FOR SIM/1 BOARD cont'd

NOTE: ALL OPTION SETUP PROCEDURE ARE BASED ON P.C. BOARD IN ORIGINAL STATE.

---

TELETYPE OPTION - First select 110 baud rate clock at the bottom left of the board. To do this cut the etch on 300 and add a jumper to 110/150 selection. Then add jumper TTY1 in the Lower Left hand corner of the Board above E43. With a scope probe at the 9600 baud rate node above E44, select R74 to yield a 2.18 us period as close as possible. R74 will normally exceed 91K if needed at all. Next cut the etch at TTY2 to the right and below E28 (or remove the modem chip E34) and put in the jumper across the dotted lines. This ground will let the ACIA begin operations. The data input will be wire or'd with the RS232, modem, cassette, TTL direct, and 20 ma. TTY current loop. Since most of these inputs normally hold the receive data line low, some of them must be jumpered out.

For the Teletype option, add jumpers RS232 and TTL by above E5 and below E13 respectively. The 20 ma will NOT be jumpered.

---

MODEM OPTION - If a modem option was not purchased, you will not have parts for the right hand 1/3 of the board. If you desire modem operation and have assembled this section, the following jumpers and cuts will be needed: put in the 20 ma, RS232, and TTL jumpers by or below X35. Verify a 1.6 microsecond period at the 9600 Baud rate node with a scope (lower left corner of the board) R74 may be changed to insure a 1.58 to 1.62 microsecond period. The board comes set for 300 Baud modem operation in half duplex. Connect X25-8 to another boards' X25-1 and vice versa to set up the two way lines. Now decide if your board is to be the originate or answer modem. If you are initiating the call, ground the switch hook signal (SH is on X25-11). If you are receiving the call, ground the ring indicator (RI is on X25-2).

If you wish to use an acoustic data coupler (Full duplex), the following additional jumpers must be set up: DCP1 is cut and a jumper put along the dotted line. DCP2 and DCP3 are set up the same way. Now X25-3 is the data line (DL) and ground is X25-5 and X25-14 (DR and GND). The OFF hook and Data Answer are on X25-4 and 12 respectively. X25-6 is for TV.

To operate at 600 Baud, change the jumper on Baud Rate from 300 (cut etch) to 600 and make the cut and jumper change at 300/600 by the crystal. If a modem is not used (i.e. cassette #1 or teletype, etc. are used), it is best not to put the modem MC6860 on the board.

There are no tune-up pots on the modem section. If the filter sections are carefully assembled, it should run with less than .0001% error at 300 baud and about .001% errors at 600 baud. Excessive errors are normally caused by resistor values outside the 1% range, or capacitors outside their 5% tolerance range.

## G ASSEMBLY INSTRUCTIONS

### G.1 KIT ASSEMBLY INSTRUCTIONS

#### G.1.5 ASSEMBLY INSTRUCTIONS FOR SIM/1 BOARD cont'd

---

CASSETTE #1 OPTION - To use ACIA #1 (E19) as a cassette interface, you must insert Jumpers 20 ma, RS232, TTL, CAS 1, CAS RXC, and CAS TXC. These latter 2 jumpers require 2 etch cuts while the former 3 are jumpers only. See description of cassette 11 for tune up involving the Trimpot R20.

X24-1 is the connection from the recorder output or "Earphone" jack.  
X24-13 is the connection to the recorder input or "mike" jack.  
X24-7 is ground.  
X24-4 and 5 are the relay contacts to control the cassette on/off function.  
X24-10 will provide 24 ma of +12 volts to drive a separate relay to control the AC power line if necessary.

Jumper TTY 2 by E32 must be added and the modem chip (MC6860) E34 must be removed. Keep E34 safe in conductive foam when not in use.

---

SECOND CASSETTE INTERFACE OPTION - E32 and the associated circuitry is also designed for a 300 baud "Kansas City" standard cassette interface and plays no part in teletypes or other serial interfaces. If your Kit has this option, you will have the following parts to be added, otherwise leave these items open and build the other sections of the board.

E27, 28, 29, 30, 32, 33, 39, 40, 47, 48,  
R48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 62, 64, 65, 66, 79, 80, 81, 82  
C37, 38, 39, 40, 41, 42, 43, 44, 54, 56, 57, 58  
Q4, Q5  
Potentiometer R63

Note that E38, R76, R77, C50, and C51 comprise the 300 baud rate clock for both cassette sections and must be included unless no cassettes are to be used.

---

TUNE UP - R63, (R20) the variable TRIMPOT must be set carefully for error-free cassette operation. One procedure is to look at the collector of Q5 (Q2 on cassette #1) with a scope. Set the vertical on 1 volt/division with the base line 2 1/2 volts below the center (when grounded). Now begin to receive from a cassette and select the time base such that several bits (0's and 1's have slightly different amplitude as well as density on the screen) are present. Now vary the Pot until the tops of the high amplitude bits are above the center line and the tops of the low amplitude bits are below the center line. This should be very close for good data transmission.

X24-11 is the input from the cassette recorder ("Earphone") jack.  
X24-12 is the output to the recorder "Mike" or "Aux" jack.  
X24-7 is GROUND for the earphone and AUX  
X24-2 and 3 are the contacts of a 10 watt relay to control the recorder on/off jack.  
X24-14 will provide 24 ma of +12v to drive a separate relay if the small on board relay can not handle your load.

G ASSEMBLY INSTRUCTIONS

G.1 KIT ASSEMBLY INSTRUCTIONS

G.1.5 ASSEMBLY INSTRUCTIONS FOR SIM/1 BOARD cont'd

PARTS LIST

				SCHEMATIC	D000023		
			1	PRINTED CIRCUIT BOARD	E000024		
-	1	-	-	CRYSTAL	1MHZ	XTAL	
-	1	-	-	RELAY	220-001-12	K3	
1	-	1	-	RELAY	220-100-12	K1,K2	
-	1	-	-	TRANSISTOR	2N2369	Q3	
1	-	1	-	TRANSISTOR	MPS6521	Q2,Q5	
1	-	1	-	TRANSISTOR	MPS6523	Q1,Q4	
-	2	-	-	CAPACITOR, 1uf		C59,60	
-	-	-	1	CAPACITOR, 100pf 600V NPO	DTZ-100	C48	
-	-	-	1	CAPACITOR, 33pf 1KV	DD-101	C47	
1	-	1	-	CAPACITOR, 470pf 1KV	DD-471	C24,56	
3	12	3	-	CAPACITOR, .01uf 150V	C15,16,18,20,22,25,28-33,45,46,50,51,53,54,57		
-	-	-	1	CAPACITOR, 100uf 10V		C12	
1	-	1	-	CAPACITOR, .0062uf 1KV	AE0062 1KV	C9,44	
1	-	1	1	CAPACITOR, 100pf 1KV	DD-101	C8,43,52	
2	-	1	-	CAPACITOR, 47uf 16V	EK47116	C7,10,11,35,42	
2	-	2	-	CAPACITOR, .001 1KV	DD-102	C5,6,40,41	
1	-	1	-	CAPACITOR, .047uf 50V	AE.047M 50V	C4,39	
1	-	1	-	CAPACITOR, .0015uf 1KV	DD-152	C3,38	
1	-	1	-	CAPACITOR, .47uf 16V		C2,37	
3	5	-	-	CAPACITOR, .1uf 50V	C1,13,14,17,21,23,26,27,34,36,49,55,58,61,62		
-	1	-	-	RESISTOR, 680ohm 1/4w	RC07GF681	R89	
-	3	-	-	RESISTOR, 1.5K 1/4w	RC07GF152	R83-85	
-	-	-	-	RESISTOR	RC07GF(SEL)	R74	
-	1	-	-	RESISTOR, 97.6K 1/4w 1%		R73	
-	1	-	-	RESISTOR, 255K 1/4w 1%		R72	
-	1	-	1	RESISTOR, 8.87K 1/4w 1%		R71,75	
-	1	-	-	RESISTOR, 95.3K 1/4w 1%		R70	
-	1	-	-	RESISTOR, 619ohm 1/4w 1%		R69	
-	1	-	-	RESISTOR, 330K 1/4w	RC07GF334	R59	
-	2	-	-	RESISTOR, 1MEG 1/4w	RC07GF105	R58,60	
-	1	-	-	RESISTOR, 237K 1/4w 1%		R47	
-	1	-	-	RESISTOR, 1.24K 1/4w 1%		R46	
-	1	-	-	RESISTOR, 8.66K 1/4w 1%		R45	
-	1	-	-	RESISTOR, 21.5K 1/4w 1%		R44	
-	1	-	-	RESISTOR, 845ohm 1/4w 1%		R42	
-	1	-	-	RESISTOR, 210K 1/4w 1%		R41	
-	1	-	-	RESISTOR, 324ohm 1/4w 1%		R40	
-	1	-	-	RESISTOR, 18.7K 1/4w 1%		R39	
-	3	-	-	RESISTOR, 510ohm 1/4	RC07GF511	R36,67,68	
1	-	1	-	RESISTOR, 100K 1/4w	RC07GF104	R33,80	
2	-	2	-	RESISTOR, 10K 1/4w	RC07GF103	R32,35,79,82	
1	-	1	-	RESISTOR, 20K 1/4 W		R34,81	
-	2	-	-	RESISTOR, 165K 1/4w 1%		R26,43	
-	1	-	-	RESISTOR, 267ohm 1/4w 1%		R25	
-	-	-	1	RESISTOR, 1.2K 1/4w	RC07GF122	R24	
1	-	1	-	POTENTIOMETER 20K	3359P	R20,63	
1	-	1	-	RESISTOR, 100OHM 1/4w	RC07GF101	R19,62	
1	2	1	-	RESISTOR, 22K 1/4w	RC07GF223	R18,21,27,64	
-	2	-	-	RESISTOR, 15K 1/4w	RC07GF153	R16,28	
-	1	-	-	RESISTOR, 620ohm 1/4w	RC07GF621	R15	

-	-	-	-	2	RESISTOR, 510OHM 1w	RC32GF511	E13,E14
-	-	-	1	-	RESISTOR, 820OHM 1w	RC32GF821	E12
-	-	-	1	-	RESISTOR, 1.1K 1w	RC32GF112	E11
1	6	1	-	2	RESISTOR, 1K 1/4w	RC07GF102	E10,17,30,37,38,57,77,86-88
1	1	1	-	-	RESISTOR, 4.7K 1/4w	RC07GF672	E8,55,61
1	-	1	-	3	RESISTOR, 3.3K 1/4w	RC07GF332	E6,29,31,53,76
3	-	3	-	1	RESISTOR, 47K 1/4w	RC07GF673	E3,4,23,50,51,66,78
4	-	4	-	-	RESISTOR, 33K 1/4w	RC07GF333	E2,7,9,22,49,54,56,65
2	-	2	-	-	RESISTOR, 2.2K 1/4w	RC07GF232	E1,5,48,52
1	2	1	3	7	DIODE	1N4001	D1-D13
1	1	-	-	2	24 PIN IC SOCKETS	324-A639D	E3,19,32,34
-	-	-	-	6	14 PIN IC SOCKETS	314-A639D	X1-3,6,24,25
-	-	-	-	2	4 BIT BINARY COUNTER	SN7493N	F44,45
-	-	-	-	1	ONE SHOT	9601(DM8601N)	F43
-	-	-	-	1	PRECISION TIMER	SN72555P	F38
-	1	-	-	-	MODEM	MC6860	F34
-	-	-	-	-	SPARE		F31
1	-	-	-	-	TRIPLE 3-INPUT NAND GATE	SN7410N	E27
1	-	1	-	1	NOR GATE	CD4001A	E23,46,48
2	-	2	-	-	DUAL D FLIP FLOP	CD4013A	E21,22,40,47
1	-	1	-	-	EXCLUSIVE OR GATE	CD4070A	E20,39
-	1	-	-	1	ACIA	MC6850	E19,32
1	1	1	-	1	HEX BUFFER	SN7407N	E18,36
-	-	-	1	-	QUAD TRANSMITTER-RS232	MCI488N	E13
-	-	-	2	-	PHOTO COUPLER	4N33N	E11,E12
1	-	1	-	-	COUNTER	CD4018A	E10,33
1	-	-	-	2	QUAD 2-INPUT NOR GATE	SN7402N	E8,9,28
1	-	-	-	1	QUAD 2-INPUT AND GATE	SN7408N	E7,30
-	8	-	-	-	OPERATIONAL AMPLIFIER	LM741	E6,15,16,24-26,35,37
-	-	-	1	-	QUAD RECEIVER-RS232	MCI489	E5
1	2	1	-	-	VOLTAGE COMPARATOR	LM311N	E4,29,41,42
-	-	-	-	1	E PROM 256 X 8 BIT	MM1702A	E3
-	-	-	1	1	HEX INVERTER	SN7404N	E2,14
-	-	-	-	2	8-INPUT NAND GATE	SN7420N	E1,17
5	4	3	2	1	ASSEMBLY		

1=STANDARD  
2=SERIAL INTERFACE  
3=CAS 1  
4=MODEM  
5=CAS 2



## H GLOSSARY

### A.

#### ACCESS TIME

The time interval between the instant when a control unit or computer calls for a transfer of data to or from a storage device and the instant when this operation is completed.

#### ADDRESS

A name, numeral, or other reference designating a particular location in storage or some other data source or destination. The operand part of an instruction To call a specific piece of information from the memory or to put it into the memory.

#### ALGORITHM

A set of well-defined rules for solving a problem in a finite number of steps. A sequence of formulas to calculate a given task.

#### ALPHANUMERIC

Pertaining to a character set including both alphabetic characters (letters) and numeric characters (digits). Most alphanumeric character sets also contain special characters (commas, dollar signs, etc.).

#### APPLICATION PACKAGE

A routine or set of routines of a computer designed for a specific application (e.g., online savings accounting, inventory control, linear programming, etc.).

#### ASCII (American Standard Code for Information Interchange)

A 7-bit (or 8-bit compatible) USA standard code adopted to facilitate the interchange of data among various types of data communications and data processing equipment.

#### ASSEMBLER

A computer program that assembles programs that are written in symbolic coding to produce machine language programs.

### B.

#### BATCH PROCESSING

A technique in which items to be processed are collected into groups (batched) to permit processing. This technique is used to optimize machine usage efficiency as apposed to the user's efficiency.

#### BAUD

A unit of signaling speed equal to the number of discrete signals per second.

#### BAUDOT CODE

A 5-bit code used in telegraphy, consisting of a start impulse and five character impulses. This code has been used for more than 100 years and still widely used in data communications and punched tape.

H GLOSSARY cont'd

BCD (Binary Coded Decimal)

Pertaining to a system of representing each of the decimal digits zero through 9 by a distinct group of binary digits. For example, in the "8-4-2-1" BCD notation, which is used in many digital computers, the decimal number 39 is represented as 0011 1001 (Whereas in pure binary notation it would be represented as 100111).

BINARY

Pertaining to a numbering system with a radix of 2, or to a property or a characteristic involving a condition or choice in which there are two possibilities. For example, the binary numeral 1101 means:

$$(1 \times 2^3) + (1 \times 2^2) + (0 \times 2^1) + (1 \times 2^0)$$

which is equivalent to decimal 13.

BIT

A binary digit; a digit (0 or 1) representing a number in binary notation.

BRANCH

(1) Same as conditional transfer. (2) A machine instruction that is executed between two successive conditional transfer instructions.

BREAKPOINT

A specified point in a program where the program may be interrupted by a monitor routine or by manual intervention.

BUFFER

A storage device used to compensate for the differences in rates of flow of data or in the times of occurrence of events when transmitting data from one device to another. A buffer holding the characters to print one line is associated with most line printers to compensate for the difference between the high speed at which the computer transmits data to the printer and the low speed of the printing operation itself.

BUG

Any mechanical, electrical or electronic mistake in the design of a program or a computer system.

BYTE

A group of adjacent bits operated on as a unit and usually shorter than a word. In several important current computer systems, this term stands specifically for a group of eight adjacent bits that can represent one alphanumeric character or two hexadecimal digits.

C.

CALL

In computer programming, a branching or transfer of control to a subroutine, usually by supplying the required parameters and executing a jump to the entry point of the subroutine.

CALLING SEQUENCE

A basic set of instructions and data necessary to call a given subroutine.

CATHODE RAY TUBE

An electronic vacuum tube containing a screen on which information can be stored or displayed. The abbreviation CRT is often used.

CENTRAL PROCESSOR

The unit of a computer system that includes the circuits which control and perform the interpretation and execution of instructions. Synonymous with CPU (central processing unit) and main frame.

CLOCK

(1) A time-keeping device within a computer system that generates the basic periodic signal used to control the timing of all operations.

(2) A device that records the progress of realtime, or some approximation of it, and whose contents are available to a computer program; the clock may also be capable of initiating a program interrupt when a specified period of time has elapsed.

COBOL (Common Business Oriented Language)

A procedure-oriented language designed to facilitate the preparation and interchange of programs which form business data processing functions. Every COBOL Source program has four divisions, whose names and functions are as follows: (1) Identification Division, identifying the source program and the output of a compilation, (2) Environment Division, which specifies aspects of a data processing problem that are dependent upon the physical characteristics of a particular computer, (3) Data Division, describing the data that the object program is to accept as input, create, manipulate, or produce as output, and (4) Procedure Division, which specifies the procedures to be performed by the object program, by means of English-like statements.

CODING

The act of preparing in code an ordered list or lists of the successive instructions which will cause a computer to perform a particular process. See also absolute coding and symbolic coding.

COMPILE

To prepare a machine language program, or a program expressed in symbolic coding from a program written in another programming language (usually a procedure-oriented language such as COBOL or FORTRAN). This process usually involves examining and making use of the overall structure of the program and/or generating more than one object program instruction for each source program statement. A computer program more powerful than an assembler. Contrast with assemble and generate.

COMPILER

A computer program that compiles and is more powerful than an assembler. It can replace certain items of input with series of instructions. Compilers permit the use of procedure-oriented languages which greatly reduces the human effort required to prepare computer programs.

H GLOSSARY cont'd

CONDITIONAL TRANSFER

An instruction that may or may not cause a jump or skip to another preset instruction from the normal sequence of executing instructions. This depends upon the result of some operation, the contents of some register, or the setting of some indicator. Contrast with unconditional transfer.

CONSOLE

A portion of a computer where the control keys and certain special devices are located. It is used for communication between operators and the computer, usually by means of displays and manual controls.

CONVERSATIONAL MODE

A mode of operation that communicates between a computer and its user, in which the computer program examines the input supplied by the user and formulates comments or questions which are directed back to the user.

CPU (Central Processing Unit)

The central processor of a computing system containing the main storage, arithmetic unit, and special register groups.

CRT

Cathode ray tube display device. An electronic vacuum tube containing a screen on which information may be stored.

CYCLE TIME

The minimum time interval between the call for, and the delivery of information from a storage unit or device.

D.

DATA BASE

Data items or information on which operations and conclusions can be based. This set of data is internally accessible to the computer and on which the computer performs.

DEBUG

To locate and eliminate mistakes in a computer program or faults in equipment. If program does not work properly, the mistakes must be traced to their source and corrected.

DEMODULATOR

A device that receives signals from a transmission circuit and converts them into electrical pulses, or bits, that can serve as inputs to a data processing machine.

DIAGNOSTIC ROUTINE

A routine designed to locate a malfunction in a computer, also to aid in locating mistakes in a computer program.

DIGITAL COMPUTER

A computer that operates by using numbers to depict all the quantities and variables of problems.

DUMP

By accident or intention to withdraw all power from a computer. To record the contents of a set of storage locations at a given instant of time, aiding in detecting program mistakes. To transfer part or all of the contents of one section of computer memory into another section.

E.

EBCDIC (Extended Binary Coded Decimal Interchange Code)

An 8-bit code that represents 256 numbers, special characters and unique letters, and is the principal code used in many of the current computers.

EDIT

To modify the form or format of data. May involve the rearrangement of data, the addition of pertinent data, the deletion of unwanted data, code translation, and the controls of layouts for printing.

EFFECTIVE ADDRESS

The address derived by performing any specified address modification operations (e.g., indexing) upon a specified address (called the presumptive address) and that is actually used to identify the current operand.

F.

FILE

A collection of related informational records similar to one another in purpose, form, and content, usually arranged in sequence according to a key contained in each record. A record is a collection of related items; an item is an arbitrary quantity of data that is treated as a unit. In payroll processing, an employee's pay rate is an item; a group of items relating to one employee is a record, and the complete set of employee records is a file.

FIXED-LENGTH RECORD

A record containing the same number of characters. The restriction may be deliberate, in order to simplify and speed processing, or it may be dictated by the characteristics of the equipment used. Contrast with variable-length record.

FIXED POINT

Pertaining to a number system in which all numerical quantities are expressed by a predetermined number of digits, and the point is implicitly located at some predetermined position. Contrast with floating point.

FLOATING POINT

Pertaining to a form of number system in which each number is represented by two sets of digits, of which the fixed-point part represents the significant digits and the exponent indicates the position of the radix point. The number represented is equal to the fixed-point part multiplied by the radix (base i.e., binary decimal) raised to the power of an exponent.

FLOWCHART

A diagram to represent, for a problem, by means of symbols and inter-connecting lines, the flow of data, procedures, documents, methods, equipment, machine instructions, etc.

.FORTRAN (FORmula TRANslator)

A programming system, including a procedure-oriented language which is designed to facilitate the preparation of computer programs that perform mathematical computations.

FULL DUPLEX

Pertaining to a two-in-one situation, where a channel provides simultaneous, independent transmission of data in both directions over a communications link. Synonymous with duplex. Contrast with half duplex and simplex.

H.

HALF DUPLEX

Pertaining to a system that permits electrical communications in only one direction at a time over a communications link. Contrast with full duplex and simplex.

HEXADECIMAL

Pertaining to the number system with a radix of 16, or to a characteristic or property which involves a choice or condition with 16 possibilities.

HIGH ORDER

Pertaining to the digit or digits of a number that have the greatest weight or significance; e.g., in the number 54166, the highest order digit is 5; the lowest order digit is 6. Contrast with low order.

I.

IMMEDIATE ADDRESS

An instruction whose address part contains, rather than its address, the value of an operand. Thus, an "immediate address" is not an address at all, but an operand as part of an instruction.

INDEX REGISTER

The contents of the index register can be added to or subtracted from an address prior to or during the execution of an instruction.

INITIALIZE

To establish the variable items of a process at initial values before the process is started; e.g., to set indicators, addresses, and counters to the appropriate starting value at prescribed points of a computer program.

INPUT/OUTPUT (I/O)

A general term for the techniques, media, and devices used to communicate with data processing equipment and for the data involved in such communications. Transmitting information from an external source to the computer or from the computer to an external source.

INSTRUCTION

A coded program step that specifies an operation to be performed by the computer, and usually, the value or locations of one or more of its operands.

INTEGRATED CIRCUIT

A complete, complex electronic circuit, capable of performing all of the functions of a conventional circuit. It contains many discrete transistors, diodes, capacitors, and/or resistors, whose component parts are fabricated and assembled in a single integrated process. If the resultant assembly is disassembled, it would be destroyed.

INTERFACE

A shared boundary between two systems, or between a computer and one of its peripheral devices.

INTERPRETIVE ROUTINE

A routine dealing with the execution of a program by translating each instruction of the source language into a sequence of machine instructions and immediately executing them before translating the next instruction. Each instruction must be translated every time it is to be executed.

INTERRUPT

A signal, condition, or event that causes an interruption in the normal flow of a system or routine; e.g., detection of incorrect parity, completion of an input or output operation, or an attempt to execute an illegal instruction or to write in a protected location. This is accomplished so that the flow can be resumed at a later date from that point.

K.

KEY

One or more characters associated with a particular item or record and utilized in identifying that item or record, especially in collating or sorting operations. The key may or may not be attached to the item or record it identifies.

L.

LABEL

A name attached to or written alongside the entity it identifies; e.g., a name written beside a statement on a coding sheet, or a key that is attached to the record or item it identifies.

LOADER

A service routine designed to read programs into internal storage to prepare for their execution.

LOOP

A series of instructions that can be executed repetitively, usually with modified data values or modified addresses. Each repetition is called a cycle. A cycle continues until a specified criterion is satisfied (e.g., until a counter reaches a predetermined value).

LOW ORDER

Pertaining to the digit or digits of a number that have the least weight or importance; e.g., in the number 42675 the low order digit is 5.

M.

MACHINE INSTRUCTION

An instruction that a computer can directly recognize and execute.

MACHINE LANGUAGE

A language that is used directly by a computer. A set of characters, signs or symbols and the rules for combining them, that conveys instructions or information which a computer can directly recognize and execute, and which will cause it to perform a particular process.

MACRO INSTRUCTION

An instruction written in a machine-oriented language. It has no equivalent operation in the computer and is replaced in the object program by a predetermined set of machine instructions. This instruction has the capability of generating more than one machine-language instruction.

MESSAGE SWITCHING

A technique within a data communications network of receiving a message from various sources at a switching center, storing it until the proper outgoing communications link is available, and the ultimate retransmission of each message.

MICROPROGRAMMING

The technique of operating the control unit of a computer in which each instruction, instead of being used to initiate control signals directly, starts the execution of a sequence of "micro instructions" at a more basic elementary operation level. The Micro instructions are usually stored in a special read-only storage unit.

MICROSECOND

One millionth of a second.

MILLISECOND

One thousandth of a second, abbreviated msec. or ms.

MNEMONIC

Pertaining to a technique used to assist the human memory.

MODEM (MODulator-DEModulator)

A device that converts data from a form which is compatible with a data-processing machine or system to form that is compatible with transmission facilities, and vice-versa.

MODULATOR

A device that receives electrical pulses, or bits, from a data processing machine and converts them into signals that are suitable for transmission over a communications link.



MULTIPLEX

The process of transmitting two or more messages simultaneously over a single channel or other transmission facility. This can be accomplished either by splitting the channel's frequency band into two or more narrower bands ("frequency-division multiplexing") or by interleaving the bits, characters, or words that make up the various messages ("time-division multiplexing").

MULTITASKING

A technical process for handling two or more independent programs simultaneously by overlapping or interleaving their execution. The overlapping or interleaving of the execution of the various programs is usually controlled by an operating system which attempts to optimize the overall performance of the computer system in accordance with the priority requirements of the various jobs.

N.

NANOSECOND

One billionth of a second, abbreviated nsec. or ns.

O.

OBJECT LANGUAGE

A machine-language that is an output from a translation process. Contrast with source language.

OBJECT PROGRAM

A program expressed in an object machine-language (e.g., a machine-language program that can be directly executed by a particular computer.)

OCTAL

Pertaining to the number system with a radix of 8 or to a characteristic or property involving a condition or choice in which there are eight possibilities.

OFFLINE (or OFF-LINE)

Descriptive of the equipment or devices that are not in direct communication with the central processor of a computer system.

ONLINE (or ON-LINE)

Descriptive of the equipment or devices that are in direct communication with the central processor of a computer system.

OPERAND

A unit of data upon which an operation is performed. An operand of a computer instruction may be an argument, a result, a parameter, or indication of the location of the next instruction.

OPERATING SYSTEM

An organized collection of procedures and routines for operating a computer. These procedures and routines will normally perform some or all of the following functions:

- (1) scheduling, initiating, loading, and supervising the execution of programs;
- (2) allocating storage, input/output units, and other facilities of the computer system;
- (3) initiating and controlling input/output operations;
- (4) handling restarts and errors;
- (5) coordinating communications between the computer system and the human operator;
- (6) maintaining a log of system operations, and
- (7) controlling operations in a multiprocessing, multiprogramming, or time-sharing mode.

OPERATION CODE

A code used to represent the specific operations to be performed by a computer.

OVERFLOW

In an arithmetic operation, the generation of a quantity beyond the capacity of the register or storage location which is to receive the result; information contained in an item of information which is more than a given amount.

P.

PARITY BIT

A bit (binary digit) added to a group of bits to make the sum of all the 1-bits in the group either always even or always odd. For example:

	Even parity			Odd parity		
Data bits	0	1	1	0	1	1
	0	1	0	0	1	0
	0	1	0	0	1	0
	0	1	1	0	1	1
	0	1	1	0	1	1
	1	1	0	1	1	0
Parity bit	1	0	1	0	1	0

PATCH

To correct a mistake or modify a program in a rough or expedient way by adding new sections of coding.

PERIPHERAL EQUIPMENT

The input/output units and secondary storage units used in combination or conjunction with the computer, but are not part of the computer itself.

PROGRAM

(1) A plan for automatically solving a problem. (2) To devise a plan for solving a problem. (3) A computer routine, i.e., a set of instructions of steps arranged in proper sequence telling the computer to perform a particular process. (4) To write a computer routine.

PROGRAMMER

A person who devises programs for a computer.

R.

RANDOM ACCESS

Pertaining to a storage device whose access time is not dependent on the location of the data to be accessed; thus, any item of data which is stored online can be accessed within a relatively short time (usually less than one second). The machine can proceed directly to the desired memory location, thus, no search is required.

READ-ONLY MEMORY

A storage device that stores data into which data cannot be written or altered by the computer with which it is used.

REALTIME (or REAL-TIME)

(1) Pertaining to the actual time during which a physical process, event, problem, or communication takes place. (2) Pertaining to fast-response online computer processing, which obtains data from an activity or a process, performs computations, and returns a response rapidly enough to direct, control, or influence the outcome of the activity or process. For example, realtime operation is essential in computers associated with process control systems, message switching systems, and reservation systems.

RECORD

A collection of items of data that are related.

REENTRANT

Pertaining to a routine that can be used by two or more independent programs at the same time, enabling interruption at any point by another user and then resumed from the interruption point. The reentrant routine cannot modify the contents of any of its own locations, and that any required temporary storage must be supplied along with each program using the reentrant routine.

REGISTER

A device capable of storing a specified amount of data, such as one or more computer word, and usually intended for some special purpose.

RELATIVE ADDRESS

An address (usually contained in an instruction) that is combined with a base address forming the absolute address of a particular storage location.

RELOCATABLE CODING

Coding existing in a form that permits it to be executed and loaded in any available region of a computer's internal storage.

REPORT PROGRAM GENERATOR (RPG)

A generator that is designed to construct programs that perform routine report-writing functions; e.g., to accept input data from magnetic tape or punched cards and produce printed reports, often with headings, subtotals, etc.

ROUTINE

A sequence of machine instructions causing a computer to perform a particular process.

S.

SERIAL

The internal handling of the elements of a word or message (e.g., the bits or characters) one after another. Contrast with parallel.

SOFTWARE

A collection of programs and routines associated with a computer (including assemblers, compilers, utility routines, and operating systems) professionally prepared to simplify the programming and operation of the computer. Contrast with hardware.

SOURCE LANGUAGE

A language that is used to specify computer processing; translated into object language by a compiler or an assembler. Contrast with object language.

SOURCE PROGRAM

A program written in other than machine language that must be translated into machine language before use (e.g., written in COBOL, FORTRAN, or symbolic coding for input to a compiler or assembler).

SPECIAL CHARACTER

A character that is neither a digit nor a letter; it may be a punctuation mark or a character that causes a particular operation to be performed.

STATEMENT

In computer programming, a generalized instruction or meaningful expression in a programming language.

SUBROUTINE

The sequence of machine instructions that complete the carefully defined function or program. A routine that can be part of another routine. An open subroutine is inserted directly into a program at each point where it is to be used. A closed subroutine is stored in one place and connected to the program by means of linkage at one or more points in the program.

SYMBOLIC ADDRESS

An address expressed in symbols for the convenience of the programmer, which must be translated into an absolute address (usually by an assembler) before it can be interpreted by a computer. For example, the storage location that holds an employee's net pay might be assigned the symbolic address NPAY.

SYMBOLIC CODING

Pertaining to a coding system that uses machine instructions with symbolic addresses. Contrast with absolute coding and relative coding.

SYSTEM

An arrangement or set of entities that forms, or is considered as, an organized whole.

SYSTEM ANALYSIS

The examination of a procedure, activity, method, technique or business to determine what needs to be done and how it can best be accomplished.

T.

THROUGHPUT

The total amount of productive work performed by a data processing system during a given period of time.

TIME SHARING

(1) The use of a given device by a number of other programs, devices, or human users, one at a time and in rapid succession. (2) A system or technique of furnishing computing services to many users simultaneously, providing rapid responses to each of the users.

TRACE ROUTINE

A diagnostic routine that is designed to check or demonstrate the operation of a program; its output usually includes some or all of the instructions in the program being checked and the immediate results of those instructions, arranged in the order in which the instructions are executed.

U.

UNCONDITIONAL TRANSFER

An instruction of basic importance that always causes a jump (i.e., a departure from the normal sequence of executing instructions). Contrast with conditional transfer.

UTILITY ROUTINE

A standard routine used to assist in the operation of a computer by performing some frequently required process such as merging, sorting, data transcription, report program generation, file maintenance, etc.

V.

VARIABLE-LENGTH RECORD

A record that may contain an unfixed number of characters. Contrast with fixed-length record.

W.

WORD

A set of bits or characters treated by the computer circuits as a unit and capable of being stored in one storage location.

WORD LENGTH

The number of bits that are in a word.

WORKING STORAGE

A storage section set aside by the programmer for use in the development of processing results, for temporarily storing results needed later in the program, for storing constants, etc.

## J MEMORY MAP

### J.1 ONE CARD COMPUTER

RAM	0000-0FFF
unused 1/2 PIA	F040-F041
TTYPIA	F042-F043
CPU ROM unused	FC00-FDFF
CPU ROM used	FE00-FFFF

#### J.1.1 EXTERNAL REFERENCES

PCVAL	0FF1-0FF2	Address open in DEBUG
XTMP	0FF3-0FF4	Index register temporary storage
XTMPDL	0FF5-0FF6	Index register save while in timing delay loop
SHDWR	0FF7-0FF8	Hardware interrupt vector
BRKADD	0FF9-0FFA	Address where breakpoint SWI is
BRKSAV	0FFB	Contents of what was where SWI is now
TTYPID	F042	Teletype data register
TTYPIC	F043	Teletype control register

#### J.1.2 ROUTINES

CASC	FE70
CNTRLO	FE68
CI	FF48
CO	FE7A
CRLF	FEA4
DSPA	FEAD
DSPX	FE96
GDIGIT	FF07
INPCHR	FEF2
INPNUM	FED2
MSGOUT	FE3C
PCOM	FE03
SPACE	FEBA

#### J.1.3 SETUP & INTERRUPT ADDRESSES

HWI	0FF7
SWI	FE34
NMI	FE1E
RESET	FE48

Stack pointer initialized to 0FF0

## J MEMORY MAP

### J.2 PDSV3N and PDSV3D in SPHERE 310, 320 & 330 COMPUTERS

RAM	0000-0FFF	310 & 320 systems
	0000-4FFF	330 systems
CRT/1	E000-E1FF	
KBD/1 in PDSV3D systems	F000-F001	(present with KBD/1 only)
unused 1/2 PIA	F002-F003	(present with KBD/1 only)
KBD/2 in PDSV3N systems	F040-F041	PIA on CPU board
unused 1/2 PIA	F042-F043	PIA on CPU board
Realtime clock reset	F044	
SIM/1 first interface	F050-F051	320 & 330 systems only
second interface	F060-F061	
SIM ROM	FB00-FBFF	320 & 330 systems only
CPU ROM	FC00-FFFF	

#### J.2.1 EXTERNAL REFERENCES

TMP	0000-0001	Temporary storage, DO NOT USE when using PDS routines
TMP1	0002-0003	Temp. storage, DO NOT USE when using PDS routines
ARB	0004-0005	Pseudo register (AR3=0004, AR2=0005)
ARA	0006-0007	Pseudo register (AR1=0006, AR0=0007)
DIGIT	0008	Temporary storage, DO NOT USE when using PDS
CSTATS	0009	Cassette status
OUTEND	000A-000B	End of output buffer
BUFADR	000C-000D	Start of I/O buffer
BUFEND	000E-000F	End of I/O buffer
unused	0010	
OUTBUF	0011-0012	Start of output buffer
unused	0013	
SRCADR	0014-0015	Source for byte move
DSRADR	0016-0017	Destination address for byte move
unused	0018-0019	
ENDMEM	001A-001B	Last contiguous memory location
CSRPTR	001C-001D	Pointer to cursor location
BUFPTR	001E-001F	Pointer to character being displayed
BUFFLO	0020-0021	Pointer to top of low buffer
BUFFHI	0022-0023	Pointer to bottom of high buffer
SCNPTR	0024-0025	Pointer to scan beginning
SRCASM	0026-0027	Beginning of assembler source code
DSTASM	0028-0029	Beginning of assembler object code
ONDVAL	002A-002B	Operand value
SYMVAL	002C-002D	Symbol value
BRKSAV	002E	Temporary storage for data displaced by SWI
unused	002F	
BRKADR	0030-0031	Address of breakpoint
EDIT	0032	Non-zero if EDITOR is running
BLKNAM	0033-0034	Name for cassette block
IOBUFF	0035-0036	Temporary output editing area
unused	0037	
ACIANO	0038-0039	Address of ACIA being used for serial I/O
NOPRNT	003A	Non zero to display SIM I/O on CRT
unused	003B	
BFRPTR	003C-003D	Start of serial I/O buffer
BFRSZE	003E-003F	End of serial I/O buffer



## J MEMORY MAP

### J.2 PDSV3N and PDSV3A in SPHERE 310, 320 & 330 COMPUTERS

#### J.2.1 EXTERNAL REFERENCES cont'd

SYMTBL	0040-00BF	Assembler symbol table	
unused	00C0-0103		
HWI vectored to	0104-0107		
NMI vectored to	0108-010B		
Stack address	01FF		
CRT buffer	E000-E1FF		
KBD data register	F040*	F000*	
control register	F041*	F001*	
1/2 spare PIA data reg.	F042*	F002*	
control register	F043*	F003*	
Realtime clock reset	F044		
SIM - ACIA DATA-CONTROL			
0	F050 F051		
1	F060 F061		
2	F052 F053		
3	F062 F063		
4	F054 F055		
5	F064 F065		
6	F056 F057		
7	F066 F067		
8	F058 F059		
9	F068 F069		
A	F05A F05B		
B	F06A F06B		
C	F05C F05D		
D	F06C F06D		
E	F05E F05F		
F	F06E F06F		

#### J.2.2 ROUTINES

ADD32	FCD5
ASCBIN	FF22
BINASC	FF64
CASIN	FB7E 320 & 330 systems only
CASOUT	FB62 320 & 330 systems only
CLEAR	FC3D
CRLF	FD14
DEBUG	FE64
DIVIDE	FFAF
EDITIN	FC75
EDITOR	FC67

- \* F000-F003 is the PIA on the KDB/1 module and is not present unless that board is present. If KBD/2 is used it plugs into the CPU board and uses the PIA on the CPU at addresses F040-F043. The PIA on the CPU is spare if KBD/1 is used. NOTE: On CPU/2 boards the CA1 PIA control line is not present on connector X4, but is used by the realtime clock to make the interrupt more selectable and is available only if the realtime clock is disconnected.

## J MEMORY MAP

### J.2 PDSV3N and PDSV3D in SPHERE 310, 320 & 330 COMPUTERS

#### J.2.2 ROUTINES cont'd

EDITRD	FC73
GETCHR	FC4A
HOME	FC37
INPCHR	FE71
INPNUM	FEE4
INTLZC	FB00 320 & 330 systems only
LFTJST	FCFD
MULT	FF93
OUTSTR	FD8E
PNTBYT	FF02
PUTCHR	FCBC
RDBLK	FB91 320 & 330 systems only
RDMOD	FB93 320 & 330 systems only
REEDIT	FC6F
SUB32	FCCB
TRNOFF	FBB0 320 & 330 systems only
TURNON	FB77 320 & 330 systems only
WRTBLK	FB2D 320 & 330 systems only
WRTMOD	FB2F 320 & 330 systems only

#### J.2.3 SETUP & INTERRUPT ADDRESSES

HWI	0104
SWI	FE4A
NMI	0108
RESET	FC00

Stack pointer initialized to 01FF

#### J.3 SDOS in SPHERE 340 SYSTEMS

RAM	0000-4FFF	
CRT/1	E000-E1FF	
KBD/1	F000-F001	(present on KBD/1 only)
unused 1/2 PIA on KBD/1	F002-F003	(present on KBD/1 only)
KBD/2	F040-F041	PIA on CPU board
unused 1/2 PIA on CPU	F042-F043	PIA on CPU board
Realtime clock reset	F044	
Disk interface	F080-F083 & F086-F087	on PIM board
unused 1/2 PIA	F084-F085	on PIM board
unused full PIA	F088-F08B	on PIM board
Printer interface	F08C-F08F	on PIM board
CPU ROM	FC00-FFFF	

#### J.3.1 EXTERNAL REFERENCES

A complete list is not currently available.

## J MEMORY MAP

### J.3 SDOS in SPHERE 340 SYSTEMS

#### J.3.2 ROUTINES

CHEX	FCFE
CI	FECA
CLEAR	FEAB
CO	FEE5
DEBUG	FEFA
INIT DISK	FC59
READ	FD1B
WRITE	FD8E

#### J.3.3 SETUP & INTERRUPT ADDRESSES

HWI	0002
SWI	FF06
NMI	0000
RESET	FFF2

Stack pointer initialized to the top of contiguous memory

COMMENT FORM

Your comments are our most valuable input. Please let us know your feelings on this manual and make specific comments. Limit comments and suggestions to this manual. Acknowledgements can not be made on an individual basis. Mail to:

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