SILICON LOGIC™

DATA BOOK 1989

UART

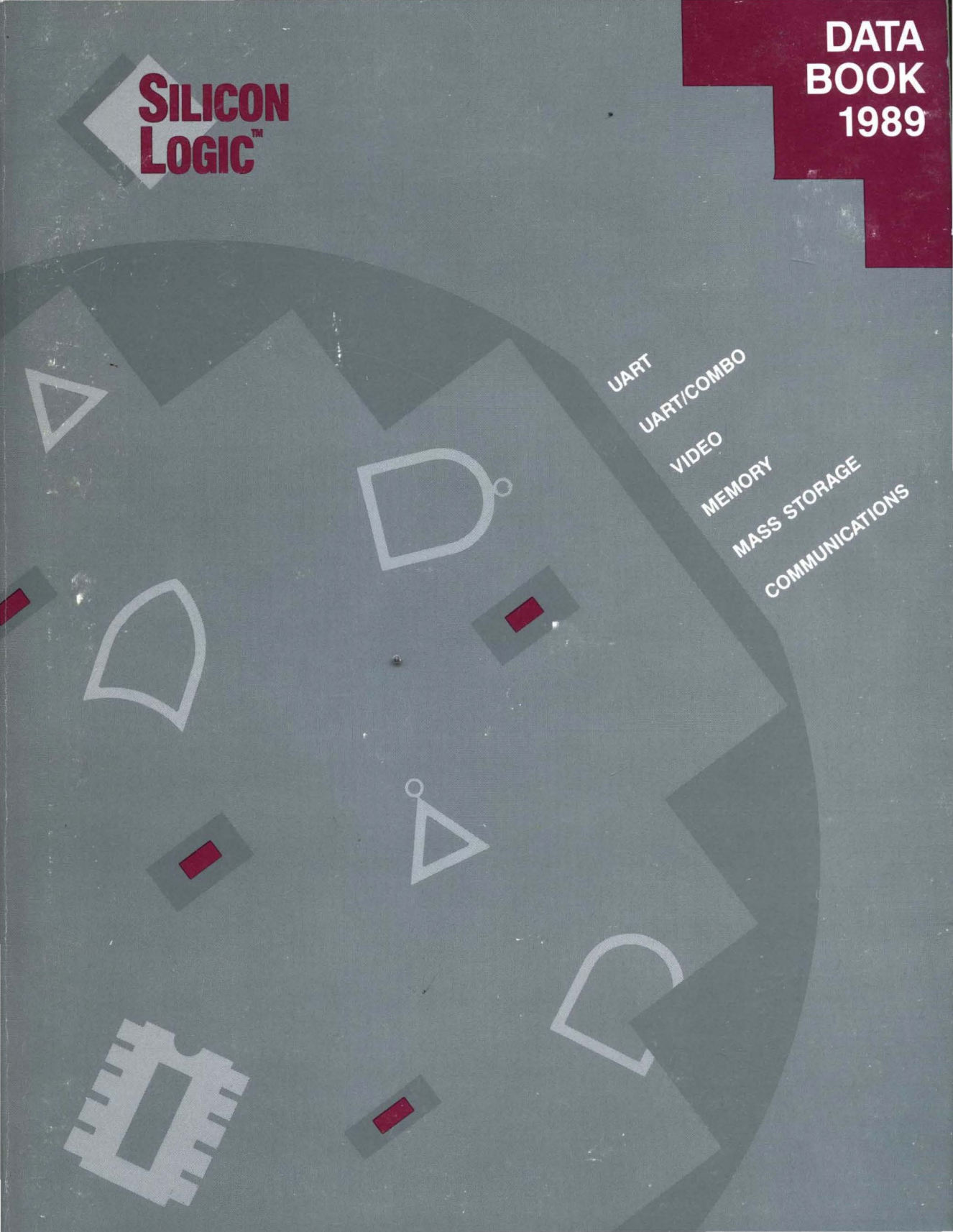
UART/COMBO

VIDEO

MEMORY

MASS STORAGE

COMMUNICATIONS



SILICON LOGIC

PRODUCT DATA BOOK 1989

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CONTENTS

SELECTION GUIDE/CROSS REFERENCE

Part Number	Short Description	Second Source Information	Packaging Information
LD805	Bidirectional Parallel (printer) Port	N/A	40 pin DIP 44 pin PLCC
LD806	Dual 74LS657 Transceiver	N/A	40 pin DIP 44 pin PLCC
LD1001 LD1002	EGA Chip Set	N/A N/A	68 pin PLCC 84 pin PLCC
LD1101	Universal Asynchronous Receiver and Transmitter	INS8250, INS8250B NS16C450 VL16C450 XR16C450 WD16C450	40 pin DIP 44 pin PLCC
LD1102	Dual LD1101	N/A	40 pin DIP 44 pin PLCC
LD1104	Video DAC with look Up Table	IMS G171 IMS G176 TRIAD 171 Bt 476	28 pin DIP 32 pin PLCC 44 pin PLCC
LD1107	Uart with Printer Port	VL16C451 WD 16C451	68 pin PLCC
LD1108	Duart with Printer Port	VI16C452 WD 16C452	68 pin PLCC
LD1201	Uart with FIFO	NS16C550 VL16C550	40 pin DIP 44 pin PLCC
LD1111	Hard Disk Controller	N/A	128 pin QFP

SILICON LOGIC HISTORY

Silicon Logic was founded in late 1982 primarily to design custom circuits. During the first four years of operation, CMOS and NMOS circuits were successfully designed and manufactured for Compaq, Microsoft, Western Digital, and Renaissance GRX Inc. In late 1987, Silicon logic was acquired by medium size US computer manufacturer. Silicon Logic operates as an independent subsidiary offering its products to the merchant IC market while having the financial stability of a major corporation.
Silicon Logic will work with independent consultants and circuit designers as well as OEMs to define common requirements so that VLSI circuit implementations can be realized in the shortest time.
Silicon Logic subcontracts its wafer fabrication to one of several US foundries depending on the volume of the specific circuit. Most of the circuits are designed using a 2 - 1½ micron, double-metal, CMOS that can be fabricated by multiple sources. Assembly is subcontracted to both on-shore and off shore sources depending on the specific situation.
Silicon Logic offers:

* Circuits having a combination of greater performance, lower power and more features into an existing footprint at a competitive price.

* Combine existing and next generation functions into new VLSI circuits.

* Develop new circuits rapidly by using advanced CAD tools and fast-turn wafer fabrication.

UART

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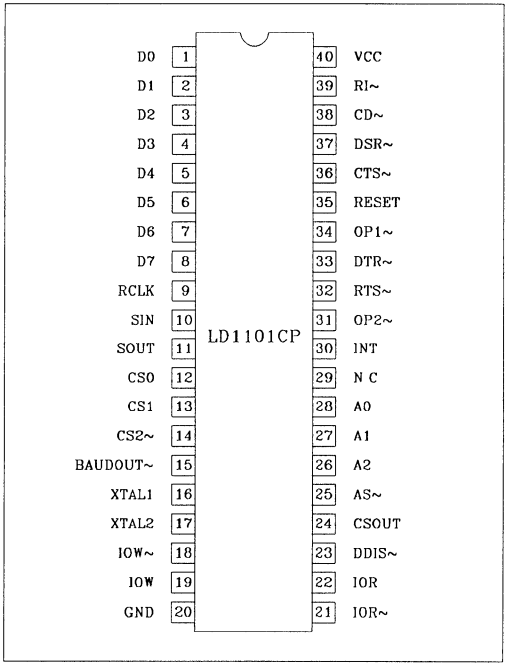
ASYNCHRONOUS RECEIVER AND TRANSMITTER

DESCRIPTION

The LD1101 is a universal asynchronous receiver and transmitter with modem control signals. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 56kHz. The LD1101 is fabricated in an advanced 2 u CMOS process to achieve low drain power and high speed requirements.



FEATURES

* Pin-to-pin and functionally compatible tolNS8250, NS16C450
* Modem control signals (CTS~, RTS~, DSR~, DTR~, RI~, CD~)
* Programmable character lengths (5, 6, 7, 8)
* Even, odd, or no parity bit generation and detection
* Status report register
* Independent transmit and receive control
* TTL compatible inputs, outputs

APPLICATIONS

* RS232 receiver or transmitter
* Serial to parallel/parallel to serial converter
* Modem handshaking

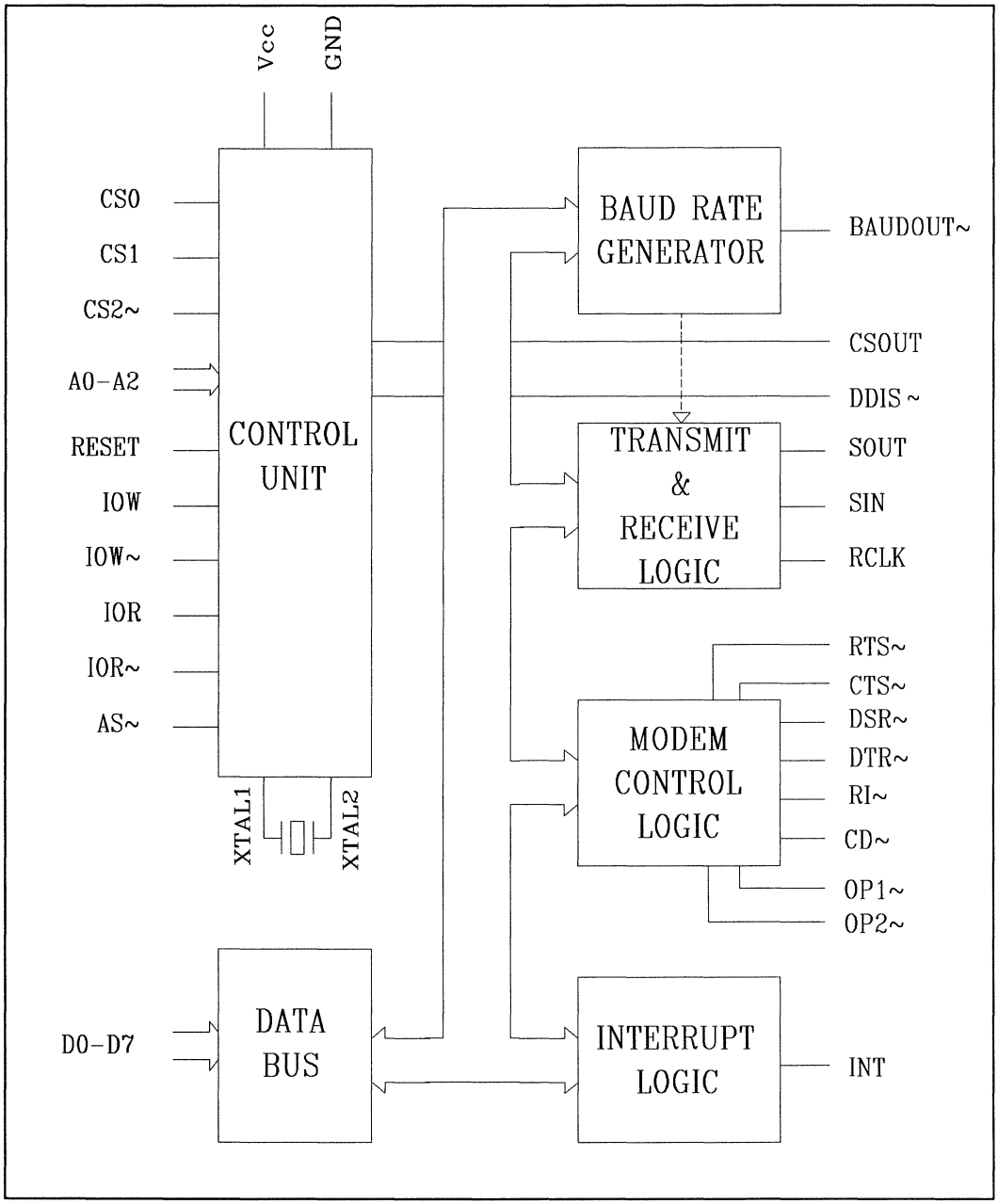
ORDERING INFORMATION

Part number	Package	Operating temperature
LD1101CP40	Plastic	0° C to +70° C
LD1101CJ44	PLCC	0° C to +70° C

GENERAL DESCRIPTION

The LD1101 is an improved version of the INS8250/ NS16C450 UART with higher speed operating access time. The LD1101 performs the parallel to serial/serial to parallel conversion on the data characters received from the CPU or the MODEM. The on board status register will provide the error conditions, type and status of the transfer operations being performed. Complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link. The LD1101 can interface easily to the most popular microprocessors and communications link faults can be detected with internal loopback capability.

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
D0-D7	1-8	I/O	Bidirectional data I/O. Eight bit, three state data bus to transfer information to or from the CPU . D0 is the least significant bit (lsb) of the data bus and the first serial data bit to be received or transmitted.
RCLK	9	I	Receive clock input. The external clock input to the LD1101 receiver section.
SIN	10	I	Serial data input. The serial information (data) received from MODEM or RS232 to LD1101 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the SIN input is disabled from external connection and connected to the SOUT output internally.
SOUT	11	O	Serial data output. The serial data is transmitted via this pin with additional start , stop and parity bits. The SOUT will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS0	12	I	Chip select 1. (active high) A high at this pin (while CS1 = h and CS2 = l) will enable the UART/CPU data transfer operation.
CS1	13	I	Chip select 2. (active high) A high at this pin (while CS0 = h and CS2 = l) will enable the UART/CPU data transfer operation.
CS2~	14	I	Chip select 3. (active low) A low at this pin (while CS0 = h and CS1 = h) will enable the UART / CPU data transfer operation.
BAUDOUT~	15	I	Baud rate generator clock output. This output provides the 16x clock of the internal selected baud rate.
XTAL1	16	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	17	I	Crystal input 2. See XTAL1.
IOW~	18	I	I/O write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOW	19	I	I/O write strobe. (active high) Same as IOW~, but uses active high input. Note that only an active IOW~ or IOW input is required to transfer data from CPU to LD1101 during write operation (while CS0 = h, CS1 = h and CS2~ = l). The unused pin should be tied to V_{CC} or GND(IOW = GND or IOW~ = V_{CC}) .
GND	20	O	Signal and power ground.

SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
IOR~	21	I	I/O read strobe. (active low) A low level on this pin (while CS0=h, CS1=h and CS2~=l) will transfer the contents of the LD1101 data bus to the CPU.
IOR	22	I	I/O read strobe. (active high) Same as IOR~, but uses active high input. Note that only an active IOR~ or IOR input is required to transfer data from LD1101 to CPU during read operation (while CS0=h, CS1=h and CS2~=l). The unused pin should be tied to V_{CC} or GND (IOR=GND or IOR~=V_{CC}).
DDIS~	23	O	Drive disable. (active low) This pin goes low when CPU is reading data from LD1101 to disable the external transceiver or logics.
CSOUT	24	O	Chip select out. A high on this pin indicates that the chip has been selected by the chip select input pins.
AS~	25	I	Address strobe. (active low) A low on this pin will latch the state of the chip selects and addressed register.
A2	26	I	Address line 2. To select internal registers.
A1	27	I	Address line 1. To select internal registers.
A0	28	I	Address line 0. To select internal registers.
INT	30	O	Interrupt output. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected.
OP2~	31	O	General purpose output. (active low) User defined output. See bit-3 modem control register.
RTS~	32	O	Request to send. (active low) To indicate the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to low state. After the reset this pin will be set to high.
DTR~	33	O	Data terminal ready. (active low) To indicate that LD1101 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR~ output to low. This pin will be set to high state after writing a "0" to that register or after the reset.
OP1~	34	O	General purpose output. (active low) User defined output. See bit-2 of modem control register.

SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
RESET	35	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS~	36	I	Clear to send. (active low) The CTS~ signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS~ has no effect on the transmitter output.
DSR~	37	I	Data set ready. (active low) A low on this pin indicates that MODEM is ready to exchange data with UART.
CD~	38	I	Carrier detect. (active low) A low on this pin indicates that a carrier has been detected by the modem.
RI~	39	I	Ring detect indicator. (active low) A low on this pin indicates that modem has received a ringing signal from telephone line.
V_{CC}	40	I	Power supply input.

PROGRAMMING TABLE

DLAB	A2	A1	A0	READ MODE	WRITE MODE
0	0	0	0	Receive Holding Register	Transmit Holding Register
0	0	0	1		Interrupt Enable Register
x	0	1	0	Interrupt Status Register	
x	0	1	1		Line Control Register
x	1	0	0		Modem Control Register
x	1	0	1	Line Status Register	
x	1	1	0	Modem Status Register	
x	1	1	1	Scratchpad Register	Scratchpad Register
1	0	0	0		LSB of Divisor Latch
1	0	0	1		MSB of Divisor Latch

REGISTER FUNCTIONAL DESCRIPTION

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register and Transmit Shift Register. The status of the transmit hold register is provided in the Line Status Register. Writing to this register will transfer the contents of data bus (D7-D0) to the transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transfered to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set. On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the SIN is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the SIN input. Receiver status codes will be posted in the Line Status Register.

LD1101 ACCESSIBLE REGISTERS

Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
ISR	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
MCR	0	0	0	loop back	OP2~	OP1~	RTS~	DTR~
LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
MSR	CD~	RI~	DSR~	CTS~	delta CD~	delta RI~	delta DSR~	delta CTS~
SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

INTERRUPT ENABLE REGISTER (IER)
The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0 = disable the receiver ready interrupt
1 = enable receiver ready interrupt

IER BIT-1:
0 = disable transmitter empty interrupt
1 = enable transmitter empty interrupt

IER BIT-2:
0 = disable receiver line status interrupt
1 = enable receiver line status interrupt

IER BIT-3:
0 = disable the modem status register interrupt
1 = enable the modem status register interrupt

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)
The LD1101 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the LD1101 provides the highest interrupt level to be serviced by CPU, no other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level	Source of the interrupts
1	ISR (Receiver Line Status Register)
2	RXRDY (Received Data Ready)
3	TXRDY (Transmitter Holding Register Empty)
4	MSR (Modem Status Register)

ISR BIT-0:
0 = an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1 = no interrupt pending

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to zero.

LINE CONTROL REGISTER (LCR)
The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.
00 = 5 bits word length
01 = 6 bits word length
10 = 7 bits word length
11 = 8 bits word length

LCR BIT-2:
The number of stop bits can be specified by this bit.
0 = 1 stop bit , when word length = 5, 6, 7, 8 bits
1 = 1 and 1/2 stop bit , when word length = 5 bits
1 = 2 stop bits, word length = 6, 7, 8 bits

LCR BIT-3:
Parity or no parity can be selected via this bit.
0 = no parity
1 = a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0 = odd parity is generated by calculating odd number of 1's in the transmitted data, receiver also checks for same format.
1 = an even parity bit is generated by calculating the number of even 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5 = 1 and LCR bit-4 = 0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5 = 1 and LCR bit-4 = 1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit.
1 = forces the transmitter output (SOUT) to go low to

alert the communication terminal
0=normal operating condition

LCR BIT-7:
The internal baud rate counter latch enable (DLAB)
0=normal operation
1=select divisor latch register

MODEM CONTROL REGISTER (MCR)
This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR~ output to high
1=force DTR~ output to low

MCR BIT-1:
0=force RTS~ output to high
1=force RTS~ output to low

MCR BIT-2:
0=set OP1 output to high
1=set OP1 output to low

MCR BIT -3:
0=set OP2~ output to high
1=set OP2~ output to low

MCR BIT -4:
0=normal operating mode
1=enable local loop-back mode (diagnostics). The transmitter output (SOUT) is set high (mark condition), the receiver input (SIN) , CTS~, DSR~, DCD~, and RI~ are disabled. Internally transmitter output is connected to the receiver input and DTR~, RTS~, OP1~, and OP2~ are connected to modem control inputs. In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)
This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1= data has been received and saved in the receive holding register

LSR BIT-1:
0=no overrun error (normal)
1=overrun error, next character arrived before receive holding register was empty

LSR BIT-2:
0=no parity error (normal)
1=parity error, received data does not have correct parity information

LSR BIT-3:
0=no framing error (normal)
1=framing error received, received data did not have a valid stop bit

LSR BIT-4:
0=no break condition (normal)
1=receiver received a break signal (SIN was low for one character time frame)

LSR BIT-5:
0=transmit holding register is full. LD1101 will not accept any data for transmission
1=transmit holding register is empty. CPU can load the next character

LSR BIT-6:
0=transmitter holding and shift registers are full
1=transmitter holding and shift registers are empty

LSR BIT-7:
Not used. Set to zero permanently.

MODEM STATUS REGISTER (MSR)
This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS~ input to the LD1101 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR~ input to the LD1101 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI~ input to the LD1101 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD~ input to the LD1101 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR. It is the compliment of the CTS~ input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR. It is the compliment of the DSR~ input.

MSR BIT-6:
This bit is equivalent to OP1 in the MCR. It is the compliment of the RI~ input.

MSR BIT-7:
This bit is equivalent to OP2 in the MCR. It is the compliment to the CD~ input.

SCRATCHPAD REGISTER (SR)
LD1101 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
150	768	
300	384	
600	192	
1200	96	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.86

LD1101 EXTERNAL RESET CONDITION TABLE

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals

SIGNALS	RESET STATE
SOUT	High
OP1~	High
OP2~	High
RTS~	High
DTR~	High
INT	BITS 0-3=low

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
T_1	Address strobe width	30			ns	
T_2	Address setup time	30			ns	
T_3	Address hold time	5			ns	
T_4	Chip select setup time	25			ns	
T_5	Chip select hold time	0			ns	
T_6	IOR~/IOR strobe width	75			ns	
T_7	Read cycle delay	50			ns	
T_8	Read cycle=$T_{20}+T_6+T_7$	135			ns	
T_9	IOR~/IOR to drive disable delay			35	ns	100 pF load
T_{10}	Delay from IOR~/IOR to data			75	ns	100 pF load
T_{11}	IOR~/IOR to floating data delay	0		50	ns	100 pF load
T_{12}	IOW~/IOW strobe width	50			ns	
T_{13}	Write cycle delay	55			ns	
T_{14}	Write cycle=$T_1+T_{12}+T_{13}$	135			ns	
T_{15}	Data setup time	10			ns	
T_{16}	Data hold time	25			ns	
T_{17}	Chip select output delay from select			50	ns	100 pF load
T_{18}	Address hold time from IOR~/IOR	0			ns	Note: 1
T_{19}	Chip select hold time from IOR~/IOR	0			ns	Note: 1
T_{20}	IOR~/IOR delay from address	10			ns	Note: 1
T_{21}	IOR~/IOR delay from chip select	10			ns	Note: 1
T_{22}	Address hold time from IOW~/IOW	5			ns	Note: 1
T_{23}	Chip select hold time from IOW~/IOW	5			ns	Note: 1
T_{24}	IOW~/IOW delay from address	25			ns	Note: 1
T_{25}	IOW~/IOW delay from select	10			ns	Note: 1
T_{26}	Reset pulse width	5			ns	
T_{27}	Clock high pulse duration	140				
T_{28}	Clock low pulse duration	140				External clock

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AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

TRANSMITTER						
T_{29}	Delay from rising edge of IOW~/IOW to reset interrupt			75	ns	100 pF load
T_{30}	Delay from initial INT reset to transmit start	24		40	*	
T_{31}	Delay from initial Write to interrupt	16		24	*	
T_{32}	Delay from stop to next start			100	ns	
T_{33}	Delay from start bit low to interrupt high			8	*	
T_{34}	Delay from IOR~/IOR to reset interrupt			75	ns	100 pF load
MODEM CONTROL						
T_{35}	Delay from IOW~/IOW to output			50	ns	100 pF load
T_{36}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{37}	Delay to reset interrupt from IOR~/IOR			70	ns	100 pF load
BAUD RATE GENERATOR						
N	Baud rate devisor	1		2^{16}-1		
T_{38}	Baud out negative edge delay			100	ns	100 pF load
T_{39}	Baud out positive edge delay			100	ns	100 pF load
T_{40}	Baud out down time	425			ns	100 pF load , Note: 2
T_{41}	Baud out up time	250			ns	100 pF load , Note: 2
RECEIVER						
T_{42}	Delay from RCLK to sample time			500	ns	
T_{43}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{44}	Delay from IOR~/IOR to reset interrupt			200	ns	100 pF load

Note 1: Applicable only when AS is tied low
Note 2: Fx=3.1 MHz clock
* Baudout~ cycle

ABSOLUTE MAXIMUM RATINGS

Operating supply range	5 Volts ± 5%
Voltage at any pin	GND-0.3 V to V_{CC}+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		V_{CC}	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		V_{CC}	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6 mA on all outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg power supply current			6	mA	
I_{IL}	Input leakage			±10	uA	
I_{CL}	Clock leakage			±10	uA	

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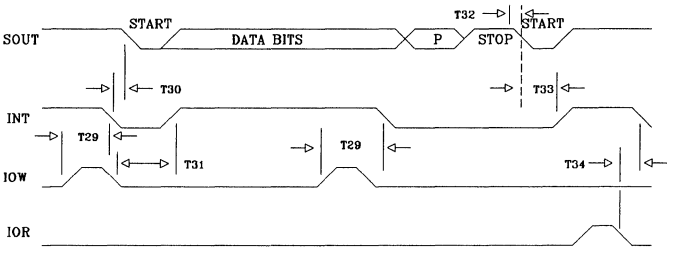
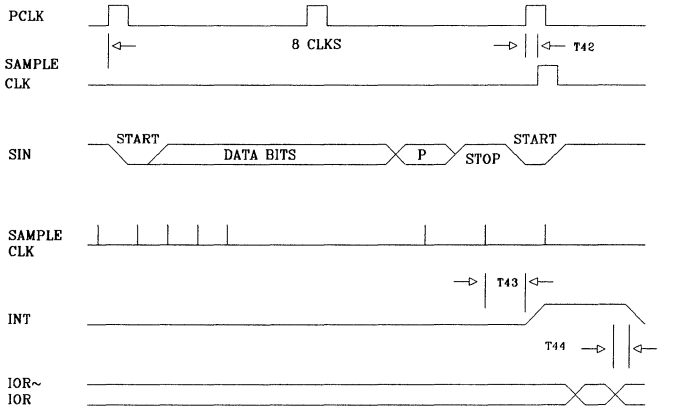
TIMING DIAGRAM

TRANSMITTER TIMING

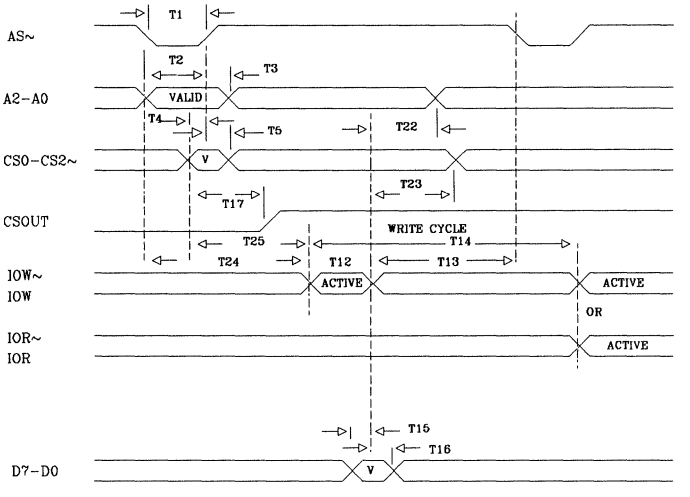


RECEIVER TIMING



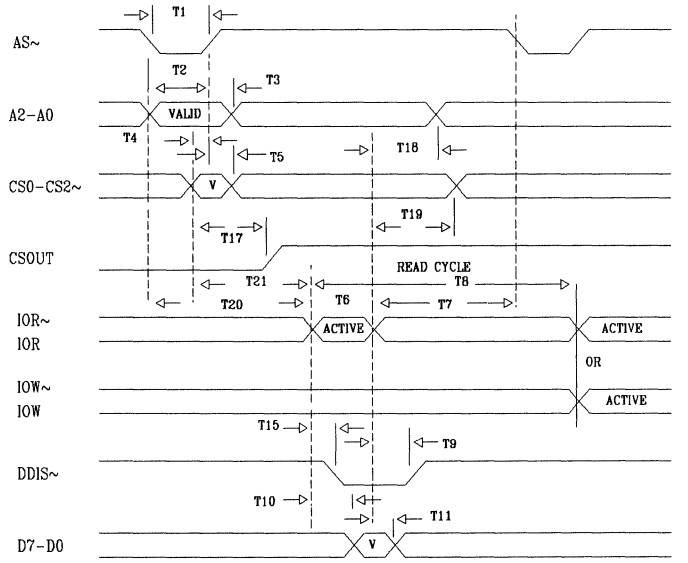
TIMING DIAGRAM

WRITE CYCLE TIMING



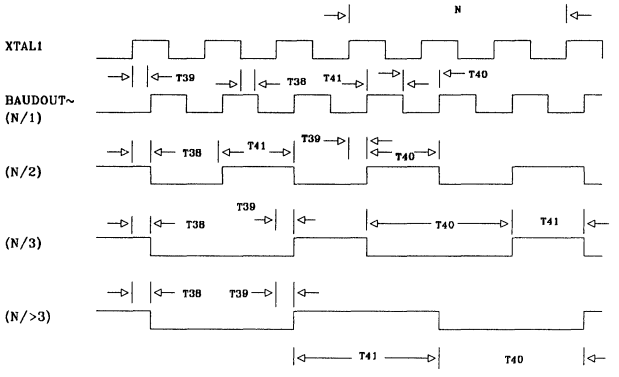
V = VALID
A = ACTIVE

READ CYCLE TIMING

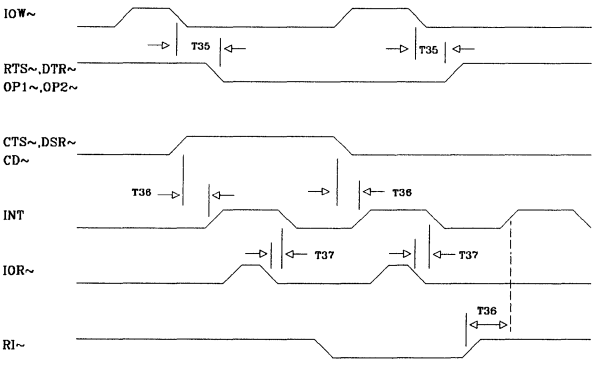


TIMING DIAGRAM

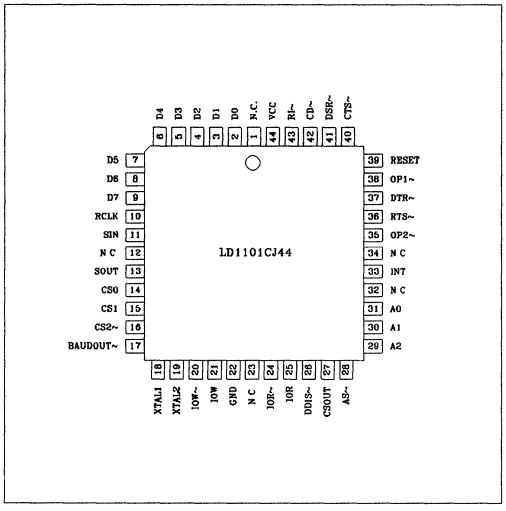
BAUDOUT~ TIMING



MODEM TIMING



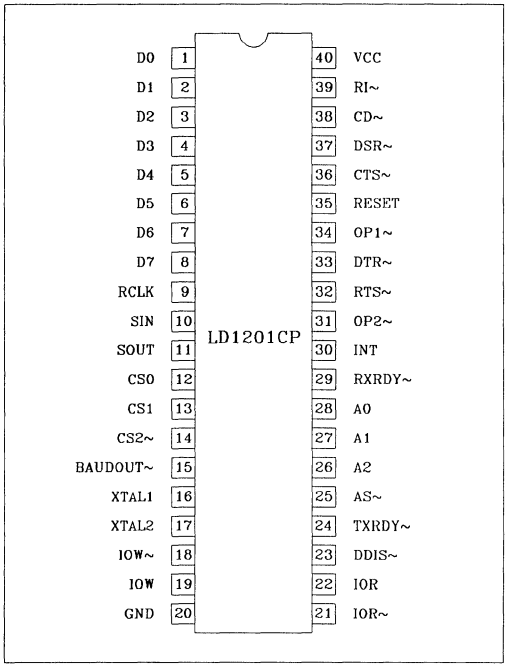
44-PIN PLCC INPUT



UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFOs

DESCRIPTION

The LD1201 is a universal asynchronous receiver and transmitter with FIFO and modem control signals. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 256KHz. The LD1201 is fabricated in an advanced 2 u CMOS process to achieve low drain power and high speed requirements.



FEATURES

*Pin to pin and functional compatible to NS16C550
*Modem control signals (CTS~, RTS~, DSR~, DTR~, RI~, CD~)
*16 byte programmable FIFO for transmit and receive section
*Programmable character lengths (5, 6, 7, 8)
*Even, odd, or no parity bit generation and detection
*Status report register
*Independent transmit and receive control
*TTL compatible inputs, outputs
*Software compatible with INS8250, NS16C450, LD1101

APPLICATIONS

* RS232 receiver or transmitter
* Serial to parallel/parallel to serial converter
* Modem handshaking
* IBM PS/2 serial port

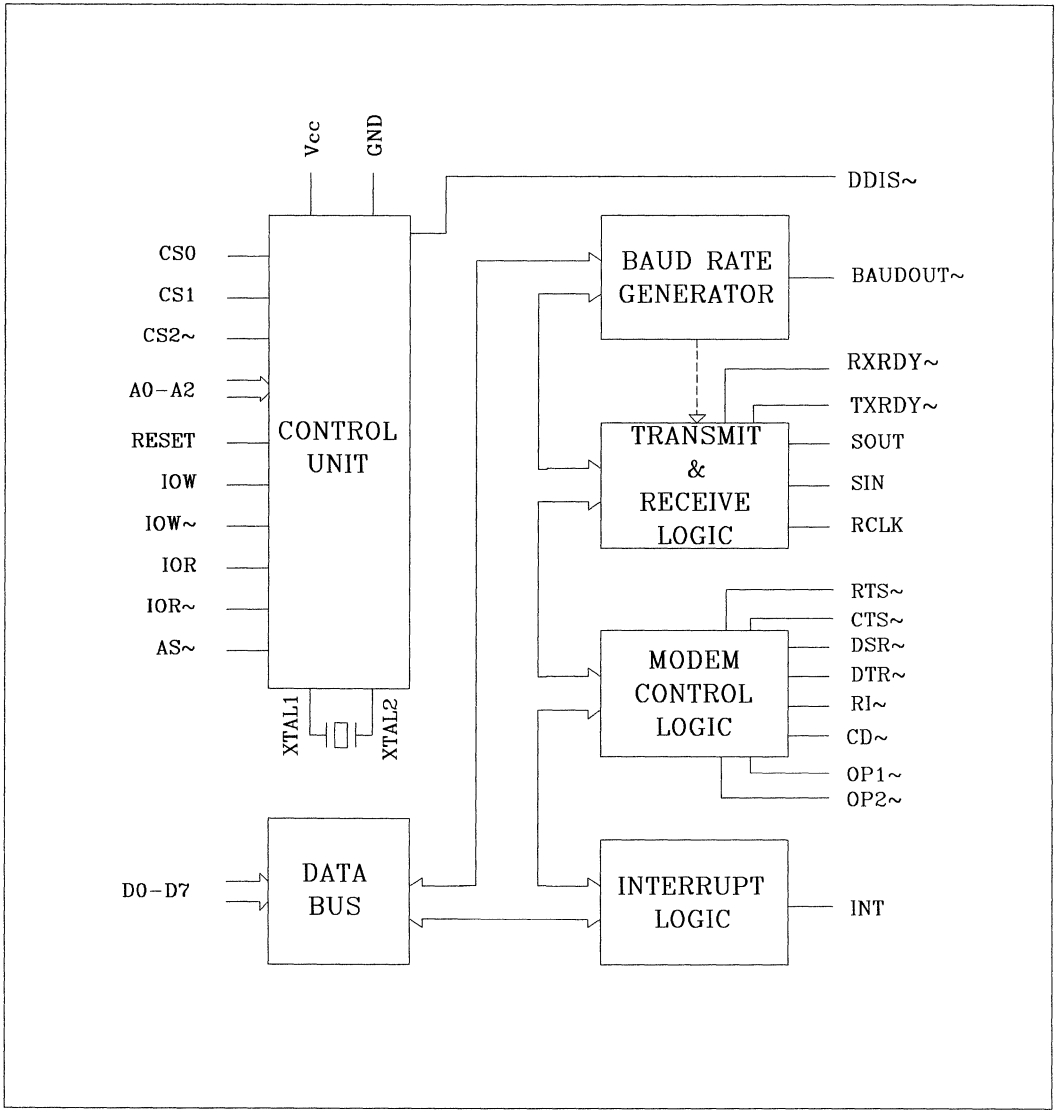
ORDERING INFORMATION

Part number	Package	Operating temperature
LD1201CP40	Plastic	0° C to + 70° C
LD1201CJ44	PLCC	0° C to + 70° C

GENERAL DESCRIPTION

The LD1201 is an improved version of the NS16C550 UART with higher operating speed and lower access time. The LD1201 performs the parallel to serial/serial to parallel conversion on the data characters received from the CPU or the MODEM. The on board status registers will provide the error conditions, type and status of the transfer operations being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link. On board 16 byte (plus 3 bits of error data per byte in the RX-FIFO) FIFO and two DMA signaling functions are designed to minimize system overhead and maximize system efficiency.The LD1201 provides internal loop-back capability for on board diagnostic testing.

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
D0-D7	1-8	I/O	Bidirectional data I/O. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit (lsb) of the data bus and the first serial data bit to be received or transmitted.
RCLK	9	I	Receive clock input. The external clock input to the LD1201 receiver section.
SIN	10	I	Serial data input. The serial information (data) received from MODEM or RS232 to LD1201 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the SIN input is disabled from external connection and connected to the SOUT output internally.
SOUT	11	O	Serial data output. The serial data is transmitted via this pin with additional start , stop and parity bits. The SOUT will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS0	12	I	Chip select 1. (active high) A high at this pin (while CS1 = h and CS2 = l) will enable the UART / CPU data transfer operation.
CS1	13	I	Chip select 2. (active high) A high at this pin (while CS0 = h and CS2 = l) will enable the UART / CPU data transfer operation.
CS2~	14	I	Chip select 3. (active low) A low at this pin (while CS0 = h and CS1 = h) will enable the UART / CPU data transfer operation.
BAUDOUT~	15	I	Baud rate generator clock output. This output provides the 16x clock of the internal selected baud rate.
XTAL1	16	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	17	I	Crystal input 2. See XTAL1.
IOW~	18	I	I/O write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOW	19	I	I/O write strobe. (active high) Same as IOW~, but uses active high input. Note that only an active IOW~ or IOW input is required to transfer data from CPU to LD1201 during write operation (while CS0 = h, CS1 = h and CS2~ = l). The unused pin should be tied to V_{CC} or GND(IOW = GND or IOW~ = V_{CC}) .

SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
GND	20	O	Signal and power ground.
IOR~	21	I	I/O read strobe. (active low) A low level on this pin (while CS0=h, CS1=h and CS2~=l) will transfer the contents of the LD1201 data bus to the CPU.
IOR	22	I	I/O read strobe. (active high) Same as IOR~, but uses active high input. Note that only an active IOR~ or IOR input is required to transfer data from LD1201 to CPU during read operation (while CS0=h, CS1=h and CS2~=l). The unused pin should be tied to V_{CC} or GND(IOR=GND or IOR~=V_{CC}) .
DDIS~	23	O	Drive disable. (active low) This pin goes low when the CPU is reading data from the LD1201 to disable the external transceiver or logics.
TXRDY~	24	O	Transmit ready. (active low) This pin goes low when the transmit FIFO of the LD1201 is full. It can be used as a single or multi-transfer DMA.
AS~	25	I	Address strobe. (active low) A low on this pin will latch the state of the chip selects and addressed register (A2-A0). This input is used when signals are not stable for the duration of a read or write operation. If not required, tie the AS~ input permanently low.
A2	26	I	Address line 2. To select internal registers.
A1	27	I	Address line 1. To select internal registers.
A0	28	I	Address line 0. To select internal registers.
RXRDY~	29	O	Receive ready. (active low) This pin goes low when the receive FIFO is full. It can be used as a single or multi-transfer DMA.
INT	30	O	Interrupt output. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
OP2~	31	O	General purpose output. (active low) User defined output. See bit-3 modem control register.
RTS~	32	O	Request to send. (active low) To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high.

SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
DTR~	33	O	Data terminal ready. (active low) To indicate that LD1201 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR~ output to low. This pin will be set to high state after writing a "0" to that register or after the reset .
OP1~	34	O	General purpose output. (active low) User defined output. See bit-2 of modem control register.
RESET	35	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS~	36	I	Clear to send. (active low) The CTS~ signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS~ has no effect on the transmitter output.
DSR~	37	I	Data set ready. (active low) A low on this pin indicates the MODEM is ready to exchange data with UART.
CD~	38	I	Carrier detect. (active low) A low on this pin indicates the carrier has been detected by the modem.
RI~	39	I	Ring detect indicator. (active low) A low on this pin indicates the modem has received a ringing signal from telephone line.
V_{CC}	40	I	Power supply input.

PROGRAMMING TABLE

DLAB	A2	A1	A0	READ MODE	WRITE MODE
0	0	0	0	Receive Holding Register	Transmit Holding Register
0	0	0	1		Interrupt Enable Register
x	0	1	0	Interrupt Status Register	FIFO Control Register
x	0	1	1		Line Control Register
x	1	0	0		Modem Control Register
x	1	0	1	Line Status Register	
x	1	1	0	Modem Status Register	
x	1	1	1	Scratchpad Register	Scratchpad Register
1	0	0	0		LSB of Divisor Latch
1	0	0	1		MSB of Divisor Latch

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transfered to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the SIN is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the SIN input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the LD1201 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

PROGRAMMABLE BAUD RATE GENERATOR

The LD1201 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-16 MHz and dividing it by any divisor from 2 to 2^{16}-1. The output frequency of the Baudout~ is equal to 16X of transmission baud rate (Baudout~ = 16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

$$\text{divisor value (decimal)} = \frac{\text{input frequency}}{\text{baud rate x 16}}$$

$$\text{EXAMPLE:} \quad \frac{1.8432 \times 10^6}{1200 \text{ (baud)} \times 16} = 96 \text{ (decimal)}$$

96 decimal = 0060 HEX Divisor MSB = 00
Divisor LSR = 60

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The LD1201 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the LD1201 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level	Source of the interrupts
1	ISR (Receiver Line Status Register)
2	RXRDY (Received Data Ready)
3	TXRDY(Transmitter Holding Register Empty)
4	MSR (Modem Status Register)

ISR BIT-0:
0 = an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1 = no interrupt pending.

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to zero.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signalling.

FCR BIT-0:
0 = Disable the transmit and receive FIFO.
1 = Enable the transmit and receive FIFO.

FCR BIT-1:
0 = No change.
1 = Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0 = No change.
1 = Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0 = No change.
1 = Changes RXRDY and TXRDY pins from mode "0" to mode "1".

FCR BIT 4-5:
Not used.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	World length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the SOUT is forced to low state).
0=normal operating condition.
1=forces the transmitter output (SOUT) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable(DLAB).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR~ output to high.
1=force DTR~ output to low.

MCR BIT-1:
0=force RTS~ output to high.
1=force RTS~ output to low.

MCR BIT-2:
0=set OP1~ output to high.
1=set OP1~ output to low.

MCR BIT-3:
0=set OP2~ output to high.
1=set OP2~ output to low.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (SOUT) is set high (Mark condition), the receiver input (SIN) , CTS~, DSR~, DCD~, and RI~ are disabled. Internally the transmitter output is connected to the receiver input and DTR~, RTS~, OP1~ and OP2~ are connected to modem control inputs. In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0 = no data in receive holding register or FIFO.
1 = data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:
0 = no overrun error (normal).
1 = overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:
0 = no parity error (normal).
1 = parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:
0 = no framing error (normal).
1 = framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
0 = no break condition (normal).
1 = receiver received a break signal (SIN was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:
0 = transmit holding register is full. LD1201 will not accept any data for transmission.
1 = transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:
0 = transmitter holding and shift registers are full.
1 = transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:
0 = Normal.
1 = at least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS~ input to the LD1201 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR~ input to the LD1201 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI~ input to the LD1201 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD~ input to the LD1201 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS~ input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR~ input.

MSR BIT-6:
This bit is equivalent to OP1 in the MCR during local loop-back mode. It is the compliment of the RI~ input.

MSR BIT-7:
This bit is equivalent to OP2 in the MCR during local loop-back mode. It is the compliment to the CD~ input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

LD1201 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.69
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.86

LD1201 EXTERNAL RESET CONDITION TABLE:

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0

SIGNALS	RESET STATE
SOUT	High
OP1~	High
OP2~	High
RTS~	High
DTR~	High
INT	BITS 0-3=low
RXRDY~	High
TXRDY~	High

LD1201 ACCESSIBLE REGISTERS

Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
ISR	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
MCR	0	0	0	loop back	OP2~	OP1~	RTS~	DTR~
LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
MSR	CD~	RI~	DSR~	CTS~	delta CD~	delta RI~	delta DSR~	delta CTS~
SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

AC ELECTRICAL CHARACTERISTICS

T_A=0° C to +70° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
T_1	Address strobe width	30			ns	
T_2	Address setup time	30			ns	
T_3	Address hold time	5			ns	
T_4	Chip select setup time	25			ns	
T_5	Chip select hold time	0			ns	
T_6	IOR~/IOR strobe width	75			ns	
T_7	Read cycle delay	50			ns	
T_8	Read cycle=T_{20}+T_6+T_7	135			ns	
T_9	IOR~/IOR to drive disable delay			35	ns	100 pF load
T_{10}	Delay from IOR~/IOR to data			75	ns	100 pF load
T_{11}	IOR~/IOR to floating data delay	0		50	ns	100 pF load
T_{12}	IOW~/IOW strobe width	50			ns	
T_{13}	Write cycle delay	55			ns	
T_{14}	Write cycle=T_1+T_{12}+T_{13}	135			ns	
T_{15}	Data setup time	10			ns	
T_{16}	Data hold time	25			ns	
T_{17}	Chip select output delay from select			50	ns	100 pF load
T_{18}	Address hold time from IOR~/IOR	0			ns	Note: 1
T_{19}	Chip select hold time from IOR~/IOR	0			ns	Note: 1
T_{20}	IOR~/IOR delay from address	10			ns	Note: 1
T_{21}	IOR~/IOR delay from chip select	10			ns	Note: 1
T_{22}	Address hold time from IOW~/IOW	5			ns	Note: 1
T_{23}	Chip select hold time from IOW~/IOW	5			ns	Note: 1
T_{24}	IOW~/IOW delay from address	25			ns	Note: 1
T_{25}	IOW~/IOW delay from select	10			ns	Note: 1
T_{26}	Reset pulse width	5			ns	
T_{27}	Clock high pulse duration	140				
T_{28}	Clock low pulse duration	140				External clock

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
TRANSMITTER						
T_{29}	Delay from rising edge of IOW~/IOW to reset interrupt			75	ns	100 pF load
T_{30}	Delay from initial INT reset to transmit start	24		40	*	
T_{31}	Delay from initial Write to interrupt	16		24	*	
T_{32}	Delay from stop to next start			100	ns	
T_{33}	Delay from start bit low to interrupt high			8	*	
T_{34}	Delay from IOR~/IOR to reset interrupt			75	ns	100 pF load
MODEM CONTROL						
T_{35}	Delay from IOW~/IOW to output			50	ns	100 pF load
T_{36}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{37}	Delay to reset interrupt from IOR~/IOR			70	ns	100 pF load
BAUD RATE GENERATOR						
N	Baud rate devisor	1		2^{16}-1		
T_{38}	Baud out negative edge delay			100	ns	100 pF load
T_{39}	Baud out positive edge delay			100	ns	100 pF load
T_{40}	Baud out down time	425			ns	100 pF load , Note: 2
T_{41}	Baud out up time	250			ns	100 pF load , Note: 2
RECEIVER						
T_{42}	Delay from RCLK to sample time			500	ns	
T_{43}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{44}	Delay from IOR~/IOR to reset interrupt			200	ns	100 pF load

ABSOLUTE MAXIMUM RATINGS

Operating Supply range	5 Volts ± 5%
Voltage at any pin	GND-0.3 V to V_{CC}+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

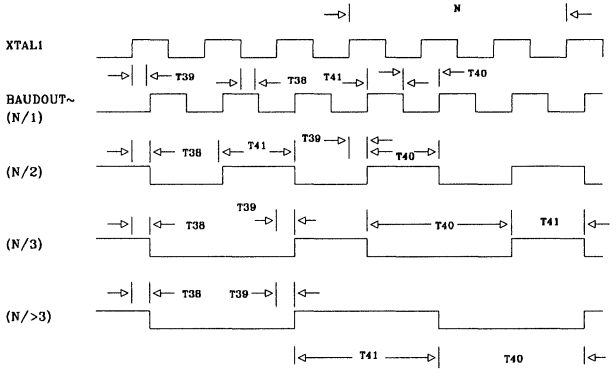
DC ELECTRICAL CHARACTERISTICS

T_A=0° C to +70° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

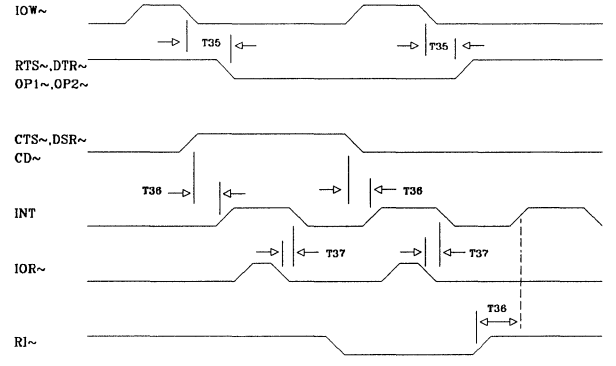
Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		V_{CC}	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		V_{CC}	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6 mA on all outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg power supply current			6	mA	
I_{IL}	Input leakage			±10	uA	
I_{CL}	Clock leakage			±10	uA	

Note 1: Applicable only when AS~ is tied low
Note 2: Fx=3.1 MHz clock
* Baudout~ cycle

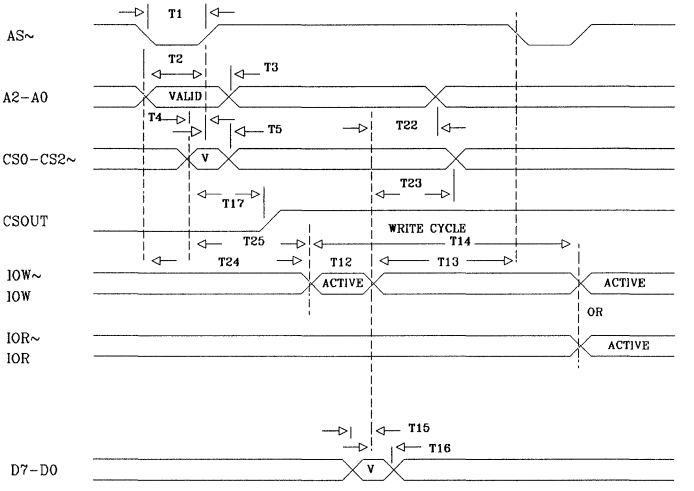
BAUDOUT~ TIMING



MODEM TIMING

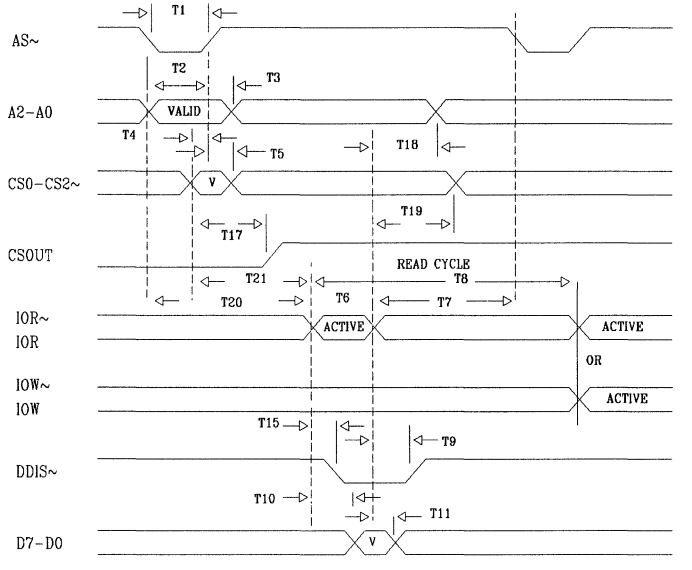


WRITE CYCLE TIMING

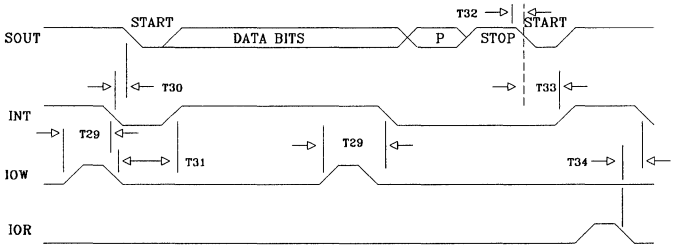


V = VALID
A = ACTIVE

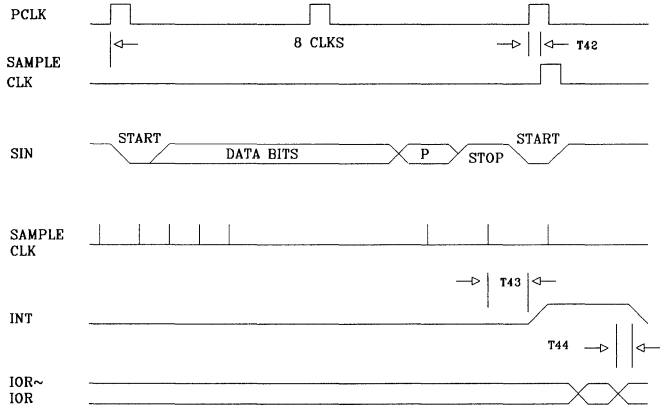
READ CYCLE TIMING



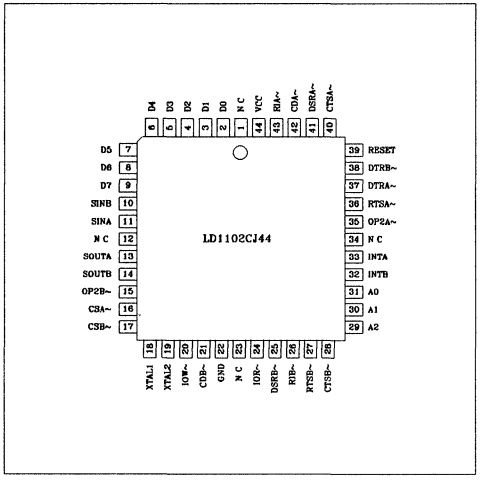
TRANSMITTER TIMING



RECEIVER TIMING



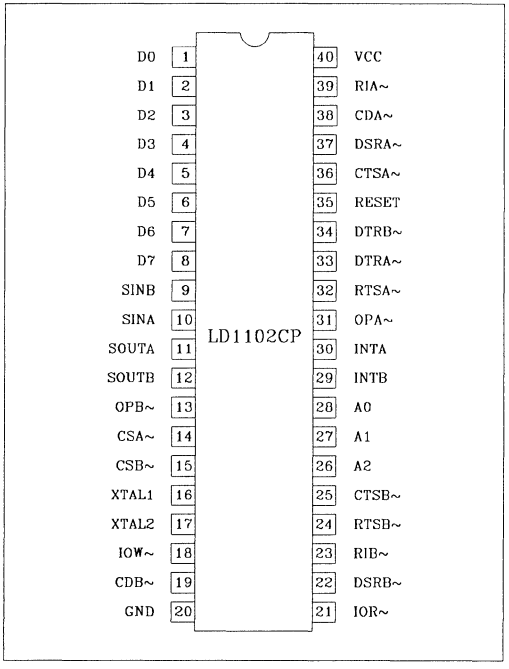
44 PIN PLCC PINOUT



DUAL ASYNCHRONOUS RECEIVER AND TRANSMITTER

DESCRIPTION

The LD1102 is a dual universal asynchronous receiver and transmitter with modem control signals. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 56KHz. The LD1102 is fabricated in an advanced 2 u CMOS process to achieve low drain power and high speed requirements.



FEATURES

* Dual LD1101
* Dual INS8250A, NS16C450
* Modem control signals (CTS~,RTS~, DSR~, DTR~, RI~, CD~)
* Programmable character lengths (5, 6, 7, 8)
* Even, odd, or no parity bit generation and detection
* Status report register
* Independent transmit and receive control
* TTL compatible inputs, outputs

APPLICATIONS

* Dual RS232 receiver and/or transmitter
* Serial to parallel / parallel to serial converter
* Modem handshaking

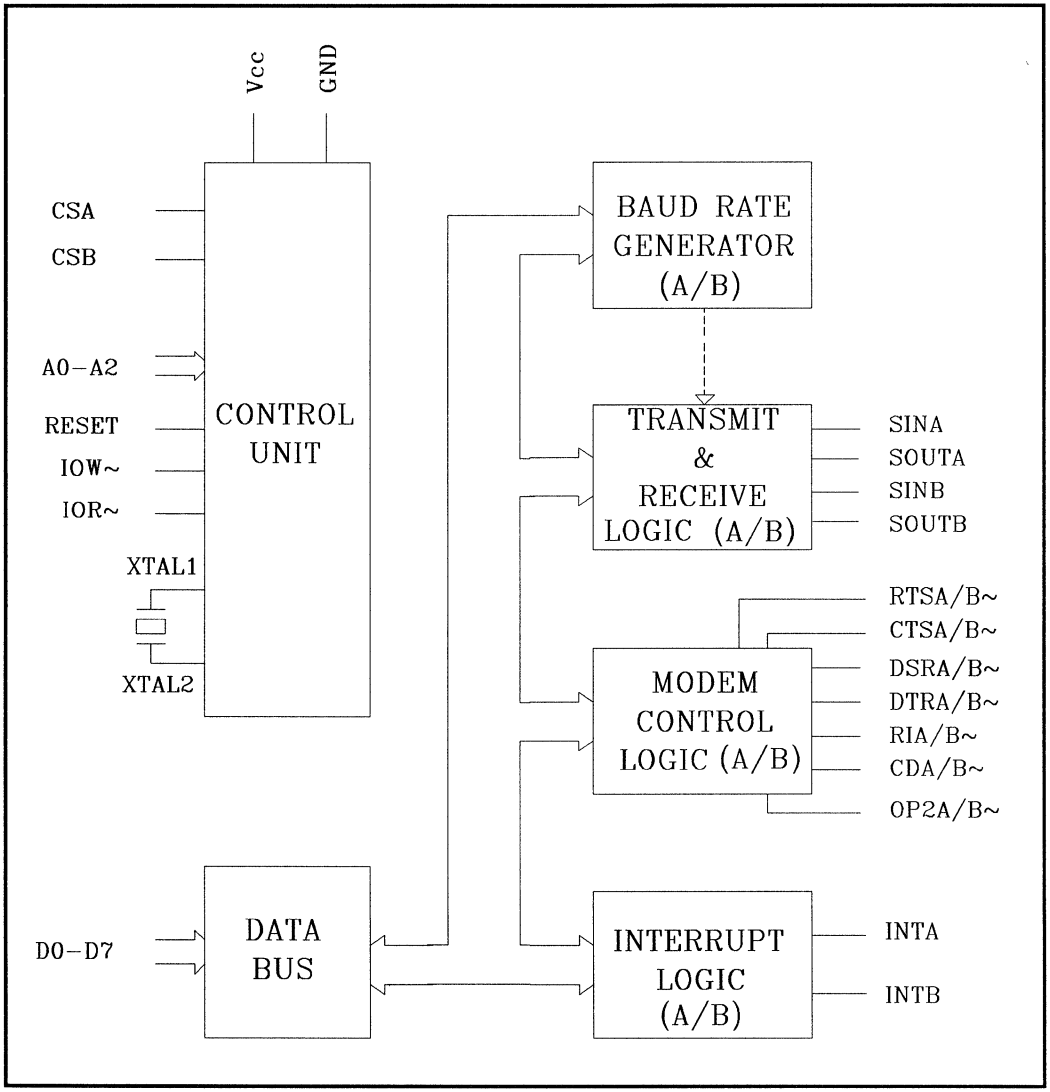
ORDERING INFORMATION

Part number	Package	Operating temperature
LD1102CP40	Plastic	0° C to +70° C
LD1102CJ44	PLCC	0° C to +70° C

GENERAL DESCRIPTION

The LD1102 is an improved, dual version of the INS8250/NS16C450 UART with higher speed operating access time. The LD1102 performs the parallel to serial/serial to parallel conversion on the data characters received from the CPU or the MODEM. The on board status registers will provide the error conditions, type and status of the transfer operations being performed. Complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link. The LD1102 can interface easily to the most popular microprocessors and communications link faults can be detected with internal loopback capability

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
D0-D7	1-8	I/O	Bidirectional data I/O. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit (lsb) of the data bus and the first serial data bit to be received or transmitted.
SINB	9	I	Serial data input B. The serial information (data) received from MODEM or RS232 to LD1102 receive B circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the SINB input is disabled from external connection and connected to the SOUTB output internally.
SINA	10	I	Serial data input A . The serial information (data) received from MODEM or RS232 to LD1102 receive A circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the SINA input is disabled from external connection and connected to the SOUTA output internally.
SOUTA	11	O	Serial data output A. The serial data of channel A is transmitted via this pin with additional start , stop and parity bits. The SOUTA will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
SOUTB	12	O	Serial data output B. The serial data of channel B is transmitted via this pin with additional start , stop and parity bits. The SOUTB will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
OP2B~	13	O	General purpose output. (active low) User defined output. See bit-3 modem control register B.
CSA~	14	I	Chip select A. (active low) A low at this pin will enable the UARTA/ CPU data transfer operation.
CSB~	15	I	Chip select B. (active low) A low at this pin will enable the UARTB/ CPU data transfer operation.
XTAL1	16	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	17	I	Crystal input 2. See XTAL1.
IOW~	18	I	I/O write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.

SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
CDB~	19	I	Carrier detect B. (active low) A low on this pin indicates that carrier has been detected by the modem B.
GND	20	O	Signal and power ground.
IOR~	21	I	I/O read strobe. (active low) A low level on this pin will transfer the contents of the LD1102 data bus to the CPU.
DSRB~	22	I	Data set ready B. (active low) A low on this pin indicates that MODEM is ready to exchange data with UART B
RIB~	23	I	Ring detect B indicator . (active low) A low on this pin indicates that modem has received a ringing signal from telephone line.
RTSB~	24	O	Request to send B. (active low) To indicate that transmitter B has data ready to send. Writing a "1" in the modem control register B (MCRB bit-1) will set this pin to low state. After the reset this pin will be set to high.
CTSB~	25	I	Clear to send B. (active low) The CTSB~ signal is a MODEM control function input whose conditions can be tested by reading the MSRB BIT-4. CTSB~ has no effect on the transmitter output.
A2	26	I	Address line 2. To select internal registers.
A1	27	I	Address line 1. To select internal registers.
A0	28	I	Address line 0. To select internal registers.
INTB	29	O	Interrupt output B. (active high) This pin goes high (when enabled by the interrupt enable register B) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected on UART B.
INTA	30	O	Interrupt output A. (active high) This pin goes high (when enabled by the interrupt enable register A) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected on UART A.
OP2A~	31	O	General purpose output A. (active low) User defined output. See bit-3 modem control register A.
RTSA~	32	O	Request to send A. (active low) To indicate that transmitter A has data ready to send. Writing a "1" in the modem control register A (MCRA bit-1) will set this pin to low state. After the reset this pin will be set to high.

SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
DTRA~	33	O	Data terminal ready A. (active low) To indicate that LD1102 (channel A) is ready to receive data. This pin can be controlled via the modem control register A (MCRA bit-0). Writing a "1" at the MCRA bit-0 will set the DTRA~ output to low. This pin will be set to high state after writing a "0" to that register or after the reset.
DTRB~	34	O	Data terminal ready B. (active low) To indicate that LD1102 (channel B) is ready to receive data. This pin can be controlled via modem control register B (MCRB bit-0). Writing a "1" at the MCRB bit-0 will set the DTRB~ output to low. This pin will be set to high state after writing a "0" to that register or after the reset .
RESET	35	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTSA~	36	I	Clear to send A. (active low) The CTSA~ signal is a MODEM control function input whose conditions can be tested by reading the MSRA BIT-4. CTSA~ has no effect on the transmitter output.
DSRA~	37	I	Data set ready A. (active low) A low on this pin indicates that MODEM is ready to exchange data with UART A.
CDA~	38	I	Carrier detect A. (active low) A low on this pin indicates that carrier has been detected by the modem A.
RIA~	39	I	Ring detect A indicator . (active low) A low on this pin indicates that modem has received a ringing signal from telephone line.
Vcc	40	I	Power supply input.

PROGRAMMING TABLE

CSB	CSA	DLAB	A2	A1	A0	READ MODE	WRITE MODE
1	0	0	0	0	0	Receive Holding Register A	Transmit Holding Register A
1	0	0	0	0	1		Interrupt Enable Register A
1	0	x	0	1	0	Interrupt Status Register A	
1	0	x	0	1	1		Line Control Register A
1	0	x	1	0	0		Modem Control Register A
1	0	x	1	0	1	Line Status Register A	
1	0	x	1	1	0	Modem Status Register A	
1	0	x	1	1	1	Scratchpad Register A	Scratchpad Register A
1	0	1	0	0	0		LSB of Divisor Latch A
1	0	1	0	0	1		MSB of Divisor Latch A
0	1	0	0	0	0	Receive Holding Register B	Transmit Holding Register B
0	1	0	0	0	1		Interrupt Enable Register B
0	1	x	0	1	0	Interrupt Status Register B	
0	1	x	0	1	1		Line Control Register B
0	1	x	1	0	0		Modem Control Register B
0	1	x	1	0	1	Line Status Register B	
0	1	x	1	1	0	Modem Status Register B	
0	1	x	1	1	1	Scratchpad Register B	Scratchpad Register B
0	1	1	0	0	0		LSB of Divisor Latch B
0	1	1	0	0	1		MSB of Divisor Latch B

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER A/B

The serial transmitter section consists of a Transmit Hold Register A/B and Transmit Shift Register A/B. The status of the transmit hold register is provided in the Line Status Register A/B. Writing to this register will transfer the contents of the data bus (D7-D0) to the transmit holding register A/B whenever the transmitter holding register A/B or transmitter shift register A/B is empty. The transmit holding register empty A/B flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register A/B. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the SINA/B is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the SINA/B input. Receiver status codes will be posted in the Line Status Register A/B.

INTERRUPT ENABLE REGISTER A/B

The Interrupt Enable Register A/B masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INTA/B output pin.

IER BIT-0:
0 = disable the receiver ready interrupt
1 = enable the receiver ready interrupt

IER BIT-1:
0 = disable transmitter empty interrupt
1 = enable transmitter empty interrupt

IER BIT-2:
0 = disable receiver line status interrupt
1 = enable receiver line status interrupt

IER BIT-3:
0 = disable the modem status register interrupt
1 = enable the modem status register interrupt

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER A/B
The LD1102 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register A/B provides the source of the interrupt in prioritized manner. During the read cycle, the LD1102 provides the highest interrupt level to be serviced by the CPU. No other interrupts are acknowledged until the particular interrupt has been serviced. The following are the prioritized interrupt levels:

Priority level	Source of the interrupts
1	ISR A/B (Receiver Line Status Register)
2	RXRDY A/B (Received Data Ready)
3	TXRDY A/B (Transmitter holding register empty)
4	MSR A/B (Modem Status Register)

ISR BIT-0:
0 = an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine
1 = no interrupt pending

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to zero.

LINE CONTROL REGISTER A/B
The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.
00 = 5 bits word length
01 = 6 bits word length
10 = 7 bits word length
11 = 8 bits word length

LCR BIT-2:
The number of stop bits can be specified by this bit.
0 = 1 stop bit , when word length = 5, 6, 7, 8 bits
1 = 1 and 1/2 stop bit , when word length = 5 bits
1 = 2 stop bits, word length = 6, 7, 8 bits

LCR BIT-3:
Parity or no parity can be selected via this bit.
0 = no parity
1 = a parity bit is generated during the transmission; receiver also checks for received parity

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0 = odd parity is generated by calculating odd number of 1's in the transmitted data; receiver also checks for same format.
1 = an even parity bit is generated by calculating the number of even 1's in the transmitted data; receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5 = 1 and LCR BIT-4 = 0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5 = 1 and LCR BIT-4 = 1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit.
1 = forces the transmitter output (SOUTA/B) to go low to alert the communication terminal
0 = normal operating condition

LCR BIT-7:
The internal baud rate counter latch enable (DLAB).
0 = normal operation
1 = select divisor latch register

MODEM CONTROL REGISTER A/B
This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0 = force DTR~ output to high
1 = force DTR~ output to low

MCR BIT-1:
0=force RTS~ output to high
1=force RTS~ output to low

MCR BIT-2:
x=not used

MCR BIT -3:
0=set OP2~ output to high
1=set OP2~ output to low

MCR BIT -4:
0=normal operating mode
1=enable local loop-back mode (diagnostics). The transmitter output (SOUTA/B) is set high (Mark condition), the Receiver inputs (SINA/B , CTSA/B~, DSRA/B~, CDA/B~, and RIA/B~) are disabled. Internally, the transmitter output is connected to the receiver input and DTRA/B~, RTSA/B~ and OP2A/B~ are connected to modem control inputs. In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupt sources are now the lower four bits of the Modem Control Register instead of the four Modem Control Inputs. The interrupts are still controlled by the IERA/B .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER A/B
This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=a data has been received and saved in the receive holding register

LSR BIT-1:
0=no overrun error (normal)
1=overrun error, next character arrived before receive holding register was empty

LSR BIT-2:
0=no parity error (normal)
1=parity error, received data does not have correct parity information

LSR BIT-3:
0=no framing error (normal)
1=framing error received, received data did not have a valid stop bit

LSR BIT-4:
0=no break condition (normal)
1=receiver received a break signal (SIN was low for one character time frame)

LSR BIT-5:
0=transmit holding register is full; LD1102 will not accept any data for transmission
1=transmit holding register is empty; CPU can load the next character

LSR BIT-6:
0=transmitter holding and shift registers are full
1=transmitter holding and shift registers are empty

LSR BIT-7:
Not used. Set to zero permanently.

MODEM STATUS REGISTER A/B
This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS~ input to the LD1102 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR~ input to the LD1102 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI~ input to the LD1102 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD~ input to the LD1102 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR. It is the compliment of the CTS~ input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR. It is the compliment of the DSR~ input.

MSR BIT-6:
This bit is equivalent to OP1 in the MCR. It is the compliment of the RI~ input.

MSR BIT-7:
This bit is equivalent to OP2 in the MCR. It is the compliment to the CD~ input.

SCRATCHPAD REGISTER A/B
LD1102 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
150	768	
300	384	
600	192	
1200	96	
1800	64	
3600	32	
4800	24	
7200	16	
9600	12	
19.2	6	
38.4K	3	
56K	2	2.86

LD1102 EXTERNAL RESET CONDITION TABLE:

REGISTERS	RESET STATE
IERA/B	IERA/B BITS 0-7=0
ISRA/B	ISRA/B BIT 0=1, ISRA/B BITS 1-7=0
LCRA/B	LCRA/B BITS 0-7=0
MCRA/B	MCRA/B BITS 0-7=0
LSRA/B	LSRA/B BITS 0-4=0, LSRA/B BITS 5-6=1, LSRA/B BIT 7=0
MSRA/B	MSRA/B BITS 0-3=0, MSRA/B BITS 4-7=input signals

SIGNALS	RESET STATE
SOUTA/B	High
OP2A/B~	High
RTSA/B~	High
DTRA/B~	High

LD1102 ACCESSIBLE REGISTERS

Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
ISR	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
MCR	0	0	0	loop back	OP2~	OP1~	RTS~	DTR~
LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
MSR	CD~	RI~	DSR~	CTS~	delta CD~	delta RI~	delta DSR~	delta CTS~
SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
T_6	IOR~ strobe width	75			ns	
T_8	Read cycle	135			ns	
T_{10}	Delay from IOR~ to data			75	ns	100 pF load
T_{11}	IOR~ to floating data delay	0		50	ns	100 pF load
T_{12}	IOW~ strobe width	50			ns	
T_{14}	Write cycle	135			ns	
T_{15}	Data setup time	10			ns	
T_{16}	Data hold time	25			ns	
T_{18}	Address hold time from IOR~	0			ns	
T_{19}	Chip select hold time from IOR~	0			ns	
T_{20}	IOR~ delay from address	10			ns	
T_{21}	IOR~ delay from chip select	10			ns	
T_{22}	Address hold time from IOW~	5			ns	
T_{23}	Chip select hold time from IOW~	5			ns	
T_{24}	IOW~delay from address	25			ns	
T_{25}	IOW~ delay from select	10			ns	
T_{26}	Reset pulse width	5			ns	
T_{27}	Clock high pulse duration	140				
T_{28}	Clock low pulse duration	140				External clock

* Baudout~ cycle

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
TRANSMITTER						
T_{29}	Delay from rising edge of IOW~ to reset interrupt			75	ns	100 pF load
T_{30}	Delay from initial INT reset to transmit start	24		40	*	
T_{31}	Delay from initial Write to interrupt	16		24	*	
T_{33}	Delay from start bit low to interrupt high			8	*	
T_{34}	Delay from IOR~ to reset interrupt		75	ns		100 pF load
MODEM CONTROL						
T_{35}	Delay from IOW~ to output		50	ns		100 pF load
T_{36}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{37}	Delay to reset interrupt from IOR~			70	ns	100 pF load
BAUD RATE GENERATOR						
N	Baud rate divisor	1		2^{16}-1		
RECEIVER						
T_{43}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{44}	Delay from IOR~ to reset interrupt			200	ns	100 pF load

1

ABSOLUTE MAXIMUM RATINGS

Operating supply range	5 Volts ± 5%
Voltage at any pin	GND-0.3 V to V_{CC}+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

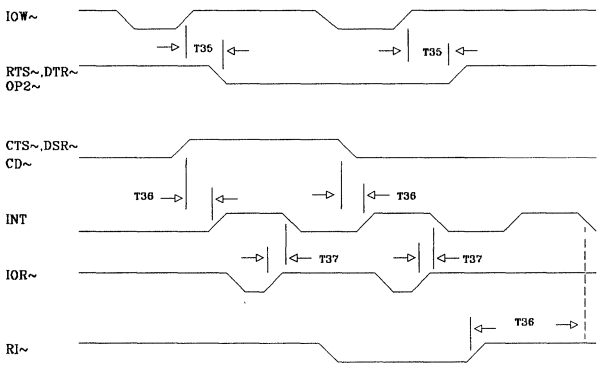
DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

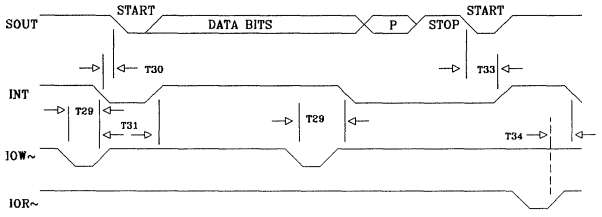
Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		V_{CC}	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		V_{CC}	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6 mA on all outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg power supply current			6	mA	
I_{IL}	Input leakage			±10	uA	
I_{CL}	Clock leakage			±10	uA	

TIMING DIAGRAM

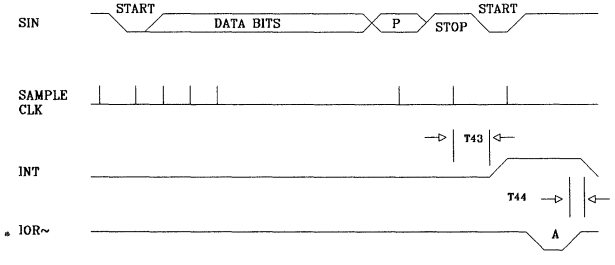
MODEM TIMING



TRANSMITTER TIMING



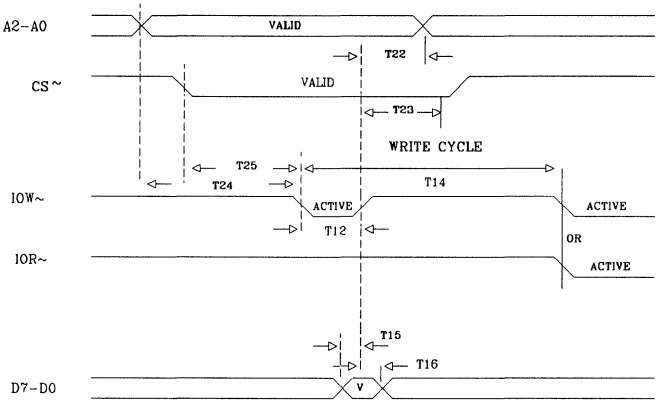
RECEIVER TIMING



1

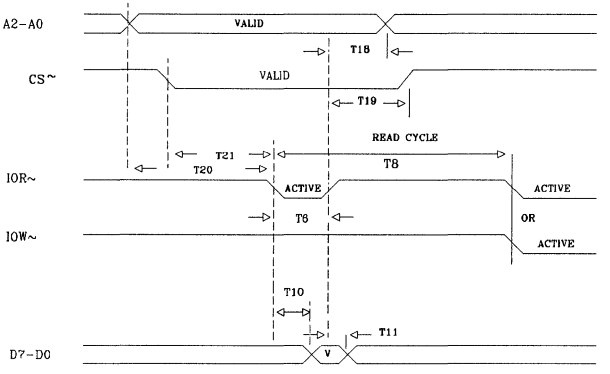
TIMING DIAGRAM

WRITE CYCLE TIMING



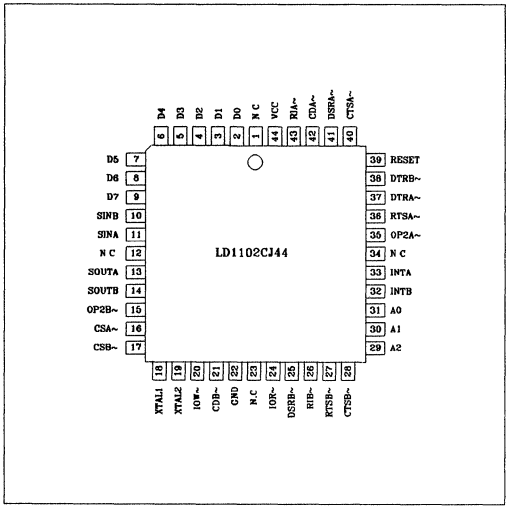
V = VALID
A = ACTIVE

READ CYCLE TIMING



V = VALID
A = ACTIVE

44 PIN PLCC PINOUT



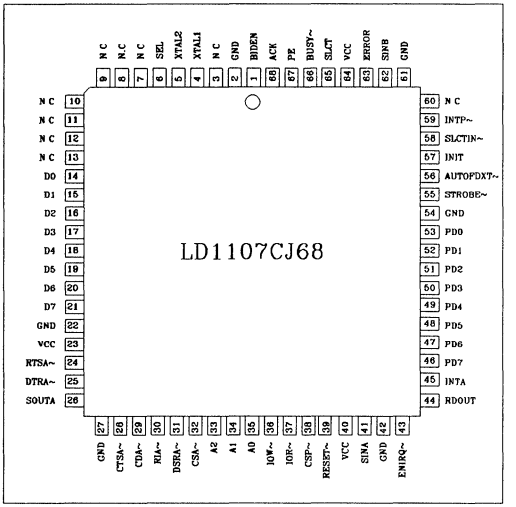
UART/COMBO

2

UNIVERSAL ASYNCHRONOUS RECEIVER AND TRANSMITTER WITH PARALLEL PRINTER PORT

DESCRIPTION

The LD1107 is a universal asynchronous receiver and transmitter with a bidirectional CENTRONICS type parallel printer port. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 56kHz. The LD1107 is fabricated in an advanced 2 u CMOS process to achieve low drain power and high speed requirements.



FEATURES

* Pin to pin and functionally compatible to VL16C451
* Bidirectional printer port
* Modem control signals (CTS~, RTS~, DSR~, DTR~, RI~, CD~)
* Programmable character lengths (5, 6, 7, 8)
* Even, odd, or no parity bit generation and detection
* Status report register
* Independent transmit and receive control
* TTL compatible inputs, outputs
* Fully compatible with all new bidirectional PS/2 printer port
* Direct replacement of logic for PC/XT/AT
* High data transfer rate

APPLICATIONS

* RS232 receiver or transmitter
* Serial to parallel / parallel to serial converter
* Modem hand-shaking
* CENTRONICS printer port
* IBM PS/2 bidirectional printer port
* External bidirectional I/O
* IBM PC/XT/AT upgrade printer port

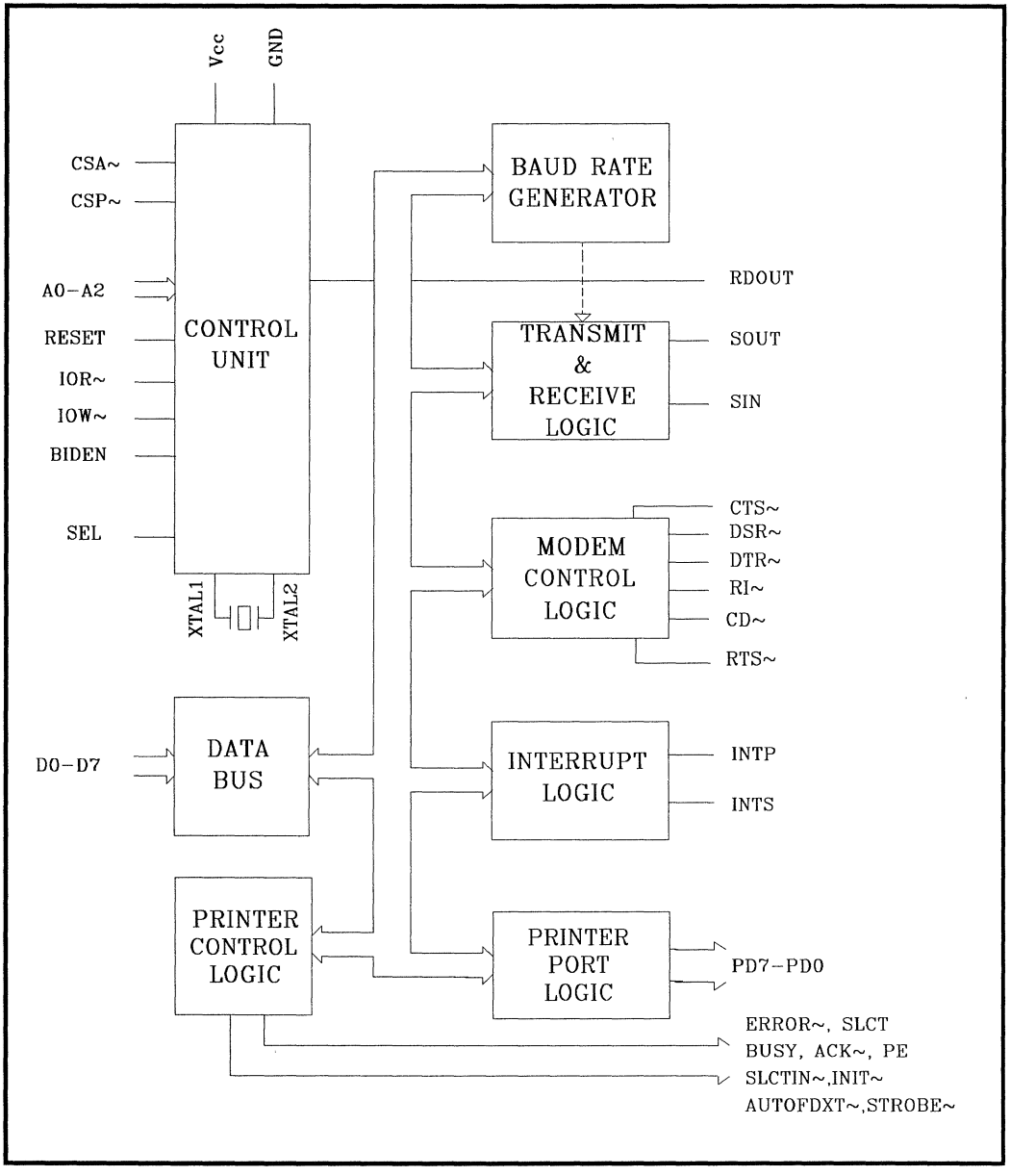
ORDERING INFORMATION

Part number	Package	Operating temperature
LD1107CJ68	PLCC	0° C to +70° C

GENERAL DESCRIPTION

The LD1107 is an improved version of the VL16C451 with higher speed operating access time. The LD1107 is the combined version of LD1101 and LD805 in a single monolithic form. The LD1107 performs the parallel to serial/serial to parallel conversion on the data characters received from the CPU or the MODEM. The LD1107 also provides the user with a fully bidirectional parallel data port that fully supports the parallel CENTRONICS type printer. The on board status registers will provide the error conditions, type and status of the transfer operations being performed. The LD1107 also has complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link. The LD1107 can interface easily to the most popular microprocessors and communications link faults can be detected with internal loopback capability.

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
BIDEN	1	I	I/O direction select. A high enables the software controlled mode (input/output). A low puts the parallel port in the output mode.
XTAL1	4	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock the internal circuit and the baud rate generator for custom transmission rates.
XTAL2	5	I	Crystal input 2. This pin should be tied to ground when the external clock is used.
SEL	6	I	Crystal or external clock select pin. To select external clock source to the LD1107 XTAL1 input, this pin should be tied to GND. On board crystal oscillator circuit can be activated by tying this pin to Vcc and connecting a crystal to XTAL1 and XTAL2 input pins.
D0-D7	14-21	I/O	Bidirectional data I/O. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit (lsb) of the data bus and the first serial data bit to be received or transmitted.
RTS~	24	O	Request to send. (active low) To indicate that transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to low state. After the reset this pin will be set to high.
DTR~	25	O	Data terminal ready. (active low) To indicate that LD1107 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR~ output to low. This pin will be set to high state after writing a "0" to that register or after the reset.
SOUT	26	O	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The SOUT will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CTS~	28	I	Clear to send. (active low) The CTS~ signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS~ has no effect on the transmitter output.
CD~	29	I	Carrier detect. (active low) A low on this pin indicates that carrier has been detected by the modem.

SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
RI~	30	I	Ring detect indicator. (active low) A low on this pin indicates that the modem has received a ringing signal from the telephone line.
DSR~	31	I	Data set ready. (active low) A low on this pin indicates that the MODEM is ready to exchange data with UART.
CSA~	32	I	Chip select A. (active low) A low at this pin (while CSP~=h) will enable the UART / CPU data transfer operation.
A2	33	I	Address line 2. To select internal registers.
A1	34	I	Address line 1. To select internal registers.
A0	35	I	Address line 0. To select internal registers.
IOW~	36	I	I/O write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR~	37	I	I/O read strobe. (active low) A low level on this pin will transfer the contents of the LD1107 data bus to the CPU.
CSP~	38	I	Chip select P. (active low) To enable the LD1107 printer operation, this pin has to go low while CSA~ is high.
RESET~	39	I	Master reset. (active low) A low on this pin will reset all the outputs and internal registers. The parallel port of the LD1107 will be set to output mode, the transmitter output and the receiver input will be disabled during reset time.
SIN	41	I	Serial data input. The serial information (data) received from MODEM or RS232 to LD1107 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the SIN input is disabled from external connection and connected to the SOUT output internally.
ENIRQ~	43	I	Interrupt source selection. (active low) The external ACK~ can be selected as an interrupt source by tying this pin to GND. Tying this pin to Vcc, will set the internal interrupt logic to the latched state, reading the STATUS register will reset the INTP output.
RDOUT	44	O	Read select out. A high on this pin indicates that the chip is being read by the CPU.
INTS	45	O	UART interrupt output. (three state) This pin goes high (when enabled by MCR BIT-3) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected.

SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
PD7-PD0	46-53	I/O	Bidirectional parallel I/O. (three state) To transfer data in or out of the LD1107 parallel port. PD7-PD0 are latched during output mode.
STROBE~	55	I/O	General purpose I/O or strobe output. (open drain active low) To transfer latched data to the external peripheral or printer.
AUTOFDXT~	56	I/O	General purpose I/O or line printer autofeed. (open drain active low) To signal the printer for continous form feed.
INIT~	57	I/O	General purpose I/O or line printer initialize. (open drain active low) To signal the line printer to enter internal initialization routine.
SLCTIN~	58	I/O	General purpose I/O or line printer select. (open drain active low) To select the line printer.
INTP~	59	O	Printer interrupt output. (active low) To signal the state of the printer port.
ERROR~	63	I	General purpose input or line printer error. (active low) This is an output from the printer to indicate an error by holding it low during error condition.
SLCT	65	I	General purpose input or line printer selected. (active high) This is an output from the printer to indicate that the line printer has been selected.
BUSY	66	I	General purpose input or line printer busy. (active high) An output from the printer to indicate printer is not ready to accept data.
PE	67	I	General purpose input or line printer paper empty. (active high) An output from the printer to indicate out of paper.
ACK~	68	I	General purpose input or line printer acknowledge. (active low) An output from the printer to indicate that data has been accepted successfully.
GND	2,7,8,9 13,22,27 42,54 61,62	O	Signal and power ground. All pins must be tied to ground.
Vcc	23,40, 64	I	Power supply input. All pins must be tied to the supply.

PROGRAMMING TABLE

DLAB	A2	A1	A0	READ MODE	WRITE MODE
0	0	0	0	Receive Holding Register	Transmit Holding Register
0	0	0	1		Interrupt Enable Register
x	0	1	0	Interrupt Status Register	
x	0	1	1	Line Control Register	
x	1	0	0		Modem Control Register
x	1	0	1	Line Status Register	
x	1	1	0	Modem Status Register	
x	1	1	1	Scratchpad Register	Scratchpad Register
1	0	0	0		LSB of Divisor Latch
1	0	0	1		MSB of Divisor Latch

REGISTER FUNCTIONAL DESCRIPTION

TRANSMIT AND RECEIVE HOLDING REGISTERS

The serial transmitter section consists of a Transmit Hold Register and Transmit Shift Register. The status of the transmit hold register is provided in the Line Status Register. Writing to this register will transfer the contents of the data bus (D7-D0) to the transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set. On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the SIN is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the SIN input. Receiver status codes will be posted in the Line Status Register.

INTERRUPT ENABLE REGISTER (IER)
The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status, and modem status registers to the INTS output pin.

IER BIT-0:
0 = disable receiver ready interrupt
1 = enable receiver ready interrupt

IER BIT-1:
0 = disable transmitter empty interrupt
1 = enable transmitter empty interrupt

IER BIT-2:
0 = disable receiver line status interrupt
1 = enable receiver line status interrupt

IER BIT-3:
0 = disable modem status register interrupt.
1 = enable modem status register interrupt.

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)
The LD1107 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized manner. During the read cycle the LD1107 provides the highest interrupt level to be serviced by the CPU,

no other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level	Source of the interrupts
1	ISR (Receiver Line Status Register)
2	RXRDY (Received Data Ready)
3	TXRDY (Transmitter holding register empty)
4	MSR (Modem Status Register)

ISR BIT-0:
0 = an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine
1 = no interrupt pending

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to zero.

LINE CONTROL REGISTER (LCR)
The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.
00 = 5 bits word length
01 = 6 bits word length
10 = 7 bits word length
11 = 8 bits word length

LCR BIT-2:
The number of stop bits can be specified by this bit.
0 = 1 stop bit , when word length = 5, 6, 7, 8 bits
1 = 1 and 1/2 stop bits , when word length = 5 bits
1 = 2 stop bits, word length = 6, 7, 8 bits

LCR BIT-3:
Parity or no parity can be selected via this bit.
0 = no parity
1 = a parity bit is generated during the transmission, receiver also checks for received parity

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0 = odd parity is generated by calculating odd number of 1's in the transmitted data, receiver also checks for same format
1 = an even parity bit is generated by calculating the number of even 1's in the transmitted or received data.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5 = 1 and LCR BIT-4 = 0 parity bit is forced to "1" in the transmitted and received data
LCR BIT-5 = 1 and LCR BIT-4 = 1 parity bit is forced to "0" in the transmitted and received data

LCR BIT-6:
Break control bit.
1 = forces the transmitter output (SOUT) to go low to alert the communication terminal
0 = normal operating condition

LCR BIT-7:
The internal baud rate counter latch enable (DLAB).
0 = normal operation
1 = select divisor latch register

MODEM CONTROL REGISTER (MCR)
This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0 = force DTR~ output to high
1 = force DTR~ output to low

MCR BIT-1:
0 = force RTS~ output to high
1 = force RTS~ output to low

MCR BIT-2:
Not used.

MCR BIT -3:
INTS output control.
0 = INTS output disabled
1 = INTS output enabled

MCR BIT -4:
0 = normal operating mode
1 = enable local loop-back mode (diagnostics). The

transmitter output (SOUT) is set high (Mark condition), the receiver input (SIN) , CTS~, DSR~, DCD~, and RI~ are disabled. Internally, the transmitter output is connected to the receiver input and DTR~, RTS~ are connected to modem control inputs. In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control Inputs. The interrupts are still controlled by the IER .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)
This register provides the status of data transfer to CPU.

LSR BIT-0:
0 = no data in receive holding register
1 = data has been received and saved in the receive holding register

LSR BIT-1:
0 = no overrun error (normal)
1 = overrun error, next character arrived before receive holding register was emptied

LSR BIT-2:
0 = no parity error (normal)
1 = parity error, received data does not have correct parity information

LSR BIT-3:
0 = no framing error (normal)
1 = framing error received, received data did not have a valid stop bit

LSR BIT-4:
0 = no break condition (normal)
1 = receiver received a break signal (SIN was low for one character time frame)

LSR BIT-5:
0 = transmit holding register is full. LD1107 will not accept any data for transmission
1 = transmit holding register is empty. CPU can load the next character.

LSR BIT-6:
0 = transmitter holding and shift registers are full
1 = transmitter holding and shift registers are empty

LSR BIT-7:
Not used. Set to zero permanently.

MODEM STATUS REGISTER (MSR)
This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS~ input to the LD1107 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR~ input to the LD1107 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI~ input to the LD1107 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD~ input to the LD1107 has changed state since the last time it was read.

MSR BIT-4:
This bit is the compliment of the CTS~ input. Equivalent to RTS in the MCR during loop-back mode.

MSR BIT-5:
This bit is the compliment of the DSR~ input. Equivalent to DTR in the MCR during loop-back mode.

MSR BIT-6:
This bit is the compliment of the RI~ input.

MSR BIT-7:
This bit is the compliment to the CD~ input.

SCRATCHPAD REGISTER (READ/WRITE)
LD1107 provides a temporary data register to store 8 bits of information for variable use.

PRINTER PORT REGISTER DESCRIPTIONS

PORT REGISTER
Bidirectional printer port.
Writing to this register during output mode will transfer the contents of the data bus to the PD7-PD0 ports . Reading this register during input mode will transfer the states of the PD7-PD0 to the data bus. This register will be set to the output mode after reset or keeping the BIDEN input in low state.

PR BIT 7-0:
PD7-PD0 bidirectional I/O ports.

STATUS REGISTER
This register provides the state of the printer outputs and the interrupt condition.

SR BIT 1-0:
Not used. Are set to "1" permanently.

SR BIT-2:
Interrupt condition.
0= an interrupt is pending
This bit will be set to "0" at the falling edge of the ACK~ input.
1= no interrupt is pending
Reading the STATUS REGISTER will set this bit to "1".

SR BIT-3:
ERROR~ input state.
0= ERROR~ input is in low state
1= ERROR~ input is in high state

SR BIT-4:
SLCT input state.
0= SLCT input is in low state
1= SLCT input is in high state

SR BIT-5:
PE input state.
0= PE input is in low state
1= PE input is in high state

SR BIT-6:
ACK~ input state.
0= ACK~ input is in low state
1= ACK~ input is in high state

SR BIT-7:
BUSY input state.
0= BUSY input is in high state
1= BUSY input is in low state

COMMAND REGISTER
The state of the STROBE~, AUTOFDXT~, INIT, SLCTIN~ pins, and interrupt enable bit can be read by this register regardless of the I/O direction.

COM BIT-0:
STROBE~ input pin.
0= STROBE~ pin is in high state
1= STROBE~ pin is in low state

COM BIT-1:
AUTOFDXT~ input pin.
0= AUTOFDXT~ pin is in high state
1= AUTOFDXT~ pin is in low state

COM BIT-2:
INIT input pin.
0= INIT pin is in low state
1= INIT pin is in high state

COM BIT-3:
SLCTIN~ input pin.
0= SLCTIN~ pin is in high state
1= SLCTIN~ pin is in low state

COM BIT-4:
Interrupt mask.
0= Interrupt (INTP output) is disabled
1= Interrupt (INTP output) is enabled

COM BIT 7-5:
Not used. Are set to "1" permanently.

CONTROL REGISTER.
Writing to this register will set the state of the STROBE~, AUTOFDXT~, INIT, SLCTIN pins, and interrupt mask register.

CON BIT-0:
STROBE~ output control bit.
0= STROBE~ output is set to high state
1= STROBE~ output is set to low state

CON BIT-1:
AUTOFDXT~ output control bit.
0= AUTOFDXT~ output is set to high state
1= AUTOFDXT~ output is set to low state

CON BIT-2:
INIT output control bit.
0 = INIT output is set to low state
1 = INIT output is set to high state

CON BIT-3:
SLCTIN~ output control bit.
0 = SLCTIN~ output is set to high state
1 = SLCTIN~ output is set to low state

CON BIT-4:
Interrupt output control bit.
0 = INTP output is disabled
1 = INTP output is enabled

CON BIT-5:
I/O select. Direction of the PD7-PD0 can be selected by setting or clearing this bit.
0 = PD7-PD0 are set for bidirectional mode
1 = PD7-PD0 are set for output mode

CON BIT 7-6:
Not used.

I/O SELECT REGISTER
Software controlled I/O select.
Bidirectional mode can be selected by keeping the BIDEN input in low state and setting CON BIT-5 to zero. Writing a "AA" Hex to the I/O SELECT REGISTER will enable the input mode and any other values will set the PD7-PD0 to the output mode.
Hardware/software I/O select can also be achieved, by utilizing the BIDEN pin. Setting CON BIT-5 to zero and writing "AA" Hex to the I/O SELECT REGISTER. PD7-PD0 will be in input mode when BIDEN is held high, otherwise output mode.

LD1107 EXTERNAL RESET CONDITION TABLE:

REGISTERS	RESET STATE
IER	IER BITS 0-7 = 0
ISR	ISR BIT-0 = 1, ISR BITS 1-7 = 0
LCR	LCR BITS 0-7 = 0
MCR	MCR BITS 0-7 = 0
LSR	LSR BITS 0-4 = 0, LSR BITS 5-6 = 1 LSR, BIT 7 = 0
MSR	MSR BITS 0-3 = 0, MSR BITS 4-7 = input signals
CR	CR BIT 4 = 0

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.86

SIGNALS	RESET STATE
SOUT	High
RTS~	High
DTR~	High
INTS	Three state
INTP	Three state
PD7-PD0	Output mode, PD7-PD0 = 0
STROBE~	Output mode, high
AUTOFDXT~	Output mode, high
INIT	Output mode, low
SLCTIN~	Output mode, high

PRINTER PORT PROGRAMMING TABLE:

A1	A0	IOW~	IOR~
0	0	PORT REGISTER	PORT REGISTER
0	1	I/O SELECT REGISTER	STATUS REGISTER *
1	0	CONTROL REGISTER	COMMAND REGISTER

* Reading the status register will reset the INTP output.

I/O SELECT REGISTER (WRITE ONLY)

CONTROL REGISTER (D5)	BIDEN	I/O SELECT REGISTER (D7-D0)	PORT MODE
1	x	xxxxxxxx	OUTPUT
0	1	xxxxxxxx	INPUT
0	0	10101010	INPUT
0	0	xxxxxxxx exp. AA Hex	OUTPUT

PRINTER PORT REGISTER CONFIGURATIONS

PORT REGISTER (READ/WRITE)

D7	D6	D5	D4	D3	D2	D1	D0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

STATUS REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
BUSY~	ACK	PE	SLCT	ERROR STATE	IRQ	1	1
					1 = No interrupt 0 = Interrupt		

COMMAND REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	IRQ ENABLE	SLCTIN~	INIT	AUTO-FDXT~	STROBE~
			0 = IRQ disabled 1 = IRQ enabled				

CONTROL REGISTER (WRITE ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
--	--	I/O SELECT	IRQ MASK	SLCTIN~	INIT	AUTO-FDXT~	STROBE~
	0 = Output 1 = Bidirectional		0 = IRQ output disabled 1 = IRQ output enabled				

LD1107 ACCESSIBLE REGISTERS

Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
ISR	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
MCR	0	0	0	loop back	interrupt enable	Not used	RTS~	DTR~
LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
MSR	CD~	RI~	DSR~	CTS~	delta CD~	delta RI~	delta DSR~	delta CTS~
SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
DLSB	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
DMSB	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
T_6	IOR~ strobe width	75			ns	
T_8	Read cycle	135			ns	
T_{10}	Delay from IOR~ to data			75	ns	100 pF load
T_{11}	IOR~ to floating data delay	0		50	ns	100 pF load
T_{12}	IOW~ strobe width	50			ns	
T_{14}	Write cycle	135			ns	
T_{15}	Data setup time	10			ns	
T_{16}	Data hold time	25			ns	
T_{18}	Address hold time from IOR~	0			ns	
T_{19}	Chip select hold time from IOR~	0			ns	
T_{20}	IOR~ delay from address	10			ns	
T_{21}	IOR~ delay from chip select	10			ns	
T_{22}	Address hold time from IOW~	5			ns	
T_{23}	Chip select hold time from IOW~	5			ns	
T_{24}	IOW~ delay from address	25			ns	
T_{25}	IOW~ delay from select	10			ns	
T_{26}	Reset pulse width	5			ns	
T_{27}	Clock high pulse duration	140				
T_{28}	Clock low pulse duration	140				External clock
TRANSMITTER						
T_{29}	Delay from rising edge of IOW~ to reset interrupt			75	ns	100 pF load
T_{30}	Delay from initial INT reset interrupt	24		40	*	
T_{31}	Delay from initial Write to interrupt	16		24	*	
T_{33}	Delay from start bit low to interrupt high			8	*	

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
T_{34}	Delay from IOR~ to reset interrupt			75	ns	100 pF load
MODEM CONTROL						
T_{35}	Delay from IOW~ to output			50	ns	100 pF load
T_{36}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{37}	Delay to reset interrupt from IOR~			70	ns	100 pF load
BAUD RATE GENERATOR						
N	Baud rate divisor	1		2^{16}-1		
RECEIVER						
T_{43}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{44}	Delay from IOR~ to reset interrupt			200	ns	100 pF load

* Baudout~ cycle

ABSOLUTE MAXIMUM RATINGS

Operating Supply range	5 Volts ± 5%
Voltage at any pin	GND-0.3 V to V_{CC}+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

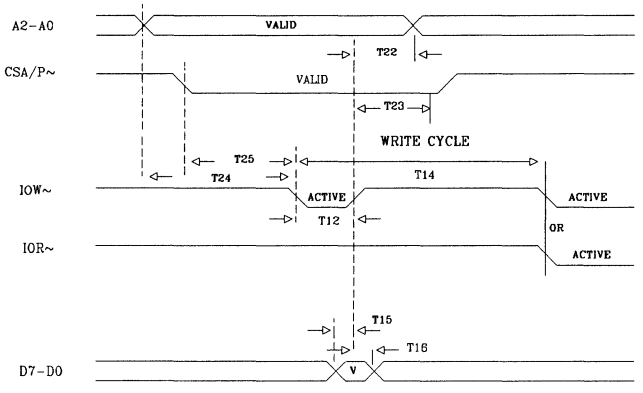
DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		V_{CC}	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		V_{CC}	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6.0 mA D7-D0 I_{OL}= 20.0 mA PD7-PD0 I_{OL}= 10 mA SLCTIN~, INIT~,STROBE~, AUTOFDXT~ I_{OL}= 6.0 mA on all other outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6.0 mA D7-D0 I_{OH}= -12.0 mA PD7-PD0 I_{OH}= -0.2 mA SLCTIN~, INIT~,STROBE~, AUTOFDXT~ I_{OH}= -6.0 mA on all other outputs
I_{CC}	Avg power supply current			30	mA	
I_{IL}	Input leakage			±10	uA	
I_{CL}	Clock leakage			±10	uA	

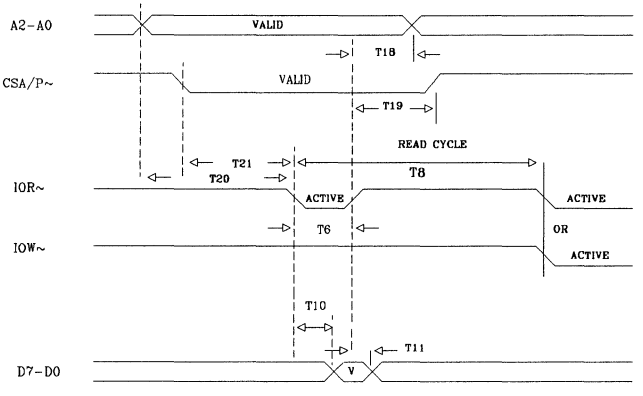
TIMING DIAGRAM

WRITE CYCLE TIMING



V = VALID
A = ACTIVE

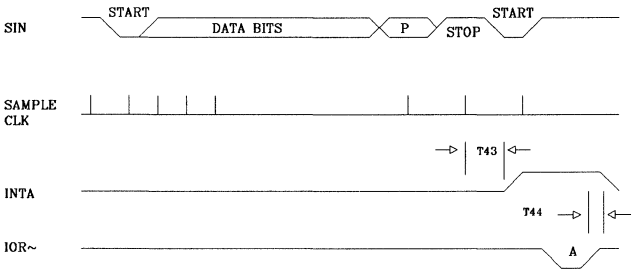
READ CYCLE TIMING



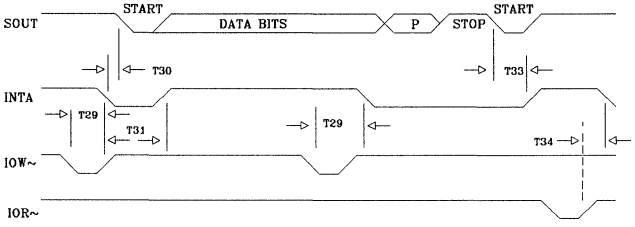
V = VALID
A = ACTIVE

TIMING DIAGRAM

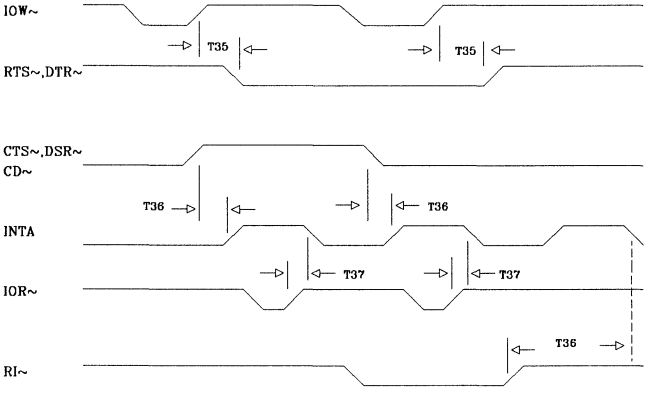
RECEIVER TIMING



TRANSMITTER TIMING



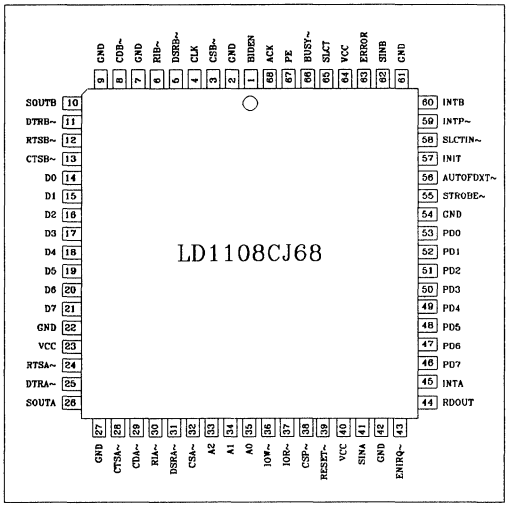
MODEM TIMING



DUAL UNIVERSAL ASYNCHRONOUS RECEIVER AND TRANSMITTER WITH PARALLEL PRINTER PORT

DESCRIPTION

The LD1108 is a dual universal asynchronous receiver and transmitter with a bidirectional CENTRONICS type parallel printer port. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 56kHz. The LD1108 is fabricated in an advanced 2u CMOS process to achieve low power drain and high speed requirements.



FEATURES

* Pin-to-pin and functionally compatible to VL16C452
* Bidirectional printer port
* Modem control signals (CTS~, RTS~, DSR~, DTR~, RI~, CD~)
* Programmable character lengths (5, 6, 7, 8)
* Even, odd, or no parity bit generation and detection
* Status report register
* Independent transmit and receive control
* TTL compatible inputs, outputs
* Fully compatible with all new bidirectional PS/2 printer port
* Direct replacement of logic for PC/XT/AT
* High data transfer rate

APPLICATIONS

* Dual RS232 receiver and/or transmitter
* Serial to parallel / parallel to serial converter
* Modem handshaking
* CENTRONICS printer port
* IBM PS/2 bidirectional printer port
* External bidirectional I/O
* IBM PC/XT/AT upgrade printer port

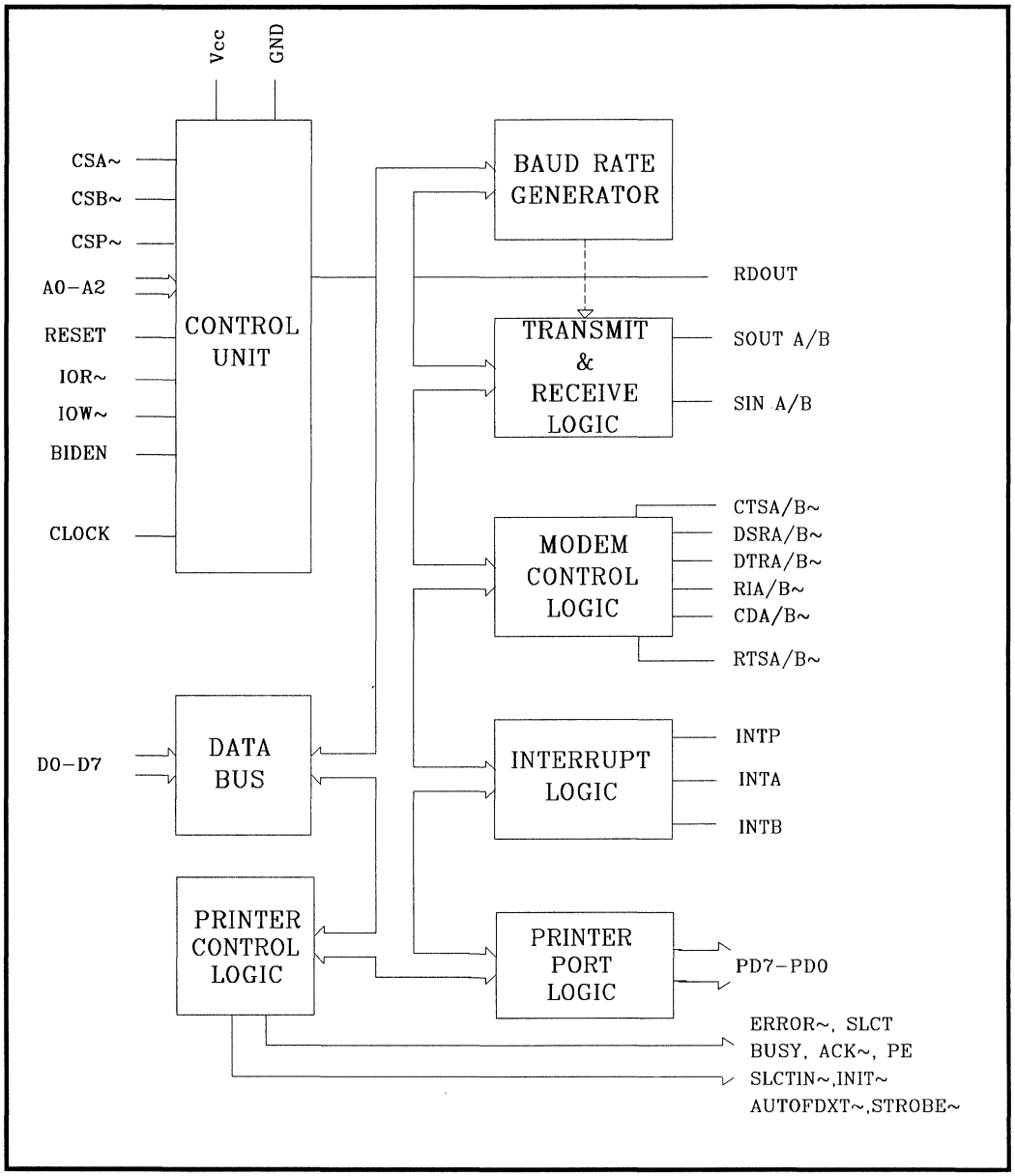
ORDERING INFORMATION

Part number	Package	Operating temperature
LD1108CJ68	PLCC	0° C to +70° C

GENERAL DESCRIPTION

The LD1108 is an improved version of the VL16C452 with higher speed operating access time. The LD1108 is the combined version of LD1102 and LD805 in a single monolithic form. The LD1108 performs the parallel to serial/serial to parallel conversion on the data characters received from the CPU or the MODEM. The LD1108 also provides the user with a fully bidirectional parallel data port that fully supports the parallel CENTRONICS type printer. The on board status registers will provide the error conditions, type and status of the transfer operations being performed. The LD1108 also has complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link. The LD1108 can interface easily to the most popular microprocessors and communications link faults can be detected with internal loopback capability.

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
BIDEN	1	I	I/O direction select. A high puts the parallel port in the software controlled mode (input/output). A low puts the parallel port in the output mode.
CSB~	3	I	Chip select B. (active low) A low at this pin (while CSA~ and CSP~ =h) will enable the UARTB / CPU data transfer operation.
CLK	4	I	External clock input. An external clock can be used to clock the internal circuit and the baud rate generator for custom and standard transmis sion rates.
DSRB~	5	I	Data set ready B. (active low) A low on this pin indicates that MODEM B is ready to exchange data with UARTB.
RIB~	6	I	Ring detect B indicator. (active low) A low on this pin indicates that MODEM B has received a ringing signal from the telephone line.
CDB~	8	I	Carrier detect B. (active low) A low on this pin indicates that carrier has been detected by the MODEM B.
SOUTB	10	O	Serial data output B. The serial data is transmitted via this pin with additional start , stop and parity bits. The SOUTB will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
DTRB~	11	O	Data terminal ready B. (active low) To indicate that LD1108 is ready to receive data. This pin can be controlled via the modem control register (MCRB bit-0). Writing a "1" at the MCRB bit-0 will set the DTRB~ output to low. This pin will be set to high state after writing a "0" to that register or after the reset .
RTSB~	12	O	Request to send B. (active low) To indicate that transmitter has data ready to send. Writing a "1" in the modem control register (MCRB bit-1) will set this pin to low state. After the reset this pin will be set to high.
CTSB~	13	I	Clear to send B. (active low) The CTSB~ signal is a MODEM control function input whose conditions can be tested by reading the MSRB BIT-4. CTSB~ has no effect on the transmitter output.
D0-D7	14-21	I/O	Bidirectional data I/O. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit (lsb) of the data bus and the first serial data bit to be received or transmit-ted.
RTSA~	24	O	Request to send A. (active low) To indicate that transmitter has data ready to send. Writing a "1" in the modem control register (MCRA bit-1) will set this pin to low state. After the reset this pin will be set to high.

SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
DTRA~	25	O	Data terminal ready A. (active low) To indicate that LD1108 is ready to receive data. This pin can be controlled via the modem control register (MCRA bit-0). Writing a "1" at the MCRA bit-0 will set the DTRA~ output to low. This pin will be set to high state after writing a "0" to that register or after the reset .
SOUTA	26	O	Serial data output A. The serial data is transmitted via this pin with additional start , stop and parity bits. The SOUTA will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CTSA~	28	I	Clear to send A. (active low) The CTSA~ signal is a MODEM control function input whose conditions can be tested by reading the MSRA BIT-4. CTSA~ has no effect on the transmitter output.
CDA~	29	I	Carrier detect A. (active low) A low on this pin indicates that carrier has been detected by the MODEM A.
RIA~	30	I	Ring detect A indicator. (active low) A low on this pin indicates that MODEM A has received a ringing signal from the telephone line.
DSRA~	31	I	Data set ready A. (active low) A low on this pin indicates that MODEM A is ready to exchange data with UARTA.
CSA~	32	I	Chip select A. (active low) A low at this pin (while CSB~ and CSP~ = h) will enable the UARTA / CPU data transfer operation.
A2	33	I	Address line 2. To select internal registers.
A1	34	I	Address line 1. To select internal registers.
A0	35	I	Address line 0. To select internal registers.
IOW~	36	I	I/O write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR~	37	I	I/O read strobe. (active low) A low level on this pin will transfer the contents of the LD1108 data bus to the CPU.
CSP~	38	I	Chip select P. (active low) To enable the LD1108 printer operation, this pin has to go low while CSA~ and CSB~ are high.
RESET~	39	I	Master reset. (active low) A low on this pin will reset all the outputs and internal registers. The parallel port of the LD1108 will be set to output mode, the transmitter output and the receiver input will be disabled during reset time.

SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
SINA	41	I	Serial data input A. The serial information (data) received from MODEM or RS232 to LD1108 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the SINA input is disabled from external connection and connected to the SOUTA output internally.
ENIRQ~	43	I	Interrupt source selection. (active low) The external ACK~ can be selected as an interrupt source by tying this pin to GND. Tying this pin to Vcc, will set the internal interrupt logic to the latched state, reading the STATUS register will reset the INTP output.
RDOUT	44	O	Read select out. A high on this pin indicates that the chip is being read by the CPU.
INTA	45	O	UART A interrupt output. (three state) This pin goes high (when enabled by MCRA BIT-3) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected.
PD7-PD0	46-53	I/O	Bidirectional parallel I/O. (three state) To transfer data in or out of the LD1108 parallel port. PD7-PD0 are latched during output mode.
STROBE~	55	I/O	General purpose I/O or strobe output. (open drain active low) To transfer latched data to the external peripheral or printer.
AUTOFDXT~	56	I/O	General purpose I/O or line printer autofeed. (open drain active low) To signal the printer for continuous form feed.
INIT~	57	I/O	General purpose I/O or line printer initialize. (open drain active low) To signal the line printer to enter internal initialization routine.
SLCTIN~	58	I/O	General purpose I/O or line printer select. (open drain active low) To select the line printer.
INTP~	59	O	Printer interrupt output. (active low) To signal the state of the printer port.
INTB	60	O	UART B interrupt output. (three state) This pin goes high (when enabled by MCRB BIT-3) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected.
SINB	62	I	Serial data input B. The serial information (data) received from MODEM or RS232 to LD1108 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the SINB input is disabled from external connection and connected to the SOUTB output internally.

SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
ERROR~	63	I	General purpose input or line printer error. (active low) This is an output from the printer to indicate an error by holding it low during error condition.
SLCT	65	I	General purpose input or line printer selected. (active high) This is an output from the printer to indicate that the line printer has been selected.
BUSY	66	I	General purpose input or line printer busy. (active high) An output from the printer to indicate printer is not ready to accept data.
PE	67	I	General purpose input or line printer paper empty. (active high) An output from the printer to indicate out of paper.
ACK~	68	I	General purpose input or line printer acknowledge. (active low) An output from the printer to indicate that data has been accepted successfully.
GND	2,7,9, 22,27, 42,54, 61	O	Signal and power ground. All pins must be tied to ground.
Vcc	23,40, 64	I	Power supply input. All pins must be tied to ground.

PROGRAMMING TABLE

CSB	CSA	DLAB	A2	A1	A0	READ MODE	WRITE MODE
1	0	0	0	0	0	Receive Holding Register A	Transmit Holding Register A
1	0	0	0	0	1		Interrupt Enable Register A
1	0	x	0	1	0	Interrupt Status Register A	
1	0	x	0	1	1		Line Control Register A
1	0	x	1	0	0		Modem Control Register A
1	0	x	1	0	1	Line Status Register A	
1	0	x	1	1	0	Modem Status Register A	
1	0	x	1	1	1	Scratchpad Register A	Scratchpad Register A
1	0	1	0	0	0		LSB of Divisor Latch A
1	0	1	0	0	1		MSB of Divisor Latch A
0	1	0	0	0	0	Receive Holding Register B	Transmit Holding Register B
0	1	0	0	0	1		Interrupt Enable Register B
0	1	x	0	1	0	Interrupt Status Register B	
0	1	x	0	1	1		Line Control Register B
0	1	x	1	0	0		Modem Control Register B
0	1	x	1	0	1	Line Status Register B	
0	1	x	1	1	0	Modem Status Register B	
0	1	x	1	1	1	Scratchpad Register B	Scratchpad Register B
0	1	1	0	0	0		LSB of Divisor Latch B
0	1	1	0	0	1		MSB of Divisor Latch B

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER A/B

The serial transmitter section consists of a Transmit Hold Register A/B and Transmit Shift Register A/B. The status of the transmit hold register is provided in the Line Status Register A/B. Writing to this register will transfer the contents of the data bus (D7-D0) to the transmit holding register A/B whenever the transmitter holding register A/B or transmitter shift register A/B is empty. The transmit holding register empty A/B flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register A/B. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the SINA/B is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the SINA/B input. Receiver status codes will be posted in the Line Status Register A/B.

INTERRUPT ENABLE REGISTER A/B

The Interrupt Enable Register A/B masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INTA/B output pin.

IER BIT-0:
0 = disable receiver ready interrupt
1 = enable receiver ready interrupt

IER BIT-1:
0 = disable transmitter empty interrupt
1 = enable transmitter empty interrupt

IER BIT-2:
0 = disable receiver line status interrupt
1 = enable receiver line status interrupt

IER BIT-3:
0=disable modem status register interrupt
1=enable modem status register interrupt

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER A/B
The LD1108 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register A/B provides the source of the interrupt in prioritized manner. During the read cycle, the LD1108 provides the highest interrupt level to be serviced by the CPU. No other interrupts are acknowledged until the particular interrupt has been serviced. The following are the prioritized interrupt levels:

Priority level	Bit-2	Bit-1	Bit-0	Source of the interrupts
1	1	1	0	ISR A/B (Receiver Line Status Register)
2	1	0	0	RXRDY A/B (Received Data Ready)
3	0	1	0	TXRDY A/B (Transmitter holding register empty)
4	0	0	0	MSR A/B (Modem Status Register)
0	0	0	1	No interrupts

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine
1=no interrupt pending

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to zero.

LINE CONTROL REGISTER A/B
The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.
00=5 bits word length
01=6 bits word length
10=7 bits word length
11=8 bits word length

LCR BIT-2:
The number of stop bits can be specified by this bit.
0=1 stop bit , when word length=5, 6, 7, 8 bits
1=1 and 1/2 stop bit , when word length=5 bits
1=2 stop bits, word length=6, 7, 8 bits

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission; receiver also checks for received parity

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=odd parity is generated by calculating odd number of 1's in the transmitted data; receiver also checks for same format.
1=an even parity bit is generated by calculating the number of even 1's in the transmitted or received data.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

LCR BIT-5=1 and LCR BIT-4=0 parity bit is forced to "1" in the transmitted and received data
LCR BIT-5=1 and LCR BIT-4=1 parity bit is forced to "0" in the transmitted and received data

LCR BIT-6:
Break control bit.
1=forces the transmitter output (SOUTA/B) to go low to alert the communication terminal
0=normal operating condition

LCR BIT-7:
The internal baud rate counter latch enable (DLAB).
0=normal operation
1=select divisor latch register

MODEM CONTROL REGISTER A/B
This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR~ output to high
1=force DTR~ output to low

MCR BIT-1:
0=force RTS~ output to high
1=force RTS~ output to low

MCR BIT-2:
Not used.

MCR BIT -3:
INTA/B output control.
0=INTA/B outputs disabled
1=INTA/B outputs enabled

MCR BIT -4:
0=normal operating mode
1=enable local loop-back mode (diagnostics). The transmitter output (SOUTA/B) is set high (Mark condition), the Receiver inputs (SINA/B, CTSA/B~, DSRA/B~, CDA/B~, and RIA/B~) are disabled. Internally, the transmitter output is connected to the receiver input and DTRA/B~, RTSA/B~ are connected to modem control inputs. In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupt sources are now the lower four bits of the Modem Control Register instead of the four Modem Control Inputs. The interrupts are still controlled by the IERA/B.

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER A/B
This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=a data has been received and saved in the receive holding register

LSR BIT-1:
0=no overrun error (normal)
1=overrun error, next character arrived before receive holding register was empty

LSR BIT-2:
0=no parity error (normal)
1=parity error, received data does not have correct parity information

LSR BIT-3:
0=no framing error (normal)
1=framing error received, received data did not have a valid stop bit

LSR BIT-4:
0=no break condition (normal)
1=receiver received a break signal (SIN was low for one character time frame)

LSR BIT-5:
0=transmit holding register is full. LD1108 will not accept any data for transmission.
1=transmit holding register is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full
1=transmitter holding and shift registers are empty

LSR BIT-7:
Not used. Set to zero permanently.

MODEM STATUS REGISTER A/B
This register provides the current state of the control lines from the modem or peripheral to the CPU. Four

bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS~ input to the LD1108 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR~ input to the LD1108 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI~ input to the LD1108 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD~ input to the LD1108 has changed state since the last time it was read.

MSR BIT-4:
This bit is the compliment of the CTS~ input. It is equivalent to RTS in the MCR during loop-back mode.

MSR BIT-5:
This bit is the compliment of the DSR~ input. It is equivalent to DTR in the MCR during loop-back mode.

MSR BIT-6:
This bit is the compliment of the RI~ input.

MSR BIT-7:
This bit is the compliment to the CD~ input.

SCRATCHPAD REGISTER A/B
LD1108 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.69
2400	48	
3600	36	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.86

The LD1108 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-16 MHz and dividing it by any divisor from 2 to 2^{16}-1. Customized Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of the baud rate generator.

$$\text{divisor value (decimal)} = \frac{\text{input frequency}}{\text{baud rate x 16}}$$

EXAMPLE: $\frac{1.8432 \times 10^6}{1200 \text{ (baud)} \times 16} = 96$ (decimal)

96 decimal = 0060 HEX
Divisor MSB = 00
Divisor LSR = 60

PRINTER PORT PROGRAMMING TABLE:

A1	A0	IOW~	IOR~
0	0	PORT REGISTER	PORT REGISTER
0	1	I/O SELECT REGISTER	STATUS REGISTER *
1	0	CONTROL REGISTER	COMMAND REGISTER

* Reading the status register will reset the INTP output.

I/O SELECT REGISTER (WRITE ONLY)

CONTROL REGISTER (D5)	BIDEN	I/O SELECT REGISTER (D7-D0)	PORT MODE
1	x	xxxxxxxxx	OUTPUT
0	1	xxxxxxxxx	INPUT
0	0	10101010	INPUT
0	0	xxxxxxxx exp. AA Hex	OUTPUT

REGISTER DESCRIPTIONS

PORT REGISTER
Bidirectional printer port.
Writing to this register during output mode will transfer the contents of the data bus to the PD7-PD0 ports . Reading this register during input mode will transfer the states of the PD7-PD0 to the data bus. This register will be set to the output mode after reset or keeping the BIDEN input in low state.

PR BIT 7-0:
PD7-PD0 bidirectional I/O ports.

STATUS REGISTER
This register provides the state of the printer outputs and the interrupt condition.

SR BIT 1-0:
Not used. Are set to "1" permanently.

SR BIT-2:
Interrupt condition.
0= an interrupt is pending
This bit will be set to "0" at the falling edge of the ACK~ input.
1= no interrupt is pending
Reading the STATUS REGISTER will set this bit to "1".

SR BIT-3:
ERROR~ input state.
0= ERROR~ input is in low state
1= ERROR~ input is in high state

SR BIT-4:
SLCT input state.
0= SLCT input is in low state
1= SLCT input is in high state

SR BIT-5:
PE input state.
0= PE input is in low state
1= PE input is in high state

SR BIT-6:
ACK~ input state.
0= ACK~ input is in low state
1= ACK~ input is in high state

SR BIT-7:
BUSY input state.
0 = BUSY input is in high state
1 = BUSY input is in low state

COMMAND REGISTER
The state of the STROBE~, AUTOFDXT~, INIT, SLCTIN~ pins, and interrupt enable bit can be read by this register regardless of the I/O direction.

COM BIT-0:
STROBE~ input pin.
0 = STROBE~ pin is in high state
1 = STROBE~ pin is in low state

COM BIT-1:
AUTOFDXT~ input pin.
0 = AUTOFDXT~ pin is in high state
1 = AUTOFDXT~ pin is in low state

COM BIT-2:
INIT input pin.
0 = INIT pin is in low state
1 = INIT pin is in high state

COM BIT-3:
SLCTIN~ input pin.
0 = SLCTIN~ pin is in high state
1 = SLCTIN~ pin is in low state

COM BIT-4:
Interrupt mask.
0 = Interrupt (INTP output) is disabled
1 = Interrupt (INTP output) is enabled

COM BIT 7-5:
Not used. Are set to "1" permanently.

CONTROL REGISTER.
Writing to this register will set the state of the STROBE~, AUTOFDXT~, INIT, SLCTIN pins, and interrupt mask register.

CON BIT-0:
STROBE~ output control bit.
0 = STROBE~ output is set to high state
1 = STROBE~ output is set to low state

CON BIT-1:
AUTOFDXT~ output control bit.
0 = AUTOFDXT~ output is set to high state
1 = AUTOFDXT~ output is set to low state

CON BIT-2:
INIT output control bit.
0 = INIT output is set to low state
1 = INIT output is set to high state

CON BIT-3:
SLCTIN~ output control bit.
0 = SLCTIN~ output is set to high state
1 = SLCTIN~ output is set to low state

CON BIT-4:
Interrupt output control bit.
0 = INTP output is disabled
1 = INTP output is enabled

CON BIT-5:
I/O select. Direction of the PD7-PD0 can be selected by setting or clearing this bit.
0 = PD7-PD0 are set for bidirectional mode
1 = PD7-PD0 are set for output mode

CON BIT 7-6:
Not used.

I/O SELECT REGISTER
Software controlled I/O select.
Bidirectional mode can be selected by keeping the BIDEN input in low state and setting **CON BIT-5** to zero. Writing a "AA" Hex to the I/O SELECT REGISTER will enable the input mode and any other values will set the PD7-PD0 to the output mode.
Hardware/software I/O select can also be achieved, by utilizing the BIDEN pin. Setting **CON BIT-5** to zero and writing "AA" Hex to the I/O SELECT REGISTER. PD7-PD0 will be in input mode when BIDEN is held high, otherwise output mode.

LD1108 EXTERNAL RESET CONDITION TABLE:

REGISTERS	RESET STATE
IERA/B	IERA/B BITS 0-7=0
ISRA/B	ISRA/B BIT 0=1, ISRA/B BITS 1-7=0
LCRA/B	LCRA/B BITS 0-7=0
MCRA/B	MCRA/B BITS 0-7=0
LSRA/B	LSRA/B BITS 0-4=0, LSRA/B BITS 5-6=1, LSRA/B BIT 7=0
MSRA/B	MSRA/B BITS 0-3=0, MSRA/B BITS 4-7=input signals
CR	CR BIT 4=0

SIGNALS	RESET STATE
SOUTA/B	High
RTSA/B~	High
DTRA/B~	High
INTA/B	Three state
INTP	Three state
PD7-PD0	Output mode, PD7-PD0=0
STROBE~	Output mode, high
AUTOFDXT~	Output mode, high
INIT	Output mode, low
SLCTIN~	Output mode, high

PRINTER PORT REGISTER CONFIGURATIONS

PORT REGISTER (READ/WRITE)

D7	D6	D5	D4	D3	D2	D1	D0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

STATUS REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
BUSY~	ACK	PE	SLCT	ERROR STATE	IRQ	1	1
					1 = No interrupt 0 = Interrupt		

COMMAND REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	IRQ ENABLE	SLCTIN~	INIT	AUTO-FDXT~	STROBE~
			0 = IRQ disabled 1 = IRQ enabled				

CONTROL REGISTER (WRITE ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
--	--	I/O SELECT	IRQ MASK	SLCTIN~	INIT	AUTO-FDXT~	STROBE~
	1 = Output 0 = Bidirectional		0 = INTP output disabled 1 = INTP output enabled				

LD1108 ACCESSIBLE REGISTERS

Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
ISR	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
MCR	0	0	0	loop back	interrupt enable	Not used	RTS~	DTR~
LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
MSR	CD~	RI~	DSR~	CTS~	delta CD~	delta RI~	delta DSR~	delta CTS~
SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
DLSB	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
DMSB	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
T_6	IOR~ strobe width	75			ns	
T_8	Read cycle	135			ns	
T_{10}	Delay from IOR~ to data			75	ns	100 pF load
T_{11}	IOR~ to floating data delay	0		50	ns	100 pF load
T_{12}	IOW~ strobe width	50			ns	
T_{14}	Write cycle	135			ns	
T_{15}	Data setup time	10			ns	
T_{16}	Data hold time	25			ns	
T_{18}	Address hold time from IOR~	0			ns	
T_{19}	Chip select hold time from IOR~	0			ns	
T_{20}	IOR~ delay from address	10			ns	
T_{21}	IOR~ delay from chip select	10			ns	
T_{22}	Address hold time from IOW~	5			ns	
T_{23}	Chip select hold time from IOW~	5			ns	
T_{24}	IOW~ delay from address	25			ns	
T_{25}	IOW~ delay from select	10			ns	
T_{26}	Reset pulse width	5			ns	
T_{27}	Clock high pulse duration	140				
T_{28}	Clock low pulse duration	140				External clock
TRANSMITTER						
T_{29}	Delay from rising edge of IOW~ to reset interrupt			75	ns	100 pF load
T_{30}	Delay from initial INT reset interrupt	24		40	*	
T_{31}	Delay from initial Write to interrupt	16		24	*	
T_{33}	Delay from start bit low to interrupt high			8	*	
T_{34}	Delay from IOR~ to reset interrupt			75	ns	100 pF load

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
MODEM CONTROL						
T_{35}	Delay from IOW~ to output			50	ns	100 pF load
T_{36}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{37}	Delay to reset interrupt from IOR~			70	ns	100 pF load
BAUD RATE GENERATOR						
N	Baud rate divisor	1		2^{16}-1		
RECEIVER						
T_{43}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{44}	Delay from IOR~ to reset interrupt			200	ns	100 pF load

* Baud cycle

ABSOLUTE MAXIMUM RATINGS

Operating Supply range	5 Volts ± 5%
Voltage at any pin	GND-0.3 V to V_{CC}+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

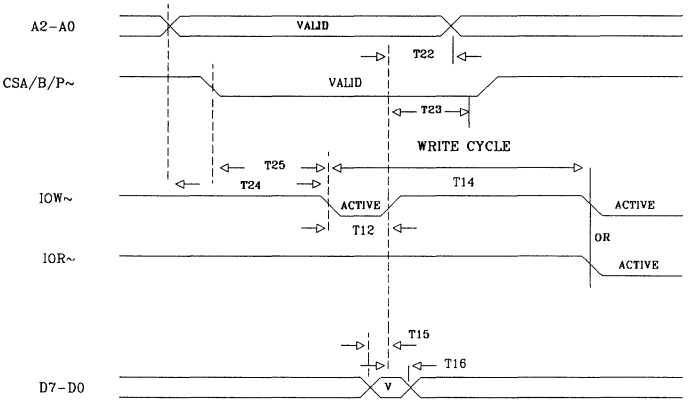
DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		V_{CC}	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		V_{CC}	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6.0 mA D7-D0 I_{OL}= 20.0 mA PD7-PD0 I_{OL}= 10 mA SLCTIN~, INIT~,STROBE~, AUTOFDXT~ I_{OL}= 6.0 mA on all other outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6.0 mA D7-D0 I_{OH}= -12.0 mA PD7-PD0 I_{OH}= -0.2 mA SLCTIN~, INIT~,STROBE~, AUTOFDXT~ I_{OH}= -6.0 mA on all other outputs
I_{CC}	Avg power supply current			30	mA	
I_{IL}	Input leakage			±10	uA	
I_{CL}	Clock leakage			±10	uA	

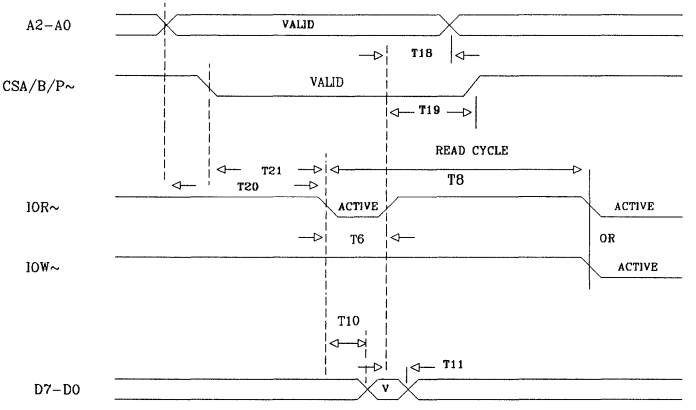
TIMING DIAGRAM

WRITE CYCLE TIMING



V = VALID
A = ACTIVE

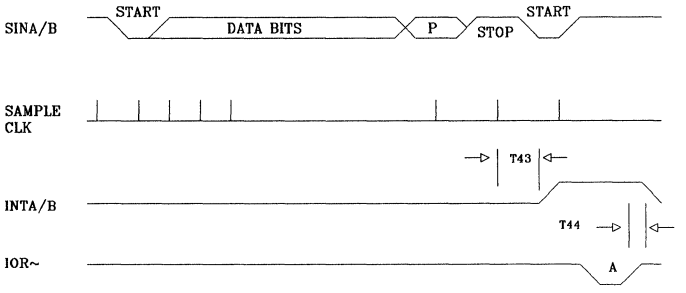
READ CYCLE TIMING



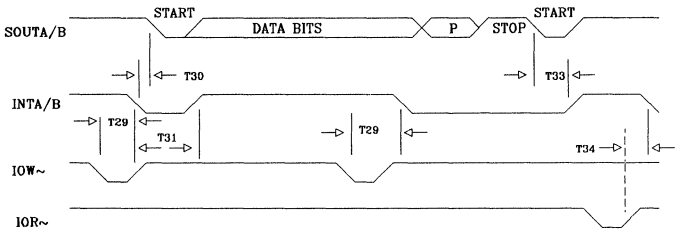
V = VALID
A = ACTIVE

TIMING DIAGRAM

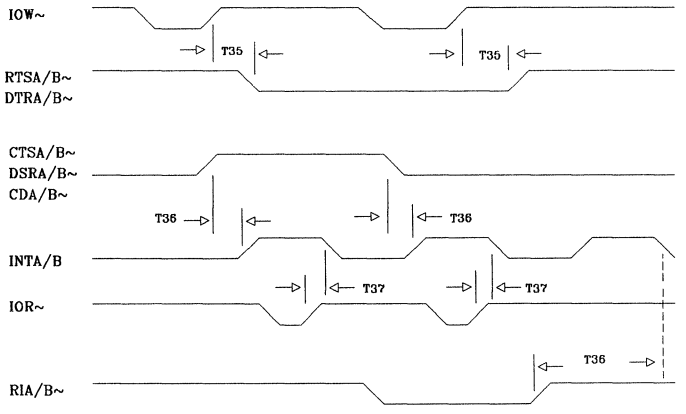
RECEIVER TIMING



TRANSMITTER TIMING



MODEM TIMING

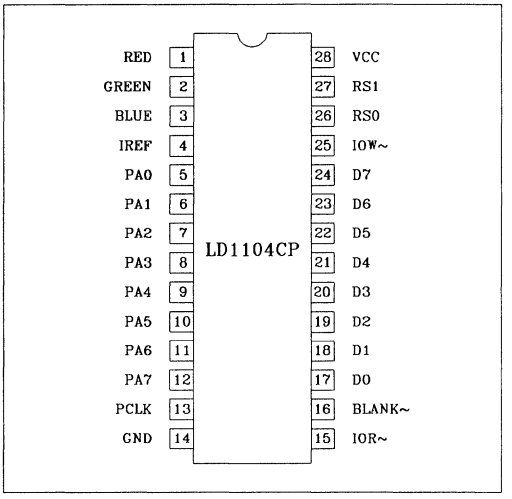


VIDEO 3

VIDEO DAC WITH LOOK-UP TABLE

DESCRIPTION

The LD1104 is a digital to analog converter with an internal look-up table designed to drive a 75 ohm line. The output of the DAC is designed to produce 0.7 volts peak white amplitude when driving a 75 ohm line with an IREF of 4.4 mA or when driving a doubly terminated 75 ohm load with an IREF of 8.8 mA. The DAC outputs will be set to their minimum values during the blanking pulse period.



FEATURES

* Pin to pin compatible with IMS G171
* 256K possible colors
* Microprocessor compatible interface
* Low power CMOS design
* 6 bit DAC per gun and RGB analog output
* Pixel rates up to 50 MHz
* Pixel word mask
* TTL compatible inputs
* Single 5 volts operating voltage

APPLICATIONS

* VGA graphic card
* Workstations with color output
* Color terminals
* Raster scan video systems

ORDERING INFORMATION

Part number	Package	Operating temperature
LD1104CP28-35	Plastic	0°C to 70°C
LD1104CJ44-35	PLCC	0°C to 70°C
LD1104CP28-50	Plastic	0°C to 70°C
LD1104CJ44-50	PLCC	0°C to 70°C

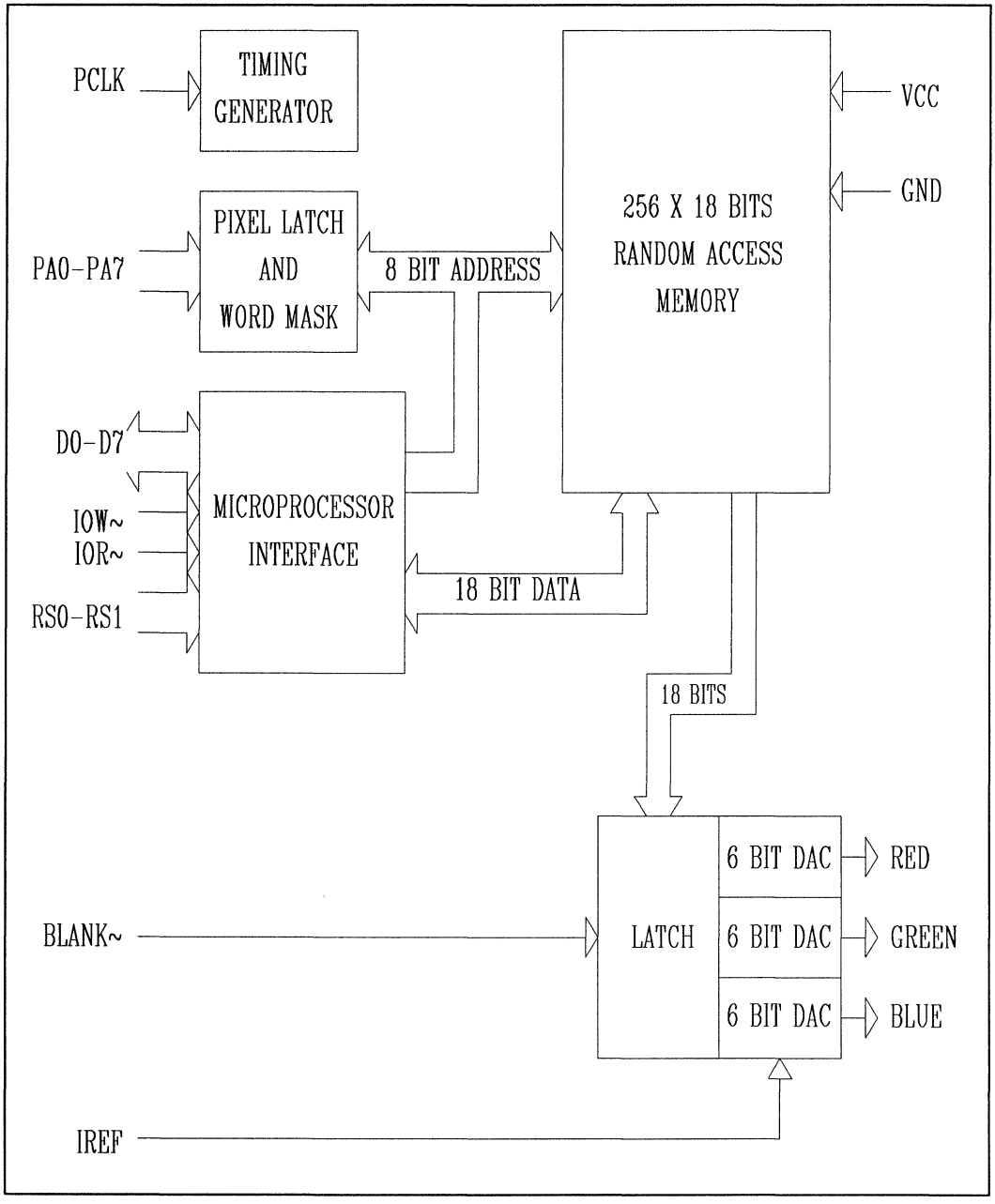
GENERAL DESCRIPTION

The LD1104 is designed to operate in a high speed analog and digital video interface environment to provide 256 different colors.

The display colors can be changed to facilitate animation, flashing or overlay objects with a single write cycle, by utilizing the pixel word mask capability without modifying the look-up table. A high speed internal random access memory has been provided to pipeline a 50 MHz pixel rate output in three clock cycles. An external blanking signal can be input to the LD1104 to synchronize the pixel stream.

The contents of the look-up table (random access memory) can be accessed via an 8 bit wide microprocessor interface bus without disturbing the video path.

BLOCK DESCRIPTION



SYMBOL DESCRIPTION

Symbol	Pin	Symbol type	Pin description
RED	1	O	Video DAC RED signal output.
GREEN	2	O	Video DAC GREEN signal output.
BLUE	3	O	Video DAC BLUE signal output.
IREF	4	I	Reference current input. The external current source is applied to this pin to regulate the internal DAC current source. Each current source produces 1/30 of the IREF when turned on.
PA0-PA7	5-12	I	Pixel address. The byte wide value sampled on these inputs is masked by the pixel Mask Register and then used as the address into the color look-up table.
PCLK	13	I	Pixel clock. The pixel address and blanking inputs are sampled at the rising edge of PCLK.
GND	14	O	Ground. Signal and power ground.
IOR~	15	I	I/O read strobe. (active low) A low on this pin will transfer the contents of the addressed memory or the color information to the data bus.
BLANK~	16	I	Blanking input. (active low) A low level on this input, when sampled at the rising edge of PCLK, will cause a color value of zero to be applied to the inputs of the three DACs regardless of the color value of the current pixel.
D0-D7	17-24	I/O	Bidirectional I/O data bus. The contents of the data bus are transferred from the LD1104 internal registers to the host processor or vice-versa.
IOW~	25	I	I/O write strobe. (active low) A low on this pin will transfer the contents of the data bus to the addressed register or the internal memory (RAM).
RS0	26	I	Least significant bit of the register select.
RS1	27	I	Most significant bit of the register select.
V_{CC}	28	I	Power supply input.

REGISTERS PROGRAMMING TABLE:

RS1	RS0	IOW~	IOR~
0	0	PIXEL ADDRESS A	PIXEL ADDRESS A
0	1	COLOR VALUE	COLOR VALUE
1	0	PIXEL MASK	
1	1	PIXEL ADDRESS B	PIXEL ADDRESS B

REGISTER DESCRIPTIONS

PIXEL ADDRESS REGISTER A/B

The contents of the PIXEL ADDRESS REGISTER A are identical to the contents of the PIXEL ADDRESS REGISTER B during the read operation.
Writing to PIXEL ADDRESS A will specify an address within the color look-up table and initializes the color value register. Writing into PIXEL ADDRESS REGISTER B specifies an address within the color look-up table and loads the color value register with the contents of the location in the color look-up table address and then increments the PIXEL ADDRESS REGISTER.

COLOR VALUE REGISTER

The color value register is internally an 18 bit wide (6 bits per color) register used as a buffer between the microprocessor interface and the color look-up table. To perform a read or write to this register it is required to have a sequence of three byte transfers from or to the register. Note that only the six least significant bits of the bus are used during the write mode and the rest are set to zero during the read mode. The internal address pointer is set to the RED color address and then increments to the GREEN and BLUE color addresses regardless of the read or write operation sequence.
After writing three values to this register its contents are written to the location in the color look-up table specified by the pixel address register and copied into the COLOR VALUE REGISTER. The PIXEL ADDRESS REGISTER then increments.

PIXEL MASK REGISTER

The PIXEL MASK REGISTER can be used to mask selected bits of the pixel address value applied to the PIXEL ADDRESS input (PA7-PA0). The PIXEL MASK REGISTER is logically anded with the PIXEL ADDRESS bits, writing a zero in each bit position will alter the values to zero. Note that writing a one to this register will not alter the PIXEL ADDRESS bits.

WRITING TO THE LOOK-UP TABLE

The color of each pixel can be changed by specifying the location (address of the pixel) in the look-up table via PIXEL ADDRESS REGISTER A. The intensity of each color (RED, GREEN, BLUE) should be written successively in the COLOR VALUE REGISTER (note that three 8 bit data are required). After the last value (BLUE) the address of the PIXEL ADDRESS REGISTER is incremented automatically to reduce the write cycle for consecutive pixel color changes.

READING FROM THE LOOK-UP TABLE

The color intensity of each pixel can be read by writing the location (address of the pixel) in the look-up table via PIXEL ADDRESS REGISTER B. The color values (intensity) of each color gun (RED, GREEN, BLUE) can be accessed from the COLOR VALUE REGISTER (note that, three consecutive reads are required to complete the read cycle). After reading the last value (BLUE) the PIXEL ADDRESS REGISTER B is incremented to reduce the read cycle for consecutive pixel reads. The read cycle can be reduced if fewer values are needed to be read by changing the PIXEL ADDRESS REGISTER B. This will terminate the previous read cycle.

AC ELECTRICAL CHARACTERISTICS

T_A=25°C , V_{CC}=5.0 V± 5% unless otherwise specified

Symbol	Parameters	Limits			Units	Conditions
		min	typ	max		
T_1	PCLK period	20		10000	nS	
T_2	PCLK jitter			±2.5	%	note:1
T_3	PCLK low width	6		10000	nS	
T_4	PCLK high width	6		10000	nS	
T_5	Pixel Word setup time	4			nS	note:2
T_6	Pixel Word hold time	4			nS	note:2
T_7	Blank~ setup time	4			nS	
T_8	Blank~ hold time	4			nS	
T_9	PCLK to valid DAC output	5		30	nS	note:3
T_{10}	Differential output delay			1	nS	note:4
T_{11}	Pixel clock transition time			50	nS	
T_{12}	IOW~ pulse width low	50			nS	
T_{13}	IOR~ pulse width low	50			nS	
T_{14}	Register select setup time	10			nS	
T_{15}	Register select setup time	10			nS	
T_{16}	Register select hold time	10			nS	
T_{17}	Register select hold time	10			nS	
T_{18}	Write data setup time	10			nS	
T_{19}	Write data hold time	10			nS	
T_{20}	Output turn on delay	5			nS	
T_{21}	Read enable access time			40	nS	
T_{22}	Output hold time	5			nS	
T_{23}	Output turn off delay time			20	nS	note:5
T_{24}	Successive write interval	$3*T_1$			nS	
T_{25}	Write followed by read interval	$3*T_1$			nS	
T_{26}	Successive read interval	$3*T_1$			nS	
T_{27}	Read followed by write interval	$3*T_1$			nS	
T_{28}	Write after color write	$3*T_1$			nS	note:6
T_{29}	Read after color write	$3*T_1$			nS	note:6
T_{30}	Read after color read	$3*T_1$			nS	note:6
T_{31}	Write after color read	$3*T_1$			nS	note:6
T_{32}	Read after read address write	$3*T_1$			nS	note:6
T_{33}	Write/Read enable transition time	50			nS	

ABSOLUTE MAXIMUM RATINGS

Operating supply range	5 Volts ±5%
Voltage at any pin	GND-0.3V to V_{CC}+0.3V
Storage temperature	-40°C to +150°C
Operating temperature	0°C to 70°C
Package dissipation	500mW

DC ELECTRICAL CHARACTERISTICS

T_A=25°C, V_{CC}=5.0V ± 5% unless otherwise specified

Symbol	Parameters	Limits			Units	Conditions
		min	typ	max		
V_{CC}	Operating supply	4.5	5.0	5.5	V	
I_{CC}	Operating current			190	mA	
I_{REF}	Reference current	4.0	8.8	10	mA	
V_{AO}	DAC output level	1.5			V	
I_{AO}	DAC output current	21			mA	
D_{DTD}	DAC to DAC correlation	±2			%	
D_{DIL}	DAC internal linearity	±0.5			LSB	
I_{IL}	Input Low current	-10			uA	
I_{IH}	Input High current			10	uA	
V_{IL}	Input Low level			0.8	V	
V_{IH}	Input High level	2.0			V	
V_{OL}	Output Low level pin D0-D7			0.4	V	Isink=8mA
V_{OH}	Output High level pin D0-D7		2.4		V	Isource=8mA

Note: 1
This parameter for allowed variation in the PCLK frequency but does not permit the PCLK period to vary outside the minimum and maximum values for PCLK period specified above.

Note: 2
It is required that the Pixel address input to the color look-up table be set up as a valid logic level with the appropriate setup and hold times to each rising of PCLK.

Note: 3
A valid analog output is defined when the changing analog signal is half way between its successive values. This parameter is stable with time but can vary between different devices and may vary with different DC operating conditions.

Note: 4
Between different analog outputs on the same device.

Note: 5
Measured ±200 mV from steady state output voltage.

Note: 6
This parameter allows for synchronization between operations on the microprocessor interface and the pixel stream being processed by the color lookup table.

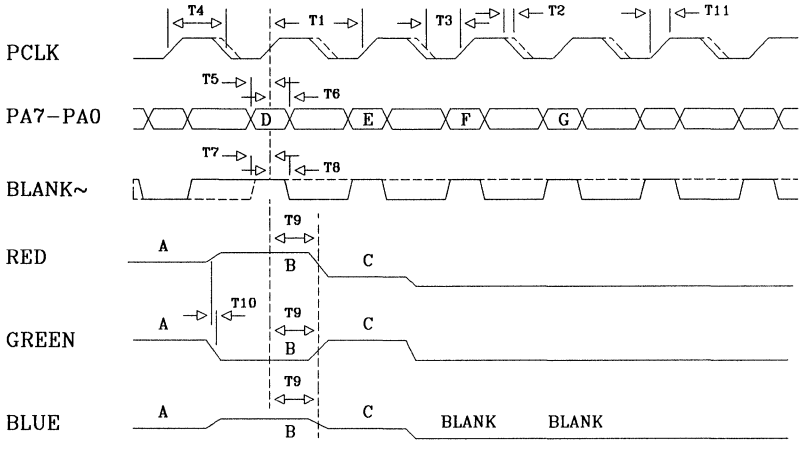
DESIGN CONSIDERATIONS

The LD1104 is fabricated in 2u CMOS technology to meet 50 MHz pixel speed requirements. Extra precautions are required to prevent damages due to electrostatic voltage discharge during handling and system manufacturing.

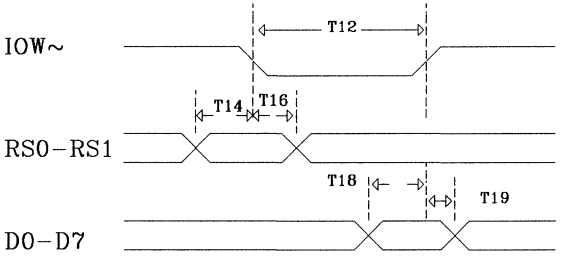
To reduce the high speed video DAC switching noises from the board or other logics, a large value capacitor (typ. 47 uF) is recommended to be connected from V_{CC} to GND pin. RGB outputs should be protected with high speed diodes going to GND and V_{CC}.

For stable output levels over the temperature variations, an active current source is recommended for IREF input connection.

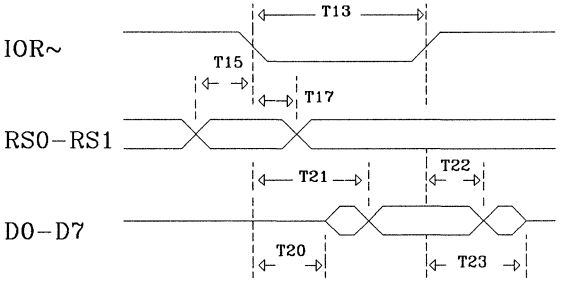
TIMING DIAGRAM



WRITE CYCLE

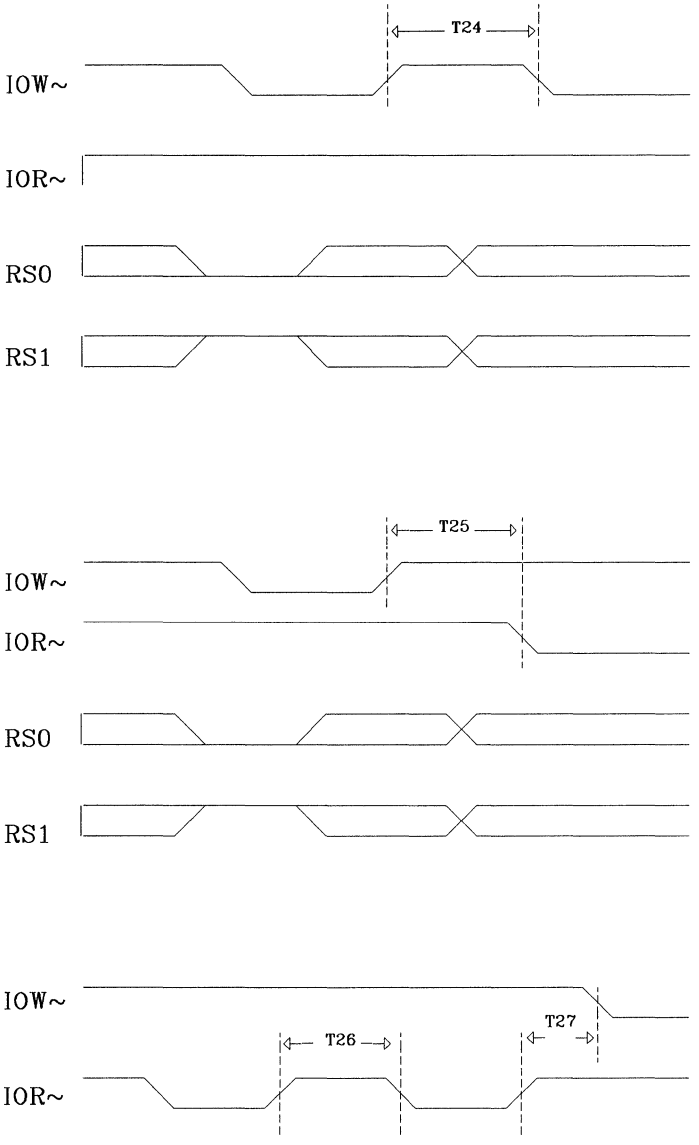


READ CYCLE



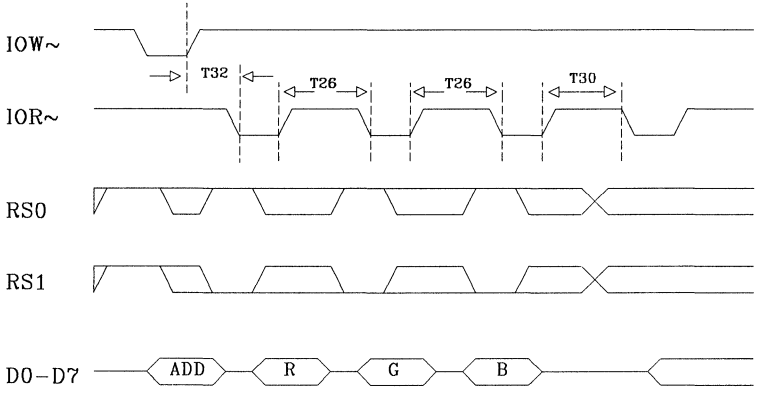
TIMING DIAGRAM

WRITE TO PIXEL MASK REGISTER FOLLOWED BY ANY ACCESS

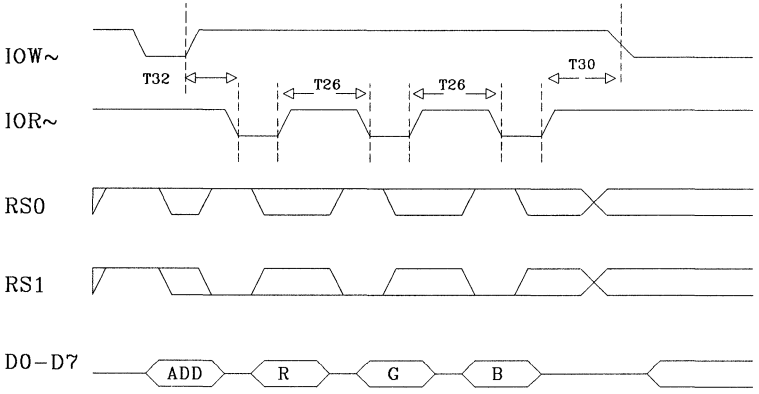


TIMING DIAGRAM

COLOR VALUE READ FOLLOWED BY ANY READ



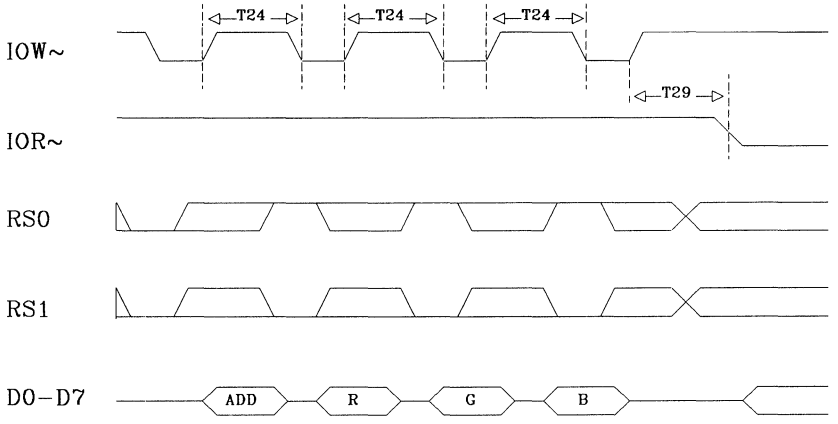
COLOR VALUE READ FOLLOWED BY ANY WRITE



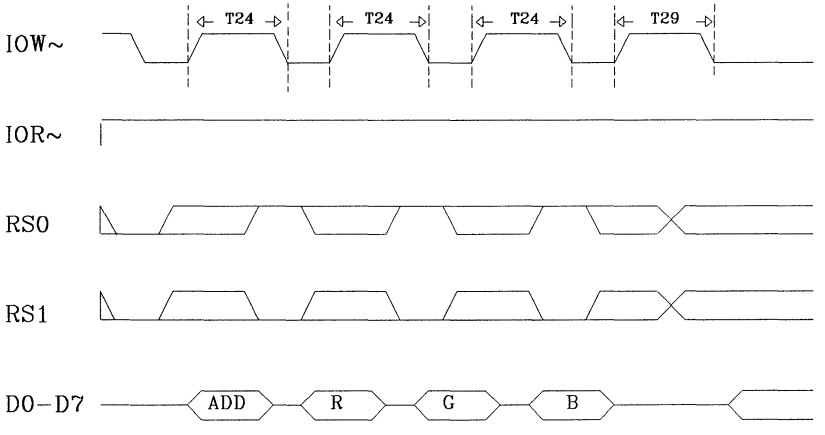
ADD=ADDRESS
R=RED
G=GREEN
B=BLUE

TIMING DIAGRAM

COLOR VALUE WRITE FOLLOWED BY ANY READ

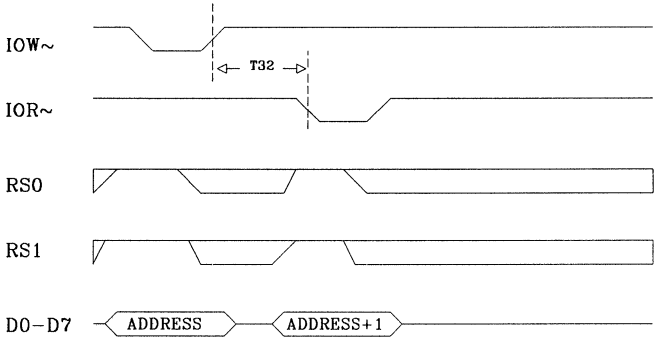


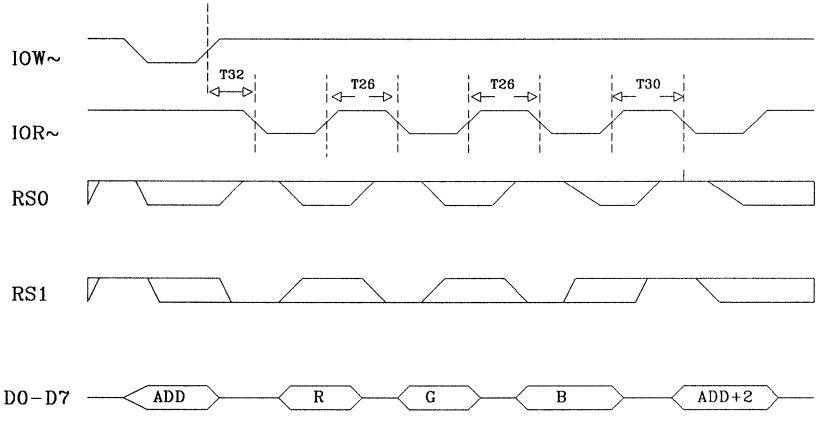
COLOR VALUE WRITE FOLLOWED BY ANY WRITE



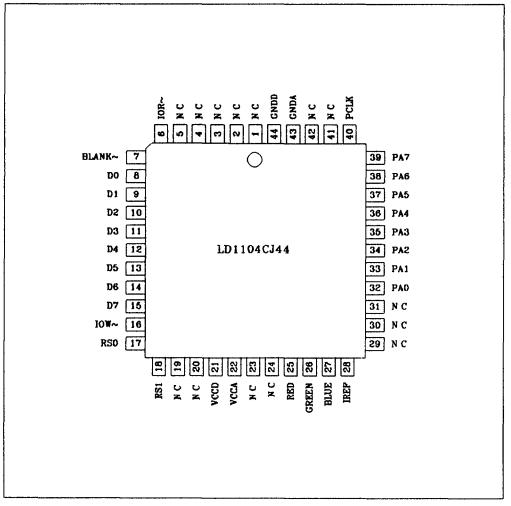
TIMING DIAGRAM

WRITE AND READ BACK ADDRESS REGISTER





44 PIN PLCC PINOUT

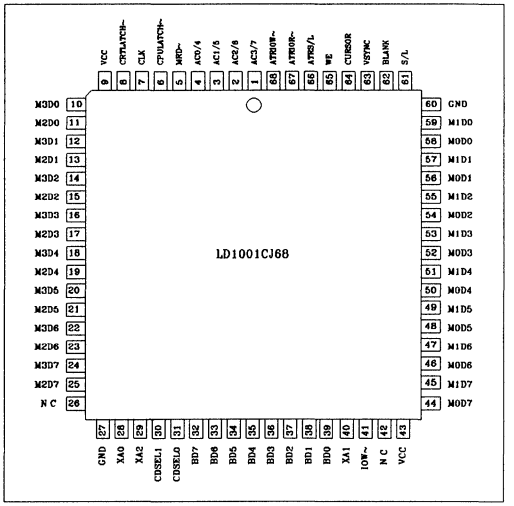


3

EGA CHIP SET

DESCRIPTION

The LD1001/1002 are EGA chip set IC's, designed to meet MDA, CGA, EGA requirements. The LD1001 is a data controller which contains the Graphics Controller 1, Graphics Controller 2, serialization, and attribute control positions of the EGA video controller. The Graphics Controller 1 and 2 control the data path and bit-level processing for video planes 0, 1, 2, 3 respectively. The LD1002 is a timing Controller which contains the CRT Controller, Light pen interface, Sequencer, Video Palette RAM and output drivers, and some Attribute Controller logic.The LD1001/LD1002 are fabricated in an advanced 2u CMOS process to achieve low drain power and high speed requirements.



FEATURES

* IBM EGA, CGA, MDA compatible
* Onboard RGB drivers
* Light pen interface
* Low power CMOS design
* 256K DRAM support
* Surface mount fabrication

APPLICATIONS

* EGA board
* High resolution Workstations

ORDERING INFORMATION

Part number	Package	Operating temperature
LD1001CJ68	PLCC	0° C to +70° C
LD1002CJ84	PLCC	0° C to +70° C

GENERAL DESCRIPTION

The LD1001 is a 68 pin PLCC data controller which supports the following functions: read masking, write data rotating, internal read data latches and Boolean logic unit for read/modify/write operations on the video memory. The Attribute serializer fetches pixel data serializes it, and sends out 4-bit color Palette address to the Timing Controller Chip. The LD1002 is an 84 pin PLCC and provides video outputs, screen refresh addresses, and arbitration between the CPU and CRT memory cycles so the screen can be redrawn without any flashing or "snow".

LD1001 SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
AC0/4 - AC3/7	1-4	O	Color palette address outputs (active high). To represent all video attributes, except for final color value.
MRD~	5	I	Memory read (avtive low). Used by CPU to read display memory in conjunction with the high going edge of the CPULATCH~ input.
CPULATCH~	6	I	CPU latch (active low). It is generated by the LD1002. The display memory data will be read into the LD1001. The low to high going edge of this signal, along with MRD~ active, will output data onto BD0-7 for a CPU memory read operation.
CLK	7	I	Clock input. This clock is used to clock the video data outputs (AC0/4 - AC3/7).
CRTLATCH~	8	I	CRT latch (active low). It is generated by the LD1002, the display memory graphics data is loaded into the LD1001 on the low to high going edge. The data in the display memory must meet set up and hold requirements. The data loaded is transferred into the Shifter Register when S/L is low.
M0D0-7		I/O	Memory data buses (three state). To send and receive data to and from the display memory.
M1D0-7		I/O	Memory data buses (three state). To send and receive data to and from the display memory.
M2D0-7		I/O	Memory data buses (three state). To send and receive data to and from the display memory.
M3D0-7		I/O	Memory data buses (three state). To send and receive data to and from the display memory.
XA0-2		I	Address lines (active high). Used to access the graphics controller register.
CDSEL0-1	30-31	O	Screen memory map controls.
BD0-7	32-37	I/O	Data bus (three state). Data is transfers from or to the LD1001 via this bus.
IOW~	41	I	Write signal (active low). Data present on BD0-7 is latched internally on the rising edge of this signal.
S/L	61	I	Shift or load. Generated by LD1002 and serves two functions. When low, the display memory is loaded into the Shifter. When high, it is shifted by one bit per clock.

LD1001 SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
BLANK	62	I	Composite blanking input. (active high). If CURSOR is high during the falling edge of BLANK , the following line will have an underline attribute.
VSYNC	63	I	Vertical sync input (active high). Increments the video blank and cursor blank counters.
CURSOR	64	I	Cursor. It indicates a valid cursor position when the display is active, and if CURSOR is high during the falling edge of BLAK, it indicates that the next line is to be underlined.
WE	65	I	Write enable (active high). When it is active, the display memory data is output on the M0D0-7, M1D0-7, M2D0-7, and M3D0-7 data buses. When WE is low, these data buses are three stated.
ATRS/L	66	I	Attribute Shift/Load. Used by the attribute controller section to load new pixel data during alphanumeric modes. When low, new pixel data is loaded; when high the data is shifted out.
ATRIOR~	67	I	Attribute controller I/O Read strobe (active low). It is used to read the STATUS 1 Register. This input also resets the attribute controller input to address (index) mode.
ATRIOW~	67	I	Attribute controller I/O Write strobe (active low). It is used to write to the attribute controller registers.
VCC	9,43	I	Most positive supply voltage.
GND	27,60	O	Signal ground.

LD1002 SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
A0-7	78-1	I	Address lines. Used to address control registers and screen RAM.
CRTINT~	8	O	CRT interrupt (open drain). If it is enabled, will go low when Vertical sync occurs
HSYNC	9	O	Horizontal retrace (active high).
VSYNC	10	O	Vertical retrace (active high).
BLANK	12	O	Composite blanking output (active high). Is used to blank the screen.
CURSOR	13	O	Cursor. It indicates a valid cursor position when the display is active, and if CURSOR is high during the falling edge of BLANK, it indicates that the next line is to be underlined.
BD0-7	14-21	I/O	Data buses (three state).
B, G, R	22-24	O	Color outputs (active high). Are the primary Red, Green, and Blue color outputs.
B', G', R'	25-27	O	Secondary color outputs (active high). In 4 bit color mode, G~ is the only one used. In monochrome mode, B~ is the video output, and G~ is the Intensity control.
RAS0-3~		O	Row address strobes (active low). To enable the screen memory planes.
IOCHRDY~	33	O	I/O ready(open drain, active low). Inserts the "wait states" to synchronize the CPU cycle to the screen RAM cycle. This single is only active during screen memory read or write cycles.
WE	34	O	Write enable (active high). Indicates that the current memory cycle will be a write cycle.
CPULATCH~	35	O	CPU latch (active low). Is used to latch screen memory for a pending CPU read cycle.
CAS~	36	O	Column address strobe (active low). To enable screen memory planes.
CLK	37	O	Video clock output. Used to clock video data through the LD1001. Depending on register initialization, this output will either follow DOTCLK, or DOTCLK divide by two.
AC0/4 - AC3/7	38-41	I	Palatte address inputs (active high).
DOTCLK	42	I	Clock input. This clock input is used internally as a master clock.

LD1002 SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
ATRS/L	43	O	Pixel load. Used by LD1001 to load new pixel data during alpha-numeric modes.
S/L	44	O	Shift load. Used by the LD1001 to load pixel data from the screen RAM during graphics modes.
VMEMR~	45	I	Video memory read request (active low). Requests a screen RAM read cycle.
VMEMW~	46	I	Video memory write request (active low). Initiates a write cycle to screen RAM.
M1D3	49	I	Plane 2 RAM select. This line selects which of the banks of RAM in plane 2 is currently in used as the font plane.
OEMX1~	50	O	Multiplexer 1 output enable (active low). To enable the external latch to drive the address bus for planes 2 and 3 during alphanumeric modes.
OEMX2~	51	O	Multiplexer 2 output enable (active low). To enable the external latch to drive the address bus for planes 2 and 3 during alphanumeric modes.
CRTLATCH~	53	O	CRT latch (active low). Is used to latch memory LD1001 for CRT display cycles.
BA0-7	61-54	O	Address bus for memory planes 2 and 3.
AA0-7	69-62	O	Address bus for memory planes 0 and 1.
A000	70	I	Memory address control input. It is used to select different address sources for screen address bit-0 during CPU cycle.
LPEN~	72	I	Light pen input strobe(Active on the falling edge). This signal is used to latch the current screen refresh address into the light pen registers of the CRTC section of the LD1002.
IOG	73	I	I/O enable (active high). Provides external decoding of address bits higher than A7. When low the internal I/O mapped registers are deactivated.
IOR~	75	I	I/O read strobe (active low). Is used to enable the data bus (BD0-7) drivers.
IOW~	76	I	I/O write strobe (active low). Data present on the BD0-7 is latched internally on the rising edge of this signal.
RESET	77	I	Reset input (active high).

LD1002 SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
A0-7	78-1	I	Address lines. Used to address control registers and screen RAM.
A8-16		I	Address lines. Used only for screen RAM accesses. Are ignored during control register accesses.
VCC	11,52	I	Most positive supply voltage.
GND	31,74	O	Signal ground.

LD1001/1002 PROGRAMMING TABLE

Description	Port Address	Index	Conditions
ATTRIBUTE CONTROL REGISTER			
Index Register	$C0, C1		IOG = high
Palette color 0	$C0, C1	$00	
Palette color 1	$C0, C1	$01	
Palette color 2	$C0, C1	$02	
Palette color 3	$C0, C1	$03	
Palette color 4	$C0, C1	$04	
Palette color 5	$C0, C1	$05	
Palette color 6	$C0, C1	$06	
Palette color 7	$C0, C1	$07	
Palette color 8	$C0, C1	$08	
Palette color 9	$C0, C1	$09	
Palette color 10	$C0, C1	$0A	
Palette color 11	$C0, C1	$0B	
Palette color 12	$C0, C1	$0C	
Palette color 13	$C0, C1	$0D	
Palette color 14	$C0, C1	$0E	
Palette color 15	$C0, C1	$0F	
Mode control	$C0, C1	$10 or $30	
Overscan (border) color	$C0, C1	$11 or $31	
Color plane enable	$C0, C1	$12 or $32	
Horizontal pixel panning	$C0, C1	$13 or $33	

LD1001/1002 PROGRAMMING TABLE

Description	Port Address	Index	Conditions
MISCELLANEOUS OUTPUT REGISTER			
Misc. output register	$C2, C3		
SEQUENCER INDEX REGISTER			
Sequencer index register	$C4		
Reset control	$C5	$00	
Clocking mode	$C5	$01	
Plane enable	$C5	$02	
Character blank select	$C5	$03	
Memory mode	$C5	$04	
GRAPHICS CONTROLLER			
Gra. cont. 2 shadow	$CA		
Gra. cont. 1 and 2 index	$CE		
Mode register shadow	$CF	$05	
Misc. shadow	$CF	$06	
LIGHT PEN			
Light pen clear	$DB		
Light pen set	$DC		
CRT CONTROL REGISTERS			
Index Register	$3x0, 2, 4, 6		x=B Monochrome
Horizontal total	$3x1, 3, 5, 7	$00	x=D Color
Horizontal display end	$3x1, 3, 5, 7	$01	
Start horizontal blank	$3x1, 3, 5, 7	$02	
End horizontal blank	$3x1, 3, 5, 7	$03	
Start horizontal retrace	$3x1, 3, 5, 7	$04	
End horizontal retrace	$3x1, 3, 5, 7	$05	
Vertical total	$3x1, 3, 5, 7	$06	
Overflow	$3x1, 3, 5, 7	$07	
Preset row scan	$3x1, 3, 5, 7	$08	
Max scan line	$3x1, 3, 5, 7	$09	
Cursor start	$3x1, 3, 5, 7	$0A	
Cursor end	$3x1, 3, 5, 7	$0B	
Start address high	$3x1, 3, 5, 7	$0C	
Start address low	$3x1, 3, 5, 7	$0D	
Cursor location high	$3x1, 3, 5, 7	$0E	
Vertical retrace start	$3x1, 3, 5, 7	$0F	
Light pen high	$3x1, 3, 5, 7	$10	
Vertical retrace end	$3x1, 3, 5, 7	$11	
Light pen low	$3x1, 3, 5, 7	$11	
Vertical display end	$3x1, 3, 5, 7	$12	

LD1001/1002 PROGRAMMING TABLE

Description	Port Address	Index	Conditions
Offset	$3x1, 3, 5, 7	$13	
Underline location	$3x1, 3, 5, 7	$14	
Start vertical blank	$3x1, 3, 5, 7	$15	
End vertical blank	$3x1, 3, 5, 7	$16	
Mode control	$3x1, 3, 5, 7	$17	
Line compare	$3x1, 3, 5, 7	$18	

REGISTER FUNCTIONAL DESCRIPTIONS

ATTRIBUTE INDEX REGISTER (AIR)

AIR BIT0-4:
Attribute address bits.
The address register is a pointer register located at 3C0 Hex. This register is loaded with a binary value that points to the attribute data register where data is to be written. The attribute controller does not have an address input to control selection of the index and data registers. Instead, the input mode toggles between the index and data registers on alternate accesses. To reset the mode to index register, read from port 3DA Hex when in the color modes, or read from port 3BA Hex when in monochrome mode.

AIR BIT 5:
Palette Address Source.
0=To load the Color Palette Register
1=To enable the screen data to access the color palette

AIR BIT 6-7: Not used.

PALETTE REGISTERS 00 - 0F Hex (PR)

PR BIT0-5:
Palettes.
These 6-bit registers allow dynamic mapping between the text attribute or graphics color input value and the displayed color on the CRT screen. A logical 1 selects the appropriate color. The Color Palette Register should be modified only during the vertical retrace interval to avoid glitches in the displayed image. Note that some color monitors do not have an intensity input and are only capable of displaying 8 colors. Monitors with 4 color inputs are capable of displaying 16 colors, and monitors with 6 color inputs are capable of displaying 64 colors.

PR BIT 0= Blue Video
PR BIT 1= Green Video
PR BIT 2= Red Video
PR BIT 3= Sec. Blue/Monochrome Video
PR BIT 4= Sec. Green/Intensity
PR BIT 5= Sec. Red
PR BIT 6-7=Not used.

MODE CONTROL REGISTER (MCR)

This is a write only register pointed to by the value in the Attribute Index Register. The value must be either 10 or 30 Hex before writing can take place.

MCR BIT 0:
Graphics/Alpha
0= Alphanumeric operation
1= Bit mapped graphics operation

MCR BIT 1:
Display type.
0= Monochrome display attributes
1= Color display attributes

MCR BIT 2:
Line graphics (character codes C0 - DF Hex).
For character fonts that do not use the line graphics character codes in the range of C0 - DF Hex, bit -2 of this register should be set to "0".

0= Set ninth column to the same color as the background
1= Enables the special line graphics character codes for the IBM Monochrome Display Adapter. Forces the ninth column dot of a line graphic character to be the same color as the eighth column dot of the character.

MCR BIT 3:
Blink enable.
0= Select the background intensity of the attribute input. This mode is available for compatibility with the MDA and CGA.
1 = Enable the blink attribute in graphic/alphanumeric modes

MCR BIT 4-7: Not used.

ATTRIBUTE OVERSCAN COLOR REGISTER (AOCR)

This is a write only register pointed to by the value in the Attribute Index Register. This value must be either 11 or 31 Hex before writing can take place. The processor output port address for this register is 3C0 Hex.

AOCR BIT 0-5:
Overscan color.
This 6 bit register determines the overscan (border) color displayed on the CRT screen.
0= Monochrome displays
1 = Select the appropriate color for each location

AOCR BIT 6-7: Not used.

ATTRIBUTE COLOR PLANE REGISTER (ACPR)

This is a write only register pointed to by the value in the Attribute Index Register. This value must be either 12 or 32 Hex before writing can take place.

ACPR BIT 0-3:
Color plane assignments.
0= Disable the respective display memory
1 = Enable the respective display memory

ACPR BIT 4-5:
Video Status Mux.
Selects two of the six color outputs to be available on the status port. the following table illustrates the combinations available and the color output wiring. Bit-4 of this register is also used to clear the blink control counters for both the cursor and attribute blink functions. When bit-4 is "1", the counters are cleared and the 6 color outputs are three stated.

ACPR		ISR1	
bit-5	bit-4	bit-5	bit-4
0	0	red	blue
0	1	sec. blue	green
1	0	sec. red	sec. green

ATTRIBUTE HORIZONTAL PEL PANNING REGISTER (AHPPR)

This is a write only register pointed to by the value in the Attribute index Register. This value must be either 13 or 33 Hex before writing can take place.

AHPPR BIT 0-3:
Horizontal Pel Panning.
This 4 bit register selects the number of picture elements (pel) to shift the video data to the left. Pel panning is available in both Alphanumeric and bit-mapped modes. In Monochrome Alphanumeric mode, the image can be shifted a maximum of 9 pels. In all other Alphanumeric modes and bit-mapped modes, the image can be shifted a maximum of 8 pels. The sequence for shifting the image is:

Monochrome Alphanumeric only
9 pels/char: 8,0,1,2,3,4,5,6,7

All other modes
8 pel/char: 0,1,2,3,4,5,6,7

AHPPR BIT 4-7: Not used.

MISCELLANEOUS OUTPUT REGISTER (MOR)

This is a write only register. To access this register, IOG must be high and A0-A7 must have a Hex value of C2. The IOW input is the write strobe. A high on reset will cause all bits to reset.

MOR BIT 0:
I/O address select.
This bit maps the CRTC I/O addresses 3Bx or 3Dx Hex for the IBM Monochrome or Color Graphics Monitor Adapter emulation.
0= Sets CRTC address to 3B0-7 Hex and Input Status Register 1's address to 3BA Hex for monochrome emulation.
1 = Sets CRTC address to 3D0-7 Hex and Input Status Register 1's address to 3DA Hex for Color/Graphics Monitor Adapter emulation.

MOR BIT 1-4: Not used.

MOR BIT 5:
Page bit.
Selects between two 64K pages of memory when in the Odd/Even modes (0, 1, 2, 3, 7).
0 = Selects the low page of memory
1 = Selects the high page of memory

MOR BIT 6-7: Not used.

SEQUENCER REGISTER

Description	Port Address	Index
Index reg.	C4	
Reset control	C5	0
Clocking mode	C5	1
Plane enable	C5	2
Character bank sel.	C5	3
Memory mode	C5	4

Note: Access to all registers is write only, and IOG must be high while IOW is used as a data strobe.

SEQUENCER INDEX REGISTER (SIR)

The Index register is a write only register. It points to the control register to be modified.

SIR BIT 0-4: Control register index value.

SIR BIT 5-7: Not used.

SEQUENCER RESET CONTROL REGISTER (SRCR)

The Reset Control Register is a write only register that is a accessed when an index value of 00 Hex is loaded into the Index Register.

SRCR BIT 0:
Async reset.
0 = Forces the sequencer to halt asynchronously and causes the following outputs to these state:

CRTLATCH	high
CLK	three state
ATRS/L	three state
S/L	three state
RAS 0-3	three state
WE	three state
CPULATCH	three state
CAS	three state

Note: Using this bit to halt the sequencer will result in corrupted screen memory.

1 = Start the sequencer (SRCR BIT 1 = 1)

SRCR BIT 1:
Sync reset.
This bit should be cleared before changing the clocking mode register to keep from corrupting screen memory.

0 = Forces the sequencer to halt synchronously
1 = Start the sequencer (SRCR BIT 0 = 1)

SRCR BIT 2-7: Not used.

SEQUENCER CLOCKING MODE REGISTER (SCMR)

The Clocking Mode Register is a write only register accessed by writing an Index Value of 01 Hex to the Index Register. Before modifying the contents of this register, the Sync Reset bit in the reset Control Register should be cleared. Then modification may take place, followed by resetting the Sync Reset bit.

SCMR BIT 0:
8/9 pixels.
0 = Select 9 pixel clocks for every character fetch
1 = Select 8 pixel clocks for every character fetch

SCMR BIT 1:
Bandwidth.
0 = Forces the sequencer to allow only one video memory cycle out of five for CPU access, while the remainder go for refreshing the screen.
1 = Sets the sequencer to allow 3 out of 5 accesses for the CPU. All high resolution modes (640 pixels or greater) uses the 20% Bandwidth mode (low) as the screen must have more data sent to it in a given amount of time.

SCMR BIT 2:
Shift load.
This mode can be used to chain 16 bits together in the shift register.
0 = Load video serialization logic with every character cycle
1 = Reload shifters every other character cycle

SCMR BIT 3:
Dot Clock Select.
0 = CLK signal will follow the DOTCLOCK pin
1 = CLK will be DOTCLOCK devided by 2. The divide by 2 mode is used for low resolution modes (320 x 200 and 40 character modes).

SCMR BIT 4-7: Not used.

SEQUENCER PLANE ENABLE REGISTER (SPER)

This is a write only register accessed with an Index Value of 02 Hex. It provides a write mask function on a plane by plane basis. By enabling all planes (writing a value of 0F Hex to the register), 32 bits at a time may be written by the CPU into the screen memory.

SPER BIT 0-3:
0 = Mask the plane
1 = Enable (in any bit location) the particular plane for modification

SPER BIT 4-7: Not used.

SEQUENCER CHARACTER BANK SELECT (SCBS)

This register is write only and is accessed with an Index Value of 03 Hex. This register is used in alphanumeric modes to provide a means of using more than 256 character types at a time.

SCBS BIT 0:
Character Bank select B.
Selects the bank of RAM used when the character attribute bit (M1D3 input) is low according to the following table:

D1	D0	Bank Selected
0	0	1st 8K of plane 2, Bank 0
0	1	1st 8K of plane 2, Bank 1
1	0	1st 8K of plane 2, Bank 2
1	1	1st 8K of plane 2, Bank 3

SCBS BIT 1:
Character Bank select A.
Selects the Bank of RAM used when the character attribute bit (M1D3 input) is low according to the following table:

D3	D2	Bank Selected
0	0	1st 8K of plane 2, Bank 0
0	1	1st 8K of plane 2, Bank 1
1	0	1st 8K of plane 2, Bank 2
1	1	1st 8K of plane 2, Bank 3

In alphanumeric modes, the M1D3 signal (bit 3 of the attribute byte) normally controls the foreground intensity on/off function. This bit, however, may be redefined as a switch between character sets. This function is enabled when there is a difference between the value in Char Bank Select A and Char Bank Select B. Whenever these two modes are the same, the character select function is disabled. The memory mode register bit 1 must be set high (indicating a full 256K of screen RAM), otherwise Bank 0 will be the only Bank selected, even if non-zero values are in this register.
The Async Reset clears this register. async Reset should only be done during a system reset.

SCBS BIT 4-7: Not used.

SEQUENCER MEMORY MODE REGISTER (SMMR)

This is a write only register accessed with an Index Value of 04 Hex.

SMMR BIT 0: Not used.

SMMR BIT 1:
Extended Memory.
0 = Expansion memory card is not installed
1 = Expansion memory card is installed and enables access to memory through address bits 14 and 15.

SMMR BIT 2:
Odd/Even.
0 = Directs Even processor addresses to access maps 0 and 2, while Odd CPU addresses access maps 1 and 3.
1 = access data sequentially within a bit map. The maps are accessed according to the value in the map mask register.

SMMR BIT 3-7: Not used.

GRAPHICS CONTROLLER REGISTER (GCR)

This is a write only register, and IOG must be high to allow further address decoding externally. IOW is the data strobe.

Description	Port Address	Index
Graphics 1 pos.	CC	
Graphics 1 pos.	CE	
Mode Register	CF	05
Miscellaneous	CF	06*

* Position dependent register, data written to this register will be invalid if wrong values are written to the Graphics 1 position register.

GRAPHICS 1 POSITION REGISTER (G1PR)

G1PR BIT 0-1:
Position Address.
These 2 bits are binary encoded hierarchy bits for the graphics controller 1 section. The position register controls which 2 bits of the processor data bus the section responds to. This register must be programmed with a value of 00 Hex for correct EGA operation.

G1PR BIT 2-7: Not used.

GRAPHICS 1 INDEX REGISTER (G1IR)

The processor port address for this register is 3CF Hex.

G1IR BIT 0-3:
Register Index.
The value written into this register is used to access the remaining registers in the Graphics 1 section.

G1IR BIT 4-7: Not used.

GRAPHICS CONTROLLER MODE REGISTER (GCMDR)

This is a write only register and is accessible when the value in the Graphics 1 Index Register is 05 Hex. The processor port address for this register is 3CF Hex.

GCMDR BIT 0-1: Not used.

GCMDR BIT 2:
Test Condition.
0 = Normal.
1 = Forces the Graphics and Chain internal signal to a logic "1".

GCMDR BIT 3-7: Not used.

GRAPHICS CONTROLLER MISCELLANEOUS REGISTER (GCMSR)

This is a write only register and is accessible when the value in the Graphics 1 Index Register is 06 Hex.

GCMSR BIT 0:
Graphics Mode.This bit controls alpha mode addressing.
0 = Normal.
1 = Selects Graphics mode addressing, which disables the character address latches, and sends identical addressing to both AA0-7 and BA0-7 Hex busses.

GCMSR BIT 1:
Chain Odd to Even.
0 = Normal.
1 = Directs the processor address bit 0 to be replaced by higher order bit. Odd/Even planes will be selected by the value of the processor A0 bit.

GCMSR BIT 2-7: Not used.

LIGHT PEN CLEAR (LPC)

This is a write only register that is used to clear the light pen input latch. Data written is ignored, so anything can be written. This register is accessed when IOG is High, DB Hex is on the A0-7 bus, and IOW is strobed.

LIGHT PEN SET (LPS)

This write only register is used to set the light pen input latch. Data written is ignored, so anything can be written. This register is accessed when IOG is high, DC Hex is on the A0-7 bus, and IOW is strobed.

CRT CONTROLLER INDEX REGISTER (CCIR)

The CRT Controller Index Register is a pointer register at the addresses 3B0, 3B2, 3B4 and 3B6 Hex in Monochrome modes, and 3D0, 3D2, 3D4 and 3D6 Hex in Color modes. This is a write only register.

CCIR BIT 0-4:
Index.
The binary coded value written to this register defines the address of the actual control register to be accessed.

CCIR BIT 5-7: Not used.

CRT CONT. HORIZ. TOTAL REGISTER (CCHTR)

This write only register is accessed when the value written to the CRT Controller Index Register is 00 Hex. The addresses that may be used to access this register are 3B1, 3B3, 3B5 and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

CCHTR BIT 0-7:
Horizontal total.
This register sets the total number of character fetches in a horizontal scan period, including both active and blanked times. This register directly controls the horizontal scan frequency that is set to the CRT display. The value loaded in this register should be the total number of fetches desired less 2.

CRT CONT. HORIZ. DISPLAY ENABLE END REGISTER (CCHDER)

This is a write only register accessed when the value written to the CRT Controller Index Register is 01 Hex. The addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

CCHDER BIT 0-7:
Horizontal enable end.
This register defines the length of the the horizontal display enable function, which determines the number of characters (or pels) that are displayed horizontally. The value written here should be one less that the desired number of characters to be displayed.

CRT CONT. START HORIZ. BLANKING REGISTER (CCSHR)

This is a write only register accessed when the value written to the CRT Controller Index Register is 02 Hex. The addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

CCSHR BIT 0-7:
Start horizontal blanking register.
This register controls when the Horizontal Blanking signal goes active. The Horizontal Blanking signal goes active when the Horizontal character count is equal to the value in this register. The underline scan line output is multiplexed on the CURSOR output pin, and will be active for one character clock cycle beyond the end of the blanking signal.

CRT CONT. END HORIZ. BLANKING REGISTER (CCEHR)

This is a write only register accessed when the value written to the CRT Controller Index Register is 03 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

CCEHR BIT 0-4:
End horizontal blanking.
These 5 bits control the length of the Horizontal Blanking signal in character clock increments. The value to be loaded into this register should be equal to the number of clock cycles to be blanked added to the value of the five least significant bits of the Start Horizontal Blanking register.

CCEHR BIT 5-6:
Display enable skew control.
These bits determine the amount of the skew in the Display Enable signal. Skew control is required to provide enough time for the CRT Controller to access the Display Buffer for a character and attribute code, access the font plane, and go through the Horizontal Panning register (in Attribute Controller section) to the character shift registers in the Attribute Controller section. Each alpha mode access requires that the Display Enable signal be skewed by one character cycle so that the video is properly aligned with the horizontal and vertical sync signals. Skew Control encoding is a follows:

BIT-6	BIT-5	
0	0	Zero character clock skew
0	1	One character clock skew
1	0	Two character clock skew
1	1	Three character clock skew

CCEHR BIT 7: Not used.

CRT CONT. START HORIZ. RETRACE REGISTER (CCSRR)

This is a write only register accessed when the value written to the CRT Controller Index Register is 04 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

CCSRR BIT 0-7:
Start horizontal retrace.
This register controls the time that the horizontal sync signal goes active. Varying this value can be used to center the image on the screen. The value loaded to this register must be equal to the character clock value at which the signal should go active.

END HORIZ. RETRACE REGISTER (EHRR)

This is a write only register accessed when the value written to the CRT Controller Index Register is 05 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

EHRR BIT 0-4:
End horizontal retrace.
These 5 bits control the duration of the HSYNC signal. The value written to this register should be equal to the desired length of the HSYNC pulse (in character clock cycles) added to the 5 least significant bits of the Start Horizontal Retrace Register.

EHRR BIT 5-6:
Horizontal retrace delay.
These bits control the skew of the horizontal sync signal (HSYNC) in character clock cycle increments. The 2 bit value is binary encoded, and writing a 00 Hex will cause the CRT Controller to produce an HSYNC with a skew of zero character clock cycle.

HERR BIT 7:
Start Odd memory address.
This bit controls whether the first screen memory fetch after a horizontal retrace is from an Even or an Odd address. This bit can be useful in horizontal panning applications. Normally it should be set to "0".
0 = Even address
1 = Odd address

CRT CONT. VERTICAL TOTAL REGISTER (CCVTR)

This is a write only register accessed when the value written to the CRT Controller Index Register is 06 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

CCVTR BIT 0-7:
Vertical total.
This register is used to control the total number of horizontal lines that are scanned during a vertical frame, including both active and blanked times. The value used is a 9 bit value. The 8 LSB's are written to this register, and the MSB is written to bit 0 of the CRT Controller Overflow Register. This register determines the Vertical Scan Frequency sent to the Crt display.

CRT CONTROLLER OVERFLOW REGISTER (CCOR)

This is a write only register accessed when the value written to the CRT Controller Index Register is 07 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

CCOR BIT 0-5:
Overflow.
This register contains the 9th bit (MSB's) for the listed control registers. The bits are used in conjunction with the registers to control their functions using 9 bits.

CCOR BIT 0: Vertical Total Bit 8.
CCOR BIT 1: Vertical Display Enable End Bit 8.
CCOR BIT 2: Vertical Retrace Start Bit 8.
CCOR BIT 3: Start Vertical Blank Bit 8.
CCOR BIT 4: Line Compare Bit 8.
CCOR BIT 5: Cursor Location Bit 8.

CCOR BIT 6-7: Not used.

CRT CONT. PRESET ROW SCAN REGISTER (CCPSR)

This is a write only register accessed when the value written to the CRT Controller Index Register is 08 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

CCPSR BIT 0-4:
Preset row scan.
This register is used to control the starting row scan count after a vertical retrace. The row scan counter is incremented each horizontal retrace time, until a maximum row scan occurs. This register is useful for doing smooth scrolling in alphanumeric modes.

CCPSR BIT 5-7: Not used.

CRT CONT. MAXIMUM SCAN LINE REGISTER (CCMSR)

This is a write only register accessed when the value written to the CRT Controller Index Register is 09 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

CCMSR BIT 0-4:
Maximum scan line.
This register controls the number of scan lines per character row. The value to be written must be the character cell height (in lines) minus one.

CCMSR BIT 5-7: Not used.

CRT CONT. CURSOR START REGISTER (CCCSR)

This is a write only register accessed when the value written to the CRT Controller Index Register is 0A Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

CCCSR BIT 0-4:
Cursor start.
This register controls which row within the character cell is where the cursor is to begin. The value to be written must be one less than the desired row number.

CCCSR BIT 5-7: Not used.

CRT CONT. CURSOR END REGISTER (CCER)

This is a write only register accessed when the value written to the CRT Controller Index Register is 0B Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

CCER BIT 0-4:
Row scan cursor end.
These bits are used to control the location within the character cell where the cursor goes inactive. The value written here should be equal to the character cell row number desired.

CCER BIT 4-6:
Cursor skew.
These 2 bits control the amount of skew (in character clock cycles) in the cursor signal. This values affects only the cursor and not the underline function, which is multiplexed on the same CURSOR line. Encoding for these bits is as follows:

BIT-6	BIT-5	
0	0	Zero character clock cycle
0	1	One character clock cycle
1	0	Two character clock cycle
1	1	Three character clock cycle

CCER BIT 7: Not used.

CRT CONT. START ADDRESS HIGH REGISTER (CSHR)

This is a read/write register accessed when the value written to the CRT Controller Index Register is 0C Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

CSHR BIT 0-7:
Start address high
This register contains the 8 high-order bits of a 16 bit value indicating the first address fetched from screen memory after a vertical retrace.

CRT CONT. START ADDRESS LOW REGISTER (CCSLR)

This is a read/write register accessed when the value written to the CRT Controller Index Register is 0D Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

CCSLR BIT 0-7:
Start address low.
This register contains the 8 low-order bits of a 16 bit value indicating the first address fetched from screen memory after a vertical retrace.

CRT CONT. CURSOR LOC. HIGH REGISTER (CCLHR)

This is a read/write register accessed when the value

written to the CRT Controller Index Register is 0E Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

CCLHR BIT 0-7:
Cursor location high.
This register contains the 8 high-order bits of a 16 bit value indicating the cursor location as referenced to the screen memory address. This allows hardware panning and scrolling through the screen memory while the cursor remains in the same location.

CRT CONT. CURSOR LOC. LOW REGISTER (CCLLR)

This is a read/write register accessed when the value written to the CRT Controller Index Register is 0F Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

CCLLR BIT 0-7:
Cursor location low.
This register contains the 8 low-order bits of a 16 bit value indicating the cursor location as referenced to the screen memory address. This is used together with the CRT Controller Cursor Location Low Register.

CRT CONT. VERTICAL RETRACE START REGISTER (CCVRR)

This is a write only register accessed when the value written to the CRT Controller Index Register is 10 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

CCVRR BIT 0-7:
Vertical retrace start.
This register is the lower 8 bits of the 9 bit value controlling the start of the Vertical Sync (VSYNC signal). This value is in horizontal scan lines. The 9th bit (MSB) of this value is written to bit 2 of the CRT Controller Overflow Register.

CRT CONT. LIGHT PEN HIGH REGISTER (CLHR)

This is a read only register accessed when the value written to the CRT Controller Index Register is 10 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

CLHR BIT 0-7:
Light pen high.
This register contains the 8 MSB's of the screen memory address being fetched when the LPEN input is triggered.

CRT CONT. VERTICAL RETRACE END REG. (CVRER)

This is a write only register accessed when the value written to the CRT Controller Index Register is 11 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

CVRER BIT 0-3:
Vertical retrace end.
These 4 bits determine the duration of the vertical sync signal (VSYNC output). The value written must equal the duration of the sync (in number of horizontal lines) added to the 4 LSB's of the Start Vertical Retrace Register.

CVRER BIT 4:
Vertical interrupt.
0 = Disable the vertical interrupt
1 = Enable the vertical interrupt

CVRER BIT 5:
Enable vertical interrupt output.
0 = Enable the vertical interrupt output
1 = Disable the vertical interrupt output

CVRER BIT 6:
Functional test mode.
0 = Normal operation
1 = Test mode

CVRER BIT 7: Not used.

CRT CONT. LIGHT PEN LOW (CCLPL)

This is a read only register accessed when the value written to the CRT Controller Index Register is 11 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

CCLPL BIT 0-7:
Light pen.
This register contains the 8 LSB's of the screen memory address being fetched when the LPEN input is triggered.

CRT CONT. VERT. DISPLAY ENABLE END REG. (CVDEG)

This is a write only register accessed when the value written to the CRT Controller Index Register is 12 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

CVDEG BIT 0-7:
This register has the lower 8 bits of the 9 bit value defining the location (in number of horizontal screen lines) where the vertical display enable goes inactive. The MSB of this value is in bit 1 of the CRT Controller Overflow Register.

CRT CONTROLLER OFFSET REGISTER (COR)

This is a write only register accessed when the value written to the CRT Controller Index Register is 13 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

COR BIT 0-7:
This register controls the logical line width of the display memory. The value written to this register controls the address offset of the character or pel directly beneath any other pixel. Depending on the clocking method selected, the address may be either a word or double word address.

CRT CONT. UNDERLINE LOC. REGISTER (CCULR)

This is a write only register accessed when the value written to the CRT Controller Index Register is 14 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

CCULR BIT 0-4:
This register controls the line within the character cell where an underline will appear. The value in this register must be one less than the screen line desired.

CCULR BIT 5-7: Not used.

CRT CONT. START VERT. BLANKING REG. (CSVBR)

This is a write only register accessed when the value written to the CRT Controller Index Register is 15 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

CSVBR BIT 0-7:
This register contains the 8 LSB's of a 9 bit value describing the horizontal screen line count at which the vertical blanking function goes active. The MSB is in bit-3 of the CRT Controller Overflow Register.

CRT CONT. END VERT. BLANKING REG. (CEVBR)

This is a write only register accessed when the value written to the CRT Controller Index Register is 16 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

CEVBR BIT 0-4:
This register controls the vertical blanking duration by setting the screen count value for when the vertical blank output becomes inactive. The value to be written here should be the desired blanking width (in horizontal lines) added to the bottom 5 bits of the value in the Start Vertical Blanking Register.

CRT CONT. MODE CONTROL REGISTER (CMCR)

This is a write only register accessed when the value written to the CRT Controller Index Register is 17 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

CMCR BIT 0:
Compatibility mode support .
0 = Row scan counter bit-0 is substituted for memory address bit 13, allowing compatibility with CGA's method of addressing screen memory.
1 = Normal.

CMCR BIT 1:
Select row scan count.
0 = Selects row scan counter bit-1 as address bit 14 for

the screen referesh address bus.
1 = Select address counter bit-14.

CMCR BIT 2:
Horizontal retrace select.
This selects either horizontal retrace or horizontal retrace divided by two as the clock that increaments the vertical resolution of the CRTC, since the 9 bit vertical timing counter can only operate up to 512 counts. By selecting the count by two option, the vertical displayed resolution can be doubled to 1024 lines.
0 = Selects horizontal retrace.
1 = Selects horizontal retrace divided by two.

CMCR BIT 3:
Count by two.
This bit controls the incrementing of the address counter.
0 = Increment address counter with every character clock cycle.
1 = Increment address counter with every second character cycle.
This is used to generate either a byte or word address for the screen memory.

CMCR BIT 4:
Output control.
0 = Enable HSYNC, VSYNC, CURSOR, and BLANK outputs.
1 = Set HSYNC, VSYNC, CURSOR, and BLANK outputs to three state.

CMCR BIT 5:
Address wrap.
This bit selects the memory address counter bit 13 or 15 to appear on the memory address bus as the LSB (A0) during Word Mode. If not in Word Mode, the state of this bit has no effect.
0 = Set for 64K configuration.
1 = Set for 256K configuration.

CMCR BIT 6:
Word/Byte mode.
0 = Word mode. This causes the memory address conter bits to be shifted down one bit on the memory address bus, With the MSB of the counter appearing on the new LSB of that address bus.
1 = Byte mode.

CMCR BIT 7:
Hi-resolution.
0 = Clear the horizontal and vertical traces.
1 = Enable the horizontal and vertical timing counters.

CRT CONT. LINE COMPARE REGISTER (CLCR)

This is a write only register accessed when the value written to the CRT Controller Index Register is 18 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

CLCR BIT 0-7:
This register is used to implement a split-screen function. When the vertical counter reaches this value, the address counters are cleared. Thus allowing a section of the screen to be immune to scrolling. The value loaded to this register is the 8 LSB's of a 9 bit value. The MSB is bit-4 of the CRT Controller Overflow register.

ATTRIBUTE CONTROL REGISTERS

Description	Decode Pin	Index
Index reg.	ATRIOW	
Mode Cont.	ATRIOW	10 or 30 Hex
Color Plane Enable	ARRIOW	12 or 32 Hex

ATTRIBUTE CONTROL INDEX REGISTER (ACIR)

This is a write only register

ACIR BIT 0-4:
Attribute register index value.
This address register is a pointer register accessed when ATRIOW is low. This register is loaded with a binary value that points to the attribute data register where data is to be written. The Attribute Controller does not have an address bit input to control selection of the Index and Data registers. Instead, the input mode toggles between Index Register and Data Register access modes on alternate accesses. To reset the Input mode to the Index Register, the STRIOR pin should be strobed active (low).

ACIR BIT 5:
Palette address source.
0 = To load color palette register.
1 = To enable the screen data to access the color palette.

ACIR BIT 6-7: Not used.

ATTRIBUTE CONT. MODE CONTROL REG. (ACMCR)

This is a write only register pointed to by the value in the Attribute Index Register. The value must be either 10 or 30 Hex before writing can take place. The processor output port for this register is 3C0 Hex.

ACMCR BIT 0:
Graphics/Alpha mode.
0 = Alphanumeric mode.
1 = Graphics mode.

ACMCR BIT 1: Not used.

ACMCR BIT 2:
Line graphics.
0 = The 9th column dot will be the same color as the background.
1 = Enables the special line graphics character codes for IBM Monochrome Display Adapter. Sets the 9th column dot of a line graphics character code to the same color as the 8th column dot of the character. The line graphics character codes are C0 through DF Hex.

ACMCR BIT 3:
Blank enable.
0 = Selects the background intensity of the attribute input. This mode was available on the MDA and CGA.
1 = Enable the blink attribute in alphanumeric or graphics modes.

ACMCR BIT 4-7: Not used.

ATTRIBUTE CONT. COLOR PLANE ENABLE REG. (ACPER)

This is a write only register pointed to by the value in the Attribute Index Register. The value must be either 12 or 32 Hex before writing can take place. The processor output port for this register is 3C0 Hex.

ACPER BIT 0-3: Not used.

ACPER BIT 4:
Video status mux 0.
0 = Resume counting operation. This does not enable the blinking function it only enables the blinking counters.
1 = Clear the blink counter and stop counting.

ACPER BIT 5-7: Not used.

GRAPHICS CONT. GRAPHICS 1 POSITION REG. (GC1PR)

This is a write only register. The processor output port address for this register is 3CC Hex.

GC1PR BIT 0-1:
These 2 bits are binary encoded hierarchy bits for the graphics controller 1 section. The position register controls which 2 bits of the processor data bus the section responds to. This register must be programmed with a value of 00 Hex for correct EGA operation.

GC1PR BIT 2-7: Not used.

GRAPHICS CONT. GRAPHICS 2 POSITION REG. (GC2PR)

This is a write only register. The processor output port address for this register is 3CA Hex.

GC2PR BIT 0-1:
These 2 bits are binary encoded hierarchy bits for the graphics controller 2 section. The position register controls which 2 bits of the processor data bus the section responds to. This register must be programmed with a value of 01 Hex for correct EGA operation.

GC2PR BIT 2-7: Not used.

GRAPHICS CONT. GRAPHICS 1 & 2 INDEX REGISTER (GC12R)

This is a write only register.

GC12R BIT 0-3:
The value written into this register is used to access the remaining registers in the graphics 1 & 2 section.

GC12R BIT 4-7: Not used.

GRAPHICS CONT. SET/RESET REGISTER (GSRR)

This is a write only register pointed to by the value in the Graphics Controller 1 and 2 Index Register. The value must be 00 Hex before writing can take place.

GSRR BIT 0-3:
These bits represent the value written to the respective memory planes when the processor does a memory write with write mode "0" selected and set/reset enabled. Set/Reset can be enabled on a plane by

plane basis by using the Enable Set/Reset Register.
0 = Reset
1 = Set

GSRR BIT 4-7: Not used.

GRAPHICS CONT. ENABLE SET/RESET REG. (GSERR)

This is a write only register and is accessible when the value in the Graphics 1 & 2 Index Register is 01 Hex.

GSERR BIT 0-3:
These bits enable the Set/Reset function for the respective memory planes. When high, the data in the respective Set/Reset bits are written into the memory. When low, processor data is written directly to memory for those bit locations. The Set/Reset function only works in write mode 00 Hex.

GSERR BIT 4-7: Not used.

GRAPHICS CONT. COLOR COMPARE REG. (GCCR)

This is a write only register and is accessible when the value in the Graphics 1 & 2 Index Register is 02 Hex.

GCCR BIT 0-3:
These bits represent a 4 bit (one per plane) color to be compared. If read mode "1" is selected, the data returned from a memory read operation will contain a "1" in each bit position where the memory data in each plane is equal to the value in this register.

GCCR BIT 4-7: Not used.

GRAPHICS CONTROLLER DATA ROTATE REG. (GCDRR)

This is a write only register and is accessible when the value in the Graphics 1 & 2 Index Register is 03 Hex.

GCDRR BIT 0-3:
Rotate count.
The value written to these locations will determine the number of bit data will be shifted left during write mode "0" memory write operations.

GCDRR BIT 3-4:
Function select.
Data written to memory can operate logically with data already in the processor latches. Data may be any of the choices selected by the Write Mode Register except processor latches. If rotated data is selected, the rotate applies before the logical function. The function codes are defined as follows:

BIT-4	BIT-3	
0	0	Data unmodified
0	1	Data AND'ed with latched data
1	0	Data OR'ed with latched data
1	1	Data XOR'ed with latched data

GCDRR BIT 5-7: Not used.

GRAPHICS CONT. READ MAP SELECT REG. (GRMSR)

This is a write only register and is accessible when the value in the Graphics 1 & 2 Index Register is 04 Hex.

GRMSR BIT 0-2:
Map select 0-2.
These bits represent an encoded value of the memory plane number from which the processor will read data. This register has no effect on the color compare read mode operation.

GRMSR BIT 3-7: Not used.

GRAPHICS CONTROLLER MODE REGISTER (GCMR)

GCMR BIT 1-0:
Write Mode.
00 = Write Mode "0", each of the 4 planes is written with the CPU date rotated left by the value in the Rotate Register. This is always true, except when the Set/Reset Register in enabled, in which case that plane would be written by the nono-rotate value in the Set/Reset Register.
01 = Write Mode "1", each plane is written with the data read from the planes by the previous memory read operation.
10 = Write Mode "2", memory planes 0-3 are filled with the values of data bits 0-3 respectively.
11 = Non valid condition.

GCMR BIT 2:
Test condition.
0 = Normal.
1 = Set internal signals of C0-3, Graphics, and Chain to logic "1".

GCMR BIT 3:
Read Mode.
0 = Normal memory read.
1 = Results of color compare operation (memory read cycles).

GCMR BIT 4:
Odd/Even.
0 = Normal
1 = Select the Odd/Even addressing mode, used for CGA emulation modes.

GCMR BIT 5:
Shift register mode.
0 = Normal.
1 = Direct the shift registers in each graphics section to format the serial stream with even numberd bits to the even numbered maps and odd numbered bits to the odd numbered maps.

GCMR BIT 6-7: Not used.

GRAPHICS CONT. MISCELLANEOUS REG. (GCMSR)

This is a write only register and is accessible when the value in the Graphics 1 & 2 Index Register is 06 Hex.

GCMSR BIT 0:
Graphics Mode.
0 = Alphanumeric mode.
1 = Graphics mode addressing, which disables the character address latches, and sends identical addressing to both AA0-7 and BA0-7 busses.

GCMSR BIT 1:
Chain Odd/Even.
0 = Normal.
1 = Direct the processor address bit-0 to be replaced by a higher order bit. Odd/Even planes will be selected by the value of the processor A0 bit.

GCMSR BIT 2:
Memory Map "0". Controls CDSEL0 output.

GCMSR BIT 3:
Memory Map "1". Controls CDSEL1 output.

GCMSR BIT 4-7: Not used.

GRAPHICS CONT. COLOR DON'T CARE REG. (GCCDR)

This is a write only register and is accessible when the value in the Graphics 1 & 2 Index Register is 07 Hex.

GCCDR BIT 0-3:
Plane 0-3 don't care.
0 = Normal.
1 = A color compare read operation will yield a "1" regardless of the actual comparison result.

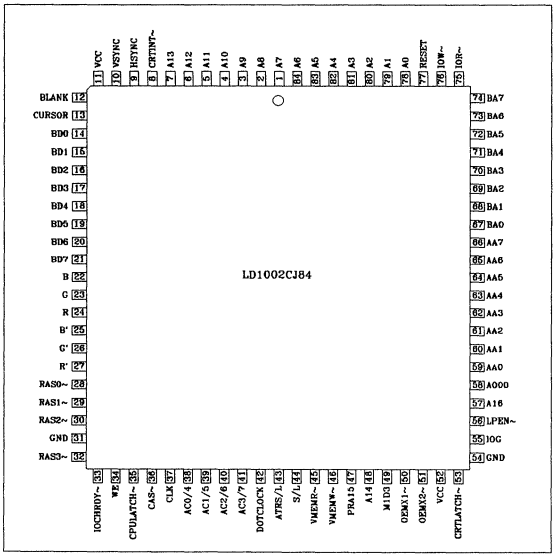
GCCDR BIT 4-7: Not used.

GRAPHICS CONT. BIT MASK REGISTER (GCBMR)

This is a write only register and is accessible when the value in the Graphics 1 & 2 Index Register is 08 Hex.

GCBMR BIT 0-7:
0 = Corresponding bit in each bit plane to be immune to change provided that the location being written was the last location read by the processor.
1 = Unimpeded modification to the appropriate bits in all planes.

LD1002 PINOUT



MEMORY

4

MASS STORAGE

5

SINGLE CHIP WINCHESTER DISK CONTROLLER

DESCRIPTION

The LD1111 is a monolithic hard disk controller IC, designed specifically for IBM AT personal computer systems and compatibles, to work with ST506/412 and ESDI standards. The LD1111 is designed to interface directly with the Western Digital WD37C65A floppy disk controller for a combined fixed/floppy disk controller. This option allows for a minimal parts count combination (the floppy function may be off-board as well). For ST506 drives, the LD1111 is designed to interface directly with the Advanced Micro Devices AMD9582 data separator.
The LD1111 architecture has been optimized for implementation in a minimal parts count disk controller board. The DC Electrical characteristics are such that the component can directly drive a motherboard slot without external drivers or receivers. Signal outputs, which drive external disk signals, must be driven with external drivers. Differential disk inputs are received externally and converted to single ended inputs before being received by the LD1111.

FEATURES

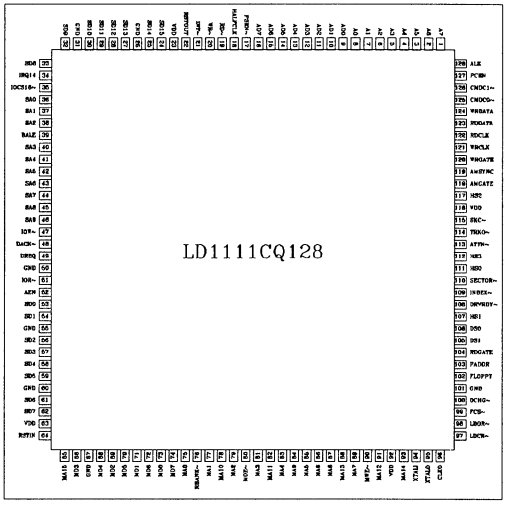
* Program selectable ST506/412 or ESDI format.
* Up to 3 Mword/sec transfer rate.
* Interface directly with the Western Digital WD37C65A floppy disk controller.
* Interface directly with the Advanced Micro Devices AMD9582 data separator.
* Can be used virtually with any 8 bit microcomputer (microcontroller) with a multiplexed address and data bus.
* Low power
* Low components count and cost.
* AT bus compatible.

APPLICATIONS

* External hard disk controller card.
* Internal hard disk controller.

ORDERING INFORMATION

Part number	Package	Operating temperature
LD1111CQ128	QuadPack	0 ° C to +70 ° C



GENERAL DESCRIPTION

The LD1111 is partitioned into three functionally separate sub-sections. The sequencer performs the bit level disk data manipulation. The buffer manager controls the byte level disk data and performs byte/word packing/unpacking. The host interface logic emulates the standard IBM AT disk controller. The three LD1111 blocks are controlled and coordinated by the microcontroller. The microcontroller performs high level computation and command parsing. Error correction, disk seeks, and overall non-realtime, housekeeping is performed by the microcontroller.
The disk sequencer is capable of manipulating disk data at rates up to 15 MBits/Sec. It contains two selectable binary polynomials for ECC with CRC-CCITT implemented automatically on the fly as configured by the microcontroller. The drive interface is program selectable for compatibility with either the ST506/412 or the ESDI standards. Throughout this text, ST506/412 drives are simply referred to as ST506 drives. The buffer control logic has internally selectable request sources primarily under the control of the disk sequencer. This logic includes control lines to access an external Static RAM (SRAM) buffer. Various configurations are possible depending on the board cost/performance trade-offs. The LD1111 includes complete control over 8 bidirectional data pins with two

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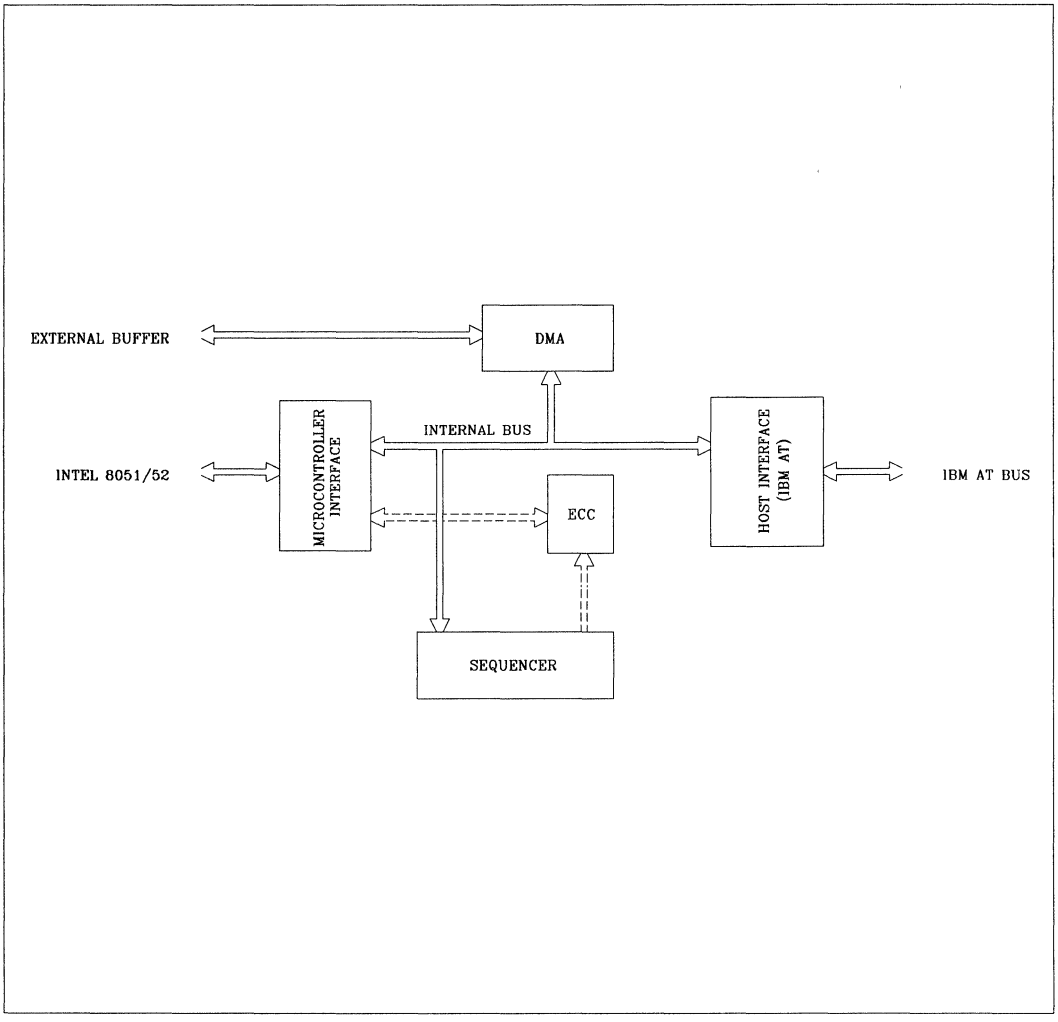
BLOCK DIAGRAM



control pins to transfer data to and from the external SRAM.
The third partition consists of the AT Host interface signals. This includes a 16 bit bi-directional data bus capable of up to 3 MWords/sec transfers. The programmed I/O addresses are decoded, inside the LD1111, with the ability to select between a primary or secondary address. The LD1111 interface is fully emulating, and accommodates all required control and timing signals from the AT Host bus. Virtually any 8 bit microcomputer (microcontroller) with a multiplexed address and data bus may be used. Ideally, the microcontroller should be I/O intensive, for non-real-time drive tasks. The Intel 8031 requires an external EPROM or ROM for program memory (address latch is required for demultiplexing the microcontroller address/data bus - contained within the LD1111). Additionally, a pull-down sip is required for the 8051 data bus and one set of drivers and receivers for the disk interface. RSTOUTmust last for at least 24 HALKCLK cycles in order to meet 8051 timing requirements. A crystal is required for the oscillator circuit. Optionally a MOS level clock can be used to drive the crystal input. Three discrete passive elements are required for the oscillator when being driven by a crystal. An external static RAM buffer is necessary in the disk controller design. The RAM must have an 8 bit bi-directional data bus. The buffer may be up to 64K bytes.

PIN DESCRIPTIONS

Symbol	Pin	Signal type	Pin description
AD7-0	16-9	I/O	8 Bit multiplexed microcontroller address and data bus.
A7-0	1-8	O	8 bit, de-multiplexed, latched microcontroller address bus.
INT~	21	O	This active low output is used to inform the system microcontroller of an interrupt condition.
PSEN~	17	I	This input indicates whether the current microcontroller cycle is an external program fetch or data operation. When high, the LD1111 will respond to a properly addressed microcontroller command as this indicates the processor is communicating with I/O peripherals and not program memory. (IO/M~).
ALE	128	I	Microcontroller address valid is specified with respect to the falling edge of this input signal.
RD~	19	I	When low, this input, gated with a valid microcontroller address and PSEN~ high, enables data from the LD1111 onto the microcontroller data bus (IOR~).
WR~	20	I	The rising edge of this input, gated with a validmicrocontroller address and PSEN~ high, loads data from the microcontroller data bus into a selected register of the LD1111 (IOW~).
MD7-0		I/O	These 8 bi-directional lines are used to transfer data between the LD1111 and an external buffer memory.
MA15-0		O	These comprise the 16 memory address lines used to access the external buffer RAM in 8 bit quantities.

PIN DESCRIPTIONS

Symbol	Pin	Signal type	Pin description
RBANK~	76	O	This output is MA15~. This signal can be used to enable a second 32K x 8 RAM.
MWE~	90	O	This line is driven active low when writing to the buffer.
MOE~	80	O	This line is driven active low when reading the buffer.
RDGATE	104	O	This output, when high, directs the PLO to start reading and should switch the VCO from crystal to PLO mode. ESDI mode requires an external open collector driver.
WRGATE	120	O	This output, going high, should enable writing on the drive. The VCO should provide a crystal clock during this time for write data reference. This signal requires an external open collector driver.
RDCLK	122	I	This input is used for disk data sequencing. If a read data clock is not available due to a data write or no drive command, then a reference clock must be switched in. During a read data command, this clock provides the read data reference timing. This input requires an external differential receiver.
WRCLK	121	O	This clock output provides a reference to the VCO for capturing the serial disk data while being written in ST506 mode. This is also the timing reference for the NRZ data being written in ESDI mode. This signal requires an external differential driver.
RDDATA	123	I	This input receives serial NRZ data during a disk read. ESDI mode requires an external differential receiver.
WRDATA	124	O	This output drives serial NRZ data to be written to the drive. The NRZ data is specified with respect to the WRTCLK output. ESDI mode requires an external differiential driver.
AMSYNC	119	I/O	This signal is dual purpose depending on the drive mode selected. It is an input in ST506 interface mode and an output in ESDI mode. In ST506 mode this input should be driven high a fixed number of read data bits before the complete address mark is read serially into the LD1111 (8 bits AMD9582). This signal establishes byte synchronization with the read data. In ESDI mode this signal, AMEN0 is an output to the first drive on the radial cable (requires an external open collector driver). This signal's operation is dependent on whether a read or write operation is being performed.
AMGATE	118	O	This signal is dual purpose depending on the drive mode selected. This signal is always an output regardless of the mode selected. As an output, AMGATE goes high in ST506 mode to signal the VCO that the address mark is being written. ESDI mode, this signal is an output to the second drive on the radial cable if present (requires an external open collector driver). The operation of AMEN varies with the command in progress (write: to generate an address mark,

PIN DESCRIPTIONS

Symbol	Pin	Signal type	Pin description
			read: enable VCO to search for an address mark).
INDEX~	109	I	This input connects to the index signal from the drive. It should pulse low once for each revolution of the drive. This signal input can be taken directly from the command cable and need not be buffered.
SECTOR~	110	I	This multipurpose input can connect directly to the command cable. In ST506 mode this input is only used for a hard sectored drive. If the drive format does not provide a sector pulse, this input should be connected to VDD. In ESDI mode this signal is used for both hard and soft sectored drives. For a hard sectored drive this is the sector pulse input. In the case of a soft sectored drive, this is the address mark found indication f rom the drive. The trailing edge indicates the beginning of the PLO field.
DRVRDY	108	I	This active low input can be taken directly from the command cable in either mode of operation. In both interface modes this signal indicates the selected drive is "ready."
ATTN~	113	I	This active low input can be taken directly from the command cable for both interface options. In the ST506 mode, WRTFLT~ indicates an error condition has occurred within the controller or drive during a write operation. This signal is ATTN~ when the ESDI interface is used.
SKC~	115	I	This active low input should be taken directly from the command cable for both interfaces. In the ST506 mode, this input, when low, indicates a seek operation has completed or there is no seek operation in progress. In ESDI mode, this input is used by the drive to present serial status and configuration data.
TRK0~	114	I	This active low input is used in both modes and should be directly connected to the command cable. In the ST506 mode, this input, when low, indicates the selected drive is positioned over cylinder zero. In the ESDI mode, this input is used to handshake command and status-configuration data.
CMDCO~	125	I	This active low input signal, from the first drive, is only used during the ESDI mode and can be directly connected to the radial connector. This signal is asserted low by the first drive to indicate completion of a command. For ST506, this input can be used for a general purpose status input (i.e. cartridge change).
CMDC1~	126	I	This active low input signal, from the second drive, is only used during the ESDI mode and can be directly connected to the radial connector. This signal is asserted low by the second drive to indicate completion of a command. For ST506, this input can be used for a general purpose status input (i.e. cartridge change).
HS3-0		O	These 4 outputs are the encoded address of the drive head selec-

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PIN DESCRIPTIONS

Symbol	Pin	Signal type	Pin description
			tion. The asserted state is considered to be active high (require external open collector drivers). These outputs are interpreted the same for both ST506 and ESDI operations.
DS1-0	105-106	O	These two outputs are used to select one of two fixed disks when asserted active high (require external open collector drivers). In ST506 mode one or the other will always be asserted. In ESDI mode the third drive select line is not used as the Host is only capable of selecting one of two fixed drives. If both signals are negated, no drive is selected. Otherwise these signals will have the binary encoded drive address to select one of the two drives.
PCEN	127	O	Precomp enable output line. THis signal is internally qualified with WRGATE.
PADDR	103	I	This input, when high causes the LD1111 to respond to the primary I/O address range (1F0H-1F7H, 3F6H, 3F7H). If low, the LD1111 responds to I/O address range (170H-177H, 376H, 377H). This pin is internally pulled up.
FLOPPY	102	I	This input, when high indicates the LD1111 is part of a single board floppy/fixed disk configuration. When low, the LD1111 is in a fixed disk only configuration. This pin is internally pulled up.
SD15-8		I/O	These 8 bi-directional signals form the most significant byte of the AT host data bus.
SD7-0		I/O	These 8 bi-directional signals comprise the least significant byte of the AT host data bus.
SA9-0		I	These 10 address inputs from the host bus are for programmed I/O port selection.
AEN	52	I	This input is used to differentiate a programmed I/O instruction from a DMA cycle on the host bus. When low, a programmed I/O instruction is indicated and when high a DMA cycle is indicated.
BALE	39	I	The rising edge of this input signal is used to indicate the beginning of a host transfer cycle.
IOR~	51	I	The active low state of this signal, together with a valid programmed I/O address, gates an 8 bit port value or 16 bit data value onto the host bus.
IOW~	47	I	The active low state of this signal, together with a valid programmed I/O address, enables data into the LD1111 and latches the values on the rising edge of this signal.
IRQ14	34	O	This active high output is used to cause a host interrupt request.

PIN DESCRIPTIONS

Symbol	Pin	Signal type	Pin description
IOCS16~	35	O	When asserted low by the LD1111, a 16 bit data transfer with 1 wait state is indicated for the current cycle.
DACK~	48	I	Optional DMA acknowledge input. This pin is internally pulled up.
DREQ	49	O	Optional DMA request output.
FCS~	99	O	This output, when low, indicates the co-resident floppy controller is selected (floppy chip select).
LDCR~	97	O	This output, when low, indicates the co-resident floppy control register is selected.
LDOR~	98	O	This output, when low, indicates the co-resident floppy operations register is selected.
DCHG~	100	I	This input, when low, reports the co-resident floppy drive disk change status is active.
RSTIN	64	I	The active high state of this signal from the host resets the LD1111 circuitry to the initialized state and releases all interface signals.
RSTOUT	22	O	This active high signal is driven by the LD1111 to reset the controller components whenever a host bus reset has been asserted or a host programmed I/O software reset is issued to the LD1111.
XTALO	95	O	One pin of a crystal should be connected to this input. Alternatively, if a crystal is not used and the XTALI pin is driven by a MOS level oscillator output then the XTALO input should be left open.
XTALI	94	I	If a crystal is used to generate the clock signal, the other pin of the crystal should be connected to this pin. If an external clock source is used to drive the LD1111, the oscillator source should be connected to this pin.
HALFCLK	18	O	This signal is one half the frequency of the crystal oscillator. It is a MOS level output of approximately 50% duty cycle.
CLK0	96	O	This signal is the same as the XTAL frequency. It is a MOS level output of approximately 50% duty cycle.
VDD		I	There are 4 VDD pins which are connected to the system positive supply voltage (5 Vdc). All VDD pins must be connected.
VSS		O	There are 7 VSS pins which are connected to the system ground return path. All ground pins must be connected.

HOST COMPUTER INTERFACE

The host computer (IBM AT) communicates with the LD1111 via a series of I/O ports. The command is sent to the controller, and status is returned to the host via these ports. Data is transferred via programmed I/O using the string I/O instruction (OUTSW, INSW). The host may use a controller supplied interrupt or poll the status register in order to perform the handshake protocol. The first section explains the host interface registers. This section is followed by the protocol algorithms the host may use in writing a device driver. A section explains how to reset the controller (and the consequences of a reset). Finally, functions shared with the floppy controller are detailed.

HOST REGISTER DEFINITIONS

The registers accessible by the host computer are 8 bits in nature, except for the 16 bit data register. These registers are used to communicate between the host and the controller. Appendix A contains a table with the actual physical addresses of the I/O ports.

DATA REGISTER

This 16 bit, read/write, register is used to transfer data using a programmed I/O protocol. The host basically waits for proper controller status, bursts a sector (usually 256 words), then checks status again. The data is read or written using 16 bit string I/O instructions (OUTSW, INSW). The controller is responsible for performing byte/word packing/unpacking at host speeds. There is an exception. When read/write long commands are issued, the sector data is burst 16 bits at a time (same as a normal read/write). But, the ECC data is transferred a byte at a time (using only the LSB of the data register) and follows a special handshake protocol.

WRITE PRECOMPENSATION REGISTER

This 8 bit, write only, register (all latches) must be written prior to writing the command register on any command which will write to the disk (write, write long, format track). The value written to this register is the cylinder address divided by 4, where reduced write current should be enabled. The controller will enable reduced write current if the cylinder specified (or a higher cylinder) is accessed and the drive has 8 or fewer heads (as specified by the control register). After a reset, this register is initialized to 20H (precomp cylinder = 128) automatically by the controller. The contents of this register remain the same until written by the host or a reset is generated.

ERROR REGISTER

This 8 bit, read only, register (all latches) is used to report the results (success/fail) of the last controller operation. The value in the register remains latched until the command register is written or the controller is reset. The error values in this port vary depending on whether a self test is initiated (diagnostic mode) or a command terminates (operational mode). The error values are as follows:

Diagnostic Mode:

01H - No Errors
02H - Controller Error
03H - Sector Buffer Error
04H - ECC Logic Error
05H - Sequencer Error

Operational Mode:

When the following bits are set:

Bit 0 - Data Address Mark Not Found
Bit 1 - Track 0 Not Found After 2047 Steps Toward Track 0
Bit 2 - Command Aborted (see Status Register)
Bit 3 - Not Used
Bit 4 - Sector ID Not Found
Bit 5 - Not Used
Bit 6 - Data ECC Error (Uncorrectable)
Bit 7 - Bad Block Detected

This register is set, by the controller, to 01H immediately following a reset. The controller then enters diagnostic mode and may change the contents of the error register (if an error is detected).

SECTOR COUNT REGISTER

This read/write, 8 bit, register is used to set the number of sectors to transfer. Before the command register is written, this register must be set to the number of sectors to transfer (0=256). After each sector is successfully transferred, this register is decremented (until it reaches 0). When the command is complete, this register contains the number of sectors not yet transferred. For a format command, this register is set to the number of sectors per track. After a reset, this register is initialized to 01H by the LD1111.

SECTOR ADDRESS REGISTER

This read/write, 8 bit, register is used to set the starting sector number to begin a transfer. Before the command register is written, this register must be set to the starting sector number to transfer (1 to sectors per track). A value of 0 will cause an error (sector ID not found). This register is updated after each sector is successfully transferred. At the end of a command, it will contain the address of the sector last accessed. After a reset, this register is initialized to 01H by the LD1111.

CYLINDER REGISTER (LSB)

This read/write, 8 bit, register (all latches) is used to set the starting cylinder number (LSB) to begin a transfer. Before the command register is written, this register must be set to the starting cylinder number to transfer (cylinder address is zero justified). This register is updated after each sector is successfully transferred. At the end of a command, it will contain the address of the cylinder last accessed. After a reset, this register is initialized to 00H by the LD1111.

CYLINDER REGISTER (MSB)

This read/write, 3 bit, register (all latches) is used to set the starting cylinder number (MSB) to begin a transfer. Before the command register is written, this register must be set to the starting cylinder number to transfer (cylinder address is zero justified). This register is updated after each sector is successfully transferred. At the end of a command, it will contain the address of the cylinder last accessed. Only the lower 3 bits of this register can be loaded. The upper 5 bits are always read back as zero. After a reset, this register is initialized to 00H by the LD1111.

DRIVE/HEAD REGISTER

This read/write, 8 bit, register is used for several purposes. It must be written prior to writing the command register. After a reset, this register is cleared.

COMMAND REGISTER

This write only, 8 bit, register (all latches) is used to specify the command to be executed and start the command execution. All other registers (sector count, sector address, etc.) must have been previously written. Any of 256 commands could be defined by this register. Section 2.2 details the commands defined for this controller. Writing the command register clears several of the status bits. Any pending host interrupt requests are cleared. BSY is automatically set, in the status register, when the command register is written.

STATUS REGISTER

This read only, 8 bit, register provides the results of the last operation. If bit 7, the Busy bit, is set to a 1, then no other bits are valid in the status port, (with the exception of DRQ), nor should any other ports be polled. Reading the status register, clears any pending host interrupt requests. .

CONTROL REGISTER

This write only, 8 bit, register is used for several system control functions.

AUXILIARY STATUS REGISTER

This read only, 8 bit, register is defined identically to the status register in 2.1.10. Unlike the status register, reading this register does not clear any pending interrupts.

DIGITAL INPUT REGISTER

This read only, 8 bit, register provides status useful in controller self test procedures.

COMMAND PROTOCOL

The host interaction with the LD1111 is detailed in the following sections. The host sends parameters to,the controller and expects certain responses within given time limits. The IBM AT BIOS driver is explained. The BIOS interrupt handler simply sets a flag in RAM and sends the interrupt controller an EOI (it does not access the disk controller).

RESTORE

The function of this command is to position the carriage over track 0. The step rate is passed as part of the command. The step rate is saved until the host changes it. The IBM AT BIOS driver performs the following algorithm:

1. Write the control register
2. Wait for busy=0 in the status port with timeout.
3. Select the drive (write to Drive/Head register).
4. Wait for ready=1 and seek complete=1 in the status port with timeout.
5. Unmask interrupt level

6. Write command register with restore command
7. Wait for an interrupt with timeout
8. Check status register for any errors. If the error bit is set, in the status register, check the error register.
9. Done

SEEK

The function of this command is to position the carriage over the selected cylinder and head. The step rate is passed as part of the command. The step rate is saved until the host changes it. The IBM AT BIOS driver performs the following algorithm:

1. Write the control register
2. Wait for busy=0 in the status port with timeout.
3. Select the drive (write to Drive/Head register).
4. Wait for ready=1 and seek complete=1 in the status port with timeout.
5. Unmask interrupt level
6. Write the LSB cylinder register
   Write the MSB cylinder register
7. Write command register with seek command
8. Wait for an interrupt with timeout
9. Check status register for any errors. If the error bit is set, in the status register, check the error register.
10. Done

READ

The function of this command is to read disk data. The IBM AT BIOS driver performs the following algorithm:

1. Write the control register
2. Wait for busy=0 in the status port with timeout.
3. Select the drive (write to Drive/Head register).
4. Wait for ready=1 and seek complete=1 in the status port with timeout.
5. Unmask interrupt level
6. Write the sector count register
   Write the sector register
   Write the LSB cylinder register
   Write the MSB cylinder register
7. Write command register with read command
8. Wait for an interrupt with timeout
9. Using string I/O, input 256 words
10. Check status register for any errors. If the error bit is set, in the status register, check the error register.
11. If more sectors to read then goto 8
12. Done

WRITE

The function of this command is to write disk data. The IBM AT BIOS driver performs the following algorithm:

1. Write the control register
2. Wait for busy=0 in the status port with timeout.
3. Select the drive (write to Drive/Head register).
4. Wait for ready=1 and seek complete=1 in the status port with timeout.
5. Unmask interrupt level
6. Write the sector count register
   Write the sector register
   Write the LSB cylinder register
   Write the MSB cylinder register
7. Write command register with write command
8. Wait status register, DRQ=1 with timeout
9. Using string I/O, output 256 words
10. Wait for interrupt with timeout
11. Check status register for any errors. If the error bit is set, in the status register, check the error register.
12. If status register, DRQ=1 then goto 9
13. Done

FORMAT TRACK

The function of this command is to format a track. The IBM AT BIOS driver performs the following algorithm:

1. Write the control register
2. Wait for busy=0 in the status port with timeout.
3. Select the drive (write to Drive/Head register).
4. Wait for ready=1 and seek complete=1 in the status port with timeout.
5. Unmask interrupt level
6. Write the sector count register (sectors per track)
   Write the LSB cylinder register
   Write the MSB cylinder register
7. Write command register with format command
8. Wait status register, DRQ=1 with timeout
9. Using string I/O, output 256 words
10. Wait for interrupt with timeout
11. Check status register for any errors. If the error bit is set, in the status register, check the error register.
12. If status register, DRQ=1 then goto 9
13. Done

READ VERIFY

The function of this command is to read disk data without transferring it to the host. The IBM AT BIOS driver performs the following algorithm:

1. Write the control register
2. Wait for busy=0 in the status port with timeout.
3. Select the drive (write to Drive/Head register).
4. Wait for ready=1 and seek complete=1 in the status

port with timeout.
5. Unmask interrupt level
6. Write the sector count register
   Write the sector register
   Write the LSB cylinder register
   Write the MSB cylinder register
7. Write command register with read verify command
8. Wait for an interrupt with timeout
9. Check status register for any errors. If the error bit is set, in the status register, check the error register.
10. Done

READ LONG

The function of this command is to read disk data and ECC data. The IBM AT BIOS driver performs the following algorithm:

1. Write the control register
2. Wait for busy=0 in the status port with timeout.
3. Select the drive (write to Drive/Head register).
4. Wait for ready=1 and seek complete=1 in the status port with timeout.
5. Unmask interrupt level
6. Write the sector count register
   Write the sector register
   Write the LSB cylinder register
   Write the MSB cylinder register
7. Write command register with read long command
8. Wait for an interrupt with timeout
9. Using string I/O, input 256 words
10. Wait for DRQ=1 in status register with timeout
11. Read ECC bytes from data register.
12. Check status register for any errors. If the error bit is set, in the status register, check the error register.
13. If more sectors to read then goto 8
14. Done

WRITE LONG

The function of this command is to write disk data and ECC data. The IBM AT BIOS driver performs the following algorithm:

1. Write the control register
2. Wait for busy=0 in the status port with timeout.
3. Select the drive (write to Drive/Head register).
4. Wait for ready=1 and seek complete=1 in the status port with timeout.
5. Unmask interrupt level
6. Write the sector count register
   Write the sector register
   Write the LSB cylinder register
   Write the MSB cylinder register
7. Write command register with write long command
8. Wait status register, DRQ=1 with timeout
9. Using string I/O, output 256 words
10. Wait for status port bit DRQ=1 with timeout
11. Output ECC bytes
12. Wait for interrupt with timeout
13. Check status register for any errors. If the error bit is set, in the status register, check the error register.
14. If status register, DRQ=1 then goto 9
15. Done

SET PARAMETERS

The function of this command is to set the controller parameters for the selected drive. The controller saves these parameters until reset or changed by the host. The IBM AT BIOS driver performs the following algorithm:

1. Write the control register
2. Wait for busy=0 in the status port with timeout.
3. Select the drive (write to Drive/Head register).
4. Wait for ready=1 and seek complete=1 in the status port with timeout.
5. Unmask interrupt level
6. Write sector count (sectors per track)
   Write Drive/Head (max head address)
7. Write command register with set parameters com mand
8. Wait for an interrupt with timeout
9. Check status register for any errors. If the error bit is set, in the status register, check the error register.
10. Done

DIAGNOSE

The function of this command is to perform contoller self test. The IBM AT BIOS driver performs the following algorithm:

1. Wait for busy=0 in the status port with timeout.
2. Write command register with diagnose command
3. Wait for busy=0 in the status port with timeout.
4. Check status register for any errors. If the error bit is set, in the status register, check the error register.
5. Done

RESET

The controller is reset when the host bus reset signal is asserted (power up) or at any time the RST bit in the control register is asserted (pulsed high for at least 24 HALFCLK periods in order to meet 8051 timing requirements). The controller responds to the release of

reset by entering a busy state. While busy, the controller performs self test and places the results in the error register. Once the controller is ready to accept a command byte, BSY is cleared.

REGISTERS SHARED WITH THE FLOPPY

One bit of one read only register is shared by the floppy disk controller. Bit 7 of the digital input register is supplied by the floppy controller and the remaining 7 bits are supplied by the LD1111. The signals involved are FLOPPY and DCHG~ . When a floppy is co-resident, DCHG~ is provided as an input to the LD1111 (the LD1111 will then drive all 8 data bits during an input of the digital input register by the host). If the floppy controller is not co-resident, bit 7 is not driven (tri-state) when the digital input register is read by the host.

INTERRUPTS

Interrupts are generated as specified by the command protocol. The interrupt is latched and remains pending until cleared. The interrupt level is cleared on any command from the host, programmed reset, hardware reset, or status read. Reading the auxiliary status register does not clear any pending interrupts.

MICROCONTROLLER PORT DEFINITIONS

The Intel 8051 family has four, 8 bit I/O ports. Two ports are dedicated for address and data (P0, P2). The other ports are used for disk control functions. High volume controller production could easily be switched to a ROM based Intel 8051/8052 microcontroller without and firmware changes.

PORT 1

This port is used for disk control outputs and configuration inputs. A reset sets all latches.

ESDI

This port is used for disk control outputs and configuration inputs. A reset sets all latches (input pins not effected).

PORT 3

This port is used for program inputs and dedicated microcontroller use. A reset sets the port to input mode.

DRIVE CONTROL INPUTS

This read only register provides current drive status to the microcontroller. The contents apply to the currently selected drive.

DRIVE CONTROL OUTPUTS

This register is used to control the drive function and configure the LD1111 for specific device attributes. This register is write only.

HEAD SELECT

This four bit, write only register is used to select the actual head on the target device. The host head address is copied to this register by the microcontroller. This register is clear by a reset.

MICROCONTROLLER COMMUNICATION WITH THE HOST

The host computer communicates with the disk controller via a series of I/O ports. The data transfer is handled by the buffer controller. The function of the microcontroller is to interpret the host command and setup the sequencer and buffer controller to carry out the realtime data transfer operations.

The microcontroller must read the host command and parameters. As a command progresses and completes, the microcontroller must update the non-realtime host registers (the buffer controller updates the sector count and sector address in realtime).

The microcontroller must be able to read the following host registers:

Precompensation Cylinder register
Sector Count register
Sector register
Cylinder registers (LSB,MSB)
Drive/Head register
Command register

The microcontroller must be able to write the following registers:

Error register
Sector Count register
Sector register
Cylinder registers (LSB,MSB)

Status register (Alternate Status register)

The microcontroller is allowed to read the host interface registers at any time. However, the contents are only valid after the command register is written and before the status register is updated. The microcontroller is only allowed to write the host interface registers while a command is in progress (after host writes the command register or pulses reset, until the microcontroller updates the status register).

SPECIAL FUNCTIONS

Some special functions have been included to allow for self test and to assist in firmware efficiency. These functions are detailed in the following subsections.

RESET HOST INTERFACE

When the host issues a diagnose command, the host interface must be reset the same way as if a host reset had been issued. A write to this port address (data = X) resets the host registers as follows:

Precompensation Cylinder register	20H
Error register	01H
Sector Count register	01H
Cylinder registers (LSB,MSB)	00H
Drive/Head register	00H
Drive Status	error latches cleared, BUSY = 1

GENERATE HOST INTERRUPT

This write only register is a strobe which sets the host interrupt latch. This latch is cleared by a reset or when the host writes the command register (also when host reads primary status register).

PRECOMPENSATION CYLINDER REGISTER

This 8 bit, read only register contains the cylinder address/4 at which to assert write precompensation and low current. The value is interpreted entirely by the microcontroller. A reset sets the register to 20H.

SECTOR COUNT REGISTER

This 8 bit, read/write register contains the number of sectors left to transfer. The microcontroller reads and saves this register before a read/write command. The buffer controller automatically decrements this register after each sector is sucessfully transferred to/from the buffer. A reset sets the register to 01H. In the case of a disk read, BUSY status is automatically cleared when the last sector is transferred to the host. In the case of a correctable ECC error, the buffer controller empties the buffer and decrements the sector count (under microcontroller control).

SECTOR REGISTER

This 8 bit, read/write register contains the sector address. The microcontroller reads and saves this register before a read/write command. The buffer controller automatically increments this register after each sector is sucessfully transferred to/from the buffer. It is not incremented after the sequencer last sector is transferred. A reset sets the register to 01H. In the case of a correctable ECC error, the microcontroller must correct the data and command the buffer controller to empty the buffer. After the last sector of a transfer (sector count = 0), the buffer controller will not increment the sector register. Otherwise, the buffer controller automatically increments the sector address after the buffer is emptied. The transfer can then proceed by programming the sequencer to start at the next sector beyond the error.

CYLINDER REGISTERS (MSB/LSB)

This 11 bit, read/write register (3 bit 8 bit) contains the cylinder address. If a multiple sector transfer causes a step to take place, the microcontroller must read the cylinder, increment it, then write it back. A reset clears the registers. Only the lower 3 bits of the MSB cylinder are defined (the upper 5 bits are reserved and should always be written as 0, see chapter 9). The microcontroller must mask off the upper 5 bits when reading the MSB cylinder register.

DRIVE/HEAD REGISTER

This 8 bit, read/write register contains several control bits and the head address. If a multiple sector transfer causes a head switch to take place, the microcontroller must update the head field of this register. A reset causes the register to be cleared.

COMMAND REGISTER

This 8 bit, read only register contains the host command. When the host writes the command register, the following hardware actions occur:

1. Error register <-- 00H (microcontroller does this)
2. Any pending host interrupt is cleared

3. Status register <-- BUSY=1, WRF=0, DRQ=0, CORR=0, ERROR=0
4. LD1111 interrupt latch (to microcontroller) is set. The LD1111 interrupt latch is cleared when the microcon troller reads the command register.

ERROR REGISTER

This 8 bit, write only register is use by the microcontroller to report an error code to the host. This register is set to 01H by a reset.

STATUS/ALTERNATE STATUS REGISTERS

This 8 bit, write only register is used to store the host completion status.

BUFFER CONTROLLER

The buffer controller transfers data between the host and the disk sequencer. There is an eight bit data path between the sequencer and the buffer controller. A 16 bit data path exists between the buffer controller and the host (read/write long ECC data is transferred 8 bits at a time in the LSB of the word). In a special error recovery mode, the microcontroller can access individual memory locations and fill/empty the buffer. The buffer controller interacts with the disk sequencer such that data late conditions can never occur. The disk sequencer will not assert write gate unless at least 1 full sector is available in the buffer. Likewise, the sequencer will not attempt to transfer data into the buffer (disk read) unless at least 1 full sector is available in the buffer. These registers are accessed by the microcontroller.

The buffer controller automatically decrements the host sector count and increments the host sector address (sector, head, cylinder) as needed. When an error occurs, the microcontroller manually resets these registers to the proper values. There are two basic modes of operation (FIFO, direct access). During the data portion of a read or write command, the buffer controller performs a FIFO action. Read/write long operations involve a modified FIFO action. In order to perform ECC data corrections and test the buffer memory, a direct access mode is also provided. The buffer controller should be setup and started before the sequencer. The buffer controller has the following programmable resources:

Buffer Control register
FIFO or direct access
Direction of transfer
Empty (1 block)
Read-verify
Long
All (empty full buffer)

Buffer Status register
FIFO empty
FIFO full
Done

Buffer Address registers (LSB, MSB)
used only for direct access

Buffer Data register
used only for direct access

Buffer Size register
used only for FIFO

Sector Size register
used only for FIFO

Sector Count register
used only for FIFO

Sector register
Start DMA strobe
used only for FIFO

Max Sector register
used only for FIFO

Max Head register
used only for FIFO

Load DMA byte counters strobe
used only for FIFO

Reset differential counter and DMA address counter strobe
used only for FIFO

The procedure for starting the DMA is as follows:

1. Load command register. The address registers are uneffected. This also the buffer controller.
2. Load address registers (non FIFO only).
   Reset differential counter and address strobe (FIFO only).
   Load buffer size register (FIFO only).
   Load sector size register (FIFO only).
   Load byte counters strobe (FIFO only).
3. Load start DMA strobe.

BUFFER CONTROL REGISTER

This register is write only.

BUFFER STATUS REGISTER

This register is read only.

BUFFER ADDRESS REGISTERS (LSB, MSB)

These write only registers are used in direct access mode to select an absolute address for access by the microcontroller. It is not intended for the microcontroller to access the buffer while the sequencer is busy transferring data. This function is provided to allow the microcontroller to test the buffer memory and to correct ECC errors. This register is cleared to zero by a FIFO reset or any reset. The address automatically increments each time the microcontroller accesses the buffer data register. When an ECC error is detected, the microcontroller should reset the FIFO so the sector in question will be stored in the buffer at absolute address 0.

BUFFER DATA REGISTER

This 8 bit, read/write register is used in direct access mode. It is not intended for the microcontroller to access the buffer while the sequencer is busy transferring data. This function is provided to allow the microcontroller to test the buffer memory and to correct ECC errors. The contents of the buffer RAM are not effected by a reset. The address automatically increments each time the microcontroller accesses the buffer register. In order to read a memory location, the address is loaded and a dummy read is required (discard data). The second read gives the correct data. Each subsequent read will yield correct data as well (dummy read not required).

A microcontroller write will store the data at the addressed location (dummy write not required).

BUFFER SIZE REGISTER

This 8 bit, write only register is loaded with the number of blocks that will fit, completely, into the buffer FIFO at one time. For example, if the block size is 512 bytes and the buffer size is 2048 bytes, this register is loaded with 4. If a long command is issued, this register is loaded with 3 (for this example). The contents of this register are not effected by a reset. This register only needs to be loaded once, after a power on reset. Loading this register with a 00H is illegal (buffer size = 0). The maximum buffer size is as follows:

Sector Size	Max Number of Buffers
128	255
256	255
512	128
1024	64

SECTOR SIZE REGISTER

Write only register is loaded with the number of bytes that the FIFO controller should consider to be a block (sector). The contents of this register are not affected by a reset. This register needs to be reloaded when the sector size is changed (strobe load DMA byte counter). This register must be loaded before the DMA start strobe. The disk sequencer also uses this register (before sequencer start strobe).

SECTOR COUNT REGISTER

This register is automatically decremented by the buffer controller during FIFO mode as each block is transferred between the host and the buffer. This register is shared with the host interface. This register is set to 01H by a reset. This register is also automatically decremented, in direct access mode, after a buffer empty command is completed.

SECTOR REGISTER

This register is automatically incremented by the Buffer Controller during FIFO mode as each block is transferred between the buffer and the host. This register is shared with the host interface. This register is set to 01H by a reset. This register is also automatically incremented, in direct access mode, after a buffer empty command is completed (and the sector count is not 0). During a head switch or step, the microcontroller must reset this register to 01H.
Since the buffer controller decrements the sector count at a different time from the sequencer incrementing the sector address, the disk address may not match the point at which the buffer is operating. If the buffer controller is programmed for 1 block per buffer, the disk address will agree with the count at all times. In other cases, if the host cannot keep up with the disk transfer rate, the two will not coincide until the entire command completes.

MAX SECTOR REGISTER

This eight bit, write only register is used to contain the maximum sector address. During a data transfer, the buffer controller will increment the sector register and wrap it around to 1 as need be.

MAX HEAD REGISTER

This four bit, write only register is used to contain the maximum head address. During a data transfer, the buffer controller will increment the head address and wrap it around to 0 as need be.

READ AHEAD CONSIDERATIONS

In order to perform read-ahead functions, the buffer controller has a special strobe to reset the differential counters and host buffer address. Otherwise the last differential count and address remain unchanged.

DISK SEQUENCER

The disk sequencer transfers data between the disk and the buffer controller. The microcontroller programs the sequencer with the appropriate parameters and monitors the sequencer status. The sequencer supports two disk formats (IBM ST506 and ESDI). Several control alternatives are programmable. These registers are accessed by the microcontroller. The sequencer performs the requested function until it completes (sequencer sector count = 0, or error) or the microcontroller resets the sequencer. The buffer controller should be setup and started before the sequencer.
The sequencer is programmed via the following registers:

Sequencer Command register
read
write
read long
write long
format track

Sequencer Status register
sequencer done
data address mark not found
write fault glitch
data ECC error
bad block detected
seek complete glitch
ready glitch
index timeout
iam timeout

Sequencer MSB Cylinder (Identity) register

Sequencer LSB Cylinder register

Sequencer Head/Flag register

Sequencer Sector register

Sequencer Track Sector Count register

Syndrome registers

GAP count

PLO count

Load State Counter (strobe)

Load State Field Address (strobe)

Sequencer Start (strobe)

The following procedure is used for sequencer operations:

1. Load sequencer MSB cylinder register
   Load sequencer LSB cylinder register
   Load sequencer head/flag register
   Load sequencer sector register
   Load sequencer track sector count register
   Load GAP and PLO registers (if format)
   Setup and start buffer controller
2. Load command register
3. Load state field address (strobe)
4. Load state counter (strobe)
5. Start (strobe)
6. Poll sequencer status until done

To abort the sequencer, write 00H to the command register.

SEQUENCER COMMAND REGISTER

This register is write only. When this register is written, the sequencer is initialized (reset, any command in progress aborts).

SEQUENCER STATUS REGISTER

This register is read only. The register is cleared when the sequencer command register is written or the board is reset.

SEQUENCER MSB CYLINDER (IDENTITY) REGISTER

This 4 bit, write only register is the encoded MSB cylinder value. The sequencer uses this value to check the ID of the target sector. This register is not shared with the host register. This register is uneffected by a reset. The following values are permissible:

MSB Cylinder (Binary)	Code (Hex)	Cylinder Range (decimal)
000	E	0-255
001	F	256-511
010	C	512-767
011	D	768-1023
100	6	1024-1279
101	7	1280-1535
110	4	1536-1791
111	5	1792-2047
	8	not allowed

SEQUENCER LSB CYLINDER REGISTER

This 8 bit, write only register is the LSB cylinder value. The sequencer uses this value to check the ID of the target sector. This register is not shared with the host interface. The microcontroller is responsible for loading/incrementing this register as need be. This register is uneffected by a reset.

SEQUENCER HEAD/FLAG REGISTER

This 8 bit, write only register is uneffected by a reset. This register is not shared with the host interface. The sequencer only reads this register. The microcontroller reloads this register when a head switch occurs.

SEQUENCER SECTOR REGISTER

This 8 bit, read/write register is the sector address. The sequencer uses this value to check the ID of the target sector. This register is uneffected by a reset.

At the end of a command, this contains the address of the last sector operated on (if no error) or the address of the sector in error. This register is not shared with the host interface. The sequencer reads this register for ID comparison and increments it as need be for multiple sector transfers. The sequencer does not increment the host sector register.

SEQUENCER TRACK SECTOR COUNT REGISTER

This 8 bit, write only register is loaded with the track sector count-1. This register is uneffected by a reset. This register should be loaded with the number of sectors to transfer this track (minus 1). The sequencer will automatically decrement it as need be for multiple sector transfers. This register is loaded with the number of sectors per track (minus 1) for a format command.

SYNDROME REGISTERS

These 8 bit, read only registers contain the ECC syndrome after reading a sector. The purpose of these registers is for the microcontroller to use the non-zero syndrome from a data ECC error to correct the data. These 7 registers are not effected by a reset.

GAP COUNT

This write only, 8 bit register is only used during a format track command. This register is not effected by a reset. See appendices F and G for additional details. The register is loaded with the byte count-1. This register is defined differently depending upon the drive configuration as follows:

TYPE	SECTORING	DEFINITION
ST506	SOFT	GAP1 and GAP3
ST506	HARD	GAP1
ESDI	SOFT	GAP1 and GAP3
ESDI	HARD	ISG

PLO SYNC COUNT

This write only, 8 bit register is used during format track and write commands. This register is not effected by a reset. See appendix G for additional details. For ESDI drives, it is loaded with the PLO (Phase Locked Oscillator) count as supplied (request configuration) by the ESDI drive in question. For ST506 drives, it is loaded with a constant. The number loaded is the byte count-1.

READ AHEAD CONSIDERATIONS

The sequencer can be made to read-ahead of the host request in anticipation of the next host access. The data is placed in the buffer until the buffer is full. If the next host request is not for the data read ahead, the microcontroller simply resets the sequencer (and buffer controller differential counter) before proceeding as usual. Otherwise, when the buffer controller is enabled, data transfers begin until the differential counter is 0 or the host request is completed.

LD1111 THEORY OF OPERATION

This chapter opens up the details of the LD1111 internal operations. The first problem is to understand the disk track format and the meaning of each field within the format. How the sequencer controls the disk format is explained. The buffer controller FIFO algorithm is explained. This chapter will clarify these problems by covering the standard track format, and explain the workings of the more critical logic sections used in processing realtime disk data.

TRACK FORMATS

The track format can be described by starting at an "arbitrary" reference point in a single track known as index. This is a pulse, supplied by the drive, that indicates the start of a track. The LD1111 sequencer assumes only the leading edge of the pulse is tightly controlled.

GAP1 - THE POST INDEX FIELD

From the leading edge of index there is a post index field referred to as GAP 1. This field may be written with any data, but the data is usually selected such that the PLO cannot achieve bit synchronization with the particular data pattern. This field is written only once on the track (during a Format command) and is not repeated anywhere else on the track. The length of this field, in bytes, is dependent on the sector size and motor speed variation of the disk spindle.

ID PLO SYNCHRONIZATION

The ID PLO synchronization field should be considered the start of the first sector. This field is repeated for the beginning of each sector on the track. This field is written with a specific data pattern (usually low or high frequency patterns are chosen) to allow the phase lock oscillator (PLO) to achieve bit synchronization. The length, in bytes, of this field is dependent on the acquisition time of the PLO. Some formats require more than one PLO field.

ADDRESS MARKS AND BYTE SYNCHRONIZATION

Following the PLO synchronization field, which achieves bit synchronization, is one character with unique characteristics used to achieve byte synchronization. Depending on the data encoding scheme, a character referred to as the address mark or sync character is written purposely violating some part of the encoding method. Hence, when the character is read back and decoded, the violation is detected and byte synchronization is established. Some formats use a field of the same character written multiple times or use multiple characters of a different value to ensure synchronization.

ID FIELD

Every sector on the track, and on the disk, has some number of bytes used to uniquely distinguish that sector from any other sector. These bytes comprise the ID Field or address of the sector. This field as a minimum must contain the cylinder number, head number, and sector address on the track. Other information may be included that gives details of the sector size or availability of the particular sector. In general though, the ID field is used to locate a particular sector for a data read or to update the data with a write data operation.

ID CHECKSUM

The ID field is so critical to the proper identification of a sector, it is always protected with some type of data checksum. This is done to ensure the integrity of the sector ID before proceeding with any operation on the sector data field. The checksum is generated when the ID field is formatted. This checksum is appended to the ID field and is regenerated every time the ID field is read. If there is a bit error in the ID field, the logic will detect a condition indicating an error exists in the data read. This checksum usually takes the form of a 16 bit CRC polynomial which can only detect an error, but sometimes an extended ECC polynomial is used which may have better error detection properties than the 16 bit CRC polynomial.

INTRASECTOR PAD

This is a null field which serves functions more important than merely being the point at which one distinguishes between the ID field and the Data field within the sector.

This null field is read to allow more time for the ID field checksum to pass completely through the checksum generator. This is required in most applications since there is usually somewhat more than one byte of latency between what the VCO reads and when the NRZ data is processed in the sequencer. During a Write command, starting with the field following the Intrasector Pad, the fields in the sector are rewritten. This implies that the write gate signal is asserted. The last byte of the Intrasector Pad is designated as a write splice area since this is the time the write current will be

applied to the drive heads. This write splice is isolated in a known area of the pad, where read gate will deassert before attempting to read the following field. For some formats this is an absolute requirement for protection of the data.

DATA PLO SYNCHRONIZATION

This field is a preamble to the data portion of the sector to allow the PLO to regain bit synchronization which is lost due to the necessity of deasserting read gate during the write splice in the pad. The characteristics of this field are similar to those required of the ID PLO field. The major difference is this field is rewritten with each Write command where as the ID PLO field is only written during a Format command.

DATA FIELD ADDRESS MARKS AND FRAMING

This is similar to the field in the ID portion of the sector, but can assume a different format. The purpose is to establish byte synchronization with the disk data once the bit synchronization was established in the PLO field. It is actually preferred or required that this synchronization format be different, in soft sector drives, such that the logic can discern the difference between the beginning of an ID field and the beginning of a Data field. This is accomplished by using a different framing character from the one in the ID field (if one is even present in the ID field). To simplify the data separator design, the special Address Mark character that violates the encode pattern is kept the same for both the ID and Data fields. This alone is sufficient for byte synchronization. Usually, as a double check on the byte framing, there is another known but not uniquely encoded character immediately following the Address Mark. These Framing Marks are made different between the ID field and the Data field.

DATA FIELD

The data field contains the actual information of interest to the disk user. Data fields vary in length but the number of bytes per data field is normally fixed for one given disk drive. Often, as a matter of convenience the number is chosen as one of four standard powers of 2. These are 128, 256, 512, and 1024 bytes. The data field is formatted with the same byte value repeated as many times as there are bytes in the Data field. Read commands do not alter the values in the data field but transfer from disk to a controller buffer. The write command is used to update or change the information actually stored in the data field.

DATA CHECKSUM FIELD

As with the ID field, the integrity of the data read from the disk and sent to the host is extremely important. Incorrect data must never be sent unknowingly to the host. For this reason, an ECC polynomial generator residue is always appended to the Data field. Unlike the CRC polynomial commonly applied to the ID field, the ECC polynomial also has the ability to correct most data errors as well as detect them. The polynomial should be chosen such that it has strong abilities to detect single and double burst errors and correct single burst errors with a very low probability of miscorrection.

DATA FIELD PAD

A pad is again used immediately succeeding the Data Checksum field to allow for the NRZ data to be processed before deasserting read gate. During this pad, write gate should remain asserted. Write gate should be deasserted soon after this pad. The timing is not as critical here as in the Intrasector Pad. This is due to the fact that the sector has essentially ended in terms of any critical information, hence read gate would never be asserted in this area.

GAP3 - POST SECTOR FIELD

Following the Data pad is a neutral field used to allow reliable data recovery even in drives with larger than average spindle speed variance. This field has historically been referred to as GAP3 or the speed tolerance field. A particular data pattern is chosen, one that will not permit the PLO to obtain bit synchronization, and is written during a Format command. The length, in bytes, of this field is related to the sector length and disk spindle speed tolerance. This field is neither read nor written for a Read or Write command. The major purpose of this field is to allow margin for writing the complete Data and Checksum fields in the event the disk spindle speed slows during the writing process. It is of course a convenient time for the microcontroller to perform between sector tasks.

GAP4 - PRE-INDEX FIELD

Starting with the ID PLO synchronization field through GAP3 (Post Sector field), each of those sections is repeated in each sector. When the given number of sectors per track has been exhausted during a Format Track command, the last sector is followed by a Pre Index Gap. This is referred to as Gap 4. The purpose of

this last field is twofold.
First, this field is only written once, during execution of a format command. It is written with one particular byte pattern repeated until the occurrence of the leading edge of the index pulse. The byte pattern is chosen such that the PLO cannot achieve bit synchronization in this field. Essentially, from the last sector until the index signal, the track is formatted with data such that it is clear this is not a usable area of the disk. The length of this field is not always predictable within an accuracy of one or two bytes. For this reason the field is started after GAP3 of the last sector and continued until the leading edge of index. The major reason one cannot predict the length of this field is again due to spindle speed variations. Thus, this is a final speed tolerance buffer for the purpose of formatting the track.

SEQUENCER OPERATION

(to be provided)

BUFFER OPERATION

(to be provided)

CLOCK FREQUENCY AND DATA RATE

The clock supplied to the LD1111, with either a crystal or an oscillator output, is used to drive the internal state machines. The frequency is related to the bit data rate in that the frequency is greater than the data rate.

CLOCK (MHz)	HALFCLK(MHz)	Max Data Rate
20	10	10 Mhz
24	12	16 Mhz

ECC CORRECTION ALGORITHM

The LD1111 has a choice of 2 fixed ECC polynomials. ST506 drives always use the 32 bit polynomial. ESDI drives always use the 56 bit polynomial. CRC-CCITT is always used for ID fields. The hardware generates/checks the polynomials on the fly. ECC/CRC registers are preset to "1" before calculations begin. If an ECC error is detected, after a disk read, the resulting syndrome will be non-zero. The microcontroller software computes the offset, correction pattern, and correctability from the syndrome.

32 BIT POLYNOMIAL

This software technique will generate the pattern and displacement for correctable ECC burst of 5 bits or less (32 bit polynomial). The displacement is from the first data sync byte. The algorithm is shown for 512 byte sectors.

Displacement	Definition
0	0A1H - data sync mark
1	0F8H - data address mark
2	first data byte
	data bytes
513	last data byte
514	ECC #1 (bits 31-24)
515	ECC #2 (bits 23-16)
516	ECC #3 (bits 15-8)
517	ECC #4 (bits 7-0)

1. Displacement = ((2 512 4) ~ 8) 8-1
2. Shift residue right 1 bit (shifting LS bit into carry and a 0 into the MS bit).
3. If carry = 0 then goto 5
4. Residue = residue XOR 8A050222H
5. If Residue bits 31-24 and 18-0 = 0 then goto 9 (correctable)
6. If displacement = 0 then uncorrectable
7. Displacement = displacement - 1
8. Goto 2
9. Shift count = remainder of (displacement/8)
10. Shift residue right according to the shift count (shifting in 0 to the MS bit).
11. Displacement = displacement - shift count
12. Displacement = displacement/8
13. XOR data at displacement 0 with residue bits 23-16
    XOR data at displacement 1 with residue bits 15-8

56 BIT POLYNOMIAL

This software technique will generate the pattern and displacement for correctable ECC burst of 12 bits or less (56 bit polynomial). The displacement is from the first data sync byte. The algorithm is shown for 512 byte sectors.

Displacement	Definition
0	0A1H - data sync mark
1	0F8H - data address mark c
2	first data byte
	data bytes
513	last data byte
514	ECC #1 (bits 55-48)
515	ECC #2 (bits 47-40)
516	ECC #3 (bits 39-32)
517	ECC #4 (bits 31-24)
518	ECC #5 (bits 23-16)
519	ECC #6 (bits 15-8)
520	ECC #7 (bits 7-0)

1. Displacement = ((2 512 7) ~ 8) 8-1
2. Shift residue right 1 bit (shifting LS bit into carry and a 0 into the MS bit).
3. If carry = 0 then goto 5
4. Residue = residue XOR 8A050222800080H
5. If Residue bits 55-48 and 35-0 = 0 then goto 9 (correctable)
6. If displacement = 0 then uncorrectable
7. Displacement = displacement - 1
8. Goto 2
9. Shift count = remainder of (displacement/8)
10. Shift residue right according to the shift count (shift ing in 0 to the MS bit).
11. Displacement = displacement - shift count
12. Displacement = displacement/8
13. XOR data at displacement 0 with residue bits 47-40
    XOR data at displacement 1 with residue bits 39-32
    XOR data at displacement 2 with residue bits 31-24

CIRCUITS OF INTEREST

This section gives further details on specific LD1111 functions which don't really relate to bit sequencing or buffer management.

ESDI SEEK COMPLETE STATUS

Since ESDI drives don't have a seek complete signal, a circuit creates synthetic seek complete status for use in the host status register.

TEST CONSIDERATIONS

Several features have been included to increase the ability for the microcontroller to verify LD1111 functionality. Previously, three methods have been discussed. The microcontroller can reset the host interface and observe the results. The microcontroller can test the buffer RAM. The microcontroller can test read/write registers. The following paragraphs detail additional microcontroller tests for the LD1111.

MSB CYLINDER/TEST FUNCTIONS

The upper 4 bits of the MSB cylinder register (see 5.5) are used for test. These bits are normally written as zero. The test functions are read only bits.

TEST REGISTER

This 8 bit, write only register is used setting drive control options and for test purposes. It is cleared to all zero by a reset.

TEST

This 8 bit, read only register, is used for test purposes to verify hardware status signals.

DRIVE/HEAD REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
ECC	SL1	SL0	SEL1	HD3	HD2	HD1	HD0

STATUS REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
BSY	RDY	WRF	SKC	DRQ	COR	IDX	ERR

CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
RSV	RSV	RSV	RSV	RWC	RST	DI	RSV

DIGITAL INPUT REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
CHG	WRG~	HD3~	HD2~	HD1~	HD0~	DS1~	DS0~

PORT 1 (ST506)

D7	D6	D5	D4	D3	D2	D1	D0
W0	W1	PCP	LED	W2	W3	DIR~	STEP~

PORT 1 (ESDI)

D7	D6	D5	D4	D3	D2	D1	D0
W0	W1	W2	LED	REQ~	CD~	W3	W4

PORT 3

D7	D6	D5	D4	D3	D2	D1	D0
RD~	WR~	CC0	CC1	WP0	INT~	RSV	WP1

DRIVE CONTROL INPUT

D7	D6	D5	D4	D3	D2	D1	D0
RSV	ATTN	READY	SEEKC	RSV	TRK0	CMD0	CMD1

DRIVE CONTROL OUTPUT

D7	D6	D5	D4	D3	D2	D1	D0
DT1	DT0	DCYC	POLY	SKON	HARD	ESDI	LOWC

HEAD SELECT

D7	D6	D5	D4	D3	D2	D1	D0
RSV	RSV	RSV	RSV	HEAD3	HEAD2	HEAD1	HEAD0

BUFFER CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
RSV	RSV	LONG	RDV	EMPTY	DIR	ALL	DAC

BUFFER STATUS REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
RSV	RSV	RSV	RSV	RSV	DONE	ODET	MXDET

SECTOR SIZE REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
RSV	RSV	RSV	RSV	BS9	BS8	BS7	BS6

MAX HEAD REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
RSV	RSV	RSV	RSV	MXHD3	MXHD2	MXHD1	MXHD0

SEQUENCER COMMAND REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
RSV	RSV	RSV	RSV	LONG	FORMAT	WRITE	READ

SEQUENCER STATUS REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
IAM	GLTH	IDTO	BAD	ECC	WTFG	DAM	DONE

SEQUENCER HEAD/FLAG REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
X	SS1	SS0	X	HD3	HD2	HD1	HD0

CYLINDER/TEST FUNCTION

D7	D6	D5	D4	D3	D2	D1	D0
SCTC1~	SCTC	HCMP	SCMP	CYL11	CYL10	CYL9	CYL8

TEST REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
RSV	RSV	EDMA	MDS14	TEST4	TEST3	TEST2	TEST1

TEST

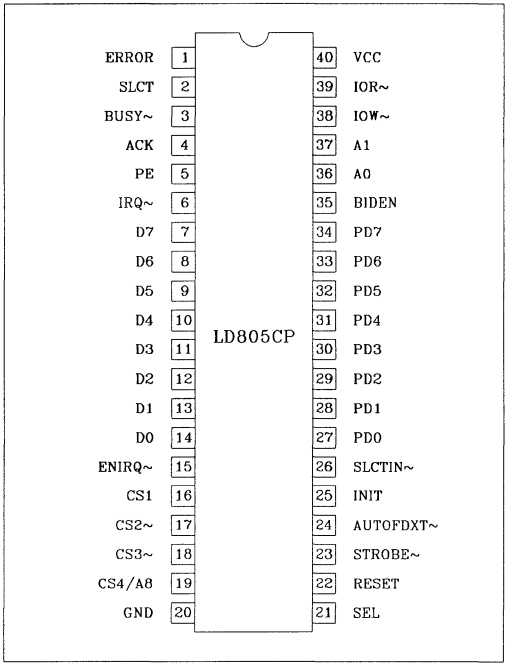
D7	D6	D5	D4	D3	D2	D1	D0
SECTC	HWCTC1	HWCTC	SWCTC1	SWCTC	RSV	RSV	RSV

COMMUNICATION 6

BIDIRECTIONAL PARALLEL PORT

DESCRIPTION

The LD805 is a monolithic Bidirectional Parallel Port Controller (BPPC) designed specifically for IBM personal computer systems and compatibles or the CENTRONICS type of handshaking.
It is fabricated in advanced 3u NMOS process, and meets TTL input/output requirements.



FEATURES

* Replaces 12 TTL logic chips
* Fully compatible with all new PS/2 systems
* Direct replacement of logic for PC/XT/AT
* High output sink current (24 mA typ.)
* Single 5 volt operating supply
* High data transfer rate (500 Kbs typ.)
* Pin selectable LPT1 or LPT2

APPLICATIONS

* CENTRONICS printer port
* IBM PS/2 bidirectional printer port
* IBM PC/XT/AT upgrade printer port
* External bidirectional I/O port
* External tape back-up port
* IBM PC/XT/AT to PS/2 data transfer I/O

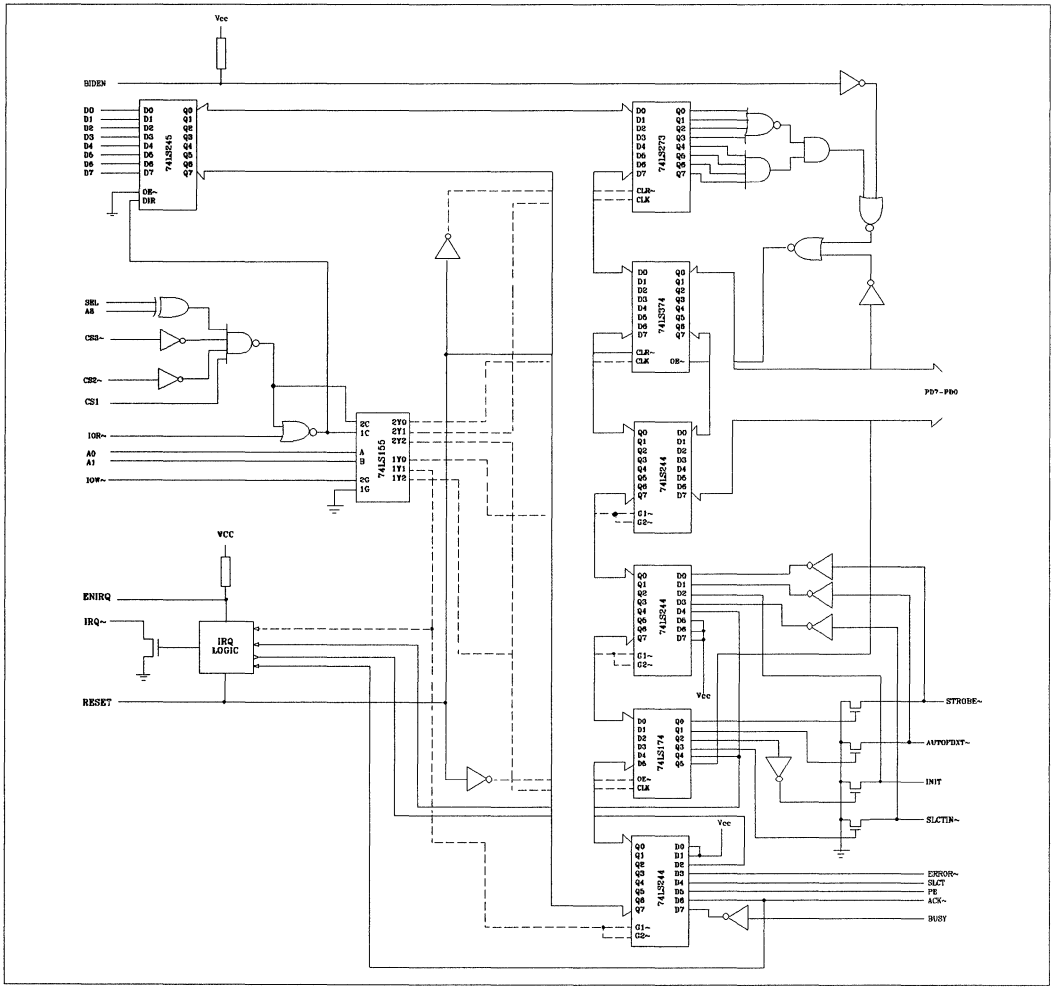
ORDERING INFORMATION

Part number	Package	Operating temperature
LD805CP40	Plastic	0°C to +70°C
LD805CJ44	PLCC	0°C to +70°C

GENERAL DESCRIPTION

The LD805 is designed to receive or transmit data via an 8-bit of parallel bus and to perform minimum handshaking. High output sink and source currents are provided for long cable length and TTL compatibility. Some of the external decoding logics are implemented to reduce external components and maintain flexibility for different types of system designs.

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
ERROR	1	I	General purpose input or line printer error. This is an output from the printer to indicate an error by holding it low during error condition.
SLCT	2	I	General purpose input or line printer selected. This is an output from the printer to indicate that line printer has been selected.
BUSY~	3	I	General purpose input or line printer busy. An output from the printer to indicate the printer is not ready to accept data.
ACK	4	I	General purpose input or line printer acknowledge. An output from the printer to indicate that data has been accepted successfully.
PE	5	I	General purpose input or line printer paper empty. An output from the printer to indicate out of paper.
IRQ~	6	O	General purpose interrupt output (open drain active low). To signal the state of the external device.
D7-D0	7-14	I/O	Bidirectional data I/O. Eight, three state data bus to transfer information to or from peripheral/printer.
ENIRQ~	15	I	Interrupt source selection (active low). This pin internally pulled high to select internal interrupt logic. Tying this pin to GND will disable the IRQ output. Pulsing this pin will set the internal interrupt logic to latched state, IRQ will reset by reading the STATUS register.
CS1	16	I	Chip select 1 (active high). To enable the LD805 operation, this pin has to go high while CS2 and CS3 are low.
CS2~	17	I	Chip select 2 (active low). See CS1.
CS3~	18	I	Chip select 3 (active low). See CS1.
CS4/A8	19	I	Chip select 4 or A8 of address bus. See SEL.
GND	20	O	Ground. Signal and power ground.
SEL	21	I	Address select. The normal or inverted state of the CS4/A8 can be selected by tying this pin to GND or VCC.
RESET	22	I	External reset input (active high). A positive going pulse will reset the internal registers and IRQ, the LD805 will be set for output mode.
STROBE~	23	I/O	General purpose I/O or strobe output (open drain active low). To transfer latched data to the external peripheral or printer.

SYMBOL DESCRIPTION

Symbol	Pin	Symbol type	Pin description
AUTOFDXT~	24	I/O	General purpose I/O or line printer autofeed (open drain active low). To signal the printer for continuous form feed.
INIT	25	I/O	General purpose I/O or line printer initialize (open drain active high). To signal the line printer to enter internal initialization routine.
SLCTIN~	26	I/O	General purpose I/O or line printer select (open drain active low). To select the line printer.
PD7-PD0	34-27	I/O	Bidirectional parallel I/O (three state). To transfer data in or out of LD805. PD7-PD0 are latched during the output mode.
BIDEN	35	I	I/O direction select. Internally pulled-up to enable the software controlled direction.
A1-A0	37-36	I	Address lines. To access the internal registers.
IOW~	38	I	I/O write strobe (active low). A low on this pin (while CS1=h, CS2=I, CS3=I, CS4=x and IOR~=h) will write the contents of the data bus into the addressed destination.
IOR~	39	I	I/O read strobe (active low). A low on this pin (while CS1=h, CS2=I, CS3=I, CS4=x, IOW~=h) will transfer the contents of the addressed register to the data bus.
VCC	40	I	Power supply input.

PROGRAMMING TABLE:

A1	A0	IOW~	IOR~
0	0	PORT REGISTER	PORT REGISTER
0	1	I/O SELECT REGISTER	STATUS REGISTER *
1	0	CONTROL REGISTER	COMMAND REGISTER

* Reading the status register will reset the IRQ output.

I/O SELECT REGISTER (WRITE ONLY)

CONTROL REGISTER (D5)	BIDEN	I/O SELECT REGISTER (D7-D0)	PORT MODE
0	x	xxxxxxxx	OUTPUT
1	1	xxxxxxxx exp. AA Hex	OUTPUT
1	1	10101010	INPUT
1	0	xxxxxxxx	INPUT

REGISTERS DESCRIPTION

PORT REGISTER
Bidirectional printer port.
Writing to this register during output mode will transfer the contents of the data bus to the PD7-PD0 ports. Reading this register during input mode will transfer the states of the PD7-PD0 to the data bus. This register will be set to the output mode after reset or keeping the BIDEN input in low state.

PR BIT 7-0:
PD7-PD0 bidirectional I/O ports.

STATUS REGISTER
This register provides the state of the printer outputs and the interrupt condition.

SR BIT 1-0:
Not used. Are set to "1" permanently.

SR BIT-2:
Interrupt condition.
0 = An interrupt is pending.
This bit will be set to "0" at the falling edge of the ACK input.
1 = No interrupt is pending.
Reading the STATUS REGISTER will set this bit to "1".

SR BIT-3:
ERROR input state.
0 = ERROR input is in low state.
1 = ERROR input is in high state.

SR BIT-4:
SLCT input state.
0 = SLCT input is in low state.
1 = SLCT input is in high state.

SR BIT-5:
PE input state.
0 = PE input is in low state.
1 = PE input is in high state.

SR BIT-6:
ACK input state.
0 = ACK input is in low state.
1 = ACK input is in high state.

SR BIT-7:
BUSY~ input state.
0 = BUSY~ input is in high state.
1 = BUSY~ input is in low state.

COMMAND REGISTER
The state of the STROBE~, AUTOFDXT~, INIT, SLCTIN~ pins, and interrupt enable bit can be read by this register regardless of the I/O direction.

COM BIT-0:
STROBE~ input pin.
0 = STROBE~ pin is in high state.
1 = STROBE~ pin is in low state.

COM BIT-1:
AUTOFDXT~ input pin.
0 = AUTOFDXT~ pin is in high state.
1 = AUTOFDXT~ pin is in low state.

COM BIT-2:
INIT input pin.
0 = INIT pin is in low state.
1 = INIT pin is in high state.

COM BIT-3:
SLCTIN~ input pin.
0= SLCTIN~ pin is in high state.
1= SLCTIN~ pin is in low state.

COM BIT-4:
Interrupt mask.
0= Interrupt (IRQ~ output) is disabled.
1= Interrupt (IRQ~ output) is enabled.

COM BIT 7-5:
Not used. Are set to "1" permanently.

CONTROL REGISTER.
Writing to this register will set the state of the STROBE~, AUTOFDXT~, INIT, SLCTIN~ pins, and interrupt mask register.

CON BIT-0:
STROBE~ output control bit.
0= STROBE~ output is set to high state.
1= STROBE~ output is set to low state.

CON BIT-1:
AUTOFDXT~ output control bit.
0= AUTOFDXT~ output is set to high state.
1= AUTOFDXT~ output is set to low state.

CON BIT-2:
INIT output control bit.
0= INIT output is set to low state.
1= INIT output is set to high state.

CON BIT-3:
SLCTIN~ output control bit.
0= SLCTIN~ output is set to high state.
1= SLCTIN~ output is set to low state.

CON BIT-4:
Interrupt output control bit.
0= IRQ~ output is disabled.
1= IRQ~ output is enabled.

CON BIT-5:
I/O select. Direction of the PD7-PD0 can be selected by setting or clearing this bit.
0= PD7-PD0 are set for bidirectional mode.
1= PD7-PD0 are set for output mode.

CON BIT 7-6:
Not used.

I/O SELECT REGISTER
Software controlled I/O select.
Bidirectional mode can be selected by keeping the BIDEN input in low state and setting **CON BIT-5** to zero. Writing a "AA" Hex to the I/O SELECT REGISTER will enable the input mode and any other values will set the PD7-PD0 to the output mode.
Hardware/software I/O select can also be achieved, by utilizing the BIDEN pin. Setting **CON BIT-5** to zero and writing "AA" Hex to the I/O SELECT REGISTER. PD7-PD0 will be in input mode when BIDEN is held high, otherwise output mode.

REGISTER CONFIGURATIONS

PORT REGISTER (READ/WRITE)

D7	D6	D5	D4	D3	D2	D1	D0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

STATUS REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
BUSY~	ACK	PE	SLCT	ERROR STATE	IRQ	1	1
					1 = No interrupt 0 = Interrupt		

COMMAND REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	IRQ STATUS	SLCTIN~	INIT	AUTO-FDXT~	STROBE~
			0 = IRQ disabled 1 = IRQ enabled				

CONTROL REGISTER (WRITE ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
--	--	I/O SELECT	IRQ MASK	SLCTIN~	INIT	AUTO-FDXT~	STROBE~
	0 = Output 1 = Bidirectional		0 = IRQ output disabled 1 = IRQ output enabled				

AC ELECTRICAL CHARACTERISTICS

$T_A = 25°$ C, $V_{cc} = 5.0$ V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
T_1	Address setup time	15	20	35	ns	
T_2	Write pulse width	60	70	80	ns	
T_3	Data setup time	15	20	35	ns	
T_4	Reset pulse width	20	40	50	ns	
T_5	Output delay from IOW~	50	100	150	ns	
T_6	IOR~ delay from select	20	30	40	ns	
T_7	Read pulse width	60	70	80	ns	
T_8	Data delay time	60	80	100	ns	
T_9	IRQ~ delay from ACK	40	50	100	ns	
T_{10}, T_{11}	ENIRQ~ setup time	20	35	45	ns	
T_{13}	ACK pulse width	60	70	80	ns	
T_{14}	Data hold time	15	20	35	ns	
T_{16}	Data hold time from IOR~	60	70	80	ns	

ABSOLUTE MAXIMUM RATINGS

Operating supply range	5 Volts ± 5%
Voltage at any pin	GND - 0.3V to V_{CC} + 0.3V
Operating temperature	0°C to +70°C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

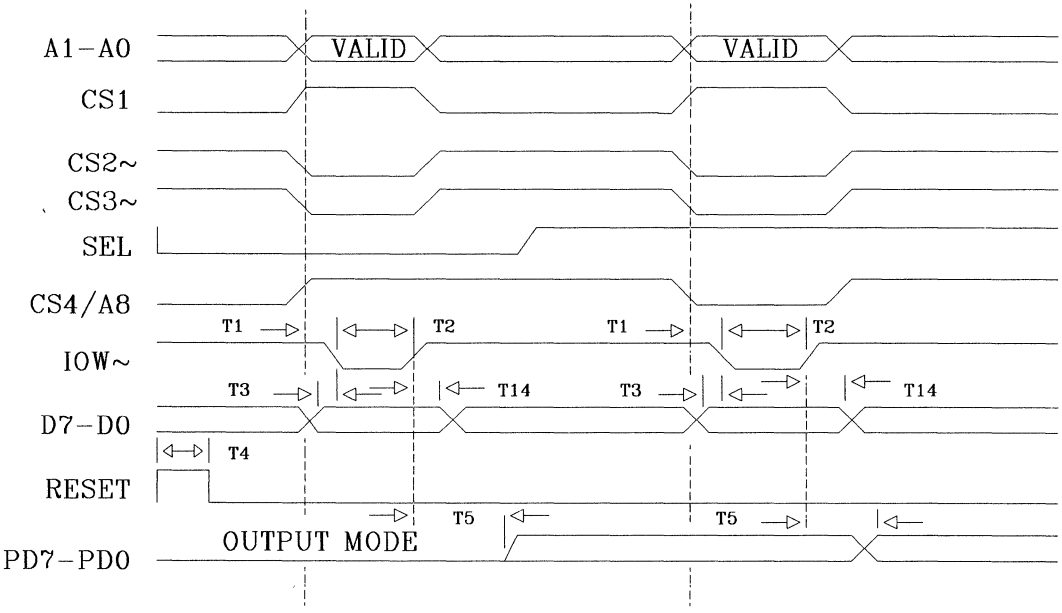
T_A=25° C, V_{CC}=5.0v ± 5% unless otherwise specified

Symbol	Parameters	Limits			Unit	Conditions
		min	typ	max		
I_{IL}	Input low current	-10			uA	exp. BIDEN, ENIRQ
I_{IH}	Input high current			10	uA	
E_{IL}	Input low current	-1			mA	BIDEN, ENIRQ
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	exp. SLCTIN, INIT, AUTOFDXT, STROBE
EV_{IH}	Input high level	3.5			V	SLCTIN, INIT, STROBE, AUTOFDXT
V_{OL}	Output low level pin D7-D0			0.4	V	Isink=24 mA
V_{OH}	Output high level	2.4			V	Isource=12 mA
PV_{OL}	Output low level pin PD7-PD0			0.4	V	Isink=8 mA
PV_{OH}	Output high level pin PD7-PD0	2.5			V	Isource=8 mA
EV_{OL}	Output low level pin STROBE,INIT, AUTOFDXT, SLCTIN			0.4	V	Isink=8 mA

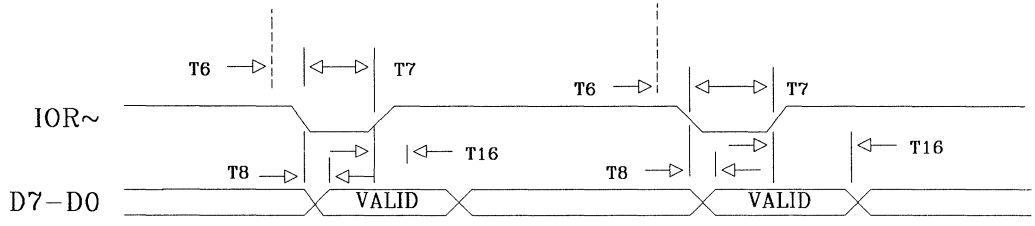
6

TIMING DIAGRAM

WRITE TIMING CYCLE

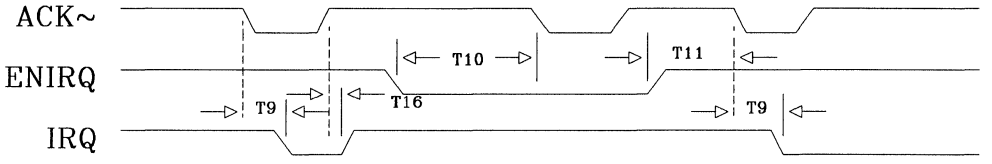


READ TIMING CYCLE

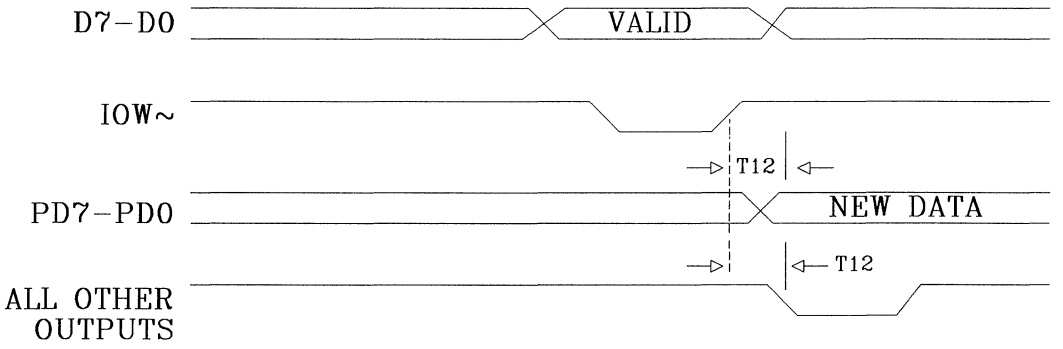


TIMING DIAGRAM

INTERRUPT TIMING CYCLE

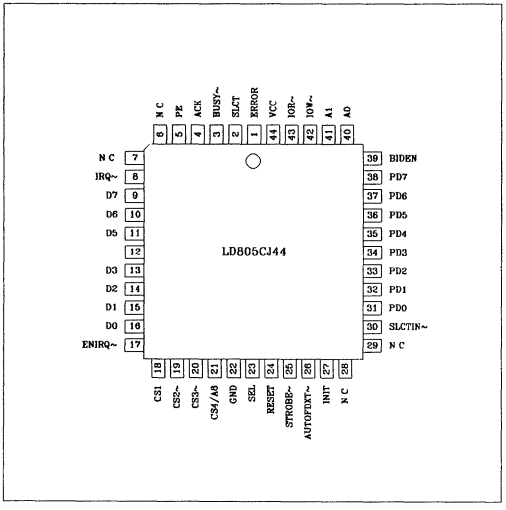


I/O TIMING



6

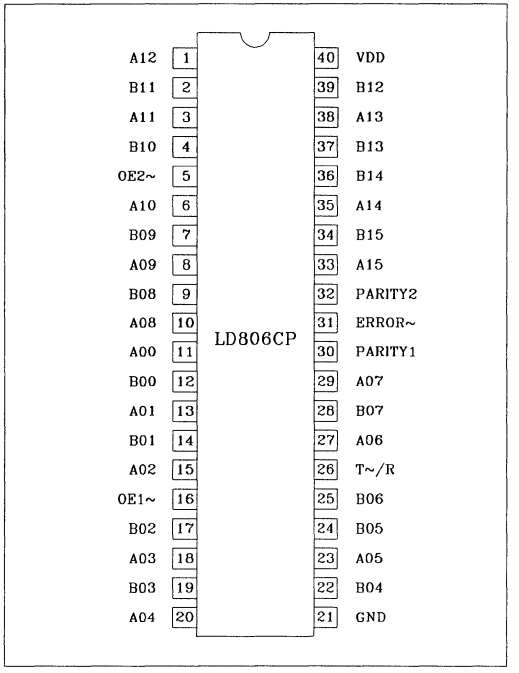
44 PIN PLCC PINOUT



DUAL CMOS TRANSCEIVER

DESCRIPTION

The LD806 is a dual 74F657 transceiver chip set in a single package. Fabricated in an advanced 2u CMOS technology to meet the TTL input/out requirements, the LD806 is designed to provide high output sink and source currents. It contains two sets of non-inverting buffers with three-state outputs and two sets of 8-bit parity generators.



FEATURES

* One chip replaces two 74F657 chips
* Three-state outputs
* 24 mA output sink current
* 15 mA output source current
* Combines two 74F245 and 74F280A chips
* Ideal in applications where light bus locking and high drive outputs are required
* Single 5 volt operating voltage

APPLICATIONS

* 16-bit transceiver bus
* IBM memory bus/card
* Add on extention boards
* 16-bit parity check
* Bus drivers

ORDERING INFORMATION

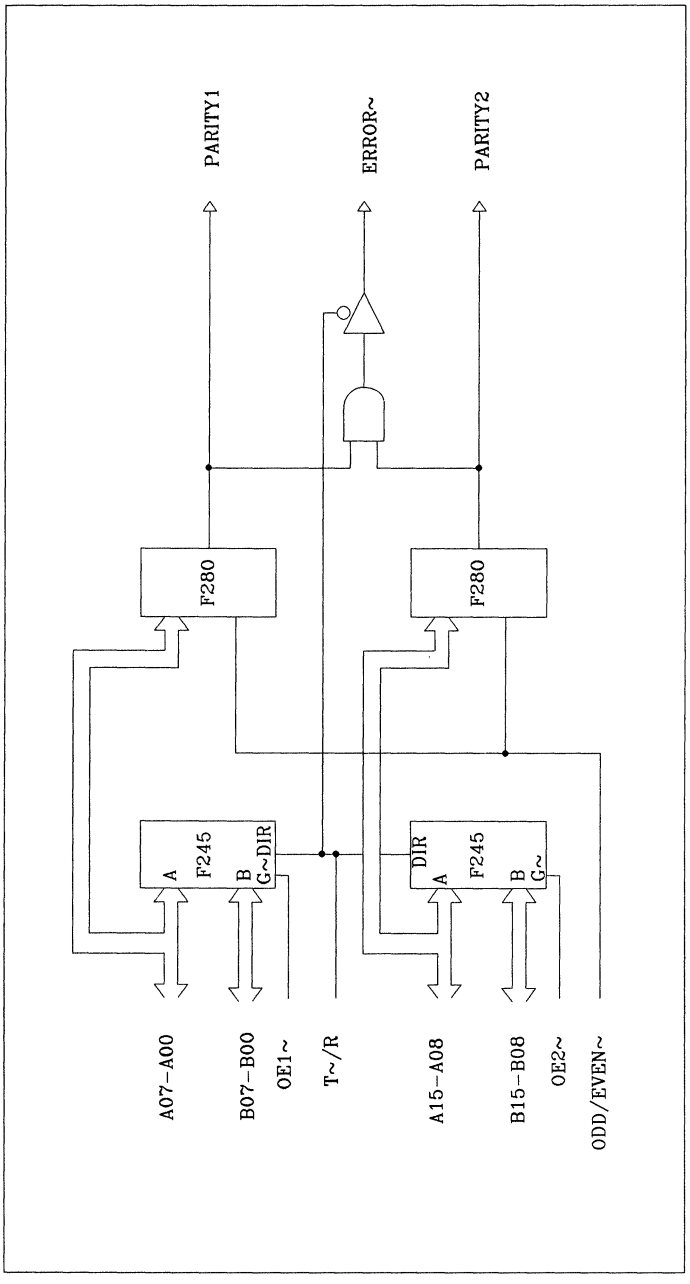
Part number	Package	Operating Temperature
LD806CP40	Plastic	0 ° C to +70 ° C
LD806CJ44	PLCC	0 ° C to +70 ° C

GENERAL DESCRIPTION

The LD806 contains two sets of octal bidirectional buffers with three-state outputs and two sets of 8-bit parity generator/checkers. The buffers sink 24 mA and source 15 mA at both A and B ports. The direction of the flow of data through the bidirectional buffer is determined by the T~/R input. A low on the T~/R enables data to flow from A to B ports and a high enables data to flow from B to A ports. A high on the OE~ inputs forces both A and B ports into a high impedance condition.

The parity select input determines whether an even or odd number of bits on the A ports are high. If the ODD/EVEN~ input is high and an even number of A inputs are high, then the parity output is high. The parity of the data received on the A port is compared with the parity select input. If the parities are not equal the ERROR~ output is low. The ODD/EVEN~ input is high in the 40-pin dip package.

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
A12	1	I/O	Bit-12 of Port A bus.
B11	2	I/O	Bit-11 of Port B bus.
A11	3	I/O	Bit-11 of Port A bus.
B10	4	I/O	Bit-10 of Port B bus.
OE2~	5	I	Chip select 2. (active low) A low on this pin will enable the A15-A08/B15-B08 data bus operation.
A10	6	I/O	Bit-10 of Port A bus.
B09	7	I/O	Bit-9 of Port B bus.
A09	8	I/O	Bit-9 of Port A bus.
B08	9	I/O	Bit-8 of Port B bus.
A08	10	I/O	Bit-8 of Port A bus.
A00	11	I/O	Bit-0 of Port A bus.
B00	12	I/O	Bit-0 of Port B bus.
A01	13	I/O	Bit-1 of Port A bus.
B01	14	I/O	Bit-1 of Port B bus.
A02	15	I/O	Bit-2 of Port A bus.
OE1~	16	I	Chip Select 1. (active low) A low on this pin will enable the A07-A00/B07-B00 data bus operation.
B02	17	I/O	Bit-2 of Port B bus.
A03	18	I/O	Bit-3 of Port A bus.
B03	19	I/O	Bit-3 of Port B bus.
A04	20	I/O	Bit-4 of Port A bus.
GND	21	O	Signal and power ground.

SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
B04	22	I/O	Bit-4 of Port B bus.
A05	23	I/O	Bit-5 of Port A bus.
B05	24	I/O	Bit-5 of Port B bus.
B06	25	I/O	Bit-6 of Port B bus.
T~/R	26	I	Port direction select. A high on this pin will transfer the B15-B00 bus to A15-A00 Port. A low on this pin will transfer the A15-A00 bus to B15-B00 Port.
A06	27	I/O	Bit-6 of Port A bus.
B07	28	I/O	Bit-7 of Port B bus.
A07	29	I/O	Bit-7 of Port A bus.
PARITY1	30	O	Port A08-A00 parity bit. This pin stays high when the A08-A00 of the data bus has an even number of parity bits. Programmable parity selection is provided on the PLCC package only.
ERROR~	31	O	Parity Error. (three state) This pin will go low if the parity of data received on the A port is not equal to the parity select pin.
PARITY2	32	O	Port A15-A08 parity bit. Same as PARITY1.
A15	33	I/O	Bit-15 of Port A bus.
B15	34	I/O	Bit-15 of Port B bus.
A14	35	I/O	Bit-14 of Port A bus.
B14	36	I/O	Bit-14 of Port B bus.
B13	37	I/O	Bit-13 of Port B bus.
A13	38	I/O	Bit-13 of Port A bus.
B12	39	I/O	Bit-12 of Port B bus.
Vcc	40	I	Power supply input . Most positive supply voltage.
ODD/EVEN	*	I	Parity bit select. Even parity is selected when this pin is low.

*** available in the 44 pin plcc only**

LD806 TRUTH TABLE:

Note: It is valid for one data port and associated OEx~ and PARITYx~.

Number of data inputs that are high	OE~	T/R~	ODD/EVEN~ *	PARITY	ERROR~	OUTPUT MODE
EVEN						
0,2,4,6,8	L	L	H	L (I)	L	Transmit
	L	L	H	H (I)	H	Transmit
	L	L	L	L (I)	H	Transmit
	L	L	L	H (I)	L	Transmit
	L	H	H	H (O)	(Z)	Receive
	L	H	L	L (O)	(Z)	Receive
ODD						
1,3,5,7	L	L	H	L (I)	H	Transmit
	L	L	H	H (I)	L	Transmit
	L	L	L	L (I)	L	Transmit
	L	L	L	H (I)	H	Transmit
	L	H	H	L (O)	(Z)	Receive
	L	H	L	H (O)	(Z)	Receive
DON'T CARE	H	X	X	(Z)	(Z)	(Z)

* Note: This pin is only available in the 44-pin package. The 40-pin package is ODD parity only (ODD/EVEN~ = H).

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ±5% unless otherwise specified.

Symbol	Parameters	Limits			Units	Conditions
		max	typ	min		
T_1	Propagation delay A>B or A<B	55	52	50	ns	
T_2	Propagation delay A>B or A<B	50	45	43	ns	
T_3	Propagation delay B>PARITY	85	80	78	ns	
T_4	Propagation delay B>PARITY	85	80	78	ns	
T_5	Propagation delay A>ERROR~	55	50	48	ns	
T_6	Propagation delay A>ERROR~	55	50	48	ns	
T_7	Propagation delay PARITY~>ERROR~	55	50	48	ns	
T_8	Propagation delay PARITY~>ERROR~	55	50	48	ns	
T_9	Propagation delay OE1~>A	50	45	43	ns	
T_{10}	Propagation delay OE1~>A	80	75	72	ns	
T_{11}	Propagation delay OEx~>PARITYx	85	80	75	ns	
T_{12}	Propagation delay OEx~>PARITYx	65	60	57	ns	

ABSOLUTE MAXIMUM RATINGS

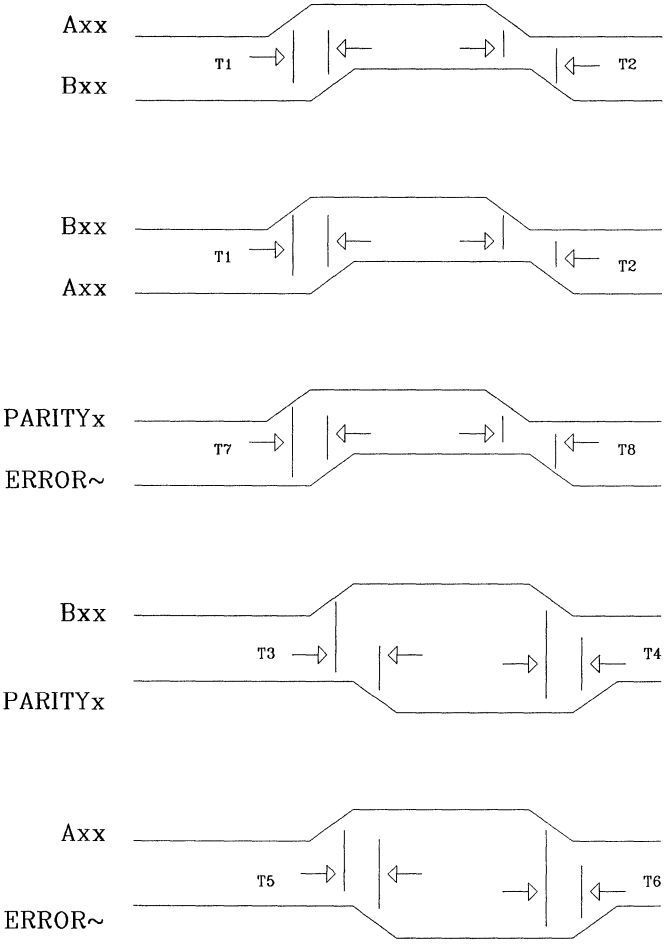
Operating supply range	5 Volts ± 5%
Voltage at any pin	GND -0.3V to V_{CC} +0.3V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

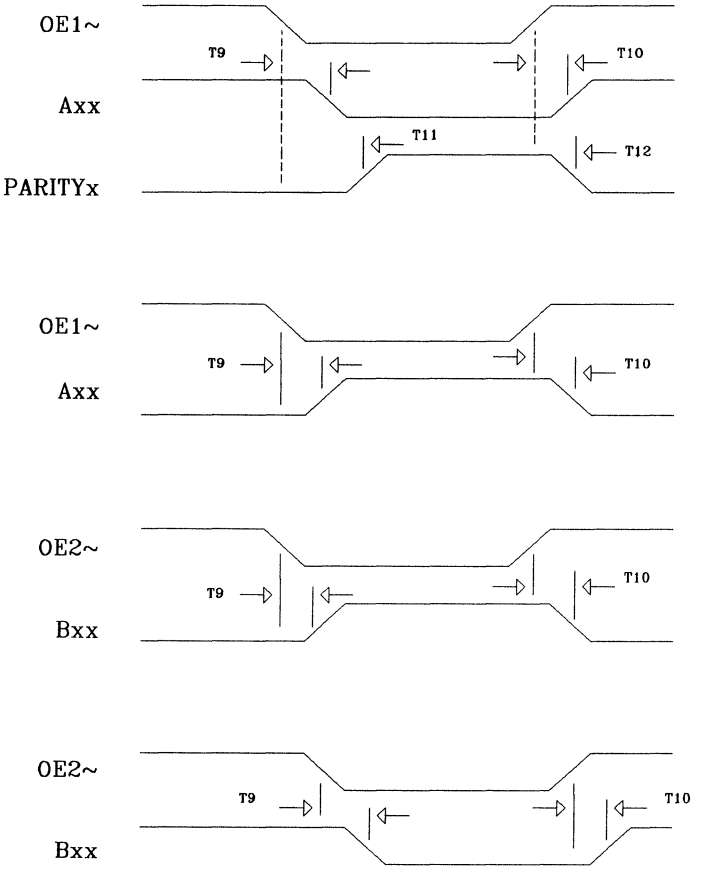
T_A=25° C, V_{CC}=5.0 V ±5% unless otherwise specified.

Symbol	Parameters	Limits			Units	Conditions
		min	typ	max		
I_{IL}	Input low current	-10			uA	exp. ODD/EVEN~
I_{IH}	Input high current			10	uA	exp. ODD/EVEN~
I_{IE}	Input low current	-2.5			mA	ODD/EVEN~ pin
I_{HE}	Input high current			1	mA	ODD/EVEN~ pin
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.4	V	exp. ERROR~, Isink=24mA
V_{OH}	Output high level	2.5			V	exp ERROR~, Isource=15mA
V_{LE}	Output low level			0.4	V	ERROR~, Isink=6mA
V_{HE}	Output high level	2.5			V	ERROR~, Isource=6mA
V_{IK}	Output leakage	-10		10	uA	all outputs

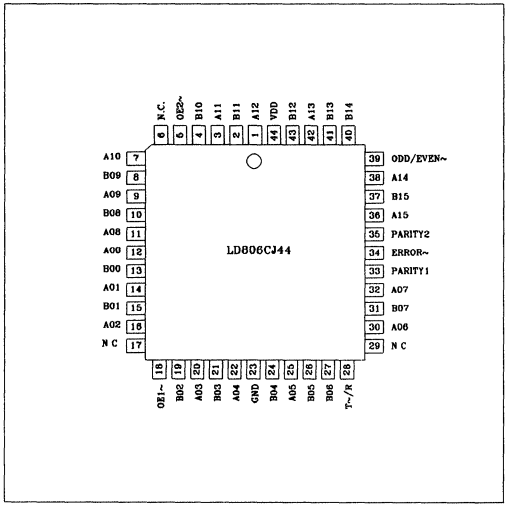
TIMING DIAGRAM



TIMING DIAGRAM



44 PIN PLCC PINOUT



APPLICATION NOTES

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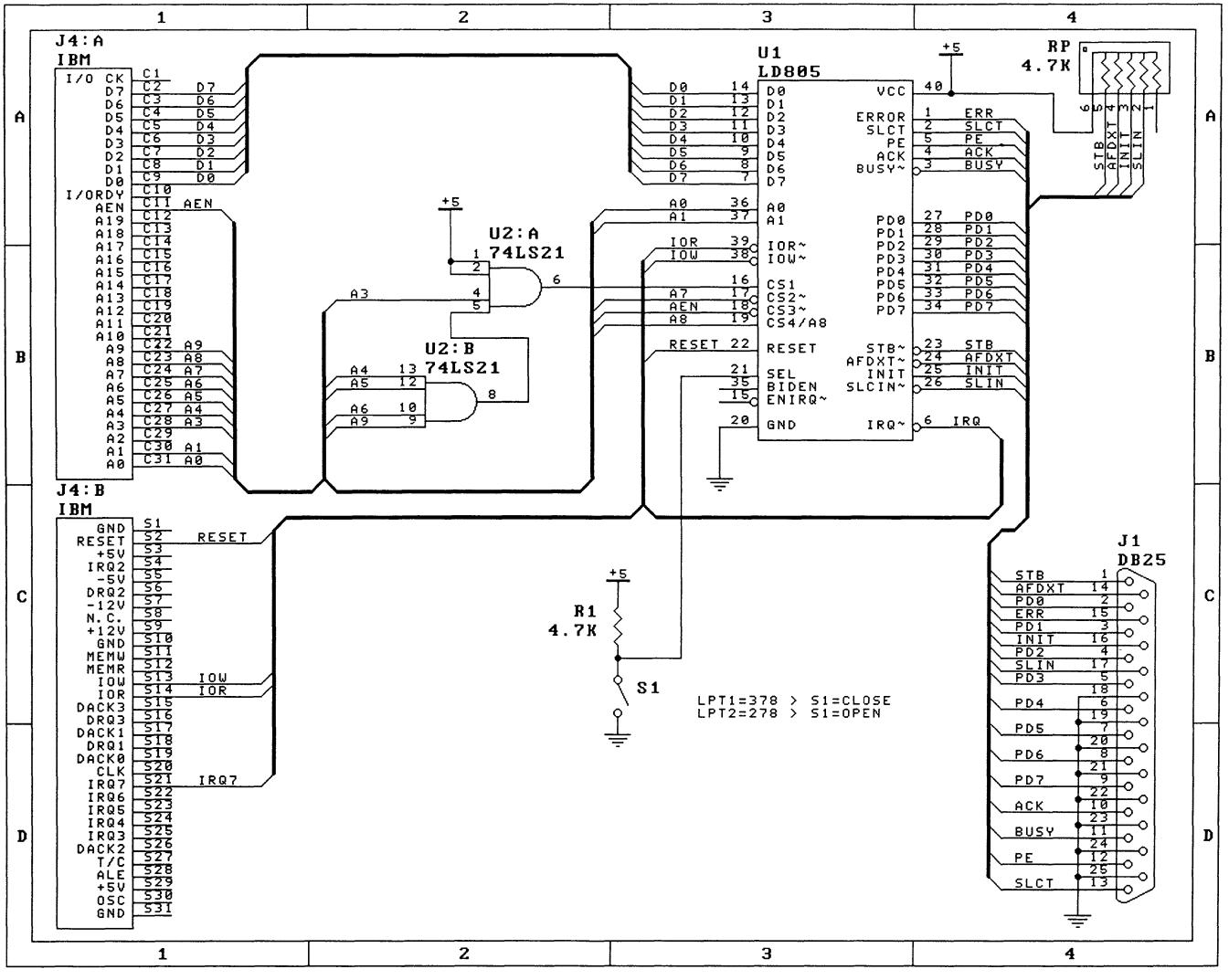
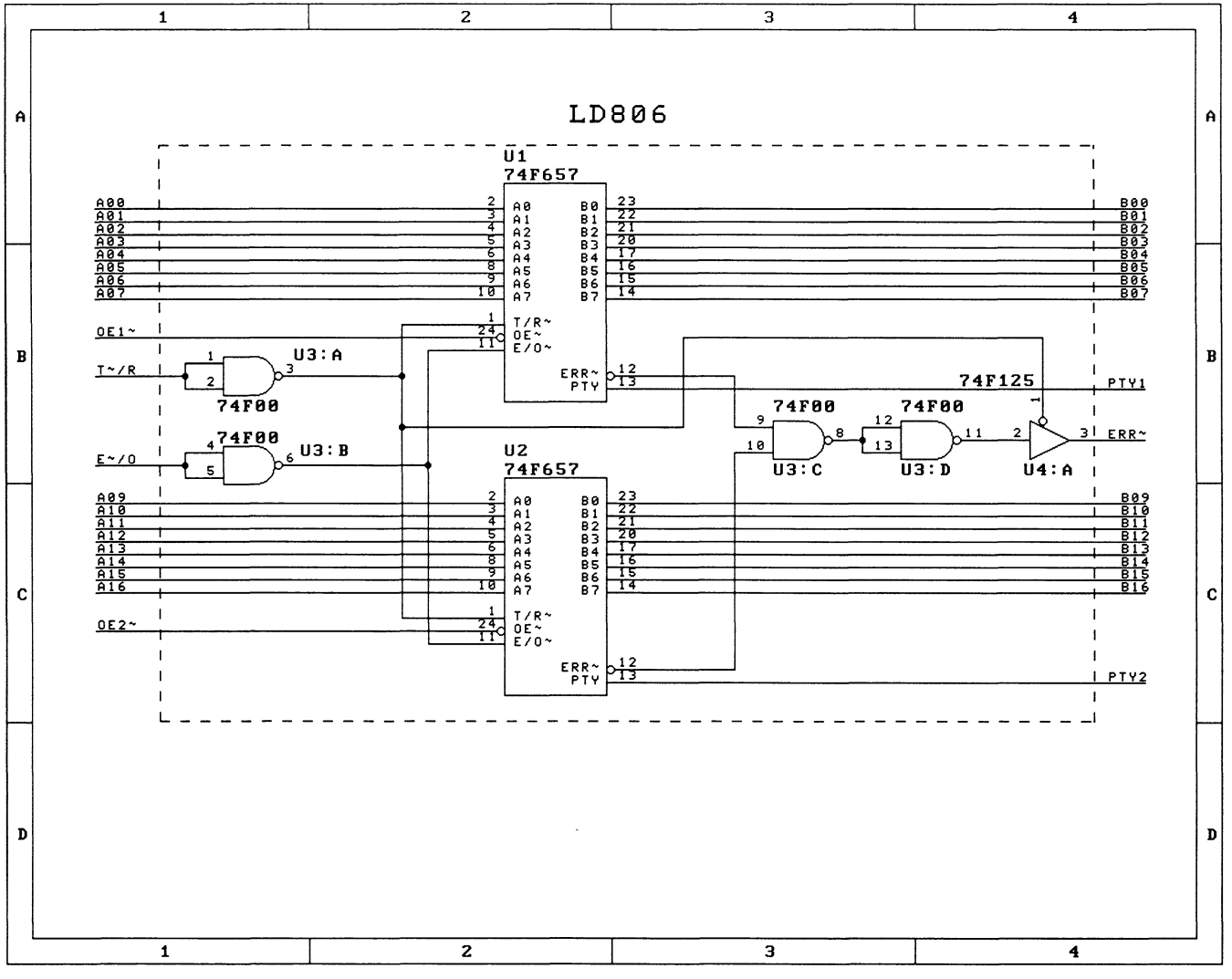
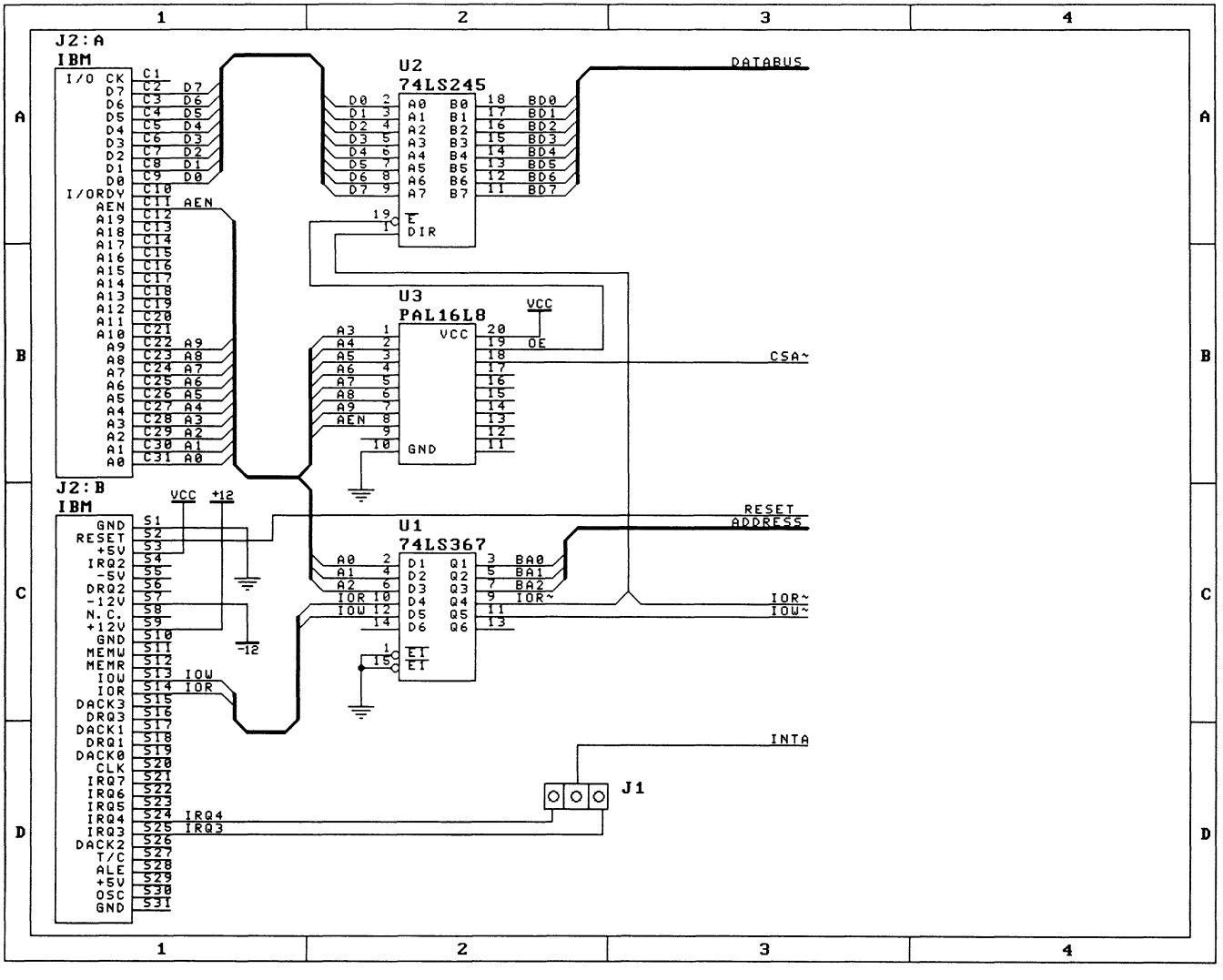
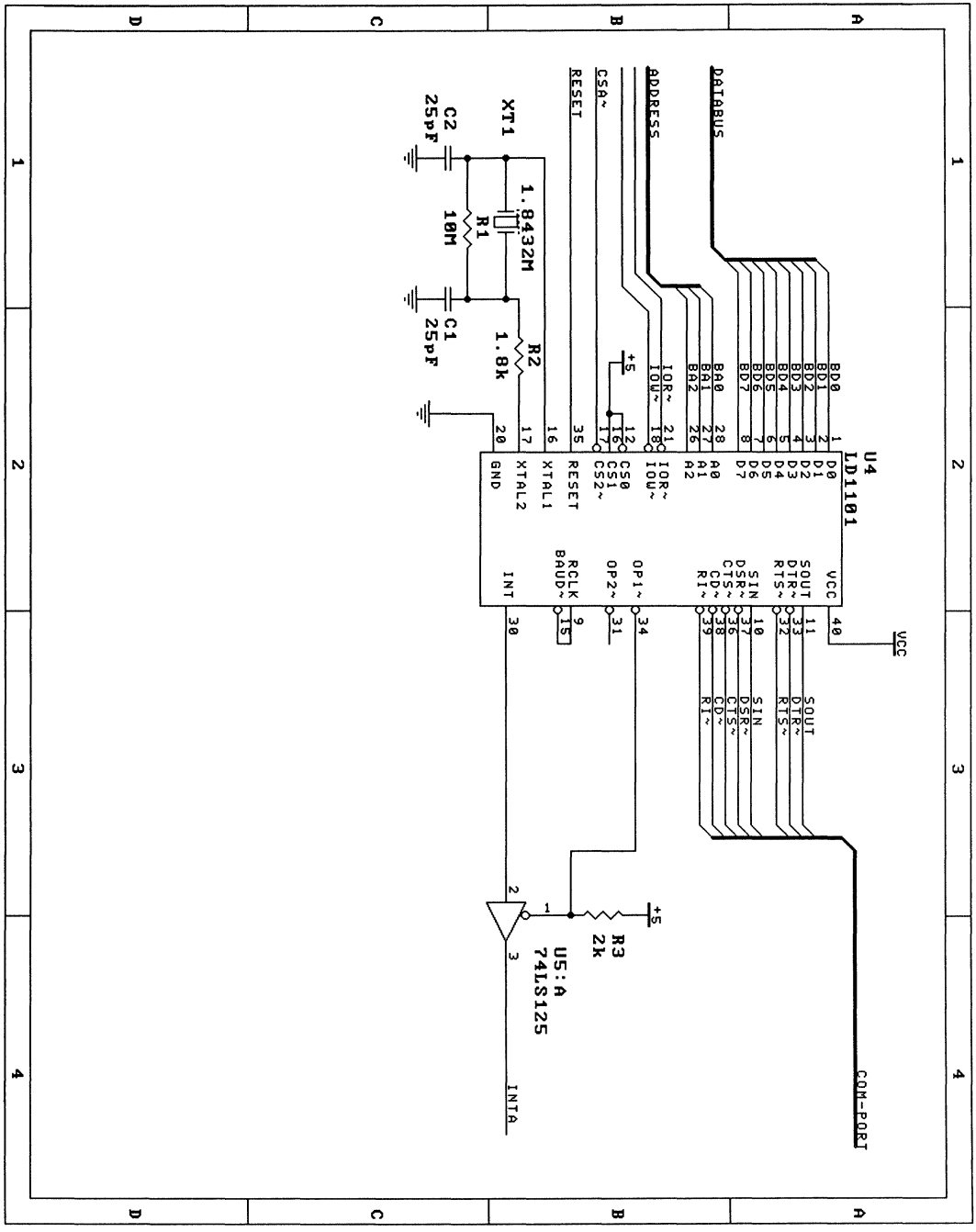
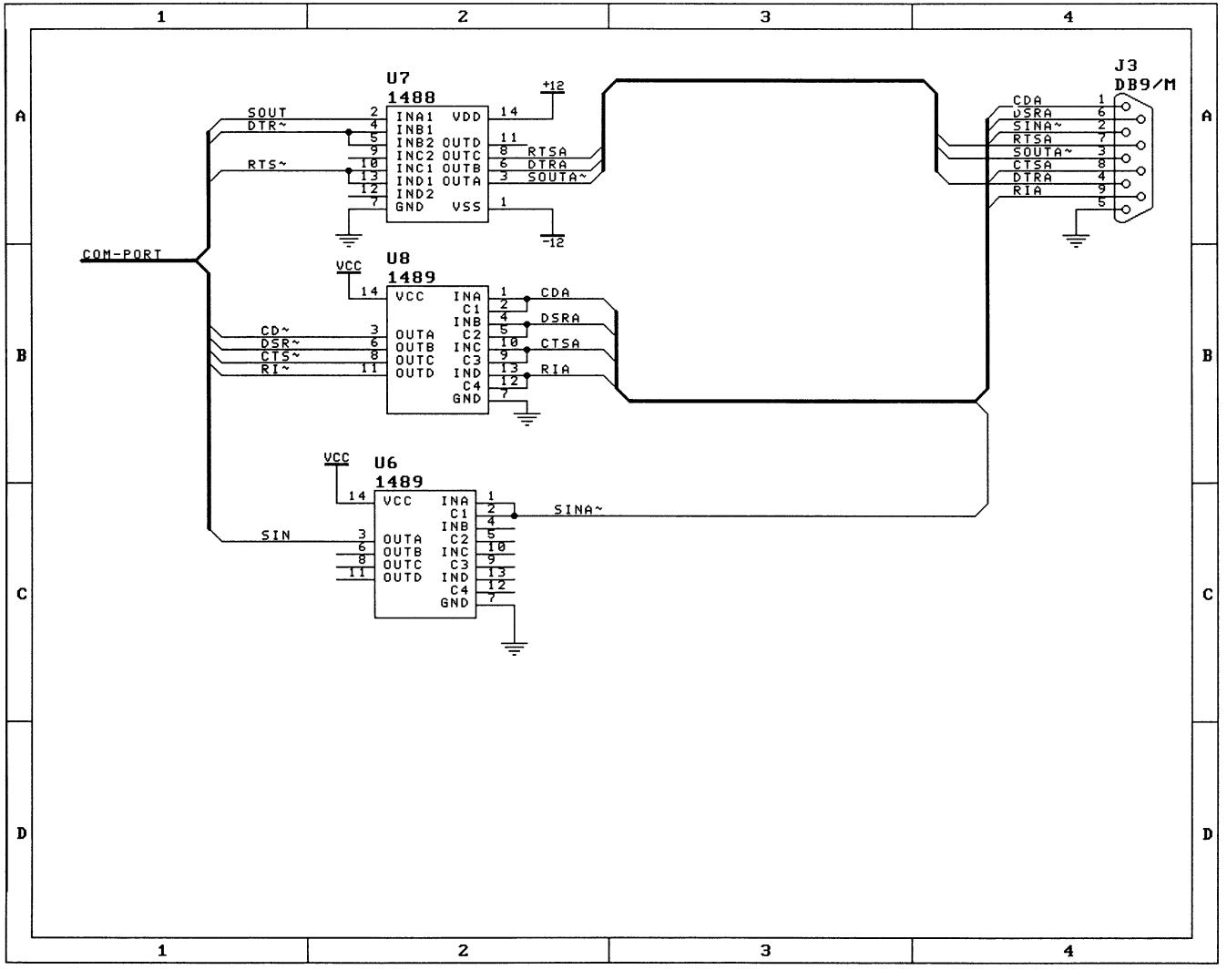
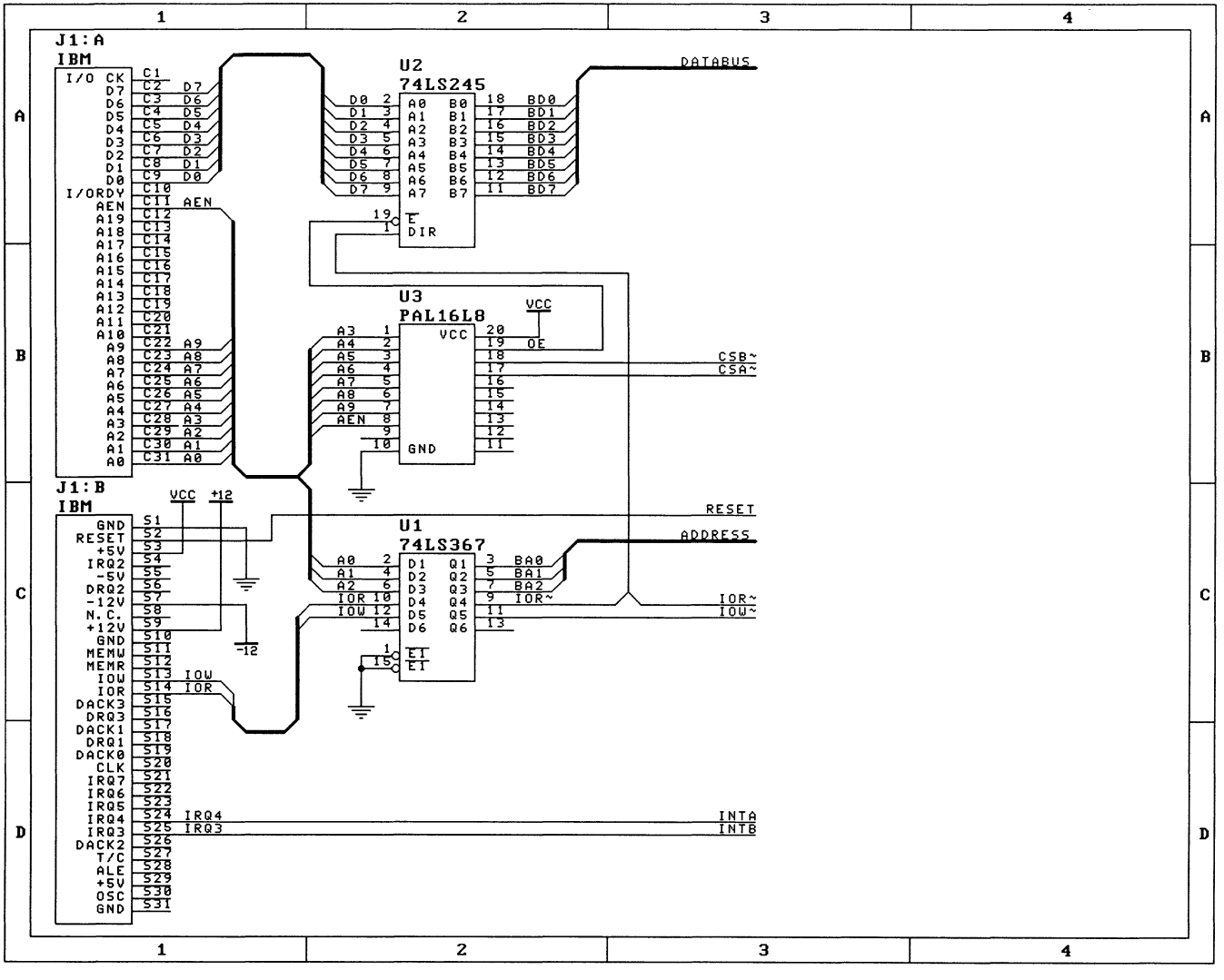

J4:A
IBM
I/O CK
D7
D6
D5
D4
D3
D2
D1
D0
I/ORDY
AEN
A19
A18
A17
A16
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
J4:B
IBM
GND
RESET
+5V
IRQ2
-5V
DRQ2
-12V
N.C.
+12V
GND
MEMW
MEMR
IOW
IOR
DACK3
DRQ3
DACK1
DRQ1
DACK0
CLK
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
DACK2
T/C
ALE
+5V
OSC
GND
U1
LD805
D0
D1
D2
D3
D4
D5
D6
D7
A0
A1
IOR~
IOW~
CS1
CS2~
CS3~
CS4/A8
RESET
SEL
BIDEN
ENIRQ~
GND
VCC
ERROR
SLCT
PE
ACK
BUSY~
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
STB~
AFDXT~
INIT
SLCIN~
IRQ~
U2:A
74LS21
U2:B
74LS21
RP
4.7K
R1
4.7K
S1
+5
J1
DB25
STB
AFDXT
PD0
ERR
PD1
INIT
PD2
SLIN
PD3
PD4
PD5
PD6
PD7
ACK
BUSY
PE
SLCT
LPT1=378 > S1=CLOSE
LPT2=278 > S1=OPEN

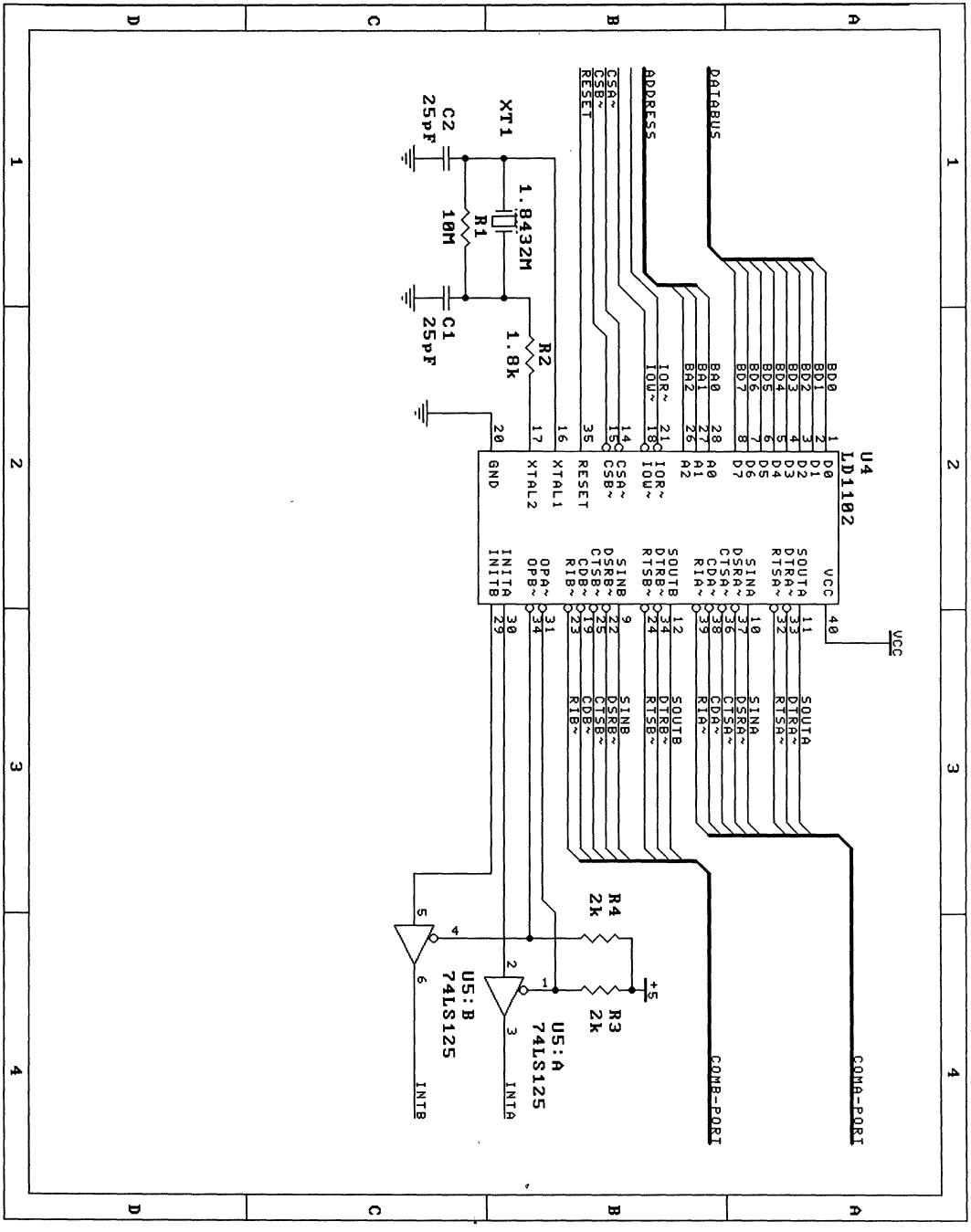

LD806
U1
74F657
U2
74F657
A00
A01
A02
A03
A04
A05
A06
A07
A09
A10
A11
A12
A13
A14
A15
A16
B00
B01
B02
B03
B04
B05
B06
B07
B09
B10
B11
B12
B13
B14
B15
B16
OE1~
OE2~
T~/R
E~/O
T/R~
OE~
E/O~
ERR~
PTY
U3:A
U3:B
U3:C
U3:D
U4:A
74F00
74F125
PTY1
PTY2
ERR~

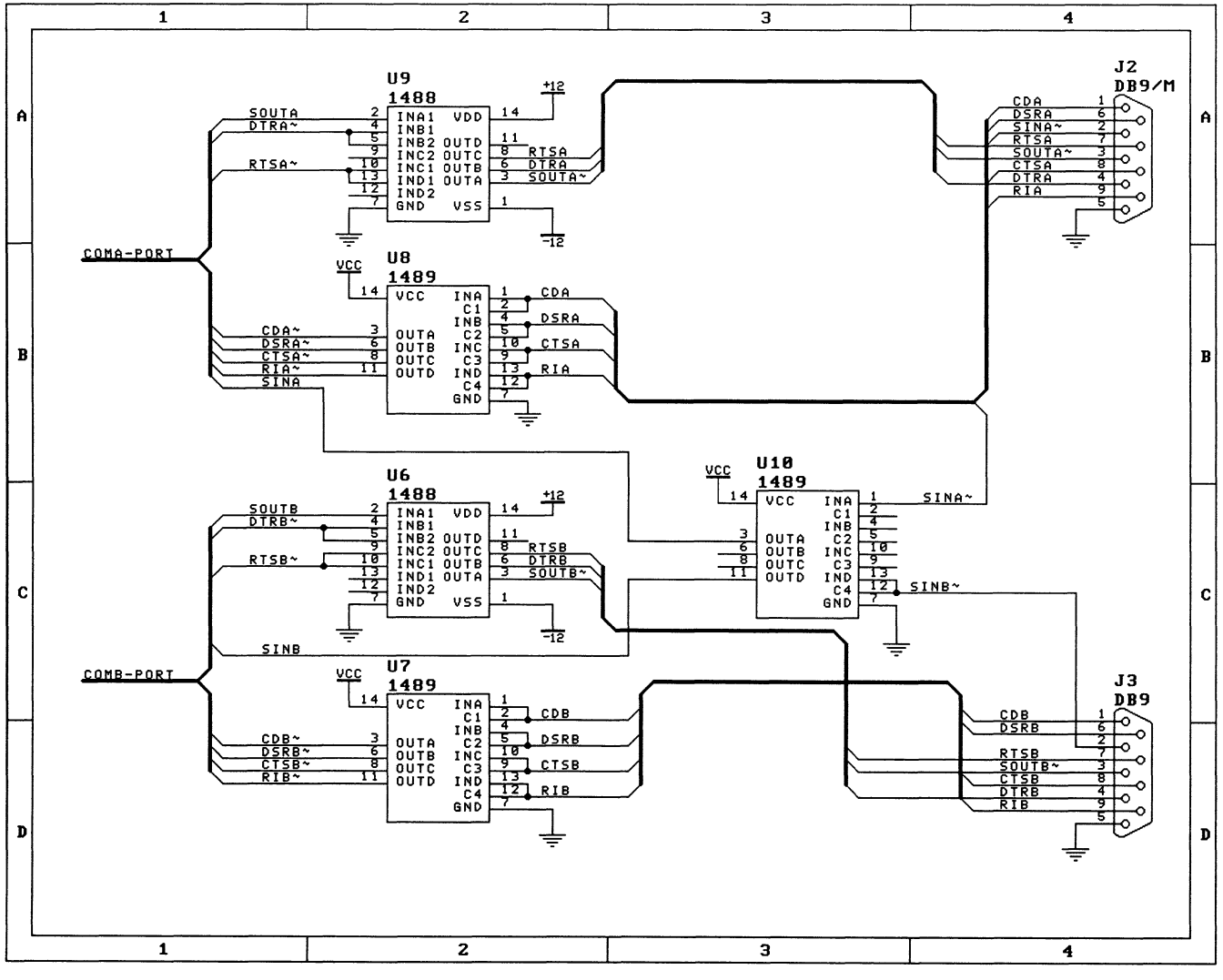

J2:A
IBM
I/O CK
D7
D6
D5
D4
D3
D2
D1
D0
I/ORDY
AEN
A19
A18
A17
A16
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
U2
74LS245
DIR
DATABUS
U3
PAL16L8
VCC
GND
OE
CSA~
J2:B
IBM
GND
RESET
+5V
IRQ2
-5V
DRQ2
-12V
N.C.
+12V
GND
MEMW
MEMR
IOW
IOR
DACK3
DRQ3
DACK1
DRQ1
DACK0
CLK
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
DACK2
T/C
ALE
+5V
OSC
GND
U1
74LS367
RESET
ADDRESS
IOR~
IOW~
INTA
J1
1
2
3
4
A
B
C
D

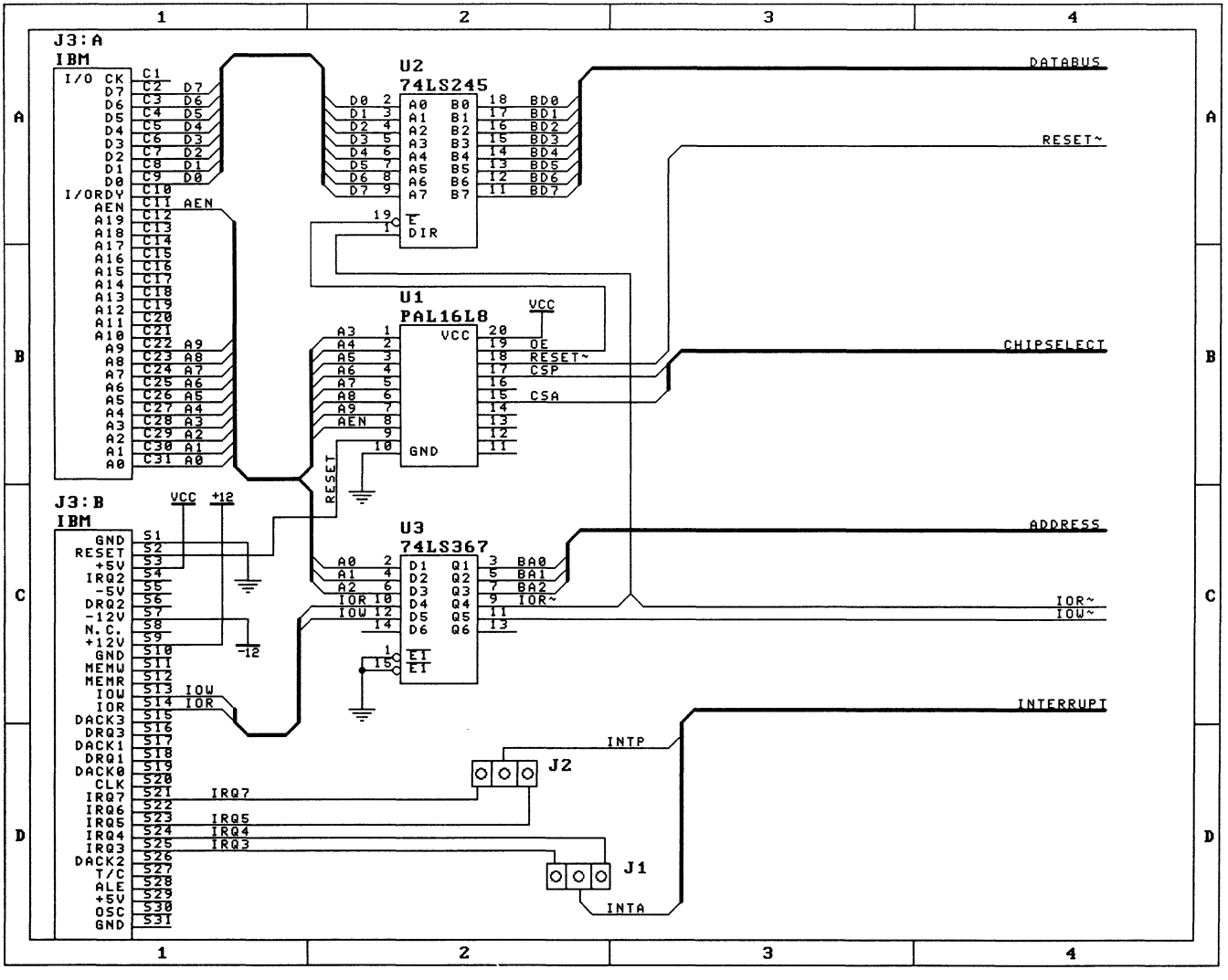

U4
LD1101
DATABUS
ADDRESS
CSA~
RESET
XT1
1.8432M
R1
10M
C2
25pF
C1
25pF
R2
1.8k
+5
VCC
GND
XTAL1
XTAL2
CS0
CS1
CS2~
IOR~
IOW~
INT
OP1~
OP2~
RCLK
BAUD~
SOUT
DTR~
RTS~
SIN
DSR~
CTS~
CD~
RI~
COM-PORT
U5:A
74LS125
R3
2k
INTA

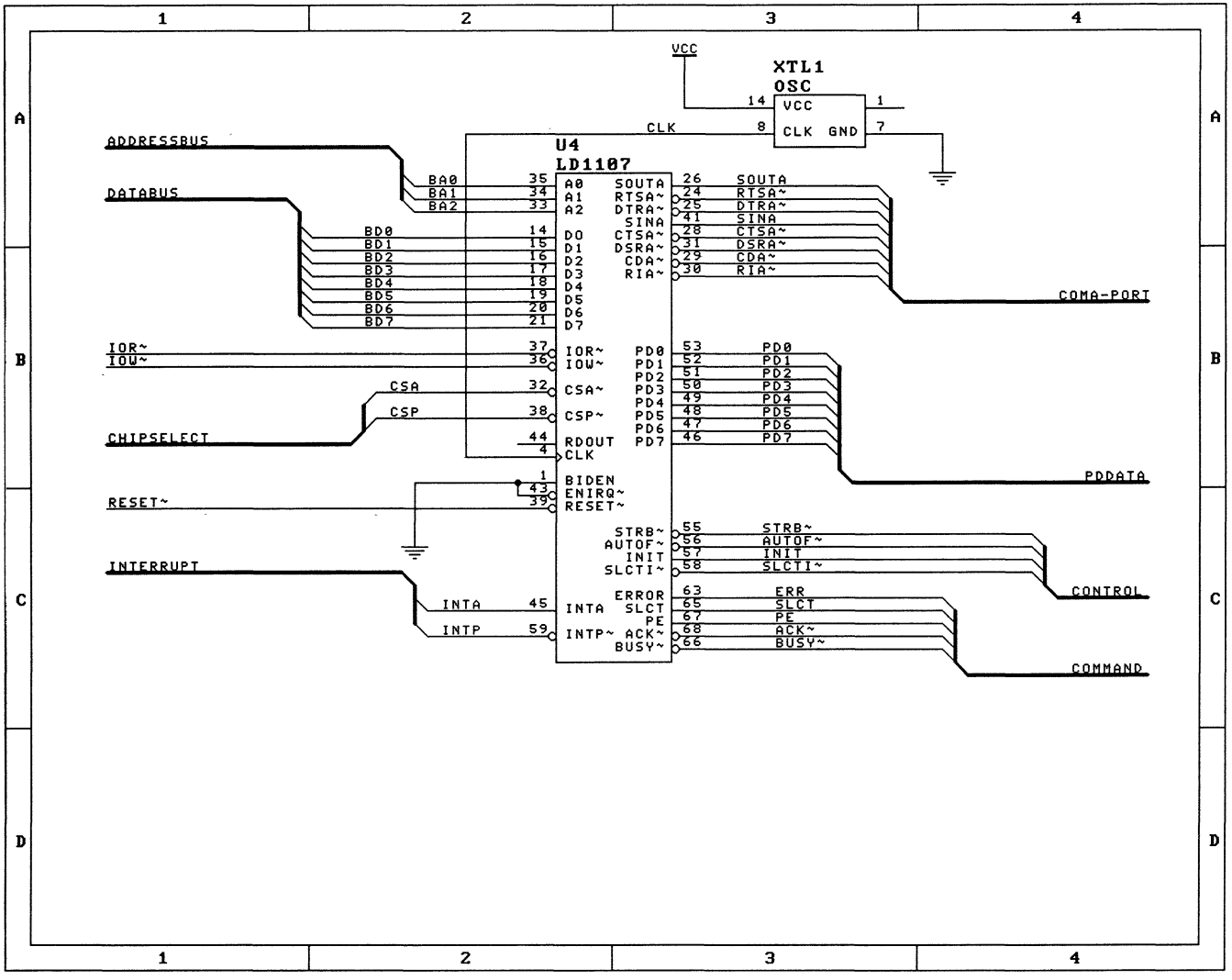

U7
1488
+12
-12
SOUT
DTR~
RTS~
INA1
INB1
INB2
INC2
INC1
IND1
IND2
GND
VDD
OUTD
OUTC
OUTB
OUTA
VSS
RTSA
DTRA
SOUTA~
J3
DB9/M
CDA
DSRA
SINA~
RTSA
SOUTA~
CTSA
DTRA
RIA
COM-PORT
U8
1489
VCC
CD~
DSR~
CTS~
RI~
CDA
DSRA
CTSA
RIA
U6
1489
SIN
SINA~
1
2
3
4
A
B
C
D

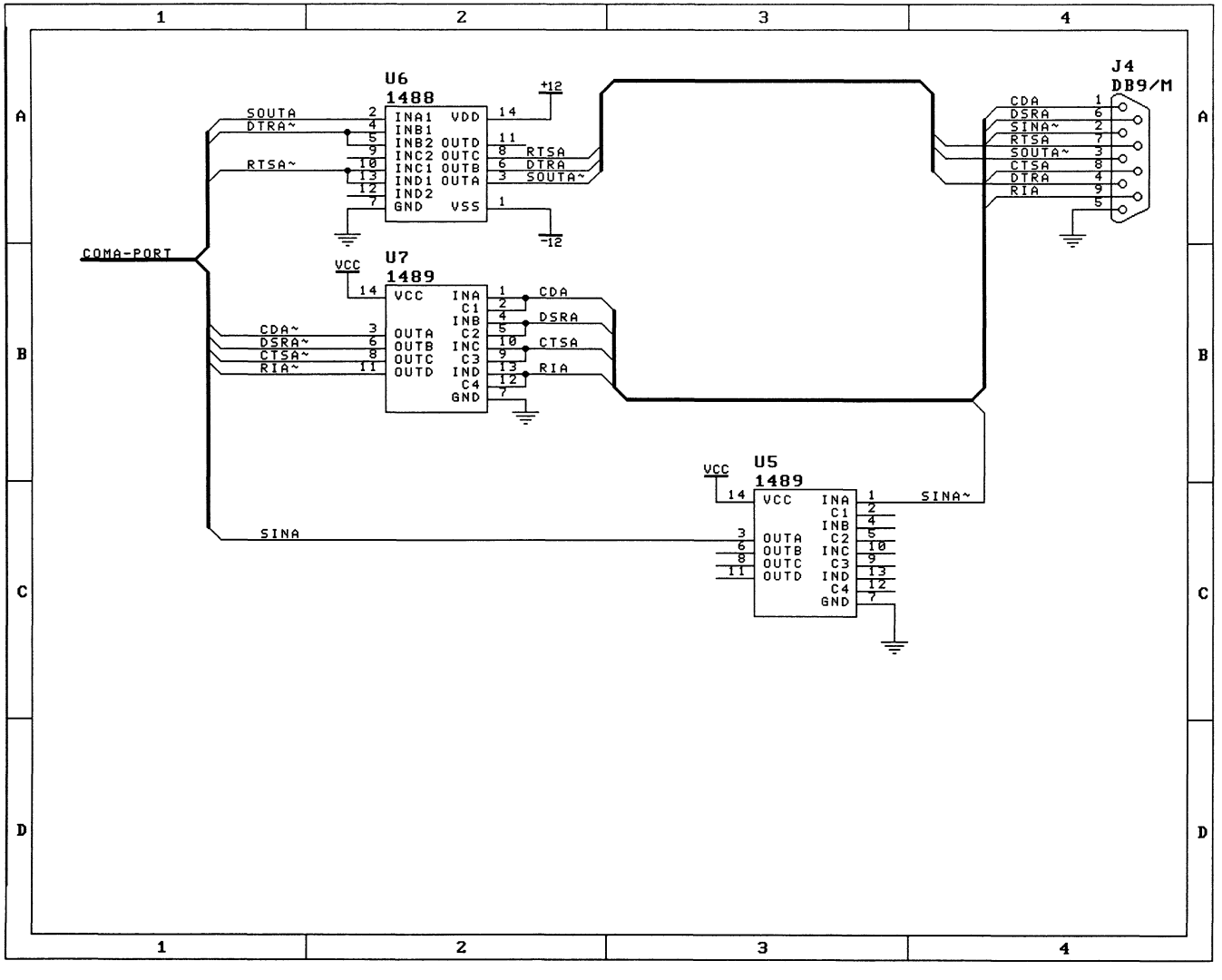

J1:A
IBM
I/O CK
D7
D6
D5
D4
D3
D2
D1
D0
I/ORDY
AEN
A19
A18
A17
A16
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
J1:B
IBM
GND
RESET
+5V
IRQ2
-5V
DRQ2
-12V
N.C.
+12V
GND
MEMW
MEMR
IOW
IOR
DACK3
DRQ3
DACK1
DRQ1
DACK0
CLK
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
DACK2
T/C
ALE
+5V
OSC
GND
U2
74LS245
DIR
U3
PAL16L8
VCC
GND
OE
U1
74LS367
DATABUS
CSB~
CSA~
RESET
ADDRESS
IOR~
IOW~
INTA
INTB

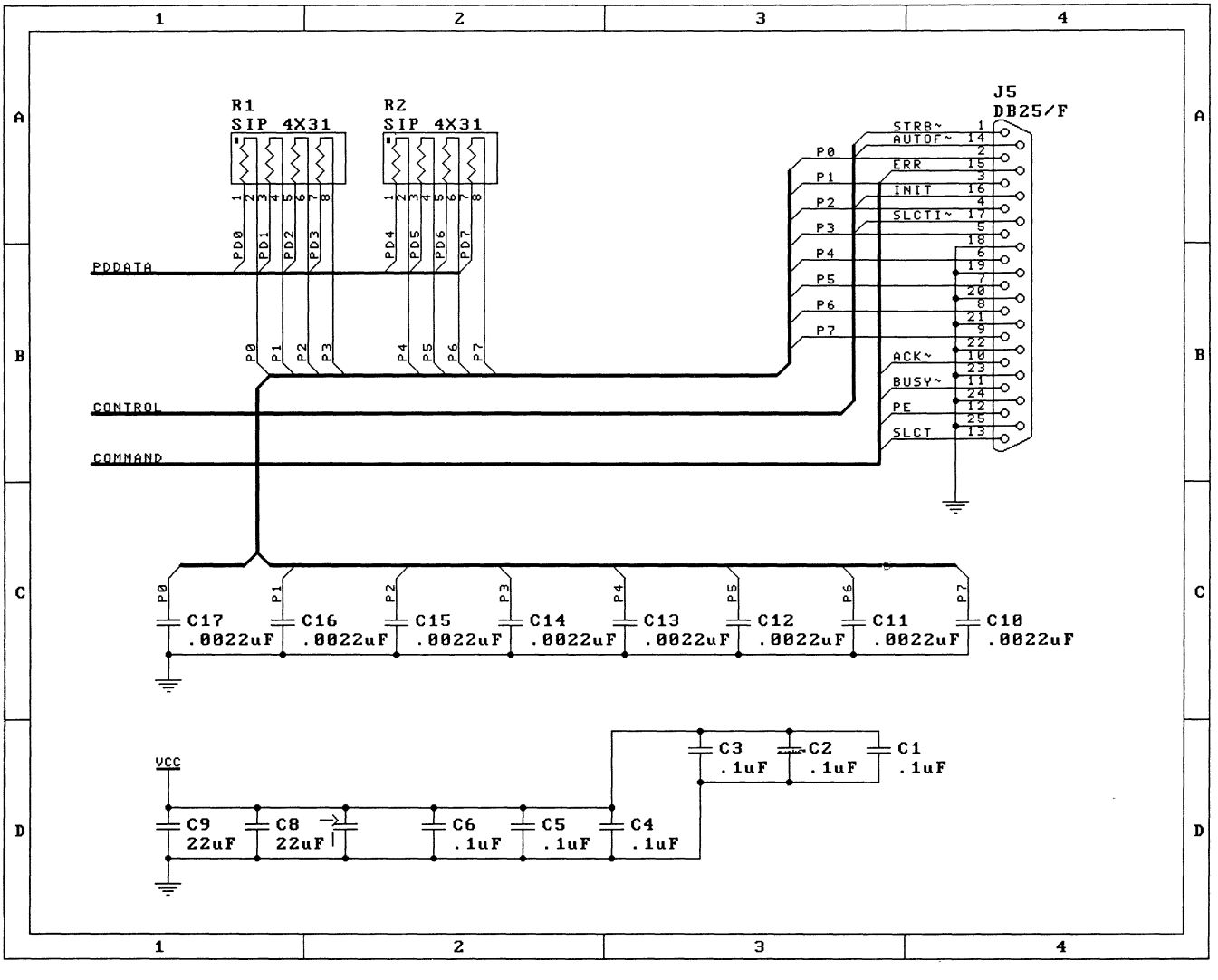

U4
LD1102
DATABUS
ADDRESS
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
BA0
BA1
BA2
IOR~
IOW~
CSA~
CSB~
RESET
XTAL1
XTAL2
GND
VCC
SOUTA
DTRA~
RTSA~
SINA
DSRA~
CTSA~
CDA~
RIA~
SOUTB
DTRB~
RTSB~
SINB
DSRB~
CTSB~
CDB~
RIB~
OPA~
OPB~
INITA
INITB
COMA-PORT
COMB-PORT
XT1
1.8432M
C2
25pF
C1
25pF
R1
10M
R2
1.8k
R3
2k
R4
2k
+5
U5:A
74LS125
U5:B
74LS125
INTA
INTB

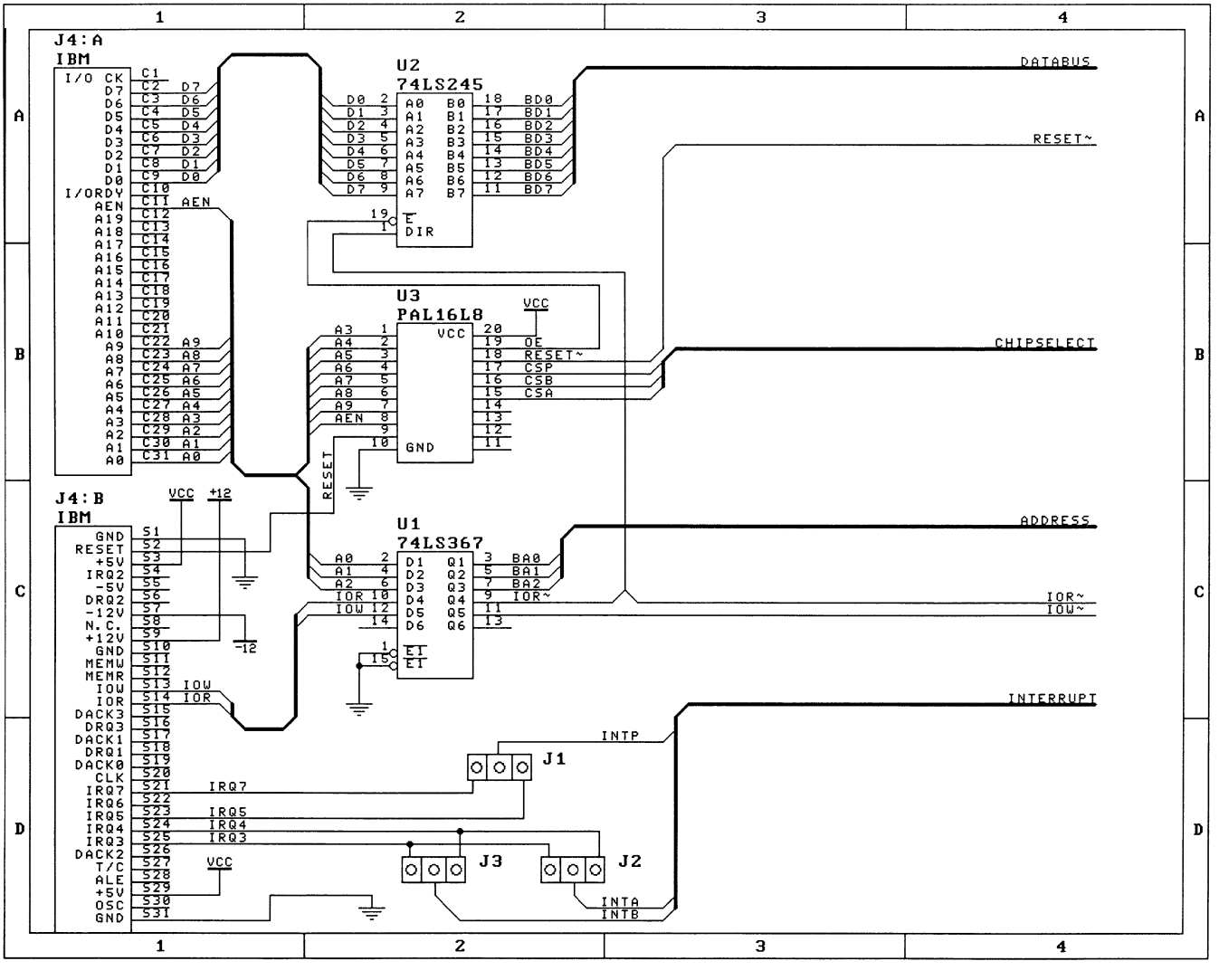

U9
1488
U8
1489
U6
1488
U7
1489
U10
1489
J2
DB9/M
J3
DB9
COMA-PORT
COMB-PORT
SOUTA
DTRA~
RTSA~
CDA~
DSRA~
CTSA~
RIA~
SINA
SOUTB
DTRB~
RTSB~
CDB~
DSRB~
CTSB~
RIB~
SINB
+12
-12
VCC
CDA
DSRA
CTSA
RIA
CDB
DSRB
CTSB
RIB
SINA~
SINB~
RTSA
DTRA
SOUTA~
RTSB
DTRB
SOUTB~

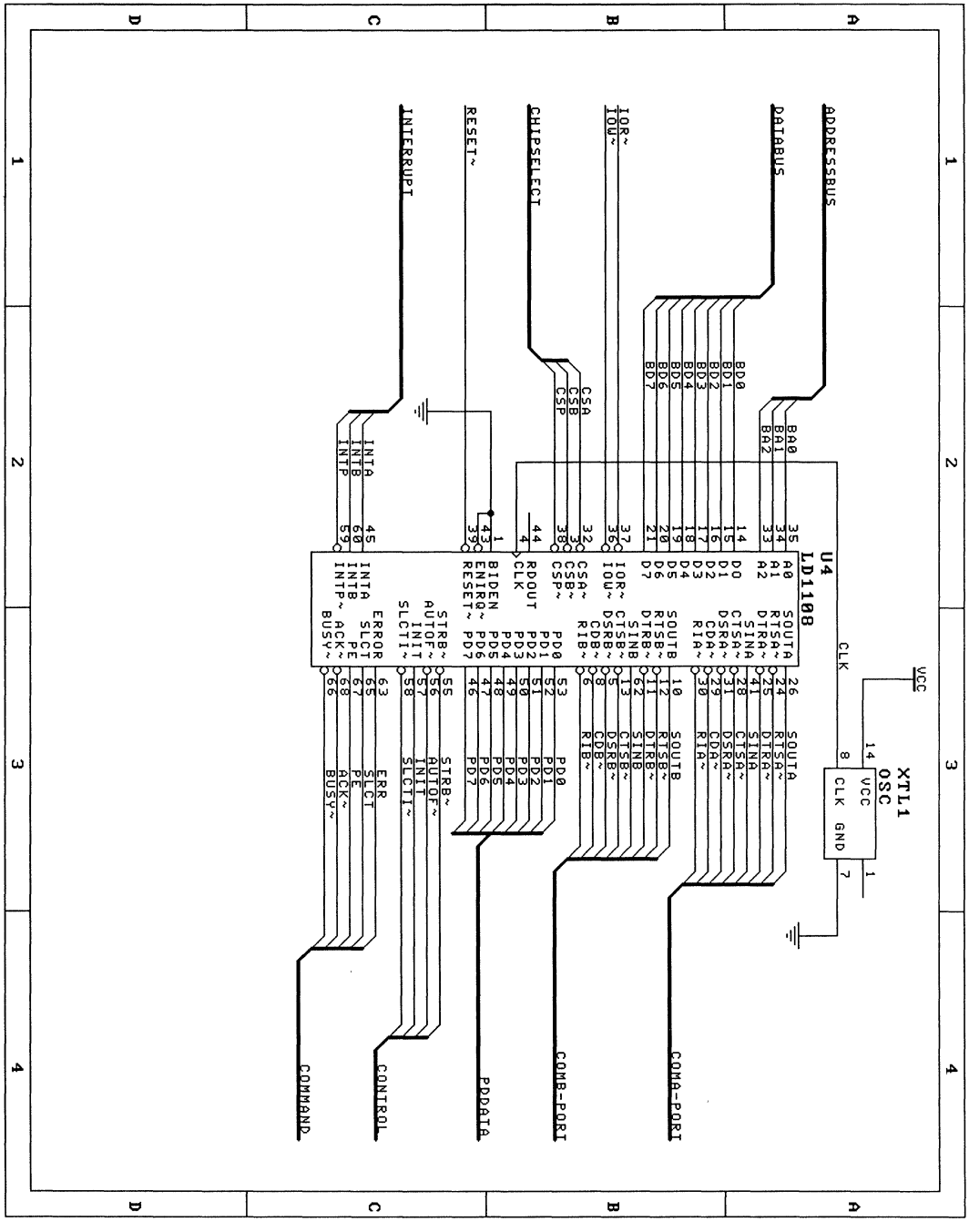

J3:A
IBM
I/O CK
D7
D6
D5
D4
D3
D2
D1
D0
I/ORDY
AEN
A19
A18
A17
A16
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
U2
74LS245
A0 B0
A1 B1
A2 B2
A3 B3
A4 B4
A5 B5
A6 B6
A7 B7
DIR
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
DATABUS
U1
PAL16L8
VCC
OE
RESET~
CSP
CSA
GND
RESET
CHIPSELECT
J3:B
IBM
GND
RESET
+5V
IRQ2
-5V
DRQ2
-12V
N.C.
+12V
GND
MEMW
MEMR
IOW
IOR
DACK3
DRQ3
DACK1
DRQ1
DACK0
CLK
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
DACK2
T/C
ALE
+5V
OSC
GND
+12
-12
U3
74LS367
D1 Q1
D2 Q2
D3 Q3
D4 Q4
D5 Q5
D6 Q6
E1
E1
BA0
BA1
BA2
ADDRESS
IOR~
IOW~
INTERRUPT
INTP
J2
J1
INTA

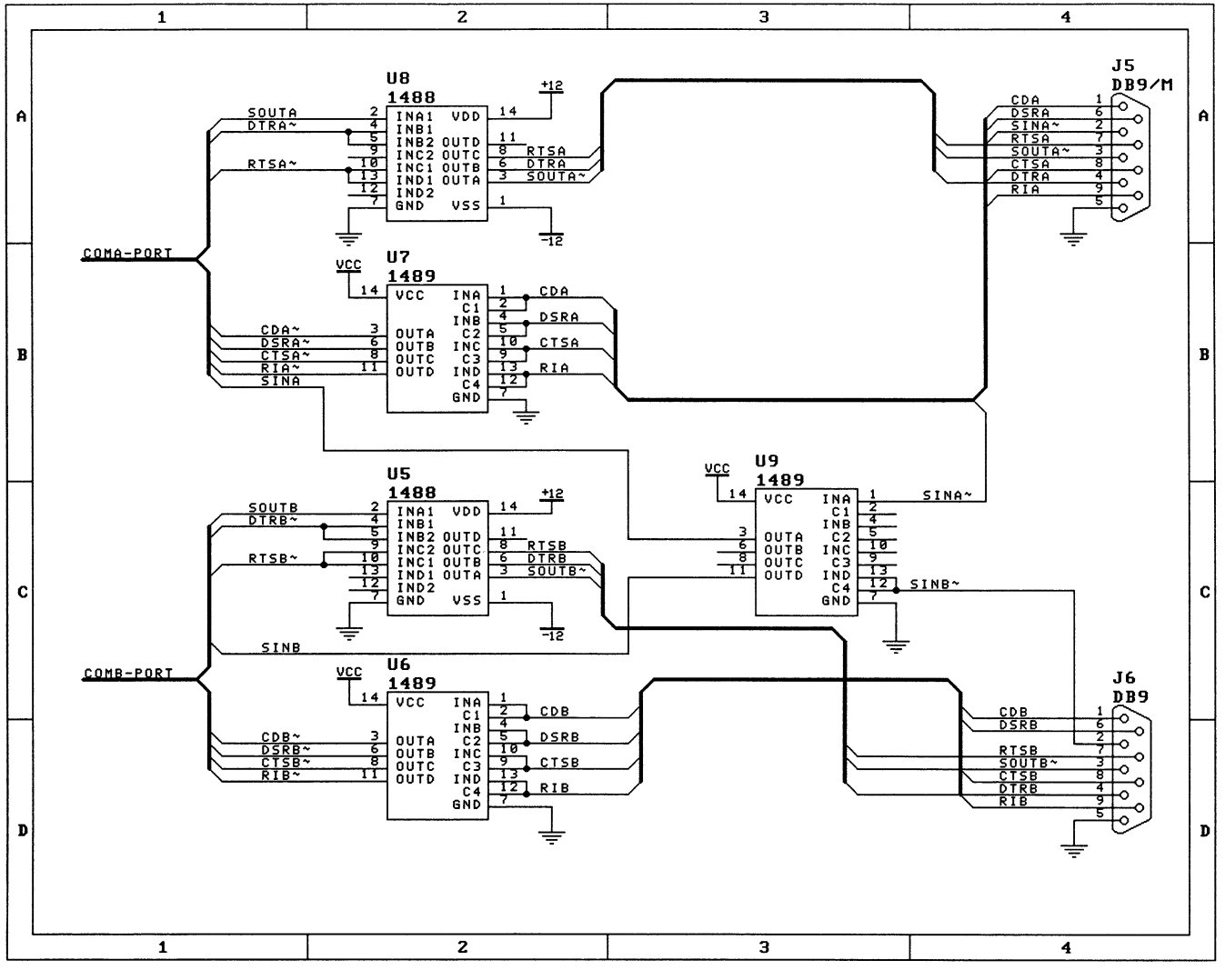

VCC
XTL1
OSC
14
VCC
1
CLK
8
CLK GND
7
U4
LD1107
ADDRESSBUS
DATABUS
BA0
BA1
BA2
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
IOR~
IOW~
CSA
CSP
CHIPSELECT
RESET~
INTERRUPT
INTA
INTP
A0
A1
A2
D0
D1
D2
D3
D4
D5
D6
D7
IOR~
IOW~
CSA~
CSP~
RDOUT
CLK
BIDEN
ENIRQ~
RESET~
INTA
INTP~
SOUTA
RTSA~
DTRA~
SINA
CTSA~
DSRA~
CDA~
RIA~
COMA-PORT
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
PDDATA
STRB~
AUTOF~
INIT
SLCTI~
CONTROL
ERROR
SLCT
PE
ACK~
BUSY~
COMMAND


1
2
3
4
A
B
C
D
U6
1488
INA1
INB1
INB2
INC2
INC1
IND1
IND2
GND
VDD
OUTD
OUTC
OUTB
OUTA
VSS
+12
-12
SOUTA
DTRA~
RTSA~
RTSA
DTRA
SOUTA~
U7
1489
VCC
INA
C1
INB
C2
INC
C3
IND
C4
GND
OUTA
OUTB
OUTC
OUTD
CDA~
DSRA~
CTSA~
RIA~
CDA
DSRA
CTSA
RIA
U5
1489
SINA~
SINA
COMA-PORT
J4
DB9/M
CDA
DSRA
SINA~
RTSA
SOUTA~
CTSA
DTRA
RIA


R1
SIP 4X31
R2
SIP 4X31
J5
DB25/F
PDDATA
CONTROL
COMMAND
STRB~
AUTOF~
ERR
INIT
SLCTI~
ACK~
BUSY~
PE
SLCT
C17 .0022uF
C16 .0022uF
C15 .0022uF
C14 .0022uF
C13 .0022uF
C12 .0022uF
C11 .0022uF
C10 .0022uF
VCC
C9 22uF
C8 22uF
C6 .1uF
C5 .1uF
C4 .1uF
C3 .1uF
C2 .1uF
C1 .1uF


J4:A
IBM
I/O CK
D7
D6
D5
D4
D3
D2
D1
D0
I/ORDY
AEN
A19
A18
A17
A16
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
U2
74LS245
A0 B0
A1 B1
A2 B2
A3 B3
A4 B4
A5 B5
A6 B6
A7 B7
DIR
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
DATABUS
U3
PAL16L8
VCC
GND
OE
RESET~
CSP
CSB
CSA
CHIPSELECT
RESET
J4:B
IBM
GND
RESET
+5V
IRQ2
-5V
DRQ2
-12V
N.C.
+12V
GND
MEMW
MEMR
IOW
IOR
DACK3
DRQ3
DACK1
DRQ1
DACK0
CLK
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
DACK2
T/C
ALE
+5V
OSC
GND
+12
-12
U1
74LS367
A0
A1
A2
IOR
IOW
D1 Q1
D2 Q2
D3 Q3
D4 Q4
D5 Q5
D6 Q6
BA0
BA1
BA2
IOR~
ADDRESS
IOR~
IOW~
INTERRUPT
INTP
J1
J2
J3
IRQ7
IRQ5
IRQ4
IRQ3
INTA
INTB


ADDRESSBUS
DATABUS
IOR~
IOW~
CHIPSELECT
RESET~
INTERRUPT
U4
LD1108
XTL1
OSC
VCC
CLK
GND
COMA-PORT
COMB-PORT
PDDATA
CONTROL
COMMAND


U8
1488
U7
1489
U5
1488
U9
1489
U6
1489
J5
DB9/M
J6
DB9
+12
-12
VCC
COMA-PORT
COMB-PORT
SOUTA
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DSRA~
CTSA~
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CTSB~
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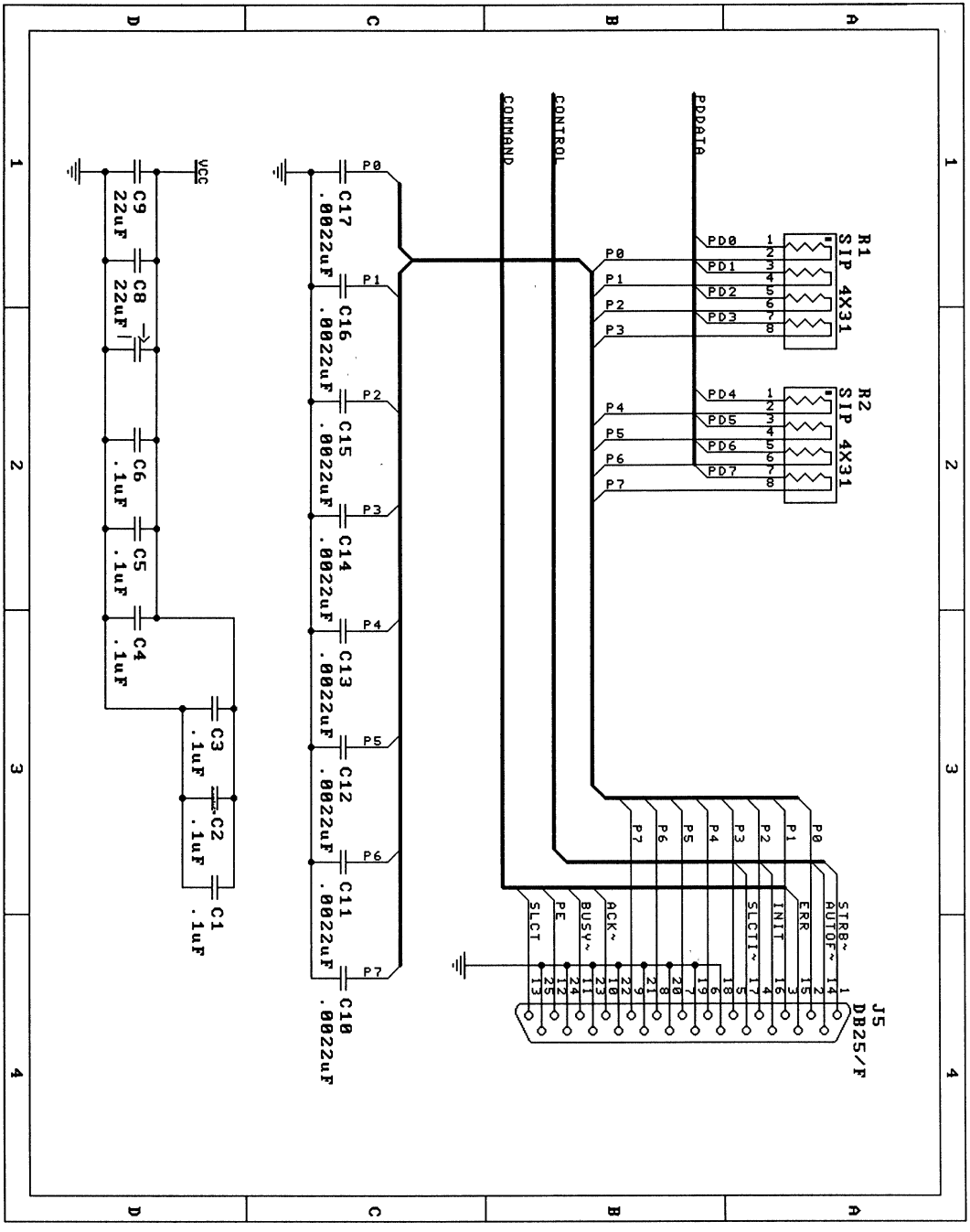
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QUALITY/RELIABILITY

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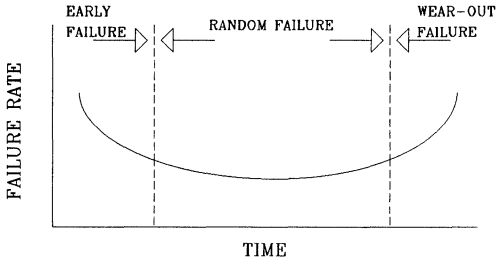
RELIABILITY THEORY

The reliability of microcircuits conforms to the following curve which plots failure rate against time. The three distinct regions of the curve can be described as infant mortality, random failure and wear out failure.



INFANT MORTALITY

These are the devices that fail in the early life of the product. Infant mortality is greatly influenced by system stress conditions other than temperature, and can vary widely from one application to another. It is this failure period that greatly influences the failure rate decline.

RANDOM FAILURE

Subsequent to infant mortality is random failure. This depicts the useful life of a device, usually expressed as failure rate in FIT's or percent per thousand hours. (500 FIT's = .05%/1000 hours)

WEAR OUT FAILURE

Such failures occur at the end of a device's life and are characterized by a rapidly increasing failure rate.

FAILURE RATE DETERMINATION

THE ARRHENIUS MODEL

The time and temperature dependence of virtualliy all long term semiconductor failure mechanisms is a well established fact. The occurrence of this failure dependency can be represented by the ARRHENIUS model. Originally developed in the 1880s to describe chemical reaction rates, the ARRHENIUS model was adapted to accelerated life testing for logical reasons. Faced with the critical need for full validation of accelerated life test data, researchers easily theorized that chemical processes were the cause of degradation of electronic parts. Since temperature was commonly used in accelerated testing, the ARRHENIUS model was applied and found to fit the data. The model was subsequently validated by years of reliability testing and found to be both a valuable design tool and useful adjunct to the sate of the art of accelerated life testing technology.
As applied to accelerated life testing of semiconductors, the ARRHENIUS model assumes that degradation of a performance parameter is linear with time, with the MTBF a function of the temperature stress. The temperature dependence is taken to be the exponential function that defines the probability of occurrence, resulting in the following formula for defining the lifetime or MTBF at a given temperature stress level when knowing the MTBF at a second temperature stress level.

$$t_1 = t_2 \exp E/K\,(1/T_1 - 1/T_2)$$

t_1 = MTBF at junction temperature T_1
t_2 = MTBF at junction temperature T_2
T = Junction temperature in °K
E = Thermal activation energy in electron volts (eV)
K = Boltzman's constant (8.617×10^{-5} eV/°K)

ACCELERATION FACTOR F

The acceleration factor F is the factore by which the failure rate can be accelerated by increased temperature. This factor can be readily derived by expressing the failure rate L as the reciprocal of MTBF, then reducing the ARRHENIUS equation to the following form:

$$L_1/L_2 = F = \exp E/K\,(1/T_2 - 1/T_1)$$

F = Acceleration factor
L_1 = Failure rate at junction temperature T_1
L_2 = Failure rate at junction temperature T_2

JUNCTION TEMPERATURE

In calculating the field reliability of a semiconductor device, it is first necessary to calculate the junction temperature both for the reliability test and for actual field operating conditions. In general, the junction temperature will depend on the ambient temperature, cooling, package type, operating cycle times, supply voltage and current. In these terms, the junction temperature T_j is given as:

$$T_j = T_A + (I_{CC} \times V_{CC})\ (A_f)(T_{JA})$$

T_j = Junction temperature
T_A = Ambient temperature
I_{CC} = Supply current
V_{CC} = Supply voltage
A_f = Air flow factore (~0.75)
T_{JA} = Package thermal resistance

ACTIVATION ENERGY

Given the temperature and failure rate for a specific reliabilty test, the remaing unknown is the activation energy E. To derive a simple formula for E, take the natural log of the failure rate. As the slope of the straight line resulting from the following formula the activation energy serves as a convenient means of characterizing the failure mechanisms. If the activation energy is known, or can be estimated, the acceleration factor can be determined, allowing field failure rate and useful life to be calculated from the accelerated life tests.

$$Ln(L_1) - Ln(L_2) = E/k\ (1/T_1 - 1/T_2)$$

FAILURE ANALYSIS

When a failure occurs in qualification tests, lot acceptance or reliability monitors, reliability engineer initiates a series of actions to analyze the cause of failure. SILICON LOGIC subcontracts a fully equipped laboratory which can perform a detailed analysis of these failed parts.
Reliability engineer conducts on-going research into the nature of fundamental failure mechanisms. These studies are carried out in conjunction with design, wafer processing and package assembly.
The purpose of this research is to:

1)understand the physics of the failure mechanisms

2)develop failure rate prediction models of each mechanism

3)identify the key physical and/or electrical parameters and thier limits

MOISTURE RESISTANCE

Moisture resistance is one of the most significant problems of plastic packaged semiconductor devices. Molding resin has a slight permeability to moisture and contains a very small amount of such elements as chlorine and sodium, which are readily ionized by water. In high humidity environments, device characteristics can easily become degraded by these ionic contaminants, including decrease of PN junction breakdown voltage, and increase of leakage current and threshold voltage shift.
In addition, the aluminum metallization patterns can become corroded by contact with water molecules and ionic substances. Since aluminum is a chemically active metal, an oxide film (AL_20_3) with a thickness of several nanometers is quickly formed when it is exposed to dry air at room temperature. Under dry conditions, oxidation does not go further, because the oxide serves as a protective film. If sufficient water molecules are present, aluminum hydroxide is amphoteric and therefore soluble in both acid and alkalai.
In order to minimize contamination, SILICON LOGIC, INC. subcontracts the wafer and assembly process to companies which provide the following services.

* Maintaining ultra clean processing areas
* Employing strict controls on process parameters
* Using molding resins with minimum impurities
* Using halide free assembly process

PASSIVATION PIN-HOLES/CRACKING

Pin holes and cracking in the passivation will allow the moisture to penetrate into the active circuit and cause failures due to leakage and/or corrosion. Pin holes occur due to processing defects and cracking because of the differences in coefficients of thermal expansion among the materials in the assembly. To improve the passivation, silicon nitride is used to seal the last layer.

RELIABILITY TESTING OF IC'S

ENVIRONMENTAL TESTS

Several tests that determine the long term stability and reliability of products. The product is exposed to various conditions and extremes of temperature, humidity, pressure or mechanical stress that stimulates potential faults to appear, and accelerates detection of device failures.

OPERATING LIFE TEST

This test detects electrical failures due to oxide contamination, pin holes or photo-masking defects. It is performed with bias and in a high temperature, typically 125 °C for plastic package devices. The operating life test is normally run up to 1000 hours or more and then extrapolated to maximum use temperature, 70 °C

to calculate failure rates.

BIAS
The electrical connection to the device pins that allows specified signals, loading, and power supply voltage to be applied.

BIASED HUMIDITY TEST
(85 °C / 85% Relative Humidity)
This test is performed to detect failures in plastic devices due to extended exposure to high temperature and humidity, and exhibited as surface contamination or metal interconnect corrosion on the IC's. Tests are carried out for a minimum of 1000 hours and up to 2000 hours in most cases. The bias conditions normally are such that minimum power dissipation occurs and voltages normally approach the maximum for a given device.

PRESSURE COOKER TEST
This test is performed without bias in a pressure cooker at 15 psi and 120 °C. This test is run for 100 hours as a product reliability monitor and 500 hours for qualification test. Experience has shown the PCT test to be the most useful test in determining bond pad corrosion caused by process residues, passivation integrity and lead to package adhesion integrity.

STRESS
An extreme environmental, electrical or physical condition applied to a device to evaluate the device performance or to accelerate reaction rates.

THERMAL SHOCK
This test is normally run per Mil Std 883C, on most package types. It detects most packaging problems related to wire bonds, die attach seal integrity and lead integrity.

BURN-IN
A thermal and electrical stress test designed to eliminate early failures. The early device failures are detected and removed, thus enhancing reliability.

FAILURE IN TIME (FIT)
A standard reliability unit that measures the device failure rate as a function of device hours. One FIT is equal to one device failure per billion device hours of operation (1 FIT = 0.0001% failues / 1000 hours).

SAMPLING
Inspection method to determine lot quality by careful examination of a small number of devices from the lot. A sampling plan is used to set sample size, based on the designed quality level.

SCREENING
The process of subjecting all products to nondestructive stressess to accelerate and identify eary failures.

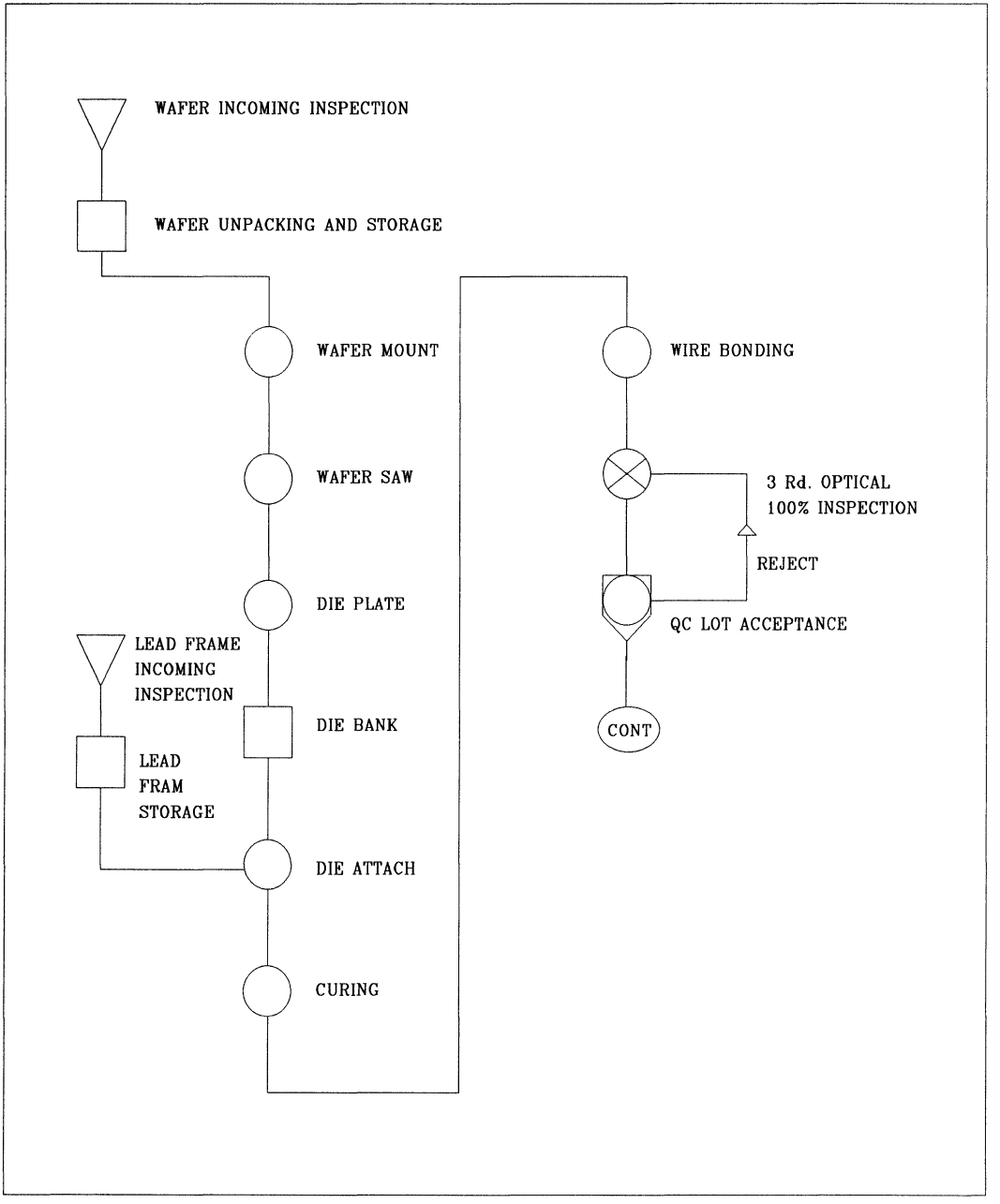
QUALITY ASSURANCE (QA)
The activity of providing, to all concerned, the evidence needed to establish confidence and assurance that all activities which affect product quality are being performed adequately.

COMMON INFANT MORTALITY FAILURE MECHANISMS

Failure Mechanism	Activation Energy	Stress Factors	Prevention
Oxide Rupture	0.35 eV	high temperature, V	ultraclean processing
Open Wire Bond		ultrasonic exposure high temperature	assembly process control "
Lifted Die Bond		high temperature centrifuge	assembly process control "
Fused Die Metallization Short		system power	adequate spacing between adjacent strips
Opens		inductive loading	adequate stripe width, thickness
Metal Corrosion	0.80 eV	high temperature high humidity	de-ionized compound clean assembly process phosphorous control improved passivation halide controls

WEAR OUT FAILURE MECHANISMAS

Failure Mechanism	Activation Energy	Stress Factors	Prevention
Electromigration	0.55 eV	high temperature high current density	optimal design rules
AuAl Intermetallic Growth	1.00 eV	high temperature storage temperature cycle	process control
Ionic Contamination	1.00 eV	high temperature	ultra clean processing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WAFER UNPACKING AND STORAGE
WAFER MOUNT
WAFER SAW
DIE PLATE
LEAD FRAME INCOMING INSPECTION
DIE BANK
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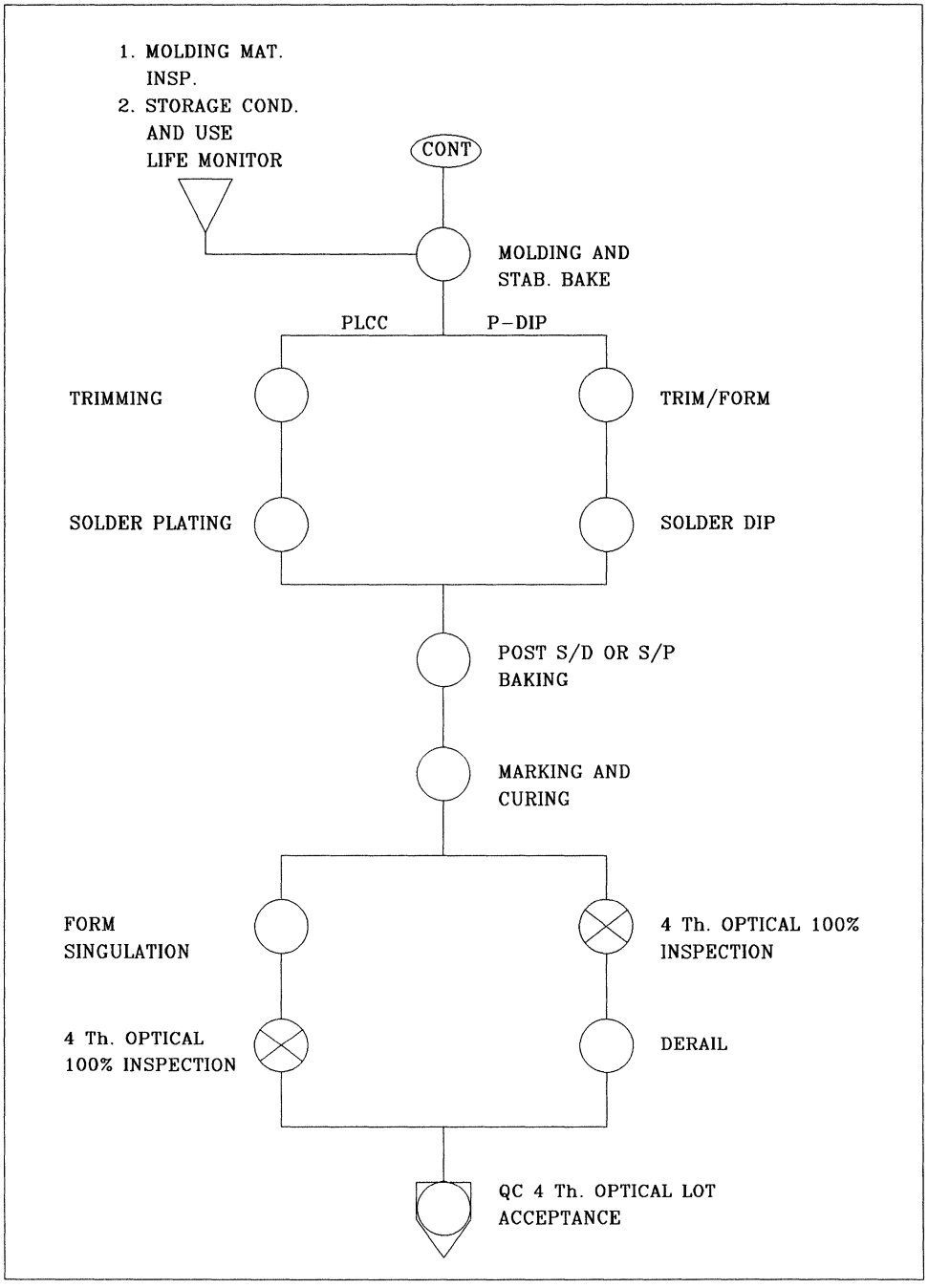
DIE ATTACH
CURING
WIRE BONDING
3 Rd. OPTICAL 100% INSPECTION
REJECT
QC LOT ACCEPTANCE
CONT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P-DIP
TRIMMING
TRIM/FORM
SOLDER PLATING
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POST S/D OR S/P BAKING
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FORM SINGULATION
4 Th. OPTICAL 100% INSPECTION
4 Th. OPTICAL 100% INSPECTION
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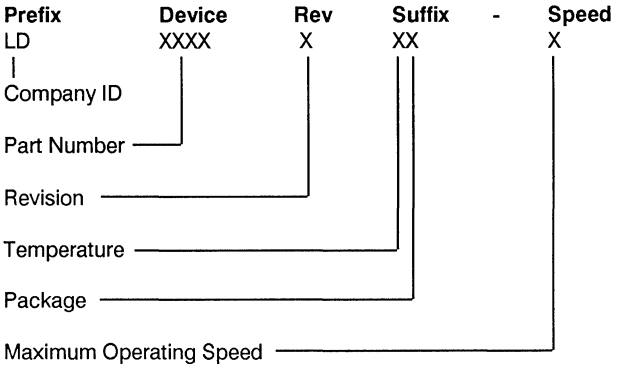
QC 4 Th. OPTICAL LOT ACCEPTANCE

ORDERING INFORMATION

9

ORDERING INFORMATION AND PART NUMBERING GUIDE



Package

P	Plastic
C	Ceramic
D	Cerdip
L	Leadless Chip Carrier (LCC)
J	Plastic Leaded Chip Carrier (PLCC)
F	Flat Pack
Q	Quad Pack
G	Pin Grid

TEMPERATURE RANGE

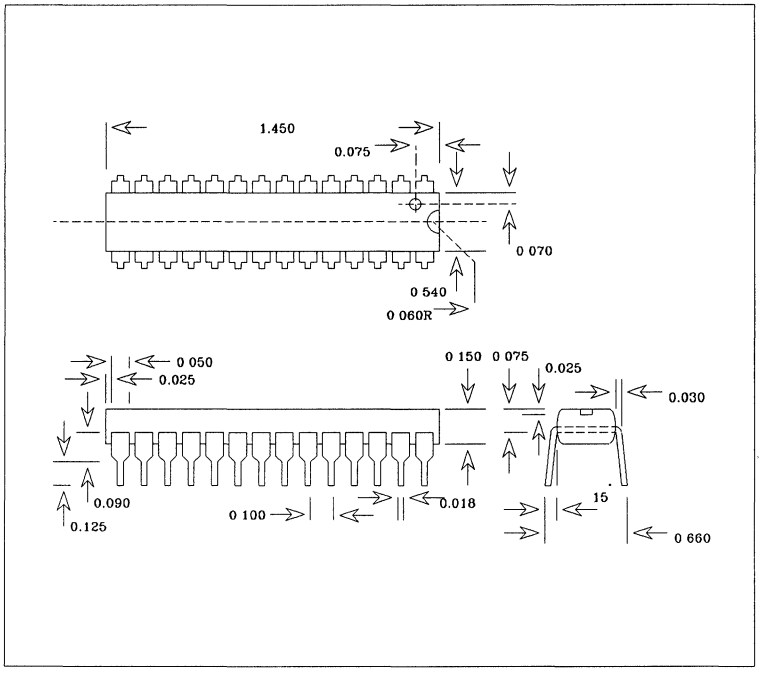
C	Commercial	0° C TO +70° C
I	Industrial	-40° C TO +85° C
M	Military	-55° C TO +125° C

9

PACKAGING INFORMATION

10

28 DIP



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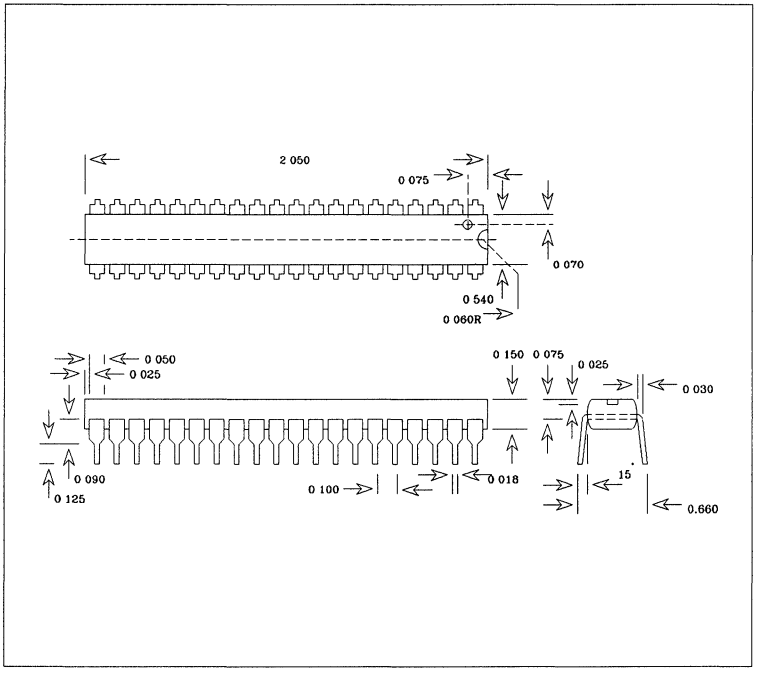
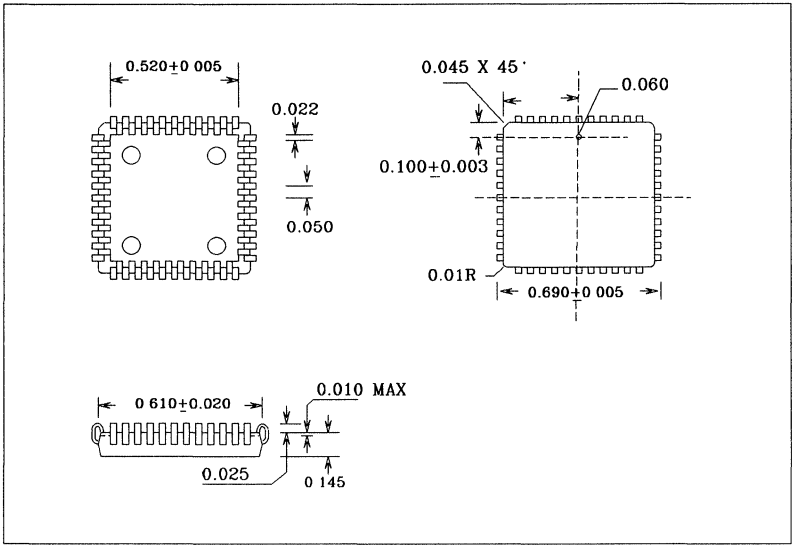


10

44 PLCC



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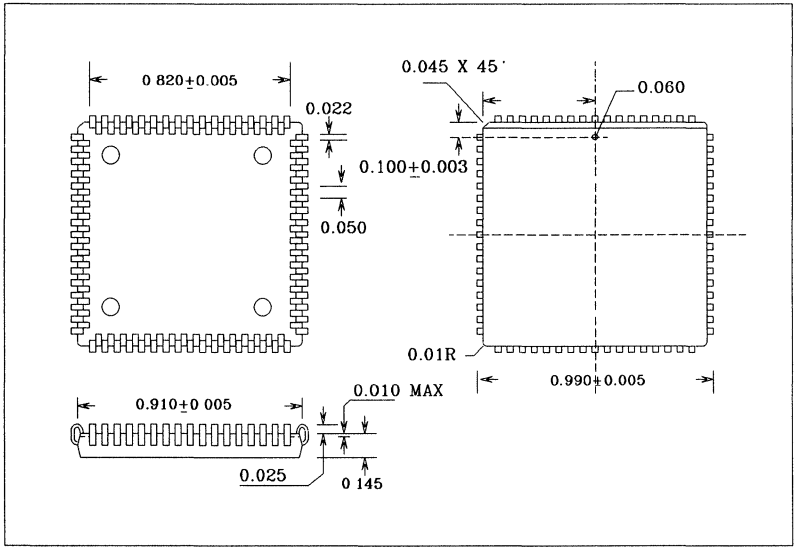

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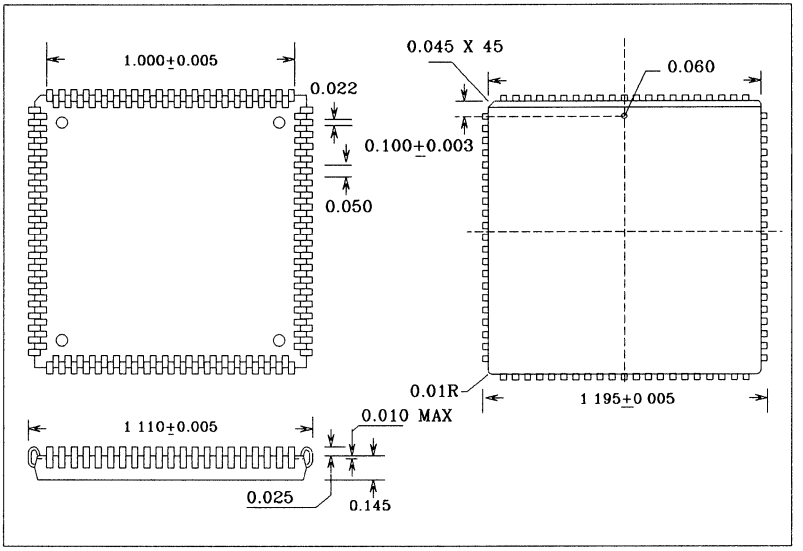
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