SIGNETICS
MOS
SILICON GATE
2500 SERIES
METAL GATE
2000/2400 SERIES
DATA BOOK

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SIGNETICS CORPORATION

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WHY SILICON GATE TECHNOLOGY?

INTRODUCTION

There are many MOS processes available today, ranging from high threshold, 1-1-1 orientation silicon, P-MOSTs to the less common dielectrically isolated,complementary MOS, ion implanted, silicon nitride, and silicon gate monolithic circuit. The problems which arise for MOS manufacturers and users can be summarized many times as one question: Which technology?

In this section, a brief comparison of the available MOS technologies is made. This is followed by a description of the silicon gate process flow sequence and a comparison of its advantages and disadvantages.

MOS TECHNOLOGIES

The numbers of MOS technologies available are numerous and each has its own advantages and disadvantages. Figure 1 shows a process ranking for some of the major technologies now available. The processes are weighted on five different factors: speed, chip area, power dissipation, bipolar compatibility and cost. The Silicon Gate Process which ranks highest forms the basis for the 2500 Series.

PROCESS RANKING						
MOS	SPEED	AREA	POWER	COMPATIBILITY	COST	RANKING
P Channel						
1-1-1 Crystal, Metal Gate	6	2	3	3	1	6
1-0-0 Crystal, Metal Gate	7	2	2	2	1	5
Nitride	5	2	2	2	2	4
Silicon Gate, (111) Crystal	3	1	2	1	2	1
Ion Impl. (Metal Gate)						
Low Threshold Approach	5	2	2	1	2	4
Self Aligned Gate	4	3	3	3	2	6
N Channel	2	2	2	1	3	2
Complementary	1	4	1	1	4	3

FIGURE 1.

SILICON GATE PROCESS

FABRICATION SEQUENCE

Basic process flow is illustrated in Figure 2. Using this chart as a guide, the process can be described as follows.

STEP A

The wafers are thoroughly inspected, cleaned, oxidized and masked to delineate the area where the drain, source and channel will eventually be formed. The gate dielectric is then grown. Both the initial oxide and the gate dielectric can be grown in any manner, to any desired thickness, without affecting junction characteristics. The initial oxide thickness is normally chosen to minimize poly-to-substrate capacitance, maximize poly-to-substrate parasitic field turn-on voltage and thin enough to minimize the step over which metal lines may eventually have to travel.

STEP B

The poly-crystalline silicon is deposited, a masking oxide is formed and the sandwich is then masked and etched to delineate the gate structure and the drain-source beds. The quality, cleanliness and thickness uniformity of the deposited poly is important. Also delineating the poly-crystalline lines is a critical step, since some of these lines determine the channel length of the completed MOS transistors.

SILICON GATE TECHNOLOGY

STEP C

Boron is deposited to dope the poly-crystalline silicon and to form the P^+ beds for source and drain. The doping of the poly lines and P^+ beds is straightforward and virtually any clean source of boron can be used. Because the pre-deposited poly-silicon gate is used to mask the boron diffusion, the gate,source and drain are automatically self aligned.

STEP D

A clean layer of oxide is deposited over the entire wafer to passivate the P^+ beds and provide isolation between poly-silicon and metal lines. Deposition of the passivating oxide requires strict control over the cleanliness of the deposition system to minimize oxide defects and contamination.

STEP E

Contacts are opened and metallization is deposited, delineated and sintered. The metallization is fairly standard. As with the metal gate processes which may have high oxide steps, care must be taken with the silicon gate process to minimize the height of the steps over which metal must travel in order to minimize metal microcracking problems.

A multi-layered protective glass is deposited over the finished structure and holes are opened to the bonding pads to give the final cross-section shown in Figure 3. Glass passivation is mandatory, even with the silicon gate process, to protect the aluminum metalization from mechanical abrasion and particulate contamination.

SILICON GATE PROCESS FLOW

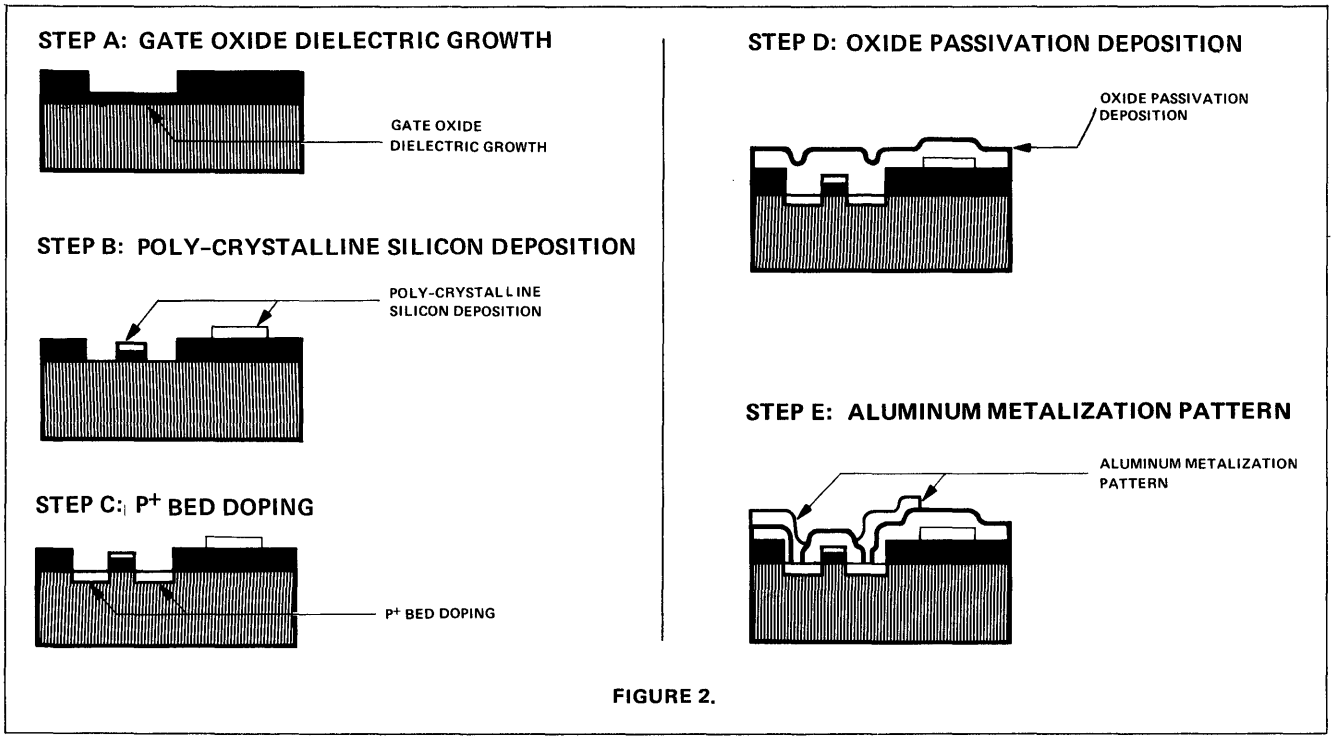


FIGURE 2.

FINAL DEVICE CROSS – SECTION

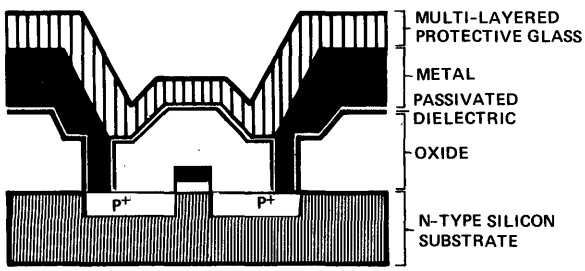


FIGURE 3.

ADVANTAGES AND DISADVANTAGES OF SILICON GATE

The silicon gate process has a number of advantages which make it attractive for the production of complex, high density circuits. Before expanding on these advantages, we will first explore two of the more prominent disadvantages of the process:

Ratio Versus Ratioless

Because of the self-aligned gate feature, the parasitic drain-to-source capacitance is small. In designing dynamic shift registers, it is advantageous to design "ratioless" devices where parasitic capacitance is used to momentarily store charge. Using silicon gate, a ratioless type design is not feasible, so the more area consuming ratio type must be used. However, the silicon gate ratio design is competitive in size with the metal gate ratioless version, since area is saved by the smaller gate area (no need for alignment tolerance allowance), plus the use of the poly-silicon as a interconnecting layer.

Additional Depositions

Silicon gate processing requires more deposition steps than is required by standard metal gate processes. However, these processes can be easily controlled using modern, automated deposition equipment and built-in process control monitors.

The potential disadvantages of the silicon gate process are outweighted by the following advantages.

Low Threshold Voltage

Doped poly-silicon, used in place of the usual aluminum gate electrode, yields threshold voltages typically around -2.0 volts. This low threshold voltage is obtained using 1-1-1 orientation silicon, so the corresponding parasitic field turn-on voltage is still very high.

High Gain

The gain of the silicon gate device is high since 1-1-1 orientation is used as the starting material. Gain is typically higher than low threshold voltage devices fabricated on 1-0-0 silicon because of higher carrier mobility.

Low Power

The silicon gate device dissipates less power:

(1) Because of its low threshold it operates with lower power supply voltages.

(2) Its self-aligned gate essentially eliminates overlap of the gate over the drain, so the capacitive load on the clock drive is less.

High Speed

High speeds are obtained because of low threshold voltages, high gain and low gate capacitance.

Minimum Area

The poly-crystalline silicon layer provides yet another "half-layer" of interconnection. We call it a "half-layer" since the crossing of poly-silicon over P^+ beds is not allowed. Shallow junctions allow close P^+ bed spacings and the self-aligned gate feature means no mask alignment tolerances are needed to register the gate to the P^+ beds. In addition, direct contact of poly-to-substrate allows further area reduction.

To illustrate the size advantages, consider Figure 4. The 2005 and 2510 are both dual 100-bit static shift registers. However, the silicon gate 2510 is 15 percent smaller than its metal gate equivalent. Not only is it smaller but it has additional functions such as recirculate logic, tri-state outputs, TTL compatibility and an on-chip clock generator. The silicon gate 2511 Dual 200-Bit Static Shift Register, offers twice the number of bits as the metal gate 2005 plus four additional functions in only 36 percent more area.

SIZE COMPARISON OF DICE

PART NUMBER	DESCRIPTION	DIE SIZE	AREA
2005	Dual 100 Bit S.S.R. (Metal Gate)	91 x 90	8,190mil^2
2510	Dual 100 Bit S.S.R. (Silicon Gate)	85 x 82	6,970mil^2
2511	Dual 200 Bit S.S.R. (Silicon Gate)	136 x 82	11,152mil^2

FIGURE 4.

High Yield

The process of forming the gate oxide at the first stage of wafer fabrication and coating with a protective layer of silicon inherently gives higher yields. In addition, the ability to compact a given circuit function into a smaller area gives a lower probability that a processing defect will occur on a die. This is especially true since the decrease in area does not come at the expense of masking tolerances. The higher yields result in lower costs.

Process Flexibility

The silicon process gate is compatible with other MOS technologies. Ion implantation can be used to adjust thresholds and/or minimize gate-to-drain capacitance. Gate dielectrics can easily be changed without affecting junction characteristics, and C-MOST and N-MOST can easily be adapted to silicon gate processing.

Low Cost Packaging

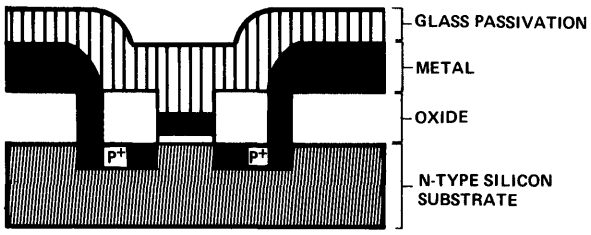
Because the gate dielectric is protected by poly-silicon and the overlying layers of oxides, it is possible to reliably package silicon gate devices in silicone packages. Cross-sections of metal gate and silicon gate devices are shown in Figure 5. The metal gate devices are protected by two layers: aluminum metallization and glass passivation. On the other hand, the silicon gate device is protected by four layers: (1) thick poly-

LOW COST PACKAGING (Cont'd)

crystalline silicon (impervious to most harmful contaminants). (2) thick clean oxide, (3) a passivated dielectric which also serves as a sodium barrier and, (4) a multi-layered protective glass.

The silicon gate process is a technology which gives all of the advantages needed to fabricate the next generation of circuits: high packing density, high speed, low power and low cost. Because of these characteristics, silicon gate MOS technology has become an industry standard for state-of-the-art MOS LSI designs.

METAL GATE PROCESS



SIGNETICS SILICON GATE PROCESS

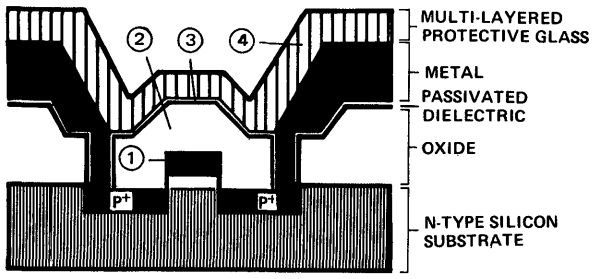


FIGURE 5.

DESIGNING WITH SILICON GATE

INTRODUCTION

Large scale, bipolar compatible MOS integrated circuits are now available to the systems designer because of the unique benefits of Signetics' Silicon Gate Technology. Using complex MOS functions to form major systems blocks, joined and controlled by today's wide variety of low cost TTL and DTL MSI and SSI functions, economical state-of-the-art systems are being produced with ease and efficiency.

THE SILICON GATE MOS BIPOLAR COMBINATION

Silicon Gate MOS - Bipolar designs offer the best of both worlds. MOS designs are most efficient when providing large, medium-speed arrays of identical cells, such as required for long serial shift registers, large Random Access Memories (RAMs) and large Read-Only-Memories (ROMs).

Bipolar designs are most efficient when providing high-speed connective logic functions (gates), small parallel registers, and small specialized logic combinations such as adders, comparators, counters, decoders, and power drivers.

MOS-BIPOLAR COMPATIBILITY

Today's systems are designed to utilize the benefits of both MOS and bipolar technology for maximum performance at minimum cost. Signetics recognizes the benefits of direct MOS-Bipolar interfacing and has created the Silicon Gate 2500 Series MOS with the express purpose of providing MOS density and bipolar compatibility.

INPUT INTERFACE

All 2500 series devices are manufactured with the P-channel enhancement mode silicon gate process. A typical data input structure is shown in Figure 1.

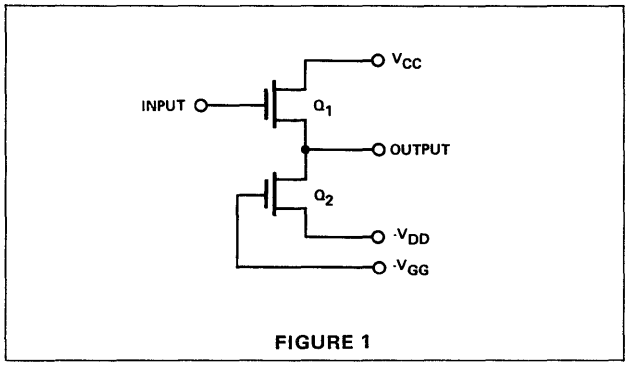


FIGURE 1

The input transistor exhibits the transfer curve shown in Figure 2. The device is fully OFF at -1.8 volts or less (V_{GS}) and fully ON at -3.5 volts or more. To simplify the interfacing of TTL and 2500 Series devices, the source voltage for the input transistor is specified at +5.0 volts. In practice, this point is tied to the +5.0 volt TTL V_{CC} supply. The required MOS input levels are then specified as positive levels referenced to the TTL ground.

Series 2500 Input Thresholds

"0" Input Voltage = V_{IL} = +1.05 maximum@ V_{CC} = 5V

"1" Input Voltage = V_{IH} = +3.2V minimum @ V_{CC} = 5V

The input levels are specified assuming V_{CC} is exactly +5.0V. The allowable V_{CC} tolerance is ±5%, however any variation in actual V_{CC} will be tracked directly by the input threshold point.

Example (a): +5% V_{CC}
@ V_{CC} = +5.25V
V_{IL} = 1.3V max.
V_{IH} = +3.45V minimum

Example (b): -5% V_{CC}
@V_{CC} = +4.75V
V_{IL} = 0.8V max.
V_{IH} = +2.95V minimum

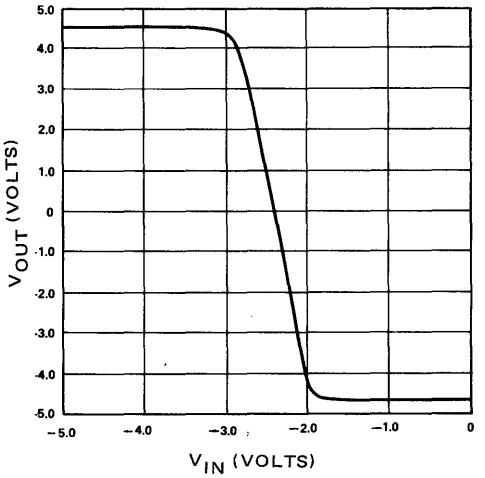


FIGURE 2

in actual practice, tying the TTL V_{CC} to the MOS V_{CC} will ensure maximum noise margin since the TTL output levels and MOS input thresholds will track.

54/7400 TTL

Figure 3(a) and (b) show a typical 7400 Series gate circuit and transfer characteristic.

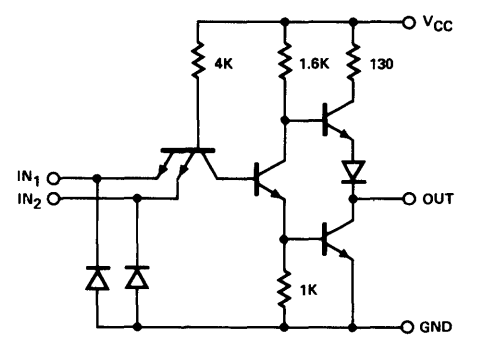


FIGURE 3(a)

54/7400 TTL

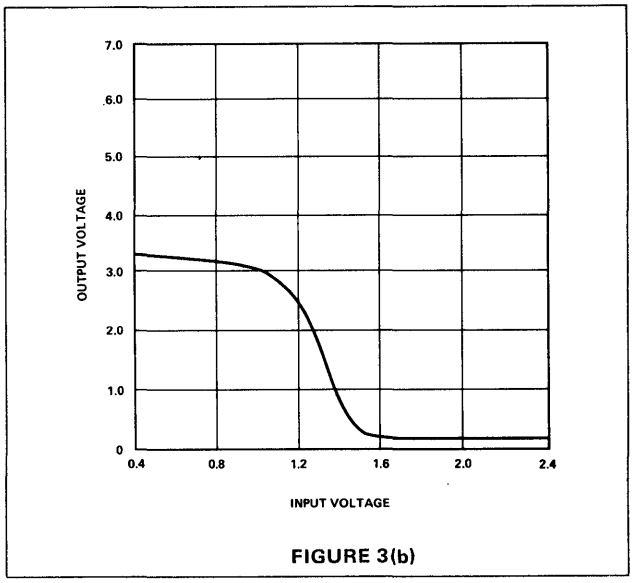


FIGURE 3(b)

The output structure shown in Figure3(a) is normally specified as follows:

@ V_{CC} = +5V ±5%

V_{OL} = +0.4V maximum @ 16 mA sink

V_{OH} = +2.4V minimum @ 400 μA source

MOS devices require only negligible D.C. input current (approximately 1μA), so the current available from the TTL output is of no interest for steady state conditions. V_{OL} is perfectly compatible with the MOS offering at least 400mV of noise margin in the 0 state. V_{OH} however, is not sufficient to guarantee a 1 level to the MOS input since the TTL V_{OH} allows a V_{CC} - V_{OH} separation of as much as 2.85V (V_{CC} = 5.25V, V_{OH} = +2.4V; 5.25V - 2.4V = 2.85V). Assuming a common V_{CC}, this results in a virtual V_{OH} of 2.15V, far too low for MOS. In practice, the TTL V_{OH} will track V_{CC}, rather than the opposite case just noted. Also V_{OH} will be higher than +2.4 at 1μA I_{OH}. However, the TTL circuit is tested and guaranteed as in the example.

The 7400 TTL output structure will typically provide a V_{OH} approximately 1.5V (two V_{be} drops) below V_{CC}. When the MOS and TTL V_{CC} are tied, a 300mV noise margin (1.8V - 1.5V = 0.3V) is obtained. If V_{CC} is not tied common, the worst case typical noise margin is a negative 200mV. In other words, a satisfactory 1 input level cannot be assured, even under typical conditions.

TO ASSURE A SATISFACTORY 1 OUTPUT LEVEL FROM SERIES 7400 IN DRIVING SERIES 2500 MOS, AN EXTERNAL PULL-UP RESISTOR SHOULD BE CONNECTED FROM THE OUTPUT TO V_{CC} AS SHOWN IN FIGURE 4.

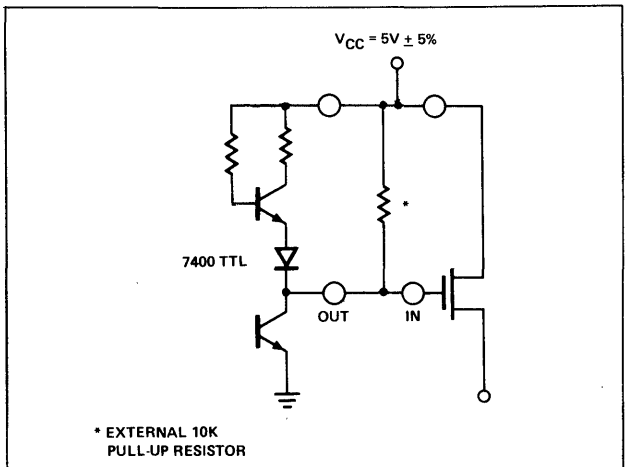


FIGURE 4

8000 TTL

Figure 5 illustrates a typical 8800 series output structure.

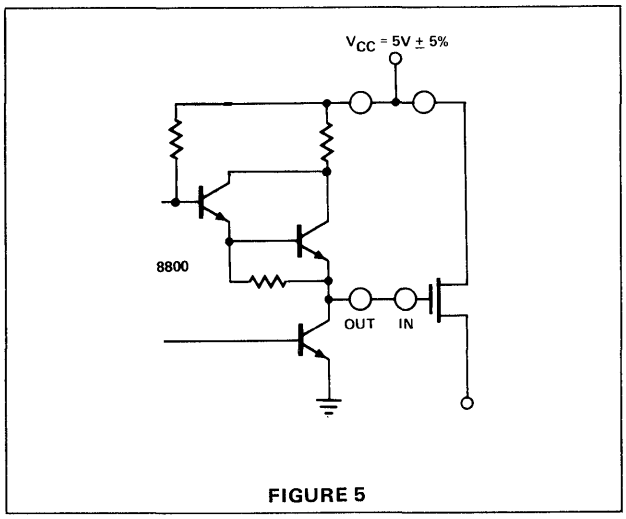


FIGURE 5

The 8800 series circuit typically offers an unloaded output voltage separated from V_{CC} by one V_{be}. Therefore the output level driving MOS will always be approximately 0.75V — higher than the preceeding example for 7400 series circuits — resulting in at least 550mV 1 level noise margin under any conditions. Noise margin at 0 level is 400 mV, the same as in the case of 7400 TTL.

Signetics guarantees 8000 Series TTL (See figure 6) V_{OH} at 3.6V @ 10μA. Under worst case conditions, this results in a minimum guaranteed 0 level noise margin of 400mV for tied V_{CC}. If the MOS and TTL V_{CC} are not tied (may vary independently), worst case guaranteed noise margin is -150mV. This configuration requires a pull-up resistor.

WHEN V_{CC}'S ARE TIED COMMON, SERIES 8000 TTL IN FIGURE 6 WILL INTERFACE DIRECTLY WITH SERIES 2500 MOS, WITHOUT THE NEED FOR AN EXTERNAL PULL-UP RESISTOR.

GATES		FLIP-FLOPS	
8808	Single 8-Input NAND Gate		
8815	Dual 4-Input NOR Gate		
8816	Dual 4-Input NAND Gate	8821	Dual Master-Slave J-K Binary
8840	Dual Expandable AND-OR-INVERT Gate	8822	Dual Master-Slave J-K Binary
8848	Expandable AND-OR-INVERT Gate	8824	Dual Master-Slave J-K Binary
8870	Triple 3-Input NAND Gate	8825	DC Clocked J-K Binary
8875	Triple 3-Input NOR Gate	8826	Dual J-K Binary
8880	Quad 2-Input NAND Gate	8827	Dual J-K Binary
8885	Quad 2-Input NOR Gate	8829	High Speed J-K Binary
	*See Note Below		

FIGURE 6

*For devices not listed, add an external pull-up resistor as in the 7400 example (Fig. 4).

DTL/UTILOGIC ®

Logic forms utilizing an internal passive pull-up resistor (such as DTL) will interface directly with 2500 Series MOS. Utilogic is guaranteed to provide output levels equivalent to those noted for Series 800 circuits.

WHEN V_{CC}'S ARE COMMON, SERIES 2500 MOS MAY BE DIRECTLY DRIVEN BY SERIES 600 DTL AND SERIES 300 UTILOGIC CIRCUITS WITHOUT THE NEED FOR AN EXTERNAL PULL-UP RESISTOR.

2500 SERIES MOS-TTL INPUT CONSIDERATIONS (TTL Level data and clock inputs)

DRIVING DEVICE	EXTERNAL PULL-UP RESISTOR(6,8)	WORST CASE GUAR. 1 LEVEL NOISE MARGIN	WORST CASE GUAR. 0 LEVEL NOISE MARGIN
Common V_{CC}			
8000(1) Series TTL	not req.	400	400
8000(2) Series TTL	10K	1300	400
7400 Series TTL	10K	1300	400
600 Series DTL (3)	not req.	400	400
600 Series DTL (4)	not req.	400	400
300 Series Utilogic (3)	not req	1300	400
300 Series Utilogic (4)	not req.	400	400
Independent V_{CC}			
All TTL	10K	800	400
600 Series DTL (3)	not req.	550	150 (5)
600 Series DTL (4)	not req.	550	150 (5)
300 Series Utilogic	10K (7)	550	150 (5)

FIGURE 7

NOTES:
(1) From List in Table I
(2) Not listed in Table I
(3) Passive Pull-up (resistor), ±10% power supply
(4) Active Pull-up, ±10% power supply
(5) Use ±5% DTL or Utilogic power supply to maintain 400 mV noise margin
(6) From driving output to V_{CC}
(7) Certain Series 300 devices utilize a passive pull-up and require no external pull-up.
(8) The 2527, 2528 and 2529 incorporate internal pull-up resistors on inputs. An external resistor is not required in any case.

OUTPUT INTERFACE

TTL/DTL INPUT STRUCTURES

Standard TTL circuits employ the input structure shown in Figure 8.

TYPICAL TTL INPUT STRUCTURE

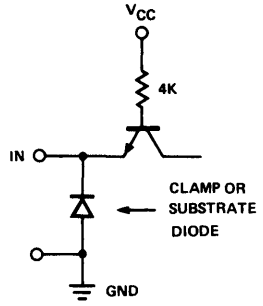


FIGURE 8

DTL circuits employ the structure shown in Figure 9.

TYPICAL DTL INPUT STRUCTURE

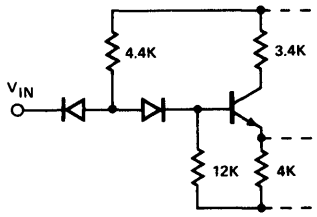


FIGURE 9

2500 SERIES OUTPUT STRUCTURES

Four basic types of output structures are used in the 2500 series:

1. Bare drain
2. Internal resistor pull-down
3. Push-pull
4. Three-state

See Figure 10.

TYPICAL 2500 SERIES OUTPUT CIRCUITS

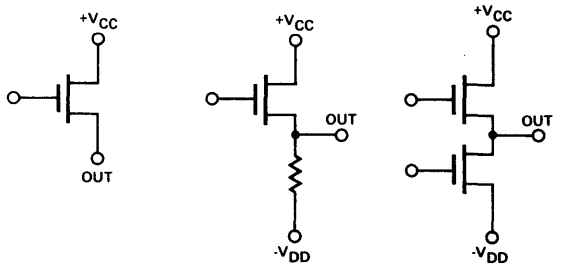


FIGURE 10

BARE DRAIN:

The bare drain output is the simplest structure and requires an external pull-down resistor. Bare drain is used where several outputs are to be tied together in a WIRED-OR configuration as shown in Figure 11.

WIRED-OR CONFIGURATION OF
TWO BARE DRAIN DEVICES

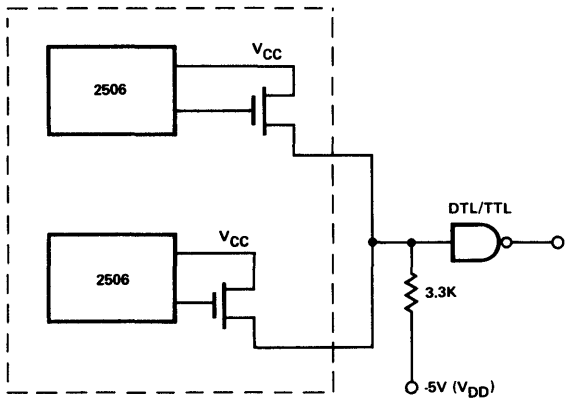


FIGURE 11

The external resistor is chosen to sink the 1.6mA required by a TTL gate. In Figure 11, a 3.3K resistor is tied to the V_{DD} supply. The output voltage will be +0.4V or less depending on the actual I_{OI} of the TTL input.

When the bare drain device is ON, it represents approximately 500 ohms. For the circuit of Figure 9, V_{OH} is approximately +3.7V – more than sufficient to drive a TTL or DTL gate. Bare drain 2500 devices are listed in Figure 12.

BARE DRAIN SERIES 2500 DEVICES

2502	2505	2519
2503	2512	2524
2504	2518	2525

FIGURE 12

RESISTOR PULL-DOWN

The second type of output has a pull-down resistor on the chip. The 2507 and 2517 are examples of this. The 2517 has a 20K ohm internal resistor for interfacing with MOS.

Resistor pull-down series 2500 devices are listed in Figure 13. The 2507 has a 7.5Kohm resistor, and if used in the WIRED-OR configuration with another 2507 output, will drive TTL directly as shown in Figure 14.

RESISTOR PULL-DOWN SERIES 2500 DEVICES

2507	7.5K
2517	20K

FIGURE 13

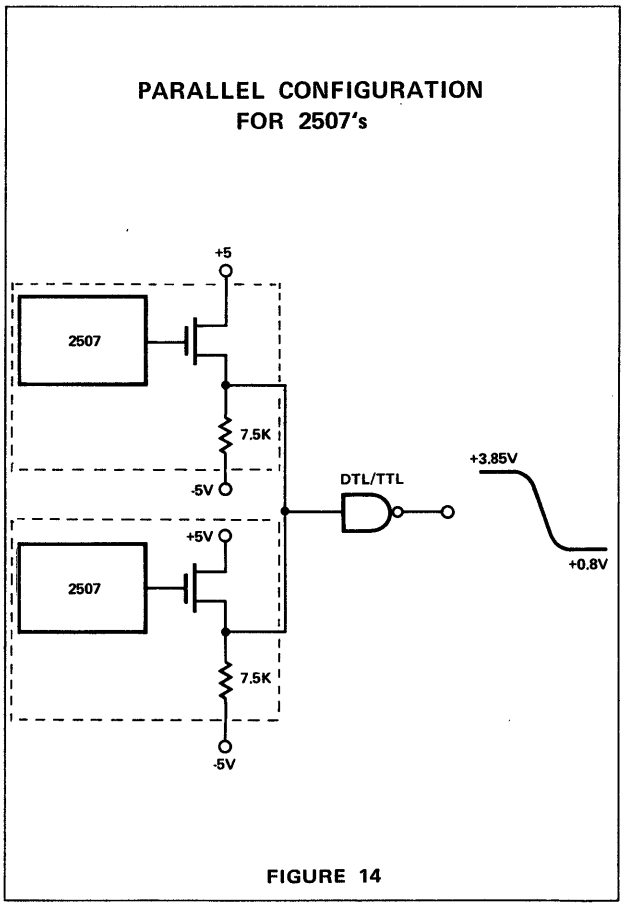


FIGURE 14

PUSH-PULL

The third type of output structure used in the 2500 Series is the push-pull circuit shown in Figure 10c. In the push-pull configuration, the gates of the two output devices are driven from complementary signals such that only one device is ON at a time. When the upper device is ON, the output is tied to V_{CC} through approximately 500 ohms. When the lower device in ON, the output is tied to V_{DD} through 500 ohms.

The advantage of this circuit is that no additional power is dissipated in either state. Both states have low impedance to the power supplies. Push-Pull output series 2500 devices are listed in Figure 15.

PUSH-PULL OUTPUT SERIES 2500 DEVICES

2521	2527	
2522	2528	2529

FIGURE 15

THREE-STATE

A disadvantage of the push-pull circuit is that paralleling of the outputs is not possible because two low impedance devices would be ON simultaneously directly across the power supplies. To avoid this condition, a three-state output is used. The third state is an open output configuration where both devices are OFF and is accomplished by using an OUTPUT ENABLE line tied to the gates of both output devices as shown in Figure 16. Three-state series 2500 devices are listed in Figure 17.

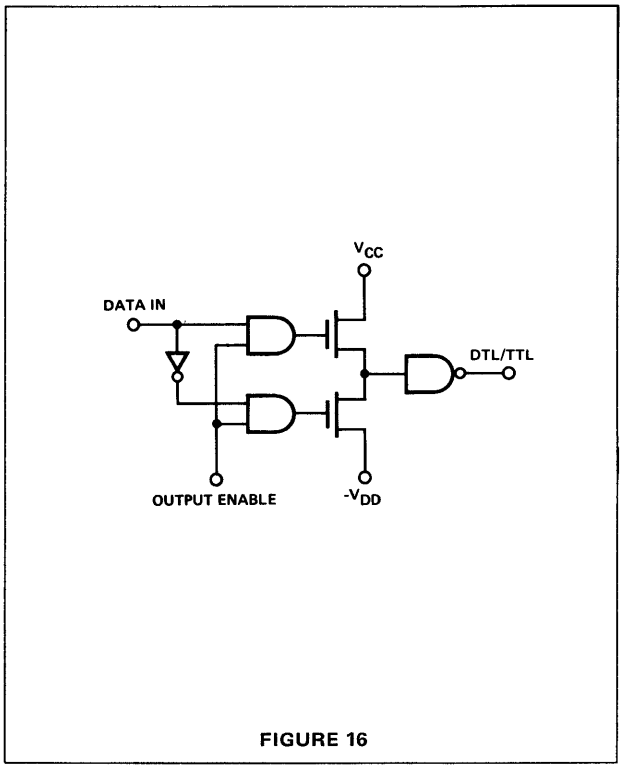


FIGURE 16

THREE-STATE SERIES 2500 DEVICES

2501	2510	2513	2516
2509	2511	2514	

FIGURE 17

Figure 18 summarizes the output configurations used on the 2500 Series circuits.

OUTPUT CONSIDERATIONS FOR 2500 LINE

PRODUCT NUMBER	DESCRIPTION	OUTPUT STRUCTURE	TO DRIVE ONE TTL/DTL USE*
1103	1024 x 1 dynamic RAM	Bare Drain	Sense Amp
2501	256 x 1 Static RAM	3-State	Direct
2502	256 x 4 Dynamic Shift Register	Bare Drain	3.0K
2503	512 x 2 Dynamic Shift Register	Bare Drain	3.0K
2504	1024 x 1 Dynamic Shift Register	Bare Drain	3.0K
2505/2524	512 x 1 Dynamic Shift Register	Bare Drain	3.0K
2506	100 x 2 Dynamic Shift Register	Bare Drain	3.0K
2507	100 x 2 Dynamic Shift Register	7.5K Resistor	6.8K
2509	50 x 2 Static Shift Register	3-State	Direct
2510	100 x 2 Static Shift Register	3-State	Direct
2511	200 x 2 Static Shift Register	3-State	Direct
2512/2525	1024 x 1 Dynamic Shift Register	Bare Drain	3.0K
2513	64 x 7 x 5 Character Generator	3-State	Direct
2514	512 x 5 ROM	3-State	Direct
2516	64 x 6 x 8 Character Generator	3-State	Direct
2517	100 x 2 Dynamic Shift Register	20K Resistor	3.3K
2518	32 x 6 Static Shift Register	Bare Drain	6.8K
2519	40 x 6 Static Shift Register	Bare Drain	6.8K
2521	128 x 2 Static Shift Register	Push-Pull	Direct
2522	132 x 2 Static Shift Register	Push-Pull	Direct
2527	256 x 2 Static Shift Register	Push-Pull	Direct
2528	250 x 2 Static Shift Register	Push-Pull	Direct
2529	240 x 2 Static Shift Register	Push-Pull	Direct

*NOTE: Values are given for the maximum value of pull-down resistor, output to V_{DD}.

FIGURE 18

"OR" TYING OUTPUTS

The characteristics of the four types of output structures differ when tied together. A basic feature of MOS is that the design limitation on output "OR"ing is related to the output voltage levels required and the RC time constant of the resulting network.

BARE DRAIN

The number of bare drain devices which can be tied together is limited by the output time constant and the V_{OH} level required.

Switching time for the pull-down condition is determined by the load resistor R_{PD} and load capacitance C_L. The MOS pull-up device is turned off and does not contribute to the negative going time constant. See Figure 19.

C_L is comprised of wiring capacitance (C_W) and output capacitance (C_{OUT}) from each of the paralleled outputs.

As the number of paralleled devices increases, the value of R_{PD} must be decreased to maintain speed.

When driving loads having significant input capacitance, C_L should be increased accordingly.

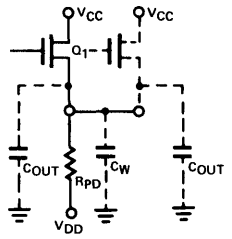


FIGURE 19

As R_{PD} is decreased, V_{OH} decreases since the impedance of Q1 when ON (approx. 500 ohms) will ratio with R_{PD} to produce V_{OH}. If R_{PD} is reduced too far, the output voltage will be insufficient to turn off the TTL gate being driven.

Figure 20 gives the recommended value of R_{PD} as a function of fan-out for 2500 series bare drain devices.

Fan-Out	C_L	R_{PD} *	V_{OH}
1	15pF	3.3K	3.7V
2	20pF	2.5K	3.3V
3	25pF	2K	3.0V
4	30pF	1.67K	2.7V
5	35pF	1.43K	2.4V

* For t_F= 50ns

FIGURE 20

Figure 20 assumes 10pF of wiring capacitance and 5pF per output. It should be noted that when the MOS device is OFF, the TTL input current of 1.6mA is sunk to -5V. When set up for a fanout of 5, the 1.6mA from the TTL gate will bring the output to only -2.7V. In actuality the input clamp or substrate diode of the TTL gate will turn on and clamp the output to -1.0V. The diode will supply the additional current (approximately 1.9mA).

INTERNAL PULL-DOWN

When 2500 Series devices with internal pull-down resistors are paralleled, the equivalent resistance R_{PD} is the parallel combination of all the internal resistors. A chart of the equivalent resistance, output time constant and V_{OH} for the 2507 with a 7.5K internal pull-down resistor is shown in Figure 21.

Fan-Out	C_L	R_{PD}	t_f	V_{OH}
1	15	7.5K	110nS	4.4V
2	20	3.75K	75nS	3.8V
3	25	2.5K	63nS	3.3V
4	30	1.87K	56nS	2.9V
5	35	1.5K	53nS	2.5V

FIGURE 21

PUSH-PULL OUTPUTS

Push-Pull outputs allow low rise and fall times but cannot be paralleled because it would then be possible to have both a push and a pull device on at the same time resulting in a low impedance between the power supplies (and indeterminate output level).

THREE STATE OUTPUTS

The three state output is designed to take advantage of push-pull drive capability plus the ability to OR the outputs.

The third (or open) state is used when the chip is unselected. The selected output is free to drive the load without being affected by the other outputs tied to the bus.

Output rise and fall times for the WIRED OR configuration of three-state devices is a function of the ON resistance of the individual pull-up and pull-down devices together with the load capacitance.

A CLOCK DRIVER FOR 2500 SERIES MOS

In order to obtain optimum performance from MOS devices, they must be provided with clock signals of the proper amplitude, shape and timing. This section will present a simple clock generator and driver scheme suitable for use with 2500 Series MOS devices.

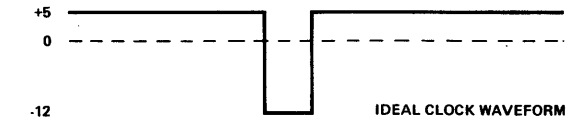
NOTE: The following devices employ on-chip clock generators and may be driven directly by TTL gates:

2509 2510 2511 2518 2519 2521 2522

The clock driver must provide relatively large voltage swings for the clock lines. In the case of 2500 Series MOS, the clock signal must swing from +5V to -12V. And it must provide a clean waveform having reasonable rise and fall times (under 40 ns.) and lack of positive overshoot.

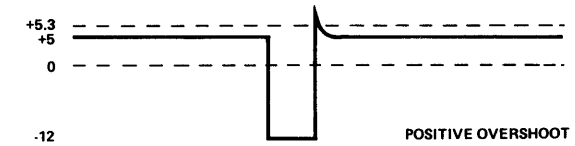
IMPROPER CLOCK WAVEFORMS

Some common examples of improper clocking are shown in Figures 23, 24, and 25.



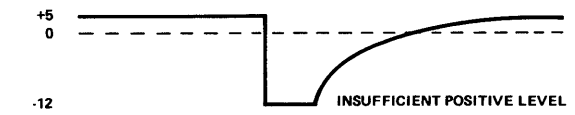
NOTE:
An ideal clock driving waveform.

FIGURE 22



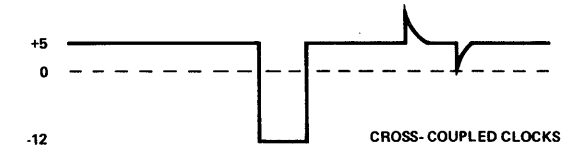
NOTE:
Shows an overshoot occurring on the positive going transition of clock. This has the effect of forward biasing the substrate diode and must be avoided to prevent erratic behavior in the driven device.

FIGURE 23



NOTE:
Shows the clock never returns to 5V (0 reference) to turn the input device OFF. This clock can sometimes appear to be functional. Data may toggle through a shift register, but will not be stored.

FIGURE 24



NOTE:
Shows cross-coupling between two clock drivers usually caused by lack of clamping or non-active (high-impedance) switching in the positive direction.

FIGURE 25

The positive overshoots illustrated in Figure 23 and Figure 25 are the most common sources of clock driving trouble. When the clock line goes positive relative to the circuit substrate (V_{CC}) by more than approximately 0.3V, the substrate diode may become forward biased. When this occurs, device operation may become erratic. And because the forward characteristics of the substrate diode may be different for different processing techniques, a clock driver may work properly with one device but not with another.

A properly designed driver utilizing level clamping will prevent the overshoot problem.

THE DRIVER OUTPUT STRUCTURE

Figures 26, 27, and 28 show possible output driver structures together with their advantages and disadvantages.

RESISTOR PULL-UP, POOR NOISE IMMUNITY, AND SLOW RISE TIME

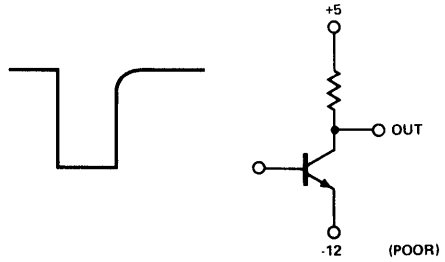


FIGURE 26

PUSH-PULL, SLOW RISE AND FALL TIME

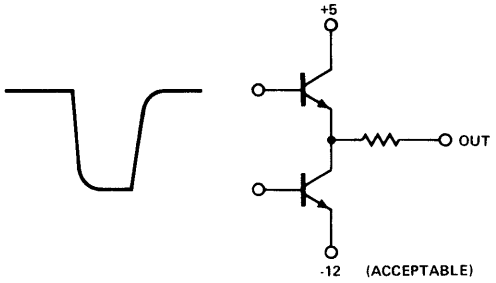


FIGURE 27

COMPLEMENTARY, EXCELLENT NOISE IMMUNITY, FAST RISE AND FALL TIME

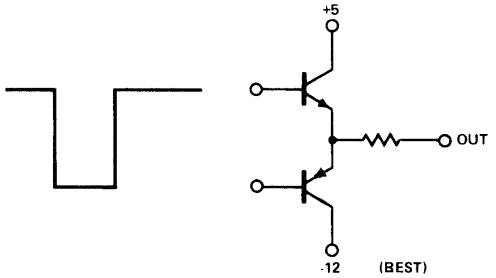
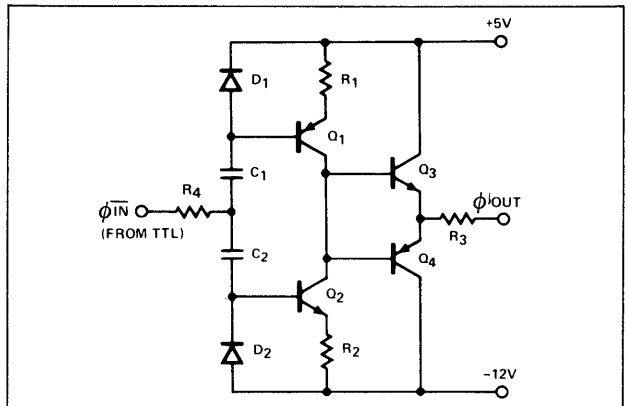


FIGURE 28

The driver circuit recommended here (Figure 29) utilizes a complementary output structure to obtain maximum noise immunity and fast rise and fall time under heavy capacitive load. It is capacitively coupled to the TTL clock generator. Resistor R_4 is required only when operating at a clock frequency of lower than 750 KHz. This resistor shifts the response of the driver input circuit toward the lower frequencies by lengthening the input time constant. One clock driver is required for each clock phase.



Q_1, Q_4 2N2905, Heat Sink Required
Q_2, Q_3 2N2222, Heat Sink Required
C_1, C_2 100pF
D_1, D_2 1N914
R_1, R_2, R_3 33 Ohm
R_4 2.2K Ohm (Required only for operation below 750KHz)

FIGURE 29

GENERATING MULTIPLE PHASES

The 2500 Series MOS devices which require high level clocks also require more than one phase. The dynamic shift registers require two phases and the 2508 dynamic RAM requires four phases.

TWO PHASE SYSTEM

The clock generator in Figure 30 produces alternate pulses - the width of which are one quarter of the input clock period (assuming a square wave clock). See Figure 32.

TWO PHASE TTL CLOCK GENERATOR

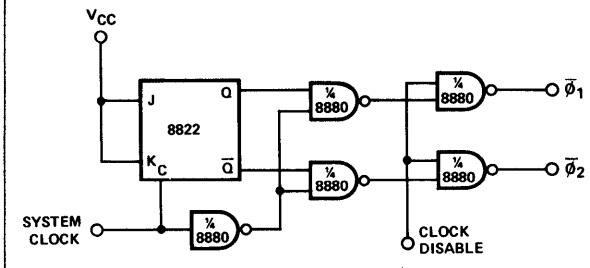


FIGURE 30

When required, the clock pulse widths can be varied by using one-shot multivibrators such as the 8162 or 74121. Each phase width can be varied independently (the limiting factor being the clock period), see Figure 31(a), or a single one-shot ahead of the clock generator will change both phases simultaneously. See Figure 31(b).

METHOD OF PROVIDING INDEPENDENTLY VARIABLE CLOCK PHASES

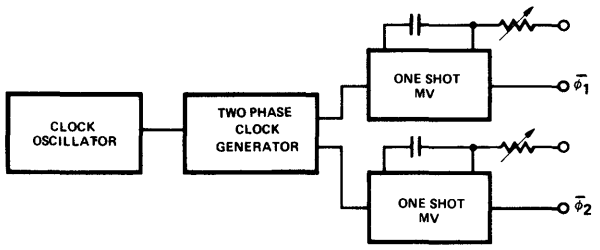


FIGURE 31(a)

METHOD OF PROVIDING VARIABLE CLOCK PHASES

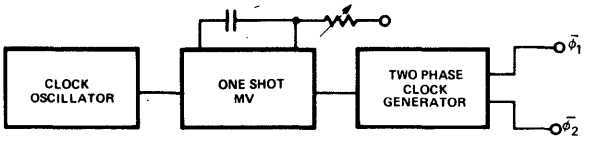


FIGURE 31(b)

TWO PHASE CLOCK GENERATOR WAVEFORMS

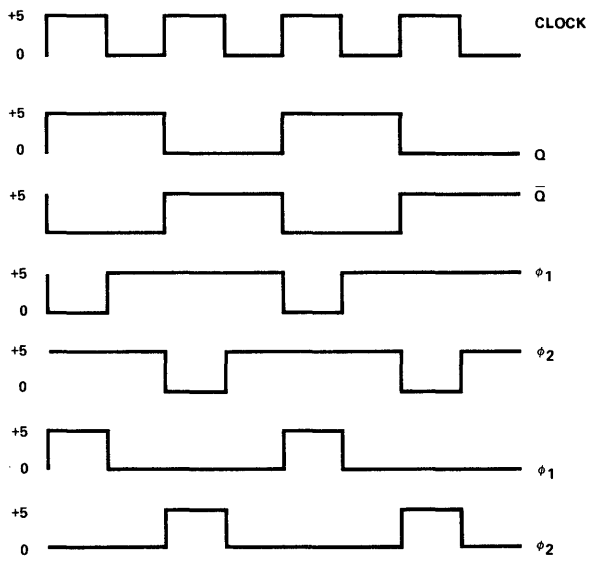


FIGURE 32

FOUR PHASE SYSTEM

The circuit shown in Figure 33(a) and (b) can be used to generate four phase clock signals for the 2508 1024 RAM.

DIVIDE-BY-12 SYNCHRONOUS COUNTER

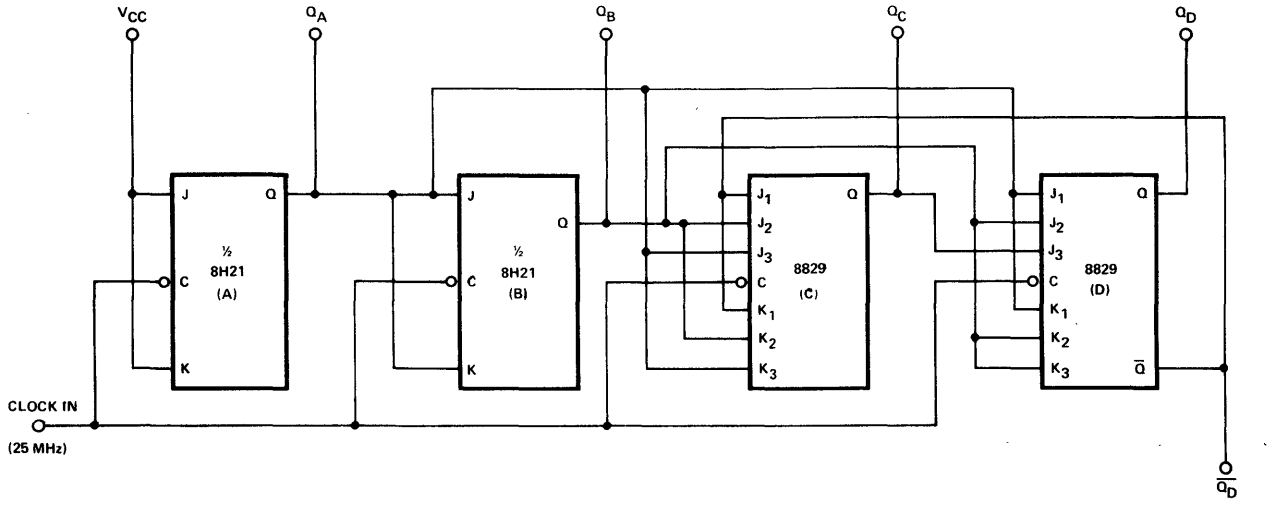


FIGURE 33(a)

FOUR PHASE SYSTEM

FOUR PHASE DECODER

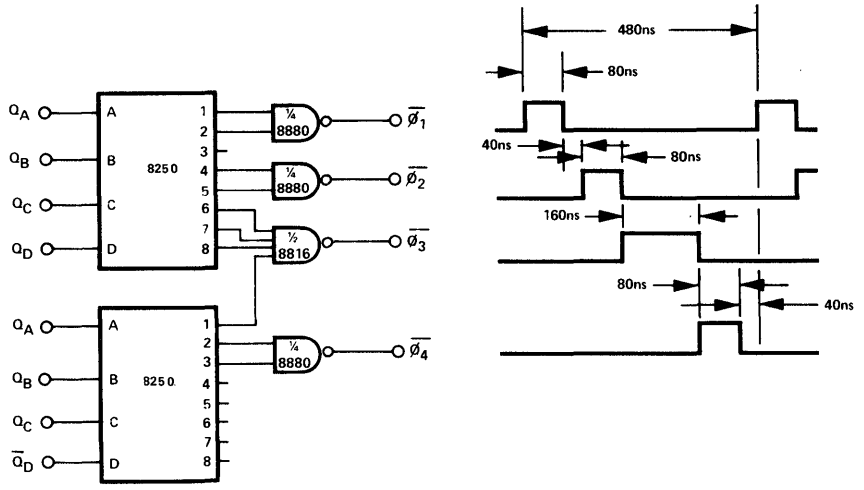


FIGURE 33(b)

Figure 34 shows typical clock input capacitances for 2500 Series devices. The number of similar devices which can be driven by one clock driver is indicated.

DEVICE	TYPICAL CLOCK CAPACITANCE (pF)	NO. OF UNITS WHICH CAN BE DRIVEN (INCLUDES ALLOWANCE FOR WIRING CAPACITANCE)	
		<2MHz (1)	2-4MHz (2)
2502	140	8	6
2503	140	8	6
2504	140	8	6
2505	80	12	9
2506	25	40	30
2507	25	40	30
2508	25	40	30
2512	100	11	7
2517	25	40	30
2524	80	12	9
2525	100	11	7

(1) Drive capacity 1200pF
(2) Drive capacity 750pF

FIGURE 34

FULLY DECODED RANDOM ACCESS 1024 BIT DYNAMIC MEMORY

1103
1103-1*

SILICON GATE 2500 SERIES

DESCRIPTION

The Signetics 1103 is designed for main memory applications where high performance, low cost and large bit storage are important design objectives. It is a 1024 word by 1 bit random access memory element using enhancement mode P-channel MOS devices integrated on a monolithic array. It is fully decoded, permitting the use of an 18-pin dual in-line package. The dynamic circuitry dissipates significant power only during precharge. Information stored in the memory is nondestructively read. Refreshing of all 1024 bits is accomplished in 32 read cycles and is required every two milliseconds. A separate cenable (chip enable) lead allows easy selection of an individual package when outputs are OR-tied.

FEATURES

- LOW POWER DISSIPATION – DISSIPATES POWER PRIMARILY ON SELECTED CHIPS
- ACCESS TIME – 300 nsec.
- CYCLE TIME – 580 nsec.
- REFRESH PERIOD – 2 MILLISECONDS FOR 0-70°C AMBIENT
- OR-TIE CAPABILITY
- SIMPLE MEMORY EXPANSION WITH CHIP ENABLE
- FULLY DECODED – ON-CHIP ADDRESS DECODE
- INPUTS PROTECTED – ALL INPUTS HAVE PROTECTION AGAINST STATIC CHARGE.
- LOW COST PACKAGING –18 PIN SILICONE AND 18 PIN CERAMIC DUAL IN-LINE

APPLICATIONS

CORE MEMORY REPLACEMENT
BUFFER STORES
MAIN MEMORY

PROCESS TECHNOLOGY

The use of Signetics' unique silicon gate low threshold process allows the design and production of higher performance MOS circuits and provides higher functional density on a chip than other MOS technologies.

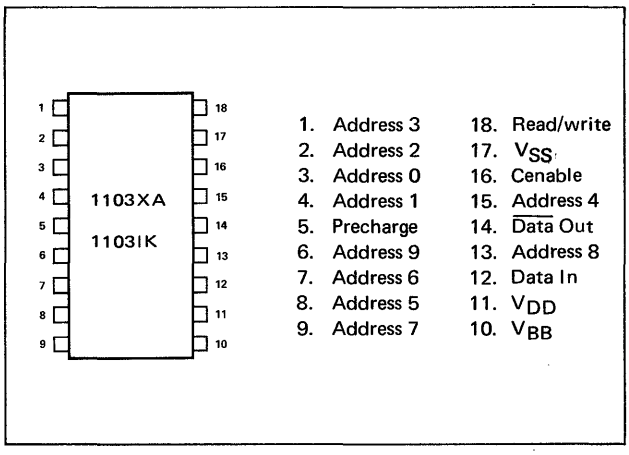
SILICONE PACKAGING

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process, the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric

SILICONE PACKAGING (Cont'd)

material over the silicon gate-oxide-substrate structure provides an ion barrier. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability and demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers.

PIN CONFIGURATION (Top View)

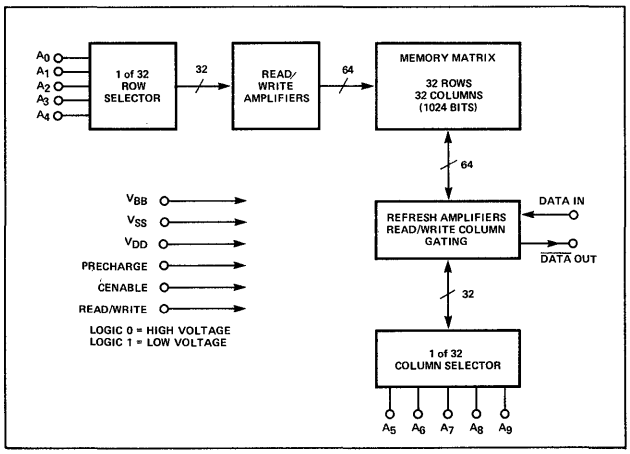


1. Address 3
2. Address 2
3. Address 0
4. Address 1
5. Precharge
6. Address 9
7. Address 6
8. Address 5
9. Address 7
10. V_{BB}
11. V_{DD}
12. Data In
13. Address 8
14. $\overline{\text{Data}}$ Out
15. Address 4
16. Cenable
17. V_{SS}
18. Read/write

PART IDENTIFICATION TABLE

TYPE	PACKAGE	OP. TEMP. RANGE
1103XA	18-Pin DIP Silicone	0-70°C
1103IK	18-Pin DIP Ceramic	0-70°C

BLOCK DIAGRAM



* HIGHER SPEED VERSION OF 1103. Contact Signetics for specifications.

MAXIMUM GUARANTEED RATINGS(10)

Operating Ambient Temperature	0°C to 70°C	Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB}	−25V to 0.3V
Storage Temperature	−65°C to +150°C	Power Dissipation	1.0W
All Input or Output Voltages with Respect to the Most Positive Supply Voltage, V_{BB}	−25V to 0.3V		

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{SS}(1) = 16V ± 5%, (V_{BB} −V_{SS})(6) = 3V to 4V, V_{DD} = 0V unless otherwise specified (Note 9).

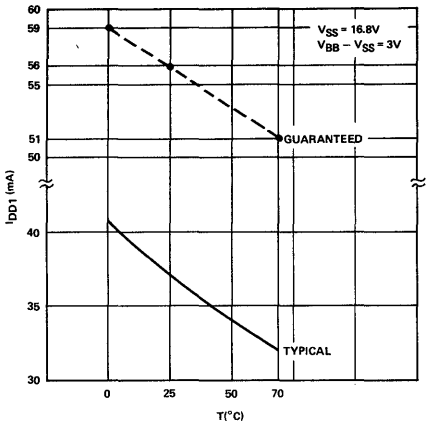
SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI}	Input Load Current (All input pins)			1	μA	V_{IN} = 0V, T_A = 25°C
I_{LO}	Output Leakage Current			1	μA	V_{OUT} = 0V, T_A = 25°C
I_{BB}	V_{BB} Supply Current			100	μA	
I_{DD1}(2)	Supply Current During t_{PC}		37	56	mA	All Addresses = 0V Precharge = 0V Cenable = V_{SS}; T_A = 25°C
I_{DD2}(2)	Supply Current During t_{OV}		38	59	mA	All Addresses = 0V Precharge = 0V Cenable = 0V; T_A = 25°C
I_{DD3}(2)	Supply Current During t_{POV}		5.5	11	mA	Precharge = V_{SS} Cenable = 0V; T_A = 25°C
I_{DD4}(2)	Supply Current During t_{CP}		3	4	mA	Precharge = V_{SS} Cenable = V_{SS}; T_A = 25°C
I_{DD}(5)AV	Average Supply Current		17	25	mA	Cycle Time = 580 ns; Precharge Width = 190 ns; T_A = 25°C
V_{IL1}(7)	Input Low Voltage (All Address & Data-in Lines)	V_{SS}−17		V_{SS}−14.2	V	T_A = 0°C
V_{IL2}(7)	Input Low Voltage (All Address & Data-in Lines)	V_{SS}−17		V_{SS}−14.5	V	T_A = 70°C
V_{IL3}(7,8)	Input Low Voltage (Precharge Cenable & Read/Write Inputs)	V_{SS}−17		V_{SS}−14.7	V	T_A = 0°C
V_{IL4}(7,8)	Input Low Voltage (Precharge Cenable & Read/Write Inputs)	V_{SS}−17		V_{SS}−15.0	V	T_A = 70°C
V_{IH1}(7)	Input High Voltage (All Inputs)	V_{SS}−1		V_{SS}+1	V	T_A = 0°C
V_{IH2}(7)	Input High Voltage (All Inputs)	V_{SS}−0.7		V_{SS}+1	V	T_A = 70°C
I_{OH1}	Output High Current	600	900	4000	μA	T_A = 25°C, R_{LOAD} = 100Ω(4)
I_{OH2}	Output High Current	500	800	4000	μA	T_A = 70°C, R_{LOAD} = 100Ω(4)
I_{OL}	Output Low Current	See Note 3				R_{LOAD} = 100Ω(4)
V_{OH1}	Output High Voltage	60	90	400	mV	T_A = 25°C, R_{LOAD} = 100Ω(4)
V_{OH2}	Output High Voltage	50	80	400	mV	T_A = 70°C, R_{LOAD} = 100Ω(4)
V_{OL}	Output Low Voltage	See Note 3				

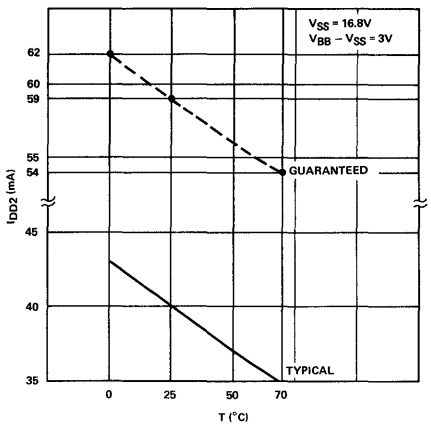
NOTES:

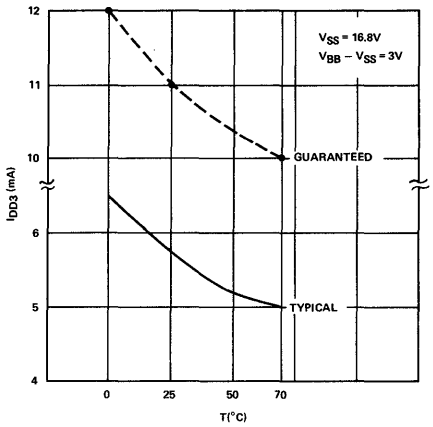
1. The V_{SS} current drain is equal to (I_{DD} + I_{OH}) or (I_{DD} + I_{OL}).
2. See Supply Current vs. Temperature (p. 3) for guaranteed current at the temperature extremes. These values are taken from a single pulse measurement.
3. The output current when reading a low output is the leakage current of the 1103 plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.
4. This value of load resistance is used for measurement purposes. In applications the resistance may range from 100Ω to 1 kΩ.
5. This parameter is periodically sampled and is not 100% tested.
6. (V_{BB} − V_{SS}) supply should be applied at or before V_{SS}.
7. The maximum values for V_{IL} and the minimum values for V_{IH} are linearly related to temperature between 0°C and 70°C. Thus any value between 0°C and 70°C can be calculated using a straignt-line relationship.
8. The maximum values for V_{IL} (for precharge, cenable & read/write) may be increased to V_{SS}−14.2 @ 0°C and V_{SS}−14.5 @ 70°C (same values as those specified for the address and data-in lines) with a 40 ns degradation (worst case) in t_{AC}, t_{PC}, t_{RC}, t_{WC}, t_{RWC}, t_{ACC1} and t_{ACC2}.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

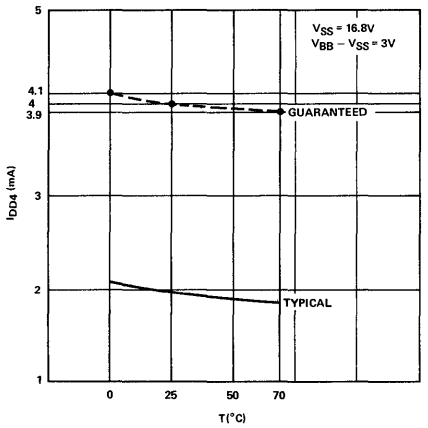
CHARACTERISTIC CURVES

SUPPLY CURRENT VS TEMPERATURE

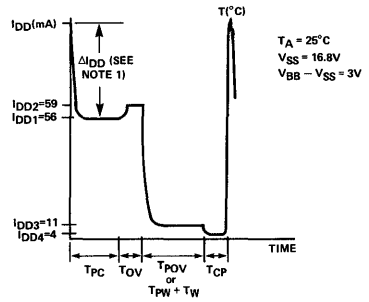








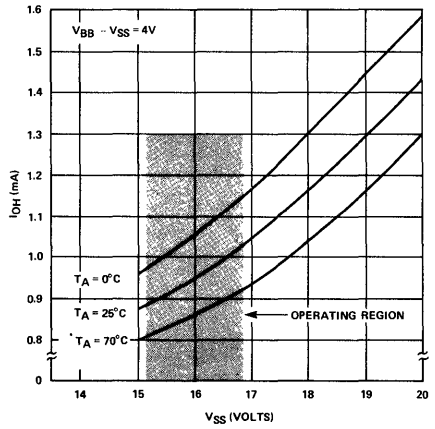
I_{DD} VS TIME

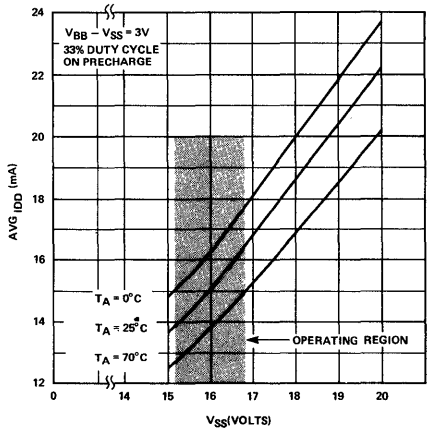


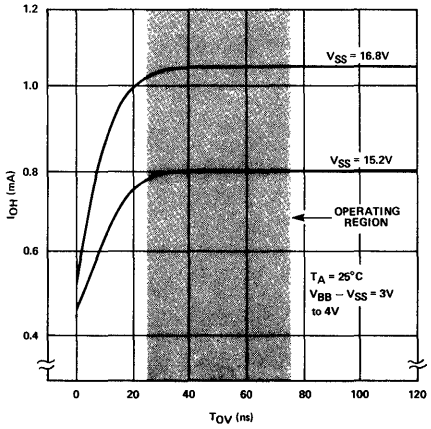
NOTES:

1. ΔI_{DD} is due to charging of internal device node capacitance at precharge.
2. These values are taken from a single pulse measurement.

CHARACTERISTIC CURVES (Cont'd)







AC CHARACTERISTICS $T_A = 25°C$, $V_{SS} = 16 \pm 5\%$, $(V_{BB} - V_{SS}) = 3.0V$ to $4.0V$, $V_{DD} = 0V$

READ, WRITE, AND READ/WRITE CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{REF}	Time Between Refresh			2	ms	
t_{AC}(1)	Address to Cenable Set Up Time	115			ns	
t_{CA}	Cenable to Address Hold Time	20			ns	
t_{PC}(1)	Precharge to Cenable Delay	125			ns	
t_{OVL}	Precharge & Cenable Overlap, Low	25		75	ns	
t_{CP}	Cenable to Precharge Delay	85			ns	
t_{OVH}	Precharge & Cenable Overlap, High			140	ns	

READ CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{RC}(1)	Read Cycle	480			ns	
t_{POV}	Precharge to End of Cenable	165		500	ns	
t_{PO}	End of Precharge to Output Delay			120	ns	t_T = 20 ns
t_{ACC1}(1)	Address to Output Access	300			ns	$t_{ACmin} + t_{OVLmin} + t_{POmax} + 2\,t_T$; C_{LOAD} = 100 pF, R_{LOAD} = 100Ω, V_{REF} = 40 mV
t_{ACC2}(1)	Precharge to Output Access	310			ns	$t_{PCmin} + t_{OVLmin} + t_{POmax} + 2\,t_T$

AC CHARACTERISTICS(Cont'd)

WRITE OR READ/WRITE CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{WC}(1)	Write Cycle	580			ns	t_T = 20 ns
t_{RWC}(1)	Read/Write Cycle	580			ns	
t_{PW}	Precharge to Read/Write Delay	165		500	ns	
t_{WP}	Read/Write Pulse Width	50			ns	
t_W	Read/Write Set Up Time	80			ns	
t_{DW}	Data Set Up Time	105			ns	
t_{DH}	Data Hold Time	10			ns	
t_{PO}	End of Precharge to Output Delay			120	ns	C_{LOAD} = 100 pF R_{LOAD} = 100Ω V_{REF} = 40 mV
t_P	Time to Next Precharge	0			ns	
t_{CW}	Read/Write Hold Time			10	ns	

CAPACITANCE (note 2)

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
C_{AD}	Address Capacitance		5	7	pF	$V_{IN} = V_{SS}$
C_{PR}	Precharge Capacitance		15	18	pF	$V_{IN} = V_{SS}$
C_{CE}	Cenable Capacitance		15	18	pF	$V_{IN} = V_{SS}$
C_{RW}	Read/Write Capacitance		11	15	pF	$V_{IN} = V_{SS}$
C_{IN1}	Data Input Capacitance		4	5	pF	Cenable = 0V $V_{IN} = V_{SS}$
C_{IN2}	Data Input Capacitance		2	4	pF	Cenable = V_{SS} $V_{IN} = V_{SS}$
C_{OUT}	Data Output Capacitance		2	3	pF	V_{OUT} = 0V

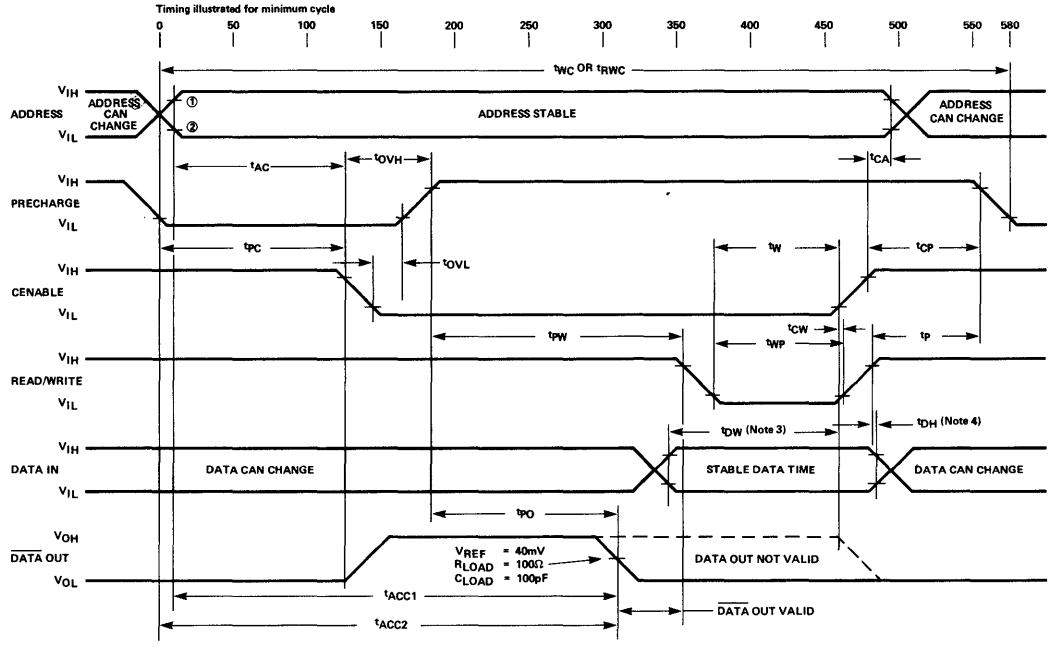
f = 1 MHz, All Unused Pins are at A.C. Ground

(1) These times will degrade by 40 ns (worst case) if the maximum values for V_{IL} (for precharge, cenable and read/write inputs) go to V_{SS} − 14.2V @ 0°C and V_{SS}−14.5V @ 70°C as defined on page 2.

(2) This parameter is periodically sampled and is not 100% tested. It is measured at worst case operating conditions. Capacitance measurements for plastic packages only.

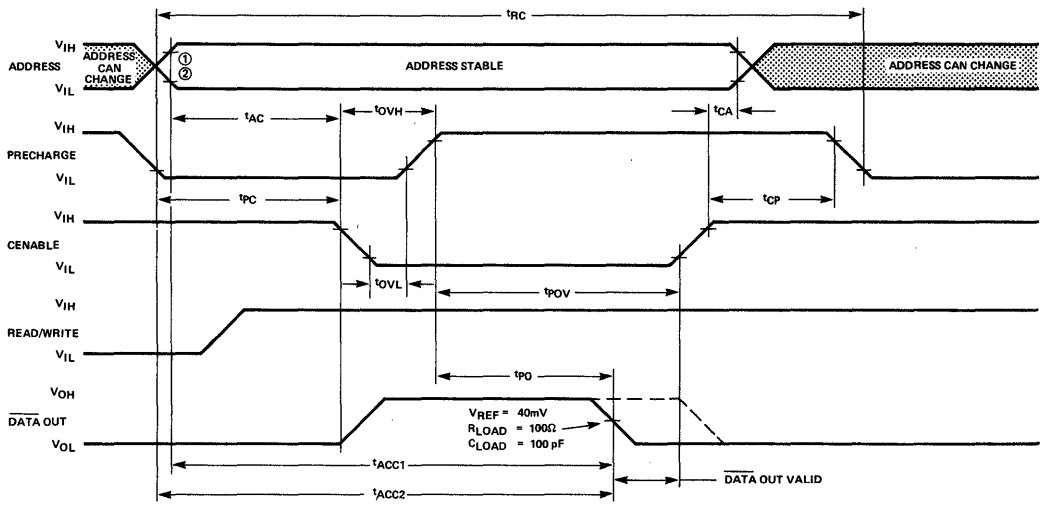
TIMING DIAGRAM

WRITE CYCLE OR READ/WRITE CYCLE



TIMING DIAGRAM (Cont'd)

READ CYCLE



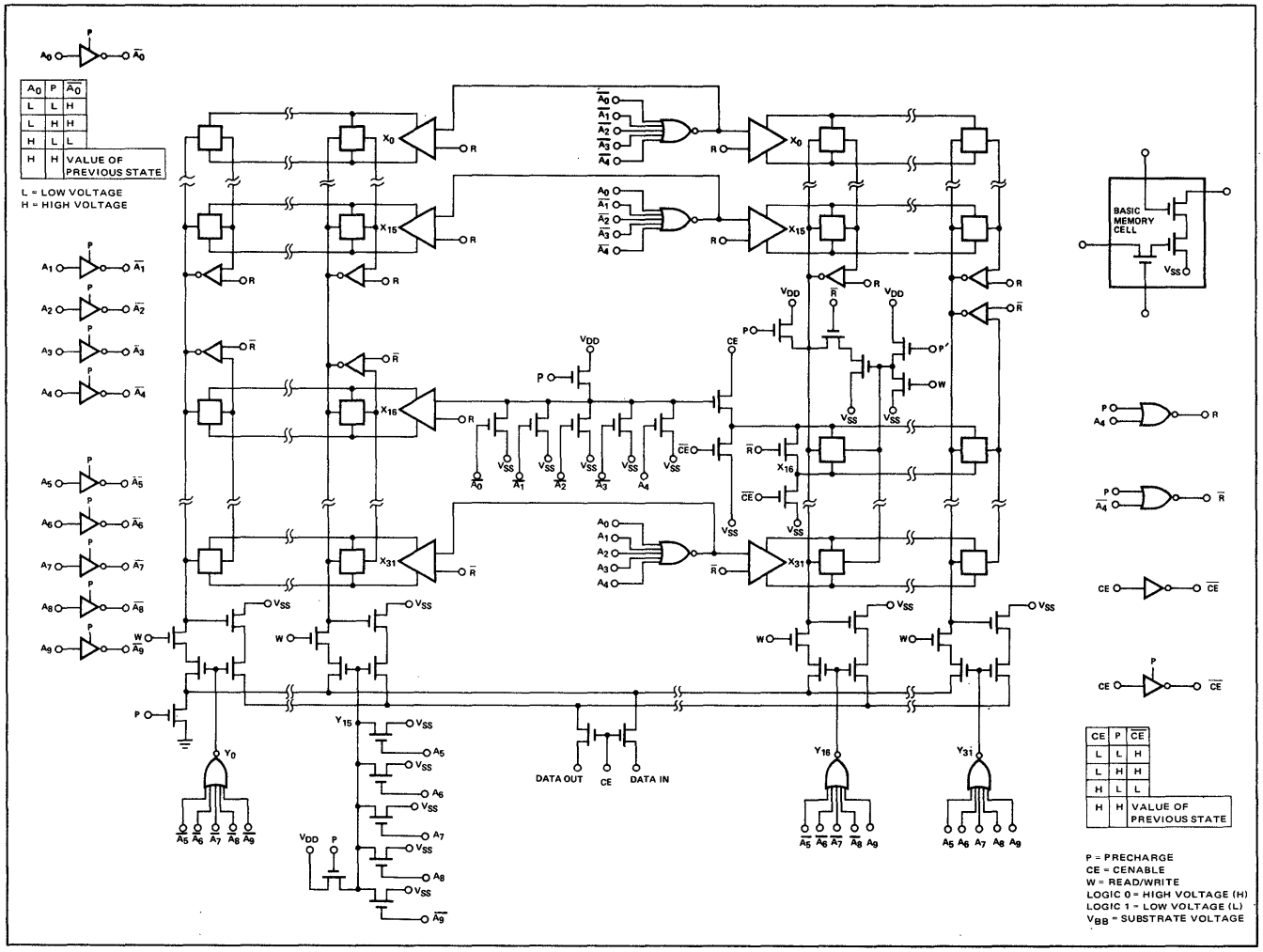
NOTES:

① V_{DD} + 2V
② V_{SS} - 2V
t_T is defined as the transitions between these two points.

3 t_{DW} is referenced to point ② of the rising edge of cenable or read/write whichever occurs first.

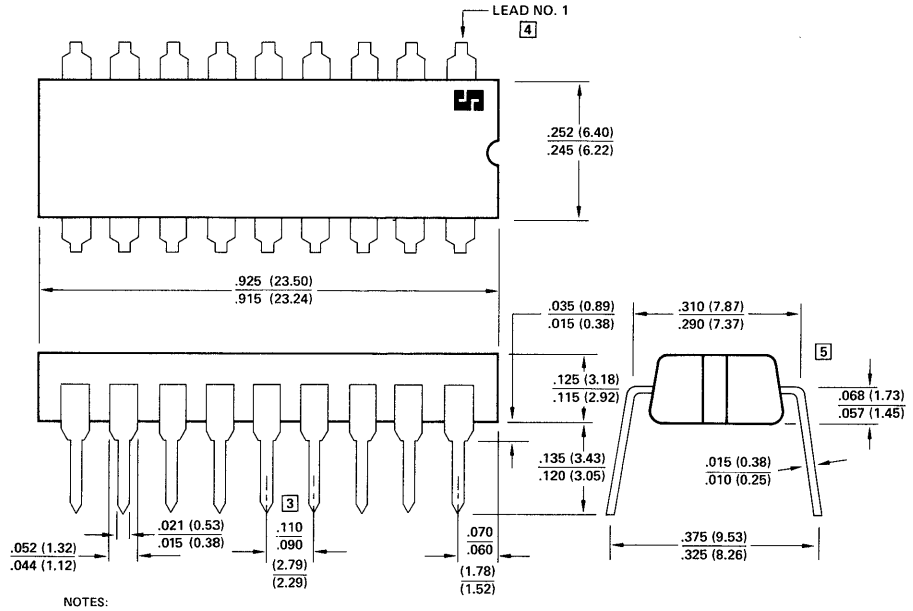
4 t_{DH} is referenced to point ① of the rising edge of cenable or read/write whichever occurs first.

CIRCUIT SCHEMATIC



PACKAGE INFORMATION

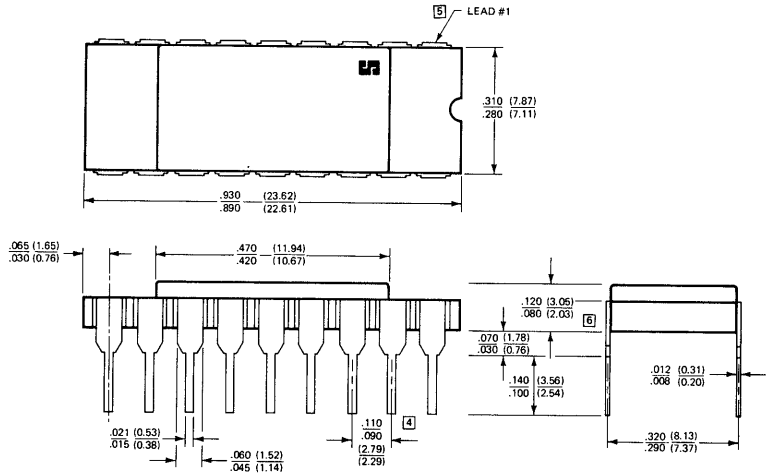
XA PACKAGE



NOTES:

1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: SILICONE MOLDED.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: Θ JA = .16°C/mW, Θ JC = .08°C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

IK PACKAGE



NOTES:

1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED.
2. BODY MATERIAL: CERAMIC WITH KOVAR OR EQUIVALENT.
3. LID MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED, ALLOY SEAL.
4. TOLERANCES NON CUMULATIVE.
5. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
6. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
7. THERMAL RESISTANCE: Θ Ja = .060°C/mW, Θ Jc = .015°C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

FULLY DECODED, 256 X 1 STATIC RANDOM ACCESS MEMORY

2501
25L01*

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The Signetics 2500 Series 256 x 1 Random Access Memory employs enhancement mode P-channel MOS devices integrated on a single monolithic chip. It is fully decoded, permitting the use of a 16-pin dual in-line package. Complete static operation requires no clocking.

FEATURES

- FULLY DECODED ADDRESS
- ACCESS TIME – 1.0μs GUARANTEED
- POWER DISSIPATION -1.6mW/BIT MAXIMUM DURING ACCESS
- STANDBY POWER DISSIPATION – 50 μW/BIT
- DTL AND TTL COMPATIBLE
- CHIP SELECT AND OUTPUT WIRED-OR CAPABILITY FOR EASY EXPANSION
- STANDARD 16-PIN DIP SILICONE PACKAGE
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY
- V_{CC} = +5V, V_{DD} = -7, V_D = -10V RECOMMENDED
- V_{DD} AND V_D MAY BE TIED FOR SINGLE NEGATIVE POWER SUPPLY (-9V RECOMMENDED)
- GUARANTEED OPERATION WITH 3V V_{DD}-V_D SEPARATION

APPLICATIONS

SMALL BUFFER STORES
SMALL CORE MEMORY REPLACEMENT
BIPOLAR COMPATIBLE DATA STORAGE

SILICONE PACKAGING

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric material over the silicon gate-oxide-substrate structure provides an ion barrier. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability and demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers.

PROCESS TECHNOLOGY

The use of Signetics' unique Silicon Gate Low Threshold Process allows the design and production of higher performance MOS circuits and provides higher functional density on a chip than other MOS technologies.

BIPOLAR COMPATIBILITY

All inputs of the 2501 can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.). The data output buffers are capable of sinking a minimum of 2.0 mA, sufficient to drive one standard TTL load.

POWER DISSIPATION

The maximum power dissipation of 1.6mW/bit is required only during Read or Write. For standby operation, 50μW/bit is obtained by removing V_D and reducing V_{DD} to −2.0V. Removal of V_D alone will cut power dissipation by a factor of 1.5.

SPECIAL FEATURE

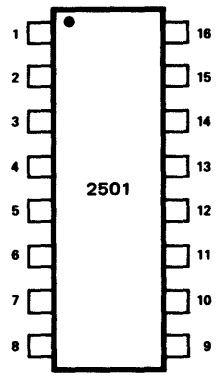
The outputs of the 2501 are effectively open circuited when the device is not selected (logic 1 on chip select). This feature allows OR-Tying for memory expansion.

PART IDENTIFICATION TABLE

TYPE	PACKAGE	OP. TEMP. RANGE
2501B	16-pin Silicone DIP	0°C. to +70°C.

PIN CONFIGURATION (Top View)

B PACKAGE



1. Address 6
2. Address 8
3. Address 7
4. V_D
5. V_{CC}
6. Address 5
7. Address 1
8. V_{DD}
16. $\overline{\text{Chip Select}}$
15. R/W
14. $\overline{\text{Data Out}}$
13. Data Out
12. Data In
11. Address 4
10. Address 2
9. Address 3

* LOW POWER VERSION OF THE 2501 FOR +5 AND −12V OPERATION. Contact Signetics for specifications.

MAXIMUM GUARANTEED RATINGS (1)

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to the Most Positive Supply Voltage, V_{CC}	+0.3V to -20V
Supply Voltages V_{DD} and V_D with Respect to V_{CC}	-18V
Power Dissipation at T_A = 70°C	640mW

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.

DC CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = +5V (8), V_{DD} = −7± 5% , V_D = −10V± 5% unless otherwise specified. See notes above)

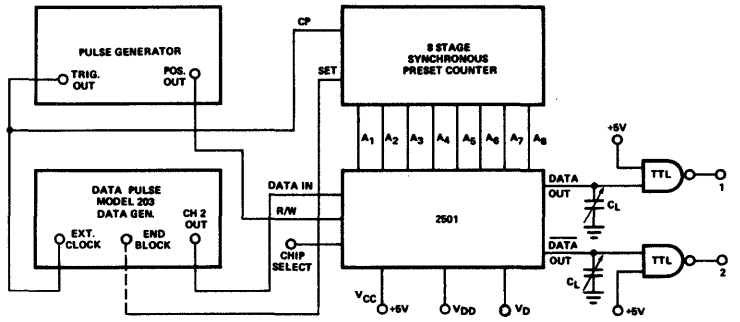
SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI}	Input Load Current (All Input Pins)		<1.0	500	nA	V_{IN} = 0.0V; T_A = +25°C
I_{LO}	Output Leakage Current		<1.0	1000	nA	V_{OUT} = 0.0V, Chip Select Input = +3.3V, T_A = +25°C
I_{DD}	Power Supply Current, V_{DD}		10	15	mA	T_A = +25°C
I_D	Power Supply Current, V_D		10	14	mA	I_{OL} = 0.0 mA T_A = +25°C
I_{DD}	Power Supply Current, V_{DD}		13.0	18	mA	T_A = +25°C, V_{DD} = V_D = −9V
I_D	Power Supply Current, V_D		8.5	12	mA	I_{OL} = 0.0mA T_A = +25°C V_{DD} = V_D = −9V
V_{IL}	Input "Low" Voltage			1.05	V	
V_{IH}	Input "High" Voltage	3.2		5.3	V	
I_{OL1}	Output Sink Current	3.0	6		mA	V_{OUT} = +0.45V, T_A = +25°C
I_{OL2}	Output Sink Current	2.0	5		mA	V_{OUT} = +0.45V, T_A = +70°C
I_{OL3}	Output Sink Current		6	13	mA	V_{OUT} = −0.7 V
I_{OH1}	Output Source Current	−3.0	-6		mA	V_{OUT} = 0.0V, T_A = +25°C
I_{OH2}	Output Source Current	−2.0	-5		mA	V_{OUT} = 0.0V, T_A = +70°C
V_{OL}	Output "Low" Voltage		−0.7	+0.45	V	I_{OL} = 3.0 mA
V_{OH}	Output "High" Voltage	+3.5	+4.5		V	I_{OH} = −100μA
C_{IN}	Input Capacitance (All Input Pins)		7	10	pF	V_{IN} = +5.0V f = 1 MHz
C_{OUT}	Output Capacitance		7	10	pF	V_{OUT} = +5.0 V f = 1 MHz

SWITCHING CHARACTERISTICS

Guaranteed Limits $T_A = +25°C$, $V_{CC} = +5V$ (8) ; $V_{DD} = -7V \pm 5\%$, $V_D = -10V \pm 5\%$ except as noted.

READ CYCLE			WRITE CYCLE		
SYMBOL	TEST	LIMITS (μsec) MAX	SYMBOL	TEST	LIMITS (μsec) MIN.
t_a	Access Time	1.0μsec	t_{WD}	Address to Write Pulse Delay	0.3
			t_{WP}	Write Pulse Width	0.4
t_a(5)	Access Time	1.0μsec	t_W	Write Time	0.3
			t_{DO}	Data-Write Pulse Overlap	0.1

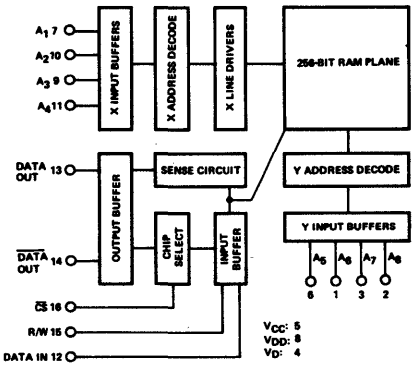
TEST SETUP FOR SPEED MEASUREMENT



NOTES:

1. Each clock time is split into a Read followed by a Write. Read and Write times can be varied by adjustment of the "delay" and "width" controls of the pulse generator.
2. Data generator produces a 256-bit block of data, 32 bits repeated 8 times. "PCM" mode used so data can be changed in 32 bits of the 2501 from one cycle to the next.
3. All inputs to the 2501 are standard TTL outputs with V_{CC} = +5V ±5%.
4. Access time is measured between A1 (least significant address input) and points 1 and 2.
5. $V_{DD} = V_D = -9V$

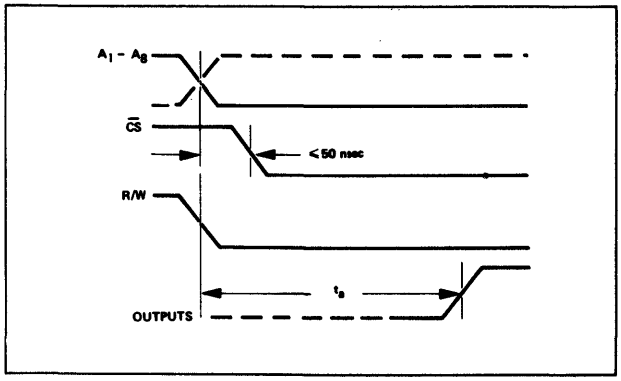
BLOCK DIAGRAM



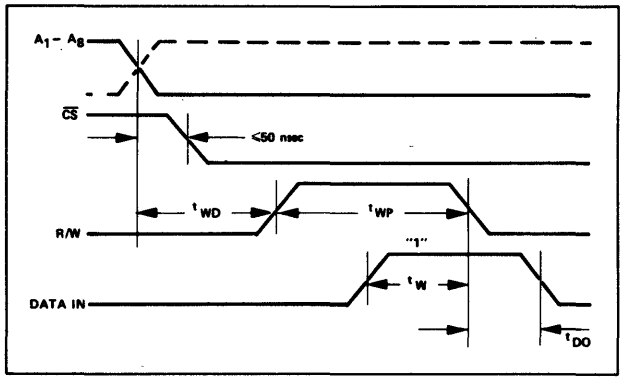
CONDITIONS OF TEST

Input pulse amplitudes: 0 to +5V, Input pulse rise and fall times: < 10 nsec. Speed measurements referenced to 1.5V levels. Output load is 1 TTL gate; measurements made at output of TTL gate ($t_{pd} \leq 10$ nsec)

READ CYCLE (For Measurement Purpose Only)

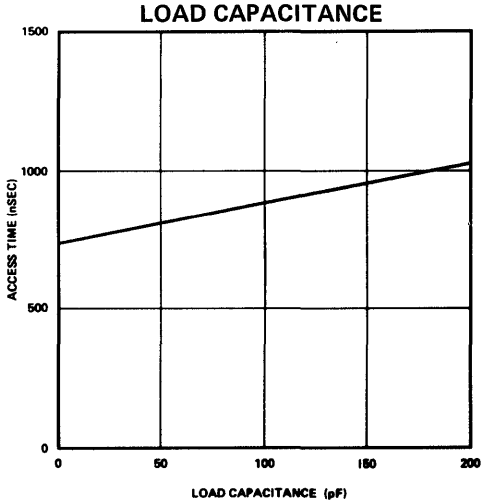


WRITE CYCLE (For Measurement Purpose Only)

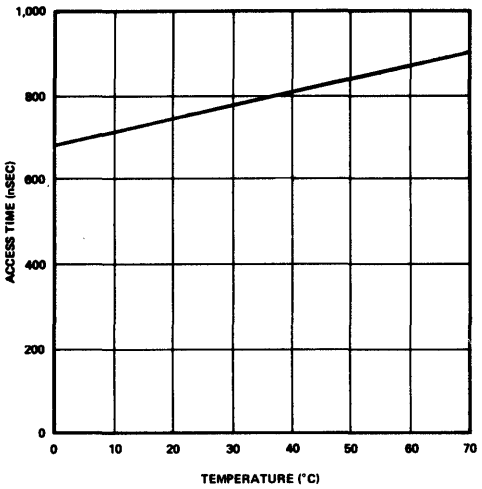


TYPICAL CHARACTERISTICS [1]

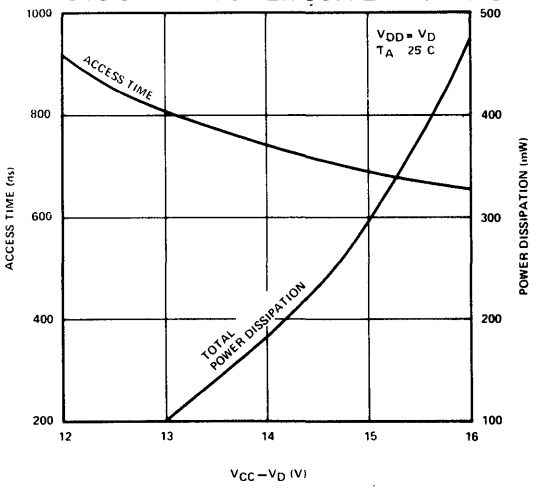
ACCESS TIME VERSUS LOAD CAPACITANCE



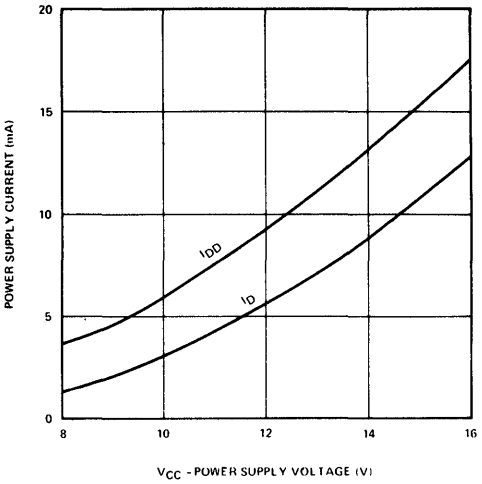
ACCESS TIME VERSUS TEMPERATURE



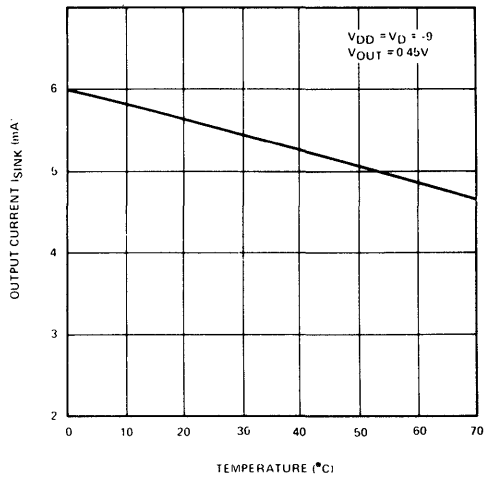
TYPICAL ACCESS TIME AND POWER DISSIPATION VERSUS SINGLE POWER SUPPLY VOLTAGE



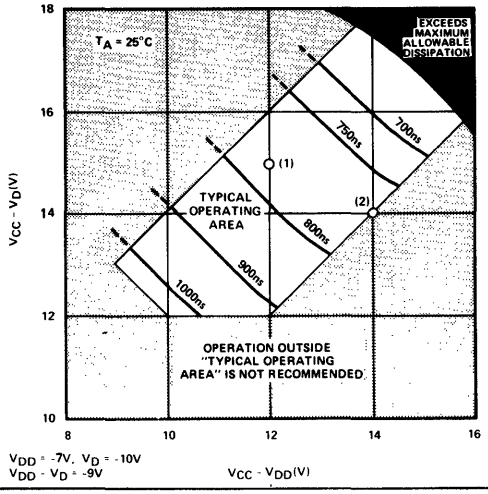
POWER SUPPLY CURRENT VERSUS POWER SUPPLY VOLTAGE



OUTPUT CURRENT VERSUS TEMPERATURE



TYPICAL ACCESS TIME VERSUS SUPPLY VOLTAGES

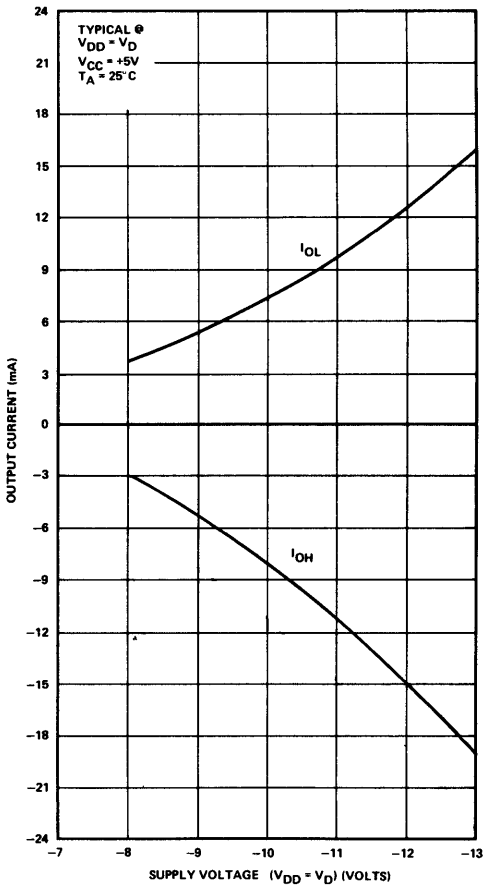


(1) $V_{DD} = -7V$, $V_D = -10V$
(2) $V_{DD} - V_D = -9V$

(1) NOTE: For all typical curves, $V_{CC} = 5V$, $V_{DD} = -7V$, $V_D = -10V$, $T_A = +25°C$ (unless otherwise noted).

TYPICAL CHARACTERISTICS (Cont'd)

OUTPUT CURRENT VERSUS SUPPLY VOLTAGE



APPLICATION INFORMATION

OPERATION

The 2501 is a 256 x 1 Random Access Memory element. It is fully decoded and provides control for Read/Write and Chip Select modes. The operation of this element is described below.

ADDRESSING

An 8-bit address code will select any one of 256 bits for either Read or Write operation. All address input logic levels are compatible with standard bipolar TTL or DTL logic levels.

READ

A logic "0" level (∿0V) applied to the R/W control will result in a Read operation. This can be presented to the R/W control simultaneously or before application of an address code. In this mode the information from the memory will be available on the outputs less than 1μsec later than the application of an address code. Note that there is no need to re-write the data into the memory after a read operation since the read is non-destructive.

WRITE

A "Write" command is a logic "1" (⩾+3.3V) level to the R/W control. This should be presented to the chip no sooner than 300 nsec after the application of an address code. This time delay is necessary for proper address decoding. This "Write" command has to be present for at least 400 nsec to insure that the information is written into the memory. The "Write" command should be off (i.e., memory should be in "Read" mode) by the time the address code is changed. The input data should be present for at least the last 300 nsec of the "Write" command.

CHIP SELECT

The memory array is inhibited with the application of a logic "1" (⩾+3.3V) to the Chip Select control. This will render both R/W and Data Input leads ineffective and will stop information transfer through the output buffer. The address decoder, however, will not be inhibited. This feature allows an effective increase in memory speed. (See below) The output leads are open while the memory array is inhibited. This allows OR-Tying of many memory arrays.

RANDOM ACCESS MEMORY

Arbitrary size memories can be built by tying appropriate numbers of 2501's together. Figure 1 shows a block diagram of a memory system containing 256 N words by M bits. For example, if the memory size were 4096 words by 12 bits, N = 16 and M = 12. Thus the number of 2501's required is M x N = 192. The address inputs A_1 through A_8 are common to all the rows. Inputs C_1 through C_n provide the column select and are wired to the Chip Select inputs of the 2501's. For the example of the 4096 word memory, a 12-bit address must be specified. The first 8 bits would drive inputs A_1 through A_8 directly. The remaining 4 bits would have to be decoded externally into the 16 lines required for the 16 columns. A block diagram of the 4096 x 12 memory is shown in Figure 2. Any number of 2501's can be OR-tied together, however, access time is affected by capacitive loading (approximately 1 nsec/pF). Each 2501 output represents 7 pF (typical) of loading, but the amount of stray capacitance contributed by the printed circuit board wiring can vary greatly and must be determined for each application. Figure 3 shows two different bit line organizations where the capacitive load that must be driven by the 2501 is reduced by employing logic gates to perform the OR-ing function. The organization of Figure 3b results in the minimum load capacitance but requires more gates per bit line than other organizations.

SEQUENTIAL MEMORY

On applications such as program memory or table lookup, where memory operations are highly sequential, but non-synchronous, the memory may be organized for a faster

SEQUENTIAL MEMORY (Cont'd)

average memory cycle than in the true random access case. This involves using the fact that access may be made through the chip select input in 0.2 μsec (typically) where a typical access time if one of the address inputs (A_1-A_8) changes, is 0.8 μsec. For the case of the 4096 word memory organized in this fashion information can be read out at an average access time of 0.25 μsec since access is made through the Chip Select input 15/16 of the time.

LOW POWER OPERATION

Another feature of this memory element is its capability of operating at very low standby power levels. The only time the element has to dissipate full power (~1.6mW/bit) is when it is exercised by either "Write" or "Read" operation. In the standby mode, when the chip will only store information, but does not need to be accessed, the peripheral power supply (V_D) is completely shut off. This will immediately cut the total power drain by a factor of 1.5.

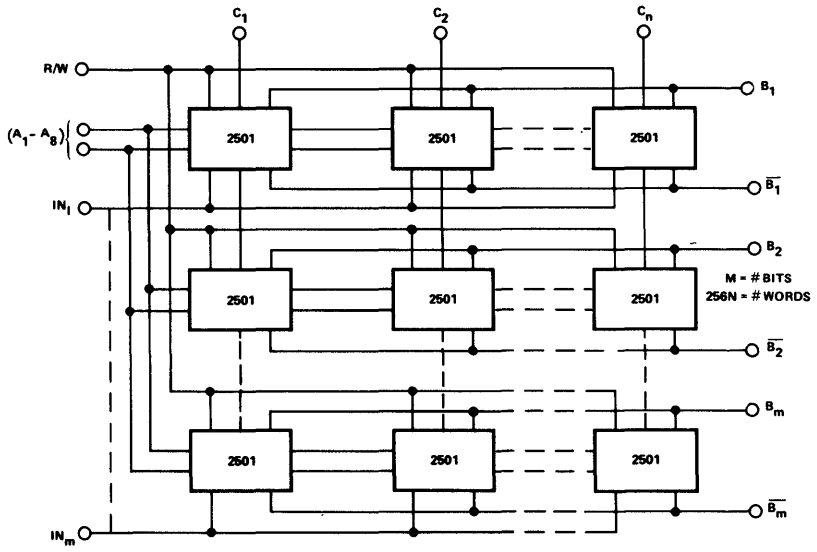


FIGURE 1. ORGANIZATION OF 2501's INTO LARGER MEMORY

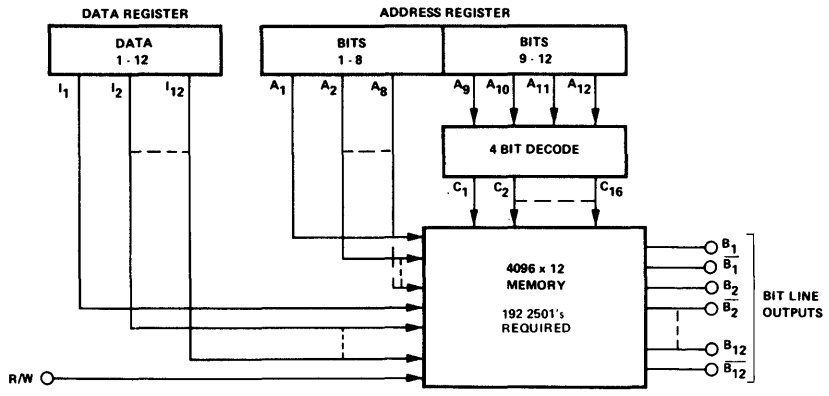
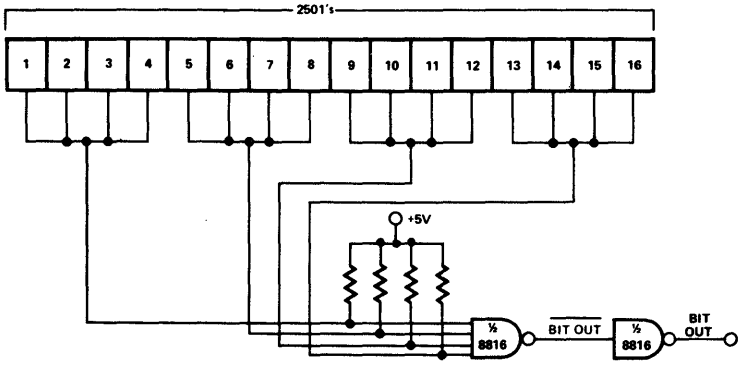
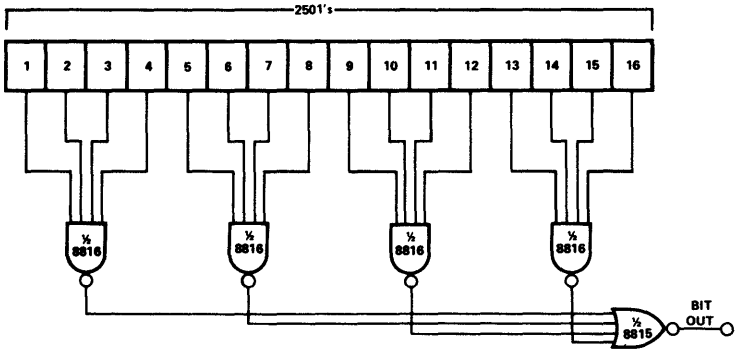


FIGURE 2. ORGANIZATION OF 4096 WORD BY 12-BIT MEMORY



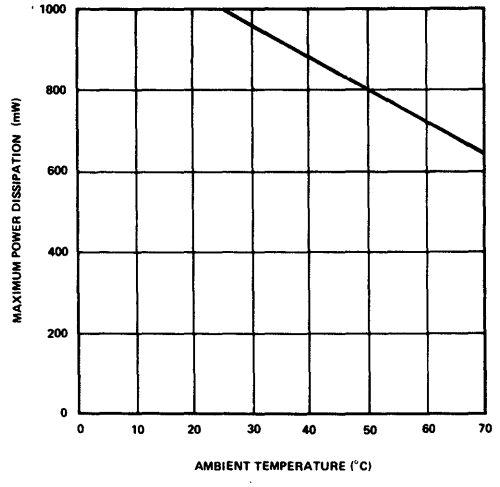
a. Combination of wire-ORing and logic-ORing of 2501's



b. Logic-ORing of 2501's

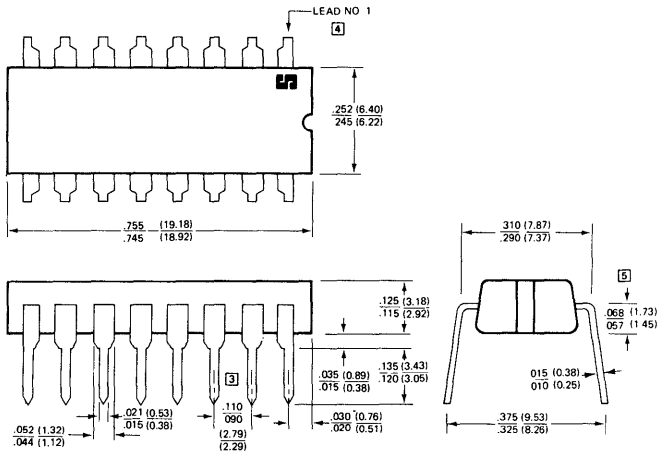
FIGURE 3. BIT LINE ORGANIZATIONS TO MINIMIZE CAPACITIVE LOAD—4096 WORDS

PACKAGE MAXIMUM POWER DISSIPATION



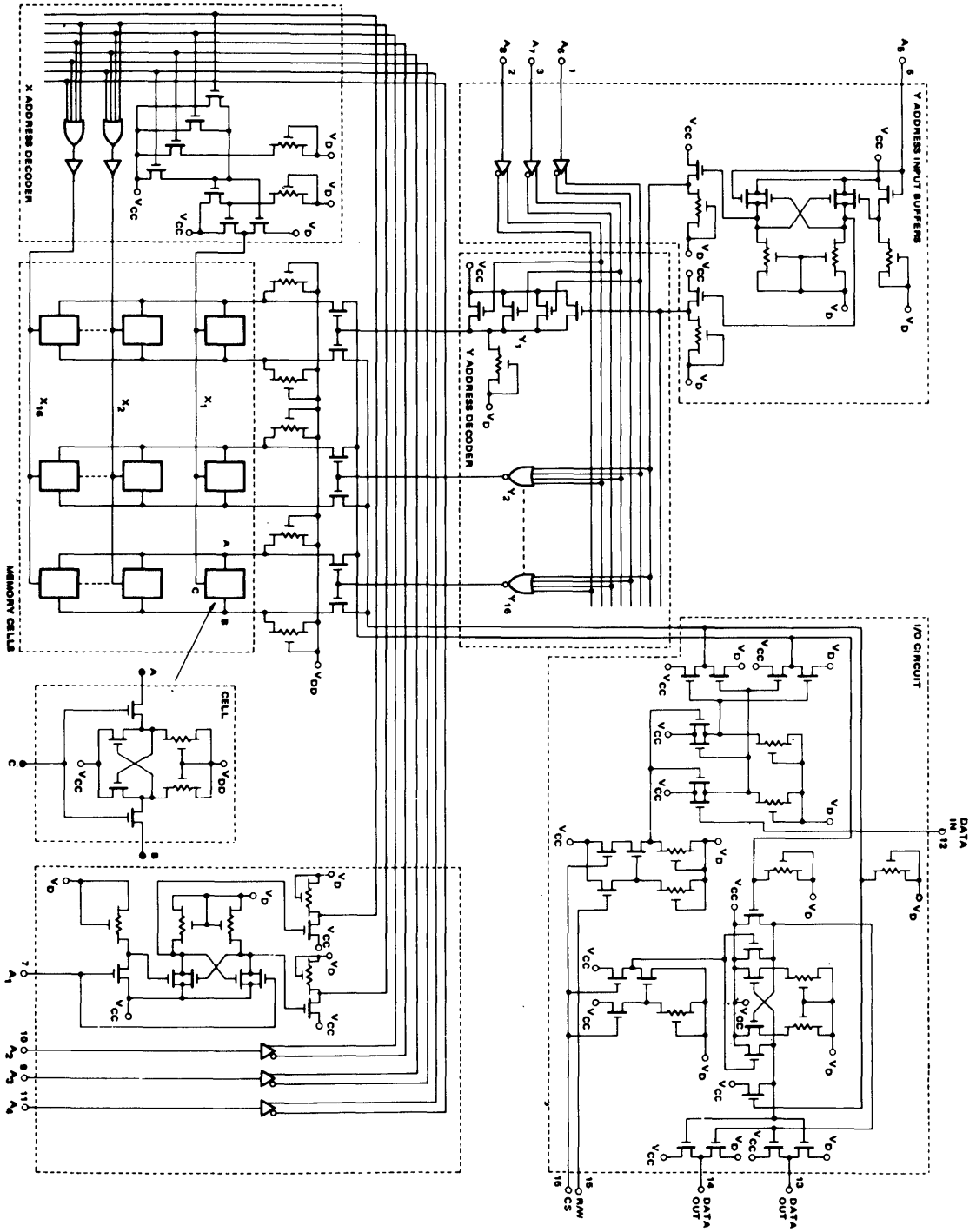
PACKAGE INFORMATION

B PACKAGE



NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: SILICONE MOLDED.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: Θ Ja = .16°C/mW, Θ Jc = .08°C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

CIRCUIT SCHEMATIC



Signetics 2501 256 X 1 Static Random Access Memory

1024 BIT CAPACITY MULTIPLEXED DYNAMIC SHIFT REGISTERS

SILICON GATE MOS 2500 SERIES

2502
2503
2504

DESCRIPTION

These Signetics 2500 Series 1024-bit multiplexed dynamic shift registers consist of enhancement mode P-channel MOS devices integrated on a single monolithic chip. Due to on-chip multiplexing, the data rate is twice the clock rate.

FEATURES

- 10 MHz TYPICAL DATA RATE
- THREE CONFIGURATIONS–QUAD 256, DUAL 512, SINGLE 1024
- LOW POWER DISSIPATION–40 μW/bit at 1 MHz DATA RATE
- LOW CLOCK CAPACITANCE–140 pF
- TTL, DTL COMPATIBLE
- STANDARD PACKAGES - 8 LEAD TO-99, 8-PIN AND 16-PIN SILICONE DUAL IN-LINE PACKAGE
- SIGNETICS P-MOS SILICON GATE PROCESS AND SILICONE PACKAGING TECHNOLOGIES

APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST BUFFER MEMORIES
CRT REFRESH MEMORIES
DELAY LINE MEMORY REPLACEMENT

PROCESS TECHNOLOGY

Use of low threshold *silicon gate technology* allows high speed (10 MHz typical) while reducing power dissipation and clock input capacitance dramatically as compared to conventional technologies.
The use of low voltage circuitry minimizes power dissipation and facilitates interfacing with bipolar integrated circuits.

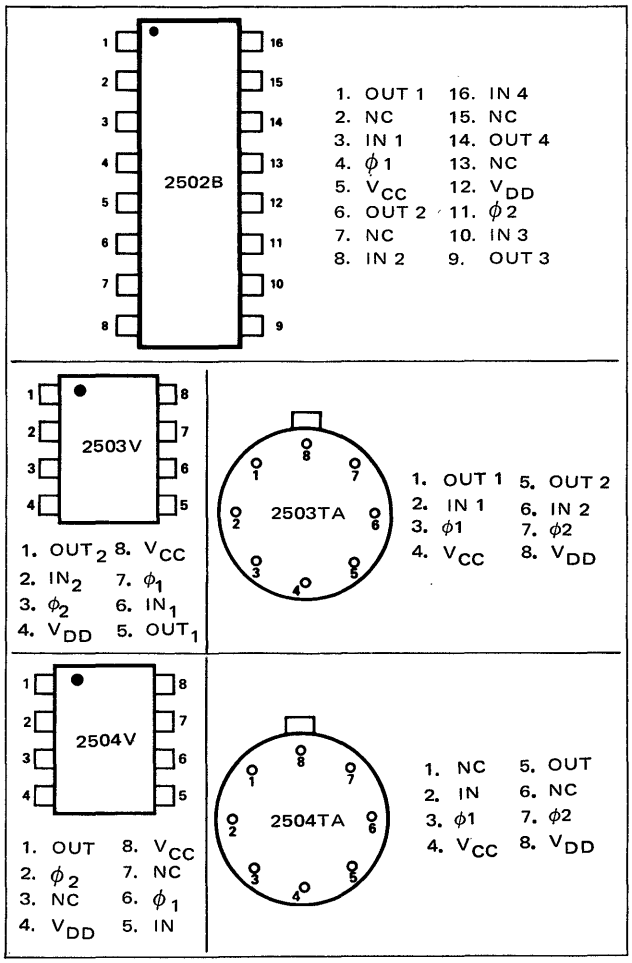
SILICONE PACKAGING

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process, the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric material over the silicon gate-oxide-substrate structure provides an ion barrier. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability and demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers.

BIPOLAR COMPATIBILITY

The data inputs of these registers can be driven directly by standard bipolar integrated (TTL, DTL, etc.) or by MOS circuits. The bare drain output stage provides driving capability for both MOS and bipolar integrated circuits (one standard TTL load).

PIN CONFIGURATIONS (Top View)



PART IDENTIFICATION TABLE

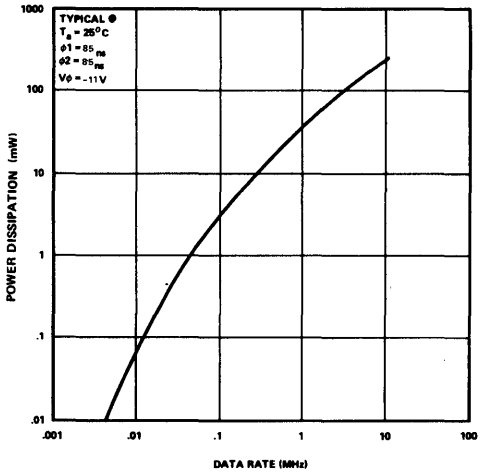
TYPE	FUNCTION	PACKAGE
2502B	Quad 256-bit	16-Pin DIP
2503TA	Dual 512-bit	TO-99
2503V	Dual 512-bit	8-Pin DIP
2504TA	Single 1024-bit	TO-99
2504V	Single 1024-bit	8-Pin DIP

MAXIMUM SIGNETICS GUARANTEED RATINGS(1)

Operating Ambient Temperature(2)	0°C to +70°C
Storage Temperature	-65°C to + 150°C
Power Dissipation(2) at T_A = 70°C	
TA and V Package	535mW
B Package	640mW
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}(3)	+0.3V to -20V

NOTES:
1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W (TA and V package)or 125° C/W (B package).
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserving the right to make design and process changes and improvements.
7. Typical values at +25°C and nominal supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}. V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.

POWER DISSIPATION VERSUS DATA RATE



DC CHARACTERISTICS

T_A = 0°C to +70°C; V_{DD} = -5V ±5%; V_{CC} = +5V(8) unless otherwise noted. (See Notes 4,5,6,7).

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} = V_{CC} to V_{DD}, T_A = 25°C
I_{LO}	Output Leakage Current		10	1000	nA	$V_{\phi1}$ = $V_{\phi2}$ = -10V V_{OUT} = 0.0V, T_A = 25°C
I_{LC}	Clock Leakage Current		10	1000	nA	V_{ILC} = -10V , T_A = 25°C
I_{DD}	Power Supply Current		15	25	mA	Outputs at logic "0", 4 MHz data rate, $\phi1$ = $\phi2$ = 85ns continuous operation, V_{ILC} = -12V T_A = 25°C
V_{IL}	Input "Low" Voltage			1.05	V	
V_{IH}	Input "High" Voltage	3.2		5.3	V	
V_{IHC}	Clock Input "High" Voltage	4.0		5.3	V	
V_{ILC}	Clock Input "Low" Voltage	-10		-12	V	

AC CHARACTERISTICS

$T_A = 25°C$, $V_{DD} = -5V \pm 5\%$; $V_{CC} = +5V$ (8) ; $V_{ILC} = -11V$, (See notes 4, 5, 6, 7).

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
Frequency	Clock Rep Rate	0.0005		4	MHz	
Frequency	Data Rep Rate	0.001		8	MHz	
ϕpw	Clock Pulse Width	85			ns	
ϕd	Clock Pulse Delay	10			ns	
t_r, t_f	Clock Pulse Transition	10		1000	ns	
t_w	Data Write Time (Setup)	50			ns	
t_{DO}	Data in Overlap	10			ns	
t_a+	Data Out			90	ns	
C_{IN}	Input Capacitance	2.5		5	pF	@ 1 MHz 25 mV p-p
C_{OUT}	Output Capacitance	2.5		5	pF	@ 1 MHz 25 mV p-p
Cϕ	Clock Capacitance	130		150	pF	@ 1 MHz 25 mV p-p
V_{OL}	Output "Low" Voltage		-0.3		V	R_L=3k, depends on R_L and TTL Gate
V_{OH1}	Output "High" Voltage Driving MOS	3.6	4.0		V	R_L = 5.6k
V_{OH2}	Output "High" Voltage Driving TTL	3.0	3.5		V	R_L = 3k

MULTIPLEXED 4-BIT MOS SHIFT REGISTER

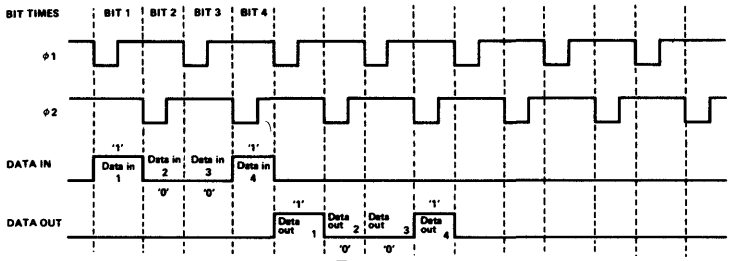


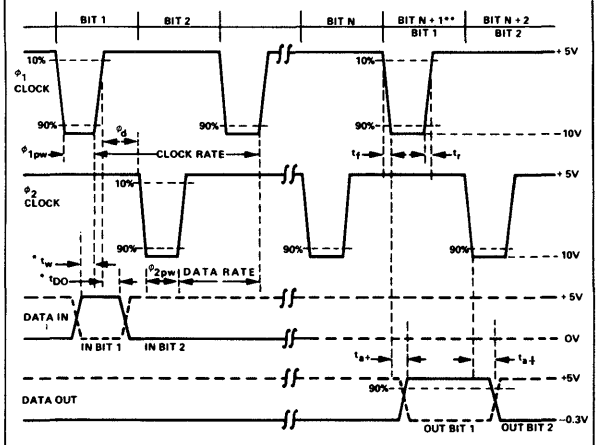
Figure 1

Figure 1 is a simplified illustration of the timing of a 4-bit multiplexed register showing input output relationships with respect to the clock. If data enters the register at ϕ1 time, it exits at ϕ1 time, (beginning on ϕ1's negative going edge and ending on the succeeding ϕ2's negative going edge).

CONDITIONS OF TEST

Input rise and fall times: 10nsec. Output load is 1 TTL gate.

TIMING DIAGRAM

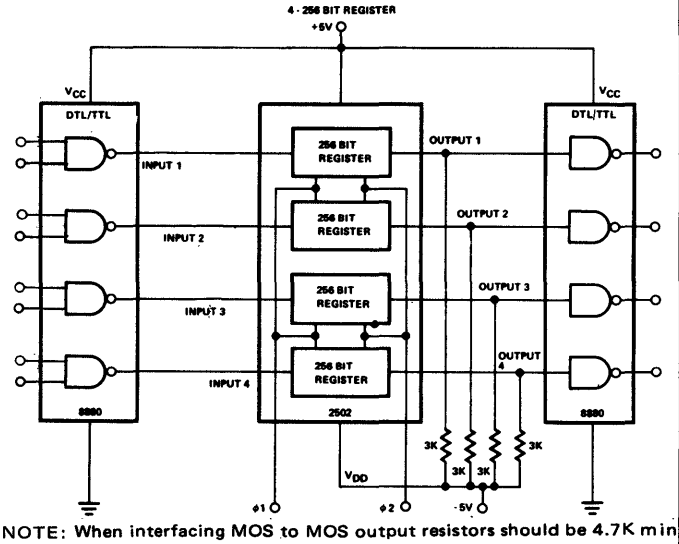


* t_W and t_{DO} same for ϕ 2

** N=256 for 2502, N = 512 for 2503, N = 1024 for 2504

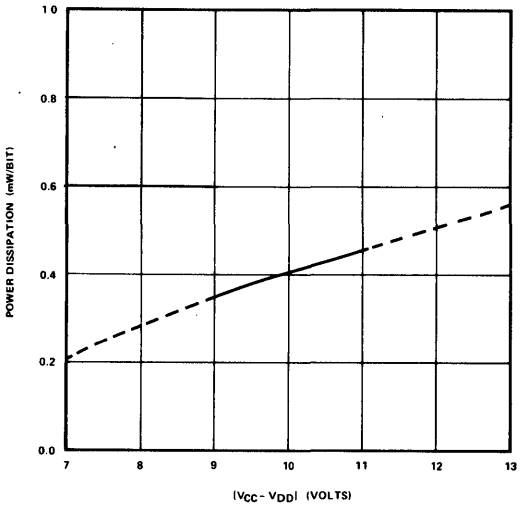
APPLICATIONS INFORMATION

DTL/TTL/MOS INTERFACES

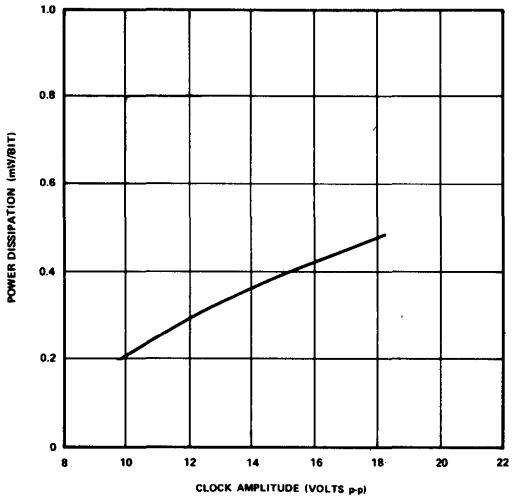


NOTE: When interfacing MOS to MOS output resistors should be 4.7K min

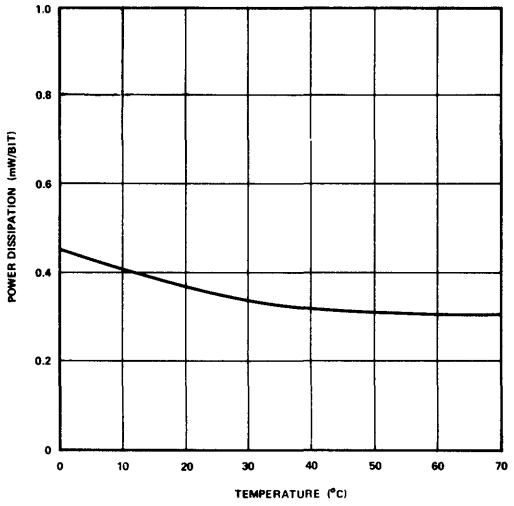
POWER DISSIPATION/BIT VERSUS SUPPLY VOLTAGE



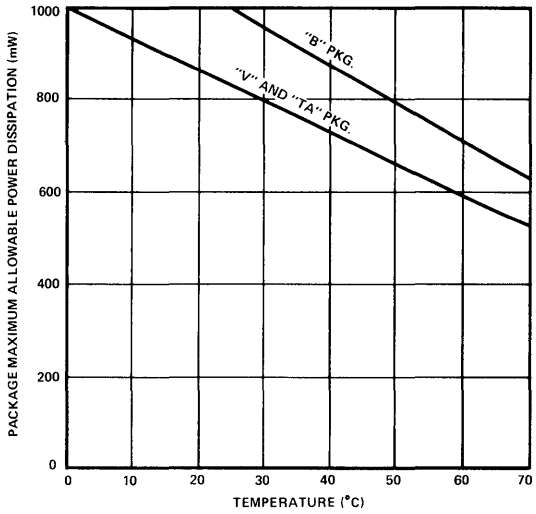
POWER DISSIPATION/BIT VERSUS CLOCK AMPLITUDE



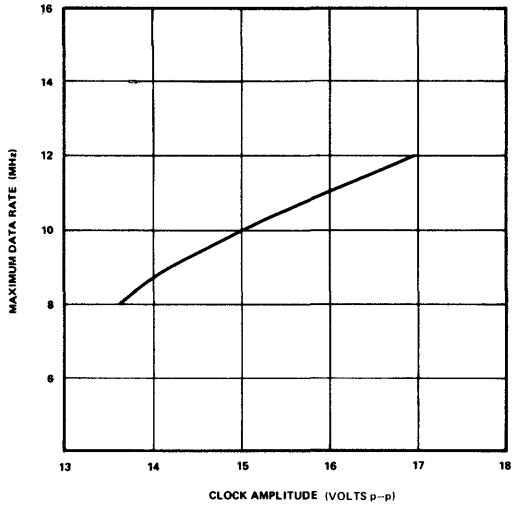
POWER DISSIPATION/BIT VERSUS TEMPERATURE



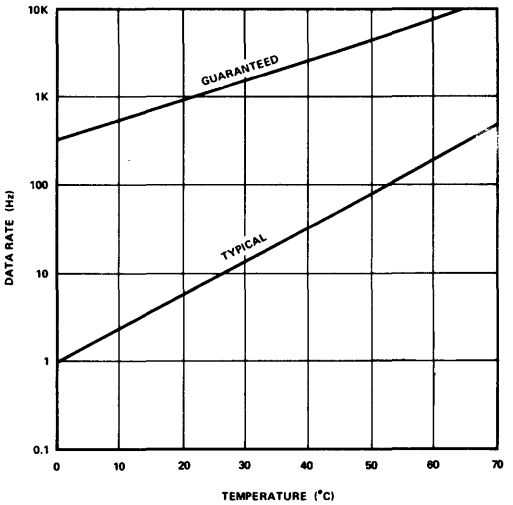
MAXIMUM ALLOWABLE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



CLOCK AMPLITUDE V_ϕ VERSUS MAXIMUM DATA RATE



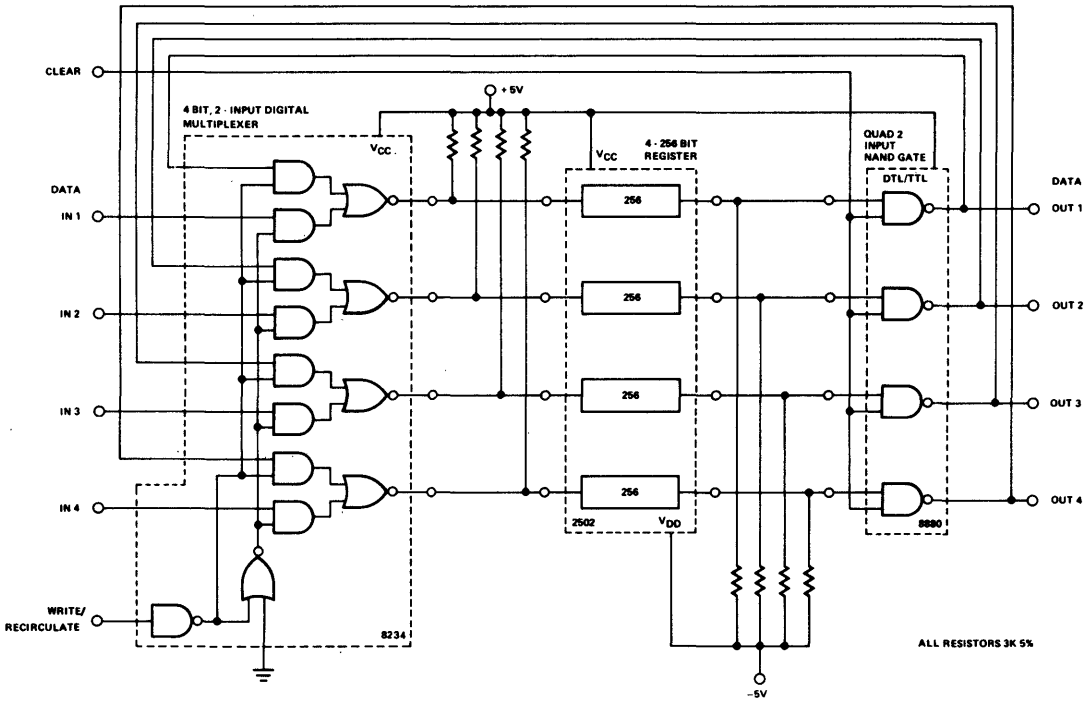
MINIMUM OPERATING DATA RATE VERSUS TEMPERATURE



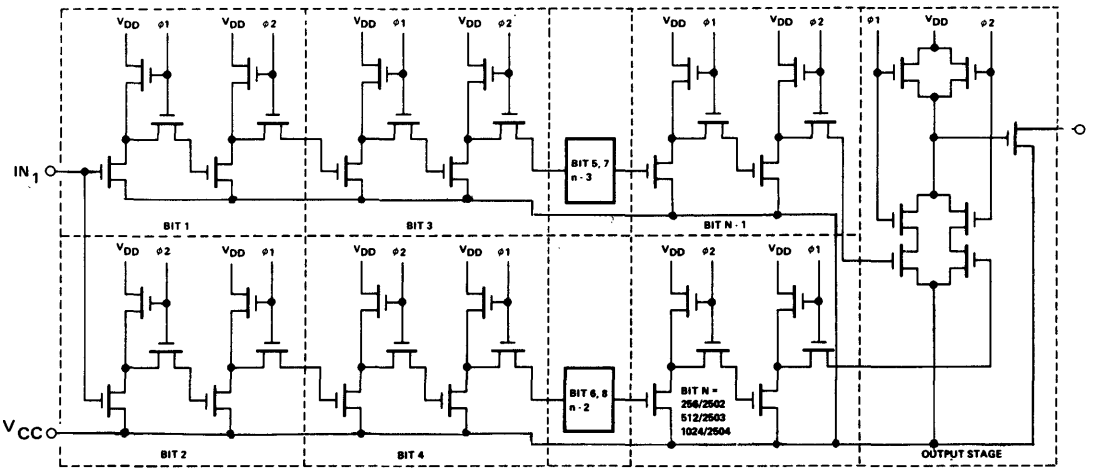
NOTE:
Conditions for Typical Curves; V_{CC} = +5V, V_{DD} = -5V, ϕ_{1PW} and ϕ_{2PW}=85ns, V_ϕ =-11V, T_A=25°C, f_{DATA}=10MHz unless otherwise noted.

APPLICATIONS (Cont'd)

WRITE/RECIRCULATE LOGIC



CIRCUIT SCHEMATIC

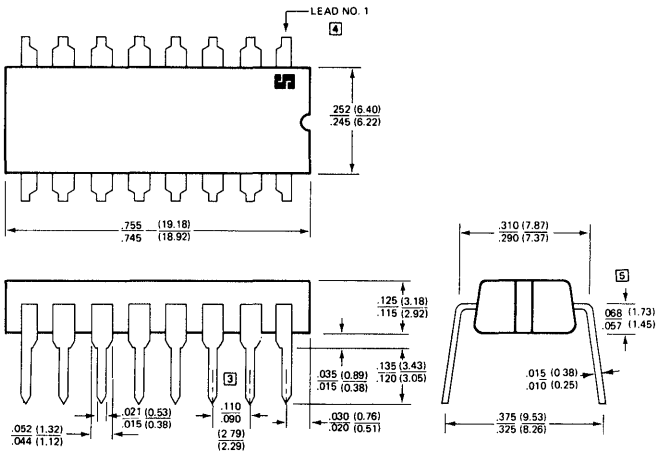


NOTES:

1. N = 1024 on 2504
2. N = 512 on 2503 schematic for second register same as above.
3. N = 256 on 2502 schematic for second, third and fourth registers same as above.

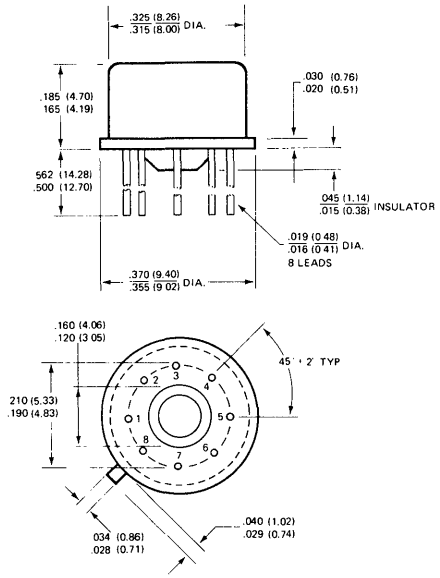
PACKAGE INFORMATION

B PACKAGE



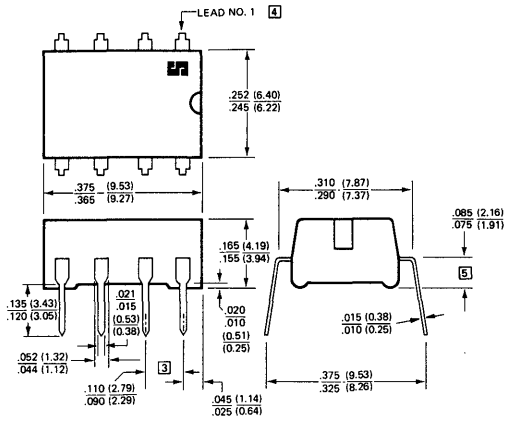
NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: SILICONE MOLDED.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: Θ Ja = .16° C/mW, Θ Jc = .08° C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

T PACKAGE



NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED.
2. BODY MATERIAL: EYELET, KOVAR OR EQUIVALENT, GOLD PLATED, GLASS BODY.
3. LID MATERIAL: NICKEL, WELD SEAL.
4. THERMAL RESISTANCE FROM JUNCTION TO CASE, Θ Ja = .150 C/mW, Θ Jc = .025 C/mW.
5. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

V PACKAGE



NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: SILICONE MOLDED.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: Θ Ja = .16 C/mW, Θ Jc = .08 C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

512 AND 1024 BIT RECIRCULATING DYNAMIC SHIFT REGISTERS

2505
2512

SILICON GATE MOS 2500 SERIES

DESCRIPTION

These Signetics 2500 Series 512 and 1024 bit recirculating dynamic shift registers consist of enhancement mode P-channel MOS devices integrated on a single monolithic chip. Internal recirculation logic plus write and read controls, together with two chip select controls are included on the chip.

FEATURES

- HIGH FREQUENCY OPERATION–3 MHz TYPICAL CLOCK RATE
- SINGLE 512, SINGLE 1024
- TTL, DTL COMPATIBLE
- 2-CHIP SELECT CONTROLS FOR XY MATRIX SELECTION
- WRITE AND READ CONTROLS INCLUDED
- LOW POWER DISSIPATION–150μW/bit at 1 MHz
- LOW CLOCK CAPACITANCE–80pF for 512, 160pF for 1024 Bits
- +5, -5V POWER SUPPLIES
- STANDARD PACKAGE–10 LEAD TO-100
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

FAST ACCESS SWAPPING MEMORY SYSTEMS
LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST BUFFER MEMORIES
CRT REFRESH MEMORIES
DELAY LINE MEMORY REPLACEMENT
DRUM MEMORY REPLACEMENT

PROCESS TECHNOLOGY

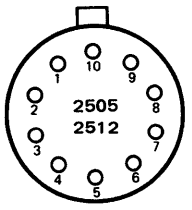
Use of low threshold *silicon gate technology* allows high speed (3MHz typical) while reducing power dissipation and clock input capacitance dramatically as compared to other technologies. The use of low voltage circuitry minimizes power dissipation and facilitates interfacing with bipolar integrated circuits.

BIPOLAR COMPATIBILITY

The signal inputs of these registers can be driven directly by standard bipolar integrated (TTL, DTL, etc.) or by MOS circuits. The bare drain output stage provides driving capability for both MOS and bipolar integrated circuits (one standard TTL load).

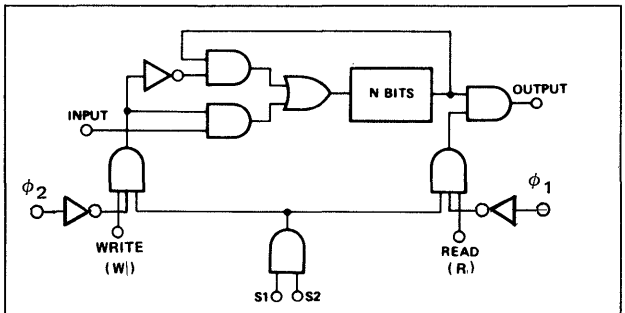
PIN CONFIGURATION (Top View)

K PACKAGE



1. Select 1
2. Write
3. Input
4. ϕ_1 Output Clock
5. V_{CC}
6. ϕ_2 Input Clock
7. Output
8. Read
9. Select 2
10. V_{DD}

BLOCK DIAGRAM



NOTES:
N = 512 or 1024 '0' = 0V, '1' = +5V.
When S1 or S2 is '0' Data Recirculates
When S1 and S2 are '1' see truth table

TRUTH TABLE

WRITE	READ	FUNCTION
0	0	Recirculate, Output is '0'
0	1	Recirculate, Output is Data
1	0	Write Mode, Output is '0'
1	1	Read/Write, Output is Data

PART IDENTIFICATION TABLE

PART NO.	BIT LENGTH	PACKAGE
2505K	512	10 pin TO - 100
2512K	1024	10 pin TO - 100

MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature (2)	0°C to +70°C
Storage Temperature	65°C to +150°C
Power Dissipation (2)	535mW@T_A>70°C
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}	+0.3V to −20V

NOTES:

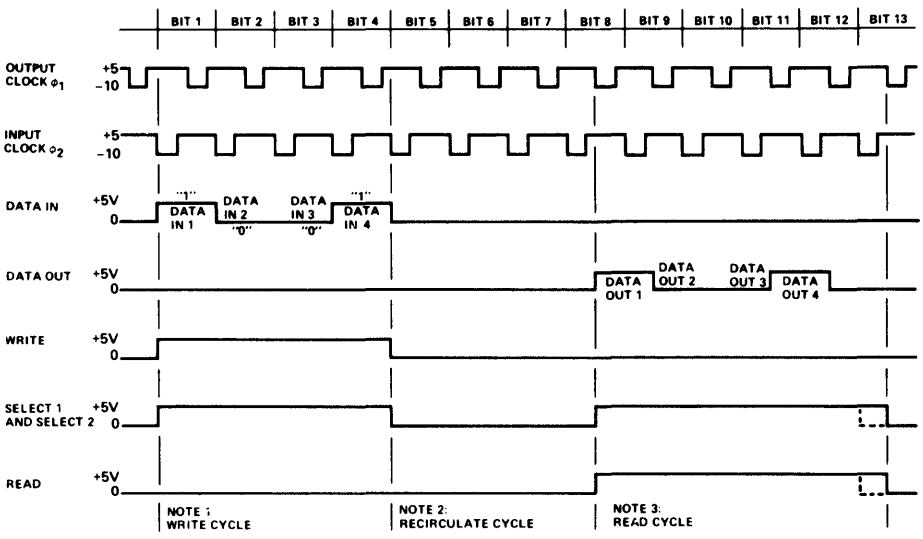
1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
3. All inputs are protected against static charge.
4. See "Minimum Operating Frequency" graph for low limits on data rep. rate.
5. Parameters are valid over operating temperature range unless otherwise specified.
6. All voltage measurements are referenced to ground.
7. Manufacturer reserves the right to make design and process changes and improvements.
8. Typical values are at +25°C and nominal supply voltages.
9. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.
10. V_{OL} is a function of the input characteristics of the driven TTL/DTL gate I_{OI} and V_{CLAMP} and the value of the pull-down resistor (R_L).

DC CHARACTERISTICS $T_A = 0°C$ to $+70°C$; $V_{CC} = +5V$ (9) ; $V_{DD} = -5V$ ±5% unless otherwise noted.

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	$V_{IN} = -5.5V$; $T_A = 25°C$
I_{LO}	Output Leakage Current		10	1000	nA	$V_{\phi1} = V_{\phi2} = -12V$, $V_{DD} = -5V$; $V_{OUT} = -5.5V$; $T_A = 25°C$
I_{LC}	Clock Leakage Current		10	1000	nA	$V_{ILC} = 12V$; $T_A = 25°C$
I_{DD}	Power Supply Current: 2505		15	25	mA	Continuous Operation; ϕ pW = 150nS, 1MHz
	2512		25	35	mA	$V_{ILC} = -12V$; $T_A = 25°C$ $V_{DD} = -5.5V$
V_{IL}	Input "Low" Voltage	-5.0		1.05	V	
V_{IH}	Input "High" Voltage	3.2		5.3	V	
V_{ILC}	Clock Input "Low" Voltage	-12.0		-10.0	V	
V_{IHC}	Clock Input "High" Voltage	4.0		5.3	V	

TIMING DIAGRAM

4-BIT RECIRCULATING SHIFT REGISTER



NOTE 1: (WRITE cycle)

The positive and negative going edge of the " W ", "S1", "S2" controls are coincident with the negative going edge of the input clock (ϕ_2). The "Read" control may be either "1" or "0".

NOTE 2: (RECIRCULATE cycle)

Data recirculates if one or more of the following control lines are "0"; S1, S2 and W . Read may be either "1" or "0"

NOTE 3: (READ cycle)

The positive going edge of the "Read", "S1", "S2" controls are coincident with the negative edge of the output clock (ϕ_1). The negative going edge of R, S1, S2 is coincident with the negative going edge of either clock pulse succeeding the last desired data output bit. W may be either "1" or "0".

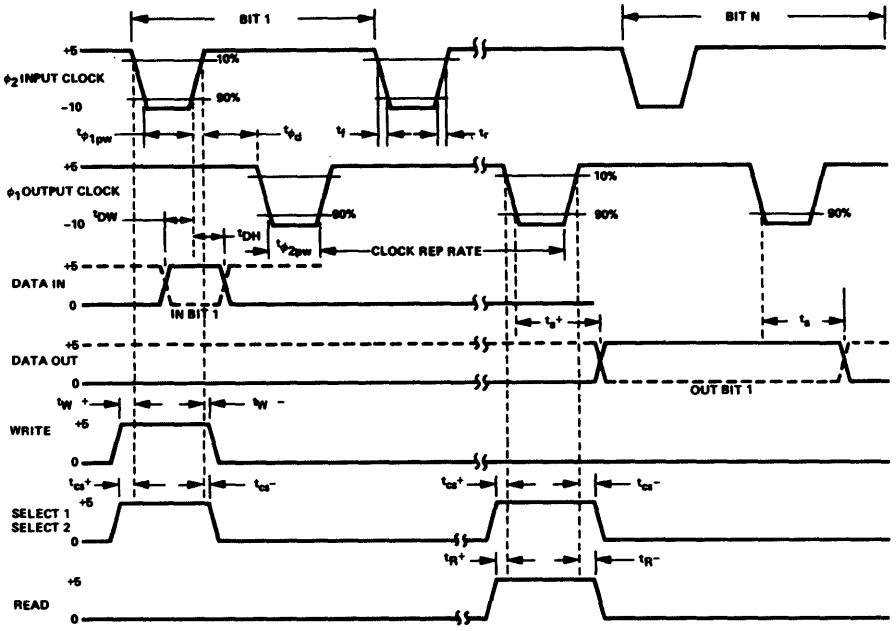
Figure 1

Figure 1 is a simplified illustration of the timing of a 4-bit recirculating shift register showing the 3 basic modes of operation.

CONDITIONS OF TEST

Input rise and fall times: 10 nsec Output load is 1 TTL gate

TIMING DIAGRAM



NOTE:

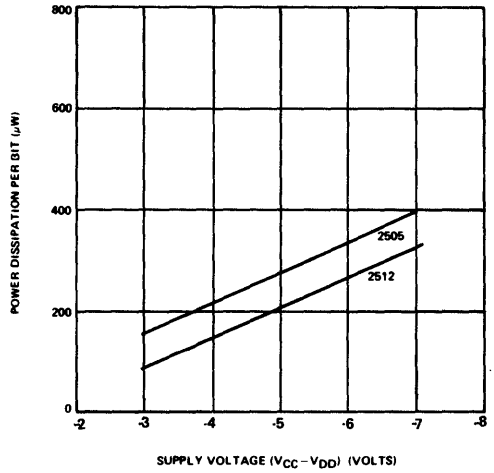
1. N=512 for 2505, N=1024 for 2512
2. Note that the Read Input is AND'ed with $\overline{\phi_1}$; therefore this function is not valid until ϕ_1 occurs.

AC CHARACTERISTICS T_A=+25°C V_{CC}=+5V (9); V_{DD}=-5V ± 5%; V_{ILC}=-11V

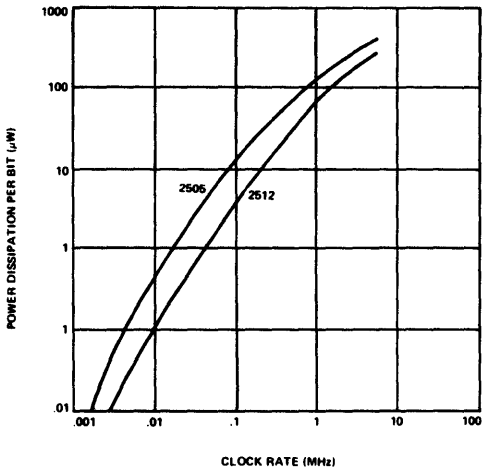
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
Frequency	Clock Data Rep Rate	.0005 (Note 4)	3	2.5	MHz	W = R = V_{CC}
$t_{\phi pw}$	Clock Pulse Width	180			nsec	
$t_{\phi d}$	Clock Pulse Delay	10			nsec	
t_r;t_f	Clock Pulse Transition			1	μsec	
t_{DW}	Data Write (Setup) Time	150			nsec	
t_{DH}	Data to Clock Hold Time	10			nsec	
t_{a+};t_{a-}	Clock to Data Out Delay			100	nsec	
t_{R-};t_{CS-} $t_{W\ -}$	Clock to "Read" or "Chip Select" or "Write" Timing	0			nsec	
t_{R-};t_{CS+} $t_{W\ +}$	Clock to "Read" or "Chip Select" or "Write" Timing	0			nsec	
C_{in}	Input Capacitance			5	pF	1 MHz; V_I=V_{CC}; V_{AC}=25mV_{P-P}
C_{out}	Output Capacitance			5	pF	1 MHz; V_O=V_{CC}; V_{AC}= 25mV_{P-P}
C_ϕ	Clock Capacitance 2505 2512			50 100	pF pF	1 MHz; V =V_{CC};V_{AC}= 25mV p-p
V_{OL}	Output "Low" Voltage		-1.0		V	R_L = 3.0K; 1 TTL Load (I_L = 1.6mA) Note 10
V_{OH1}	Output "High" Voltage Driving 1 TTL Load	2.4	3.5		V	R_L = 3.0K; 1 TTL Load (I_L = 100μA)
V_{OH2}	Output "High" Voltage Driving MOS	3.6	4.0		V	R_L = 5.6K; C_L = 10 pF

CHARACTERISTICS CURVES

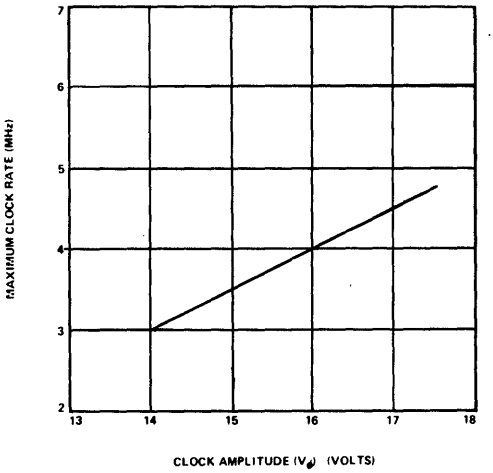
POWER DISSIPATION/BIT VERSUS SUPPLY VOLTAGE



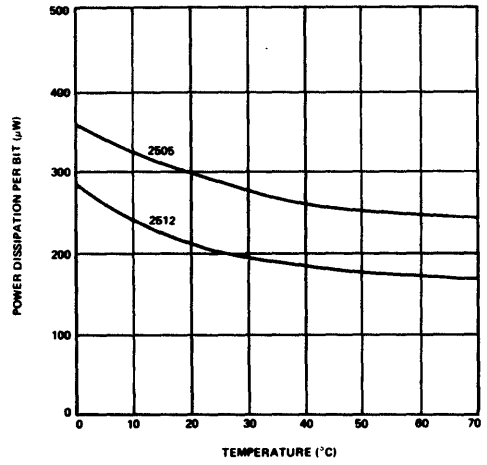
POWER DISSIPATION/BIT VERSUS CLOCK RATE



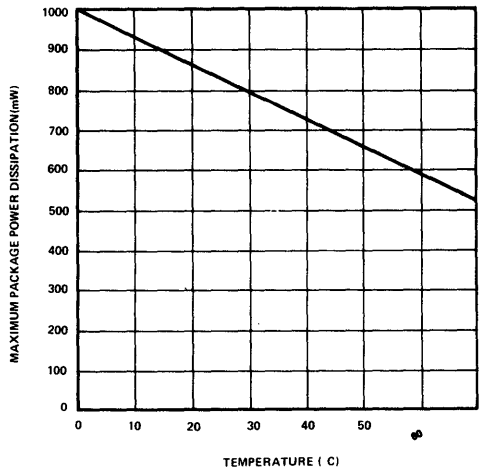
MAXIMUM CLOCK RATE VERSUS CLOCK AMPLITUDE



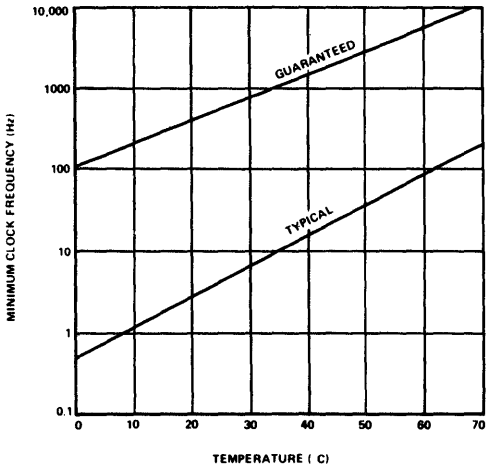
POWER DISSIPATION/BIT VERSUS TEMPERATURE



MAXIMUM PACKAGE POWER DISSIPATION VERSUS TEMPERATURE



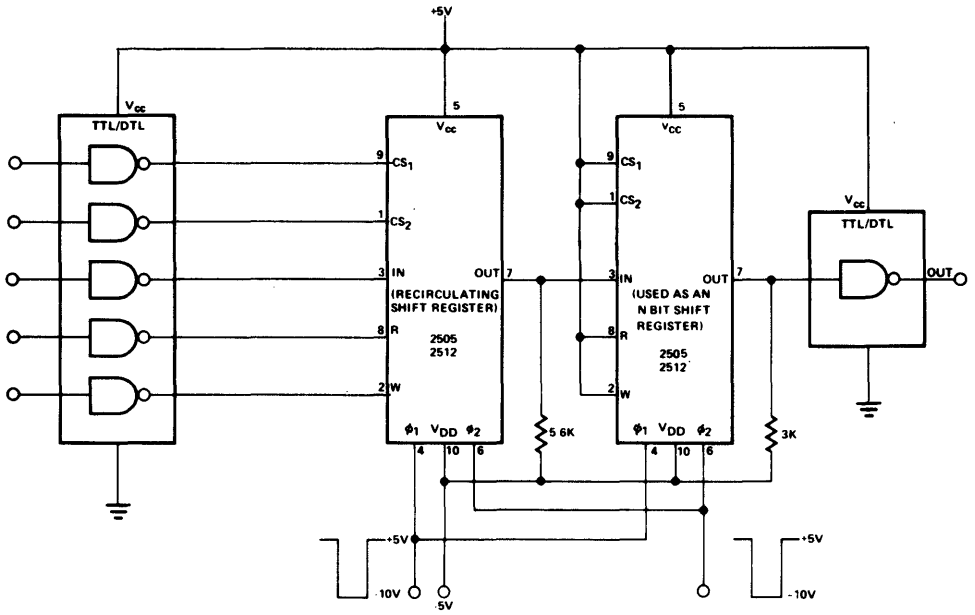
MINIMUM OPERATING CLOCK FREQUENCY



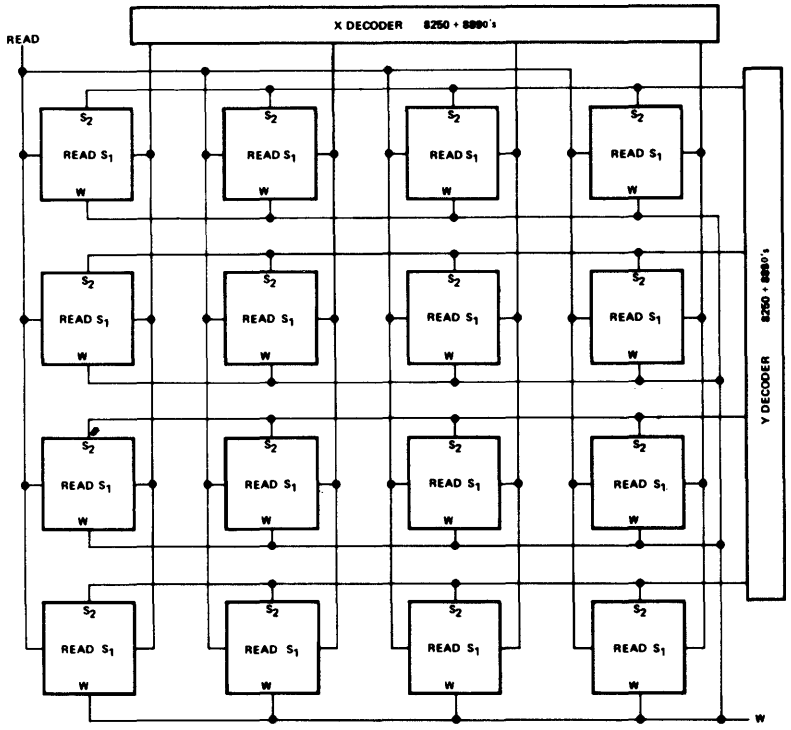
NOTE:
Conditions for Typical Curves = V_{CC}=+5V, V_{DD}=−5V, Clock Duty Cycle=35°C, f_{CLK}=2.5MHz, $V_{\phi p\text{-}p}$=16V, ϕ_{PW} =180ns, T_A=25°C unless otherwise noted

APPLICATIONS DATA

TTL/DTL/MOS INTERFACES

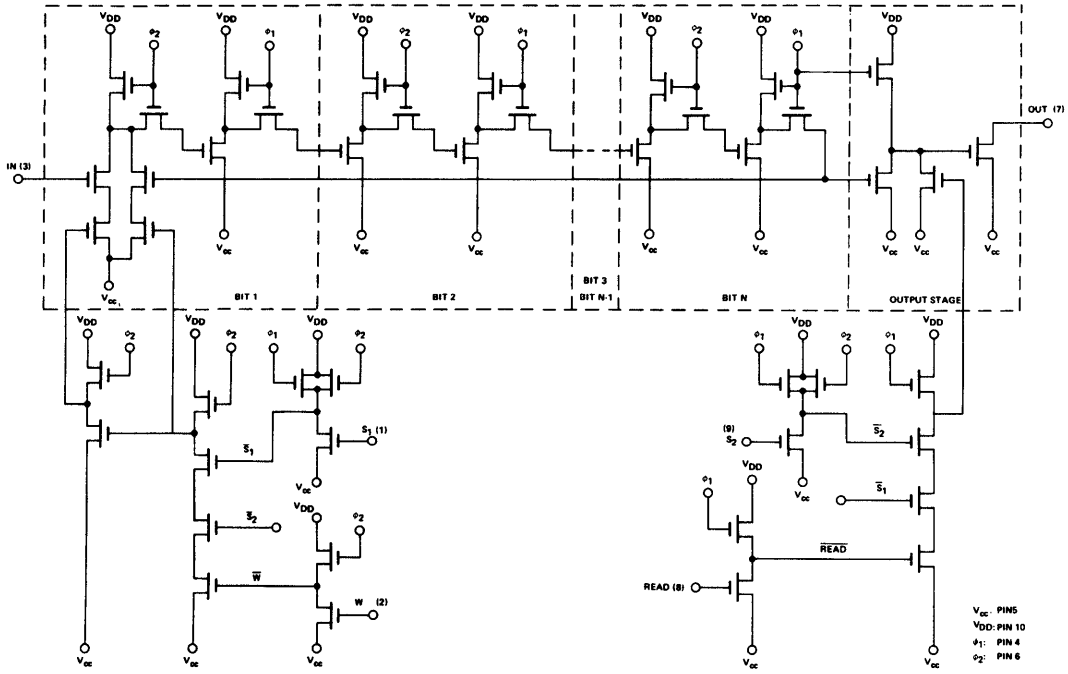


MATRIX CHIP SELECT LOGIC



NOTES:
1. Outputs common for each plane
2. All inputs common for each plane
3. All ϕ_1's common
4. All ϕ_2's common
5. All V_{CC} common
6. All V_{DD} common

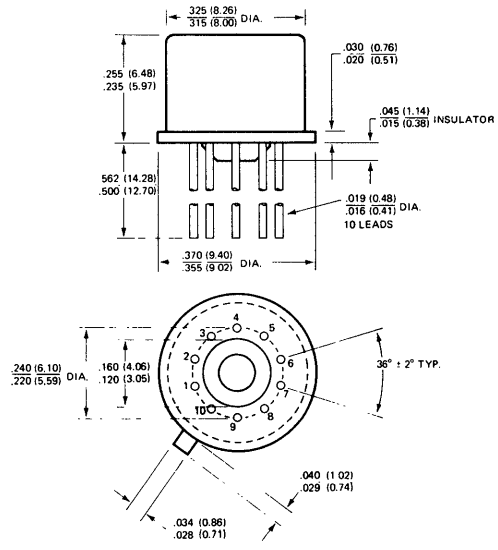
CIRCUIT SCHEMATIC



NOTE: N = 512 for 2505
N = 1024 for 2512

PACKAGE INFORMATION

K PACKAGE



NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED.
2. BODY MATERIAL: CERAMIC WITH KOVAR OR EQUIVALENT.
3. LID MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED, ALLOY SEAL.
4. TOLERANCES NON CUMULATIVE.
5. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
6. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
7. THERMAL RESISTANCE: Θ Ja = .060°C/mW, Θ Jc = .015°C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

DUAL 100-BIT DYNAMIC SHIFT REGISTER

SILICON GATE MOS 2500 SERIES

2506
2507
2517

DESCRIPTION

These Signetics 2500 Series dual 100-Bit dynamic shift registers consist of enhancement mode P-channel MOS devices integrated on a single monolithic chip. They use two clock phases.

FEATURES

- **HIGH FREQUENCY OPERATION**
  4 MHz TYPICAL CLOCK RATE
- **TTL, DTL COMPATIBLE**
- **LOW POWER DISSIPATION — 400 μW/BIT AT 1 MHz**
- **LOW CLOCK CAPACITANCE 40pF MAXIMUM**
- **LOW OUTPUT IMPEDANCE — 300 OHMS TYPICAL**
- **BARE DRAIN AND MOS RESISTOR VERSIONS AVAILABLE**
- **STANDARD PACKAGES — 8 LEAD TO-5 AND 8 LEAD SILICONE DIP**
- **SIGNETICS P-MOS SILICON GATE AND SILICONE PACKAGING TECHNOLOGIES**

APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST BUFFER MEMORIES

PROCESS TECHNOLOGY

Use of the low threshold silicon gate technology allows high speed (3 MHz guaranteed), while reducing power dissipation by a factor of 2 and reducing clock input capacitance dramatically as compared to conventional MOS technologies.

SILICONE PACKAGING

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric material over the silicon gate-oxide-substrate structure provides an ion barrier. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability, demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers. For further information reference Signetics - "Silicone Package Qualification Report".

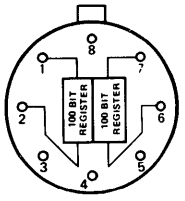
BIPOLAR COMPATIBILITY

The dual 100 bit device can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.) or by MOS circuits. The design of the output stage provides driving capability for MOS or bipolar IC's.

It is available in bare drain configuration or with internal pull down resistor values of 7.5k or 20k to provide easier interfacing with other MOS circuitry.

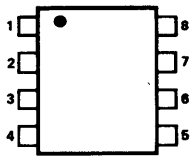
PIN CONFIGURATIONS (TOP VIEW)

T PACKAGE



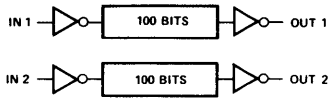
1. Input 1
2. Output 1
3. Input Clock (ϕ_2)
4. V_{CC}
5. Output Clock (ϕ_1)
6. Output 2
7. Input 2
8. V_{DD}

V PACKAGE



1. Output Clock (ϕ_1)
2. Output 2
3. Input 2
4. V_{DD}
5. Input 1
6. Output 1
7. Input Clock (ϕ_2)
8. V_{CC}

BLOCK DIAGRAM



PART IDENTIFICATION TABLE

PART NO.	OUTPUT	PACKAGE
2506 T	Bare Drain	8 Pin TO-5
2506 V	Bare Drain	8 Pin DIP
2507 T	7.5k Pull Down	8 Pin TO-5
2507 V	7.5k Pull Down	8 Pin DIP
2517 T	20k Pull Down	8 Pin TO-5
2517 V	20k Pull Down	8 Pin DIP

MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient	0°C + 70°C
Storage Temperature	-65°C + 150°C
Power Dissipation (Note 2) @ T_A=70°C	
T Package	535mW
V Package	455mW
Clock Input Voltages with respect to V_{CC}(3)	+0.3 to -20V
Supply and Data Input Voltages with respect to V_{CC}(3)	+0.3 to -12V

NOTES:
1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W (T package) or 175° C/W (V package).
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless otherwise specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}. V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.
9. V_{OL} (for this bare drain device) is a function only of the driven gate characteristics together with the external pull-down resistor. (R_{PD}).
10. See Figure 2 for definitions.
11. Logic Convention: Data Lines - Positive; Clocks - Negative.

DC CHARACTERISTICS

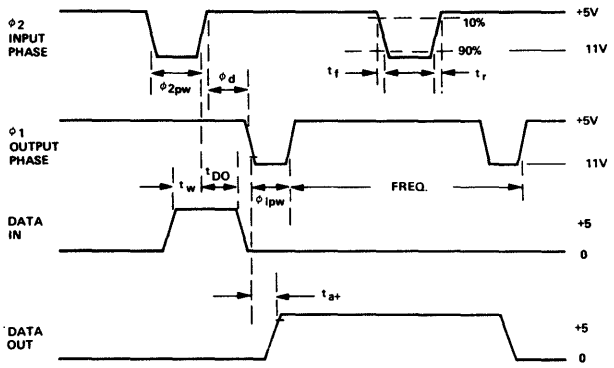
T_A = 0°C to +70°C; V_{DD} = -5V ±5%; V_{CC} = +5 (8); unless otherwise noted(Notes: 4,5,6,7).

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI}	Input Load Current (Input 1)		10	500	nA	+5V ON OUT 1, ϕ1, ϕ2, V_{CC}, IN 2, OUT 2, IN 1 = −5.5V, V_{DD} = −4.5V, T_A = 25°C
I_{LI}	Input Load Current (Input 2)		10	500	nA	+5V ON OUT 2, ϕ1, ϕ2, V_{CC}, IN 1, OUT 1, IN 2 = −5.5V, V_{DD} = −4.5V, T_A = 25°C
I_{LO}	Output Leakage Current (OUT 1) (Notes 9 & 10)		10	1000	nA	+5V ON IN 1, V_{CC}, OUT 2, ϕ2, IN 2, V_{DD}, OUT 1 = −5.5V ϕ1 = −10V, T_A = 25°C (2506 Only)
I_{LO}	Output Leakage Current (OUT 2) (Notes 9 & 10)		10	1000	nA	+5V ON IN 1, OUT 1, V_{CC}, ϕ2, IN 2, V_{DD}, OUT 2 = −5.5V, ϕ = −10V, T_A = 25°C (2506 Only)
I_{LC}	Clock Leakage Current (ϕ1)		10	1000	nA	Vϕ1 = −12V, V_{DD} = −4.5V All other pins +5V, T_A = 25°C
I_{LC}	Clock Leakage Current (ϕ2)		10	1000	nA	Vϕ2 = −12V, V_{DD} = −4.5V All other pins +5V T_A = 25°C
V_{IL}	Input "Low" Voltage (Note 11)	−5		1.05	V	
V_{IH}	Input "High" Voltage (Note 11)	3.2		5.3	V	
C_{IN}	Input Capacitance (Inputs 1 & 2)		2.5	5	pF	V_{IN} = V_{CC}, 1 MHz, 25 mV p-p
C_{ϕ}	Clock Input Capacitance (ϕ1, ϕ2)		25	40	pF	V_{ϕ} = V_{CC}, 1 MHz, 25 mV p-p
V_{IHC}	Clock Input "High" Voltage	4		5.3	V	
V_{ILC}	Clock Input "Low" Voltage	−12		−10	V	

CONDITIONS OF TEST

Data amplitude +1.05 to +3.2 Input rise and fall times: 10 nsec. Output load is 1 TTL gate.

TIMING DIAGRAM



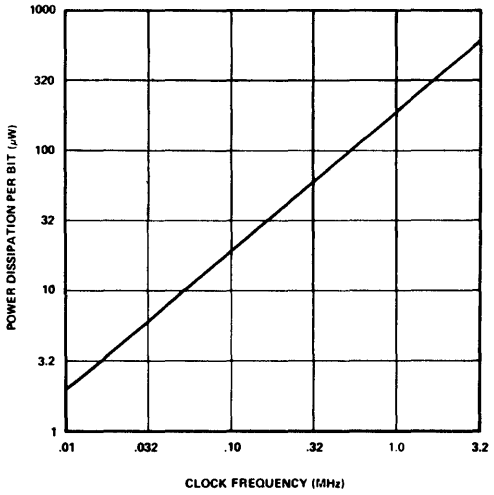
AC CHARACTERISTICS

$T_A = 25°C$; $V_{DD} = -5V \pm 5\%$; $V_{CC} = +5V$ (8) ; $V_{ILC} = -11V$

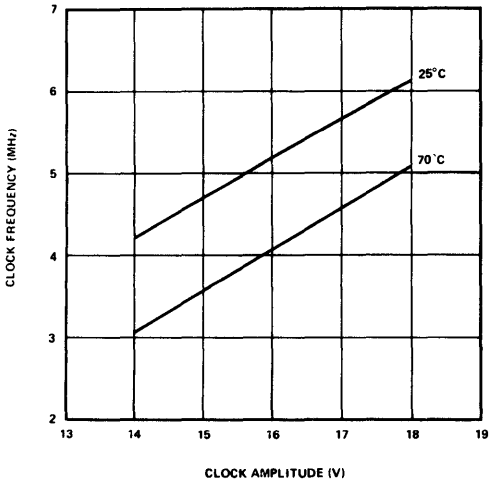
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
Frequency	Clock Rep Rate	.0006	4	3	MHz	
ϕ IPW	Clock Pulse Width ϕ 1	150			nsec	@ 3MHz.
ϕ 2PW	Clock Pulse Width ϕ 2	100			nsec	@ 3MHz.
ϕ_d	Clock Pulse Delay	10			nsec	@ 3MHz
t_r, t_f	Clock Pulse Transition	10		1000	nsec	
t_W	Data Write Time (Set-Up)	75				
t_{DO}	Data In Overlap	10				$t_{r\phi 2} = t_{r\phi 1} = 10nS$
t_{a+}	Clock to Data Out		90	150		$V\phi = V_{CC} - 16V$, DATA OUT =+2.5V
V_{OH1}	Output "High" Voltage driving MOS (Note 11)	3.4	4.0		V	R_{INT} = 7.5k nom., C_L = 10pF, 2507 Only, R_{INT} = 20k nom. 2517 only
V_{OH2}	Output "High" Voltage driving TTL (Note 11)	3.0	3.5		V	R_L = 3.3k, V_{DD} = -5V 2506 only
I_{DD}	Power Supply Current (V_{DD})		12	26	mA	Outputs @ logic "0" or "1", 3MHz, ϕ 1 = 150ns, ϕ 2 = 100ns

CHARACTERISTIC CURVES

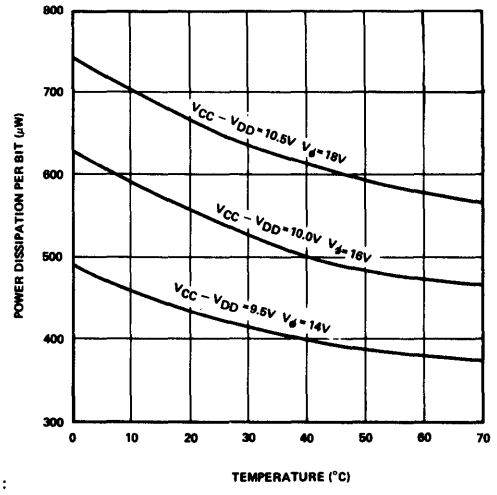
POWER DISSIPATION PER BIT VERSUS FREQUENCY



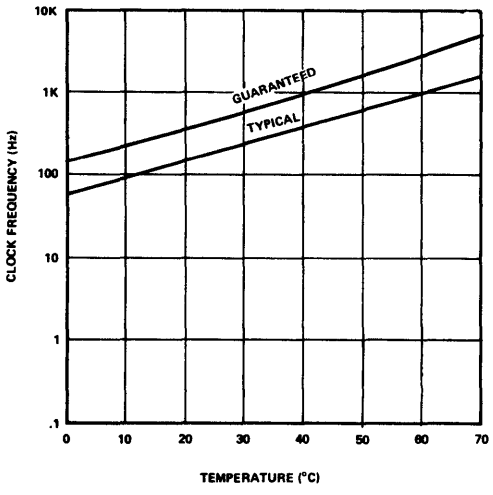
TYPICAL CLOCK FREQUENCY VERSUS CLOCK AMPLITUDE



POWER DISSIPATION BIT VERSUS TEMPERATURE



MINIMUM OPERATING CLOCK RATE

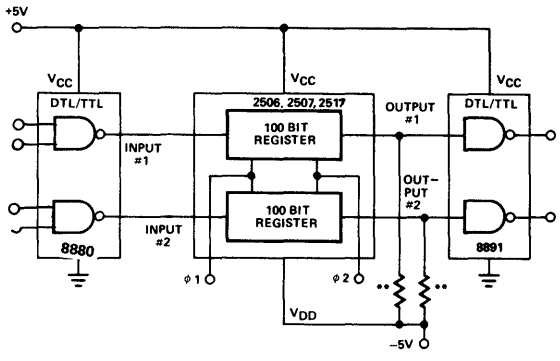


NOTE:
Contitions for Typical Curves: V_{CC}=+5V, V_{DD}=-5V. V_{ILC}=-11V, ϕ_{PW1}=150ns, ϕ_{PW2}=100ns, f=3MHz, T_A=+25°C unless otherwise noted.

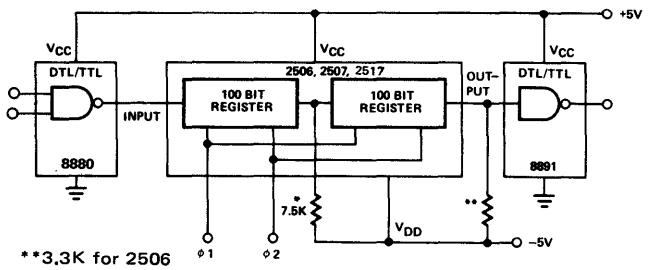
APPLICATIONS DATA

DTL/TTL/MOS INTERFACES

100-BIT DELAY



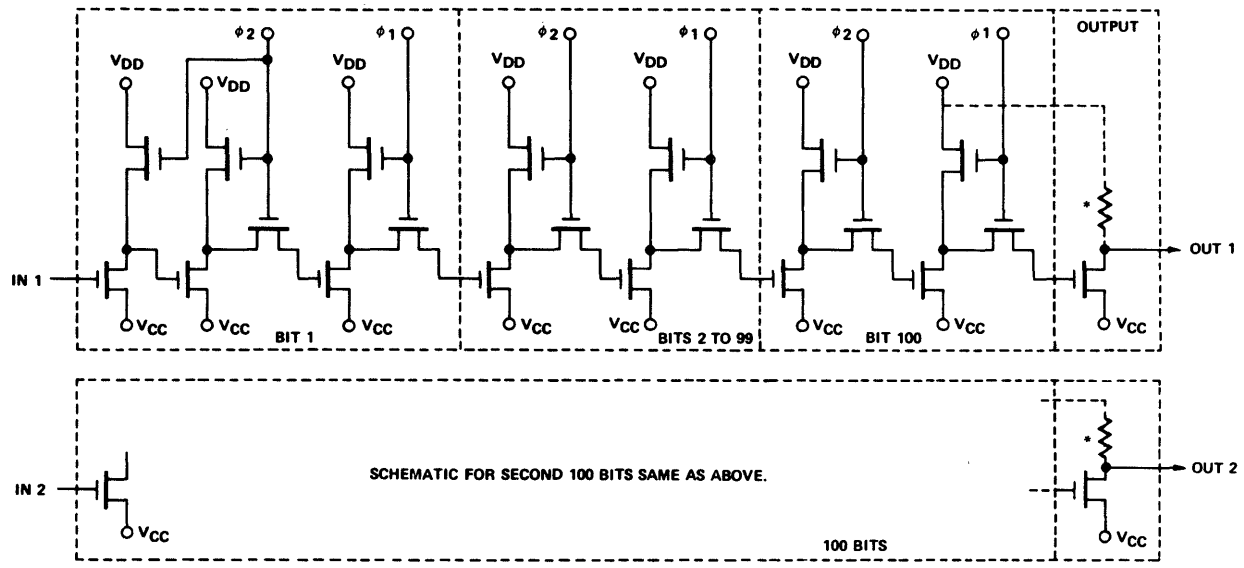
200-BIT DELAY



**3.3K for 2506
6.8K for 2507
3.3K for 2517

*For 2506 only.

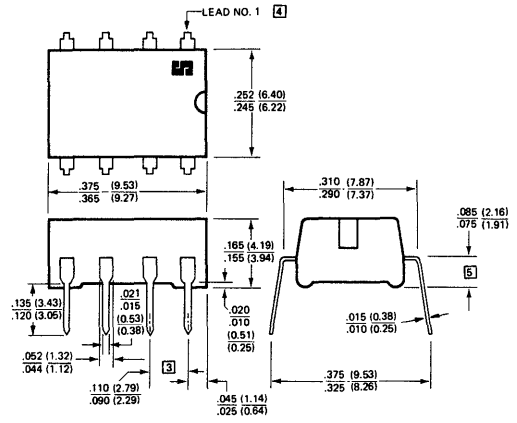
CIRCUIT SCHEMATIC



*For 2507 and 2517 Options Only.

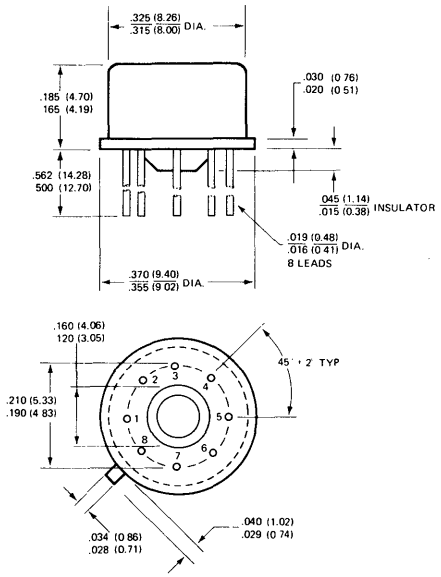
PACKAGE INFORMATION

V PACKAGE



NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: SILICONE MOLDED.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: Θ Ja = .16 C/mW, Θ Jc = .08 C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

T PACKAGE



NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED.
2. BODY MATERIAL: EYELET, KOVAR OR EQUIVALENT, GOLD PLATED, GLASS BODY.
3. LID MATERIAL: NICKEL, WELD SEAL.
4. THERMAL RESISTANCE FROM JUNCTION TO CASE, Θ Ja = .150 C/mW, Θ Jc = .025 C/mW.
5. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

TRI-STATE OUTPUT DUAL 50-100-200 BIT STATIC SHIFT REGISTERS

2509
2510
2511

SILICON GATE MOS 2000 SERIES

DESCRIPTION

These Signetics 2500 Series Dual 50, 100, and 200 bit recirculating static shift registers consist of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip. Internal recirculation logic plus TTL/DTL level clock signals plus TRI-STATE outputs are provided for maximum interfacing capability.

FEATURES

- TRI-STATE MOS OUTPUTS - PROVIDE POWERFUL BUSSING CAPABILITY
- TTL/DTL COMPATIBLE CLOCKS - PROVIDE EXTREMELY LOW CLOCK CAPACITANCE
- RECIRCULATION PATH ON CHIP
- THREE BIT LENGTHS AVAILABLE
- HIGH FREQUENCY OPERATION
- 2MHz GUARANTEED CLOCK RATE
- TTL, DTL COMPATIBLE SIGNALS
- STANDARD PACKAGES - 10 LEAD TO-100, 14 PIN DIP
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST STATIC BUFFER MEMORIES
CRT REFRESH MEMORIES - LINE STORAGE

SPECIAL FEATURES

The three clock phases used by the register cells are generated internally by an on-chip generator. This clock generator is controlled by a single TTL/DTL 5V logic level input.

The output has three states:
"1" low impedance to +5V
"0" low impedance to -5V
"OFF" high impedance ≃ 10 M ohm

The "OFF" state is controlled by the Output Enable control input.

PROCESS TECHNOLOGY

Use of low threshold silicon gate technology allows high speed (2 MHz Guaranteed) while reducing power dissipation and clock input capacitance dramatically as compared to conventional technologies.

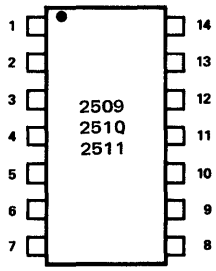
The use of low voltage circuitry minimizes power dissipation and facilitates interfacing with bipolar integrated circuits.

BIPOLAR COMPATIBILITY

The clock and signal inputs of these registers can be driven directly by standard bipolar integrated (TTL, DTL, etc.) or by MOS circuits. The TRI-STATE output stage provides driving capability for both MOS and bipolar integrated circuits (one standard TTL load).

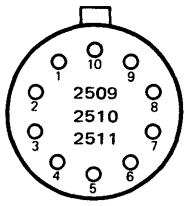
PIN CONFIGURATIONS (Top View)

A PACKAGE



1. $\overline{\text{Recirculate}}$
2. IN_1
3. OUT_1
4. NC
5. NC
6. NC
7. V_{DD}
14. V_{CC}
13. IN_2
12. OUT_2
11. NC
10. V_{GG}
9. Output Enable
8. ϕIN

K PACKAGE



1. IN_1
2. OUT_1
3. V_{DD}
4. ϕIN
5. V_{CC}
6. Output Enable
7. V_{GG}
8. OUT_2
9. IN_2
10. $\overline{\text{Recirculate}}$

PART IDENTIFICATION TABLE

PART NUMBER	BIT LENGTH	PACKAGE
2509K	Dual 50	10 Pin, TO-100
2509A	Dual 50	14 Pin, DIP
2510K	Dual 100	10 Pin, TO-100
2510A	Dual 100	14 Pin, DIP
2511K	Dual 200	10 Pin, TO-100
2511A	Dual 200	14 Pin, DIP

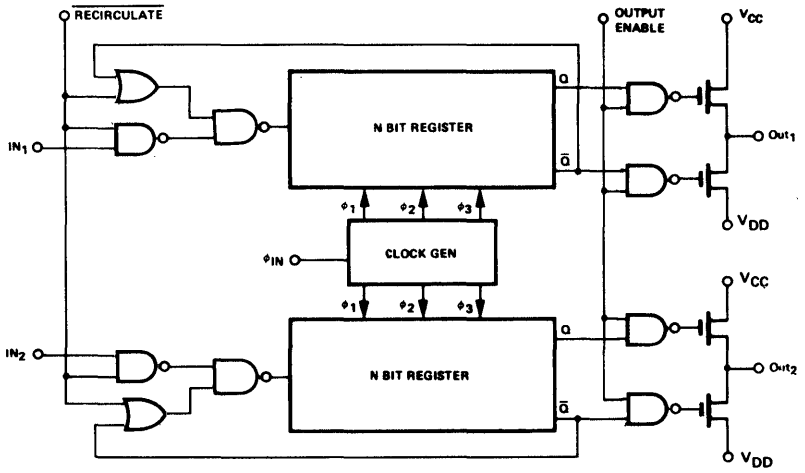
MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature (2)	0°C to +70°C
Storage Temperature	-65°C to +150°C
Package Power Dissipation (A & K) (Note 2) @ T_A = 70°C	535mW
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC} (3)	+0.3V to -20V

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless otherwise specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}. V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.

BLOCK DIAGRAM



NOTES:
1: If output enable = "0", output is "off"
2: If output enable = "1", see Truth Table.

TRUTH TABLE:

$\overline{\text{RECIRCULATE}}$	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is Written
1	1	"1" is Written

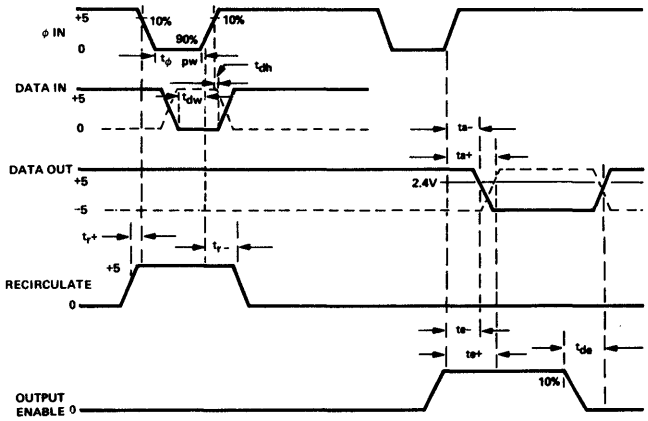
NOTE: "0" = OV; "1" = +5V.

DC CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = +5V (8); V_{DD} = -5V ±5%; V_{GG} = -12V ±5% unless otherwise noted. (Notes 4,5,6,7)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} =-5.5V, T_A = 25°C
I_{LO}	Output Leakage Current		10	1000	nA	V_{CE} =1.05V,T_A = 25°C, V_{OUT} = -5V
I_{LC}	Clock Leakage Current		10	500	nA	V_{ILC} = GND, T_A = 25°C
I_{DD}	Power Supply Current					
	(Dual 50)		6.5	15	mA	Continuous Operation
	(Dual 100)		12	30	mA	F = 2MHz, T_A = 25°C
	(Dual 200)		20	40	mA	
I_{GG}	Power Supply Current		4.5	7.5	mA	
V_{IL}	Input "Low" Voltage			1.05	V	
V_{IH}	Input "High" Voltage	3.2		5.3	V	
V_{ILC}	Clock Input "Low" Voltage	-5		1.05	V	
V_{IHC}	Clock Input "High" Voltage	3.2		5.3	V	

TIMING DIAGRAM

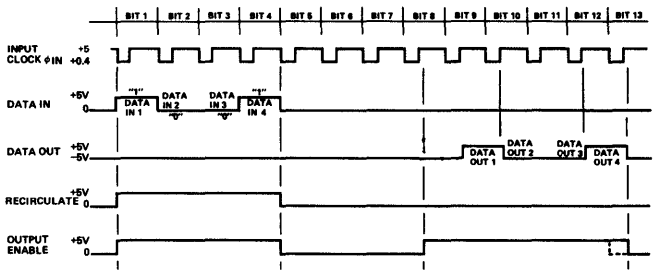


AC CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = +5V$ (8); $V_{DD} = -5V \pm 5\%$; $V_{ILC} = +0.4V$ to $4V$; $V_{GG} = -12V \pm 5\%$.

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
Frequency	Clock Rep Rate	DC	3	2	MHz	
$t_{\phi PW}$	Clock Pulse Width	.290	.150	100	μsec	
$\overline{t_{\phi PW}}$	Clock Pulse Width	.210		DC	μsec	
t_r; t_f	Clock Pulse Transition			1	μsec	
t_{DW}	Data Write (Set-up) Time	50			nsec	
t_{DH}	Data to Clock Hold Time	50			nsec	
t_{a+}; t_{a-}	Clock to Data Out Delay		200	350	nsec	
t_{r-}	Clock to Recirculate	50			nsec	
t_{cs-}, t_{cs+}	Output Enable to Data Out			300	nsec	
t_{DE}	Output Enable to Data Out Disconnect			300	nsec	
C_{IN}	Input Capacitance			5	pF	@ 1 MHz; $V_{IN} = V_{CC}$; $V_{AC} = 25$mV p-p
C_{OUT}	Output Capacitance			5	pF	@ 1 MHz; $V_{OUT} = V_{CC}$; $V_{AC} = 25$mV p-p
C_ϕ	Clock Capacitance			5	pF	@ 1 MHz; $V_\phi = V_{CC}$; $V_{AC} = 25$mV p-p
V_{OL}	Output "Low" Voltage			0.4	V	1 TTL load $I_L = 1.6$mA
V_{OH1}	Output "High" Voltage Driving 1 TTL Load	3.0	3.5		V	1 TTL load ($I_L = 100\mu$A)
V_{OH2}	Output "High" Voltage Driving MOS	3.6	4		V	

TIMING DIAGRAM



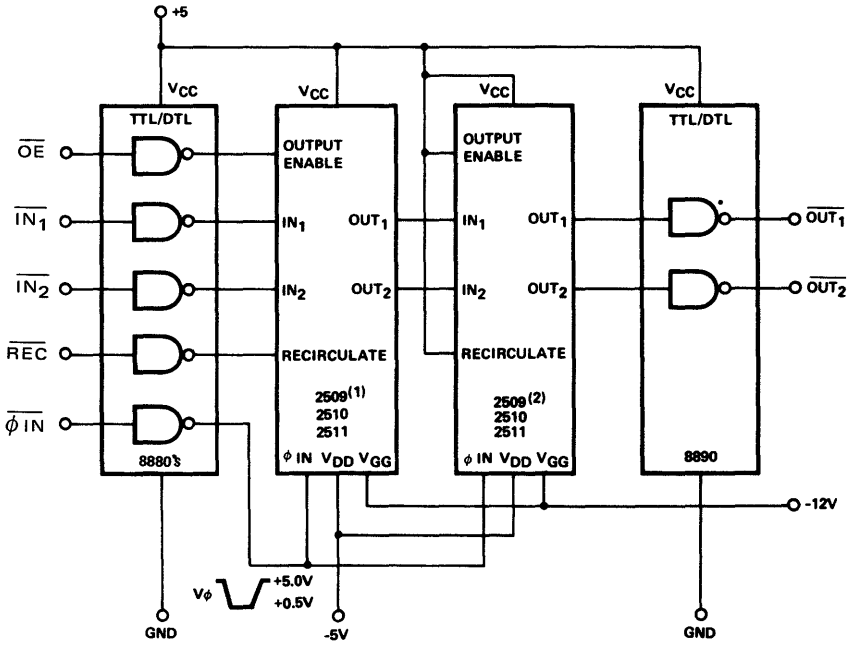
NOTE 1: WRITE CYCLE
The positive going edge of the recirculate control is coincident with the negative going edge of the input clock (ϕ_{IN}). The output enable control may be either "1" or "0".

NOTE 2: RECIRCULATE CYCLE
Data recirculates if the recirculate control is a "0" the output enable may be either "1" or "0".

NOTE 3: READ CYCLE
The negative going edge of the output enable control is coincident with the positive edge of the clock (ϕ_{IN}). Recirculate may be either "1" or "0".

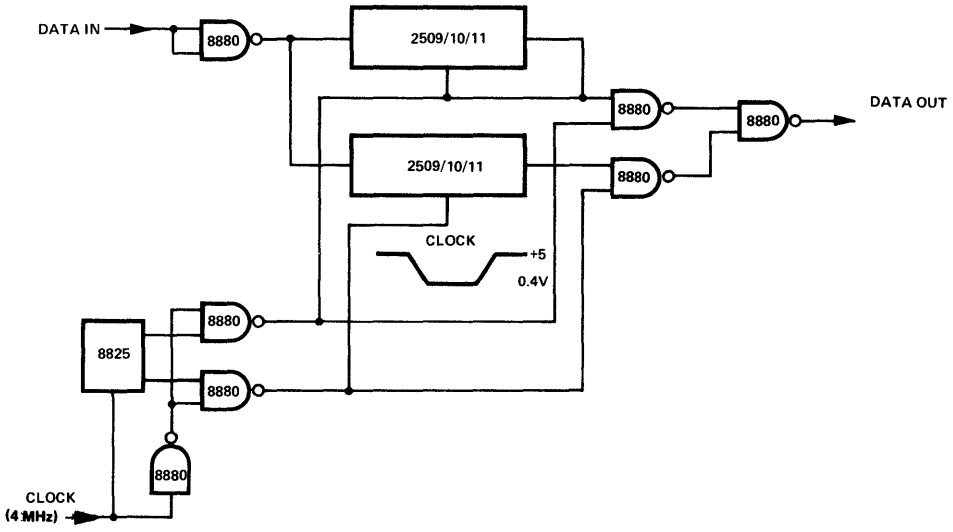
APPLICATIONS INFORMATION

TTL/DTL/MOS INTERFACES



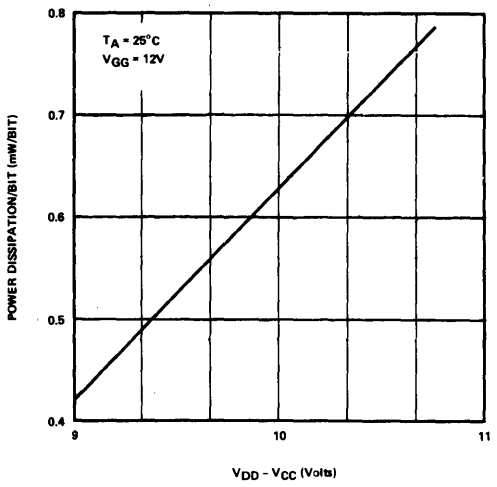
NOTES:
1. Register used as a recirculating register.
2. Register used as serial in/serial out shift register.

MULTIPLEXING MEMORY REGISTERS AT 4MHz DATA RATE

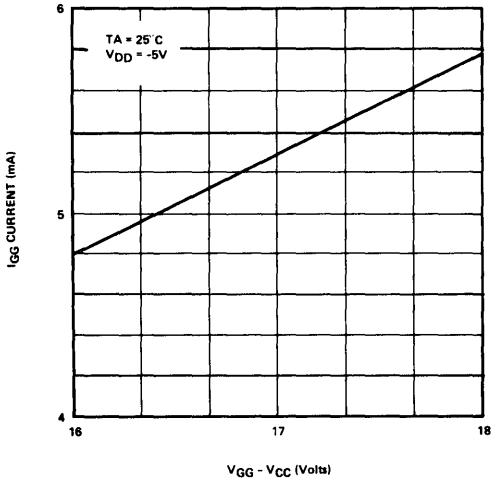


CHARACTERISTIC CURVES

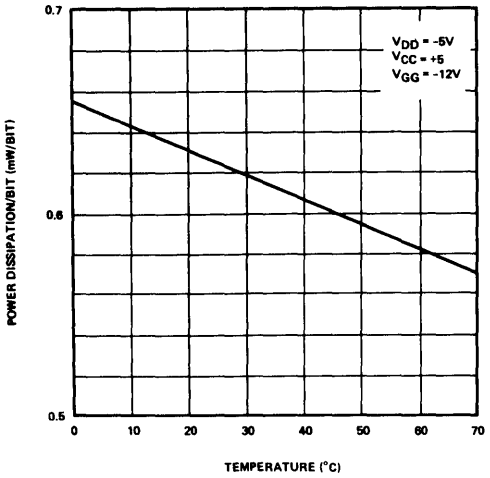
POWER DISSIPATION/BIT VERSUS V_{DD} SUPPLY VOLTAGE



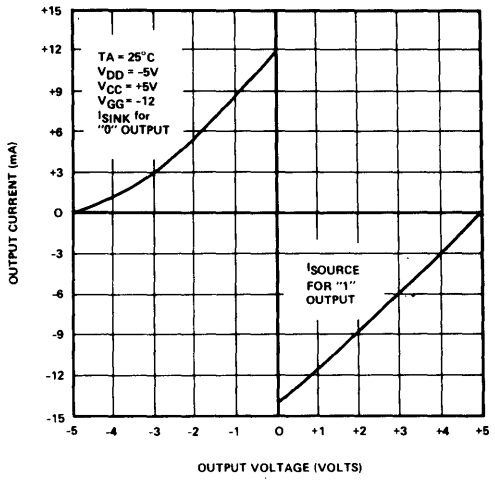
I_{GG} CURRENT VERSUS V_{GG} SUPPLY VOLTAGE



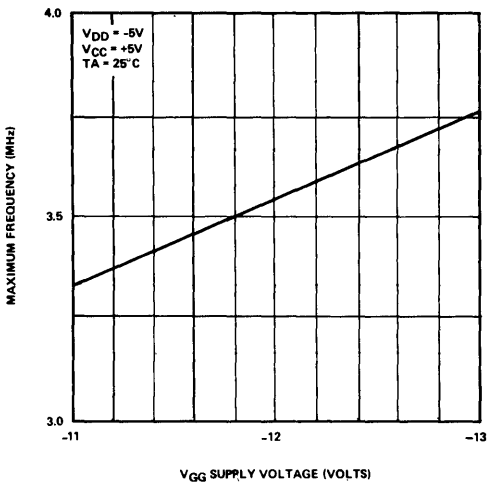
POWER DISSIPATION/BIT VERSUS TEMPERATURE



OUTPUT VOLTAGE VERSUS OUTPUT CURRENT

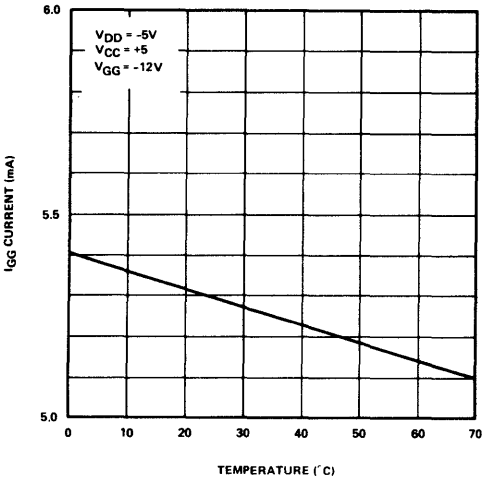


MAXIMUM FREQUENCY VERSUS V_{GG} SUPPLY VOLTAGE

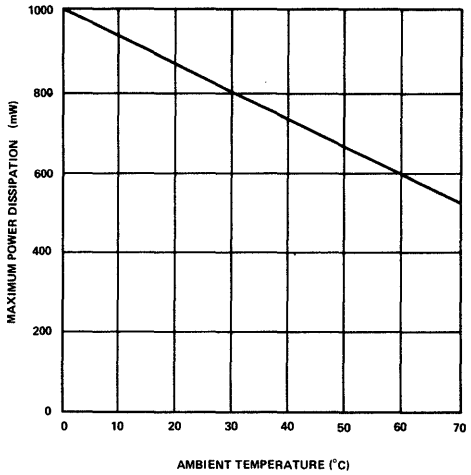


CHARACTERISTIC CURVES (Cont'd.)

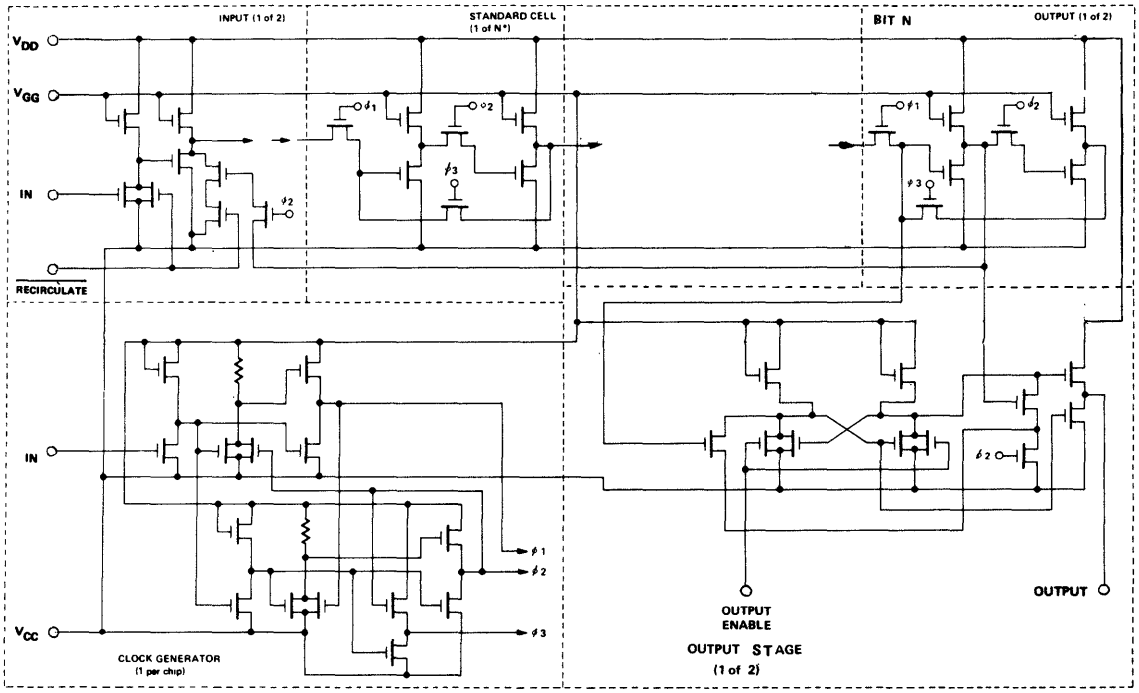
I_{GG} CURRENT VERSUS TEMPERATURE



PACKAGE MAXIMUM POWER DISSIPATION

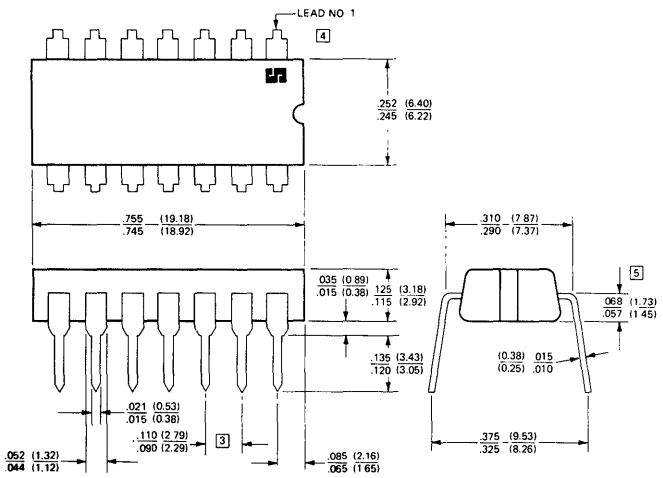


SCHEMATIC DIAGRAM



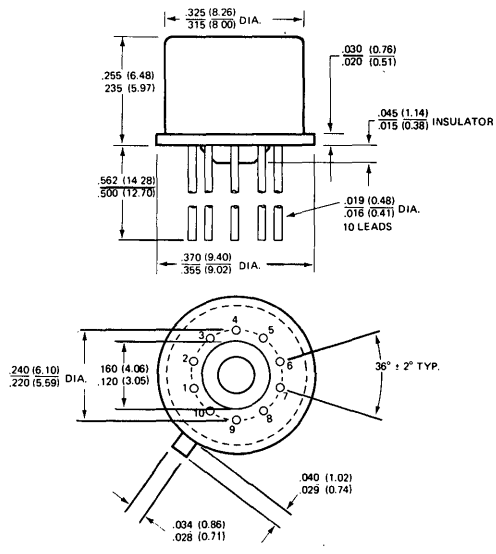
PACKAGE INFORMATION

A PACKAGE



NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: SILICONE MOLDED.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: Θ Ja = .16 C/mW, Θ Jc = .08 C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

K PACKAGE



NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED.
2. BODY MATERIAL: CERAMIC WITH KOVAR OR EQUIVALENT.
3. LID MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED, ALLOY SEAL.
4. TOLERANCES NON CUMULATIVE.
5. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
6. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
7. THERMAL RESISTANCE: Θ Ja = .060°C/mW, Θ Jc = .015°C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

HIGH SPEED 64 X 7 X 5 CHARACTER GENERATOR 512 X 5 STATIC READ-ONLY MEMORY

2513

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The Signetics 2513/2514† is a high speed 2560-bit Static ROM available in 64X7X5, 64X8X5, and 512X5 versions. The product uses +5V, -5V and -12V power supplies, 5V TTL level input signals and Tri-State-Outputs for direct, low cost interfacing with TTL, DTL and 2500 Series MOS.

FEATURES

- 450 ns TYPICAL ACCESS TIME
- STATIC OPERATION
- TTL/DTL COMPATIBLE INPUTS
- +5, -5, -12V POWER SUPPLIES
- TRI-STATE OUTPUT CONTROLLED BY CHIP ENABLE FOR POWERFUL BUSSING CAPABILITY
- 2513/CM2140 ASCII FONT STANDARD (7 X 5)
- 2514 SEPARATE V_{DD} FOR POWER REDUCTION
- 24-PIN SILICONE DIP
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

RASTER SCAN CRT DISPLAYS (ROW OUTPUT)
PRINTER CHARACTER GENERATOR
PANEL DISPLAYS AND BILLBOARDS
MICRO-PROGRAMMING
CODE CONVERSION

PROCESS TECHNOLOGY

The use of Signetics' unique Silicon Gate Low Threshold Process allows the design and production of higher functional density and operating speed than other techniques.

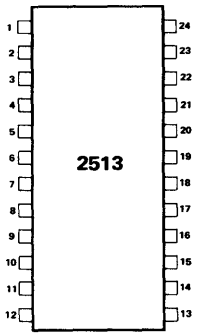
SILICONE PACKAGING

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process the silicon material over the gate oxide passivates the MOS transistors. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability, superior moisture resistance, and ionic contamination barriers. For further information reference Signetics - "Silicone Package Qualification Report".

BIPOLAR COMPATIBILITY

All inputs of the 2513/14 can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc). The data output buffers are capable of sinking a minimum of 1.6 mA, sufficient to drive one standard TTL load.

PIN CONFIGURATION (Top View)



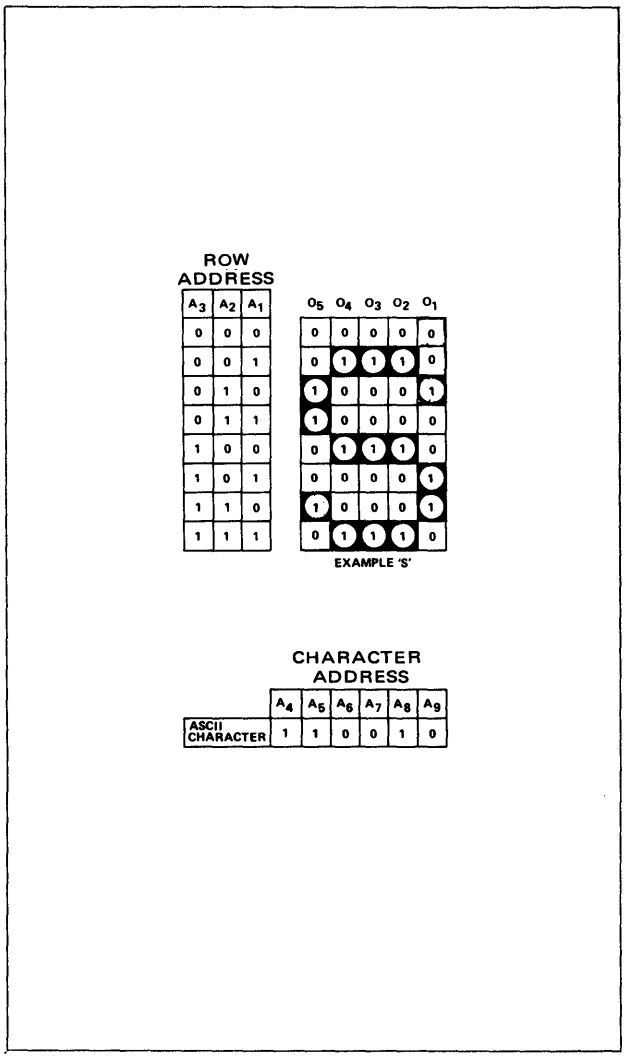
1.	V_{GG}	24.	V_{CC}
2.	NC	23.	NC
3.	NC	22.	Address 9
4.	Out 1	21.	Address 8
5.	Out 2	20.	Address 7
6.	Out 3	19.	Address 6
7.	Out 4	18.	Address 5
8.	Out 5	17.	Address 4
9.	NC	16.	Address 3
10.	Ground	15.	Address 2
11.	Chip Enable	14.	Address 1
12.	V_{DD}	13.	NC

PART IDENTIFICATION TABLE

PART	ORGANIZATION	PROGRAMMING
2513NX** CM2140	64X8X5	ASCII Font
2513NX** CMXXXX	64X7X5 64X8X5	Custom *

† The 2514 has been discontinued.
* Ask for "Signetics 2513/2514 Read Only Memory Software Package"
** Effective July 1, 1972 all new orders will be manufactured in the 'N' package.

CHARACTER FORMAT



MAXIMUM GUARANTEED RATINGS(1)

Operating Ambient Temperature	0°C to 70°C
Storage Temperature	-65°C to +150°C
Package Power Dissipation(2) @T_A 70°C	730mW
Input(3) and Supply Voltages with respect to V_{CC}	+0.3 to -20V

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 110°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}. V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.

DC CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = +5V (8) ; V_{DD} =-5V; V_{GG} = -12V ±5% unless otherwise noted. (Notes 4, 5, 6, 7)

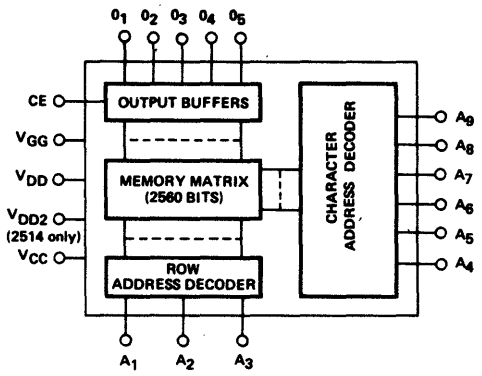
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} = -5.5V T_A = 25°C
I_{LO}	Output Leakage Current		10	1000	nA	V_{OUT} = -5.5V T_A = 25°C V_{CE} = V_{CC}
I_{DD}	V_{DD} Power Supply Current		12	18	mA	Outputs Open
I_{GG}	V_{GG} Power Supply Current		7	10	mA	Outputs Open
V_{IL}	Input Logic "0"			1.05	V	
V_{IH}	Input Logic "1"	3.2		5.3	V	

AC CHARACTERISTICS

T_A = 25°C; V_{CC} = 5V (8) ; V_{DD} =-5V ±5%; V_{GG} = -12V ±5%; unless otherwise noted.

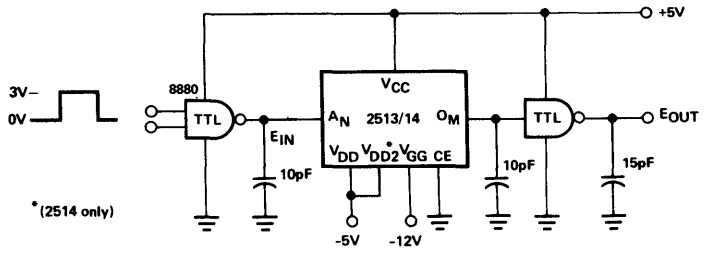
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OL}	Output Logic "Zero"	-5		0.4	V	One TTL Load
V_{OH}	Output Logic "One"	3.0			V	One TTL Load
t_{CA} (2513/ CM2140)	Character Access Time		500	600	ns	See AC Test Setup
t_{CA}(2514)	Access Time (A_4 - A_9)		500	600	ns	See AC Test Setup
t_{RA}	Row Access Time (A_1 - A_3)		450	500	ns	See AC Test Setup
t_{CE}	Chip Enable to Output		150		ns	
C_{IN}	Address Input Capacitance			10	pF	f = 1 MHz, V_{IH} = V_{CC}, 25mV p - p

BLOCK DIAGRAM

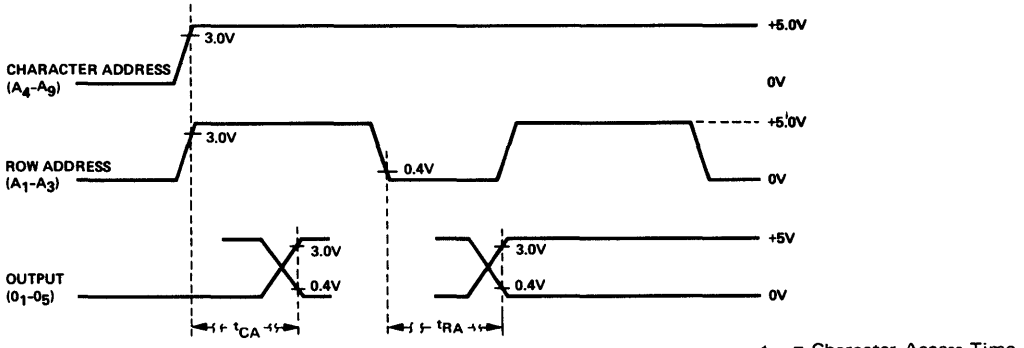


CE	OUTPUT
0	DATA
1	OPEN

AC TEST SETUP



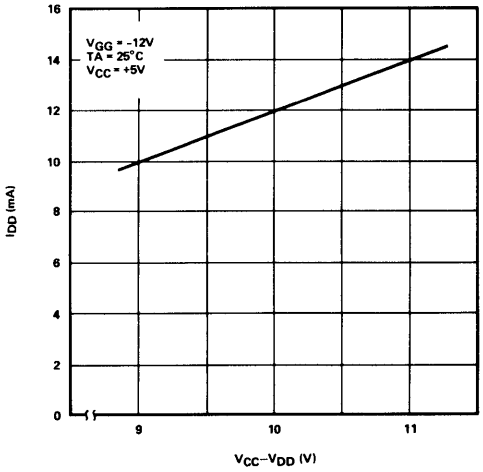
TIMING DIAGRAM (ADDRESS TIME)



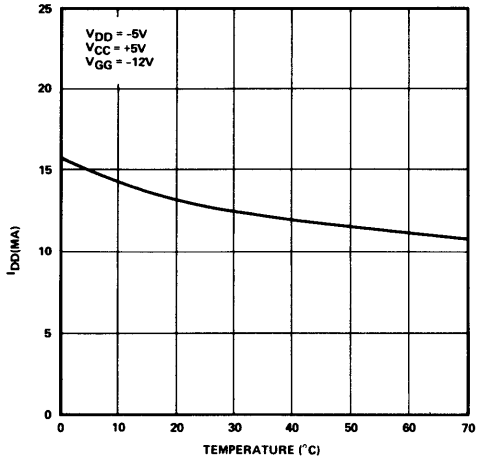
t_{CA} = Character Access Time
t_{RA} = Row Access Time

CHARACTERISTIC CURVES

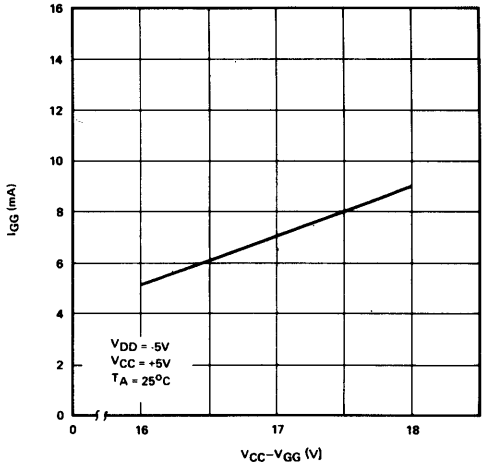
V_{DD} POWER SUPPLY CURRENT VERSUS VOLTAGE



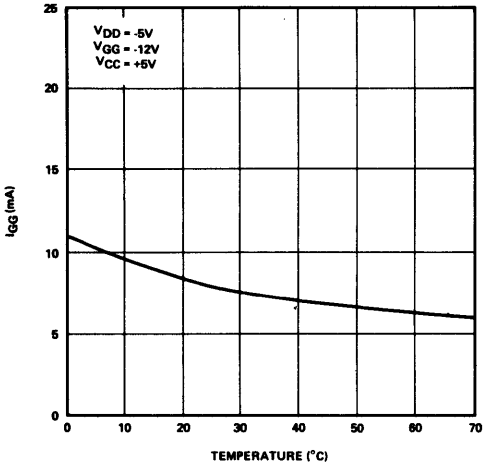
V_{DD} POWER SUPPLY CURRENT VERSUS TEMPERATURE



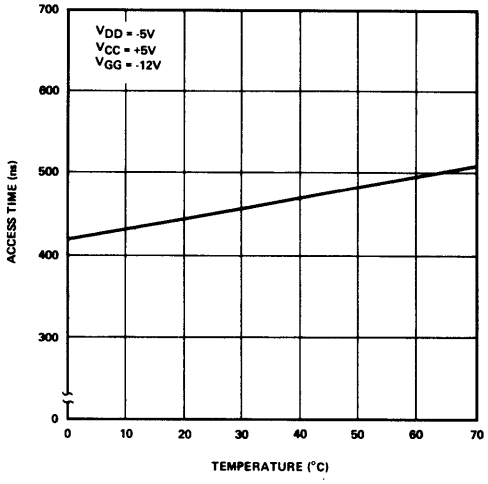
V_{GG} POWER SUPPLY CURRENT VERSUS VOLTAGE



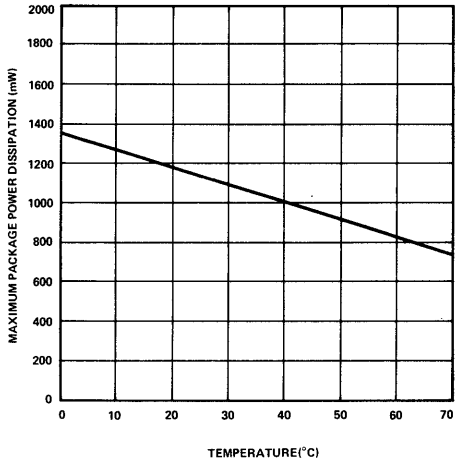
V_{GG} POWER SUPPLY CURRENT VERSUS TEMPERATURE



TYPICAL ACCESS TIME VERSUS TEMPERATURE

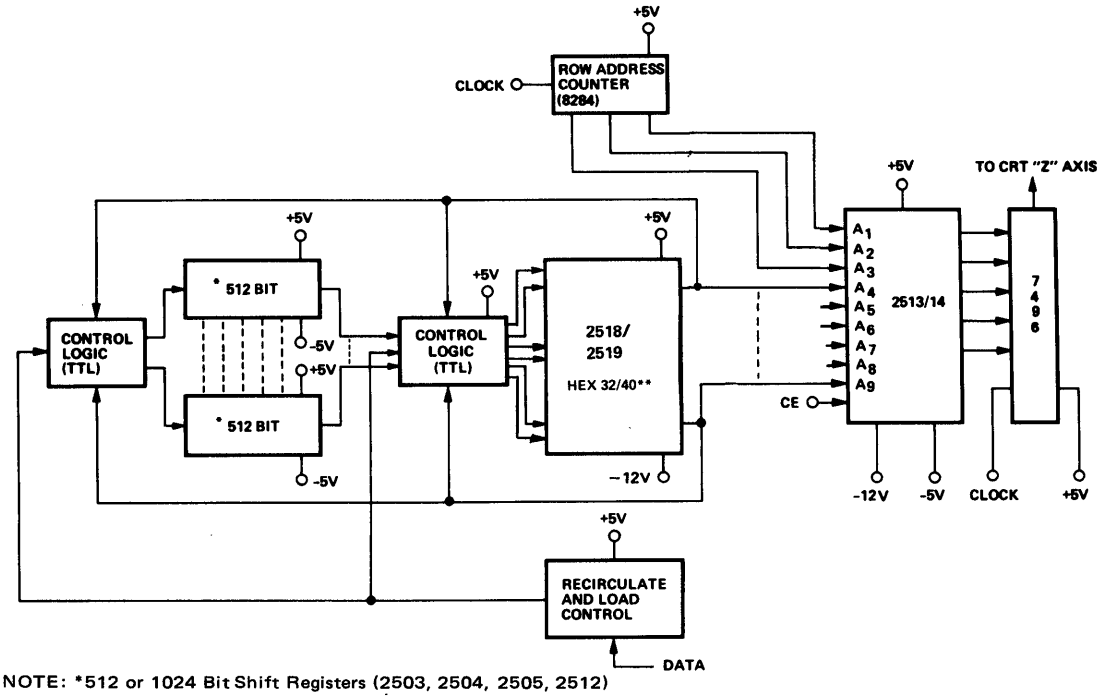


MAXIMUM PACKAGE POWER DISSIPATION



APPLICATIONS INFORMATION

CRT DISPLAY MEMORY AND CHARACTER GENERATOR

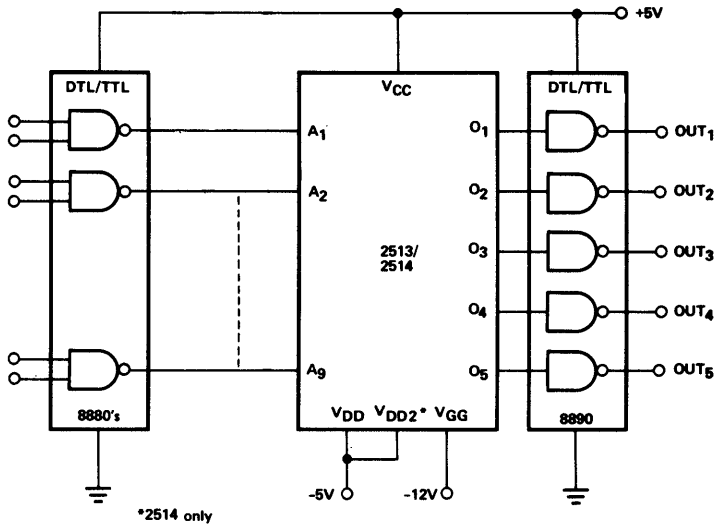


NOTE: *512 or 1024 Bit Shift Registers (2503, 2504, 2505, 2512)

** or Hex 64 BIT Two 2518's

Hex 72 BIT 2518 + 2519's

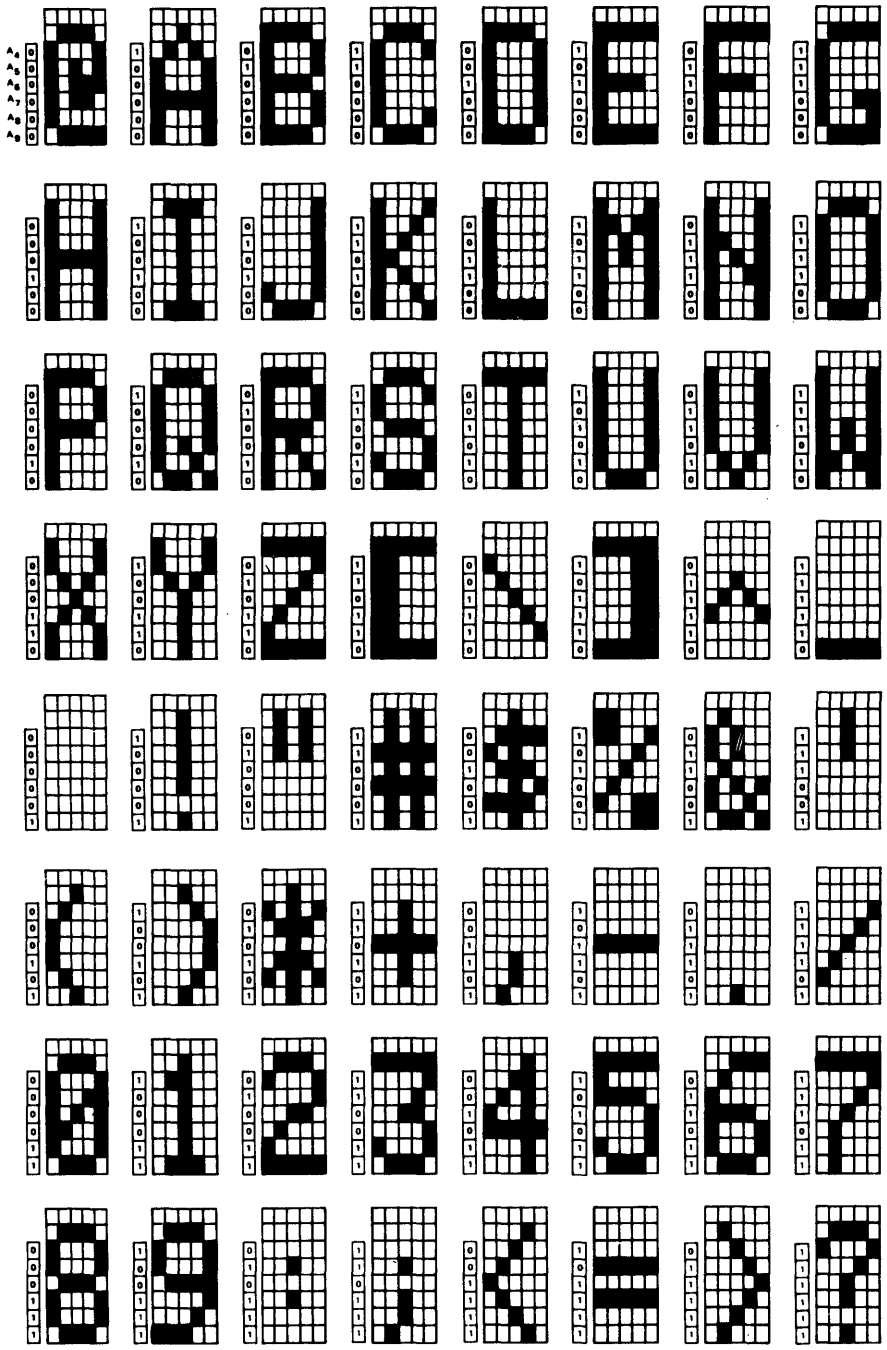
DTL/TTL INTERFACING



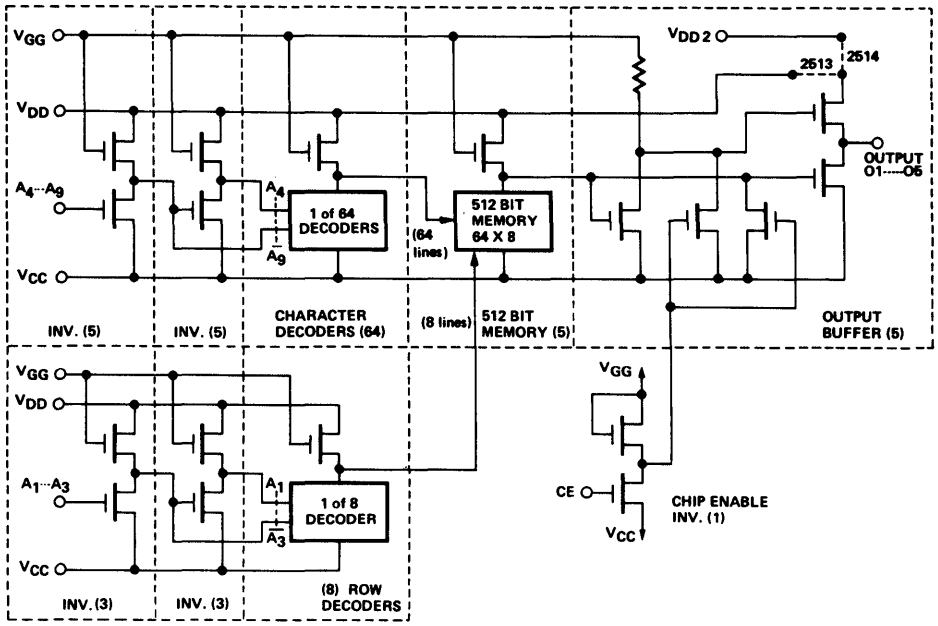
*2514 only

ASCII CHARACTER FONT

2513NX/CM2140

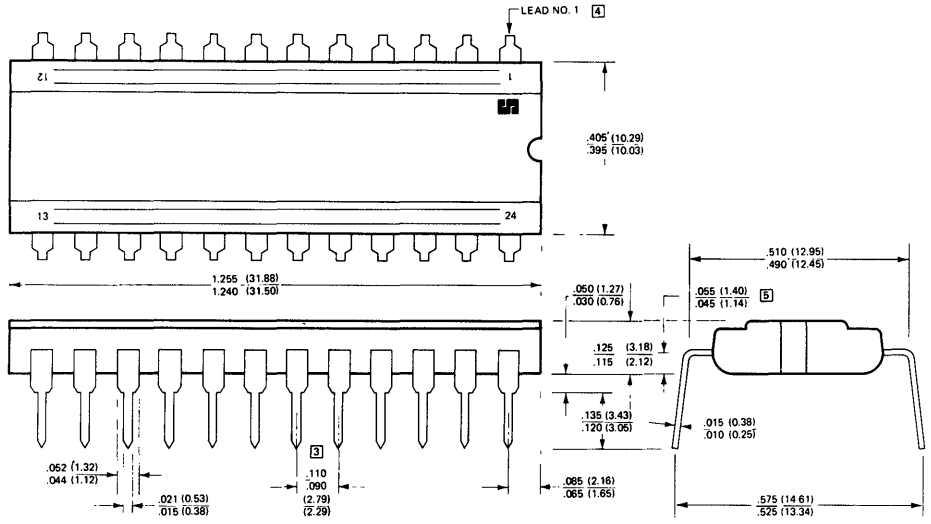


CIRCUIT SCHEMATIC



PACKAGE INFORMATION

N PACKAGE



NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: SILICONE MOLDED.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: Θ Ja = .12 C/mW, Θ Jc = .05 C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

HIGH SPEED 64 X 6 X 8 STATIC CHARACTER GENERATOR

2516

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The Signetics 2516 is a high speed 3072-bit Static ROM available in a 64 x 6 x 8 organization. The product uses +5V, -5V and -12V power supplies, 5V TTL level input signals and Tri-State-Outputs for direct, low cost interfacing with TTL, DTL and 2500 Series MOS.

FEATURES

- COLUMN OUTPUT
- 450 ns TYPICAL ACCESS TIME
- STATIC OPERATION
- TTL/DTL COMPATIBLE INPUTS
- +5, -5, -12V POWER SUPPLIES
- TRI-STATE OUTPUT CONTROLLED BY CHIP ENABLE FOR POWERFUL BUSSING CAPABILITY
- 2516/CM 2150 ASCII FONT STANDARD (5 x 7)
- OPTIONAL SEPARATE OUTPUT V_{DD} FOR POWER REDUCTION
- OPTIONAL CHIP ENABLE "2" FOR 4 BIT WORD ORGANIZATION
- 24-PIN SILICONE DIP
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

VERTICAL SCAN CRT DISPLAYS (COLUMN OUTPUT)
PRINTER CHARACTER GENERATOR
PANEL DISPLAYS AND BILLBOARDS
MICRO-PROGRAMMING
CODE CONVERSION

PROCESS TECHNOLOGY

The use of Signetics' unique Silicon Gate Low Threshold Process allows the design and production of higher functional density and operating speed than other techniques.

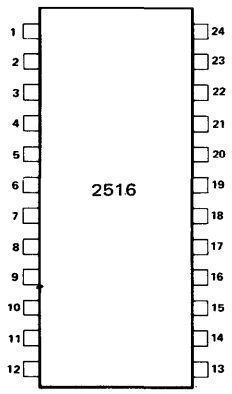
BIPOLAR COMPATIBILITY

All inputs of the 2516 can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.). The data output buffers are capable of sinking a minimum of 1.6mA, sufficient to drive one standard TTL load.

SILICONE PACKAGING

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process the silicon material over the gate oxide passivates the MOS transistors. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability, superior moisture resistance, and ionic contamination barriers. For further information reference Signetics - "Silicone Package Qualification Report."

PIN CONFIGURATION (Top View)



1.	Chip Enable	24.	V_{CC}
2.	NC	23.	V_{GG}
3.	Output 8	22.	Address 9
4.	Output 7	21.	Address 8
5.	Output 6	20.	Address 7
6.	Output 5	19.	Address 6
7.	Output 4	18.	Address 5
8.	Output 3	17.	Address 4
9.	Output 2	16.	Address 3
10.	Output 1	15.	Address 2
11.	Ground	14.	Address 1
12.	V_{DD}	13.	NC

*Optional on all custom ROMs (NC on CM 2150)

PART IDENTIFICATION TABLE

PART	ORGANIZATION	PROGRAMMING
2516NX** CM 2150	64 x 6 x 8	ASCII Font
2516NX** CMXXXX	64 x 6 x 8	Custom*

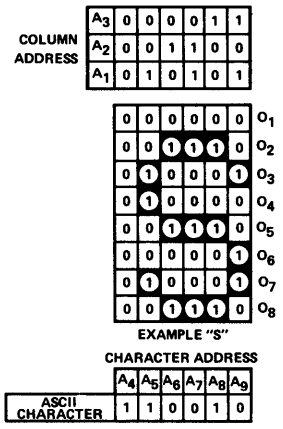
*Ask for "Signetics 2516 Read-Only-Memory Software Package" (See Section 6)

** Effective July 1, 1972 all new orders will be manufactured in the 'N' package.

MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature	0°C to 70°C
Storage Temperature	-65°C to +150°C
Package Power Dissipation(2) @ 70°C	730 mW
Input(3) and Supply Voltages with respect to V_{CC}	+0.3 to -20V

CHARACTER FORMAT



NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 110°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH}, and V_{OH} which are stated for a V_{CC} of exactly 5 volts.

DC CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = +5V; V_{DD} = -5V ±5%; V_{GG} = -12V ±5%; unless otherwise noted. (Notes 4, 5, 6, 7)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} = -5.5V T_A = 25°C
I_{LO}	Output Leakage Current		10	1000	nA	V_{OUT} = -5.5V T_A = 25°C
I_{DD}	V_{DD} Power Supply Current		14	21	mA	V_{CE} = V_{CC} Outputs Open
I_{GG}	V_{GG} Power Supply Current		8	12	mA	Outputs Open
V_{IL}	Input Logic "0"	-5		1.05	V	
V_{IH}	Input Logic "1"	3.2		5.3	V	

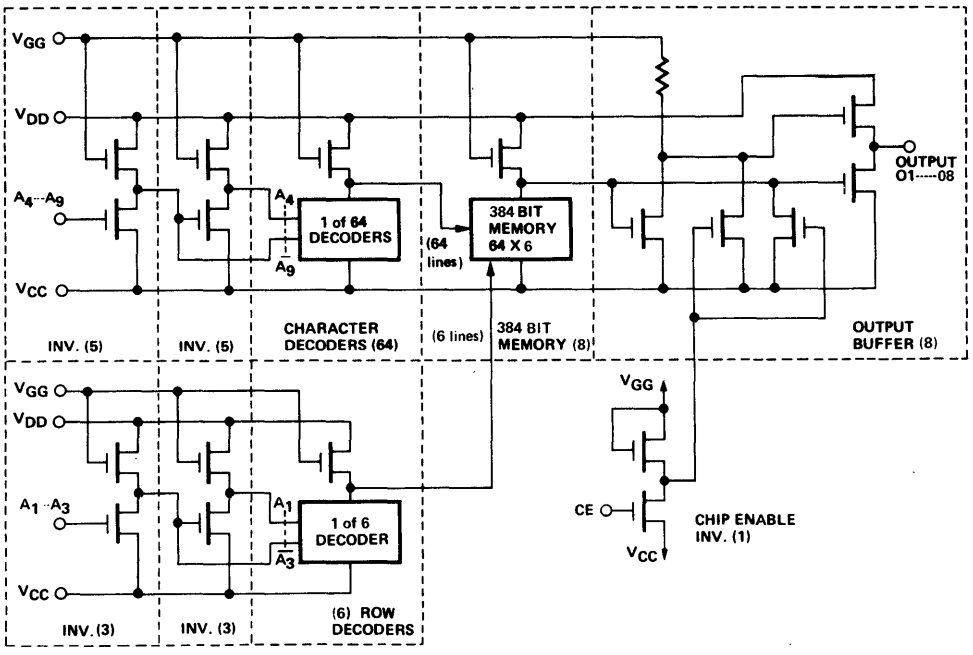
AC CHARACTERISTICS

T_A = 25°C; V_{CC} = 5V(8); V_{DD} = -5V ±5%; V_{GG} = -12V ±5%; unless otherwise noted.

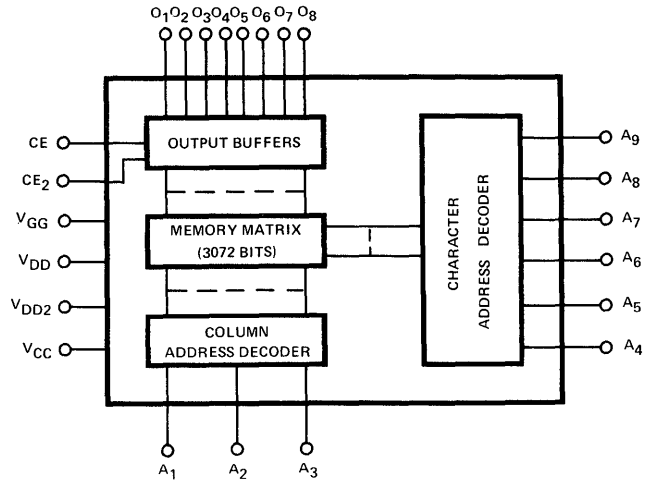
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OL}	Output Logic "Zero"	-5		0.8	V	One TTL Load
V_{OH}	Output Logic "One"	3.0			V	One TTL Load
t_{CA}	Character Access Time		500	600	ns	See AC Test Setup*
t_{CA}	Column Access Time (A_1 - A_3)		400	500	ns	See AC Test Setup*
C_{IN}	Address Input Capacitance			10	pF	f = 1MHz, V_{IH} = V_{CC}, 25mV p-p

*T_A=0°C to +70°C

CIRCUIT SCHEMATIC



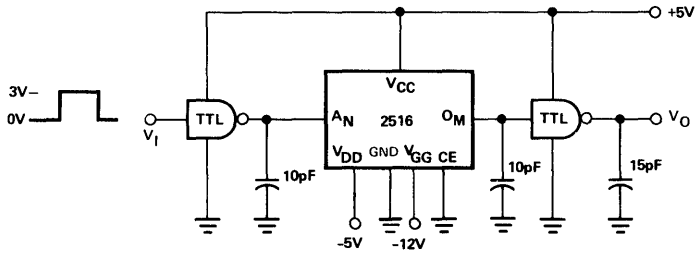
BLOCK DIAGRAM



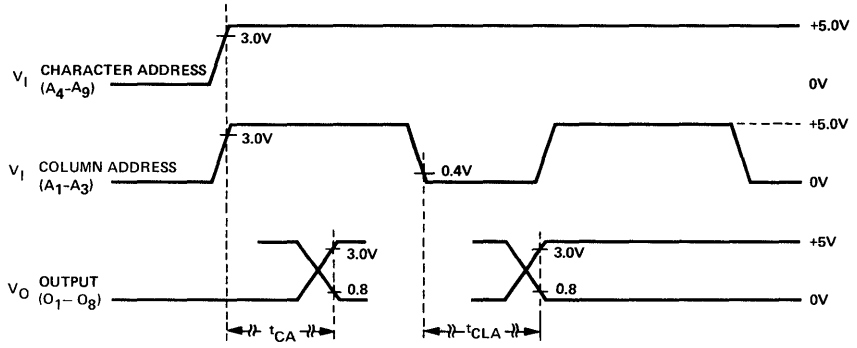
Note: For 4-Bit organization
Chip Enable 1 controls
$O_1 - O_4$, Chip Enable
2 controls $O_5 - O_8$.

CE	OUTPUT
0	DATA
1	OPEN

AC TEST SETUP



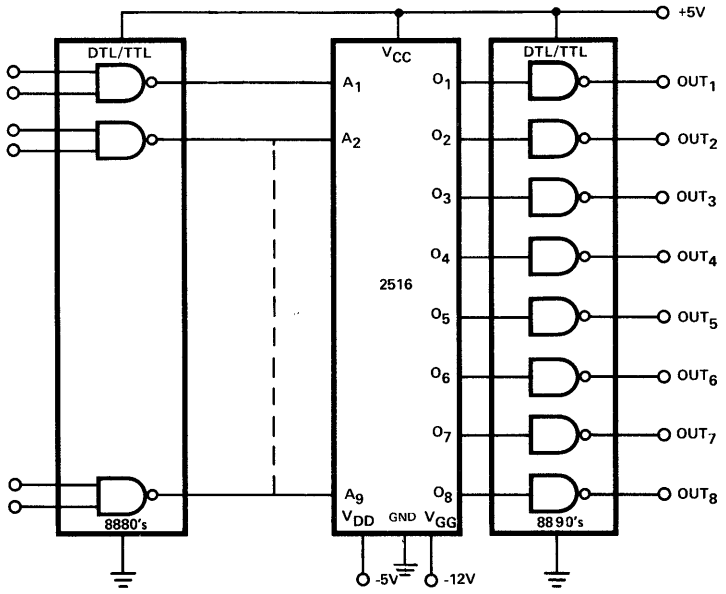
TIMING DIAGRAM (ADDRESS TIME)



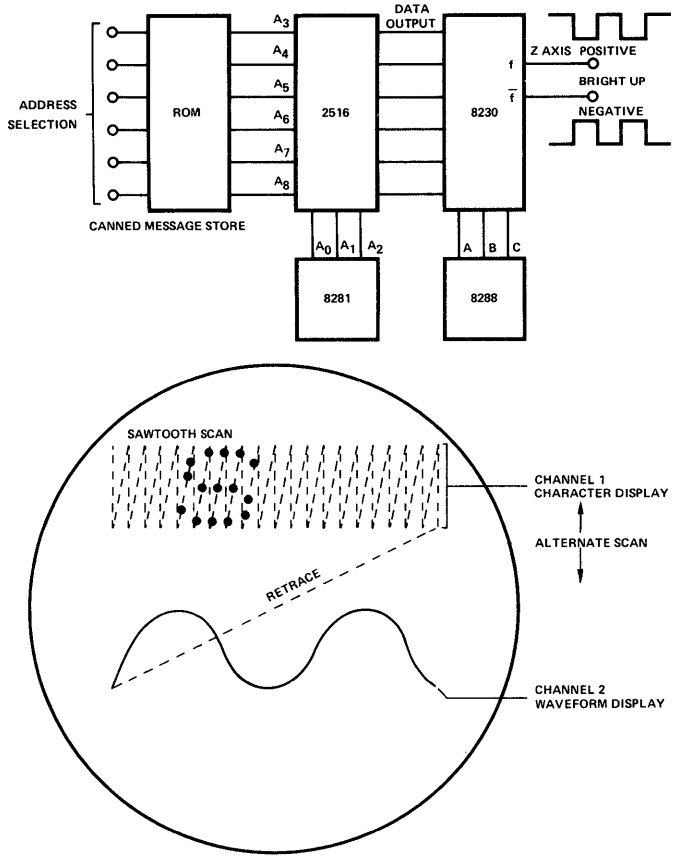
t_{CA}=CHARACTER ACCESS TIME
t_{CLA}=COLUMN ACCESS TIME

APPLICATIONS INFORMATION

DTL/TTL INTERFACING

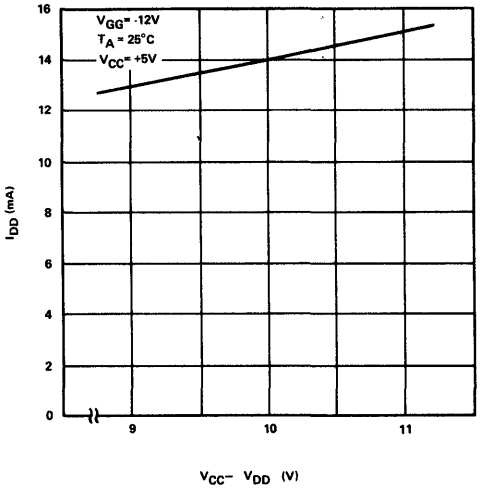


CRT DISPLAY MEMORY AND CHARACTER GENERATOR

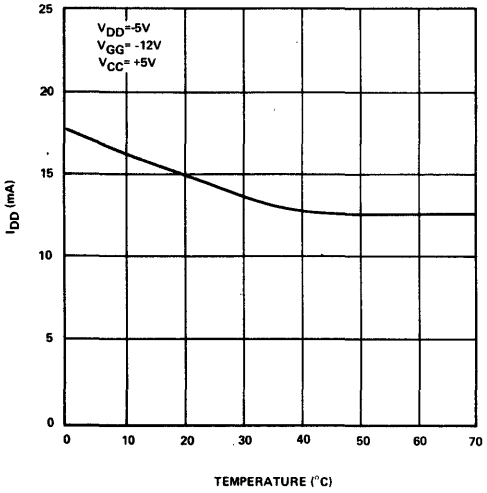


CHARACTERISTIC CURVES

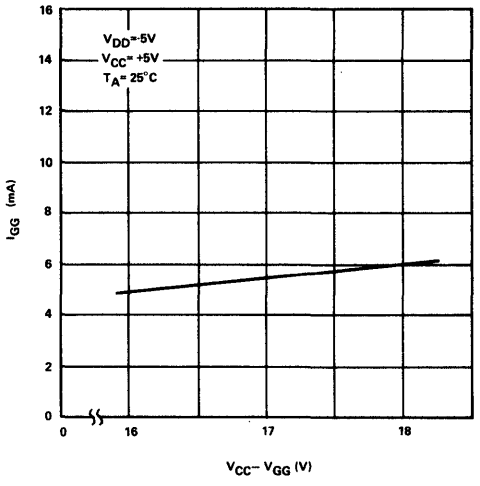
V_{DD} POWER SUPPLY CURRENT VERSUS VOLTAGE



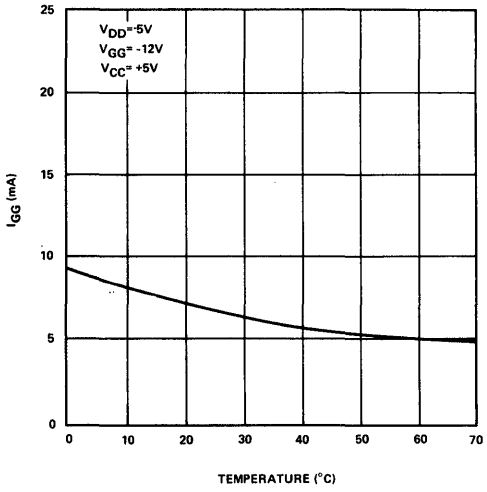
V_{DD} POWER SUPPLY CURRENT VERSUS TEMPERATURE



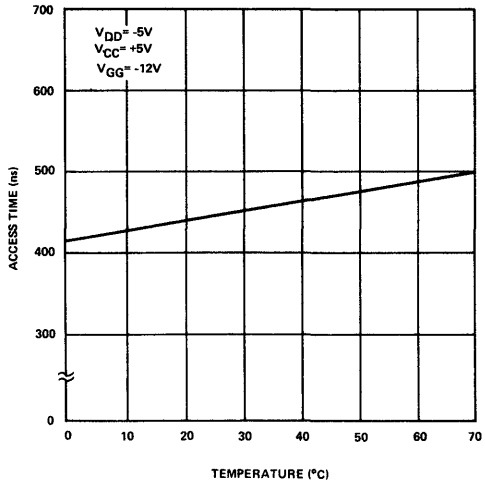
V_{GG} POWER SUPPLY CURRENT VERSUS VOLTAGE



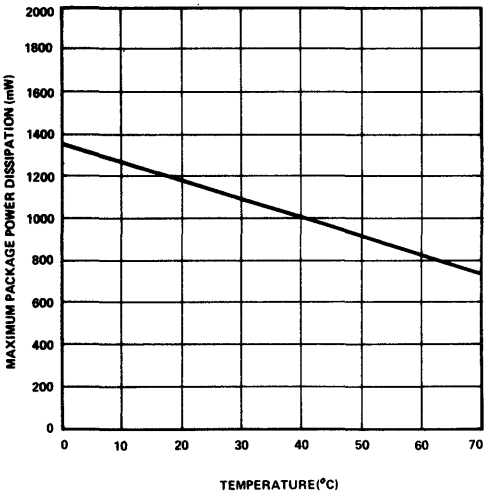
V_{GG} POWER SUPPLY CURRENT VERSUS TEMPERATURE



TYPICAL ACCESS TIME VERSUS TEMPERATURE

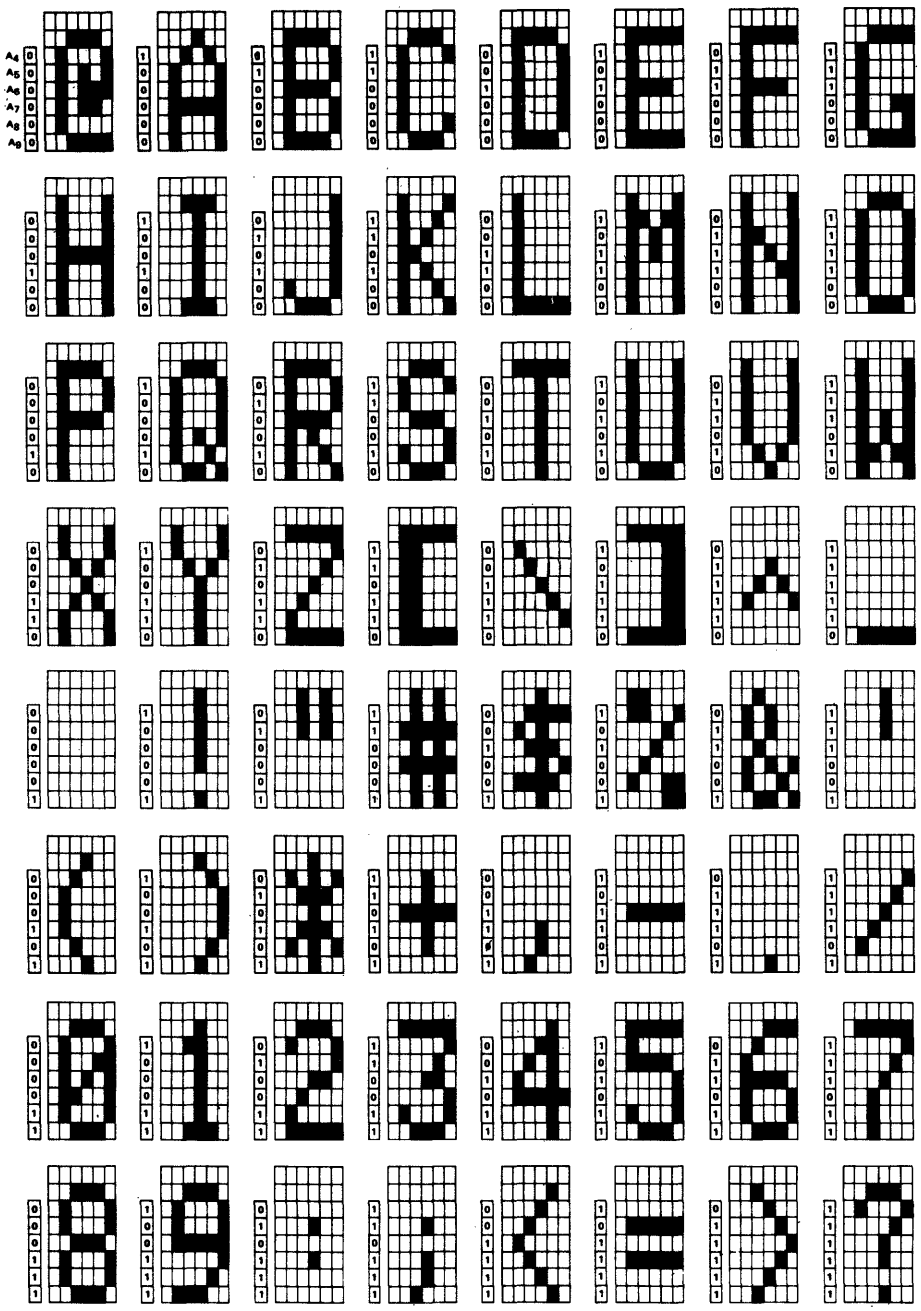


MAXIMUM PACKAGE POWER DISSIPATION VERSUS TEMPERATURE



ASCII CHARACTER FONT

2516NX/CM2150



APPLICATIONS DATA:

OUTPUT INTERFACING NOTES

The tri-state outputs on this device exhibit three states:

"1" – low impedance to +5V
"0" – low impedance to -5V
OFF – high impedance = 10 megohm

The "off" state is controlled by the chip enable control inputs.

CUSTOM ROM ORGANIZATIONS

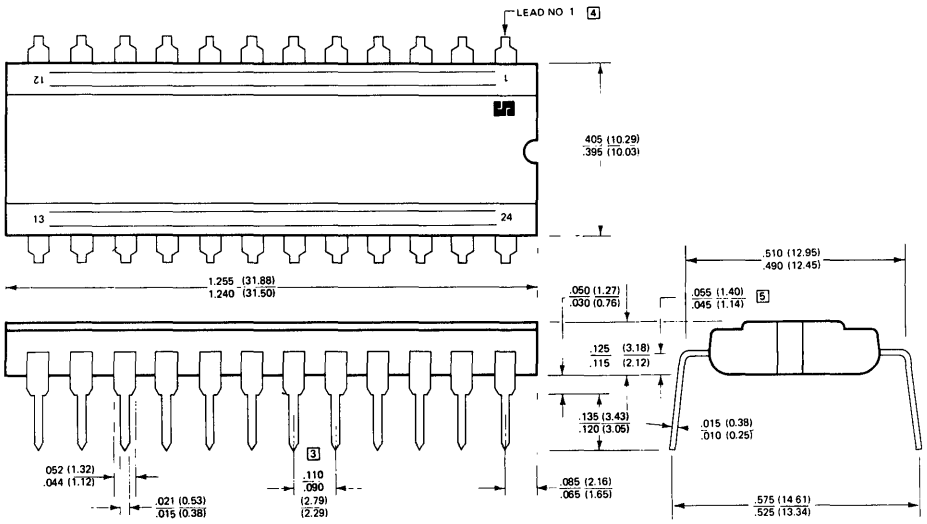
The 2516 is a static ROM with a total 64 x 6 x 8 bit capacity. This allows a standard 5 x 7 font to be encoded in the ROM, e.g., the 2516/CM2150 ASCII font standard product. Also custom coding of up to 6 x 8 character generators, also 256 x 8, 384 x 8, or 768 x 4 ROMs are available using Signetics "2516 Read Only Memory Software Package."

For applications requiring a 708 x 4 organization, CHIP ENABLE and CHIP ENABLE 2 are used to control outputs 1-4 and 5-8 respectively. The outputs are externally hard wired in pairs for this organization.

Custom versions of the 2516 can be supplied with a separate V_{DD} supply terminal for the output buffer. This feature permits operation at reduced power dissipation.

PACKAGE INFORMATION

N PACKAGE



NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: SILICONE MOLDED.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: Θ Ja = .12 C/mW, Θ Jc = .05 C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

HEX 32-HEX 40-BIT STATIC SHIFT REGISTERS

2518
2519

SILICON GATE MOS 2500 SERIES

DESCRIPTION

These Signetics 2500 Series Hex 32 and 40-bit recirculating static shift registers consists of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip. Internal recirculation logic plus TTL/DTL level clock signals are provided for maximum interfacing capability.

FEATURES

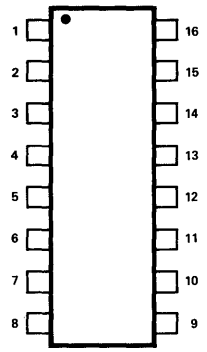
- TYPICAL CLOCK AND DATA RATE = 3MHz
- TTL/DTL COMPATIBLE CLOCK (SINGLE) PROVIDES EXTREMELY LOW CLOCK CAPACITANCE
- RECIRCULATION PATH ON CHIP
- TWO BIT LENGTHS AVAILABLE
- SINGLE-ENDED (BARE DRAIN) BUFFERS
- TTL, DTL COMPATIBLE SIGNALS
- STANDARD PACKAGE – 16 PIN SILICONE DIP
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST STATIC BUFFER MEMORIES
CRT REFRESH MEMORIES – LINE STORAGE
LINE PRINTERS
CARD EQUIPMENT BUFFERS

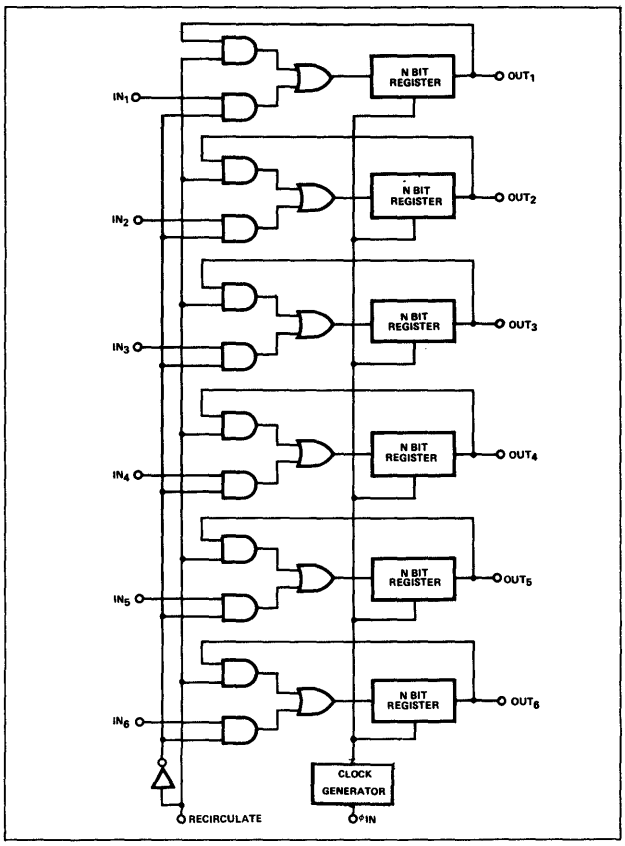
PIN CONFIGURATION (Top View)

B PACKAGE



1. IN_4
2. IN_5
3. IN_6
4. Recirculate
5. V_{GG}
6. Clock
7. OUT_6
8. OUT_5
9. OUT_4
10. OUT_3
11. OUT_2
12. OUT_1
13. IN_1
14. IN_2
15. IN_3
16. V_{CC}

BLOCK DIAGRAM



TRUTH TABLE

RECIRCULATE	INPUT	FUNCTION
1	0	Recirculate
1	1	Recirculate
0	0	"0" is Written
0	1	"1" is Written

PART IDENTIFICATION TABLE

PART NUMBER	BIT LENGTH	PACKAGE
2518B	HEX 32	16-Pin DIP
2519B	HEX 40	16-Pin DIP

MAXIMUM GUARANTEED RATINGS (1)

Operating Temperature (2)	0°C to +70°C
Storage Temperature	-65°C to +150°C
Package Power Dissipation at T_A = 70°C	640 mW
Data and Clock Input Voltages and Supply Voltages with Respect to V_{CC}	+0.3V to -20V

NOTES:

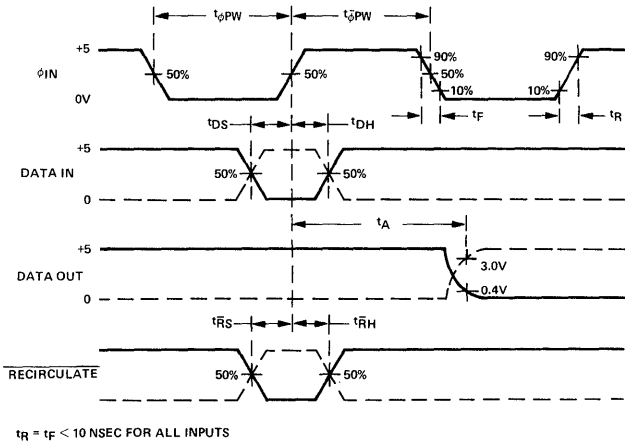
1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 125°C C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. V_{CC} tolerance is ±5% Any variation in actual V_{CC} will be tracked directly by V_{IL}. V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.
9. V_{OL} is dependent on R_L and characteristics of driven gate.

DC CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = +5V (8); V_{GG} = -12V ± 5% unless otherwise noted. (Notes: 3,4,5,6,7)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	INPUT LOAD CURRENT		10	500	nA	V_{in} = -5.5V, T_A = 25°C
I_{LO}	OUTPUT LEAKAGE CURRENT		10	1000	nA	T_A = 25°C
I_{LC}	CLOCK LEAKAGE CURRENT		10	500	nA	V_{ILC} = GND, T_A = 25°C
I_{GG}	POWER SUPPLY CURRENT		16	25	mA	CONTINUOUS OPERATION T_A = 25°C F = 2MHz
V_{IL}	INPUT "LOW" VOLTAGE			1.05	V	
V_{IH}	INPUT "HIGH"VOLTAGE	3.2		5.3	V	
V_{ILC}	CLOCK INPUT "LOW" VOLTAGE			1.05	V	
V_{IHC}	CLOCK INPUT "HIGH" VOLTAGE	3.2		5.3	V	

TIMING DIAGRAM



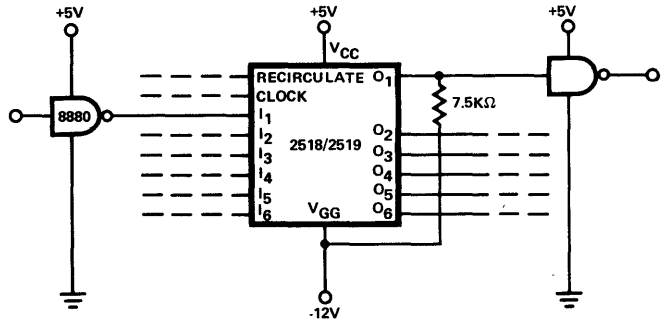
$t_R = t_F < 10$ NSEC FOR ALL INPUTS

Note: Input rise and fall times: 10nsec. Output load is 1 TTL gate.

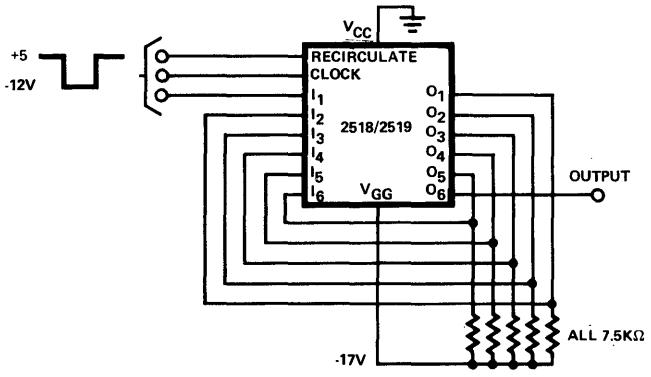
AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = +5V$; (8) $V_{GG} = -12V \pm 5\%$, $V_{ILC} = 0.4V$ to $4.0V$

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
FREQUENCY	CLOCK REP RATE	DC	3	2	MHz	See Max Frequency Curve
$t_{\phi PW}$	CLOCK PULSE WIDTH	.300		100	μsec	
t_R, t_F	CLOCK PULSE TRANSITION			5	μsec	
t_{OS}	DATA WRITE (SET-UP) TIME	100			nsec	
t_{DS}	DATA TO CLOCK HOLD TIME	50			nsec	
t_A	CLOCK TO DATA OUT DELAY		300	350	nsec	
t_{RS}	RECIRCULATE SET-UP TIME	150			ns	
t_{RH}	RECIRCULATE HOLD TIME	50			ns	
$\overline{t_{\phi PW}}$	CLOCK PULSE WIDTH	.200		DC	μsec	
C_{in}	INPUT CAPACITANCE		5	7	pF	@ 1MHz; $V_{in} = V_{CC}$; V_{AC} = 25mV p-p
$C\phi$	CLOCK CAPACITANCE		6	7	pF	@ 1MHz; $V_\phi = V_{CC}$; V_{AC} = 25mV p-p
V_{OL}	OUTPUT "LOW" VOLTAGE		0.4		V	Note 9
V_{OH}	OUTPUT "HIGH" VOLTAGE	3.6			V	$R_L = 7.5K\Omega$ to V_{GG}

APPLICATIONS INFORMATION



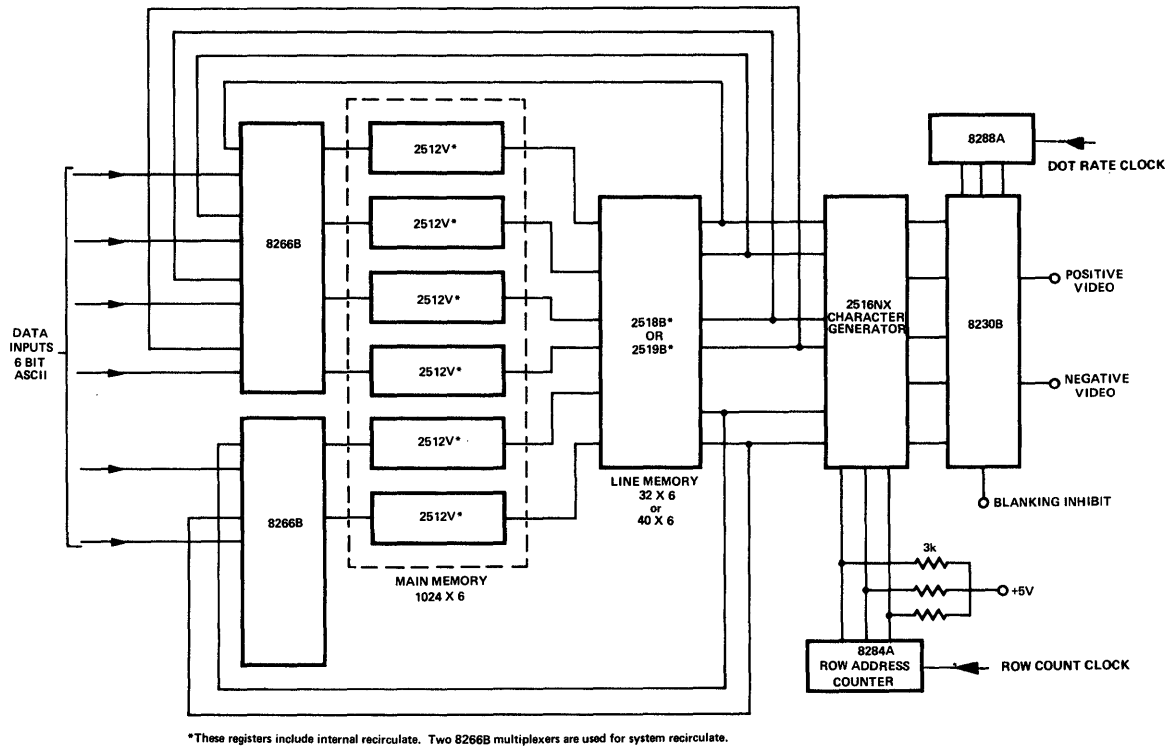
TTL INTERFACE



MOS INTERFACE

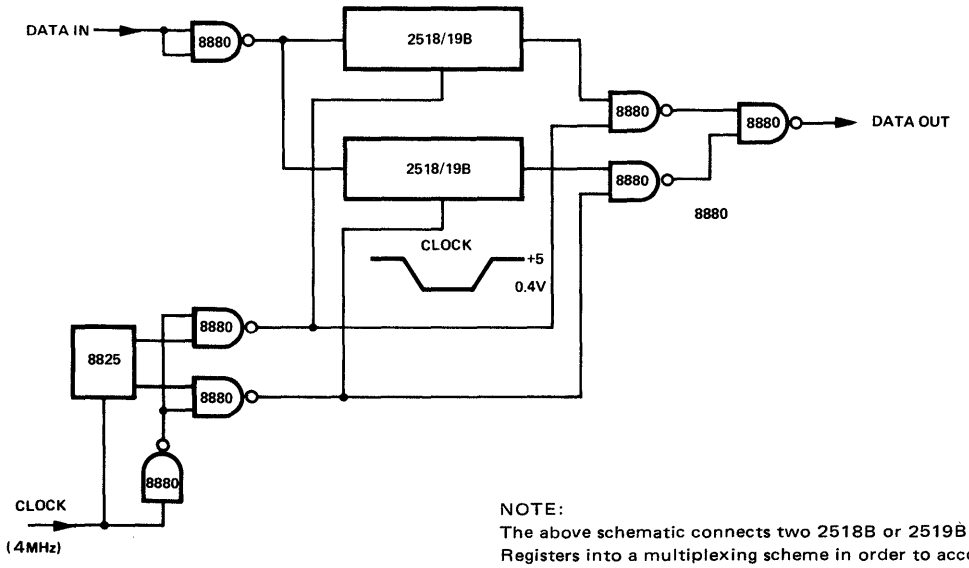
APPLICATIONS DATA

32 or 40 POSITION CRT DISPLAY MEMORY SYSTEM



*These registers include internal recirculate. Two 8266B multiplexers are used for system recirculate.

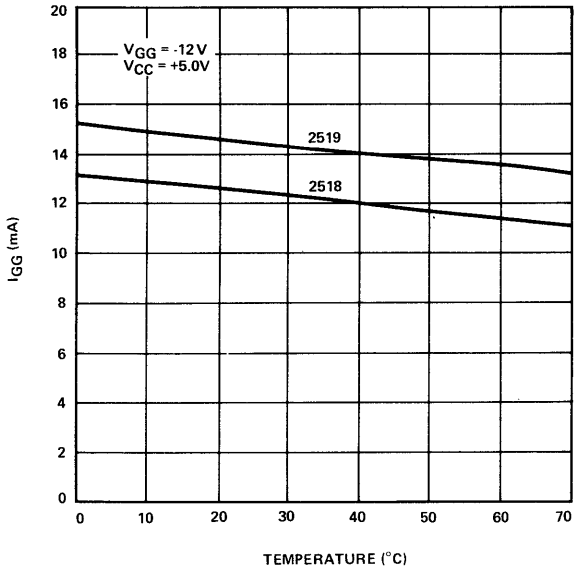
MULTIPLEXING LINE MEMORY REGISTERS AT 4MHz DATA RATE



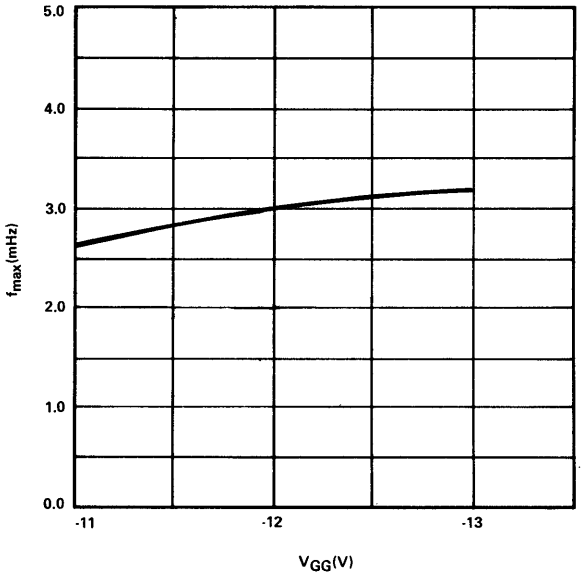
NOTE:
The above schematic connects two 2518B or 2519B Hex Shift Registers into a multiplexing scheme in order to accomplish a 64 or 80 character/line display at 4MHz data rate..

CHARACTERISTIC CURVES

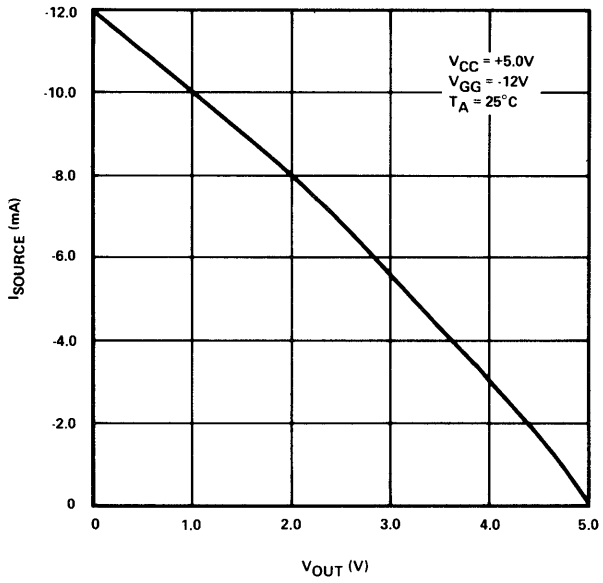
I_{GG} VERSUS TEMPERATURE



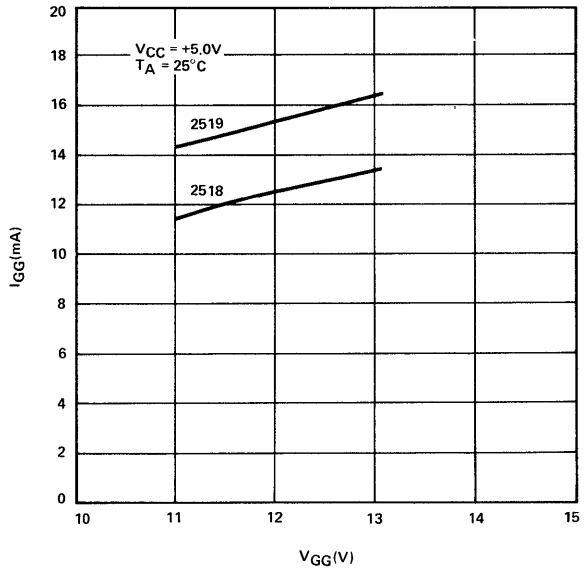
MAXIMUM SHIFT FREQUENCY VERSUS V_{GG}



I_{SOURCE} VERSUS V_{OUT}

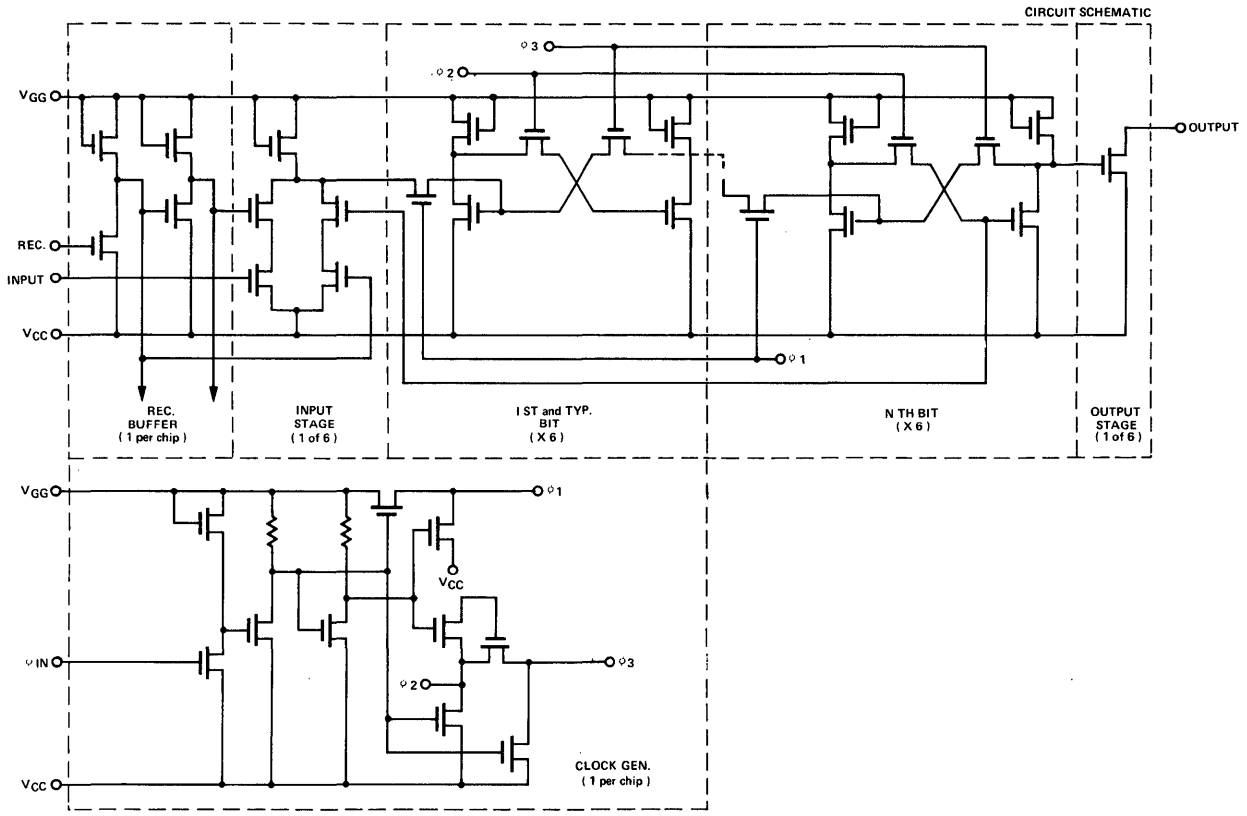


I_{GG} VERSUS V_{GG}



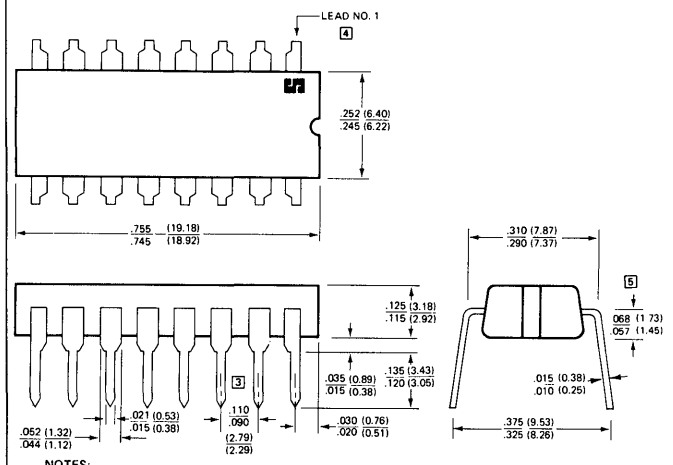
CIRCUIT SCHEMATIC

2518, 2519 STATIC REGISTER



PACKAGE INFORMATION

B PACKAGE



NOTES:

1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: SILICONE MOLDED.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: Θ Ja = .16°C/mW, Θ Jc = .08°C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

DUAL 128-132 BIT STATIC SHIFT REGISTERS

2521
2522

SILICON GATE MOS 2500 SERIES

DESCRIPTION

These Signetics 2500 Series Dual 128 and 132 bit recirculating static shift registers consist of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip.

FEATURES

- PUSH-PULL OUTPUTS
- TTL/DTL COMPATIBLE CLOCK – PROVIDES EXTREMELY LOW CLOCK CAPACITANCE
- RECIRCULATION PATH ON CHIP
- TWO BIT LENGTHS AVAILABLE
- HIGH FREQUENCY OPERATION – 2MHz TYPICAL CLOCK RATE
- TTL, DTL COMPATIBLE SIGNALS
- STANDARD PACKAGE – 8 LEAD SILICONE DIP
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

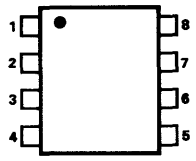
LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST STATIC BUFFER MEMORIES
CRT REFRESH MEMORIES – LINE STORAGE
LINE PRINTERS
CASSETTE RECORDERS

BIPOLAR COMPATIBILITY

The clock and signal inputs of these registers can be driven directly by standard bipolar integrated (TTL, DTL, etc.) or by MOS circuits.

PIN CONFIGURATION (Top View)

V PACKAGE



1. $\overline{\text{Recirculate}}$
2. IN_1
3. OUT_1
4. V_{GG}
8. V_{CC}
7. IN_2
6. OUT_2
5. ϕ_{IN}

TRUTH TABLE

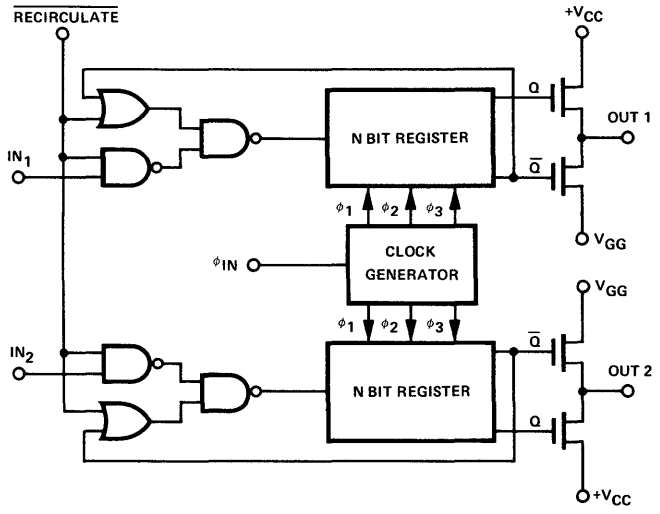
$\overline{\text{RECIRCULATE}}$	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is Written
1	1	"1" is Written

NOTE: "0" = 0V; "1" = +5V.

PART IDENTIFICATION TABLE

PART NUMBER	BIT LENGTH	PACKAGE
2521V	Dual 128	8 Pin DIP
2522V	Dual 132	8 Pin DIP

BLOCK DIAGRAM



MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature (2)	0°C to +70°C
Storage Temperature	-65°C to +150°C
Package Power Dissipation at T_A = 70°C	535 mW
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}	+0.3V to -20V

NOTES:

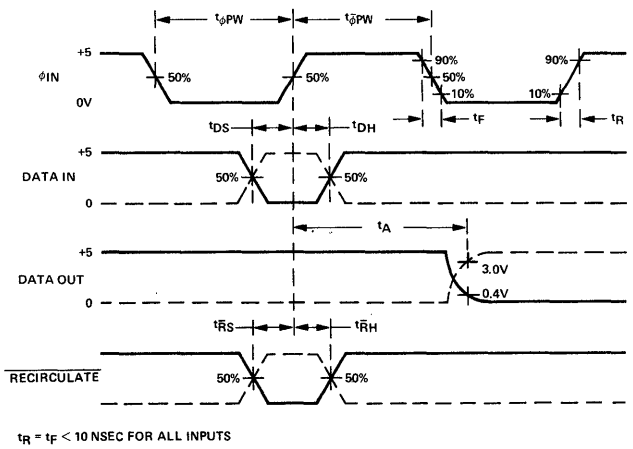
1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserving the right to make design and process changes and improvements.
7. Typical values are at +25°C and nomin. supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH}, and V_{OH} which are stated for a V_{CC} of exactly 5 volts.

DC CHARACTERISTICS T_A = 0°C to +70°C; V_{CC} = +5V(8); V_{GG} = -12V ±5% unless otherwise noted.

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	INPUT LOAD CURRENT		10	500	nA	V_{in} = 5.5V, T_A = 25°C
I_{LC}	CLOCK LEAKAGE CURRENT		10	500	nA	V_{ILC} = GND, T_A = 25°C
I_{GG}	POWER SUPPLY CURRENT		28	32	mA	CONTINUOUS OPERATION F = 1.5MHz, T_A=25°C
V_{IL}	INPUT "LOW" VOLTAGE			1.05	V	
V_{IH}	INPUT "HIGH" VOLTAGE	3.2		5.3	V	
V_{ILC}	CLOCK INPUT "LOW" VOLTAGE			1.05	V	
V_{IHC}	CLOCK INPUT "HIGH" VOLTAGE	3.2		5.3	V	

CONDITIONS OF TEST Input rise and fall times: 10 nsec. Output load is 1 TTL gate

TIMING DIAGRAM



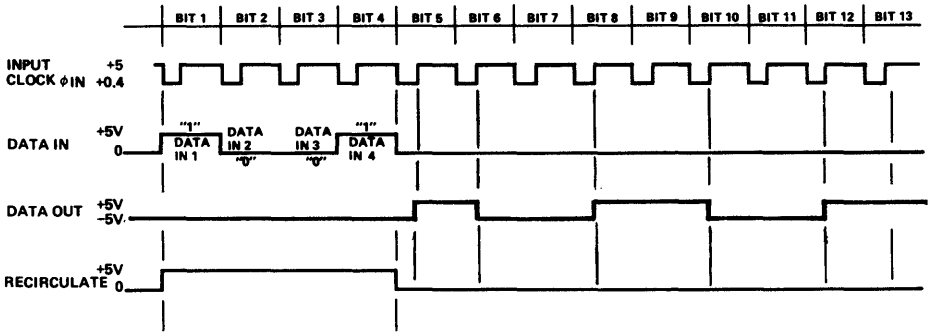
$t_R = t_F < 10$ NSEC FOR ALL INPUTS

AC CHARACTERISTICS $T_A = 25°C, V_{CC} = +5V(8); V_{GG} = -12V \pm 5\%, V_{IC}=0.4$ to 4.0

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
FREQUENCY	CLOCK REP RATE	DC		1.5	MHz	See Maximum Frequency Curve
$t\phi_{PW}$	CLOCK PULSE WIDTH	.350	.100	100	μsec	
$t_{\phi PW}$	CLOCK PULSE WIDTH	.200		DC	μsec	
t_R, t_F	CLOCK PULSE TRANSITION			1	usec	
t_{DW}	DATA WRITE (SET-UP) TIME	75			nsec	
t_{DS}	DATA TO CLOCK HOLD TIME	50			nsec	
t_A	CLOCK TO DATA OUT DELAY		250	350	nsec	
t_{RS}	RECIRCULATE SET-UP TIME	50			ns	
t_{RH}	RECIRCULATE HOLD TIME	50			ns	
C_{IN}	INPUT CAPACITANCE			5	pF	@ 1MHz; $V_{in} = V_{CC}$; V_{AC} = 25mV p-p
$C\phi$	CLOCK CAPACITANCE			5	pF	@ 1MHz; $V_\phi = V_{CC}$; V_{AC} = 25mV p-p
V_{OL}	OUTPUT "LOW" VOLTAGE	-4.0		0.4	V	1 TTL load (I_L=1.6mA)
V_{OH1}	OUTPUT "HIGH" VOLTAGE DRIVING 1 TTL LOAD	3.0	3.5		V	1 TTL load (I_1 = 100μA)
V_{OH2}	OUTPUT "HIGH" VOLTAGE DRIVING MOS	3.5	4.0		V	

TIMING DIAGRAM

4 BIT RECIRCULATING SHIFT REGISTER *

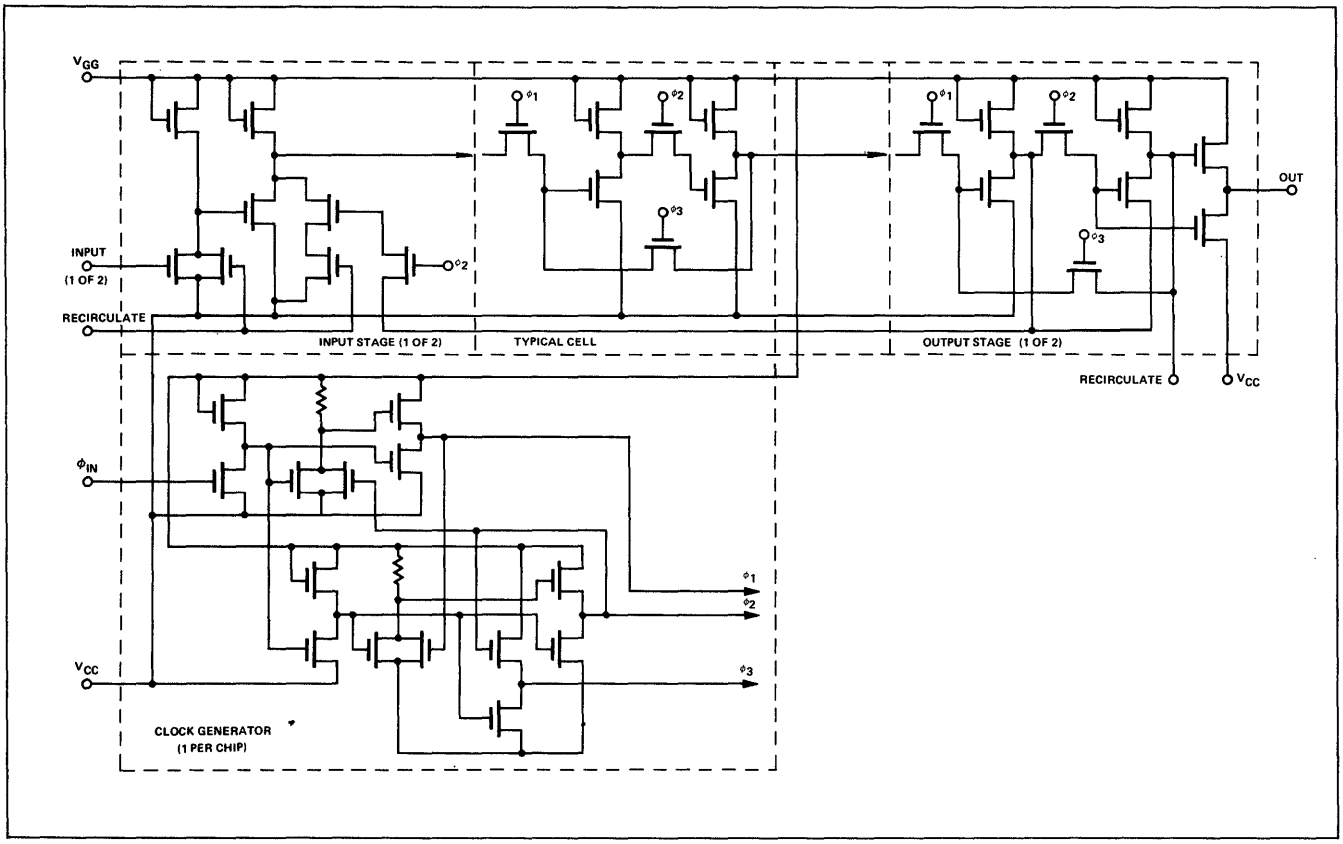


NOTE 1: WRITE CYCLE
The positive going edge of the recirculative control is coincident with the negative going edge of the input clock (ϕ_{IN}).

NOTE 2: RECIRCULATE CYCLE
Data recirculates if the recirculate control is a "0"

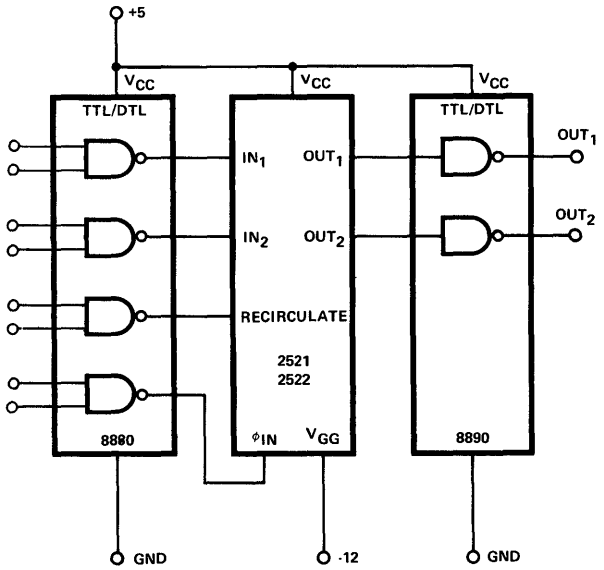
*For clarity, a four bit hypothetical example is shown

SCHEMATIC DIAGRAM



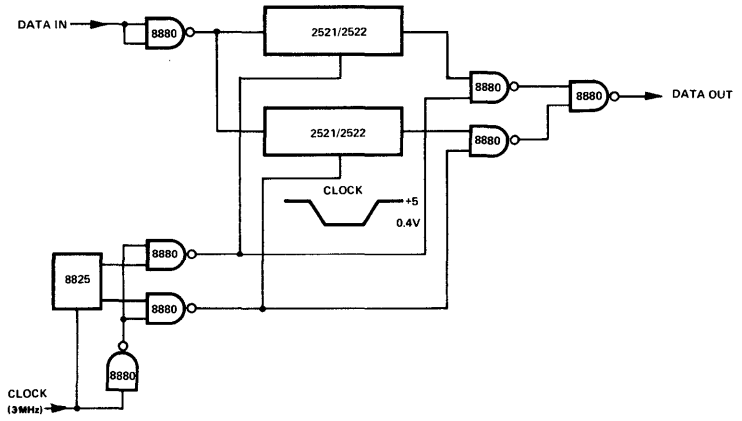
APPLICATIONS DATA

TTL/DTL/MOS INTERFACES



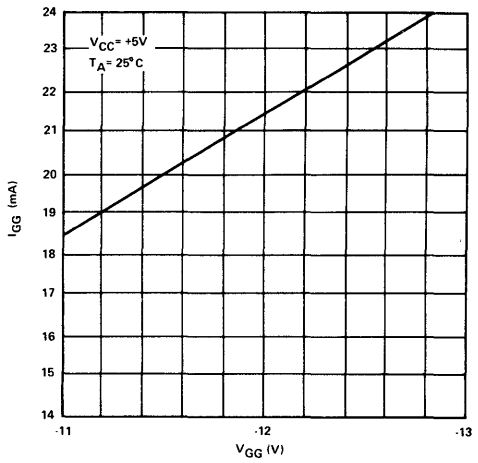
APPLICATIONS INFORMATION

MULTIPLEXING LINE MEMORY REGISTERS AT 3MHz DATA RATE

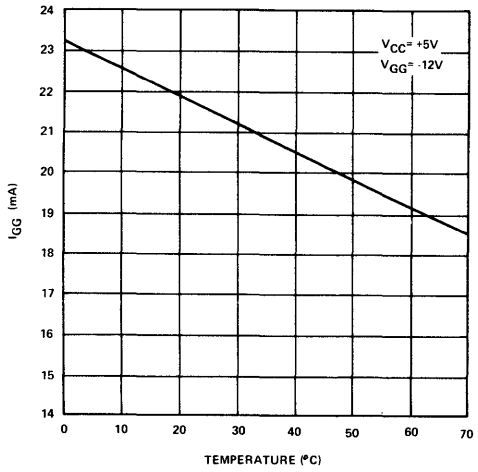


CHARACTERISTIC CURVES

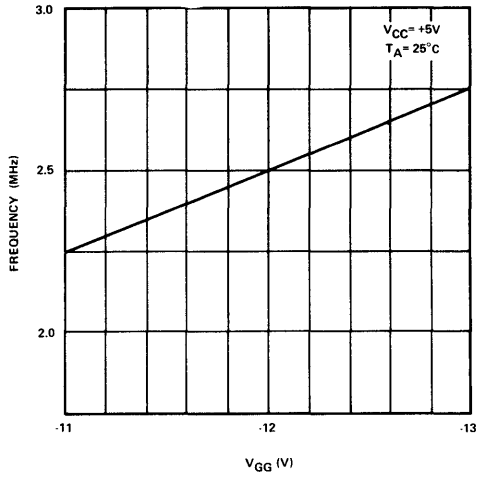
POWER SUPPLY CURRENT VERSUS POWER SUPPLY VOLTAGE



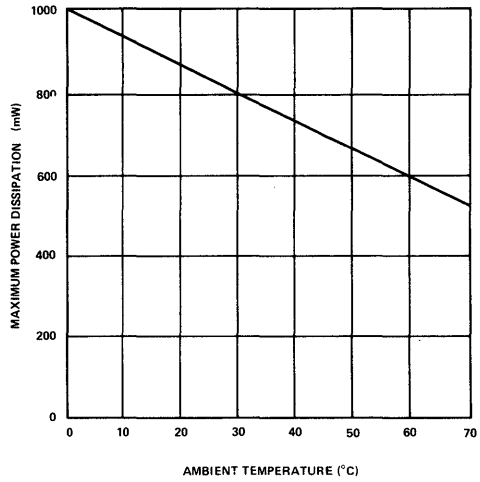
POWER SUPPLY CURRENT VERSUS TEMPERATURE



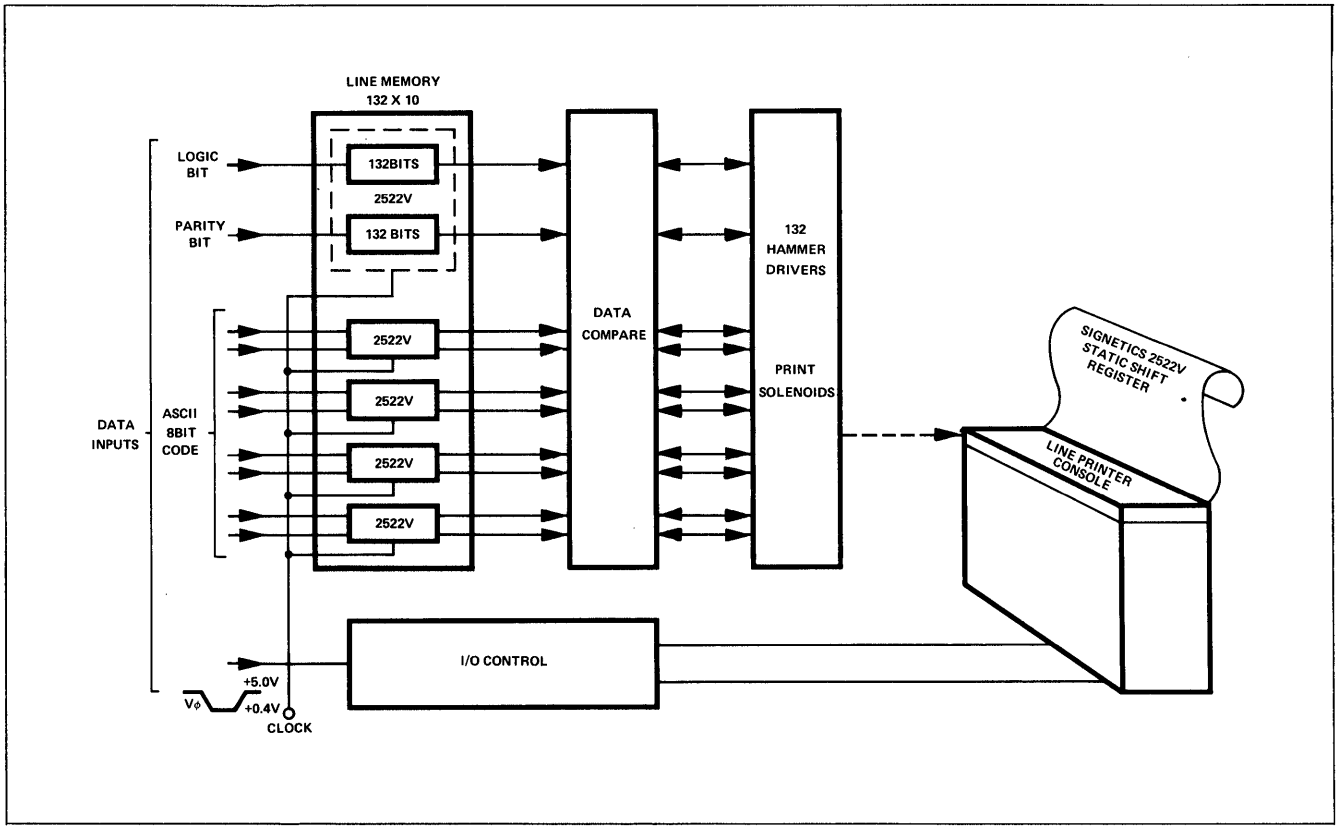
TYPICAL OPERATING FREQUENCY VERSUS SUPPLY VOLTAGE



PACKAGE MAXIMUM POWER DISSIPATION

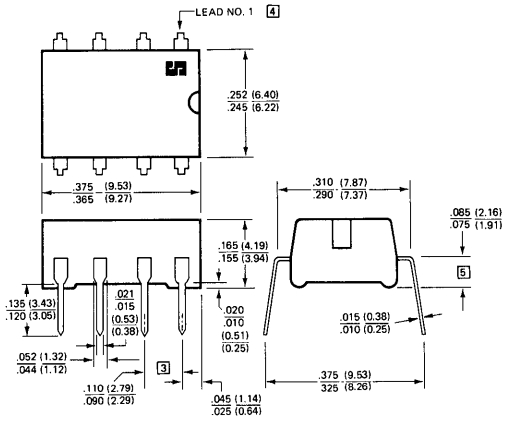


132 COLUMN LINE PRINTER



PACKAGE INFORMATION

V PACKAGE



NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: SILICONE MOLDED.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: θ Ja = .16 C/mW, θ Jc = .08 C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

512 AND 1024 BIT RECIRCULATING DYNAMIC SHIFT REGISTERS

2524
2525

SILICON GATE MOS 2500 SERIES

DESCRIPTION

These Signetics 2500 Series 512 and 1024 bit recirculating dynamic shift registers consist of enhancement mode P-channel MOS devices integrated on a single monolithic chip. Internal recirculation logic plus write and read controls are included on the chip.

FEATURES

- HIGH FREQUENCY OPERATION-5 MHz Typical Clock Rate
- SINGLE 512, SINGLE 1024
- TTL, DTL COMPATIBLE
- WRITE AND READ CONTROLS INCLUDED
- LOW POWER DISSIPATION-150μW/bit at 1 MHz
- LOW CLOCK CAPACITANCE-80pF for 512, 160pF for 1024 Bits
- +5, -5 POWER SUPPLIES
- STANDARD PACKAGE 8-LEAD DIP
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

FAST ACCESS SWAPPING MEMORY SYSTEMS
LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST BUFFER MEMORIES
CRT REFRESH MEMORIES
DELAY LINE MEMORY REPLACEMENT
DRUM MEMORY REPLACEMENT

PROCESS TECHNOLOGY

Use of low threshold *silicon gate technology* allows high speed (5MHz typical) while reducing power dissipation and clock input capacitance dramatically as compared to other technologies. The use of low voltage circuitry minimizes power dissipation and facilitates interfacing with bipolar integrated circuits.

BIPOLAR COMPATIBILITY

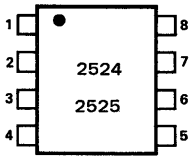
The signal inputs of these registers can be driven directly by standard bipolar integrated (TTL, DTL, etc.) or by MOS circuits. The bare drain output stage provides driving capability for both MOS and bipolar integrated circuits (one standard TTL load).

SILICONE PACKAGING

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric material over the silicon gate-oxide-substrate structure provides an ion barrier. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability and demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers.

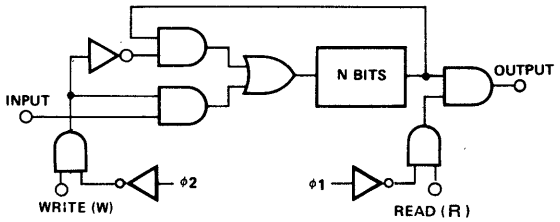
PIN CONFIGURATION (Top View)

V PACKAGE



1. ϕ_2 Input clock
2. Output
3. Read
4. V_{DD}
8. V_{CC}
7. ϕ_1 Output clock
6. Input
5. Write

BLOCK DIAGRAM



NOTE
N = 512 or 1024 '0' = 0V, '1' = +5V.

TRUTH TABLE

WRITE	READ	FUNCTION
0	0	Recirculate, Output is '0'
0	1	Recirculate, Output is Data
1	0	Write Mode, Output is '0'
1	1	Read Mode Output is Data

PART IDENTIFICATION TABLE

PART NO.	BIT LENGTH	PACKAGE
2524V	512	8 pin DIP
2525V	1024	8 pin DIP

MAXIMUM GUARANTEED RATINGS (1)

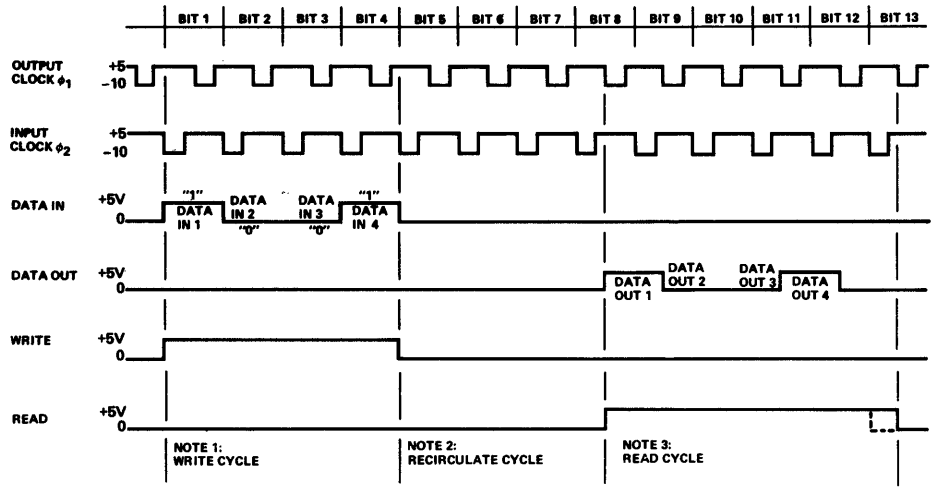
Operating Ambient Temperature (2)	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation (2)	535mW@T_A>70°C
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}	+ 0.3V to −20V

NOTES:
1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
3. All inputs are protected against static charge.
4. See "Minimum Operating Frequency" graph for low limits on data rep. rate.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserving the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. Parameters are valid over operating temperature range unless otherwise specified.
9. V_{CC} tolerance is ± 5%. Any variation is actual V_{CC} will be tracked directly by V_{IL}, V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.
10. V_{OL} is a function of the input characteristics of the driven TTL/DTL gate I_{OI} and V_{CLAMP} and the value of the pull-down resistor (R_L).

DC CHARACTERISTICS T_A = 0°C to +70°C; V_{CC} = +5V(9); V_{DD} = 5V ±5% unless otherwise noted.

SYMBOL	TEST	MIN	TYPICAL	MAX	UNIT	CONDITION
I_{LI}	Input Load Current		10	500	nA	V_{IN} =-5.5V; T_A = 25°C
I_{LO}	Output Leakage Current		10	1000	nA	$V_{\phi1}$ = $V_{\phi2}$ = -12V; V_{DD} = -5 V_{OUT} =-5.5V; T_A = 25°C
I_{LC}	Clock Leakage Current		10	1000	nA	V_{ILC} = -12V ; T_A = 25°C
I_{DD}	Power Supply Current: 2524		15	35	mA	Continuous Operation; ϕpW = 150nS; 1MHz
	2525		25	35	mA	V_{ILC} = -12V; T_A = 25°C V_{DD} = -5.5V
V_{IL}	Input "Low" Voltage	-5.0		1.05	V	
V_{IH}	Input "High" Voltage	3.2		5.3	V	
V_{ILC}	Clock Input "Low" Voltage	-12.0		-10.0	V	
V_{IHC}	Clock Input "High" Voltage	4.0		5.3	V	

TIMING DIAGRAM



NOTE:
This is a simplified illustration of the timing of a 4 bit recirculating shift register showing the 3 basic modes of operation.

NOTE 1: (WRITE cycle)

The positive and negative going edge of the "Write" control is coincident with the negative going edge of the input clock (ϕ_2). The "Read" control may be either "1" or "0"

NOTE 2: (RECIRCULATE cycle)

Data recirculates if the "Write" control line is "0". "Read" may be either "1" or "0".

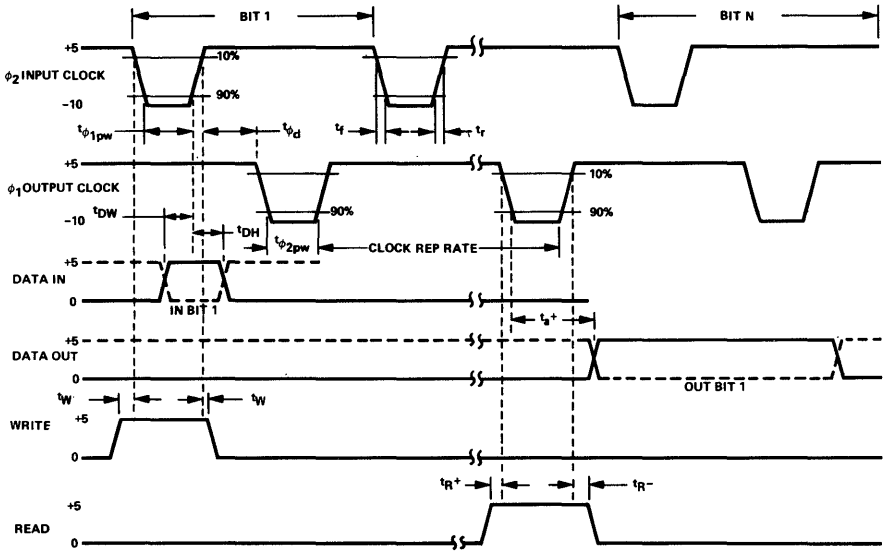
NOTE 3: (READ cycle)

The positive going edge of the "Read" control is coincident with the negative edge of the output clock (ϕ_1). The negative going edge of "Read" is coincident with the negative going edge of either clock pulse succeeding the last desired data output bit. "Write" may be either "1" or "0".

CONDITIONS OF TEST

Input rise and fall times: 10 sec Output load is 1 TTL gate

TIMING DIAGRAM



NOTE:

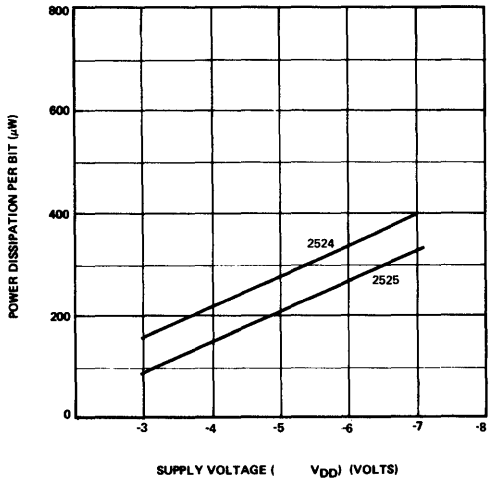
1. N = 512 for 2524 N= 1024 for 2525
2. Note that the Read Input is AND'ed with $\overline{\phi}_1$; therefore this function is not valid until ϕ_1 occurs.

AC CHARACTERISTICS $T_A = +25°C$ $V_{CC} = +5V(9)$; $V_{DD} = -5V \pm 5\%$; $V_{ILC} = -11V$

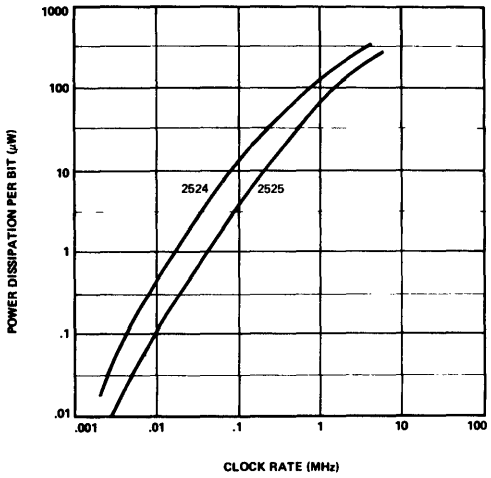
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
Frequency	Clock Data Rep Rate	.0005 (Note 4)	5	3	MHz	W = R = V_{CC}
$t_{\phi pw}$	Clock Pulse Width	135	85		ns	
$t_{\phi d}$	Clock Pulse Delay	10			ns	
t_r;t_f	Clock Pulse Transition	10		1000	ns	
t_{DW}	Data Write (Setup) Time	70			ns	
t_{DH}	Data to Clock Hold Time	20			ns	
t_{a+}	Clock to Data Out Delay			100	ns	
t_{R-}; t_{W-}	Clock to "Read" or "Write" Timing	0			ns	
t_{R-}; t_{W+}	Clock to "Read" or "Write" Timing	0			ns	
C_{in}	Input Capacitance			5	pF	1MHz; V_I=V_{CC};V_{AC}=25m V_{P-P}
C_{out}	Output Capacitance			5	pF	1MHz; V_0=V_{CC};V_{AC}=25m V_{P-P}
C_ϕ	Clock Capacitance 2524 2525			 80 160	 pF pF	1MHz; V=V_{CC}; V_{AC}=25m V_{P-P}
V_{OL}	Output "Low" Voltage		-1.0		V	R_L =3.0K; 1 TTL Load (I_L = 1.6mA) Note 10
V_{OHI}	Output "High" Voltage Driving 1 TTL Load	2.4	3.5		V	R_L=3.0K; 1 TTL Load (I_L=100μA)
V_{OH2}	Output "High" Voltage Driving MOS	3.6	4.0		V	R_L = 5.6K; C_L = 10pF

CHARACTERISTIC CURVES

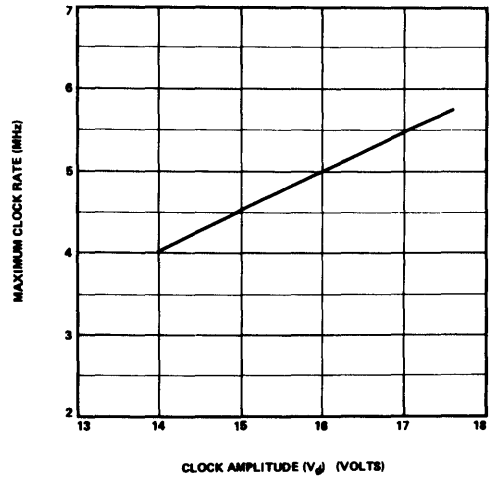
POWER DISSIPATION/BIT VERSUS SUPPLY VOLTAGE



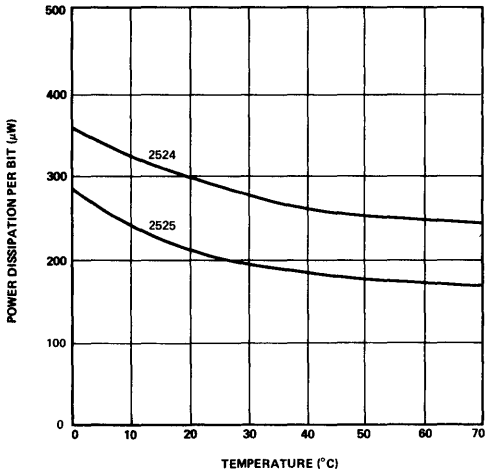
POWER DISSIPATION/BIT VERSUS CLOCK RATE



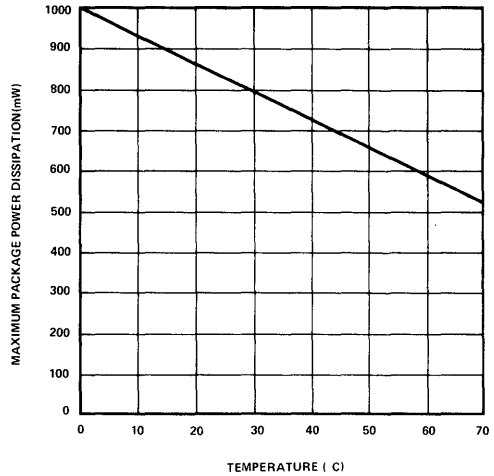
MAXIMUM CLOCK RATE VERSUS CLOCK AMPLITUDE



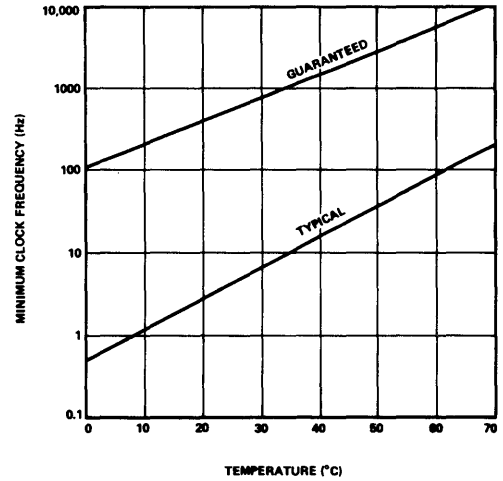
POWER DISSIPATION/BIT VERSUS TEMPERATURE



MAXIMUM PACKAGE POWER DISSIPATION VERSUS TEMPERATURE



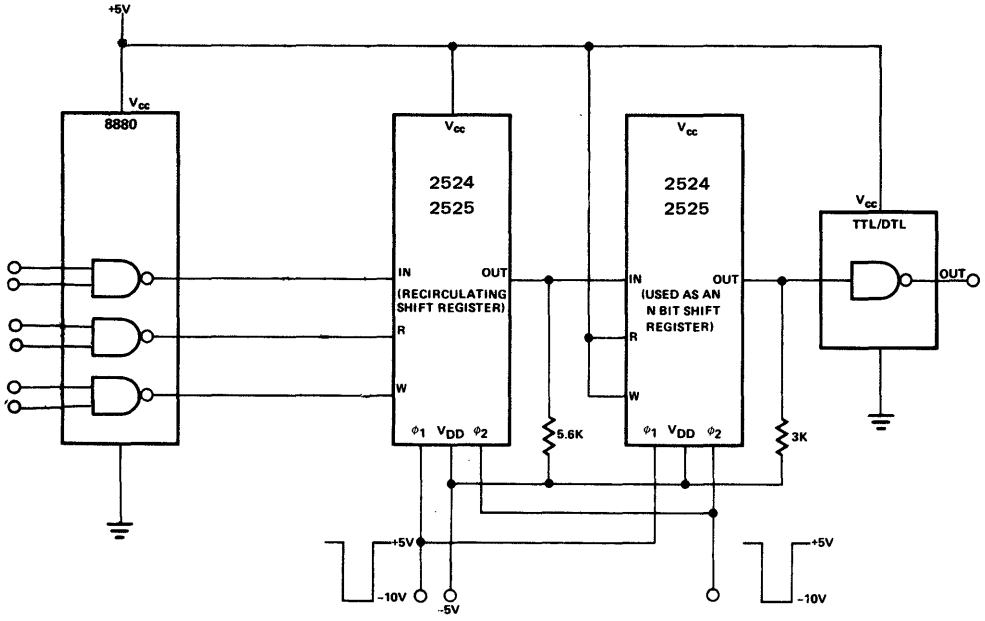
MINIMUM OPERATING CLOCK FREQUENCY VERSUS TEMPERATURE



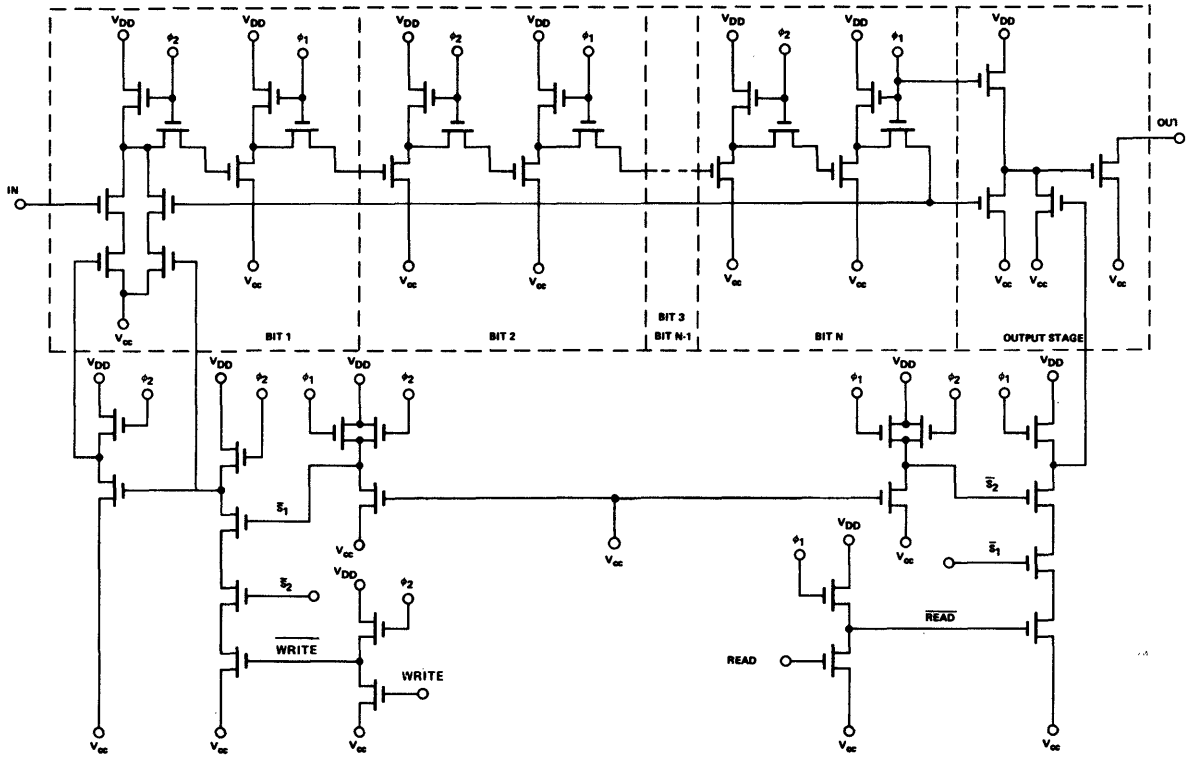
NOTE:
Conditions for typical curves: V_{CC} = +5V, V_{DD} = -5V, clock duty cycle = 35%, f_{CLK} = 3MHz, $V\phi_{p\text{-}p}$ = 16V, $\phi_{PW1} = \phi_{PW2}$ = 80ns, T_A = +25°C unless otherwise noted.

APPLICATIONS DATA

TTL/DTL/MOS INTERFACES



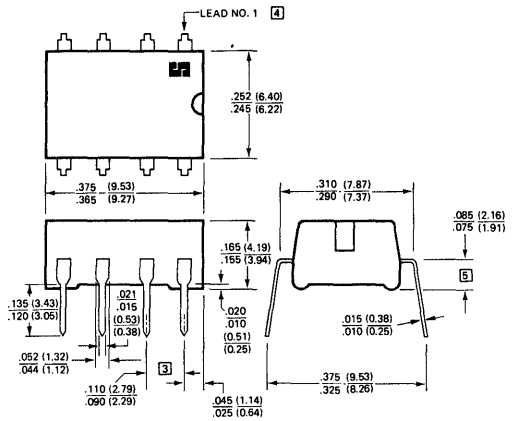
CIRCUIT SCHEMATIC



NOTE
N = 512 for 2524
N = 1024 for 2525

PACKAGE INFORMATION

V PACKAGE



NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: SILICONE MOLDED.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: Θ Ja = .16 C/mW, Θ Jc = .08 C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

DUAL 256-250-240 BIT STATIC SHIFT REGISTERS

PRELIMINARY SPECIFICATION

SILICON GATE 2500 SERIES

2527
2528
2529

DESCRIPTION

The Signetics 2500 Series Dual 256, 250 and 240 bit recirculating static shift registers consist of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip.

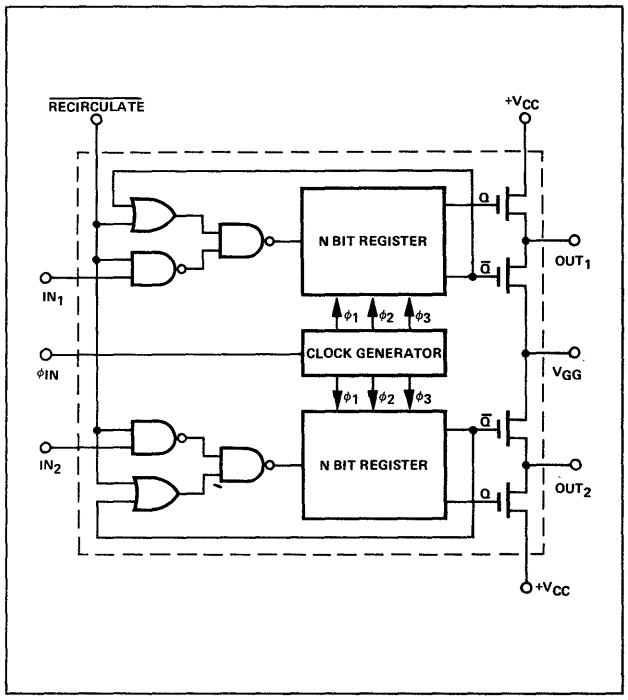
FEATURES

- PUSH-PULL OUTPUTS
- TTL/DTL COMPATIBLE CLOCK – PROVIDES EXTREMELY LOW CLOCK CAPACITANCE
- RECIRCULATION PATH ON CHIP
- THREE BIT LENGTHS AVAILABLE
- HIGH FREQUENCY OPERATION – 3 MHz TYPICAL CLOCK & DATA RATE
- TTL, DTL COMPATIBLE INPUTS AND OUTPUTS
- STANDARD PACKAGE – 8 LEAD SILICONE DIP
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST STATIC BUFFER MEMORIES
CRT REFRESH MEMORIES – LINE STORAGE
DELAY LINES
CASSETTE RECORDERS

BLOCK DIAGRAM

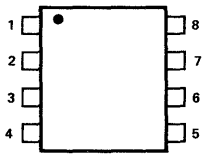


BIPOLAR COMPATIBILITY

The clock and signal inputs of these registers can be driven directly by standard bipolar integrated (TTL, DTL, etc.) or by MOS circuits. The outputs drive directly into TTL/DTL without requiring external resistors.

PIN CONFIGURATION (Top View)

V PACKAGE



1. $\overline{\text{Recirculate}}$
2. IN_1
3. OUT_1
4. V_{GG}
5. ϕ_{IN}
6. OUT_2
7. IN_2
8. V_{CC}

TRUTH TABLE

$\overline{\text{RECIRCULATE}}$	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is Written
1	1	"1" is Written

NOTE: "0" = 0V; "1" = +5V

PART IDENTIFICATION TABLE

PART NUMBER	BIT LENGTH	PACKAGE
2527V	Dual 256	8 Pin DIP
2528V	Dual 250	8 Pin DIP
2529V	Dual 240	8 Pin DIP

MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature (2)	0°C to +70°C
Storage Temperature	-65°C to +150°C
Package Power Dissipation at T_A = 70°C	535 mW
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}	+0.3V to -20V

NOTES:
1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH}, and V_{OH} which are stated for a V_{CC} of exactly 5 volts.

DC CHARACTERISTICS T_A = 0°C to +70°C; V_{CC} = +5V (8); V_{GG} = -12V ±5% unless otherwise noted.

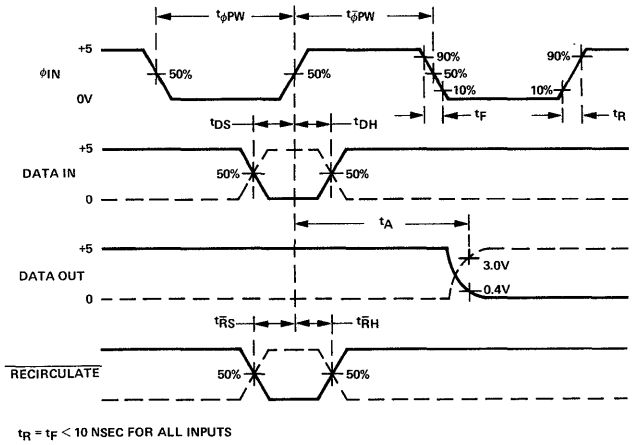
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} = 5.5V, T_A = 25°C
I_{LC}	Clock Leakage Current		10	500	nA	V_{ILC} = 0V, T_A = 25°C
I_{GG}	Power Supply Current		28	35	mA	Continuous Operation F = 2.5 MHz, T_A = 25°C Outputs Open
V_{IL}	Input "Low" Voltage			1.05	V	
V_{IH}	Input "High" Voltage	3.2		5.3	V	
V_{ILC}	Clock Input "Low" Voltage			1.05	V	
V_{IHC}	Clock Input "High" Voltage	3.2		5.3	V	

AC CHARACTERISTICS T_A = 25°C, V_{CC} = +5V (8); V_{GG} = -12V ±5%, V_{IC} = 0.4 to 4.0V

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
FREQUENCY	Clock Rep Rate	DC	3.0	2.5	MHz	See Maximum Frequency Curve
$t_{\phi PW}$	Clock Pulse Width	0.2	0.1	100	μs	
$t_{\overline{\phi} PW}$	$\overline{\text{Clock}}$ Pulse Width	0.2		DC	μs	
t_R t_F	Clock Pulse Transition			1	μs	
t_{DS}	Data Set-up Time	50			ns	
t_{DH}	Data Hold Time	50			ns	
t_A	Clock to Data Out Delay		250	330	ns	
$t_{\overline{RS}}$	$\overline{\text{Recirculate}}$ Set-up Time	50			ns	
$t_{\overline{RH}}$	$\overline{\text{Recirculate}}$ Hold Time	50			ns	
C_{IN}	Input Capacitance			5	pF	@ 1 MHz; V_{IN} = V_{CC}; V_{AC} = 25mV p-p
C_ϕ	Clock Capacitance			5	pF	@ 1 MHz; V_ϕ = V_{CC}; V_{AC} = 25mV p-p
V_{OL}	Output "Low" Voltage			0.4	V	1 TTL load (I_L = 1.6mA)
V_{OH1}	Output "High" Voltage Driving 1 TTL Load	3.0	3.5		V	1 TTL load (I_I = 100μA)
V_{OH2}	Output "High" Voltage Driving MOS	3.5	4.0		V	

CONDITIONS OF TEST Input rise and fall times: 10 nsec. Output load is 1 TTL gate.

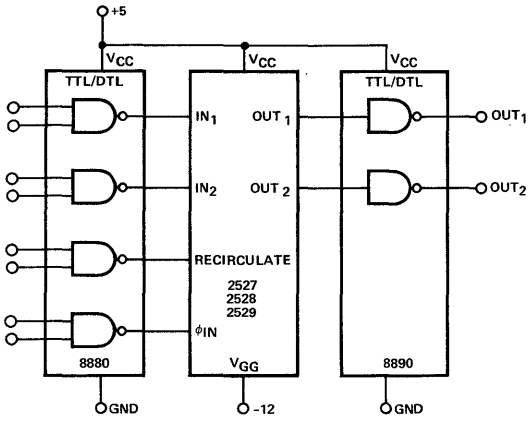
TIMING DIAGRAM



$t_R = t_F < 10$ NSEC FOR ALL INPUTS

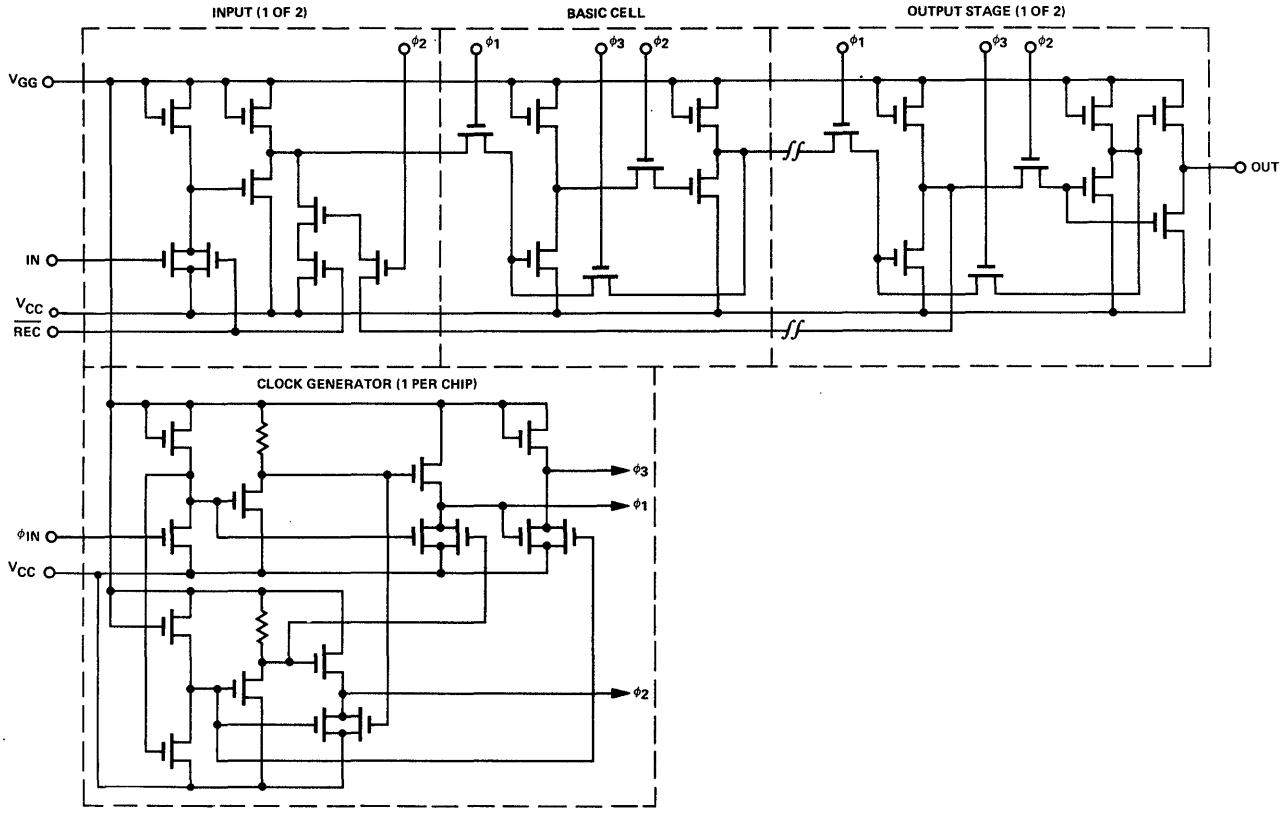
APPLICATIONS INFORMATION

TTL/DTL/MOS INTERFACES

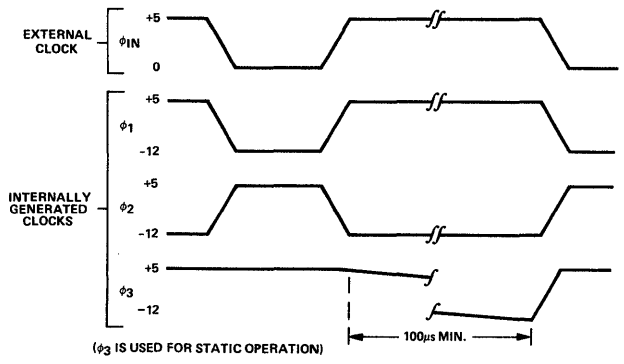


Note: When using 7400 series data, recirculate and clock drivers, connect 10k resistor from driver output to V_{CC}. This insures an adequate "1" level input for the MOS register. See page 13 of MOS Handbook.

SCHEMATIC DIAGRAM

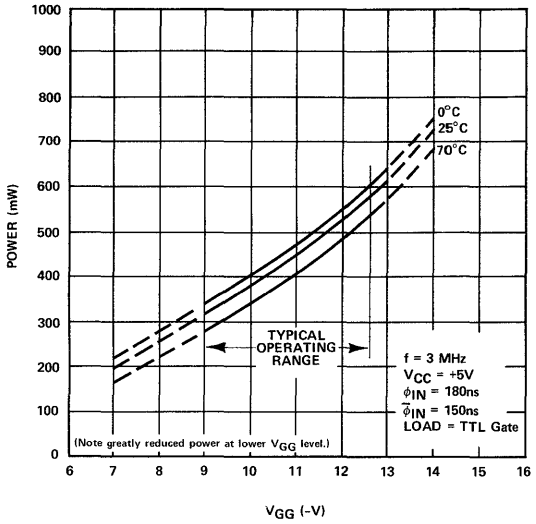


CLOCKING WAVEFORMS

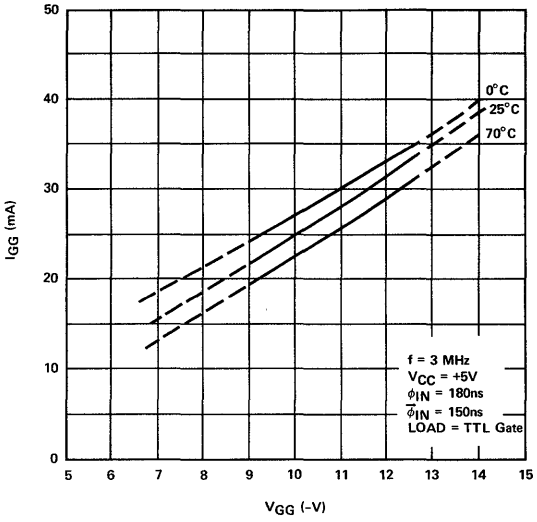


CHARACTERISTIC CURVES

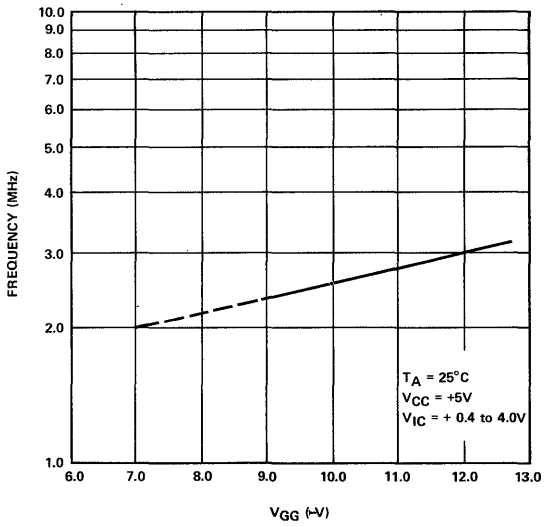
POWER DISSIPATION VS SUPPLY VOLTAGE



SUPPLY CURRENT VS SUPPLY VOLTAGE

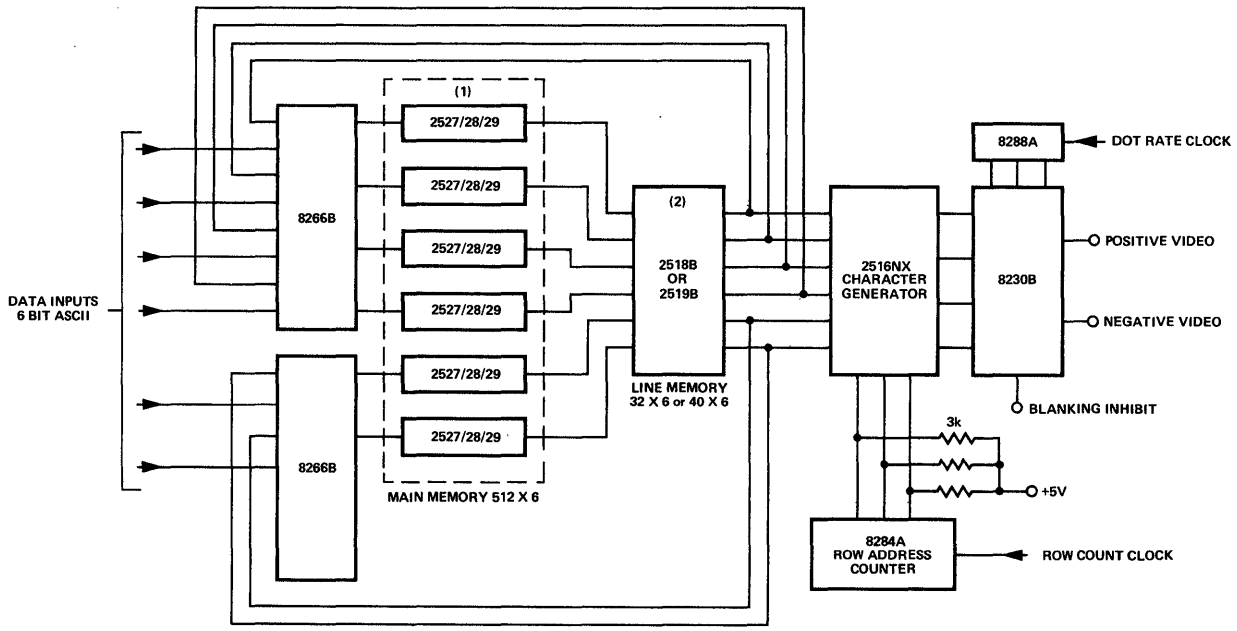


TYPICAL DATA RATE VS SUPPLY VOLTAGE



APPLICATIONS INFORMATION (Cont'd)

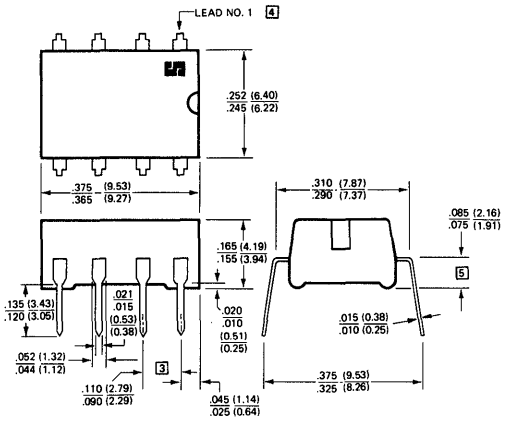
12 LINE, 32 OR 40 CHARACTER PER LINE CRT DISPLAY MEMORY SYSTEM



(1) Duals connected in series.
(2) These registers include internal recirculate. Two 8266B multiplexers are used for system recirculate.

PACKAGE INFORMATION

V PACKAGE



NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: SILICONE MOLDED.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: Θ Ja = .16 C/mW, Θ Jc = .08 C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

HIGH SPEED 64 x 9 x 9 STATIC CHARACTER GENERATOR

2526

ADVANCE SPECIFICATION

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The 2526 is a high speed 5,184-bit Static Read-Only Memory available in a 64x9x9 organization. This device has TTL compatible inputs and outputs and requires +5V and −12V power supplies. A $\overline{\text{READ}}$ input controls the entry of data from the ROM into output latches. Three-state outputs allow OR tying for implementing larger memories. OUTPUT ENABLE controls the nine output devices without affecting address circuitry.

FEATURES

- 64x9x9 ORGANIZATION
- 450ns TYPICAL ACCESS TIME
- STATIC OPERATION
- OUTPUT LATCHES
- TTL/DTL COMPATIBLE INPUTS
- TTL/DTL COMPATIBLE THREE-STATE OUTPUTS
- V_{CC} = +5V, V_{GG} = −12V
- 24-PIN SILICONE DIP
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

VERTICAL OR RASTER SCAN DISPLAYS (7x9 MATRIX)
PRINTER CHARACTER GENERATOR
PANEL DISPLAYS AND BILLBOARDS
MICRO-PROGRAMMING
CODE CONVERSION

BIPOLAR COMPATIBILITY

All inputs of the 3940 can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.). The data output buffers are capable of sinking a minimum of 1.6mA sufficient to drive one standard TTL load.

STANDARD TRUTH TABLES

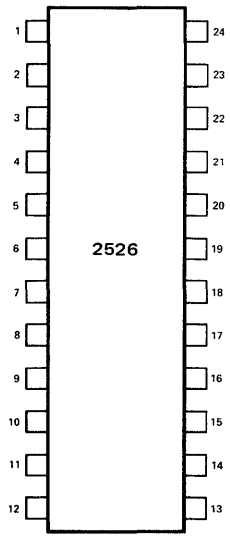
The 2526NX/CM3530 is a 7x9 matrix, ASCII character set (raster scan) utilizing the two unused left-most columns for BCDIC-ASCII and BAUDOT-ASCII code converters. Use this device for evaluation or for suitable application. Other standards will be announced as they become available.

CUSTOM TRUTH TABLES

Ask your Signetics Representative for recommended coding format.

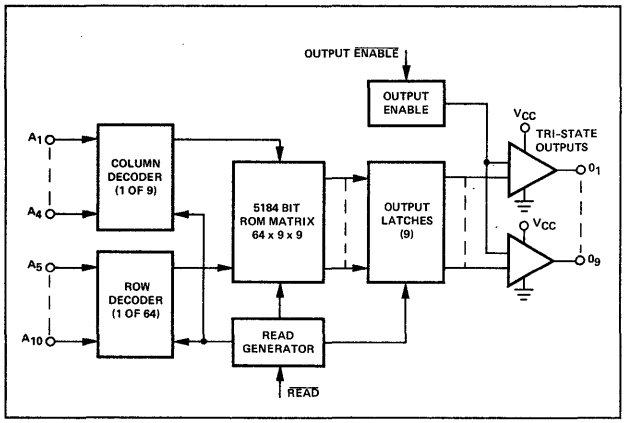
PIN CONFIGURATION (Top View)

NX PACKAGE



1.	Output 6	24.	V_{CC}
2.	Output 7	23.	Output 5
3.	Output 8	22.	Output 4
4.	Output 9	21.	Output 3
5.	Ground	20.	Output 2
6.	Address 4	19.	Output 1
7.	Address 3	18.	$\overline{\text{Read}}$
8.	Address 2	17.	Address 10
9.	Address 1	16.	Address 9
10.	Output Enable	15.	Address 8
11.	Address 5	14.	Address 7
12.	V_{GG}	13.	Address 6

BLOCK DIAGRAM



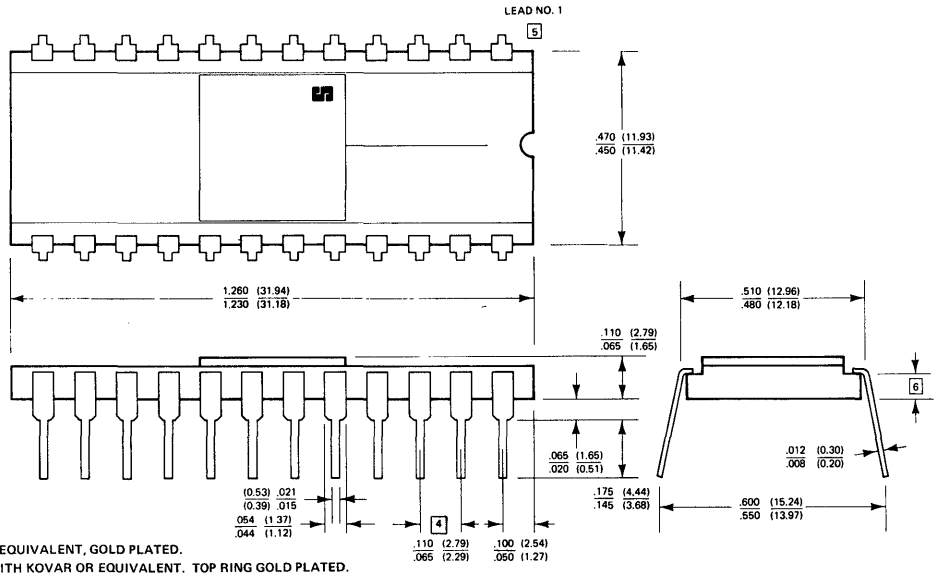
PART IDENTIFICATION

PART NUMBER	OP. TEMP. RANGE	PACKAGE
2526N	0-70°C	24-Pin DIP

NOTE: "0" = 0V, "1" = +5V

PACKAGE INFORMATION

N PACKAGE



NOTES:

1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED.
2. BODY MATERIAL: CERAMIC WITH KOVAR OR EQUIVALENT. TOP RING GOLD PLATED.
3. LID MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED, ALLOY SEAL.
4. TOLERANCES NON CUMULATIVE.
5. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
6. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
7. THERMAL RESISTANCE: Θ Ja = .050°C/mW, Θ Jc = .010°C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

HIGH SPEED 512x8 STATIC READ-ONLY MEMORY | 2530

ADVANCE SPECIFICATION

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The 2530 is a high speed 4,096-bit Static Read-Only Memory available in a 512x8 organization. This device has TTL compatible inputs and outputs and requires +5V and −12V power supplies. A $\overline{\text{READ}}$ input controls the entry of data from the ROM into output latches. Three-state outputs allow OR tying for implementing larger memories. Two OUTPUT ENABLES control the eight output devices without affecting address circuitry.

FEATURES

- 512x8 ORGANIZATION
- 450ns TYPICAL ACCESS TIME
- STATIC OPERATION
- ADDRESS LATCHES
- TTL/DTL COMPATIBLE INPUTS
- TTL/DTL COMPATIBLE THREE STATE OUTPUTS
- V_{CC} = +5V, V_{GG} = −12V
- 24-PIN SILICONE DIP
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

MICRO-PROGRAMMING
CODE-CONVERSION

BIPOLAR COMPATIBILITY

All inputs of the 2530 can be driven directly by standard bipolar integrated circuits, (TTL, DTL, etc.). The data output buffers are capable of sinking a minimum of 1.6mA sufficient to drive one standard TTL load.

STANDARD TRUTH TABLES

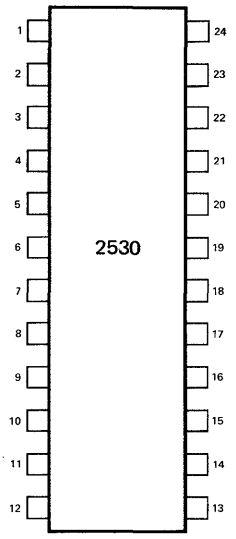
The 2530NX/CM3530 is an ASCII-EBCDIC and EBCDIC-ASCII code converter. Use this device for evaluation or for applications requiring this conversion. Other standards will be announced as they become available.

CUSTOM TRUTH TABLES

Ask your Signetics Representative for recommended coding format.

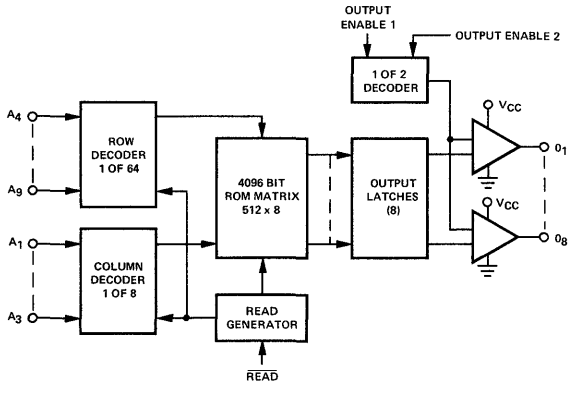
PIN CONFIGURATION (Top View)

NX PACKAGE



1.	Output 6	24.	V_{CC}
2.	Output 7	23.	Output 5
3.	Output 8	22.	Output 4
4.	Ground	21.	Output 3
5.	Address 1	20.	Output 2
6.	Address 2	19.	Output 1
7.	Address 3	18.	$\overline{\text{Read}}$
8.	Output Enable 1	17.	NC
9.	Output Enable 2	16.	Address 9
10.	Address 4	15.	Address 8
11.	Address 5	14.	Address 7
12.	V_{GG}	13.	Address 6

BLOCK DIAGRAM



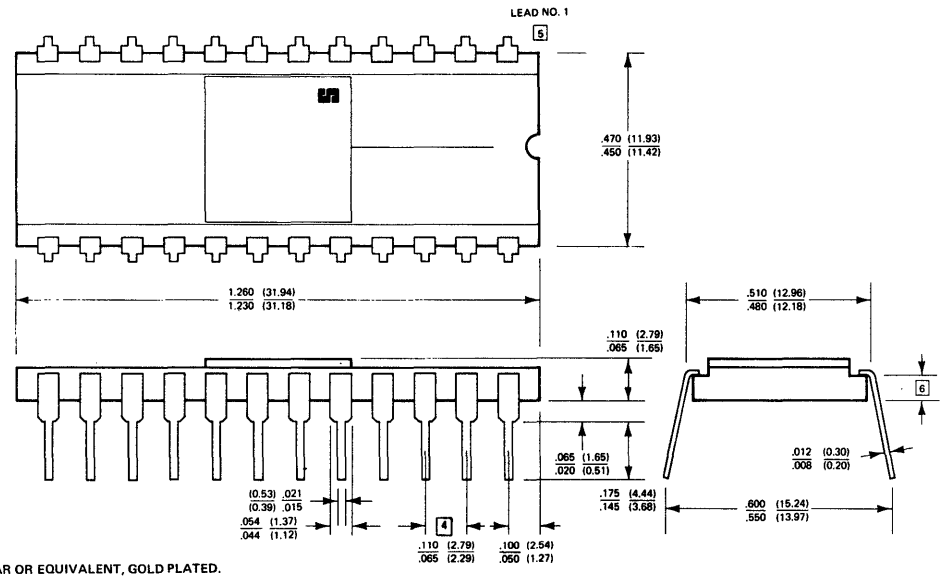
PART IDENTIFICATION

PART NUMBER	OP. TEMP. RANGE	PACKAGE
2530N	0-70°C	24-Pin DIP

NOTE: "0" = 0V, "1" = +5V

PACKAGE INFORMATION

N PACKAGE



NOTES:

1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED.
2. BODY MATERIAL: CERAMIC WITH KOVAR OR EQUIVALENT. TOP RING GOLD PLATED.
3. LID MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED, ALLOY SEAL.
4. TOLERANCES NON CUMULATIVE.
5. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
6. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
7. THERMAL RESISTANCE: Θ Ja = .050°C/mW, Θ Jc = .010°C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

QUAD 80-BIT STATIC SHIFT REGISTER | 2532

ADVANCE SPECIFICATION

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The Signetics 2532 Static Shift Register consists of enhancement mode P-Channel silicon gate MOS devices integrated on a single monolithic chip. Each of the four 80-bit registers is provided with an independent input, push-pull output and recirculation control. The single phase clock is common to all four registers. All inputs and outputs including the clock interface directly with TTL or DTL circuits without external components.

Data is entered when the clock is at a logic "1". Data is shifted when the clock goes low. When the Recirculate control is at a logic "1", data recirculates and is continuously available at the output, data input is inhibited. With the Recirculate control is at a logic "0", data is entered.

FEATURES

- TOTAL TTL COMPATIBILITY
- SINGLE CLOCK LINE
- RECIRCULATE PATH ON CHIP
- DC TO 2.5 MHz OPERATION GUARANTEED
- LOW POWER (TYPICALLY 40 μW/BIT)
- PIN-FOR-PIN REPLACEMENT FOR (DYNAMIC) MK1007P AND TMS3409
- POWER SUPPLIES +5V AND −12V

APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST STATIC BUFFER MEMORIES
CRT REFRESH MEMORIES – LINE STORAGE
DELAY LINES
DIGITAL FILTERING

SPECIAL FEATURES

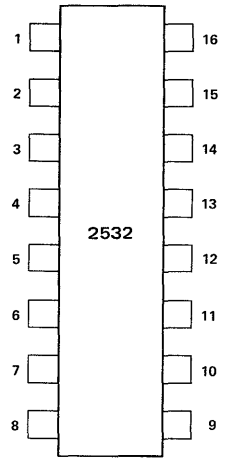
The three clock phases used by the static register cells are generated internally by an on-chip generator. This clock generator is controlled by a single TTL/DTL logic level input.

BIPOLAR COMPATIBILITY

All inputs of these registers, including the clock can be driven directly by bipolar TTL/DTL integrated circuits without external components. Each input is equipped with an internal pull-up resistor to enhance the "1" level of the TTL driver. Outputs are push-pull operating between 0V and +5V and provide a sink current of 1.6mA for one TTL fanout.

PIN CONFIGURATION (Top View)

B PACKAGE



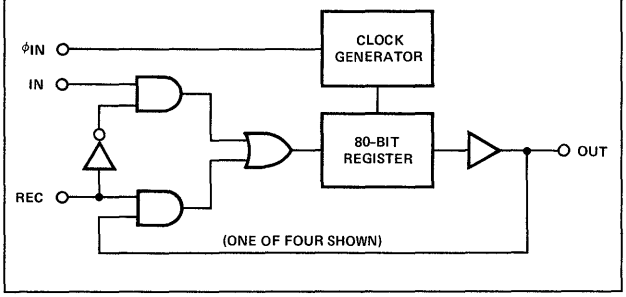
1.	OUT 1	16.	V_{CC}
2.	Recirculate 1	15.	IN 4
3.	IN 1	14.	Recirculate 4
4.	OUT 2	13.	OUT 4
5.	Recirculate 2	12.	V_{GG}
6.	IN 2	11.	ϕ IN
7.	OUT 3	10.	IN 3
8.	V_{DD} (Ground)	9.	Recirculate 3

TRUTH TABLE

RECIRCULATE	INPUT	FUNCTION
0	0	"0" is Written
0	1	"1" is Written
1	0	Recirculate
1	1	Recirculate

NOTE: "0" = 0V, "1" = +5V

BLOCK DIAGRAM

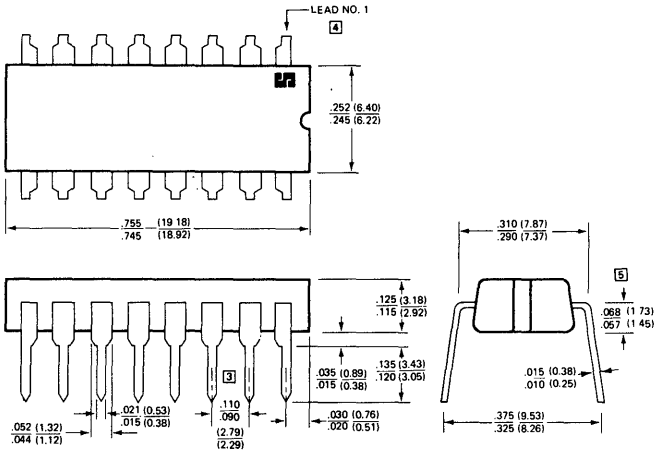


PART IDENTIFICATION

PART NUMBER	BIT LENGTH	PACKAGE
2532B	Quad 80	16-Pin DIP

PACKAGE INFORMATION

B PACKAGE



NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: SILICONE MOLDED.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: Θ Ja = .16°C/mW, Θ Jc = .08°C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

1024-BIT STATIC SHIFT REGISTER | 2533

ADVANCE SPECIFICATION

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The Signetics 2533 Static Shift Register consists of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip.

The 1024-bit register is equipped with two data inputs together with a "Stream Select" control to facilitate external recirculation.

The single phase clock input, data input, data output, and stream select control will interface directly with TTL/DTL circuits without external components.

Data is entered when the clock is at a logic "1". Data is shifted when the clock goes low.

FEATURES

- TOTAL TTL COMPATIBILITY
- SINGLE CLOCK LINE
- DC TO 1.0 MHz GUARANTEED
- LOW POWER (TYPICALLY 160 μW/BIT)
- POWER SUPPLIES +5V AND −12V
- 8-PIN DIP
- STREAM SELECT FOR EASY RECIRCULATION

APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST STATIC BUFFER MEMORIES
CRT REFRESH – LINE AND PAGE
DELAY LINES
DRUM MEMORY REPLACEMENT

SPECIAL FEATURES

The three clock phases used by the static register cells are generated internally by an on-chip generator. This clock generator is controlled by a single TTL/DTL 5V logic level input.

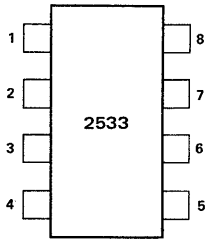
Recirculation of data in the 2533 is accomplished by simply jumpering the output back to IN 2. The stream select control then becomes a Data Entry/Recirculate Control.

BIPOLAR COMPATIBILITY

All inputs of this register, including the clock can be driven directly by bipolar TTL/DTL integrated circuits without external components. Each input is equipped with an internal pull-up resistor to enhance the "1" level of the TTL driver. The output is push-pull, operating between 0V and +5V, and provides a sink current of 1.6mA for one TTL fanout.

PIN CONFIGURATION (Top View)

V PACKAGE



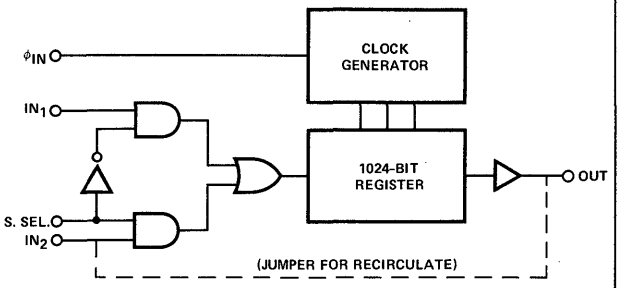
1. OUT
2. V_{GG}
3. Stream Select
4. V_{DD} (Ground)
5. IN 1
6. ϕ IN
7. IN 2
8. V_{CC}

TRUTH TABLE

STREAM SELECT	FUNCTION
0	IN 1
1	IN 2

Note: "0" = 0V, "1" = +5V

BLOCK DIAGRAM

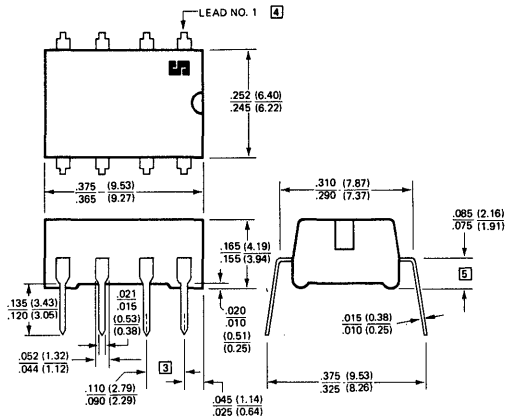


PART IDENTIFICATION

PART NUMBER	BIT LENGTH	PACKAGE
2533V	1024	8-Pin DIP

PACKAGE INFORMATION

V PACKAGE



NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: SILICONE MOLDED.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: Θ Ja = .16 C/mW, Θ Jc = .08 C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

UNIVERSAL ASYNCHRONOUS FIRST-IN, FIRST-OUT BUFFER REGISTER

2535

ADVANCE SPECIFICATION

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The Signetics 2535 is a P-Channel MOS asynchronous buffer memory consisting of 32 8-bit words. Both input and output can be either serial or parallel with a data rate of DC to 1 MHz in either mode of operation.

The register is designed so that information entered at the input will "fall through" to the lowest unoccupied location. Input and output may be accessed asynchronously. Control logic provides flag signals indicating presence of data and availability status of empty storage locations.

The 2535 may be expanded in either the bit or word direction. All inputs and outputs are directly DTL/TTL compatible.

FEATURES

- ASYNCHRONOUS LOAD AND DUMP
- 32 WORD BY 8-BIT ELASTIC STORAGE
- DC TO 1 MHz OPERATION
- SERIAL OR PARALLEL OPERATION
- TTL COMPATIBLE
- 28-PIN DIP PACKAGE
- V_{CC} = +5V, V_{GG} = −12V

APPLICATIONS

INTERFACE BETWEEN INDEPENDENTLY CLOCKED SYSTEMS
KEYBOARD TO LINE BUFFER MEMORY
DISC AND TAPE BUFFER MEMORIES
DATA CONCENTRATORS
DATA "SILO'S"
BIT RATE SMOOTHING
MODEMS
CPU/TERMINAL BUFFERING

BIPOLAR COMPATIBILITY

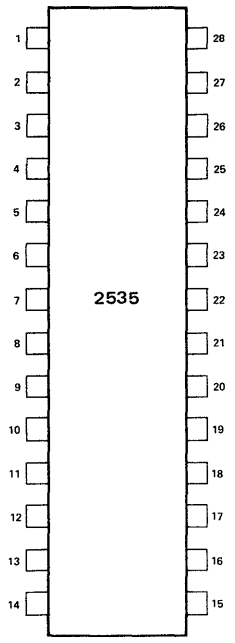
All inputs of the 2535 can be driven directly from TTL output levels. Outputs will sink and source sufficient current for one TTL fan-out.

PART IDENTIFICATION

TYPE	PACKAGE	OP. TEMP. RANGE
2535I	28-Pin Ceramic DIP	0-70°C
2535N	28-Pin Ceramic DIP	0-70°C

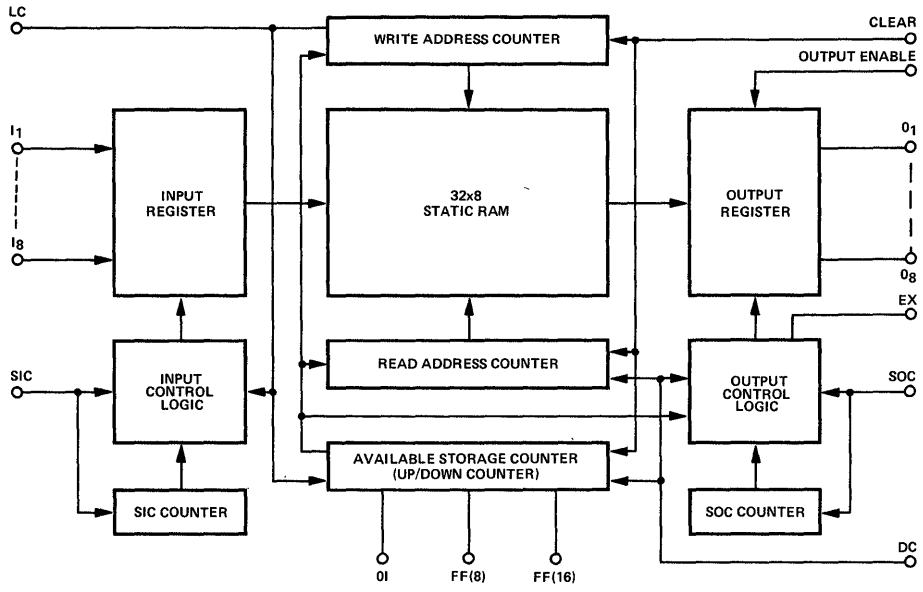
PIN CONFIGURATION (Top View)

I PACKAGE
N PACKAGE



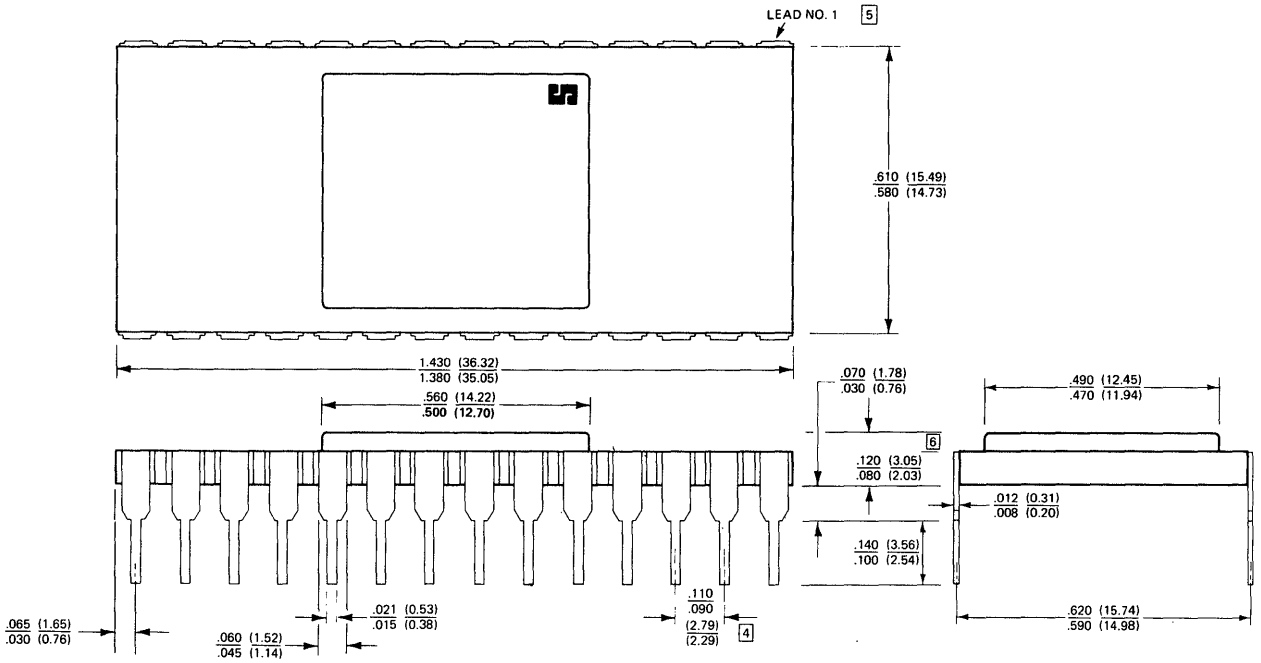
1.	Input 2	28.	Input 3
2.	Input 1	27.	Input 4
3.	V_{GG}	26.	Overflow Indicator
4.	Extend	25.	V_{CC}
5.	Dump Control	24.	Input 5
6.	Serial Output Control	23.	Input 6
7.	Output 1	22.	Input 7
8.	Output 2	21.	Input 8
9.	Output 3	20.	Fullness Flag (8)
10.	Output 4	19.	Fullness Flag (16)
11.	Chip Enable	18.	Load Control
12.	Output 5	17.	Serial Input Control
13.	Output 6	16.	Ground
14.	Output 7	15.	Output 8

BLOCK DIAGRAM



PACKAGE INFORMATION

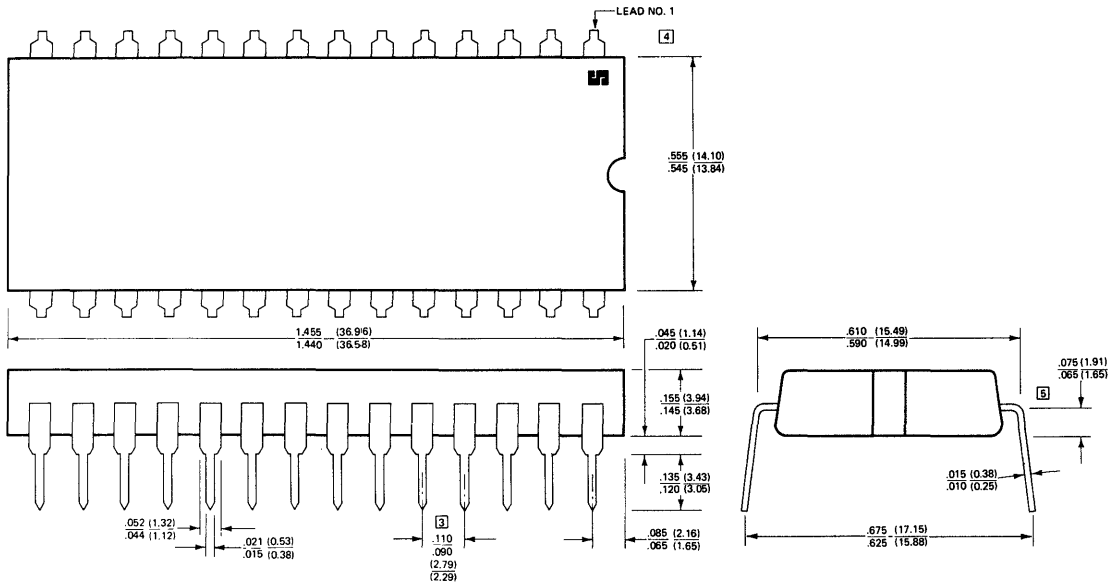
I PACKAGE



Notes:
1. Lead Material: Kovar or Equivalent, Gold Plated.
2. Body Material: Ceramic with Kovar or Equivalent. Top Ring Gold Plated.
3. Lid Material: Kovar or Equivalent, Gold Plated, Alloy Seal.
4. Tolerances Non Cumulative.
5. Signetics Symbol Denotes Lead No. 1.
6. Lead Spacing Shall be Measured within this Zone.
7. Thermal Resistance: ϑ Ja = .050°C/mW, Θ Jc = .010°C/mW.
8. All Dimensions Shown in Parentheses are Metric Equivalents. (Millimeters)

PACKAGE INFORMATION

N PACKAGE



NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: SILICONE MOLDED
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: Θ Ja = .12°C/mW, Θ Jc = .05°C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

UAR-T UNIVERSAL ASYNCHRONOUS RECEIVER-TRANSMITTER

2536

ADVANCE SPECIFICATION

SILICON GATE MOS 2500 SERIES

DESCRIPTION

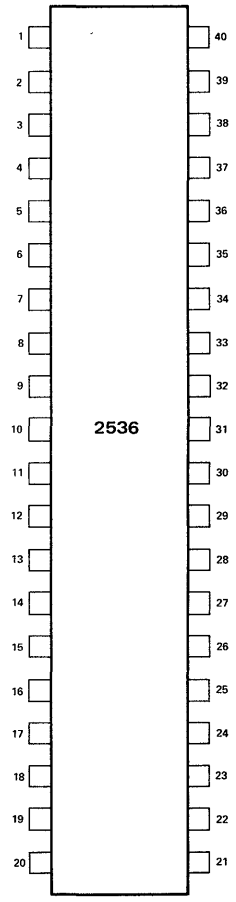
The Signetics 2536 Universal Asynchronous Receiver-Transmitter is a general purpose, programmable MOS/LSI subsystem integrated on a single monolithic chip. The device can simultaneously convert asynchronous serial binary characters to a parallel format (receiver) and parallel binary characters to serial, asynchronous output (transmitter) with start, parity, and stop bits added or verified. Both receiver and transmitter are double buffered and fully compatible with bipolar logic. The UAR-T may be programmed as follows: the word length can be either 5, 6, 7, or 8 bits; parity generation and checking may be inhibited; the parity may be even or odd; and the number of stop bits may be either one or two.

FEATURES

- DIRECTLY TTL/DTL COMPATIBLE – NO INTERFACING CIRCUITS REQUIRED
- FULLY DOUBLE BUFFERED – ELIMINATES NEED FOR SYSTEM SYNCHRONIZATION: FACILITATES HIGH SPEED OPERATION
- FULL DUPLEX OPERATION – TRANSMITS AND RECEIVES DATA SIMULTANEOUSLY
- FULLY PROGRAMMABLE – EXTERNALLY SELECTABLE:
  - WORD LENGTH
  - BAUD RATE
  - EVEN/ODD PARITY
  - PARITY INHIBIT
  - SINGLE OR DOUBLE STOP BIT GENERATION
- HIGH SPEED OPERATION – 30K BAUD, 250ns STROBES
- AUTOMATIC DATA STATUS GENERATION:
  - TRANSMISSION COMPLETE
  - BUFFER REGISTER TRANSFER COMPLETE
  - RECEIVED DATA AVAILABLE
  - PARITY ERROR
  - FRAMING ERROR
  - OVERRUN ERROR
- TRI-STATE OUTPUTS-BUSSING CAPABILITY
  - DATA OUTPUTS
  - STATUS FLAGS
- STATIC LOGIC – STABLE
- STANDARD POWER SUPPLIES – +5, –12

PIN CONFIGURATION (Top View)

I PACKAGE

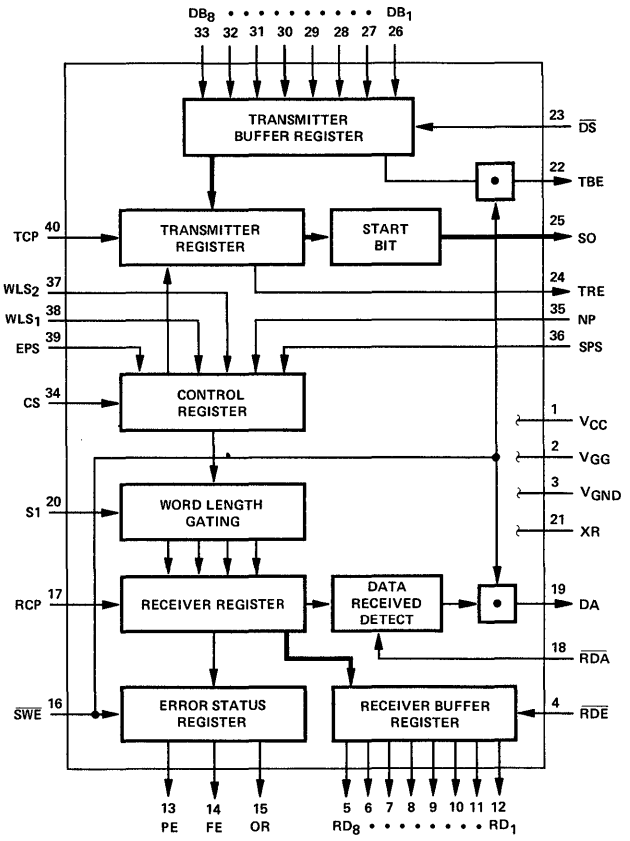


1. V_{CC}
2. V_{GG}
3. Ground
4. $\overline{\text{Received data enable}}$
5. Received data bits (RD_1 – RD_8)
6.
7.
8.
9.
10.
11.
12.
13. Parity error
14. Framing error
15. Over-run
16. $\overline{\text{Status flag enable}}$
17. Receiver clock
18. $\overline{\text{Reset data available}}$
19. Data available
20. Receiver serial input
21. External (master) reset
22. Transmitter buffer empty
23. $\overline{\text{Data load strobe}}$
24. Transmitter register empty
25. Transmitter serial output
26. Transmitter data inputs (DB_1 – DB_8)
27.
28.
29.
30.
31.
32.
33.
34. Control load strobe
35. No parity
36. Stop bit(s) select
37. Word length select 2
38. Word length select 1
39. Odd/even parity select
40. Transmitter clock pulse

APPLICATIONS

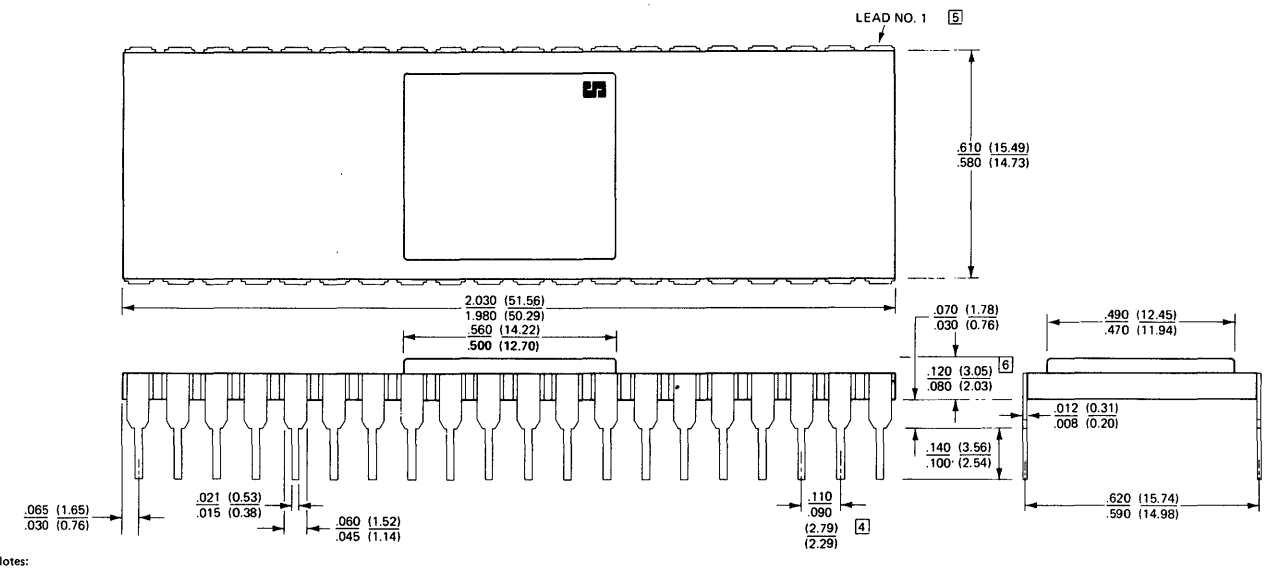
PERIPHERALS
TERMINALS
PRINTERS
MINI-COMPUTERS
MODEMS
CONCENTRATORS
MULTIPLEXERS
CONTROLLERS
CARD AND TAPE READERS
KEYBOARD ENCODERS
REMOTE DATA ACQUISITION SYSTEMS

BLOCK DIAGRAM



PACKAGE INFORMATION

I PACKAGE



Notes:
1. Lead Material: Kovar or Equivalent, Gold Plated.
2. Body Material: Ceramic with Kovar or Equivalent. Top Ring Gold Plated.
3. Lid Material: Kovar or Equivalent, Gold Plated, Alloy Seal.
4. Tolerances Non Cumulative.
5. Signetics Symbol Denotes Lead No. 1.
6. Lead Spacing Shall be Measured within this Zone.
7. Thermal Resistance: Θ Ja = .050°C/mW, Θ Jc = .010°C/mW.
8. All Dimensions Shown in Parentheses are Metric Equivalents. (Millimeters)

FULLY DECODED, 2048-BIT RANDOM ACCESS MEMORY

2548

ADVANCE SPECIFICATION

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The Signetics 2458 2048x1 Dynamic Random Access Memory employs enhancement mode P-channel devices integrated on a single monolithic chip. The device is fully decoded and contains built-in refresh amplifiers. All address input data and control lines are directly TTL compatible. Clocking is performed by three high level (0V to −20V) non-overlapping clock inputs. (Use Signetics N575 Clock Driver.) The output data line supplies a minimum "1" level output of 600μA. (Use Signetics 8T25 Sense Amplifier.)

FEATURES

- HIGH STORAGE DENSITY
- READ ACCESS TIME 300ns MAX.
- CYCLE TIME 615ns MAX.
- LOW POWER DISSIPATION (80 μW/BIT)
- AUTOMATIC REFRESH DURING READ (2 ms)
- LOW CLOCK CAPACITANCE (ϕ1 35 pF; ϕ2, ϕ3 25 pF)
- STANDARD 22-PIN DIP, CERAMIC
- V_{CC} = +5V, V_{BB} = +7V, V_{DD} = −15V
- ALL INPUTS EXCEPT CLOCK ARE TTL COMPATIBLE

APPLICATIONS

CORE MEMORY REPLACEMENT

DOUBLED STORAGE CAPACITY (OVER 1K RAMS)

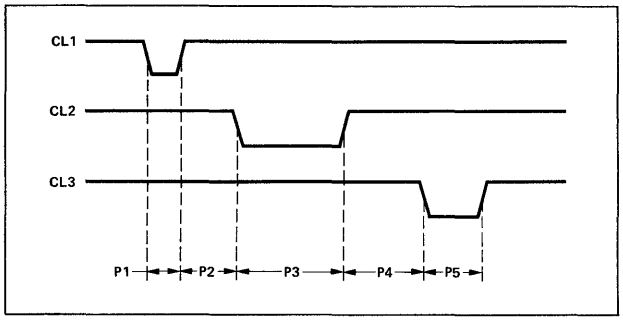
BUFFER STORES

MAIN MEMORY

BIPOLAR COMPATIBILITY

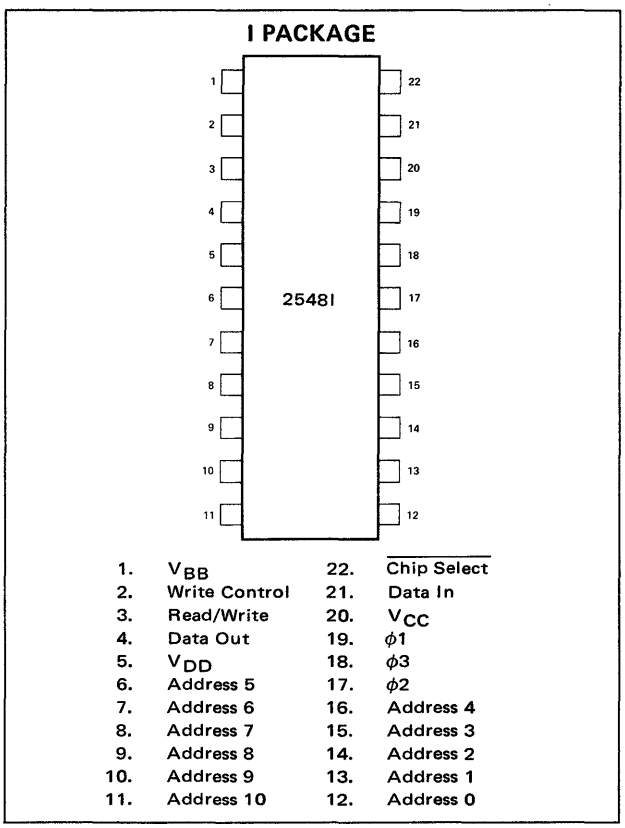
All address lines, control lines and data input lines are directly TTL compatible. Three clock lines require high level drivers. The data out line requires a sense amplifier. (Signetics N575 Clock Driver and 8T25 Sense Amplifier are recommended.)

GENERAL TIMING AND OPERATION



1. During period 1 internal nodes are precharged. The rising edge of CL1 (end of Period 1) clocks input address and CS data into storage elements.
2. During period 2 the row and column decoders select the desired bit.

PIN CONFIGURATION (Top View)



1.	V_{BB}	22.	$\overline{\text{Chip Select}}$
2.	Write Control	21.	Data In
3.	Read/Write	20.	V_{CC}
4.	Data Out	19.	ϕ1
5.	V_{DD}	18.	ϕ3
6.	Address 5	17.	ϕ2
7.	Address 6	16.	Address 4
8.	Address 7	15.	Address 3
9.	Address 8	14.	Address 2
10.	Address 9	13.	Address 1
11.	Address 10	12.	Address 0

3. During period 3 the information in the bit is exclusive OR'd with the selected information contained in the column inversion memory. The result is sent to the output. The output information is stable near the end of period 3.
4. During period 4 the write enable circuitry is activated. The internal data-in level is determined by exclusive OR'ing the actual input with the selected information contained in the column inversion memory.
5. If a write is desired during period 5, data is written into the selected bit. The information stored in all other bits sharing the same addressed column is inverted and refreshed. The appropriate bit of the column inversion memory is also inverted and refreshed.

   If a refresh is desired during period 5, the information stored in all bits sharing the same addressed column is inverted and refreshed. The appropriate bit of the column inversion memory is also inverted and refreshed.

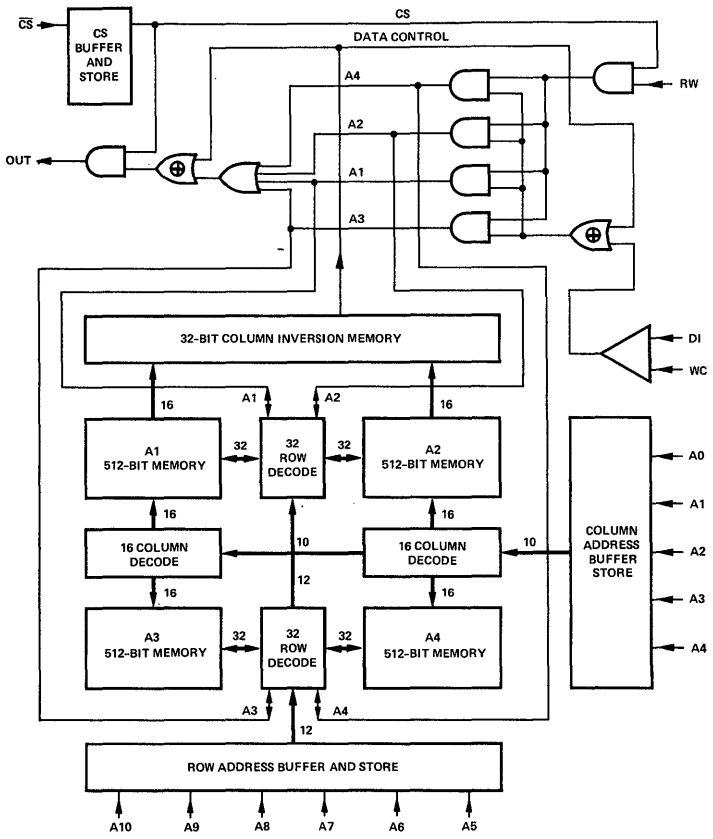
PART IDENTIFICATION

TYPE	PACKAGE	OP. TEMP. RANGE
25481	22-Pin Ceramic DIP (0.4")	0-70°C

NOTE: "0" = 0V, "1" = +5V

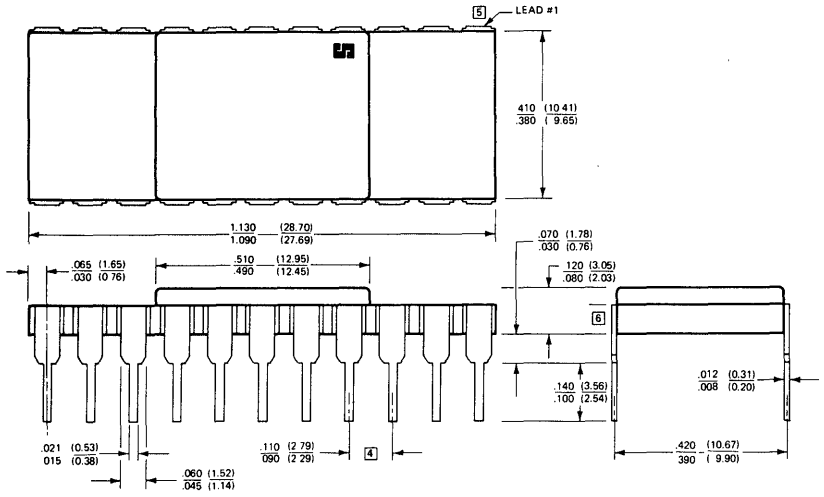
BLOCK DIAGRAM

2048 BIT RAM



PACKAGE INFORMATION

I PACKAGE



NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED.
2. BODY MATERIAL: CERAMIC WITH KOVAR OR EQUIVALENT. TOP RING GOLD PLATED.
3. LID MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED, ALLOY SEAL.
4. TOLERANCES NON CUMULATIVE.
5. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
6. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
7. THERMAL RESISTANCE: Θ Ja = .055°C/mW, Θ Jc = .012°C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

FULLY DECODED, HIGH SPEED, 1024-BIT DYNAMIC, RANDOM ACCESS MEMORY

2601

ADVANCED SPECIFICATION

SILICON GATE MOS 2600 SERIES

DESCRIPTION

The Signetics 2601 is a high speed, dynamic random access memory offering a 1024x1 organization. Fabricated with low threshold N-Channel silicon gate technology, the 2601 yields an access time of less than 80ns and allows a cycle time of less than 200ns. Cell refresh is accomplished automatically during row (A_0-A_4) addressing. The clocking scheme is straight-forward, requiring three non-overlapping controls: Clock ϕ1, Chip Select, and $\overline{\text{READ}}$/Write. Recommend Signetics N577 Clock Driver, N8T25 for output sense amplifier.

FEATURES

- HIGH SPEED ACCESS . . . . 80ns MAX
- CYCLE TIME 200ns MAX.
- 1024x1 ORGANIZATION
- POSITIVE VOLTAGE CONTROL SIGNALS
- OUTPUT CURRENT . . . . 1.2 mA MIN
- REFRESH TIME 2ms
- 18-PIN DIP PACKAGE
- BUSSABLE OUTPUT
- EASY CLOCKING
- V_{DD} = +16V, V_{BB} = −2.5V
- SIGNETICS N-CHANNEL SILICON GATE TECHNOLOGY

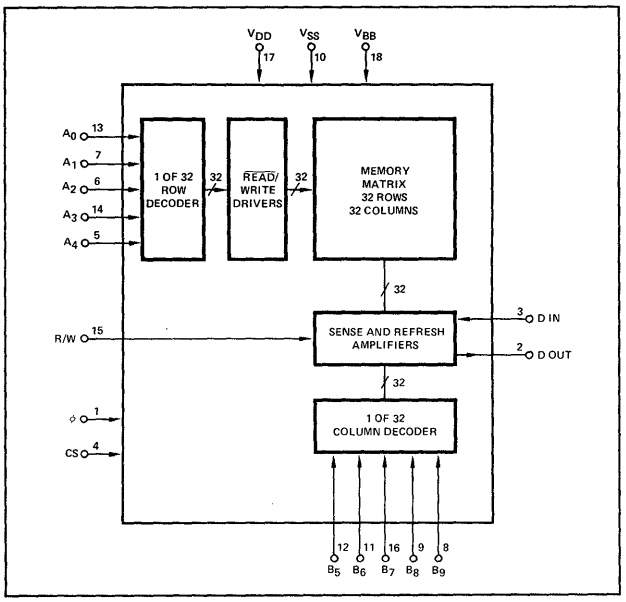
APPLICATIONS

HIGH SPEED MAINFRAME MEMORY

CORE MEMORY REPLACEMENT

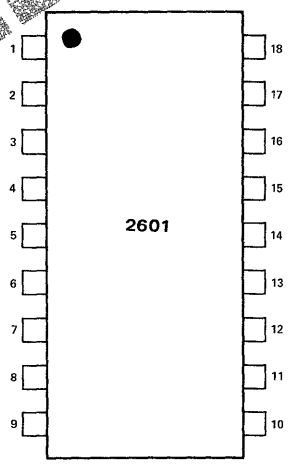
HIGH SPEED BUFFER STORES

BLOCK DIAGRAM



PIN CONFIGURATION

I & XA PACKAGES

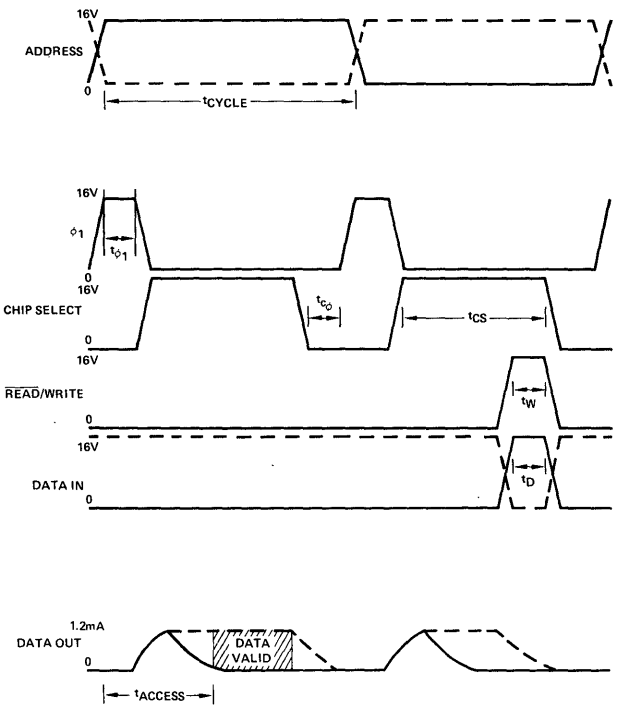


1. Clock ϕ
2. Data Out
3. Data In
4. Chip Select
5. Address 4
6. Address 2
7. Address 1
8. Address 9
9. Address 8
10. V_{SS} (Ground)
11. Address 6
12. Address 5
13. Address 0
14. Address 3
15. $\overline{\text{Read}}$/Write
16. Address 7
17. V_{DD}
18. V_{BB}

PART IDENTIFICATION

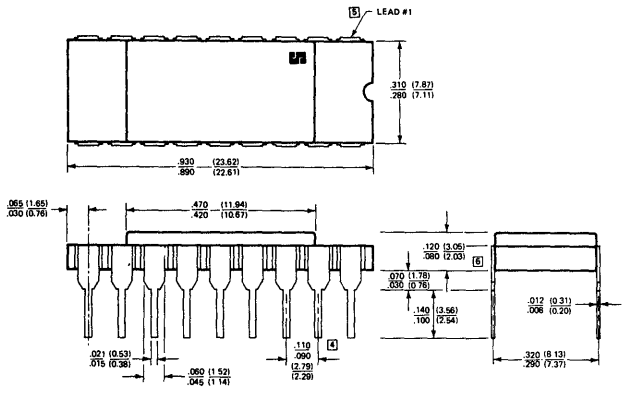
TYPE	PACKAGE	OP. TEMP. RANGE
2601XA	18-Pin Plastic DIP	0-70°C
2601I	18-Pin Ceramic DIP	0-70°C

TIMING DIAGRAM



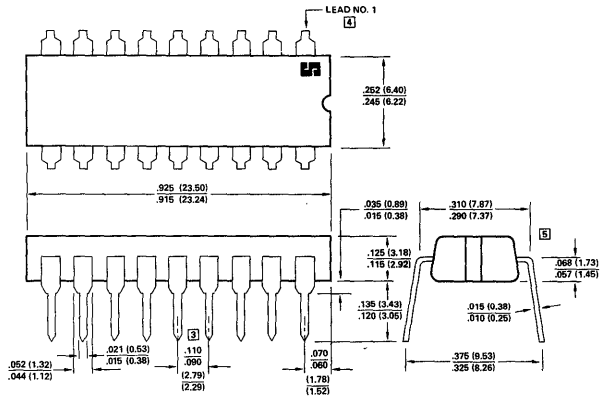
PACKAGE INFORMATION

I PACKAGE



NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED.
2. BODY MATERIAL: CERAMIC WITH KOVAR OR EQUIVALENT.
3. LID MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED, ALLOY SEAL.
4. TOLERANCES NON CUMULATIVE.
5. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
6. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
7. THERMAL RESISTANCE: Θ Ja = .060°C/mW, Θ Jc = .015°C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

XA PACKAGE



NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: SILICONE MOLDED.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: Θ JA = .16°C/mW, Θ JC = .08°C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

FULLY DECODED, 1024-BIT STATIC RANDOM ACCESS MEMORY

2602
2602-1

ADVANCED SPECIFICATION

SILICON GATE MOS 2600 SERIES

DESCRIPTION

The Signetics 2602 is a medium speed, static random access memory offering a 1024x1 organization. Fabricated with low threshold N-Channel silicon gate technology, the 2602 yields an access and read cycle time of less than 1 μs for the standard version and 500ns for the -1 version. Write cycle time is 500ns.

The 2602 is fully static, requiring no clocks and is completely DTL/TTL compatible including the single +5V power supply requirement.

FEATURES

- 1024x1 STATIC OPERATION
- 100% TTL COMPATIBLE
- LOW ACCESS AND CYCLE TIME: 2602 1μs
  2602-1 500ns
- LOW POWER DISSIPATION 0.2mW/BIT
- STANDARD PACKAGE 16-PIN DIP
- V_{CC} = +5V
- SIGNETICS N-CHANNEL SILICON GATE TECHNOLOGY

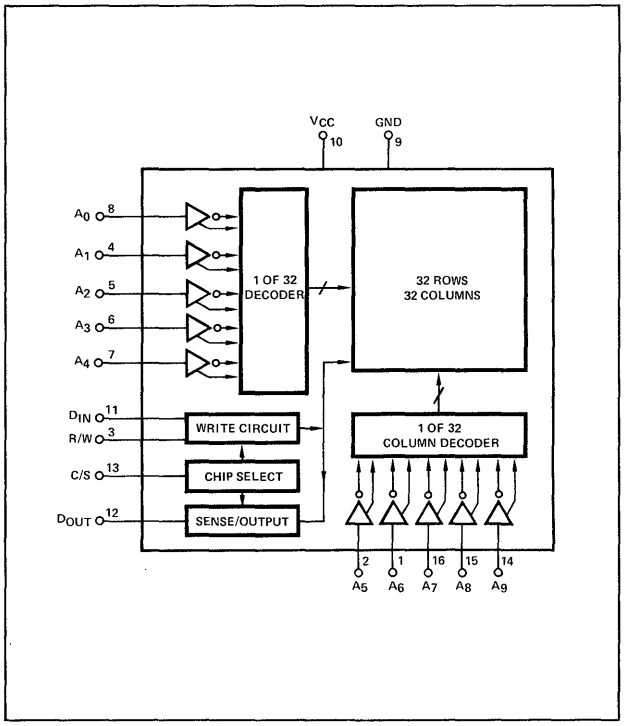
APPLICATIONS

PERIPHERAL MEMORIES

BUFFER MEMORIES

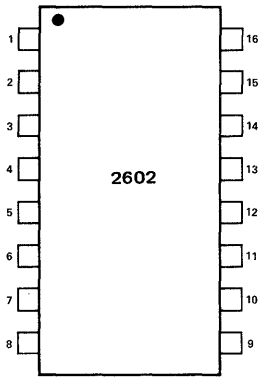
MINICOMPUTER MEMORY

BLOCK DIAGRAM



PIN CONFIGURATION

B & I PACKAGES



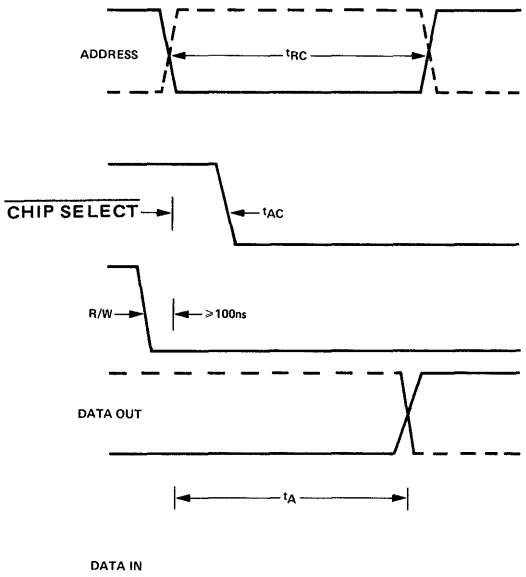
1. Address 6	16. Address 7
2. Address 5	15. Address 8
3. $\overline{\text{Read}}$/Write	14. Address 9
4. Address 1	13. $\overline{\text{Chip Select}}$
5. Address 2	12. Data Out
6. Address 3	11. Data In
7. Address 4	10. V_{CC}
8. Address 0	9. Ground

PART IDENTIFICATION

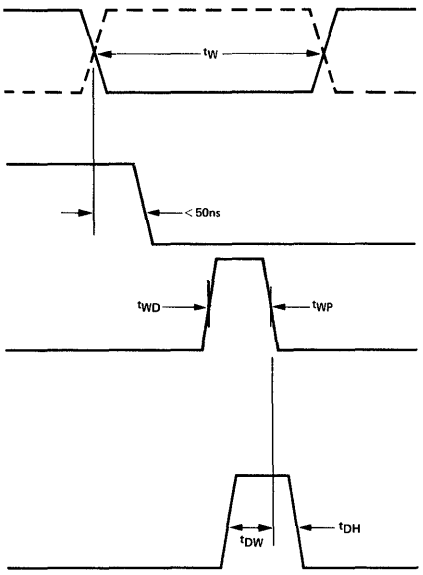
TYPE	PACKAGE	T_A	OP. TEMP. RANGE
2602B	16-Pin Plastic DIP	1μs	0-70°C
2602-1B	16-Pin Plastic DIP	500ns	0-70°C
2602 I	16-Pin Ceramic DIP	1μs	0-70°C
2602-1I	16-Pin Ceramic DIP	500ns	0-70°C

TIMING DIAGRAMS

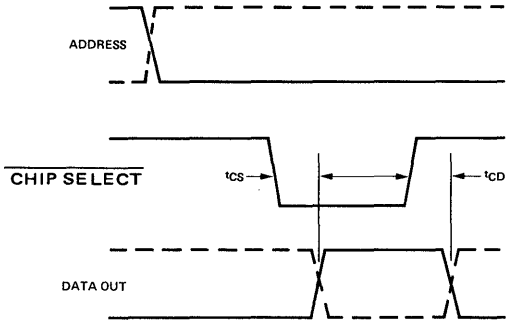
READ CYCLE



WRITE CYCLE

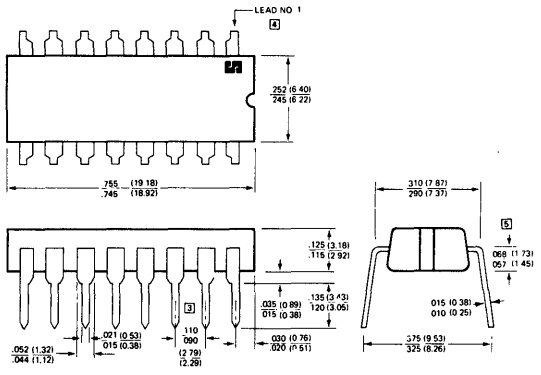


CHIP SELECT AND DESELECT



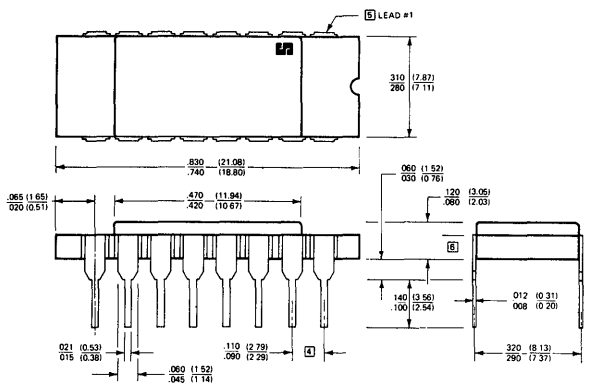
PACKAGE INFORMATION

B PACKAGE



NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: SILICONE MOLDED.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: Θ Ja = .16°C/mW, Θ Jc = .08°C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

I PACKAGE



NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED.
2. BODY MATERIAL: CERAMIC WITH KOVAR OR EQUIVALENT. TOP RING GOLD PLATED.
3. LID MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED, ALLOY SEAL.
4. TOLERANCES NON CUMULATIVE.
5. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
6. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
7. THERMAL RESISTANCE: Θ Ja = .062°C/mW, Θ Jc = .018°C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

DUAL STATIC SHIFT REGISTERS 2000

METAL GATE MOS 2000 SERIES

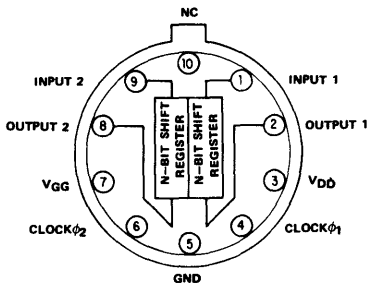
DESCRIPTION

The S2001K, S2002K, S2003K, S2004K, and S2005K are Dual Static Shift Registers manufactured with a "P" channel enhancement mode process.

The registers vary in length from dual 16 to dual 100. Two power supplies and 2 external 28 volt clocks are required. Static operation is assured with a third clock phase that is generated on the chip. The pin configuration allows interchanging of register lengths without rewiring the socket. Data is transferred into the register during ϕ_1 and output data appears on the negative-going edge of ϕ_2. For static operation ϕ_1 must be a "0" and ϕ_2 "1".

PIN CONFIGURATION

BOTTOM VIEW



NC–NO INTERNAL CONNECTION

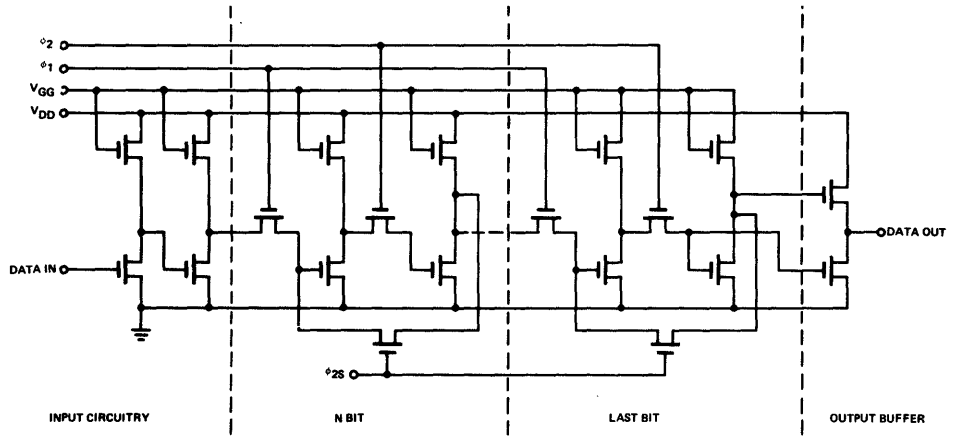
PARTS IDENTIFICATION TABLE

PART NO.	BIT LENGTH	PACKAGE
S2001K	16	10 Pin TO-100
S2002K	25	10 Pin TO-100
S2003K	32	10 Pin TO-100
S2004K	50	10 Pin TO-100
S2005K	100	10 Pin TO-100

ABSOLUTE MAXIMUM RATINGS

V_{dd} with respect to Gnd	-16V to 0.3V
V_{gg} with respect to Gnd	-30V to 0.3V
Clock and In with respect to Gnd	-30V to 0.3V
Operating Temperature	-55°C to +85°C
Storage Temperature	-55°C to +150°C

CIRCUIT SCHEMATIC



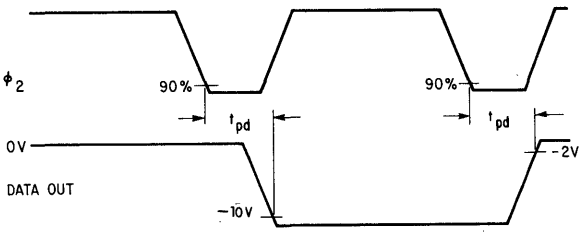
ELECTRICAL CHARACTERISTICS (Notes: 1, 2, 3, 4 and 5)

CHARACTERISTICS	LIMITS				TEST CONDITIONS							NOTES
	MIN	TYP	MAX	UNITS	TEMP °C	V_{DD}	V_{GG}	Vin	$V\phi_1$	$V\phi_2$	OUTPUT	
"1" Output Voltage	-11	-13		V		-13	-27	-10	-27	-27		5
"0" Output Voltage		-0.3	-1	V		-15	-29	-2	-29	-29		5
Output Drive Capability												
2001	-8	-10		V		-13	-27	-10	-27	-27		R_L = 17kΩ to Gnd
	-4	-6		V		-13	-27	-10	-27	-27		R_L = 4 kΩ to Gnd
2002/3/4/5	-10	-11		V		-13	-27	-10	-27	-27		R_L = 17 kΩ to Gnd
	-6	-8		V		-13	-27	-10	-27	-27		R_L = 4 kΩ to Gnd
Input Leakage Current												
Data Inputs			0.5	μA	+85	0	0	-20	0	0		
Clock Inputs												
ϕ_1			50	μA	+85	0	0	0	-28	0		
ϕ_2			50	μA	+85	0	0	0	0	-28		
Output Impedance												
2001			2.5	kΩ		-13	-27	-2	-27	-27	0 to -1V	
2002/3/4/5			1.5	kΩ		-13	-27	-2	-27	-27	0 to -1V	
Input Capacitance												
Data Inputs		3	5	pF	25	-14	-28	0	0	0		8
Clock Inputs												
2001		8	10	pF	25	-14	-28	0	0	0		8
2002		8	12	pF	25	-14	-28	0	0	0		8
2003		8	13	pF	25	-14	-28	0	0	0		8
2004		12	18	pF	25	-14	-28	0	0	0		8
2005		16	33	pF	25	-14	-28	0	0	0		8
Power Supply Current												
I_{DD}												
2001		-3	-10	mA	-55	-15	-29		0	-29		
2002		-5	-20	mA	-55	-15	-29		0	-29		
2003		-6	-24	mA	-55	-15	-29		0	-29		
2004		-7	-17	mA	-55	-15	-29		0	-29		
2005		-14	-32	mA	-55	-15	-29		0	-29		
I_{GG}												
2001/2/3		-0.8	-3.5	mA	-55	-15	-29		0	-29		
2004/5		-0.5	-3.0	mA	-55	-15	-29		0	-29		
Propagation Delay (tpd) from ϕ_2												
2001		300	475	ns	25	-14	-28		-28	-28		6, 7
2002/3/4/5		300	450	ns	25	-14	-28		-28	-28		6, 7

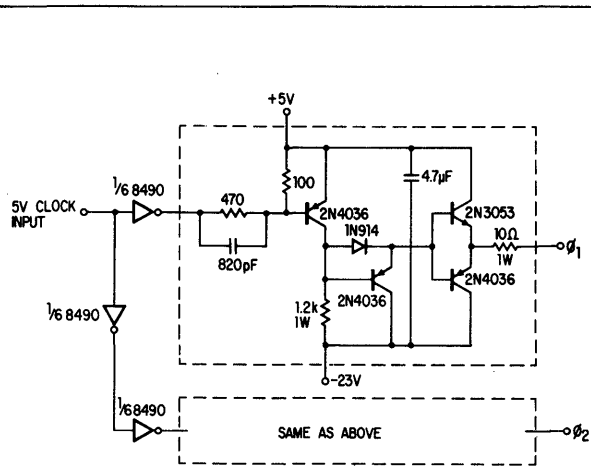
NOTES FOR ELECTRICAL CHARACTERISTICS:

1. Parameter valid over operating temperature range unless otherwise specified.
2. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are tied to ground.
3. Negative logic definition: "DOWN" Level = "1", "UP" Level = "0".
4. Manufacturer reserves the right to make design and process changes and improvements.
5. Output voltage levels valid from D.C. to 1 MHz.
6. See output timing diagram.
7. Output load is 10 pF and 1 MΩ
8. f = 1 MHz, Vac = 25 mV_{rms}. All pins not specifically referenced are tied to guard terminal for capacitance tests. Output pins are left open.
9. All typical values are at 25°C and nominal supply voltages.

OUTPUT TIMING DIAGRAM



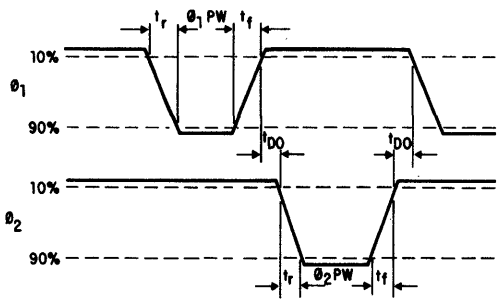
CLOCK DRIVER



Note: At high repetition rates and/or high capacitance loads, the transistors may require heat sinking, i.e., 1000 pF at 1 MHz.

FORCING FUNCTIONS

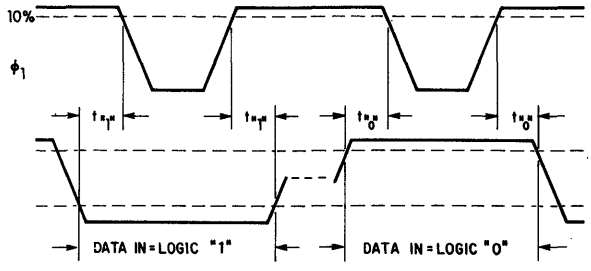
CLOCK REQUIREMENTS



VOLTAGE LEVELS	MIN	TYP	MAX	UNITS
ϕ_1 ϕ_2 "0"	0	-1	-2.0	Volts
ϕ_1 ϕ_2 "1"	-27	-28	-29	Volts
TIMING				
t_r & t_f	.025		5	μsec
ϕ_1 PW	0.4		10	μsec
ϕ_2 PW	0.4			μsec
t_{DO}	0			μsec

Note: ϕ_2 may not be at "0" logic level for more than 10 μs.

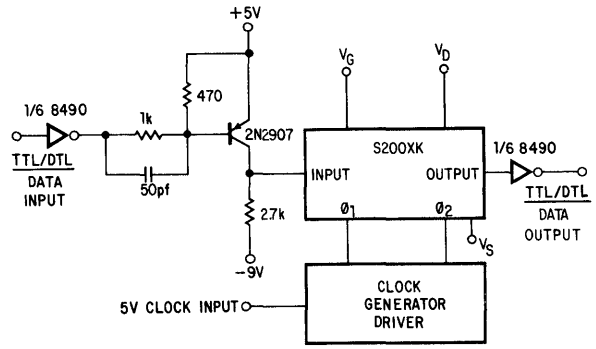
INPUT REQUIREMENTS



CHARACTERISTIC	MIN	MAX	UNITS
Data in "0"	+0.3	-2.0	Volts
Data in "1"	-10		Volts
$t_{"1"}$ & $t_{"0"}$	0		μsec

Note: Data In must be stable between the 10% points of ϕ_1.

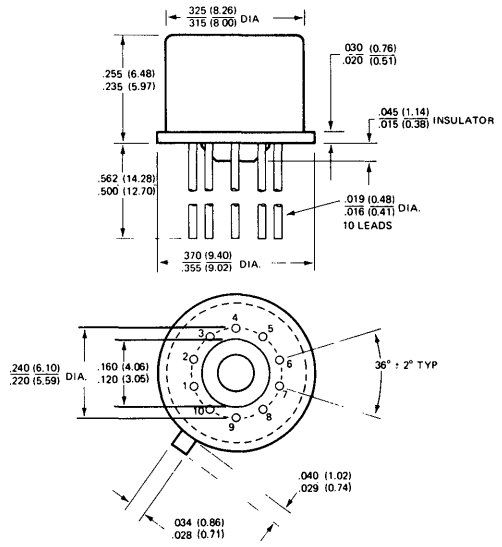
TTL INTERFACE REQUIREMENTS



V_S = +5V, V_D = -9V, V_G = -23V

PACKAGE INFORMATION

K-PACKAGE (TO-100)



NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED.
2. BODY MATERIAL: CERAMIC WITH KOVAR OR EQUIVALENT.
3. LID MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED, ALLOY SEAL.
4. TOLERANCES NON CUMULATIVE.
5. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
6. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
7. THERMAL RESISTANCE: Θ Ja = .060°C/mW, Θ Jc = .015°C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

DUAL 100-BIT STATIC SHIFT REGISTER DC TO 3 MHZ

2010

METAL GATE MOS 2000 SERIES

DESCRIPTION

The N2010K Dual 100-Bit Static Shift Register is designed for use at shift rates from 0 to 3 MHz.* The device employs "P" channel enhancement mode MOS techniques. Power supply requirements are -14 and -28 Vdc. Clocking is provided by two external -28 volt clock phases. A delayed second clock phase (ϕ_{2S}) is generated on the chip.

Data is transferred into the register during ϕ_1. Output data appears on the negative going edge of ϕ_2. For static operation, ϕ_1 must be a "0" and ϕ_2 a "1".

The N2010K is a direct pin replacement for the S2005K/ 3003 1MHz Static Shift Register.

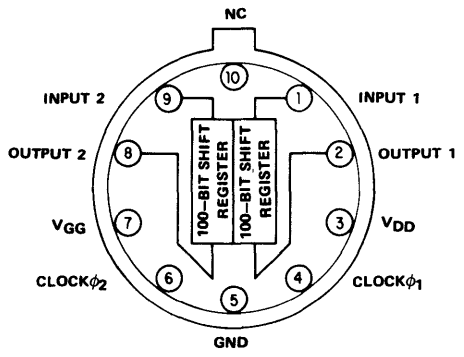
*(25°)

ABSOLUTE MAXIMUM RATINGS:

V_{DD} with respect to Gnd	-16V to 0.3V
V_{GG} with respect to Gnd	-30 to 0.3V
Clock and Input with respect to Gnd	-30V to 0.3V
Operating Temperature	0°C to +70°C
Storage Temperature	-55°C to +150°C

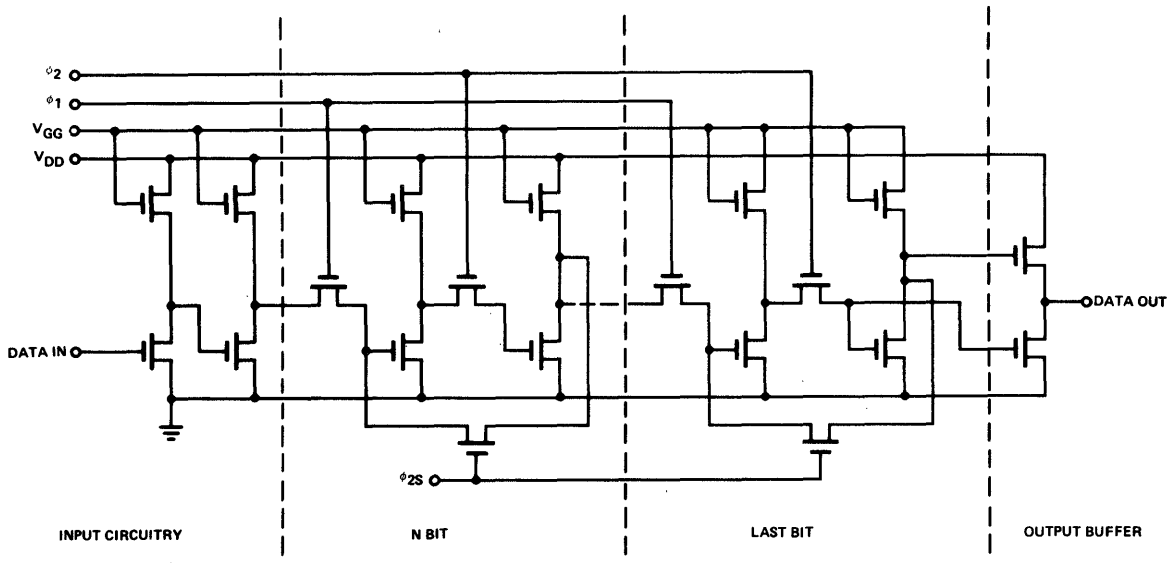
PIN CONFIGURATION

BOTTOM VIEW



NC–NO INTERNAL CONNECTION

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (Notes: 1, 2, 3, 4, 9)

RECOMMENDED POWER SUPPLY VOLTAGES: V_{DD} = −14 ±1 Vdc, V_{GG} = −28 ±1Vdc

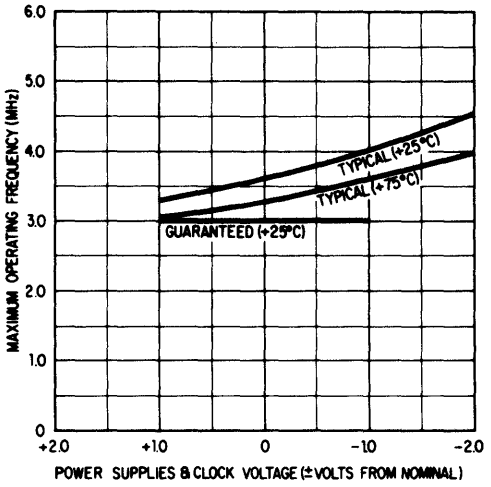
CHARACTERISTICS	LIMITS			UNITS	TEST CONDITIONS							NOTES
	MIN	TYP	MAX		TEMP °C	V_{DD}	V_{GG}	V_{in}	$V_{\phi1}$	$V_{\phi2}$	OUTPUT	
"1" Output Voltage	−8	−10		V	25	−13	−27	−7	−27	−27		5, 7
"0" Output Voltage		−0.3	−1.0	V	25	−15	−29	−2	−29	−29		5, 7
Output Drive Capability	−4	−6		V	25	−13	−27	−7	−27	−27		R_L = 4kΩ to Gnd
Input Leakage Current												
Data Inputs			−0.5	μA	25	0	0	−15	0	0		
Clock Inputs												
ϕ_1			−50	μA	25	0	0	0	−28	0		
ϕ_2			−50	μA	25	0	0	0	0	−28		
Output Impedance			1.5	kΩ	25	−13	−27	−2	−27	−27	0 to −1V	
Input Capacitance												
Data Inputs		3	5	pF	25	−14	−28	0	0	0		8
Clock Inputs		16	33	pF	25	−14	−28	0	0	0		8
Power Supply Current												
I_{DD}		−14	−20	mA	25	−15	−29		0	−29		
I_{GG}		−0.8	−3.0	mA	25	−15	−29		0	−29		
Propagation Delay (tdp) from ϕ_2		200	250	ns	25	−14	−28		−28	−28		6, 7

NOTES:

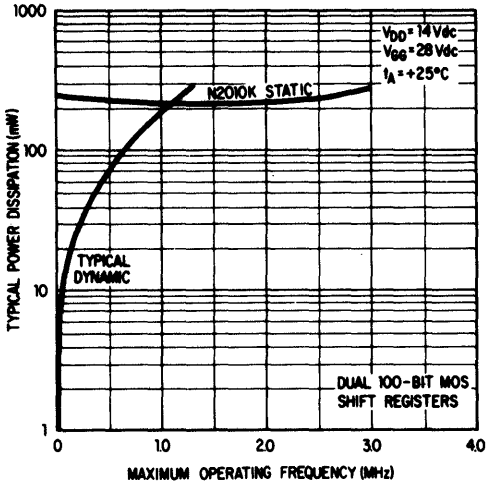
1. Parameter valid at +25°C unless otherwise specified.
2. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are tied to ground.
3. Negative logic definition: "DOWN" Level = "1", "UP" Level = "0".
4. Manufacturer reserves the right to make design and process changes and improvements.
5. Output voltage levels valid from DC to 3 MHz.
6. See output timing diagram.
7. Output load is 10pF and 1 MΩ.
8. f = 1 MHz, Vac = 25mV rms. All pins not specifically referenced are tied to guard terminal for capacitance tests. Output pins are left open.
9. All typical values are at 25°C and nominal supply voltages.

TYPICAL PERFORMANCE CHARACTERISTICS

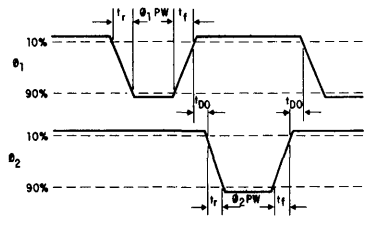
MAXIMUM OPERATION FREQUENCY
VERSUS CLOCK AND SUPPLY VOLTAGE



POWER DISSIPATION
VERSUS OPERATING FREQUENCY



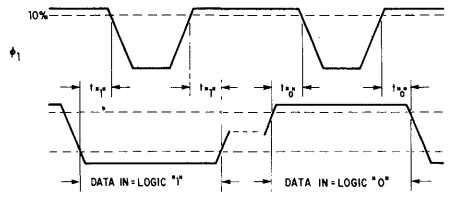
CLOCK REQUIREMENTS



VOLTAGE LEVELS	MIN	NOM	MAX	UNITS
ϕ_1 ϕ_2 "0"	0	-1	-2.0	Volts
ϕ_1 ϕ_2 "1"	-27	-28	-29	Volts
TIMING				
t_r & t_f	.010		5	μsec
ϕ_1 PW	0.10		10	μsec
ϕ_2 PW	0.15			μsec
t_{DO}	0			μsec
Clock Repetition Rate	0		3	MHz

Note: ϕ_2 may not be at "0" logic level for more than 10 μs.

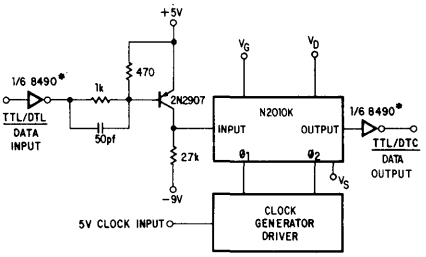
INPUT REQUIREMENTS



CHARACTERISTIC	MIN	MAX	UNITS
Data in "0"	+0.3	-2.0	Volts
Data in "1"	-7.0		Volts
$t_{"1"}$ & $t_{"0"}$	0		μsec

Note: Data In must be stable between the 10% points of ϕ_1.

TTL INTERFACE REQUIREMENTS

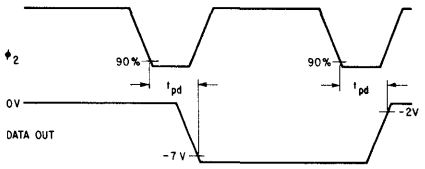


NOTES:

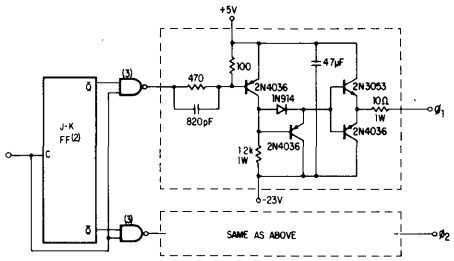
1. Register ground (V_S) is tied to the bipolar integrated circuit V_{CC} power supply for proper biasing.
2. V_S = +5VDC
   V_D = -9 VDC
   V_G = -23 VDC

*3. Signetics Corp. N8490A

OUTPUT TIMING DIAGRAM



CLOCK DRIVER

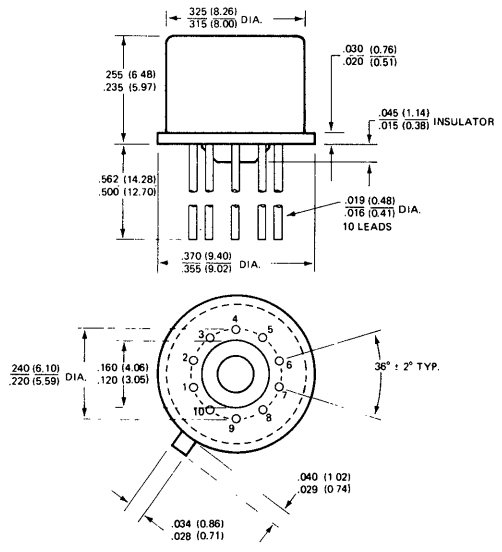


NOTES:

1. At high repetition rates and/or high capacitance loads, the transistors may require heat sinking, i.e., 1000 pF at 3MHz.
2. ½ N8822B, SP322B etc.
3. ½ N8880A, SP387A etc.

PACKAGE INFORMATION

K-PACKAGE



NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT– GOLD PLATED.
2. BODY MATERIAL: EYELET, KOVAR OR EQUIVALENT– GOLD PLATED GLASS BODY.
3. LID MATERIAL: NICKEL, WELD SEAL.
4. THERMAL RESISTANCE FROM JUNCTION TO CASE, Θ Jc = .025°C/mW, Θ Ja = .150°C/mW.
5. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

FULLY DECODED 1024 AND 2048 STATIC READ-ONLY MEMORIES

2400

METAL GATE MOS 2400 SERIES

DESCRIPTION

The Signetics 2400 Series devices are high speed, fully decoded, MOS static 1024 and 2048-bit read-only memories offering 128X8, 256X8, 256X4, and 512X4 organizations.

Two output structure options, plus both single line and 3-bit binary coded chip select options, provide for wide versatility and economy of application. The devices interface directly with standard TTL/DTL or MOS logic circuits. Process technology is P-Channel enhancement mode.

FEATURES

- **128X8, 256X8, 256X4, 512X4 ORGANIZATIONS**
- **STATIC OPERATION - NO CLOCKS**
- **FULLY DECODED ADDRESS**
- **500ns TYPICAL ACCESS TIME**
- **TTL/DTL COMPATIBILITY**
- **OUTPUT OPTIONS:**
  - **BARE DRAIN**
  - **20K OHM PULL-DOWN RESISTOR**
- **TWO CHIP SELECT OPTIONS:**
  - **SINGLE LINE**
  - **3-BIT BINARY CODED**
- **EBCDIC-ASCII CONVERSION TABLE IS CATALOG STANDARD, OTHER STANDARDS AVAILABLE**
- **+12, -12V POWER SUPPLIES**
- **STANDARD PINNING IN 16 AND 24 PIN CERAMIC DUAL IN-LINE PACKAGES**

APPLICATIONS:

CODE CONVERSION
LOOK-UP TABLES
MICRO-PROGRAMMING
RANDOM LOGIC SYNTHESIS
CHARACTER GENERATION

SPECIAL FEATURES

Output Options: Two output structure options allow ease of interfacing with TTL/DTL or other MOS circuits.

Chip Select Options: Both the 2420 and 2430 group may be specified with either single line chip select or a 3 line, 3-bit binary coded chip select. The coded chip select allows one-of-eight chip selection without external logic components for larger memory matrices. The 2410 group is pin limited to single line chip select

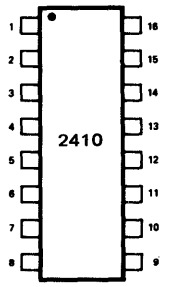
Package Options: The 256X4 organization is available in *either* a 16-pin or 24-pin dual in-line package.

For a detailed listing of part numbers and options see the PART IDENTIFICATION TABLE.

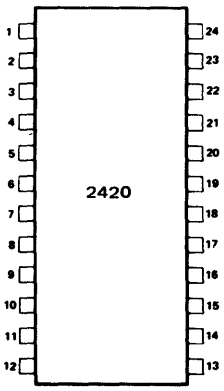
CUSTOM ENCODING

You may describe the particular option you desire in a booklet which will be provided by Signetics. Ask your local Signetics representative for a copy of "SIGNETICS 2400 SERIES STATIC READ-ONLY MEMORIES – MOS-ROM PROGRAMMING" The booklet contains a blank truth table and instructions for preparing punched data cards.

PIN CONFIGURATIONS (Top View)

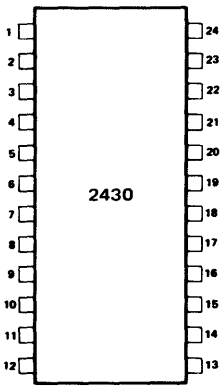


1.	Address 3	16.	V_{DD}
2.	Address 2	15.	Address 4
3.	Address 1	14.	Address 5
4.	Output 1	13.	Address 6
5.	Output 2	12.	Address 7
6.	Output 3	11.	V_{GG}
7.	Output 4	10.	Chip Enable
8.	V_{SS}	9.	Address 8



1.	Address 3	24.	V_{DD}
2.	Address 2	23.	Chip Enable 3*
3.	Address 1	22.	Chip Enable 2*
4.	Output 1	21.	Address 4
5.	Output 2	20.	Address 5
6.	Output 3	19.	Address 6
7.	Output 4	18.	Address 7
8.	Output 5	17.	V_{GG}
9.	Output 6	16.	Mode Control
10.	Output 7	15.	Chip Enable
11.	Output 8	14.	Address 8
12.	V_{SS}	13.	No Connection

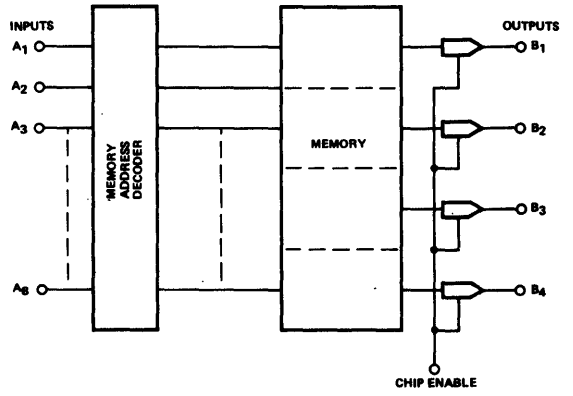
*No connection for single chip enable options.



1.	Address 3	24.	V_{DD}
2.	Address 2	23.	Chip Enable 3*
3.	Address 1	22.	Chip Enable 2*
4.	Output 1	21.	Address 4
5.	Output 2	20.	Address 5
6.	Output 3	19.	Address 6
7.	Output 4	18.	Address 7
8.	Output 5	17.	Address 8
9.	Output 6	16.	V_{GG}
10.	Output 7	15.	Mode Control
11.	Output 8	14.	Chip Enable
12.	V_{SS}	13.	Address 9

*No connection for single chip enable options.

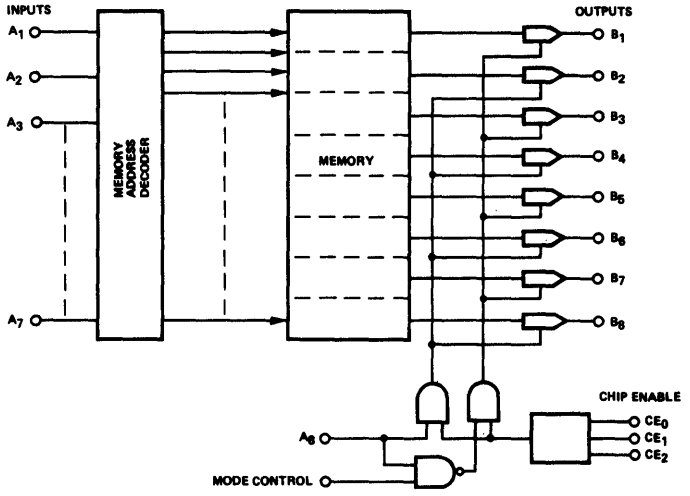
BLOCK DIAGRAMS



2410

OPERATING MODE

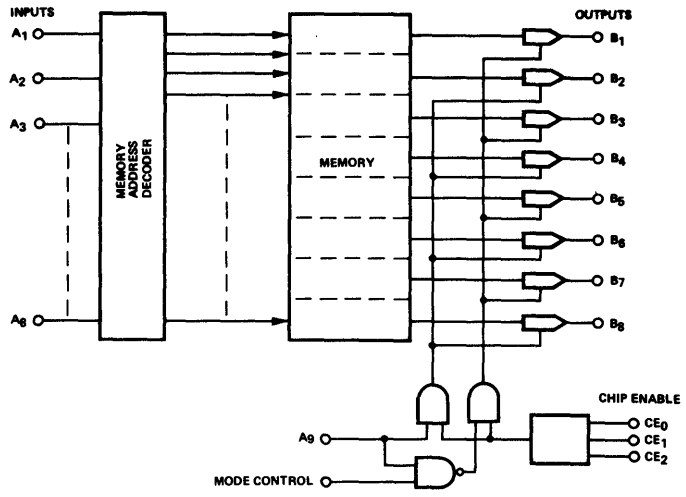
1. Logic "1" level enables outputs.



2420

OPERATING MODES

1. 128 x 8 ROM Connections
   Mode Control – Logic "0"
   A 8 – Logic "1"
2. 256 x 4 ROM Connection
   Mode Control – Logic "1"
   A8 – Logic "0" Enables the odd (B1, B3, B5, B7) outputs.
   – Logic "1" Enables the even (B2, B4, B6, B8) outputs
3. CE_0, CE_1, and CE_2 are AND'ed per customer instructions.



2430

OPERATING MODES

1. 256 x 8 ROM Connection
   Mode Control – Logic "0"
   A9 – Logic "1"
2. 512 x 4 ROM Connection
   Mode Control – Logic "1"
   A9 – Logic "0" Enables the odd (B1, B3 . . B7) Outputs
   – Logic "1" Enables the even (B2, B4...B8) Outputs
3. CE_0, CE_1, and CE_2 are AND'ed per customer instructions.

ABSOLUTE MAXIMUM RATINGS

Operating Ambient Temperature		-25°C to +70°C
Storage Temperature		-65°C to + 150°C
Power Dissipation (2)	("Y" Package)	@70°C 1.14W
	("I" Package)	@70°C 0.80W
V_{GG} (3)		-30 to +0.3
V_{DD} (3)		-30 to +0.3
Input Voltage (3, 4)		-30 to +0.3

DC CHARACTERISTICS

T_A = -25°C to +70°C; V_{SS} = +12V (17); V_{DD} = 0V; V_{GG} = -12V ±10% unless otherwise noted (Notes: 10, 11, 12, 13, 14, 16).

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
V_{IL}	Input Logic "0"	10			V	
V_{IH}	Input Logic "1"			4	V	
I_{SS}	V_{SS} Power Supply Current		14	20	mA	T_A = 25°C
I_{GG}	V_{GG} Power Supply Current			1	μA	Note 5, T_A = 25°C
I_{IH}	Input Leakage			1	μA	V_{IN} = 0V
R_{PD}	Pull-down Resistor					Note 6
	2410, 20 25, 30, 35		12	20	k ohm	

AC CHARACTERISTICS

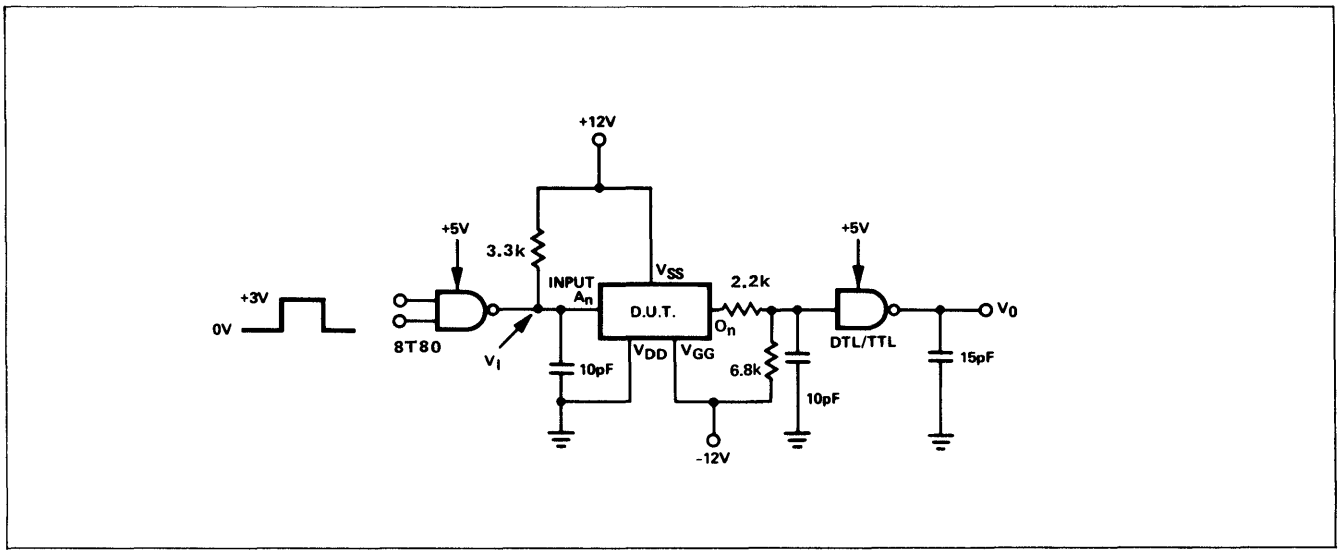
T_A = 25°C; V_{SS} = +12V (17); V_{DD} = 0V; V_{GG} = -12V ±10% unless otherwise noted . (Notes: 11, 12, 13, 14, 16).

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OL}	Output Logic "0" MOS to MOS	11			V	1 Megohm to Ground, Note 8
V_{OH}	Output Logic "1" MOS to MOS			+3	V	1 Megohm to Ground, Note 8
V_{OL}	Output Logic "0" MOS to TTL	+2.5			V	Note 7, 9
V_{OH}	Output Logic "1" MOS to TTL			+0.4	V	Note 7, 9
t_{A1}	Address Time (bare drain)		500	750	ns	Note 15
t_{A0}	Address Time (bare drain)		400	500	ns	

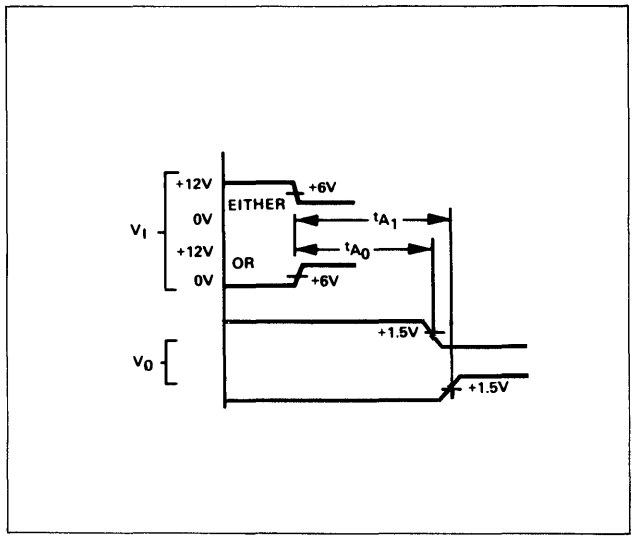
NOTES:

1. Stresses above those listed under "Maximum Guaranteed Ratings" may cause permanent damage to the device. This is a stress rating only. Operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied.
2. For operation at elevated temperatures, the device must be derated based on a maximum junction temperature of 150°C and a thermal resistance of 70°C/W junction to ambient for the "Y" package. The "I" package is derated based on 100°C/W junction to ambient.
3. These voltages are referenced to network ground terminal (V_{SS}).
4. All inputs are protected against damage by static charge.
5. The V_{GG} supply may be clocked to reduce device power without affecting access time.
6. Output to V_{DD}.
7. 6.8kΩ to V_{GG} plus 1 standard TTL gate input.
8. This test is for devices using a 20kΩ MOS pull-down resistor (2410, 20, 25, 30, 35,).
9. This test is for devices supplied with a bare drain output (2411, 21, 26, 31, 36).
10. Parameter valid over operating temperature range unless otherwise specified.
11. All voltage measurements referenced to ground.
12. Manufacturer reserves the right to make design changes and process improvements.
13. Typical values are at 25°C and nominal supply voltages.
14. Negative logic definition is employed for this device, i.e., more negative level is logic "1", most positive level is logic "0".
15. For bare drain devices, T_{A1} is primarily a function of the time constant of the load capacitance and external load resistor ($t_{A1} \cong 4R_L C_L$ +50ns).
16. CAUTION: These devices will be permanently damaged if reversed in board or socket.
17. V_{CC} tolerance is ±10%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH}, and V_{OH} which are stated for a V_{CC} of exactly 12 volts.

AC TEST SETUP

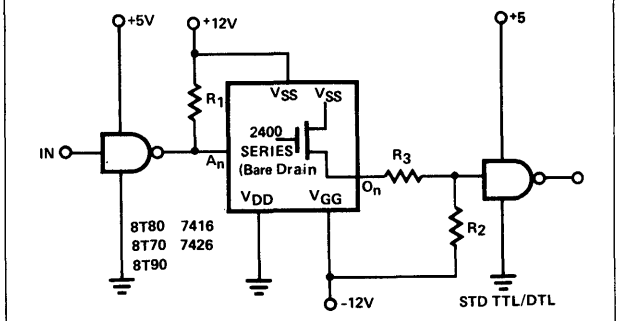


TIMING DIAGRAM



APPLICATIONS

TTL-MOS-TTL INTERFACING



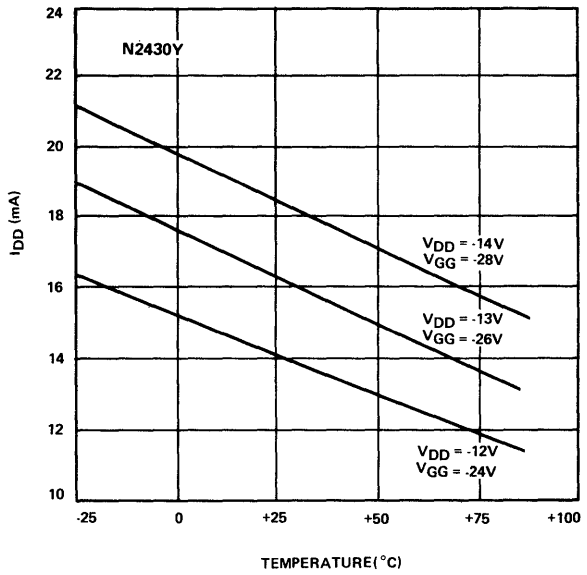
R_1 may range from 680Ω to 33k, typically 3.3k is satisfactory.
R_2 6.8k for a standard TTL (I_o IN = 1.6mA)
R_3 = 2.2k

PART IDENTIFICATION TABLE

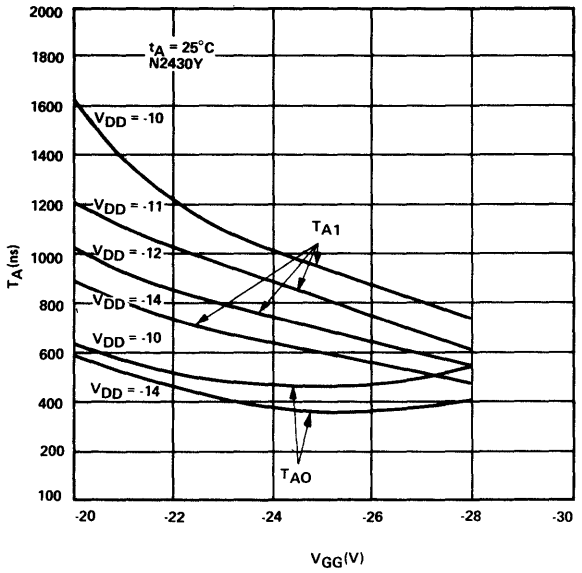
PART	ORGANIZATION	PACKAGE	OUTPUTS	CHIP SELECT CONTROLS
N2410I	256 x 4	16-pin Cer. DIP	20k ohm Pull-down	1
N2411I	256 x 4	16-pin Cer. DIP	Bare Drain	1
N2420Y	128 x 8 or 256 x 4	24-pin Cer. DIP	20k ohm Pull-down	1
N2421Y	128 x 8 or 256 x 4	24-pin Cer. DIP	Bare Drain	1
N2425Y	128 x 8 or 256 x 4	24-pin Cer. DIP	20k ohm Pull-down	3
N2426Y	128 x 8 or 256 x 4	24-pin Cer. DIP	Bare Drain	3
N2430Y/CM000	256 x 8 (EBCDIC-ASCII)	24-pin Cer. DIP	20k ohm Pull-down	1
N2430Y	256 x 8 or 512 x 4	24-pin Cer. DIP	20k ohm Pull-down	1
N2431Y	256 x 8 or 512 x 4	24-pin Cer. DIP	Bare Drain	1
N2435Y	256 x 8 or 512 x 4	24-pin Cer. DIP	20k ohm Pull-down	3
N2436Y	256 x 8 or 512 x 4	24-pin Cer. DIP	Bare Drain	3

CHARACTERISTIC CURVES

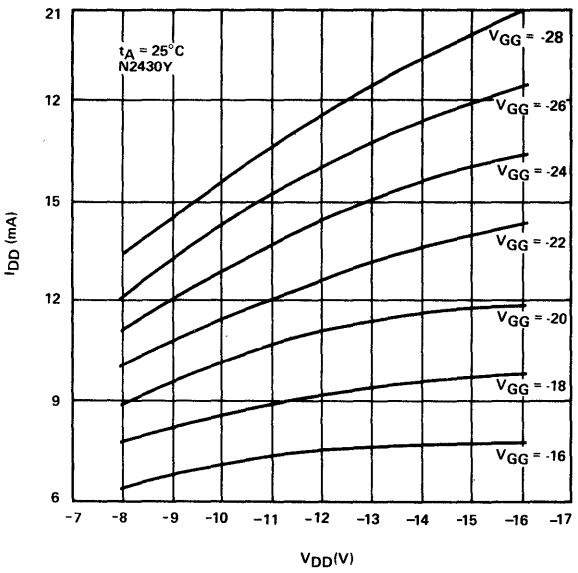
I_{DD} VERSUS TEMPERATURE AND POWER SUPPLY VOLTAGE



ACCESS TIME VERSUS SUPPLY VOLTAGE



I_{DD} VERSUS SUPPLY VOLTAGE



NOTE: For typical curves, V_{SS} = OV.

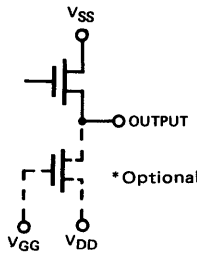
NOTE: Blanks are logic 1's.

CM0000 TRUTH TABLE

EBCDIC WORD #	ASCII Code Bit Number 1 2 3 4 5 6 7	EBCDIC WORD #	ASCII Code Bit Number 1 2 3 4 5 6 7	EBCDIC WORD #	ASCII Code Bit Number 1 2 3 4 5 6 7	EBCDIC WORD #	ASCII Code Bit Number 1 2 3 4 5 6 7
0	0 0 0 0 0 0 0	65		130	0 1 0 0 0 1 1	195	1 1 0 0 0 0 1
1	1 0 0 0 0 0 0	66		131	1 1 0 0 0 1 1	196	0 0 1 0 0 0 1
2	0 1 0 0 0 0 0	67		132	0 0 1 0 0 1 1	197	1 0 1 0 0 0 1
3	1 1 0 0 0 0 0	68		133	1 0 1 0 0 1 1	198	0 1 1 0 0 0 1
4		69		134	0 1 1 0 0 1 1	199	1 1 1 0 0 0 1
5	0 1 1 0 0 0 0	70		135	1 1 1 0 0 1 1	200	0 0 0 1 0 0 1
6		71		136	0 0 0 1 0 1 1	201	1 0 0 1 0 0 1
7	1 1 1 1 1 1 1	72		137	1 0 0 1 0 1 1	202	
8		73		138		203	
9		74		139		204	
10		75	0 1 1 1 0 1 0	140		205	
11	1 1 0 1 0 0 0	76	0 0 1 1 1 1 0	141		106	
12	0 0 1 1 0 0 0	77	0 0 0 1 0 1 0	142		207	
13	1 0 1 1 0 0 0	78	1 1 0 1 0 1 0	143		208	
14	0 1 1 1 0 0 0	79	0 0 1 1 1 1 1	144		209	0 1 0 1 0 0 1
15	1 1 1 1 0 0 0	80	0 1 1 0 0 1 0	145	0 1 0 1 0 1 1	210	1 1 0 1 0 0 1
16	0 0 0 0 1 0 0	81		146	1 1 0 1 0 1 1	211	1 1 1 1 1 1 1
17	1 0 0 0 1 0 0	82		147	0 0 1 1 0 1 1	212	1 0 1 1 0 0 1
18	0 1 0 0 1 0 0	83		148	1 0 1 1 0 1 1	213	0 1 1 1 0 0 1
19	1 1 0 0 1 0 0	84		149	0 1 1 1 0 1 1	214	1 1 1 1 0 0 1
20		85		150	1 1 1 1 0 1 1	215	0 0 0 0 1 0 1
21		86		151	0 0 0 0 1 1 1	216	1 0 0 0 1 0 1
22	0 0 0 1 0 0 0	87		152	1 0 0 0 1 1 1	217	0 1 0 0 1 0 1
23		88		153	0 1 0 0 1 1 1	218	
24	0 0 0 1 1 0 0	89		154		219	
25	1 0 0 1 1 0 0	90	1 0 0 0 0 1 0	155		220	
26		91	0 0 1 0 0 1 0	156		221	
27		92	0 1 0 1 0 1 0	157		222	
28	0 0 1 1 1 0 0	93	1 0 0 1 0 1 0	158		223	
29	1 0 1 1 1 0 0	94	1 1 0 1 1 1 0	159		224	
30	0 1 1 1 1 0 0	95		160		225	
31	1 1 1 1 1 0 0	96	1 0 1 1 0 1 0	161		226	1 1 0 0 1 0 1
32		97	1 1 1 1 0 1 0	162	1 1 0 0 1 1 1	227	0 0 1 0 1 0 1
33		98		163	0 0 1 0 1 1 1	228	1 0 1 0 1 0 1
34		99		164	1 0 1 0 1 1 1	229	0 1 1 0 1 0 1
35		100		165	0 1 1 0 1 1 1	230	1 1 1 0 1 0 1
36		101		166	1 1 1 0 1 1 1	231	0 0 0 1 1 0 1
37	0 1 0 1 0 0 0	102		167	0 0 0 1 1 1 1	232	1 0 0 1 1 0 1
38	1 1 1 0 1 0 0	103		168	1 0 0 1 1 1 1	233	0 1 0 1 1 0 1
39	1 1 0 1 1 0 0	104		169	0 1 0 1 1 1 1	234	
40		105		170		235	
41		106		171		236	
42		107	0 0 1 1 0 1 0	172		237	
43		108	1 0 1 0 0 1 0	173		238	
44		109	1 1 1 1 1 0 1	174		239	
45	1 0 1 0 0 0 0	110	0 1 1 1 1 1 0	175		240	0 0 0 0 1 1 0
46	0 1 1 0 0 0 0	111	1 1 1 1 1 1 0	176		241	1 0 0 0 1 1 0
47	1 1 1 0 0 0 0	112		177		242	0 1 0 0 1 1 0
48		113		178		243	1 1 0 0 1 1 0
49		114		179		244	0 0 1 0 1 1 0
50	0 1 1 0 1 0 0	115		180		245	1 0 1 0 1 1 0
51		116		181		246	0 1 1 0 1 1 0
52		117		182		247	1 1 1 0 1 1 0
53		118		183		248	0 0 0 1 1 1 0
54		119		184		249	1 0 0 1 1 1 0
55	0 0 1 0 0 0 0	120		185		250	
56		121		186		251	
57		122	0 1 0 1 1 1 0	187		252	
58		123	1 1 0 0 0 1 0	188		253	
59		124	0 0 0 0 0 0 1	189		254	
60	0 0 1 0 1 0 0	125	1 1 1 0 0 1 0	190		255	
61	1 0 1 0 1 0 0	126	1 0 1 1 1 1 0	191			
62		127	0 1 0 0 0 1 0	192			
63	0 1 0 1 1 0 0	128		193	1 0 0 0 0 0 1		
64	0 0 0 0 0 1 0	129	1 0 0 0 0 1 1	194	0 1 0 0 0 0 1		

SCHEMATIC DIAGRAM

OUTPUT STRUCTURE



*Optional 20K MOS pulldown resistor
N2410,20,25,30 and 35 only

EXERPT FROM SOFTWARE PACKAGE (CARD FORMAT)

CARD 1

COLUMN	DATA
1 8	STARTING AT COLUMN 1 PUNCH "CODED" OR "SINGLE"
9 11*	IF "CODED", PUNCH THE BINARY CODE CHIP SELECT (i e , 101) IF "SINGLE" LEAVE BLANK.
12	LEAVE BLANK
13 17	PUNCH THE ROM ORGANIZATION DESIRED i e , 8 X 256, 4 X 512, ETC
18	BLANK
19 21	PUNCH MOS FOR AN MOS OUTPUT PUNCH TTL FOR A TTL OUTPUT (BARE DRAIN)
22 27	BLANK
28 33	PUNCH THE BASIC DEVICE TYPE DESIRED i e , N2410, N2420Y, ETC.
34 80	COMMENTS PUNCHED HERE WILL APPEAR AS THE TITLE ON THE TRUTH TABLE THIS SHOULD INCLUDE CUSTOMER PART IDENTIFICATION

* CE_3, CE_2 and CE_1 respectively

CARD 2 THROUGH 129 (8 X 128Organization)
2 THROUGH 256 (8 X 256 Organization)

EACH CARD SPECIFIES THE OUTPUT OF ONE 8-BIT WORD IN COLUMNS 1 THROUGH 8. THE DECIMAL EQUIVALENT OF THE BINARY CODED INPUT ADDRESS FOR THAT WORD IS PUNCHED IN COLUMNS 78, 79 AND 80.

COLUMNS	DATA
1 8	PUNCH OUTPUTS B1 THROUGH B8 IN COLUMNS ONE THROUGH EIGHT RESPECTIVELY.
9 77	LEAVE BLANK
78 80	PUNCH DECIMAL EQUIVALENT OF BINARY CODED INPUT ADDRESS WHICH CORRESPONDS TO THE OUTPUTS PUNCHED IN COLUMNS 1-8 COLUMN 78 HUNDREDS DIGIT COLUMN 79 TENS DIGIT COLUMN 80 UNITS DIGIT

CARDS 2 THROUGH 129 (4 X 256 Organization only)

EACH CARD SPECIFIES THE OUTPUT OF TWO 4-BIT WORDS IN COLUMNS 1 THROUGH 8. THE DECIMAL EQUIVALENT OF THE BINARY CODED INPUT ADDRESS IS PUNCHED IN COLUMNS 78, 79, AND 80.

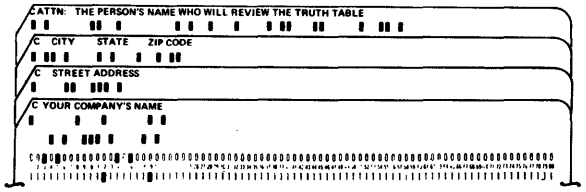
COLUMN	DATA
1 4	PUNCH OUTPUT FOR WORDS 0 255
5 8	PUNCH OUTPUT FOR WORDS 256 511
9 77	LEAVE BLANK
78 80	PUNCH DECIMAL EQUIVALENT OF BINARY CODED INPUT ADDRESS OF THE WORD CORRESPONDING TO THE OUTPUTS PUNCHED IN COLUMNS 1 4 COLUMN 78 HUNDREDS DIGIT COLUMN 79 TENS DIGIT COLUMN 80 UNITS DIGIT

CARDS 2 THROUGH 257 (4 X 512 Organization only)

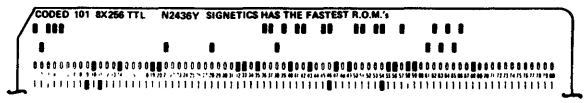
EACH CARD SPECIFIES THE OUTPUT OF TWO 4-BIT WORDS IN COLUMNS 1 THROUGH 8. THE DECIMAL EQUIVALENT OF THE BINARY CODED INPUT ADDRESS IS PUNCHES IN COLUMNS 78, 79, AND 80.

COLUMN	DATA
1 4	PUNCH OUTPUT FOR WORDS 0 127
5 8	PUNCH OUTPUT FOR WORDS 128 255
9 77	LEAVE BLANK
78 80	PUNCH DECIMAL EQUIVALENT OF BINARY CODED INPUT ADDRESS CORRESPONDING TO THE OUTPUTS PUNCHED IN COLUMNS 1 4. COLUMN 78 HUNDREDS DIGIT COLUMN 79 TENS DIGIT COLUMN 80 UNITS DIGIT

EXAMPLE:
ADDRESS CARDS

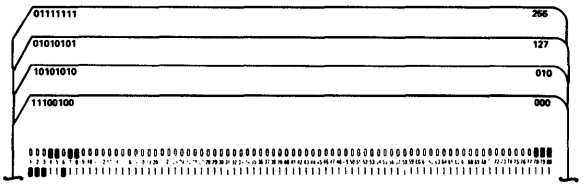


EXAMPLE:
CARD 1



THE ABOVE SPECIFIES A "CODED" ROM WITH THE BINARY CODED CHIP SELECT "101" ORGANIZED 8 X 256 WITH TTL OUTPUTS (BARE DRAIN). THE BASIC DEVICE TYPE IS A N2436Y ("Y" INDICATES A 24-PIN CERAMIC DIP. N INDICATES TEMPERATURE RANGE: -25°C – +70°C.)

EXAMPLE:
CARDS 2-129 AND CARDS 2-257



- OUTPUTS B1 THROUGH B8 ARE IN COLUMNS 1 THROUGH 8 RESPECTIVELY.
- DECIMAL EQUIVALENT OF BINARY CODED INPUT ADDRESS IS IN COLUMNS 78, 79, AND 80.
- FOR 8 X 128 AND 8 X 256 ORGANIZATIONS – OUTPUTS ARE B1 THROUGH B8 RESPECTIVELY.
- FOR 4 X 512 ORGANIZATION:

DATA CARD 0	WORD 000 OUTPUTS B1 THROUGH B4 RESPECTIVELY WORD 256 OUTPUTS B5 THROUGH B8 RESPECTIVELY
DATA CARD 10	WORD 010 OUTPUTS B1 THROUGH B4 RESPECTIVELY WORD 266 OUTPUTS B5 THROUGH B8 RESPECTIVELY

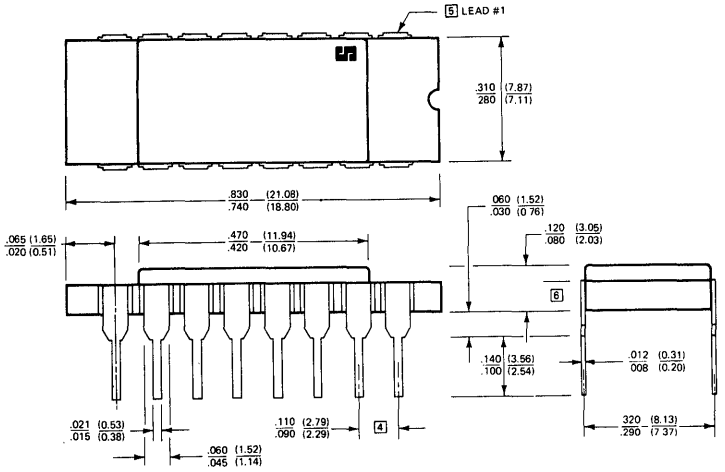
ETC.

- FOR 4 X 256 ORGANIZATION:

DATA CARD 0	WORD 000 OUTPUTS B1 THROUGH B4 RESPECTIVELY WORD 128 OUTPUTS B5 THROUGH B8 RESPECTIVELY
DATA CARD 10	WORD 010 OUTPUTS B1 THROUGH B4 RESPECTIVELY WORD 138 OUTPUTS B5 THROUGH B8 RESPECTIVELY

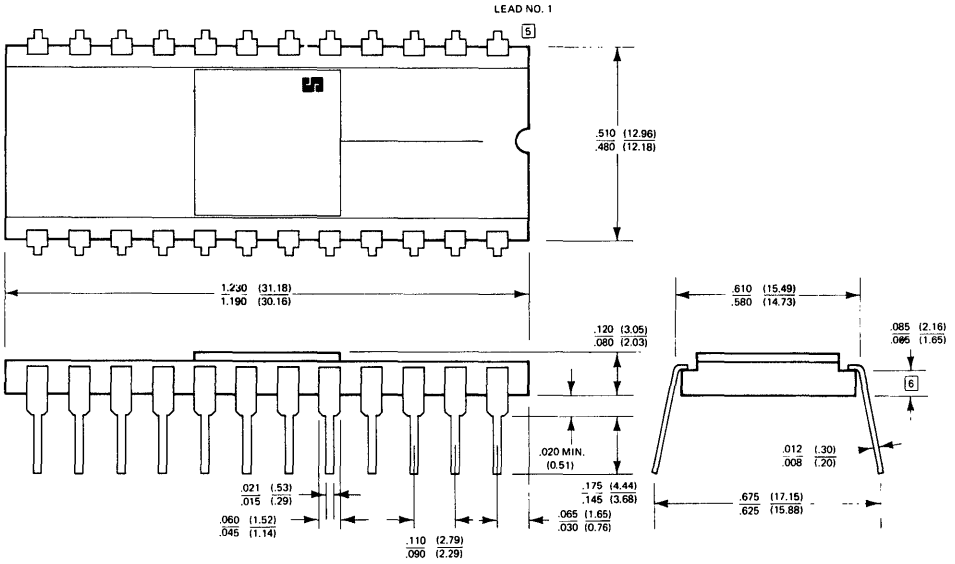
PACKAGE INFORMATION

I PACKAGE



NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED.
2. BODY MATERIAL: CERAMIC WITH KOVAR OR EQUIVALENT. TOP RING GOLD PLATED.
3. LID MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED, ALLOY SEAL.
4. TOLERANCES NON CUMULATIVE.
5. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
6. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
7. THERMAL RESISTANCE: Θ Ja = .062 C/mW, Θ Jc = .018 C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

Y PACKAGE



NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED.
2. BODY MATERIAL: CERAMIC WITH KOVAR OR EQUIVALENT.
3. LID MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED, ALLOY SEAL.
4. TOLERANCES NON CUMULATIVE.
5. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
6. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
7. THERMAL RESISTANCE: Θ Ja = .050°C/mW, Θ Jc = .010°C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

FULLY DECODED 1024 AND 2048 STATIC READ-ONLY MEMORIES

2441 2451 2461 2462

METAL GATE MOS

DESCRIPTION

These Signetics devices are high speed, fully decoded, MOS static 1024 and 2048-bit read-only memories offering 128X8, 126X4, and 512X4 organizations.

Both single line and 3-bit binary coded chip select options, provide for wide versatility and economy of application. The devices interface directly with standard TTL/DTL logic circuits. Process technology is P-Channel enhancement mode.

FEATURES

- 128X8, 256X8, 256X4, 512X4 ORGANIZATIONS
- STATIC OPERATION - NO CLOCKS
- FULLY DECODED ADDRESS
- ACCESS TIME 950ns MAX.
- TTL/DTL COMPATIBILITY
- BARE DRAIN OUTPUT
- TWO CHIP SELECT OPTIONS:
  - SINGLE LINE
  - 3-BIT BINARY CODED
- EBCDIC-ASCII CONVERSION TABLE IS CATALOG STANDARD, OTHER STANDARDS AVAILABLE
- +5, -12V POWER SUPPLIES
- STANDARD PINNING IN 16 AND 24 PIN CERAMIC DUAL IN-LINE PACKAGES

APPLICATIONS

CODE CONVERSION
LOOK-UP TABLES
MICRO-PROGRAMMING
RANDOM LOGIC SYNTHESIS
CHARACTER GENERATION

SPECIAL FEATURES

Chip Select Options: Both the 2451 and 2461 may be specified with either single line chip select or a 3 line, 3-bit binary coded chip select. The coded chip select allows one-of-eight chip selection without external logic components for larger memory matrices. The 2441 and 2462 are pin limited to single line chip select.

Package Options: The 256X4 organization is available in *either* a 16-pin or 24-pin dual in-line package.

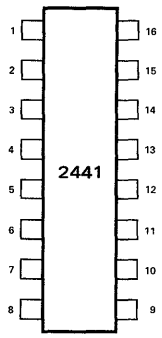
For a detailed listing of part numbers and options see the PART IDENTIFICATION TABLE.

CUSTOM ENCODING

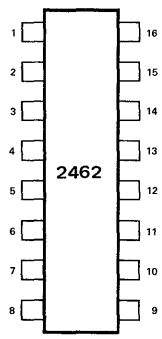
You may describe the particular option you desire in a booklet which will be provided by Signetics. Ask your local Signetics representative for a copy of "SIGNETICS 2400 SERIES STATIC READ-ONLY MEMORIES – MOS-ROM PROGRAMMING". The booklet contains a blank truth table and instructions for preparing punched data cards.

PIN CONFIGURATIONS (Top View)

I PACKAGE

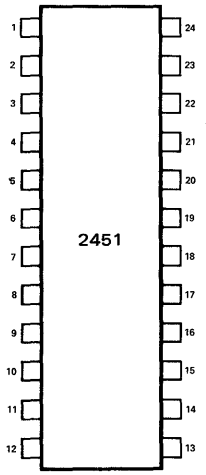


1. Address 3
2. Address 2
3. Address 1
4. Output 1
5. Output 2
6. Output 3
7. Output 4
8. V_{SS}
9. Address 8
10. Chip Enable
11. V_{GG}
12. Address 7
13. Address 6
14. Address 5
15. Address 4
16. V_{DD}



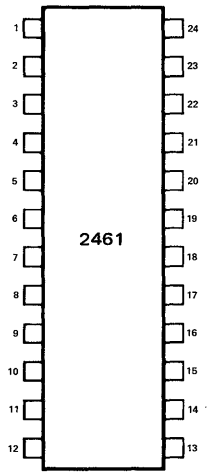
1. Address 3
2. Address 2
3. Address 1
4. Output 1
5. Output 2
6. Output 3
7. Output 4
8. V_{SS}
9. Address 9
10. Chip Enable
11. V_{GG}, V_{DD}
12. Address 8
13. Address 7
14. Address 6
15. Address 5
16. Address 4

Y PACKAGE



1. Address 3
2. Address 2
3. Address 1
4. Output 1
5. Output 2
6. Output 3
7. Output 4
8. Output 5
9. Output 6
10. Output 7
11. Output 8
12. V_{SS}
13. No Connection
14. Address 8
15. Chip Enable
16. Mode Control
17. V_{GG}
18. Address 7
19. Address 6
20. Address 5
21. Address 4
22. Chip Enable 2*
23. Chip Enable 3*
24. V_{DD}

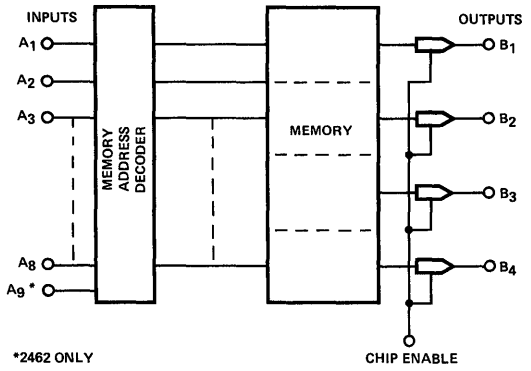
* No connection for single chip enable options.



1. Address 3
2. Address 2
3. Address 1
4. Output 1
5. Output 2
6. Output 3
7. Output 4
8. Output 5
9. Output 6
10. Output 7
11. Output 8
12. V_{SS}
13. Address 9
14. Chip Enable
15. Mode Control
16. V_{GG}
17. Address 8
18. Address 7
19. Address 6
20. Address 5
21. Address 4
22. Chip Enable 2*
23. Chip Enable 3*
24. V_{DD}

*No connection for single chip enable options.

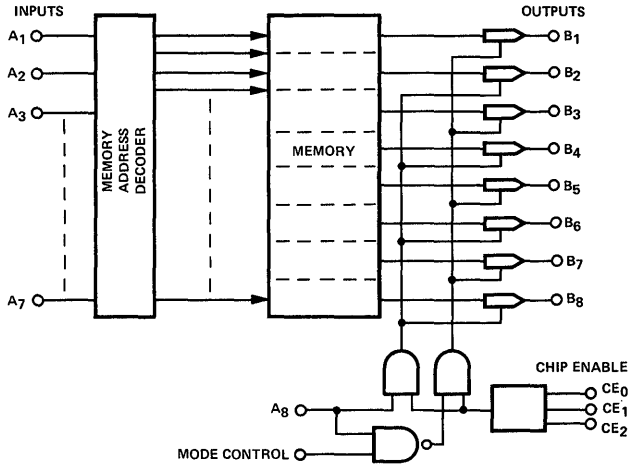
BLOCK DIAGRAMS



2441, 2462

OPERATING MODE

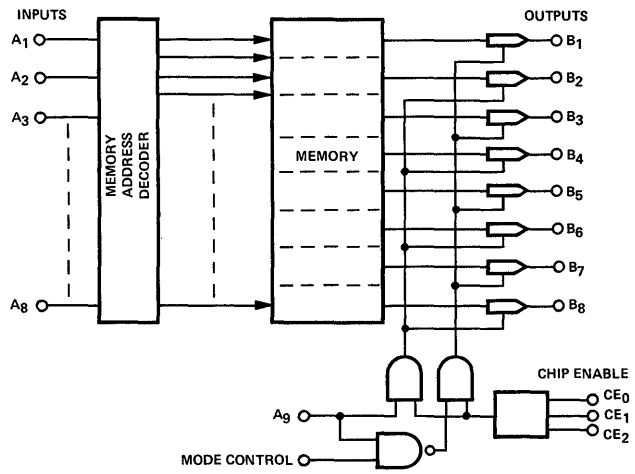
1. Logic "1" level enables outputs.



2451

OPERATING MODES

1. 128 x 8 ROM Connections
   Mode Control – Logic "0"
   A8 – Logic "1"
2. 256 x 4 ROM Connection
   Mode Control – Logic "1"
   A8 – Logic "0" Enables the odd (B1, B3, B5, B7) outputs.
   – Logic "1" Enables the even (B2, B4, B6, B8) outputs
3. CE_0, CE_1, and CE_2 are AND'ed per customer instructions.



2461

OPERATING MODES

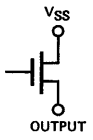
1. 256 x 8 ROM Connection
   Mode Control – Logic "0"
   A9 – Logic "1"
2. 512 x 4 ROM Connection
   Mode Control – Logic "1"
   A9 – Logic "0" Enables the odd (B1, B3 . . B7) Outputs
   – Logic "1" Enables the even (B2, B4. . B8) Outputs
3. CE_0, CE_1, and CE_2 are AND'ed per customer instructions.

ABSOLUTE MAXIMUM RATINGS (1)

Operating Ambient Temperature		$-25^{\circ}C$ to $+70^{\circ}C$
Storage Temperature		$-65^{\circ}C$ to $+150^{\circ}C$
Power Dissipation (2)	("Y" Package)	@$70^{\circ}C$ 1.14W
	("I" Package)	@$70^{\circ}C$ 0.80W
V_{GG}(3)		−20 to +0.3
V_{DD}(3)		−15 to +0.3
Input Voltage (3,4)		−20 to +0.3

SCHEMATIC DIAGRAM

OUTPUT STRUCTURE



DC CHARACTERISTICS

$T_A = -25^{\circ}C$ to $+70^{\circ}C$; $V_{SS} = +5V \pm 5\%$; $V_{DD} = V_{GG} = -12V \pm 5\%$ unless otherwise noted (Notes: 8, 9, 10, 11, 12, 14)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
V_{IL}	Input Logic "0"	3			V	
V_{IH}	Input Logic "1"			0.8	V	
I_{SS}	V_{SS} Power Supply Current		14	20	mA	$T_A = 25^{\circ}C$
I_{GG}	V_{GG} Power Supply Current			1	μA	Note 5, $T_A = 25^{\circ}C$
I_{IH}	Input Leakage			1	μA	$V_{IN} = -12V$

AC CHARACTERISTICS

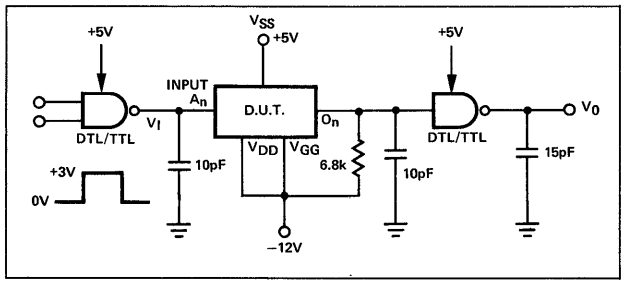
$T_A = 25^{\circ}C$; $V_{SS} = +5V \pm 5\%$; $V_{DD} = V_{GG} = -12V \pm 5\%$ unless otherwise noted (Notes 9, 10, 11, 12, 14)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OL}	Output Logic "0" MOS to TTL	+2.4			V	Note 6
V_{OH}	Output Logic "1"			+0.4	V	Note 6
t_{A1}	Access Time			750	ns	Note 13
t_{A0}	Access Time			950	ns	
C_{IN}	Input Capacitance		5		pF	Note 7, f = 1 MHz, $V_{IN} = 0$

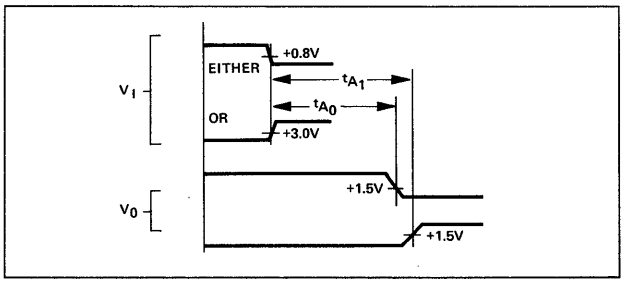
NOTES:

1. Stresses above those listed under "Maximum Guaranteed Ratings" may cause permanent damage to the device. This is a stress rating only. Operation of the device at those or any other conditions above those indicated in the operational sections of the specification is not implied.
2. For operation at elevated temperatures, the device must be derated based on a maximum junction temperature of $150^{\circ}C$ and a thermal resistance of $70^{\circ}C/W$ junction to ambient for the "Y" package. The "I" package is derated based on $100^{\circ}C/W$ junction to ambient.
3. These voltages are referenced to network ground terminal (V_{SS}).
4. All inputs are protected against damage by static charge.
5. The V_{GG} supply may be clocked to reduce device power without affecting access time.
6. 6.8kΩ to V_{GG} plus 1 standard TTL gate input.
7. Capacitance measured on lot sample basis only.
8. Parameter valid over operating temperature range unless otherwise specified.
9. All voltage measurements referenced to ground.
10. Manufacturer reserves the right to make design changes and process improvements.
11. Typical values are at $25^{\circ}C$ and nominal supply voltages.
12. Negative logic definition is employed for this device. i.e., more negative level is logic "1", most positive level is logic "0".
13. For bare drain devices, T_{A1} is primarily a function of the time constant of the load capacitance and external load resistor ($t_{A1} \cong 4R_L C_L$ +50 ns).
14. CAUTION: These devices will be permanently damaged if reversed in board or socket.

AC TEST SETUP



TIMING DIAGRAM



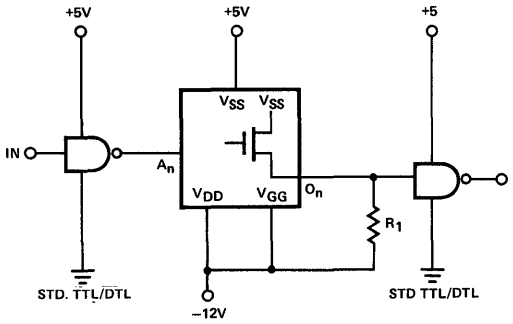
PART IDENTIFICATION TABLE

PART	ORGANIZATION	PACKAGE	OUTPUTS
N2441I	256 x 4	16-pin Cer. DIP	Bare Drain
N2451Y	128 x 8 or 256 x 4	24-pin Cer. DIP	Bare Drain
N2461Y/CM	256 x 8 (EBCDIC-ASCII)*	24-pin Cer. DIP	Bare Drain
N2461Y	256 x 8 or 512 x 4	24-pin Cer. DIP	Bare Drain
N2462I	512 x 4	16-pin Cer. DIP	Bare Drain

* Demonstrator

APPLICATIONS

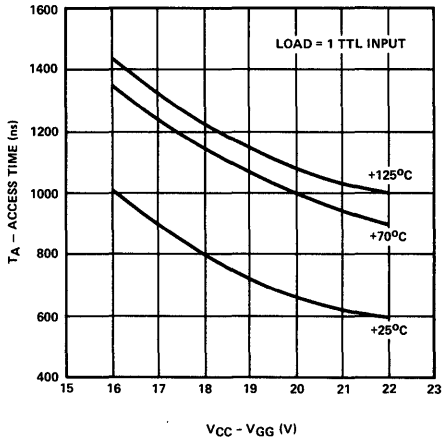
MOS-TTL INTERFACING



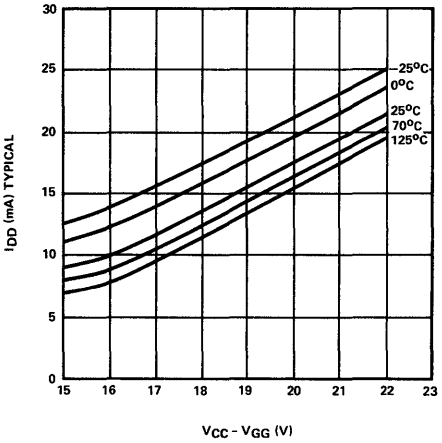
R_1 = 6.8k for a standard TTL (I_o IN = 1.6mA)

CHARACTERISTIC CURVES

TYPICAL ACCESS TIME VS. SUPPLY VOLTAGE



TYPICAL POWER SUPPLY CURRENT VS. POWER SUPPLY VOLTAGE



NOTE: For typical curves, V_{SS} = 0V.

NOTE: Blanks are logic 1's.

CM 4030 TRUTH TABLE

EBCDIC WORD #	ASCII CODE BIT NUMBER 1	2	3	4	5	6	7	EBCDIC WORD #	ASCII CODE BIT NUMBER 1	2	3	4	5	6	7	EDCDIC WORD #	ASCII CODE BIT NUMBER 1	2	3	4	5	6	7	EBCDIC WORD #	ASCII CODE BIT NUMBER 1	2	3	4	5	6	7
0	0	0	0	0	0	0	0	65								130	0	1	0	0	0	1	1	195	1	1	0	0	0	0	1
1	1	0	0	0	0	0	0	66								131	1	1	0	0	0	1	1	196	0	0	1	0	0	0	1
2	0	1	0	0	0	0	0	67								132	0	0	1	0	0	1	1	197	1	0	1	0	0	0	1
3	1	1	0	0	0	0	0	68								133	1	0	1	0	0	1	1	198	0	1	1	0	0	0	1
4								69								134	0	1	1	0	0	1	1	199	1	1	1	0	0	0	1
5	0	1	1	0	0	0	0	70								135	1	1	1	0	0	1	1	200	0	0	0	1	0	0	1
6								71								136	0	0	0	1	0	1	1	201	1	0	0	1	0	0	1
7	1	1	1	1	1	1	1	72								137	1	0	0	1	0	1	1	202							
8								73								138								203							
9								74								139								204							
10								75	0	1	1	1	0	1	0	140								205							
11	1	1	0	1	0	0	0	76	0	0	1	1	1	1	0	141								206							
12	0	0	1	1	0	0	0	77	0	0	0	1	0	1	0	142								207							
13	1	0	1	1	0	0	0	78	1	1	0	1	0	1	0	143								208							
14	0	1	1	1	0	0	0	79	0	0	1	1	1	1	1	144								209	0	1	0	1	0	0	1
15	1	1	1	1	0	0	0	80	0	1	1	0	0	1	0	145	0	1	0	1	0	1	1	210	1	1	0	1	0	0	1
16	0	0	0	0	1	0	0	81								146	1	1	0	1	0	1	1	211	1	1	1	1	1	1	1
17	1	0	0	0	1	0	0	82								147	0	0	1	1	0	1	1	212	1	0	1	1	0	0	1
18	0	1	0	0	1	0	0	83								148	1	0	1	1	0	1	1	213	0	1	1	1	0	0	1
19	1	1	0	0	1	0	0	84								149	0	1	1	1	0	1	1	214	1	1	1	1	0	0	1
20								85								150	1	1	1	1	0	1	1	215	0	0	0	0	1	0	1
21								86								151	0	0	0	0	1	1	1	216	1	0	0	0	1	0	1
22	0	0	0	1	0	0	0	87								152	1	0	0	0	1	1	1	217	0	1	0	0	1	0	1
23								88								153	0	1	0	0	1	1	1	218							
24	0	0	0	1	1	0	0	89								154								219							
25	1	0	0	1	1	0	0	90	1	0	0	0	0	1	0	155								220							
26								91	0	0	1	0	0	1	0	156								221							
27								92	0	1	0	1	0	1	0	157								222							
28	0	0	1	1	1	0	0	93	1	0	0	1	0	1	0	158								223							
29	1	0	1	1	1	0	0	94	1	1	0	1	1	1	0	159								224							
30	0	1	1	1	1	0	0	95								160								225							
31	1	1	1	1	1	0	0	96	1	0	1	1	0	1	0	161								226	1	1	0	0	1	0	1
32								97	1	1	1	1	0	1	0	162	1	1	0	0	1	1	1	227	0	0	1	0	1	0	1
33								98								163	0	0	1	0	1	1	1	228	1	0	1	0	1	0	1
34								99								164	1	0	1	0	1	1	1	229	0	1	1	0	1	0	1
35								100								165	0	1	1	0	1	1	1	230	1	1	1	0	1	0	1
36								101								166	1	1	1	0	1	1	1	231	0	0	0	1	1	0	1
37	0	1	0	1	0	0	0	102								167	0	0	0	1	1	1	1	232	1	0	0	1	1	0	1
38	1	1	1	0	1	0	0	103								168	1	0	0	1	1	1	1	233	0	1	0	1	1	0	1
39	1	1	0	1	1	0	0	104								169	0	1	0	1	1	1	1	234							
40								105								170								235							
41								106								171								236							
42								107	0	0	1	1	0	1	0	172								237							
43								108	1	0	1	0	0	1	0	173								238							
44								109	1	1	1	1	1	0	1	174								239							
45	1	0	1	0	0	0	0	110	0	1	1	1	1	1	0	175								240	0	0	0	0	1	1	0
46	0	1	1	0	0	0	0	111	1	1	1	1	1	1	0	176								241	1	0	0	0	1	1	0
47	1	1	1	0	0	0	0	112								177								242	0	1	0	0	1	1	0
48								113								178								243	1	1	0	0	1	1	0
49								114								179								244	0	0	1	0	1	1	0
50	0	1	1	0	1	0	0	115								180								245	1	0	1	0	1	1	0
51								116								181								246	0	1	1	0	1	1	0
52								117								182								247	1	1	1	0	1	1	0
53								118								183								248	0	0	0	1	1	1	0
54								119								184								249	1	0	0	1	1	1	0
55	0	0	1	0	0	0	0	120								185								250							
56								121								186								251							
57								122	0	1	0	1	1	1	0	187								252							
58								123	1	1	0	0	0	1	0	188								253							
59								124	0	0	0	0	0	0	1	189								254							
60	0	0	1	0	1	0	0	125	1	1	1	0	0	1	0	190								255							
61	1	0	1	0	1	0	0	126	1	0	1	1	1	1	0	191															
62								127	0	1	0	0	0	1	0	192															
63	0	1	0	1	1	0	0	128	0	1	0	0	0	1	0	193	1	0	0	0	0	0	1								
64	0	0	0	0	0	1	0	129	1	0	0	0	0	1	1	194	0	1	0	0	0	0	1								

EXERPT FROM SOFTWARE PACKAGE (CARD FORMAT)

CARD 1

COLUMN	DATA
1 8	STARTING AT COLUMN 1 PUNCH "CODED" OR "SINGLE"
9 11*	IF "CODED", PUNCH THE BINARY CODE CHIP SELECT (i e , 101) IF "SINGLE" LEAVE BLANK
12	LEAVE BLANK
13 17	PUNCH THE ROM ORGANIZATION DESIRED (i e 8 X 256 4 X 512, ETC
18	BLANK
19 21	PUNCH MOS FOR AN MOS OUTPUT PUNCH TTL FOR A TTL OUTPUT (BARE DRAIN)
22 27	BLANK
28 33	PUNCH THE BASIC DEVICE TYPE DESIRED (i e N2401 N2420Y ETC
34 80	COMMENTS PUNCHED HERE WILL APPEAR AS THE TITLE ON THE TRUTH TABLE THIS SHOULD INCLUDE CUSTOMER PART IDENTIFICATION

* CE_3, CE_2 and CE_1 respectively

CARDS 2 THROUGH 129 (4 X 256 Organization only)

EACH CARD SPECIFIES THE OUTPUT OF TWO 4-BIT WORDS IN COLUMNS 1 THROUGH 8. THE DECIMAL EQUIVALENT OF THE BINARY CODED INPUT ADDRESS IS PUNCHED IN COLUMNS 78, 79, AND 80

COLUMN	DATA
1 4	PUNCH OUTPUT FOR WORDS 0 255
5 8	PUNCH OUTPUT FOR WORDS 256 511
9 77	LEAVE BLANK
78 80	PUNCH DECIMAL EQUIVALENT OF BINARY CODED INPUT ADDRESS OF THE WORD CORRESPONDING TO THE OUTPUTS PUNCHED IN COLUMNS 1 4 COLUMN 78 HUNDREDS DIGIT COLUMN 79 TENS DIGIT COLUMN 80 UNITS DIGIT

CARD 2 THROUGH 129 (8 X 128Organization)
2 THROUGH 256 (8 X 256 Organization)

EACH CARD SPECIFIES THE OUTPUT OF ONE 8 BIT WORD IN COLUMNS 1 THROUGH 8 THE DECIMAL EQUIVALENT OF THE BINARY CODED INPUT ADDRESS FOR THAT WORD IS PUNCHED IN COLUMNS 78, 79 AND 80.

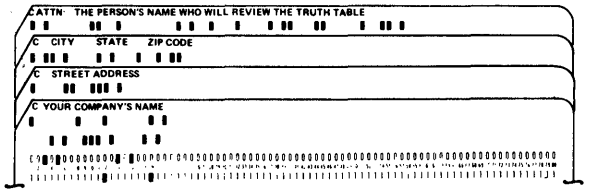
COLUMNS	DATA
1 8	PUNCH OUTPUTS B1 THROUGH B8 IN COLUMNS ONE THROUGH EIGHT RESPECTIVELY
9 77	LEAVE BLANK
78 80	PUNCH DECIMAL EQUIVALENT OF BINARY CODED INPUT ADDRESS WHICH CORRESPONDS TO THE OUTPUTS PUNCHED IN COLUMNS 1 8 COLUMN 78 HUNDREDS DIGIT COLUMN 79 TENS DIGIT COLUMN 80 UNITS DIGIT

CARDS 2 THROUGH 257(4 X 512 Organization only)

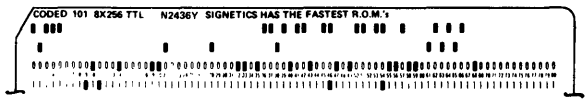
EACH CARD SPECIFIES THE OUTPUT OF TWO 4 BIT WORDS IN COLUMNS 1 THROUGH 8 THE DECIMAL EQUIVALENT OF THE BINARY CODED INPUT ADDRESS IS PUNCHES IN COLUMNS 78, 79, AND 80.

COLUMN	DATA
1 4	PUNCH OUTPUT FOR WORDS 0 127
5 8	PUNCH OUTPUT FOR WORDS 128 255
9 77	LEAVE BLANK
78 80	PUNCH DECIMAL EQUIVALENT OF BINARY CODED INPUT ADDRESS CORRESPONDING TO THE OUTPUTS PUNCHED IN COLUMNS 1 4 COLUMN 78 HUNDREDS DIGIT COLUMN 79 TENS DIGIT COLUMN 80 UNITS DIGIT

EXAMPLE:
ADDRESS CARDS

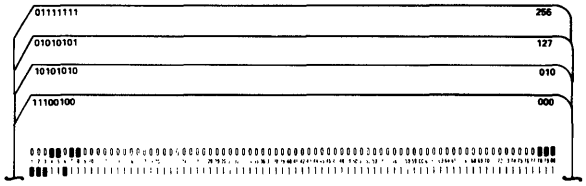


EXAMPLE
CARD 1



THE ABOVE SPECIFIES A "CODED" ROM WITH THE BINARY CODED CHIP SELECT "101" ORGANIZED 8 X 256 WITH TTL OUTPUTS (BARE DRAIN). THE BASIC DEVICE TYPE IS A N2436Y ("Y" INDICATES A 24-PIN CERAMIC DIP N INDICATES TEMPERATURE RANGE: -25 C – +70°C.)

EXAMPLE
CARDS 2 129 AND CARDS 2-257



- OUTPUTS B1 THROUGH B8 ARE IN COLUMNS 1 THROUGH 8 RESPECTIVELY.
- DECIMAL EQUIVALENT OF BINARY CODED INPUT ADDRESS IS IN COLUMNS 78, 79, AND 80
- FOR 8 X 128 AND 8 X 256 ORGANIZATIONS – OUTPUTS ARE B1 THROUGH B8 RESPECTIVELY
- FOR 4 X 512 ORGANIZATION:

DATA CARD 0	WORD 000 OUTPUTS B1 THROUGH B4 RESPECTIVELY WORD 256 OUTPUTS B5 THROUGH B8 RESPECTIVELY
DATA CARD 10	WORD 010 OUTPUTS B1 THROUGH B4 RESPECTIVELY WORD 266 OUTPUTS B5 THROUGH B8 RESPECTIVELY

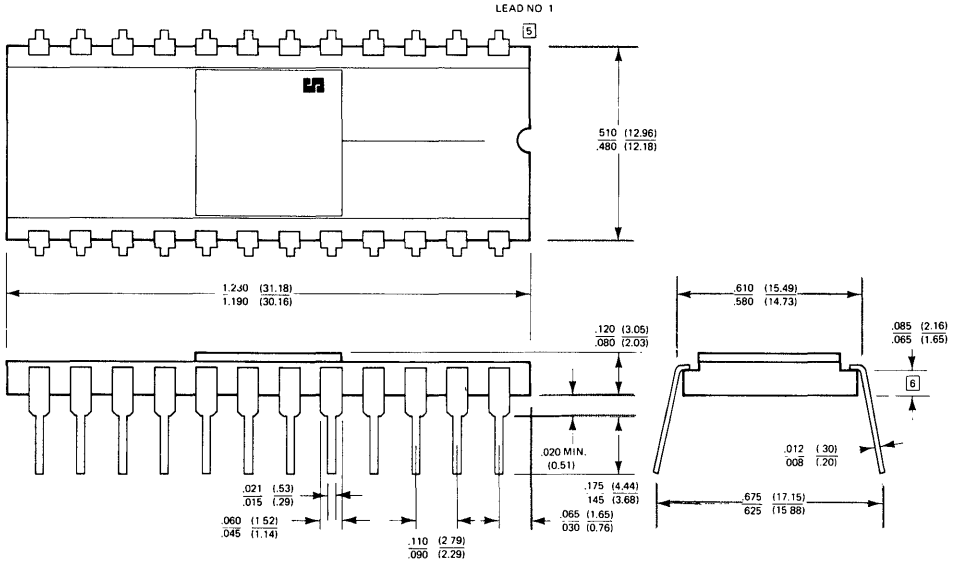
ETC.

- FOR 4 X 256 ORGANIZATION:

DATA CARD 0	WORD 000 OUTPUTS B1 THROUGH B4 RESPECTIVELY WORD 128 OUTPUTS B5 THROUGH B8 RESPECTIVELY
DATA CARD 10	WORD 010 OUTPUTS B1 THROUGH B4 RESPECTIVELY WORD 138 OUTPUTS B5 THROUGH B8 RESPECTIVELY

PACKAGE INFORMATION

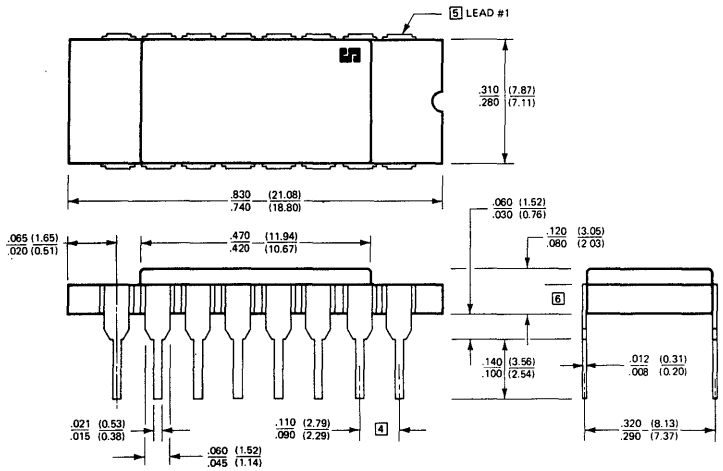
Y PACKAGE



NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED.
2. BODY MATERIAL: CERAMIC WITH KOVAR OR EQUIVALENT.
3. LID MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED, ALLOY SEAL.
4. TOLERANCES NON CUMULATIVE.
5. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
6. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
7. THERMAL RESISTANCE: Θ Ja = .050°C/mW, Θ Jc = .010°C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

PACKAGE INFORMATION

I PACKAGE



NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED.
2. BODY MATERIAL: CERAMIC WITH KOVAR OR EQUIVALENT. TOP RING GOLD PLATED.
3. LID MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED, ALLOY SEAL.
4. TOLERANCES NON CUMULATIVE.
5. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
6. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
7. THERMAL RESISTANCE: Θ Ja = .062°C/mW, Θ Jc = .018°C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

QUALIFICATION AND SCREENING PROGRAM FOR MOS DEVICES

The Signetics SURE*/883 Program consists of a combination of 100 percent and statistical sample tests designed to assure specified performance, continuing uniformity, and long term reliability of Signetics products. These tests are made regularly at no extra cost to the user and are performed in addition to the 40 quality assurance inspections and tests to which every circuit is subjected before final seal. The tests, tabulated below the specifier's convenience, are performed in accordance with the following conditions, sequence, and schedules on equipment calibrated to meet all requirements of MIL-Q-9858A and MIL-C-45662A.

Every circuit of every lot is processed to the environmental screens shown in Table I. These screens are performed in production and include 100% final production electrical test. Any unit failing either the environmental screens or the final production electrical tests is rejected and removed from the lot.

After completion of Table I tests, each manufacturing lot is sampled and tested by Quality Assurance for conformance to the requirements of Table II. The unsampled portion of the lot is held pending acceptance of the lot sample. Detailed test limits and conditions applicable to test group are shown in the Electrical Characteristics table of the individual part type data sheets.

Tables III, and IV provide a complete process qualification and verification program. These tests are performed once in every 90 day manufacturing period, on representative devices from each standard production die process family and on each production package family. The representative circuits and packages selected are changed routinely, and the tests performed monitor and qualify all structurally similar devices produced by the same process and production during that period.

All of the applicable Electrical Parameters on the data sheets are performed at pretest on the Table IV samples. These tests are performed on representative circuit types from every die process family type in manufacturing during this period.

Table III consists of the Package oriented qualification environmental stress tests of MIL-STD-883, Groups B and C. Representative samples from each package product family type are monitored and qualified every 90 day period by these tests. A common device is used as the die type for these package and assembly qualification tests.

Table IV consists of the die process oriented qualification electrical stress or operational tests at high temperature. Representative devices from each die process are monitored and qualified every 90 day period by these tests. The package type is randomly selected as applicable.

TABLE I – 100% PRODUCTION SCREEN TESTS

TEST	CONDITIONS
Preseal Visual	High Power Low Power Liquid to Liquid
Thermal Shock	5 Cycles; 60 Seconds at 0°C, 60 Seconds at 100°C, Transfer Time 5 Seconds. Note 1.
Centrifuge	Y_1 Axis; 30,000 G Minimum 1 Minute. Note 1.
Hermeticity	Gross Leak Test (Bubble Test) Note 1.
Production Electrical Tests	AC and DC, $T_A = 25°C$

NOTE:
1. Not applicable to solid molded packaged devices.

TABLE II – SIGNETICS ACCEPTANCE TESTS (See Notes 2 and 3)

TEST GROUP	CONDITIONS	AQL	MIL-STD-105 INSPECTION LEVEL
Visual and Mechanical Inspection	MIL-STD-883 Method 2009	1.0%	II
DC Parameters	$T_A = +25°C$	1.0%	II
DC Parameters	$T_A = 70°C$	1.0%	II
DC Parameters	$T_A = 0°C$	1.0%	II
AC Parameters	$T_A = +25°C$	1.0%	II

*Systematic Uniformity and Reliability Evaluation

NOTES:
2. All test equipment calibrated to meet requirements of MIL-Q-9858A and MIL-C-45662A.
3. Detailed tests, conditions, and limits applicable to each test group are given in the Signetics data sheet ELECTRICAL CHARACTERISTICS table.

TABLE III – MIL-STD-833 GROUPS B AND C ENVIRONMENTAL TESTS

TEST DESCRIPTION	MIL-STD-833 METHOD	CONDITIONS	LTPD
Physical Dimensions	2008	Test Condition A	15
Marking Permanency	2008	Test Condition B, Para. 3.2.1	4 devices/no failures
Visual and Mechanical	2008	Test Condition B	1 device/no failures
Bond Strength	2011	Test Condition D, Para. 3.7	15
Solderability	2003	Solder Temperature 260°C ±10°C	15
Lead Fatigue	2004	Test Condition B_2	15
Hermeticity	1014	Note 4	
a. Fine		Test Condition A or B	
b. Gross		Test Condition C	
Pre-Test Electrical Parameters		Table V as Applicable	
Thermal Shock	1011	15 Cycles. Test Condition C, +150°C to -65°C	15
Temperature Cycle	1010	10 Cycles. Test Condition C, +150°C to -65°C	
Moisture Resistance	1004	Omit Vibration and Initial Conditioning	
End Point Electrical Parameters		Table V as Applicable	
FAILURE CRITERIA		Refer to Table V	
Pre-Test Electrical Parameters		Table V as Applicable	
Mechanical Shock	2002	Test Condition B	15
Vibration Variable Frequency	2007	Test Condition A	
Constant Acceleration	2001		
End Point Electrical Parameters		Table V as Applicable	
FAILURE CRITERIA		Refer to Table V	
Salt Atmosphere	1009	Test Condition A. Omit Initial Conditioning.	
Pre-Test Electical Parameters		Table V as Applicable	
High Temperature Storage	1008	T_A = +150°C, t = 1000 hours	15
End Point Electrical Parameters		Table V as Applicable	
FAILURE CRITERIA		Refer to Table V	

NOTE:
4. The hermeticity tests are not employed for solid molded packages.

TABLE IV – HIGH TEMPERATURE OPERATING LIFE TESTS

TEST DESCRIPTION	CONDITIONS	LTPD
Pre-Test Electrical Parameters	Refer to Table V	
Operating Life	$T_A = 70^\circ C$; t = 1000 hours	10
Shift Registers	Logic 1's Clocked Through Register	
ROMs, RAMs	Addresses Being Counted Through in a Binary Fashion	

TABLE V – SIGNETICS FAILURE CRITERIA

SHIFT REGISTERS

TEST	INPUT LEAKAGE	I_{DD}	t_{ACCESS}	"1" LEVELS	"0" LEVELS
Delta Limit	5X or 100nA whichever is greater	20%	Data Sheet Limits	20%	20%

ROMs

TEST	INPUT LEAKAGE	CLOCK LEAKAGE	I_{DD}	"1"LEVELS	"0" LEVELS
Delta Limit	5X or 100nA whichever is greater	5X or 100nA whichever is greater	20%	20%	20%

RAMs

TEST	INPUT LEAKAGE	t_{ACCESS}	t_{REFESH}*	"1" LEVELS	"0" LEVELS
Data Limit	5X or 100nA whichever is greater	Data Sheet Limit	Data Sheet Limits	20%	20%

*For dynamic memories.

COMPANY _____

ADDRESS _____

CITY _____ STATE _____ ZIP _____

TEL. _____

AUTHORIZED SIGNATURE _____

BASIC PRODUCT TYPE _____

DATE _____

CUSTOMER PRINT OR I.D. NUMBER _____

PURCHASE ORDER NUMBER _____

_____

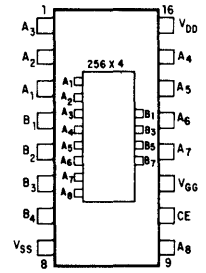
BASIC INFORMATION

- DEVICE TYPE N24 ☐ ☐
- NUMBER OF CHIP SELECTS ☐ 1 ☐ 3
- CHIP SELECT CODE ☐ CE_3 ☐ CE_2 ☐ CE_1
- OUTPUT DEVICE ☐ MOS RESISTOR
  ☐ TTL (Bare Drain)
- ORGANIZATION ☐ 8 X 256 ☐ 4 X 512
  ☐ 8 X 128 ☐ 4 X 256
- PACKAGE ☐ 16 PIN ☐ 24 PIN
- LOGIC "1" MORE NEGATIVE VOLTAGE
  LOGIC "2" MORE POSITIVE VOLTAGE
- INSTRUCTIONS FOR COMPLETING TRUTH TABLE
  (Required only if computer punch cards are not used)
  FOR 8 X 256 USE COLUMN I ADDRESS– OUTPUTS B1–B8
  FOR 8 X 128 USE COLUMN I ADDRESS– OUTPUTS B1–B8
  FOR 4 X 256 USE COLUMN I ADDRESS WORDS 0–127, OUTPUTS B1–B4; COLUMN II ADDRESS WORDS 128–255, OUTPUTS B5–B8
  FOR 4 X 512 USE COLUMN I ADDRESS WORDS 0–255, OUTPUTS B1–B4; COLUMN III ADDRESS WORDS 256–511, OUTPUTS B5–B8

ORGANIZATION

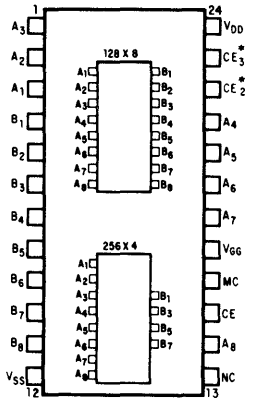
The Signetics 2400 Series is a family of read-only memories. The 2410, 2420, and 2430 Series are offered with the following organizations.

2410



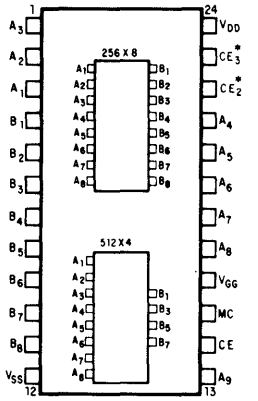
2410 Series- 1024 bit read-only memory organized as 256 words of 4 bits in a 16 pin dip.

2420



2420 Series- 1024 bit read-only memory organized a 128 words by 8 bits or 256 words by 4 bits If the 256 words by 4 organization is specified outputs will appear on pins 4, 6, 8, and 10.

2430



2430 Series- 2048 bit read-only memory organized as 256 words by 8 bits or 512 words by 4 bits. If the 512 word by 4 organization is specified outputs will appear on pins 4, 6, 8, and 10.

ROM SELECTION CHART

TYPE	ORGANIZATION	PACKAGE	OUTPUTS	CHIP SELECT CONTROLS
N2410I	256 x 4	16-Pin Ceramic DIP	MOS Pull-up	1
N2411I	256 x 4	16-Pin Ceramic DIP	Bare Drain	1
N2420Y	128 x 8, 256 x 4	24-Pin Ceramic DIP	MOS Pull-up	1
N2421Y	128 x 8, 256 x 4	24-Pin Ceramic DIP	Bare Drain	1
N2425Y	128 x 8, 256 x 4	24-Pin Ceramic DIP	MOS Pull-up	3 (binary coded)*
N2426Y	128 x 8, 256 x 4	24-Pin Ceramic DIP	Bare Drain	3 (binary coded)*
N2430Y	512 x 4, 256 x 8	24-Pin Ceramic DIP	MOS Pull-up	1
N2431Y	512 x 4, 256 x 8	24-Pin Ceramic DIP	Bare Drain	1
N2435Y	512 x 4, 256 x 8	24-Pin Ceramic DIP	MOS Pull-up	3 (binary coded)*
N2436Y	512 x 4, 256 x 8	24-Pin Ceramic DIP	Bare Drain	3 (binary coded)*

*Mask Programmable

CIRCUIT OPTION

The following circuit options are available for the user's particular needs:

OUTPUT BUFFER

For all series the user has the option of MOS or TTL outputs. This must be specified by the user.

- MOS output- an output having an MOS resistor connected to V_{DD}. This allows interfacing with other MOS devices.
- TTL output- an output having no MOS resistor connected to V_{DD}. Commonly called a "bare drain" output; this allows direct interfacing with TTL circuits and external "wired AND" capability.

CHIP SELECT

- "Single" ROM- one which has only one chip select. A logical "0" on the chip select line places all outputs in the "1" state (or open-circuited in the case of a "TTL" output).
- "Coded" ROM- one which has a three digit binary code chip select. This allows paralleling up to eight devices without external chip select logic thereby allowing the user to save the cost of extra packages and PC board space.
- 2410 Series may only be ordered as a "single" ROM (one chip select).
- 2420 and 2430 Series may be ordered as "single" or "coded" ROM's (one chip select or three chip selects).

DEFINITIONS

Logic definition:
All logic is assumed negative
"0" is the more positive voltage
"1" is the more negative voltage

Input definition:
A1 is the least significant input address
A8 is the most significant input address

INPUT FORMAT

Programming information for Signetics' 2400 Series should be transmitted to Signetics in the form of computer punched cards accompanied by information on the various circuit options desired. Upon receipt of each deck and the circuit option desired for that deck a computer generated truth table will be made and a copy of this truth table returned to the customer. This minimizes the possibility of error and allows the best possible delivery (normally 4 weeks after receipt of card deck).

Upon receipt of the computer generated truth table check it carefully and if any errors are discovered notify Signetics immediately.

The Signetics' 2400 Series Read-Only Memory can be programmed so that for any binary input A1 through A8 the outputs B1 through B8 are uniquely determined. Each deck of cards sent to Signetics must contain a card describing the options desired (card 1), the unique outputs for each word in memory (cards 2 through 129 or 257, depending on organization), and cards specifying the address to which the computer generated truth table should be sent. Cards should be punched according to the format on the following pages.

If it is not feasible to use computer punched cards, the user should describe the circuit option desired and complete the truth table. Upon receipt of pages Signetics will punch the computer cards and return a copy of the computer generated truth table, (the user can realize a substantial savings associated with the coding charge by using computer cards).

CARD 1

COLUMN	DATA
1-8	Starting at column 1- punch "coded" or "single"
9-11*	If "coded", punch the binary code chip select (i.e., 101), if "single" leave blank
12	Leave blank
13-17	Punch the ROM organization desired (i.e., 8 X 256, 4 X 512), etc.
18	Leave blank
19-21	Punch MOS for an MOS output. Punch TTL for a TTL output (bare drain)
22-27	Leave blank (For CM No.)
28-33	Punch the basic device type desired (i.e., N2410I, N2420Y), etc.
34-80	Comments punched here will appear as the title on the truth table. This should include customer part identification

*CE_3, CE_2 and CE_1 respectively

CARD 2 THROUGH 129 (8 X 128 Organization)
2 THROUGH 257 (8 X 256 Organization)

Each card specifies the output of one 8-bit word in columns 1 through 8. The decimal equivalent of the binary coded input address for that word is punched in columns 78, 79, and 80.

COLUMN	DATA
1-8	Punch outputs B1 through B8 in columns one through eight respectively
9-77	Leave blank
78-80	Punch decimal equivalent of binary coded input address which corresponds to the outputs punched in Columns 1-8

Column 78- Hundreds Digit
Column 79- Tens Digit
Column 80- Units Digit

CARDS 2 THROUGH 257
(4 X 512 Organization only)

Each card specifies the output of two 4-bit words in columns 1 through 8. The decimal equivalent of the binary coded input address is punched in columns 78. 79, and 80.

COLUMN	DATA
1-4	Punch output for words 0-255
5-8	Punch output for words 256-511
9-77	Leave blank
78-8	Punch decimal equivalent of binary coded input address of the word corresponding to the outputs punched in Columns 1-4

Column 78- Hundreds Digit
Column 79- Tens Digit
Column 80- Units Digit

CARDS 2 THROUGH 129
(4 X 256 Organization only)

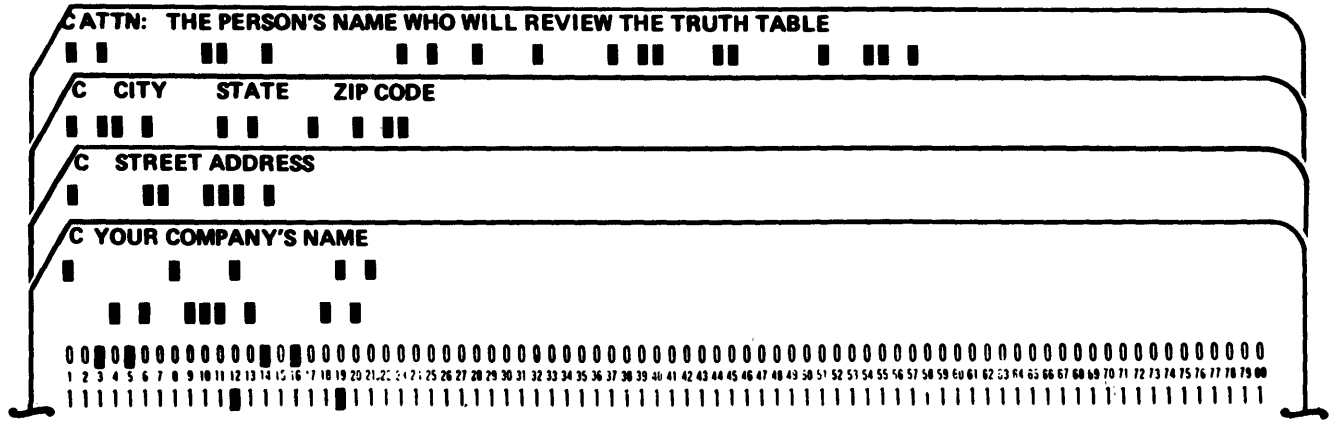
Each card specifies the output of two 4-bit words in columns 1 through 8. The decimal equivalent of the binary coded input address is punched in columns 78, 79, and 80.

COLUMN	DATA
1-4	Punch output for words 0-127
5-8	Punch output for words 128-255
9-77	Leave blank
78-80	Punch decimal equivalent of binary coded input address corresponding to the outputs punched in Columns 1-4

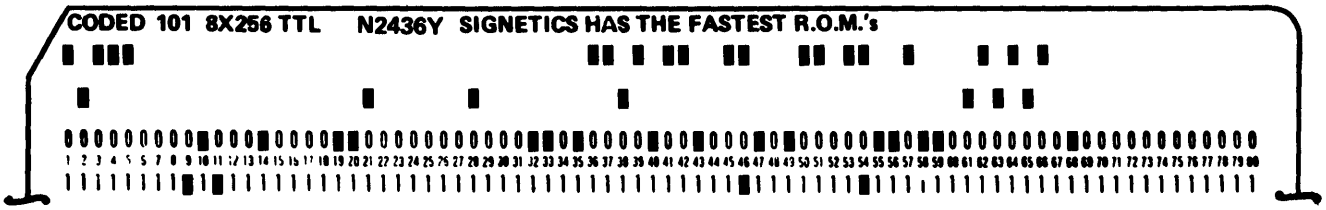
Column 78-Hundreds Digit
Column 79- Tens Digit
Column 80- Units Digit

EXAMPLE CARDS:

ADDRESS CARDS

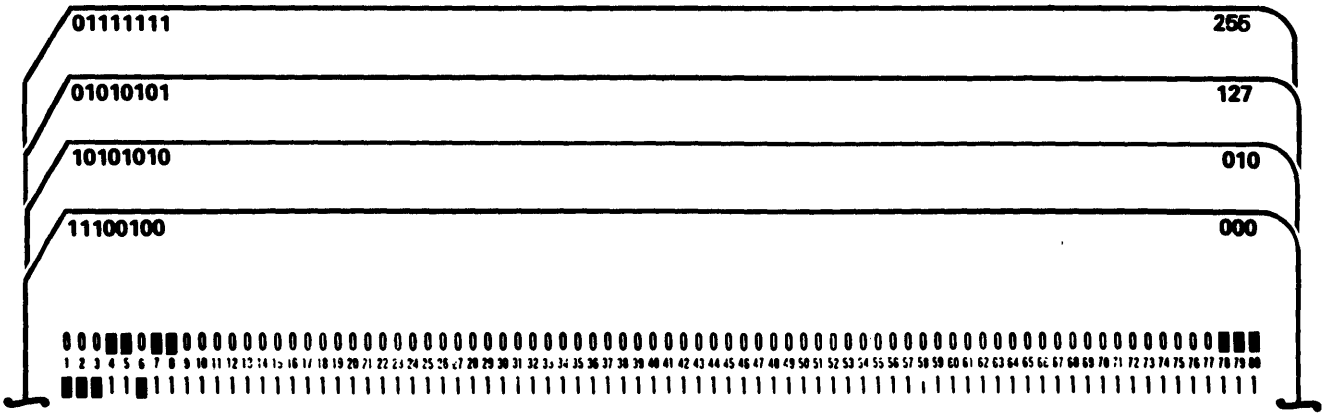


CARD 1



The above specifies a "coded" ROM with the binary coded chip select "101" organized 8 X 256 with TTL outputs (bare drain). The basic device type is a N2436Y ("Y" indicates a 24-pin ceramic DIP. N indicates temperature range: -25°C– +70°C).

CARDS 2-129 AND CARDS 2-257



- Outputs B1 through B8 are in columns 1 through 8 respectively
- Decimal equivalent of binary coded input address is in columns 78, 79, and 80
- For 8 X 128 and 8 X 256 organizations- outputs are B1 through B8 respectively
- For 4 X 512 organization:

  Data card 0 — Word 000 outputs B1 through B4 respectively
  Word 256 outputs B5 through B8 respectively

  Data card 10 — Word 010 outputs B1 through B4 respectively
  Word 266 outputs B5 through B8 respectively

- For 4 X 256 Organization:

  Data card 0 — Word 000 outputs B1 through B4 respectively
  Word 128 outputs B5 through B8 respectively

  Data card 10 — Word 010 outputs B1 through B4 respectively
  Word 138 outputs B5 through B8 respectively

ADDRESS INPUT GATE								DECIMAL ADDRESS			OUTPUT DATA								USER'S CHAR-ACTER
A8	A7	A6	A5	A4	A3	A2	A1	I	II	III	B1	B2	B3	B4	B5	B6	B7	B8	
0	0	0	0	0	0	0	0	000	128	256									
0	0	0	0	0	0	0	1	001	129	257									
0	0	0	0	0	0	1	0	002	130	258									
0	0	0	0	0	0	1	1	003	131	259									
0	0	0	0	0	1	0	0	004	132	260									
0	0	0	0	0	1	0	1	005	133	261									
0	0	0	0	0	1	1	0	006	134	262									
0	0	0	0	0	1	1	1	007	135	263									
0	0	0	0	1	0	0	0	008	136	264									
0	0	0	0	1	0	0	1	009	137	265									
0	0	0	0	1	0	1	0	010	138	266									
0	0	0	0	1	0	1	1	011	139	267									
0	0	0	0	1	1	0	0	012	140	268									
0	0	0	0	1	1	0	1	013	141	269									
0	0	0	0	1	1	1	0	014	142	270									
0	0	0	0	1	1	1	1	015	143	271									
0	0	0	1	0	0	0	0	016	144	272									
0	0	0	1	0	0	0	1	017	145	273									
0	0	0	1	0	0	1	0	018	146	274									
0	0	0	1	0	0	1	1	019	147	275									
0	0	0	1	0	1	0	0	020	148	276									
0	0	0	1	0	1	0	1	021	149	277									
0	0	0	1	0	1	1	0	022	150	278									
0	0	0	1	0	1	1	1	023	151	279									
0	0	0	1	1	0	0	0	024	152	280									
0	0	0	1	1	0	0	1	025	153	281									
0	0	0	1	1	0	1	0	026	154	282									
0	0	0	1	1	0	1	1	027	155	283									
0	0	0	1	1	1	0	0	028	156	284									
0	0	0	1	1	1	0	1	029	157	285									
0	0	0	1	1	1	1	0	030	158	286									
0	0	0	1	1	1	1	1	031	159	287									
0	0	1	0	0	0	0	0	032	160	288									
0	0	1	0	0	0	0	1	033	161	289									
0	0	1	0	0	0	1	0	034	162	290									
0	0	1	0	0	0	1	1	035	163	291									
0	0	1	0	0	1	0	0	036	164	292									

ADDRESS INPUT GATE								DECIMAL ADDRESS			OUTPUT DATA								USER'S CHAR-ACTER
A8	A7	A6	A5	A4	A3	A2	A1	I	II	III	B1	B2	B3	B4	B5	B6	B7	B8	
0	0	1	0	0	1	0	1	037	165	293									
0	0	1	0	0	1	1	0	038	166	294									
0	0	1	0	0	1	1	1	039	167	295									
0	0	1	0	1	0	0	0	040	168	296									
0	0	1	0	1	0	0	1	041	169	297									
0	0	1	0	1	0	1	0	042	170	298									
0	0	1	0	1	0	1	1	043	171	299									
0	0	1	0	1	1	0	0	044	172	300									
0	0	1	0	1	1	0	1	045	173	301									
0	0	1	0	1	1	1	0	046	174	302									
0	0	1	0	1	1	1	1	047	175	303									
0	0	1	1	0	0	0	0	048	176	304									
0	0	1	1	0	0	0	1	049	177	305									
0	0	1	1	0	0	1	0	050	178	306									
0	0	1	1	0	0	1	1	051	179	307									
0	0	1	1	0	1	0	0	052	180	308									
0	0	1	1	0	1	0	1	053	181	309									
0	0	1	1	0	1	1	0	054	182	310									
0	0	1	1	0	1	1	1	055	183	311									
0	0	1	1	1	0	0	0	056	184	312									
0	0	1	1	1	0	0	1	057	185	313									
0	0	1	1	1	0	1	0	058	186	314									
0	0	1	1	1	0	1	1	059	187	315									
0	0	1	1	1	1	0	0	060	188	316									
0	0	1	1	1	1	0	1	061	189	317									
0	0	1	1	1	1	1	0	062	190	318									
0	0	1	1	1	1	1	1	063	191	319									
0	1	0	0	0	0	0	0	064	192	320									
0	1	0	0	0	0	0	1	065	193	321									
0	1	0	0	0	0	1	0	066	194	322									
0	1	0	0	0	0	1	1	067	195	323									
0	1	0	0	0	1	0	0	068	196	324									
0	1	0	0	0	1	0	1	069	197	325									
0	1	0	0	0	1	1	0	070	198	326									
0	1	0	0	0	1	1	1	071	199	327									
0	1	0	0	1	0	0	0	072	200	328									
0	1	0	0	1	0	0	1	073	201	329									

ADDRESS INPUT GATE								DECIMAL ADDRESS			OUTPUT DATA								USER'S CHAR-ACTER
A8	A7	A6	A5	A4	A3	A2	A1	I	II	III	B1	B2	B3	B4	B5	B6	B7	B8	
0	1	0	0	1	0	1	0	074	202	330									
0	1	0	0	1	0	1	1	075	203	331									
0	1	0	0	1	1	0	0	076	204	332									
0	1	0	0	1	1	0	1	077	205	333									
0	1	0	0	1	1	1	0	078	206	334									
0	1	0	0	1	1	1	1	079	207	335									
0	1	0	1	0	0	0	0	080	208	336									
0	1	0	1	0	0	0	1	081	209	337									
0	1	0	1	0	0	1	0	082	210	338									
0	1	0	1	0	0	1	1	083	211	339									
0	1	0	1	0	1	0	0	084	212	340									
0	1	0	1	0	1	0	1	085	213	341									
0	1	0	1	0	1	1	0	086	214	342									
0	1	0	1	0	1	1	1	087	215	343									
0	1	0	1	1	0	0	0	088	216	344									
0	1	0	1	1	0	0	1	089	217	345									
0	1	0	1	1	0	1	0	090	218	346									
0	1	0	1	1	0	1	1	091	219	347									
0	1	0	1	1	1	0	0	092	220	348									
0	1	0	1	1	1	0	1	093	221	349									
0	1	0	1	1	1	1	0	094	222	350									
0	1	0	1	1	1	1	1	095	223	351									
0	1	1	0	0	0	0	0	096	224	352									
0	1	1	0	0	0	0	1	097	225	353									
0	1	1	0	0	0	1	0	098	226	354									
0	1	1	0	0	0	1	1	099	227	355									
0	1	1	0	0	1	0	0	100	228	356									
0	1	1	0	0	1	0	1	101	229	357									
0	1	1	0	0	1	1	0	102	230	358									
0	1	1	0	0	1	1	1	103	231	359									
0	1	1	0	1	0	0	0	104	232	360									
0	1	1	0	1	0	0	1	105	233	361									
0	1	1	0	1	0	1	0	106	234	362									
0	1	1	0	1	0	1	1	107	235	363									
0	1	1	0	1	1	0	0	108	236	364									
0	1	1	0	1	1	0	1	109	237	365									
0	1	1	0	1	1	1	0	110	238	366									

ADDRESS INPUT GATE								DECIMAL ADDRESS			OUTPUT DATA								USER'S CHAR-ACTER
A8	A7	A6	A5	A4	A3	A2	A1	I	II	III	B1	B2	B3	B4	B5	B6	B7	B8	
0	1	1	0	1	1	1	1	111	239	367									
0	1	1	1	0	0	0	0	112	240	368									
0	1	1	1	0	0	0	1	113	241	369									
0	1	1	1	0	0	1	0	114	242	370									
0	1	1	1	0	0	1	1	115	243	371									
0	1	1	1	0	1	0	0	116	244	372									
0	1	1	1	0	1	0	1	117	245	373									
0	1	1	1	0	1	1	0	118	246	374									
0	1	1	1	0	1	1	1	119	247	375									
0	1	1	1	1	0	0	0	120	248	376									
0	1	1	1	1	0	0	1	121	249	377									
0	1	1	1	1	0	1	0	122	250	378									
0	1	1	1	1	0	1	1	123	251	379									
0	1	1	1	1	1	0	0	124	252	380									
0	1	1	1	1	1	0	1	125	253	381									
0	1	1	1	1	1	1	0	126	254	382									
0	1	1	1	1	1	1	1	127	255	383									
1	0	0	0	0	0	0	0	128		384									
1	0	0	0	0	0	0	1	129		385									
1	0	0	0	0	0	1	0	130		386									
1	0	0	0	0	0	1	1	131		387									
1	0	0	0	0	1	0	0	132		388									
1	0	0	0	0	1	0	1	133		389									
1	0	0	0	0	1	1	0	134		390									
1	0	0	0	0	1	1	1	135		391									
1	0	0	0	1	0	0	0	136		392									
1	0	0	0	1	0	0	1	137		393									
1	0	0	0	1	0	1	0	138		394									
1	0	0	0	1	0	1	1	139		395									
1	0	0	0	1	1	0	0	140		396									
1	0	0	0	1	1	0	1	141		397									
1	0	0	0	1	1	1	0	142		398									
1	0	0	0	1	1	1	1	143		399									
1	0	0	1	0	0	0	0	144		400									
1	0	0	1	0	0	0	1	145		401									
1	0	0	1	0	0	1	0	146		402									
1	0	0	1	0	0	1	1	147		403									

ADDRESS INPUT GATE								DECIMAL ADDRESS			OUTPUT DATA								USER'S CHAR-ACTER
A8	A7	A6	A5	A4	A3	A2	A1	I	II	III	B1	B2	B3	B4	B5	B6	B7	B8	
1	0	0	1	0	1	0	0	148		404									
1	0	0	1	0	1	0	1	149		405									
1	0	0	1	0	1	1	0	150		406									
1	0	0	1	0	1	1	1	151		407									
1	0	0	1	1	0	0	0	152		408									
1	0	0	1	1	0	0	1	153		409									
1	0	0	1	1	0	1	0	154		410									
1	0	0	1	1	0	1	1	155		411									
1	0	0	1	1	1	0	0	156		412									
1	0	0	1	1	1	0	1	157		413									
1	0	0	1	1	1	1	0	158		414									
1	0	0	1	1	1	1	1	159		415									
1	0	1	0	0	0	0	0	160		416									
1	0	1	0	0	0	0	1	161		417									
1	0	1	0	0	0	1	0	162		418									
1	0	1	0	0	0	1	1	163		419									
1	0	1	0	0	1	0	0	164		420									
1	0	1	0	0	1	0	1	165		421									
1	0	1	0	0	1	1	0	166		422									
1	0	1	0	0	1	1	1	167		423									
1	0	1	0	1	0	0	0	168		424									
1	0	1	0	1	0	0	1	169		425									
1	0	1	0	1	0	1	0	170		426									
1	0	1	0	1	0	1	1	171		427									
1	0	1	0	1	1	0	0	172		428									
1	0	1	0	1	1	0	1	173		429									
1	0	1	0	1	1	1	0	174		430									
1	0	1	1	1	1	1	1	175		431									
1	0	1	1	0	0	0	0	176		432									
1	0	1	1	0	0	0	1	177		433									
1	0	1	1	0	0	1	0	178		434									
1	0	1	1	0	0	1	1	179		435									
1	0	1	1	0	1	0	0	180		436									
1	0	1	1	0	1	0	1	181		437									
1	0	1	1	0	1	1	0	182		438									
1	0	1	1	0	1	1	1	183		439									
1	0	1	1	1	0	0	0	184		440									

ADDRESS INPUT GATE								DECIMAL ADDRESS			OUTPUT DATA								USER'S CHAR-ACTER
A8	A7	A6	A5	A4	A3	A2	A1	I	II	III	B1	B2	B3	B4	B5	B6	B7	B8	
1	0	1	1	1	0	0	1	185		441									
1	0	1	1	1	0	1	0	186		442									
1	0	1	1	1	0	1	1	187		443									
1	0	1	1	1	1	0	0	188		444									
1	0	1	1	1	1	0	1	189		445									
1	0	1	1	1	1	1	0	190		446									
1	0	1	1	1	1	1	1	191		447									
1	1	0	0	0	0	0	0	192		448									
1	1	0	0	0	0	0	1	193		449									
1	1	0	0	0	0	1	0	194		450									
1	1	0	0	0	0	1	1	195		451									
1	1	0	0	0	1	0	0	196		452									
1	1	0	0	0	1	0	1	197		453									
1	1	0	0	0	1	1	0	198		454									
1	1	0	0	0	1	1	1	199		455									
1	1	0	0	1	0	0	0	200		456									
1	1	0	0	1	0	0	1	201		457									
1	1	0	0	1	0	1	0	202		458									
1	1	0	0	1	0	1	1	203		459									
1	1	0	0	1	1	0	0	204		460									
1	1	0	0	1	1	0	1	205		461									
1	1	0	0	1	1	1	0	206		462									
1	1	0	0	1	1	1	1	207		463									
1	1	0	1	0	0	0	0	208		464									
1	1	0	1	0	0	0	1	209		465									
1	1	0	1	0	0	1	0	210		466									
1	1	0	1	0	0	1	1	211		467									
1	1	0	1	0	1	0	0	212		468									
1	1	0	1	0	1	0	1	213		469									
1	1	0	1	0	1	1	0	214		470									
1	1	0	1	0	1	1	1	215		471									
1	1	0	1	1	0	0	0	216		472									
1	1	0	1	1	0	0	1	217		473									
1	1	0	1	1	0	1	0	218		474									
1	1	0	1	1	0	1	1	219		475									
1	1	0	1	1	1	0	0	220		476									
1	1	0	1	1	1	0	1	221		477									

ADDRESS INPUT GATE								DECIMAL ADDRESS			OUTPUT DATA								USER'S CHAR-ACTER
A8	A7	A6	A5	A4	A3	A2	A1	I	II	III	B1	B2	B3	B4	B5	B6	B7	B8	
1	1	0	1	1	1	1	0	222		478									
1	1	0	1	1	1	1	1	223		479									
1	1	1	0	0	0	0	0	224		480									
1	1	1	0	0	0	0	1	225		481									
1	1	1	0	0	0	1	0	226		482									
1	1	1	0	0	0	1	1	227		483									
1	1	1	0	0	1	0	0	228		484									
1	1	1	0	0	1	0	1	229		485									
1	1	1	0	0	1	1	0	230		486									
1	1	1	0	0	1	1	1	231		487									
1	1	1	0	1	0	0	0	232		488									
1	1	1	0	1	0	0	1	233		489									
1	1	1	0	1	0	1	0	234		490									
1	1	1	0	1	0	1	1	235		491									
1	1	1	0	1	1	0	0	236		492									
1	1	1	0	1	1	0	1	237		493									
1	1	1	0	1	1	1	0	238		494									
1	1	1	0	1	1	1	1	239		495									
1	1	1	1	0	0	0	0	240		496									
1	1	1	1	0	0	0	1	241		497									
1	1	1	1	0	0	1	0	242		498									
1	1	1	1	0	0	1	1	243		499									
1	1	1	1	0	1	0	0	244		500									
1	1	1	1	0	1	0	1	245		501									
1	1	1	1	0	1	1	0	246		502									
1	1	1	1	0	1	1	1	247		503									
1	1	1	1	1	0	0	0	248		504									
1	1	1	1	1	0	0	1	249		505									
1	1	1	1	1	0	1	0	250		506									
1	1	1	1	1	0	1	1	251		507									
1	1	1	1	1	1	0	0	252		508									
1	1	1	1	1	1	0	1	253		509									
1	1	1	1	1	1	1	0	254		510									
1	1	1	1	1	1	1	1	255		511									

COMPANY_____

ADDRESS_____

CITY_____STATE_____ZIP____

TELEPHONE_____

AUTHORIZED SIGNATURE_____

DATE_____

CUSTOMER PRINT OR ID NO._____

PURCHASE ORDER NUMBER_____

DEVICE TYPE_____2413_____2415____

CUSTOM PATTERN NUMBER (TO BE ENTERED BY SIGNETICS)_____

INTRODUCTION

The Signetics 2513 and 2514 are high speed silicon gate MOS 2560-Bit read-only memories whose organizations are specially suited for 64 X 8 X 5 raster scan character generation.

MAJOR FEATURES OF THE 2513 AND 2514

- ACCESS TIME 450ns TYPICALLY
- STATIC OPERATION
- TTL/DTL COMPATIBLE
- TRI-STATE OUTPUTS (HIGH-LOW-DISCONNECTED) FOR POWERFUL BUSSING CAPABILITY
- +5, -5, -12V POWER SUPPLIES
- 24-PIN SIGNETICS SILICONE DIP
- SIGNETICS SILICON GATE PROCESS TECHNOLOGY FOR PERFORMANCE AND RELIABILITY

ORGANIZATION AS CHARACTER GENERATOR

A six-bit binary address (A_4 through A_9) selects 1-of-64 matrix characters arranged 5 dots horizontally and 8 dots vertically. A three bit binary address code (A_1 through A_3) selects 1 of 8 rows. Five outputs display a complete row of the character matrix. See Figure 1. The devices may also be used in pairs to provide 9 X 7 and 10 X 8 vertical scan formats.

CHARACTER FORMAT

ROW ADDRESS

ROW ADDRESS

A_3	A_2	A_1
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

O_5	O_4	O_3	O_2	O_1
0	0	0	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	0	0
0	1	1	1	0
0	0	0	0	1
1	0	0	0	1
0	1	1	1	0

EXAMPLE 'S'

FIGURE 1

CHARACTER ADDRESS

COLUMN ADDRESS

	A_4	A_5	A_6	A_7	A_8	A_9
ASCII CHARACTER	1	1	0	0	1	0

FIGURE 2

ORGANIZATION AS READ-ONLY MEMORY

For a straight 512 X 5 read-only memory, the five outputs will display any one of 512 5-bit stored words corresponding to a 9-bit address applied to A_1 through A_9.

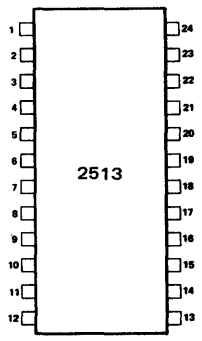
DEVICE TYPE SELECTION

The only difference between the 2513 and 2514 consists of a separate V_{DD} terminal for the output device on the 2514. This feature allows flexibility in power dissipation and output "0" voltage level. Otherwise the 2513 and 2514 may be used as either straight ROMs or character generators.

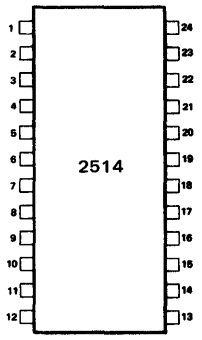
STANDARD PATTERN

A standard ASCII character font is available for the 2513. This device (2513NX/CM2140) may be used for ASCII character generation or for device evaluation.

PIN CONFIGURATION (Top View)



1. V_{GG}
2. NC
3. NC
4. Out 1
5. Out 2
6. Out 3
7. Out 4
8. Out 5
9. NC
10. NC
11. Chip Enable
12. V_{DD}
13. NC
14. Address 1
15. Address 2
16. Address 3
17. Address 4
18. Address 5
19. Address 6
20. Address 7
21. Address 8
22. Address 9
23. NC
24. V_{CC}



1. V_{GG}
2. NC
3. NC
4. Out 1
5. Out 2
6. Out 3
7. Out 4
8. Out 5
9. NC
10. Chip Enable
11. V_{DD2}
12. V_{DD}
13. NC
14. Address 1
15. Address 2
16. Address 3
17. Address 4
18. Address 5
19. Address 6
20. Address 7
21. Address 8
22. Address 9
23. NC
24. V_{CC}

CUSTOM DEVICES

For unique custom memory patterns, this form should be used to transmit coding instructions. The nomenclature for a custom device will consist of the basic product type followed by a unique CM number assigned by Signetics. For example, "2513NX/CM2141".

- **PROGRAMMING WITH PUNCHED CARDS**
  For maximum accuracy and minimum cost and turn-around time, the truth table should be transmitted to Signetics in the form of punched cards according to the format indicated on the following pages.
- **PROGRAMMING WITH WRITTEN TRUTH TABLE**
  When punched data cards cannot be supplied, the truth table may be transmitted in written form using the attached blank truth table.

VERIFICATION

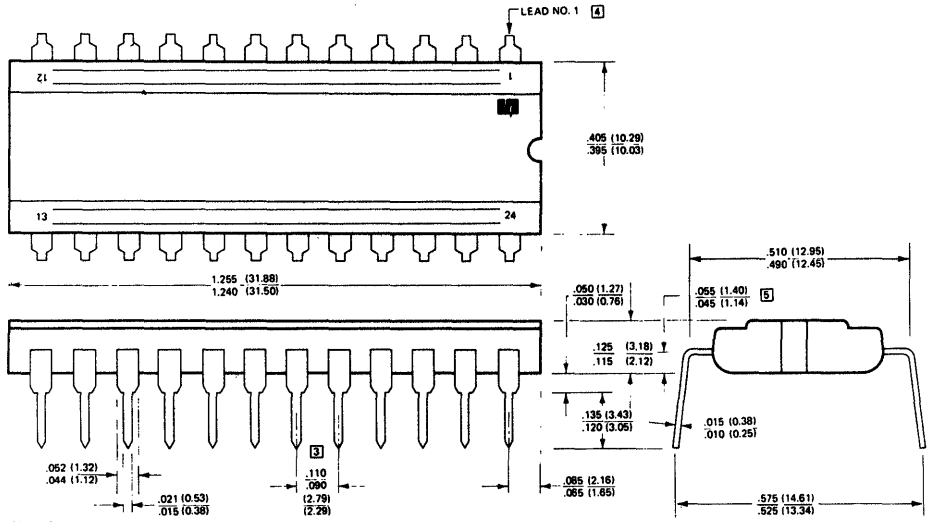
Upon receipt of either punched card or written truth table information, Signetics will prepare a computer tabulation of the instructions and return to the address indicated. If errors are detected, they should be transmitted to Signetics as quickly as possible.

LOGIC CONVENTION

Logic "1"s or blackened squares in the truth table will result in "high" output from the indicated output terminal (i.e. 3.2V minimum). Similarly, a "1" address input level is interpreted as 3.2V minimum.

PACKAGE INFORMATION

NX PACKAGE



NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: SILICONE MOLDED.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: Θ Ja = .12 C/mW, Θ Jc = .05 C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

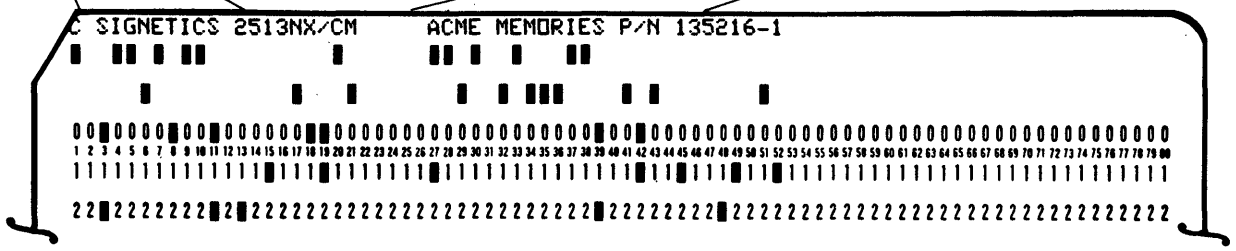
IDENTIFICATION CARDS

INDICATES "COMMENT" CARD

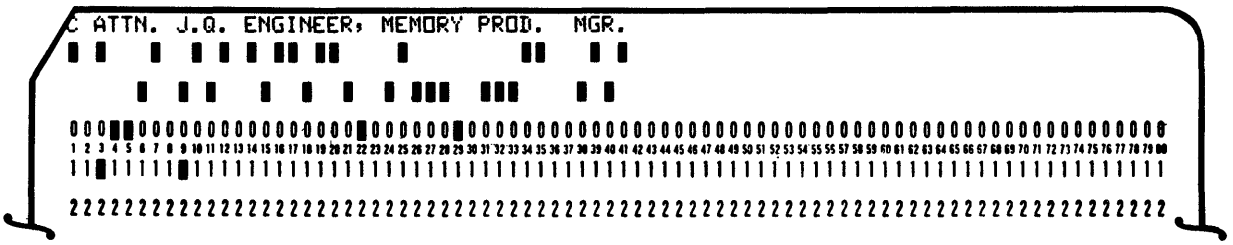
LEAVE COLS. 22, 23, 24, 25 BLANK
FOR ASSIGNMENT OF CM NO. BY SIGNETICS

BASIC PART TYPE

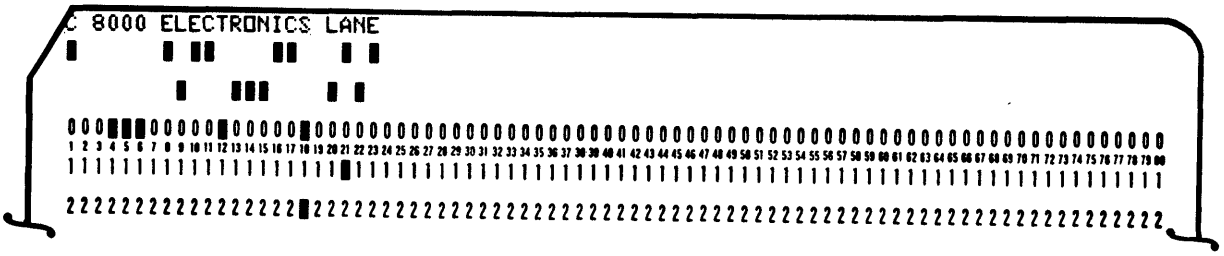
CUSTOMER P/N IDENTIFICATION



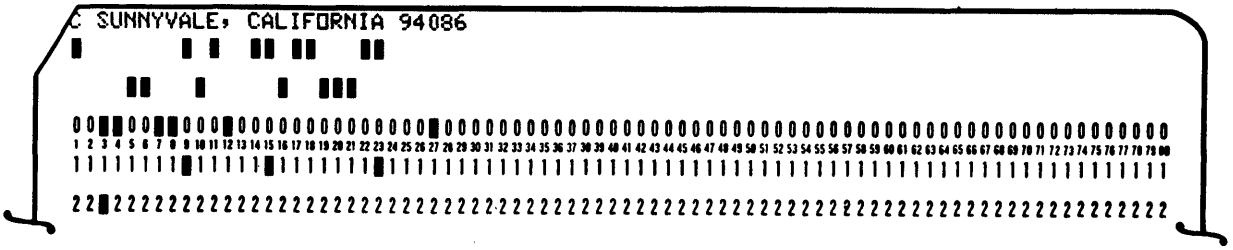
PERSON RESPONSIBLE FOR REVIEWING SIGNETICS
COMPUTER GENERATED TRUTH TABLE



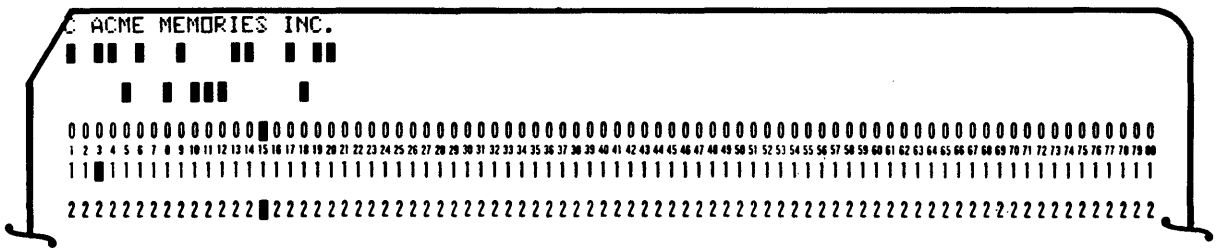
STREET ADDRESS



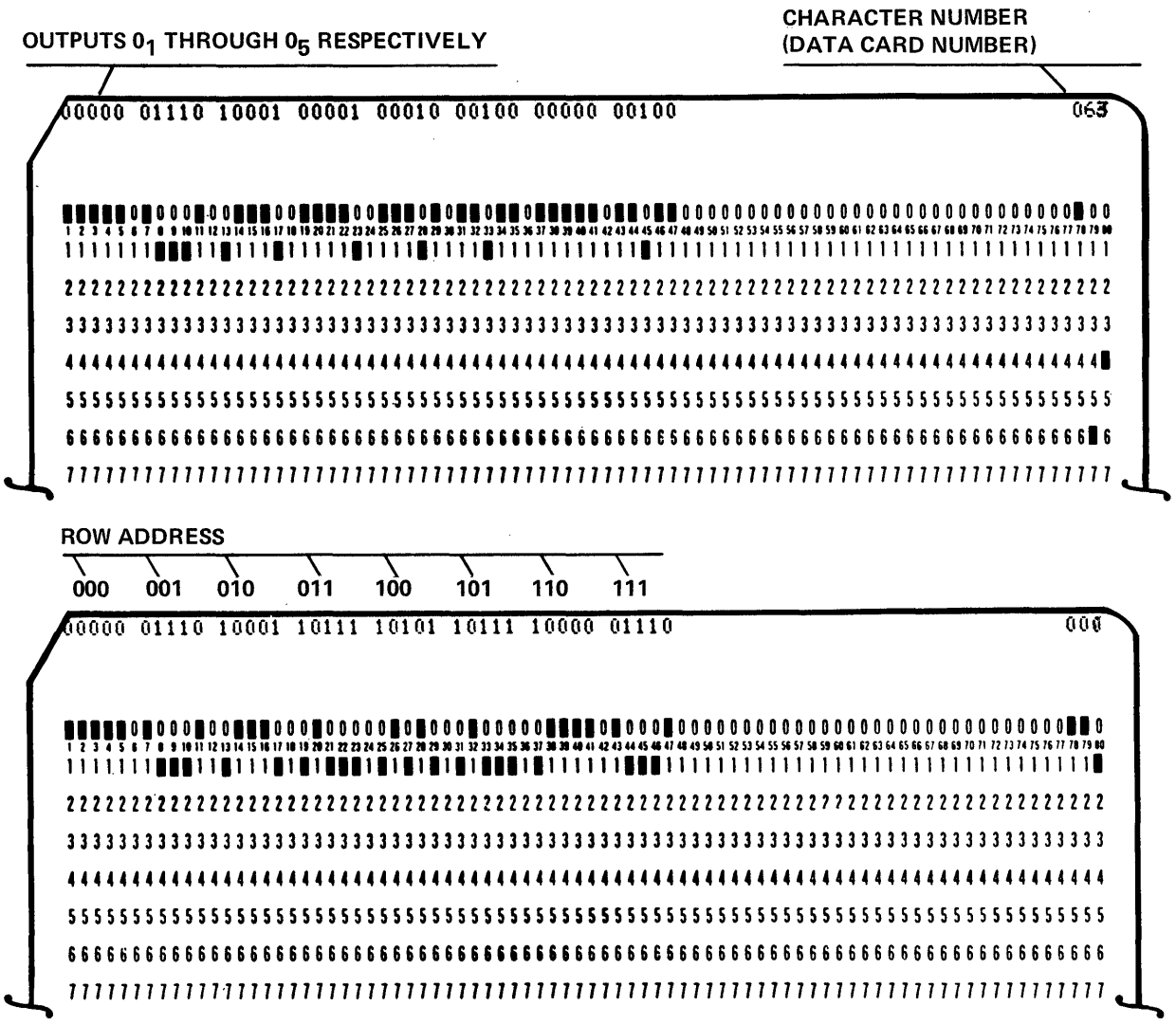
CITY STATE ZIP



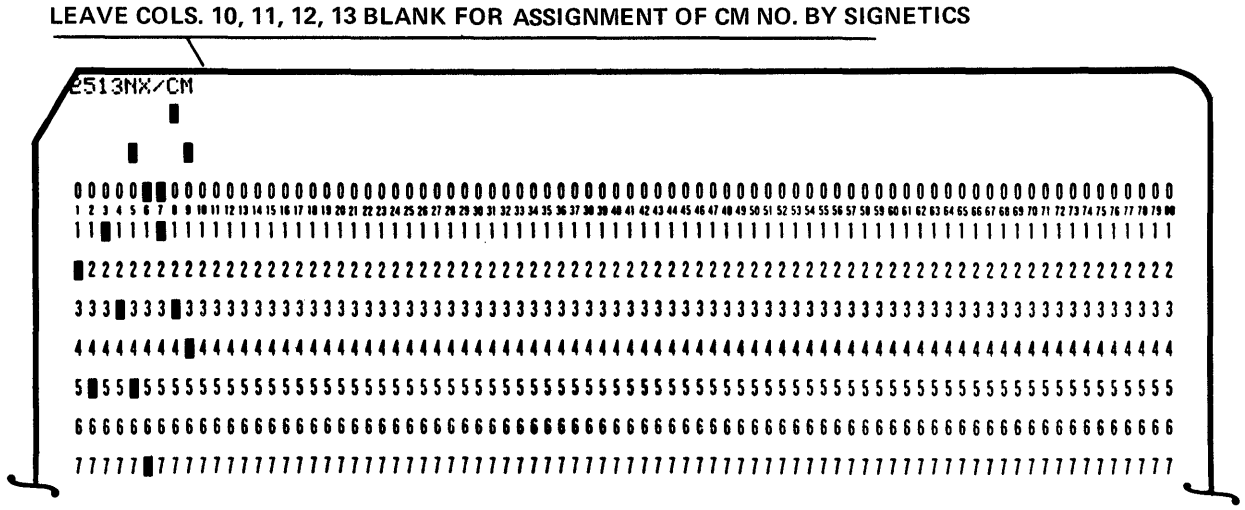
COMPANY NAME



DATA CARDS



BASIC DEVICE TYPE



NOTE:
"Character" number is in columns 78, 79, and 80. Note that each group of eight 5-bit words is treated as a character for convenience of coding.

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
0 0 0 0 0 0 0 0 0	000						
0 0 0 0 0 0 0 0 1	001						
0 0 0 0 0 0 0 1 0	002						
0 0 0 0 0 0 0 1 1	003						
0 0 0 0 0 0 1 0 0	004						
0 0 0 0 0 0 1 0 1	005						
0 0 0 0 0 0 1 1 0	006						
0 0 0 0 0 0 1 1 1	007						
0 0 0 0 0 1 0 0 0	008						
0 0 0 0 0 1 0 0 1	009						
0 0 0 0 0 1 0 1 0	010						
0 0 0 0 0 1 0 1 1	011						
0 0 0 0 0 1 1 0 0	012						
0 0 0 0 0 1 1 0 1	013						
0 0 0 0 0 1 1 1 0	014						
0 0 0 0 0 1 1 1 1	015						
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0 0 0 0 1 0 0 0 1	017						
0 0 0 0 1 0 0 1 0	018						
0 0 0 0 1 0 0 1 1	019						
0 0 0 0 1 0 1 0 0	020						
0 0 0 0 1 0 1 0 1	021						
0 0 0 0 1 0 1 1 0	022						
0 0 0 0 1 0 1 1 1	023						
0 0 0 0 1 1 0 0 0	024						
0 0 0 0 1 1 0 0 1	025						
0 0 0 0 1 1 0 1 0	026						
0 0 0 0 1 1 0 1 1	027						
0 0 0 0 1 1 1 0 0	028						
0 0 0 0 1 1 1 0 1	029						
0 0 0 0 1 1 1 1 0	030						
0 0 0 0 1 1 1 1 1	031						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
0 0 0 1 0 0 0 0 0	032						
0 0 0 1 0 0 0 0 1	033						
0 0 0 1 0 0 0 1 0	034						
0 0 0 1 0 0 0 1 1	035						
0 0 0 1 0 0 1 0 0	036						
0 0 0 1 0 0 1 0 1	037						
0 0 0 1 0 0 1 1 0	038						
0 0 0 1 0 0 1 1 1	039						
0 0 0 1 0 1 0 0 0	040						
0 0 0 1 0 1 0 0 1	041						
0 0 0 1 0 1 0 1 0	042						
0 0 0 1 0 1 0 1 1	043						
0 0 0 1 0 1 1 0 0	044						
0 0 0 1 0 1 1 0 1	045						
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0 0 0 1 0 1 1 1 1	047						
0 0 0 1 1 0 0 0 0	048						
0 0 0 1 1 0 0 0 1	049						
0 0 0 1 1 0 0 1 0	050						
0 0 0 1 1 0 0 1 1	051						
0 0 0 1 1 0 1 0 0	052						
0 0 0 1 1 0 1 0 1	053						
0 0 0 1 1 0 1 1 0	054						
0 0 0 1 1 0 1 1 1	055						
0 0 0 1 1 1 0 0 0	056						
0 0 0 1 1 1 0 0 1	057						
0 0 0 1 1 1 0 1 0	058						
0 0 0 1 1 1 0 1 1	059						
0 0 0 1 1 1 1 0 0	060						
0 0 0 1 1 1 1 0 1	061						
0 0 0 1 1 1 1 1 0	062						
0 0 0 1 1 1 1 1 1	063						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
0 0 1 0 0 0 0 0 0	064						
0 0 1 0 0 0 0 0 1	065						
0 0 1 0 0 0 0 1 0	066						
0 0 1 0 0 0 0 1 1	067						
0 0 1 0 0 0 1 0 0	068						
0 0 1 0 0 0 1 0 1	069						
0 0 1 0 0 0 1 1 0	070						
0 0 1 0 0 0 1 1 1	071						
0 0 1 0 0 1 0 0 0	072						
0 0 1 0 0 1 0 0 1	073						
0 0 1 0 0 1 0 1 0	074						
0 0 1 0 0 1 0 1 1	075						
0 0 1 0 0 1 1 0 0	076						
0 0 1 0 0 1 1 0 1	077						
0 0 1 0 0 1 1 1 0	078						
0 0 1 0 0 1 1 1 1	079						
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0 0 1 0 1 0 0 1 0	082						
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0 0 1 0 1 0 1 1 0	086						
0 0 1 0 1 0 1 1 1	087						
0 0 1 0 1 1 0 0 0	088						
0 0 1 0 1 1 0 0 1	089						
0 0 1 0 1 1 0 1 0	090						
0 0 1 0 1 1 0 1 1	091						
0 0 1 0 1 1 1 0 0	092						
0 0 1 0 1 1 1 0 1	093						
0 0 1 0 1 1 1 1 0	094						
0 0 1 0 1 1 1 1 1	095						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
0 0 1 1 0 0 0 0 0	096						
0 0 1 1 0 0 0 0 1	097						
0 0 1 1 0 0 0 1 0	098						
0 0 1 1 0 0 0 1 1	099						
0 0 1 1 0 0 1 0 0	100						
0 0 1 1 0 0 1 0 1	101						
0 0 1 1 0 0 1 1 0	102						
0 0 1 1 0 0 1 1 1	103						
0 0 1 1 0 1 0 0 0	104						
0 0 1 1 0 1 0 0 1	105						
0 0 1 1 0 1 0 1 0	106						
0 0 1 1 0 1 0 1 1	107						
0 0 1 1 0 1 1 0 0	108						
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0 0 1 1 0 1 1 1 0	110						
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0 0 1 1 1 0 0 0 0	112						
0 0 1 1 1 0 0 0 1	113						
0 0 1 1 1 0 0 1 0	114						
0 0 1 1 1 0 0 1 1	115						
0 0 1 1 1 0 1 0 0	116						
0 0 1 1 1 0 1 0 1	117						
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0 0 1 1 1 1 0 0 0	120						
0 0 1 1 1 1 0 0 1	121						
0 0 1 1 1 1 0 1 0	122						
0 0 1 1 1 1 0 1 1	123						
0 0 1 1 1 1 1 0 0	124						
0 0 1 1 1 1 1 0 1	125						
0 0 1 1 1 1 1 1 0	126						
0 0 1 1 1 1 1 1 1	127						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
0 1 0 0 0 0 0 0 0	128						
0 1 0 0 0 0 0 0 1	129						
0 1 0 0 0 0 0 1 0	130						
0 1 0 0 0 0 0 1 1	131						
0 1 0 0 0 0 1 0 0	132						
0 1 0 0 0 0 1 0 1	133						
0 1 0 0 0 0 1 1 0	134						
0 1 0 0 0 0 1 1 1	135						
0 1 0 0 0 1 0 0 0	136						
0 1 0 0 0 1 0 0 1	137						
0 1 0 0 0 1 0 1 0	138						
0 1 0 0 0 1 0 1 1	139						
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0 1 0 0 0 1 1 1 1	143						
0 1 0 0 1 0 0 0 0	144						
0 1 0 0 1 0 0 0 1	145						
0 1 0 0 1 0 0 1 0	146						
0 1 0 0 1 0 0 1 1	147						
0 1 0 0 1 0 1 0 0	148						
0 1 0 0 1 0 1 0 1	149						
0 1 0 0 1 0 1 1 0	150						
0 1 0 0 1 0 1 1 1	151						
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0 1 0 0 1 1 0 1 0	154						
0 1 0 0 1 1 0 1 1	155						
0 1 0 0 1 1 1 0 0	156						
0 1 0 0 1 1 1 0 1	157						
0 1 0 0 1 1 1 1 0	158						
0 1 0 0 1 1 1 1 1	159						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
0 1 0 1 0 0 0 0 0	160						
0 1 0 1 0 0 0 0 1	161						
0 1 0 1 0 0 0 1 0	162						
0 1 0 1 0 0 0 1 1	163						
0 1 0 1 0 0 1 0 0	164						
0 1 0 1 0 0 1 0 1	165						
0 1 0 1 0 0 1 1 0	166						
0 1 0 1 0 0 1 1 1	167						
0 1 0 1 0 1 0 0 0	168						
0 1 0 1 0 1 0 0 1	169						
0 1 0 1 0 1 0 1 0	170						
0 1 0 1 0 1 0 1 1	171						
0 1 0 1 0 1 1 0 0	172						
0 1 0 1 0 1 1 0 1	173						
0 1 0 1 0 1 1 1 0	174						
0 1 0 1 0 1 1 1 1	175						
0 1 0 1 1 0 0 0 0	176						
0 1 0 1 1 0 0 0 1	177						
0 1 0 1 1 0 0 1 0	178						
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0 1 0 1 1 0 1 0 1	181						
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0 1 0 1 1 1 0 0 0	184						
0 1 0 1 1 1 0 0 1	185						
0 1 0 1 1 1 0 1 0	186						
0 1 0 1 1 1 0 1 1	187						
0 1 0 1 1 1 1 0 0	188						
0 1 0 1 1 1 1 0 1	189						
0 1 0 1 1 1 1 1 0	190						
0 1 0 1 1 1 1 1 1	191						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
0 1 1 0 0 0 0 0 0	192						
0 1 1 0 0 0 0 0 1	193						
0 1 1 0 0 0 0 1 0	194						
0 1 1 0 0 0 0 1 1	195						
0 1 1 0 0 0 1 0 0	196						
0 1 1 0 0 0 1 0 1	197						
0 1 1 0 0 0 1 1 0	198						
0 1 1 0 0 0 1 1 1	199						
0 1 1 0 0 1 0 0 0	200						
0 1 1 0 0 1 0 0 1	201						
0 1 1 0 0 1 0 1 0	202						
0 1 1 0 0 1 0 1 1	203						
0 1 1 0 0 1 1 0 0	204						
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0 1 1 0 1 0 0 1 0	210						
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0 1 1 0 1 1 0 0 0	216						
0 1 1 0 1 1 0 0 1	217						
0 1 1 0 1 1 0 1 0	218						
0 1 1 0 1 1 0 1 1	219						
0 1 1 0 1 1 1 0 0	220						
0 1 1 0 1 1 1 0 1	221						
0 1 1 0 1 1 1 1 0	222						
0 1 1 0 1 1 1 1 1	223						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
0 1 1 1 0 0 0 0 0	224						
0 1 1 1 0 0 0 0 1	225						
0 1 1 1 0 0 0 1 0	226						
0 1 1 1 0 0 0 1 1	227						
0 1 1 1 0 0 1 0 0	228						
0 1 1 1 0 0 1 0 1	229						
0 1 1 1 0 0 1 1 0	230						
0 1 1 1 0 0 1 1 1	231						
0 1 1 1 0 1 0 0 0	232						
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0 1 1 1 1 1 0 0 0	248						
0 1 1 1 1 1 0 0 1	249						
0 1 1 1 1 1 0 1 0	250						
0 1 1 1 1 1 0 1 1	251						
0 1 1 1 1 1 1 0 0	252						
0 1 1 1 1 1 1 0 1	253						
0 1 1 1 1 1 1 1 0	254						
0 1 1 1 1 1 1 1 1	255						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
1 0 0 0 0 0 0 0 0	256						
1 0 0 0 0 0 0 0 1	257						
1 0 0 0 0 0 0 1 0	258						
1 0 0 0 0 0 0 1 1	259						
1 0 0 0 0 0 1 0 0	260						
1 0 0 0 0 0 1 0 1	261						
1 0 0 0 0 0 1 1 0	262						
1 0 0 0 0 0 1 1 1	263						
1 0 0 0 0 1 0 0 0	264						
1 0 0 0 0 1 0 0 1	265						
1 0 0 0 0 1 0 1 0	266						
1 0 0 0 0 1 0 1 1	267						
1 0 0 0 0 1 1 0 0	268						
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1 0 0 0 0 1 1 1 1	271						
1 0 0 0 1 0 0 0 0	272						
1 0 0 0 1 0 0 0 1	273						
1 0 0 0 1 0 0 1 0	274						
1 0 0 0 1 0 0 1 1	275						
1 0 0 0 1 0 1 0 0	276						
1 0 0 0 1 0 1 0 1	277						
1 0 0 0 1 0 1 1 0	278						
1 0 0 0 1 0 1 1 1	279						
1 0 0 0 1 1 0 0 0	280						
1 0 0 0 1 1 0 0 1	281						
1 0 0 0 1 1 0 1 0	282						
1 0 0 0 1 1 0 1 1	283						
1 0 0 0 1 1 1 0 0	284						
1 0 0 0 1 1 1 0 1	285						
1 0 0 0 1 1 1 1 0	286						
1 0 0 0 1 1 1 1 1	287						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
1 0 0 1 0 0 0 0 0	288						
1 0 0 1 0 0 0 0 1	289						
1 0 0 1 0 0 0 1 0	290						
1 0 0 1 0 0 0 1 1	291						
1 0 0 1 0 0 1 0 0	292						
1 0 0 1 0 0 1 0 1	293						
1 0 0 1 0 0 1 1 0	294						
1 0 0 1 0 0 1 1 1	295						
1 0 0 1 0 1 0 0 0	296						
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1 0 0 1 0 1 0 1 0	298						
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1 0 0 1 0 1 1 1 1	303						
1 0 0 1 1 0 0 0 0	304						
1 0 0 1 1 0 0 0 1	305						
1 0 0 1 1 0 0 1 0	306						
1 0 0 1 1 0 0 1 1	307						
1 0 0 1 1 0 1 0 0	308						
1 0 0 1 1 0 1 0 1	309						
1 0 0 1 1 0 1 1 0	310						
1 0 0 1 1 0 1 1 1	311						
1 0 0 1 1 1 0 0 0	312						
1 0 0 1 1 1 0 0 1	313						
1 0 0 1 1 1 0 1 0	314						
1 0 0 1 1 1 0 1 1	315						
1 0 0 1 1 1 1 0 0	316						
1 0 0 1 1 1 1 0 1	317						
1 0 0 1 1 1 1 1 0	318						
1 0 0 1 1 1 1 1 1	319						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
1 0 1 0 0 0 0 0 0	320						
1 0 1 0 0 0 0 0 1	321						
1 0 1 0 0 0 0 1 0	322						
1 0 1 0 0 0 0 1 1	323						
1 0 1 0 0 0 1 0 0	324						
1 0 1 0 0 0 1 0 1	325						
1 0 1 0 0 0 1 1 0	326						
1 0 1 0 0 0 1 1 1	327						
1 0 1 0 0 1 0 0 0	328						
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1 0 1 0 1 0 0 1 0	338						
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1 0 1 0 1 0 1 0 0	340						
1 0 1 0 1 0 1 0 1	341						
1 0 1 0 1 0 1 1 0	342						
1 0 1 0 1 0 1 1 1	343						
1 0 1 0 1 1 0 0 0	344						
1 0 1 0 1 1 0 0 1	345						
1 0 1 0 1 1 0 1 0	346						
1 0 1 0 1 1 0 1 1	347						
1 0 1 0 1 1 1 0 0	348						
1 0 1 0 1 1 1 0 1	349						
1 0 1 0 1 1 1 1 0	350						
1 0 1 0 1 1 1 1 1	351						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
1 0 1 1 0 0 0 0 0	352						
1 0 1 1 0 0 0 0 1	353						
1 0 1 1 0 0 0 1 0	354						
1 0 1 1 0 0 0 1 1	355						
1 0 1 1 0 0 1 0 0	356						
1 0 1 1 0 0 1 0 1	357						
1 0 1 1 0 0 1 1 0	358						
1 0 1 1 0 0 1 1 1	359						
1 0 1 1 0 1 0 0 0	360						
1 0 1 1 0 1 0 0 1	361						
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1 0 1 1 1 0 0 1 0	370						
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1 0 1 1 1 0 1 0 0	372						
1 0 1 1 1 0 1 0 1	373						
1 0 1 1 1 0 1 1 0	374						
1 0 1 1 1 0 1 1 1	375						
1 0 1 1 1 1 0 0 0	376						
1 0 1 1 1 1 0 0 1	377						
1 0 1 1 1 1 0 1 0	378						
1 0 1 1 1 1 0 1 1	379						
1 0 1 1 1 1 1 0 0	380						
1 0 1 1 1 1 1 0 1	381						
1 0 1 1 1 1 1 1 0	382						
1 0 1 1 1 1 1 1 1	383						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
1 1 0 0 0 0 0 0 0	384						
1 1 0 0 0 0 0 0 1	385						
1 1 0 0 0 0 0 1 0	386						
1 1 0 0 0 0 0 1 1	387						
1 1 0 0 0 0 1 0 0	388						
1 1 0 0 0 0 1 0 1	389						
1 1 0 0 0 0 1 1 0	390						
1 1 0 0 0 0 1 1 1	391						
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1 1 0 0 1 0 0 0 0	400						
1 1 0 0 1 0 0 0 1	401						
1 1 0 0 1 0 0 1 0	402						
1 1 0 0 1 0 0 1 1	403						
1 1 0 0 1 0 1 0 0	404						
1 1 0 0 1 0 1 0 1	405						
1 1 0 0 1 0 1 1 0	406						
1 1 0 0 1 0 1 1 1	407						
1 1 0 0 1 1 0 0 0	408						
1 1 0 0 1 1 0 0 1	409						
1 1 0 0 1 1 0 1 0	410						
1 1 0 0 1 1 0 1 1	411						
1 1 0 0 1 1 1 0 0	412						
1 1 0 0 1 1 1 0 1	413						
1 1 0 0 1 1 1 1 0	414						
1 1 0 0 1 1 1 1 1	415						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
1 1 0 1 0 0 0 0 0	416						
1 1 0 1 0 0 0 0 1	417						
1 1 0 1 0 0 0 1 0	418						
1 1 0 1 0 0 0 1 1	419						
1 1 0 1 0 0 1 0 0	420						
1 1 0 1 0 0 1 0 1	421						
1 1 0 1 0 0 1 1 0	422						
1 1 0 1 0 0 1 1 1	423						
1 1 0 1 0 1 0 0 0	424						
1 1 0 1 0 1 0 0 1	425						
1 1 0 1 0 1 0 1 0	426						
1 1 0 1 0 1 0 1 1	427						
1 1 0 1 0 1 1 0 0	428						
1 1 0 1 0 1 1 0 1	429						
1 1 0 1 0 1 1 1 0	430						
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1 1 0 1 1 0 0 1 0	434						
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1 1 0 1 1 1 0 0 0	440						
1 1 0 1 1 1 0 0 1	441						
1 1 0 1 1 1 0 1 0	442						
1 1 0 1 1 1 0 1 1	443						
1 1 0 1 1 1 1 0 0	444						
1 1 0 1 1 1 1 0 1	445						
1 1 0 1 1 1 1 1 0	446						
1 1 0 1 1 1 1 1 1	447						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
1 1 1 0 0 0 0 0 0	448						
1 1 1 0 0 0 0 0 1	449						
1 1 1 0 0 0 0 1 0	450						
1 1 1 0 0 0 0 1 1	451						
1 1 1 0 0 0 1 0 0	452						
1 1 1 0 0 0 1 0 1	453						
1 1 1 0 0 0 1 1 0	454						
1 1 1 0 0 0 1 1 1	455						
1 1 1 0 0 1 0 0 0	456						
1 1 1 0 0 1 0 0 1	457						
1 1 1 0 0 1 0 1 0	458						
1 1 1 0 0 1 0 1 1	459						
1 1 1 0 0 1 1 0 0	460						
1 1 1 0 0 1 1 0 1	461						
1 1 1 0 0 1 1 1 0	462						
1 1 1 0 0 1 1 1 1	463						
1 1 1 0 1 0 0 0 0	464						
1 1 1 0 1 0 0 0 1	465						
1 1 1 0 1 0 0 1 0	466						
1 1 1 0 1 0 0 1 1	467						
1 1 1 0 1 0 1 0 0	468						
1 1 1 0 1 0 1 0 1	469						
1 1 1 0 1 0 1 1 0	470						
1 1 1 0 1 0 1 1 1	471						
1 1 1 0 1 1 0 0 0	472						
1 1 1 0 1 1 0 0 1	473						
1 1 1 0 1 1 0 1 0	474						
1 1 1 0 1 1 0 1 1	475						
1 1 1 0 1 1 1 0 0	476						
1 1 1 0 1 1 1 0 1	477						
1 1 1 0 1 1 1 1 0	478						
1 1 1 0 1 1 1 1 1	479						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
1 1 1 1 0 0 0 0 0	480						
1 1 1 1 0 0 0 0 1	481						
1 1 1 1 0 0 0 1 0	482						
1 1 1 1 0 0 0 1 1	483						
1 1 1 1 0 0 1 0 0	484						
1 1 1 1 0 0 1 0 1	485						
1 1 1 1 0 0 1 1 0	486						
1 1 1 1 0 0 1 1 1	487						
1 1 1 1 0 1 0 0 0	488						
1 1 1 1 0 1 0 0 1	489						
1 1 1 1 0 1 0 1 0	490						
1 1 1 1 0 1 0 1 1	491						
1 1 1 1 0 1 1 0 0	492						
1 1 1 1 0 1 1 0 1	493						
1 1 1 1 0 1 1 1 0	494						
1 1 1 1 0 1 1 1 1	495						
1 1 1 1 1 0 0 0 0	496						
1 1 1 1 1 0 0 0 1	497						
1 1 1 1 1 0 0 1 0	498						
1 1 1 1 1 0 0 1 1	499						
1 1 1 1 1 0 1 0 0	500						
1 1 1 1 1 0 1 0 1	501						
1 1 1 1 1 0 1 1 0	502						
1 1 1 1 1 0 1 1 1	503						
1 1 1 1 1 1 0 0 0	504						
1 1 1 1 1 1 0 0 1	505						
1 1 1 1 1 1 0 1 0	506						
1 1 1 1 1 1 0 1 1	507						
1 1 1 1 1 1 1 0 0	508						
1 1 1 1 1 1 1 0 1	509						
1 1 1 1 1 1 1 1 0	510						
1 1 1 1 1 1 1 1 1	511						

COMPANY _____

ADDRESS _____

CITY _____ STATE _____ ZIP ____

TELEPHONE _____

AUTHORIZED SIGNATURE _____

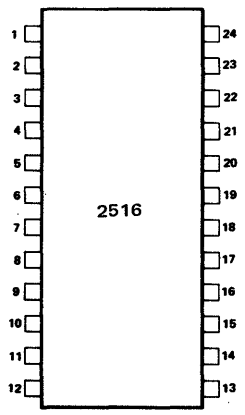
DATE _____

CUSTOMER PRINT OR ID NO. _____

PURCHASE ORDER NUMBER _____

CUSTOM PATTERN NUMBER (TO BE ENTERED BY SIGNETICS) _____

PIN CONFIGURATION



1. Chip Enable
2. NC
3. Output 8
4. Output 7
5. Output 6
6. Output 5
7. Output 4
8. Output 3
9. Output 2
10. Output 1
11. V_{DD} 2*
12. V_{DD}
24. V_{CC}
23. V_{GG}
22. Address 9
21. Address 8
20. Address 7
19. Address 6
18. Address 5
17. Address 4
16. Address 3
15. Address 2
14. Address 1
13. Chip Enable 2*

*Optional on all custom ROMs (NC on CM 2150)

INTRODUCTION

The Signetics 2516 is a high speed silicon gate MOS read-only memories whose organization is specially suited for 64 X 6 X 8 vertical scan character generation.

MAJOR FEATURES OF THE 2516

- 64 X 6 X 8 CHARACTER MATRIX
- COLUMN OUTPUT
- ACCESS TIME 450ns TYPICALLY
- STATIC OPERATION
- TTL/DTL COMPATIBLE
- TRI-STATE OUTPUTS (HIGH-LOW-DISCONNECTED) FOR POWERFUL BUSSING CAPABILITY
- +5, -5, -12V POWER SUPPLIES
- 24-PIN SIGNETICS SILICONE DIP
- SIGNETICS SILICON GATE PROCESS TECHNOLOGY FOR PERFORMANCE AND RELIABILITY

ORGANIZATION AS CHARACTER GENERATOR

A six-bit binary address (A_4 through A_9) selects 1-of-64 matrix characters arranged 6 dots horizontally and 8 dots vertically. A three bit-binary address code (A_1 through A_3) selects 1 or 6 columns. Eight outputs display a complete column of the character matrix. See Figure 1.

CHARACTER FORMAT

ROW ADDRESS

COLUMN ADDRESS							
	A_3	0	0	0	0	1	1
	A_2	0	0	1	1	0	0
	A_1	0	1	0	1	0	1

0	0	0	0	0	0	O_1
0	0	1	1	1	0	O_2
0	1	0	0	0	1	O_3
0	1	0	0	0	0	O_4
0	0	1	1	1	0	O_5
0	0	0	0	0	1	O_6
0	1	0	0	0	1	O_7
0	0	1	1	1	0	O_8

EXAMPLE "S"

FIGURE 1

CHARACTER ADDRESS

	CHARACTER ADDRESS					
	A_4	A_5	A_6	A_7	A_8	A_9
ASCII CHARACTER	1	1	0	0	1	0

FIGURE 2

STANDARD PATTERN

A standard ASCII Character Font is available for the 2516. This device (2516NX/CM2150) may be used for ASCII character generation or for device evaluation.

CUSTOM DEVICES

For unique custom memory patterns, this form should be used to transmit coding instructions. The nomenclature for custom device will consist of the basic product type followed by a unique "CM" number assigned by Signetics. For example, "2516NX/CM2151".

- **Programming with punched cards.**
  For maximum accuracy and minimum cost and turnaround time, the truth table should be transmitted to Signetics in the form of punched cards according to the format indicated on the following pages.
- **Programming with written truth table.**
  When punched data cards cannot be supplied, the truth table may be transmitted in written form using the attached blank truth table.

VERIFICATION

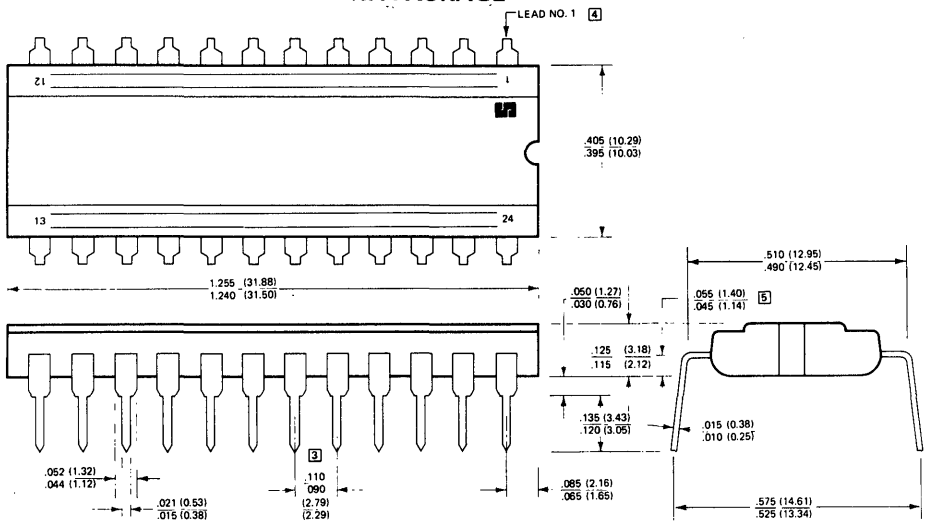
Upon receipt of either punched card or written truth table information, Signetics will prepare a computer tabulation of the instructions and return to the address indicated. If errors are detected, they should be transmitted to Signetics as quickly as possible.

LOGIC CONVENTION

Logic "1"s or blackened squares in the truth table will result in "high" output from the indicated output terminal (i.e. +3.6V minimum). Similarly, a "1" address input level is interpreted as +3.2V minimum.

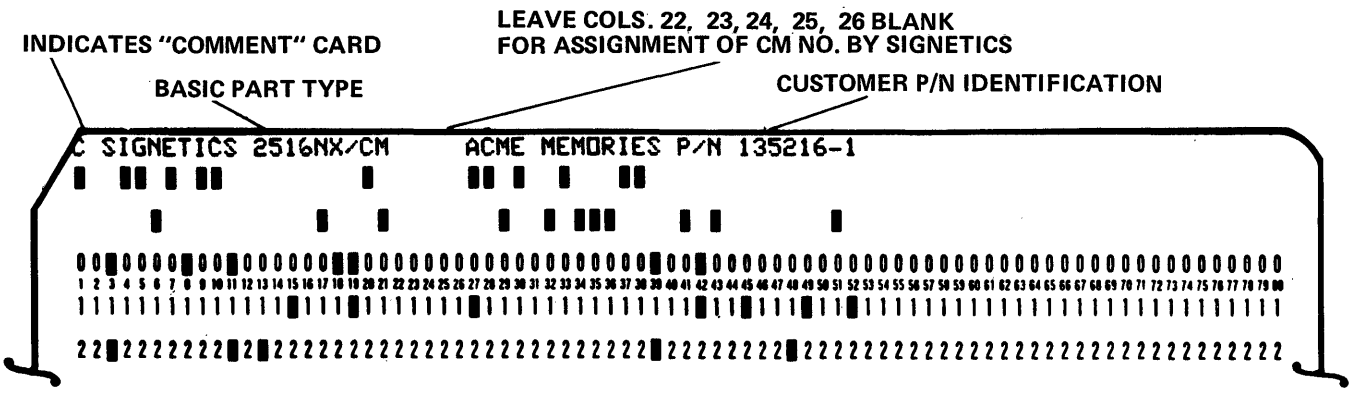
PACKAGE INFORMATION

NX PACKAGE



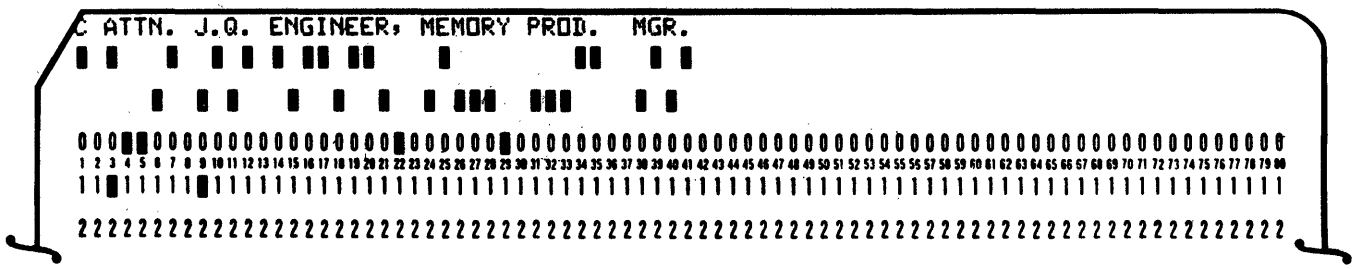
NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: SILICONE MOLDED.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: Θ Ja = .12 C/mW, Θ Jc = .05 C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

IDENTIFICATION CARDS

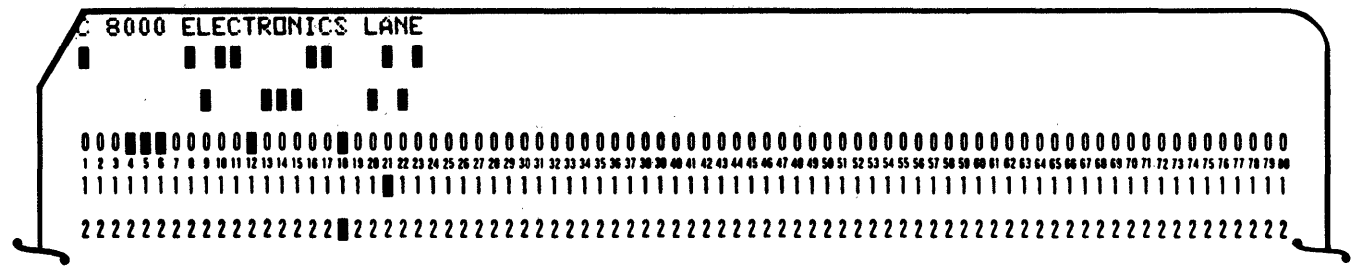


IDENTIFICATION CARDS(Cont'd)

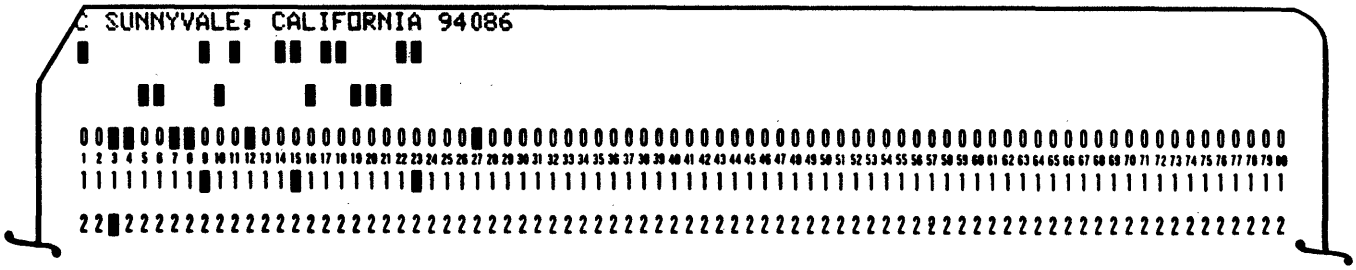
PERSON RESPONSIBLE FOR REVIEWING SIGNETICS
COMPUTER GENERATED TRUTH TABLE



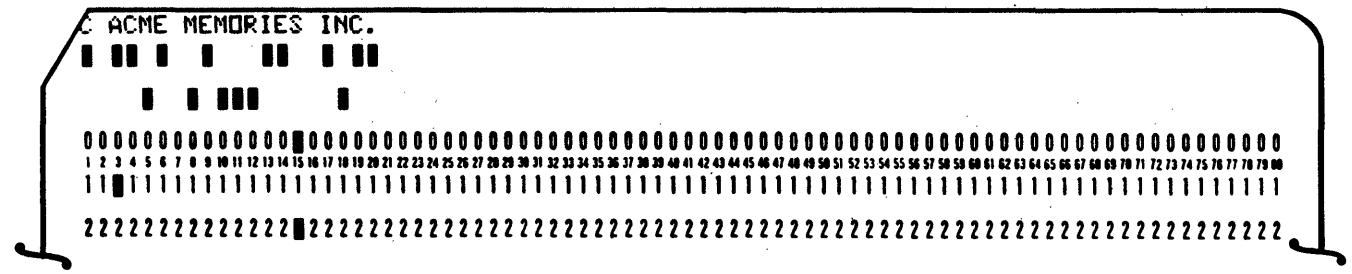
STREET ADDRESS



CITY STATE ZIP



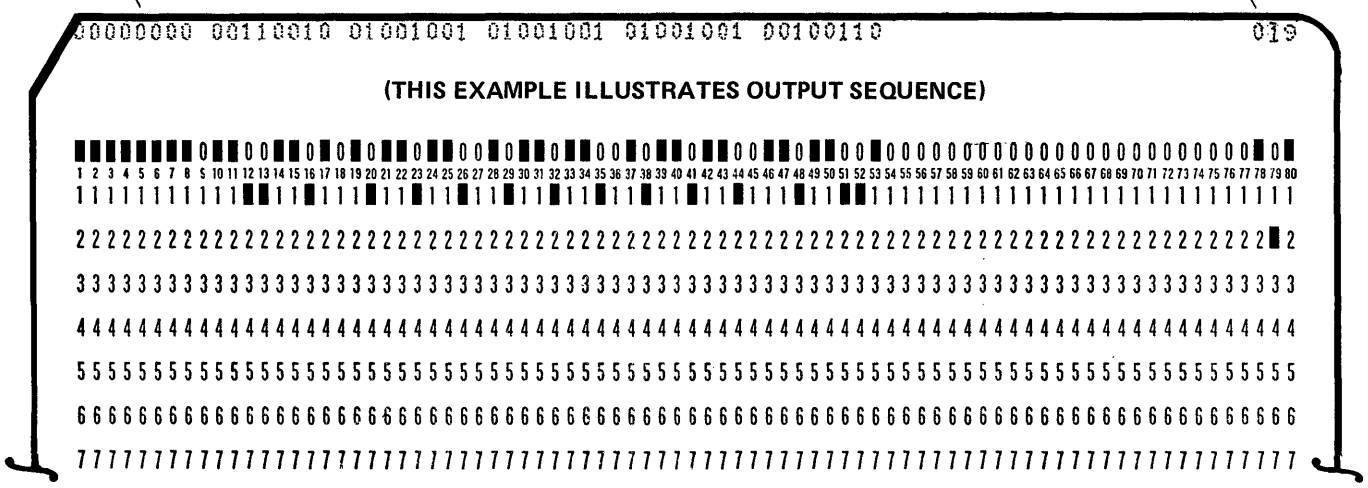
COMPANY NAME



DATA CARDS

OUTPUTS O_8 THROUGH O_1 RESPECTIVELY

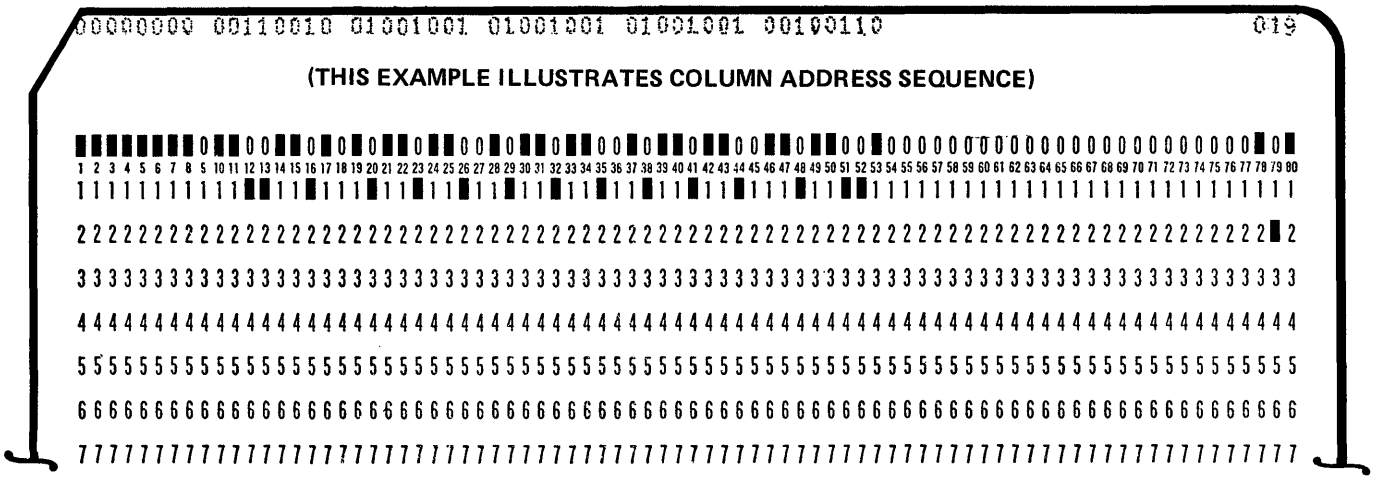
DECIMAL CHARACTER ADDRESS
(DATA CARD NUMBER 001 THRU 064)



(THIS EXAMPLE ILLUSTRATES OUTPUT SEQUENCE)

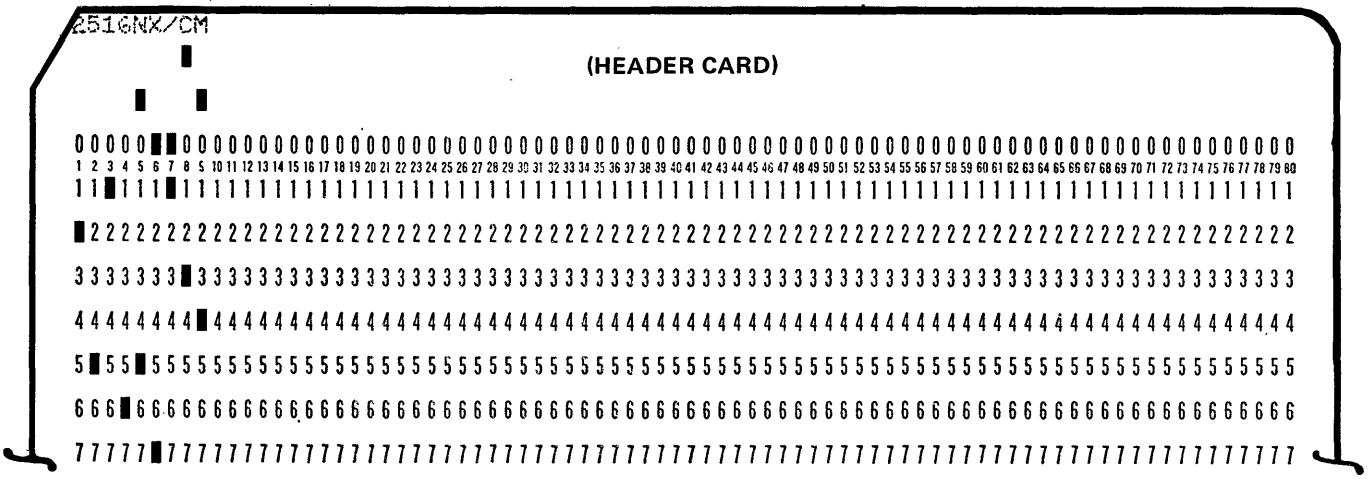
COLUMN ADDRESS(A_3,A_2,A_1)

000 001 010 011 100 101



(THIS EXAMPLE ILLUSTRATES COLUMN ADDRESS SEQUENCE)

BASIC DEVICE TYPE
LEAVE COLS. 10, 11, 12, 13 BLANK FOR ASSIGNMENT OF CM NO. BY SIGNETICS



(HEADER CARD)

NOTE

"Character" number is in columns 78, 79, and 80.

Character Number	001					
Column Binary Address	Column Decimal Address					
	000	001	002	003	004	005
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	002					
Column Binary Address	Column Decimal Address					
	008	009	010	011	012	013
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	003					
Column Binary Address	Column Decimal Address					
	016	017	018	019	020	021
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	004					
Column Binary Address	Column Decimal Address					
	024	025	026	027	028	029
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	005					
Column Binary Address	Column Decimal Address					
	032	033	034	035	036	037
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	006					
Column Binary Address	Column Decimal Address					
	040	041	042	043	044	045
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	007					
Column Binary Address	Column Decimal Address					
	048	049	050	051	052	053
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	008					
Column Binary Address	Column Decimal Address					
	056	057	058	059	060	061
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 009						
Column Binary Address	Column Decimal Address					
	064	065	066	067	068	069
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 010						
Column Binary Address	Column Decimal Address					
	072	073	074	075	076	077
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 011						
Column Binary Address	Column Decimal Address					
	080	081	082	083	084	085
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 012						
Column Binary Address	Column Decimal Address					
	088	089	090	091	092	093
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 013						
Column Binary Address	Column Decimal Address					
	096	097	098	099	100	101
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 014						
Column Binary Address	Column Decimal Address					
	104	105	106	107	108	109
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 015						
Column Binary Address	Column Decimal Address					
	112	113	114	115	116	117
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 016						
Column Binary Address	Column Decimal Address					
	120	121	122	123	124	125
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 017						
Column Binary Address	Column Decimal Address					
	128	129	130	131	132	133
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 018						
Column Binary Address	Column Decimal Address					
	136	137	138	139	140	141
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 019						
Column Binary Address	Column Decimal Address					
	144	145	146	147	148	149
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 020						
Column Binary Address	Column Decimal Address					
	152	153	154	155	156	157
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 021						
Column Binary Address	Column Decimal Address					
	160	161	162	163	164	165
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 022						
Column Binary Address	Column Decimal Address					
	168	169	170	171	172	173
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 023						
Column Binary Address	Column Decimal Address					
	176	177	178	179	180	181
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 024						
Column Binary Address	Column Decimal Address					
	184	185	186	187	188	189
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 025						
Column Binary Address	Column Decimal Address					
	192	193	194	195	196	197
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 026						
Column Binary Address	Column Decimal Address					
	200	201	202	203	204	205
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 027						
Column Binary Address	Column Decimal Address					
	208	209	210	211	212	213
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 028						
Column Binary Address	Column Decimal Address					
	216	217	218	219	220	221
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 029						
Column Binary Address	Column Decimal Address					
	224	225	226	227	228	229
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 030						
Column Binary Address	Column Decimal Address					
	232	233	234	235	236	237
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 031						
Column Binary Address	Column Decimal Address					
	240	241	242	243	244	245
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 032						
Column Binary Address	Column Decimal Address					
	248	249	250	251	252	253
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 033	Column Decimal Address					
Column Binary Address	256	257	258	259	260	261
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 034	Column Decimal Address					
Column Binary Address	264	265	266	267	268	269
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 035	Column Decimal Address					
Column Binary Address	272	273	274	275	276	277
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 036	Column Decimal Address					
Column Binary Address	280	281	282	283	284	285
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 037	Column Decimal Address					
Column Binary Address	288	289	290	291	292	293
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 038	Column Decimal Address					
Column Binary Address	296	297	298	299	300	301
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 039	Column Decimal Address					
Column Binary Address	304	305	306	307	308	309
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 040	Column Decimal Address					
Column Binary Address	312	313	314	315	316	317
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	041					
Column Binary Address	Column Decimal Address					
	320	321	322	323	324	325
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	042					
Column Binary Address	Column Decimal Address					
	328	329	330	331	332	333
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	043					
Column Binary Address	Column Decimal Address					
	336	337	338	339	340	341
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	044					
Column Binary Address	Column Decimal Address					
	344	345	346	347	348	349
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	045					
Column Binary Address	Column Decimal Address					
	352	353	354	355	356	357
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	046					
Column Binary Address	Column Decimal Address					
	360	361	362	363	364	365
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	047					
Column Binary Address	Column Decimal Address					
	368	369	370	371	372	373
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	048					
Column Binary Address	Column Decimal Address					
	376	377	378	379	380	381
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	049					
Column Binary Address	Column Decimal Address					
	384	385	386	387	388	389
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	050					
Column Binary Address	Column Decimal Address					
	392	393	394	395	396	397
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	051					
Column Binary Address	Column Decimal Address					
	400	401	402	403	404	405
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	052					
Column Binary Address	Column Decimal Address					
	408	409	410	411	412	413
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	053					
Column Binary Address	Column Decimal Address					
	416	417	418	419	420	421
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	054					
Column Binary Address	Column Decimal Address					
	424	425	426	427	428	429
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	055					
Column Binary Address	Column Decimal Address					
	432	433	434	435	436	437
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	056					
Column Binary Address	Column Decimal Address					
	440	441	442	443	444	445
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 057						
Column Binary Address	Column Decimal Address					
	448	449	450	451	452	453
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 058						
Column Binary Address	Column Decimal Address					
	456	457	458	459	460	461
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 059						
Column Binary Address	Column Decimal Address					
	464	465	466	467	468	469
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 060						
Column Binary Address	Column Decimal Address					
	472	473	474	475	476	477
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 061						
Column Binary Address	Column Decimal Address					
	480	481	482	483	484	485
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 062						
Column Binary Address	Column Decimal Address					
	488	489	490	491	492	493
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 063						
Column Binary Address	Column Decimal Address					
	496	497	498	499	500	501
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 064						
Column Binary Address	Column Decimal Address					
	504	505	506	507	508	509
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

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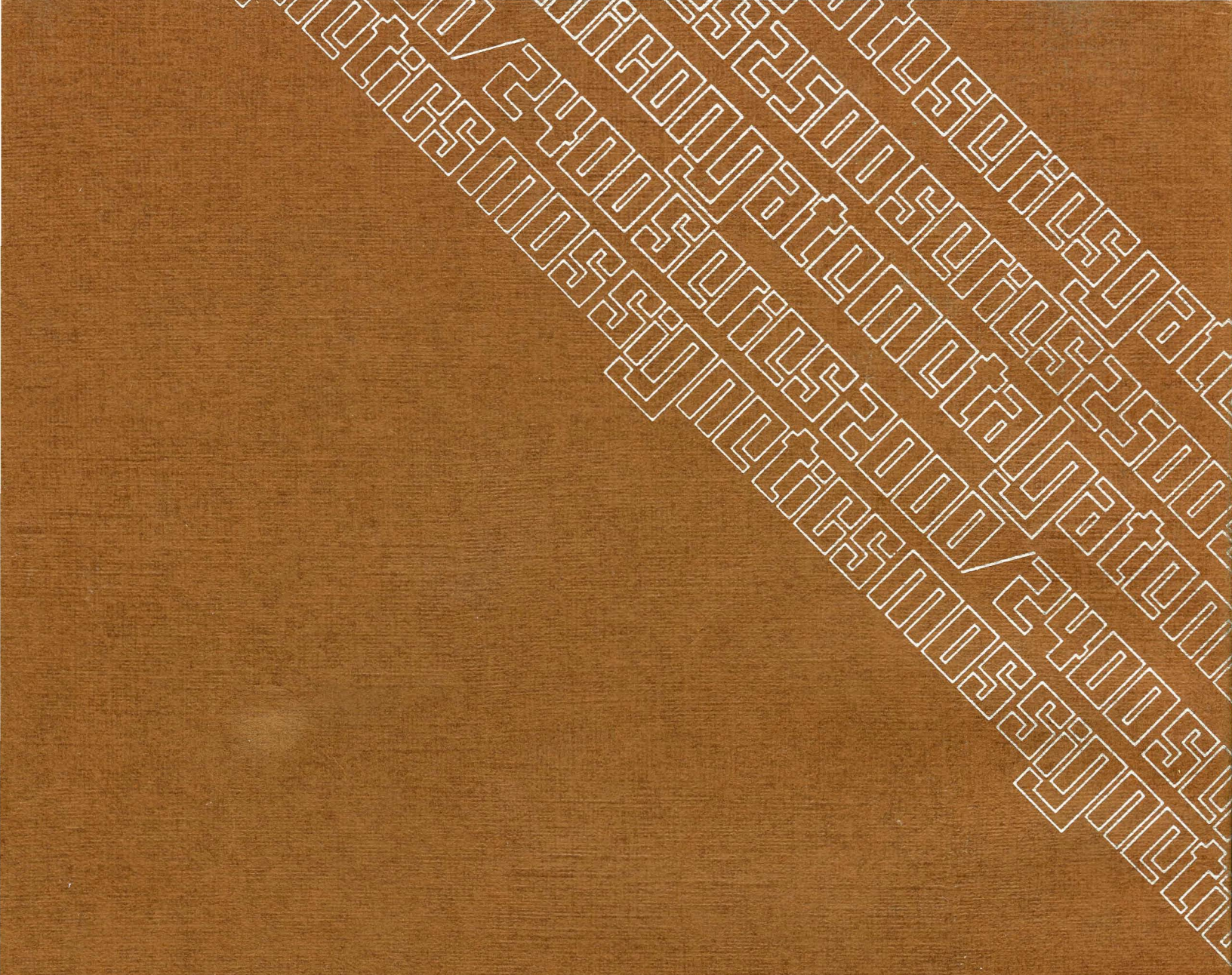

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